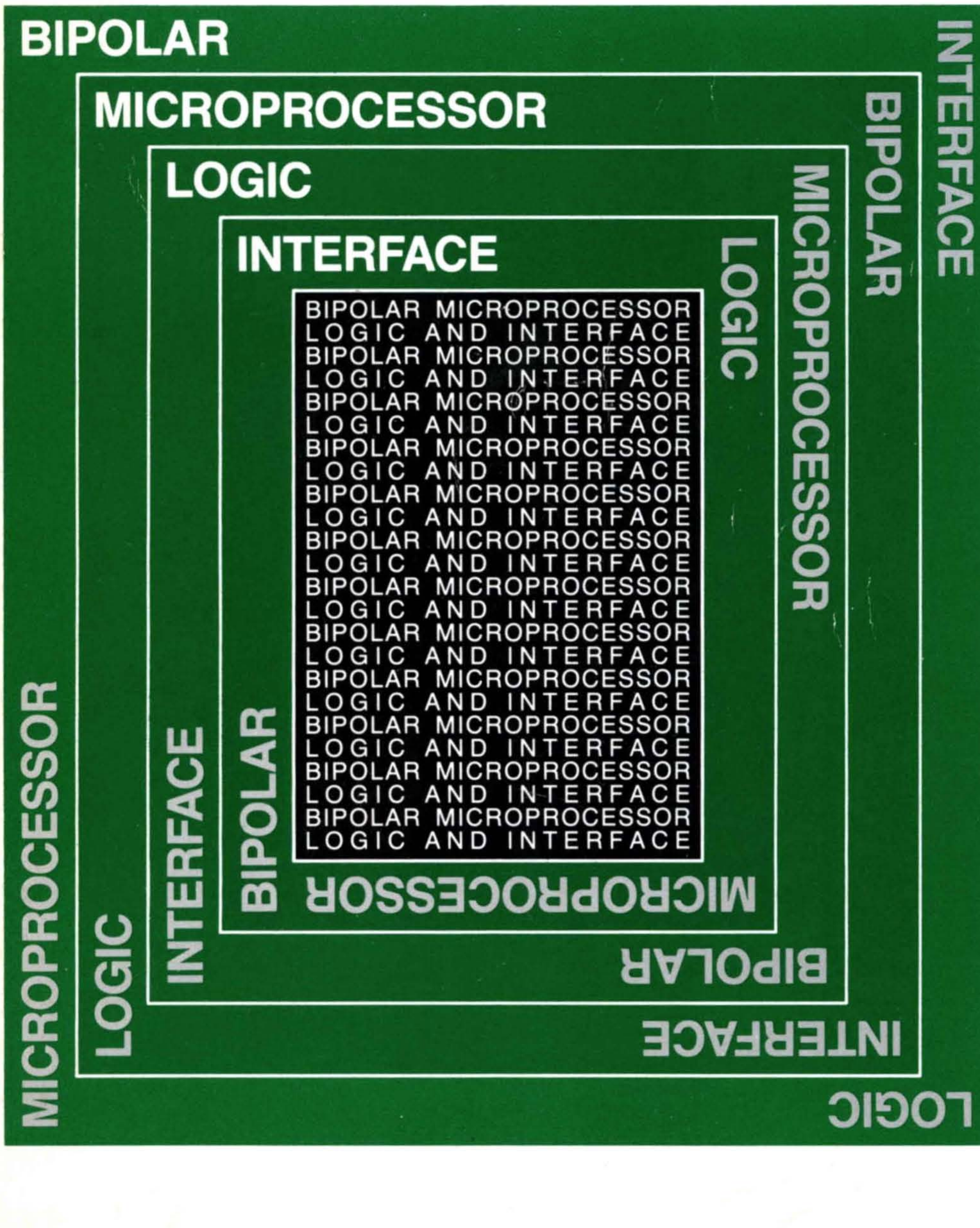
Bipolar Microprocessor Logic and Interface

Am2900 Family
1983 Data Book



ADVANCED MICRO DEVICES

Advanced Micro Devices

Bipolar Microprocessor Logic and Interface Data Book

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Bipolar Technologies

Advanced Micro Devices emphasizes Research and Development expenditures for developing the most advanced technologies for Bipolar processing, circuit design, and Very Large Scale Integration (VLSI).

Today, Advanced Micro Devices' bipolar products combine ECL-internal circuitry, the super high performance IMOX™ process, and VLSI integration to offer the system designer the most compact high performance integrated circuits. This, plus AMD's systems solution approach to design problems, makes the Am2900 Family the best choice for fastest applications.

IMOX

First introduced in 1980, IMOX is the name of Advanced Micro Devices' proprietary bipolar process. IMOX is an acronym which means: 1) Ion-IMplantation of dopants for tighter parameter control and lower power consumption; and, 2) OXide-isolation of transistor structures which results in faster transistor switching and tighter packing. Older, LS-type processes used diffused isolation for isolating transistor structures; this had the disadvantage of a large die area and high parasitic capacitance.

AMD is also applying IMOX to bring out higher-speed versions of earlier Am2900 devices. Figure 1 shows the evolution of the Am2901 Four-bit Microprocessor Slice. First introduced in 1975, the Am2901 has been repeatedly redesigned and is now available in the IMOX Am2901C version, which is less than half the size and more than twice the speed of the original Am2901 – and costs less. The current generation IMOX process has an 8 micron pitch (pitch equals the total of the width of metal lines plus the spacings between metal lines). In 1983, AMD is bringing into full scale production a completely new Fabrication Facility in San Antonio, Texas which will feature the state-of-the-art in process and masking equipment, and allow products which feature the IMOX process but with a pitch of only 4 microns, by late 1983. This version of IMOX is termed IMOX-S2. The 50% reduction in metal pitch will dramatically increase the level of integration of new products and also provides >30% increase in device speed.

ECL-INTERNAL CIRCUITRY

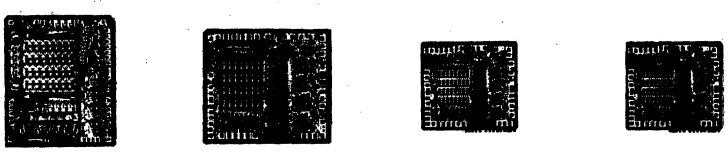
All Am2900 devices today are TTL-compatible on inputs and outputs and use standard +5V and ground for supply voltages. TTL is a good interface standard for systems design today, but TTL gates are slow, and ECL gates are much faster. To offer TTL-compatibility but near-ECL speeds to our customers, AMD has adopted a circuit design approach which features all ECL-circuitry for the internal circuitry of all LSI and VLSI devices (see Figure 2).

This approach, ECL-internal circuitry, provides near-ECL speeds to TTL-I/O designers. Of course the ECL gate structures inside the device are completely transparent to system designers because of the 100% adherence to TTL standards for I/O specs. Also, these chips only require +5V and ground because internal gates are not the same type of ECL gates as those used with 10K or 100K logic. The final point to note is that ECL has a reputation for being very power intensive. While the Am2900 Family are not low-power devices, they do significantly reduce the total power usage in a high performance

Figure 1. Bipolar Speed/Density Improvements

Am2901 FOUR-BIT MICROPROCESSOR SLICE

540 GATES
800mW
40-PIN DIP



DIE SIZE	Am2901 33,000 MILS^2	Am2901A 20,000 MILS^2	Am2901B 15,000 MILS^2	Am2901C 15,000 MILS^2
SPEED A, B G, P	80ns	65ns	50ns	**37ns**
TECHNOLOGY	LOW-POWER SCHOTTKY	DUAL LAYER METAL ION-IMPLANTATION	PROJECTION PRINTING	ECL INTERNAL TTL I/O IMOX
	1975	1977	1978	1981

MPL-076

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systems design because of the large number of SSI/MSI devices they replace. These ECL gates are not run at the very high power levels of traditional ECL circuits.

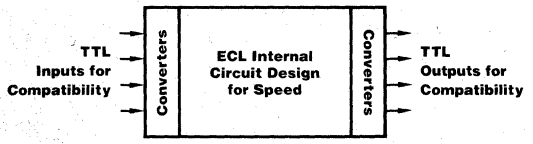
Using internal ECL with TTL-I/O does involve paying a translation speed penalty at the inputs and outputs of the device, but because these devices are LSI and VLSI with many levels of internal gating between input and output, the translation penalty is more than compensated for by the extra performance gained by the multiple layers of high speed ECL gates. Figure 3 shows an approximate comparison of the IMOX-with-internal-ECL approach to other process/circuit offerings available to designers utilizing high speed. TTL-compatible ICs. IMOX offers an excellent combination of high speed and relatively low power. The speed comes not only from the IMOX process but also from the use of ECL gates for internal circuitry. The FAST and AS/ALS Families are populated primarily with MSI devices where ECL-internal gating is not feasible due to the few layers of internal gating relative to the TTL/ECL translation delay penalty. Note also that Am2900/IMOX devices use an order of magnitude less power per gate than traditional ECL 10K and 100K devices.

BIPOLAR VLSI

Advanced Micro Devices is the leader in high integration, high performance integrated circuits. Our largest device to date, the Am29116, is a 2500-gate device measuring 68,000 square mils in area, and currently in development are devices of four times that complexity using our new IMOX-S2 process. AMD's emphasis on Very Large Scale Integration bipolar is best illustrated in Figure 4 below.

Figure 4 demonstrates AMD's commitment and leadership in large scale integration bipolar since the introduction of the original Am2901 in 1975. Another graphic demonstration of the growing complexity of our devices is the relative die sizes of successively complex arithmetic processors, as shown in Figure 5.

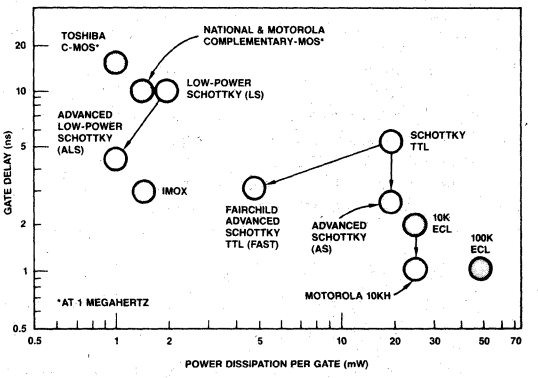
Figure 2. Am2900 Circuit Design for Maximum Speed



- **All ECL would only be 7-15% faster**
- **Practical approach for LSI/VLSI**

MPL-077

Figure 3.



SOURCE: MOTOROLA AND *ELECTRONICS*

MPL-078

Figure 4. Am2900 Bipolar LSI/VLSI

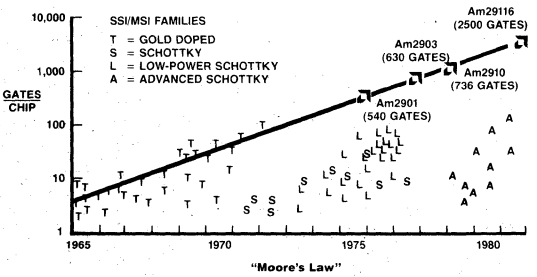


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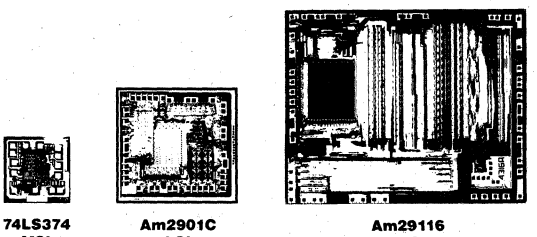
Figure 5.



74LS374 MSI | **Am2901C LSI** | **Am29116 VLSI**

MPL-080

Am2900 Components Continuously Become Faster and Faster

MORE SPEED: NO MORE POWER

There's a good old tried and proven way to make faster IC's – burn more power. (That's the only real difference between "LS" and "S" devices). But that solution isn't satisfactory for LSI devices like the Am2900 Family. Power is constrained to existing levels for reliability reasons.

Am2900 parts are always designed to obtain the maximum speed at a power level which is safe for the package types and operating environment of the part. To increase speeds, new technologies must be used to build faster components at no increase in power.

NEW CIRCUIT DESIGN TECHNIQUES MAKE FASTER GATES

One way to make faster components is to use new circuit design techniques. The most obvious is internal ECL, which provides very fast gates at similar power levels to LS TTL. The Am29116 reaches microcycle times of 100ns through the use of internal ECL. Other design techniques, such as low-level logic (with very small logic swings on-chip), can also provide higher speeds without introducing the time penalty of ECL to TTL conversion.

Finally, very low power gates used in non-critical speed paths make more power available for use in critical speed paths. As the 2900 Family develops, all these technologies will be used within a single component to achieve the highest speeds without increasing power. The Am2903A is one of the first products to take advantage of this mixed circuit technology.

IMPROVED PROCESS CONTROL ALLOWS TIGHTER SPECS

Today's 2900 parts are carefully characterized over a wide range of voltages, temperatures, and process parameters before an AC specification is published. As manufacturing technology improves, the process is subject to smaller run-to-run variations, so that all of the product is closer to design nominal. This makes it possible to specify parameters more closely to typical without incurring large yield losses. The first product reflecting this is the Am2903.

WHAT'S GOOD FOR THE GOOSE IS GOOD FOR THE GANDER

Many new tools in production technology are emerging, primarily spurred by the emphasis on high-speed MOS memories. The same tools, such as projection masking, also provide for smaller geometries in bipolar circuits. As MOS gets faster, so does bipolar. The Am2901C obtains its speed improvement over the Am2901B through these tools.

PROCESS TECHNOLOGY TAKES A QUANTUM LEAP

Current generation LSI/VLSI bipolar devices call for state-of-the-art processing technologies. IMOX™ ion-implanted micro-oxide technology gives the Am2901C its performance improvement over the Am2901B. IMOX also generates incredible packing densities – the Am29116 has 2500 gates on a single bipolar chip!

DESIGN FOR THE FUTURE

Every Am2900 part will undergo an evolution as new technologies become practical for production. Every part type will continuously become faster. The results are easy to observe – increases in performance at no additional cost (see Figure 1).

Most existing 2900 designs can be offered in higher performance versions simply by substitution of the 2901C for the 2901B, the 2909A for the 2909, the 2903A for the 2903, and so forth. Your 2900 design won't run out of speed in a few years. Advanced Micro Devices' 2900 Family will serve tomorrow's needs as well as today's.

Figure 1. Price/Performance Improvements

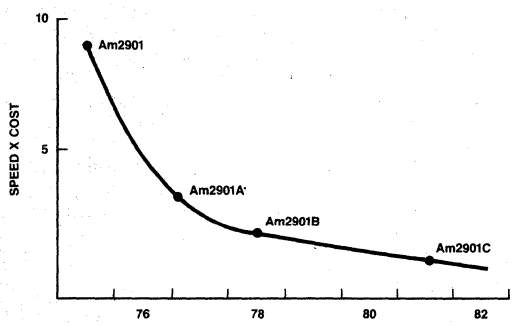
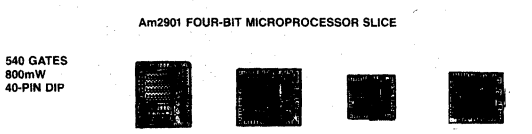


Figure 2. Bipolar Speed/Density Improvements



DIE SIZE	Am2901 33,000 MILS^2	Am2901A 20,000 MILS^2	Am2901B 15,000 MILS^2	Am2901C 15,000 MILS^2
SPEED A, B G, P	80ns	65ns	50ns	**37ns**
TECHNOLOGY	LOW-POWER SCHOTTKY	DUAL LAYER METAL ION-IMPLANTATION	PROJECTION PRINTING	ECL INTERNAL TTL I/O IMOX
	1975	1977	1978	1981

IMOX is a trademark of Advanced Micro Devices.

Introduction

THREE GENERATIONS OF TTL

Transistor-transistor logic has been the dominant technology for digital circuits since it was developed in the mid-1960's. It has proven itself to be manufacturable in high volume using an extremely reliable process technology. The processes used for TTL have evolved over the years, making components smaller, faster and less expensive. Relative to a TTL gate manufactured in 1966, a gate on a circuit manufactured today occupies 1/5 the area, consumes 1/10 the power, is twice as fast and costs less than 1/100 the price.

The circuits built using TTL technology have gone through two generations; the Am2900 Family represents the beginning of the third. Each generation consists of circuits which are fundamental building blocks of systems – circuits which can be interconnected in many different ways to build many different systems. Only by producing such universal circuits can manufacturing volumes be high enough to generate the rapid cost reductions characteristic of the integrated circuit industry.

The quality which distinguishes one generation from another is the level of integration used, and, because of the level of integration, the philosophy behind the circuit.

If one draws a curve plotting the cost of an individual gate against the number of gates on a chip, Figure 1 results.

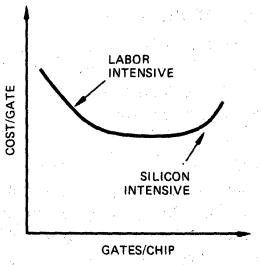


Figure 1. MPR-001

At the left, cost per gate is inversely proportional to the number of gates on the chip. The chip is small enough that it does not represent a significant portion of the cost of the product – it is virtually free. The cost of the product is composed of labor in assembly and test, the cost of processing an order, shipping and fixed overhead. Doubling the number of gates on the chip doesn't materially affect the cost so the cost per gate halves. As the number of gates per chip increases, the die begins to cost more, reversing the downward trend. As die cost dominates, the cost per gate remains relatively flat until the yield of the die begins to decline markedly. The cost per gate then begins to rise again. The lowest cost per gate is achieved at a level of integration corresponding to the flat region. This is the optimum level of integration.

As technology improves, costs are constantly reduced and the optimum level of integration occurs at more and more gates per chip.

The three curves of Figure 2 are the reason for the three generations of TTL. Each generation has consisted of fundamental system building blocks designed to take advantage of the optimum level of integration at the time.

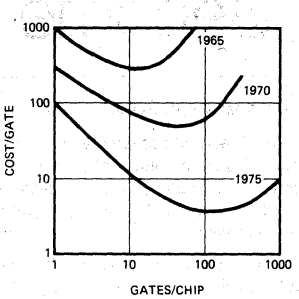


Figure 2. MPR-002

GENERATION I – SSI, 1965

In 1965, the optimum level of integration was three-to-six gates per chip. Users were delighted to buy such chips at $10-20 each. The circuits were useful in many systems. They consisted of gates – the 7400, 7410, 7420 – and, pressing the state of the art, some flip-flops. They were fundamental building blocks.

GENERATION II – MSI, 1970

Beginning around 1968, it became economical to put more gates on a chip and the industry was faced with a problem: How does one put 20 gates on a chip and build a universal building block? Clearly, one answer was to bring the inputs and outputs off chip as had been done before. But that was the wrong answer. The right answer was to redefine fundamental building blocks. The new building blocks fell into seven categories:

- Counters
- Decoders
- Multiplexers
- Operators (adders, comparators)
- Encoders
- Registers
- Latches

All systems could be defined in terms of these seven functions, and integrated circuits could be defined at the 20-50 gate/chip level which performed these functions efficiently. This, of course, is MSI. Over the last six or seven years, more and more circuits of this type have been introduced, utilizing standard gold-doped technology, low-power TTL, high-speed TTL, Schottky TTL, and now low-power Schottky TTL technology. Today, there are over 250 different MSI circuits and new ones appear every month. But in today's technology, many of these circuits are not particularly cost effective. They are too small for today's technology and their costs are labor intensive. (Labor costs do not follow traditional semiconductor pricing patterns.) In 1977, the optimum level of integration for bipolar logic was around 500 gates chip.

GENERATION III – The Am2900 Family, 1976

At a 500-gate-per-chip level of integration, one does not build counters, decoders, and multiplexers. A new definition of fundamental system functions was needed. Advanced Micro Devices has defined these eight categories:

- Data Manipulation
- Microprogram Control
- Macroprogram Control
- Priority Interrupt
- Direct Memory Access
- I/O Control
- Memory Control
- Front Panel Control

The Am2900 Family includes circuits designed to perform those functions efficiently. They are fundamental system building blocks; they contain hundreds of gates per chip; they are fast – utilizing Low-Power Schottky TTL technology and AMD's proprietary IMOX™ technology; they are expandable; they are flexible – useful in emulation; and they are driven under microprogram control.

IMOX AND ECL – THE NEXT STEP

Ever increasing device complexity placed greater and greater demands on existing process technologies. Advanced Micro Devices responded to this challenge by introducing its revolutionary IMOX ion-implanted micro-oxide technology in 1980. Oxide isolation generated faster transistor switching and tighter packaging. Ion-implantation meant tighter parameter control and lower power consumption. The bottom line – an unequalled combination of speed and density culminating in the Am29116 with a staggering 2500 gates-per-chip. Figure 3 shows this climb in gate density.

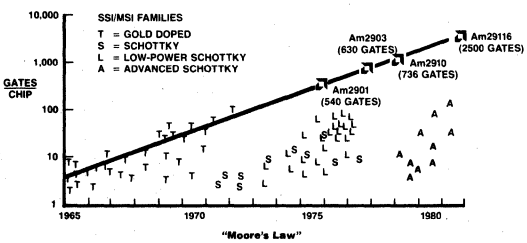


Figure 3. Am2900 Bipolar LSI/VLSI

Future refinements of IMOX and new device technologies will keep AMD on the leading edge in bipolar LSI/VLSI. Designed to take advantage of these improvements in process technology, a new family of microprogrammable 32-bit controller products will set the pace for bipolar VLSI in the mid-1980s.

THE Am2900 FAMILY

The Am2900 Family consists of a series of LSI building blocks designed for use in microprogrammed computers and controllers. Each device is designed to be expandable and sufficiently flexible to be suitable for emulation of many existing machines. It is the wide variety of machine architectures possible with the Am2900 Family which sets it apart from the fixed-instruction microprocessors such as the Am8086.

While an Am8086 can be used to build a microcomputer with only four or five packages, an Am2900 design will require 30 or 40 or more. The Am8086 design will, therefore, almost always be cheaper. But the Am8086, or any other fixed-instruction processor, can execute only one instruction set, so it is not really suitable for emulation of another machine.

Moreover, a fixed-instruction processor operates only on words of a single length, usually eight bits. An Am2900 design, on the other hand, can be constructed for any word length which is a multiple of four bits.

Many applications require specialized operations to be performed at relatively high speed. Such functions as multiply and divide and special graphic control operations, can be done in microcode 10–100 times faster than in fixed-instruction MOS processors.

MICROPROGRAMMED ARCHITECTURE

Most small processors today are being designed using a technique called microprogramming. In microprogrammed systems, a large portion of the system's control is performed by a read only memory (usually PROM) rather than large arrays of gates and flip-flops. This technique frequently reduces the package count in the controller and provides a highly ordered structure in the controller, not present when random logic is used. Moreover, microprogramming makes changes in the machines' instruction set very simple to perform – reducing the post-production engineering costs for the system substantially.

The Am2900 Family of Bipolar LSI devices has been designed for use in microprogrammed systems. Each device performs a basic system function and is driven by a set of control lines from a microinstruction.

Figure 4 illustrates a typical system architecture. There are two "sides" to the system. At the left is the control circuitry and on the right is the data manipulation circuitry. The block labeled "2901C array" consists of the ALU, scratchpad registers, data steering logic (all internal to the Am2901Cs), plus left/right shift control and carry lookahead circuit. Data is processed by moving it from main memory (not shown) into the 2901C registers, performing the required operations on it and returning the result to main memory. Memory addresses may also be generated in the 2901Cs and sent out to the memory address register (MAR). The four status bits from the 2901Cs ALU are captured in the status register after each operation.

The logic on the left side is the control section of the computer. This is where the Am2909A, 2910A, or 2911A is used. The entire system is controlled by a memory, usually PROM, which contains long words called microinstructions. Each microinstruction contains bits to control each of the data manipulation elements in the system. There are, for example, nine bits for the 2901C instruction lines, eight bits for the A and B register addresses, two or three bits to control the shifting multiplexers at the ends of the 2901C array (see Figure 19, 2901C data sheet), and bits to control the register enables on the MAR, instruction register, and various bus transceivers. When the bits in a microinstruction are applied to all the data elements and everything is clocked, then one small operation (such as a data transfer or a register-to-register add) will occur.

A "machine instruction" (such as a minicomputer instruction or an 8086 instruction) is performed by executing several microinstructions in sequence. Each microinstruction therefore contains not only bits to control the data hardware, but also bits to define the location in PROM of the next microinstruction to be executed. The fields are labeled in Figure 4 as I, CC, and BA. The I field controls the sequencer. It indicates where the next address is located – the μPC, the stack, or the direct inputs – and whether the stack is to be pushed or popped.

The CC field contains bits indicating the conditions under which the I field applies. These are compared with the condition codes in the status register and may cause modification to the I field. The comparing and modification occurs in the

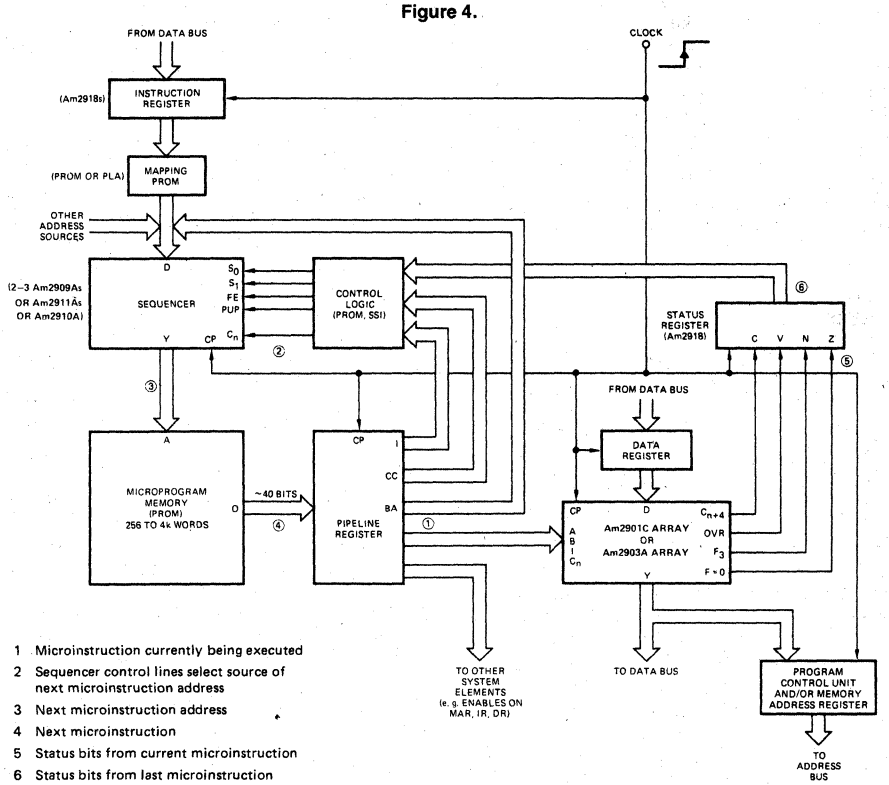
block labeled "control logic". Frequently this is a PROM or PLA. In the case of the Am2910, it is built into the chip. The BA field is a branch address or the address of a subroutine.

PIPELINING

The address for the microinstructions is generated by the sequencer, starting from a clock edge. The address goes from the sequencer to the ROM and, an access time later, the microinstruction is at the ROM outputs.

A pipeline register is a register placed on the output of the microprogram memory to essentially split the system in two. The pipeline register contains the microinstruction currently being executed ①. (Refer to the circled numbers in Figure 4.) The data manipulation control bits go out to the system elements and a portion of the microinstruction is returned to the sequencer ② to determine the address of the next microinstruction to be executed. That address ③ is sent to the ROM and the next microinstruction ④ sits at the input of the pipeline register. So while the 2901Cs are executing one instruction, the next instruction is being fetched from ROM. Note that there is no sequential logic in the sequencer between the select lines and the output. This is important because the loop ① to ② to ③ to ④ must occur during a single clock cycle. During the same time, the loop from ① to ⑤ must occur in the 2901Cs. These two paths are roughly the same (around 200ns worst case for a 16-bit system). The presence of the pipeline register allows the microinstruction fetch to occur in parallel with the data operation rather than serially, allowing the clock frequency to be doubled.

Figure 4.



The system shown in Figure 4 works as follows. A sequence of microinstructions in the PROM is executed to fetch an instruction from main memory. This requires that the program counter, often in a 2901C working register, be sent to the memory address register and incremented. The data returned from memory is loaded into the instruction register. The contents of the instruction register is passed through a PROM or PLA to generate the address of the first microinstruction which must be executed to perform the required function. A branch to this address occurs through the sequencer. Several microinstructions may be executed to fetch data from memory, perform ALU operations, test for overflow, and so forth. Then a branch will be made back to the instruction fetch cycle. At this point, there may be branches to other sections of microcode. For example, the machine might test for an interrupt here and obtain an interrupt service routine address from another mapping ROM rather than start on the next machine instruction. There are obviously many possibilities. Throughout this data book, in application notes, and within data sheets, some suggested techniques will be found.

Additional application notes are in preparation and are planned for publication. Advanced Micro Devices' Applications' staff is available to answer questions and provide technical assistance as well. They may be reached by calling (408) 732-2400, or, outside California (800) 538-8450. Ask for Am2900 Family Applications.

Am29100 High-Performance Controller Products

A BETTER WAY IS HERE

A new family of products from Advanced Micro Devices makes high-performance controller design a snap.

MICROPROGRAMMING; BEST FOR COMPUTERS, BEST FOR CONTROLLERS

Microprogramming, long the preferred approach for computer design, offers lots of advantages in controllers as well. The ease with which the functions of a microprogrammed controller can be enhanced and modified made the original 2900 Family popular for many disk, printer and communications controllers. The high-speed operation of these microprogrammed systems makes it possible to handle higher data rates from newer peripheral devices and to build intelligence into the controller.

But the original 2900 products are architecturally oriented toward computers, with design features optimized for arithmetic functions and short sequences of microinstructions. MOS processors are good choices for many low-speed applications, but when the demand for speed and intelligence goes up, they cannot keep pace. Controllers need something better: the 29100 Family.

The 29100 Family products have been designed from the ground up with peripheral control applications in mind. They are fast, they are optimized for bit-manipulation, character handling, data communication and long, sophisticated microprograms and they are designed to work together in a system.

FAST LIKE YOU'VE NEVER HAD

The central element of our new high-speed controller family is the Am29116 – a 16-bit bipolar microprocessor. It's not a slice – it's a complete 16-bit processor, with three-input ALU, 32 scratchpad registers, an accumulator, data latch, barrel shifter, priority encoder and status register with conditional code generation logic. But the Am29116 is far more than a very fast number cruncher – it's been optimized for controller-oriented applications. It's instruction set has instructions often needed in controllers that are not available in any other processor.

A WHOLE FAMILY OF FAST LSI CONTROLLER PARTS

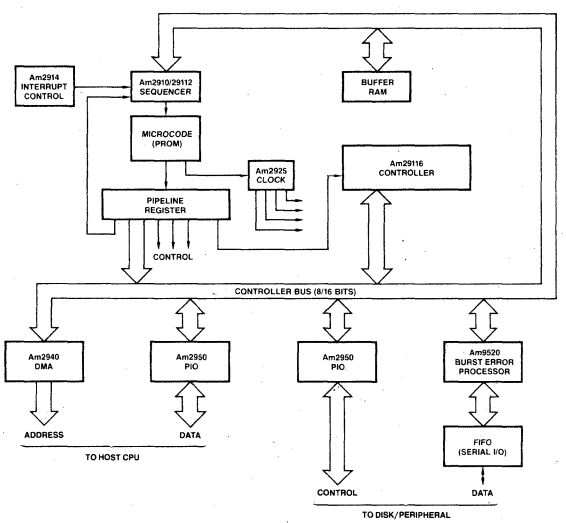
There's more to our controller family than just the Am29116. A new sequencer, the Am29112, has been expressly designed for 10MHz microprogram control, with features like real-time interrupt servicing and deep subroutining. Rapid internal data transfer is handled by the Am2940 DMA Address Generator and by the Am2950 handshaking I/O port. The Am9520 Burst Error Processor will provide a solution for error correction on disk reads. Now, more than ever, the 2900 Family is the better solution for high data rate and highly intelligent control problems.

TYPICAL CONFIGURATION USING THE 2900 CONTROLLER FAMILY

A typical intelligent controller configuration is shown below. The basic controller consists of the Am29116, a microprogram control unit and a high-speed buffer memory. Each microinstruction includes: a) a 16-bit instruction field to the Am29116, b) next-microinstruction selection bits, c) control for the buffer memory, d and e) control for the interface circuits and f) possibly an 8 or 16-bit data field.

Interface circuits like the Am2940 and Am2950 are used to provide DMA and to pass data between the controller and the host computer. Other circuits are used to interface to the peripheral. In this example, a disk interface is shown with a serial-parallel converter, a FIFO and a burst error processor. Controllers for other peripherals use identical hardware except for the peripheral interface itself.

HIGH-PERFORMANCE INTELLIGENT CONTROLLER



The Am29500 Family

A New High-Performance Architecture for Digital Signal/Array Processing

The new system designs of the '80s will continue to press the performance limits of technology. Parallel processing and pipelined architectures will become the standard approach. The new architectures are best implemented with a chip set that has been designed from the ground up with high speed array processing in mind.

The Am29500 Family is designed specifically for these new architectures. Every key product feature supports the system end objective of maximum performance and flexibility. These include:

- Microprogrammable, parallel functions
- Pipelined organization used throughout
- IMOX™ process and ECL internal structures
- TTL I/O for easy interfacing

The first members of the family are targeted for the efficient execution of DSP and array processing algorithms. The most common include Infinite Impulse Response (IIR) and Finite Impulse Response (FIR) digital filters and Fast Fourier Transform (FFT) processors.

The first major building blocks are designed to support maximum performance signal processing applications.

Included are:

- **Am29501 Multi-Port Pipelined Processor**

  A specialized parallel processor which executes multiple simultaneous data operations. Its Register/ALU structure provides the key functional element for a high performance signal processing system. Eight-bit slice!

- **Am29540 FFT Address Sequencer**

  This algorithm-specific VLSI chip generates data and coefficient addresses for the Fast Fourier Transform. It supports a wide variety of FFT algorithms in either radix-2 or radix-4.

- **Am29516/29517 High Speed 16 x 16-Bit Parallel Multipliers**

  Both are 16 x 16-bit Parallel Multipliers. The Am29516 is pin and functionally compatible with the MPY-16HJ, but with an added multiplexer to output the LSP at the MSP port. The Am29517 is the same function, but with clock enables for microprogrammed applications.

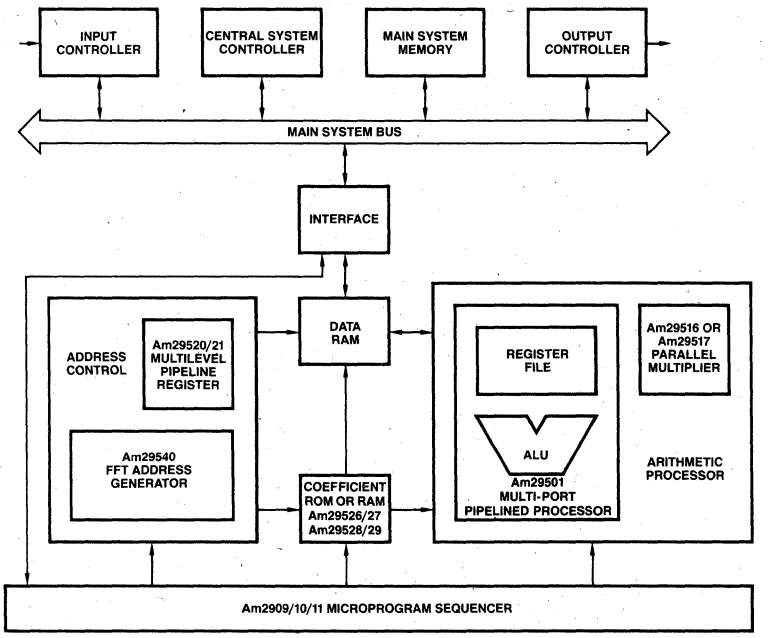
- **Am29520/29521 Multilevel Pipeline Registers**

  Both devices contain four 8-bit registers for dual two-stage (FFT butterfly) or single four-stage (general purpose) data or address pipelining. Combined load-and-shift (Am29520) or separate load-and-shift (Am29521) control options are available.

- **Am29526/29527/29528/29529 High-Speed Sine/Cosine Function Generators**

  The sine and cosine functions are necessary for Fast Fourier Transforms (FFT). The Am29526/527 generate the most significant and least significant byte of the 16-bit sine function and the Am29528/529 generate the most significant and least significant byte of the 16-bit cosine function. The sine and cosine functions are generated to provide a range of θ for a half cycle, $0 \leq \theta \leq \pi$, in increments of $\pi/2048$. All four units have a 50ns maximum commercial generation time.

HIGH PERFORMANCE SIGNAL PROCESSOR



MPL-025

A high-performance signal processor may be constructed as shown in the diagram. The processor is built entirely with new Am29500 digital signal processing and Am2900 devices. Such a processor is attached as a slave to the main system bus to perform the multitude of arithmetic operations which prevail in DSP algorithms.

Using this architecture it is possible to implement a radix-2FFT butterfly in four instruction cycles. This allows a 1024-point complex FFT to be performed in approximately 2ms.

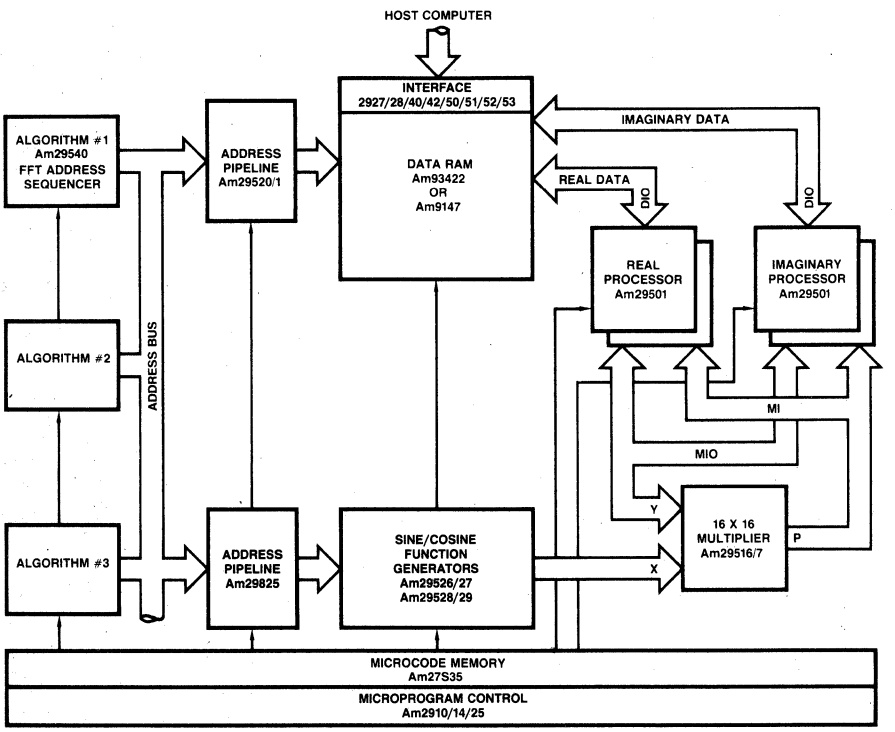
Fast multiplication is the key to high-speed digital-signal processing and high-speed array processing. In addition to the Am29516 and Am29517, Advanced Micro Devices is developing an extensive family of multipliers. The first addition to the high-performance multiplier group:

- Am29510 High-Performance 16 x 16 Bit Multiply Accumulator

The multiply accumulator provides single cycle multiply accumulation or subtraction. The Am29510 is a pin- and function-compatible alternate source for the TRW TDC1010J. As illustrated with the Am29516/517, the multiply accumulator will have a speed improvement over existing multiply accumulators.

- Am295XX to be announced.
  - *More Multipliers*
    A proliferation of the existing multiplier architectures will generate a complete family of multipliers and multiplier accumulators.
  - *Floating Point Processors* (FPP)
    A 32-bit FPP capable of performing single-cycle double-precision floating-point addition, subtraction, and multiplication. The FPP performs the arithmetic operations in DEC or IEEE format. Available 1984.

Am29500 ARRAY PROCESSOR



MPL-026

Am2960-70 Memory Support Family System Overview

Memory system designs are increasingly shaped by three requirements:

1. Higher system performance
2. More memory capacity in less space
3. Increased reliability

The Am2960-70 Memory Support Family is a family of LSI building blocks which excels in satisfying these three requirements and provides a complete systems solution for designs using 64K or 256K DRAMs. The family members include:

Am2960 Error Detection and Correction Unit
Am2961/62 EDC Bus Buffers
Am2964B Dynamic Memory Controller (64K DRAM Version)
Am2965/66 Dynamic RAM Drivers
Am2968 Dynamic Memory Controller (256K DRAM Version)
Am2969 Timing Controller
Am2970 Timing Controller
Am8163/67 System and Timing Controller for MOS MPUs

These are general purpose products. They will support any suppliers' DRAMs and will work with any processor type: 8086, 80186, 80286, 68000, Z8000, and Am2900 processors. They may also be used to support word widths of any size from 8 bits to 64 bits.

Figure 1 shows the system interconnection for a typical memory system for 256K DRAMs, and Figure 2 shows the system interconnection for a typical memory system using 64K DRAMs. In both cases, the memory support subsystem interfaces to the System Data Bus, Address Bus, and control signals. Also, in both cases all, or almost all, of the memory support functions are handled by AMD LSI devices. This simplifies the design of the memory system and, more importantly, allows the board space available for DRAMs to be maximized because the LSI solution for control and error correction is very compact.

ERROR DETECTION AND CORRECTION

It is important that memory systems function reliably. The number of bytes of storage is increasing rapidly in memory systems at the same time that the density of the MOS DRAMs is growing. With 64K and 256K DRAMs, alpha particle sensitivity is much greater than that of smaller DRAMs because of the reduced size of the memory cells and the smaller stored charge of the cell. A Technical Report follows the Am2960 data sheet in this section and is entitled "Am2960 Boosts Memory Reliability." This technical report gives some statistics on soft error rates for DRAMs and demonstrates the dramatic increase in memory reliability gained from the use of Hamming Code Error Detection and Correction schemes, such as those used by the Am2960 EDC (Error Detection and Correction) unit.

Data interface between the dynamic memories, the Am2960 EDC chip and the system data bus is accomplished by means of the Am2961/62 bus buffers. Figure 3 depicts the architecture of these devices along with a simplified block diagram of the Am2960. The Am2961 is inverting between the system data bus and the EDC bus while the Am2962 is noninverting. As shown in Figure 3, the Am2961 and Am2962 contain two internal latches, a multiplexer, and a RAM driver output buffer.

These devices feature 4-bit-wide data paths to and from the RAM, the EDC, and the system data bus. The bus-input (BI) latch is used predominantly in byte WRITE operations, so that an incoming byte from the system data bus can be stored while the memory is being read, and any necessary correction made in the bytes not being changed. The bus-output (BO) latch is used predominantly for storing the output data if the processor is in the single-step mode. In the single-step mode it is necessary to hold the output data on the system data bus, but the memory must be released for refresh.

The Am2960 Error Detection and Correction Unit contains all the logic necessary to generate check bits on a 16-bit data field according to a modified Hamming code and to correct the data word when check bits are supplied. Operating on the data read from memory, the Am2960 will correct any single-bit error and will detect all double- and some triple-bit errors. For 16-bit words, 6 check bits are used. The Am2960 is expandable to operate on 32-bit words (7 check bits) and 64-bit words (8 check bits). In all configurations, the device makes the error syndrome bits available on separate outputs for data logging.

The Am2960 also features two diagnostic modes in which diagnostic data can be forced into portions of the device to simplify device testing and to execute system diagnostic functions.

The 16-bit Diagnostic Latch is loadable from the bidirectional data lines under control of the Diagnostic Latch Enable, LE DIAG. It contains check bit information in one byte and control information in the other, and is used for driving the device when in the Internal Control mode, or for supplying check bits when in one of the Diagnostic modes.

The control logic determines the specific operating mode. Normally the control logic is driven by external control inputs; however, in the Internal Control mode, the control signals are instead read from the Diagnostic Latch.

The Am2960 is a very fast EDC device, but even faster versions will soon be available. A speed selected version, the Am2960-1, is described in the Am2960 data sheet, and an IMOX™ version, the Am2960A, will be available by early 1984. All speed-improved versions have identical functions and are electrically plug-compatible with the current Am2960.

MEMORY SYSTEM CONTROL AND TIMING

Two Dynamic Memory Controllers are available for generating address, $\overline{RAS}$, and $\overline{CAS}$ signals for memory banks. The Am2964B is designed to work with 64K DRAMs of which each device can handle up to four banks for a total control capacity of 256K words. The new Am2968 is designed to work with 256K DRAMs and can also handle up to four banks for a total control capacity of 1 Megaword (the words can be as many bits wide as desired). Also, the Am2968 does not require external driver chips as does the Am2964B – the Am2968 has the memory drivers, with all of the undershoot control and speed features of the Am2965/66, built right into its address, $\overline{RAS}$, and $\overline{CAS}$ outputs.

For generating the timing and control signals required by the Am2964B/68 and the Am2960/61/62, there are several different devices available, optimized for different system requirements. For MOS Microprocessor systems, use the Am8163 or Am8167.

IMOX is a trademark of Advanced Micro Devices, Inc.

Figure 1. Am2900 High Performance Memory Subsystem Using 256K DRAMs

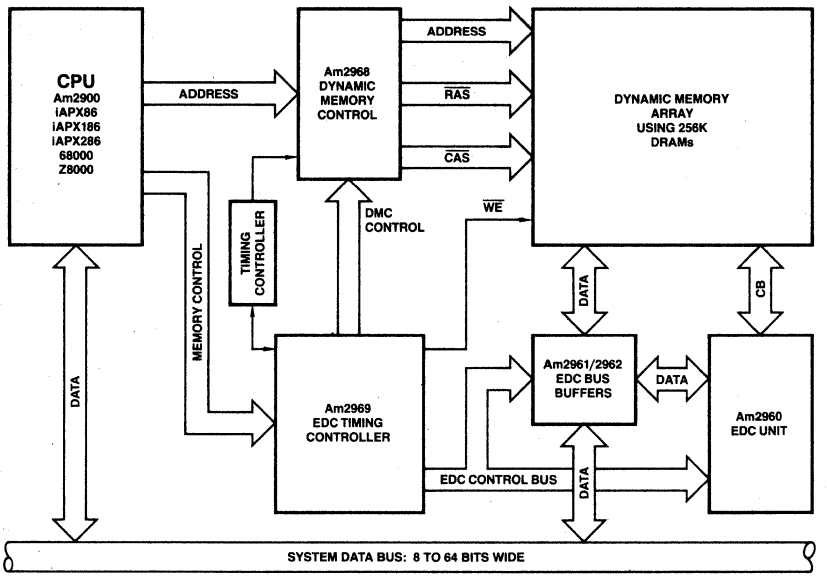


Figure 2. Am2900 High Performance Memory Subsystem Using 64K DRAMs

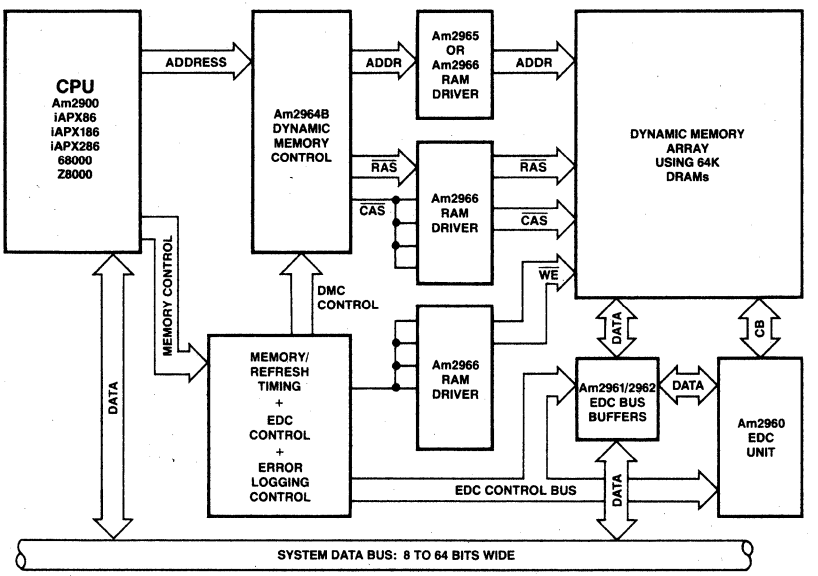


Figure 3. EDC Data Path

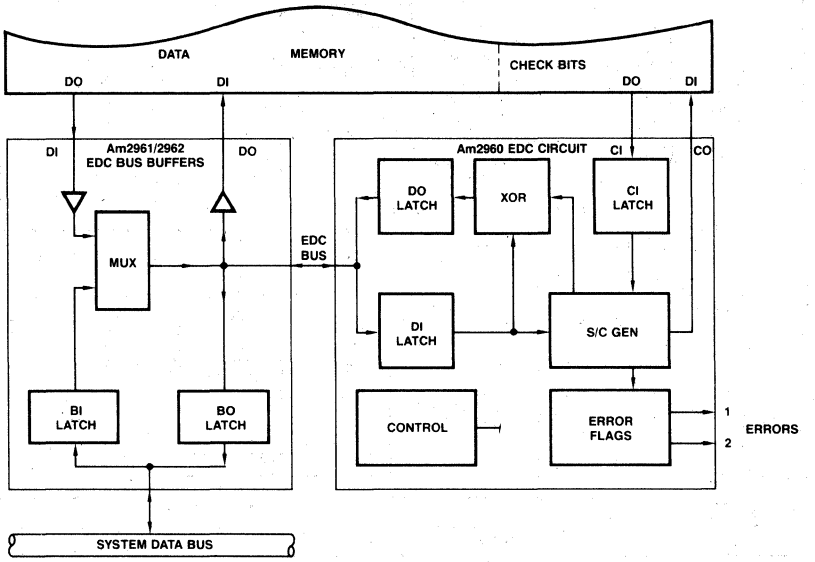
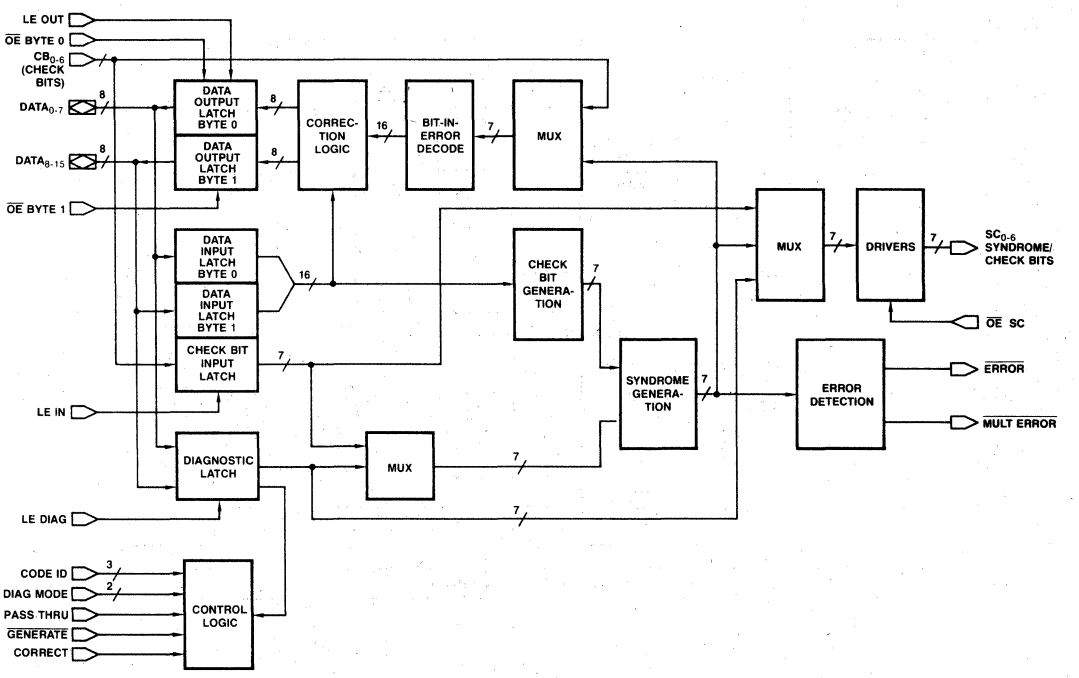


Figure 4. Am2960 Block Diagram



Both of these devices will interface easily to iAPX86/186/286, Z8000, or 68000 microprocessors. The Am8163 and Am8167 provide the control signals and timing signals for the memory controllers, the EDC, and the data bus buffers – in addition, the Am8163/67 decode the memory system control signals directly from the MOS Microprocessor, requiring in most cases only a single PAL™ for interfacing. In this section are detailed block diagrams of systems showing how to interface the Am2960-70 Family devices to the most popular MOS microprocessors.

For high-performance Am2900-based processors or other high-speed processor designs, use the Am2969 or Am2970 to generate timing and control signals.

Following is a description of the function of the Am2964B/65/66 for Dynamic Memory Control for 64K DRAMs. The Am2968 incorporates these features and more into a single IC for use with 256K DRAMs.

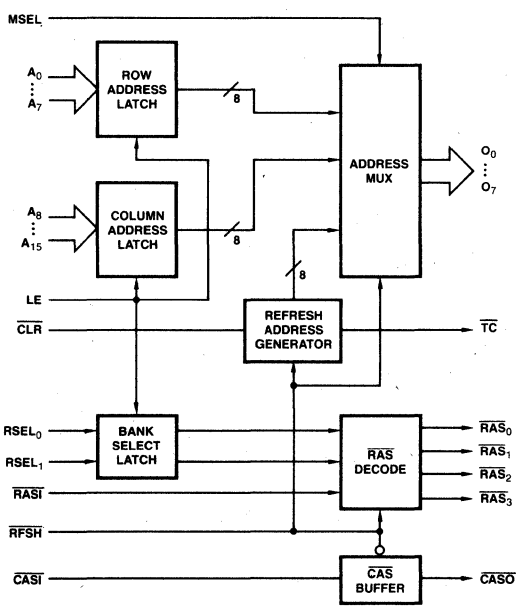
The Am2964B Dynamic Memory Controller is used to provide all address handling, as well as $\overline{RAS}$ and $\overline{CAS}$ decoding and control. A block diagram of the Am2964B Dynamic Memory Controller is shown in Figure 5. The device contains 18 input latches for capturing an 18-bit address for memory control; the two highest order addresses are decoded in the Am2964B to select one of four banks of RAM by selecting one of the four $\overline{RAS}$ outputs.

The Am2964B is designed to operate with either 16K Dynamic RAMs or 64K Dynamic RAMs. Thus, the designer either uses 14 of the multiplexer address inputs and 7 of the address outputs or all 16 of the multiplexer address inputs and all 8 of the address outputs as needed by the memory. In the case of 16K Dynamic RAMs, 7 address inputs are provided to the RAM during the $\overline{RAS}$ LOW signal, and then the 8-bit multiplexer is switched so that 7 upper address bits are provided to the RAM for the $\overline{CAS}$ LOW part of the cycle. The Am2964B Dynamic Memory Controller contains an 8-bit refresh counter that is used to supply the refresh address to the dynamic memory during the refresh cycle. This counter can be used in either the 128 or 256 line refresh mode. A $\overline{CAS}$ buffer is included in the dynamic memory controller so that the $\overline{CAS}$ output can be inhibited during refresh.

Normal operation of the Dynamic Memory Controller is to provide the address, close the input address latches and kick off a normal memory cycle. This is accomplished by bringing the $\overline{RASI}$ input LOW, which will cause one of the $\overline{RAS}$ outputs to go LOW. After the required memory timing, the MSEL input will be used to switch the multiplexer to the other address latch, then, the $\overline{CASI}$ input will be driven LOW causing the $\overline{CASO}$ output to go LOW and execute the $\overline{CAS}$ part of the memory cycle. The refresh cycle is executed by driving the $\overline{RFSH}$ input LOW which causes the multiplexer to connect the refresh counter to its address outputs. Then, the $\overline{RASI}$ input is driven LOW which causes all four $\overline{RAS}$ outputs to go LOW. This will simultaneously refresh all four banks of dynamic RAMs controlled by the Am2964B Dynamic Memory Controller. When either the $\overline{RFSH}$ or $\overline{RASI}$ input is brought HIGH, the refresh counter is advanced so it will be ready for the next refresh cycle.

As can be seen in Figure 1, Dynamic RAM Drivers can be used in large memory systems to buffer the Address, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WRITE\ ENABLE}$ signals to the RAMs. The Am2965 and Am2966 are pin compatible devices with the Am74S240 and Am74S244. These RAM drivers are specifically designed for driving dynamic RAMs and feature high capacitance drive, guaranteed maximum undershoot of less than −0.5 volts and high V_{OH} of greater than V_{CC} −1.15 volts. The Am2965 is inverting and the Am2966 is noninverting. The devices feature symmetrical rise and fall times and have guaranteed minimum and maximum t_{PD} specifications for both 50pF and 500pF loads.

Figure 5. Am2964B Dynamic Memory Controller



Am2900 Family Design Aids Index

Am2900 Family Applications Literature

Available from AMD's Customer Education Center

Bit-Slice Design: Controllers and ALUs, White D.E., Garland STPM Press, N.Y. © 1981 Price: $34.50 + Tax + Shipping ISBN 0-8240-7103-4	This book provides the inexperienced bit-slice design engineer with an easily understood description of how a computer control unit and ALU is built with the fundamental Am2900 devices (Am2901B, Am2909/11, Am2903, Am2910 and Am2914). This book forms the basis of the introductory bit-slice design course (ED2900A) at the AMD Customer Education Center.
Bit-Slice Microprocessor Design, Mick and Brick, McGraw-Hill Publishing Co. 1221 Avenue of the Americas New York, N.Y. 10020 Price: $18.50 + Tax + Shipping ISBN 0-07-041781-4	This comprehensive book discusses in detail the design of a microprogrammed computer using the Am2900 Family for the more experienced bit-slice designer. The book also includes sections on DMA design with the Am2940/Am2942 and Program Control Unit design with the Am2930/Am2932. The book's chapters are: I – Computer Architecture II – Microprogrammed Design III – The Data Path IV – The Data Path, Part Two V – Program Control Unit VI – Interrupt VII – Direct Memory Access VIII – The Hex 29 IX – The Super Sixteen
ED2900A Study Guide Price: $18.00 + Tax + Shipping	This study guide is used in conjunction with the ED2900A course and complements Bit-Slice Design: Controllers and ALUs. The study guide contains example design problems, exercises and example AMSYS®29 programs.

Ordering Information

The above literature may be ordered directly from:

Customer Education Center
Advanced Micro Devices, Inc.
490-A Lakeside Drive, MS: 71
Sunnyvale, CA 94086

The Am2900 Evaluation and Learning Kit

The Am2900 Evaluation Kit system consists of a microprogrammed control unit which controls all the inputs to an Am2901 microprocessor slice. Thirty-two bit microinstructions are entered into a RAM in the control unit using the switch register. Each microinstruction contains bit to control the Am2901A's A and B addresses, instruction, carry in, and data input. Additional bits in the microinstruction control an Am2909 sequencer which generates the addresses for the microprogram memory. Once entered, microinstructions may be executed using a single step clock or using a pulse generator. The LED display provides access to nearly every signal path in the system.

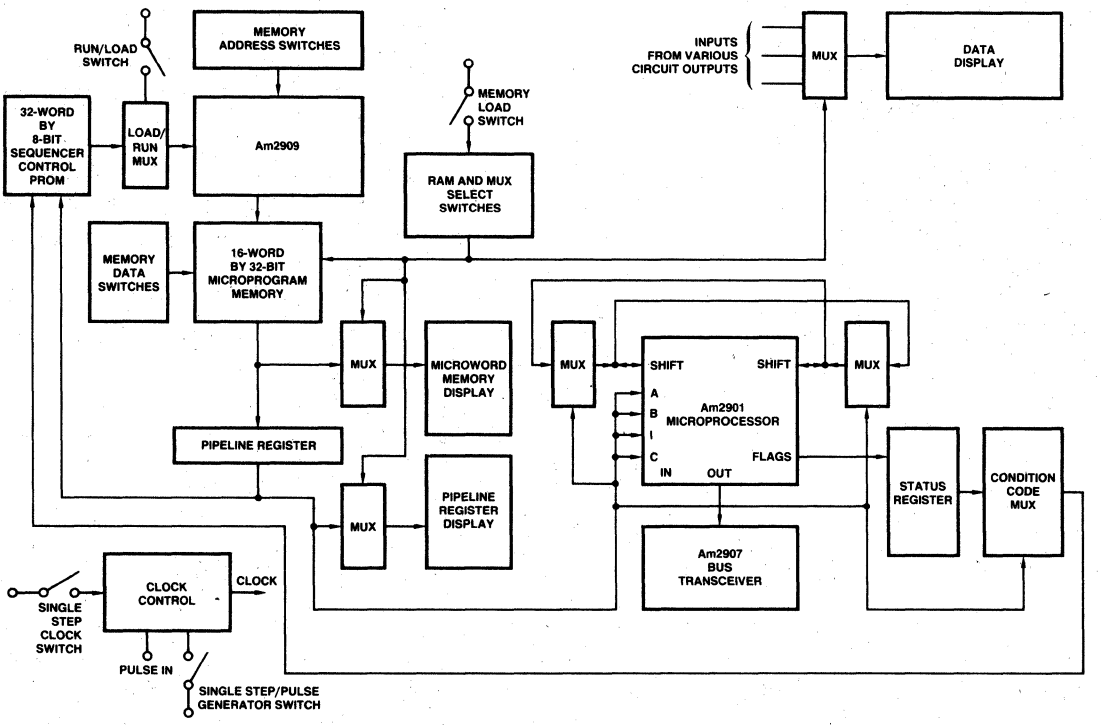
Sixteen "sequence control" instructions are available, including execute, branch conditional, jump-to-subroutine, return, and loop. Because the set of sequence instructions is implemented in a PROM, the user can devise his own set of operations by programming a new PROM.

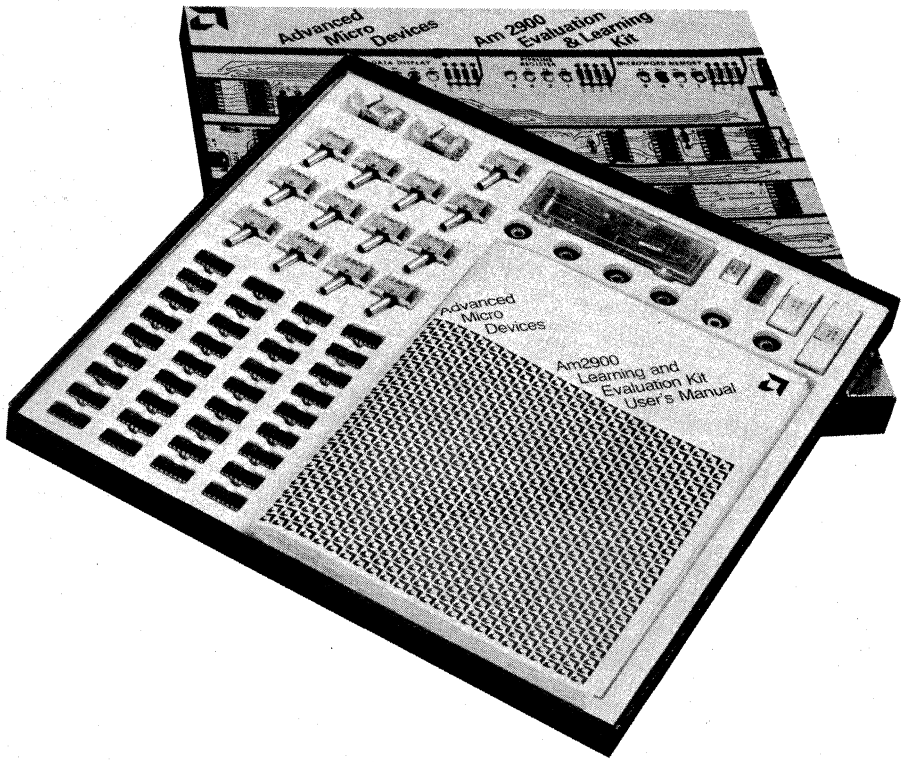
The kit is supplied as a preassembled board with a manual containing theory and a set of exercises. The user need only attach a 5V power supply (2.0 ampere rating).

Working with the kit, the user will gain familiarity with a high performance pipelined microprogrammed architecture, and with the operation of the Am2909 and Am2901A. By driving the kit from a pulse generator, the user can observe the operation of the components in real time, executing real instructions.

The part number for this kit is Am2900K1.

Figure 1. Block Diagram of the Am2900 Evaluation and Learning Kit




Advanced
Micro
Devices
Am 2900
Evaluation
& Learning
Kit
Advanced
Micro
Devices
Am2900
Learning and
Evaluation Kit
User's Manual

Am29203 Evaluation Board

Microprogramming Evaluation System

DISTINCTIVE CHARACTERISTICS

- 16-bit word size –
  System based around four Am29203 bipolar microprocessor slices
- Structured system approach –
  Integrated system features Am29203, Am2910, Am2904, Am2902, and Am2925 functional modules
- Monitor interface –
  Allows user to develop and analyze microprograms through an external screen oriented terminal
- I/O capability –
  Memory mapped I/O serial port via microprogram controllable UART. Additional RS-232 serial port dedicated for use by monitor terminal
- Sequence control –
  Monitor allows Halt, Single Step, and Run control as well as breakpoints and escapes from program flow
- On-board memory –
  1024 word by 48-bit Writeable Control Store and 1K by 16-bit RAM macro-memory on-board
- Complete user's manual

FUNCTIONAL DESCRIPTION

The Am29203 Evaluation Board is a complete 16-bit microprogrammable computer system based on the Am29203 bit-slice microprocessor. This single board computer is designed to demonstrate comprehensively the execution of a microprogrammed bit-slice system.

The Am29203 Evaluation Board consists of two logical parts, the primary system and the monitor as shown in Figure 1. The primary system contains a microprogram controller, the Am2910, an arithmetic section centered around the Am29203 and Am2904, and a macro-memory module which includes an I/O controller. This portion of the system is designed for user control and interaction (Figure 2).

The monitor functional unit provides the user interface for control of the primary system from an external terminal or computer.

It allows the user to examine and load various memory, register, and ALU bus contents. Additional features include run/halt/single-step control modes, breakpoint and escape capability, and bulk I/O transfer.

The system comes completely assembled on a single circuit board. Two serial I/O ports allow the monitor to interface with an external terminal while leaving one port free for user applications. On-board memory includes a 1K word Writeable Control Store for microcode and a 1K word macro memory. All control signals are available at an edge connector for support of up to 32K words of external memory.

The Am29203 Evaluation Board is intended to familiarize the user with a high-performance pipelined microprogrammed architecture. To that end, the board can execute preprogrammed microcode routine examples as well as user programs. The board supports more than nineteen different macroinstructions in six different formats (including indexed addressing).

A complete user's manual covers architecture, microprogramming, I/O control, monitor operation, and interface to external devices. It includes definition files, schematics, and timing diagrams.

Figure 1. Evaluation Board Organization

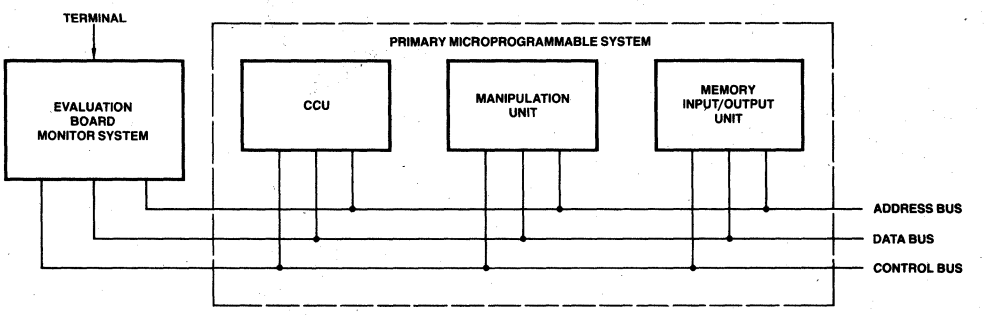
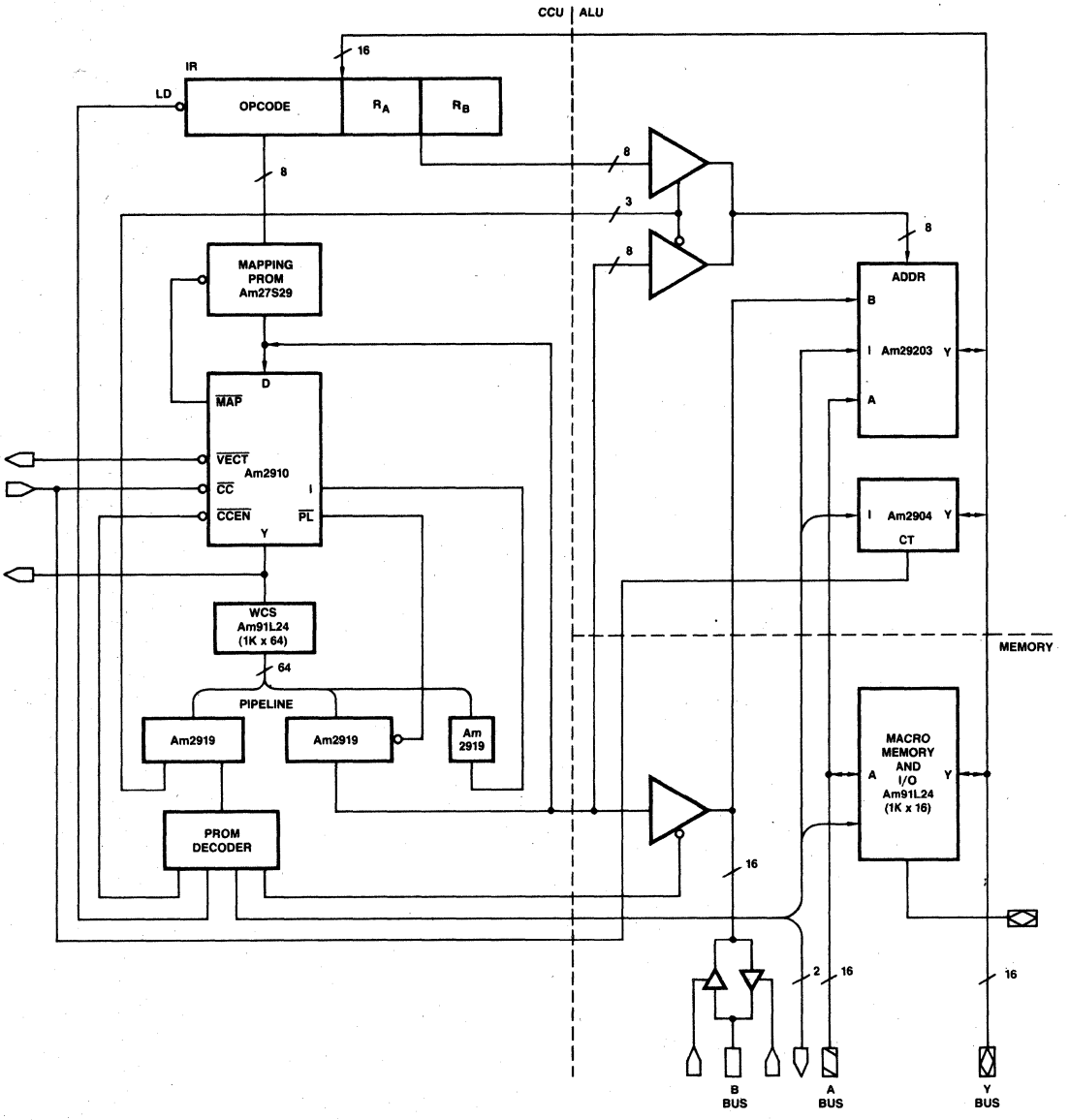


Figure 2. Primary System Architecture



MPR-858

School of Advanced Engineering

BIPOLAR APPLICATION DESIGN COURSES

AMD's School of Advanced Engineering offers graduate-level instruction in designing with the newest technologies. Bipolar design courses take you from the basics of bit-slice architecture through basic design with the 2900 Family on to the microprogram development system and its application to your design and finally to emulation and CPU architecture where students create microcode to drive an actual system, using the writable control store of the AmSYS29 development system.

For More Information:

Contact your AMD Sales Representative or write to:

Advanced Micro Devices
School of Advanced Engineering
Customer Education Center
490-A Lakeside Drive
P.O. Box 453
Sunnyvale, California 94086 U.S.A.

AmSYS®29

Microprogram Development System

AmSYS29, from Advanced Micro Computers, is the proven system for developing microprogrammed machines. It greatly simplifies the speed of developing and integrating software and hardware for Am2900 based microprogrammed machines. AmSYS29 supports 2901/03 based CPU designs, 29116 based controller designs and 295XX based signal processing designs.

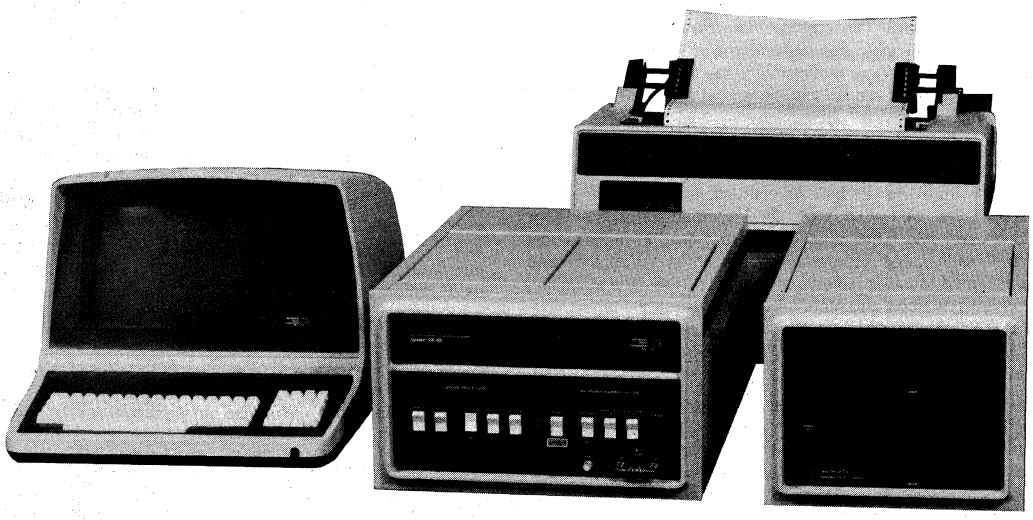
A microcode assembly language of your specifications is implemented through AMDASM™. You can then write the microprogram in your symbolic language and assemble the source file with AMDASM.

The Control Store Emulator contains a high-speed Writable Control Store to replace microprogram PROM during development. Your microsequencer address accesses a block of microcode in WCS RAM that can be mapped anywhere in your target system memory.

Emulator Control Logic controls the target system clock providing single-step and full speed control with multiple breakpoints. Monitor points provide measurements of the target system logic state during hardware debug.

Microprogram support software moves microcode object files out to Writable Control Store and saves working programs on to disk. DDT29 procedure interfaces the system console to the Control Store Emulator providing clock control, breakpoint setting, microprogram address control, logic state tracing and microcode editing.

AmSYS29 provides complete software and hardware support for the development of any microprogrammed system.



Macro Meta Assembler from Microtec*

The Macro Meta Assember is a valuable programming tool for those faced with the problem of writing micro-programs for bit slice processors such as the AMD 2901 and other similar microprogrammable microprocessors. It is a necessity for anyone faced with the problem of micro-programming any wide-word driven micro-sequencer system.

The Macro Meta Assembler is an enhanced version of Microtec's Meta Assembler. It is totally upward compatible, yet can perform many functions that are difficult or impossible with more basic packages.

The principal new feature of the Macro Meta Assembler is a powerful macro facility that enables the user to define variable length microinstructions using a single mnemonic; to encode complex overlayed instructions, and to encode non-contiguous fields. Macros may be passed a variety of parameter types: Symbols, Numbers, Opcodes, and Character Strings. Within the Macro-expansion parameters may be dynamically concatenated to existing text or other parameters, Symbols may be declared Local to the current Macro or be defined globally, and a wide variety of operators have been implemented for use with conditional Macro expansion. Macro calls may be nested and may be recursive.

Other features that have been added to the language include the availability of boolean and relational operators in expressions, automatic generation of parity bits and entry point PROMs.

The Meta Assembler consists of three separate programs: the Definition Program, the Assembly Program, and the PROM Formatter Program. These programs allow the user to define a unique assembly language, assemble a program written in the user-defined language, and organize the resulting object module into arrays that are compatible with the target ROM/PROM memories.

The Definition Program allows the user to define instruction mnemonics and their associated formats. Instruction lengths may vary from 1 to 128 bits. An instruction format is defined by breaking the microword into fields as variables, constants, or "don't care" bits. The variable fields are filled in at Assembly time. Default values and certain permanent attributes may also be assigned to variable fields at Definition time. The Definition Program produces an output listing and a disk file which contains the symbols and instruction mnemonics. This Definition file is used by the Assembly program as a reference when assembling a program.

The Assembly Program is similar to a traditional two-pass assembler. A symbolic source program utilizing the mnemonics and symbols defined in the Definition Program is read as input; a program listing and object module are generated as output. The Assembler provides symbolic addressing, relative addressing, paged addressing, and other features found in typical assembly programs. The instruction syntax and assembler directives are compatible with those utilized by AMD in its literature and software products. Additional directives have been implemented for versatile listing and output controls.

Both the Definition Program and the Assembly Program are implemented with Conditional Assembly Operators. Conditional statements may be nested up to 16 levels and can be made dependent on general expressions, character string equality, and symbol definition status. A full cross reference table is provided in both programs.

The following directives are included in Microtec's Macro Meta Assembler Program:

MACRO	–	Define a Macro
ENDM	–	End a Macro Definition
EXITM	–	Alternate Macro Exit
LOCAL	–	Define a Macro Local Symbol
IF	–	Conditional Assembly if Expression is Non-Zero
ELSE	–	Conditional Assembly Statement Converse
ENDIF	–	Conditional Assembly Statement End
IFC	–	Conditional Assembly if Character Strings Compare
IFNC	–	Conditional Assembly if Character Strings Don't Compare
IFD	–	Conditional Assembly if Symbol Defined
IFND	–	Conditional Assembly if Symbol Not Defined
MAP	–	Generate Entry Point Table
DUP	–	Duplicate a Line (in timesharing version of AMDASM)
DATA	–	Define Data Word (in timesharing version of AMDASM)

The PROM Formatter Program reads the object module produced by the Assembly Program and translates the format into one that can be read by a PROM programmer. BNPF, Data I/O ASCII hexadecimal, and the Step Engineering format are supported. Microwords in the object module can be divided into organizations that are compatible with the target PROM/ROM array. The length and width of PROMS may be specified as well as the value of "don't care" bits. The PROM Formatter has three new features that add to the versatility of the program: single bit parity generation; column switching; and column overlaying.

The Macro Meta Assembler is written in ANSI Fortran and will run on any general purpose digital computer that has a Fortran IV compiler, a word length of at least 16 bits, a disk or magnetic tape facility and 20–24K words of program memory. In most systems these programs can be run in an overlayed mode if the required memory is not available.

The programs are well commented and modular. A detailed manual, source listing, test programs, and test program output listings accompany each software order. The test programs allow the operation of the software to be verified quickly and easily. A manual is available for a small fee, if further information is desired.

For additional information, contact Microtec, P.O. Box 60337, Sunnyvale, California 94088. Telephone (408) 733-2919.

*This information was provided by Microtec. AMD is not associated with Microtec and does not guarantee their products.

Meta Assembler Program from Microtec*

Microtec has available a Meta Assembler program for the AMD 2900 microprocessor and other similar microprogrammable microprocessors. The Assembler is compatible with AMD's AMDASM program, but is written in ANSI standard Fortran IV and will run on any machine that has:

1. A Fortran IV compiler
2. A word length of at least 16 bits
3. A disc or magnetic tape facility
4. 18K words of Random Access Memory
   (in most systems these programs can be run in an overlayed mode if the required memory is not available)

The Meta Assembler Software Package actually consists of three separate programs, a Definition Program, an Assembly Program, and a PROM Formatter Program.

The Definition Program allows the user to define instruction mnemonics and their associated formats. Instruction lengths may vary from 1 to 128 bits. Symbolic Constants and reserved words may also be defined in the Definition Program. An instruction format is defined by breaking the microword into fields and defining the fields as constants, don't care bits, or variables which are filled in at assembly time. Default values and certain permanent attributes may also be assigned to variable fields at Definition time. The Definition Program produces an output listing and a disk file consisting of the defined symbols and instruction mnemonics. This Definition file is used by the Assembly program as a reference when assembling a program.

The Assembly program operates like a traditional assembler. A symbolic source program utilizing the mnemonics and symbols defined in the Definition Program is read as input, and a listing and object module are generated as output. The Assembler provides symbolic addressing, relative addressing, paged addressing, and other features found in typical assembly programs. The instruction syntax and assembler directives are compatible with those utilized by AMD in its literature and software products. Additional directives have been implemented to provide for versatile listing and output controls.

Conditional Assembly statements are provided in both the Definition and Assembly programs. These statements may be nested up to 16 levels and can be made dependent on general expression. A full cross reference table is also provided in both programs.

Some features of Microtec's Meta Assembler are particularly helpful when assembling code for microprogrammable machines. The existence of don't care bits and instruction overlaying are included among these features. Bits of a microword which are not relevant to a particular instruction format may be defined as don't care bits. Don't care bits are printed as X's on the listing and do not have to be defined until the PROM Formatter program is executed. An instruction format with don't care bits can be overlayed with other instruction formats. Therefore when useful, an instruction format can be used to define only part of the microword, padding out the word with don't care bits.

The PROM Formatter Program reads the object module file produced by the Assembly program and translates the format into one that can be read by a PROM programmer. Both BNPF and Data I/O's ASCII hexadecimal format are supported. Microwords in the object module can be broken up into organizations that are compatible with the target PROM/ROM array. Users may specify PROMs of any width and length, as well as the value of don't care bits. Any or all PROMs may be listed and/or punched.

The programs are well commented and modular. A detailed manual, source listing, test programs, and test program output listings accompany each software order. The test programs allow the operation of the software to be verified quickly and easily. If the information given here is not sufficient, a manual is available for a small fee.

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*This information was provided by Microtec. AMD is not associated with Microtec, and does not guarantee their products.

Videotape Seminar Kits

Advanced Micro Devices regularly prepares and presents seminars worldwide that describe the function and application of its Am2900 Family products. These seminars may also be presented at local factory or design centers through arrangement with the Field Applications Engineer located at the local AMD Sales Office.

It is now also possible to order the following seminars in videotape form with literature kits.

- **Am29116 Sixteen-Bit Bipolar Microprocessor and Peripherals**
- **Am29500 Array Processing/Digital Signal Processing Family**

The videotape is a 2–3 hour seminar covering the products function in detail and demonstrating aspects of system integration using the products. The literature kit includes a slide booklet, data sheets of all products covered in the seminar, and other relevant material.

These kits may be ordered from AMD's Customer Education Center. Contact your AMD Sales Representative for more information.

	Order Code	Price (USA)
Am29116 Sixteen-Bit Bipolar Microprocessor and Peripherals		
– Videotape (includes one set of literature)	Am29116–VIDEO	$99/Videotape
– Literature Kit (each additional set)	Am29116–LIT	$5/set
Am29500 Array Processing (Digital Signal Processing Family)		
– Videotape (includes one set of literature)	Am29116–VIDEO	$99/Videotape
– Literature Kit (each additional set)	Am29116–LIT	$5/set

Am2960-2970
Dynamic Memory Support Index

A New Generation of Am2960 Family Memory Support Products

Advanced Micro Devices and Motorola have agreed to cooperate on the development of the next generation of the Am2960 Family of Memory Support products. These devices are designed to maximize the speed and minimize the cost of memory systems based on the new generation of high performance 64K and 256K MOS Dynamic RAMs (DRAMs).

The products included in this joint development and alternate sourcing agreement are a Dynamic Memory Controller (DMC), the Am2968, and two Memory Timing Controllers (MTC), the Am2969 and Am2970. These functions are partitioned such that address generation and refresh are provided by the Am2968. Memory timing and control is achieved with either the Am2969 or Am2970. This partitioning allows greater design flexibility and higher system performance than would be possible by combining the DMC and MTC functions on a single chip. All three devices will be fabricated using the high performance, oxide-isolated bipolar technologies with TTL compatible I/O levels.

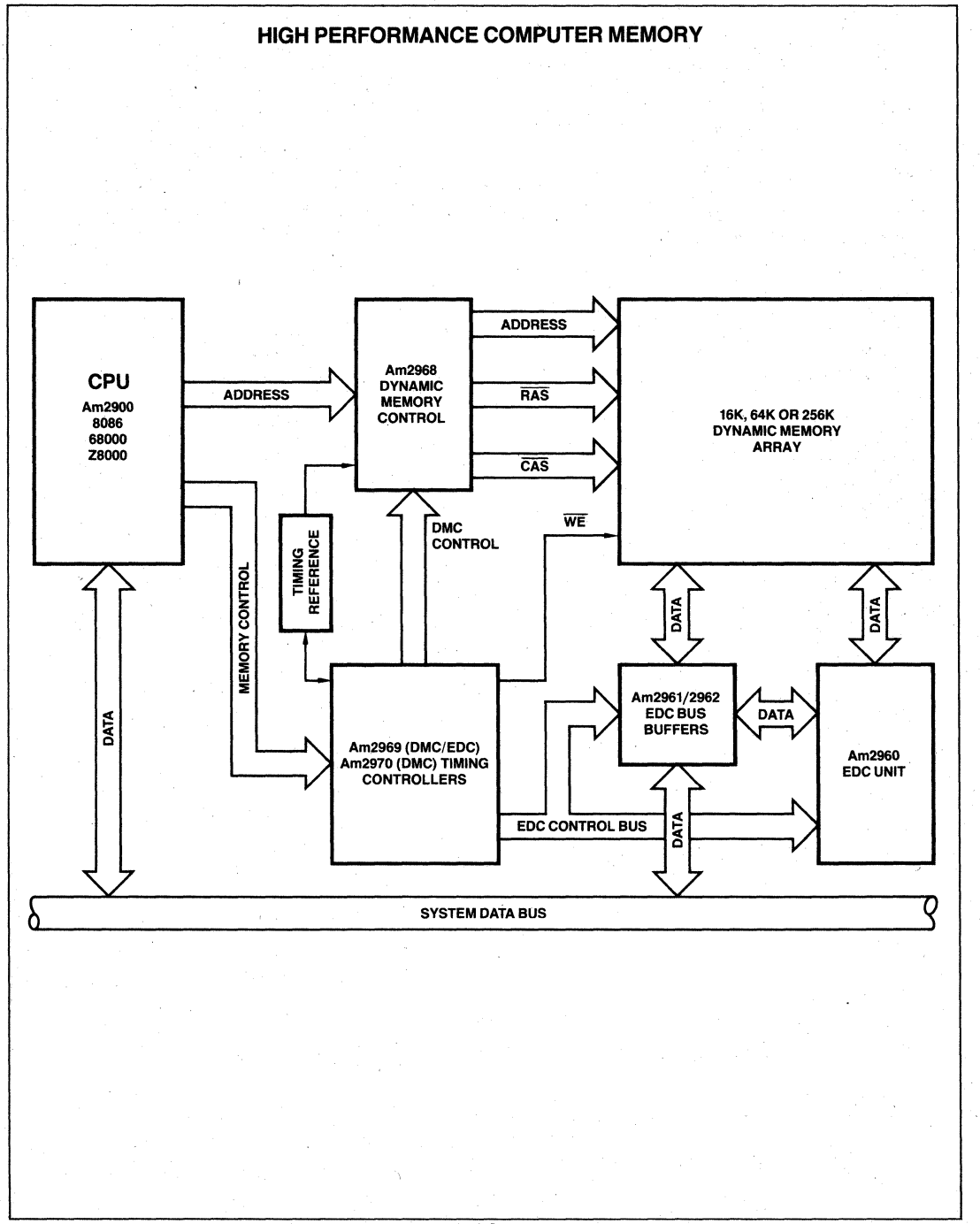
The Dynamic Memory Controller, Am2968, will provide complete address multiplexing, refreshing, and output drive for up to 88 Dynamic Random Access Memories (DRAMs). The Am2968 will be packaged in a 48-pin DIP and will interface with 16K, 64K or 256K DRAMs.

The memory timing controller will be available in two versions. The Am2969, a 48-pin version, will provide all control signals for both the Am2968 Memory Controller and the existing Am2960 Error Detection and Correction circuit (EDC). The Am2969 Timing Controller will support error logging and also handle memory initialization, refresh timing, and memory cycle arbitration. The general purpose microprocessor interface on the Am2969 will facilitate its use with most microprocessors with minimal external logic. The AMD/Intel iAPX86, MC68000 and AMD 2900 bit-slice and 29116 devices are notable examples. System timing for all memory functions is derived from an external delay line to provide maximum performance and flexibility.

For systems not utilizing the Am2960 Error Detection and Correction circuit (EDC), a second version of the timing controller, the Am2970, will be available without EDC interface/functions. The Am2970 will save on IC cost and board space as it will be packaged in 24-pin, 300-mil wide DIP.

Sample quantities on the Am2968 and the Am2970 are expected in the fourth quarter 1983, with production commencing early in 1984.

The Next Generation of Dynamic Memory Support Products



The Am2960 Family Dynamic Memory Support Products

Advanced Micro Devices has developed a set of bipolar high-performance memory-support products to maximize the speed and reliability of MOS dynamic RAM systems. This family is designed to provide, in the minimum package count, all the logic, interface and control functions required in the address and data paths of memory systems based on 16K and 64K devices.

These TTL-compatible products are specified for use in equipment based on either bipolar or MOS CPUs. The Am2960 Series serves bipolar microprocessors such as the Am2901, Am29203, etc., while the AmZ8160 Series serves MOS microprocessors, such as the 16-bit AmZ8000.

Key System Level Features

Maximum Memory Performance

- Schottky performance with matched T_{PD} paths and skew limit guarantees.
- Optimized interface devices for maximum speed.
- Hamming code EDC with internal ECL circuitry for maximum speed combined with maximum memory reliability.

Lowest Package Count Plus Maximum Flexibility

- LSI DMC Controller is designed for up to 64K RAMs.
- EDC is 16-bit expandable slice with byte I/O controls.
- Flexible interface for speed or minimum parts count.

Operation in Any Timing Environment

- Synchronous Clock Timing (AmZ8000 systems).
- Delay-line timing for maximum performance.

Operation with Any RAM Refresh Mode

- 128 of 256 Line Refresh

All Refresh Modes

- Burst Refresh
- Hidden (transparent) Refresh
- Cycle Steal Refresh

Am2960 Family Product Summary

Am2960 • AmZ8160 Error Detection and Correction (EDC)

- High-speed 16-bit slice expandable to 64 bits
- Single-bit correction/double-bit detection
- Byte-op controls
- Initialization and diagnostics built-in

Am2961/62 • AmZ8161/62 EDC Data Bus Buffer

- EDC interface between RAM, EDC and data bus
- 24mA bus drive with three-state control
- Separated RAM I/O with undershoot protection
- Bus latches for byte-op or multiplexed buses

AmZ8163 EDC and Refresh Control for AmZ8000 Systems

- RAS/MUX/CAS timing control for AmZ8164
- EDC control for word or byte read and write
- Memory/refresh request arbitration
- Refresh timer and control independent of CPU

Am2964 • AmZ8164 Dynamic Memory Control (DMC)

- 16-bit address for up to 64K RAMs
- Refresh Counter for 128- or 256-line refresh
- 3-port 8-bit Schottky speed address MUX
- RAS and CAS paths on-chip for minimum skew

Am2965/66 • AmZ8165/66 Octal Dynamic RAM Drivers

- −0.5V maximum undershoot
- V_{OH}/I_{OH} specs for MOS with no external resistors
- t_{PLH}/t_{PHL} min and max specs for 50pF and 500pF
- Pin-compatible with 'S240/244

Am2960 • Am2960-1 • Am2960A Fast Error Detection and Correction for Memories

Corrects All Single-Bit Errors

Corrects all single bit errors. Detects all double and some triple bit errors.

Expandable

One Am2960 provides Error Detection and Correction for 16-bits. Two Am2960s handle 32 bits; four Am2960s handle 64 bits.

Fast

Worst case 32 nanoseconds for error detect and 65 nanoseconds for error correct (16 bits).

Latches Built-In

Check Bit, Data, and Diagnostic latches are built-in to save MSI.

Flexible

Can be used with Am2900-based designs, the AmZ8000 or other processors.

Diagnostics Built-In

Logic on-chip for device test and software-controlled diagnostics.

Increases Memory Reliability

And can significantly reduce field maintenance costs.

A Must for 64K RAMs

Alpha error rates are several times higher for 64K RAMs than 16Ks.

Also available as the AmZ8160 for AmZ8000 Systems

Am2960 • Am2960-1 Am2960A

Cascadable 16-Bit Error Detection and Correction Unit

4

DISTINCTIVE CHARACTERISTICS

- **Boosts Memory Reliability**
  Corrects all single-bit errors. Detects all double and some triple-bit errors. Reliability of dynamic RAM systems is increased more than 60-fold.
- **Very High Speed**
  Perfect for MOS microprocessor, minicomputer, and mainframe systems.
  - Data in to error detect: 32ns worst case.
  - Data in to corrected data out: 65ns worst case.

  High performance systems can use the Am2960 EDC in check-only mode to avoid memory system slowdown.
- **Replaces 25 to 50 MSI chips**
  All necessary features are built-in to the Am2960 EDC, including diagnostics, data in, data out, and check bit latches.
- **Handles Data Words From 8 to 64 Bits**
  The Am2960 EDC cascades: 1 EDC for 8 or 16 bits, 2 for 32 bits, 4 for 64 bits.
- **Easy Byte Operations**
  Separate byte enables on the data out latch simplify the steps and cuts the time required for byte writes.
- **Diagnostics Built-In**
  The processor may completely exercise the EDC under software control to check for proper operation of the EDC.

GENERAL DESCRIPTION

The Am2960 Error Detection and Correction Unit (EDC) contains the logic necessary to generate check bits on a 16-bit data field according to a modified Hamming Code, and to correct the data word when check bits are supplied. Operating on data read from memory, the Am2960 will correct any single bit error and will detect all double and some triple bit errors. For 16-bit words, 6 check bits are used. The Am2960 is expandable to operate on 32-bit words (7 check bits) and 64-bit words (8 check bits). In all configurations, the device makes the error syndrome available on separate outputs for data logging.

The Am2960 also features two diagnostic modes, in which diagnostic data can be forced into portions of the chip to simplify device testing and to execute system diagnostic functions. The product is supplied in a 48 lead hermetic DIP package.

TABLE OF CONTENTS

ADVANCED INFORMATION

Am2960-1

- Speed selected version of Am2960 on the critical data paths
- Plug-in replacement for Am2960

Am2960A

- Second generation of Am2960 EDC internal ECL circuitry and state-of-the-art process technology combined to provide fastest version of popular Am2960.
- Plug-in replacement for Am2960
- Improved speed
  25–30% speed improvement on the critical paths versus the Am2960

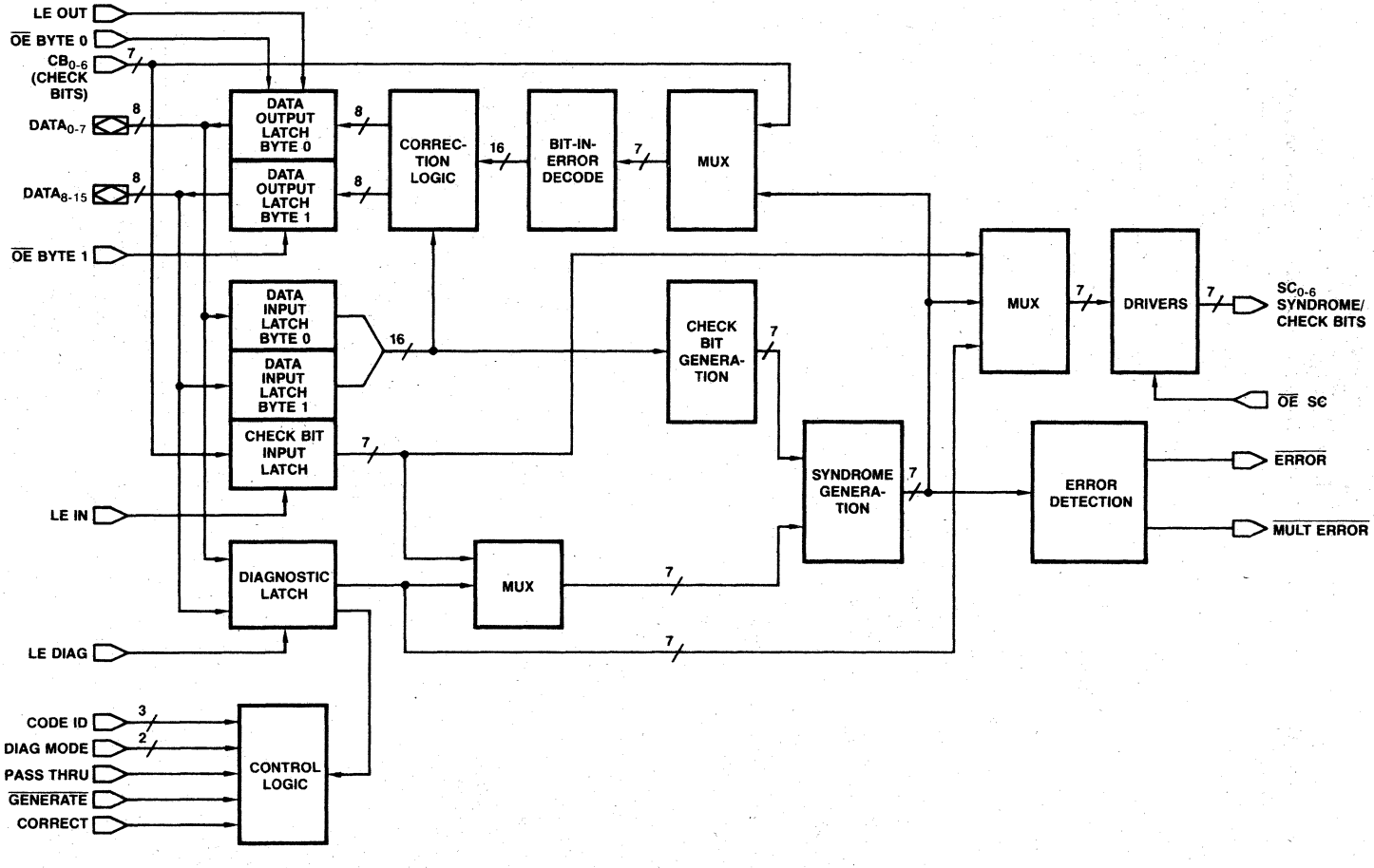
Am2960-1

- Speed selected version of Am2960 on the critical data paths.
- Plug-in replacement for Am2960.

Am2960A

- Second generation of Am2960 EDC internal ECL circuitry and state-of-the-art process technology combined to provide fastest version of popular Am2960.
- Plug-in replacement for Am2960.
- Improved speed
  25–30% speed improvement on the critical paths versus the Am2960.

BLOCK DIAGRAM



MPR-729

EDC Architecture

The EDC Unit is a powerful 16-bit cascadable slice used for check bit generation, error detection, error correction and diagnostics.

As shown in the block diagram, the device consists of the following:

- Data Input Latch
- Check Bit Input Latch
- Check Bit Generation Logic
- Syndrome Generation Logic
- Error Detection Logic
- Error Correction Logic
- Data Output Latch
- Diagnostic Latch
- Control Logic

Data Input Latch

16 bits of data are loaded from the bidirectional DATA lines under control of the Latch Enable input, LE IN. Depending on the control mode the input data is either used for check bit generation or error detection/correction.

Check Bit Input Latch

Seven check bits are loaded under control of LE IN. Check bits are used in the Error Detection and Error Correction modes.

Check Bit Generation Logic

This block generates the appropriate check bits for the 16 bits of data in the Data Input Latch. The check bits are generated according to a modified Hamming code.

Syndrome Generation Logic

In both Error Detection and Error Correction modes, this logic block compares the check bits read from memory against a newly generated set of check bits produced for the data read in from memory. If both sets of check bits match, then there are no errors. If there is a mismatch, then one or more of the data or check bits is in error.

The syndrome bits are produced by an exclusive-OR of the two sets of check bits. If the two sets of check bits are identical (meaning there are no errors) the syndrome bits will be all zeroes. If there are errors, the syndrome bits can be decoded to determine the number of errors and the bit-in-error.

Error Detection Logic

This section decodes the syndrome bits generated by the Syndrome Generation Logic. If there are no errors in either the input data or check bits, the $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ outputs remain HIGH. If one or more errors are detected, $\overline{\text{ERROR}}$ goes LOW. If two or more errors are detected, both $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ go LOW.

Error Correction Logic

For single errors, the Error Correction Logic complements (corrects) the single data bit in error. This corrected data is loadable into the Data Output Latch, which can then be read onto the bidirectional data lines. If the single error is one of the check bits, the correction logic does not place corrected check bits on the syndrome/check bit outputs. If the corrected check bits are needed the EDC must be switched to Generate Mode.

Data Output Latch

The Data Output Latch is used for storing the result of an error correction operation. The latch is loaded from the correction logic under control of the Data Output Latch Enable, LE OUT. The Data Output Latch may also be loaded directly from the Data Input Latch under control of the PASS THRU control input.

The Data Output Latch is split into two 8-bit (byte) latches which may be enabled independently for reading onto the bidirectional data lines.

Diagnostic Latch

This is a 16-bit latch loadable from the bidirectional data lines under control of the Diagnostic Latch Enable, LE DIAG. The Diagnostic Latch contains check bit information in one byte and control information in the other byte. The Diagnostic Latch is used for driving the device when in Internal Control Mode, or for supplying check bits when in one of the Diagnostic Modes.

Control Logic

The control logic determines the specific mode the device operates in. Normally the control logic is driven by external control inputs. However, in Internal Control Mode, the control signals are instead read from the Diagnostic Latch.

PIN DEFINITIONS

$DATA_{0-15}$ 16 bidirectional data lines. They provide input to the Data Input Latch and Diagnostic Latch, and receive output from the Data Output Latch. $DATA_0$ is the least significant bit; $DATA_{15}$ the most significant.

CB_{0-6} Seven Check Bit input lines. The check bit lines are used to input check bits for error detection. Also used to input syndrome bits for error correction in 32 and 64-bit configurations.

LE IN Latch Enable – Data Input Latch. Controls latching of the input data. When HIGH the Data Input Latch and Check Bit Input Latch follow the input data and input check bits. When LOW, the Data Input Latch and Check Bit Input Latch are latched to their previous state.

$\overline{\text{GENERATE}}$ Generate Check Bits input. When this input is LOW the EDC is in the Check Bit Generate Mode. When HIGH the EDC is in the Detect Mode or Correct Mode.

In the Generate Mode the circuit generates the check bits or partial check bits specific to the data in the Data Input Latch. The generated check bits are placed on the SC outputs.

In the Detect or Correct Modes the EDC detects single and multiple errors, and generates syndrome bits based upon the contents of the Data Input Latch and Check Bit Input Latch. In Correct Mode, single-bit errors are also automatically corrected – corrected data is placed at the inputs of the Data Output Latch. The syndrome result is placed on the SC outputs and indicates in a coded form the number of errors and the bit-in-error.

SC_{0-6} Syndrome/Check Bit outputs. These seven lines hold the check/partial-check bits when the EDC is in Generate Mode, and will hold the syndrome/partial syndrome bits when the device is in Detect or Correct Modes. These are 3-state outputs.

$\overline{\text{OE SC}}$ Output Enable – Syndrome/Check Bits. When LOW, the 3-state output lines SC_{0-6} are enabled. When HIGH, the SC outputs are in the high impedance state.

$\overline{\text{ERROR}}$ Error Detected output. When the EDC is in Detect or Correct Mode, this output will go LOW if one or more syndrome bits are asserted, meaning there are one or more bit errors in the data or check bits. If no syndrome bits are asserted, there are no errors detected and the output will be HIGH. In Generate Mode, $\overline{\text{ERROR}}$ is forced HIGH. (In a 64-bit configuration, $\overline{\text{ERROR}}$ must be externally implemented.)

$\overline{\text{MULT ERROR}}$ Multiple Errors Detected output. When the EDC is in Detect or Correct Mode, this output if LOW indicates that there are two or more bit errors that have been detected. If HIGH this indicates that either one or no errors have been detected. In Generate mode, $\overline{\text{MULT ERROR}}$ is forced HIGH. (In a 64-bit configuration, $\overline{\text{MULT ERROR}}$ must be externally implemented.)

CORRECT Correct input. When HIGH this signal allows the correction network to correct any single-bit error in the Data Input Latch (by complementing the bit-in-error) before putting it onto the Data Output Latch. When LOW the EDC will drive data directly from the Data Input Latch to the Data Output Latch without correction.

LE OUT Latch Enable – Data Output Latch. Controls the latching of the Data Output Latch. When LOW the Data Output Latch is latched to its previous state. When HIGH the Data Output Latch follows the output of the Data Input Latch as modified by the correction logic network. In Correct Mode, single-bit errors are corrected by the network before loading into the Data Output Latch. In Detect Mode, the contents of the Data Input Latch are passed through the correction network unchanged into the Data Output Latch. The inputs to the Data Output Latch are unspecified if the EDC is in Generate Mode.

$\overline{\text{OE}}$ BYTE 0, $\overline{\text{OE}}$ BYTE 1 Output Enable – Bytes 0 and 1, Data Output Latch. These lines control the 3-state outputs for each of the two bytes of the Data Output Latch. When LOW these lines enable the Data Output Latch and when HIGH these lines force the Data Output Latch into the high impedance state. The two enable lines can be separately activated to enable only one byte of the Data Output Latch at a time.

PASS THRU Pass Thru input. This line when HIGH forces the contents of the Check Bit Input Latch onto the Syndrome/Check Bit outputs (SC_{0-6}) and the unmodified contents of the Data Input Latch onto the inputs of the Data Output Latch.

DIAG $MODE_{0-1}$ Diagnostic Mode Select. These two lines control the initialization and diagnostic operation of the EDC.

CODE ID_{0-2} Code Identification inputs. These three bits identify the size of the total data word to be processed and which 16-bit slice of larger data words a particular EDC is processing. The three allowable data word sizes are 16, 32 and 64 bits and their respective modified Hamming codes are designated 16/22, 32/39 and 64/72. Special CODE ID input 001 (ID_2, ID_1, ID_0) is also used to instruct the EDC that the signals CODE ID_{0-2}, DIAG $MODE_{0-1}$, CORRECT and PASS THRU are to be taken from the Diagnostic Latch, rather than from the input control lines.

LE DIAG Latch Enable – Diagnostic Latch. When HIGH the Diagnostic Latch follows the 16-bit data on the input lines. When LOW the outputs of the Diagnostic Latch are latched to their previous states. The Diagnostic Latch holds diagnostic check bits, and internal control signals for CODE ID_{0-2}, DIAG $MODE_{0-1}$, CORRECT and PASS THRU.

FUNCTIONAL DESCRIPTION

The EDC contains the logic necessary to generate check bits on a 16-bit data field according to a modified Hamming code. Operating on data read from memory, the EDC will correct any single-bit error, and will detect all double and some triple-bit errors. The Am2960 may be configured to operate on 16-bit data words (with 6 check bits), 32-bit data words (with 7 check bits) and 64-bit data words (with 8 check bits). In fact the EDC can be configured to work on data words from 8 to 64 bits. In all configurations, the device makes the error syndrome bits available on separate outputs for error data logging.

Code and Byte Specification

The EDC may be configured in several different ways and operates differently in each configuration. It is necessary to indicate to the device what size data word is involved and which bytes of the data word it is processing. This is done with input lines CODE ID_{0-2}, as shown in Table I. The three modified Hamming codes referred to in Table I are:

- 16/22 – 16 data bits
  – 6 check bits
  – 22 bits in total.
- 32/39 code – 32 data bits
  – 7 check bits
  – 39 bits in total.
- 64/72 code – 64 data bits
  – 8 check bits
  – 72 bits in total.

CODE ID input 001 (ID_2, ID_1, ID_0) is a special code used to operate the device in Internal Control Mode (described later in this section).

Control Mode Selection

The device control lines are $\overline{\text{GENERATE}}$, CORRECT, PASS THRU, DIAG $MODE_{0-1}$ and CODE ID_{0-2}. Table III indicates the operating modes selected by various combinations of the control line inputs.

Diagnostics

Table II shows specifically how DIAG $MODE_{0-1}$ select between normal operation, initialization and one of two diagnostic modes.

The Diagnostic Modes allow the user to operate the EDC under software control in order to verify proper functioning of the device.

Check and Syndrome Bit Labeling

The check bits generated in the EDC are designated as follows:

- 16-bit configuration – CX C0, C1, C2, C4, C8;
- 32-bit configuration – CX, C0, C1, C2, C4, C8, C16;
- 64-bit configuration – CX, C0, C1, C2, C4, C8, C16, C32.

Syndrome bits are similarly labeled SX through S32. There are only 6 syndrome bits in the 16-bit configuration, 7 for 32 bits and 8 syndrome bits in the 64-bit configuration.

Initialize Mode

The inputs of the Data Output Latch are forced to zeroes. The check bit outputs (SC) are generated to correspond to the all-zero data. $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ are forced HIGH in the Initialize Mode.

Initialize Mode is useful after power up when RAM contents are random. The EDC may be placed in initialize mode and its' outputs written in to all memory locations by the processor.

TABLE I. HAMMING CODE AND SLICE IDENTIFICATION.

CODE ID_2	CODE ID_1	CODE ID_0	Hamming Code and Slice Selected
0	0	0	Code 16/22
0	0	1	Internal Control Mode
0	1	0	Code 32/39, Bytes 0 and 1
0	1	1	Code 32/39, Bytes 2 and 3
1	0	0	Code 64/72, Bytes 0 and 1
1	0	1	Code 64/72, Bytes 2 and 3
1	1	0	Code 64/72, Bytes 4 and 5
1	1	1	Code 64/72, Bytes 6 and 7

TABLE II. DIAGNOSTIC MODE CONTROL.

DIAG $MODE_1$	DIAG $MODE_0$	Diagnostic Mode Selected
0	0	**Non-diagnostic mode.** The EDC functions normally in all modes.
0	1	**Diagnostic Generate.** The contents of the Diagnostic Latch are substituted for the normally generated check bits when in the Generate Mode. The EDC functions normally in the Detect or Correct modes.
1	0	**Diagnostic Detect/Correct.** In the Detect or Correct Mode, the contents of the Diagnostic Latch are substituted for the check bits normally read from the Check Bit Input Latch. The EDC functions normally in the Generate Mode.
1	1	**Initialize.** The outputs of the Data Input Latch are forced to zeroes (and latched upon removal of the Initialize Mode) and the check bits generated correspond to the all-zero data.

HAMMING CODE SELECTION

The Am2960 EDC uses a modified Hamming Code that allows 1) the EDC to be cascaded, 2) all double errors to be detected, 3) the gross error conditions of all 0s or 1s to be detected.

The error correction code can be selected independent of the processor with the exception of diagnostics software.

Diagnostic software run by a processor to checkout the EDC system must know specifically which code is being used. This is only a problem when the EDC replaces an existing MSI implementation on an existing computer. In this case, the computer's software must first determine which of two codes (the old one used by the MSI implementation or the new one used by the EDC) is used by the computer's memory system.

This is easily determined by writing a test data word into memory and then examining whether the generated check bits are typical of the old or the new code. From then on the software runs only the diagnostic appropriate for the code used on that particular computer's memory system.

TABLE III. Am2960 OPERATING MODES

Operating Mode	Diagnostic Mode**		$\overline{\text{GENERATE}}$	
	DM_1	DM_0	0	1
Normal	0	0	Generate	Correct*
Diagnostic Generate	0	1	Diagnostic Generate	Correct*
Diagnostic Correct	1	0	Generate	Diagnostic Correct*
Initialize	1	1	Initialize	Initialize
Pass Thru	When PASS THRU is asserted the Operating Mode is defaulted to the Pass Thru Mode.			

*Correct if the CORRECT Input is HIGH, Detect if the CORRECT Input is LOW.
**In Code $ID_{2\text{-}0}$ 001 (ID_2, ID_1, ID_0) DM_1 and DM_0 are taken from the Diagnostic Latch.

FUNCTIONAL DESCRIPTION – 16-BIT DATA WORD CONFIGURATION

The 16-bit format consists of 16 data bits, 6 check bits and is referred to as 16/22 code (see Figure 5.)

The 16-bit configuration is shown in Figure 6.

Generate Mode

In this mode check bits will be generated that correspond to the contents of the Data Input Latch. The check bits generated are placed on the outputs SC_{0-5} (SC_6 is a logical one, or high).

Check bits are generated according to a modified Hamming code. Details of the code for check bit generation are contained in Table IV. Each check bit is generated as either an XOR or XNOR of eight of the 16 data bits as indicated in the table. The XOR function results in an even parity check bit, the XNOR is an odd parity check bit.

Figure 1 shows the data flow in the Generate Mode.

Detect Mode

In this mode the device examines the contents of the Data Input Latch against the Check Bit Input Latch, and will detect all single-bit errors, all double-bit errors and some triple-bit errors. If one or more errors are detected, $\overline{\text{ERROR}}$ goes LOW. If two or more errors are detected, $\overline{\text{MULT ERROR}}$ goes LOW. Both error indicators are HIGH if there are no errors.

Also available on device outputs SC_{0-5} are the syndrome bits generated by the error detection step. The syndrome bits may be decoded to determine if a bit error was detected and, for single-bit errors, which of the data or check bits is in error. Table V gives the chart for decoding the syndrome bits generated by the 16-bit configuration (as an example, if the syndrome bits SX/S0/S1/S2/S4/S8 were 101001 this would be decoded to indicate that there is a single-bit error at data bit 9). If no error is detected the syndrome bits will all be zeroes.

In Detect Mode, the contents of the Data Input Latch are driven directly to the inputs of the Data Output Latch without correction.

Correct Mode

In this mode, the EDC functions the same as in Detect Mode except that the correction network is allowed to correct (complement) any single-bit error of the Data Input Latch before putting it onto the inputs of the Data Output Latch. (see Figure 2.) If multiple errors are detected, the output of the correction network is unspecified. If the single-bit error is a check bit there is no automatic correction. If check bit correction is desired, this can be done by placing the device in Generate Mode to produce a correct check bit sequence for the data in the Data Input Latch.

Pass Thru Mode

In this mode, the unmodified contents of the Data Input Latch are placed on the inputs of the Data Output Latch and the contents of the Check Bit Input Latch are placed on outputs SC_{0-5}. $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ are forced HIGH in this mode.

Diagnostic Latch

The Diagnostic Latch serves both for diagnostic uses and internal control uses. It is loaded from the DATA lines under the control of LE DIAG. Table VI shows the loading definitions for the DATA lines.

Diagnostic Generate
Diagnostic Detect
Diagnostic Correct

These are special diagnostic modes selected by DIAG $MODE_{0-1}$ where either normal check bit inputs or outputs are substituted for by check bits loaded into the Diagnostic Latch. See Table III for details. Figures 3 and 4 illustrate the flow of data during the two diagnostic modes.

Internal Control Mode

This mode is selected by CODE ID_{0-2} input 001 (ID_2, ID_1, ID_0).

When in Internal Control Mode, the EDC takes the CODE ID_{0-2}, DIAG $MODE_{0-1}$, CORRECT and PASS THRU control signals from the internal Diagnostic Latch rather than from the external input lines.

Table VI gives the format for loading the Diagnostic Latch.

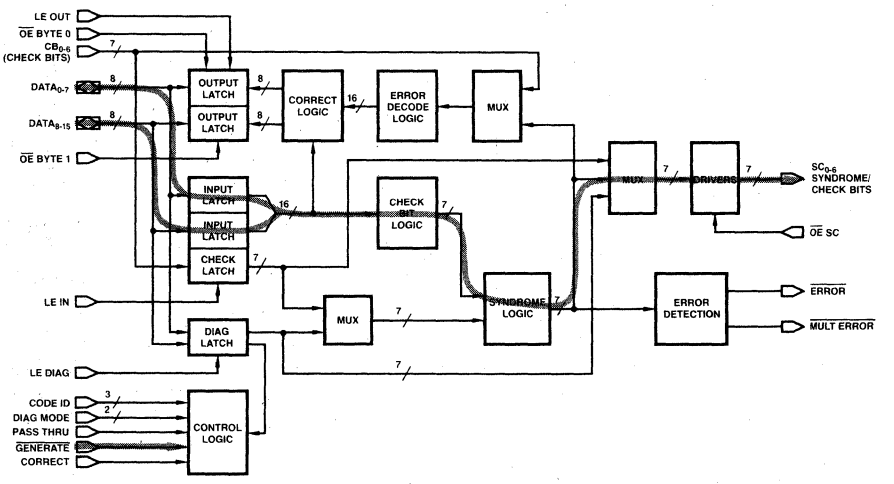


Figure 1. Check Bit Generation

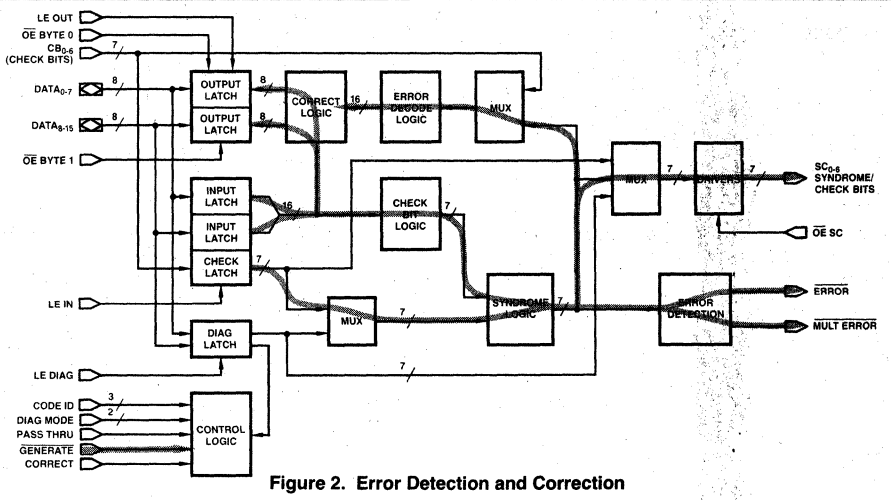


Figure 2. Error Detection and Correction

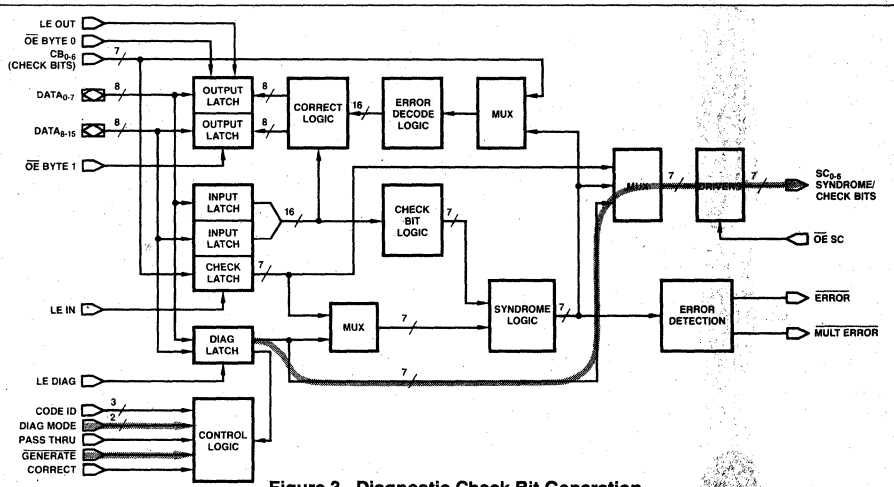


Figure 3. Diagnostic Check Bit Generation

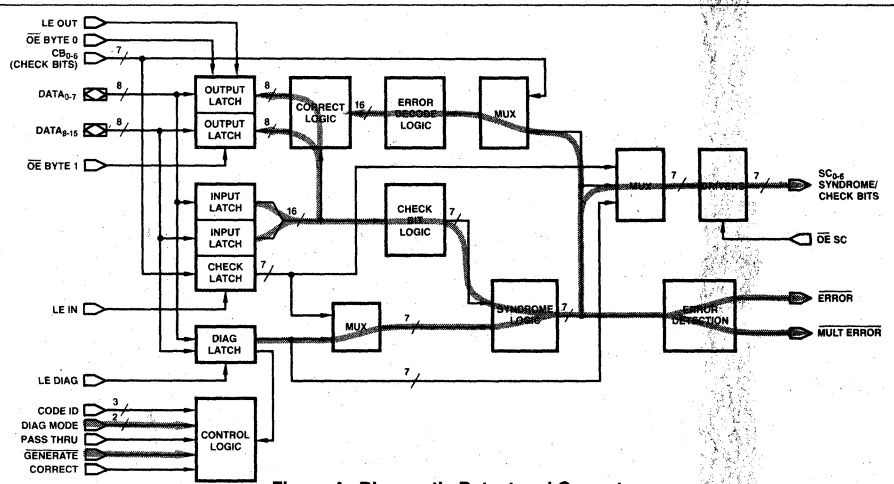
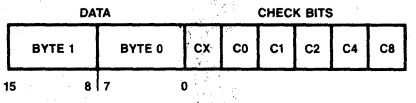


Figure 4. Diagnostic Detect and Correct



Uses Modified Hamming Code 16/22
- 16 data bits
- 6 check bits
- 22 bits in total

Figure 5. 16-Bit Data Format

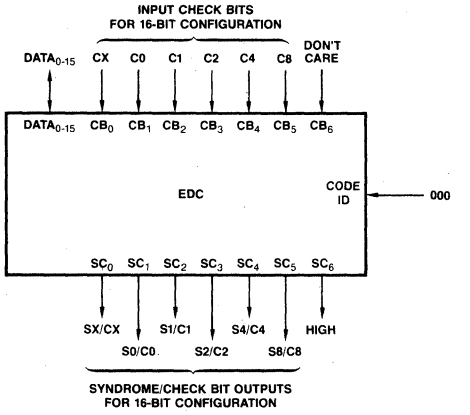


Figure 6. 16-Bit Configuration

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TABLE IV. 16-BIT MODIFIED HAMMING CODE – CHECK BIT ENCODE CHART.

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X

The check bit is generated as either an XOR or XNOR of the eight data bits noted by an "X" in the table.

TABLE V. SYNDROME DECODE TO BIT-IN-ERROR.

Syndrome Bits			S8	0	1	0	1	0	1	0	1
			S4	0	0	1	1	0	0	1	1
			S2	0	0	0	0	1	1	1	1
SX	S0	S1									
0	0	0		*	C8	C4	T	C2	T	T	M
0	0	1		C1	T	T	15	T	13	7	T
0	1	0		C0	T	T	M	T	12	6	T
0	1	1		T	10	4	T	0	T	T	M
1	0	0		CX	T	T	14	T	11	5	T
1	0	1		T	9	3	T	M	T	T	M
1	1	0		T	8	2	T	1	T	T	M
1	1	1		M	T	T	M	T	M	M	T

* – no errors detected
Number – the location of the single bit-in-error
T – two errors detected
M – three or more errors detected

TABLE VI. DIAGNOSTIC LATCH LOADING – 16-BIT FORMAT.

Data Bit	Internal Function
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6, 7	Don't Care
8	CODE ID 0
9	CODE ID 1
10	CODE ID 2
11	DIAG MODE 0
12	DIAG MODE 1
13	CORRECT
14	PASS THRU
15	Don't Care

FUNCTIONAL DESCRIPTION – 32-BIT DATA WORD CONFIGURATION

The 32-bit format consists of 32 data bits, 7 check bits and is referred to as 32/39 code (see Figure 7).

The 32-bit configuration is shown in Figure 8.

The upper EDC (Slice 0/1) handles the least significant bytes 0 and 1 – the external DATA lines 0 to 15 are connected to the same numbered inputs of the upper device. The lower EDC (Slice 2/3) handles the most significant bytes 2 and 3 – the external DATA lines for bits 16 to 31 are connected to inputs $DATA_0$ through $DATA_{15}$ respectively.

The valid syndrome and check bit outputs are those of Slice 2/3 as shown in the diagram. In Correct Mode these must be read into Slice 0/1 via the CB inputs and are selected by the MUX as inputs to the bit-in-error decoder (see block diagram), thus requiring external buffering and output enabling of the check bit lines as shown. The $\overline{OE}$ SC signal can be used to control enabling of check bit inputs – when syndrome outputs are enabled, the external check bit inputs will be disabled.

The valid $\overline{ERROR}$ and $\overline{MULT\ ERROR}$ outputs are those of the Slice 2/3. The $\overline{ERROR}$ and $\overline{MULT\ ERROR}$ outputs of Slice 0/1 are unspecified. All of the latch enables and control signals must be input to both of the devices.

Generate Mode

In this mode check bits will be generated that correspond to the contents of the Data Input Latch. The check bits generated are placed on the outputs $SC_{0\text{-}6}$ of Slice 2/3.

Check bits are generated according to a modified Hamming code. Details of the code for check bit generation are contained in Table X. Check bits are generated as either an XOR or XNOR of 16 of the 32 data bits as indicated in the table. The XOR function results in an even parity check bit, the XNOR in an odd parity check bit.

Detect Mode

In this mode the device examines the contents of the Data Input Latch against the Check Bit Input Latch, and will detect all single-bit errors, all double-bit errors and some triple-bit errors. If one or more errors are detected, $\overline{ERROR}$ goes LOW. If two or more errors are detected, $\overline{MULT\ ERROR}$ goes LOW. Both error indicators are HIGH if there are no errors. The valid $\overline{ERROR}$ and $\overline{MULT\ ERROR}$ signals are those of Slice 2/3 – those of Slice 0/1 are undefined.

Also available on Slice 2/3 outputs $SC_{0\text{-}6}$ are the syndrome bits generated by the error detection step. The syndrome bits may be decoded to determine if a bit error was detected and, for single-bit errors, which of the data or check bits is in error. Table VII gives the chart for decoding the syndrome bits generated for the 32-bit configuration (as an example, if the syndrome bits SX/S0/S1/S2/S4/S8/S16 were 0010011 this would be decoded to indicate that there is a single-bit error at data bit 25). If no error is detected the syndrome bits will be all zeroes.

In Detect Mode, the contents of the Data Input Latch are driven directly to the inputs of the Data Output Latch without corrections.

Correct Mode

In this mode, the EDC functions the same as in Detect Mode except that the correction network is allowed to correct (complement) any single-bit error of the Data Input Latch before putting it onto the inputs of the Data Output Latch. If multiple errors are detected, the output of the correction network is unspecified. If the single-bit error is a check bit there is no automatic correction – if desired this would be done by placing the device in Generate Mode to produce a correct check bit sequence for the data in the Data Input Latch.

For data correction, both Slices 0/1 and 2/3 require access to the syndrome bits on Slice 2/3's outputs $SC_{0\text{-}6}$. Slice 2/3 has access to these syndrome bits through internal data paths, but for Slice 0/1 they must be read through the inputs $CB_{0\text{-}6}$. The device connections for this are shown in Figure 8. When in Correct Mode the SC outputs must be enabled so that they are available for reading in through the CB inputs.

Pass Thru Mode

In this mode, the unmodified contents of the Data Input Latch are placed on the inputs of the Data Output Latch and the contents of the Check Bit Input Latch are placed on outputs $SC_{0\text{-}6}$ of Slice 2/3. $\overline{ERROR}$ and $\overline{MULT\ ERROR}$ are forced HIGH in this mode.

TABLE VII. SYNDROME DECODE TO BIT-IN-ERROR.

Syndrome Bits				S16	0	1	0	1	0	1	0	1
				S8	0	0	1	1	0	0	1	1
				S4	0	0	0	0	1	1	1	1
SX	S0	S1	S2									
0	0	0	0		*	C16	C8	T	C4	T	T	30
0	0	0	1		C2	T	T	27	T	5	M	T
0	0	1	0		C1	T	T	25	T	3	15	T
0	0	1	1		T	M	13	T	23	T	T	M
0	1	0	0		C0	T	T	24	T	2	M	T
0	1	0	1		T	1	12	T	22	T	T	M
0	1	1	0		T	M	10	T	20	T	T	M
0	1	1	1		16	T	T	M	T	M	M	T
1	0	0	0		CX	T	T	M	T	M	14	T
1	0	0	1		T	M	11	T	21	T	T	M
1	0	1	0		T	M	9	T	19	T	T	31
1	0	1	1		M	T	T	29	T	7	M	T
1	1	0	0		T	M	8	T	18	T	T	M
1	1	0	1		17	T	T	28	T	6	M	T
1	1	1	0		M	T	T	26	T	4	M	T
1	1	1	1		T	0	M	T	M	T	T	M

* – no errors detected
Numbers – number of the single bit-in-error
T – two errors detected
M – three or more errors detected

Uses Modified Hamming Code 32/39
– 32 data bits
– 7 check bits
– 39 bits in total

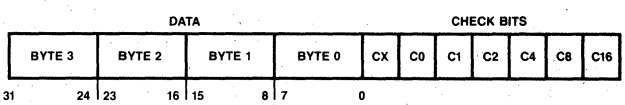

Figure 7. 32-Bit Data Format

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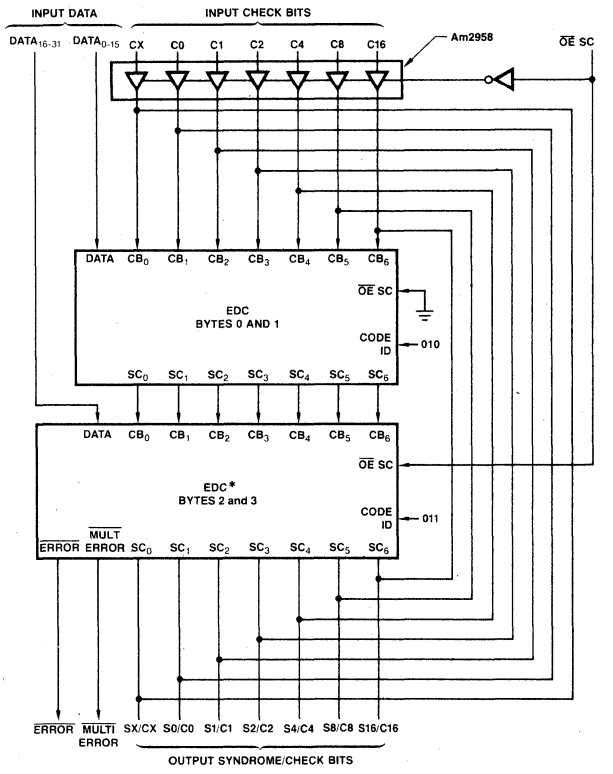


*Check Bit Latch is Forced Transparent in this Code ID Combination for this Slice.

Figure 8. 32-Bit Configuration

TABLE VIII. KEY AC CALCULATIONS FOR THE 32-BIT CONFIGURATION

32-Bit Propagation Delay		Component Delay from Am2960 AC Specifications, Table C
From	To	
DATA	Check Bits Out	(DATA to SC) + (CB to SC, CODE ID 011)
DATA In	Corrected DATA Out	(DATA to SC) + (CB to SC, CODE ID 011) + (CB to DATA, CODE ID 010)
DATA	Syndromes Out	(DATA to SC) + (CB to SC, CODE ID 011)
DATA	$\overline{\text{ERROR}}$ for 32 Bits	(DATA to SC) + (CB to $\overline{\text{ERROR}}$, CODE ID 011)
DATA	$\overline{\text{MULT ERROR}}$ for 32 Bits	(DATA to SC) + (CB to $\overline{\text{MULT ERROR}}$, CODE ID 011)

TABLE IX. DIAGNOSTIC LATCH LOADING – 32-BIT FORMAT.

Data Bit	Internal Function
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6	Diagnostic Check Bit 16
7	Don't Care
8	Slice 0/1 – CODE ID 0
9	Slice 0/1 – CODE ID 1
10	Slice 0/1 – CODE ID 2
11	Slice 0/1 – DIAG MODE 0
12	Slice 0/1 – DIAG MODE 1
13	Slice 0/1 – CORRECT
14	Slice 0/1 – PASS THRU
15	Don't Care
16-23	Don't Care
24	Slice 2/3 – CODE ID 0
25	Slice 2/3 – CODE ID 1
26	Slice 2/3 – CODE ID 2
27	Slice 2/3 – DIAG MODE 0
28	Slice 2/3 – DIAG MODE 1
29	Slice 2/3 – CORRECT
30	Slice 2/3 – PASS THRU
31	Don't Care

TABLE X. 32-BIT MODIFIED HAMMING CODE – CHECK BIT ENCODE CHART.

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)	X				X		X	X	X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								

Generated Check Bits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CX	Even (XOR)		X	X	X		X					X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X

The check bit is generated as either an XOR or XNOR of the sixteen data bits noted by an "X" in the table.

FUNCTIONAL DESCRIPTION – 64-BIT DATA WORD CONFIGURATION

The 64-bit format consists of 64 data bits, 8 check bits and is referred to as 64/72 code (see Figure 9.).

The configuration to process 64-bit format is shown in Figure 6. In this configuration a portion of the syndrome generation and error detection is implemented externally of the EDCs in MSI. For error correction the syndrome bits generated must be read back into all four EDCs through the CB inputs. This necessitates the check bit buffering shown in the connection diagram of Figure 10. The $\overline{OE}$ SC signal can control the check bit enabling – when syndrome bit outputs are enabled the external check bit lines will be disabled so that the syndrome bits may be read onto the CB inputs.

The error detection signals for the 64-bit configuration differ from the 16 and 32-bit configurations. The $\overline{ERROR}$ signal functions the same: it is LOW if one or more errors are detected, and HIGH if no errors are detected. The DOUBLE ERROR signal is HIGH if and only if a double-bit error is detected – it is LOW otherwise. All of the $\overline{MULT\ ERROR}$ outputs of the four devices are valid. $\overline{MULT\ ERROR}$ is LOW for all three ERROR cases and some DOUBLE ERROR combinations. (See TOME definition in Functional Equations section.) It is HIGH if either zero or one errors are detected.

This is a different meaning for $\overline{MULT\ ERROR}$ than in other configurations.

Generate Mode

In this mode check bits will be generated that correspond to the contents of the Data Input Latch. The check bits generated appear at the outputs of the XOR gates as indicated in Figure 10.

Check bits are generated according to a modified Hamming code. Details of the code for check bit generation are contained in Table XII. Check bits are generated as either an XOR or XNOR of 32 of the 64 bits as indicated in the table. The XOR function results in an even parity check bit, the XNOR in an odd parity check bit.

Detect Mode

In this mode the device examines the contents of the Data Input Latch against the Check Bit Input Latch, and will detect all single-bit errors, all double-bit errors and some triple-bit errors. If one or more errors are detected, $\overline{ERROR}$ goes LOW. If exactly two errors are detected, DOUBLE ERROR goes HIGH. If three or more errors are detected, $\overline{MULT\ ERROR}$ goes LOW – the $\overline{MULT\ ERROR}$ output of any of the four EDCs may be used.

Available as XOR gate outputs are the generated syndrome bits (see Figure 10). The syndrome bits may be decoded to determine if a bit error was detected and, for single-bit errors, which of the data or check bits is in error. Table XIII gives the chart for encoding the syndrome bits generated for the 64-bit configuration (as an example, if the syndrome bits SX/S1/S2/S4/S8/S16/S32 were 00100101 this would be decoded to indicate that there is a single-bit error at data bit 41). If no error is detected the syndrome bits will all be zeroes.

In Detect Mode the contents of the Data Input Latch are driven directly to the inputs of the Data Output Latch without corrections.

Correct Mode

In this mode, the EDC functions the same as in Detect Mode except that the correction network is allowed to correct (complement) any single-bit error of the Data Input Latch before putting it onto the inputs of the Data Output Latch. If multiple errors are detected, the output of the correction network is unspecified. If the single bit error is a check bit there is no automatic correction. Check bit correction can be done by placing the device in generate mode to produce a correct check bit sequence for the data in the Data Input Latch.

To perform the correction step, all four slices require access to the syndrome bits which are generated externally of the devices. This access is provided by reading the syndrome bits in through the CB inputs where they are selected as inputs to the bit-in-error decoder by the multiplexer (see block diagram). The device connections for this are shown in Figure 10. When in Correct Mode the SC outputs must be enabled so that the syndrome bits are available at the CB inputs.

Pass Thru Mode

In this mode, the unmodified contents of the Data Input Latch are placed on the inputs of the Data Output Latch, and the contents of the Check Bit Input Latch are passed through the external XOR network and appear inverted at the XOR gate outputs labeled CX to C32 (see Figure 10).

Diagnostic Latch

The Diagnostic Latch serves both for diagnostic uses and internal control uses. It is loaded from the DATA lines under the control of LE DIAG. Table XIV shows the loading definitions for the DATA lines.

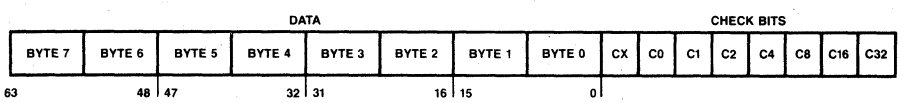
Diagnostic Generate
Diagnostic Detect
Diagnostic Correct

These are special diagnostic modes selected by DIAG $MODE_{0\text{-}1}$ where either normal check bit inputs or outputs are substituted for by check bits from the Diagnostic Latch. See Table II for details.

Internal Control Mode

This mode is selected by CODE $ID_{0\text{-}2}$, input 001 (ID_2, ID_1, ID_0).

When in Internal Control Mode the EDC takes the CODE $ID_{0\text{-}2}$, DIAG $MODE_{0\text{-}1}$, CORRECT and PASS THRU signals from the internal Diagnostic Latch rather than from the external control lines. Table XIV gives format for loading the Diagnostic Latch.



Uses Modified Hamming Code 64/72
- 64 data bits
- 8 check bits
- 72 bits in total

Figure 9. 64-Bit Data Format

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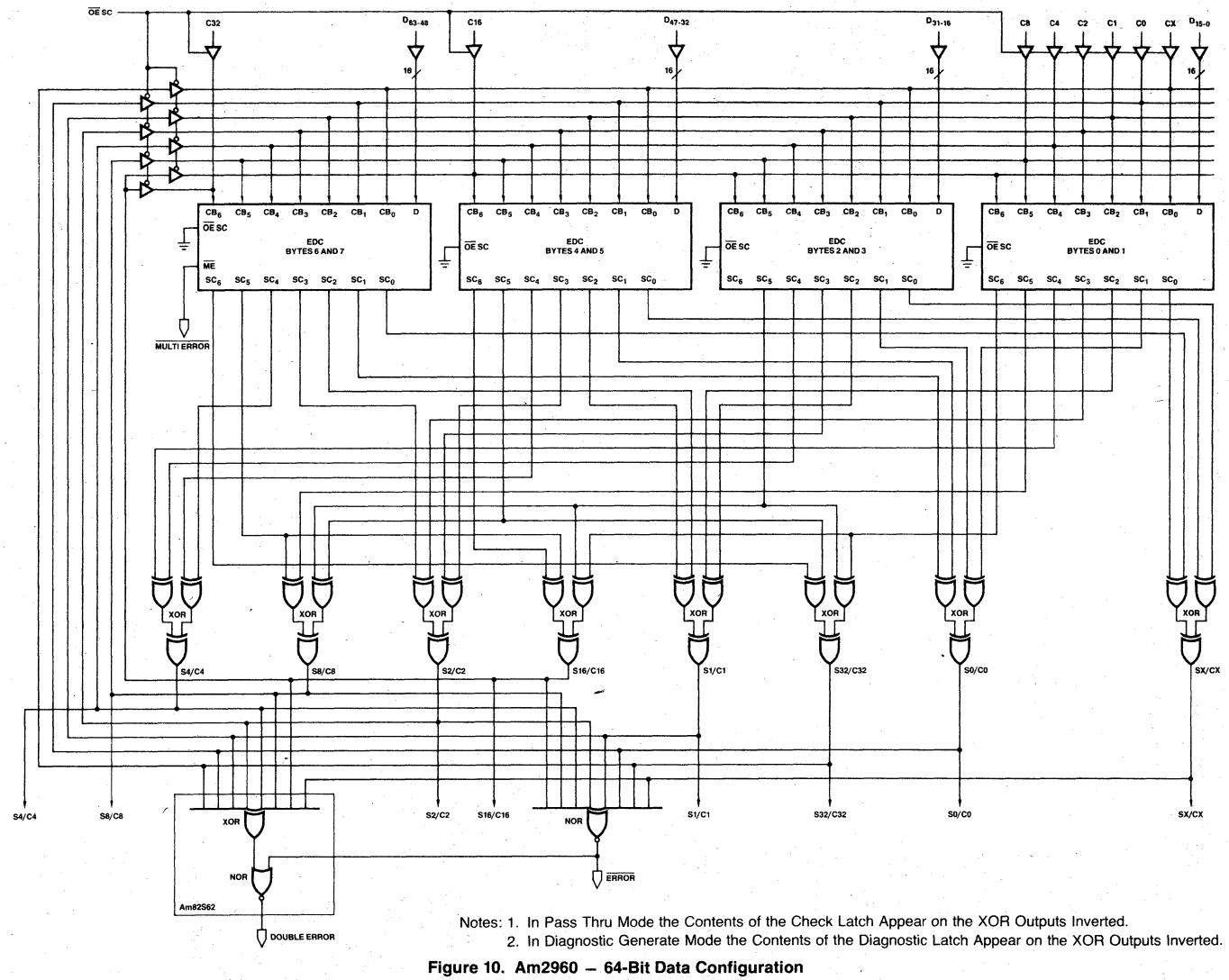


Notes: 1. In Pass Thru Mode the Contents of the Check Latch Appear on the XOR Outputs Inverted.
2. In Diagnostic Generate Mode the Contents of the Diagnostic Latch Appear on the XOR Outputs Inverted.

Figure 10. Am2960 – 64-Bit Data Configuration

TABLE XI. KEY AC CALCULATIONS FOR THE 64-BIT CONFIGURATION

64-Bit Propagation Delay		Component Delays from Am2960 AC Specifications, Table C (plus MSI)
From	To	
DATA	Check Bits Out	(DATA to SC) + (XOR Delay)
DATA In	Corrected DATA Out	(DATA to SC) + (XOR Delay) + (Buffer Delay) + (CB to DATA, CODE ID 1xx)
DATA	Syndromes	(DATA to SC) + (XOR Delay)
DATA	$\overline{\text{ERROR}}$ for 64 Bits	(DATA to SC) + (XOR Delay) + (NOR Delay)
DATA	$\overline{\text{MULT ERROR}}$ for 64 Bits	(DATA to SC) + (XOR Delay) + (Buffer Delay) + (CB to $\overline{\text{MULT ERROR}}$, CODE ID 1xx)
DATA	DOUBLE ERROR for 64 Bits	(DATA to SC) + (XOR Delay) + (XOR/NOR Delay)

4

TABLE XII. 64-BIT MODIFIED HAMMING CODE – CHECK BIT ENCODE

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								
C32	Even (XOR)	X	X	X	X	X	X	X	X								

Generated Check Bits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X
C32	Even (XOR)									X	X	X	X	X	X	X	X

Generated Check Bits	Parity	Participating Data Bits															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
CX	Even (XOR)	X				X		X	X			X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								
C32	Even (XOR)									X	X	X	X	X	X	X	X

Generated Check Bits	Parity	Participating Data Bits															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CX	Even (XOR)	X				X		X	X			X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X
C32	Even (XOR)	X	X	X	X	X	X	X	X								

The check bit is generated as either an XOR or XNOR of the 32 data bits noted by an "X" in the table.

TABLE XIII. SYNDROME DECODE TO BIT-IN-ERROR.

Syndrome Bits																			
				S32	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
				S16	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
				S8	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
				S4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
SX	S0	S1	S2																	
0	0	0	0		*	C32	C16	T	C8	T	T	M	C4	T	T	M	T	46	62	T
0	0	0	1		C2	T	T	M	T	43	59	T	T	53	37	T	M	T	T	M
0	0	1	0		C1	T	T	M	T	41	57	T	T	51	35	T	15	T	T	31
0	0	1	1		T	M	M	T	13	T	T	29	23	T	T	7	T	M	M	T
0	1	0	0		C0	T	T	M	T	40	56	T	T	50	34	T	M	T	T	M
0	1	0	1		T	49	33	T	12	T	T	28	22	T	T	6	T	M	M	T
0	1	1	0		T	M	M	T	10	T	T	26	20	T	T	4	T	M	M	T
0	1	1	1		16	T	T	0	T	M	M	T	T	M	M	T	M	T	T	M
1	0	0	0		CX	T	T	M	T	M	M	T	T	M	M	T	14	T	T	30
1	0	0	1		T	M	M	T	11	T	T	27	21	T	T	5	T	M	M	T
1	0	1	0		T	M	M	T	9	T	T	25	19	T	T	3	T	47	63	T
1	0	1	1		M	T	T	M	T	45	61	T	T	55	39	T	M	T	T	M
1	1	0	0		T	M	M	T	8	T	T	24	18	T	T	2	T	M	M	T
1	1	0	1		17	T	T	1	T	44	60	T	T	54	38	T	M	T	T	M
1	1	1	0		M	T	T	M	T	42	58	T	T	52	36	T	M	T	T	M
1	1	1	1		T	48	32	T	M	T	T	M	M	T	T	M	T	M	M	T

* – no errors detected
Number – the number of the single bit-in-error
T – two errors detected
M – more than two errors detected

TABLE XIV. DIAGNOSTIC LATCH LOADING – 64-BIT FORMAT.

Data Bit	Internal Function
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6, 7	Don't Care
8	Slice 0/1 – CODE ID 0
9	Slice 0/1 – CODE ID 1
10	Slice 0/1 – CODE ID 2
11	Slice 0/1 – DIAG MODE 0
12	Slice 0/1 – DIAG MODE 1
13	Slice 0/1 – CORRECT
14	Slice 0/1 – PASS THRU
15	Don't Care
16-23	Don't Care
24	Slice 2/3 – CODE ID 0
25	Slice 2/3 – CODE ID 1
26	Slice 2/3 – CODE ID 2
27	Slice 2/3 – DIAG MODE 0
28	Slice 2/3 – DIAG MODE 1
29	Slice 2/3 – CORRECT
30	Slice 2/3 – PASS THRU

Data Bit	Internal Function
31	Don't Care
32-37	Don't Care
38	Diagnostic Check Bit 16
39	Don't Care
40	Slice 4/5 – CODE ID 0
41	Slice 4/5 – CODE ID 1
42	Slice 4/5 – CODE ID 2
43	Slice 4/5 – DIAG MODE 0
44	Slice 4/5 – DIAG MODE 1
45	Slice 4/5 – CORRECT
46	Slice 4/5 – PASS THRU
47	Don't Care
48-54	Don't Care
55	Diagnostic Check Bit 32
56	Slice 6/7 – CODE ID 0
57	Slice 6/7 – CODE ID 1
58	Slice 6/7 – CODE ID 2
59	Slice 6/7 – DIAG MODE 0
60	Slice 6/7 – DIAG MODE 1
61	Slice 6/7 – CORRECT
62	Slice 6/7 – PASS THRU
63	Don't Care

MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Case) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for high Output State	−0.5V to V_{CC} max.
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0 mA

OPERATING RANGE

P/N	Range	Temperature	V_{CC}	
Am2960DC, XC	COM'L	T_A = 0 to +70°C	V_{CC} = 5.0V ±5%	(MIN = 4.75V, MAX = 5.25V)
Am2960DM, FM, XM	MIL	T_C = −55 to +125°C	V_{CC} = 5.0V ± 10%	(MIN = 4.50V, MAX = 5.50V)

DC CHARACTERISTICS

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −0.8mA	COM'L	2.7			Volts
				MIL	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8mA				0.5	Volts
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 7)			2.0			Volts
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 7)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V	$DATA_{0-15}$				−410	μA
			All Other Inputs				−360	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	$DATA_{0-15}$				70	μA
			All Other Inputs				50	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} MAX	$DATA_{0-15}$	V_O = 2.4			70	μA
				V_O = 0.5			−410	
			SC_{0-6}	V_O = 2.4			50	
				V_O = 0.5			−50	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = V_{CC} MAX +0.5V, V_O = 0.5V			−25		−85	mA
I_{CC}	Power Supply Current (Note 6)	V_{CC} = MAX	COM'L	T_A = 25°C		275	390	mA
				T_A = 0 to +70°C			400	
				T_A = +70°C			365	
			MIL	T_C = −55 to +125°C			400	
				T_C = +125°C			345	

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These are three-state outputs internally connected to TTL inputs. Input Characteristics are measured with output enables HIGH.
5. "MIL" = Am2960XM, DM, FM. "COM'L" = Am2960XC, DC.
6. Worst case I_{CC} is at minimum temperature.
7. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the complexity and power levels of the part. The following notes may be useful.

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5-8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100's of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \leq 2.4V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

1. Am2960 Guaranteed Commercial Range Performance

The tables below specify the guaranteed performance of the Am2960 over the commercial operating range of 0 to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2960DC, XC.

A. Combinational Propagation Delays
C_L = 50pF

From Input \ To Output	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	32	65*	32	50
CB_{0-6} (CODE ID_{2-0} 000, 011)	28	56	29	47
CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)	28	45	29	34
$\overline{GENERATE}$	35	63	36	55
CORRECT (Not Internal Control Mode)	–	45	–	–
DIAG MODE (Not Internal Control Mode)	50	78	59	75
PASS THRU (Not Internal Control Mode)	36	44	29	46
CODE ID_{2-0}	61	90	60	80
LE IN (From latched to transparent)	39	72*	39	59
LE OUT (From latched to transparent)	–	31	–	–
LE DIAG (From latched to transparent; Not Internal Control Mode)	45	78	45	65
Internal Control Mode: LE DIAG (From latched to transparent)	67	96	66	86
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	67	96	66	86

*Data In (or LE In) to Correct Data Out measurement requires timing as shown in Figure D opposite.

B. Set-up and Hold Times Relative to Latch Enables

From Input	To (Latching Up Data)	Set-up Time	Hold Time
$DATA_{0-15}$	LE IN	6	7
CB_{0-6}	LE IN	5	6
$DATA_{0-15}$	LE OUT	44	5
CB_{0-6} (CODE ID 000, 011)	LE OUT	35	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111)	LE OUT	27	0
$\overline{GENERATE}$	LE OUT	42	0
CORRECT	LE OUT	26	1
DIAG MODE	LE OUT	69	0
PASS THRU	LE OUT	26	0
CODE ID_{2-0}	LE OUT	81	0
LE IN	LE OUT	51	5
$DATA_{0-15}$	LE DIAG	6	8

C. Output Enable/Disable Times

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$ BYTE 0, $\overline{OE}$ BYTE 1	$DATA_{0-15}$	30	30
$\overline{OE}$ SC	SC_{0-6}	30	30

D. Minimum Pulse Widths

LE IN, LE OUT, LE DIAG	15

4

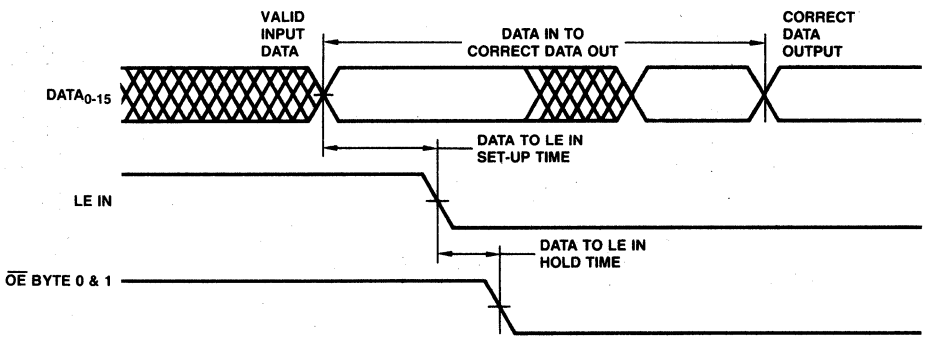


Figure D.

1. Am2960 Guaranteed Military Range Performance

The tables below specify the guaranteed performance of the Am2960 over the military operating range of −55 to +125°C case temperature, with V_{CC} from 4.5V to 5.5V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2960DM, FM, XM.

A. Combinational Propagation Delays
C_L = 50pF

From Input \ To Output	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	35	73*	36	56
CB_{0-6} (CODE ID_{2-0} 000, 011)	30	61	31	50
CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)	30	50	31	37
$\overline{GENERATE}$	38	69	41	62
CORRECT (Not Internal Control Mode)	–	49	–	–
DIAG MODE (Not Internal Control Mode)	58	89	65	90
PASS THRU (Not Internal Control Mode)	39	51	34	54
CODE ID_{2-0}	69	100	68	90
LE IN (From latched to transparent)	44	82*	43	66
LE OUT (From latched to transparent)	–	33	–	–
LE DIAG (From latched to transparent; Not Internal Control Mode)	50	88	49	72
Internal Control Mode: LE DIAG (From latched to transparent)	75	106	74	96
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	75	106	74	96

*Data In (or LE In) to Correct Data Out measurement requires timing as shown in Figure D opposite.

B. Set-up and Hold Times Relative to Latch Enables

From Input	To (Latching Up Data)	Set-up Time	Hold Time
$DATA_{0-15}$	LE IN	7	7
CB_{0-6}	LE IN	5	7
$DATA_{0-15}$	LE OUT	50	5
CB_{0-6} (CODE ID 000, 011)	LE OUT	38	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111)	LE OUT	30	0
$\overline{GENERATE}$	LE OUT	46	0
CORRECT	LE OUT	28	1
DIAG MODE	LE OUT	84	0
PASS THRU	LE OUT	30	0
$CODE\ ID_{2-0}$	LE OUT	89	0
LE IN	LE OUT	59	5
$DATA_{0-15}$	LE DIAG	7	9

C. Output Enable/Disable Times

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$ BYTE 0, $\overline{OE}$ BYTE 1	$DATA_{0-15}$	35	35
$\overline{OE}$ SC	SC_{0-6}	35	35

D. Minimum Pulse Widths

LE IN, LE OUT, LE DIAG	15

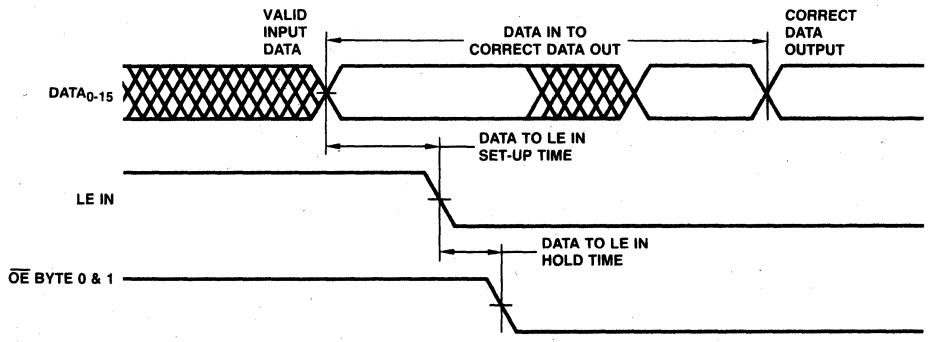


Figure D.

Am2960-1 Guaranteed Commercial Range Performance

The tables below specify the guaranteed performance of the Am2960-1 over the commercial operating range of 0 to +70°C, with V_{CC} from 4.75 to 5.25V. All data are in ns, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2960-1DC, XC.

A. Combinational Propagation Delays
C_L = 50pF

To Output / From Input	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$	28	52	25	50
CB_{0-6} (CODE ID_{2-0} 000, 011)	23	50	23	47
CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)	28	34	29	34 (100, 101, 110, 111)
$\overline{GENERATE}$	35	63	36	55
CORRECT (Not Internal Control Mode)	–	45	–	–
DIAG MODE (Not Internal Control Mode)	50	78	59	75
PASS THRU (Not Internal Control Mode)	36	44	29	46
CODE ID_{2-0}	61	90	60	80
LE IN (From latched to transparent)	39	72*	39	59
LE OUT (From latched to transparent)	–	31	–	–
LE DIAG (From latched to transparent; Not Internal Control Mode)	45	78	45	65
Internal Control Mode: LE DIAG (From latched to transparent)	67	96	66	86
Internal Code Mode: $DATA_{0-15}$ (Via Diagnostic Latch)	67	96	66	86

*Data In (or LE In) to Correct Data Out measurement requires timing as shown in Figure D opposite.

B. Set-up and Hold Times Relative to Latch Enables

From Input	To (Latching Up Data)	Set-up Time	Hold Time
$DATA_{0-15}$	LE IN	6	7
CB_{0-6}	LE IN	5	6
$DATA_{0-15}$	LE OUT	34	5
CB_{0-6} (CODE ID 000, 011)	LE OUT	35	0
CB_{0-6} (CODE ID 010, 100, 101, 110, 111)	LE OUT	27	0
$\overline{GENERATE}$	LE OUT	42	0
CORRECT	LE OUT	26	1
DIAG MODE	LE OUT	69	0
PASS THRU	LE OUT	26	0
CODE ID_{2-0}	LE OUT	81	0
LE IN	LE OUT	51	5
$DATA_{0-15}$	LE DIAG	6	8

C. Output Enable/Disable Times

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$ BYTE 0, $\overline{OE}$ BYTE 1	$DATA_{0-15}$	30	30
$\overline{OE}$ SC	SC_{0-6}	30	30

D. Minimum Pulse Widths

LE IN, LE OUT, LE DIAG	15

4

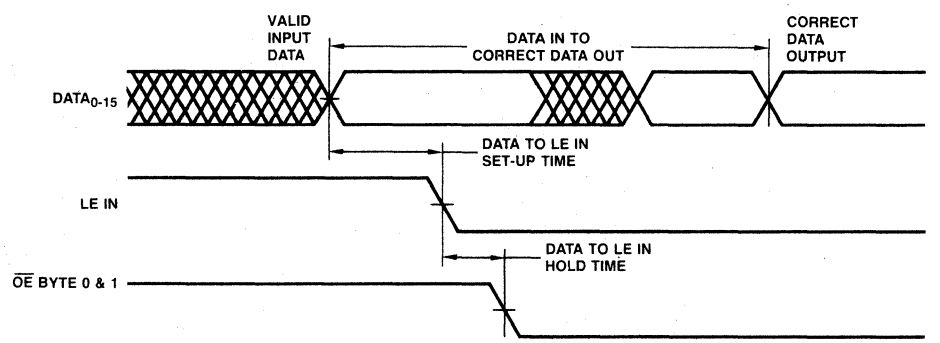


Figure D.

Am2960A Guaranteed Commercial Range Performance

The tables below specify the guaranteed performance of the Am2960A over the commercial operating range of 0 to +70°C, with V_{CC} from 4.75 to 5.25V. All data are in ns, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2960ADC, XC.

A. Combinational Propagation Delays
C_L = 50pF

From Input \ To Output	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$				
CB_{0-6} (CODE ID_{2-0} 000, 011)				
CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)				
$\overline{GENERATE}$				
CORRECT (Not Internal Control Mode)				
DIAG MODE (Not Internal Control Mode)				
PASS THRU (Not Internal Control Mode)				
CODE ID_{2-0}				
LE IN (From latched to transparent)				
LE OUT (From latched to transparent)				
LE DIAG (From latched to transparent; Not Internal Control Mode)				
Internal Control Mode: LE DIAG (From latched to transparent)				
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)				

*Data In (or LE In) to Correct Data Out measurement requires timing as shown in Figure D opposite.

B. Set-up and Hold Times Relative to Latch Enables

From Input	To (Latching Up Data)	Set-up Time	Hold Time
$DATA_{0-15}$	LE IN		
CB_{0-6}	LE IN		
$DATA_{0-15}$	LE OUT		
CB_{0-6} (CODE ID 000, 011)	LE OUT		
CB_{0-6} (CODE ID 010, 100, 101, 110, 111)	LE OUT		
$\overline{GENERATE}$	LE OUT		
CORRECT	LE OUT		
DIAG MODE	LE OUT		
PASS THRU	LE OUT		
$CODE\ ID_{2-0}$	LE OUT		
LE IN	LE OUT		
$DATA_{0-15}$	LE DIAG		

C. Output Enable/Disable Times

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$ BYTE 0, $\overline{OE}$ BYTE 1	$DATA_{0-15}$		
$\overline{OE}$ SC	SC_{0-6}		

D. Minimum Pulse Widths

LE IN, LE OUT, LE DIAG	

4

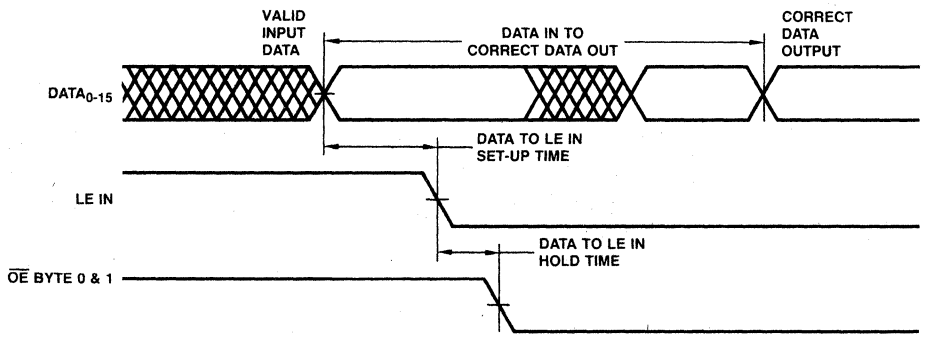


Figure D.

Am2960A Guaranteed Military Range Performance

The tables below specify the guaranteed performance of the Am2960A over the military operating range of −55 to +125°C case temperature, with V_{CC} from 4.5 to 5.5V. All data are in ns, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have the maximum DC load.

This data applies to the following part numbers: Am2960ADM, FM, XM.

A. Combinational Propagation Delays
C_L = 50pF

To Output / From Input	SC_{0-6}	$DATA_{0-15}$	$\overline{ERROR}$	$\overline{MULT\ ERROR}$
$DATA_{0-15}$				
CB_{0-6} (CODE ID_{2-0} 000, 011)				
CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)				
$\overline{GENERATE}$				
CORRECT (Not Internal Control Mode)				
DIAG MODE (Not Internal Control Mode)				
PASS THRU (Not Internal Control Mode)				
CODE ID_{2-0}				
LE IN (From latched to transparent)				
LE OUT (From latched to transparent)				
LE DIAG (From latched to transparent; Not Internal Control Mode)				
Internal Control Mode: LE DIAG (From latched to transparent)				
Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)				

*Data In (or LE In) to Correct Data Out measurement requires timing as shown in Figure D opposite.

B. Set-up and Hold Times Relative to Latch Enables

From Input	To (Latching Up Data)	Set-up Time	Hold Time
$DATA_{0-15}$	LE IN		
CB_{0-6}	LE IN		
$DATA_{0-15}$	LE OUT		
CB_{0-6} (CODE ID 000, 011)	LE OUT		
CB_{0-6} (CODE ID 010, 100, 101, 110, 111)	LE OUT		
$\overline{GENERATE}$	LE OUT		
CORRECT	LE OUT		
DIAG MODE	LE OUT		
PASS THRU	LE OUT		
$CODE\ ID_{2-0}$	LE OUT		
LE IN	LE OUT		
$DATA_{0-15}$	LE DIAG		

C. Output Enable/Disable Times

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$ BYTE 0, $\overline{OE}$ BYTE 1	$DATA_{0-15}$		
$\overline{OE}$ SC	SC_{0-6}		

D. Minimum Pulse Widths

LE IN, LE OUT, LE DIAG	

4

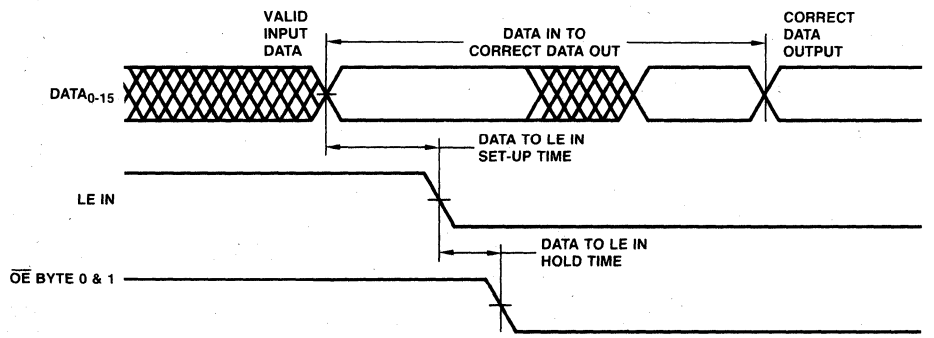
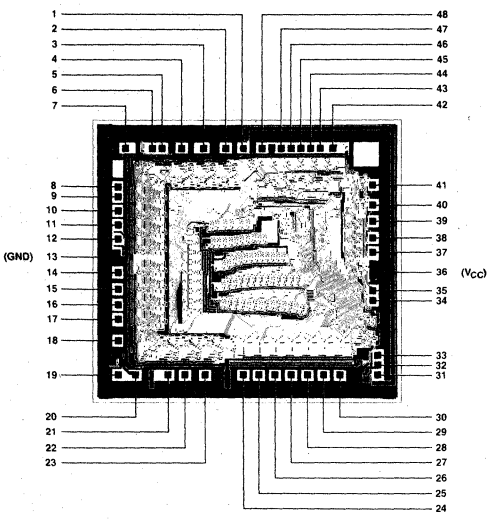


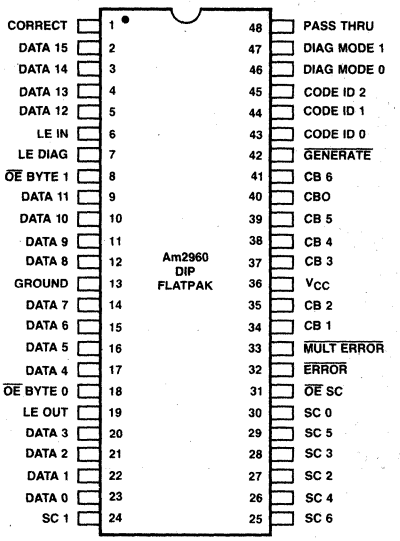
Figure D.

METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.200" X 0.183"

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2960 Order Number (Note 3)	Package Type Order Number	Operating Range (Note 1)	Screening Level (Note 2)
AM2960DC	D-48	C	C-1
AM2960DC-B	D-48	C	B-2 (Note 4)
AM2960DM	D-48	M	C-3
AM2960DM-B	D-48	M	B-3
AM2960FM	F-48	M	C-3
AM2960FM-B	F-48	M	B-3
AM2960XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2960XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to +70°C, V_{CC} = 4.75V to 5.25V, M = −55 to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

TEST OUTPUT LOAD CONFIGURATION FOR Am2960

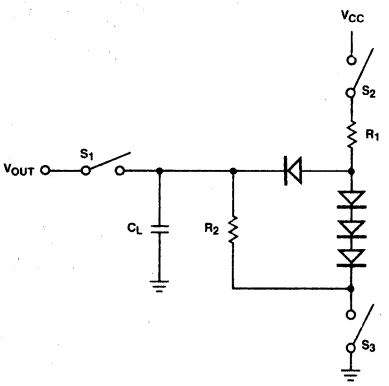


Figure 11. Three-State Outputs

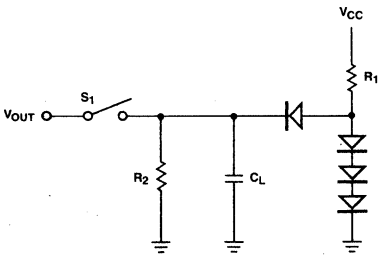


Figure 12. Normal Outputs

Notes:
1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function test and all A.C. tests, except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
   S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. R_2 = 1K for three-state output.
   R_2 is determined by the I_{OH} at V_{OH} = 2.4V for non-three-state outputs.
5. R_1 is determined by I_{OL} (MIL) with V_{CC} = 5.0V minus the current to ground through R_2.
6. C_L = 5.0 pF for output disable tests.

TEST OUTPUT LOADS

Pin #	Pin Label	Test Circuit	R_1	R_2
–	D_0-D_{15}	Fig. 11	430Ω	1kΩ
24-30	SC_0-SC_6	Fig. 11	430Ω	1kΩ
32	$\overline{\text{ERROR}}$	Fig. 12	470Ω	3kΩ
33	$\overline{\text{MULTERROR}}$	Fig. 12	470Ω	3kΩ

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

APPLICATIONS

Byte Write

Byte operations are increasingly common for 16 and 32-bit processors. These complicate memory operations because check bits are generated for a complete 16 or 32 or 64-bit memory word, not for a single byte.

To write a byte into memory with EDC requires the following steps:

- Latch the byte into the Am2961/62 bus buffers (Figure 13)
- Read the complete data word from memory (Figure 13)
- Correct the complete data word if necessary (Figure 13)
- Insert the byte to be written into the data word (Figure 14)
- Generate new check bits for the entire data word (Figure 14)
- Store the data word back into memory (Figure 14)

(In fact these steps must be taken for any piece of data being written into memory that is not as wide as a full memory word).

The Am2960 EDC is designed with the intent of keeping byte operations simple in EDC systems. The EDC has separate output enables for each byte in the Data Output Latch. As shown in figures 13 and 14, this allows the data word to be read from memory, the new byte to be inserted among the old, and new check bits to be generated using less time and less hardware than if separate byte enables were not available.

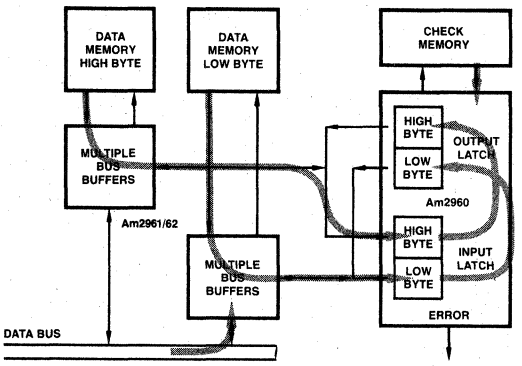


Figure 13. Byte Write, Phase 1: Read Out the Old Word and Correct

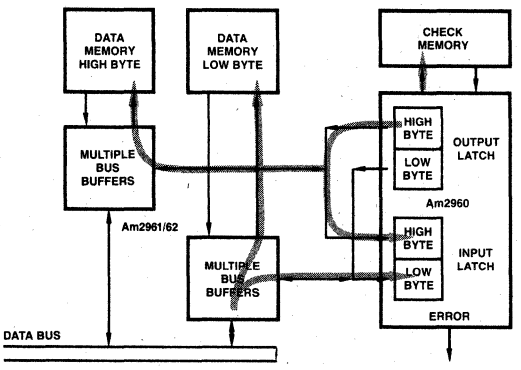


Figure 14. Byte Write, Phase 2: Insert the New Byte, Generate Checks and Write Into Memory

Diagnostics

EDC is used to boost the reliability of the overall system. It is necessary to also be able to check the operation of the EDC itself. For this reason the EDC has an internal control mode, a diagnostic latch, and two diagnostic modes.

To check that the EDC is functioning properly, the processor can put the EDC under software control by setting CODE ID_{2-0} to 001. This puts the EDC into Internal Control Mode. In Internal Control Mode the EDC is controlled by the contents of the Diagnostic Latch which is loaded from the DATA inputs under processor control.

The EDC is set into CORRECT Mode. The processor loads in a known set of check bits into the Diagnostic Latch, a known set of data bits into the Data In Latch, and forces data errors. The output of the EDC (syndromes, error flags, corrected data) is then compared against the expected responses. By exercising the EDC with a string of data/check combinations and comparing the output against the expected responses, the EDC can be fully checked out.

Eight Bit Data Word

Eight bit MOS microprocessors can use EDC too. Only five check bits are required. The EDC configuration for eight bits is shown in Figure 15. It operates as does the normal 16-bit configuration with the upper byte fixed at 0.

Check bit overhead for 8-bit data words can be reduced two ways. See the sections "Single Error Correction Only" and "Reducing Check Bit Overhead."

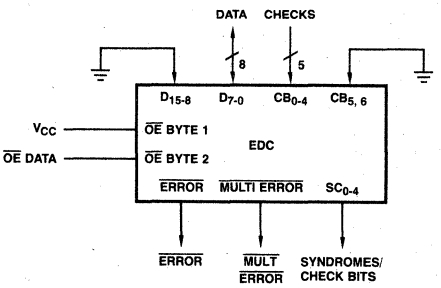


Figure 15. 8-Bit Configuration

Other Word Widths

EDC on data words other than 8, 16, 32, of 64 bits can be accomplished with the Am2960. In most cases the extra data bits can be forced to a constant, and EDC will procede as normal. For example a 24-bit data word is shown in Figure 16.

Single Error Correction Only

The EDC normally corrects all single bit errors *and* detects all double bit and some triple bit errors. To save one check bit per word the ability to detect double bit errors can be sacrificed – single errors are still detected and corrected.

Data Bits	Check Bits Required	
	Single Error Correction Only	Single Error Correct & Double Error Detect
8	4	5
16	5	6
32	6	7
64	7	8

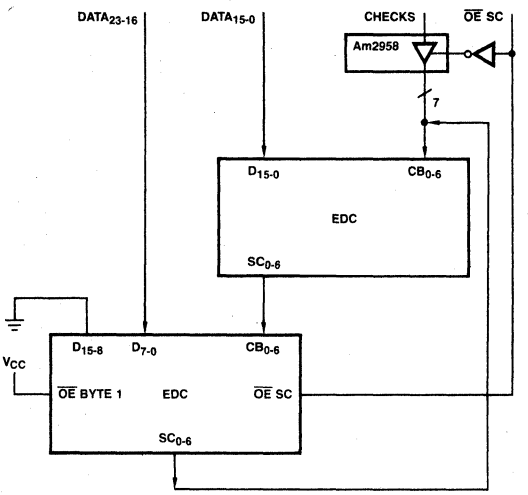


Figure 16. 24-Bit Configuration

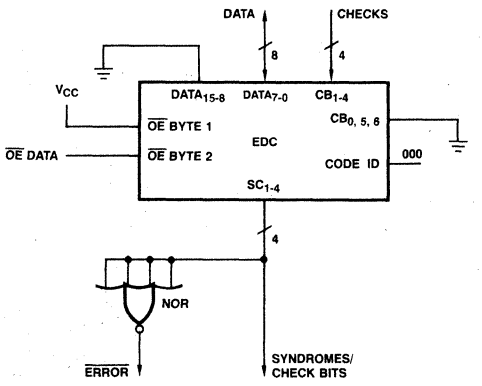


Figure 17. 8-Bit Single Error Correction Only

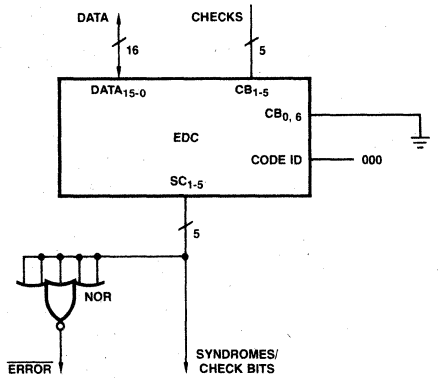
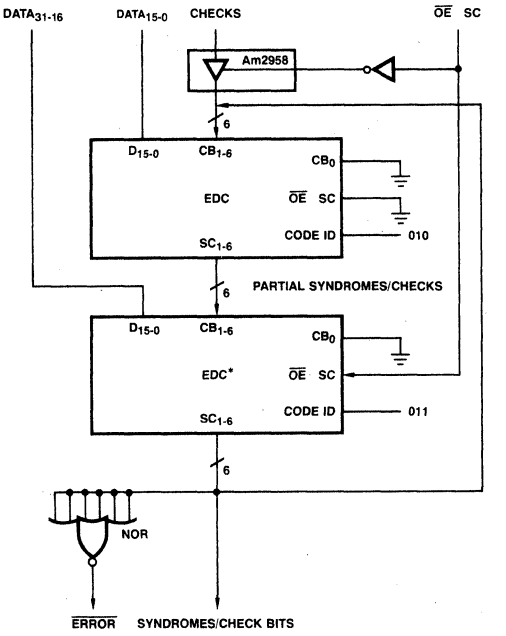


Figure 18. 16-Bit Single Error Correction Only



*The Code ID Combination for this Slice Forces the Check Bit Latch Transparent.

Figure 19. 32-Bit Single Correct Only

Figures 17, 18, 19, 20 show single error correction only configurations for 8, 16, 32, and 64-bit data words respectively.

Check Bit Correction

The EDC detects single bit errors whether the error is a data bit or a check bit. Data bit errors are automatically corrected by the EDC. To generate corrected check bits once a single check bit error is detected, the EDC need only be switched to GENERATE mode (data in the DATA INPUT LATCH is valid).

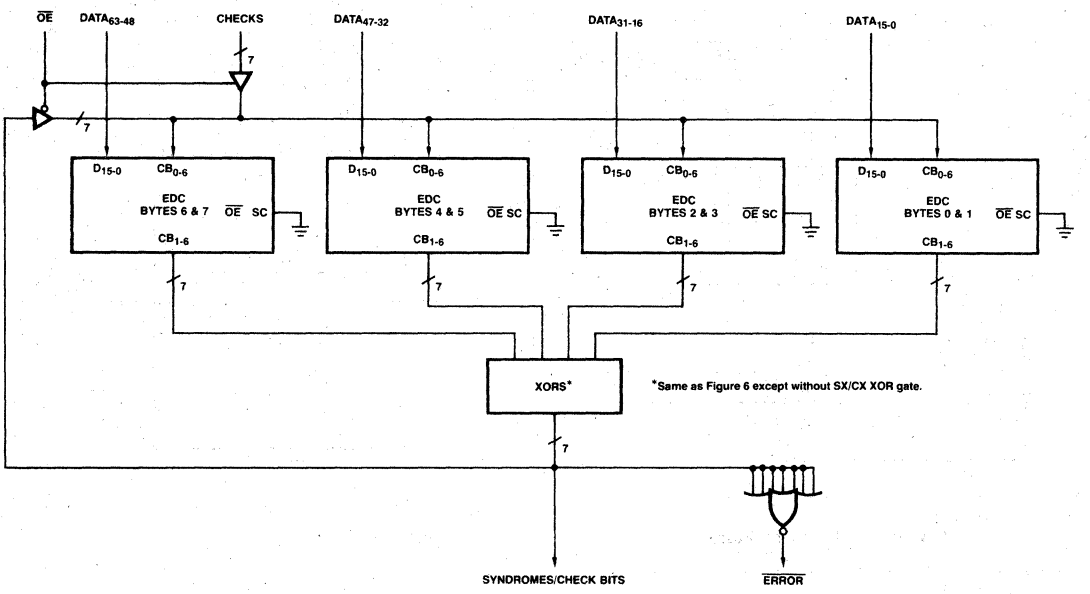
The syndromes generated by the EDC may be decoded to determine whether the single bit error is a check bit.

In many memory systems, a check bit error will be ignored on the memory read and corrected during a periodic "scrubbing" of memory (see section in System Design Considerations).

Multiple Errors

The bit-in-error decode logic uses syndrome bits S0 through S32 to correct errors, SX is only used in developing the multiple error signal. This means that some multiple errors will cause a data bit to be inverted.

For example, in the 16-bit mode if data bits 8 and 13 are in error the syndrome 111100 (SX, S0, S1, S2, S4, S8) is produced. This is flagged a double error by the error detection logic, but the bit-in-error decoder only receives syndrome 11100 (S0, S1, S2, S4, S8) which it decodes as a single error in data bit 0 and inverts that bit. If it is desired to inhibit this inversion, the multiple error output may be connected to the correct input as in Figure 21. This will inhibit correction when a multiple error occurs. Extra time delay may be introduced in the data to correct data path when this is done.



Notes: 1. In Pass Thru Mode the Contents of the Check Latch Appear on the XOR Outputs Inverted.
2. In Diagnostic Generate Mode the Contents of the Diagnostic Latch appear on the XOR Outputs Inverted.

Figure 20. 64-Bit Single Correct Only

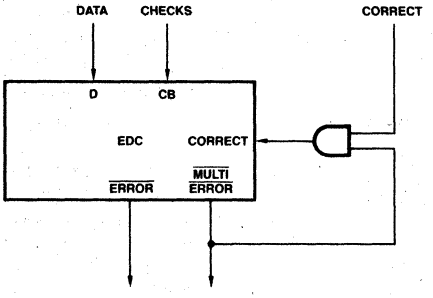


Figure 21. Inhibition of Data Modification

SYSTEM DESIGN CONSIDERATIONS

High Performance Parallel Operation

For maximum memory system performance the EDC should be used in the Check-Only configuration shown in Figure 22. With this configuration the memory system operates as fast with EDC as it would without.

On reads from memory, data is read out from the RAMs directly to the data bus (same as in a non-EDC system). At the same time, the data is read into the EDC to check for errors. If an error exists the EDC's error flags are used to interrupt the CPU and/or to stretch the memory cycle. If no error is detected, no slowdown is required.

If an error is detected, the EDC generates corrected data for the processor. At the designer's option the correct data may be written back into memory; error logging and diagnostic routines may also be run under processor control.

The Check-Only configuration allows data reads to proceed as fast with EDC as without. Only if an error is detected is there any slowdown. But even if the memory system had an error every hour this would mean only one error every 3-4 *billion* memory cycles. So even with a very high error rate, EDC in a Check-Only configuration has essentially zero impact on memory system speed.

On writes to memory, check bits must be generated before the full memory word can be written into memory. But using the Am2961/62 Data Bus Buffers allows the data word to be buffered on the memory board while check bits are generated. This makes the check bit generate time transparent to the processor.

EDC in the Data Path

The simplest configuration for EDC is to have the EDC directly in the data path as shown in Figure 23 (Correct-Always Configuration). In this configuration data read from memory is always corrected prior to putting the data on the data bus. The advantages are simpler operation and no need for mid-cycle interrupts. The disadvantage is that memory system speed is slowed by the amount of time it takes for error correction on ever cycle.

Usually the Correct-Always Configuration will be used with MOS microprocessors which have ample memory timing budgets. Most high performance processors will use the high performance parallel configuration shown in Figure 22. (Check-Only Configuration).

Scrubbing Avoids Double Errors

Single-bit errors are by far the most common in a memory system and are always correctable by the EDC.

Double bit memory errors are far less frequent than single bit (50 to 1, or 100 to 1) and are always detected by the EDC but not corrected.

In a memory system, soft errors occur only one at a time. A double bit error in a data word occurs when a single soft error is left uncorrected and is followed by another error in the data word hours, days, or weeks after the first.

"Scrubbing" memory periodically avoids almost all double-bit errors. In the scrubbing operation, every data word in memory is periodically checked by the EDC for single-bit errors. If one is found, it is corrected and the data word written back into memory. Errors are not allowed to pile up, and most double-bit errors are avoided.

The scrubbing operation is generally done as a background routine when the memory is not being used by the processor. If memory is scrubbed frequently, errors that are detected and corrected during processor accesses need not be immediately written back into memory. Instead the error will be corrected in memory during scrubbing. This reduces the time delay involved in a processor access of an incorrect memory word.

Correction of Double-Bit Errors

In some cases, double-bit memory errors can be corrected! This is possible when one of the two bit errors is a hard error.

When a double bit error is detected the data word should be checked to determine if one of the errors is a hard error. If so the

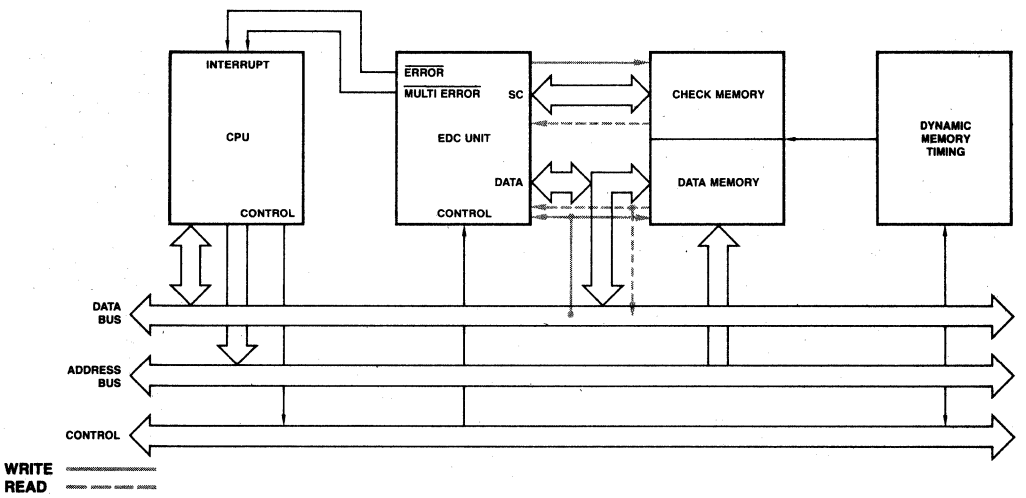


Figure 22. Check-Only Configuration

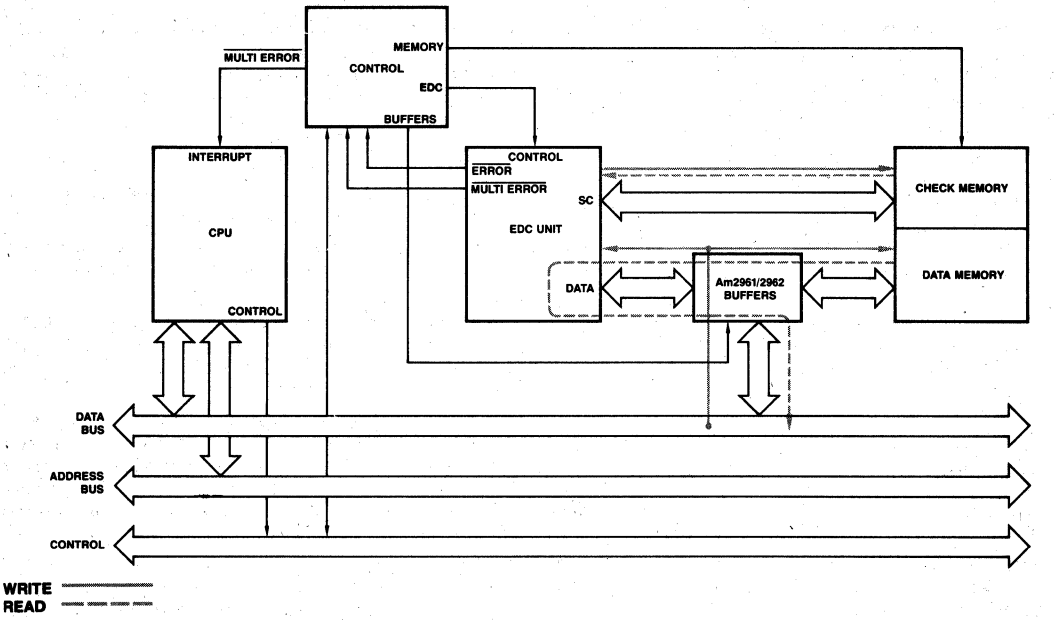


Figure 23. Correct-Always Configuration

hard error bit may be corrected by inverting it leaving only a single, correctable error. The time for this operation is negligible since it will occur infrequently.

The procedure after detection of a double error is as follows:

- Invert the data bits read from memory.
- Write the inverted data back into the same memory word.
- Re-read the memory location and XOR the newly read out value with the old. If there is no hard error then the XOR result will be all 1's. If there is a hard error, it will have the same bit value regardless of what was written in. So it will show as a 0 after the XOR operation
- Invert the hard error bit (this will "correct" it) leaving only one error in the data.
- The EDC can then correct the single bit error.
- Rewrite the correct data word into memory. This does not change the hard error but does eliminate the soft error. So the next memory access will find only a single-bit, correctable error.

An example helps to illustrate the procedure:

Example of Double Bit Error Correction When One is a Hard Error

1) Data Read from Memory (D_1)	1111111100000011	011010
2) EDC detects a multiple error. Syndromes:		011000
3) Syndrome decode indicates a double bit error.		
4) Invert the bits read from memory (D_1)	0000000011111100	100101
5) Write D_1 back to the same memory location		
6) Read back the memory location (D_2)	0000000011111101	100101
7) XOR D_1 and D_2	1111111111111110	111111
8) So the last data bit is the hard error. Use this to modify D_1	1111111100000010	011010
9) Pass the modified D_1 through the EDC. The EDC detects a single bit correctable error and outputs corrected data:	1111111100000000	011010
10) Write the corrected data back to memory to fix the soft error.		

Error Logging and Preventative Maintenance

The effectiveness of preventative maintenance can be increased by logging information on errors detected by the EDC. This is called error logging.

The EDC provides syndromes when errors are detected. The syndromes indicate which bit is in error. In most memory systems, each individual RAM supplies only one bit of the memory word. So the syndrome and data word address specify which RAM was in error.

Typically a permanent/hard RAM failure is preceded by a period of time where the RAM displays an increasing frequency of intermittent, soft errors. Error logging statistic can be used to detect an increasing intermittent error frequency so that the RAM can be replaced before a permanent failure occurs.

Error logging also records the location of already hard failed RAMs. With EDC a hard failure will not halt system operation. EDC always can correct single bit errors even if it is a hard error. EDC can also correct double bit errors where one is hard and one soft (see "Correction of Double Bit Errors" Section). The ability to continue operation despite hard errors can greatly reduce the need for emergency field maintenance. The hard-failed RAMs can be instead replaced at low cost during a regularly scheduled preventative maintenance session.

Reducing Check Bit Overhead

Memory word widths need not be the same as the data word width of the processor. There is a substantial reduction in check bit overhead if wider memory words are used:

Memory Word		Check Bit Overhead
# Data Bits	# Check Bits	
8	5	38%
16	6	27%
32	7	14%
64	8	11%

This reduction in check bit overhead lowers cost and increases the amount of data that can be packed on to each board.

The trade off is that when writing data pieces into memory that are narrower than the memory word width, more steps are required. These steps are exactly the same as those described in Byte Write in the Applications section. No penalty exists for reads from memory.

EDC Per Board vs EDC Per System

The choice of an EDC per system or per board depends on the economics and the architecture of the system.

Certainly the cheaper approach is to have only one EDC per system and this is a viable solution if only one memory location is accessed at at time.

This solution does require that the system has both data and check bit lines (see Figure 25). This makes retrofitting a system difficult and creates complications if static or ROM memory, which do not require check bits, are mixed in with dynamic RAM.

If the system has an advanced architecture it is quite likely that it is necessary to simultaneously access memory locations on different memory boards (see Figure 24). Architectural features that require this are interleaved memory, cache memory, and DMA that is done simultaneously with processor memory accesses. EDC per board is a simpler system from a design standpoint.

The EDC is designed to work efficiently in either the per system or per board configurations.

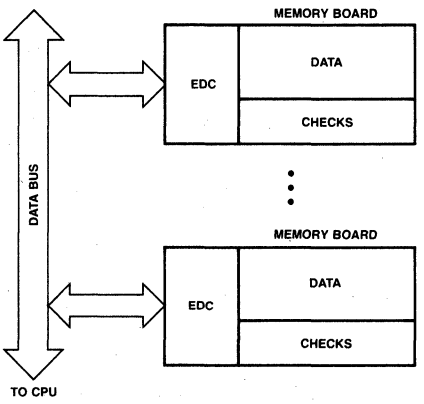


Figure 24. EDC Per Board

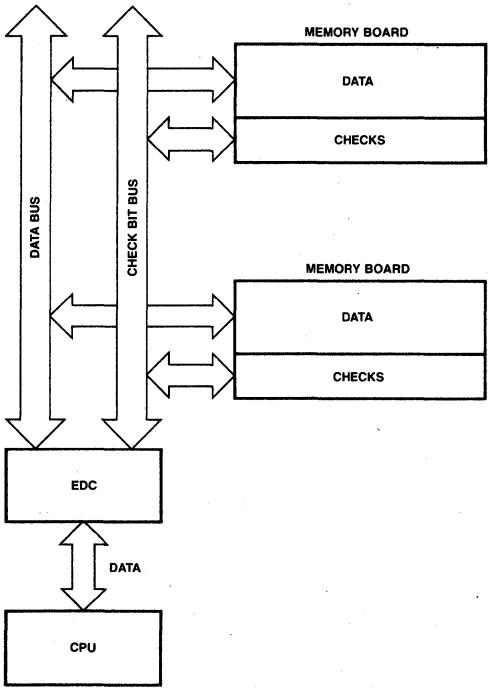


Figure 25. EDC Per System

FUNCTIONAL EQUATIONS

The following equations and tables describe in detail how the output values of the Am2960 EDC are determined as a function of the value of the inputs and the internal states. Be sure to carefully read the following definitions of symbols before examining the tables.

Definitions

D_i ← ($DATA_i$ if LE IN is HIGH or the output of bit i of the Data Input Latch if LE IN is LOW)
C_i ← (CB_i if LE IN is HIGH or the output of bit i of the Check Bit Latch if LE IN is LOW)
DL_i ← Output of bit i of the Diagnostic Latch
S_i ← Internally generated syndromes (same as outputs of SC_i if outputs enabled)
PA ← D0 ⊕ D1 ⊕ D2 ⊕ D4 ⊕ D6 ⊕ D8 ⊕ D10 ⊕ D12
PB ← D0 ⊕ D1 ⊕ D2 ⊕ D3 ⊕ D4 ⊕ D5 ⊕ D6 ⊕ D7
PC ← D8 ⊕ D9 ⊕ D10 ⊕ D11 ⊕ D12 ⊕ D13 ⊕ D14 ⊕ D15
PD ← D0 ⊕ D3 ⊕ D4 ⊕ D7 ⊕ D9 ⊕ D10 ⊕ D13 ⊕ D15
PE ← D0 ⊕ D1 ⊕ D5 ⊕ D6 ⊕ D7 ⊕ D11 ⊕ D12 ⊕ D13
PF ← D2 ⊕ D3 ⊕ D4 ⊕ D5 ⊕ D6 ⊕ D7 ⊕ D14 ⊕ D15
PG_1 ← D0 ⊕ D4 ⊕ D6 ⊕ D7
PG_2 ← D1 ⊕ D2 ⊕ D3 ⊕ D5
PG_3 ← D8 ⊕ D9 ⊕ D11 ⊕ D14
PG_4 ← D10 ⊕ D12 ⊕ D13 ⊕ D15

Error Signals

$$\overline{\text{ERROR}} \leftarrow \overline{(S6 \bullet (ID_1 + ID_2))} \bullet \overline{S5} \bullet \overline{S4} \bullet \overline{S3} \bullet \overline{S2} \bullet \overline{S1} \bullet \overline{S0} + \text{GENERATE} + \text{INITIALIZE} + \text{PASSTHRU}$$

$$\overline{\text{MULT ERROR}} \text{ (16 and 32-Bit Modes)} \leftarrow \overline{((\overline{S6 \bullet ID_1}) \oplus S5 \oplus S4 \oplus S3 \oplus S2 \oplus S1 \oplus S0)\,(\overline{\text{ERROR}})} + \text{TOME} + \text{GENERATE} + \text{PASSTHRU} + \text{INITIALIZE}$$

$$\overline{\text{MULT ERROR}} \text{ (64-Bit Modes)} \leftarrow \text{TOME} + \text{GENERATE} + \text{PASSTHRU} + \text{INITIALIZE}$$

TOME (Three or More Errors)*

S1	S2	S3 \ S0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
		**S6	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
		**S5	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
		**S4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
0	0	0	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0	0
0	0	1	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
0	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
1	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
1	1	0	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
1	1	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

*S6, S5, . . . S0 are internal syndromes except in Modes 010, 100, 101, 110, 111 (CODE ID_2, ID_1, ID_0). In these modes the syndromes are input over the Check-Bit lines. S6 ← C6, S5 ← C5, . . . S1 ← C1, S0 ← C0.

**The S6 internal syndrome is always forced to 0 in CODE ID 000.

SC Outputs

Tables XV, XVI, XVII, XVIII, XIX show how outputs SC_{0-6} are generated in each control mode for various CODE IDs (internal control mode not applicable).

TABLE XV.

GENERATE Mode (Check Bits) \ CODE ID_{2-0}	000	010	011	100	101	110	111
$SC_0 \leftarrow$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_3$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
$SC_1 \leftarrow$	PA	PA	$PA \oplus CB_1$	PA	PA	PA	PA
$SC_2 \leftarrow$	$\overline{PD}$	$\overline{PD}$	$PD \oplus CB_2$	$\overline{PD}$	PD	PD	PD
$SC_3 \leftarrow$	$\overline{PE}$	$\overline{PE}$	$PE \oplus CB_3$	$\overline{PE}$	PE	PE	PE
$SC_4 \leftarrow$	PF	PF	$PF \oplus CB_4$	PF	PF	PF	PF
$SC_5 \leftarrow$	PC	PC	$PC \oplus CB_5$	PC	PC	PC	PC
$SC_6 \leftarrow$	1	PB	$PC \oplus CB_6$	PB	PB	PB	PB

TABLE XVI.

Detect and Correct Modes (Syndromes) \ CODE ID_{2-0}	000	010	011*	100	101	110	111
$SC_0 \leftarrow$	$PG_2 \oplus PG_3 \oplus C0$	$PG_1 \oplus PG_3 \oplus C0$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3 \oplus C0$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
$SC_1 \leftarrow$	$PA \oplus C1$	$PA \oplus C1$	$PA \oplus CB_1$	$PA \oplus C1$	PA	PA	PA
$SC_2 \leftarrow$	$\overline{PD} \oplus C2$	$\overline{PD} \oplus C2$	$PD \oplus CB_2$	$\overline{PD} \oplus C2$	PD	PD	PD
$SC_3 \leftarrow$	$\overline{PE} \oplus C3$	$\overline{PE} \oplus C3$	$PE \oplus CB_3$	$\overline{PE} \oplus C3$	PE	PE	PE
$SC_4 \leftarrow$	$PF \oplus C4$	$PF \oplus C4$	$PF \oplus CB_4$	$PF \oplus C4$	PF	PF	PF
$SC_5 \leftarrow$	$PC \oplus C5$	$PC \oplus C5$	$PC \oplus CB_5$	$PC \oplus C5$	PC	PC	PC
$SC_6 \leftarrow$	1	$PB \oplus C6$	$PC \oplus CB_6$	PB	PB	$PB \oplus C6$	$PB \oplus C6$

*In CODE ID_{2-0} 011 the Check-Bit Latch is forced transparent, the Data Latch operates normally.

TABLE XVII.

Diagnostic Read Mode \ CODE ID_{2-0}	000	010	011*	100	101	110	111
$SC_0 \leftarrow$	$PG_2 \oplus PG_3 \oplus DL_0$	$PG_1 \oplus PG_3 \oplus DL_0$	$PG_2 \oplus PG_4 \oplus CB_0$	$PG_2 \oplus PG_3 \oplus DL_0$	$PG_2 \oplus PG_3$	$PG_1 \oplus PG_4$	$PG_1 \oplus PG_4$
$SC_1 \leftarrow$	$PA \oplus DL_1$	$PA \oplus DL_1$	$PA \oplus CB_1$	$PA \oplus DL_1$	PA	PA	PA
$SC_2 \leftarrow$	$\overline{PD} \oplus DL_2$	$\overline{PD} \oplus DL_2$	$PD \oplus CB_2$	$\overline{PD} \oplus DL_2$	PD	PD	PD
$SC_3 \leftarrow$	$\overline{PE} \oplus DL_3$	$\overline{PE} \oplus DL_3$	$PE \oplus CB_3$	$\overline{PE} \oplus DL_3$	PE	PE	PE
$SC_4 \leftarrow$	$PF \oplus DL_4$	$PF \oplus DL_4$	$PF \oplus CB_4$	$PF \oplus DL_4$	PF	PF	PF
$SC_5 \leftarrow$	$PC \oplus DL_5$	$PC \oplus DL_5$	$PC \oplus CB_5$	$PC \oplus DL_5$	PC	PC	PC
$SC_6 \leftarrow$	1	$PB \oplus DL_6$	$PC \oplus CB_6$	PB	PB	$PB \oplus DL_6$	$PB \oplus DL_7$

*In CODE ID_{2-0} 011 the Check-Bit Latch is forced transparent, the Data Latch operates normally.

TABLE XVIII.

CODE ID_{2-0} / Diagnostic Write Mode	000	010	011*	100	101	110	111
$SC_0 \leftarrow$	DL_0	DL_0	CB_0	DL_0	1	1	1
$SC_1 \leftarrow$	DL_1	DL_1	CB_1	DL_1	1	1	1
$SC_2 \leftarrow$	DL_2	DL_2	CB_2	DL_2	1	1	1
$SC_3 \leftarrow$	DL_3	DL_3	CB_3	DL_3	1	1	1
$SC_4 \leftarrow$	DL_4	DL_4	CB_4	DL_4	1	1	1
$SC_5 \leftarrow$	DL_5	DL_5	CB_5	DL_5	1	1	1
$SC_6 \leftarrow$	1	DL_6	CB_6	1	1	DL_6	DL_7

*In CODE ID_{2-0} 011 the Check-Bit Latch is forced transparent; the Data Input Latch operates normally.

TABLE XIX.

CODE ID_{2-0} / PASS THRU Mode	000	010	011*	100	101	110	111
$SC_0 \leftarrow$	C0	C0	CB_0	C0	1	1	1
$SC_1 \leftarrow$	C1	C1	CB_1	C1	1	1	1
$SC_2 \leftarrow$	C2	C2	CB_2	C2	1	1	1
$SC_3 \leftarrow$	C3	C3	CB_3	C_3	1	1	1
$SC_4 \leftarrow$	C4	C4	CB_4	C4	1	1	1
$SC_5 \leftarrow$	C5	C5	CB_5	C5	1	1	1
$SC_6 \leftarrow$	1	C6	CB_6	1	1	C6	C6

*In CODE ID_{2-0} 011 the Check-Bit Latch is forced transparent; the Data Input Latch operates normally.

Data Correction

Tables XX to XXVI shows which data output bits are corrected (inverted) depending upon the syndromes and the CODE ID position. Note that the syndromes that determine data correction are in some cases syndromes input externally via the CB inputs and in some cases syndromes generated internally by that EDC (S_i are the internal syndromes and are the same as the value of the SC_i output of that EDC if enabled).

The tables show the number of data bit inverted (corrected) if any for the CODE ID and syndrome combination.

TABLE XX. CODE ID_{2-0} = 000*

	S5	0	0	0	0	1	1	1	1
	S4	0	0	1	1	0	0	1	1
	S3	0	1	0	1	0	1	0	1
S2	S1								
0	0	–	–	–	5	–	11	14	–
0	1	–	1	2	6	8	12	–	–
1	0	–	–	3	7	9	13	15	–
1	1	–	0	4	–	10	–	–	–

*Unlisted S combinations are no correction.

TABLE XXI. CODE ID_{2-0} = 010*

	CB_6	0	0	0	0	1	1	1	1
	CB_5	1	1	1	1	0	0	0	0
	CB_4	0	0	1	1	0	0	1	1
	CB_3	0	1	0	1	0	1	0	1
CB_2	CB_1								
0	0	–	11	14	–	–	–	–	5
0	1	8	12	–	–	–	1	2	6
1	0	9	13	15	–	–	–	3	7
1	1	10	–	–	–	–	0	4	–

*Unlisted CB combinations are no correction.

TABLE XXII. CODE ID_{2-0} = 011*

S6	0	0	0	0	1	1	1	1
S5	0	0	0	0	1	1	1	1
S4	0	0	1	1	0	0	1	1
S3	0	1	0	1	0	1	0	1
S2 S1								
0 0	–	–	–	5	–	11	14	–
0 1	–	1	2	6	8	12	–	–
1 0	–	–	3	7	9	13	15	–
1 1	–	0	4	–	10	–	–	–

*Unlisted S combinations are no correction.

TABLE XXIII. CODE ID_{2-0} = 100*

CB_0	0	0	0	0	1	1	1	1
CB_6	0	0	0	0	1	1	1	1
CB_5	1	1	1	1	0	0	0	0
CB_4	0	0	1	1	0	0	1	1
CB_3	0	1	0	1	0	1	0	1
CB_2 CB_1								
0 0	–	11	14	–	–	–	–	5
0 1	8	12	–	–	–	1	2	6
1 0	9	13	15	–	–	–	3	7
1 1	10	–	–	–	–	0	4	–

*Unlisted CB combinations are no correction

TABLE XXIV. CODE ID_{2-0} = 101*

CB_0	0	0	0	0	1	1	1	1
CB_6	0	0	0	0	1	1	1	1
CB_5	0	0	0	0	1	1	1	1
CB_4	0	0	1	1	0	0	1	1
CB_3	0	1	0	1	0	1	0	1
CB_2 CB_1								
0 0	–	–	–	5	–	11	14	–
0 1	–	1	2	6	8	12	–	–
1 0	–	–	3	7	9	13	15	–
1 1	–	0	4	–	10	–	–	–

*Unlisted CB combinations are no correction.

TABLE XXV. CODE ID_{2-0} = 110*

CB_0	0	0	0	0	1	1	1	1
CB_6	1	1	1	1	0	0	0	0
CB_5	0	0	0	0	1	1	1	1
CB_4	0	0	1	1	0	0	1	1
CB_3	0	1	0	1	0	1	0	1
CB_2 CB_1								
0 0	–	–	–	5	–	11	14	–
0 1	–	1	2	6	8	12	–	–
1 0	–	–	3	7	9	13	15	–
1 1	–	0	4	–	10	–	–	–

*Unlisted CB combinations are no correction.

TABLE XXVI. CODE ID_{2-0} = 111*

CB_0	0	0	0	0	1	1	1	1
CB_6	1	1	1	1	0	0	0	0
CB_5	1	1	1	1	0	0	0	0
CB_4	0	0	1	1	0	0	1	1
CB_3	0	1	0	1	0	1	0	1
CB_2 CB_1								
0 0	–	11	14	–	–	–	–	5
0 1	8	12	–	–	–	1	2	6
1 0	9	13	15	–	–	–	3	7
1 1	10	–	–	–	–	0	4	–

*Unlisted CB combinations are no correction.

Am2960 Boosts Memory Reliability

Technical Report
Advanced Micro Devices

ABSTRACT

Memory error frequency will increase due to the use of larger memory systems and the use of 16K and 64K RAMs, which are more susceptible to soft errors because of their smaller memory cell geometry.

At the same time, the need for reliability is increasing, both for the user and the system manufacturer. EDC (Error Detection and Correction) can reduce system downtime, can reduce field maintenance expenses and can provide manufacturers a marketing advantage due to increased reliability.

The Am2960 implements EDC using a modified Hamming code, and so boosts memory reliability by a factor of 60 or better. It slashes package count and adds initialization, byte-write and diagnostic features. It is fast and flexible enough to handle word widths from 8 to 64 bits.

The Am2960 is one of a series of Memory Support devices designed for use with dynamic MOS RAM memory systems.

Prepared by: Advanced Micro Devices, Bipolar Microprocessor.

NOVEMBER 1980

Am2960 BOOSTS MEMORY RELIABILITY

The Am2960 is a 16-bit, expandable Error Detection and Correction (EDC) unit. It is used in conjunction with system main memories to boost memory reliability.

The Am2960 can correct *all* single-bit memory errors in a data word. It detects all double-bit errors and even some triple-bit errors. The gross error conditions of all 0s or all 1s are always detected.

Memory error and detection using the Am2960 boosts system reliability by a factor of 60 or better. System crashes will occur far less frequently and maintenance costs can be slashed.

MEMORY ERRORS

Memory Error Frequency

Memory errors are becoming *more* frequent due to two general trends:

1. Total system memory size is growing, and,
2. The geometry of individual memory cells in dynamic RAMs is shrinking, making them more susceptible to "soft" errors.

There are two basic types of memory errors. Hard errors are permanent physical failures of either the whole RAM, a row, a column, or a single bit. Hard errors are caused by power shorts, open leads, and various other factors. Initial testing and burn-in will reduce but not eliminate hard error failures in RAMs during system operation.

Soft errors are non-repeating, single-bit errors where there is no permanent damage. A soft error occurs when the charge state of a bit incorrectly shifts from 0 to 1 or from 1 to 0. This can be caused by system noise, pattern sensitivity, power surges[6] or alpha particles. The new 16K and 64K dynamic RAMs, with their smaller memory cell geometries are especially susceptible to soft errors induced by alpha particles. (The smaller the memory cell geometry, the less energy is required to cause the cell to change state.)

A paper given at Wescon, 1979[1] presented these failure rates for dynamic RAMs of increasing size (see Table 1). This table reflects only soft errors due to alpha particles.

Undetected Memory Failures are Expensive

Memory failures will occur in a system. When they do they will result either in a system crash or in loss of data integrity, unless memory error detection schemes are used. Either situation is expensive and inconvenient for the system users. Either situation can result in maintenance calls to the system manufacturer.

If the memory error occurs in an instruction word and the instruction is executed without being corrected, then a system crash will almost certainly occur. For example, an "Add" instruction could be changed to a "Jump" instruction with only a one-bit change – if the error is undetected, the jump would take place to essentially a random location.

If the error occurs in a word that is used for storing data, then data integrity is lost. In typical applications this could mean that bank account balances would be altered, blood diagnosis would be incorrect, or cooling water valves could be closed instead of opened.

System failures of any kind will often result in unscheduled maintenance requests to the system manufacturers. Maintenance calls are expensive for the system manufacturer and are to be avoided by preventative means if at all possible.

Strategies for Memory Errors

For reliability and maintenance cost reduction, memory errors must be dealt with by the system designer.

A common scheme is to use parity. But parity schemes cannot correct errors and can detect only single-bit errors. If a double-bit error occurs in a word, the parity is unchanged and so the error goes undetected. Parity cannot correct errors.

Error detection and correction (EDC) is implemented by the Am2960 using a modified Hamming code. The Hamming code scheme involves generating several check bits that contain enough redundant information to correct *all* single-bit errors and to detect all double-bit errors and some triple-bit errors. Also, the EDC modified Hamming code detects the gross error conditions of all 0s and all 1s.

Table 2 demonstrates that EDC is the superior strategy for both the system user and the system manufacturer.

TABLE 1. ERRORS ARE INCREASING.

Density Bits/Chip	Typical Error Rate (% per 1,000 Hours)	
	Soft*	Hard**
1K	.001	.0001
4K	.02	.002
16K	.10	.011
*64K	.5***	.016

*Reflects alpha particles only. Does not include errors due to noise, power, patterns.
**After infant mortality.
***Based on initial customer evaluation.
Note: 0.1% per 1000 hours equals 1 failure in 10^6 hours.

TABLE 2. COMPARISON OF ERROR STRATEGIES.

Error Type	No Checking	Parity	EDC Using Am2960
Single-Bit Error	System crash.	System halt.	Correctable. System runs.
Double-Bit Error	System crash.	System crash.	System halt.
Entire RAM Failure	System crash.	System halt.	Correctable. System runs.

With EDC, the incidence of maintenance calls is significantly reduced. Even the failure of an entire RAM chip will not necessarily result in a system failure. Double-bit errors are not corrected but are detected so that the system may be halted and the user informed of a memory error and the exact location of it. A controlled system halt is far more desirable than an uncontrolled system crash.

EDC Improves MTTF

Error detection and correction as implemented on the Am2960 significantly improves the MTTF (mean time to failure) of memory systems.

A paper presented at Wescon, 1979[1] used the dynamic RAM error rates shown previously to calculate the following MTTFs for a 16 Megabyte system using 64K RAMs (see Table 3).

TABLE 3.

Error Type	MTTF*
Correctable Soft Error (Single-Bit)	13 days
Correctable Hard Error (Single-Bit)	110 days
Non-Correctable Soft Error (Double-Bit)	864 days
Non-Correctable Hard Error (Double-Bit)	7,021 days

*Based on 64K RAM alpha error rate of 0.13% per 1000 hours.

The MTTF improves by a factor of at least 60 with EDC. This improvement factor has been noted by others[2].

Another paper [3,4] calculated that with EDC, RAM errors would become a small factor in memory based failures relative to failures of other board components such as MSI, capacitors and resistors. The same paper[4] discusses how frequently preventative maintenance should be done so that a hard-failed RAM is replaced prior to a second RAM experiencing a hard-failure. The Am2960 has features that allow easy logging of data errors – this aids the maintenance engineer in quickly pinpointing hard-failed RAMs and RAMs displaying excessive soft error rates.

Memory Reliability is a Competitive Edge

EDC boosts memory reliability and gives you two competitive advantages:

1. Your system is more reliable.
2. Your field maintenance costs are reduced.

The demand for reliable system performance is increasing steadily. Reliability is a must for applications in aerospace, medical, banking, process control and on-line systems. Applications such as word-processors, small business systems and telecommunications also need memory reliability, as their users do not have the technical staff to handle system failures and are willing to pay for the convenience of smooth, error-free operation.

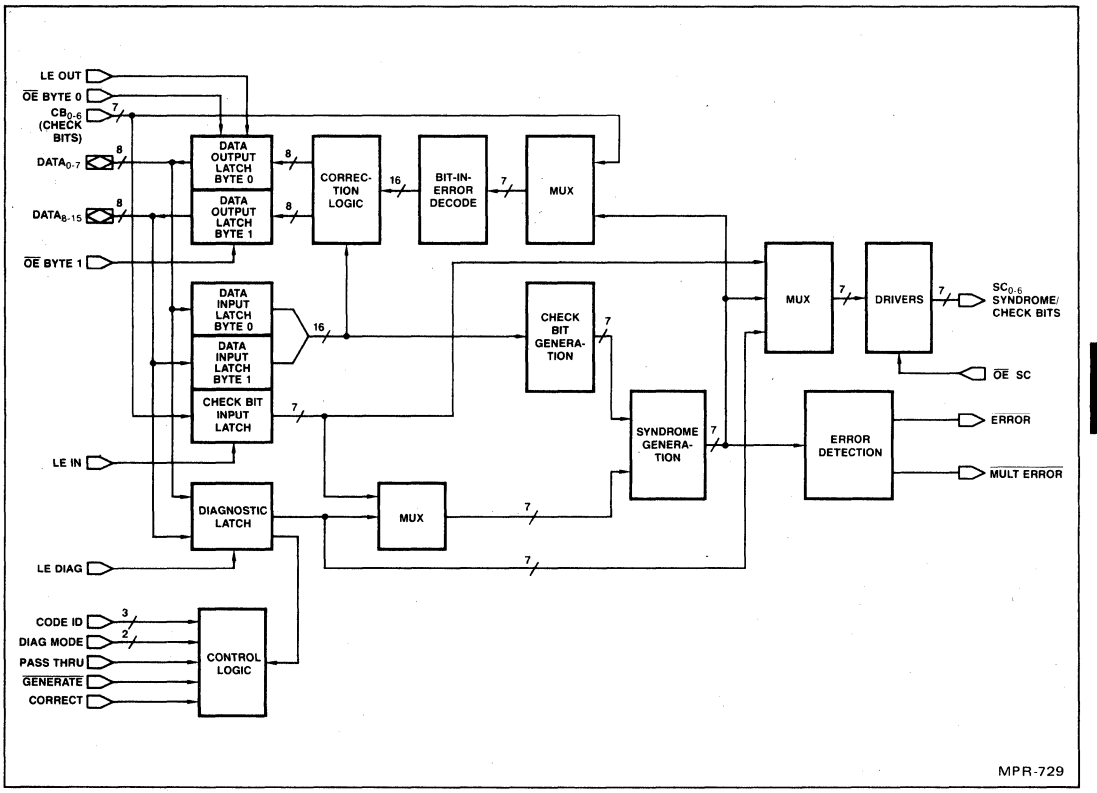


Figure 1. Block Diagram.

Am2960 ERROR DETECTION AND CORRECTION

Figure 1 shows the block diagram of the Am2960 EDC unit. The following is intended only to summarize Am2960 operation. A complete data sheet on the Am2960 EDC unit is available.

Write to Memory

On a write to memory, the Am2960 generates check bits according to a modified Hamming code. The check bits generated are stored in memory along with the data bits.

The Am2960 is a 16-bit slice and can handle all common word widths. The number of check bits required depends on the word width (see Table 4).

TABLE 4.

Number of Data Bits	Number of Check Bits Required	Number of Am2960 Required
8	5	1
16	6	1
32	7	2
48	8	3
64	8	4

Read from Memory

On a read from memory, the EDC reads in both the data and the check bits. The EDC uses the data bits to generate a second set of check bits. If the new check bits match the old, there is no error. If the check bits do not match, an exclusive-or of the two sets of check bits produce "syndrome bits," which are decoded to determine the type of error. For single-bit errors, $\overline{\text{ERROR}}$ is asserted. For multiple-bit errors, $\overline{\text{MULT ERROR}}$ is asserted. Errors are detected for data bits and check bits.

Two Operating Modes

The Am2960 can be used in two ways to protect systems from memory errors.

High-performance systems (Figure 2) may use the Am2960 in a check-only mode without slowing system operation. The Am2960 will monitor the data path and will generate a CPU interrupt if an error is detected. This error interrupt typically occurs just 25ns after data appears on the bus. The CPU then takes the corrective action chosen by the designer: automatic correction, write-back to memory, error logging, or diagnostics.

A simpler mode is to have the Am2960 in the data path (Figure 3), always correcting data on every read from memory. This simplifies CPU design and adds typically 40ns which is well within the memory cycle timing budget of most MOS microprocessor systems.

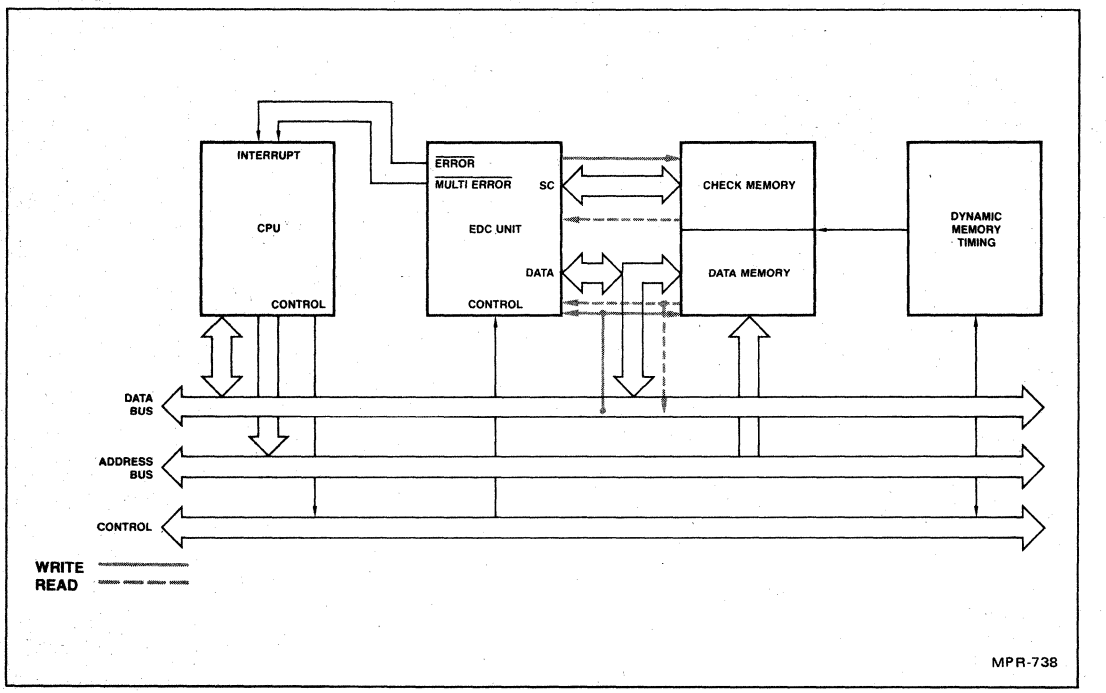


Figure 2. Check-Only Configuration.

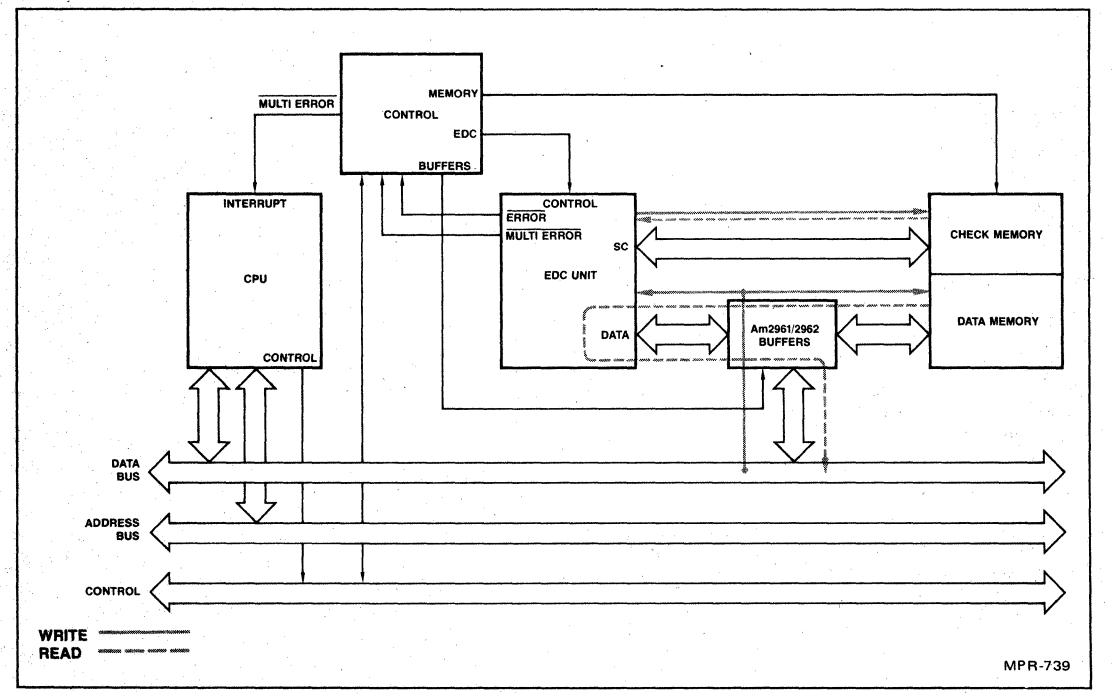


Figure 3. Correct-Always Configuration.

Byte Operations

The Am2960 has byte-wide enables on the output latch. This greatly simplifies byte-write operations. The steps for a byte-write are: 1) read the full word from memory into the EDC input latch, 2) correct the full data word and latch into the EDC output latch, 3) enable the outputs of byte 0 (or byte 1) of the EDC output latch and enable the data line inputs for byte 1 (or byte 0) to read in the new byte, 4) latch the new word into the EDC input latch, then 5) generate new check bits and write both check and data bits into memory.

Without the byte-wide enables on output, the byte-write operation would require extra steps, extra time and extra hardware.

Initialization

After power-up, system memory will contain random bit patterns with check bits that do not match the data bits. So system memory must be initialized. The Am2960 has a built-in initialization feature that forces the Data Output latch to all zeros and generates the correct corresponding check bits for writing into all system memory at power-up.

Diagnostics are Key

Since memory errors occur only every million or billion of cycles, a diagnostic feature has been built into the Am2960 that allows the device to be checked out under software control. In diagnostic mode the user may load predetermined check bits into the diagnostic latch. These check bits are then used to do a diagnostic write or a diagnostic read. The write allows diagnostic check bits to be written into memory. The read substitutes diagnostic check bits for those normally read from memory. Either operation can then be followed by bit test instructions to evaluate the EDC's response to the fictitious check bits.

A Family of Memory Support Devices

The Am2960 EDC is one of a family of memory support devices that includes:

Am2961/62 – EDC Bus Buffers
Am2964 – Dynamic Memory Controller
Am2965/66 – Memory Bus Drivers

Figure 4 shows a typical high-performance memory configuration using Am2960 Series Memory Support Devices.

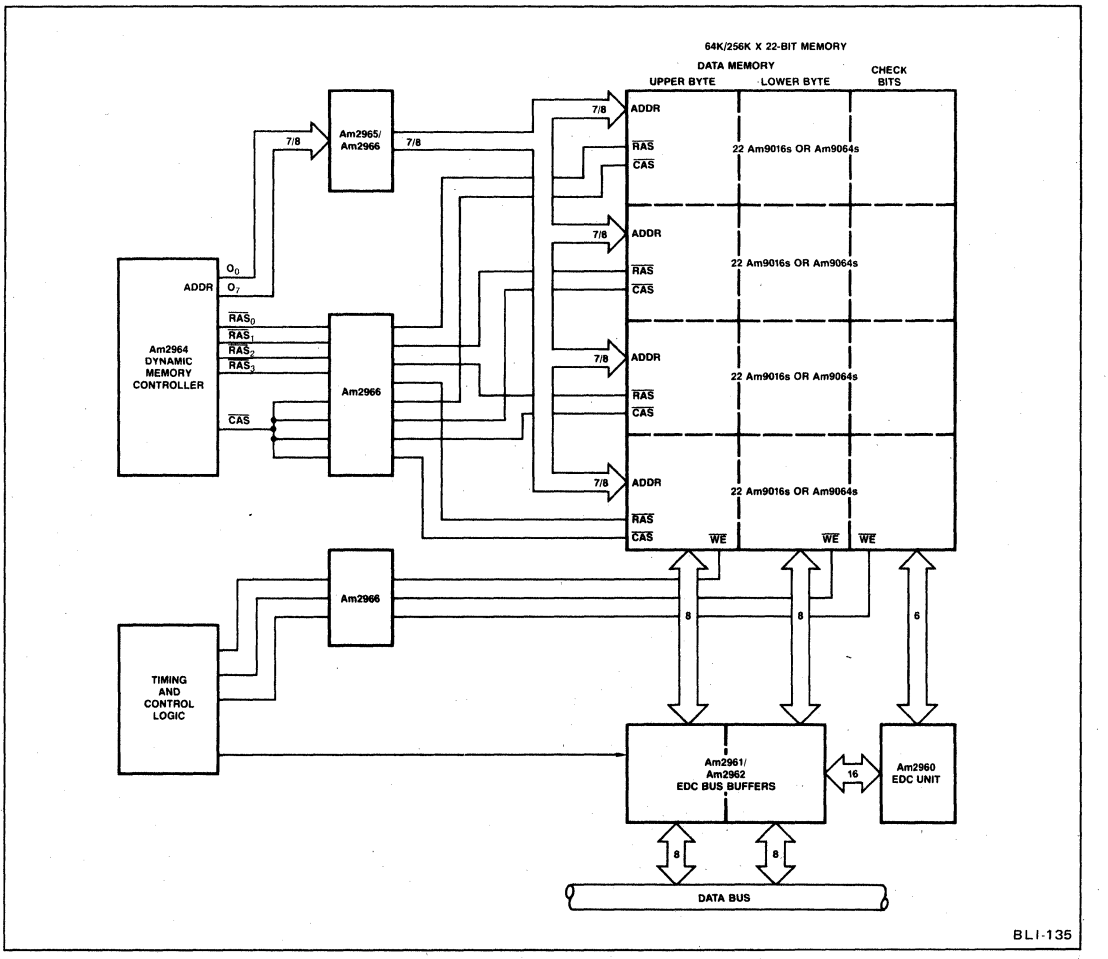


Figure 4. Dynamic Memory Control with Error Detection and Correction.

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3. Robert Koppel, "RAM Reliability in Large Memory Systems – Significance of Predicting MTBF," Computer Design, February, 1979.
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5. A.V. Ferris-Prabhu, IBM General Technology Division, "Improving Memory Reliability Through Error Correction," Computer Design, July, 1979.
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9. "Alphas Cause Rift at ECC," Electronic Engineering Times, May 28, 1979.
10. Ernst L. Wall, ITT, "Applying the Hamming Code to Microprocessor-Based Systems," Electronics, November 22, 1979.

For further information,
contact Advanced Micro Devices
Bipolar Microprocessor Applications
(408) 732-2400

These devices are also characterized as:
AmZ8161
AmZ8162

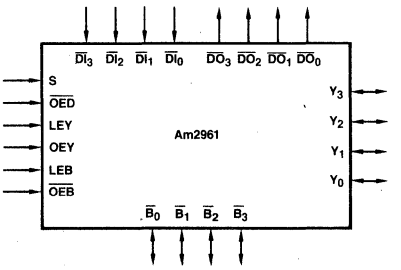
Am2961 • Am2962

4-Bit Error Correction Multiple Bus Buffers

DISTINCTIVE CHARACTERISTICS

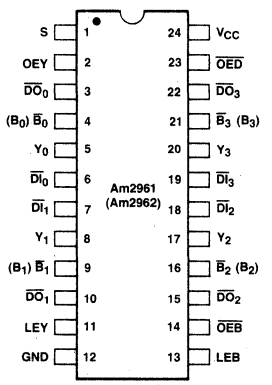
- Quad high-speed LSI bus-transceiver
- Provides complete data path interface between the Am2960 Error Detection and Correction Unit, the system data bus and dynamic RAM memory
- Three-state 24mA output to data bus
- Three-state data output to memory
- Inverting data bus for Am2961 and noninverting for Am2962
- Data bus latches allow operation with multiplexed buses
- Space saving 24-pin 0.3" package

LOGIC SYMBOL



B-Bus is noninverting for Am2962.

CONNECTION DIAGRAM
Top View



24 pin slim (0.3")

Note: Pin 1 is marked for orientation. BLI-122

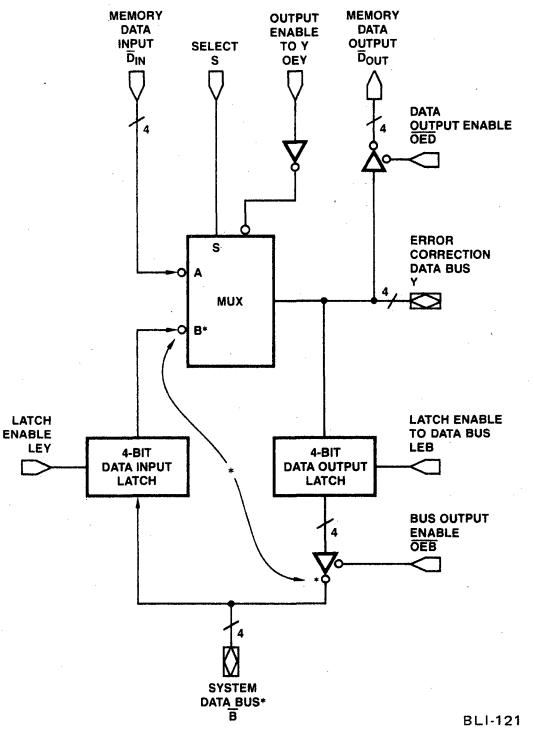
FUNCTIONAL DESCRIPTION

The Am2961 and Am2962 are high-performance, low-power Schottky multiple bus buffers that provide the complete data path interface between the Am2960 Error Detection and Correction Unit, dynamic RAM memory and the system data bus. The Am2961 provides an inverting data path between the data bus (B_i) and the Am2960 error correction data input (Y_i) and the Am2962 provides a noninverting configuration (B_i to Y_i). Both devices provide inverting data paths between the Am2960 and memory data bus thereby optimizing internal data path speeds.

The Am2961 and Am2962 are 4-bit devices. Four devices are used to interface each 16-bit Am2960 Error Detection and Correction Unit with dynamic memory. The system can easily be expanded to 32 or more bits for wider memory applications. The 4-bit configuration allows enabling the appropriate devices two-at-a-time for intermixed word or byte, read and write in 16-bit systems with error correction.

Data latches between the error correction data bus and the system data bus facilitate byte writing in memory systems wider than 8-bits. They also provide a data holding capability during single-step system operation.

LOGIC DIAGRAM



BLI-121

*Am2962 is the same function but noninverting to the system data bus, B.

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0 to +70°C V_{CC} = 5.0V ±5% (MIN = 4.75V MAX = 5.25V)

MIL T_A = −55 to +125°C V_{CC} = 5.0V ±10% (MIN = 4.50V MAX = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE – Y BUS

Parameters	Description	Test Conditions (Note 1)			Min	Typ. (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.0mA		2.4	3.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8mA			0.3	0.45	Volts
			I_{OL} = 16mA			0.35	0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V		OEY = LOW			−2.0	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		OEY = LOW			100	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V		OEY = LOW			1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−30		−130	mA

DC CHARACTERISTICS OVER OPERATING RANGE – B BUS

Parameters	Description	Test Conditions (Note 1)			Min	Typ. (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.0mA		2.4			Volts
			I_{OH} = −15mA		2.0			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA			0.3	0.45	Volts
			I_{OL} = 24mA			0.35	0.50	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V		$\overline{OEB}$ = HIGH			−1.0	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		$\overline{OEB}$ = HIGH			100	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V		$\overline{OEB}$ = HIGH			1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−50		−150	mA

Notes: 1. For conditions as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

DC CHARACTERISTICS OVER OPERATING RANGE – DO OUTPUTS

Parameters	Description	Test Conditions (Note 1)		Min	Typ. (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL I_{OH} = −50μA	2.5			Volts
			COM'L I_{OH} = −100μA	2.7			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 1mA			0.4	Volts
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−50		−150	mA
I_O	Off-State Out Current	V_{CC} = MAX	V_O = 0.4V			−100	μA
			V_O = 2.4V			+100	

DC CHARACTERISTICS OVER OPERATING RANGE – DI INPUTS AND CONTROLS

Parameters	Description	Test Conditions (Note 1)		Min	Typ. (Note 2)	Max	Units
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_C	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	DI Inputs			−1.0	mA
			Controls			−1.6	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA

DC CHARACTERISTICS OVER OPERATING RANGE – POWER SUPPLY

Parameters	Description	Test Conditions (Note 1)	Min	Typ. (Note 2)	Max	Units
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX		110	155	mA

Note 4:

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} MAX
DC Input Voltage	5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

Am2961
SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	COM'L T_A = 0 to +70°C, V_{CC} = 5.0V ±5% Min	COM'L Max	MIL T = −55 to +125°C, V_{CC} = 5.0V ±10% Min	MIL Max	Units	Test Conditions
t_{PLH}	Propagation Delay $\overline{B}$ to Y (Latch Transparent, OEY = LEY = HIGH)		25		28	ns	Figure 1, C_L = 5pF, R_L = 390Ω, R_2 = 1kΩ
t_{PHL}			25		28	ns	
t_{PLH}	Propagation Delay $\overline{DI}$ to Y (OEY = HIGH, S = LOW)		15		18	ns	
t_{PHL}			15		18	ns	
t_{PLH}	Propagation Delay S to Y (OEY = HIGH)		25		28	ns	
t_{PHL}			25		28	ns	
t_{PLH}	Propagation Delay LEY to Y (OEY = S = HIGH)		25		30	ns	
t_{PHL}			35		40	ns	
t_{PZH}	Y Bus Output Enable Time OEY to Y		18		21	ns	
t_{PZL}			18		21	ns	
t_{PHZ}	Y Bus Output Disable Time OEY to Y		18		21	ns	
t_{PLZ}			18		21	ns	
t_{PLH}	Propagation Delay LEB to $\overline{B}$ ($\overline{OEB}$ = LOW)		25		30	ns	Figure 1, C_L = 50pF, R_L = 270Ω, R_2 = 1kΩ
t_{PHL}			35		40	ns	
t_{PLH}	Propagation Delay Y to $\overline{B}$ (Latch Transparent, LEB = HIGH, $\overline{OEB}$ = LOW, OEY = LOW)		18		21	ns	
t_{PHL}			20		23	ns	
t_{PLH}	Propagation Delay Y to $\overline{B}$ (Latch Transparent, LEB = HIGH, $\overline{OEB}$ = LOW, OEY = LOW)		26		30	ns	Figure 1, C_L = 300pF, R_L = 270Ω, R_2 = 1kΩ
t_{PHL}			31		35	ns	
t_{PZH}	$\overline{B}$ Bus Output Enable Time $\overline{OEB}$ to $\overline{B}$		18		21	ns	Figure 1, C_L = 50pF, R_L = 270Ω, R_2 = 1kΩ
t_{PZL}			18		21	ns	
t_{PLZ}	$\overline{B}$ Bus Output Disable Time $\overline{OEB}$ to $\overline{B}$		18		21	ns	
t_{PHZ}			18		21	ns	
t_{PLH}	Propagation Delay Y to $\overline{DO}$ ($\overline{OED}$ = OEY = LOW)		15		18	ns	Figure 2, C_L = 50pF, R = 2kΩ
t_{PHL}			20		23	ns	
t_{PZH}	$\overline{DO}$ Output Enable Time $\overline{OED}$ to $\overline{DO}$		28		30	ns	S = 2 — Figure 3, C_L = 50pF, R = 680Ω
t_{PZL}			28		30	ns	S = 1
t_{PHZ}	$\overline{DO}$ Output Disable Time $\overline{OED}$ to $\overline{DO}$		16		18	ns	S = 2
t_{PLZ}			24		28	ns	S = 1
t_S	$\overline{B}$ to LEY Set-up Time ($\overline{OEB}$ = HIGH)	6		6		ns	Figure 1, C_L = 50pF, R_L = 390Ω, R_2 = 1kΩ
t_H	$\overline{B}$ to LEY Hold Time ($\overline{OEB}$ = HIGH)	9		10		ns	
t_S	Y to LEB Set-up Time (OEY = LOW)	6		6		ns	Figure 1, C_L = 50pF, R_L = 270Ω, R_2 = 1kΩ
t_H	Y to LEB Hold Time (OEY = LOW)	9		10		ns	

*AC perfomance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

SWITCHING TEST CIRCUITS

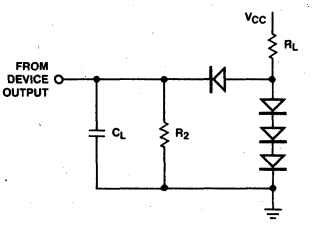


Figure 1.

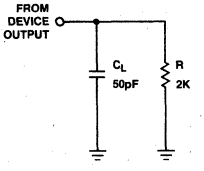


Figure 2.

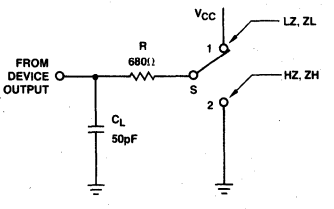


Figure 3.

Am2962
SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	COM'L T_A = 0 to +70°C, V_{CC} = 5.0V ±5% Min	COM'L Max	MIL T = −55 to +125°C, V_{CC} = 5.0V ±10% Min	MIL Max	Units	Test Conditions
t_{PLH}	Propagation Delay B to Y (Latch Transparent, OEY = LEY = HIGH)		27		28	ns	Figure 1, C_L = 5pF, R_L = 390Ω, R_2 = 1kΩ
t_{PHL}			27		28	ns	
t_{PLH}	Propagation Delay $\overline{DI}$ to Y (OEY = HIGH, S = LOW)		15		18	ns	
t_{PHL}			15		18	ns	
t_{PLH}	Propagation Delay S to Y (OEY = HIGH)		25		28	ns	
t_{PHL}			25		28	ns	
t_{PLH}	Propagation Delay LEY to Y (OEY = S = HIGH)		25		30	ns	
t_{PHL}			35		40	ns	
t_{PZH}	Y Bus Output Enable Time OEY to Y		18		21	ns	
t_{PZL}			18		21	ns	
t_{PHZ}	Y Bus Output Disable Time OEY to Y		18		21	ns	
t_{PLZ}			18		21	ns	
t_{PLH}	Propagation Delay LEB to B ($\overline{OEB}$ = LOW)		25		30	ns	Figure 1, C_L = 50pF, R_L = 270Ω, R_2 = 1kΩ
t_{PHL}			35		40	ns	
t_{PLH}	Propagation Delay Y to B (Latch Transparent, LEB = HIGH, $\overline{OEB}$ = LOW, OEY = LOW)		20		23	ns	
t_{PHL}			21		24	ns	
t_{PLH}	Propagation Delay Y to B (Latch Transparent, LEB = HIGH, $\overline{OEB}$ = LOW, OEY = LOW)		28		32	ns	Figure 1, C_L = 300pF, R_L = 270Ω, R_2 = 1kΩ
t_{PHL}			32		36	ns	
t_{PZH}	B Bus Output Enable Time $\overline{OEB}$ to B		18		21	ns	Figure 1, C_L = 50pF, R_L = 270Ω, R_2 = 1kΩ
t_{PZL}			18		21	ns	
t_{PLZ}	B Bus Output Disable Time $\overline{OEB}$ to B		18		21	ns	
t_{PHZ}			18		21	ns	
t_{PLH}	Propagation Delay Y to $\overline{DO}$ ($\overline{OED}$ = OEY = LOW)		15		18	ns	Figure 2, C_L = 50pF, R = 2kΩ
t_{PHL}			20		23	ns	
t_{PZH}	$\overline{DO}$ Output Enable Time $\overline{OED}$ to $\overline{DO}$		28		30	ns	S = 2
t_{PZL}			28		30	ns	S = 1
t_{PHZ}	$\overline{DO}$ Output Disable Time $\overline{OED}$ to $\overline{DO}$		16		18	ns	S = 2
t_{PLZ}			24		28	ns	S = 1
							Figure 3, C_L = 50pF, R = 680Ω
t_S	B to LEY Set-up Time ($\overline{OEB}$ = HIGH)	8		8		ns	Figure 1, C_L = 50pF, R_L = 390Ω, R_2 = 1kΩ
t_H	B to LEY Hold Time ($\overline{OEB}$ = HIGH)	8		9		ns	
t_S	Y to LEB Set-up Time (OEY = LOW)	8		8		ns	Figure 1, C_L = 50pF, R_L = 270Ω, R_2 = 1kΩ
t_H	Y to LEB Hold Time (OEY = LOW)	8		9		ns	

*AC perfomance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

B_0, B_1 B_2, B_3 The four bidirectional system data bus inputs/outputs. The B-to-Y path is inverting for the Am2961 ($\overline{B}_i$) and noninverting for the Am2962 (B_i).

$\overline{OEB}$ The three-state Output Enable for the system data bus output drivers. When $\overline{OEB}$ is LOW data from the Data Output Latch is output to the system data bus. When $\overline{OEB}$ is HIGH the bus drivers are in the high-impedance state and the Data Input Latch can receive input data from the system data bus.

LEB Latch Enable for the Data Output Latch. When LEB is HIGH the latch is transparent and Y-Bus data is output to the B-Bus. When LEB goes LOW, Y-Bus data meeting the latch set-up and hold time requirements is latched for output to the B-Bus.

Y_0, Y_1, Y_2, Y_3 The four bidirectional EDC data inputs/outputs for connection to the EDC data I/O port.

LEY The Latch Enable control for the Data Input Latch for the data input from the system data bus (B). When LEY is HIGH the latch is transparent and B input data is available at the MUX input for selection to the Y outputs. When LEY goes LOW, B input data meeting the latch set-up and hold time requirements is latched for subsequent selection to the Y outputs.

OEY Output Enable for the Y (EDC) Bus outputs. When OEY is HIGH data selected by the input data multiplexer is output to the Y-bus. When OEY is LOW the MUX output is in the high-impedance state and the Y-Bus can receive input data from the EDC Unit.

S The Select input for the input data multiplexer. A LOW input selects data from the memory data input, $\overline{DI}$, for output to the EDC bus (Y). A HIGH input selects data from the system data bus Data Input Latch (B or $\overline{B}$).

$\overline{DO}_0$, $\overline{DO}_1$, $\overline{DO}_2$, $\overline{DO}_3$ The Data Outputs to the memory data inputs. The $\overline{DO}$ outputs are inverted with respect to the EDC Bus (Y). These outputs are "RAM Driver" outputs with a collector resistor in the lower output driver to protect against undershoot on the HIGH-to-LOW transition.

$\overline{OED}$ Output Enable for the $\overline{DO}$ outputs. An active LOW input causes the $\overline{DO}$ outputs to output inverted data from the EDC (Y) Bus and a HIGH input puts the $\overline{DO}$ outputs in the high-impedance state.

$\overline{DI}_0$, $\overline{DI}_1$, $\overline{DI}_2$, $\overline{DI}_3$ The Data Inputs from memory. $\overline{DI}$ inputs are selected by the data input MUX for output to the EDC (Y) Bus (controlled by S and OEY) and/or output to the system data bus (B) (controlled by LEB and $\overline{OEB}$).

FUNCTION TABLES

Y-BUS OUTPUT

LEY	$\overline{DI_i}$	$\overline{B_i}$* Am2961	B_i* Am2962	S	OEY	Y
X	X	X	X	X	L	Z
X	L	X	X	L	H	H
X	H	X	X	L	H	L
H	X	L	H	H	H	H
H	X	H	L	H	H	L
L	X	X	X	H	H	NC

*$\overline{OEB}$ = HIGH for B data input

B-BUS OUTPUT

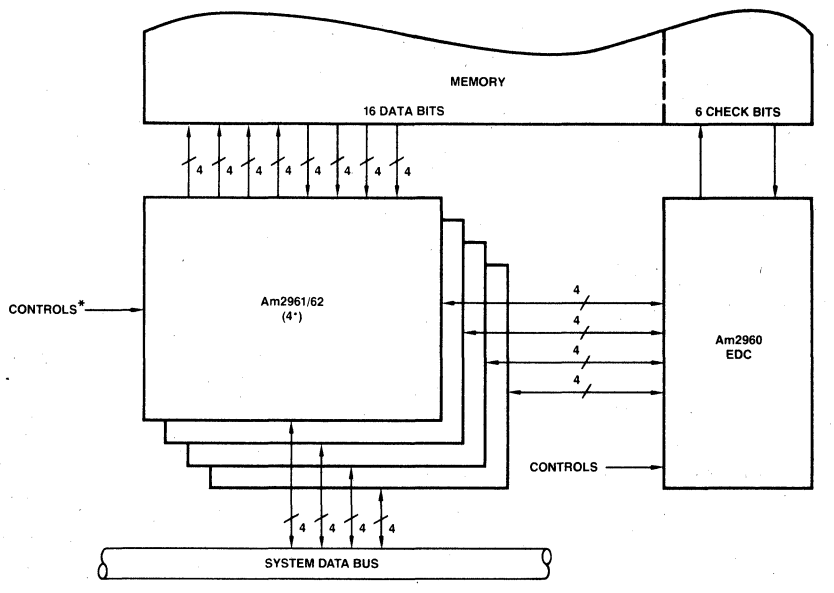
Y* Input	LEB	$\overline{OEB}$	$\overline{B}$ Am2961	B Am2962
X	X	H	Z	Z
L	H	L	H	L
H	H	L	L	H
X	L	L	NC	NC

*OEY = LOW for B data input

$\overline{DO}$ PORT OUTPUT

Y	$\overline{OED}$	$\overline{DO}$
X	H	Z
L	L	H
H	L	L

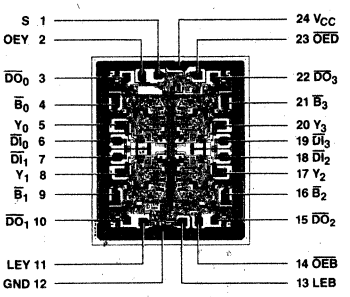
APPLICATION



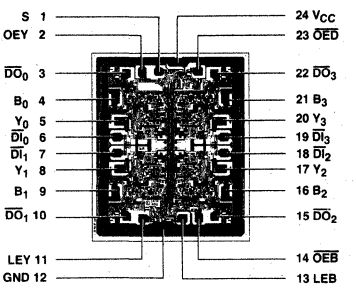
*Since the EDC Data Bus Buffers are four-bit wide devices, controls can be paired to device inputs to provide byte level controls (for any data width).

METALLIZATION AND PAD LAYOUTS

Am2961



Am2962



DIE SIZES .102" X .087"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2961 Order Number	Am2962 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2961DC	AM2962DC	D-24-SLIM	C	C-1
AM2961DC-B	AM2962DC-B	D-24-SLIM	C	B-2 (Note 4)
AM2961DM	AM2962DM	D-24-SLIM	M	C-3
AM2961DM-B	AM2962DM-B	D-24-SLIM	M	B-3
AM2961FM	AM2962FM	F-24	M	C-3
AM2961FM-B	AM2962FM-B	F-24	M	B-3
AM2961LC	AM2962LC	L-20	C	C-1
AM2961LCB	AM2962LCB	L-20	C	B-2
AM2961LM	AM2962LM	L-20	M	C-3
AM2961LMB	AM2962LMB	L-20	M	B-3
AM2961XC	AM2962XC	Dice	C	Visual inspection to MIL-STD-883 method 2010B
AM2961XM	AM2962XM	Dice	M	

Notes: 1. D = Hermetic DIP, F = Flat Pak, L = Chip-Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to +70°C, V_{CC} = 4.75V to 5.25V, M = −55 to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

Am2964B

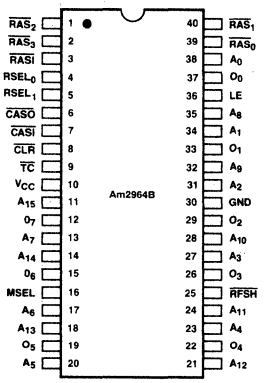
Dynamic Memory Controller

DISTINCTIVE CHARACTERISTICS

- Dynamic Memory Controller for 16K and 64K MOS dynamic RAMs
- 8-Bit Refresh Counter for refresh address generation, has clear input and terminal count output
- Refresh Counter terminal count selectable at 256 or 128
- Latch input $\overline{RAS}$ Decoder provides 4 $\overline{RAS}$ outputs, all active during refresh
- Dual 8-Bit Address Latches plus separate $\overline{RAS}$ Decoder Latches
- Grouping functions on a common chip minimizes speed differential or skew between address, $\overline{RAS}$ and $\overline{CAS}$ outputs
- 3-Port, 8-Bit Address Multiplexer with Schottky speed
- Burst mode, distributed refresh or transparent refresh mode determined by user
- Noninverting address, $\overline{RAS}$ and $\overline{CAS}$ paths

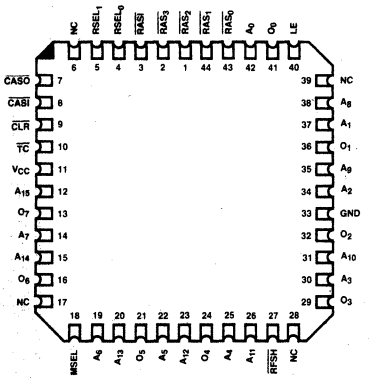
CONNECTION DIAGRAMS
Top Views

DIP



BLI-124

Chip-Pak



Note: Pin 1 is marked for orientation.

FUNCTIONAL DESCRIPTION

The Am2964B Dynamic Memory Controller (DMC) replaces a dozen MSI devices by grouping several unique functions. Two 8-bit latches capture and hold the memory address. These latches and a clearable, 8-bit refresh counter feed into an 8-bit, 3-input, Schottky speed MUX, for output to the dynamic RAM address lines.

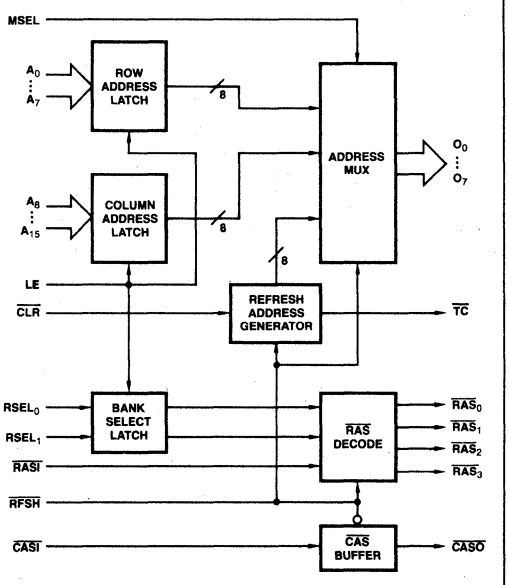
The same silicon chip also includes a special $\overline{RAS}$ decoder and $\overline{CAS}$ buffer. Placing these functions on the same chip minimizes the time skew between output functions which would otherwise be separate MSI chips, and therefore, allows a faster memory cycle time by the amount of skew eliminated.

The $\overline{RAS}$ Decoder allows upper addresses to select one-of-four banks of RAM by determining which bank receives a $\overline{RAS}$ input. During refresh ($\overline{RFSH}$ = LOW) the decoder mode is changed to four-of-four and all banks of memory receive a $\overline{RAS}$ input for refresh in response to a $\overline{RASI}$ active LOW input. $\overline{CAS}$ is inhibited during refresh.

Burst mode refresh is accomplished by holding $\overline{RFSH}$ LOW and toggling $\overline{RASI}$.

A_{15} is a dual function input which controls the refresh counter's range. For 64K RAMs it is an address input. For 16K RAMs it can be pulled to +12V through 1KΩ to terminate the refresh count at 128 instead of 256.

LOGIC DIAGRAM



BLI-123

MAXIMUM RATINGS (Above which useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} MAX
DC Input Voltage	−0.5 to 5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise noted)

(Group A, Subgroups 1, 2 and 3)

Am2964XC T_A = 0 to + 70°C V_{CC} = 5.0V ± 5% (Com'l) MIN = 4.75V MAX = 5.25V

Am2964XM T_C = −55 to +125°C V_{CC} = 5.0V ± 10% (MIL) MIN = 4.50V MAX = 5.50V

Parameters	Description	Test Conditions (Note 1)		Min	TYP (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}, I_{OH} = −1mA	$\overline{TC}$	2.5			Volts
			Others	3.0			Volts
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}, I_{OH} = −15mA	All outputs except $\overline{TC}$	2.0			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	All outputs except $\overline{TC}$, I_{OL} = 16mA			0.5	Volts
			$\overline{TC}$, I_{OL} = 8mA			0.5	Volts
V_{IH}	Input HIGH level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	$\overline{RASI}$			−3.2	mA
			$\overline{CASI}$, MSEL, $\overline{RFSH}$			−1.6	mA
			A_0 − A_{15}, $\overline{CLR}$ $RSEL_{0,1}$, LE			−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	$\overline{RASI}$			100	µA
			$\overline{CASI}$, MSEL, $\overline{RFSH}$			50	µA
			A_0-A_{15}, $\overline{CLR}$ $RSEL_{0,1}$, LE			20	µA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V	$\overline{RASI}$			2.0	mA
			$\overline{CASI}$, MSEL, $\overline{RFSH}$			1.0	mA
		V_{CC} = MAX, V_{IN} = 5.5V	A_0-A_{15}, $\overline{CLR}$ $RSEL_{0,1}$, LE			0.1	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX (Note 3)		−40		−100	mA
I_{CC}	Power Supply Current (Note 4)	25°C, 5V			122		mA
		0 to 70°C	COM'L			173	mA
		70°C				165	mA
		−55 to +125°C	MIL			165	mA
		+125°C				150	mA
I_T	A_{15} Enable Current	A_{15} connected to +12V through 1KΩ ± 10%				5	mA

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} is worst case when the Address inputs are latched HIGH, the refresh counter is at terminal count (255), $\overline{RASI}$ and $\overline{CASI}$ are HIGH and all other inputs are LOW.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR C_L = 50pF

(Notes 5, 6)

Parameter		Description	T_A = +25°C, V_{CC} = 5.0V	COM'L: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%		MIL: T_C = −55°C to +125°C, V_{CC} = 5.0V ± 10%		Units	Test Conditions
			Typ.	Min.	Max.	Min.	Max.		
1	t_{PD}	A_i to O_i Delay	14		19		23	ns	C_L = 50pF
2	t_{PHL}	$\overline{RASI}$ to $\overline{RAS_i}$ ($\overline{RFSH}$ = H)	14		20		23	ns	
3	t_{PHL}	$\overline{RASI}$ to $\overline{RAS_i}$ ($\overline{RFSH}$ = L)	14		20		23	ns	
4	t_{PD}	MSEL to O_i	17	9		9		ns	
5	t_{PD}	MSEL to O_i	17		21		25	ns	
6	t_{PHL}	$\overline{CASI}$ to $\overline{CASO}$ ($\overline{RFSH}$ = H)	12		17		19	ns	
7	t_{PHL}	$RSEL_i$ to $\overline{RAS_i}$ (LE = H, $\overline{RASI}$ = L)	15		20		24	ns	
8	t_{PLH}	$\overline{RFSH}$ to $\overline{TC}$ ($\overline{RASI}$ = L)	30		40		50	ns	
9	t_{PLH}	$\overline{RASI}$ to $\overline{TC}$ ($\overline{RFSH}$ = L)	25		35		40	ns	
10	t_{PW}	$\overline{RASI}$ = L ($\overline{RFSH}$ = L)	10	50		50		ns	
11	t_{PW}	$\overline{RASI}$ = H ($\overline{RFSH}$ = L)	10	50		50		ns	
12	t_{PD}	$\overline{RFSH}$ to O_i ($\overline{RASI}$ = X)	17		21		25	ns	
13	t_{PHL}	$\overline{RFSH}$ to $\overline{RAS_i}$ ($\overline{RASI}$ = L)	19		26		29	ns	
14	t_{PW}	$\overline{CLR}$ = L	10	30		35		ns	
15	t_{PLH}	$\overline{RFSH}$ to $\overline{CASO}$ ($\overline{RASI}$ = L $\overline{CASI}$ = L, Note 7)	16		21		25	ns	
16	t_{PD}	LE to O_i	25		35		40	ns	
17	t_{PHL}	LE to $\overline{RAS_i}$	30		40		45	ns	
18	t_{PLH}	$\overline{CLR}$ to $\overline{TC}$	35		45		56	ns	
19	t_{PLH}	$\overline{CLR}$ to O_i ($\overline{RFSH}$ = L)	31		44		54	ns	
20	t_S	A_i to LE Set-up Time	0	5		5		ns	
21	t_H	A_i to LE Hold Time	5	12		15		ns	
22	t_S	$RSEL_i$ to LE Set-up Time	0	5		5		ns	
23	t_H	$RSEL_i$ to LE Hold Time	10	17		25		ns	
24	t_S	$\overline{CLR}$ Recovery Time	10	16		18		ns	
25	t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = H, Note 8)	2		5		6	ns	
26	t_{SKEW}	O_i to $\overline{CASO}$ (Note 8)	6		8		8	ns	
27	t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = L, Note 9)	6		8		10	ns	
28	t_{SKEW}	O_i to $\overline{RAS_i}$ (MSEL = ↯, Note 10)	1		5		5	ns	

Notes:
5. Minimum spec limits for t_{PW}, t_S and t_H are minimum system operating requirements. Limits for t_{SKEW} and t_{PD} are guaranteed test limits for the device.
6. All AC parameters are specified at the 1.5V level.
7. $\overline{RFSH}$ inhibits $\overline{CASO}$ during refresh. Specification is for $\overline{CASO}$ inhibit time.
8. O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = HIGH) skew is guaranteed maximum difference between fastest $\overline{RASI}$ to $\overline{RAS_i}$ delay and slowest A_i to O_i delay within a single device. O_i to $\overline{CASO}$ skew is maximum difference between fastest $\overline{CASI}$ to $\overline{CASO}$ delay and slowest MSEL to O_i delay within a single device. See application section entitled Memory Cycle Timing for correlation to System Timing requirements.
9. O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = LOW) skew is guaranteed maximum difference between fastest $\overline{RASI}$ to $\overline{RAS_i}$ delay and slowest $\overline{RFSH}$ to O_i delay within a single device. See application section on Refresh Timing for correlation to system refresh timing requirements.
10. O_i to $\overline{RAS_i}$ (MSEL = ↯) skew is guaranteed maximum difference between fastest MSEL ↯ to O_i delay and slowest $\overline{RASI}$ to $\overline{RAS_i}$ delay within a single device.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR C_L = 150pF

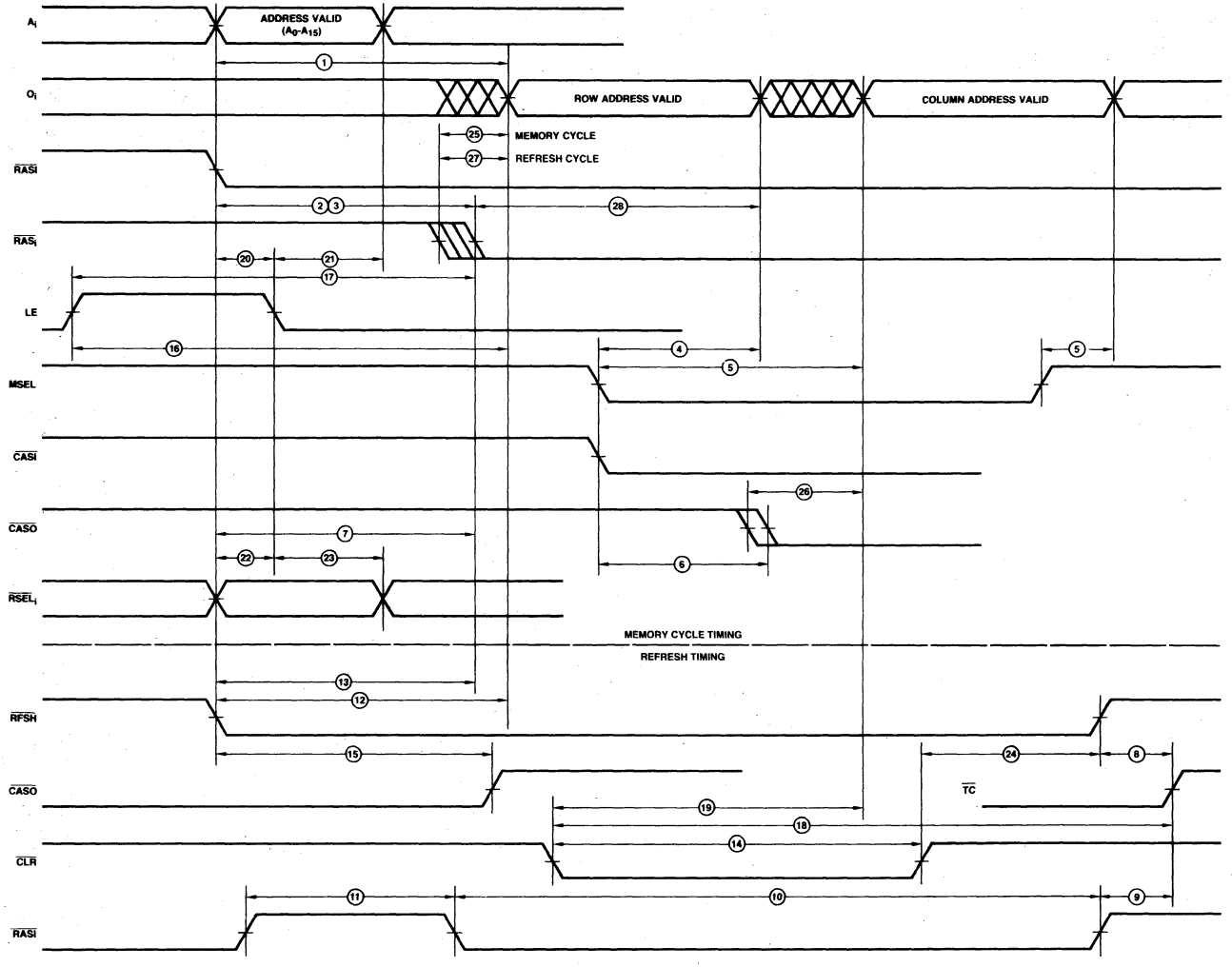
(Notes 5, 6)

Parameter		Description	T_A = +25°C, V_{CC} = 5.0V Typ.	COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5% Min.	COM'L Max.	MIL T_C = −55°C to +125°C, V_{CC} = 5.0V ± 10% Min.	MIL Max.	Units	Test Conditions
1	t_{PD}	A_i to O_i Delay	20		25		30	ns	
2	t_{PHL}	$\overline{RASI}$ to $\overline{RAS_i}$ ($\overline{RFSH}$ = H)	18		24		27	ns	
3	t_{PHL}	$\overline{RASI}$ to $\overline{RAS_i}$ ($\overline{RFSH}$ = L)	18		24		27	ns	
4	t_{PD}	MSEL to O_i	23	12		12		ns	
5	t_{PD}	MSEL to O_i	23		27		31	ns	
6	t_{PHL}	$\overline{CASI}$ to $\overline{CASO}$ ($\overline{RFSH}$ = H)	17		24		26	ns	
7	t_{PHL}	$RSEL_i$ to $\overline{RAS_i}$ (LE = H, $\overline{RASI}$ = L)	19		27		30	ns	
8	t_{PLH}	$\overline{RFSH}$ to $\overline{TC}$ ($\overline{RASI}$ = L)	34		45		55	ns	
9	t_{PLH}	$\overline{RASI}$ to $\overline{TC}$ ($\overline{RFSH}$ = L)	32		45		55	ns	
10	t_{PW}	$\overline{RASI}$ = L ($\overline{RFSH}$ = L)	10	50		50		ns	
11	t_{PW}	$\overline{RASI}$ = H ($\overline{RFSH}$ = L)	10	50		50		ns	
12	t_{PD}	$\overline{RFSH}$ to O_i ($\overline{RASI}$ = X)	21		27		30	ns	
13	t_{PHL}	$\overline{RFSH}$ to $\overline{RAS_i}$ ($\overline{RASI}$ = L)	25		33		36	ns	C_L = 150pF
14	t_{PW}	$\overline{CLR}$ = L	10	30		35		ns	
15	t_{PLH}	$\overline{RFSH}$ to $\overline{CASO}$ ($\overline{RASI}$ = L $\overline{CASI}$ = L, Note 7)	21		27		31	ns	
16	t_{PD}	LE to O_i	30		40		50	ns	
17	t_{PHL}	LE to $\overline{RAS_i}$	34		45		54	ns	
18	t_{PLH}	$\overline{CLR}$ to $\overline{TC}$	39		55		60	ns	
19	t_{PLH}	$\overline{CLR}$ to O_i ($\overline{RFSH}$ = L)	38		50		62	ns	
20	t_S	A_i to LE Set-up Time	0	5		5		ns	
21	t_H	A_i to LE Hold Time	5	12		12		ns	
22	t_S	$RSEL_i$ to LE Set-up Time	0	5		5		ns	
23	t_H	$RSEL_i$ to LE Hold Time	10	17		25		ns	
24	t_S	$\overline{CLR}$ Recovery Time	10	16		18		ns	
25	t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = H, Note 8)	3		6		7	ns	
26	t_{SKEW}	O_i to $\overline{CASO}$ (Note 8)	6		8		8	ns	
27	t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{RFSH}$ = L, Note 9)	6		9		10	ns	
28	t_{SKEW}	O_i to $\overline{RAS_i}$ ($\overline{MSEL}$ = ↯, Note 10)	1		5		5	ns	

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful.

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5−8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100's of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.



Am2964B Dynamic Memory Controller Timing

DEFINITION OF FUNCTIONAL TERMS

A_0-A_7 The low order Address inputs are used to latch eight Row Address inputs for the RAM. These inputs drive the outputs 0_0-0_7 when MSEL is HIGH.

A_8-A_{15} The high order Address inputs are used to latch eight Column Address inputs for the RAM. These inputs drive the outputs 0_0-0_7 when MSEL is LOW.

A_{15} A_{15} is a dual input. With normal TTL level inputs A_{15} acts as address input A_{15} for 64K RAMs. If A_{15} is pulled up to +12V through a 1KΩ resistor, the terminal count output, $\overline{TC}$, will go LOW every 128 counts (for 16K RAMs) instead of every 256 counts.

0_0-0_7 The RAM address outputs. The eight-bit width is designed for dynamic RAMs up to 64K.

MSEL The Multiplexer-SELect input determines whether low order or high order address inputs appear at the multiplexer outputs 0_0-0_7. When MSEL is HIGH the low order address latches (A_0-A_7) are connected to the outputs. When MSEL is LOW the high order address latches are connected to the outputs.

$\overline{RFSH}$ The Refresh control input. When active LOW the $\overline{RFSH}$ input switches the address output multiplexer to output the inverted contents of the 8-bit refresh counter. $\overline{RFSH}$ LOW also inhibits the $\overline{CAS}$ buffer and changes the mode of the $\overline{RAS}$ decoder from one-of-four to four-of-four so that all four $\overline{RAS}$ decoder outputs, $\overline{RAS_0}$, $\overline{RAS_1}$, $\overline{RAS_2}$ and $\overline{RAS_3}$, go LOW in response to a LOW input at $\overline{RASI}$. This action refreshes one row address in each of the four $\overline{RAS}$ decoded memory banks. The refresh counter is advanced at the end of each refresh cycle by the LOW-to-HIGH transition of $\overline{RFSH}$ or $\overline{RASI}$ (whichever occurs first). In burst mode refresh, $\overline{RFSH}$ may be held LOW and refresh accomplished by toggling $\overline{RASI}$.

$\overline{TC}$ The Terminal Count output. A LOW output at $\overline{TC}$ indicates that the refresh counter has been sequenced through either 128 or 256 refresh addresses depending on A_{15}. The $\overline{TC}$ output remains active LOW until the refresh counter is advanced by the rising edge of $\overline{RASI}$ or $\overline{RFSH}$.

$\overline{CLR}$ The refresh counter Clear input. An active LOW input at $\overline{CLR}$ resets the refresh counter to all LOW (refresh address output to all HIGH).

LE The address latch enable input. An active HIGH input at LE causes the two 8-bit address latches and the 2-bit $\overline{RAS}$ Select input latch to go transparent, accepting new input data. A LOW input on LE latches the input data which meets set-up and hold time requirements.

$RSEL_0$ and $RSEL_1$ The $\overline{RAS}$ decoder Select inputs. Data (latched) at these inputs (normally higher order addresses) is decoded by the $\overline{RAS}$ Decoder to "$\overline{RAS}$ Select" one of four banks of memory with $\overline{RAS_0}$, $\overline{RAS_1}$, $\overline{RAS_2}$ or $\overline{RAS_3}$.

$\overline{RASI}$ The Row Address Strobe Input. During normal memory cycles the selected $\overline{RAS}$ Decoder output $\overline{RAS_0}$, $\overline{RAS_1}$, $\overline{RAS_2}$ or $\overline{RAS_3}$ will go active LOW in response to an active LOW input at $\overline{RASI}$. During refresh ($\overline{RFSH}$ = LOW), all $\overline{RAS}$ outputs go LOW in response to $\overline{RASI}$ = LOW.

$\overline{RAS_0}$, $\overline{RAS_1}$ $\overline{RAS_2}$, $\overline{RAS_3}$ Row Address Strobe outputs ($\overline{RAS_i}$). Each provides a Row Address Strobe for one of the four banks of memory. Each will go active LOW only when selected by $RSEL_0$ and $RSEL_1$ and only when $\overline{RASI}$ goes active LOW. All $\overline{RAS_{0\text{-}3}}$ outputs go active low in response $\overline{RASI}$ when $\overline{RFSH}$ goes LOW.

$\overline{CASI}$ The Column Address Strobe. An active LOW input at $\overline{CASI}$ will result in an active LOW output at $\overline{CASO}$, unless a refresh cycle is in progress ($\overline{RFSH}$ = LOW).

$\overline{CASO}$ The Column Address Strobe output. The active LOW $\overline{CASO}$ output strobes the Column Address into the dynamic RAM. $\overline{CASO}$ is inhibited during refresh ($\overline{RFSH}$ = LOW).

$\overline{RAS}$ OUTPUT FUNCTION TABLE

$\overline{RFSH}$	$\overline{RASI}$	$RSEL_1$	$RSEL_0$	$\overline{RAS_0}$	$\overline{RAS_1}$	$\overline{RAS_2}$	$\overline{RAS_3}$
L	H	X	X	H	H	H	H
L	L	X	X	L	L	L	L
H	H	X	X	H	H	H	H
H	L	L	L	L	H	H	H
H	L	L	H	H	L	H	H
H	L	H	L	H	H	L	H
H	L	H	H	H	H	H	L

$\overline{CASO}$ FUNCTION TABLE

$\overline{RFSH}$	$\overline{CASI}$	$\overline{CASO}$
H	L	L
H	H	H
L	X	H

ADDRESS OUTPUT FUNCTION TABLE

MSEL	$\overline{RFSH}$	0_0-0_7
H	H	A_0-A_7
L	H	A_8-A_{15}
X	L	Refresh Address

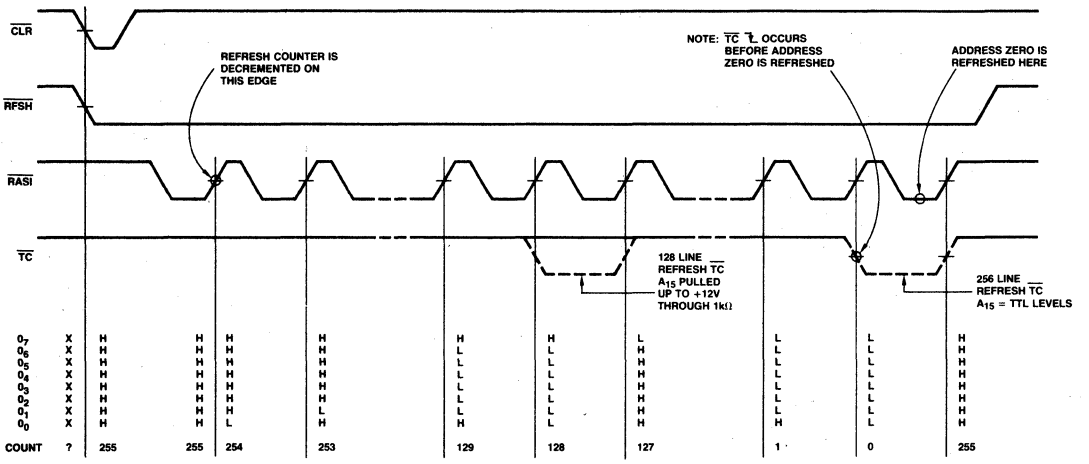
REFRESH ADDRESS COUNTER FUNCTION TABLE

A_{15}	$\overline{CLR}$	$\overline{RFSH}$	$\overline{RASI}$	$\overline{TC}$	REFRESH COUNT	FUNCTION
X	L	X	X	X	FF_H	Clear Counter
X	H	↓	X	X	NC	Output Refresh Address No Change for Counter
X	H	↓	L	X	Count − 1	Return to Memory Cycle Mode and Decrement Counter
X	H	L	↓	X	NC	Output all RAS_i to RAM No Change for Counter
X	H	L	↓	X	Count − 1	Return RAS_i to HIGH and Decrement Counter
L or H	H	X	X	L	00_H	Terminal Count for 256 Line Refresh
+12V*	H	X	X	L	00_H and 80_H	Terminal Count for 128 Line Refresh

*Through 1 kΩ resistor.

4

BURST REFRESH TIMING



The timing shown assumes that burst mode applications may power-down the Am2964B with the RAM. Therefore the counter is cleared prior to executing the refresh sequence.

APPLICATION

ARCHITECTURE

The Dynamic Memory Controller (DMC) provides address multiplexing, refresh address generation and $\overline{RAS}/\overline{CAS}$ control for the MOS dynamic RAM memories of any data width. The eight bit address path is designed for 64K RAMs and can be used with 16K RAMs.

Sixteen address input latches and two $\overline{RAS}$ Select latches (for higher order addresses) allow the DMC to control up to 256K words of memory (with 64K RAMs) by using the internal $\overline{RAS}$ decoder to select from one-of-four banks of RAMs.

SPEED WITH MINIMUM SKEW

The DMC provides Schottky speed in all of the critical paths. In addition, time skew between the Address, $\overline{RAS}$ and $\overline{CAS}$ paths is minimized (and specified) by placing these functions on the same chip. The inclusion of the $\overline{CAS}$ buffer allows matching of its propagation delay, plus provides the $\overline{CAS}$ inhibit function during $\overline{RAS}$ – only refresh.

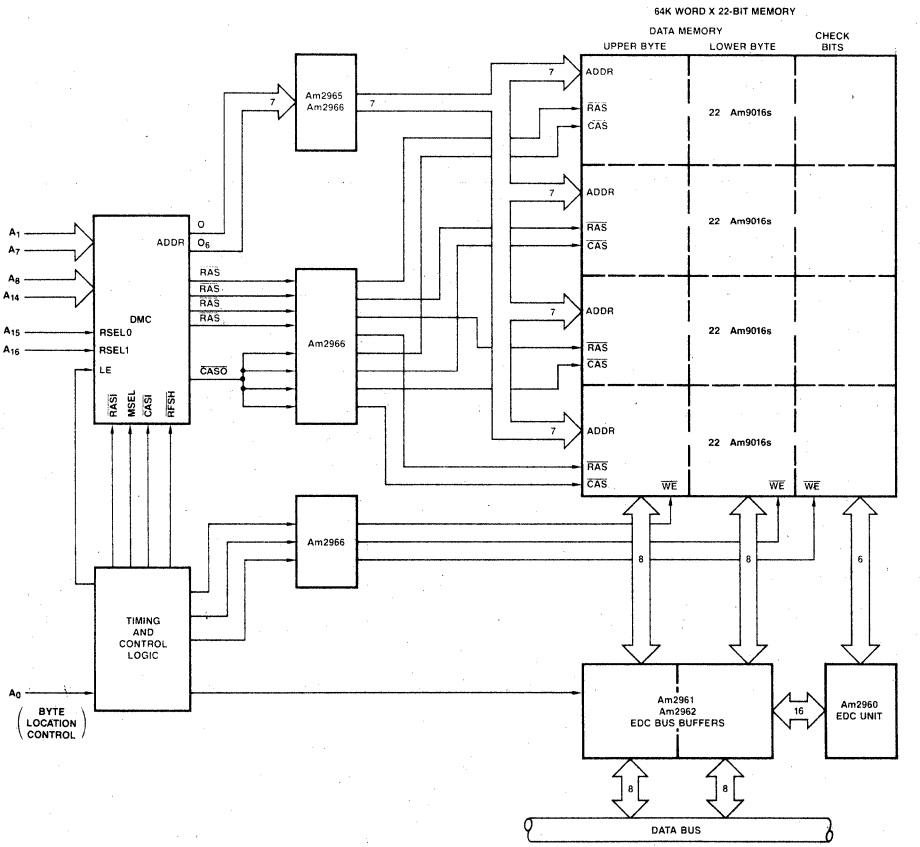
INPUT LATCHES

The eighteen input latches are transparent when LE is HIGH and latch the input data meeting set-up and hold time requirements when LE goes LOW. In systems with separate address and data buses, LE may be permanently enabled HIGH.

REFRESH COUNTER

The 8-bit refresh counter provides both 128 and 256 line refresh capability. Refresh control is external to allow maximum user flexibility. Transparent (hidden), burst, synchronous or asynchronous refresh modes are all possible.

The refresh counter is advanced at the LOW-to-HIGH transition of $\overline{RFSH}$ (or $\overline{RASI}$). This assures a stable counter output for the next refresh cycle. The counter will continue to cycle through 256 addresses unless reset to zero by $\overline{CLR}$. This actually causes all outputs to go HIGH since the output MUX is inverting. (Address inputs to outputs are non-inverting since both the input latches and output MUX are inverting).



*Address and $\overline{RAS}/\overline{CAS}$ drivers each drive 22 RAM inputs at each output. Timing skew is minimized by using one device for address lines and one device for $\overline{RAS}/\overline{CAS}$, spreading the $\overline{CAS}$ loading over four drivers to equalize the capacitive load on each driver.

Figure 1. Dynamic Memory Control with Error Detection and Correction

REFRESH TERMINAL COUNT

The refresh counter also provides a Terminal Count output for burst mode refresh applications. $\overline{TC}$ normally occurs at count 255 (0_0 to 0_7 all LOW when $\overline{RFSH}$ is LOW). $\overline{TC}$ can be made to occur at count 127 for 128 line burst mode refresh by pulling A_{15} up to +12V through a 1KΩ ± 10% resistor. The counter actually cycles through 256 with $\overline{TC}$ determined by A_{15}. Otherwise A_{15} functions as an address input when driven at normal TTL levels.

THREE INPUT 8-BIT ADDRESS MULTIPLEXER

The address MUX is 8-bits wide (for 64K RAMs) and has three data sources, the lower address input latch (A_0 to A_7), the upper address input latch (A_8 to A_{15}) and the internal refresh counter. The lower address latch is selected when MSEL is HIGH. This is normally the Row address. The upper address latch is selected when MSEL is LOW. This is normally the Column address. The third source – the refresh counter is selected when $\overline{RFSH}$ is LOW and overrides MSEL.

When $\overline{RFSH}$ goes LOW, the MUX selects the refresh counter address and $\overline{CASO}$ is inhibited. Also, the $\overline{RAS}$ Decoder function is changed from one-of-four to four-of-four so all $\overline{RAS}$ outputs $\overline{RAS_0}$-$\overline{RAS_3}$ go LOW to refresh all banks of memory when $\overline{RASI}$ goes LOW. When RFSH is HIGH only one $\overline{RAS}$ output goes low, determined by the $\overline{RAS}$ Select inputs, $RSEL_0$ and $RSEL_1$. In either case the $\overline{RAS}$ Decoder output timing is controlled by $\overline{RASI}$ to make sure the refresh count appears at 0_0-0_7 before $\overline{RAS_0}$-$\overline{RAS_3}$ go LOW. This assures meeting Row address Set-up time requirement of the RAM (t_{ASR}).

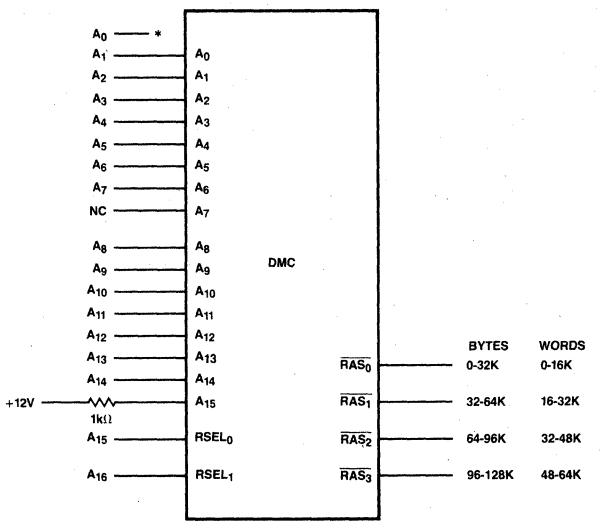
MAXIMUM PERFORMANCE SYSTEM

The typical organization of a maximum performance 16-bit system including Error Detection and Correction is shown in Figure 1. Delay lines provide the most accurate timing and are recommended for $\overline{RAS}$/MSEL/$\overline{CAS}$ timing in this type of system.

CONTROLLING 16K RAMS OR SMALLER SYSTEMS

16K RAMs require seven address inputs and 128 line refresh. Also, A_0 is often used to designate upper or lower byte trans actions in 16-bit systems. These modifications are shown in Figure 2.

4



*A_0 Controls Byte Select Logic

Figure 2. Word Organized Memory Using 16K RAMs

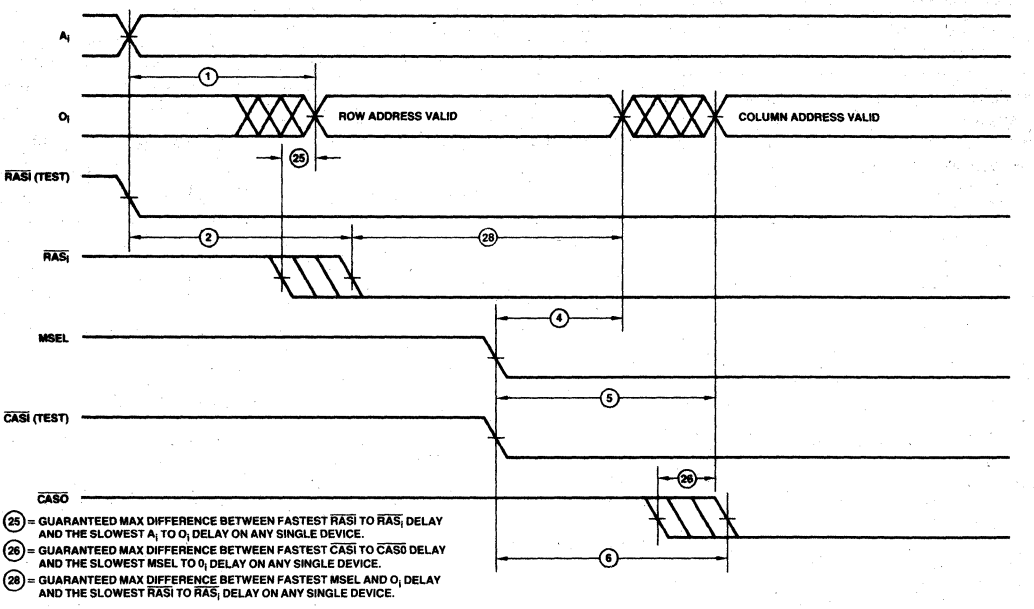
MEMORY CYCLE TIMING

The relationship between DMC specifications and system timing requirements are shown in Figure 3. T_1, T_2 and T_3 represent the minimum timing requirements at the DMC inputs to guarantee that RAM timing requirements are met and that maximum system performance is achieved.

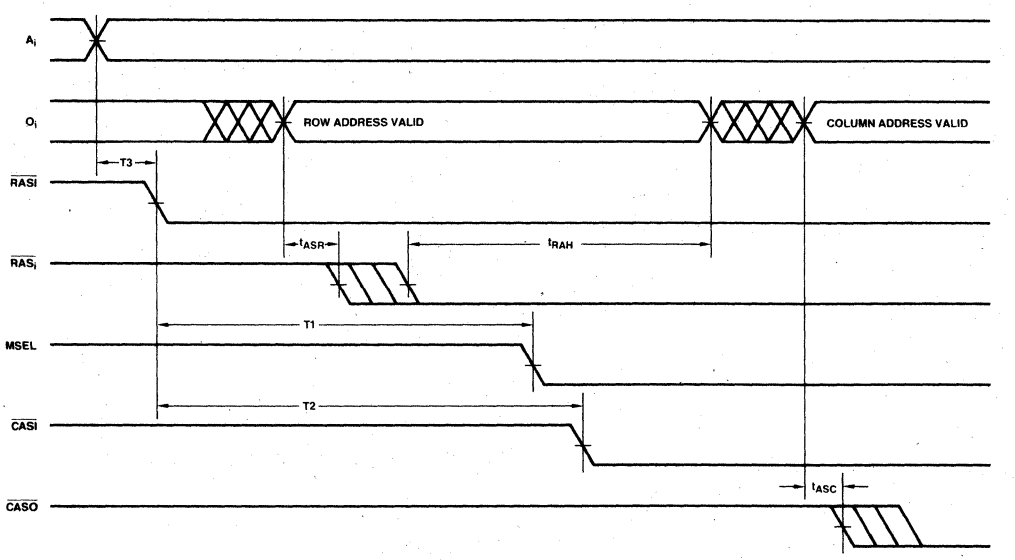
The minimum requirement for T_1, T_2, and T_3 are as follows:

$T_1MIN = t_{RAH} + t_{28}$
$T_2MIN = T_1 + t_{26} + t_{ASC}$
$T_3MIN = t_{ASR} + t_{25}$

See RAM data sheet for applicable values for t_{RAH}, t_{ASC} and t_{ASR}.



a) Specifications Applicable to Memory Cycle Timing



b) Desired System Timing

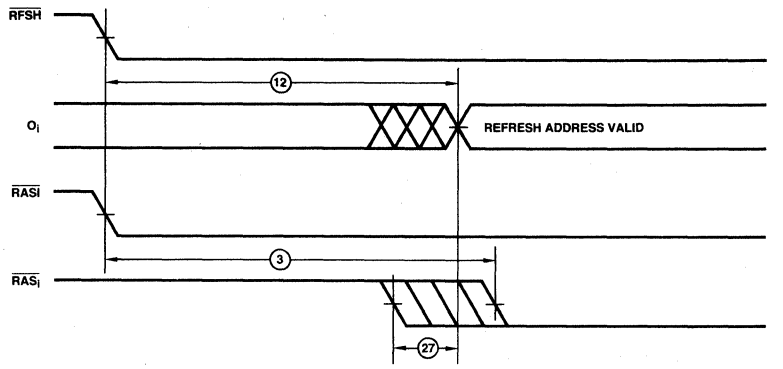
Figure 3. Memory Cycle Timing

REFRESH CYCLE TIMING

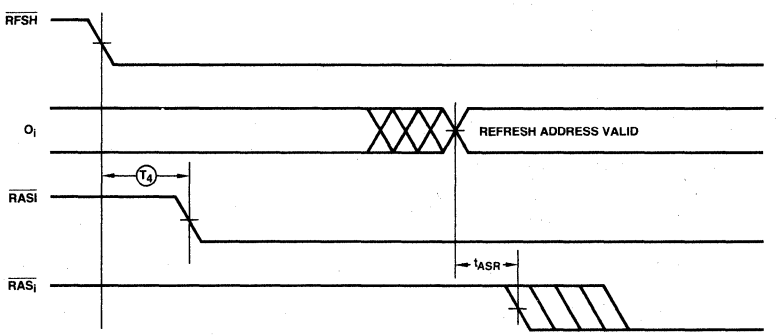
The timing relationships for refresh are shown in Figure 4.

T_4 minimum is calculated as follows:

$$T_4 = t_{ASR} + t_{27}$$



a) Test Waveforms

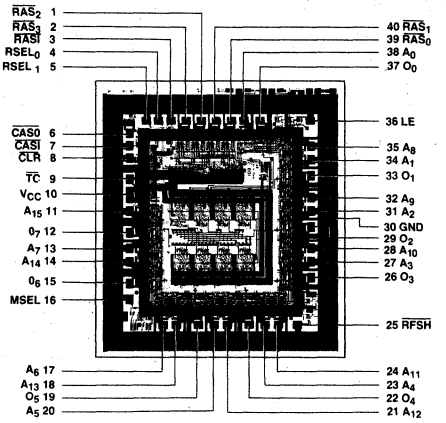


(27) = GUARANTEED MAX DIFFERENCE BETWEEN FASTEST $\overline{RASI}$ TO $\overline{RAS}_i$ DELAY AND SLOWEST $\overline{RFSH}$ TO O_i DELAY ON ANY SINGLE DEVICE.

b) Desired System Timing

Figure 4. Refresh Timing

Metallization and Pad Layout



DIE SIZE 0.156" X 0.143"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2964B Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2964BPC	P-40	C	C-1
AM2964BDC	D-40	C	C-1
AM2964BDC-B	D-40	C	B-2 (Note 4)
AM2964BDM	D-40	M	C-3
AM2964BDM-B	D-40	M	B-3
AM2964BLC	L-44	C	C-1
AM2964BLM	L-44	M	C-1
AM2964BLM-B	L-44	M	B-3
AM2964BXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2964BXM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = −55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

This device is also characterized as:
AmZ8165
AmZ8166

Am2965 • Am2966

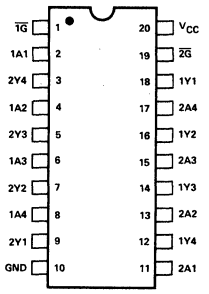
Octal Dynamic Memory Drivers with Three-State Outputs

4

DISTINCTIVE CHARACTERISTICS

- **Controlled rise and fall characteristics**
  Internal resistors provide symmetrical drive to HIGH and LOW states, eliminating need for external series resistor.
- **Output swings designed to drive 16K and 64K RAMs**
  V_{OH} guaranteed at V_{CC} −1.15V. Undershoot going LOW guaranteed at less than 0.5V.
- **Large capacitive drive capability**
  35mA min source or sink current at 2.0V. Propagation delays specified for 50pF and 500pF loads.
- **Pin-compatible with 'S240 and 'S244**
  Non-inverting Am2966 replaces 74S244; inverting Am2965 replaces 74S240. Faster than 'S240/244 under equivalent load.
- **No-glitch outputs**
  Outputs forced into OFF state during power up and down. No glitch coming out of three-state.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BLI-125

FUNCTIONAL DESCRIPTION

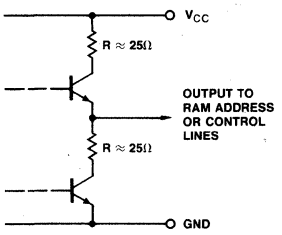
The Am2965 and Am2966 are designed and specified to drive the capacitive input characteristics of the address and control lines of MOS dynamic RAMs. The unique design of the lower output driver includes a collector resistor to control undershoot on the HIGH-to-LOW transition. The upper output driver pulls up to V_{CC} − 1.15V to be compatible with MOS memory and is designed to have a rise time symmetrical with the lower output's controlled fall time. This allows optimization of Dynamic RAM performance.

The Am2965 and Am2966 are pin-compatible with the popular 'S240 and 'S244 with identical 3-state output enable controls. The Am2965 has inverting drivers and the Am2966 has non-inverting drivers.

The inclusion of an internal resistor in the lower output driver eliminates the requirement for an external series resistor, therefore reducing package count and the board area required. The internal resistor controls the output fall and undershoot without slowing the output rise.

These devices are designed for use with the Am2964 Dynamic Memory Controller where large dynamic memories with highly capacitive input lines require additional buffering. Driving eight address lines or four $\overline{RAS}$ and four $\overline{CAS}$ lines with drivers on the same silicon chip also provides a significant performance advantage by minimizing skew between drivers. Each device has specified skew between drivers to improve the memory access worst case timing over the min and max t_{PD} difference of unspecified devices.

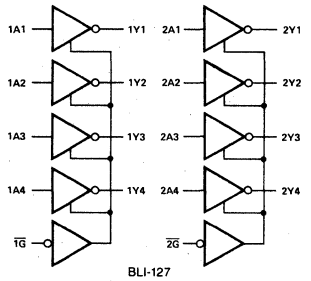
TYPICAL OUTPUT DRIVER



BLI-126

LOGIC DIAGRAMS

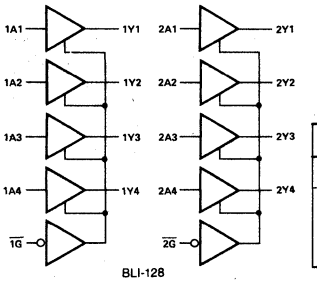
Am2965



BLI-127

Inputs		Outputs
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

Am2966



BLI-128

Inputs		Outputs
$\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5 to +7.0V
DC Output Current, into Outputs	200mA
DC Input Current	−30 to +5.0mA

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

Am2965/66XC, DC, PC	T_A = 0 to 70°C	V_{CC} = 5.0V ±10%	(MIN = 4.50V MAX = 5.50V)
Am2965/66XM, DM	T_A = −55 to +125°C	V_{CC} = 5.0V ±10%	(MIN = 4.50V MAX = 5.50V)
Am2965/66FM	T_C = −55 to +125°C	V_{CC} = 5.0V ±10%	(MIN = 4.50V MAX = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description		Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output High Voltage		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1mA	V_{CC}−1.15	V_{CC}−0.7V		Volts
V_{OL}	Output LOW Voltage		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 1mA			0.5	Volts
				I_{OL} = 12mA			0.8	
V_{IH}	Input HIGH Level		Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level		Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage		V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current		V_{CC} = MAX, V_{IN} = 0.4V	DATA			−200	μA
				$\overline{1G}$, $\overline{2G}$			−400	
I_{IH}	Input HIGH Current		V_{CC} = MAX, V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current		V_{CC} = MAX, V_{IN} = 7.0V				0.1	mA
I_{OZH}	Off-State Current		V_O = 2.7V				100	μA
I_{OZL}	Off-State Current		V_O = 0.4V				−200	μA
I_{OL}	Output Sink Current		V_{OL} = 2.0V		50			mA
I_{OH}	Output Source Current		V_{OH} = 2.0V		−35			mA
I_{SC}	Output Short Circuit Current (Note 3)		V_{CC} = MAX		−60 (see I_{OH})		−200	mA
I_{CC}	Supply Current	Am2965	All Outputs HIGH	V_{CC} = MAX Outputs Open		24	50	mA
			All Outputs LOW			86	125	
			All Outputs Hi-Z			86	125	
		Am2966	All Outputs HIGH	V_{CC} = MAX Outputs Open		53	75	
			All Outputs LOW			92	130	
			All Outputs Hi-Z			116	150	

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Am2965 • Am2966
SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time from LOW-to-HIGH Output	Figure 1 Test Circuit Figure 3 Voltage Levels and Waveforms	C_L = 0pF		6	(Note 4)	ns
			C_L = 50pF	6	9	15	
			C_L = 500pF	18	22	30	
t_{PHL}	Propagation Delay Time from HIGH-to-LOW Output		C_L = 0pF		4	(Note 4)	ns
			C_L = 50pF	5	7	15	
			C_L = 500pF	18	22	30	
t_{PLZ}	Output Disable Time from LOW, HIGH	Figures 2 and 4, S = 1			11	20	ns
t_{PHZ}		Figures 2 and 4, S = 2			6.5	12	
t_{PZL}	Output Enable Time from LOW, HIGH	Figures 2 and 4, S = 1			12	20	ns
t_{PZH}		Figures 2 and 4, S = 2			12	20	
t_{SKEW}	Output-to-Output Skew	Figures 1 and 3, C_L = 50pF			±0.5	±3.0 (Note 5)	ns
V_{ONP}	Output Voltage Undershoot	Figures 1 and 3, C_L = 50pF			0	−0.5	Volts

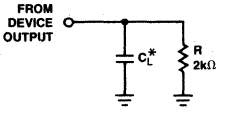
4

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Note 6)

Parameters	Description	Test Conditions		COM'L T_A = 0 to 70°C V_{CC} = 5.0V ±10% Min	COM'L Max	MIL (Note 7) T_A = −55 to +125°C V_{CC} = 5.0V ±10% Min	MIL Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Output	Figures 1 and 3	C_L = 50pF	4	17	4	20	ns
			C_L = 500pF	18	35	18	40	
t_{PHL}	Propagation Delay Time HIGH-to-LOW Output	Figures 1 and 3	C_L = 50pF	4	17	4	20	ns
			C_L = 500pF	18	35	18	40	
t_{PLZ}	Output Disable Time from LOW, HIGH	Figures 2 and 4	S = 1		24		24	ns
t_{PHZ}			S = 2		16		16	
t_{PZL}	Output Enable Time from LOW, HIGH	Figures 2 and 4	S = 1		28		28	ns
t_{PZH}			S = 2		28		28	
V_{ONP}	Output Voltage Undershoot	Figures 1 and 3, C_L = 50pF			−0.5		−0.5	Volts

Notes: 4. Typical time shown for reference only – not tested.
5. Time Skew specification is guaranteed by design but not tested.
6. AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.
7. T_C = −55 to +125°C for Flatpak versions.

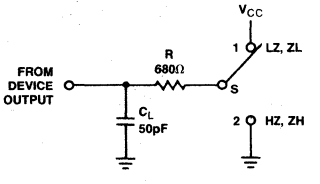
SWITCHING TEST CIRCUITS



BLI-129

*t_{pd} specified at C = 50 and 500pF.

Figure 1. Capacitive Load Switching.

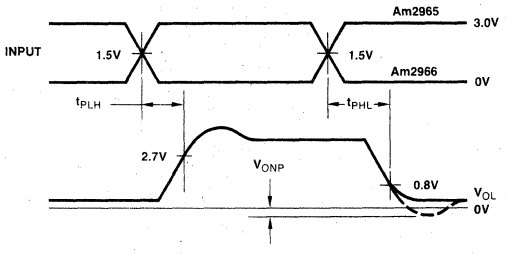


BLI-130

Figure 2. Three-State Enable/Disable.

TYPICAL SWITCHING CHARACTERISTICS

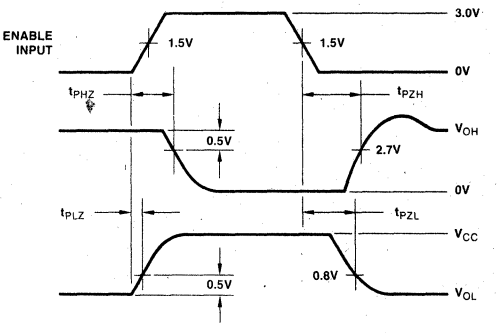
VOLTAGE WAVEFORMS



BLI-131

$t_r = t_f = 2.5ns$
f = 2.5MHz
$t_{pw} = 200ns$

Figure 3. Output Drive Levels.



BLI-132

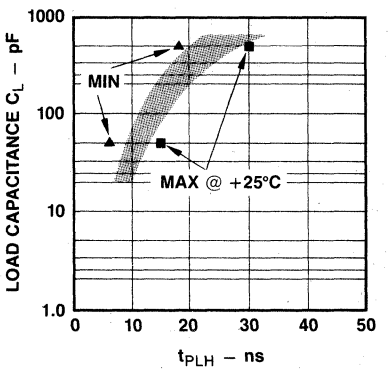
$t_r = t_f = 2.5ns$
f = 1MHz
$t_{pw} = 800ns$

Figure 4. Three-State Control Levels.

The RAM Driver symmetrical output design offers significant improvement over a standard Schottky output by providing a balanced drive output impedance (≈25Ω both HIGH and LOW), and by pulling up to MOS V_{OH} levels (V_{CC} − 1.5V). External resistors, not required with the RAM Driver, protect standard Schottky drivers from error causing undershoot but also slow the output rise by adding to the internal R.

The RAM Driver is optimized to drive LOW at maximum speed based on safe undershoot control and to drive HIGH with a symmetrical speed characteristic. This is an optimum approach because the dominant RAM loading characteristic is input capacitance.

The curves shown below provide performance characteristics typical of both the inverting (Am2965) and non-inverting (Am2966) RAM Drivers.



BLI-133

Figure 5. t_{PLH} for V_{OH} = 2.7 Volts vs. C_L.

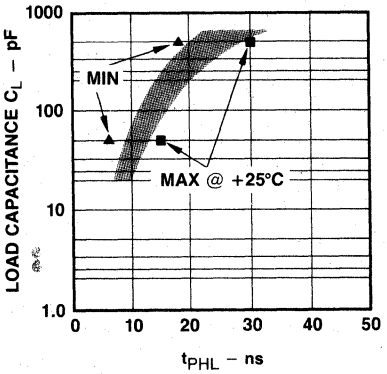
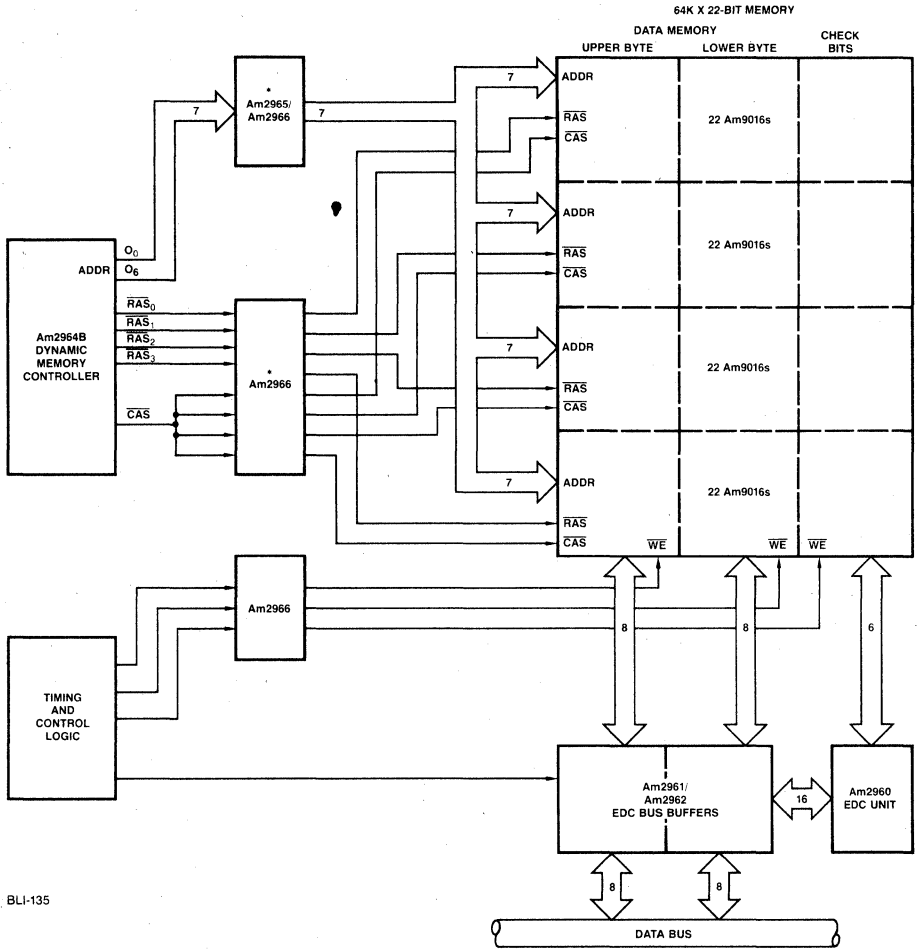


Figure 6. t_{PHL} for V_{OL} = 0.8 Volts vs. C_L.

The curves above depict the typical tPLH and tPHL for the RAM Driver outputs as a function of load capacitance. The minimums and maximums are shown for worst case design. The typical band is provided as a guide for intermediate capacitive loads.

APPLICATION

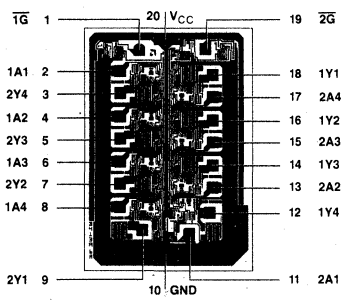


*Address and $\overline{RAS}/\overline{CAS}$ drivers each drive 22 RAM inputs at each output. Timing skew is minimized by using one device for address lines and one device for $\overline{RAS}/\overline{CAS}$, spreading the $\overline{CAS}$ loading over four drivers to equalize the capacitive load on each driver.

DYNAMIC MEMORY CONTROL WITH ERROR DETECTION AND CORRECTION

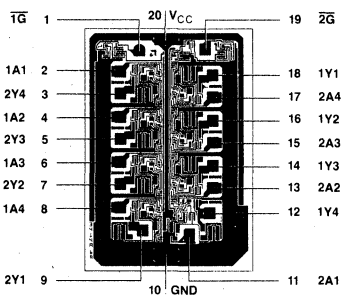
Metallization and Pad Layouts

Am2965



DIE SIZE 0.094" X 0.060"

Am2966



DIE SIZE 0.094" X 0.066"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2965 Order Number	Am2966 Order Number	Package Type	Temperature Range	Screening Level
AM2965PC	AM2966PC	P-20	C	C-1
AM2965DC	AM2966DC	D-20	C	C-1
AM2965DCB	AM2966DCB	D-20	C	B-1
AM2965DM	AM2966DM	D-20	M	C-3
AM2965DMB	AM2966DMB	D-20	M	B-3
AM2965FM	AM2966FM	F-20	M	C-3
AM2965FMB	AM2966FMB	F-20	M	B-3
AM2965XC	AM2966XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2965XM	AM2966XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flatpak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless othewise specified.
2. C = 0 to 70°C, V_{CC} = 4.50V to 5.50V, M = −55 to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am2965 • Am2966

Dynamic Memory Drivers Improve Memory Performance

By John Mick and Roy Levy

OVERVIEW

The Am2965 and Am2966 are bipolar octal drivers for 16K and 64K dynamic RAMs. The devices offer a guaranteed maximum undershoot of −0.5V without requiring external resistors. The Am2965 and Am2966 feature a t_{PD} minimum and maximum specified at 50pF and 500pF. The V_{OH} is guaranteed at V_{CC} −1.15V minimum, and I_{OH} and I_{OL} are specified at +2.0V for minimum guarantee of charging capacitance. There are glitch-free three-state outputs during power-up and power-down as well as symmetrical, controlled rise time and fall time.

While the Am2965 and Am2966 have low-power Schottky input characteristics and are pin-compatible replacement for design using the 'S240 and 'S244 (plus external resistors), the Am2965/2966 offer improved performance. The cost of the components is also comparable to Schottky buffer/external resistor systems.

To assure product quality, the Am2965 and Am2966 are specified for COM'L and MIL-STD-883.

INTRODUCTION

In the past, memory system designers have used Schottky devices such as the Am74S240 or Am74S244 to drive the highly capacitive inputs of MOS Dynamic RAMs. However, because of the distributed inductance and distributed capacitance associated with many dynamic RAMs on printed circuit board, resistors are usually placed in series with the Schottky TTL outputs to minimize undershoot and dampen the ringing that occurs when driving the inductive/capacitive load.

To achieve maximum performance in today's memory systems, the designer should use the Am2965 or the Am2966 to drive large arrays of MOS Dynamic RAMs. These devices increase system speed by providing high-capacity drive and optimizing the drive characteristic time constant. They provide a new system solution for solving these problems that eliminates the external resistor and guarantees the maximum undershoot will not exceed −0.5V.

The address lines on most dynamic RAMs are specified at 5pF maximum while the $\overline{RAS}$, write enable ($\overline{WE}$) and $\overline{CAS}$ inputs can be as high as 10pF. Thus the RAM driver's output must drive extremely high capacitive levels with good speed and without undershoot. When several dynamic RAMs are put onto a printed circuit board, the traces look inductive, so the result resembles a transmission line with distributed inductance and capacitance.

More than 0.5V of undershoot at the RAM inputs can create serious memory system problems by causing internal breakdown and loss of data in RAM chips and possibly damaging the RAM.

System designers must also maintain voltage levels at the RAM inputs. Specifications require the data lines to exceed 2.4V, and the $\overline{RAS}$ and $\overline{CAS}$ lines actually have to exceed 2.7V. Speed must then be maintained while driving all of that capacity.

THE RAM DRIVING PROBLEM

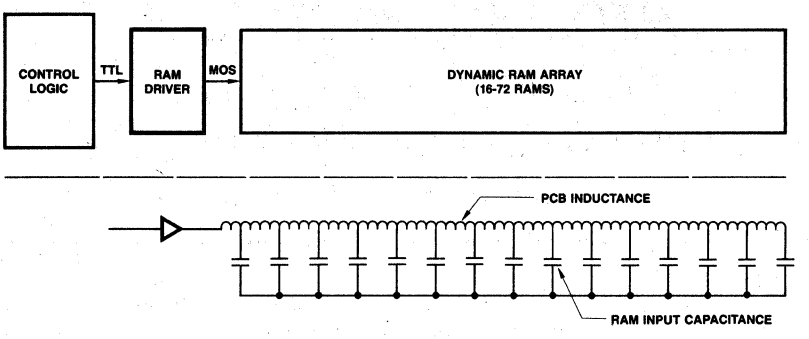
The situation can be pinpointed to an inductor/capacitance driving problem (Figure 1a). There is some inductance in series with the capacitance associated with each RAM input. In a simplified circuit, the inductance is being driven from a voltage having source impedance marked as R_S on Figure 1b. If the transition is LOW-to-HIGH, the voltage goes from LOW-to-HIGH with ringing at the HIGH state (Figure 2). Only above the 2.7V or 2.4V levels, depending upon the type of input, can a steady-state HIGH level be guaranteed on the RAM input. The rise time of the signal is a design consideration, recognizing the amount of capacitance being driven.

Conversely, when the signal drops from HIGH-to-LOW again, ringing can occur. If the ringing causes the voltage to go below ground, it is called undershoot. Figure 3a shows the signal falling to zero volts more quickly than the signal in Fig. 3b, resulting in a severe undershoot that takes longer to settle at the LOW steady state voltage. This delay time associated with the RC time constant is independent of the specification for the HIGH-to-LOW propagation delay time, t_{PHL}. It is a hidden delay that must be compensated for.

VOLTAGE SWING CONSIDERATIONS

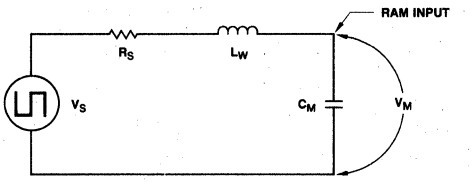
Recognizing that some ringing will occur, the system designer must determine how quickly the signal can be stabilized within the threshold limits of 0.5V below ground and 0.8V above ground. The best way to predict what happens with overshoot and undershoot is to examine the method of driving RAMs. Typically, it is done using one of several Schottky TTL devices connected directly to the RAM. Figure 4a shows an output transistor/resistor structure of a Schottky TTL device. When Q_1 is off and Q_2 is on, the LOW source impedance is about 3 ohms. When Q_2 is off and Q_1 is on, the HIGH impedance is that of the Q_1 transistor and the short circuit R_1. R_1 typically represents about 30-ohm source impedance, so that the source impedance HIGH and source impedance LOW represent a 10-to-1 difference with respect to each other (Figure 4b).

Other TTL devices can be driven in this way, but it is unacceptable for driving RAMs with this type of source impedance for several reasons. First, low source impedance in the LOW states causes ringing by turning on so fast that undershoot results at the RAM inputs. The impedance, however, drives well in the HIGH state. However, to solve the HIGH-to-LOW transition and undershoot problems a resistor is usually placed in series externally between the Schottky TTL gate and the RAM (Figure 4c). The resistor, of about 30 ohms, virtually eliminates undershoot by raising the source impedance in the LOW state to 33 ohms (Q_1 plus R_2).



Objective: Drive the load
- Avoid undershoot
- At MOS voltage levels
- Faster than Schottky

a) The RAM Driver Interface



V_S = the signal driving the chip
R_S = the output resistance of the driving source
L_W = the inductance of the circuit wiring between driving source and memory
C_M = input capacitance of memory chip
V_M = input signal to memory and voltage developed across capacitor

b) Model of Circuit Driving a Memory Chip

Figure 1.

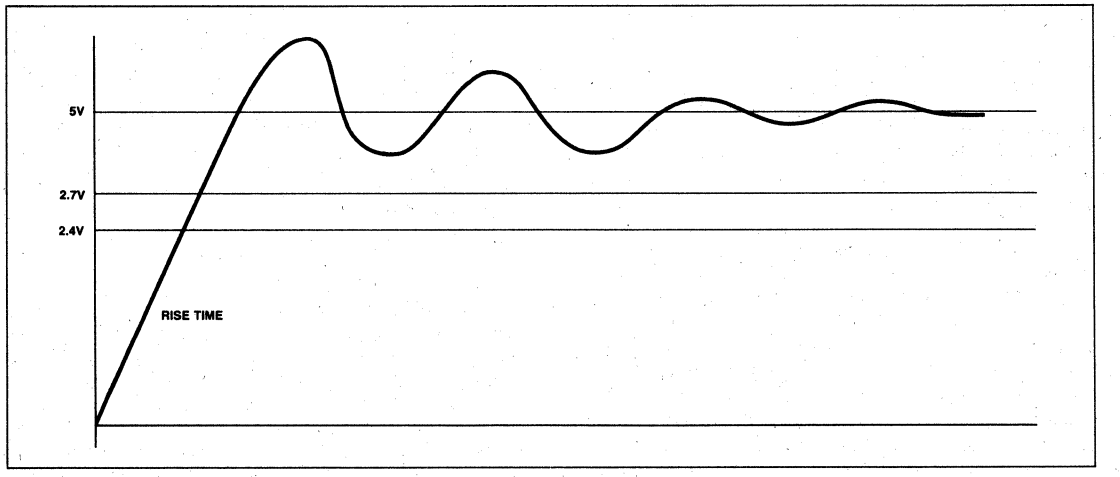


Figure 2. Overshoot in a Rising Signal

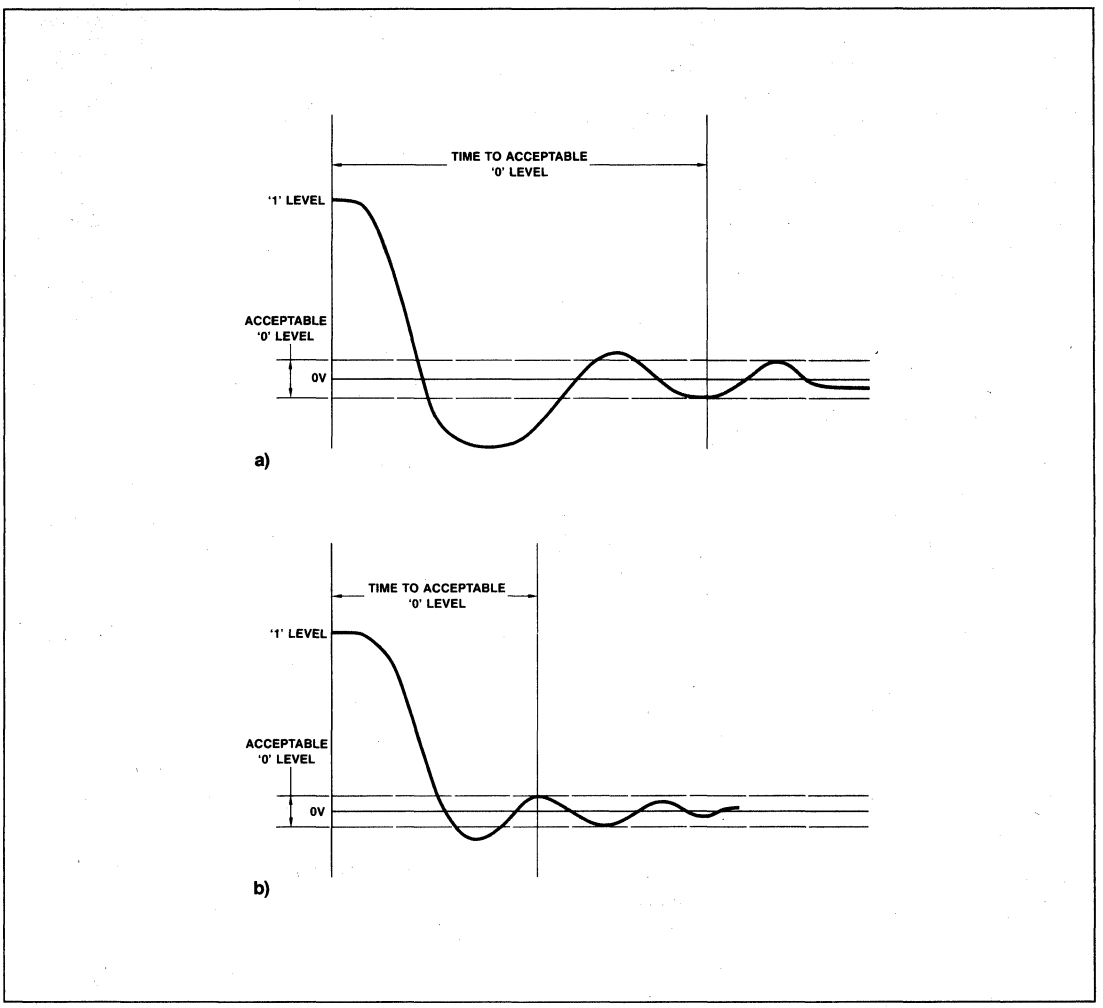


Figure 3. Undershoot in Falling Signals

When the HIGH state is turned on, the 30-ohm external resistor added to the 30-ohm terminal resistor in series totals 60 ohms of source impedance – an amount double of what is needed. While adding the external resistor in series solves undershoot, it causes the rise time (i.e., LOW-to-HIGH transition) to be slowed considerably – probably by a factor of two because resistance is doubled, so the RC time constant is doubled.

The ideal RAM driver source impedance is about 30 ohms in the HIGH state and 20 to 30 ohms in the LOW state (Figure 4d). The Am2965/2966 achieves the ideal RAM driver configuration by having approximately a 20- to 25-ohm source impedance in the LOW state and 25- to 30-ohm source impedance in the HIGH state. This ideal configuration is achieved by including a resistor (R_2) inside the Am2965/66 in series with the collector of Q_2. R_2 adds approximately a 15- to 20-ohm series resistance that has a source impedance in the LOW state of about 20 to 25 ohms and a source impedance in the HIGH state of about 25 to 30 ohms.

Remember, these figures are very nearly what was previously defined as the ideal RAM driver. What results is $R_1 + Q_1$ equivalent resistance in the HIGH state and $R_2 + Q_2$ resistance in the LOW state. The AMD family of RAM driver parts places the resistor inside and only increases the source impedance in the LOW state to achieve the ideal RAM driver configuration shown in Figures 4d and 4e. Now no resistor is needed outside the RAM driver as is typically used with today's Schottky devices.

APPLICATION

Figures 5a and 5b show typical overall memory subsystems for AmZ8000 and 2900 Family CPUs. The subsystems consist of the RAM drivers surrounding the RAMs almost directly; a dynamic memory controller; and interface, timing and controls required to drive the RAMS. There may also be an error detection and correction device as the figure shows.

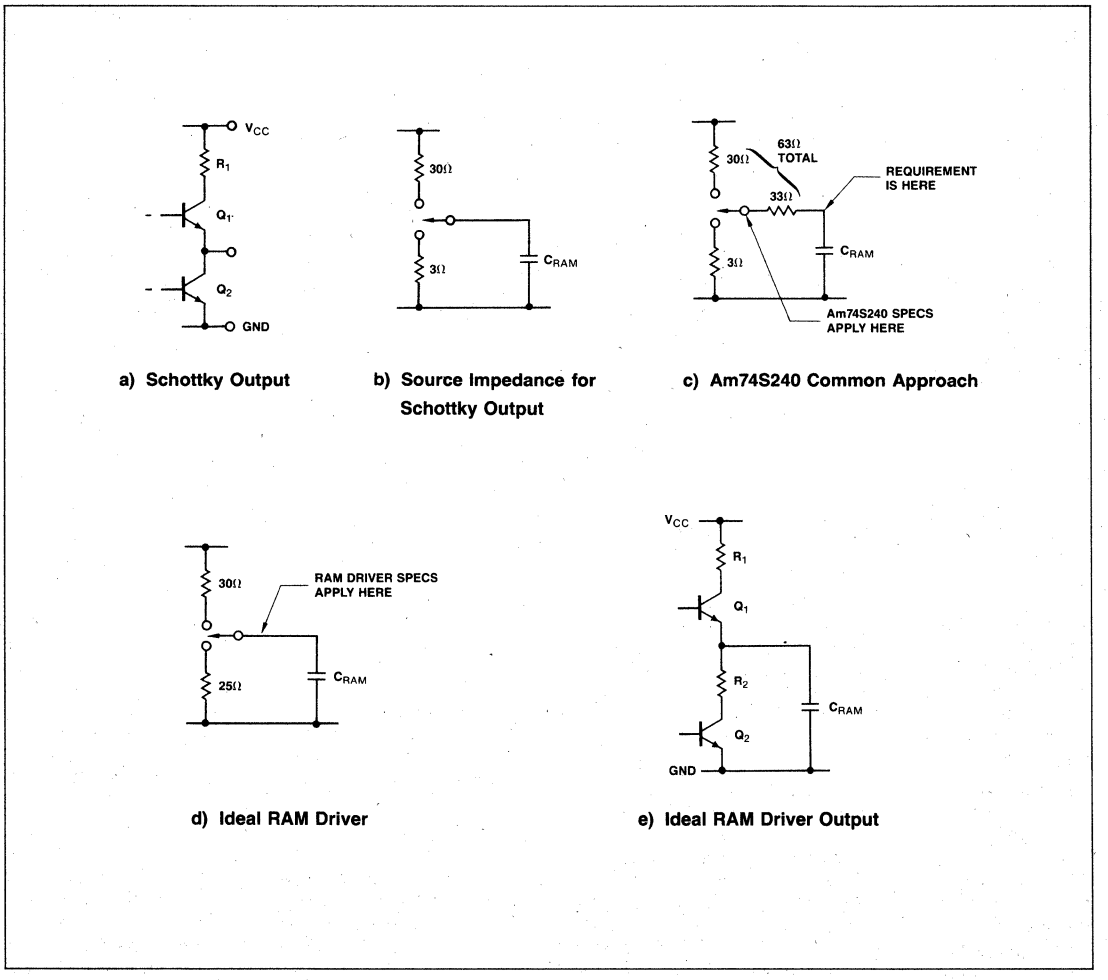
The objective of the memory subsystem is to drive the capacitive RAM inputs as rapidly as possible while meeting all the requirements for the undershoot and threshold levels. Figure 6 shows typical locations for RAM drivers to achieve this goal. Since a majority of the propagation delay times is an RC consideration, design flexibility allows the number of RAM input loads to be chosen for each RAM driver output. The best tradeoff includes fan-out choice and skew consideration. The skew specification for the Am2965 and Am2966 applies across the eight driver outputs but not between different devices.

The memory configuration of Figure 6 consists of an array of four rows by 16 columns of dynamic RAM chips for a total of 64 devices (Figure 7). The address drivers in Figure 6 have 16 x 4 x 5pF maximum = 320 pF (ignoring board capacitance) loading if one RAM driver drives all 64 RAM address inputs. Splitting this load with two RAM drivers reduces the capacitive load for each to 160pF and typically reduces the t_{PD} by 6 to 8nsec.

One of the unique aspects of the design in Figure 7 is the balanced number of loads on the $\overline{RAS}$ outputs of the RAM drivers and the number on loads of the $\overline{CAS}$ outputs of the RAM drivers.

Each driver drives the same number of RAMs. To balance the $\overline{CAS}$ line, the $\overline{CAS}$ inputs of four of the eight buffers are tied together on the RAM driver. Each RAM $\overline{RAS}$ and $\overline{CAS}$ input is 10pF maximum, so the $\overline{RAS}$ and $\overline{CAS}$ loading is 160pF at each RAM driver. The $\overline{CAS}$ inputs of each row are spread across four outputs to match the RAS loading and are shown using the same driver to reduce skew between the $\overline{RAS}$ and the $\overline{CAS}$ signals. The $\overline{WE}$ inputs are organized into upper and lower byte $\overline{WE}$ drive for each of the four rows. This amounts to 8 inputs x 10pF maximum = 80pF loading. By fanning out a full driver to the $\overline{WE}$ lines, four inputs are tied in parallel, balanced loading on the outputs are maintained.

If a full error detection and correction scheme shown in Figure 5 is used, all 22 bits in the row must be written simultaneously so a slightly different $\overline{WE}$ configuration would be used.



a) Schottky Output

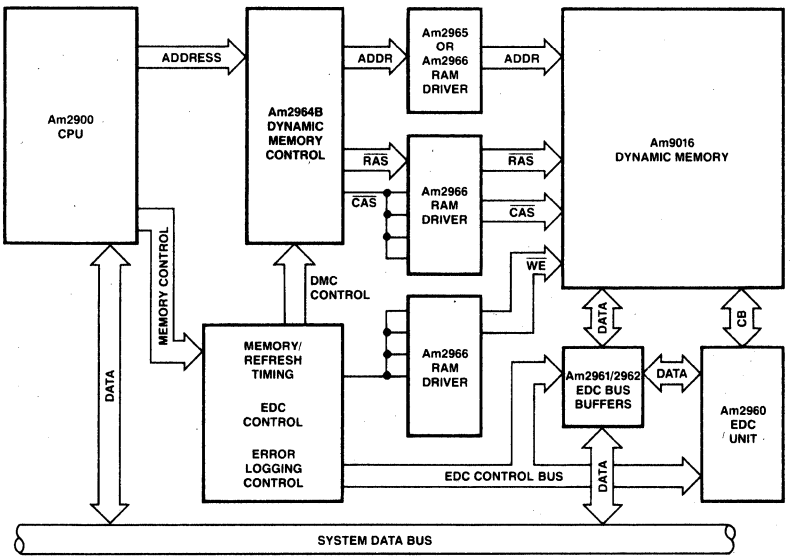
b) Source Impedance for Schottky Output

c) Am74S240 Common Approach

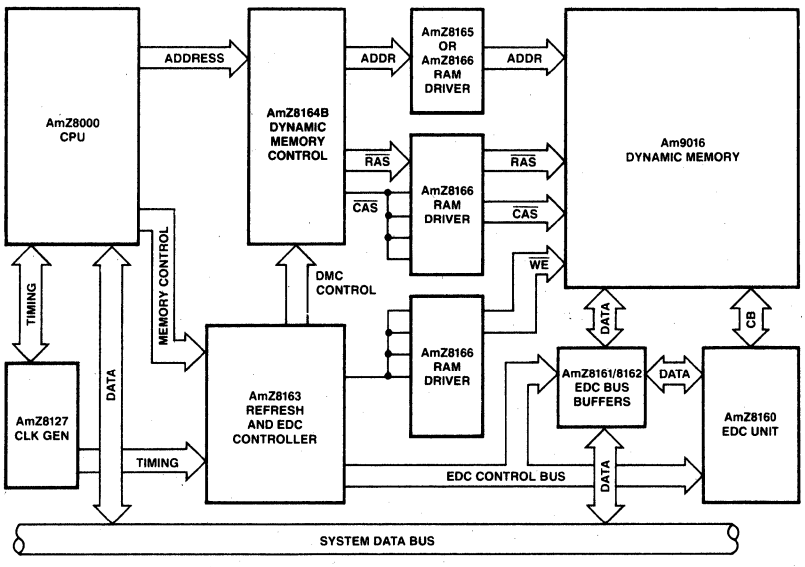
d) Ideal RAM Driver

e) Ideal RAM Driver Output

Figure 4. RAM Drivers vs. Schottky Output



a) High Performance Computer Memory



b) MOS Microcomputer Memory System

Figure 5. Overall Memory Subsystems for the Am2900 and AmZ8000 Family CPUs

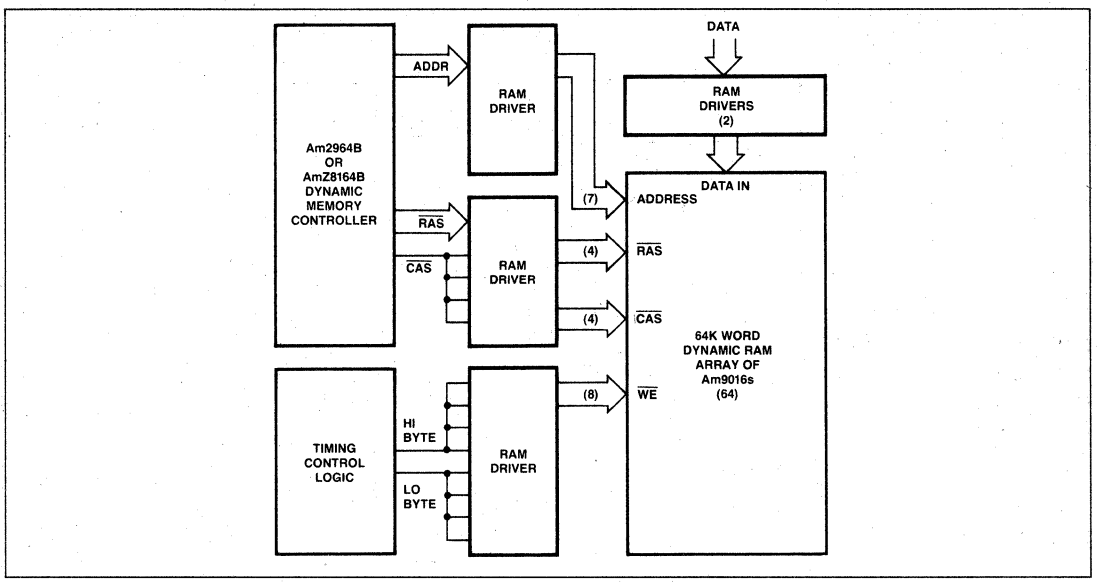


Figure 6. Typical Locations for RAM Drivers

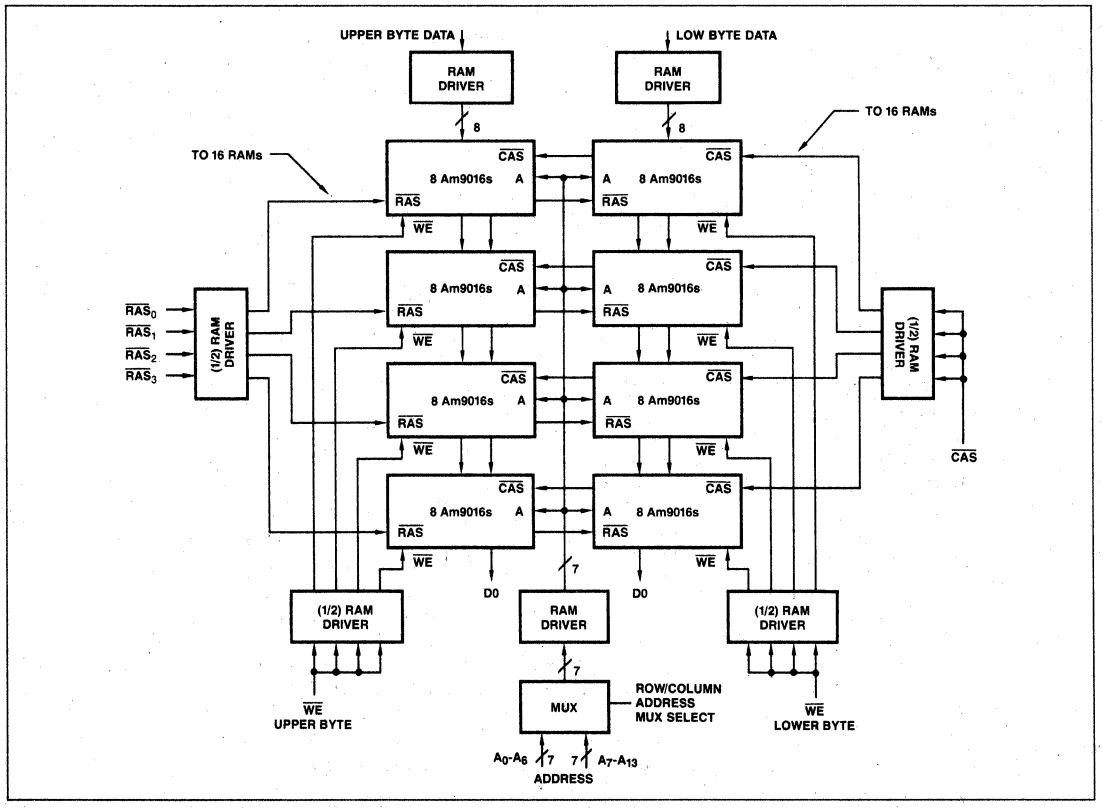


Figure 7. Typical 64K Word by 16-Bit Memory System

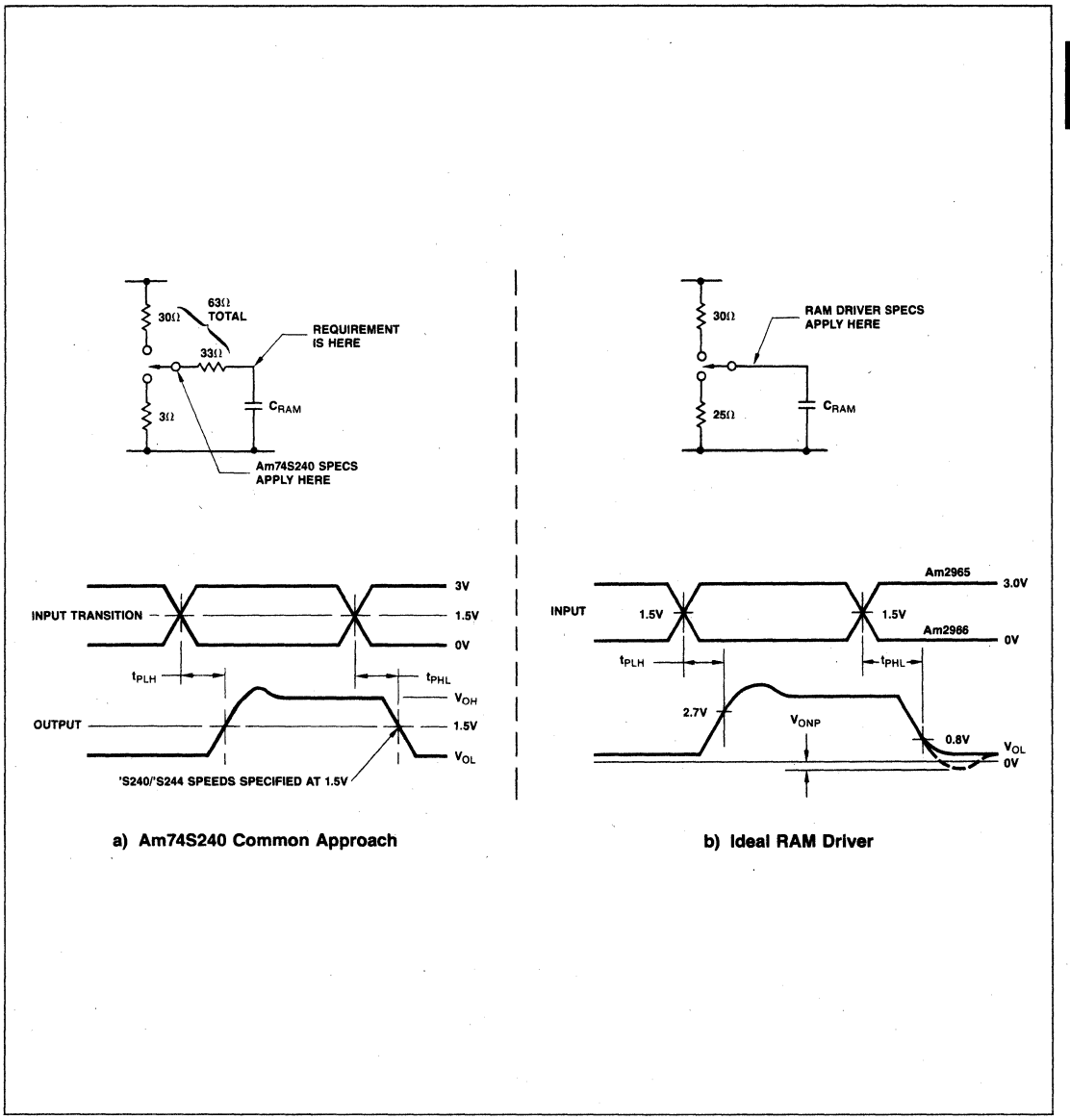
DESIGN ADVANTAGES OF THE Am2965/2966

Compared with Schottky parts such as the Am74S240 or Am74S244, which are used as RAM drivers today, the Am2965/66 RAM drivers offer more advantages than just a RAM driver having no external source resistor.

First, as Figure 8a shows, propagation delays for the Schottky Am74S240 or Am74S244 are measured at 1.5V, which is not where the RAM thresholds are. They are at 0.8V, 2.4V and 2.7V as shown in Figure 8b.

On the Am2965 and Am2966, the LOW-to-HIGH transition voltage propagation delay speeds are measured at 2.7V. Going from HIGH-to-LOW, speed is measured at 0.8V, which is where the actual RAM thresholds are.

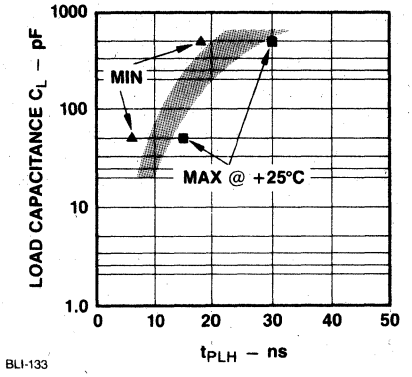
Propagation delays are specified differently, which also makes the Am2965/66 unique (Figure 9). Both minimum and maximum propagation delays are specified at 25°C and 5V. This enables the design engineer to do a worst-case design using both minimum and maximum numbers for the drivers to determine the skew between various drivers. A specified t_{PD} minimum of 50pF and an unusual maximum of 500pF provide a full range of capacitance specifications for both LOW-to-HIGH and HIGH-to-LOW transitions.



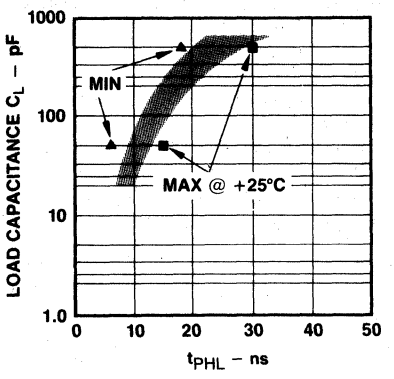
a) Am74S240 Common Approach

b) Ideal RAM Driver

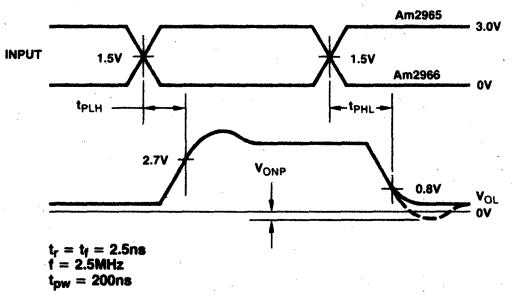
Figure 8. Am2965/66 • AmZ8165/66 Comparison with Am74S240



a) t_{PLH} for V_{OH} = 2.7 Volts vs. C_L



b) t_{PHL} for V_{OL} = 0.8 Volts vs. C_L



c) Output Drive Levels

Figure 9. RAM Driver Propagation Delays

Am2968
Dynamic Memory Controller

DISTINCTIVE CHARACTERISTICS

- Provides control for 16K, 64K, and 256K DRAMs
- Directly drives up to 88 DRAMs
- Highest-order two address bits select one of four banks of RAMs
- Separate output enable for multi-channel access to memory
- Chip select for easy expansion
- Burst, distributed, or transparent refresh mode determined by user
- Supports scrubbing operations and nibble-mode access
- IMOX™ processing
- 48-pin dual in-line package
- 100% product assurance testing to MIL-STD-883

FUNCTIONAL DESCRIPTION

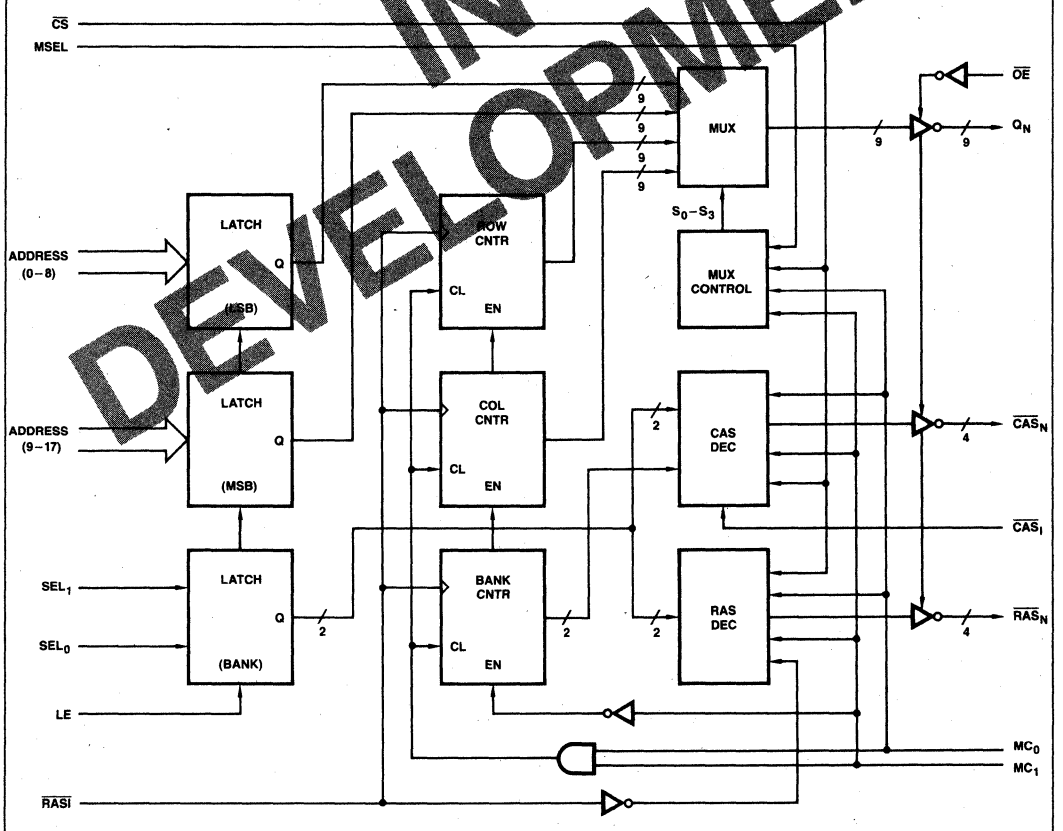
The Am2968 Dynamic Memory Controller is intended to be used with today's high performance memory systems. It has two 9-bit address latches which allow the chip to be used with 16K, 64K, or 256K dynamic RAMs. A two-bit bank select latch for the two high-order address bits is provided to select one each of the four $\overline{RAS}$ and $\overline{CAS}$ outputs.

In refresh mode, two counters cycle through the refresh addresses. Only the ROW counter is used for refresh without scrubbing, generating up to 512 addresses to refresh a 512-cycle-refresh 256K DRAM. The column counter is used only in refresh with scrubbing. In this mode all $\overline{RAS}$ outputs are generated with only one $\overline{CAS}$ output.

4

LOGIC DIAGRAM

Am2968 DYNAMIC MEMORY CONTROLLER



Am2969 • Am2970

Memory Timing Controllers

DISTINCTIVE CHARACTERISTICS

Am2969

- Provides complete timing control for Dynamic Memory Controllers
- Complete timing control for the Am2960, Am2961/2962 Error Correction Circuits including scrubbing
- Delay-line-controlled timing
- Arbitrates between refresh and memory requests
- Supports 128-, 256-, 512-cycle burst refresh
- Initializes memory on power-up
- Provides $\overline{WE}$ drive for memory array (up to 88 DRAMs)
- IMOX™ processing
- 48-pin DIP package
- 100% MIL-STD-883 reliability assurance testing

Am2970

- Provides timing control for Dynamic Memory Controllers
- Delay-line timing reference
- Supports 128-, 256-, 512-cycle burst refresh
- Arbitrates refresh and memory cycle requests
- Performs memory initialization
- Provides $\overline{WE}$ drive for memory array (up to 88 DRAMs)
- IMOX processing
- 24-pin 0.3″ space-saving package

FUNCTIONAL DESCRIPTION

The Am2969/2970 are high performance memory timing controllers. The Am2969 is designed to provide all the control signals for the Am2968 Dynamic Memory Controller and the existing Am2960 error detection and correction (EDC) unit. For memory systems not utilizing the Am2960 EDC unit, the Am2970 will provide all the control signals for the Am2968 Dynamic Memory Controller. It will also reduce IC cost and board space. The use of a delay line with both the Am2969 and Am2970 provides maximum flexibility to the system designer as well as allowing him to achieve maximum performance.

The Am2970 supports functions which are a subset of the Am2969. By choosing not to utilize the EDC functions, the Am2970 can be packaged into a 24-pin DIP.

The Am2969 timing controller may be segregated into seven functional parts:

CPU status decode – Latches status of the CPU and decodes the control bits to define the type of cycle.

Configuration and timing control – Receives control bits which define the type of refresh cycle.

Refresh timer – Determines when a refresh cycle is needed.

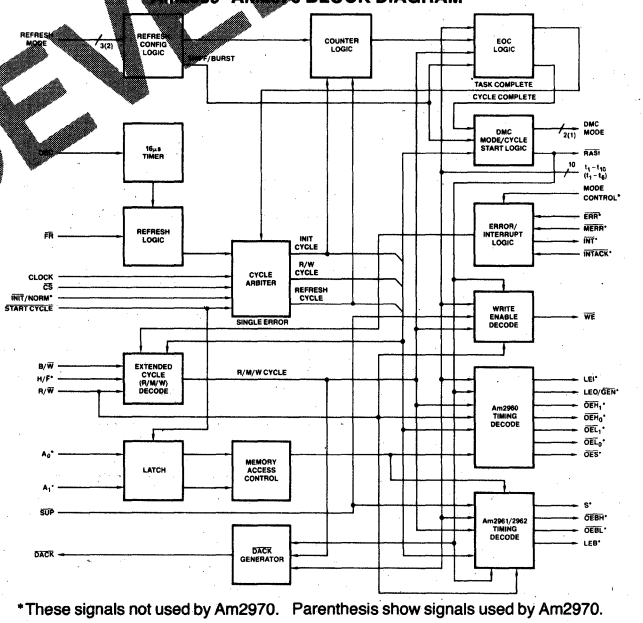
Arbiter – Determines whether a refresh or a read/write cycle should be started.

DMC controller – Generates the interface control signals to be sent to the Dynamic Memory Controller.

EDC and multiple bus controller – Generates the interface control signals to the EDC units and the Multiple Bus Buffers.

Error and interrupt control – Controls the timing of signals to the EDC unit to allow it time to correct bits in error.

Am2969 • Am2970 BLOCK DIAGRAM



*These signals not used by Am2970. Parenthesis show signals used by Am2970.

IMOX is a trademark of Advanced Micro Devices, Inc.

Am8163 • Am8167

Dynamic Memory Timing, Refresh and EDC Controllers

DISTINCTIVE CHARACTERISTICS

- Complete CPU to dynamic RAM control interface
- $\overline{RAS}$/MSEL/$\overline{CAS}$ Sequencer to eliminate delay lines
- Memory request/refresh arbitration
- Complete EDC/data path controls for Word/Byte read or write
- Automatic write-back of corrected data and check bits when single errors are detected on any read cycle
- Refresh interval timer independent of CPU
- Refresh control during Single-Step or Halt modes
- EDC error flag latches for error logging under software control
- Two timing configurations support a broad range of processors (Z80, Z8000, 8086, 8088, MC68000)

TABLE OF CONTENTS

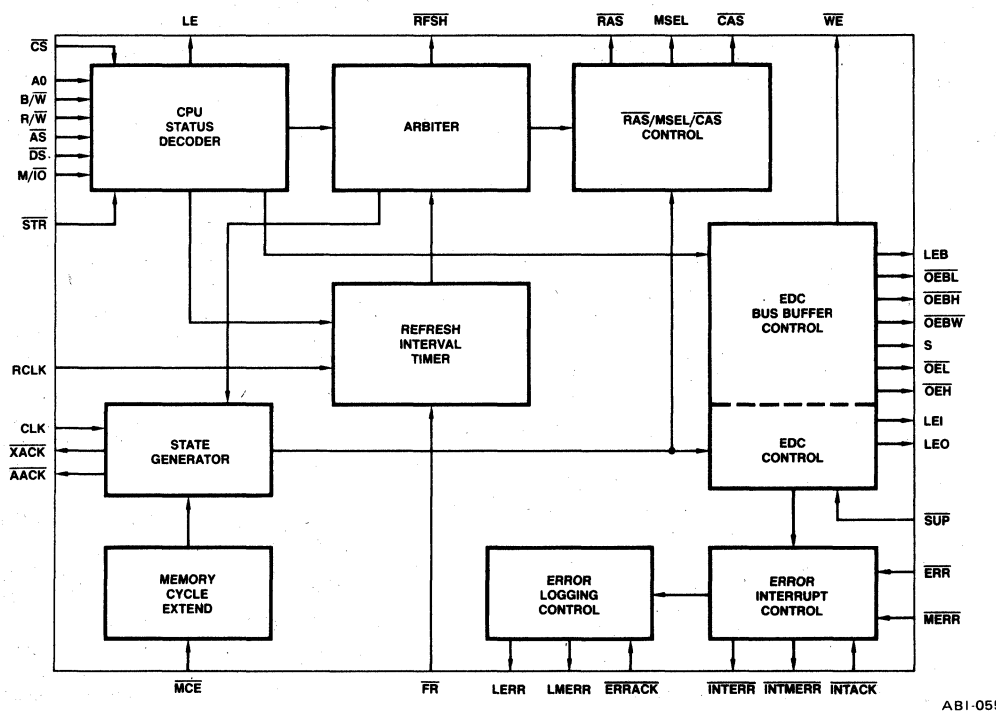
GENERAL DESCRIPTION

The Am8163 and Am8167 are high speed bus interface controllers forming an integral part of the 8086 and AmZ8000* memory support chip set using dynamic MOS RAMs with Error Detection and Correction (EDC). The complete chip set includes the Am8284A and AmZ8127 Clock Generators, the Am2964B Dynamic Memory Controller, the Am2961/62 EDC Bus Buffers, the Am2960 EDC Unit and Am2965/66 RAM Drivers.

The Am8163 and Am8167 provide all of the control interface functions including $\overline{RAS}$/Address-MUX/$\overline{CAS}$ timing (without delay lines), refresh timing, memory request/refresh arbitration and all EDC enables and controls. The enable controls are configured for both word and byte operations including the data controls for byte write with error correction. The Am8163/7 generates bus and operating mode controls for the Am8160 EDC Unit.

The Am8163/7 uses the AmZ8127 oscillator output to generate $\overline{RAS}$/Address MUX/$\overline{CAS}$ timing. An internal refresh interval timer generates the memory refresh request independent of the CPU to guarantee the proper refresh timing under all combinations of CPU and DMA memory requests.

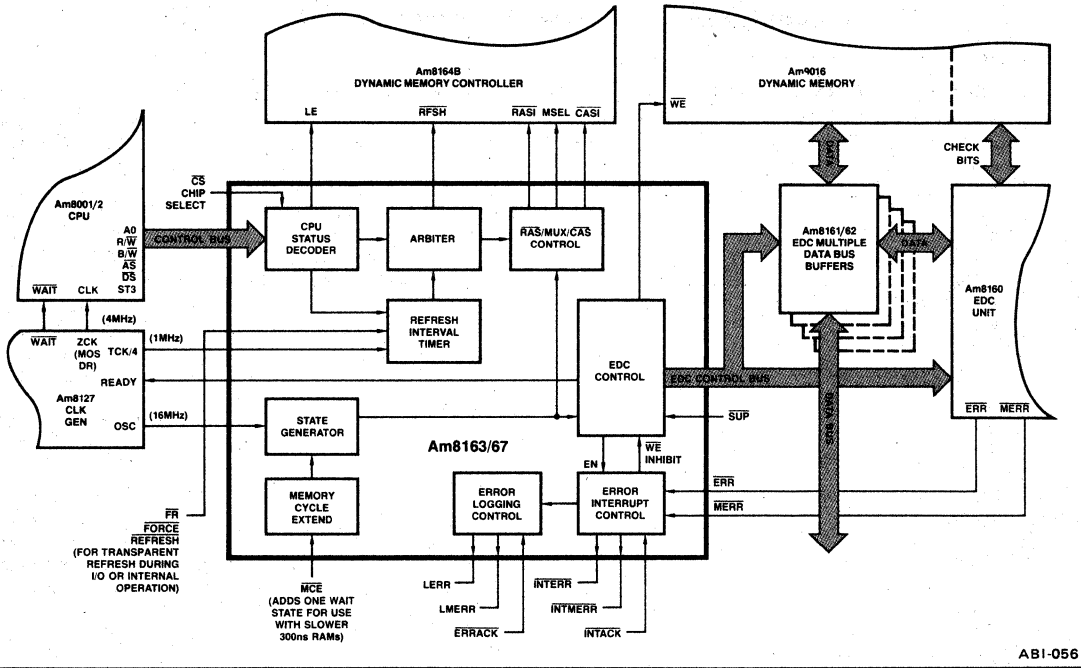
BLOCK DIAGRAM



ABI-055

*Z8000 is a trademark of Zilog.

SYSTEM DIAGRAM



ABI-056

Am8163/67 FUNCTIONAL DESCRIPTION

The Am8163/67 provides timing and control for Error Detection and Correction (EDC) using dynamic Random Access Memories (RAM) together with the Am2960 family of EDC devices. See Table 1 to determine which device (Am8163/67) is best suited to which processor.

The Am2960 family provides an optimized, but also flexible solution to the interface between MOS microprocessors and dynamic MOS RAMs.

The Am2960 performs the function of error detection and correction, using a modification of the well-known Hamming Code algorithm.

The Am2961 and Am2962 are bus buffers optimized for operation with the Am2960.

TABLE 1.

Processor			Am8163	Am8167
Z80A			X	
Z80B			X	
Z8000	–	4MHz	X	
	–	6MHz		X
	–	8MHz	X	X
8086	–	5MHz	X	
	–	10MHz		X
8088	–	5MHz	X	
	–	10MHz		X
68000	–	4MHz	X	
	–	6MHz		X
	–	8MHz	X	X
	–	10MHz	X	X
	–	12MHz	X	X

Note: Where X's appear in both columns either device may be used.

The Am2964B performs address latching and multiplexing for the RAS/CAS sequence. It also contains a refresh counter that can be multiplexed onto the address outputs.

The Am2965 and Am2966 are octal memory address bus drivers, similar and pin compatible to the popular 74LS240 and 74LS244, but with on-chip resistors that reduce the problem of undershoot on unterminated address lines.

None of the above mentioned circuits contain timing elements. To achieve the greatest versatility, this function is concentrated in the Am8163.

The Am8163/67 performs two independent functions:

1. It provides timing and control to the Am2964B Dynamic Memory Controller, i.e. the RAS/CAS Refresh address multiplexer.
2. It provides timing and control for the 2960, 2961, or 2962 EDC circuits and interfaces with the microprocessor's interrupt lines and WAIT input.

RAS/CAS and Refresh

The Am8163/67 accepts several control signals from the microprocessor (BYTE/WORD, READ/WRITE, Address Strobe, Data Strobe, Memory/IO) and a Refresh clock signal from the clock generator.

From these inputs the Am8163/67 generates control signals for the 2964B RAS/CAS and Refresh multiplexer.

The LE output, when HIGH, makes the 2964B input latches transparent. The HIGH-to-LOW transition of LE latches address information into the 2964B.

The RAS output is activated when the appropriate combination of STR, M/IO, and CS occur or when a refresh operation is to be performed. MSEL goes LOW one clock period after RAS went LOW.

$\overline{CAS}$ goes LOW a short specified delay after MSEL went LOW. $\overline{RAS}$, MSEL and $\overline{CAS}$ go HIGH together, eight clock periods after RAS went LOW. The RAS/CAS timing is thus derived from a high frequency (16MHz clock) without any monostables or delay lines.

The Am8163 and Am8167 are comparable except for the CAS timing sequence.

The Am8163 timing is optimized for operation with a 4MHz microprocessor clock, derived from a 16MHz oscillator. The $\overline{RAS}$ to MS delay is one oscillator period (62ns) and the MS to $\overline{CAS}$ delay is combinatorial, 16ns minimum.

The Am8167 timing is optimized for operation with a 5.5MHz microprocessor clock, derived from a 22MHz oscillator. The $\overline{RAS}$ to MS delay is one oscillator period (47ns) and the MS to $\overline{CAS}$ delay is also one oscillator period (47ns).

Dynamic Memory Refresh

The proper sequencing of refresh operations can be performed either by the CPU (transparent refresh) or by the memory controller (stand-alone refresh).

Transparent refresh, as implemented in the Z80 and Z8000 microprocessors is simple and avoids all memory contention, but it wastes processor time and is not fully compatible with DMA operation.

"Stand-alone" refresh puts the responsibility of refresh address generation and timing on the memory controller. The Am8163/67 performs the necessary timing and access arbitration. The internal refresh interval timer generates a refresh request after every 16 clock pulses on the RCLK refresh clock input (typically 1MHz). When FR (force refresh) goes LOW, the ÷ 16 counter is cleared and the internal refresh request is generated.

Refresh requests and memory requests are synchronized inside the Am8163/67 where the arbiter circuit resolves potential conflicts. If a refresh request occurs after a memory request or during a memory operation, this refresh request will be honored after the memory transaction is complete and the necessary additional precharge time has elapsed.

Similarly, if a memory request occurs after a refresh request or during a refresh operation, this memory request will not be acknowledged until the refresh operation is completed and the necessary precharge time has elapsed. When memory and refresh requests occur simultaneously, the arbiter favors the memory request.

Error Detection/Correction

The other function of the Am8163/67 is timing and control for Error Detection and Correction using the 2960, 2961 or 2962 circuits.

The Am8163/67 drives the ECC Control Bus and receives ERROR or MULTIPLE ERROR inputs from the 2960 Error Detection and Correction Unit. The Am8163/67 also interfaces with the microcomputer interrupt structure and with the error logging circuitry.

The 2960 can support two methods of error correction, "Correct Only On Error" and "Correct Always".

"Correct Only On Error" relies on the fact that error detection is faster than correction. Data read from the memory is fed directly to the processor. A read error will insert a wait state while the error is being corrected and data is also being written back into the memory. At reasonably low error rates this scheme achieves the highest possible throughput, but it is incompatible with all present microprocessors, since they sample their WAIT input too early in the cycle.

The Am8163/67 implements the other scheme, "Correct Always," which is compatible with all modern microprocessors.

This scheme allocates enough time to insure corrected data is sent to the CPU. Additionally the Am8163/67 allows time after each memory read operation, to write the corrected result back into the memory. This write operation, however, is executed only if there was a single error: There is no need to write correct data back, and it is undesireable to write the wrong result of a double error.

The Am8163/67 also provides the proper control signals to allow byte write operation in 16-bit memory systems with Error Correction. The Am8163/67 automatically first performs a word read operation, retains the corrected unused byte in the 2960, and then writes the composite word and check bits into the memory. Outputs LEO, LEI, $\overline{OEH}$, $\overline{OEL}$ and S, are responsible for this.

- $\overline{OEL}$ is pulsed LOW during every read operation (byte or word) and during a byte write operation with A0 = 0 (even address)
- $\overline{OEH}$ is pulsed LOW during every read operation (byte or word) and during a byte write operation with A0 = 1 (odd address)
- $\overline{OEBW}$ is pulsed LOW during every read operation
- $\overline{OEBL}$ is pulsed LOW during every read operation with A0 = 1 (odd address)
- $\overline{OEBH}$ is pulsed LOW during every read operation with A0 = 0 (even address)

Note: The $\overline{OE}$ and $\overline{OEB}$ outputs interpret A0 in opposite ways. This is consistent with 2960/61 operation.

R/$\overline{W}$	B/$\overline{W}$	A0	$\overline{OEH}$	$\overline{OEL}$	$\overline{OEBW}$	$\overline{OEBH}$	$\overline{OEBL}$
L	L	L	H	H	H	H	H
L	L	H	H	H	H	H	H
L	H	L	H	L	H	H	H
L	H	H	L	H	H	H	H
H	L	L	L	L	L	L	H
H	L	H	L	L	L	H	L
H	H	L	L	L	L	L	H
H	H	H	L	L	L	H	L

$\overline{OEBW}$, $\overline{OEBH}$, and $\overline{OEBL}$ can be active (LOW) only if:
$\overline{DS}$ = $\overline{CS}$ = L AND $\overline{SUP}$ = H

Note that 16-bit memory with EDC must always be initialized with word write operations in order to allow a later byte write operation. (An uninitialized memory would most likely read multiple errors and would then not allow byte write operation).

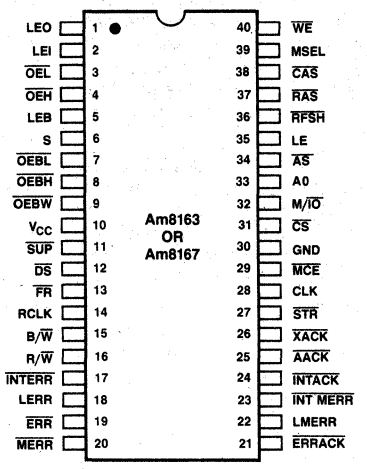
Error Interrupt Control

The Am8163/67 clocks in the $\overline{ERROR}$ and $\overline{MULTIPLE\ ERROR}$ signals coming from the 2960 and stores them in both the Interrupt Logic and in the Error Control Logic.

Interrupt Acknowledge clears both $\overline{INTERR}$ and $\overline{INTMERR}$. The latter must therefore always be the higher priority interrupt.

The Error Logic Control circuit latches up the two bits in the Error Interrupt Control circuit. The LERR and LMERR outputs are cleared by $\overline{ERRACK}$, provided that the interrupts have been cleared first. These signals are normally used to control updating of the syndrome latch or other diagnostic circuitry.

CONNECTION DIAGRAM
Top View



ABI-057

Note: Pin 1 is marked for orientation.

FUNCTIONAL PIN DESCRIPTION

BUS CONTROL

CLK **CLOCK (input)**
The CLK input determines memory cycle timing via the internal state machine from which the control outputs are derived. It is normally 16MHz for the Am8163 and 22MHz for the Am8167. The clock can run at lower frequencies but not higher because of other memory timing constraints.

RCLK **REFRESH CLOCK (input)**
This input determines the period of the internal refresh interval ÷ 16 timer and is normally 1MHz. This results in a refresh cycle every 16 microseconds. This provides an internal refresh request to guarantee valid memory data independent of other system operating modes, (memory request, DMA, etc.).

$\overline{FR}$ **FORCE REFRESH (input)**
FR is used to force a refresh cycle at user designated times. One example is transparent refresh during I/O operations. The refresh interval timer is reset so the next refresh occurs 16 RCLK cycles later if no other $\overline{FR}$ pulses occur. $\overline{FR}$ can be used to minimize collisions with memory requests, thereby reducing the amount of time the CPU waits for refresh.

$\overline{XACK}$ **TRANSFER ACKNOWLEDGE (output, open collector)**
This active LOW output indicates that corrected data has been latched in the Am8160 EDC output latch (as opposed to indicating data is valid on the system bus).

$\overline{AACK}$ **ADVANCED ACKNOWLEDGE (output, open collector)**
This active LOW output indicates that a memory access has started. It can be used to run without wait states when the memory system timing is synchronous with the CPU clock. Multibus or asynchronous configuration should use $\overline{XACK}$ to control the CPU Ready input.

$\overline{SUP}$ **SUPPRESS (input)**
This active LOW input inhibits access to the RAM in memory access protected systems. It must be valid before the HIGH-to-LOW transition of $\overline{DS}$ to suppress a read cycle. It must remain valid until after the cycle ($\overline{RAS}$). This is required because $\overline{SUP}$ simply inhibits $\overline{WE}$ on a write and inhibits $\overline{OEBH}$, $\overline{OEBL}$, and $\overline{OEBW}$ on a read, without halting the internal state generator.

$\overline{DS}$ **DATA STROBE (input)**
This active LOW input is used during read cycles to generate $\overline{OEBL}$, $\overline{OEBH}$ and $\overline{OEBW}$. These signals control when data is enabled onto the system data bus.

A0 **ADDRESS BIT 0 (input)**
A0 data input is latched internally on the LOW-to-HIGH transition of $\overline{AS}$. It is used during byte operations to designate whether high byte or low byte data is being accessed.

A0 = LOW for high byte operations and A0 = HIGH for low byte operations with the AmZ8000 Family CPU's. A0 phasing is opposite for 8086 and inversion can be avoided by interchanging the roles of $\overline{OEL}$ and $\overline{OEH}$ (and $\overline{OEBL}$ and $\overline{OEBH}$).

$\overline{AS}$ **ADDRESS STROBE (input)**
The $\overline{AS}$ input is used to control the A0 latch. When HIGH, A0 data is latched. For non-multiplexed buses, the $\overline{AS}$ input is tied LOW to make the latch transparent.

B/$\overline{W}$ **BYTE/$\overline{WORD}$ (input)**
This input designates a byte operation if HIGH and a word operation if LOW. It must be valid throughout the memory transaction. The Am8163/7 uses this input to determine $\overline{OEH}$ and $\overline{OEL}$.

R/$\overline{W}$ **READ/$\overline{WRITE}$ (input)**
This input indicates a read operation when HIGH and a write operation when LOW. It must be valid throughout the memory transaction. The Am8163/7 uses this input to determine the outputs $\overline{OEH}$, $\overline{OEL}$, $\overline{OEBH}$, $\overline{OEBL}$, and $\overline{OEBW}$.

M/$\overline{IO}$ **MEMORY/$\overline{INPUT\text{-}OUTPUT}$ (input)**
This signal serves as an active HIGH chip select for memory operations. It is used in conjunction with $\overline{CS}$ to determine if $\overline{STR}$ is valid. It must be HIGH before the LOW-to-HIGH transition of $\overline{STR}$ if the $\overline{STR}$ input command is a pulse (AmZ8000). When using a level input (multibus) to start the cycle, M/$\overline{IO}$ must become valid no later than one clock period after the HIGH-to-LOW transition of $\overline{STR}$.

$\overline{CS}$ **CHIP SELECT (input)**
This active LOW input is one of the enables for the Am8163/7. It must be LOW before the LOW-to-HIGH transition of $\overline{STR}$ when using a pulse to start a memory access. When using a level input to start

the cycle, $\overline{CS}$ must become valid no later than one clock period after the HIGH-to-LOW transition of $\overline{STR}$.

$\overline{STR}$ **$\overline{START}$ (input)**
This active LOW input can be a pulse or a level. It is used to indicate when memory access is requested. It must not extend past the LOW-to-HIGH transition of $\overline{DS}$.

ADDRESS CONTROL

LE **LATCH ENABLE (output)**
This output controls the LATCH ENABLE input of the Dynamic Memory Controller. When LE is HIGH the DMC address input latch is transparent. When LE is LOW the address is latched. This signal is $\overline{AS}$ inverted.

$\overline{RFSH}$ **$\overline{REFRESH}$ (output)**
This active LOW output indicates a refresh operation is to be done. The Dynamic Memory Controller uses this signal to select the refresh address output.

$\overline{RAS}$ **$\overline{ROW\ ADDRESS\ STROBE}$ (output)**
This active LOW output strobes the row address into memory. The $\overline{RAS}$ HIGH-to-LOW transition occurs during t_0 if $\overline{STR}$, M/$\overline{IO}$ and $\overline{CS}$ have selected a memory cycle. Additionally, $\overline{RAS}$ will be active one t-state after the $\overline{RFSH}$ HIGH-to-LOW transition occurs during refresh. The $\overline{RAS}$ LOW-to-HIGH transition at the end of each cycle starts an internally timed $\overline{RAS}$ precharge time consisting of three t-states.

MSEL **MULTIPLEXER SELECT (output)**
This output controls the row and column address selection in the DMC. When MSEL is HIGH, the row address is selected and when LOW, the column address is selected. MSEL is normally HIGH and goes LOW only during memory accesses.

$\overline{CAS}$ **$\overline{COLUMN\ ADDRESS\ STROBE}$ (output)**
This active LOW output strobes the column address into memory. It is generated only during memory accesses.

ERROR LOGGING AND CONTROL

$\overline{ERR}$ **$\overline{ERROR}$ (input)**
This active LOW signal from the Am8160 EDC indicates when an error has occurred. The Am8163 samples this input just before the HIGH-to-LOW transition of $\overline{LEO}$. Single errors cause an automatic write-back of corrected data.

$\overline{MERR}$ **$\overline{MULTIPLE\ ERROR}$ (input)**
This active LOW signal from the EDC indicates when a multiple error has occurred. Write back to memory is inhibited if a $\overline{MULTIPLE\ ERROR}$ occurs on a read cycle.

LERR **LATCHED ERROR (output)**
This active HIGH output is set HIGH as a result of the $\overline{ERR}$ input becoming active. LERR HIGH indicates an error has occurred. LERR is normally used to control error logging. It is reset when $\overline{ERRACK}$ goes LOW.

LMERR **LATCHED MULTIPLE ERROR (output)**
This active HIGH output is set HIGH as a result of the $\overline{MERR}$ input. When HIGH, it indicates a multiple error has occurred. It is reset when $\overline{ERRACK}$ goes low.

$\overline{INTERR}$ **$\overline{INTERRUPT\ ERROR}$ (output, open collector)**
This active LOW output is used to interrupt the CPU when an error occurs. This can be used for diagnostics or error logging. $\overline{INTERR}$ has high output drive capability in order to drive system buses.

$\overline{INTMERR}$ **$\overline{INTERRUPT\ MULTIPLE\ ERROR}$ (output, open collector)**
This active LOW output is used to interrupt the CPU when a multiple error occurs. This can be used for diagnostics or error logging. $\overline{INTMERR}$ has high output drive capability in order to drive system buses.

$\overline{INTACK}$ **$\overline{INTERRUPT\ ACKNOWLEDGE}$ (input)**
This active LOW input resets both the $\overline{INTERR}$ and $\overline{INTMERR}$ signals.

$\overline{ERRACK}$ **$\overline{ERROR\ ACKNOWLEDGE}$ (input)**
This active LOW input resets the error logging flags, LERR and LMERR. It is only effective when $\overline{INTACK}$ has previously cleared the interrupt flags, $\overline{INTERR}$ and $\overline{INTMERR}$.

EDC CONTROL

LEB **LATCH ENABLE BUS (output)**
LEB is used to latch corrected data in the external Am8161/2 EDC Data Bus Buffers. By latching data output to the system data bus, the CPU can be operated in a single-step mode. The data latch is required to capture data so the memory can be released for refresh immediately after a read (or write) cycle.

LEO **LATCH ENABLE OUTPUT (output)**
LEO is used to latch corrected data in the Am8160 EDC data output latch. Correct data is then available to regenerate correct check bits for the write portion of the read-modify-write cycle. LEO can also control LEY of the Am8161/2 EDC Data Bus Buffers (the input latch from the system data bus). This is required in systems where the CPU removes data from the system data bus before the Am8163/7 has completed a write cycle.

LEI **LATCH ENABLE INPUT (output)**
LEI is used to control the Am8160 EDC's input latch. It is normally LOW when a memory cycle is not in progress. This prevents transitions on the bus from toggling the EDC logic, thereby reducing power dissipation and system noise. LEI latches the input data so the EDC data bus (Y bus) can be TURNED AROUND WHILE the EDC is correcting the data. Cycle time is reduced by doing these functions in parallel.

S **SELECT (output)**
This output controls the multiplexer that selects EDC input data. It is normally HIGH to select data from the system bus. When LOW it selects data from memory. Since all cycles are a read-modify-writes, S switches every cycle. All memory operations take the same number of internal t-states. There is no difference in the length of a cycle on read or write, error or no error.

$\overline{OEBH}$ **OUTPUT ENABLE BUS HIGH (output)**
$\overline{OEBH}$ output enables the high byte data onto the system data bus during byte read operations. It is used when interfacing to 8-bit data buses or the Multibus.*

$\overline{OEBL}$ **OUTPUT ENABLE BUS LOW (output)**
$\overline{OEBL}$ output enables the low byte of data onto the system data bus during Byte Read operations. It is used when interfacing to 8-bit data buses or the Multibus.

$\overline{OEBW}$ **OUTPUT ENABLE BUS WORD (output)**
$\overline{OEBW}$ output enables data onto the system data bus. It occurs on every read cycle independent of B/$\overline{W}$. It is used for 16-bit systems or Multibus systems.

$\overline{OEH}$ **OUTPUT ENABLE HIGH (output)**
$\overline{OEH}$ controls the high byte of the EDC data bus (Y bus). When $\overline{OEH}$ is HIGH the Am2961/62 are driving the bus. When $\overline{OEH}$ is LOW, the Am8160 EDC is driving the bus. $\overline{OEH}$ is HIGH during word writes and goes low on reads and byte writes.

$\overline{OEL}$ **OUTPUT ENABLE LOW (output)**
$\overline{OEL}$ controls the low byte of the EDC data bus (Y bus). When HIGH, the Am2961/62's are driving the bus. When LOW, the Am2960 is driving the bus. $\overline{OEL}$ is HIGH during word writes and goes LOW on reads and byte writes.

OTHER CONTROLS

$\overline{WE}$ **WRITE ENABLE (output)**
$\overline{WE}$ controls the memory during a write operation. It is generated during a byte or word write and also during a read if a single error has occurred. $\overline{WE}$ always occurs at the end of the memory cycle. Thus, the RAM is always doing a late write.

$\overline{MCE}$ **MEMORY CYCLE EXTEND (input)**
This input is normally not used and is pulled up internally to produce "normal" timing. When tied LOW it extends the memory cycle (adds 5 t_2 states for Am8163 and adds 4 t_3 states for Am8167). This allows use of slower RAMs. Note that $\overline{MCE}$ affects the refresh cycle as well as the normal cycle. By adding external logic the user may extend the cycle by 1, 2 or 3 t-states instead. This is done by keeping MCE low until 2, 3, or 4 clocks after MS for the 8163 or 2, 3, or 4 clocks after $\overline{CAS}$ for the 8167.

*Multibus is a registered trademark of Intel Corporation.

FUNCTION TABLES
Am8163/8167

R/$\overline{W}$	B/$\overline{W}$	A0	$\overline{OEH}$	$\overline{OEL}$
L	L	L	H	H
L	L	H	H	H
L	H	L	H	L
L	H	H	L	H
H	L	L	L	L
H	L	H	L	L
H	H	L	L	L
H	H	H	L	L

OEH and OEL are enabled by appropriate sequencer "T" states. (See Timing diagram)

$\overline{DS}$	R/$\overline{W}$	B/$\overline{W}$	A0	$\overline{OEBH}$	$\overline{OEBL}$	$\overline{OEBW}$
X	L	L	L	H	H	H
X	L	L	H	H	H	H
X	L	H	L	H	H	H
X	L	H	H	H	H	H
L	H	L	L	L	H	L
L	H	L	H	H	L	L
L	H	H	L	L	H	L
L	H	H	H	H	L	L
H	X	X	X	H	H	H

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5 to +5.5V
DC Output Current, into Outputs	30mA
DC Input Current	−30 to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise noted)

MIL T_C = −55 to +125°C V_{CC} = 4.50 to 5.50V
COM'L T_C = 0 to 70°C V_{CC} = 4.75 to 5.25V

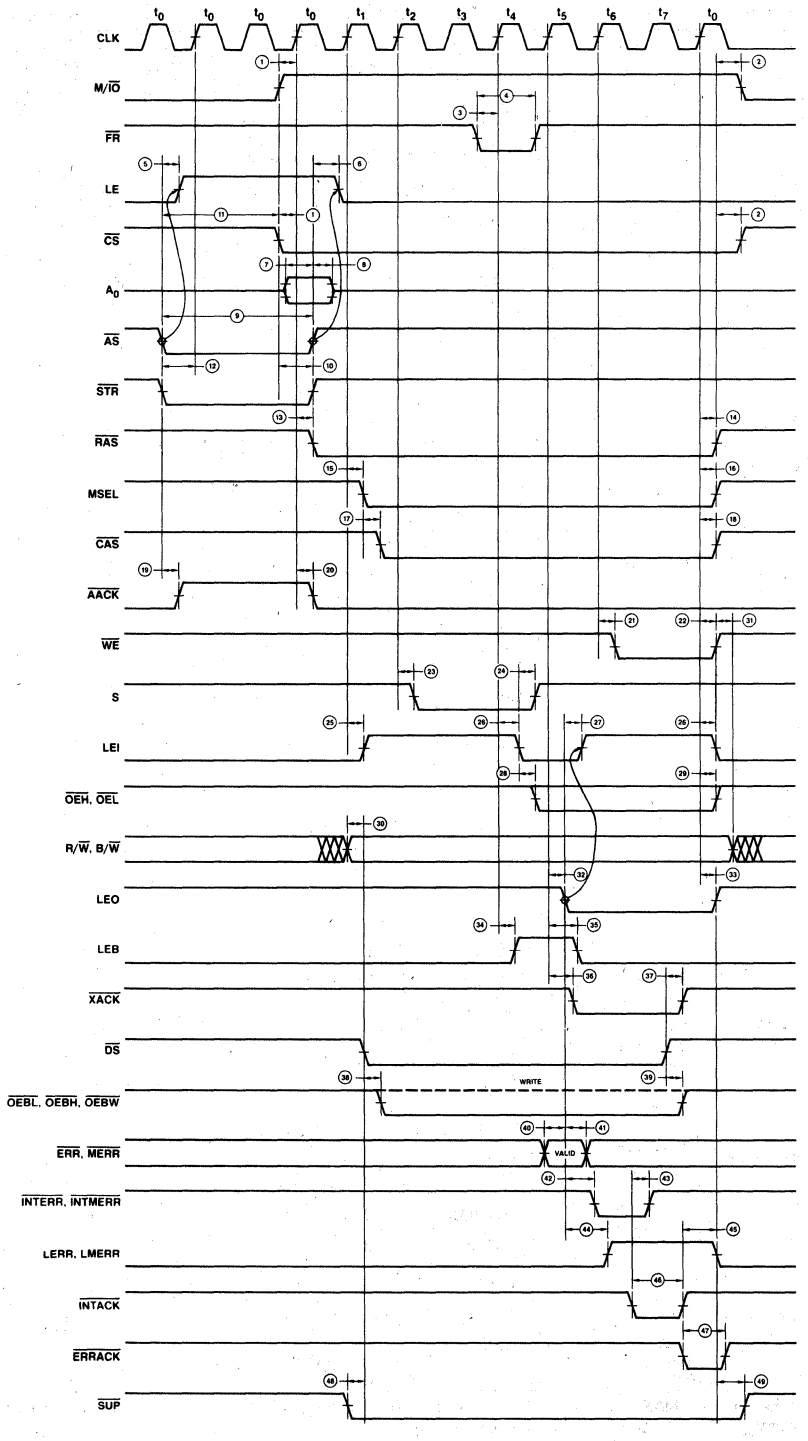
(Group A, Subgroups 1, 2 and 3)

Parameters	Description		Test Conditions		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	**Output(s):** All except open collectors	MIL, I_{OH} = −1.0mA	2.4			Volts
				COM'L, I_{OH} = −2.6mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	**Output(s):** LERR, LMERR	I_{OL} = 8mA			0.50	Volts
			$\overline{CAS}$, $\overline{RAS}$, $\overline{OEBH}$, $\overline{OEBL}$	I_{OL} = 12mA			0.50	
			$\overline{OEH}$, $\overline{OEL}$, $\overline{OEBW}$, $\overline{RFSH}$	I_{OL} = 12mA			0.50	
			LEO, LEI, $\overline{WE}$	I_{OL} = 12mA			0.50	
			LEB, LE, S, MSEL	I_{OL} = 12mA			0.50	
			$\overline{INTMERR}$, $\overline{INTERR}$	I_{OL} = 16mA			0.50	
			$\overline{XACK}$, $\overline{AACK}$	I_{OL} = 32mA			0.50	
V_{IH}	Guaranteed Input Logical HIGH Voltage		**Input(s):** All		2.0			Volts
V_{IL}	Guaranteed Input Logical LOW Voltage		**Input(s):** All	MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	**Input(s):** All	I_{IN} = −18mA			−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = Max V_{IN} = 0.5V	**Input(s):** A0, M/$\overline{IO}$, RCLK, B/$\overline{W}$, R/$\overline{W}$, $\overline{STR}$, $\overline{AS}$, $\overline{INTACK}$	MIL			−0.42	mA
				COM'L			−0.40	
			$\overline{FR}$, $\overline{SUP}$, $\overline{ERRACK}$, $\overline{MCE}$	MIL			−0.82	mA
				COM'L			−0.8	
			$\overline{CLK}$, $\overline{CS}$, $\overline{DS}$, $\overline{ERR}$	MIL			−2.1	mA
				COM'L			−2.0	
			$\overline{MERR}$	MIL			−2.6	mA
				COM'L			−2.4	
I_{IH}	Input HIGH Current	V_{CC} = Max V_{IN} = 2.7V	**Input(s):** $\overline{MERR}$	MIL			100	μA
				COM'L			70	
			CLK, $\overline{CS}$, $\overline{DS}$, $\overline{ERR}$	MIL			70	μA
				COM'L			50	
			$\overline{FR}$, $\overline{SUP}$, $\overline{MCE}$, $\overline{ERRACK}$				40	μA
			M/$\overline{IO}$, A0, RCLK, B/$\overline{W}$, R/$\overline{W}$				20	
			$\overline{AS}$, $\overline{STR}$, $\overline{INTACK}$				20	
I_I	Input HIGH Current	V_{CC} = Max V_{IN} = 5.5V	**Input(s):** CLK, $\overline{CS}$, $\overline{DS}$, $\overline{ERR}$, $\overline{MERR}$				1.0	mA
			$\overline{SUP}$, $\overline{MCE}$, $\overline{FR}$				1.0	
		V_{CC} = Max V_{IN} = 7.0V	M/$\overline{IO}$, A0, RCLK, B/$\overline{W}$, R/$\overline{W}$ $\overline{INTACK}$, $\overline{AS}$, $\overline{STR}$				0.10	
			$\overline{ERRACK}$				0.20	
I_{OH}	Output HIGH Current	V_{CC} = Min V_{OH} = 5.5V	**Output(s):** $\overline{INTMERR}$, $\overline{INTERR}$				100	μA
			$\overline{XACK}$, $\overline{AACK}$				150	
I_{OS}	Output Short Circuit Current	V_{CC} = Max +0.5V V_O = 0.5V	**Output(s):** All (Note 3)		−15		−85	mA
I_{CC}	Power Supply Current		25°C, 5V			280		mA
		8163	0 to 70°C	COM'L			365	mA
		8167	0 to 70°C				390	mA
		8163	−55 to +125°C	MIL			385	mA
		8167	−55 to +125°C				420	mA

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

TIMING WAVEFORMS

Am8163 TIMING



ABI-058

Am8163/67 SWITCHING CHARACTERISTICS

Parameters		Description	$T_A = +25°C$ $V_{CC} = 5.0V$ Min	Typ	Max	Units
1	t_S	M/$\overline{IO}$↑ or $\overline{CS}$↓ to CLK Setup Time	0	−4		ns
2	t_H	M/$\overline{IO}$↓ or $\overline{CS}$↑ to $\overline{RAS}$↑ Hold Time	0	−10		ns
3	t_S	$\overline{FR}$↓ to CLK Setup Time	5	2		ns
4	t_{PWL}	$\overline{FR}$ LOW Pulse Width	tp + 5	tp + 2		ns
5	t_{PLH}	$\overline{AS}$↓ to LE↑ Propagation Delay		12	18	ns
6	t_{PHL}	$\overline{AS}$↑ to LE↓ Propagation Delay		12	18	ns
7	t_S	A0 to $\overline{AS}$↑ Setup Time	1	0		ns
8	t_H	A0 to $\overline{AS}$↑ Hold Time	9	5		ns
9	t_{PWL}	$\overline{AS}$, $\overline{STR}$ LOW Pulse Width	20	9		ns
10	t_S	M/$\overline{IO}$↑ or $\overline{CS}$↓ to $\overline{STR}$↑ Setup Time	2	0		ns
11	t_S	$\overline{CS}$↓ to $\overline{STR}$↓ Setup Time	−tp	−(tp + 10)		ns
12	t_S	$\overline{STR}$↓ to CLK Setup Time	10	6		ns
13	t_{PHL}	CLK to $\overline{RAS}$↓ Propagation Delay		36	41	ns
14	t_{PLH}	CLK to $\overline{RAS}$↑ Propagation Delay		26	34	ns
15	t_{PHL}	CLK to $\overline{MSEL}$↓ Propagation Delay		17	22	ns
16	t_{PLH}	CLK to $\overline{MSEL}$↑ Propagation Delay		21	26	ns
17a	t_{PHL}	$\overline{MSEL}$↓ to $\overline{CAS}$↓ Propagation Delay − 8163	18	23		ns
17b	t_{PHL}	CLK to $\overline{CAS}$↓ Propagation Delay − 8167		17	22	ns
18a	t_{PLH}	CLK to $\overline{CAS}$↑ Propagation Delay − 8163		34	43	ns
18b	t_{PLH}	CLK to $\overline{CAS}$↑ Propagation Delay − 8167		21	26	ns
19	t_{PLH}	$\overline{STR}$↓ to $\overline{AACK}$↑ Propagation Delay		30	35	ns
20	t_{PHL}	CLK to $\overline{AACK}$↓ Propagation Delay		33	41	ns
21	t_{PHL}	CLK to $\overline{WE}$↓ Propagation Delay		17	22	ns
22	t_{PLH}	CLK to $\overline{WE}$↑ Propagation Delay		20	26	ns
23	t_{PHL}	CLK to S↓ Propagation Delay		16	22	ns
24a	t_{PLH}	LEI↓ to S↑ Propagation Delay − 8163	1.0	3.0		ns
24b	t_{PLH}	CLK to S↑ Propagation Delay − 8167		21	26	ns
25	t_{PLH}	CLK to LEI↑ Propagation Delay		20	26	ns
26	t_{PHL}	CLK to LEI↓ Propagation Delay		17	22	ns
27	t_{PLH}	LEO↓ to LEI↑ Propagation Delay	15	20		ns
28a	t_{PHL}	LEI↓ to $\overline{OEH}$↓, $\overline{OEL}$↓ Propagation Delay − 8163	4.5	7.0		ns
28b	t_{PHL}	CLK to $\overline{OEH}$↓, $\overline{OEL}$↓ Propagation Delay − 8167		24	30	ns
29	t_{PLH}	CLK to $\overline{OEH}$↑, $\overline{OEL}$↑ Propagation Delay		24	30	ns
30	t_S	R/$\overline{W}$, B/$\overline{W}$ to $\overline{DS}$↓ Setup Time	0	−1.5		ns
31	t_H	R/$\overline{W}$, B/$\overline{W}$ to $\overline{WE}$↑ Hold Time	0	−10		ns
32	t_{PHL}	CLK to LEO↓ Propagation Delay		15	21	ns
33	t_{PLH}	CLK to LEO↑ Propagation Delay		21	26	ns
34	t_{PLH}	CLK to LEB↑ Propagation Delay		21	26	ns
35	t_{PHL}	CLK to LEB↓ Propagation Delay		24	30	ns
36	t_{PHL}	CLK to $\overline{XACK}$↑ Propagation Delay		29	36	ns
37	t_{PLH}	DS↑ to $\overline{XACK}$↑ Propagation Delay		24	30	ns
38	t_{PHL}	DS↓ to $\overline{OEBL}$↓, $\overline{OEBH}$↓, $\overline{OEBW}$↓ Propagation Delay		13	18	ns
39	t_{PLH}	DS↑ to $\overline{OEBL}$↑, $\overline{OEBH}$↑, $\overline{OEBW}$↑ Propagation Delay		13	18	ns
40	t_S	$\overline{ERR}$, $\overline{MERR}$ to LEO↓ Setup Time	1.5	0		ns
41	t_H	$\overline{ERR}$, $\overline{MERR}$ to LEO↓ Hold Time	6.5	4		ns
42	t_{PHL}	LEO↓ to $\overline{INTERR}$↓, $\overline{INTMERR}$↓ Propagation Delay		19	24	ns
43	t_{PLH}	$\overline{INTACK}$↓ to $\overline{INTERR}$↑, $\overline{INTMERR}$↑ Propagation Delay		23	30	ns

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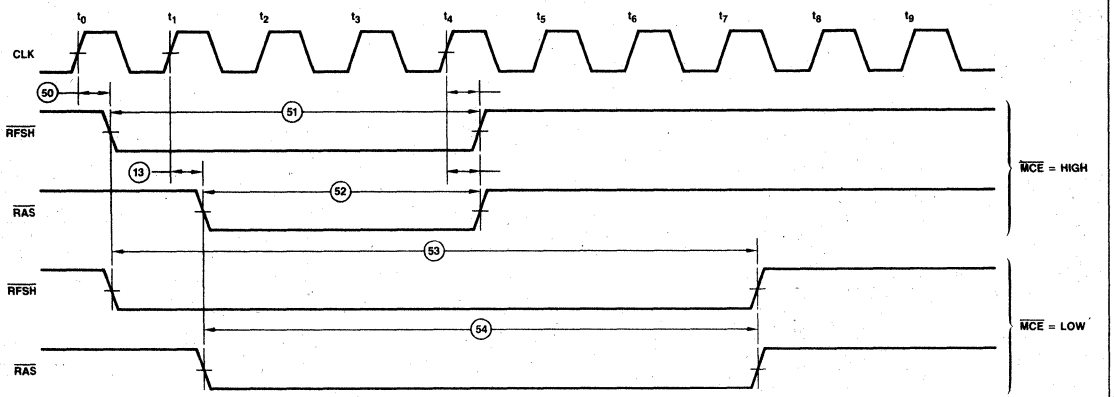
Am8163/67 SWITCHING CHARACTERISTICS (Cont.)

Parameters		Description	$T_A = +25°C$ $V_{CC} = 5.0V$ Min	Typ	Max	Units
44	t_{PLH}	LEO↓ to LERR↑, LMERR↑ Propagation Delay		30	39	ns
45	t_{PHL}	$\overline{ERRACK}$↓ to LERR↓, LMERR↓ Propagation Delay		9	14	ns
46	t_{PWL}	$\overline{INTACK}$ LOW Pulse Width	20	9		ns
47	t_{PWL}	$\overline{ERRACK}$ LOW Pulse Width	20	9		ns
48	t_S	$\overline{SUP}$↓ to $\overline{DS}$↓ Setup Time	0	−5		ns
49	t_H	$\overline{WE}$↑ to SUP↑ Hold Time	0	−10		ns
50	t_{PHL}	CLK to $\overline{RFSH}$↓ Propagation Delay		16	21	ns
51a	t_{PWL}	$\overline{RFSH}$ LOW Pulse Width ($\overline{MCE}$ = HIGH) – 8163		4tp		
51b	t_{PWL}	$\overline{RFSH}$ LOW Pulse Width ($\overline{MCE}$ = HIGH) – 8167		5tp		
52a	t_{PWL}	$\overline{RAS}$ LOW Pulse Width During Refresh ($\overline{MCE}$ = HIGH) – 8163		3tp		
52b	t_{PWL}	$\overline{RAS}$ LOW Pulse Width During Refresh ($\overline{MCE}$ = HIGH) – 8167		4tp		
53a	t_{PWL}	$\overline{RFSH}$ LOW Pulse Width ($\overline{MCE}$ = LOW) – 8163		7tp		
53b	t_{PWL}	$\overline{RFSH}$ LOW Pulse Width ($\overline{MCE}$ = LOW) – 8167		9tp		
54a	t_{PWL}	$\overline{RAS}$ LOW Pulse Width During Refresh ($\overline{MCE}$ = LOW) – 8163		6tp		
54b	t_{PWL}	$\overline{RAS}$ LOW Pulse Width During Refresh ($\overline{MCE}$ = LOW) – 8167		8tp		
55a	t_{OSC}	CLK Frequency – 8163			16	MHz
55b	t_{OSC}	CLK Frequency – 8167			22	MHz

TIMING WAVEFORMS (Cont.)

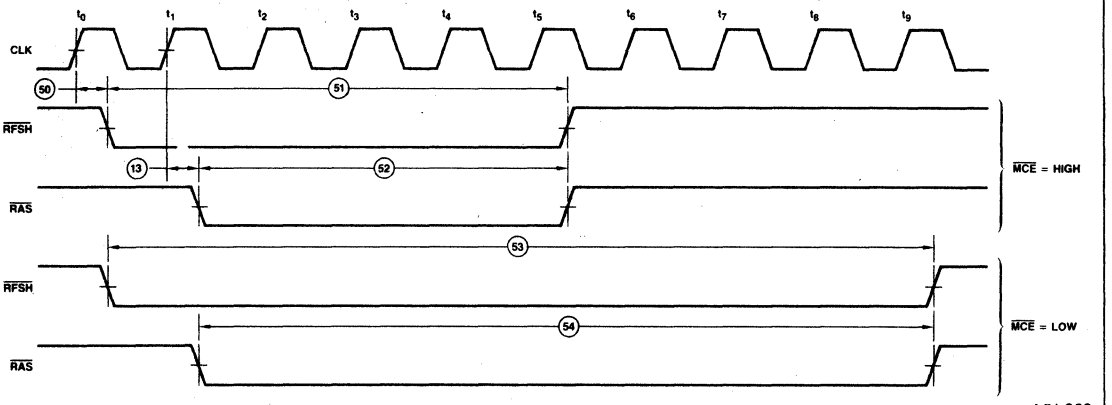
Am8163 REFRESH TIMING



AB1-059

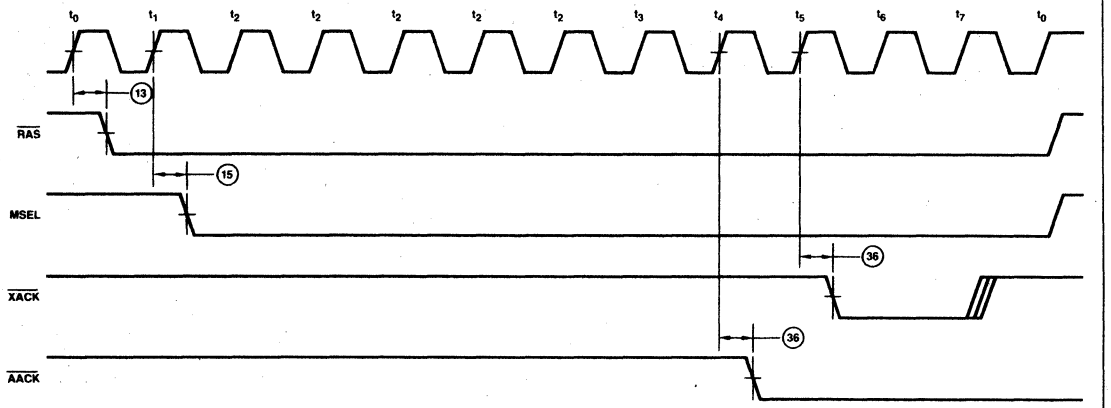
TIMING WAVEFORMS (Cont.)

Am8167 REFRESH TIMING



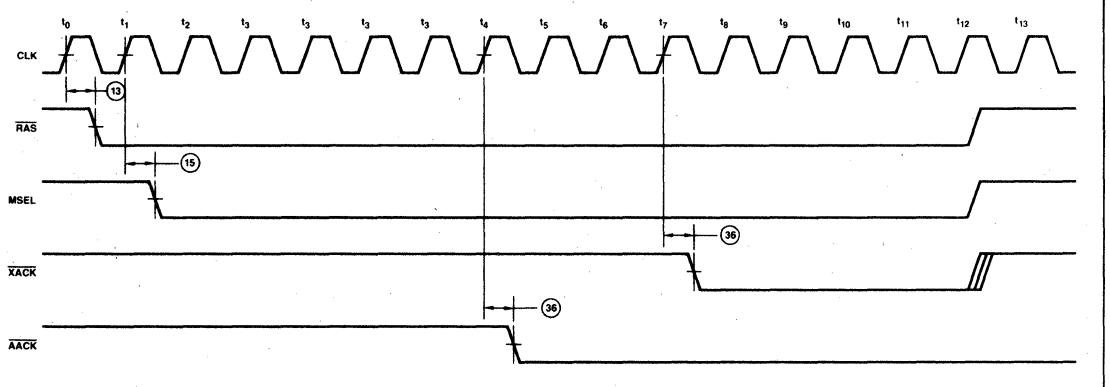
ABI-060

Am8163 MEMORY CYCLE EXTEND TIMING ($\overline{MCE}$ = LOW)



ABI-061

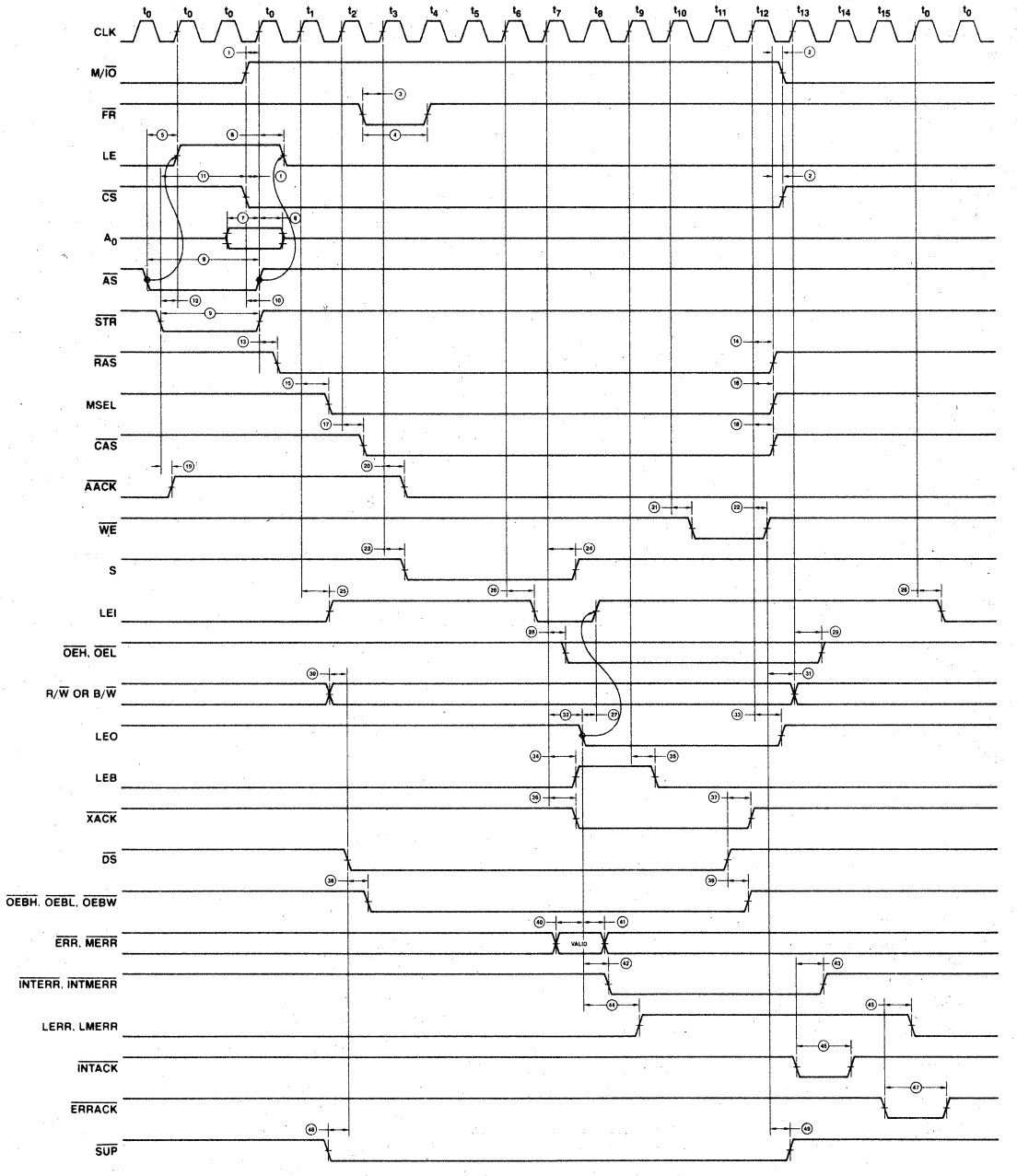
Am8167 MEMORY CYCLE EXTEND TIMING ($\overline{MCE}$ = LOW)



ABI-062

TIMING WAVEFORMS (Cont.)

Am8167 TIMING



AB1-063

Am8163/67 SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters		Description	COM'L T_A = 0 to +70°C V_{CC} = 5.0V ± 5% Min	COM'L Max	MIL T_A = −55 to +125°C V_{CC} = 5.0V ± 10% Min	MIL Max	Units
1	t_S	M/$\overline{IO}$↑ or $\overline{CS}$↓ to CLK Setup Time	5		5		ns
2	t_H	M/$\overline{IO}$↓ or $\overline{CS}$↑ to $\overline{RAS}$↑ Hold Time	5		5		ns
3	t_S	$\overline{FR}$↓ to CLK Setup Time	9		9		ns
4	t_{PWL}	$\overline{FR}$ LOW Pulse Width	tp + 10		tp + 10		ns
5	t_{PLH}	$\overline{AS}$↓ to LE↑ Propagation Delay		22		22	ns
6	t_{PHL}	$\overline{AS}$↑ to LE↓ Propagation Delay		22		22	ns
7	t_S	A0 to $\overline{AS}$↑ Setup Time	1.5		1.5		ns
8	t_H	A0 to $\overline{AS}$↑ Hold Time	10		10		ns
9	t_{PWL}	$\overline{AS}$, $\overline{STR}$ LOW Pulse Width	20		20		ns
10	t_S	M/$\overline{IO}$↑ or $\overline{CS}$↓ to $\overline{STR}$↑ Setup Time	5		5		ns
11	t_S	$\overline{CS}$↓ to $\overline{STR}$↓ Setup Time	−tp		−tp		ns
12	t_S	$\overline{STR}$↓ to CLK Setup Time	10		12		ns
13	t_{PHL}	CLK to $\overline{RAS}$↓ Propagation Delay		45		45	ns
14	t_{PLH}	CLK to $\overline{RAS}$↑ Propagation Delay		40		40	ns
15	t_{PHL}	CLK to $\overline{MSEL}$↓ Propagation Delay		25		25	ns
16	t_{PLH}	CLK to $\overline{MSEL}$↑ Propagation Delay		30		30	ns
17a	t_{PHL}	$\overline{MSEL}$↓ to $\overline{CAS}$↓ Propagation Delay − 8163	16		16		ns
17b	t_{PHL}	CLK to $\overline{CAS}$↓ Propagation Delay − 8167		25		25	ns
18a	t_{PLH}	CLK to $\overline{CAS}$↑ Propagation Delay − 8163		50		50	ns
18b	t_{PLH}	CLK to $\overline{CAS}$↑ Propagation Delay − 8167		30		30	ns
19	t_{PLH}	$\overline{STR}$↓ to $\overline{AACK}$↑ Propagation Delay		40		40	ns
20	t_{PHL}	CLK to $\overline{AACK}$ ↓ Propagation Delay		46		46	ns
21	t_{PHL}	CLK to $\overline{WE}$↓ Propagation Delay		25		25	ns
22	t_{PLH}	CLK to $\overline{WE}$↑ Propagation Delay		30		30	ns
23	t_{PHL}	CLK to S↓ Propagation Delay		25		25	ns
24a	t_{PLH}	LEI↓ to S↑ Propagation Delay − 8163	0		0		ns
24b	t_{PLH}	CLK to S↑ Propagation Delay − 8167		30		30	ns
25	t_{PLH}	CLK to LEI↑ Propagation Delay		30		30	ns
26	t_{PHL}	CLK to LEI↓ Propagation Delay		25		25	ns
27	t_{PLH}	LEO↓ to LEI↑ Propagation Delay	10		10		ns
28a	t_{PHL}	LEI↓ to $\overline{OEH}$↓, $\overline{OEL}$↓ Propagation Delay − 8163	4.0		4.0		ns
28b	t_{PHL}	CLK to $\overline{OEH}$↓, $\overline{OEL}$↓ − 8167		35		35	ns
29	t_{PLH}	CLK to $\overline{OEH}$↑, $\overline{OEL}$↑ Propagation Delay		35		35	ns
30	t_S	R/$\overline{W}$, B/$\overline{W}$ to $\overline{DS}$↓ Setup Time	0		1.0		ns
31	t_H	R/$\overline{W}$, B/$\overline{W}$ to $\overline{WE}$↑ Hold Time	0		0		ns
32	t_{PHL}	CLK to LEO↓ Propagation Delay		25		25	ns
33	t_{PLH}	CLK to LEO↑ Propagation Delay		30		30	ns
34	t_{PLH}	CLK to LEB↑ Propagation Delay		30		30	ns
35	t_{PHL}	CLK to LEB↓ Propagation Delay		35		35	ns
36	t_{PHL}	CLK to $\overline{XACK}$↓ Propagation Delay		40		41	ns
37	t_{PLH}	$\overline{DS}$↑ to $\overline{XACK}$↑ Propagation Delay		35		35	ns
38	t_{PHL}	$\overline{DS}$↓ to $\overline{OEBL}$↓, $\overline{OEBH}$↓, $\overline{OEBW}$↓ Propagation Delay		22		22	ns
39	t_{PLH}	$\overline{DS}$↑ to $\overline{OEBL}$↑, $\overline{OEBH}$↑, $\overline{OEBW}$↑ Propagation Delay		22		22	ns

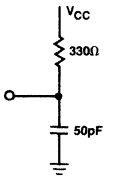
Am8163/67 SWITCHING CHARACTERISTICS (Cont.)

Parameters		Description	COM'L T_A = 0 to +70°C, V_{CC} = 5.0V ± 5% Min	COM'L Max	MIL T_A = −55 to +125°C, V_{CC} = 5.0V ± 10% Min	MIL Max	Units
40	t_S	$\overline{ERR}$, $\overline{MERR}$ to LEO↓ Setup Time	2.0		3.0		ns
41	t_H	$\overline{ERR}$, $\overline{MERR}$ to LEO↓ Hold Time	8.0		8.0		ns
42	t_{PHL}	LEO↓ to $\overline{INTERR}$↓, $\overline{INTMERR}$↓ Propagation Delay		28		28	ns
43	t_{PLH}	$\overline{INTACK}$↓ to $\overline{INTERR}$↑, $\overline{INTMERR}$↑ Propagation Delay		38		38	ns
44	t_{PLH}	LEO↓ to LERR↑, LMERR↑ Propagation Delay		46		46	ns
45	t_{PHL}	$\overline{ERRACK}$↓ to LERR↓, LMERR↓ Propagation Delay		20		20	ns
46	t_{PWL}	$\overline{INTACK}$ LOW Pulse Width	20		20		ns
47	t_{PWL}	$\overline{ERRACK}$ LOW Pulse Width	20		20		ns
48	t_S	$\overline{SUP}$↓ to $\overline{DS}$↓ Setup Time	5		5		ns
49	t_H	$\overline{WE}$↑ to $\overline{SUP}$↑ Hold Time	5		5		ns
50	t_{PHL}	CLK to $\overline{RFSH}$↓ Propagation Delay		25		25	ns
51a	t_{PWL}	$\overline{RFSH}$ LOW Pulse Width ($\overline{MCE}$ = HIGH) – 8163	4tp-3ns		4tp-3ns		
51b	t_{PWL}	$\overline{RFSH}$ LOW Pulse Width ($\overline{MCE}$ = HIGH) – 8167	5tp-3ns		5tp-3ns		
52a	t_{PWL}	$\overline{RAS}$ LOW Pulse Width During Refresh ($\overline{MCE}$ = HIGH) – 8163	3tp-3ns		3tp-3ns		
52b	t_{PWL}	$\overline{RAS}$ LOW Pulse Width During Refresh ($\overline{MCE}$ = HIGH) – 8167	4tp-3ns		4tp-3ns		
53a	t_{PWL}	$\overline{RFSH}$ LOW Pulse Width ($\overline{MCE}$ = LOW) – 8163	7tp-3ns		7tp-3ns		
53b	t_{PWL}	$\overline{RFSH}$ LOW Pulse Width ($\overline{MCE}$ = LOW) – 8167	9tp-3ns		9tp-3ns		
54a	t_{PWL}	$\overline{RAS}$ LOW Pulse Width During Refresh ($\overline{MCE}$ = LOW) – 8163	6tp-3ns		6tp-3ns		
54b	t_{PWL}	$\overline{RAS}$ LOW Pulse Width During Refresh ($\overline{MCE}$ = LOW) – 8167	8tp-3ns		8tp-3ns		
55a	f_{OSC}	CLK Frequency – 8163		16		16	MHz
55b	f_{OSC}	CLK Frequency – 8167		22		22	MHz

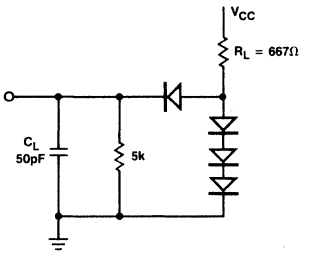
*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am8163/67 TEST LOADS

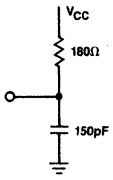
$\overline{\text{INTERR}}$,$\overline{\text{INT MERR}}$



OTHER OUTPUTS



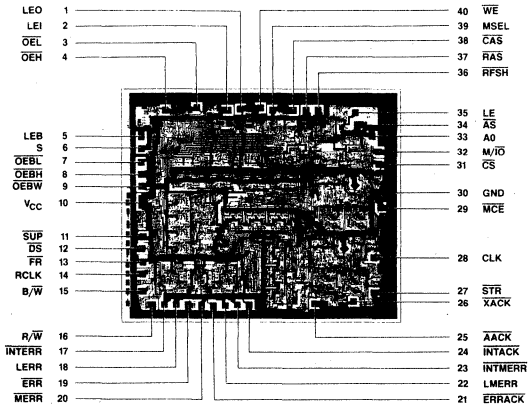
$\overline{\text{XACT}}$, $\overline{\text{AACK}}$



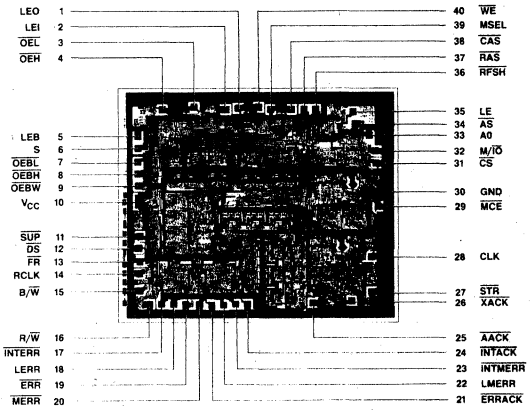
ABI-064

METALLIZATION AND PAD LAYOUT

Am8163

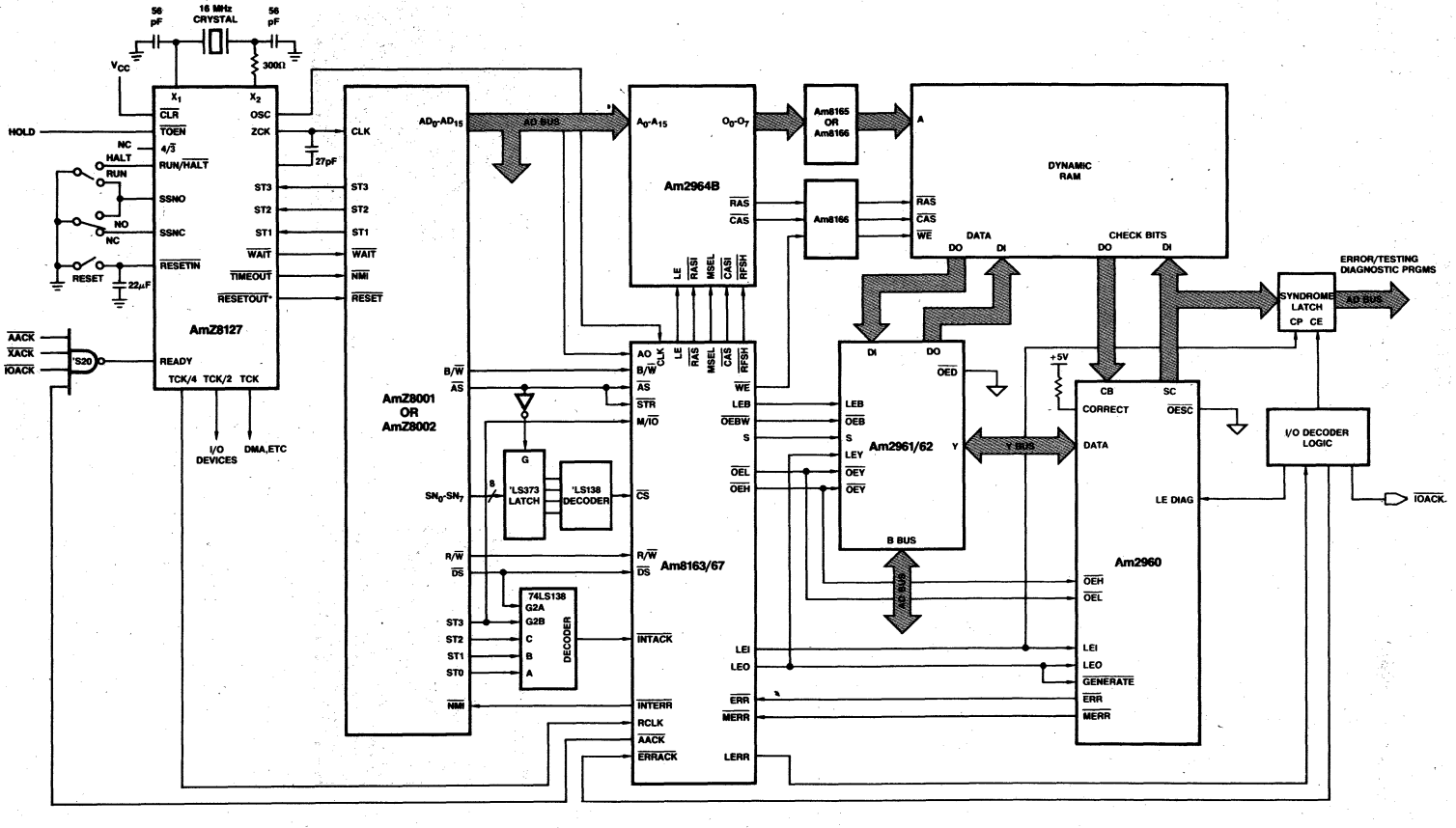


Am8167

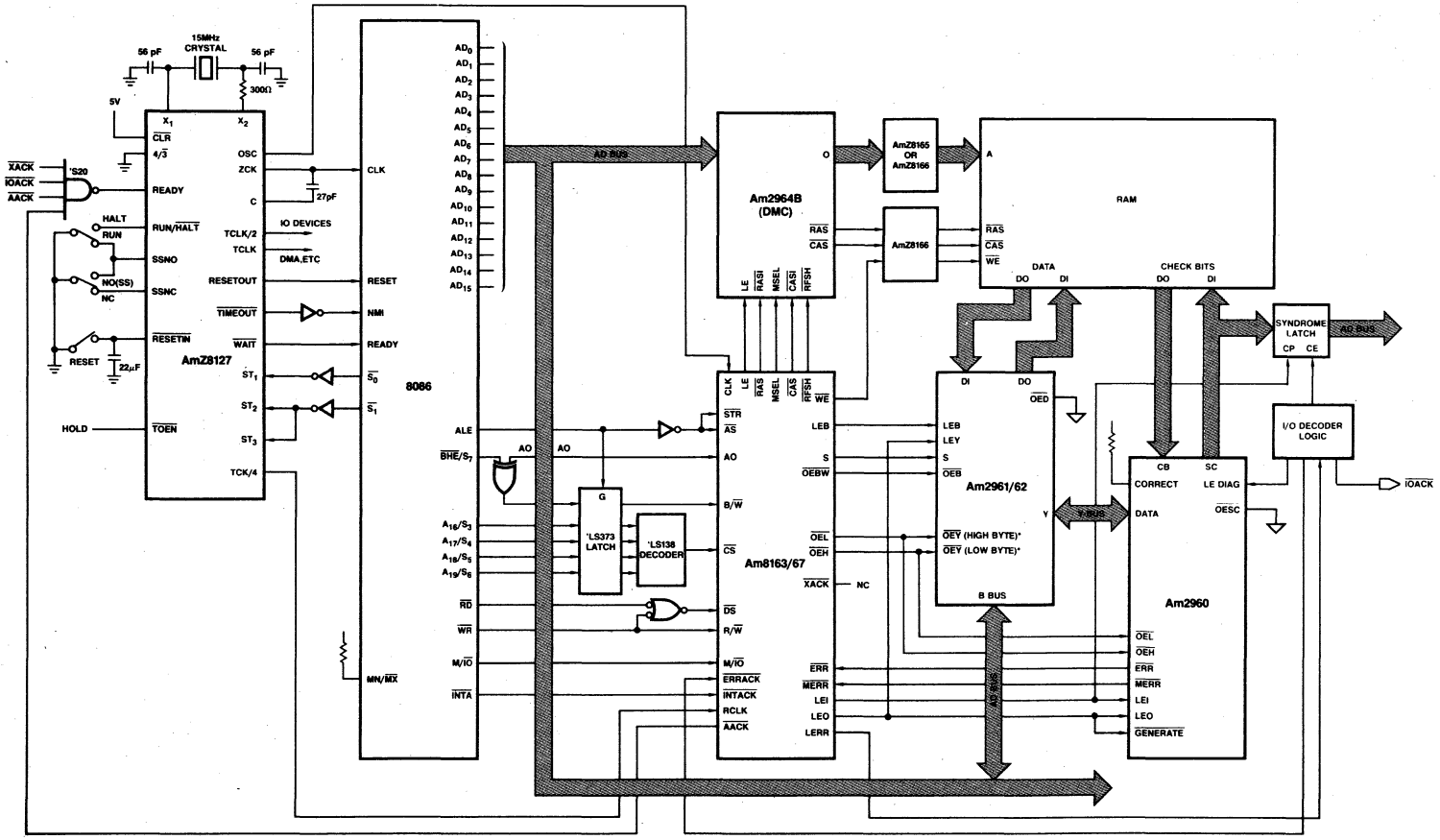


DIE SIZE 0.185″ x 0.156″

Am8163/67 APPLICATION WITH Am8001/2 AND Am8127 CLOCK GENERATOR

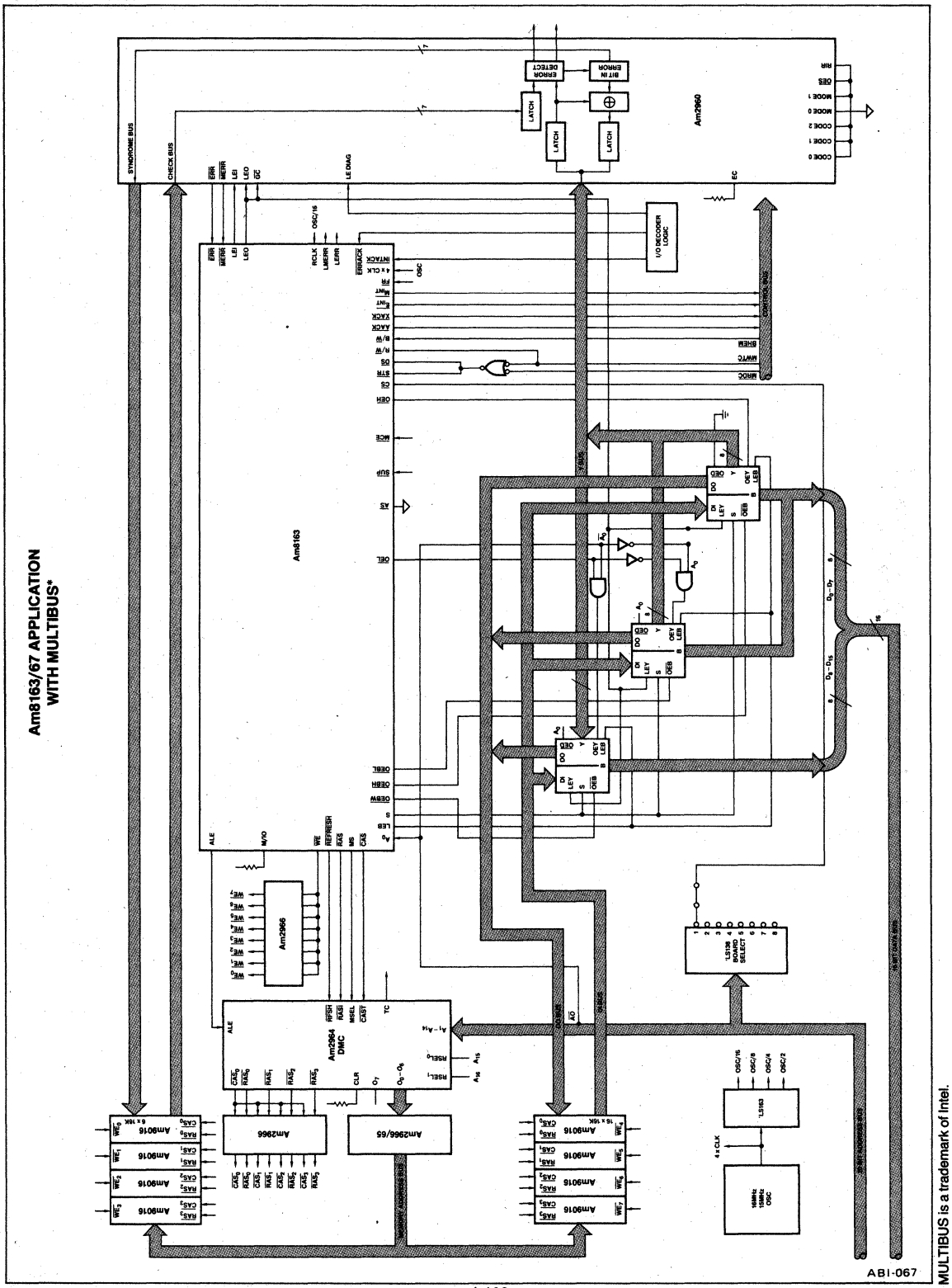


Am8163/67 APPLICATION WITH Am8086 CPU AND Am8127 CLOCK GENERATOR



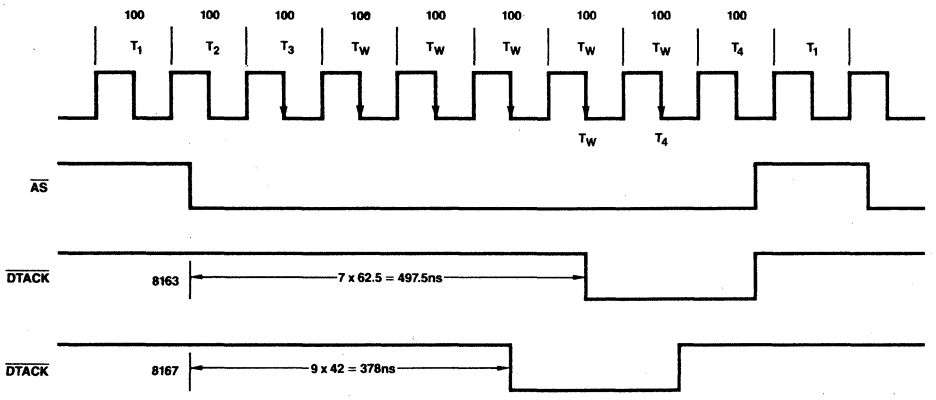
ABI-066

Am8163/67 APPLICATION WITH MULTIBUS*

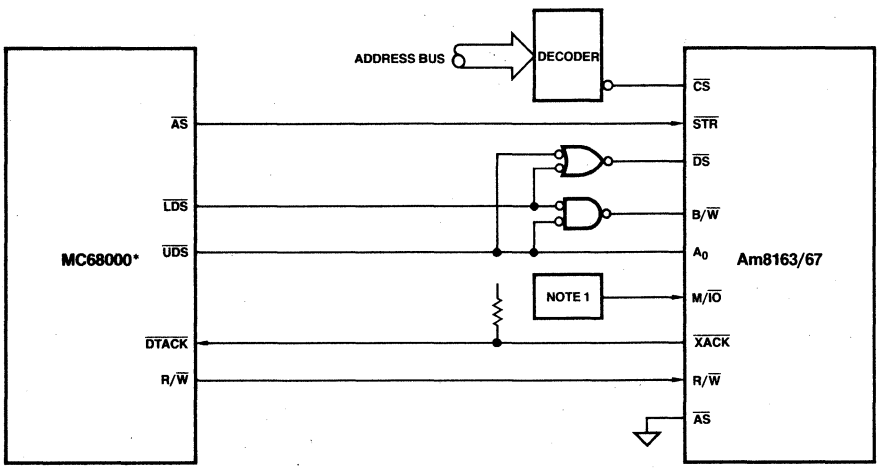


*MULTIBUS is a trademark of Intel.

Am8163/67 APPLICATION WITH MC68000



ABI-068



ABI-069

*Timing refers to 10MHz MC68000.

Note 1: M/IO may be tied HIGH or connected to an address pin. It may also be connected to an I/O port. The main consideration is not to start the 8163/67 when communicating with the 2960 Diagnostic Latch.

ORDERING INFORMATION

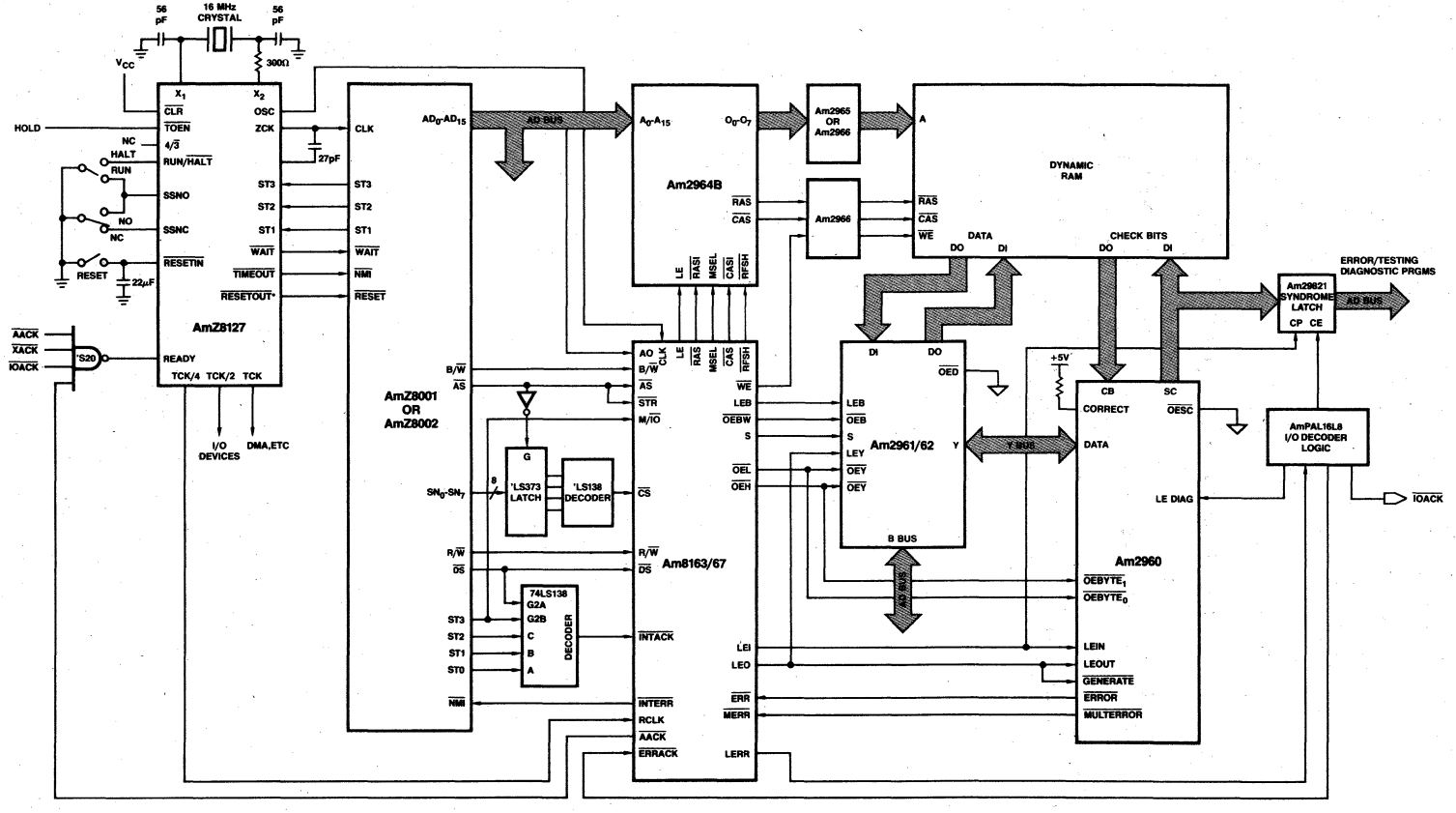
Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM8163/67DC	D-40-1	C	C-1
AM8163/67DCB	D-40-1	C	B-2 (Note 4)
AM8163/67DM	D-40-1	M	C-3
AM8163/67DMB	D-40-1	M	B-3
AM8163/67LC	L-28-1	C	C-1
AM8163/67LCB	L-28-1	C	B-2 (Note 4)
AM8163/67LM	L-28-1	M	C-3
AM8163/67LMB	L-28-1	M	B-3
AM8163/67XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM8163/67XM	Dice	M	

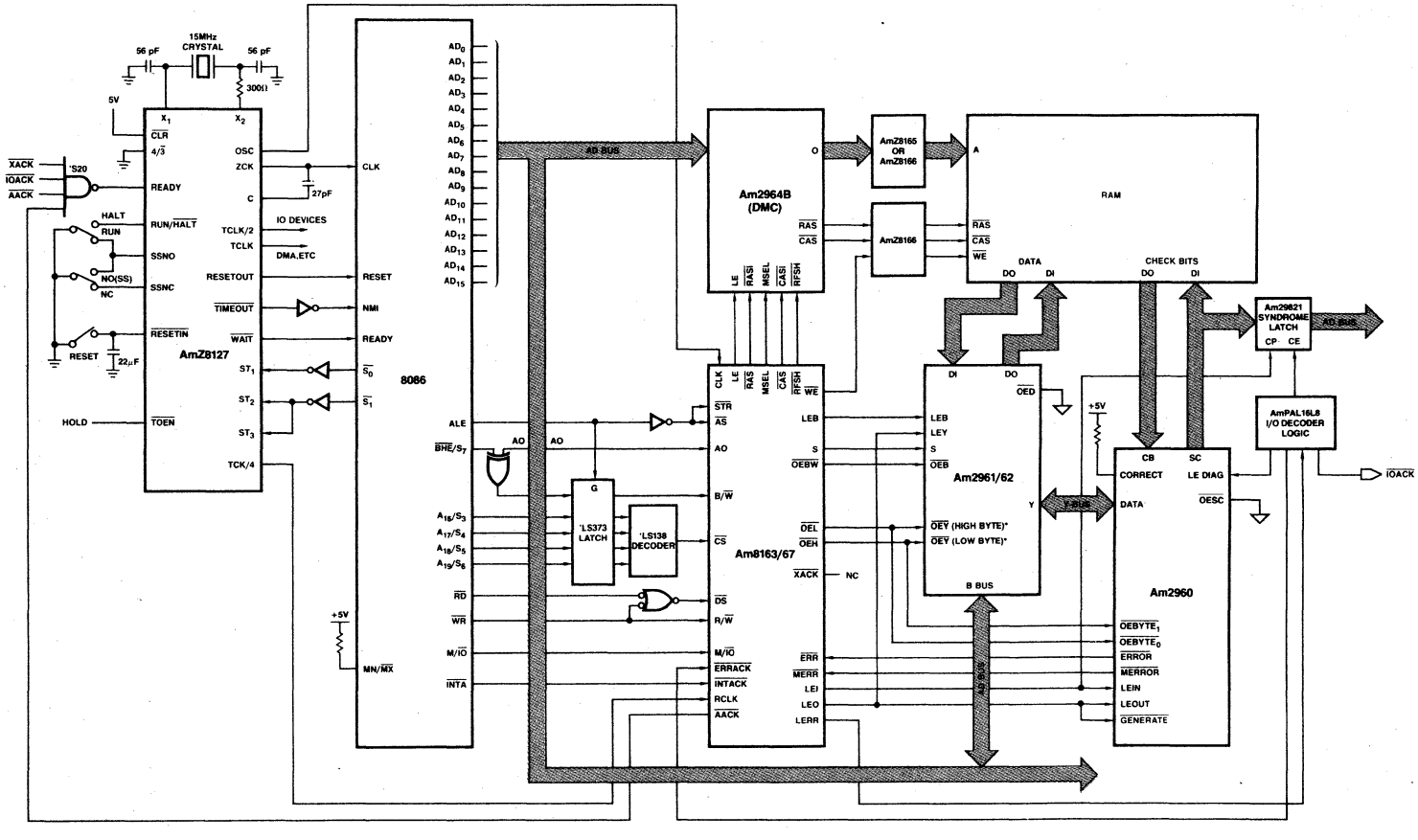
Notes: 1. D = hermetic DIP, L = Chip-Pak. Number following letter is number of leads.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 160 hour burn-in.

Typical Systems Utilizing the Am2960 Memory Support Products

Am8163/67 APPLICATION WITH Am8001/2 AND Am8127 CLOCK GENERATOR

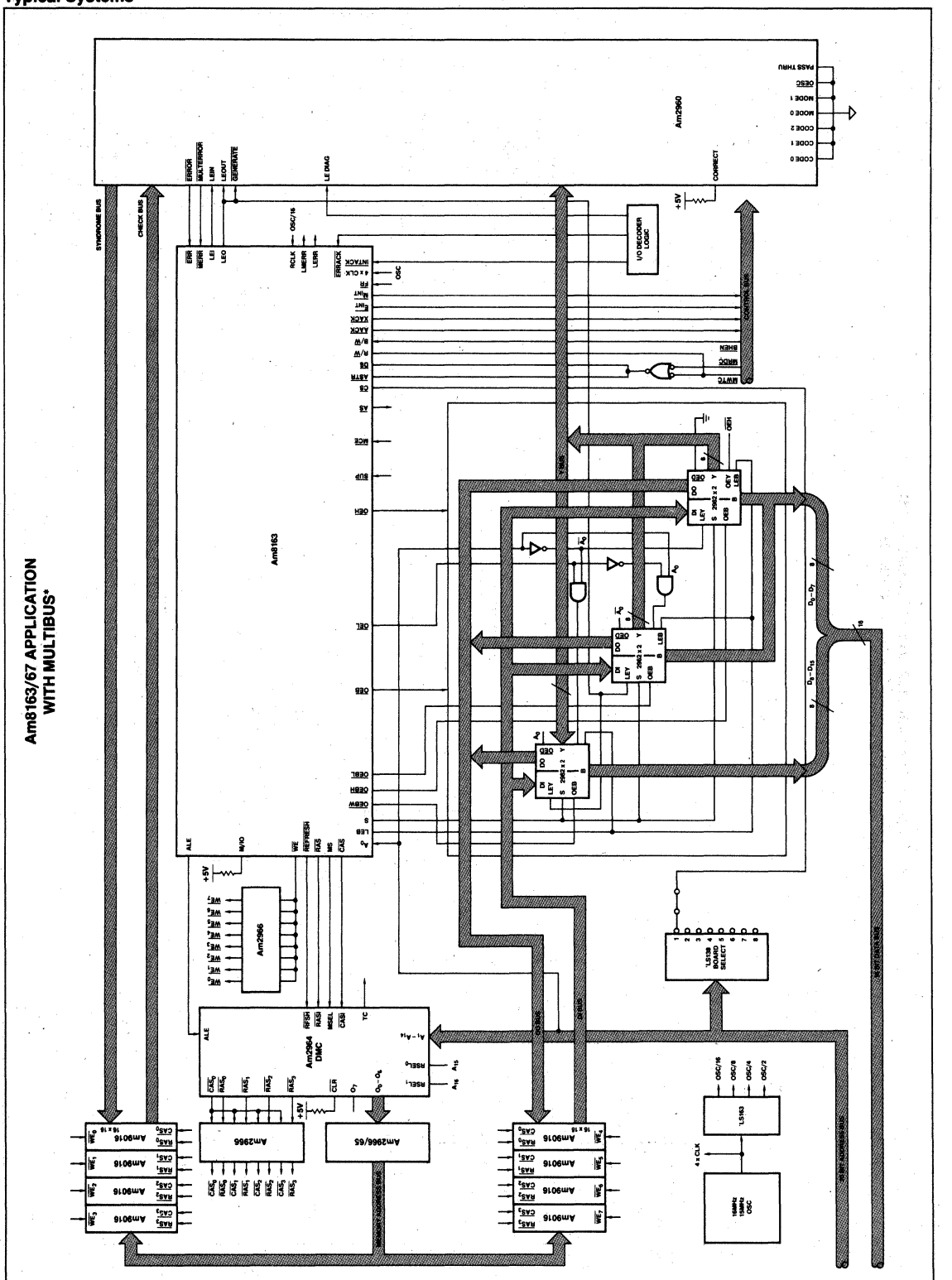


Am8163/67 APPLICATION WITH Am8086 CPU AND Am8127 CLOCK GENERATOR

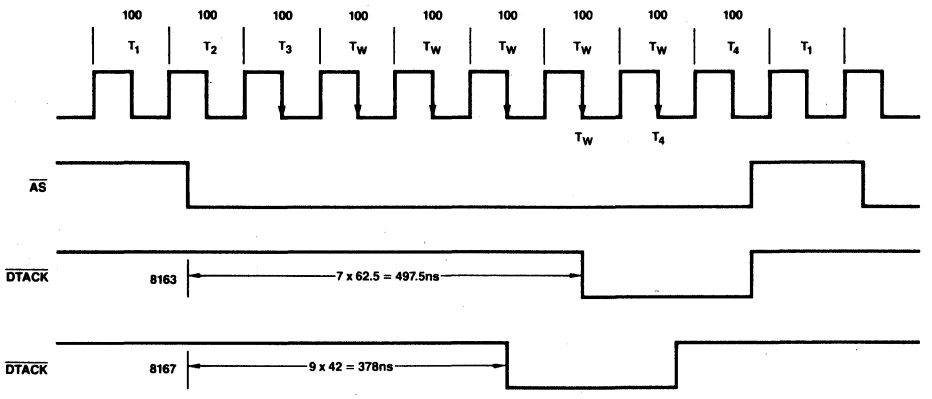


Typical Systems

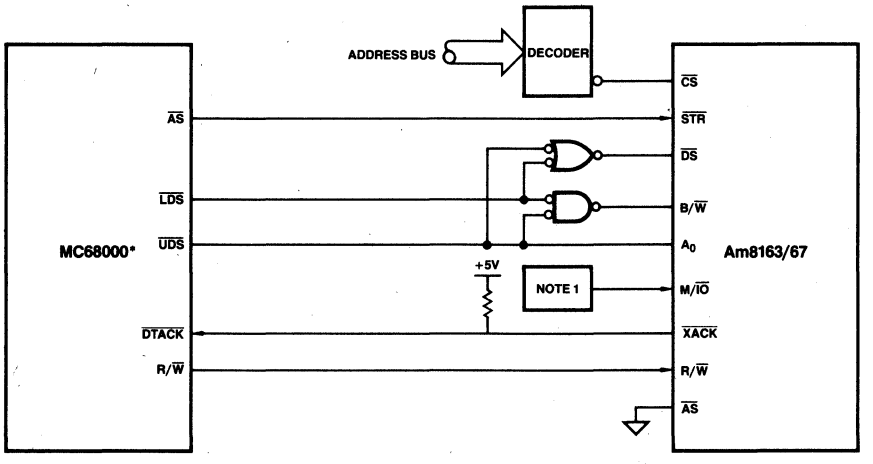
Am8163/67 APPLICATION WITH MULTIBUS*



Am8163/67 APPLICATION WITH MC68000



ABI-069



ABI-068

*Timing refers to 10MHz MC68000 (2 wait states with 8MHz 68000).

Note 1: M/$\overline{IO}$ may be tied HIGH or connected to an address pin. It may also be connected to an I/O port. The main consideration is not to start the 8163/67 when communicating with the 2960 Diagnostic Latch.

Am2900 Processors and Peripherals Family Index

Am2900 Components Continuously Become Faster and Faster

MORE SPEED: NO MORE POWER

There's a good old tried and proven way to make faster IC's – burn more power. (That's the only real difference between "LS" and "S" devices). But that solution isn't satisfactory for LSI devices like the Am2900 Family. Power is constrained to existing levels for reliability reasons.

Am2900 parts are always designed to obtain the maximum speed at a power level which is safe for the package types and operating environment of the part. To increase speeds, new technologies must be used to build faster components at no increase in power.

NEW CIRCUIT DESIGN TECHNIQUES MAKE FASTER GATES

One way to make faster components is to use new circuit design techniques. The most obvious is internal ECL, which provides very fast gates at similar power levels to LS TTL. The Am29116 reaches microcycle times of 100ns through the use of internal ECL. Other design techniques, such as low-level logic (with very small logic swings on-chip), can also provide higher speeds without introducing the time penalty of ECL to TTL conversion.

Finally, very low power gates used in non-critical speed paths make more power available for use in critical speed paths. As the 2900 Family develops, all these technologies will be used within a single component to achieve the highest speeds without increasing power. The Am2903A is one of the first products to take advantage of this mixed circuit technology.

IMPROVED PROCESS CONTROL ALLOWS TIGHTER SPECS

Today's 2900 parts are carefully characterized over a wide range of voltages, temperatures, and process parameters before an AC specification is published. As manufacturing technology improves, the process is subject to smaller run-to-run variations, so that all of the product is closer to design nominal. This makes it possible to specify parameters more closely to typical without incurring large yield losses. The first product reflecting this is the Am2903.

WHAT'S GOOD FOR THE GOOSE IS GOOD FOR THE GANDER

Many new tools in production technology are emerging, primarily spurred by the emphasis on high-speed MOS memories. The same tools, such as projection masking, also provide for smaller geometries in bipolar circuits. As MOS gets faster, so does bipolar. The Am2901C obtains its speed improvement over the Am2901B through these tools.

PROCESS TECHNOLOGY TAKES A QUANTUM LEAP

Current generation LSI/VLSI bipolar devices call for state-of-the-art processing technologies. IMOX™ ion-implanted micro-oxide technology gives the Am2901C its performance improvement over the Am2901B. IMOX also generates incredible packing densities – the Am29116 has 2500 gates on a single bipolar chip!

DESIGN FOR THE FUTURE

Every Am2900 part will undergo an evolution as new technologies become practical for production. Every part type will continuously become faster. The results are easy to observe – increases in performance at no additional cost (see Figure 1).

Most existing 2900 designs can be offered in higher performance versions simply by substitution of the 2901C for the 2901B, the 2909A for the 2909, the 2903A for the 2903, and so forth. Your 2900 design won't run out of speed in a few years. Advanced Micro Devices' 2900 Family will serve tomorrow's needs as well as today's.

Figure 1. Price/Performance Improvements

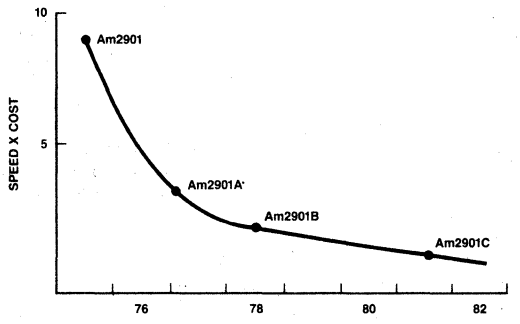


Figure 2. Bipolar Speed/Density Improvements

Am2901 FOUR-BIT MICROPROCESSOR SLICE

540 GATES
800mW
40-PIN DIP

DIE SIZE	Am2901 33,000 MILS^2	Am2901A 20,000 MILS^2	Am2901B 15,000 MILS^2	Am2901C 15,000 MILS^2
SPEED A, B G, P	80ns	65ns	50ns	**37ns**
TECHNOLOGY	LOW-POWER SCHOTTKY	DUAL LAYER METAL ION-IMPLANTATION	PROJECTION PRINTING	ECL INTERNAL TTL I/O IMOX
	1975	1977	1978	1981

IMOX is a trademark of Advanced Micro Devices.

Introduction

THREE GENERATIONS OF TTL

Transistor-transistor logic has been the dominant technology for digital circuits since it was developed in the mid-1960's. It has proven itself to be manufacturable in high volume using an extremely reliable process technology. The processes used for TTL have evolved over the years, making components smaller, faster and less expensive. Relative to a TTL gate manufactured in 1966, a gate on a circuit manufactured today occupies 1/5 the area, consumes 1/10 the power, is twice as fast and costs less than 1/100 the price.

The circuits built using TTL technology have gone through two generations; the Am2900 Family represents the beginning of the third. Each generation consists of circuits which are fundamental building blocks of systems – circuits which can be interconnected in many different ways to build many different systems. Only by producing such universal circuits can manufacturing volumes be high enough to generate the rapid cost reductions characteristic of the integrated circuit industry.

The quality which distinguishes one generation from another is the level of integration used, and, because of the level of integration, the philosophy behind the circuit.

If one draws a curve plotting the cost of an individual gate against the number of gates on a chip, Figure 1 results.

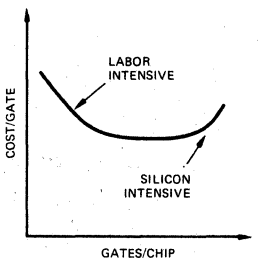


Figure 1. MPR-001

At the left, cost per gate is inversely proportional to the number of gates on the chip. The chip is small enough that it does not represent a significant portion of the cost of the product – it is virtually free. The cost of the product is composed of labor in assembly and test, the cost of processing an order, shipping and fixed overhead. Doubling the number of gates on the chip doesn't materially affect the cost so the cost per gate halves. As the number of gates per chip increases, the die begins to cost more, reversing the downward trend. As die cost dominates, the cost per gate remains relatively flat until the yield of the die begins to decline markedly. The cost per gate then begins to rise again. The lowest cost per gate is achieved at a level of integration corresponding to the flat region. This is the optimum level of integration.

As technology improves, costs are constantly reduced and the optimum level of integration occurs at more and more gates per chip.

The three curves of Figure 2 are the reason for the three generations of TTL. Each generation has consisted of fundamental system building blocks designed to take advantage of the optimum level of integration at the time.

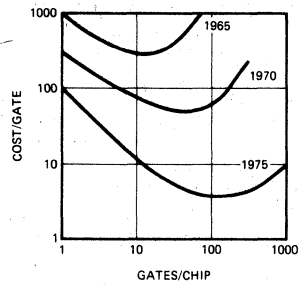


Figure 2. MPR-002

GENERATION I – SSI, 1965

In 1965, the optimum level of integration was three-to-six gates per chip. Users were delighted to buy such chips at $10-20 each. The circuits were useful in many systems. They consisted of gates – the 7400, 7410, 7420 – and, pressing the state of the art, some flip-flops. They were fundamental building blocks.

GENERATION II – MSI, 1970

Beginning around 1968, it became economical to put more gates on a chip and the industry was faced with a problem: How does one put 20 gates on a chip and build a universal building block? Clearly, one answer was to bring the inputs and outputs off chip as had been done before. But that was the wrong answer. The right answer was to redefine fundamental building blocks. The new building blocks fell into seven categories:

- Counters
- Decoders
- Multiplexers
- Operators (adders, comparators)
- Encoders
- Registers
- Latches

All systems could be defined in terms of these seven functions, and integrated circuits could be defined at the 20-50 gate/chip level which performed these functions efficiently. This, of course, is MSI. Over the last six or seven years, more and more circuits of this type have been introduced, utilizing standard gold-doped technology, low-power TTL, high-speed TTL, Schottky TTL, and now low-power Schottky TTL technology. Today, there are over 250 different MSI circuits and new ones appear every month. But in today's technology, many of these circuits are not particularly cost effective. They are too small for today's technology and their costs are labor intensive. (Labor costs do not follow traditional semiconductor pricing patterns.) In 1977, the optimum level of integration for bipolar logic was around 500 gates chip.

GENERATION III – The Am2900 Family, 1976

At a 500-gate-per-chip level of integration, one does not build counters, decoders, and multiplexers. A new definition of fundamental system functions was needed. Advanced Micro Devices has defined these eight categories:

- Data Manipulation
- Microprogram Control
- Macroprogram Control
- Priority Interrupt
- Direct Memory Access
- I/O Control
- Memory Control
- Front Panel Control

The Am2900 Family includes circuits designed to perform those functions efficiently. They are fundamental system building blocks; they contain hundreds of gates per chip; they are fast – utilizing Low-Power Schottky TTL technology and AMD's proprietary IMOX™ technology; they are expandable; they are flexible – useful in emulation; and they are driven under microprogram control.

IMOX AND ECL – THE NEXT STEP

Ever increasing device complexity placed greater and greater demands on existing process technologies. Advanced Micro Devices responded to this challenge by introducing its revolutionary IMOX ion-implanted microoxide technology in 1980. Oxide isolation generated faster transistor switching and tighter packaging. Ion-implantation meant tighter parameter control and lower power consumption. The bottom line – an unequalled combination of speed and density culminating in the Am29116 with a staggering 2500 gates-per-chip. Figure 3 shows this climb in gate density.

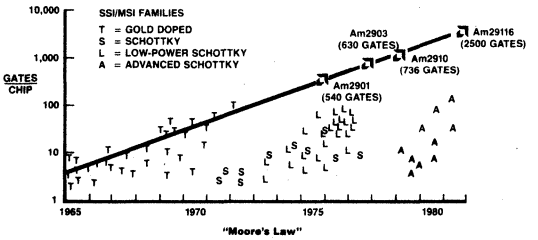


Figure 3. Am2900 Bipolar LSI/VLSI

Future refinements of IMOX and new device technologies will keep AMD on the leading edge in bipolar LSI/VLSI. Designed to take advantage of these improvements in process technology, a new family of microprogrammable 32-bit controller products will set the pace for bipolar VLSI in the mid-1980s.

THE Am2900 FAMILY

The Am2900 Family consists of a series of LSI building blocks designed for use in microprogrammed computers and controllers. Each device is designed to be expandable and sufficiently flexible to be suitable for emulation of many existing machines. It is the wide variety of machine architectures possible with the Am2900 Family which sets it apart from the fixed-instruction microprocessors such as the Am8086.

While an Am8086 can be used to build a microcomputer with only four or five packages, an Am2900 design will require 30 or 40 or more. The Am8086 design will, therefore, almost always be cheaper. But the Am8086, or any other fixed-instruction processor, can execute only one instruction set, so it is not really suitable for emulation of another machine.

Moreover, a fixed-instruction processor operates only on words of a single length, usually eight bits. An Am2900 design, on the other hand, can be constructed for any word length which is a multiple of four bits.

Many applications require specialized operations to be performed at relatively high speed. Such functions as multiply and divide and special graphic control operations, can be done in microcode 10-100 times faster than in fixed-instruction MOS processors.

MICROPROGRAMMED ARCHITECTURE

Most small processors today are being designed using a technique called microprogramming. In microprogrammed systems, a large portion of the system's control is performed by a read only memory (usually PROM) rather than large arrays of gates and flip-flops. This technique frequently reduces the package count in the controller and provides a highly ordered structure in the controller, not present when random logic is used. Moreover, microprogramming makes changes in the machines' instruction set very simple to perform – reducing the post-production engineering costs for the system substantially.

The Am2900 Family of Bipolar LSI devices has been designed for use in microprogrammed systems. Each device performs a basic system function and is driven by a set of control lines from a microinstruction.

Figure 4 illustrates a typical system architecture. There are two "sides" to the system. At the left is the control circuitry and on the right is the data manipulation circuitry. The block labeled "2901C array" consists of the ALU, scratchpad registers, data steering logic (all internal to the Am2901Cs), plus left/right shift control and carry lookahead circuit. Data is processed by moving it from main memory (not shown) into the 2901C registers, performing the required operations on it and returning the result to main memory. Memory addresses may also be generated in the 2901Cs and sent out to the memory address register (MAR). The four status bits from the 2901Cs ALU are captured in the status register after each operation.

The logic on the left side is the control section of the computer. This is where the Am2909A, 2910A, or 2911A is used. The entire system is controlled by a memory, usually PROM, which contains long words called microinstructions. Each microinstruction contains bits to control each of the data manipulation elements in the system. There are, for example, nine bits for the 2901C instruction lines, eight bits for the A and B register addresses, two or three bits to control the shifting multiplexers at the ends of the 2901C array (see Figure 19, 2901C data sheet), and bits to control the register enables on the MAR, instruction register, and various bus transceivers. When the bits in a microinstruction are applied to all the data elements and everything is clocked, then one small operation (such as a data transfer or a register-to-register add) will occur.

A "machine instruction" (such as a minicomputer instruction or an 8086 instruction) is performed by executing several microinstructions in sequence. Each microinstruction therefore contains not only bits to control the data hardware, but also bits to define the location in PROM of the next microinstruction to be executed. The fields are labeled in Figure 4 as I, CC, and BA. The I field controls the sequencer. It indicates where the next address is located – the μPC, the stack, or the direct inputs – and whether the stack is to be pushed or popped.

The CC field contains bits indicating the conditions under which the I field applies. These are compared with the condition codes in the status register and may cause modification to the I field. The comparing and modification occurs in the

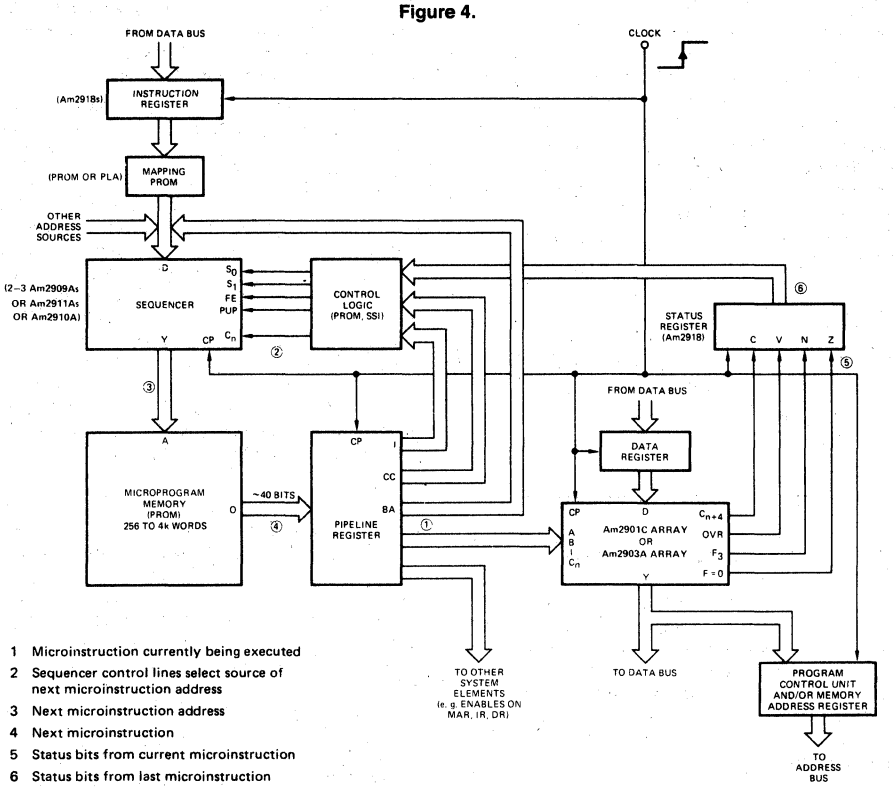
block labeled "control logic". Frequently this is a PROM or PLA. In the case of the Am2910, it is built into the chip. The BA field is a branch address or the address of a subroutine.

PIPELINING

The address for the microinstructions is generated by the sequencer, starting from a clock edge. The address goes from the sequencer to the ROM and, an access time later, the microinstruction is at the ROM outputs.

A pipeline register is a register placed on the output of the microprogram memory to essentially split the system in two. The pipeline register contains the microinstruction currently being executed ①. (Refer to the circled numbers in Figure 4.) The data manipulation control bits go out to the system elements and a portion of the microinstruction is returned to the sequencer ② to determine the address of the next microinstruction to be executed. That address ③ is sent to the ROM and the next microinstruction ④ sits at the input of the pipeline register. So while the 2901Cs are executing one instruction, the next instruction is being fetched from ROM. Note that there is no sequential logic in the sequencer between the select lines and the output. This is important because the loop ① to ② to ③ to ④ must occur during a single clock cycle. During the same time, the loop from ① to ⑤ must occur in the 2901Cs. These two paths are roughly the same (around 200ns worst case for a 16-bit system). The presence of the pipeline register allows the microinstruction fetch to occur in parallel with the data operation rather than serially, allowing the clock frequency to be doubled.

Figure 4.



1 Microinstruction currently being executed
2 Sequencer control lines select source of next microinstruction address
3 Next microinstruction address
4 Next microinstruction
5 Status bits from current microinstruction
6 Status bits from last microinstruction

The system shown in Figure 4 works as follows. A sequence of microinstructions in the PROM is executed to fetch an instruction from main memory. This requires that the program counter, often in a 2901C working register, be sent to the memory address register and incremented. The data returned from memory is loaded into the instruction register. The contents of the instruction register is passed through a PROM or PLA to generate the address of the first microinstruction which must be executed to perform the required function. A branch to this address occurs through the sequencer. Several microinstructions may be executed to fetch data from memory, perform ALU operations, test for overflow, and so forth. Then a branch will be made back to the instruction fetch cycle. At this point, there may be branches to other sections of microcode. For example, the machine might test for an interrupt here and obtain an interrupt service routine address from another mapping ROM rather than start on the next machine instruction. There are obviously many possibilities. Throughout this data book, in application notes, and within data sheets, some suggested techniques will be found.

Additional application notes are in preparation and are planned for publication. Advanced Micro Devices' Applications' staff is available to answer questions and provide technical assistance as well. They may be reached by calling (408) 732-2400, or, outside California (800) 538-8450. Ask for Am2900 Family Applications.

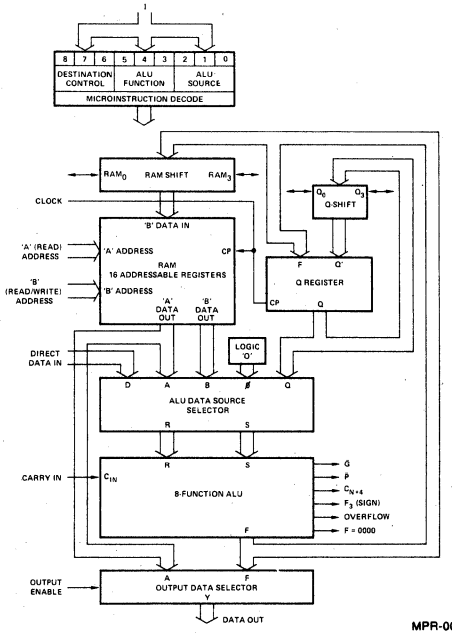
Am2901B • Am2901C • Am2901C-1

Four-Bit Bipolar Microprocessor Slice

DISTINCTIVE CHARACTERISTICS

- **Two-address architecture –**
  Independent simultaneous access to two working registers saves machine cycles.
- **Eight-function ALU –**
  Performs addition, two subtraction operations, and five logic functions on two source operands.
- **Flexible data source selection –**
  ALU data is selected from five source ports for a total of 203 source operand pairs for every ALU function.
- **Left/right shift independent of ALU –**
  Add and shift operations take only one cycle.
- **Four status flags –**
  Carry, overflow, zero, and negative.
- **Expandable –**
  Connect any number of Am2901s together for longer word lengths.
- **Microprogrammable –**
  Three groups of three bits each for source operand, ALU function, and destination control.
- **Fast –**
  Am2901C is up to 33% faster than Am2901B. The Am2901C meets or exceeds all of the specifications for the Am2901B.
- **IMOX –**
  Am2901C is processed with AMD's proprietary IMOX™ Process.

MICROPROCESSOR SLICE BLOCK DIAGRAM



MPR-004

GENERAL DESCRIPTION

The Am2901 industry standard four-bit microprocessor slice is a high-speed cascadable ALU intended for use in CPUs, peripheral controllers, and programmable microprocessors. The microinstruction flexibility of the Am2901 permits efficient emulation of almost any digital computing machine.

The device, as shown in the block diagram below, consists of a 16-word by 4-bit two-port RAM, a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The nine-bit microinstruction word is organized into three groups of three bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable with full look ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU. AMD's ion-implanted micro-oxide (IMOX) processing is used to fabricate the 40-lead LSI chip.

The Am2901C is a plug-in replacement for the Am2901B, but is 33% faster than the Am2901B. The Am2901C-1 is a speed selected version of the Am2901C offering a 20–30% speed improvement on critical paths.

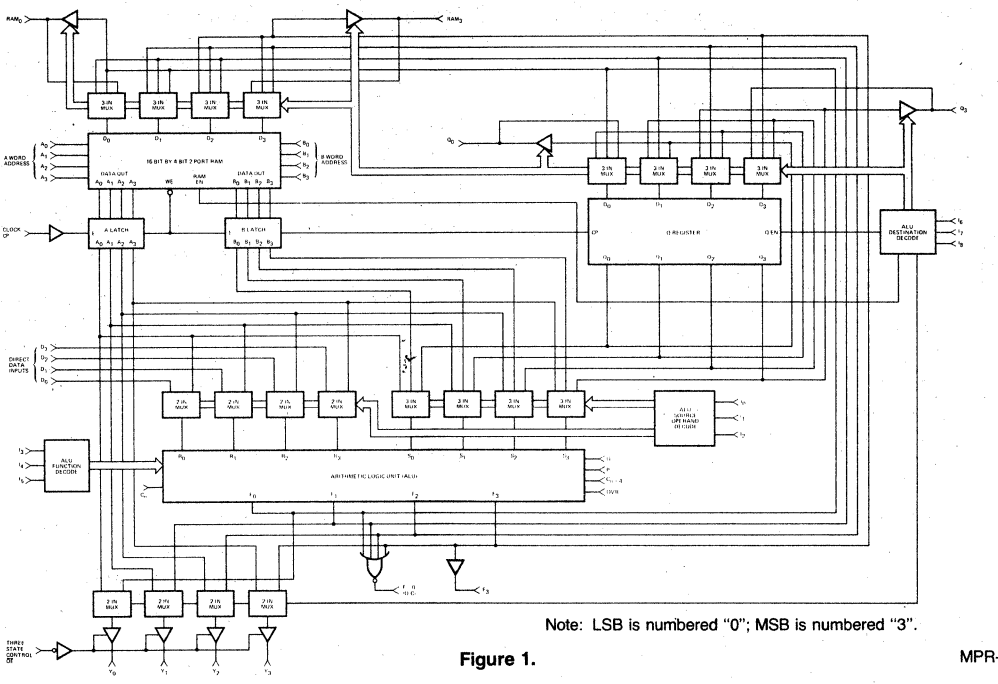
RELATED DEVICES

Part No.	Description
Am2902A	Carry Look-Ahead Generator
Am2904	Status and Shift Control Unit
Am2910A	Microprogram Controller
Am2914	Vectored Priority Interrupt Controller
Am2917A	Bus Transceiver
Am2918	Pipeline Register
Am2920	Octal Register
Am2922	Condition Code MUX
Am2925	System Clock Generator
Am2940	DMA Address Generator
Am2952	Bidirectional I/O Port
Am27S35	Registered PROM

For applications information see the last part of this data sheet and chapters III and IV of **Bit Slice Microprocessor Design,** by Mick and Brick, McGraw Hill Publishers.

IMOX is a trademark of Advanced Micro Devices

DETAILED Am2901C MICROPROCESSOR BLOCK DIAGRAM



Note: LSB is numbered "0"; MSB is numbered "3".

Figure 1. MPR-005

PIN DEFINITIONS

A_{0-3} The four address inputs to the register stack used to select one register whose contents are displayed through the A-port.

B_{0-3} The four address inputs to the register stack used to select one register whose contents are displayed through the B-port and into which new data can be written when the clock goes LOW.

I_{0-8} The nine instruction control lines. Used to determine what data sources will be applied to the ALU (I_{012}), what function the ALU will perform (I_{345}), and what data is to be deposited in the Q-register or the register stack (I_{678}).

Q_3 RAM_3 A shift line at the MSB of the Q register (Q_3) and the register stack (RAM_3). Electrically these lines are three-state outputs connected to TTL inputs internal to the device. When the destination code on I_{678} indicates an up shift (octal 6 or 7) the three-state outputs are enabled and the MSB of the Q register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM_3 pin. Otherwise, the three-state outputs are OFF (high-impedance) and the pins are electrically LS-TTL inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of the Q register (octal 4) and RAM (octal 4 or 5).

Q_0 RAM_0 Shift lines like Q_3 and RAM_3, but at the LSB of the Q-register and RAM. These pins are tied to the Q_3 and RAM_3 pins of the adjacent device to transfer data between devices for up and down shifts of the Q register and ALU data.

D_{0-3} Direct data inputs. A four-bit data field which may be selected as one of the ALU data sources for entering data into the device. D_0 is the LSB.

Y_{0-3} The four data outputs. These are three-state output lines. When enabled, they display either the four outputs of the ALU or the data on the A-port of the register stack, as determined by the destination code I_{678}.

$\overline{OE}$ Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF; when $\overline{OE}$ is LOW, the Y outputs are active (HIGH or LOW).

$\overline{G}$, $\overline{P}$ The carry generate and propagate outputs of the internal ALU. These signals are used with the Am2902 for carry-lookahead.

OVR Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.

F = 0 This is an open collector output which goes HIGH (OFF) if the data on the four ALU outputs F_{0-3} are all LOW. In positive logic, it indicates the result of an ALU operation is zero.

F_3 The most significant ALU output bit.

C_n The carry-in to the internal ALU.

C_{n+4} The carry-out of the internal ALU.

CP The clock input. The Q register and register stack outputs change on the clock LOW-to-HIGH transition. The clock LOW time is internally the write enable to the 16 x 4 RAM which compromises the "master" latches of the register stack. While the clock is LOW, the "slave" latches on the RAM outputs are closed, storing the data previously on the RAM outputs. This allows synchronous master-slave operation of the register stack.

ARCHITECTURE

A detailed block diagram of the bipolar microprogrammable microprocessor structure is shown in Figure 1. The circuit is a four-bit slice cascadable to any number of bits. Therefore, all data paths within the circuit are four bits wide. The two key elements in the Figure 1 block diagram are the 16-word by 4-bit 2-port RAM and the high-speed ALU.

Data in any of the 16 words of the Random Access Memory (RAM) can be read from the A-port of the RAM as controlled by the 4-bit A address field input. Likewise, data in any of the 16 words of the RAM as defined by the B address field input can be simultaneously read from the B-port of the RAM. The same code can be applied to the A select field and B select field in which case the identical file data will appear at both the RAM A-port and B-port outputs simultaneously.

When enabled by the RAM write enable (RAM EN), new data is always written into the file (word) defined by the B address field of the RAM. The RAM data input field is driven by a 3-input multiplexer. This configuration is used to shift the ALU output data (F) if desired. This three-input multiplexer scheme allows the data to be shifted up one bit position, shifted down one bit position, or not shifted in either direction.

The RAM A-port data outputs and RAM B-port data outputs drive separate 4-bit latches. These latches hold the RAM data while the clock input is LOW. This eliminates any possible race conditions that could occur while new data is being written into the RAM.

The high-speed Arithmetic Logic Unit (ALU) can perform three binary arithmetic and five logic operations on the two 4-bit input words R and S. The R input field is driven from a 2-input multiplexer, while the S input field is driven from a 3-input multiplexer. Both multiplexers also have an inhibit capability; that is, no data is passed. This is equivalent to a "zero" source operand.

Referring to Figure 1, the ALU R-input multiplexer has the RAM A-port and the direct data inputs (D) connected as inputs. Likewise, the ALU S-input multiplexer has the RAM A-port, the RAM B-port and the Q register connected as inputs.

This multiplexer scheme gives the capability of selecting various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. These five inputs, when taken two at a time, result in ten possible combinations of source operand pairs. These combinations include AB, AD, AQ, A0, BD, BQ, B0, DQ, D0 and Q0. It is apparent that AD, AQ and A0 are somewhat redundant with BD, BQ and B0 in that if the A address and B address are the same, the identical function results. Thus, there are only seven completely non-redundant source operand pairs for the ALU. The Am2901 microprocessor implements eight of these pairs. The microinstruction inputs used to select the ALU source operands are the I_0, I_1, and I_2 inputs. The definition of I_0, I_1, and I_2 for the eight source operand combinations are as shown in Figure 2. Also shown is the octal code for each selection.

The two source operands not fully described as yet are the D input and Q input. The D input is the four-bit wide direct data field input. This port is used to insert all data into the working registers inside the device. Likewise, this input can be used in the ALU to modify any of the internal data files. The Q register is a separate 4-bit file intended primarily for multiplication and division routines but it can also be used as an accumulator or holding register for some applications.

The ALU itself is a high-speed arithmetic/logic operator capable of performing three binary arithmetic and five logic functions. The I_3, I_4, and I_5 microinstruction inputs are used to select the ALU function. The definition of these inputs is shown in Figure 3. The octal code is also shown for reference. The normal technique for cascading the ALU of several devices is in a look-ahead carry mode. Carry generate, $\overline{G}$, and carry propagate, $\overline{P}$, are outputs of the device for use with a carry-look-ahead-generator such as the Am2902. A carry-out, C_{n+4}, is also generated and is available as an output for use as the carry flag in a status register. Both carry-in (C_n) and carry-out (C_{n+4}) are active HIGH.

The ALU has three other status-oriented outputs. These are F_3, F = 0, and overflow (OVR). The F_3 output is the most significant (sign) bit of the ALU and can be used to determine positive or negative results without enabling the three-state data outputs. F_3 is non-inverted with respect to the sign bit output Y_3. The F = 0 output is used for zero detect. It is an open-collector output and can be wire OR'ed between microprocessor slices. F = 0 is HIGH when all F outputs are LOW. The overflow output (OVR) is used to flag arithmetic operations that exceed the available two's complement number range. The overflow output (OVR) is HIGH when overflow exists. That is, when C_{n+3} and C_{n+4} are not the same polarity.

The ALU data output is routed to several destinations. It can be a data output of the device and it can also be stored in the RAM or the Q register. Eight possible combinations of ALU destination functions are available as defined by the I_6, I_7, and I_8 microinstruction inputs. These combinations are shown in Figure 4.

The four-bit data output field (Y) features three-state outputs and can be directly bus organized. An output control ($\overline{OE}$) is used to enable the three-state outputs. When $\overline{OE}$ is HIGH, the Y outputs are in the high-impedance state.

A two-input multiplexer is also used at the data output such that either the A-port of the RAM or the ALU outputs (F) are selected at the device Y outputs. This selection is controlled by the I_6, I_7, and I_8 microinstruction inputs. Refer to Figure 4 for the selected output for each microinstruction code combination.

As was discussed previously, the RAM inputs are driven from a three-input multiplexer. This allows the ALU outputs to be entered non-shifted, shifted up one position (X2) or shifted down one position (÷2). The shifter has two ports; one is labeled RAM_0 and the other is labeled RAM_3. Both of these ports consist of a buffer-driver with a three-state output and an input to the multiplexer. Thus, in the shift up mode, the RAM_3 buffer is enabled and the RAM_0 multiplexer input is enabled. Likewise, in the shift down mode, the RAM_0 buffer and RAM_3 input are enabled. In the no-shift mode, both buffers are in the high-impedance state and the multiplexer inputs are not selected. This shifter is controlled from the I_6, I_7 and I_8 microinstruction inputs as defined in Figure 4.

Similarly, the Q register is driven from a 3-input multiplexer. In the no-shift mode, the multiplexer enters the ALU data into the Q register. In either the shift-up or shift-down mode, the multiplexer selects the Q register data appropriately shifted up or down. The Q shifter also has two ports; one is labeled Q_0 and the other is Q_3. The operation of these two ports is similar to the RAM shifter and is also controlled from I_6, I_7, and I_8 as shown in Figure 4.

The clock input to the Am2901 controls the RAM, the Q register, and the A and B data latches. When enabled, data is clocked into the Q register on the LOW-to-HIGH transition of the clock. When the clock input is HIGH, the A and B latches are open and will pass whatever data is present at the RAM outputs. When the clock input is LOW, the latches are closed and will retain the last data entered. If the RAM-EN is enabled, new data will be written into the RAM file (word) defined by the B address field when the clock input is LOW.

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FUNCTIONAL TABLES

	MICRO CODE				ALU SOURCE OPERANDS	
Mnemonic	I_2	I_1	I_0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	O	Q
ZB	L	H	H	3	O	B
ZA	H	L	L	4	O	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	O

Figure 2. ALU Source Operand Control.

	MICRO CODE				ALU	SYMBOL
Mnemonic	I_5	I_4	I_3	Octal Code	Function	
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S − R
SUBS	L	H	L	2	R Minus S	R − S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R}$ ∧ S
EXOR	H	H	L	6	R EX-OR S	R ∀ S
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \forall S}$

Figure 3. ALU Function Control.

	MICRO CODE				RAM FUNCTION		Q-REG. FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
Mnemonic	I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0	RAM_3	Q_0	Q_3
QREG	L	L	L	0	X	NONE	NONE	F → Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F → B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F → B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F_0	IN_3	Q_0	IN_3
RAMD	H	L	H	5	DOWN	F/2 → B	X	NONE	F	F_0	IN_3	Q_0	X
RAMQU	H	H	L	6	UP	2F → B	UP	2Q → Q	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	UP	2F → B	X	NONE	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state
B = Register Addressed by B inputs.
UP is toward MSB, DOWN is toward LSB.

Figure 4. ALU Destination Control.

OCTAL I_{210}	OCTAL I_{543} ALU Source / ALU Function	0	1	2	3	4	5	6	7
		A, Q	A, B	O, Q	O, B	O, A	D, A	D, Q	D, O
0	C_n = L, R Plus S	A+Q	A+B	Q	B	A	D+A	D+Q	D
	C_n = H	A+Q+1	A+B+1	Q+1	B+1	A+1	D+A+1	D+Q+1	D+1
1	C_n = L, S Minus R	Q−A−1	B−A−1	Q−1	B−1	A−1	A−D−1	Q−D−1	−D−1
	C_n = H	Q−A	B−A	Q	B	A	A−D	Q−D	−D
2	C_n = L, R Minus S	A−Q−1	A−B−1	−Q−1	−B−1	−A−1	D−A−1	D−Q−1	D−1
	C_n = H	A−Q	A−B	−Q	−B	−A	D−A	D−Q	D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
6	R EX-OR S	A ∀ Q	A ∀ B	Q	B	A	D ∀ A	D ∀ Q	D
7	R EX-NOR S	$\overline{A \forall Q}$	/ $\overline{A \forall B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \forall A}$	$\overline{D \forall Q}$	$\overline{D}$

+ = Plus; − = Minus; ∨ = OR; ∧ = AND; ∀ = EX-OR

Figure 5. Source Operand and ALU Function Matrix.

SOURCE OPERANDS AND ALU FUNCTIONS

There are eight source operand pairs available to the ALU as selected by the I_0, I_1, and I_2 instruction inputs. The ALU can perform eight functions; five logic and three arithmetic. The I_3, I_4, and I_5 instruction inputs control this function selection. The carry input, C_n, also affects the ALU results when in the arithmetic mode. The C_n input has no effect in the logic mode. When I_0 through I_5 and C_n are viewed together, the matrix of Figure 5 results. This matrix fully defines the ALU/source operand function for each state.

The ALU functions can also be examined on a "task" basis, i.e., add, subtract, AND, OR, etc. In the arithmetic mode, the carry will affect the function performed while in the logic mode, the carry will have no bearing on the ALU output. Figure 6 defines the various logic operations that the Am2901 can perform and Figure 7 shows the arithmetic functions of the device. Both carry-in LOW (C_n = 0) and carry-in HIGH (C_n = 1) are defined in these operations.

Octal I_{543}, I_{210}	Group	Function
4 0	AND	$A \wedge Q$
4 1		$A \wedge B$
4 5		$D \wedge A$
4 6		$D \wedge Q$
3 0	OR	$A \vee Q$
3 1		$A \vee B$
3 5		$D \vee A$
3 6		$D \vee Q$
6 0	EX-OR	$A \veebar Q$
6 1		$A \veebar B$
6 5		$D \veebar A$
6 6		$D \veebar Q$
7 0	EX-NOR	$\overline{A \veebar Q}$
7 1		$\overline{A \veebar B}$
7 5		$\overline{D \veebar A}$
7 6		$\overline{D \veebar Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A} \wedge Q$
5 1		$\overline{A} \wedge B$
5 5		$\overline{D} \wedge A$
5 6		$\overline{D} \wedge Q$

Figure 6. ALU Logic Mode Functions.

Octal	C_n = 0 (Low)		C_n = 1 (High)	
I_{543}, I_{210}	Group	Function	Group	Function
0 0	ADD	A+Q	ADD plus one	A+Q+1
0 1		A+B		A+B+1
0 5		D+A		D+A+1
0 6		D+Q		D+Q+1
0 2	PASS	Q	Increment	Q+1
0 3		B		B+1
0 4		A		A+1
0 7		D		D+1
1 2	Decrement	Q–1	PASS	Q
1 3		B–1		B
1 4		A–1		A
2 7		D–1		D
2 2	1's Comp.	–Q–1	2's Comp. (Negate)	–Q
2 3		–B–1		–B
2 4		–A–1		–A
1 7		–D–1		–D
1 0	Subtract (1's Comp)	Q–A–1	Subtract (2's Comp)	Q–A
1 1		B–A–1		B–A
1 5		A–D–1		A–D
1 6		Q–D–1		Q–D
2 0		A–Q–1		A–Q
2 1		A–B–1		A–B
2 5		D–A–1		D–A
2 6		D–Q–1		D–Q

Figure 7. ALU Arithmetic Mode Functions.

LOGIC FUNCTIONS FOR G, P, C_{n+4}, AND OVR

The four signals G, P, C_{n+4}, and OVR are designed to indicate carry and overflow conditions when the Am2901 is in the add or subtract mode. The table below indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to Figure 2.

Definitions (+ = OR)

$P_0 = R_0 + S_0$ $\quad G_0 = R_0S_0$

$P_1 = R_1 + S_1$ $\quad G_1 = R_1S_1$

$P_2 = R_2 + S_2$ $\quad G_2 = R_2S_2$

$P_3 = R_3 + S_3$ $\quad G_3 = R_3S_3$

$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_n$

$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

I_{543}	Function	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$	C_4	$C_3 \forall C_4$
1	S − R	← Same as R + S equations, but substitute $\overline{R_i}$ for R_i in definitions →			
2	R − S	← Same as R + S equations, but substitute $\overline{S_i}$ for S_i in definitions →			
3	R ∨ S	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0} + C_n$	$\overline{P_3P_2P_1P_0} + C_n$
4	R ∧ S	LOW	$\overline{G_3 + G_2 + G_1 + G_0}$	$G_3 + G_2 + G_1 + G_0 + C_n$	$G_3 + G_2 + G_1 + G_0 + C_n$
5	$\overline{R}$ ∧ S	LOW	← Same as R ∧ S equations, but substitute $\overline{R_i}$ for R_i in definitions →		
6	R ∀ S	← Same as $\overline{R \forall S}$, but substitute $\overline{R_i}$ for R_i in definitions →			
7	$\overline{R \forall S}$	$G_3 + G_2 + G_1 + G_0$	$G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0 (G_0 + \overline{C_n})}$	See note

Note: $[\overline{P}_2+\overline{G}_2\overline{P}_1+\overline{G}_2\overline{G}_1\overline{P}_0+\overline{G}_2\overline{G}_1\overline{G}_0C_n] \forall [\overline{P}_3+\overline{G}_3\overline{P}_2+\overline{G}_3\overline{G}_2\overline{P}_1+\overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0+\overline{G}_3\overline{G}_2\overline{G}_1\overline{G}_0C_n]$ + = OR

Figure 8.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

OPERATING RANGE

Part Number Suffix	V_{CC}	Temperature
PC, PCB, DC, DCB XC	4.75V to 5.25V	T_A = 0°C to +70°C
DM, DMB FM, FMB XM	4.50V to 5.50V	T_C = −55°C to +125°C

Figure 9.

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

(Group A, Subgroups 1, 2, and 3)

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}		I_{OH} = −1.6mA Y_0, Y_1, Y_2, Y_3	2.4			Volts
				I_{OH} = −1.0mA, C_{n+4}	2.4			
				I_{OH} = −800μA, OVR, $\overline{P}$	2.4			
				I_{OH} = −600μA, F_3	2.4			
				I_{OH} = −600μA $RAM_{0,3}$, $Q_{0,3}$	2.4			
				I_{OH} = −1.6mA, $\overline{G}$	2.4			
I_{CEX}	Output Leakage Current for F = 0 Output	V_{CC} = MIN., V_{OH} = 5.5V, V_{IN} = V_{IH} or V_{IL}					250	μA
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Y_0, Y_1, Y_2, Y_3	I_{OL} = 20mA (COM'L)			0.5	Volts
				I_{OL} = 16mA (MIL)			0.5	
			$\overline{G}$, F = 0	I_{OL} = 16mA			0.5	
			C_{n+4}	I_{OL} = 10mA			0.5	
			OVR, $\overline{P}$	I_{OL} = 8.0mA			0.5	
			F_3, $RAM_{0,3}$, $Q_{0,3}$	I_{OL} = 6.0mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 7)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 7)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V		Clock, $\overline{OE}$			−0.36	mA
				A_0, A_1, A_2, A_3			−0.36	
				B_0, B_1, B_2, B_3			−0.36	
				D_0, D_1, D_2, D_3			−0.72	
				I_0, I_1, I_2, I_6, I_8			−0.36	
				I_3, I_4, I_5, I_7			−0.72	
				$RAM_{0,3}$, $Q_{0,3}$ (Note 4)			−0.8	
				C_n			−3.6	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V		Clock, $\overline{OE}$			20	μA
				A_0, A_1, A_2, A_3			20	
				B_0, B_1, B_2, B_3			20	
				D_0, D_1, D_2, D_3			40	
				I_0, I_1, I_2, I_6, I_8			20	
				I_3, I_4, I_5, I_7			40	
				$RAM_{0,3}$, $Q_{0,3}$ (Note 4)			100	
				C_n			200	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = MAX.		Y_0, Y_1, Y_2, Y_3 V_O = 2.4V			50	μA
				V_O = 0.5V			−50	
				$RAM_{0,3}$ $Q_{0,3}$ V_O = 2.4V (Note 4)			100	
				V_O = 0.5V (Note 4)			−800	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = MAX. + 0.5V, V_O = 0.5V		$Y_0, Y_1, Y_2, Y_3, \overline{G}$	−30		−85	mA
				C_{n+4}	−30		−85	
				OVR, $\overline{P}$	−30		−85	
				F_3	−30		−85	
				$RAM_{0,3}$, $Q_{0,3}$	−30		−85	
I_{CC}	Power Supply Current (Note 6)	V_{CC} = MAX.	COM'L and MIL	T_A = 25°C		160	250	mA
			COM'L Only	T_A = 0°C to +70°C			265	
				T_A = +70°C			220	
			MIL Only	T_C = −55°C to +125°C			280	
				T_C = +125°C			198	

Notes:
1. V_{CC} conditions shown as MIN. or MAX., refer to the military (±10%) or commercial (±5%) V_{CC} limits.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be stored at a time. Duration of the short circuit test should not exceed one second.
4. These are three-state outputs internally connected to TTL inputs. Input characteristics are measured with I_{678} in a state such that the three-state output is OFF.
5. "MIL" = Am2901CXM, DM, FM, LM. "COM'L" = Am2901CXC, PC, DC, LC.
6. Worst case I_{CC} is measured at the lowest temperature in the specified operating range.
7. These input levels provide zero noise immunity and should only be static tested in a noise-free environment, (not functionally tested).

Figure 10.

I. Am2901C Guaranteed Commercial Range Performance

The tables below specify the guaranteed performance of the Am2901C over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2901CPC
Am2901CDC
Am2901CLC

A. Cycle Time and Clock Characteristics.

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.)	31ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	32MHz
Minimum Clock LOW Time	15ns
Minimum Clock HIGH Time	15ns
Minimum Clock Period	31ns

B. Combinational Propagation Delays.
C_L = 50pF

To Output / From Input	Y	F3	Cn+4	$\overline{G}$, $\overline{P}$	F=0	OVR	RAM0 RAM3	Q0 Q3
A, B Address	40	40	40	37	40	40	40	–
D	30	30	30	30	38	30	30	–
Cn	22	22	20	–	25	22	25	–
I012	35	35	35	37	37	35	35	–
I345	35	35	35	35	38	35	35	–
I678	25	–	–	–	–	–	26	26
A Bypass ALU (I = 2XX)	35	–	–	–	–	–	–	–
Clock ↓	35	35	35	35	35	35	35	28

C. Set-up and Hold Times Relative to Clock (CP) Input.

Input	CP: Set-up Time Before H → L	Hold Time After H → L	Set-up Time Before L → H	Hold Time After L → H
A, B Source Address	15	1 (Note 3)	30, 15 + T_{PWL} (Note 4)	1
B Destination Address	15	Do Not Change		1
D	–	–	25	0
Cn	–	–	20	0
I012	–	–	30	0
I345	–	–	30	0
I678	10	Do Not Change		0
RAM0, 3, Q0, 3	–	–	12	0

D. Output Enable/Disable Times.
Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$	Y	23	23

Notes:

1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. **Normally A and B are not changed during the clock LOW time.**
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes **all** the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

II. Am2901C Guaranteed Military Range Performance

The tables below specify the guaranteed performance of the Am2901B over the military operating range of −55°C to +125°C, with V_{CC} from 4.5V to 5.5V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2901CDM
Am2901CFM
Am2901CLM

A. Cycle Time and Clock Characteristics.

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.)	32ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	31MHz
Minimum Clock LOW Time	15ns
Minimum Clock HIGH Time	15ns
Minimum Clock Period	32ns

B. Combinational Propagation Delays.
C_L = 50pF

To Output / From Input	Y	F3	Cn+4	$\overline{G}$, $\overline{P}$	F=0	OVR	RAM0 RAM3	Q0 Q3
A, B Address	48	48	48	44	48	48	48	
D	37	37	37	34	40	37	37	
Cn	25	25	21		28	25	28	
I012	40	40	40	44	44	40	40	
I345	40	40	40	40	40	40	40	
I678	29						29	29
A Bypass ALU (I = 2XX)	40							
Clock ↓	40	40	40	40	40	40	40	33

C. Set-up and Hold Times Relative to Clock (CP) Input.

Input	CP: Set-up Time Before H → L	Hold Time After H → L	Set-up Time Before L → H	Hold Time After L → H
A, B Source Address	15	2 (Note 3)	30, 15 + T_{PWL} (Note 4)	2
B Destination Address	15	Do Not Change		2
D			25	0
Cn			20	0
I012			30	0
I345			30	0
I678	10	Do Not Change		0
RAM0, 3, Q0, 3			12	0

D. Output Enable/Disable Times.
Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$	Y	25	25

Notes:
1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. **Normally A and B are not changed during the clock LOW time.**
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes **all** the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

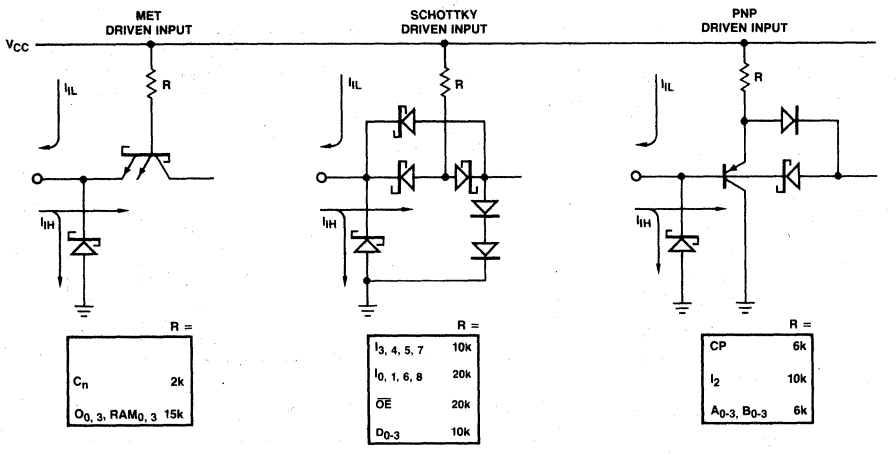
IV. Am2901B Guaranteed Commercial Range Performance

The Am2901C meets or exceeds all of the specifications for the earlier Am2901B and Am2901A. Parts may still be ordered and marked as Am2901B or Am2901A.

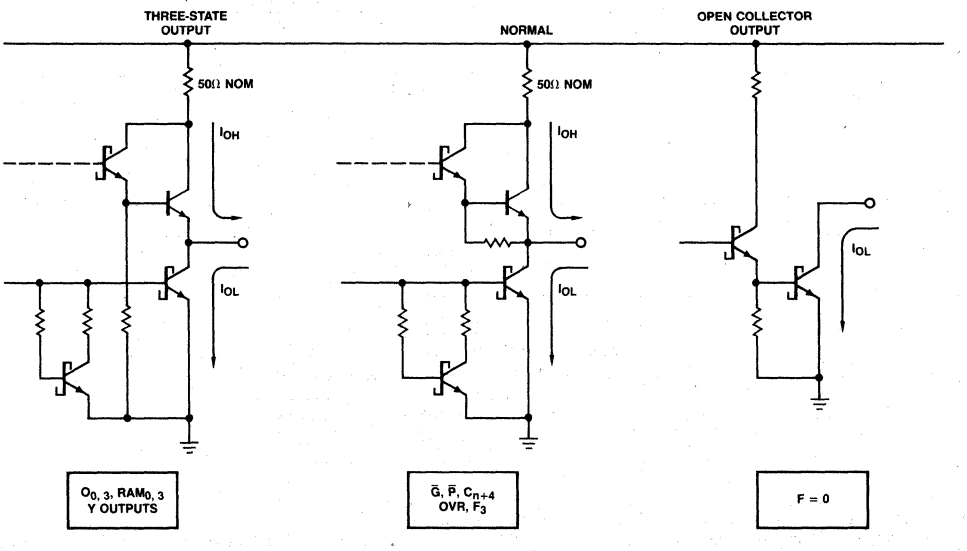
V. Am2901B Guaranteed Military Range Performance

The Am2901C meets or exceeds all of the specifications for the earlier Am2901B and Am2901A. Parts may still be ordered and marked as Am2901B or Am2901A.

TTL INPUT/OUTPUT CURRENT INTERFACES



$C_I \approx 5.0pF$, all inputs

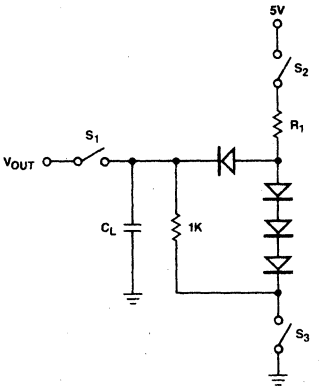


$C_O \approx 5.0pF$, all outputs

Figure 11.

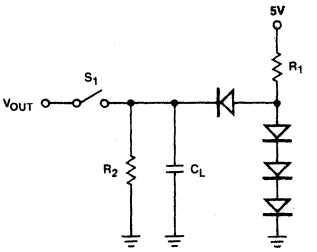
TEST OUTPUT LOAD CONFIGURATIONS FOR Am2901C

A. THREE-STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

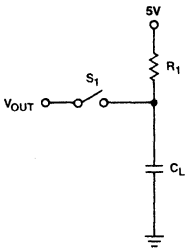
B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

C. OPEN-COLLECTOR OUTPUTS



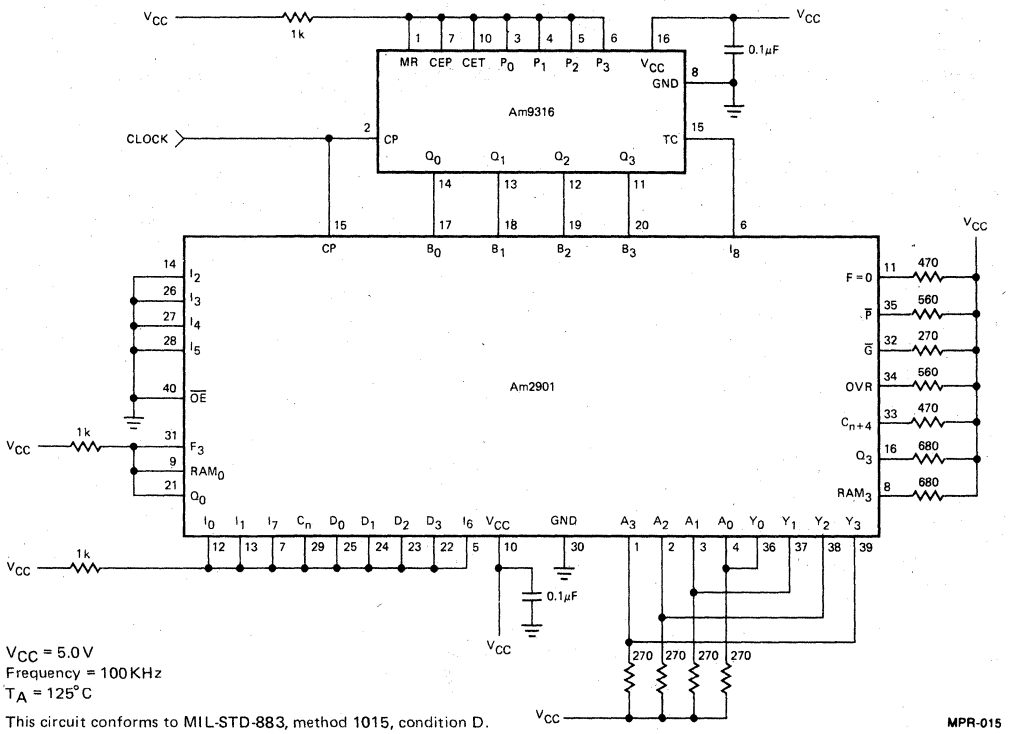
$$R_1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2901C (DIP)

Pin #	Pin Label	Test Circuit	R_1	R_2
8	RAM_3	A	560	1K
9	RAM_0	A	560	1K
11	F = 0	C	270	–
16	Q_3	A	560	1K
21	Q_0	A	560	1K
31	F_3	B	620	3.9K
32	G	B	220	1.5K
33	C_{n+4}	B	360	2.4K
34	OVR	B	470	3K
35	P	B	470	3K
36–39	Y_{0-3}	A	220	1K

LIFE TEST AND BURN-IN CIRCUIT FOR MILITARY CLASS B PARTS.



(Contact Factory for Commercial Burn-in Conditions)

Figure 12.

Notes on Testing

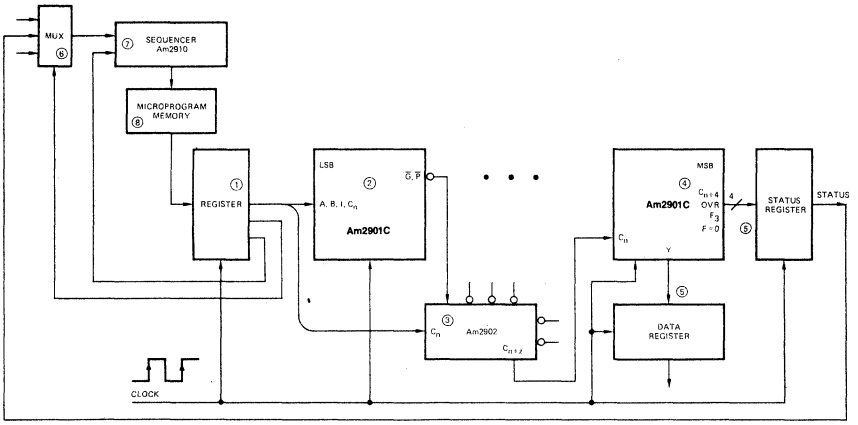
Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful.

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5-8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100's of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

For additional information on testing, see section
"Guidelines on Testing Am2900 Family Devices"
in the Bipolar Microprocessor Logic and Interface Data Book.

MINIMUM CYCLE TIME CALCULATIONS FOR 16-BIT SYSTEMS

Speeds used in calculations for parts other than Am2901C are representative for available MSI parts.



Pipelined System. Add without Simultaneous Shift. MPR-010

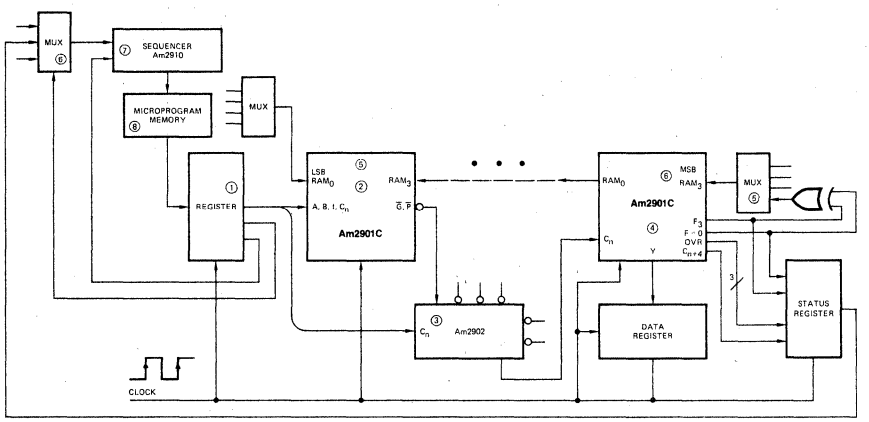
DATA LOOP

	① Register	Clock to Output	9
+	② 2901C	A, B to $\overline{G}$, $\overline{P}$	37
+	③ 2902	$\overline{G}_0$, $\overline{P}_0$ to C_{n+z}	10
+	④ 2901C	C_n to C_{n+4}, OVR, F_3, F = 0, Y	25
+	⑤ Register	Set-up Time	2
			83ns

CONTROL LOOP

	① Register	Clock to Output	9
+	⑥ MUX	Select to Output	13
+	⑦ 2910	CC to Output	45
+	⑧ PROM	Access Time	40
+	① Register	Set-up Time	2
			109ns

Minimum clock period = 109ns



Pipelined System. Simultaneous Add and Shift Down. MPR-011

DATA LOOP

	① Register	Clock to Output	9
+	② 2901C	A, B to $\overline{G}$, $\overline{P}$	37
+	③ 2902	$\overline{G}_0$, $\overline{P}_0$ to C_{n+z}	10
+	④ 2901	C_n to F_3, OVR	25
+	⑤ XOR and MUX		21
+	⑥ 2901	RAM_3 Set-up	12
			114ns

CONTROL LOOP

	① Register	Clock to Output	9
+	⑥ MUX	Select to Output	13
+	⑦ 2910	CC to Output	45
+	⑧ PROM	Access Time	40
+	① Register	Set-up Time	2
			109ns

Minimum clock period = 114ns

Figure 13.

III. Am2901C-1 Switching Characteristics

The Am2901C-1 is a speed selected version of the Am2901C offering a 20–30% speed improvement on critical paths.

A. Cycle Time and Clock Characteristics.

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.)	
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	
Minimum Clock LOW Time	
Minimum Clock HIGH Time	
Minimum Clock Period	

B. Combinational Propagation Delays.

C_L = 50pF

To Output / From Input	Y	F3	Cn+4	$\overline{G}$, $\overline{P}$	F=0	OVR	RAM0 RAM3	Q0 Q3
A, B Address								
D								
Cn								
I012								
I345								
I678								
A Bypass ALU (I = 2XX)								
Clock ↓								

C. Set-up and Hold Times Relative to Clock (CP) Input.

Input	CP: Set-up Time Before H → L	Hold Time After H → L	Set-up Time Before L → H	Hold Time After L → H
A, B Source Address				
B Destination Address				
D				
Cn				
I012				
I345				
I678				
RAM0, 3, Q0, 3				

D. Output Enable/Disable Times.

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable

Notes:

1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. **Normally A and B are not changed during the clock LOW time.**
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes **all** the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

ORDERING INFORMATION

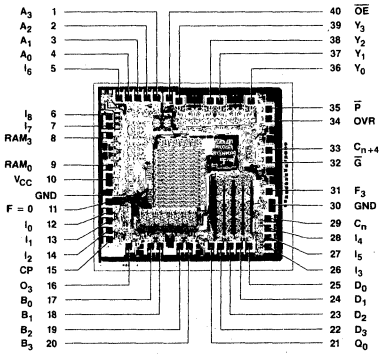
Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2901B (Note 5)	Am2901C	Am2901C-1 (Note 6)	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2901BPC	AM2901CPC		P-40	C	C-1
AM2901BDC	AM2901CDC		D-40	C	C-1
AM2901BDC-B	AM2901CDC-B		D-40	C	B-2 (Note 4)
AM2901BDM	AM2901CDM	FUTURE	D-40	M	C-3
AM2901BDM-B	AM2901CDM-B		D-40	M	B-3
AM2901BFM	AM2901CFM		F-42	M	C-3
AM2901BFM-B	AM2901CFM-B		F-42	M	B-3
	AM2901CLC		L-44	C	C-1
	AM2901CLM		L-44	M	C-3
	AM2901CLM-B		L-44	M	B-3
AM2901BXC	AM2901CXC		Dice	C	Visual Inspection to MIL-STD-883 Method 2010B
AM2901BXM	AM2901CXM		Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B (in Bipolar Microprocessor Logic and Interface Data Book) for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A (in Bipolar Microprocessor Logic and Interface Data Book) for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.
5. Am2901B orders may be shipped with Am2901C die with the package marked Am2901B.
6. When available.

5

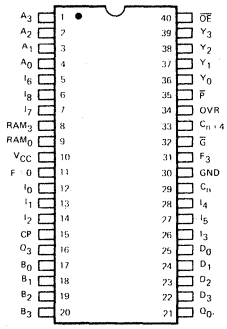
METALLIZATION AND PAD LAYOUT



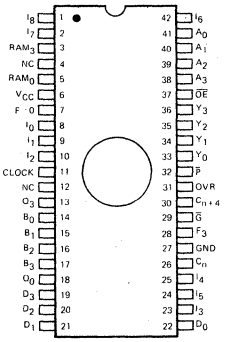
DIE SIZE 0.130" x 0.123"

CONNECTION DIAGRAMS – Top Views

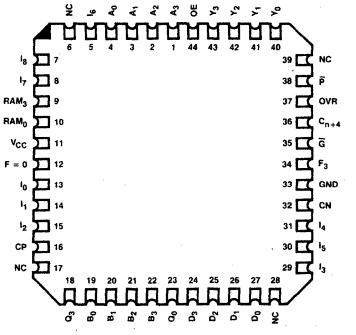
P-40, D-40



F-42



Chip-Pak™ L-44-1



Note: Pin 1 is marked for orientation.

Figure 14.

Using the Am2901

BASIC SYSTEM ARCHITECTURE

The Am2901 is designed to be used in microprogrammed systems. The nine instruction lines, the A and B addresses, and the D data inputs normally will all come from registers clocked at the same time as the Am2901. The register inputs come from a ROM or PROM – the "microprogram store." This memory contains sequences of microinstructions, typically 28 to 40 bits wide, which apply the proper control signals to the Am2901s and other circuits to execute the desired operation.

The address lines of the microprogram store are driven from the Am2901 microprogram sequencer. This device has facilities for storing an address, incrementing an address, jumping to any address, and linking subroutines. The Am2901 is controlled by some of the bits coming from the microprogram store. Essentially these bits are the "next instruction" control.

Note that with the microprogram register in-between the microprogram memory store and the Am2901s, an instruction accessed on one cycle is executed on the next cycle. As one instruction is executed, the next instruction is being read from microprogram memory. In this configuration, system speed is improved because the execution time in the Am2901s occurs in parallel with the access time of the microprogram store. Without the "pipeline register," these two functions must occur serially.

EXPANSION OF THE Am2901

The Am2901 is a four-bit CPU slice. Any number of Am2901s can be interconnected to form CPUs of 12, 16, 24, 36 or more bits, in four-bit increments. Figure 16 illustrates the interconnection of three Am2901s to form a 12-bit CPU, using ripple carry. Figure 17 illustrates a 16-bit CPU using carry lookahead, and Figure 18 is the general carry lookahead scheme for long words.

With the exception of the carry interconnection, all expansion schemes are the same. Refer to Figure 16. The Q_3 and RAM_3 pins are bidirectional left/right shift lines at the MSB of the device. For all devices except the most significant, these lines are connected to the Q_0 and RAM_0 pins of the adjacent more significant device. These connections allow the Q-registers of all Am2901s to be shifted left or right as a contiguous n-bit register, and also allow the ALU output data to be shifted left or right as a contiguous n-bit word prior to storage in the RAM. At the LSB and MSB of the CPU, the shift pins should be connected to three-state multiplexers which can be controlled by the microcode to select the appropriate input signals to the shift inputs. (See Figure 19)

The open collector F = 0 outputs of all the Am2901s are connected together and to a pull-up resistor. This line will go HIGH if and only if the ouput of the ALU contains all zeroes. Most systems will use this line as the Z (zero) bit of the processor status word.

The overflow and F_3 pins are generally used only at the most significant end of the array, and are meaningful only when two's complement signed arithmetic is used. The overflow pin is the

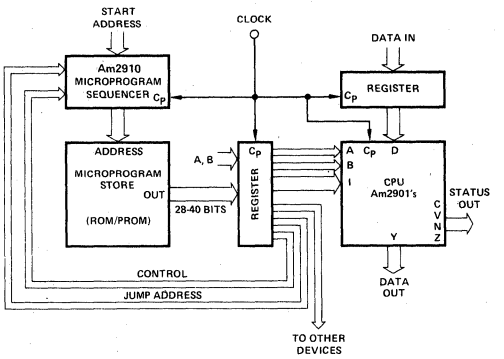


Figure 15. Microprogrammed Architecture Around Am2901s.

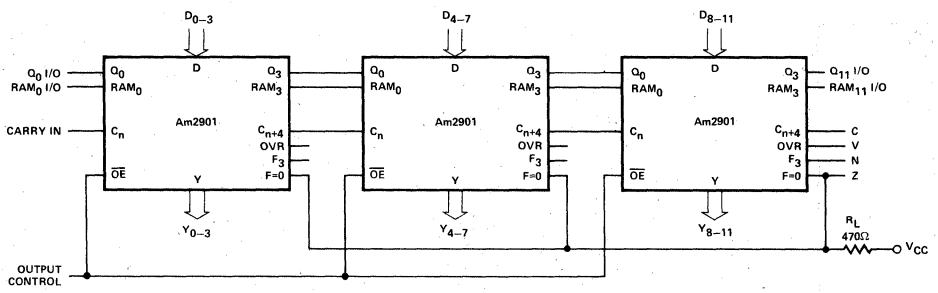


Figure 16. Three Am2901s Used to Construct 12-Bit CPU with Ripple Carry. Corresponding A, B and I Pins on all Devices are Connected together.

Exclusive-OR of the carry-in and carry-out of the sign bit (MSB). It will go HIGH when the result of an arithmetic operation is a number requiring more bits than are available, causing the sign bit to be erroneous. This is the overflow (V) bit of the processor status word. The F_3 pin is the MSB of the ALU output. It is the sign of the result in two's complement notation, and should be used as the Negative (N) bit of the processor status word.

The carry-out from the most significant Am2901 (C_{n+4} pin) is the carry-out from the array, and is used as the carry (C) bit of the processor status word.

Carry interconnections between devices may use either ripple carry or carry lookahead. For ripple carry, the carry-out (C_{n+4}) of each device is connected to the carry-in (C_n) of the next more significant device. Carry lookahead uses the Am2902 lookahead carry generator. The scheme is identical to that used with the 74181/74182. Users unfamiliar with this technique should refer to AMD's application note on Arithmetic Logic Units. Figure 17 and 18 illustrate single and multiple level lookahead.

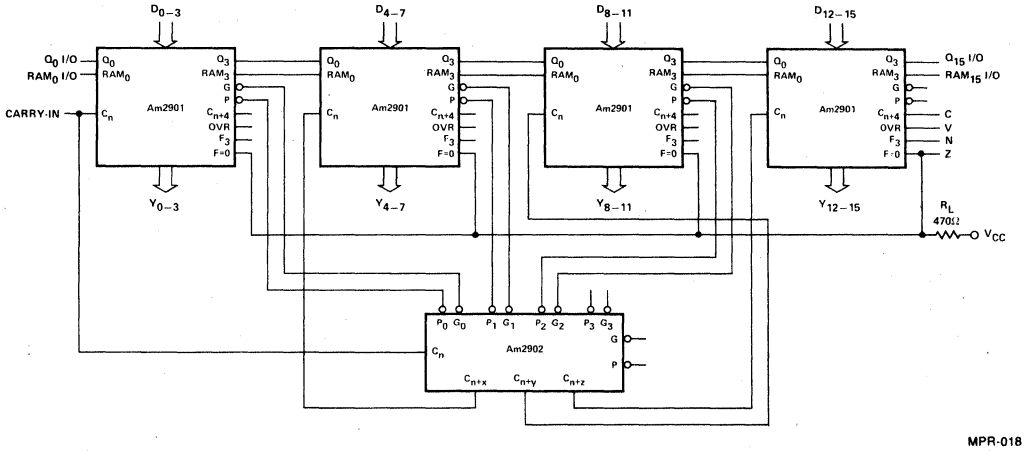


Figure 17. Four Am2901s in a 16-Bit CPU Using the Am2902 for Carry Lookahead.

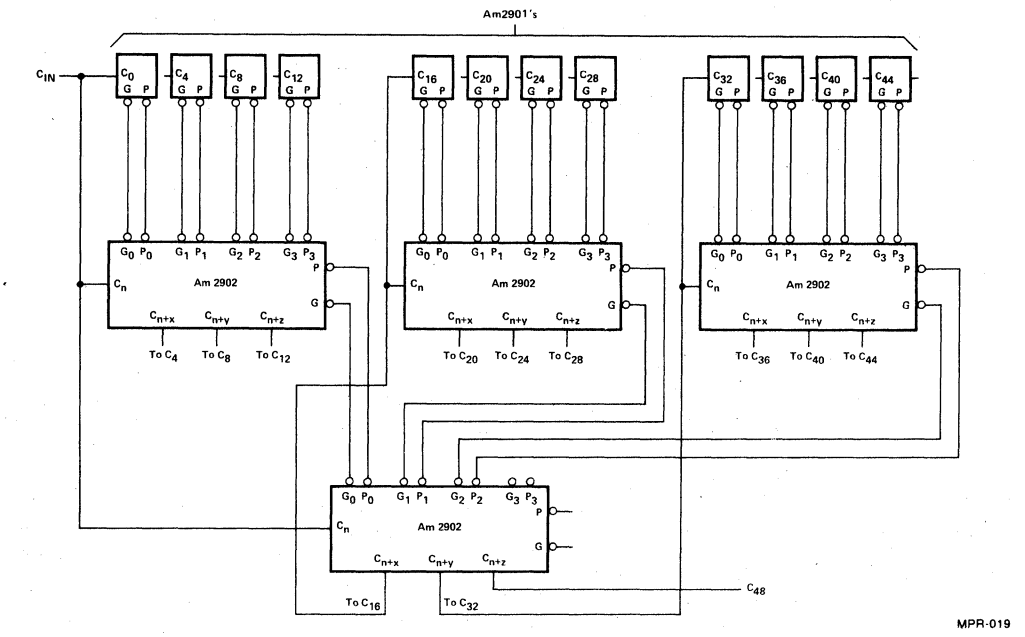


Figure 18. Carry Lookahead Scheme for 48-Bit CPU Using 12 Am2901s. The Carry-Out Flag (C_{48}) should be taken from the Lower Am2902 Rather than the Right-Most Am2901 for Higher Speed.

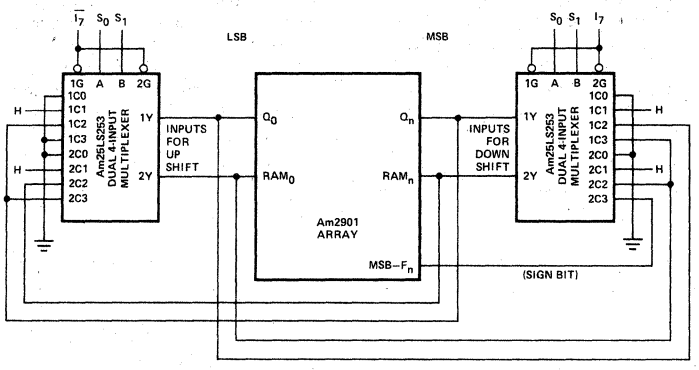


Figure 19. Three-State Multiplexers Used on Shift I/O Lines.

SHIFT I/O LINES AT THE END OF THE ARRAY

The Q-register and RAM left/right shift data transfers occur between devices over bidirectional lines. At the ends of the array, three-state multiplexers are used to select what the new inputs to the registers should be during shifting. The Am2904 includes these multiplexers in a single LSI chip. Figure 19 shows two Am25LS253 dual four-input multiplexers connected to provide four shift modes. Instruction bit I_7 (from the Am2901) is used to select whether the left-shift multiplexer or the right-shift multiplexer is active. The four shift modes in this example are:

Zero A LOW is shifted into the MSB of the RAM on a down shift. If the Q-register is also shifted, then a LOW is deposited in the Q-register MSB. If the RAM or both registers are shifted up, LOWs are placed in the LSBs.

One Same as zero, but a HIGH level is deposited in the LSB or MSB.

Rotate A single precision rotate. The RAM MSB shifts into the LSB on a right shift and the LSB shifts into the MSB on a left shift. The Q-register, if shifted, will rotate in the same manner.

Arithmetic A double-length Arithmetic Shift if Q is also shifted. On an up shift a zero is loaded into the Q-register LSB and the Q-register MSB is loaded into the RAM LSB. On a down shift, the RAM LSB is loaded into the Q-register MSB and the ALU output MSB (F_n, the sign bit) is loaded into the RAM MSB. (This same bit will also be in the next less significant RAM bit.)

Code			Source of New Data				Shift	Type
I_7	S_1	S_0	Q_0	Q_n	RAM_0	RAM_n		
H	L	L	0	Q_{n-1}	0	F_{n-1}	Up	Zero
H	L	H	1	Q_{n-1}	1	F_{n-1}		One
H	H	L	Q_n	Q_{n-1}	F_n	F_{n-1}		Rotate
H	H	H	0	Q_{n-1}	Q_n	F_{n-1}		Arithmetic
L	L	L	Q_1	0	F_1	0	Down	Zero
L	L	H	Q_1	1	F_1	1		One
L	H	L	Q_1	Q_0	F_1	F_0		Rotate
L	H	H	Q_1	F_0	F_1	$RAM_n = RAM_{n-1} = F_n$		Arithmetic

HARDWARE MULTIPLICATION

Figure 20 illustrates the interconnections for a hardware multiplication using the Am2901. The system shown uses two devices for 8 x 8 multiplication, but the expansion to more bits is simple — the significant connections are at the LSB and MSB only.

The basic technique used is the "add and shift" algorithm. One clock cycle is required for each bit of the multiplier. On each cycle, the LSB of the multiplier is examined; if it is a "1", then the multiplicand is added to the partial product to generate a new partial product. The partial product is then shifted one place toward the LSB, and the multiplier is also shifted one place toward the LSB. The old LSB of the multiplier is discarded. The cycle is then repeated on the new LSB of the multiplier available at Q_0.

The multiplier is in the Am2901 Q-register. The multiplicand is in one of the registers in the register stack, R_a. The product will be developed in another of the registers in the stack, R_b.

The A address inputs are used to address the multiplicand in R_a, and the B address inputs are used to address the partial product in R_b. On each cycle, R_a is conditionally added to R_b, depending on the LSB of Q as read from the Q_0 output, and both Q and the ALU output are shifted down one place. The instruction lines to the Am2901 on every cycle will be:

I_{876} = 4 (shift register stack input and Q register left)
I_{543} = 0 (Add)
I_{210} = 1 or 3 (select A, B or 0, B as ALU sources)

Figure 20 shows the connections for multiplication. The circled numbers refer to the paragraphs below.

1. The adjacent pins of the Q-register and RAM shifters are connected together so that the Q-registers of both (or all) Am2901s shift left or right as a unit. Similarly, the entire eight-bit (or more) ALU output can be shifted as a unit prior to storage in the register stack.

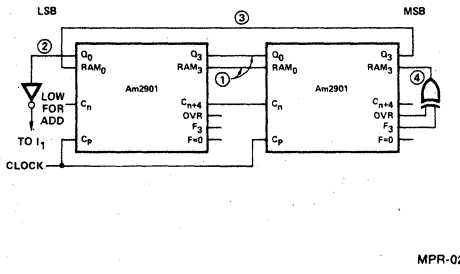


Figure 20. Interconnection for Dedicated Multiplication (8 by 8 bit) (Corresponding A, B and I Connected together).

2. The shift output at the LSB of the Q-register determines whether the ALU source operands will be A and B (add multiplicand to partial product) or 0 and B (add nothing to partial product. Instruction bit I_1 can select between A, B or 0, B as the source operands; it can be driven directly from the complement of the LSB of the multiplier.

3. As the new partial product appears at the input to the register stack, it is shifted left by the RAM shifter. The new LSB of the partial product, which is complete and will not be affected by future operations, is available on the RAM_0 pin. This signal is returned to the MSB of the Q-register. On each cycle then, the just-completed LSB of the product is deposited in the MSB of the Q-register; the Q-register fills with the least significant half of the product.

4. As the ALU output is shifted down on each cycle, the sign bit of the new partial product should be inserted in the RAM MSB shift input. The F_3 flag will be the correct sign of the partial product unless overflow has occurred. If overflow occurs during an addition or subtraction, the OVR flag will go HIGH and F_3 is not the sign of the result. The sign of the result must then be the complement of F_3. The correct sign bit to shift into the MSB of the partial product is therefore $F3 \oplus OVR$; that is, F_3 if overflow has not occurred and $\overline{F_3}$ if overflow has occurred. On the last cycle, when the MSB of the multiplier is examined, a conditional subtraction rather than addition should be performed, because the sign bit of the multiplier carries negative rather than positive arithmetic weight.

$$Y = -Y_i 2^i + Y_{i-1} 2^{i-1} + \ldots + Y_0 2^0$$

This scheme will produce a correct two's complement product for all multiplicands and multipliers in two's complement notation.

Figure 21 is a table showing the input states of the Am2901 for each step of a signed, two's complement multiplication. The Am2904 LSI chip conveniently implements the required shift linkages and the EX-OR function for this algorithm.

Initial Register States

R	
0	Multiplier
1	Multiplicand
2	X
3	X

Am2901 Microcode

Program 2's Comp. Multiply
Date 8/5/75 By J. S.

Final Register States

R	
0	Multiplier
1	Multiplicand
2	LSH Product
3	MSH Product

S, F →	D	Description	Repeat	Pin States (Octal)										Jump	
				A	B	I_{876}	I_{543}	I_{210}	C_n	Q_0	Q_3	RAM_0	RAM_3	To	If
O∨A	Q	Move Multiplier to Q	–	0	X	0	3	4	X	X	X	X	X		
O∧B	B	Clear R_3	–	X	3	2	4	3	X	X	X	X	X		
(O+B)/2 (A+B)/2	B	Cond. Add & Shift	n–1	1	3	4	0	1 or 3 $I_1 = \overline{Q_0}$LO	0	–	RAM_0	–	$F_3 \forall OVR$		
(B–O)/2 (B–A)/2	B	Cond. Subt. & Shift	–	1	3	4	1	1 or 3 $I_1 = \overline{Q_0}$LO	1	–	RAM_0	–	$F_3 \forall OVR$		
O∨Q	B	Move LSH Prod. to R_2	–	X	2	2	3	2	X	X	X	X	X		

X = Don't Care S = Source F = Function D = Destination

Figure 21.

HARDWARE DIVISION

Division, unlike multiplication, is much more difficult to realize. One of these difficulties can be easily understood by visualizing a 2n-bit Dividend (X) and an n-bit Divisor (Y). The Quotient (Q) can range from 1 bit (when $X < Y$) to 2 n bits (when $Y = 1$), discarding the attempt to divide by 0. In most of the divide functions, the Remainder (R) is as important to find as is the Quotient – there is no equivalent to it in multiplication. Division becomes even more complicated when negative numbers are represented in the 2's complement notation. In the "everyday" decimal system, using Sign-and-Magnitude notation, dealing with negative numbers is relatively easy: The sign of the quotient is determined first and then a normal division is performed. Note that in this "normal" division we first "guess" the first digit of the quotient by comparing the most significant part of the dividend to the divisor. Then verify our guess by a multiplication (no "direct" division method is known), and continue to do so for all of the other digits, shifting the divisor to the right one place at a time.

The most straightforward division scheme (for unsigned numbers) is Subsequent Subtraction. The algorithm is as follows: Subtract divisor from dividend and increment a counter (initially reset to zero). Continue to do so as long as the Remainder is positive. When the Remainder becomes negative cancel the last step; i.e., add back divisor and decrement counter. The counter will contain the Quotient and the Remainder will be correct. The main drawback of this scheme is, of course, the great number of arithmetic operations needed. Again, when dealing with signed numbers, the subtraction should be substituted by addition and vice versa.

A more rapid division can be realized by calculating the Quotient digits instead of counting them. In this algorithm, the divisor is first subtracted from the most significant part of the dividend. If the remainder is positive, the quotient digit is "1," otherwise the subtraction is cancelled (by adding the divisor to the remainder) and the quotient digit will be "0." Now shift the remainder one place to the right (much like you do in a "paper and pencil" division) and repeat until all the quotient digits have been calculated. This algorithm is called "Restoring Division." When signed numbers are involved, inversion of the operations and the quotient digits will be necessary and correction should be performed in some cases. Some time is wasted in the Restoring Division because for every "0" digit in the quotient, two arithmetic operations are needed. This can be saved in the "Non-Restoring Division."

The basis of Non-Restoring Division is the same as in Restoring Division. Consider first unsigned (positive) numbers only. At the beginning, the divisor is subtracted from the most significant part of the dividend. If the result (first remainder) is positive (or zero), the first quotient digit is "1." Otherwise, the quotient digit is "0," but do not restore. Shift divisor one place to the right (or remainder to the left) and add if last quotient digit was "0;" otherwise subtract. Determine quotient digit as before and continue until all quotient digits have been computed. The remainder will be correct if it is non-negative, otherwise correction is needed by a restoring operation (on the remainder only). Extreme care should be taken of the number of bits and the value of the divisor. Assuming the divisor has n bits and the dividend as 2n bits, the above process develops $n + 1$ bits of the quotient. This will not be sufficient if the divisor is a small number and more digits are needed in the quotient. This condition can be easily detected as the most significant half of the dividend will be greater than the divisor in this case and division can then be terminated after setting the overflow flag. The flow chart for unsigned nonrestoring division is shown in Figure 25.

The unsigned division scheme can be applied to signed *positive* numbers without any change. When negative numbers are encountered, however, changes in the algorithm are necessary. The straightforward method of signed division seems to be "division in the first quadrant." In that scheme, negative numbers are 2's complemented to obtain positive numbers, remembering the changes done. If overflow occurs when the dividend is complemented (i.e., dividend is -2^{2n-1}, the least negative number), the overflow flag can be set and an exit from the routine taken. This is due to the fact that (-2^{2n-1}) divided by any number of n-bits cannot be represented in n bits. On the other hand, if overflow occurs when the divisor is complemented, a more complex action is needed. In this case, the dividend and the divisor should be shifted right by one place and the shifted out bit should be stored in a flag, say "Z." At the same time, a flag, "W" should also be set to indicate that division by -2^{n-1} is being attempted. These actions need to be taken since the quotient might be representable in n bits. (Here instead of dividend = divisor quotient or remainder, we have dividend/2 = divisor/2* quotient + rem/2. The remainder obtained should be shifted left and the bit Z be added to give the correct remainder.) The division is performed on positive numbers, and finally 2's complementing is done whenever necessary. Figure 22 is the flowchart for this algorithm.

Figure 23 is the Interconnection Diagram for Division Algorithm. It is assumed that the most significant half Dividend is in Register R_X (it will be lost during the division and replaced by the Remainder), the least significant half in the Q Register and that the Divisor is in Register R_Y. The Quotient will be generated in the Q register.

After checking the signs of the Dividend and Divisor, setting the flags and negating (using 23 or 24 octal as I_5 through I_0 ALU control bits) when necessary the overflow condition should be checked. If R_X is greater than , then R_Y, overflow occurs, hence the division can be terminated by setting the overflow flag.

The first step in the Division routine is a subtract, then shift the R_X and Q registers up. I_{876} will be 6 in octal while $I_{210} = 1$ in octal and $I_5 = I_4 =$ LOW. Pulling the CL bit in the microcode to HIGH, both I_3 and C_n will be high and the ALU is performing a 2's complement subtract. The sign of the Remainder will be latched in the Status Register and the complement of it will be stored in the LSB of the Q register during the shift up operation, which also discards the sign bit of the Remainder.

Now repeating the same operation for all of the other bits of the Remainder with the CL bit in the microcode LOW will leave the control of I_3 to the (complemented) previous sign bit. If it was "0" ($R < 0$), I_3 and C_n will be HIGH and the ALU will subtract; if it was 1 ($R > 0$), I_3 and C_n will be LOW and the ALU will ADD, as required. In each up shift, the complement of the present sign bit will be placed at the right of the Quotient, again, as required.

At the end of the division, the sign bit of the Remainder should be examined and if it is HIGH, the Divisor should be added to it. This can be easily implemented (not depicted on Figure 23) by performing an unconditional ADD (with C_n LOW), letting I_2 LOW, I_0 HIGH and controlling I_1 by the complement of the sign of the Remainder, thus adding to the RX either RY (if $R_S = 1$) or zero (if $R_S = 0$). If the dividend and divisor were shifted right because the divisor was equal to -2^{n-1}, the true remainder is obtained by shifting the remainder left and adding the flag "Z." The above method generates $n + 1$ bits of the quotient ($q_n \ldots q_0$) of which $q_n = 0$, since most significant half of dividend is less than the divisor. The overflow flag should be set if $q_{n-1} = 1$ since $q_{n-1} \ldots q_0$ is an unsigned positive number.

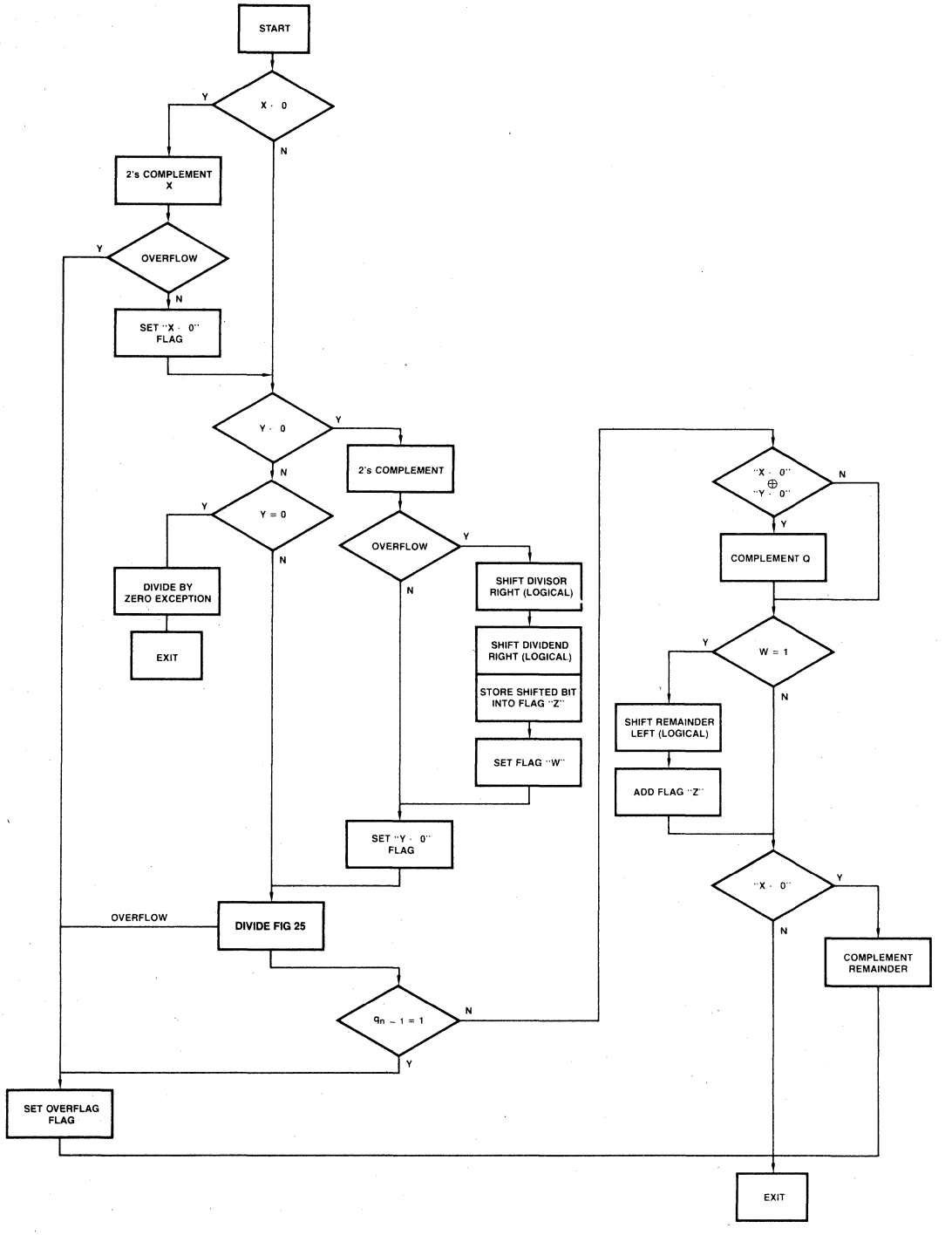


Figure 22. Flowchart for Division with Signed Numbers (Quotient = q_n, $q_n - 1 \cdots q_0$ where $q_n = 0$)

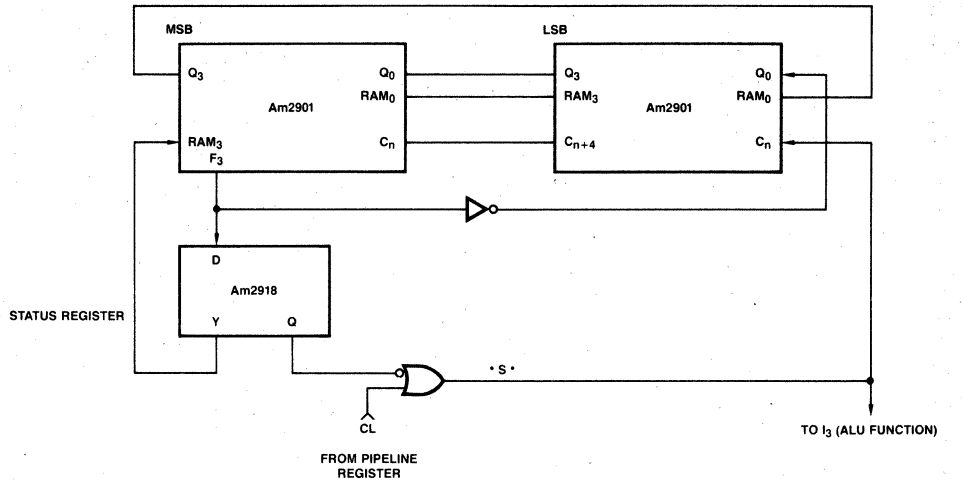


Figure 23. Interconnections for Dedicated Division

Initial Register Status

R

0	MSH Dividend
1	Divisor
Q	LSH Dividend

Am2901 Microcode

Program: 2's Complement Division

Final Register Status

R

0	Remainder
1	Divisor
Q	Quotient

S, F	D	Description	CL	Repeat	Pin Status (Octal)										Jump	
					A	B	I_{876}	I_{543}	I_{210}	C_n	Q_0	Q_3	RAM_0	RAM_3	to	if
(B−A) *2	B	First Subtract & Shift	1	–	1	0	6	1	1	1	F_3	X	0	X		
(B±A) *2	B	Loop Subtract/Add & Shift	0	N	1	0	6	1/0	1	1/0	F_3	X	0	X		
B+0	B	Correct Remainder	X	–	1	0	3	0	1/3	0	X	X	X	X		

k = Number of leading zeros of the Divisor

N = Number of bits in the Divisor

Figure 24. Am2901 Microcode for Dedicated Division

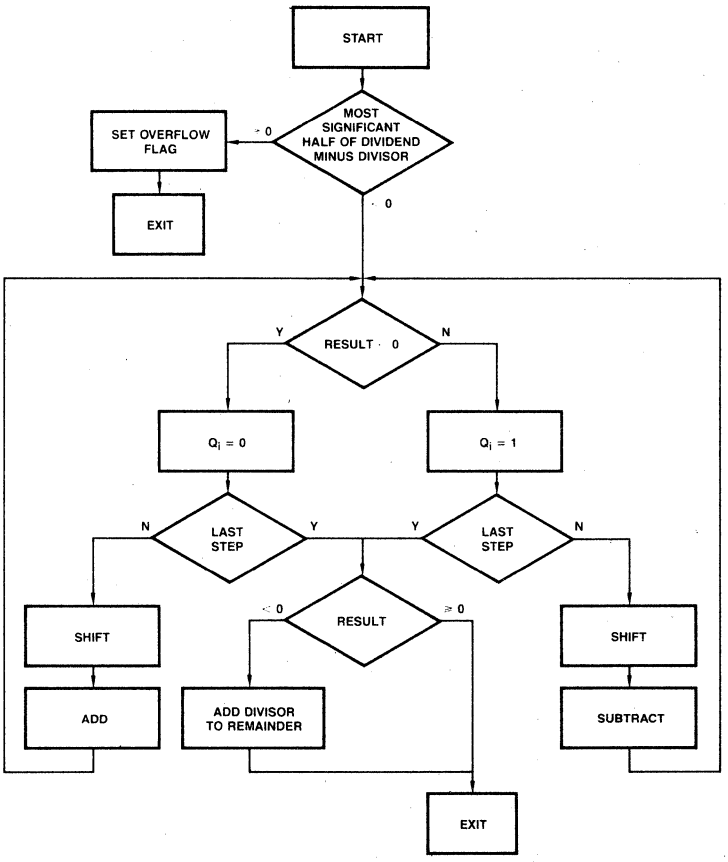


Figure 25. Flowchart for Nonrestoring Division (Unsigned Numbers)

Finally, the Quotient and/or Remainder should be 2's complemented again according to the flags. Complementation of the remainder cannot generate an overflow – because the maximum remainder after divide (Figure 25) is 0011 . . . 1 and the remainder correction when W = 1 can make the remainder at most 0111 . . . 1.

EXAMPLES OF SOME OTHER OPERATIONS

1. Byte Swapping

Occasionally the two halves of a 16-bit word must be swapped. D_{0-7} is interchanged with D_{8-15}. The quickest way to perform this operation is to rotate the word in RAM, shifting two bits at a time. Only four shift cycles are required. The same register is selected on both the A and B ports; the two are added together with carry-in connected to carry-out, producing a right shift of one place; then the ALU is shifted right one more place prior to storage.

Byte Swap of R_0

A = B = 0 I = 701 $RAM_0 = RAM_{15}$ $C_{IN} = C_{OUT}$

Repeat 4 times.

2. Instruction Fetch Cycle

Execution of a macroinstruction generally begins with an instruction fetch cycle. The current contents of the PC (in one of the registers) is the address of the macroinstruction to be fetched, and must be read out to the memory address register. Then the PC is incremented to point to the next macroinstruction. The macroinstruction obtained from memory is then loaded into the microprogram sequencer to cause a jump to the microcode for executing the instruction.

The PC can be read out and incremented in one cycle by using the Am2901 destination code 2, and addressing the PC with both the A and B addresses. The current value of PC will appear on the Y outputs, and PC+1 will be returned to the register. If the PC is in register 15, then:

A = B = 15, I = 203, Carry-in = 1

The PC will be on the Y outputs via the RAM A-port. On the clock LOW-to-HIGH transition, the program counter is incremented and the value on the Y outputs is loaded into the memory address register. During the following cycle, the memory is read and, on the next clock LOW-to-HIGH transition the instruction from the memory is dropped into the instruction register. The fetch operation requires only two microcycles.

Am2902A

High-Speed Look-Ahead Carry Generator

DISTINCTIVE CHARACTERISTICS

- Provides look-ahead carries accross a group of four Am2901 or Am2903 microprocessor ALU's
- Capability of multi-level look-ahead for high-speed arithmetic operation over large word lengths
- Typical carry propagation delay of 4.5ns

RELATED PRODUCTS

Part No.	Description
Am2901	4-Bit Microprocessor Slice
Am2903	4-Bit Microprocessor Slice
Am29203	Improved 2903
Am29501	Multiport Pipelined Processor

FUNCTIONAL DESCRIPTION

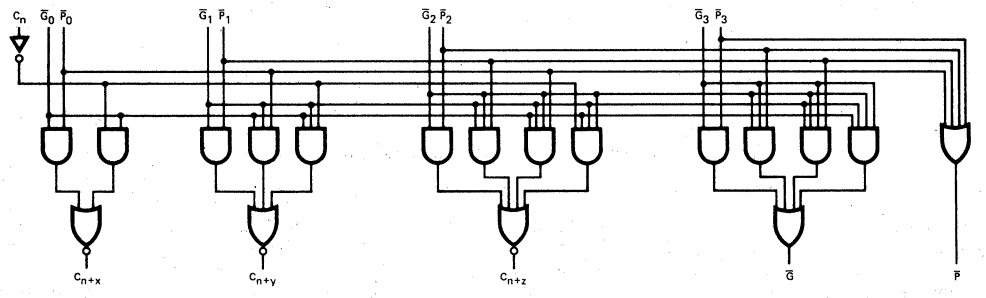
The Am2902A is a high-speed, look-ahead carry generator which accepts up to four pairs of carry propagate and carry generate signals and a carry input and provides anticipated carries across four groups of binary ALU's. The device also has carry propagate and carry generate outputs which may be used for further levels of look-ahead.

The Am2902A is generally used with the Am2901 bipolar microprocessor unit to provide look-ahead over word lengths of more than four bits. The look-ahead carry generator can be used with binary ALU's in an active LOW or active HIGH input operand mode by reinterpreting the carry functions. The connections to and from the ALU to the look-ahead carry generator are identical in both cases.

The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$G = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$$
$$P = P_3P_2P_1P_0$$

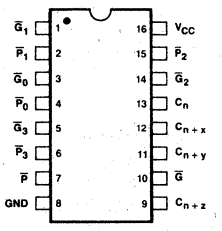
LOGIC DIAGRAM



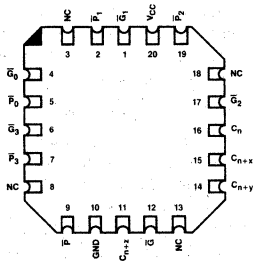
MPR-026

CONNECTION DIAGRAMS – Top Views

P-16, D-16



Leadless Chip Carrier L-20-1

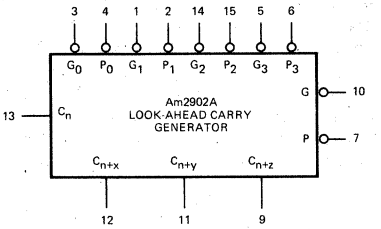


F-16 pin configuration identical to D-16, P-16.

Note: Pin 1 is marked for orientation.

MPR-027

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

MPR-025

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am2902AXC T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am2902AXM T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL) MIN. = 4.50V MAX. = 5.50V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1mA, V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V	C_n			−2	mA
			$\overline{P}_3$			−4	
			$\overline{P}_2$			−6	
			$\overline{P}_0$, $\overline{P}_1$, $\overline{G}_3$			−8	
			$\overline{G}_0$, $\overline{G}_2$			−14	
			$\overline{G}_1$			−16	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	C_n			50	μA
			$\overline{P}_3$			100	
			$\overline{P}_2$			150	
			$\overline{P}_0$, $\overline{P}_1$, $\overline{G}_3$			200	
			$\overline{G}_0$, $\overline{G}_2$			350	
			$\overline{G}_1$			400	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit (Note 3)	V_{CC} = MAX., V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All Outputs LOW	MIL		69	99	mA
			COM'L		69	109	
		V_{CC} = MAX., All Ouputs HIGH	MIL		35		mA
			COM'L		35		

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	C_n to C_{n+x}, C_{n+y}, or C_{n+z}		6.5	10	ns	C_L = 15pF, R_L = 280Ω
t_{PHL}			7	10.5		
t_{PLH}	$\overline{P}_i$ or $\overline{G}_i$ to C_{n+x}, C_{n+y}, or C_{n+z}		4.5	7	ns	
t_{PHL}			4.5	7		
t_{PLH}	$\overline{P}_i$ or $\overline{G}_i$ to $\overline{G}$		5	7.5	ns	
t_{PHL}			7	10.5		
t_{PLH}	$\overline{P}_i$ to $\overline{P}$		4.5	6.5	ns	
t_{PHL}			6.5	10		

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Max.	T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Max.	Units	Test Conditions
t_{PLH}	C_n to C_{n+x}, C_{n+y}, or C_{n+z}		13		15	ns	C_L = 50pF, R_L = 280Ω
t_{PHL}			14		16.5	ns	
t_{PLH}	$\overline{P}_i$ or $\overline{G}_i$ to C_{n+x}, C_{n+y}, or C_{n+z}		8		9.5	ns	
t_{PHL}			9		11.5	ns	
t_{PLH}	$\overline{P}_i$ or $\overline{G}_i$ to $\overline{G}$		12		16.5	ns	
t_{PHL}			12		13.5	ns	
t_{PLH}	$\overline{P}_i$ to $\overline{P}$		9.5		11.5	ns	
t_{PHL}			11		12	ns	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

C_n Carry-in. The carry-in input to the look-ahead generator. Also the carry-in input to the nth Am2901A microprocessor ALU input.

C_{n+j} Carry-out. (j = x, y, z). The carry-out output to be used at the carry-in inputs of the n+1, n+2 and n+3 microprocessor ALU slices.

G_i, P_i Generate and propagate inputs respectively (i = 0, 1, 2, 3). The carry generate and carry propagate inputs from the n, n+1, n+2 and n+3 microprocessor ALU slices.

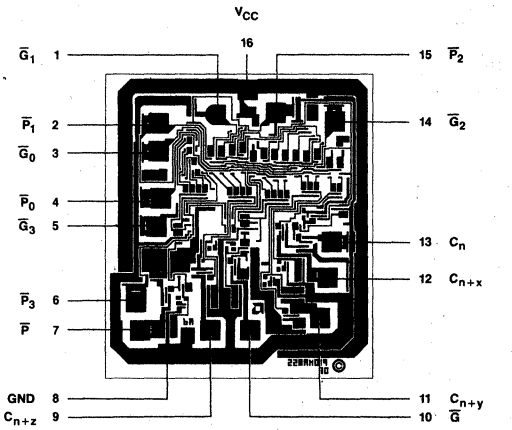
G, P Generate and propagate outputs respectively. The carry generate and carry propagate outputs that can be used with the next higher level of carry look-ahead if used.

TRUTH TABLE

Inputs									Outputs				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	L	X					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
X			X	X	X	X	H	H				H	
X			X	X	H	H	H	X				H	
X			H	H	H	X	H	X				H	
H			H	X	H	X	H	X				H	
X			X	X	X	X	L	X				L	
X			X	X	L	X	X	L				L	
X			L	X	L	X	X	L				L	
L			X	L	X	L	X	L				L	
	X			X		X		X					H
	X			H		X		X					H
	X			X		H		X					H
	H			X		X		H					H
	X			X		X		L					L
	L			L		L		L					L

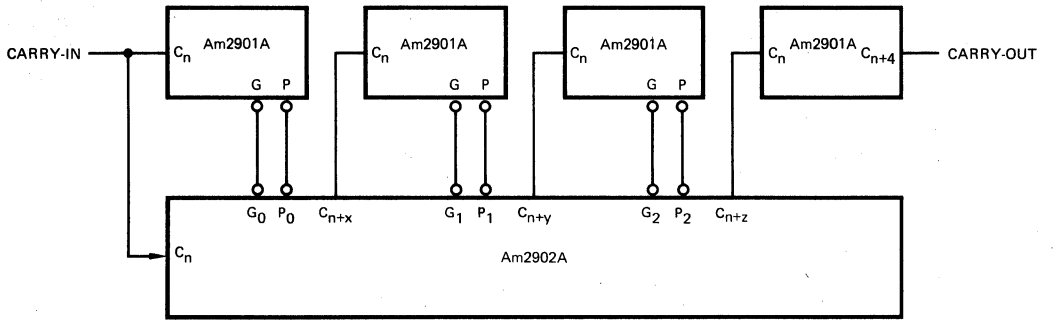
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

METALLIZATION AND PAD LAYOUT



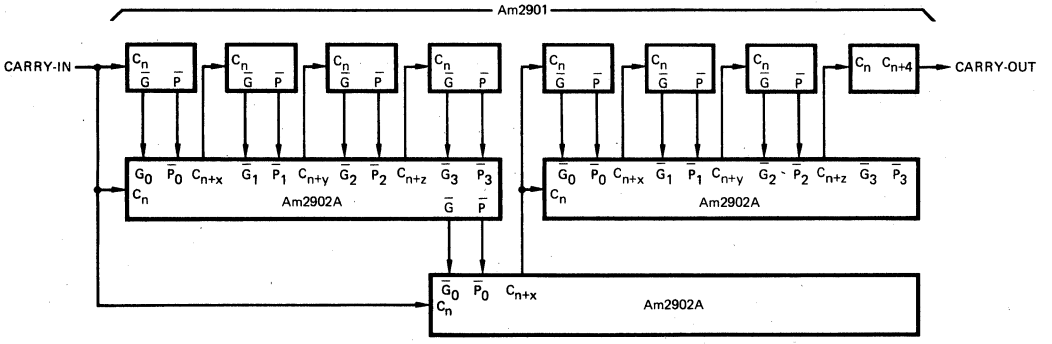
DIE SIZE 0.062" X 0.067"

APPLICATIONS



16-BIT CARRY LOOK-AHEAD CONNECTION.

MPR-028



32-BIT ALU, THREE LEVEL CARRY LOOK-AHEAD.

MPR-029

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2902APC	P-16	C	C-1
AM2902ADC	D-16	C	C-1
AM2902ADC-B	D-16	C	B-1
AM2902ADM	D-16	M	C-3
AM2902ADM-B	D-16	M	B-3
AM2902AFM	F-16	M	C-3
AM2902AFM-B	F-16	M	B-3
AM2902ALC	L-20-1	C	C-1
AM2902ALC-B	L-20-1	C	B-1
AM2902ALM	L-20-1	M	C-3
AM2902ALM-B	L-20-1	M	B-3
AM2902AXC	Dice	C	Visual inspection to MIL-STD-883. Method 2010B.
AM2902AXM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Flat-Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am2903/2903A

Four-Bit Bipolar Microprocessor Slice

DISTINCTIVE CHARACTERISTICS

- **Expandable Register File –**
  Like the Am2901, the Am2903 contains 16 internal working registers arranged in a two-address architecture. But the Am2903 includes the necessary "hooks" to expand the register file externally to any number of registers.
- **Built-in Multiplication Logic –**
  Performing multiplication with the Am2901 requires a few external gates – these gates are contained on-chip in the Am2903. Three special instructions are used for unsigned multiplication, two's complement multiplication and the last cycle of a two's complement multiplication.
- **Built-in Division Logic –**
  The Am2903 contains all logic and interconnects for execution of a non-restoring, multiple-length division with correction of the quotient.
- **Built-in Normalization Logic –**
  The Am2903 can simultaneously shift the Q Register and count in a working register. Thus, the mantissa and exponent of a floating-point number can be developed using a single microcycle per shift. Status flags indicate when the operation is complete.
- **Built-in Parity Generation Circuitry –**
  The Am2903 can supply parity across the entire ALU output for use in error detection.
- **Built-in Sign Extension Circuitry –**
  To facilitate operation on different length two's complement numbers, the Am2903 provides the capability to extend the sign at any slice boundary.
- **Fast –**
  The Am2903A is up to 30% faster than the Am2903 and meets or exceeds all of the specifications for the Am2903.
- **IMOX –**
  The Am2903A is processed with AMD's proprietary IMOX™ technology.

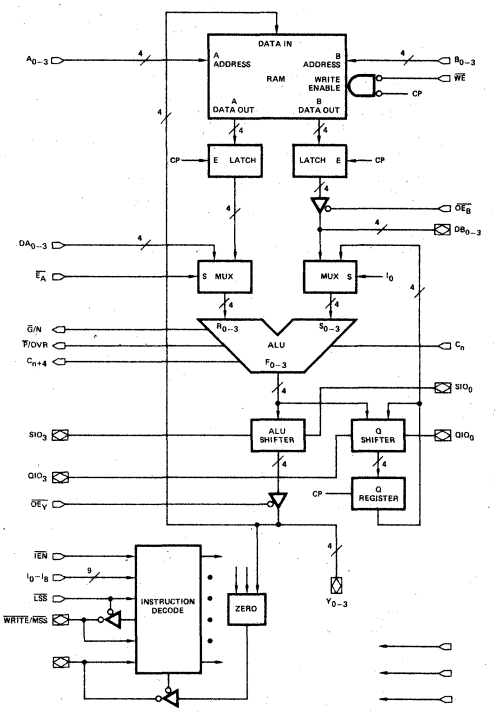
RELATED PRODUCTS

Part No.	Description	Page
Am2902A	Carry Look-Ahead Generator	
Am2904	Status and Shift Control Unit	
Am2910A	Microprogram Controller	
Am2914	Vectored Priority Interrupt Controller	
Am2918	Pipeline Register	
Am2920	Octal Register	
Am2922	Condition Code MUX	
Am2925	System Clock Generator	
Am2940	DMA Address Generator	
Am2952	Bidirectional I/O Port	
Am29705A	Two-Port RAM	
Am27S35	Registered PROM	

GENERAL DESCRIPTION

The Am2903 is a four-bit expandable bipolar microprocessor slice. The Am2903 performs all functions performed by the industry standard Am2901 and, in addition, provides a number of significant enhancements that are especially useful in arithmetic-oriented processors. Infinitely expandable memory and three-port, three-address architecture are provided by the Am2903. In addition to its complete arithmetic and logic instruction set, the Am2903 provides a special set of instructions which facilitate the implementation of multiplication, division, normalization, and other previously time-consuming operations. The Am2903A is identical to the Am2903 but up to 30% faster.

BLOCK DIAGRAM



Notes: 1. DA_{0-3} is input only on Am2903, but is I/O port on Am29203.
2. On Am2903, zero logic is connected to Y, after the $\overline{OE}_Y$ buffer.
3. On Am2903 $\overline{IEN}$ controls $\overline{WRITE}$. On Am29203 $\overline{WRITE}$ is not affected by $\overline{IEN}$.

MPR-030

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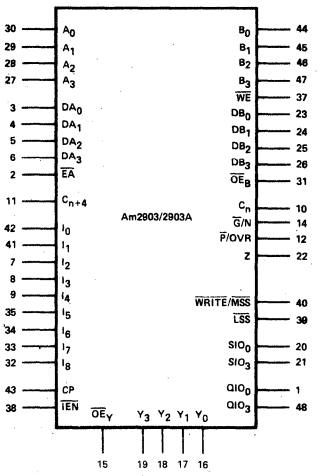
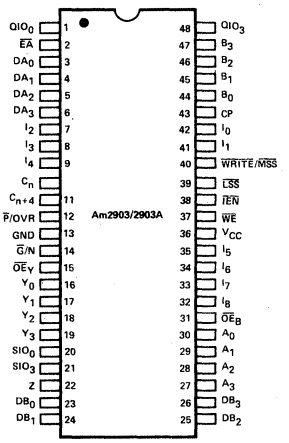
LOGIC SYMBOL

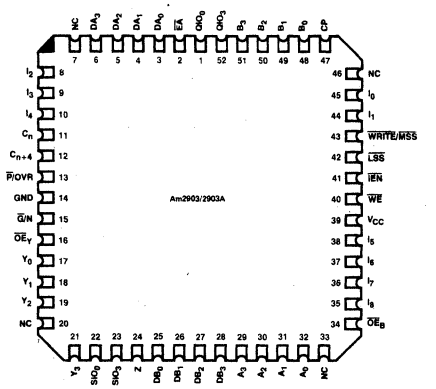


CONNECTION DIAGRAMS
Top Views

DIP
D-48



Leadless Chip Carrier
L-52-1



Note: Pin 1 is marked for orientation.

5

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2903 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2903DC	D-48	C	C-1
AM2903DC-B	D-48	C	B-2 (Note 4)
AM2903DM	D-48	M	C-3
AM2903DM-B	D-48	M	B-3
AM2903FM	F-48	M	C-3
AM2903FM-B	F-48	M	B-3
AM2903LC	L-52	C	C-1
AM2903LM	L-52	M	C-3
AM2903LM-B	L-52	M	B-3
AM2903XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2903XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak, L = Leadless Chip-Pak. Number following letter is number of leads. See Appendix B for detailed outline.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

PIN DEFINITIONS

A_{0-3} Four RAM address inputs which contain the address of the RAM word appearing at the RAM A output port.

B_{0-3} Four RAM address inputs which contain the address of the RAM word appearing at the RAM B output port and into which new data is written when the $\overline{WE}$ input and the CP input are LOW.

$\overline{WE}$ The RAM write enable input. If $\overline{WE}$ is LOW, data at the Y I/O port is written into the RAM when the CP input is LOW. When $\overline{WE}$ is HIGH, writing data into the RAM is inhibited.

DA_{0-3} A four-bit external data input which can be selected as one of the Am2903 ALU operand sources; DA_0 is the least significant bit.

$\overline{EA}$ A control input which, when HIGH selects DA_{0-3} as the ALU R operand, and, when LOW, selects RAM output A as the ALU R operand and the DA_{0-3} output data.

DB_{0-3} A four-bit external data input/output. Under control of the $\overline{OE_B}$ input, RAM output port B can be directly read on these lines, or input data on these lines can be selected as the ALU S operand.

$\overline{OE_B}$ A control input which, when LOW, enables RAM output B onto the DB_{0-3} lines and, when HIGH, disables the RAM output B tri-state buffers.

C_n The carry-in input to the Am2903 ALU.

I_{0-8} The nine instruction inputs used to select the Am2903 operation to be performed.

$\overline{IEN}$ The instruction enable input which, when LOW, allows the Q Register and the Sign Compare flip-flop to be written. When $\overline{IEN}$ is HIGH, the Q Register and Sign Compare flip-flop are in the hold mode. On the Am2903, $\overline{IEN}$ also controls $\overline{WRITE}$.

C_{n+4} This output generally indicates the carry-out of the Am2903 ALU. Refer to Table 5 for an exact definition of this pin.

$\overline{G}$/N A multi-purpose pin which indicates the carry generate, $\overline{G}$, function at the least significant and intermediate slices, and generally indicates the sign, N, of the ALU result at the most significant slice. Refer to Table 5 for an exact definition of this pin.

$\overline{P}$/OVR A multi-purpose pin which indicates the carry propagate, $\overline{P}$, function at the least significant and intermediate slices, and indicates the conventional two's complement overflow, OVR, signal at the most significant slice. Refer to Table 5 for an exact definition of this pin.

Z An open-collector input/output pin which, when HIGH, generally indicates the outputs are all LOW. For some Special Functions, Z is used as an input pin. Refer to Table 5 for an exact definition of this pin.

SIO_0, SIO_3 Bidirectional serial shift inputs/outputs for the ALU shifter. During a shift-up operation, SIO_0 is an input and SIO_3 an output. During a shift-down operation, SIO_3 is an input and SIO_0 is an output. Refer to Tables 3 and 4 for an exact definition of these pins.

QIO_0, QIO_3 Bidirectional serial shift inputs/outputs for the Q shifter which operate like SIO_0 and SIO_3. Refer to Tables 3 and 4 for an exact definition of these pins.

$\overline{LSS}$ An input pin which, when tied LOW, programs the chip to act as the least significant slice (LSS) of an Am2903 array and enables the $\overline{WRITE}$ output onto the $\overline{WRITE}/\overline{MSS}$ pin. When $\overline{LSS}$ is tied HIGH, the chip is programmed to operate as either an intermediate or most significant slice and the $\overline{WRITE}$ output buffer is disabled.

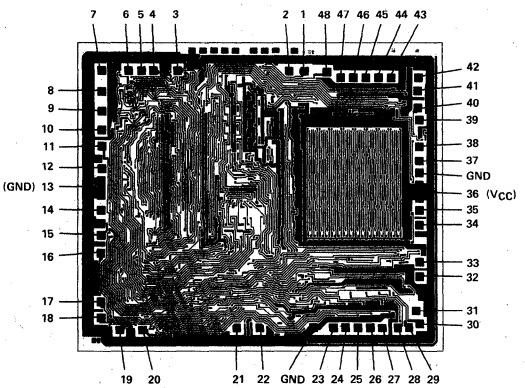
$\overline{WRITE}$/$\overline{MSS}$ When $\overline{LSS}$ is tied LOW, the $\overline{WRITE}$ output signal appears at this pin; the $\overline{WRITE}$ signal is LOW when an instruction which writes data into the RAM is being executed. When $\overline{LSS}$ is tied HIGH, $\overline{WRITE}/\overline{MSS}$ is an input pin; tying it HIGH programs the chip to operate as an intermediate slice (IS) and tying it LOW programs the chip to operate as the most significant slice (MSS).

Y_{0-3} Four data inputs/outputs of the Am2903. Under control of the $\overline{OE_Y}$ input, the ALU shifter output data can be enabled onto these lines, or these lines can be used as data inputs when external data is written directly into the RAM.

$\overline{OE_Y}$ A control input which, when LOW, enables the ALU shifter output data onto the Y_{0-3} lines and, when HIGH, disables the Y_{0-3} three-state output buffers.

CP The clock input to the Am2903. The Q Register and Sign Compare flip-flop are clocked on the LOW-to-HIGH transition of the CP signal. When enabled by $\overline{WE}$, data is written in the RAM when CP is LOW.

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.163" X 0.197"

Note: Pin numbers correspond to DIP package.

Am 2903

ARCHITECTURE OF THE Am2903

The Am2903 is a high-performance, cascadable, four-bit bipolar microprocessor slice designed for use in CPU's, peripheral controllers, microprogrammable machines, and numerous other applications.The microinstruction flexibility of the Am2903 allows the efficient emulation of almost any digital computing machine. The nine-bit microinstruction selects the ALU sources, function and destination. The Am2903 is cascadable with full lookahead or ripple carry, has three-state outputs, and provides various ALU status flag outputs. Advanced Low-Power Schottky processing is used to fabricate this 48-pin LSI circuit.

All data paths within the device are four bits wide. As shown in the block diagram, the device consists of a 16-word by 4-bit, two-port RAM with latches on both output ports, a high-performance ALU and shifter, a multi-purpose Q Register with shifter input, and a nine-bit instruction decoder.

Two-Port RAM

Any two RAM words addressed at the A and B address ports can be read simultaneously at the respective RAM A and B output ports. Identical data appear at the two output ports when the same address is applied to both address ports. The latches at the RAM output ports are transparent when the clock input, CP, is HIGH and they hold the RAM output data when CP is LOW. Under control of the $\overline{OE_B}$ three-state output enable, RAM data can be read directly at the Am2903 DB I/O port.

External data at the Am2903 Y I/O port can be written directly into the RAM, or ALU shifter output data can be enabled onto the Y I/O port and entered into the RAM. Data is written into the RAM at the B address when the write enable input, $\overline{WE}$, is LOW and the clock input, CP, is LOW.

Arithmetic Logic Unit

The Am2903 high-performance ALU can perform seven arithmetic and nine logic operations on two 4-bit operands. Multiplexers at the ALU inputs provide the capability to select various pairs of ALU source operands. The $\overline{E_A}$ input selects either the DA external data input or RAM output port A for use as one ALU operand and the $\overline{OE_B}$ and I_0 inputs select RAM output port B, DB external data input, or the Q Register content for use as the second ALU operand. Also, during some ALU operations, zeroes are forced at the ALU operand inputs. Thus, the Am2903 ALU can operate on data from two external sources, from an internal and external source, or from two internal sources. Table I shows all possible pairs of ALU source operands as a function of the $\overline{E_A}$, $\overline{OE_B}$, and I_0 inputs.

When instruction bits I_4, I_3, I_2, I_1, and I_0 are LOW, the Am2903 executes special functions. Table 4 defines these special functions and the operation which the ALU performs for each. When the Am2903 executes instructions other than the nine special functions, the ALU operation is determined by instruction bits I_4, I_3, I_2, and I_1. Table 2 defines the ALU operation as a function of these four instruction bits.

TABLE 1. ALU OPERAND SOURCES

$\overline{E_A}$	I_0	$\overline{OE_B}$	ALU Operand R	ALU Operand S
L	L	L	RAM Output A	RAM Output B
L	L	H	RAM Output A	DB_{0-3}
L	H	X	RAM Output A	Q Register
H	L	L	DA_{0-3}	RAM Output B
H	L	H	DA_{0-3}	DB_{0-3}
H	H	X	DA_{0-3}	Q Register

L = LOW H = HIGH X = Don't Care

TABLE 2. Am2903 ALU FUNCTIONS

I_4	I_3	I_2	I_1	Hex Code	ALU Functions	
L	L	L	L	0	I_0 = L	Special Functions
					I_0 = H	F_i = HIGH
L	L	L	H	1	F = S Minus R Minus 1 Plus C_n	
L	L	H	L	2	F = R Minus S Minus 1 Plus C_n	
L	L	H	H	3	F = R Plus S Plus C_n	
L	H	L	L	4	F = S Plus C_n	
L	H	L	H	5	F = $\bar{S}$ Plus C_n	
L	H	H	L	6	F = R Plus C_n	
L	H	H	H	7	F = $\bar{R}$ Plus C_n	
H	L	L	L	8	F_i = LOW	
H	L	L	H	9	F_i = $\bar{R}_i$ AND S_i	
H	L	H	L	A	F_i = R_i EXCLUSIVE NOR S_i	
H	L	H	H	B	F_i = R_i EXCLUSIVE OR S_i	
H	H	L	L	C	F_i = R_i AND S_i	
H	H	L	H	D	F_i = R_i NOR S_i	
H	H	H	L	E	F_i = R_i NAND S_i	
H	H	H	H	F	F_i = R_i OR S_i	

L = LOW H = HIGH i = 0 to 3

Am2903s may be cascaded in either a ripple carry or lookahead carry fashion. When a number of Am2903s are cascaded, each slice must be programmed to be a most significant slice (MSS), intermediate slice (IS), or least significant slice (LSS) of the array. The carry generate, G, and carry propagate, P, signals required for a lookahead carry scheme are generated by the Am2903 and are available as outputs of the least significant and intermediate slices.

The Am2903 also generates a carry-out signal, C_{n+4}, which is generally available as an output of each slice. Both the carry-in, C_n, and carry-out, C_{n+4}, signals are active HIGH. The ALU generates two other status outputs. These are negative, N, and overflow, OVR. The N output is generally the most significant (sign) bit of the ALU output and can be used to determine positive or negative results. The OVR output indicates that the arithmetic operation being performed exceeds the available two's complement number range. The N and OVR signals are available as outputs of the most significant slice. Thus, the multipurpose $\overline{G}$/N and $\overline{P}$/OVR outputs indicate $\overline{G}$ and $\overline{P}$ at the least significant and intermediate slices, and sign and overflow at the most significant slice. To some extent, the meaning of the C_{n+4}, $\overline{P}$/OVR, and $\overline{G}$/N signals vary with the ALU function being performed. Refer to Table 5 for an exact definition of these four signals as a function of the Am2903 instruction.

ALU Shifter

Under instruction control, the ALU shifter passes the ALU output (F) non-shifted, shifts it up one bit position (2F), or shifts it down one bit position (F/2). Both arithmetic and logical shift operations are possible. An arithmetic shift operation shifts data around the most significant (sign) bit position of the most significant slice,

and a logical shift operation shifts data through this bit position (see Figure A). SIO_0 and SIO_3 are bidirectional serial shift inputs/outputs. During a shift-up operation, SIO_0 is generally a serial shift input and SIO_3 a serial shift output. During a shift-down operation, SIO_3 is generally a serial shift input and SIO_0 a serial shift output.

To some extent, the meaning of the SIO_0 and SIO_3 signals is instruction dependent. Refer to Tables 3 and 4 for an exact definition of these pins.

The ALU shifter also provides the capability to sign extend at slice boundaries. Under instruction control, the SIO_0 (sign) input can be extended through Y_0, Y_1, Y_2, Y_3 and propagated to the SIO_3 output.

A cascadable, five-bit parity generator/checker is designed into the Am2903 ALU shifter and provides ALU error detection capability. Parity for the F_0, F_1, F_2, F_3 ALU outputs and SIO_3 input is generated and, under instruction control, is made available at the SIO_0 output. Refer to the Am2903 applications section for a more detailed description of the Am2903 sign extension and parity generation/checking capability.

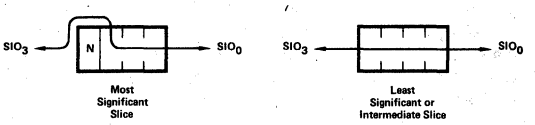
The instruction inputs determine the ALU shifter operation. Table 4 defines the special functions and the operation the ALU shifter performs for each. When the Am2903 executes instructions other than the special functions, the ALU shifter operation is determined by instruction bits I_8, I_7, I_6, I_5. Table 3 defines the ALU shifter operation as a function of these four bits.

Q Register

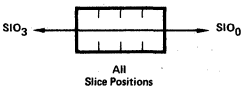
The Q Register is an auxiliary four-bit register which is clocked on the LOW-to-HIGH transition of the CP input. It is intended primarily for use in multiplication and division operations; however, it can also be used as an accumulator or holding register for some applications. The ALU output, F, can be loaded into the Q Register, and/or the Q Register can be selected as the source for the ALU S operand. The shifter at the input to the Q Register provides the capability to shift the Q Register contents up one bit position (2Q) or down one bit position (Q/2). Only logical shifts are performed. QIO_0 and QIO_3 are bidirectional shift serial inputs/outputs. During a Q Register shift-up operation, QIO_0 is a serial shift input and QIO_3 is a serial shift output. During a shift-down operation, QIO_3 is a serial shift input and QIO_0 is a serial shift output.

Figure A.

Am2903 Arithmetic Shift Path



Am2903 Logical Shift Path



Double-length arithmetic and logical shifting capability is provided by the Am2903. The double-length shift is performed by connecting QIO_3 of the most significant slice to SIO_0 of the least significant slice, and executing an instruction which shifts both the ALU output and the Q Register.

The Q Register and shifter are controlled by the instruction inputs. Table 4 defines the Am2903 special functions and the operations which the Q Register and shifter perform for each. When the Am2903 executes instructions other than the special functions, the Q Register and shifter operation is controlled by instruction bits I_8, I_7, I_6, I_5. Table 3 defines the Q Register and shifter operation as a function of these four bits.

Output Buffers

The DB and Y ports are bidirectional I/O ports driven by three-state output buffers with external output enable controls. The Y output buffers are enabled when the $\overline{OE_Y}$ input is LOW and are in the high impedance state when $\overline{OE_Y}$ is HIGH. The DB output buffers are enabled when the $\overline{OE_B}$ input is LOW.

TABLE 3. ALU DESTINATION CONTROL FOR I_0 OR I_1 OR I_2 OR I_3 = HIGH, $\overline{IEN}$ = LOW.

I_8	I_7	I_6	I_5	Hex Code	ALU Shifter Function	SIO_3		Y_3		Y_2		Y_1	Y_0	SIO_0	$\overline{Write}$	Q Reg & Shifter Function	QIO_3	QIO_0
						Most Sig. Slice	Other Slices	Most Sig. Slice	Other Slices	Most Sig. Slice	Other Slices							
L	L	L	L	0	Arith. F/2→Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Hold	Hi-Z	Hi-Z
L	L	L	H	1	Log. F/2→Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Hold	Hi-Z	Hi-Z
L	L	H	L	2	Arith. F/2→Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Log. Q/2→Q	Input	Q_0
L	L	H	H	3	Log. F/2→Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Log. Q/2→Q	Input	Q_0
L	H	L	L	4	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	Hold	Hi-Z	Hi-Z
L	H	L	H	5	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	Log. Q/2→Q	Input	Q_0
L	H	H	L	6	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	F→Q	Hi-Z	Hi-Z
L	H	H	H	7	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	F→Q	Hi-Z	Hi-Z
H	L	L	L	8	Arith. 2F→Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	L	L	H	9	Log. 2F→Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	L	H	L	A	Arith. 2F→Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q→Q	Q_3	Input
H	L	H	H	B	Log. 2F→Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q→Q	Q_3	Input
H	H	L	L	C	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	H	Hold	Hi-Z	Hi-Z
H	H	L	H	D	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	H	Log. 2Q→Q	Q_3	Input
H	H	H	L	E	SIO_0→Y_0, Y_1, Y_2, Y_3	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	H	H	H	F	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	L	Hold	Hi-Z	Hi-Z

Parity = $F_3 \forall F_2 \forall F_1 \forall F_0 \forall SIO_3$
$\forall$ = Exclusive OR

L = LOW
H = HIGH

Hi-Z = High Impedance

TABLE 4. SPECIAL FUNCTIONS FOR $I_4 = I_3 = I_2 = I_1 = I_0$ = LOW (Note 4)

(Hex) $I_8I_7I_6I_5$	Special Function	ALU Function	ALU Shifter Function	SIO_3 Most Sig Slice	SIO_3 Other Slices	SIO_0	Q Reg & Shifter Function	QIO_3	QIO_0	$\overline{WRITE}$
0	Unsigned Multiply	F = S + C_n if Z = L F = R + S + C_n if Z = H	Log F/2 → Y (Note 1)	Z	Input	F_0	Log Q/2 → Q	Input	Q_0	L
1	(Note 5)									
2	Two's Complement Multiply	F = S + C_n if Z = L F = R + S + C_n if Z = H	Log F/2 → Y (Note 2)	Z	Input	F_0	Log Q/2 → Q	Input	Q_0	L
3	(Note 5)									
4	Increment by One or Two	F = S + 1 + C_n	F → Y	Input	Input	Parity	Hold	Z	Z	L
5	Sign/Magnitude Two's Complement	F = $\overline{S}$ + C_n if Z = L F = $\overline{S}$ + C_n if Z = H	F → Y (Note 3)	Input	Input	Parity	Hold	Z	Z	L
6	Two's Complement Multiply, Last Cycle	F = S + C_n if Z = L F = S − R − 1 + C_n if Z = H	Log F/2 → Y (Note 2)	Z	Input	F_0	Log Q/2 → Q	Input	Q_0	L
7	(Note 5)									
8	Single Length Normalize	F = S + C_n	F → Y	F_3	F_3	Z	Log 2Q → Q	Q_3	Input	L
9	Binary to BCD Conversion	(Note 5)	Log 2F → Y	F_3	F_3	Input	Log 2Q → Q	Q_3	Input	L
A	Double Length Normalize and First Divide Op	F = S + C_n	Log 2F → Y	$R_3 \forall F_3$	F_3	Input	Log 2Q → Q	Q_3	Input	L
B	(Note 5)									
C	Two's Complement Divide	F = S + R + C_n if Z = L F = S − R − 1 + C_n if Z = H	Log 2F → Y	$\overline{R_3 \forall F}$	F_3	Input	Log 2Q → Q	Q_3	Input	L
D	(Note 5)									
E	Two's Complement Divide Correction and Remainder	F = S + R + C_n if Z = L F = S − R − 1 + C_n if Z = H	F → Y	F_3	F_3	Z	Log 2Q → Q	Q_3	Input	L
F	(Note 5)									

Notes:
1. At the most significant slice only, the C_{n+4} signal is internally gated to the Y_3 output.
2. At the most significant slice only, $F_3 \forall$ OVR is internally gated to the Y_3 output.
3. At the most significant slice only, $S_3 \forall F_3$ is generated at the Y_3 output.
4. The Q Register cannot be used explicitly as an operand for any Special Functions. It is defined implicitly within the functions.
5. Available on Am29203 only.

L = LOW Hi-Z = High Impedance
H = HIGH $\forall$ = Exclusive OR
X = Don't Care Parity = $SIO_3 \forall F_3 \forall F_2 \forall F_1 \forall F_0$

The zero, Z, pin is an open collector input/output that can be wire-OR'ed between slices. As an output it can be used as a zero detect status flag and generally indicates that the Y_{0-3} pins are all LOW. To some extent the meaning of this signal varies with the instruction being performed. Refer to Table 5 for an exact definition of this signal as a function of the Am2903 instructions.

Instruction Decoder

The Instruction Decoder generates required internal control signals as a function of the nine Instruction inputs, I_{0-8}; the Instruction Enable input, $\overline{IEN}$; the $\overline{LSS}$ input; and the $\overline{WRITE}/\overline{MSS}$ input/output.

The $\overline{WRITE}$ output is LOW when an instruction which writes data into the RAM is being executed. Refer to Tables 3 and 4 for a definition of the $\overline{WRITE}$ output as a function of the Am2903 instruction inputs.

On the Am2903, when $\overline{IEN}$ is HIGH, the $\overline{WRITE}$ output is forced HIGH and the Q Register and Sign Compare Flip-Flop contents are preserved. When $\overline{IEN}$ is LOW, the $\overline{WRITE}$ output is enabled and the Q Register and Sign Compare Flip-Flop can be written according to the Am2903 instruction. The Sign Compare Flip-Flop is an on-chip flip-flop which is used during an Am2903 divide operation (see Figure B). On the Am29203, $\overline{IEN}$ controls internal writing, but does not affect $\overline{WRITE}$. The $\overline{IEN}$ signal can then be controlled separately at each chip to facilitate byte operations.

Programming the Am2903 Slice Position

Tying the $\overline{LSS}$ input LOW programs the slice to operate as a least significant slice (LSS) and enables the $\overline{WRITE}$ output signal onto the $\overline{WRITE}/\overline{MSS}$ bidirectional I/O pin. When $\overline{LSS}$ is tied HIGH, the $\overline{WRITE}/\overline{MSS}$ pin becomes an input pin; tying the $\overline{WRITE}/\overline{MSS}$ pin HIGH programs the slice to operate as an intermediate slice (IS) and tying it LOW programs the slice to operate as a most significant slice (MSS). The $\overline{W}/\overline{MSS}$ pin must be tied HIGH through a resistor. $\overline{W}/\overline{MSS}$ and $\overline{LSS}$ should not be connected together. See Figure 2 of applications.

Am2903 SPECIAL FUNCTIONS

The Am2903 provides nine Special Functions which facilitate the implementation of the following operations:

- Single- and Double-Length Normalization
- Two's Complement Division
- Unsigned and Two's Complement Multiplication
- Conversion Between Two's Complement and Sign/Magnitude Representation
- Incrementation by One or Two

Table 4 defines these Special Functions.

The Single-Length and Double-Length Normalization functions can be used to adjust a single-precision or double-precision floating point number in order to bring its mantissa within a specified range.

Three Special Functions which can be used to perform a two's complement, non-restoring divide operation are provided by the Am2903. These functions provide both single- and double-precision divide operations and can be performed in "n" clock cycles, where "n" is the number of bits in the quotient.

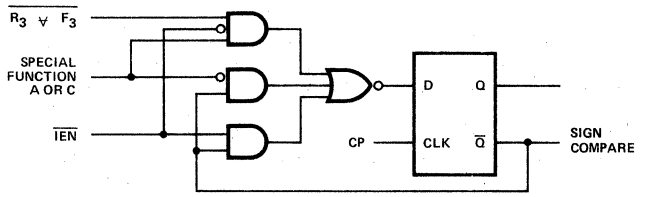
The Unsigned Multiply Special Function and the two Two's Complement Multiply Special Functions can be used to multiply two n-bit, unsigned or two's complement numbers, respectively, in n clock cycles. These functions utilize the conditional add and shift algorithm. During the last cycle of the two's complement multiplication, a conditional subtraction, rather than addition, is performed because the sign bit of the multiplier carries negative weight.

The Sign/Magnitude-Two's Complement Special Function can be used to convert number representation systems. A number expressed in Sign/Magnitude representation can be converted to the Two's Complement representation, and vice-versa, in one clock cycle.

The Increment by One or Two Special Function can be used to increment an unsigned or two's complement number by one or two. This is useful in 16-bit word, byte-addressable machines, where the word addresses are multiples of two.

Refer to Am2903 applications section for a more detailed description of these Special Functions.

Figure B. Sign Compare Flip-Flop



The sign compare signal appears at the Z output of the most significant slice during special functions C, D and E, F. Refer to Table 5.

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TABLE 5. Am2903 STATUS OUTPUTS

(Hex) $I_8I_7I_6I_5$	(Hex) $I_4I_3I_2I_1$	I_0	GI (i = 0 to 3)	PI (i = 0 to 3)	C_{n+4}	$\overline{P}$/OVR Most Sig Slice	$\overline{P}$/OVR Other Slices	$\overline{G}$/N Most Sig Slice	$\overline{G}$/N Other Slices	Z ($\overline{OE}_Y$ = LOW) Most Sig Slice	Z ($\overline{OE}_Y$ = LOW) Intermediate Slice	Z ($\overline{OE}_Y$ = LOW) Least Sig Slice
X	0	X	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	1	X	$R_i \wedge S_i$	$\overline{R_i} \vee S_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	2	X	$R_i \wedge S_i$	$R_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	3	X	$R_i \wedge S_i$	$R_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	4	X	0	S_i	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	5	X	0	$\overline{S_i}$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	6	X	0	R_i	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	7	X	0	$\overline{R_i}$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	8	X	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	9	X	$\overline{R_i} \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	A	X	$R_i \wedge S_i$	$R_i \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	B	X	$\overline{R_i} \wedge S_i$	$\overline{R_i} \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	C	X	$R_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	D	X	$\overline{R_i} \wedge \overline{S_i}$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	E	X	$R_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	F	X	$\overline{R_i} \wedge \overline{S_i}$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
0	0	L	0 if Z = L $R_i \wedge S_i$ if Z = H	S_i if Z = L $R_i \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
	0	L	(Note 6)									
1	8	L	(Note 6)									
2	0	L	0 if Z = L $R_i \wedge S_i$ if Z = H	S_i if Z = L $R_i \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
3	0	L	(Note 6)									
4	0	L	(Note 1)	(Note 2)	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
5	0	L	0	S_i if Z = L S_i if Z = H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3 if Z = L $F_3 \forall S_3$ if Z = H	$\overline{G}$	S_3	Input	Input
6	0	L	0 if Z = L $R_i \wedge S_i$ if Z = H	S_i if Z = L $R_i \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
7	0	L	(Note 6)									
8	0	L	0	S_i	(Note 3)	Q_2 Q_1	$\overline{P}$	Q_3	$\overline{G}$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
9	0	L	(Note 6)									
9	8	L	(Note 6)									
A	0	L	0	S_i	(Note 4)	F_2 F_1	$\overline{P}$	F_3	$\overline{G}$	(Note 5)	(Note 5)	(Note 5)
B	0	L	(Note 6)									
C	0	L	$R_i \wedge S_i$ if Z = L $\overline{R_i} \wedge S_i$ if Z = H	$R_i \vee S_i$ if Z = L $\overline{R_i} \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input
D	0	L	(Note 6)									
E	0	L	$R_i \wedge S_i$ if Z = L $\overline{R_i} \wedge S_i$ if Z = H	$R_i \vee S_i$ if Z = L $\overline{R_i} \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input
F	0	L	(Note 6)									

Notes:
1. If $\overline{LSS}$ is LOW, $G_0 = S_0$ and $G_{1,2,3} = 0$. If $\overline{LSS}$ is HIGH, $G_{0,1,2,3} = 0$.
2. If $\overline{LSS}$ is LOW, $P_0 = 1$ and $P_{1,2,3} = S_{1,2,3}$. If $\overline{LSS}$ is HIGH, $P_i = S_i$.
3. At the most significant slice, $C_{n+4} = Q_3 \forall Q_2$. At other slices, $C_{n+4} = G \vee PC_n$.
4. At the most significant slice, $C_{n+4} = F_3 \forall F_2$. At other slices, $C_{n+4} = G \vee PC_n$.
5. $Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3\overline{F}_0\overline{F}_1\overline{F}_2\overline{F}_3$.
6. Am29203 only.

L = LOW = 0
H = HIGH = 1
= OR
= AND
= EXCLUSIVE OR

P = $P_3P_2P_1P_0$

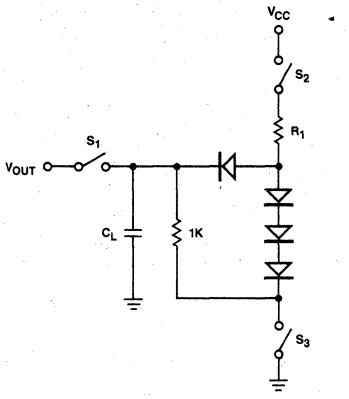
G = $G_3 \vee G_2P_3 \vee G_1P_2P_3 \vee G_0P_1P_2P_3$

C_{n+3} = $G_2 \vee G_1P_2 \vee G_0P_1P_2 \vee C_nP_0P_1P_2$

5

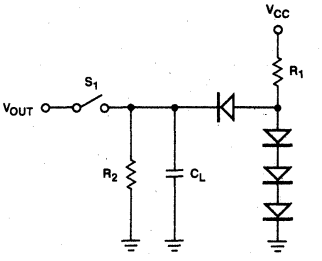
TEST OUTPUT LOAD CONFIGURATIONS FOR Am2903

A. THREE-STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

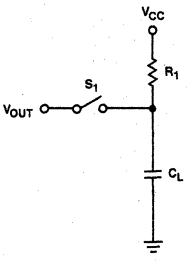
B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

C. OPEN-COLLECTOR OUTPUTS



$$R_1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in hand in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all A.C. tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2903

Pin#	Pin Label	Test Circuit	R_1	R_2
1	QIO_0	A	458	1K
11	C_{n+4}	B	478	3K
12	$\overline{P}$/OVR	B	383	3K
14	$\overline{G}$/N	B	212	1.5K
16-19	Y_{0-3}	A	241	1K
20	SIO_0	A	458	1K
21	SIO_3	A	458	1K
22	Z	C	281	–
23-26	DB_{0-3}	A	458	1K
40	$\overline{WRITE}/\overline{MSS}$	A	458	1K
48	QIO_3	A	458	1K

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

OPERATING RANGES (over which DC, switching, and functional specifications apply)

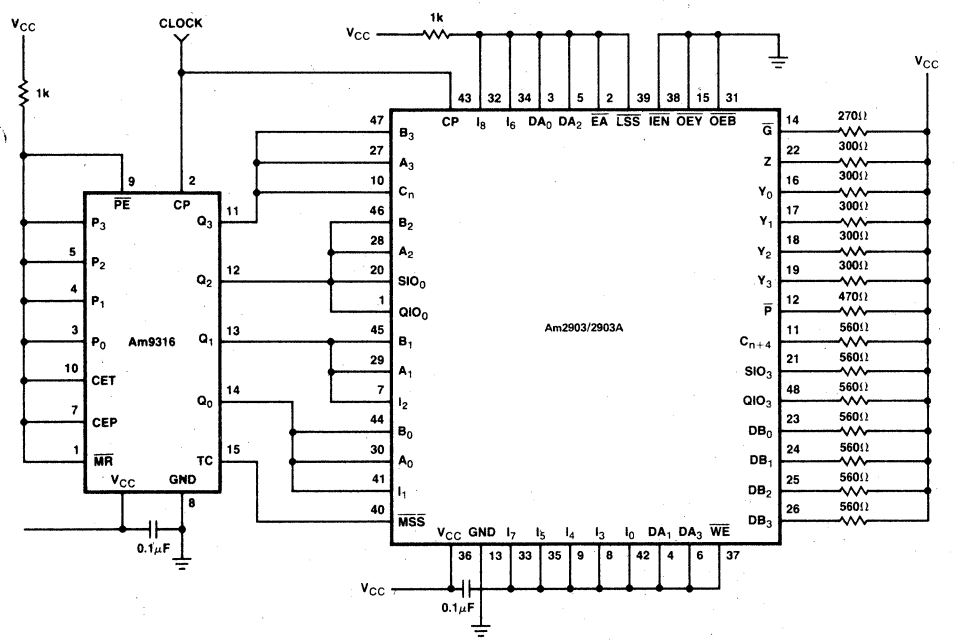
Range	Part Number Suffix	Temperature	V_{CC}
COM'L	PC, PCB, DC, DCB, XC	T_A = 0 to +70°C	4.75 to 5.25V
MIL	DM, DMB, FM, FMB, XM	T_C = −55 to +125°C	4.50 to 5.50V

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5 to +V_{CC} max.
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

5

Am2903 Burn-in and Life Test Circuit



Am2903 · Am2903A
DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.6mA Y_0-Y_3, $\overline{G}$/N		2.4			Volts
			I_{OH} = −800μA DB_{0-3}, $\overline{P}$/OVR SIO_0, SIO_3, QIO_0, QIO_3, $\overline{WRITE}$, C_{n+4}		2.4			
I_{CEX}	Output Leakage Current for Z Output (Note 4)	V_{CC} = MIN., V_{OH} = 5.5V V_{IN} = V_{IH} or V_{IL}					250	μA
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} = or V_{IL}	Y_0, Y_1, Y_2 Y_3, Z	I_{OL} = 20mA (COM'L)			0.5	Volts
				I_{OL} = 16mA (MIL)				
			DB_0, DB_1, DB_2, DB_3	I_{OL} = 12mA (COM'L)			0.5	
				I_{OL} = 8.0mA (MIL)				
			$\overline{G}$/N	I_{OL} = 18mA			0.5	
			$\overline{P}$/OVR	I_{OL} = 10mA			0.5	
			C_{n+4}, SIO_0 SIO_3, QIO_0 QIO_3, $\overline{WRITE}$	I_{OL} = 8.0mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 6)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 6)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V (Note 4)	C_n				−3.6	mA
			Y_0, Y_1, Y_2, Y_3				−1.13	
			I_0, I_1, I_2, I_3, I_4 DA_0, DA_1, DA_2, DA_3				−0.72	
			SIO_0, SIO_3, QIO_0, QIO_3, $\overline{MSS}$, DB_0, DB_1, DB_2, DB_3				−0.77	
			All other inputs				−0.36	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V (Note 4)	C_n				200	μA
			Y_0, Y_1, Y_2, Y_3				110	
			I_0-I_4, DA_0-DA_3				40	
			SIO_0, SIO_3, QIO_0, QIO_3, DB_{0-3}, $\overline{MSS}$				90	
			All other inputs				20	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (HIGH Impedance) Output Current	V_{CC} = MAX., (Note 4)	Y_0-Y_3	V_O = 2.4V			110	μA
				V_O = 0.5V			−1130	
			DB_{0-3}, QIO_0, QIO_3, SIO_0, SIO_3, $\overline{WRITE}$/$\overline{MSS}$	V_O = 2.4V			90	
				V_O = 0.5V			−770	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = MAX + 0.5V V_O = 0.5V			−30		−85	mA
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX.	T_A = 25°C			220	335	mA
			COM'L	T_A = 0 to 70°C			350	
				T_A = 70°C			291	
			MIL	T_C = −55 to 125°C			395	
				T_C = 125°C			258	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Y_{0-3}, DB_{0-3}, $SIO_{0,3}$, $QIO_{0,3}$ and WRITE/MSS are three state outputs internally connected to TTL inputs. Z is an open-collector output internally connected to a TTL input. Input characteristics are measured under conditions such that the outputs are in the OFF state.
5. Worst case I_{CC} is at minimum temperature.
6. These input levels provide zero noise immunity and should only be static tested in a noise-free environment (not functionally tested).

I. Am2903 Guaranteed Commercial Range Performance

The tables below specify the guaranteed performance of the Am2903 over the commercial operating range of 0 to +70°C, with V_{CC} from 4.75 to 5.25V. All data are in ns, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

Clock and Write Pulse Characteristics
All Functions

Minimum Clock LOW Time	30	ns
Minimum Clock HIGH Time	30	ns
Minimum Time CP and WE both LOW to Write	30	ns

Enable/Disable Times
All Functions

From	To	Enable	Disable	
OEY	Y_i	27	25	ns
OEB	DB_i	31	25	ns
I_8	SIO_0, SIO_3		25	ns
I_{8765}	QIO_0, QIO_3		60	ns
I_{43210}	QIO_0, QIO_3	65	60	ns
$\overline{LSS}$	$\overline{WRITE}$	31	25	ns

Note:
1. C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

Combinational Delays
All Functions

From Input \ To Output	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A Address (Arith. Mode)	86	81	69	110	86	108	–	–	–	84	94	115
B Address	99	88	81	123	99	112	49	–	–	94	104	140
A Address (Logic Mode)	87	–	68	111	89	–	–	–	–	79	94	115
B Address	84	–	73	108	84	–	49	–	–	84	90	120
DA Inputs (Arith. Mode)	63	60	49	87	64	89	–	–	–	60	70	101
DB Inputs	61	59	47	85	62	84	–	–	–	62	68	98
DA Inputs (Logic Mode)	64	–	48	88	66	–	–	–	–	61	72	101
DB Inputs	55	–	32	79	57	–	–	–	–	52	61	93
$\overline{EA}$	59	53	42	83	59	83	–	–	–	57	64	98
C_n	40	30	–	64	40	58	–	–	–	38	46	67
I_0	52	48	36	76	52	63	–	49	*	50*	58*	93*
I_{4321}	71	65	72	95	69	84	–	49	*	66*	73*	105*
I_{8765}	42	–	–	66	–	–	–	50	60*	42*	45*	42*
$\overline{IEN}$	–	–	–	–	–	–	–	22	–	–	–	–
SIO_3, SIO_0	26	–	–	50	–	–	–	–	–	–	29	36
Clock	87	87	71	111	88	108	37	–	40	84	92	105
Y	–	–	–	24	–	–	–	–	–	–	–	–
$\overline{MSS}$	44	–	44	68	44	44	–	–	–	44	46	44

Note: An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an * is the delay to correct data on an enabled output. An * shown without a number means the output is disabled by the input or it is enabled but the delay to correct the data is determined by something else.

Setup and Hold Times
All Functions

CAUTION: READ NOTES. NA = Not Applicable; no timing constraint.

From Input \ To Output	With Respect to this Signal	HIGH-to-LOW Set-up	HIGH-to-LOW Hold	LOW-to-HIGH Set-up	LOW-to-HIGH Hold	Comment
Y	Clock	NA	NA	20	3	To store Y in RAM or Q
$\overline{WE}$ HIGH	Clock	25	Note 2	Note 2	0	To Prevent Writing
$\overline{WE}$ LOW	Clock	NA	NA	30	0	To Write into RAM
A, B as Sources	Clock	33	3	NA	NA	See Note 3
B as a Destination	Clock and WE both LOW	6	Note 4	Note 4	3	To Write Data only into the Correct B Address
QIO_0, QIO_3	Clock	NA	NA	21	3	To Shift Q
I_{8765}	Clock	24	Note 5	Note 5	0	
$\overline{IEN}$ HIGH	Clock	30	Note 2	Note 2	0	To Prevent Writing into Q
$\overline{IEN}$ LOW	Clock	NA	NA	30	0	To Write into Q
I_{43210}	Clock	24	–	68	0	See Note 6

Notes:
1. For setup times from all inputs not specified, the setup time is computed by calculating the delay to stable Y outputs and then allowing the Y setup time. Even if the RAM is not being loaded, the Y setup time is necessary to set up the Q register. All unspecified hold times are less than or equal to zero relative to the clock LOW-to-HIGH edge.
2. WE controls writing into the RAM. IEN controls writing into Q and, indirectly, controls $\overline{WE}$ through the write output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must be HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
3. A and B addresses must be set-up prior to clock LOW transition to capture data in latches at RAM output.
4. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
5. Because I_{8765} control the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, preventing writing.
6. The set-up time prior to the clock LOW-to-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-to-LOW transition and the clock LOW time. The actual set-up time requirement on I_{43210}, relative to the clock LOW-to-HIGH transition, is the longer of (1) the set-up time prior to clock L → H, and (2) the sum of the set-up time prior to clock H → L and the clock LOW time.

II. Am2903 Guaranteed Military Range Performance

The tables below specify the guaranteed performance of the Am2903 over the military operating range of −55 to +125°C, with V_{CC} from 4.5 to 5.5V. All data are in ns, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

Clock and Write Pulse Characteristics
All Functions

Minimum Clock LOW Time	40	ns
Minimum Clock HIGH Time	40	ns
Minimum Time CP and WE both LOW to Write	40	ns

Enable/Disable Times
All Functions

From	To	Enable	Disable	
OEY	Y_i	27	25	ns
OEB	DB_i	34	25	ns
I_8	SIO_0, SIO_3		25	ns
I_{8765}	QIO_0, QIO_3		60	ns
I_{43210}	QIO_0, QIO_3	70	60	ns
$\overline{LSS}$	$\overline{WRITE}$	34	25	ns

Note:
1. C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

Combinational Delays
All Functions

From Input \ To Output	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A Address (Arith. Mode)	91	85	72	116	92	115	–	–	–	89	98	120
B Address	101	93	84	126	102	118	52	–	–	97	106	148
A Address (Logic Mode)	92	–	72	117	93	–	–	–	–	84	98	120
B Address	86	–	73	111	89	–	52	–	–	86	92	125
DA Inputs (Arith. Mode)	64	62	51	89	66	94	–	–	–	62	71	107
DB Inputs	63	60	48	88	63	89	–	–	–	64	68	100
DA Inputs (Logic Mode)	65	–	51	90	67	–	–	–	–	62	72	108
DB Inputs	56	–	32	81	57	–	–	–	–	52	63	100
$\overline{EA}$	60	56	43	85	60	87	–	–	–	58	64	103
C_n	40	30	–	65	40	59	–	–	–	38	46	69
I_0	52	50	36	77	52	66	–	53	*	51 *	58 *	96 *
I_{4321}	72	69	73	97	71	88	–	53	*	66 *	75 *	111 *
I_{8765}	44	–	–	69	–	–	–	50	65 *	42 *	45 *	42 *
$\overline{IEN}$	–	–	–	–	–	–	–	24	–	–	–	–
SIO_3, SIO_0	26	–	–	51	–	–	–	–	–	–	29	36
Clock	89	90	74	114	89	116	39	–	42	91	96	110
Y	–	–	–	25	–	–	–	–	–	–	–	–
$\overline{MSS}$	45	–	44	70	44	44	–	–	–	44	46	44

Note: An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an * is the delay to correct data on an enabled output. An * shown without a number means the output is disabled by the input or it is enabled but the delay to correct the data is determined by something else.

Setup and Hold Times
All Functions

CAUTION: READ NOTES. NA = Not Applicable; no timing constraint.

Input	With Respect to this Signal	HIGH-to-LOW Set-up	HIGH-to-LOW Hold	LOW-to-HIGH Set-up	LOW-to-HIGH Hold	Comment
Y	Clock	NA	NA	23	3	To store Y in RAM or Q
$\overline{WE}$ HIGH	Clock	25	Note 2	Note 2	0	To Prevent Writing
$\overline{WE}$ LOW	Clock	NA	NA	35	0	To Write into RAM
A, B as Sources	Clock	38	3	NA	NA	See Note 3
B as a Destination	Clock and WE both LOW	6	Note 4	Note 4	3	To Write Data only into the Correct B Address
QIO_0, QIO_3	Clock	NA	NA	23	3	To Shift Q
I_{8765}	Clock	24	Note 5	Note 5	0	
$\overline{IEN}$ HIGH	Clock	30	Note 2	Note 2	0	To Prevent Writing into Q
$\overline{IEN}$ LOW	Clock	NA	NA	30	0	To Write into Q
I_{43210}	Clock	24	–	74	0	See Note 6

Notes:
1. For setup times from all inputs not specified, the setup time is computed by calculating the delay to stable Y outputs and then allowing the Y setup time. Even if the RAM is not being loaded, the Y setup time is necessary to set up the Q register. All unspecified hold times are less than or equal to zero relative to the clock LOW-to-HIGH edge.
2. $\overline{WE}$ controls writing into the RAM. $\overline{IEN}$ controls writing into Q and, indirectly, controls $\overline{WE}$ through the write output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must be HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
3. A and B addresses must be set-up prior to clock LOW transition to capture data in latches at RAM output.
4. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
5. Because I_{8765} control the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, preventing writing.
6. The set-up time prior to the clock LOW-to-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-to-LOW transition and the clock LOW time. The actual set-up time requirement on I_{43210}, relative to the clock LOW-to-HIGH transition, is the longer of (1) the set-up time prior to clock L → H, and (2) the sum of the set-up time prior to clock H → L and the clock LOW time.

I. Am2903A Preliminary Commercial Range Performance

The tables below specify the preliminary performance of the Am2903 over the commercial operating range of 0 to +70°C, with V_{CC} from 4.75 to 5.25V. All data are in ns, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

Clock and Write Pulse Characteristics
All Functions

Minimum Clock LOW Time		ns
Minimum Clock HIGH Time		ns
Minimum Time CP and WE both LOW to Write		ns

Enable/Disable Times
All Functions

From	To	Enable	Disable	
OEY	Y_i			ns
OEB	DB_i			ns
I_8	SIO_0, SIO_3			ns
I_{8765}	QIO_0, QIO_3			ns
I_{43210}	QIO_0, QIO_3			ns
$\overline{LSS}$	$\overline{WRITE}$			ns

Note:
1. C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

Combinational Delays
All Functions

From Input \ To Output	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A Address (Arith. Mode)							–	–	–			
B Address								–	–			
A Address (Logic Mode)		–				–	–	–	–			
B Address		–				–		–	–			
DA Inputs (Arith. Mode)							–	–	–			
DB Inputs							–	–	–			
DA Inputs (Logic Mode)		–				–	–	–	–			
DB Inputs		–				–	–	–	–			
$\overline{EA}$							–	–	–			
C_n			–				–	–	–			
I_0							–		*			
I_{4321}							–		*			
I_{8765}		–	–		–	–	–					
$\overline{IEN}$	–	–	–	–	–	–	–		–	–	–	–
SIO_3, SIO_0		–	–		–	–	–	–	–	–		
Clock								–				
Y	–	–	–		–	–	–	–	–	–	–	–
$\overline{MSS}$		–					–	–	–			

Note: An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an * is the delay to correct data on an enabled output. An * shown without a number means the output is disabled by the input or it is enabled but the delay to correct the data is determined by something else.

Setup and Hold Times
All Functions

CAUTION: READ NOTES. NA = Not Applicable; no timing constraint.

From Input \ To Output	With Respect to this Signal	HIGH-to-LOW Set-up	HIGH-to-LOW Hold	LOW-to-HIGH Set-up	LOW-to-HIGH Hold	Comment
Y	Clock	NA	NA			To store Y in RAM or Q
$\overline{WE}$ HIGH	Clock		Note 2	Note 2		To Prevent Writing
$\overline{WE}$ LOW	Clock	NA	NA			To Write into RAM
A, B as Sources	Clock			NA	NA	See Note 3
B as a Destination	Clock and WE both LOW		Note 4	Note 4		To Write Data only into the Correct B Address
QIO_0, QIO_3	Clock	NA	NA			To Shift Q
I_{8765}	Clock		Note 5	Note 5		
$\overline{IEN}$ HIGH	Clock		Note 2	Note 2		To Prevent Writing into Q
$\overline{IEN}$ LOW	Clock	NA	NA			To Write into Q
I_{43210}	Clock		–			See Note 6

Notes:
1. For setup times from all inputs not specified, the setup time is computed by calculating the delay to stable Y outputs and then allowing the Y setup time. Even if the RAM is not being loaded, the Y setup time is necessary to set up the Q register. All unspecified hold times are less than or equal to zero relative to the clock LOW-to-HIGH edge.
2. WE controls writing into the RAM. IEN controls writing into Q and, indirectly, controls $\overline{WE}$ through the write output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must be HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
3. A and B addresses must be set-up prior to clock LOW transition to capture data in latches at RAM output.
4. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
5. Because I_{8765} control the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, preventing writing.
6. The set-up time prior to the clock LOW-to-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-to-LOW transition and the clock LOW time. The actual set-up time requirement on I_{43210}, relative to the clock LOW-to-HIGH transition, is the longer of (1) the set-up time prior to clock L → H, and (2) the sum of the set-up time prior to clock H → L and the clock LOW time.

5

II. Am2903A Preliminary Military Range Performance

The tables below specify the preliminary performance of the Am2903 over the military operating range of −55 to +125°C, with V_{CC} from 4.5 to 5.5V. All data are in ns, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

Clock and Write Pulse Characteristics
All Functions

Minimum Clock LOW Time		ns
Minimum Clock HIGH Time		ns
Minimum Time CP and WE both LOW to Write		ns

Enable/Disable Times
All Functions

From	To	Enable	Disable	
OEY	Y_i			ns
OEB	DB_i			ns
I_8	SIO_0, SIO_3			ns
I_{8765}	QIO_0, QIO_3			ns
I_{43210}	QIO_0, QIO_3			ns
$\overline{LSS}$	$\overline{WRITE}$			ns

Note:
1. C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

Combinational Delays
All Functions

From Input \ To Output	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A Address (Arith. Mode)							–	–	–			
B Address								–	–			
A Address (Logic Mode)		–				–	–	–	–			
B Address		–				–		–	–			
DA Inputs (Arith. Mode)							–	–	–			
DB Inputs							–	–	–			
DA Inputs (Logic Mode)		–				–	–	–	–			
DB Inputs		–				–	–	–	–			
$\overline{EA}$							–	–	–			
C_n			–				–	–	–			
I_0							–		*			
I_{4321}							–		*			
I_{8765}		–	–		–	–	–					
$\overline{IEN}$	–	–	–	–	–	–	–		–	–	–	–
SIO_3, SIO_0		–	–		–	–	–	–	–	–		
Clock								–				
Y	–	–	–		–	–	–	–	–	–	–	–
$\overline{MSS}$		–					–	–	–			

Note: An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an * is the delay to correct data on an enabled output. An * shown without a number means the output is disabled by the input or it is enabled but the delay to correct the data is determined by something else.

Setup and Hold Times
All Functions

CAUTION: READ NOTES. NA = Not Applicable; no timing constraint.

Input	With Respect to this Signal	HIGH-to-LOW Set-up	HIGH-to-LOW Hold	LOW-to-HIGH Set-up	LOW-to-HIGH Hold	Comment
Y	Clock	NA	NA			To store Y in RAM or Q
$\overline{WE}$ HIGH	Clock		Note 2	Note 2		To Prevent Writing
$\overline{WE}$ LOW	Clock	NA	NA			To Write into RAM
A, B as Sources	Clock			NA	NA	See Note 3
B as a Destination	Clock and WE both LOW		Note 4	Note 4		To Write Data only into the Correct B Address
QIO_0, QIO_3	Clock	NA	NA			To Shift Q
I_{8765}	Clock		Note 5	Note 5		
$\overline{IEN}$ HIGH	Clock		Note 2	Note 2		To Prevent Writing into Q
$\overline{IEN}$ LOW	Clock	NA	NA			To Write into Q
I_{43210}	Clock					See Note 6

Notes:
1. For setup times from all inputs not specified, the setup time is computed by calculating the delay to stable Y outputs and then allowing the Y setup time. Even if the RAM is not being loaded, the Y setup time is necessary to set up the Q register. All unspecified hold times are less than or equal to zero relative to the clock LOW-to-HIGH edge.
2. $\overline{WE}$ controls writing into the RAM. $\overline{IEN}$ controls writing into Q and, indirectly, controls $\overline{WE}$ through the write output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must be HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
3. A and B addresses must be set-up prior to clock LOW transition to capture data in latches at RAM output.
4. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
5. Because I_{8765} control the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, preventing writing.
6. The set-up time prior to the clock LOW-to-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-to-LOW transition and the clock LOW time. The actual set-up time requirement on I_{43210}, relative to the clock LOW-to-HIGH transition, is the longer of (1) the set-up time prior to clock L → H, and (2) the sum of the set-up time prior to clock H → L and the clock LOW time.

III. Am2903 Guaranteed Combinational Delays for Special Functions.

The switching characteristics of the Am2903 are a function of power supply voltage, temperature, and the operating mode of the device. The following tables define the speeds of the combinational paths for each of the special functions. Setup and hold times do not change for the special functions. Data is shown in boldface where different from the standard function tables.

Except where otherwise noted, data is taken with inputs switching between 0 and 3.0V at 1V/ns, with the measurement point at 1.5V. Outputs are measured at 1.5V and are loaded with C_L = 50pF and maximum DC load.

Times are specified as Commercial Range/Military Range where the commercial operating range is 0 to +70°C, and the military range is −55 to +125°C.

INDEX TO SWITCHING TABLES

COMMERCIAL RANGE/MILITARY RANGE

A. Combinational Delays
Increment by One or Two Instruction
(I_{8765} = 4_H, I_{4321} = 0_H, I_0 = 0)

From Input \ To Output	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith Mode)	MSS	99/101	88/93	–	123/126	99/102	112/118	49/52	–	–	–	–	140/148
	IS, LSS	99/101	88/93	81/84	123/126	–	–	49/52	–	–	–	–	140/148
DA, DB Inputs	MSS	63/64	60/62	–	87	64	89	–	–	–	–	–	101/107
	IS, LSS	63/64	60/62	49/51	87/89	–	–	–	–	–	–	–	101/107
$\overline{EA}$	MSS	–	–	–	–	–	–	–	–	–	–	–	–
	IS, LSS	–	–	–	–	–	–	–	–	–	–	–	–
C_n	MSS	40/40	30/30	–	64/65	40/40	58/59	–	–	–	–	–	67/69
	IS, LSS	40/40	30/30	–	64/65	40/40	58/59	–	–	–	–	–	67/69
I_0	MSS	66/73	60/61	–	90/98	71/72	82/87	–	–	*	*	*	103/110*
	IS	66/73	60/61	58/62	90/98	–	–	–	–	*	*	*	103/110*
	LSS	66/73	60/61	58/62	90/98	–	–	–	49/53	*	*	*	103/110*
I_{4321}	MSS	71/72	60/61	–	95/97	72/74	80/87	–	–	*	*	*	102/110*
	IS	71/72	60/61	58/62	95/97	–	–	–	–	*	*	*	102/110*
	LSS	71/72	60/61	58/62	95/97	–	–	–	49/53	*	*	*	102/110*
I_{8765}	MSS	71/72	60/61	–	95/97	72/74	82/87	–	–	*	*	*	102/110*
	IS	71/72	60/61	58/62	95/97	–	–	–	–	*	*	*	102/110*
	LSS	71/72	60/61	58/62	95/97	–	–	–	50/50	*	*	*	102/110*
Clock	MSS	87/89	87/90	71/74	111/114	88/89	108/116	37/39	–	40/42	–	–	105/110
	IS, LSS	87/89	87/90	71/74	111/114	88/89	108/116	37/39	–	40/42	–	–	105/110
Z	MSS	Z is an Output											
	IS, LSS	Z is an Output											
Y	Any	–	–	–	24/25	–	–	–	–	–	–	–	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	22/24	–	–	–	–
SIO_3, SIO_0	Any	26/26	–	–	–	–	–	–	–	–	–	–	–

$F = S + 1 + C_n$

Notes: 1. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an * is the delay to correct data on an enabled output. An * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in boldface is different from standard function table; other data is the same.

B. Combinational Delays
Two's Complement Multiply Instruction
(I_{8765} = 2_H, I_{4321} = 0_H, I_0 = 0)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith Mode)	MSS	106/113	88/93	–	–	99/102	112/118	49/52	–	–	94/97	–	–
	IS, LSS	99/101	88/93	81/84	–	–	–	49/52	–	–	94/97	–	–
DA, DB Inputs	MSS	78/78	60/62	–	–	64/66	89/94	–	–	–	62/64	–	–
	IS, LSS	63/64	60/62	49/51	–	–	–	–	–	–	62/64	–	–
$\overline{EA}$	MSS	85/85	53/56	–	–	59/60	83/87	–	–	–	57/58	–	–
	IS, LSS	59/60	53/56	42/43	–	–	–	–	–	–	57/58	–	–
C_n	MSS	58/58	30/30	–	–	40/40	58/59	–	–	–	38/38	–	–
	IS, LSS	40/40	30/30	–	–	–	–	–	–	–	38/38	–	–
I_0	MSS	104/105	95/97	–	–	89/89	102/102	–	–	*	68/71*	*	–
	IS	104/105	95/97	78/81	–	–	–	–	–	*	68/71*	*	–
	LSS	104/105	95/97	78/81	42/42	–	–	–	49/53	*	68/71*	*	–
I_{4321}	MSS	112/112	95/98	–	–	94/94	108/111	–	–	*	71/75*	*	–
	IS	112/112	95/98	78/85	–	–	–	–	–	*	71/75*	*	–
	LSS	112/112	95/98	78/85	43/43	–	–	–	49/53	*	71/75*	*	–
I_{8765}	MSS	98/99	84/86	–	–	76/78	100/100	–	–	*	71/74*	*	–
	IS	98/99	84/86	82/84	–	–	–	–	–	*	71/74*	*	–
	LSS	98/99	84/86	82/84	46/48	–	–	–	50/50	*	71/74*	*	–
Clock	MSS	100/107	87/90	–	–	88/89	108/116	37/39	–	40/42	84/91	–	–
	IS, LSS	87/89	87/90	71/74	53/57	–	–	37/39	–	40/42	84/91	–	–
Z	MSS	90/90	62/65	–	–	69/70	78/81	–	–	–	71/72	–	–
	IS	90/90	62/65	48/48	–	–	–	–	–	–	71/72	–	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	22/24	–	–	–	–
SIO_3, SIO_0	Any	26/26	–	–	–	–	–	–	–	–	–	–	–

F = S – C_n if Z = 0
R – S – C_n if Z = 1

Y_3 = F_3 ⊕ OVR (MSS)

Z = Q_0 (LSS)

Notes: 1. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an * is the delay to correct data on an enabled output. An * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in boldface is different from standard function table; other data is the same.

COMMERCIAL RANGE/MILITARY RANGE (Cont.)

C. Combinational Delays
Unsigned Multiply Instruction
($I_{8765} = 0_H$, $I_{4321} = 0_H$, $I_0 = 0$)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith Mode)	MSS	102/103	88/93	–	–	99/102	112/118	49/52	–	–	94/97	–	–
	IS, LSS	99/101	88/93	81/84	–	–	–	49/52	–	–	94/97	–	–
DA, DB Inputs	MSS	65/66	60/62	–	–	64/66	89/94	–	–	–	62/64	–	–
	IS, LSS	63/64	60/62	49/51	–	–	–	–	–	–	62/64	–	–
$\overline{EA}$	MSS	73/74	53/56	–	–	59/60	83/87	–	–	–	57/58	–	–
	IS, LSS	59/60	53/56	42/43	–	–	–	–	–	–	57/58	–	–
C_n	MSS	45/45	30/30	–	–	40/40	58/59	–	–	–	38/38	–	–
	IS, LSS	40/40	30/30	–	–	–	–	–	–	–	38/38	–	–
I_0	MSS	94/97	95/97	–	–	87/87	102/106	–	–	*	70/71*	*	–
	IS	94/97	95/97	80/85	–	–	–	–	–	*	70/71*	*	–
	LSS	94/97	95/97	80/85	42/42	–	–	–	49/53	*	70/71*	*	–
I_{4321}	MSS	102/103	96/100	–	–	92/94	110/111	–	–	*	72/73*	*	–
	IS	102/103	96/100	81/86	–	–	–	–	–	*	72/73*	*	–
	LSS	102/103	96/100	81/86	43/43	–	–	–	49/53	*	72/73*	*	–
I_{8765}	MSS	102/102	90/93	–	–	77/76	84/89	–	–	*	72/75*	*	–
	IS	102/102	90/93	84/92	–	–	–	–	–	*	72/75*	*	–
	LSS	102/102	90/93	84/92	46/51	–	–	–	50/50	*	72/75*	*	–
Clock	MSS	91/94	87/90	–	–	88/89	108/116	37/39	–	40/42	84/91	–	–
	IS, LSS	87/89	87/90	71/74	53/57	–	–	37/39	–	40/42	84/91	–	–
Z	MSS	74/76	62/65	–	–	70/70	78/81	–	–	–	71/72	–	–
	IS	74/76	62/65	48/49	–	–	–	–	–	–	71/72	–	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	22/24	–	–	–	
SIO_3, SIO_0	Any	26/26	–	–	–	–	–	–	–	–	–	–	–

F = S + C_n if Z = 0
S + R + C_n if Z = 1

Y_3 = C_{n+4} (MSS)

Z = Q_0 (LSS)

Notes: 1. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an * is the the delay to correct data on an enabled output. An * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in boldface is different from standard function table; other data is the same.

D. Combinational Delays
Two's Complement Multiply, Last Cycle
($I_{8765} = 6_H$, $I_{4321} = 0_H$, $I_0 = 0$)

From Input \ To Output	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith Mode)	MSS	120/121	88/93	–	–	99/102	112/118	49/52	–	–	94/97	–	–
	IS, LSS	99/101	88/93	81/84	–	–	–	49/52	–	–	94/97	–	–
DA, DB Inputs	MSS	85/88	60/62	–	–	64/66	89/94	–	–	–	62/64	–	–
	IS, LSS	63/64	60/62	49/51	–	–	–	–	–	–	62/64	–	–
$\overline{EA}$	MSS	93/96	53/56	–	–	59/60	83/87	–	–	–	57/58	–	–
	IS, LSS	59/60	53/56	42/43	–	–	–	–	–	–	57/58	–	–
C_n	MSS	64/64	30/30	–	–	40/40	58/59	–	–	–	38/38	–	–
	IS, LSS	40/40	30/30	–	–	–	–	–	–	–	38/38	–	–
I_0	MSS	112/118	99/102	–	–	91/97	120/126	–	–	*	98/102*	*	–
	IS	112/118	99/102	86/87	–	–	–	–	–	*	98/102*	*	–
	LSS	112/118	99/102	86/87	42/42	–	–	–	49/53	*	98/102*	*	–
I_{4321}	MSS	115/120	93/101	–	–	94/97	124/127	–	–	*	97/101*	*	–
	IS	115/120	93/101	85/86	–	–	–	–	–	*	97/101*	*	–
	LSS	115/120	93/101	85/86	43/43	–	–	–	49/53	*	97/101*	*	–
I_{8765}	MSS	105/105	93/98	–	–	88/88	114/115	–	–	*	96/102*	*	–
	IS	105/105	93/98	78/86	–	–	–	–	–	*	96/102*	*	–
	LSS	105/105	93/98	78/86	50/51	–	–	–	50/50	*	96/102*	*	–
Clock	MSS	110/110	87/90	–	–	88/89	108/116	37/39	–	40/42	84/91	–	–
	IS, LSS	87/89	87/90	71/74	53/58	–	–	37/39	–	40/42	84/91	–	–
Z	MSS	91/92	64/67	–	–	74/80	98/103	–	–	–	70/72	–	–
	IS	91/92	64/67	50/53	–	–	–	–	–	–	70/72		
$\overline{IEN}$	Any	–	–	–	–	–	–	–	22/24	–	–	–	
SIO_3, SIO_0	Any	26/26	–	–	–	–	–	–	–	–	–	–	–

F = S + C_n if Z = 0
S − R − 1 + C_n if Z = 1

Y_3 = (OVR ⊕ F_3) MSS

Z = Q_0 (LSS)

Notes: 1. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an * is the delay to correct data on an enabled output. An * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in boldface is different from standard function table; other data is the same.

COMMERCIAL RANGE/MILITARY RANGE (Cont.)

E. Combinational Delays
Sign Magnitude/Two's Complement Conversion
($I_{8765} = 5_H$, $I_{4321} = 0_H$, $I_0 = 0$)

From Input \ To Output	Slice Position	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith Mode)	MSS	138/143	88/93	–	70/78	138/143	112/118	49/52	–	–	–	–	140/148
	IS, LSS	99/101	88/93	81/84	–	–	–	49/52	–	–	–	–	140/148
DA, DB Inputs	MSS	98/103	60/62	–	40/40	98/103	89/94	–	–	–	–	–	101/107
	IS, LSS	63/64	60/62	49/51	–	–	–	–	–	–	–	–	101/107
$\overline{EA}$	MSS	–	–	–	–	–	–	–	–	–	–	–	–
	IS, LSS	–	–	–	–	–	–	–	–	–	–	–	–
C_n	MSS	79/83	30/30	–	–	79/83	58/59	–	–	–	–	–	67/69
	IS, LSS	40/40	30/30	–	–	–	–	–	–	–	–	–	67/69
I_0	MSS	102/102	78/80	–	46/50	100/100	112/115	–	–	*	*	*	131/132*
	IS	102/102	78/80	70/70	–	–	–	–	–	*	*	*	131/132*
	LSS	102/102	78/80	70/70	–	–	–	–	49/53	*	*	*	131/132*
I_{4321}	MSS	102/102	78/80	–	46/50	100/102	103/110	–	–	*	*	*	131/132*
	IS	102/102	78/80	72/75	–	–	–	–	–	*	*	*	131/132*
	LSS	102/102	78/80	72/75	–	–	–	–	49/53	*	*	*	131/132*
I_{8765}	MSS	100/103	78/80	–	46/50	97/100	105/112	–	–	*	*	*	138/142*
	IS	100/103	78/80	65/65	–	–	–	–	–	*	*	*	138/142*
	LSS	100/103	78/80	65/65	–	–	–	–	50/50	*	*	*	138/142*
Clock	MSS	118/120	87/90	71/–	58/61	118/120	108/116	37/39	–	–	–	–	105/110
	IS, LSS	87/89	87/90	71/74	–	–	–	37/39	–	–	–	–	105/110
Z	MSS	Z is an Output											
	IS, LSS	72/76	60/61	48/51	–	–	–	–	–	–	–	–	114/118
$\overline{IEN}$	Any	–	–	–	–	–	–	–	22/24	–	–	–	–
SIO_3, SIO_0	Any	26/26	–	–	–	–	–	–	–	–	–	–	–

F = S + C_n if Z = 0
S + C_n if Z = 1

$Y_3 = S_3 \oplus F_3$ (MSS)

$Z = S_3$ (MSS)

Notes: 1. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an * is the delay to correct data on an enabled output. An * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in boldface is different from standard function table; other data is the same.

F. Combinational Delays
Single-Length Normalize Instruction
($I_{8765} = 8_H$, $I_{4321} = 0_H$, $I_0 = 0$)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith Mode)	MSS	99/101	88/93	–	–	99/102	112/118	49/52	–	–	–	–	–
	IS, LSS	99/101	88/93	81/84	–	–	–	49/52	–	–	–	–	–
DA, DB Inputs	MSS	63/63	60/60	–	–	64/66	89/94	–	–	–	–	–	–
	IS, LSS	63/63	60/60	49/51	–	–	–	–	–	–	–	–	–
$\overline{EA}$	MSS	59/60	53/56	–	–	59/60	83/87	–	–	–	–	–	–
	IS, LSS	59/60	53/56	42/43	–	–	–	–	–	–	–	–	–
C_n	MSS	40/40	30/30	–	–	40/40	58/59	–	–	–	–	–	–
	IS, LSS	40/40	30/30	–	–	–	–	–	–	–	–	–	–
I_0	MSS	67/72	52/60	–	33/34	45/43	42/42	–	–	*	*	72/78*	–
	IS	67/72	52/60	58/59	33/34	–	–	–	–	*	*	72/78*	–
	LSS	67/72	52/60	58/59	33/34	–	–	–	49/53	*	*	72/78*	–
I_{4321}	MSS	68/72	58/60	–	34/38	45/48	47/47	–	–	*	*	72/78*	–
	IS	67/72	58/60	58/60	36/38	–	–	–	–	*	*	72/78*	–
	LSS	68/72	58/60	58/60	36/38	–	–	–	49/53	*	*	72/78*	–
I_{8765}	MSS	66/67	70/58	–	44/50	50/53	47/47	–	–	*	*	72/72*	–
	IS	66/67	70/58	41/42	44/50	–	–	–	–	*	*	72/72*	–
	LSS	66/67	70/58	41/42	44/50	–	–	–	50/50	*	*	72/72*	–
Clock	MSS	87/89	49/53	–	46/53	49/49	47/49	37/39	–	40/42	–	92/96	–
	IS, LSS	87/89	87/90	71/74	48/53	–	–	37/39	–	40/42	–	92/96	–
Z	MSS	Z is an Output											
	IS, LSS	Z is an Output											
$\overline{IEN}$	Any	–	–	–	–	–	–	–	22/24	–	–	–	–
SIO_3, SIO_0	Any	26/26	–	–	–	–	–	–	–	–	–	–	–

F = S + C_n
C_{n+4} = $Q_3 \oplus Q_2$ (MSS)
OVR = $Q_2 \oplus Q_1$ (MSS)
N = Q_3 (MSS)
Z = $\overline{Q_0}\overline{Q_1}\overline{Q_2}\overline{Q_3}$

Notes: 1. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an * is the delay to correct data on an enabled output. An * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in boldface is different from standard function table; other data is the same.

COMMERCIAL RANGE/MILITARY RANGE (Cont.)

G. Combinational Delays
First Divide Operation (Double Length Normalize)
($I_{8765} = A_H$, $I_{4321} = 0_H$, $I_0 = 0$)

To Output / From Input	Slice Position	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith Mode)	MSS	99/101	113/122	–	94/96	94/100	102/112	49/52	–	–	–	120/130	–
	IS, LSS	99/101	88/93	81/84	–/96	–	–	49/52	–	–	–	104/106	–
DA, DB Inputs	MSS	63/64	75/80	–	54/63	54/65	62/72	–	–	–	–	80/84	–
	IS, LSS	63/64	60/62	49/51	–/63	–	–	–	–	–	–	70/71	–
$\overline{EA}$	MSS	–	–	–	–	–	–	–	–	–	–	76/80	–
	IS, LSS	–	–	–	–	–	–	–	–	–	–	64/46	–
C_n	MSS	40/40	54/57	–	45/48	45/48	50/55	–	–	–	–	68/68	–
	IS, LSS	40/40	30/30	–	–/48	–	–	–	–	–	–	46/46	–
I_0	MSS	69/71	95/98	–	68/85	72/72	86/91	–	–	*	*	96/101*	–
	IS	69/71	95/98	56/61	68/85	–	–	–	–	*	*	96/101*	–
	LSS	69/71	95/98	56/61	68/85	–	–	–	49/53	*	*	96/101*	–
I_{4321}	MSS	69/71	94/98	–	68/85	72/76	86/91	–	–	*	*	96/101*	–
	IS	69/71	94/98	57/61	68/85	–	–	–	–	*	*	96/101*	–
	LSS	69/71	94/98	57/61	68/85	–	–	–	49/53	*	*	96/101*	–
I_{8765}	MSS	69/71	95/98	–	68/85	72/76	86/91	–	–	*	*	96/101*	–
	IS	69/71	95/98	57/61	68/85	–	–	–	–	*	*	96/101*	–
	LSS	69/71	95/98	57/61	68/85	–	–	–	50/50	*	*	96/101*	–
Clock	MSS	87/89	101/113	–	80/90	84/87	86/98	37/39	–	40/42	–	106/114	–
	IS, LSS	87/89	87/90	71/74	80/90	–	–	37/39	–	40/42	–	92/96	–
Z	MSS	Z is an Output											
	IS	Z is an Output											
$\overline{IEN}$	Any	–	–	–	–	–	–	–	22/24	–	–	–	–
SIO_3, SIO_0	Any	26/26	–	–	–	–	–	–	–	–	–	–	–

F = $S + C_n$
N = F_3 (MSS)
SIO_3 = $F_3 \oplus R_3$ (MSS)
C_{n+4} = $F_3 \oplus F_2$ (MSS)
OVR = $F_2 \oplus F_1$ (MSS)
Z = $\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3\overline{F}_0\overline{F}_1\overline{F}_2\overline{F}_3$

Notes: 1. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an * is the delay to correct data on an enabled output. An * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in boldface is different from standard function table; other data is the same.

5

H. Combinational Delays
Two's Complement Divide Operation
($I_{8765} = C_H$, $I_{4321} = 0_H$, $I_0 = 0$)

From Input \ To Output	Slice Position	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith Mode)	MSS	99/101	88/93	–	–	99/102	112/118	49/52	–	–	–	107/112	–
	IS, LSS	99/101	88/93	81/84	–	–	–	49/52	–	–	–	104/106	–
DA, DB Inputs	MSS	63/64	60/62	–	–	64/66	89/94	–	–	–	–	84/88	–
	IS, LSS	63/64	60/62	49/51	–	–	–	–	–	–	–	70/71	–
$\overline{EA}$	MSS	59/60	53/56	–	–	59/60	83/87	–	–	–	–	91/96	–
	IS, LSS	59/60	53/56	42/43	–	–	–	–	–	–	–	64/64	–
C_n	MSS	40/40	30/30	–	–	40/40	58/59	–	–	–	–	64/64	–
	IS, LSS	40/40	30/30	–	–	–	–	–	–	–	–	46/46	–
I_0	MSS	94/95	93/96	–	39/42	94/98	120/127	–	–	*	*	108/113*	–
	IS	94/95	93/96	74/77	–	–	–	–	–	*	*	108/113*	–
	LSS	94/95	93/96	74/77	–	–	–	–	49/53	*	*	108/113*	–
I_{4321}	MSS	94/95	84/96	–	42/42	93/97	120/124	–	–	*	*	108/114*	–
	IS	94/96	84/97	74/82	–	–	–	–	–	*	*	108/114*	–
	LSS	94/96	84/97	74/82	–	–	–	–	49/53	*	*	108/114*	–
I_{8765}	MSS	93/98	89/97	–	43/44	93/102	120/112	–	–	*	*	108/119*	–
	IS	93/98	89/97	64/64	–	–	–	–	–	*	*	108/119*	–
	LSS	93/98	89/97	64/64	–	–	–	–	50/50	*	*	108/119*	–
Clock	MSS	87/89	87/90	–	53/58	88/89	108/116	37/39	–	40/42	–	130/136	–
	IS, LSS	87/89	87/90	74/74	–	–	–	37/39	–	40/42	–	92/96	–
Z	MSS	Z is an Output											
	IS, LSS	68/71	65/68	52/56	–	–	–	–	–	–	–	77/81	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	22/24	–	–	–	–
SIO_3, SIO_0	Any	26/26	–	–	–	–	–	–	–	–	–	–	–

F = R + S + C_n if Z = 0
S − R − 1 + C_n if Z = 1

SIO_3 = $\overline{F_3} \oplus \overline{R_3}$ (MSS)

Z = $\overline{F_3} \oplus \overline{R_3}$ (MSS) from previous cycle

Notes: 1. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an * is the delay to correct data on an enabled output. An * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in boldface is different from standard function table; other data is the same.

COMMERCIAL RANGE/MILITARY RANGE (Cont.)

I. Combinational Delays
Two's Complement Divide, Correction
($I_{8765} = E_H$, $I_{4321} = 0_H$, $I_0 = 0$)

From Input \ To Output	Slice Position	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, B Address (Arith Mode)	MSS	99/101	88/93	–	–	99/102	112/118	49/52	–	–	–	104/106	–
	IS, LSS	99/101	88/93	81/84	–	–	–	49/52	–	–	–	104/106	–
DA, DB Inputs	MSS	63/64	60/62	–	–	64/66	89/94	–	–	–	–	70/71	–
	IS, LSS	63/64	60/62	49/51	–	–	–	–	–	–	–	70/71	–
$\overline{EA}$	MSS	59/60	53/56	–	–	59/60	83/87	–	–	–	–	64/64	–
	IS, LSS	59/60	53/56	42/43	–	–	–	–	–	–	–	64/64	–
C_n	MSS	40/40	30/30	–	–	40/40	58/59	–	–	–	–	46/46	–
	IS, LSS	40/40	30/30	–	–	–	–	–	–	–	–	46/46	–
I_0	MSS	95/98	91/96	–	42/42	94/96	120/127	–	–	*	*	98/105*	–
	IS	95/98	91/96	72/78	–	–	–	–	–	*	*	98/105*	–
	LSS	95/98	91/96	72/78	–	–	–	–	49/53	*	*	98/105*	–
I_{4321}	MSS	96/100	91/96	–	42/43	94/97	118/123	–	–	*	*	98/104*	–
	IS	96/100	91/96	78/84	–	–	–	–	–	*	*	98/104*	–
	LSS	96/100	91/96	78/84	–	–	–	–	49/53	*	*	98/104*	–
I_{8765}	MSS	85/85	78/78	–	43/44	74/78	89/95	–	–	*	*	88/89*	–
	IS	85/85	78/78	62/62	–	–	–	–	–	*	*	88/89*	–
	LSS	85/85	78/78	62/62	–	–	–	–	50/50	*	*	88/89*	–
Clock	MSS	87/89	87/90	–	53/58	88/89	108/116	37/39	–	40/42	–	92/96	–
	IS, LSS	87/89	87/90	71/74	–	–	–	37/39	–	40/42	–	92/96	–
Z	MSS	Z is an Output											
	IS, LSS	73/76	66/70	54/54	–	–	–	–	–	–	–	79/79	–
$\overline{IEN}$	Any	–	–	–	–	–	–	–	22/24	–	–	–	–
SIO_3, SIO_0	Any	26/26	–	–	–	–	–	–	–	–	–	–	–

F = R + S + C_n if Z = 0
S − R − 1 + C_n if Z = 1

Z = $\overline{F_3} \oplus R_3$ (MSS) from previous cycle

Notes: 1. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an * is the delay to correct data on an enabled output. An * shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
2. A "–" means the delay path does not exist.
3. Data in boldface is different from standard function table; other data is the same.

CYCLE TIMES FOR 16-BIT SYSTEM FOR COMMON OPERATIONS

The illustration below shows a typical configuration using 4 Am2903 Superslices, an Am2902A carry lookahead chip, and the Am2904 for shift multiplexers, status registers, and carry-in control. For the system enclosed within the dashed lines, there are four major switching paths whose values for various kinds of cycles are summarized below, and shown on the timing waveform.

1. MICROCYCLE TIME (TCHCH).
   The minimum time which must elapse between a LOW-TO-HIGH clock transition and the next LOW-TO-HIGH clock transition.
2. DATA SET-UP TIME (TDVCH).
   The minimum time which must be allowed between valid, stable data on the D inputs and the clock LOW-TO-HIGH transition.
3. D TO Y (TDVYV).
   The maximum time required to obtain valid Y output data after the D inputs are valid. This is the combinational delay through the parts from D to Y.
4. CP TO Y (TCHYV).
   The maximum time required to obtain valid Y outputs after a clock LOW-TO-HIGH transition.

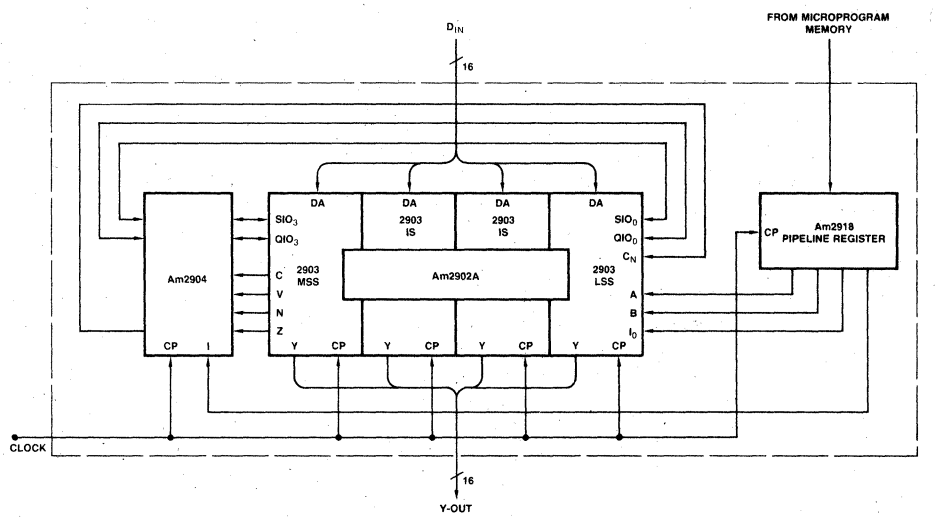
The types of cycles for which data is summarized are as follows:

1. Logic – Any logical operation without a shift.
2. Logic Rotate – Any logic operation with a rotate or shift.
3. Arithmetic – An add or subtract with no shift.
4. Multiply – The first cycle of a 2's complement multiply instruction. Subsequent cycles require less time.
5. Divide – The iterative divide cycle. The first divide instruction and the last divide (correction) instruction require less time.

Time in ns Over Commercial Operating Range

CYCLE	TCHCH	TDVCH	TDVYV	TCHYV
LOGIC	143	105	64	102
LOGIC ROTATE	180	143	123	160
ARITHMETIC	184	137	96	143
MULTIPLY	200	140	120	180
DIVIDE	228	167	128	189

16-Bit System with Am2903, Am2902A, Am2904



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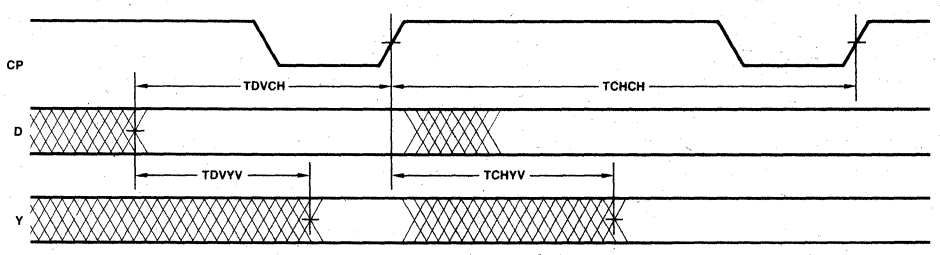
Timing Waveforms for Data In, Clock, and Y Out



MPR-584

USING THE Am2903

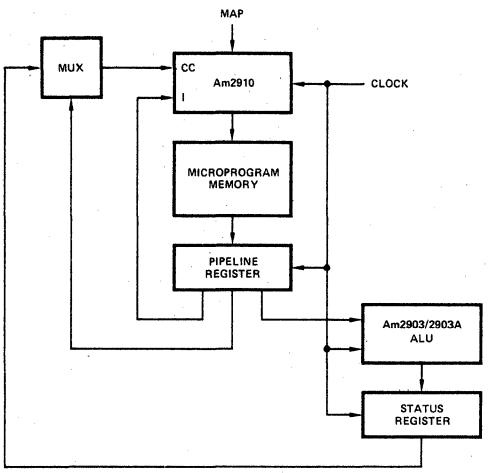
For additional applications information, see chapters III and IV of *Bit Slice Microprocessor Design,* Mick and Brick, McGraw-Hill Publishers.

Am2903 APPLICATIONS

The Am2903 is designed to be used in microprogrammed systems. Figure 1 illustrates a recommended architecture. The control and data inputs to the Am2903 normally will all come from registers clocked at the same time as the Am2903. The register inputs come from a ROM or PROM – the "microprogram store". This memory contains sequences of microinstructions which apply the proper control signals to the Am2903's and other circuits to execute the desired operation.

The address lines of the microprogram store are driven from the Am2910 Microprogram Sequencer. This device has facilities for storing an address, incrementing an address, jumping to any address, and linking subroutines. The Am2910 is controlled by some of the bits coming from the microprogram store. Essentially, these bits are the "next instruction" control.

Figure 1. Typical Microprogram Architecture.



One Level Pipeline Based System

MPR-035

Note that with the microprogram register in between the microprogram memory store and the Am2903's, a microinstruction accessed on one cycle is executed on the next cycle. As one microinstruction is executed, the next microinstruction is being read from microprogram memory. In this configuration, system speed is improved because the execution time in the Am2903's occurs in parallel with the access time of the microprogram store. Without the "pipeline register", these two functions must occur serially.

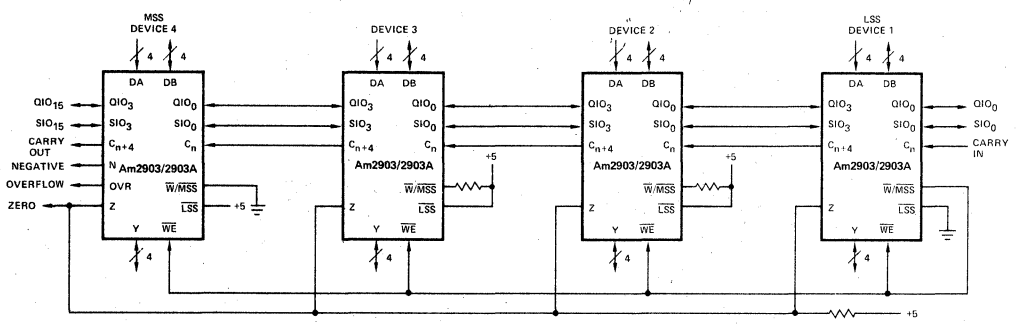
Expansion of the Am2903

The Am2903 is a four-bit CPU slice. Any number of Am2903's can be interconnected to form CPU's of 8, 16, 32, or more bits, in four-bit increments. Figure 2 illustrates the interconnection of four Am2903's to form a 16-bit CPU, using ripple carry.

With the exception of the carry interconnection, all expansion schemes are the same. The QIO_3 and SIO_3 pins are bidirectional left/right shift lines at the MSB of the device. For all devices except the most significant, these lines are connected to the QIO_0 and SIO_0 pins of the adjacent more significant device. These connections allow the Q Registers of all Am2903's to be shifted left or right as a contiguous n-bit register, and also allow the ALU output data to be shifted left or right as a contiguous n-bit word prior to storage in the RAM. At the LSB and MSB of the CPU, the shift pins should be connected to a shift multiplexer which can be controlled by the microcode to select the appropriate input signals to the shift inputs.

Device 1 has been defined as the least significant slice (LSS) and its $\overline{LSS}$ pin has accordingly been grounded. The Write/Most Significant Slice ($\overline{WRITE}/\overline{MSS}$) pin of device 1 is now defined as being the Write output, which may now be used to drive the write enable ($\overline{WE}$) signal common to the four devices. Devices 2 and 3 are designated as intermediate slices and hence the $\overline{LSS}$ and $\overline{WRITE}/\overline{MSS}$ pins are tied HIGH. Caution: $\overline{W}/\overline{MSS}$ must be tied to V_{CC} through a resistor; $\overline{W}/\overline{MSS}$ and $\overline{LSS}$ may not be shorted directly together. Device 4 is designated the most significant slice ($\overline{MSS}$) with the $\overline{LSS}$ pin tied HIGH and the $\overline{WRITE}/\overline{MSS}$ pin held LOW. The open collector, bidirectional Z pins are tied together for detecting zero or for inter-chip communication for some special instruction. The Carry-Out (C_{n+4}) is connected to the Carry-In (C_n) of the next chip in the case of ripple carry. For a faster carry scheme, an Am2902 may be employed (as shown in Figure 3) such that the $\overline{G}$ and $\overline{P}$ outputs of the Am2903 are connected to the appropriate $\overline{G}$ and $\overline{P}$ inputs of the Am2902, while the C_{n+x}, C_{n+y}, and C_{n+z} outputs of the Am2902 are connected to the C_n input of the appropriate Am2903. Note that $\overline{G}$/N and $\overline{P}$/OVR pin functions are device dependent. The most significant slice outputs N and OVR while all other slices output $\overline{G}$ and $\overline{P}$.

Figure 2. 16-Bit CPU with Ripple Carry.



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The $\overline{IEN}$ pin of the Am2903 allows the option of conditional instruction execution. If $\overline{IEN}$ is LOW, all internal clocking is enabled, allowing the latches, RAM, and Q Register to function. If $\overline{IEN}$ is HIGH, the RAM and Q Register are disabled. The RAM is controlled by $\overline{IEN}$ if $\overline{WE}$ is connected to the $\overline{WRITE}$ output.

It would be appropriate at this point to mention that the Am2903 may be microcoded to work in either two-or three-address architecture modes. The two-address modes allow A+B→B while the three-address mode makes possibleA+B→C. Implementation of a three-address architecture is made possible by varying the timing of $\overline{IEN}$ in relationship to the external clock and changing the B address as shown in Figure 4. This technique is discussed in more detail under Memory Expansion.

Parity

The Am2903 computes parity on a chosen word when the instruction bits I_{5-8} have the values of 4_{16} to 7_{16} as shown in Table 3. The computed parity is the result of the exclusive OR of the individual ALU outputs and SIO_3. Parity output is found on SIO_0. Parity between devices may be cascaded by the interconnection of the SIO_0 and SIO_3 ports of the devices as shown in Figure 3. The equation for the parity output at SIO_0 port of device 1 is given by $SIO_0 = F_{15} \forall F_{14} \forall F_{13} \forall \ldots \forall F_1 \forall F_0 \forall SIO_{15}$.

Figure 3. 16-Bit CPU with Carry Look Ahead.

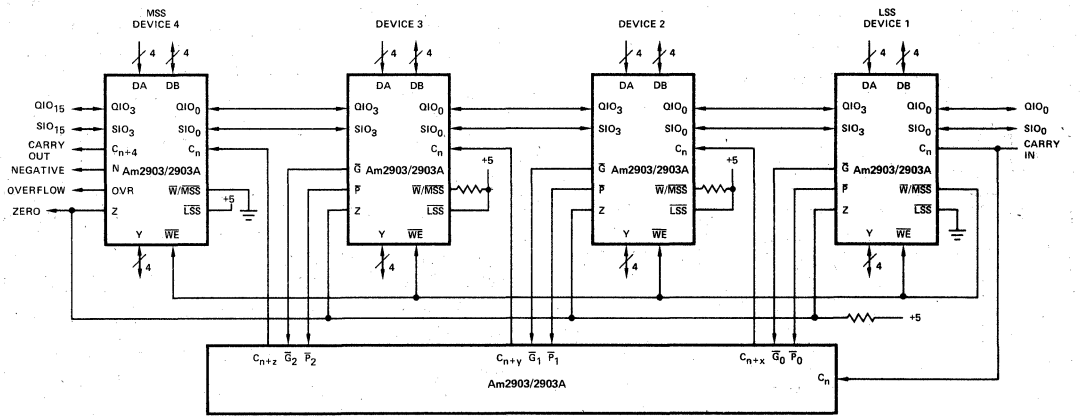

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Figure 4. Relationship of $\overline{IEN}$ and Clock During Two Address and Three Address Modes.

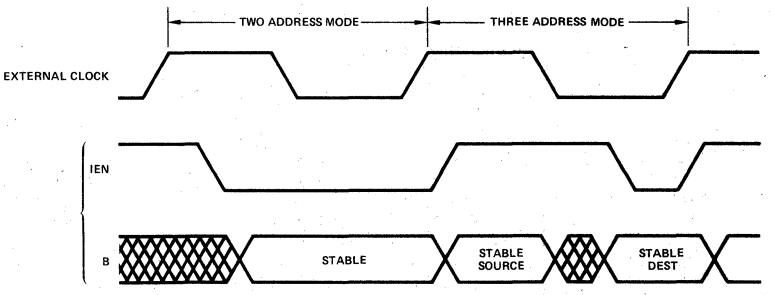

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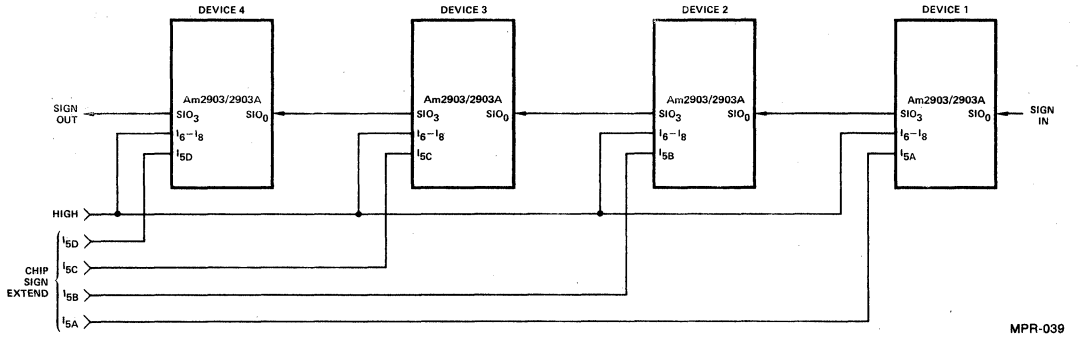
Figure 5. Sign Extend.



Sign Extend

Sign extension across any number of Am2903 devices can be done in one microcycle. Referring again to the table of instructions (Table 3), the sign extend instruction (Hex instruction E) on I_{5-8} causes the sign present at the SIO_0 port of a device to be extended across the device and appear at the SIO_3 port and at the Y outputs. If the least significant bit of the instruction (bit I_5) is HIGH, Hex instruction F is present on I_{5-8}, commanding a shifter pass instruction. At this time, F_3 of the ALU is present on the SIO_3 output pin. It is then possible to control the extension of the sign across chip boundaries by controlling the state of I_5 when I_{6-8} are HIGH. Figure 5 outlines the Am2903 in sign extend mode. With I_{6-8} held HIGH, the individual chip sign extend is controlled by I_{5A-D}. If, for example, I_{5A} and I_{5B} are HIGH while I_{5C} and I_{5D} are LOW, the signal present at the boundaries of devices 2 and 3 (F_3 of device 2) will be extended across devices 3 and 4 at the SIO_3 pin of device 4. The output of the four devices will be available at their respective Y data ports. The next positive edge of the clock will load the Y outputs into the address selected by the B port. Hence, the results of the sign extension is stored in the RAM.

SPECIAL FUNCTIONS

When $I_{0-4} = 0$, the Am2903 is in the Special Function mode. In this mode, both the source and destination are controlled by I_{5-8}. The Special Functions are in essence special microinstructions that are used to reduce the number of microcycles needed to execute certain functions in the Am2903.

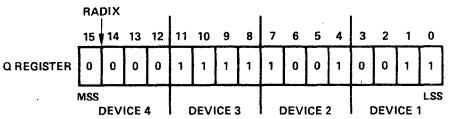
NORMALIZATION, SINGLE- AND DOUBLE-LENGTH

Normalization is used as a means of referencing a number to a fixed radix point. Normalization strips out all leading sign bits such that the two bits immediately adjacent to the radix point are of opposite polarity.

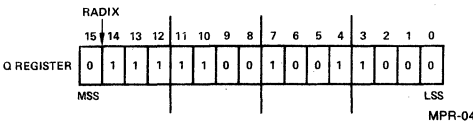
Normalization is commonly used in such operations as fixed-to-floating point conversion and division. The Am2903 provides for normalization by using the Single-Length and Double-Length Normalize commands. Figure 6a represents the Q Register of a 16-bit processor which contains a positive number. When the Single-Length Normalize command is applied, each positive edge of the clock will cause the bits to shift toward the most significant bit (bit 15) of the Q Register. Zeros are shifted in via the QIO_0 port. When the bits on either side of the radix point (bits 14 and 15) are of opposite value, the number is considered to be normalized as shown in Figure 6b. The event of normalization is externally indicated by a HIGH level on the C_{n+4} pin of the most significant slice (C_{n+4} MSS = Q_3 MSS $\forall$ Q_2 MSS).

Figure 6.

a) Unnormalized Positive Number.



b) Normalized Positive Number.



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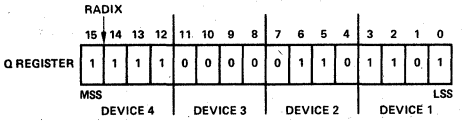
There are also provisions made for a normalization indication via the OVR pin one microcycle before the same indication is available on the C_{n+4} pin (OVR = Q_2 MSS $\forall$ Q_1 MSS). This is for use in applications that require a stage of register buffering of the normalization indication.

Since a number comprised of all zeros is not considered for normalization, the Am2903 indicates when such a condition arises. If the Q Register is zero and the Single-Length Normalization command is given, a HIGH level will be present on the Z line. The sign output, N, indicates the sign of the number stored in the Q register, Q_3 MSS. An unnormalized negative number (Figure 7a) is normalized in the same manner as a positive number. The results of single-length normalization are shown in Figure 7b. The device interconnection for single-length normalization is outlined in Figure 8. During single length normalization, the number of shifts performed to achieve normalization can be counted and stored in one of the working registers. This can be achieved by forcing a HIGH at the C_n input of the least significant slice, since during this special function the ALU performs the function [B] + C_n and the result is stored in B.

Normalizing a double-length word can be done with the Double-Length Normalize command which assumes that a user-selected RAM Register contains the most significant portion of the word to be normalized while the Q Register holds the least significant half (Figure 9). The device interconnection for double-length normalization is shown in Figure 10. The C_{n+4}, OVR, N, and Z outputs of the most significant slice perform the same functions in double-length normalization as they did in single-length normalization except that C_{n+4}, OVR, and N are derived from the output of the ALU of the most significant slice in the case of double-length normalization, instead of the Q Register of the most significant

Figure 7.

a) Unnormalized Negative Single Length Number.



b) Normalized Negative Single Length Number.

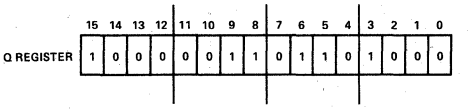


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Figure 8. Single Length Normalize.

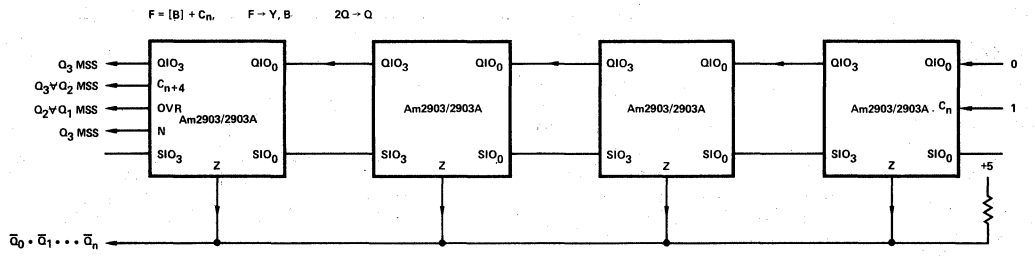

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Figure 9. Double Length Word.

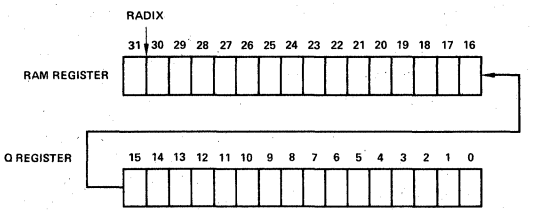

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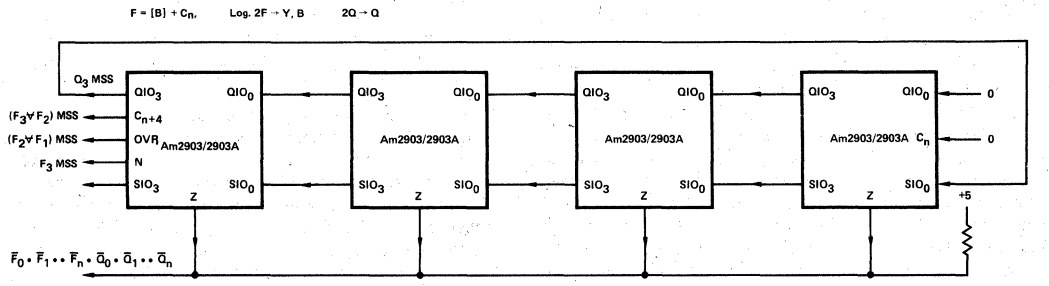
Figure 10. Double Length Normalize.



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slice as in single-length normalization. A high-level Z line in double-length normalization reveals that the outputs of the ALU and Q Register are both zero, hence indicating that the double-length word is zero.

When double-length normalization is being performed, shift counting is done either with an extra microcycle or with an external counter.

SIGN MAGNITUDE, TWO'S COMPLEMENT CONVERSION

As part of the special instruction set, the Am2903 can convert between two's complement and sign/magnitude representations. Figure 11 illustrates the interconnection needed for sign magnitude/two's complement conversion. The word to be converted is applied to the S input port of the ALU (from the RAM B port or the DB I/O port). The C_n input of device 1 is connected to the Z pin. The sign bit (S_3MSS) is brought out on the Z line and informs the other ALU's if the conversion is being performed on a negative or positive number. If the number to be converted is the most negative number in two's complement [i.e., 100 . . . 00 (-2^n)], an overflow indication will occur. This is because -2^n is one greater than any number that can be represented in sign magnitude notation and hence an attempted conversion to sign magnitude from -2^n will cause an overflow. When minus zero in sign magnitude notation (100 . . . 0) is converted to two's complement notation, the correct result is obtained (0 . . .0).

INCREMENT BY ONE OR TWO

Incrementation by One or Two is made possible by the Special Function of the same name. This command is quite useful in the case of byte addressable words. Referencing Figure 12, a word may be incremented by one if C_n is LOW or incremented by two if C_n is HIGH.

UNSIGNED MULTIPLY

This Special Function allows for easy implementation of unsigned multiplication. Figure 13 is the unsigned multiply flow chart. The algorithm requires that initially the RAM word addressed by Address port B be zero, that the multiplier be in the Q Register, and that the multiplicand be in the register addressed by Address port A. The initial conditions for the execution of the algorithm are that: 1) register R_0 be reset to zero; 2) the multiplicand be in R_1; and 3) the multiplier be in R_2. The first operation transfers the multiplier, R_2, to the Q Register. The Unsigned Multiply instruction is then executed 16 times. During the Unsigned Multiply instruction, R_0 is addressed by RAM address port B and the multiplicand is addressed by RAM address port A.

When the unsigned Multiply command is given, the Z pin of device 1 becomes an output while the Z pins of the remaining devices are specified as inputs as shown in Figure 15. The Z output of device 1 is the same state as the least significant bit of the multiplier in the Q Register. The Z output of device 1 informs the ALU's of all the slices, via their Z pins, to add the partial product (referenced by the B address port) to the mul-

Figure 11. 2's Complement ⟷ Sign/Magnitude.

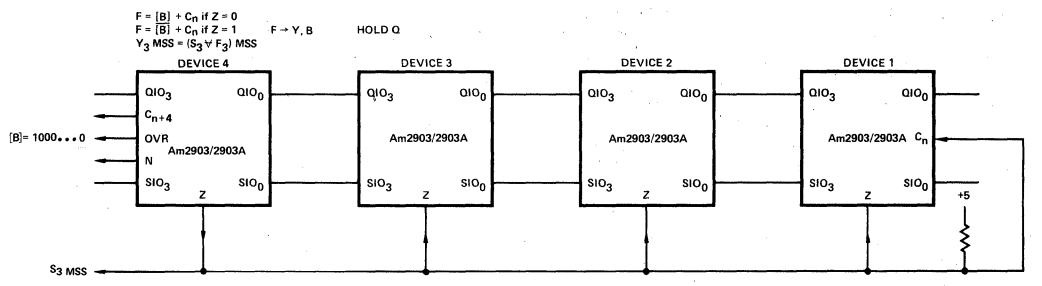

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Figure 12. Increment by 2/1.

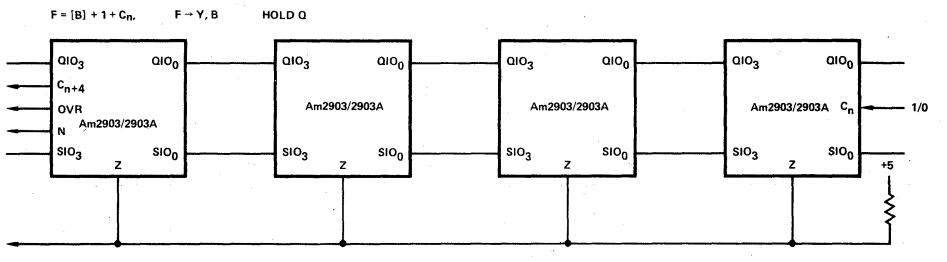

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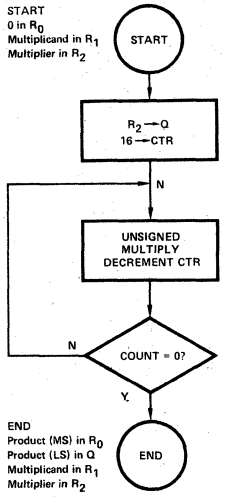
Figure 13. Unsigned 16 X 16 Multiply Flowchart.



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tiplicand (referenced by the A address port) if Z = 1. If Z = 0, the output of the ALU is simply the partial product (referenced by the B address port). Since C_n is held LOW, it is not a factor in the computation. Each positive-going edge of the clock will internally shift the ALU outputs toward the least significant bit and simultaneously store the shifted results in the register selected by the B address port, thus becoming the new partial sum. During the down shifting process, the C_{n+4} generated in device 4 is internally shifted into the Y_3 position of device 4. At this time, one bit of the multiplier will down shift out of the QIO_0 ports of each device into the QIO_3 port of the next less significant slice. The partial product is shifted down between chips in a like manner, between the SIO_0 and SIO_3 ports, with SIO_0 of device 1 being connected to QIO_3 of device 4 for purposes of constructing a 32-bit long register to hold the 32-bit product. At the finish of the 16 x 16 multiply, the most significant 16 bits of the product will be found in the register referenced by the B address lines while the least significant 16 bits are stored in the Q Register. Using a typical Computer Control Unit (CCU), as shown in Figure 16, the unsigned multiply operation requires only two lines of microcode, as shown in Figure 17, and is executed in 17 microcycles.

TWO'S COMPLEMENT MULTIPLICATION

The algorithm for two's complement multiplication is illustrated by Figure 14. The initial conditions for two's complement multiplication are the same as for the unsigned multiply operation. The Two's Complement Multiply Command is applied for 15 clock cycles in the case of a 16 x 16 multiply. During the down shifting process the term $N \forall OVR$ generated in device 4 is internally shifted into the Y_3 position of device 4. The data flow shown in Figure 15 is still valid. After 15 cycles, the sign bit of the multiplier is present at the Z output of device 1. At this time, the user must place the Two's Complement Multiply Last cycle command on the instruction lines. The interconnection for this instruction is shown in Figure 18. On the next positive edge of the clock, the Am2903 will adjust the partial product, if the sign of the multiplier is negative, by subtracting out the two's complement representation of the multiplicand. If the sign bit is positive, the partial product is not adjusted. At this point, two's complement multiplication is completed. Using a typical CCU, as shown in Figure 16, the two's complement multiply operation requires only three lines of microcode, as shown in Figure 19, and is executed in 17 microcycles.

Figure 14. 2's Complement 16 X 16 Multiply.

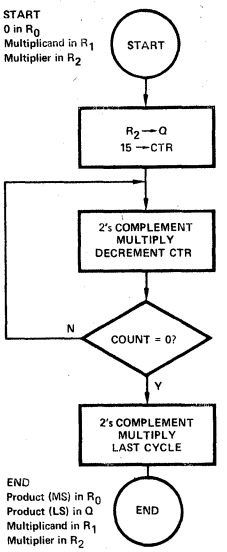

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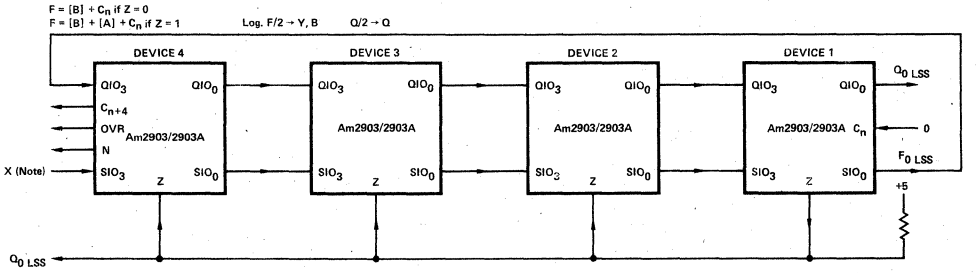
Figure 15. Multiply.



Note: For unsigned multiply, C_{n+4} MSS is internally shifted into position Y_3 MSS; 2's complement multiply $N \forall OVR$ is internally shifted into position Y_3 MSS.

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Figure 16. Typical Computer Control Unit (CCU).

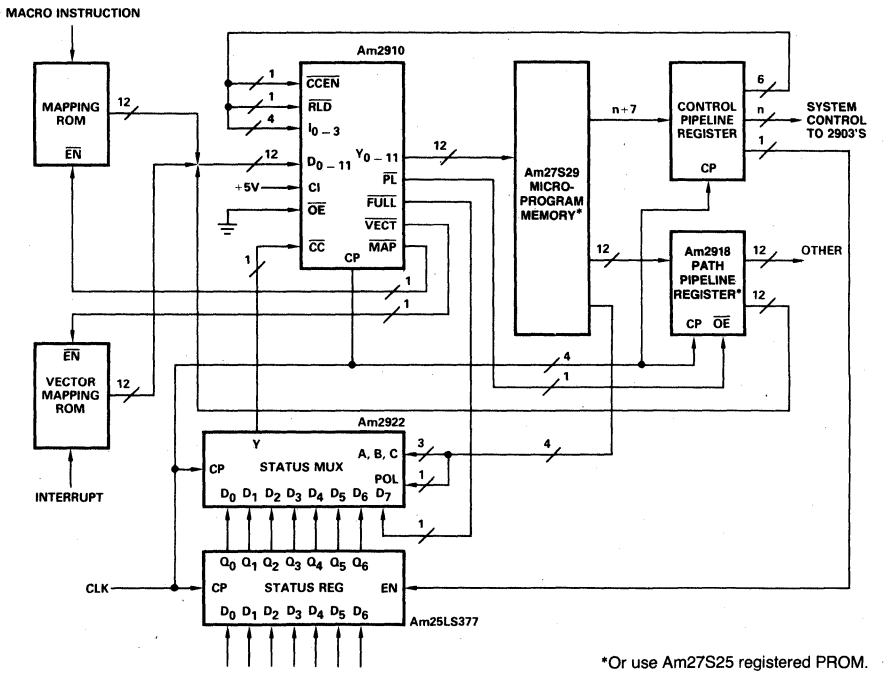

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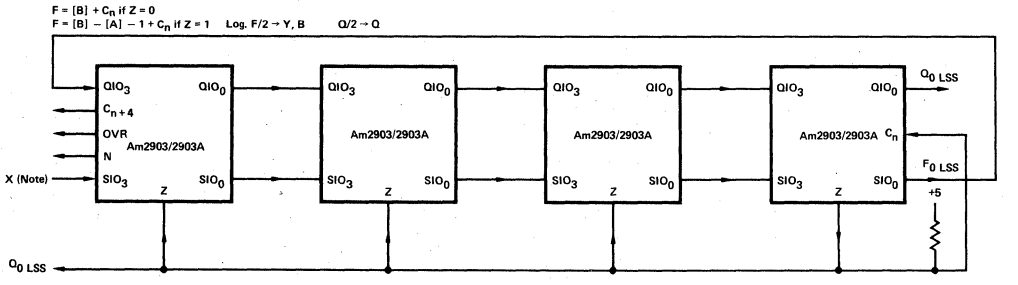
Figure 17. Micro Code for Unsigned 16 X 16 Multiply.

Micro Memory Address	Am2910 Inst	Data Pipeline Reg.	I_0	I_4-I_1	I_8-I_5	$\overline{OEB}$	$\overline{OEY}$	A_3-A_0	B_3-B_0	C_n	Comment
n	LDCT	$00F_{16}$	H	6	6	X	X	R_2	X	0	Load Counter & $R_2 \rightarrow Q$
n+1	RPCT	n+1	0	0	0	0	0	R_1	R_0	0	Unsigned Multiply

Figure 18. 2's Complement Multiply, Last Cycle.



Note: N ∀ OVR is internally shifted into position Y_3 MSS.

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Figure 19. Microcode for 2's Complement 16 x 16 Multiply.

Memory Address	Am2910 Inst	Data Pipeline Reg.	I_0	$I_4 - I_1$	$I_8 - I_5$	$\overline{OEB}$	$\overline{OEY}$	$A_3 - A_0$	$B_3 - B_0$	C_n	Comment
n	LDCT	$00E_{16}$	X	6	6	X	X	R_2	X	0	Load Counter & $R_2 \rightarrow Q$
n+1	RPCT	n+1	0	0	2	0	0	R_1	R_0	0	2's Complement Multiply
n+2	X	X	0	0	6	0	0	R_1	R_0	Z	2's Complement Multiply (Last Cycle)

TWO'S COMPLEMENT DIVISION

Three instructions on the Am2903/203 can be used to microcode signed integer division. The algorithm is a non-restoring four-quadrant division, with different preamble and postamble microcode for single- and double-precision integer division.

Single-precision signed integer divide is the most straightforward. Other than division by zero, there is only one case when an overflow results, namely when the most negative number (-2^{n-1}) is divided by -1. This case is detected by the postamble, and does not require separate tests of dividend and divisor in the preamble.

Single-precision signed integer divide is the most straightforward. Other than division by zero, there is only one case when an overflow results, namely when the most negative number (-2^{n-1}) is divided by -1. This case is detected by the postamble, and does not require separate tests of dividend and divisor in the preamble.

Single-precision division begins by loading the Q Register with the dividend. Following this, the negative bit of the status register is tested and the dividend register is loaded with all ones or all zeros so as to sign extend the Q Register. The dividend is now a double-precision integer, with the least significant half in the Q Register and the most significant half in the dividend register. This double-precision integer is then shifted up one position in preparation for the divide.

The division starts with the First Divide Operation applied to the divisor register (A address) and the dividend register (B address). This operation computes the quotient sign as the exclusive OR of dividend and divisor sign, and shifts it into the least significant position of the Q Register while simultaneously upshifting the double-precision dividend one bit. The First Divide Operation also updates the Sign Compare Flip-Flop (in the MSS) with the exclusive NOR of the dividend and divisor sign, which determines whether the next operation will be an add or a subtract.

The stage is now set for repeated execution of the divide step. Provided correct shift linkages externally (SIO_3 on the MSS to QIO_0 on the LSS, and QIO_3 on MSS to SIO_0 on the LSS), each execution of the divide step computes a new quotient bit by either adding the divisor to the dividend (if the sign compare flip-flop is HIGH) or subtracting the divisor from the dividend (if the sign compare flip-flop is LOW), and then producing the exclusive NOR of the sign of the result and the divisor sign as the new quotient bit and the new value of the sign compare flip-flop. The upshifted result replaces the partial remainder in the dividend register. The divide step must be repeated $n-2$ times for n bit signed integers. Note that the sign compare flip-flop resides on the most significant slice, and controls the other slices through the zero pin which becomes an input on the intermediate and least significant slices for this operation.

The divide correction step also adds or subtracts the divisor from the partial remainder in the dividend register, but does not upshift the result. The quotient bit shifted into the Q Register by this step is always a 1. This means that the quotient produced by the divide algorithm is always odd; in half the cases, of course, this guess is wrong, and must be corrected. At each step of the divide algorithm, the result of the previous guess is corrected and a new guess is made. Since correction lags computation of the quotient bits by one step, after the last step there is still one correction needed.

After the divide correction step, the product of quotient and divisor plus the remainder is guaranteed to be equal to the dividend. However, the magnitude of the quotient may be off by one, the sign of the remainder may be wrong, and the magnitude of the remainder may lie between the magnitude of the divisor and zero.

In general, correction is needed when the sign of the remainder and initial dividend differ. For positive quotients, the correction is performed by subtracting one from the quotient and adding the divisor back to the remainder. For negative quotients, the correction is performed by adding one to the quotient and subtracting the divisor from the remainder.

A special case arises when the dividend is negative and the remainder at the end of the division is exactly zero. Since zero appears to be positive in two's complement, it appears that correction is necessary, whereas in fact it is not. This case is easily detected by testing the remainder for zero after the last divide step, and terminating the algorithm if it is. A related problem arises with negative dividends when the partial remainder becomes exactly zero in an intermediate step of the division. Once again, the algorithm sees this as a change of sign, and records the wrong quotient bit. However, in such cases, the final remainder always has the same magnitude as the divisor, but has the same sign as the dividend. Since the multiplicative rule is still satisfied, this means that the quotient is too small in magnitude by one. This case is detected by adding the magnitude of the divisor to the remainder and testing for zero, and the correction is the opposite of the "normal" correction: positive quotients are incremented, and negative quotients are decremented. (The remainder should be made exactly zero). Note that the single case that produces overflow for single-precision signed integer divide may be detected by checking the overflow in this correction step.

The complete algorithm is shown in Figure 20. It is important to remember that the zero status available at the end of the divide correction step is the sign compare flip-flop output, and does not reflect whether the final partial remainder is zero or not. Also, in interruptible systems, the division steps must not be interrupted, because the sign compare flip-flop cannot be saved or restored on the interrupt. However, division *can* be stopped and resumed provided no instruction in between affects the state of the sign compare flip-flop. Some examples of the correction for single-precision signed divide are shown in Figure 21.

The shift linkage requirements for the divide steps are summarized in Figures 22, 23 and 24. These figures should be used as guidelines when microcoding the fields controlling the shift multiplexers in the 2904 for the divide steps.

Except for the overflow problem, the same algorithm with minor variations in the preamble implements double-precision division. Of course, in this case, sign extension is not needed; instead, the least significant half of the double-precision dividend is loaded in the Q Register, the most significant half remains in the "dividend" registers, and, after the initial upshift by one bit, the divide steps are executed exactly as before.

When a double-precision signed integer is divided by a single-precision signed integer, overflow occurs when the quotient requires more than n bits to represent. For example 2^{2n-2} divided by 1 requires 2n bits to represent. A subset of these cases of overflow is the case where the *magnitude* of the quotient requires exactly n bits to represent, leaving no bits for the sign; and a special case of this is where the quotient magnitude is 2^{n-1}. The preamble to the divide presented below detects the first two cases in that order, and the postamble detects the last case.

The principle of overflow detection used here is to first calculate the quotient sign, and then calculate n+1 bits of quotient. There is an overflow when bits n+1 and n differ from the sign. This detects cases where the quotient requires more than n+1 bits to represent (quotient bit n+1 differs from the quotient sign), and where the quotient requires exactly n+1 bits to represent (quotient bit n+1 is the same as the quotient sign but quotient bit n differs from the quotient sign). Unfortunately quotients with a magnitude of 2^{n-1} do not fit this scheme: when the quotient is -2^{n-1}, this test indicates an overflow, and when the quotient is 2^{n-1} (an overflow), this test does not show an overflow. In other words, when there is a disagreement between the n^{th} quotient bit and the quotient sign, it does not necessarily indicate an overflow; and it is not until all the quotient bits are calculated that it can be decided whether there was an overflow or not. This irregularity is a consequence of the asymmetry of the two's complement number system.

The implementation of this algorithm on the Am2903/203 is simplified by using a flip-flop on the SIO_3 line out of the MSS to store a copy of the new quotient bit calculated each cycle. If this flip-flop output is connected to a sequencer test multiplexer input, then testing of quotient bits can be pipelined. This is useful in the preamble for overflow detection and in the postamble for the correction steps.

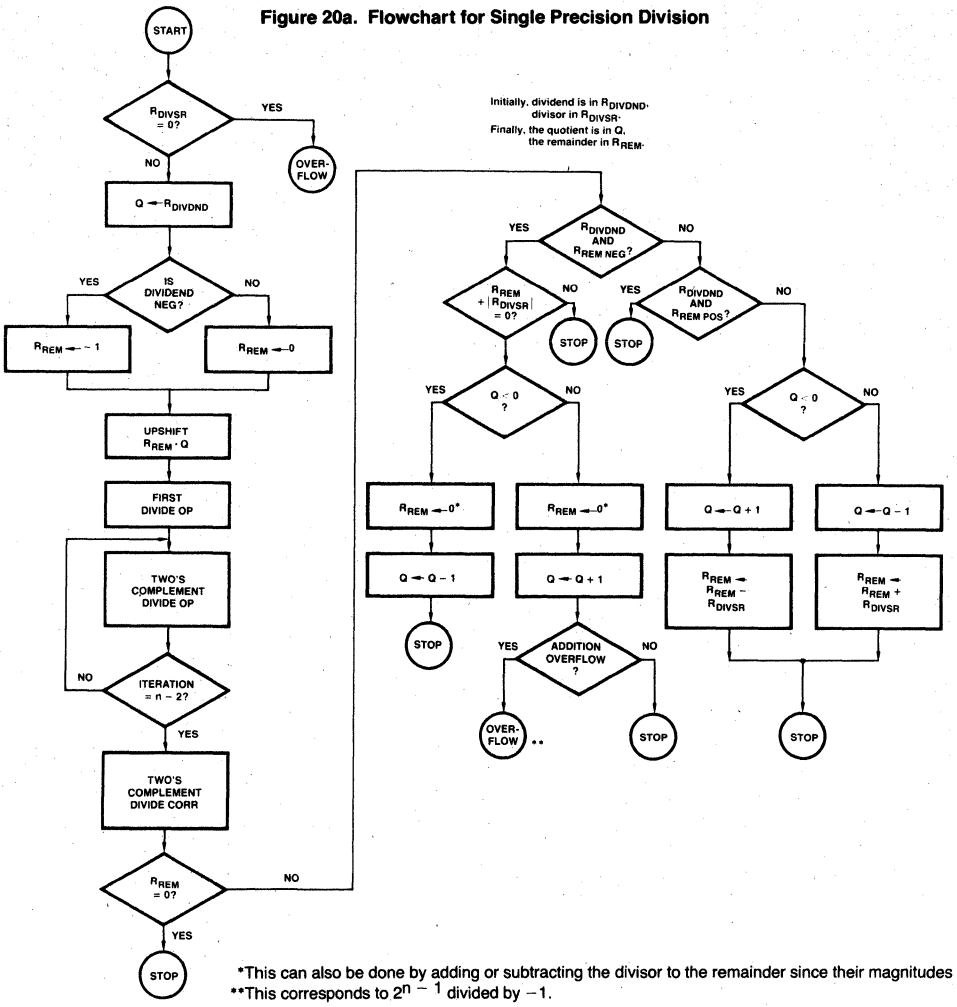
The microcode for the double-precision divide is outlined in Figure 25. The divide operation is first applied to the dividend and divisor without the initial upshift of the dividend. This calculates the quotient sign and updates the sign compare flip-flop. At the end of the cycle, the complement of the quotient sign is setup at the input to the external flip-flop, which can be tested in the next cycle to determine the quotient sign. However, the divide first operation has the side-effect of upshifting the dividend. This side-effect is undesirable because it prevents the divide step from calculating the $n+1^{th}$ quotient bit. For this reason, the dividend is shifted down again with the sign bit of the status register selected as the linkage in. Following this, a divide step is executed and the algorithm terminated on overflow if the quotient bit calculated by the divide steps is different from the sign bit. The algorithm proceeds to calculate the n^{th} quotient bit. If the n^{th} quotient bit agrees with the quotient sign, there still may be an overflow if the quotient turns out to be 2^{n-1}; and if the nth quotient bit disagrees with the quotient sign, there still may not be an overflow if the quotient turns out to be -2^{n-1}. So at this stage the algorithm cannot decide whether there is an overflow or not based on the quotient bit; instead, it proceeds to calculate the remaining quotient bits, retaining the information about potential overflow in the control flow.

After the last divide step (the so-called "divide correction"), the algorithm again tests the state of the external flip-flop, "storing" it in the control flow. This last state of the divide flip-flop would be lost without the external flip-flop, since the quotient bit shifted in is always a I in this case, and the internal divide flip-flop is not updated. (The state of the external flip-flop after this cycle determines whether the correction requires incrementing or decrementing of the quotient). Concurrently with the testing of the external flip-flop, the microcode also passes the remainder through the ALU to update the Z bit of the status register. In the next cycle, the Z bit is tested and the algorithm terminates if it is set. This is followed by a test for negative remainder and dividend. If the test fails, a branch is taken to the test for positive dividend and remainder. Concurrently, the remainder is added to the divisor with $\overline{IEN}$ high and the Z flag again updated. This is the first part of the test for the absolute value of the remainder being equal to the divisor. In the next cycle, the Z flag is tested; if it is set, a branch is taken to the correction step. Again, in the same cycle, the remainder is subtracted from the divisor with $\overline{IEN}$ high to complete the magnitude test.

In the following cycle, the Z flag is tested as before. If it is not set, the algorithm terminates. The test for positive dividend and remainder computes the OR of the remainder and initial dividend with $\overline{IEN}$ high, and updates the N flag of the status register. In the next cycle the algorithm tests the N flag and exits if it is low, indicating that the dividend and remainder signs agreed. Otherwise, the correction steps are executed.

The algorithm has been written for fastest execution, not shortest possible microcode. The technique of using the control flow to "remember" states of flags leads to duplication of code but saves cycles on testing flags and branching. At the end of the algorithm, there are two places where the quotient is incremented. One of these sequences corresponds to the "normal" case (quotient bit n agreed with quotient sign). This microcycle produces an overflow when the quotient is 2^{n-1}. The other sequence where the quotient is incremented corresponds to the case where the n^{th} bit of quotient disagreed with the quotient sign. This case is an overflow unless the quotient is $-2^n - 1$; however, then an overflow is produced by the correction, when $2^n - 1 - 1$ is incremented. Hence, in this case, if the correction does *not* produce an overflow, then there *is* an overflow.

Figure 20a. Flowchart for Single Precision Division



*This can also be done by adding or subtracting the divisor to the remainder since their magnitudes are equal.
**This corresponds to $2^n - 1$ divided by −1.

Figure 20b. Single-Precision Divide Microcode

	1. Y ← R_{DIVSR}, UPDATE Z FLAG;	Test for divisor = 0
	2. IF Z GOTO OVERFLOW, Q ← R_{DIVDND}, UPDATE N;	Test quotient sign for sign extension
	3. IF NOT N GOTO UPSH, R_{REM} ← 0;	zero extend into R_{REM}
	4. R_{REM} ← −1;	One extend if negative
UPSH:	5. UPSHIFT R_{REM} Q;	Logic upshift R_{REM} and Q, zero fill
	6. FOR (n − 3), FIRST DIVIDE OP (R_{REM}, R_{DIVSR});	Loop setup: load 2910 counter and push PC
	7. ENDFOR, TWO'S COMPLEMENT DIVIDE OP (R_{REM}, R_{DIVSR});	R_{REM} on B address; repeat n − 2 times
	8. DIVIDE "CORRECTION" OP (R_{REM}, R_{DIVSR});	Shift in '1' into Q_0 of LSS
	9. Y ← R_{REM}, UPDATE Z, V;	Test remainder for zero
	10. IF Z GOTO DONE, Y ← R_{REM} AND R_{DIVDND}, UPDATE N;	Done if remainder = 0, check for dividend
	11. IF NOT N GOTO NORMCHK, Y ← R_{DIVSR} − R_{REM}, UPDATE Z;	and remainder being negative
	12. IF Z GOTO EQMAG, Y ← R_{DIVSR} + R_{REM}, UPDATE Z;	First half of magnitude check
	13. IF Z GOTO EQMAGNXT, Y ← Q, UPDATE N;	Other half of magnitude check
DONE:	14. IF NOT V RETURN, R_{QUOT} ← Q;	If magnitude equal, then go test
	15. GOTO OVERFLOW;	sign of Q else return
NORMCHK:	16. Y ← R_{REM} OR R_{DIVDND}, UPDATE N;	Check if remainder and dividend positive
	17. IF NOT N GOTO DONE, Y ← Q, UPDATE N;	If yes, exit
	18. IF N GOTO ADDONE;	Increment negative quotients
SUBONE:	19. R_{REM} ← R_{REM} + R_{DIVSR};	
	20. Q ← Q − 1, UPDATE V, GOTO DONE;	This can never overflow since Q is odd
EQMAG:	21. Y ← Q, UPDATE N;	
EQMAGNXT:	22. IF N GOTO SUBONE;	Decrement negative quotients
ADDONE:	23. R_{REM} ← R_{REM} − R_{DIVSR};	
	24. Q ← Q + 1, UPDATE V, GOTO DONE;	This could overflow for positive Q
OVERFLOW:	25. (. . . . OVERFLOW MICROCODE)	

Note: Where Y is specified as destination, use IEN = HIGH.

Figure 21. Examples of Single-Precision Signed Divide

Operation	Before Correction		After Correction		Comments
	Q	REM	Q	REM	
12 ÷ 5	3	−3	2	2	Normal correction: decrement positive quotients, increment negative quotients
12 ÷ −5	−3	−3	−2	2	
−12 ÷ 5	−3	3	−2	−2	
−12 ÷ −5	3	3	2	−2	
12 ÷ 4	3	0	3	0	No correction necessary: zero remainder
12 ÷ −4	−3	0	−3	0	
−12 ÷ 4	−3	0	−3	0	
−12 ÷ −4	3	0	3	0	
12 ÷ 3	5	−3	4	0	Normal correction
12 ÷ −3	−5	−3	−4	0	
−12 ÷ 3	−3	−3	−4	0	Special case: increment positive quotients
−12 ÷ −3	3	−3	4	0	
−32768 ÷ −1	32767	−1	−32768	0	Overflow!
−32768 ÷ 1	−32767	−1	−32768	0	Special case

Figure 22. Double Length Normalize/First Divide Operation

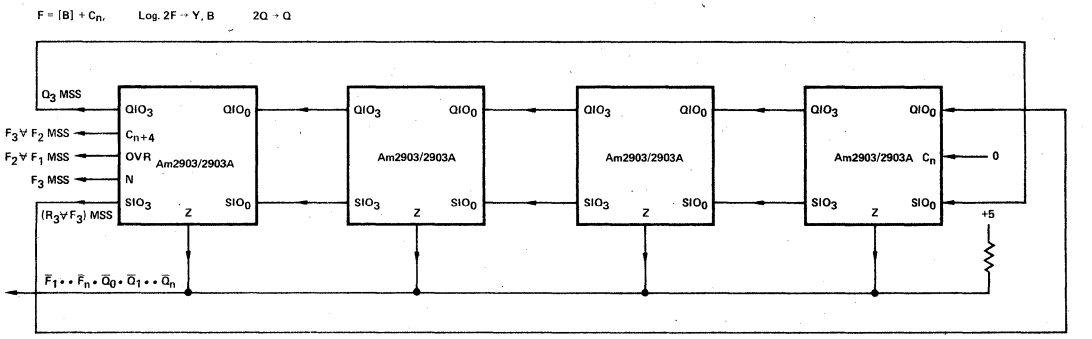


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Figure 23. Two's Complement Divide

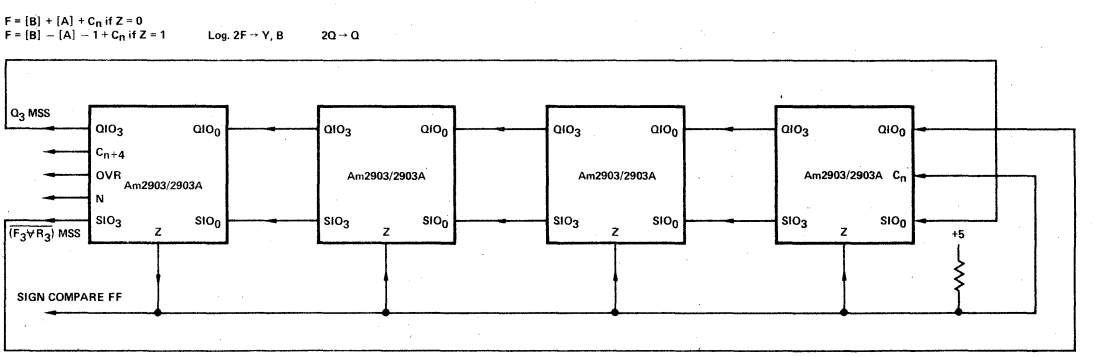

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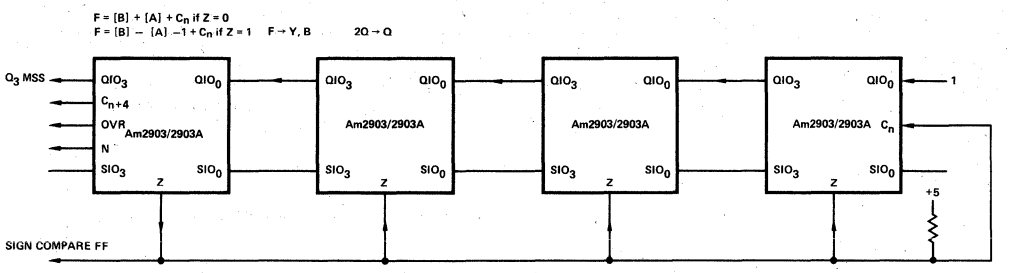
Figure 24. Two's Complement Divide Correction



MPR-055

Figure 25. Double-Precision Signed Division Microcode

	1. Q ← $R_{DIVDNDLSH}$;	Initialize Q Register
	2. R_{REM} ← $R_{DIVDNDMSH}$;	Initialize remainder register R_{REM}
	3. DIVIDE FIRST OP (R_{REM}, R_{DIVSR}), UPDATE N;	Find quotient sign, setup external quotient flip-flop (EXTQFF)
	4. IF EXTQFF GOTO NEGQUOT, DOWNSH R_{REM} • Q WITH N FILL;	Branch on quotient sign; restore dividend by downshift
	5. TWO'S COMPLEMENT DIVIDE OP (R_{REM}, R_{DIVSR});	Compute bit n+1 of quotient
	6. IF EXTQFF GOTO OVERFLOW, TWO'S COMPLEMENT DIVIDE OP (R_{REM}, R_{DIVSR});	Error if different from sign; compute bit n of quotient
	7. IF EXTQFF GOTO POSSBLOVF, TWO'S COMPLEMENT DIVIDE OP (R_{REM}, R_{DIVSR});	Possible overflow if different from sign
LOOP:	8. FOR (n−5), TWO'S COMPLEMENT DIVIDE OP (R_{REM}, R_{DIVSR});	Iterate setup
	9. ENDFOR, TWO'S COMPLEMENT DIVIDE OP (R_{REM}, R_{DIVSR});	Iterate divide step
	10. DIVIDE "CORRECTION" STEP (R_{REM}, R_{DIVSR});	Divide last step: quotient bit is always a '1'; setup EXTQFF
	11. IF EXTQFF GOTO SUB, Y ← R_{REM}, UPDATE Z;	Last state of EXTQFF decides direction of connection
	12. IF Z GOTO DONE, Y ← R_{REM} AND $R_{DIVDNDMSH}$, UPDATE Z, V;	Exit if remainder zero; test for negative remainder and dividend
	13. IF NOT N GOTO NORMCHK1, Y ← R_{REM} + R_{DIVSR}, UPDATE Z;	If test failed, go check for positive remainder and dividend
	14. IF Z GOTO CORRECT1, Y ← R_{REM} − R_{DIVSR}, UPDATE Z;	For negative remainder and dividend, check remainder magnitude
	15. IF Z GOTO CORRECT1;	If remainder magnitude = divisor magnitude, connect quotient
DONE:	16. IF NOT V RETURN, R_{QUOT} ← Q;	Else if no overflow return
	17. GOTO OVERFLOW;	Else overflow
NORMCHK1:	18. Y ← R_{REM} OR $R_{DIVDNDMSH}$, UPDATE N, V;	Check for positive dividend and remainder
	19. IF NOT N GOTO DONE;	If test passed, done
CORRECT1:	20. R_{REM} ← R_{REM} + R_{DIVSR};	Else correct remainder
	21. Q ← Q − 1, GOTO DONE;	Correct quotient, and exit
SUB:	22. IF Z GOTO DONE, Y ← R_{REM} AND $R_{DIVDNDMSH}$, UPDATE Z, V;	This part of the algorithm repeats the correction code for the case where the last value of the EXTQFF was a high, indicating correction in the opposite direction.
	23. IF NOT N GOTO NORMCHK2, Y ← R_{REM} + R_{DIVSR}, UPDATE Z;	
	24. IF Z GOTO CORRECT2, Y ← R_{REM} − R_{DIVSR}, UPDATE Z;	
	25. IF Z GOTO CORRECT2;	
	26. GOTO DONE;	
NORMCHK2:	27. Y ← R_{REM} OR $R_{DIVDNDMSH}$, UPDATE N, V;	
	28. IF NOT N GOTO DONE;	
	29. R_{REM} ← R_{REM} − R_{DIVSR};	
	30. Q ← Q + 1, UPDATE V;	
	31. GOTO DONE;	
NEGQUOT:	32. TWO'S COMPLEMENT DIVIDE OP (R_{REM}, R_{DIVSR});	Executed instead of 5, 6, 7 when the quotient is negative
	33. IF NOT EXTQFF GOTO OVERFLOW, TWO'S COMPLEMENT DIVIDE OP (R_{REM}, R_{DIVSR});	
	34. IF EXTQFF GOTO LOOP, TWO'S COMPLEMENT DIVIDE OP (R_{REM}, R_{DIVSR});	
POSSBLOVF:	35. FOR (n−5), TWO'S COMPLEMENT DIVIDE OP (R_{REM}, R_{DIVSR});	This is executed when the n^{th} quotient bit differs from the quotient sign. The division is completed to check whether the quotient is -2^{n-1}.
	36. ENDFOR, TWO'S COMPLEMENT DIVIDE OP (R_{REM}, R_{DIVSR});	
	37. DIVIDE "CORRECTION" STEP (R_{REM}, R_{DIVSR});	
	38. IF NOT EXTQFF GOTO OVERFLOW, R_{REM} ← 0;	This is signalled by an overflow in the correction step. Otherwise, there has been a division overflow.
	39. Q ← Q + 1, UPDATE V;	
	40. IF V GOTO DONE;	
	41. GOTO OVERFLOW;	

BYTE SWAP

The multi-port architecture of the Am2903 allows for easy implementation of high- and low-order byte swapping. Figure 26 outlines a byte swap implementation utilizing two data ports. Initially, the lower order 8-bit byte is stored in devices 1 and 2, while the high-order byte is in devices 3 and 4. When the user wishes to exchange the two bytes, the register location of the desired word is placed on the B address port. When the byte swap line is brought LOW, the bytes to be swapped will be flowing from the DB ports of the Am2903 through the Am2958/2959 Three-state Buffers. The outputs of the three-state buffers are permuted such that the byte swap is achieved.

The resultant permuted data is presented to the DA ports of the Am2903 where it is re-loaded into the memories of the Am2903 on the next positive edge of CP using the source and function commands of F = A plus C_n (C_n = 0) for the Am2958 or F = A plus C_n (C_n = 0) for the Am2959 and the destination command F Y, B.

A higher speed technique for achieving the byte swap operation is illustrated in Figure 27. Instead of inputting the permuted data via the DA ports, the permuted data is entered via the Y input/output ports with $\overline{OE_Y}$ held HIGH. This technique bypasses the ALU, thus allowing faster operation. The Am2903 destination command F → Y, B should be used.

Figure 26. Byte Swap.

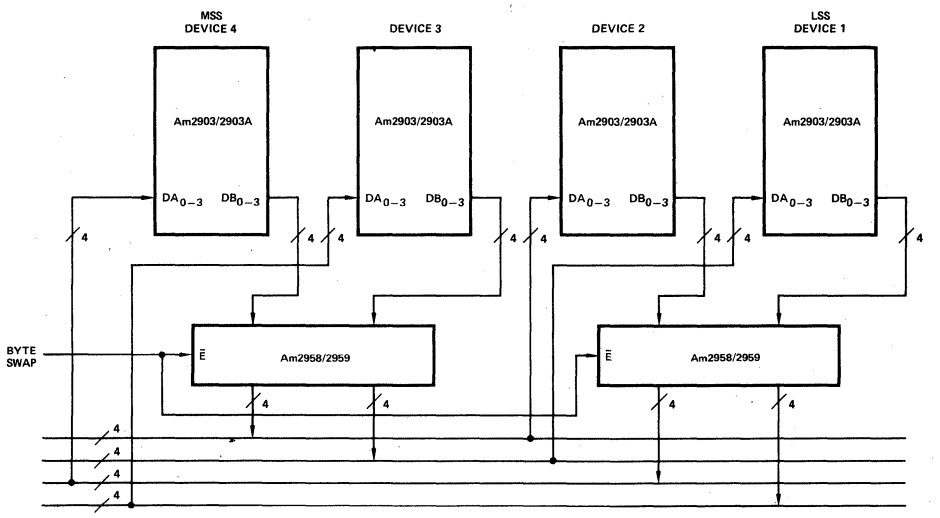


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Figure 27. High Speed Byte Swap.

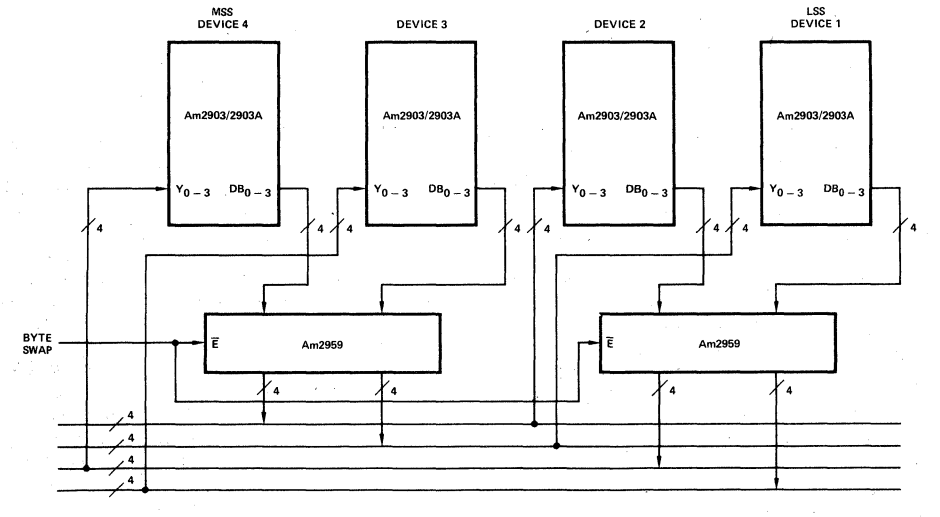

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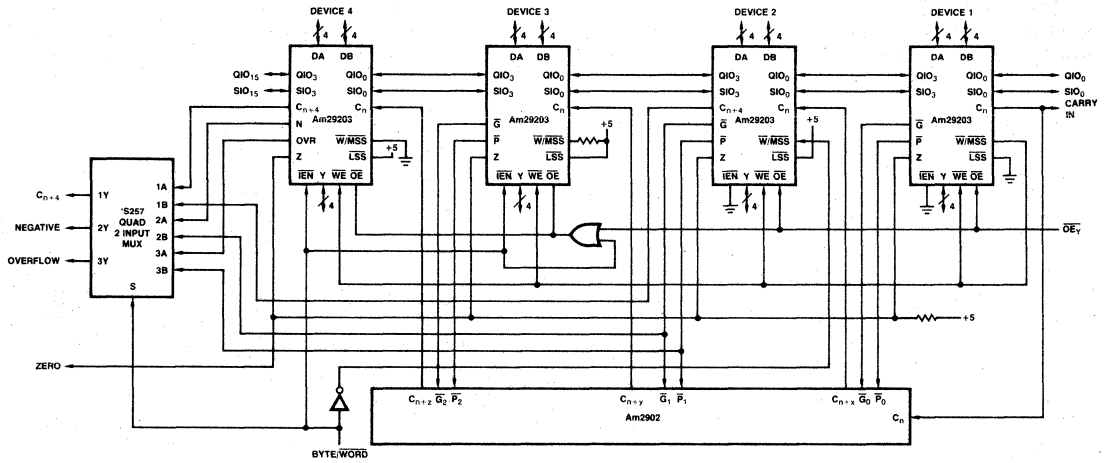
Figure 28. Connections for Word/Byte Operations (Am29203 Only).

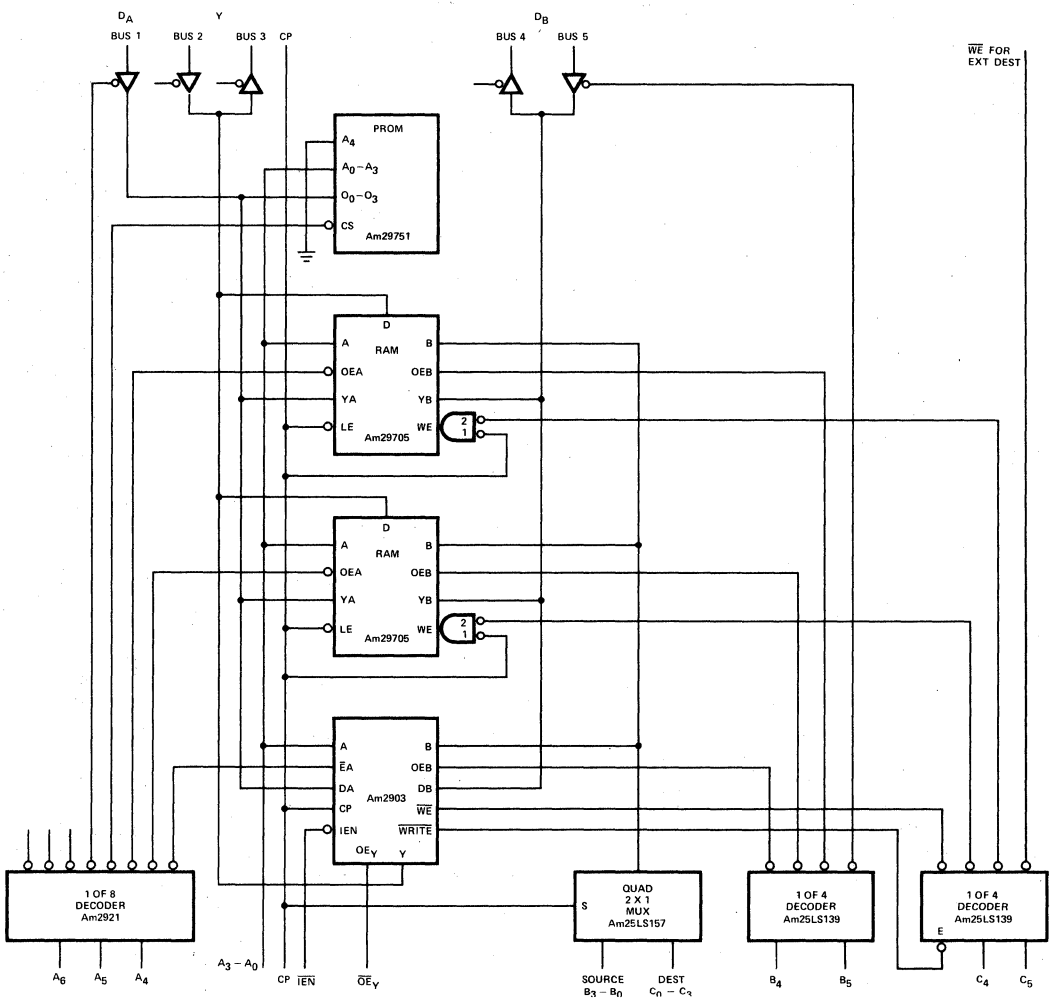


MPR-719

The Am2903 theoretically allows for an infinite memory expansion. Figure 27, *Am2903 and Am29705,* pictures a 4-bit slice of a system which has 48 words of RAM and 16 words of ROM. RAM storage is provided by the Am2903 and the Am29705s. The Am29705 RAM is functionally identical to the Am2903 RAM. The Am27S19 is used to store constants and masks and is addressable from address port A only. The system is organized around five data buses. Inter-bus communication may be done through the Am29705s or the Am2903. The memory addressing scheme specifies the data source for the R input of the ALU eminating from the register locations specified by address field A. A_{0-3} addresses 16 memory locations in each chip while address bits A_{4-6} are decoded and used for the output enable for the desired chip. The B address field is used to select the S input of the ALU and the C field is used to specify the register location where the result of the ALU operation is to be stored.

Bits B_{0-3} are for source register addressing in each chip. Bits B_4 and B_5 are used for chip output enable selection. C_{0-3} access the 16 destination addresses on each chip while bits C_4 and C_5 control the Write Enable of the desired chip. The source and destination register address are multiplexed such that when the clock is HIGH, the source register address is presented to the B address ports of the RAM's. The Instruction Enable ($\overline{IEN}$) is HIGH at this time. The data flows from the Y port or the internal B port as selected by the decoder whose inputs are B_4 and B_5. When the clock goes LOW, the data eminating from the selected Y outputs of the Am29705's and the RAM outputs of the Am2903 are latched and the destination address is now selected for use by the RAM address lines. When the destination address stabilizes on the address lines, the $\overline{IEN}$ pin is brought LOW. The $\overline{WRITE}$ output of the Am2903 will now go LOW, enabling the decoder sourced by address bits C_4 and C_5. The selected decoder line will go LOW, allowing the desired memory location to be written into. To switch between two- and three-address architecture, the user simply makes the source and destination addresses the same; i.e., $B_{0-3} = C_{0-3}$ and $B_{4-5} = C_{4-5}$. For two-address architecture, the MUX is removed from the circuit.

Figure 29. Expanded Memory on Am2903



MPR-059

Am2904

Status and Shift Control Unit

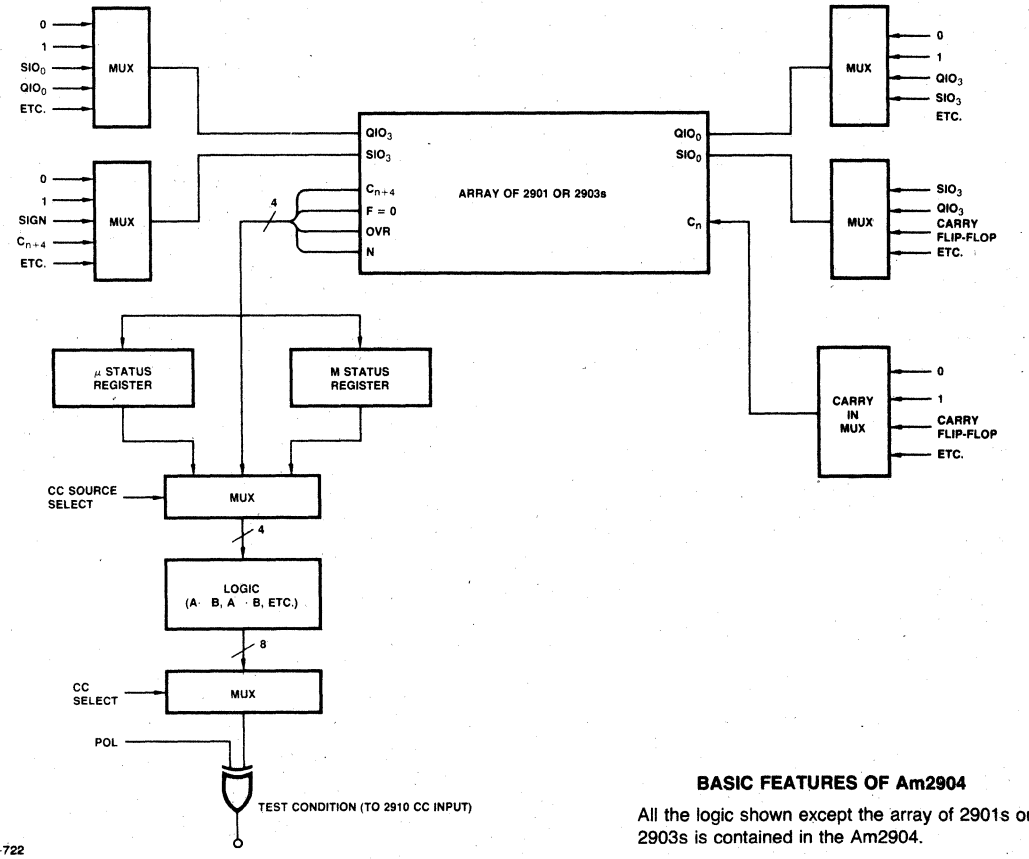
DISTINCTIVE CHARACTERISTICS

- **Replaces most MSI used around any ALU** including the Am2901, Am2903 and MSI ALUs.
- **Generates Carry-In to the ALU**
  Carry signal is selectable from 7 different sources.
- **Contains shift linkage multiplexers**
  Connects to shift lines at the ends of an Am2901 or Am2903 array to implement single and double length arithmetic and logical shifts and rotates – 32 different modes in all.
- **Contains two edge-triggered status registers**
  Use for foreground/background registers in controllers or as microlevel and machine level status registers. Bit manipulating instructions are provided.
- **Condition Code Multiplexer on chip**
  Single cycle tests for any of 16 different conditions. Tests can be performed on either of the two status registers or directly on the ALU output.

DESCRIPTION

The Am2904 is designed to perform all the miscellaneous functions which are usually performed in MSI around an ALU. These include the generation of the carry-in signal to the ALU and carry lookahead unit; the interconnection of the data path, auxiliary register, and carry flip-flop during shift operations; and the storage and testing of ALU status flags. These tasks are accomplished in the Am2904 by three nearly independent blocks of logic. The carry-in is generated by a multiplexer. The shift linkages are established by four three-state multiplexers. There are two registers for storing the carry, overflow, zero, and negative status flags. The condition code multiplexer on the Am2904 can look at true or complement of any of the four status bits and certain combinations of status bits from either of the storage registers or directly from the ALU.

For additional applications refer to Chapter 4 of **Bit Slice Microprocessor Design**, Mick & Brick, McGraw Hill Publications.

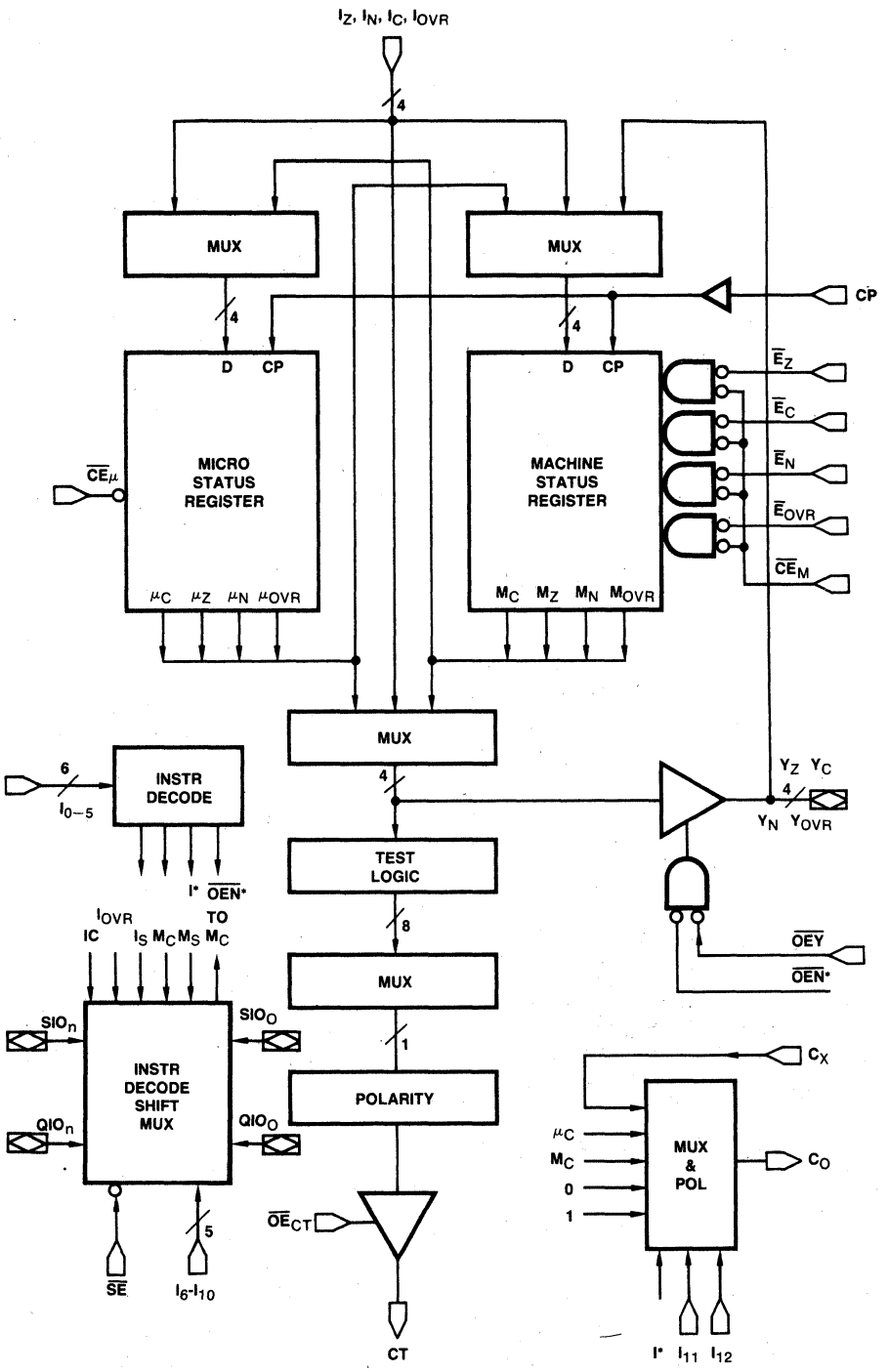


MPR-722

BASIC FEATURES OF Am2904

All the logic shown except the array of 2901s or 2903s is contained in the Am2904.

BLOCK DIAGRAM



*INTERNAL

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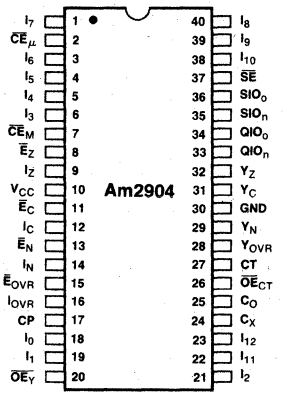
CONNECTION DIAGRAMS
Top Views

D-40



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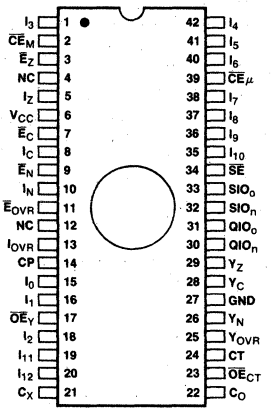
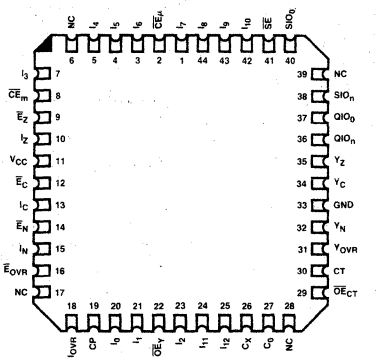
F-42-1



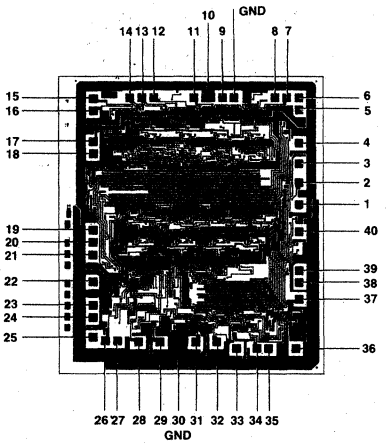
MPR-724

Chip-Pak™ L-44-1



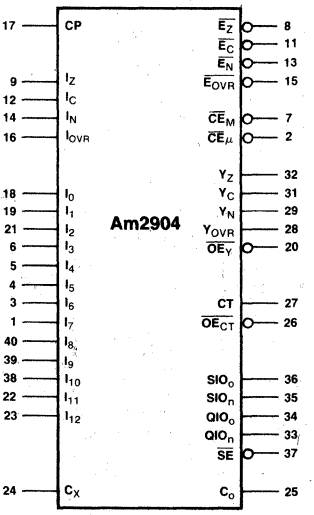
Note: Pin 1 is marked for orientation.
NC = No Connection.

Am2904 Metallization and Pad Layout



DIE SIZE 0.140" X 0.161"
Pad Numbers correspond to DIP pinout

LOGIC SYMBOL (DIP)



V_{CC} = Pin 10
GND = Pin 30

MPR-725

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

PIN DEFINITIONS

I_Z Zero status input pin, intended for connection to the Z outputs of the Am2903 or the F = 0 ouputs of the Am2901.

I_C Carry status input pin, intended for connection to the C_{n+4} output of the most significant ALU slice.

I_N Sign status input pin, intended for connection to the most significant ALU slice. The connection is to the N pin on the Am2903, and the F_3 pin on the Am2901.

I_{OVR} Overflow status input pin, intended for connection to the OVR pin on the most significant ALU slice.

I_{0-12} The thirteen instruction pins which select the operation the Am2904 is to perform.

$\overline{CE_M}$ This pin, used in conjunction with $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$ acts as the overall enable for the machine status register. When the pin is LOW, MSR bits may be modified, according to the states of $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$. When HIGH, the MSR will retain the present state, regardless of the state of $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$.

$\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$ These pins, when LOW, enable the corresponding bits in the Machine Status Register. When HIGH, they will prevent the corresponding bits from changing state. By using these pins together with the $\overline{CE_M}$ pin, MSR bits can be selectively modified.

$\overline{CE_\mu}$ This pin, when LOW, enables all four bits of the Micro Status Register. When this pin is HIGH, the μSR will not change state.

Y_Z, Y_C, Y_N, Y_{OVR} These pins form a three-state bidirectional bus over which MSR and μSR status can be read out or the MSR can be loaded in parallel.

$\overline{OE_Y}$ When LOW, this pin enables the Y pins as outputs. When HIGH, the Y outputs are in the high impedance state.

CT The conditional test output. The output of the Condition Code multiplexer appears here.

$\overline{OE_{CT}}$ When this pin is LOW, the CT pin is active. When HIGH the CT pin is in the high impedance state.

SIO_o, SIO_n, QIO_o, QIO_n These pins complete the linking for the various shift and rotate conditions. SIO_0 is intended for connection to the SIO_0 pin of the least significant Am2903 slice (RAM_0 for Am2901). SIO_n connects to the SIO_3 pin of the most significant Am2903 slice, (RAM_3 for Am2901). QIO_0 connects to the QIO_0 pin of the least significant Am2903 slice (QIO_0 for Am2901) and QIO_n connects to the QIO_3 pin of the most significant Am2903 slice (Q_3 for Am2901).

$\overline{SE}$ This pin controls the state of the shift outputs. When LOW, the shift outputs are enabled. When HIGH, the shift outputs are in the high impedance state.

C_0 This pin is the output of the Carry In control multiplexer. It connects to the C_n input of the least significant ALU slice, and the C_n input of the Am2902A.

C_X This pin is used as an input to the Carry In Control multiplexer which can route it to the C_0 pin. The C_X pin is intended for connection to the Z output of the Am2903 to facilitate some of the Am2903 special instructions.

CP The clock input to the device. The μSR and MSR are modified on the LOW to HIGH transition of the clock input. All other portions of the Am2904 are combinational and are unaffected by CP.

5

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2904DC	D-40	C	C-1
AM2904DC-B	D-40	C	B-2 (Note 4)
AM2904DM	D-40	M	C-3
AM2904DM-B	D-40	M	B-3
AM2904FM	F-42	M	C-3
AM2904FM-B	F-42	M	B-3
AM2904LC	L-44	C	C-1
AM2904LM	L-44	M	C-3
AM2904LM-B	L-44	M	B-3
AM2904XC	Dice	C	Visual Inspection to MIL-STD-883 Method 2010B.
AM2904XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Case) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

OPERATING RANGE

P/N	Range	Temperature	V_{CC}	
Am2904PC, DC	COM'L	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5%	(MIN. = 4.75V, MAX. = 5.25V)
Am2904DM, FM	MIL	T_C = −55°C to +125°C	V_{CC} = 5.0V ±10%	(MIN. = 4.50V, MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.6mA Y_Z, Y_C, Y_N, Y_{OVR}		2.4			Volts
			I_{OH} = −0.8mA SIO_o, SIO_n, QIO_o QIO_n, CT, CO		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Y_Z, Y_C Y_N, Y_{OVR}	I_{OL} = 24mA (Com'l)			0.5	Volts
				I_{OL} = 16mA (MIL)			0.5	
			SIO_o, QIO_o, CT, SIO_n, QIO_n, CO	I_{OL} = 8mA			0.5	
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 7)			2.0			Volts
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 7)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V	CP				−0.7	mA
			$\overline{CE_m}$, $\overline{CE_\mu}$				−1.8	
			I_Z, I_C, I_N, I_{OVR}				−1.2	
			I_0-I_{12}, $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$ $\overline{E_{OVR}}$, $\overline{OE_Y}$, $\overline{OE_{CT}}$, C_X, Y_Z, Y_C, Y_N, Y_{OVR}				−0.45	
			$\overline{SE}$, SIO_o, SIO_n, QIO_o, QIO_n				−1.35	
I_{IH}	Input HIGH Current	V_{CC} = MAX. V_{IN} = 2.7V	CP, I_0-I_{12}, $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$, $\overline{OE_Y}$, $\overline{OE_{CT}}$, C_X				20	μA
			$\overline{CE_m}$, $\overline{CE_\mu}$				80	
			I_Z, I_C, I_N, I_{OVR}, $\overline{SE}$				60	
			SIO_o, SIO_n, QIO_o, QIO_n				110	
			Y_Z, Y_C, Y_N, Y_{OVR}				70	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = MAX.	CT	V_O = 2.4			50	μA
				V_O = 0.5			−50	
			SIO_o, SIO_n, QIO_o, QIO_n (Note 4)	V_O = 2.4			110	
				V_O = 0.5			−1350	
			Y_Z, Y_C, Y_N, Y_{OVR} (Note 4)	V_O = 2.4			70	
				V_O = 0.5			−450	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = 5.75V, V_O = 0.5V			−30		−85	mA
I_{CC}	Power Supply Current (Note 6)	V_{CC} = MAX.		T_A = 25°C		180	296	mA
			Am2904DC	T_A = 0°C to +70°C			318	
				T_A = +70°C			262	
			Am2904DM, FM	T_C = −55°C to +125°C			348	
				T_C = +125°C			222	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These are three-state outputs internally connected to TTL inputs. Input Characteristics are measured with output enables HIGH.
5. "MIL" = Am2904 XM, DM, FM. "COM'L" = Am2904 XC, PC, DC.
6. Worst case I_{CC} is at minimum temperature.
7. These input levels provide zero noise immunity and should only be static tested in a noise-free environment (not functionally tested.)

Am2904 ARCHITECTURE

The Am2904 Status and Shift Control Unit provides four functions which are included in all processors. These are: a) Status Register, b) Condition Code Multiplexer, c) Shift Linkages and d) Carry-in Control. The architecture and instruction codes have been designed to complement the flexibility of the 2900 Family.

Status Register

The Am2904 contains two four-bit registers which can store the status outputs of an ALU: Carry (C), Negative (N), Zero (Z), and Overflow (OVR). They are designated Micro Status Register (μSR) and Machine Status Register (MSR). Each register can be independently controlled. The registers use edge-triggered D-type flip-flops which change state on the LOW to HIGH transition of the Clock Input.

The μSR can be loaded from the four status inputs (I_C, I_N, I_Z, I_{OVR}) or from the MSR under instruction control (I_{0-5}). The bits in the μSR can also be individually set or reset under instruction control (I_{0-5}). When the $\overline{CE}\mu$ input is HIGH, the μSR is inhibited from changing, independent of the I_{0-5} inputs.

The MSR can be loaded from the four status inputs (I_C, I_N, I_Z, I_{OVR}), from the μSR, and from the four parallel input/output pins (Y_C, Y_N, Y_Z, Y_{OVR}) under instruction control (I_{0-5}) .The MSR can also be set, reset or complemented under instruction control (I_{0-5}). The bits in the MSR can be selectively updated by controlling the four bit-enable inputs ($\overline{E_Z}$, $\overline{E_N}$, $\overline{E_C}$, $\overline{E_{OVR}}$) and the $\overline{CE_M}$ input. A LOW on both the $\overline{CE_M}$ input and the bit enable input for a specific bit enables updating that bit. A HIGH on a given bit enable input prevents the corresponding bit changing in the MSR. A HIGH on $\overline{CE_M}$ prevents any bits changing in the MSR.

The four parallel bidirectional input/output pins (Y_Z, Y_N, Y_C, Y_{OVR}) allow the contents of both the μSR and the MSR to be transferred to the system data bus and also allows the MSR to be loaded from the system data bus. This capability is used to save and restore the status registers during certain subroutines and when servicing interrupts.

Condition Code Multiplexer

The Condition Code Multiplexer output, CT, can be selected from 16 different functions. These include the true and complemented state of each of the status bits and combinations of these bits to detect such conditions as "greater than", "greater than or equal to", "less than" or "less than or equal to" for unsigned or two's complement numbers.

The Am2904 can perform these tests on the contents of the μSR, the MSR or the direct status inputs, (I_Z, I_N, I_C, I_{OVR}). The CT output is used as the test ($\overline{CC}$) input of the Am2910 and is provided with an output enable, $\overline{OE_{CT}}$ to make the addition of other condition inputs to this point easy.

Shift Linkage Multiplexer

The Shift Linkage Multiplexer generates the necessary linkages to allow the ALU to perform 32 different shift and rotate functions. Both single length and double length shifts and rotates, with and without carry (M_C), are provided. When the $\overline{SE}$ input is HIGH, the four input/output pins (SIO_0, SIO_n, QIO_0, QIO_n) are disabled. The SIO_0, SIO_n, QIO_0, QIO_n pins of the Am2904 are intended to be directly connected to the RAM_0, RAM_3, Q_0 and Q_3 pins of the Am2901 or the SIO_0, SIO_3, QIO_0, QIO_3 pins of the Am2903.

Carry-In Control Multiplexer

The Carry-In Control Multiplexer generates the C_0 output which can be selected from 7 functions (0, 1, C_X, μ_C, M_C, $\overline{\mu_C}$, $\overline{M_C}$). These functions allow easy implementation of both single length and double length addition and subtraction. The C_X input is intended to be connected to the Z output of the Am2903 to facilitate execution of some of the Am2903 special instructions. The C_0 pin is to be connected to the C_n pin of the least significant Am2901 or Am2903 and the C_n pin of the Am2902A.

Am2904 INSTRUCTION SET

The Am2904 is controlled by manipulating the 13 instruction lines, I_{0-12}, together with the nine enable lines, $\overline{CE_M}$, $\overline{CE}\mu$, $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$, $\overline{OE_Y}$, $\overline{OE_{CT}}$, $\overline{SE}$. Most systems will save on microword bits by tying some of these lines to a fixed level or by connecting certain lines together, or by decoding microinstructions to generate appropriate Am2904 controls.

Status Registers

Instruction lines I_5, I_4, I_3, I_2, I_1, I_0 control the Status Registers. Below, these lines are referred to as two octal digits.

Micro Status Register (μSR)

The instruction codes for the Micro Status Register fall into three groups: Bit Operations, Register Operations and Load Operations (See Table 1 and Map 1). All operations require

TABLE 1. MICRO STATUS REGISTER INSTRUCTION CODES.

Bit Operations

I_{543210} Octal	μSR Operation	Comments
10	$0 \rightarrow \mu_Z$	RESET ZERO BIT
11	$1 \rightarrow \mu_Z$	SET ZERO BIT
12	$0 \rightarrow \mu_C$	RESET CARRY BIT
13	$1 \rightarrow \mu_C$	SET CARRY BIT
14	$0 \rightarrow \mu_N$	RESET SIGN BIT
15	$1 \rightarrow \mu_N$	SET SIGN BIT
16	$0 \rightarrow \mu_{OVR}$	RESET OVERFLOW BIT
17	$1 \rightarrow \mu_{OVR}$	SET OVERFLOW BIT

Register Operations

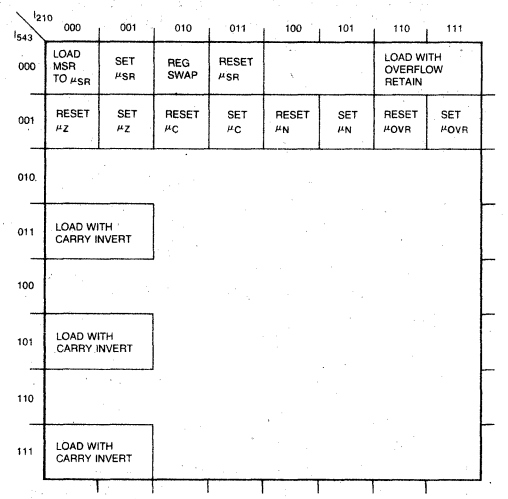
I_{543210} Octal	μSR Operation	Comments
00	$M_X \rightarrow \mu_X$	LOAD MSR TO μSR
01	$1 \rightarrow \mu_X$	SET μSR
02	$M_X \rightarrow \mu_X$	REGISTER SWAP
03	$0 \rightarrow \mu_X$	RESET μSR

Load Operations

I_{543210} Octal	μSR Operation	Comments
06, 07	$I_Z \rightarrow \mu_Z$ $I_C \rightarrow \mu_C$ $I_N \rightarrow \mu_N$ $I_{OVR} + \mu_{OVR} \rightarrow \mu_{OVR}$	LOAD WITH OVERFLOW RETAIN
30, 31 50, 51 70, 71	$I_Z \rightarrow \mu_Z$ $\overline{I_C} \rightarrow \mu_C$ $I_N \rightarrow \mu_N$ $I_{OVR} \rightarrow \mu_{OVR}$	LOAD WITH CARRY INVERT
04, 05 20-27 32-47 52-67 72-77	$I_Z \rightarrow \mu_Z$ $I_C \rightarrow \mu_C$ $I_N \rightarrow \mu_N$ $I_{OVR} \rightarrow \mu_{OVR}$	LOAD DIRECTLY FROM I_Z, I_C, I_N, I_{OVR}

Note: The above tables assume $\overline{CE}\mu$ is LOW.

MAP 1. MICRO STATUS REGISTER INSTRUCTION CODES.



Notes: 1. All unmarked locations are a load direct from I_Z, I_C, I_N, I_{OVR}.

that $\overline{CE}_\mu$ be LOW to operate.

Instruction Codes 10_8 to 17_8 are BIT operations. These operations set or reset the individual bits in the μSR.

Instruction Codes 00_8 to 03_8 are REGISTER operations. These operations affect all bits in the μSR.

00_8 This instruction loads the μSR with the contents of the MSR while loading the MSR from the Y inputs and is further explained under "INTERRUPTS".

01_8 This instruction SETS all μSR bits.

02_8 This instruction SWAPS the contents of the μSR and the MSR. It will also COPY one register to the other if the register to be copied is not enabled.

03_8 This instruction RESETS all μSR bits.

All instruction codes except those mentioned in the above two sections cause a LOAD operation from the I_Z, I_C, I_N, I_{OVR} inputs.

06_8, 07_8 When a series of arithmetic operations are being executed sometimes it is not necessary to test for an overflow condition after *each* operation, but rather it is sufficient simply to know that an overflow occured during any one of the operations. Use of these instructions captures the overflow condition by loading the μSR overflow bit with the LOGICAL OR of its present state and I_{OVR}. Thus, once an overflow occurs, μOVR will remain set throughout the remaining operations.

30_8, 31_8, 50_8, 51_8, 70_8, 71_8 These instructions cause a load from the I inputs, but invert the carry bit. The reason for this is explained more fully under the "BORROW SAVE" section.

All others The remaining instructions load the μSR directly from the I_Z, I_C, I_N, I_{OVR} inputs.

Machine Status Register (MSR)

The instruction codes for the MSR fall into two groups; REGISTER Operations and LOAD Operations. All operations require that $\overline{CE}_M$ be LOW to operate (See Table 2 and Map 2).

BIT operations are accomplished by the use of Register or Load Operations with the $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$ inputs selectively set LOW.

Instruction codes 00_8-03_8 and 05_8 are REGISTER operations. They affect only those bits enabled by $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$.

00_8 This instruction loads the MSR from the Y inputs while transferring the present contents to the μSR. The use of this instruction is further explained under "INTERRUPTS".

01_8 This instruction SETS all enabled MSR bits.

02_8 This instruction SWAPS the contents of the μSR and the MSR. It will also COPY one register to the other if the register to be copied is not enabled.

03_8 This instruction RESETS all enabled MSR bits.

05_8 This instruction COMPLEMENTS all enabled MSR bits.

All instruction codes except those mentioned in the above section cause a LOAD operation from the I_Z, I_C, I_N, I_{OVR} inputs.

04_8 The Am2904 Shift Linkage Multiplexer allows for shifts and rotates through the MSR CARRY bit. Some machines require a shift or rotate through the OVERFLOW bit. By using this code, which swaps the contents of the MSR CARRY bit (M_C) and OVERFLOW bit (M_{OVR}), the shift or rotate can be made to appear to take place through the OVERFLOW bit. The procedure is to swap the bits, shift or rotate (any number or positions) then swap the bits again.

TABLE 2. MACHINE STATUS REGISTER INSTRUCTION CODES.

Register Operations

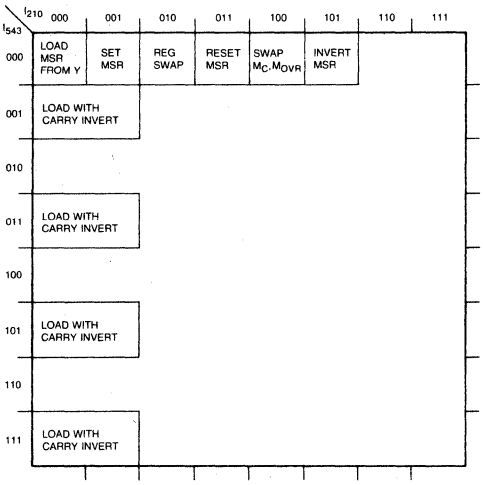
I_{543210} Octal	MSR Operation	Comments
00	$Y_X \rightarrow M_X$	LOAD Y_Z, Y_C, Y_N, Y_{OVR} TO MSR
01	$1 \rightarrow M_X$	SET MSR
02	$\mu_X \rightarrow M_X$	REGISTER SWAP
03	$0 \rightarrow M_X$	RESET MSR
05	$\overline{M_X} \rightarrow M_X$	INVERT MSR

Load Operations

I_{543210} Octal	MSR Operation	Comments
04	$I_Z \rightarrow M_Z$ $M_{OVR} \rightarrow M_C$ $I_N \rightarrow M_N$ $M_C \rightarrow M_{OVR}$	LOAD FOR SHIFT THROUGH OVERFLOW OPERATION
10, 11 30, 31 50, 51 70, 71	$I_Z \rightarrow M_Z$ $\overline{I_C} \rightarrow M_C$ $I_N \rightarrow M_N$ $I_{OVR} \rightarrow M_{OVR}$	LOAD WITH CARRY INVERT
06, 07 12-17 20-27 32-37 40-47 52-67 72-77	$I_Z \rightarrow M_Z$ $I_C \rightarrow M_C$ $I_N \rightarrow M_N$ $I_{OVR} \rightarrow M_{OVR}$	LOAD DIRECTLY FROM I_Z, I_C I_N, I_{OVR}

Notes: 1. The above tables assume $\overline{CE_M}$, $\overline{E_Z}$, $\overline{E_C}$, $\overline{E_N}$, $\overline{E_{OVR}}$ are LOW.
2. A shift-through-carry instruction loads M_C irrespective of I_5-I_0.

MAP 2. MACHINE STATUS REGISTER INSTRUCTION CODES.



Note 1. All unmarked locations are a load direct from I_Z, I_C, I_{OVR}, I_N.

06_8, 07_8 These instructions load the MSR directly from the 12_8-27_8 I_Z, I_C, I_N, I_{OVR} inputs. 32_8-47_8 52_8-67_8 72_8-77_8

10_8, 11_8 These instructions cause a load from the I inputs 30_8, 31_8 but invert the CARRY bit. The reason for this is 50_8, 51_8 explained more fully under the "BORROW SAVE" 70_8, 71_8 section

Condition Code Multiplexer

The four instruction lines I_3, I_2, I_1, I_0 will select one of 16 possible operations to be carried out on the input bits, the result being routed to the Conditional Test Output (CT). Eight of the operations supply an individual status bit or its complement to the CT output. Another four do more complex operations while the remaining four are the complemented results of these (See Table 4).

TABLE 3. Y OUTPUT INSTRUCTION CODES.

$\overline{OE_Y}$	I_5	I_4	Y Output	Comment
1	X	X	Z	Output Off High Impedance
O	O	X	$\mu_i \rightarrow Y_i$	See Note 1
O	1	O	$M_i \rightarrow Y_i$	
O	1	1	$I_i \rightarrow Y_i$	

Notes: 1. For the conditions:
I_5, I_4, I_3, I_2, I_1, I_0 are LOW, Y is an input.
$\overline{OE_Y}$ is "Don't Care" for this condition.
2. X is "Don't Care" condition.

TABLE 4. CONDITION CODE OUTPUT (CT) INSTRUCTION CODES.

$I_3 - 0$ HEX	I_3	I_2	I_1	I_0	$I_5 = I_4 = 0$	$I_5 = 0, I_4 = 1$	$I_5 = 1, I_4 = 0$	$I_5 = I_4 = 1$
0	0	0	0	0	$(\mu_N \oplus \mu_{OVR}) + \mu_Z$	$(\mu_N \oplus \mu_{OVR}) + \mu_Z$	$(M_N \oplus M_{OVR}) + M_Z$	$(I_N \oplus I_{OVR}) + I_Z$
1	0	0	0	1	$(\mu_N \odot \mu_{OVR}) \cdot \bar{\mu}_Z$	$(\mu_N \odot \mu_{OVR}) \cdot \bar{\mu}_Z$	$(M_N \odot M_{OVR}) \cdot \bar{M}_Z$	$(I_N \odot I_{OVR}) \cdot \bar{I}_Z$
2	0	0	1	0	$\mu_N \oplus \mu_{OVR}$	$\mu_N \oplus \mu_{OVR}$	$M_N \oplus M_{OVR}$	$I_N \oplus I_{OVR}$
3	0	0	1	1	$\mu_N \odot \mu_{OVR}$	$\mu_N \odot \mu_{OVR}$	$M_N \odot M_{OVR}$	$I_N \odot I_{OVR}$
4	0	1	0	0	μ_Z	μ_Z	M_Z	I_Z
5	0	1	0	1	$\bar{\mu}_Z$	$\bar{\mu}_Z$	$\bar{M}_Z$	$\bar{I}_Z$
6	0	1	1	0	μ_{OVR}	μ_{OVR}	M_{OVR}	I_{OVR}
7	0	1	1	1	$\bar{\mu}_{OVR}$	$\bar{\mu}_{OVR}$	$\bar{M}_{OVR}$	$\bar{I}_{OVR}$
8	1	0	0	0	$\mu_C + \mu_Z$	$\mu_C + \mu_Z$	$M_C + M_Z$	$\bar{I}_C + I_Z$ (2)
9	1	0	0	1	$\bar{\mu}_C \cdot \bar{\mu}_Z$	$\bar{\mu}_C \cdot \bar{\mu}_Z$	$\bar{M}_C \cdot \bar{M}_Z$	$I_C \cdot \bar{I}_Z$ (2)
A	1	0	1	0	μ_C	μ_C	M_C	I_C
B	1	0	1	1	$\bar{\mu}_C$	$\bar{\mu}_C$	$\bar{M}_C$	$\bar{I}_C$
C	1	1	0	0	$\bar{\mu}_C + \mu_Z$	$\bar{\mu}_C + \mu_Z$	$\bar{M}_C + M_Z$	$\bar{I}_C + I_Z$
D	1	1	0	1	$\mu_C \cdot \bar{\mu}_Z$	$\mu_C \cdot \bar{\mu}_Z$	$M_C \cdot \bar{M}_Z$	$I_C \cdot \bar{I}_Z$
E	1	1	1	0	$I_N \oplus M_N$	μ_N	M_N	I_N
F	1	1	1	1	$I_N \odot M_N$	$\bar{\mu}_N$	$\bar{M}_N$	$\bar{I}_N$

Notes: 1. $\oplus$ Represents EXCLUSIVE-OR
$\odot$ Represents EXCLUSIVE-NOR or coincidence.
2. Correct code as stated.

TABLE 5. CRITERIA FOR COMPARING TWO NUMBERS FOLLOWING "A MINUS B" OPERATION.

	For Unsigned Numbers			For 2's Complement Numbers		
		I_{3-0}			I_{3-0}	
Relation	Status	CT = H	CT = L	Status	CT = H	CT = L
A = B	Z = 1	4	5	Z = 1	4	5
A ≠ B	Z = 0	5	4	Z = 0	5	4
A ≥ B	C = 1	A	B	N $\odot$ OVR = 1	3	2
A < B	C = 0	B	A	N $\oplus$ OVR = 1	2	3
A > B	C · $\overline{Z}$ = 1	D	C	(N $\odot$ OVR) · $\overline{Z}$ = 1	1	0
A ≤ B	$\overline{C}$ + Z = 1	C	D	(N $\oplus$ OVR) + Z = 1	0	1

$\oplus$ = Exclusive OR H = HIGH Note: For Am2910, the CC input is active LOW, so use I_{3-0} code to produce
$\odot$ = Exclusive NOR L = LOW CT = L for the desired test.

The more complex operations are intended to follow the calculation A-B to give an indication of which is the larger (A, B unsigned) or more positive (A, B in 2's complement form). See Table 5.

The two instruction lines I_4, I_5 select whether the μSR, the MSR or the direct inputs I_Z, I_C, I_N, I_{OVR} are used as the inputs to the Y output buffer and the CT output (see Tables 3 and 4).

Instruction codes 16_8 and 17_8 form the EXCLUSIVE – OR and the EXCLUSIVE – NOR functions of M_N and I_N. The use of these instructions is explained under "NORMALIZING".

Shift Linkage Multiplexer

The five instruction lines I_{10}, I_9, I_8, I_7, I_6 control the SHIFT LINKAGE multiplexer. All instructions set up the linkages for both the ALU shifter (RAM shifter on the Am2901A) and the Q register.

UP and DOWN shifts are decided by I_{10} which should be connected to I_8 of the Am2903's instruction lines or I_7 of the Am2901's instruction lines. A wide range of input and output connections are provided, allowing for single or double length shifting or rotating with or without the use of the MSR CARRY or SIGN bits (See Table 7).

In the following discussion of some of the shifts the instruction codes are given as two octal digits AB; A represents I_{10}, I_9, B represents I_8, I_7, I_6.

When adding and down shifting on the same microcycle, (i.e. when doing multiplication or averaging) the shifter input must be the present CARRY, I_C, rather than the carry resulting from the last cycle (M_C). Instruction Code 13_8 accomplishes this for unsigned arithmetic. For 2's complement arithmetic, the required shifter input is: $I_N \oplus I_{OVR}$. This is provided by Instruction Code 16_8.

Instruction Codes 14_8, 15_8, 17_8 provide the RIGHT ROTATE THROUGH CARRY, ROTATE BRANCH CARRY and ROTATE WITHOUT CARRY functions respectively.

Instruction Codes 34_8, 35_8, 37_8 provide the LEFT ROTATE THROUGH CARRY, ROTATE BRANCH CARRY and ROTATE WITHOUT CARRY functions respectively.

The shift outputs are in the high impedance state unless $\overline{SE}$ is LOW.

Loading of the M_C bit by a shift operation overrides any loading or holding of the M_C bit by MSR Instructions (I_{0-5}, $\overline{CE_M}$ and $\overline{E_C}$).

"CARRY-IN" Control Multiplexer

The two instruction lines I_{12}, I_{11} control the source of the CARRY output (C_0).

When $I_{12} = 0$ $\quad C_0 = I_{11}$

When $I_{12} = 1$ and $I_{11} = 0$, the external carry input C_X is presented to the carry output.

When $I_{12} = I_{11} = 1$ the carry output is selected from μ_C, $\overline{\mu_C}$, M_C or $\overline{M_C}$ as defined by I_5, I_3, I_2, I_1 (See Table 6).

TABLE 6. CARRY-IN CONTROL MULTIPLEXER INSTRUCTION CODES.

I_{12}	I_{11}	I_5	I_3	I_2	I_1	C_0
0	0	X	X	X	X	0
0	1	X	X	X	X	1
1	0	X	X	X	X	C_X
1	1	0	0	X	X	μ_C
1	1	0	X	1	X	μ_C
1	1	0	X	X	1	μ_C
1	1	0	1	0	0	$\overline{\mu}_C$
1	1	1	0	X	X	M_C
1	1	1	X	1	X	M_C
1	1	1	X	X	1	M_C
1	1	1	1	0	0	$\overline{M}_C$

APPLICATIONS INFORMATION

Borrow – Save

One of the capabilities of the Am2900 Family is the complete emulation of other processing machines. One requirement of an emulator is that, when a calculation is being performed, not only must the answer obtained from the Am2900 chips be the same as that from the machine being emulated, but after each machine level instruction, the status bits must be indentical.

There are alternative methods for subtracting in a digital machine and the state of the CARRY after the calculation depends on the method. For instance, the subtraction of 0100 from 1010 by the 2's complement add method generates a result of 0110 with a CARRY. Direct subtraction however, yields an answer of 0110 with no BORROW.

Many machines store the state of the CARRY for subtract operations, and this is the recommended method for maximum effective use of the Am2904, but, to allow those machines which store the BORROW to be efficiently emulated, the Am2904 has allocated special instructions. Using these codes causes the CARRY bit to be inverted before storage in the status registers and also re-inverts these status bits before using them as carry inputs. These codes are 10_8, 11_8, 30_8, 31_8, 50_8, 51_8, 70_8, 71_8 (I_{5-0}).

Notice that when these codes are used to load the inverted CARRY to either of the status registers, the CT output selected by the Condition Code Multiplexer assumes the CARRY is inverted and still defines whether $A > B$ or $A \leq B$ (See Table 4).

Similarly, when doing a compare on a machine which saves the borrow, testing for $A > B$, $A \leq B$ forces the complement of the CARRY to be stored in the status registers (See Tables 1 and 2).

Normalizing

Normalizing is the process of stripping off all leading sign bits until the two most significant bits are complementary. The Am2904 facilitates both single and double length normalization in the Am2901 and the Am2903. When using the NORMALIZE special instructions with the Am2903, the EXCLUSIVE – OR of the most significant two bits is generated at the C_{n+4} pin of the most significant Am2903. The EXCLUSIVE – OR of the two bits next to the most significant bit is also generated at the OVR pin. The procedure for normalizing then is to loop on the normalize instruction with a branch condition on the C_{n+4} state or the OVR state, depending on the architecture employed. The C_{n+4} or OVR output is routed to the Am2910 CC input through the Am2904 Condition Code multiplexer. As the contents of the status registers always refers to the last cycle, not the present one, the last operation in Normalizing is to downshift, bringing the sign bit (M_N) back into the most significant bit position. This is achieved using the shift operations 05_8 (I_{10-6}) for double length normalizing,

TABLE 7. SHIFT LINKAGE MULTIPLEXER INSTRUCTION CODES.

I_{10}	I_9	I_8	I_7	I_6	M_C RAM Q	SIO_0	SIO_n	QIO_0	QIO_n	Loaded into M_C
					MSB LSB MSB LSB					
0	0	0	0	0		Z	0	Z	0	
0	0	0	0	1		Z	1	Z	1	
0	0	0	1	0		Z	0	Z	M_N	SIO_0
0	0	0	1	1		Z	1	Z	SIO_0	
0	0	1	0	0		Z	M_C	Z	SIO_0	
0	0	1	0	1		Z	M_N	Z	SIO_0	
0	0	1	1	0		Z	0	Z	SIO_0	
0	0	1	1	1		Z	0	Z	SIO_0	QIO_0
0	1	0	0	0		Z	SIO_0	Z	QIO_0	SIO_0
0	1	0	0	1		Z	M_C	Z	QIO_0	SIO_0
0	1	0	1	0		Z	SIO_0	Z	QIO_0	
0	1	0	1	1		Z	I_C	Z	SIO_0	
0	1	1	0	0		Z	M_C	Z	SIO_0	QIO_0
0	1	1	0	1		Z	QIO_0	Z	SIO_0	QIO_0
0	1	1	1	0		Z	$I_N \oplus I_{OVR}$	Z	SIO_0	
0	1	1	1	1		Z	QIO_0	Z	SIO_0	
					MSB LSB MSB LSB					
1	0	0	0	0		0	Z	0	Z	SIO_n
1	0	0	0	1		1	Z	1	Z	SIO_n
1	0	0	1	0		0	Z	0	Z	
1	0	0	1	1		1	Z	1	Z	
1	0	1	0	0		QIO_n	Z	0	Z	SIO_n
1	0	1	0	1		QIO_n	Z	1	Z	SIO_n
1	0	1	1	0		QIO_n	Z	0	Z	
1	0	1	1	1		QIO_n	Z	1	Z	
1	1	0	0	0		SIO_n	Z	QIO_n	Z	SIO_n
1	1	0	0	1		M_C	Z	QIO_n	Z	SIO_n
1	1	0	1	0		SIO_n	Z	QIO_n	Z	
1	1	0	1	1		M_C	Z	0	Z	
1	1	1	0	0		QIO_n	Z	M_C	Z	SIO_n
1	1	1	0	1		QIO_n	Z	SIO_n	Z	SIO_n
1	1	1	1	0		QIO_n	Z	M_C	Z	
1	1	1	1	1		QIO_n	Z	SIO_n	Z	

Notes: 1. Z = High impedance (outputs off) state.
2. Outputs enabled and M_C loaded only if $\overline{SE}$ is LOW.
3. Loading of M_C from I_{10-6} overrides control from I_{5-0}, $\overline{CE}_M$, $\overline{E}_C$.

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and 02_8 for single length normalizing. For more details regarding normalizing with the Am2903 see the Am2903 data sheet.

The Am2901 does not have the EXCLUSIVE – OR gates to help with normalizing, so the Am2904 includes in the Condition Code multiplexer the EXCLUSIVE – OR and EXCLUSIVE – NOR functions of M_N (the sign bit resulting from the last operation) and I_N (the sign bit resulting from the present operation).

Interrupts

Some machines allow interrupts only at the machine instruction level while others allow them at the microinstruction level. The Am2904 is designed to handle both cases.

When the machine is interrupted, it is necessary to store the contents of either the MSR (machine instruction level interrupts) or both the status registers (micro instruction level interrupts) into an external store. This transfer is intended to take place over the Y input/output pins (See Table 3).

After the interrupt has been serviced the registers must be restored to their pre-interrupt state. This is accomplished by two operations of instruction 00_8 (I_{5-0}) which loads the MSR from the Y inputs while loading the μSR from the MSR. Thus, the pre-interrupt contents of the μSR are first loaded to the MSR (first instruction 00_8), then this data is transferred to the μSR while the MSR is restored to its pre-interrupt state (second instruction 00_8).

In controllers and some other microprogrammed machines the applications program itself is often in the microprogram memory; that is, there is no macroinstruction set. These machines require only a microstatus register since there is no separate machine status. The MSR in the Am2904 can be used as a one-level stack on the microstatus register. When an interrupt occurs, the μSR and the MSR are simply swapped ($I_{5-0} = 02_8$).

SWITCHING CHARACTERISTICS

The tables below define the Am2904 switching characteristics. Tables A are set-up and hold times relative to the clock LOW-to-HIGH transition. Tables B are combinational delays. Tables C are clock requirements. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns. All outputs have maximum DC loading.

GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

(T_A = 0 to +70°C, V_{CC} = 4.75 to +5.25V, C_L = 50pF)

A. Set-up and Hold Times (ns)

Input	t_s	t_h
I_Z, I_N, I_{OVR}	14	5
I_C (I_1 I_2 I_3 = 001)	27	5
I_C (I_1 I_2 I_3 ≠ 001)	14	5
$\overline{CE}_\mu$	18	3
$\overline{CE}_M$	23	3
$\overline{E}_Z$, $\overline{E}_C$, $\overline{E}_N$ $\overline{E}_{OVR}$	22	3(b)
I_0-I_5	41	1
I_6-I_{10}	40	1
$\overline{SE}$	36	0
Y_Z, Y_C, Y_N, Y_{OVR} ($I_{0\text{-}5}$ = LOW)	15	5
SIO_o, SIO_n, QIO_o, QIO_n	20	5

B. Combinational Delays (ns)

From (Input)	To (Output)	t_{pd}
I_Z I_C I_N I_{OVR}	Y_Z Y_C Y_N Y_{OVR}	38
CP	Y_Z, Y_C, Y_N, Y_{OVR}	41
I_4, I_5	Y_Z, Y_C, Y_N, Y_{OVR}	35
I_Z, I_C, I_N, I_{OVR}	CT	33
CP	CT	36
I_0-I_5	CT	33
C_X	C_O	20
CP	C_O	27
$I_{1, 2, 3, 5, 11, 12}$	C_O	39
SIO_n, QIO_n	SIO_o	19
SIO_o, QIO_o	SIO_n	19
I_C, I_N, I_{OVR}	SIO_n	26
SIO_n, QIO_n	QIO_o	19
SIO_o, QIO_o	QIO_n	19
CP	SIO_o, SIO_n QIO_o, QIO_n	30
I_6-I_{10}	SIO_o, SIO_n QIO_o, QIO_n	26

C. Clock Requirements (ns)

Minimum Clock LOW Time	20
Minimum Clock HIGH Time	20

D. Enable/Disable Times (ns)

C_L = 5.0pF for output disable tests

From (Input)	To (Output)	Enable	Disable
OE_{CT}	CT	23	18
SE	SIO_o, SIO_n QIO_o, QIO_n	30	12
I_{10}	SIO_o, SIO_n QIO_o, QIO_n	39	29
OE_Y	Y_Z, Y_C, Y_N, Y_{OVR}	26	21
I_0-I_5	Y_Z, Y_C, Y_N, Y_{OVR}	28	40

5

GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

(T_C = −55 to +125°C, V_{CC} = 4.5 to +5.5V, C_L = 50pF)

A. Set-up and Hold Times (ns)

Input	t_s	t_h
I_Z, I_N, I_{OVR}	15	5
I_C (I_1 I_2 I_3 = 001)	28	5
I_C (I_1 I_2 I_3 ≠ 001)	15	5
$\overline{CE}_\mu$	20	3
$\overline{CE}_M$	23	4
$\overline{E}_Z$, $\overline{E}_C$, $\overline{E}_N$ $\overline{E}_{OVR}$	23	4
I_0-I_5	48	2
I_6-I_{10}	44	2
$\overline{SE}$	40	0
Y_Z, Y_C, Y_N, Y_{OVR} ($I_{0\text{-}5}$ = LOW)	16	6
SIO_o, SIO_n, QIO_o, QIO_n	20	5

B. Combinational Delays (ns)

From (Input)	To (Output)	t_{pd}
I_Z I_C I_N I_{OVR}	Y_Z Y_C Y_N Y_{OVR}	40
CP	Y_Z, Y_C, Y_N, Y_{OVR}	45
I_4, I_5	Y_Z, Y_C, Y_N, Y_{OVR}	38
I_Z, I_C, I_N, I_{OVR}	CT	44
CP	CT	40
I_0-I_5	CT	41
C_X	C_O	22
CP	C_O	28
$I_{1, 2, 3, 5, 11, 12}$	C_O	42
SIO_n, QIO_n	SIO_o	20
SIO_o, QIO_o	SIO_n	20
I_C, I_N, I_{OVR}	SIO_n	29
SIO_n, QIO_n	QIO_o	20
SIO_o, QIO_o	QIO_h	20
CP	SIO_o, SIO_n QIO_o, QIO_n	32
I_6-I_{10}	SIO_o, SIO_n QIO_o, QIO_n	31

C. Clock Requirements (ns)

Minimum Clock LOW Time	25
Minimum Clock HIGH Time	25

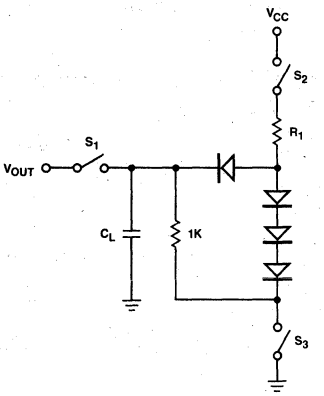
D. Enable/Disable Times (ns)

C_L = 5.0pF for output disable tests

From (Input)	To (Output)	Enable	Disable
OE_{CT}	CT	25	18
SE	SIO_o, SIO_n QIO_o, QIO_n	35	16
I_{10}	SIO_o, SIO_n QIO_o, QIO_n	43	32
OE_Y	Y_Z, Y_C, Y_N, Y_{OVR}	28	23
I_0-I_5	Y_Z, Y_C, Y_N, Y_{OVR}	30	41

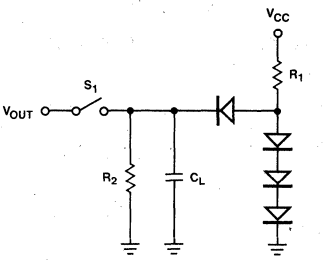
TEST OUTPUT LOAD CONFIGURATIONS FOR Am2904

A. THREE-STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2904

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
25	C_0	B	470	3K
27	CT	A	430	1K
28	Y_{OVR}	A	220	1K
29	Y_N	A	220	1K
31	Y_C	A	220	1K
32	Y_Z	A	220	1K
33	QIO_N	A	430	1K
34	QIO_0	A	430	1K
35	SIO_N	A	430	1K
36	SIO_0	A	430	1K

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5–8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

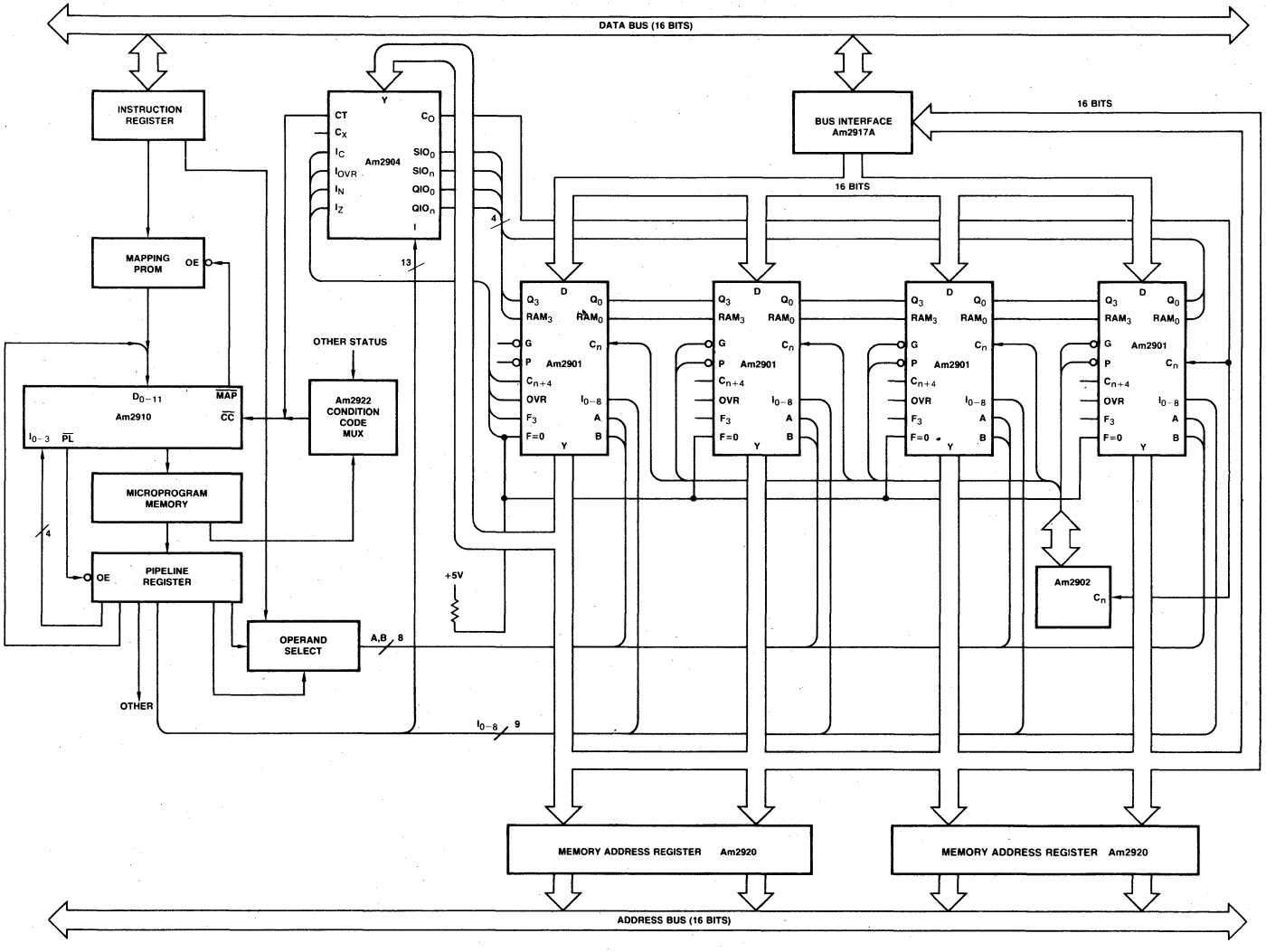


Figure 1. Typical Application of Am2904 with Am2901.

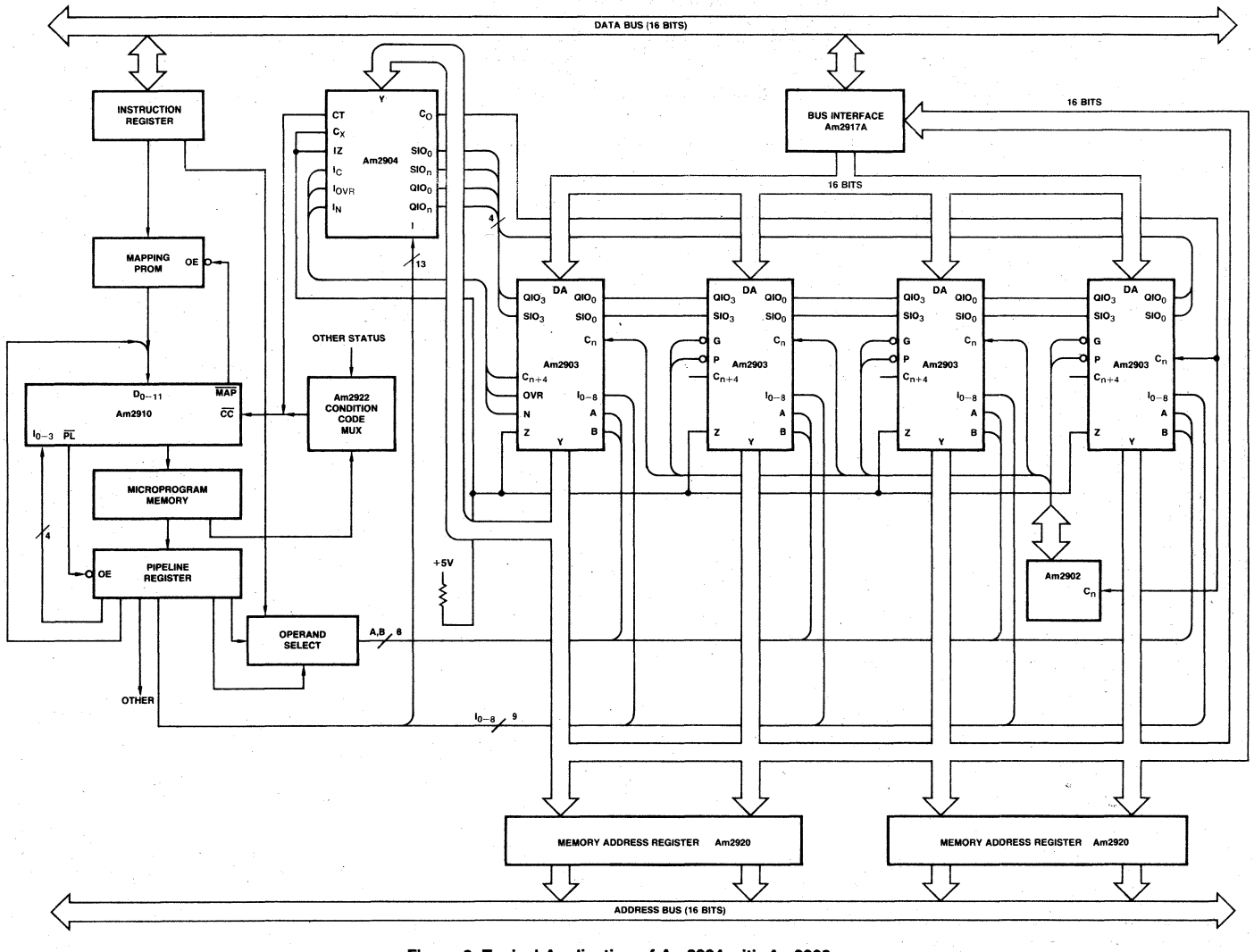


Figure 2. Typical Application of Am2904 with Am2903.

Am2905

Quad Two-Input OC Bus Transceiver with Three-State Receiver

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Open-collector bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 100 mA at 0.8V max.
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12 mA
- Advanced low-power Schottky processing

FUNCTIONAL DESCRIPTION

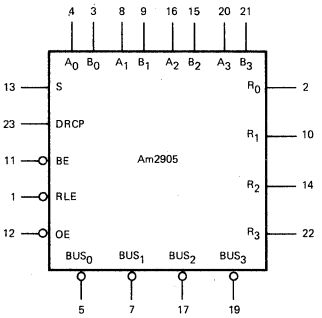
The Am2905 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches that feature three-state outputs.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B inputs is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

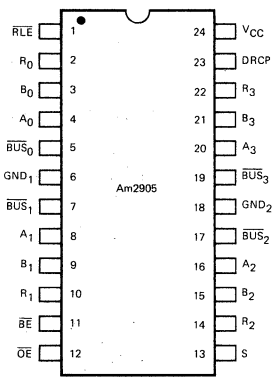
LOGIC SYMBOL



V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

MPR-063

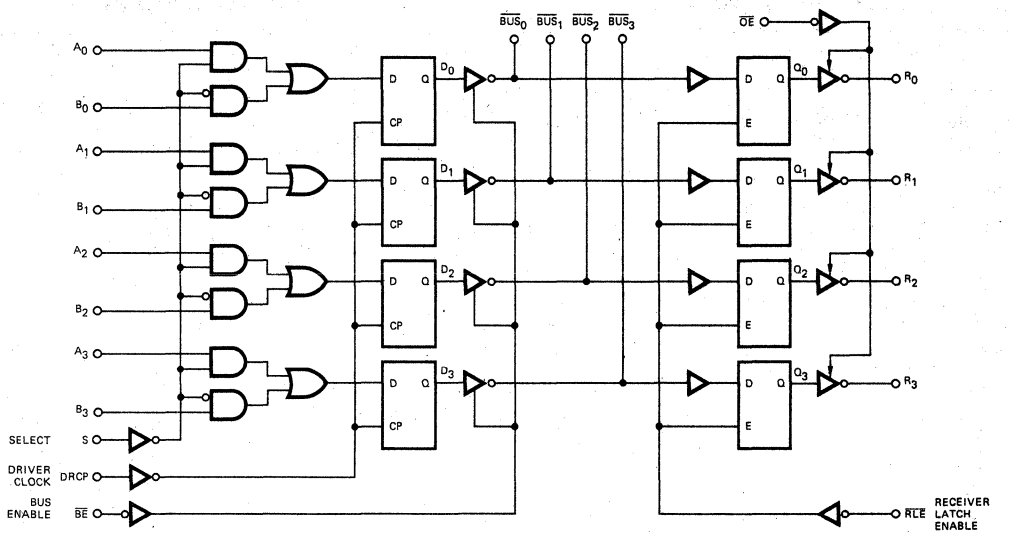
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-064

LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	200mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2905XC (COM'L) T_A = 0°C to +70°C V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V
Am2905XM (MIL) T_A = −55°C to +125°C V_{CC} MIN. = 4.50V V_{CC} MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.	V_O = 0.4V				−50	µA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V					100	µA
V_{TH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus enable = 2.4V		MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2905XC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
Am2905XM MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

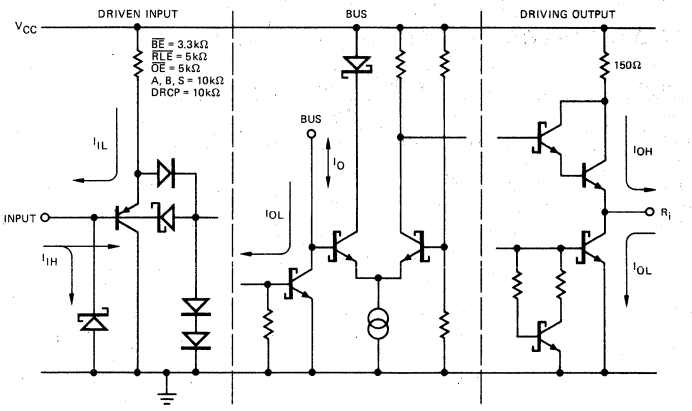
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	$V_{CC} = V_{IN}$, $V_{IN} = V_{IL}$ or V_{IH}	MIL, $I_{OH} = -1.0$mA	2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6$mA	2.4	3.4		
V_{OL}	Receiver Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 4mA		0.27	0.4	Volts
			I_{OL} = 8mA		0.32	0.45	
			I_{OL} = 12mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18$mA				−1.5	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4$V				−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7$V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 5.5$V				100	μA
I_O	Receiver Off-State Output Current	V_{CC} = MAX.	$V_O = 2.4$V			20	μA
			$V_O = 0.4$V			−20	
I_{SC}	Receiver Output Short Circuit Current	V_{CC} = MAX.		−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All inputs = GND			69	105	mA

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2905XM Min.	Am2905XM Typ. (Note 2)	Am2905XM Max.	Am2905XC Min.	Am2905XC Typ. (Note 2)	Am2905XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 50Ω		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_s	Data Inputs (A or B)	C_L = 15pF, R_L = 2.0kΩ	25			23			ns
t_h			8.0			7.0			
t_s	Select Input (S)		33			30			ns
t_h			8.0			7.0			
t_{PW}	Driver Clock (DRCP) Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enable)			18	37		18	34	ns
t_{PHL}				18	37		18	34	
t_{PLH}	Latch Enable to Receiver Output			21	37		21	34	ns
t_{PHL}				21	37		21	34	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{ZH}	Output Control to Receiver Output			14	28		14	25	ns
t_{ZL}				14	28		14	25	
t_{HZ}	Output Control to Receiver Output			14	28		14	25	ns
t_{LZ}				14	28		14	25	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

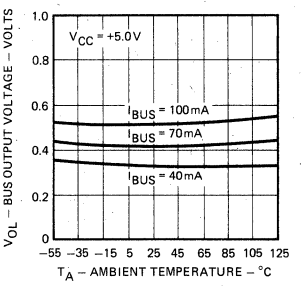


Note: Actual current flow direction shown.

MPR-066

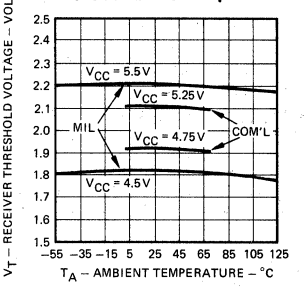
TYPICAL PERFORMANCE CURVES

Bus Output Low Voltage Versus Ambient Temperature



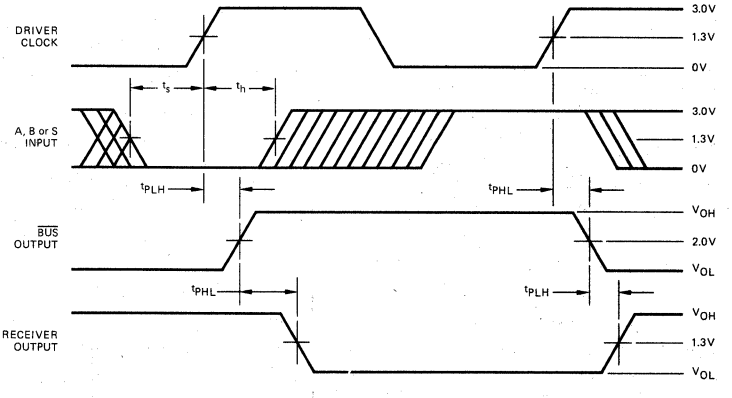
MPR-067

Receiver Threshold Variation Versus Ambient Temperature



MPR-068

SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

MPR-069

FUNCTION TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2905PC	P-24	C	C-1
AM2905DC	D-24	C	C-1
AM2905DC-B	D-24	C	B-1
AM2905DM	D-24	M	C-3
AM2905DM-B	D-24	M	B-3
AM2905FM	F-24-1	M	C-3
AM2905FM-B	F-24-1	M	B-3
AM2905XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2905XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V.
   M = −55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

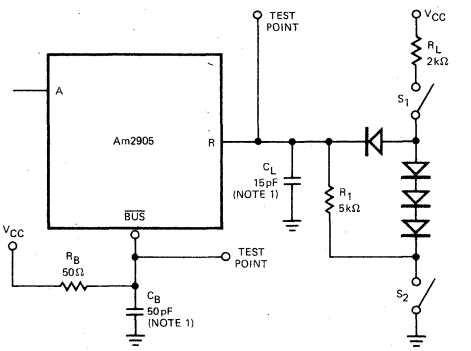
$\overline{BUS}_0$, $\overline{BUS}_1$ $\overline{BUS}_2$, $\overline{BUS}_3$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

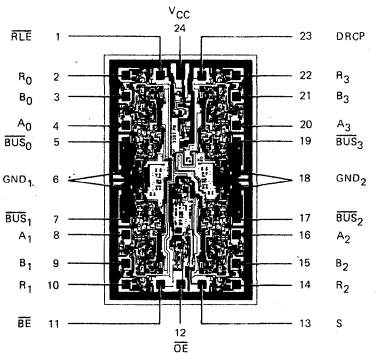
$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

LOAD TEST CIRCUIT



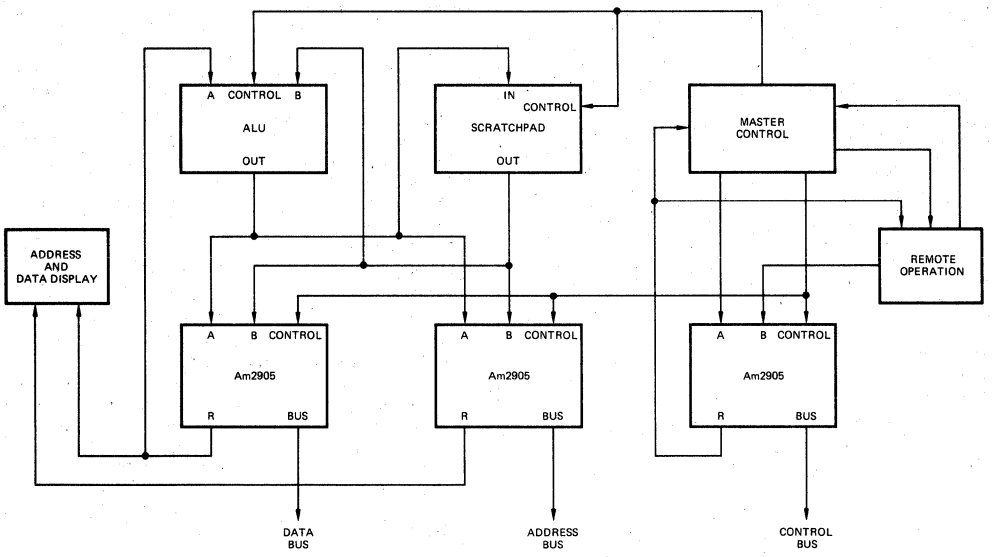
MPR-070

Metallization and Pad Layout



DIE SIZE 0.080" X 0.130"

APPLICATIONS



The Am2905 is a universal Bus Transceiver useful for many system data, address, control and timing input/output interfaces.

MPR-071

Am2906

Quad Two-Input OC Bus Transceiver with Parity

Distinctive Characteristics

- Quad high-speed LSI bus transceiver.
- Open-collector bus driver.
- Two-port input to D-type register on driver.
- Bus driver output can sink 100 mA at 0.8V max.
- Internal odd 4-bit parity checker/generator.
- Receiver has output latch for pipeline operation.
- Receiver outputs sink 12 mA.
- Advanced low-power Schottky processing.

FUNCTIONAL DESCRIPTION

The Am2906 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches. The device also contains a four-bit odd parity checker/generator.

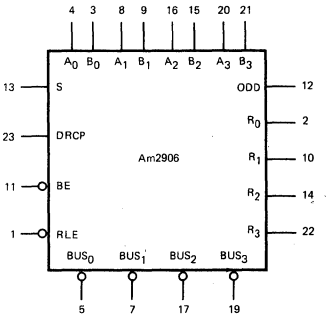
This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input.

The Am2906 features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A or B field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

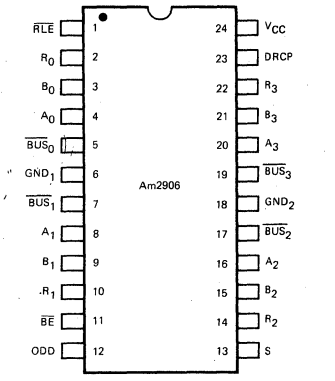
LOGIC SYMBOL



V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

MPR-073

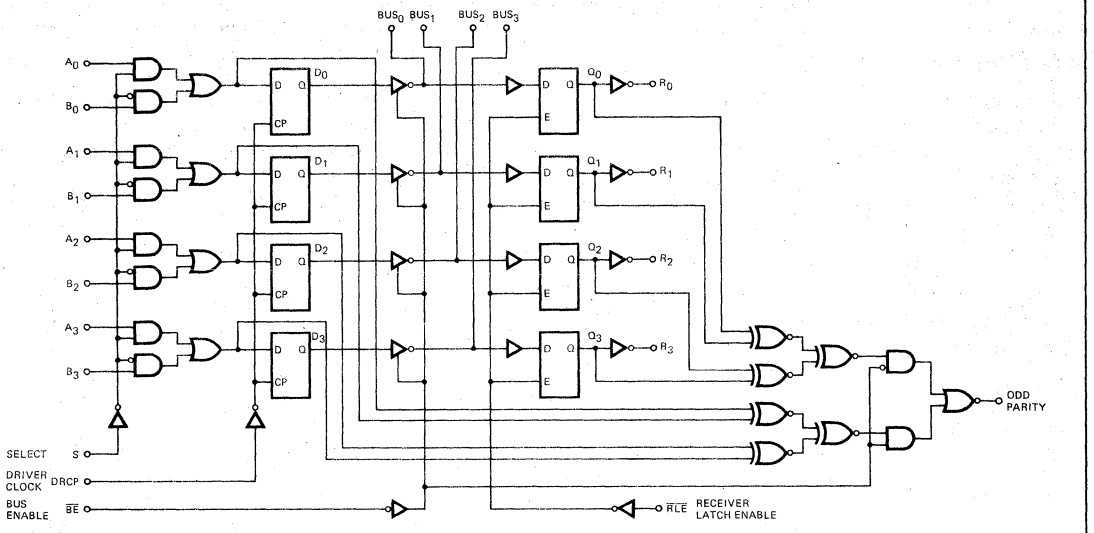
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-074

LOGIC DIAGRAM



MPR-075

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	200mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2906XC (COM'L)	T_A = 0°C to +70°C	V_{CC} MIN. = 4.75V	V_{CC} MAX. = 5.25V
Am2906XM (MIL)	T_A = −55°C to +125°C	V_{CC} MIN. = 4.50V	V_{CC} MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Bus Output LOW Voltage		I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.	V_O = 0.4V				−50	μA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus enable = 2.4V		MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2906XC (COM'L)	$T_A = 0°C$ to $+70°C$	V_{CC} MIN. = 4.75V	V_{CC} MAX. = 5.25V
Am2906XM (MIL)	$T_A = -55°C$ to $+125°C$	V_{CC} MIN. 4.5V	V_{CC} MAX. = 5.5V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

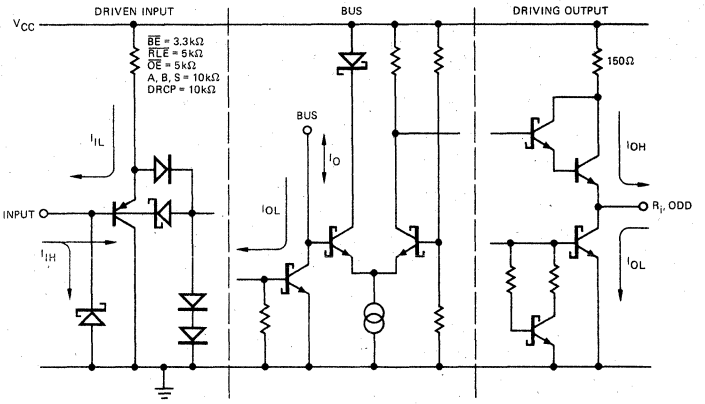
Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL	$I_{OH} = -1mA$	2.4	3.4		Volts
			COM'L	$I_{OH} = -2.6mA$	2.4	3.4		
	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu A$, $V_{IN} = V_{IH}$ or V_{IL}		MIL	2.5	3.4		
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	$I_{OL} = 4mA$			0.27	0.4	Volts
			$I_{OL} = 8mA$			0.32	0.45	
			$I_{OL} = 12mA$			0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18mA$					−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4V$					−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7V$					20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 5.5V$					100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.			−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All inputs = GND				72	105	mA

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2906XM Min.	Am2906XM Typ. (Note 2)	Am2906XM Max.	Am2906XC Min.	Am2906XC Typ. (Note 2)	Am2906XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 50Ω		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_s	Data Inputs (A or B)	C_L = 15pF, R_L = 2.0kΩ	25			23			ns
t_h			8.0			7.0			
t_s	Select Inputs (S)		33			30			ns
t_h			8.0			7.0			
t_{PW}	Clock Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	37		18	34	ns
t_{PHL}				18	37		18	34	
t_{PLH}	Latch Enable to Receiver Output			21	37		21	34	ns
t_{PHL}				21	37		21	34	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{PLH}	A or B Data to Odd Parity Output (Driver Enabled)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Bus to Odd Parity Output (Driver Inhibited, Latch Enabled)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	40		21	36	ns
t_{PHL}				21	40		21	36	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

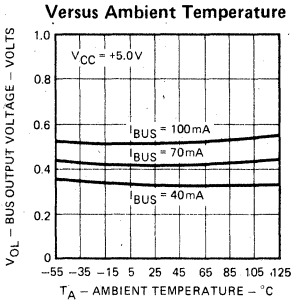


Note: Actual current flow direction shown.

MPR-076

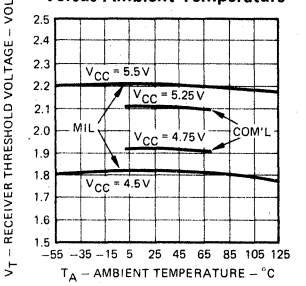
TYPICAL PERFORMANCE CURVES

Bus Output Low Voltage Versus Ambient Temperature



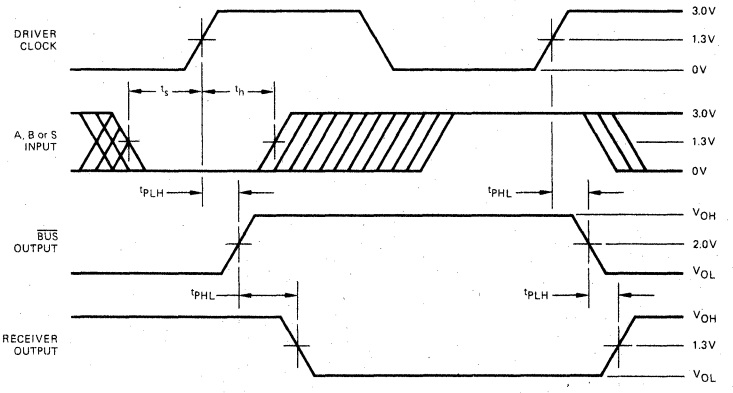
MPR-077

Receiver Threshold Variation Versus Ambient Temperature



MPR-078

SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

MPR-079

FUNCTION TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2906PC	P-24	C	C-1
AM2906DC	D-24	C	C-1
AM2906DC-B	D-24	C	B-1
AM2906DM	D-24	M	C-3
AM2906DM-B	D-24	M	B-3
AM2906FM	F-24-1	M	C-3
AM2906FM-B	F-24-1	M	B-3
AM2906XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2906XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V.
   M = −55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

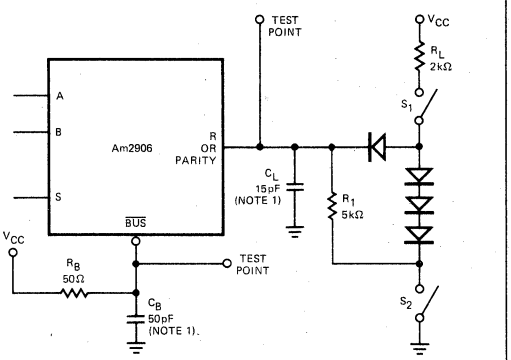
$\overline{BUS}_0, \overline{BUS}_1$ $\overline{BUS}_2, \overline{BUS}_3$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

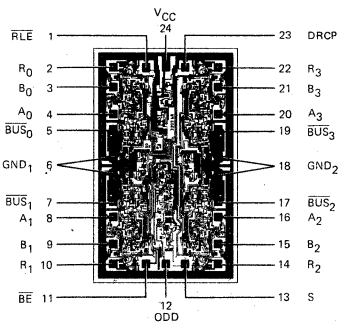
$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

LOAD TEST CIRCUIT



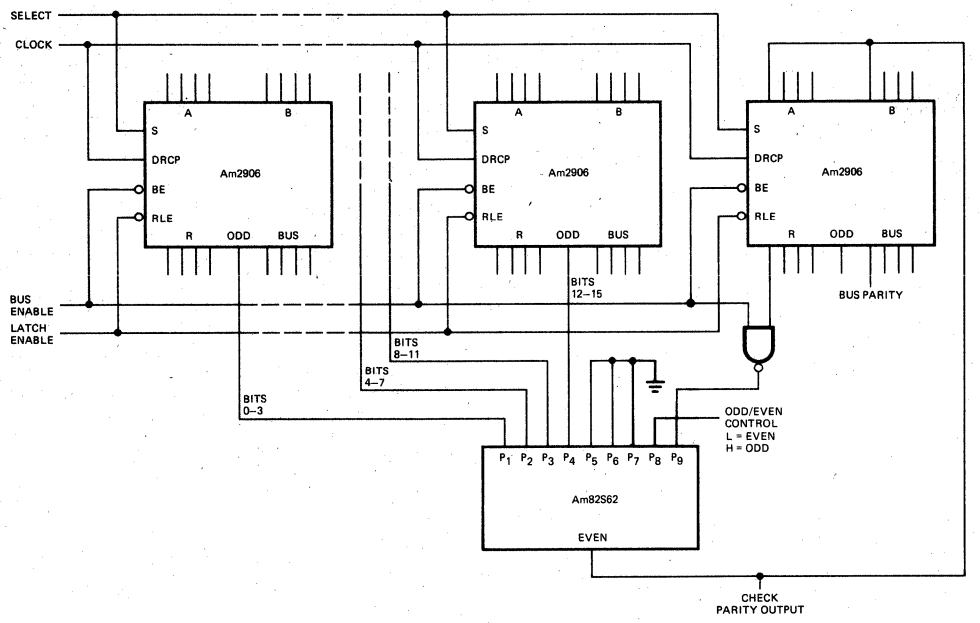
MPR-080

Metallization and Pad Layout



DIE SIZE 0.080" X 0.130"

APPLICATIONS



Generating or checking parity for 16 data bits.

MPR-081

Am2907 • Am2908

Quad Bus Transceivers with Interface Logic

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Open-collector bus driver
- D-type register on driver
- Bus driver output can sink 100mA at 0.8V max.
- Internal odd 4-bit parity checker/generator
- Am2907 has 2.0V input receiver threshold; Am2908 is "DEC Q or LSI-II bus compatible" with 1.5V receiver threshold
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- Advanced Low-power Schottky processing

5

FUNCTIONAL DESCRIPTION

The Am2907 and Am2908 are high-performance bus transceivers intended for bipolar or MOS microprocessor system applications. The Am2908 is Digital Equipment Corporation "Q or LSI-II bus compatible" while the Am2907 features a 2.0V receiver threshold. These devices consist of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches, that feature three-state outputs. The devices also contain a four-bit odd parity checker/generator.

These LSI bus transceivers are fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

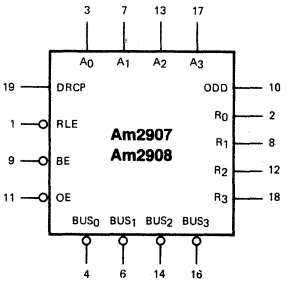
The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the A_i data into this driver register on the LOW-to-HIGH transition.

Data from the A input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted form driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

The Am2907 and Am2908 feature a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

The Am2907 has receiver threshold typically of 2.0V while the Am2908 threshold is typically 1.5V.

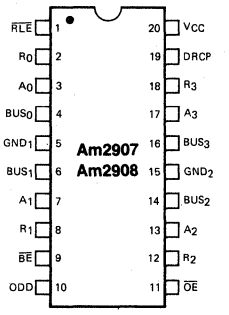
LOGIC SYMBOL



V_{CC} = Pin 20
GND_1 = Pin 5
GND_2 = Pin 15

MPR-083

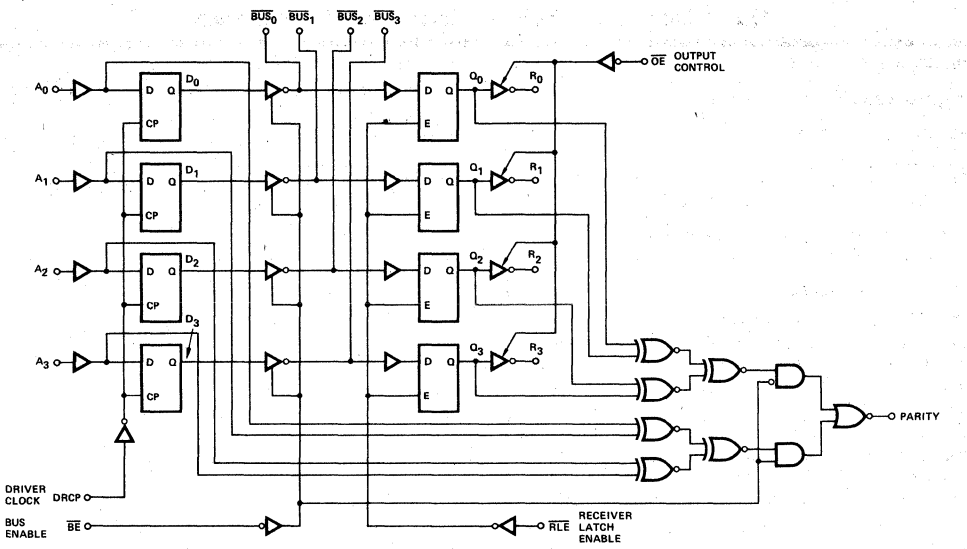
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-084

LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs (Except BUS)	30 mA
DC Output Current, Into Bus	200 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2907XC, Am2908XC (COM'L) T_A = 0°C to +70°C V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V
Am2907XM, Am2908XM (MIL) T_A = −55°C to +125°C V_{CC} MIN. = 4.50V V_{CC} MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.	V_O = 0.4V				−50	μA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power Off)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input HIGH Threshold	Bus Enable = 2.4V	Am2907	MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
			Am2908	MIL	1.9	1.5		
				COM'L	1.7	1.5		
V_{TL}	Receiver Input LOW Threshold	Bus Enable = 2.4V	Am2907	MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	
			Am2908	MIL		1.5	1.1	
				COM'L		1.5	1.3	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2907XC, Am2908XC (COM'L) T_A = 0°C to +70°C V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V

Am2907XM, Am2908XM (MIL) T_A = −55°C to +125°C V_{CC} MIN. = 4.50V V_{CC} MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN. V_{IN} = V_{IL} or V_{IH}	MIL: I_{OH} = −1mA		2.4	3.4		Volts
			COM'L: I_{OH} = −2.6mA		2.4	3.4		
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −660μA V_{IN} = V_{IH} or V_{IL}		MIL	2.5	3.4		Volts
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN. V_{IN} = V_{IL} or V_{IH}	I_{OL} = 4mA			0.27	0.4	Volts
			I_{OL} = 8mA			0.32	0.45	
			I_{OL} = 12mA			0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4 V					−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7 V					20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 5.5 V					100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.			−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All Inputs = GND		Am2907		75	110	mA
				Am2908		80	120	
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX.	V_O = 2.4 V				20	μA
			V_O = 0.4 V				−20	

Am2907 SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2907XM Min.	Am2907XM Typ. (Note 2)	Am2907XM Max.	Am2907XC Min.	Am2907XC Typ. (Note 2)	Am2907XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF R_L (BUS) = 50Ω		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_s	Data Inputs	C_L = 15pF R_L = 2.0kΩ	18			15			ns
t_h			8.0			7.0			
t_{PW}	Clock Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	37		18	34	ns
t_{PHL}				18	37		18	34	
t_{PLH}	Latch Enable to Receiver Output			21	37		21	34	ns
t_{PHL}				21	37		21	34	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{PLH}	Data to Odd Parity Out (Driver Enabled)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Bus to Odd Parity Out (Driver Inhibit)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{ZH}	Output Control to Output			14	28		14	25	ns
t_{ZL}				14	28		14	25	
t_{HZ}	Output Control to Output	C_L = 5.0pF R_L = 2.0kΩ		14	28		14	25	ns
t_{LZ}				14	28		14	25	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Am2907/2908
Am2908 SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2908XM Min.	Am2908XM Typ. (Note 2)	Am2908XM Max.	Am2908XC Min.	Am2908XC Typ. (Note 2)	Am2908XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L(BUS) = 50pF, R_L(BUS): 91Ω to V_{CC}, 200Ω to GND		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_r	Bus Output Rise Time		5	10		7	10		ns
t_f	Bus Output Fall Time		3	6		4	6		
t_s	Data Inputs		18			15			ns
t_h			8.0			7.0			
t_{PW}	Clock Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)	C_L = 50pF, R_L = 2.0kΩ		18	38		18	35	ns
t_{PHL}				18	38		18	35	
t_{PLH}	Latch Enable to Receiver Output			21	38		21	35	ns
t_{PHL}				21	38		21	35	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{PLH}	Data to Odd Parity Out (Driver Enabled)	C_L = 15pF, R_L = 2.0kΩ		21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Bus to Odd Parity Out (Driver Inhibit)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{ZH}	Output Control to Output			14	28		14	25	ns
t_{ZL}				14	28		14	25	
t_{HZ}	Output Control to Output	C_L = 5.0pF, R_L = 2.0kΩ		14	28		14	25	ns
t_{LZ}				14	28		14	25	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics fo the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

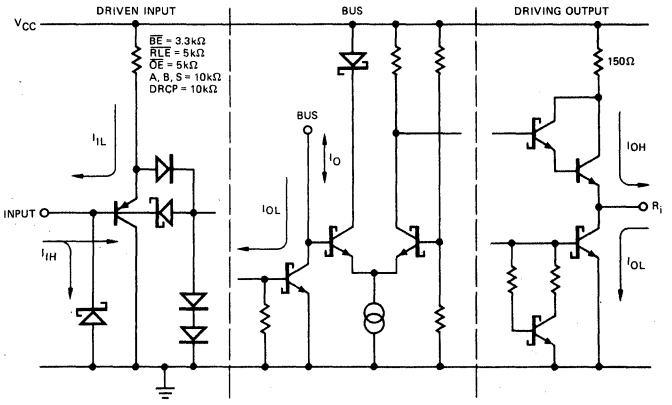
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2907 Order Number	Am2908 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2907PC	AM2908PC	P-20	C	C-1
AM2907DC	AM2908DC	D-20	C	C-1
AM2907DC-B	AM2908DC-B	D-20	C	B-1
AM2907DM	AM2908DM	D-20	M	C-3
AM2907DM-B	AM2908DM-B	D-20	M	B-3
AM2907FM	AM2908FM	F-20	M	C-3
AM2907FM-B	AM2908FM-B	F-20	M	B-3
AM2907XC	AM2908XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2907XM	AM2908XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = −55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C, Level B-3 conforms to MIL-STD-883, Class B.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



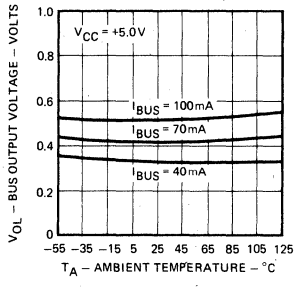
Note: Actual current flow direction shown.

MPR-086

5

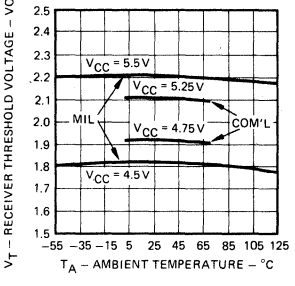
TYPICAL PERFORMANCE CURVES

Bus Output Low Voltage Versus Ambient Temperature



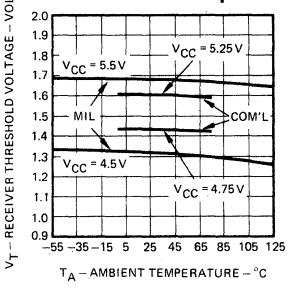
MPR-087

Am2907 Receiver Threshold Variation Versus Ambient Temperature



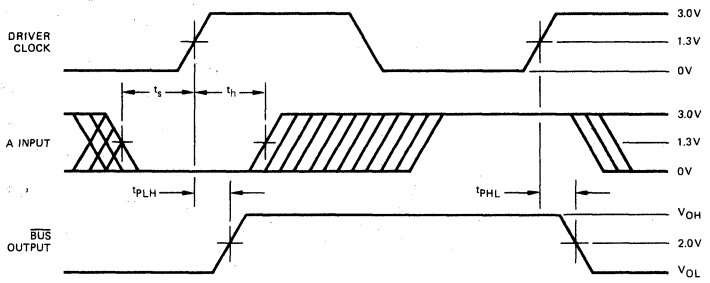
MPR-088

Am2908 Receiver Threshold Variation Versus Ambient Temperature



MPR-508

Am2907/08 SWITCHING WAVEFORMS



1. INPUT SET-UP AND HOLD TIMES.

MPR-089

TRUTH TABLE

INPUTS					INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
A_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	B_i	R_i	
X	X	H	X	X	X	X	H	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	H	L	L	X	H	H	L	
X	X	X	H	X	X	NC	X	X	Latch received data
L	↑	X	X	X	L	X	X	X	Load driver register
H	↑	X	X	X	H	X	X	X	
X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	H	X	X	X	NC	X	X	X	
X	X	L	X	X	L	X	H	X	Drive Bus
X	X	L	X	X	H	X	L	X	

H = HIGH Z = High Impedance X = Don't Care i = 0, 1, 2, 3
L = LOW NC = No Change ↑ = LOW-to-HIGH Transition

PARITY OUTPUT FUNCTION TABLE

$\overline{BE}$	ODD PARITY OUTPUT
L	ODD = $A_0 \oplus A_1 \oplus A_2 \oplus A_3$
H	ODD = $Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$

DEFINITION OF FUNCTIONAL TERMS

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

BUS_0, BUS_1, BUS_2, BUS_3 The four driver outputs and receiver inputs (data is inverted).

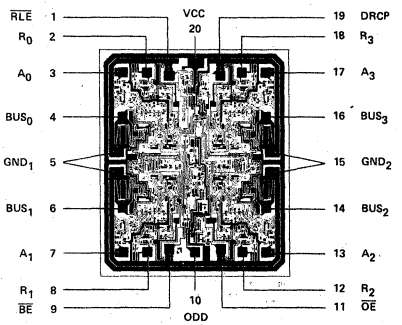
R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

ODD Odd parity output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.

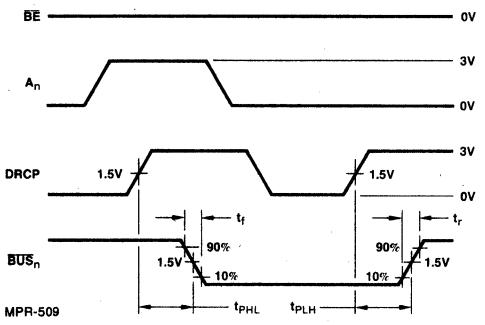
$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three-state receiver outputs are in the high-impedance state.

Metallization and Pad Layout

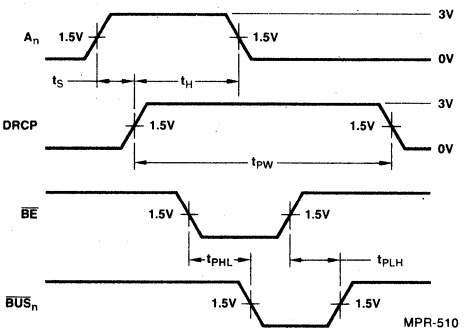


DIE SIZE 0.088" X 0.103"

Am2907/08 SWITCHING WAVEFORMS AND LOAD TEST CIRCUITS

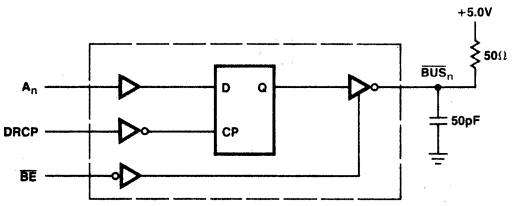


2. DRIVER CLOCK (DRCP) TO BUS

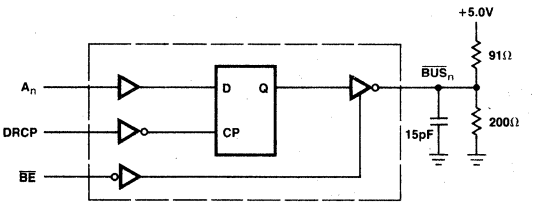


3. BUS ENABLE ($\overline{BE}$) TO BUS

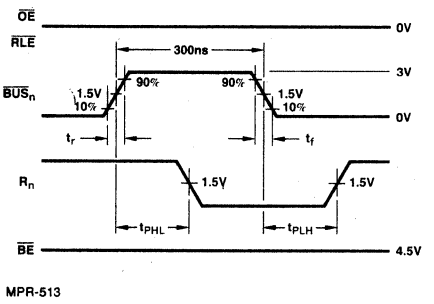
DRIVER SWITCHING WAVEFORMS



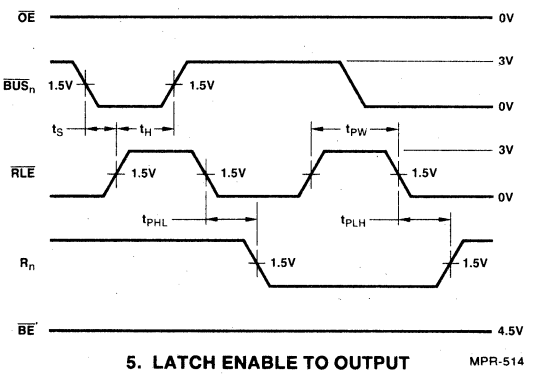
Am2907
DRIVER LOAD TEST CIRCUIT



Am2908
DRIVER LOAD TEST CIRCUIT

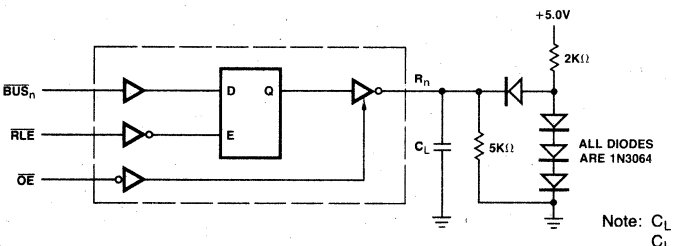


4. BUS TO RECEIVER OUTPUT (LATCH ENABLED)



5. LATCH ENABLE TO OUTPUT

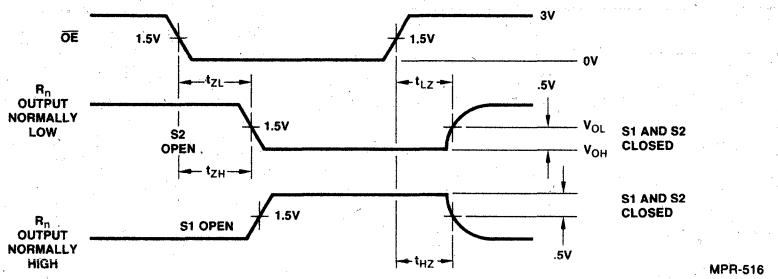
RECEIVER SWITCHING WAVEFORMS



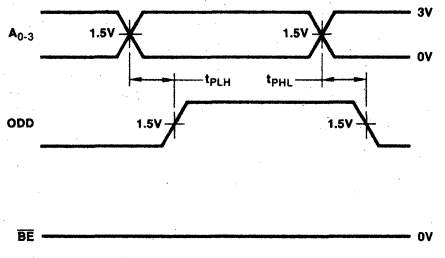
Note: C_L = 15pF for Am2907
C_L = 50pF for Am2908

Am2907/08 RECEIVER LOAD TEST CIRCUIT.

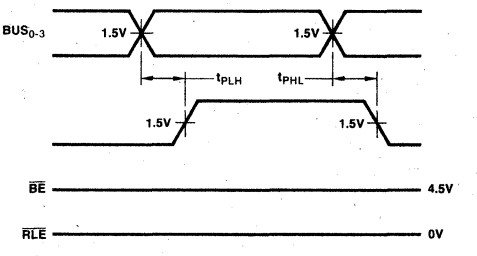
Am2907/08 SWITCHING WAVEFORMS AND LOAD TEST CIRCUITS (Cont.)



6. RECEIVER TRI-STATE WAVEFORMS

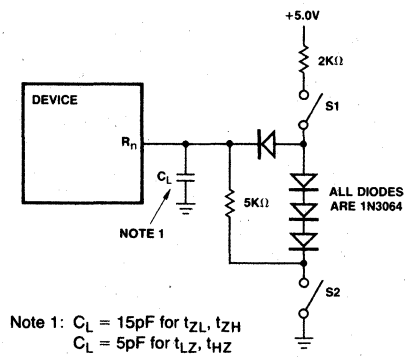


7. A INPUT TO PARITY OUTPUT

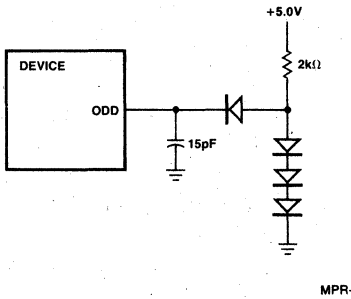


8. BUS TO PARITY OUTPUT

ODD PARITY OUTPUT WAVEFORMS

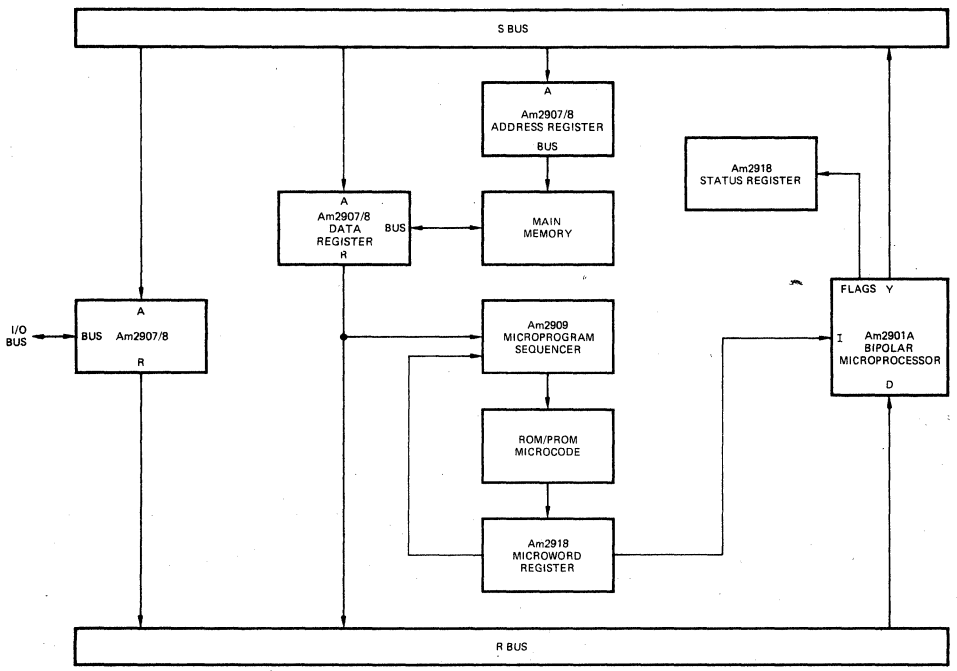


LOAD FOR RECEIVER TRI-STATE TEST



LOAD FOR PARITY OUTPUT

APPLICATIONS



The Am2907 can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high-speed Microprocessor Systems.

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5

Am2909 • Am2911
Am2909A • Am2911A
Microprogram Sequencers

DISTINCTIVE CHARACTERISTICS

- 4-bit slice cascadable to any number of microwords
- Internal address register
- Branch input for N-way branches
- Cascadable 4-bit microprogram counter
- 4 x 4 file with stack pointer and push pop control for nesting microsubroutines
- Zero input for returning to the zero microcode word
- Individual OR input for each bit for branching to higher microinstructions (Am2909 only)
- Three-state outputs
- All internal registers change state on the LOW-to-HIGH transition of the clock
- Am2909 in 28-pin package
- Am2911 in 20-pin package
- New high-speed versions (Am2909A and Am2911A) are plug-in replacements for original Am2909 and Am2911 with critical path speeds improved by about 25%

GENERAL DESCRIPTION

The Am2909 is a four-bit wide address controller intended for sequencing through a series of microinstructions contained in a ROM or PROM. Two Am2909's may be interconnected to generate an eight-bit address (256 words), and three may be used to generate a twelve-bit address (4K words).

The Am2909 can select an address from any of four sources. They are: 1) a set of external direct inputs (D); 2) external data from the R inputs, stored in an internal register; 3) a four-word deep push/pop stack; or 4) a program counter register (which usually contains the last address plus one). The push/pop stack includes certain control lines so that it can efficiently execute nested subroutine linkages. Each of the four outputs can be OR'ed with an external input for conditional skip or branch instructions, and a separate line forces the outputs to all zeroes. The outputs are three-state.

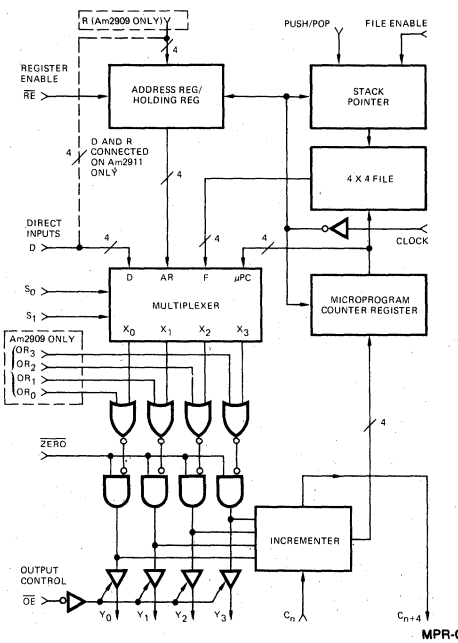
The Am2911 is an identical circuit to the Am2909, except the four OR inputs are removed and the D and R inputs are tied together. The Am2911 is in a 20-pin, 0.3" centers package. The Am2909A and Am2911A are direct plug-in replacements for the Am2909 and Am2911, but are about 25% faster.

RELATED PRODUCTS

Part No.	Description
Am2918	Pipeline Register
Am2922	Condition Code MUX
Am29803A	16-Way Branch Control Unit
Am29811A	Next Address Control
Am25LS163	4-Bit Counter
Am27S35	Registered PROM

For applications information, see Chapter II of **Bit Slice Microprocessor Design**, Mick & Brick, McGraw Hill Publications.

MICROPROGRAM SEQUENCER BLOCK DIAGRAM



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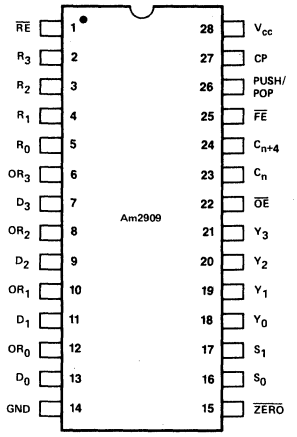
CONNECTION DIAGRAMS – Top Views

P-28, D-28



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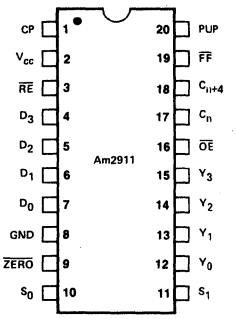
P-20, D-20



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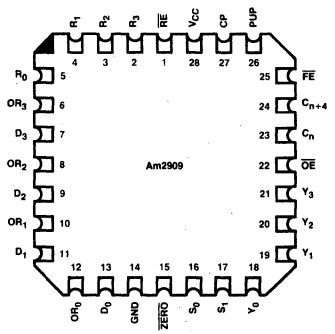
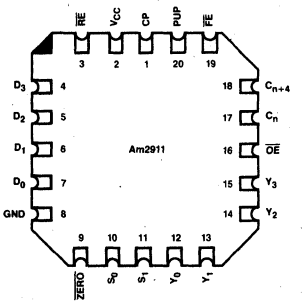
Note: Pin 1 is marked for orientation.

LEADLESS CHIP CARRIERS

L-28-1



L-20-1



ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2911 Order Number	Am2911A Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2911PC	AM2911APC	P-20	C	C-1
AM2911DC	AM2911ADC	D-20	C	C-1
AM2911DC-B	AM2911ADC-B	D-20	C	B-2 (Note 4)
AM2911DM	AM2911ADM	D-20	M	C-3
AM2911DM-B	AM2911ADM-B	D-20	M	B-3
AM2911FM	AM2911AFM	F-20-1	M	C-3
AM2911FM-B	AM2911AFM-B	F-20-1	M	B-3
AM2911LC	AM2911ALC	L-20-1	C	C-1
AM2911LM	AM2911ALM	L-20-1	M	C-3
AM2911LM-B	AM2911ALM-B	L-20-1	M	B-3
AM2911XC	AM2911AXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2911XM	AM2911AXM	Dice	M	

Am2909 Order Number	Am2909A Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2909PC	AM2909APC	P-28	C	C-1
AM2909DC	AM2909ADC	D-28	C	C-1
AM2909DC-B	AM2909ADC-B	D-28	C	B-2 (Note 4)
AM2909DM	AM2909ADM	D-28	M	C-3
AM2909DM-B	AM2909ADM-B	D-28	M	B-3
AM2909FM	AM2909AFM	F-28-1	M	C-3
AM2909FM-B	AM2909AFM-B	F-28-1	M	B-3
AM2909LC	AM2909ALC	L-28-1	C	C-1
AM2909LM	AM2909ALM	L-28-1	M	C-3
AM2909LM-B	AM2909ALM-B	L-28-1	M	B-3
AM2909XC	AM2909AXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2909XM	AM2909AXM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to −70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hours of burn-in.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

OPERATING RANGE

Operating Range	Part Number Suffix	Power Supply	Temperature Range
Commercial	PC, DC	5.0V ±5%	T_A = 0°C to +70°C
Military	DM, FM	5.0V ±10%	T_C = −55°C to +125°C

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Notes)

(For Am2909, Am2911, Am2909A, Am2911A)

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	MIL	I_{OH} = −1.0mA	2.4			Volts
			COM'L	I_{OH} = −2.6mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA, 2909/11				0.4	Volts
			I_{OL} = 8.0mA, 2909/11				0.45	
			I_{OL} = 12mA, 2909/11 (Note 5)				0.5	
			I_{OL} = 16mA, 2909A/11A				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL, 2909/11			0.7	Volts
				All others			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	C_n				−1.08	mA
			Push/Pop, $\overline{OE}$				−0.72	
			Others (Note 6)				−0.36	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	C_n				40	μA
			Push/Pop				40	
			Others (Note 6)				20	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V	C_n, Push/Pop				0.2	mA
			Others (Note 6)				0.1	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = 6V, V_{OUT} = .5V		$Y_0 - Y_3$	−30		−100	mA
				$C_n + 4$	−30		−85	
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 4)	COM'L and MIL	T_A = +25°C			130	mA
			COM'L Only	T_A = 0 to +70°C			130	
			MIL Only	T_C = −55 to +125°C			140	
				T_C = +125°C			110	
I_{OZL}	Output OFF Current	V_{CC} = MAX., $\overline{OE}$ = 2.7 V	Y_{0-3}	V_{OUT} = 0.4 V			−20	μA
I_{OZH}				V_{OUT} = 2.7 V			20	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Apply GND to C_n, R_0, R_1, R_2, R_3, OR_0, OR_1, OR_2, OR_3, D_0, D_1, D_2, and D_3. Other inputs high. All outputs open. Measured after a LOW-to-HIGH clock transition.
5. The 12mA guarantee applies only to Y_0, Y_1, Y_2 and Y_3.
6. For the Am2911 and Am2911A, D_i and R_i are internally connected. Loading is doubled (to same values as Push/Pop).

Am2909A/Am2911A SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Tables I, II and III below define the timing characteristics of the Am2909A/Am2911A over the operating voltage and temperature range. The tables are divided into three types of parameters; clock characteristics, combinational delays from inputs to outputs, and set-up and hold time requirements. The latter table defines the time prior to the end of the cycle (i.e., clock LOW-to-HIGH transition) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level. All outputs have maximum DC loading. The data on this page applies to the following part numbers:

Operating Range	Part Numbers	Power Supply	Temperature Range
Com'l	Am2909APC, DC Am2911APC, DC	5.0V ±5%	T_A = 0°C to +70°C
Mil	Am2909ADM, FM Am2911ADM	5.0V ±10%	T_C = −55°C to +125°C

TABLE I
CYCLE TIME AND CLOCK CHARACTERISTICS

Time	COMMERCIAL	MILITARY
Minimum Clock LOW Time	20	20
Minimum Clock HIGH Time	20	20

TABLE II
MAXIMUM COMBINATIONAL PROPAGATION DELAYS
(all in ns, C_L = 50pF (except output disable tests))

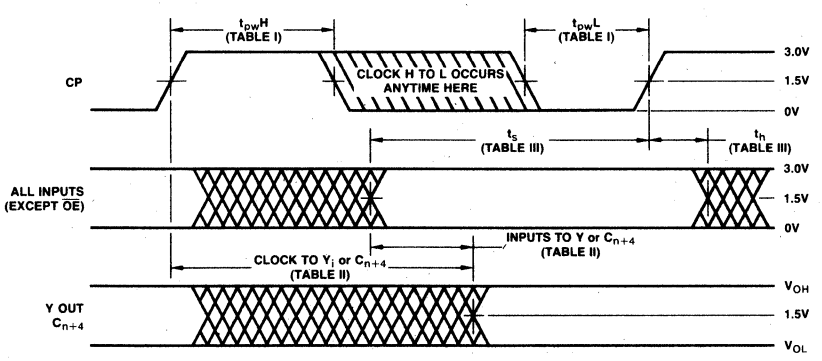
	COMMERCIAL		MILITARY	
From Input	Y	C_{n+4}	Y	C_{n+4}
D_i	17	22	20	25
S_0, S_1	29	34	29	34
OR_i	17	22	20	25
C_n	–	14	–	16
$\overline{ZERO}$	29	34	30	35
OE LOW (enable)	25	–	25	–
OE HIGH (disable)*	25	–	25	–
Clock ↑ S_1S_0 = LH	39	44	45	50
Clock ↑ S_1S_0 = LL	39	44	45	50
Clock ↑ S_1S_0 = HL	44	49	53	58

*C_L = 5pF

TABLE III
GUARANTEED SET-UP AND HOLD TIMES (all in ns) (Note 1)

From Input	Notes	COMMERCIAL		MILITARY	
		Set-Up Time	Hold Time	Set-Up Time	Hold Time
$\overline{RE}$		19	4	19	5
R_i	2	10	4	12	5
PUSH/POP		25	4	27	5
FE		25	4	27	5
C_n		18	4	18	5
D_i		25	0	25	0
OR_i		25	0	25	0
S_0, S_1		25	0	29	0
$\overline{ZERO}$		25	0	29	0

Notes: 1. All times relative to clock LOW-to-HIGH transition.
2. On Am2911A, R_i and D_i are internally connected and labeled D_i. Use R_i set-up and hold times when D inputs are used to load register.



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Am2909/09A/11/11A
Am2909 and Am2911
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Tables I, II, and III below define the timing characteristics of the Am2909 and Am2911 over the operating voltage and temperature range. The tables are divided into three types of parameters; clock characteristics, combinational delays from inputs to outputs, and set-up and hold time requirements. The latter table defines the time prior to the end of the cycle (i.e. clock LOW-to-HIGH transition) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level. All outputs have maximum DC loading. The data on this page applies to the following part numbers:

Operating Range	Part Numbers	Power Supply	Temperature Range
Com'l	Am2909PC, DC Am2911PC, DC	5.0V ±5%	T_A = 0°C to +70°C
Mil	Am2909DM, FM Am2911DM	5.0V ±10%	T_C = −55°C to +125°C

TABLE I
CYCLE TIME AND CLOCK CHARACTERISTICS

TIME	COMMERCIAL	MILITARY
Minimum Clock LOW Time	30	35
Minimum Clock HIGH Time	30	35

TABLE II
MAXIMUM COMBINATIONAL PROPAGATION DELAYS
(all in ns, C_L = 50pF (except output disable tests))

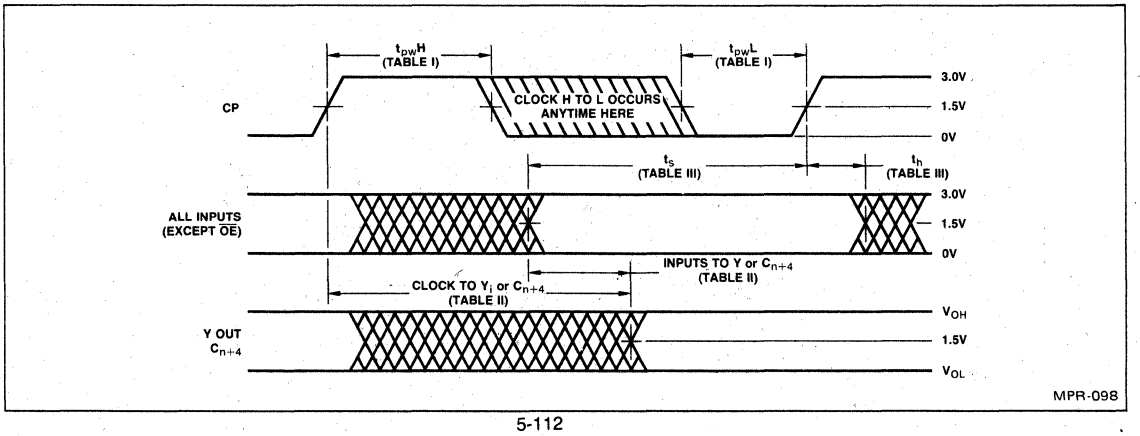
From Input	COMMERCIAL		MILITARY	
	Y	C_{n+4}	Y	C_{n+4}
D_i	17	30	20	32
S_0, S_1	30	48	40	50
OR_i	17	30	20	32
C_n	–	14	–	16
$\overline{ZERO}$	30	48	40	50
$\overline{OE}$ LOW (enable)	25	–	25	–
$\overline{OE}$ HIGH (disable)*	25	–	25	–
Clock ↑ S_1S_0 = LH	43	55	50	62
Clock ↑ S_1S_0 = LL	43	55	50	62
Clock ↑ S_1S_0 = HL	80	95	90	102

*C_L = 5.0pF

TABLE III
GUARANTEED SET-UP AND HOLD TIMES (all in ns) (Note 1)

From Input	Notes	COMMERCIAL		MILITARY	
		Set-Up Time	Hold Time	Set-Up Time	Hold Time
$\overline{RE}$		22	5	22	5
R_i	2	10	5	12	5
PUSH/POP		26	6	30	7
$\overline{FE}$		26	5	30	5
C_n		28	5	30	5
D_i		30	0	35	3
OR_i		30	0	35	3
S_0, S_1		45	0	50	0
$\overline{ZERO}$		45	0	50	0

Notes: 1. All times relative to clock LOW-to-HIGH transition.
2. On Am2911, R_i and D_i are internally connected together and labeled D_i. Use R_i set-up and hold times when D inputs are used to load register.



OPERATION OF THE Am2909/Am2911

Figure 5 lists the select codes for the multiplexer. The two bits applied from the microword register (and additional combinational logic for branching) determine which data source contains the address for the next microinstruction. The contents of the selected source will appear on the Y outputs. Figure 5 also shows the truth table for the output control and for the control of the push/pop stack. Figure 6 shows in detail the effect of S_0, S_1, $\overline{FE}$ and PUP on the Am2909. These four signals define what address appears on the Y outputs and what the state of all the internal registers will be following the clock LOW-to-HIGH edge. In this illustration, the microprogram counter is assumed to contain initially some word J, the address register some word K, and the four words in the push/pop stack contain R_a through R_d.

Address Selection

OCTAL	S_1	S_0	SOURCE FOR Y OUTPUTS	SYMBOL
0	L	L	Microprogram Counter	μPC
1	L	H	Address/Holding Register	AR
2	H	L	Push-Pop stack	STK0
3	H	H	Direct inputs	D_i

Output Control

OR_i	$\overline{ZERO}$	$\overline{OE}$	Y_i
X	X	H	Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S_0 S_1

Z = High Impedance

Synchronous Stack Control

$\overline{FE}$	PUP	PUSH-POP STACK CHANGE
H	X	No change
L	H	Increment stack pointer, then push current PC onto STK0
L	L	Pop stack (decrement stack pointer)

H = High
L = Low
X = Don't Care

Figure 5.

CYCLE	S_1, S_0, $\overline{FE}$, PUP	μPC	REG	STK0	STK1	STK2	STK3	Y_{OUT}	COMMENT	PRINCIPLE USE
N	0 0 0 0	J	K	Ra	Rb	Rc	Rd	J	Pop Stack	End
N+1	–	J+1	K	Rb	Rc	Rd	Ra	–		Loop
N	0 0 0 1	J	K	Ra	Rb	Rc	Rd	J	Push μPC	Set-up
N+1	–	J+1	K	J	Ra	Rb	Rc	–		Loop
N	0 0 1 X	J	K	Ra	Rb	Rc	Rd	J	Continue	Continue
N+1	–	J+1	K	Ra	Rb	Rc	Rd	–		
N	0 1 0 0	J	K	Ra	Rb	Rc	Rd	K	Pop Stack;	End
N+1	–	K+1	K	Rb	Rc	Rd	Ra	–	Use AR for Address	Loop
N	0 1 0 1	J	K	Ra	Rb	Rc	Rd	K	Push μPC;	JSR AR
N+1	–	K+1	K	J	Ra	Rb	Rc	–	Jump to Address in AR	
N	0 1 1 X	J	K	Ra	Rb	Rc	Rd	K	Jump to Address in AR	JMP AR
N+1	–	K+1	K	Ra	Rb	Rc	Rd	–		
N	1 0 0 0	J	K	Ra	Rb	Rc	Rd	Ra	Jump to Address in STK0;	RTS
N+1	–	Ra+1	K	Rb	Rc	Rd	Ra	–	Pop Stack	
N	1 0 0 1	J	K	Ra	Rb	Rc	Rd	Ra	Jump to Address in STK0;	
N+1	–	Ra+1	K	J	Ra	Rb	Rc	–	Push μPC	
N	1 0 1 X	J	K	Ra	Rb	Rc	Rd	Ra	Jump to Address in STK0	Stack Ref
N+1	–	Ra+1	K	Ra	Rb	Rc	Rd	–		(Loop)
N	1 1 0 0	J	K	Ra	Rb	Rc	Rd	D	Pop Stack;	End
N+1	–	D+1	K	Rb	Rc	Rd	Ra	–	Jump to Address on D	Loop
N	1 1 0 1	J	K	Ra	Rb	Rc	Rd	D	Jump to Address on D;	JSR D
N+1	–	D+1	K	J	Ra	Rb	Rc	–	Push μPC	
N	1 1 1 X	J	K	Ra	Rb	Rc	Rd	D	Jump to Address on D	JMP D
N+1	–	D+1	K	Ra	Rb	Rc	Rd	–		

X = Don't care, 0 = LOW, 1 = HIGH, Assume C_n = HIGH
Note: STK0 is the location addressed by the stack pointer.

Figure 6. Output and Internal Next-Cycle Register States for Am2909/Am2911.

Figure 7 illustrates the execution of a subroutine using the Am2909. The configuration of Figure 3 is assumed. The instruction being executed at any given time is the one contained in the microword register (μWR). The contents of the μWR also controls (indirectly, perhaps) the four signals S_0, S_1, $\overline{FE}$, and PUP. The starting address of the subroutine is applied to the D inputs of the Am2909 at the appropriate time.

In the columns on the left is the sequence of microinstructions to be executed. At address J+2, the sequence control portion of the microinstruction contains the comand "Jump to subroutine at A". At the time T_2, this instruction is in the μWR, and the Am2909 inputs are set-up to execute the jump and save the return address. The subroutine address A is applied to the D inputs from the μWR and appears on the Y outputs. The first instruction of the subroutine, I(A), is accessed and is at the inputs of the μWR. On the next clock transition, I(A) is loaded into the μWR for execution, and the return address J+3 is pushed onto the stack. The return instruction is executed at T_5. Figure 8 is a similar timing chart showing one subroutine linking to a second, the latter consisting of only one microinstruction.

CONTROL MEMORY

Execute Cycle	Microprogram Address	Microprogram Sequencer Instruction
	J−1	–
T_0	J	–
T_1	J+1	–
T_2	J+2	JSR A
T_6	J+3	–
T_7	J+4	–
	–	–
	–	–
	–	–
	–	–
	–	–
T_3	A	I(A)
T_4	A+1	–
T_5	A+2	RTS
	–	–
	–	–
	–	–
	–	–
	–	–
	–	–
	–	–

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Clock											
Signals											
Am2909 Inputs (from μWR)	S_1, S_0	0	0	3	0	0	2	0	0		
	$\overline{FE}$	H	H	L	H	H	L	H	H		
	PUP	X	X	H	X	X	L	X	X		
	D	X	X	A	X	X	X	X	X		
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	J+4	J+5		
	STK0	–	–	–	J+3	J+3	J+3	–	–		
	STK1	–	–	–	–	–	–	–	–		
	STK2	–	–	–	–	–	–	–	–		
	STK3	–	–	–	–	–	–	–	–		
Am2909 Output	Y	J+1	J+2	A	A+1	A+2	J+3	J+4	J+5		
ROM Output	(Y)	I(J+1)	**JSR A**	I(A)	I(A+1)	**RTS**	I(J+3)	I(J+4)	I(J+5)		
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J+1)	**JSR A**	I(A)	I(A+1)	**RTS**	I(J+3)	I(J+4)		

Figure 7. Subroutine Execution. C_n = HIGH

CONTROL MEMORY

Execute Cycle	Microprogram Address	Microprogram Sequencer Instruction
	J−1	–
T_0	J	–
T_1	J+1	–
T_2	J+2	JSR A
T_9	J+3	–
	–	–
	–	–
	–	–
	–	–
T_3	A	–
T_4	A+1	–
T_5	A+2	JSR B
T_7	A+3	–
T_8	A+4	RTS
	–	–
	–	–
	–	–
	–	–
T_6	B	RTS
	–	–
	–	–

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Clock											
Signals											
Am2909 Inputs (from μWR)	S_1, S_0	0	0	3	0	0	3	2	0	2	0
	$\overline{FE}$	H	H	L	H	H	L	L	H	L	H
	PUP	X	X	H	X	X	H	L	X	L	X
	D	X	X	A	X	X	B	X	X	X	X
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	B+1	A+4	A+5	J+4
	STK0	–	–	–	J+3	J+3	J+3	A+3	J+3	J+3	–
	STK1	–	–	–	–	–	–	J+3	–	–	–
	STK2	–	–	–	–	–	–	–	–	–	–
	STK3	–	–	–	–	–	–	–	–	–	–
Am2909 Output	Y	J+1	J+2	A	A+1	A+2	B	A+3	A+4	J+3	J+4
ROM Output	(Y)	I(J+1)	**JSR A**	I(A)	I(A+1)	**JSR B**	**RTS**	I(A+3)	**RTS**	I(J+3)	I(J+4)
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J+1)	**JSR A**	I(A)	I(A+1)	**JSR B**	**RTS**	I(A+3)	**RTS**	I(J+3)

Figure 8. Two Nested Subroutines. Routine B is Only One Instruction. C_n = HIGH

USING THE Am2909 AND Am2911

The Am2909 and Am2911 are four-bit slice sequencers which are cascaded to form a microprogram memory address generator. Both products make available to the user several lines which are used to directly control the internal holding register, multiplexer and stack. By appropriate control of these lines, the user can implement any desired set of sequence control functions; by cascading parts he can generate any desired address length. These two qualities set the Am2909 and Am2911 apart from the Am2910, which is architecturally similar, but is fixed at 12 bits in length and has a fixed set of 16 sequence control instructions. The Am2909 or Am2911 should be selected instead of the Am2910 under the following conditions:

- Address less than 8 bits and not likely to be expanded
- Address longer than 12 bits
- More complex instruction set needed than is available on Am2910

Architecture of the Control Unit

The recommended architecture using the Am2909 or Am2911 is shown in Figure 1. Note that the path from the pipeline register output through the next address logic, multiplexer, and microprogram memory is all combinational. The pipeline register contains the current microinstruction being executed. A portion of that microinstruction consists of a sequence control command such as "continue", "loop", "return-from-subroutine", etc. The bits representing this sequence command are logically combined with bits representing such things as test conditions and system state to generate the required control signals to the Am2909 or Am2911. The block labeled "next address logic" may consist of simple gates, a PROM or a PLA, but it should be all combinational.

5

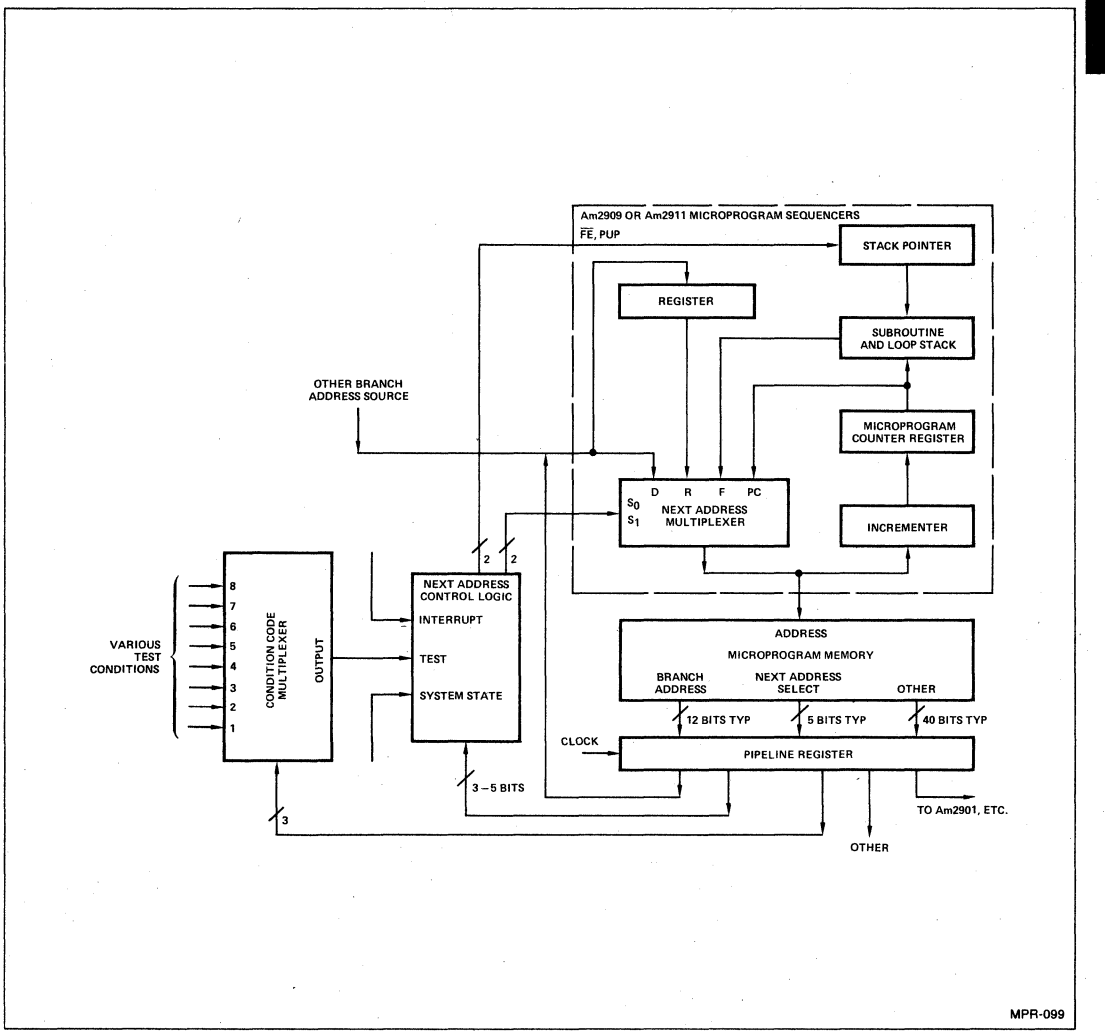


Figure 1. Recommended Computer Control Unit Architecture Using the Am2911 or Am2909.

The Am29811A is a combinational circuit which implements 16 sequence control instructions; it may be used with either an Am2909 or an Am2911. The set of instructions is nearly identical to that implemented internally in the Am2910.

Figure 2 shows the CCU of Figure 1 with the Am29811A in place. The Am29811A, in addition to controlling the Am2911, also controls a loop counter and several branch address sources. The instructions which are implemented by the Am29811A are shown in Figure 3, along with the Am29811A outputs for each instruction. Generating any instruction set consists simply of writing a truth table and designing combinational logic to implement it. For more detailed information refer to "The Microprogramming Handbook".

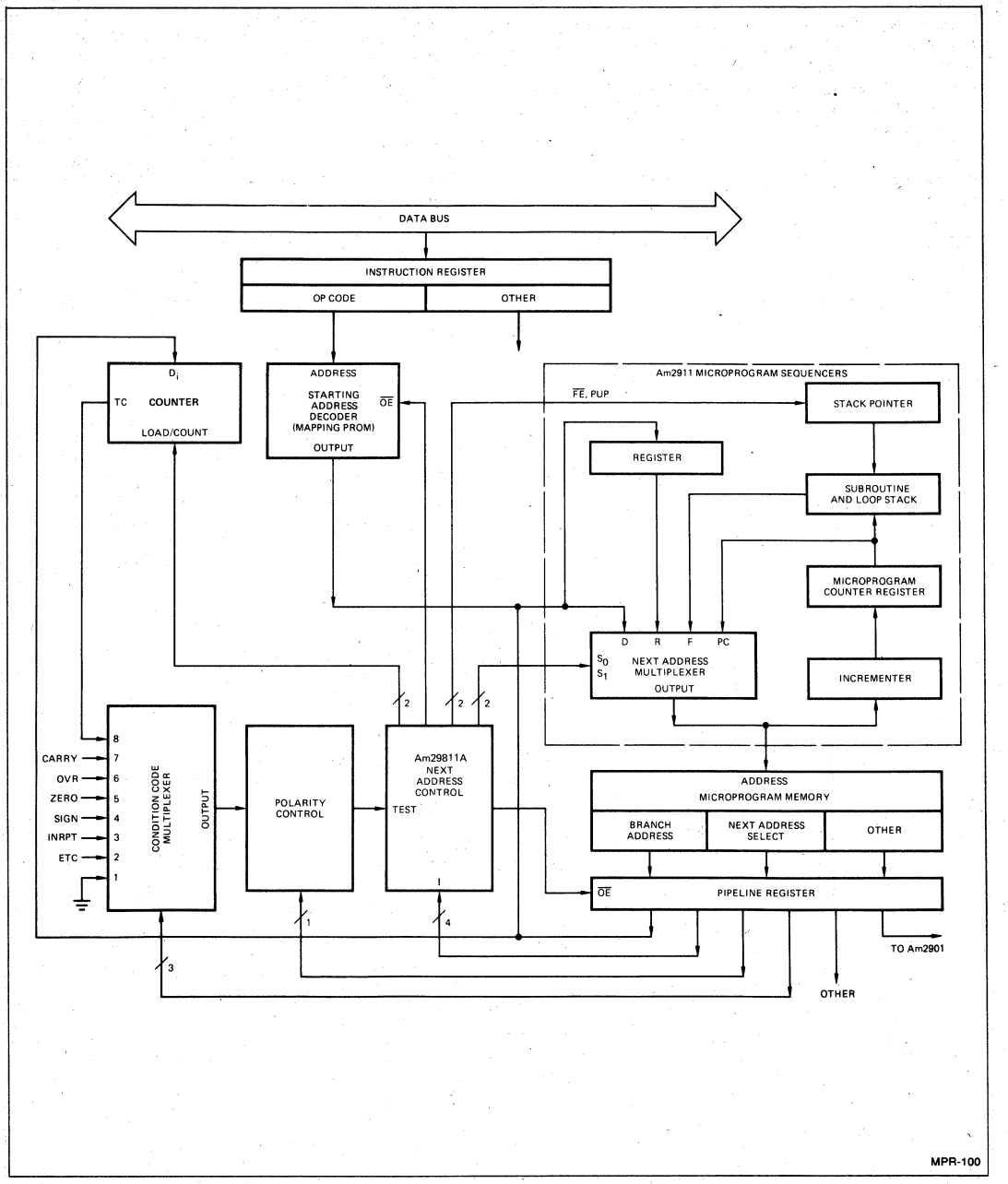


Figure 2. A Typical Computer Control Unit Using the Am2911 and Am29811A.

Expansion of the Am2909 or Am2911

Figure 4 shows the interconnection of three Am2911's to form a 12-bit sequencer. Note that the only interconnection between packages, other than the common clock and control lines, is the ripple carry between μPC incrementors. This carry path is not in the critical speed path if the Am2911 Y outputs drive the microprogram memory, because the ripple carry occurs in parallel with the memory access time. If, on the other hand, a micro-address register is placed at the Am2911 output, then the carry may lie in the critical speed path, since the last carry-in must be stable for a set-up time prior to the clock.

Selecting Between the Am2909 and Am2911

The difference between the Am2909 and the Am2911 involves two signals: the data inputs to the holding register and the "OR" inputs. In the Am2909, separate four-bit fields are provided for the holding register and the direct branch inputs to the multiplexer. In the Am2911, these fields are internally tied together. This may affect the design of the branch address system, as shown in Figure 5. Using the Am2909, the register inputs may be connected directly to the microprogram memory; the internal register replaces part of the pipeline register. The direct (D) inputs may be tied to the mapping logic which translates instruction op codes into microprogram addresses. While the same technique might be used with the Am2911, it is more common to connect the Am2911's D inputs to a branch address bus onto which various sources may be enabled. Shown in Figure 5 is a pipeline register and a mapping ROM. Other sources might also be applied to the same bus. The internal register is used only for temporary storage of some previous branch address.

5

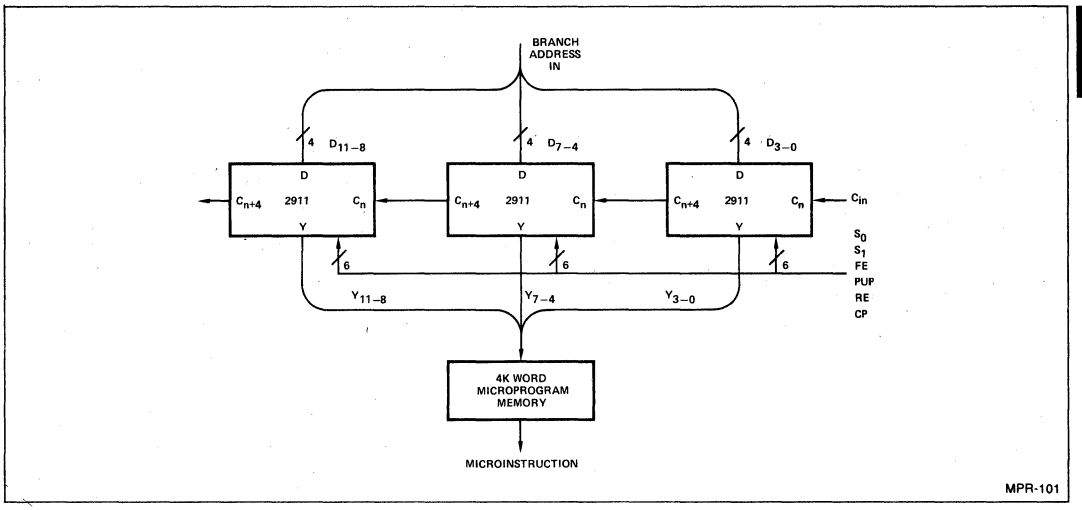


Figure 4. Twelve Bit Sequencer.

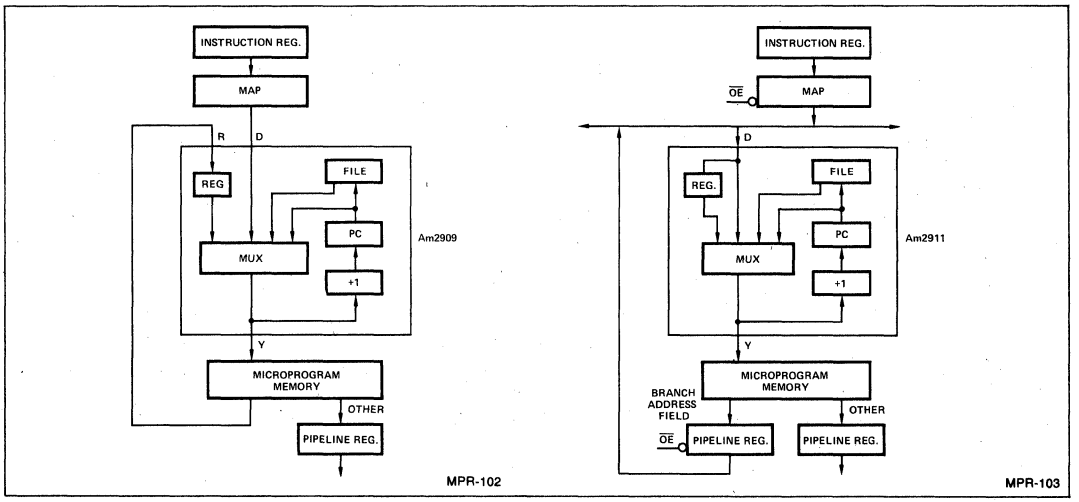


Figure 5. Branch Address Structures.

The second difference between the Am2909 and Am2911 is that the Am2909 has OR inputs available on each address output line. These pins can be used to generate multi-way single-cycle branches by simply tying several test conditions into the OR lines. See Figure 6. Typically, a branch is taken to an address with zeroes in the least significant bits. These bits are replaced with 1's or 0's by test conditions applied to the OR lines. In Figure 6, the states of the two test conditions X and Y result in a branch to 1100, 1101, 1110, or 1111.

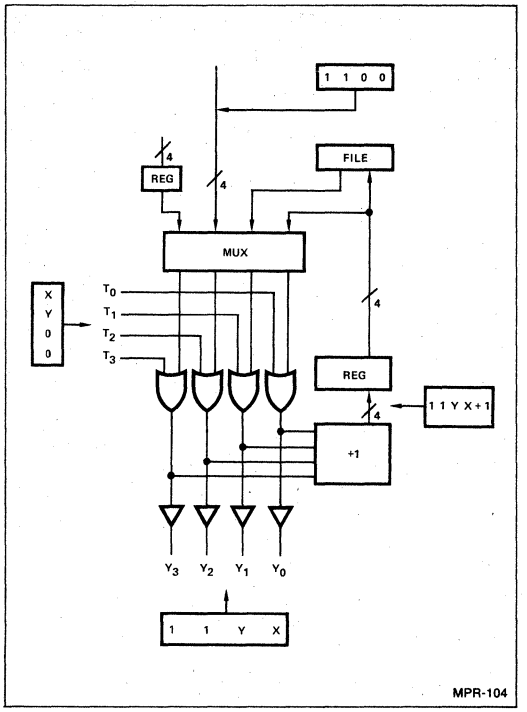


Figure 6. Use of OR Inputs to Obtain 4 - Way Branch.

The Am29803A has been designed to selectively apply any or all of four different test conditions to an Am2909. Figure 7 shows the truth table for this device. A nice trade off between flexibility and board space is achieved by using a single 28-pin Am2909 for the least significant four bits of a sequencer, and using the space-saving 20-pin Am2911's for the remainder of the bits. A detailed logic design for such a system is contained in The Microprogramming Handbook.

How to Perform Some Common Functions with the Am2909 or Am2911

1. CONTINUE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
PC	HOLD	1	0	0	1	X

Contents of PC placed on Y outputs; PC incremented.

2. BRANCH

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
D	HOLD	1	1	1	1	X

Feed data on D inputs straight through to memory address lines. Increment address and place in PC.

3. JUMP-TO-SUBROUTINE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
D	PUSH	1	1	1	0	1

Sub-routine address fed from D inputs to memory address. Current PC is pushed onto stack, where it is saved for the return.

4. RETURN-FROM-SUBROUTINE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
STACK	POP	1	1	0	0	0

The address at the top of the stack is applied to the microprogram memory, and is incremented for PC on the next cycle. The stack is popped to remove the return address.

Am29803A FUNCTION TABLE

	BRANCH ON	I_3	I_2	I_1	I_0	OR_3	OR_2	OR_1	OR_0
NONE	NONE	L	L	L	L	L	L	L	L
Two-Way Branches	T_0	L	L	L	H	L	L	L	T_0
	T_1	L	L	H	L	L	L	L	T_1
	T_2	L	H	L	L	L	L	L	T_2
	T_3	H	L	L	L	L	L	L	T_3
Four-Way Branches	T_1 & T_0	L	L	H	H	L	L	T_1	T_0
	T_2 & T_0	L	H	L	H	L	L	T_2	T_0
	T_3 & T_0	H	L	L	H	L	L	T_3	T_0
	T_2 & T_1	L	H	H	L	L	L	T_2	T_1
	T_3 & T_1	H	L	H	L	L	L	T_3	T_1
	T_3 & T_2	H	H	L	L	L	L	T_3	T_2
Eight-Way Branches	T_2, T_1, T_0	L	H	H	H	L	T_2	T_1	T_0
	T_3, T_1, T_0	H	L	H	H	L	T_3	T_1	T_0
	T_3, T_2, T_0	H	H	L	H	L	T_3	T_2	T_0
	T_3, T_2, T_1,	H	H	H	L	L	T_3	T_2	T_1
Sixteen-Way Branch	T_3, T_2, T_1, T_0	H	H	H	H	T_3	T_2	T_1	T_0

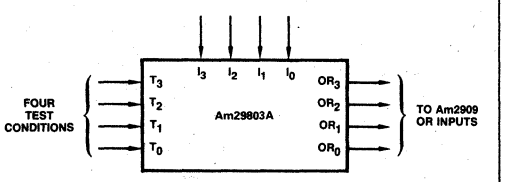
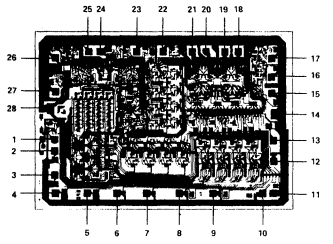


Figure 7.

Metallization and Pad Layouts

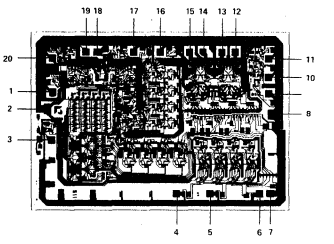
Am2909



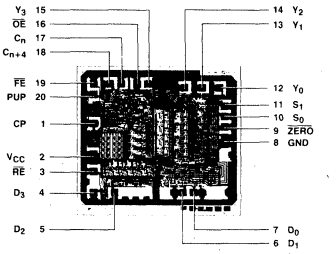
Numbers correspond to DIP pin-out

DIE SIZE 0.110" X 0.160"

Am2911



Am2911A



DIE SIZE 86 X 98 Mils

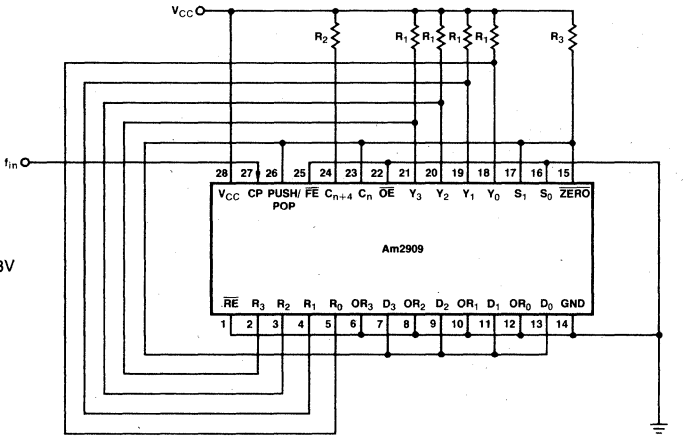
5

Burn-in Circuit for Am2909 (Flatpack and Hermetic DIP)

Notes:
Max. I_{CC} = 200mA
T_A = +125°C
Resistors = ±5%

R_1 = 390Ω
R_2 = 560Ω
R_3 = 1kΩ
f_{in} = 100kHz, 50% duty-cycle, 0-3V

V_{CC} min. = 5.0V
V_{CC} max. = 5.1V



This circuit conforms to MIL-STD-883, Method 1005 and 1015, Condition D. Parallel excitation.

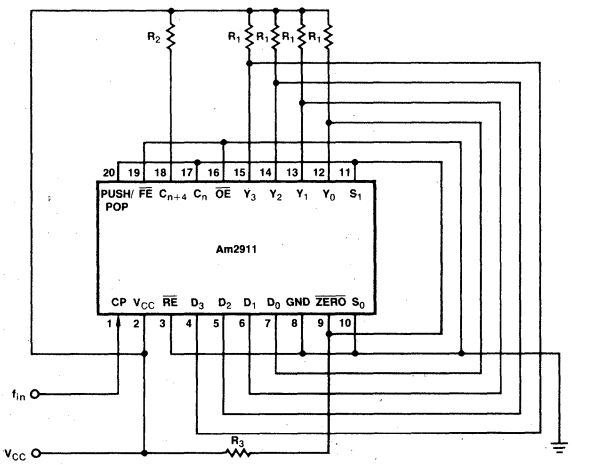
MPR-726

Burn-in Circuit for Am2911

Notes:
Max. I_{CC} = 200mA
T_A = +125°C
Resistors = ±5%

R_1 = 390Ω
R_2 = 560Ω
R_3 = 1kΩ
f_{in} = 100kHz, 50% duty-cycle, 0-3V

From clock buffer on each board:
V_{CC} min. = 5.0V
V_{CC} max. = 5.1V

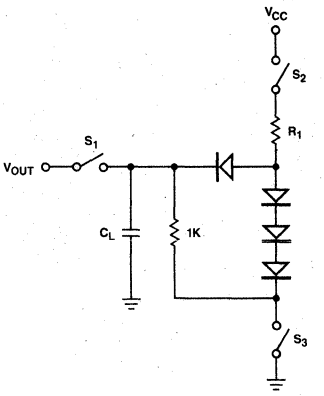


This circuit conforms to MIL-STD-883, Method 1005 and 1015, Condition D. Parallel excitation.

MPR-727

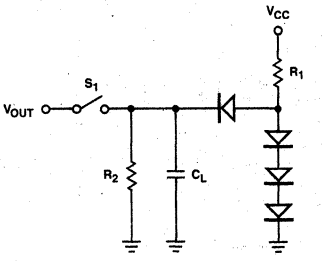
TEST OUTPUT LOAD CONFIGURATIONS FOR Am2909/2911 AND Am2909A/2911A

A. THREE-STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC test except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS

Pin # (DIP)	Pin Label	Test Circuit	Am2909		Am2909A	
			R_1	R_2	R_1	R_2
18-21	Y_{0-3}	A	300	1K	220	1K
24	C_{n+4}	B	470	2.4K	220	2.4K

TEST OUTPUT LOADS

Pin # (DIP)	Pin Label	Test Circuit	Am2911		Am2911A	
			R_1	R_2	R_1	R_2
12-15	Y_{0-3}	A	300	1K	220	1K
18	C_{n+4}	B	470	2.4K	220	2.4K

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5–8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

ARCHITECTURE OF THE Am2909/Am2911

The Am2909/Am2911 are bipolar microprogram sequencers intended for use in high-speed microprocessor applications. The device is a cascadable 4-bit slice such that two devices allow addressing of up to 256-words of microprogram and three devices allow addressing of up to 4K words of microprogram. A detailed logic diagram is shown in Figure 2.

The device contains a four-input multiplexer that is used to select either the address register, direct inputs, microprogram counter, or file as the source of the next microinstruction address. This multiplexer is controlled by the S_0 and S_1 inputs.

The address register consists of four D-type, edge triggered flip-flops with a common clock enable. When the address register enable is LOW, new data is entered into the register on the clock LOW-to-HIGH transition. The address register is available at the multiplexer as a source for the next microinstruction address. The direct input is a four-bit field of inputs to the multiplexer and can be selected as the next microinstruction address. On the Am2911, the direct inputs are also used as inputs to the register. This allows an N-way branch where N is any word in the microcode.

The Am2909/Am2911 contains a microprogram counter (μPC) that is composed of a 4-bit incrementer followed by a 4-bit register. The incrementer has carry-in (C_n) and carry-out (C_{n+4}) such that cascading to larger word lengths is straightforward. The μPC can be used in either of two ways. When the least significant carry-in to the incrementer is HIGH, the microprogram register is loaded on the next clock cycle with the current Y output word plus one (Y+1→μPC.) Thus sequential microinstructions can be executed. If this least significant C_n is LOW, the incrementer passes the Y output word unmodified and the microprogram register is loaded with the same Y word on the next clock cycle (Y→μPC). Thus, the same microinstruction can be executed any number of times by using the least significant C_n as the control.

The last source available at the multiplexer input is the 4 x 4 file (stack). The file is used to provide return address linkage when executing microsubroutines. The file contains a built-in stack pointer (SP) which always points to the last file word written. This allows stack reference operations (looping) to be performed without a push or pop.

The stack pointer operates as an up/down counter with separate push/pop and file enable inputs. When the file enable input is LOW and the push/pop input is HIGH, the PUSH operation is enabled. This causes the stack pointer to increment and the file to be written with the required return linkage — the next microinstruction address following the subroutine jump which initiated the PUSH.

If the file enable input is LOW and the push/pop control is LOW, a POP operation occurs. This implies the usage of the return linkage during this cycle and thus a return from subroutine. The next LOW-to-HIGH clock transition causes the stack pointer to decrement. If the file enable is HIGH, no action is taken by the stack pointer regardless of any other input.

The stack pointer linkage is such that any combination of pushes, pops or stack references can be achieved. One microinstruction subroutines can be performed. Since the stack is 4 words deep, up to four microsubroutines can be nested.

The ZERO input is used to force the four outputs to the binary zero state. When the ZERO input is LOW, all Y outputs are LOW regardless of any other inputs (except $\overline{OE}$). Each Y output bit also has a separate OR input such that a conditional logic one can be forced at each Y output. This allows jumping to different microinstructions on programmed conditions.

The Am2909/Am2911 feature three-state Y outputs. These can be particularly useful in military designs requiring external Ground Support Equipment (GSE) to provide automatic checkout of the microprocessor. The internal control can be placed in the high-impedance state, and preprogrammed sequences of microinstructions can be executed via external access to the control ROM/PROM.

DEFINITION OF TERMS

A set of symbols is used in this data sheet to represent various internal and external registers and signals used with the Am2909. They are:

Inputs to Am2909/Am2911

S_1, S_0	Control lines for address source selection
$\overline{FE}$, PUP	Control lines for push/pop stack
$\overline{RE}$	Enable line for internal address register
OR_i	Logic OR inputs on each address output line
$\overline{ZERO}$	Logic AND input on the output lines
$\overline{OE}$	Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF (high impedance)
C_n	Carry-in to the incrementer
R_i	Inputs to the internal address register
D_i	Direct inputs to the multiplexer
CP	Clock input to the AR and μPC register and Push-Pop stack

Outputs from the Am2909/Am2911

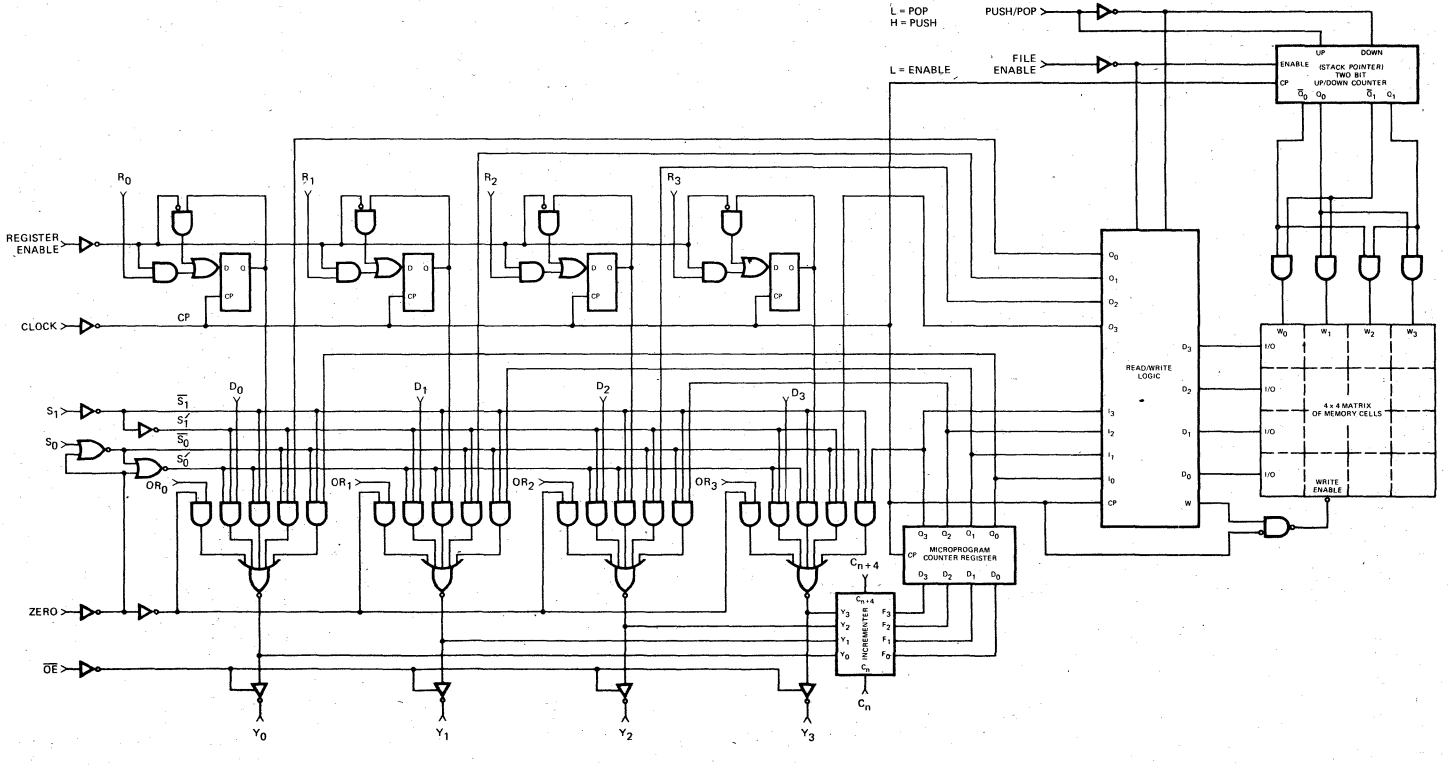
Y_i	Address outputs from Am2909. (Address inputs to control memory.)
C_{n+4}	Carry out from the incrementer

Internal Signals

μPC	Contents of the microprogram counter
AR	Contents of the address/holding register
STK0-STK3	Contents of the push/pop stack. By definition, the word in the four-by-four file, addressed by the stack pointer is STK0. Conceptually data is pushed into the stack at STK0; a subsequent push moves STK0 to STK1; a pop implies STK3 → STK2 → STK1 → STK0. Physically, only the stack pointer changes when a push or pop is performed. The data does not move. I/O occurs at STK0.
SP	Contents of the stack pointer

External to the Am2909/Am2911

A	Address to the control memory
I(A)	Instruction in control memory at address A
μWR	Contents of the microword register (at output of control memory). The microword register contains the instruction currently being executed.
T_n	Time period (cycle) n



Note: R_i and D_i connected together on Am2911 and OR_i removed.

Figure 2. Microprogram Sequencer Block Diagram.

MPR-094

Am2910 • Am2910-1 • Am2910A

Microprogram Controller

DISTINCTIVE CHARACTERISTICS

- Twelve Bits Wide
  Address up to 4096 words of microcode with one chip. All internal elements are a full 12 bits wide.
- Internal Loop Counter
  Pre-settable 12-bit down-counter for repeating instructions and counting loop iterations.
- Four Address Sources
  Microprogram Address may be selected from microprogram counter, branch address bus, 5-level push/pop stack, or internal holding register.
- Sixteen Powerful Microinstructions
  Executes 16 sequence control instructions, most of which are conditional on external condition input, state of internal loop counter, or both.
- Output Enable Controls for Three Branch Address Sources
  Built-in decoder function to enable external devices onto branch address bus. Eliminates external decoder.
- All Registers Positive Edge-triggered
  Simplifies timing problems. Eliminates long setup times.
- Fast Control from Condition Input
  Delay from condition code input to address output only 21ns typical.
- Fast
  The Am2910-1 supports 100ns cycle times. The Am2910A will meet or exceed all Am2910-1 specifications and will be 25–30% faster than the Am2910.
- IMOX™
  The Am2910A will be processed with AMD's proprietary IMOX technology.

GENERAL DESCRIPTION

The Am2910 Microprogram controller is an address sequencer intended for controlling the sequence of execution of microinstructions stored in microprogram memory. Besides the capability of sequential access, it provides conditional branching to any microinstruction within its 4096-microword range. A last-in, first-out stack provides microsubroutine return linkage and looping capability; there are five levels of nesting of microsubroutines. Microinstruction loop count control is provided with a count capacity of 4096.

During each microinstruction, the microprogram controller provides a 12-bit address from one of four sources: 1) the microprogram address register (μPC), which usually contains an address one greater than the previous address; 2) an external (direct) input (D); 3) a register/counter (R) retaining data loaded during a previous microinstruction; or 4) a five-deep last-in, first-out stack (F).

The Am2910-1 is a speed selected plug-in replacement for the Am2910 capable of 100ns cycle times. The Am2910A is a speed improved plug-in replacement of the Am2910 featuring AMD's ion-implanted micro-oxide (IMOX) processing and offering 25–30% speed improvement. The Am2910A also features a nine-word deep stack versus the five-deep stack of the Am2910.

Am2910 BLOCK DIAGRAM

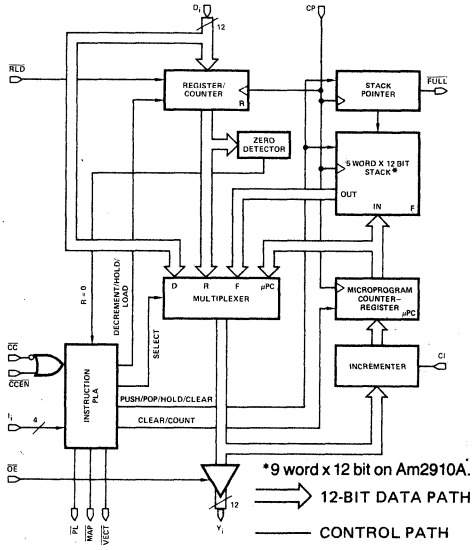


Figure 1.

RELATED PRODUCTS

Part No.	Description
Am2914	Vectored Interrupt Controller
Am2918	Pipeline Register
Am2922	Condition Code MUX
Am25LS377	Status Register
Am27S35	Registered PROM

For applications information, see Chapter II of **Bit Slice Microprocessor Design,** Mick & Brick, McGraw Hill Publications.

IMOX is a trademark of Advanced Micro Devices, Inc.

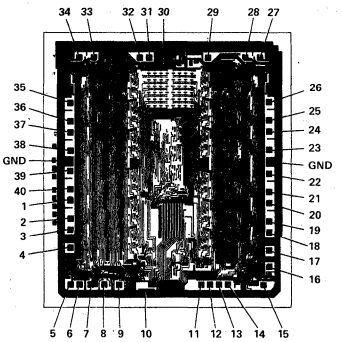
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2910A Order Number	Am2910-1 Order Number	Am2910 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
Available 1H1983	AM2910-1DM	AM2910PC	P-40	C	C-1
	AM2910-1DC	AM2910DC	D-40	C	C-1
		AM2910DC-B	D-40	C	B-2 (Note 4)
		AM2910DM	D-40	M	C-3
		AM2910DM-B	D-40	M	B-3
		AM2910FM	F-42	M	C-3
		AM2910FM-B	F-42	M	B-3
		AM2910LC	L-44	C	C-1
		AM2910LM	L-44	M	C-3
		AM2910LM-B	L-44	M	B-3
		AM2910XC	Dice	C	Visual inspection to MIL-STD-883 Method 20110B.
		AM2910XM	Dice	M	

Notes: 1. P = Molded DIP, D =.Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

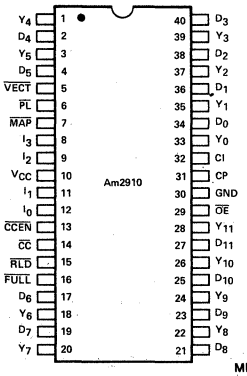
Metallization and Pad Layout



Die Size 0.170" x 0.194"
(Note: Numbers refer to DIP connections)

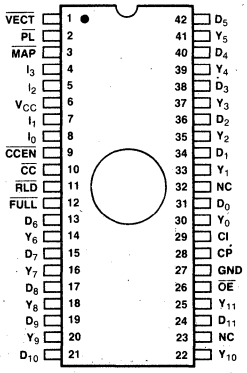
CONNECTION DIAGRAMS – Top Views

D-40, P-40



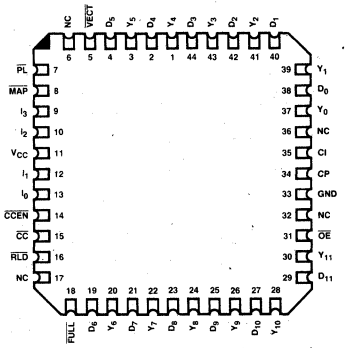
MPR-107

F-42-1



MPR-108

Chip-Pak™ L-44-1



Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5% MIN. = 4.75V MAX. = 5.25V

MIL T_C = −55°C to +125°C V_{CC} = 5.0V ±10% MIN. = 4.50V MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1.6mA, V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Y_{0-11}, I_{OL} = 12mA			0.5	Volts
			$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$, $\overline{FULL}$, I_{OL} = 8mA				
V_{IH}	Input HIGH Level (Note 4)	Guaranteed Input Logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Note 4)	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V	D_{0-11}			−0.87	mA
			CI, $\overline{CCEN}$			−0.54	
			I_{0-3}, $\overline{OE}$, $\overline{RLD}$			−0.72	
			$\overline{CC}$			−1.31	
			CP			−2.14	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	D_{0-11}			80	µA
			CI, $\overline{CCEN}$			30	
			I_{0-3}, $\overline{OE}$, $\overline{RLD}$			40	
			$\overline{CC}$			50	
			CP			100	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−30		−85	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX., $\overline{OE}$ = 2.4V	V_{OUT} = 0.5V			−50	µA
I_{OZH}			V_{OUT} = 2.4V			50	
I_{CC}	Power Supply Current	V_{CC} = MAX.	T_A = 25°C		195	320	mA
		Am2910PC, DC	T_A = 0°C to +70°C			344	
			T_A = +70°C			280	
		Am2910DM, FM	T_C = −55°C to +125°C			340	
			T_C = +125°C			227	

Notes: 1. For conditions shown as MIN., or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should only be static tested in a noise-free environment, (not functionally tested).

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5−8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

Am2910 SWITCHING CHARACTERISTICS

The tables below define the Am2910 switching characteristics. Tables A are set-up and hold times relative to the clock LOW-to-HIGH transition. Tables B are combinational delays. Tables C are clock requirements. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns. All outputs have maximum DC loading.

I. GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

Am2910PC,DC (T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V, C_L = 50pF)

A. Set-up and Hold Times

Input	t_s	t_h
$D_i \rightarrow R$	24	6
$D_i \rightarrow PC$	58	4
I_0-I_3	104	0
$\overline{CC}$	80	0
$\overline{CCEN}$	80	0
CI	46	5
$\overline{RLD}$	36	6

B. Combinational Delays

Input	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{Full}$
D_0-D_{11}	20	–	–
I_0-I_3	70	51	–
$\overline{CC}$	43	–	–
$\overline{CCEN}$	45	–	–
CP (Note 2) I = 8, 9, 15	100	–	60
	125	–	60
CP All other I	55	–	60
$\overline{OE}$ (Note 3)	35/30	–	–

C. Clock Requirements (Note 1)

Minimum Clock LOW Time	50	ns
Minimum Clock HIGH Time	35	ns
Minimum Clock Period, I = 8, 9, 15 (Note 2)	138	ns
	163	
Minimum Clock Period, I=14	93	ns

II. GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

Am2910DM,FM (T_C = −55 to +125°C, V_{CC} = 4.5 to 5.5V, C_L = 50pF)

A. Set-up and Hold Times

Input	t_s	t_h
$D_i \rightarrow R$	28	6
$D_i \rightarrow PC$	62	4
I_0-I_3	110	0
$\overline{CC}$	86	0
$\overline{CCEN}$	86	0
CI	58	5
$\overline{RLD}$	42	6

B. Combinational Delays

Input	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{Full}$
D_0-D_{11}	25	–	–
I_0-I_3	75	58	–
$\overline{CC}$	48	–	–
$\overline{CCEN}$	50	–	–
CP (Note 2) I = 8, 9, 15	106	–	67
	130	–	67
CP All other I	61	–	67
$\overline{OE}$ (Note 3)	40/30	–	–

C. Clock Requirements (Note 1)

Minimum Clock LOW Time	58	ns
Minimum Clock HIGH Time	42	ns
Minimum Clock Period, I = 8, 9, 15 (Note 2)	143	ns
	167	
Minimum Clock Period, I=14	100	ns

NOTES:
1. Clock periods for instructions not specified are determined by external conditions.
2. These instructions are conditional on the counter. Use the shorter specified delay times if the previous instruction could produce no change in the counter or could only decrement the counter. Use the longer delays from CP to outputs if the instruction prior to the clock was 4 or 12 or $\overline{RLD}$ was LOW.
3. Enable/Disable. Disable times measured to 0.5V change on output voltage level with C_L = 5.0pF.

Am2910-1 SWITCHING CHARACTERISTICS

The tables below define the Am2910-1 switching characteristics. Tables A are setup and hold times relative to the clock LOW-to-HIGH transition. Tables B are combinational delays. Tables C are clock requirements. All measurements are made at 1.5V with input levels at 0 or 3V. All values are in ns. All outputs have maximum DC loading.

I. GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

Am2910-1DC (T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V, C_L = 50pF)

A. Set-up and Hold Times

Input	t_s	t_h
$D_i \rightarrow R$	24	6
$D_i \rightarrow PC$	58	4
I_0-I_3	**75**	0
$\overline{CC}$	**63**	0
$\overline{CCEN}$	**63**	0
CI	46	5
$\overline{RLD}$	36	6

B. Combinational Delays

Input	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{Full}$
D_0-D_{11}	20	–	–
I_0-I_3	**50**	51	–
$\overline{CC}$	**30**	–	–
$\overline{CCEN}$	**30**	–	–
CP (Note 2) I = 8, 9, 15	**75**	–	60
	85	–	60
CP All other I	55	–	60
$\overline{OE}$ (Note 3)	35/30	–	–

C. Clock Requirements (Note 1)

Minimum Clock LOW Time	50	ns
Minimum Clock HIGH Time	35	ns
Minimum Clock Period, I = 8, 9, 15 (Note 2)	**113**	ns
	123	
Minimum Clock Period, I=14	93	ns

Boldface times indicate speed selected critical paths.

II. GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

Am2910-1DM (T_C = −55 to +125°C, V_{CC} = 4.5 to 5.5V, C_L = 50pF)

A. Set-up and Hold Times

Input	t_s	t_h
$D_i \rightarrow R$	28	6
$D_i \rightarrow PC$	62	4
I_0-I_3	**81**	0
$\overline{CC}$	**65**	0
$\overline{CCEN}$	**63**	0
CI	58	5
$\overline{RLD}$	42	6

B. Combinational Delays

Input	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{Full}$
D_0-D_{11}	25	–	–
I_0-I_3	**54**	58	–
$\overline{CC}$	**35**	–	–
$\overline{CCEN}$	**37**	–	–
CP (Note 2) I = 8, 9, 15	**77**	–	67
	98	–	67
CP All other I	61	–	67
$\overline{OE}$ (Note 3)	40/30	–	–

C. Clock Requirements (Note 1)

Minimum Clock LOW Time	58	ns
Minimum Clock HIGH Time	42	ns
Minimum Clock Period, I = 8, 9, 15 (Note 2)	**114**	ns
	125	
Minimum Clock Period, I=14	100	ns

NOTES:
1. Clock periods for instructions not specified are determined by external conditions.
2. These instructions are conditional on the counter. Use the shorter specified delay times if the previous instruction could produce no change in the counter or could only decrement the counter. Use the longer delays from CP to outputs if the instruction prior to the clock was 4 or 12 or $\overline{RLD}$ was LOW.
3. Enable/Disable. Disable times measured to 0.5V change on output voltage level with C_L = 5.0pF.

Am2910A SWITCHING CHARACTERISTICS

The tables below define the Am2910A switching characteristics. Tables A are setup and hold times relative to the clock LOW-to-HIGH transition. Tables B are combinational delays. Tables C are clock requirements. All measurements are made at 1.5V with input levels at 0 or 3V. All values are in ns. All outputs have maximum DC loading.

I. GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

Am2910APC,DC (T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V, C_L = 50pF)

A. Set-up and Hold Times

Input	t_S	t_h
$D_i \rightarrow R$		
$D_i \rightarrow PC$		
I_0-I_3		
$\overline{CC}$		
$\overline{CCEN}$		
CI		
$\overline{RLD}$		

B. Combinational Delays

Input	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{Full}$
D_0-D_{11}		–	–
I_0-I_3			–
$\overline{CC}$		–	–
$\overline{CCEN}$		–	–
CP (Note 2)		–	60
I = 8, 9, 15		–	60
CP	55	–	60
All other I			
$\overline{OE}$ (Note 3)	35/30	–	–

C. Clock Requirements (Note 1)

Minimum Clock LOW Time		ns
Minimum Clock HIGH Time		ns
Minimum Clock Period, I = 8, 9, 15 (Note 2)		ns
Minimum Clock Period, I = 14		ns

II. GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

Am2910ADM,FM (T_C = −55 to +125°C, V_{CC} = 4.5 to 5.5V, C_L = 50pF)

A. Set-up and Hold Times

Input	t_S	t_h
$D_i \rightarrow R$		
$D_i \rightarrow PC$		
I_0-I_3		
$\overline{CC}$		
$\overline{CCEN}$		
CI		
$\overline{RLD}$		

B. Combinational Delays

Input	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{Full}$
D_0-D_{11}		–	–
I_0-I_3			–
$\overline{CC}$		–	–
$\overline{CCEN}$		–	–
CP (Note 2)		–	
I = 8, 9, 15		–	
CP		–	
All other I			
$\overline{OE}$ (Note 3)		–	–

C. Clock Requirements (Note 1)

Minimum Clock LOW Time		ns
Minimum Clock HIGH Time		ns
Minimum Clock Period, I = 8, 9, 15 (Note 2)		ns
Minimum Clock Period, I = 14		ns

NOTES:
1. Clock periods for instructions not specified are determined by external conditions.
2. These instructions are conditional on the counter. Use the shorter specified delay times if the previous instruction could produce no change in the counter or could only decrement the counter. Use the longer delays from CP to outputs if the instruction prior to the clock was 4 or 12 or $\overline{RLD}$ was LOW.
3. Enable/Disable. Disable times measured to 0.5V change on output voltage level with C_L = 5.0pF.

ARCHITECTURE OF THE Am2910

The Am2910 is a bipolar microprogram controller intended for use in high-speed microprocessor applications. It allows addressing of up to 4K words of microprogram. A block diagram is shown in Figure 1.

The controller contains a four-input multiplexer that is used to select either the register/counter, direct input, microprogram counter, or stack as the source of the next microinstruction address.

The register/counter consists of 12 D-type, edge-triggered flip-flops, with a common clock enable. When its load control, $\overline{RLD}$, is LOW, new data is loaded on a positive clock transition. A few instructions include load; in most systems, these instructions will be sufficient, simplifying the microcode. The output of the register/counter is available to the multiplexer as a source for the next microinstruction address. The direct input furnishes a source of data for loading the register/counter.

The Am2910 contains a microprogram counter (μPC) that is composed of a 12-bit incrementer followed by a 12-bit register. The μPC can be used in either of two ways: When the carry-in to the incrementer is HIGH, the microprogram register is loaded on the next clock cycle with the current Y output word plus one ($Y + 1 \rightarrow \mu PC$). Sequential microinstructions are thus executed. When the carry-in is LOW, the incrementer passes the Y output word unmodified so that μPC is reloaded with the same Y word on the next clock cycle ($Y \rightarrow \mu PC$). The same microinstruction is thus executed any number of times.

The third source for the multiplexer is the direct (D) input. This source is used for branching.

The fourth source available at the multiplexer input is a 5-word by 12-bit stack (file). The stack is used to provide return address linkage when executing microsubroutines or loops. The stack contains a built-in stack pointer (SP) which always points to the last file word written. This allows stack reference operations (looping) to be performed without a pop.

The stack pointer operates as an up/down counter. During microinstructions 1, 4, and 5, the PUSH operation may occur. This causes the stack pointer to increment and the file to be written with the required return linkage. On the cycle following the PUSH, the return data is at the new location pointed to by the stack pointer.

During five microinstructions, a POP operation may occur. The stack pointer decrements at the next rising clock edge following a POP, effectively removing old information from the top of the stack.

The stack pointer linkage is such that any sequence of pushes, pops, or stack references can be achieved. At RESET (Instruction 0), the depth of nesting becomes zero. For each PUSH, the nesting depth increases by one; for each POP, the depth decreases by one. The depth can grow to five. After a depth of five is reached, $\overline{FULL}$ goes LOW. Any further PUSHes onto a full stack overwrite information at the top of the stack, but leave the stack pointer unchanged. This operation will usually destroy useful information and is normally avoided. A POP from an empty stack may place non-meaningful data on the Y outputs, but is otherwise safe. The stack pointer remains at zero whenever a POP is attempted from a stack already empty.

The register/counter is operated during three microinstructions (8, 9, 15) as a 12-bit down counter, with result = zero available as a microinstruction branch test criterion. This provides efficient iteration of microinstructions. The register/counter is arranged such that if it is preloaded with a number N and then used as a loop termination counter, the sequence will be executed exactly N+1 times. During instruction 15, a three-way branch under combined control of the loop counter and the condition code is available.

The device provides three-state Y outputs. These can be particularly useful in designs requiring automatic checkout of the processor. The microprogram controller outputs can be forced into the high-impedance state, and pre-programmed sequences of microinstructions can be executed via external access to the address lines.

OPERATION

Table I shows the result of each instruction in controlling the multiplexer which determines the Y outputs, and in controlling the three enable signals $\overline{PL}$, $\overline{MAP}$, and $\overline{VECT}$. The effect on the register/counter and the stack after the next positive-going clock edge is also shown. The multiplexer determines which internal source drives the Y outputs. The value loaded into μPC is either identical to the Y output, or else one greater, as determined by CI. For each instruction, one and only one of the three outputs $\overline{PL}$, $\overline{MAP}$, and $\overline{VECT}$ is LOW. If these outputs control three-state enables for the primary source of microprogram jumps (usually part of a pipeline register), a PROM which maps the instruction to a microinstruction starting location, and an optional third source (often a vector from a DMA or interrupt source), respectively, the three-state sources can drive the D inputs without further logic.

Several inputs, as shown in Table II, can modify instruction execution. The combination $\overline{CC}$ HIGH and $\overline{CCEN}$ LOW is used as a test in 9 of the 16 instructions. $\overline{RLD}$, when LOW, causes the D input to be loaded into the register/counter, overriding any HOLD or DEC operation specified in the instruction. $\overline{OE}$, normally LOW, may be forced HIGH to remove the Am2910 Y outputs from a three-state bus.

The stack, a five-word last-in, first-out 12-bit memory, has a pointer which addresses the value presently on the top of the stack. Explicit control of the stack pointer occurs during instruction 0 (RESET), which makes the stack empty by resetting the SP to zero. After a RESET, and whenever else the stack is empty, the contents of the top of stack is undefined until a PUSH occurs. Any POPs performed while the stack is empty put undefined data on the F outputs and leave the stack pointer at zero.

Any time the stack is full (five more PUSHes than POPs have occurred since the stack was last empty), the $\overline{FULL}$ warning output occurs. This signal first appears on the microcycle after a fifth PUSH. No additional PUSH should be attempted onto a full stack; if tried, information within the stack will be overwritten and lost.

TABLE I. INSTRUCTIONS

I_3-I_0	MNEMONIC	NAME	REG/ CNTR CON-TENTS	FAIL $\overline{CCEN}$ = LOW and $\overline{CC}$ = HIGH		PASS $\overline{CCEN}$ = HIGH or $\overline{CC}$ = LOW		REG/ CNTR	ENABLE
				Y	STACK	Y	STACK		
0	JZ	JUMP ZERO	X	0	CLEAR	0	CLEAR	HOLD	PL
1	CJS	COND JSB PL	X	PC	HOLD	D	PUSH	HOLD	PL
2	JMAP	JUMP MAP	X	D	HOLD	D	HOLD	HOLD	MAP
3	CJP	COND JUMP PL	X	PC	HOLD	D	HOLD	HOLD	PL
4	PUSH	PUSH/COND LD CNTR	X	PC	PUSH	PC	PUSH	Note 1	PL
5	JSRP	COND JSB R/PL	X	R	PUSH	D	PUSH	HOLD	PL
6	CJV	COND JUMP VECTOR	X	PC	HOLD	D	HOLD	HOLD	VECT
7	JRP	COND JUMP R/PL	X	R	HOLD	D	HOLD	HOLD	PL
8	RFCT	REPEAT LOOP, CNTR ≠ 0	≠ 0	F	HOLD	F	HOLD	DEC	PL
			= 0	PC	POP	PC	POP	HOLD	PL
9	RPCT	REPEAT PL, CNTR ≠ 0	≠ 0	D	HOLD	D	HOLD	DEC	PL
			= 0	PC	HOLD	PC	HOLD	HOLD	PL
10	CRTN	COND RTN	X	PC	HOLD	F	POP	HOLD	PL
11	CJPP	COND JUMP PL & POP	X	PC	HOLD	D	POP	HOLD	PL
12	LDCT	LD CNTR & CONTINUE	X	PC	HOLD	PC	HOLD	LOAD	PL
13	LOOP	TEST END LOOP	X	F	HOLD	PC	POP	HOLD	PL
14	CONT	CONTINUE	X	PC	HOLD	PC	HOLD	HOLD	PL
15	TWB	THREE-WAY BRANCH	≠ 0	F	HOLD	PC	POP	DEC	PL
			= 0	D	POP	PC	POP	HOLD	PL

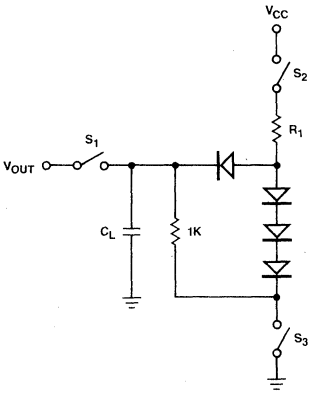
Note 1: If $\overline{CCEN}$ = LOW and $\overline{CC}$ = HIGH, hold; else load. X = Don't Care

TABLE II. PIN FUNCTIONS

Abbreviation	Name	Function
D_i	Direct Input Bit i	Direct input to register/counter and multiplexer. D_0 is LSB
I_i	Instruction Bit i	Selects one-of-sixteen instructions for the Am2910
$\overline{CC}$	Condition Code	Used as test criterion. Pass test is a LOW on $\overline{CC}$.
$\overline{CCEN}$	Condition Code Enable	Whenever the signal is HIGH, $\overline{CC}$ is ignored and the part operates as though $\overline{CC}$ were true (LOW).
CI	Carry-In	Low order carry input to incrementer for microprogram counter
$\overline{RLD}$	Register Load	When LOW forces loading of register/counter regardless of instruction or condition
$\overline{OE}$	Output Enable	Three-state control of Y_i outputs
CP	Clock Pulse	Triggers all internal state changes at LOW-to-HIGH edge
V_{CC}	+5 Volts	
GND	Ground	
Y_i	Microprogram Address Bit i	Address to microprogram memory. Y_0 is LSB, Y_{11} is MSB
$\overline{FULL}$	Full	Indicates that five items are on the stack
$\overline{PL}$	Pipeline Address Enable	Can select #1 source (usually Pipeline Register) as direct input source
$\overline{MAP}$	Map Address Enable	Can select #2 source (usually Mapping PROM or PLA) as direct input source
$\overline{VECT}$	Vector Address Enable	Can select #3 source (for example, Interrupt Starting Address) as direct input source

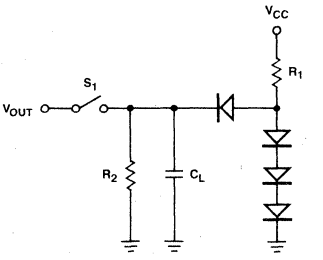
TEST OUTPUT LOAD CONFIGURATIONS FOR Am2910

A. THREE-STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

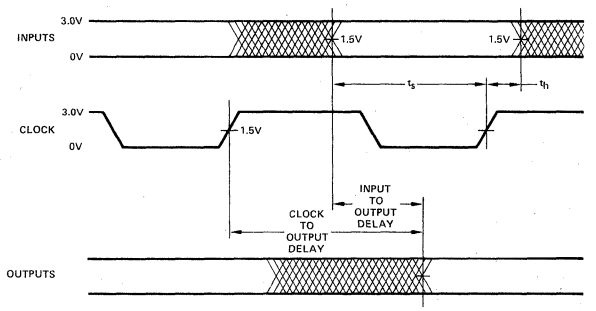
Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
   S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTUPT LOADS FOR Am2910

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
–	$Y_{0\text{-}11}$	A	300	1K
5	$\overline{VECT}$	B	470	1.5K
6	$\overline{PL}$	B	470	1.5K
7	$\overline{MAP}$	B	470	1.5K
16	$\overline{FULL}$	B	470	1.5K

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

Figure 2. Switching Waveforms.



See Tables A for t_s and t_h for various inputs. See Tables B for combinational delays from clock and other inputs to outputs. See Figure 5 for timing of a typical CCU cycle.

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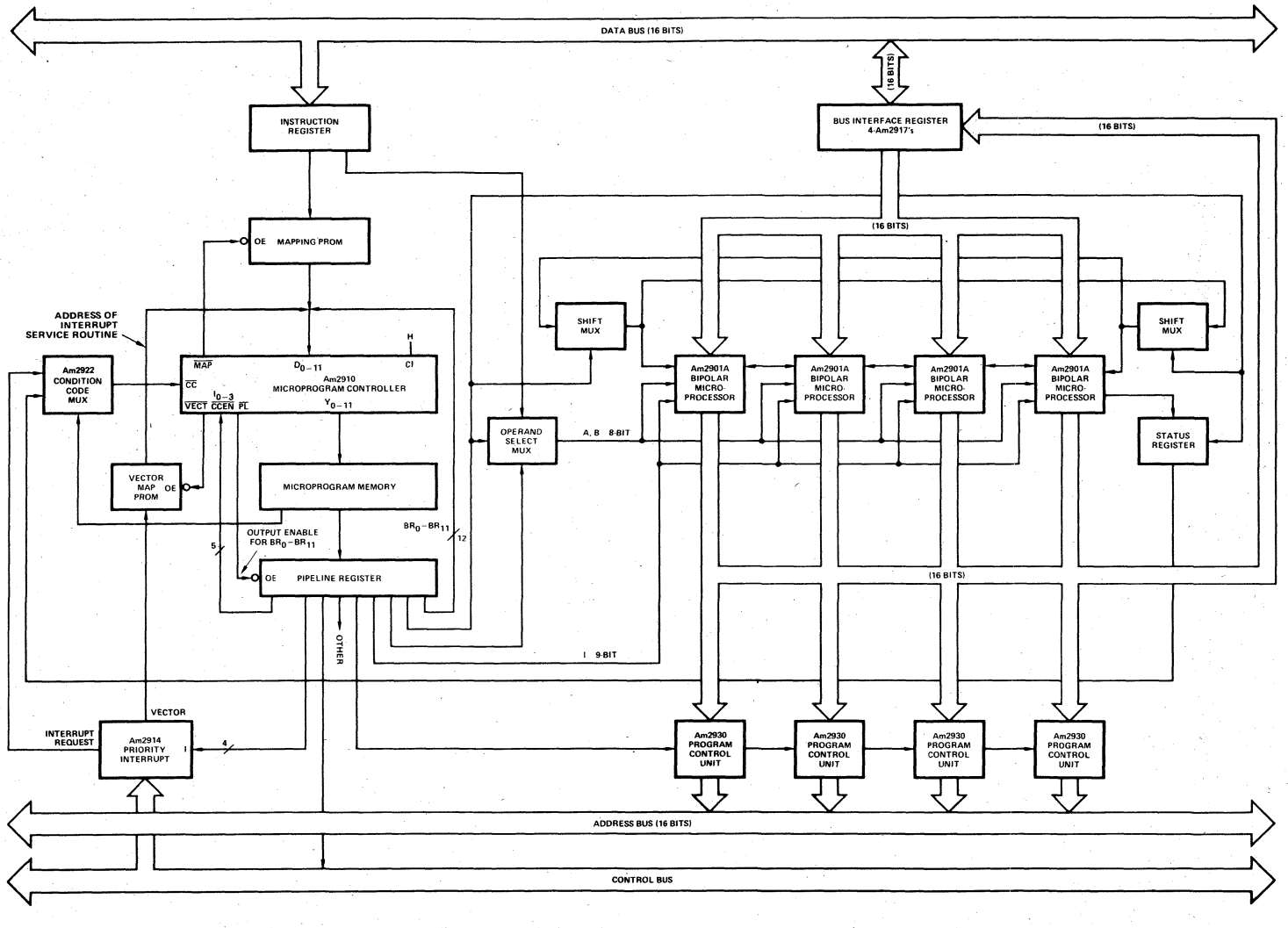

Figure 3. Typical Bipolar Microcomputer Using Am2910.

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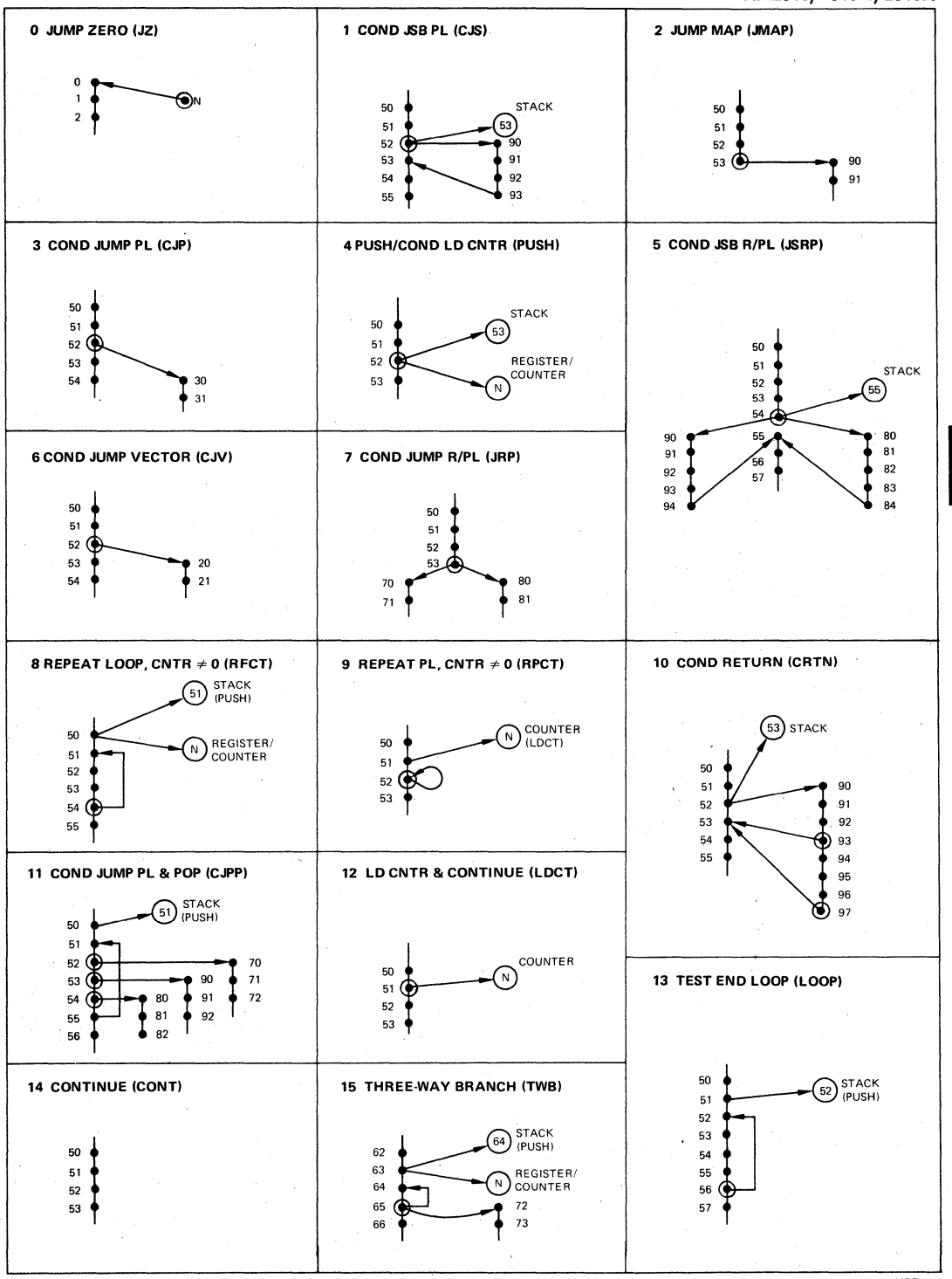

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Figure 4. Am2910 Execution Examples.

THE Am2910 INSTRUCTION SET

The Am2910 provides 16 instructions which select the address of the next microinstruction to be executed. Four of the instructions are unconditional – their effect depends only on the instruction. Ten of the instructions have an effect which is partially controlled by an external, data-dependent condition. Three of the instructions have an effect which is partially controlled by the contents of the internal register/counter. The instruction set is shown in Table I. In this discussion it is assumed that C_i is tied HIGH.

In the ten conditional instructions, the result of the data-dependent test is applied to $\overline{CC}$. If the $\overline{CC}$ input is LOW, the test is considered to have been passed, and the action specified in the name occurs; otherwise, the test has failed and an alternate (often simply the execution of the next sequential microinstruction) occurs. Testing of $\overline{CC}$ may be disabled for a specific microinstruction by setting $\overline{CCEN}$ HIGH, which unconditionally forces the action specified in the name; that is, it forces a pass. Other ways of using $\overline{CCEN}$ include (1) tying it HIGH, which is useful if no microinstruction is data-dependent; (2) tying it LOW if data-dependent instructions are never forced unconditionally; or (3) tying it to the source of Am2910 instruction bit I_0, which leaves instructions 4, 6, and 10 as data-dependent but makes others unconditional. All of these tricks save one bit of microcode width.

The effect of three instructions depends on the contents of the register/counter. Unless the counter holds a value of zero, it is decremented; if it does hold zero, it is held and a different microprogram next address is selected. These instructions are useful for executing a microinstruction loop a known number of times. Instruction 15 is affected both by the external condition code and the internal register/counter.

Perhaps the best technique for understanding the Am2910 is to simply take each instruction and review its operation. In order to provide some feel for the actual execution of these instructions, Figure 4 is included and depicts examples of all 16 instructions.

The examples given in Figure 4 should be interpreted in the following manner: The intent is to show microprogram flow as various microprogram memory words are executed. For example, the CONTINUE instruction, instruction number 14, as shown in Figure 4, simply means that the contents of microprogram memory word 50 is executed, then the contents of word 51 is executed. This is followed by the contents of microprogram memory word 52 and the contents of microprogram memory word 53. The microprogram addresses used in the examples were arbitrarily chosen and have no meaning other than to show instruction flow. The exception to this is the first example, JUMP ZERO, which forces the microprogram location counter to address ZERO. Each dot refers to the time that the contents of the microprogram memory word is in the pipeline register. While no special symbology is used for the conditional instructions, the text to follow will explain what the conditional choices are in each example.

It might be appropriate at this time to mention that AMD has a microprogram assembler called AMDASM, which has the capability of using the Am2910 instructions in symbolic representation. AMDASM's Am2910 instruction symbolics (or mnemonics) are given in Figure 4 for each instruction and are also shown in Table I.

Instruction 0, JZ (JUMP and ZERO, or RESET) unconditionally specifies that the address of the next microinstruction is zero. Many designs use this feature for power-up sequences and provide the power-up firmware beginning at microprogram memory word location 0.

Instruction 1 is a CONDITIONAL JUMP-TO-SUBROUTINE via the address provided in the pipeline register. As shown in Figure 4, the machine might have executed words at address 50, 51, and 52. When the contents of address 52 is in the pipeline register, the next address control function is the CONDITIONAL JUMP-TO-SUBROUTINE. Here, if the test is passed, the next instruction executed will be the contents of microprogram memory location 90. If the test has failed, the JUMP-TO-SUBROUTINE will not be executed; the contents of microprogram memory location 53 will be executed instead. Thus, the CONDITIONAL JUMP-TO-SUBROUTINE instruction at location 52 will cause the instruction either in location 90 or in location 53 to be executed next. If the TEST input is such that location 90 is selected, value 53 will be pushed onto the internal stack. This provides the return linkage for the machine when the subroutine beginning at location 90 is completed. In this example, the subroutine was completed at location 93 and a RETURN-FROM-SUBROUTINE would be found at location 93.

Instruction 2 is the JUMP MAP instruction. This is an unconditional instruction which causes the $\overline{MAP}$ output to be enabled so that the next microinstruction location is determined by the address supplied via the mapping PROMs. Normally, the JUMP MAP instruction is used at the end of the instruction fetch sequence for the machine. In the example of Figure 4, microinstructions at locations 50, 51, 52, and 53 might have been the fetch sequence and at its completion at location 53, the jump map function would be contained in the pipeline register. This example shows the mapping PROM outputs to be 90; therefore, an unconditional jump to microprogram memory address 90 is performed.

Instruction 3, CONDITIONAL JUMP PIPELINE, derives its branch address from the pipeline register branch address value (BR_0 – BR_{11} in Figure 2). This instruction provides a technique for branching to various microprogram sequences depending upon the test condition inputs. Quite often, state machines are designed which simply execute tests on various inputs waiting for the condition to come true. When the true condition is reached, the machine then branches and executes a set of microinstructions to perform some function. This usually has the effect of resetting the input being tested until some point in the future. Figure 4 shows the conditional jump via the pipeline register address at location 52. When the contents of microprogram memory word 52 are in the pipeline register, the next address will be either location 53 or location 30 in this example. If the test is passed, the value currently in the pipeline register (30) will be selected. If the test fails, the next address selected will be contained in the microprogram counter which, in this example, is 53.

Instruction 4 is the PUSH/CONDITIONAL LOAD COUNTER instruction and is used primarily for setting up loops in microprogram firmware. In Figure 4, when instruction 52 is in the pipeline register, a PUSH will be made onto the stack and the counter will be loaded based on the condition. When a PUSH occurs, the value pushed is always the next sequential instruction address. In this case, the address is 53. If the test fails, the counter is not loaded; if it is passed, the counter is loaded with the value contained in the pipeline register branch address field. Thus, a single microinstruction can be used to set up a loop to be executed a specific number of times. Instruction 8 will

THE Am2910 INSTRUCTION SET (Cont.)

describe how to use the pushed value and the register/counter for looping.

Instruction 5 is a CONDITIONAL JUMP-TO-SUBROUTINE via the register/counter or the contents of the PIPELINE register. As shown in Figure 4, a PUSH is always performed and one of two subroutines executed. In this example, either the subroutine beginning at address 80 or the subroutine beginning at address 90 will be performed. A return-from-subroutine (instruction number 10) returns the microprogram flow to address 55. In order for this microinstruction control sequence to operate correctly, both the next address fields of instruction 53 and the next address fields of instruction 54 would have to contain the proper value. Let's assume that the branch address fields of instruction 53 contain the value 90 so that it will be in the Am2910 register/counter when the contents of address 54 are in the pipeline register. This requires that the instruction at address 53 load the register/counter. Now, during the execution of instruction 5 (at address 54), if the test failed, the contents of the register (value = 90) will select the address of the next microinstruction. If the test input passes, the pipeline register contents (value = 80) will determine the address of the next microinstruction. Therefore, this instruction provides the ability to select one of two subroutines to be executed based on a test condition.

Instruction 6 is a CONDITIONAL JUMP VECTOR instruction which provides the capability to take the branch address from a third source heretofore not discussed. In order for this instruction to be useful, the Am2910 output, $\overline{VECT}$ is used to control a three-state control input of a register, buffer, or PROM containing the next microprogram address. This instruction provides one technique for performing interrupt type branching at the microprogram level. Since this instruction is conditional, a pass causes the next address to be taken from the vector source, while failure causes the next address to be taken from the microprogram counter. In the example of Figure 4, if the CONDITIONAL JUMP VECTOR instruction is contained at location 52, execution will continue at vector address 20 if the $\overline{CC}$ input is LOW and the microinstruction at address 53 will be executed if the $\overline{CC}$ input is HIGH.

Instruction 7 is a CONDITIONAL JUMP via the contents of the Am2910 REGISTER/COUNTER or the contents of the PIPELINE register. This instruction is very similar to instruction 5; the conditional jump-to-subroutine via R or PL. The major difference between instruction 5 and instruction 7 is that no push onto the stack is performed with 7. Figure 4 depicts this instruction as a branch to one of two locations depending on the test condition. The example assumes the pipeline register contains the value 70 when the contents of address 52 is being executed. As the contents of address 53 is clocked into the pipeline register, the value 70 is loaded into the register/counter in the Am2910. The value 80 is available when the contents of address 53 is in the pipeline register. Thus, control is transferred to either address 70 or address 80 depending on the test condition.

Instruction 8 is the REPEAT LOOP, COUNTER ≠ ZERO instruction. This microinstruction makes use of the decrementing capability of the register/counter. To be useful, some previous instruction, such as 4, must have loaded a count value into the register/counter. This instruction checks to see whether the register/counter contains a non-zero value. If so, the register/counter is decremented, and the address of the next microinstruction is taken from the top of the stack. If the register counter contains zero, the loop exit condition is occuring; control falls through to the next sequential microinstruction by selecting μPC; the stack is POP'd by decrementing the stack pointer, but the contents of the top of the stack are thrown away.

An example of the REPEAT LOOP, COUNTER ≠ ZERO instruction is shown in Figure 4. In this example, location 50 most likely would contain a PUSH/CONDITIONAL LOAD COUNTER instruction which would have caused address 51 to be PUSHed on the stack and the counter to be loaded with the proper value for looping the desired number of times.

In this example, since the loop test is made at the end of the instructions to be repeated (microaddress 54), the proper value to be loaded by the instructions at address 50 is one less than the desired number of passes through the loop. This method allows a loop to be executed 1 to 4096 times. If it is desired to execute the loop from 0 to 4095 times, the firmware should be written to make the loop exit test immediately after loop entry.

Single-microinstruction loops provide a highly efficient capability for executing a specific microinstruction a fixed number of times. Examples include fixed rotates, byte swap, fixed point multiply, and fixed point divide.

Instruction 9 is the REPEAT PIPELINE REGISTER, COUNTER ≠ ZERO instruction. This instruction is similar to instruction 8 except that the branch address now comes from the pipeline register rather than the file. In some cases, this instruction may be thought of as a one-word file extension; that is, by using this instruction, a loop with the counter can still be performed when subroutines are nested five deep. This instruction's operation is very similar to that of instruction 8. The differences are that on this instruction, a failed test condition causes the source of the next microinstruction address to be the D inputs; and, when the test condition is passed, this instruction does not perform a POP because the stack is not being used.

In the example of Figure 4, the REPEAT PIPELINE, COUNTER ≠ ZERO instruction is instruction 52 and is shown as a single microinstruction loop. The address in the pipeline register would be 52. Instruction 51 in this example could be the LOAD COUNTER AND CONTINUE instruction (number 12). While the example shows a single microinstruction loop, by simply changing the address in a pipeline register, multi-instruction loops can be performed in this manner for a fixed number of times as determined by the counter.

Instruction 10 is the conditional RETURN-FROM-SUBROUTINE instruction. As the name implies, this instruction is used to branch from the subroutine back to the next microinstruction address following the subroutine call. Since this instruction is conditional, the return is performed only if the test is passed. If the test is failed, the next sequential microinstruction is performed. The example in Figure 4 depicts the use of the conditional RETURN-FROM-SUBROUTINE instruction in both the conditional and the unconditional modes. This example first shows a jump-to-subroutine at instruction location 52 where control is transferred to location 90. At location 93, a conditional RETURN-FROM-SUBROUTINE instruction is performed. If the test is passed, the stack is accessed and the program will transfer to the next instruction at address 53. If the test is failed, the next microinstruction at address 94 will be executed. The program will continue to address 97 where the subroutine is complete. To perform an unconditional RETURN-FROM-SUBROUTINE, the conditional RETURN-FROM-SUBROUTINE instruction is executed unconditionally; the microinstruction at address 97 is programmed to force

5

THE Am2910 INSTRUCTION SET (Cont.)

$\overline{CCEN}$ HIGH, disabling the test and the forced PASS causes an unconditional return.

Instruction 11 is the CONDITIONAL JUMP PIPELINE register address and POP stack instruction. This instruction provides another technique for loop termination and stack maintenance. The example in Figure 4 shows a loop being performed from address 55 back to address 51. The instructions at locations 52, 53, and 54 are all conditional JUMP and POP instructions. At address 52, if the $\overline{CC}$ input is LOW, a branch will be made to address 70 and the stack will be properly maintained via a POP. Should the test fail, the instruction at location 53 (the next sequential instruction) will be executed. Likewise, at address 53, either the instruction at 90 or 54 will be subsequently executed, respective to the test being passed or failed. The instruction at 54 follows the same rules, going to either 80 or 55. An instruction sequence as described here, using the CONDITIONAL JUMP PIPELINE and POP instruction, is very useful when several inputs are being tested and the microprogram is looping waiting for any of the inputs being tested to occur before proceeding to another sequence of instructions. This provides the powerful jump-table programming technique at the firmware level.

Instruction 12 is the LOAD COUNTER AND CONTINUE instruction, which simply enables the counter to be loaded with the value at its parallel inputs. These inputs are normally connected to the pipeline branch address field which (in the architecture being described here) serves to supply either a branch address or a counter value depending upon the microinstruction being executed. There are altogether three ways of loading the counter — the explicit load by this instruction 12; the conditional load included as part of instruction 4; and the use of the $\overline{RLD}$ input along with any instruction. The use of $\overline{RLD}$ with any instruction overrides any counting or decrementation specified in the instruction, calling for a load instead. Its use provides additional microinstruction power, at the expense of one bit of microinstruction width. This instruction 12 is exactly equivalent to the combination of instruction 14 and $\overline{RLD}$ LOW. Its purpose is to provide a simple capability to load the register/counter in those implementations which do not provide microprogrammed control for $\overline{RLD}$.

Instruction 13 is the TEST END-OF-LOOP instruction, which provides the capability of conditionally exiting a loop at the bottom; that is, this is a conditional instruction that will cause the microprogram to loop, via the file, if the test is failed else to continue to the next sequential instruction. The example in Figure 4 shows the TEST END-OF-LOOP microinstruction at address 56. If the test fails, the microprogram will branch to address 52. Address 52 is on the stack because a PUSH instruction had been executed at address 51. If the test is passed at instruction 56, the loop is terminated and the next sequential microinstruction at address 57 is executed, which also causes the stack to be POP'd; thus, accomplishing the required stack maintenance.

Instruction 14 is the CONTINUE instruction, which simply causes the microprogram counter to increment so that the next sequential microinstruction is executed. This is the simplest microinstruction of all and should be the default instruction which the firmware requests whenever there is nothing better to do.

Instruction 15, THREE-WAY BRANCH, is the most complex. It provides for testing of both a data-dependent condition and the counter during one microinstruction and provides for selecting among one of three microinstruction addresses as the next microinstruction to be performed. Like instruction 8, a previous instruction will have loaded a count into the register/counter while pushing a microbranch address onto the stack. Instruction 15 performs a decrement-and-branch-until-zero function similar to instruction 8. The next address is taken from the top of the stack until the count reaches zero; then the next address comes from the pipeline register. The above action continues as long as the test condition fails. If at any execution of instruction 15 the test condition is passed, no branch is taken; the microprogram counter register furnishes the next address. When the loop is ended, either by the count becoming zero, or by passing the conditional test, the stack is POP'd by decrementing the stack pointer, since interest in the value contained at the top of the stack is then complete.

The application of instruction 15 can enhance performance of a variety of machine-level instructions. For instance, (1) a memory search instruction to be terminated either by finding a desired memory content or by reaching the search limit; (2) variable-field-length arithmetic terminated early upon finding that the content of the portion of the field still unprocessed is all zeroes; (3) key search in a disc controller processing variable length records; (4) normalization of a floating point number.

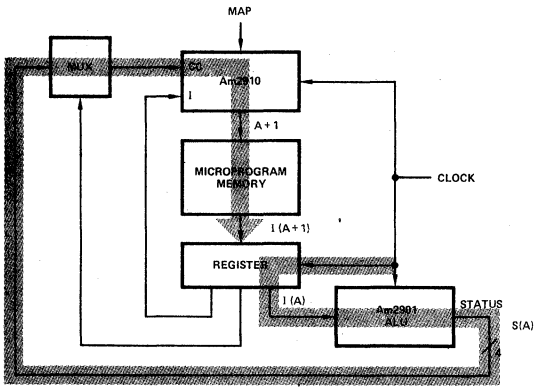
As one example, consider the case of a memory search instruction. As shown in Figure 4, the instruction at microprogram address 63 can be Instruction 4 (PUSH), which will push the value 64 onto the microprogram stack and load the number N, which is one less than the number of memory locations to be searched before giving up. Location 64 contains a microinstruction which fetches the next operand from the memory area to be searched and compares it with the search key. Location 65 contains a microinstruction which tests the result of the comparison and also is a THREE-WAY BRANCH for microprogram control. If no match is found, the test fails and the microprogram goes back to location 64 for the next operand address. When the count becomes zero, the microprogram branches to location 72, which does whatever is necessary if no match is found. If a match occurs on any execution of the THREE-WAY BRANCH at location 65, control falls through to location 66 which handles this case. Whether the instruction ends by finding a match or not, the stack will have been POP'd once, removing the value 64 from the top of the stack.

OTHER ARCHITECTURES USING THE Am2910

(Shading shows path(s) which usually limit speed)

Figure 6.

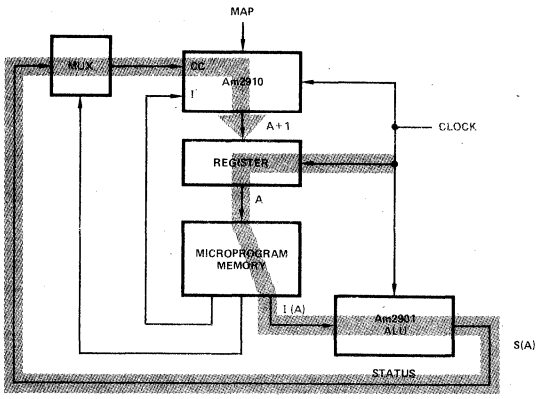
A. Instruction Based



A Register at the Microprogram Memory output contains the microinstruction being executed. The microprogram memory and Am2901 delay are in series. Conditional branches are executed on same cycle as the ALU operation generating the condition.

MPR-114

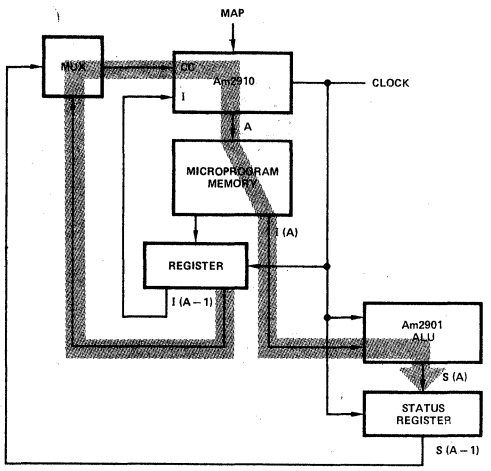
B. Addressed Based



The Register at the Am2910 output contains the address of the microinstruction being executed. The Microprogram Memory and Am2901 are in series in the critical path. This architecture provides about the same speed as the Instruction based architecture, but requires fewer register bits, since only the address (typically 10-12 bits) is stored instead of the instruction (typically 40-60 bits).

MPR-115

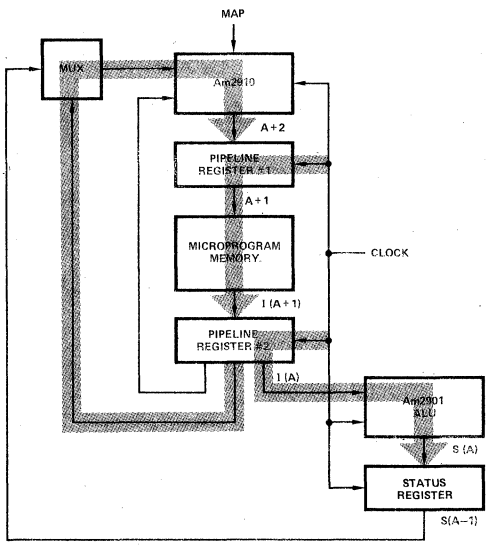
C. Data Based



The Status Register provides conditional Branch control based on results of previous ALU cycle. The Microprogram Memory and Am2901 are in series in the critical paths.

MPR-116

D. Two Level Pipeline Based



Two level pipeline provides highest possible speed. It is more difficult to program because the selection of a microinstruction occurs two instructions ahead of its execution.

MPR-117

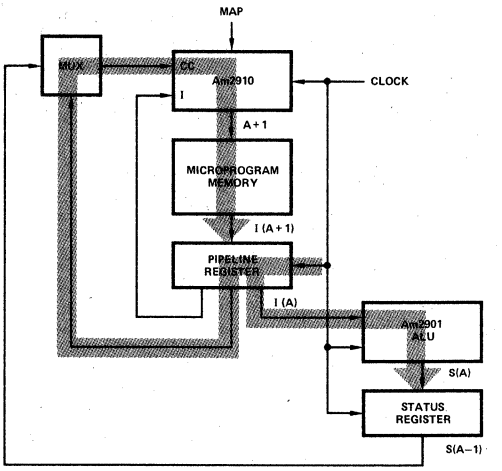
5

ARCHITECTURES USING THE Am2910

(Shading shows path(s) which usually limit speed)

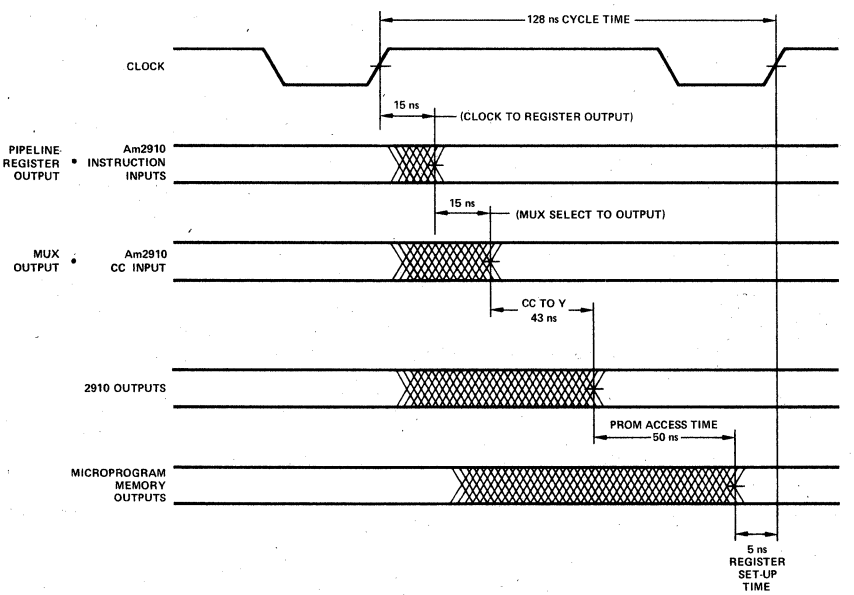
Figure 5.

One Level Pipeline Based
(Recommended)



One level pipeline provides better speed than most other architectures. The μProgram Memory and the Am2901 array are in parallel speed paths instead of in series. This is the recommended architecture for Am2900 designs.

MPR-112



Typical CCU Cycle Timing Waveforms.

This drawing shows the timing relationships in the CCU illustrated above.

MPR-113

Am2910 HIGH SPEED APPLICATION

Optimal Am2910 configurations can support high speed bit slice designs. When used with high speed registers and PROMs', the Am2910-1/Am2910A can execute simple instructions in 100ns.

The following figure illustrates the usual critical path in the sequencer.

Timing on the critical paths becomes

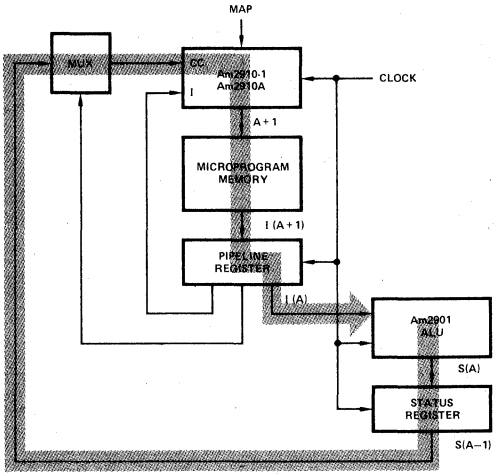
Device	Path	Delay
Status Register	Clock → Output	12ns
Fast MUX	Select → Output	20ns
Am2910-1/Am2910A	CC → Y	30ns
Fast PROM	Addr → Output	35ns
Pipeline Register	Setup	5ns
		102ns

All delay times are worst case times in ns.

The following gives one suggested parts configuration to meet this design criterion.

Status Register	Am29825
MUX	Am2922
PROM	Am27S35
Pipeline Register	Am2918

One Level Pipeline Based (Recommended)



Am2912
Quad Bus Transceiver

Distinctive Characteristics

- Input to bus is inverting
- Quad high-speed open collector bus transceiver
- Driver outputs can sink 100mA at 0.8V maximum
- Bus compatible with Am2905, Am2906, Am2907
- Advanced Schottky processing
- PNP inputs to reduce input loading

FUNCTIONAL DESCRIPTION

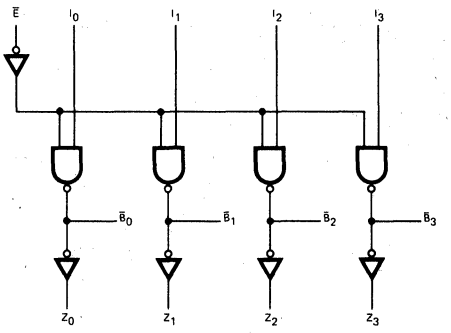
The Am2912 is a quad Bus Transceiver consisting of four high-speed bus drivers with open-collector outputs capable of sinking 100mA at 0.8 volts and four high-speed bus receivers. Each driver output is connected internally to the high-speed bus receiver in addition to being connected to the package pin. The receiver has a Schottky TTL output capable of driving 10 Schottky TTL unit loads.

An active LOW enable gate controls the four drivers so that outputs of different device drivers can be connected together for party-line operation. The enable input can be conveniently driven by active LOW decoders such as the Am25LS139.

The bus output high-drive capability in the LOW state allows party-line operation with a line impedance as low as 100Ω. The line can be terminated at both ends, and still give considerable noise margin at the receiver. The receiver typical switching point is 2.0 volts.

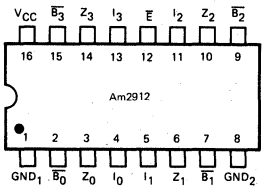
The Am2912 features advanced Schottky processing to minimize propagation delay. The device package also has two ground pins to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both GND_1 and GND_2 should be tied to the ground bus external to the device package.

LOGIC DIAGRAM



BLI-061

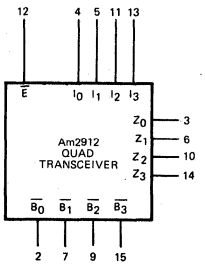
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BLI-062

LOGIC SYMBOL



LIC-370

V_{CC} = Pin 16
GND_1 = Pin 1
GND_2 = Pin 8

BLI-063

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Bus	200 mA
Output Current, Into Outputs (Except Bus)	30 mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Am2912PC, DC, XC T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am2912DM, FM, XM T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL) MIN. = 4.5V MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage (Receiver Outputs)	V_{CC} = MIN., I_{OH} = −1.0mA, V_{IN} = V_{IL} or V_{IH}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Receiver Outputs)	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = V_{IL} or V_{IH}				0.5	Volts
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs				0.8	Volts
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4V	Enable			−0.36	mA
			Data			−0.54	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7V	Enable			20	µA
			Data			30	
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 5.5V				100	µA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX. (Note 3)	MIL	−20		−55	mA
			COM'L	−18		−60	
I_{CCL}	Power Supply Current (All Bus Outputs LOW)	V_{CC} = MAX., Enable = GND			45	70	mA

Bus Input/Output Characteristics

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Output LOW Voltage	V_{CC} = MIN.	MIL	I_{OL} = 40mA		0.33	0.5	Volts
				I_{OL} = 70mA		0.42	0.7	
				I_{OL} = 100mA		0.51	0.8	
			COM'L	I_{OL} = 40mA		0.33	0.5	
				I_{OL} = 70mA		0.42	0.7	
				I_{OL} = 100mA		0.51	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.		V_O = 0.8V			−50	µA
			MIL	V_O = 4.5V			200	
			COM'L	V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power Off)	V_O = 4.5V					100	µA
V_{TH}	Receiver Input HIGH Threshold	Bus Enable = 2.4V, V_{CC} = MAX		MIL	2.4	2.0		Volts
				COM'L	2.25	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus Enable = 2.4V, V_{CC} = MIN		MIL		2.0	1.6	Volts
				COM'L		2.0	1.75	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Data Input to Bus	R_B = 50Ω, C_B = 50pF (Note 1)		10	15	ns
t_{PHL}				10	15	
t_{PLH}	Enable Input to Bus			14	18	ns
t_{PHL}				13	18	
t_{PLH}	Bus to Receiver Out	R_B = 50Ω, R_L = 280Ω, C_B = 50pF (Note 1), C_L = 15pF		10	15	ns
t_{PHL}				10	15	
t_r	Bus	R_B = 50Ω, C_B = 50pF (Note 1)	4.0	10		ns
t_f	Bus		2.0	4.0		ns

Note 1. Includes probe and jig capacitance.

TRUTH TABLE

Inputs		Outputs	
$\overline{E}$	I	$\overline{B}$	Z
L	L	H	L
L	H	L	H
H	X	Y	$\overline{Y}$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Y = Voltage Level of Bus (Assumes Control by Another Bus Transceiver)

ORDERING INFORMATION

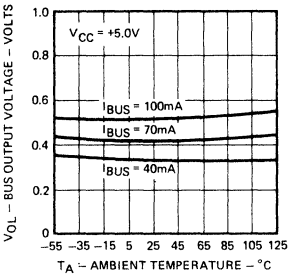
Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2912PC	P-16-1	C	C-1
AM2912DC	D-16-1	C	C-1
AM2912DC-B	D-16-1	C	B-1
AM2912DM	D-16-1	M	C-3
AM2912DM-B	D-16-1	M	B-3
AM2912FM	F-16-1	M	C-3
AM2912FM-B	F-16-1	M	B-3
AM2912XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2912XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to 70°C, V_{CC} = 4.75V to 5.25V, M = −55 to + 125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

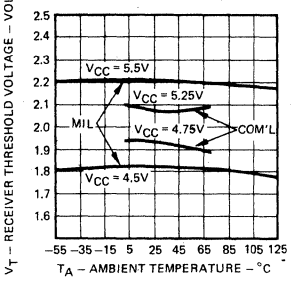
TYPICAL PERFORMANCE CURVES

Typical Bus Output Low Voltage Versus Ambient Temperature



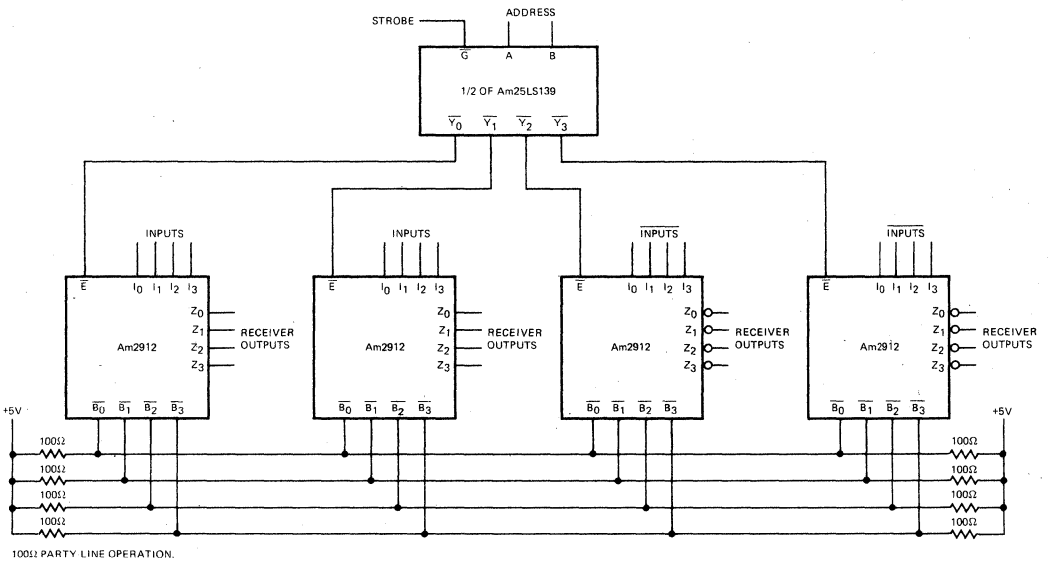
BLI-064

Receiver Threshold Variation Versus Ambient Temperature



BLI-065

TYPICAL APPLICATION

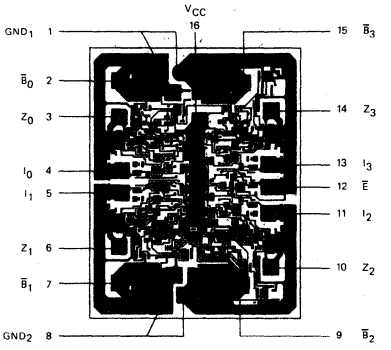


100Ω PARTY LINE OPERATION.

BLI-066

Metallization and Pad Layout

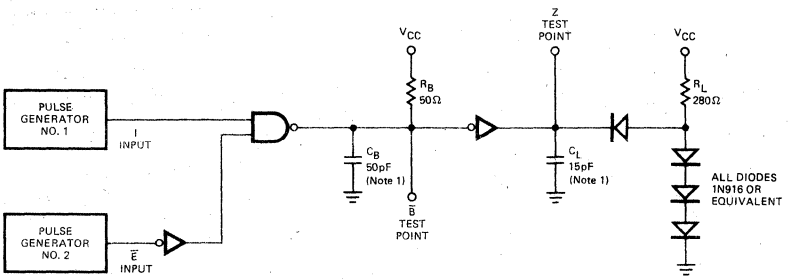
Am2912



DIE SIZE 0.059" X 0.075"

SWITCHING CHARACTERISTICS

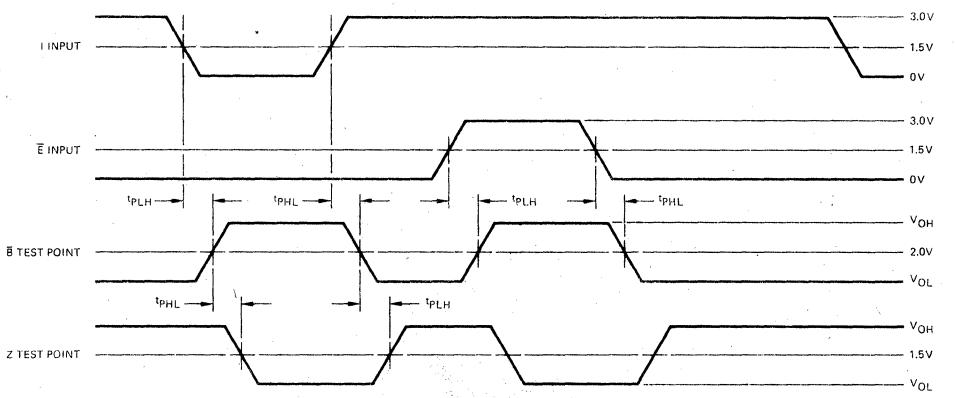
TEST CIRCUIT



BLI-067

Note 1. Includes Probe and Jig Capacitance.

WAVEFORMS



BLI-068

Am2913

Priority Interrupt Expander

Distinctive Characteristics

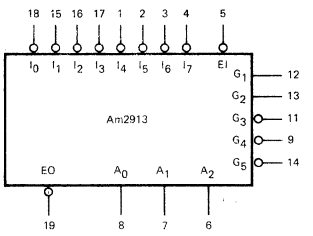
- Encodes eight lines to three-line binary
- Expands use of Am2914
- Cascadable
- Similar in function to Am54LS/74LS/25LS148/2513
- Gated three-state output
- Advanced Low-Power Schottky processing

FUNCTIONAL DESCRIPTION

The Low-Power Schottky Priority Interrupt Expander is an extention of the Am2900 series of Bipolar Processor family and is used to expand and prioritize the output of the Am2914 Priority Interrupt circuit. Affording an increase of vectored priority interrupt in groups of eight, this unit accepts active LOW inputs and produces a three-state active HIGH output prioritized from active $\overline{I}_7$ to $\overline{I}_0$. The output is gated by five control signals, three active LOW and two active HIGH. Also provided is a cascade input ($\overline{EI}$) and Enable Output ($\overline{EO}$).

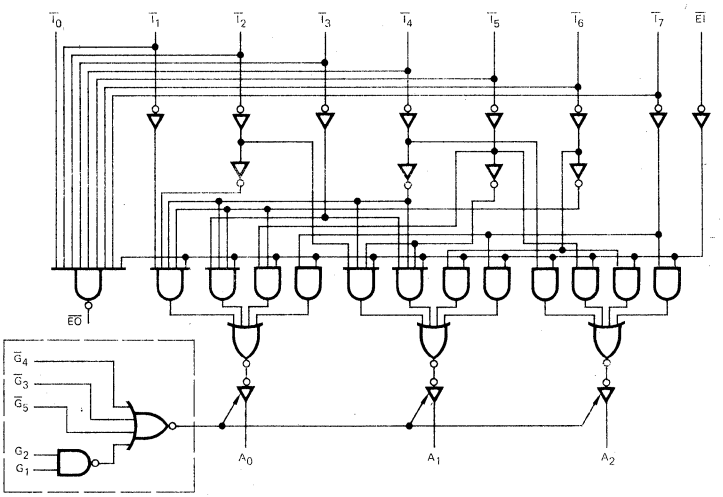
One Am2913 will accept and encode group signal lines from up to 8 Am2914's (64 levels of interrupt). Additional Am2913's may be used to encode more interrupt levels.

LOGIC SYMBOL



MPR-118

LOGIC DIAGRAM



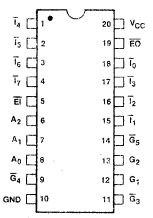
MPR-119

RELATED PRODUCTS

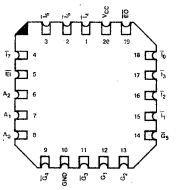
Part No.	Description
Am2914	Vectored Priority Interrupt Controller
Am25LS2513	8 to 3 Line Priority Encoder

CONNECTION DIAGRAMS – Top Views

P-20, D-20



Leadless Chip Carrier L-20-1



F-20 pin configuration identical to D-20, P-20.

MPR-120 Note: Pin 1 is marked for orientation.

Am2913
ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$	MIN. = 4.75V	MAX. = 5.25V
MIL	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$	MIN. = 4.50V	MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	MIL, $I_{OH} = -1.0mA$		2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6mA$		2.4	3.2		
			$\overline{EO}$, $I_{OH} = -440\mu A$	MIL	2.5	3.4		
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$				0.4	Volts
			$I_{OL} = 8.0mA$				0.45	
			$I_{OL} = 12mA (A_n$ Outputs)				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$	$\overline{E1}, G_1, G_2, \overline{G_3}, \overline{G_4}, \overline{G_5}, \overline{I_0}$				0.4	mA
			All others				0.8	
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$	$\overline{E1}, G_1, G_2, \overline{G_3}, \overline{G_4}, \overline{G_5}, \overline{I_0}$				20	μA
			All others				40	
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$	$\overline{E1}, G_1, G_2, \overline{G_3}, \overline{G_4}, \overline{G_5}, \overline{I_0}$				0.1	mA
			All others				0.2	
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$				−20	μA
			$V_O = 2.4V$				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				15	24	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All inputs and outputs open.

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2913PC	P-20	C	C-1
AM2913DC	D-20	C	C-1
AM2913DC-B	D-20	C	B-1
AM2913DM	D-20	M	C-3
AM2913DM-B	D-20	M	B-3
AM2913FM	F-20	M	C-3
AM2913FM-B	F-20	M	B-3
AM2913LC	L-20-1	C	C-1
AM2913LC-B	L-20-1	C	B-1
AM2913LM	L-20-1	M	C-3
AM2913LM-B	L-20-1	M	B-3
AM2913XC	Dice	C	Visual inspection to MIL-STD-883. Method 2010B.
AM2913XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Flat-Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to +70°C, $V_{CC} = 4.75$ to 5.25V, M = −55 to +125°C, $V_{CC} = 4.50$ to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.*	Max.	Units	Test Conditions
t_{PLH}	$\overline{I_i}$ to A_n (In-phase)		17	25	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}			17	25		
t_{PLH}	$\overline{I_i}$ to A_n (Out-phase)		11	17	ns	
t_{PHL}			12	18		
t_{PLH}	$\overline{I_i}$ to $\overline{EO}$		7.0	11	ns	
t_{PHL}			24	36		
t_{PLH}	$\overline{EI}$ to $\overline{EO}$		11	17	ns	
t_{PHL}			23	34		
t_{PLH}	$\overline{EI}$ to A_n		12	18	ns	
t_{PHL}			14	21		
t_{ZH}	G_1 or G_2 to A_n		23	40	ns	
t_{ZL}			20	37		
t_{ZH}	$\overline{G_3}$, $\overline{G_4}$, $\overline{G_5}$ to A_n		20	30	ns	
t_{ZL}			18	27		
t_{HZ}	G_1 or G_2 to A_n		17	27	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			19	28		
t_{HZ}	$\overline{G_3}$, $\overline{G_4}$, $\overline{G_5}$ to A_n		16	24	ns	
t_{LZ}			18	27		

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am2913 COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am2913 COM'L Max.	Am2913 MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am2913 MIL Max.	Units	Test Conditions
t_{PLH}	$\overline{I_i}$ to A_n (In-phase)		31		37	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}			30		34		
t_{PLH}	$\overline{I_i}$ to A_n (Out-phase)		22		27	ns	
t_{PHL}			22		25		
t_{PLH}	$\overline{I_i}$ to $\overline{EO}$		15		18	ns	
t_{PHL}			48		60		
t_{PLH}	$\overline{EI}$ to $\overline{EO}$		19		21	ns	
t_{PHL}			46		57		
t_{PLH}	$\overline{EI}$ to A_n		22		25	ns	
t_{PHL}			27		32		
t_{ZH}	G_1 or G_2 to A_n		42		49	ns	
t_{ZL}			43		49		
t_{ZH}	$\overline{G_3}$, $\overline{G_4}$, $\overline{G_5}$ to A_n		36		43	ns	
t_{ZL}			35		43		
t_{HZ}	G_1 or G_2 to A_n		34		40	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			34		40		
t_{HZ}	$\overline{G_3}$, $\overline{G_4}$, $\overline{G_5}$ to A_n		30		35	ns	
t_{LZ}			31		35		

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Note: i = 0 to 7
n = 0 to 2

DEFINITIONS OF FUNCTIONAL TERMS

A0, A1, A2	Three-state, active high encoder outputs
$\overline{EI}$	Enable input provided to allow cascaded operation
$\overline{EO}$	Enable output provided to enable the next lower order priority chip
G_1, G_2	Active high three-state output controls
$\overline{G}_3, \overline{G}_4, \overline{G}_5$	Active low three-state output controls
$\overline{I}_{0\text{-}7}$	Active low encoder inputs

TRUTH TABLE

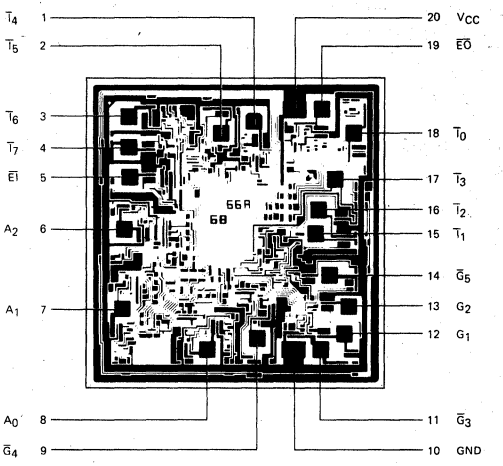
Inputs								Outputs			
$\overline{EI}$	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	A_0	A_1	A_2	$\overline{EO}$
H	X	X	X	X	X	X	X	X	L	L	L	H
L	H	H	H	H	H	H	H	H	L	L	L	L
L	X	X	X	X	X	X	X	L	H	H	H	H
L	X	X	X	X	X	X	L	H	L	H	H	H
L	X	X	X	X	X	L	H	H	H	L	H	H
L	X	X	X	X	L	H	H	H	L	L	H	H
L	X	X	X	L	H	H	H	H	H	H	L	H
L	X	X	L	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
For G_1 = H, G_2 = H, G_3 = L, G_4 = L, G_5 = L

G1	G2	$\overline{G3}$	$\overline{G4}$	$\overline{G5}$	A_0	A_1	A_2
H	H	L	L	L	Enabled		
L	X	X	X	X	Z	Z	Z
X	L	X	X	X	Z	Z	Z
X	X	H	X	X	Z	Z	Z
X	X	X	H	X	Z	Z	Z
X	X	X	X	H	Z	Z	Z

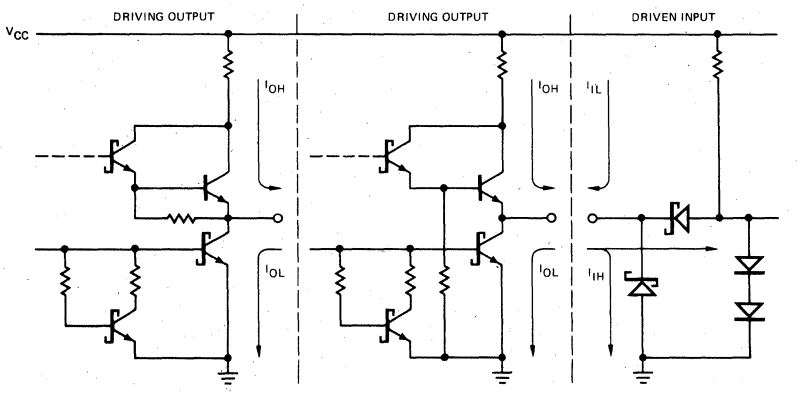
Z = HIGH Impedance

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.082" X 0.085"

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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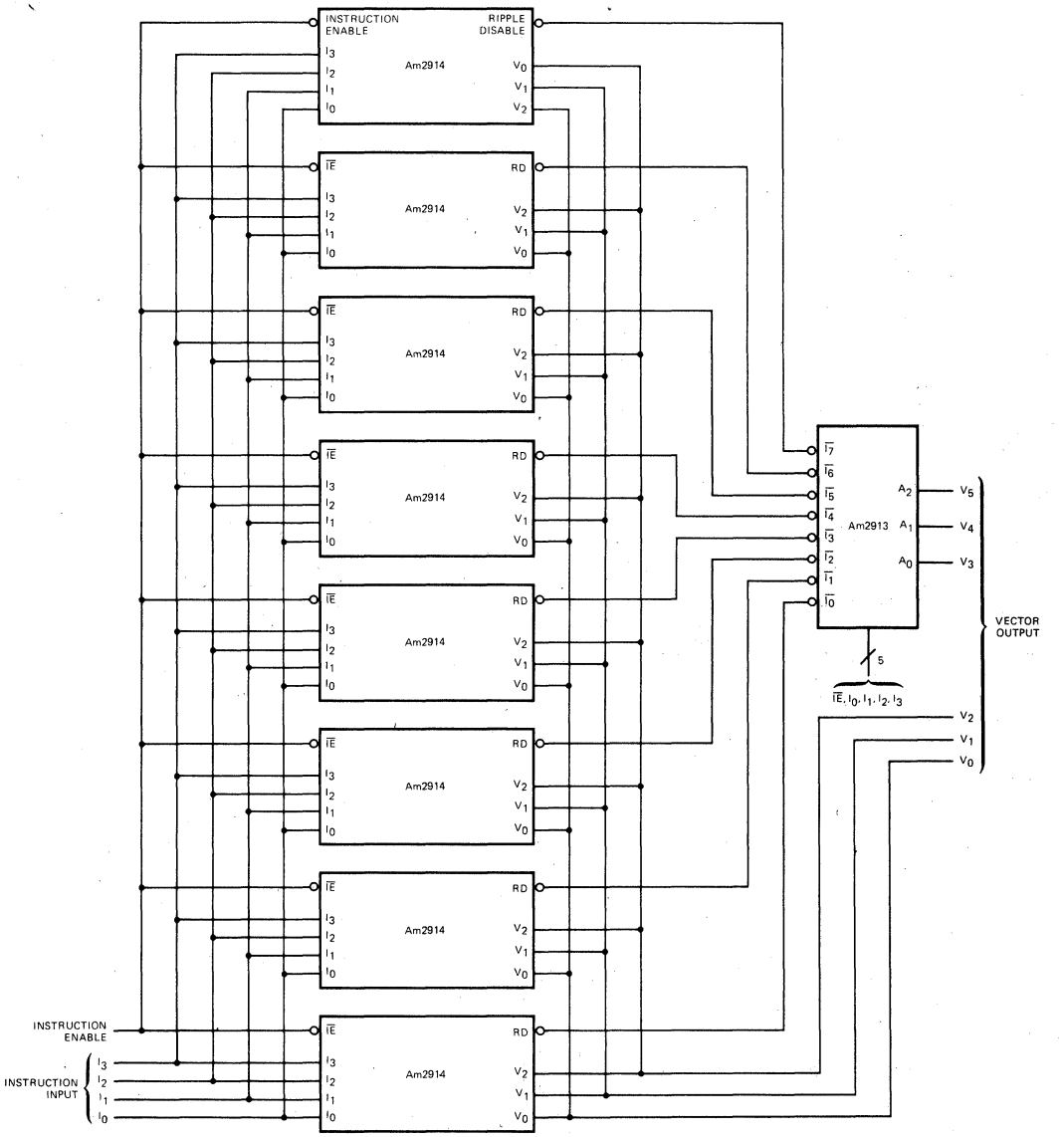


Shown above is the connection of the instruction lines and vector output lines in a 64-input priority interrupt system. The Am2913 is used to encode the most significant bits associated with the vector output.

MPR-122

Am2914

Vectored Priority Interrupt Controller

DISTINCTIVE CHARACTERISTICS

- Accepts 8 interrupt inputs
  Interrupts may be pulses or levels and are stored internally
- Built-in mask register
  Six different operations can be performed on mask register
- Built-in status register
  Status register holds code for lowest allowed interrupt
- Vectored output
  Output is binary code for highest priority un-masked interrupt
- Expandable
  Any number of Am2914's may be stacked for large interrupt systems
- Microprogrammable
  Executes 16 different microinstructions
  Instruction enable pin aids in vertical microprogramming
- High-speed operation
  Delay from an interrupt clocked into the interrupt register to interrupt request output is typically 60 ns

RELATED PRODUCTS

Part No.	Description
Am2902A	Carry Look-ahead Generator
Am2913	Priority Interrupt Expander
Am25LS138	3-to-8 Decoder
Am27S19	Mapping PROM

TABLE OF CONTENTS

For applications information, see Chapter VI of **Bit Slice Microprocessor Design**, Mick & Brick, McGraw Hill Publications.

FUNCTIONAL DESCRIPTION

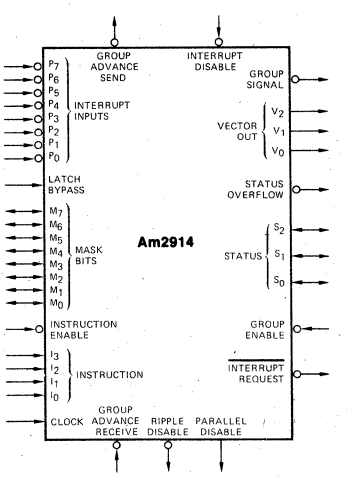
The Am2914 is a high-speed, eight-bit priority interrupt unit that is cascadable to handle any number of priority interrupt request levels. The high-speed of the Am2914 makes it ideal for use in Am2900 family microcomputer designs, but it can also be used with the Am9080A MOS microprocessor.

The Am2914 receives interrupt requests on 8 interrupt input lines (P_0-P_7). A LOW level is a request. An internal latch may be used to catch pulses on these lines, or the latch may be bypassed so the request lines drive the edge-triggered interrupt register directly. An 8-bit mask register is used to mask individual interrupts. Considerable flexibility is provided for controlling the mask register. Requests in the interrupt register are ANDed with the corresponding bits in the mask register and the results are sent to an 8-input priority encoder, which produces a three bit encoded vector representing the highest numbered input which is not masked.

An internal status register is used to point to the lowest priority at which an interrupt will be accepted. The contents of the status register are compared with the output of the priority encoder, and an interrupt request output will occur if the vector is greater than or equal to status. Whenever a vector is read from the Am2914 the status register is automatically updated to point to one level higher than the vector read. (The status register can be loaded externally or read out at any time using the S pins.) Signals are provided for moving the status upward across devices (Group Advance Send and Group Advance Receive) and for inhibiting lower priorities from higher order devices (Ripple Disable, Parallel Disable, and Interrupt Disable). A status overflow output indicates that an interrupt has been read at the highest priority.

The Am2914 is controlled by a 4-bit instruction field I_0-I_3. The command on the instruction lines is executed if IE is LOW and is ignored if IE is HIGH, allowing the 4 I bits to be shared with other devices.

LOGIC SYMBOL



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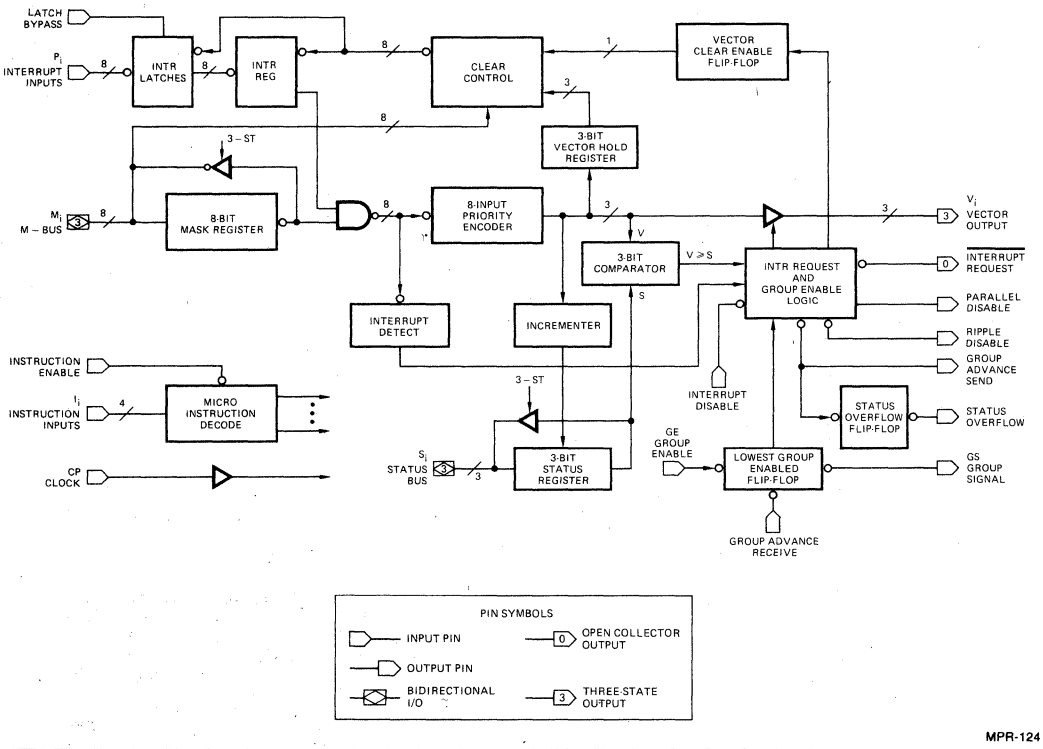
BLOCK DIAGRAM



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BLOCK DIAGRAM DESCRIPTION

The Microinstruction Decode circuitry decodes the Interrupt Microinstructions and generates required control signals for the chip.

The Interrupt Register holds the Interrupt Inputs and is an eight-bit, edge-triggered register which is set on the rising edge of the CP Clock signal.

The Interrupt latches are set/reset-type latches. When the Latch Bypass signal is LOW, the latches are enabled and act as negative pulse catchers on the inputs to the Interrupt Register. When the Latch Bypass signal is HIGH, the Interrupt latches are transparent.

The Mask Register holds the eight mask bits associated with the eight interrupt levels. The register may be loaded from or read to the M Bus. Also, the entire register or individual mask bits may be set or cleared.

The Interrupt Detect circuitry detects the presence of any unmasked Interrupt Input. The eight-input Priority Encoder determines the highest priority, non-masked Interrupt Input and forms a binary coded interrupt vector. Following a Vector Read, the three-bit Vector Hold Register holds the binary coded interrupt vector. This stored vector is used for clearing interrupts.

The three-bit Status Register holds the status bits and may be loaded from or read to the S Bus. During a Vector Read, the Incrementer increments the interrupt vector by one, and the result is clocked into the Status Register. Thus the Status Register always points to the lowest level at which an interrupt will be accepted.

The three-bit Comparator compares the Interrupt Vector with the contents of the Status Register and indicates if the Interrupt Vector is greater than or equal to the contents of the Status Register.

The Lowest Group Enabled Flip-Flop is used when a number of 2914's are cascaded. In a cascaded system, only one Lowest Group Enabled Flip-Flop is LOW at a time. It indicates the eight interrupt group, which contains the lowest priority interrupt level which will be accepted and is used to form the higher order status bits.

The Interrupt Request and Group Enable logic contain various gating to generate the Interrupt Request, Parallel Disable, Ripple Disable, and Group Advance Send signals.

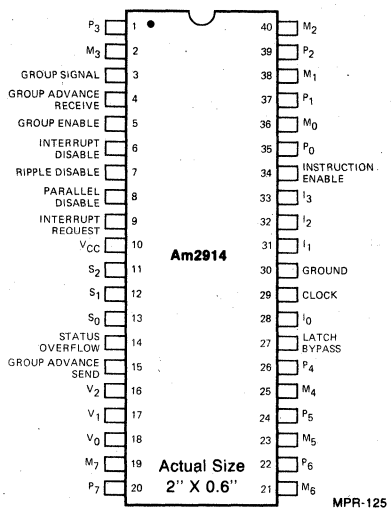
The Status Overflow signal is used to disable all interrupts. It indicates the highest priority interrupt vector has been read and the Status Register has overflowed.

The Clear Control logic generates the eight individual clear signals for the bits in the Interrupt Latches and Register. The Vector Clear Enable Flip-Flop indicates if the last vector read was from this group. When it is set, it enables the Clear Control Logic.

The CP clock signal is used to clock the Interrupt Register, Mask Register, Status Register, Vector Hold Register, and the Lowest Group Enabled, Vector Clear Enable and Status Overflow Flip-Flops, all on the clock LOW-to-HIGH transition.

CONNECTION DIAGRAMS – Top Views

D-40, P-40



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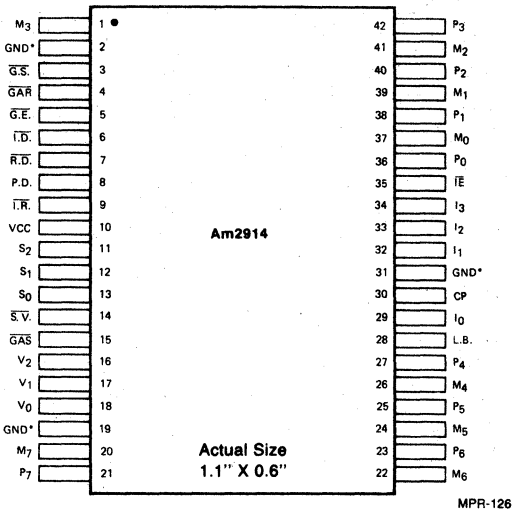
F-42-1



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*Note: GND's and pins 2, 19, 31 must all be tied together externally.

Note: Pin 1 is marked for orientation.

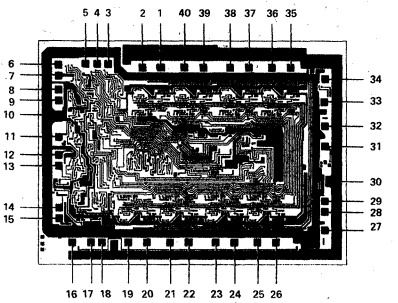
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2914PC	P-40	C	C-1
AM2914DC	D-40	C	C-1
AM2914DC-B	D-40	C	B-2 (Note 4)
AM2914DM	D-40	M	C-3
AM2914DM-B	D-40	M	B-3
AM2914FM	F-42	M	C-3
AM2914FM-B	F-42	M	B-3
AM2914LC	L-44	C	C-1
AM2914LM	L-44	M	C-3
AM2914LM-B	L-44	M	B-3
AM2914XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2914XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

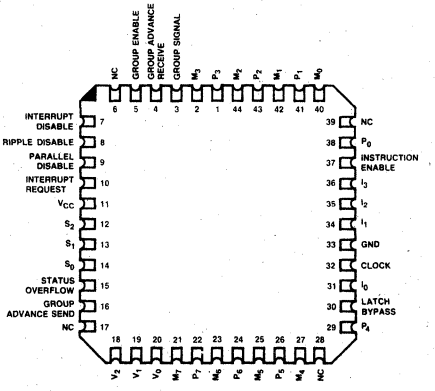
Metallization and Pad Layout



DIE SIZE
0.133" X 0.187"

Numbers correspond to DIP pin-out.

Chip-Pak™ L-44-2



STANDARD SCREENING

(Conforms to MIL-STD-883 for Class C Parts)

Step	MIL-STD-883 Method	Conditions	Level	
			Am2914PC, DC	Am2914DM, FM
Pre-Seal Visual Inspection	2010	B	100%	100%
Stabilization Bake	1008	C 24-hour 150°C	100%	100%
Temperature Cycle	1010	C −65°C to +150°C 10 cycles	100%	100%
Centrifuge	2001	B 10,000 G	100% *	100%
Fine Leak	1014	A 5×10^{-8} atm-cc/sec	100% *	100%
Gross Leak	1014	C2 Fluorocarbon	100% *	100%
Electrical Test Subgroups 1 and 7	5004	See below for definitions of subgroups	100%	100%
Insert Additional Screening here for Class B Parts				
Group A Sample Tests	5005	See below for definitions of subgroups. Maximum accept number is 3		
Subgroup 1			LTPD = 5	LTPD = 5
Subgroup 2			LTPD = 7	LTPD = 7
Subgroup 3			LTPD = 7	LTPD = 7
Subgroup 7			LTPD = 7	LTPD = 7
Subgroup 8			LTPD = 7	LTPD = 7
Subgroup 9			LTPD = 7	LTPD = 7

*Not applicable for Am2914PC.

TABLE 1

MICROINSTRUCTION SET FOR Am2914 PRIORITY INTERRUPT CIRCUIT

Decimal $I_3I_2I_1I_0$	Mnemonic	Instruction
		Mask Register Functions
14	LDM	Load mask register from M bus
7	RDM	Read mask register to M bus
12	CLRM	Clear mask register (enables all priorities)
8	SETM	Set mask register (inhibits all interrupts)
10	BCLRM	Bit clear mask register from M bus
11	BSETM	Bit set mask register from M bus
		Status Register Functions
9	LDSTA	Load status register from S bus and LGE flip-flop from GE input
6	RDSTA	Read status register to S bus
		Interrupt Request Control
15	ENIN	Enable interrupt request
13	DISIN	Disable interrupt request
		Vectored Output
5	RDVC	Read vector output to V outputs, load V+1 into status register, load V into vector hold register and set vector clear enable flip-flop.
		Priority Interrupt Register Clear
1	CLRIN	Clear all interrupts
3	CLRMR	Clear interrupts from mask register data (uses the M bus)
2	CLRMB	Clear interrupts from M bus data
4	CLRVC	Clear the individual interrupt associated with the last vector read
		Master Clear
0	MCLR	Clear all interrupts, clear mask register, clear status register, clear LGE flip-flop, enable interrupt request.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +110°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	+0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to 5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

OPERATING RANGE

P/N	Temperature	V_{CC}
Am2914PC, DC	0°C to +70°C	4.75V to 5.25V
Am2914DM, FM	−55°C to +125°C	4.50V to 5.50V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

(Group A, Subgroups 1, 2, and 3)

Am2914XC T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am2914XM T_C = −55°C to +125°C V_{CC} = 5.0V ± 10% (MIL) MIN. = 4.50V MAX. = 5.50V

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −1.0mA		2.4			Volts
			COM'L, I_{OH} = −2.6mA		2.4			
I_{CEX}	Output Leakage Current for IR Output	V_{CC} = MIN., V_O = 5.5V					250	µA
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
			I_{OL} = 12mA				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	M_{0-7}				−0.15	mA
			S_{0-2}				−0.1	
			L. B.				−0.4	
			$\overline{I. D.}$				−2.0	
			$\overline{IE}$				−1.08	
			All Others				−0.8	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	M_{0-7}				150	µA
			S_{0-2}				100	
			$\overline{GE}$, $\overline{GAR}$				40	
			$\overline{IE}$				60	
			$\overline{I. D.}$				60	
			All Others				20	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{OZL}	Off-State Output Current	V_{CC} = MAX.	V_{OUT} = 0.5V	M_{0-7}			−150	µA
				S_{0-2}			−100	
				V_{0-2}			−50	
I_{OZH}			V_{OUT} = 2.4V	M_{0-7}			150	
				S_{0-2}			100	
				V_{0-2}			50	
I_{CC}	Power Supply Current	V_{CC} = MAX.		25°C		170	286	mA
			COM'L	0°C			305	
				70°C			250	
			MIL	−55°C			310	
				125°C			200	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−30		−85	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS AT 25°C AND 5.0 VOLTS

Note: Guaranteed limits at 25°C and 5.0V are group A, subgroup 9 tests
All outputs fully loaded. C_L = 50pF. Measurements made at 1.5V with
input levels of 0V and 3.0V. All numbers are in ns.
For interrupt request output, R_L = 470Ω

TABLE I. CLOCK AND INTERRUPT INPUT PULSE WIDTHS (ns)

Time	GUARANTEED
Minimum Clock LOW Time	30
Minimum Clock HIGH Time	30
Minimum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Acceptance (Pulse Mode)	25
Maximum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Rejection (Pulse Mode)	10

TABLE II. COMBINATIONAL PROPAGATION DELAYS (ns)

	TYPICAL						GUARANTEED					
To Output / From Input	M Bus	S Bus	V_{012}	Irpt Req	Ripple Disable	Group Advance Send	M Bus	S Bus	V_{012}	Irpt Req	Ripple Disable	Group Advance Send
$\overline{IE}$	36	40	40	–	–	30	48	55	55	–	–	47
I_{0123}	36	40	40	–	–	30	48	55	55	–	–	47
Irpt. Disable	–	–	25	35	8	19	–	–	37	42	18	25

TABLE III. DELAYS FROM CLOCK TO OUTPUTS (ns)

Clock Path	TYPICAL							GUARANTEED						
	To V_{012}	To Irpt Req	To PD	To $\overline{RD}$	To $\overline{GAS}$	To Status O'flow	To $\overline{GS}$	To V_{012}	To Irpt Req	To PD	To $\overline{RD}$	To $\overline{GAS}$	To Status O'flow	To $\overline{GS}$
Irpt Latches and Register	55	65	37	39	47	–	–	67	82	57	57	66	–	–
Mask Register	55	65	37	39	47	–	–	67	82	57	57	66	–	–
Status Register	45	55	28	31	37	–	–	59	74	57	57	58	–	–
Lowest Group Enabled Flip-Flop	–	–	22	25	–	–	17	–	–	42	45	–	–	32
Irpt Request Enable Flip-Flop	–	40	–	–	–	–	–	–	56	–	–	–	–	–
Status Overflow Flip-Flop	–	–	–	–	–	17	–	–	–	–	–	–	30	–

TABLE IV. SET-UP AND HOLD TIME REQUIREMENTS (ns)

(All relative to clock LOW-to-HIGH transition)

From Input	GUARANTEED	
	Set-up Time	Hold Time
S-Bus	11	8
M-Bus	11	8
$\overline{P_0}$-$\overline{P_7}$	11	6
Latch Bypass	16	0
$\overline{IE}$ I_{0123} (See Note)	46 t_{pwL} + 29	0
$\overline{GE}$	11	11
$\overline{GAR}$	11	11
$\overline{Irpt\ Disable}$	35	0
P_0-P_7 Hold Time Relative to LB	–	21

Note: t_{pwL} is the Clock LOW Time. Both Set-up times must be met.

SWITCHING CHARACTERISTICS OVER OPERATING VOLTAGE AND TEMPERATURE RANGE

(Group A, subgroup 10 and 11 tests and limits)

All outputs fully loaded, C_L = 50pF. Measurements made at 1.5V with input levels of 0 and 3.0V. For Interrupt Request Output, R_L = 390Ω, V_{LOAD} = 5.0V

TABLE I. CLOCK AND INTERRUPT INPUT PULSE WIDTHS (ns)

Time	Am2914PC, DC, XC T_A = 0°C to +70°C, 5V ± 5%	Am2914DM, FM, XM T_C = –55°C to +125°C, 5V ± 10%
Minimum Clock LOW Time	30	30
Minimum Clock HIGH Time	30	30
Minimum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Acceptance (Pulse Mode)	40	40
Maximum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Rejection (Pulse Mode)	8	8
Minimum Clock Period, $\overline{IE}$ = H on current cycle and previous cycle	50	55
Minimum Clock Period, $\overline{IE}$ = L on current cycle or previous cycle	100	110

TABLE II. MAXIMUM COMBINATIONAL PROPAGATION DELAYS (ns)

	Am2914PC, DC, XC T_A = 0°C to +70°C, 5V ± 5%						Am2914DM, FM, XM T_C = –55°C to +125°C, 5V ± 10%					
To Output / From Input	M Bus	S Bus	V_{012}	Irpt Req	Ripple Disable	Group Advance Send	M Bus	S Bus	V_{012}	Irpt Req	Ripple Disable	Group Advance Send
$\overline{IE}$	52	60	65	–	–	56	60	68	70	–	–	62
I_{0123}	52	60	65	–	–	56	60	68	70	–	–	62
Irpt. Disable	–	–	45	52	20	30	–	–	48	60	22	33

TABLE III. MAXIMUM DELAYS FROM CLOCK TO OUTPUTS (ns)

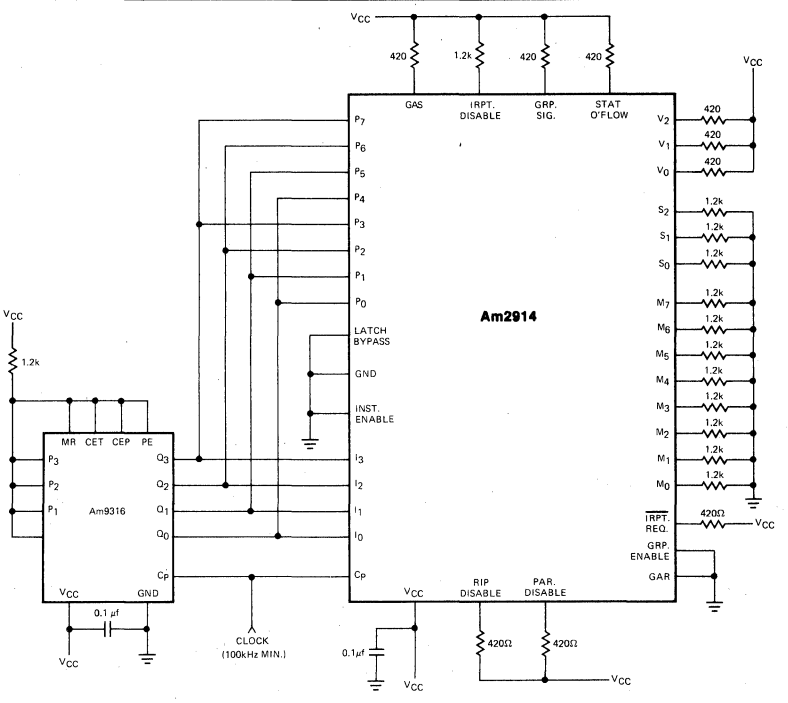
Clock Path	Am2914PC, DC, XC T_A = 0°C to +70°C, 5V ± 5%							Am2914DM, FM, XM T_C = –55°C to +125°C, 5V ± 10%						
	To V_{012}	To Irpt Req	To PD	To $\overline{RD}$	To $\overline{GAS}$	To Status O'flow	To $\overline{GS}$	To V_{012}	To Irpt Req	To PD	To $\overline{RD}$	To $\overline{GAS}$	To Status O'flow	To $\overline{GS}$
Irpt Latches and Register	76	97	67	67	80	–	–	82	105	75	75	85	–	–
Mask Register	76	97	67	67	80	–	–	82	105	75	75	85	–	–
Status Register	67	88	63	63	70	–	–	73	96	66	66	76	–	–
Lowest Group Enabled Flip-Flop	–	–	48	52	–	–	38	–	–	54	58	–	–	45
Irpt Request Enable Flip-Flop	–	62	–	–	–	–	–	–	66	–	–	–	–	–
Status Overflow Flip-Flop	–	–	–	–	–	35	–	–	–	–	–	–	40	–

TABLE IV. SETUP AND HOLD TIME REQUIREMENTS (ns)

(All relative to clock LOW-to-HIGH transition)

From Input	Am2914PC, DC, XC T_A = 0°C to +70°C, 5V ± 5%		Am2914DM, FM, XM T_C = –55°C to +125°C, 5V ± 10%	
	Set-Up Time	Hold Time	Set-Up Time	Hold Time
S-Bus	15	10	15	10
M-Bus	15	10	15	10
$\overline{P_0}$-$\overline{P_7}$	15	8	15	8
Latch Bypass	20	0	20	0
$\overline{IE}$ I_{0123} (See Note)	55 t_{pwL} + 33	0	55 t_{pwL} + 40	0
$\overline{GE}$	15	13	15	13
$\overline{GAR}$	15	13	15	13
$\overline{Irpt\ Disable}$	42	0	42	0
P_0–P_7 Hold Time Relative to LB	—	25	—	25

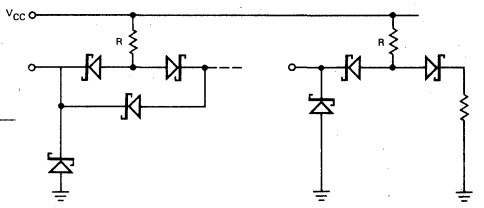
Note: t_{pwL} is the Clock LOW Time. Both Set-up times must be met.



Am2914 Burn-in Circuit

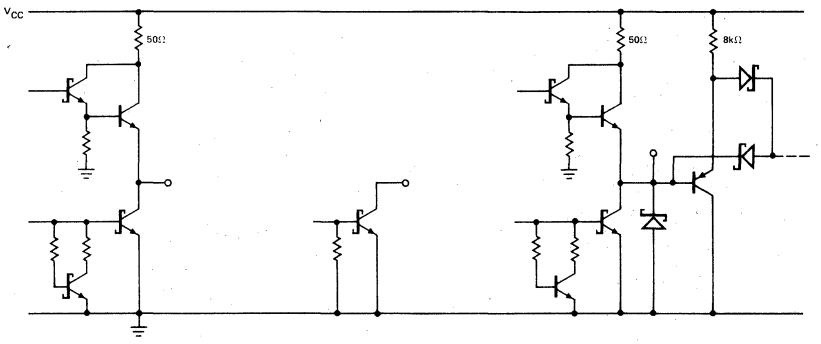
MPR-127

INPUT/OUTPUT CIRCUITS



INPUT	R
I_0-I_3, CP, $\overline{GE}$, $\overline{GAR}$	10K
$\overline{LB}$	20K
$\overline{IE}$	6.7K
$\overline{ID}$	4K

INPUT	R
$\overline{P_7}$-$\overline{P_0}$	10K



OUTPUTS	
V_0-V_3	$\overline{SO}$
$\overline{GAS}$	PD
$\overline{GS}$	$\overline{RD}$

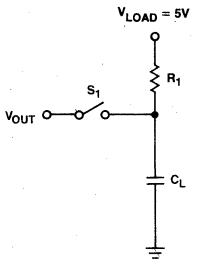
OUTPUT
$\overline{IR}$

OUTPUTS
M_0-M_7
S_0-S_3

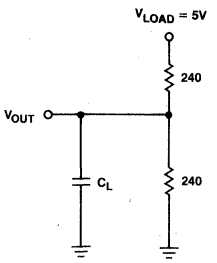
MPR-128

TEST OUTPUT LOAD CONFIGURATIONS FOR Am2914

C. OPEN-COLLECTOR OUTPUTS



D. THREE-STATE OUTPUTS



TEST OUTPUT LOADS FOR Am2914

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
3	Group Signal	C	2K	–
4	Group Advance Receive	C	2K	–
7	Ripple Disable	C	2K	–
8	Parallel Disable	C	2K	–
9	Interrupt Request	C	390	–
13-11	S_{0-2}	D	240	240
14	Status Overflow	C	2K	–
18-16	V_{0-2}	D	240	240
–	M_{0-7}	D	240	240

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5–8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

A Microprogrammable, Bipolar, LSI Interrupt Structure Using the Am2914

INTRODUCTION

Advanced Micro Devices' introduction of the Am2914 Vectored Priority Interrupt Controller now makes possible the structuring of a microprogrammable bipolar LSI interrupt system. The design engineer may use the Am2914 to simplify his design process, dramatically reduce the system cost, size and package count, and increase the speed, capability and reliability of his interrupt system.

The Am2914 is a modular, low cost, standard LSI component that may be microprogrammed to meet the requirements of specific applications. Today's engineer may utilize the Am2914 microprogrammability to provide functional flexibility and ease of engineering change, while taking advantage of its modularity to provide hardware regularity and future expansion capability.

THE INTERRUPT CONCEPT

In any state machine, a requirement exists for the efficient synchronization and response to asynchronous events such as power failure, machine malfunctions, control panel service requests, external timer signals, supervisory calls, program errors, and input/output device service requests. The merit of such an "asynchronous event handler" may be measured in terms of response time, system throughput, real time overhead, hardware cost and memory space required.

The simplest approach to asynchronous event handling is the poll approach. A status indicator is associated with each possible asynchronous event. The processor tests each indicator in sequence and, in effect, "asks" if service is required. This program-driven method is inefficient for a number of reasons. Much time is consumed polling when no service is required; programs must have frequent test points to poll indicators, and since indicators are polled in sequence, considerable time may elapse before the processor responds to an event. Thus, system throughput is low; real time overhead and response time are high, and a large memory space is required.

The interrupt method is a much more efficient way of servicing asynchronous requests. An asynchronous event requiring service generates an interrupt request signal to the processor. When the processor receives the interrupt request, it may suspend the program it is currently executing, execute an interrupt service routine which services the asynchronous request, then resume the execution of the suspended program. In this system, the execution of the service routine is initiated by an interrupt request; thus, the system is interrupt driven and service routines are executed only when service is requested. Although hardware cost may be higher in this type of system, it is more efficient since system throughput is higher, response time is faster, real time overhead is lower and less memory space is required.

INTERRUPT SYSTEM FUNCTIONAL DEFINITION

A complete and clear functional definition is key to the design of a good interrupt system. The following features are useful.

Multiple Interrupt Request Handling: Since interrupt requests are generated from a number of different sources, the interrupt system's ability to handle interrupt requests from several sources is important.

Interrupt Request Prioritization: Since the processor can service only one interrupt request at a time, it is important that the interrupt system has the ability to prioritize the requests and determine which has the highest priority.

Interrupt Service Routine "Nesting": This feature allows an interrupt service routine for a given priority request to be interrupted in turn, but only by a higher priority interrupt request. The service routine for the higher priority request is executed, then the execution of the interrupted service routine is resumed. If there are "n" interrupt requests, an "n" deep "nest" is possible.

Dynamic Interrupt Enabling/Disabling: The ability to enable/disable all interrupts "on the fly" under microprogram control can be used to prevent interruption of certain processes.

Dynamic Interrupt Request Masking: The ability to selectively inhibit or "mask" individual interrupt requests under microprogram control is useful.

Interrupt Request Vectoring: Many times, a particular interrupt request requires the execution of a unique interrupt service routine. For this reason, the generation of a unique binary coded vector for each interrupt request is very helpful. This vector can be used as a pointer to the start of a unique service routine.

Interrupt Request Priority Threshold: The ability to establish a priority threshold is valuable. In this type of operation, only those interrupt requests which have higher priority than a specified threshold priority are accepted. The threshold priority can be defined by microprogram or can be automatically established by hardware at the interrupt currently being serviced plus one. This automatic threshold prevents multiple interrupts from the same source. Also useful is the ability to read the threshold priority under microprogram control. Thus, the interrupt request being serviced may be determined by the microprogram.

Interrupt Request Clearing Flexibility: Flexibility in the method of clearing interrupt requests allows different modes of interrupt system operation. Of particular value are the abilities to clear the interrupt currently being serviced, clear all interrupts, or clear interrupts via a programmable mask register or bus.

Microprogrammability: Microprogrammability permits the construction of a general purpose or "universal" interrupt structure which can be microprogrammed to meet a specific application's requirements. The universality of the structure allows standardization of the hardware and amortization of the hardware development costs across a much broader user base. The end result is a flexible, low cost interrupt structure.

Hardware Modularity: Modular interrupt system hardware is beneficial in two ways. First, hardware modularity provides expansion capability. Additional modules may be added as the need to service additional requests arises. Secondly, hardware modularity provides a structural regularity which simplifies the system structure and also reduces the number of hardware part numbers.

Fast Interrupt System Response Time: Quick interrupt system response provides more efficient system operation. Fast response reduces real time overhead and increases overall system throughput.

INTERRUPT SYSTEM IMPLEMENTATION USING THE Am2914

The Am2914 provides all of the foregoing features on a single LSI chip. The Am2914 is a high-speed, eight-bit priority interrupt unit that is cascadable to handle any number of priority interrupt request levels. The Am2914's high speed is ideal for use in Am2900 Family microcomputer designs, but it can also be used with the Am9080A MOS microprocessor.

The Am2914 receives interrupt requests on eight Interrupt Input lines (P_0-P_7). A LOW level is a request. An internal latch may be used to catch pulses (HIGH-LOW-HIGH) on these lines, or the latch may be bypassed so that the request lines drive the D-inputs to the edge-triggered Interrupt Register directly. An eight-bit Mask Register is used to mask individual interrupts. Considerable flexibility is provided for controlling the Mask Register. Requests in the Interrupt Register (P_0-P_7) are ANDed with the corresponding bits in the mask register (M_0-M_7) and the results are sent to an eight-input priority encoder, which produces a three-bit encoded vector representing the highest priority input which is not masked.

An internal Status Register is used to point to the lowest priority at which an interrupt will be accepted. The contents of the Status Register are compared with the output of the priority encoder, and an Interrupt Request output will occur if the vector is greater than or equal to the contents of the Status Register. Whenever a vector is read from the Am2914, the Status Register is automatically updated to point to one level higher than the vector read. (The Status Register can be loaded externally or read out at any time using the S-Bus.) Signals are provided for moving the status upward across devices (Group Advance Send and Group Advance Receive) and for inhibiting lower priorities from higher order devices (Ripple Disable, Parallel Disable, and Interrupt Disable). A Status Overflow output indicates that an interrupt has been read at the highest priority.

The Am2914 is controlled by a four-bit microinstruction field I_0-I_3. The microinstruction is executed if $\overline{IE}$ (Instruction Enable) is LOW and is ignored if $\overline{IE}$ is HIGH, allowing the four I bits to be shared with other functions. Sixteen different microinstructions are executed. Figure 2 shows the microinstructions and the microinstruction codes.

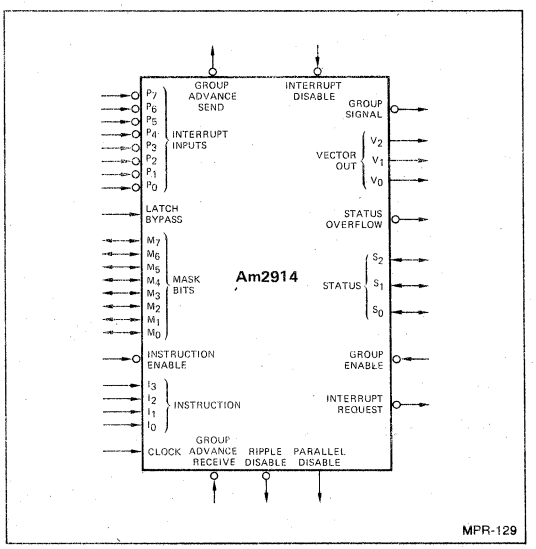


Figure 1. Am2914 Logic Symbol.

MICROINSTRUCTION DESCRIPTION	MICROINSTRUCTION CODE $I_3I_2I_1I_0$
MASTER CLEAR	0000
CLEAR ALL INTERRUPTS	0001
CLEAR INTERRUPTS FROM M-BUS	0010
CLEAR INTERRUPTS FROM MASK REGISTER	0011
CLEAR INTERRUPT, LAST VECTOR READ	0100
READ VECTOR	0101
READ STATUS REGISTER	0110
READ MASK REGISTER	0111
SET MASK REGISTER	1000
LOAD STATUS REGISTER	1001
BIT CLEAR MASK REGISTER	1010
BIT SET MASK REGISTER	1011
CLEAR MASK REGISTER	1100
DISABLE INTERRUPT REQUEST	1101
LOAD MASK REGISTER	1110
ENABLE INTERRUPT REQUEST	1111

Figure 2. Am2914 Microinstruction Set.

In this microinstruction set, the *Master Clear* microinstruction is selected as binary zero so that during a power up sequence, the microinstruction register in the microprogram control unit of the central processor can be cleared to all zeros. Thus, on the next clock cycle, the Am2914 will execute the *Master Clear* function. This includes clearing the Interrupt Latches and Register as well as the Mask Register and Status Register. The LGE flip-flop of the least significant group is set LOW because the Group Advance Receive input is tied LOW. All other Group Advance Receive inputs are tied to Group Advance Send outputs and these are forced HIGH during this instruction. This clear instruction also sets the Interrupt Request Enable flip-flop so that a fully interrupt driven system can be easily initiated from any interrupt.

The *Clear All Interrupts* microinstruction clears the Interrupt Latches and Register.

The *Clear Interrupts from Mask Register* microinstruction clears those Interrupt Latches and Register bits which have corresponding Mask Register bits set equal to one. The M-Bus is used by the Am2914 during the execution of this microinstruction and must be floating.

The *Clear Interrupts from M-Bus* microinstruction clears those Interrupt Latches and Register bits which have corresponding M-Bus bits set equal to one.

The *Clear Interrupt, Last Vector Read* microinstruction clears the Interrupt Latch and Register bit associated with the last vector read.

The *Read Vector* microinstruction is used to read the vector value of the highest priority request causing the interrupt. The vector outputs are three-state drivers that are enabled onto the $V_0V_1V_2$ bus during this instruction. This microinstruction also automatically loads the value "vector plus one" into the Status Register. In addition, this instruction sets the Vector Clear Enable flip-flop and loads the current vector value into the Vector Hold Register so that this value can be used by the *Clear Interrupt, Last Vector Read* microinstruction. This allows the user to read the vector associated with the interrupt, and at some later time clear the Interrupt Latch and Register bit associated with the vector read.

The *Load Status Register* microinstruction loads S-Bus data into the Status Register and also loads the LGE flip-flop from the Group Enable input.

During the *Read Status Register* microinstruction, the Status Register outputs are enabled onto the Status Bus (S_0-S_2). The Status Bus is a three-bit, bi-directional, three-state bus.

The *Load Mask Register* microinstruction loads data from the three-state, bi-directional M-Bus into the Mask Register.

The *Read Mask Register* microinstruction enables the Mask Register outputs onto the bi-directional, three-state M-Bus.

The *Set Mask Register* microinstruction sets all the bits in the Mask Register to one. This results in all interrupts being inhibited.

The entire Mask Register is cleared by the *Clear Mask Register* microinstruction. This enables all interrupts subject to the Interrupt Enable flip-flop and the Status Register.

The *Bit Clear Mask Register* microinstruction may be used to selectively clear individual Mask Register bits. This microinstruction clears those Mask Register bits which have corresponding M-Bus bits equal to one. Mask Register bits with corresponding M-Bus bits equal to zero are not affected.

The *Bit Set Mask Register* microinstruction sets those Mask Register bits which have corresponding M-Bus bits equal to one. Other Mask Register bits are not affected.

All Interrupt Requests may be disabled by execution of the *Disable Interrupt Request* microinstruction. This microinstruction resets an Interrupt Request Enable flip-flop on the chip.

The *Enable Interrupt Request* microinstruction sets the Interrupt Enable flip-flop. Thus, Interrupt Requests are enabled subject to the contents of the Mask and Status Registers.

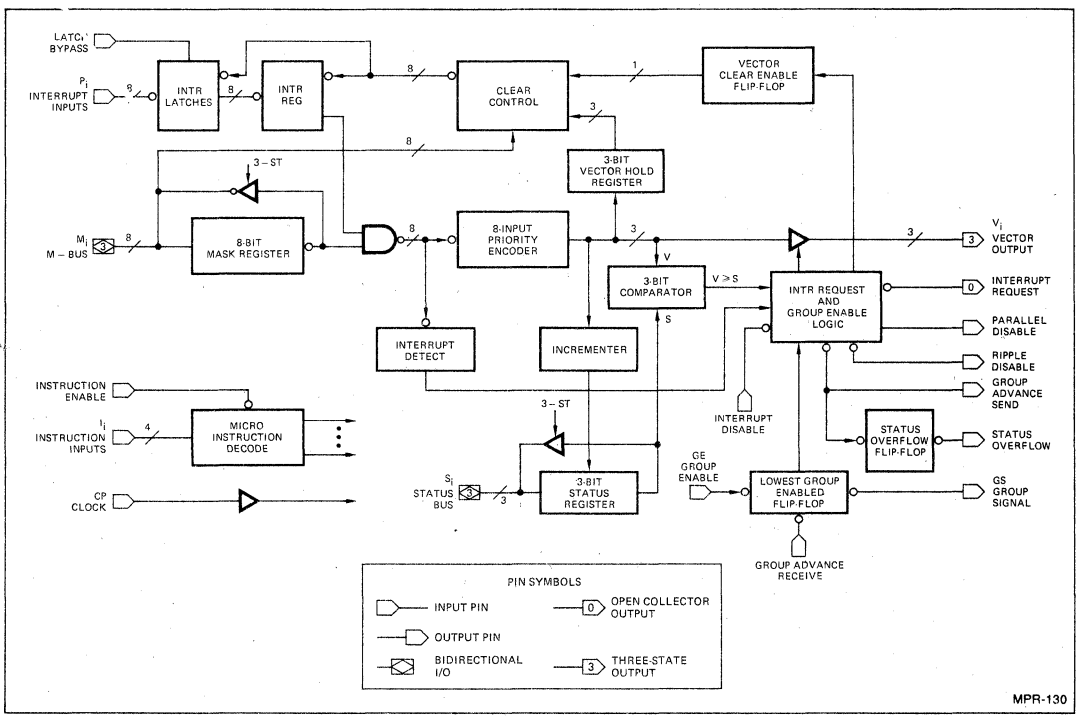


Figure 3. Am2914 Block Diagram.

Am2914 BLOCK DIAGRAM DESCRIPTION

The Am2914 block diagram is shown in Figure 3. The Micro-instruction Decode circuitry decodes the Interrupt Micro-instructions and generates required control signals for the chip.

The Interrupt Register holds the Interrupt Inputs and is an eight-bit, edge-triggered register which is set on the rising edge of the CP Clock signal if the Interrupt Input is LOW.

The Interrupt latches are set/reset latches. When the Latch Bypass signal is LOW, the latches are enabled and act as negative pulse catchers on the inputs to the Interrupt Register. When the Latch Bypass signal is HIGH, the Interrupt latches are transparent.

The Mask Register holds the eight mask bits associated with the eight interrupt levels. The register may be loaded from or read to the M-Bus. Also, the entire register or individual mask bits may be set or cleared.

The Interrupt Detect circuitry detects the presence of any unmasked Interrupt Input. The eight-input Priority Encoder determines the highest priority, non-masked Interrupt Input and forms a binary coded interrupt vector. Following a Vector Read, the three-bit Vector Hold Register holds the binary coded interrupt vector. This stored vector can be used later for clearing interrupts.

The three-bit Status Register holds the status bits and may be loaded from or read to the S-Bus. During a Vector Read, the Incrementer increments the interrupt vector by one, and the result is clocked into the Status Register. Thus, the Status Register points to a level one greater than the vector just read.

The three-bit Comparator compares the Interrupt Vector with the contents of the Status Register and indicates if the Interrupt Vector is greater than or equal to the contents of the Status Register.

The Lowest Group Enabled Flip-Flop is used when a number of Am2914's are cascaded. In a cascaded system, only one Lowest Group Enabled Flip-Flop is LOW at a time. It indicates the eight interrupt group, which contains the lowest priority interrupt level which will be accepted and is used to form the higher order status bits.

The Interrupt Request and Group Enable logic contain various gating to generate the Interrupt Request, Parallel Disable, Ripple Disable, and Group Advance Send signals.

The Status Overflow signal is used to disable all interrupts. It indicates the highest priority interrupt vector has been read and the Status Register has overflowed.

The Clear Control logic generates the eight individual clear signals for the bits in the Interrupt Latches and Register. The Vector Clear Enable Flip-Flop indicates if the last vector read was from this chip. When it is set it enables the Clear Control Logic.

The CP clock signal is used to clock the Interrupt Register, Mask Register, Status Register, Vector Hold Register, and the Lowest Group Enabled, Vector Clear Enable and Status Overflow Flip-Flops, all on the clock LOW-to-HIGH transition.

The Am2914 can be microprogrammed in many different ways. Figure 4 shows an example interrupt sequence. The *Read Vector* microinstruction is necessary in order to read the interrupt priority level. Since vector plus one is automatically loaded into the Status Register when a *Read Vector* microinstruction is executed, the Status Register possibly will overflow and disable all interrupts. For this reason, the Status Register must be reloaded periodically. The other Am2914 microinstructions are optional.

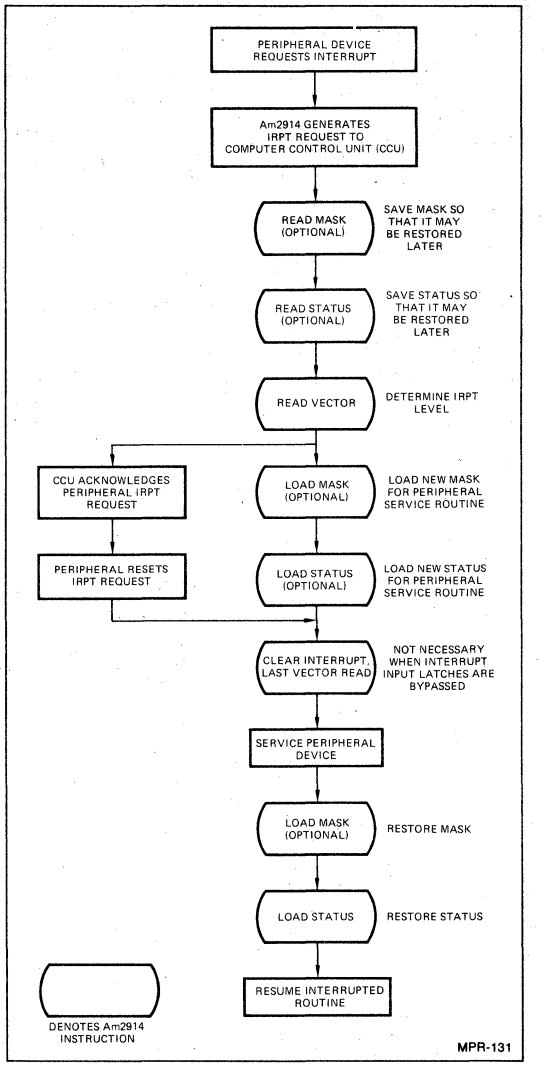


Figure 4. Example Interrupt Sequence.

CASCADING THE Am2914

A number of input/output signals are provided for cascading the Am2914 Vectored Priority Interrupt Encoder. A definition of these I/O signals and their required connections follows:

Group Signal ($\overline{GS}$) – This signal is the output of the Lowest Group Enabled flip-flop and during a Read Status micro-instruction is used to generate the high order bits of the Status word.

Group Enable ($\overline{GE}$) – This signal is one of the inputs to the Lowest Group Enable flip-flop and is used to load the flip-flop during the Load Status microinstruction.

Group Advance Send ($\overline{GAS}$) – During a Read Vector microinstruction, this output signal is LOW when the highest priority vector (vector seven) of the group is being read. In a cascaded system Group Advance Send must be tied to the Group Advance Receive input of the next higher group in order to transfer status information.

Group Advance Receive ($\overline{GAR}$) – During a Master Clear or Read Vector microinstruction, this input signal is used with other internal signals to load the Lowest Group Enabled flip-flop. The Group Advance Receive input of the lowest priority group must be tied to ground.

Status Overflow ($\overline{SV}$) – This output signal becomes LOW after the highest priority vector (vector seven) of the group has been read and indicates the Status Register has overflowed. It stays LOW until a Master Clear or Load Status microinstruction is executed. The Status Overflow output of the highest priority group should be connected to the Interrupt Disable input of the same group and serves to disable all interrupts until new status is loaded or the system is master cleared. The Status Overflow outputs of lower priority groups should be left open (see Figure 7).

Interrupt Disable ($\overline{ID}$) – When LOW, this input signal inhibits the Interrupt Request output from the chip and also generates a Ripple Disable output.

Ripple Disable ($\overline{RD}$) – This output signal is used only in the Ripple Cascade Mode (see below). The Ripple Disable output is LOW when the Interrupt Disable input is LOW, the Lowest Group Enabled flip-flop is LOW, or an Interrupt Request is generated in the group. In the ripple cascade mode, the

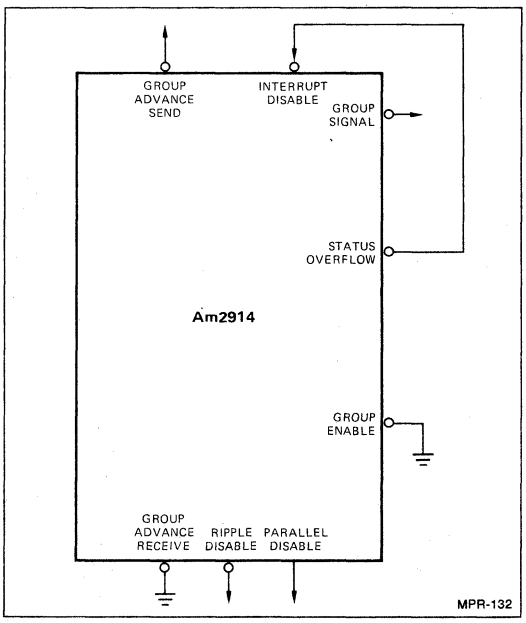


Figure 5. Cascade Lines Connection for Single Chip System.

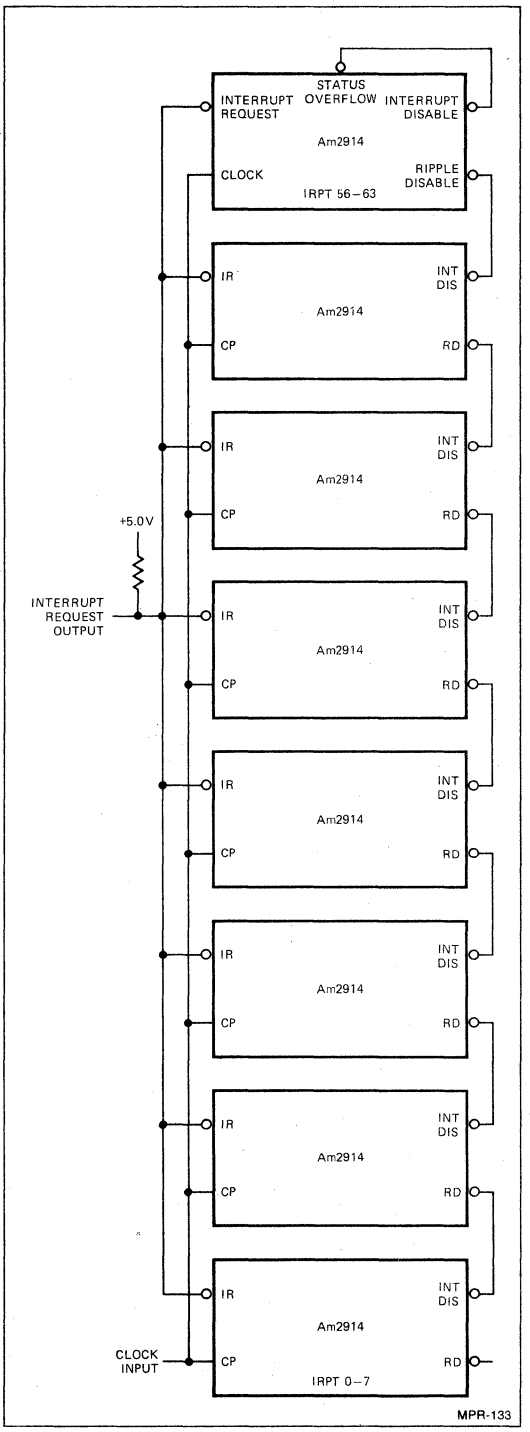


Figure 6. Interrupt Disable Connections for Ripple Cascade Mode.

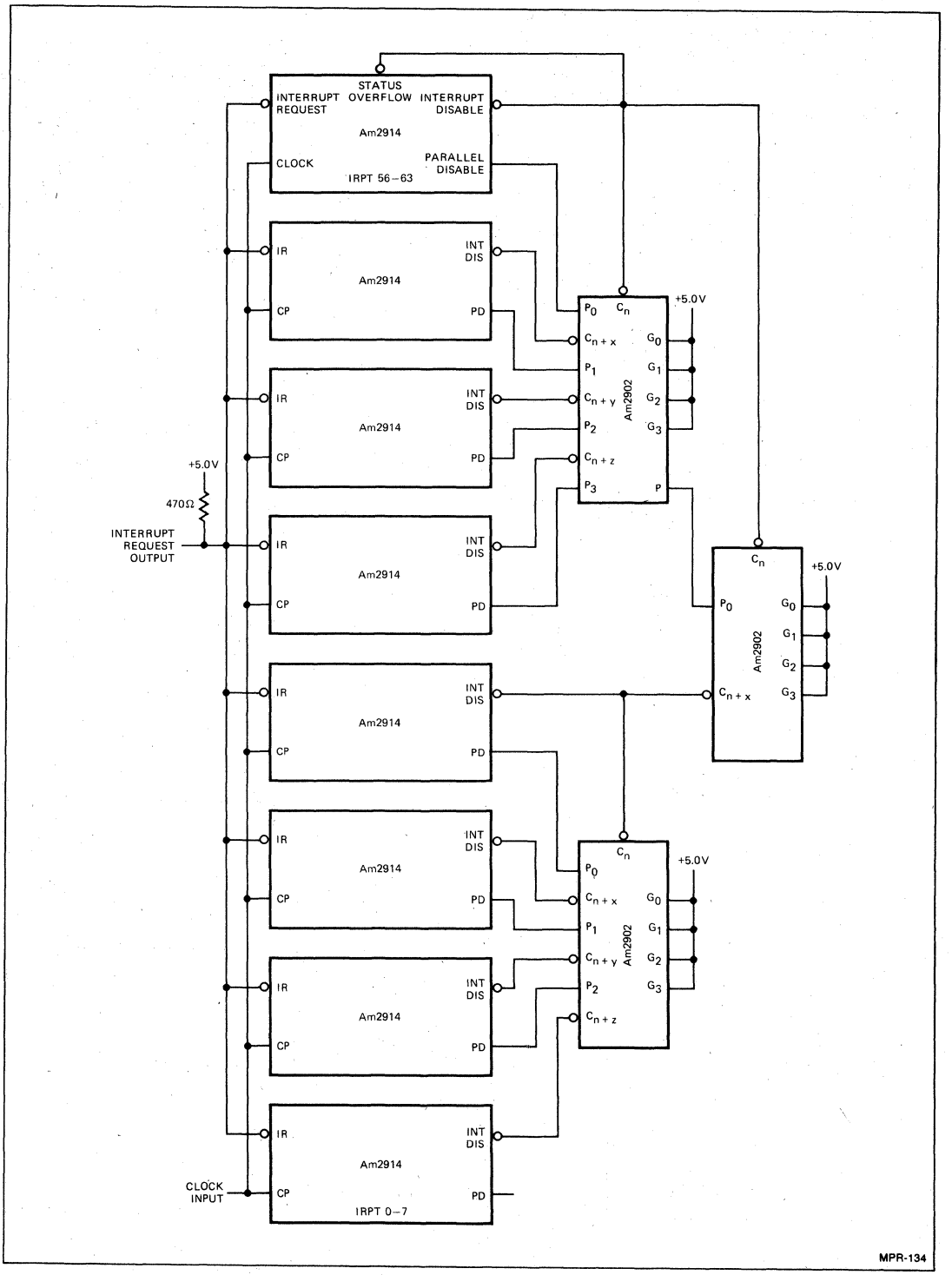


Figure 7. Interrupt Disable Connections for Parallel Cascade Mode.

Ripple Disable output is tied to the Interrupt Disable input of the next lower priority group (see Figure 6).

Parallel Disable (PD) – This output is used only in the parallel cascade mode (see below). It is HIGH when the Lowest Group Enabled flip-flop is LOW or an Interrupt Request is generated in the group. It is not affected by the Interrupt Disable input.

A single Am2914 chip may be used to prioritize and encode up to eight interrupt inputs. Figure 5 shows how the above cascade lines should be connected in such a single chip system.

The Group Advance Receive and Group Enable inputs should be connected to ground so that the Lowest Group Enabled flip-flop is forced LOW during a *Master Clear* or *Load Status* microinstruction. Status Overflow should be connected to Interrupt Disable in order to disable interrupts when vector seven is read. The Group Advance Send, Ripple Disable, Group Signal and Parallel Disable pins should be left open.

The Am2914 may be cascaded in either a Ripple Cascade Mode or a Parallel Cascade Mode. In the Ripple Cascade Mode, the Interrupt Disable signal, which disables lower priority interrupts, is allowed to ripple through lower priority groups. Figures 6, 9 and 11 show the cascade connections required for a ripple cascade 64 input interrupt system.

In the parallel cascade mode, a parallel lookahead scheme is employed using the high-speed Am2902 Lookahead Carry Generator. Figures 7, 9 and 10 show the cascade connections required for a parallel cascade 64-input interrupt system. For this application, the Am2902 is used as a lookahead interrupt disable generator. A Parallel Disable output from any group results in the disabling of all lower priority groups in parallel. Figure 8 shows the Am2902 logic diagram and equations.

In Figures 9 and 10, the Am2913 Priority Interrupt Expander is shown forming the high order bits of the vector and status, respectively. The Am2913 is an eight-line to three-line priority encoder with three-state outputs which are enabled by the five output control signals G1, G2, $\overline{G3}$, $\overline{G4}$, and $\overline{G5}$. In Figure 9, the Am2913 is connected so that its outputs are enabled during a Read Vector instruction, and in Figure 10 the Am2913 is connected so that its outputs are enabled during a Read Status instruction. The Am2913 logic diagram and truth table are shown in Figure 11.

The Am25LS138 three-line to eight-line Decoder also is shown in Figure 10. It is used to decode the three high order status bits during a Load Status instruction. The Am25LS138 logic diagram and truth table are shown in Figure 12.

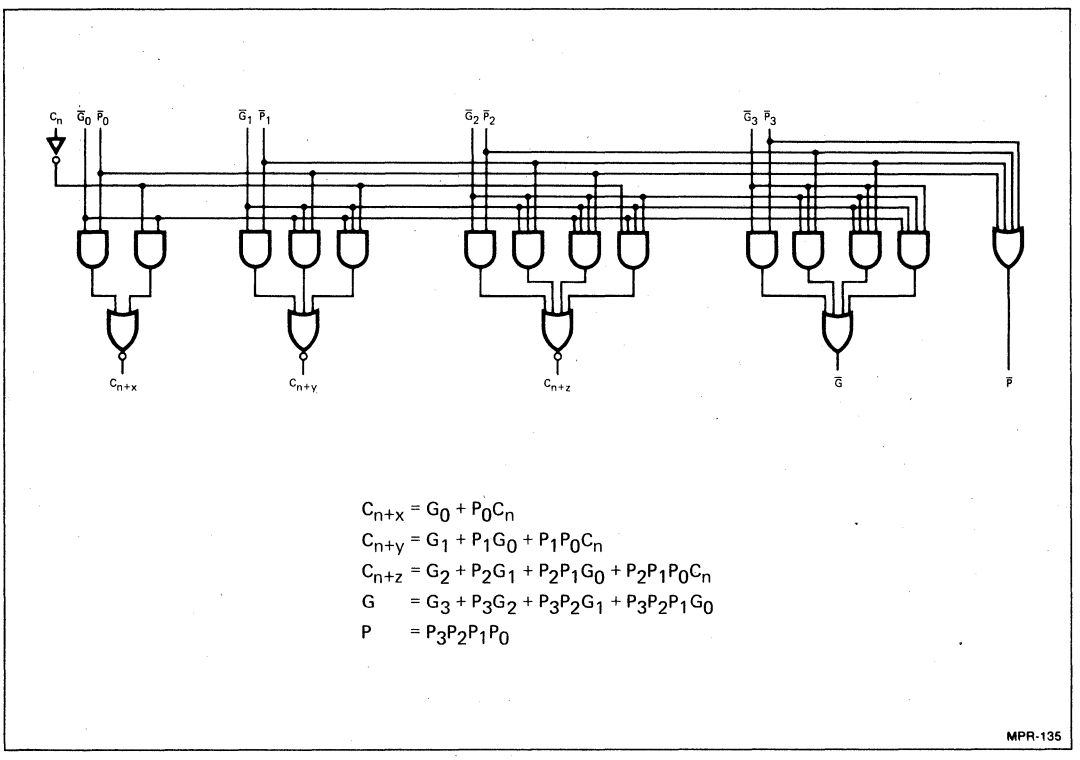


Figure 8. Am2902 Carry Look-Ahead Generator Logic Diagram and Equations.

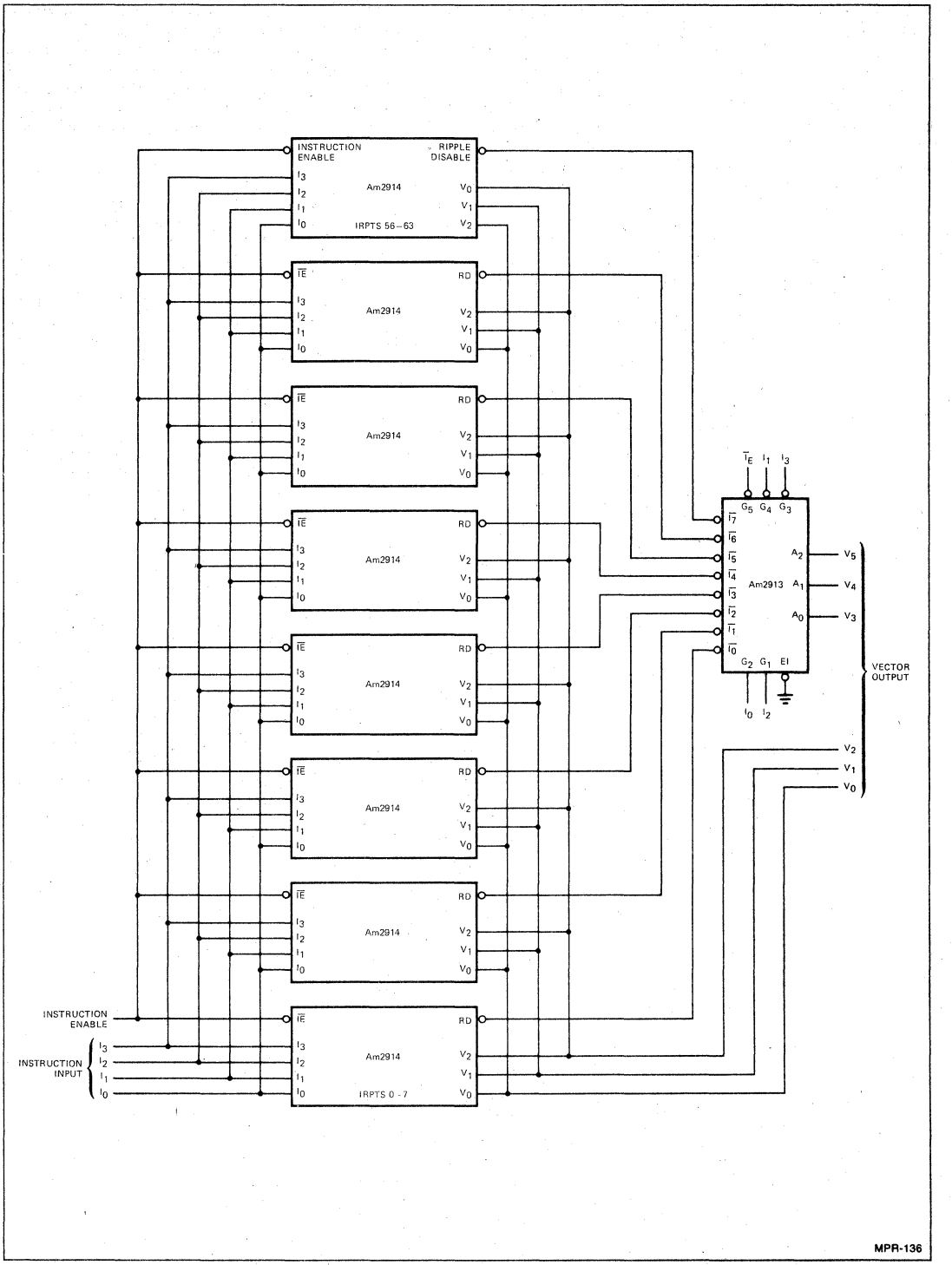


Figure 9. Vector Connections for both the Parallel and Ripple Cascade Modes.

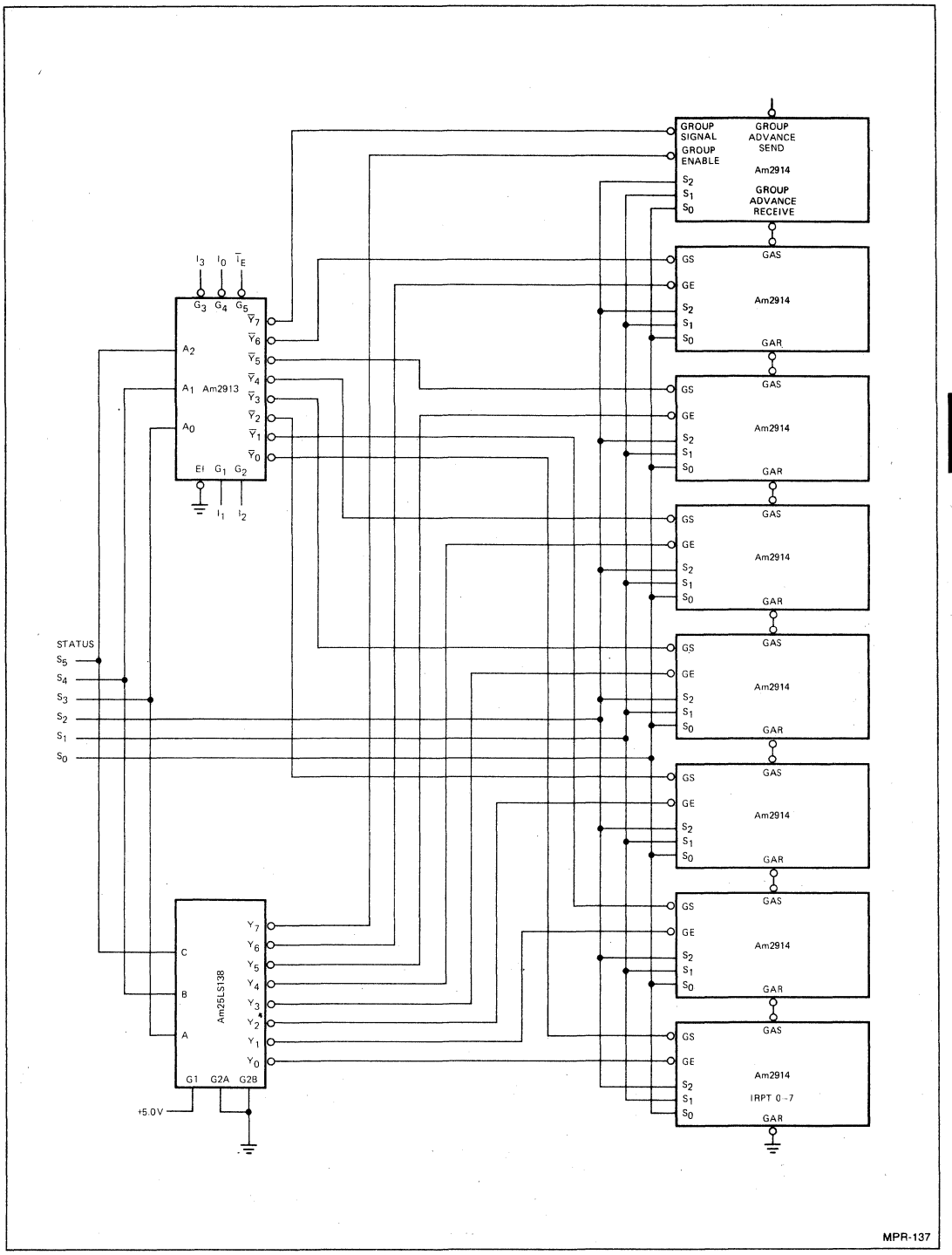
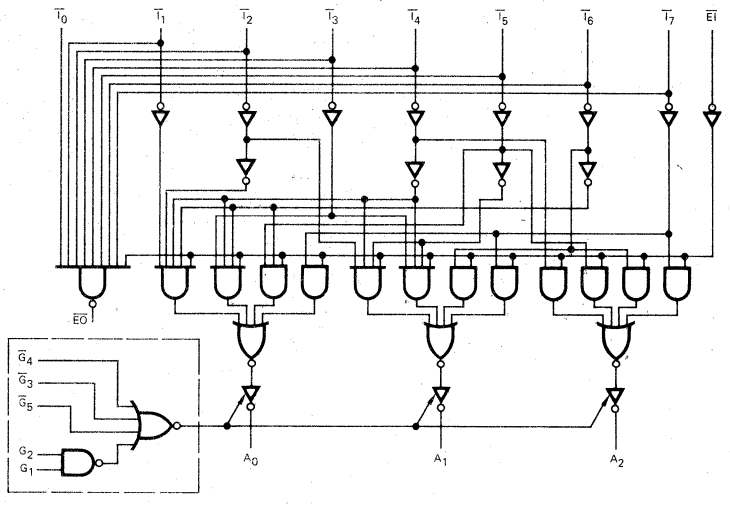


Figure 10. Group Signal, Group Enable, Group Advance Send, Group Advance Receive and Status Connections for Both the Parallel and Ripple Cascade Modes.



Inputs								Outputs			
$\overline{EI}$	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	A_0	A_1	A_2	$\overline{EO}$
H	X	X	X	X	X	X	X	X	L	L	L	H
L	H	H	H	H	H	H	H	H	L	L	L	L
L	X	X	X	X	X	X	X	L	H	H	H	H
L	X	X	X	X	X	X	L	H	L	H	H	H
L	X	X	X	X	X	L	H	H	H	L	H	H
L	X	X	X	X	L	H	H	H	L	L	H	H
L	X	X	X	L	H	H	H	H	H	H	L	H
L	X	X	L	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
For G1 = H, G2 = H,
G3 = L, G4 = L, G5 = L

G1	G2	$\overline{G3}$	$\overline{G4}$	$\overline{G5}$	A_0	A_1	A_2
H	H	L	L	L	Enabled		
L	X	X	X	X	Z	Z	Z
X	L	X	X	X	Z	Z	Z
X	X	H	X	X	Z	Z	Z
X	X	X	H	X	Z	Z	Z
X	X	X	X	H	Z	Z	Z

Z = HIGH Impedance

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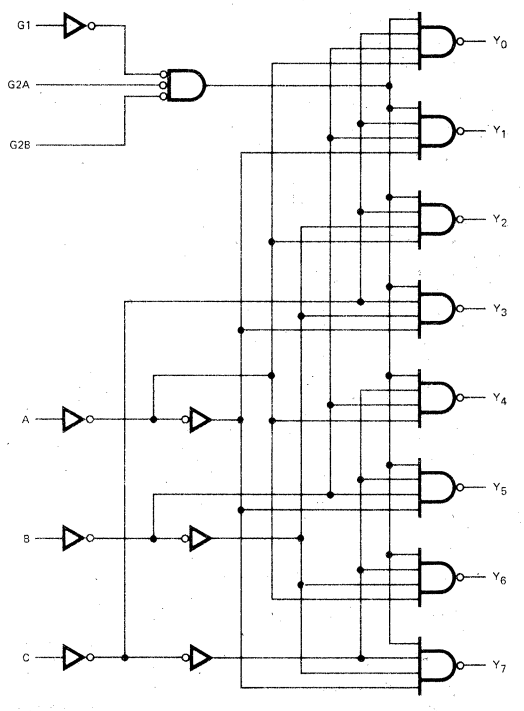
Figure 11. Am2913 Priority Interrupt Expander Logic Diagram and Truth Table.



Inputs						Outputs							
Enable			Select										
G1	G2A	G2B	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = HIGH
L = LOW
X = Don't Care

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Figure 12. Am25LS138 3 to 8 Line Decoder Logic Diagram and Truth Table.

EXAMPLE INTERRUPT SYSTEMS DESIGNS FOR AN Am2900 SYSTEM

A classical computer architecture is shown in Figure 13. The Computer Control Unit controls the internal busses and subsystems of the processor, synchronizes internal and external events and grants or denies permission to external systems. The data bus is commonly used by all of the subsystems in the computer. Information, instructions, address operands, data and sometimes control signals are transmitted down the data bus under control of a microprogram. The microprogram selects the source of the data as well as the destination(s) of the data. The Address Bus is typically used to select a word in memory for an internal computer function or to select an input/output port for an external subsystem or peripheral function. The source of the data for the address bus, also selected by microprogram commands, may be the program counter, the memory address register, a direct memory address controller, an interface controller, etc.

The arithmetic/logic unit (ALU) is that portion of the processor that computes. Under control of the microprogram, the ALU performs a number of different arithmetic and logic functions on data in the working registers or from the data bus. The ALU also provides a set of condition codes as a result of the current arithmetic or logic operation. The condition codes, along with other computer status information, are stored in a register for later use by the programmer or computer control unit.

The program counter and the memory address register are the two main sources of memory word and I/O address select data on the address bus. The program counter contains the address of the next instruction or instruction operand that is to be fetched from main memory, and the memory address register contains instruction address operands which are necessary to fetch the data required for the execution of the current instruction.

A subroutine address stack is provided to allow the return address linkage to be handled easily when exiting a subroutine. The address stack is a last-in, first-out stack that is controlled by a jump-to-subroutine, PUSH, or a return-from-subroutine, POP, instruction from the CCU microinstruction word.

The next microprogram address control (NMAC) circuitry controls the generation of microinstruction addresses. Based on microprogram control, interrupt requests, test conditions and commands from a control panel or other processor, the NMAC determines the address of the next microinstruction to be executed.

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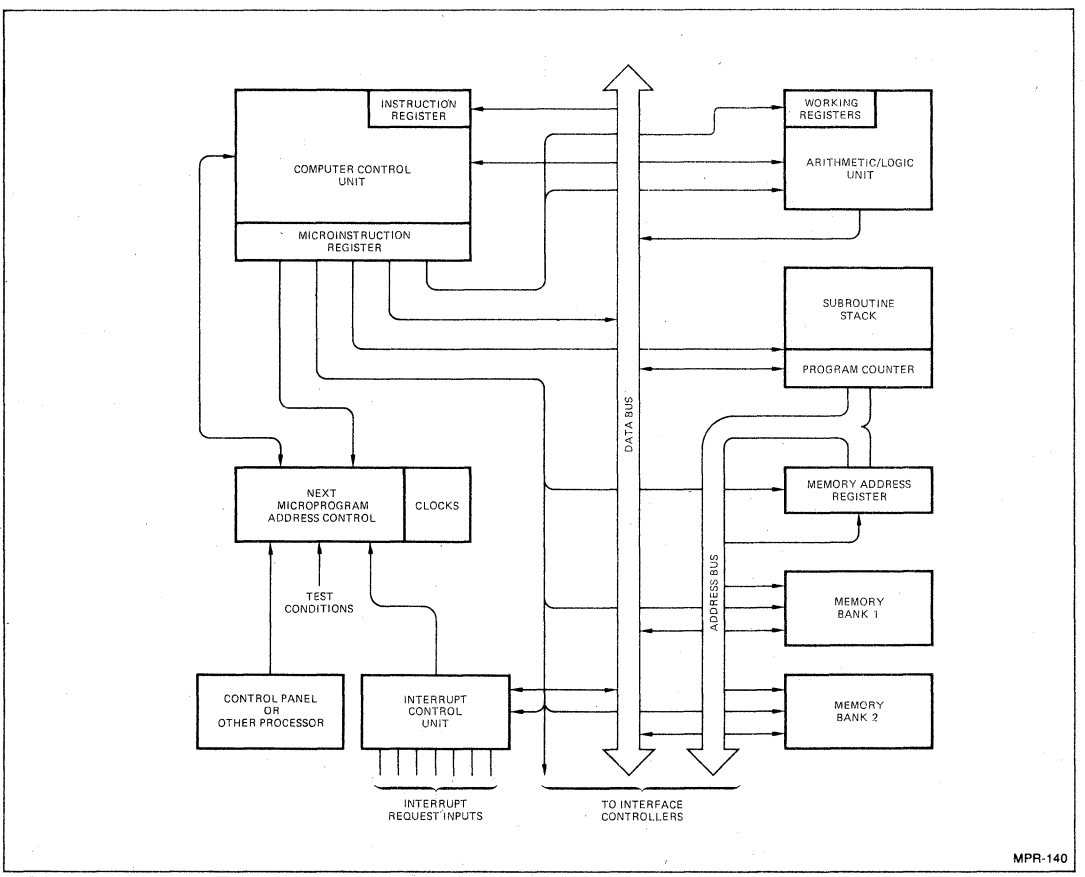

Figure 13. Generalized Computer Architecture.

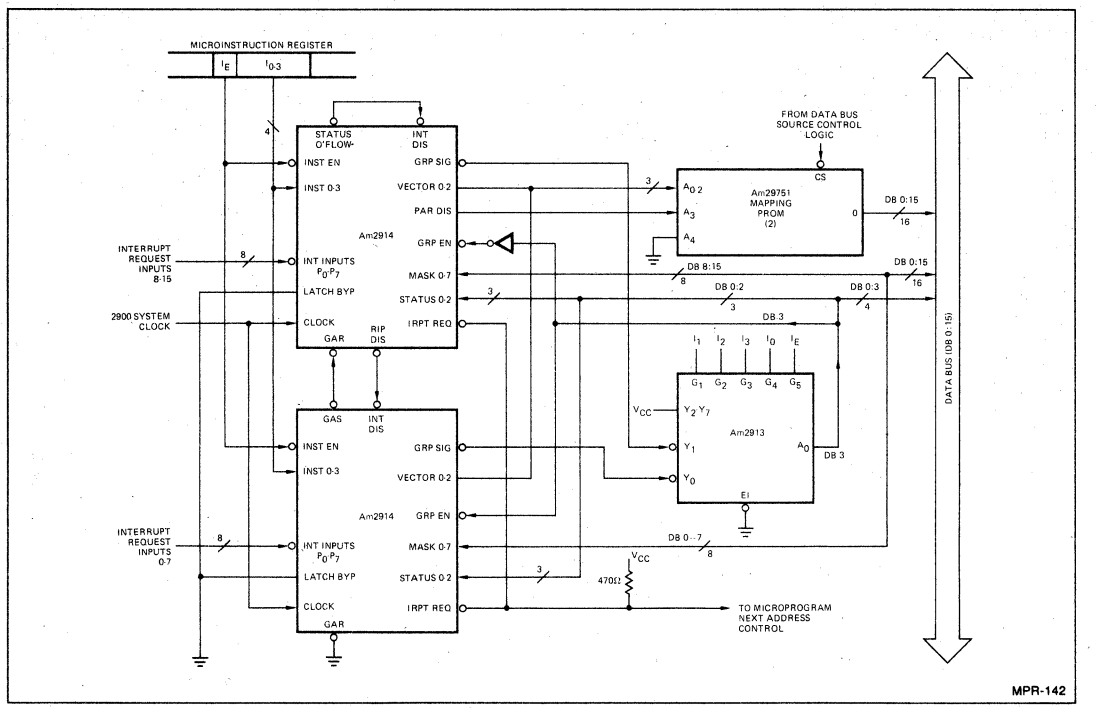

Figure 15. 16 Level Interrupt Control Unit for Am2900 System.

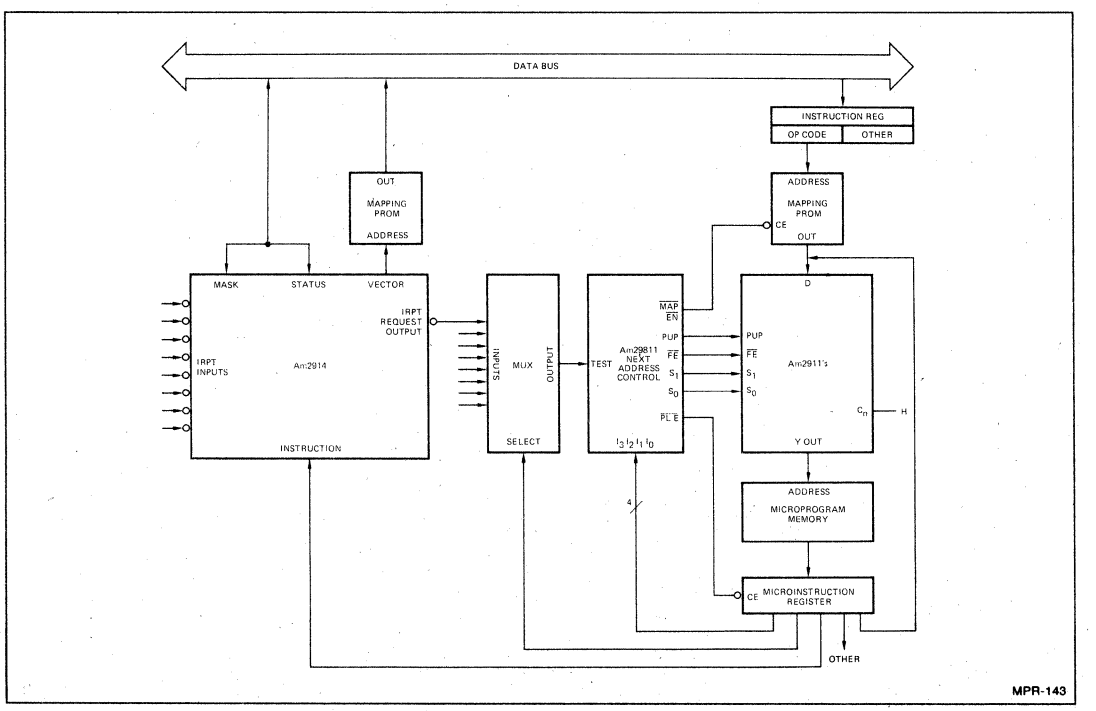

Figure 16. Computer Control Unit for Machine Program Interrupt System.

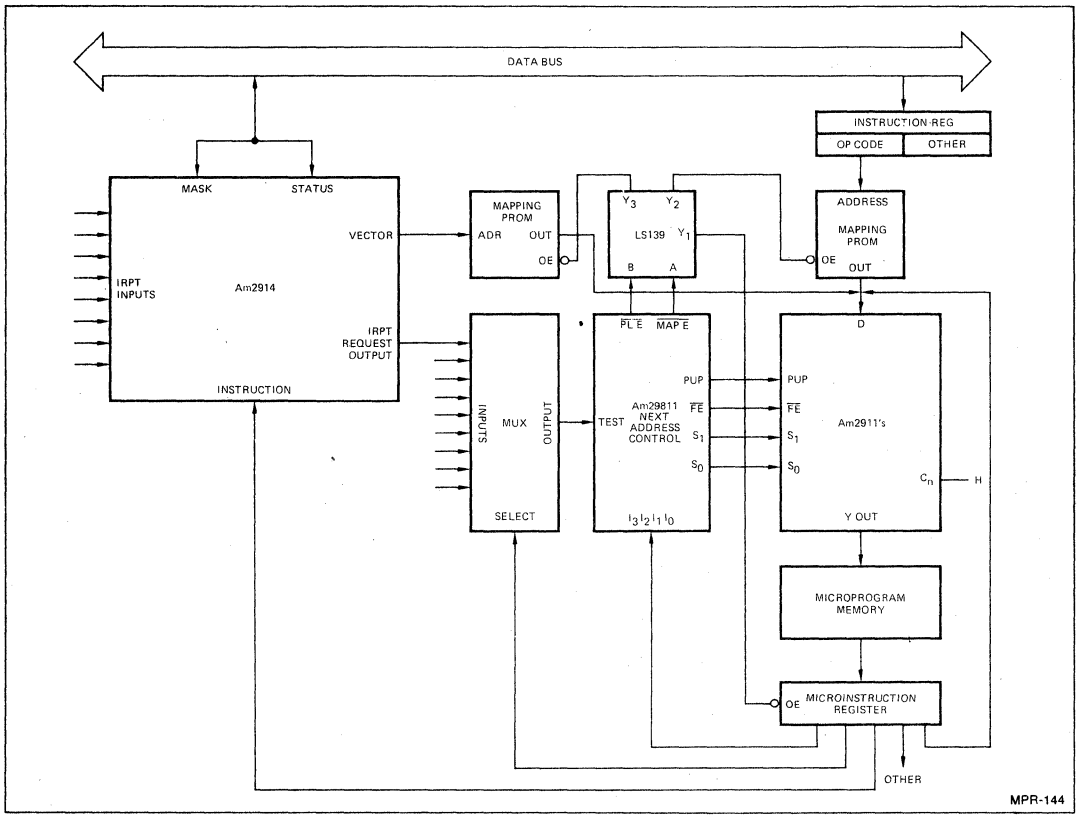

Figure 17. Computer Control Unit for Microprogram Interrupt System.

EXAMPLE INTERRUPT SYSTEM DESIGN FOR AN Am9080A SYSTEM

The Am2914 can be used in an Am9080A system also. Figure 18 shows the detailed hardware design of an eight-level ICU for an Am9080A system. The ICU attaches to the Am8228 data bus and uses any two I/O port addresses, designated X and Y. Three Am8228 control lines, $\overline{INTA}$, $\overline{I/O\ R}$ and $\overline{I/O\ W}$, are used to control the ICU, and the Am8224 ϕ_2 (TTL) output is used as the ICU clock. The ICU provides the INT (interrupt request) input to the Am9080A.

The Am9080A acknowledges an interrupt request with the $\overline{INTA}$ signal which selects the A inputs of the Am25LS09 Instruction Register. The Am25LS09 is a quad, two-input register which is set on the LOW-to-HIGH transition of the clock. The A inputs are wired so that an Am2914 Read Vector instruction is forced at the Am2914 Instruction Inputs. The $\overline{INTA}$ signal also forces the Am2914 Instruction Enable signal LOW and enables the Am25LS241 outputs onto the Am8228 data bus. The Am25LS241 is an eight-bit, three-state bus driver in a 20-pin package. Figure 19 shows a logic diagram of the Am25LS241. Five Am25LS241 inputs are wired HIGH so that, along with the Am2914 Vector outputs, they force an Am9080A Restart instruction onto the Am8228 data bus. The Am9080A then uses the vector to branch to an interrupt service routine.

During the interrupt service routine, the Am2914 is driven by Am9080A software. Figure 20 shows example Am9080A instruction code for Am2914 control and the comments describe the operation of the ICU hardware in detail. The Am2920 Data Out Register buffers data during operations which require the transfer of data from the Am9080A to the Am2914, such as the load mask and load status operations. The Am2920 contains eight "D" type flip-flops. Figure 21 shows the Am2920 logic diagram.

The Am25LS374 Data In Register buffers data during operations which require transfer of data from the Am2914 to the Am9080A, such as the read mask and read status operations. The Am25LS374 contains eight "D" type flip-flops in a 20-pin package. Figure 22 shows the logic diagram for the Am25LS374.

The Am25LS175 "D" type flip-flops are used to synchronize incoming and outgoing control signals with the ϕ_2 clock to meet the Am2914 and Am9080A timing requirements. In this design, the Latch Bypass input is connected to ground so that a negative pulse will be detected at any of the interrupt inputs. As always when a single Am2914 is used, the Status Overflow output is connected to the Interrupt Disable input, and the Group Advance Receive and Group Enable inputs are connected to ground.

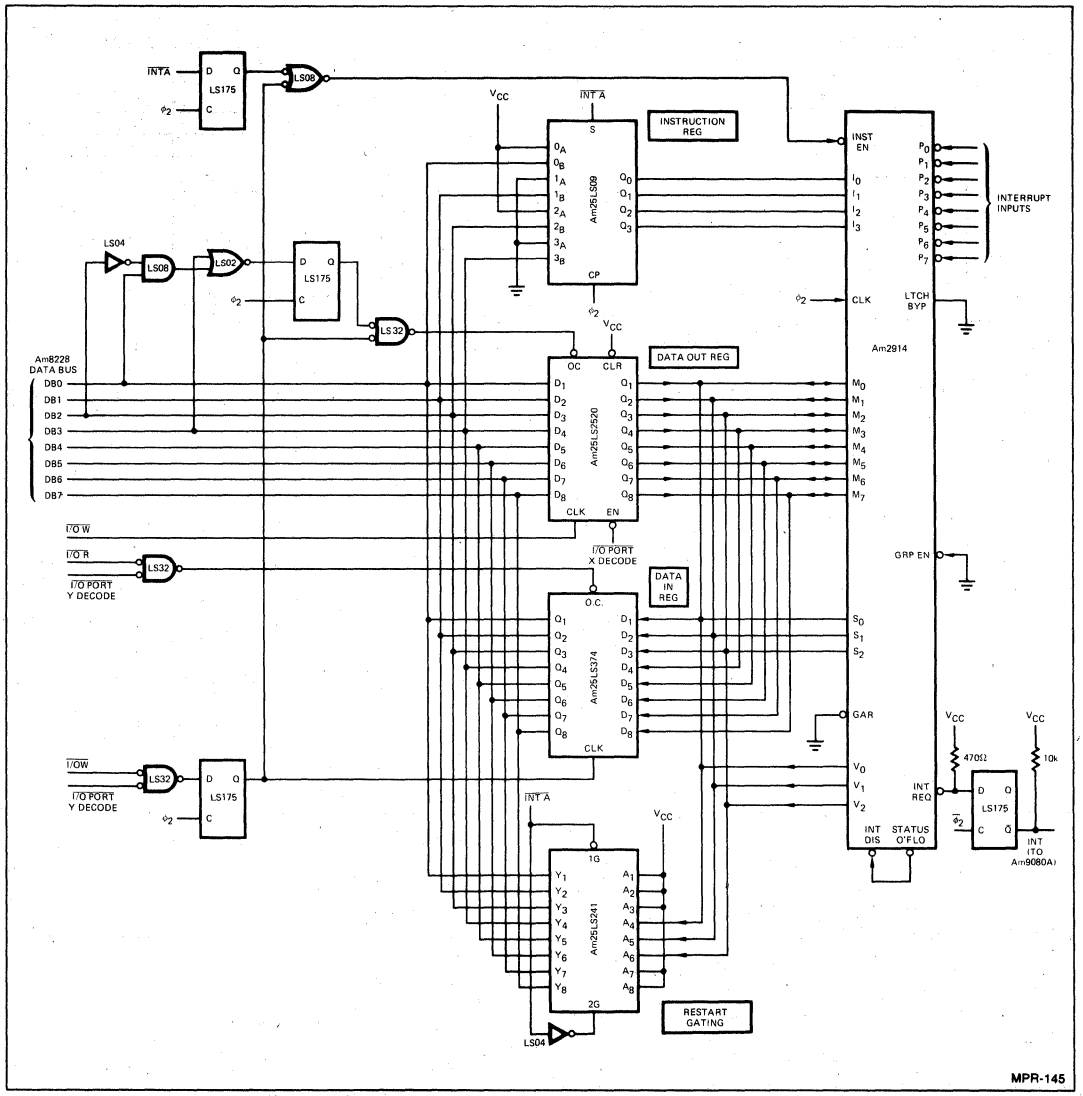

Figure 18. 8 Level Interrupt Control Unit for Am9080A System.

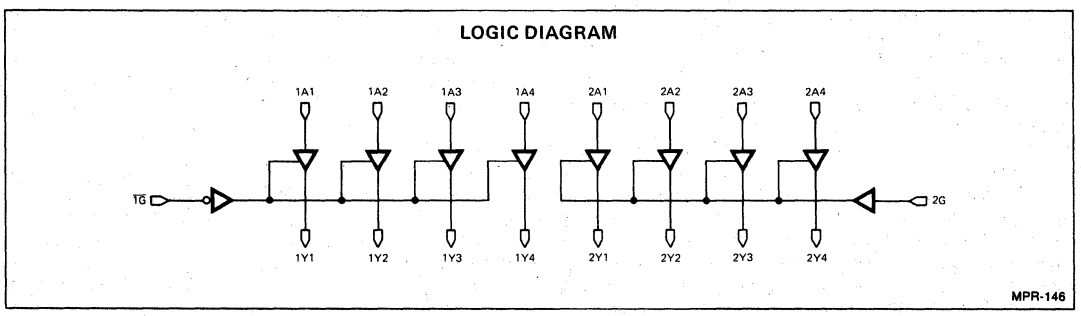

Figure 19. Am25LS241 Octal Bus Driver with 3-State Outputs, 20 Pin Package.

Am9080A MNEMONIC	Am9080A CODE (HEX)	COMMENTS	
MVI A	3E X0	LOAD IMMEDIATE THE Am2914 MASTER CLEAR INSTRUCTION INTO Am9080A ACCUMULATOR	Am2914 MASTER CLEAR OPERATION
OUT	D3 PORT Y ADR	OUTPUT ACCUMULATOR TO ICU INSTRUCTION REG & ENABLE Am2914 INSTRUCTION	
MVI A	3E MASK PATTERN	LOAD IMMEDIATE THE MASK BIT PATTERN INTO THE Am9080A ACCUMULATOR	Am2914 LOAD MASK OPERATION
OUT	D3 PORT X ADR	OUTPUT ACCUMULATOR TO ICU DATA OUT REG	
MVI A	3E XE	LOAD IMMEDIATE THE Am2914 LOAD MASK INSTRUCTION INTO Am9080A ACCUMULATOR	
OUT	D3 PORT Y ADR	OUTPUT ACCUMULATOR TO ICU INST REG, ENABLE INST., & ENABLE DATA OUT REG OUTPUTS	
MVI A	3E X6	LOAD IMMEDIATE THE Am2914 READ STATUS INSTRUCTION INTO Am9080A ACCUMULATOR	Am2914 READ STATUS OPERATION
OUT	D3 PORT Y ADR	OUTPUT ACCUMULATOR TO ICU INST REG, ENABLE INST., & CLOCK DATA IN REG	
IN	DB PORT Y ADR	ENABLE DATA IN REG ONTO DATA BUS & READ IT INTO THE Am9080A ACCUMULATOR	

Note: Am2914 instruction bits I_0-I_3 must be on data bus bits DB_0-DB_3, respectively.
X = Don't Care.

Figure 20. Example Am9080A Instruction Code for Am2914 Control.

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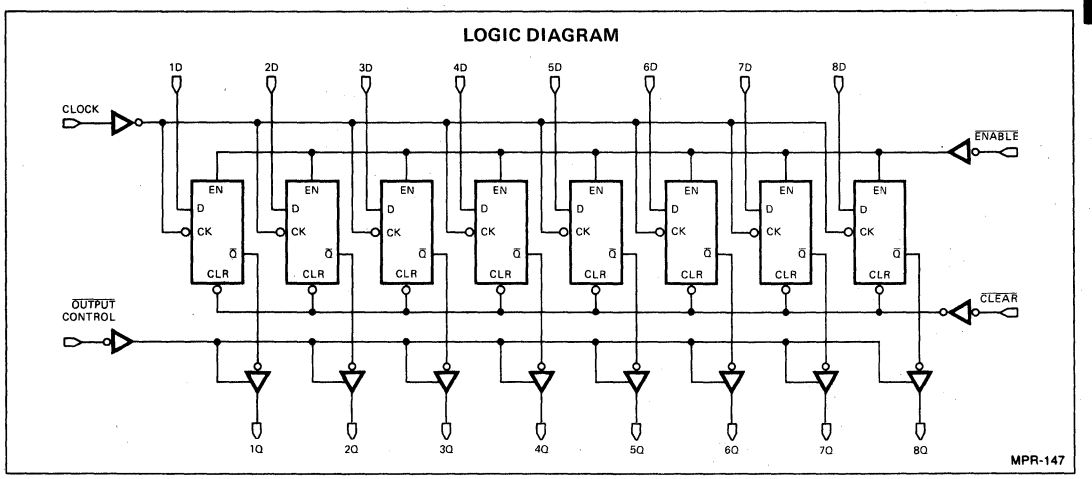


Figure 21. Am2920 Octal D-Type Flip-Flops with 3-State Outputs. Common Clock, Clear, Clock Enable and Output Control, 22 Pin Package.

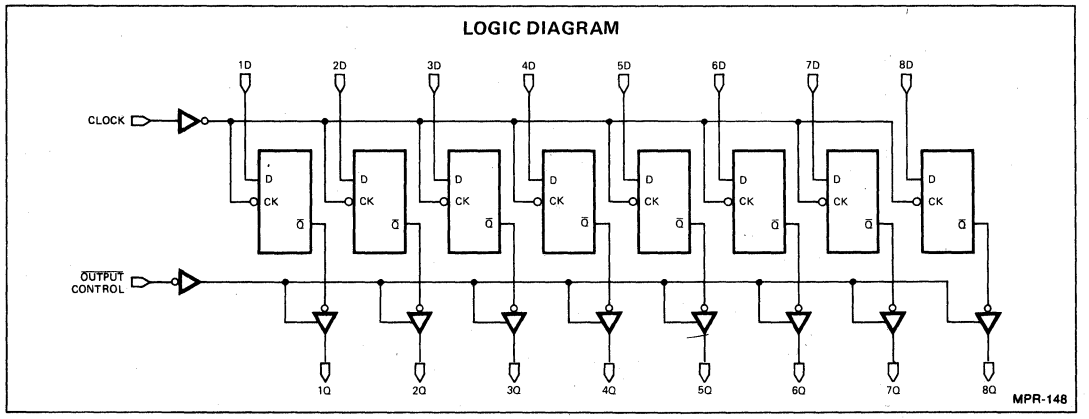


Figure 22. Am25LS374 Octal D-Type Flip-Flops with 3-State Outputs, 20 Pin Package.

Implementing Interrupts for Bit-Slice Processors

By Vern Coleman

Interrupt detection and handling at the microprogram level can be easily implemented in the Am2900 bit-slice processor family thanks to versatile components like the Am2914 priority interrupt encoder and others. The interrupt scheme can generally be extended to other systems at the cost of additional circuitry.

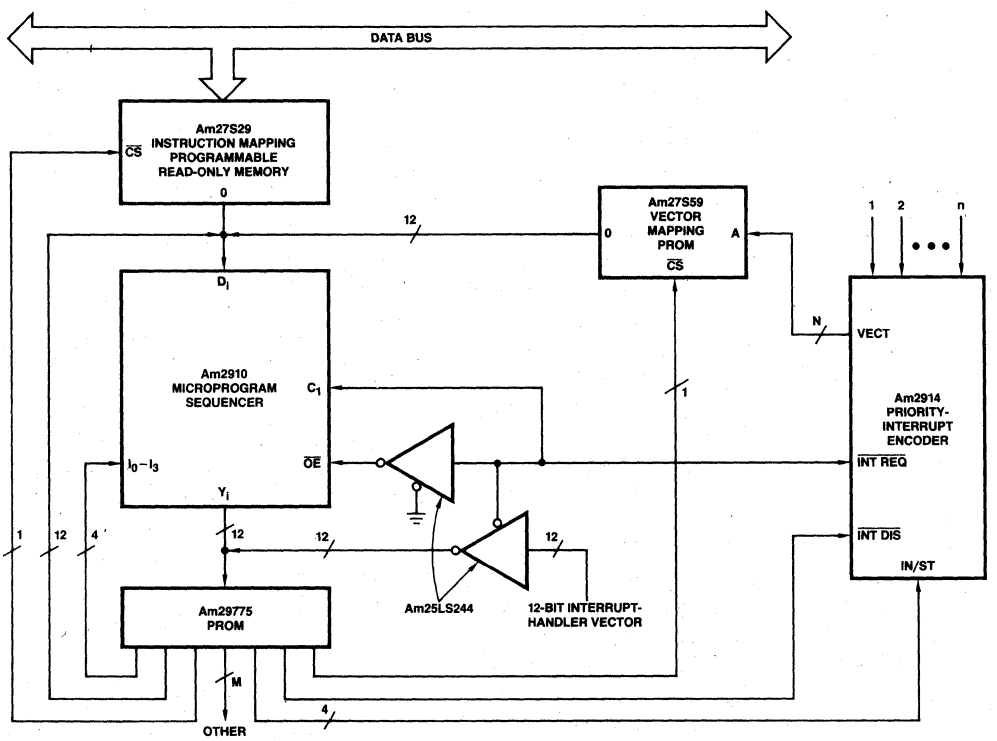
As shown in the figure, the components required are the 2914, the 2910 microprogram sequencer, a 29775 programmable read-only memory, and two separate PROMs for mapping instructions from main memory and interrupt vectors from the 2914 into starting addresses for the 2910.

If an interrupt is detected by the 2914 as the 2910 executes an instruction, the interrupt-request output of the encoder moves low. This action turns off the carry input of the 2910, for all practical purposes causing the sequencer to halt for a microcycle. It also causes any data that would normally appear at the Y_i outputs to be stored in the sequencer's program counter.

The interrupt request also forces the output of the sequencer into a high-impedance state. This allows an interrupt-handling vector to be applied at the Y_i outputs, thereby addressing the first instruction of the interrupt routine in the microprogram memory.

The 2914 is thus instructed to place an interrupt vector on its output port. The same word in microprogram memory also enables the output of the vector-mapping PROM to allow decoding of the interrupt vector. The result is then applied to the D inputs of the 2910 while it does a jump to the appropriate subroutine. Thus the first address of the interrupt routine is brought in, and the address to which the previously executed program is to return after the interrupt is serviced is stored away. If there is a point in the microprogram routing where no interrupts are to be allowed, a logic 0 can be applied to the interrupt disable input pin on the 2914.

The microcode for handling interrupts is shown in the table. The first entry commences with address 1. This vector instructs the 2914 to execute a jump to subroutine if its condition code input is low. The encoder is then commanded to place its interrupt vector associated with the current interrupt request on its output port. At this time, it may be desirable to disable any further interrupts, in which case the appropriate pin should be brought low, as explained above. A logic 0 is also placed on the vector-mapping PROM while a logic 1 is placed on the data-mapping PROM's output-enable lead and the pipeline output-enable of the 29775. Thus the vector-mapping PROM will be the sole source of any input to the D port of the 2910.



At address I + 1, the interrupt associated with the previous vector read into the 2914 may be cleared, and the vector-mapping PROM disabled by bringing its output-enable lead high. At address I + 2 and subsequent addresses, the 2914 may be commanded to accept any interrput by use of the enable interrupt request. The vector-mapping PROM is first disabled with a logic 1 signal. At this time the interrupt-disable pin of the 2914 is deactivated. At the end of the interrupt routine, an exit is achieved via the conditional-return instruction of the 2910. A logic 0 should be simultaneously applied to the condition-code inputs of the sequencer.

There is nothing that precludes the use of this architecture in a stacked-interrupt system. The number of interrupts that can be stacked is limited by the depth of the 2910. It is only necessary to issue a simple command to return from the subroutine utilized to the main program, for each stacked interrupt.

STOP

Standard elements of the Am2900 Family are easily configured to provide interrupt capability for bit-slice microprocessors. Architecture is applicable to stacked interrupt systems. Microcode for handling interrupts (see table) is fast and simple.

Interrupt Address	Am2910 Instruction	Am2914		Vector-Mapping PROM	Data-Mapping PROM
		Instruction	Interrupt Disable		
I	CJS	Read vector	0	0	0
I + 1	–	Clear interrupt, last vector read	0	1	–
I + 2	–	Enable interrupt request	1	1	–
I + 3	CRTN	–	1	–	–

5

Am2914 Priority Interrupt Encoder Detailed Logic Description

INTRODUCTION

A clear understanding of the Am2914 Priority Interrupt controller's operation facilitates its efficient use. With that idea in mind, a detailed logic description of the Am2914 is presented here. A detailed logic diagram and control signal truth table are shown, and significant aspects of the Am2914 design are described verbally.

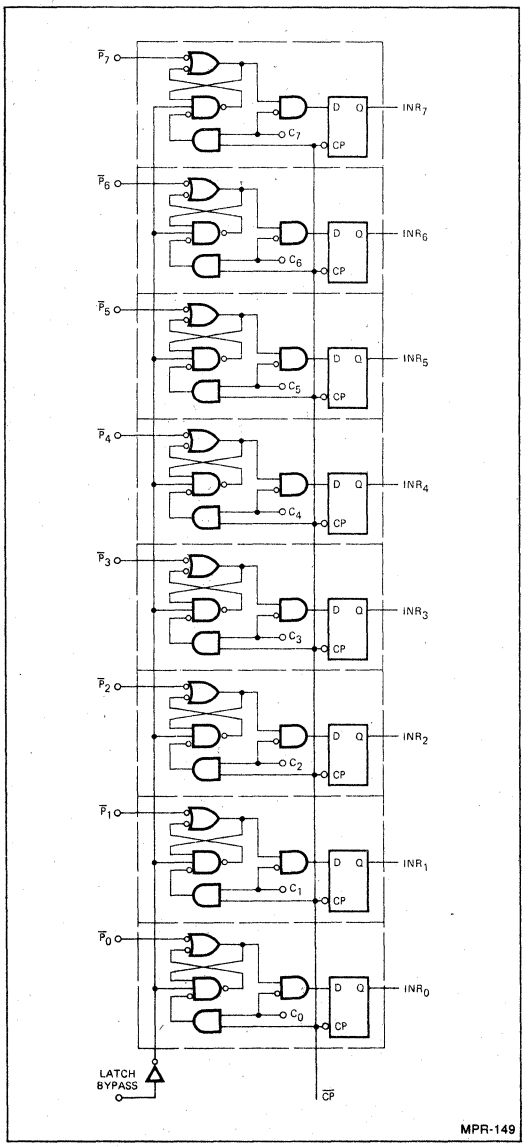


Figure 1. Interrupt Latches and Register.

LOGIC DIAGRAM DESCRIPTION

The Interrupt Latches and Register are shown in Figure 1. The Interrupt latches are set/reset-type latches. When the Latch Bypass signal is LOW, the latches are enabled and act as negative pulse catchers on the inputs to the Interrupt Register. When the Latch Bypass signal is HIGH, the Interrupt latches are transparent. The Interrupt Register holds the Interrupt Inputs and is an eight-bit, edge-triggered register. It is updated on the LOW-to-HIGH transition of the clock pulse (HIGH-to-LOW transition of the $\overline{CP}$ signal) as are all of the flip-flops on the chip.

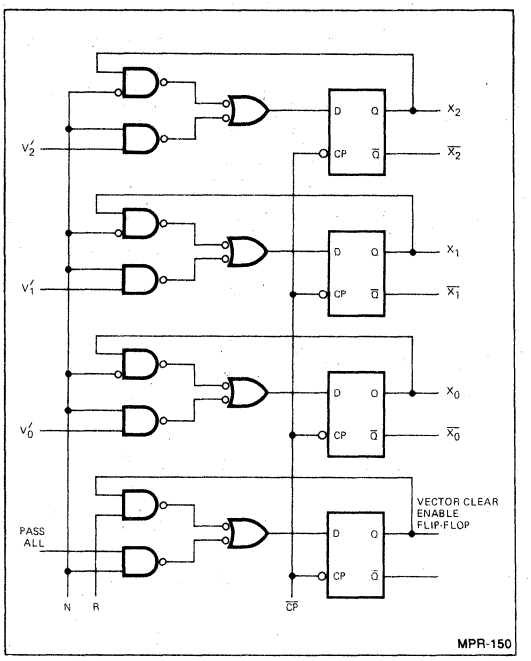


Figure 2. Vector Hold Register

When a Read Vector instruction is executed, the binary coded vector is loaded into the Vector Hold Register of Figure 2. This stored vector can be used later for clearing the interrupt associated with the last vector that was read. The Vector Clear Enable Flip-Flop of Figure 2 is set when a Read Vector instruction is executed and the PASS ALL signal is HIGH. A HIGH PASS ALL signal level indicates that this group is enabled and that an interrupt request in this group was detected and passed priority. The Vector Hold Register and the Vector Clear Enable Flip-Flop are cleared when a Master Clear, Clear All Interrupts, or Clear Interrupt Last Vector Read is executed. Table 1 shows the generation of the "N and R" control signals for each of these operations.

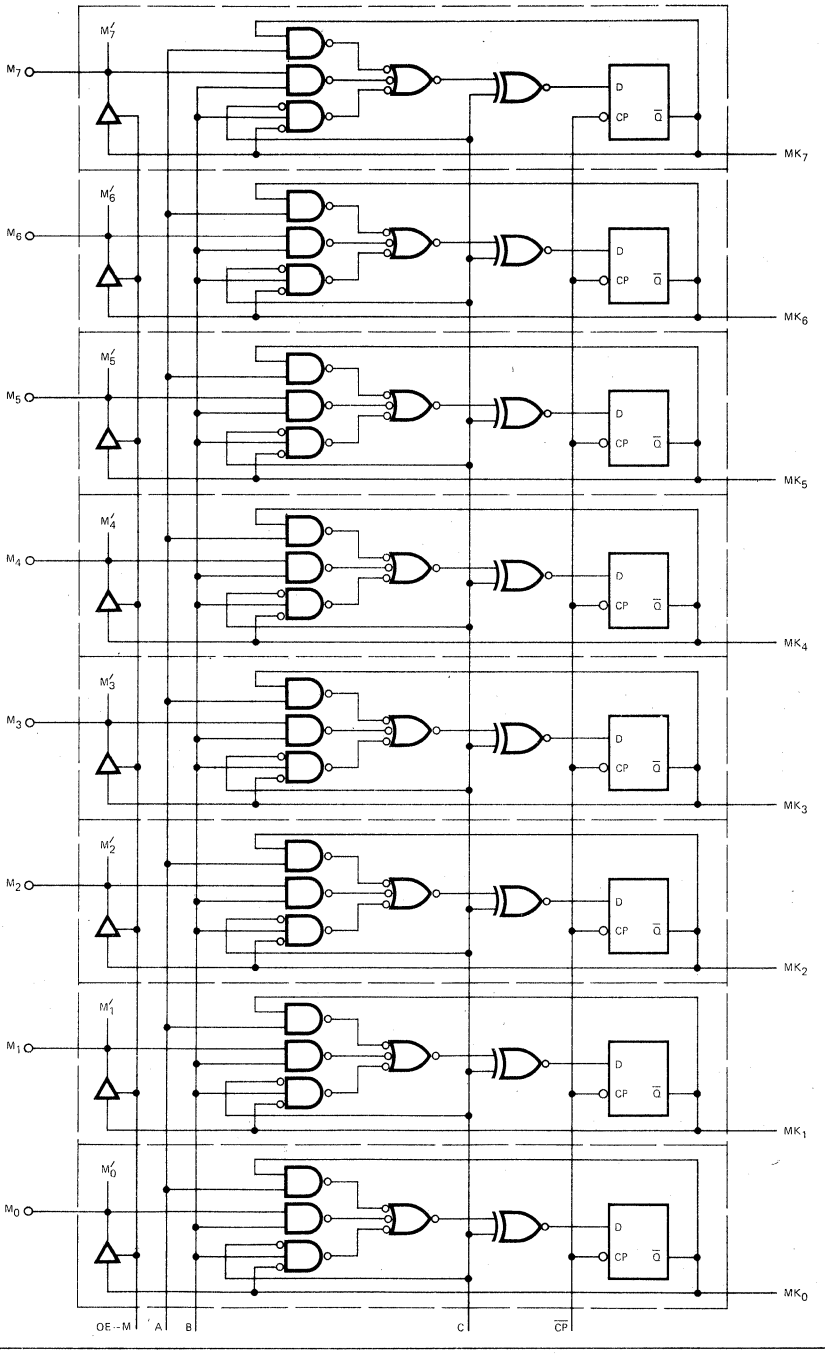


Figure 3. Mask Register.

The Mask Register shown in Figure 3 holds the eight mask bits associated with the eight interrupt levels. The register may be set or cleared, bit set or bit cleared from the "M" bus, or loaded or read to the "M" bus. Table 1 shows the generation of the "A", "B", "C" and "OE-M" control signals for each of these operations.

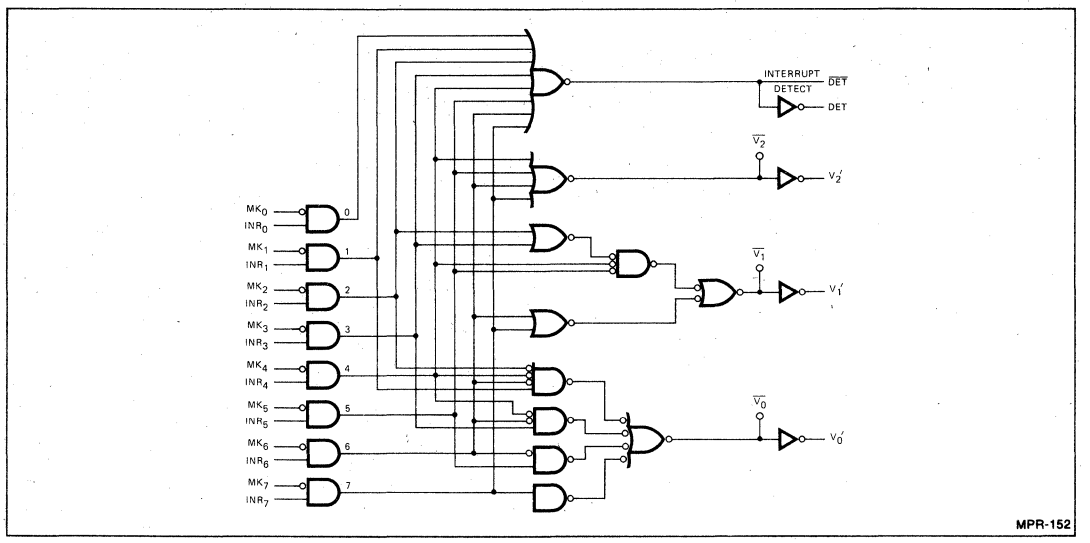


Figure 4. Interrupt Request Detect and Priority Decoder.

The Interrupt Request Detect and Priority Encode circuitry are shown in Figure 4. The Interrupt Detect circuitry detects the presence of any unmasked Interrupt Input. The eight-input Priority Encoder determines the highest priority, non-masked Interrupt Input and forms a binary coded interrupt vector, V_0-V_2.

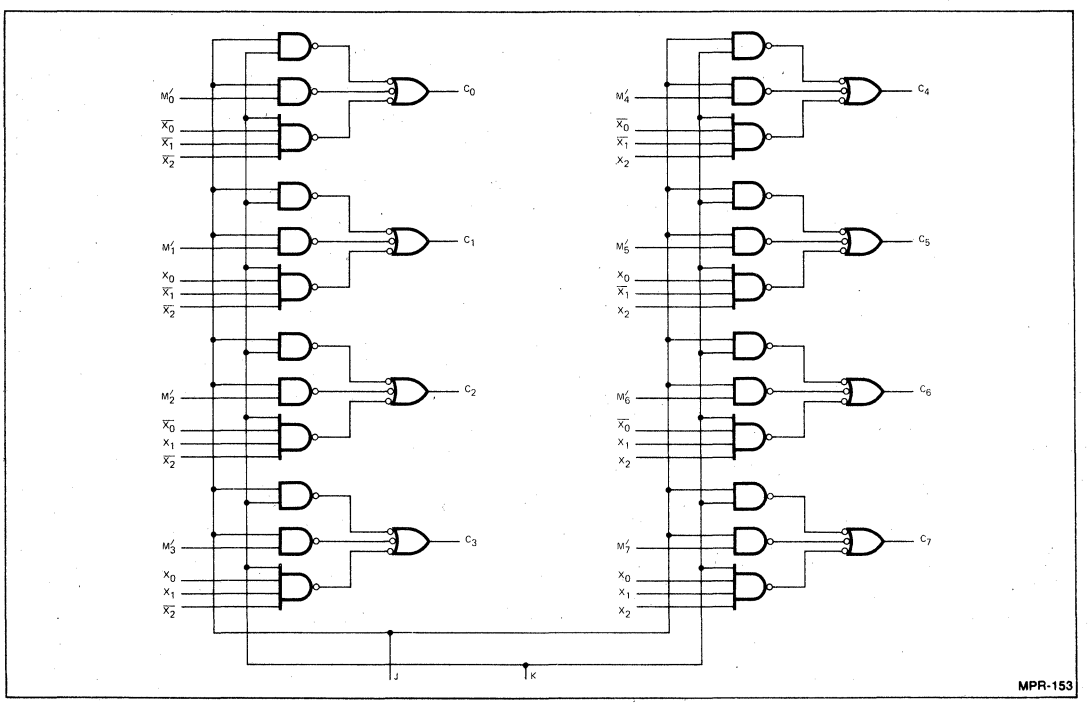


Figure 5. Clear Control.

The Clear Control logic of Figure 5 generates the eight individual clear signals for the eight Interrupt Register bits. Under microinstruction control, all interrupts, interrupts with corresponding mask register bits set, interrupts with corresponding mask bus bits equal to one, or the interrupt associated with the last vector read may be cleared. Table 1 shows the generation of the "J" and "K" control signals for each of these operations.

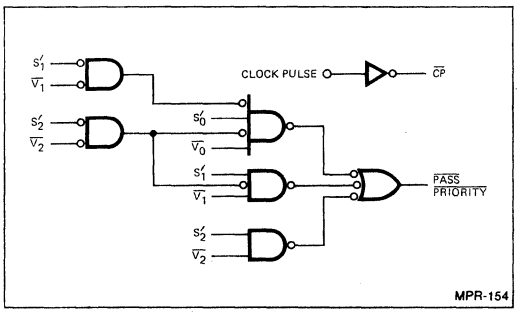


Figure 6. Three-Bit comparator.

The three-bit Comparator of Figure 6 compares the interrupt vector with the contents of the Status Register. A LOW signal level at the PASS PRIORITY output indicates that the interrupt vector is greater than or equal to the contents of the Status Register.

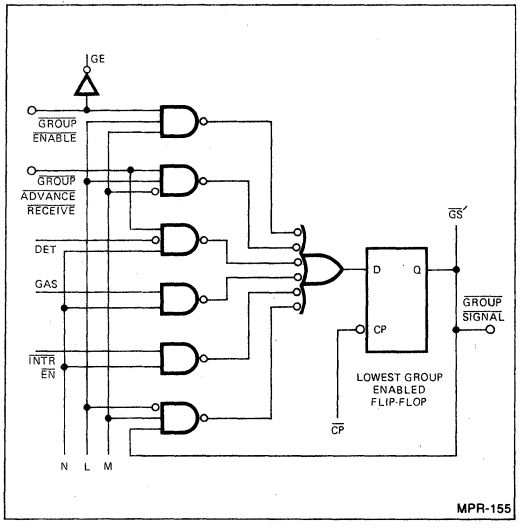


Figure 7. Group Enable Logic.

The Lowest Group Enabled Flip-Flop, Figure 7, is used when a number of Am2914's are cascaded. In a cascaded system, only one Lowest Group Enabled Flip-Flop is LOW at a time. It indicates the group which contains the lowest priority interrupt which will be accepted and is used to form the high order status bits. When a Load Status instruction is executed, the flip-flop is loaded from the GROUP ENABLE input. When a Master Clear instruction is executed, it is loaded from the GROUP ADVANCE RECEIVE input. The flip-flop is set HIGH when a Read Vector instruction is executed if a Group Advance is not received and no interrupt in this group is detected, if a Group Advance is sent from this group, or if interrupts from this group are disabled. For all other instructions, the flip-flop remains the same. Table 1 shows the generation of the "N", "L" and "M" control signals for these operations.

The Status Register holds the status bits and may be loaded from or read to the "S" bus as shown in Figure 8. Note that when a Load Status instruction is executed, status from the "S" bus is loaded into the Status Register only if the GROUP ENABLE input is LOW; if the GROUP ENABLE input is HIGH, the Status Register is cleared. Also note that during a Read Status instruction, the Status Register outputs are enabled onto the "S" bus only if the Lowest Group Enabled Flip-Flop of this group is LOW. When a Read Vector instruction is executed, the incrementer increases the vector by one and the result is loaded into the Status Register. Thus, the Status Register always points to the lowest level at which an interrupt will be accepted. Table 1 shows the generation of the "F", "G" and "OE-S" control signals for Status Register operations.

The Interrupt Request Logic, shown in Figure 9, generates the RIPPLE DISABLE, PARALLEL DISABLE, INTERRUPT REQUEST, GROUP ADVANCE SEND, and STATUS OVERFLOW output signals. The PARALLEL DISABLE signal is generated when the Lowest Group Enabled signal is LOW or an interrupt request in this group is detected and passes priority. The RIPPLE DISABLE signal is generated when the PARALLEL DISABLE signal is generated and also when the INTERRUPT DISABLE input signal is LOW. The INTERRUPT REQUEST output signal is generated when interrupt requests in this group are enabled and a request is detected and passes priority. The GROUP ADVANCE SEND output signal is generated when a vector of value seven is being read. The Status Overflow Flip-Flop is set LOW when a vector of value seven is read and indicates the Status Register has overflowed. The Interrupt Request Enable Flip-Flop is either set or reset by the Enable Request or Disable Request microinstructions respectively, and is used to enable or disable the INTERRUPT REQUEST output. Table 1 shows the generation of control signals "D", "E", "S" and "H".

Note that the vector outputs are enabled only when a Read Vector is being executed. Also note that when a Read Vector instruction is executed, the vector outputs will be disabled after the execution of the instruction since the Status Register is loaded with V+1, and the INTERRUPT REQUEST will no longer be generated.

The Microinstruction Decode circuitry, Figure 10, decodes the Am2914 microinstructions and generates the required internal control signals. Table 1 shows the truth table for these functions and Figure 11 shows the function tables.

Table 1. Am2914 Control Signal Truth Table.
0 = LOW, 1 = HIGH

Microinstruction						Function	Mask Register			Status Register			Group Enable		Clear Control		Irpt Request Enable		Vector Hold Register		Other	
Decimal	$\overline{I_E}$	I_3	I_2	I_1	I_0	Description	A	B	C	OE-M	F	G	$\overline{OE\text{-}S}$	L	M	J	K	D	E	N	R	S	H
0	0	0	0	0	0	Master Clear	0	0	1	0	0	0	1	1	0	1	1	0	1	0	0	1	1
1	0	0	0	0	1	Clear All Interrupts	1	0	1	0	0	1	1	0	1	1	1	1	X	0	0	1	0
2	0	0	0	1	0	Clear Intr Via M Bus	1	0	1	0	0	1	1	0	1	1	0	1	X	0	1	1	0
3	0	0	0	1	1	Clear Intr Via M Reg	1	0	1	1	0	1	1	0	1	1	0	1	X	0	1	1	0
4	0	0	1	0	0	Clear Intr, Last Vector	1	0	1	0	0	1	1	0	1	0	1/0	1	X	0	0	1	0
5	0	0	1	0	1	Read Vector	1	0	1	0	0/1	0	1	0	0	0	0	1	X	1	0	0	1
6	0	0	1	1	0	Read Status Reg	1	0	1	0	0	1	0	0	1	0	0	1	X	0	1	1	0
7	0	0	1	1	1	Read Mask Reg	1	0	1	1	0	1	1	0	1	0	0	1	X	0	1	1	0
8	0	1	0	0	0	Set Mask Reg	0	0	0	0	0	1	1	0	1	0	0	1	X	0	1	1	0
9	0	1	0	0	1	Load Status Reg	1	0	1	0	1	1	1	1	1	0	0	1	X	0	1	1	1
10	0	1	0	1	0	Bit Clear Mask Reg	0	1	0	0	0	1	1	0	1	0	0	1	X	0	1	1	0
11	0	1	0	1	1	Bit Set Mask Reg	1	1	1	0	0	1	1	0	1	0	0	1	X	0	1	1	0
12	0	1	1	0	0	Clear Mask Reg	0	0	1	0	0	1	1	0	1	0	0	1	X	0	1	1	0
13	0	1	1	0	1	Disable Request	1	0	1	0	0	1	1	0	1	0	0	0	0	0	1	1	0
14	0	1	1	1	0	Load Mask Reg	0	1	1	0	0	1	1	0	1	0	0	1	X	0	1	1	0
15	0	1	1	1	1	Enable Request	1	0	1	0	0	1	1	0	1	0	0	0	1	0	1	1	0
X	1	X	X	X	X	Instruction Disable	1	0	1	0	0	1	1	0	1	0	0	1	X	0	1	1	0

Notes: 1. Control line "F" during "READ VECTOR" instruction is 0 when "PASS ALL" is LOW and 1 when "PASS ALL" is HIGH.
2. Control line "K" during "Clear Intr, Last Vector" instruction is 0 when "Vector Clear Enable" is LOW and 1 when "Vector Clear Enable" is HIGH.

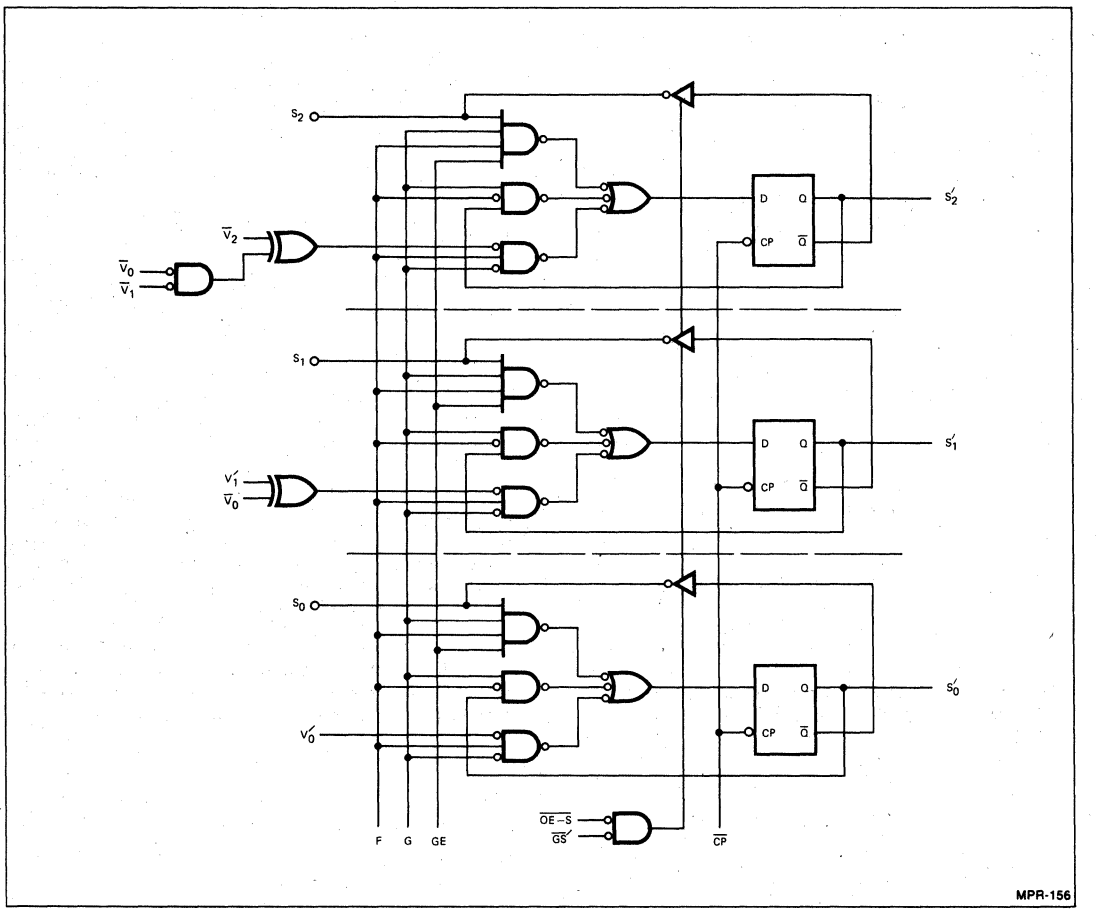


Figure 8. Incrementer and Status Register.

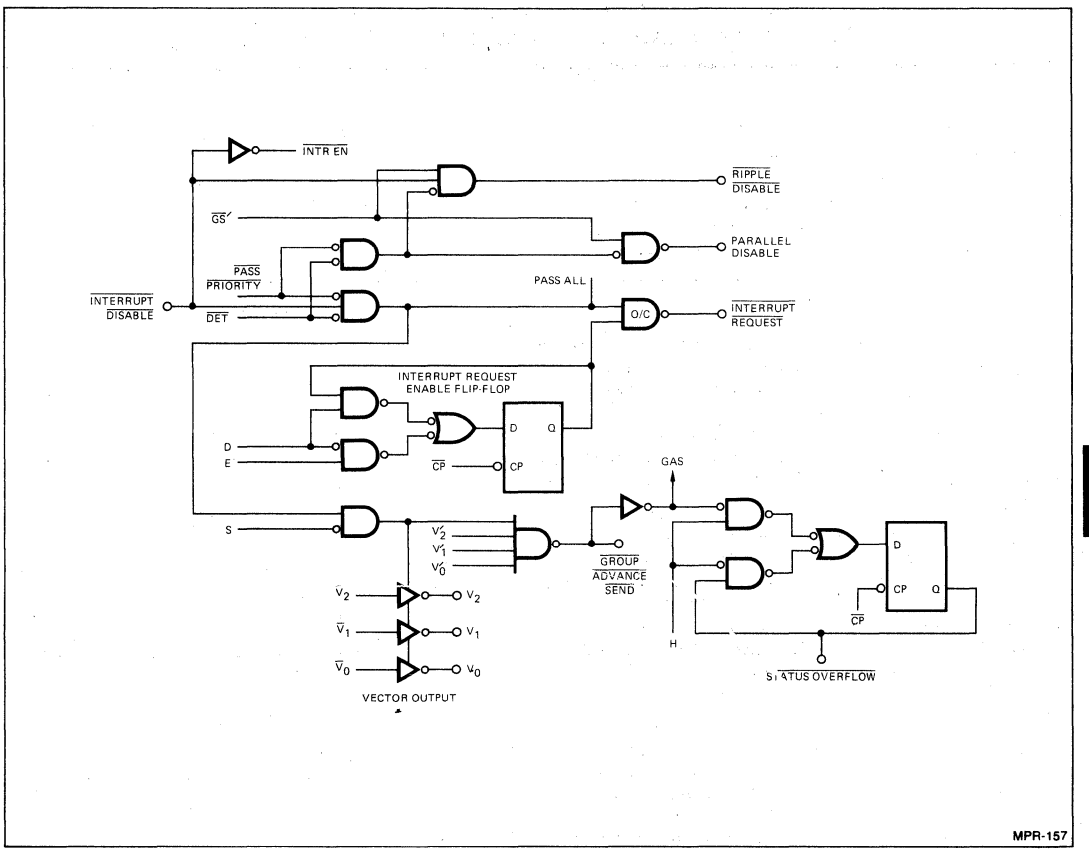


Figure 9. Interrupt Request Logic.

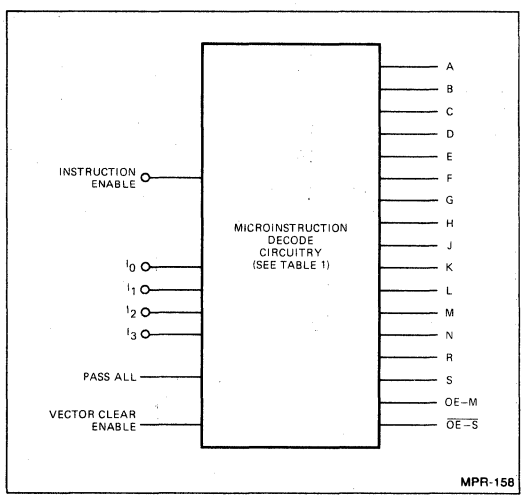


Figure 10.

MASK REGISTER

A	B	C	FUNCTION
0	0	0	SET
0	0	1	CLEAR
0	1	0	BIT CLEAR
0	1	1	LOAD
1	0	1	HOLD
1	1	1	BIT SET

CLEAR CONTROL

J	K	FUNCTION
0	0	NO CLEAR
0	1	CLEAR IRPT, VECTOR
1	0	CLEAR IRPTS VIA M
1	1	CLEAR ALL IRPTS

VECTOR HOLD REGISTER

N	FUNCTION
0	HOLD
1	LOAD

LOWEST GROUP ENABLED FLIP-FLOP

L	M	FUNCTION
0	0	UPDATE
0	1	HOLD
1	0	LOAD VIA GROUP ADVANCE RECEIVE
1	1	LOAD VIA GROUP ENABLE

STATUS REGISTER

F	G	FUNCTION
0	0	CLEAR
0	1	HOLD
1	0	LOAD VECTOR + 1
1	1	LOAD VIA "S" BUS

INTERRUPT REQUEST ENABLE FLIP-FLOP

D	E	FUNCTION
0	0	DISABLE IRPTS
0	1	ENABLE IRPTS
1	X	HOLD

VECTOR CLEAR ENABLE FLIP-FLOP

N	R	FUNCTION
0	0	CLEAR
0	1	HOLD
1	0	LOAD

STATUS OVERFLOW FLIP-FLOP

H	FUNCTION
0	HOLD
1	LOAD

Figure 11. Control Function Tables.

Am2915A

Quad Three-State Bus Transceiver with Interface Logic

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 48mA at 0.5V max.
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

FUNCTIONAL DESCRIPTION

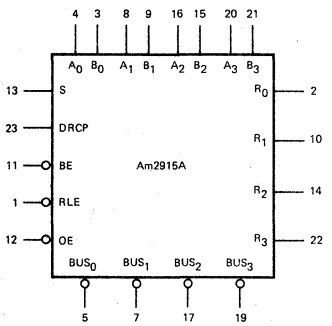
The Am2915A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches that feature three-state outputs.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The V_{OH} and V_{OL} of the bus driver are selected for compatibility with standard and Low-Power Schottky inputs.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B inputs is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and OE LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

LOGIC SYMBOL



V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

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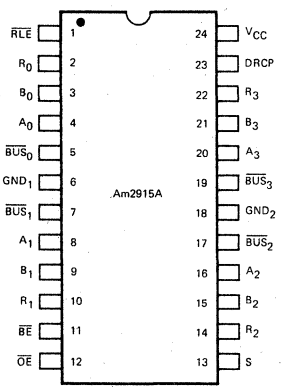
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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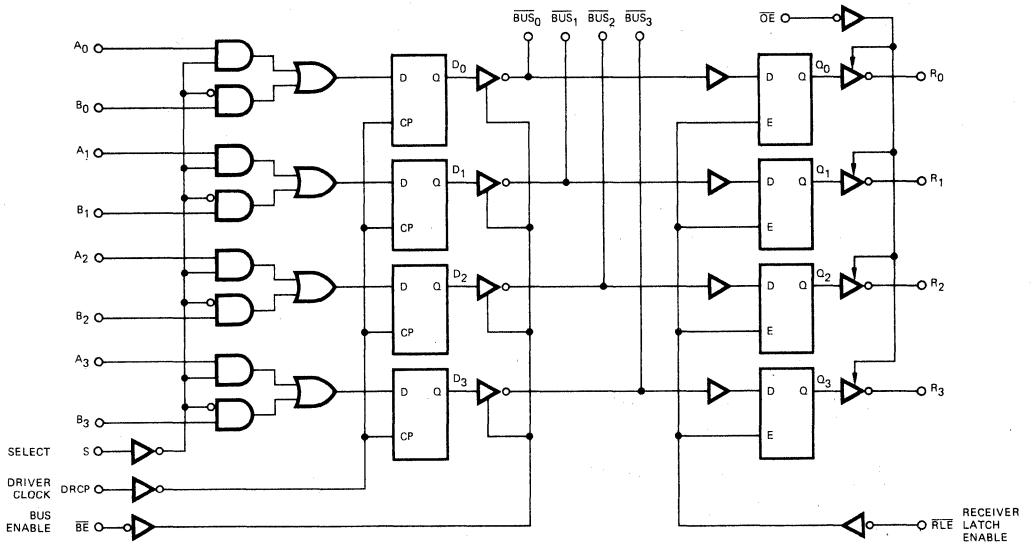
LOGIC DIAGRAM



5

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	100mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2915AXC (COM'L) T_A = 0°C to +70°C V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V
Am2915AXM (MIL) T_A = −55°C to +125°C V_{CC} MIN. = 4.50V V_{CC} MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ.	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 24mA			0.4	Volts
			I_{OL} = 48mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN.	COM'L, I_{OH} = −20mA	2.4			Volts
			MIL, I_{OH} = −15mA				
I_O	Bus Leakage Current (High Impedance)	V_{CC} = MAX. Bus enable = 2.4V	V_O = 0.4V			−200	μA
			V_O = 2.4V			50	
			V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V V_{CC} = 0V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4V	COM'L			0.8	Volts
			MIL			0.7	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX. V_O = 0V		−50	−120	−225	mA

Am2915A
ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2915AXC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
Am2915AXM (MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

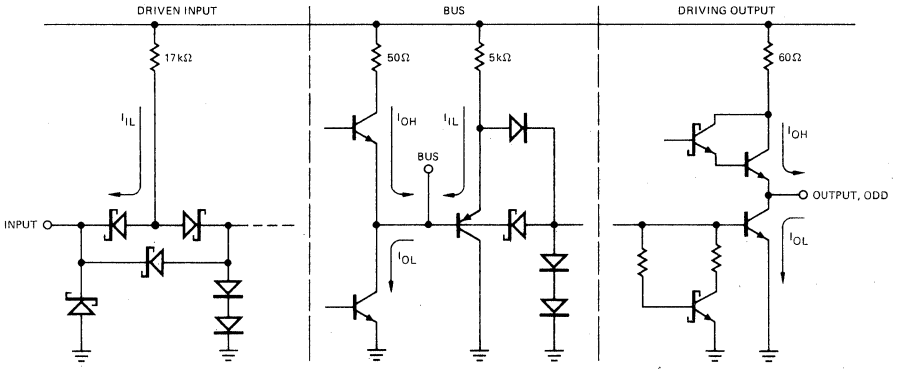
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1.0$mA	2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6$mA	2.4	3.4		
		V_{CC} = 5.0 V, $I_{OH} = -100\mu$A		3.5			
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 4.0mA		0.27	0.4	Volts
			I_{OL} = 8.0mA		0.32	0.45	
			I_{OL} = 12mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18$mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4 V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7 V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 7.0 V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.		−30		−130	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.			63	95	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX.	V_O = 2.4 V			50	μA
			V_O = 0.4 V			−50	

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2915AXM Min.	Am2915AXM Typ. (Note 2)	Am2915AXM Max.	Am2915AXC Min.	Am2915AXC Typ. (Note 2)	Am2915AXC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 130Ω		21	36		21	32	ns
t_{PLH}				21	36		21	32	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{HZ}, t_{LZ}				13	21		13	18	
t_s	Data Inputs (A or B)	C_L = 15pF, R_L = 2.0kΩ	15			12			ns
t_h			8.0			6.0			
t_s	Select Input (S)		28			25			ns
t_h			8.0			6.0			
t_{PW}	Driver Clock (DRCP) Pulse Width (HIGH)		20			17			ns
t_{PLH}	Bus to Receiver Output (Latch Enable)			18	33		18	30	ns
t_{PHL}				18	30		18	27	
t_{PLH}	Latch Enable to Receiver Output			21	33		21	30	ns
t_{PHL}				21	30		21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)		15			13			ns
t_h			6.0			4.0			
t_{ZH}, t_{ZL}	Output Control to Receiver Output	C_L = 5pF, R_L = 2.0kΩ		14	26		14	23	ns
t_{HZ}, t_{LZ}				14	26		14	23	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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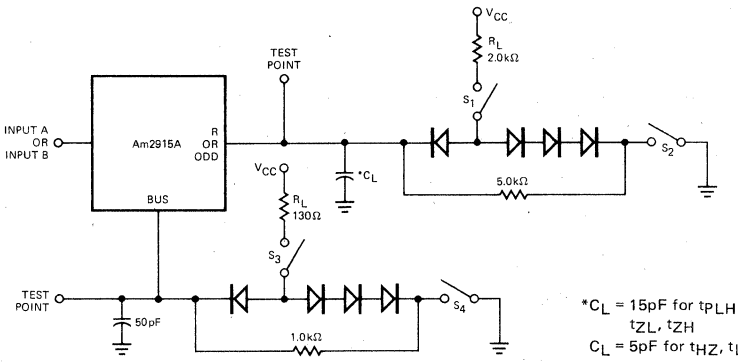
SWITCHING TEST CIRCUIT



*C_L = 15pF for t_{PLH}, t_{PHL}, t_{ZL}, t_{ZH}
C_L = 5pF for t_{HZ}, t_{LZ}

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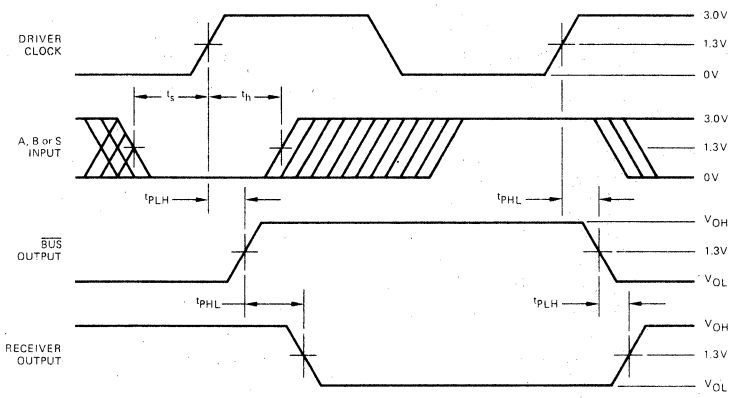
SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

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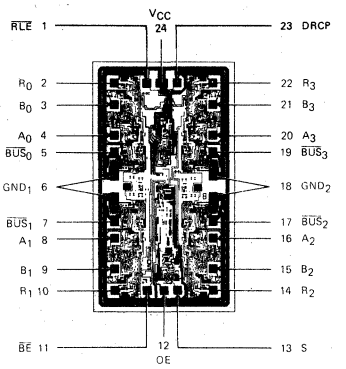
FUNCTIONAL TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

Metallization and Pad Layout



DIE SIZE .074" X .130"

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

$\overline{BUS}_0$, $\overline{BUS}_1$ $\overline{BUS}_2$, $\overline{BUS}_3$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

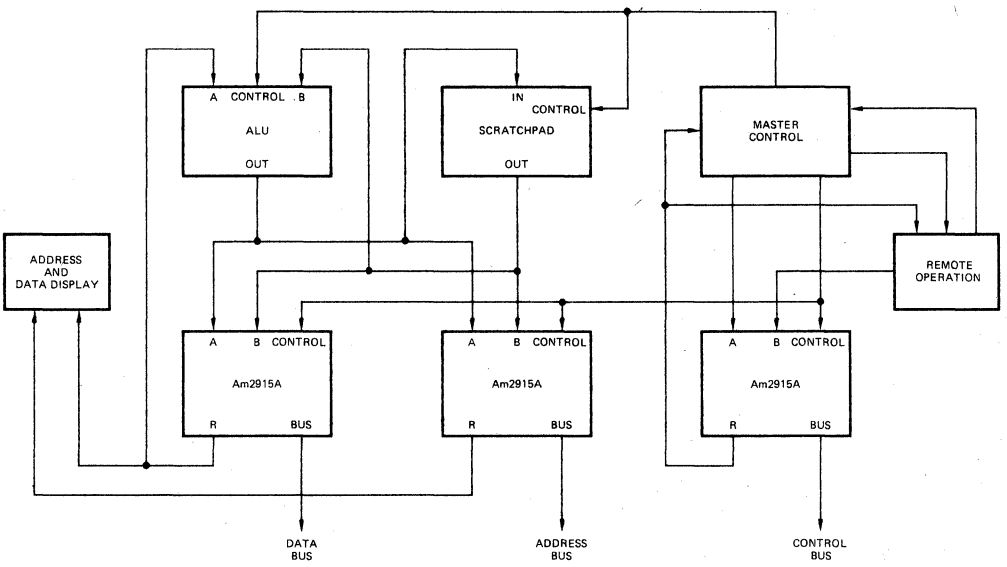
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2915APC	P-24	C	C-1
AM2915ADC	D-24	C	C-1
AM2915ADC-B	D-24	C	B-1
AM2915ADM	D-24	M	C-3
AM2915ADM-B	D-24	M	B-3
AM2915AFM	F-24-1	M	C-3
AM2915AFM-B	F-24-1	M	B-3
AM2915AXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2915AXM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

APPLICATIONS



The Am2915A is a universal Bus Transceiver useful for many system data, address, control and timing input/output interfaces.

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Am2916A

Quad Three-State Bus Transceiver with Interface Logic

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 48mA at 0.5V max.
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

FUNCTIONAL DESCRIPTION

The Am2916A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches. The device also contains a four-bit odd parity checker/generator.

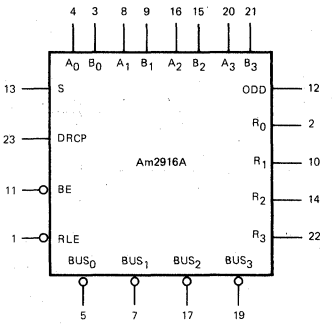
The LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data in non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input.

The Am2916A features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A or B field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

LOGIC SYMBOL



V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

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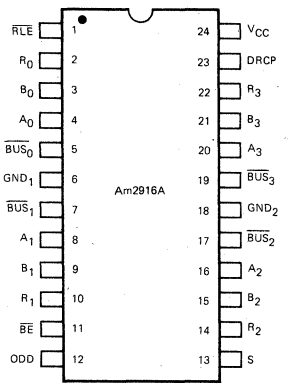
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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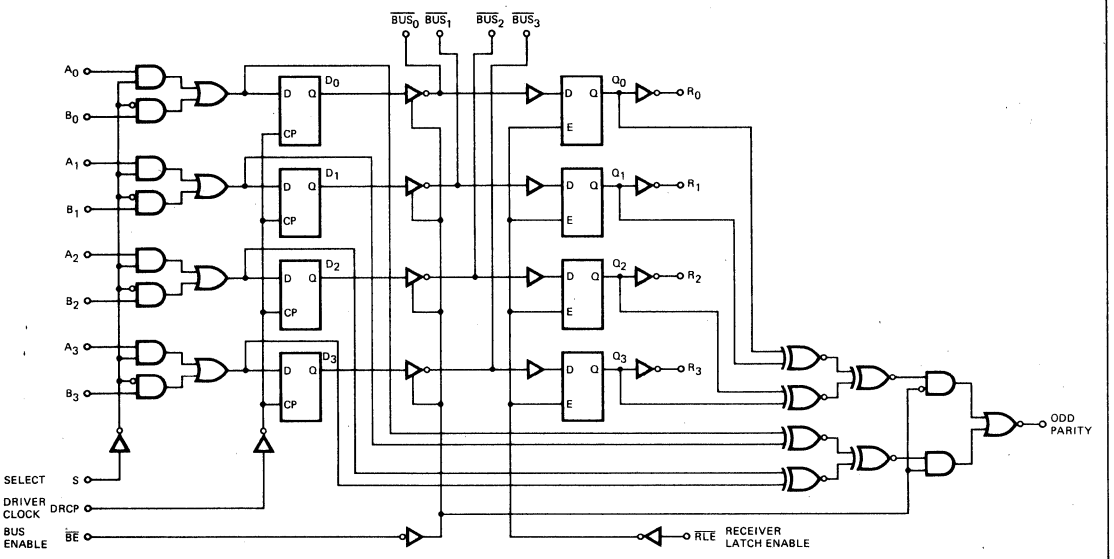
LOGIC DIAGRAM



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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	100mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2916AXC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V
Am2916AXM (MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50V V_{CC} MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ.	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 24mA			0.4	Volts
			I_{OL} = 48mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN.	COM'L, I_{OH} = −20mA	2.4			Volts
			MIL, I_{OH} = −15mA				
I_O	Bus Leakage Current (High Impedance)	V_{CC} = MAX. Bus enable = 2.4V	V_O = 0.4V			−200	μA
			V_O = 2.4V			50	
			V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V, V_{CC} = 0V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4V	COM'L			0.8	Volts
			MIL			0.7	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX., V_O = 0V		−50	−120	−225	mA

Am2916A
ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2916AXC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V
Am2916AXM (MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50V V_{CC} MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

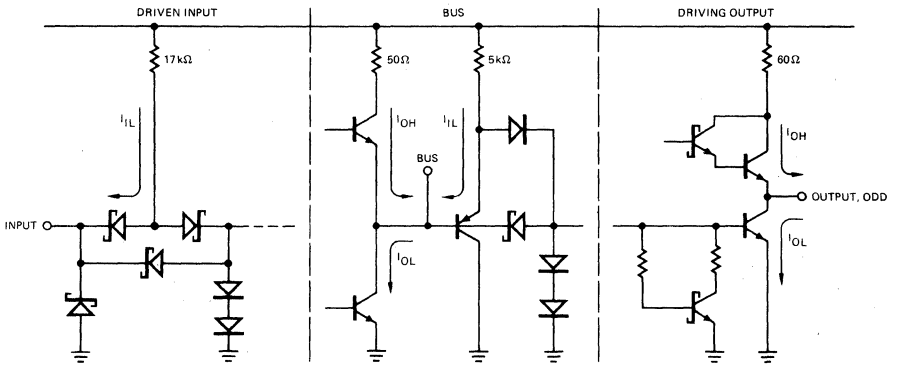
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN. $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1.0mA$	2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6mA$	2.4	3.4		
		$V_{CC} = 5.0V$, $I_{OH} = -100\mu A$		3.5			
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu A$ $V_{IN} = V_{IH}$ or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN. $V_{IN} = V_{IL}$ or V_{IH}	$I_{OL} = 4.0mA$		0.27	0.4	Volts
			$I_{OL} = 8.0mA$		0.32	0.45	
			$I_{OL} = 12mA$		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18mA$				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4V$	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7V$				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 7.0V$				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.	RECEIVER	−30		−130	mA
			PARITY	−20		−100	
I_{CC}	Power Supply Current	V_{CC} = MAX., All Inputs = GND			75	110	mA

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2916AXM Min.	Am2916AXM Typ. (Note 2)	Am2916AXM Max.	Am2916AXC Min.	Am2916AXC Typ. (Note 2)	Am2916AXC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF R_L (BUS) = 130Ω		21	36		21	32	ns
t_{PLH}				21	36		21	32	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{HZ}, t_{LZ}				13	21		13	18	
t_s	Data Inputs (A or B)	C_L = 15pF $R_L = 2.0k\Omega$	15			12			ns
t_h			8.0			6.0			
t_s	Select Inputs (S)		28			25			ns
t_h			8.0			6.0			
t_{PW}	Clock Pulse Width (HIGH)		20			17			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	33		18	30	ns
t_{PHL}				18	30		18	27	
t_{PLH}	Latch Enable to Receiver Output			21	33		21	30	ns
t_{PHL}				21	30		21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)		15			13			ns
t_h			6.0			4.0			
t_{PLH}	A or B Data to Odd Parity Output (Driver Enabled)			32	46		32	42	ns
t_{PHL}				26	40		26	36	
t_{PLH}	Bus to Odd Parity Output (Driver Inhibited, Latch Enabled)			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	36		21	32	ns
t_{PHL}				21	36		21	32	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test shoul not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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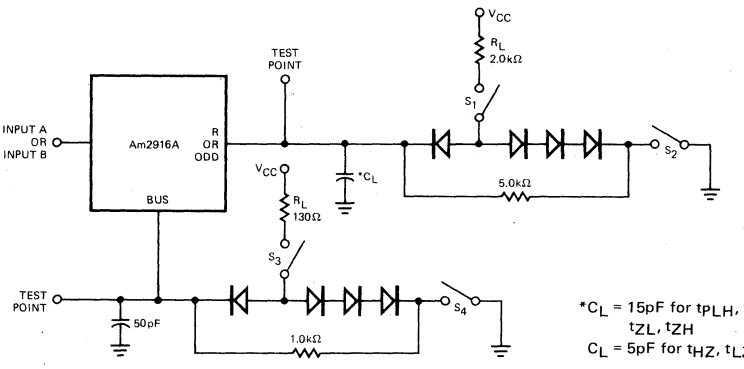
SWITCHING TEST CIRCUIT



*C_L = 15pF for t_{PLH}, t_{PHL}, t_{ZL}, t_{ZH}
C_L = 5pF for t_{HZ}, t_{LZ}

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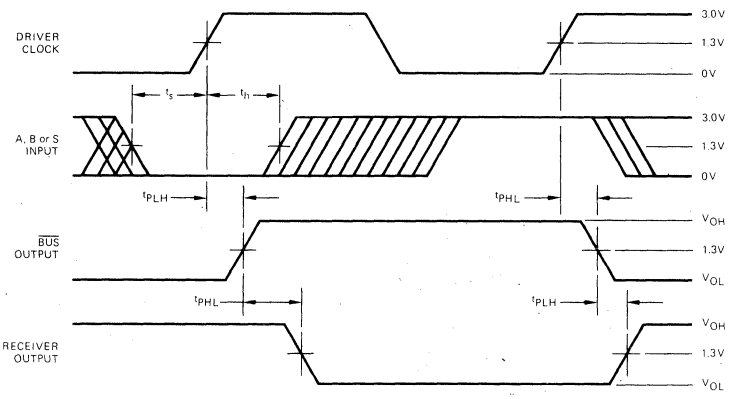
SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

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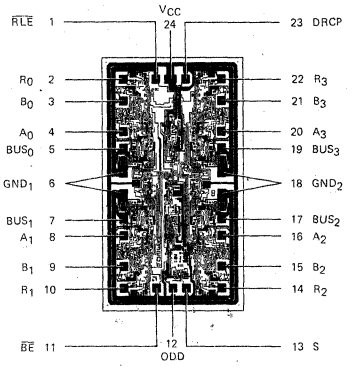
FUNCTION TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS_i}$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

Metallization and Pad Layout



'DIE SIZE .074" X .130"

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

$\overline{BUS_0}$, $\overline{BUS_1}$ $\overline{BUS_2}$, $\overline{BUS_3}$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

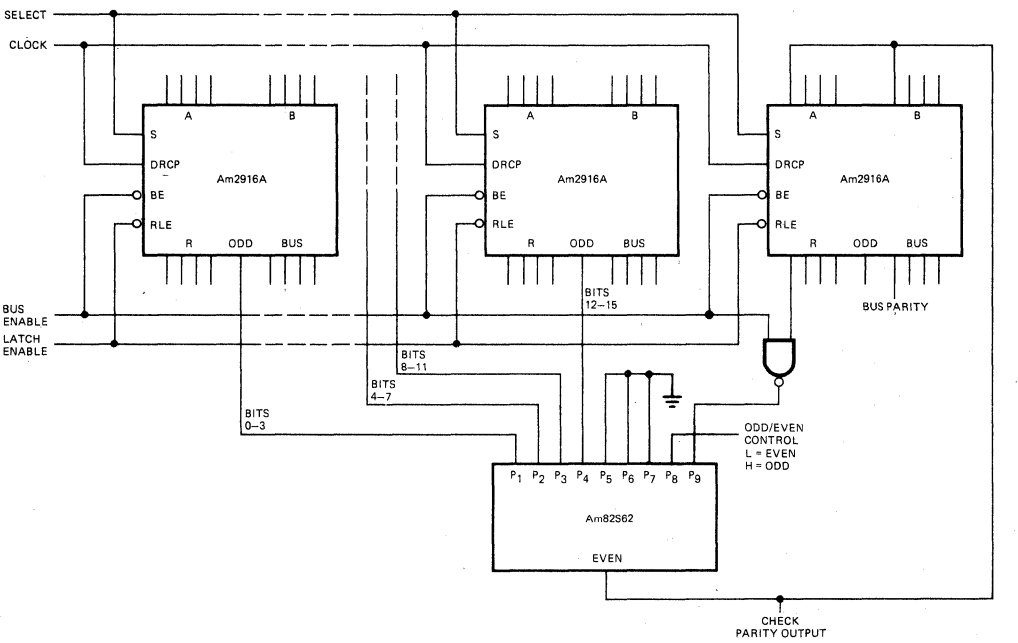
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2916APC	P-24	C	C-1
AM2916ADC	D-24	C	C-1
AM2916ADC-B	D-24	C	B-1
AM2916ADM	D-24	M	C-3
AM2916ADM-B	D-24	M	B-3
AM2916AFM	F-24-1	M	C-3
AM2916AFM-B	F-24-1	M	B-3
AM2916AXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2916AXM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

APPLICATIONS



Generating or checking parity for 16 data bits.

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Am2917A

Quad Three-State Bus Transceiver with Interface Logic

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- D-type register on driver
- Bus driver output can sink 48mA at 0.5V max.
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

FUNCTIONAL DESCRIPTION

The Am2917A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches, that feature three-state outputs. The device also contains a four-bit odd parity checker/generator.

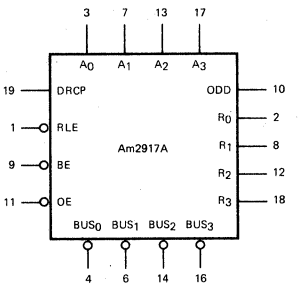
The LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled.

The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the A_i data into this driver register on the LOW-to-HIGH transition.

Data from the A input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

The Am2917A features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

LOGIC SYMBOL



V_{CC} = Pin 20
GND_1 = Pin 5
GND_2 = Pin 15

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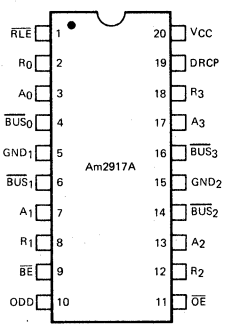
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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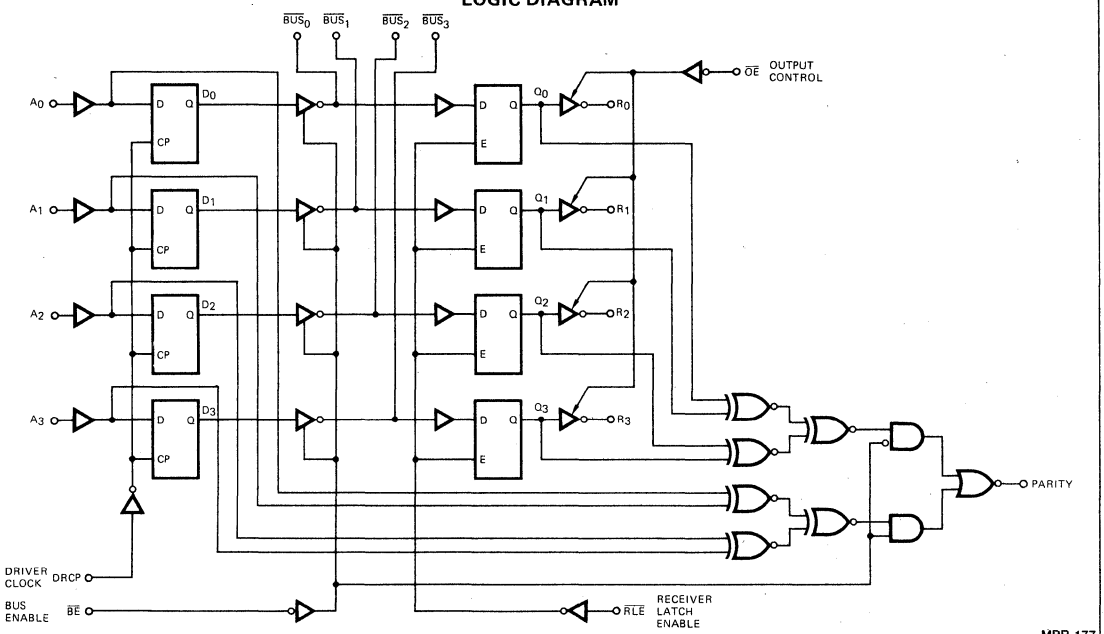
LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7 V
DC Output Current, Into Outputs (Except BUS)	30 mA
DC Output Current, Into Bus	100 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2917AXC (COM'L) T_A = 0°C to +70°C V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
Am2917AXM (MIL) T_A = −55°C to +125°C V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ.	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 24 mA			0.4	Volts
			I_{OL} = 48 mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN.	COM'L, I_{OH} = −20 mA	2.4			Volts
			MIL, I_{OH} = −15 mA				
I_O	Bus Leakage Current (High Impedance)	V_{CC} = MAX. Bus enable = 2.4 V	V_O = 0.4 V			−200	μA
			V_O = 2.4 V			50	
			V_O = 4.5 V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5 V V_{CC} = 0 V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4 V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4 V	COM'L			0.8	Volts
			MIL			0.7	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX. V_O = 0 V		−50	−120	−225	mA

Am2917A
ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2917AXC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
Am2917AXM (MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

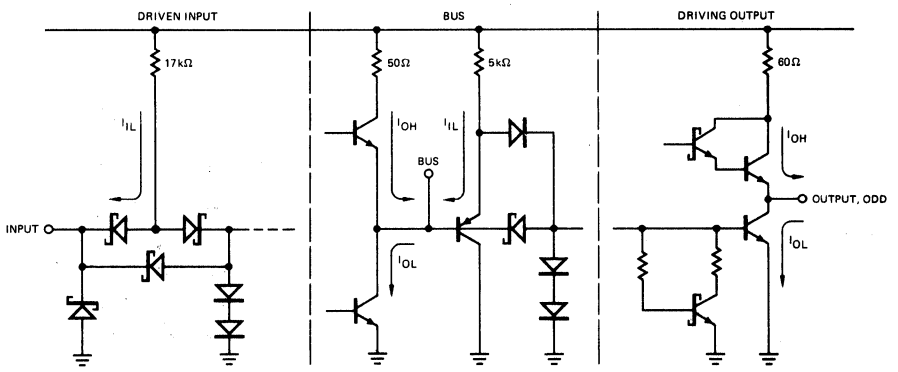
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1.0$mA	2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6$mA	2.4	3.4		
		V_{CC} = 5.0 V, $I_{OH} = -100\mu$A		3.5			
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu$A, $V_{IN} = V_{IH}$ or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 4.0 mA		0.27	0.4	Volts
			I_{OL} = 8.0 mA		0.32	0.45	
			I_{OL} = 12 mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18$mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4 V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7 V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 7.0 V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.	RECEIVER	−30		−130	mA
			PARITY	−20		−100	
I_{CC}	Power Supply Current	V_{CC} = MAX.			63	95	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX.	V_O = 2.4 V			50	μA
			V_O = 0.4 V			−50	

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2917AXM Min.	Am2917AXM Typ. (Note 2)	Am2917AXM Max.	Am2917AXC Min.	Am2917AXC Typ. (Note 2)	Am2917AXC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50 pF, R_L (BUS) = 130 Ω		21	36		21	32	ns
t_{PLH}				21	36		21	32	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{HZ}, t_{LZ}				13	21		13	18	
t_s	A Data Inputs	C_L = 15 pF, R_L = 2.0 kΩ	15			12			ns
t_h			8.0			6.0			
t_{PW}	Clock Pulse Width (HIGH)		20			17			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	33		18	30	ns
t_{PHL}				18	30		18	27	
t_{PLH}	Latch Enable to Receiver Output			21	33		21	30	ns
t_{PHL}				21	30		21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)		15			13			ns
t_h			6.0			4.0			
t_{PLH}	A Data to Odd Parity Out (Driver Enabled)			32	46		32	42	ns
t_{PHL}				26	40		26	36	
t_{PLH}	Bus to Odd Parity Out (Driver Inhibit)			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{ZH}, t_{ZL}	Output Control to Output			14	26		14	23	ns
t_{HZ}, t_{LZ}		C_L = 5 pF, R_L = 2.0 kΩ		14	26		14	23	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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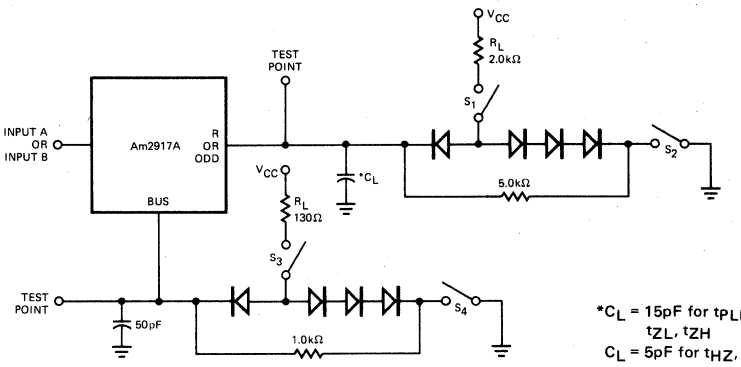
SWITCHING TEST CIRCUIT



*C_L = 15pF for t_{PLH}, t_{PHL}, t_{ZL}, t_{ZH}
C_L = 5pF for t_{HZ}, t_{LZ}

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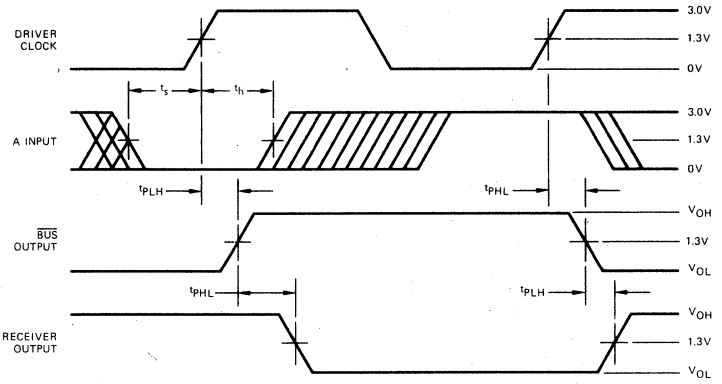
SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the BUS to R combinatorial delay.

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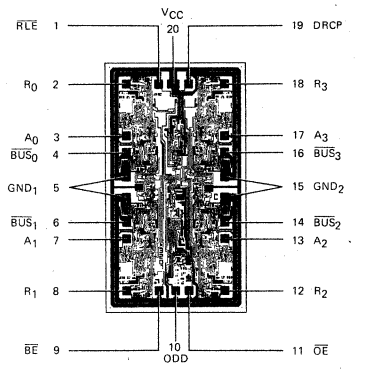
FUNCTION TABLE

INPUTS					INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
A_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	BUS_i	R_i	
X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	H	L	L	X	H	H	L	
X	X	X	H	X	X	NC	X	X	Latch received data
L	↑	X	X	X	L	X	X	X	Load driver register
H	↑	X	X	X	H	X	X	X	
X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	H	X	X	X	NC	X	X	X	
X	X	L	X	X	L	X	H	X	Drive Bus
X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

Metallization and Pad Layout



DIE SIZE .074" X .130"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2917APC	P-20	C	C-1
AM2917ADC	D-20	C	C-1
AM2917ADC-B	D-20	C	B-1
AM2917ADM	D-20	M	C-3
AM2917ADM-B	D-20	M	B-3
AM2917AFM	F-20	M	C-3
AM2917AFM-B	F-20	M	B-3
AM2917AXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2917AXM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V.
   M = −55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

DEFINITION OF FUNCTIONAL TERMS

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

BUS_0, BUS_1, BUS_2, BUS_3 The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

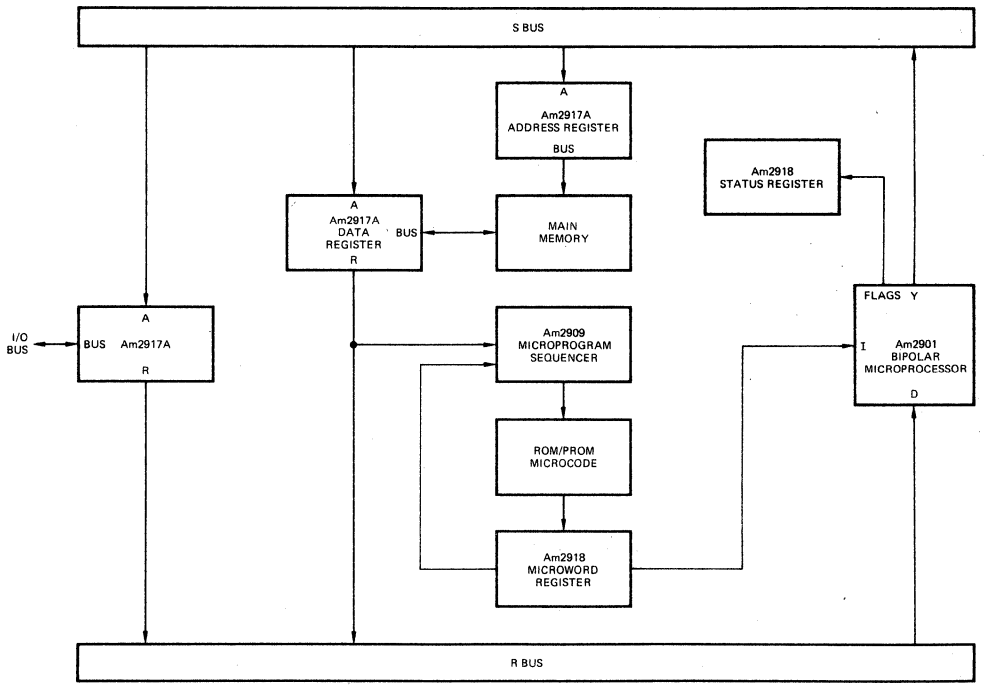
ODD Odd parity output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.

$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three-state receiver outputs are in the high-impedance state.

PARITY OUTPUT FUNCTION TABLE

$\overline{BE}$	ODD PARITY OUTPUT
L	ODD = $A_0 \oplus A_1 \oplus A_2 \oplus A_3$
H	ODD = $Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$

APPLICATIONS



The Am2917A can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high-speed Microprocessor Systems.

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Am2918

Quad D Register with Standard and Three-State Outputs

Distinctive Characteristics

- Advanced Schottky technology
- Four D-type flip-flops
- Four standard totem-pole outputs
- Four three-state outputs
- 75 MHz clock frequency

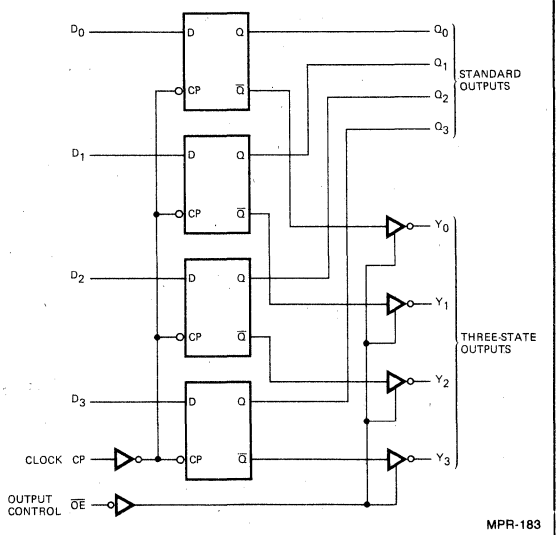
FUNCTIONAL DESCRIPTION

New Schottky circuits such as the Am2918 register provide the design engineer with additional flexibility in system configuration – especially with regard to bus structure, organization and speed. The Am2918 is a quadruple D-type register with four standard totem pole outputs and four three-state bus-type outputs. The 16-pin device also features a buffered common clock (CP) and a buffered common output control ($\overline{OE}$) for the Y outputs. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" ($\overline{OE}$) input is LOW. When the $\overline{OE}$ input is HIGH, the Y outputs are in the high-impedance state.

The Am2918 register can be used in bipolar microprocessor designs as an address register, status register, instruction register or for various data or microword register applications. Because of the unique design of the three-state output, the device features very short propagation delay from the clock to the Q or Y outputs. Thus, system performance and architectural design can be improved by using the Am2918 register. Other applications of Am2918 register can be found in microprogrammed display systems, communication systems and most general or special purpose digital signal processing equipment.

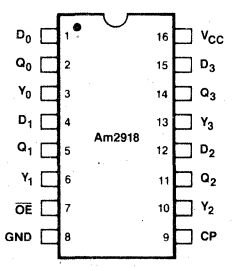
LOGIC DIAGRAM



RELATED PRODUCTS

Part No.	Description
Am29LS18	Low Power Version
Am2919	Quad Register

CONNECTION DIAGRAMS – Top Views



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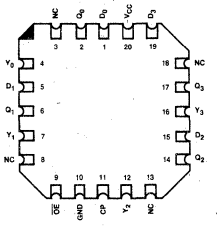
Note: Pin 1 is marked for orientation.

Leadless Chip Carrier
L-20-1



ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2918PC	P-16	C	C-1
AM2918DC	D-16	C	C-1
AM2918DC-B	D-16	C	B-1
AM2918DM	D-16	M	C-3
AM2918DM-B	D-16	M	B-3
AM2918FM	F-16	M	C-3
AM2918FM-B	F-16	M	B-3
AM2918LC	L-20-1	C	C-1
AM2918LC-B	L-20-1	C	B-1
AM2918LM	L-20-1	M	C-3
AM2918LM-B	L-20-1	M	B-3
AM2918XC	Dice	C	Visual inspection to MIL-STD-883. Method 2010B.
AM2918XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Flat-Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am2918XC	T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5% (COM'L)	MIN. = 4.75V	MAX. = 5.25V	
Am2918XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ± 10% (MIL)	MIN. = 4.5V	MAX. = 5.5V	

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Q	I_{OH} = −1mA MIL	2.5	3.4		Volts
				I_{OH} = −1mA COM'L	2.7	3.4		
			Y	XM, I_{OH} = −2mA	2.4	3.4		
				XC, I_{OH} = −6.5mA	2.4	3.4		
V_{OL}	Output LOW Voltage (Note 6)	V_{CC} = MIN., I_{OL} = 20mA; V_{IN} = V_{IH} or V_{IL}					0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V					−2.0	mA
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V					50	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_O	Y Output Off-State Leakage Current	V_{CC} = MAX.		V_O = 2.4V			50	μA
				V_O = 0.4V			−50	
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.			−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)				80	130	mA

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, T_A = 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (see Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test shoud not exceed one second.
5. I_{CC} is measured with all inputs at 4.5V and all outputs open.
6. Measured on Q outputs with Y outputs open. Measured on Y outputs with Q outputs open.

Switching Characteristics (T_A = +25°C, V_{CC} = 5.0V, R_L = 280Ω)

Parameters	Description		Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Clock to Q Output		C_L = 15pF		6.0	9.0	ns
t_{PHL}					8.5	13	
t_{pw}	Clock Pulse Width	HIGH		7.0			ns
		LOW		9.0			
t_s	Data			5.0			ns
t_h	Data			3.0			ns
t_{PLH}	Clock to Y Output (OE LOW)				6.0	9.0	ns
t_{PHL}					8.5	13	
t_{ZH}	Output Control to Output		C_L = 15 pF		12.5	19	ns
t_{ZL}					12	18	
t_{HZ}			C_L = 5.0 pF		4.0	6.0	
t_{LZ}					7.0	10.5	
f_{max}	Maximum Clock Frequency		C_L = 15pF	75	100		MHz

TRUTH TABLE

INPUTS			OUTPUTS		NOTES
$\overline{OE}$	CLOCK CP	D	Q	Y	
H	L	X	NC	Z	–
H	H	X	NC	Z	–
H	↑	L	L	Z	–
H	↑	H	H	Z	–
L	↑	L	L	L	–
L	↑	H	H	H	–
L	–	–	L	L	1
L	–	–	H	H	1

L = LOW
H = HIGH
X = Don't care

NC = No change
↑ = LOW to HIGH transition
Z = High impedance

Note: 1. When $\overline{OE}$ is LOW, the Y output will be in the same logic state as the Q output.

DEFINITION OF FUNCTIONAL TERMS

D_i The four data inputs to the register.

Q_i The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.

Y_i The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the Y_i outputs to the high-impedance state.

CP Clock. The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.

$\overline{OE}$ Output Control. When the $\overline{OE}$ input is HIGH, the Yi outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

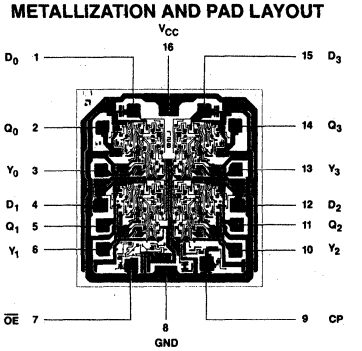
LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
D_0	1	1	–	–
Q_0	2	–	20	10*
Y_0	3	–	40/130	10*
D_1	4	1	–	–
Q_1	5	–	20	10*
Y_1	6	–	40/130	10*
$\overline{OE}$	7	1	–	–
GND	8	–	–	–
CP	9	1	–	–
Y_2	10	–	40/130	10*
Q_2	11	–	20	10*
D_2	12	1	–	–
Y_3	13	–	40/130	10*
Q_3	14	–	20	10*
D_3	15	1	–	–
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

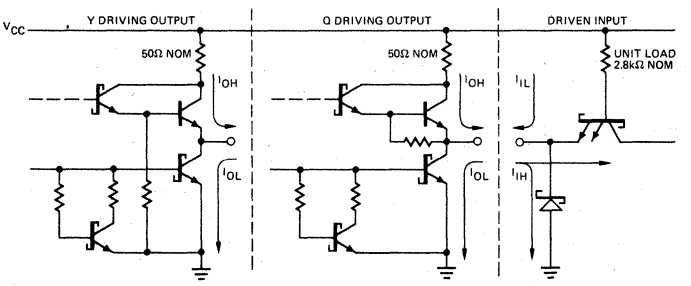
*Fan-out on each Q_i and Y_i output pair should not exceed 15 unit loads (30mA) for i = 0, 1, 2, 3.

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.070" X 0.072"

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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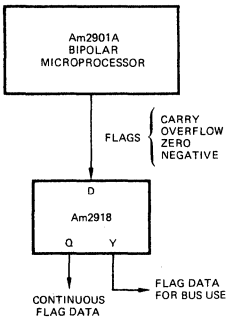
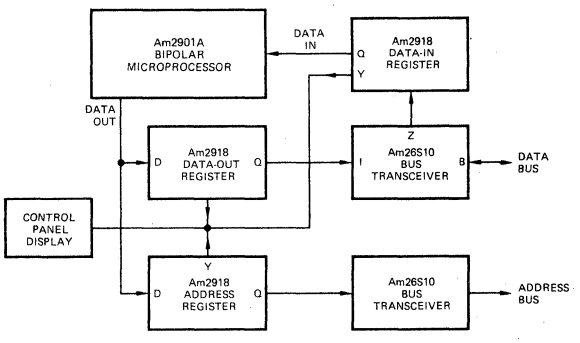
APPLICATIONS



The Am2918 as a 4-Bit status register



The Am2918 used as data-in, data-out and address registers.

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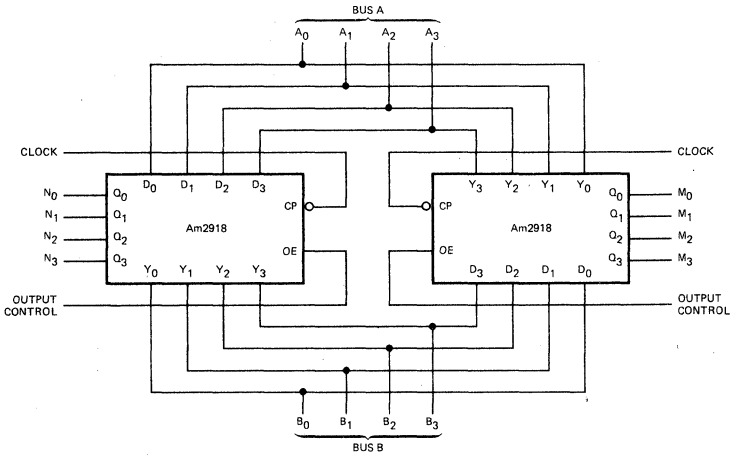

The Am2918 can be connected for bi-directional interface between two buses. The device on the left stores data from the A-bus and drives the A-bus. The device on the right stores data from the B-bus and drives the A-bus. The output control is used to place either or both drivers in the high-impedance state. The contents of each register are available for continuous usage at the N and M ports of the device.

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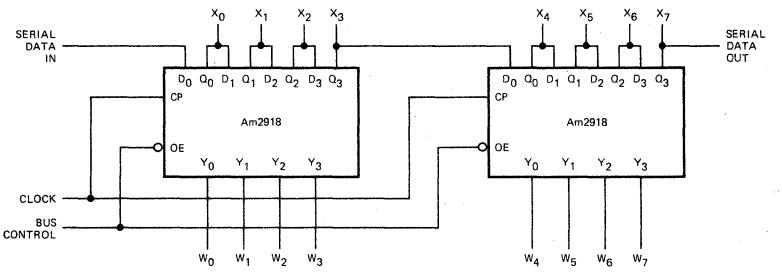


8-Bit serial to parallel converter with three-state output (W) and direct access to the register word (X).

MPR-189

Am29LS18

Quad D Register with Standard and Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Low-power Schottky version of the popular Am2918
- Four standard totem-pole outputs
- Four three-state outputs
- Four D-type flip-flops

RELATED PRODUCTS

Part No.	Description
Am25S18	Quad D Register
Am25LS2518	Quad D Register
Am25LS2519	Quad Register

FUNCTIONAL DESCRIPTION

The Am29LS18 consists of four D-type flip-flops with a buffered common clock. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

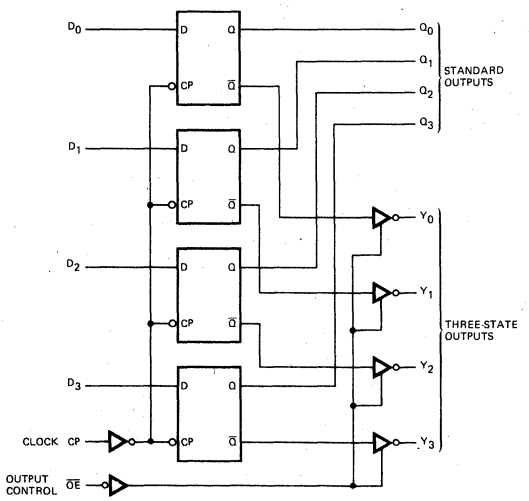
The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" ($\overline{OE}$) input is LOW. When the $\overline{OE}$ input is HIGH, the Y outputs are in the high-impedance state.

The Am29LS18 is a 4-bit, high-speed register intended for use in real-time signal processing systems where the standard outputs are used in a recursive algorithm and the three-state outputs provide access to a data bus to dump the results after a number of iterations.

The device can also be used as an address register or status register in computers or computer peripherals.

Likewise, the Am29LS18 is also useful in certain display applications where the standard outputs can be decoded to drive LED's (or equivalent) and the three-state outputs are bus organized for occasional interrogation of the data as displayed.

LOGIC DIAGRAM



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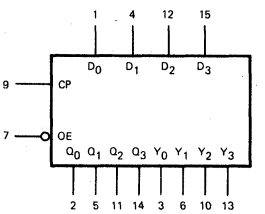
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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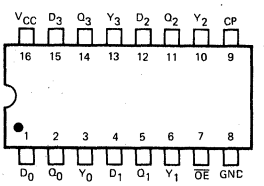
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75 V MAX. = 5.25 V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50 V MAX. = 5.50 V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	Q, $I_{OH} = -660\mu A$	MIL	2.5	3.4		Volts
				COM'L	2.7	3.4		
			Y	MIL, $I_{OH} = -1.0mA$	2.4	3.4		
				COM'L, $I_{OH} = 2.6mA$	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$				0.4	Volts
			$I_{OL} = 8.0mA$				0.45	
			$I_{OL} = 12mA$				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$					−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$					20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$					0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$				−20	μA
			$V_O = 2.4V$				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				17	28	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} is measured with all inputs at 4.5V and all outputs open.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

Am29LS18
SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Q_i			18	27	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}				18	27		
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)			18	27	ns	
t_{PHL}				18	27		
t_{pw}	Clock Pulse Width	LOW	18			ns	
		HIGH	15				
t_s	Data		15			ns	
t_h	Data		5.0			ns	
t_{ZH}	$\overline{OE}$ to Y_i			7.0	11	ns	
t_{ZL}				8	12		
t_{HZ}	$\overline{OE}$ to Y_i			14	21	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				12	18		
f_{max}	Maximum Clock Frequency (Note 1)		35	50		MHz	

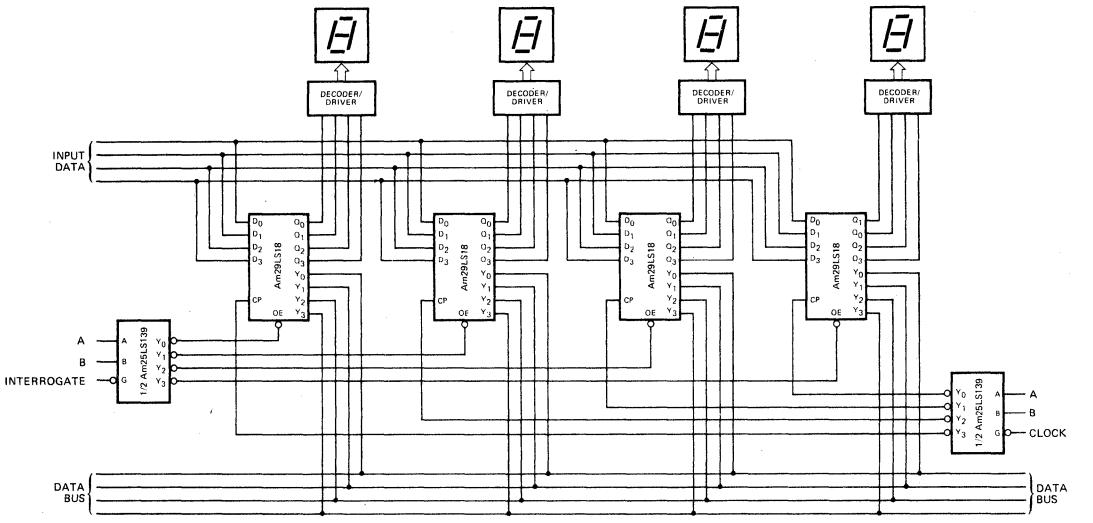
Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am29LS18PC, DC: T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%		Am29LS18DM, FM: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%		Units	Test Conditions
			Min.	Max.	Min.	Max.		
t_{PLH}	Clock to Q_i			38		45	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}				38		45		
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)			35		40	ns	
t_{PHL}				35		40		
t_{pw}	Clock Pulse Width	LOW	20		20		ns	
		HIGH	20		20			
t_s	Data		15		15		ns	
t_h	Data		5.0		5.0		ns	
t_{ZH}	$\overline{OE}$ to Y_i			15		17	ns	
t_{ZL}				16		17		
t_{HZ}	$\overline{OE}$ to Y_i			27		30	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				24		30		
f_{max}	Maximum Clock Frequency (Note 1)		30		25		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

APPLICATIONS



The Am29LS18 used as a display register with bus interrogate capability.

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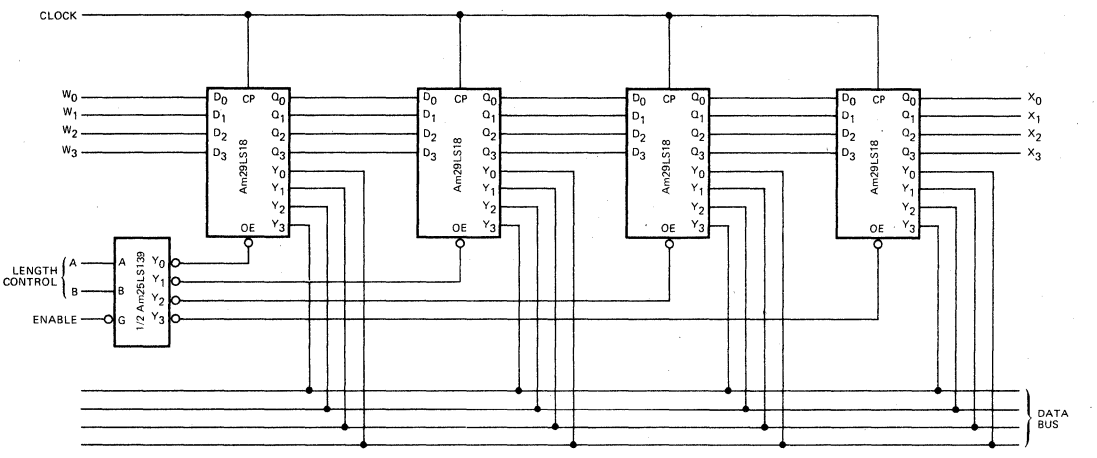
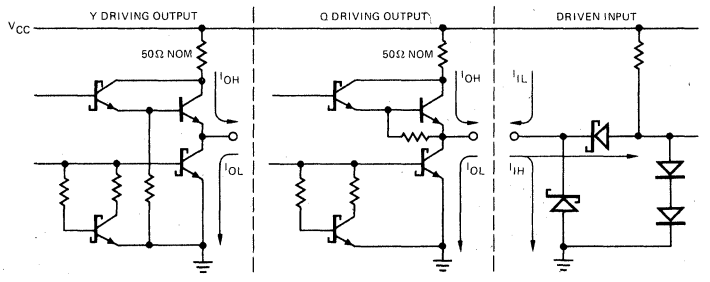


The Am29LS18 as a variable length (1, 2, 3 or 4 word) shift register.

MPR-194

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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DEFINITION OF FUNCTIONAL TERMS

D_i The four data inputs to the register.

Q_i The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.

Y_i The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the Y_i outputs to the high-impedance state.

CP Clock. The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.

$\overline{OE}$ Output Control. When the $\overline{OE}$ input is HIGH, the Yi outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

TRUTH TABLE

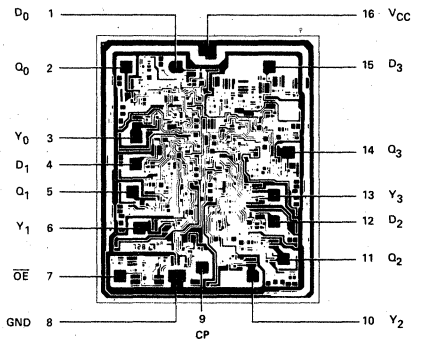
INPUTS			OUTPUTS		NOTES
$\overline{OE}$	CLOCK CP	D	Q	Y	
H	L	X	NC	Z	–
H	H	X	NC	Z	–
H	↑	L	L	Z	–
H	↑	H	H	Z	–
L	↑	L	L	L	–
L	↑	H	H	H	–
L	–	–	L	L	1
L	–	–	H	H	1

L = LOW
H = HIGH
X = Don't care

NC = No change
↑ = LOW to HIGH transition
Z = High impedance

Note: 1. When $\overline{OE}$ is LOW, the Y output will be in the same logic state as the Q output.

Metallization and Pad Layout



DIE SIZE 0.083" x 0.099"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM29LS18PC	P-16	C	C-1
AM29LS18DC	D-16	C	C-1
AM29LS18DC-B	D-16	C	B-1
AM29LS18DM	D-16	M	C-3
AM29LS18DM-B	D-16	M	B-3
AM29LS18FM	F-16	M	C-3
AM29LS18FM-B	F-16	M	B-3
AM29LS18XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM29LS18XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = – 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am2919

Quad Register with Dual Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Two sets of three-state outputs
- Four D-type flip-flops
- Polarity control on one set of outputs
- Buffered common clock enable
- Buffered common asynchronous clear
- Separate buffered common output enable for each set of outputs

RELATED PRODUCTS

Part No.	Description
Am25LS2519	Quad Register
Am25LS2518	Quad D Register

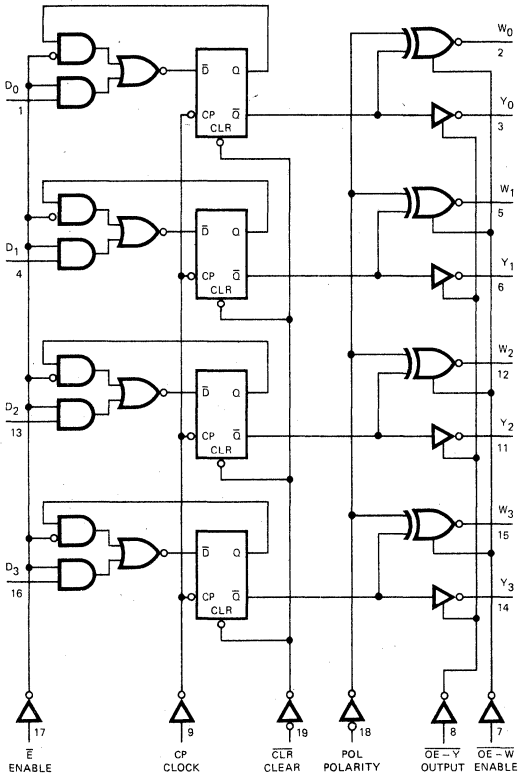
FUNCTIONAL DESCRIPTION

The Am2919 consists of four D-type flip-flops with a buffered common clock enable. Information meeting the set-up and hold time requirements of the D inputs is transferred to the flip-flop outputs on the LOW-to-HIGH transition of the clock. Data on the Q outputs of the flip-flops is enabled at the three-state outputs when the output control ($\overline{OE}$) input is LOW. When the appropriate $\overline{OE}$ input is HIGH, the outputs are in the high impedance state. Two independent sets of outputs—W and Y—are provided such that the register can simultaneously and independently drive two buses. One set of outputs contains a polarity control such that the outputs can either be inverting or non-inverting.

The device also features an active LOW asynchronous clear. When the clear input is LOW, the Q output of the internal flip-flops are forced LOW independent of the other inputs. The Am2919 is packaged in a space-saving (0.3-inch row spacing) 20-pin package.

5

LOGIC DIAGRAM



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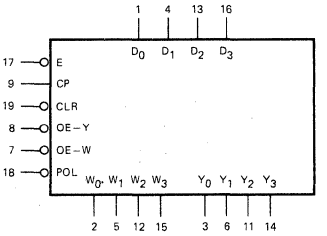
LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

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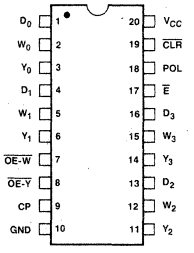
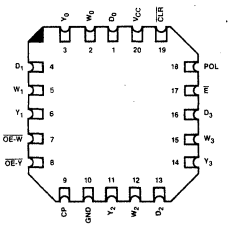
CONNECTION DIAGRAMS
Top Views

P-20, D-20



Leadless Chip Carrier
L-20-1



F-20 pin configuration identical to D-20, P-20.

Note: Pin 1 is marked for orientation.

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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	MIL, $I_{OH} = -1.0mA$		2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6mA$		2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$				0.4	Volts
			$I_{OL} = 8.0mA$				0.45	
			$I_{OL} = 12mA$				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$					−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$					20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$					0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$				−20	μA
			$V_O = 2.4V$				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.		MIL		24	36	mA
				COM'L		24	39	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Inputs grounded; outputs open.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

FUNCTION TABLE

FUNCTION	INPUTS							INTERNAL	OUTPUTS	
	CP	D_i	$\overline{E}$	$\overline{CLR}$	POL	$\overline{OE\text{-}W}$	$\overline{OE\text{-}Y}$	Q	W_i	Y_i
Output Three-State Control	X	X	X	X	X	H	L	NC	Z	Enabled
	X	X	X	X	X	L	H	NC	Enabled	Z
	X	X	X	X	X	H	H	NC	Z	Z
	X	X	X	X	X	L	L	NC	Enabled	Enabled
W_i Polarity	X	X	X	X	L	L	L	NC	Non-Inverting	Non-Inverting
	X	X	X	X	H	L	L	NC	Inverting	Non-Inverting
Asynchronous Clear	X	X	X	L	L	L	L	L	L	L
	X	X	X	L	H	L	L	L	H	L
Clock Enabled	↑	X	H	H	X	X	X	NC	NC	NC
	↑	L	L	H	L	L	L	L	L	L
	↑	L	L	H	H	L	L	L	H	L
	↑	H	L	H	L	L	L	H	H	H
	↑	H	L	H	H	L	L	H	L	H

L = LOW H = HIGH Z = High Impedance NC = No Change X = Don't Care ↑ = LOW-to-HIGH Transition

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PHL}	Clock to Y_i			22	33	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}				20	30		
t_{PLH}	Clock to W_i (Either Polarity)			24	36	ns	
t_{PHL}				24	36		
t_{PHL}	Clear to Y_i			29	43	ns	
t_{PLH}	Clear to W_i			25	37	ns	
t_{PHL}				30	45		
t_{PLH}	Polarity to W_i			23	34	ns	
t_{PHL}				25	37		
t_{pw}	Clear		18			ns	
t_{pw}	Clock Pulse Width	LOW	15			ns	
		HIGH	18				
t_s	Data		15			ns	
t_h	Data		5			ns	
t_s	Data Enable		20			ns	
t_h	Data Enable		0			ns	
t_s	Set-up Time, Clear Recovery (Inactive) to Clock		20	15		ns	
t_{ZH}	Output Enable to W or Y			11	17	ns	
t_{ZL}				13	20		
t_{HZ}	Output Enable to W or Y			13	20	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				11	17		
f_{max}	Maximum Clock Frequency (Note 1)		35	45		MHz	C_L = 15pF, R_L = 2.0kΩ

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am2919PC, DC T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%		Am2919DM, FM T_A = −55°C to +125°C, V_{CC} = 5.0V ±10%		Units	Test Conditions
			Min.	Max.	Min.	Max.		
t_{PLH}	Clock to Y_i			39		42	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}				39		45		
t_{PLH}	Clock to W_i (Either Polarity)			41		43	ns	
t_{PHL}				44		48		
t_{PHL}	Clear to Y_i			52		58	ns	
t_{PLH}	Clear to W_i			42		43	ns	
t_{PHL}				51		53		
t_{PLH}	Polarity to W_i			41		45	ns	
t_{PHL}				42		44		
t_{pw}	Clear		20		20		ns	
t_{pw}	Clock	LOW	20		20		ns	
		HIGH	20		20			
t_s	Data		15		15		ns	
t_h	Data		10		10		ns	
t_s	Data Enable		25		25		ns	
t_h	Data Enable		0		0		ns	
t_s	Set-up Time, Clear Recovery (Inactive) to Clock		23		24		ns	
t_{ZH}	Output Enable to W_i or Y_i			24		27	ns	
t_{ZL}				29		35		
t_{HZ}	Output Enable to W_i or Y_i			33		45	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				22		26		
f_{max}	Maximum Clock Frequency (Note 1)		30		25		MHz	C_L = 50pF, R_L = 2.0kΩ

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

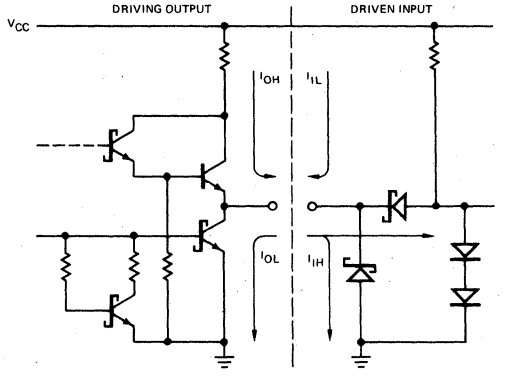
D_i	Any of the four D flip-flop data lines.
$\overline{E}$	Clock Enable. When LOW, the data is entered into the register on the next clock LOW-to-HIGH transition. When HIGH, the data in the register remains unchanged, regardless of the data in.
CP	Clock Pulse. Data is entered into the register on the LOW-to-HIGH transition.
$\overline{OE}$-W, $\overline{OE}$-Y	Output Enable. When $\overline{OE}$ is LOW, the register is enable to the output. When HIGH, the output is in the high-impedance state. The $\overline{OE}$-W controls the W set of outputs, and $\overline{OE}$-Y controls the Y set.
Y_i	Any of the four non-inverting three-state output lines.
W_i	Any of the four three-state outputs with polarity control.
POL	Polarity Control. The W_i outputs will be non-inverting when POL is LOW, and when it is HIGH, the outputs are inverting.
$\overline{CLR}$	Asynchronous Clear. When $\overline{CLR}$ is LOW, the internal Q flip-flops are reset to LOW.

GUARANTEED LOADING RULES OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and –0.36mA measured at 0.4V LOW.

Pin No.'s	Input/Output	Input Load	Output HIGH MIL	Output HIGH COM'L	Output LOW MIL	Output LOW COM'L
1	D_0	1.0	–	–	–	–
2	W_0	–	50	130	33	33
3	Y_0	–	50	130	33	33
4	D_1	1.0	–	–	–	–
5	W_1	–	50	130	33	33
6	Y_1	–	50	130	33	33
7	$\overline{OE}$-W	1.0	–	–	–	–
8	$\overline{OE}$-Y	1.0	–	–	–	–
9	CP	1.0	–	–	–	–
10	GND	–	–	–	–	–
11	Y_2		50	130	33	33
12	W_2		50	130	33	33
13	D_2	1.0	–	–	–	–
14	Y_3	–	50	130	33	33
15	W_3	–	50	130	33	33
16	D_3	1.0	–	–	–	–
17	$\overline{E}$	1.0	–	–	–	–
18	POL	1.0	–	–	–	–
19	$\overline{CLR}$	1.0	–	–	–	–
20	V_{CC}	–	–	–	–	–

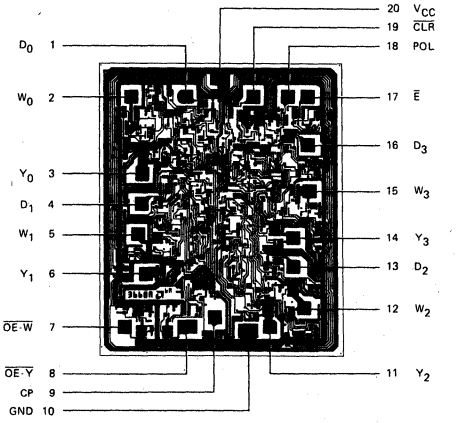
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

MPR-199

Metallization and Pad Layout



DIE SIZE 0.083" X 0.099"

ORDERING INFORMATION

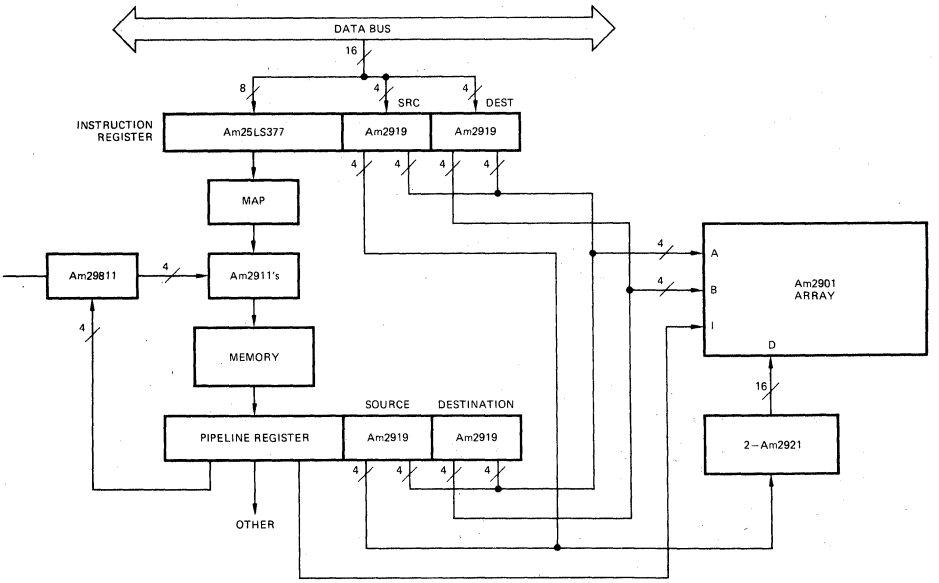
Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2919PC	P-20	C	C-1
AM2919DC	D-20	C	C-1
AM2919DC-B	D-20	C	B-1
AM2919DM	D-20	M	C-3
AM2919DM-B	D-20	M	B-3
AM2919FM	F-20	M	C-3
AM2919FM-B	F-20	M	B-3
AM2919LC	L-20-1	C	C-1
AM2919LC-B	L-20-1	C	B-1
AM2919LM	L-20-1	M	C-3
AM2919LM-B	L-20-1	M	B-3
AM2919XC	Dice	C	Visual inspection to MIL-STD-883. Method 2010B.
AM2919XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Flat-Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

5

APPLICATION



The Am2919 provides for easy control of the selection of source and destination register addresses for the Am2901. These controls can emanate from both the instruction register and the pipeline register. The control is accomplished by three-state action at the Am2919 outputs. Four different register outputs can be selected by the B address which is the destination register in the Am2901. Two registers can be selected for the Am2901 A input which is a second RAM source.

The other pair of three-state outputs can be used for function control select as shown with the Am2921. Here, bit set, bit clear, bit toggle and bit test on any of the 16 bits can be performed.

MPR-200

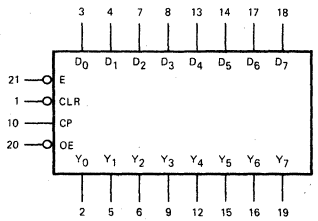
Am2920

Octal D-Type Flip-Flop with Clear, Clock Enable and Three-State Control

DISTINCTIVE CHARACTERISTICS

- Buffered common clock enable input
- Buffered common asynchronous clear input
- Three-state outputs
- 8-bit, high-speed parallel register with positive edge-triggered, D-type flip-flops

LOGIC SYMBOL



V_{CC} = Pin 22

GND = Pin 11

FUNCTIONAL DESCRIPTION

The Am2920 is an 8-bit register built using advanced Low-Power Schottky technology. The register consists of eight D-type flip-flops with a buffered common clock, a buffered common clock enable, a buffered asynchronous clear input, and three-state outputs.

When the clear input is LOW, the internal flip-flops of the register are reset to logic 0 (LOW), independent of all other inputs. When the clear input is HIGH, the register operates in the normal fashion.

When the three-state output enable ($\overline{OE}$) input is LOW, the Y outputs are enabled and appear as normal TTL outputs. When the output enable ($\overline{OE}$) input is HIGH, the Y outputs are in the high impedance (three-state) condition. This does not affect the internal state of the flip-flop Q output.

The clock enable input ($\overline{E}$) is used to selectively load data into the register. When the $\overline{E}$ input is HIGH, the register will retain its current data. When the $\overline{E}$ is LOW, new data is entered into the register on the LOW-to-HIGH transition of the clock input.

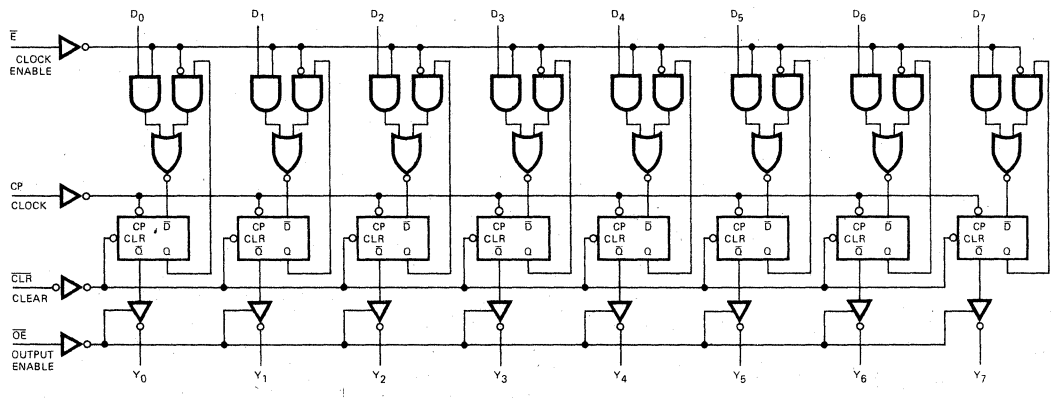
This device is packaged in a space-saving (0.4-inch row spacing) 22-pin package and in a 24-pin flatpack.

RELATED PRODUCTS

Part No.	Description
Am25LS2520	Octal D-Type Flip-Flop
Am2918	Quad D-Registers
Am2954/55	Octal D-Registers
Am29821-26	8, 9, 10-Bit Registers

MPR-203

LOGIC DIAGRAM



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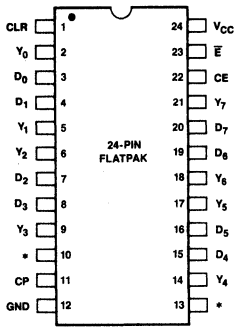
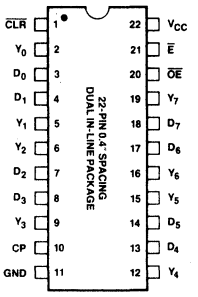
CONNECTION DIAGRAMS
Top Views

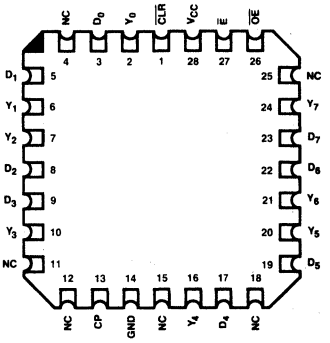
F-24



P-22, D-22



Leadless Chip Carrier
L-28-1



Note: Pin 1 is marked for orientation.

*Reserved – do not use.

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2920PC	P-22	C	C-1
AM2920DC	D-22	C	C-1
AM2920DC-B	D-22	C	B-1
AM2920DM	D-22	M	C-3
AM2920DM-B	D-22	M	B-3
AM2920FM	F-24	M	C-3
AM2920FM-B	F-24	M	B-3
AM2920LC	L-28-1	C	C-1
AM2920LC-B	L-28-1	C	B-1
AM2920LM	L-28-1	M	C-3
AM2920LM-B	L-28-1	M	B-3
AM2920XC	Dice	C	Visual inspection to MIL-STD-883. Method 2010B.
AM2920XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Flat-Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN. $V_{IN} = V_{IH}$ or V_{IL}	MIL, $I_{OH} = -1.0mA$		2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6mA$		2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN. $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$				0.4	Volts
			$I_{OL} = 8.0mA$				0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$					−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$					20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$					0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$				−20	μA
			$V_O = 2.4V$				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				24	37	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All outputs open, $\overline{E}$ = GND, Di inputs = CLR = $\overline{OE}$ = 4.5V. Apply momentary ground, then 4.5V to clock input.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)			18	27	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}				24	36		
t_{PHL}	Clear to Y			22	35	ns	
t_s	Data (D_i)		10	3		ns	
t_h	Data (D_i)		10	3		ns	
t_s	Enable ($\overline{E}$)	Active	15	10		ns	
		Inactive	20	12			
t_h	Enable ($\overline{E}$)		0	0		ns	
t_s	Clear Recovery (In-Active) to Clock		11	7		ns	
t_{pw}	Clock	HIGH	20	14		ns	
		LOW	25	13			
t_{pw}	Clear		20	13		ns	
t_{ZH}	$\overline{OE}$ to Y_i			9	13	ns	
t_{ZL}				14	21		
t_{HZ}	$\overline{OE}$ to Y_i			20	30	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				24	36		
f_{max}	Maximum Clock Frequency (Note 1)			40		MHz	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am2920PC,DC T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5% Min.	Am2920PC,DC Max.	Am2920DM,FM T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10% Min.	Am2920DM,FM Max.	Units	Test Conditions
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)			33		39	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}				45		54		
t_{PHL}	Clear to Y			43		51	ns	
t_s	Data (D_i)		12		15		ns	
t_h	Data (D_i)		12		15		ns	
t_s	Enable ($\overline{E}$)	Active	17		20		ns	
		Inactive	20		23			
t_h	Enable ($\overline{E}$)		0		0		ns	
t_s	Clear Recovery (In-Active) to Clock		13		15		ns	
t_{pw}	Clock	HIGH	25		30		ns	
		LOW	30		35			
t_{pw}	Clear		22		25		ns	
t_{ZH}	$\overline{OE}$ to Y_i			19		25	ns	
t_{ZL}				30		39		
t_{HZ}	$\overline{OE}$ to Y_i			35		40	ns	C_L = 5.0 pF, R_L = 2.0 kΩ
t_{LZ}				39		42		
f_{max}	Maximum Clock Frequency (Note 1)		25		20		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

D_i The D flip-flop data inputs.

$\overline{CLR}$ When the clear input is LOW, the Q_i outputs are LOW, regardless of the other inputs. When the clear input is HIGH, data can be entered into the register.

CP Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.

Y_i The register three-state outputs.

$\overline{E}$ Clock Enable. When the clock enable is LOW, data on the D_i input is transferred to the Q_i output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_i outputs do not change state, regardless of the data or clock input transitions.

$\overline{OE}$ Output Control. When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

FUNCTION TABLE

	Inputs					Internal	Outputs
Function	$\overline{OE}$	$\overline{CLR}$	$\overline{E}$	D_i	CP	Q_i	Y_i
Hi-Z	H	X	X	X	X	X	Z
Clear	H	L	X	X	X	L	Z
	L	L	X	X	X	L	L
Hold	H	H	H	X	X	NC	Z
	L	H	H	X	X	NC	NC
Load	H	H	L	L	↑	L	Z
	H	H	L	H	↑	H	Z
	L	H	L	L	↑	L	L
	L	H	L	H	↑	H	H

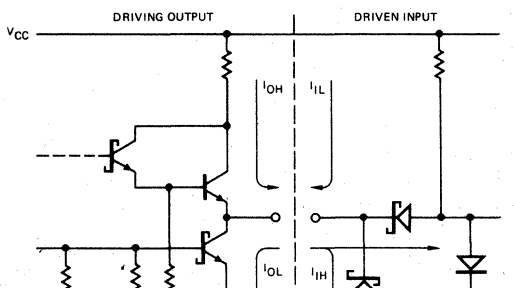
H = HIGH
L = LOW
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

GUARANTEED LOADING RULES OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

		Am2920				
		Input	Output HIGH		Output LOW	
Pin No.'s	Input/Output	Load	MIL	COM'L	MIL	COM'L
1	$\overline{CLR}$	1	–	–	–	–
2	Y_0	–	50	130	22	22
3	D_0	1	–	–	–	–
4	D_1	1	–	–	–	–
5	Y_1	–	50	130	22	22
6	Y_2	–	50	130	22	22
7	D_2	1	–	–	–	–
8	D_3	1	–	–	–	–
9	Y_3	–	50	130	22	22
10	CP	1	–	–	–	–
11	GND	–	–	–	–	–
12	Y_4	–	50	130	22	22
13	D_4	1	–	–	–	–
14	D_5	1	–	–	–	–
15	Y_5	–	50	130	22	22
16	Y_6	–	50	130	22	22
17	D_6	1	–	–	–	–
18	D_7	1	–	–	–	–
19	Y_7	–	50	130	22	22
20	$\overline{OE}$	1	–	–	–	–
21	$\overline{E}$	1	–	–	–	–
22	V_{CC}	–	–	–	–	–

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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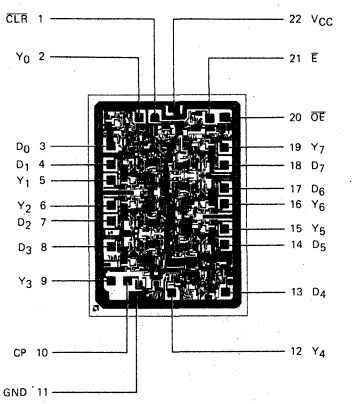
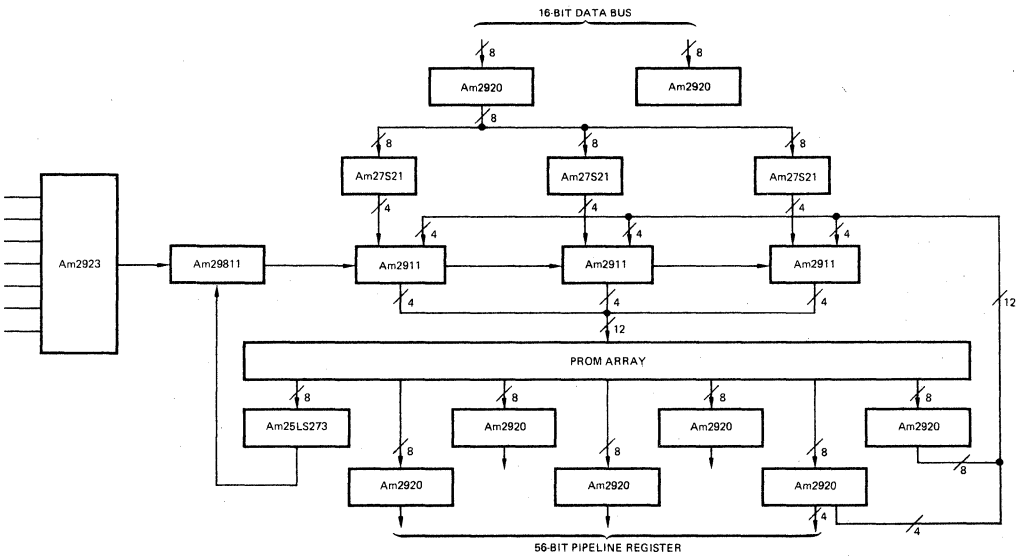
METALLIZATION AND PAD LAYOUT



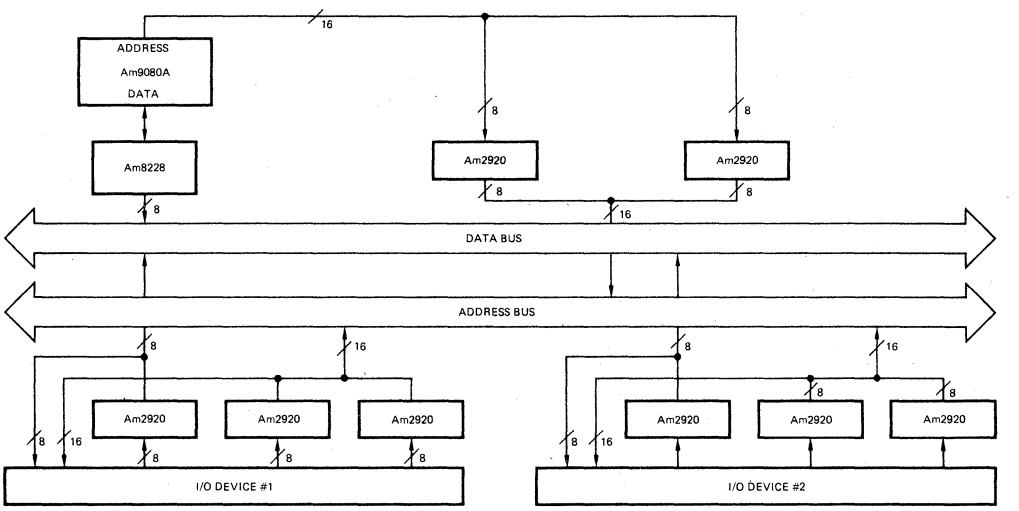
DIE SIZE 0.080" X 0.111"

APPLICATIONS



A typical Computer Control Unit for a microprogrammed machine.

MPR-205



The Am2920 is a useful device in interfacing with the Am9080A system buses.

MPR-206

Am2921

One-of-Eight Decoder with Three-State Outputs and Polarity Control

DISTINCTIVE CHARACTERISTICS

- Three-state decoder outputs
- Buffered common output polarity control
- Inverting and non-inverting enable inputs
- AC parameters specified over operating temperature and power supply ranges.

RELATED PRODUCTS

Part No.	Description
Am25LS2536	8-Bit Decoder
Am25LS2537	1 of 10 Decoder
Am25LS2538	1 of 8 Decoder
Am25LS2539	Dual 1 of 4 Decoder
Am2924	3 to 8 Line Decoder/Demultiplexer

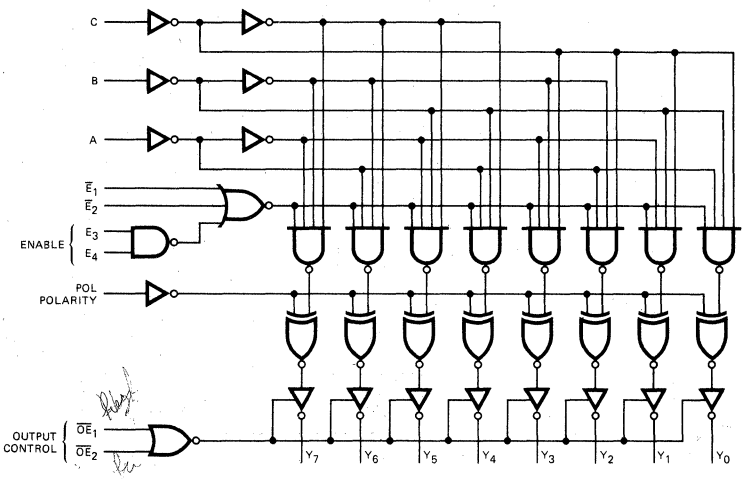
FUNCTIONAL DESCRIPTION

The Am2921 is a three-line to eight-line decoder/demultiplexer fabricated using advanced Low-Power Schottky technology. The decoder has three buffered select inputs A, B, and C, which are decoded to one-of-eight Y outputs. Two active-HIGH and two active-LOW enables can be used for gating the decoder or can be used with incoming data for demultiplexing applications.

A separate polarity (POL) input can be used to force the function active-HIGH or active-LOW at the output. Two separate active-LOW output enables ($\overline{OE}$) inputs are provided. If either $\overline{OE}$ input is HIGH, the output is in the high impedance (off) state. When the POL input is LOW, the Y outputs are active-HIGH and when the POL input is HIGH, the Y outputs are active-LOW.

The device is packaged in a space saving (0.3-inch row spacing) 20-pin package.

LOGIC DIAGRAM
One-of-Eight Decoder



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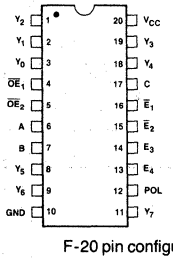
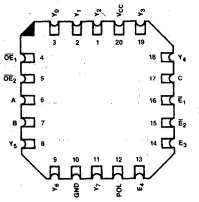
CONNECTION DIAGRAMS – Top Views

P-20, D-20



Leadless Chip Carrier L-20-1



F-20 pin configuration identical to D-20, P-20.

Note: Pin 1 is marked for orientation.

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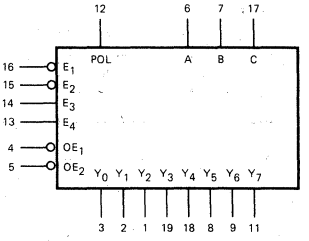
LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75V MAX. = 5.25V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50V MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = 1.0mA (MIL)		2.4	3.4		Volts
			I_{OH} = −2.6mA (COM'L)		2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 4.0mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
			I_{OL} = 12mA				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V					−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V					20	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V					0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	V_O = 0.4V				−20	μA
			V_O = 2.4V				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				21	34	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: A = B = C = $\overline{E}_1 = \overline{E}_2$ = GND : $E_3 = E_4$ = POL = $\overline{OE}_1 = \overline{OE}_2$ = 4.5V.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

Am2921
SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

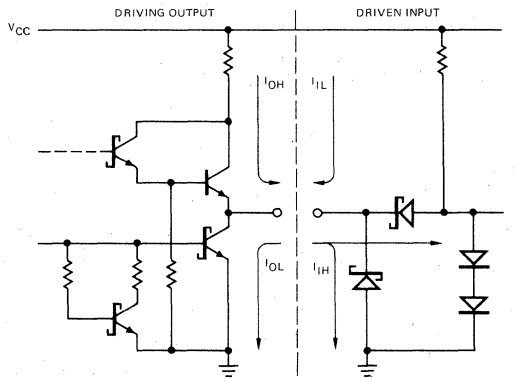
Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	A, B, C to Y_i		20	30	ns	C_L = 15pF R_L = 2.0kΩ
t_{PHL}			15	22		
t_{PLH}	$\overline{E_1}$, $\overline{E_2}$ to Y_i		19	28	ns	
t_{PHL}			20	30		
t_{PLH}	E_3, E_4 to Y_i		21	31	ns	
t_{PHL}			23	34		
t_{PLH}	POL to Y_i		16	24	ns	
t_{PHL}			20	30		
t_{ZH}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i		17	25	ns	
t_{ZL}			14	21		
t_{HZ}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i		17	25	ns	C_L = 5.0pF R_L = 2.0kΩ
t_{LZ}			20	30		

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am2921PC, DC T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% Min.	Max.	Am2921DM, FM T_A = –55°C to +125°C V_{CC} = 5.0V ± 10% Min.	Max.	Units	Test Conditions
t_{PLH}	A, B, C to Y_i		36		42	ns	C_L = 50pF R_L = 2.0kΩ
t_{PHL}			29		37		
t_{PLH}	$\overline{E_1}$, $\overline{E_2}$ to Y_i		34		39	ns	
t_{PHL}			38		45		
t_{PLH}	E_3, E_4 to Y_i		38		45	ns	
t_{PHL}			43		52		
t_{PLH}	POL to Y_i		29		34	ns	
t_{PHL}			39		49		
t_{ZH}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i		38		45	ns	
t_{ZL}			23		25		
t_{HZ}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i		29		33	ns	C_L = 5.0pF R_L = 2.0kΩ
t_{LZ}			33		36		

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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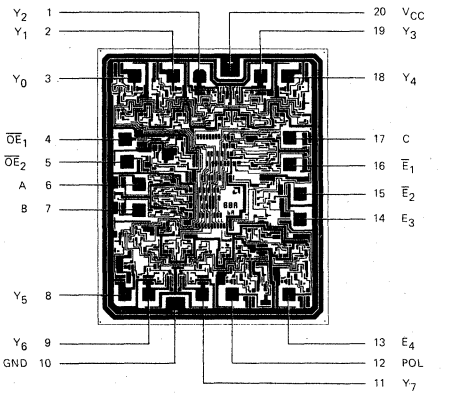
Metallization and Pad Layout



DIE SIZE 0.081" X 0.096"

DEFINITION OF FUNCTIONAL TERMS

A, B, C, D — The three select inputs to the decoder/demultiplexer.

$\overline{E}_1$, $\overline{E}_2$ — The active LOW enable inputs. A HIGH on either the $\overline{E}_1$ or $\overline{E}_2$ input forces all decoded functions to be disabled.

E_3, E_4 — The active HIGH enable inputs. A LOW on either E_3 or E_4 inputs forces all the decoded functions to be inhibited.

POL — Polarity Control. A LOW on the polarity control input forces the output to the active-HIGH state while a HIGH on the polarity control input forces the Y outputs to the active-LOW state.

$\overline{OE}_1$, $\overline{OE}_2$ — Output Enable. When both the $\overline{OE}_1$ and $\overline{OE}_2$ inputs are LOW, the Y outputs are enabled. If either $\overline{OE}_1$ or $\overline{OE}_2$ input is HIGH, the Y outputs are in the high impedance state.

Y_i — The eight outputs for the decoder/demultiplexer.

GUARANTEED LOADING RULES OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

Pin No.'s	Input/Output	Input Load	Output HIGH MIL	Output HIGH COM'L	Output LOW MIL	Output LOW COM'L
1	Y_2	–	50	130	33	33
2	Y_1	–	50	130	33	33
3	Y_0	–	50	130	33	33
4	$\overline{OE}_1$	1.0	–	–	–	–
5	$\overline{OE}_2$	1.0	–	–	–	–
6	A	1.0	–	–	–	–
7	B	1.0	–	–	–	–
8	Y_5	–	50	130	33	33
9	Y_6	–	50	130	33	33
10	GND	–	–	–	–	–
11	Y_7	–	50	130	33	33
12	POL	1.0	–	–	–	–
13	E_4	1.0	–	–	–	–
14	E_3	1.0	–	–	–	–
15	$\overline{E}_2$	1.0	–	–	–	–
16	$\overline{E}_1$	1.0	–	–	–	–
17	C	1.0	–	–	–	–
18	Y_4	–	50	130	33	33
19	Y_3	–	50	130	33	33
20	V_{CC}	–	–	–	–	–

FUNCTION TABLE

FUNCTION	INPUTS										OUTPUTS							
	$\overline{OE}_1$	$\overline{OE}_2$	$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	POL	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
High Impedance	H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
	X	H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
Disable	L	L	H	X	X	X	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	H	X	X	X	H	X	X	X	H	H	H	H	H	H	H	H
	L	L	X	H	X	X	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	X	H	X	X	H	X	X	X	H	H	H	H	H	H	H	H
	L	L	X	X	L	X	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	X	X	L	X	H	X	X	X	H	H	H	H	H	H	H	H
	L	L	X	X	X	L	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	X	X	X	L	H	X	X	X	H	H	H	H	H	H	H	H
Active-HIGH Output	L	L	L	L	H	H	L	L	L	L	H	L	L	L	L	L	L	L
	L	L	L	L	H	H	L	L	L	H	L	H	L	L	L	L	L	L
	L	L	L	L	H	H	L	L	H	L	L	L	H	L	L	L	L	L
	L	L	L	L	H	H	L	L	H	H	L	L	L	H	L	L	L	L
	L	L	L	L	H	H	L	H	L	L	L	L	L	L	H	L	L	L
	L	L	L	L	H	H	L	H	L	H	L	L	L	L	L	H	L	L
	L	L	L	L	H	H	L	H	H	L	L	L	L	L	L	L	H	L
	L	L	L	L	H	H	L	H	H	H	L	L	L	L	L	L	L	H
Active-LOW Output	L	L	L	L	H	H	H	L	L	L	L	H	H	H	H	H	H	H
	L	L	L	L	H	H	H	L	L	H	H	L	H	H	H	H	H	H
	L	L	L	L	H	H	H	L	H	L	H	H	L	H	H	H	H	H
	L	L	L	L	H	H	H	L	H	H	H	H	H	L	H	H	H	H
	L	L	L	L	H	H	H	H	L	L	H	H	H	H	L	H	H	H
	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	L	H	H
	L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	L	H
	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH L = LOW X = Don't Care Z = High Impedance

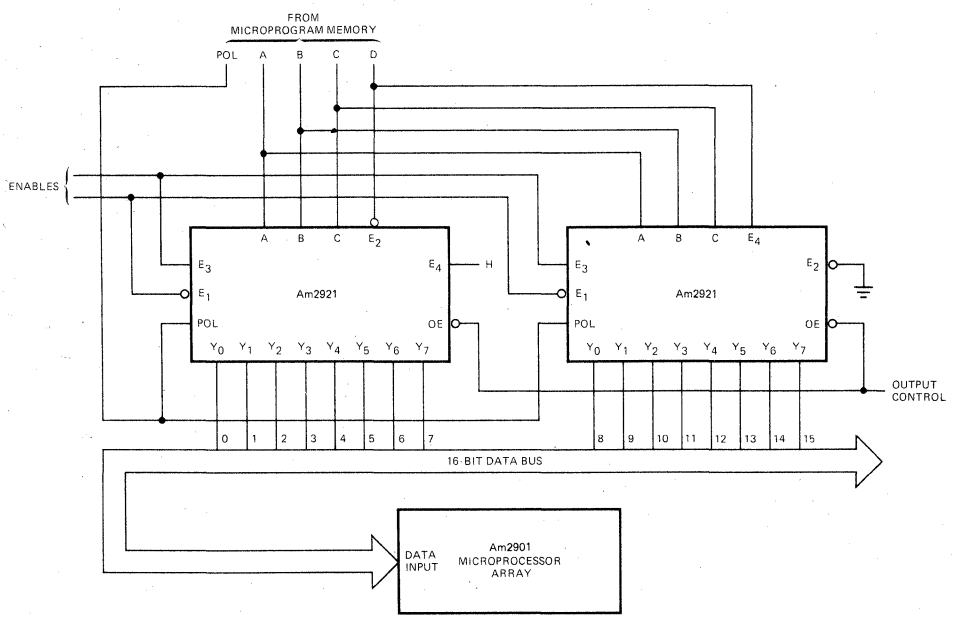
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2921PC	P-20	C	C-1
AM2921DC	D-20	C	C-1
AM2921DC-B	D-20	C	B-1
AM2921DM	D-20	M	C-3
AM2921DM-B	D-20	M	B-3
AM2921FM	F-20	M	C-3
AM2921FM-B	F-20	M	B-3
AM2921LC	L-20-1	C	C-1
AM2921LC-B	L-20-1	C	B-1
AM2921LM	L-20-1	M	C-3
AM2921LM-B	L-20-1	M	B-3
AM2921XC	Dice	C	Visual inspection to MIL-STD-883, Method 2010B.
AM2921XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Flat-Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

APPLICATIONS



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Two Am2921's can be used to perform a bit set, bit clear, bit toggle or bit test on any of sixteen bits in a microprocessor system. Examples of the operations performed are as follows:

Microprogram Control					16-Bit Field From Am2921															Am2901 ALU Function	Bit Function Performed On Selected Register
D	C	B	A	POL	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	OR	BIT SET
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	AND	BIT TEST
0	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	AND	BIT CLEAR
1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	EX NOR	BIT TOGGLE
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	EX OR	BIT TOGGLE

Note: Bit test is performed using F = 0 output of Am2901A.

Am2922

Eight Input Multiplexer with Control Register

DISTINCTIVE CHARACTERISTICS

- High speed eight-input multiplexer
- On-chip Multiplexer Select and Polarity Control Register
- Output polarity control for inverting or non-inverting output
- Common register enable
- Asynchronous register clear
- Three-state output for expansion
- AC parameters specified over operating temperature and power supply ranges.

RELATED PRODUCTS

Part No.	Description
Am25LS2535	8-Input Multiplexer
Am2923	8-Input Multiplexer

FUNCTIONAL DESCRIPTION

The Am2922 is an eight-input Multiplexer with Control Register. The device features high speed from clock to output and is intended for use in high speed computer control units or structured state machine designs.

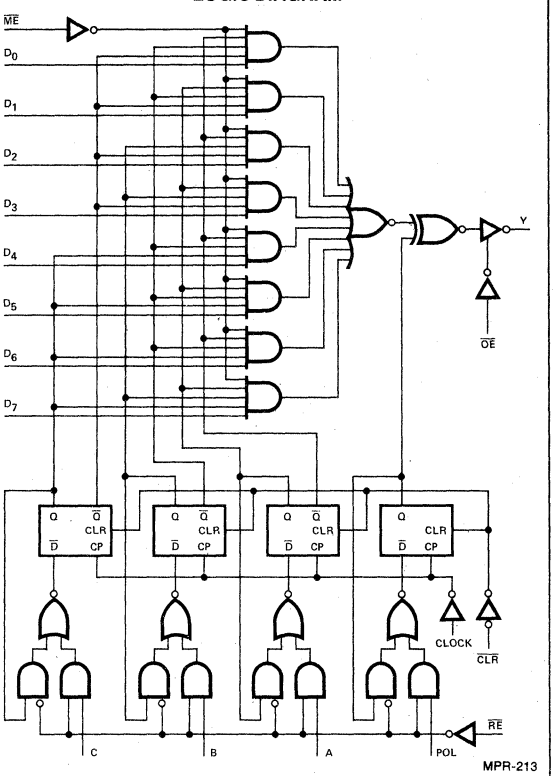
The Am2922 contains an internal register which holds the A, B and C multiplexer select lines as well as the POL (Polarity) control bit. When the Register Enable input ($\overline{RE}$) is LOW, new data is entered into the register on the LOW-to-HIGH, transition of the clock. When $\overline{RE}$ is HIGH, the register retains its current data. An asynchronous clear input ($\overline{CLR}$) is used to reset the register to a logic LOW level.

The A, B and C register outputs select one of eight multiplexer data inputs. A HIGH on the Polarity Control flip-flop output causes a true (non-inverting) multiplexer output, and a LOW causes the output to be inverted. In a computer control unit, this allows testing of either true or complemented flag data at the microprogram sequencer test input.

An active LOW Multiplexer Enable input ($\overline{ME}$) allows the selected multiplexer input to be passed to the output. When $\overline{ME}$ is HIGH, the output is determined only by the Polarity Control bit.

The Am2922 also features a three-state Output Enable control ($\overline{OE}$) for expansion. When $\overline{OE}$ is LOW, the output is enabled. When $\overline{OE}$ is HIGH, the output is in the high impedance state.

LOGIC DIAGRAM



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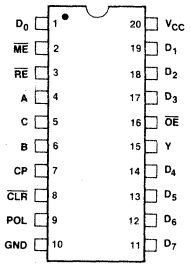
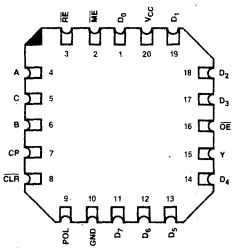
CONNECTION DIAGRAMS – Top Views

D-20, P-20



Leadless Chip Carrier L-20-1

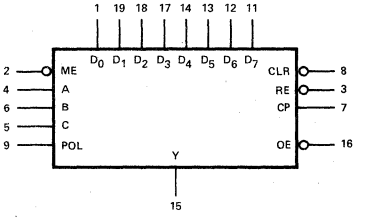


F-20 pin configuration identical to D-20, P-20.

Note: Pin 1 is marked for orientation.

MPR-212

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

MPR-214

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	MIL, $I_{OH} = -2.0mA$		2.4	3.4		Volts
			COM'L, $I_{OH} = -6.5mA$		2.4	3.2		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$				0.4	Volts
			$I_{OL} = 8.0mA$				0.45	
			$I_{OL} = 20mA$				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$	$\overline{ME}$, $\overline{OE}$, $\overline{RE}$				−0.72	mA
			D_N, A, B, C, POL, CP, $\overline{CLR}$				−2.0	
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$	$\overline{ME}$, $\overline{OE}$, $\overline{RE}$				40	μA
			D_N, A, B, C, POL, CP, $\overline{CLR}$				50	
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 5.5V$	$\overline{ME}$, $\overline{OE}$, $\overline{RE}$				0.1	mA
			D_N, A, B, C, POL, CP, $\overline{CLR}$				1.0	
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$				−50	μA
			$V_O = 2.4V$				50	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−40		−100	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				97	148	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. D_N, A, B, C, POL, $\overline{ME}$ at Gnd. All other inputs and outputs open. Measured after a momentary ground then 4.5V applied to clock input.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to $+V_{CC}$ max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0 V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Y POL – LOW		21	32	ns	C_L = 15pF R_L = 2.0kΩ
t_{PHL}			19	29		
t_{PLH}	Clock to Y POL – HIGH		16	24	ns	
t_{PHL}			19	29		
t_{PLH}	D_n to Y		10	16	ns	
t_{PHL}			13	19		
t_{PLH}	CLR to Y		22	33	ns	
t_{PHL}			22	33		
t_{PLH}	$\overline{ME}$ to Y		12	18	ns	
t_{PHL}			12	18		
t_{ZL}	$\overline{OE}$ to Y		8	14	ns	
t_{ZH}			8	14		
t_{LZ}			10	17	ns	C_L = 5.0pF R_L = 2.0kΩ
t_{HZ}			10	17		
t_S	A, B, C, POL	10			ns	C_L = 15pF R_L = 2.0kΩ
	CE	15				
t_S	CLR Recovery	5			ns	
t_{pw}	Clock	10			ns	
	Clear (LOW)	10				
t_h	A, B, C, POL, CE	0			ns	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am2922PC, DC T_A = 0°C to +70°C V_{CC} = 5.0V ±5% Min.	Max.	Am2922DM, FM T_A = −55°C to +125°C V_{CC} = 5.0V ±10% Min.	Max.	Units	Test Conditions
t_{PLH}	Clock to Y, POL-L		40		47	ns	C_L = 50pF R_L = 2.0kΩ
t_{PHL}			34		38		
t_{PLH}	Clock to Y, POL-H		29		33	ns	
t_{PHL}			35		41		
t_{PLH}	D_N to Y		19		21	ns	
t_{PHL}			22		24		
t_{PLH}	CLR to Y		39		45	ns	
t_{PHL}			39		45		
t_{PLH}	$\overline{ME}$ to Y		22		26	ns	
t_{PHL}			19		20		
t_{ZL}	$\overline{OE}$ to Y		19		24	ns	
t_{ZH}			22		29		
t_{LZ}	$\overline{OE}$ to Y		24		30	ns	C_L = 5.0pF R_L = 2.0kΩ
t_{HZ}			24		30		
t_S	A, B, C POL	11		12		ns	C_L = 50pF R_L = 2.0kΩ
	CE	18		20			
t_S	CLR Recovery	6		7		ns	
t_{pw}	Clock	11		12		ns	
	Clear (LOW)	11		12			
t_H	A, B, C, POL, CE	3		3		ns	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

A, B, C Multiplexer Select Lines. One of eight multiplexer data inputs is selected by the A, B and C register outputs.

POL Polarity Control Bit. A HIGH register output causes a true (non-inverted) output and a LOW causes the output to be inverted.

$\overline{ME}$ Multiplexer Enable. When LOW, it enabled the 8-input multiplexer. When HIGH, the Y output is determined by only the Polarity Control bit.

$\overline{RE}$ Register Enable. When LOW, the Multiplexer Select and Polarity Control Register is enabled for loading. When HIGH, the register holds its current data.

$\overline{CLR}$ Clear. A LOW asynchronously resets the Multiplexer Select and Polarity Control Register.

D_1-D_8 Data Inputs to the 8-input multiplexer.

CP Clock Pulse. When $\overline{RE}$ is LOW, the Multiplexer Select and Polarity Control Register changes state on the LOW-to-HIGH transition of CP.

$\overline{OE}$ Output Enable. When LOW, the output is enabled. When HIGH, the output is in the high impedance state.

Y The chip output.

FUNCTION TABLE

MODE	INPUTS							INTERNAL				INPUTS		OUTPUT
	C	B	A	POL	$\overline{RE}$	$\overline{CLR}$	CP	Q_C	Q_B	Q_A	Q_{POL}	$\overline{ME}$	$\overline{OE}$	Y
Clear	X	X	X	X	X	L	X	L	L	L	L	H	L	H
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	L	L	$\overline{D}_0$
												X	H	Z
Reg. Disable	X	X	X	X	H	H	X	NC	NC	NC	NC	L	L	$\overline{D}_i/D_i$ (Note 1)
Select (Multiplex)	L	L	L	L/H	L	H	↑	L	L	L	L/H	L	L	$\overline{D}_0/D_0$
	L	L	H	↓	↓	↓	↓	L	L	H	↓	↓	↓	$\overline{D}_1/D_1$
	L	H	L	↓	↓	↓	↓	L	H	L	↓	↓	↓	$\overline{D}_2/D_2$
	L	H	H	↓	↓	↓	↓	L	H	H	↓	↓	↓	$\overline{D}_3/D_3$
	H	L	L	↓	↓	↓	↓	H	L	L	↓	↓	↓	$\overline{D}_4/D_4$
	H	L	H	↓	↓	↓	↓	H	L	H	↓	↓	↓	$\overline{D}_5/D_5$
	H	H	L	↓	↓	↓	↓	H	H	L	↓	↓	↓	$\overline{D}_6/D_6$
	H	H	H	↓	↓	↓	↓	H	H	H	↓	↓	↓	$\overline{D}_7/D_7$
Multiplexer Disable	X	X	X	X	X	H	X	X	X	X	L	H	L	H
	↓	↓	↓	↓	↓	↓	↓	X	X	X	H	H	L	L
Tri-state Output Disable	↓	↓	↓	↓	↓	↓	↓	X	X	X	X	X	H	Z

NC = No Change
X = Don't Care

Note 1: The output will follow the selected input, D_i, or its complement depending on the state of the POL flip-flop.

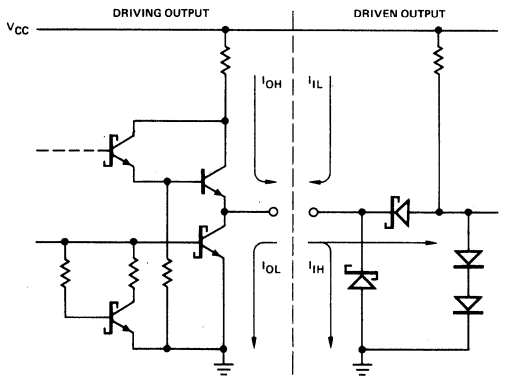
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2922PC	P-20	C	C-1
AM2922DC	D-20	C	C-1
AM2922DC-B	D-20	C	B-1
AM2922DM	D-20	M	C-3
AM2922DM-B	D-20	M	B-3
AM2922FM	F-20	M	C-3
AM2922FM-B	F-20	M	B-3
AM2922LC	L-20-1	C	C-1
AM2922LC-B	L-20-1	C	B-1
AM2922LM	L-20-1	M	C-3
AM2922LM-B	L-20-1	M	B-3
AM2922XC	Dice	C	Visual inspection to MIL-STD-883. Method 2010B.
AM2922XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Flat-Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

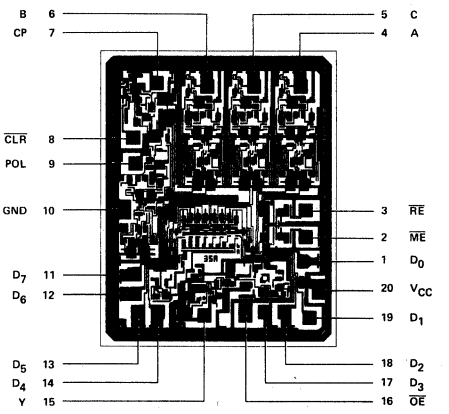
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

MPR-215

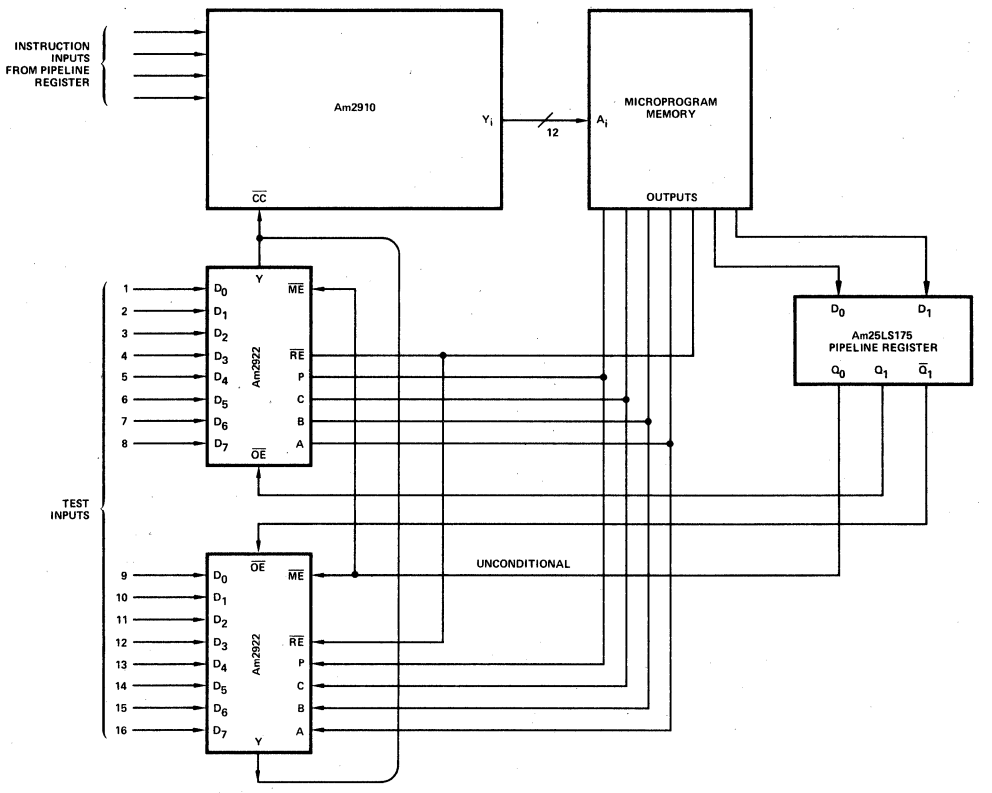
Metallization and Pad Layout



DIE SIZE 0.080" X 0.099"

5

APPLICATION



A versatile one-of-sixteen Test Select with Polarity Control and Test Select Hold.

MPR-216

Am2923

Eight-Input Multiplexer

Distinctive Characteristics

- Advanced Schottky technology
- Switches one of eight inputs to two complementary outputs
- 3-state output for bus organized systems

FUNCTIONAL DESCRIPTION

The Am2923 is an 8-input multiplexer that switches one of eight inputs onto the inverting and non-inverting outputs under the control of a 3-bit select code. The inverting output is one gate delay faster than the non-inverting output.

The Am2923 features a 3-state output for data bus organization. The active-LOW strobe, or "output control" applies to both the inverting and non-inverting output. When the output control is HIGH, the outputs are in the high-impedance state. When the output control is LOW, the active pull-up output is enabled.

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

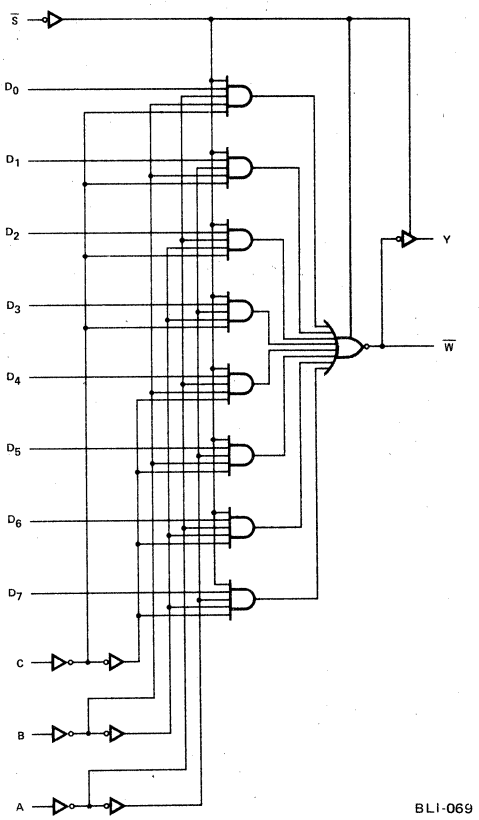
Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2923PC	P-16-1	C	C-1
AM2923DC	D-16-1	C	C-1
AM2923DC-B	D-16-1	C	B-1
AM2923DM	D-16-1	M	C-3
AM2923DM-B	D-16-1	M	B-3
AM2923FM	F-16-1	M	C-3
AM2923FM-B	F-16-1	M	B-3
AM2923LC	L-20-1	C	C-1
AM2923LC-B	L-20-1	C	B-1
AM2923LM	L-20-1	M	C-3
AM2923LM-B	L-20-1	M	B-3
AM2923XC	Dice	C	Visual inspection to MIL-STD-883. Method 2010B.
AM2923XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Flat-Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

RELATED PRODUCTS

Part No.	Description
Am2922	8 Input MUX with Register Control
Am25LS2535	8 Input MUX with Register Control

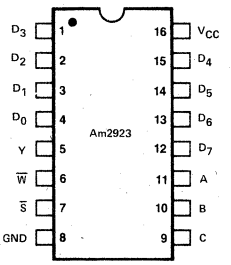
LOGIC DIAGRAM



BLI-069

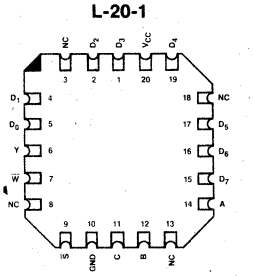
CONNECTION DIAGRAMS – Top Views

D-16, P-16



BLI-070

Leadless Chip Carrier L-20-1



BLI-071

F-16 pin configuration identical to D-16, P-16.

MAXIMUM RATINGS (Above which the useful life may be impaired).

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to + V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Output	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am2923PC, DC, XC T_A =0 to 70°C V_{CC} = 5.0V ±5% (COM'L) MIN = 4.75V MAX = 5.25V
Am2923DM, FM, XM T_A = −55 to +125°C V_{CC} = 5.0V ±10% (MIL) MIN = 4.5V MAX = 5.5V

Parameters	Description		Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	MIL	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −2mA	2.4	3.4		Volts
		COM'L		I_{OH} = −6.5mA	2.4	3.2		
V_{OL}	Output LOW Voltage		V_{CC} = MIN, I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level		Guaranteed input logical HIGH voltage for all inputs		2			Volts
V_{IL}	Input LOW Level		Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage		V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current		V_{CC} = MAX, V_{IN} = 0.5				−2	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current		V_{CC} = MAX, V_{IN} = 2.7				50	μA
I_I	Input HIGH Current		V_{CC} = MAX, V_{IN} = 5.5V				1	mA
I_O(off)	Off-State (High-Impedance) Output Current		V_{CC} = MAX, V_{IN} = V_{IH} or V_{IL}	V_O = 2.4V			50	μA
				V_O = 0.5V			−50	
I_{SC}	Output Short Circuit Current (Note 4)		V_{CC} = MAX, V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current		V_{CC} = MAX (Note 5)			55	85	mA

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (see Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} is measured with all outputs open and all inputs at 4.5V.

SWITCHING CHARACTERISTICS (T_A = 25°C)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	A, B, or C to Y; 4 Levels of Delay	V_{CC} = 5.0V, R_L = 280Ω, C_L = 15pF		12	18	ns
t_{PHL}				13	19.5	
t_{PLH}	A, B, or C to $\overline{W}$; 3 Levels of Delay			10	15	ns
t_{PHL}				9	13.5	
t_{PLH}	Any D to Y			8	12	ns
t_{PHL}				8	12	
t_{PLH}	Any D to $\overline{W}$			4.5	7	ns
t_{PHL}				4.5	7	
t_{ZH}	Output Enable to Y	V_{CC} = 5.0V, R_L = 280Ω, C_L = 15pF		13	19.5	ns
t_{ZL}				14	21	
t_{ZH}	Output Enable to $\overline{W}$			13	19.5	ns
t_{ZL}				14	21	
t_{HZ}	Output Enable to Y	V_{CC} = 5.0V, R_L = 280Ω, C_L = 5pF		5.5	8.5	ns
t_{LZ}				9	14	
t_{HZ}	Output Enable to $\overline{W}$			5.5	8.5	ns
t_{LZ}				9	14	

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FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			Output Control		
C	B	A	$\overline{S}$	Y	$\overline{W}$
X	X	X	H	Z	Z
L	L	L	L	D_0	D_0
L	L	H	L	D_1	D_1
L	H	L	L	D_2	D_2
L	H	H	L	D_3	D_3
H	L	L	L	D_4	D_4
H	L	H	L	D_5	D_5
H	H	L	L	D_6	D_6
H	H	H	L	D_7	D_7

H = HIGH X = Don't Care
L = LOW Z = High Impedance

D_0–D_7 = The output will follow the HIGH-level or LOW-level of the selected input.

$\overline{D}_0$–$\overline{D}_7$ = The output will follow the complement of the HIGH-level or LOW-level of the selected input.

DEFINITION OF FUNCTIONAL TERMS

A, B, C The three select inputs of the multiplexer.

D_0, D_1, D_2, D_3, D_4, D_5, D_6, D_7 The eight data inputs of the multiplexer.

Y The true multiplexer output.

$\overline{W}$ The complement multiplexer output.

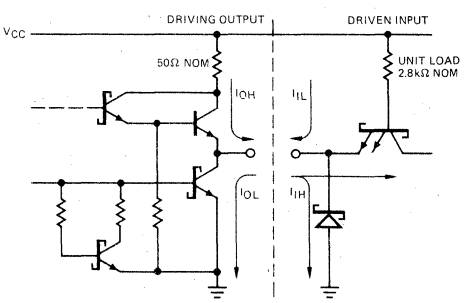
$\overline{S}$ Output Control. HIGH on the output control (or strobe) forces both the $\overline{W}$ and Y outputs to the high-impedance (off) state.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
D_3	1	1	–	–
D_2	2	1	–	–
D_1	3	1	–	–
D_0	4	1	–	–
Y	5	–	20	10
$\overline{W}$	6	–	20	10
$\overline{S}$	7	1	–	–
GND	8	–	–	–
C	9	1	–	–
B	10	1	–	–
A	11	1	–	–
D_7	12	1	–	–
D_6	13	1	–	–
D_5	14	1	–	–
D_4	15	1	–	–
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and –2.0mA measured at 0.5V LOW.

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



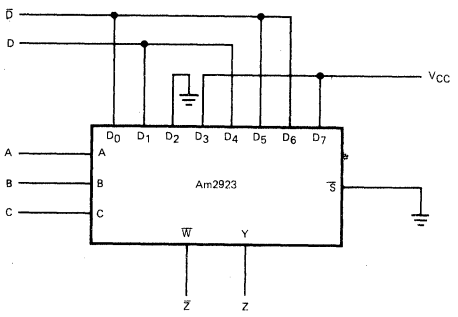
Note: Actual current flow direction shown.

BLI-072

Am2923

APPLICATIONS

LOGIC FUNCTION GENERATION



$Z = ABCD + \overline{A}BCD + A\overline{C}D + AB + \overline{A}CD + \overline{B}CD$

BLI-073

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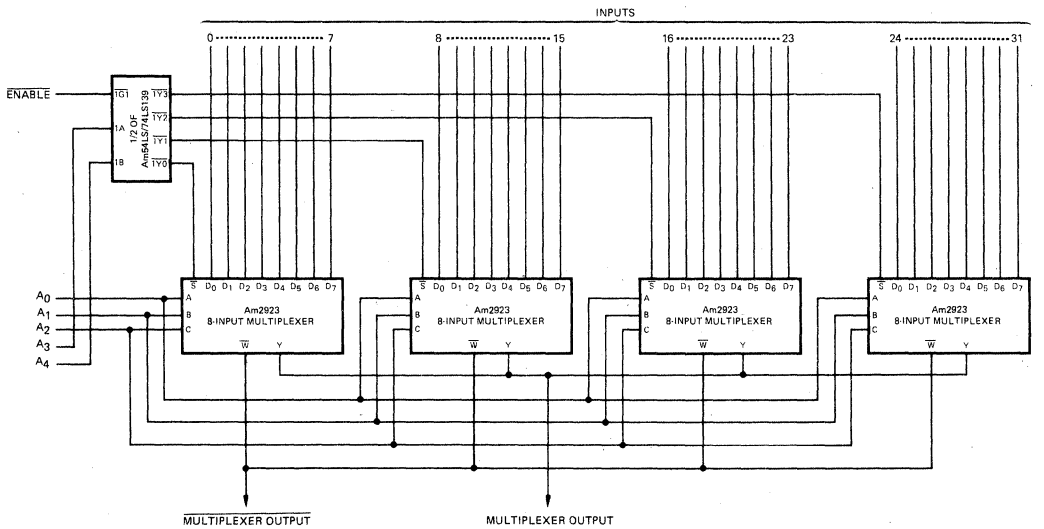
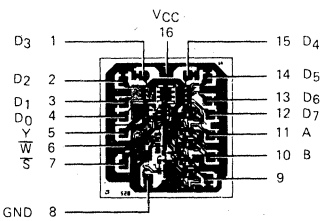
32-INPUT MULTIPLEXER



METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.064" X 0.067"

BLI-074

Am2924

Three-Line to Eight-Line Decoder/Demultiplexer

Distinctive Characteristics

- Advanced Schottky technology
- Inverting and non-inverting enable inputs

FUNCTIONAL DESCRIPTION

The Am2924 is a 3-line to 8-line decoder/demultiplexer fabricated using advanced Schottky technology. The decoder has three buffered select inputs A, B and C that are decoded to one of eight $\overline{Y}$ outputs.

One active-HIGH and two active-LOW enables can be used for gating the decoder or can be used with incoming data for demultiplexing applications. When the enable input function is in the disable state, all eight $\overline{Y}$ outputs are HIGH regardless of the A, B and C select inputs.

RELATED PRODUCTS

Part No.	Description
Am25LS2536	8-Bit Decoder
Am25LS2537	1 of 10 Decoder
Am25LS2538	1 of 8 Decoder
Am25LS2539	Dual 1 of 4 Decoder
Am25LS2548	Chip Select Address Decoder
Am2921	1 of 8 Decoder

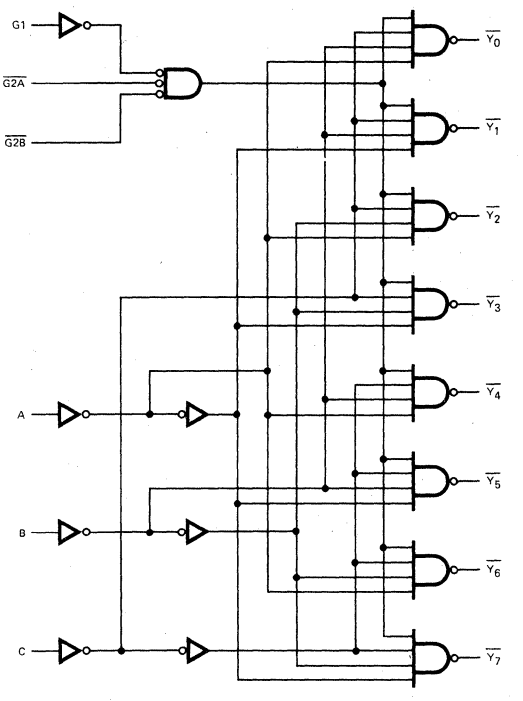
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2924PC	P-16-1	C	C-1
AM2924DC	D-16-1	C	C-1
AM2924DC-B	D-16-1	C	B-1
AM2924DM	D-16-1	M	C-3
AM2924DM-B	D-16-1	M	B-3
AM2924FM	F-16-1	M	C-3
AM2924FM-B	F-16-1	M	B-3
AM2924LC	L-20-1	C	C-1
AM2924LC-B	L-20-1	C	B-1
AM2924LM	L-20-1	M	C-3
AM2924LM-B	L-20-1	M	B-3
AM2924XC	Dice	C	Visual inspection to MIL-STD-883. Method 2010B.
AM2924XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Flat-Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

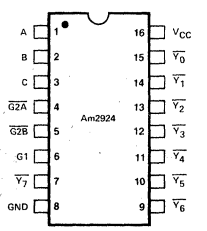
LOGIC DIAGRAM



BLI-075

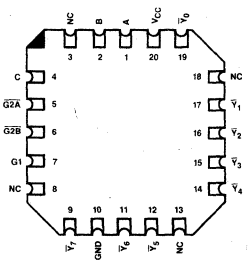
CONNECTION DIAGRAMS – Top Views

D-16, P-16



BLI-076

Leadless Chip Carrier L-20-1



F-16 pin configuration identical to D-16, P-16.

Note: Pin 1 is marked for orientation.

BLI-077

Am2924

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +Vcc max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am2924PC, DC, XC $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (COM'L) MIN. = 4.75V MAX. = 5.25V
Am2924DM, FM, XM $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIL) MIN. = 4.5V MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1mA V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V				−2	mA
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)			49	74	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Outputs enabled and open.

Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Two Level Delay Select to Output	V_{CC} = 5V, C_L = 15pF, R_L = 280Ω		4.5	7	ns
t_{PHL}				7	10.5	
t_{PLH}	Three Level Delay Select to Output			7.5	12	ns
t_{PHL}				8	12	
t_{PLH}	$\overline{G2A}$ or $\overline{G2B}$ to Output			5	8	ns
t_{PHL}				7	11	
t_{PLH}	G1 to Output			7	11	ns
t_{PHL}				7	11	

FUNCTION TABLE

Inputs						Outputs							
Enable			Select										
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	$\overline{Y_0}$	$\overline{Y_1}$	$\overline{Y_2}$	$\overline{Y_3}$	$\overline{Y_4}$	$\overline{Y_5}$	$\overline{Y_6}$	$\overline{Y_7}$
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = HIGH
L = LOW
X = Don't care

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Unit Load	Fan-out Output HIGH	Fan-out Output LOW
A	1	1	–	–
B	2	1	–	–
C	3	1	–	–
$\overline{G2A}$	4	1	–	–
$\overline{G2B}$	5	1	–	–
G1	6	1	–	–
$\overline{Y_7}$	7	–	20	10
GND	8	–	–	–
$\overline{Y_6}$	9	–	20	10
$\overline{Y_5}$	10	–	20	10
$\overline{Y_4}$	11	–	20	10
$\overline{Y_3}$	12	–	20	10
$\overline{Y_2}$	13	–	20	10
$\overline{Y_1}$	14	–	20	10
$\overline{Y_0}$	15	–	20	10
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

DEFINITION OF FUNCTIONAL TERMS:

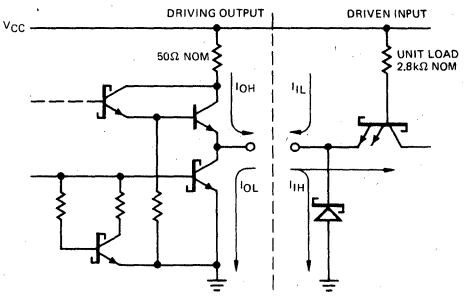
A, B, C Select. The three select inputs to the decoder.

G1 The active-HIGH enable input. A LOW on the G1 input forces all $\overline{Y}$ outputs HIGH regardless of any other inputs.

$\overline{G2A}$, $\overline{G2B}$ The active-LOW enable input. A HIGH on either the $\overline{G2A}$ or $\overline{G2B}$ input forces all $\overline{Y}$ outputs HIGH regardless of any other inputs.

$\overline{Y_0}$, $\overline{Y_1}$, $\overline{Y_2}$, $\overline{Y_3}$, $\overline{Y_4}$, $\overline{Y_5}$, $\overline{Y_6}$, $\overline{Y_7}$ The eight decoder outputs.

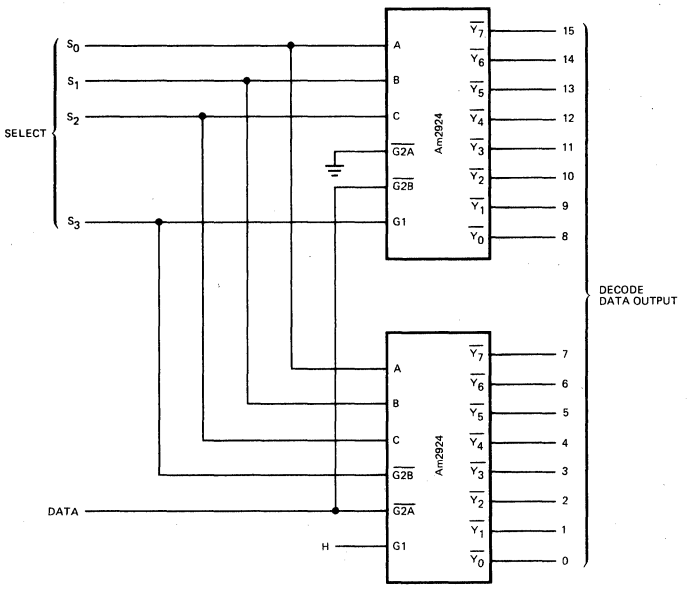
SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

BLI-078

APPLICATION

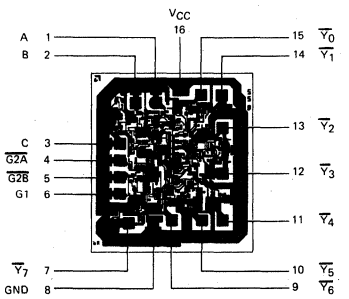


H=HIGH

One-of-Sixteen Demultiplexer

BLI-079

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.065" X 0.070"

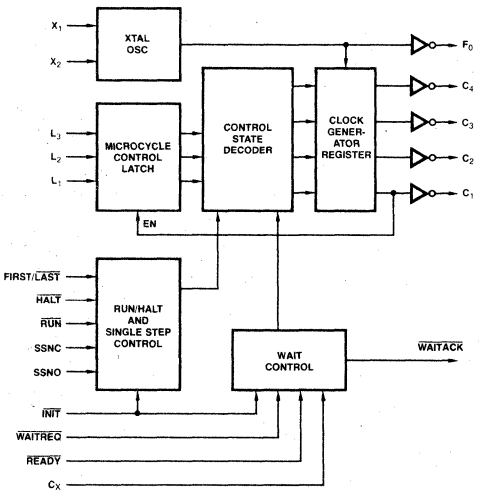
Am2925

Clock Generator and Microcycle Length Controller

DISTINCTIVE CHARACTERISTICS

- **Crystal controlled oscillator**
  Stable operation from 1MHz to over 31MHz
- **Four microcode controlled clock outputs**
  Allows clock cycle length control for 15–30% increase in system throughput. Microcode selects one of eight clock patterns from 3 to 10 oscillator cycles in length
- **System controls for Run/Halt and Single Step**
  Switch debounced inputs provide flexible halt controls
- **Slim 0.3" 24-pin package**
  LSI complexity in minimum board area

BLOCK DIAGRAM



ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2925DC	D-24-Slim	C	C-1
AM2925DC-B	D-24-Slim	C	B-1
AM2925DM	D-24-Slim	M	C-3
AM2925DM-B	D-24-Slim	M	B-3
AM2925LC	L-28-1	C	C-1
AM2925LC-B	L-28-1	C	C-3
AM2925LM	L-28-1	M	B-1
AM2925LM-B	L-28-1	M	B-3
AM2925XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2925XM	Dice	M	

Notes: 1. D = Hermetic DIP. Number following letter is number of leads.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

FUNCTIONAL DESCRIPTION

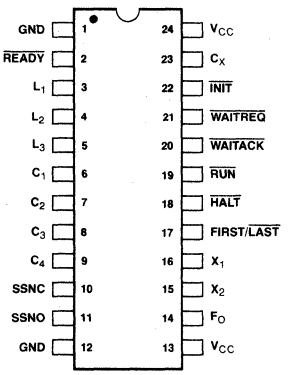
The Am2925 is a single-chip general purpose clock generator/driver. It is crystal controlled, and has microprogrammable clock cycle length to provide significant speed-up over fixed clock cycle approaches and meet a variety of system speed requirements. The Am2925 generates four different simultaneous clock output waveforms tailored to meet the needs of Am2900 and other bipolar and MOS microprocessor based systems. One-of-eight cycle lengths may be generated under microprogram control using the Cycle Length inputs L_1, L_2, and L_3.

The Am2925 oscillator runs at frequencies to over 31MHz. A buffered oscillator output, F_0, is provided for external system timing in addition to the four microcode controlled clock outputs C_1, C_2, C_3 and C_4.

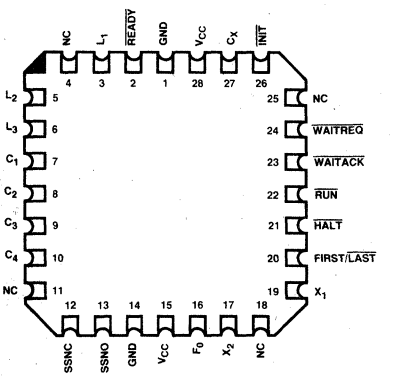
System control functions include Run, Halt, Single-Step, Initialize and Ready/Wait controls. In addition, the FIRST/LAST input determines where a halt occurs and the C_X input determines the end point timing of wait cycles. WAITACK indicates that the Am2925 is in a wait state.

CONNECTION DIAGRAMS – Top Views

D-24-Slim

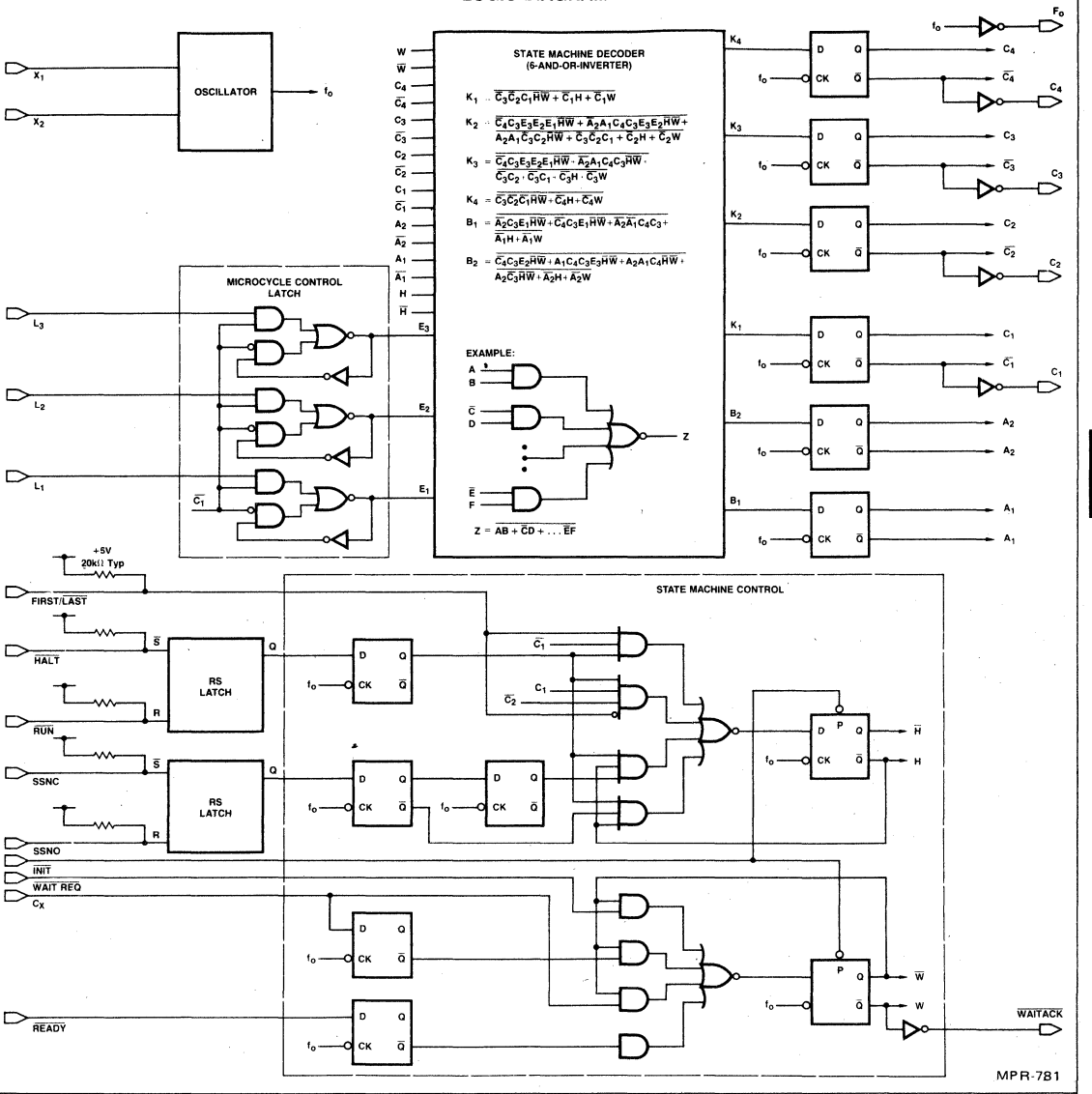


Leadless Chip Carrier
L-28-1



Note: Pin 1 is marked for orientation.

LOGIC DIAGRAM



DEFINITION OF FUNCTIONAL TERMS

C_1, C_2, C_3, C_4 System clock outputs. These outputs are all active during every system clock cycle. Their timing is determined by clock cycle length controls, L_1, L_2 and L_3.

L_1, L_2, L_3 Clock cycle length control inputs. These inputs receive the microcode bits that select the microcycle lengths. They form a control word which selects one of the eight microcycle waveform patterns F_3 through F_{10}.

F_0 The buffered oscillator output. F_0 internally generates all of the timing edges for outputs C_1, C_2, C_3, C_4 and $\overline{WAITACK}$. F_0 rises just prior to all of the C_1, C_2, C_3, C_4 transitions.

$\overline{HALT}$ and $\overline{RUN}$ Debounced inputs to provide $\overline{HALT}$ control. These inputs determine whether the output clocks run or not. A LOW input on $\overline{HALT}$ ($\overline{RUN}$ = HIGH) will stop all clock outputs.

FIRST/$\overline{LAST}$ $\overline{HALT}$ time control input. A HIGH input in conjunction with a $\overline{HALT}$ command will cause a halt to occur when C_4 = LOW and $C_1 = C_2 = C_3$ = HIGH (see clock waveforms). A LOW input causes a $\overline{HALT}$ to occur when $C_1 = C_2 = C_3$ = LOW and C_4 = HIGH.

SSNO and SSNC Single Step control inputs. These debounced inputs allow system clock cycle single stepping while $\overline{HALT}$ is activated LOW.

DEFINITION OF FUNCTIONAL TERMS (Cont.)

$\overline{\text{WAITREQ}}$ The Wait Request active LOW input. When LOW this input will cause the outputs to halt during the next oscillator cycle before the C_X input goes LOW.

C_X Wait cycle control input. The clock outputs respond to a wait request one oscillator clock cycle after C_X goes LOW. C_X is normally tied to any one of C_1, C_2, C_3 or C_4.

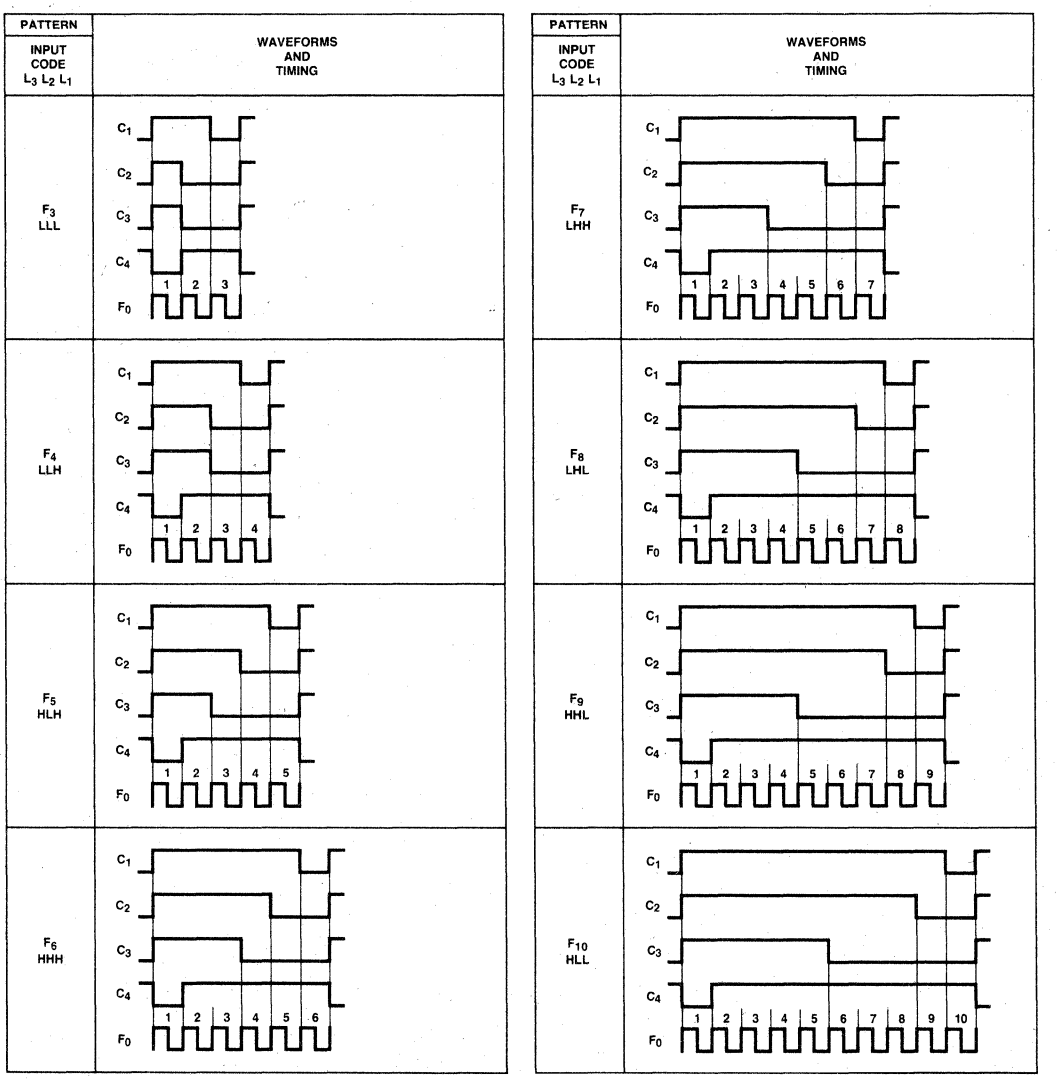
$\overline{\text{WAITACK}}$ The Wait Acknowledge active LOW output. When LOW, this output indicates that all clock outputs are in the "WAIT" state.

$\overline{\text{READY}}$ The $\overline{\text{READY}}$ active LOW input is used to continue normal clock output patterns after a wait stage.

$\overline{\text{INIT}}$ The Initialize active LOW input. This input is intended for use during power up initialization of the system. When LOW all clock outputs free run regardless of the state of the Halt, Single Step, Wait Request and Ready inputs.

X_1, X_2 External crystal connections. X_1 can also be driven by a TTL frequency source.

Am2925 CLOCK WAVEFORMS



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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0 to 70°C V_{CC} = 5.0V ±5% (MIN = 4.75V MAX = 5.25V)
MIL T_C = −55 to 125°C V_{CC} = 5.0V ±10% (MIN = 4.50V MAX = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.0mA		2.5			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	$\overline{WAITACK}$, C_i	I_{OL} = 4.0mA			0.4	Volts
				I_{OL} = 8.0mA			0.45	
				I_{OL} = 12mA			0.5	
			F_0	I_{OL} = 16mA			0.5	Volts
V_{IH}	Input HIGH Level (Note 3)	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW level (Note 3)	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage (Note 3)	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	$\overline{READY}$, $\overline{INIT}$, L_1, L_2, L_3				−0.4	mA
			$\overline{WAITREQ}$, X_1 (See Figure 1)				−0.8	mA
			SSNO, SSNC, $\overline{RUN}$, $\overline{HALT}$				−1.0	mA
			C_X				−1.2	mA
			FIRST/$\overline{LAST}$				−1.5	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	$\overline{READY}$, $\overline{INIT}$, L_1, L_2, L_3				20	μA
			$\overline{WAITREQ}$				50	μA
			SSNO, SSNC, $\overline{RUN}$, $\overline{HALT}$				−500	μA
			C_X				70	μA
			FIRST/$\overline{LAST}$				−750	μA
			X_1 (See Figure 1)				500	μA
I_I	Input HIGH Current	V_{CC} = MAX	V_{IN} = 5.5V	$\overline{READY}$, $\overline{INIT}$, L_1, L_2, L_3			100	μA
			V_{IN} = V_{CC}	SSNO, SSNC, $\overline{RUN}$, $\overline{HALT}$			100	μA
			V_{IN} = 5.5V	$\overline{WAITREQ}$, C_X			1.0	mA
			V_{IN} = V_{CC}	FIRST/$\overline{LAST}$			1.0	mA
			V_{IN} = 4.0V	X_1 (See Figure 1)			1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX			−30		−85	mA
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX				85	120	mA

Notes:
1. For conditions shown as MIN or MAX use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Does not apply to X_1 and X_2.
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} varies with temperature and oscillation frequency as shown in Figure 2. The parameters specified (worst case) applies to f_0 = 0, +25°C, C_1 = C_2 = C_3 = LOW, C_4 = HIGH, X_1 = 2.4V, X_2 = open and F_0 = LOW. The variations shown in Figure 2 apply to typical values.

MAXIMUM RATINGS (Above which the useful life may be impaired)

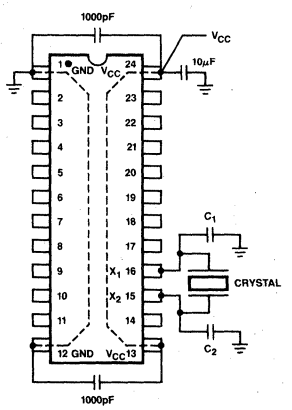
Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

	Parameters	Description	Min	Typ	Max	Units	Test Conditions
1	f_{MAX1}	F_0 Frequency (C_X Connected) (Note 6)	31			MHz	C_L = 15pF, R_L = 280Ω
2	f_{MAX2}	F_0 Frequency (C_X = HIGH)		42			
3	t_{OFFSET}	F_0 (↓) to C_1, C_2, C_3, C_4 or $\overline{WAITACK}$ (↓)	0	5.0	7.5	ns	
4	t_{OFFSET}	F_0 (↓) to C_1, C_2, C_3, C_4 or $\overline{WAITACK}$ (↑)	3	11.5	16	ns	
5	t_{SKEW}	C_1 (↓) to C_2 (↓)	0	0.5	2	ns	
6	t_{SKEW}	C_1 (↓) to C_3 (↓)	0	0.5	2	ns	
7	t_{SKEW}	C_1 (↓) to C_4 (↑) Opposite Transition	4	7	10	ns	
8	t_S	L_1, L_2, L_3 to C_1 (↓)	5			ns	
9	t_H	L_1, L_2, L_3 to C_1 (↓)	9			ns	
10	t_S	C_X to F_0 (↓) (Note 7)	20	17		ns	
11	t_H	C_X to F_0 (↓) (Note 7)	0	−10		ns	C_L = 50pF, R_L = 2.0kΩ
12	t_S	$\overline{WAITREQ}$ to F_0 (↓) (Note 8)	20	17		ns	
13	t_H	$\overline{WAITREQ}$ to F_0 (↓) (Note 8)	0	−10		ns	
14	t_S	$\overline{READY}$ to F_0 (↓) (Note 8)	20	17		ns	
15	t_H	$\overline{READY}$ to F_0 (↓) (Note 8)	0	−10		ns	
16	t_S	$\overline{RUN}$, $\overline{HALT}$ (↑) to F_0 (↓) (Notes 8, 9)	20	14		ns	
17	t_S	SSNC, SSNO to F_0 (↓) (Notes 8, 9)	20	14		ns	
18	t_S	FIRST/$\overline{LAST}$ to F_0 (↓) (Note 10)	25	17		ns	
19	t_S	$\overline{INIT}$ (↑) to F_0 (↓) (Note 8)	30			ns	
20	t_{PWL}	$\overline{INIT}$ LOW Pulse Width	15	10		ns	
21	t_{PLH}	$\overline{INIT}$ to $\overline{WAITACK}$		16	23	ns	
22	t_{PLH}	Propagation Delay (Note 11) X_1 to F_0		13	16	ns	C_L = 15pF, R_L = 280Ω
23	t_{PHL}			14	17	ns	

TYPICAL EXTERNAL CONNECTIONS



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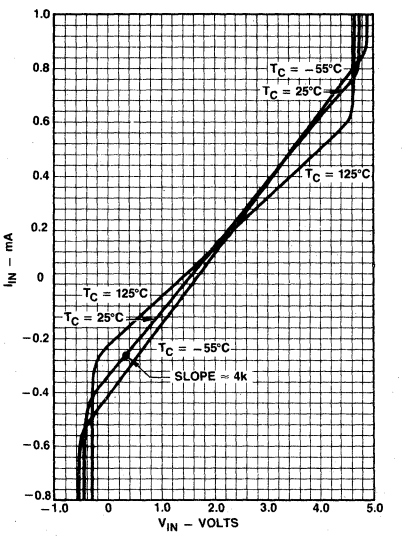
DESIGN CONSIDERATIONS

1. Oscillator external connections should be less than 1" long – wirewrap is not recommended.
2. V_{CC} and GND connections should be less than ½" long to power plane.
3. Supply decoupling includes both high frequency and bulk storage elements.
4. The same considerations apply for 3rd overtone configurations.



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X_1 is not a TTL input. It is a crystal connection to an inverting linear oscillator amplifier, and is specified primarily for test convenience.

Figure 1. Am2925 X_1 Input Characteristics (Typical, V_{CC} = 5.0V)

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

	Parameters	Description	Am2925 COM'L T_A = 0 to +70°C V_{CC} = 5.0V ±5% Min	Am2925 COM'L Max	Am2925 MIL T_C = −55 to +125°C V_{CC} = 5.0V ±10% Min	Am2925 MIL Max	Units	Test Conditions
1	f_{MAX1}	F_0 Frequency (C_X Connected) (Note 6)	31		31		MHz	C_L = 15pF R_L = 280Ω
2	f_{MAX2}	F_0 Frequency (C_X = HIGH)						
3	t_{OFFSET}	F_0 (↓) to C_1, C_2, C_3, C_4 or $\overline{WAITACK}$ (↓)		8.5		8.5	ns	
4	t_{OFFSET}	F_0 (↓) to C_1, C_2, C_3, C_4 or $\overline{WAITACK}$ (↑)		17.0		18.0	ns	
5	t_{SKEW}	C_1 (↓) to C_2 (↓)		2		2	ns	
6	t_{SKEW}	C_1 (↓) to C_3 (↓)		2		2	ns	
7	t_{SKEW}	C_1 (↓) to C_4 (↑) Opposite Transition		11		11	ns	
8	t_S	L_1, L_2, L_3 to C_1 (↓)	6		7		ns	
9	t_H	L_1, L_2, L_3 to C_1 (↓)	11		11		ns	
10	t_S	C_X to F_0 (↓) (Note 7)	25		25		ns	
11	t_H	C_X to F_0 (↓) (Note 7)	0		0		ns	C_L = 50pF R_L = 2.0kΩ
12	t_S	$\overline{WAITREQ}$ to F_0 (↓) (Note 8)	25		25		ns	
13	t_H	$\overline{WAITREQ}$ to F_0 (↓) (Note 8)	0		0		ns	
14	t_S	$\overline{READY}$ to F_0 (↓) (Note 8)	25		25		ns	
15	t_H	$\overline{READY}$ to F_0 (↓) (Note 8)	0		0		ns	
16	t_S	$\overline{RUN}$, $\overline{HALT}$ (↑) to F_0 (↓) (Notes 8,9)	25		25		ns	
17	t_S	SSNC, SSNO to F_0 (↓) (Notes 8, 9)	25		25		ns	
18	t_S	FIRST/$\overline{LAST}$ to F_0 (↓) (Note 10)	30		35		ns	
19	t_S	$\overline{INIT}$ (↑) to F_0 (↓) (Note 8)	33		35		ns	
20	t_{PWL}	$\overline{INIT}$ LOW Pause Width	20		25		ns	
21	t_{PLH}	$\overline{INIT}$ to $\overline{WAITACK}$		25		27	ns	
22	t_{PLH}	Propagation Delay (Note 11) X_1 to F_0		23		26	ns	C_L = 15pF R_L = 280Ω
23	t_{PHL}			21		23	ns	

Notes:
6. The frequency guarantees apply with C_X connected to C_1, C_2, C_3, C_4 or HIGH. The C_X input load must be considered part of the 50pF/2.0kΩ clock output loading.
7. These setup and hold times apply to the F_0 LOW-to-HIGH transition of the period in which C_X goes LOW.
8. These inputs are synchronized internally. Failure to meet t_s may cause a $1/F_0$ delay but will not cause incorrect operation.
9. These inputs are "debounced" by an internal R-S flip-flop and are intended to be connected to manual break-before-make switches.
10. FIRST/LAST is normally wired HIGH or LOW.
11. Reference point of T offset has been moved forward which has increased T offsets.

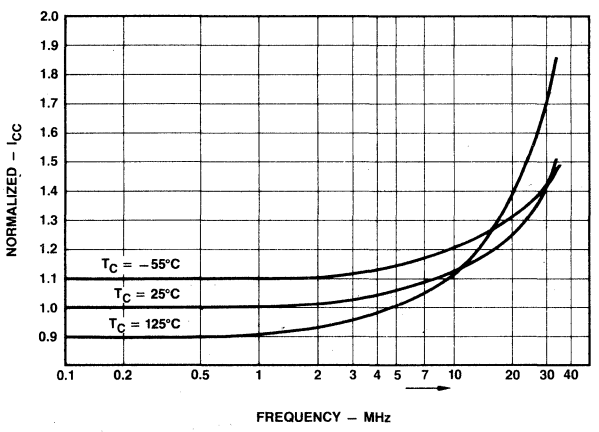
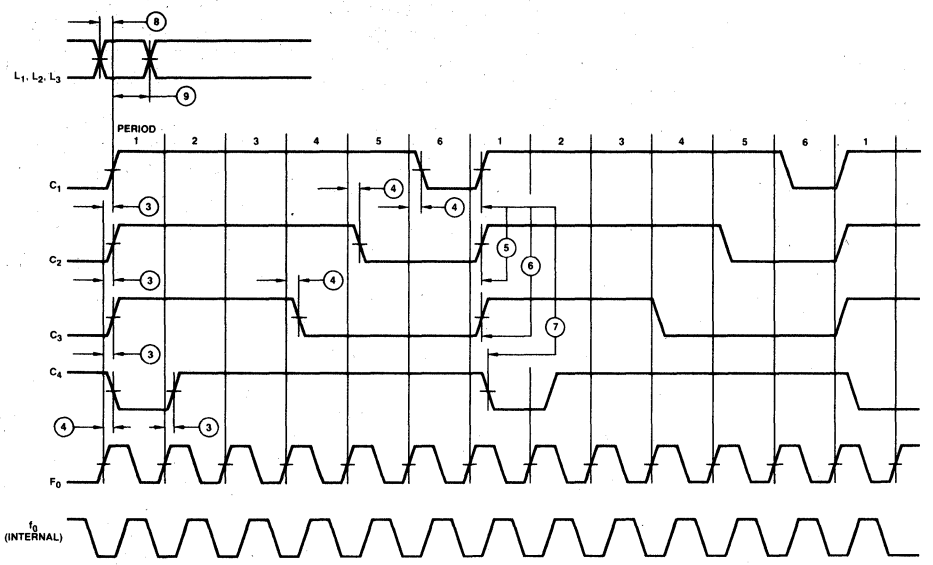


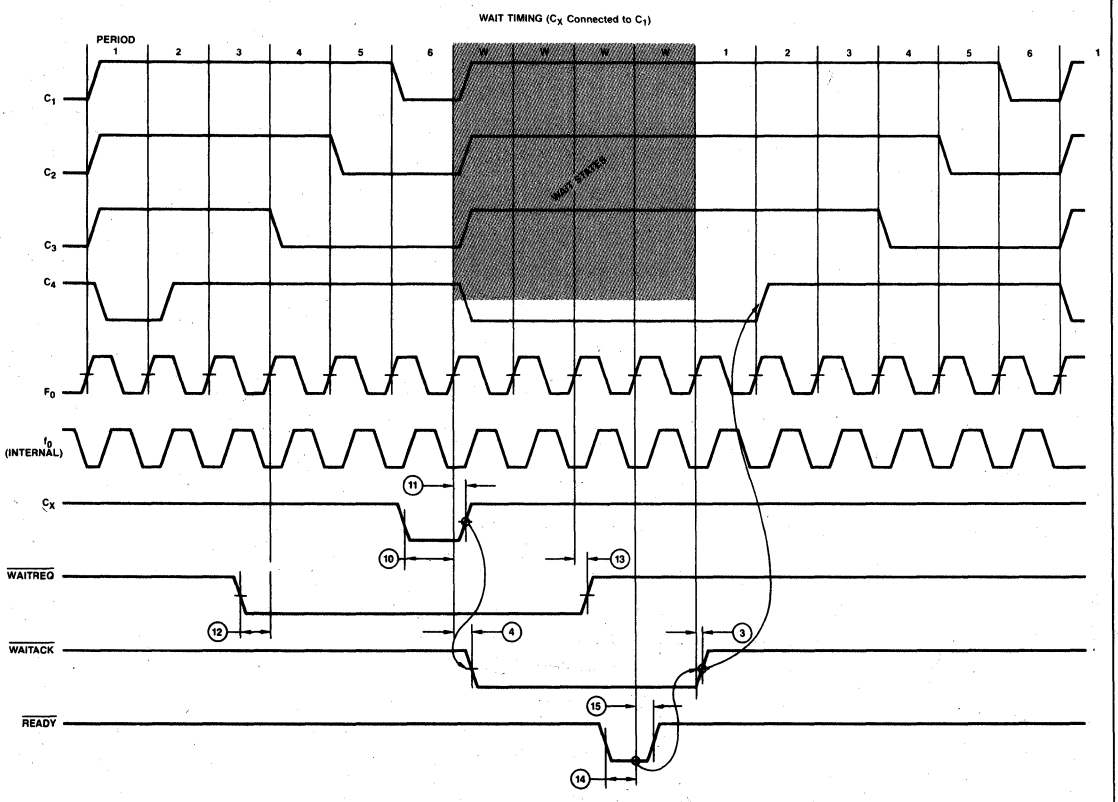
Figure 2. Am2925 I_{CC} Normalized vs Frequency (V_{CC} = 5.5V)

MPR-785

SWITCHING CHARACTERISTICS



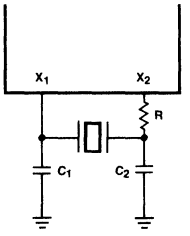
NORMAL CYCLE WITHOUT WAIT STATES (Pattern F_6 Shown) MPR-786



WAIT TIMING (C_X Connected to C_1) MPR-787

Am2925 OSCILLATOR APPLICATIONS

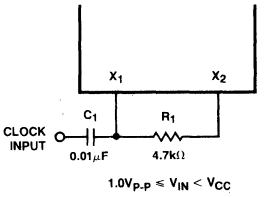
EXTERNAL COMPONENT CALCULATIONS SUMMARY



R = 0Ω for 6-20 MHz

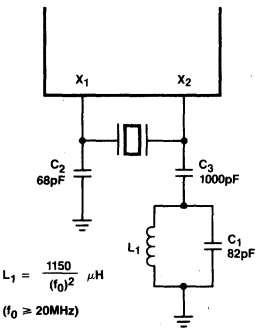
$R = X_{C_2} \simeq \frac{1}{2\pi f C_2}$ for 1-6 MHz

FUNDAMENTAL OSCILLATOR MPR-788



$1.0V_{P\text{-}P} \leq V_{IN} < V_{CC}$

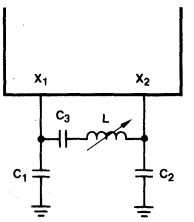
EXTERNAL CLOCK DRIVE MPR-789



$L_1 = \frac{1150}{(f_0)^2}\ \mu H$

$(f_0 \geq 20MHz)$

3rd HARMONIC OSCILLATOR MPR-790



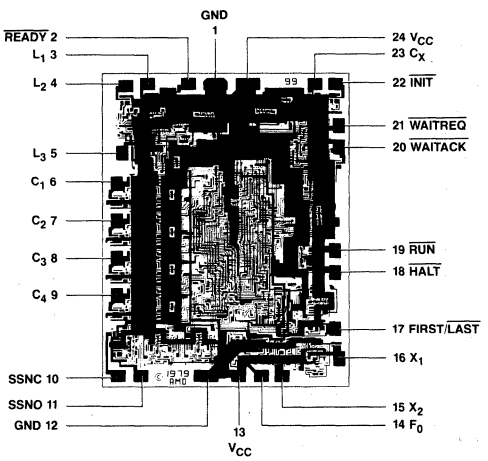
$f_0 = \frac{1}{2\pi\sqrt{2LC}}$

$C_1 = C_2 = C$

$X_{C_3} \ll X_L$

L-C OSCILLATOR MPR-791

METALLIZATION AND PAD LAYOUT



DIE SIZE .097" X .122"

Am2925 APPLICATIONS

DETAILED FUNCTIONAL DESCRIPTION

The Am2925 is a dynamically programmable general-purpose clock generator/driver. It can be logically separated into three parts. There is an oscillator, a state machine decoder and a state machine control section.

The oscillator is a linear inverting amplifier which with a minimum of external parts may be configured as a 1st harmonic* crystal oscillator, 3rd harmonic* crystal oscillator, L-C oscillator or used to buffer an external clock. the buffered, inverted output of this oscillator is availavble as F_0.

The state machine takes microcode information from the Microcycle Length "L" inputs L_1, L_2 and L_3 and counts the fundamental frequency of the internal oscillator, F_0, to create the clock outputs, C_1, C_2, C_3 and C_4.

The clock outputs have a characteristic wave shape relationship for each microcycle length. For example, C_1 is always LOW only on the last F_0 clock period of a microcycle and C_4 is always LOW on the first. C_3 has an approximately 50% duty cycle, and C_2 is HIGH for all but the last two periods.

The current state of the machine is contained in a register, part of which is the Clock Generator Register. C_1, C_2, C_3 and C_4 are the outputs of this register. These outputs and the outputs of the Microcycle Control Latch are fed into a set of combinatorial logic to generate the next state. On each falling edge of the internal clock the next state is entered into the current state register. The Microcycle Control Latch is latched when C_1 is HIGH. This means that it will be loaded during the last state of each microcycle, (C_1 = C_2 = C_3 = LOW, C_4 = HIGH). This internal latch selects one of eight possible microcycle lengths, F_3 to F_{10}.

The state machine control logic, which determines the mode of operation of the state machine, is intended to be connected to a front panel. There are four basic modes of operation of the Am2925 comprised of Run, Halt, Wait and Single Step.

SYSTEM TIMING

In the typical computer, the time required to execute different instructions varies. However, the time allotted to each instruction is the time that it takes to execute the longest instruction. The Am2925 allows the user to dynamically vary the time allotted for each instruction, thereby allowing the user to realize a higher throughput.

This application note will cover several aspects of the Am2925. The first topic to be covered is the oscillator section which is responsible for providing the basis of all system timing. Second will be how to operate the Am2925; last will be an example of an Am2925 in a 16-bit microprogrammed machine.

OSCILLATOR

The Am2925 contains an inverting, linear amplifier which is intended to form the basis of a crystal oscillator. In designing this oscillator it is necessary to consider several factors related to the application.

The first consideration is the desired frequency accuracy. This may be subdivided into several areas. An oscillator is considered stable if it is insensitive to variations in temperature and supply voltage, and if it is unaffected by individual component changes and aging. The design of the Am2925 is such that the degree to which these goals are met is determined primarily by the choice of external components. Various types of crystals are available and the manufacturers' literature should be consulted to determine the appropriate type. For good temperature stability, zero temperature coefficient capacitors should be used (Type NPO). For extreme temperature stability, an oven must be used or some other form of temperature compensation applied.

Absolute frequency accuracy must also be considered. The resonant frequency varies with load capacitance. It is therefore important to match the load specified by the crystal manufacturer for a standard crystal (usually 32pF), or to specify the load when ordering a special crystal. It should then be possible to determine from the crystal characteristics the load tolerance to maintain a given accuracy. If the "set-on" error due to load tolerance is unacceptable, a trimmer capacitor should be incorporated for fine adjustment.

The mechanism by which a crystal resonates is electromechanical. This resonance occurs at a fundamental frequency (1st harmonic) and at all odd harmonics of this frequency (even harmonic resonance is not mechanically possible). Unless otherwise constrained crystal oscillators operate at their fundamental frequency. However, crystals are not generally available with fundamental frequencies above 20-25MHz. At higher frequencies, an overtone oscillator must be used. In this case, the crystal is designed to oscillate efficiently at one of its odd harmonic frequencies and additional components are included in the oscillator circuit to prevent it oscillating at lower harmonics.

Where a high degree of accuracy or stability is not required, the amplifier may be configured as an L-C oscillator. It may also be driven from an external clock source if operation is required in synchronism with that source.

1st Harmonic (Fundamental) Oscillator

The circuit of a typical 1st harmonic oscillator is shown in Figure 1. The crystal load is comprised of the two 68pF capacitors in series. This 34pF approximates the standard 32pF crystal load. If a closer match is required then one of the capacitors should be replaced with a parallel combination of a fixed capacitor and a trimmer. The nominal value of the combination should be 60pF to provide proper crystal loading.

A typical crystal specification for use in this circuit is:

Frequency Range: 5–20MHz
Resonance: Parallel Mode
Load: 32pF
Stability: .01% or to match systems requirements
Case: H-17 – for smaller size
Temp Range: −30 to +70°C
Note: Frequency will change over temp

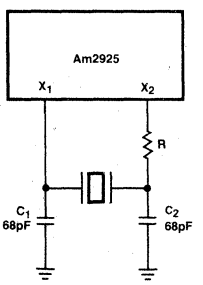


Figure 1. Connections for 5-20 MHz MPR-792

*It is understood that the terms "fundamental mode" and "3rd overtone" are generally regarded as more technically correct, but "1st harmonic" and "3rd harmonic" are used here because of their more generally accepted usage

It is good practice to ground the case of the crystal to eliminate stray pick-up and keep all connections as short as possible.

Note: At fundamental frequencies below 5MHz it is possible for the oscillator to operate at the 3rd harmonic. To prevent this a resistor should be added in series with the X_2 pin as shown in the circuit diagram.

The resistor value should match the impedance of C_2:

$$R = X_{C_2} = \frac{1}{2\pi f C_2}$$

3rd Harmonic Oscillator

At frequencies greater than 20MHz the crystal can be operated at its 3rd harmonic. A typical circuit is shown in Figure 2. Two additional components are included; an inductor, L_1, and a capacitor, C_3. The purpose of the capacitor is to block the d.c. path through the inductor and thereby maintain the correct amplifier bias. C_3 should be large (≥1000pF).

The inductor forms a parallel tuned circuit with C_1. This circuit has its resonance set between the 1st and 3rd harmonics of the crystal and is used to prevent the oscillator operating at the 1st harmonic. In the 1st harmonic oscillator (Figure 1), the crystal appears as an inductor and forms a π-network with the two capacitors, thus providing the necessary phase shift for oscillation. In the 3rd harmonic oscillator, L_1 and C_1 are chosen such that at the 3rd harmonic the impedance of circuit is equivalent to that of the capacitor C_2 in the 1st harmonic oscillator, (Figure 3b). Thus, the same π-network is formed (Figure 3c) and oscillation is possible. At the 1st harmonic the tuned circuit appears as an inductor (Figure 3a), the π-network is not formed and oscillation is not possible.

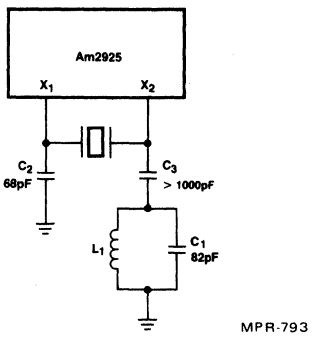
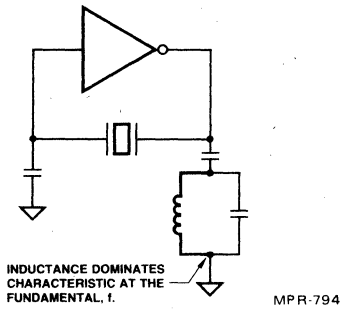


Figure 2. Connections for Frequencies above 20MHz

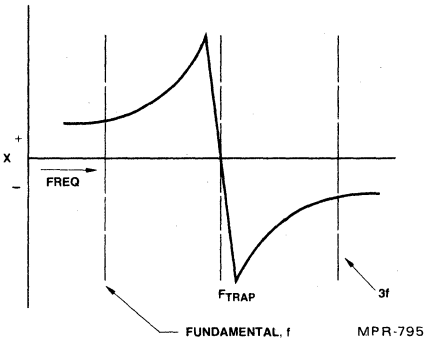
The following specification is typical for a crystal to be used in a 3rd harmonic oscillator.

Frequency Range: Above 20MHz
Resonance: Parallel Mode
Load: 32pF
Stability: .01% or to match systems requirements
Case: H-17 – for smaller size
Temp Range: −30 to +70°C
Note: Frequency will change temp

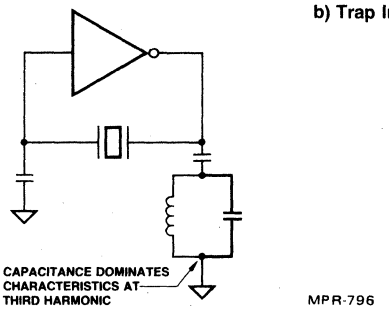
Again it is good practice to ground the crystal case and keep connections short.



a) Fundamental Equivalent



b) Trap Impedance



c) 3rd Harmonic Equivalent

Figure 3. Forcing Third Harmonic Oscillation

Design Procedure

(1) Assume C_1 = 82pF and C_2 = 68pF (this gives a sensible inductor value). L_1 is calculated according to the formula

$$L_1 = \frac{1151}{f_o{}^2}$$

f_o = Operating frequency in MHz
L_1 in μH

This sets the resonant frequency of the L-C combination at 0.52 f_o.

(2) Select the closest standard value inductor for L_1. Using this value calculate C_1 such that the resulting crystal load at the 3rd harmonic is 32pF.

$$C_1 = 60 + \frac{25330}{L_1 \cdot f_o{}^2} \qquad C_1 \text{ in pF.}$$

Choose the closest standard capacitor value to this.

Using standard values both the resonant frequency of the L-C circuit (f_r) and the crystal load are non-optimal. This will cause a slight error in the oscillating frequency. If this is not permissible C_1 may be a fixed capacitor in parallel with a trimmer such that the range of adjustment includes the calculated value for C_1. This is then set to give the desired frequency. In either case the approximate inductor value will cause the resonant frequency to the L-C circuit to change. This frequency, f_r, may be computed and should remain approximately midway between the 1st and 3rd harmonic.

$$f_r = \frac{159}{\sqrt{L_1 \cdot C_1}}$$

f_r in MHz
L_1 in μH
C_1 in pF.

L-C Oscillator

The Am2925 can be operated as an L-C tuned oscillator (Figure 4) and will perform as a stable oscillator within the restrictions of the chosen frequency determining components, i.e., (inductor and capacitors). The circuit chosen is a classical π-network with DC loop isolation. The Am2925 oscillator is a DC biased linear amplifier. This DC bias is necessary and therefore C_3 is included to block the DC path through the inductor. If a variable slug tuned inductor is used a moderate range of frequency adjustment tuneability (approximately 2:1) can be achieved. The range can be enhanced by switching the two resonant capacitors (C_1, C_2) to larger or smaller values. The specific frequency of operation can be determined by the formula

$$f = \frac{1}{2\pi\sqrt{L\,C}}$$

(where C is C_1 and C_2 in series).

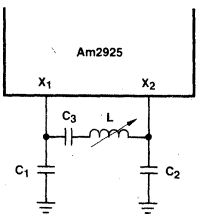


Figure 4. L-C Tuned Oscillator

External Clock Drive

The Am2925 can be driven from an external clock source at a signal level of 1.0V P-P or greater. This is accomplished by reducing the gain of the amplifier, and AC coupling the input signal (Figure 5). The gain is reduced by feeding the amplifier output back to the input through a 4.7kΩ resistor. AC coupling is provided by a 0.01μF capacitor. The controlled gain minimizes ringing caused by the fast rising edges of the driver.

The AC coupling maintains oscillator output symmetry by preserving oscillator DC bias levels. X_1 can be driven directly by TTL levels meeting the DC input requirements.

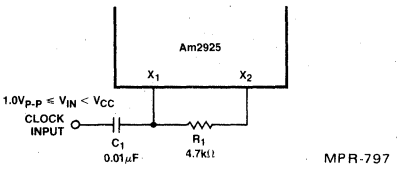


Figure 5. External Clock Drive

Am2925 Control Inputs

The control inputs fall into two categories, microcycle length control and clock control. Microcycle length control is provided via the "L" inputs which is intended to be connected to the microprogram memory. The "L" inputs are used to select one of eight cycle lengths ranging from three oscillator cycles for pattern F_3 to ten oscillator cycles for pattern F_{10}. This information is always loaded at the end of the microcycle into the Microcycle Control Latch. The microcycle latch performs the function of a pipeline register for the microcycle length microcode bits. Therefore, the cycle length goes in the same microword as the instruction that it is associated with.

The clock control inputs are used to synchronize the microprogram machine with the external world and I/O devices. Inputs like $\overline{\text{RUN}}$, $\overline{\text{HALT}}$, SSNO and SSNC, which start and stop execution, are meant to be connected to switches on the front panel of the microprogrammed machine (see Figure 6). These inputs have internal pull-up resistors and are connected to an R-S flip-flop in order to provide switch debouncing. The FIRST/$\overline{\text{LAST}}$ input is used to determine at what point of the microcycle the Am2925 will halt when $\overline{\text{HALT}}$ or a SINGLE STEP is initiated. In most applications the user wires this input HIGH or LOW depending on his design.

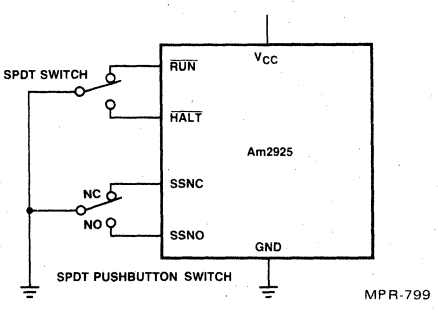


Figure 6. Switch Connection for $\overline{\text{RUN}}$/$\overline{\text{HALT}}$ and Single Step

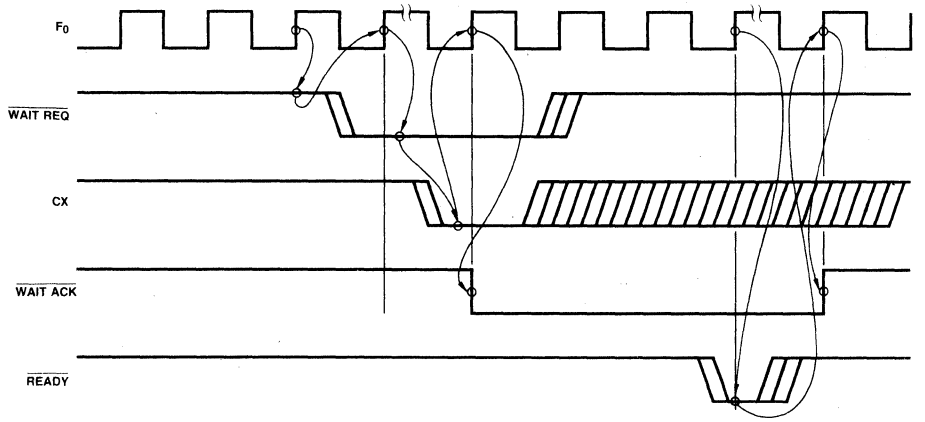


Figure 7. Am2925 $\overline{\text{WAIT}}/\overline{\text{READY}}$ Timing MPR-800

When $\overline{\text{HALT}}$ is held low ($\overline{\text{RUN}}$ = HIGH) the state machine will start the halt mode on the last (C_1 = LOW) or the first (C_4 = LOW) state of the microcycle as determined by the FIRST/$\overline{\text{LAST}}$ input. When $\overline{\text{RUN}}$ goes low ($\overline{\text{HALT}}$ = HIGH) the state machine will resume the run mode.

The $\overline{\text{WAITREQ}}$, C_X, $\overline{\text{READY}}$ and $\overline{\text{WAITACK}}$ signals are used to synchronize other parts of a computer system (memory, I/O devices) to the CPU by dynamically stretching the microcycle. For example, the CPU may access a slow peripheral that requires the data remain on the data bus for several microseconds in which case the peripheral pulls the $\overline{\text{WAITREQ}}$ line LOW. The C_X input lets the designer specify when the $\overline{\text{WAITREQ}}$ line is sampled in the microcycle. This has a direct impact on how much time the peripheral has to respond in order to request a wait cycle (see Figure 7). The $\overline{\text{READY}}$ line is used by the peripheral to signal when it is ready to resume execution of the rest of the microcycle. The $\overline{\text{WAITACK}}$ line goes LOW on the next oscillator cycle after the C_X input goes LOW and remains LOW until the second oscillator cycle after $\overline{\text{READY}}$ goes LOW.

The SSNO and SSNC inputs are used to initiate the SINGLE STEP mode. These debounced inputs allow a single microcycle to occur while in the halt mode. SSNO (normally open) and SSNC (normally closed) are intended to be connected to a momentary SPDT switch. After SSNO has been low for one clock edge, the state machine will change to the run mode. The microcycle will end on the first or last state of the microcycle depending on the state of the FIRST/$\overline{\text{LAST}}$.

AC Timing Signal References

Set-up and hold times in registers and latches are measured relative to the clock signals that drives them. In the Am2925, the crystal oscillator provides a free running clock signal that drives all the registers on the devices. This clock is provided for the user through the buffered output of F_0. Therefore, F_0 is used as the reference for set-up, hold and clock to output times. However for the Microcontrol Latch, the set-up and hold times are referenced to the C_1 output which is the buffered version of the latch enable. This reference is appropriate for the Microcontrol Latch because in a typical application this latch is considered part of the pipeline register which is also driven by one of the "C" outputs.

Clock Outputs

There are four clock outputs provided for the user which have different duty cycles. The user must make a decision as to which one best fits his purposes. For example, in a three address architecture, with the Am2903 (Figure 8), the C_3 clock (approximately 50% duty cycle) could be used to drive the clock input while C_2 (always low last two oscillator cycles) drives Instruction Enable. This guarantees, for microcycle lengths greater than four, that the internal RAM data latches of the Am2903 are closed and the destination address is multiplexed onto the B address bus before the RAM begins the Write cycle (Figure 9).

16-BIT MACHINE WITH Am2925

The block diagram in Figure 10 shows a 16-bit microprogrammed machine which uses an Am2925 to generate system timing. The design decisions include oscillator frequency and clock pattern selections.

Selecting the Crystal

In order to pick the oscillator frequency, a detailed timing analysis of the machine must be done in order to determine the execution length of every operation to be performed. For each operation there will be several delay paths, which usually include the ALU and the microprogram control.

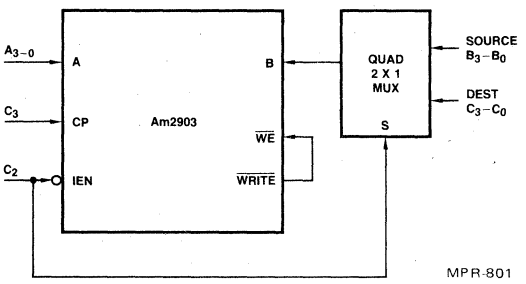


Figure 8. Am2903 Three Address Architecture

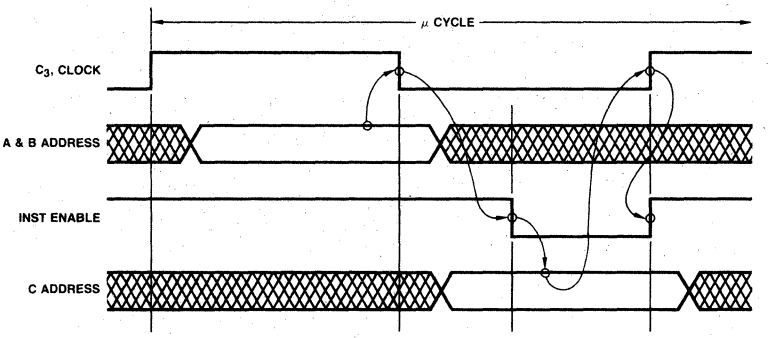


Figure 9. Am2903 Three Address Operation MPR-802

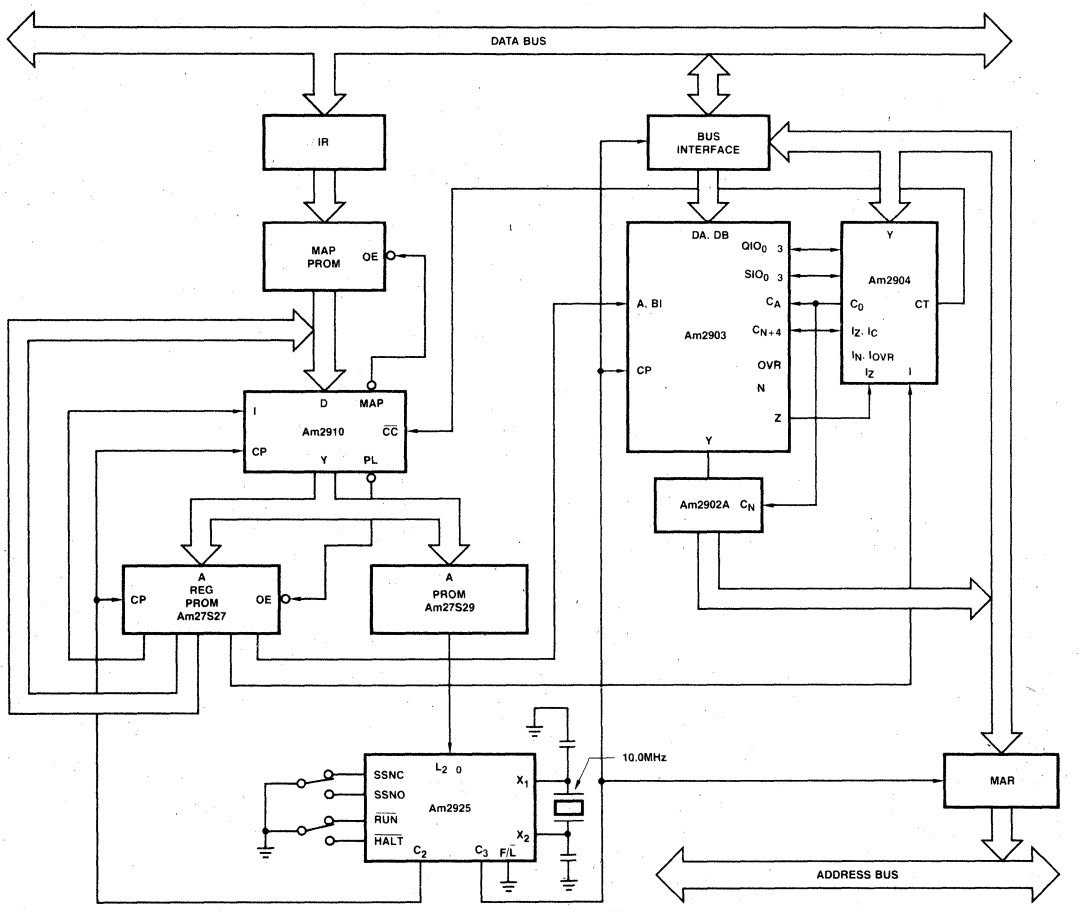


Figure 10. 16-Bit Microprogrammed Machine MPR-803

Figure 11 is an example of two of these paths. PATH 1 is a path through the Am2910 (Figure 10) for a microprogram Conditional Jump Subroutine. PATH 2 is a data flow path through the Am2903 for an Add instruction. Therefore, if the operation were an Add with a Conditional Jump Subroutine the maximum delay would be 196ns. If there were a Program Control Unit also, then delays through it would have to be considered.

After the execution times all of the instruction types have been calculated, the oscillator frequency can be selected. It is desirable to minimize the difference between the most commonly used instructions and multiples of the oscillator period. In this way the most efficient use can be made of the variable microcycle scheme.

For example, in the hypothetical machine in Figure 10 there are five instruction types (most machines will have more). Figure 12 is a table which lists each instruction type, corresponding execution time, and anticipated percentage of the typical instruction stream for each instruction. Several possible frequencies are shown which contain the next highest multiple of the corresponding oscillator period for each instruction. 20MHz is the best choice because it comes closest to matching instructions A and C which compose 90% of the typical instruction stream.

In this example, 20MHz was chosen. At 20MHz there is a choice between fundamental or overtone crystals. Fundamental frequency crystals are commonly available up to 25MHz and 3rd harmonic crystals are available above 17MHz. A fundamental crystal was selected for the example machine because the component count for the oscillator design is lower than for the overtone design. However, if it had turned out that 30MHz was a better choice then overtone operation would be chosen since fundamental crystals above 25MHz are not generally available.

Fixed Bandwidth Buses

For those designs that require a data bus with fixed bandwidth and fixed time slots for each memory access, the designer should consider using cycle lengths which are a multiple of the shortest cycle length, i.e., cycle lengths 3, 6 and 9 or cycle lengths 4 and 8. The design could further require that the bus be accessed only during the shortest cycle length. Therefore, by using multiple cycle lengths it can be predicted when the CPU will access the bus and for how long, thereby maintaining the fixed bandwidth.

Performance Comparison

Estimated performance can be calculated directly from Figure 12. For a fixed microcycle machine the longest instruction execution time would have to be used for all instructions, yielding an average instruction time of 228ns. With a variable microcycle machine the average instruction time is the sum of the products for each instruction, of the percentage of the instruction stream and the next highest multiple. The average instruction for the example machine with a 20MHz crystal is:

$$(0.6 \times 150 + .08 \times 200 + .3 + 200 + .01 \times 200 + .01 + 250) = 170.5\text{ns}$$

This represents a 25% increase in system performance without requiring any other system speed-ups and without requiring faster devices.

Device No.	Device Path	Path 1	Path 2
Am27S27	CP – Q	27	27
Am2904	INST – CT	58	–
Am2903	I/AB – GP	–	81
Am2910	CC – Y	43	–
Am2902A	GP – CN + Z	–	7
Am27S27	TS	55	–
Am2903	CN – Z	–	64
Am2904	TSZ	–	17
Total	ns	183	196

Figure 11. Delay Path Totals for an Add and a Conditional Jump Subroutine

Instruction Type	A	B	C	D	E	Unit
Execution Time	143	180	184	200	228	ns
Percentage of Instruction Stream	60%	8%	30%	1%	1%	%
Closest Multiple Oscillator Period						
20MHz P = 50	150 (3P)	200 (4P)	200 (4P)	200 (4P)	250 (5P)	ns
25MHz P = 40	160 (4P)	200 (5P)	200 (5P)	200 (5P)	240 (6P)	ns
30MHz P = 33	167 (5P)	200 (6P)	200 (6P)	200 (6P)	233 (7P)	ns
33MHz P = 30	150 (5P)	180 (6P)	210 (7P)	210 (7P)	240 (8P)	ns

Figure 12. Instruction Time Analysis

Am2926 • Am2929

Schottky Three-State Quad Bus Driver/Receiver

Distinctive Characteristics

- Advanced Schottky technology
- 48mA driver sink current
- 3-state outputs on driver and receiver
- PNP inputs
- Am2926 has inverting outputs
- Am2929 has non-inverting outputs
- Driver propagation delay – 14ns max for Am2926; 17ns max for Am2929
- Receiver propagation delay – 14ns max for Am2926; 17ns max for Am2929

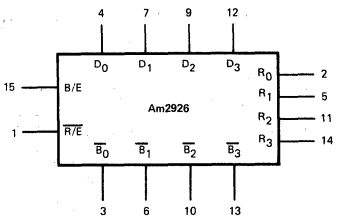
FUNCTIONAL DESCRIPTION

The Am2926 and Am2929 are high speed bus transceivers consisting of four bus drivers with three-state outputs and four bus receivers, also with three-state outputs. Each driver output is internally connected to a receiver input. Both the drivers and receivers have PNP inputs.

One buffered common "bus enable" input is connected to the four drivers and another buffered common "receiver enable" input is connected to the receivers. A LOW on the bus enable (B/E) input forces the four driver outputs to the high-impedance state. A HIGH on the bus enable allows input data to be transferred onto the data bus.

A HIGH on the receiver enable ($\overline{R/E}$) input forces the four receiver outputs to the high-impedance state while a LOW on the receiver enable input allows the received data to be transferred to the output. The complementary design of the bus enable and receiver enable inputs allows these control inputs to be connected together externally such that a single transmit/receive function is derived.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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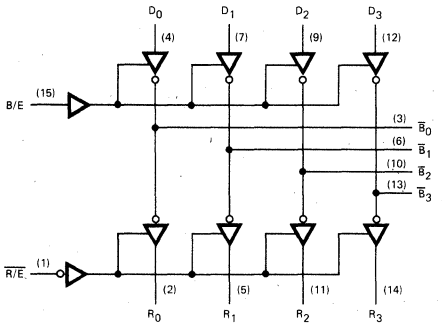
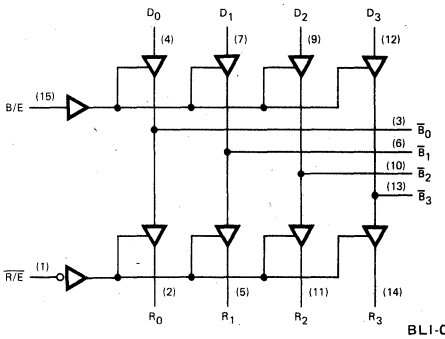
LOGIC DIAGRAMS

Am2926
Inverting Output (3-State)



Am2929
Non-Inverting Output (3-State)



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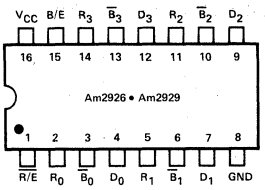
CONNECTION DIAGRAM
Top View



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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs (Receiver)	30mA
DC Output Current, Into Outputs (BUS)	80mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

The Following Conditions Apply Unless Otherwise Noted:

Am2926PC, DC, XC Am2929PC, DC, XC T_A = 0°C to +75°C (COM'L) MIN. = 4.75 V MAX. = 5.25 V

Am2929DM, XM Am2926DM, XM T_A = −55°C to +125°C (MIL) MIN. = 4.50 V MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
Driver						
I_{IL}	Low Level Input Current	V_{IN} = 0.4 V			−200	μA
I_{IL}	Low Level Input Current (Disabled)	V_{IN} = 0.4 V			−25	μA
I_{IH}	High Level Input Current (D_{IN}, D_E)	V_{IN} = V_{CC} MAX.			25	μA
V_{OL}	Low Level Output Voltage	I_{OUT} = 48 mA (Note 5)			0.5	Volts
V_{OH}	High Level Output Voltage	I_{OUT} = −10 mA, V_{CC} = V_{CC} MIN. (Note 6)	2.4			Volts
I_{OS}	Short Circuit Output Current	V_{OUT} = 0 V, V_{CC} = V_{CC} MAX. (Note 4)	−50		−150	mA
Receiver						
I_{IL}	Low Level Input Current	V_{IN} = 0.4 V			−200	μA
I_{IH}	High Level Input Current (R_E)	V_{IN} = V_{CC} MAX.			25	μA
V_{OL}	Low Level Output Voltage	I_{OUT} = 20 mA (Note 5)			0.5	Volts
V_{OH}	High Level Output Voltage	I_{OUT} = −100 μA, V_{CC} = 5.0 V	3.5			Volts
		I_{OUT} = −2.0 mA (Note 6)	2.4			
I_{OS}	Short Circuit Output Current	V_{OUT} = 0 V, V_{CC} = V_{CC} MAX.	−30		−75	mA
Both Driver and Receiver						
V_{TL}	Low Level Input Threshold Voltage		0.85			Volts
V_{TH}	High Level Input Threshold Voltage				2.0	Volts
I_O	Low Level Output Off Leakage Current	V_{OUT} = 0.5 V			−100	μA
	High Level Output Off Leakage Current	V_{OUT} = 2.4 V			100	μA
V_I	Input Clamp Voltage	I_{IN} = −12 mA			−1.0	Volts
P_{WR}/I_{CC}	Power/Current Consumption (Am2926)	V_{CC} = V_{CC} MAX.			457/87	mW/mA
	Power/Current Consumption (Am2929)	V_{CC} = V_{CC} MAX.			578/110	

Switching Characteristics (T_A = +25°C, V_{CC} = 5.0 V)

Parameters	Description	Test Conditions	Am2926 Min.	Am2926 Typ.	Am2926 Max.	Am2929 Min.	Am2929 Typ.	Am2929 Max.	Units
t_{PLH}	Driver Input to Bus	Figure 1		10	14		13	17	ns
t_{PHL}				10	14		13	17	
t_{PLH}	Bus to Receiver Output	Figure 2		9.0	14		12	17	ns
t_{PHL}				6.0	14		9.0	17	
t_{ZL}	Driver Enable to Bus	Figure 3		19	25		21	28	ns
t_{LZ}				15	20		18	23	
t_{ZL}	Receiver Enable to Receiver Output	Figure 4		15	20		18	23	ns
t_{LZ}				10	15		13	18	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Output sink current is supplied through a resistor to V_{CC}.
6. Measurements apply to each output and the associated data input independently.

DEFINITION OF FUNCTIONAL TERMS

D_0, D_1, D_2, D_3 The four driver inputs.

$\overline{B_0}, \overline{B_1}, \overline{B_2}, \overline{B_3}$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the driver inputs is non-inverted.

B/E Bus enable input. When the bus enable input is LOW, the four driver outputs are in the high-impedance state.

$\overline{R/E}$ Receiver enable input. When the receiver enable input is HIGH, the four receiver outputs are in the high-impedance state.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	LOW Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{R/E}$	1	1/8	–	–
R_0	2	–	50	10
$\overline{B_0}$	3	1/16	250	25
D_0	4	1/8	–	–
R_1	5	–	50	10
$\overline{B_1}$	6	1/16	250	25
D_1	7	1/8	–	–
GND	8	–	–	–
D_2	9	1/8	–	–
$\overline{B_2}$	10	1/16	250	25
R_2	11	–	50	10
D_3	12	1/8	–	–
$\overline{B_3}$	13	1/16	250	25
R_3	14	–	50	10
B/E	15	1/8	–	–
V_{CC}	16	–	–	–

A TTL Unit Load is defined as −1.6mA measured at 0.4V LOW and 40μA measured at 2.4V HIGH.

DRIVER FUNCTION TABLE

INPUTS		Am2926 OUTPUT	Am2929 OUTPUT
B/E	D_i	$\overline{B_i}$	$\overline{B_i}$
L	X	Z	Z
H	L	H	L
H	H	L	H

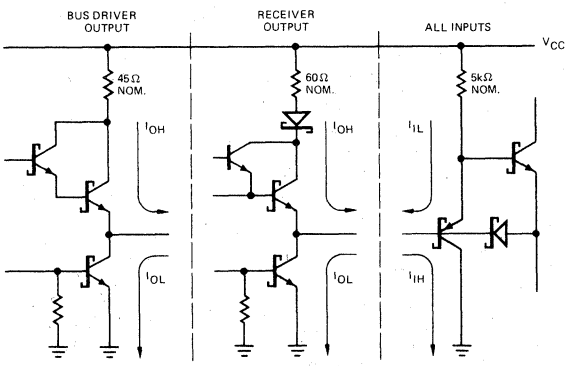
L = LOW X = Don't Care
H = HIGH Z = High Impedance
i = 0, 1, 2, or 3

RECEIVER FUNCTION TABLE

INPUTS		Am2926 OUTPUT	Am2929 OUTPUT
$\overline{R/E}$	$\overline{B_i}$	R_i	R_i
H	X	Z	Z
L	L	H	L
L	H	L	H

L = LOW X = Don't Care
H = HIGH Z = High Impedance
i = 0, 1, 2, or 3

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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AC TEST CIRCUITS AND WAVEFORMS

PROPAGATION DELAY (Data In to Bus)

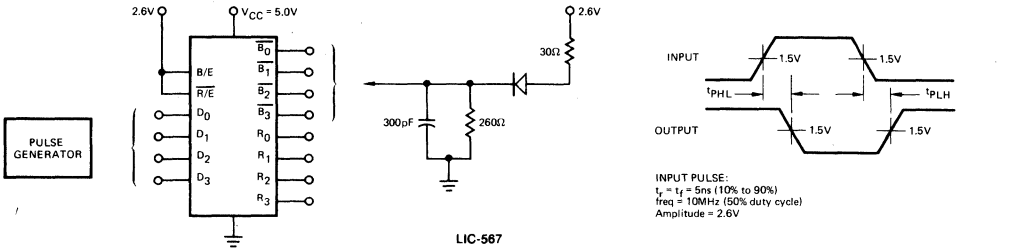

Figure 1

BLI-083

PROPAGATION DELAY (Bus to Receiver Out)

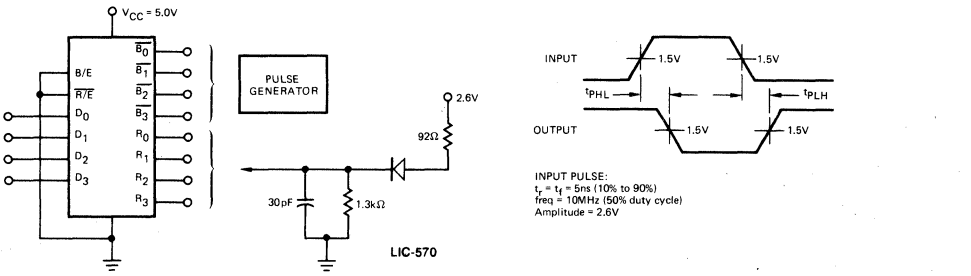

Figure 2

BLI-084

PROPAGATION DELAY (Bus Enable to Bus Output)

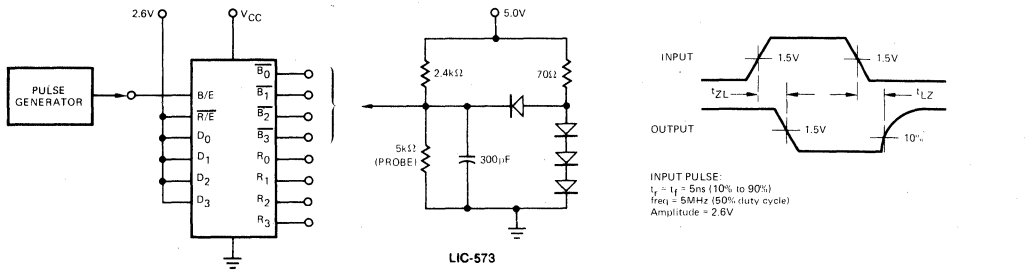

Figure 3

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PROPAGATION DELAY (Receive Enable to Receive Output)

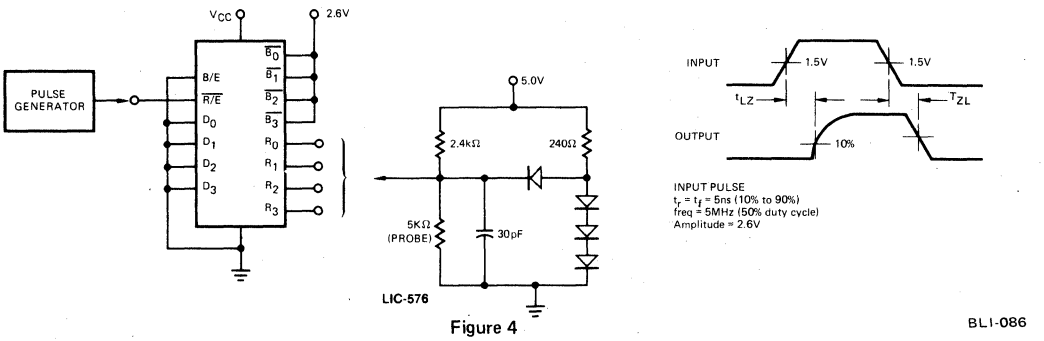

Figure 4

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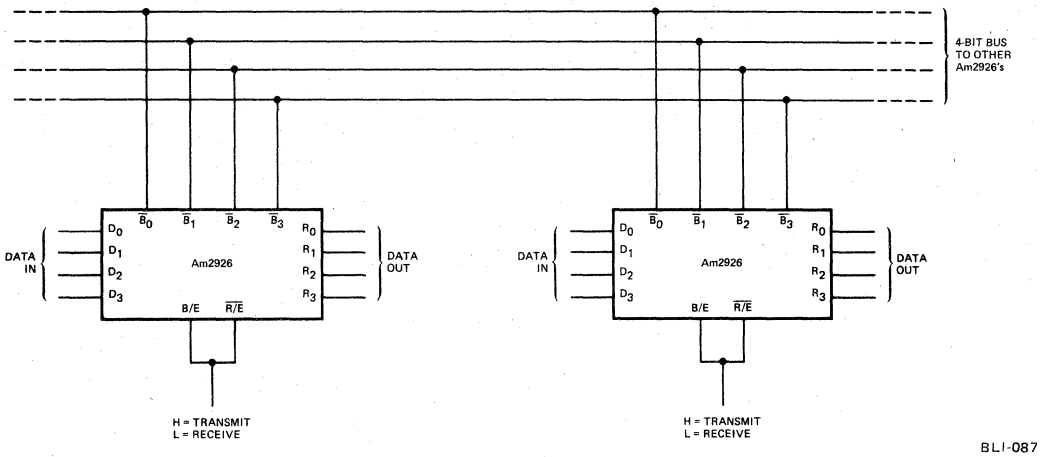
APPLICATION



ORDERING INFORMATION

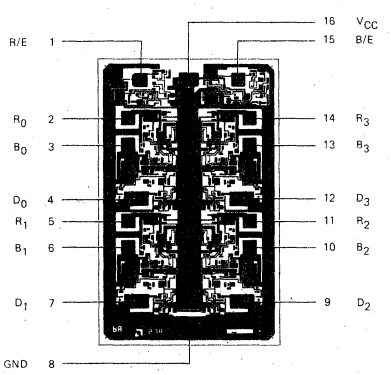
Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2926 Order Number	Am2929 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2929PC	AM2929PC	P-16-1	C	C-1
AM2929DC	AM2929DC	D-16-1	C	C-1
AM2929DC-B	AM2929DC-B	D-16-1	C	B-1
AM2926DM		D-16-1	M	C-3
AM2926DM-B		D-16-1	M	B-3
AM2926XC	AM2929XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010 B.
AM2926XM		Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to 70°C, V_{CC} = 4.75V to 5.25V, M = −55 to + 125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

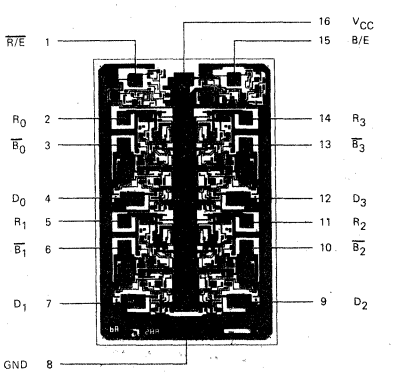
Metallization and Pad Layouts

Am2926



DIE SIZE 0.058" X 0.091"

Am2929



DIE SIZE 0.058" X 0.091"

Am2927 • Am2928

Quad Three-State Bus Transceivers With Clock Enable

DISTINCTIVE CHARACTERISTICS

- Quad high-speed LSI bus-transceivers
- Three-state bus driver and receiver outputs
- D-type register on drivers
- Latch output on Am2927
- Registered output on Am2928
- Output data to input wrap around gating
- Input register to output transfer gating with or without driving data bus
- Clock enabled registers
- Bus driver outputs can sink 48mA at 0.5V max.
- Three-state receiver outputs sink 24mA at 0.5V max.
- 3.0V minimum V_{OH} for direct interface to MOS microprocessors
- Advanced low-power Schottky processing

FUNCTIONAL DESCRIPTION

The Am2927 and Am2928 are high-performance, low-power Schottky, quad bus transceivers intended for use in bipolar or MOS microprocessor system applications.

Both devices feature register enable lines which function as clock enables without introducing gate delay in the clock inputs. The four transceivers share common enables, clock, select and three-state control lines.

The Am2927 consists of four D-type edge-triggered flip-flops. Each flip-flop output is connected to a three-state data bus driver and separately to the input of a corresponding receiver latch input. The receiver latch can select input from the driver or the data bus. The select line determines the source of input data for the bus driver choosing between input data or data recirculated from the receiver output. The receiver output also has a three-state output buffer.

The combination of the select input, S, the driver input enable, $\overline{ENDR}$, and the receiver latch enable, $\overline{RLE}$, provide seven different data path operating modes not available in other transceivers. For example, transmitted data can be stored in the receiver for subsequent retransmission. Also, received data can be output to the system and simultaneously fed back to the driver input.

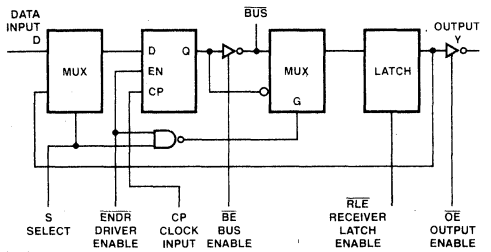
The Am2928 is similar to the Am2927, but with a D-type edge-triggered register in the receiver and a receiver enable, $\overline{ENREC}$, which functions as a common clock enable.

Data from each D input is inverted at the bus output. Likewise, data at the bus input is inverted at the receiver output.

All three-state controls and enable lines are active low (the Am2927 receiver latch is transparent when $\overline{RLE}$ is LOW). The select input, S, determines whether the enabled driver input accepts data from the data input, D, or from the corresponding receiver output, Y. Similarly, the select line determines whether the receiver accepts input data from the data bus, or the driver output.

SIMPLIFIED LOGIC DIAGRAMS

Am2927



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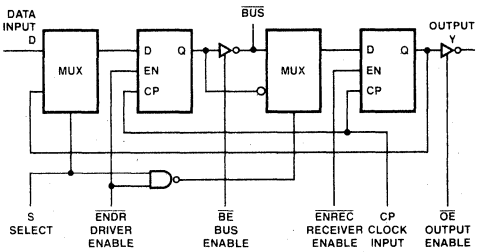
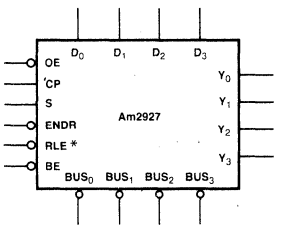
Am2928



LOGIC SYMBOL



*ENREC for Am2928

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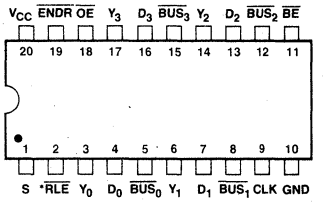
Am2927 CONNECTION DIAGRAM – Top View



Note: Pin 1 is marked for orientation.

*ENREC for Am2928

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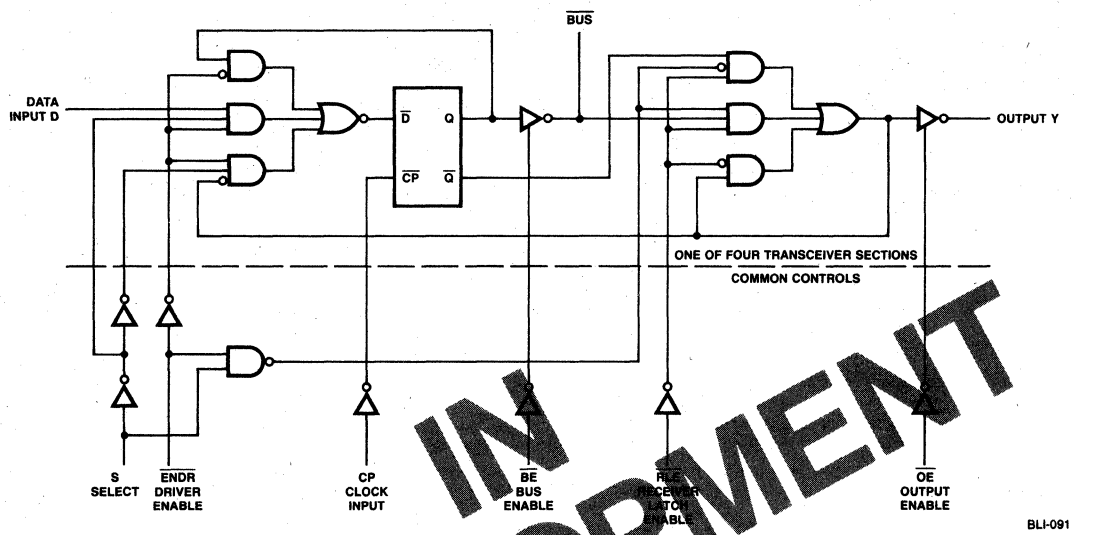
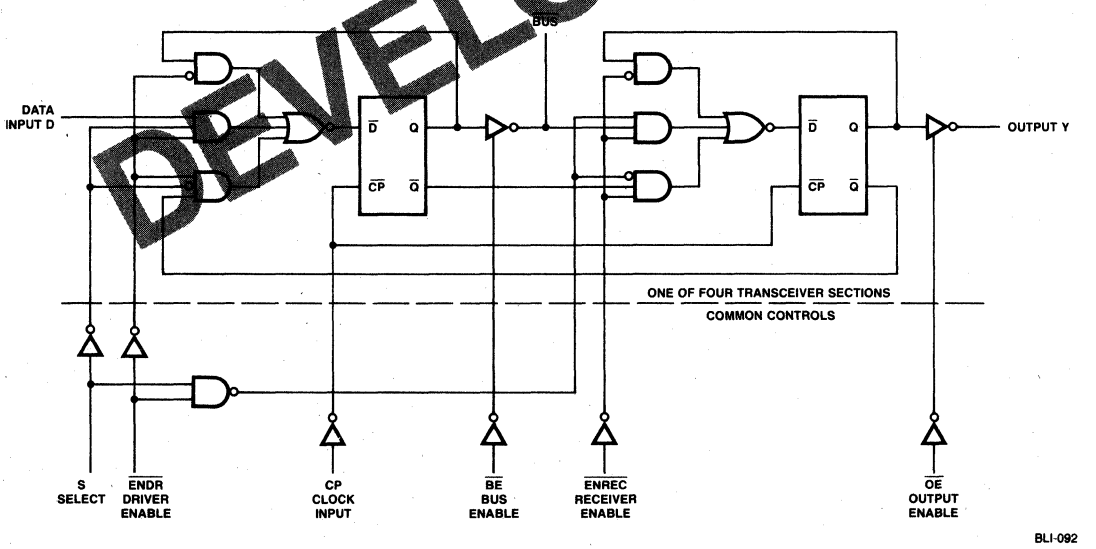
DETAILED LOGIC DIAGRAMS

Am2927



Am2928



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential	−0.5 to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs (Except BUS)	30 mA
DC Output Current, Into Bus	100 mA
DC Input Current	−30 to +5.0mA

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	T_A = 0 to +70°C	V_{CC} = 5.0V ±5%	(MIN = 4.75V MAX = 5.25V)
MIL	T_A = −55 to +125°C	V_{CC} = 5.0V ±10%	(MIN = 4.50V MAX = 5.50V)

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN	I_{OL} = 24mA			0.4	Volts
			I_{OL} = 48mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN	COM'L, I_{OH} = −20mA	2.4			Volts
			MIL, I_{OH} = −15mA	2.4			
V_{IH}	Receiver Input HIGH Threshold	Bus Enable = 2.4V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus Enable = 2.4V				0.8	Volts
I_{OFF}	Bus Leakage Current (Power Off)	V_{CC} = 0V, V_O = 4.5V				100	µA
I_{OZL}	Bus Leakage Current (HIGH Impedance)	V_{CC} = MAX Bus Enable = 2.4V	V_O = 0.4V			−1.4	mA
I_{OZH}			V_O = 2.5V			100	µA
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX, V_O = 0V		−50		−255	mA
C_B	Bus Capacitance (Note 4)	V_{CC} = 0V			8		pF

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. This parameter is typical of device characterization data and is not tested in production.

5

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	T_A = 0 to +70°C	V_{CC} = 5.0V ±5%	(MIN = 4.75V MAX = 5.25V)
MIL	T_A = −55 to +125°C	V_{CC} = 5.0V ±10%	(MIN = 4.50V MAX = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE (Except Bus Ports)

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −2.0mA	2.4	3.4		Volts
			COM'L, I_{OH} = −6.5mA	2.4	3.4		
		V_{CC} = 5.0V	I_{OH} = −100µA	3.0			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH}	I_{OL} = 24mA			0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.8	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	S, $\overline{ENDR}$			−2.8	mA
			All other inputs			−1.4	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	S, $\overline{ENDR}$			100	µA
			All other inputs			50	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{OZH}	Off-State Output Current (Receiver Output)	V_{CC} = MAX	V_O = 2.4V			100	µA
I_{OZL}			V_O = 0.5V			−50	
I_{SC}	Output Short Circuit Current	V_{CC} = MAX	Receiver	−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX	Am2927		150	185	mA
			Am2928		153	190	

Am2927/2928
Am2927
SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2927XM			Am2927XC			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Driver Clock, CP, to $\overline{BUS}$	C_L (BUS) = 50pF, R_L (BUS) = 130Ω		18	26		18	23	ns
t_{PHL}				18	26		18	23	
$t_{ZH} \bullet t_{ZL}$	Bus Enable, $\overline{BE}$, to $\overline{BUS}$			14	26		14	23	ns
t_{HZ} / t_{LZ}		R_L = 130Ω, C_L = 5pF		12	18/30		12	16/23	
t_{PW}	Min Clock Pulse Width (HIGH or LOW)		18			15			ns
t_{PLH}	$\overline{BUS}$ to Receiver Output (Latch Enabled)	C_L = 50pF, R_L = 270Ω			23		16	20	ns
t_{PHL}					23		16	20	
t_{PLH}	Latch Enable, $\overline{RLE}$, to Receiver Output				26		18	23	ns
t_{PHL}					26		18	23	
$t_{ZH} \bullet t_{ZL}$	Output Enable, $\overline{OE}$, to Receiver Output				23			21	ns
$t_{HZ} \bullet t_{LZ}$		C_L = 5pF, R_L = 270Ω			21		14	18	
t_s	Driver Enable, $\overline{ENDR}$, to Clock		10			9			ns
t_h			3			3			
t_s	Select, S, to Clock ($\overline{RLE}$ = HIGH)		18			15			ns
t_h			3			2			
t_{PLH}	Select, S, to Receiver Output	C_L = 50pF, R_L = 270Ω			26			23	ns
t_{PHL}					35			30	
t_s	Data Inputs, D, to Clock		9						ns
t_h			5			4			
t_s	$\overline{BUS}$ to Latch Enable, $\overline{RLE}$		11			10			ns
t_h			2			3			

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Am2928
SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2928XM			Am2928XC			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Clock, CP, to $\overline{BUS}$	C_L (BUS) = 50pF, R_L (BUS) = 130Ω			26		18	23	ns
t_{PHL}					26		18	23	
$t_{ZH} \bullet t_{ZL}$	Bus Enable, $\overline{BE}$, to $\overline{BUS}$				26		14	23	ns
t_{HZ} / t_{LZ}		R_L = 130Ω, C_L = 5pF			18/30		12	16/23	
t_{PLH}	Clock, CP, to Receiver Output	C_L = 50pF, R_L = 270Ω			26		18	23	ns
t_{PHL}					26		18	23	
t_{PW}	Min Clock Pulse Width (HIGH or LOW)		18			15			ns
$t_{ZH} \bullet t_{ZL}$	Output Enable, $\overline{OE}$, to Receiver Output				23		14	21	ns
$t_{HZ} \bullet t_{LZ}$		C_L = 5pF, R_L = 270Ω			26		21	18	
t_s	Driver Enable, $\overline{ENDR}$, to Clock		10			9			ns
t_h			3			3			
t_s	$\overline{BUS}$ to Clock (Receiver Register)		8			7			ns
t_h			5			4			
t_s	Receiver Enable, $\overline{ENREC}$, to Clock		10			8			ns
t_h			5			4			
t_s	S to Clock		12			10			ns
t_h			5			4			
t_s	Data Inputs, D, to Clock (Driver Register)		9			7			ns
t_h			5			4			

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

DEFINITION OF FUNCTIONAL TERMS

CP Clock Pulse to internal registers enters data on the LOW-to-HIGH transition.

$\overline{BE}$ Bus Enable. When Bus Enable is LOW the four drivers drive the $\overline{BUS}$ outputs.

$\overline{BUS}_0$, $\overline{BUS}_1$, $\overline{BUS}_2$, $\overline{BUS}_3$ The four driver outputs and receiver inputs.

D_0, D_1, D_2, D_3 The four driver data inputs inverting from D to $\overline{BUS}$.

Y_0, Y_1, Y_2, Y_3 The four receiver data outputs inverting from $\overline{BUS}$ to Y.

S Select input controls data path modes in conjunction with $\overline{ENDR}$ and $\overline{RLE}$ (or $\overline{ENREC}$).

$\overline{OE}$ Output Enable. When Output Enable is LOW the four receiver outputs Y are active.

$\overline{ENDR}$ Driver Enable. Common clock enable for the input register. Allows the data on the D inputs to be loaded into the driver register on the clock LOW-to-HIGH transition.

$\overline{RLE}$ Receiver Latch Enable (Am2927 only). When Receiver Latch Enable is LOW, the four receiver latches are transparent. The latches hold received data when $\overline{RLE}$ is HIGH.

$\overline{ENREC}$ Receiver Enable (Am2928 only). Common clock enable for the receiver register. Allows the $\overline{BUS}$ driver or previous receiver data to enter the receiver register on the rising edge of the clock.

Am2927 FUNCTION TABLES

Driver Register Control

$\overline{ENDR}$	S	$\overline{RLE}$	Driver Register
H	X	X	Hold Previous Data
L	L	X	Load from D Input
L	H	L	Load from $\overline{BUS}$
L	H	H	Load Latched Receiver Data

Receiver Latch Control

$\overline{ENDR}$	S	$\overline{RLE}$	Receiver Output
X	X	H	Data Latched
H	H	L	Driver Register Output at Y Output (Latch Transparent)
X	L	L	Bus Data at Y Output (Latch Transparent)
L	X	L	

Am2928 FUNCTION TABLES

Driver Register Control

$\overline{ENDR}$	S	Driver Register
H	X	Hold Previous Data
L	L	Load from D Input
L	H	Load from Receiver Register

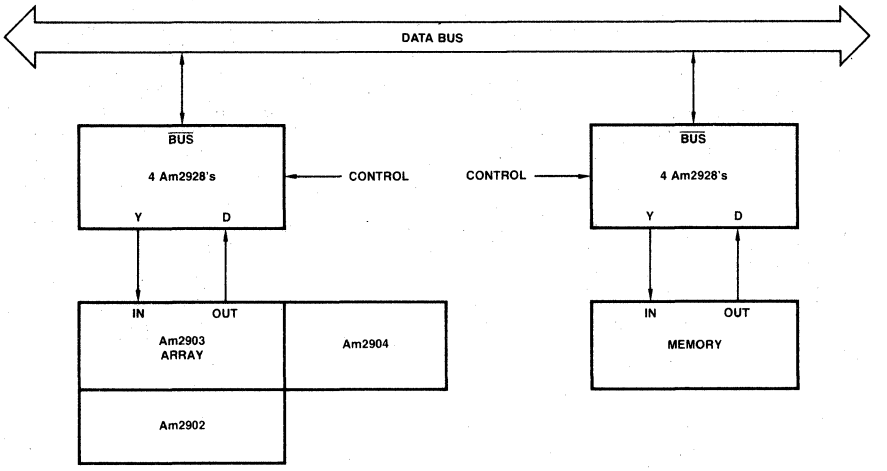
Receiver Register Control

$\overline{ENDR}$	S	$\overline{ENREC}$	Receiver Output
X	X	H	Hold Previous Data
H	H	L	Load from Driver Register
X	L	L	Load from $\overline{BUS}$
L	X	L	

ORDERING INFORMATION

Am2927 Order Number	Am2928 Order Number	Package Type	Operating Range	Screening Level
AM2927DC	AM2928DC	D-20	C	C-1
AM2927DM	AM2928DM	D-20	M	C-3
AM2927LC	AM2928LC	L-28	C	C-1
AM2927LCB	AM2928LCB	L-28	C	B-2
AM2927LM	AM2928LM	L-28	M	C-3
AM2927LMB	AM2928LMB	L-28	M	B-3
AM2927XC	AM2928XC	Dice	C	Visual inspection to MIL-STD-883 method 2010B
AM2927XM	AM2928XM	Dice	M	

APPLICATION



The Am2927 and Am2928 can be used to provide Data Bus, Address Bus and Control Bus Interface in a high-speed bipolar microprocessor system.

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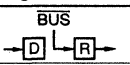
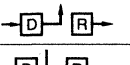
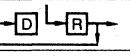
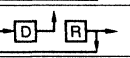
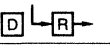
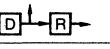
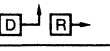
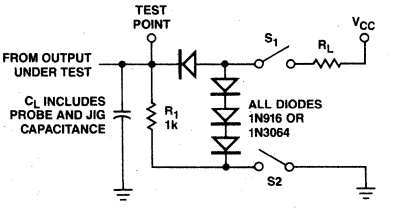
Am2927 AND Am2928 FUNCTION TABLE

Driver Input From	Receiver Input From	Control Input Condition			Signal Flow	$\overline{BE}$
		S	$\overline{ENDR}$	*		
D Input	BUS	L	L	L		H
	(No Load)	L	L	H		L
Receiver	BUS	H	L	L		H
	(No Load)	H	L	H		L
(No Load)	BUS	L	H	L		H
	Driver	H	H	L		X
	(No Load)	X	H	H		L

*$\overline{RLE}$ for Am2927 (asynchronous) or $\overline{ENREC}$ for Am2928 (⌐).

LOAD TEST CIRCUIT



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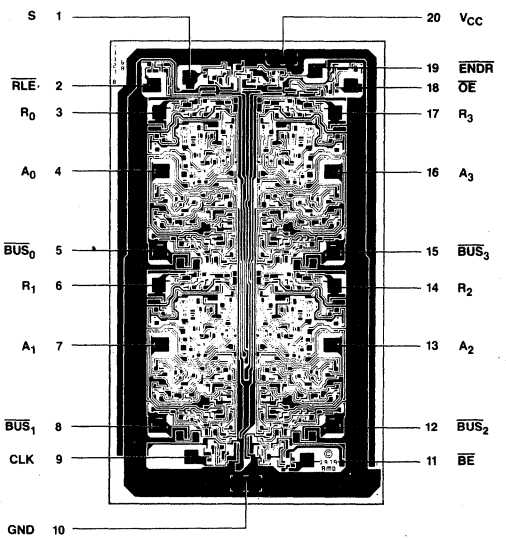
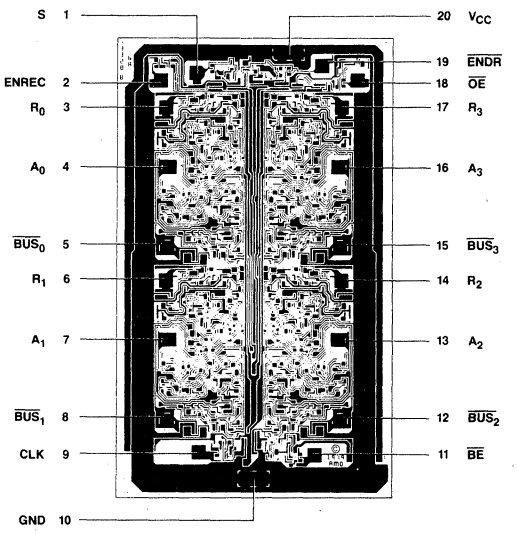
Note: For standard totem-pole outputs, remove R_1; S_1 and S_2 closed.

METALLIZATION AND PAD LAYOUTS

Am2927



Am2928



DIE SIZE 0.087" X 0.144"

Am2930
Program Control Unit

DISTINCTIVE CHARACTERISTICS

- Powerful, 4-bit slice address controller for memories
  Useful with both main memory and microprogram memory
  Expandable to generate any address length
- Executes 32 instructions
  Automatic generation of address and update of program counter for fetch cycles, branch cycles, and subroutine call and return
- Contains cascadable full adder
  Twelve different relative address instructions are provided; including jump-to-subroutine relative and return-from-subroutine relative
- Built-in condition code input
  Sixteen instructions are dependent on external condition control
- Seventeen-level push/pop stack
  On-chip storage of subroutine return addresses nested up to 17 levels deep
- Separate incrementer for program counter
  A relative address may be computed and PC may be incremented by one on a single cycle

GENERAL DESCRIPTION

The Am2930 is a four-bit wide Program Control Unit intended to perform machine level addressing functions, although the device can also be used as a microprogram sequencer. Four Am2930's may be interconnected to generate a 16-bit address (64K words). The Am2930 contains a program counter, a subroutine stack, an auxiliary register, and a full adder for computing relative addresses.

The Am2930 performs five types of instructions. These are: 1) Unconditional Fetch; 2) Conditional Jump; 3) Conditional Jump-to-Subroutine; 4) Conditional Return-from-Subroutine; and 5) miscellaneous instructions.

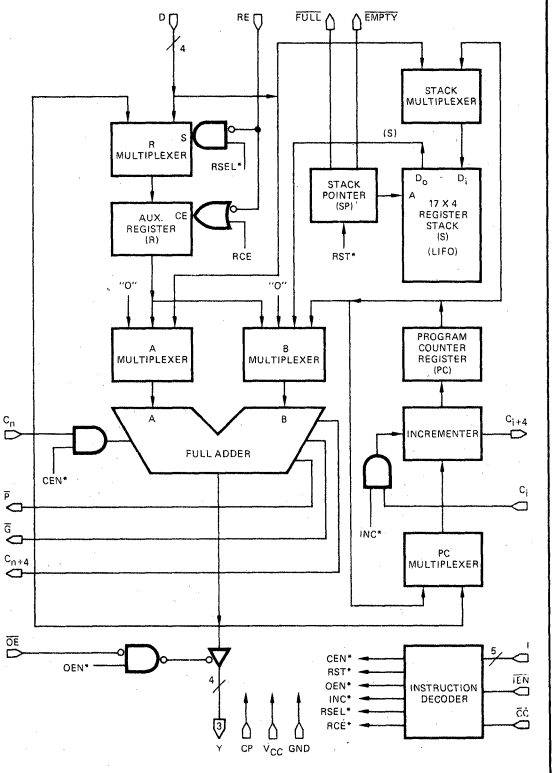
There are four sources of data for the adder which generates the Address outputs (Y_0-Y_3). These are: 1) the Program Counter (PC); 2) the Stack (S); 3) the auxiliary Register(R); and 4) the Direct inputs (D). Under control of the Instruction inputs (I_0-I_4), the multiplexers at the adder inputs allow various combinations of these terms to be generated at the three-state Y address outputs. The instruction lines also control the updating of the program counter and the auxiliary register. A condition code input is provided for conditional instructions.

RELATED PRODUCTS

Part No.	Description
Am2902A	Carry Look-Ahead Generator
Am2904	Status and Shift Control Unit
Am2920	8-Bit Register
Am2922	Condition Code MUX

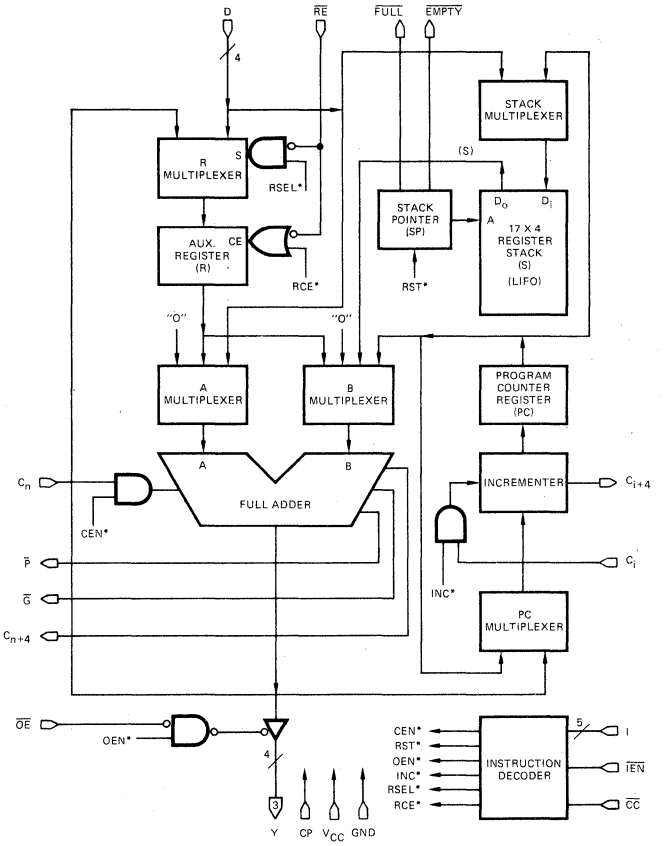
For applications information, see Chapter V of **Bit Slice Microprocessor Design**, Mick & Brick, McGraw Hill Publications.

BLOCK DIAGRAM



MPR-221

BLOCK DIAGRAM

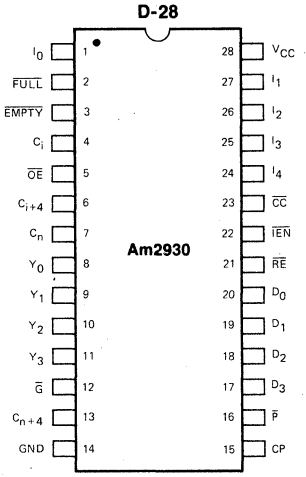


*INTERNAL

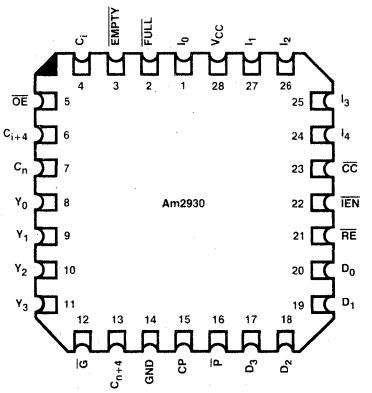
MPR-221

CONNECTION DIAGRAMS – Top Views

D-28



L-28-1



F-28 pin configuration identical to D-28.

Note: Pin 1 is marked for orientation.

MPR-225

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max.
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

OPERATING RANGE

Part Number	Temperature	V_{CC}
Am2930PC, DC	T_A = 0 to 70°C	4.75V to 5.25V
Am2930DM, FM	T_C = −55 to +125°C	4.50V to 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IL} or V_{IH}	Y_0, Y_1, Y_2, Y_3 $\overline{G}$, C_{n+4}, C_{i+4}	I_{OH} = −1.6mA	2.4			Volts
			$\overline{P}$, $\overline{FULL}$, $\overline{EMPTY}$	I_{OH} = −1.2mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IL} or V_{IH}	Y_0, Y_1, Y_2, Y_3	I_{OL} = 20mA (COM'L)			0.5	Volts
				I_{OL} = 16mA (MIL)			0.5	
			$\overline{G}$, C_{n+4} C_{i+4}	I_{OL} = 16mA			0.5	
			$\overline{P}$, $\overline{FULL}$, $\overline{EMPTY}$	I_{OL} = 12mA			0.5	
V_{IH}	Input HIGH Level (Note 4)				2.0			Volts
V_{IL}	Input LOW Level (Note 4)						0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V	D_{0-3}				−.360	mA
			I_{0-4}, $\overline{RE}$, $\overline{IEN}$, CP, $\overline{OE}$				−.702	
			$\overline{CC}$				−.657	
			C_i				−2.31	
			C_n				−3.25	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	D_{0-3}				20	μA
			I_{0-4}, $\overline{RE}$, $\overline{IEN}$, CP, $\overline{OE}$				40	
			$\overline{CC}$				50	
			C_i				90	
			C_n				250	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−30		−85	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX., $\overline{OE}$ = 2.4V	Y_{0-3}	V_{OUT} = 0.5V			−50	μA
I_{OZH}				V_{OUT} = 2.4V			50	
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX.		T_A = 25°C		150	205	mA
				T_C = −55 to +125°C			239	
				T_C = +125°C			170	
				T_A = 0 to 70°C			220	
				T_A = 70°C			185	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should only be tested in a static-, noise-free environment.
5. Minimum I_{CC} is at maximum temperature.

Am2930 SWITCHING CHARACTERISTICS

Tables A, B, C and D define the timing characteristics of the Am2930. Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level.

I. GUARANTEED PERFORMANCE OVER COMMERCIAL OPERATING RANGE.

V_{CC} = 4.75 to 5.25V, T_A = 0 to 70°C

TABLE IA
Clock Characteristics.

Minimum Clock LOW Time	31ns
Minimum Clock HIGH Time	33ns

TABLE IB
Output Enable/Disable Times.
All in ns.
C_L = 5.0pF for output disable tests.

From	To	Enable	Disable
$\overline{OE}$	Y	27	26
$\overline{CC}$ (Note 1)	Y	55	37
I_{4-0} (Note 1)	Y	80	55

Note 1: "Suspend" instruction.

TABLE IC
Combinational Propagation Delays.
All in ns.
Outputs fully loaded. C_L = 50pF.

From Input \ To Output	Y	$\overline{G}$, $\overline{P}$	C_{n+4}	C_{i+4} I_4=L	C_{i+4} I_4=H	$\overline{Full}$	$\overline{Empty}$
I_{4-0}	81	67	77	80	91	69	–
$\overline{CC}$	63	45	55	–	72	42	–
C_n	32	–	25	–	45	–	–
C_i	–	–	–	22	22	–	–
CP	69	53	61	43	78	55	55
D	49	33	40	–	59	–	–
$\overline{IEN}$	–	–	–	–	–	40	–

TABLE ID
Setup and Hold Times. All in ns.
All relative to clock
LOW-to-HIGH transition.

Input	CP: Set-up Time	CP: Hold Time
I_{4-0}	114	0
$\overline{CC}$	75	0
$\overline{IEN}$	55	0
C_n	43	0
C_i	32	5
D ($\overline{RE}$ = L, I_{4-0} = 0-8 or 10-15)	25	2
D (All other conditions)	66	2
$\overline{RE}$	24	4

II. GUARANTEED PERFORMANCE OVER MILITARY OPERATING RANGE.

V_{CC} = 4.5 to 5.5V, T_C = −55 to +125°C

TABLE IIA
Clock Characteristics.

Minimum Clock LOW Time	35ns
Minimum Clock HIGH Time	35ns

TABLE IIB
Output Enable/Disable Times.
All in ns.
C_L = 5.0pF for output disable tests.

From	To	Enable	Disable
$\overline{OE}$	Y	32	31
$\overline{CC}$ (Note 1)	Y	60	42
I_{4-0} (Note 1)	Y	85	60

Note 1: "Suspend" instruction.

TABLE IIC
Combinational Propagation Delays.
All in ns.
Outputs fully loaded. C_L = 50pF.

From Input \ To Output	Y	$\overline{G}$, $\overline{P}$	C_{n+4}	C_{i+4} I_4=L	C_{i+4} I_4=H	$\overline{Full}$	$\overline{Empty}$
I_{4-0}	88	74	82	87	97	78	–
$\overline{CC}$	68	52	60	–	78	47	–
C_n	37	–	30	–	46	–	–
C_i	–	–	–	23	23	–	–
CP	74	58	66	48	84	60	60
D	55	38	45	–	65	–	–
$\overline{IEN}$	–	–	–	–	–	45	–

TABLE IID
Setup and Hold Times. All in ns.
All relative to clock
LOW-to-HIGH transition.

Input	CP: Set-up Time	CP: Hold Time
I_{4-0}	124	0
$\overline{CC}$	80	0
$\overline{IEN}$	69	0
C_n	52	0
C_i	37	5
D ($\overline{RE}$ = L, I_{4-0} = 0-8 or 10-15)	30	2
D (All other conditions)	72	2
$\overline{RE}$	29	4

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5−8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

ARCHITECTURE OF THE Am2930

The Am2930 is a bipolar Program Control Unit intended for use in high-speed microprocessor applications. The device is a cascadable, four-bit slice such that three devices allow addressing of up to 4K words of memory and four devices allow addressing of up to 64K words of memory.

As shown in the Block Diagram, the device consists of the following:

1) A full adder with input multiplexers
2) A Program Counter Register with an incrementer and an input multiplexer
3) A 17 x 4 Last-In, First-Out (LIFO) stack consisting of an input multiplexer, a 17 x 4 RAM, and a Stack Pointer
4) An auxiliary register with an input multiplexer
5) An instruction decoder
6) Four 3-state output buffers on the address outputs

The following paragraphs describe each of these blocks in detail.

Full Adder

The Full Adder is a binary device with full lookahead carry logic for high-speed addition and provision is made for further lookahead by including both carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs. In slower systems, the carry output (C_{n+4}) can be connected to the next higher C_n to provide ripple block arithmetic. The carry input to the adder (C_n) is internally inhibited during those instructions which do not require an addition to be performed. For these instructions, the data is passed directly through the adder, independent of the state of C_n.

The multiplexers at the A and B inputs of the adder are controlled by the Instruction decoder which selects the appropriate adder inputs for the selected instruction.

Program Counter

The program counter consists of a register preceeded by an incrementer. The Program Counter Register (PC) is a four-bit, edge-triggered, D-type register which is loaded from the incrementer output on the LOW-to-HIGH transition of the clock input (CP) at the end of every instruction.

The incrementer utilizes full lookahead logic for high speed. For cascading devices, the carry output of the incrementer (C_{i+4}) is connected to the incrementer carry input (C_i) of the next higher device. The output of the incrementer, which is loaded into the PC, is equal to the incrementer input plus C_i. Therefore, it is possible to control the entire cascaded incrementer from the C_i input of the least significant device; a LOW on the C_i input of the least significant device will simply pass the data from the multiplexer output to the inputs of PC; a HIGH will cause the outputs of the multiplexer to be incremented before they are loaded into PC. During three instructions (unconditional Hold and conditional Hold and Suspend when the $\overline{CC}$ input is LOW), the C_i input is internally inhibited; therefore, data is passed from the multiplexer output to the PC without incrementing. The multiplexer selects the input to the incrementer from either PC or the output of the Full Adder, depending upon the instruction being executed. During the Jump, Jump-to-Subroutine, and Return instructions, the multiplexer chooses the Full Adder outputs as the input to the incrementer if the $\overline{CC}$ input is LOW. The Full Adder output is also selected for the Reset instruction. For all other instructions, the PC is selected as the input to the incrementer.

17 x 4 LIFO Stack

The 17 x 4 LIFO stack consists of a multiplexer, a 17 x 4 RAM, and a Stack Pointer (SP) which address the words in the RAM.

The SP always points to the last word written into the RAM (Top of the Stack). The Top of the Stack (S) is available at the output of the RAM.

Data is pushed onto the Top of the Stack from either D or PC. It is written into memory location SP+1. The SP is incremented on the LOW-to-HIGH clock transition at the end of the cycle so that it still points to the last data written into the RAM.

For a Pop operation, the contents of the RAM are not changed, but the SP is decremented at the end of the cycle so that it then points to the new Top of the Stack.

The SP is an up/down counter which changes state on the LOW-to-HIGH transition of the Clock input. It is internally prevented from incrementing when the stack is full and from decrementing when the Stack is empty. When the Stack is full, the RAM write circuitry is also inhibited.

The active LOW Empty output ($\overline{EMPTY}$) is LOW when the stack is empty (after the Reset instruction and after the last word has been Popped from the stack); the active LOW Full output ($\overline{FULL}$) is LOW either when the stack is full or when the current instruction being executed will fill the stack (during and after the 17th Push).

Auxiliary Register (R)

The Auxiliary Register (R) can be loaded from either the Direct inputs (D) or the output of the Full Adder. It is loaded on the LOW-to-HIGH transition of the clock input (CP) if the Register Enable input ($\overline{RE}$) is LOW or if the Instruction inputs call for it to be loaded. When $\overline{RE}$ is LOW, R is loaded from the D inputs unless the Instruction dictates that R be loaded from the output of the Full Adder.

Instruction Decoder

The Instruction Decoder generates the signals necessary to establish the data paths and to enable the loading of the PC, R, SP, and RAM.

For unconditional instructions, the $\overline{CC}$ input is not utilized; it may be either HIGH or LOW. For conditional instructions, if $\overline{CC}$ is LOW, the condition is met and the conditional operation is performed; if $\overline{CC}$ is HIGH, a Fetch PC is performed.

Output Buffers

The Address outputs (Y_0-Y_3) are three-state drivers which may be disabled either under Instruction control or by a HIGH on the Output Enable input ($\overline{OE}$). Disabling the Y outputs does not affect the execution of instructions inside the Am2930.

Instruction Enable

When HIGH, the Instruction Enable input ($\overline{IEN}$) forces PC and SP into the hold mode and disables the write circuitry to the RAM. The auxiliary register (R) is under control of the $\overline{RE}$ input when $\overline{IEN}$ is HIGH, independent of the state of the Instruction inputs. The $\overline{IEN}$ input does not affect the combinatorial data paths or Y outputs in the Am2930. The data paths are selected by the Instruction and $\overline{CC}$ inputs and are not affected by $\overline{IEN}$.

Am2930 INSTRUCTION SET

The Am2930 Instruction set can be divided into five types of instructions. These are:

- Unconditional Fetches
- Conditional Jumps
- Conditional Jumps-to-Subroutine
- Conditional Returns-from-Subroutine
- Miscellaneous Instructions

The following paragraphs describe each of these types in detail.

Unconditional Fetches

As can be seen from Table 1, there are nine unconditional Fetch instructions (Instructions 1-9). Under control of the Instruction inputs, the desired value is placed at the Y outputs. For all Fetch instructions, PC is incremented if C_i of the least significant device is HIGH. For Instructions 1 through 7, the auxiliary register is under control of the RE input. For Instructions 8 and 9, R is loaded with PC and R + D, respectively. The RAM and Stack Pointer are not changed during a Fetch instruction.

Conditional Jumps

There are six conditional Jump instructions (Instructions 16 through 21). Under control of the Instruction inputs, the desired value is placed at the Y outputs. Additionally, the value is incremented if C_i of the least significant device is HIGH and loaded into PC. During these instructions, R is controlled by $\overline{RE}$. The RAM and Stack Pointer are not changed during these instructions. The above operations are performed if the $\overline{CC}$ input is LOW; if $\overline{CC}$ is HIGH, a Fetch PC operation is performed.

Conditional Jumps-to-Subroutine

There are six conditional Jump-to-Subroutine instructions (Instructions 22 through 27). Under control of the Instruction inputs, the desired value is placed on the Y outputs. On the rising edge of the clock the value is incremented* and loaded into PC, PC is loaded into the RAM at location SP + 1; and SP is incremented.

As with Conditional Jump Instructions, R is controlled by $\overline{RE}$ and whether the Jump-to-Subroutine or Fetch PC is performed depends upon the state of the $\overline{CC}$ input.

Conditional Returns-from-Subroutine

There are two conditional Return-from-Subroutine instructions (Instructions 28 and 29). Under control of the instruction inputs, either S or S+D is placed at the Y outputs. Additionally, the selected value is incremented* and loaded into PC and SP is decremented at the end of the cycle (on the rising edge of the clock).

* If C_i of the least significant device is HIGH.

As with the Condition Jump and Jump-to-Subroutine Instructions, R is controlled by $\overline{RE}$ and whether the Return-from-Subroutine or Fetch PC is performed depends upon the state of the $\overline{CC}$ input.

Miscellaneous Instructions

Each of the nine miscellaneous instructions is described individually.

Reset (Instruction 0)

The Reset instruction forces the Y outputs to zero, loads either zero or one into PC, depending upon the C_i input of the least significant device, and resets SP. The RAM is unchanged and R is controlled by $\overline{RE}$.

Load R (Instruction 10)

This instruction loads the data on the D inputs into R. PC is either incremented or held depending upon C_i of the least significant device. The SP and RAM are not changed.

Push PC (Instruction 11)

This instruction is the same as Fetch PC except that PC is loaded into RAM and SP is incremented at the end of the cycle; i.e., the current PC is Pushed onto the stack.

Push D (Instruction 12)

This instruction is the same as Fetch PC except that D is loaded into the RAM and SP is incremented at the end of the cycle; i.e., external data is Pushed onto the stack.

Pop S (Instruction 13)

This instruction places the Top of the Stack (S) at the Y outputs and decrements SP at the end of the cycle. The PC is incremented if the C_i input of the least significant device is HIGH. R is controlled by $\overline{RE}$.

Pop PC (Instruction 14)

This instruction is the same as Fetch PC except SP is decremented at the end of the cycle, causing the data at the top of the stack to be lost.

Hold (Instruction 15)

This instruction places PC at the Y outputs and inhibits any change in PC, SP, and RAM. R is controlled by $\overline{RE}$.

Conditional Hold (Instruction 30)

This instruction is the same as Hold except $\overline{CC}$ must be LOW. If $\overline{CC}$ is HIGH, the Fetch PC instruction is performed.

Suspend (Instruction 31)

The Suspend instruction is the same as th Conditional Hold instruction except the Y outputs are forced into the high-impedance state if $\overline{CC}$ is LOW.

TABLE I – Am2930 INSTRUCTION SET

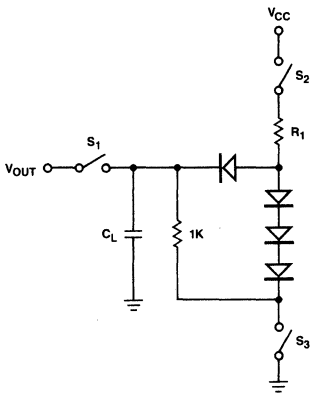
Mnemonic	Instruction Number	I_4	I_3	I_2	I_1	I_0	$\overline{CC}$	$\overline{IEN}$	Instruction	Y_0-Y_3	Next State (after CP ↓) (Note 3) PC	R $\overline{RE}$ = L	R $\overline{RE}$ = H	RAM	SP
		X	X	X	X	X	X	H	Instruction Disable	Note 1	–	D	–	–	–
PRST	0	L	L	L	L	L	X	L	RESET	"0"	"0"+C_i	D	–	–	Reset
FPC	1	L	L	L	L	H	X	L	FETCH PC	PC	PC+C_i	D	–	–	–
FR	2	L	L	L	H	L	X	L	FETCH R	R	PC+C_i	D	–	–	–
FD	3	L	L	L	H	H	X	L	FETCH D	D	PC+C_i	D	–	–	–
FRD	4	L	L	H	L	L	X	L	FETCH R+D	R+D+C_n	PC+C_i	D	–	–	–
FPD	5	L	L	H	L	H	X	L	FETCH PC+D	PC+D+C_n	PC+C_i	D	–	–	–
FPR	6	L	L	H	H	L	X	L	FETCH PC+R	PC+R+C_n	PC+C_i	D	–	–	–
FSD	7	L	L	H	H	H	X	L	FETCH S+D	S+D+C_n	PC+C_i	D	–	–	–
FPLR	8	L	H	L	L	L	X	L	FETCH PC → R	PC	PC+C_i	PC	PC	–	–
FRDR	9	L	H	L	L	H	X	L	FETCH R+D → R	R+D+C_n	PC+C_i	R+D+C_n	R+D+C_n	–	–
PLDR	10	L	H	L	H	L	X	L	LOAD R	PC	PC+C_i	D	D	–	–
PSHP	11	L	H	L	H	H	X	L	PUSH PC	PC	PC+C_i	D	–	PC → Loc SP+1	SP+1
PSHD	12	L	H	H	L	L	X	L	PUSH D	PC	PC+C_i	D	–	D → Loc SP+1	SP+1
POPS	13	L	H	H	L	H	X	L	POP S	S	PC+C_i	D	–	–	SP–1
POPP	14	L	H	H	H	L	X	L	POP PC	PC	PC+C_i	D	–	–	SP–1
PHLD	15	L	H	H	H	H	X	L	HOLD	PC	–	D	–	–	
	16-31	H	X	X	X	X	H	L	FAIL COND'L TEST (FETCH PC)	PC	PC+C_i	D	–	–	–
JMPR	16	H	L	L	L	L	L	L	JUMP R	R	R+C_i	D	–	–	–
JMPD	17	H	L	L	L	H	L	L	JUMP D	D	D+C_i	D	–	–	–
JMPZ	18	H	L	L	H	L	L	L	JUMP "0"	"0"	"0"+C_i	D	–	–	–
JPRD	19	H	L	L	H	H	L	L	JUMP R+D	R+D+C_n	R+D+C_n+C_i	D	–	–	–
JPPD	20	H	L	H	L	L	L	L	JUMP PC+D	PC+D+C_n	PC+D+C_n+C_i	D	–	–	–
JPPR	21	H	L	H	L	H	L	L	JUMP PC+R	PC+R+C_n	PC+R+C_n+C_i	D	–	–	–
JSBR	22	H	L	H	H	L	L	L	JSB R	R	R+C_i	D	–	PC → Loc SP+1	SP+1
JSBD	23	H	L	H	H	H	L	L	JSB D	D	D+C_i	D	–	PC → Loc SP+1	SP+1
JSBZ	24	H	H	L	L	L	L	L	JSB "0"	"0"	"0"+C_i	D	–	PC → Loc SP+1	SP+1
JSRD	25	H	H	L	L	H	L	L	JSB R+D	R+D+C_n	R+D+C_n+C_i	D	–	PC → Loc SP+1	SP+1
JSPD	26	H	H	L	H	L	L	L	JSB PC+D	PC+D+C_n	PC+D+C_n+C_i	D	–	PC → Loc SP+1	SP+1
JSPR	27	H	H	L	H	H	L	L	JSB PC+R	PC+R+C_n	PC+R+C_n+C_i	D	–	PC → Loc SP+1	SP+1
RTS	28	H	H	H	L	L	L	L	RETURN S	S	S+C_i	D	–	–	SP–1
RTSD	29	H	H	H	L	H	L	L	RETURN S+D	S+D+C_n	S+D+C_n+C_i	D	–	–	SP–1
CHLD	30	H	H	H	H	L	L	L	HOLD	PC	–	D	–	–	–
PSUS	31	H	H	H	H	H	L	L	SUSPEND	Z (Note 2)	–	D	–	–	–

PC – Program Counter SP – Stack Pointer S – Stack Top
R – Auxiliary Register D – Direct Inputs

Notes: 1. When $\overline{IEN}$ is HIGH, the Y_0-Y_3 outputs contain the same data as when $\overline{IEN}$ is LOW, as determined by I_0-I_4 and $\overline{CC}$.
2. Z = High impedance state (outputs "OFF").
3. – = No change.

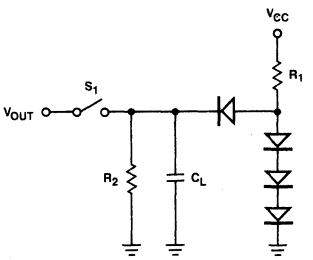
TEST OUTPUT LOAD CONFIGURATIONS FOR Am2930

A. THREE STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2930

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
2	$\overline{FULL}$	B	300	2K
3	$\overline{EMPTY}$	B	300	2K
6	C_{i+4}	B	240	1.5K
8-11	Y_{0-3}	A	240	1K
12	$\overline{G}$	B	240	1.5K
13	C_{n+4}	B	240	1.5K
16	P	B	300	2K

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

APPLICATIONS

The Am2930 is shown in a typical 16-bit, 2900 Microcomputer design in Figure 1.

The Direct inputs (D) of the Am2930 are derived from one of three sources: the Instruction Register, the Data Bus via a 16-bit register (two Am2920 8-bit Registers), and the output of the Am2901's via a 16-bit register.

The Address outputs (Y) of the Am2930 are loaded into a 16-bit Memory Address Register (MAR). Although the MAR is shown as part of the CPU, in some applications it may be part of the memory.

An Am2902 High-Speed Lookahead Carry Generator is utilized to provide high-speed relative and indexed addressing. In slower systems, the C_{n+4} output can be wired to the next higher C_n input to provide ripple block arithmetic.

The Condition Code input ($\overline{CC}$) is derived from the same condition code multiplexer which generates the condition code input for the microprogram sequencer.

The control inputs of the Am2930 (I_{0-4}, $\overline{IEN}$, $\overline{RE}$, $\overline{OE}$, and C_i and C_n of the least significant device) are shown originating at the Pipeline Register. Although it is not shown in Figure 1, it is possible to share the Pipeline Register outputs which go to these pins with another device. This can be accomplished if both the Am2930 and the other device do not operate on the same microcycle. Forcing the $\overline{IEN}$ input HIGH inhibits any changes in the Am2930 internal registers, independent of the state of these seven inputs. This allows the Am2930 to be placed in a hold mode while the other device is using the same Pipeline Register outputs as control signals.

PIN DEFINITIONS

I_{0-4} The five Instruction control lines to the Am2930, used to establish data paths and enable internal registers.

$\overline{IEN}$ The Instruction Enable Input, used to enable and disable internal registers. When $\overline{IEN}$ is LOW, all internal registers are under control of the Instruction inputs. When $\overline{IEN}$ is HIGH, all internal registers except R are inhibited from changing state. R is controlled by the $\overline{RE}$ input. The $\overline{IEN}$ input does not affect the combinatorial data paths and the outputs established by the Instruction inputs.

$\overline{CC}$ The Condition Code input determines whether or not a conditional instruction (Instructions 16-31) is performed. If $\overline{CC}$ is LOW, the conditional instruction is executed. If $\overline{CC}$ is HIGH, Fetch PC (Instruction 1) is executed. The $\overline{CC}$ input may be either HIGH or LOW for unconditional instructions (Instructions 0-15).

$\overline{RE}$ The Register Enable input for the Auxiliary Register (R). A LOW on $\overline{RE}$ causes the Auxiliary Register (R) to be loaded from the D inputs unless Instruction 8 or 9 is being executed and $\overline{IEN}$ is LOW.

C_n The carry-in to the Full Adder.

C_{n+4} The carry-out of the Full Adder.

$\overline{P}$, $\overline{G}$ The carry generate and propagate outputs of the Full Adder.

C_i The carry-in to the program counter incrementer.

C_{i+4} The carry-out of the program counter incrementer.

Y_{0-3} The four address outputs of the Am2930. These are three-state output lines. When enabled, they display the outputs of the Full Adder.

$\overline{OE}$ Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF (high-impedance); when $\overline{OE}$ is LOW, the Y outputs are active (HIGH or LOW).

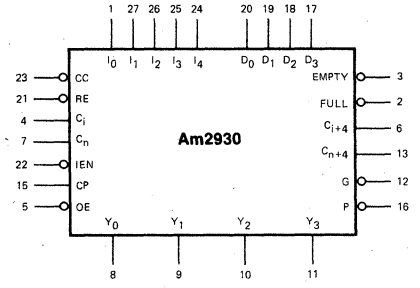
D_{0-3} The four Direct inputs which are used as inputs to the Auxiliary Register, the RAM, and the Full Adder, under instruction control.

$\overline{Empty}$ The Empty output is LOW when the Stack is empty.

$\overline{Full}$ The Full output is LOW when the LIFO stack is full – during and after the 17th push operation.

CP The clock input to the Am2930. All internal registers (R, SP, PC) and the RAM are updated on the LOW-to-HIGH transition of the clock input.

LOGIC SYMBOL (DIP)



V_{CC} = Pin 28
GND = Pin 14

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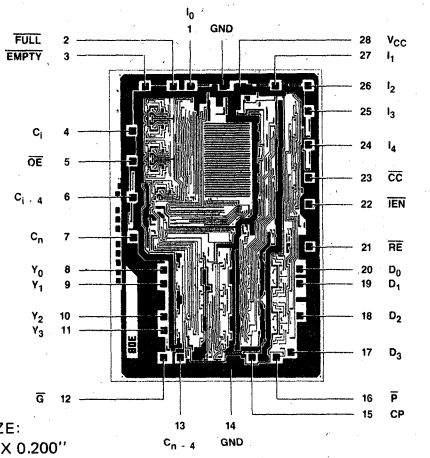
METALLIZATION AND PAD LAYOUT



DIE SIZE:
0.133" X 0.200"

Pad numbers correspond to DIP pinout.

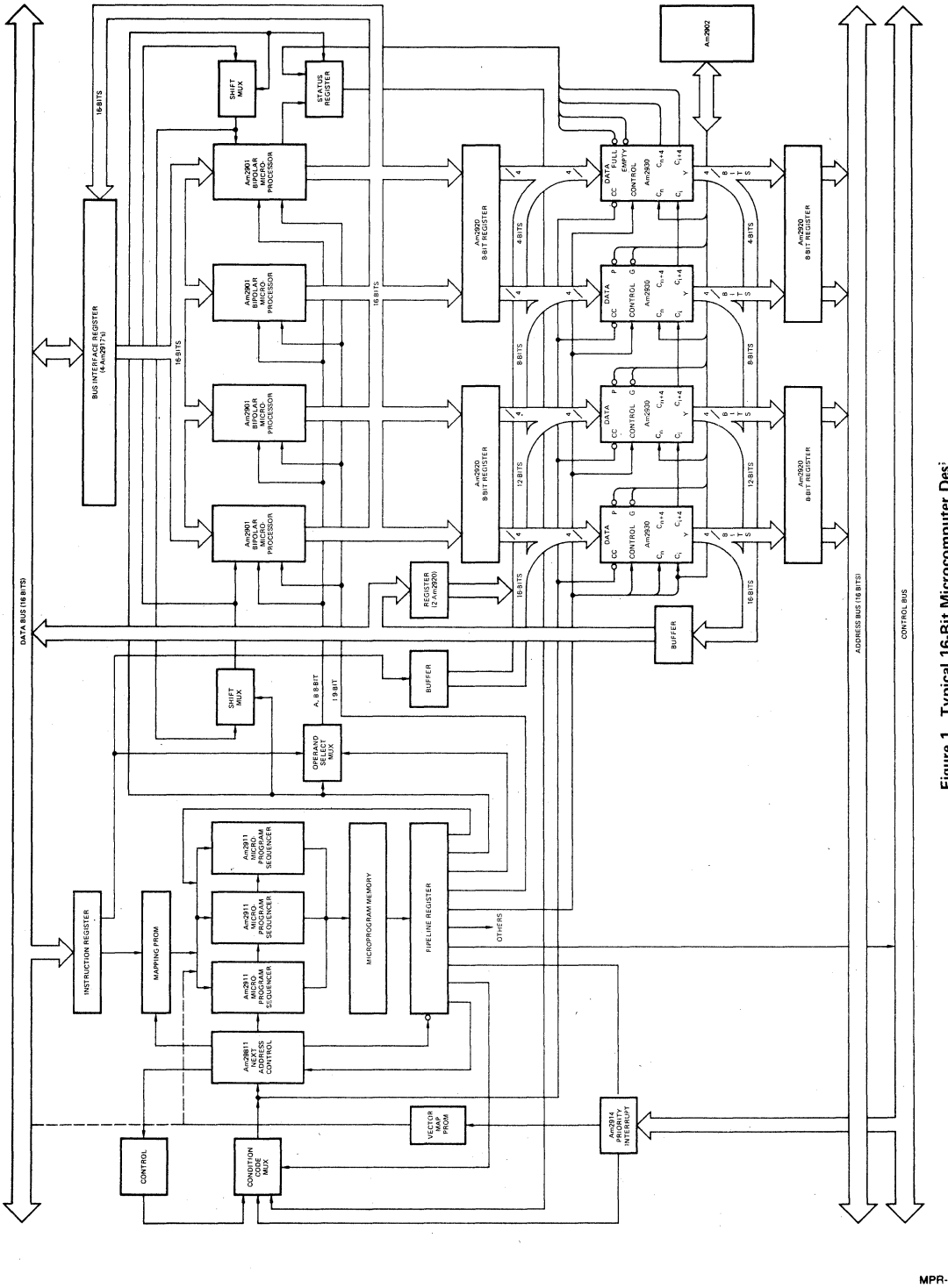


Figure 1. Typical 16-Bit Microcomputer Des

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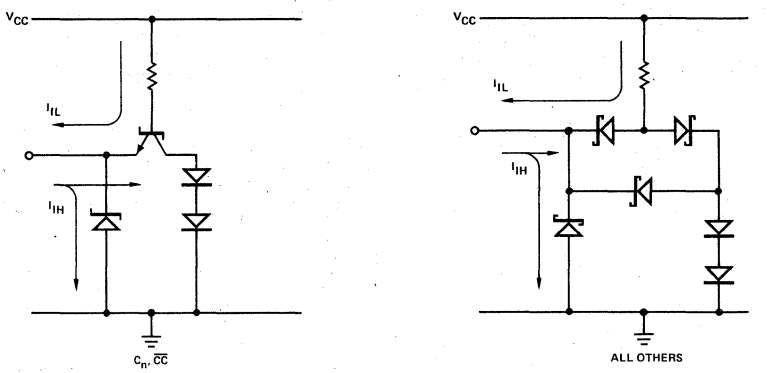
INPUT/OUTPUT CIRCUIT CURRENT INTERFACE

DRIVEN INPUTS



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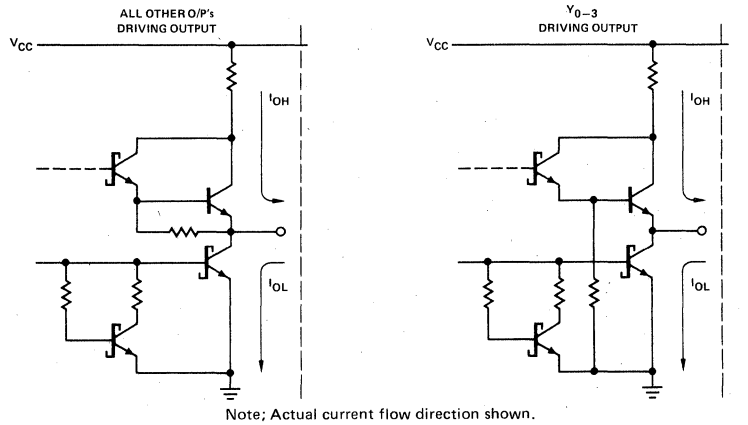
Note; C_i input is connected to both configurations in parallel.

DRIVING OUTPUTS



Note; Actual current flow direction shown.

MPR-224

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2930DC	D-28	C	C-1
AM2930DC-B	D-28	C	B-2 (Note 4)
AM2930DM	D-28	M	C-3
AM2930DM-B	D-28	M	B-3
AM2930FM	F-28-2	M	C-3
AM2930FM-B	F-28-2	M	B-3
AM2930CLC	L-28-1	C	C-1
AM2930CLM	L-28-1	M	C-3
AM2930CLM-B	L-28-1	M	B-3
AM2930XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2930XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat-Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

Am2932

Program Control Unit/Push-Pop Stack

DISTINCTIVE CHARACTERISTICS

- Powerful, 4-bit slice address controller for memories
  Useful with both main memory and microprogram memory
  Expandable to generate any address length
- Executes 16 instructions
  Automatic generation of address and update of program counter for fetch cycles, branch cycles, and subroutine call and return
- Contains cascadable full adder
  Eight relative address instructions are provided, including jump relative and jump-to-subroutine relative
- Seventeen-level push/pop stack
  On-chip storage of subroutine return addresses nested up to 17 levels deep
- Separate incrementer for program counter
  A relative address may be computed and PC may be incremented by one on a single cycle

GENERAL DESCRIPTION

The Am2932 is a four-bit wide Program Control Unit intended to perform machine level addressing functions, although the device can also be used as a microprogram sequencer. Four Am2932s may be interconnected to generate a 16-bit address (64K words). The Am2932 contains a program counter, a subroutine stack, an auxiliary register, and a full adder for computing relative addresses.

The Am2932 performs five types of instructions. These are: 1) Fetch; 2) Jump; 3) Jump-to-Subroutine; 4) Return-from-Subroutine; and 5) miscellaneous instructions.

There are four sources of data for the adder which generates the Address outputs (Y_0-Y_3). These are: 1) the Program Counter(PC); 2) the Stack (S); 3) the auxiliary Register(R); and 4) the Direct inputs (D). Under control of the Instruction inputs (I_0-I_3), the multiplexers at the adder inputs allow various combinations of these terms to be generated at the three-state Y address outputs. The instruction lines also control the updating of the program counter and the auxiliary register.

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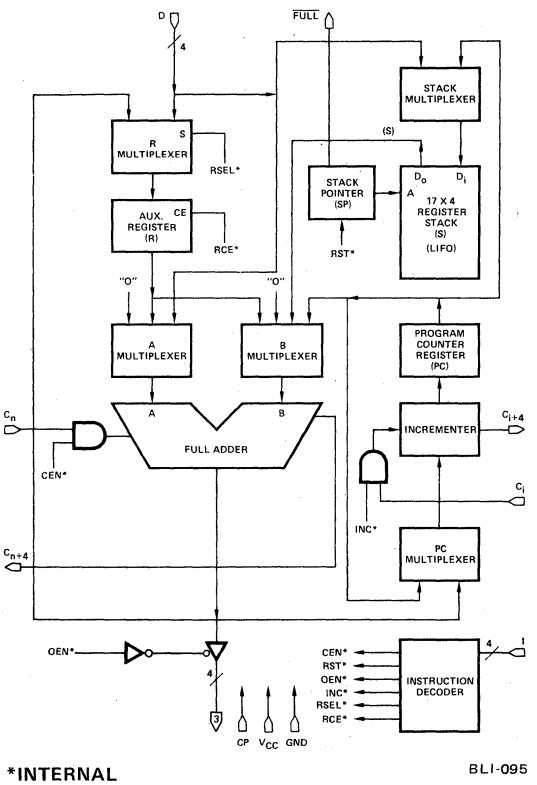
RELATED PRODUCTS

Part No.	Description
Am2902A	Carry Look-Ahead Generator
Am2904	Status and Shift Control Unit
Am2920	8-Bit Register
Am2922	Condition Code MUX

For applications information, see Chapter V of **Bit Slice Microprocessor Design**, Mick & Brick, McGraw Hill Publications.

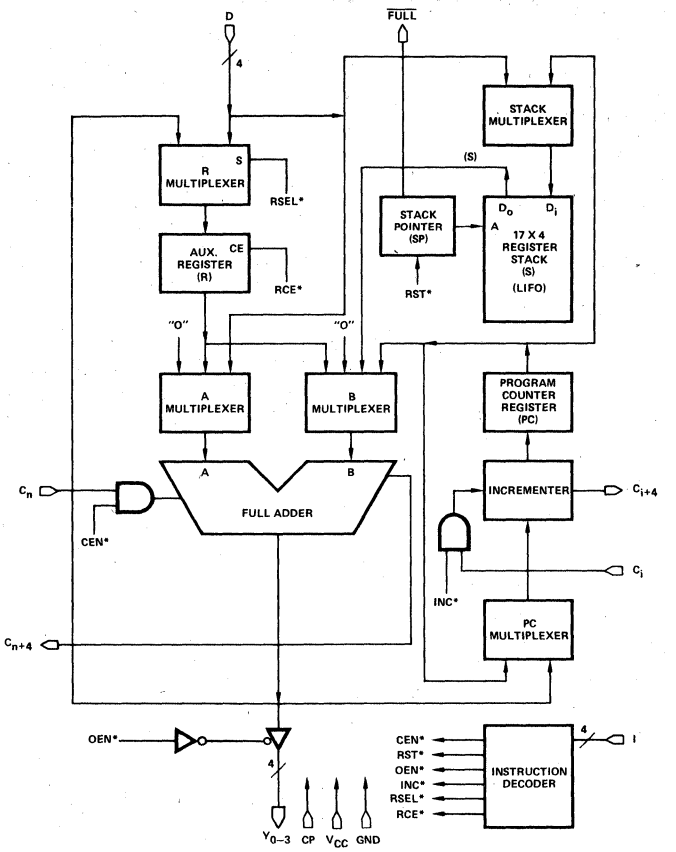
BLOCK DIAGRAM



*INTERNAL

BLI-095

BLOCK DIAGRAM

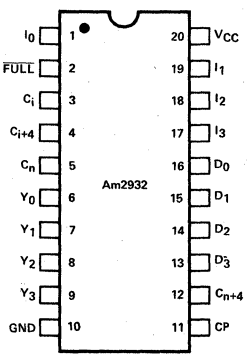


*INTERNAL

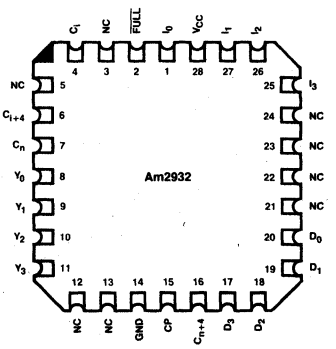
BLI-096

CONNECTION DIAGRAMS – Top Views

D-20



L-28-1



BLI-097

Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max.
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

OPERATING RANGE

Part Number	Temperature	V_{CC}
Am2932DC	T_A = 0 to 70°C	4.75V to 5.25V
Am2932DM	T_C = −55 to +125°C	4.50V to 5.50V

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DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IL} or V_{IH}	Y_0, Y_1, Y_2, Y_3 C_{n+4} C_{i+4}	I_{OH} = −1.6mA	2.4			Volts
			$\overline{FULL}$	I_{OH} = −1.2mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IL} or V_{IH}	Y_0, Y_1, Y_2, Y_3	I_{OL} = 20mA (COM'L)			0.5	Volts
				I_{OL} = 16mA (MIL)			0.5	
			C_{n+4}, C_{i+4}	I_{OL} = 16mA			0.5	
			$\overline{FULL}$	I_{OL} = 12mA			0.5	
V_{IH}	Input HIGH Level (Note 4)				2.0			Volts
V_{IL}	Input LOW Level (Note 4)						0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V	D_{0-3}				−.360	mA
			I_{0-3}, CP				−.702	
			C_i				−2.0	
			C_n				−3.69	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	D_{0-3}				20	μA
			I_{0-3}, CP				40	
			C_i				90	
			C_n				250	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−30		−85	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX., $\overline{OE}$ = 2.4V	Y_{0-3}	V_{OUT} = 0.5V			−50	μA
I_{OZH}				V_{OUT} = 2.4V			50	
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX.		T_A = 25°C		128	176	mA
				T_C = −55 to +125°C			210	
				T_C = +125°C			145	
				T_A = 0 to 70°C			190	
				T_A = 70°C			160	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should only be tested in a static-, noise-free environment.
5. Minimum I_{CC} is at maximum temperature.

Am2932 SWITCHING CHARACTERISTICS

Tables A, B, C and D define the timing characteristics of the Am2932. Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level.

I. GUARANTEED PERFORMANCE OVER COMMERCIAL OPERATING RANGE.

V_{CC} = 4.75 to 5.25V, T_A = 0 to +70°C

TABLE IA
Clock Characteristics.

Minimum Clock LOW Time	31ns
Minimum Clock HIGH Time	33ns

TABLE IB
Output Enable/Disable Times.
All in ns.
C_L = 5.0pF for output disable tests.

From	To	Enable	Disable
I_{3-0}	Y	80	55

TABLE IC
Combinational Propagation Delays.
All in ns.
Outputs fully loaded. C_L = 50pF.

From Input \ To Output	Y	C_{n+4}	C_{i+4} (Note 1)	C_{i+4} (Note 2)	$\overline{Full}$
I_{3-0}	81	77	91	80	69
C_n	32	25	45	–	–
C_i	–	–	22	22	–
CP	69	61	78	43	55
D	39	–	50	–	–

TABLE ID
Set-up and Hold Times. All in ns.
All relative to clock LOW-to-HIGH transition.

Input	CP: Set-up Time	Hold Time
C_n	43	0
C_i	32	5
D	52	2
I_{3-0}	114	0

Notes: 1. Instructions 5, 7, 11, 12, 13, 14.
2. All instructions except 5, 7, 11, 12, 13, 14.

II. GUARANTEED PERFORMANCE OVER MILITARY OPERATING RANGE.

V_{CC} = 4.5 to 5.5V, T_C = −55 to +125°C

TABLE IIA
Clock Characteristics.

Minimum Clock LOW Time	35ns
Minimum Clock HIGH Time	35ns

TABLE IIB
Output Enable/Disable Times.
All in ns.
C_L = 5.0pF for output disable tests.

From	To	Enable	Disable
I_{3-0}	Y	85	60

TABLE IIC
Combinational Propagation Delays.
All in ns.
Outputs fully loaded. C_L = 50pF.

From Input \ To Output	Y	C_{n+4}	C_{i+4} (Note 1)	C_{i+4} (Note 2)	$\overline{Full}$
I_{3-0}	88	82	97	87	78
C_n	37	30	46	–	–
C_i	–	–	23	23	–
CP	74	66	84	45	60
D	44	–	55	–	–

TABLE IID
Set-up and Hold Times. All in ns.
All relative to clock LOW-to-HIGH transition.

Input	CP: Set-up Time	Hold Time
C_n	52	0
C_i	37	5
D	60	2
I_{3-0}	124	0

Notes: 1. Instructions 5, 7, 11, 12, 13, 14.
2. All instructions except 5, 7, 11, 12, 13, 14.

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5−8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

ARCHITECTURE OF THE Am2932

The Am2932 is a bipolar Program Control Unit intended for use in high-speed microprocessor applications. The device is a cascadable, four-bit slice such that three devices allow addressing of up to 4K words of memory and four devices allow addressing of up to 64K words of memory.

As shown in the Block Diagram, the device consists of the following:

1) A full adder with input multiplexers
2) A Program Counter Register with an incrementer and an input multiplexer
3) A 17 x 4 Last-In, First-Out (LIFO) stack consisting of an input multiplexer, a 17 x 4 RAM, and a Stack Pointer
4) An auxiliary register with an input multiplexer
5) An instruction decoder
6) Four 3-state output buffers on the address outputs

The following paragraphs describe each of these blocks in detail.

Full Adder

The Full Adder is a binary device with full lookahead carry logic for high-speed addition. The carry output (C_{n+4}) can be connected to the next higher C_n to provide ripple block arithmetic. The carry input to the adder (C_n) is internally inhibited during those instructions which do not require an addition to be performed. For these instructions, the data is passed directly through the adder, independent of the state of C_n.

The multiplexers at the A and B inputs of the adder are controlled by the Instruction decoder which selects the appropriate adder inputs for the selected instruction.

Program Counter

The program counter consists of a register preceded by an incrementer. The Program Counter Register (PC) is a four-bit, edge-triggered, D-type register which is loaded from the incrementer output on the LOW-to-HIGH transition of the clock input (CP) at the end of every instruction.

The incrementer utilizes full lookahead logic for high speed. For cascading devices, the carry output of the incrementer (C_{i+4}) is connected to the incrementer carry input (C_i) of the next higher device. The output of the incrementer, which is loaded into the PC, is equal to the incrementer input plus C_i. Therefore, it is possible to control the entire cascaded incrementer from the C_i input of the least significant device; a LOW on the C_i input of the least significant device will simply pass the data from the multiplexer output to the inputs of PC; a HIGH will cause the outputs of the multiplexer to be incremented before they are loaded into PC. During the suspend instruction the C_i input is internally inhibited; therefore, data is passed from the multiplexer output to the PC without incrementing. The multiplexer selects the input to the incrementer from either PC or the output of the Full Adder, depending upon the instruction being executed. During the Jump, Jump-to-Subroutine, and Return instructions, the multiplexer chooses the Full Adder outputs as the input to the incrementer. The Full Adder output is also selected for the Reset instruction. For all other instructions, the PC is selected as the input to the incrementer.

17 x 4 LIFO Stack

The 17 x 4 LIFO stack consists of a multiplexer, a 17 x 4 RAM, and a Stack Pointer (SP) which address the words in the RAM.

The SP always points to the last word written into the RAM (Top of the Stack). The Top of the Stack (S) is available at the output of the RAM.

Data is pushed onto the Top of the Stack from either D or PC. It is written into memory location SP+1. The SP is incremented on the LOW-to-HIGH clock transition at the end of the cycle so that it still points to the last data written into the RAM.

For a Pop operation, the contents of the RAM are not changed, but the SP is decremented at the end of the cycle so that it then points to the new Top of the Stack.

The SP is an up/down counter which changes state on the LOW-to-HIGH transition of the Clock input. It is internally prevented from incrementing when the stack is full and from decrementing when the Stack is empty. When the Stack is full, the RAM write circuitry is also inhibited.

The active LOW Full output ($\overline{FULL}$) is LOW either when the stack is full or when the current instruction being executed will fill the stack (during and after the 17th Push).

Auxiliary Register (R)

The Auxiliary Register (R) can be loaded from either the Direct inputs (D) or the output of the Full Adder. It is loaded on the LOW-to-HIGH transition of the clock input (CP) if the Instruction inputs call for it to be loaded.

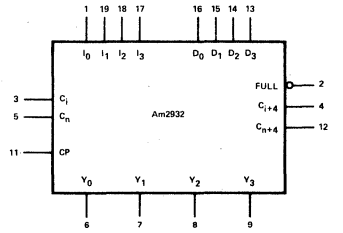
Instruction Decoder

The Instruction Decoder generates the signals necessary to establish the data paths and to enable the loading of the PC, R, SP, and RAM.

Output Buffers

The Address outputs (Y_0-Y_3) are three-state drivers which may be disabled under Instruction control.

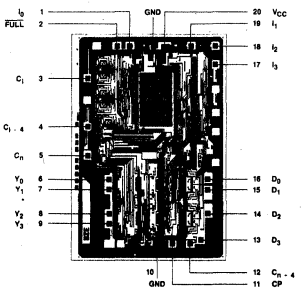
LOGIC SYMBOL (DIP)



V_{CC} = Pin 20
GND = Pin 10

BLI-094

METALLIZATION AND PAD LAYOUT



DIE SIZE:
0.134" X 0.200"

Pad numbers correspond to DIP pinout.

TABLE I – Am2932 INSTRUCTION SET

Instruction Number	I_3	I_2	I_1	I_0	Mnemonic	Instruction	Y_0-Y_3	Next State (after CP↑) – Note 2			
								PC	R	RAM	SP
0	L	L	L	L	PRST	RESET	"0"	"0"+C_i	–	–	Reset
1	L	L	L	H	PSUS	SUSPEND	Z (Note 1)	–	–	–	–
2	L	L	H	L	PSHD	PUSH D	PC	PC+C_i	–	D→Loc SP+1	SP+1
3	L	L	H	H	POPS	POP S	S	PC+C_i	–	–	SP–1
4	L	H	L	L	FPC	FETCH PC	PC	PC+C_i	–	–	–
5	L	H	L	H	JMPD	JUMP D	D	D+C_i	–	–	–
6	L	H	H	L	PSHP	PUSH PC	PC	PC+C_i	–	PC→Loc SP+1	SP+1
7	L	H	H	H	RTS	RETURN S	S	S+C_i	–	–	SP–1
8	H	L	L	L	FR	FETCH R	R	PC+C_i	–	–	–
9	H	L	L	H	FPR	FETCH PC+R	PC+R+C_n	PC+C_i	–	–	–
10	H	L	H	L	FPLR	FETCH PC→R	PC	PC+C_i	PC	–	–
11	H	L	H	H	JMPR	JUMP R	R	R+C_i	–	–	–
12	H	H	L	L	JPPR	JUMP PC+R	PC+R+C_n	PC+R+C_n+C_i	–	–	–
13	H	H	L	H	JSBR	JSB R	R	R+C_i	–	PC→Loc SP+1	SP+1
14	H	H	H	L	JSPR	JSB PC+R	PC+R+C_n	PC+R+C_n+C_i	–	PC→Loc SP+1	SP+1
15	H	H	H	H	PLDR	LOAD R	PC	PC+C_i	D	–	–

Notes: 1. Z = High impedance state (outputs "OFF").
2. – = No change.

PC – Program Counter
R – Auxiliary Register
S – Stack Top
SP – Stack Pointer
D – Direct Inputs

Am2932 INSTRUCTION SET

The Am2932 Instruction set can be divided into five types of instructions. These are:

- Fetches
- Jumps
- Jumps-to-Subroutine
- Return-from-Subroutine
- Miscellaneous Instructions

The following paragraphs describe each of these types in detail.

Fetches

As can be seen from Table I, there are four Fetch instructions (Instructions 4, 8, 9, 10). Under control of the Instructions inputs, the desired value is placed at the Y outputs. For all Fetch instructions, PC is incremented if C_i of the least significant device is HIGH. For Instruction 10 R is loaded with PC. The RAM and Stack Pointer are not changed during a Fetch instruction.

Jumps

There are three Jump instructions (Instructions 5, 11, 12). Under control of the Instruction inputs, the desired value is placed at the Y outputs. Additionally, the value is incremented if C_i of the least significant device is HIGH and loaded into PC. The RAM, Stack Pointer and R are not changed during these instructions.

Jumps-to-Subroutine

There are two Jump-to-Subroutine instructions (Instructions 13 and 14). Under control of the Instruction inputs, the desired value is placed on the Y outputs. On the rising edge of the clock the value is incremented* and loaded into PC, PC is loaded into the RAM at location SP+1; and SP is incremented.

During these instructions, R is not changed.

Return-from-Subroutine (Instruction 7)

Under control of the instruction inputs, S is placed at the Y outputs. Additionally, the value of S is incremented* and loaded into PC and SP is decremented at the end of the cycle (on the rising edge of the clock).

During this instruction, R is not changed.

Miscellaneous Instructions

Each of the nine miscellaneous instructions is described individually.

Reset (Instruction 0)

The Reset instruction forces the Y outputs to zero, loads either zero or one into PC, depending upon the C_i input of the least significant device, and resets SP. The RAM and R are unchanged.

Load R (Instruction 15)

This instruction loads the data on the D inputs into R. PC is either incremented or held depending upon C_i of the least significant device. The SP and RAM are not changed.

Push PC (Instruction 6)

This instruction is the same as Fetch PC except that PC is loaded into RAM and SP is incremented at the end of the cycle; i.e., the current PC is Pushed onto the stack.

Push D (Instruction 2)

This instruction is the same as Fetch PC except that D is loaded into the RAM and SP is incremented at the end of the cycle; i.e., external data is Pushed onto the stack.

Pop S (Instruction 3)

This instruction places the Top of the Stack (S) at the Y outputs and decrements SP at the end of the cycle. The PC is incremented if the C_i input of the least significant device is HIGH. R is not changed.

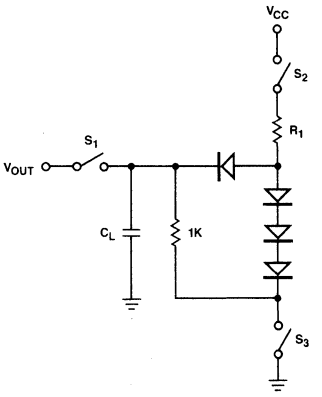
Suspend (Instruction 1)

The Suspend instruction inhibits any change in PC, SP, R and RAM and forces the Y outputs into the high impedance state.

*If C_i of the least significant device is HIGH.

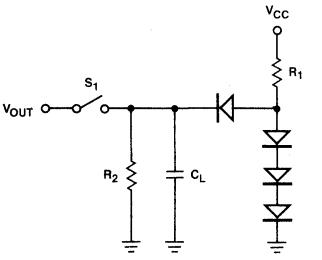
TEST OUTPUT LOAD CONFIGURATIONS FOR Am2932

A. THREE STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2932

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
2	$\overline{FULL}$	B	300	2K
4	C_{i+4}	B	240	1.5K
6-9	Y_{0-3}	A	240	1K
12	C_{n+4}	B	240	1.5K

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

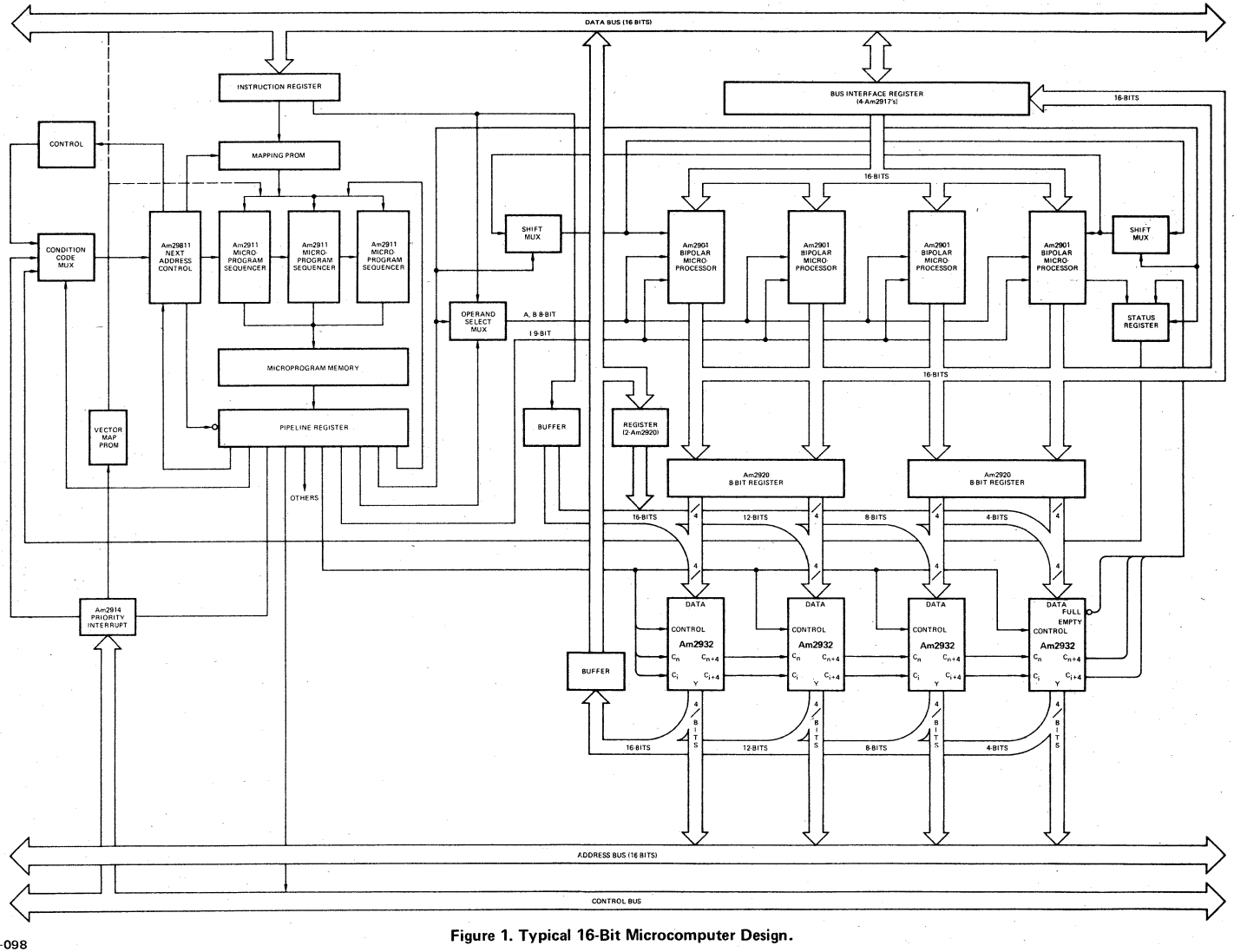


Figure 1. Typical 16-Bit Microcomputer Design.

BLI-098

APPLICATIONS

The Am2932 is shown in a typical 16-bit, 2900 Microcomputer design in Figure 1.

The Direct inputs (D) of the Am2932 are derived from one of three sources: the Instruction Register, the Data Bus via a 16-bit register (two Am2920 8-bit Registers), and the output of the Am2901s via a 16-bit register.

The Address outputs (Y) of the Am2932 are passed to the address bus.

The C_{n+4} output can be wired to the next higher C_n input to provide ripple block arithmetic.

The control inputs of the Am2932 (I_{0-3}, C_i and C_n of the least significant device) are shown originating at the Pipeline Register.

PIN DEFINITIONS

I_{0-3} The four Instruction control lines to the Am2932, used to establish data paths and enable internal registers.

C_n The carry-in to the Full Adder.

C_{n+4} The carry-out of the Full Adder.

C_i The carry-in to the program counter incrementer.

C_{i+4} The carry-out of the program counter incrementer.

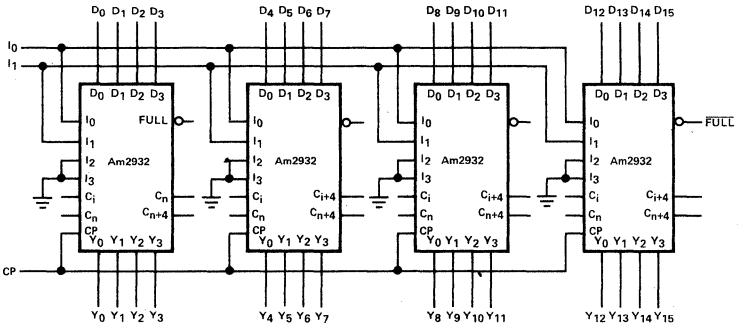
Y_{0-3} The four address outputs of the Am2932. These are three-state output lines. When enabled, they display the outputs of the Full Adder.

D_{0-3} The four Direct inputs which are used as inputs to the Auxiliary Register, the RAM, and the Full Adder, under instruction control.

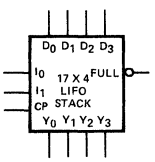
$\overline{Full}$ The Full output is LOW when the LIFO stack is full – during and after the 17th push operation.

CP The clock input to the Am2932. All internal registers (R, SP, PC) and the RAM are updated on the LOW-to-HIGH transition of the clock input.

5



I_1	I_0	INSTRUCTION	Y OUTPUTS
L	L	RESET	"0"
L	H	SUSPEND	Z (HIGH IMPEDANCE)
H	L	PUSH D	SEE NOTE 1
H	H	POP S	TOP OF STACK



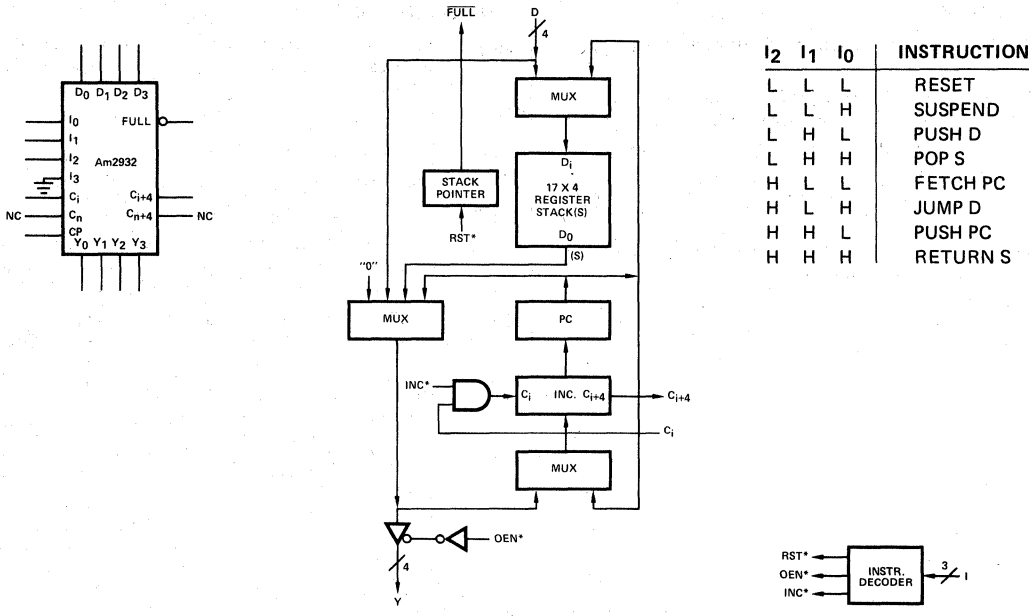
BLI-099

Equivalent Logic Symbol for Am2932 with I_2, I_3 Grounded

Figure shows the use of four Am2932s as a 17-word by 16-bit LIFO stack by grounding I_2 and I_3. The effect of grounding I_3 is shown in Figure 3.

Note 1. During this instruction, PC is placed on the Y outputs. If C_i is held LOW, the Y outputs will be LOW for this instruction after the device is initialized with a Reset instruction.

Figure 2. Application of Four Am2932s as a 17-Word by 16-Bit LIFO Stack.



I_2	I_1	I_0	INSTRUCTION
L	L	L	RESET
L	L	H	SUSPEND
L	H	L	PUSH D
L	H	H	POP S
H	L	L	FETCH PC
H	L	H	JUMP D
H	H	L	PUSH PC
H	H	H	RETURN S

Figure 3. Equivalent Circuit of Am2932 with I_3 Grounded.

BLI-100

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2932DC	D-20	C	C-1
AM2932DC-B	D-20	C	B-2 (Note 4)
AM2932DM	D-20	M	C-3
AM2932DM-B	D-20	M	B-3
AM2932LC	L-28-2	C	C-1
AM2932LM	L-28-2	M	C-3
AM2932LM-B	L-28-2	M	B-3
AM2932XC	Dice	C	Visual inspection to MIL-STD-883. Method 2010B.
AM2932XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat-Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

Am2940
DMA Address Generator

DISTINCTIVE CHARACTERISTICS

- DMA Address Generation
  Generates memory address, word count and DONE signal for DMA transfer operation.
- Expandable Eight-bit Slice
  Any number of Am2940's can be cascaded to form larger memory addresses – three devices address 16 megawords.
- Repeat Data Transfer Capability
  Initial memory address and word count are saved so that the data transfer can be repeated.
- Programmable Control Modes
  Provides four types of DMA transfer control plus memory address increment/decrement.
- High Speed, Bipolar LSI
  Advanced Low-Power Schottky TTL technology provides typical CLOCK to DONE propagation delay of 50ns and 24mA output current sink capability.
- Microprogrammable
  Executes 8 different instructions.

GENERAL DESCRIPTION

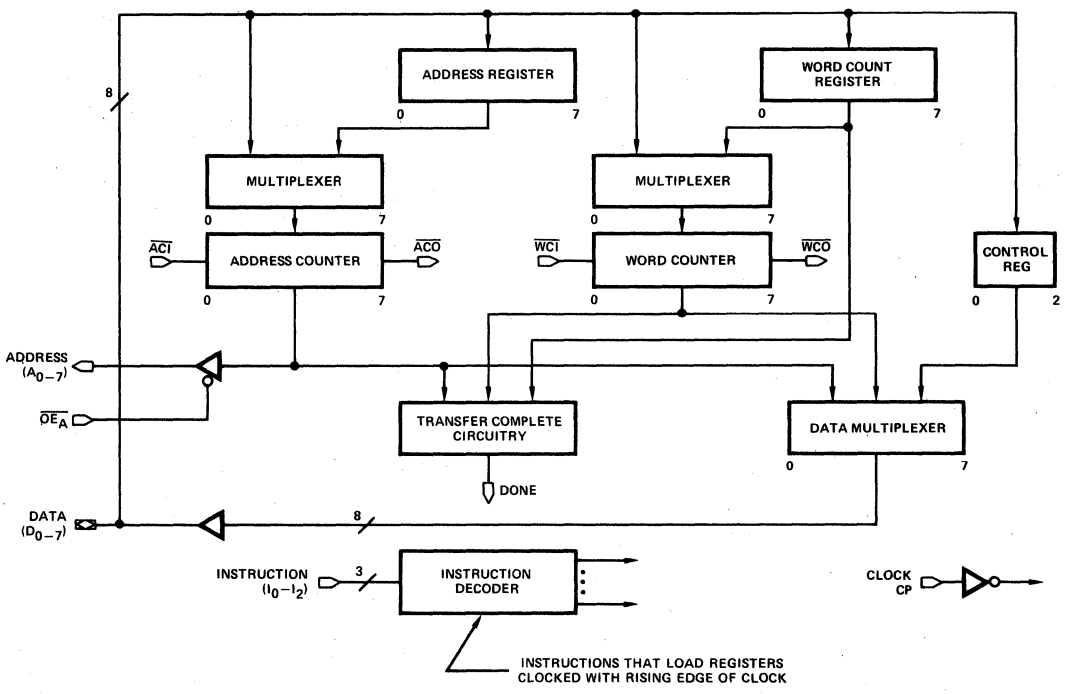
The Am2940, a 28-pin member of Advanced Micro Devices Am2900 family of Low-Power Schottky bipolar LSI chips, is a high-speed, cascadable, eight-bit wide Direct Memory Access Address Generator slice. Any number of Am2940's can be cascaded to form larger addresses.

The primary function of the device is to generate sequential memory addresses for use in the sequential transfer of data to or from a memory. It also maintains a data word count and generates a DONE signal when a programmable terminal count has been reached. The device is designed for use in peripheral controllers with DMA capability or in any other system which transfers data to or from sequential locations of a memory.

The Am2940 can be programmed to increment or decrement the memory address in any of four control modes, and executes eight different instructions. The initial address and word count are saved internally by the Am2940 so that they can be restored later in order to repeat the data transfer operation.

5

BLOCK DIAGRAM



For applications information see the last part of this data sheet and chapter VII of *Bit Slice Microprocessor Design*, by Mick and Brick, McGraw-Hill Publishers.

Am2940 DMA Address Generator MPR-226

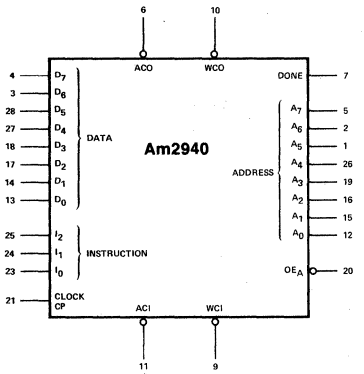
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

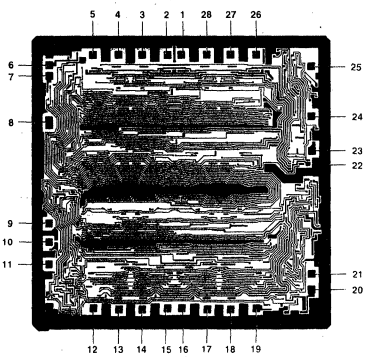
Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2940DC	D-28	C	C-1
AM2940DC-B	D-28	C	B-2 (Note 4)
AM2940DM	D-28	M	C-3
AM2940DM-B	D-28	M	B-3
AM2940FM	F-28-2	M	C-3
AM2940FM-B	F-28-2	M	B-3
AM2940LC	L-28	C	C-1
AM2940LM	L-28	M	C-3
AM2940LM-B	L-28	M	B-3
AM2940XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2940XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V. M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

LOGIC SYMBOL



METALLIZATION AND PAD LAYOUT

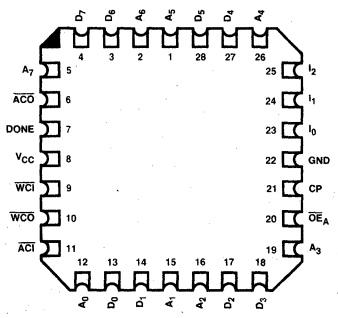


Note: Numbers refer to DIP pin connections.

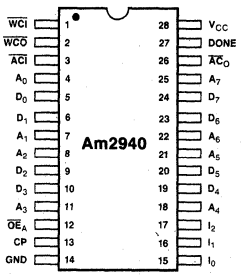
DIE SIZE: 0.178" X 0.181"

CONNECTION DIAGRAMS – Top Views

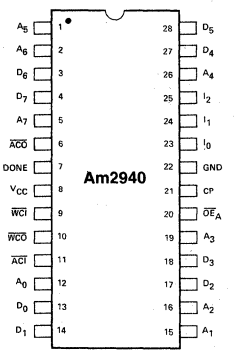
Chip-Pak™ L-28



F-28-2



D-28



Note: Pin 1 is marked for orientation

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

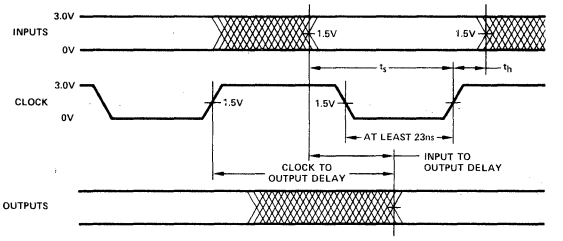
OPERATING RANGE

P/N	Range	Temperature	V_{CC}	
Am2940DC	COM'L	T_A = 0 to +70°C	V_{CC} = 5.0V ±5%	(MIN. = 4.75V MAX. = 5.25V)
Am2940DM, FM	MIL	T_C = −55 to +125°C	V_{CC} = 5.0V ±10%	(MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}		MIL I_{OH} = −1.0mA COM'L I_{OH} = −2.6mA	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL} (Note 5)	WCO, ACO	MIL I_{OL} = 8.0mA COM'L I_{OL} = 12mA			0.5	Volts
			A_{0-7}, D_{0-7} DONE	MIL I_{OL} = 16mA COM'L I_{OL} = 24mA				
V_{IH}	Input HIGH Level (Note 4)	Guaranteed Input Logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Note 4)	Guaranteed Input Logical LOW voltage for all inputs					0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V		D_{0-7} All Others			−0.15 −0.8	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V		D_{0-7} All Others			150 40	µA
I_{CEX}	Output Leakage on DONE	V_{CC} = MAX., V_O = 5.5V					250	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX. + 0.5V, V_O = 0.5V			−30		−85	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX. $\overline{OE}$ = 2.4V	V_{OUT} = 0.5V	A_{0-7} D_{0-7}			−50 −150	µA
I_{OZH}			V_{OUT} = 2.4V	A_{0-7} D_{0-7}			50 150	
I_{CC}	Power Supply Current	V_{CC} = MAX.		T_A = 25°C		170	275	mA
			Am2940DC	T_A = 0°C to +70°C			290	
				T_A = +70°C			235	
			Am2940DM, FM	T_C = −55°C to +125°C			315	
				T_C = +125°C			225	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should only be static tested in a noise-free environment (not functionally tested).
5. I_{OL} limit on A_i and D_i (i = 0 to 7) applies to either output individually, but not both at the same time. The sum of the loading on A_i plus D_i is limited to 24mA MIL or 32mA COM'L.



See Tables A for t_s and t_h for various inputs. See Tables B for combinational delays from clock and other inputs to outputs.

Figure 2. Switching Waveforms.

MPR-728

SWITCHING CHARACTERISTICS

The tables below define the Am2940 switching characteristics. Tables A are set-up and hold times relative to the clock LOW-to-HIGH transition. Tables B are combinational delays. Tables C are clock requirements. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns with C_L = 50pF except output disable times ($\overline{OE}$ to A and I to D) which are specified or a 5pF load. All times are in ns.

I. GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

Am2940DC (T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	24	4
I_{012}	46	5
$\overline{ACI}$	30	4
$\overline{WCI}$ (Note 1)	30	3

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	A_{0-7}	DONE	D_{0-7}
$\overline{ACI}$	20	–	–	–	–
$\overline{WCI}$ (Note 2)	–	20	–	46	–
I_{0-2}	–	–	–	–	37
CP (Note 3)	58	58	54	85	–

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	34	ns
Maximum Clock Frequency	17	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
I_{012}	D_{0-7}	35	35	ns
$\overline{OE}$	A_{0-7}	25	25	ns

II. GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

Am2940DM, FM (T_C = −55 to +125°C, V_{CC} = 4.5 to 5.5V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	27	6
I_{012}	49	5
$\overline{ACI}$	34	5
$\overline{WCI}$ (Note 1)	34	5

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	A_{0-7}	DONE	D_{0-7}
$\overline{ACI}$	21	–	–	–	–
$\overline{WCI}$ (Note 2)	–	21	–	54	–
I_0-I_2	–	–	–	–	41
CP (Note 3)	64	64	62	88	–

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	35	ns
Maximum Clock Frequency	16	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
I_{012}	D_{0-7}	42	42	ns
$\overline{OE}$	A_{0-7}	30	30	ns

Notes: 1. Control modes 0, 1, and 3 only.
2. $\overline{WCI}$ to Done occurs only in control modes 0 and 1.
3. CP to Done occurs only in control modes 0, 1, and 2.

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful.

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5-8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100's of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

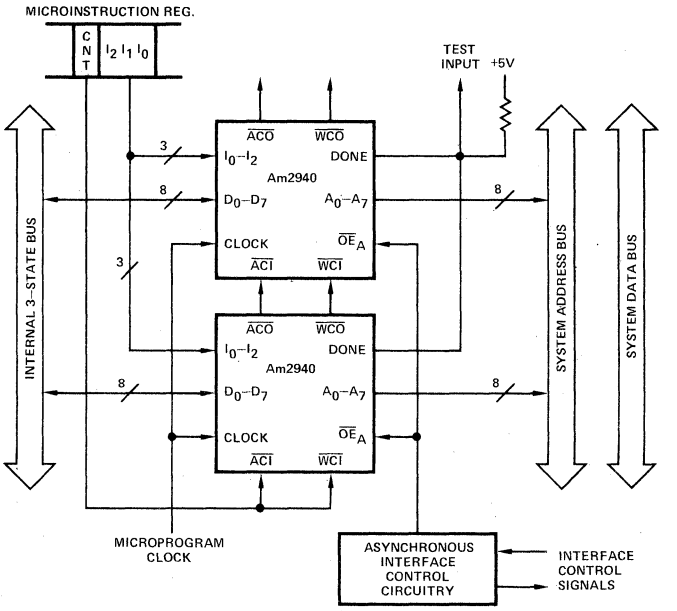


Figure 4. Am2940 Interconnections.

Am2940 ARCHITECTURE

As shown in the Block Diagram, the Am2940 consists of the following:

- A three-bit Control Register.
- An eight-bit Address Counter with input multiplexer.
- An eight-bit Address Register.
- An eight-bit Word Counter with input multiplexer.
- An eight-bit Word Count Register.
- Transfer complete circuitry.
- An eight-bit wide data multiplexer with three-state output buffers.
- Three-state address output buffers with external output enable control.
- An instruction decoder.

Control Register

Under instruction control, the Control Register can be loaded or read from the bidirectional DATA lines D_0-D_7. Control Register bits 0 and 1 determine the Am2940 Control Mode, and bit 2 determines whether the Address Counter increments or decrements. Figure 1 defines the Control Register format.

Address Counter

The Address Counter, which provides the current memory address, is an eight-bit, binary, up/down counter with full look-ahead carry generation. The Address Carry input ($\overline{ACI}$) and Address Carry Output ($\overline{ACO}$) allow cascading to accommodate larger addresses. Under instruction control, the Address Counter can be enabled, disabled, and loaded from the DATA inputs, D_0-D_7, or the Address Register. When enabled and the $\overline{ACI}$ input is LOW, the Address Counter increments/decrements on the LOW to HIGH transition of the CLOCK input, CP. The Address Counter output can be enabled onto the three-state ADDRESS outputs A_0-A_7 under control of the Output Enable input, $\overline{OE}_A$.

Address Register

The eight-bit Address Register saves the initial address so that it can be restored later in order to repeat a transfer operation. When the LOAD ADDRESS instruction is executed, the Address Register and Address Counter are simultaneously loaded from the DATA inputs, D_0-D_7.

Word Counter and Word Count Register

The Word Counter and Word Count Register, which maintain and save a word count, are similar in structure and operation to the Address Counter and Address Register, with the exception that the Word Counter increments in Control Modes 1 and 3, decrements in Control Mode 0, and is disabled in Control Mode 2. The LOAD WORD COUNT instruction simultaneously loads the Word Counter and Word Count Register.

Transfer Complete Circuitry

The Transfer Complete Circuitry is a combinational logic network which detects the completion of the data transfer operation in three Control Modes and generates the DONE output signal. The DONE signal is a open-collector output, which can be dot-anded between chips.

Data Multiplexer

The Data Multiplexer is an eight-bit wide, 3-input multiplexer which allows the Address Counter, Word Counter, and Control Register to be read at the DATA lines, D_0-D_7. The Data Multiplexer and three-state Data output buffers are instruction controlled.

Address Output Buffers

The three-state Address Output Buffers allow the Address Counter output to be enabled onto the ADDRESS lines, A_0-A_7, under external control. When the Output Enable input, $\overline{OE}_A$, is LOW, the Address output buffers are enabled; when $\overline{OE}_A$ is HIGH, the ADDRESS lines are in the high-impedance state. The address and Data Output Buffers can sink 24mA output current over the commercial operating range.

Instruction Decoder

The Instruction Decoder generates required internal control signals as a function of the INSTRUCTION inputs, I_0-I_2 and Control Register bits 0 and 1.

Clock

The CLOCK input, CP is used to clock the Address Register, Address Counter, Word Count Register, Word Counter, and Control Register, all on the LOW to HIGH transition of the CP signal.

Control Register

CR_2	CR_1	CR_0

CR_1	CR_0	Control Mode Number	Control Mode Type	Word Counter	DONE Output Signal	
					$\overline{WCI}$ = LOW	$\overline{WCI}$ = HIGH
L	L	0	Word Count Equals Zero	Decrement	HIGH when Word Counter = 1	HIGH when Word Counter = 0
L	H	1	Word Count Compare	Increment	HIGH when Word Counter + 1 = Word Count Reg.	HIGH when Word Counter = Word Count Reg.
H	L	2	Address Compare	Hold	HIGH when Word Counter = Address Counter	
H	H	3	Word Counter Carry Out	Increment	Always LOW	

CR_2	Address Counter
L	Increment
H	Decrement

H = HIGH
L = LOW

Figure 1. Control Register Format Definition.

Am2940 CONTROL MODES

Control Mode 0 – Word Count Equals Zero Mode

In this mode, the LOAD WORD COUNT instruction loads the word count into the Word Count Register and Word Counter. When the Word Counter is enabled and the Word Counter Carry-in, WCI, is LOW, the Word Counter decrements on the LOW to HIGH transition of the clock input, CP. Figure 1 specifies when the DONE signal is generated.

Control Mode 1 – Word Count Compare Mode

In this mode the LOAD WORD COUNT instruction loads the word count into the Word Count Register and clears the Word Counter. When the Word Counter is enabled and the Word Counter Carry-in $\overline{WCI}$, is LOW, the Word Counter increments on the LOW to HIGH transition of the clock input, CP. Figure 1 specifies when the DONE signal is generated.

Control Mode 2 – Address Compare Mode

In this mode, only an initial and final memory address need be specified. The initial Memory Address is loaded into the Address Register and Address Counter and the final memory address is loaded into the Word Count Register and Word Counter. The Word Counter is always disabled in this mode and serves as a holding register for the final memory address. When the Address Counter is enabled and the $\overline{ACI}$ input is LOW, the Address Counter increments or decrements (depending on Control Register bit 2) on the LOW to HIGH transition of the CLOCK input, CP. The Transfer Complete Circuitry compares the Address Counter with the Word Counter and generates the DONE signal during the last word transfer, i.e. when the Address Counter equals the Word Counter.

Control Mode 3 – Word Counter Carry Out Mode

For this mode of operation, the user can load the Word Count Register and Word Counter with the two's complement of the number of data words to be transferred. When the Word Counter is enabled and the $\overline{WCI}$ input is LOW, the Word Counter increments on the LOW to HIGH transition of the CLOCK input, CP. A Word Counter Carry Out signal, $\overline{WCO}$, indicates the last data word is being transferred. The DONE signal is not required in this mode and, therefore, is always LOW.

Am2940 INSTRUCTIONS

The Am2940 instruction set consists of eight instructions. Six instructions load and read the Address Counter, Word Counter and Control Register, one instruction enables the Address and Word counters, and one instruction reinitializes the Address and Word Counters. The function of the REINITIALIZE COUNTERS, LOAD WORD COUNT, and ENABLE COUNTERS instructions varies with the Control Mode being utilized. Table 1 defines the Am2940 Instructions as a function of Instruction inputs I_0-I_2 and the four Am2940 Control Modes.

The WRITE CONTROL REGISTER instruction writes DATA input D_0-D_2 into the Control Register; DATA inputs D_3-D_7 are "don't care" inputs for this instruction. The READ CONTROL REGISTER instruction gates the Control Register outputs to DATA lines, D_0-D_2. DATA lines D_3-D_7 are in the HIGH state during this instruction.

The Word Counter can be read using the READ WORD COUNTER instruction, which gates the Word Counter outputs to DATA lines D_0-D_7. The LOAD WORD COUNT instruction is Control Mode dependent. In Control Modes 0, 2, and 3, DATA inputs D_0-D_7 are written into both the Word Count Register and Word Counter. In Control Mode 1, DATA inputs D_0-D_7 are written into the Word Count Register and the Word Counter is cleared.

The READ ADDRESS COUNTER instruction gates the Address Counter outputs to DATA lines D_0-D_7, and the LOAD ADDRESS instruction writes DATA inputs D_0-D_7 into both the Address Register and Address Counter.

In Control Modes 0, 1, and 3, the ENABLE COUNTERS instruction enables both the Address and Word Counters; in Control Mode 2, the Address Counter is enabled and the Word Counter holds its contents. When enabled and the carry input is active, the counters increment on the LOW to HIGH transition of the CLOCK input, CP. Thus, with this instruction applied, counting can be controlled by the carry inputs.

The REINITIALIZE COUNTERS instruction also is Control Mode dependent. In Control Modes 0, 2, and 3, the contents of the Address Register and Word Count Register are transferred to the respective Address Counter and Word Counter; in Control Mode 1, the content of the Address Register is transferred to the Address Counter and the Word Counter is cleared. The REINITIALIZE COUNTERS instruction allows a data transfer operation to be repeated without reloading the address and word count from the DATA lines.

TABLE I. Am2940 INSTRUCTIONS

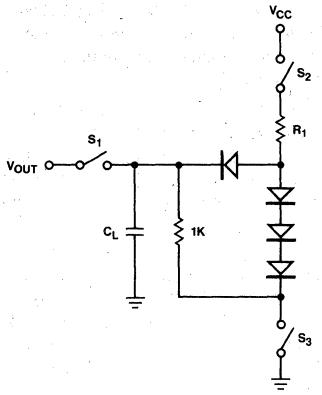
I_2 I_1 I_0	Octal Code	Function	Mnemonic	Control Mode	Word Reg.	Word Counter	Address Reg.	Address Counter	Control Register	Data D_0-D_7
L L L	0	WRITE CONTROL REGISTER	WRCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	D_0-D_2→CR	INPUT
L L H	1	READ CONTROL REGISTER	RDCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	CR→D_0-D_2 (Note 1)
L H L	2	READ WORD COUNTER	RDWC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	WC→D
L H H	3	READ ADDRESS COUNTER	RDAC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	AC→D
H L L	4	REINITIALIZE COUNTERS	REIN	0, 2, 3	HOLD	WCR→WC	HOLD	AR→AC	HOLD	Z
				1	HOLD	ZERO→WC	HOLD	AR→AC	HOLD	Z
H L H	5	LOAD ADDRESS	LDAD	0, 1, 2, 3	HOLD	HOLD	D→AR	D→AC	HOLD	INPUT
H H L	6	LOAD WORD COUNT	LDWC	0, 2, 3	D→WR	D→WC	HOLD	HOLD	HOLD	INPUT
				1	D→WR	ZERO→WC	HOLD	HOLD	HOLD	INPUT
H H H	7	ENABLE COUNTERS	ENCT	0, 1, 3	HOLD	ENABLE COUNT	HOLD	ENABLE COUNT	HOLD	Z
				2	HOLD	HOLD	HOLD	ENABLE COUNT	HOLD	Z

CR = Control Reg.
AR = Address Reg.
AC = Address Counter
WCR = Word Count Reg.
WC = Word Counter
D = Data
L = LOW
H = HIGH
Z = High Impedance

Note 1:
Data Bits D_3-D_7 are high during this instruction.

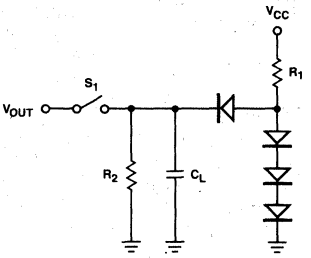
TEST OUTPUT LOAD CONFIGURATIONS FOR Am2940

A. THREE STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

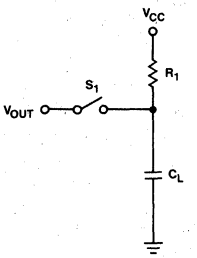
B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

C. OPEN-COLLECTOR OUTPUTS



$$R_1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2940 (DIP)

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
–	A_{0-7}	A	220	1K
–	D_{0-7}	A	220	1K
6	$\overline{ACO}$	B	470	2.4K
7	DONE	C	270	–
10	$\overline{WCO}$	B	470	2.4K

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

APPLICATIONS

The Am2940 is designed for use in peripheral controllers with DMA capability or in any other system which transfers data to or from sequential locations of a memory. One or more Am2940's can be used in each peripheral controller of a distributed DMA system to provide the memory address and word count required for DMA operation.

Figure 3 shows a block diagram of an example microprogrammed DMA peripheral controller. The Am2910 Microprogram Sequencer, Microprogram Memory, and the Microinstruction Register form the microprogram control portion of this peripheral controller. The Am2940 generates the memory address and maintains the word count required for DMA operation. An internal three-state bus provides the communication path between the Microinstruction Register, the Am2917 Data Transceivers, the Am2940, the Am2901A Microprocessor, and the Device Interface Circuitry.

The Am2940 interconnections are shown in detail in Figure 4. Two Am2940's are cascaded to generate a sixteen-bit address. The Am2940 ADDRESS and DATA output current sink capability is 24mA over the commercial operating range. This allows the Am2940's to drive the System Address Bus and Internal Three-State Bus directly, thereby eliminating the need for separate bus drivers. Three-bits in the Microinstruction Register provide the Am2940 Instruction Inputs, I_0-I_2. The microprogram clock is used to clock the Am2940's and, when the ENABLE COUNTERS instruction is applied, address and word counting is controlled by the CNT bit of the Microinstruction Register.

Asynchronous interface control circuitry generates System Bus control signals and enables the Am2940 Address onto the System Address Bus at the appropriate time. The open-collector DONE outputs are dot-anded and used as a test input to the Am2910 Microprogram Sequencer.

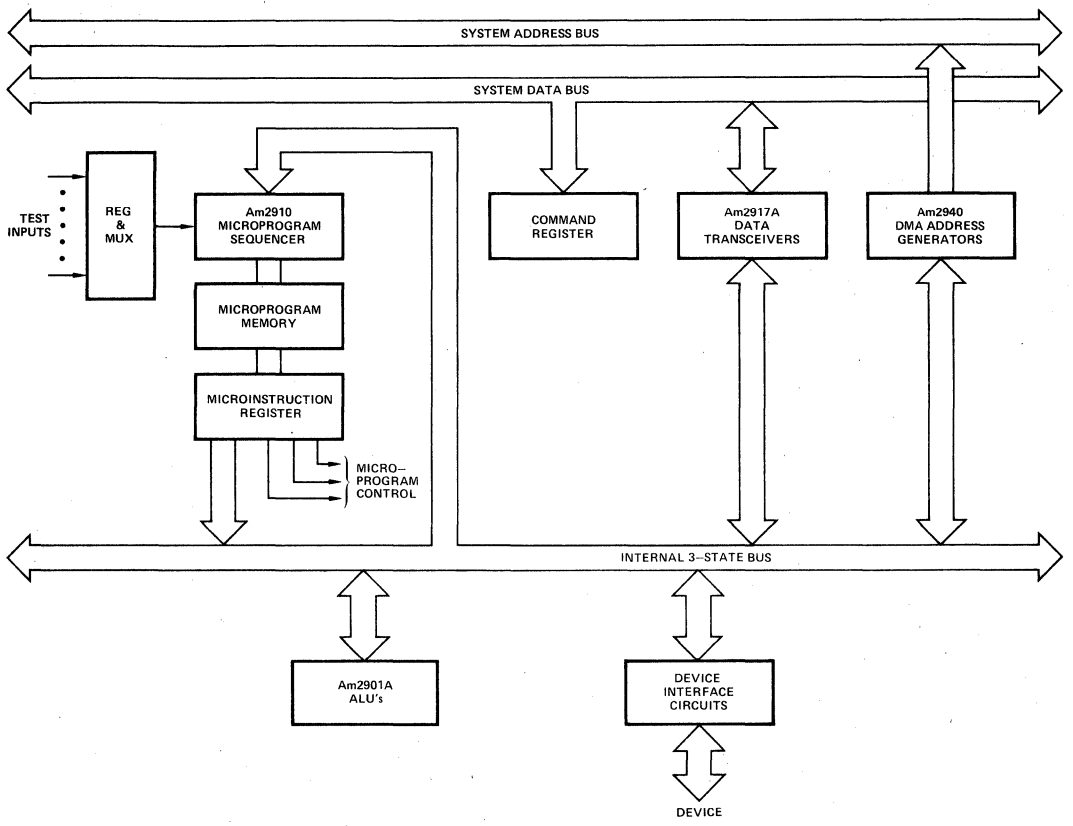


Figure 3. DMA Peripheral Controller Block Diagram.

Am2942

Programmable Timer/Counter DMA Address Generator

DISTINCTIVE CHARACTERISTICS

- 22-pin version of Am2940 –
  Provides multiplexed Address and Data lines plus additional Instruction Input and Instruction Enable pins.
- Can be used as either DMA Address Generator or Programmable Timer Counter.
- Executes 16 instructions –
  Eight DMA instructions plus eight Timer/Counter instructions
- Provides two independent programmable 8-bit up/down counters in a 22-pin package –
  Counters can be cascaded to form single-chip 16-bit up/down counter.
- Reinitialize capability –
  Counters can be reinitialized from on-chip registers.
- Expandable eight-bit slice –
  Any number of Am2942s can be cascaded. Three devices provide a 48 bit counter.
- Programmable control modes –
  Provide four types of control.
- High speed bipolar LSI –
  Advanced Low-Power Schottky TTL technology provides typical count frequency of 25MHz and 24mA output current sink capability.

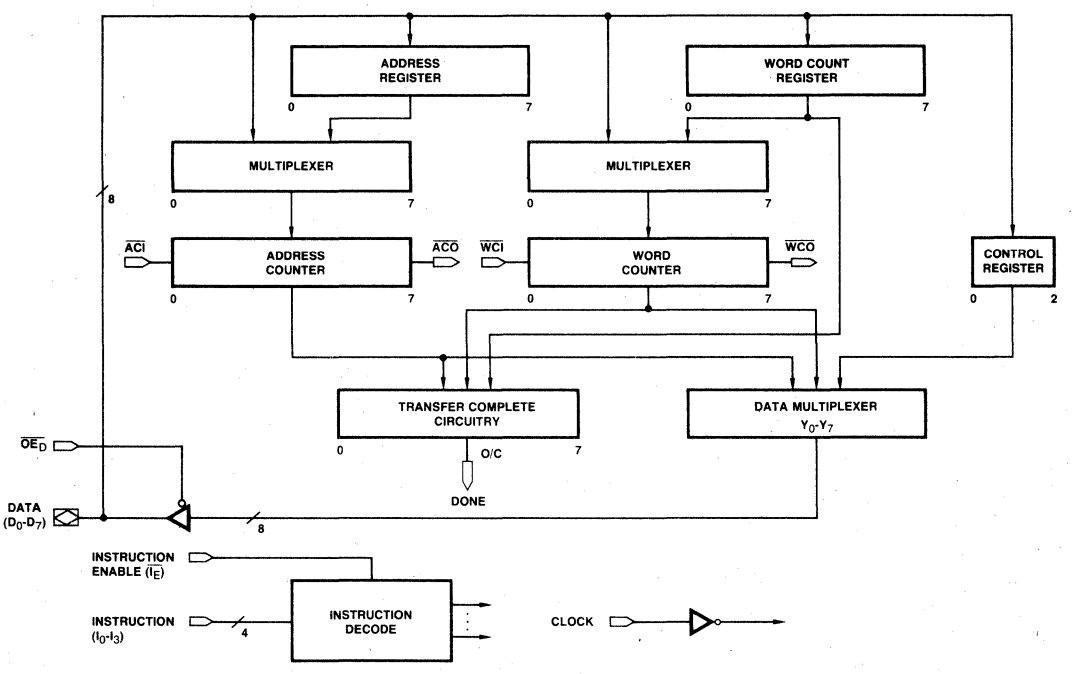
GENERAL DESCRIPTION

The Am2942, a 22-pin version of the Am2940, can be used as a high-speed DMA Address Generator or Programmable Timer/Counter. It provides multiplexed Address and Data lines, for use with a common bus, and additional Instruction Input and Instruction Enable pins. The Am2942 executes 16 instructions; eight are the same as the Am2940 instructions, and eight instructions facilitate the use of the Am2942 as a Programmable Timer/Counter. The Instruction Enable input allows the sharing of the Am2942 instruction field with other devices.

When used as a Timer/Counter, the Am2942 provides two independent, programmable, eight-bit, up-down counters in a 22-pin package. The two on-chip counters can be cascaded to form a single chip, 16-bit counter. Also, any number of chips can be cascaded – for example three cascaded Am2942s form a 48-bit timer/counter.

Reinitialization instructions provide the capability to reinitialize the counters from on-chip registers. Am2942 Programmable Control Modes, identical to those of the Am2940, offer four different types of programmable control.

BLOCK DIAGRAM



For applications information see the last part of this data sheet and Chapter VII of *Bit Slice Microprocessor Design,* by Mick and Brick, McGraw-Hill Publishers.

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ORDERING INFORMATION

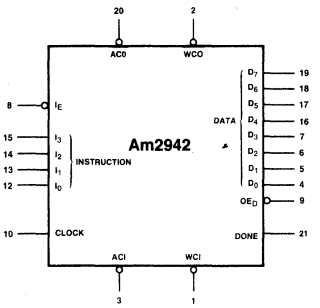
Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2942DC	D-22	C	C-1
AM2942DC-B	D-22	C	B-2 (Note 4)
AM2942DM	D-22	M	C-3
AM2942DM-B	D-22	M	B-3
AM2942FM	F-22	M	C-3
AM2942FM-B	F-22	M	B-3
AM2942LC	L-28	C	C-1
AM2942LM	L-28	M	C-3
AM2942LM-B	L-28	M	B-3
AM2942XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2942XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

5

LOGIC SYMBOL



V_{CC} = Pin 22
GND = Pin 11

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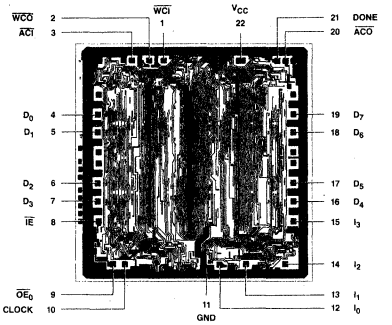
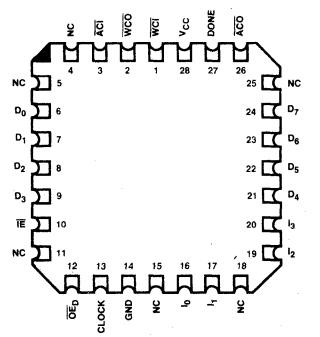
METALLIZATION AND PAD LAYOUT



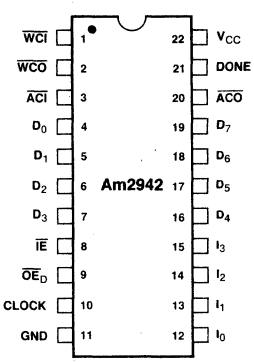
DIE SIZE: 0.181″ X 0.178″

CONNECTION DIAGRAMS – Top Views

Chip-Pak™ L-28-1



D-22



F-22 Pin Configuration identical to D-22

Note: Pin 1 is marked for orientation.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

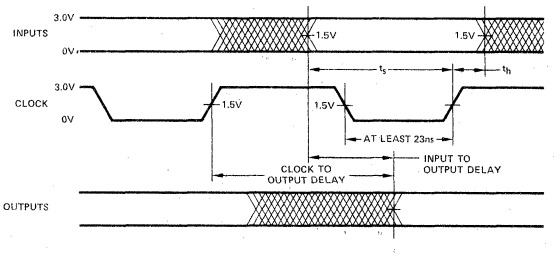
OPERATING RANGE

P/N	Range	Temperature	V_{CC}	
Am2942DC	COM'L	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5%	(MIN. = 4.75V MAX. = 5.25V)
Am2942DM, FM	MIL	T_C = −55° to +125°C	V_{CC} = 5.0V ±10%	(MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}		MIL I_{OH} = −1.0mA COM'L I_{OH} = −2.6mA	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	WCO, ACO	MIL I_{OL} = 8.0mA COM'L I_{OL} = 12mA			0.5	Volts
			D_{0-7}, DONE	MIL I_{OL} = 16mA COM'L I_{OL} = 24mA				
V_{IH}	Input HIGH Level (Note 4)	Guaranteed Input Logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Note 4)	Guaranteed Input Logical LOW voltage for all inputs					0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V		D_{0-7} All Others			−0.15 −0.8	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V		D_{0-7} All Others			150 40	μA
I_{CEX}	Output Leakage on DONE	V_{CC} = MAX., V_O = 5.5V					250	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX. + 0.5V, V_O = 0.5V			−30		−85	mA
I_{OZL} I_{OZH}	Output OFF Current	V_{CC} = MAX. $\overline{OE}$ = 2.4V	V_{OUT} = 0.5V V_{OUT} = 2.4V	D_{0-7} D_{0-7}			−150 150	μA
I_{CC}	Power Supply Current	V_{CC} = MAX.		T_A = 25°C		155	250	mA
			Am2942PC, DC	T_A = 0°C to +70°C			265	
				T_A = +70°C			220	
			Am2942DM, FM	T_C = −55°C to +125°C			285	
				T_C = +125°C			205	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should only be static tested in a noise-free environment (not functional testing).



See Tables A for t_s and t_h for various inputs. See Tables B for combinational delays from clock and other inputs to outputs.

Figure 5. Switching Waveforms.

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SWITCHING CHARACTERISTICS

The tables below define the Am2942 switching characteristics. Tables A are set-up and hold times relative to the clock LOW-to-HIGH transition. Tables B are combinational delays. Tables C are clock requirements. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns with C_L = 50pF except output disable times (I to D) which are specified for a 5pF load. All times are in ns.

I. GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

Am2942PC, DC (T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	24	6
I_{0-3}	46	5
$\overline{ACI}$	30	4
$\overline{WCI}$	30	3
I_E	46	5

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	DONE	D_{0-7}
$\overline{ACI}$	20	–	–	–
$\overline{WCI}$ (Note 1)	–	20	46	–
I_{0-3}	–	–	–	37
CP (Note 2)	58	58	85	59
I_E	–	–	–	37

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	34	ns
Maximum Clock Frequency	17	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
$\overline{OE}$	D_{0-7}	25	25	ns

II. GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

Am2942DM, FM (T_C = −55 to +125°C, V_{CC} = 4.5 to 5.5V, C_L = 50pF)

A. Set-up and Hold Times (Relative to clock LOW-to-HIGH transition)

Input	t_s	t_h
D_{0-7}	27	7
I_{0-3}	49	5
$\overline{ACI}$	34	5
$\overline{WCI}$	34	5
I_E	49	5

B. Combinational Delays

Input	$\overline{ACO}$	$\overline{WCO}$	DONE	D_{0-7}
$\overline{ACI}$	21	–	–	–
$\overline{WCI}$ (Note 1)	–	21	54	–
I_{0-3}	–	–	–	41
CP (Note 2)	64	64	88	68
I_E	–	–	–	41

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	35	ns
Maximum Clock Frequency	17	MHz

D. Enable/Disable Times

From	To	Disable	Enable	
$\overline{OE}$	D_{0-7}	30	30	ns

Notes: 1. $\overline{WCI}$ to Done occurs only in control modes 0 and 1.
2. CP to Done occurs only in control modes 0, 1, and 2.

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5–8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

Am2942 ARCHITECTURE

As shown in the Block Diagram, the Am2942 consists of the following:

- A three-bit Control Register.
- An eight-bit Address Counter with input multiplexer.
- An eight-bit Address Register.
- An eight-bit Word Counter with input multiplexer.
- An eight-bit Word Count Register.
- Transfer complete circuitry.
- An eight-bit wide data multiplexer with three-state output buffers.
- An instruction decoder.

Control Register

Under instruction control, the Control Register can be loaded or read from the bidirectional DATA lines D_0-D_7. Control Register bits 0 and 1 determine the Am2942 Control Mode, and bit 2 determines whether the Address Counter increments or decrements. Figure 1 defines the Control Register format.

Address Counter

The Address Counter, which provides the current memory address, is an eight-bit, binary, up/down counter with full look-ahead carry generation. The Address Carry input ($\overline{ACI}$) and Address Carry Output ($\overline{ACO}$) allow cascading to accommodate larger addresses. Under instruction control, the Address Counter can be enabled, disabled, and loaded from the DATA inputs, D_0-D_7, or the Address Register. When enabled and the $\overline{ACI}$ input is LOW, the Address Counter increments/decrements on the LOW to HIGH transition of the CLOCK input, CP.

Address Register

The eight-bit Address Register saves the initial address so that it can be restored later in order to repeat a transfer operation. When the LOAD ADDRESS instruction is executed, the Address Register and Address Counter are simultaneously loaded from the DATA inputs, D_0-D_7.

Word Counter and Word Count Register

The Word Counter and Word Count Register, which maintain and save a word count, are similar in structure and operation to the Address Counter and Address Register, with the exception that the Word Counter increments in Control Modes 1 and 3, and decrements in Control Modes 0 and 2. The LOAD WORD COUNT instruction simultaneously loads the Word Counter and Word Count Register.

Transfer Complete Circuitry

The Transfer Complete Circuitry is a combinational logic network which detects the completion of the data transfer operation in three Control Modes and generates the DONE output signal. The DONE signal is a open-collector output, which can be dot-anded between chips.

Data Multiplexer

The Data Multiplexer is an eight-bit wide, three-input multiplexer which allows the Address Counter, Word Counter and Control Register to be read at DATA lines D_0-D_7. The Data Multiplexer output, Y_0-Y_7, is enabled onto DATA lines D_{0-7} if and only if the Output Enable input, $\overline{OE_D}$, is LOW. (Refer to Figure 2.)

Instruction Decoder

The Instruction Decoder generates required internal control signals as a function of the INSTRUCTION inputs, I_0-I_3 Control Register bits 0 and 1, and the INSTRUCTION ENABLE input, $\overline{I_E}$.

Clock

The CLOCK input, CP is used to clock the Address Register, Address Counter, Word Count Register, Word Counter, and Control Register, all on the LOW to HIGH transition of the CP signal.

Control Register

CR_2	CR_1	CR_0

CR_1	CR_0	Control Mode Number	Control Mode Type	Word Counter	DONE Output Signal	
					$\overline{WCI}$ = LOW	$\overline{WCI}$ = HIGH
L	L	0	Word Count Equals Zero	Decrement	HIGH when Word Counter = 1	HIGH when Word Counter = 0
L	H	1	Word Count Compare	Increment	HIGH when Word Counter + 1 = Word Count Reg.	HIGH when Word Counter = Word Count Reg.
H	L	2	Address Compare	Decrement	HIGH when Word Counter = Address Counter	
H	H	3	Word Counter Carry Out	Increment	Always LOW	

H = HIGH
L = LOW

CR_2	Address Counter
L	Increment
H	Decrement

Figure 1. Control Register Format Definition.

$\overline{OE_D}$	D_0-D_7
L	DATA MULTIPLEXER OUTPUT, Y_0-Y_7
H	HIGH Z

Figure 2. Data Bus Output Enable Function.

Am2942 INSTRUCTIONS

The Am2942 instruction set consists of sixteen instructions. Eight are DMA Instructions and are similar to the Am2940 instructions. The remaining eight instructions are designed to facilitate the use of the Am2942 as a Programmable Timer/Counter. Figures 3 and 4 define the Am2942 Instructions.

Instructions 0-7 are DMA instructions. The WRITE CONTROL REGISTER instruction writes DATA input D_0-D_2 into the Control Register; DATA inputs D_3-D_7 are "don't care" inputs for this instruction. The READ CONTROL REGISTER instruction gates the Control Register to Data Multiplexer outputs Y_0-Y_2. Outputs Y_3-Y_7 are HIGH during this instruction.

The Word Counter can be read using the READ WORD COUNTER instruction, which gates the Word Counter to Data Multiplexer outputs, Y_0-Y_7. The LOAD WORD COUNT instruction is Control Mode dependent. In Control Modes 0, 2, and 3, DATA inputs D_0-D_7 are written into both the Word Count Register and Word Counter. In Control Mode 1, DATA inputs D_0-D_7 are written into the Word Count Register and the Word Counter is cleared.

The READ ADDRESS COUNTER instruction gates the Address Counter to Data Multiplexer outputs, Y_0-Y_7, and the LOAD ADDRESS instruction writes DATA inputs D_0-D_7 into both the Address Register and Address Counter.

In Control Modes 0, 1, and 3, the ENABLE COUNTERS instruction enables both the Address and Word Counters; in Control Mode 2, the Address Counter is enabled and the Word Counter holds its contents. When enabled and the carry input is active, the counters increment on the LOW to HIGH transition of the CLOCK input, CP. Thus, with this instruction applied, counting can be controlled by the carry inputs.

The REINITIALIZE COUNTERS instruction also is Control Mode dependent. In Control Modes 0, 2, and 3, the contents of the Address Register and Word Count Register are transferred to the respective Address Counter and Word Counter; in Control Mode 1, the content of the Address Register is transferred to the Address Counter and the Word Counter is cleared. The REINITIALIZE COUNTERS instruction allows a data transfer operation to be repeated without reloading the address and word count from the DATA lines.

When $\overline{I_E}$ is HIGH, Instruction inputs, I_0-I_2, are disabled. If I_3 is LOW, the function performed is identical to that of the ENABLE COUNTERS instruction. Thus, counting can be controlled by the carry inputs with the ENABLE COUNTERS instruction applied or with Instruction Inputs I_0-I_2 disabled.

Instructions 8-F facilitate the use of the Am2942 as a Programmable Timer/Counter. They differ from instructions 0-7 in that they provide independent control of the Address Counter, Word Counter and Control Register.

The WRITE CONTROL REGISTER, T/C instruction writes DATA input D_0-D_2 into the Control Register. DATA inputs D_3-D_7 are "don't care" inputs for this instruction. The Address and Word Counters are enabled, and the Control Register contents appear at the Data Multiplexer output.

The REINITIALIZE ADDRESS COUNTER instruction allows the independent reinitialization of the Address Counter. The Word Counter is enabled and the contents of the Address Counter appear at the Data Multiplexer output.

$\overline{I_E}$	I_3	I_2	I_1	I_0	HEX CODE		
0	0	0	0	0	0	WRITE CONTROL REGISTER	DMA INSTRUCTIONS
0	0	0	0	1	1	READ CONTROL REGISTER	
0	0	0	1	0	2	READ WORD COUNTER	
0	0	0	1	1	3	READ ADDRESS COUNTER	
0	0	1	0	0	4	REINITIALIZE COUNTERS	
0	0	1	0	1	5	LOAD ADDRESS	
0	0	1	1	0	6	LOAD WORD COUNT	
0	0	1	1	1	7	ENABLE COUNTERS	
1	0	X	X	X	0-7	INSTRUCTION DISABLE	
0	1	0	0	0	8	WRITE CONTROL REGISTER, T/C	TIMER/COUNTER INSTRUCTIONS
0	1	0	0	1	9	REINITIALIZE ADDRESS COUNTER	
0	1	0	1	0	A	READ WORD COUNTER, T/C	
0	1	0	1	1	B	READ ADDRESS COUNTER, T/C	
0	1	1	0	0	C	REINITIALIZE ADDRESS & WORD COUNTERS	
0	1	1	0	1	D	LOAD ADDRESS, T/C	
0	1	1	1	0	E	LOAD WORD COUNT, T/C	
0	1	1	1	1	F	REINITIALIZE WORD COUNTER	
1	1	X	X	X	8-F	INSTRUCTION DISABLE, T/C	

0 = LOW 1 = HIGH X = DON'T CARE

Notes: 1. When I_3 is tied LOW, the Am2942 acts as a DMA circuit: When I_3 is tied HIGH, the Am2942 acts as a Timer/Counter circuit.
2. Am2942 instructions 0 through 7 are the same as Am2940 instructions.

Figure 3. Am2942 Instructions.

The Word Counter can be read, using the READ WORD COUNTER, T/C instruction. Both counters are enabled when this instruction is executed.

When the READ ADDRESS COUNTER, T/C instruction is executed, both counters are enabled and the address counter contents appear at the Data Multiplexer output.

The REINITIALIZE ADDRESS and WORD COUNTERS instruction provides the capability to reinitialize both counters at the same time. The Address Counter contents appear at the Data Multiplexer output.

DATA inputs D_0-D_7 are loaded into both the Address Register and Counter when the LOAD ADDRESS, T/C instruction is executed. The Word Counter is enabled and its contents appear at the Data Multiplexer output.

The LOAD WORD COUNT, T/C instruction is identical to the LOAD WORD COUNT instruction with the exception that Address Counter is enabled.

The Word Counter can be independently reinitialized using the REINITIALIZE WORD COUNTER instruction. The Address Counter is enabled and the Word Counter contents appear at the Data Multiplexer output.

When the $\overline{I_E}$ input is HIGH, Instruction inputs, I_0-I_2, are disabled. The function performed when I_3 is HIGH is identical to that performed when I_3 is LOW, with the exception that the Word Counter contents appear at the Data Multiplexer output.

$\overline{I_E}$	$I_3I_2I_1I_0$ (Hex)	Function	Mnemonic	Control Mode	Word Reg.	Word Counter	Adr. Reg.	Adr. Counter	Control Reg.	Data Multiplexer Output
L	0	WRITE CONTROL REGISTER	WRCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	$D_{0\text{-}2} \rightarrow$ CR	FORCED HIGH
L	1	READ CONTROL REGISTER	RDCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	CONTROL REG.
L	2	READ WORD COUNTER	RDWC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	WORD COUNTER
L	3	READ ADDRESS COUNTER	RDAC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	ADR. COUNTER
L	4	REINITIALIZE COUNTERS	REIN	0, 2, 3	HOLD	WR → WC	HOLD	AR → AC	HOLD	ADR. CNTR.
				1	HOLD	ZERO → WC	HOLD	AR → AC	HOLD	ADR. CNTR.
L	5	LOAD ADDRESS	LDAD	0, 1, 2, 3	HOLD	HOLD	D → AR	D → AC	HOLD	WORD COUNTER
L	6	LOAD WORD COUNT	LDWC	0, 2, 3	D → WR	D → WC	HOLD	HOLD	HOLD	FORCED HIGH
				1	D → WR	ZERO → WC	HOLD	HOLD	HOLD	FORCED HIGH
L	7	ENABLE COUNTERS	ENCT	0, 1, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	ADR. CNTR.
				2	HOLD	HOLD	HOLD	ENABLE	HOLD	ADR. CNTR.
H	0-7	INSTRUCTION DISABLE	–	0, 1, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	ADR. CNTR.
				2	HOLD	HOLD	HOLD	ENABLE	HOLD	ADR. CNTR.
L	8	WRITE CONTROL REGISTER, T/C	WCRT	0, 1, 2, 3	HOLD	ENABLE	HOLD	ENABLE	$D_{0\text{-}2} \rightarrow$ CR	CONTROL REG.
L	9	REINITIALIZE ADR. COUNTER	REAC	0, 1, 2, 3	HOLD	ENABLE	HOLD	AR → AC	HOLD	ADR. COUNTER
L	A	READ WORD COUNTER, TC	RWCT	0, 1, 2, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	WORD COUNTER
L	B	READ ADDRESS COUNTER, T/C	RACT	0, 1, 2, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	ADR. COUNTER
L	C	REINITIALIZE ADDRESS AND WORD COUNTERS	RAWC	0, 2, 3	HOLD	WR → WC	HOLD	AR → AC	HOLD	ADR. CNTR.
				1	HOLD	ZERO → WC	HOLD	AR → AC	HOLD	ADR. CNTR.
L	D	LOAD ADDRESS, T/C	LDAT	0, 1, 2, 3	HOLD	ENABLE	D → AR	D → AC	HOLD	WORD COUNTER
L	E	LOAD WORD COUNT, T/C	LWCT	0, 2, 3	D → WR	D → WC	HOLD	ENABLE	HOLD	FORCED HIGH
				1	D → WR	ZERO → WC	HOLD	ENABLE	HOLD	FORCED HIGH
L	F	REINITIALIZE WORD COUNTER	REWC	0, 2, 3	HOLD	WR → WC	HOLD	ENABLE	HOLD	WD. CNTR.
				1	HOLD	ZERO → WC	HOLD	ENABLE	HOLD	WD. CNTR.
H	8-F	INSTRUCTION DISABLE, T/C	–	0, 1, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	WD. CNTR.
				2	HOLD	HOLD	HOLD	ENABLE	HOLD	WD. CNTR.

WR = WORD REGISTER
WC = WORD COUNTER
AR = ADDRESS REGISTER
AC = ADDRESS COUNTER
CR = CONTROL REGISTER
D = DATA

Figure 4. Am2942 Function Table.

Am2942 CONTROL MODES

Control Mode 0 – Word Count Equals Zero Mode

In this mode, the LOAD WORD COUNT instruction loads the word count into the Word Count Register and Word Counter. When the Word Counter is enabled and the Word Counter Carry-in, $\overline{WCI}$, is LOW, the Word Counter decrements on the LOW to HIGH transition of the CLOCK input, CP. Figure 1 specifies when the DONE signal is generated in this mode.

Control Mode 1 – Word Count Compare Mode

In this mode the LOAD WORD COUNT instruction loads the word count into the Word Count Register and clears the Word Counter. When the Word Counter is enabled and the Word Counter Carry-in, $\overline{WCI}$, is LOW, the Word Counter increments on the LOW to HIGH transition of the clock input, CP. Figure 1 specifies when the DONE signal is generated.

Control Mode 2 – Address Compare Mode

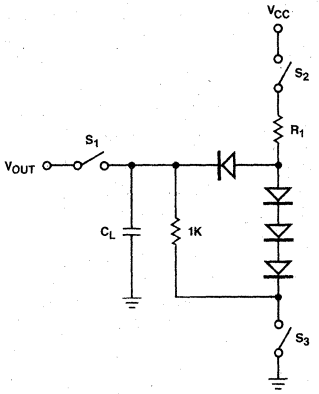
In this mode, only an initial and final memory address need to be specified. The initial Memory Address is loaded into the Address Register and Address Counter and the final memory address is loaded into the Word Count Register and Word Counter. The Word Counter is always disabled in this mode and serves as a holding register for the final memory address. When the Address Counter is enabled and the $\overline{ACI}$ input is LOW, the Address Counter increments or decrements (depending on Control Register bit 2) on the LOW to HIGH transition of the CLOCK input, CP. The Transfer Complete Circuitry compares the Address Counter with the Word Counter and generates the DONE signal during the last word transfer, i.e. when the Address Counter equals the Word Counter.

Control Mode 3 – Word Counter Carry Out Mode

For this mode of operation, the user can load the Word Count Register and Word Counter with the two's complement of the number of data words to be transferred. When the Word Counter is enabled and the $\overline{WCI}$ input is LOW, the Word Counter increments on the LOW to HIGH transition of the CLOCK input, CP. A Word Counter Carry Out signal, $\overline{WCO}$, indicates the last data word is being transferred. The DONE signal is not required in this mode and, therefore, is always LOW.

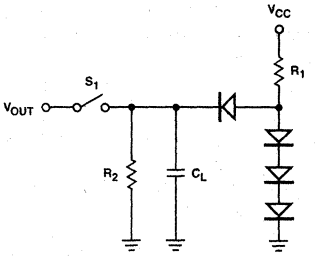
TEST OUTPUT LOAD CONFIGURATIONS FOR Am2942

A. THREE STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

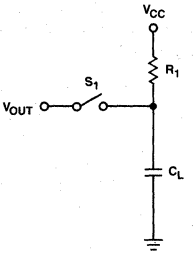
B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

C. OPEN-COLLECTOR OUTPUTS



$$R_1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2942 (DIP)

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
–	$D_{0\text{-}7}$	A	220	1K
20	$\overline{ACO}$	B	470	2.4K
21	DONE	C	270	–
2	$\overline{WCO}$	B	470	2.4K

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

APPLICATIONS

Figure 6 shows an Am2942 used as two independent, programmable eight-bit timer/counters. In this example, an Am2910 Microprogram Sequencer provides an address to Am27S27 512 x 8 Registered PROMs. The on-chip PROM output register is used as the Microinstruction Register.

The Am2942 Instruction input, I_3, is tied HIGH to select the eight Timer/Counter instructions. The $\overline{I_E}$, I_0-I_2, and $\overline{OE_D}$ inputs are provided by the microinstruction, and the D_0-D_7 data lines are connected to a common Data Bus. GATE WC and GATE AC are separate enable controls for the respective Word Counter and Address Counter. The DONE, $\overline{ACO}$ and $\overline{WCO}$ output signals indicate that a pre-programmed time or count has been reached.

Figure 7 shows an Am2942 used as a single 16-bit programmable timer/counter. In this example, the Word Counter carry-out, $\overline{WCO}$, is connected to the Address Counter carry-in, $\overline{ACI}$, to form a single 16-bit counter which is enabled by the GATE signal.

Figure 8 shows two Am2942s cascaded to form a 32-bit programmable timer/counter. The two Word Counters form the low order 16 bits, and the two Address Counters form the high order bits. This allows the timer/counter to be loaded and read 16 bits at a time.

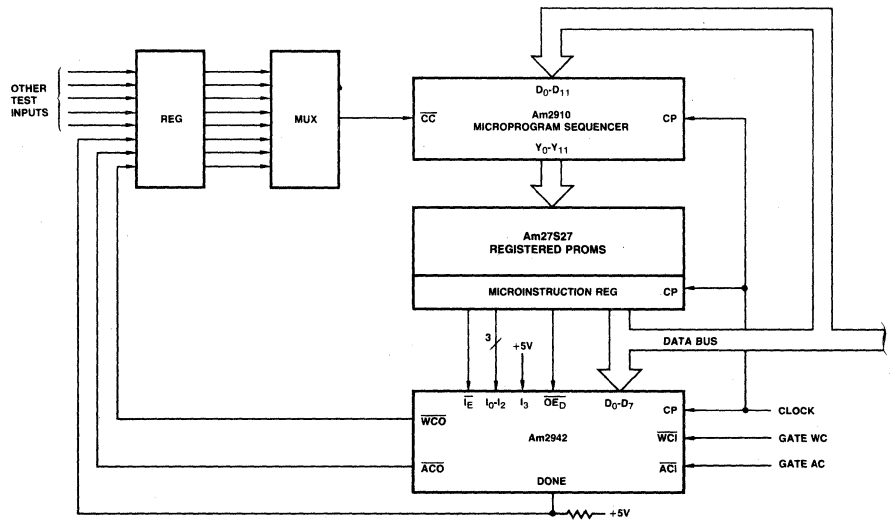


Figure 6. Two 8-Bit Programmable Counters/Timers in a 22-Pin Package.

MPR-234

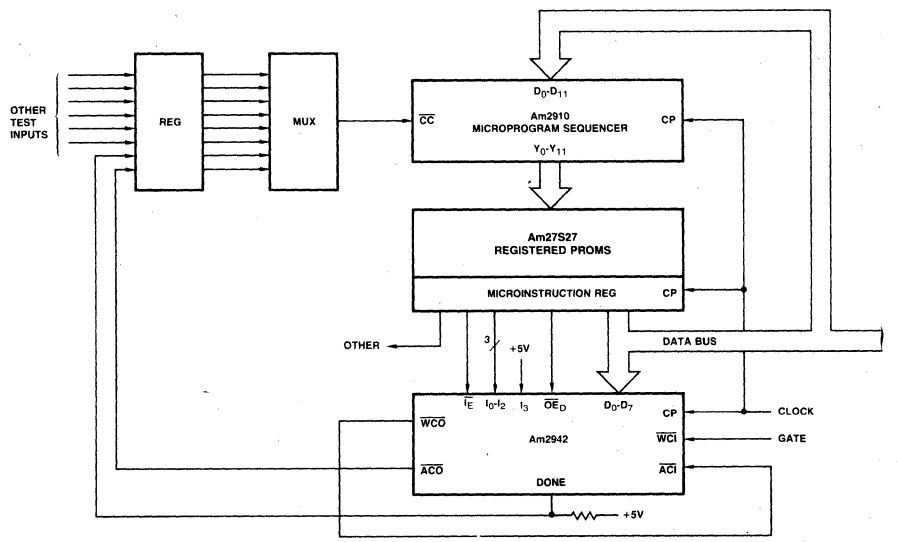


Figure 7. 16-Bit Programmable Counter/Timer Using a Single Am2942.

MPR-235

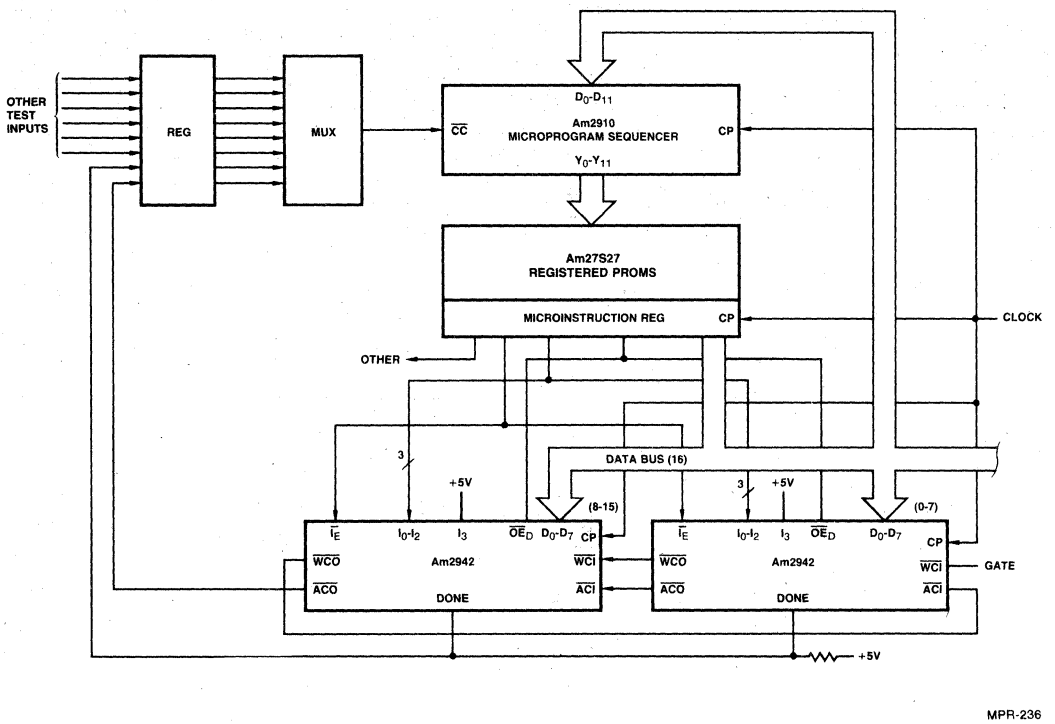


Figure 8. 32-Bit Programmable Counter/Timer Using Two Am2942s.

Am2946 • Am2947

Octal Three-State Bidirectional Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- 8-bit bidirectional data flow reduces system package count
- 3-state inputs/outputs for interfacing with bus-oriented systems
- PNP inputs reduce input loading
- V_{CC} – 1.15 V_{OH} interfaces with TTL, MOS and CMOS
- 48mA, 300pF bus drive capability
- Am2946 inverting transceivers
- Am2947 noninverting transceivers
- Transmit/$\overline{\text{Receive}}$ and Chip Disable simplify control logic
- 20-pin ceramic and molded DIP package
- Low power – 8mA per bidirectional bit
- Advanced Schottky processing
- Bus port stays in hi-impedance state during power up/down

FUNCTIONAL DESCRIPTION

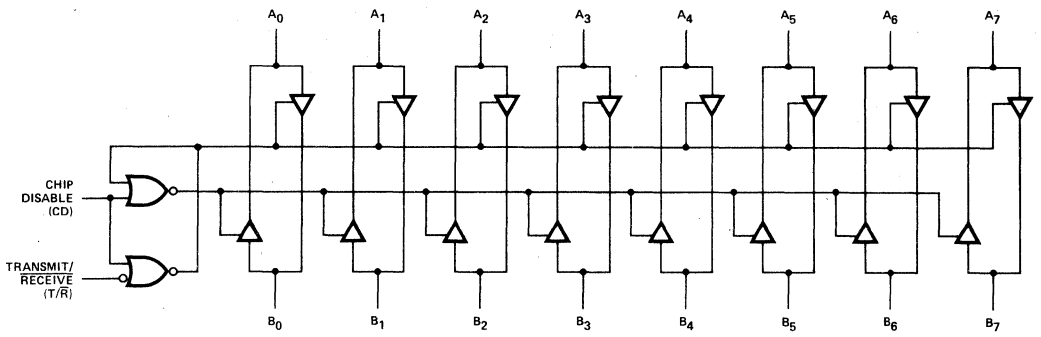
The Am2946 and Am2947 are 8-bit state Schottky transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 24mA drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

One input, Transmit/$\overline{\text{Receive}}$ determines the direction of logic signals through the bidirectional transceiver. The Chip Disable input disables both A and B ports by placing them in a 3-state condition. Chip Disable is functionally the same as an active LOW chip select.

The output high voltage (V_{OH}) is specified at V_{CC} – 1.15V minimum to allow interfacing with MOS, CMOS, TTL, ROM, RAM, or microprocessors.

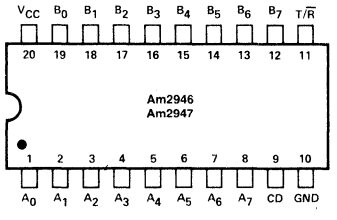
5

Am2947
LOGIC DIAGRAM



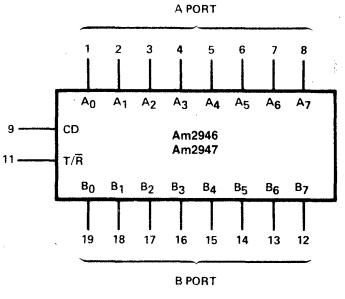
Am2946 has inverting transceivers.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientaton.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Lead Temperature (Soldering, 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:

MIL	T_A = −55 to +125°C	V_{CC} MIN = 4.5V	V_{CC} MAX = 5.5V
COM'L	T_A = 0 to +70°C	V_{CC} MIN = 4.75V	V_{CC} MAX = 5.25V

DC ELECTRICAL CHARACTERISTICS over operating temperature range

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
A PORT (A_0-A_7)							
V_{IH}	Logical "1" Input Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V		2.0			Volts
V_{IL}	Logical "0" Input Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V	COM'L			0.8	Volts
			MIL			0.7	
V_{OH}	Logical "1" Output Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = 0.8V	I_{OH} = −0.4mA	V_{CC}−1.15	V_{CC}−0.7		Volts
			I_{OH} = −3.0mA	2.7	3.95		
V_{OL}	Logical "0" Output Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = 0.8V	I_{OL} = 12mA		0.3	0.4	Volts
			COM'L I_{OL} = 24mA		0.35	0.50	
I_{OS}	Output Short Circuit Current	CD = V_{IL} MAX, T/$\overline{R}$ = 0.8V, V_O = 0V, V_{CC} = MAX, Note 2		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V, V_I = 2.7V			0.1	80	µA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} MAX, V_I = V_{CC} MAX				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V, V_I = 0.4V			−70	−200	µA
V_C	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12mA			−0.7	−1.5	Volts
I_{OD}	Output/Input 3-State Current	CD = 2.0V	V_O = 0.4V			−200	µA
			V_O = 4.0V			80	
B PORT (B_0-B_7)							
V_{IH}	Logical "1" Input Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = V_{IL} MAX		2.0			Volts
V_{IL}	Logical "0" Input Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = V_{IL} MAX	COM'L			0.8	Volts
			MIL			0.7	
V_{OH}	Logical "1" Output Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V	I_{OH} = −0.4mA	V_{CC}−1.15	V_{CC}−0.8		Volts
			I_{OH} = −5.0mA	2.7	3.9		
			I_{OH} = −10mA	2.4	3.6		
V_{OL}	Logical "0" Output Voltage	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V	I_{OL} = 20mA		0.3	0.4	Volts
			I_{OL} = 48mA		0.4	0.5	
I_{OS}	Output Short Circuit Current	CD = V_{IL} MAX, T/$\overline{R}$ = 2.0V, V_O = 0V, V_{CC} = MAX, Note 2		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL} MAX, T/$\overline{R}$ = V_{IL} MAX, V_I = 2.7V			0.1	80	µA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = MAX, V_I = V_{CC} MAX				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL} MAX, T/$\overline{R}$ = V_{IL} MAX, V_I = 0.4V			−70	−200	µA
V_C	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12mA			−0.7	−1.5	Volts
I_{OD}	Output/Input 3-State Current	CD = 2.0V	V_O = 0.4V			−200	µA
			V_O = 4.0V			200	
CONTROL INPUTS CD, T/$\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			Volts
V_{IL}	Logical "0" Input Voltage		COM'L			0.8	Volts
			MIL			0.7	
I_{IH}	Logical "1" Input Current	V_I = 2.7V			0.5	20	µA
I_I	Input Current at Maximum Input Voltage	V_{CC} = MAX, V_I = V_{CC} MAX				1.0	mA
I_{IL}	Logical "0" Input Current	V_I = 0.4V	T/$\overline{R}$		−0.1	−0.25	mA
			CD		−0.1	−0.25	
V_C	Input Clamp Voltage	I_{IN} = −12mA			−0.8	−1.5	Volts
	POWER SUPPLY CURRENT						
I_{CC}	Power Supply Current	Am2946	CD = V_I = 2.0V, V_{CC} = MAX		70	100	mA
			CD = 0.4V, V_{INA} = T/$\overline{R}$ = 2.0V, V_{CC} = MAX		100	150	
		Am2947B	CD = 2.0V, V_I = 0.4V, V_{CC} = MAX		70	100	mA
			CD = V_{INA} = 0.4V, T/$\overline{R}$ = 2.0V, V_{CC} = MAX		90	140	

Am2946
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C)

Parameter	Description	Test Conditions	Typ (Note 1)	Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	8	12	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	11	16	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	10	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 30pF	19	25	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 5k, C_4 = 30pF	19	25	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	12	18	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	7	12	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	15	20	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	9	14	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	25	35	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	16	22	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 300pF	22	35	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	14	22	ns
TRANSMIT RECEIVE MODE SPECIFICATIONS					
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 5pF S_2 = 1, R_3 = 1k, C_2 = 30pF	23	33	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 100Ω, C_3 = 5pF S_2 = 0, R_3 = 5k, C_2 = 30pF	22	33	ns
t_{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 300pF S_2 = 1, R_3 = 300Ω, C_2 = 5pF	26	35	ns
t_{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 1k, C_3 = 300pF S_2 = 0, R_3 = 300Ω, C_2 = 5pF	27	35	ns

Notes: 1. All typical values given are for V_{CC} = 5.0V and T_A = 25°C.
2. Only one output at a time should be shorted.

FUNCTION TABLE

Inputs	Conditions		
Chip Disable	0	0	1
Transmit/$\overline{Receive}$	0	1	X
A Port	Out	In	HI-Z
B Port	In	Out	HI-Z

AC ELECTRICAL CHARACTERISTICS over operating range

Parameter	Description	Test Conditions	Am2946 COM'L T_A = 0 to +70°C V_{CC} = 5.0V ±5% Max	Am2946 MIL T_A = −55 to +125°C V_{CC} = 5.0V ±10% Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	16	19	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	20	23	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	18	21	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	18	21	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 30pF	28	33	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 5k, C_4 = 30pF	28	33	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	24	29	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	16	19	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	25	30	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	19	22	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	23	26	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	18	21	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	38	43	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	26	30	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 300pF	38	43	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	26	30	ns
TRANSMIT RECEIVE MODE SPECIFICATIONS					
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 5pF S_2 = 1, R_3 = 1k, C_2 = 30pF	38	43	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 100Ω, C_3 = 5pF S_2 = 0, R_3 = 5k, C_2 = 30pF	38	43	ns
t_{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 300pF S_2 = 1, R_3 = 300Ω, C_2 = 5pF	41	47	ns
t_{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 1k, C_3 = 300pF S_2 = 0, R_3 = 300Ω, C_2 = 5pF	41	47	ns

Am2947
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C)

Parameter	Description	Test Conditions	Typ (Note 1)	Max	Units
		A PORT DATA/MODE SPECIFICATIONS			
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	14	18	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	13	18	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	11	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 30pF	19	25	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 5k, C_4 = 30pF	19	25	ns
		B PORT DATA/MODE SPECIFICATIONS			
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	18	23	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	11	18	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	16	23	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	11	18	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	25	35	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	16	22	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 300pF	26	35	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	14	22	ns
		TRANSMIT RECEIVE MODE SPECIFICATIONS			
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 5pF S_2 = 1, R_3 = 1k, C_2 = 30pF	28	38	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 5pF S_2 = 0, R_3 = 5k, C_2 = 30pF	28	38	ns
t_{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 300pF S_2 = 0, R_3 = 300Ω, C_2 = 5pF	31	40	ns
t_{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 1k, C_3 = 300pF S_2 = 1, R_3 = 300Ω, C_2 = 5pF	31	40	ns

Notes: 1. All typical values given are for V_{CC} = 5.0V and T_A = 25°C.
2. Only one output at a time should be shorted.

DEFINITION OF FUNCTIONAL TERMS

A_0-A_7 A port inputs/outputs are receiver output drivers when T/$\overline{R}$ is LOW and are transmit inputs when T/$\overline{R}$ is HIGH.

B_0-B_7 B port inputs/outputs are transmit output drivers when T/$\overline{R}$ is HIGH and receiver inputs when T/$\overline{R}$ is LOW.

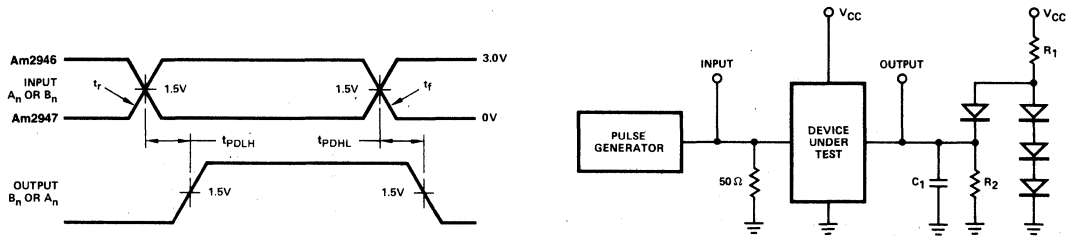
CD Chip Disable forces all output drivers into 3-state when HIGH (same function as active LOW chip select, $\overline{CS}$).

T/$\overline{R}$ Transmit/$\overline{Receive}$ direction control determines whether A port or B port drivers are in 3-state. With T/$\overline{R}$ HIGH A port is the input and B port is the output. With T/$\overline{R}$ LOW A port is the output and B port is the input.

AC ELECTRICAL CHARACTERISTICS over operating range

Parameter	Description	Test Conditions	Am2947 COM'L T_A = 0 to +70°C, V_{CC} = 5.0V ±5% Max	Am2947 MIL T_A = −55 to +125°C, V_{CC} = 5.0V ±10% Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	21	24	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1) R_1 = 1k, R_2 = 5k, C_1 = 30pF	21	24	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	18	21	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	18	21	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from CD to A Port	B_0 to B_7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 30pF	28	33	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from CD to A Port	B_0 to B_7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3) S_3 = 0, R_5 = 5k, C_4 = 30pF	28	33	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	28	34	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	22	25	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	28	34	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	22	25	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 1k, C_4 = 15pF	23	26	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 15pF	18	21	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from CD to B Port	A_0 to A_7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	38	43	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	26	30	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from CD to B Port	A_0 to A_7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) S_3 = 0, R_5 = 1k, C_4 = 300pF	38	43	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	26	30	ns
TRANSMIT RECEIVE MODE SPECIFICATIONS					
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 100Ω, C_3 = 5pF S_2 = 1, R_3 = 1k, C_2 = 30pF	42	48	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to A Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 5pF S_2 = 0, R_3 = 5k, C_2 = 30pF	42	48	ns
t_{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 1, R_4 = 100Ω, C_3 = 300pF S_2 = 1, R_3 = 300Ω, C_2 = 5pF	45	51	ns
t_{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1", T/$\overline{R}$ to B Port	CD = 0.4V (Figure 2) S_1 = 0, R_4 = 1k, C_3 = 300pF S_2 = 1, R_3 = 300Ω, C_2 = 5pF	45	51	ns

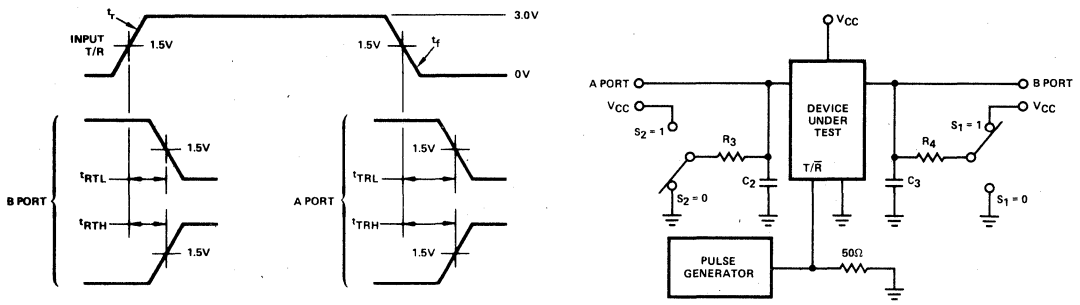
SWITCHING TIME WAVEFORMS AND AC TEST CIRCUITS



$t_r = t_f < 10ns$
10% to 90%

Note: C_1 includes test fixture capacitance.

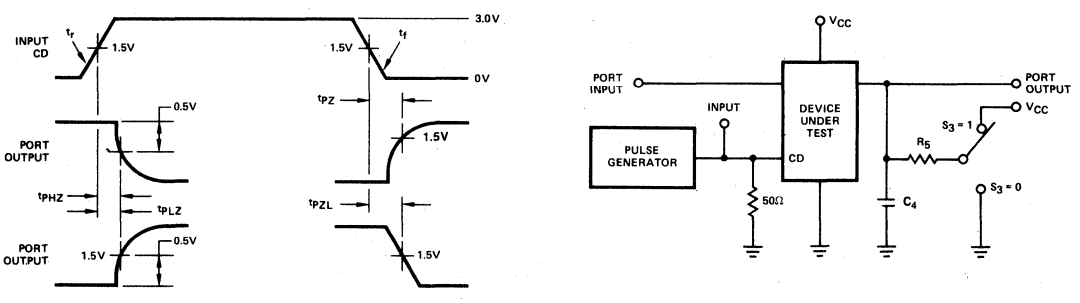
Figure 1. Propagation Delay from A Port to B Port or from B Port to A Port.



$t_r = t_f < 10ns$
10% to 90%

Note: C_2 and C_3 include test fixture capacitance.

Figure 2. Propagation Delay from $\overline{T/R}$ to A Port or B Port.



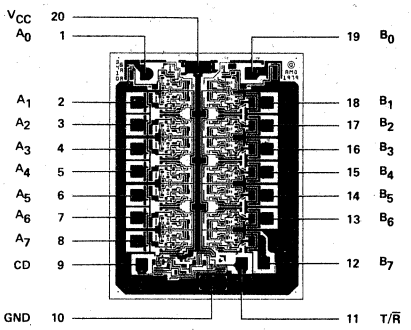
$t_r = t_f < 10ns$
10% to 90%

Note: C_4 includes test fixture capacitance.
Port input is in a fixed logical condition.

Figure 3. Propagation Delay from CD to A Port or B Port.

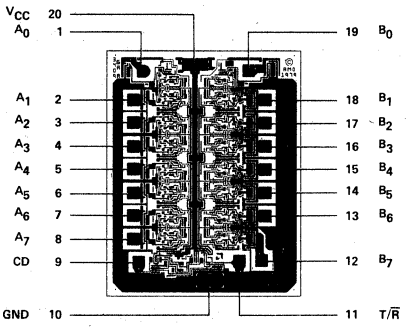
Metallization and Pad Layouts

Am2946



DIE SIZE .069" X .089"

Am2947



DIE SIZE .069" X .089"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2946 Order Number	Am2947 Order Number	Package Type (Note 1)	Operating (Note 2)	Screening Level (Note 3)
AM2946PC	AM2947PC	D-20-1	C	C-1
AM2946DC	AM2947DC	D-20-1	C	C-1
AM2946DC-B	AM2947DC-B	D-20-1	C	B-1
AM2946DM	AM2947DM	D-20-1	M	C-3
AM2946DM-B	AM2947DM-B	D-20-1	M	B-3
AM2946XC	AM2947XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to 70°C, V_{CC} = 4.75V to 5.25V, M = −55 to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

Am2948 • Am2949

Octal Three-State Bidirectional Bus Transceivers

DISTINCTIVE CHARACTERISTICS

- 8-bit bidirectional data flow reduces system package count
- 3-state inputs/outputs for interfacing with bus-oriented systems
- PNP inputs reduce input loading
- V_{CC} – 1.15V V_{OH} interfaces with TTL, MOS, and CMOS
- 48mA, 300pF bus drive capability
- Am2948 has inverting tranceivers
- Am2949 has noninverting transceivers
- Separate $\overline{\text{TRANSMIT}}$ and $\overline{\text{RECEIVE}}$ Enables
- 20 pin ceramic and molded DIP package
- Low power – 8mA per bidirectional bit
- Advanced Schottky processing
- Bus port stays in hi-impedance state during power up/down

GENERAL DESCRIPTION

The Am2948 and Am2949 are 8-bit, 3-state Schottky transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 24mA drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

Separate $\overline{\text{TRANSMIT}}$ and $\overline{\text{RECEIVE}}$ Enables are provided for microprocessor system with separated read and write control bus lines.

The output high voltage (V_{OH}) is specified at V_{CC} – 1.15V minimum to allow interfacing with MOS, CMOS, TTL, ROM, RAM, or microprocessors.

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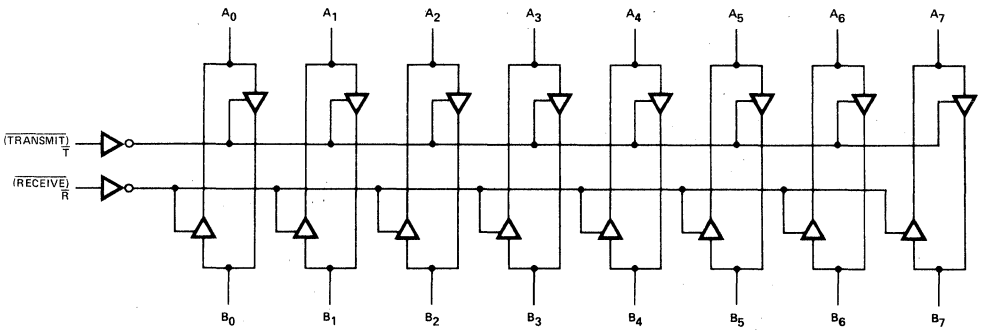
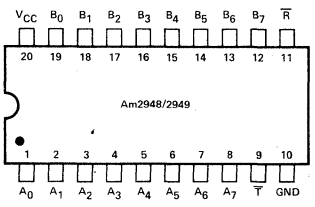
Am2949
LOGIC DIAGRAM



Am2948 has inverting transceivers.

BLI-177

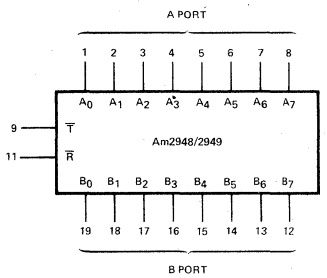
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.
Am2948 is inverting from Ai to Bi

BLI-108

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

BLI-109

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Lead Temperature (Soldering, 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:

MIL	T_A = −55 to +125°C	V_{CC} MIN = 4.5V	V_{CC} MAX = 5.5V
COM'L	T_A = 0 to +70°C	V_{CC} MIN = 4.75V	V_{CC} MAX = 5.25V

DC ELECTRICAL CHARACTERISTICS over operating temperature range

Parameters	Description		Test Conditions			Min	Typ (Note 1)	Max	Units
A PORT (A_0-A_7)									
V_{IH}	Logical "1" Input Voltage		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V			2.0			Volts
V_{IL}	Logical "0" Input Voltage		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V		COM'L			0.8	Volts
					MIL			0.7	
V_{OH}	Logical "1" Output Voltage		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V	I_{OH} = −0.4mA		V_{CC}−1.15	V_{CC}−0.7		Volts
				I_{OH} = −3.0mA		2.7	3.95		
V_{OL}	Logical "0" Output Voltage		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V	I_{OL} = 12mA			0.3	0.4	Volts
				COM'L	I_{OL} = 24mA		0.35	0.50	
I_{OS}	Output Short Circuit Current		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V, V_O = 0V, V_{CC} = MAX, Note 2			−10	−38	−75	mA
I_{IH}	Logical "1" Input Current		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V, V_I = 2.7V				0.1	80	μA
I_I	Input Current at Maximum Input Voltage		$\overline{T}$ = $\overline{R}$ = 2.0V, V_{CC} = MAX, V_I = V_{CC} MAX					1	mA
I_{IL}	Logical "0" Input Current		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V, V_I = 0.4V				−70	−200	μA
V_C	Input Clamp Voltage		$\overline{T}$ = $\overline{R}$ = 2.0V, I_{IN} = −12mA				−0.7	−1.5	Volts
I_{OD}	Output/Input 3-State Current		$\overline{T}$ = $\overline{R}$ = 2.0V	V_O = 0.4V				−200	μA
				V_O = 4.0V				80	
B PORT (B_0-B_7)									
V_{IH}	Logical "1" Input Voltage		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V			2.0			Volts
V_{IL}	Logical "0" Input Voltage		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V		COM'L			0.8	Volts
					MIL			0.7	
V_{OH}	Logical "1" Output Voltage		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V	I_{OH} = −0.4mA		V_{CC}−1.15	V_{CC}−0.8		Volts
				I_{OH} = −5.0mA		2.7	3.9		
				I_{OH} = −10mA		2.4	3.6		
V_{OL}	Logical "0" Output Voltage		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V	I_{OL} = 20mA			0.3	0.4	Volts
				I_{OL} = 48mA			0.4	0.5	
I_{OS}	Output Short Circuit Current		$\overline{T}$ = 0.8V, $\overline{R}$ = 2.0V, V_O = 0V V_{CC} = MAX, Note 2			−25	−50	−150	mA
I_{IH}	Logical "1" Input Current		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V, V_I = 2.7V				0.1	80	μA
I_I	Input Current at Maximum Input Voltage		$\overline{T}$ = $\overline{R}$ = 2.0V, V_{CC} = MAX, V_I = V_{CC} MAX					1	mA
I_{IL}	Logical "0" Input Current		$\overline{T}$ = 2.0V, $\overline{R}$ = 0.8V, V_I = 0.4V				−70	−200	μA
V_C	Input Clamp Voltage		$\overline{T}$ = $\overline{R}$ = 2.0V, I_{IN} = −12mA				−0.7	−1.5	Volts
I_{OD}	Output/Input 3-State Current		$\overline{T}$ = $\overline{R}$ = 2.0V	V_O = 0.4V				−200	μA
				V_O = 4.0V				200	
CONTROL INPUTS $\overline{T}$, $\overline{R}$									
V_{IH}	Logical "1" Input Voltage					2.0			Volts
V_{IL}	Logical "0" Input Voltage				COM'L			0.8	Volts
					MIL			0.7	
I_{IH}	Logical "1" Input Current		V_I = 2.7V				0.5	20	μA
I_I	Input Current at Maximum Input Voltage		V_{CC} = MAX, V_I = V_{CC} MAX					1.0	mA
I_{IL}	Logical "0" Input Current		V_I = 0.4V		$\overline{R}$		−0.1	−0.25	mA
					$\overline{T}$		−0.25	−0.5	
V_C	Input Clamp Voltage		I_{IN} = −12mA				−0.8	−1.5	Volts
POWER SUPPLY CURRENT									
I_{CC}	Power Supply Current	Am2948	$\overline{T}$ = $\overline{R}$ = 2.0V, V_I = 2.0V, V_{CC} = MAX				70	100	mA
			$\overline{T}$ = 0.4V, V_{INA} = $\overline{R}$ = 2.0V, V_{CC} = MAX				100	150	
		Am2949	$\overline{T}$ = $\overline{R}$ = 2.0V, V_I = 0.4V, V_{CC} = MAX				70	100	mA
			$\overline{T}$ = V_{INA} = 0.4V, $\overline{R}$ = 2.0V, V_{CC} = MAX				90	140	

Am2948
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C)

Parameter	Description	Test Conditions	Typ	Max	Units
	A PORT DATA/MODE SPECIFICATIONS				
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	8	12	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	11	16	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	10	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 30pF	20	27	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 5k, C_4 = 30pF	20	27	ns
	B PORT DATA/MODE SPECIFICATIONS				
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	12	18	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	8	12	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	15	20	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	9	14	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	25	35	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	18	25	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 300pF	25	35	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	16	25	ns

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FUNCTION TABLE

Control Inputs		Resulting Conditions	
Transmit	**Receive**	**A Port**	**B Port**
1	0	Out	In
0	1	In	Out
1	1	3-State	3-State
0	0	Both Active*	

*This is not an intended logic condition and may cause oscillations.

AC ELECTRICAL CHARACTERISTICS over operating range

Parameter	Description	Test Conditions	Am2948 COM'L $T_A = 0$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$ Max	Am2948 MIL $T_A = -55$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$ Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	19	16	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	23	20	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 30pF	35	30	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 5k, C_4 = 30pF	35	30	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	29	24	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	19	16	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	30	25	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	22	19	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	26	23	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	43	38	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	33	28	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 300pF	43	38	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	33	28	ns

Am2949
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V, T_A = 25°C)

Parameter	Description	Test Conditions	Typ	Max	Units
	A PORT DATA/MODE SPECIFICATIONS				
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	14	18	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	13	18	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	11	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 30pF	20	27	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 5k, C_4 = 30pF	20	27	ns
	B PORT DATA/MODE SPECIFICATIONS				
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	18	23	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	11	18	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	16	23	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	11	18	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	8	15	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	25	35	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	17	25	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 300pF	24	35	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	17	25	ns

DEFINITION OF FUNCTIONAL TERMS

A_0-A_7 A port inputs/outputs are receiver output drivers when $\overline{Receive}$ is LOW and $\overline{Transmit}$ is HIGH, and are transmit inputs when $\overline{Receive}$ is HIGH and $\overline{Transmit}$ is LOW.

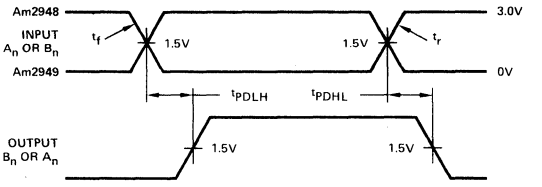
B_0-B_7 B port inputs/outputs are transmit output drivers when $\overline{Transmit}$ is LOW and $\overline{Receive}$ is HIGH, and are receiver inputs when $\overline{Transmit}$ is HIGH and $\overline{Receive}$ is LOW.

$\overline{Transmit}$, $\overline{Receive}$ These controls determine whether A port and B port drivers are in 3-state. With both $\overline{Transmit}$ and $\overline{Receive}$ HIGH both ports are in 3-state. $\overline{Transmit}$ and $\overline{Receive}$ both LOW activate both drivers and may cause oscillations. This is not an intended logic condition. With $\overline{Transmit}$ HIGH and $\overline{Receive}$ LOW A port is the output and B port is the input. With $\overline{Transmit}$ LOW and $\overline{Receive}$ HIGH B port is the output and A port is the input.

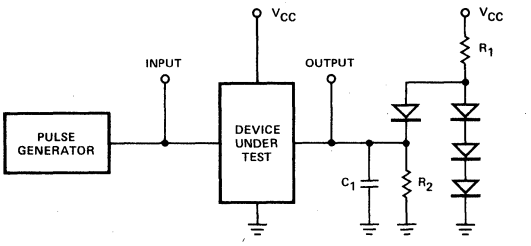
AC ELECTRICAL CHARACTERISTICS over operating range

Parameter	Description	Test Conditions	Am2949 COM'L $T_A = 0$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$ Max	Am2949 MIL $T_A = -55$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$ Max	Units
A PORT DATA/MODE SPECIFICATIONS					
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	24	21	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (Figure A) R_1 = 1k, R_2 = 5k, C_1 = 30pF	24	21	ns
t_{PLZA}	Propagation Delay from a Logical "0" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PHZA}	Propagation Delay from a Logical "1" to 3-State from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PZLA}	Propagation Delay from 3-State to a Logical "0" from $\overline{R}$ to A Port	B_0 to B_7 = 0.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 30pF	35	30	ns
t_{PZHA}	Propagation Delay from 3-State to a Logical "1" from $\overline{R}$ to A Port	B_0 to B_7 = 2.4V, $\overline{T}$ = 2.4V (Figure B) S_3 = 0, R_5 = 5k, C_4 = 30pF	35	30	ns
B PORT DATA/MODE SPECIFICATIONS					
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	34	28	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	25	22	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (Figure A) R_1 = 100Ω, R_2 = 1k, C_1 = 300pF	34	28	ns
		R_1 = 667Ω, R_2 = 5k, C_1 = 45pF	25	22	ns
t_{PLZB}	Propagation Delay from a Logical "0" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 1k, C_4 = 15pF	26	23	ns
t_{PHZB}	Propagation Delay from a Logical "1" to 3-State from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 15pF	21	18	ns
t_{PZLB}	Propagation Delay from 3-State to a Logical "0" from $\overline{T}$ to B Port	A_0 to A_7 = 0.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 1, R_5 = 100Ω, C_4 = 300pF	43	38	ns
		S_3 = 1, R_5 = 667Ω, C_4 = 45pF	33	28	ns
t_{PZHB}	Propagation Delay from 3-State to a Logical "1" from $\overline{T}$ to B Port	A_0 to A_7 = 2.4V, $\overline{R}$ = 2.4V (Figure B) S_3 = 0, R_5 = 1k, C_4 = 300pF	43	38	ns
		S_3 = 0, R_5 = 5k, C_4 = 45pF	33	28	ns

SWITCHING TIME WAVEFORMS AND AC TEST CIRCUITS

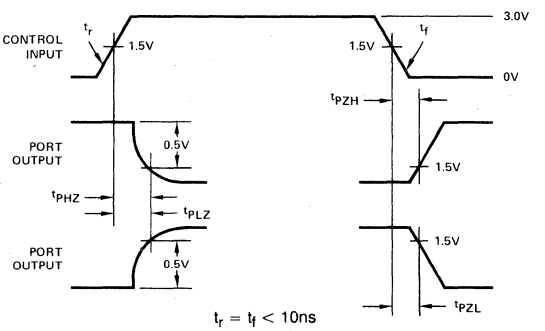


$t_r = t_f < 10ns$
10% to 90%

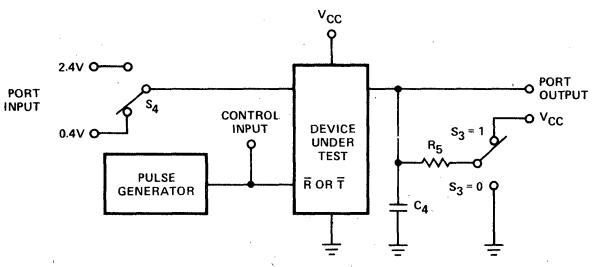


Note: C_1 includes test fixture capacitance.

Figure A. Propagation Delay from A Port to B Port or from B Port to A Port



$t_r = t_f < 10ns$
10% to 90%

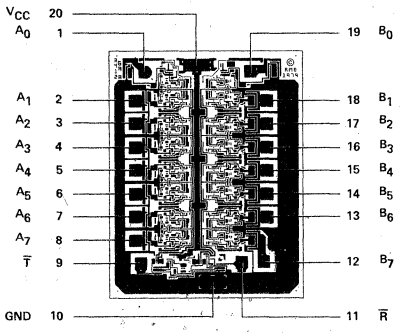


Note: C_4 includes test fixture capacitance. Port input is in a fixed logical condition. See AC table.

Figure B. Propagation Delay to/from Three-State from $\overline{R}$ to A Port and $\overline{T}$ to B Port

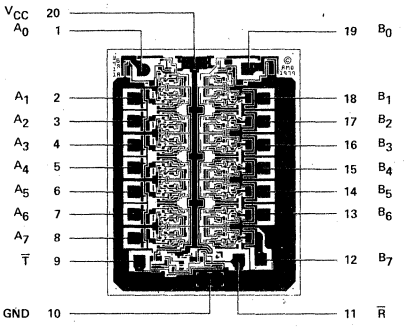
Metallization and Pad Layouts

Am2948



DIE SIZE .069" X .089"

Am2949



DIE SIZE .069" X .089"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2948 Order Number	Am2949 Order Number	Package Type (Note 1)	Operating (Note 2)	Screening Level (Note 3)
AM2948PC	AM2949PC	P-20-1	C	C-1
AM2948DC	AM2949DC	D-20-1	C	C-1
AM2948DC-B	AM2949DC-B	D-20-1	C	B-1
AM2948DM	AM2949DM	D-20-1	M	C-3
AM2948DM-B	AM2949DM-B	D-20-1	M	B-3
AM2948XC	AM2949XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to 70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

Am2950 • Am2950A
Am2951 • Am2951A

Eight-Bit Bidirectional I/O Ports with Handshake

DISTINCTIVE CHARACTERISTICS

- Eight-Bit, Bidirectional I/O Port with Handshake – Two eight-bit, back-to-back registers store data moving in both directions between two bidirectional busses.
- Register Full/Empty Flags – On-chip flag flip-flops provide data transfer handshaking signals.
- Separate Clock, Clock Enable and Three-State Output Enable for Each Register.
- Separate, Edge-Sensitive Clear Control for Each Flag Flip-Flop.
- Inverting and Non-Inverting Versions – The Am2950 provides non-inverting data outputs. The Am2951 provides inverting data outputs.
- 24mA Output Current Sink Capability.
- Fast – The Am2950A and Am2951A will be 25 – 30% faster than the Am2950 and Am2951.

GENERAL DESCRIPTION

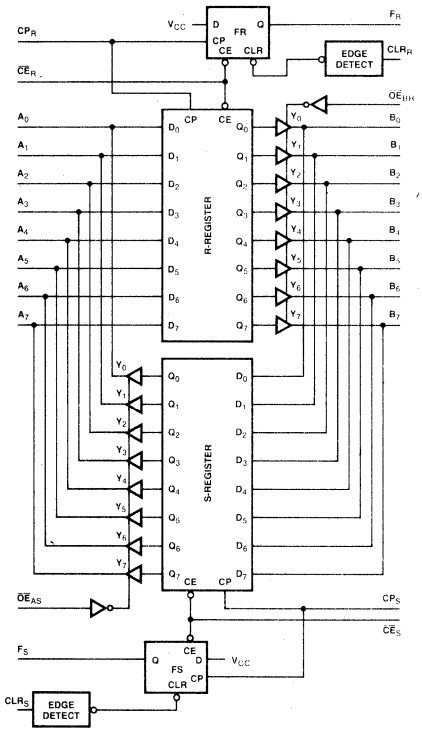
The Am2950 and Am2951, members of Advanced Micro Devices Am2900 Family, are designed for use as parallel data I/O ports. Two eight-bit, back to back registers store data moving in both directions between two bidirectional, 3-state busses. On chip flag flip-flops, set automatically when a register is loaded, provide the handshaking signals required for demand-response data transfer.

Considerable flexibility is designed into the Am2950 • Am2951. Separate clock, clock enable and three-state output enable signals are provided for each register, and edge-sensitive clear inputs are provided for each flag flip-flop. A number of these circuits can be used for wider I/O ports. Both inverting and non-inverting versions are available.

Twenty-four mA output current sink capability, sufficient for most three-state busses, is provided by the Am2950 • Am2951.

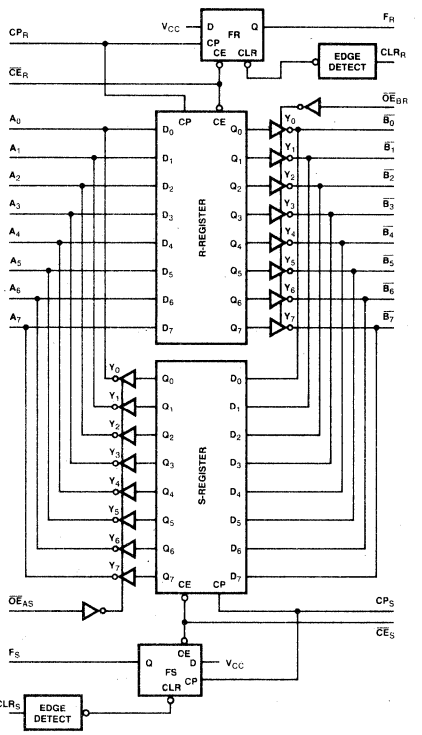
The Am2950A and Am2951A feature AMD's ion-implanted micro-oxide (IMOX™) processing. They are plug-in replacements for the Am2950 and Am2951 respectively but will be approximately 30% faster.

Am2950 BLOCK DIAGRAM



MPR-573

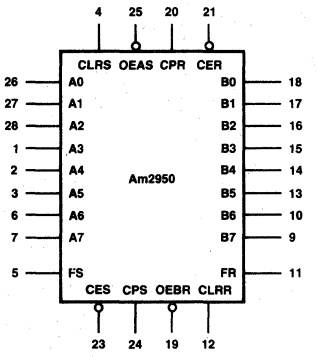
Am2951 BLOCK DIAGRAM



MPR-574

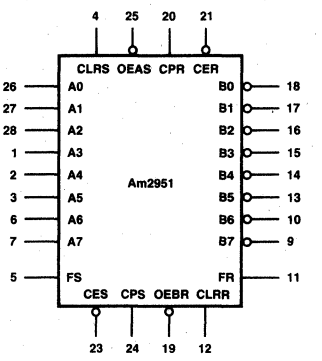
LOGIC SYMBOLS

Am2950



MPR-575

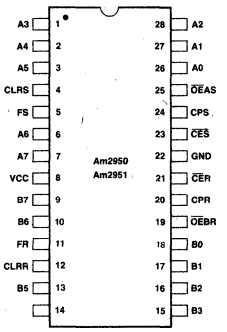
Am2951



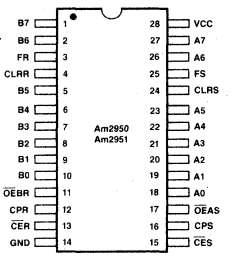
MPR-576

CONNECTION DIAGRAMS
Top Views

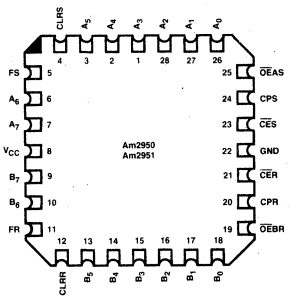
D-28, P-28



F-28-2



Leadless Chip Carrier
L-28-1



Note: Pin 1 is marked for orientation.
Bi is inverted on Am2951.

MPR-577

MPR-585

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Am2950A Order Number (Note 5)	Am2951A Order Number (Note 5)	Am2950 Order Number	Am2951 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2950APC	AM2951APC	AM2950PC	AM2951PC	P-28	C	C-1
AM2950ADC	AM2951ADC	AM2950DC	AM2951DC	D-28	C	C-1
AM2950ADC-B	AM2951ADC-B	AM2950DC-B	AM2951DC-B	D-28	C	B-2 (Note 4)
AM2950ADM	AM2951ADM	AM2950DM	AM2951DM	D-28	M	C-3
AM2950ADM-B	AM2951ADM-B	AM2950DM-B	AM2951DM-B	D-28	M	B-3
AM2950AFM	AM2951AFM	AM2950FM	AM2951FM	F-28-2	M	C-3
AM2950AFM-B	AM2950AFM-B	AM2950FM-B	AM2951FM-B	F-28-2	M	B-3
AM2950ALC	AM2951ALC	AM2950LC	AM2951LC	L-28	C	C-1
AM2950ALM	AM2951ALM	AM2950LM	AM2951LM	L-28	C	C-3
AM2950ALM-B	AM2951ALM-B	AM2950LM-B	AM2951LM-B	L-28	M	B-3
AM2950AXC	AM2951AXC	AM2950XC	AM2951XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2950AXM	AM2951AXM	AM2950XM	AM2951XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.
5. When available.

REGISTER FUNCTION TABLE
(Applies to R or S Register)

Inputs			Internal	
D	CP	$\overline{CE}$	Q	Function
X	X	H	NC	Hold Data
L	↑	L	L	Load Data
H	↑	L	H	

OUTPUT CONTROL

	Internal	Y-Outputs		
$\overline{OE}$	Q	Am2950	Am2951	Function
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

FLAG FLIP-FLOP FUNCTION TABLE
(Applies to R or S Flag Flip-Flop)

Inputs			F-Output	Function
$\overline{CE}$	CP	CLR		
H	X	↑	NC	Hold Flag
X	X	↑	L	Clear Flag
L	↑	↑	H	Set Flag

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance
NC = NO CHANGE
↑ = LOW-to-HIGH Transition
↑ = NO LOW-to-HIGH Transition

5

DEFINITION OF FUNCTIONAL TERMS

A0-7 Eight bidirectional lines carrying the R Register inputs or S Register outputs.

B0-7 Eight bidirectional lines carrying the S Register inputs or R Register outputs.

CPR The clock for the R Register and FR Flip-Flop. When $\overline{CE}$R is LOW, data is entered into the R Register and the FR Flip-Flop is set on the LOW to HIGH transition of the CPR signal.

$\overline{CE}$R The Clock Enable for the R Register and FR Flip-Flop. When $\overline{CE}$R is LOW, data is entered into the R Register and the FR Flip-Flop is set on the LOW to HIGH transition of the CPR signal. When $\overline{CE}$R is HIGH, The R Register and FR Flip-Flop hold their contents, regardless of CPR signal transitions.

$\overline{OE}$BR The Output Enable for the R Register. When $\overline{OE}$BR is LOW, The R Register three-state outputs are enabled onto the B0-7 lines. When $\overline{OE}$BR is HIGH, the R Register outputs are in the high-impedance state.

FR The FR Flip-Flop output.

CLRR The clear control for the FR Flip-Flop. The FR Flip-Flop is cleared on the LOW to HIGH transition of CLRR signal.

CPS The clock for the S Register and FS Flip-Flop. When $\overline{CE}$S is LOW, data is entered into the S Register and the FS Flip-Flop is set on the LOW to HIGH transtion of the CPS signal.

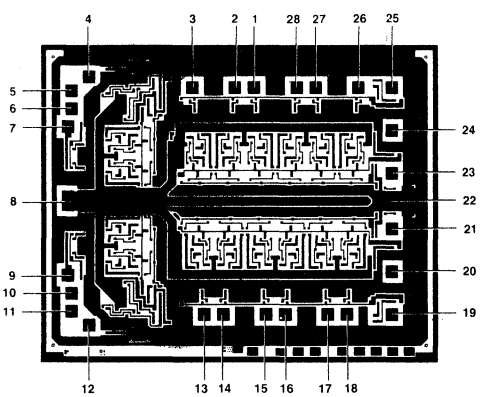
$\overline{CE}$S The clock enable for the S Register and FS Flip-Flop. When $\overline{CE}$S is LOW, data is entered into the S Register and the FS Flip-Flop is set on the LOW to HIGH transition of the CPS signal. When $\overline{CE}$S is HIGH, the S Register and FS Flip-Flop hold their contents, regardless of CPS signal transitions.

$\overline{OE}$AS The output enable for the S Register. When $\overline{OE}$AS is LOW, the S Register three-state outputs are enabled onto the A0-7 lines. When OEAS is HIGH, the S Register outputs are in the high-impedance state.

FS The FS Flip-Flop output.

CLRS The clear control for the FS Flip-Flop. The FS Flip-Flop is cleared on the LOW to HIGH transition of CLRS signal.

METALLIZATION AND PAD LAYOUT



Numbers refer to DIP pin connection
DIE SIZE 0.107" X 0.138"

Am2950/50A/51/51A

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +VCC max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

OPERATING RANGE

Part Number	Range	Temperature	VCC
Am2950/51PC, DC	COM'L	T_A = 0°C to +70°C	VCC = 5.0V ±5% (MIN. = 4.75V, MAX. =5.25V)
Am2950/51DM, FM	MIL	TC = −55°C to +125°C	VCC = 5.0V ±10% (MIN. = 4.50V, MAX. = 5.50V)

Am2950, Am2951

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
VOH	Output HIGH Voltage	VCC = MIN. VIN = VIH or VIL	FR, FS	IOH = −1mA	2.4	3.4		Volts
			A0-7, B0-7	MIL, IOH = −2mA	2.4	3.4		
				COM'L, IOH = −6.5mA	2.4	3.4		
VOL	Output LOW Voltage	VCC = MIN. VIN = VIH or VIL	FR, FS	IOL = 12mA			0.5	Volts
			A0-7, B0-7	MIL IOL = 16mA			0.5	
				COM'L IOL = 24mA			0.5	
VIH	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
VIL	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
VI	Input Clamp Voltage	VCC = MIN., IIN = −18mA					−1.5	Volts
IIL	Input LOW Current	VCC = MAX., VIN = 0.5V		A0-7, B0-7			−250	μA
				CLRR, CLRS			−2.0	mA
				Others			−360	μA
IIH	Input HIGH Current	VCC = MAX., VIN = 2.7V		A0-7, B0-7			70	μA
				CLRR, CLRS			100	
				Others			20	
II	Input HIGH Current	VCC = MAX., VIN = 5.5V					1.0	mA
IO	Output Off-state Leakage Current	VCC = MAX.	A0-7, B0-7	V0 = 2.4V			70	μA
				V0 = 0.4V			−250	
ISC	Output Short Circuit Current (Note 3)	VCC = MAX.			−30		−85	mA
ICC	Power Supply Current (Notes 4, 5)	VCC = MAX.		T_A = 25°C		156	263	mA
			COM'L	T_A = 0°C to +70°C			275	
				T_A = +70°C			228	
			MIL	T_C = −55°C to +125°C			309	
				T_C = +125°C			202	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at VCC = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. ICC is measured with all inputs at 4.5V and all outputs open.
5. Worst case ICC is at minimum temperature.

Am2950A • Am2951A SWITCHING CHARACTERISTICS

The tables below define the Am2950A • Am2951A switching characteristics. Tables A are setup and hold times relative to a clock LOW-to-HIGH transition. Tables B are propagational delays. Tables C are recovery times. Tables D are pulse-width requirements. Tables E are enable/disable times. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns with RL on Ai and Bi = 220Ω and RL on FS and FR = 300Ω. CL = 50pF except output disable times which are specified at CL = 5pF.

GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

(T_A = 0 to +70°C, VCC = 4.75 to 5.25V, C_L = 50pF)

A. Set-up and Hold Times.

Input	With Respect To	ts	th
A0-7	CPR ↓		
B0-7	CPS ↓		
$\overline{CES}$	CPS ↓		
$\overline{CER}$	CPR ↓		

B. Propagation Delays

Input	A0-7	B0-7	FS	FR
CPS ↓				
CPR ↓				
CLRS ↓				
CLRR ↓				

C. Recovery Times

From	To	tREC
CLRS ↓	CPS ↓	
CLRR ↓	CPR ↓	

D. Pulse-Width Requirements

Input	Min. LOW Pulse Width	Min. HIGH Pulse Width
CPS		
CPR		
CLRS		
CLRR		

E. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}$AS	A0-7		
$\overline{OE}$BR	B0-7		

*Where two numbers appear, the first is the Am2950A spec, the second is the Am2951A spec.

GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

(T_C = −55 to +125°C, VCC = 4.5 to 5.5V, C_L = 50pF)

A. Set-up and Hold Times.

Input	With Respect To	ts	th
A0-7	CPR ↓		
B0-7	CPS ↓		
$\overline{CES}$	CPS ↓		
$\overline{CER}$	CPR ↓		

B. Propagation Delays

Input	A0-7	B0-7	FS	FR
CPS ↓				
CPR ↓				
CLRS ↓				
CLRR ↓				

C. Recovery Times

From	To	tREC
CLRS ↓	CPS ↓	
CLRR ↓	CPR ↓	

D. Pulse-Width Requirements

Input	Min. LOW Pulse Width	Min. HIGH Pulse Width
CPS		
CPR		
CLRS		
CLRR		

E. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}$AS	A0-7		
$\overline{OE}$BR	B0-7		

*Where two numbers appear, the first is the Am2950A spec, the second is the Am2951A spec.

Am2950 • Am2951 SWITCHING CHARACTERISTICS

The tables below define the Am2950 • Am2951 switching characteristics. Tables A are set-up and hold times relative to a clock LOW-to-HIGH transition. Tables B are propagational delays. Tables C are recovery times. Tables D are pulse-width requirements. Tables E are enable/disable times. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns with RL on Ai and Bi = 220Ω and RL on FS and FR = 300Ω. CL = 50pF except output disable times which are specified at CL = 5pF.

GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

(T_A = 0 to +70°C, VCC = 4.75 to 5.25V, C_L = 50pF)

A. Set-up and Hold Times.

Input	With Respect To	ts	th
A0-7	CPR ↑	7	5
B0-7	CPS ↑	7	5
$\overline{CES}$	CPS ↑	*19/15	4
$\overline{CER}$	CPR ↑	*19/15	4

B. Propagation Delays

Input	A0-7	B0-7	FS	FR
CPS ↑	*30/26	–	20	–
CPR ↑	–	*30/26	–	20
CLRS ↑	–	–	22	–
CLRR ↑	–	–	–	22

C. Recovery Times

From	To	tREC
CLRS ↑	CPS ↑	31
CLRR ↑	CPR ↑	31

D. Pulse-Width Requirements

Input	Min. LOW Pulse Width	Min. HIGH Pulse Width
CPS	20	20
CPR	20	20
CLRS	20	20
CLRR	20	20

E. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}$AS	A0-7	22	27
$\overline{OE}$BR	B0-7	22	27

*Where two numbers appear, the first is the Am2950 spec, the second is the Am2951 spec

GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

(T_C = −55 to +125°C, VCC = 4.5 to 5.5V, C_L = 50pF)

A. Set-up and Hold Times.

Input	With Respect To	ts	th
A0-7	CPR ↑	11	8
B0-7	CPS ↑	11	8
$\overline{CES}$	CPS ↑	*20/15	4
$\overline{CER}$	CPR ↑	*20/15	4

B. Propagation Delays

Input	A0-7	B0-7	FS	FR
CPS ↑	*35/28	–	20	–
CPR ↑	–	*35/28	–	20
CLRS ↑	–	–	22	–
CLRR ↑	–	–	–	22

C. Recovery Times

From	To	tREC
CLRS ↑	CPS ↑	34
CLRR ↑	CPR ↑	34

D. Pulse-Width Requirements

Input	Min. LOW Pulse Width	Min. HIGH Pulse Width
CPS	20	20
CPR	20	20
CLRS	20	20
CLRR	20	20

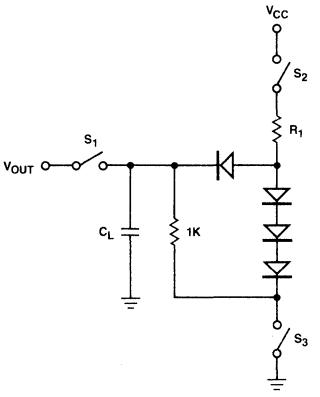
E. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}$AS	A0-7	24	28
$\overline{OE}$BR	B0-7	24	28

*Where two numbers appear, the first is the Am2950 spec, the second is the Am2951 spec

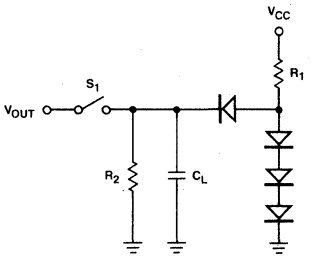
TEST OUTPUT LOAD CONFIGURATIONS FOR Am2950/2951

A. THREE-STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2950/2951 (DIP)

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
–	A_{0-7}	A	220	1K
–	B_{0-7}	A	220	1K
5	FS	B	300	2.4K
11	FR	B	300	2.4K

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5–8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

APPLICATIONS

The Am2950 • Am2951 provides data transfer handshaking signals as well as eight-bit, bidirectional data storage. Its flexibility allows it to be used in any type of computer system, including Am2900, 8080, 8085, 8086, Z80, and Z8000 systems.

Figure 1 shows an Am2950 used to store data moving in both directions between a bidirectional system data bus and a bidirectional peripheral data bus. The on-chip Flag flip-flops provide the data in, data out handshaking signals required for data transfer and interrupt request generation.

Figure 2 shows a multiple I/O port system using Am2950's. Two Am2950's are used at each port to interface the 16-bit system data bus. The Am2950 flags are used to generate I/O interrupt requests.

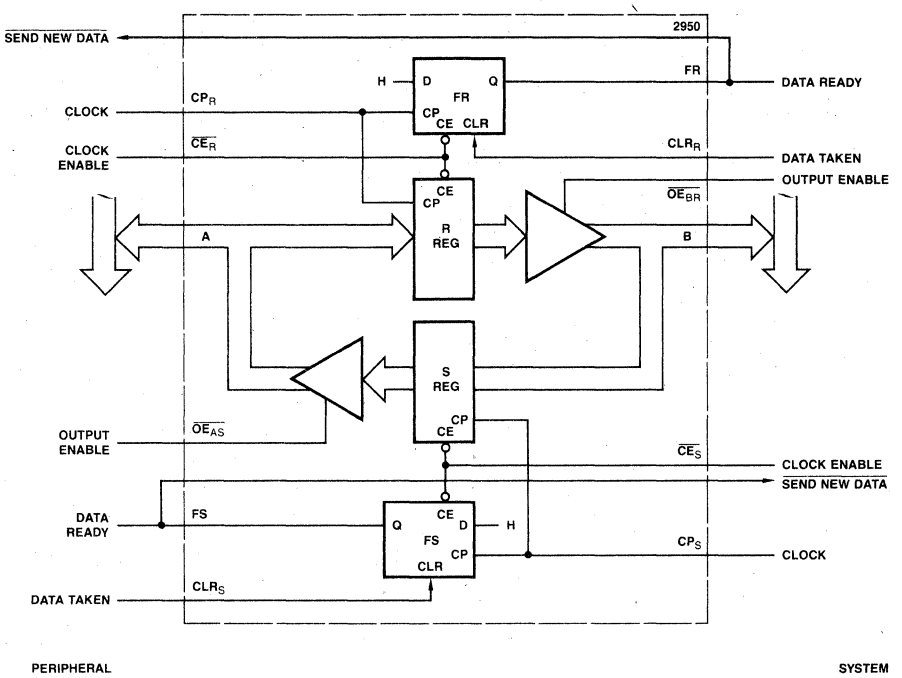


Figure 1. A Bidirectional I/O Port with Handshaking Using the Am2950.

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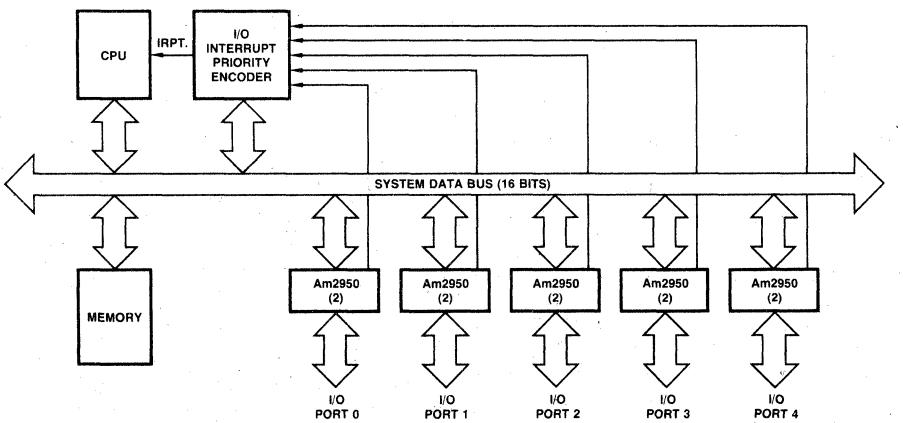


Figure 2. Multiple I/O Port System.

MPR-579

Am2952 • Am2952A
Am2953 • Am2953A

Eight-Bit Bidirectional I/O Ports

DISTINCTIVE CHARACTERISTICS

- Eight-Bit, Bidirectional I/O Port
  Two eight-bit, back-to-back registers store data moving in both directions between two bidirectional busses.
- Separate Clock, Clock Enable and Three-State Output Enable for Each Register.
- Inverting and Non-Inverting Versions –
  The Am2952 provides non-inverting data ouputs. The Am2953 provides inverting data outputs.
- 24mA Output Current Sink Capability.
- 24-Pin Slim Package
- Fast –
  The Am2952A and Am2953A will be 25 – 30% faster than the Am2952 and Am2953.

GENERAL DESCRIPTION

The Am2952 and Am2953, members of Advanced Micro Devices Am2900 Family, are designed for use as parallel data I/O ports. Two eight-bit, back to back registers store data moving in both directions between two bidirectional, 3-state busses.

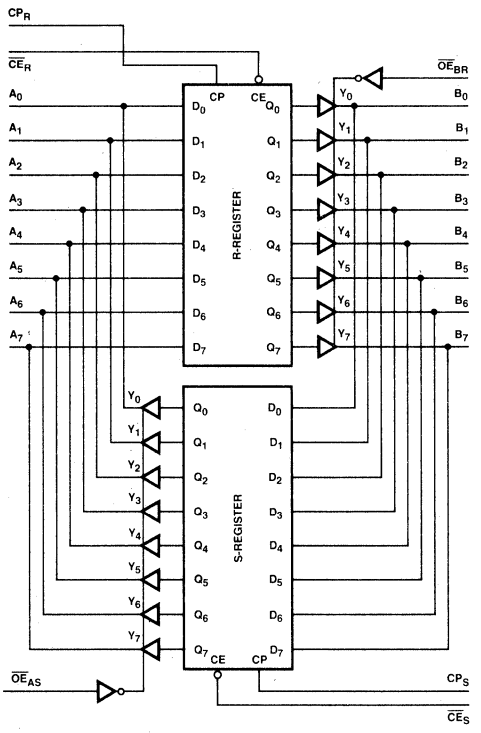
Considerable flexibility is designed into the Am2952 • Am2953. Separate clock, clock enable and three-state output enable signals are provided for each register. A number of these circuits can be used for wider I/O ports. Both inverting and non-inverting versions are available.

Twenty-four mA output current sink capability, sufficient for most three-state busses, is provided by the Am2952 • Am2953.

The Am2952A and Am2953A feature AMD's ion-implanted micro-oxide (IMOX™) processing. They are plug-in replacements for the Am2950 and Am2951 respectively but will be approximately 30% faster.

5

Am2952 BLOCK DIAGRAM



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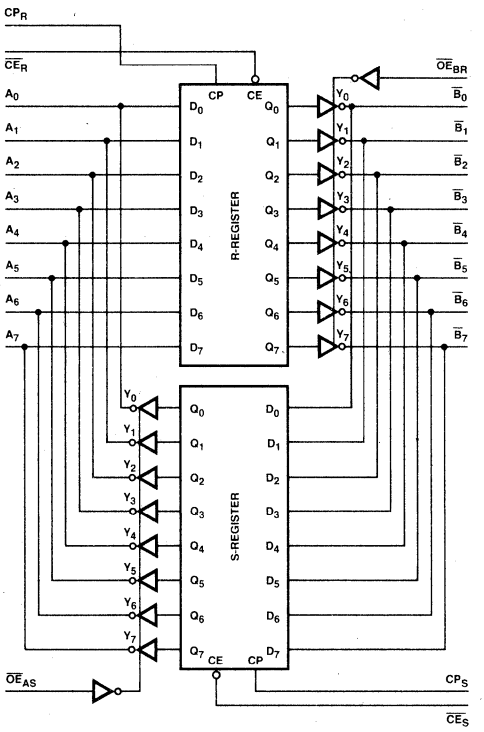
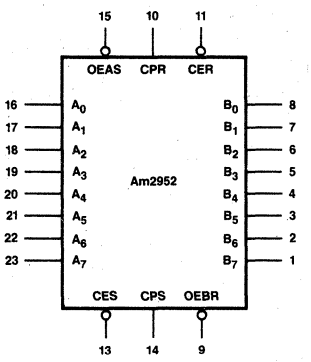
Am2953 BLOCK DIAGRAM



MPR-805

LOGIC SYMBOLS

Am2952



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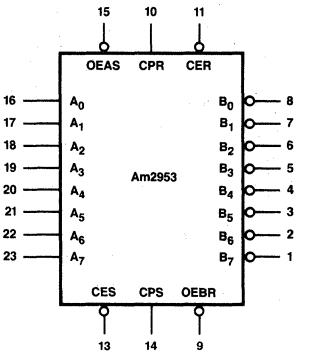
Am2953



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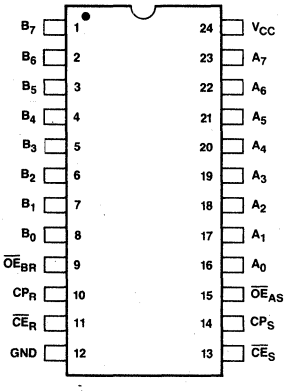
CONNECTION DIAGRAM
Top View
D-24



Note: Pin 1 is marked for orientation.
B_i is inverted on Am2953.

MPR-808

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2952A Order Number (Note 5)	Am2953A Order Number (Note 5)	Am2952 Order Number	Am2953 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2952ADC	AM2953ADC	AM2952DC	AM2953DC	D-24	C	C-1
AM2952ADC-B	AM2953ADC-B	AM2952DC-B	AM2953DC-B	D-24	C	B-2 (Note 4)
AM2952ADM	AM2953ADM	AM2952DM	AM2953DM	D-24	M	C-3
AM2952ADM-B	AM2953ADM-B	AM2952DM-B	AM2953DM-B	D-24	M	B-3
AM2952AXC	AM2953AXC	AM2952XC	AM2953XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2952AXM	AM2953AXM	AM2952XM	AM2953XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to 70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.
5. When available.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +VCC max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

OPERATING RANGE

Part Number	Range	Temperature	V_{CC}	
Am2952/53DC	COM'L	T_A = 0 to +70°C	V_{CC} = 5.0V ±5%	(MIN = 4.75V, MAX = 5.25V)
Am2952/53DM	MIL	T_C = −55 to +125°C	V_{CC} = 5.0V ±10%	(MIN = 4.50V, MAX = 5.50V)

5

Am2952, Am2953
DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min	Typ. (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	A_{0-7}, B_{0-7}	MIL, I_{OH} = −2mA	2.4	3.4		Volts
				COM'L, I_{OL} = −6.5mA	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	A_{0-7}, B_{0-7}	MIL, I_{OL} = 16mA			0.5	Volts
				COM'L, I_{OL} = 24mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V		A_{0-7}, B_{0-7}			−250	μA
				Others			−360	μA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		A_{0-7}, B_{0-7}			70	μA
				Others			20	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_O	Output Off-state Leakage Current	V_{CC} = MAX	A_{0-7}, B_{0-7}	V_O = 2.4V			70	μA
				V_O = 0.4V			−250	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−30		−85	mA
I_{CC}	Power Supply Current (Notes 4, 5)	V_{CC} = MAX		T_A = 25°C		156	263	mA
			COM'L	T_A = 0 to +70°C			275	
				T_A = +70°C			228	
			MIL	T_C = −55 to +125°C			309	
				T_C = +125°C			202	

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} is measured with all inputs at 4.5V and all outputs open.
5. Worst case I_{CC} is at minimum temperature.

Am2952A • Am2953A SWITCHING CHARACTERISTICS

The tables below define the Am2952A • Am2953A switching characteristics. Tables A are setup and hold times relative to a clock LOW-to-HIGH transition. Tables B are propagational delays. Tables C are pulse-width requirements. Tables D are enable/disable times. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns with R_L on A_i and B_i = 220Ω and R_L on FS and FR = 300Ω. C_L = 50pF except output disable times which are specified at C_L = 5pF.

GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

(T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V, C_L = 50pF)

A. Set-up and Hold Times

Input	With Respect to	t_s	t_h
A_{0-7} ↓	CPR		
B_{0-7} ↓	CPS		
$\overline{CES}$ ↓	CPS		
$\overline{CER}$ ↓	CPR		

B. Propagation Delays

Input	A_{0-7}	B_{0-7}
CPS ↓		
CPR ↓		

C. Pulse-Width Requirements

Input	Min. LOW Pulse Width	Min. HIGH Pulse Width
CPS		
CPR		

D. Enable/Disable Times

From	To	Disable	Enable
$\overline{OEAS}$	A_{0-7}		
$\overline{OEBR}$	B_{0-7}		

*Where two numbers appear, the first is the Am2952A spec, the second is the Am2953A spec.

GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

(T_C = −55 to +125°C, V_{CC} = 4.5 to 5.5V, C_L = 50pF)

A. Set-up and Hold Times

Input	With Respect to	t_s	t_h
A_{0-7} ↓	CPR		
B_{0-7} ↓	CPS		
$\overline{CES}$ ↓	CPS		
$\overline{CER}$ ↓	CPR		

B. Propagation Delays

Input	A_{0-7}	B_{0-7}
CPS ↓		
CPR ↓		

C. Pulse-Width Requirements

Input	Min. LOW Pulse Width	Min. HIGH Pulse Width
CPS		
CPR		

D. Enable/Disable Times

From	To	Disable	Enable
$\overline{OEAS}$	A_{0-7}		
$\overline{OEBR}$	B_{0-7}		

*Where two numbers appear, the first is the Am2952A spec, the second is the Am2953A spec.

Am2952 • Am2953 SWITCHING CHARACTERISTICS

The tables below define the Am2952 • Am2953 switching characteristics. Tables A are set-up and hold times relative to a clock LOW-to-HIGH transition. Tables B are propagational delays. Tables C are pulse-width requirements. Tables D are enable/disable times. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns with R_L on A_i and B_i = 220Ω and R_L on FS and FR = 300Ω. C_L = 50pF except output disable times which are specified at C_L = 5pF.

GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

(T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V, C_L = 50pF)

A. Set-up and Hold Times

Input	With Respect to	t_s	t_h
A_{0-7} ↓	CPR	7	5
B_{0-7} ↓	CPS	7	5
$\overline{CES}$ ↓	CPS	*19/15	4
$\overline{CER}$ ↓	CPR	*19/15	4

B. Propagation Delays

Input	A_{0-7}	B_{0-7}
CPS ↓	*30/26	–
CPR ↓	–	*30/26

C. Pulse-Width Requirements

Input	Min. LOW Pulse Width	Min. HIGH Pulse Width
CPS	20	20
CPR	20	20

D. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}$AS	A_{0-7}	22	27
$\overline{OE}$BR	B_{0-7}	22	27

*Where two numbers appear, the first is the Am2952 spec, the second is the Am2953 spec

GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

(T_C = −55 to+125°C, V_{CC} = 4.5 to 5.5V, C_L = 50pF)

A. Set-up and Hold Times

Input	With Respect to	t_s	t_h
A_{0-7} ↓	CPR	11	8
B_{0-7} ↓	CPS	11	8
$\overline{CES}$ ↓	CPS	*20/15	4
$\overline{CER}$ ↓	CPR	*20/15	4

B. Propagation Delays

Input	A_{0-7}	B_{0-7}
CPS ↓	*35/28	–
CPR ↓	–	*35/28

C. Pulse-Width Requirements

Input	Min. LOW Pulse Width	Min. HIGH Pulse Width
CPS	20	20
CPR	20	20

D. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}$AS	A_{0-7}	24	28
$\overline{OE}$BR	B_{0-7}	24	28

*Where two numbers appear, the first is the Am2952 spec, the second is the Am2953 spec

REGISTER FUNCTION TABLE
(Applies to R or S Register)

Inputs			Internal	
D	CP	$\overline{CE}$	Q	Function
X	X	H	NC	Hold Data
L	↑	L	L	Load Data
H	↑	L	H	

OUTPUT CONTROL

	Internal	Y-Outputs		
$\overline{OE}$	Q	Am2950	Am2951	Function
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

DEFINITION OF FUNCTIONAL TERMS

A0-7 Eight bidirectional lines carrying the R Register inputs or S Register outputs.

B0-7 Eight bidirectional lines carrying the S Register inputs or R Register outputs.

CPR The clock for the R Register. When $\overline{CER}$ is LOW, data is entered into the R Register on the LOW to HIGH transition of the CPR signal.

$\overline{CER}$ The Clock Enable for the R Register. When $\overline{CER}$ is LOW, data is entered into the R Register on the LOW to HIGH transition of the CPR signal. When $\overline{CER}$ is HIGH, the R Register holds its contents, regardless of CPR signal transitions.

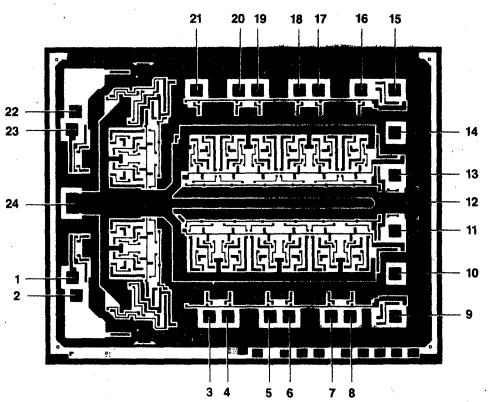
$\overline{OEBR}$ The Output Enable for the R Register. When $\overline{OEBR}$ is LOW, The R Register three-state outputs are enabled onto the B0-7 lines. When $\overline{OEBR}$ is HIGH, the R Register outputs are in the high-impedance state.

CPS The clock for the S Register. When $\overline{CES}$ is LOW, data is entered into the S Register on the LOW to HIGH transition of the CPS signal.

$\overline{CES}$ The clock enable for the S Register. When $\overline{CES}$ is LOW, data is entered into the S Register on the LOW to HIGH transition of the CPS signal. When $\overline{CES}$ is HIGH, the S Register holds its contents, regardless of CPS signal transitions.

$\overline{OEAS}$ The output enable for the S Register. When $\overline{OEAS}$ is LOW, the S Register three-state outputs are enabled onto the A0-7 lines. When OEAS is HIGH, the S Register outputs are in the high-impedance state.

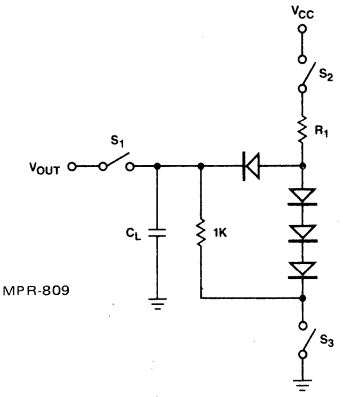
METALLIZATION AND PAD LAYOUT



DIE SIZE 0.107" X 0.138"

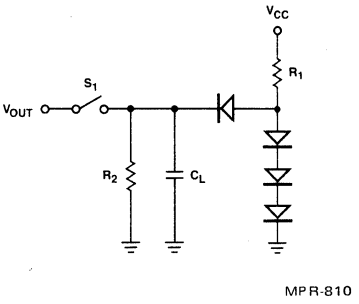
TEST OUTPUT LOAD CONFIGURATIONS FOR Am2952/Am2953

A. THREE-STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am2952/2953

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
–	A_{0-7}	A	220	1K
–	B_{0-7}	A	220	1K

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5–8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

Am2954 • Am2955

Octal Registers with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Eight-bit, high-speed parallel registers
- Am2954 has non-inverting inputs
- Am2955 has inverting inputs
- Positive, edge-triggered, D-type flip-flops
- Buffered common clock and buffered common three-state control
- V_{OL} = 0.5V (max) at I_{OL} = 32mA
- High-speed – Clock to output 11ns typical

RELATED PRODUCTS

Part No.	Description
Am29821-26	8, 9, 10-Bit Registers
Am2918	Quad D-Register
Am2920	Quad D-Type Flip-Flop

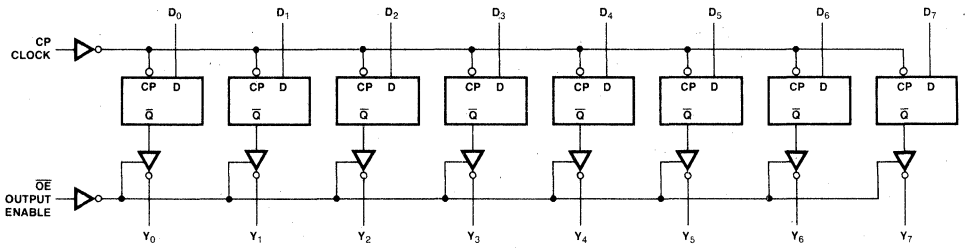
FUNCTIONAL DESCRIPTION

The Am2954 and Am2955 are 8-bit registers built using high-speed Schottky technology. The registers consist of eight D-type flip-flops with a buffered common clock and a buffered 3-state output control. When the output enable ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the 3-state condition.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the Y outputs on the LOW-to-HIGH transition of the clock input.

The devices are packaged in a space-saving (0.3-inch row spacing) 20-pin package.

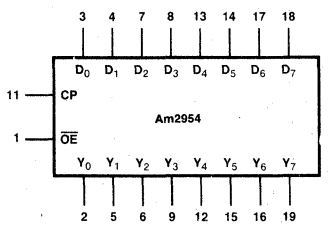
LOGIC DIAGRAM
Am2954

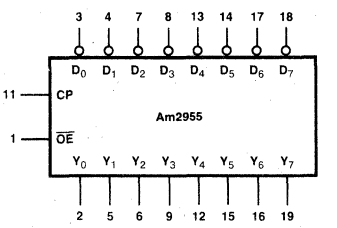


Inputs D_0 through D_7 are inverted on the Am2955.

BLI-110

LOGIC SYMBOLS



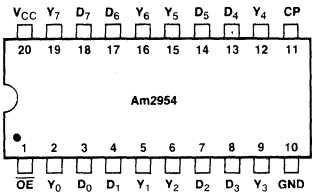


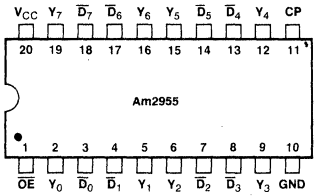
V_{CC} = Pin 20
GND = Pin 10

BLI-112

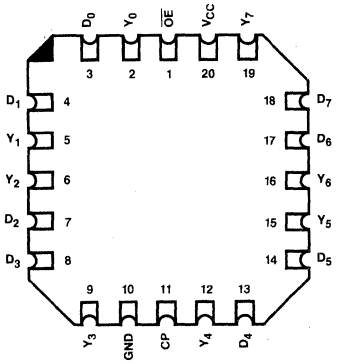
CONNECTION DIAGRAMS
Top Views

D-20, P-20





Leadless Chip Carrier
L-20-1



F-20 pin configuration identical to D-20, P-20.

Note: Pin 1 is marked for orientation.

BLI-111

5

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Am2954 Order Number	Am2955 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2954PC	AM2955PC	P-20	C	C-1
AM2954DC	AM2955DC	D-20	C	C-1
AM2954DC-B	AM2955DC-B	D-20	C	B-1
AM2954DM	AM2955DM	D-20	M	C-3
AM2954DM-B	AM2955DM-B	D-20	M	B-3
AM2954FM	AM2955FM	F-20	M	C-3
AM2954FM-B	AM2955FM-B	F-20	M	B-3
AM2954LC	AM2955LC	L-20-1	C	C-1
AM2954LC-B	AM2955LC-B	L-20-1	C	B-1
AM2954LM	AM2955LM	L-20-1	M	C-3
AM2954LM-B	AM2955LM-B	L-20-1	M	B-3
AM2954XC	AM2955XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2954XM	AM2955XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Flat-Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.

2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Levels B-3 conform to MIL-STD-883, Class B.

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

Am2954XC, DC, PC	Am2955XC, DC, PC	T_A = 0 to 70°C	V_{CC} = 4.75 to 5.25V
Am2954XM, DM, FM	Am2955XM, DM, FM	T_C = −55 to +125°C	V_{CC} = 4.50 to 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −2.0mA	2.4	3.4		Volts
			COM'L, I_{OH} = −6.5mA	2.4	3.1		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20mA			.45	Volts
			I_{OL} = 32mA			.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V				−250	μA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX	V_O = 0.5V			−50	μA
			V_O = 2.4V			50	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−40		−100	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX			90	140	mA

Notes:
1. For conditions shown as MIN or MAX use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Am2954 measured at CLK = LOW-to-HIGH, $\overline{OE}$ = HIGH, and all data inputs are LOW.
   Am2955 measured at CLK = LOW-to-HIGH, $\overline{OE}$ = HIGH, and all data inputs are LOW.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

DEFINITION OF FUNCTIONAL TERMS

D_i The D flip-flop data inputs (Am2954, non-inverting).

$\overline{D_i}$ The D flip-flop data inputs (Am2955, inverting).

CP Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.

Y_i The register three-state outputs (Am2954, non-inverting).

$\overline{OE}$ Output Control. An active-LOW three-state control used to enable the outputs. A HIGH level input forces the outputs to the high impedance (off) state.

FUNCTION TABLE

Function	Inputs				Internal	Outputs
	$\overline{OE}$	Clock	Am2954 D_i	Am2955 $\overline{D_i}$	Q_i	Y_i
Hi-Z	H	L	X	X	NC	Z
	H	H	X	X	NC	Z
LOAD REGISTER	L	↑	L	H	L	L
	L	↑	H	L	H	H
	H	↑	L	H	L	Z
	H	↑	H	L	H	Z

H = HIGH
L = LOW
X = Don't Care
NC = No Change
Z = High Impedance
↑ = LOW-to-HIGH transition

SWITCHING CHARACTERISTICS

(T_A = 25°C, V_{CC} = 5.0V)

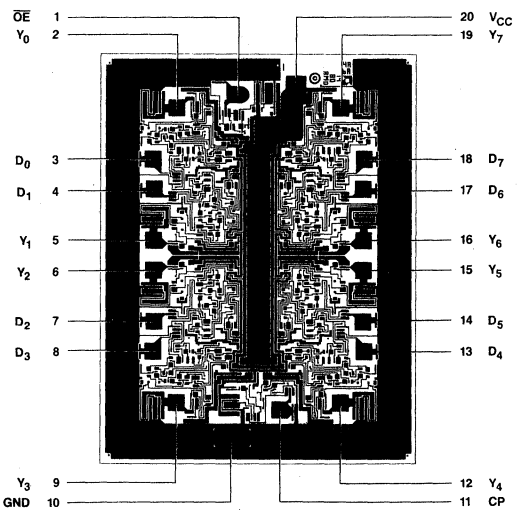
Parameters	Description		Am2954 • Am2955 Min	Typ	Max	Units	Test Conditions
t_{PLH}	Clock to Output, Y_i			8	15	ns	C_L = 15pF, R_L = 280Ω
t_{PHL}				11	17	ns	
t_{ZH}	$\overline{OE}$ to Y_i			8	15	ns	
t_{ZL}				11	18	ns	
t_{HZ}	$\overline{OE}$ to Y_i			5	9	ns	C_L = 5pF, R_L = 280Ω
t_{LZ}				7	12	ns	
t_{PW}	Clock Pulse Width	HIGH	6			ns	C_L = 15pF, R_L = 280Ω
		LOW	7.3			ns	
t_S	Data to Clock		5			ns	
t_H			2			ns	
f_{max}	Maximum Clock Frequency (Note 1)		75	100		MHz	

Note: 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

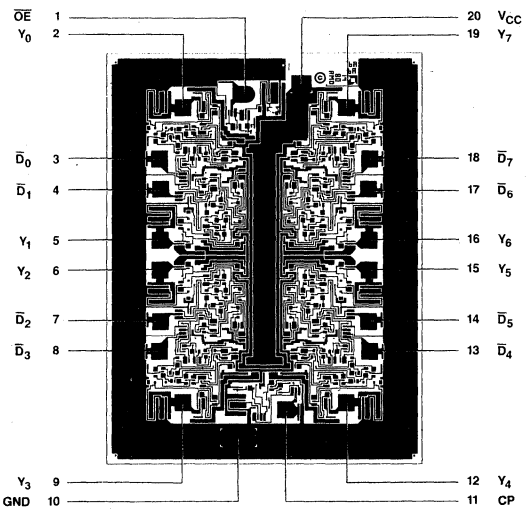
5

METALLIZATION AND PAD LAYOUTS

Am2954

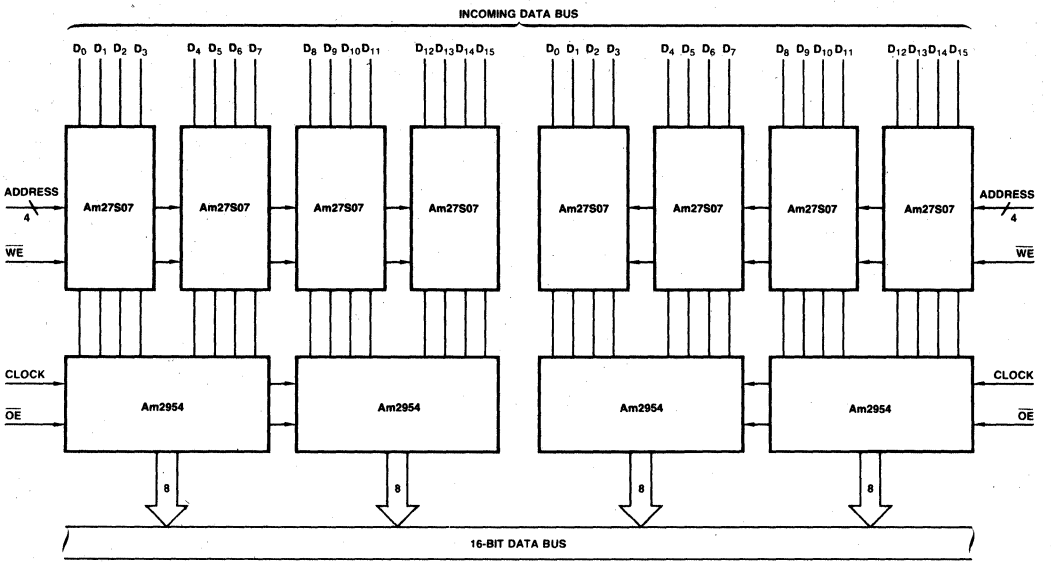


Am2955



DIE SIZE 0.085" X 0.110"

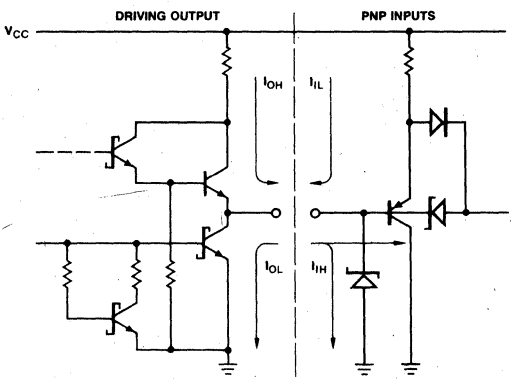
APPLICATION



Dual 16-word by 16-bit non-inverting high-speed data buffer.

BLI-113

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

BLI-114

Am2956 • Am2957

Octal Latches with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- 8-bit, high-speed parallel latches
- Am2956 has non-inverting inputs
- Am2957 has inverting inputs
- V_{OL} = 0.5V (max) at I_{OL} = 32mA
- Hysteresis on latch enable input for improved noise margin
- 3-state outputs interface directly with bus organized systems

RELATED PRODUCTS

Part No.	Description
Am29841-46	8, 9, 10-Bit Latches

FUNCTIONAL DESCRIPTION

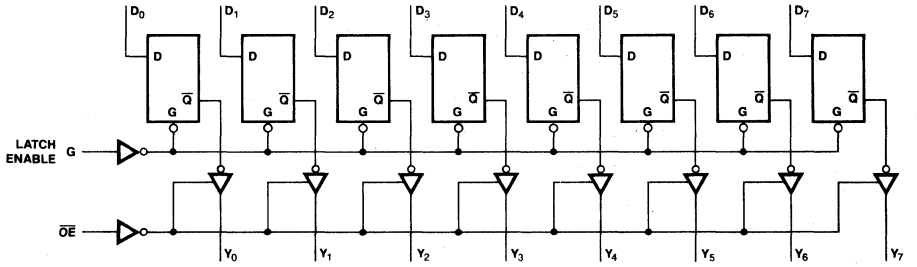
The Am2956 and Am2957 are octal latches with 3-state outputs for bus organized system applications. The latches appear to be transparent to the data (data changes asynchronously) when latch enable, G, is HIGH. When G is LOW, the data that meets the set-up times is latched. Data appears on the bus when the output enable, $\overline{OE}$, is LOW. When $\overline{OE}$ is HIGH the bus output is in the high-impedance state.

The Am2956 presents non-inverted data at the outputs while the Am2957 is inverting.

The devices are packaged in a space-saving (0.3-inch row spacing) 20-pin package.

5

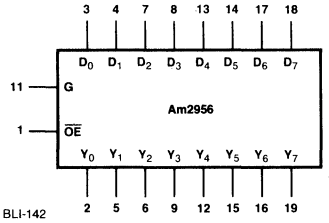
LOGIC DIAGRAM
Am2956



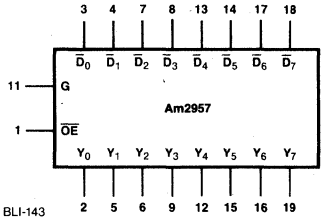
Inputs D_0 through D_7 are inverted on the Am2957.

BLI-139

LOGIC SYMBOLS



BLI-142

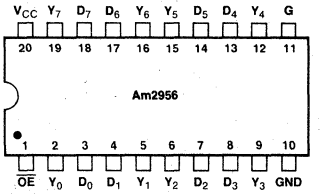


BLI-143

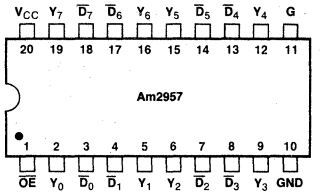
V_{CC} = Pin 20
GND = Pin 10

CONNECTION DIAGRAMS
Top Views

D-20, P-20

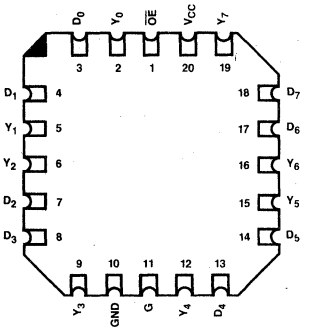


BLI-140



BLI-141

Leadless Chip Carrier
L-20-1



F-20 pin configuration identical to D-20, P-20.

Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Am2956 Order Number	Am2957 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2956PC	AM2957PC	P-20	C	C-1
AM2956DC	AM2957DC	D-20	C	C-1
AM2956DCB	AM2957DCB	D-20	C	B-1
AM2956DM	AM2957DM	D-20	M	C-3
AM2956DMB	AM2957DMB	D-20	M	B-3
AM2956FM	AM2957FM	F-20	M	C-3
AM2956FMB	AM2957FMB	F-20	M	B-3
AM2956LC	AM2957LC	L-20-1	C	C-1
AM2956LCB	AM2957LCB	L-20-1	C	B-1
AM2956LM	AM2957LM	L-20-1	M	C-3
AM2956LMB	AM2957LMB	L-20-1	M	B-3
AM2956XC	AM2957XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2956XM	AM2957XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak, F = Flat-Pak. Number following letter is number of leads.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See standard AMD Product Assurance Brochures for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Levels B-3 conform to MIL-STD-883, Class B.

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

Am2956/2957XC, DC, PC	T_A = 0 to 70°C	V_{CC} = 4.75 to 5.25V
Am2956/2957XM, DM	T_A = −55 to +125°C	V_{CC} = 4.50 to 5.50V
Am2956/2957FM	T_C = −55 to +125°C	V_{CC} = 4.50 to 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description		Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −2.0mA	2.4	3.4		Volts
				COM'L, I_{OH} = −6.5mA	2.4	3.1		
V_{OL}	Output LOW Voltage		V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20mA			.45	Volts
				I_{OL} = 32mA			.5	
V_{IH}	Input HIGH Level		Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level		Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage		V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current		V_{CC} = MAX, V_{IN} = 0.5V				−250	μA
I_{IH}	Input HIGH Current		V_{CC} = MAX, V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current		V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{OZ}	Off-State (High-Impedance) Output Current		V_{CC} = MAX	V_O = 0.5V			−50	μA
				V_O = 2.4V			50	
I_{SC}	Output Short Circuit Current (Note 3)		V_{CC} = MAX		−40		−100	mA
I_{CC}	Power Supply Current (Note 4)	2956	V_{CC} = MAX			105	160	mA
		2957				110	168	

Notes: 1. For conditions shown as MIN or MAX use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Inputs grounded; outputs open.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

Am2956
SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min	Typ	Max	Units	Test Conditions
t_{PLH}	Enable to Output		7	14	ns	C_L = 15pF, R_L = 280Ω
t_{PHL}			12	18	ns	
t_{PLH}	Data Input to Output		5	9	ns	
t_{PHL}			9	13	ns	
t_s(H)	HIGH Data to Enable	0			ns	
t_s(L)	LOW Data to Enable	0			ns	
t_h(H)	HIGH Data to Enable	10			ns	
t_h(L)	LOW Data to Enable	10			ns	
t_{pwH}	Enable Pulse Width	6			ns	
t_{pwL}		7.3			ns	
t_{ZH}	$\overline{OE}$ to Y_i		8	15	ns	
t_{ZL}			11	18	ns	
t_{HZ}	$\overline{OE}$ to Y_i		6	9	ns	C_L = 5pF, R_L = 280Ω
t_{LZ}			8	12	ns	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

FUNCTION TABLES

Am2956

Inputs			Internal	Outputs	Function
$\overline{OE}$	G	D_i	Q_i	Y_i	
H	X	X	X	Z	Hi-Z
L	H	L	H	L	Transparent
L	H	H	L	H	
L	L	X	NC	NC	Latched

Am2957

Inputs			Internal	Outputs	Function
$\overline{OE}$	G	$\overline{D_i}$	Q_i	Y_i	
H	X	X	X	Z	Hi-Z
L	H	L	H	H	Transparent
L	H	H	L	L	
L	L	X	NC	NC	Latched

H = HIGH
L = LOW
X = Don't Care

NC = No Change
Z = High Impedance

DEFINITION OF FUNCTIONAL TERMS

Am2956

D_i The latch data inputs.

G The latch enable input. The latches are transparent when G is HIGH. Input data is latched on the HIGH-to-LOW transition.

Y_i The 3-state latch outputs.

$\overline{OE}$ The output enable control. When $\overline{OE}$ is LOW, the outputs Y_i are enabled. When $\overline{OE}$ is HIGH, the outputs Y_i are in the high-impedance (off) state.

Am2957

$\overline{D_i}$ The latch inverting data inputs.

G The latch enable input. The latches are transparent when G is HIGH. Input data is latched on the HIGH-to-LOW transition.

$\overline{Y_i}$ The 3-state latch outputs.

$\overline{OE}$ The output enable control. When $\overline{OE}$ is LOW, the inverted outputs Y_i are enabled. When $\overline{OE}$ is HIGH, the outputs Y_i are in the high-impedance (off) state.

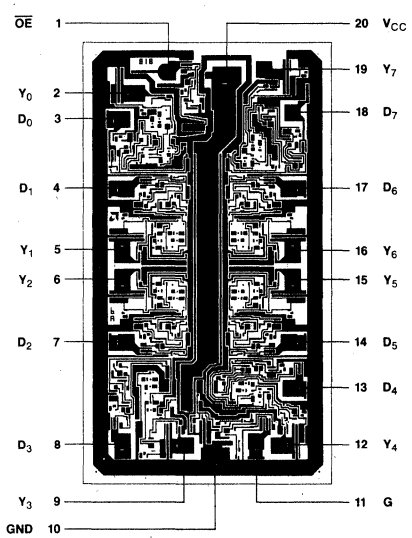
Am2957
SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min	Typ	Max	Units	Test Conditions
t_{PLH}	Enable to Output		17	24	ns	C_L = 15pF R_L = 280Ω
t_{PHL}			19	26	ns	
t_{PLH}	Data Input to Output		10	14	ns	
t_{PHL}			14	20	ns	
t_s(H)	HIGH Data to Enable	0			ns	
t_s(L)	LOW Data to Enable	0			ns	
t_h(H)	HIGH Data to Enable	10			ns	
t_h(L)	LOW Data to Enable	10			ns	
t_{pwH}	Enable Pulse Width	6			ns	
t_{pwL}		7.3			ns	
t_{ZH}	$\overline{OE}$ to Y_i		8	15	ns	
t_{ZL}			11	18	ns	
t_{HZ}	$\overline{OE}$ to Y_i		6	9	ns	C_L = 5pF R_L = 280Ω
t_{LZ}			8	10	ns	

5

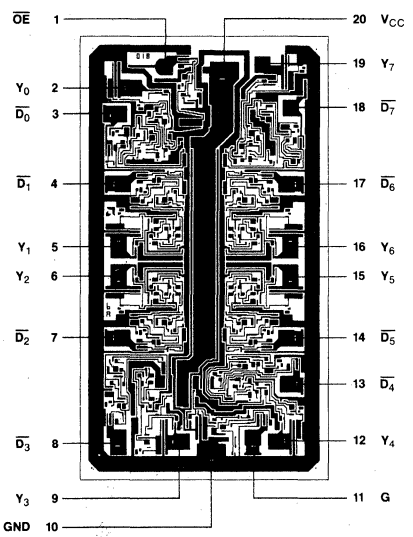
Metallization and Pad Layouts

Am2956



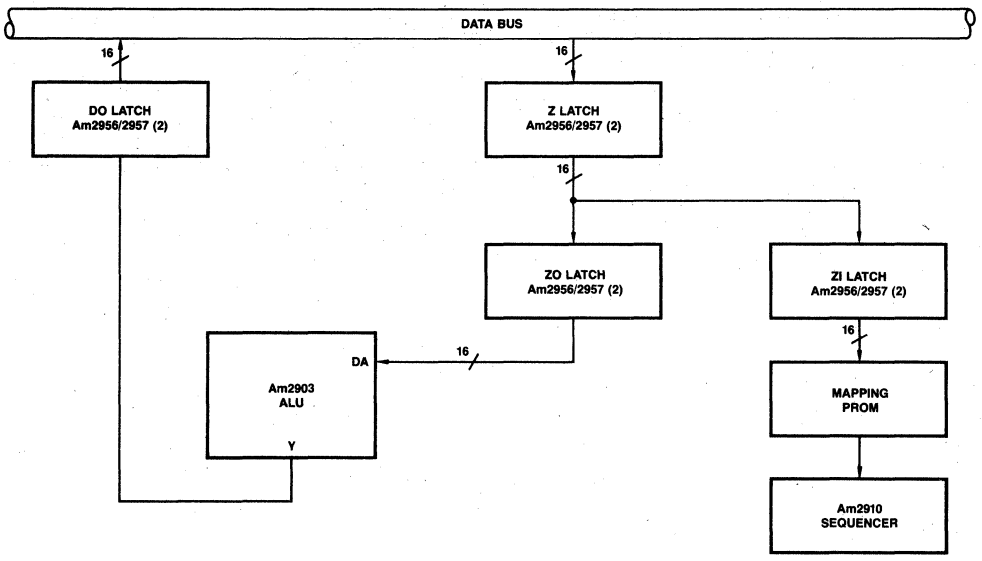
DIE SIZE 0.066" X 0.119"

Am2957



DIE SIZE 0.066" X 0.119"

APPLICATION



Transparent Latches are used in high performance CPU designs. The Z Latch configuration shown provides overlapped fetch of machine instructions and operand data.

BLI-144

Am2958 • Am2959

Octal Buffers/Line Drivers/Line Receivers with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Three-state outputs drive bus lines directly
- Advanced Schottky processing
- Hysteresis at inputs improve noise margin
- PNP inputs reduce D.C. loading on bus lines
- V_{OL} of 0.55V at 65mA for commercial-range product; 48mA for military-range product
- Data-to-output propagation delay times:
  - Inverting – 7.0ns MAX
  - Non-inverting – 9.0ns MAX
- Enable-to-output – 15.0ns MAX
- 20-pin hermetic and molded DIP packages

FUNCTIONAL DESCRIPTION

These buffers/line drivers, used as memory-address drivers, clock drivers, and bus oriented transmitters/receivers, provide improved PC board density. The outputs of the commercial temperature range versions have 64mA sink and 15mA source capability, which can be used to drive terminated lines down to 133Ω. The outputs of the military temperature range versions have 48mA sink and 12mA source current capability.

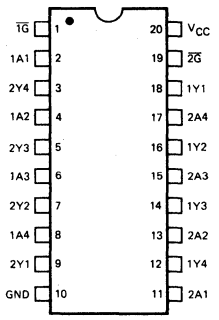
Featuring 0.2V minimum guaranteed hysteresis at each low-current PNP data input, they provide improved noise rejection and high-fan-out outputs to restore Schottky TTL levels completely.

The Am2958 and Am2959 have four buffers enabled from one common line, and the other four buffers enabled from another common line. The Am2958 is inverting, while the Am2959 presents true data at the outputs.

5

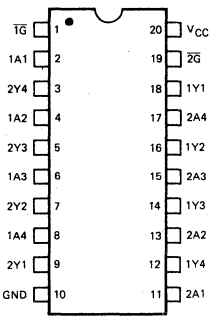
CONNECTION DIAGRAMS
Top Views

Am2958



BLI-137

Am2959



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ORDERING INFORMATION

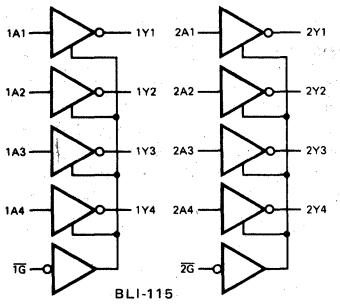
Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am2958 Order Number	Am2959 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2958PC	AM2959PC	P-20-1	C	C-1
AM2958DC	AM2959DC	D-20-1	C	C-1
AM2958DC-B	AM2959DC-B	D-20-1	C	B-1
AM2958DM	AM2959DM	D-20-1	M	C-3
AM2958DM-B	AM2959DM-B	D-20-1	M	B-3
Am2958XC	Am2959XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
Am2958XM	Am2959XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to 70°C, V_{CC} = 4.75V to 5.25V, M = −55 to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883.

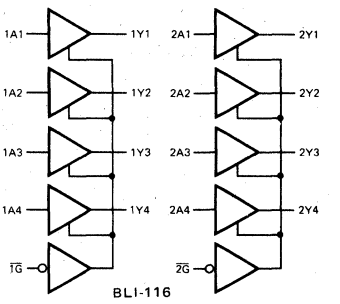
LOGIC DIAGRAMS

Am2958



BLI-115

Am2959



BLI-116

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current	150mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:

Am2958 (MIL)	T_A = −55 to +125°C	V_{CC} (MIN.) = 4.50V	V_{CC} (MAX.) = 5.50V
Am2959 (COM'L)	T_A = 0 to 70°C	V_{CC} (MIN.) = 4.75V	V_{CC} (MAX.) = 5.25V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

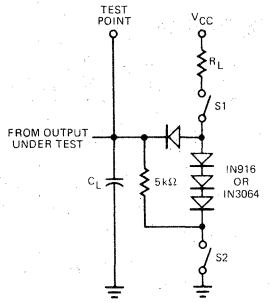
Parameters	Description			Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{IH}	High-Level Input Voltage					2.0			Volts
V_{IL}	Low-Level Input Voltage						0.8		Volts
V_{IK}	Input Clamp Voltage			V_{CC} = MIN., I_I = −18mA				−1.2	Volts
	Hystersis ($V_{T+} - V_{T-}$)			V_{CC} = MIN.		0.2	0.4		Volts
V_{OH}	High-Level Output Voltage			V_{CC} = MIN. V_{CC} = 0.8V	COM'L, I_{OH} = −1mA	2.7			Volts
					I_{OH} = −3mA	2.4	3.4		
				V_{CC} = MIN. V_{IL} = 0.5V	MIL, I_{OH} = −12mA	2.0			
					COM'L, I_{OH} = −15mA	2.0			
V_{OL}	Low-Level Output Voltage			V_{CC} = MIN. V_{IL} = 0.8V	MIL, I_{OL} = 48mA			0.55	Volts
					COM'L, I_{OL} = 64mA			0.55	
I_{OZH}	Off-State Output Current, High-Level Voltage Applied			V_{CC} = MAX. V_{IH} = 2.0V V_{IL} = 0.8V	V_O = 2.4V			50	μA
I_{OZL}	Off-State Output Current, Low-Level Voltage applied				V_O = 0.5V			−50	
I_I	Input Current at Maximum Input Voltage			V_{CC} = MAX., V_I = 5.5V				1.0	mA
I_{IH}	High-Level Input Current, Any Input			V_{CC} MAX., V_{IH} = 2.7V				50	μA
I_{IL}	Low-Level Input Circuit		Any A	V_{CC} = MAX., V_{IL} = 0.5V				−400	μA
			Any G					−2.0	mA
I_{OS}	Short-Circuit Output Current (Note 3)			V_{CC} = MAX.		−50		−225	mA
I_{CC}	Supply Current	Am2958	All Outputs HIGH	V_{CC} = MAX, Outputs Open	MIL and COM'L		37	65	mA
			All Outputs LOW				59	90	
			Outputs at Hi-Z				69	105	
		Am2959	All Outputs HIGH	V_{CC} = MAX, Outputs Open	MIL and COM'L		37	65	mA
			All Outputs LOW				63	105	
			Outputs at Hi-Z				72	120	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions.
2. All typical values are V_{CC} = 5.0V, T_A = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed on second.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C)

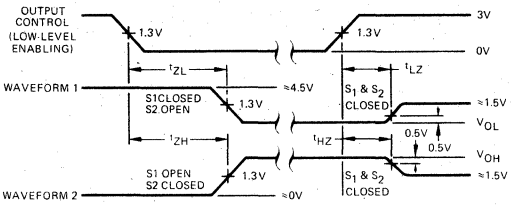
Parameter	Description	Test Conditions	Am2958 Min.	Am2958 Typ.	Am2958 Max.	Am2959 Min.	Am2959 Typ.	Am2959 Max.	Units
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	C_L = 50pF, R_L = 90Ω (Note 3)		4.5	7.0		6.0	9.0	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output			4.5	7.0		6.0	9.0	ns
t_{ZL}	Output Enable Time to Low Level			10	15		10	15	ns
t_{ZH}	Output Enable Time to High Level			6.5	10		8.0	12	ns
t_{LZ}	Output Disable Time from Low Level	C_L = 5.0pF, R_L = 90Ω (Note 3)		10	15		10	15	ns
t_{HZ}	Output Disable Time from High Level			6.0	9.0		6.0	9.0	ns

LOAD CIRCUIT FOR THREE-STATE OUTPUTS



BLI-117

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



BLI-118

Notes: 1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily. PRR ≤ 1.0MHz, $Z_{OUT} \approx 50\Omega$ and $t_r \leq 2.5$ns, $t_f \leq 2.5$ns.

FUNCTION TABLES

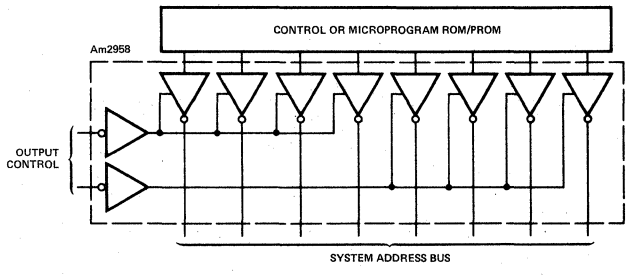
Am2958

INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

Am2959

INPUTS		OUTPUT
$\overline{G}$	A	
H	X	Z
L	H	H
L	L	L

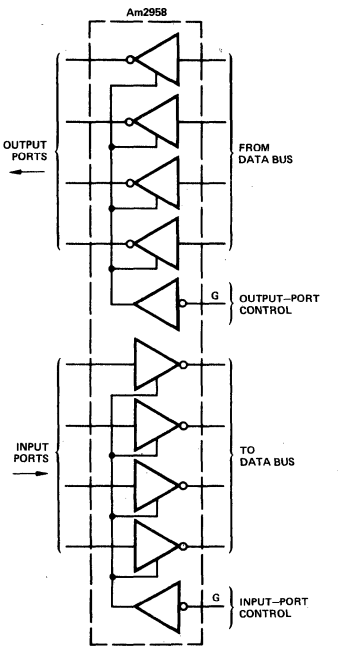
Am2958 USED AS SYSTEM BUS DRIVER – 4-BIT ORGANIZATION CAN BE APPLIED TO HANDLE BINARY OR BCD



BLI-119

APPLICATIONS (Cont.)

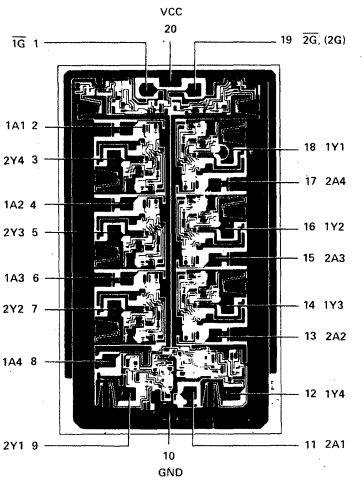
INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS IN A SINGLE PACKAGE



BLI-120

Metallization and Pad Layout

Am2958 • Am2959



DIE SIZE 0.077" X 0.124"

Am29203

Four-Bit Bipolar Microprocessor Slice

DISTINCTIVE CHARACTERISTICS

- **Expandable Register File –**
  Like the Am2901, the Am29203 contains 16 internal working registers arranged in a two-address architecture. But the Am29203 includes the necessary "hooks" to expand the register file externally to any number of registers.
- **Built-in Multiplication Logic –**
  Performing multiplication with the Am2901A requires a few external gates – these gates are contained on-chip in the Am29203. Three special instructions are used for unsigned multiplication, two's complement multiplication and the last cycle of a two's complement multiplication.
- **Built-in Division Logic –**
  The Am29203 contains all logic and interconnects for execution of a non-restoring, multiple-length division with correction of the quotient.
- **Built-in Normalization Logic –**
  The Am29203 can simultaneously shift the Q register and count in a working register. Thus, the mantissa and exponent of a floating-point number can be developed using a single microcycle per shift. Status flags indicate when the operation is complete.
- **Built-in Parity Generation Circuitry –**
  The Am29203 can supply parity across the entire ALU output for use in error detection.
- **Built-in Sign Extension Circuitry –**
  To facilitate operation on different length two's complement numbers, the Am29203 provides the capability to extend the sign at any slice boundary.
- **BCD Arithmetic –**
  The Am29203 features automatic BCD add and subtract and conversion between binary and BCD.
- **Improved Byte Handling –**
  On the Am29203 zero detection and register writing can be performed on a single byte rather than the whole word.
- **Two Bidirectional Data Lines**
- **Improved I/O Capability –**
  Both the DA and DB data buses are bidirectional on the Am29203. In addition, the Y port is also bidirectional.

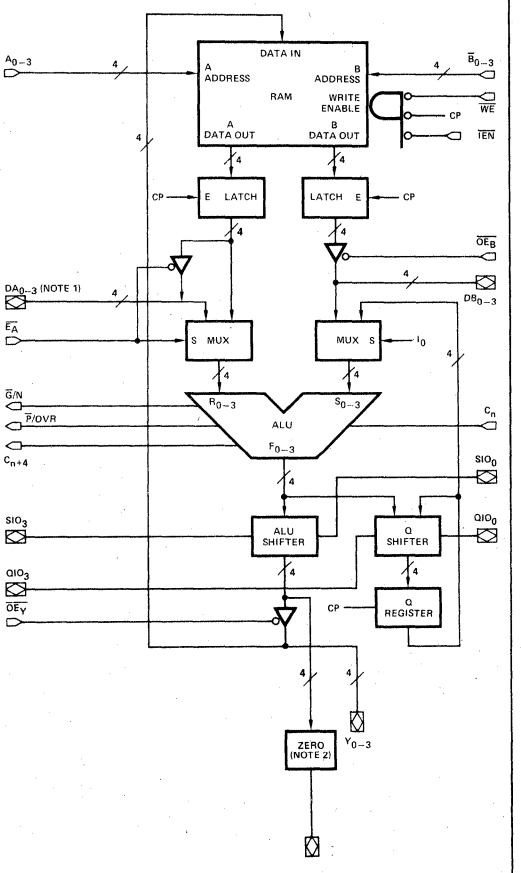
RELATED PRODUCTS

Part No.	Description
Am2902A	Carry Look-Ahead Generator
Am2904	Status and Shift Control Unit
Am2910A	Microprogram Controller
Am2914	Vectored Priority Interrupt Controller
Am2917A	Bus Transceiver
Am2918	Pipeline Register
Am2920	Octal Register
Am2922	Condition Code MUX
Am2925	System Clock Generator
Am2940	DMA Address Generator
Am2952	Bidirectional I/O Port
Am29707	Two-Port RAM
Am27S35	Registered PROM

GENERAL DESCRIPTION

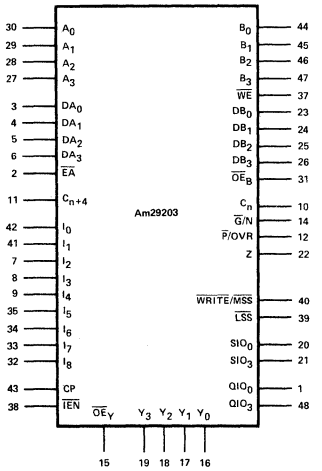
The Am29203 is a four-bit expandable bipolar microprocessor slice. The Am29203 performs all functions performed by the industry standard Am2901 and, in addition, provides a number of significant enhancements that are especially useful in arithmetic-oriented processors. Infinitely expandable memory and three-port, three-address architecture are provided by the Am29203. In addition to its complete arithmetic and logic instruction set, the Am29203 provides a special set of instructions which facilitate the implementation of multiplication, division, normalization, BCD arithmetic and conversion, and other previously time consuming operations. The Am29203 has three bidirectional ports and features AMD's ion-implanted micro-oxide (IMOX™) technology.

BLOCK DIAGRAM



IMOX is a trademark of Advanced Micro Devices, Inc.

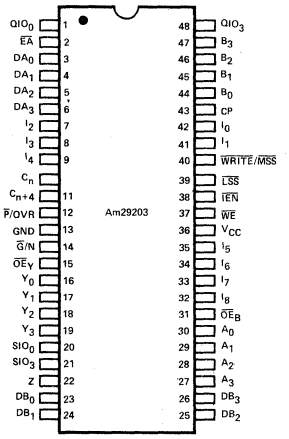
LOGIC SYMBOL



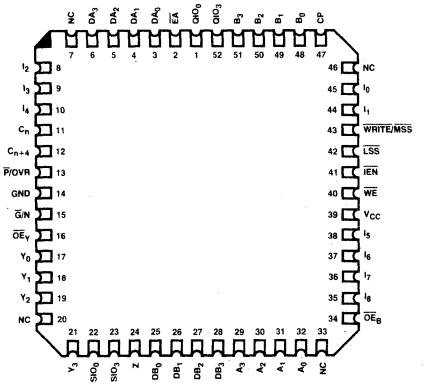
V_{CC} = Pin 36
GND = Pin 13

CONNECTION DIAGRAMS
Top Views

DIP
D-48



Leadless Chip Carrier
L-52-1



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am29203 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM29203DC	D-48	C	C-1
AM29203DC-B	D-48	C	B-2 (Note 4)
AM29203DM	D-48	M	C-3
AM29203DM-B	D-48	M	B-3
AM29203FM	F-48	M	C-3
AM29203FM-B	F-48	M	B-3
AM29203LC	L-52	C	C-1
AM29203LM	L-52	M	C-3
AM29203LM-B	L-52	M	B-3
AM29203XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM29203XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak, L = Leadless Chip-Pak. Number following letter is number of leads. See Appendix B for detailed outline.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

PIN DEFINITIONS

A_{0-3} Four RAM address inputs which contain the address of the RAM word appearing at the RAM A output port.

B_{0-3} Four RAM address inputs which contain the address of the RAM word appearing at the RAM B output port and into which new data is written when the $\overline{WE}$ input and the CP input are LOW.

$\overline{WE}$ The RAM write enable input. If $\overline{WE}$ is LOW, data at the Y I/O port is written into the RAM when the CP input is LOW. When $\overline{WE}$ is HIGH, writing data into the RAM is inhibited.

DA_{0-3} A four-bit external data input which can be selected as one of the ALU operand sources; DA_0 is the least significant bit. On the Am29203, the DA path is bidirectional, operating as either an ALU source operand or as an external output for the RAM A-port.

$\overline{EA}$ A control input which, when HIGH selects DA_{0-3} as the ALU R operand, and, when LOW, selects RAM output A as the ALU R operand and the DA_{0-3} output data.

DB_{0-3} A four-bit external data input/output. Under control of the $\overline{OE_B}$ input, RAM output port B can be directly read on these lines, or input data on these lines can be selected as the ALU S operand.

$\overline{OE_B}$ A control input which, when LOW, enables RAM output B onto the DB_{0-3} lines and, when HIGH, disables the RAM output B tri-state buffers.

C_n The carry-in input to the Am29203 ALU.

I_{0-8} The nine instruction inputs used to select the Am29203 operation to be performed.

$\overline{IEN}$ The instruction enable input which, when LOW, allows the Q Register and the Sign Compare flip-flop to be written. When $\overline{IEN}$ is HIGH, the Q Register and Sign Compare flip-flop are in the hold mode. On the Am29203, $\overline{WRITE}$ is not affected by $\overline{IEN}$, but internally disables the RAM write enable.

C_{n+4} This output generally indicates the carry-out of the Am29203 ALU. Refer to Table 5 for an exact definition of this pin.

$\overline{G}$/N A multi-purpose pin which indicates the carry generate, $\overline{G}$, function at the least significant and intermediate slices, and generally indicates the sign, N, of the ALU result at the most significant slice. Refer to Table 5 for an exact definition of this pin.

$\overline{P}$/OVR A multi-purpose pin which indicates the carry propagate, $\overline{P}$, function at the least significant and intermediate slices, and indicates the conventional two's complement overflow, OVR, signal at the most significant slice. Refer to Table 5 for an exact definition of this pin.

Z An open-collector input/output pin which, when HIGH, generally indicates the outputs are all LOW. For some Special Functions, Z is used as an input pin. Refer to Table 5 for an exact definition of this pin.

SIO_0, SIO_3 Bidirectional serial shift inputs/outputs for the ALU shifter. During a shift-up operation, SIO_0 is an input and SIO_3 an output. During a shift-down operation, SIO_3 is an input and SIO_0 is an output. Refer to Tables 3 and 4 for an exact definition of these pins.

QIO_0, QIO_3 Bidirectional serial shift inputs/outputs for the Q shifter which operate like SIO_0 and SIO_3. Refer to Tables 3 and 4 for an exact definition of these pins.

$\overline{LSS}$ An input pin which, when tied LOW, programs the chip to act as the least significant slice (LSS) of an Am29203 array and enables the $\overline{WRITE}$ output onto the $\overline{WRITE}/\overline{MSS}$ pin. When $\overline{LSS}$ is tied HIGH, the chip is programmed to operate as either an intermediate or most significant slice and the $\overline{WRITE}$ output buffer is disabled.

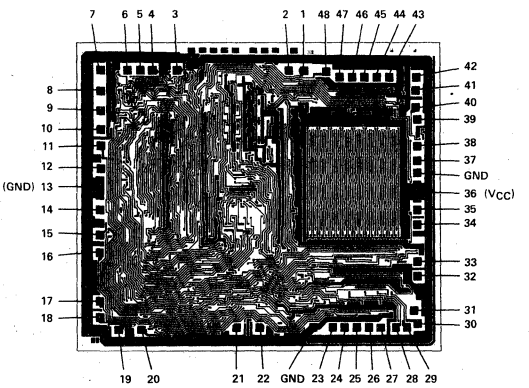
$\overline{WRITE}/\overline{MSS}$ When $\overline{LSS}$ is tied LOW, the $\overline{WRITE}$ output signal appears at this pin; the $\overline{WRITE}$ signal is LOW when an instruction which writes data into the RAM is being executed. When $\overline{LSS}$ is tied HIGH, $\overline{WRITE}/\overline{MSS}$ is an input pin; tying it HIGH programs the chip to operate as an intermediate slice (IS) and tying it LOW programs the chip to operate as the most significant slice (MSS).

Y_{0-3} Four data inputs/outputs of the Am29203. Under control of the $\overline{OE_Y}$ input, the ALU shifter output data can be enabled onto these lines, or these lines can be used as data inputs when external data is written directly into the RAM.

$\overline{OE_Y}$ A control input which, when LOW, enables the ALU shifter output data onto the Y_{0-3} lines and, when HIGH, disables the Y_{0-3} three-state output buffers.

CP The clock input to the Am29203. The Q register and Sign Compare flip-flop are clocked on the LOW-to-HIGH transition of the CP signal. When enabled by $\overline{WE}$, data is written in the RAM when CP is LOW.

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.163" X 0.197"

Note: Pin numbers correspond to DIP package.

Am29203

ARCHITECTURE OF THE Am29203

The Am29203 is a high-performance, cascadable, four-bit bipolar microprocessor slice designed for use in CPUs, peripheral controllers, microprogrammable machines, and numerous other applications.The microinstruction flexibility of the Am29203 allows the efficient emulation of almost any digital computing machine. The nine-bit microinstruction selects the ALU sources, function and destination. The Am29203 is cascadable with full lookahead or ripple carry, has three-state outputs, and provides various ALU status flag outputs. Advanced Low-Power Schottky processing is used to fabricate this 48-pin LSI circuit.

All data paths within the device are four bits wide. As shown in the block diagram, the device consists of a 16-word by 4-bit, two-port RAM with latches on both output ports, a high-performance ALU and shifter, a multi-purpose Q Register with shifter input, and a nine-bit instruction decoder.

Two-Port RAM

Any two RAM words addressed at the A and B address ports can be read simultaneously at the respective RAM A and B output ports. Identical data appear at the two output ports when the same address is applied to both address ports. The latches at the RAM output ports are transparent when the clock input, CP, is HIGH and they hold the RAM output data when CP is LOW. Under control of the $\overline{OE_B}$ three-state output enable, RAM data can be read directly at the Am2903 DB I/O port. On the Am29203, E_A provides the same feature at the DA port.

External data at the Am29203 Y I/O port can be written directly into the RAM, or ALU shifter output data can be enabled ontc the Y I/O port and entered into the RAM. Data is written into the RAM at the B address when the write enable input, $\overline{WE}$, is LOW and the clock input, CP, is LOW.

Arithmetic Logic Unit

The Am29203 high-performance ALU can perform seven arithmetic and nine logic operations on two 4-bit operands. Multiplexers at the ALU inputs provide the capability to select various pairs of ALU source operands. The $\overline{E_A}$ input selects either the DA external data input or RAM output port A for use as one ALU operand and the $\overline{OE_B}$ and I_0 inputs select RAM output port B, DB external data input, or the Q register content for use as the second ALU operand. Also, during some ALU operations, zeroes are forced at the ALU operand inputs. Thus, the Am29203 ALU can operate on data from two external sources, from an internal and external source, or from two internal sources. Table 1 shows all possible pairs of ALU source operands as a function of the $\overline{E_A}$, $\overline{OE_B}$, and I_0 inputs.

TABLE 1. ALU OPERAND SOURCES

$\overline{E_A}$	I_0	$\overline{OE_B}$	ALU Operand R	ALU Operand S
L	L	L	RAM Output A	RAM Output B
L	L	H	RAM Output A	DB_{0-3}
L	H	X	RAM Output A	Q Register
H	L	L	DA_{0-3}	RAM Output B
H	L	H	DA_{0-3}	DB_{0-3}
H	H	X	DA_{0-3}	Q Register

L = LOW H = HIGH X = Don't Care

TABLE 2. Am29203 ALU FUNCTIONS

I_4	I_3	I_2	I_1	I_0	ALU Functions
L	L	L	L	L	Special Functions
L	L	L	L	H	F_i = HIGH
L	L	L	H	X	F = S Minus R Minus 1 Plus C_n
L	L	H	L	X	F = R Minus S Minus 1 Plus C_n
L	L	H	H	X	F = R Plus S Plus C_n
L	H	L	L	X	F = S Plus C_n
L	H	L	H	X	F = $\overline{S}$ Plus C_n
L	H	H	L	L	Reserved Special Functions
L	H	H	L	H	F = R Plus C_n
L	H	H	H	L	Reserved Special Functions
L	H	H	H	H	F = $\overline{R}$ Plus C_n
H	L	L	L	L	Special Functions
H	L	L	L	H	F_i = LOW
H	L	L	H	X	$F_i = \overline{R_i}$ AND S_i
H	L	H	L	X	$F_i = R_i$ EXCLUSIVE NOR S_i
H	L	H	H	X	$F_i = R_i$ EXCLUSIVE OR S_i
H	H	L	L	X	$F_i = R_i$ AND S_i
H	H	L	H	X	$F_i = R_i$ NOR S_i
H	H	H	L	X	$F_i = R_i$ NAND S_i
H	H	H	H	X	$F_i = R_i$ OR S_i

L = LOW H = HIGH i = 0 to 3
X = LOW or HIGH

When instruction bits I_4, I_3, I_2, I_1, and I_0 are LOW, the Am29203 executes special functions. Table 4 defines these special functions and the operation which the ALU performs for each. When the Am29203 executes instructions other than the 16 special functions, the ALU operation is determined by instruction bits I_4, I_3, I_2, and I_1. Table 2 defines the ALU operation as a function of these four instruction bits.

Am29203s may be cascaded in either a ripple carry or lookahead carry fashion. When a number of Am29203s are cascaded, each slice must be programmed to be a most significant slice (MSS), intermediate slice (IS), or least significant slice (LSS) of the array. The carry generate, $\overline{G}$, and carry propagate, $\overline{P}$, signals required for a lookahead carry scheme are generated by the Am29203 and are available as outputs of the least significant and intermediate slices.

The Am29203 also generates a carry-out signal, C_{n+4}, which is generally available as an output of each slice. Both the carry-in, C_n, and carry-out, C_{n+4}, signals are active HIGH. The ALU generates two other status outputs. These are negative, N, and overflow, OVR. The N output is generally the most significant (sign) bit of the ALU output and can be used to determine positive or negative results. The OVR output indicates that the arithmetic operation being performed exceeds the available two's complement number range. The N and OVR signals are available as outputs of the most significant slice. Thus, the multipurpose $\overline{G}$/N and $\overline{P}$/OVR outputs indicate $\overline{G}$ and $\overline{P}$ at the least significant and intermediate slices, and sign and overflow at the most significant slice. To some extent, the meaning of the C_{n+4}, $\overline{P}$/OVR, and $\overline{G}$/N signals vary with the ALU function being performed. Refer to Table 5 for an exact definition of these four signals as a function of the Am29203 instruction.

5

ALU Shifter

Under instruction control, the ALU shifter passes the ALU output (F) non-shifted, shifts it up one bit position (2F), or shifts it down one bit position (F/2). Both arithmetic and logical shift operations are possible. An arithmetic shift operation shifts data around the most significant (sign) bit position of the most significant slice, and a logical shift operation shifts data through this bit position (see Figure A). SIO_0 and SIO_3 are bidirectional serial shift inputs/outputs. During a shift-up operation, SIO_0 is generally a serial shift input and SIO_3 a serial shift output. During a shift-down operation, SIO_3 is generally a serial shift input and SIO_0 a serial shift output.

To some extent, the meaning of the SIO_0 and SIO_3 signals is instruction dependent. Refer to Tables 3 and 4 for an exact definition of these pins.

The ALU shifter also provides the capability to sign extend at slice boundaries. Under instruction control, the SIO_0 (sign) input can be extended through Y_0, Y_1, Y_2, Y_3 and propagated to the SIO_3 output.

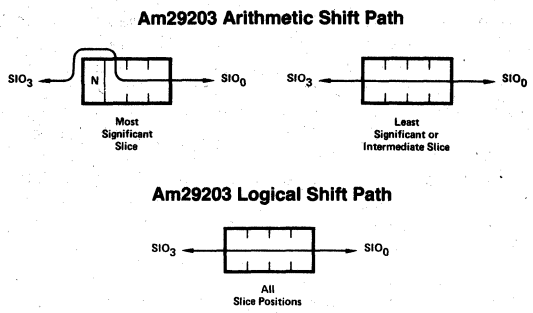
A cascadable, five-bit parity generator/checker is designed into the Am29203 ALU shifter and provides ALU error detection capability. Parity for the F_0, F_1, F_2, F_3 ALU outputs and SIO_3 input is generated and, under instruction control, is made available at the SIO_0 output. Refer to the Am29203 applications section for a more detailed description of the Am29203 sign extension and parity generation/checking capability.

The instruction inputs determine the ALU shifter operation. Table 4 defines the special functions and the operation the ALU shifter performs for each. When the Am29203 executes instructions other than the special functions, the ALU shifter operation is determined by instruction bits I_8, I_7, I_6, I_5. Table 3 defines the ALU shifter operation as a function of these four bits.

Q Register

The Q Register is an auxiliary four-bit register which is clocked on the LOW-to-HIGH transition of the CP input. It is intended primarily for use in multiplication and division operations; however, it can also be used as an accumulator or holding register for some applications. The ALU output, F, can be loaded into the Q Register, and/or the Q Register can be selected as the source for the ALU S operand. The shifter at the input to the Q Register provides the capability to shift the Q Register contents up one bit position (2Q) or down one bit position (Q/2). Only logical shifts are performed. QIO_0 and QIO_3 are bidirectional shift serial inputs/outputs. During a Q Register shift-up operation, QIO_0 is a serial shift input and QIO_3 is a serial shift output. During a shift-down operation, QIO_3 is a serial shift input and QIO_0 is a serial shift output.

Figure A.



Double-length arithmetic and logical shifting capability is provided by the Am29203. The double-length shift is performed by connecting QIO_3 of the most significant slice to SIO_0 of the least significant slice, and executing an instruction which shifts both the ALU output and the Q register.

The Q register and shifter are controlled by the instruction inputs. Table 4 defines the Am29203 special functions and the operations which the Q register and shifter perform for each. When the Am29203 executes instructions other than the special functions, the Q register and shifter operation is controlled by instruction bits I_8, I_7, I_6, I_5. Table 3 defines the Q register and shifter operation as a function of these four bits.

Output Buffers

The DB, DA, and Y ports are bidirectional I/O ports driven by three-state output buffers with external output enable controls.

TABLE 3. ALU DESTINATION CONTROL FOR I_0 OR I_1 OR I_2 OR I_3 = HIGH, IEN = LOW

I_8	I_7	I_6	I_5	Hex Code	ALU Shifter Function	SIO_3 Most Sig. Slice	SIO_3 Other Slices	Y_3 Most Sig. Slice	Y_3 Other Slices	Y_2 Most Sig. Slice	Y_2 Other Slices	Y_1	Y_0	SIO_0	$\overline{Write}$	Q Reg & Shifter Function	QIO_3	QIO_0
L	L	L	L	0	Arith. F/2→Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Hold	Hi-Z	Hi-Z
L	L	L	H	1	Log. F/2→Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Hold	Hi-Z	Hi-Z
L	L	H	L	2	Arith. F/2→Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Log. Q/2→Q	Input	Q_0
L	L	H	H	3	Log. F/2→Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Log. Q/2→Q	Input	Q_0
L	H	L	L	4	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	Hold	Hi-Z	Hi-Z
L	H	L	H	5	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	Log. Q/2→Q	Input	Q_0
L	H	H	L	6	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	F→Q	Hi-Z	Hi-Z
L	H	H	H	7	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	F→Q	Hi-Z	Hi-Z
H	L	L	L	8	Arith. 2F→Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	L	L	H	9	Log. 2F→Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	L	H	L	A	Arith. 2F→Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q→Q	Q_3	Input
H	L	H	H	B	Log. 2F→Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q→Q	Q_3	Input
H	H	L	L	C	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	H	Hold	Hi-Z	Hi-Z
H	H	L	H	D	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	H	Log. 2Q→Q	Q_3	Input
H	H	H	L	E	SIO_0→Y_0, Y_1, Y_2, Y_3	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	H	H	H	F	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	L	Hold	Hi-Z	Hi-Z

Parity = $F_3 \forall F_2 \forall F_1 \forall F_0 \forall SIO_3$
$\forall$ = Exclusive OR

L = LOW
H = HIGH

Hi-Z = High Impedance

TABLE 4. SPECIAL FUNCTIONS (Note 7)

(Hex) $I_8I_7I_6I_5$	I_4	(Hex) $I_3I_2I_1I_0$	Special Function	ALU Function	ALU Shifter Function	SIO_3 Most Sig Slice	SIO_3 Other Slices	SIO_0	Q Reg & Shifter Function	QIO_3	QIO_0	$\overline{WRITE}$
0	L	0	Unsigned Multiply	$F = S + C_n$ if Z = L $F = R + S + C_n$ if Z = H	Log F/2 → Y (Note 1)	Z	Input	F_0	Log Q/2→ Q	Input	Q_0	L
1	L	0	BCD to Binary Conversion	(Note 4)	Log F/2→ Y	Input	Input	F_0	Log Q/2→ Q	Input	Q_0	L
1	H	0	Multiprecision BCD to Binary	(Note 4)	Log F/2→ Y	Input	Input	F_0	Hold	Z	Q_0	L
2	L	0	Two's Complement Multiply	$F = S + C_n$ if Z = L $F = R + S + C_n$ if Z = H	Log F/2 → Y (Note 2)	Z	Input	F_0	Log Q/2→ Q	Input	Q_0	L
3	L	0	Decrement by One or Two	$F = S - 2 + C_n$	F→ Y	Z	Z	Parity	Hold	Z	Z	L
4	L	0	Increment by One or Two	$F = S + 1 + C_n$	F → Y	Input	Input	Parity	Hold	Z	Z	L
5	L	0	Sign/Magnitude Two's Complement	$F = S + C_n$ if Z = L $F = \overline{S} + C_n$ if Z = H	F → Y (Note 3)	Input	Input	Parity	Hold	Z	Z	L
6	L	0	Two's Complement Multiply, Last Cycle	$F = S + C_n$ if Z = L $F = S - R - 1 + C_n$ if Z = H	Log F/2 → Y (Note 2)	Z	Input	F_0	Log Q/2→ Q	Input	Q_0	L
7	L	0	BCD Divide by Two	(Note 4)	F→ Y	Z	Z	Parity	Hold	Z	Z	L
8	L	0	Single Length Normalize	$F = S + C_n$	F → Y	F_3	F_3	Z	Log 2Q→ Q	Q_3	Input	L
9	L	0	Binary to BCD Conversion	(Note 5)	Log 2F→ Y	F_3	F_3	Input	Log 2Q→ Q	Q_3	Input	L
9	H	0	Multiprecision Binary to BCD	(Note 5)	Log 2F→ Y	F_3	F_3	Input	Hold	Z	Input	L
A	L	0	Double Length Normalize and First Divide Op	$F = S + C_n$	Log 2F → Y	$R_3 \forall F_3$	F_3	Input	Log 2Q→ Q	Q_3	Input	L
B	L	0	BCD Add	$F = R + S + C_n$ BCD (Note 6)	F→ Y	0	0	Z	Hold	Z	Z	L
C	L	0	Two's Complement Divide	$F = S + R + C_n$ if Z = L $F = S - R - 1 + C_n$ if Z = H	Log 2F → Y	$\overline{R_3 \forall F}$	F_3	Input	Log 2Q→ Q	Q_3	Input	L
D	L	0	BCD Subtract	$F = R - S - 1 + C_n$ BCD (Note 6)	F→ Y	0	0	Z	Hold	Z	Z	L
E	L	0	Two's Complement Divide Correction and Remainder	$F = S + R + C_n$ if Z = L $F = S - R - 1 + C_n$ if Z = H	F → Y	F_3	F_3	Z	Log 2Q→ Q	Q_3	Input	L
F	L	0	BCD Subtract	$F = S - R - 1 + C_n$ BCD (Note 6)	F→ Y	0	0	Z	Hold	Z	Z	L

Notes:
1. At the most significant slice only, the C_{n+4} signal is internally gated to the Y_3 output.
2. At the most significant slice only, $F_3 \forall$ OVR is internally gated to the Y_3 output.
3. At the most significant slice only, $S_3 \forall F_3$ is generated at the Y_3 output.
4. On each slice, F = S if magnitude of S_{0-3} is less than 8 and F = S minus 3 if magnitude of S_{0-3} is 8 or greater.
5. On each slice, F = S if magnitude of S_{0-3} is less than 5 and F = S plus 3 if magnitude of S_{0-3} is 5 or greater. Addition is module 16.
6. Additions and subtractions are BCD adds and subtracts. Results are undefined if R or S are not in valid BCD format.
7. The Q Register cannot be used explicitly as an operand for any Special Functions. It is defined implicitly within the functions.

L = LOW Hi-Z = High Impedance
H = HIGH = Exclusive OR
X = Don't Care Parity = $SIO_3 \forall F_3 \forall F_2 \forall F_1 \forall F_0$

The Y output buffers are enabled when the $\overline{OE_Y}$ input is LOW and are in the high impedance state when $\overline{OE_Y}$ is HIGH. The DB output buffers are enabled when the $\overline{OE_B}$ input is LOW and the DA buffers are enabled when $\overline{E_A}$ is LOW.

The zero, Z, pin is an open collector input/output that can be wire-OR'ed between slices. As an output it can be used as a zero detect status flag and generally indicates that the Y_{0-3} pins are all LOW. To some extent the meaning of this signal varies with the instruction being performed. Refer to Table 5 for an exact definition of this signal as a function of the Am29203 instructions. On the Am29203, the Z pin will be HIGH if $\overline{OE_Y}$ is HIGH, allowing zero detection on less than the full word.

Instruction Decoder

The Instruction Decoder generates required internal control signals as a function of the nine Instruction inputs, I_{0-8}; the Instruction Enable input, $\overline{IEN}$; the $\overline{LSS}$ input; and the $\overline{WRITE}/\overline{MSS}$ input/output.

The $\overline{WRITE}$ output is LOW when an instruction which writes data into the RAM is being executed. Refer to Tables 3 and 4 for a definition of the $\overline{WRITE}$ output as a function of the Am29203 instruction inputs.

On the Am29203, when $\overline{IEN}$ is HIGH, the Q register and Sign Compare Flip-Flop contents are preserved. When $\overline{IEN}$ is LOW, the Q register and Sign Compare Flip-Flop can be written according to the Am29203 instruction. The Sign Compare Flip-Flop is an on-chip flip-flop which is used during an Am29203 divide operation (see Figure B). On the Am29203, $\overline{IEN}$ controls internal writing, but does not affect $\overline{WRITE}$. The $\overline{IEN}$ signal can then be controlled separately at each chip to facilitate byte operations.

Programming the Am29203 Slice Position

Tying the $\overline{LSS}$ input LOW programs the slice to operate as a least significant slice (LSS) and enables the $\overline{WRITE}$ output signal onto the $\overline{WRITE}/\overline{MSS}$ bidirectional I/O pin. When $\overline{LSS}$ is tied HIGH, the

$\overline{\text{WRITE}}/\overline{\text{MSS}}$ pin becomes an input pin; tying the $\overline{\text{WRITE}}/\overline{\text{MSS}}$ pin HIGH programs the slice to operate as an intermediate slice (IS) and tying it LOW programs the slice to operate as a most significant slice (MSS). The $\overline{\text{W}}/\overline{\text{MSS}}$ pin must be tied HIGH through a resistor. $\overline{\text{W}}/\overline{\text{MSS}}$ and $\overline{\text{LSS}}$ should not be connected together. See Figure 2 of applications.

Am29203 SPECIAL FUNCTIONS

The Am29203 provides 16 Special Functions which facilitate the implementation of the following operations:

- Single- and Double-Length Normalization
- Two's Complement Division
- Unsigned and Two's Complement Multiplication
- Conversion Between Two's Complement and Sign/Magnitude Representation
- Incrementation and Decrementation by One or Two
- BCD add, subtract, and divide by two
- Single- and double-precision BCD to Binary and Binary to BCD conversion.

Table 4 defines these Special Functions.

The Single-Length and Double-Length Normalization functions can be used to adjust a single-precision or double-precision floating point number in order to bring its mantissa within a specified range.

Three Special Functions which can be used to perform a two's complement, non-restoring divide operation are provided by the Am29203. These functions provide both single- and double-precision divide operations and can be performed in "n" clock cycles, where "n" is the number of bits in the quotient.

The Unsigned Multiply Special Function and the two Two's Complement Multiply Special Functions can be used to multiply two n-bit, unsigned or two's complement numbers, respectively, in n clock cycles. These functions utilize the conditional add and shift algorithm. During the last cycle of the two's complement multiplication, a conditional subtraction, rather than addition, is performed because the sign bit of the multiplier carries negative weight.

The Sign/Magnitude-Two's Complement Special Function can be used to convert number representation systems. A number expressed in Sign/Magnitude representation can be converted to the Two's Complement representation, and vice-versa, in one clock cycle.

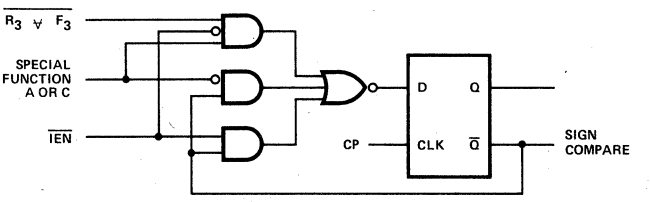
The Increment by One or Two Special Function can be used to increment an unsigned or two's complement number by one or two. This is useful in 16-bit word, byte-addressable machines, where the word addresses are multiples of two.

The BCD arithmetic special functions can be used to add or subtract two BCD numbers and generate a valid BCD result in one microcycle. In addition a BCD divide by two adjust instruction can be used to obtain a valid BCD representation after shifting a number down by one bit.

The BCD/Binary conversion special function instructions facilitate single- and double-precision algorithms to convert from BCD to Binary and from Binary to BCD.

Refer to Am29203 applications section for a more detailed description of these Special Functions.

Figure B. Sign Compare Flip-Flop



The sign compare signal appears at the Z output of the most significant slice during special functions C, D and E, F. Refer to Table 5.

TABLE 5. Am29203 STATUS OUTPUTS

(Hex) $I_8I_7I_6I_5$	(Hex) $I_4I_3I_2I_1$	I_0	Gi (i = 0 to 3)	Pi (i = 0 to 3)	C_{n+4}	$\overline{P}$/OVR		$\overline{G}$/N		Z ($\overline{OE}_Y$ = LOW)		
						Most Sig Slice	Other Slices	Most Sig Slice	Other Slices	Most Sig Slice	Intermediate Slice	Least Sig Slice
X	0	X	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	1	X	$\overline{R}_i \wedge S_i$	$\overline{R}_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	2	X	$R_i \wedge S_i$	$R_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	3	X	$R_i \wedge S_i$	$R_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	4	X	0	S_i	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	5	X	0	$\overline{S}_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	6	X	0	R_i	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	7	X	0	$\overline{R}_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	8	X	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	9	X	$\overline{R}_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	A	X	$R_i \wedge S_i$	$R_i \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	B	X	$\overline{R}_i \wedge S_i$	$\overline{R}_i \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	C	X	$R_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	D	X	$\overline{R}_i \wedge \overline{S}_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	E	X	$R_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	F	X	$\overline{R}_i \wedge \overline{S}_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
0	0	L	0 if Z = L $R_i \wedge S_i$ if Z = H	S_i if Z = L $R_i \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
1	0	L	0	S_i	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
1	8	L	0	S_i	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
2	0	L	0 if Z = L $R_i \wedge S_i$ if Z = H	S_i if Z = L $R_i \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
3	0	L	(Note 6)	(Note 7)	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
4	0	L	(Note 1)	(Note 2)	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
5	0	L	0	S_i if Z = L $\overline{S}_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3 if Z = L $F_3 \forall S_3$ if Z = H	$\overline{G}$	S_3	Input	Input
6	0	L	0 if Z = L $\overline{R}_i \wedge S_i$ if Z = H	S_i if Z = L $\overline{R}_i \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
7	0	L	0	S_i	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
8	0	L	0	S_i	(Note 3)	Q_2 Q_1	$\overline{P}$	Q_3	$\overline{G}$	$\overline{Q_0Q_1Q_2Q_3}$	$\overline{Q_0Q_1Q_2Q_3}$	$\overline{Q_0Q_1Q_2Q_3}$
9	0	L	0	S_i	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Q_0Q_1Q_2Q_3}$	$\overline{Q_0Q_1Q_2Q_3}$	$\overline{Q_0Q_1Q_2Q_3}$
9	8	L	0	S_i	0	0	0	F_3	$\overline{G}$	$\overline{Q_0Q_1Q_2Q_3}$	$\overline{Q_0Q_1Q_2Q_3}$	$\overline{Q_0Q_1Q_2Q_3}$
A	0	L	0	S_i	(Note 4)	F_2 F_1	$\overline{P}$	F_3	$\overline{G}$	(Note 5)	(Note 5)	(Note 5)
B	0	L	$R_i \wedge S_i$	R_i S_i	$G \vee PC_n$	(Note 8)	(Note 8)	(Note 9)	(Note 9)	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
C	0	L	$R_i \wedge S_i$ if Z = L $\overline{R}_i \wedge S_i$ if Z = H	$R_i \vee S_i$ if Z = L $\overline{R}_i \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input
D	0	L	$R_i \wedge \overline{S}_i$	$R_i \vee \overline{S}_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
E	0	L	$R_i \wedge S_i$ if Z = L $\overline{R}_i \wedge S_i$ if Z = H	$R_i \vee S_i$ if Z = L $\overline{R}_i \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input
F	0	L	$\overline{R}_i \wedge S_i$	$\overline{R}_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$

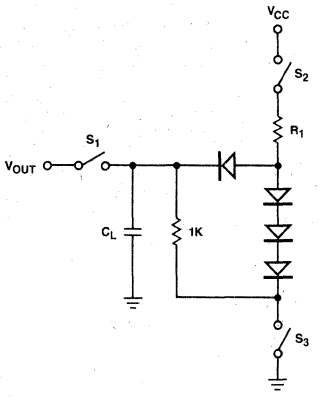
Notes:
1. If $\overline{LSS}$ is LOW, $G_0 = S_0$ and $G_{1,2,3} = 0$. If $\overline{LSS}$ is HIGH, $G_{0,1,2,3} = 0$.
2. If $\overline{LSS}$ is LOW, $P_0 = 1$ and $P_{1,2,3} = S_{1,2,3}$. If $\overline{LSS}$ is HIGH, $P_i = S_i$.
3. At the most significant slice, $C_{n+4} = Q_3 \forall Q_2$. At other slices, $C_{n+4} = G \vee PC_n$.
4. At the most significant slice, $C_{n+4} = F_3 \forall F_2$. At other slices, $C_{n+4} = G \vee PC_n$.
5. $Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3\overline{F}_0\overline{F}_1\overline{F}_2\overline{F}_3$.
6. If $\overline{LSS}$ is LOW, $G_0 = 0$ and $G_{1,2,3} = S_{1,2,3}$. If $\overline{LSS}$ is HIGH, $G_{0,1,2,3} = S_{0,1,2,3}$.
7. If $\overline{LSS}$ is LOW, $P_0 = S_0$ and $P_{1,2,3} = 1$. If $\overline{LSS}$ is HIGH, $P_{0,1,2,3} = 1$.
8. On all slices $\overline{P} = (\overline{P}_0 + \overline{P}_3)(\overline{P}_0 + \overline{G}_2)(\overline{P}_0 + \overline{G}_1 + \overline{P}_2)$.
9. On all slices $\overline{G} = \overline{G}_3(\overline{G}_0 + \overline{G}_1 + \overline{P}_2)(\overline{G}_0 + \overline{G}_1)(\overline{P}_1 + \overline{G}_2)(\overline{P}_3 + \overline{P}_1 \cdot \overline{P}_2 \cdot \overline{G}_0)$.

L = LOW = 0
H = HIGH = 1
$\vee$ = OR
$\wedge$ = AND
$\forall$ = EXCLUSIVE OR
$P = P_3P_2P_1P_0$
$G = G_3 \vee G_2P_3 \vee G_1P_2P_3 \vee G_0P_1P_2P_3$
$C_{n+3} = G_2 \vee G_1P_2 \vee G_0P_1P_2 \vee C_nP_0P_1P_2$

5

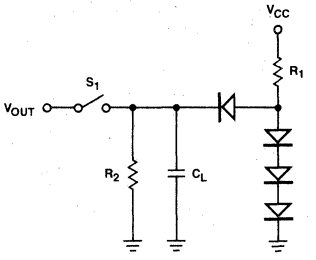
TEST OUTPUT LOAD CONFIGURATIONS FOR Am29203

A. THREE-STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

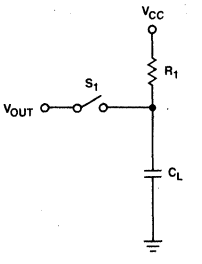
B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

C. OPEN-COLLECTOR OUTPUTS



$$R_1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in hand in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all A.C. tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

TEST OUTPUT LOADS FOR Am29203

Pin#	Pin Label	Test Circuit	R_1	R_2
1	QIO_0	A	458	1K
11	C_{n+4}	B	478	3K
12	$\overline{P}$/OVR	B	383	3K
14	$\overline{G}$/N	B	212	1.5K
16-19	Y_{0-3}	A	241	1K
20	SIO_0	A	458	1K
21	SIO_3	A	458	1K
22	Z	C	281	–
23-26	DB_{0-3}	A	458	1K
40	$\overline{WRITE}/\overline{MSS}$	A	458	1K
48	QIO_3	A	458	1K

For additional information on testing, see section "Guidelines on Testing Am2900 Family Devices."

OPERATING RANGES (over which DC, switching, and functional specifications apply)

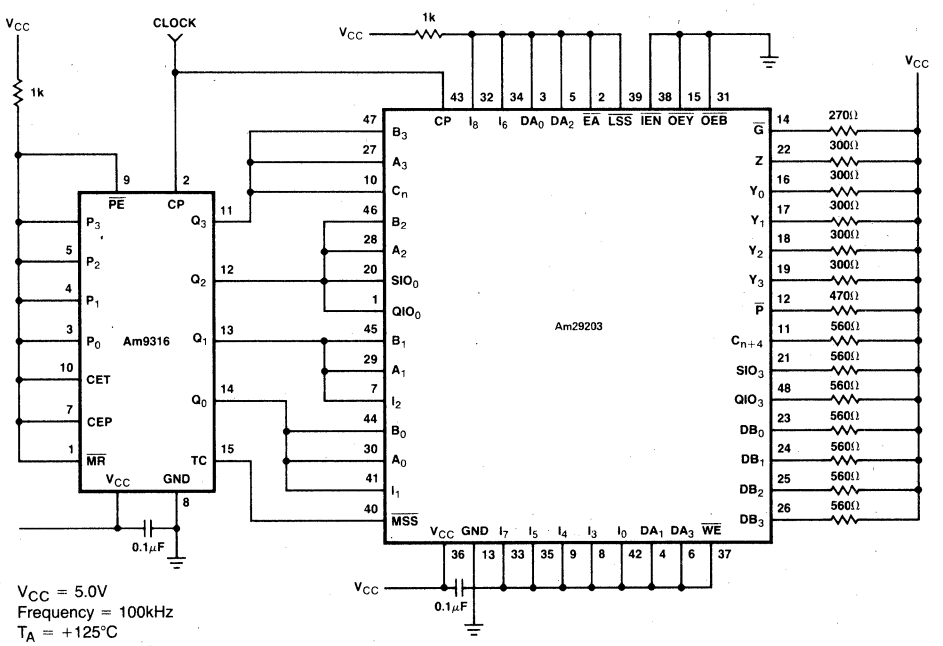
Range	Part Number Suffix	Temperature	V_{CC}
COM'L	PC, PCB, DC, DCB, XC	T_A = 0 to 70°C	4.75 to 5.25V
MIL	DM, DMB, FM, FMB, XM	T_C = −55 to +125°C	4.50 to 5.50V

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5 to +V_{CC} max.
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

5

Am2903 Burn-in and Life Test Circuit



V_{CC} = 5.0V
Frequency = 100kHz
T_A = +125°C
All registers are 1/4 watt ±5%
This circuit conforms to MIL-STD-883, Methods 1005 and 1015, Condition D.
One Am9316 Can Drive Maximum of Five Am2903s.

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5−8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

Am29203
DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.6mA Y_0-Y_3, $\overline{G}$/N		2.4			Volts
			I_{OH} = −800μA DB_{0-3}, $\overline{P}$/OVR SIO_0, SIO_3, QIO_0, QIO_3, $\overline{WRITE}$, C_{n+4}		2.4			
I_{CEX}	Output Leakage Current for Z Output (Note 4)	V_{CC} = MIN., V_{OH} = 5.5V V_{IN} = V_{IH} or V_{IL}					250	μA
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} = or V_{IL}	Y_0, Y_1, Y_2 Y_3, Z	I_{OL} = 20mA (COM'L)			0.5	Volts
				I_{OL} = 16mA (MIL)				
			DB_0, DB_1, DB_2, DB_3	I_{OL} = 12mA (COM'L)			0.5	
				I_{OL} = 8.0mA (MIL)				
			$\overline{G}$/N	I_{OL} = 18mA			0.5	
			$\overline{P}$/OVR	I_{OL} = 10mA			0.5	
			C_{n+4}, SIO_0 SIO_3, QIO_0 QIO_3, $\overline{WRITE}$	I_{OL} = 8.0mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 6)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 6)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V (Note 4)	C_n				−3.6	mA
			Y_0, Y_1, Y_2, Y_3				−1.13	
			I_0, I_1, I_2, I_3, I_4 DA_0, DA_1, DA_2, DA_3				−0.72	
			SIO_0, SIO_3, QIO_0, QIO_3, $\overline{MSS}$, DB_0, DB_1, DB_2, DB_3				−0.77	
			All other inputs				−0.36	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V (Note 4)	C_n				200	μA
			Y_0, Y_1, Y_2, Y_3				110	
			I_0-I_4, DA_0-DA_3				40	
			SIO_0, SIO_3, QIO_0, QIO_3, DB_{0-3}, $\overline{MSS}$				90	
			All other inputs				20	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (HIGH Impedance) Output Current	V_{CC} = MAX., (Note 4)	Y_0-Y_3	V_O = 2.4V			110	μA
				V_O = 0.5V			−1130	
			DB_{0-3}, QIO_0, QIO_3, SIO_0, SIO_3, $\overline{WRITE}$/$\overline{MSS}$	V_O = 2.4V			90	
				V_O = 0.5V			−770	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = MAX + 0.5V V_O = 0.5V			−30		−85	mA
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX.	T_A = 25°C			220	335	mA
			COM'L	T_A = 0 to 70°C			350	
				T_A = 70°C			291	
			MIL	T_C = −55 to 125°C			395	
				T_C = 125°C			258	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Y_{0-3}, DB_{0-3}, $SIO_{0,3}$, $QIO_{0,3}$ and WRITE/MSS are three state outputs internally connected to TTL inputs. Z is an open-collector output internally connected to a TTL input. Input characteristics are measured under conditions such that the outputs are in the OFF state.
5. Worst case I_{CC} is at minimum temperature.
6. These input levels provide zero noise immunity and should only be static tested in a noise-free environment (not functionally tested).

I. Am29203 Guaranteed Commercial Range Performance

The tables below specify the performance of the Am29203 over the commercial operating range of 0 to +70°C, with V_{CC} from 4.75 to 5.25V. All data are in ns, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

Clock and Write Pulse Characteristics
All Functions

Minimum Clock LOW Time	30	ns
Minimum Clock HIGH Time	30	ns
Minimum Time CP and WE both LOW to Write	30	ns

Enable/Disable Times
All Functions

From	To	Enable	Disable	
OEY	Y_i	27	25	ns
OEB	DB_i	31	25	ns
I_8	SIO_0, SIO_3		25	ns
I_{8765}	QIO_0, QIO_3		60	ns
I_{43210}	QIO_0, QIO_3	65	60	ns
$\overline{LSS}$	$\overline{WRITE}$	31	25	ns

Note:
1. C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

Combinational Delays
All Functions

From Input \ To Output	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A Address (Arith. Mode)	86	81	69	110	86	108	–	–	–	84	94	115
B Address	99	88	81	123	99	112	49	–	–	94	104	140
A Address (Logic Mode)	87	–	68	111	89	–	–	–	–	79	94	115
B Address	84	–	73	108	84	–	49	–	–	84	90	120
DA Inputs (Arith. Mode)	63	60	49	87	64	89	–	–	–	60	70	101
DB Inputs	61	59	47	85	62	84	–	–	–	62	68	98
DA Inputs (Logic Mode)	64	–	48	88	66	–	–	–	–	61	72	101
DB Inputs	55	–	32	79	57	–	–	–	–	52	61	93
$\overline{EA}$	59	53	42	83	59	83	–	–	–	57	64	98
C_n	40	30	–	64	40	58	–	–	–	38	46	67
I_0	52	48	36	76	52	63	–	49	*	50*	58*	93*
I_{4321}	71	65	72	95	69	84	–	49	*	66*	73*	105*
I_{8765}	42	–	–	66	–	–	–	50	60*	42*	45*	42*
$\overline{IEN}$	–	–	–	–	–	–	–	22	–	–	–	–
SIO_3, SIO_0	26	–	–	50	–	–	–	–	–	–	29	36
Clock	87	87	71	111	88	108	37	–	40	84	92	105
Y	–	–	–	24	–	–	–	–	–	–	–	–
$\overline{MSS}$	44	–	44	68	44	44	–	–	–	44	46	44

Note: A "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct the data is determined by something else.

Setup and Hold Times
All Functions
CAUTION: READ NOTES. NA = Not Applicable; no timing constraint.

From Input \ To Output	With Respect to this Signal	HIGH-to-LOW Set-up	HIGH-to-LOW Hold	LOW-to-HIGH Set-up	LOW-to-HIGH Hold	Comment
Y	Clock	NA	NA	20	3	To store Y in RAM or Q
$\overline{WE}$ HIGH	Clock	25	Note 2	Note 2	0	To Prevent Writing
$\overline{WE}$ LOW	Clock	NA	NA	30	0	To Write into RAM
A, B as Sources	Clock	27	3	NA	NA	See Note 3
B as a Destination	Clock and WE both LOW	6	Note 4	Note 4	3	To Write Data only into the Correct B Address
QIO_0, QIO_3	Clock	NA	NA	21	3	To Shift Q
I_{8765}	Clock	24	Note 5	Note 5	0	
$\overline{IEN}$ HIGH	Clock	30	Note 2	Note 2	0	To Prevent Writing
$\overline{IEN}$ LOW	Clock	NA	NA	30	0	To Write into Q
I_{43210}	Clock	24	–	68	0	See Note 6

Notes:
1. For setup times from all inputs not specified, the setup time is computed by calculating the delay to stable Y outputs and then allowing the Y setup time. Even if the RAM is not being loaded, the Y setup time is necessary to setup the Q register. All unspecified hold times are less than or equal to zero relative to the clock LOW-to-HIGH edge.
2. $\overline{WE}$ controls writing into the RAM. $\overline{IEN}$ controls writing into Q and, indirectly, controls $\overline{WE}$ through the write output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must be HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
3. A and B addresses must be set-up pri tion to capture data in latches at P
4. Writing occurs when CP and W dress should be stable durin
5. Because I_{8765} control the RAM and Q, they shoul time unless $\overline{IEN}$ is HI
6. The set-up time prior to occurs in parallel with the s to-LOW transition and the cloc time requirement on I_{43210}, relati transition, is the longer of (1) the L → H, and (2) the sum of the set- H → L and the clock LOW time.

II. Am29203 Guaranteed Military Range Performance

The tables below specify the performance of the Am29203 over the military operating range of −55 to +120°C, with V_{CC} from 4.50 to 5.50V. All data are in ns, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

Clock and Write Pulse Characteristics
All Functions

Minimum Clock LOW Time	40	ns
Minimum Clock HIGH Time	40	ns
Minimum Time CP and WE both LOW to Write	40	ns

Enable/Disable Times
All Functions

From	To	Enable	Disable	
OEY	Y_i	27	25	ns
OEB	DB_i	34	25	ns
I_8	SIO_0, SIO_3		25	ns
I_{8765}	QIO_0, QIO_3		60	ns
I_{43210}	QIO_0, QIO_3	70	60	ns
$\overline{LSS}$	$\overline{WRITE}$	34	25	ns

Note:
1. C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

Combinational Delays
All Functions

From Input \ To Output	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z (s)	N	OVR	DB	$\overline{WRITE}$	QIO_0 QIO_3	SIO_0	SIO_3	SIO_0 Parity
A Address (Arith. Mode)	91	85	72	116	92	115	–	–	–	89	98	120
B Address	101	93	84	126	102	118	52	–	–	97	106	148
A Address (Logic Mode)	92	–	72	117	93	–	–	–	–	84	98	120
B Address	86	–	73	111	89	–	52	–	–	86	92	125
DA Inputs (Arith. Mode)	64	62	51	89	66	94	–	–	–	62	71	107
DB Inputs	63	60	48	88	63	89	–	–	–	64	68	100
DA Inputs (Logic Mode)	65	–	51	90	67	–	–	–	–	62	72	108
DB Inputs	56	–	32	81	57	–	–	–	–	52	63	100
$\overline{EA}$	60	56	43	85	60	87	–	–	–	58	64	103
C_n	40	30	–	65	40	59	–	–	–	38	46	69
I_0	52	50	36	77	52	66	–	53	*	51*	58*	96*
I_{4321}	72	69	73	97	71	88	–	53	*	66*	75*	111*
I_{8765}	44	–	–	69	–	–	–	50	65*	42*	45*	42*
$\overline{IEN}$	–	–	–	–	–	–	–	24	–	–	–	–
SIO_3, SIO_0	26	–	–	51	–	–	–	–	–	–	29	36
Clock	89	90	74	114	89	116	39	–	42	91	96	110
Y	–	–	–	25	–	–	–	–	–	–	–	–
$\overline{MSS}$	45	–	44	70	44	44	–	–	–	44	46	44

Note: A "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with a * is the delay to correct data on an enabled output. A * shown without a number means the output is disabled by the input or it is enabled but the delay to correct the data is determined by something else.

Setup and Hold Times
All Functions
CAUTION: READ NOTES. NA = Not Applicable; no timing constraint.

Input	With Respect to this Signal	HIGH-to-LOW Set-up	HIGH-to-LOW Hold	LOW-to-HIGH Set-up	LOW-to-HIGH Hold	Comment
Y	Clock	NA	NA	23	3	To store Y in RAM or Q
$\overline{WE}$ HIGH	Clock	25	Note 2	Note 2	0	To Prevent Writing
$\overline{WE}$ LOW	Clock	NA	NA	35	0	To Write into RAM
A, B as Sources	Clock	38	3	NA	NA	See Note 3
B as a Destination	Clock and WE both LOW	6	Note 4	Note 4	3	To Write Data only into the Correct B Address
QIO_0, QIO_3	Clock	NA	NA	23	3	To Shift Q
I_{8765}	Clock	24	Note 5	Note 5	0	
$\overline{IEN}$ HIGH	Clock	30	Note 2	Note 2	0	To Prevent Writing into Q
$\overline{IEN}$ LOW	Clock	NA	NA	30	0	To Write into Q
I_{43210}	Clock	24	–	74	0	See Note 6

Notes:
1. For setup times from all inputs not specified, the setup time is computed by calculating the delay to stable Y outputs and then allowing the Y setup time. Even if the RAM is not being loaded, the Y setup time is necessary to setup the Q register. All unspecified hold times are less than or equal to zero relative to the clock LOW-to-HIGH edge.
2. $\overline{WE}$ controls writing into the RAM. $\overline{IEN}$ controls writing into Q and, indirectly, controls $\overline{WE}$ through the write output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must be HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
3. A and B addresses must be set-up prior to clock LOW transition to capture data in latches at RAM output.
4. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
5. Because I_{8765} control the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, preventing writing.
6. The set-up time prior to the clock LOW-to-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-to-LOW transition and the clock LOW time. The actual set-up time requirement on I_{43210}, relative to the clock LOW-to-HIGH transition, is the longer of (1) the set-up time prior to clock L → H, and (2) the sum of the set-up time prior to clock H → L and the clock LOW time.

Am29203 Guaranteed Commercial Range Performance

The tables below specify the guaranteed performance of the Am29203 over the commercial operating range of 0 to +70°C, with V_{CC} from 4.75 to 5.25V. All data are in ns, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

Clock Characteristics
All Functions

Minimum Clock LOW Time	30	ns
Minimum Clock HIGH Time	30	ns
Minimum Time CP and WE* both LOW to Write	30	ns

Output Enable/Disable Times
All Functions

Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

From	To	Enable	Disable	
OEY	Y_i	27	25	ns
OEB	DB_i	31	25	ns
I_8	SIO_0, SIO_3		25	ns
I_{8765}	QIO_0, QIO_3		60	ns
I_{43210}	QIO_0, QIO_3	65	60	ns
$\overline{LSS}$	$\overline{WRITE}$	31	25	ns

Combinational Propagation Delays
C_L = 50pF
Standard Functions

From Input \ To Output	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	DA	DB	$\overline{WR}$	QIO_0	QIO_3	SIO_0	SIO_3	SIO_0 Parity
A Addr	68	56	52	72	61	67	24	–	–	–	–	42	62	78
B Addr	65	52	49	70	60	64	–	24	–	–	–	38	60	76
DA	55	40	43	62	50	53	–	–	–	–	–	30	53	65
DB	59	49	44	65	54	55	–	–	–	–	–	32	56	60
C_n	40	18	–	32	26	24	–	–	–	–	–	21	27	38
I_{8-0}	64 (1)	65	50	72 (1)	59	68	–	–	26	21 (2)	20 (2)	53 (2)	60 (2)	74 (2)
Clock	60	43	43	62	55	59	21	21	–	21	21	36	55	60
$\overline{IEN}$	–	–	–	–	–	–	–	–	22	–	–	–	–	–
$\overline{MSS}$	44	–	44	68	44	44	–	–	–	–	–	44	46	44
SIO_{0-3}	23	–	–	29	–	–	–	–	–	–	–	–	29	17

Notes:
1. A (1) means the output depends on the other input disabled or enabled by the controlling inputs. The number shown is based on all other inputs enabled with valid data applied.
2. A (2) means the output is enabled or disabled by the input. See Output Enable/Disable times. A number shown with a (2) is the delay to correct data on an enabled output.
3. A "–" means the delay path does not exist.

Setup and Hold Times
All Functions

CAUTION: READ NOTES. NA = Not Applicable; no timing constraint.

From Input \ To Output	With Respect to this Signal	HIGH-to-LOW Setup	HIGH-to-LOW Hold	LOW-to-HIGH Setup	LOW-to-HIGH Hold	Comment
Y	Clock	NA	NA	18	3	To Store Y in RAM or Q
$\overline{WE}$ HIGH	Clock	10	Note 2	Note 2	0	To Prevent Writing
$\overline{WE}$ LOW	Clock	NA	NA	16	0	To Write into RAM
A, B as Sources	Clock	17	3	NA	NA	See Note 3
B as a Destination	Clock and WE both LOW	6	Note 4	Note 4	3	To Write Data Only into the Correct B Address
QIO_0, QIO_3	Clock	NA	NA	14	3	To Shift Q
I_{8765}	Clock	12	Note 5	Note 5	0	
$\overline{IEN}$ HIGH	Clock	20	Note 2	Note 2	0	To Prevent Writing into Q
$\overline{IEN}$ LOW	Clock	NA	NA	18	0	To Write into Q
I_{43210}	Clock	12	–	35	0	See Note 6

Notes:
1. For setup times from all inputs not specified in Table B, the setup time is computed by calculating the delay to stable Y outputs and then allowing the Y setup time. Even if the RAM is not being loaded, the Y setup time is necessary to setup the Q register. All unspecified hold times are less than or equal to zero relative to the clock LOW-to-HIGH edge.
2. $\overline{WE}$ controls writing into the RAM. $\overline{IEN}$ controls writing into Q. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must be HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW setup times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
3. A and B addresses must be setup prior to clock LOW transition to capture data in latches at RAM output.
4. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
5. Because I_{8765} control the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, preventing writing.
6. The setup time prior to the clock LOW-to-HIGH transition occurs in parallel with the setup time prior to the clock HIGH-to-LOW transition and the clock LOW time. The actual setup time requirement on I_{43210}, relative to the clock LOW-to-HIGH transition, is the longer of (1) the setup time prior to clock L → H, and (2) the sum of the setup time prior to clock H → L and the clock LOW time.

5

Am29203 Guaranteed Commercial Range Performance

The Am29203 switching characteristics are a function of the power supply voltage, the temperature, and the operating mode of the device. The data has been condensed onto the tables on the following pages. These tables define the speeds of the combinational paths for each of the special functions.

Data is shown in bold type where different from the timing specifications for the standard functions. Except where otherwise noted, data is taken with inputs switching between 0 and 3.0V at 1V/ns, with the measurement point at 1.5V. Outputs are measured at 1.5V and are loaded with C_L = 50pF and maximum DC load.

SPECIAL FUNCTIONS

(Hex) $I_8I_7I_6I_5$	I_4	(Hex) $I_3I_2I_1I_0$	Available On	Special Function
0	L	0	Am2903 Am29203	Unsigned Multiply
1	L	0	Am29203	BCD to Binary Conversion
1	H	0	Am29203	Multiprecision BCD to Binary
2	L	0	Am2903 Am29203	Two's Complement Multiply
3	L	0	Am29203	Decrement by One or Two
4	L	0	Am2903 Am29203	Increment by One or Two
5	L	0	Am2903 Am29203	Sign/Magnitude Two's Complement
6	L	0	Am2903 Am29203	Two's Complement Multiply Last Cycle
7	L	0	Am29203	BCD Divide by Two

(Hex) $I_8I_7I_6I_5$	I_4	(Hex) $I_3I_2I_1I_0$	Available On	Special Function
8	L	0	Am2903 Am29203	Single Length Normalize
9	L	0	Am29203	Binary to BCD Conversion
9	H	0	Am29203	Multiprecision Binary to BCD
A	L	0	Am2903 Am29203	Double Length Normalize and First Divide Op
B	L	0	Am29203	BCD Add
C	L	0	Am2903 Am29203	Two's Complement Divide
D	L	0	Am29203	BCD Subtract
E	L	0	Am2903 Am29203	Two's Complement Divide Correction and Remainder
F	L	0	Am29203	BCD Subtract

BCD Functions
SF_1, SF_7, SF_9, SF_B, SF_D, SF_F

From Input \ To Output	Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	DA	DB	$\overline{WR}$	QIO_0	QIO_3	SIO_0	SIO_3	SIO_0 Parity
A, Addr	76	65	76	84	76	76	24	–	–	–	–	76	52	85
B, Addr	82	65	76	83	76	76	–	24	–	–	–	76	52	85
DA	60	41	53	58	53	53	–	–	–	–	–	–	–	–
DB	59	41	50	50	50	50	–	–	–	–	–	58	41	79
C_n	40	22	–	32	34	34	–	–	–	–	–	38	44	43
I_{8-0}	77 (1)	55	44	70 (1)	59	62	–	–	26	21 (2)	21 (2)	81 (2)	55 (2)	86 (2)
Clock	76	59	70	78	70	70	21	21	–	21	21	70	46	83
$\overline{IEN}$	–	–	–	–	–	–	–	–	22	–	–	–	–	–
$\overline{MSS}$	44	–	44	68	44	44	–	–	–	–	–	44	46	44
SIO_{0-3}	23	–	–	29	–	–	–	–	–	–	–	–	–	17

Notes:

1. A (1) means the output depends on the other input disabled or enabled by the controlling inputs. The number shown is based on all other inputs enabled with valid data applied.
2. A (2) means the output is enabled or disabled by the input. See Output Enable/Disable times. A number shown with a (2) is the delay to correct data on an enabled output.
3. A "–" means the delay path does not exist.

Guaranteed Combinational Delays
T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V
Special Functions 0, 2, 6

From Input \ To Output		Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	SIO_0	DA, DB	QIO_{0-3}	$\overline{WR}$
A, B Addr	MSS	**68**	56	–	–	61	67	42	24	–	–
	IS	68	56	52	–	–	–	42	24	–	–
	LSS	68	56	52	–	–	–	42	24	–	–
DA, DB	MSS	**59**	49	–	–	–	–	32	–	–	–
	IS	59	49	48	–	–	–	32	–	–	–
	LSS	59	49	48	–	–	–	32	–	–	–
C_n	MSS	40	18	–	–	–	–	21	–	–	–
	IS	40	18	–	–	–	–	21	–	–	–
	LSS	40	18	–	–	–	–	21	–	–	–
I_{0-5}	MSS	84 (1)	**67**	–	–	**74**	**74**	**68**	–	**21**	–
	IS	84 (1)	**67**	**74**	–	–	–	**68**	–	**21**	–
	LSS	84 (1)	**67**	**74**	**31**	–	–	**68**	–	**21**	26
Clock	MSS	**60**	43	–	–	55	59	36	21	21	–
	IS	60	43	43	–	–	–	36	21	21	–
	LSS	60	43	43	**29**	–	–	36	21	21	–
Z	MSS	**71**	**52**	–	–	**64**	**60**	**42**	–	–	–
	IS	**71**	**52**	**50**	–	–	–	**42**	–	–	–
$\overline{IEN}$		–	–	–	–	–	–	–	–	–	22
SIO_{0-3}		23	–	–	–	–	–	–	–	–	–

SF 0:
F = S + C_n if Z = 0
S + R + C_n if Z = 1
Y_3 = C_{n+4} (MSS)
Z = Q_0 (LSS)

SF 2:
F = S + C_n if Z = 0
R + S + C_n if Z = 1
Y_3 = $F_3 \oplus$ OVR (MSS)
Z = Q_0 (LSS)

SF 6:
F = S + C_n if Z = 0
S − R − 1 + C_n if Z = 1
Y_3 = OVR $\oplus$ F_3 (MSS)
Z = Q_0 (LSS)

Guaranteed Combinational Delays
T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V
Special Functions 3 and 4

From Input \ To Output		Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	SIO_3 Parity	DA, DB	QIO_{0-3}	$\overline{WR}$
A, B Addr	MSS	68	56	–	72	61	67	78	24	–	–
	IS	68	56	52	72	–	–	78	24	–	–
	LSS	68	56	52	72	–	–	78	24	–	–
DA, DB	MSS	59	49	–	65	54	55	65	–	–	–
	IS	59	49	48	65	–	–	65	–	–	–
	LSS	59	49	48	65	–	–	65	–	–	–
C_n	MSS	40	18	–	32	26	24	38	–	–	–
	IS	40	18	–	32	–	–	38	–	–	–
	LSS	40	18	–	32	–	–	38	–	–	–
I_{0-5}	MSS	**54**	**52**	–	**54**	**52**	**64**	**74**	–	**21**	–
	IS	**54**	**52**	**40**	**54**	–	–	**74**	–	**21**	–
	LSS	**54**	**52**	**40**	**54**	–	–	**74**	–	**21**	–
Clock	MSS	60	43	–	62	55	59	60	21	21	–
	IS	60	43	43	62	–	–	60	21	21	–
	LSS	60	43	43	62	–	–	60	21	21	–
Z	Z is an Output for all Slices										
$\overline{IEN}$		–	–	–	–	–	–	–	–	–	22
SIO_{0-3}		23	–	–	–	–	–	–	–	–	–

SF 3:
F = S − 2 + C_n

SF 4:
F = S + 1 + C_n

Guaranteed Combinational Delays
T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V
Special Function 5

From Input \ To Output		Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	SIO_3	DA, DB	QIO_{0-3}	$\overline{WR}$
A, B Addr	MSS	**96**	56	–	43	**96**	67	78	24	–	–
	ISS	68	56	52	–	–	–	78	24	–	–
	LSS	68	56	52	–	–	–	78	24	–	–
DA, DB	MSS	**90**	49	–	–	**89**	55	65	–	–	–
	ISS	59	49	48	–	–	–	65	–	–	–
	LSS	59	49	48	–	–	–	65	–	–	–
C_n	MSS	40	18	–	–	**28**	24	38	–	–	–
	ISS	40	18	–	–	–	–	38	–	–	–
	LSS	40	18	–	–	–	–	38	–	–	–
I_{0-5}	MSS	**94**	**64**	–	**31**	**94**	**88**	**97**	–	**21**	–
	ISS	**83**	**64**	**64**	–	–	–	**86**	–	**21**	–
	LSS	**83**	**64**	**64**	–	–	–	**86**	–	**21**	26
Clock	MSS	**97**	43	–	**38**	**89**	59	60	21	21	–
	ISS	60	43	64	–	–	–	60	21	21	–
	LSS	60	43	64	–	–	–	60	21	21	–
Z	IS	**62**	**44**	**43**	–	–	–	**85**	–	–	–
	LSS	**62**	**44**	**43**	–	–	–	**85**	–	–	–
$\overline{IEN}$		–	–	–	–	–	–	–	–	–	–
SIO_{0-3}		23	–	–	–	–	–	–	–	–	22

SF 5:
F = S + C_n if Z = 0
$\overline{S}$ + C_n if Z = 1
Y_3 = $S_3 \oplus F_3$ (MSS)
Z = S_3 (MSS)

Guaranteed Combinational Delays
T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V
Special Function 8

From Input \ To Output		Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	SIO_3	DA, DB	QIO_{0-3}	$\overline{WR}$
A, B Addr	MSS	68	–	–	–	–	–	62	24	–	–
	IS	68	56	52	–	–	–	62	24	–	–
	LSS	68	56	52	–	–	–	62	24	–	–
DA, DB	MSS	59	–	–	–	–	–	56	–	–	–
	IS	59	49	48	–	–	–	56	–	–	–
	LSS	59	49	48	–	–	–	56	–	–	–
C_n	MSS	40	–	–	–	–	–	27	–	–	–
	IS	40	18	–	–	–	–	27	–	–	–
	LSS	40	18	–	–	–	–	27	–	–	–
I_{0-5}	MSS	**61**	**43**	–	**28**	**23**	**24**	**60**	–	**21**	–
	IS	**52**	**66**	**40**	**28**	–	–	**60**	–	**21**	–
	LSS	**52**	**66**	**40**	**28**	–	–	**60**	–	**21**	26
Clock	MSS	60	**27**	–	**29**	**23**	**28**	55	21	21	–
	IS	60	43	43	**29**	–	–	55	21	21	–
	LSS	60	43	43	**29**	–	–	55	21	21	–
Z	IS	Z is an Output for all Slices									
	LSS										
$\overline{IEN}$		–	–	–	–	–	–	–	–	–	22
SIO_{0-3}		23	–	–	–	–	–	–	–	–	–

SF 8:
F = S + C_n
C_{n+4} = $Q_3 \oplus Q_2$ (MSS)
OVR = $Q_2 \oplus Q_1$ (MSS)
N = Q_3 (MSS)
Z = $\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$

Guaranteed Combinational Delays
T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V
Special Function A

From Input \ To Output		Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	SIO_3	DA, DB	QIO_{0-3}	$\overline{WR}$
A, B Addr	MSS	68	56	–	72	**43**	**64**	62	24	–	–
	ISS	68	56	52	72	–	–	62	24	–	–
	LSS	68	56	52	72	–	–	62	24	–	–
DA, DB	MSS	59	**50**	–	72	**43**	**58**	56	–	–	–
	ISS	59	49	48	72	–	–	56	–	–	–
	LSS	59	49	48	72	–	–	56	–	–	–
C_n	MSS	40	**37**	–	**27**	**25**	**28**	27	–	–	–
	ISS	40	18	–	**27**	–	–	27	–	–	–
	LSS	40	18	–	**27**	–	–	27	–	–	–
I_{0-5}	MSS	61 (1)	**70**	–	**52**	**52**	**66**	**67**	–	**21**	–
	ISS	52 (1)	**66**	**40**	**52**	–	–	**60**	–	**21**	–
	LSS	52 (1)	**66**	**40**	**52**	–	–	**60**	–	**21**	–
Clock	MSS	60	**44**	–	**42**	**38**	**49**	**43**	21	21	–
	ISS	60	43	43	**42**	–	–	55	21	21	–
	LSS	60	43	43	**42**	–	–	55	21	21	–
Z	Z is an Output for all Slices										
$\overline{IEN}$		23	–	–	–	–	–	–	–	–	22
SIO_{0-3}		23	–	–	–	–	–	–	–	–	–

SF A:
F = S + C_n
N = F_3 (MSS)
SIO_3 = $F_3 \oplus R_3$ (MSS)
C_{n+4} = $F_3 \oplus F_2$ (MSS)
OVR = $F_2 \oplus F_1$ (MSS)
Z = $\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3\overline{F}_0\overline{F}_1\overline{F}_2\overline{F}_3$

Guaranteed Combinational Delays
T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V
Special Function C

From Input \ To Output		Y	C_{n+4}	$\overline{G}$, $\overline{P}$	Z	N	OVR	SIO_3	DA, DB	QIO_{0-3}	$\overline{WR}$
A, B Addr	MSS	68	56	–	–	61	67	62	24	–	–
	IS	68	56	52	–	–	–	62	24	–	–
	LSS	68	56	52	–	–	–	62	24	–	–
DA, DB	MSS	59	49	–	–	54	55	56	–	–	–
	IS	59	49	48	–	–	–	56	–	–	–
	LSS	59	49	48	–	–	–	56	–	–	–
C_n	MSS	40	18	–	–	26	24	40	–	–	–
	IS	40	18	–	–	–	–	27	–	–	–
	LSS	40	18	–	–	–	–	27	–	–	–
I_{0-5}	MSS	91 (1)	**70**	–	**28**	**77**	**72**	**89**	–	**21**	–
	IS	68 (1)	**65**	**61**	–	–	–	**66**	–	**21**	–
	LSS	68 (1)	**65**	**61**	–	–	–	**66**	–	**21**	26
Clock	MSS	60	43	–	**30**	55	59	**88**	21	21	–
	IS	60	43	43	–	–	–	55	21	21	–
	LSS	60	43	43	–	–	–	55	21	21	–
Z	IS	**62**	**44**	**46**	–	–	–	**65**	–	–	–
	LSS	**62**	**44**	**46**	–	–	–	**65**	–	–	–
$\overline{IEN}$		–	–	–	–	–	–	–	–	–	22
SIO_{0-3}		23	–	–	–	–	–	–	–	–	–

SF C:
F = R + S + C_n if Z = 0
S – R – 1 + C_n if Z = 1
SIO_3 = $\overline{F_3 \oplus R_3}$ (MSS)
Z = $F_3 \oplus R_3$ (MSS) from previous cycle

5

Guaranteed Combinational Delays
T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V
Special Function E

From Input \ To Output		Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	SIO_3	DA, DB	QIO_{0-3}	$\overline{WR}$
A, B Addr	MSS	68	56	–	–	61	67	62	24	–	–
	IS	68	56	52	–	–	–	62	24	–	–
	LSS	68	56	52	–	–	–	62	24	–	–
DA, DB	MSS	59	49	–	–	54	55	56	–	–	–
	IS	59	49	48	–	–	–	56	–	–	–
	LSS	59	49	48	–	–	–	56	–	–	–
C_n	MSS	40	18	–	–	26	24	27	–	–	–
	IS	40	18	–	–	–	–	27	–	–	–
	LSS	40	18	–	–	–	–	27	–	–	–
I_{0-5}	MSS	**91**	**70**	–	**28**	**77**	**72**	**79**	–	**21**	–
	IS	**68**	**65**	**61**	–	–	–	**66**	–	**21**	–
	LSS	**68**	**65**	**61**	–	–	–	**66**	–	**21**	26
Clock	MSS	60	43	–	**30**	55	59	55	21	21	–
	IS	60	43	43	–	–	–	55	21	21	–
	LSS	60	43	43	–	–	–	55	21	21	–
Z	IS	**62**	**44**	**46**	–	–	–	**65**	–	–	–
	LSS	**62**	**44**	**46**	–	–	–	**65**	–	–	–
$\overline{IEN}$		–	–	–	–	–	–	–	–	–	22
SIO_{0-3}		23	–	–	–	–	–	–	–	–	–

SF E:

$F = R + S + C_n$ if $Z = 0$

$S - R - 1 + C_n$ if $Z = 1$

$Z = \overline{F_3} \oplus \overline{R_3}$ (MSS) from previous cycle

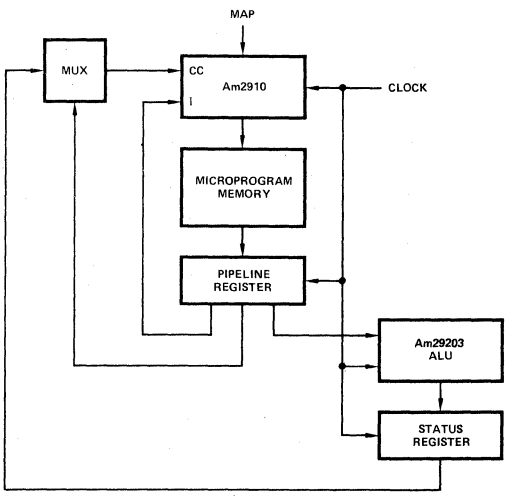
USING THE Am29203

Am29203 APPLICATIONS

The Am29203 is designed to be used in microprogrammed systems. Figure 1 illustrates a recommended architecture. The control and data inputs to the Am29203 normally will all come from registers clocked at the same time as the Am29203. The register inputs come from a ROM or PROM – the "microprogram store." This memory contains sequences of microinstructions which apply the proper control signals to the Am29203s and other circuits to execute the desired operation.

The address lines of the microprogram store are driven from the Am2910 Microprogram Sequencer. This device has facilities for storing an address, incrementing an address, jumping to any address, and linking subroutines. The Am2910 is controlled by some of the bits coming from the microprogram store. Essentially, these bits are the "next instruction" control.

Figure 1. Typical Microprogram Architecture.



One Level Pipeline Based System

Note that with the microprogram register in between the microprogram memory store and the Am29203s, a microinstruction accessed on one cycle is executed on the next cycle. As one microinstruction is executed, the next microinstruction is being read from microprogram memory. In this configuration, system speed is improved because the execution time in the Am29203s occurs in parallel with the access time of the microprogram store. Without the "pipeline register," these two functions must occur serially.

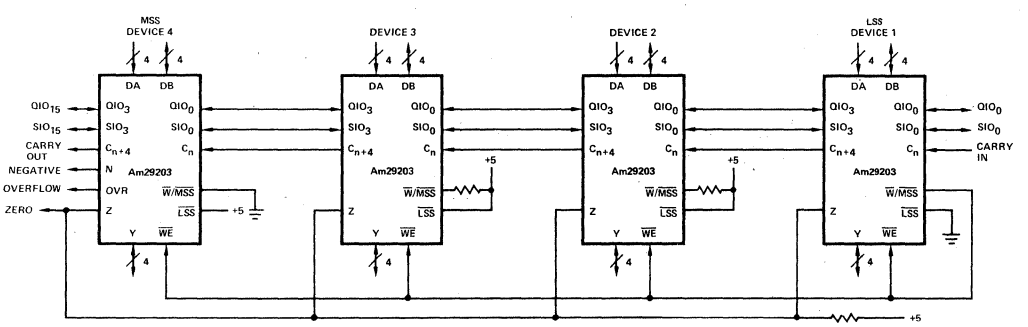
Expansion of the Am29203

The Am29203 is a four-bit CPU slice. Any number of Am29203s can be interconnected to form CPUs of 8, 16, 32, or more bits, in four-bit increments. Figure 2 illustrates the interconnection of four Am29203s to form a 16-bit CPU, using ripple carry.

With the exception of the carry interconnection, all expansion schemes are the same. The QIO_3 and SIO_3 pins are bidirectional left/right shift lines at the MSB of the device. For all devices except the most significant, these lines are connected to the QIO_0 and SIO_0 pins of the adjacent more significant device. These connections allow the Q registers of all Am29203s to be shifted left or right as a contiguous n-bit register, and also allow the ALU output data to be shifted left or right as a contiguous n-bit word prior to storage in the RAM. At the LSB and MSB of the CPU, the shift pins should be connected to a shift multiplexer which can be controlled by the microcode to select the appropriate input signals to the shift inputs.

Device 1 has been defined as the least significant slice (LSS) and its $\overline{LSS}$ pin has accordingly been grounded. The Write/Most Significant Slice ($\overline{WRITE}/\overline{MSS}$) pin of device 1 is now defined as being the Write output, which may now be used to drive the write enable ($\overline{WE}$) signal common to the four devices. Devices 2 and 3 are designated as intermediate slices and hence the $\overline{LSS}$ and $\overline{WRITE}/\overline{MSS}$ pins are tied HIGH. Caution: $\overline{W}/\overline{MSS}$ must be tied to V_{CC} through a resistor; $\overline{W}/\overline{MSS}$ and $\overline{LSS}$ may not be shorted directly together. Device 4 is designated the most significant slice ($\overline{MSS}$) with the $\overline{LSS}$ pin tied HIGH and the $\overline{WRITE}/\overline{MSS}$ pin held LOW. The open collector, bidirectional Z pins are tied together for detecting zero or for inter-chip communication for some special instruction. The Carry-Out (C_{n+4}) is connected to the Carry-In (C_n) of the next chip in the case of ripple carry. For a faster carry scheme, an Am2902 may be employed (as shown in Figure 3) such that the $\overline{G}$ and $\overline{P}$ outputs of the Am2903 are connected to the appropriate $\overline{G}$ and $\overline{P}$ inputs of the Am2902, while the C_{n+x}, C_{n+y}, and C_{n+z} outputs of the Am2902 are connected to the C_n input of the appropriate Am2903. Note that $\overline{G}$/N and $\overline{P}$/OVR pin functions are device dependent. The most significant slice outputs N and OVR while all other slices output $\overline{G}$ and $\overline{P}$.

Figure 2. 16-Bit CPU with Ripple Carry.



The $\overline{IEN}$ pin of the Am29203 allows the option of conditional instruction execution. If $\overline{IEN}$ is LOW, all internal clocking is enabled, allowing the latches, RAM, and Q Register to function. If $\overline{IEN}$ is HIGH, the RAM and Q Register are disabled. The RAM is controlled by $\overline{IEN}$ if $\overline{WE}$ is connected to the $\overline{WRITE}$ output.

It would be appropriate at this point to mention that the Am29203 may be microcoded to work in either two-or three-address architecture modes. The two-address modes allow A+B→B while the three-address mode makes possibleA+B→C. Implementation of a three-address architecture is made possible by varying the timing of $\overline{IEN}$ in relationship to the external clock and changing the B address as shown in Figure 4. This technique is discussed in more detail under Memory Expansion.

Parity

The Am29203 computes parity on a chosen word when the instruction bits I_{5-8} have the values of 4_{16} to 7_{16} as shown in Table 3. The computed parity is the result of the exclusive OR of the individual ALU outputs and SIO_3. Parity output is found on SIO_0. Parity between devices may be cascaded by the interconnection of the SIO_0 and SIO_3 ports of the devices as shown in Figure 3. The equation for the parity output at SIO_0 port of device 1 is given by $SIO_0 = F_{15} \vee F_{14} \vee F_{13} \vee \ldots \vee F_1 \vee F_0 \vee SIO_{15}$.

Figure 3. 16-Bit CPU with Carry Look Ahead.

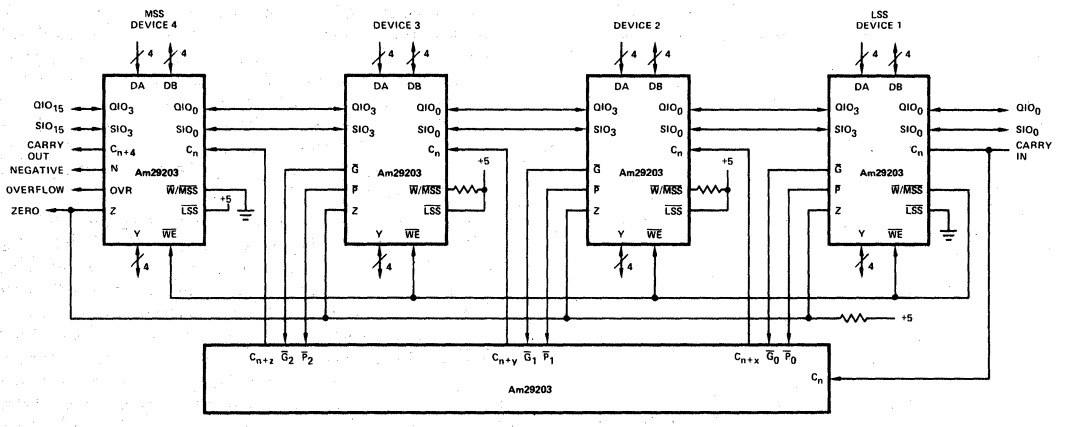


Figure 4. Relationship of $\overline{IEN}$ and Clock During Two Address and Three Address Modes.

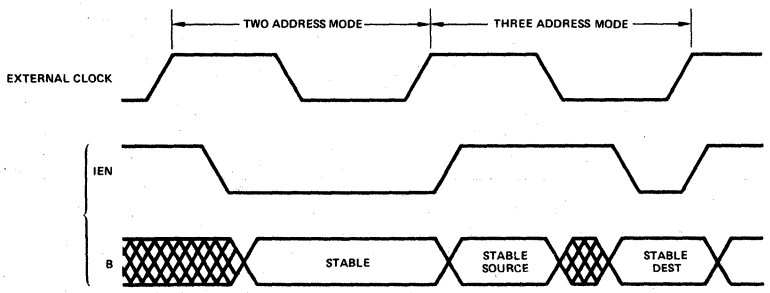
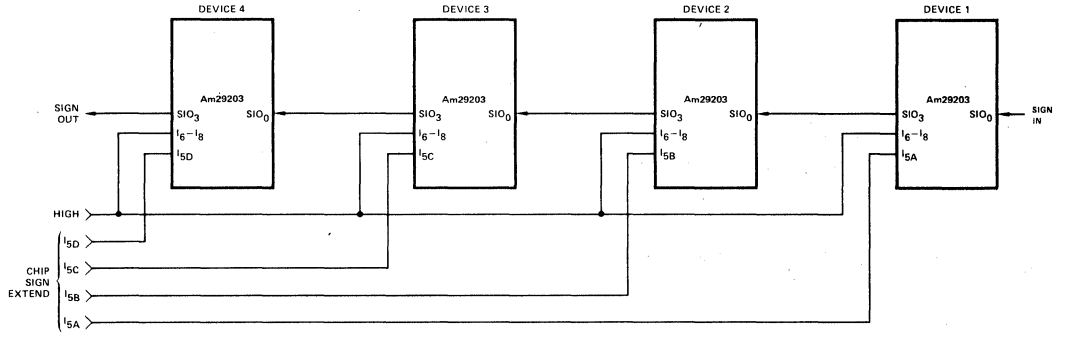


Figure 5. Sign Extend.



Sign Extend

Sign extension across any number of Am29203 devices can be done in one microcycle. Referring again to the table of instructions (Table 3), the sign extend instruction (Hex instruction E) on I_{5-8} causes the sign present at the SIO_0 port of a device to be extended across the device and appear at the SIO_3 port and at the Y outputs. If the least significant bit of the instruction (bit I_5) is HIGH, Hex instruction F is present on I_{5-8}, commanding a shifter pass instruction. At this time, F_3 of the ALU is present on the SIO_3 output pin. It is then possible to control the extension of the sign across chip boundaries by controlling the state of I_5 when I_{6-8} are HIGH. Figure 5 outlines the Am29203 in sign extend mode. With I_{6-8} held HIGH, the individual chip sign extend is controlled by $I_{5A\text{-}D}$. If, for example, I_{5A} and I_{5B} are HIGH while I_{5C} and I_{5D} are LOW, the signal present at the boundaries of devices 2 and 3 (F_3 of device 2) will be extended across devices 3 and 4 at the SIO_3 pin of device 4. The output of the four devices will be available at their respective Y data ports. The next positive edge of the clock will load the Y outputs into the address selected by the B port. Hence, the results of the sign extension is stored in the RAM.

SPECIAL FUNCTIONS

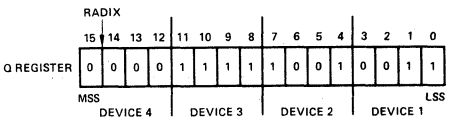
When $I_{0-4} = 0$, the Am2903 is in the Special Function mode. In this mode, both the source and destination are controlled by I_{5-8}. The Special Functions are in essence special microinstructions that are used to reduce the number of microcycles needed to execute certain functions in the Am29203.

NORMALIZATION, SINGLE- AND DOUBLE-LENGTH

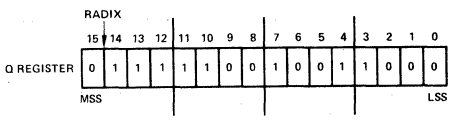
Normalization is used as a means of referencing a number to a fixed radix point. Normalization strips out all leading sign bits such that the two bits immediately adjacent to the radix point are of opposite polarity.

Normalization is commonly used in such operations as fixed-to-floating point conversion and division. The Am2903 provides for normalization by using the Single-Length and Double-Length Normalize commands. Figure 6a represents the Q Register of a 16-bit processor which contains a positive number. When the Single-Length Normalize command is applied, each positive edge of the clock will cause the bits to shift toward the most significant bit (bit 15) of the Q Register. Zeros are shifted in via the QIO_0 port. When the bits on either side of the radix point (bits 14 and 15) are of opposite value, the number is considered to be normalized as shown in Figure 6b. The event of normalization is externally indicated by a HIGH level on the C_{n+4} pin of the most significant slice (C_{n+4} MSS = Q_3 MSS $\forall$ Q_2 MSS).

Figure 6.



a) Unnormalized Positive Number.



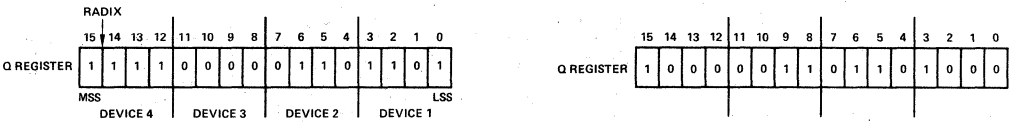
b) Normalized Positive Number.

There are also provisions made for a normalization indication via the OVR pin one microcycle before the same indication is available on the C_{n+4} pin (OVR = Q_2 MSS $\forall$ Q_1 MSS). This is for use in applications that require a stage of register buffering of the normalization indication.

Since a number comprised of all zeros is not considered for normalization, the Am29203 indicates when such a condition arises. If the Q Register is zero and the Single-Length Normalization command is given, a HIGH level will be present on the Z line. The sign output, N, indicates the sign of the number stored in the Q register, Q_3 MSS. An unnormalized negative number (Figure 7a) is normalized in the same manner as a positive number. The results of single-length normalization are shown in Figure 7b. The device interconnection for single-length normalization is outlined in Figure 8. During single length normalization, the number of shifts performed to achieve normalization can be counted and stored in one of the working registers. This can be achieved by forcing a HIGH at the C_n input of the least significant slice, since during this special function the ALU performs the function [B] + C_n and the result is stored in B.

Normalizing a double-length word can be done with the Double-Length Normalize command which assumes that a user-selected RAM Register contains the most significant portion of the word to be normalized while the Q Register holds the least significant half (Figure 9). The device interconnection for double-length normalization is shown in Figure 10. The C_{n+4}, OVR, N, and Z outputs of the most significant slice perform the same functions in double-length normalization as they did in single-length normalization except that C_{n+4}, OVR, and N are derived from the output of the ALU of the most significant slice in the case of double-length normalization, instead of the Q Register of the most significant

Figure 7.



a) Unnormalized Negative Single Length Number.

b) Normalized Negative Single Length Number.

Figure 8. Single Length Normalize.

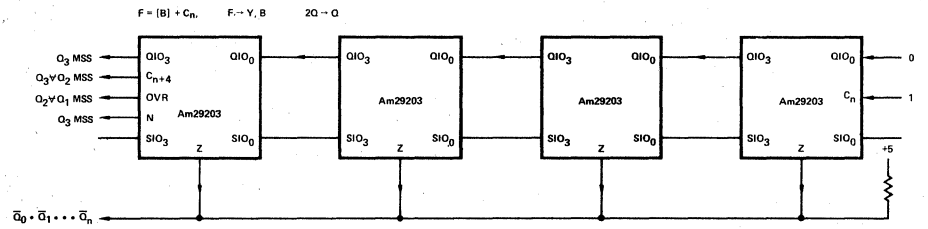


Figure 9. Double Length Word.

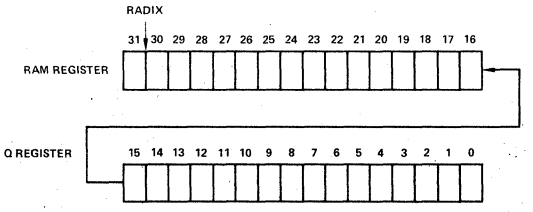
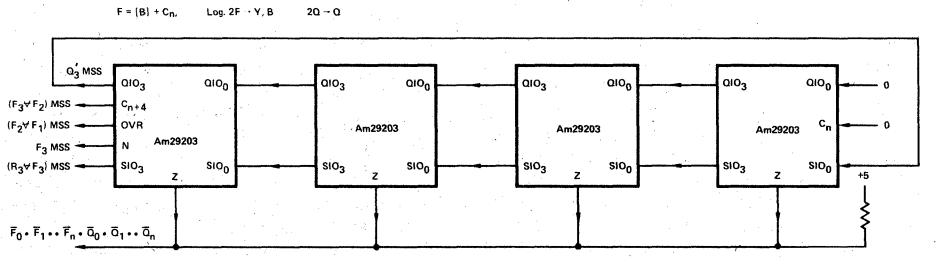


Figure 10. Double Length Normalize.



slice as in single-length normalization. A high-level Z line in double-length normalization reveals that the outputs of the ALU and Q Register are both zero, hence indicating that the double-length word is zero.

When double-length normalization is being performed, shift counting is done either with an extra microcycle or with an external counter.

SIGN MAGNITUDE, TWO'S COMPLEMENT CONVERSION

As part of the special instruction set, the Am2903 can convert between two's complement and sign/magnitude representations. Figure 11 illustrates the interconnection needed for sign magnitude/two's complement conversion. The word to be converted is applied to the S input port of the ALU (from the RAM B port or the DB I/O port). The C_n input of device 1 is connected to the Z pin. The sign bit (S_3MSS) is brought out on the Z line and informs the other ALU's if the conversion is being performed on a negative or positive number. If the number to be converted is the most negative number in two's complement [i.e., 100 . . . 00 (-2^n)], an overflow indication will occur. This is because -2^n is one greater than any number that can be represented in sign magnitude notation and hence an attempted conversion to sign magnitude from -2^n will cause an overflow. When minus zero in sign magnitude notation (100 . . . 0) is converted to two's complement notation, the correct result is obtained (0 . . .0).

INCREMENT BY ONE OR TWO

Incrementation by One or Two is made possible by the Special Function of the same name. This command is quite useful in the case of byte addressable words. Referencing Figure 12, a word may be incremented by one if C_n is LOW or incremented by two if C_n is HIGH.

UNSIGNED MULTIPLY

This Special Function allows for easy implementation of unsigned multiplication. Figure 13 is the unsigned multiply flow chart. The algorithm requires that initially the RAM word addressed by Address port B be zero, that the multiplier be in the Q Register, and that the multiplicand be in the register addressed by Address port A. The initial conditions for the execution of the algorithm are that: 1) register R_0 be reset to zero; 2) the multiplicand be in R_1; and 3) the multiplier be in R_2. The first operation transfers the multiplier, R_2, to the Q Register. The Unsigned Multiply instruction is then executed 16 times. During the Unsigned Multiply instruction, R_0 is addressed by RAM address port B and the multiplicand is addressed by RAM address port A.

When the unsigned Multiply command is given, the Z pin of device 1 becomes an output while the Z pins of the remaining devices are specified as inputs as shown in Figure 15. The Z output of device 1 is the same state as the least significant bit of the multiplier in the Q Register. The Z output of device 1 informs the ALU's of all the slices, via their Z pins, to add the partial product (referenced by the B address port) to the mul-

5

Figure 11. 2's Complement ⟷ Sign/Magnitude.

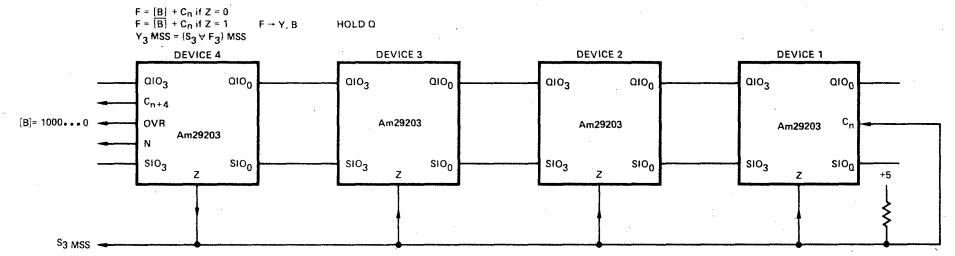


Figure 12. Increment by 2/1.

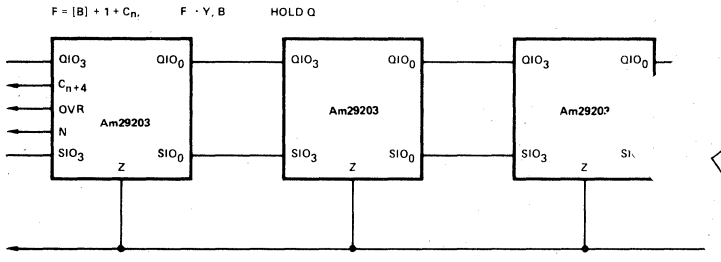
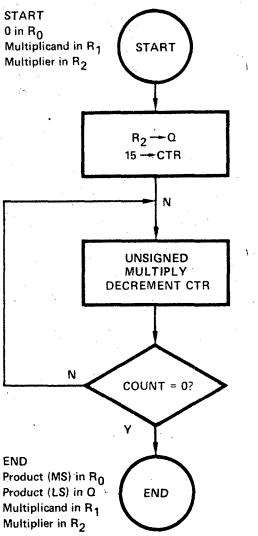


Figure 13. Unsigned 16 X 16 Multiply Flowchart.



ti d (referenced by the A address port) if Z = 1. If Z = 0, ti put of the ALU is simply the partial product (referenced by B address port). Since C_n is held LOW, it is not a factor he computation. Each positive-going edge of the clock will i ernally shift the ALU outputs toward the least significant bit ar l simultaneously store the shifted results in the register selected by the B address port, thus becoming the new partial sum. During the down shifting process, the C_{n+4} generated in device 4 is internally shifted into the Y_3 position of device 4. At this time, one bit of the multiplier will down shift out of the QIO_0 ports of each device into the QIO_3 port of the next less significant slice. The partial product is shifted down between chips in a like manner, between the SIO_0 and SIO_3 ports, with SIO_0 of device 1 being connected to QIO_3 of device 4 for purposes of constructing a 32-bit long register to hold the 32-bit product. At the finish of the 16 x 16 multiply, the most significant 16 bits of the product will be found in the register referenced by the B address lines while the least significant 16 bits are stored in the Q Register. Using a typical Computer Control Unit (CCU), as shown in Figure 16, the unsigned multiply operation requires only two lines of microcode, as shown in Figure 17, and is executed in 17 microcycles.

TWO'S COMPLEMENT MULTIPLICATION

The algorithm for two's complement multiplication is illustrated by Figure 14. The initial conditions for two's complement multiplication are the same as for the unsigned multiply operation. The Two's Complement Multiply Command is applied for 15 clock cycles in the case of a 16 x 16 multiply. During the down shifting process the term N⊻OVR generated in device 4 is internally shifted into the Y_3 position of device 4. The data flow shown in Figure 15 is still valid. After 15 cycles, the sign bit of the multiplier is present at the Z output of device 1. At this time, the user must place the Two's Complement Multiply Last cycle command on the instruction lines. The interconnection for this instruction is shown in Figure 18. On the next positive edge of the clock, the Am2903 will adjust the partial product, if the sign of the multiplier is negative, by subtracting out the two's complement representation of the multiplicand. If the sign bit is positive, the partial product is not adjusted. At this point, two's complement multiplication is completed. Using a typical CCU, as shown in Figure 16, the two's complement multiply operation requires only three lines of microcode, as shown in Figure 19, and is executed in 17 microcycles.

Figure 14. 2's Complement 16 X 16 Multiply.

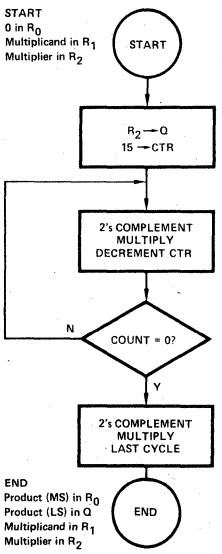
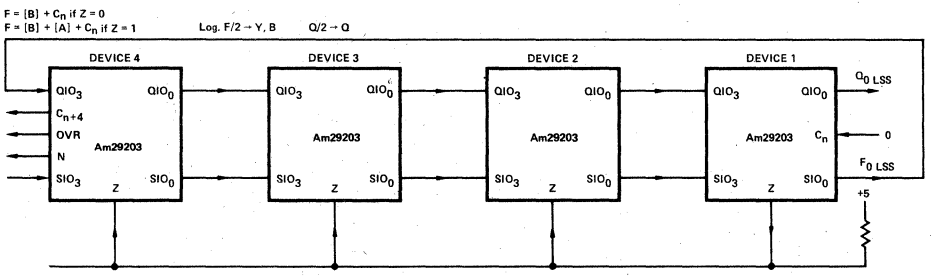


Figure 15. Multiply.



ed multiply, C_{n+4} MSS is internally shifted into position Y_3 MSS; 2's complement multiply N V OVR is internally shifted into MSS.

Figure 16. Typical Computer Control Unit (CCU).

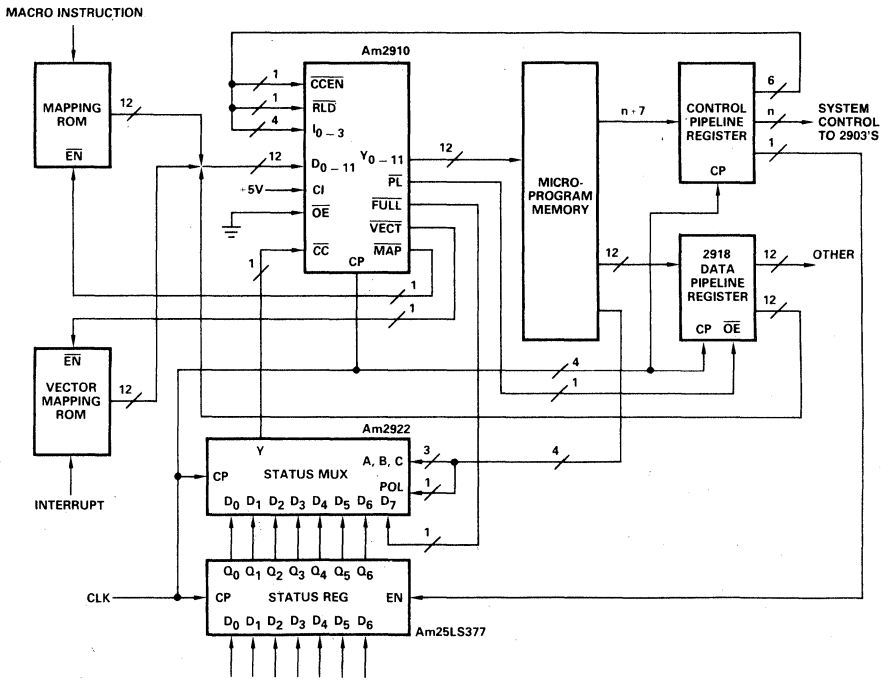
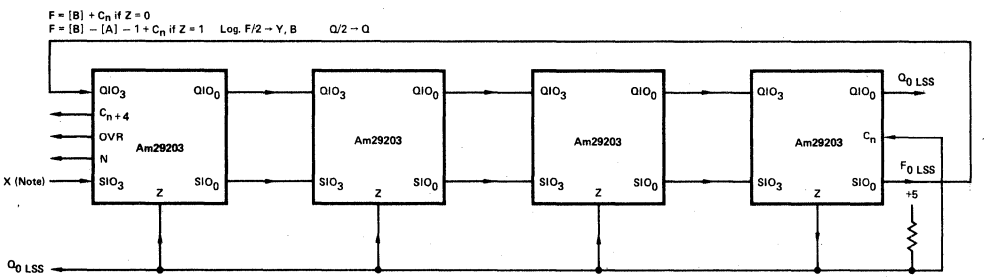


Figure 17. Micro Code for Unsigned 16 X 16 Multiply.

Micro Memory Address	Am2910 Inst	Data Pipeline Reg.	I_0	I_4-I_1	I_8-I_5	$\overline{OEB}$	$\overline{OEY}$	A_3-A_0	B_3-B_0	C_n	Comment
n	LDCT	$00F_{16}$	H	6	6	X	X	R_2	X	0	Load Counter & $R_2 \rightarrow Q$
n+1	RPCT	n+1	0	0	0	0	0	R_1	R_0	0	Unsigned Multiply

Figure 18. 2's Complement Multiply, Last Cycle.



Note: N V OVR is internally shifted into position Y_3 MSS.

Figure 19. Microcode for 2's Complement 16 x 16 Multiply.

Memory Address	Am2910 Inst	Data Pipeline Reg.	I_0	$I_4 - I_1$	$I_8 - I_5$	$\overline{OEB}$	$\overline{OEY}$	$A_3 - A_0$	$B_3 - B_0$	C_n	Comment
n	LDCT	$00E_{16}$	X	6	6	X	X	R_2	X	0	Load Counter & $R_2 \rightarrow Q$
n+1	RPCT	n+1	0	0	2	0	0	R_1	R_0	0	2's Complement Multiply
n+2	X	X	0	0	6	0	0	R_1	R_0	Z	2's Complement Multiply (Last Cycle)

TWO'S COMPLEMENT DIVISION

Three instructions on the Am29203 can be used to microcode signed integer division. The algorithm is a non-restoring four-quadrant division, with different preamble and postamble microcode for single- and double-precision integer division.

Single-precision signed integer divide is the most straightforward. Other than division by zero, there is only one case when an overflow results, namely when the most negative number (-2^{n-1}) is divided by -1. This case is detected by the postamble, and does not require separate tests of dividend and divisor in the preamble.

Single-precision division begins by loading the Q register with the dividend. Following this, the negative bit of the status register is tested and the dividend register is loaded with all ones or all zeros so as to sign extend the Q register. The dividend is now a double-precision integer, with the least significant half in the Q register and the most significant half in the dividend register. This double-precision integer is then shifted up one position in preparation for the divide.

The division starts with the First Divide Operation applied to the divisor register (A address) and the dividend register (B address). This operation computes the quotient sign as the exclusive OR of dividend and divisor sign, and shifts it into the least significant position of the Q register while simultaneously upshifting the double-precision dividend one bit. The First Divide Operation also updates the Sign Compare Flip-Flop (in the MSS) with the exclusive NOR of the dividend and divisor sign, which determines whether the next operation will be an add or a subtract.

The stage is now set for repeated execution of the divide step. Provided correct shift linkages externally (SIO_3 on the MSS to QIO_0 on the LSS, and QIO_3 on MSS to SIO_0 on the LSS), each execution of the divide step computes a new quotient bit by either adding the divisor to the dividend (if the sign compare flip-flop is HIGH) or subtracting the divisor from the dividend (if the sign compare flip-flop is LOW), and then producing the exclusive NOR of the sign of the result and the divisor sign as the new quotient bit and the new value of the sign compare flip-flop. The upshifted result replaces the partial remainder in the dividend register. The divide step must be repeated $n-2$ times for n bit signed integers. Note that the sign compare flip-flop resides on the most significant slice, and controls the other slices through the zero pin which becomes an input on the intermediate and least significant slices for this operation.

The divide correction step also adds or subtracts the divisor from the partial remainder in the dividend register, but does not upshift the result. The quotient bit shifted into the Q register by this step is always a 1. This means that the quotient produced by the divide algorithm is always odd; in half the cases, of course, this guess is wrong, and must be corrected. At each step of the divide algorithm, the result of the previous guess is corrected and a new guess is made. Since correction lags computation of the quotient bits by one step, after the last step there is still one correction needed.

After the divide correction step, the product of quotient and divisor plus the remainder is guaranteed to be equal to the dividend. However, the magnitude of the quotient may be off by one, the sign of the remainder may be wrong, and the magnitude of the remainder may lie between the magnitude of the divisor and zero.

In general, correction is needed when the sign of the remainder and initial dividend differ. For positive quotients, the correction is performed by subtracting one from the quotient and adding the divisor back to the remainder. For negative quotients, the correction is performed by adding one to the quotient and subtracting the divisor from the remainder.

A special case arises when the dividend is negative and the remainder at the end of the division is exactly zero. Since zero appears to be positive in two's complement, it appears that correction is necessary, whereas in fact it is not. This case is easily detected by testing the remainder for zero after the last divide step, and terminating the algorithm if it is. A related problem arises with negative dividends when the partial remainder becomes exactly zero in an intermediate step of the division. Once again, the algorithm sees this as a change of sign, and records the wrong quotient bit. However, in such cases, the final remainder always has the same magnitude as the divisor, but has the same sign as the dividend. Since the multiplicative rule is still satisfied, this means that the quotient is too small in magnitude by one. This case is detected by adding the magnitude of the divisor to the remainder and testing for zero, and the correction is the opposite of the "normal" correction: positive quotients are incremented, and negative quotients are decremented. (The remainder should be made exactly zero). Note that the single case that produces overflow for single-precision signed integer divide may be detected by checking the overflow in this correction step.

The complete algorithm is shown in Figure 20. It is important to remember that the zero status available at the end of the divide correction step is the sign compare flip-flop output, and does not reflect whether the final partial remainder is zero or not. Also, in interruptible systems, the division steps must not be interrupted, because the sign compare flip-flop cannot be saved or restored on the interrupt. However, division *can* be stopped and resumed provided no instruction in between affects the state of the sign compare flip-flop. Some examples of the correction for single-precision signed divide are shown in Figure 21.

The shift linkage requirements for the divide steps are summarized in Figures 22, 23 and 24. These figures should be used as guidelines when microcoding the fields controlling the shift multiplexers in the 2904 for the divide steps.

Except for the overflow problem, the same algorithm with minor variations in the preamble implements double-precision division. Of course, in this case, sign extension is not needed; instead, the least significant half of the double-precision dividend is loaded in the Q register, the most significant half remains in the "dividend" registers, and, after the initial upshift by one bit, the divide steps are executed exactly as before.

When a double-precision signed integer is divided by a single-precision signed integer, overflow occurs when the quotient requires more than n bits to represent. For example 2^{2n-2} divided by 1 requires 2n bits to represent. A subset of these cases of overflow is the case where the *magnitude* of the quotient requires exactly n bits to represent, leaving no bits for the sign; and a special case of this is where the quotient magnitude is 2^{n-1}. The preamble to the divide presented below detects the first two cases in that order, and the postamble detects the last case.

The principle of overflow detection used here is to first calculate the quotient sign, and then calculate $n+1$ bits of quotient. There is an overflow when bits $n+1$ and n differ from the sign. This detects cases where the quotient requires more than $n+1$ bits to represent (quotient bit $n+1$ differs from the quotient sign), and where the quotient requires exactly $n+1$ bits to represent (quotient bit $n+1$ is the same as the quotient sign but quotient bit n differs from the quotient sign). Unfortunately quotients with a magnitude of 2^{n-1} do not fit this scheme: when the quotient is -2^{n-1}, this test indicates an overflow, and when the quotient is 2^{n-1} (an overflow), this test does not show an overflow. In other words, when there is a disagreement between the n^{th} quotient bit and the quotient sign, it does not necessarily indicate an overflow; and it is not until all the quotient bits are calculated that it can be decided whether there was an overflow or not. This irregularity is a consequence of the asymmetry of the two's complement number system.

The implementation of this algorithm on the Am29203 is simplified by using a flip-flop on the SIO_3 line out of the MSS to store a copy of the new quotient bit calculated each cycle. If this flip-flop output is connected to a sequencer test multiplexer input, then testing of quotient bits can be pipelined. This is useful in the preamble for overflow detection and in the postamble for the correction steps.

The microcode for the double-precision divide is outlined in Figure 25. The divide operation is first applied to the dividend and divisor without the initial upshift of the dividend. This calculates the quotient sign and updates the sign compare flip-flop. At the end of the cycle, the complement of the quotient sign is setup at the input to the external flip-flop, which can be tested in the next cycle to determine the quotient sign. However, the divide first operation has the side-effect of upshifting the dividend. This side-effect is undesirable because it prevents the divide step from calculating the $n+1^{th}$ quotient bit. For this reason, the dividend is shifted down again with the sign bit of the status register selected as the linkage in. Following this, a divide step is executed and the algorithm terminated on overflow if the quotient bit calculated by the divide steps is different from the sign bit. The algorithm proceeds to calculate the n^{th} quotient bit. If the n^{th} quotient bit agrees with the quotient sign, there still may be an overflow if the quotient turns out to be 2^{n-1}; and if the nth quotient bit disagrees with the quotient sign, there still may not be an overflow if the quotient turns out to be -2^{n-1}. So at this stage the algorithm cannot decide whether there is an overflow or not based on the quotient bit; instead, it proceeds to calculate the remaining quotient bits, retaining the information about potential overflow in the control flow.

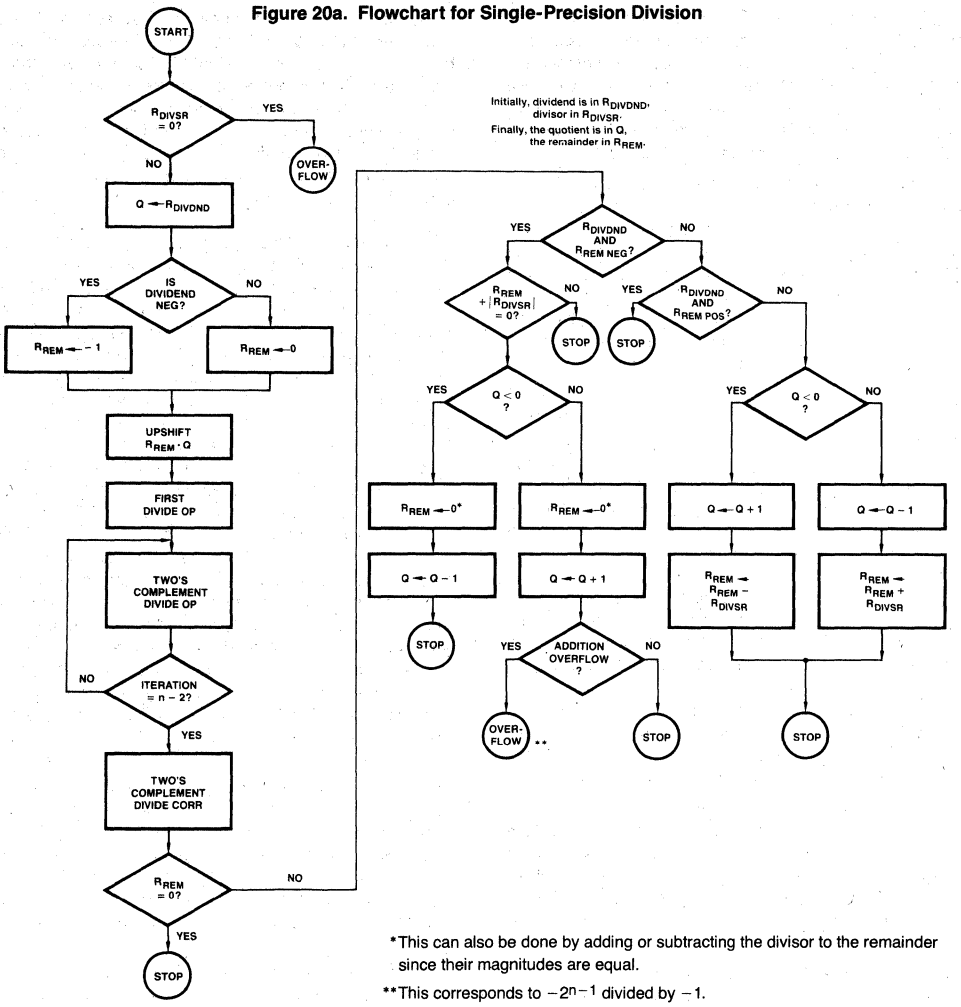
After the last divide step (which performs "divide correction"), the algorithm again tests the state of the external flip-flop, "storing" it in the control flow. This last state of the divide flip-flop would be lost without the external flip-flop, since the quotient bit shifted in is always a 1 in this case. The two's complement divide op is used instead of the divide correction so as to have access to the sign compare on the SIO_3 line. (The state of the external flip-flop after this cycle determines whether the correction requires incrementing or decrementing of the quotient). Note that the remainder now needs to be shifted down by one bit; this is done concurrently with the testing of the external flip-flop, and the microcode also updates the Z bit of the status register. In the next cycle, the Z bit is tested and the algorithm terminates if it is set. This is followed by a test for negative remainder and dividend. If the test fails, a branch is taken to the test for positive dividend and remainder. Concurrently, the remainder is added to the divisor with $\overline{IEN}$ high and the Z flag again updated. This is the first part of the test for the absolute value of the remainder being equal to the divisor. In the next cycle, the Z flag is tested; if it is set, a branch is taken to the correction step. Again, in the same cycle, the divisor is subtracted from the remainder with $\overline{IEN}$ high to complete the magnitude test.

In the following cycle, the Z flag is tested as before. If it is not set, the algorithm terminates. The test for positive dividend and remainder computes the OR of the remainder and initial dividend with $\overline{IEN}$ high, and updates the N flag of the status register. In the next cycle the algorithm tests the N flag and exits if it is low, indicating that the dividend and remainder signs agreed. Otherwise, the correction steps are executed.

The algorithm has been written for fastest execution, not shortest possible microcode. The technique of using the control flow to "remember" states of flags leads to duplication of code but saves cycles on testing flags and branching. At the end of the algorithm, there are two places where the quotient is incremented. One of these sequences corresponds to the "normal" case (quotient bit n agreed with quotient sign). This microcycle produces an overflow when the quotient is 2^{n-1}. The other sequence where the quotient is incremented corresponds to the case where the n^{th} bit of quotient disagreed with the quotient sign. This case is an overflow unless the quotient is -2^{n-1}; however, then an overflow is produced by the correction, when $2^{n-1}-1$ is incremented. Hence, in this case, if the correction does *not* produce an overflow, then there *is* an overflow.

5

Figure 20a. Flowchart for Single-Precision Division



*This can also be done by adding or subtracting the divisor to the remainder since their magnitudes are equal.

**This corresponds to -2^{n-1} divided by -1.

Figure 20b. Single-Precision Divide Microcode

	1. Y ← R_{DIVSR}, UPDATE Z FLAG;	Test for divisor = 0
	2. IF Z GOTO OVERFLOW, Q ← R_{DIVDND}, UPDATE N;	Test quotient sign for sign extension
	3. IF NOT N GOTO UPSH, R_{REM} ← 0;	zero extend into R_{REM}
	4. R_{REM} ← −1;	One extend if negative
UPSH:	5. UPSHIFT R_{REM}.Q;	Logic upshift R_{REM} and Q, zero fill
	6. FOR (n−3), FIRST DIVIDE OP (R_{REM}, R_{DIVSR});	Loop setup: load 2910 counter and push PC
	7. ENDFOR, TWO'S COMPLEMENT DIVIDE OP (R_{REM}, R_{DIVSR});	R_{REM} on B address; repeat n−2 times
	8. DIVIDE "CORRECTION" OP (R_{REM}, R_{DIVSR});	Shift in '1' into $Q0_0$ of LSS
	9. Y ← R_{REM}, UPDATE Z, V;	Test remainder for zero
	10. IF Z GOTO DONE, Y ← R_{REM} AND R_{DIVDND}, UPDATE N;	Done if remainder = 0, check for dividend
	11. IF NOT N GOTO NORMCHK, Y ← R_{DIVSR} − R_{REM}, UPDATE Z;	and remainder being negative
	12. IF Z GOTO EQMAG, Y ← R_{DIVSR} + R_{REM}, UPDATE Z;	First half of magnitude check
	13. IF Z GOTO EQMAGNXT, Y ← Q, UPDATE N;	Other half of magnitude check
DONE:	14. IF NOT V RETURN, R_{QUOT} ← Q;	If magnitude equal, then go test
	15. GOTO OVERFLOW;	sign of Q else return
NORMCHK:	16. Y ← R_{REM} OR R_{DIVDND}, UPDATE N;	Check if remainder and dividend positive
	17. IF NOT N GOTO DONE, Y ← Q, UPDATE N;	If yes, exit
	18. IF N GOTO ADDONE;	Increment negative quotients
SUBONE:	19. R_{REM} ← R_{REM} + R_{DIVSR};	This can never overflow since Q is odd
	20. Q ← Q − 1, UPDATE V, GOTO DONE;	
EQMAG:	21. Y ← Q, UPDATE N;	Decrement negative quotients
EQMAGNXT:	22. IF N GOTO SUBONE;	This could overflow for positive Q
ADDONE:	23. R_{REM} ← R_{REM} − R_{DIVSR};	
	24. Q ← Q + 1, UPDATE V, GOTO DONE;	
OVERFLOW:	25. (. . . . OVERFLOW MICROCODE)	

Note: Where Y is specified as destination, use $\overline{IEN}$ = HIGH.

Figure 21. Examples of Single-Precision Signed Divide

Operation	Before Correction		After Correction		Comments
	Q	REM	Q	REM	
12 ÷ 5	3	−3	2	2	Normal correction: decrement positive quotients, increment negative quotients
12 ÷ −5	−3	−3	−2	2	
−12 ÷ 5	−3	3	−2	−2	
−12 ÷ −5	3	3	2	−2	
12 ÷ 4	3	0	3	0	No correction necessary: zero remainder
12 ÷ −4	−3	0	−3	0	
−12 ÷ 4	−3	0	−3	0	
−12 ÷ −4	3	0	3	0	
12 ÷ 3	5	−3	4	0	Normal correction
12 ÷ −3	−5	−3	−4	0	
−12 ÷ 3	−3	−3	−4	0	Special case: increment positive quotients
−12 ÷ −3	3	−3	4	0	
−32768 ÷ −1	32767	−1	−32768	0	Overflow!
−32768 ÷ 1	−32767	−1	−32768	0	Special case

Figure 22. Double Length Normalize/First Divide Operation

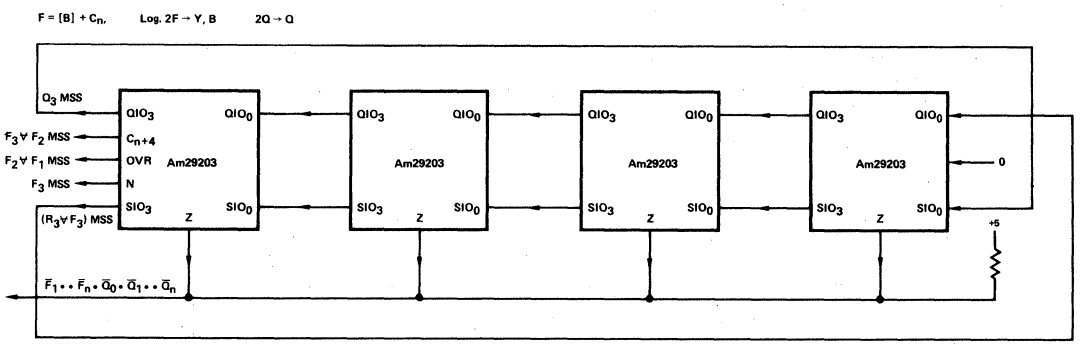


Figure 23. Two's Complement Divide

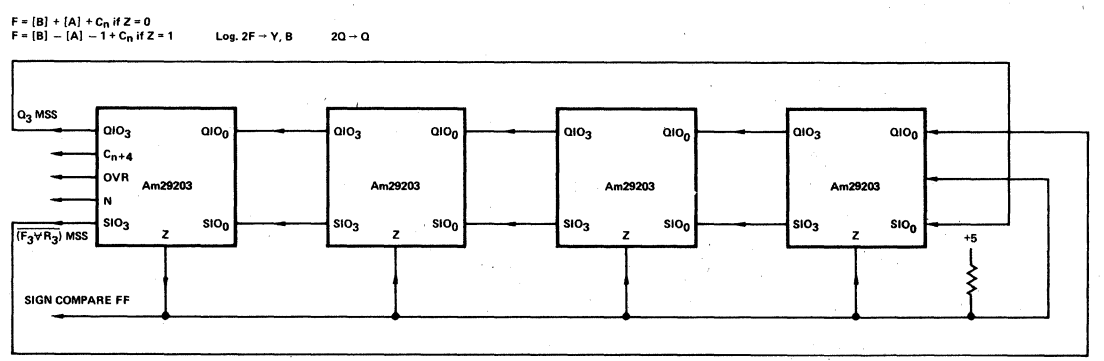


Figure 24. Two's Complement Divide Correction

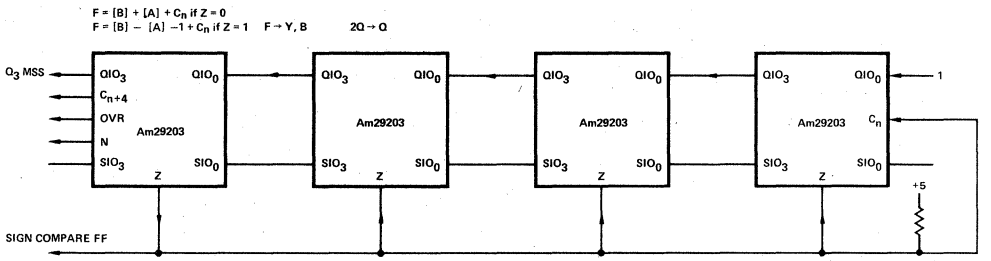


Figure 25. Double-Precision Signed Division Microcode

```
                1. Q ← R_DIVDNDLSH;                          Initialize Q register
                2. R_REM ← R_DIVDNDMSH;                      Initialize remainder register R_REM
                3. DIVIDE FIRST OP (R_REM, R_DIVSR), UPDATE N;   Find quotient sign, setup external quotient flip-flop (EXTQFF)
                4. IF EXTQFF GOTO NEGQUOT, DOWNSH R_REM • Q WITH N FILL;   Branch on quotient sign; restore dividend by downshift
                5. TWO'S COMPLEMENT DIVIDE OP (R_REM, R_DIVSR);   Compute bit n+1 of quotient
                6. IF EXTQFF GOTO OVERFLOW, TWO'S COMPLEMENT DIVIDE OP (R_REM, R_DIVSR);   Error if different from sign; compute bit n of quotient
                7. IF EXTQFF GOTO POSSBLOVF, TWO'S COMPLEMENT DIVIDE OP (R_REM, R_DIVSR);   Possible overflow if different from sign
LOOP:           8. FOR (n−5), TWO'S COMPLEMENT DIVIDE OP (R_REM, R_DIVSR);   Setup iteration count
                9. ENDFOR, TWO'S COMPLEMENT DIVIDE OP (R_REM, R_DIVSR);   Iterate divide step
               10. TWO'S COMPLEMENT DIVIDE OP (R_REM, R_DIVSR), UPDATE N, QIO0 ← 1;   Divide last step: quotient bit is always a '1'; setup EXTQFF
               11. IF EXTQFF GOTO SUB, R_REM ← DOWNSH R_REM, SIO3 ← N, UPDATE Z;   Last state of EXTQFF decides direction of connection
               12. IF Z GOTO DONE, Y ← R_REM AND R_DIVDNDMSH, UPDATE Z, V;   Exit if remainder zero; test for negative remainder and dividend
               13. IF NOT N GOTO NORMCHK1, Y ← R_REM + R_DIVSR, UPDATE Z;   If test failed, go check for positive remainder and dividend
               14. IF Z GOTO CORRECT1, Y ← R_REM − R_DIVSR, UPDATE Z;   For negative remainder and dividend, check remainder magnitude
               15. IF Z GOTO CORRECT1;                       If remainder magnitude = divisor magnitude, connect quotient
DONE:          16. IF NOT V RETURN, R_QUOT ← Q;              Else if no overflow return
               17. GOTO OVERFLOW;                            Else overflow;
NORMCHK1:      18. Y ← R_REM OR R_DIVDNDMSH, UPDATE N, V;    Check for positive dividend and remainder
               19. IF NOT N GOTO DONE;                       If test passed, done
CORRECT1:      20. R_REM ← R_REM + R_DIVSR;                  Else correct remainder
               21. Q ← Q − 1, GOTO DONE;                     Correct quotient, and exit
SUB:           22. IF Z GOTO DONE, Y ← R_REM AND R_DIVDNDMSH, UPDATE Z, V;
               23. IF NOT N GOTO NORMCHK2, Y ← R_REM + R_DIVSR, UPDATE Z;
               24. IF Z GOTO CORRECT2, Y ← R_REM − R_DIVSR, UPDATE Z;
               25. IF Z GOTO CORRECT2;                       This part of the algorithm repeats the correction code for the
               26. GOTO DONE;                                  case where the last value of the EXTQFF was a high,
NORMCHK2:      27. Y ← R_REM OR R_DIVDNDMSH, UPDATE N, V;      indicating correction in the opposite direction.
               28. IF NOT N GOTO DONE;
CORRECT2       29. R_REM ← R_REM − R_DIVSR;                  Executed instead of 5, 6, 7 when the quotient is negative
               30. Q ← Q + 1, UPDATE V;
               31. GOTO DONE;
NEGQUOT:       32. TWO'S COMPLEMENT DIVIDE OP (R_REM, R_DIVSR);   This is executed when the n^th quotient bit differs from the
               33. IF NOT EXTQFF GOTO OVERFLOW, TWO'S COMPLEMENT DIVIDE OP (R_REM, R_DIVSR);      quotient sign. The division is completed to check whether
               34. IF EXTQFF GOTO LOOP, TWO'S COMPLEMENT DIVIDE OP (R_REM, R_DIVSR);              the quotient is −2^(n−1)
POSSBLOVF:     35. FOR (n−5), TWO'S COMPLEMENT DIVIDE OP (R_REM, R_DIVSR);
               36. ENDFOR, TWO'S COMPLEMENT DIVIDE OP (R_REM, R_DIVSR);   This is signalled by an overflow in the
               37. TWO'S COMPLEMENT DIVIDE OP (R_REM, R_DIVSR), UPDATE N, QIO0 ← 1;      correction step. Otherwise, there has been a division overflow.
               38. IF NOT EXTQFF GOTO OVERFLOW, R_REM ← 0;
               39. Q ← Q + 1, UPDATE V;
               40. IF V GOTO DONE;
               41. GOTO OVERFLOW;
```

BYTE SWAP

The multi-port architecture of the Am2903 allows for easy implementation of high- and low-order byte swapping. Figure 26 outlines a byte swap implementation utilizing two data ports. Initially, the lower order 8-bit byte is stored in devices 1 and 2, while the high-order byte is in devices 3 and 4. When the user wishes to exchange the two bytes, the register location of the desired word is placed on the B address port. When the byte swap line is brought LOW, the bytes to be swapped will be flowing from the DB ports of the Am2903 through the Am2958/2959 Three-state Buffers. The outputs of the three-state buffers are permuted such that the byte swap is achieved.

The resultant permuted data is presented to the DA ports of the Am2903 where it is re-loaded into the memories of the Am2903 on the next positive edge of CP using the source and function commands of F = A plus C_n (C_n = 0) for the Am2958 or F = A plus C_n (C_n = 0) for the Am2959 and the destination command F Y, B.

A higher speed technique for achieving the byte swap operation is illustrated in Figure 27. Instead of inputting the permuted data via the DA ports, the permuted data is entered via the Y input/output ports with $\overline{OE_Y}$ held HIGH. This technique bypasses the ALU, thus allowing faster operation. The Am2903 destination command F → Y, B should be used.

Figure 26. Byte Swap.

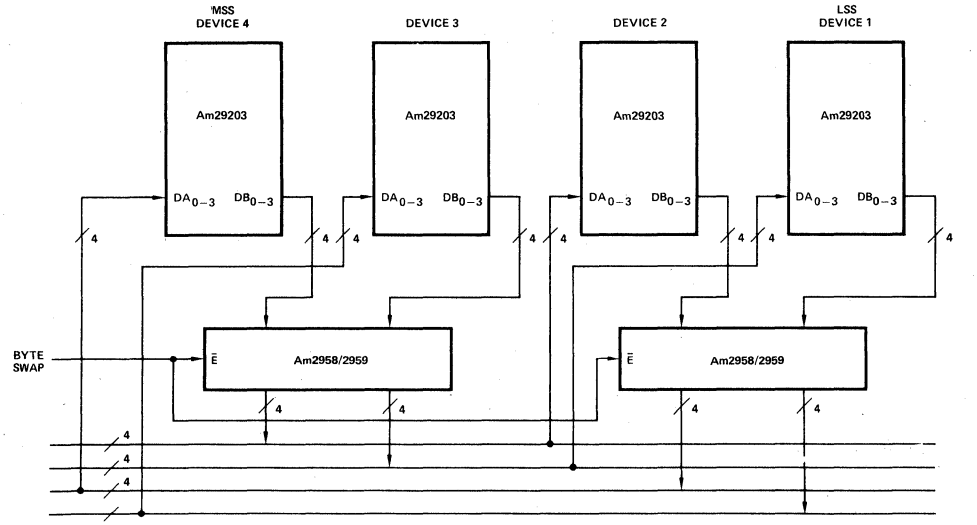
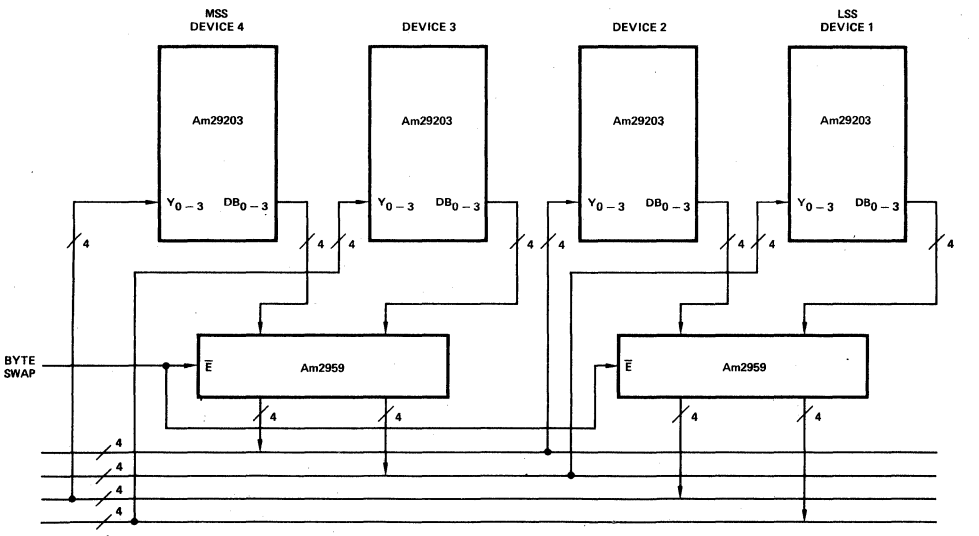


Figure 27. High Speed Byte Swap.



BCD OPERATIONS WITH THE Am29203

BCD FUNCTIONS

Binary Coded Decimal (BCD) numbers are a means to represent decimal numbers in binary form such that each digit is represented by four bits of its equivalent binary value. They are useful in applications where there is a considerable amount of interaction with the decimal number representation. The value of the four binary bits corresponding to each BCD digit does not exceed nine.

As part of the special instruction set, the Am29203 can convert numbers between binary and BCD representations. It also performs basic arithmetic operations on BCD numbers.

BINARY TO BCD CONVERSION

This instruction, when executed several times, allows conversion from binary to BCD numbers. Using the same number of bits, the binary representation of numbers has a larger range of values than a BCD representation. Hence, care must be taken to see that the value of the binary number does not exceed the BCD range before using this instruction. Multiprecision representations where the width of the BCD number is larger than the width of the system, allows a larger range on numbers. The binary number may be stored as multiprecision as well. Usually multiprecision representations are integer multiples of the width of the system.

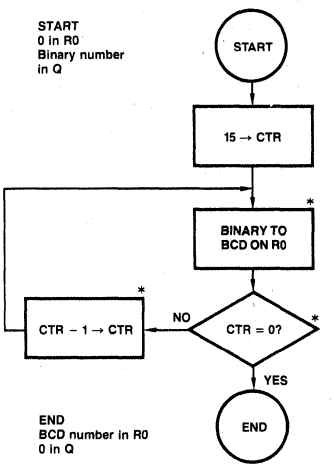
Figure 28 shows a flow chart for a single precision conversion in a 16-bit wide system. It involves executing the Binary to BCD conversion instruction 16 times.

In case of single-precision, this instruction requires that the binary number be present in the Q register and uses one of the RAM registers for storing the BCD number during and after the conversion. The RAM register is cleared before use. Each instruction is composed of two steps. The first step adds a binary value of three to each BCD digit which is five or greater as a preadjustment for a shift which follows. This addition is performed independently over each slice and the carry bits from each slice are ignored. The second step shifts up the Q register and the RAM register with the interconnections as in Figure 29, for a 16-bit system. The Am29203 executes both the steps in one microcycle. The number of shifts have to be a multiple of four to obtain a meaningful result.

The Am29203 also has another special instruction to facilitate multiprecision Binary to BCD conversions. This instruction referred to as "Multiprecision Binary to BCD Conversion" does the same action as the "Binary to BCD Conversion" except for the shifting of the Q register.

The flow chart for the simplest double precision Binary to BCD conversion algorithm in a 16-bit system is shown in Figure 30. Initially the Q register stores the most significant half of the binary number. Two registers R0 and R1, which are both cleared initially, are used for storing the most significant and least significant half of the BCD number after conversion respectively. The shift for each binary bit requires two microcycles. The Binary to BCD conversion instruction is executed first of R1 and the most significant bit from R1 that is shifted out is stored as the Mc or carry bit of the Am2904. The shift linkages for this step are shown in Figure 31. Next the Multiprecision Binary to BCD conversion instruction is executed so that R0 is also adjusted and the Mc or carry bit is shifted in. These two instructions together account for one equivalent shift of the double precision number as a whole. After 16 such shifts, the Q register is loaded with the least significant half of the binary number and the same operations are performed again 16 times. Once the single precision binary number is converted to a double precision BCD number, then the algorithm can be terminated after 16 shifts of the binary number.

Figure 28. Binary to BCD Conversion – Single Precision



* – Operations occur in same cycle in microcode.

Figure 29. Binary to BCD Conversion

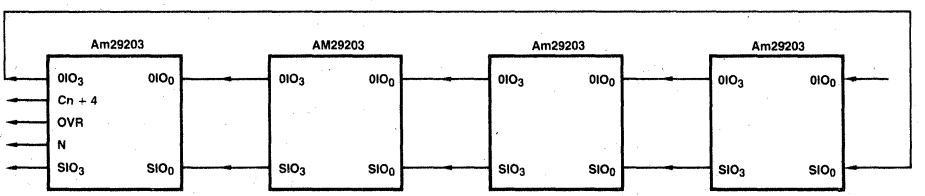
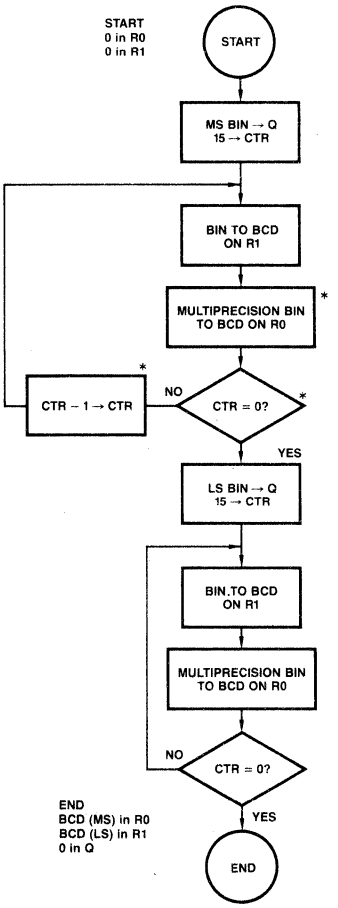


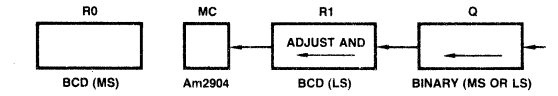
Figure 30. Double Precision 16-Bit Binary to BCD Conversion



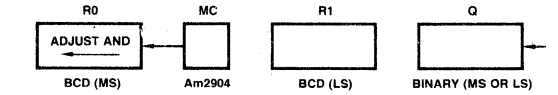
* – Operations occur in same cycle in microcode.

Figure 31. Shift Linkages During Double Precision Binary to BCD Conversion

a) Binary to BCD on R1



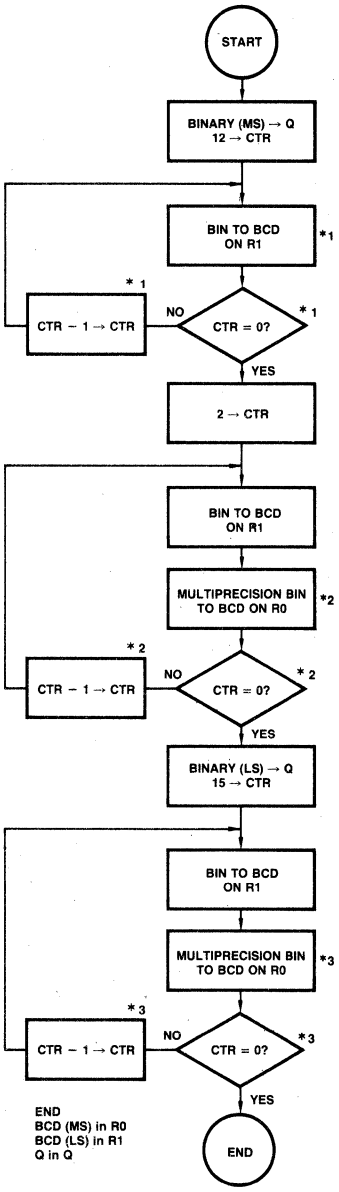
b) Multiprecision Binary to BCD on R0



The above algorithm can be made more efficient by noting that the shifting of R0 is not necessary for the first few cycles.

This is because mostly zeros are shifted into the already cleared register for the most part of the first 16 shifts of the double precision number. The flow chart for implementing this on double precision representations in a 16-bit system is shown in Figure 32. The most significant half of the binary number is first loaded in the Q register. For the first 13 cycles it is sufficient to shift only the

Figure 32. 16-Bit Double Precision Binary to BCD Conversion



* – Operations occur in same cycle in microcode.

5

R1 register during conversion. After this both R0 and R1 have to be shifted as cascaded registers. This is because the value of the largest unsigned 16-bit binary number is 65535 and thus requires 19 bits for representing in BCD. As a result, a non-zero bit may be shifted out of R1 after 13 shifts and it is necessary to start shifting R0 as well after this. After the first 16 shifts on the Q register, the least significant binary number is loaded in Q and 16 more double precision shifts are done. The shift-linkages while shifting R0 and R1 are same as the previous case and are shown in Figure 31.

BCD TO BINARY CONVERSIONS

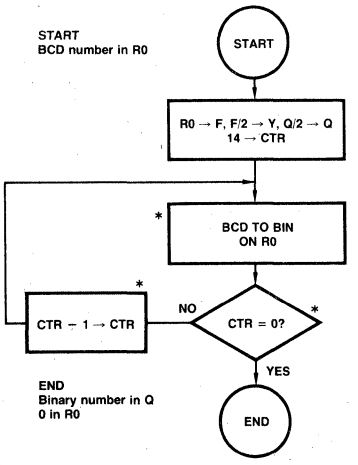
The BCD to Binary conversion instruction essentially reverses the steps of the Binary to BCD instruction described earlier. The BCD number is initially present in one of the RAM registers and the Q register is used during the conversion to store the binary equivalent. The BCD to Binary conversion algorithm requires that the BCD number first be shifted one bit down and then an adjustment done on the BCD digits, which subtracts three from each BCD digit which is eight or greater. However, since the Am29203 has its shifter after the ALU section, the BCD to Binary conversion instruction first performs the adjustment for a previous shift and then performs the shift in preparation for the next instruction. A flow chart for this conversion is shown in Figure 33. The BCD number in R0 is first shifted down one bit to load its least significant bit into the most significant bit of the Q register. After this, the BCD to Binary conversion instruction is executed 15 times to perform the necessary adjustments and shifts successively. The interconnections are shown in Figure 34. Thus, 16 shifts and 15 adjustments are performed on the 16-bit number. The adjustment on the final shift is not required as the binary number is fully formed anyway and the BCD number is zero at this stage.

As in the case of the Binary to BCD conversion instruction, it may be noted that the adjustment is done independently over each slice and the carry bits play no role in this adjustment.

The scheme for converting multiprecision BCD numbers to binary is similar to the one outlined in the Binary to BCD conversion section. The simplest, but not the most efficient scheme, uses the flow chart shown in Figure 35 for a double precision number in a 16-bit system. The shift linkages are shown in Figure 36. Initially, the most significant half of the BCD number is stored in R0 and the least significant half is in R1. The Q register is used for storing a part of the binary equivalent during and after the conversion. The BCD number as a whole has to be first shifted down one bit. First R0 is downshifted with the linkages shown in Figure 36a so that its least significant bit is collected in the Mc or carry flip-flop of the Am2904. Then R1 and Q are shifted down as shown in Figure 36b so that Mc is loaded in the MSB of R1. The next two instructions perform the adjustment on this shift and also downshift the adjusted numbers by one bit in preparation for the next adjust and shift. The Multiprecision BCD to Binary conversion instruction is executed on R0 so as to adjust and downshift R0 and its LSB is stored in Mc as shown in Figure 36c. The BCD to Binary conversion instruction following this adjusts R1 and downshifts R1 and Q with Mc being loaded into the MSB of R1 as shown in Figure 36d. These two instructions are performed 15 times in a loop. As a result, R0 and Q get shifted 16 times including the initial shift. Since the contents of R0 are now zeros, it is no longer necessary to shift it further. The Q register contains the least significant half of the binary result which is transferred to R2. After this the BCD to Binary conversion is performed on R1, 16 times with the linkages shown in Figure 36e, so that a zero is input in the MSB of R1. The most significant half of the binary number is available in the Q register at the end of the operation. The double precision BCD to Binary Conversion Algorithm can be made more efficient for certain statistical distribution of numbers. This is possible when it is recognized that the most significant half of the BCD number is equal to zero in the beginning and only a single precision conversion is required on the least significant half. Also when the contents of R0, which initially contains the most significant half of the BCD number, become zero before the first 16 cycles, it is no longer necessary to perform a shifting on it.

One such algorithm is outlined in Figure 37. The initial and final contents of the registers are the same as in Figure 35. Initially, it is tested to see if R0 is equal to zero. If it is, then a single precision conversion is performed on R1 so that the least significant half of the binary equivalent is available in the Q register. This is then transferred to R2 and Q is loaded with a zero. If R0 is not zero, then it is downshifted into Mc as shown in Figure 36a, and the status is loaded in this step to see if the shifted number had reached zero. R1 cascaded with Q is then downshifted into MC as shown in Figure 36b, and the status is not loaded in this step so

Figure 33. BCD to Binary Conversion – Single Precision



* – Operations occur in the same cycle in microcode.

Figure 34. BCD to Binary Conversion

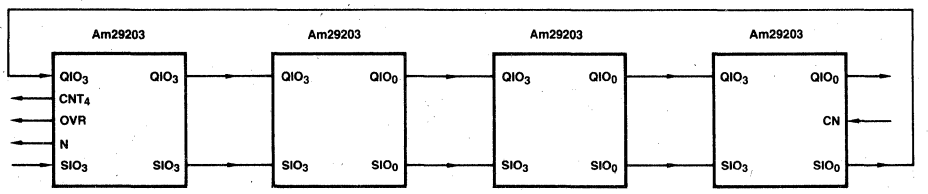
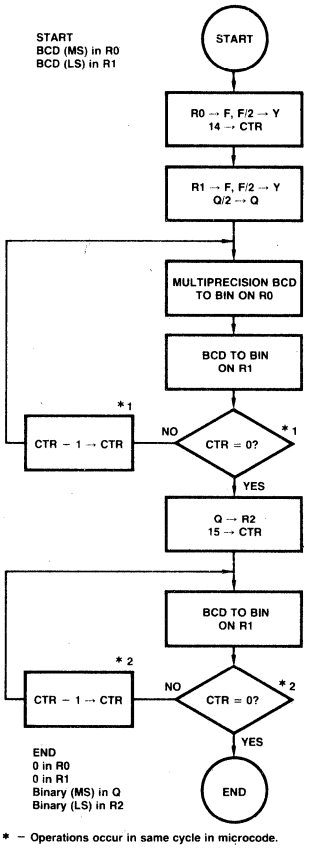
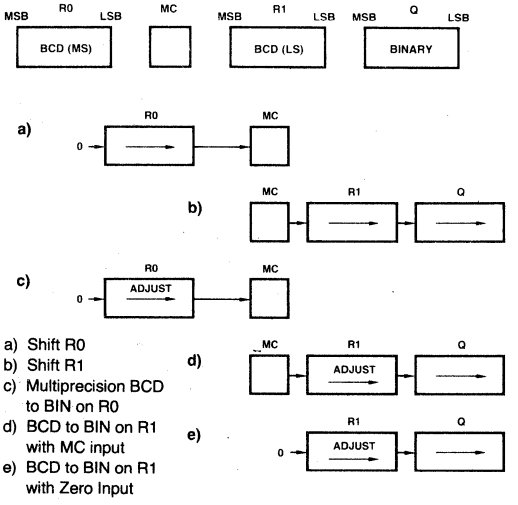


Figure 35. Simple 16-Bit Double Precision BCD to Binary Conversion



* − Operations occur in same cycle in microcode.

Figure 36. Shift Linkages for Double-Precision BCD to Binary Conversion



a) Shift R0
b) Shift R1
c) Multiprecision BCD to BIN on R0
d) BCD to BIN on R1 with MC input
e) BCD to BIN on R1 with Zero Input

that the previously set status can be used for a conditional branch later on while executing a loop. The Multiprecision BCD to binary conversion is performed on R0 and a simultaneous branch is taken if the previously loaded status indicated R0 to be zero. If R0 is non-zero then the algorithm does a double precision conversion on R0 and R1 15 times. The status is set while shifting R0 and is left unchanged while shifting R1 so that a branch can be taken when R0 becomes zero. If it does, the conversion is performed on R1 alone for the remaining cycles. After the first 16 shifts on R1 it may be necessary to unload the Q register in to R2 before completing the last 16 cycles of conversion. This algorithm trades off the number of lines of microcode for a statistically faster conversion. This happens whenever small numbers are being dealt with more frequently in a system where multiprecision numbers may also be required less often. The advantage increases with wider systems.

DIVIDE BY TWO ADJUST

This instruction is useful in dividing BCD numbers by two. It should be used after an instruction which shifts the number down by one bit. The instruction essentially performs a correction on the downshifted number to obtain a valid BCD representation again. The correction performed is identical to the BCD to Binary conversion instruction, but no shifting is done.

DECREMENT BY ONE OR TWO

This function available in the Am29203 does not require the storing of commonly used constants such as one or two in the RAM registers or memory. The instruction decrements by one when Cn is high and by two when Cn is low. The instruction is also useful for addressing byte addressable memories in a 16-bit wide system.

BCD ADD AND SUBTRACT

The Am29203 provides instructions to add or subtract two BCD numbers in one microcycle. There are two subtract instructions whereby the R and S operands can be subtracted from each other. When the BCD addition or subtraction is performed on BCD numbers the result is a valid BCD number. The result is undefined if either of the operands is an invalid BCD representation, so considered when any of the groups of four bits over a slice has a value greater than nine.

The Carry, Propagate and Generate signals have a different significance in BCD arithmetic as compared to binary arithmetic. During addition, the Carry output from a slice indicates that the result of the addition was greater than nine over the slice and that a one should be added to the next BCD digit. In order to speed up the addition process, the Look-Ahead Carry Generator, Am2902, can still be used as before. In case of BCD additions, Propagate signifies that the result equals nine and if there is a carry input to the slice then the carry will have to be propagated out of the slice. The Generate signal while performing additions signifies that the result is already greater than nine and a carry output needs to be generated whether or not the carry input exists. The state of the Propagate signal for results greater than nine does not matter because the Generate signal produces a carry output anyway. In case of subtract operations, the Carry output may be interpreted as a "borrow". Borrowing is necessary in BCD arithmetic when the digit to be subtracted is larger than the digit it is subtracted from. If both the digits are equal then a borrow from a higher digit is not necessary unless the previous digit borrows too. This is equivalent to a propagation of the borrow signal and is indicated on the Propagation line. Whenever borrowing is necessary, irrespective of the previous digit, then the Generate signal is active.

Generate overrides the Propagate and whenever Generate is active and the state of the Propagate does not matter. The Carry output signal, Cn + 4, goes low whenever a borrowing is done from a higher order digit.

BCD MULTIPLICATION AND DIVISION

Most general purpose machines do not have hardwired combinatorial logic to perform multiplication and division because of cost trade-offs. In most applications the multiplications are performed at least one order of magnitude or more less lower case often than adds, division being at least another order of magnitude again. Therefore, the small frequency of use and high hardware cost of combinatorial methods justify implementing divide and multiply with microcode algorithms. Algorithms for BCD multiply and divide parallel some of the more classical binary methods with little change. These algorithms are built of simple operation, such as shift, add, and subtract which the Am29203 provides in both binary and BCD.

MULTIPLY

In its most simple form, multiplication can be performed by repeatedly adding the multiplicand to itself as numbered in the multiplier. This method however is very costly in CPU cycles. With a slight modification in concept the computation time can be reduced significantly.

An improved method starts by zeroing the accumulator and adding to it the multiplicand as many times as numbered by the least significant digit (LSD) of the multiplier. The multiplicand is then multiplied by ten (a shift of 4 bits left) and added to the accumulator as numbered by the next least significant digit of the multiplier. The algorithm iterates until the most significant digit of the multiplier is used. This method achieves an improvement ratio of approximately $10^n - 1/n \times 9$ (where n is the number of digits in the multiplier).

The previous method can be further improved by precomputing and holding the nine multiples of the multiplicand in a register file. The correct multiple can be selected by routing the multiplier digit onto the register file address bus. Multiply by ten of the multiplicand can be performed by adding it to a shifted accumulator rather than shifting the multiplicand. The improvement ratio over the previous method is approximately $n \times 9/n + 10$ (where n is *related* to the number of digits in the multiplier).

MULTIPLICATION HARDWARE IMPLEMENTATION

The preceding paragraphs have discussed the theoretical algorithm and hardware for BCD multiplication. Figure 37 shows a particular implementation of hardware using the Am29203 which will do ten's complement BCD multiplication using the last method discussed.

The purpose of the hardware around the Am29203 can best be described by grouping it into three sections. In the lower left corner is the logic which detects overflow conditions during BCD adds and subtracts. The buffers over the MSD (Most Significant Device) are used for sign fill during BCD shift. When a BCD shift is being performed the BCD number is brought out on the DB bus and passed to the next lower digit via the DA port and then passed through the ALU into the RAM. However, on the MSD the sign digit is wrapped around from DB_{MSD} to DA_{MSD}. The final group of logic is the register A which holds a link digit in order to implement multiprecision BCD shifts. Register A also serves to hold the LSD (Least Significant Digit) of the multiplier so it can be presented to the A address bus.

Figure 38 shows a flow chart of the ten's complement multiply microcode.

The top box in the chart contains instructions to clear the accumulator and generate the multiples of the multiplicand. It takes eleven cycles to execute. The next box initializes the counter in the sequencer to one less than the desired number of iterations. It also loads the LSD of the multiplier into register A.

The main part of the multiplication code is the inner loop. Register A selects which multiple of the multiplicand will be added to the partial product in the accumulator. The next two instructions perform a BCD shift of the accumulator (R12, R13) with sign fill. The last instruction BCD-shifts the multiplier, loads link register A with the LSD, while checking the loop counter. The loop is executed seven times.

The last group of instructions performs an adjust according to the sign digit which is now in the LSD and register A. In radix complement forms of numbers (such as ten's complement), the

Figure 37. Ten's Complement BCD Multiplication Implementation

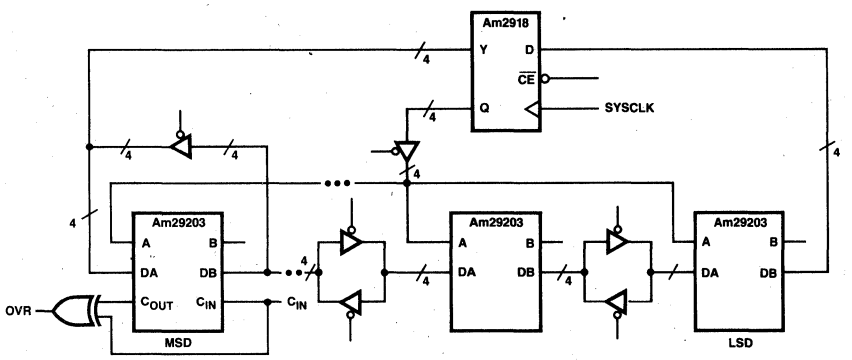
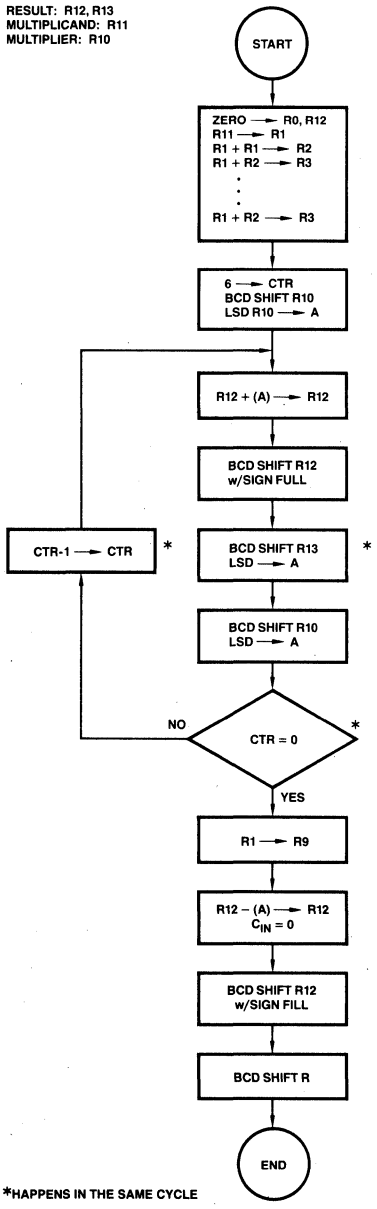


Figure 38. Ten's Complement BCD Multiplication



sign digit has a numeric weight of $-1 \times r^n$ where r is the radix and n is the number of digits including the sign. Therefore, register A is used to select 0 or the multiplier and subtract it from the multiplicand.

In this multiply algorithm there is a buffer digit between the sign digit and the digit with the first significant data. The buffer digit prevents an overflow from happening during the addition in the multiply loop. This condition could be ignored if overflow was detected after addition and a routine were conditionally called to handle the case. The overflow condition can be corrected by subtracting one from the sign digit after the BCD shift. The buffer digit can also be avoided by converting the numbers to positive sign magnitude numbers, multiplying them, and then adjusting the result according to the product of original signs of multiplier and multiplicand. The final option is to use the hardware shown in Figure 39. This hardware, during shift, shifts in the sign, if it was an overflow a 1 is subtracted from the sign.

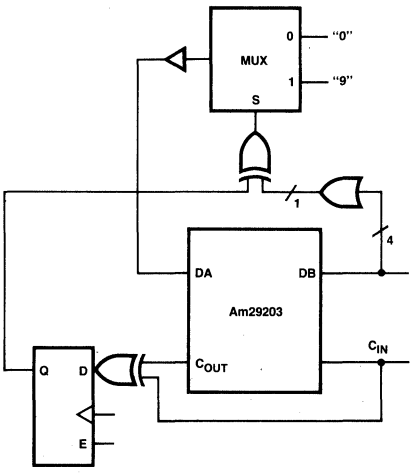
DIVISION IN BCD

As pointed out previously, the algorithms for binary can be applied to BCD. BCD division can be accomplished with repeated subtractions of the divisor from the dividend and keeping count. This method can be very costly if the dividend is big and the divisor very small. However, it helps to explain the method below which called a restoring radix ten division.

Without loss of generality, it will be assumed that both the dividend and the divisor are fractions, as well as the generated quotient. Also assumed is that the dividend and divisor are normalized (which implies keeping track of exponents implicitly or explicitly) and that both are positive.

The restoring division algorithm starts by subtracting the divisor from the dividend until a negative partial dividend is created. The divisor is then added back to the partial dividend to restore to a positive partial dividend. A count is kept of how many divisors went into the dividend before there was a negative dividend. This count is the most significant digit of the quotient. The partial dividend is then shifted up one digit (multiply by radix ten). The procedure of subtracting the divisor and counting is repeated for each digit in the quotient. This method is

Figure 39. Buffer Digit Correction Logic



similar to the scheme which is taught in grade school where trial divisors are tested and finally subtracted from the dividend. After each division the trial divisor is moved over one column.

On the average the restoring algorithm must perform five subtracts and one addition for each digit in the quotient. The addition may be eliminated by performing a non-restoring algorithm. This makes approximately 20% improvement in execution time.

The non-restoring division algorithm proceeds like the restoring algorithm until the negative partial dividend at which point the dividend is shifted up one BCD digit without restoring. The count which was kept is placed into the most significant digit of the quotient. The counter is then set to 9 and is decremented each time the divisor is added to the dividend. The adding and decrementing is continued until the partial dividend is positive. The contents of the counter is then placed in the second most significant digit of the quotient and the partial dividend is shifted up on BCD digit. At this point the algorithm is started over with the subtracting and counting.

HARDWARE IMPLEMENTATION OF DIVISION

Of the shift and subtract class of algorithms discussed above, non-restoring was the best because it eliminated the restoration step. A further improvement can be made on the algorithm. Instead of repeatedly subtracting the divisor from the dividend, binary weighted multiples may be subtracted in a successive approximation sequence.

The algorithm starts by subtracting eight times the divisor from the dividend, then four times the divisor, two times divisor, and finally the divisor. Each time a multiple is subtracted, the sign of the result is inspected. If the sign does not change, then a one is placed in the corresponding bit of the quotient digit. For example, if eight times the divisor worked, then a one would be placed in the most significant bit of the quotient digit (2^3). If the sign changes, then a 0 is placed in the corresponding bit position. When the sign changes during operations with the next lower binary weighted multiples, the algorithm continues in a similar fashion but addition is performed rather than subtraction. As long as the result of each addition is negative, 0 is entered into the appropriate quotient digit. The algorithm continues adding whenever the partial dividend is negative and subtracting when it is positive.

Whenever one times the divisor multiple has been added or subtracted from the partial dividend, the partial dividend is shifted up (times ten) by one BCD digit and calculation of the next significant digit of the quotient begins.

Calculation of the next quotient digit starts with subtracting eight times the divisor from the partial dividend if the partial dividend is positive. If the partial dividend is negative, it is an indication that the divisor was subtracted from the partial dividend once too often. A correction must therefore be added to the partial dividend. Since the partial dividend is shifted up by one digit, the correction is performed by adding in ten times the divisor. These steps however, can be combined into one step by adding two times the divisor rather than adding ten times and then subtracting eight times the divisor.

The flow chart in Figure 41 is an implementation of the above algorithm. This implementation assumes that the numbers are positive signed normalized fractions to begin with. It first generates the multiples of the divisor and stores them in the register file. Next, the counter in the sequencer is loaded with two less than the desired number of times through the loop.

The major block of the flow chart that follows, performs the division. This flow chart can be viewed as a state diagram which not only instructs the Am29203 what to perform, but also contains the sign of the dividend as state information. The left hand column represents the states where the dividend is positive and the right hand column is where the dividend is negative. When the dividend is positive, subtractions are performed and when it is negative, additions are performed. Switching between the two columns is performed by checking the carry-out of the MSD. If the dividend is positive and the subtraction results in no carry-out, then the new partial dividend is negative at which point the algorithm flow is switched right to the column. If the dividend is negative and the subtraction results in a carry-out, then the new partial dividend is positive at which point the algorithm flow switches to the left column.

The last box which is a BCD shift left (times ten) of the dividend also shifts in the quotient digit which was assembled in a shift register. During the last shift instruction, the counter can be tested and the algorithm terminated on zero count.

Figure 40 shows the hardware to perform the division. Besides the Am29203, there are two other important groups of logic

Figure 40. BCD Division Implementation

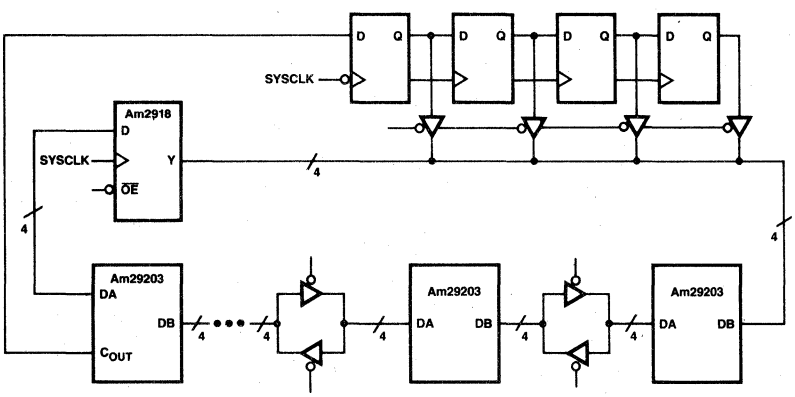
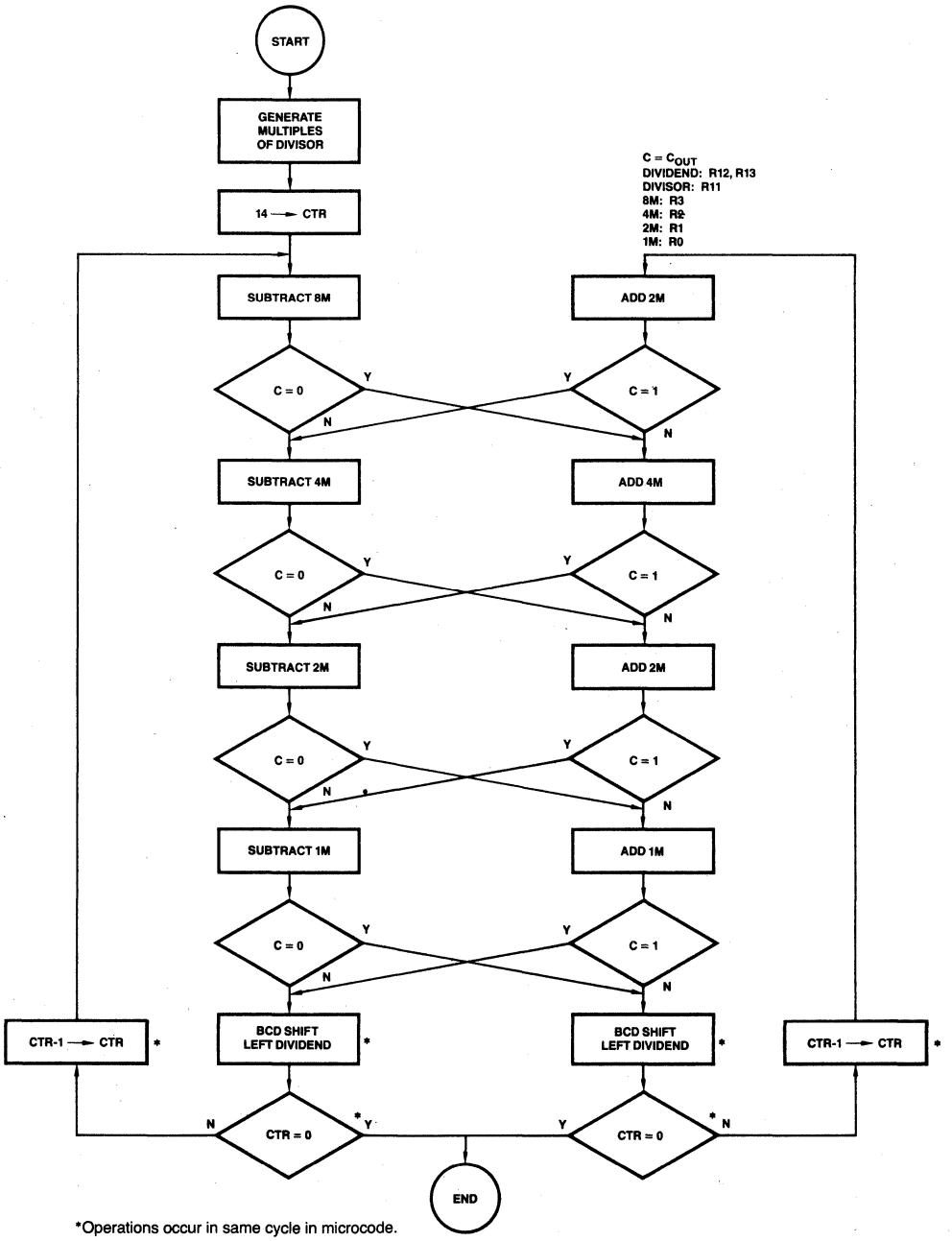


Figure 41. BCD Division



*Operations occur in same cycle in microcode.

shown in the diagram. The carry (sign) is fed into a shift register which assembles each quotient digit. When the dividend is shifted up one digit, the new quotient digit is shifted into the LSD of the least significant half of the dividend as the MSD is shifted into a link register. The link register can then be shifted into the LSD of the most significant half of the dividend.

In a non-pipelined system, the total algorithm takes 5 cycles per quotient digit and 5 cycles to set up. Therefore, 16 digits divided by 8 digits in an 8 digit machine will take 45 cycles to execute.

In a pipelined system the status flags, (such as carry-out) are registered in order to break up long delay paths. This results in shorter microprogram instruction cycle time which is set in accordance with the longest delay path in the machine. A branch based on the carry-out cannot be performed in the same cycle as the arithmetic operation and therefore an extra cycle must be added for each conditional branch. The CTR conditional branch, decrement and BCD shift happens in one cycle because the CTR zero flag is not registered in the Am2910. The algorithm, therefore, takes 85 cycles to execute in a single pipelined system.

The execution time, in a pipelined system, may be substantially decreased by implementing a conditional BCD ADD or SUBTRACT, thereby eliminating the need for a separate conditional branch. In order to achieve such, a multiplexer is placed in the Am29203 instruction path. During normal operation instructions are passed through it from the pipeline register to the Am29203. During BCD DIVISION the multiplexer is used to select between BCD ADD or SUBTRACT based on the registered carry-out of the previous ADD or SUBTRACT.

The resulting algorithm, shown in Figure 42, executes in 5 cycles for each BCD digit. Although it takes just as many cycles as the non-pipelined system, there is a net gain because the pipelined system has a faster cycle time than the non-pipelined system.

WORD/BYTE OPERATIONS

The Am29203 allows for Word/Byte Operations. Figure 45 pictures a 16-bit system which is capable of doing word or byte (lower half of word) operations.

In the Byte mode the BYTE/$\overline{\text{WORD}}$ line is HIGH which in turn asserts a LOW on the $\overline{\text{W}}/\overline{\text{MSS}}$ input of Device 2 making it the MSS device. At the same time the multiplexer selects the status flags of Device 2. The $\overline{\text{IEN}}$ and $\overline{\text{OE}}_Y$ of Devices 4 and 3 are forced HIGH which disables them from writing into RAM or onto the Y bus.

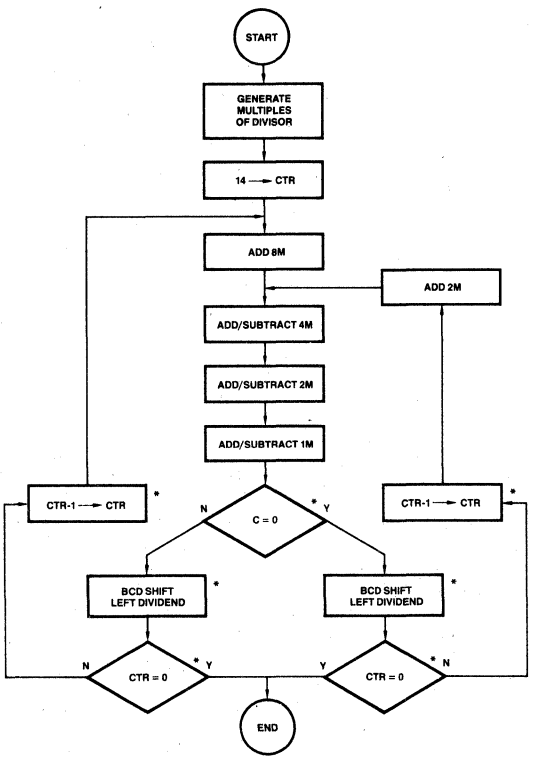
In the word mode Device 4 is the MSS device and the multiplexer selects its status flags. The $\overline{\text{IEN}}$ inputs are brought low which enables writing in to RAM. The $\overline{\text{OE}}_Y$ is also allowed to go low.

MEMORY EXPANSION

The Am29203 allows for a theoretically infinite memory expansion. Figure 44, *Am29203 and Am29707*, pictures a 4-bit slice of a system which has 48 words of RAM and 16 words of ROM. RAM storage is provided by the Am29203 and the Am29707s. The Am29707 RAM is functionally identical to the Am29203 RAM. The Am27S19 is used to store constants and masks and is addressable from address port A only. The system is organized around five data buses. Inter-bus communication may be done through the Am29707 or the Am29203. The memory addressing scheme specifies the data source for the R input of the ALU eminating from the register locations specified by address field A. A_{0-3} addresses 16 memory locations in each chip while address bits A_{4-6} are decoded and used for the output enable for the desired chip. The B address field is used to select the S input of the ALU and the C field is used to specify the register location where the result of the ALU operation is to be stored.

Bits B_{0-3} are for source register addressing in each chip. Bits B_4 and B_5 are used for chip output enable selection. C_{0-3} access the 16 destination addresses on each chip while bits C_4 and C_5 control the Write Enable of the desired chip. The source and destination register address are multiplexed such that when the clock is HIGH, the source register address is presented to the B address ports of the RAMs. The Instruction Enable ($\overline{\text{IEN}}$) is HIGH at this time. The data flows from the Y port or the internal B port as selected by the decoder whose inputs are B_4 and B_5. When the clock goes LOW, the data eminating from the selected Y outputs of the Am29707s and the RAM outputs of the Am29203 are latched and the destination address is now selected for use by the RAM address lines.

Figure 42. BCD Division (Pipelined System Configuration)



When the destination address stabilizes on the address lines, the $\overline{IEN}$ pin is brought LOW. When the $\overline{WRITE}$ output goes LOW as part of a write data instruction execution, address bits C_4 and C_5 of the corresponding decoder are enabled. The selected decoder line will go LOW, allowing the desired memory location to be written into. To switch between two- and three-address architecture, the user simply makes the source and destination addresses the same; i.e., $B_{0-3} = C_{0-3}$ and $B_{4-5} = C_{4-5}$. For two-address architecture, the MUX is removed from the circuit.

The advantage of separating the write signal from the $\overline{IEN}$ signal is that writing can be controlled over less than the full word length. For example, in a 16-bit system, the lower two devices can have one $\overline{IEN}$ signal and the upper two devices a second $\overline{IEN}$ signal. Controlling these two signals separately allows data to be written in either byte without disturbing the other byte. The 2- and 3-address architecture is handled in the same way as with the Am2903.

Figure 43. Statistically Efficient 16-Bit Double Precision BCD to Bin Conversion

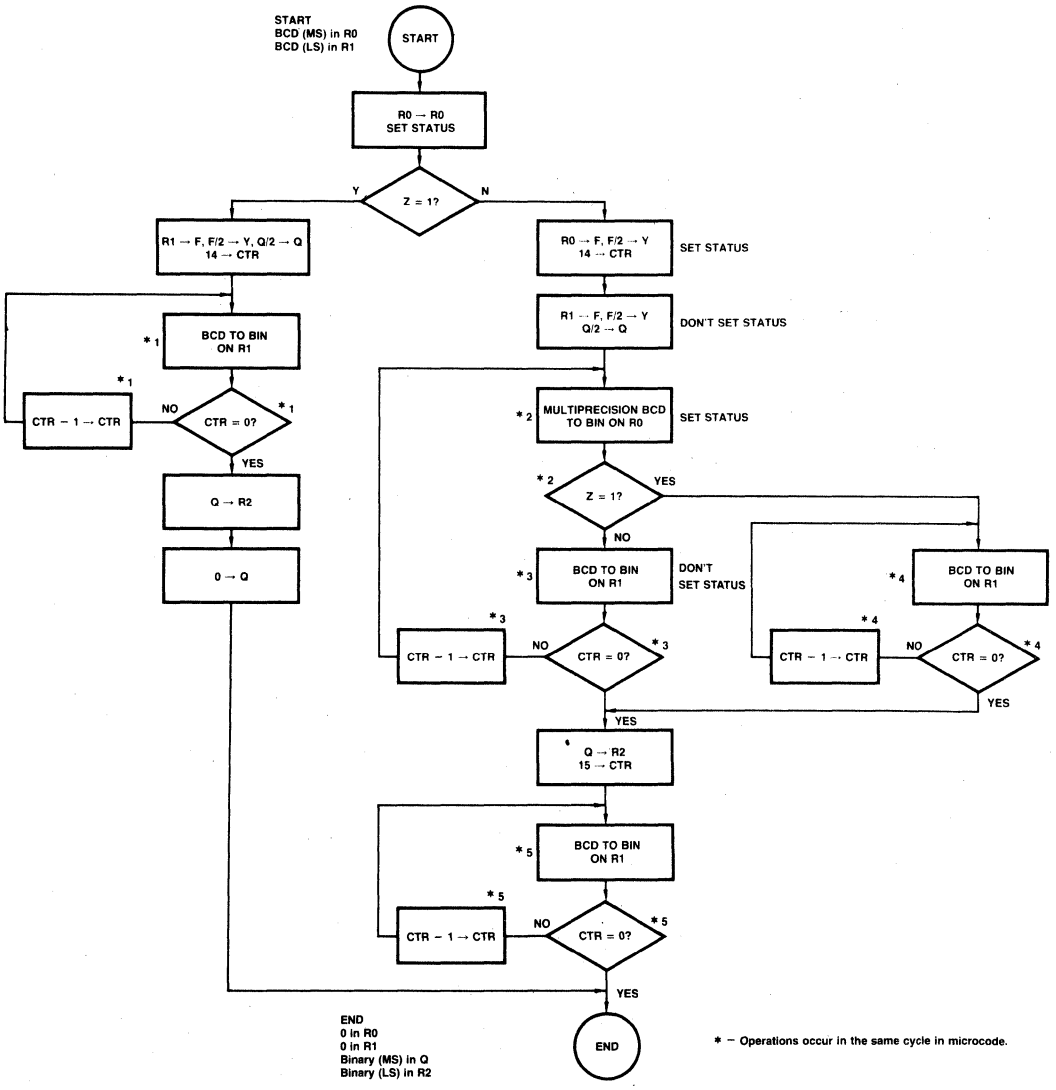


Figure 44. Expanded Memory for Am29203/29707

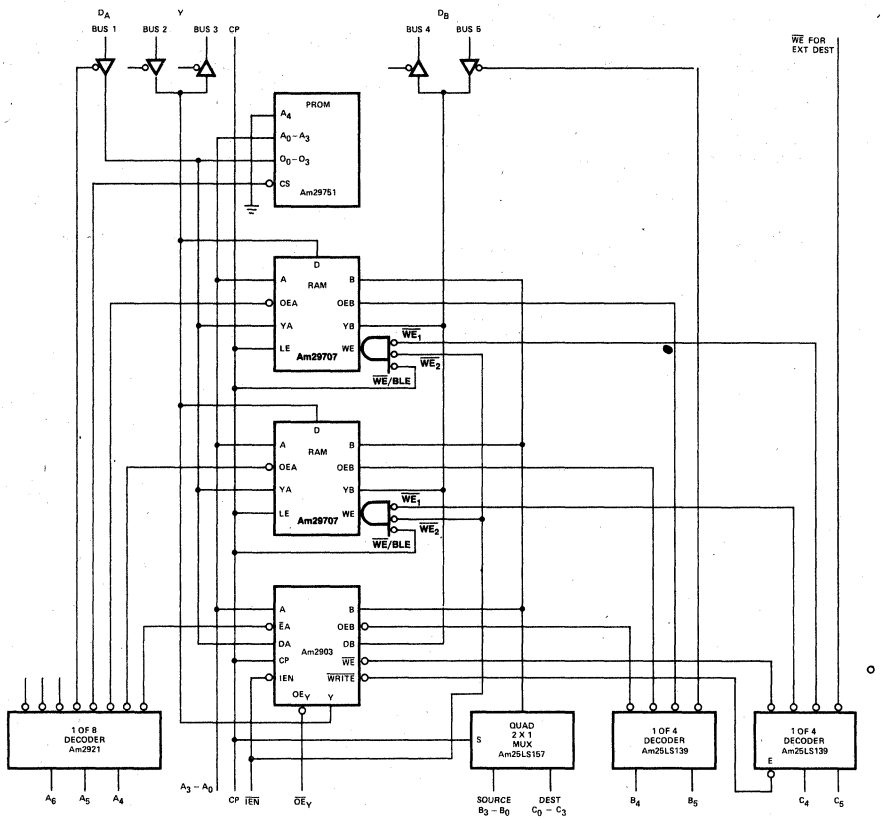
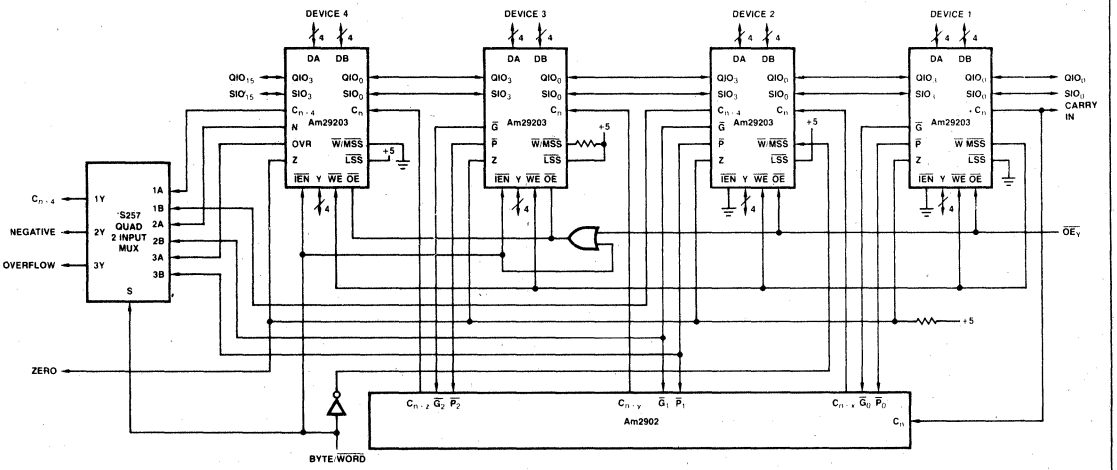


Figure 45. Connections for Word/Byte Operations (Am29203 Only)



MICROPROGRAMMED SYSTEM DESIGN

A family of bit-slice chips provides modules for customizing processors and microcode

by Sunil Joshi and Deepak Mithani

Microprogramming is used in systems with large and very large scale integration building blocks, as well as within the integrated circuits themselves for implementing the control sections. In systems, the technique is applied wherever conventional microprocessors fall short of speed and adaptability requirements. With microprogrammable large scale integration building blocks, customizing computer architecture to suit various applications becomes easier, faster, and more efficient. Larger systems that use a microprogrammed approach can remove speed bottlenecks and increase throughput. Embedding the most frequently used software in microcode provides a speed advantage. Possibilities include word processing routines, compilers, database managers, and interpreters. To cut software size, microcode can directly execute higher level languages, such as Pascal or C. Moreover, developing powerful customized instructions substantially improves throughput.

A custom designed computer has two options: a random logic hardwired approach or a microprogrammed approach. With random logic, the control section of the machine is reduced to a state machine design that can be implemented in hardware. Microprogramming provides a more modular and systematic method of implementing the control mechanism of a machine, because the control sequence is stored in an array that can be accessed systematically. Modularization of the random logic to reside in an array makes it as easy to change as if it were software; this firmware pattern usually resides in a programmable read only memory (PROM). A sequencer then addresses different locations of the PROM to execute different controls to the other sections of the machine. PROM microcoding is not as fast as hardwired logic for the same level of technology because of its slower access time. However, microprogramming is typically used for building high speed systems that are several times faster than those built using general purpose microprocessors. This is possible because most building blocks for microprogrammed systems use bipolar technology, which is faster than metal oxide semiconductor (MOS).

Although the concept of bit slicing is independent of microprogramming, bit-slice processors are commonly used in microprogrammed systems. The flexibility of microprogramming can be used effectively for cascading and controlling several bit-slice processors to form larger-width systems. Together with bit slicing, microprogramming achieves high performance through variable data widths, customized instruction sets, and novel architectures. Typically, this technique requires more hardware than microprocessor designs. Because of

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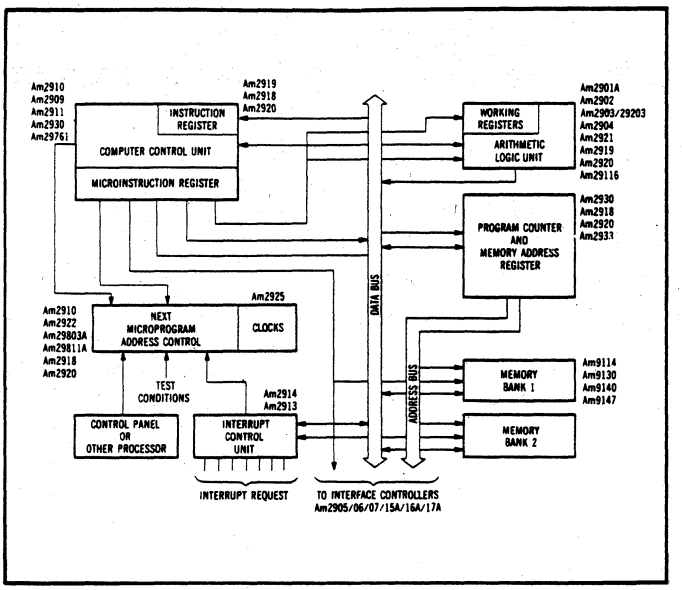

Fig 1 Generalized computer architecture. Control path occupies key path position, influencing throughput.

their flexibility, microprogrammed systems can be optimized for various considerations such as speed, power dissipation, chip count, and design time. Cost and design time, for example, are not easy to estimate. Although it may take longer and cost more to design a new system, only minor microcode changes may be necessary to upgrade to the next version, reflecting a lower overall cost. The Am2900 family of large and very large scale integration building blocks for microprogrammed systems is used here to illustrate the architectural issues and design tradeoffs involved in selecting and configuring microprogrammed devices.

Control path

The heart of the microprogrammed machine, the control path comprises a sequencer, the microprogram memory where the control bits are stored, and a pipeline register at the

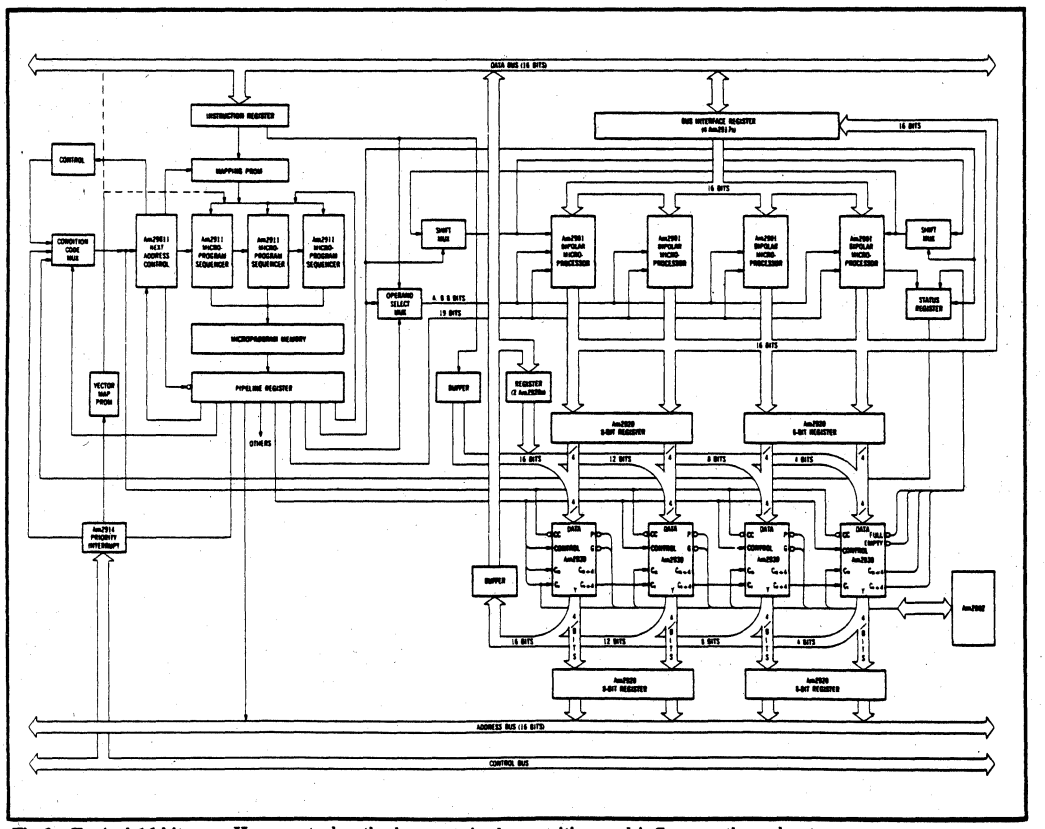

Fig 2 Typical 16-bit CPU. Here control path also occupies key position and influences throughput.

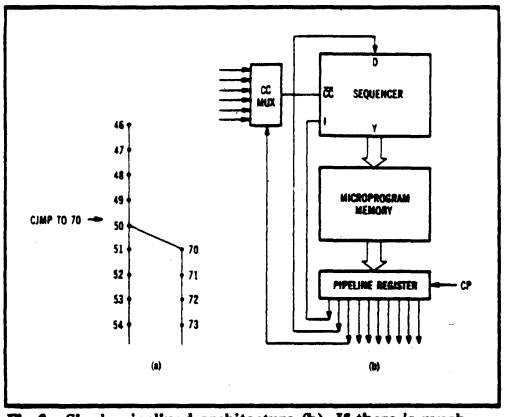

Fig 3 Single-pipelined architecture (b). If there is much branching in microcode flow (a), single pipeline will not waste cycles branching, and therefore have fast clock time.

output of the memory. (See Fig 1 and Fig 2.) The sequencer provides the addresses to the PROM for the control word, which must execute next, and controls the program flow and branching. This is the only hardware required for a controller that does not require an arithmetic and logic unit (ALU).

Pipelining. The pipeline (PL) register at the output of the PROM breaks the address path to prevent race conditions. The microinstruction in the PL register executes in the current cycle while the next microaddress is simultaneously computed in the sequencer, which then accesses

An important consideration in choosing between single and double pipelining is the throughput, as opposed to raw speed.

the contents of this address in the PROM. Several bits in the microword act as an instruction field for the sequencer. This field tells the sequencer to continue to the next address, and whether or not a conditional branch or subroutine access is required. When a branch on a condition is desired, the appropriate condition is selected through the condition code multiplexer, which causes the sequencer to branch if the condition is met (Fig 3). That is, if a branch is performed while instruction at address 50 is in the PL, then either 51 or the branch address 70 is at the output of the sequencer for PROM access. Other controls specified in address 50 execute whether the branch is taken or not.

Critical speed path for this architecture, called single pipelining, consists of the sequencer propagation delay in series with the PROM access time. This path may limit the fastest cycle time of the machine. When a faster cycle time is necessary, a double-pipelined architecture breaks the critical path into two smaller paths by placing a second PL register at the output of the sequencer (Fig 4). When the contents of address 50 are in the PL1 register and the instruction is a branch, address 51 is present in PL2. If the branch is taken, address 70 is at the output of the sequencer. Thus, when a branch is taken, the contents of address 51 execute before the contents in the branch address 70 appear in the PL1. Because the PL register has to be "flushed," a latency of one clock cycle is added before the required branch instruction executes. Double-pipelined architectures require two cycles to take a branch of any kind, including subroutine jumps, returns, and so forth. In most cases this extra instruction cannot perform a useful operation in the ALU, and becomes a "no operation."

One important consideration when choosing between a single- and double-pipelined scheme is the throughput that can be achieved, as opposed to raw speed. Because of shorter critical paths, double pipelining allows faster clocking speeds. However, if considerable branching exists in the microcode flow, it may take two cycles to execute every branch. One cycle may not function usefully in the ALU, thereby reducing the machine's overall throughput. Double pipelining is more useful when the program flow consists of very few branches. When much branching is required, more functions can be performed in a fixed amount of time using single pipelining, even though the clock speed is slower. Double pipelining for applications using frequent branching results in extra code space, which increases the length of the code and may call for more PROMs. The microcode may also be difficult to read and debug, increasing the design time.

The PL register shown for the single-pipelined architecture may not be required for some bits of the microword (Fig 5). This happens when a register is built at the input of the controlled device for the purpose of synchronization, as in the case of the Am2925. In such a case a registered PROM cannot be used for these bits.

Horizontal and vertical microprogramming. In horizontal code, the microword bits are assigned so that all the devices controlled by the microcode have their control bits allocated in the same word, allowing them to be controlled simultaneously. With dedicated bit control for all the devices, parallelism is at a maximum, and many events can be initiated in a single cycle. In vertical microcoding several devices are assigned for a 1-bit field with only one device selected per cycle. Since only one device can be controlled at a time, several lines of code may be required to control all the devices sequentially.

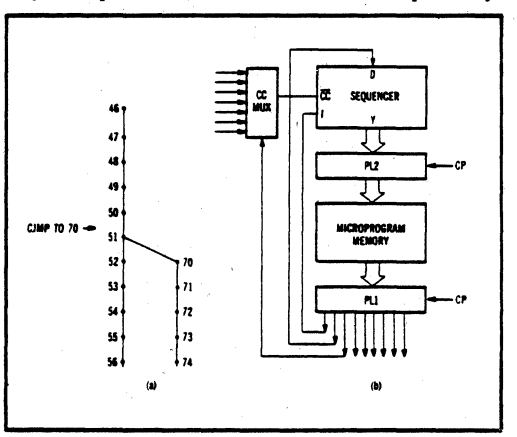

Fig 4 Double-pipelined architecture (b) can achieve shorter critical paths and use faster clocking than single pipelining when branching occurs (a).

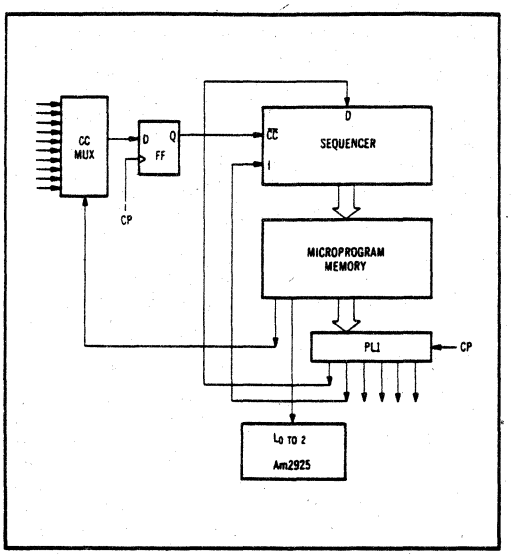

Fig 5 Single-pipelined architecture with bypassed PL register. Some bits of microword are input directly into Am2925 when pipelining is not required for entire microword.

Vertical microcoding is so called because the width of the code is reduced by field sharing but the length increases; additional instruction enable bits in the microword indicate which device is selected. Since the total amount of PROM adds to the cost of the system, it is important to minimize the width and length of the microcode. In many cases vertical microprogramming reduces the chip count for the PROMs, as those with a larger addressing space or depth are more common than those having a greater data width. Horizontal code, on the other hand, allows maximum parallelism and hence maximum throughput. The desirable approach, therefore, is to share fields where parallelism is not required. This is possible for example, while controlling the Am2914, which is an interrupt controller. In central processing unit (CPU) emulations it is checked for interrupts only at the end of every machine cycle but its four instruction lines can share code with some other device.

One commonly shared field for the sequencer is the branch address field of the Am2910, which is also used for loading the register/counter. With the restriction that no branching will be allowed while loading the counter, several bits of code can be shared. Other fields that can be shared with ALU fields are the interrupt controller (Am2914), the status controller (Am2904) and the program control unit (Am2930) fields. The direct memory access (DMA) controller (Am2940, Am2942) fields are usually not shared with the ALU fields because the ALU is used for loading the DMA device. The Am2910 branch address field can also be shared with the Am2904. Most of the Am2900 family devices have an instruction enable $\overline{IEN}$ pin to permit field sharing.

Microprogram memory. The microprogram memory is usually a PROM or an electrically programmable read only memory (EPROM). Sometimes a random access memory (RAM) may be used, which is referred to as a writable control store (WCS). The WCS is not only useful for program debugging, but can also be used for context switching between different microcodes. A WCS can be built using a dual-ported RAM that can be written into by one address port and read via the sequencer address port. The use of a WCS, however, complicates the hardware around the sequencer because extra logic is required to bootstrap the WCS during startup. A WCS is typically used for development system design and for machines which change their personality by reloading a different microcode.

Sequencers. A commonly used sequencer is the Am2910 because it has a 12-bit wide address path to access 4k words of microcode, and a 5-deep stack for subroutine nesting. It also contains a counter that executes microcode loops. The 4-bit wide Am2909 or Am2911 may sometimes be preferred, because they are faster and less complex than the Am2910. Each requires either external small scale integration or an Am29811 and a counter to control them, but they can cascade to form address widths larger than 12 bits, making them suitable for specialized applications. The Am2911 is a 20-pin version of the 28-pin Am2909 and saves board space, while the Am2909 offers a degree of parallelism in that its register can be loaded while a branch is being taken via the D input. Both allow a custom designed instruction set.

Data path

Most microprogrammed systems have an ALU selected on the basis of the numerical computation required by the desired applications. Some applications need the emulation of an existing CPU while others involve new designs. A major consideration for CPU's is the ALU's number crunching capability. The other class of application is general purpose, such as disk or communication controllers. Controllers usually do not require much arithmetic capability but must be efficient for high speed data transfer and bit manipulations.

The Am2901 and the Am2903 have been used widely as ALUs in the past, and two new introductions to the family constitute the Am29203 and the Am29116. The first three are 4-bit slices and can be used for variable data widths, while the Am29116 is a 16-bit fixed width ALU. The Am2901 is the simplest of the 4-bit ALU slices and has a basic instruction set for logical and arithmetic operations, and also has a 16-word dual-ported RAM and a shifter. This device allows the fastest cycle time among ALUs and is used for simple but high speed controller designs.

As opposed to the raw speed that can be achieved using the Am2901, the Am2903 allows for a higher throughput. The Am2903 has its shifter after the ALU, several data entry ports (DA, DB, and Y) and an expandable register file. Its special instructions include unsigned and 2's complement multiply, divide, normalize, and sign extend. Thus, multiply and divide routines can be written for both integer and floating point operations. The normalize instruction allows incrementing the exponent and the shift operation in the same cycle using a single line of microcode.

Am29203 is an enhancement of the Am2903. In addition to the Am2903 instruction set, the Am29203 has instructions for binary coded decimal (BCD) arithmetic. BCD numbers are useful in applications that may be input/output (I/O) intensive and need to input or output data in decimal or ASCII formats. Retaining this data as

BCD, instead of converting it to binary, has the advantage of not requiring overhead in converting data types for input and output.

Machines using BCD representations tend to perform more additions and subtractions on these numbers than multiplications and divisions. Therefore, the Am29203 instruction set has single-cycle BCD add and subtract instructions, with mechanisms provided for BCD multiply and divide in multiple cycles. The Am29203 also has bidirectional data buses DA and DB, so that they are symmetrical. This is unlike the Am2903, in which only the DB bus is bidirectional. The architectural impact of this is that data could be output on both DA and DB simultaneously from the dual-ported RAM, and could also be used internally by the ALU for computation. Data output on DA and DB could be used to provide a parallelism in the data paths or even to implement fault tolerant ALU schemes. In the latter case, an external parity checking circuit verifies the parity of the data both before and after the ALU operation. The Am29203 also provides multiprecision arithmetic capability for BCD numbers. Since each BCD digit occupies 4 bits, a 16- or 24-bit machine may be able to store only 4 or 6 BCD digits, respectively, using single precision. However, double- or triple-precision representations allow the use of many more BCD digits for accuracy without adding to the cost of the system by adding more slices.

Am2903 and Am29203 are suited for designing CPUs that are either accumulator based or general register based. In general register architecture it is possible to have 1-, 2-, or 3-register addressing. The 3-address machine is implemented by multiplexing the third address on the B address port. Some CPU designs require more than 16 registers. Even this can be achieved by adding the expander register file Am29705 or Am29707 to the ALUs. These ALUs can also be used for designing stack oriented CPUs by adding an address control section that treats the register file as a stack and keeps track of the pointers.

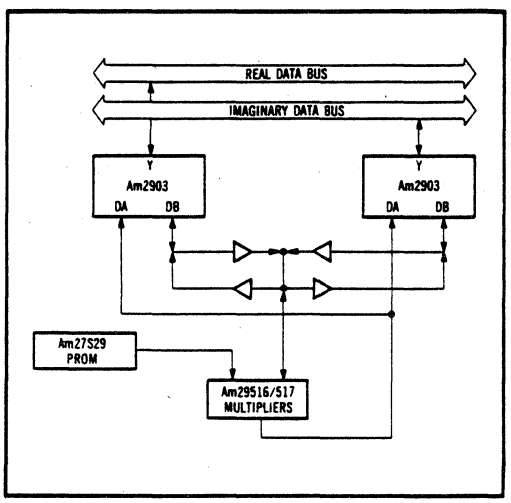

Fig 6 External multiplier with Am2903. Bidirectional DB port allows use of hardware multipliers with external PROMs for applications requiring large amount of fast multiplication.

If the Am2903 or the Am29203 are used for CPUs, the Am2904 status and control chip can be used for compressing most of the small scale integration around them into one chip. The Am2904 incorporates all the multiplexers, status registers, and linkage control hardware in a single chip; it is also useful for several CPU emulations because its instructions allow efficient manipulation of status bits. For example, some machines either store a borrow on subtraction, or just store a carry. The Am2904 can convert between the two schemes because it has both a micro and machine status register. The micro status register is particularly useful where interrupts can occur at microcycle boundaries, and saving of micro status is essential.

Another consideration in CPU design is interfacing with various buses and peripherals. The ALUs described here interface to both multiplexed and demultiplexed data and address buses on the backplane. Three separate buses (DA, DB, and Y) on the Am2903 and the Am29203 permit a variety of architectures. Reliability of the data path can be improved by adding error detection and correction capability in the paths to and from the memory to the ALU. Error detection and correction can be implemented by using schemes such as Hamming codes, which add redundancy to the data paths by adding extra check bits. The Am2960 error detection and correction chip uses modified Hamming code for detection and correction of single-bit errors and detection of double-bit and some multiple-bit errors. It is cascadable and can handle data width from 8 to 64 bits when used with bit-slice ALUs.

In spite of the extremely fast speeds that can be obtained by using bit-slice parts, these ALUs may still be slow for some specialized applications. Examples of these are in signal processing where a great deal of multiplication using complex numbers has to be performed. The Am2903 and the Am29203 have been designed with the necessary hooks for configuring them with a hardware multiplier or an external PROM for fast table lookups. Fig 6 shows how the bidirectional DB port can be used as an advantage for hooking up to a 16 x 16 multiplier. This achieves an order of magnitude improvement in throughput.

Although the Am2901 and Am2903 were designed and optimized for CPU applications, they have also been commonly used for controller designs. Intelligent controllers must be very efficient in the movement of data, manipulation of status, and response to events and interrupts. They are characterized more by bit manipulation and logical operations than by number crunching and complex arithmetic. The Am29116 is a 16-bit fixed width processor optimized for controllers. Its architecture is characterized by a single-port RAM, an accumulator and a data latch for temporary storage of data, and a 3-input ALU for performing an operation on three operands simultaneously.

The Am29116 has a bidirectional bus for the input and output of data. A 16-bit barrel shifter is provided to rotate a word by up to 16 bits in one microcycle. The combination of a 3-input ALU and a barrel shifter allows operations such as rotate and merge, where one operand is rotated up to 16 places, and selectively merged with another operand using a third operand as a mask for the selection. In addition, the Am29116 has features such as priority encoding, cyclic redundancy check computation,

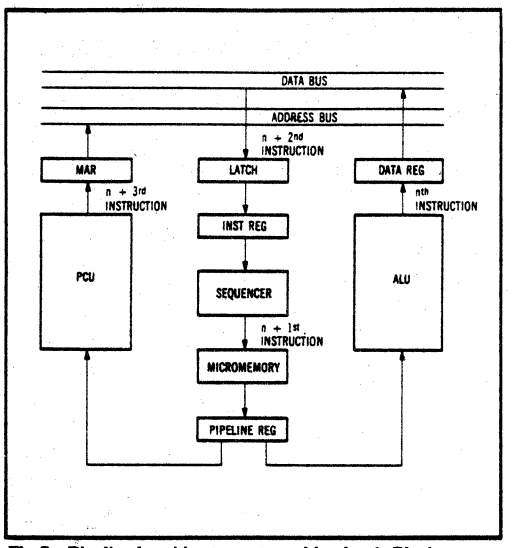

Fig 7 Pipelined architecture at machine level. Placing address generation in separate hardware, relieving ALU, allows increased parallelism.

and the capability to execute immediate instructions where constants can be brought in on the instruction inputs using two cycles. It also improves the power dissipation and the chip count compared to an implementation using the Am2901 or the Am2903.

Address path

System performance is largely determined by the addressing mechanisms and modes employed. Need for efficient memory addressing becomes more evident with the availability of the faster and more efficient processors. To access random information from the memory, different addressing techniques are used. In general register architecture, one register is designated as the program counter and others may be assigned tasks such as index register, stack pointer, upper bound and lower bound for stack, and so on. Using these registers, different addressing techniques such as program counter relative, indexed, immediate, base register relative, and indirect addressing can be implemented very efficiently. In addition, ability to manage stacks for subroutine linkage and for expression evaluation enhances the flow of control though a system.

A system that does not use a separate program control subsystem usually uses a general register architecture for addressing. In this situation, address for the main memory is generated by the ALU. If all the registers associated with main memory addressing are removed from the ALU and placed in the program control subsystem, then the address computation for the next macroinstruction can be done concurrently with the ALU operation. Thus, the use of separate hardware allows more parallelism in a system at the macroinstruction level.

Such a program control unit can be implemented using the Am2901s or Am2930s. In this system (Fig 7), the nth instruction is executed in the ALU during a register to register instruction. The instruction register is loaded with the n + 1st instruction from the Z latch, and the starting address is generated in the sequencer. The n + 2nd instruction is read into the Z latch from the main memory, and the address for the n + 3rd instruction is loaded into the memory address register (MAR).

The most general purpose type of program control unit can be implemented with Am2901s. Its 16-register, 2-port file structure provides several advantages in terms of stack pointer control, stack pointer boundary checking, program control, and implementation of different addressing modes. For a simple program control unit, the Am2930 provides 17-deep subroutine linkage stack, index register, program counter, and an ALU for relative addressing. Both devices are 4-bit slices and are cascadable up to any width of address required, which makes the expansion of the main memory easy.

System timings

Clock speed, which increases the performance, is determined by the delays through the various paths, the longest being the critical path. In a conventionally microprogrammed system, the slowest microinstruction execution time determines the microcycle time, even if it is the only slow microinstruction. In such a system, much microcycle time goes unused during the execution of all other microinstructions. To improve the microcycle time, these functions are sometimes broken into several shorter instructions, but this is cumbersome and adds to the amount of microcode. An alternative solution is to vary the microcycle time and stretch the cycle whenever the slow microinstructions are executed (Fig 8). This solution provides maximum usage of the microcycle time for all microinstructions.

The Am2925 clock generator and microcycle length controller can vary microcycle length depending upon the microinstruction being executed. The Am2925 takes the oscillator output as basic clock, (FO), and generates four clock outputs, each with a different duty cycle. The output clocks can have a period from three to ten times the basic FO clock period. Information about the microcycle length is extracted from the microcode in the preceding microcycle (Fig 5). For simple applications, the Am2925 generates a clock with approximately 50% duty cycles. For special applications, like the 3-address architecture with the Am29203, the Am2925 also generates an appropriate clock (always low during the last two FO cycles) to drive the instruction enable input for proper write timing into the 2-port RAM. In addition, the Am2925 can insert wait states to synchronize other parts of the computer system, such as memory and I/O devices, with the CPU. For debugging a system, the Am2925 also permits single-stepping of the microcycle. In general, the throughput of a system can be improved by 10% to 25%, using the Am2925, depending upon the instruction mix over the fixed length system.

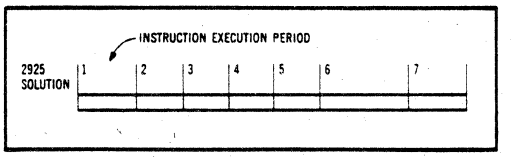

Fig 8 Microcycle stretching. Varying microcycle time improves overall microinstruction efficiency.

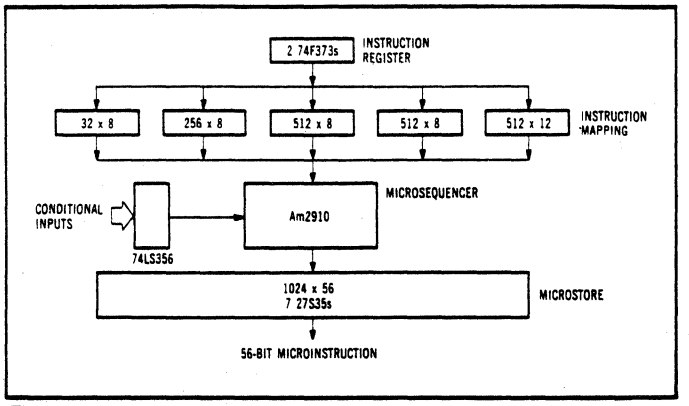

Fig 1 HP 1000 A600 sequencer. Registered PROMs contain A600 microstore and pipeline register in only seven packages.

HP 1000 architecture permits referencing registers as memory location 0 or 1. An FPLA detects this condition, and the ALU source or destination is selected as either memory, or the ALU register file accordingly. An additional FPLA is part of the status register and determines, based on the status register contents and the instruction register contents, whether conditional instructions will skip the next instruction.

A600 memory is both a memory controller and a memory array. The array portion can be either 128k or 512k bytes, with additional array cards able to increase main memory to 4M bytes. Memory has a cycle time of 454 ns and uses simple parity for error detection. A dynamic mapping system is also part of the memory controller. It consists of 32 sets of 32 page-mapping registers, and maps logical addresses into physical addresses as shown in Fig 3.

Every memory cycle is a mapped memory access. The address extension register is loaded by the processor or direct memory access (DMA) and selects one of the 32 sets of maps. Each 15-bit logical address is divided into two parts: a page number and an offset. The page number selects one of the 32 page-mapping registers. Since each page is 1024 words, the 32 map registers provide a 32k logical address space. Each register contains a write protection bit and a 14-bit physical page number. If the write protection bit is set, any write cycle to this page will not be permitted and will generate a processor interrupt. The 14-bit physical page number is combined with the logical address offset to provide a 24-bit physical address. This allows the microcomputer to address 32M bytes of physical memory.

Standard HP 1000 minicomputer input/output (I/O) interface cards, which were introduced with the HP 1000 L-series computer, are also used with the A600. Each interface card contains a custom complementary metal oxide semiconductor (CMOS) I/O processor capable of executing I/O instructions to communicate with the processor board, and of performing DMA transfers with memory on a cycle stealing basis. The microcomputer provides a memory page map for each I/O interface, permitting DMA transfers to any page or combination of pages in physical memory. Its memory cycle time of 454 ns provides a backplane bandwidth of 4.3M bytes/s.

Software compatibility guarantees that a correctly written application program for a member of the minicomputer family will execute correctly on the A600 microcomputer. For the microcomputer design, software compatibility meant that the macro level machine characteristics had to be fixed. Thus, the microcomputer has the same register set, instruction set, time base generator, memory mapping, memory protection, and powerfail capabilities as the minicomputer members of the family.

Rather than a limitation, the software compatibility requirement was actually a benefit. Instead of requiring months of effort to invent a new architecture, the microcomputer architecture was well defined from the start. This permitted the design team to concentrate on features to improve the computer price/performance

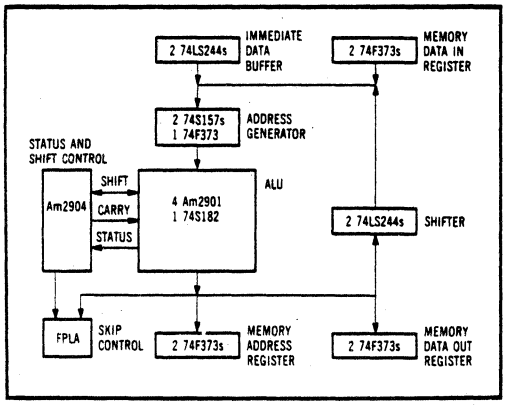

Fig 2 HP 1000 A600 arithmetic unit. Implementing ALU with bit-slice LSI chips delivers outstanding price/performance while minimizing board space.

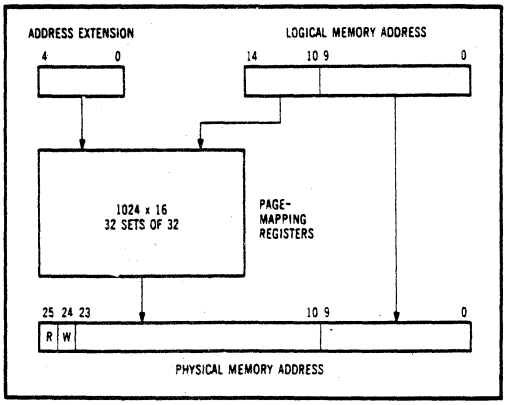

Fig 3 Logical address to physical address translation. Mapping hardware allows A600 microcomputer to access 32M bytes of memory with read and write protection.

Interrupts

Interdevice communication efficiency depends on the ability of the CPU to handle asynchronous events. Polling is one way of interdevice communication in which the CPU interrogates each device by asking it if service is required, starting with the highest priority device. This approach is slow and inefficient, causing more overhead. The more efficient way of servicing asynchronous events is the interrupt method. Whenever a device needs service from the CPU it generates an interrupt request signal to it. If the requesting device is of the highest priority, then the CPU suspends the program currently executing and services the requesting device as soon as it receives the interrupt request. After servicing the device, the CPU resumes the previously suspended program if there are no other devices requesting service. If more than one device requests service at the same time, then the device with the highest priority will be serviced first. When an interrupt request is being serviced, only another interrupt request with a higher priority can interrupt the routine; this allows nesting of interrupts within interrupts. These functions are usually performed by an interrupt controller that may also have features to selectively mask certain interrupts.

Interrupt handling can be efficiently implemented by the Am2914 vectored priority interrupt controller. Cascadable to any number of priority levels, it can be microprogrammed to meet the requirements of specific applications. For example, interrupts can be handled at two levels by the microprogrammed CPU—the macrolevel interrupt or microlevel interrupt. In the macrolevel interrupt, the CPU checks for any interrupt request after completing the execution of every macroinstruction. If any request is pending, the CPU services the device and then returns to the interrupted program. As soon as the device request is granted by the controller, the CPU completes the current microinstruction and jumps to the service routine for that particular device. The Am2914 can be used for both types of interrupts.

Direct memory access

High speed techniques are required for transferring blocks of data between the main memory and the I/O devices. The three most widely used techniques are programmed I/O, memory mapped I/O, and direct memory access I/O. The DMA technique uses a direct path between the main memory and the I/O device to perform data transfers, thus relieving the CPU for other tasks. The CPU initializes the DMA device by sending a memory address and the number of words to be transferred. Actual data transfer is done directly between the I/O devices and the memory through the DMA interface. DMA transfer can be implemented by three methods. In the first method, the CPU is put on halt, while the DMA data transfer is being performed. The second method time slices each memory cycle into halves; one for the CPU and the other for DMA transfer. But the most commonly used technique is cycle stealing, which is also the most efficient way to utilize the available resources. In this method, the DMA device steals a CPU memory cycle whenever the CPU is not using one, and performs a DMA transfer.

Am2940 DMA address generator is partitioned into 8-bit slices cascadable to form large memory addresses. With the Am2950 I/O port, it can handle over 5M words/s. The Am2940 generates sequential addresses for block transfer. Word count for block transfer can be programmed by the CPU, and the Am2940 also maintains the word count and generates a signal when the block transfer is complete. One or more Am2940s can be used in each peripheral controller of a distributed DMA system. Microprogrammability of this part provides complete flexibility for the desired architecture.

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Design

Combining the speed of bipolar 4-bit-slice architecture with new decimal-arithmetic capability, a microprocessor takes aim at business-system applications formerly dominated by large computers.

Bit-slice processor speeds through BCD math

5

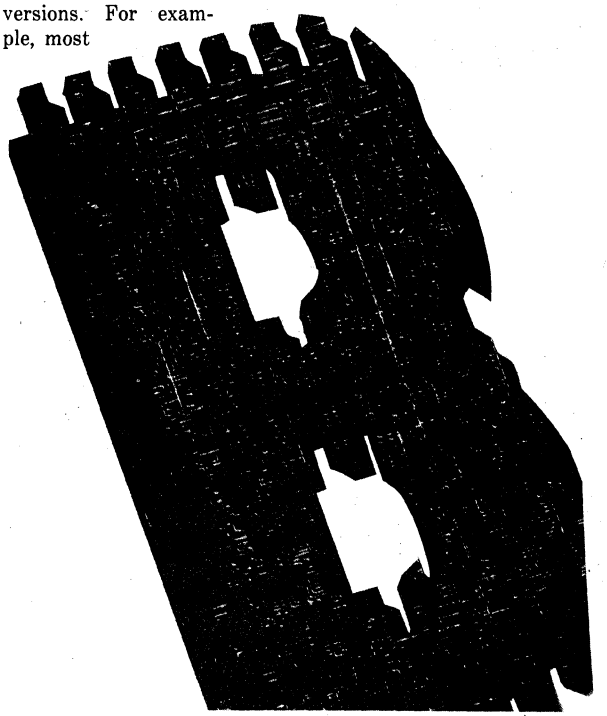
For the first time, binary-coded-decimal (BCD) arithmetic will be brought to minicomputer-class systems. The vehicle is the Am29203 microprocessor slice, which calculates directly in the decimal system. As a result, such systems will be able to make inroads into a growing number of business applications, including distributed satellite office machines and point-of-sale terminals. Previously, BCD data handling was dominated by large computers of the IBM 360/370 variety and desktop calculators.

Taking up where the Am2901 and 2903 left off, the 29203 continues the tradition of flexible, microprogrammed building blocks with low package count (see "Benefits of a Microprogrammed Machine"). Like its predecessors, the 29203 is a 4-bit-slice ALU and shifter with two operands entering from a two-port register file. Although it features the standard ALU functions of the Am2903, the Am29203 has twice the number of special instructions—the 2903 instructions are a subset of the 29203 instruction set. A major portion of the expanded instructions allows designers to manipulate the new BCD-type numbers.

The 29203 adds BCD arithmetic capability to TTL processors, along with the speed and flexibility for which the Am2900 family is already known. Behind the new processor's performance is the combination of AMD's proprietary LSI technology, called the Imox process, and internal ECL circuitry.

A processor that operates directly on decimal numbers offers many benefits in business applications, notably processing numbers created by and for the business community. Compared with "scientific" numbers—data produced for engineering or scientific use—"business" numbers have limited precision (about eight or nine decimal digits). A business number begins in ASCII format, is changed to BCD, where addition and subtraction are done—there are few divisions and multiplications—and is displayed or stored after being converted into a form readable by humans (ASCII). This type of cycle is I/O-intensive, whereas scientific applications are computation-intensive.

Most of the benefits of business processing stem from not having to convert input data to binary, as required by scientific applications. Performing arithmetic directly on BCD data has two advantages: speed and accuracy. Significant processing time is saved by eliminating base conversions. For example, most



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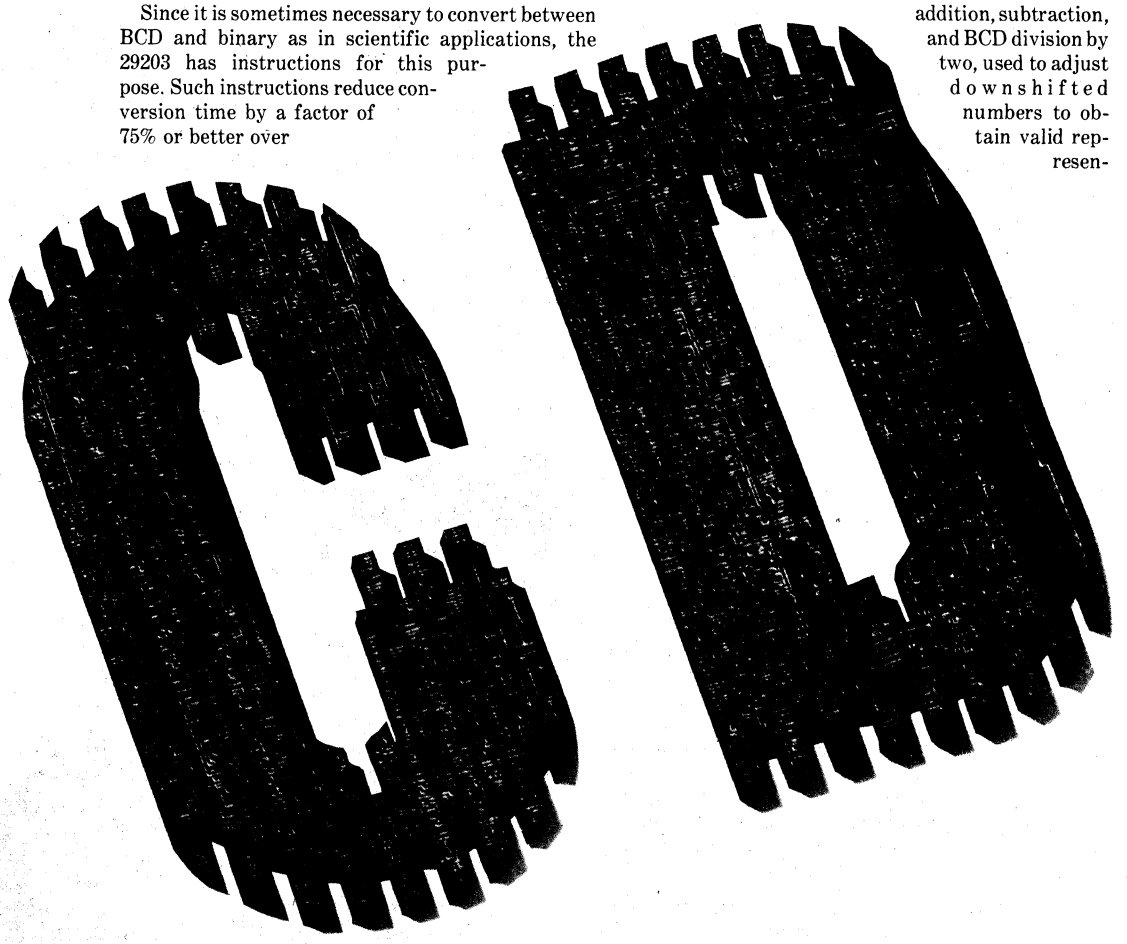
processors communicate data to terminals and printers in alphanumeric code such as ASCII or EBCDIC. But the data must first be converted into a computable form such as BCD or binary. Whether or not the final encoding is BCD or binary, alphanumeric code must first be converted into BCD. This conversion is simple because there is a one-to-one correspondence between ASCII or EBCDIC characters and BCD. It is equivalent to a look-up table procedure followed by packing operations.

When the target encoding is binary, a packed number must be converted from BCD into binary with an iterative algorithm using four operations per digit. In machines without special BCD capabilities, converting into and from binary requires an order of magnitude more time than conversions between alphanumeric code and BCD.

Since it is sometimes necessary to convert between BCD and binary as in scientific applications, the 29203 has instructions for this purpose. Such instructions reduce conversion time by a factor of 75% or better over machines with no BCD capabilities. These instructions handle both single- and double-precision calculations.

One benefit of not having to convert into binary concerns round-off problems When a number is converted from one base into another, it may not be possible to represent it in the new base with a finite number of digits. For example, converting \$0.30 in base 10 into binary gives the infinite series 0.01001101. . . Now the converted number must be truncated and rounded off to fit the limited storage range. Unfortunately, converting from binary back into base 10 does not give the original value. Thus, a computer that performs calculations in the native-base representation is able to eliminate round-off errors. For this purpose, the 29203 has built-in BCD arithmetic capabilities. These include single-cycle addition, subtraction, and BCD division by two, used to adjust downshifted numbers to obtain valid represen-



Bit-slice processor for BCD

tations in the binary-coded-decimal format.

The 29203's overall structure consists of a RAM connected to the inputs of an ALU, the output of which is passed through a shifter and back into the RAM (Fig. 1). The ALU is optimized to execute powerful logic and arithmetic operations on unsigned, two's-complement, and BCD numbers. The ALU, shifters, and RAM all can be cascaded to form larger words and more temporary storage registers can also be added.

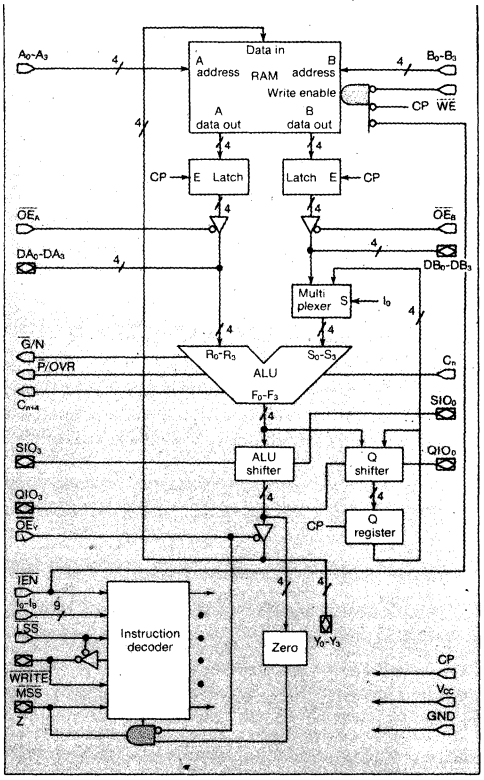
Three buses give flexibility

Using three bidirectional buses, the 29203 is highly suitable for microprogrammed systems that require considerable data-flow flexibility. Buses DA and DB bring external data or constants directly into the ALU for computation. The R and S multiplexers provide the selection between external data and the dual-ported RAM as data sources for the ALU. The result of an ALU operation can be either loaded into the temporary Q register or made available at the Y port after shifting (if necessary). In this case, the Y port may be used as an output port. The result of an ALU operation can be written into any RAM location during this same cycle.

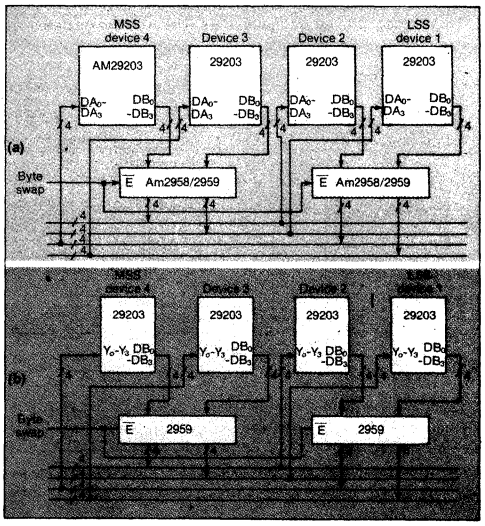
Another way to bring data into the ALU is through the bidirectional Y bus. Under these conditions, output buffers on the Y bus go into three-state operation and data on the Y bus is written into the internal RAM. While this is occuring, the ALU can perform an operation that involves writing into the Q register but does not require the Y bus as an ouput. Buses DA and DB also provide added flexibility when used as outputs. In the simplest case, one or both operands can be put onto these buses, with the result of the operation appearing on the Y bus. Because these outputs are available, they can be used by a fault-tolerant computer for performing external parity checks on the data paths preceding the ALU. Then the parity or check bits can be matched with those derived from the ALU's output—including the Y bus and shifted data—to indicate a fault.

When used as outputs, the DA and DB buses allow an external processor to operate on data stored in the RAM. This increases the effective instruction set of the ALU section. Moreover, it is advantageous for configuring a parallel multiplier for fast multiplication. The multiplier accepts data from the DA and DB ports, multiplies it, and loads the result back into the RAM, using the Y bus as an input.

The 2903's multiport architecture makes the implementation of high- and low-order byte swapping simple. Figure 2a shows a byte swap using two data ports. Initially, the low-order byte is stored in devices 1 and 2, and the high-order byte in devices 3 and 4. To make an exchange, the register location of the



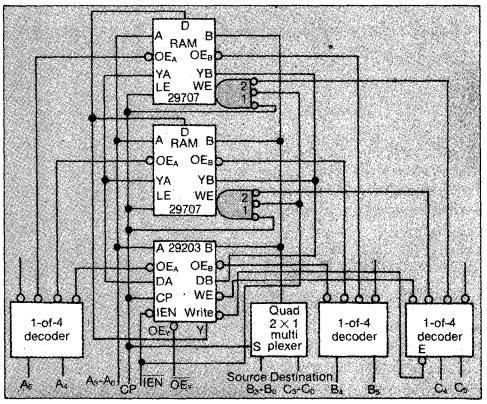
1. Designed around an ALU and an on-board RAM, the Am29203 4-bit-slice processor relies on a bidirectional three-bus architecture to bring external data and constants into the ALU for computation. It can be cascaded to form larger words.



2. Using multiport architecture, the 29203 allows high- and low-order byte swapping (a) and fast byte swapping (b). Permutations of the three-state buffers (Am2958/59) produce any combination of output data. The high-speed byte swap bypasses the processor's ALU, permitting faster operation.

desired word is placed on the B-address port. When the byte swap line is brought low, the bytes to be swapped flow from the DB ports of the 29203 through the 2958/2959 three-state buffers. Permutations of the three-state buffer outputs achieve the byte swap. The resulting permuted data are presented to the DA ports of the 29203, where they are reloaded into memory on the next positive edge of the clock (CP). That is accomplished using the source and function command, $F = A + C_n (C_n = 0)$, for the 2958, or $F = A + C_n (C_n = 0)$ for the 2959, and the destination command, F → Y, B.

A faster circuit for byte swapping is illustrated in Fig. 2b. Instead of being entered via the DA ports, permuted data are entered through the Y I/O ports of OE_Y (held high). This technique bypasses the ALU, allowing faster operation. The 29203 destination command, F → Y, B, should be used in this mode.



3. The 29203's 16-word RAM can be expanded in multiples of 16 words to form long register files. The ALU draws data from any two register locations.

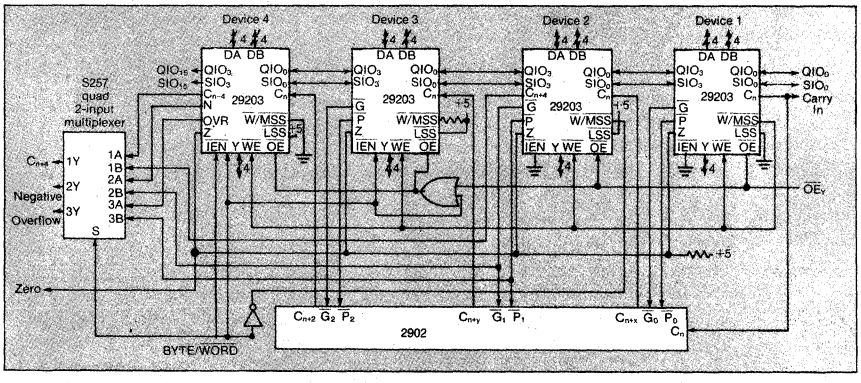
The 29303 contains a 16-word, dual-ported, RAM for temporary data storage. The RAM, which serves as a register file, can be expanded in multiples of 16 words to accommodate as many registers as necessary, using the 29707 (Fig. 3). In addition, the 29203 permits a three-address architecture so that ALU operands may be selected from any two register locations, including the extended registers.

These operations can be achieved in a single microcycle by switching the port-B address in the middle of the cycle. Latches at the RAM output capture the source operands during the first half of the cycle. With the instruction-enable signal ($\overline{IEN}$) held inactive to prevent writing into RAM, the third address can be multiplexed—when it stabilizes, writing takes place by activating $\overline{IEN}$. Using $\overline{IEN}$ as a control also permits a partial word to be written into the RAM. Thus, in a 16-bit system, the upper or lower byte of a word can be independently written by providing an $\overline{IEN}$ control signal for each half of the word.

System handles 16-bit words as well as bytes

In a 16-bit system, both word and byte operations may have to be performed. Apart from the ALU result, status conditions must be available in the word and byte modes. The 29203 forces the open-collector zero-detection pin (Z) to a high whenever the output buffers on the Y bus are three-stated. Thus, a zero-detecting flag is detected only on the byte that is selected. As shown in Fig. 4, the byte-word-selection line turns off the $\overline{IEN}$ and $\overline{OEY}$ signals on the upper two bit-slices and forces the third slice to act as the most significant slice (MSS). As a result, the carry, negative, overflow, and zero flags then apply to the byte mode.

In most ALUs, the zero-detection flag is the last flag to stabilize. This indicates that a microcycle can



4. Word/Byte operations among four 29203 processors are possible using the circuit illustrated. The byte-word selection line determines which 29203 acts as the most significant slice (MSS).

Bit-slice processor for BCD

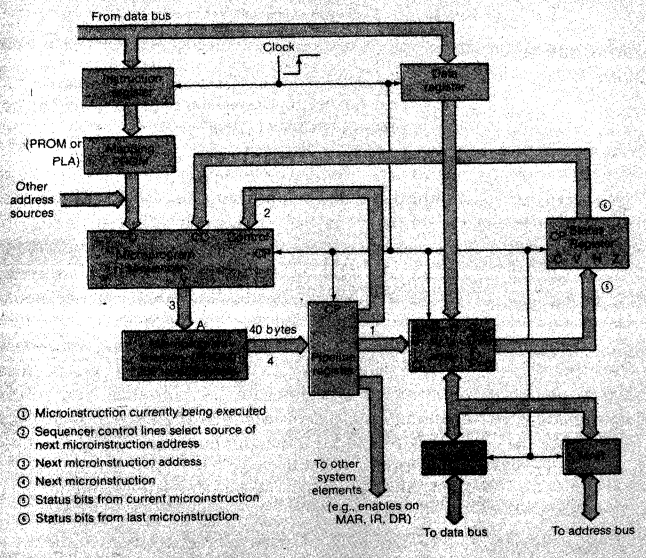
be completed only after this flag stabilizes at the input of the status register. In the 29203, zero detection is performed at the output of the ALU shifter, before the Y-bus output buffers. In that way, the zero-detection flag is available simultaneously with data on the Y bus. Propagation delays are shortened through one of the critical paths by performing zero detection in parallel, with data going through the output buffers, which are also responsible for translating ECL into TTL levels. Special design techniques have been used in the 29203 to increase the speed of the zero-detection circuitry

Benefits of a microprogrammed machine

Many current processors are designed using microprogramming techniques, in which a large part of the system control is performed by read-only memory—usually PROMs—rather than by arrays of gates and flip-flops. The technique often reduces the package count of the controller, gives it a highly ordered structure, unlike random logic systems. Moreover, because firmware, rather than hardware, is altered, microprogramming simplifies changes to a machine's instruction set, substantially reducing postproduction engineering costs. This is vital in extending the product life cycle and allows devices to be changed rapidly to suit user demands.

Although the concept of microprogramming has existed for 25 years, it was not until Advanced Micro Devices introduced its Am2900 family that it came into widespread use. Today, in new system design, a designer can choose between microprocessors with a fixed instruction set—the 8080, 8086, and Z8000 are examples—and microprogrammable devices. The benefits of the former include a very low package count—three or four devices—and predesigned instruction sets. Thus designers can begin at a higher design level with respect to the total system solution. With a microprogrammable processor, a designer can define a custom instruction set that is executed much faster than a fixed set, but at the expense of a larger package count.

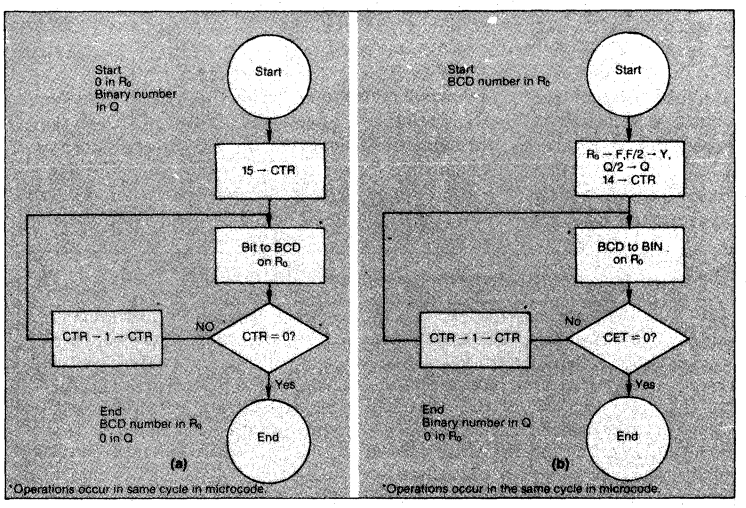
Because firmware implements specialized functions, it can also be used for self-testing. Tests such as system verification and diagnostics speed production testing, in addition to aiding repair personnel in testing the system.



Each device in the 2900 family performs a basic system function and is driven by a set of control lines from a microinstruction. The figure illustrates a typical system architecture. The system has two "sides": The left contains control circuitry, and the right contains data-manipulation circuits. The ALU-array block composes the ALU, scratchpad registers, data-steering logic, left-and right-shift-control, and a carry-look-ahead circuit. Data are processed by moving it from main memory (not shown) into the scratchpad registers, performing operations, and returning the results to main memory. Memory addresses can also be transferred in and out through the memory-address register (MAR). Four status bits from the ALU are captured in the status register after each operation.

In operation, a sequence of microinstructions stored in ROM is executed to fetch an instruction from main memory. This requires that program-counter data—stored in an ALU working register—be sent to the MAR and incremented. The data returned from memory are loaded into the instruction register. Then the instruction register's contents are passed through a PROM or programmable logic array to generate the address of the first microinstruction that must be executed to perform the required function. A branch to this address occurs through the sequencer.

Several microinstructions can be executed to fetch data from memory, perform ALU operations, test for overflows, and so on. Then a branch is made back to the instruction-fetch cycle. There may also be branches to other sections of microcode.



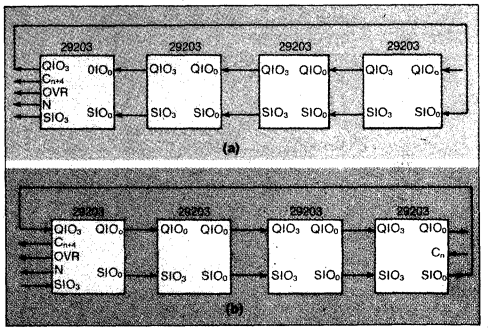
5. Both binary-to-BCD (a) and BCD-to-binary (b) conversions can be performed by the 29203, with either single or double precision. This gives the processor the flexibility to handle business calculations with decimal numbers or scientific work in binary.

(see "Taking Advantage of ECL Technology").

To maintain software compatibility with the 2903, the 29203's instruction set is a complete superset of the 2903's and has the same op-code assignments. The set provides powerful instructions for performing single- and double-length normalization of floating-point numbers, sign extension, and multiplication and division of integers as well as floating-point numbers. Instructions for incrementing and decrementing operands by one or two are included, making it unnecessary to store constants such as one or two. The shift instructions permit both arithmetic and logical shifts. The processor also has a provision for computing the parity of a number that is present in several cascaded slices.

Decimal applications abound

The 29203 is an excellent choice for high-performance, I/O-intensive systems found in a wide variety of applications. They can be small or medium-sized processors that perform word processing, data retrieval and processing, accounting, data management, and inventory control. On the other hand, I/O-intensive systems can also be large, distributed multistation systems having a large control CPU, mass disk storage, and several intelligent terminals—such as for point-of-sale terminals in department stores. Other I/O-intensive uses include high-end data acquisition and control systems that must interface to off-the-shelf programmable instrumentation as well as with analog and digital interfaces.



6. Converting from binary to BCD (a) requires a series of addition and shift operations, essentially the reverse of BCD-to-binary conversion (b). The instructions must be performed several times on a number to yield the correct result.

All these applications require decimal arithmetic capability, plus the ability to handle ASCII formats and binary numbers efficiently. They also require fast responses to events, since a real-time application or human interface may be involved. Human-interface devices, in particular, must have response times no longer than a few seconds, even under maximum load conditions in systems that can be tied up by file look-ups, calculations, and file scans. Such applications necessitate a bit-slice microprogrammed approach, in which the system width can be tailored and the throughput maximized to handle large amounts of data efficiently and quickly.

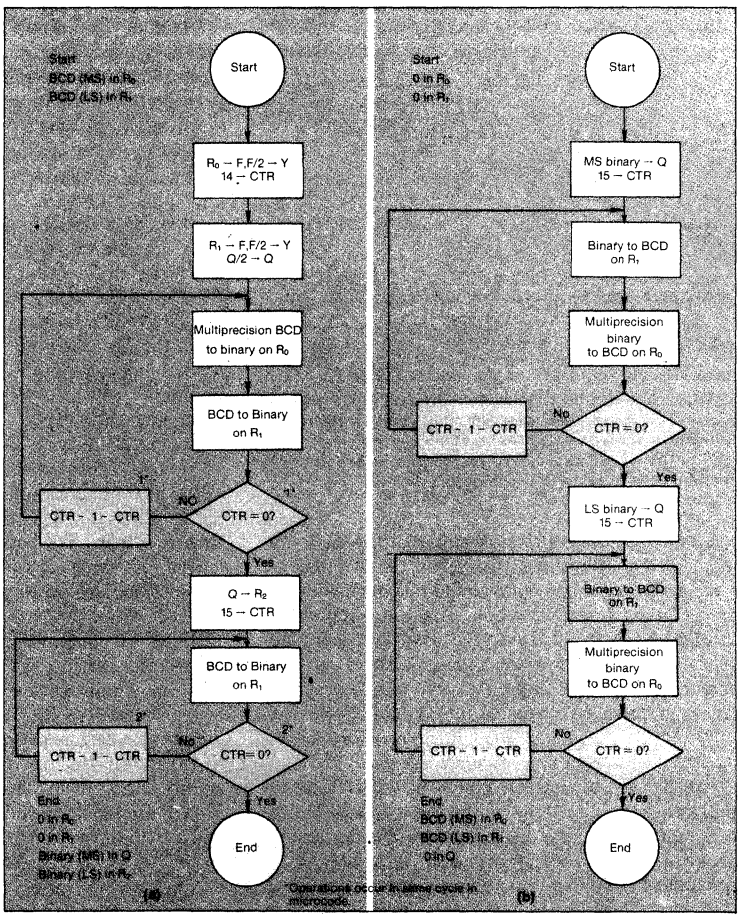
The 29203 has instructions for converting between

Bit-slice processor for BCD

BCD and binary formats and for performing the basic arithmetic functions in both formats. BCD addition and subtraction are the most commonly used arithmetic instructions when calculating with decimal numbers. The 29203 has instructions for adding or subtracting two BCD numbers in one microcycle. The external connections for these operations are the same as for binary addition and subtraction.

A internal carry-look-ahead scheme enables a BCD operation to be executed as fast as a binary one. There are two subtraction instructions in which the R and S operands can be subtracted from each other. When BCD addition or subtraction is performed on BCD numbers, the result is a valid BCD number—but the result is undefined if either operand is an invalid BCD number. An invalid number exists when any group of 4 bits over a slice has a value greater then 9. During addition, the carry output indicates that the result of the addition was greater than 9 over the slice, and that a 1 must be added to the next BCD digit.

The addition process can be speeded up by using a 2902 carry-look-ahead generator. In BCD additions, the propagation signal signifies that the result must be propagated out of the slice. The generation signal indicates that a result is already greater than 9, and that a carry output must be generated regardless of whether the carry input exists. The state of the propagation signal for results greater than 9 is



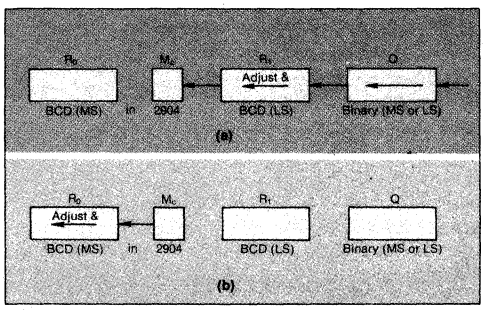
7. Flowcharts for double-precision BCD-to-binary conversion (a) and binary-to-BCD conversion (b) are similar to those for single-precision except for special shifting operations involved in multiprecision operation.

Bit-slice processor for BCD

of shifts must be a multiple of 4 to yield a meaningful result.

Another special instruction facilitates multiprecision binary-to-BCD conversions. Called a multiprecision binary-to-BCD conversion, it acts like a normal binary-to-BCD conversion except for shifting of the Q register. Figure 7 shows the flowchart for the simplest double-precision binary-to-BCD conversion algorithm in a 16-bit system. Initially, the Q register stores the most significant half of the binary number after conversions, two registers, R_0 and R_1—both initially cleared—store the most significant and least significant halves, respectively, of the BCD number.

The shift for each binary bit requires two microcycles. The binary-to-BCD conversion is executed first on R_1, and the most significant bit shifted out of R_1 is stored as the carry bit (M_c) of the 2904 (Fig. 8). Then the multiprecision binary-to-BCD



8. Shift linkages between registers allow the 29203 to perform binary-to-BCD conversions (a), and multiprecision binary-to-BCD conversions. Usually, 16 shifts between registers are required to convert a number correctly from one base into another. Each bit takes two microcycles.

conversion instruction is executed so the R_0 is adjusted as M_c is shifted on. Together, the two instructions account for one equivalent shift of the double-precision number as a whole. After 16 such shifts, the Q register is loaded with the least significant half of the binary number and the same operations are performed again 16 times. Once the single-precision binary number is converted into a double-precision BCD number, the algorithm can be terminated after 16 shifts of the binary number.

The BCD-to-binary-conversion instruction essentially reverses the steps of the binary-to-BCD conversion (Fig. 6b). The BCD number initially resides in one of the RAM registers and the Q register stores the binary equivalent during conversion. The BCD-to-binary algorithm requires that the BCD number first be shifted 1 bit down. Then 3 is subtracted from any BCD digit having a value of 8 or greater. However, since the 2903's shifter comes after the ALU, the BCD-to-binary conversion instruction first performs the adjustment for a previous shift and then performs the shift in anticipation of the next instruction. The BCD number in R_0 is first shifted down 1 bit to load its least significant bit into the most significant bit of the Q register. Then BCD-to-binary conversion is executed 15 times to perform the necessary adjustments and shift successively (Fig. 7). Ultimately, 16 shifts and 15 adjustments are performed on the binary number. An adjustment of the final shift is not required, since the binary number is fully formed, and the BCD number is zero at this point. As in the binary-to-BCD conversion instruction, the adjustment is done independently over each slice, and the carry bits play no role.

Converting multiprecision BCD numbers to binary is similar to binary-to-BCD conversions. The simplest, but not the most efficient, scheme operates according to the flowchart in Fig. 5b for a double-precision number in a 16-bit system.

Initially, the most significant half of the BCD number is stored in R_0, and the least significant half in R_1. The Q register stores a part of the binary equivalent during and after conversion. The BCD number as a whole must first be shifted down by 1 bit. Register R_0 is shifted down as shown so that its least significant bit is collected in the M_c or carry flip-flop of the 2904. Next, R_1 and Q are shifted down, allowing M_c to be loaded into the most significant bit of R_1. The following two instructions perform the adjustments on this shift and downshift the adjusted numbers by 1 bit in preparation for the next adjustment and shift cycle.

The multiprecision BCD-to-binary conversion instruction is executed in R_0, which allows adjustment, downshifting, and storage of the least significant bit in M_c. The following conversion instruction adjusts R_1 and downshifts both R_1 and Q, with M_c being loaded into the most significant bit of R_1. These two instructions are performed 15 times in a loop. As a result, R_0 and Q are shifted 16 times.

Since the contents in R_0 are now all 0s, there is no need for further shifting. The Q register contains the least significant half of the binary result, which is transferred to R_2. Then the BCD-to-binary conversion is performed 16 times on R_1—using the linkages—so that a 0 is entered into the most significant bit of R_1. The most significant half of the binary number is available in the Q register at the end of the operation.□

inconsequential, since the generation signal produces a carry output anyway.

In subtractions, the carry output can be interpreted as a borrow. Borrowing is necessary in BCD arithmetic when the digit to be subtracted is larger than the digit from which it is subtracted. If both digits are equal, a borrow from a higher digit is necessary only if the previous digit borrows. This is equivalent to a borrow signal and is indicated on the propagation line. When borrowing is necessary, regardless of the previous digit, the generation line is active.

A generation signal overrides a propagation, and when it is active, the state of the propagation does not matter. The carry-output signal, CN + 4, goes low when a borrow occurs from a high-order digit. Thus, when a larger number is subtracted from a smaller one, the absence of a carry-output signal from the most significant slice indicates that the result is available as a ten's-complement number. The information then can be used for adjusting the sign of the number. There are several ways to store the sign of BCD numbers; usually they involve a tag bit or a digit to provide sign information.

Binary to BCD and vice-versa

The binary-to-BCD conversion instruction must be performed several times for a conversion. For the same number of bits, a binary representation of a number has a larger range of values than a BCD representation. Designers must therefore ensure that the binary number value does not exceed the BCD range before using the instruction. Multiprecision representations, in which the width of the BCD number is larger than the width of the system, permit a larger number range. A binary number can also be stored as a multiprecision number. Usually, multiprecision representations are integer multiples of the width of the system. Figure 5 shows a flowchart for a single-precision conversion in a 16-bit-wide system. In this case, the binary-to-BCD conversion instruction must be executed 16 times.

In single-precision conversion, an instruction requires that the binary number be present in the Q register. The instruction uses one of the RAM registers for storing the BCD number during and after conversion; the RAM register must be cleared before use. Each instruction consists of two steps: The first adds a binary value of 3 to any BCD digit having a value of 5 or greater, as a preadjustment for a shift operation that follows. Addition is performed independently over each slice, and the carry bits from each slice are ignored. The second step shifts up the Q register and the RAM register—interconnections are shown in Fig. 6a for a 16-bit system. The 29203 executes both steps in one microcycle. The number

Taking advantage of ECL technology

Zero-detection logic exemplifies the methods used to improve the system performance of the Am29203 4-bit-slice processor. The device was analyzed in a typical system configuration to identify critical-speed paths both in the chip and in the system. This analysis was performed by modeling various important buses and pins as nodes of a network and assigning realistic delay times for the paths connected by the nodes.

A computer program identified the critical paths in the system. The 29203's ECL technology was used to shorten the delays. For example, the speed of individual ECL gates may be changed merely by varying the gate's power consumption. The more power supplied, the higher the speed, or the shorter the delay time through the gate. ECL designs have an advantage over TTL in that the speed-power curve is linear over a larger range of power. Thus, a wide variation in gate power consumption and speed is possible with ECL; with TTL, in contrast, a substantial change in power may not significantly increase gate speed.

Because the total system power is a limited resource, it must be used efficiently; more power must flow to gates in critical paths than to those in noncritical paths. Using this criterion, the critical paths in the 29203 have been optimized for the greatest possible speed with the technology. Examples of critical paths are the carry, propagation, and generation signals, which need maximum speed for interfacing with an external Am29202 when several chips are cascaded.

ECL design provides other important features that optimize logic for high speed. TTL design often requires an inverter in a signal path to obtain the desired polarity of a signal. To obtain the true and complementary forms of a signal, the TTL inverter introduces delay into one of the paths. But ECL design, through its differential amplifier circuits, automatically generates both polarities of a signal. That helps reduce gate delays in critical paths. What's more, ECL allows design techniques such as wired-OR and wired-AND, which aid in generating the OR and AND functions without consuming significant power or introducing a full gate delay. Aside from reducing delay, the technique makes more power available for speeding up other critical paths. Through this advanced technology, as well as architectural improvements, the 29203 achieves greater overall speed than other members of the 2900 family.

5

Am29705 • Am29705A • Am29707

16-Word by 4-Bit 2-Port RAM

DISTINCTIVE CHARACTERISTICS

- 16-word by 4-bit, 2-port RAM
- Two output ports, each with separate output control
- Separate four-bit latches on each output port (Am29707 has separate output control)
- Data output is noninverting with respect to data input
- Chip select and write enable inputs for ease in cascading
- Am29707 offers 20% improved cycle time over Am29705A when used with Am29203 in three address architecture
- Am29705A is a pin-for-pin replacement for the Am29705 with about a 30% speed improvement on the critical paths

RELATED PRODUCTS

Part No.	Description
Am29751A	Bipolar PROM
Am2921	One-of-Eight Decoder
Am25LS138	One-of-Four Decoder
Am25LS139	Dual One-of-Four Decoder
Am25LS157	Quad 2-by-1 MUX

GENERAL DESCRIPTION

The Am29705 is a 16-word by 4-bit, two-port RAM built using advanced Low-Power Schottky processing. This RAM features two separate output ports such that any two 4-bit words can be read from these outputs simultaneously. Each output port has a four-bit latch but a common Latch Enable (LE) input is used to control all eight latches. The device has two Write Enable ($\overline{WE}$) inputs and is designed such that the Write Enable 1 ($\overline{WE}_1$) and Latch Enable (LE) inputs can be wired together to make the operation of the RAM appear edge triggered.

The device has a fully decoded four-bit A-address field to address any of the 16 memory words for the A-output port. Likewise, a four-bit B-address input is used to simultaneously select any of the 16 words for presentation at the B-output port. New incoming data is written into the four-bit RAM word selected by the B-address. The D inputs are used to load new data into the device.

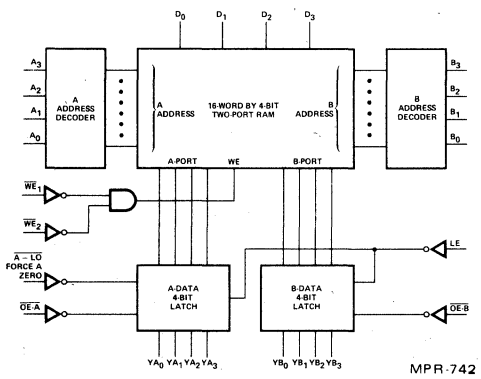
The Am29705 features three-state outputs so that several devices can be cascaded to increase the total number of memory words in the system. The A-output port is in the high-impedance state when the $\overline{OE}$-A input is HIGH. Likewise, the B-output port is in the high-impedance state when the $\overline{OE}$-B input is HIGH. Four devices can be paralleled using only one Am25LS139 decoder for output control.

The Write Enable inputs control the writing of new data into the RAM. When both Write Enable inputs are LOW, new data is written into the word selected by the B-address field. When either Write Enable input is HIGH, no data is written into the RAM.

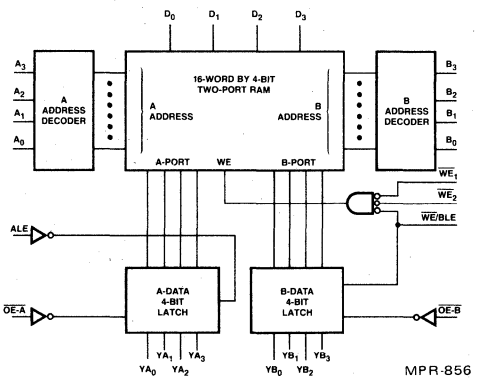
The Am29707 is an identical circuit to the Am29705, except each output port has a separate Latch Enable (LE) input. An extra write enable input ($\overline{WE}_2$) may be connected directly to the IEN of the Am29203 for improved cycle times over the Am29705A. The $\overline{WE}$/BLE input can then be connected directly to system clock.

The Am29705A is a plug-in replacement for the Am29705, but is about 30% faster. The Am29705A and Am29707 feature AMD's advanced ion-implanted micro-oxide (IMOX™) processing.

Am29705 • Am29705A BLOCK DIAGRAM



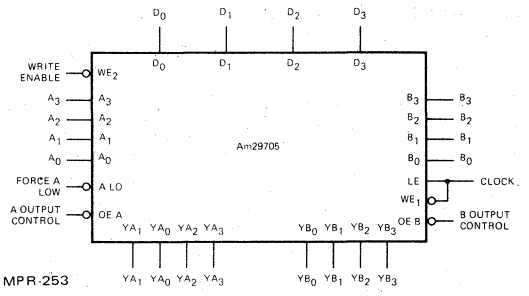
Am29707 BLOCK DIAGRAM



IMOX is a trademark of Advanced Micro Devices, Inc.

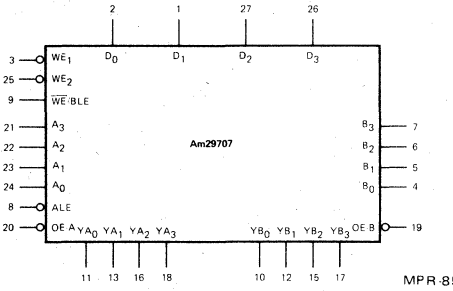
LOGIC SYMBOLS

Am29705 • Am29705A



MPR-253

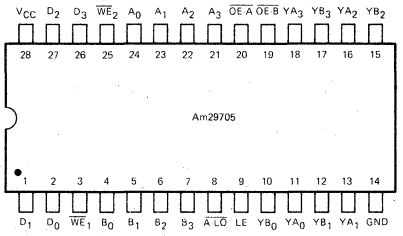
Am29707



MPR-850

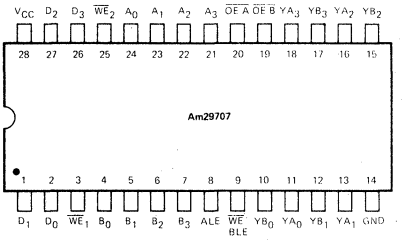
CONNECTION DIAGRAMS – Top Views

Am29705 • Am29705A



MPR-252

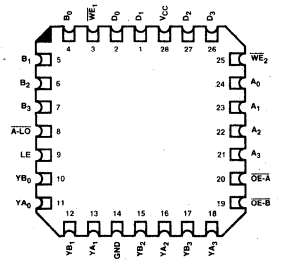
Am29707



MPR-851

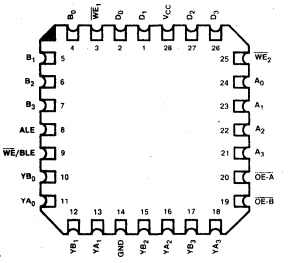
Leadless Chip Carriers

L-28-1



MPR-852

L-28-1



MPR-853

Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Am29707 Order Number	Am29705A Order Number	Am29705 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM29707PC	AM29705APC	AM29705PC	P-28	C	C-1
AM29707DC	AM29705ADC	AM29705DC	D-28	C	C-1
AM29707DC-B	AM29705ADC-B	AM29705DC-B	D-28	C	B-2 (Note 4)
AM29707DM	AM29705ADM	AM29705DM	D-28	M	C-3
AM29707DM-B	AM29705ADM-B	AM29705DM-B	D-28	M	B-3
AM29707FM	AM29705AFM	AM29705FM	F-28-1	M	C-3
AM29707FM-B	AM29705AFM-B	AM29705FM-B	F-28-1	M	B-3
AM29707LC	AM29705ALC	AM29705LC	L-28	C	C-1
AM29707LM	AM29705ALM	AM29705LM	L-28	M	C-3
AM29707LM-B	AM29705ALM-B	AM29705LM-B	L-28	M	B-3
AM29707XC	AM29705AXC	AM29705XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM29707XM	AM29705AXM	AM29705XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

PIN DEFINITIONS

D_0-D_3 **Data Inputs**
New data is written into the RAM through these inputs.

A_0-A_3 **The A-Address Inputs**
The four-bit field presented at the A inputs selects one of the 16 memory words for presentation to the A-Data Latch.

B_0-B_3 **The B-Address Inputs**
The four bit field presented at the B inputs selects one of the 16 memory words for presentation to the B-Data Latch. The B address field also selects the word into which new data is written.

YA_0-YA_3 **The Four A-Data Latch Outputs**

YB_0-YB_3 **The Four B-Data Latch Outputs**

$\overline{WE}_1$, $\overline{WE}_2$ **Write Enables**
When both Write Enables are LOW, new data is written into the word selected by the B-address field. If either Write Enable input is HIGH, no new data can be written into the memory.

$\overline{OE}$-A **A-Port Output Enable**
When $\overline{OE}$-A is LOW, data in the A-Data Latch is present at the YA_i outputs. If $\overline{OE}$-A is HIGH, the YA_i outputs are in the high-impedance (off) state.

$\overline{OE}$-B **B-Port Output Enable**
When $\overline{OE}$-B is LOW, data in the B-Data Latch is present at the YB_i outputs. When $\overline{OE}$-B is HIGH the YB_i outputs are in the high-impedance (off) state.

LE **Latch Enable**
The LE input controls the latches for both the RAM A-output port and RAM B-output port. When the LE input is HIGH, the latches are open (transparent) and data from the RAM, as selected by the A and B address fields, is present at the outputs. When LE is LOW, the latches are closed and they retain the last data read from the RAM independent of the current A and B address field inputs. (Am29705A • Am29705A only.)

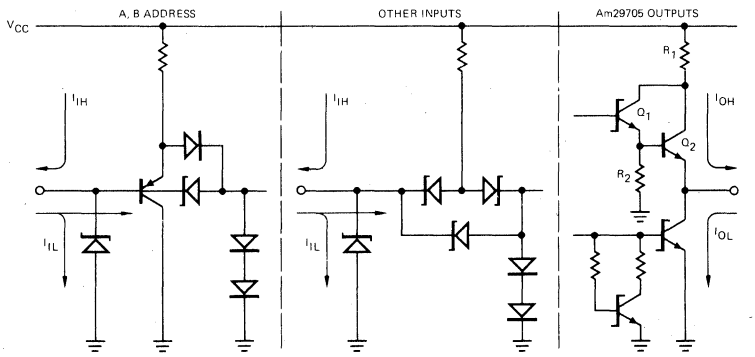
$\overline{A\text{-}LO}$ **Force A Zero**
This input is used to force the outputs of the A-port latches LOW independent of the Latch Enable input or A-address field select inputs. Thus, the A-output bus can be forced LOW using this control signal. When the $\overline{A\text{-}LO}$ input is HIGH, the A latches operate in their normal fashion. Once the A latches are forced LOW, they remain LOW independent of the $\overline{A\text{-}LO}$ input if the latches are closed. (Am29705 • Am29705A only.)

ALE **A-Output Port Latch Enable**
When ALE is HIGH, the A latch is open (transparent) and data from the RAM, as selected by the A address field, is present at the A output. When ALE is LOW, the A latch is closed and retains the last data read from the RAM independent of the current A address field input. (Am29707 only.)

$\overline{WE}$/BLE **Write Enable/B-Output Port Latch Enable**
When $\overline{WE}$/BLE is LOW together with $\overline{WE}_1$ and $\overline{WE}_2$, new data is written into the word selected by the B address field. When $\overline{WE}$/BLE or any Write Enable input is HIGH, no data is written into the RAM.

$\overline{WE}$/BLE also controls the B output port. When $\overline{WE}$/BLE is HIGH, the B latch is open (transparent), and when this input is LOW, the B latch is closed (Am29707 only).

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

MPR-254

FUNCTION TABLES

Am29705 • Am29705A
WRITE CONTROL

$\overline{WE_1}$	$\overline{WE_2}$	Function	RAM Outputs at Latch Inputs	
			A-Port	B-Port
L	L	Write D into B	A data (A = B)	Input Data
L	L	Write D into B	(A = B) Input Data	Input Data
X	H	No Write	A Data	B Data
H	X	No Write	A Data	B Data

H = HIGH L = LOW X = Don't Care

YA READ

Inputs			YA Output	Function
$\overline{OE\text{-}A}$	$\overline{A\text{-}LO}$	LE		
H	X	X	Z	High Impedance
L	L	X	L	Force YA LOW
L	H	H	A-Port RAM Data	Latches Transparent
L	H	L	NC	Latches Retain Data

H = HIGH L = LOW X = Don't Care Z = High Impedance NC = No Change

YB READ

Inputs		YB Output	Function
$\overline{OE\text{-}B}$	LE		
H	X	Z	High Impedance
L	H	B-Port RAM Data	Latches Transparent
L	L	NC	Latches Retain Data

H = HIGH L = LOW X = Don't Care Z = High Impedance NC = No change

Am29707
WRITE CONTROL

$\overline{WE_1}$	$\overline{WE_2}$	$\overline{WE}$/BLE	Function	RAM Outputs at Latch Inputs	
				A-Port	B-Port
L	L	L	Write D into B	A Data (A = B)	Not Specified
X	X	H	No Write	A Data	B Data
X	H	X	No Write	A Data	B Data
H	X	X	No Write	A Data	B Data

H = HIGH L = LOW X = Don't Care

YA READ

Inputs		YA Output	Function
$\overline{OE\text{-}A}$	ALE		
H	X	Z	High Impedance
L	H	A-Port RAM Data	Latches Transparent
L	L	NC	Latches Retain Data

H = HIGH L = LOW D = Don't Care Z = High Impedance NC = No Change

YB READ

Inputs		YB Output	Function
$\overline{OE\text{-}B}$	$\overline{WE}$/BLE		
H	X	Z	High Impedance
L	H	B-Port RAM Data	Latches Transparent
L	L	NC	Latches Retain Data

H = HIGH L = LOW D = Don't Care Z = High Impedance NC = No Change

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
D_1	1	1	–	–
D_0	2	1	–	–
$\overline{WE}_1$	3	1	–	–
B_0	4	0.55	–	–
B_1	5	0.55	–	–
B_2	6	0.55	–	–
B_3	7	0.55	–	–
$\overline{A-LO}$ (29705 Only)	8	1	–	–
LE (29705 Only)	9	1	–	–
ALE (29707 Only)	8	1	–	–
$\overline{WE}$/BLE (29707 Only)	9	1	–	–
YB_0	10	–	100/200	33
YA_0	11	–	100/200	33
YB_1	12	–	100/200	33
YA_1	13	–	100/200	33
GND	14	–	–	–
YB_2	15	–	100/200	33
YA_2	16	–	100/200	33
YB_3	17	–	100/200	33
YA_3	18	–	100/200	33
$\overline{OE-B}$	19	1	–	–
$\overline{OE-A}$	20	1	–	–
A_3	21	0.55	–	–
A_2	22	0.55	–	–
A_1	23	0.55	–	–
A_0	24	0.55	–	–
$\overline{WE}_2$	25	1	–	–
D_3	26	1	–	–
D_2	27	1	–	–
V_{CC}	28	–	–	–

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

OPERATING RANGE

Part Number Suffix	V_{CC}	Temperature
PC, PC-B DC, DC-B XC	4.75 to 5.25V	T_A = 0 to +70°C
DM, DM-B FM, FM-B XM	4.5 to 5.5V	T_A = −55 to +125°C

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

5

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −2.0mA	2.4			Volts
			COM'L, I_{OH} = −4.0mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
			I_{OL} = 12mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	A_i, B_i			−0.25	mA
			$\overline{OE\text{-}A}$, $\overline{OE\text{-}B}$			−0.54	
			Others			−0.36	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				20	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				0.1	mA
I_O	Off State (High Impedance) Output Current	V_{CC} = MAX. V_{IN} = V_{IH} or V_{IL}	V_O = 2.7V			20	µA
			V_O = 0.4V			−20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−30		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Worst case I_{CC} is at minimum temperature) (Note 4)	T_A = 25°C		121	195	mA
			T_A = 0°C to +70°C			210	
			T_A = 70°C			170	
			T_C = −55°C to +125°C			210	
			T_C = 125°C			150	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All inputs grounded except $\overline{OE\text{-}A}$ and $\overline{OE\text{-}B}$ =2.4V.

Am29705A SWITCHING CHARACTERISTICS

(Output levels = 0 and 3.0V, transitions measured at 1.5V)
($R_L = 390\Omega$, $C_L = 50pF$)

Parameters	From	To	Test Conditions	$T_A = 0$ to $+70°C$ $V_{CC} = 4.75$ to $5.25V$	$T_A = -55$ to $+125°C$ $V_{CC} = 4.5$ to $5.5V$
Access Time	A Address Stable or B Address Stable	YA Stable or YB Stable	LE = HIGH	28	30
Turn-On Time	$\overline{OE}$-A or $\overline{OE}$-B LOW	YA or YB Stable		20	20
Turn-Off Time	$\overline{OE}$-A or $\overline{OE}$-B HIGH	YA or YB Off		20	20
Reset Time	$\overline{A\text{-}LO}$ LOW	YA LOW		20	25
Enable Time	LE HIGH	YA and YB Stable		20	25
Transparency	$\overline{WE}$ or $\overline{WE_2}$	YA or YB		35	40
	D	YA or YB		35	40

MINIMUM SETUP AND HOLD TIME (in ns)

Parameters	From	To	Test Conditions	$T_A = 0$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ Max	$T_A = -55$ to $+125°C$ $V_{CC} = 4.5$ to $5.5V$
Data Setup Time	D Stable	Either $\overline{WE}$ HIGH		12	15
Data Hold Time	Either $\overline{WE}$ HIGH	D Changing		3	0
Address Setup Time	B Stable	Both $\overline{WE}$ LOW		0	3
Address Hold Time	Either $\overline{WE}$ HIGH	B Changing		3	0
Latch Close Before Write Begins	LE LOW	$\overline{WE_1}$ LOW	$\overline{WE_2}$ LOW	0	0
	LE LOW	$\overline{WE_2}$ LOW	$\overline{WE_1}$ LOW	0	0
Address Setup Before Latch Closes	A or B Stable	LE LOW		15	20

MINIMUM PULSE WIDTHS

Parameters	Input	Pulse	Test Conditions	$T_A = 0$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ Max	$T_A = -55$ to $+125°C$ $V_{CC} = 4.5$ to $5.5V$
Write Pulse Width	$\overline{WE_1}$	HIGH-LOW-HIGH	$\overline{WE_2}$ LOW	20	20
	$\overline{WE_2}$	HIGH-LOW-HIGH	$\overline{WE_1}$ LOW	20	20
A Latch Reset Pulse	$\overline{A\text{-}LO}$	HIGH-LOW-HIGH		15	15
Latch Data Capture	LE	LOW-HIGH-LOW		15	15

Note: The Am29705A meet or exceeds all of the specifications of the Am29705.

Am29705 SWITCHING CHARACTERISTICS

(Output levels = 0 and 3.0V, transitions measured at 1.5V)
(R_L = 390Ω, C_L = 50pF)

Parameters	From	To	Test Conditions	T_A = 0 to +70°C V_{CC} = 4.75 to 5.25V	T_A = −55 to +125°C V_{CC} = 4.5 to 5.5V
Access Time	A Address Stable or B Address Stable	YA Stable or YB Stable	LE = HIGH	53	58
Turn-On Time	$\overline{OE}$-A or $\overline{OE}$-B LOW	YA or YB Stable		30	30
Turn-Off Time	$\overline{OE}$-A or $\overline{OE}$-B HIGH	YA or YB Off		20	20
Reset Time	A-$\overline{LO}$ LOW	YA LOW		35	35
Enable Time	LE HIGH	YA and YB Stable		32	32

MINIMUM SETUP AND HOLD TIMES (in ns)

Parameters	From	To	Test Conditions	T_A = 0 to +70°C V_{CC} = 5.0V ±5% Max	T_A = −55 to +125°C V_{CC} = 4.5 to 5.5V
Data Setup Time	D Stable	Either $\overline{WE}$ HIGH		20	25
Data Hold Time	Either $\overline{WE}$ HIGH	D Changing		3	5
Address Setup Time	B Stable	Both $\overline{WE}$ LOW		5	5
Address Hold Time	Either $\overline{WE}$ HIGH	B Changing		0	0
Latch Close Before Write Begins	LE LOW	$\overline{WE_1}$ LOW	$\overline{WE_2}$ LOW	0	0
	LE LOW	$\overline{WE_2}$ LOW	$\overline{WE_1}$ LOW	0	0
Address Setup Before Latch Closes	A or B Stable	LE LOW		45	50

MINIMUM PULSE WIDTHS

Parameters	Input	Pulse	Test Conditions	T_A = 0 to +70°C V_{CC} = 5.0V ±5% Max	T_A = −55 to +125°C V_{CC} = 4.5 to 5.5V
Write Pulse Width	$\overline{WE_1}$	HIGH-LOW-HIGH	$\overline{WE_2}$ LOW	25	25
	$\overline{WE_2}$	HIGH-LOW-HIGH	$\overline{WE_1}$ LOW	20	20
A Latch Reset Pulse	A-$\overline{LO}$	HIGH-LOW-HIGH		20	20
Latch Data Capture	LE	LOW-HIGH-LOW		20	25

Am29707 SWITCHING CHARACTERISTICS

(Output levels = 0 and 3.0V, transitions measured at 1.5V)
(R_L = 390Ω, C_L = 50pF)

Parameters	From	To	Conditions	T_A = 25°C V_{CC} = 4.75 to 5.25V
Access Time	A Address Stable or B Address Stable	YA Stable or YB Stable	LE = HIGH	13
Turn-On Time	$\overline{OE}$-A or $\overline{OE}$-B LOW	YA or YB Stable		6
Turn-Off Time	$\overline{OE}$-A or $\overline{OE}$-B HIGH	YA or YB Off		13
Reset Time	$\overline{A\text{-}LO}$ LOW	YA LOW		8
Enable Time	LE HIGH	YA and YB Stable		8
Transparency	$\overline{WE}$ or $\overline{WE}_2$	YA or YB		12
	D	YA or YB		14

Minimum Set-up and Hold Times (in ns)

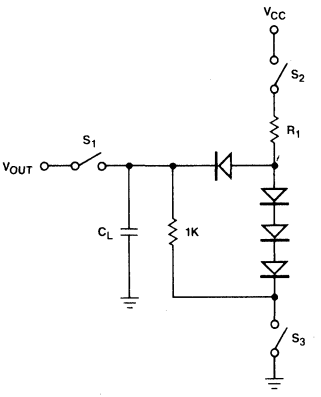
Parameters	From	To	Conditions	T_A = 25°C V_{CC} = 5.0V ±5% Max
Data Set-Up Time	D Stable	Either $\overline{WE}$ HIGH		2
Data Hold Time	Either $\overline{WE}$ HIGH	D Changing		4
Address Set-Up Time	B Stable	Both $\overline{WE}$ LOW		−1
Address Hold Time	Either $\overline{WE}$ HIGH	B Changing		8
Latch Close Before Write Begins	LE LOW	$\overline{WE}_1$ LOW	$\overline{WE}_2$ LOW	0
	LE LOW	$\overline{WE}_2$ LOW	$\overline{WE}_1$ LOW	0
Address Set-Up Before Latch Closes	A or B Stable	LE LOW		7

Minimum Pulse Widths

Parameters	Input	Pulse	Conditions	T_A = 0 to +70°C V_{CC} = 5.0V ±5% Max
Write Pulse Width	$\overline{WE}_1$	HIGH-LOW-HIGH	$\overline{WE}_2$ LOW	25
	$\overline{WE}_2$	HIGH-LOW-HIGH	$\overline{WE}_1$ LOW	20
A Latch Reset Pulse	$\overline{A\text{-}LO}$	HIGH-LOW-HIGH		20
Latch Data Capture	LE	LOW-HIGH-LOW		20

TEST OUTPUT LOAD CONFIGURATIONS FOR Am29705

A. THREE-STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

MPR-854

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all A.C. tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5pF for output disable tests.

TEST OUTPUT LOADS FOR Am29705

Pin # (DIP)	Pin Label	Test Circuit	R_1	R_2
–	YA_{0-3}	A	312	1K
–	YB_{0-3}	A	312	1K

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5–8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

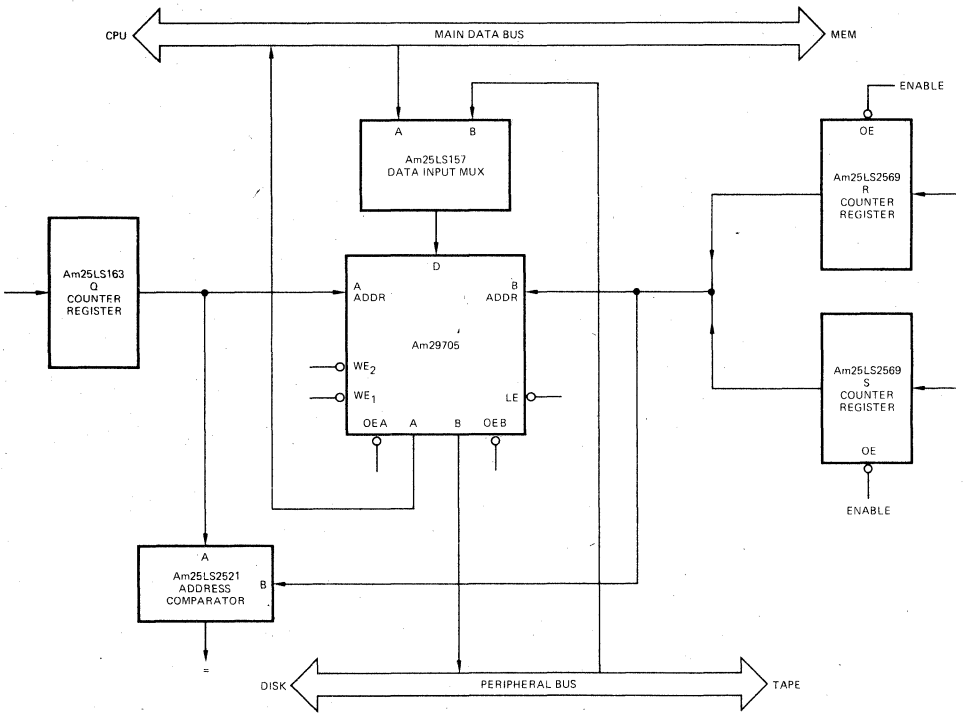
USING THE Am29705 AND Am29707

The Am2903 and Am29203 each contain only 16 scratchpad registers plus the Q register. For applications which require more than 17 registers, the register set of the Am2903 and Am29203 can be easily expanded.

- Use the Am29705 with the Am2903
- Use the Am29707 with the Am29203

All references to the Am29705 include the Am29705A.

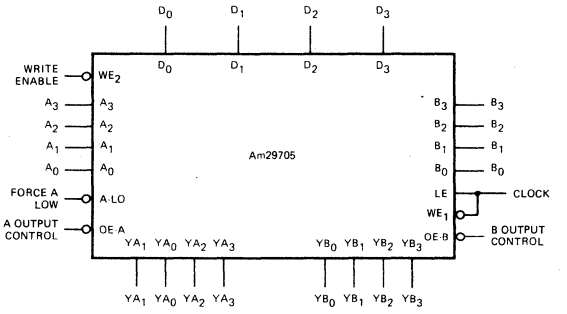
For further applications information on using the Am29705 with the Am2903, see Chapter lil of *Bit Slice Microprocessor Design*, Mick and Brick, McGraw-Hill Publications.



MPR-259

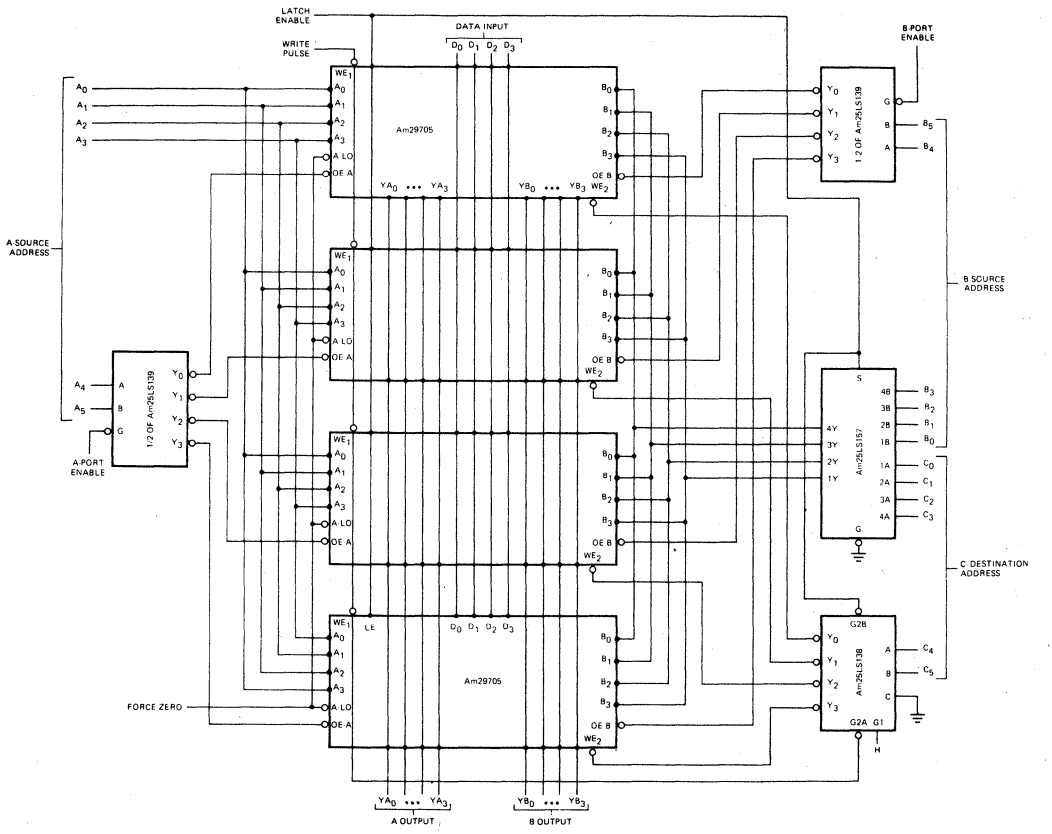
The Am29705 as a two-way interface buffer. Data may be passed between the main data bus and the peripheral data bus under I/O control. The two-port RAM allows data to be written into buffer storage from a peripheral device, using the B address port and the S counter register, while it is being read into main memory, using the A address port and the Q counter register. This simultaneous read/write capability facilitates DMA transfers because the CPU can ignore write requests from the peripheral device. Data output from CPU to the peripheral device is handled by sequential write and read operations. Data is written into buffer storage from the CPU, using the B address port and the R counter register. It is read onto the peripheral device using the B address port and either the R register, for single word transfers, or the S register, for block transfers.

APPLICATIONS (Cont.)



MPR-257

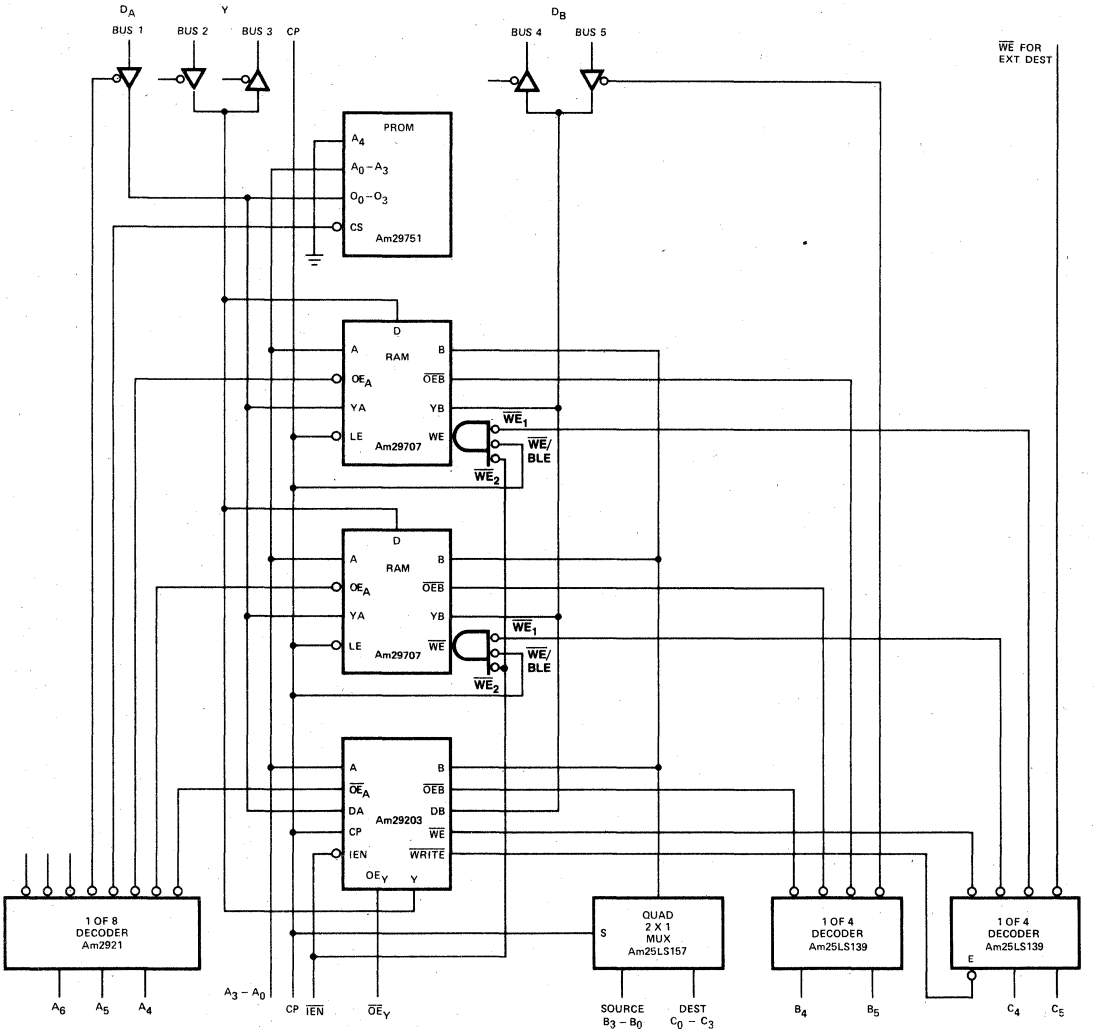
A 16-word by 4-bit two-port RAM with LE and WE_1 connected to make the device appear edge triggered. WE_1 and WE_2 are logically identical but are electrically slightly different. For synchronous operation without possibility of race, WE_1 should be connected to LE.



MPR-258

A 64-word by 4-bit three address memory. Data is read from the A address to the YA outputs and from the B address to the YB outputs while the latch enable is HIGH. When the latch enable goes LOW, the YA and YB data is held in the internal latches, and the RAM B address is switched to the C-destination address lines. A write pulse will then deposit the input data into the location selected by the C address.

APPLICATIONS (Cont.)



Am29203 EXPANDED MEMORY

A 48-word by 4-bit expanded memory for the Am29203 using the Am29707. The Am29751 PROM serves as a constant store.

Am29803A

16-Way Branch Control Unit

DISTINCTIVE CHARACTERISTICS

- 16 separate instructions – 2, 4, 8 or 16-way branch in one microprogram execution cycle
- Four individual test inputs
- Four individual outputs for driving the four OR inputs on the Am2909A Microprogram Sequencer
- Provides maximum branch capability in a microprogram control unit using the Am2909
- Advanced Low-Power Schottky processing

FUNCTIONAL DESCRIPTION

The Am29803A is a Low-Power Schottky processed device that provides 16-way branch control when used in conjunction with the Am2909A Microprogram Sequencer.

The device features 16 instructions that provide all combinations of simultaneous testing of four different inputs. The device has four outputs that are used to drive the four OR inputs of the Am2909A Microprogram Sequencer.

The "zero" instruction inhibits the testing of any of the four test (T) inputs. The remaining 15 instructions are used to test combinations of 1, 2, 3 or 4 of the T inputs simultaneously. If one T input is being tested, the Am29803A will select one of two possible addresses. If two T inputs are being tested, the device will select one of four possible addresses. If three T inputs are being tested, the device will select one of eight possible addresses. If all four T inputs are being tested, the device will select one of sixteen addresses as the field used to drive the OR inputs of the Am2909A.

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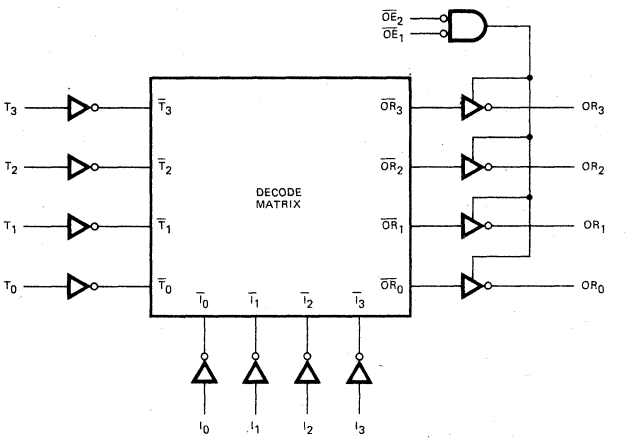
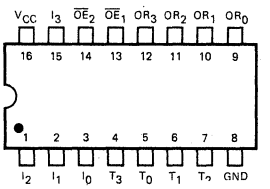
LOGIC DIAGRAM



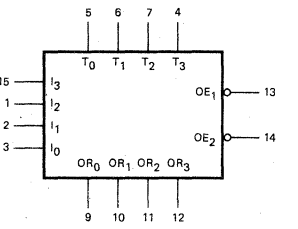
CONNECTION DIAGRAM – Top View
D16, P16



F-16 pin configuration identical to D-16, P16.

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 16

GND = Pin 8

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	Am29803ADC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	Am29803ADM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V		−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			25	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		95	130	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX., $V_{\overline{CS1}}$ = 2.4V; V_O = 4.5V			40	μA
		V_{CC} = MAX., $V_{\overline{CS1}}$ = 2.4V; V_O = 2.4V			40	μA
		V_{CC} = MAX., $V_{\overline{CS1}}$ = 2.4V; V_O = 0.4V			−40	μA
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz (Note 3)		4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz (Note 3)		8		pF

Note 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C

2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

3. These parameters are not 100% tested, but are periodically sampled.

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH} / t_{PHL}	I_i to OR_i	C_L = 15pF, R_L = 2.0kΩ		25	35	ns
t_{PLH} / t_{PHL}	T_i to OR_i	C_L = 15pF, R_L = 2.0kΩ		25	35	ns
t_{ZH} / t_{ZL}	$\overline{OE}_i$ to OR_i	C_L = 15pF, R_L = 2.0kΩ		15	18	ns
t_{HZ} / t_{LZ}	$\overline{OE}_i$ to OR_i	C_L = 5.0pF, R_L = 2.0kΩ		15	18	ns

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions	COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	COM'L Max.	MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	MIL Max.	Units
t_{PLH} / t_{PHL}	I_i to OR_i	C_L = 15pF, R_L = 2.0kΩ		45		60	ns
t_{PLH} / t_{PHL}	T_i to OR_i	C_L = 15pF, R_L = 2.0kΩ		45		60	ns
t_{ZH} / t_{ZL}	$\overline{OE}_i$ to OR_i	C_L = 15pF, R_L = 2.0kΩ		30		30	ns
t_{HZ} / t_{LZ}	$\overline{OE}_i$ to OR_i	C_L = 15pF, R_L = 2.0kΩ		20		20	ns

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DEFINITION OF FUNCTIONAL TERMS

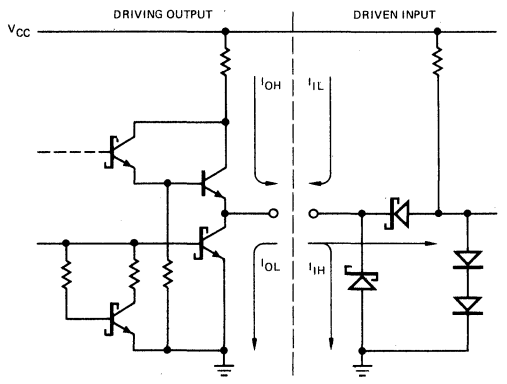
I_0, I_1, I_2, I_3 — The four instruction inputs to the device

T_0, T_1, T_2, T_3 — The four test inputs for the device

OR_0, OR_1, OR_2, OR_3 — The four outputs of the device that are connected to the four OR inputs of the Am2909

$\overline{OE}_1, \overline{OE}_2$ — Output Enable. When either $\overline{OE}$ input is HIGH, the OR_i outputs are in the high impedance state. When both the $\overline{OE}_1$ and $\overline{OE}_2$ inputs are LOW, the OR outputs are enabled and the selected data will be present.

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

MPR-312

GUARANTEED LOADING RULES OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

Pin No.'s	Input/Output	Input Load	Output HIGH	Output LOW MIL	Output LOW COM'L
1	I_2	0.5	–	–	–
2	I_1	0.5	–	–	–
3	I_0	0.5	–	–	–
4	T_3	0.5	–	–	–
5	T_0	0.5	–	–	–
6	T_1	0.5	–	–	–
7	T_2	0.5	–	–	–
8	GND	–	–	–	–
9	OR_0	–	100	44	44
10	OR_1	–	100	44	44
11	OR_2	–	100	44	44
12	OR_3	–	100	44	44
13	$\overline{OE}_1$	0.5	–	–	–
14	$\overline{OE}_2$	0.5	–	–	–
15	I_3	0.5	–	–	–
16	V_{CC}	–	–	–	–

FUNCTION TABLE

Function	I_3	I_2	I_1	I_0	T_3	T_2	T_1	T_0	OR_3	OR_2	OR_1	OR_0
No Test	L	L	L	L	X	X	X	X	L	L	L	L
Test T_0	L	L	L	H	X X	X X	X X	L H	L L	L L	L L	L H
Test T_1	L	L	H	L	X X	X X	L H	X X	L L	L L	L L	L H
Test T_0 & T_1	L	L	H	H	X X X X	X X X X	L L H H	L H L H	L L L L	L L L L	L L H H	L H L H
Test T_2	L	H	L	L	X X	L H	X X	X X	L L	L L	L L	L H
Test T_0 & T_2	L	H	L	H	X X X X	L L H H	X X X X	L H L H	L L L L	L L L L	L L H H	L H L H
Test T_1 & T_2	L	H	H	L	X X X X	L L H H	L H L H	X X X X	L L L L	L L L L	L L H H	L H L H
Test T_0, T_1 & T_2	L	H	H	H	X X X X X X X X	L L L L H H H H	L L H H L L H H	L H L H L H L H	L L L L L L L L	L L L L H H H H	L L H H L L H H	L H L H L H L H
Test T_3	H	L	L	L	L H	X X	X X	X X	L L	L L	L L	L H
Test T_0 & T_3	H	L	L	H	L L H H	X X X X	X X X X	L H L H	L L L L	L L L L	L L H H	L H L H
Test T_1 & T_3	H	L	H	L	L L H H	X X X X	L H L H	X X X X	L L L L	L L L L	L L H H	L H L H
Test T_0, T_1 & T_3	H	L	H	H	L L L L H H H H	X X X X X X X X	L L H H L L H H	L H L H L H L H	L L L L L L L L	L L L L H H H H	L L H H L L H H	L H L H L H L H
Test T_2 & T_3	H	H	L	L	L L H H	L H L H	X X X X	X X X X	L L L L	L L L L	L L H H	L H L H
Test T_0, T_2 & T_3	H	H	L	H	L L L L H H H H	L L H H L L H H	X X X X X X X X	L H L H L H L H	L L L L L L L L	L L L L H H H H	L L H H L L H H	L H L H L H L H
Test T_1, T_2 & T_3	H	H	H	L	L L L L H H H H	L L H H L L H H	L H L H L H L H	X X X X X X X X	L L L L L L L L	L L L L H H H H	L L H H L L H H	L H L H L H L H
Test T_0, T_1, T_2 & T_3	H	H	H	H	L L L L L L L L H H H H H H H H	L L L L H H H H L L L L H H H H	L L H H L L H H L L H H L L H H	L H L H L H L H L H L H L H L H	L L L L L L L L H H H H H H H H	L L L L H H H H L L L L H H H H	L L H H L L H H L L H H L L H H	L H L H L H L H L H L H L H L H

L = LOW, H = HIGH, X = Don't care

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM29803APC	P-16	C	C-1
AM29803ADC	D-16	C	C-1
AM29803ADC-B	D-16	C	B-1
AM29803ADM	D-16	M	C-3
AM29803ADM-B	D-16	M	B-3
AM29803AFM	F-16	M	C-3
AM29803AFM-B	F-16	M	B-3

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

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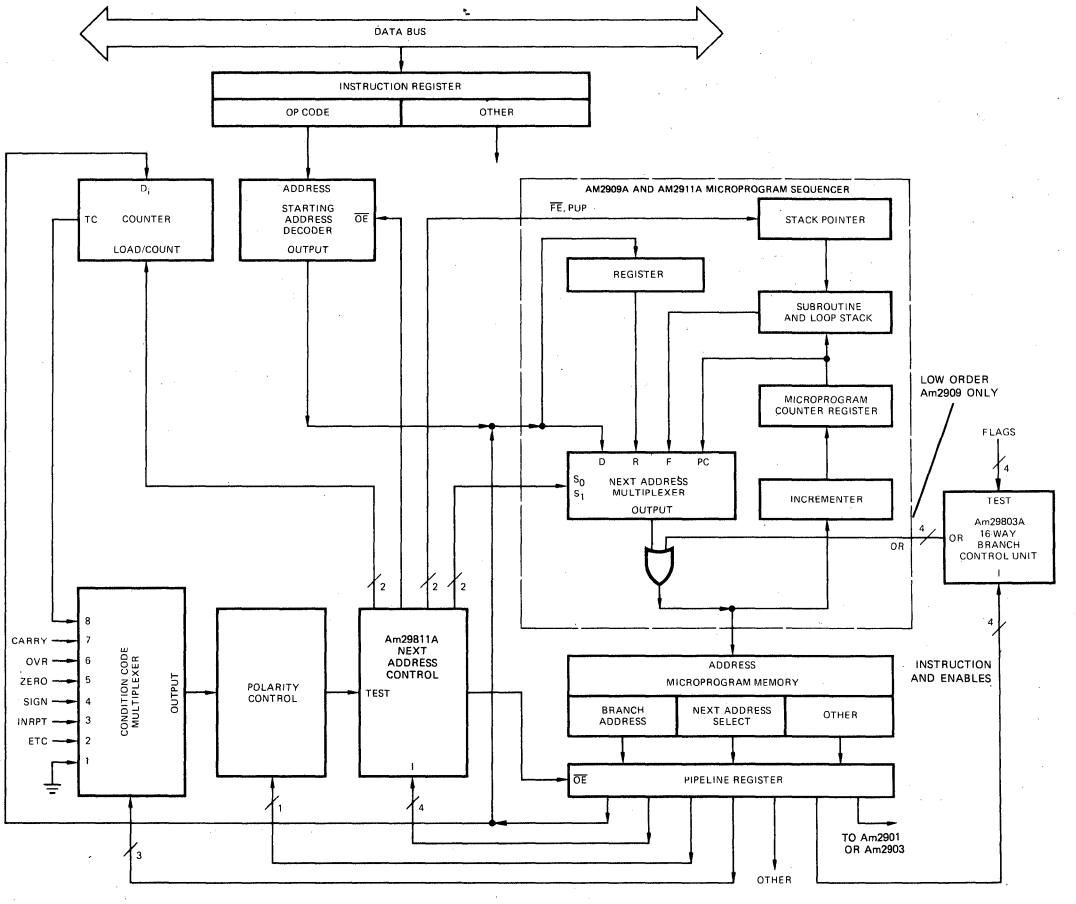
APPLICATION



A typical computer control unit using the Am2909, Am2911, Am29803A and Am29811A. Note that the least significant microprogram sequencer is an Am2909 and the more significant sequencers are Am2911's.

MPR-313

Am29811A

Next Address Control Unit

DISTINCTIVE CHARACTERISTICS

- Next address control unit for the Am2911A Microprogram Sequencer
- 16 next address instructions
- Test input for conditional instructions
- Separate outputs to control the Am2911A, an independent event counter, and a mapping PROM/branch address interface
- Advanced Low-Power Schottky technology

FUNCTIONAL CHARACTERISTICS

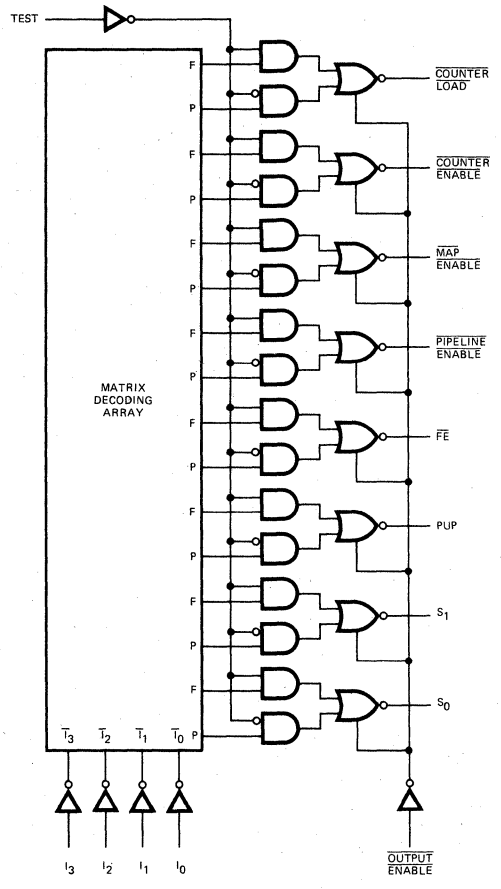
The Am29811A is a Low-Power Schottky device designed specifically for next address control of the Am2911A Microprogram Sequencer. The device contains all outputs required to control a high-performance computer control unit or a structured state machine design using microprogramming techniques.

Sixteen instructions are available by using a four-bit instruction field I_{0-3}. In addition, a test input is available such that conditional instructions can be performed based on a condition code test input.

The full instruction set consists of such functions as conditional jumps, conditional jump-to-subroutine, conditional return-from-subroutine, conditional repeat loops, conditional branch to starting address, and so forth.

One Am29811A can be used to control any number of Am2911A Microprogram Sequencers. The Am2911A Sequencer is a four-bit slice itself. Thus, one Am29811A Next Address Control Unit and three Am2911A Microprogram Sequencers can be used to build a powerful, microprogram sequencer capable of controlling 4k words of microprogram memory.

LOGIC DIAGRAM



P = Pass
F = Fail

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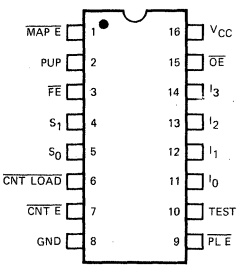
CONNECTION DIAGRAM
Top View

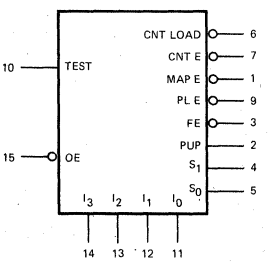
P16, D16



F-16 pin configuration identical to D-16, P-16.
Note: Pin 1 is marked for orientation.

MPR-315

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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MAXIMUM RATINGS (Above which the useful life may be impaired)	
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	Am29811ADC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	Am29811ADM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

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ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V		−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			25	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		90	115	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; V_O = 4.5V			40	μA
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; V_O = 2.4V			40	
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz (Note 3)		4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz (Note 3)		8		

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but periodically sampled.

Am29811A
SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH} t_{PHL}	I_i to Any Output	C_L = 15pF R_L = 2.0kΩ		25	35	ns
t_{PLH} t_{PHL}	Test to Any Output			25	35	ns
t_{ZH} t_{ZL}	$\overline{OE}$ to Any Output			15	20	ns
t_{HZ} t_{LZ}	$\overline{OE}$ to Any Output	C_L = 5.0pF R_L = 2.0kΩ		15	20	ns

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions	COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	COM'L Max.	MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	MIL Max.	Units
t_{PLH} t_{PHL}	I_i to Any Output	C_L = 15pF R_L = 2.0kΩ		40		50	ns
t_{PLH} t_{PHL}	Test to Any Output			40		50	ns
t_{ZH} t_{ZL}	$\overline{OE}$ to Any Output			25		30	ns
t_{HZ} t_{LZ}	$\overline{OE}$ to Any Output			25		30	ns

DEFINITION OF FUNCTIONAL TERMS

I_0, I_1, I_2, I_3 The four instruction inputs to the Am29811A.

TEST The condition code input to the device. When the test input is LOW, the device assumes the test has failed. When the test input is HIGH, the device assumes the condition code required has been met; the test has passed.

$\overline{\text{Counter Load}}$ This output is used to drive the parallel load input of an Am25LS169 up/down counter.

$\overline{\text{Counter Enable}}$ This output is used to drive the counter enable input of an Am25LS169 up/down counter.

$\overline{\text{Map Enable}}$ This output is used to control the three-state outputs of the mapping PROM or PLA used to provide the initial starting address for each machine instruction.

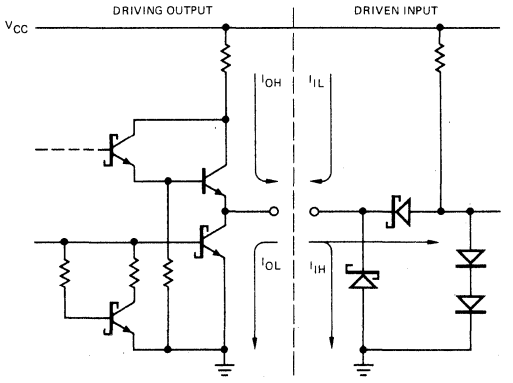
$\overline{\text{Pipeline Enable}}$ This output is used to control the three-state output of the pipeline register (Am2918) containing the branch address for the computer control unit.

$\overline{\text{FE}}$ File Enable This output is used to drive the file enable input of the Am2911. When the file enable output is LOW, a stack operation will take place.

PUP Push/Pop. The PUP output is used to drive the push/pop input of the Am2911 Microprogram Sequencer. When the PUP output is HIGH, a push will take place when the file is enabled. When the PUP output is LOW, a pop will take place when the file is enabled.

S_0, S_1 These two outputs are used to drive the S_0 and S_1 inputs to the Am2911 Microprogram Sequencer. These outputs control whether the direct input, the register, the microprogram counter, or the stack is selected as the source of the next address for the microprogram memory.

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

MPR-317

GUARANTEED LOADING RULES OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

Pin No.'s	Input/Output	Input Load	Output HIGH	Output LOW MIL	Output LOW COM'L
1	$\overline{\text{MAP E}}$	–	100	44	44
2	PUP	–	100	44	44
3	$\overline{\text{FE}}$	–	100	44	44
4	S_1	–	100	44	44
5	S_0	–	100	44	44
6	$\overline{\text{CNT LOAD}}$	–	100	44	44
7	$\overline{\text{CNT E}}$	–	100	44	44
8	GND	–	–	–	–
9	$\overline{\text{PL E}}$	–	100	44	44
10	TEST	0.5	–	–	–
11	I_0	0.5	–	–	–
12	I_1	0.5	–	–	–
13	I_2	0.5	–	–	–
14	I_3	0.5	–	–	–
15	$\overline{\text{OE}}$	–	100	44	44
16	V_{CC}	–	–	–	–

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INSTRUCTION TABLE

MNEMONIC	I_3 I_2 I_1 I_0	INSTRUCTION
JZ	L L L L	Jump to Address Zero
CJS	L L L H	Conditional Jump-to-Subroutine with Jump Address in Pipeline Register.
JMAP	L L H L	Jump to Address at Mapping PROM Output.
CJP	L L H H	Conditional Jump to Address in Pipeline Register
PUSH	L H L L	Push Stack and Conditionally Load Counter
JSRP	L H L H	Jump-to-Subroutine with Starting Address Conditionally Selected from Am2911 R-Register or Pipeline Register.
CJV	L H H L	Conditional Jump to Vector Address.
JRP	L H H H	Jump to Address Conditionally Selected from Am2911 R-Register or Pipeline Register.
RFCT	H L L L	Repeat Loop if Counter is not Equal to Zero.
RPCT	H L L H	Repeat Pipeline Address if Counter is not Equal to Zero.
CRTN	H L H L	Conditional Return-from-Subroutine.
CJPP	H L H H	Conditional Jump to Pipeline Address and Pop Stack.
LDCT	H H L L	Load Counter and Continue.
LOOP	H H L H	Test End of Loop.
CONT	H H H L	Continue to Next Address.
JP	H H H H	Jump to Pipeline Register Address.

Am29811A FUNCTION TABLE

MNEMONIC	INPUTS				OUTPUTS				
	INSTRUCTION I_3 I_2 I_1 I_0	FUNCTION	TEST INPUT	NEXT ADDR SOURCE	FILE	COUNTER	MAP-E	PL-E
JZ	L L L L	JUMP ZERO	X	D	HOLD	LL*	H	L
CJS	L L L H	COND JSB PL	L	PC	HOLD	HOLD	H	L
			H	D	PUSH	HOLD	H	L
JMAP	L L H L	JUMP MAP	X	D	HOLD	HOLD	L	H
CJP	L L H H	COND JUMP PL	L	PC	HOLD	HOLD	H	L
			H	D	HOLD	HOLD	H	L
PUSH	L H L L	PUSH/COND LD CNTR	L	PC	PUSH	HOLD	H	L
			H	PC	PUSH	LOAD	H	L
JSRP	L H L H	COND JSB R/PL	L	R	PUSH	HOLD	H	L
			H	D	PUSH	HOLD	H	L
CJV	L H H L	COND JUMP VECTOR	L	PC	HOLD	HOLD	H	H
			H	D	HOLD	HOLD	H	H
JRP	L H H H	COND JUMP R/PL	L	R	HOLD	HOLD	H	L
			H	D	HOLD	HOLD	H	L
RFCT	H L L L	REPEAT LOOP, CNTR ≠ 0	L	F	HOLD	DEC	H	L
			H	PC	POP	HOLD	H	L
RPCT	H L L H	REPEAT PL, CNTR ≠ 0	L	D	HOLD	DEC	H	L
			H	PC	HOLD	HOLD	H	L
CRTN	H L H L	COND RTN	L	PC	HOLD	HOLD	H	L
			H	F	POP	HOLD	H	L
CJPP	H L H H	COND JUMP PL & POP	L	PC	HOLD	HOLD	H	L
			H	D	POP	HOLD	H	L
LDCT	H H L L	LOAD CNTR & CONTINUE	X	PC	HOLD	LOAD	H	L
LOOP	H H L H	TEST END LOOP	L	F	HOLD	HOLD	H	L
			H	PC	POP	HOLD	H	L
CONT	H H H L	CONTINUE	X	PC	HOLD	HOLD	H	L
JP	H H H H	JUMP PL	X	D	HOLD	HOLD	H	L

L = LOW
H = HIGH
X = Don't Care

DEC = Decrement
*LL = Special Case

Am29811A TRUTH TABLE

MNEMONIC	FUNCTION	INPUTS					OUTPUTS							
		I_3	I_2	I_1	I_0	TEST	NEXT ADDR SOURCE S_1	S_0	FILE $\overline{FE}$	PUP	COUNTER $\overline{LOAD}$	$\overline{EN}$	MAP $\overline{E}$	PL $\overline{E}$
	PIN NO.	14	13	12	11	10	4	5	3	2	6	7	1	9
JZ	JUMP ZERO	L	L	L	L	L	H	H	H	H	L	L	H	L
		L	L	L	L	H	H	H	H	H	L	L	H	L
CJS	COND JSB PL	L	L	L	H	L	L	L	H	H	H	H	H	L
		L	L	L	H	H	H	H	L	H	H	H	H	L
JMAP	JUMP MAP	L	L	H	L	L	H	H	H	H	H	H	L	H
		L	L	H	L	H	H	H	H	H	H	H	L	H
CJP	COND JUMP PL	L	L	H	H	L	L	L	H	H	H	H	H	L
		L	L	H	H	H	H	H	H	H	H	H	H	L
PUSH	PUSH/COND LD CNTR	L	H	L	L	L	L	L	L	H	H	H	H	L
		L	H	L	L	H	L	L	L	H	L	H	H	L
JSRP	COND JSB R/PL	L	H	L	H	L	L	H	L	H	H	H	H	L
		L	H	L	H	H	H	H	L	H	H	H	H	L
CJV	COND JUMP VECTOR	L	H	H	L	L	L	L	H	H	H	H	H	H
		L	H	H	L	H	H	H	H	H	H	H	H	H
JRP	COND JUMP R/PL	L	H	H	H	L	L	H	H	H	H	H	H	L
		L	H	H	H	H	H	H	H	H	H	H	H	L
RFCT	REPEAT LOOP, CTR ≠ 0	H	L	L	L	L	H	L	H	L	H	L	H	L
		H	L	L	L	H	L	L	L	L	H	H	H	L
RPCT	REPEAT PL, CTR ≠ 0	H	L	L	H	L	H	H	H	H	H	L	H	L
		H	L	L	H	H	L	L	H	H	H	H	H	L
CRTN	COND RTN	H	L	H	L	L	L	L	H	L	H	H	H	L
		H	L	H	L	H	H	L	L	L	H	H	H	L
CJPP	COND JUMP PL & POP	H	L	H	H	L	L	L	H	L	H	H	H	L
		H	L	H	H	H	H	H	L	L	H	H	H	L
LDCT	LD CNTR & CONTINUE	H	H	L	L	L	L	L	H	H	L	H	H	L
		H	H	L	L	H	L	L	H	H	L	H	H	L
LOOP	TEST END LOOP	H	H	L	H	L	H	L	H	L	H	H	H	L
		H	H	L	H	H	L	L	L	L	H	H	H	L
CONT	CONTINUE	H	H	H	L	L	L	L	H	H	H	H	H	L
		H	H	H	L	H	L	L	H	H	H	H	H	L
JP	JUMP PL	H	H	H	H	L	H	H	H	H	H	H	H	L
		H	H	H	H	H	H	H	H	H	H	H	H	L

L = LOW
H = HIGH

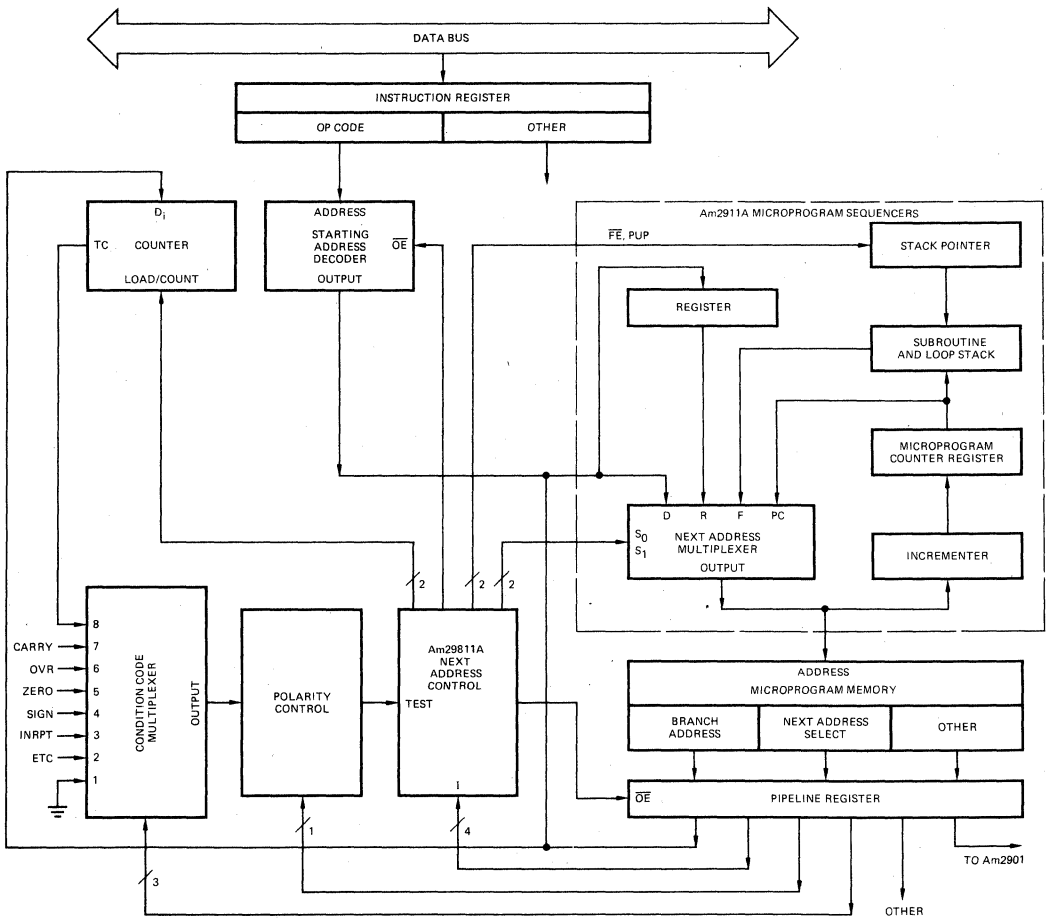
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM29811APC	P-16	C	C-1
AM29811ADC	D-16	C	C-1
AM29811ADC-B	D-16	C	B-1
AM29811ADM	D-16	M	C-3
AM29811ADM-B	D-16	M	B-3
AM29811AFM	F-16	M	C-3
AM29811AFM-B	F-16	M	B-3

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, M = − 55°C to +125°C, V_{CC} = 4.50V to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

APPLICATION



A Typical Computer Control Unit Using the Am2911 and Am29811A.

MPR-318

Am29100
Controller Family Products Index

Am29100 High-Performance Controller Products

A BETTER WAY IS HERE

A new family of products from Advanced Micro Devices makes high-performance controller design a snap.

MICROPROGRAMMING; BEST FOR COMPUTERS, BEST FOR CONTROLLERS

Microprogramming, long the preferred approach for computer design, offers lots of advantages in controllers as well. The ease with which the functions of a microprogrammed controller can be enhanced and modified made the original 2900 Family popular for many disk, printer and communications controllers. The high-speed operation of these microprogrammed systems makes it possible to handle higher data rates from newer peripheral devices and to build intelligence into the controller.

But the original 2900 products are architecturally oriented toward computers, with design features optimized for arithmetic functions and short sequences of microinstructions. MOS processors are good choices for many low-speed applications, but when the demand for speed and intelligence goes up, they cannot keep pace. Controllers need something better: the 29100 Family.

The 29100 Family products have been designed from the ground up with peripheral control applications in mind. They are fast, they are optimized for bit-manipulation, character handling, data communication and long, sophisticated microprograms and they are designed to work together in a system.

FAST LIKE YOU'VE NEVER HAD

The central element of our new high-speed controller family is the Am29116 – a 16-bit bipolar microprocessor. It's not a slice – it's a complete 16-bit processor, with three-input ALU, 32 scratchpad registers, an accumulator, data latch, barrel shifter, priority encoder and status register with conditional code generation logic. But the Am29116 is far more than a very fast number cruncher – it's been optimized for controller-oriented applications. It's instruction set has instructions often needed in controllers that are not available in any other processor.

A WHOLE FAMILY OF FAST LSI CONTROLLER PARTS

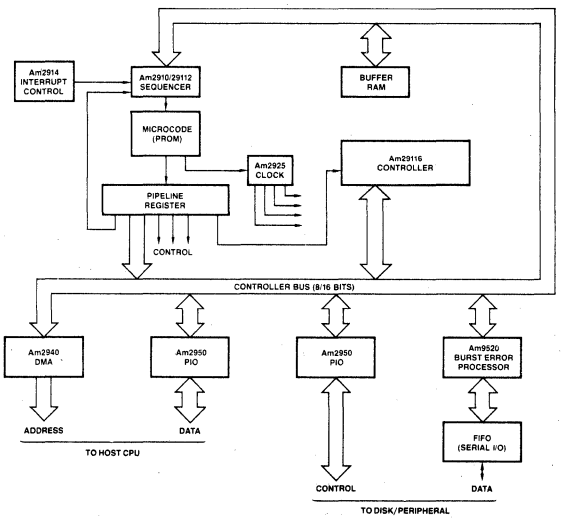
There's more to our controller family than just the Am29116. A new sequencer, the Am29112, has been expressly designed for 10MHz microprogram control, with features like real-time interrupt servicing and deep subroutining. Rapid internal data transfer is handled by the Am2940 DMA Address Generator and by the Am2950 handshaking I/O port. The Am9520 Burst Error Processor will provide a solution for error correction on disk reads. Now, more than ever, the 2900 Family is the better solution for high data rate and highly intelligent control problems.

TYPICAL CONFIGURATION USING THE 2900 CONTROLLER FAMILY

A typical intelligent controller configuration is shown below. The basic controller consists of the Am29116, a microprogram control unit and a high-speed buffer memory. Each microinstruction includes: a) a 16-bit instruction field to the Am29116, b) next-microinstruction selection bits, c) control for the buffer memory, d and e) control for the interface circuits and f) possibly an 8 or 16-bit data field.

Interface circuits like the Am2940 and Am2950 are used to provide DMA and to pass data between the controller and the host computer. Other circuits are used to interface to the peripheral. In this example, a disk interface is shown with a serial-parallel converter, a FIFO and a burst error processor. Controllers for other peripherals use identical hardware except for the peripheral interface itself.

HIGH-PERFORMANCE INTELLIGENT CONTROLLER



Am29112

A High-Performance 8-Bit Slice Microprogram Sequencer

DISTINCTIVE CHARACTERISTICS

- **Fast –**
  The Am29112 is designed to operate in 10MHz microprogrammed systems.
- **Expandable –**
  A single Am29112 is 8 bits wide and addresses 256 words of microprogram memory. Two Am29112's may be cascaded to directly address up to 64K of microprogram memory.
- **Deep stack –**
  A 33 deep on-chip stack is used for subroutine linkage, interrupt handling and loop control.
- **Interruptible at the microprogram level –**
  Two kinds of interrupts: maskable and unmaskable.
- **Powerful loop control –**
  Features an 8-bit counter for loop control. When two Am29112s are cascaded, the counters can act as a single 16-bit counter or two independent 8-bit counters.
- **Powerful addressing modes –**
  Features direct, multiway, multiway relative and program counter relative addressing.
- **Support for writable control store**
- **Hold feature –**
  A hold pin facilitates multiple sequencer implementations.
- **48-pin Hermetic DIP**

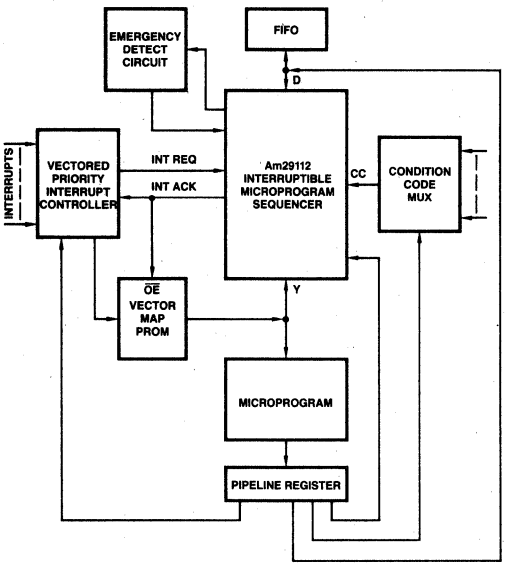
FUNCTIONAL DESCRIPTION

The Am29112 is a high performance interruptible microprogram controller intended for use in very high speed microprogrammed machines and optimized for the new state-of-the-art ALU's and other processing components.

It has an instruction set featuring relative and multiway branching, a rich variety of looping constructs, and provision for loading and unloading the on-chip stack.

Interrupts are accepted at the microcycle level and serviced in a manner completely transparent to the interrupted microcode.

Figure 1. Am29112 in a Single Pipelined System



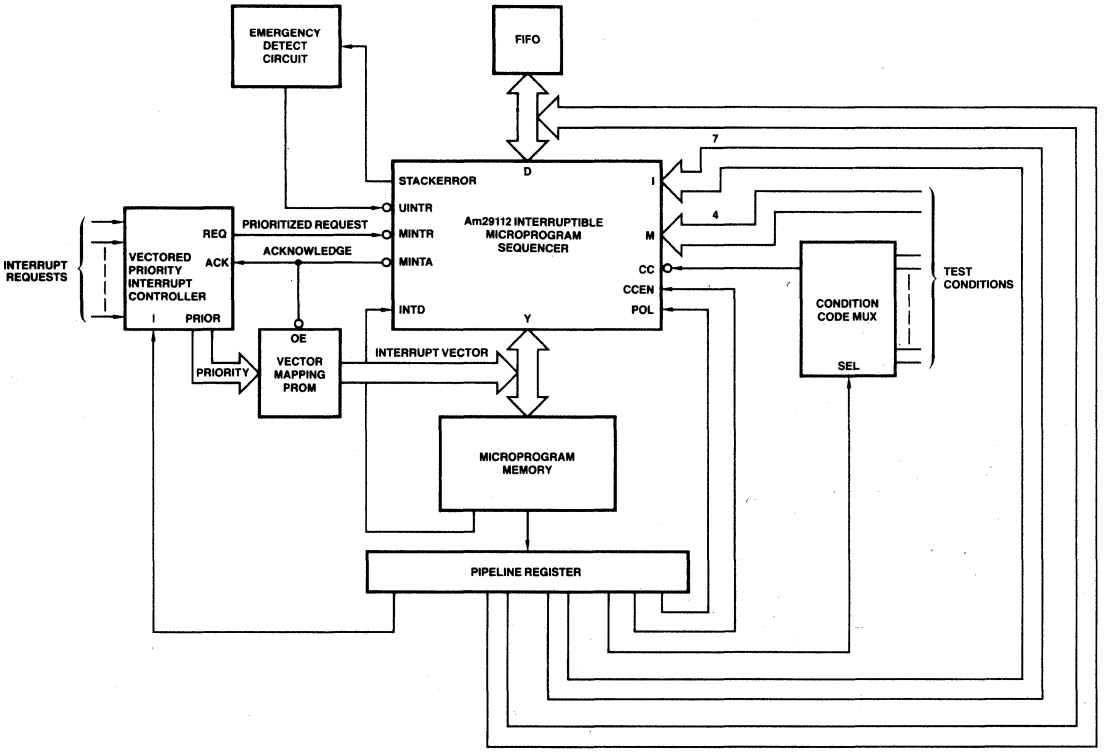
RELATED PRODUCTS

Part No.	Description
Am29116	A 16-Bit Bipolar Microprocessor
Am2904	Status and Shift Control Unit
Am2910A	Microprogram Controller
Am2914	Vectored Priority Interrupt Controller
Am2925	System Clock Generator and Driver
Am2940	DMA Address Generator
Am2942	Programmable Timer/Counter/DMA
Am2950/51/52/53	8-Bit Bidirectional I/O Port
Am29118	8-Bit Bidirectional I/O Port/Accumulator

APPLICATION NOTES REFERENCE

- Microprogrammed CPU using Am29116
- An intelligent fast disk controller
- Am29116 architecture speeds pixel manipulation in interactive bit mapped graphics

Figure 1. Control Path in a Single Pipelined System Using the Am29112



PIN FUNCTIONS

$D_0 - D_7$ Bidirectional data input for direct input to address multiplexer, counter and other control registers and stack output.

$Y_0 - Y_7$ Bidirectional microprogram address bus outputs microprogram address and inputs interrupt vector.

$M_0 - M_3$ Multiway input pins for up to 16 way branches.

HOLD When this signal is high, the Y bus is three-stated and the carry in to the program counter incrementer is forced low. Also, the CMUX output is selected at the incrementer input.

$\overline{CC}$ Test input for the sequencer. (See Table 2.)

CCEN Test enable for the sequencer. (See Table 2.)

POL Polarity input for test. (See Table 2.)

$I_0 - I_4$ Instruction input.

$I_5 - I_6$ Mode control input. Select one of three modes: normal, extended or forced continue. (See Table 1.)

STKERR Indicates stack overflow or underflow.

$\overline{UINTR}$ Unmaskable interrupt request input.

$\overline{MINTR}$ Maskable interrupt request input.

INTD Disable for maskable interrupts.

$\overline{MINTA}$ Maskable interrupt acknowledge.

LSS Programs the least significant chip when high, most significant chip when low.

RST Reset input. Selects zero as the next microprogram address, resets the stack pointer and interrupt logic, and disables maskable interrupts.

CP Clock input.

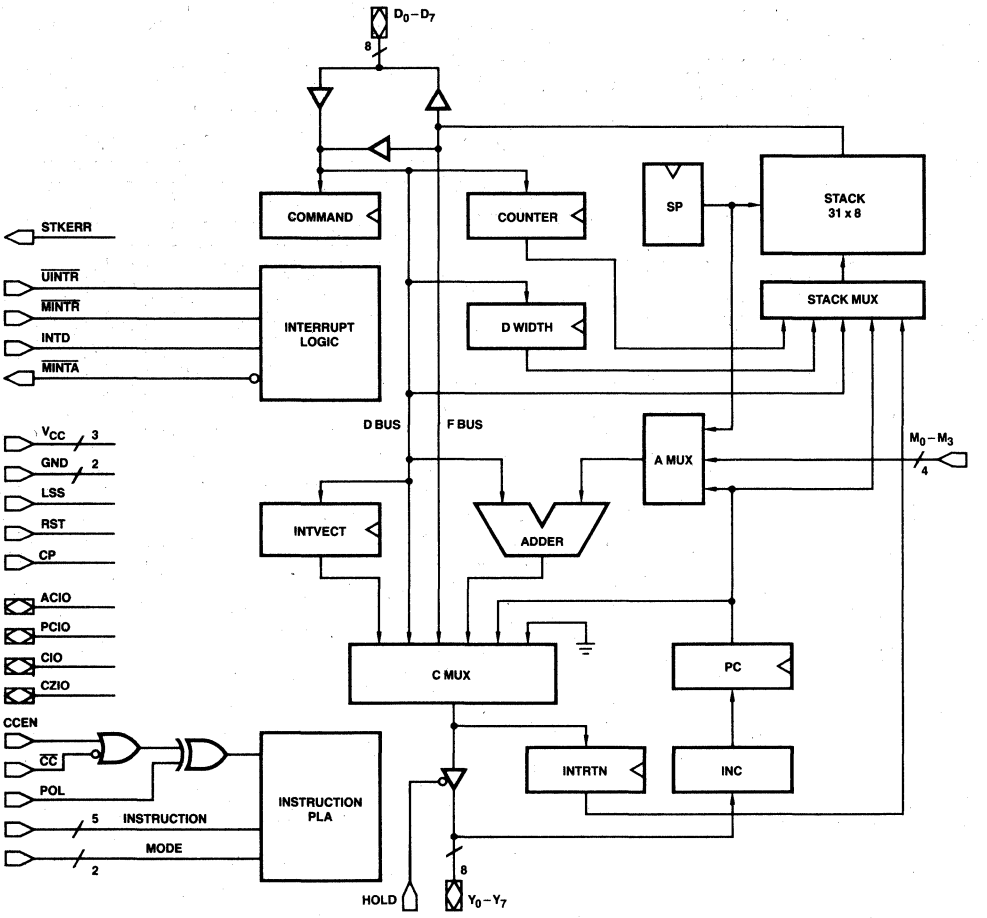
ACIO Bidirectional adder I/O line for cascaded Am29112s.

PCIO Bidirectional program counter I/O line for cascaded Am29112s.

CIO Bidirectional counter I/O line for cascaded Am29112s.

CZIO Bidirectional counter zero I/O line for cascaded Am29112s.

Figure 2. Am29112 48-Pin Package



SYSTEM OVERVIEW

The Am29112 is designed for use in single-level pipelined systems. A typical configuration is shown in Figure 1.

Branch addresses, constants for the various registers, and stack pointer values are supplied to the Am29112 through the D port which is bidirectional to allow the stack to be unloaded onto an external LIFO. The next address generated by the sequencer is output on the Y port and directly drives the microprogram memory. A single register at the output of the microprogram memory contains the microinstruction being executed, while the next is being fetched. External conditions are applied to the $\overline{CC}$ input of the Am29112 via the condition code MUX and also to the multiway inputs.

A vectored priority interrupt controller generates a prioritized interrupt request ($\overline{MINTR}$) to the Am29112, which acknowledges the request via the $\overline{MINTA}$ pin. Upon receiving the acknowledge, the priority interrupt control puts out the encoded priority of the interrupt, which is translated to a vector by the vector mapping PROM. The $\overline{MINTA}$ output of the Am29112 turns on the PROM output and simultaneously turns off the Y port, enabling the interrupt vector onto the microprogram address bus. In the Am29112, internal states are automatically saved on the stack while the interrupt vector is transmitted through the Y port and incremented to form the next microprogram address.

The emergency detect circuit generates an unmaskable interrupt request upon power failure or stack error. On receiving an unmaskable interrupt, the sequencer branches to the unmaskable interrupt routine; the address of this routine is stored on the Am29112 in the INTVECT register. Detailed interrupt handling is discussed in a later section.

ARCHITECTURE OF THE Am29112

The internal organization of the Am29112 is shown in Figure 2. The most important control loop inside the sequencer consists of the CMUX, incrementer, and PC register. The CMUX selects the next microprogram address based on the instruction and condition code inputs. The next microprogram address is selected from the PC register for a continue, the D port for a branch, the adder for relative and multiway branches, the interrupt register for unmaskable interrupts, the stack for subroutine returns or loop repeats, or all zeros for the JUMP ZERO instruction.

The Am29112 has many registers other than the PC register and the interrupt register. There is an 8-bit counter used for loop control; the DWIDTH register is a 4-bit register which programs the number of least significant bits of the D port that are added to the PC in relative addressing modes; the stack pointer is a 5-bit counter/register that points to the top of stack element; the 4-bit command register is used to program the chip on power-up for compatibility with the external hardware configuration; finally, there is the INTRTN register which is used for saving the CMUX output on the stack when an interrupt occurs.

With the exception of the INTRTN register and the stack pointer, each of the above registers can be loaded directly from the D port of the Am29112.

The Am29112 features a high speed adder with full carry lookahead across 8-bits. The adder is used for PC relative addressing (branch address is PC + D), multiway relative addressing (branch address is D + M, where M is the 4-bit multiway input), and for testing the stack pointer against the D bus. In cascaded configurations, carry ripples from the LSS adder to the MSS adder over the CIO line.

The on-chip stack is 33 deep, and the Am29112 has instructions to save the D inputs, counter, multiway register, and PC-register on the stack. The stack output bus is connected via three-state buffers to the D port. It is possible to pop the stack to the D port.

INSTRUCTION SET OF THE Am29112

MODE BITS ($I_{6,5}$)

The Am29112 is controlled by 5 instruction inputs, two mode inputs, and the condition code. In typical applications it is expected that the instruction inputs are driven directly from the pipeline, whereas the mode inputs are either permanently wired high or low to select the desired operating mode, or driven indirectly via external logic. (In some applications it might be justifiable to drive the mode bits directly from the pipeline). The two mode bits select among three operating modes: normal (00), extended (01) and forced continue (10 and 11). In the normal mode, the entire instruction set of the Am29112 applies.

TABLE 1. MODE CONTROLS

I_{65}	Mode	Description
00	Normal	For cascaded Am29112s, two independent 8-bit counters
01	Extended	For cascaded Am29112s, one 16-bit counter
10	Forced Continue	The Am29112 executes a continue instruction regardless of instruction, condition code, and multiway inputs.
11		

EXTENDED MODE

The instruction set includes instructions that differentiate between upper and lower counters (when there are two cascaded Am29112s). In the normal mode, the two counters on cascaded Am29112s function independently, and it is possible to set up a doubly nested loop without having to save and restore counter values on the stack. In the extended mode, however, the counters on cascaded Am29112s behave like one 16-bit counter and instructions that differentiate between the counters degenerate into identical instructions. Hence in a system with only one Am29112 there is no use for the extended mode.

FORCED CONTINUE MODE

In the forced continue mode the Am29112 executes a continue in every cycle regardless of the instruction bits, condition code, and multiway inputs. The simplest application (if mode bits are driven directly from the pipeline) is to use forced continue for straight-line segments of code thereby permitting most of the sequencer control fields of the pipeline to be shared. The forced continue also has an important application in systems with a writeable control store where it is necessary to step through the addresses sequentially while loading the WCS.

The instructions of the Am29112 are classified into four groups:

- Branching and subroutine linkage
- Looping
- Stack and register
- Interrupt

The sequencer has an instruction repertoire of altogether 40 different instructions. In order to encode these instructions with only 5 instruction lines, the condition code is used in some cases to differentiate between two distinct instructions sharing the same opcode. This way of encoding is used for the stack and register, and interrupt groups of instructions. For these instructions, therefore, the condition code multiplexer is not used to select an external condition. However it is required to force the condition code to unconditional Pass or Fail. The condition code enable and polarity logic has been designed with this in mind. Using the enable and polarity, it is possible to generate both unconditional Pass and unconditional Fail (regardless of the condition code input). Hence the condition code is for these instructions is like a sixth instruction line, and the condition code multiplexer field of the pipeline can be shared for these instructions (see Figure 4 and Table 2).

Figure 4. Condition Code Circuit

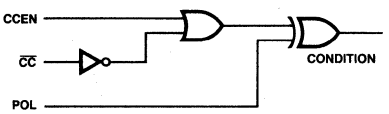


TABLE 2. CONDITION CODE TABLE

CCEN	CC	POL	Condition
0	0	0	PASS
0	1	0	FAIL
0	0	1	FAIL
0	1	1	PASS
1	0	0	PASS
1	1	0	PASS
1	0	1	FAIL
1	1	1	FAIL

Am29112 Instruction Set

Opcode (I_{40})	Condition	Mnemonic	Description
0	X	JZ.U	UNCONDITIONAL JUMP ZERO
1	PASS	PUSHD.P	PUSH D (PASS)
1	FAIL	LDCMD.F	LOAD COMMAND REGISTER FROM D (FAIL)
2	COND	POP.C	POP; CONDITIONAL STACKOUT TO D
3	COND	CJD.C	CONDITIONAL JUMP D
4	COND	CJSD.C	CONDITIONAL JUMP SUBROUTINE D
5	COND	CJMW.C	CONDITIONAL JUMP MULTIWAY D
6	COND	CJSMW.C	CONDITIONAL JUMP SUBROUTINE MULTIWAY D
7	COND	CRTN.C	CONDITIONAL RETURN
8	COND	PUSHPL.C	PUSH PC; COND LOAD LOWER COUNTER
9	COND	LDLC.C	LOAD LOWER COUNTER; COND PUSH COUNTER
10	PASS	POPLC.P	POP TO LOWER COUNTER (PASS)
11	PASS	RSTSP.P	RESET STACK POINTER (PASS)
11	FAIL	LDINTV.F	LOAD UNMASKABLE INTERRUPT VECTOR (FAIL)
12*	PASS	RFCTU.P	REPEAT LOOP, UPPER COUNTER = 0 (PASS)
12*	FAIL	RFCTL.F	REPEAT LOOP, LOWER COUNTER = 0 (FAIL)
13**	PASS	RPCTU.P	REPEAT PIPELINE, UPPER COUNTER = 0 (PASS)
13**	FAIL	RPCTL.F	REPEAT PIPELINE, LOWER COUNTER = 0 (FAIL)
14	COND	LOOP.C	TEST END LOOP
15	PASS	ENINT.P	ENABLE INTERRUPTS (PASS)
15	FAIL	DISINT.F	DISABLE INTERRUPTS (FAIL)
16***	COND	TWBL.C	THREE-WAY BRANCH, LOWER COUNTER
17***	COND	TWBU.C	THREE-WAY BRANCH, UPPER COUNTER
18	PASS	TSTSP.P	TEST SP WITH D (PASS)
18	FAIL	TSTMT.F	JUMP D IF STACK NOT EMPTY
19	COND	CJDF.C	COND JUMP D/STACK AND POP
20	COND	CJSDF.C	COND JUMP SUBROUTINE D/STACK AND POP
21	COND	CJMWR.C	COND JUMP MULTIWAY RELATIVE D
22	COND	CJSMWR.C	COND JUMP SUBROUTINE MULTIWAY RELATIVE D
23	COND	CJPP.C	COND JUMP PIPELINE AND POP
24	COND	PUSHPU.C	PUSH PC; COND LOAD UPPER COUNTER
25	COND	LDUC.C	LOAD UPPER COUNTER; COND PUSH COUNTER
26	PASS	POPUC.P	POP TO UPPER COUNTER (PASS)
26	FAIL	POPDW.F	POP TO DISPLACEMENT WIDTH (FAIL)
27	COND	LDDW.C	LOAD DISPLACEMENT WIDTH; COND PUSH DW
28	COND	CJR.C	COND JUMP D PC REL
29	COND	CJRN.C	COND JUMP D PC REL NEGATIVE
30	COND	CJSR.C	COND JUMP SUBROUTINE D PC REL
31	COND	CJSRN.C	COND JUMP SUBROUTINE D PC REL NEGATIVE

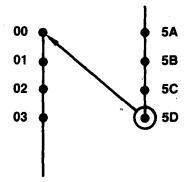
*These instructions are identical in the extended mode.
**These too.
***These too.

Extensions: U – unconditional; C – conditional; P – PASS condition; F – FAIL condition.

Note: PASS/FAIL condition can be produced as follows. P stands for polarity and I for input.

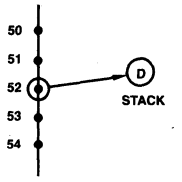
CC	CCEN	POL	Condition
X	1	0	PASS
X	1	1	FAIL
I	0	P	COND

0 Jump Zero (JZ.U)



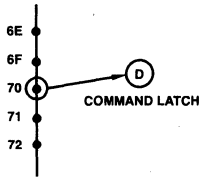
UNCONDITIONAL

1 Push D (PUSHD.P)



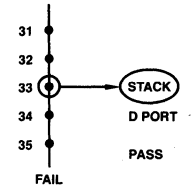
FORCED PASS

1 Load Command Latch from D (LDCMD.F)



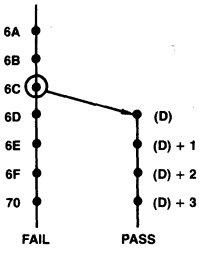
FORCED FAIL

2 Pop and Unconditional Stackout to D (POP.C)



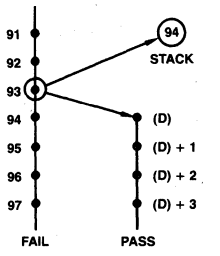
CONDITIONAL

3 Jump D (CJD. C)



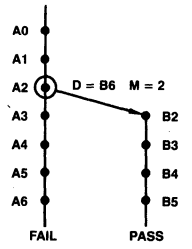
CONDITIONAL

4 Jump Subroutine D (CJSD.C)



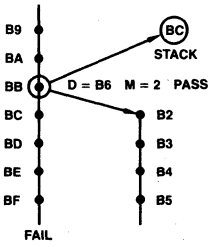
CONDITIONAL

5 Jump Multiway D (CJMW.C)



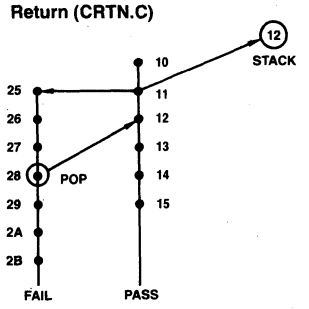
CONDITIONAL

6 Jump Subroutine Multiway D (CJSMW.C)



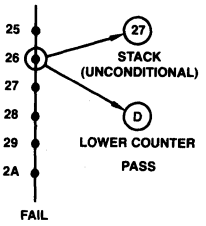
CONDITIONAL

7 Return (CRTN.C)



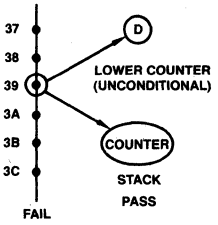
CONDITIONAL

8 Push PC and Conditional Load Lower Counter (PUSHPL.C)



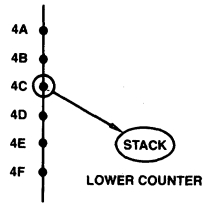
CONDITIONAL

9 Load Lower Counter and Conditional Push Counter (LDLC. C)



CONDITIONAL

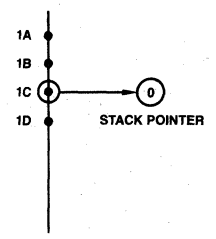
10 Pop to Lower Counter (POPLC.P)



FORCED PASS

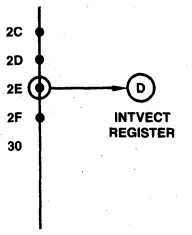
6

11 Reset Stack Pointer (RSTSP.P)



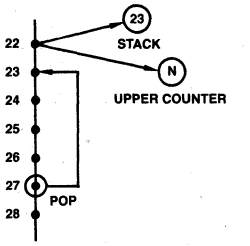
FORCED PASS

11 Load Unmaskable Interrupt Vector (LDINTV.F)



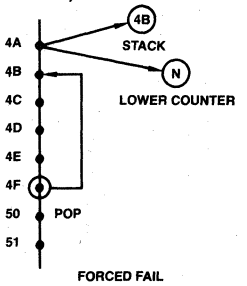
FORCED FAIL

12 Repeat Loop, Upper Counter (RFCTU.P)



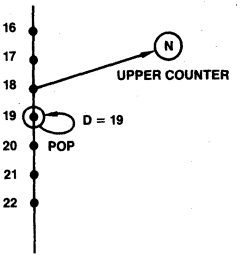
FORCED PASS

12 Repeat Loop, Lower Counter (RFCTL.F)



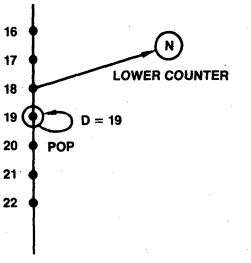
FORCED FAIL

13 Repeat Pipeline, Upper Counter (RPCTL.P)



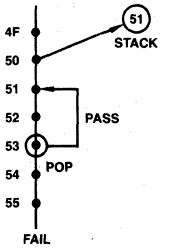
FORCED PASS

13 Repeat Pipeline, Lower Counter (RPCTL.F)



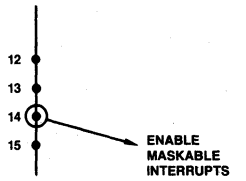
FORCED FAIL

14 Test End Loop (LOOP.C)



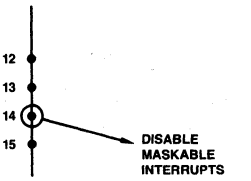
CONDITIONAL

15 Enable Interrupts (ENINT.P)



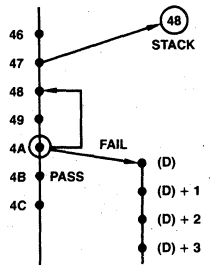
FORCED PASS

15 Disable Interrupts (DISINT.F)



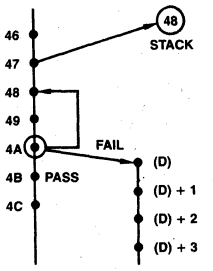
FORCED FAIL

16 Three-Way Branch, Lower Counter (TWBL.C)



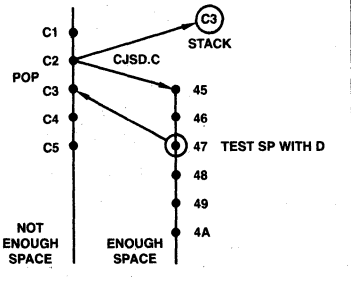
CONDITIONAL

17 Three-Way Branch, Upper Counter (TWBU.C)



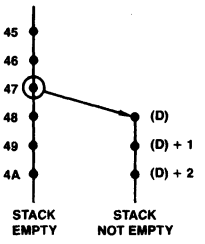
CONDITIONAL

18 Test SP with D (TSTSP.P)



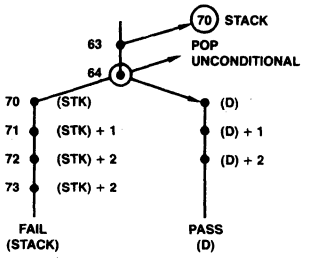
FORCED PASS

18 Jump D if Stack Not Empty (TSTMT.F)



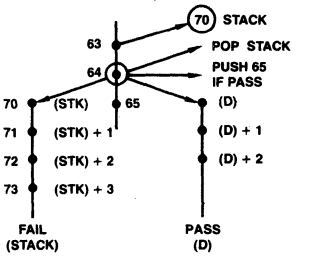
FORCED FAIL

19 Conditional Jump D/Stack and Pop (CJDF.C)



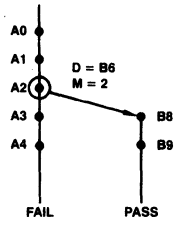
CONDITIONAL

20 Conditional Jump Subroutine D/Stack and Pop (CJSDF.C)



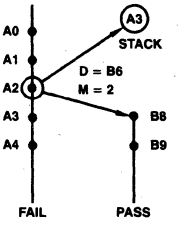
CONDITIONAL

21 Conditional Jump Multiway Relative D (CJMWR.C)



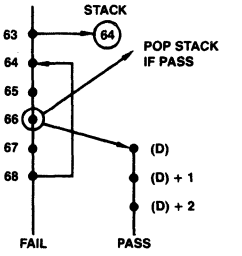
CONDITIONAL

22 Conditional Jump Subroutine Multiway Relative D (CJSMWR.C)



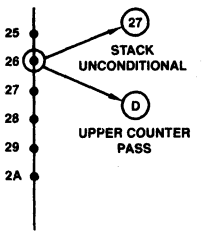
CONDITIONAL

23 Conditional Jump Pipeline and Pop (CJPP)



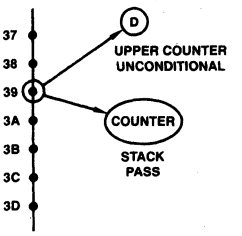
CONDITIONAL

24 Push PC and Conditional Load Upper Counter (PUSHPU.C)



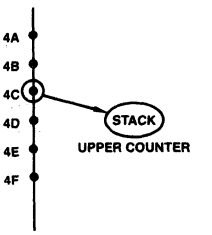
CONDITIONAL

25 Load Upper Counter and Conditional Push Counter (LDUC.C)



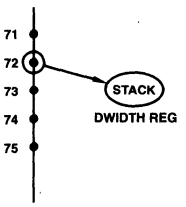
CONDITIONAL

26 Pop to Upper Counter (POPUC.P)



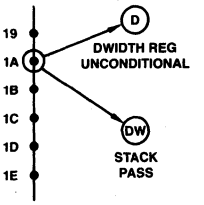
FORCED PASS

26 Pop to Displacement Width (POPDW.F)



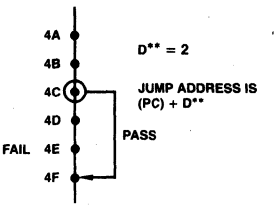
FORCED FAIL

27 Load Displacement Width and Conditional Push DW (LDDW.C)



CONDITIONAL

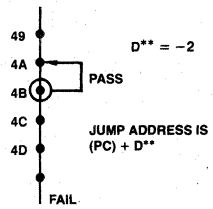
28 Conditional Jump D PC Relative (CJR.C)



D** is displacement (see 1).

CONDITIONAL

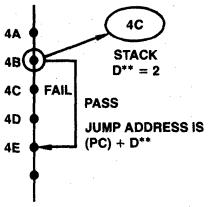
29 Conditional Jump D PC Relative Negative (CJRN.C)



D** = −2, should be two's complement (see 2).

CONDITIONAL

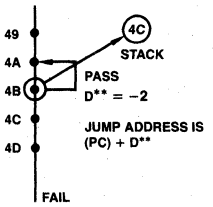
30 Conditional Jump Subroutine D PC Relative (CJSR.C)



D** is displacement (see 1).

CONDITIONAL

31 Conditional Jump Subroutine D PC Relative Negative (CJSRN.C)



D** = −2, should be two's complement (see 2).

CONDITIONAL

Notes: 1. The number of bits of D used as displacement is stored in DWIDTH register. The remaining high order bits are zero-extended.
2. The number of bits of D used as displacement is stored in DWIDTH register. The remaining high order bits are one-extended.

BRANCHING INSTRUCTIONS

Direct Branching

Instruction 0 is the unconditional jump to zero instruction. This instruction also resets the stack pointer and the interrupt logic.

Direct branching is implemented by instruction 3 (COND JUMP D) and 4 (COND JSB D). The branch address is input through the D port. If the condition is PASS, the branch is taken, otherwise the sequencer executes a continue. Two-way direct branching is implemented by instruction 19 (COND JMP D/STACK) and instruction 20 (COND JSB D/STACK). If the condition is Pass, the branch address is taken from the D input port, otherwise, the branch address is taken from the stack. In either case the stack is popped. This instruction assumes that the alternative address was pushed on the stack by a previous instruction. Jump to subroutine differs from JUMP in that the PC register is pushed on the stack if the condition is PASS for a jump subroutine. This enables the subroutine to use COND RETURN (7) to return to the point of call. Note that the two-way jump to subroutine (20) causes a simultaneous pop and push so that the stack pointer is unaffected but the top of stack element is replaced by the return address.

Relative Branching

In the relative branch instructions, a dynamically alterable subfield of the D inputs is added to the PC to form the branch address. The remaining most significant bits of the D inputs are ignored and internally converted to all 0's for forward branches and all 1's for backward branches. The displacement width (DWIDTH) register in the Am29112 holds the number of least significant bits of D that participate in the relative branch as the displacement, and can be loaded from the D port. In cascaded systems, the displacement width has to be loaded consistently in the two chips. For example, for a displacement width of 9, the lower order chip gets a displacement width of 8 and the higher order chip gets a displacement width of 1. As another example, if the lower order chip has a displacement width of less than 8 bits, the higher order chip must have a displacement width of zero. If the displacement width register is loaded with any value greater than 8, it is exactly as if it were loaded with 8.

Instruction 28 (29) is the relative jump (jump back) instruction, and instruction 30 (31) is the relative jump to subroutine (jump back to subroutine). For backward relative branches, the displacement must be coded as a two's complement negative number. When the displacement width is the same as the microaddress width the forward and backward relative branch instructions are identical. When the displacement width is less than the microaddress width, the more significant bits of D outside the displacement are forced to all zeros for positive branches and to all ones for negative branches. This is effectively like sign extension except that the sign information is contained in the instruction rather than the displacement, and there is no need for sign information to propagate between cascaded chips since it is assumed that the displacement width registers in the two chips have been consistently loaded.

The disadvantage of having the sign information in the instruction rather than the displacement can be overcome by a judicious choice of instruction format. The opcodes for forward and backward relative branch instructions have been chosen to differ in the least significant bit position only, with a '0' in that bit for forward branches and a '1' for backward branches. If the sequencer instruction field is contiguous with and on the more significant side of the displacement field in the pipeline register, then the least significant instruction bit is like the sign bit for the displacement for relative branch instructions. This permits the assembler to use the same opcode for forward and backward relative branch instructions, but *overlap* the displacement field (now declared to be one bit longer than the actual displacement field in the pipeline) with the sequencer instruction field by one bit. If the assembler now generates a negative displacement, the sequencer opcode formed is the backward branch; while if the displacement is positive, the sequencer opcode formed is forward branch.

When the instruction is executed, the PC already has been incremented and points to the next sequential instruction, hence a forward branch with a displacement of 0 causes the next sequential instruction to be executed.

Multiway Branching

Two variants of multiway branching are available on the Am29112 – multiway substitute D and multiway relative D. In multiway substitute D the 4 multiway inputs directly replace the 4 least significant bits of the branch address input at D. Instruction 5 is a conditional multiway branch and instruction 6 a conditional multiway subroutine call. In these instructions, the least significant 4 bits of the D input port are not used by the

sequencer, and may be shared, for instance to select among different sets of multiway inputs.

Multiway branching has the disadvantage that the jump table must be aligned on a 16 word boundary. This disadvantage is overcome in the Am29112 multiway relative branching instructions. In these instructions, the number input on the multiway pins is added to the branch address input at D. Instruction 21 is a conditional multiway relative branch and instruction 22 a conditional multiway relative subroutine call.

One of the advantages of multiway branching is that it enables a 16 way decision to be made in exactly one microcycle. However, the 16 target addresses are constrained to be contiguous in memory. Hence, if the target routines need more than one microword each, as is very likely, they are addressed indirectly through a table of 16 contiguous branch instructions. For very high speed applications, the extra microcycle needed to branch indirectly off the jump table may not be acceptable. This penalty is avoidable if the multiway bits are offset with respect to the D inputs. When two cascaded Am29112's are used, there are two sets of 4-bit multiway inputs. The least significant chip has a multiway input with no offset, while the most significant chip has a multiway input with an 8-bit offset. The Am29112 command register has a bit CR(1) that enables or disables multiway branching on the chip. In a system with two cascaded Am29112s, each chip has a command register bit. Multiway branching may be disabled in either chip by resetting the command register bit on that chip, or enabled by setting the command register bit. When multiway branching is disabled on a chip, for that chip both multiway and multiway relative branches are converted to direct branches, and the multiway inputs are a don't care. Multiway branching with an 8-bit offset is implemented by disabling multiway in the least significant slice and enabling it in the most significant slice. In this case, the 16 target addresses are dispersed in memory, separated by 256 locations each. Another useful configuration is obtained by enabling multiway on both chips. In this case, up to 16 sets of target addresses are dispersed in memory, separated by 256 locations each.

The Am29112 does not have an unconditional continue in its instruction set. This is not expected to be a drawback because the instruction set requires that both unconditional PASS and unconditional FAIL are required by the sequencer to select among different instructions sharing the same opcode. Hence, a continue is obtained by executing instruction 3 (COND JUMP D) with a forced FAIL condition.

LOOPING INSTRUCTIONS

The looping instructions on the Am29112 are of two kinds: conditional, which depend on an external condition to signal loop termination, and iterative, which decrement the Am29112 counter and check for a count of zero. There is also a three-way branch instruction that combines the check for external condition with the check for count of zero in a single instruction.

All the looping instructions are similar in two respects. Firstly, the check for the loop condition is done at the end of the loop. This implies that the loop body is always executed at least once. Secondly, in the case that the loop has to be repeated, a backward branch to the loop head is made by using the address on top of stack. This frees the D inputs for other use, but makes it necessary to push the address of the start of the loop on the stack before entering the loop. Also, if the loop is iterative, it is necessary to load a count value in the counter at the same time. Instructions 24 (PUSH PC; COND LOAD UPPER COUNTER) and 8 (PUSH PC; COND LOAD LOWER COUNTER) combine both these requirements.

Instruction 14 implements a simple conditional repeat loop. If the condition is FAIL the sequencer loops back using the top of stack address, and if the condition is PASS, the sequencer performs a continue to the next sequential address, and simultaneously pops the stack to remove the address of the loop head. The instruction may be described in Pascal-like syntax as:

repeat PUSH PC
  LOOP BODY
until condition = TRUE;

Instruction 23 (COND LOOP EXIT) implements a loop exit that may be used with any of the Am29112 loop instructions. It is a conditional jump to D, which simultaneously pops the stack. If the condition is FAIL, it simply performs a continue.

As discussed earlier, the counters present in cascaded Am29112s may be used independently or cascaded as a single 16-bit counter under microprogram control. The mode bits select the cascaded configuration only in the extended mode. There are separate repeat and three-way branch instructions for upper and lower counters. In the case of the repeat instructions, the condition code is used to differentiate between the repeat on the upper and the repeat on lower counter (a condition of PASS selects the upper counter). In the case of the three-way branch, which needs the condition code input for the external condition, there are two separate opcodes for three-way branch on upper (opcode 17) and three-way branch on lower (opcode 16). When a single Am29112 is used only the repeat on lower counter instructions are useful; and when two Am29112s are cascaded but operated in the extended mode, the repeat instructions on upper and lower counter are identical in effect and both operate on the 16-bit cascaded counter.

Instruction 12 (REPEAT LOOP IF COUNTER NOT ZERO) is the iterative analog of instruction 14 (CONDITIONAL REPEAT LOOP). Instruction 8 (PUSH PC; COND LOAD COUNTER) is used with condition code as forced PASS and the desired count in the D field of pipeline. This causes the address of the loop head to be pushed on the stack, and the lower counter loaded with the count. At the end of the loop body, the repeat instruction checks if the count is zero. If it is not zero, it performs a loop back using the top of stack address; and simultaneously decrements the counter; if it is zero, it pops the address of the loop head off the stack and simultaneously selects the next sequential address thereby exiting the loop. A repeat loop on the upper counter can be set up using instruction 24 instead of 8 to push PC and load upper counter, and using instruction 14 to loop back with condition code as forced PASS. Note the potential off-by-one error: since the count is checked before it is decremented, a count of 1 causes two iterations: the first iteration finds a count of 1 and decrements; on the second iteration the count is found to be zero and the loop terminates. Hence, the value of count loaded should be *one less* than the desired number of iterations. In the example above, loading the counter with 7 resulted in 8 iterations.

The single instruction repeat (instruction 13) is provided for applications where the loop body is a single microinstruction, for example, an ALU shift. The loop is set up as before using instruction 8 or 7 (PUSH PC; COND LOAD COUNTER). The repeat instruction then presents its own address to the D inputs of the sequencer. As with the repeat loop instruction, the single instruction repeat checks for counter = 0. If the counter is equal to zero, it pops the stack and continues to the next sequential instruction; otherwise it repeats the address presented to the D inputs, which is its own address, and decrements the count by one. Instruction 13 can also be used in place of

instruction 12 where there is no stack location available to hold the address of the loop head.

Often it is necessary to repeat an action until either some external condition becomes true or a predetermined count is reached: for example, searching a character string for an occurance of some character. The three-way branch instructions of the Am29112 combine the test for count and external condition in one cycle. At any loop iteration, if the condition becomes PASS when the three-way branch is executed, then the sequencer performs a continue to the next sequential instruction, and pops the stack. If the condition is FAIL when the three-way branch is executed, the sequencer tests the count. If the count is zero, then the search is unsuccessful and the sequencer performs a branch to the address input at the D port, simultaneously popping the stack. If the count is not zero, and the condition is FAIL, the sequencer performs a loop back via the stack, and decrements the counter by one.

Since interrupts may occur at any point in the execution of microcode, it is necessary to be able to save counter values on the stack so that the interrupt routines can use the counter without interfering with the operation of the interrupted code. The sequencer provides instructions that permit arbitrary nesting of loops and subroutine calls. Instruction 9 (LOAD LOWER COUNTER; CONDITIONAL PUSH COUNTER) can be used to load the lower counter from the D port. If the condition is PASS, then the instruction also causes the old counter value to be pushed on the stack. To restore the counter from the stack, instruction 10 (POP TO LOWER COUNTER) can be used with a forced FAIL condition. Instructions 25 (LOAD UPPER COUNTER; CONDITIONAL PUSH COUNTER) and 26 (COND POP TO UPPER COUNTER/POP TO DISPLACEMENT WIDTH) are the counterparts for operating on the upper counter. Note that in cascaded systems, when the counter is pushed, regardless of whether instruction 25 or instruction 10 is executed the entire counter is pushed to keep the stack balanced in the two Am29112s.

STACK AND REGISTER INSTRUCTIONS

In addition to all the instructions mentioned earlier that explicitly or implicitly alter the stack, the Am29112 has some specialized instructions for stack manipulation.

The stack on the Am29112 is 33 deep. Attempting to push when the stack is full or to pop when the stack is empty causes the STACK ERROR signal out of the Am29112 to be generated. The error is latched internally and persists until either the chip is reset, or the stack is popped in case of overflow or pushed in case of underflow. When the stack overflows, the stack pointer does not wrap around, and all subsequent pushes on the full stack write over the top-of-stack location.

The stack on the Am29112 can be loaded through the D port using instruction 1 (COND PUSH D/LOAD COMMAND REGISTER) with condition as forced PASS and unloaded out of the D port using instruction 2 (POP; COND STACKOUT TO D) with a forced PASS condition. In the stackout instruction the D port becomes an output port. Care must be taken to avoid contention on the D bus when this instruction is executed. The ability to load and unload the stack is useful for implementing context switches. For fast unloading of the stack, a tight two-instruction loop can be set up using instruction 12 (POP; COND STACKOUT TO D) with a forced FAIL condition and instruction 18 (COND TEST SP/BRANCH STACK NOT EMPTY) also with a forced FAIL condition. The branch instruction performs a branch to D if the stack is not empty.

The stack nesting level in an interruptible sequencer varies dynamically. Hence, the Am29112 is provided with instructions for checking the available stack space: instruction 18 (COND TEST SP/BRANCH STACK NOT EMPTY). Two distinct instructions for testing the stack pointer have been packed into the same opcode, and are differentiated by the condition code. A condition code of PASS selects the Test Stack Pointer instruction. In this instruction, the sequencer tests the stack to see if there is enough space, as determined by a constant input at the D port; if there is enough space, the sequencer performs a continue, whereas if there is not enough space, the sequencer performs a subroutine return. The number of stack locations required is input at the D port. In a system with only one Am29112, the least significant 6 bits of the D are used within the chip for this instruction. In a system with two cascaded Am29112s the determination is made *independently* in the two chips (since the stack pointer is at all times identical in the two chips). Hence, the same number must be presented to the two chips. The adders in the two Am29112s are not cascaded for this instruction but function independently. In both Am29112s only the 6 LSBs of the D port are actually used in the comparison.

INTERRUPT HANDLING

The Am29112 recognizes two kinds of interrupts: maskable and unmaskable. Maskable interrupts cause automatic saving of status on the internal stack and can be inhibited, either externally via the INTERRUPT DISABLE pin, or internally via instruction 15 (COND ENABLE/DISABLE INTERRUPT). In addition, maskable interrupts are disabled when there is not enough space on the stack to service the interrupt, though this internal inhibit can be overidden be clearing a bit in the command register. The unmaskable interrupt, on the other hand, cannot be disabled and does not cause saving of status on the internal stack. It is intended for handling abnormal and irrecoverable situations like power failure or stack overflow. When an unmaskable interrupt occurs, the sequencer branches to the address of the unmaskable interrupt routine stored in the INTVECT register. This address is stored on chip at system initialize time using instruction 11 (COND RESET SP/LOAD INTERRUPT REGISTER) with a condition of FAIL. If a maskable interrupt is being processed when the unmaskable interrupt occurs, the unmaskable interrupt may be delayed at most one cycle to prevent contention on the Y bus. In any case, the unmaskable interrupt request should persist for at least one clock edge.

The Am29112 contains an interrupt disable flip-flop on-chip. The flip-flop is set by the DISABLE INTERRUPT instruction (opcode 15 with forced FAIL) and reset by the ENABLE INTERRUPT instruction (opcode 15 with forced PASS). The flip-flop output performs the same function as the interrupt disable pin. On reset, or on receiving an unmaskable interrupt, the flip-flop is set thereby disabling maskable interrupts. Hence, at the end of initialization, the ENABLE INTERRUPT instruction will have to be executed to reset the flip-flop and enable maskable interrupts.

In the case of maskable interrupts, the interrupt return address is saved on the stack automatically using the INTRTN register. The INTRTN register is loaded with the CMUX output with every clock. When an interrupt is acknowledged, the Am29112 output is turned off and the vector applied externally. However, the sequencer executes the instruction which is in the pipeline register in that cycle. The result of executing the interrupted instruction, namely the next address, does not come out of the Am29112 Y bus because the Y bus is used to input the interrupt vector. It is clocked into the INTRTN register. On the first cycle of the interrupt routine, the sequencer pushes the return

address on the stack so that the interrupt routine returns by doing a COND RETURN, like any other subroutine.

THE INVISIBLE STACK PUSH THAT THE SEQUENCER EXECUTES WHEN IT IS INTERRUPTED OCCURS IN THE FIRST CYCLE OF THE INTERRUPT SERVICE ROUTINE. HENCE, THE FIRST INSTRUCTION OF THE INTERRUPT SERVICE ROUTINE MAY NOT BE ANY INSTRUCTION THAT USES THE STACK.

Before acknowledging an interrupt, the sequencer checks the stack to see if there is enough space to handle the interrupt. If there is insufficient space on the stack, the acknowledge is not generated. This feature may be disabled by a bit in the command register.

CR(0) = 1 INHIBIT ACKNOWLEDGE ON STACK FULL (DEFAULT)

CR(0) = 0 GENERATE ACKNOWLEDGE ON STACK FULL

MASKABLE INTERRUPTS

The branch vector for maskable interrupts is applied externally to the Y port of the Am29112. This section discusses the system timing considerations and their impact on interrupt handling in the Am29112.

Figure 3(a) shows a general system configuration highlighting the interrupt portion of the circuitry and the control loop. A priority interrupt controller generates an interrupt request for the highest priority pending interrupt. This request is applied to the $\overline{\text{MINTR}}$ pin of the Am29112. If the request is not masked, the Am29112 puts out an acknowledge on the $\overline{\text{MINTA}}$ pin. The interrupt controller then puts out the encoded priority of the highest priority interrupt to the vector PROM, which maps the priority code into a vector.

The $\overline{\text{MINTA}}$ line turns on the vector PROM output at the same time as the Y port on the Am29112 is three-stated. Hence, the interrupt vector gets onto the micromemory address bus and is also input into the Am29112, and incremented to form the next address. The Am29112 saves the return address on the stack so that when the interrupt service routine does a subroutine return, control returns to the instruction following the interrupted instruction.

The maskable interrupt request is synchronized on the Am29112. If there is no disable, therefore, the acknowledge always is active in the cycle following the request. However, the acknowledge to Y bus three-stating delay is programmable: the Y bus three-stating signal can occur either in the same cycle as, or in the cycle following, the $\overline{\text{MINTA}}$ acknowledge, depending on a bit in the command latch of the Am29112.

The command register bit that programs the postdelay option is bit 2, the third least significant bit. The command register has 3 bits altogether and is loaded from the 3 LSBs of the D inputs using instruction 1 (COND PUSH D/LOAD COMMAND REGISTER) with a condition of PASS. Note that in a system with two cascaded Am29112s the command registers in the two chips must both be loaded with the same data on system initialization. The postdelay bit in the command register selects the postdelay option when it is zero.

Figure 3(b) shows the configuration without postdelay, including a simplified view of the acknowledge circuit. The acknowledge is granted at the same time the Y output of the Am29112 is three-stated and the vector PROM enabled by the MINTA signal out of the Am29112. The critical delay path in this case is clock to acknowledge (Am29112) + acknowledge to priority out (interrupt controller) + vector PROM access time + microprogram memory access time + pipeline setup time. Obviously, this delay will have a significant impact on overall cycle time. However, in slow systems or in systems where the vector is always available immediately with acknowledge, this configuration is acceptable. It is also acceptable if the vector mapping PROM is made part of the microprogram memory by dedicating the locations in low memory addressed by the priority to hold vectors to the corresponding interrupt routines.

Figure 3(c) shows a simplified view of the Am29112 configured with postdelay active. An external D-type flip-flop adds a one cycle delay to the $\overline{\text{MINTA}}$ signal before it switches the output enable on the vector register. The interrupt request to acknowledge delay is the same as in the circuit with postdelay inactive, but the Y bus three-stating signal occurs one cycle later than the acknowledge. The critical path has been broken into two with the register at the vector PROM output. In this case the critical delay path is cut short by the microprogram memory access time. While the vector PROM accesses the interrupt vector, the microprogram memory accesses the next sequential instruction. This implies that one more instruction of the interrupted code executes after the cycle in which the acknowledge is granted. (If that instruction happens to be a DISABLE INTERRUPT instruction, then even though no more interrupts will be accepted by the Am29112, the interrupt which has been acknowledged goes through and the corresponding interrupt service routine may enable interrupts again using the ENABLE INTERRUPT instruction.)

The command register bits are summarized below:

CR(0) : Interrupt acknowledge on stack full

CR(0) = 1: inhibit acknowledge on stack full
CR(0) = 0: generate acknowledge on stack full

CR(1) : Multiway enable

CR(1) = 1: enable multiway branching
CR(1) = 0: disable multiway branching

CR(2) : Interrupt postdelay flip-flop

CR(2) = 1: no postdelay
CR(2) = 0: postdelay

HOLD

The Am29112 is equipped with a HOLD pin for configurations utilizing more than one sequencer driving a common microprogram address bus. In such situations, it is necessary to cause the unselected sequencer to hold its internal state while some other sequencer executes, so that it can resume execution at the point where it was held. The HOLD pin, when asserted, three-states the Y bus, forces low the carry into the PC incrementer, and selects the internal CMUX output (instead of the Y bus) at the incrementer input. To complete the HOLD function, it is also necessary to disable interrupts and to put the sequencer into the forced continue mode. Under these conditions, the value of the PC is recirculated through the CMUX and the incrementer until the HOLD is released; and all the remaining state bits in the sequencer are not altered because of the forced continue.

Figure 3a. Interrupt Control Loop

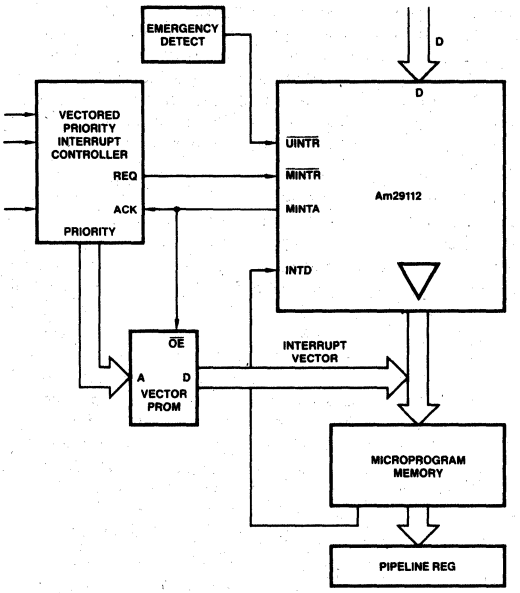
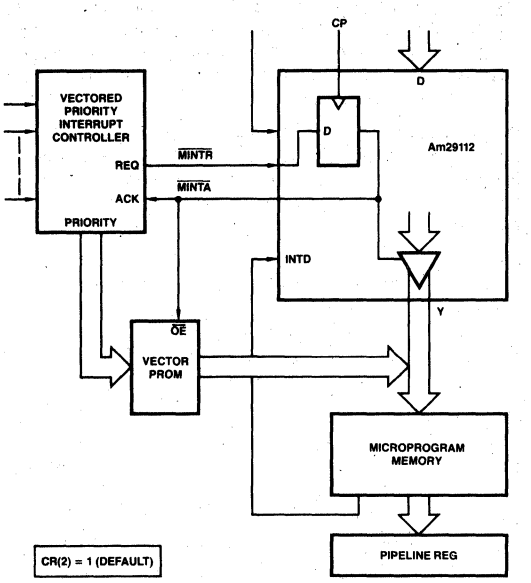
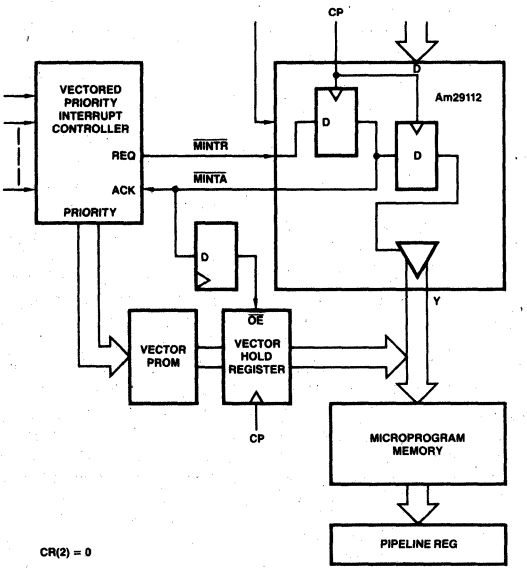


Figure 3b. No Postdelay



Note: The INTD connection directly from microprogram memory.

Figure 3c. With Postdelay



Am29116

A High-Performance 16-Bit Bipolar Microprocessor

DISTINCTIVE CHARACTERISTICS

- **Optimized for High-Performance Controllers**
  Architecture and instruction set optimized for high-performance, intelligent controllers in microprogrammed environments. Excellent solution for applications requiring speed and bit-manipulation power.
- **Fast**
  Supports 100ns microcycle time/10MHz data rate for all instructions.
- **Flexible 16-Bit Data Path**
  The ALU and all on-chip data storage elements are interconnected via a common 16-bit data bus. All instructions executable on bytes or 16-bit words.
- **16-Bit Barrel Shifter**
  Contains a 16-bit Barrel Shifter which can shift or rotate a word up to 15 positions in a single instruction cycle.
- **Immediate Instruction Capability**
  Immediate instruction capability for multiplexing data and instructions. May be used for storing constants in microcode or for configuring a second data port.
- **Powerful Field Insertion/Extraction and Bit Manipulation Instructions**
  Rotate and Merge, Rotate and Compare and bit manipulation instructions provided for complex bit control.
- **32-Working Registers**
  Contains 32 working registers arranged in a single port RAM architecture. RAM may be configured to accept different source and destination addresses within single cycle.
- **Status Register and Condition-Code Generator/Multiplexer**
  Contains status manipulation capability for condition code initiated branching and user definable flag manipulation.
- **CRC Generation**
  Has instructions which perform both forward and reverse CRC (Cyclic-Redundancy Check), calculations for any CRC polynomial of 16 bits or less. (Supports 5MHz data rate)
- **52-Pin Hermetic DIP**

OTHER LITERATURE

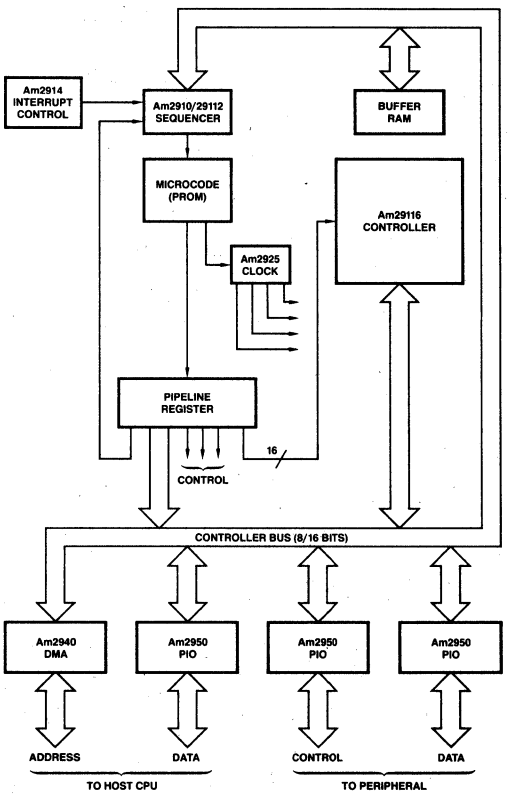
- Am29116 Electrical Characteristics
- An Intelligent Fast Disk Controller Using the Am29116 Application Note.
- A Microprogrammed CPU Using the Am29116 Application Note

TABLE OF CONTENTS

FUNCTIONAL DESCRIPTION

The Am29116 is a microprogrammable 16-bit bipolar microprocessor whose architecture and instruction set is optimized for high performance peripheral controllers, like graphics controllers, disk controllers, communications controllers, front-end concentrators and modems. The device also performs well in microprogrammed processor applications, especially when combined with the Am29516 16x16 multiplier (65ns worst-case 16x16 multiply). In addition to its complete arithmetic and logic instruction set, the Am29116 instruction set contains functions particularly useful in controller applications; bit set, bit reset, bit test, rotate and merge, rotate and compare, and cyclic-redundancy-check (CRC) generation.

Am29116 BASED HIGH PERFORMANCE PERIPHERAL CONTROLLER



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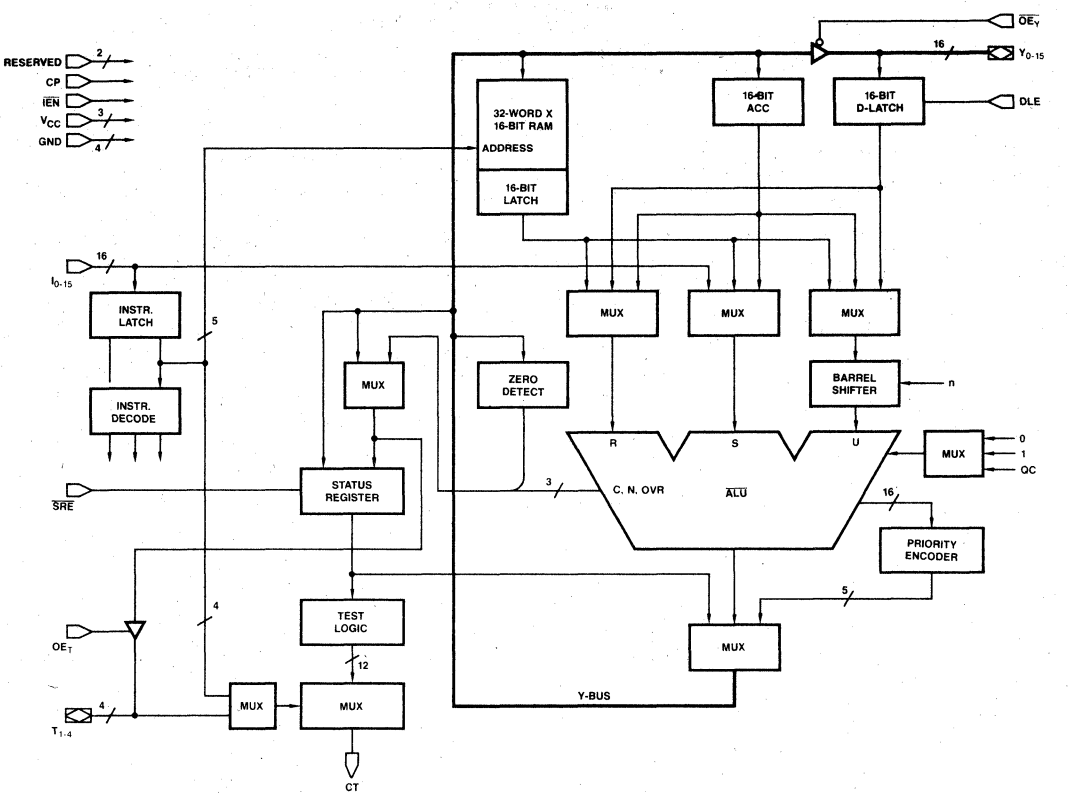


Figure 1. Detailed Am29116 Block Diagram MPR-740

PIN DEFINITIONS (Pin out provided on back page)

Y_0-Y_{15} Data Input/Output Lines. When $\overline{OE}_Y$ is HIGH, Y_0-Y_{15} are used as external data inputs which allow data to be directly loaded into the 16-bit data latch. Having $\overline{OE}_Y$ LOW allows the ALU data to be output on Y_0-Y_{15}.

DLE Data Latch Enable. When DLE is HIGH, the 16-bit data latch is transparent and is latched when DLE is LOW.

$\overline{OE}_Y$ Output Enable. When $\overline{OE}_Y$ is HIGH, the 16-bit Y outputs are disabled (high-impedance); when $\overline{OE}_Y$ is LOW, the 16-bit Y outputs are enabled (HIGH or LOW).

I_0-I_{15} Sixteen Instruction Inputs. Used to select the operations to be performed in the Am29116. Also used as data inputs while performing immediate instructions.

$\overline{IEN}$ Instruction Enable. With $\overline{IEN}$ LOW, data can be written into the RAM when the clock is LOW. The Accumulator can accept data during the LOW-HIGH transition of the clock. Having $\overline{IEN}$ LOW, the Status Register can be updated when $\overline{SRE}$ is LOW. With $\overline{IEN}$ HIGH, the conditional test output, $\overline{CT}$, is disabled as a function of the instruction inputs. $\overline{IEN}$ should be LOW for the first half of the first cycle of an immediate instruction.

$\overline{SRE}$ Status Register Enable. When $\overline{SRE}$ and $\overline{IEN}$ are both LOW, the Status Register is updated at the end of all instructions with the exception of NO-OP, Save Status, and Test Status. Having either $\overline{SRE}$ or $\overline{IEN}$ HIGH will inhibit the Status Register from changing.

CP Clock Pulse. The clock input to the Am29116. The RAM latch is transparent when the clock is HIGH. When the clock goes LOW, the RAM output is latched. Data is written into the RAM during the low period of the clock provided IEN is LOW and if the instruction being executed designates the RAM as the destination of operation. The Accumulator and Status Register will accept data on the LOW-HIGH transition of the clock if $\overline{IEN}$ is also LOW. The instruction latch becomes transparent when it exits an immediate instruction mode during a LOW-HIGH transition of the clock.

T_1-T_4 Input/Output Pin. Under the control of OE_T, the four lower status bits Z, C, N, OVR become outputs on T_1-T_4, respectively when OE_T goes HIGH. When OE_T is LOW, T_1-T_4 are used as inputs to generate the CT output.

OE_T Output Enable. When OE_T is LOW, the 4-bit T outputs are disabled (high-impedance); when OE_T is HIGH, the 4-bit T outputs are enabled (HIGH or LOW).

CT Conditional Test. The condition code multiplexer selects one of the twelve condition code signals and places them on the CT output. A HIGH on the CT output indicates a passed condition and a LOW indicates a failed condition.

ARCHITECTURE OF THE Am29116

The Am29116 is a high-performance, microprogrammable 16-bit bipolar microprocessor.

As shown in the Block Diagram, Figure 1, the device consists of the following elements interconnected with 16-bit data paths.

- 32-Word by 16-Bit RAM
- Accumulator
- Data Latch
- Barrel Shifter
- ALU
- Priority Encoder
- Status Register
- Condition-Code Generator/Multiplexer
- Three-State Output Buffers
- Instruction Latch and Decoder

32-Word by 16-Bit RAM

The 32-Word by 16-Bit RAM is a single-port RAM with a 16-bit latch at its output. The latches are transparent when the clock input (CP) is HIGH and latched when the clock input is LOW. Data is written into the RAM while the clock is LOW if the $\overline{IEN}$ input is also LOW and if the instruction being executed defines the RAM as the destination of the operation. For byte instructions, only the lower eight RAM bits are written into; for word instructions, all 16 bits are written into. With the use of an external multiplexer on five of the instruction inputs, it is possible to select separate read and write addresses for the same instruction. This two-address operation is not allowed for immediate instructions.

Accumulator

The 16-bit Accumulator is an edge-triggered register. The Accumulator accepts data on the LOW-to-HIGH transition of the clock input if the $\overline{IEN}$ input is LOW and if the instruction being executed defines the Accumulator as the destination of the operation. For byte instructions, only the lower eight bits of the Accumulator are written into; for word instructions, all 16 bits are written into.

Data Latch

The 16-bit Data Latch holds the data input to the Am29116 on the bi-directional Y bus. The latch is transparent when the DLE input is HIGH and latched when the DLE input is LOW.

Barrel Shifter

A 16-bit Barrel Shifter is used as one of the ALU inputs. This permits rotating data from either the RAM, the Accumulator or the Data Latch up to 15 positions. In the word mode, the Barrel Shifter rotates a 16-bit word; in the byte mode, it rotates only the lower eight bits.

Arithmetic Logic Unit

The Am29116 contains a 16-bit ALU with full carry lookahead across all 16 bits in the arithmetic mode. The ALU is capable of operating on either one, two or three operands, depending upon the instruction being executed. It has the ability to execute all conventional one and two operand operations, such as pass, complement, two's complement, add, subtract, AND, NAND, OR, NOR, EXOR, and EX-NOR. In addition, the ALU can also execute three-operand instructions such as rotate and merge and rotate and compare with mask. All ALU operations can be performed on either a word or byte basis, byte operations being performed on the lower eight bits only.

The ALU produces three status outputs, C (carry), N (negative) and OVR (overflow). The appropriate flags are generated at the byte or word level, depending upon whether the device is executing in the byte or word mode. The Z (zero) flag, although not generated by the ALU, detects zero at both the byte and word level.

The carry input to the ALU is generated by the Carry Multiplexer which can select an input of zero, one, or the stored carry bit from the Status Register, QC. Using QC as the carry input allows execution of multiprecision addition and subtractions.

Priority Encoder

The Priority Encoder produces a binary-weighted code to indicate the locations of the highest order ONE at its input. The input to the Priority Encoder is generated by the ALU which performs an AND operation on the operand to be prioritized and a mask. The mask determines which bit locations to eliminate from prioritization. In the word mode, if no bit is HIGH, the output is a binary zero. If bit 15 is HIGH, the output is a binary one. Bit 14 produces a binary two, etc. Finally, if only bit 0 is HIGH, a binary 16 is produced.

In the byte mode, bits 8 thru 15 do not participate. If none of bits 7 thru 0 are HIGH, the output is a binary zero. If bit 7 is HIGH a binary one is produced. Bit 6 produces a binary two, etc. Finally, if only bit 0 is HIGH, a binary 8 is produced.

Status Register

The Status Register holds the 8-bit status word. With the Status-Register Enable, ($\overline{SRE}$) input LOW and the $\overline{IEN}$ input LOW, the Status Register is updated at the end of all instructions except NO-OP, Save-Status and Test-Status instructions. $\overline{SRE}$ going HIGH or $\overline{IEN}$ going HIGH inhibits the Status Register from changing.

The lower four bits of the Status Register contain the ALU status bits of Zero (Z), Carry, (C) Negative (N), and Overflow (OVR). The upper four bits contain a Link bit and three user-definable status bits (Flag 1, Flag 2, Flag 3).

With $\overline{SRE}$ LOW and $\overline{IEN}$ LOW, the lower four status bits are updated after each instruction except those mentioned above, NO-OP, Save Status, Status Test and the Status Set/Reset instruction for the upper four bits. Under the same conditions, the upper four status bits are changed only during their respective Status Set/Reset instructions and during Status Load instuctions in the word mode. The Link-Status bit is also updated after each shift instruction.

The Status Register can be loaded from the internal Y-bus, and can also be selected as a source for the internal Y-bus. When the Status Register is loaded in the word mode, all 8-bits are updated; in the byte mode, only the lower 4 bits (Z, C, N, OVR) are updated.

When the Status Register is selected as a source in the word mode, all eight bits are loaded into the lower byte of the destination; the upper byte of the destination is loaded with all zeros. In the byte mode, the Status Register again loads into the lower byte of the destination, but the upper byte remains unchanged. This Store and Load combination allows saving and restoring the Status Register for interrupt and subroutine processing. The four lower status bits (Z, C, N, OVR) can be read directly via the bidirectional T bus. These four bits are available as outputs on the $T_{1\text{-}4}$ outputs whenever OE_T is HIGH.

Condition-Code Generator/Multiplexer

The Condition-Code Generator/Multiplexer contains the logic necessary to develop the 12 condition-code test signals. The multiplexer portion can select one of these test signals and place it on the CT output for use by the microprogram sequence. The multiplexer may be addressed in two different ways: One way is through the Test Instruction. This instruction specifies the test condition to be placed in the CT output, but does not allow an ALU operation at the same time. The second method uses the bidirectional T bus as an input. This requires extra bits in the microword, but provides the ability to simultaneously test and execute. The test instruction lines, $I_{0\text{-}4}$ have priority over $T_{1\text{-}4}$ for testing status.

Three-State Output Buffers

There are two sets of Three-State Output Buffers in the Am29116. One set controls the bidirectional, 16-bit Y bus. These outputs are enabled by placing a LOW on the $\overline{OE}$ input. A HIGH puts the Y outputs in the high-impedance state, allowing data to be input to the Data latch from an external source.

The second set of Three-State Output Buffers control the bidirectional 4-bit T bus and is enabled by placing a HIGH on the OE_T input. This allows storing the four internal ALU status bits (Z, C, N, OVR) externally. A LOW OE_T input forces the T outputs into the high-impedance state. External devices can then drive the T bus to select a test condition for the CT output.

Instruction Latch and Decoder

The 16-bit Instruction Latch is normally transparent to allow decoding of the Instruction Inputs by the Instruction Decoder into the internal control signals for the Am29116. All instructions except Immediate Instructions are executed in a single clock cycle.

Immediate instructions require two clock cycles for execution. During the first clock cycle, the Instruction Decoder recognizes that an Immediate Instruction is being specified and captures the data on the Instruction Inputs in the Instruction Latch. During the second clock cycle, the data on the Instruction Inputs is used as one of the operands for the function specified during the first clock cycle. At the end of the second clock cycle, the Instruction Latch is returned to its transparent state.

INSTRUCTION SET

The instruction set of the Am29116 is very powerful. In addition to the single and two operand logical and arithmetic instructions, the Am29116 instruction set contains functions particularly useful in controller applications; bit set, bit reset, bit test, rotate and merge, rotate and compare, and cyclic-redundancy-check (CRC) generation. Complex instructions like rotate and merge, rotate and compare, and prioritize are executed in a single microcycle.

Three data types are supported by the Am29116.

- Bit
- Byte
- Word (16-bit)

In the byte mode data is written into the lower half of the word and the upper half is unchanged. The special case is when the status register is specified as the destination. In the byte mode the LSH (OVR, N, C, Z) of the status register is updated and in the word mode all eight bits of the status register are updated. The status register does not change for save status and test status instructions. In the test status instructions the CT output has the result and the Y-bus is undefined.

The Am29116 Instruction Set can be divided into eleven types of instructions. These are:

- Single Operand
- Two Operand
- Single Bit Shift
- Rotate and Merge
- Bit Oriented
- Rotate by n Bits
- Rotate and Compare
- Prioritize
- Cyclic-Redundancy-Check
- Status
- No-Op

Each instruction type is arbitrarily divided into quadrants. Two of the sixteen instruction lines decode to four quadrants labelled from 0 to 3. The quadrants were defined mainly for convenience in classification of the instruction set and addressing modes and can be used together with the OP CODES to distinguish the instructions.

The following pages describe each of the instruction types in detail. Throughout the description $\overline{OEy}$ is assumed to be LOW allowing ALU outputs on the Y-bus.

Table 1 illustrates operand source-destination combinations for each instruction type.

TABLE 1. OPERAND SOURCE/DESTINATION COMBINATIONS

Instruction Type	Operand Combinations (Note 1)		
Single Operand	Source (R/S)		Destination
	RAM (Note 2) ACC D D(0E) D(SE) I 0		RAM ACC Y Bus Status ACC and Status
Two-Operand	Source (R)	Source (S)	Destination
	RAM RAM D D ACC D	ACC I RAM ACC I I	RAM ACC Y Bus
Single Bit Shift	Source (U)		Destination
	RAM ACC ACC D D D		RAM ACC Y Bus RAM ACC Y Bus
Rotate n Bits	Source (U)		Destination
	RAM ACC D		RAM ACC Y Bus
Bit Oriented	Source (R/S)		Destination
	RAM ACC D		RAM ACC Y Bus
Rotate and Merge	Rotated Source (U)	Mask (S)	Non-Rotated Source/ Destination (R)
	D D D D ACC RAM	I RAM I ACC I I	ACC ACC RAM RAM RAM ACC
Rotate and Compare	Rotated Source (U)	Mask (S)	Non-Rotated Source/ Destination (R)
	D D D RAM	I I ACC I	ACC RAM RAM ACC

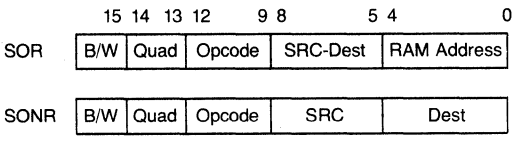
Instruction Type	Operand Combinations (Note 1)		
Prioritize (Note 3)	Source (R)	Mask (S)	Destination
	RAM ACC D	RAM ACC I 0	RAM ACC Y Bus
Cyclic Redundancy Check	Data In	Destination	Polynomial
	QLINK	RAM	ACC
No Operation	–		
Set Reset Status	Bits Affected		
	OVR, N, C, Z LINK Flag 1 Flag 2 Flag 3		
Store Status	Source		Destination
	Status		RAM ACC Y Bus
Status Load	Source (R)	Source (S)	Destination
	D ACC D	ACC I I	Status Status and ACC
Test Status	Test Condition (CT)		
	(N⊕OVR) + Z N⊕OVR Z OVR Low C Z + $\overline{C}$ N LINK Flag1 Flag2 Flag3		

Notes:
1. When there is no dividing line between the R&S OPERAND or SOURCE and DESTINATION, the two must be used as a given pair. But where there exists such a separation, any combination of them is possible.
2. In the SINGLE OPERAND INSTRUCTION, RAM cannot be used when both ACC and STATUS are designated as a DESTINATION.
3. In the PRIORITIZE INSTRUCTIONS, OPERAND and MASK must be different sources.

SINGLE OPERAND INSTRUCTIONS

The Single Operand Instructions contain four indicators; byte or word mode, opcode, source and destination. It is further subdivided into two types. The first type uses RAM as a source or destination or both, and the second type does not use RAM as a source or destination. Both types have different instruction formats as shown below. Under the control of instruction inputs, the desired function is performed on the source and the result is either stored in the specified destination or placed on the Y-bus or both. For a special case where 8-bit to 16-bit conversion is needed, the Am29116 is capable of extending sign bit (D(SE)) or binary zero (D(0E)) over 16-bits in the word mode. The least significant four bits of the Status Register (OVR, N, C, Z) are affected by the function performed in this category. The most significant bits of status register (FLAG1, FLAG2, FLAG3, LINK) are not affected. The only limitation in this type is that the RAM cannot be used as a source when both ACC and the Status Register are specified as a destination.

SINGLE OPERAND FIELD DEFINITIONS



SINGLE OPERAND INSTRUCTION

15 14 13 12 9 8 5 4 0

Instruction[1]	B/W[2]	Quad[3]	Opcode			R/S[4]		Dest[4]	RAM Address		
SOR	0 = B 1 = W	10	1100	MOVE	SRC → Dest	0000	SORA	RAM ACC	00000	R00	RAM Reg 00
			1101	COMP	$\overline{SRC}$ → Dest	0010	SORY	RAM Y Bus	. .	. .	. . . .
			1110	INC	SRC +1 → Dest	0011	SORS	RAM Status	11111	R31	RAM Reg 31
			1111	NEG	$\overline{SRC}$ +1 → Dest	0100	SOAR	ACC RAM			
						0110	SODR	D RAM			
						0111	SOIR	I RAM			
						1000	SOZR	0 RAM			
						1001	SOZER	D(0E) RAM			
						1010	SOSER	D(SE) RAM			
						1011	SORR	RAM RAM			

Instruction	B/W	Quad	Opcode			R/S[4]		Destination		
SONR	0 = B 1 = W	11	1100	MOVE	SRC → Dest	0100	SOA	ACC	00000	NRY	Y Bus
			1101	COMP	$\overline{SRC}$ → Dest	0110	SOD	D	00001	NRA	ACC
			1110	INC	SRC +1 → Dest	0111	SOI	I	00100	NRS	Status
			1111	NEG	$\overline{SRC}$ +1 → Dest	1000	SOZ	0	00101	NRAS	ACC, Status
						1001	SOZE	D(0E)			
						1010	SOSE	D(SE)			

Notes: 1. The instruction mnemonic designates different instruction formats used in the Am29116. They are useful in assembly microcode with the System 29 AMDASM™ meta assembler.
2. B = Byte Mode, W = Word Mode.
3. See Instruction Set description.
4. R = Source; S = Source; Dest = Destination.

Y BUS AND STATUS – SINGLE OPERAND INSTRUCTIONS

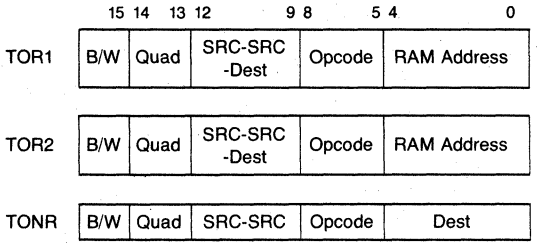
Instruction	Opcode	Description	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
SOR SONR	MOVE	SRC → Dest	0 = B	$Y_i \leftarrow SRC_i$	NC	NC	NC	NC	U	U	U	U
	COMP	$\overline{SRC}$ → Dest	1 = W	$Y_i \leftarrow \overline{SRC_i}$	NC	NC	NC	NC	U	U	U	U
	INC	SRC +1 → Dest		Y ← SRC +1	NC	NC	NC	NC	U	U	U	U
	NEG	$\overline{SRC}$ +1 → Dest		Y ← $\overline{SRC}$ +1	NC	NC	NC	NC	U	U	U	U

SRC = Source
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

TWO OPERAND INSTRUCTIONS

The Two Operand Instructions contain five indicators; byte or word mode, opcode, R source, S source, and destination. It is further subdivided into two types. The first type uses RAM as the source and/or destination and the second type does not use RAM as source or destination. The first type has two formats; the only difference is in the quadrant. Under the control of instruction inputs, the desired function is performed on the specified sources and the result is stored in the specified destination or placed on the Y-bus or both. The least significant four bits of the status register (OVR, N, C, Z) are affected by the arithmetic functions performed and only the N and Z bits are affected by the logical functions performed. The OVR and C bits of the status register are forced to ZERO for logical functions. Add with carry and Subtract with carry instructions are useful for Multiprecision Add or Subtract.

TWO OPERAND FIELD DEFINITIONS:



TWO OPERAND INSTRUCTIONS

Instruction	B/W	Quad			R[1]	S[1]	Dest[1]	Opcode			RAM Address		
TOR1	0 = B 1 = W	00	0000	TORAA	RAM	ACC	ACC	0000	SUBR	S minus R	00000	R00	RAM Reg 00
			0010	TORIA	RAM	I	ACC	0001	SUBRC	S minus R	. .	. .	. . . .
			0011	TODRA	D	RAM	ACC			with carry	11111	R31	RAM Reg 31
			1000	TORAY	RAM	ACC	Y Bus	0010	SUBS	R minus S			
			1010	TORIY	RAM	I	Y Bus	0011	SUBSC	R minus S			
			1011	TODRY	D	RAM	Y Bus			with carry			
			1100	TORAR	RAM	ACC	RAM	0100	ADD	R plus S			
			1110	TORIR	RAM	I	RAM	0101	ADDC	R plus S			
			1111	TODRR	D	RAM	RAM			with carry			
								0110	AND	$R \cdot S$			
								0111	NAND	$\overline{R \cdot S}$			
								1000	EXOR	$R \oplus S$			
								1001	NOR	$\overline{R + S}$			
								1010	OR	$R + S$			
								1011	EXNOR	$\overline{R \oplus S}$			
Instruction	**B/W**	**Quad**			**R[1]**	**S[1]**	**Dest[1]**	**Opcode**			**RAM Address**		
TOR2	0 = B 1 = W	10	0001	TODAR	D	ACC	RAM	0000	SUBR	S minus R	00000	R00	RAM Reg 00
			0010	TOAIR	ACC	I	RAM	0001	SUBRC	S minus R	. .	. .	. . . .
			0101	TODIR	D	I	RAM			with carry	11111	R31	RAM Reg 31
								0010	SUBS	R minus S			
								0011	SUBSC	R minus S			
										with carry			
								0100	ADD	R plus S			
								0101	ADDC	R plus S			
										with carry			
								0110	AND	$R \cdot S$			
								0111	NAND	$\overline{R \cdot S}$			
								1000	EXOR	$R \oplus S$			
								1001	NOR	$\overline{R + S}$			
								1010	OR	$R + S$			
								1011	EXNOR	$\overline{R \oplus S}$			

Note 1: R = Source
S = Source
Dest = Destination

TWO OPERAND INSTRUCTIONS

Instruction	B/W	Quad	R[1]	S[1]	Opcode			Destination		
	0 = B	11	0001 TODA	D ACC	0000	SUBR	S minus R	00000	NRY	Y Bus
	1 = W		0010 TOAI	ACC I	0001	SUBRC	S minus R with carry	00001	NRA	ACC
			0101 TODI	D I				00100	NRS	Status
					0010	SUBS	R minus S	00101	NRAS	ACC, Status
TONR					0011	SUBSC	R minus S with carry			
					0100	ADD	R plus S			
					0101	ADDC	R plus S with carry			
					0110	AND	$R \cdot S$			
					0111	NAND	$\overline{R \cdot S}$			
					1000	EXOR	$R \oplus S$			
					1001	NOR	$\overline{R + S}$			
					1010	OR	$R + S$			
					1011	EXNOR	$\overline{R \oplus S}$			

Notes 1: R = Source
S = Source

Y BUS AND STATUS CONTENTS – TWO OPERAND INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
	SUBR	S minus R	0 = B	$Y \leftarrow S - R$	NC	NC	NC	NC	U	U	U	U
	SUBRC	S minus R with carry	1 = W	$Y \leftarrow S + \overline{R} - 1 + QC$	NC	NC	NC	NC	U	U	U	U
	SUBS	R minus S		$Y \leftarrow R - S$	NC	NC	NC	NC	U	U	U	U
TOR1 TOR2 TONR	SUBSC	R minus S with carry		$Y \leftarrow R + \overline{S} - 1 + QC$	NC	NC	NC	NC	U	U	U	U
	ADD	R plus S		$Y \leftarrow R + S$	NC	NC	NC	NC	U	U	U	U
	ADDC	R plus S with carry		$Y \leftarrow R + S + QC$	NC	NC	NC	NC	U	U	U	U
	AND	$R \cdot S$		$Y \leftarrow R_i$ AND S_i	NC	NC	NC	NC	0	U	0	U
	NAND	$\overline{R \cdot S}$		$Y_i \leftarrow R_i$ NAND S_i	NC	NC	NC	NC	0	U	0	U
	EXOR	$R \oplus S$		$Y_i \leftarrow R_i$ EXOR S_i	NC	NC	NC	NC	0	U	0	U
	NOR	$\overline{R + S}$		$Y_i \leftarrow R_i$ NOR S_i	NC	NC	NC	NC	0	U	0	U
	OR	$R + S$		$Y_i \leftarrow R_i$ OR S_i	NC	NC	NC	NC	0	U	0	U
	EXNOR	$\overline{R \oplus S}$		$Y_i \leftarrow R_i$ EXNOR S_i	NC	NC	NC	NC	0	U	0	U

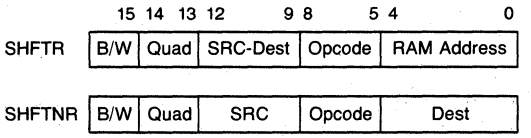
SRC = Source
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

6

SINGLE BIT SHIFT INSTRUCTIONS

The Single Bit Shift Instructions contain four indicators; byte or word mode, direction and shift linkage, source and destination. It is further subdivided into two types. The first type uses RAM as the source and/or destination and the second type does not use RAM as source or destination. Under the control of the instruction inputs, the desired shift function is performed on the specified source and the result is stored in the specified destination or placed on the Y-bus or both. The direction and shift linkage indicator defines the direction of the shift (up or down) as well as what will be shifted into the vacant bit. On a shift-up instruction, the LSB may be loaded with ZERO, ONE, or the Link-Status bit (QLINK). The MSB is loaded into the Link-Status bit as shown in Figure 2. On a shift-down instruction, the MSB may be loaded with ZERO, ONE, the contents of the Status Carry flip-flop, (QC), the Exclusive-OR of the Negative-Status bit and the Overflow-Status bit (QN⊕QOVR) or the Link-Status bit. The LSB is loaded into the Link-Status bit as shown in Figure 3. The N and Z bits of the Status register are affected but the OVR and C bits are forced to ZERO. The Shift-Down with QN⊕QOVR is useful for Two's Complement multiplication.

SINGLE BIT SHIFT FIELD DEFINITIONS:



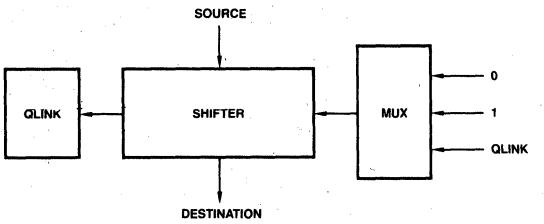


Figure 2. Shift Up Function

MPR-763

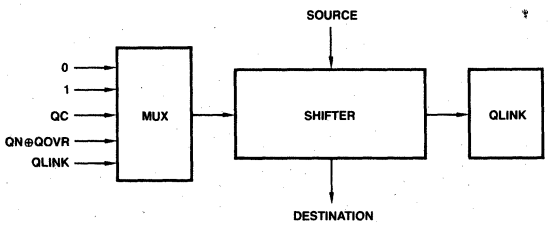


Figure 3. Shift Down Function

MPR-764

SINGLE BIT SHIFT INSTRUCTIONS

SINGLE BIT SHIFT

Instruction	B/W	Quad	U[1]	Dest[1]	Opcode				RAM Address		
SHFTR	0 = B 1 = W	10	0110 SHRR RAM 0111 SHDR D	RAM RAM	0000 SHUPZ Up 0 0001 SHUP1 Up 1 0010 SHUPL Up QLINK 0100 SHDNZ Down 0 0101 SHDN1 Down 1 0110 SHDNL Down QLINK 0111 SHDNC Down QC 1000 SHDNOV Down QN⊕QOVR				00000 R00 RAM Reg 00 . . . . . . 11111 R31 RAM Reg 31		
Instruction	**B/W**	**Quad**	**U[1]**		**Opcode**				**Destination**		
SHFTNR	0 = B 1 = W	11	0110 SHA ACC 0111 SHD D		0000 SHUPZ Up 0 0001 SHUP1 Up 1 0010 SHUPL Up QLINK 0100 SHDNZ Down 0 0101 SHDN1 Down 1 0110 SHDNL Down QLINK 0111 SHDNC Down QC 1000 SHDNOV Down QN⊕QOVR				00000 NRY Y Bus 00001 NRA ACC		

Note 1. U = Source
Dest = Destination

Y BUS AND STATUS – SINGLE BIT SHIFT INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
SHR SHNR	SHUPZ SHUP1 SHUPL	Up 0 Up 1 Up QLINK	1 = W	$Y_i \leftarrow SRC_{i-1}$, i = 1 to 15; $Y_0 \leftarrow$ Shift Input	NC	NC	NC	SRC_{15}*	0	SRC_{14}	0	U
			0 = B	$Y_i \leftarrow SRC_{i-1}$, i = 1 to 7; $Y_0 \leftarrow$ Shift Input; $Y_8 \leftarrow SRC_7$, $Y_i \leftarrow SRC_{i-8}$ for i = 9 to 15	NC	NC	NC	SRC_7*	0	SRC_6	0	U
	SHDNZ SHDN1 SHDNL SHDNC SHCNOV	Down 0 Down 1 Down QLINK Down QC Down QN⊕QOVR	0 = W	$Y_i \leftarrow SRC_{i+1}$, i = 14 to 0; $Y_{15} \leftarrow$ Shift Input	NC	NC	NC	SRC_0*	0	Shift Input	0	U
			0 = B	$Y_i \leftarrow SRC_{i+1}$, i = 1 to 6; $Y_i \leftarrow SRC_{i-7}$, i = 8 to 14; $Y_{7,15} \leftarrow$ Shift Input	NC	NC	NC	SRC_0*	0	Shift Input	0	U

SRC = Source;
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

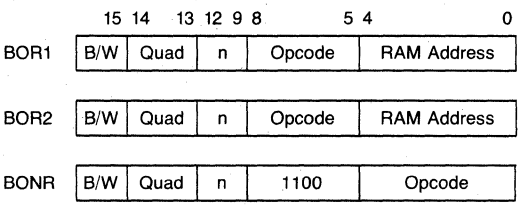
*Shifted Output is loaded into the QLINK.

6

BIT ORIENTED INSTRUCTIONS

The Bit Oriented Instructions contain four indicators; byte or word mode, operation, source/destination, and the bit position of the bit to be operated on (Bit 0 is the least significant bit). It is further subdivided into two types. The first type uses the RAM as both source and destination and has two kinds of formats which differ only by quadrant. The second type does not use the RAM as a source or a destination. Under the control of the instruction inputs, the desired function is performed on the specified source and the result is stored in the specified destination or placed on the Y-bus or both. The operations which can be performed are: Set Bit n which forces the n^{th} bit to a ONE leaving other bits unchanged; Reset Bit n which forces the n^{th} bit to ZERO leaving the other bits unchanged; Test Bit n, which sets the ZERO Status Bit depending on the state of bit n leaving all the bits unchanged; Load 2^n, which loads ONE in Bit position n and ZERO in all other bit positions; Load $\overline{2^n}$ which loads ZERO in bit position n and ONE in all other bit positions; increment by 2^n, which adds 2^n to the operand; and decrement by 2^n which subtracts 2^n from the operand. For all the Load Set, Reset and Test instructions, the N and Z bits are affected and OVR and C bit of the Status register are forced to ZERO. For all arithmetic instructions the LSH (OVR, C, N, Z bits) of the Status register is affected.

BIT ORIENTED FIELD DEFINITIONS



BIT ORIENTED INSTRUCTIONS

Instruction	B/W	Quad	n	Opcode			RAM Address		
BOR1	0 = B 1 = W	11	0 to 15	1101 1110 1111	SETNR RSTNR TSTNR	Set RAM, bit n Reset RAM, bit n Test RAM, bit n	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31
Instruction	**B/W**	**Quad**	**n**	**Opcode**			**RAM Address**		
BOR2	0 = B 1 = W	10	0 to 15	1100 1101 1110 1111	LD2NR LDC2NR A2NR S2NR	$2^n \rightarrow$ RAM $\overline{2^n} \rightarrow$ RAM RAM plus $2^n \rightarrow$ RAM RAM minus $2^n \rightarrow$ RAM	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31
Instruction	**B/W**	**Quad**	**n**				**Opcode**		
BONR	0 = B 1 = W	11	0 to 15	1100			00000 00001 00010 00100 00101 00110 00111 10000 10001 10010 10100 10101 10110 10111	TSTNA RSTNA SETNA A2NA S2NA LD2NA LDC2NA TSTND RSTND SETND A2NDY S2NDY LS2NY LDC2NY	Test ACC, bit n Reset ACC, bit n Set ACC, bit n ACC plus $2^n \rightarrow$ ACC ACC minus $2^n \rightarrow$ ACC $2^n \rightarrow$ ACC $\overline{2^n} \rightarrow$ ACC Test D, bit n Reset D, bit n Set D, bit n D plus $2^n \rightarrow$ Y Bus D minus $\overline{2^n} \rightarrow$ Y Bus $2^n \rightarrow$ Y Bus $\overline{2^n} \rightarrow$ Y Bus

BIT ORIENTED INSTRUCTIONS

Y BUS AND STATUS – BIT ORIENTED INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
BOR1	SETNR	Set RAM Bit n	0 = B	$Y_i \leftarrow RAM_i$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	RSTNR	Reset RAM, Bit n	1 = W	$Y_i \leftarrow RAM_i$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	U
	TSTNR	Test RAM, Bit n		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow SRC_n$	NC	NC	NC	NC	0	U	0	U
BOR2	LD2NR	$2^n \rightarrow$ RAM		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	LDC2NR	$\overline{2^n} \rightarrow$ RAM		$Y_i \leftarrow 1$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	0
	A2NR	RAM + $2^n \rightarrow$ RAM		$Y_i \leftarrow$ RAM + 2^n	NC	NC	NC	NC	U	U	U	U
	S2NR	RAM – $2^n \rightarrow$ RAM		$Y_i \leftarrow$ RAM – 2^n	NC	NC	NC	NC	U	U	U	U
BONR	TSTNA	Test ACC, Bit n		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow ACC_n$	NC	NC	NC	NC	0	U	0	U
	RSTNA	Reset ACC, Bit n		$Y_i \leftarrow ACC_i$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	U
	SETNA	Set ACC, Bit n		$Y_i \leftarrow ACC_i$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	A2NA	ACC + $2^n \rightarrow$ ACC		$Y_i \leftarrow$ ACC + 2^n	NC	NC	NC	NC	U	U	U	U
	S2NA	ACC – $2^n \rightarrow$ ACC		$Y_i \leftarrow$ ACC – 2^n	NC	NC	NC	NC	U	U	U	U
	LD2NA	$2^n \rightarrow$ ACC		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	LDC2NA	$\overline{2^n} \rightarrow$ ACC		$Y_i \leftarrow 1$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	0
	TSTND	Test D, Bit n		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow D_n$	NC	NC	NC	NC	0	U	0	U
	RSTND	Reset D, Bit n*		$Y_i \leftarrow D_i$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	U
	SETND	Set D, Bit n*		$Y_i \leftarrow D_i$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	A2NDY	D + $2^n \rightarrow$ Y Bus		$Y \leftarrow D + 2^n$	NC	NC	NC	NC	U	U	U	U
	S2NDY	D – $2^n \rightarrow$ Y Bus		$Y \leftarrow D - 2^n$	NC	NC	NC	NC	U	U	U	U
	LD2NY	$2^n \rightarrow$ Y Bus		$Y_i \leftarrow 0$ for $i \neq n$; $Y_n \leftarrow 1$	NC	NC	NC	NC	0	U	0	0
	LDC2NY	$\overline{2^n} \rightarrow$ Y Bus		$Y_i \leftarrow 1$ for $i \neq n$; $Y_n \leftarrow 0$	NC	NC	NC	NC	0	U	0	0

SRC = Source
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

*Destination is not D Latch but Y Bus.

ROTATE BY n BITS INSTRUCTIONS

The Rotate by n Bits Instructions contain four indicators: byte or word mode, source, destination and the number of places the source is to be rotated. It is further subdivided into two types. The first type uses RAM as a source and/or a destination and the second type does not use RAM as a source or destination. The first type has two different formats and the only difference is in the quadrant. The second type has only one format as shown in the table. Under the control of instruction inputs, the n indicator specifies the number of bit positions the source is to be rotated up (0 to 15) and the result is either stored in the specified destination or placed on the Y-bus or both. An example of this instruction is given in Figure 4. In the Word mode, all 16-bits are rotated up while in the Byte mode, only lower 8-bits (0-7) are rotated up. In the Word mode, a rotate up by n bits is equivalent to a rotate down by (16-n) bits. Similarly, in the Byte mode a rotate up by n bits is equivalent to a rotate down by (8-n) bits. The N and Z bits of the Status Register are affected and OVR and C bits are forced to ZERO.

EXAMPLE: n = 4, Word Mode

Source	0001	0011	0111	1111
Destination	0011	0111	1111	0001

EXAMPLE: n = 4, Byte Mode

Source	0001	0011	0111	1111
Destination	0001	0011	1111	0111

Figure 4. Rotate by n Example

ROTATE BY n BITS FIELD DEFINITIONS:

	15	14	13	12	9	8	5	4	0
ROTR1	B/W		Quad		n		SRC-Dest		RAM Address
ROTR2	B/W		Quad		n		SRC-Dest		RAM Address
ROTNR	B/W		Quad		n		1100		SRC-Dest

ROTATE BY n BITS INSTRUCTIONS

Instruction	B/W	Quad	n	U[1]		Dest[1]	RAM Address		
ROTR1	0 = B 1 = W	00	0 to 15	1100 1110 1111	RTRA RTRY RTRR	RAM RAM RAM	ACC Y Bus RAM	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31
Instruction	**B/W**	**Quad**	**n**	**U[1]**		**Dest[1]**	**RAM Address**		
ROTR2	0 = B 1 = W	01	0 to 15	0000 0001	RTAR RTDR	ACC D	RAM RAM	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31
Instruction	**B/W**	**Quad**	**n**					**U[1]**	**Dest[1]**
ROTNR	0 = B 1 = W	11	0 to 15	1100			11000 11001 11100 11101	RTDY RTDA RTAY RTAA	D D ACC ACC	Y Bus ACC Y Bus ACC

Note 1: U = Source
Dest = Destination

Y BUS AND STATUS – ROTATE BY n BITS INSTRUCTIONS

Instruction	Opcode	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
ROTR1 ROTR2 ROTNR		1 = W	$Y_i \leftarrow SRC_{(i-n) mod 16}$	NC	NC	NC	NC	0	SRC_{15-n}	0	U
		0 = B	$Y_i \leftarrow SRC_i + 8 = SRC_{(i-n) mod 8}$ for i = 0 to 7	NC	NC	NC	NC	0	SRC_{8-n}	0	U

SRC = Source
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

ROTATE AND MERGE INSTRUCTION

The Rotate and Merge Instructions contain five indicators: byte or word mode, rotated source, non-rotated source/destination, mask and the number of bit positions a source is to be rotated. The function performed by the Rotate and Merge instruction is illustrated in Figure 5. The rotated source, U, is rotated up by the Barrel Shifter n places. The mask input then selects, on a bit by bit basis, the rotated U input or R input. A ZERO in bit i of the mask will select the i^{th} bit of the R input as the i^{th} output bit, while ONE in bit i will select the i^{th} rotated U input as the output bit. The output word is stored in the non-rotated operand location. The N and Z bits are affected. The OVR and C bits of the Status register are forced to ZERO. An example of this instruction is given in Figure 6.

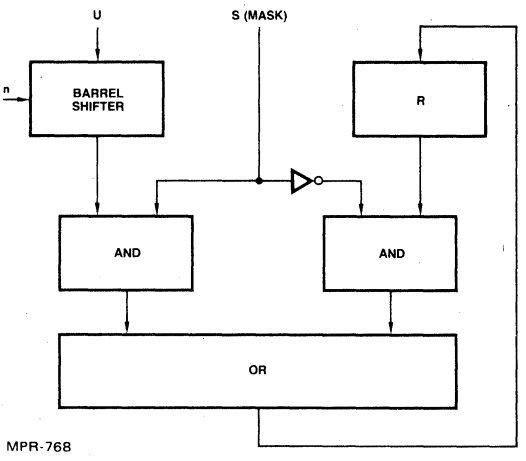


Figure 5. Rotate and Merge Function

EXAMPLE: n = 4, Word Mode

U	0011	0001	0101	0110
Rotated U	0001	0101	0110	0011
R	1010	1010	1010	1010
Mask (S)	0000	1111	0000	1111
Destination	1010	0101	1010	0011

Figure 6. Rotate and Merge Example

ROTATE AND MERGE FIELD DEFINITIONS:

	15 14	13 12 9 8		5 4	0
ROTM	B/W	Quad	n	ROT SRC-Non ROT SRC-Mask	RAM Address

6

ROTATE AND MERGE INSTRUCTION

Instruction	B/W	Quad	n			U[1]	R/Dest[1]	S[1]	RAM Address		
ROTM	0 = B 1 = W	01	0 to 15	0111 1000 1001 1010 1100 1110	MDAI MDAR MDRI MDRA MARI MRAI	D D D D ACC RAM	ACC ACC RAM RAM RAM ACC	I RAM I ACC I I	00000 .. 11111	R00 .. R31	RAM Reg 00 .... RAM Reg 31

Note 1. U = Rotated Source
R/Dest = Non Rotated Source and Destination
S = Mask

Y BUS AND STATUS – ROTATED MERGE

Instruction	Opcode	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
ROTM		1 = W	$Y_i \leftarrow (\text{Non Rot Op})_i \cdot \overline{(\text{mask})_i} + (\text{Rot Op})_{(i-n) \bmod 16} \cdot (\text{mask})_i$	NC	NC	NC	NC	0	U	0	U
		0 = B	$Y_i \leftarrow (\text{Non Rot Op})_i \cdot \overline{(\text{mask})_i} + (\text{Rot Op})_{(i-n) \bmod 8} \cdot (\text{mask})_i$	NC	NC	NC	NC	0	U	0	U

SRC = Source
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

ROTATE AND COMPARE INSTRUCTIONS

The Rotate and Compare Instructions contain five indicators: byte or word mode, rotated source, non-rotated source, mask, and the number of bit positions the rotated source is to be rotated up. Under the control of instruction inputs, the function performed by the Rotate and Compare instruction is illustrated in Figure 7. The rotated operand is rotated by the Barrel Shifter n places. The mask is inverted and ANDed on a bit-by-bit basis with the output of the Barrel Shifter and R input. Thus, a ONE in the mask input eliminates that bit from the comparison. A ZERO allows the comparison. If the comparison passes, the Zero flag is set. If it fails, the Zero flag is reset. The N and Z bit are affected. The OVR and C bits of the Status register are forced to ZERO. An example of this instruction is given in Figure 8.

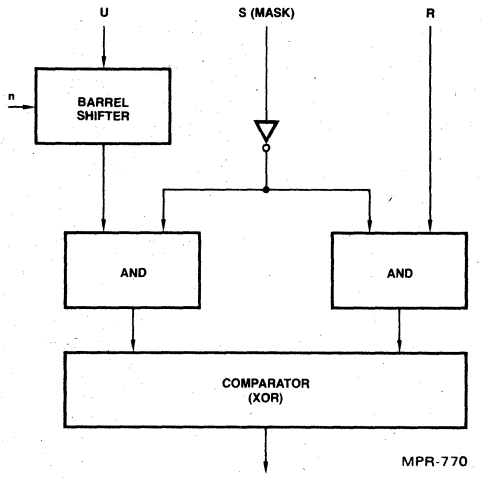


Figure 7. Rotate and Compare Function

EXAMPLE: n = 4, Word Mode

U	0011	0001	0101	0110
U Rotated	0001	0101	0110	0011
R	0001	0101	1111	0000
Mask (S)	0000	0000	1111	1111

Z (status) = 1

Figure 8. Rotate and Compare Examples

ROTATE AND COMPARE FIELD DEFINITIONS

	15 14	13 12	9 8	5 4	0
ROTC	B/W	Quad	n	Rot Src-Non Rot Src-Mask	RAM Address

ROTATE AND COMPARE INSTRUCTIONS

Instruction	B/W	Quad	n			U[1]	R	S[1]	RAM Address		
ROTC	0 = B 1 = W	01	0 to 15	0010 0011 0100 0101	CDAI CDRI CDRA CRAI	D D D RAM	ACC RAM RAM ACC	I I ACC I	00000 .. 11111	R00 .. R31	RAM Reg 00 ... RAM Reg 31

Note 1. U = Rotated Source
R/Dest = Non Rotated Source and Destination
S = Mask

Y BUS AND STATUS – ROTATE AND COMPARE

Instruction	Opcode	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
ROTC		1 = W	$Y_i \leftarrow (\text{Rot Op})_i \cdot \overline{(\text{mask})_i} \oplus (\text{Non Rot Op})_{(i-n) \bmod 16} \cdot (\text{mask})_i$	NC	NC	NC	NC	0	U	0	U
		0 = B	$Y_i \leftarrow (\text{Rot Op})_i \cdot \overline{(\text{mask})_i} \oplus (\text{Non Rot Op})_{(i-n) \bmod 8} \cdot (\text{mask})_i$	NC	NC	NC	NC	0	U	0	U

SRC = Source
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

PRIORITIZE INSTRUCTION

The Prioritize Instructions contain four indicators: byte or word mode, operand source (R), mask source (S) and destination. It is further subdivided into two types. The function performed by the Prioritize instruction is shown in Figure 9. The R operand is ANDed with the complement of the Mask operand. A ZERO in the Mask operand allows the corresponding bit in the R operand to participate in the priority encoding function. A ONE in the Mask operand forces the corresponding bit in the R operand to a ZERO, eliminating it from participation in the priority encoding function.

The priority encoder accepts a 16-bit input and produces a 5-bit binary-weighted code indicating the bit position of the highest priority active bit. If none of the inputs are active, the output is ZERO. In the Word mode, if input bit 15 is active, the output is 1, etc. Figure 10 lists the output as a function of the highest-priority active-bit position in both the Word and Byte mode. The N and Z bits are affected and the OVR and C bits of the status register are forced to ZERO. The only limitation in this instruction is that the operand and the mask must be different sources.

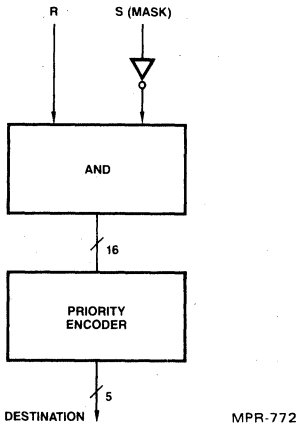


Figure 9. Prioritize Function

WORD MODE		BYTE MODE*	
Highest-Priority Active Bit	Encoder Output	Highest Priority Active Bit	Encoder Output
None	0	None	0
15	1	7	1
14	2	6	2
.	.	.	.
.	.	.	.
1	15	1	7
0	16	0	8

*Bits 8 through 15 do not participate.

Figure 10.

PRIORITZE INSTRUCTION FIELD DEFINITIONS

15 14	13 12	9 8	5 4	0
B/W	Quad	Destination	Source (R)	RAM Address/ Mask (s)
B/W	Quad	Mask (s)	Destination	RAM Address/ Source (R)
B/W	Quad	Mask (s)	Source (R)	RAM Address/ Destination
B/W	Quad	Mask (s)	Source (R)	Destination

PRIORITIZE INSTRUCTION

Instruction	B/W	Quad	Destination			Source (R)			RAM Address/Mask (S)		
PRT1	0 = B 1 = W	10	1000 1010 1011	PRIA PR1Y PR1R	ACC Y Bus RAM	0111 1001	PRT1A PR1D	ACC D	00000 . . . 11111	R00 . . . R31	RAM Reg 00 . . . . RAM Reg 31
Instruction	**B/W**	**Quad**	**Mask (S)**			**Destination**			**RAM Address/Source (R)**		
PRT2	0 = B 1 = W	10	1000 1010 1011	PRA PRZ PRI	ACC 0 I	0000 0010	PR2A PR2Y	ACC Y Bus	00000 . . 11111	R00 . . R31	RAM Reg 00 . . . . RAM Reg 31
Instruction	**B/W**	**Quad**	**Mask (S)**			**Source (R)**			**RAM Address/Dest**		
PRT3	0 = B 1 = W	10	1000 1010 1011	PRA PRZ PRI	ACC 0 I	0011 0100 0110	PR3R PR3A PR3D	RAM ACC D	00000 . . 11111	R00 . . R31	RAM Reg 00 . . . . RAM Reg 31
Instruction	**B/W**	**Quad**	**Mask (S)**			**Source (R)**			**Destination**		
PRTNR	0 = B 1 = W	11	1000 1010 1011	PRA PRZ PRI	ACC 0 I	0100 0110	PRTA PRTD	ACC D	00000 00001	NRY NRA	Y Bus ACC

Y BUS AND STATUS – PRIORITIZE INSTRUCTION

Instruction	Opcode	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
PRT1 PRT2 PRT3 PRTNR		1 = W	$Y_i \leftarrow$ CODE ($SRC_n \cdot \overline{mask_n}$); $Y_m \leftarrow 0$; i = 0 to 4 and n = 0 to 15 m = 5 to 15	NC	NC	NC	NC	0	U	0	U
		0 = B	$Y_i \leftarrow$ CODE ($SRC_n \cdot \overline{mask_n}$); $Y_m \leftarrow 0$; i = 0 to 2 and n = 0 to 7 m = 3 to 15	NC	NC	NC	NC	0	U	0	U

SRC = Source NC = No Change 1 = Set
U = Update 0 = Reset i = 0 to 15 when not specified

CRC INSTRUCTION

The CRC (Cyclic-Redundancy-Check) Instructions contain one indicator: address of a RAM register to use as the check sum register. The CRC instruction provides a method for generation of the check bits in a CRC calculation. Two CRC instructions are provided-CRC Forward and CRC Reverse. The reason for providing two instructions is that CRC standards do not specify which data bit is to be transmitted first, the LSB or the MSB, but they do specify which check bit must be transmitted first. Figure 11 illustrates the method used to generate these check bits for the CRC Forward function and Figure 12 illustrates method used for the CRC Reverse function. The ACC serves as a polynomial mask to define the generating polynomial while the RAM register holds the partial result and eventually the calculated check sum. The LINK-bit is used as the serial input. The serial input combines with the MSB of the check-sum register, according to the polynomial defined by the polynomial mask register. When the last input bit has been processed, the check-sum register contains the CRC check bits. The LINK, N and Z bits are affected and the OVR and C bits of the Status register are forced to ZERO.

CYCLIC-REDUNDANCY-CHECK FIELD DEFINITIONS:

	15	14	13	12	9	8	5	4	0
CRCF	1	Quad	0110		0011		RAM Address		
CRCR	1	Quad	0110		1001		RAM Address		

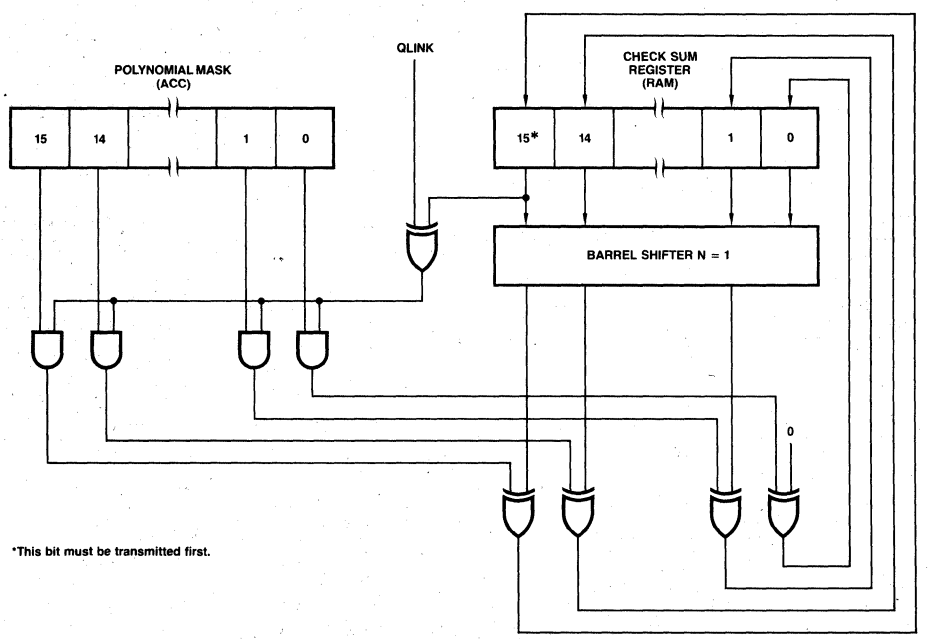


Figure 11. CRC Forward Function

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CRC INSTRUCTION

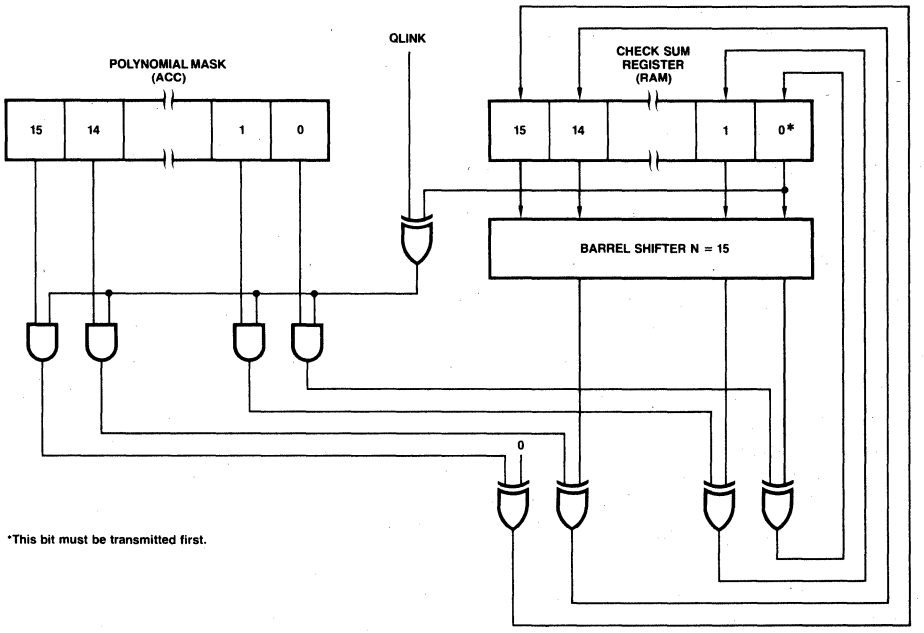

Figure 12. CRC Reverse Function

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CYCLIC REDUNDANCY CHECK

Instruction	B/W	Quad			RAM Address		
CRCF	1	10	0110	0011	00000 •• 11111	R00 •• R31	RAM Reg 00 •••• RAM Reg 31
Instruction	**B/W**	**Quad**			**RAM Address**		
CRCR	1	10	0110	1001	00000 •• 11111	R00 •• R31	RAM Reg 00 •••• RAM Reg 31

Y BUS AND STATUS – CYCLIC REDUNDANCY CHECK

Instruction	Opcode	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
CRCF		1 = W	$Y_i \leftarrow [(QLINK \oplus RAM_{15}) \cdot ACC_i] \oplus RAM_{i-1}$ for i = 15 to 1 $Y_0 \leftarrow [(QLINK \oplus RAM_{15}) \cdot ACC_0] \oplus 0$	NC	NC	NC	RAM_{15}*	0	U	0	U
CRCR		1 = W	$Y_i \leftarrow [(QLINK \oplus RAM_0) \cdot ACC_i] \oplus RAM_{i+1}$ for i = 14 to 0 $Y_{15} \leftarrow [(QLINK \oplus RAM_0) \cdot ACC_{15}] \oplus 0$	NC	NC	NC	RAM_0*	0	U	0	U

SRC = Source
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

*QLINK is loaded with the shifted out bit from the checksum register.

STATUS INSTRUCTIONS

Status Instructions – The Set Status Instruction contains a single indicator. This indicator specifies which bit or group of bits, contained in the status register (Figure 13), are to be set (forced to a ONE).

7	6	5	4	3	2	1	0
Flag3	Flag2	Flag1	LINK	OVR	N	C	Z

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Figure 13. Status Byte

The Reset Status Instruction contains a single indicator. This indicator specifies which bit or group of bits, contained in the status register are to be reset (forced to ZERO).

The Store Status Instruction contains two indicators; byte/word and a second indicator that specifies the destination of the status register. The Store Status Instruction allows the status of the processor to be saved and restored later, which is an especially useful function for interrupt handling.

The status register is always stored in the lower byte of the RAM or the ACC register. Depending upon byte or word mode the upper byte is unchanged or loaded with all ZEROs respectively.

The Load Status instructions are included in the single operand instruction type.

The Test Status Instructions contain a single indicator which specifies which one of the 12 possible test conditions are to be placed on the Conditional-Test output. Besides the eight bits in the Status register (QZ, QC, QN, QOVR, QLINK, QFlag1, QFlag2, and QFlag3), four logical functions (QN ⊕ QOVR, (QN ⊕ QOVR) + QZ, QZ + $\overline{QC}$ and LOW may also be selected. These functions are useful in testing results of Two's Complement and unsigned number arithmetic operations. The status register may also be tested via the bidirectional T bus. The code to test the status register via T bus is similar to the code used by instruction lines I_1 to I_4 as shown below. Instruction lines I_{0-4} have priority over T bus for testing the status register on CT output. See the discussion on the status register for a full description.

T_4 I_4	T_3 I_3	T_2 I_2	T_1 I_1	CT
0	0	0	0	(N ⊕ OVR) + Z
0	0	0	1	N ⊕ OVR
0	0	1	0	Z
0	0	1	1	OVR
0	1	0	0	LOW
0	1	0	1	C
0	1	1	0	Z + $\overline{C}$
0	1	1	1	N
1	0	0	0	LINK
1	0	0	1	Flag1
1	0	1	0	Flag2
1	0	1	1	Flag3

STATUS:

	15	14	13	12	9	8	5	4	0
SETST	0		Quad	1011	1010		Opcode		
RSTST	0		Quad	1010	1010		Opcode		
SVSTR	B/W		Quad	0111	1010		RAM Address/Dest		
SVSTNR	B/W		Quad	0111	1010		Destination		

STATUS INSTRUCTIONS

Instruction	B/W	Quad			Opcode		
SETST	0	11	1011	1010	00011 00101 00110 01001 01010	SONCZ SL SF1 SF2 SF3	Set OVR, N, C, Z Set LINK Set Flag1 Set Flag2 Set Flag3
Instruction	**B/W**	**Quad**			**Opcode**		
RSTST	0	11	1010	1010	00011 00101 00110 01001 01010	RONCZ RL RF1 RF2 RF3	Reset OVR, N, C, Z Reset LINK Reset Flag1 Reset Flag2 Reset Flag3
Instruction	**B/W**	**Quad**			**RAM Address/Dest**		
SVSTR	0 = B 1 = W	10	0111	1010	00000 •• 11111	R00 •• R31	RAM Reg 00 •••• RAM Reg 31
					Destination		
SVSTNR	0 = B 1 = W	11	0111	1010	00000 00001	NRY NRA	Y Bus ACC

STATUS INSTRUCTIONS

Instruction	B/W	Quad			Opcode (CT)		
Test	0	11	1001	1010	00000	TNOZ	Test (N⊕OVR) + Z
					00010	TNO	Test N⊕OVR
					00100	TZ	Test Z
					00110	TOVR	Test OVR
					01000	TLOW	Test LOW
					01010	TC	Test C
					01100	TZC	Test Z + $\overline{C}$
					01110	TN	Test N
					10000	TL	Test LINK
					10010	TF1	Test Flag1
					10100	TF2	Test Flag2
					10110	TF3	Test Flag3

Note: $\overline{IEN}$ • test status instruction has priority over T_{1-4} instruction.

Y BUS AND STATUS – FOR STATUS INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
SETST	SONCZ	Set OVR, N, C, Z	0 = B	$Y_i \leftarrow 1$ for i = 0 to 15	NC	NC	NC	NC	1	1	1	1
	SL	Set LINK			NC	NC	NC	1	NC	NC	NC	NC
	SF1	Set Flag1			NC	NC	1	NC	NC	NC	NC	NC
	SF2	Set Flag2			NC	1	NC	NC	NC	NC	NC	NC
	SF3	Set Flag3			1	NC	NC	NC	NC	NC	NC	NC
RSTST	RONCZ	Reset OVR, N, C, Z	0 = B	$Y_i \leftarrow 0$ for i = 0 to 15	NC	NC	NC	NC	0	0	0	0
	RL	Reset LINK			NC	NC	NC	0	NC	NC	NC	NC
	RF1	Reset Flag1			NC	NC	0	NC	NC	NC	NC	NC
	RF2	Reset Flag2			NC	0	NC	NC	NC	NC	NC	NC
	RF3	Reset Flag3			0	NC	NC	NC	NC	NC	NC	NC
SVSTR SVSTNR		Save Status*	0 = B 1 = W	$Y_i \leftarrow$ Status$_i$ for i = 0 to 7; $Y_i \leftarrow 0$ for i = 8 to 15	NC	NC	NC	NC	NC	NC	NC	NC

SRC = Source
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

*In byte mode only the lower byte from the Y bus is loaded into the RAM or ACC and in word mode all 16-bits from the Y bus are loaded into the RAM or ACC.

Y BUS AND STATUS – FOR STATUS TEST INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
Test	TNOZ	Test (N⊕OVR) + Z	0 = B	*	NC	NC	NC	NC	NC	NC	NC	NC
	TNO	Test N⊕OVR			NC	NC	NC	NC	NC	NC	NC	NC
	TZ	Test Z			NC	NC	NC	NC	NC	NC	NC	NC
	TOVR	Test OVR			NC	NC	NC	NC	NC	NC	NC	NC
	TLOW	Test LOW			NC	NC	NC	NC	NC	NC	NC	NC
	TC	Test C			NC	NC	NC	NC	NC	NC	NC	NC
	TZC	Test Z + $\overline{C}$			NC	NC	NC	NC	NC	NC	NC	NC
	TN	Test N			NC	NC	NC	NC	NC	NC	NC	NC
	TL	Test LINK			NC	NC	NC	NC	NC	NC	NC	NC
	TF1	Test Flag1			NC	NC	NC	NC	NC	NC	NC	NC
	TF2	Test Flag2			NC	NC	NC	NC	NC	NC	NC	NC
	TF3	Test Flag3										

*Y-Bus is undefined

SRC = Source
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

NO-OP INSTRUCTION

The NO-OP Instruction has a fixed 16-bit code. This instruction does not change any internal registers in the Am29116. It preserves the status register, RAM register and the ACC register.

NO OPERATION FIELD DEFINITION:

	15 14	13 12	9 8	5 4	0
NOOP	0	11	1000	1010	00000

NO-OP INSTRUCTION

Instruction	B/W	Quad			
NOOP	0	11	1000	1010	00000

Y BUS AND STATUS – NO-OP INSTRUCTION

Instruction	Opcode	B/W	Y – Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
NOOP		0 = B	*	NC	NC	NC	NC	NC	NC	NC	NC

SRC = Source
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

*Y-Bus is undefined.

SUMMARY OF MNEMONICS

Instruction Type

SOR	Single Operand RAM
SONR	Single Operand Non-RAM
TOR1	Two Operand RAM (Quad 0)
TOR2	Two Operand RAM (Quad 2)
TONR	Two Operand Non-RAM
SHFTR	Single Bit Shift RAM
SHFTNR	Single Bit Shift Non-RAM
ROTR1	Rotate n Bits RAM (Quad 0)
ROTR2	Rotate n Bits RAM (Quad 1)
ROTNR	Rotate n Bits Non-RAM
BOR1	Bit Oriented RAM (Quad 3)
BOR2	Bit Oriented RAM (Quad 2)
BONR	Bit Oriented Non-RAM
ROTM	Rotate and Merge
ROTC	Rotate and Compare
PRT1	Prioritize RAM; Type 1
PRT2	Prioritize RAM; Type 2
PRT3	Prioritize RAM; Type 3
PRTNR	Prioritize Non-RAM
CRCF	Cyclic Redundancy Check Forward
CRCR	Cyclic Redundancy Check Reverse
NOOP	No Operation
SETST	Set Status
RSTST	Reset Status
SVSTR	Save Status RAM
SVSTNR	Save Status Non-RAM
TEST	Test Status

SOURCE AND DESTINATION

Single Operand

SORA	Single Operand RAM to ACC
SORY	Single Operand RAM to Y Bus
SORS	Single Operand RAM to Status
SOAR	Single Operand ACC to RAM
SODR	Single Operand D to RAM
SOIR	Single Operand I to RAM
SOZR	Single Operand 0 to RAM
SOZER	Single Operand D(0E) to RAM
SOSER	Single Operand D(SE) to RAM
SORR	Single Operand RAM to RAM
SOA	Single Operand ACC
SOD	Single Operand D
SOI	Single Operand I
SOZ	Single Operand 0
SOZE	Single Operand D(0E)
SOSE	Single Operand D(SE)
NRY	Non-RAM Y Bus
NRA	Non-RAM ACC
NRS	Non-RAM Status
NRAS	Non-RAM ACC, Status

Two Operand

TORAA	Two Operand RAM, ACC to ACC
TORIA	Two Operand RAM, I to ACC
TODRA	Two Operand D, RAM to ACC
TORAY	Two Operand RAM, ACC to Y Bus
TORIY	Two Operand RAM, I to Y Bus
TODRY	Two Operand D, RAM to Y Bus
TORAR	Two Operand RAM, ACC to RAM
TORIR	Two Operand RAM, I to RAM
TODRR	Two Operand D, RAM to RAM
TODAR	Two Operand D, ACC to RAM
TOAIR	Two Operand ACC, I to RAM
TODIR	Two Operand D, I to RAM
TODA	Two Operand D, ACC
TOAI	Two Operand ACC, I
TODI	Two Operand D, I

Single Bit Shift

SHRR	Shift RAM, Store in RAM
SHDR	Shift D, Store in RAM
SHA	Shift ACC
SHD	Shift D

Rotate n Bits

RTRA	Rotate RAM, Store in ACC
RTRY	Rotate RAM, Place on Y Bus
RTRR	Rotate RAM, Store in RAM
RTAR	Rotate ACC, Store in RAM
RTDR	Rotate D, Store in RAM
RTDY	Rotate D, Place on Y Bus
RTDA	Rotate D, Store in ACC
RTAY	Rotate ACC, Place on Y Bus
RTAA	Rotate ACC, Store in ACC

Rotate and Merge

MDAI	Merge Disjoint Bits of D and ACC Using I as Mask and Store in ACC
MDAR	Merge Disjoint Bits of D and ACC Using RAM as Mask and Store in ACC
MDRI	Merge Disjoint Bits of D and RAM Using I as Mask and Store in RAM
MDRA	Merge Disjoint Bits of D and RAM Using ACC as Mask and Store in RAM
MARI	Merge Disjoint Bits of ACC and RAM Using I as Mask and Store in RAM
MRAI	Merge Disjoint Bits of RAM and ACC Using I as Mask and Store in ACC

Rotate and Compare

CDAI	Compare Unmasked Bits of D and ACC Using I as Mask
CDRI	Compare Unmasked Bits of D and RAM Using I as Mask
CDRA	Compare Unmmasked Bits of D and RAM Using ACC as Mask
CRAI	Compare Unmasked Bits of RAM and ACC Using I as Mask

Prioritize

PR1A	ACC as Destination for Prioritize Type 1
PR1Y	Y Bus as Destination for Prioritize Type 1
PR1R	RAM as Destination for Prioritize Type 1
PRT1A	ACC as Source for Prioritize Type 1
PR1D	D as Source for Prioritize Type 1
PR2A	ACC as Destination for Prioritize Type 2
PR2Y	Y Bus as Destination for Prioritize Type 2
PR3R	RAM as Source for Prioritize Type 3
PR3A	ACC as Source for Prioritize Type 3
PR3D	D as Source for Prioritize Type 3
PRTA	ACC as Source for Prioritize Type Non-RAM
PRTD	D as Source for Prioritize Type Non-RAM
PRA	ACC as Mask for Prioritize Type 2, 3, and Non-RAM

SUMMARY OF MNEMONICS

PRZ	Mask Equal to Zero for Prioritize Type 2, 3, and Non-RAM
PRI	I as Mask for Prioritize Type 2, 3, and Non-RAM

OPCODE

Addition

ADD	Add without Carry
ADDC	Add with Carry
A2NA	Add 2^n to ACC
A2NR	Add 2^n to RAM
A2NDY	Add 2^n to D, Place on Y Bus

Subtraction

SUBR	Subtract R from S without Carry
SUBRC	Subtract R from S with Carry
SUBS	Subtract S from R without Carry
SUBSC	Subtract S from R with Carry
S2NR	Subtract 2^n from RAM
S2NA	Subtract 2^n from ACC
S2NDY	Subtract 2^n from D, Place on Y Bus

Logical Operations

AND	Boolean AND
NAND	Boolean NAND
EXOR	Boolean EXOR
NOR	Boolean NOR
OR	Boolean OR
EXNOR	Boolean EXNOR

SHIFTS

SHUPZ	Shift Up Towards MSB with 0 Insert
SHUP1	Shift Up Towards MSB with 1 Insert
SHUPL	Shift Up Towards MSB with LINK Insert
SHDNZ	Shift Down Towards LSB with 0 Insert
SHDN1	Shift Down Towards LSB with 1 Insert
SHDNL	Shift Down Towards LSB with LINK Insert
SHDNC	Shift Down Towards LSB with Carry Insert
SHDNOV	Shift Down Towards LSB with Sign EXOR Overflow Insert

Loads

LD2NR	Load 2^n into RAM
LDC2NR	Load $\overline{2^n}$ into RAM
LD2NA	Load 2^n into ACC
LDC2NA	Load $\overline{2^n}$ into ACC
LD2NY	Place 2^n on Y Bus
LDC2NY	Place $\overline{2^n}$ on Y Bus

Bit Oriented

SETNR	Set RAM, Bit n
SETNA	Set ACC, Bit n
SETND	Set D, Bit n
SONCZ	Set OVR, N, C, Z, in Status Register
SL	Set LINK Bit in Status Register
SF1	Set Flag1 Bit in Status Register
SF2	Set Flag2 Bit in Status Register
SF3	Set Flag3 Bit in Status Register
RSTNR	Reset RAM, Bit n
RSTNA	Reset ACC, Bit n
RSTND	Reset D, Bit n
RONCZ	Reset OVR, N, C, Z, in Status Register
RL	Reset LINK Bit in Status Register
RF1	Reset Flag1 Bit in Status Register
RF2	Reset Flag2 Bit in Status Register
RF3	Reset Flag3 Bit in Status Register
TSTNR	Test RAM, Bit n
TSTNA	Test ACC, Bit n
TSTND	Test D, Bit n

Arithmetic Operations

MOVE	Move and Update Status
COMP	Complement (1's Complement)
INC	Increment
NEG	Two's Complement

Conditional Test

TNOZ	Test $(N \oplus OVR) + Z$
TNO	Test $N \oplus OVR$
TZ	Test Zero Bit
TOVR	Test Overflow Bit
TLOW	Test for LOW
TC	Test Carry Bit
TZC	Test $Z + \overline{C}$
TN	Test Negative Bit
TL	Test LINK Bit
TF1	Test Flag1 Bit
TF2	Test Flag2 Bit
TF3	Test Flag3 Bit

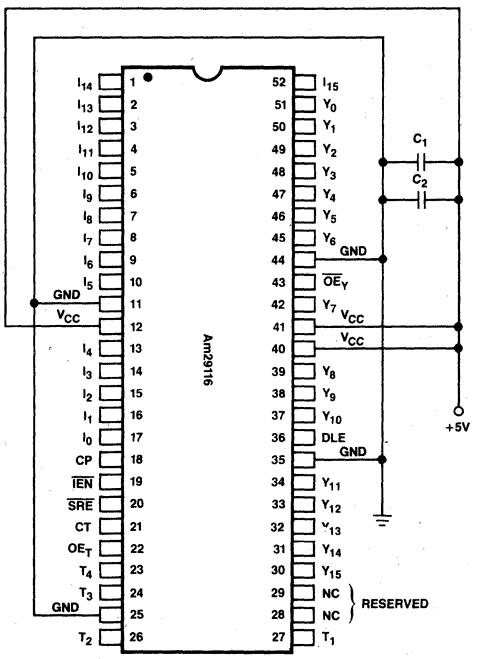
MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Case) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} MAX
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

OPERATING RANGE

P/N	Range	Temperature	V_{CC}
AM29116DC, DCB	Commercial	T_A = 0 to +70°C	V_{CC} = 5.0V ±5% (MIN = 4.75V, MAX = 5.25V)
AM29116DM, DMB	Military	T_C = −55 to +125°C	V_{CC} = 5.0V ±10% (MIN = 4.50V, MAX = 5.50V)

V_{CC} AND GROUND PIN CONNECTIONS



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Notes: 1. All V_{CC} and all GND pins must be connected as shown. Offsets between any two V_{CC} pins or between any two GND pins should be avoided.
2. C_1 = 1.0μF, C_2 = 0.01μF.
The C_1 and C_2 capacitors should be used to shunt low- and high-frequency noise from V_{CC}. Do not replace with one capacitor.

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL}	Y_{0-15} T_{1-4} CT	I_{OH} −1.6mA, COM'L −1.2mA, MIL	2.4 2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL}	Y_{0-15} T_{1-4} CT	I_{OL} (COM'L/MIL) 16mA/12mA			0.5	Volts
V_{IH}	Guaranteed Input Logical HIGH Voltage (Note 6)		All Inputs		2.0			Volts
V_{IL}	Guaranteed Input Logical LOW Voltage (Note 6)		All Inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN	All Inputs	I_{IN} −18mA			−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX V_{IN} = 0.5 Volts (Note 4)	$\overline{IEN}$ $\overline{SRE}$ DLE I_{0-4} I_{5-15} $\overline{OE}_T$ $\overline{OE}_Y$ CP T_{1-4} Y_{0-15}				−0.50 −0.50 −1.00 −1.00 −0.50 −0.50 −0.50 −1.50 −0.55 −0.55	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX V_{IN} = 2.4 Volts (Note 4)	$\overline{IEN}$ $\overline{SRE}$ DLE I_{0-4} I_{5-15} $\overline{OE}_T$ $\overline{OE}_Y$ CP T_{1-4} Y_{0-15}				50 50 100 100 50 50 50 150 100 100	μA
I_I	Input HIGH Current	V_{CC} = MAX V_{IN} = 5.5 Volts	All Inputs				1.0	mA
I_{OZH}	Off State (HIGH Impedance) Output Current	V_{CC} = MAX V_O = 2.4 Volts (Note 4)	T_{1-4} Y_{0-15}				100	μA
I_{OZL}	Off State (HIGH Impedance) Output Current	V_{CC} = MAX V_O = 0.5 Volts (Note 4)	T_{1-4} Y_{0-15}				−550	μA
I_{OS}	Output Short Circuit Current	V_{CC} = MAX +0.5 Volts V_O = 0.5 Volts (Note 3)			−30		−85	mA
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX		T_A = 25°C		595		mA
			COM'L	T_A = 0 to 70°C (Note 7)			735	
				T_A = 70°C			535	
			MIL	T_C = −55 to 125°C (Note 7)			745	
				T_C = 125°C			485	

Notes:
1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Range for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Y_{0-15}, T_{1-4} are three-state outputs internally connected to TTL inputs. Input characteristics are measured under conditions such that the outputs are in the OFF state.
5. Worst case I_{CC} is at minimum temperature.
6. These input levels provide zero noise immunity and should be tested only in a static, noise-free environment.
7. Cold start.

SWITCHING CHARACTERISTICS

The tables below define the Am29116 switching characteristics. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in nsec. All outputs have maximum DC loading.

TYPICAL ROOM TEMPERATURE CHARACTERISTICS

(T_A = 25°C; V_{CC} = 5.0V, C_L = 50pF)

A. Combinational Delays (nsec)

		Outputs		
		Y_{0-15}	T_{1-4}	CT
	I_{0-4} (ADDR)	55	56	–
	I_{0-15} (DATA)	55	56	–
	I_{0-15} (INSTR)	55	56	29
Input	DLE	37**	39	–
	T_{1-4}	–	–	25
	CP	40	40	24
	Y_{0-15}	37**	39*	–
	$\overline{IEN}$	–	–	27

*Y_{0-15} must be stored in the Data Latch and its source disabled before the delay to Y_{0-15} as an output can be measured.
**Guaranteed indirectly by other tests.

B. Enable/Disable Times (nsec) (C_L = 5pF for disable only)

From Input	To Output	Enable		Disable	
		t_{PZH}	t_{PZL}	t_{PHZ}	t_{PLZ}
$\overline{OE}_Y$	Y_{0-15}	11	13	18	13
OE_T	T_{1-4}	14	20	22	18

C. Clock and Pulse Requirements (nsec)

Input	Min Low Time	Min High Time
CP	10	8
DLE	–	10
$\overline{IEN}$	10	–

D. Setup and Hold Times (nsec)

Input	With Respect to	High-to-Low Transition				Low-to-High Transition				Comment	
		Setup		Hold		Setup		Hold			
I_{0-4} (RAM ADDR)	CP	(t_{s1}) 12		(t_{h1}) 0		–		–		Single ADDR (Source)	
I_{0-4} (RAM ADDR)	CP and $\overline{IEN}$ both LOW	(t_{s2}) 5		Do Not Change				(t_{h7}) 0		Two ADDR (Destination)	
I_{0-15} (DATA)	CP	–		–		(t_{s8}) 45		(t_{h8}) 0			
I_{0-15} (INSTR)	CP	(t_{s3}) 27		(t_{h3})† 5		(t_{s9}) 45		(t_{h9}) 0			
$\overline{IEN}$ HIGH	CP	(t_{s4}) 5		–		–		(t_{h10}) 0		Disable	
$\overline{IEN}$ LOW	CP	–	(t_{s5}) 10	–	(t_{h5})† 0	(t_{s11}) 11	–	(t_{h11})†† 0	–	Enable	Immediate first cycle
$\overline{SRE}$	CP	–		–		(t_{s12}) 7		(t_{h12}) 0			
Y	CP	–		–		(t_{s13}) 29		(t_{h13}) 0			
Y	DLE	(t_{s6}) 5		(t_{h6}) 2		–		–			
DLE	CP	–		–		(t_{s14}) 30		(t_{h14}) 0			

†Timing for immediate instruction for the first cycle.
††Status register and accumulator destination only.

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SWITCHING CHARACTERISTICS (Cont.)

PRELIMINARY CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

(T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V, C_L = 50pF)

A. Combinational Delays (nsec)

		Outputs		
		Y_{0-15}	T_{1-4}	CT
	I_{0-4} (ADDR)	79	84	–
	I_{0-15} (DATA)	79	84	–
	I_{0-15} (INSTR)	79	84	48
Input	DLE	58**	60	–
	T_{1-4}	–	–	39
	CP	56	62	36
	Y_{0-15}	62**	64*	–
	$\overline{IEN}$	–	–	43

*Y_{0-15} must be stored in the Data Latch and is source disabled before the delay to Y_{0-15} as an output can be measured.
**Guaranteed indirectly by other tests.

B. Enable/Disable Times (nsec)
(C_L = 5pF for disable only)

From Input	To Output	Enable		Disable	
		t_{PZH}	t_{PZL}	t_{PHZ}	t_{PLZ}
$\overline{OE}_Y$	Y_{0-15}	20	20	20	20
OE_T	T_{1-4}	25	25	25	25

C. Clock and Pulse Requirements (nsec)

Input	Min Low Time	Min High Time
CP	20	30
DLE	–	15
$\overline{IEN}$	22	–

D. Setup and Hold Times (nsec)

Input	With Respect to	High-to-Low Transition				Low-to-High Transition				Comment	
		Setup		Hold		Setup		Hold			
I_{0-4} (RAM ADDR)	CP	(t_{s1}) 24		(t_{h1}) 0		–		–		Single ADDR (Source)	
I_{0-4} (RAM ADDR)	CP and $\overline{IEN}$ both LOW	(t_{s2}) 10		Do Not Change				(t_{h7}) 0		Two ADDR (Destination)	
I_{0-15} (DATA)	CP	–		–		(t_{s8}) 65		(t_{h8}) 0			
I_{0-15} (INSTR)	CP	(t_{s3}) 38†		(t_{h3})† 17		(t_{s9}) 65		(t_{h9}) 0			
$\overline{IEN}$ HIGH	CP	(t_{s4}) 10		–		–		(t_{h10}) 0		Disable	
$\overline{IEN}$ LOW	CP	–	(t_{s5}) 20	–	(t_{h5})† 0	(t_{s11}) 22	–	(t_{h11})†† 0	–	Enable	Immediate first cycle
$\overline{SRE}$	CP	–		–		(t_{s12}) 17		(t_{h12}) 0			
Y	CP	–		–		(t_{s13}) 44		(t_{h13}) 0			
Y	DLE	(t_{s6}) 10		(t_{h6}) 6		–		–			
DLE	CP	–		–		(t_{s14}) 42		(t_{h14}) 0			

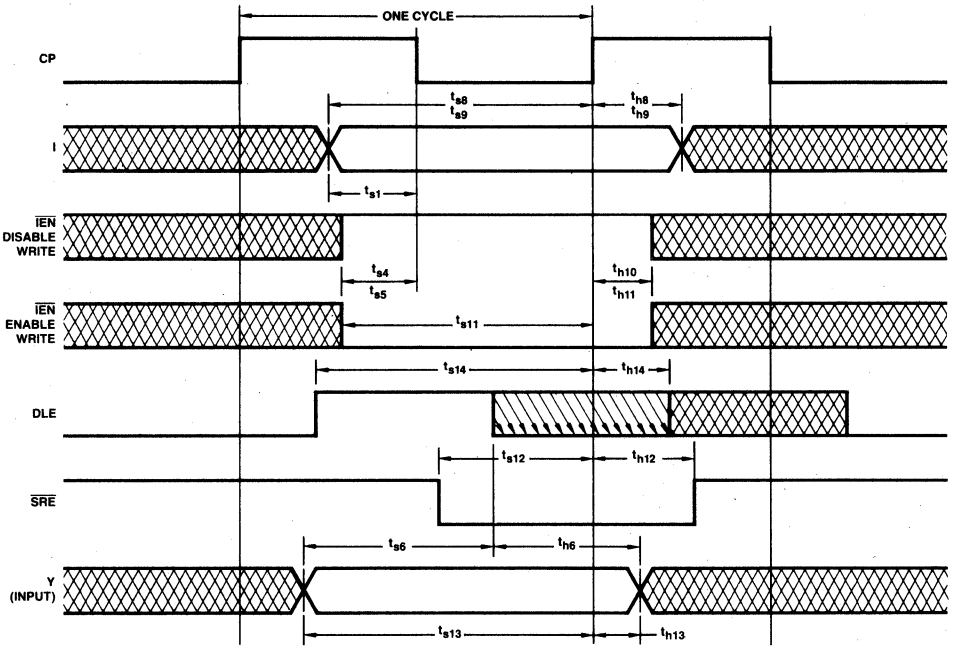
†Timing for immediate instruction for the first cycle.
††Status register and accumulator destination only.

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5–8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

Am29116
SINGLE ADDRESS ACCESS TIMING



If t_{h6} is satisfied, t_{h13} need not be satisfied.

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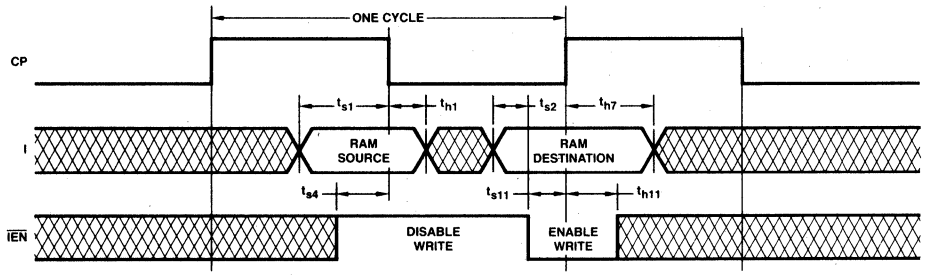
DOUBLE ADDRESS ACCESS TIMING



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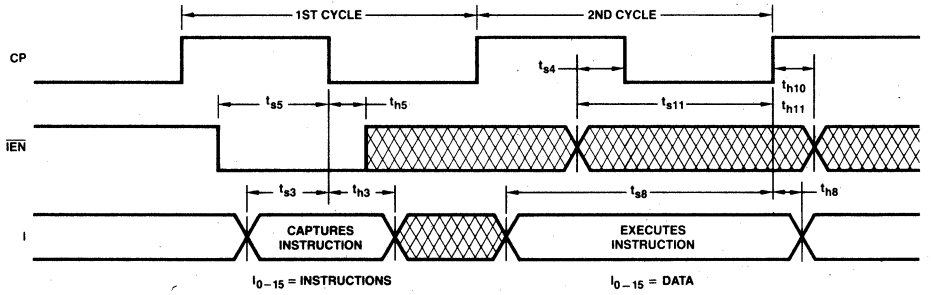
IMMEDIATE INSTRUCTION CYCLE TIMING



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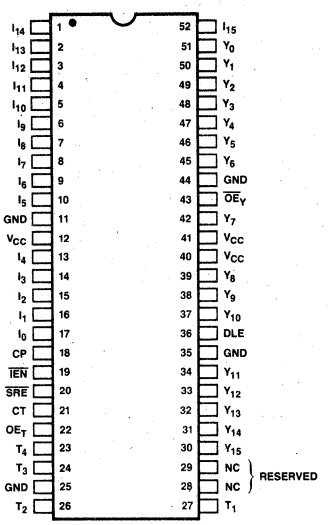
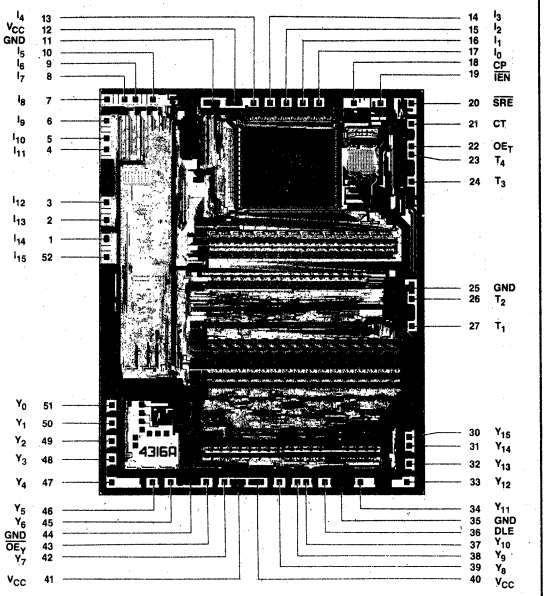
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation. MPR-812

METALLIZATION AND PAD LAYOUT



ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am29116 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM29116DC	D-52	C	C-1
AM29116DC-B	D-52	C	B-2 (Note 4)
AM29116DM	D-52	M	C-3
AM29116DM-B	D-52	M	B-3
AM29116XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM29116XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V.
   M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

THE USE OF AN EXTERNAL STATUS REGISTER IN REDUCING MICROCYCLE LENGTH

The standard connection of the CT pin of the Am29116 and microcycle length calculation arising from that connection are shown below:

CRITICAL PATH TIMING (Figure A)

Part Number	Path	Maximum Commercial Delay (ns)
Pipeline Register	CP → Q	12
Am29116	T → CT	39
Fast MUX	SEL or D_{IN} → Y	20
Am2910-1	$\overline{CC}$ → Y	30
Am27S35 (Registered PROM)	PROM access time and Pipeline Register Setup	40
		141

While 141ns cycle is quite fast, it can be improved by using an external register for status testing.

CRITICAL PATH TIMING (Figure B)

Part Number	Path	Maximum Commercial Delay (ns)
Am298XX Status Register	CP → Y	12
Fast MUX	SEL or D_{IN} → Y	20
Am2910-1	$\overline{CC}$ → Y	30
Am27S35	PROM Access Time	40
		102

The cycle time has been reduced from 141 to 102ns.

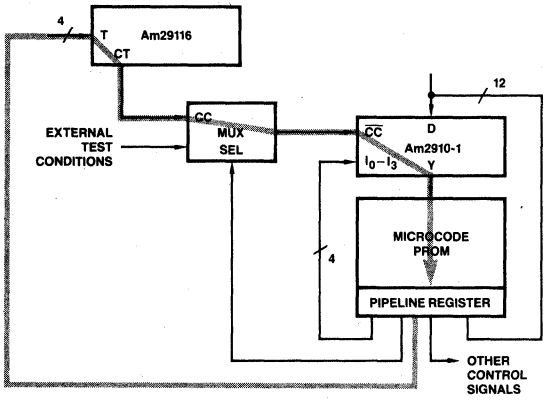


Figure A.

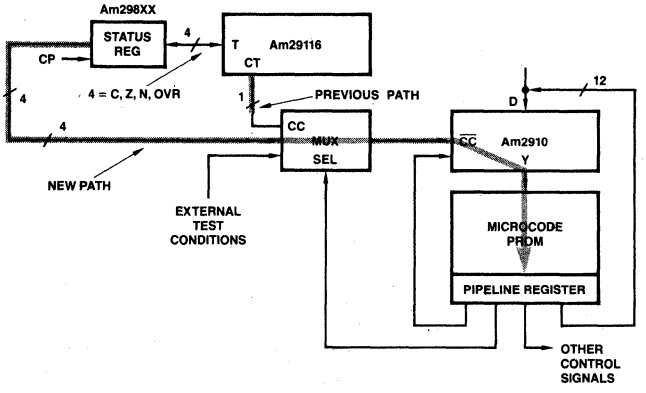


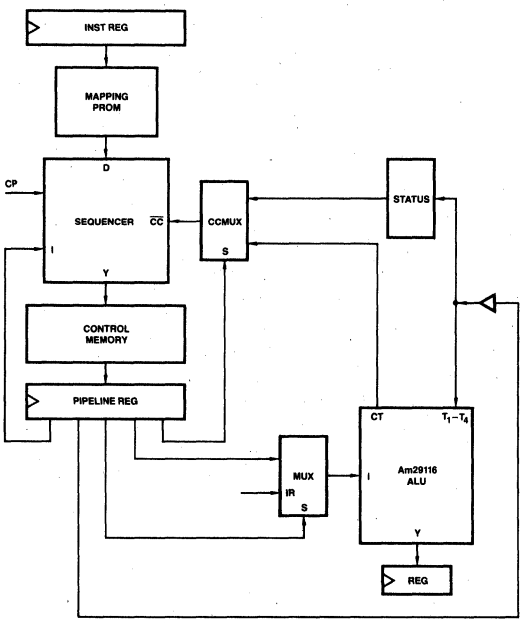
Figure B.

Am29116 System Cycle Times

Based on the preliminary commercial AC timing for the 29116, system microcycle times are estimated and included in the next few pages. Several observations can be made as follows:

1. The data path microcycle is roughly 110ns (even for Y-bus input/output in a single cycle). This will increase if external multiplexers (e.g., for 2 address, N-count register) or other system glues are used.
2. The control path is the system bottleneck.
   a. If CT from the 29116 is used, cycle time will be in the 169ns (2910) range.
   b. A lookahead scheme (placing a flip-flop in front of the sequencer $\overline{CC}$ input), will decrease the cycle time. This causes conditional branches to have different test condition setup requirements (single cycle for simple status, two cycles for a complex test), which is undesirable for most applications.
   c. The sensible way is to use an external status register and a 2925 at maximum speed (31MHz) for variable cycle control. For example, in a 2910-1 system, one can switch between divide by 4 and by 5, to get 132 and 165ns cycle respectively for conditional branch using status register and CT from 29116.

SYSTEM BLOCK DIAGRAM



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DATA PATH TIMING ANALYSIS

I. Without Any External Logic

a. Pipeline Register	(29821)	CP-Q	12ns	
RALU	(29116)	I-T_{1-4}	84	
Status Register	(29821)	Setup	4	
			100ns	
b. Pipeline Register	(29821)	CP-Q	12ns	
RALU	(29116)	I-Y	79	
Data Register	(29821)	Setup	4	
			95ns	

II. With Multiplexers for Address, N-Count, etc.

a. Pipeline Register	(29821)	CP-Q	12ns	
Multiplexer	(S157)	Sel-Y	20	
RALU	(29116)	I-T_{1-4}	84	
Status Register	(29821)	Setup	4	
			120ns	
b. Pipeline Register	(29821)	CP-Q	12ns	
Multiplexer	(S157)	Sel-Y	20	
RALU	(29116)	I-Y	79	
Data Register	(29821)	Setup	4	
			115ns	

III. Using Y-Bus as Input/Output in One Cycle

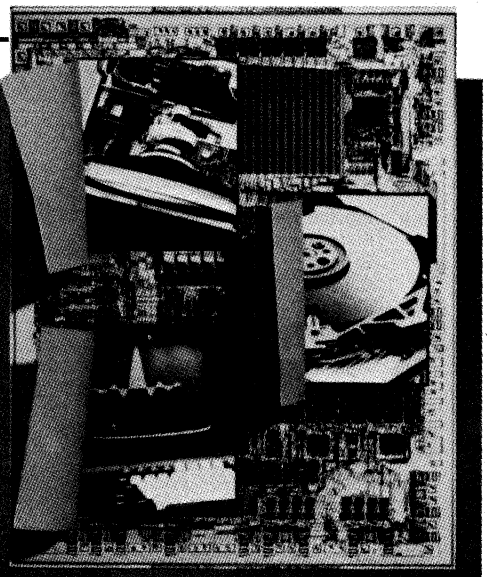
a. Pipeline Register	(29821)	CP-Q	12ns	
Decoder	(2924)	Sel-Y	12	
Source Select	(2918)	OE-Y	19	
RALU	(29116)	$Y_{IN}-Y_{OUT}$	62	(est.)
Destination	(29821)	Setup	4	
			109ns	

DLE can go LOW 10ns after data is valid on Y-bus (i.e., 53ns after CP↑). $\overline{OE_Y}$ should go LOW before 80ns from CP↑. Therefore a 50% duty cycle clock will work at 110ns with DLE tied to $\overline{OE_Y}$ to CP.

CONTROL PATH TIMING ANALYSIS

			Am2910	Am2910-1	Type
I.	**Pipeline Register** (29821)	CP-Q	12	12	
	Mapping PROM (27S190A)	t_{AA}	35	35	
	Sequencer	D-Y	20	20	Branch Map
	Control Memory	t_{AA}	40	40	Non-Relative
	Pipeline Register (29821)	Setup	4	4	
	Cycle Time:		111	111	
II.	**Pipeline Register** (29821)	CP-Q	12	12	
	Buffer Enable (2959)	OE-Y	20	20	
	Sequencer	D-Y	20	20	Relative
	Control Memory	t_{AA}	40	40	Branch
	Pipeline Register (29821)	Setup	4	4	
	Cycle Time:		96	96	
III.	**Pipeline Register** (29821)	CP-Q	12	12	
	RALU (Am29116)	I, T-CT	48	48	
	CC-MUX (Am2923)	D-W	12	12	Conditional
	Polarity (74S86)	D-Y	11	11	Branch
	Sequencer	CC-Y	43	30	Using CT
	Control Memory	t_{AA}	40	40	from 29116
	Pipeline Register (29821)	Setup	4	4	
	Cycle Time:		170	157	
IV.	**Pipeline Register** (29821)	CP-Q	12	12	
	CC-MUX (2923)	Sel-W	20	20	
	Polarity (74S86)	D-Y	11	11	Conditional
	Sequencer	CC-Y	43	30	Branch Using
	Control Memory	t_{AA}	40	40	External Status
	Pipeline Register (29821)	Setup	4	4	Register
	Cycle Time:		130	117	
V.	**Pipeline Register** (29821)	CP-Q	12	12	
	Sequencer	I-Y	70	50	Instruction to
	Control Memory	t_{AA}	40	40	Output Path
	Pipeline Register (29821)	Set-up	4	4	
	Cycle Time:		126	106	
VI.	**Sequencer**	CP-Y	125	85	
	Control Memory	t_{AA}	40	40	Clock to
	Pipeline Register	Setup	4	4	Output Path
	Cycle Time:		169	129	

Technical articles



Bipolar VLSI builds 16-bit controller handling many fast peripherals at once

Special-purpose microprocessor has controller instruction set in microcode, manipulates three operands in one cycle

by Sunil Joshi, Deepak Mithani, and Steve Stephansen
Advanced Micro Devices Inc., Sunnyvale, Calif.

☐ In the last decade, peripheral controllers have evolved from little more than simple input/output ports into highly sophisticated dedicated processors that command the level of performance necessary for handling high data rates. They also must now provide intelligent pre- and post-processing of data to offload from the host computer the specialized tasks intelligent controllers perform.

Recognizing the need for such a processor, Advanced Micro Devices has combined its proprietary Imox processing technology with a bipolar circuit design of scaled emitter-coupled logic based on very large-scale integration to produce the Am29116 16-bit bipolar microprocessor. The largest and the most complex bipolar device ever produced, the 29116 has an architecture and an instruction set specifically designed for high-performance, intelligent peripheral controllers. The high performance is a result of its unique architecture, microprogrammable instruction set, and processing technology; its requisite high speed is achieved by designing the part in ECL with TTL-compatible levels at the pins (see "What is microprogramming?" p. 100).

The instruction set of the 29116 has extensive data and bit manipulation capability to mask, rotate-and-merge, or rotate-and-compare, data in one microcycle—functions that are useful for field extraction, field insertion, and data alignment, which are frequently encountered in controllers. The architecture provides flexibility and parallelism in the data paths so that the device can perform in one microcycle a complex function that would take other processors several cycles to execute. One such feature is the barrel shifter, which rotates a 16-bit word by up to 15 places in one microcycle before the arithmetic operation is performed. The part also has an on-chip priority encoder and cyclic-redundancy-checking logic for specialized functions.

Created for a microprogrammed environment, the 29116 gives the user the flexibility to tailor the controller architecture for a specific application. MOS microprocessors, with their fixed architecture and instruction set, are limited in this respect. The performance is at least an order of magnitude higher than that of any available MOS device (see "Imox: a union of TTL and ECL," p. 102).

The 52-pin device has a microcycle time of 100 nanoseconds. In one cycle, the three-input arithmetic-and-logic unit operates on one, two, or three operands, while the barrel shifter is rotating one of the operands before it is used for an operation. The part also has a single-port register file that is 32 words deep by 16 bits wide and a dedicated accumulator to store temporary results. In this way, the advantages of both register-based and accumulator-based machines can be obtained (Fig. 1).

Bidirectional busing

The bidirectional 16-bit Y-bus is the primary off-chip data input and output port. The 16-bit D-latch at the input allows the data to be presented directly to the ALU, or be latched and used in the next cycle. This latch can thus be used as a pipeline for prefetching data while the ALU is performing a different function. It is also possible to bring data onto the chip on the Y-bus, perform some function on it, and then send it out again on the same bus without even having to store it.

The priority encoder generates a binary coded number, indicating the most significant bit in the operand that is a one. This special-purpose hardware module saves a significant amount of time, since a subroutine is ordinarily required to perform this often-used operation.

The status register is clocked with the ALU every cycle

and can even contain user-defined status bits whose function is defined by the microcode. Using microinstructions, it is also possible to provide a condition-test output based on the status. The bidirectional T-bus, when used as an input, exploits the device's parallelism further by allowing the user to select a condition for branching, while simultaneously executing an instruction in the ALU. The user can also select separate read and write addresses for the same instruction in both the byte and 16-bit word modes.

In addition to having full-carry lookahead across all 16 bits, the ALU executes all the conventional one- and two-operand instructions, such as move, complement, 2's complement, add, subtract, AND, NAND, OR, NOR, exclusive-OR, and exclusive-NOR.

Masking in a microcycle

Where the 29116 departs from convention is in its ability to operate on three operands simultaneously in a single microcycle. Thus a bit field can be selected from the two data operands with a masking operand all in a single microcycle.

The ALU produces three status outputs: overflow, negative, and carry. The zero flag, although not generated by the ALU, detects zero at both the byte and word level. The carry input to the ALU selects an input of 0, 1, or the stored carry bit from the status register, QC. Using QC as the carry input allows efficient execution of multiprecision addition and subtraction.

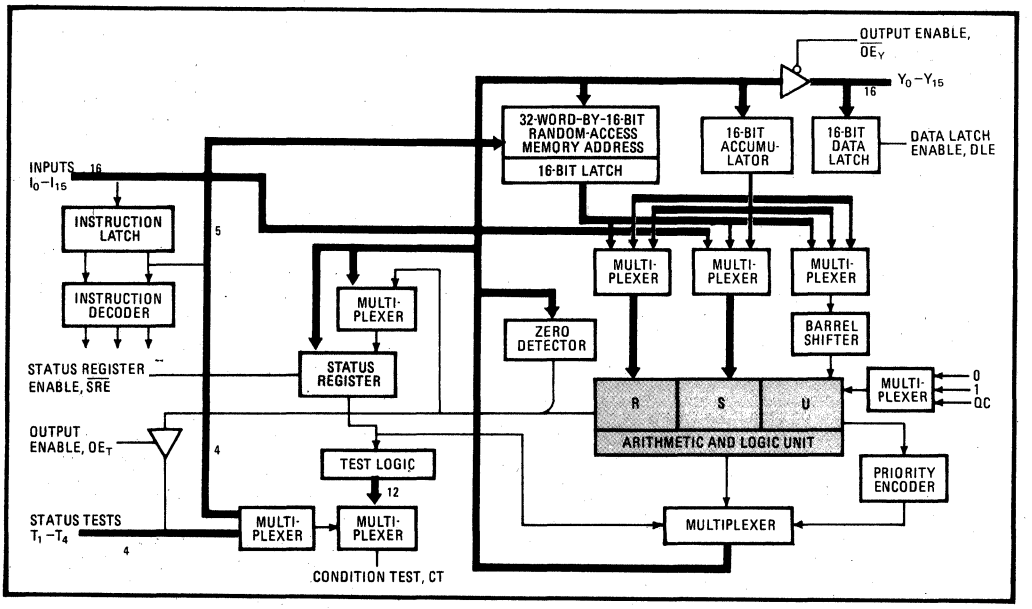
The condition-code generator contains the logic necessary to develop the 12 condition-code test signals. The condition-code multiplexer selects one of these test signals and places it on the CT condition-test output for use by the microprogram sequencer. The multiplexer may be addressed in two different ways. In the first, a test instruction specifies the test condition to be placed on the CT output but does not allow an ALU operation at the same time. The second method uses the bidirectional T-bus as an input, which requires extra microcode but lets the controller simultaneously test and execute.

Specialized instructions

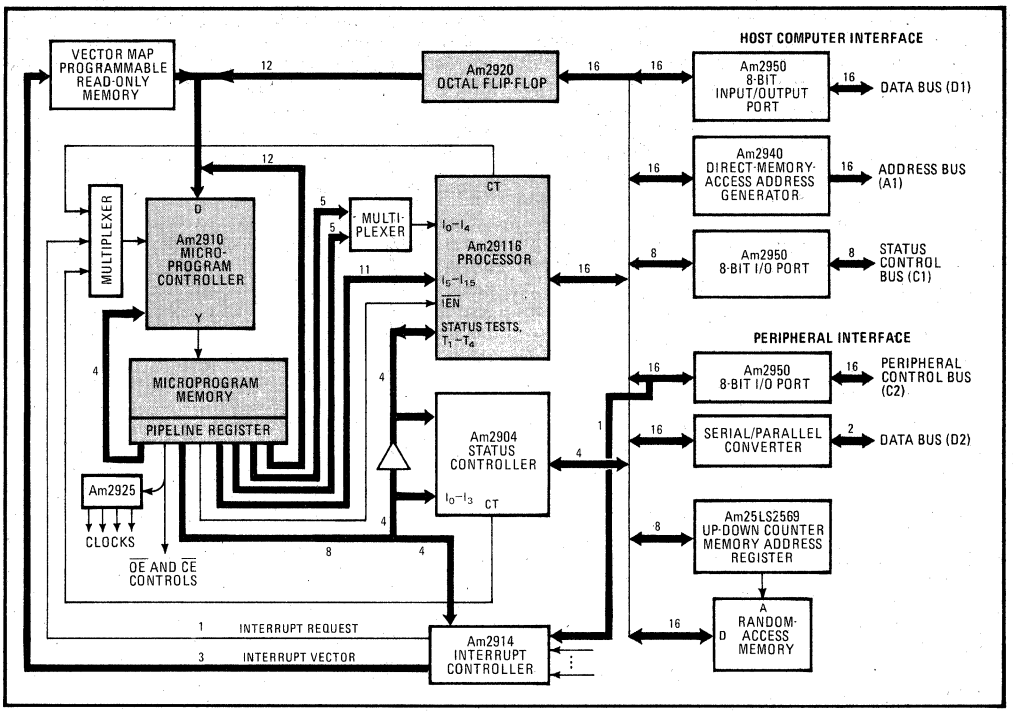
Immediate instructions are executed in two clock cycles. During the first clock cycle, the instruction decoder recognizes that an immediate instruction is being specified and captures the data on the inputs in the instruction latch. In the second clock cycle, the data on the instruction inputs is used as one of the operands for the function specified during the first clock cycle. At the end of the second clock cycle, the instruction latch is returned to its transparent state.

Since the 29116 is optimized for intelligent controllers, it has extensive bit manipulation instructions operating in either the byte or the word mode. These instructions allow operations such as setting, resetting, and testing of any particular bit without affecting the rest of the bits. Single-bit masks can also be created, such as a single 1 in a field of 0s or a single 0 in a field of 1s in a single microcycle. In addition, the instructions can generate memory addresses in powers of 2 by incrementing or decrementing a number by 2^n, where n can vary from 0 to 15.

The rotate-by-n instruction uses the barrel shifter with n specifying the number of bit positions the source is to be rotated. In the word mode, a specified number of bits are wrapped around over the 16-bit boundary; in the



1. Novel architecture. The arithmetic-and-logic unit on the 29116 16-bit bipolar microprocessor has three inputs so that a masking operation can be performed simultaneously with another instruction. The barrel shifter and priority encoder further optimize it for control.



2. Maximum system. If the highest speeds are required, then the 29116 can be assisted by support chips from the 2900 family. However, a minimum system configuration can be realized by using only the shaded components, though system throughput will be slightly degraded.

byte mode, the bits are rotated around the 8-bit boundary of the least significant byte.

The rotate-and-merge instruction can merge two operands on a bit-by-bit basis, under the control of the mask as a third operand. Thus, in one microcycle, translation from one code to another, such as from ASCII to hexadecimal, can be done with this instruction. This sort of operation would require at least three instructions with a conventional ALU.

The rotate-and-compare instruction compares a rotated operand with a nonrotated operand. A 1 at the mask input (third operand) eliminates that bit from the

What is microprogramming?

Most instructions execute a fixed sequence of steps to perform their function. This control sequence may be realized as a hardwired random-logic state machine that provides the necessary outputs for controlling the different functions. The disadvantage of this approach is that it leads to a design that is irregular and inflexible.

An alternative is the microprogrammed approach, where the control information is obtained from a regular structure, such as a programmable array or a read-only memory. A sequence of controls is obtained by accessing different words in the array. This access is usually obtained by cycling through consecutive words in the array until the instruction is completed. The action is performed by a sequencer that selects the microsubroutines that execute instructions.

Thus, a microprogrammed control mechanism consists of a memory and a sequencer. The memory can be a ROM, programmable ROM or random-access memory, and the information residing in it is referred to as the microcode. The sequencer controls the order of execution of the microcode words. In a microprogrammed system, the output of that microcode memory, however it is stored, directly controls the machine's hardware. This memory in essence replaces the random-logic control mechanism of a machine.

The modularity of this scheme results in a design that is easy to upgrade or modify, since programming a PROM takes much less time than redesigning a random-logic state machine. In the same way that assemblers simplify machine language programming, programs called meta-assemblers can aid in the writing of microcode. A development system called System 29 aids the design of microprogrammed systems. It also contains a meta-assembler called Amdasm for assembling the firmware portion of a system. Using Amdasm, it is possible to write microcode using user-definable mnemonics and the other facilities provided by System 29 help in the development and debugging of this firmware.

comparison. The result of the comparison is loaded in the 0 bit of the status register. If the comparison passes, the 0 bit is set.

The 29116 can also prioritize a masked operand, which is ideal for performing n-way jumps as well as for normalizing numbers. The priority encoder accepts a 16-bit input and produces a 5-bit binary-weighted code indicating the bit position of the highest-priority active bit. If none of the bits is active, the output is 0. Such an operation requires a separate subroutine when carried out on conventional microprocessors.

Forward and reverse

For reliable data transmission, the cyclic-redundancy-check instructions permit generation and comparison of the CRC check bits using any 16-bit polynomial. Since the CRC code standard does not indicate which data bit must be transmitted first, the 29116 supplies both forward and reverse CRC instructions, each of which consumes only two microcycles per bit—perfect for bidirectional tape drives.

In the first cycle, the data bit is shifted from one of the registers into the link bit of the status register. During the second cycle, check bits are generated by executing either the CRC forward or reverse instructions. The result is stored back into the check-sum register.

The part also includes such niceties as exclusive-NOR sign extention for converting 8-bit integers into 16-bit ones and a single-bit shift directly on a register.

A typical system configuration for the 29116 consists of a host computer, memory, and peripheral controller interfaced through three buses. The peripheral controller and the peripheral devices are interfaced with a separate data bus, which may be either serial or parallel, and a control bus. Information on the control buses comprises status, command, and timing signals.

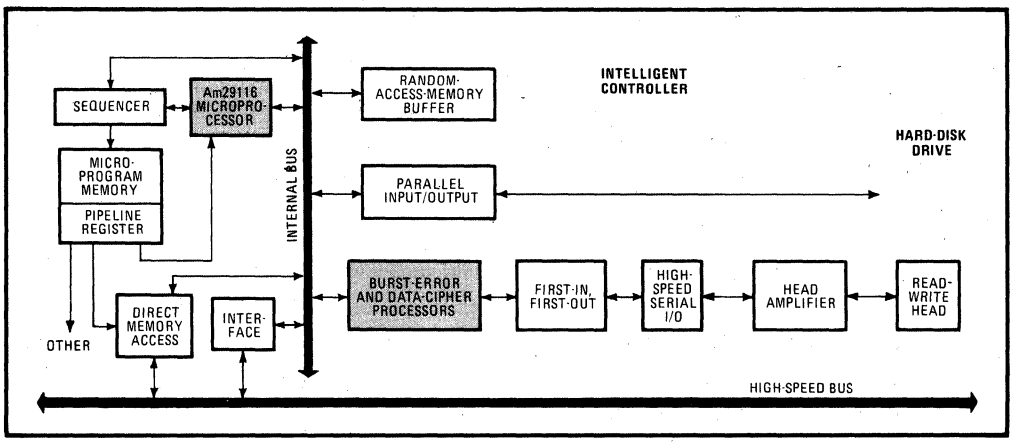
In a typical implementation of the peripheral controller portion of a system, the bidirectional interface to the host's data bus is via two Am2950 8-bit parallel I/O ports. Two Am2940 8-bit direct-memory-access address generators drive the associated address bus, and another 2950 interfaces with the bidirectional control bus. The interface to the serial peripheral data bus in this case is serial. The interface between these bus-interface units and the 29116 is a 16-bit bidirectional bus that connects to its Y port. A 256-word random-access memory for temporary data storage and a 12-bit interface to the microprogram controller connect to the D inputs of the AM2910 microprogram sequencer. The bus-control and clock-enable signals for these devices are generated by the pipeline register at the output of the microprogram memory.

The 29116, 2910, and the microprogram memory perform the data manipulation and routing; command and status generation and testing; and the timing-signal generation functions. This implementation minimizes the amount of hardware necessary to implement a controller, which is accomplished by sharing the instruction-inputs to the 29116 with the inputs to the 2910; by generating all the necessary test conditions within the 29116, which permits connecting the CT output of the 29116 directly to the condition code ($\overline{CC}$) inputs of the 2910; by performing all the necessary status manipulations within the 29116; and by using the same RAM address for reading and writing.

A tradeoff

Although the peripheral-controller implementation described above minimizes the amount of required hardware, it does limit the throughput. The architecture shown in Fig. 2 uses the same bus interface circuits but maximizes the throughput of the controller at the expense of additional hardware. In this implementation, the instruction inputs of the 29116 and the D inputs of the 2910 are driven from separate microcode bits, making possible simultaneous instruction execution in the 29116 and direct jumping in the 2910.

The multiplexer at the $\overline{CC}$ input of the 2910 allows conditions to be tested without loading the signals into the 29116. Four additional bits of microcode drive the T



3. Typical application. The 29116 is ideal for controlling Winchester disk drives. It can handle up to eight such drives simultaneously and, with the addition of a burst-error processor and data-ciphering processor, it can be made very reliable as well.

Imox: A union of TTL and ECL

The Imox process is an advanced oxide-isolated structure developed by Advanced Micro Devices to address the reproducibility requirements of die sizes in excess of 50,000 square mils. It employs fully ion-implanted transistors, walled emitters, and two layers of metal interconnections. Assuming the same feature sizes, Imox can produce devices with less than half the base area and two thirds the collector substrate area of a diffused-isolation washed-emitter low-power Schottky transistor. Smaller sizes and inert isolation regions significantly reduce device capacitances and increase potential speed.

The approach selected was to combine an oxide-isolated device structure with emitter-coupled-logic internal and TTL input/output circuitry. The technique enabled engineers at AMD to pack the equivalent of over 2,500 TTL gates into 78,000 square mils of silicon, using 3-micrometer minimum features and an 8-μm metal pitch.

As with all large-scale integrated processes, Imox is a marriage of circuit and process approaches. The reason that the internal circuitry of the 29116 is implemented in ECL, while the inputs and outputs are all standard TTL levels with translators to the ECL interior, is because ECL possesses the ability to create dense structures with an excellent speed-power product through series gating.

The barrel shifter in the 29116 is an excellent example of how ECL can be applied to a complex LSI device. This function performs a selectable n-bit shift or rotate. It is the equivalent of 276 gates and is implemented with 526 components, consumes 92 milliwatts, and exhibits delays of less than 7 nanoseconds.

inputs of the 29116, permitting simultaneous conditional testing and execution of an instruction in the controller. In addition, the ALU status bits can be selectively loaded into the 2904 to reduce the number of cycles necessary to perform status manipulation.

By adding five additional microcode bits and a multiplexer at the I inputs of the part, separate source and destination addresses can be used in the same microcycle. For example, the contents of the third register can be added to the contents of the accumulator and the results can be stored in register 7.

In addition to supplying the basic oscillator and clock driver functions, the 2925 system-clock generator and driver lets the user dynamically alter the length of the microcycle and, thus, interface the 29116 with slower bus-interface and peripheral circuits. The 2914 handles high-speed interrupts from the peripheral controllers.

The 29116 functions as a superior disk controller because its bipolar technology enables it to perform at much higher speeds than MOS processors and, therefore, handle as many as eight Winchester disk drives simultaneously (Fig. 3). Its microprogrammability lets it be tailored to the requirements of a specific application. Efficient data movement and data compression is possible using instructions, such as rotate-and-merge.

Major application areas

The unit's bit manipulation instructions are useful for checking control and status bits. A microprogrammed system allows the controller to initiate a task such as positioning the disk head while performing other tasks until notified that the head is in position.

Fast response to interrupts as well as other speed enhancements can be designed in, using other 2900 bit-slice-family components. The CRC instructions can be used for the checking and generating the file header CRC bits; the CRC reverse instruction is included for systems (such as with magnetic tape) in which reading data in a forward and in a reverse direction is desirable to avoid time-wasting back-space and reread operations.

Graphics processors vary in complexity based on the performance required from them, but sophisticated image processors require very high-speed controllers. The 29116 is well-suited for systems that include character and vector display or partition the screen into various regions that may need independent scrolling, cursor control, zoom and pan, scaling, and translation and transfer of data between various sections of the memory.

If the part is used for address generation, the arithmetic instructions using 2^n are useful. For example, in a windowing operation, there are certain bits in every horizontal scan that must be selected. The next line is displaced in the memory by a fixed address equal to the number of pixels in the horizontal line.

Thus, address generation is simplified considerably. In addition, vectors can be generated from the coordinates of two points to be connected can be done easily using algorithms that generate the intermediate points and require only additions and subtractions for interpolation.

Saving cycles

The rotate, rotate-and-merge, and other specialized instructions of the 29116 let the user perform the functions in one cycle that would take several cycles on conventional processors. For example, when a copying operation is performed on the display, a section of the area that was previously aligned with the 16-bit word boundary of the controller may no longer be aligned. The realigning may require rotation with a mask to leave the area outside the window unchanged.

Another excellent application for the 29116 is as a cluster controller that manages a group of devices requiring service on a statistical basis. These devices could be terminals or printers or specialized I/O ports. The controller can dynamically alter device priorities to assure a fast response to the active devices at the expense of the inactive ones.

The kinds of functions that a cluster controller may have to perform are data transfers between the devices themselves or between a memory and the devices, checking of device status, diagnostics, and assigning of service priorities. The priorities can be of different kinds and may be dynamically alterable. For example, when all devices are of equal priority, then a round-robin scheme can be used so that the device just serviced gets the last priority for the next service. □

A Microprogrammed CPU Using Am29116

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Advanced Micro Devices

6

A Microprogrammed CPU Using Am29116

INTRODUCTION

This application note shows techniques for designing a high-performance CPU using the Am29116 16-bit Bipolar Microprocessor. The Am29116 design maintains architectural and software compatibility with the Super-16, a 16-bit computer designed at AMD. An alternative implementation using the Am2901 and Am2903 4-bit Bipolar Microprocessor slices is described in chapter 9 of "Bit Slice Microprocessor Design" by John Mick and James Brick.

The architecture of the CPU incorporates pipelining at the microprogram level as well as at the macroinstruction level. It has the same instruction set as the Super-16, so it can run all its existing software with no modification. Although the Am29116 is optimized for peripheral controllers, it is an ideal choice for the CPU. It has a powerful instruction set for arithmetic operations, data movements, multiple bit shifts, bit manipulations and status manipulations. In addition to speed, the Am29116 design reduces power requirements and PC board area.

SYSTEM ORGANIZATION

In a simple system comprising a main memory 16-bits wide and the CPU (Figure 1), the main memory is designed with static RAM chips (such as Am93422). A simple bus structure communicates between two devices. Although the interface to other I/O devices is not discussed, the bus can easily be modified to accommodate bus request, bus acknowledge and other interface signals. Addition of other I/O devices would require a bus controller to arbitrate bus requests from the CPU or I/O devices that require Direct Memory Access (DMA) transfers.

The interface signals between the memory and the CPU are shown in Figure 2. The handshaking is done over a 16-bit-wide address bus, a 16-bit-wide bidirectional data bus and a control bus. The control bus comprises Memory Request, Read/Write, Address Accepted, Data Strobe, Data Synch, and Interrupt Control lines.

To use the data in the n + 1 cycle, the Am29116 generates the main memory address during the n − 1 cycle and the data is read

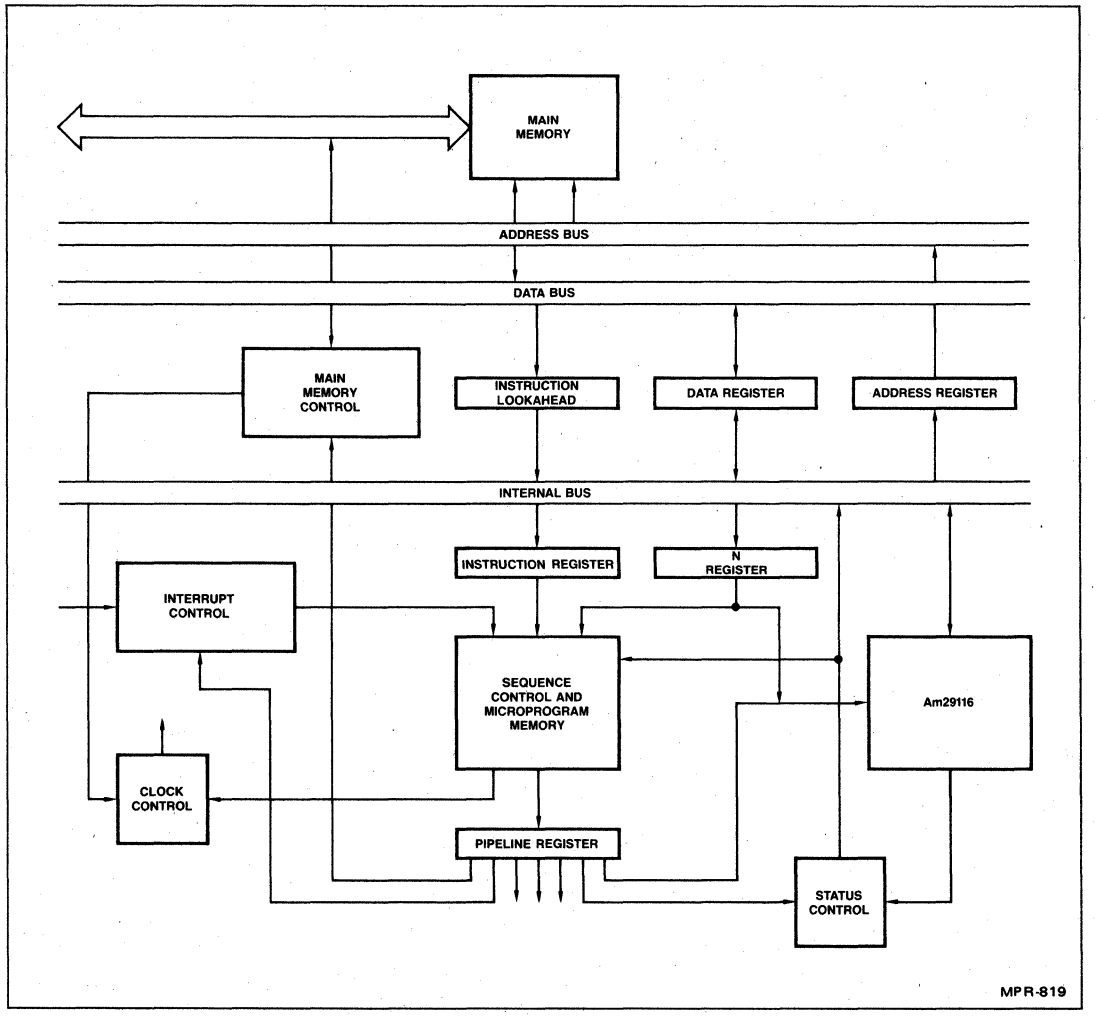

Figure 1. Central Processing Unit Block Diagram

during the n cycle (Figure 3). The n cycle is longer than normal CPU cycles to accommodate for the main memory read timings. Information to stretch the cycle is provided during the n – 1 cycle to the Am2925 system clock generator. The CPU generates the address, memory request and read/write signals during the n cycle. The main memory responds to the memory requests by pulling the Address Accepted signal LOW. If the memory is busy, it does not generate the Address Accepted signal; instead the CPU waits until it receives this signal. The CPU responds to the Address Accepted signal by generating the Data Strobe signal, indicating that it is expecting data from the memory. The Data Synchronous signal is generated by the memory, indicating valid data on the bus for the read operation. The Data Strobe and Data Synchronous signals generate either the load Z Latch or Load Data Register signal, depending upon whether the information requested is instruction or data, respectively.

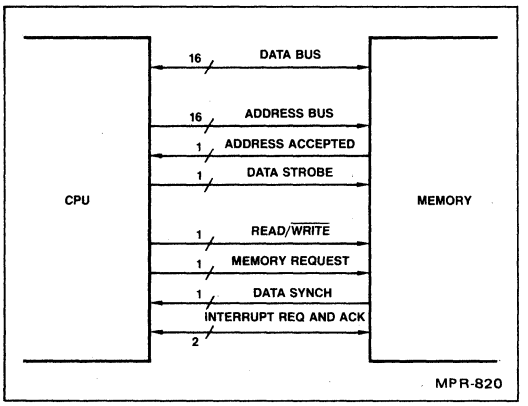

Figure 2. Memory – CPU Handshaking Protocol

Since the Am29116 generates the main memory address and the data to be written, the memory write operation is done in two cycles (Figure 4). The address and the memory request are held active for two clocks. The n clock is longer than the normal CPU clock to accommodate the main memory write timings. If the memory is not busy then the READ/$\overline{\text{WRITE}}$ signal is generated in the next cycle along with the Data Strobe signal, indicating valid write data on the bus. The main memory write pulse is generated from the Data Strobe and R/$\overline{\text{W}}$ signals. Acceptance of the write data is indicated to the CPU by the Data Synchronous pulse.

INSTRUCTION FORMATS

Instructions, which are stored in the main memory, are either one or two words long, with a word being 16 bits wide (Figure 5). The most significant half (MSH) of the first word is the operation code field. The least significant half (LSH) is divided into two fields, four bits each, indicating register assignment for the operands and the result. The lower half (registers 0-15) of the 32-register file in the Am29116 is used as a scratch pad by the user; the upper half

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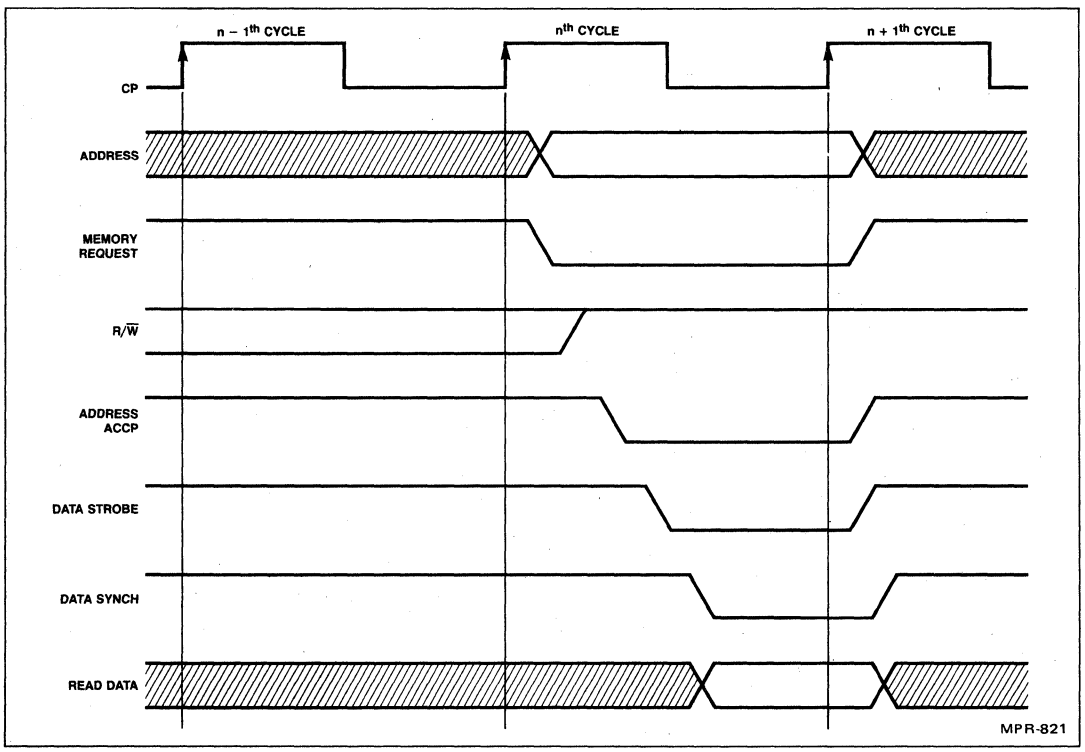


Figure 3. Memory Read

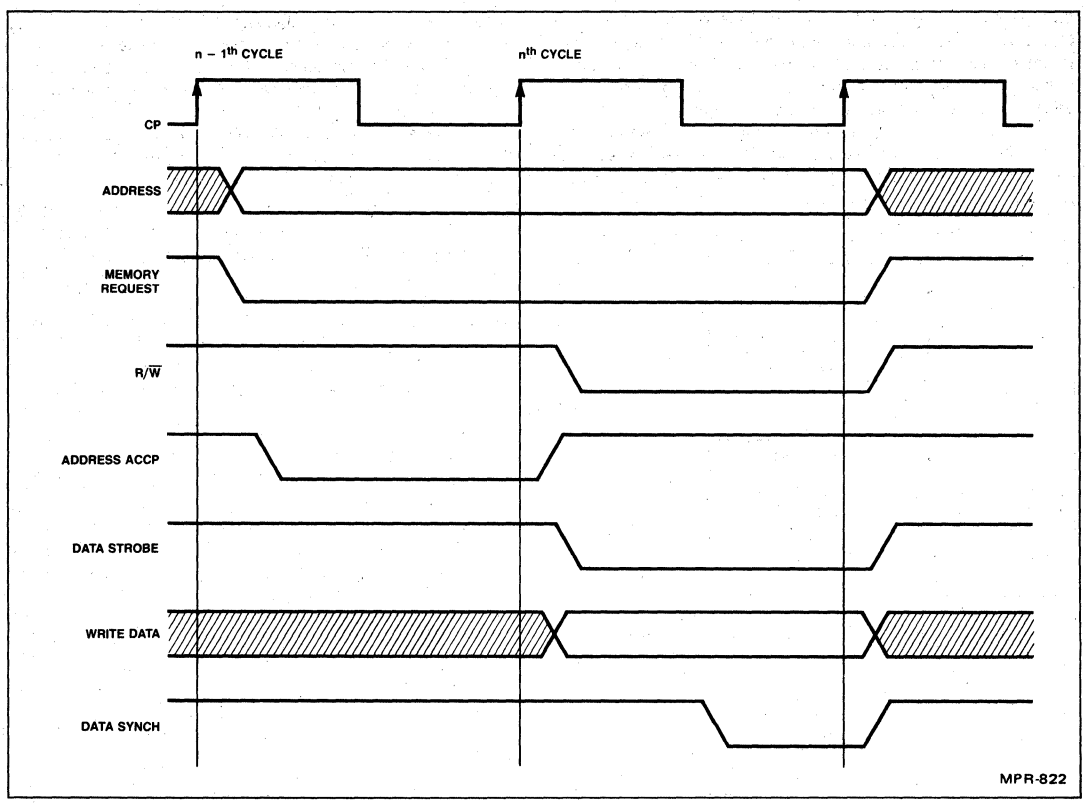


Figure 4. Memory Write

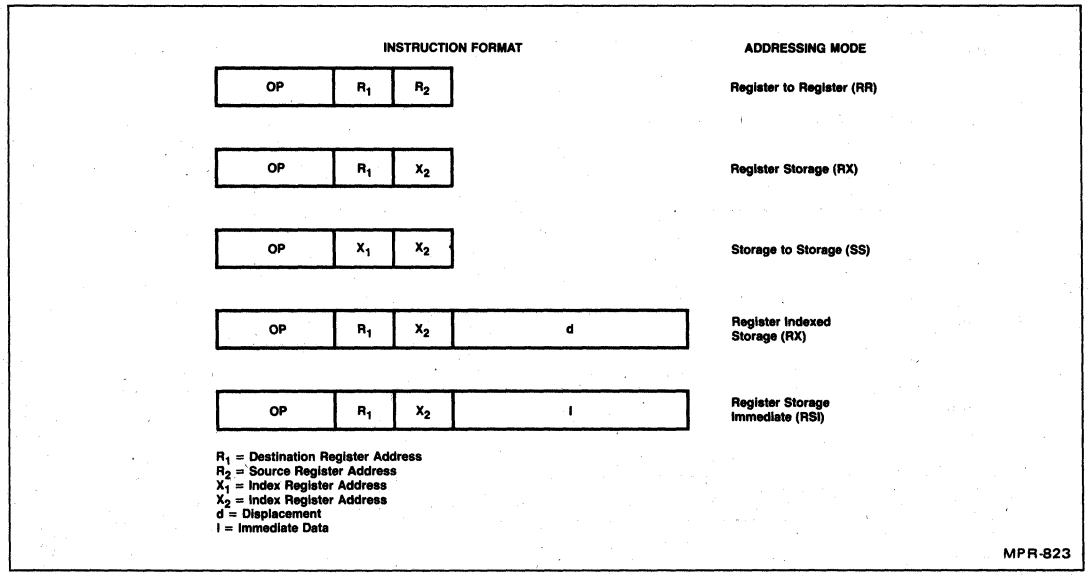


Figure 5. Instruction Formats

(registers 16-31) is used by the operating system to track memory stacks, counter, and so on. The first word of a two-word instruction has the same format as the one word instruction explained above. The second word is always a 16-bit value, which is either a displacement address or an immediate data.

There are 256 instructions possible with the 8-bit-wide operation code, which is usually more than enough for the general-purpose machine. The instruction set includes operation codes that can operate on the following data types:

- Bit
- Nibble
- Byte
- Word

The information about the addressing mode is designed into the operation code for different instructions. In addition the instruction set also includes the PUSH/POP instruction to maintain single or multiple stacks, I/O instructions, decimal and binary integer arithmetic.

Depending upon the addressing mode, the register specified by the instruction can act as either an accumulator for the arithmetic and logic operation or an index register to manipulate the operand address for the main memory. For the operations where the result is placed in the register, the R1 field depicts the destination register address and R2 (or R2 + d) is the source register (or points to the source field in the main memory). For the operations where the result is transferred from the register to the main memory, the R1 field depicts the source register address and R2 (R2 + d) points to the destination memory location. For the memory-to-memory transfer, the R2 field is the source pointer and the R1 is the destination pointer for the main memory.

The microprogram architecture provides the flexibility for designers to select different formats and define the machine-level instructions. The instructions and instruction format are similar to the Super-16 computer designed at Advanced Micro Devices. For more detailed information refer to chapter 9 of "Bit-Slice Microprocessor Design" by John Mick and Jim Brick (a McGraw-Hill Publication).

CPU ARCHITECTURE

In the block diagram of the CPU (Figure 6), all internal data transfers are done through the 16-bit-wide internal bus. The data transfer between the system bus and the internal CPU bus is done through the Data Register, the Address Register and the Z latch. The design incorporates single-level pipeline structure. The register at the output of the microprogram memory acts as a pipeline register, providing the capability to execute simultaneously one microinstruction while fetching the next. The Instruction Register (IR) and the Z latch allow macrolevel pipelining. While the macroinstruction in the Instruction Register is being decoded, the Z latch may contain the next macroinstruction (in the register-to-register mode) or the displacement field (in the index addressing) or the data (in the immediate addressing).

Data Path (Macroinstruction)

The macroinstruction from the main memory is either loaded into the Z latch or into the Instruction Register. A macroinstruction can be loaded directly into the Instruction Register by making the Z latch transparent. The Z latch is made transparent by forcing its enable signal HIGH. The decision to load either the Z latch or the Instruction Register is made by the addressing mode of the macroinstruction being decoded. During the pipefill operation, the first macroinstruction is loaded into the Instruction Register. All single-word instructions are next loaded into the Z latch, then into the Instruction Register after execution of the current macroinstruction. Since a two-word instruction consumes information stored in both the Instruction Registers (which contains the instruction) and the Z latch (which contains the displacement), the next macroinstruction from the main memory is directly loaded into the Instruction Register. During the decoding of a two-word instruction, if the content of the Z latch is decoded to be a displacement then it is used by the Am29116 during the form operand address cycle. If it is decoded as immediate data, then it is used during the execute cycle. (See Instruction Execution section for both situations).

The data transfer between the processor and other devices is implemented using the Am2918 data registers and tri-state buffer chips (Figure 7). The data receive register (DRX reg.) receives data from the system data bus under microprogram control. The data transmit register (DTX reg.) acts either as the register to transmit data on system data bus or as a temporary register for the CPU internal bus. As a temporary register, data can be loaded from the internal bus and read to the bus under the control of microprogram.

The D latch at the input port of the Am29116 provides the capability to input and output data in the same microcycle. Data is brought in through the Y port (either from Z latch or DTX register) and loaded into the D latch during the first half of the cycle. During the second half, the D latch is disabled. The Y output buffers can be turned on to allow the ALU result to appear on the internal bus.

The N register permits incorporation of functions such as N-way jump and normalization. A 16-bit word can be prioritized in the Am29116 under the control of a mask. The five-bit vector is loaded into the N-register and used in the next cycle either to branch to a specific microroutine or as a number "n" in the instruction to rotate a word in the barrel shifter.

Microprogram Control

The control logic generates the proper sequence of microprogram execution. The Am2910 Microprogram Controller generates the address for the next microinstruction to be executed. It can perform either sequential access or conditional branch to any microinstruction within its 4k microword range. The Am2910 receives the branch address (at D inputs) from one of the four sources: 1) Pipeline Register, 2) Interrupt Vector Decoder, 3) Macroinstruction Decoder, or 4) N-register. The macroinstruction Decoder (Mapping PROM) uses the operation code (bits 8-15 of IR) as an address and provides the starting address of the microroutine that executes each macroinstruction. The interrupt vector decoder uses the three-bit vector (generated by the Am2914 Vectored Priority Interrupt Controller) unique to a requesting device and generates the starting address for interrupt service routine. The N-register provides the capability to do n-way jump. The prioritize instruction in the Am29116 generates a five-bit binary vector indicating the most significant one in the 16-bit word. This vector along with other predefined bits can be used as a branch address.

The decision to branch in the Am2910 depends upon the condition presented at the $\overline{CC}$ input. The status bits from the Am29116 T-bus (Carry, Overflow, Zero, Negative) can be used to branch in the next cycle by selecting one out of four (T_1 to T_4) inputs at the CC-MUX. The condition test output from the Am29116 or the Am2904 can be selected at the CC-MUX to branch on complex conditions (such as less than, equal, etc.) or to branch on the condition generated previously.

Microcycle timing analysis for some selected critical paths is shown in Figure 8. This analysis is done using worst case propogation delays of each chip. The timing path through the pipeline

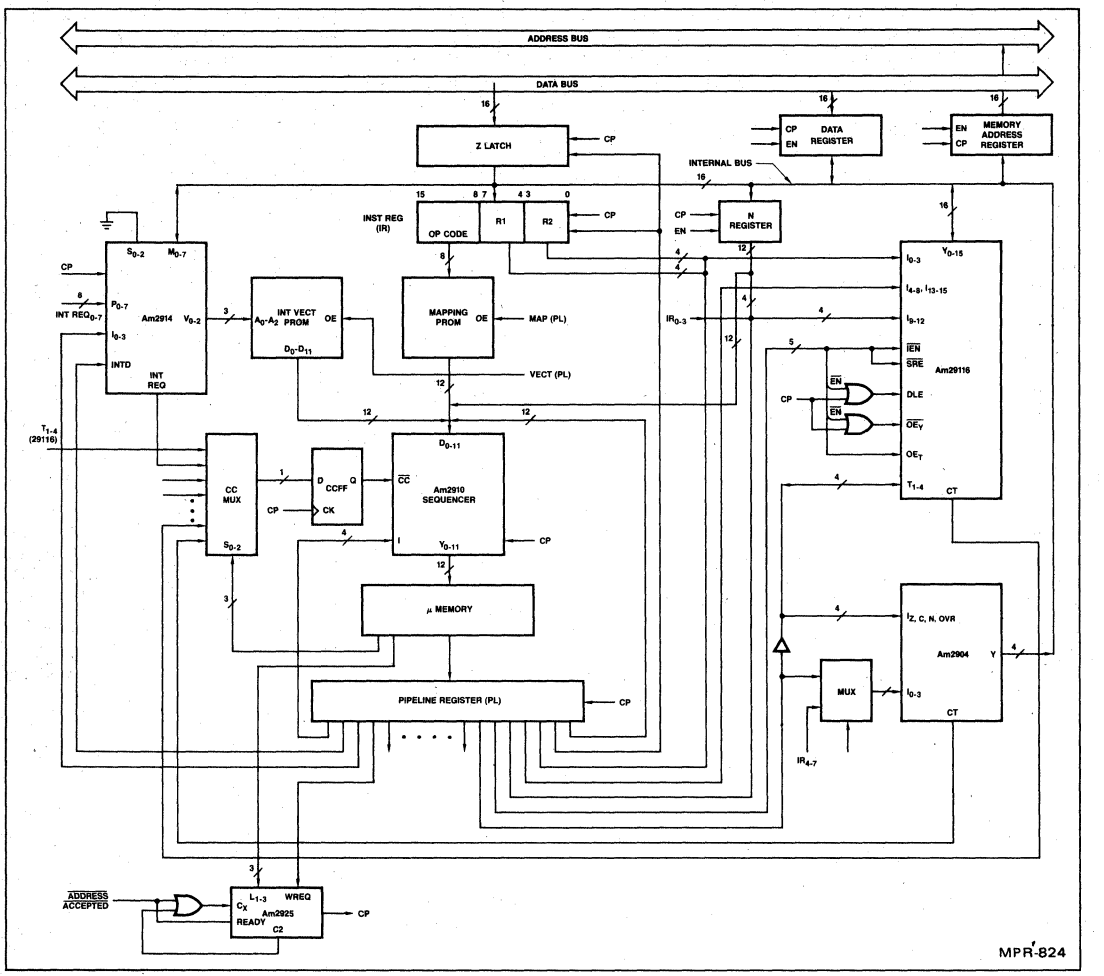


Figure 6. Central Processing Unit

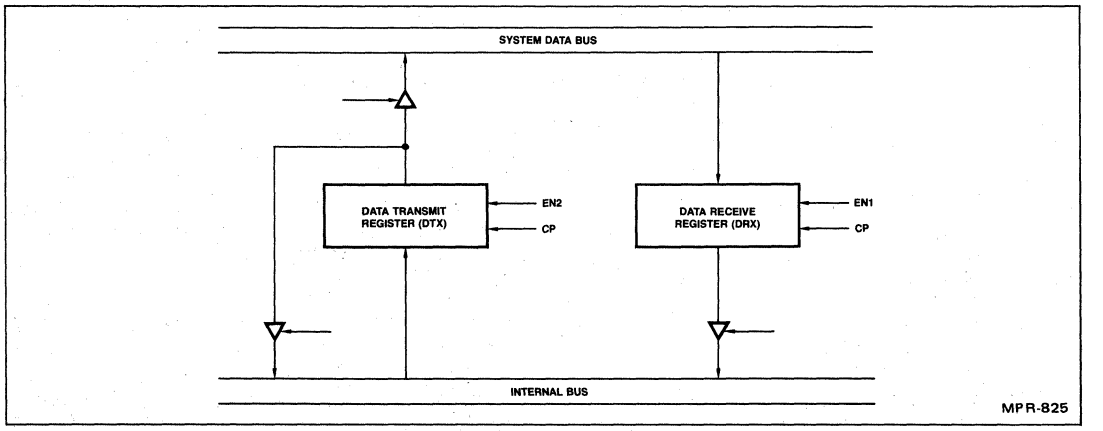
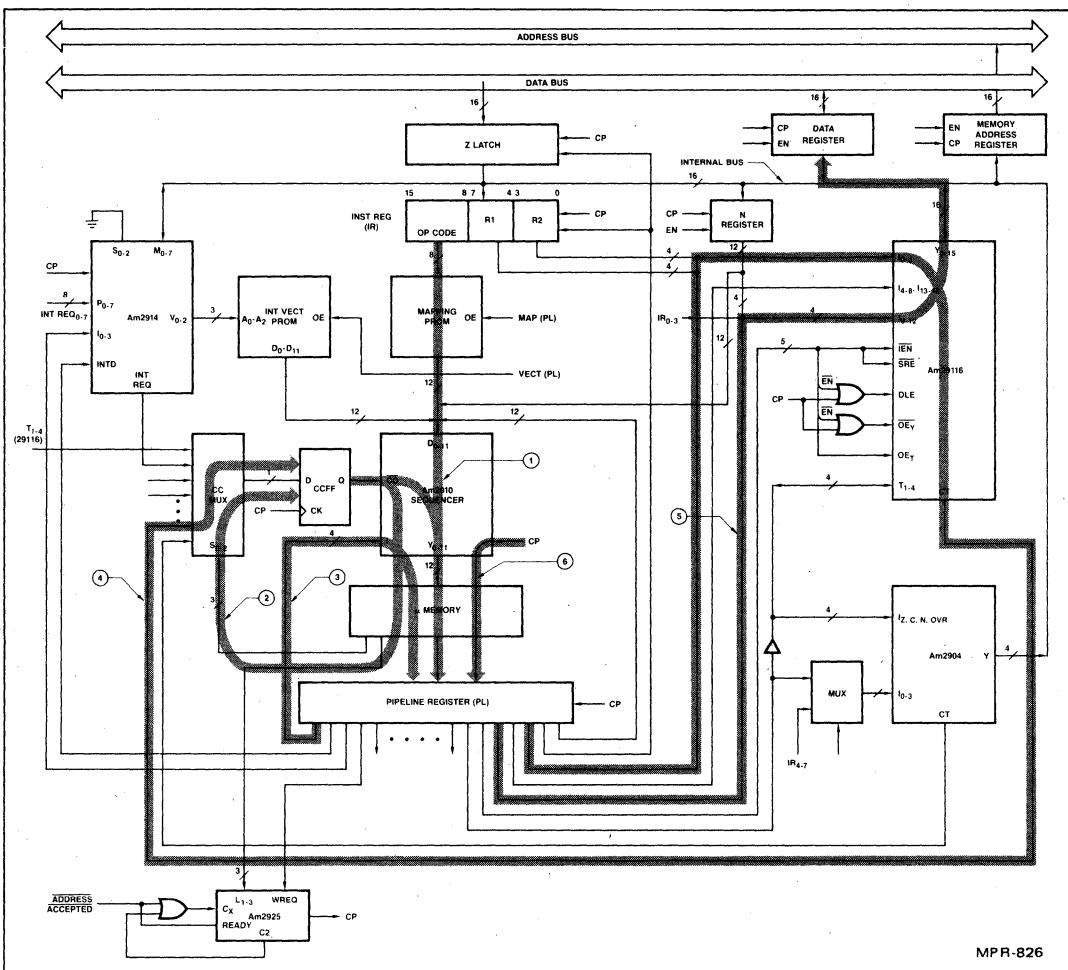


Figure 7. Bidirectional Data Register Configuration



TIMING ANALYSIS

Path 1

Instruction Register	CP	Q	12ns
Mapping PROM	ADD	Y	35ns
Sequencer	D	Y	20ns
Micro-memory	Add	Y	40ns
Pipeline Register	Set up		5ns
			112ns

Path 2

CC Flip Flop	CP	Q	12ns
Sequencer	CC	Y	43ns
Micro-memory	Add	Y	40ns
CC-MUX	Sel	Y	15ns
CC Flip Flop	Set up		5ns
			115ns

Path 3

Pipeline Register	CP	Y	12ns
Sequencer	I	Y	70ns
Micro-memory	Add	Y	40ns
Pipeline Register	Set up		5ns
			127ns

Path 4

Pipeline Register	CP	Y	12ns
Tri-State Gate	Enable	Y	29ns
Am29116 (preliminary data)	I	CT	48ns
CC-MUX	DIN	Y	15ns
CC Flip Flop	Set up		5ns
			109ns

Path 5

Pipeline Register	CP	Y	12ns
Tri-State Gate	Enable	Y	29ns
Am29116 (preliminary data)	I	Y	79ns
Data Reg	Set up		5ns
			125ns

Path 6

Am2910 (PC and Stack)	CP	Y	100ns*
Micro-memory	Add	Y	40ns
Pipeline Register	Set up		5ns
			145ns

*It is assumed that the previous instruction could produce no change in the counter or could only decrement the counter.

Figure 8. System Timing Analysis

register (CP to Q), Am29116 (I to CT), CCMUX (D to Y), Am2910 ($\overline{CC}$ to Y), microprogram memory (address access) and back to the pipeline register (set-up time) was the most critical path affecting the microcycle. However, the use of D-Flip Flop (CCFF) separates the cycle time for that path into two non-critical paths. Since the D-Flip Flop delayed the condition code ($\overline{CC}$) signal at the input of Am2910 by a clock, the CC-Mux select lines are taken out from the microprogram memory to align the selection of the condition code and the execution of microinstruction. With the CCFF in, the most critical path in the system is through the Am2910 (CP to Y), microprogram memory (address access) and the pipeline register (set-up time). This critical path can be made non-critical by adopting two level architecture, which is not discussed in this application note for simplicity.

Am29116

The Am29116 allows the processor to perform powerful arithmetic and logic functions. In addition, the Am29116 also maintains and generates main memory addresses. Its 32-word RAM provides ample temporary storage to enhance the throughput of the processor. The lower half (Registers 0-15) of the 32-register file in the Am29116 is used as a scratch pad by the user, the upper half (Registers 16-31) is used by the operating system for tracking memory stacks, counter, etc. For high-level language implementation, the barrel shifter allows field insertion and extraction, rotation and table lookup. An onboard status register provides the ability to check the user-definable and other status flags through either the instruction inputs or the bidirectional T-bus with result appearing at the CT output.

The instruction set of the Am29116 provides additional power to the processor. The prioritize and rotate instructions can be used to normalize a floating point instruction. The bit manipulation capability provides easy address manipulation and pattern generation.

The detail CPU diagram (Figure 6) indicates that the 16-bit instruction inputs of the Am29116 are driven by the microcode bits. The multiplexer (tri-state bus) at the input of bits 0 to 3 provide flexibility to address sixteen registers by either the macroinstruction field (R1 or R2) or from the microcode. Similarly, to provide flexibility in specifying the number "N" for rotating a word from either the macroinstruction or N-Register or microinstruction, a multiplexer (tri-state bus) is used at the input of bits 9 to 12. The outputs of the R1 and the R2 field of the Instruction Register are controlled by separate microcode bits. Since the Am29116 has a single-port RAM, it takes two cycles to perform register-to-register operation. In the first cycle, the contents of R2 are moved to the Accumulator. In the second cycle, an operation between R1 and the Accumulator is performed with R1 as the destination. Four additional bits of microcode drive the T_1 to T_4 inputs of the Am29116. This allows simultaneous testing of the status and execution of an instruction in the Am29116. The four status bits (C, N, OVR, Z) can be loaded into the status register or can be taken out on the T-bus. Thus selective loading of the status bit can be done in the Am2904 using the T-bus. The flexibility of the Am2904 reduces the number of cycles necessary to perform status manipulations. To allow branching in the next cycle, on these (C, N, OVR, Z) status bits, the T-bus also goes to the CC-MUX input.

The Am2904 has two status registers, one for the micro level status and the other for the machine (macro) level status. The micro-status is updated every microcycle if the T-port of the Am29116 is the output port. The macro-status is updated at the end of each machine instruction. Thus branching at the micro-level or machine-level becomes easier with the Am2904.

The Am2925 system clock generator and driver, which provides basic clock oscillator and driver functions, can generate four different clock waveforms (different duty cycle). The Am2925 provides the capability to alter the length of the microcycle dynamically, and it responds to asynchronous interfaces by generating a wait state. The capability of the Am2925 to stretch the cycle and generate a wait state enhances the CPU power by making the interface with slower device easier and more efficient.

INSTRUCTION EXECUTION

The normal instruction cycle has four basic sequences of operations:

1. Form memory address of instruction
2. Fetch Instruction
3. Decode Instruction
4. Execute

For instructions that require operands from the memory rather than the local register file, two extra steps will be required after the decode operation: form operand address and fetch operand.

The performance is increased by prefetching the next instruction during the execution of the current instruction. The pipeline architecture partially utilizes the overlapping capability of the fetch, decode and the execute operations of the different instructions because the Am29116 is acting as both the Program Control Unit and the Arithmetic Logic Unit. The use of separate PCUs (2901 or 2930) will increase the performance of the system and utilizes the pipeline architecture to the fullest extent.

Each operation is detailed below.

Form Memory Address (1 microcycle)

The Program Counter (PC) is incremented by two and the result is loaded into the Memory Address Register (MAR) and back into the PC. This can be done by selecting RAM as the destination and $\overline{OE}_y$ LOW in the Am29116.

Fetch Instruction (1 microcycle)

The Main Memory Request and the Read Strobe is generated. The memory uses the address generated in the same cycle and puts the data on the bus. The instruction is loaded into the Instruction Register at the next rising edge of the microcycle.

Decode Instruction (1 microcycle)

The Instruction falls through the Z latch into the IR. The mapping PROM generates appropriate starting address for the microprogram from the operation code.

Form Operand Address (1 microcycle)

After every instruction fetch another read cycle occurs. The data is stored in the Z Latch. Depending upon the addressing mode of the instruction during the decode cycle, the decoding logic determines whether the data in the Z Latch is the next instruction the displacement or the immediate data. This displacement value is used with the specified index register to form an operand address and loaded into the MAR.

Fetch Operand (1 microcycle)

The Operand is read from the memory address generated in the previous clock and stored in the Z Latch (or D-Reg).

EXECUTE

The Am29116 performs the specified operation on the operands.Two microcycles are required for a register-to-register type of instruction because of the single port register file in the Am29116. This can be done in one cycle by two address architectures.

The instruction cycle for the Register-to-Register type (RR) is shown in Figure 9a. A second memory fetch occurs after the instruction fetch cycle during the pipefill operation. The second instruction fetched is stored in the Z-latch. The next instruction is loaded from the Z-latch into the IR after executing the current instruction. Concurrently, the address for the following instruction to be fetched is placed on the address bus. During the next cycle, the instruction fetched from the memory is stored into the Z-latch.

The execution of each instruction takes two clocks as explained before. Figure 5a indicates that, except for the pipefill operation, the Am29116 is used in all the cycles either for the execution of an instruction or for the generation of the main memory address.

The instruction cycle for the Register-to-Index storage (RX) type is shown in Figure 9b. During the pipefill operation the displacement is fetched immediately after the instruction. After the pipe is

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	
Form Instruction Address	A	B				C			D			E										**PC + 2 → PC** **PC + 2 → MAR**
Fetch Instruction		IR A	Z B				Z C			Z D			Z E									**PC + 2 → MAR and Load Z Latch or IR**
Decode			A			IR B			IR C			IR D									**Decode Instruction and Load Pipeline Register**
Form Operand Address																					**Z + Index Register → MAR**
Fetch Operand																					**Load Data Register**
Execute				A	A		B	B		C	C		D	D							
	Y	Y		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y							**The Am29116 Usage**

A, B, C, D are Register to Register type instructions.
Z = Z Latch
IR = Instruction Register

Figure 9a. Register to Register Instruction Cycle

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	
Form Instruction Address	A	A_D			B		B_D			C		C_D										**PC + 2 → MAR** **PC + 2 → PC**
Fetch Instruction		IR A	Z A_D			IR B		Z B_D			IR C		Z C_D									**(PC + 2 → MAR and PC)*** **Load IR or Z Latch**
Decode			A				B					C										**PC + 2 → MAR and PC** **Decode and Load Pipeline Register**
Form Operand Address				A					B					C								**Z + Index Register → MAR**
Fetch Operand					A					B					C							**PC + 2 → PC and MAR** **Load Operand in Data Register**
Execute						A					B					C						
	Y	Y		Y	Y	Y	Y		Y	Y	Y	Y		Y	Y	Y						**The Am29116 Usage**

*For pipefill operation only.

A, B C are Register to Index storage type instructions.
A_D, B_D, C_D are displacement.
Z = Z Latch
IR = Instruction Register

Figure 9b. Register to Index Storage Instruction Cycle

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	
Form Instruction Address	A	A_D			B or K	B_D K_D			B+2 K+2		B+2$_D$ K+2$_D$											PC + 2 → MAR PC + 2 → PC
Fetch Instruction		IR A	Z A_D			IR B or K	Z B_D K_D			IR B+2 K+2		Z B+2$_D$ K+2$_D$										(PC + 2 → MAR and PC)* Load IR or Z Latch
Decode			A				B K				B+2 K+2											PC + 2 → MAR and PC Decode and Load Pipeline Register
Form Operand Address								B K					B+2 K+2									Z + Index Register → MAR
Fetch Operand									B K					B+2 K+2								PC + 2 → PC and MAR Load Operand in Data Register
Execute				A*						B K					B+2 or K+2							
	Y	Y		Y	Y	Y		Y	Y	Y	Y		Y	Y	Y							The Am29116 Usage

*During this cycle decision to branch takes place
If condition is true, Address = K = Index Reg + A_D
If condition is false, Address = B = A+1

Z = Z Latch
IR = Instruction Register

Figure 9c. Branch or Condition RX Type Instruction Cycle

filled, generation of the next instruction address and fetching of an operand can be done concurrently. The Am29116 is used in six out of the seven cycles needed to execute the RX type of instruction (Figure 5b).

M specifies conditions for jump. (X_2) + displacement is the branch address.

The decision to branch on the RX-type instruction occurs after the CPU determines that the condition is true or false (during execute A cycle) (Figure 9c). The format for the macro-branch is shown in Figure 10. The condition code for the branching is presented to the Am2904. The Am2904 presents this condition to the Am2910 where the decision to branch takes place.

MICROWORD FORMAT

The microinstruction is 78 bits wide (Figure 11). The control bits for each functional unit are grouped together for better readability. Definitions of each control bits are shown in Table I. The enable signals for loading the Z latch and the D latch of the Am29116 can be used with the clocks or other timing waveform to ensure proper operation. Proper waveforms for the memory interface can be generated from the Data Strobe and the READ/$\overline{\text{WRITE}}$ signals depending upon the type of static RAM chips used in the main memory.

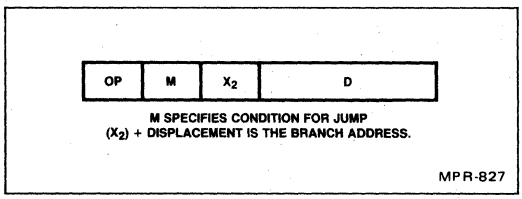


Figure 10. Branch on Condition (RX) Instruction Format

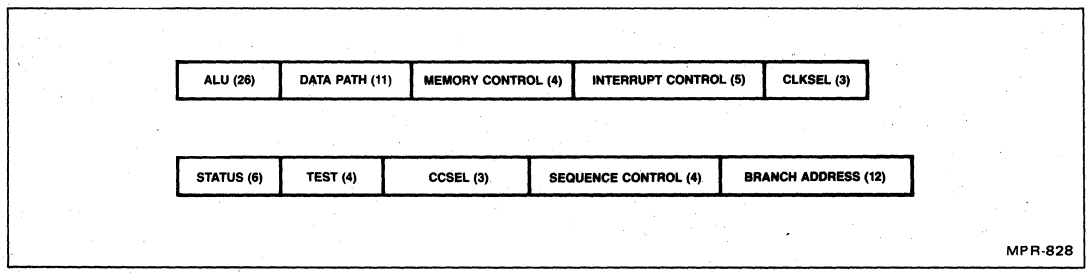


Figure 11. Microword Format

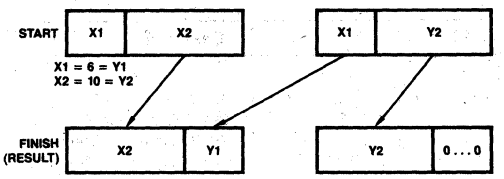
TABLE 1. MICROINSTRUCTION FIELDS

Field Width	Mnemonic	Description
ALU		
16	I_0-I_{15}	29116 Instruction
1	DLE	29116 Data Latch Enable
1	IEN	29116 Instruction Enable
1	OEY	29116 Output Enable Y-bus
1	SRE	29116 Status Register Enable
1	OET	29116 Output Enable T-bus
3	RAMSRC	29116 I_0-I_4 Source Select
2	NSRC	29116 I_9-I_{12} Source Select
Data Path		
4	DSEL	Data Register Source/Destination Select
1	DLD	Data Register Enable
1	MARLD	Memory Address Enable
1	IRLD	Instruction Register Enable
1	ZLD	Z Latch Enable
1	NLD	N Register Enable
1	MAP	Mapping PROM Output Enable
1	VECT	Interrupt Vector PROM Output Enable
Memory Control		
1	R/W	Memory READ/WRITE Pulse
1	WREQ	Wait Request
1	DATASTB	Data Strobe
1	MEMREQ	Memory Request
Interrupt Control		
4	I_0-I_3	2914 Instruction
1	INTD	2914 Interrupt Disable
Clock Select		
3	L_1-L_3	2925 Clock Length Select
Status		
1	EZ	2904 Enable Zero
1	EC	2904 Enable Carry
1	ES	2904 Enable Sign
1	EOVR	2904 Enable Overflow
1	CEM	2904 Enable Machine Status
1	CEMICRO	2904 Enable Micro Status
Test		
4	T_1-T_4	29116 or 2904 Test Status Instruction
CCSEL		
3	CCSEL	Condition Code MUX Select
Sequence Control		
4	I_0-I_3	2910 Instruction
Branch Address		
12	BA	Next Micro Address
78		

6

EXAMPLE

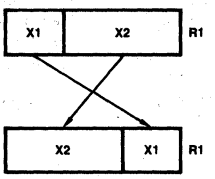
One of the frequent operations performed in the floating point CPU is normalization (Figure 12). A 23-bit mantissa is stored in two registers. To start, the MSH of mantissa is in register R1 and the LSH is in the Accumulator. The contents of R1 is checked for zero. If it is not zero, prioritization is done on R1; otherwise, it is done on the Accumulator to determine the bit position of the most significant one. The actual number of positions to be shifted is one less than the binary weighted code generated from the Am29116; this can be done directly in the microroutine, which performs the normalization. Knowing the number of leading zeroes, the contents of the R1 can be rotated (Figure 13a). In the second step, the contents of the Accumulator can be rotated on the fly and merged with the contents of the R1 under the control of mask.The result is stored back in R1 (Figure 13b). Since the MSH of the result is formed, the LSH can be formed by rotating the contents of the Accumulator by N and merging it with zero under the control of different mask (Figures 13c and 13d). Flow chart of the normalization is shown in Figure 14.



Example: Floating Point Normalization

MPR-829

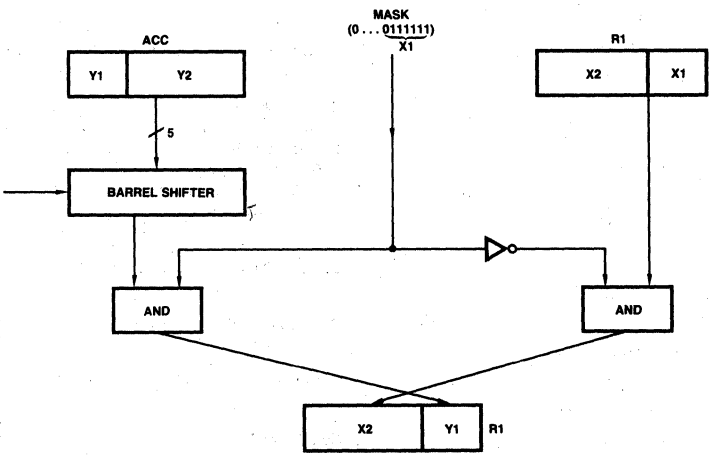
Figure 12.



Step 1: ROTR1, W, N, RTRR, R1 (Am29116 Instruction)

MPR-830

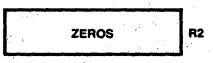
Figure 13a.



Step 2: ROTM, W, N, MARI, R1

MPR-831

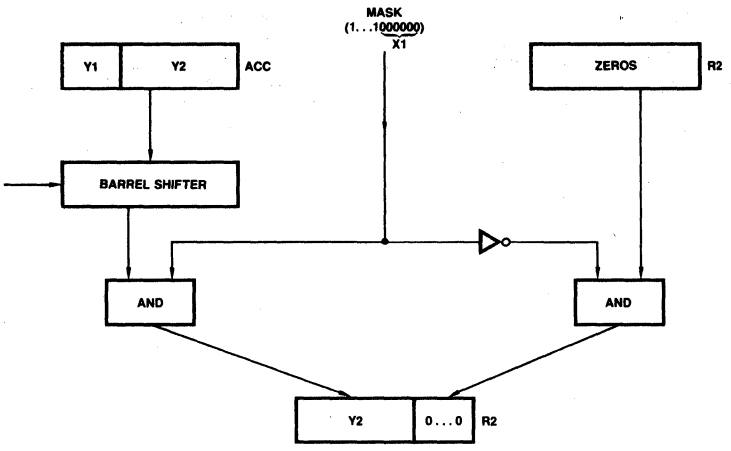
Figure 13b.



Step 3: SOR, W, MOVE, SOZR, R2

MPR-832

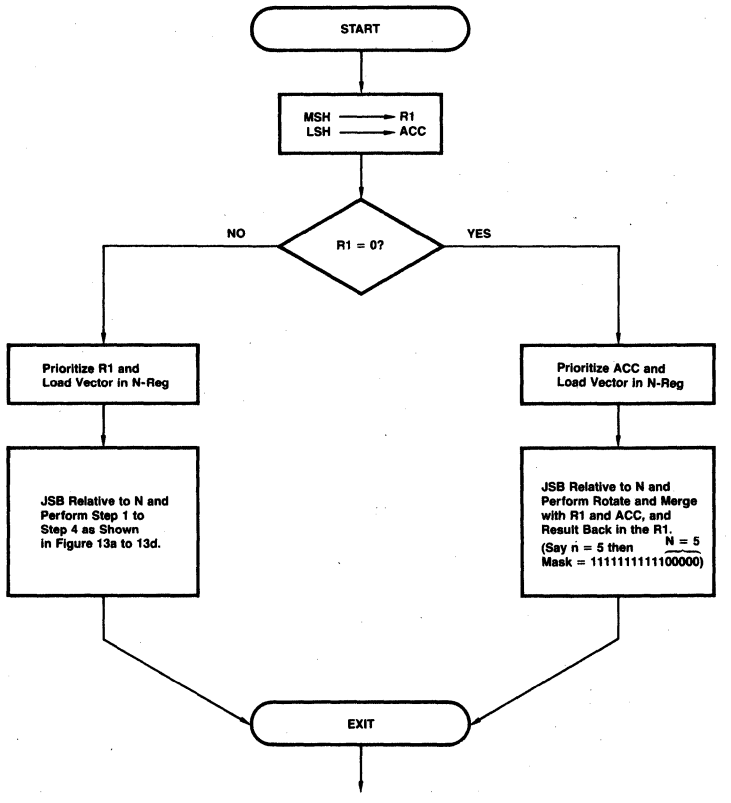
Figure 13c.



Step 4: ROTM, W, N, MARI, R2

MPR-833

Figure 13d.



MPR-834

Figure 14. Normalization of Floating Point Mantissa

CONCLUSION

Microprogrammability of the Am2900 devices makes customized architecture easier and faster to design. The powerful instruction set of the Am29116 provides additional capability to the CPU to do bit manipulation, Multiple Bit Rotate, Rotate and Merge, Rotate and Compare and prioritize functions besides normal arithmetic and logical operation.

The design shown in this application note is done with minimum part configuration. The throughput of the system can be increased with a separate Program Control Unit designed using the Am2930 or Am2901 executing concurrently with the Am29116 (ALU), thus relieving the Am29116 from generating the main memory addresses.

An Intelligent, Fast Disk Controller Using the Am29116

By Paul Chu, Brad Kitson, and Otis Tabler
Advanced Micro Devices

Until recently, advances in high-performance disk systems were limited mainly by the state of the art in Read/Write circuits and head. Today, track densities and transfer rates are becoming so high that the design of the controller is becoming a bottleneck. The need for high bandwidth is accompanied by demands for more powerful command sets and the transfer of many operating system software tasks into the controller firmware.

To implement intelligent high-bandwidth controllers, flexible and very fast VLSI building blocks are needed. This article shows how two such building blocks, the Am29116 Bipolar Microprocessor and the Am9520 Burst Error Processor, can be combined to form a disk controller with over 20MHz bandwidth, and incorporate such features as detection and correction of burst errors up to 11 bits long, I/O request queue sorting, sector caching, device transparency, logical record I/O, and associative (content-addressed) reading and writing of logical records.

The Am29116 performs 10 million instructions per second within a 16-bit parallel architecture and 32 x 16 register file. Its 16-bit barrel shifter allows an operand to be masked and rotated from 1 to 15 places and then optionally compared with a second operand within a single instruction cycle. Within a single cycle, it is also possible to rotate an operand and merge it with a second operand under a mask.

Other important features of the Am29116 includes its generation of forward and reverse CRCs; its ability to prioritize event and status bits under mask; and its ability to set, reset, and test arbitrary bits. The Am29116 is the largest and most complex such bipolar device produced. Fabricated using AMD's proprietary ion-implemented oxide-isolated (IMOX™) process, it contains emitter-coupled logic (ECL) circuitry scaled to VLSI proportions. Although ECL is used internally, all input and output buffers are fully TTL-compatible.

The Am9520's features, which make it a cornerstone of this design, include the ability to generate check bits and detect and correct single and burst errors for four different modified Fire code polynomials--including the popular 48-bit polynomial and the exceptionally powerful 56-bit polynomial used in this design. High throughput of the Am9520 is achieved by using an 8-bit parallel network of exclusive OR gates that accomplishes the equivalent, in a single clock, of eight clockings of a linear feedback shift register. In less than 200 microseconds, the correct high speed mode of the Am9520, which is used in this design, permits correction of a maximum-length error burst (11 bits) anywhere within a 256-byte sector using the microcode logic shown and the 56-bit polynomial. The Am9520 performs the correct high-speed function by simultaneously dividing the data input by all of the factors (except the first) of the polynomial. Location and correction of the error burst is fast because the periods of the factors are short compared with the period of the composite polynomial.

Am29116 Organization

The Am29116 includes a 32 x 16 RAM with latched outputs, a 16-bit accumulator, a 16-bit data input latch, a 16-bit barrel shifter, a three-input arithmetic/logic unit, a 16-bit priority encoder, a status register, a condition-code generator/multiplexer, 16 tristate output buffers and a 16-bit instruction latch and decoder (Figure 1).

The single-port RAM has output latches that are transparent when the clock input CP is HIGH and latched when CP is LOW. Data is written into the RAM while the clock is low if the $\overline{IEN}$ input is also LOW and if the instruction being executed selects the RAM as destination. Data is written into the low-order 8 bits of the addressed word for byte instructions and into all 16 bits for word instructions. Separate read and write RAM addresses may be used by supplying a multiplexer on instruction inputs I4-I0 using CP as the select signal.

The accumulator, which is edge-triggered, accepts data on the LOW-to-HIGH transition of CP if $\overline{IEN}$ is also LOW and if the instruction being executed selects it as the

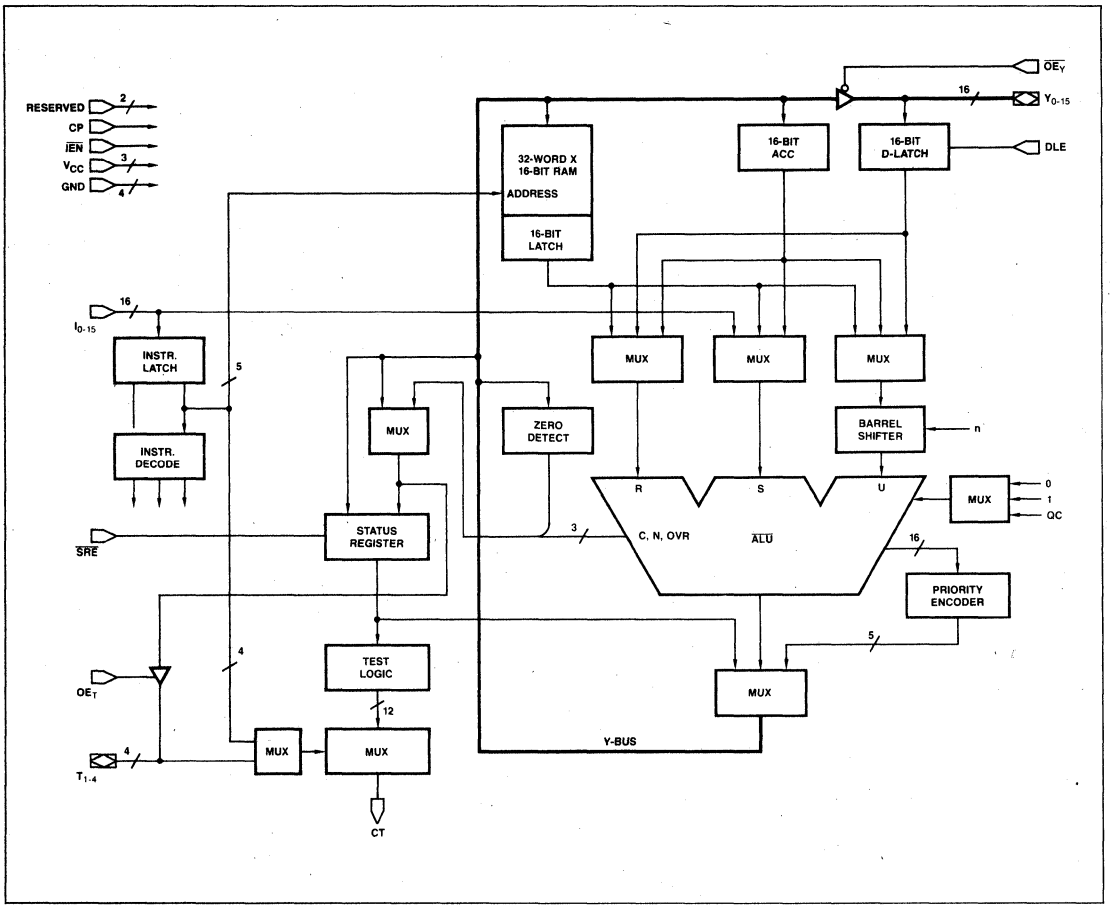


Figure 1. Am29116 Organization

destination. As with RAM locations, byte instructions modify only the lower half of the accumulator while word instructions modify the full register.

The data input latch (D-latch) holds the data input to the ALU on the bidirectional Y bus. The latch is transparent when the DLE input is HIGH and latched when the DLE input is LOW. The sources of the ALU operation are the RAM, the accumulator, the D-latch and the instruction inputs during IMMEDIATE instructions.

The ALU, which can operate on one, two, or three operands depending upon the instruction being executed, contains full carry lookahead across all 16 bits. All ALU operations can be performed in either word or byte mode. Status outputs Carry (C), Negative (N), and Overflow (OVR) are generated at the byte level for byte-mode operations and at the word level for word-mode operations. A fourth flag, Zero (Z), is generated outside the ALU and also operates in either byte or word mode. The Stored Carry (QC) bit of the status register may be selected (along with 0 and 1) as the ALU carry input to support multi-precision arithmetic operations. This is used by the correct high speed microcode of the disk controller, which employs coefficients as large as 2,647,216.

The priority encoder produces a binary-weighted code to indicate the location of the highest-order non-masked one at its input. If none of the masked bits is HIGH, the output of the priority encoder is zero. If bit i is the most significant HIGH bit then the output of the priority encoder is equal to s - i + 1 where s is the position of the sign bit and is equal to 15 in word mode and 7 in byte mode. To understand why s - i + 1 is used in place of s - i (the usual priority encoding), consider the following example (Figure 2). The eight Attention Drive signals are presented on the time-

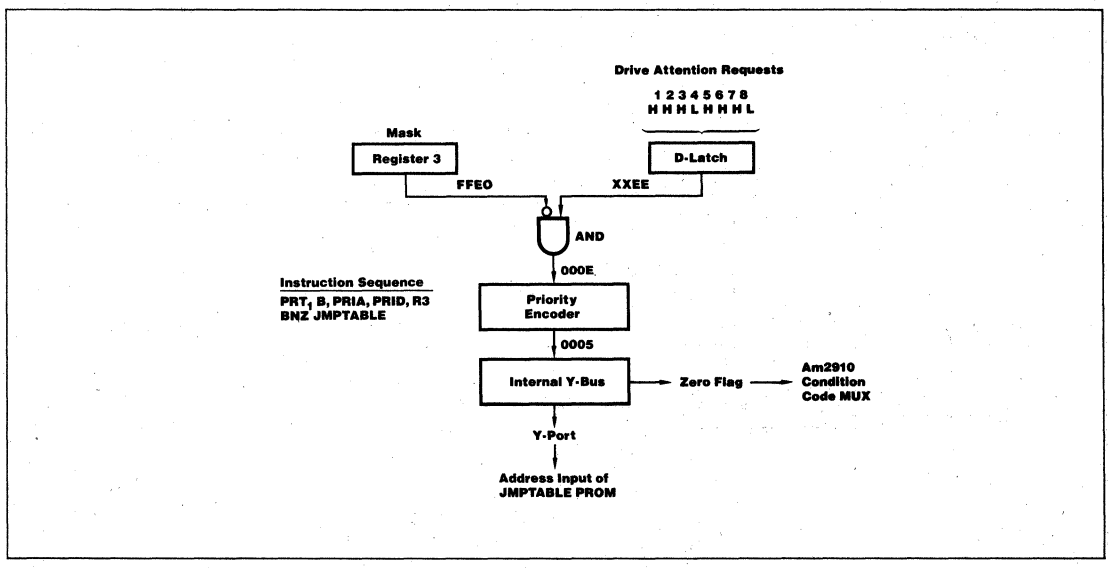


Figure 2. Using the Am29116 Prioritize Instruction

multiplexed drive command/data bus and are read through the Y-bus and data input latch of the Am29116. If the controller has already serviced all attention requests from drives 1-3 and wishes to service the highest priority attention request (if any) from drives 4-8, it executes a Prioritize instruction in byte mode using hexadecimal FFE0 as the mask, followed by a Branch if Not Zero into a jump table indexed by the priority encoder output.

The 8-bit status register and the condition-code generator/multiplexer contain the information and logic necessary to develop 12 condition-code test signals. The multiplexer selects one test signal and places it on the condition-code test (CT) output for use by the microprogram sequencer. The multiplexer is addressed in two ways. In the first, which is used here to maximize throughput, the T-bus is used in input-only mode to specify the multiplexer select position directly. In the second, the CT output is selected through a test instruction.

The output enable Y-bus ($\overline{OEY}$) input enables the 16 tristate output buffers when it is LOW. When $\overline{OEY}$ is HIGH, the output buffers are read in the high-impedance state (allowing read/write and status data to reach the D-latch from the controller's 16-bit system data bus).

The 16-bit instruction latch is normally transparent to allow decoding of the 16 instruction inputs I15-0 into internal control signals for the Am29116 and the execution of the instruction within a single clock cycle. The only exceptions to this rule are the immediate-operand instructions, which execute in two clock cycles rather than one. These are captured in the instruction latch during the first clock and executed during the second. It is during the second clock that the immediate operand, which resides in the I15-0 field of the next microinstruction, is fetched and execution is completed. Immediate instructions are used extensively in the disk controller microcode whenever masks and special arithmetic constants are needed. (The Am29116 allows the addition or subtraction of 2^N, and the use of 2^N and its complement as a mask, for any N between 0 and 15 within a single clock, so that for these 16 common numbers and 32 common masks, an immediate instruction is not required).

6

Am29116 Instructions

The 16-bit instructions of the Am29116 can be grouped into eleven types which correspond in a natural way with the Am29116's internal instruction decoding logic: single operand, two operand, single bit shift, rotate and merge, bit oriented, rotate by n bits, rotate and compare, prioritize, cyclic redudancy check, status, and no-op. The microprogrammer needs to be familiar with these groupings (and certain subgroupings) because the System 29 AMDASM DEF file provides mnemonics that correspond to them. For example, the AMDASM SRC file line

```
SOR             W,INC,SORY,R1
```

increments the full 16-bit contents of Am29116 RAM location 1 by one and places it onto the Y-bus and

```
TOR1            B,SUBR,TORAR,R2
```

subtracts the low-order byte of the

accumulator from the low-order byte of RAM location 2 while leaving the high-order byte of location 2 unchanged.

Table 1 summarizes the basic operations that Am29116 instructions can perform within a single cycle. (Two cycles are used if one operand is immediate data.) Note that for a typical line of this table, there are several Am29116 mnemonic operation codes, depending upon the choice of operand source(s) and destination.

TABLE 1. SINGLE-CLOCK Am29116 OPERATIONS

Add
Add with Carry
Add 2^N
And
Complement
Accumulate forward CRC
Accumulate reverse CRC
Exclusive Nor
Exclusive Or
Increment
Load 2^N
Load 2^N Complemented
Move
Nand
Negate (2's complement)
Nor
Or
Prioritize under mask
Reset bit N
Reset status bit
Rotate N bits
Rotate N bits and compare under mask
Rotate N bits and merge according to mask
Set bit N
Set status bit
Single bit shift
Subtract
Subtract with Carry
Subtract 2^N
Test bit N
Test status bit

Many of the operations prove particularly useful when implementing intelligent disk controllers. For example, the packing of ASCII characters (which occupy 8-bit bytes in main memory yet need only occupy 7-bit contiguous frames in the disk record) is accomplished efficiently and at high speed by Rotate and Merge instructions as shown in Figure 3. The microinstructions shown on the arrows perform the bit mapping indicated by them. In this example, 8 ASCII bytes requiring 64 bits of main storage are packed into 56 bits (8 7-bit contiguous frames) prior to being written to disk. In general, the ability of the Am29116 to rotate a 16-bit operand by N bits and merge it with a second 16-bit operand under mask within a single cycle makes the manipulation of arbitrary-length, arbitrarily-aligned data fields efficient and simple. Other operations that are especially valuable in this application are provided by the CRC Forward instruction (used to generate or check the integrity of header records), the instructions which add and subtract 2^N, load 2^N and its complement, reset, set, and test bit N, and (as indicated above) the masked Prioritize instruction. If the intelligence incorporated into the controller includes associative retrieval based upon recognition of an arbitrary bit string within the data record, the instructions which rotate by N bits and then (within the same cycle) compare under mask are almost indispensable.

6

Functions of An Intelligent Controller

The interface signal names, polarities, and functions used in this article are similar to those used in the current ANSI standard for rigid disks. However, the methods and

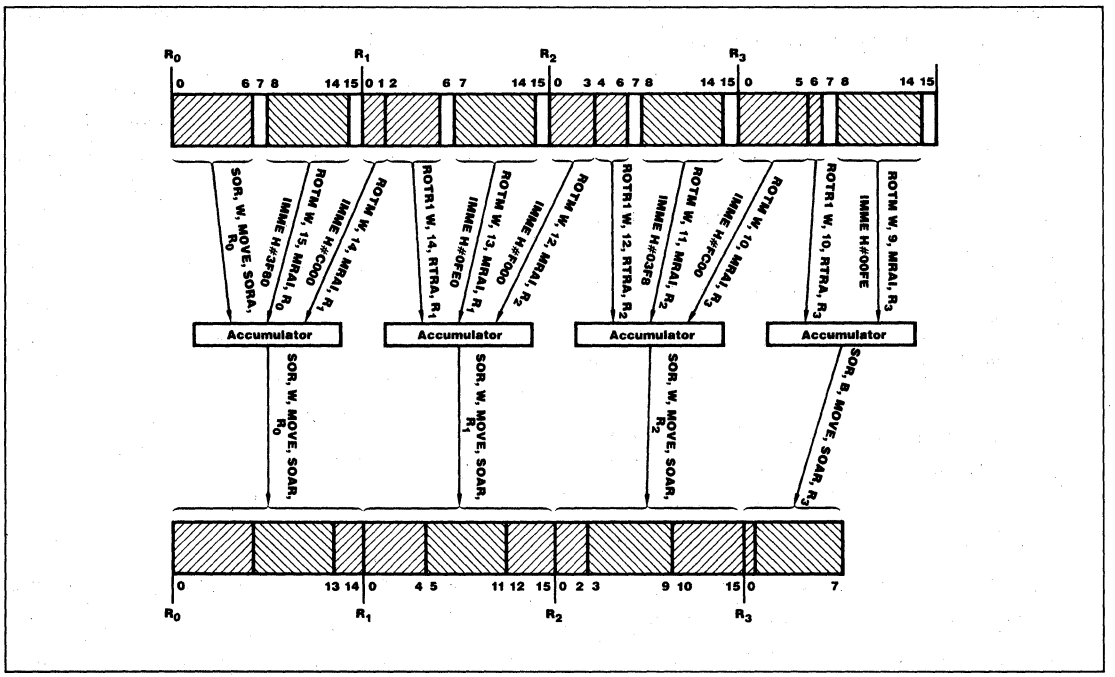


Figure 3. Packing ASCII Fields by Means of the Rotate and Merge Instruction

functions discussed can be used for most current rigid or flexible disk drives. With minimal external logic, the Am29116 and Am9520 perform all the functions needed to format, read, and write disks at over 20 MegaBits per second. These include generating and checking header CRCs, performing header-sector acquisitions, enabling and disabling drive read/write circuits at the appropriate times, managing data flow through a high-speed buffer memory, generating check bits during writes, and detecting and correcting single and burst errors up to 11 bits long during reads.

Except for seeks, retries, and formatting, all of the above have been microcoded. The microcode fits within 256 words (one-fourth of the microprogram memory used in the design), and it is appropriate here to describe some additional intelligent functions that can be microprogrammed:

Maintaining I/O Request Queues. To maximize throughput, the controller orders its read and write request queues by sector, head, drive, and cylinder. (Cylinders appear last in the order of sorting because a seek on one drive may be overlapped with a read or write on another.) The Am29116 maintains the read/write request queue in its 4096 x 16 high-speed buffer memory.

Selective sorting of the read/write request queue is performed by the controller. Each new request is assigned a "bump count" of 0 when the controller receives it. The request is then placed into the queue at the position determined by the following:

(1) Behind all requests whose bump counts equal N ("Queue 1")
(2) Inserted in sorted order into the remaining queue of requests whose bump counts are less than N ("Queue 2") as follows:

(a)	By type (read after write)
(b)	By sector number
(c)	By head number
(d)	By drive number
(e)	Finally, by cylinder number

(3) Before each new request is queued, Queue 2 is scanned head-to-tail. Each request encountered during the scan that has a bump count of N is removed from Queue 2 and placed at the end of Queue 1.
(4) After each new request is queued, the bump count is increased by 1 for each Queue 2 member that has been bumped by it (i.e., now follows it).

It should be noted that the choice of N is application-dependent, since increasing N increases throughput but also lengthens response time for some read/write requests.

2. Avoiding Redundant Reads. The Am29116 also maintains copies of the last eight sectors read from or written to disk. Before each read request is entered into the queue, the Am29116 compares it with

a list of buffer memory-resident sector images. If a match is found, the contents of the sector images are used to satisfy the read request and no enqueueing is performed.

3. Performing Logical Record I/O and Maintaining Device Transparency. The Am29116 translates I/O requests by logical record number into physical select, seek, and I/O operations by drive, track, head, and sector numbers. The CPU software need not concern itself with the characterisitics of the particular drives attached, and it is minimally affected by deletions and additions of drives of varying types.

4. Performing Associative Logical Record I/O. The Am29116 reads, writes, or returns the logical record numbers of logical records that contain specified fields. The CPU software merely specifies the type of operation to be performed and the length, relative position within the logical record, and value of the content-addressing field.

5. Performing Data Compression and Expansion. Much of the information routinely stored on disk as 8-bit bytes is character data. While it is convenient to manipulate these data in the central processor in 8-bit EBCDIC notation, they can usually be stored much more efficiently on disk as either 6-bit BCD (or FIELDATA) bytes or 7-bit ASCII bytes. The usefulness of compressing information in this manner depends entirely upon the database. For example, most accounting and management information system data do not involve lower-case alphabetics and can be recorded in 6-bit BCD (or FIELDATA), giving approximately a 25% reduction in disk storage occupied and a 33% increase in storage effectiveness. Most word processing data involve lower-case alphabetics but can be recorded in 7-bit ASCII, giving approximately a 12.5% reduction in disk storage occupied and a 14.3% increase in storage effectiveness. The recording of data compressed in this manner is accomplished by a translation from EBCDIC to BCD/FIELDATA or ASCII followed by packing and an unformatted write operation. Compressed data are read by an unformatted read operation followed by unpacking and a translation from BCD/FIELDATA or ASCII to ECBDIC. The translations are performed two bytes at a time by the two 2048 x 8 Am27S291 PROMs illustrated in Figure 8. The three microcode bits labelled XLAT2 -XLAT0 select one of eight code translations; four are used by the BCD/FIELDATA and ASCII compression algorithms and four are spares.

Many other types of application-dependent data compression can be performed directly by the controller. The following IBM VM/370 CMS commands perform various types of compression depending upon the old file type:

(1) COPY ,old file name. ,old file type. ,old file mode. ,new file name. ,new file type. ,new file mode. (REP PACK)

(2) COPY ,old file name. ,old file type. ,old file mode. ,new file name. ,new file type. ,new file mode. (REP UNPACK)

All the functions of COPY (PACK) and COPY (UNPACK) can be performed by the Am29116 and Am9520-based controller. The controller allows packed files to be read and written as if they were unpacked, just as it allows 6-bit BCD/FIELDATA and 7-bit ASCII files to be read and written as if they were 8-bit EBCDIC files.

System Organization

Figure 4 is an overall block diagram of the disk controller. The interface to the drives includes separate bit-serial data paths for read data and write data, and byte-parallel paths for commands, disk addresses, and disk status as described in the current ANSI standard. The Am2910 microsequencer and 1K x 8 Am27S35 registered microprogram memory drive the 80-bit control bus that directs the actions of the other components. Data flows serially and asynchronously at over 20 MegaBits per second between the drives and the time-division multiplexed serial input/serial output ports of the 16 x 16 FIFO array. Data flows synchronously in 16-bit parallel form between the FIFO array and the 4K x 16 Am9147 buffer memory. In this design, it is assumed that support of disk transfer rates of close to 30Mbit/sec. is desirable. This is why the burst error processor, which can handle data up to 20Mbit/sec, is placed in parallel with the first-in-first-out memory array and the Am9147 RAM buffer*. During

*AMD now offers the Am9520-1, a 30Mbit/sec part which will simplify the microcode shown in the application note.

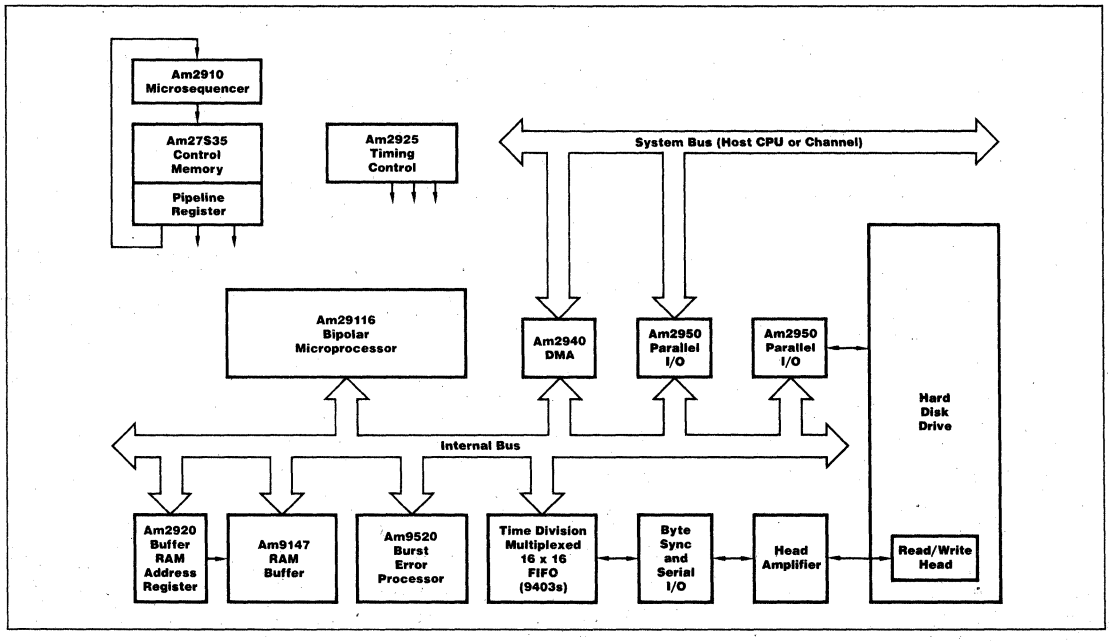


Figure 4. Block Diagram of the Am29116/Am9520 Disk Controller

disk reads, the Am29116 maintains two pointers: a write pointer for transferring data from the FIFO array to the buffer memory at a rate close to 30MHz, and a read pointer for concurrently transferring data from the buffer memory to the burst error processor at a rate equivalent to 15MHz. During disk writes, in which the timing of the checksum calculation is more critical, the transfers are not overlapped. If the data transfer rate needed is 20Mbit/sec or less in an alternative design, the burst error processor can be placed in line with the FIFO array. Table 2 lists the interface signals between the controller and up to eight drives.

TABLE 2. CONTROLLER/DRIVE INTERFACE SIGNALS

SYMBOL	PROSE SIGNAL NAME	SIGNAL SOURCE
$\overline{ADMC}$	Address Mark Control	Controller
$\overline{ATTN}$	Attention	Selected Drive
$\overline{BACK}$	Bus Acknowledge	Selected Drive
$\overline{BOUT}$	Bus Direction Out	Controller
$\overline{BUSY}$	Busy	Selected Drive
$\overline{CBPA}$	Control Bus Parity	Controller or Selected Drive
$\overline{CBDA}_{0-7}$	Control Bus Data (multiplexed with $SADR_{0-7}$)	Controller or Selected Drive
$\overline{CREQ}$	Command Request	Controller
$\overline{INDX}$	Index	Selected Drive
$\overline{PENB}$	Port Enable	Controller
$\overline{PREQ}$	Parameter Request	Controller
$\overline{RDCM}$	Read/Reference Clock -	Selected Drive
$\overline{RDCP}$	Read/Reference Clock +	Selected Drive

TABLE 2 CONTROLLER/DRIVE INTERFACE SIGNALS (Cont.)

SYMBOL	PROSE SIGNAL NAME	SIGNAL SOURCE
$\overline{RDDM}$	Read Data -	Selected Drive
$\overline{RDDP}$	Read Data +	Selected Drive
$\overline{RDGA}$	Read Gate	Controller
$\overline{SADR}_{0-7}$	Select/Attention Drive$_{0-7}$ (multiplexed with $\overline{CBDA}_{0-7}$)	Controller or Selected Drive
$\overline{SAMD}$	Sector/Address Mark Detected	Selected Drive
$\overline{SAST}$	Select/Attention Strobe	Controller
$\overline{WRCM}$	Write Clock -	Controller
$\overline{WRCP}$	Write Clock +	Controller
$\overline{WRDM}$	Write Data -	Controller
$\overline{WRDP}$	Write Data +	Controller
$\overline{WRGA}$	Write Gate	Controller

The host CPU and memory interface is through either DMA or a host data channel, depending upon the host machine and application. Although the interface is not shown in detail, it can readily be implemented using the Am2940 DMA Address Generator and the Am2950 Parallel I/O Data Port.

Figure 5 depicts the byte-sync logic and timing logic for the FIFO buffer. It has been assumed here that the encoding scheme used by the drives is one that employs all-zero preambles (e.g., Modified Frequency Modulation). If 3PM or any other non-zero-preamble scheme is used, the byte-sync logic shown must be appropriately redesigned. Redesign of the byte-sync logic will also be necessary for drives that suppress transmission of part or all of the preamble.

Byte sync is achieved by three binary counters, which present and maintain a low output as soon as at least K zeroes followed by binary 11111110 (hexadecimal FE) have been encountered. The value of K may be "programmed" by means of the D, C, B, A

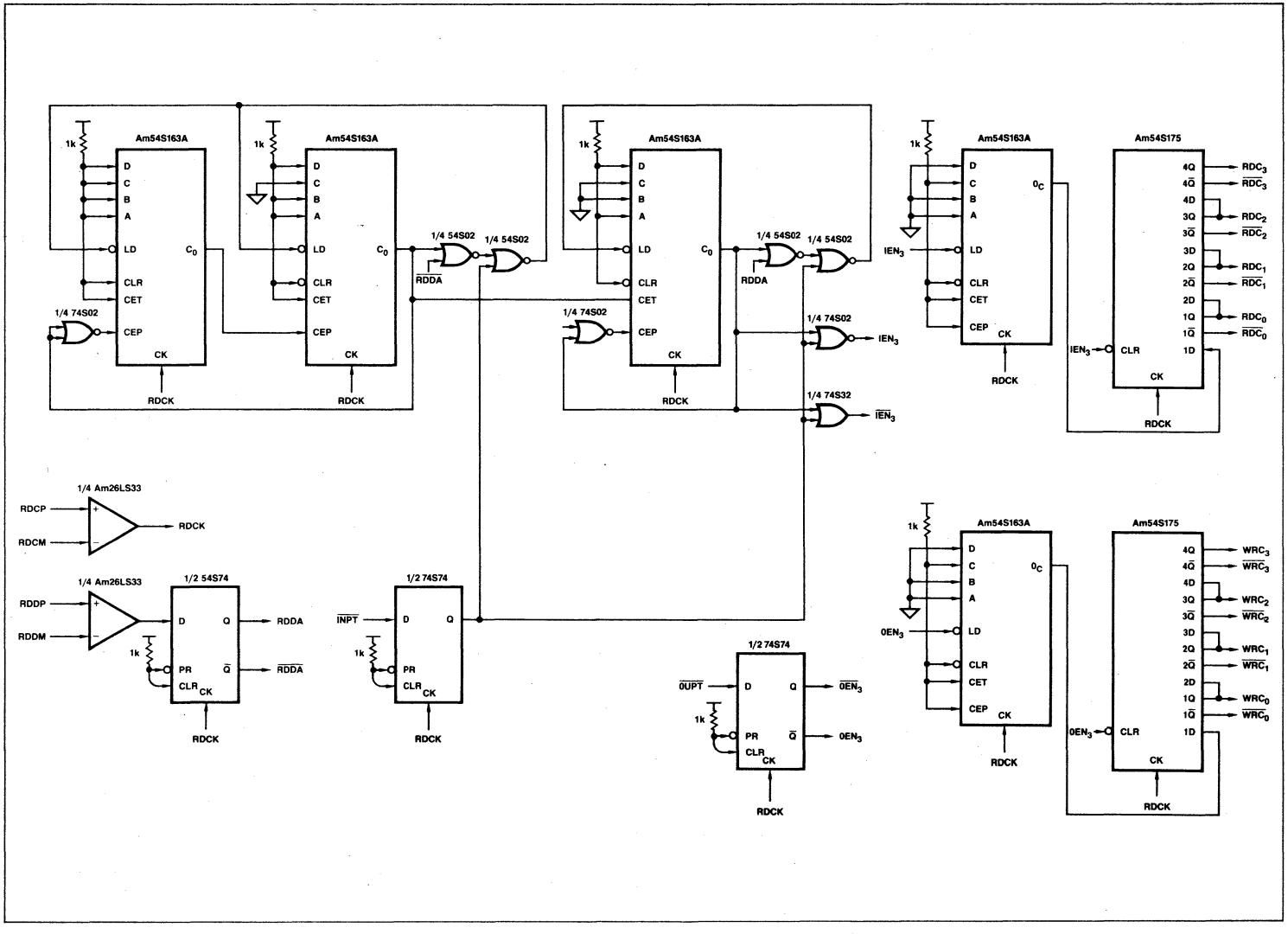


Figure 5. Byte-Sync and Timing Logic

inputs to U1 and U2. These inputs are shown tied to hexadecimal F7. Since FF_{16} - $F7_{16}$ = 08_{16} = 08_{10}, K = 8 for this instance. Higher values of K may render the detector unduly sensitive to phase locktime jitter and should be avoided. The bits first encountered during a sync burst are the least likely to be sampled correctly, since the drive's clock/data separator is still acquiring phase lock with the sync byte train. The optimal choice for K depends upon the acquisition rate and other characteristics of the clock/data separator.

Figure 6 depicts the serial-to-parallel and parallel-to-serial conversion interface using an array of 9403As operated in

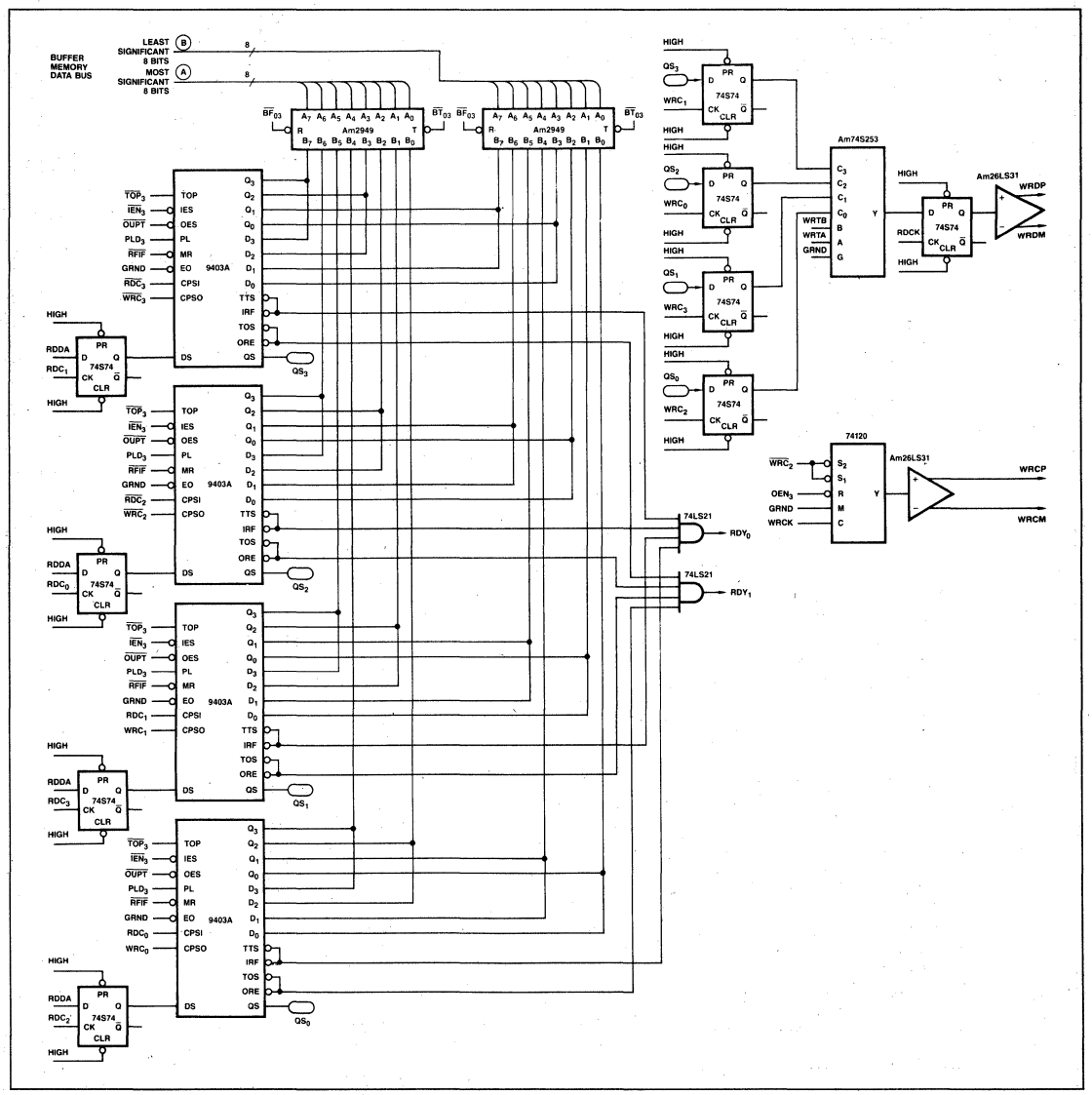


Figure 6. Serial: Parallel Interfacing

parallel at an aggregate rate of 30Mbit/sec per second. The FIFOs themselves are individually operated at 7.5Mbit/sec per second, and the 30Mb aggregate data rate is achieved by an alternate clocking scheme (Figure 7). This same scheme is used for both read and write clocking and that the FIFO serial input and output clocks, $\overline{CPSI}$ and $\overline{CPSO}$, are falling-edge active. Pipelining is used to satisfy the setup time requirements of the FIFO serial inputs, DS. The FIFO serial outputs QS are also pipelined. However, the FIFO parallel inputs and outputs, D3-D0 and Q3-Q0, are fast enough to communicate with the buffer memory bus without pipelining.

The major elements of the remaining portion of the data path are the Am29116, the Am9520 and 4096 words of Am9147-55 buffer memory (Figure 8). These elements interface through an internal 16-bit data bus. The Am29116 is connected to this bus through two Am2949 bidirectional bus transceivers. During data compression operations, the read and write data are actually routed through two sets of Am27S291 translation PROMs. The Am29116 also generates and maintains the buffer memory addresses. The buffer memory comprises sixteen Am9147-55 4096 x 1 RAMs. It contains images of the last eight sectors read from or written to disk, the I/O request queues, and additional

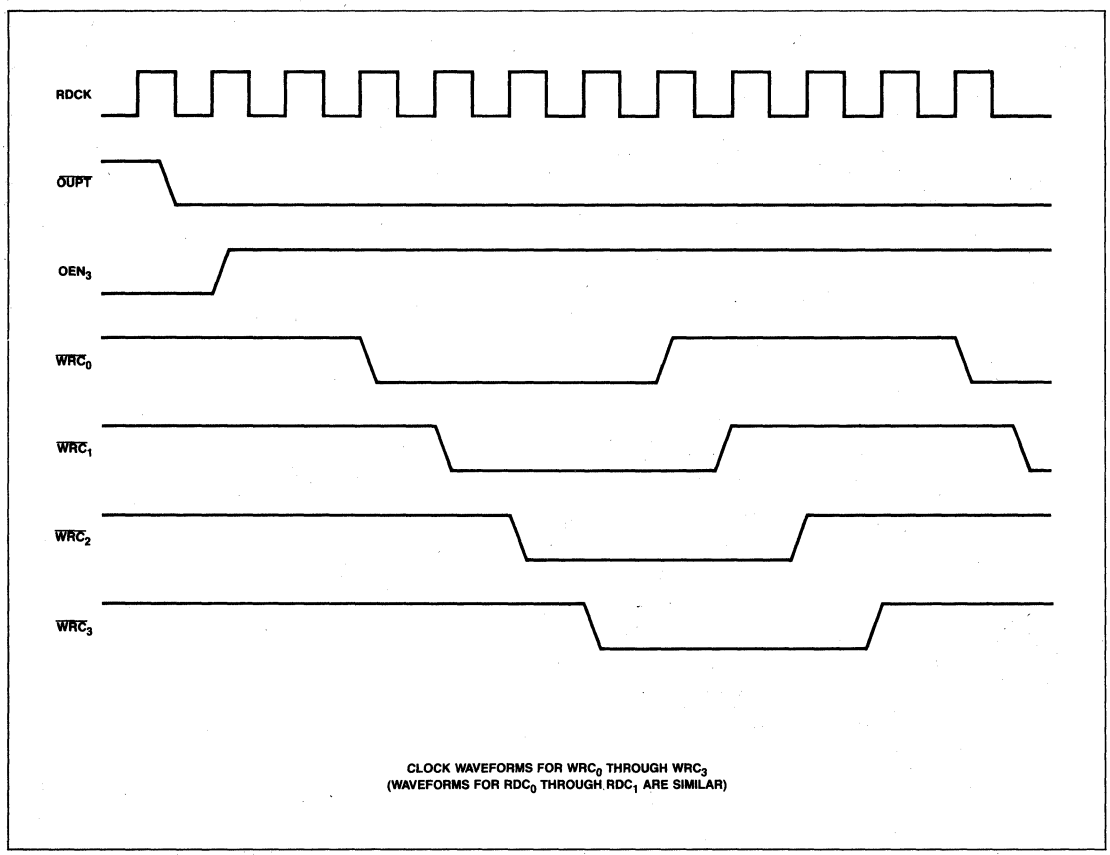


Figure 7. FIFO Alternate Clocking

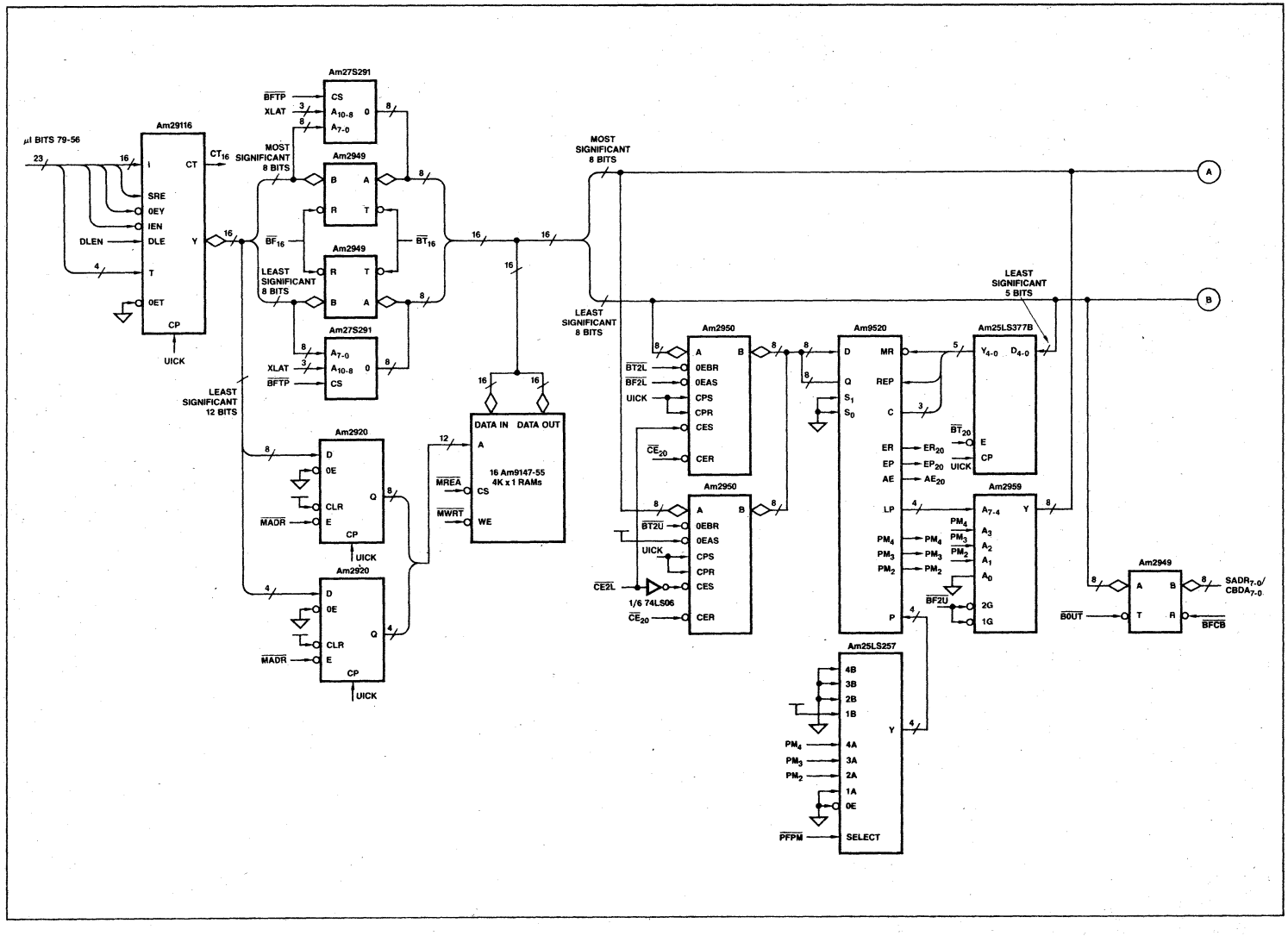


Figure 8. Processors and Buffer Memory

housekeeping tables. The 8-bit data input and output lines of the Am9520 are connected to the 16-bit internal data bus through a low and high byte bidirectional I/O port using two Am2950s. The instruction (C2-0) and read error pattern (REP) inputs of the Am9520 are generated by the Am29116 and are strobed into the command register under microprogram control. The Am9520 status signals--located error pattern (LP3-0) and pattern match (PM4-2)--are communicated to the Am29116 through the Am2959 buffer during high-speed error correction. In addition, the ANSI Control Bus Data ($CBDA_{7-0}$) and the Select/Attention Drive ($\overline{SADR}_{7-0}$) signals to and from the selected drive are multiplexed and connected to the least significant byte of the internal data bus through an Am2949 bidirectional bus transceiver.

The Am2910 microprogram sequencer generates the next address to 1K words of control memory (Figure 9). The control memory is 80 bits wide and is configured using ten Am27S35 1024 x 8 registered PROMs. The test condition ($\overline{CC}$) input to the Am2910 comes from one of sixteen sources (including a forced HIGH and a forced LOW) selected through multiplexers by five microinstruction bits. Except for the Am29116 CT status output, all of the test conditions are synchronized by the microinstruction clock (MICK) because they are from such asynchronous sources as the disk drives and the FIFO array.

Microinstruction Format

The format of the 80-bit microinstruction is outlined in Figure 10. The intent here is not to create a minimum-width, shared-field control word but to demonstrate microcoding the controller in a straightforward manner. Table 3 details the definition for each of the fields. A microinstruction word and field definition (DEF) file incorporating these is available to System 29 users.

Sample microcode has been written (and a source (SRC) file is available to System 29 users) for uncompressed sector read and write operations. The header and data segment format is shown in Figure 11. The code includes header and sector acquisition, error checking of the header (via CRC), and error checking and correction of the data segments (via the Am9520 and its 56-bit modified Fire code polynomial) (Figure 12).

The sector input/output microroutine (SECTIO) performs input or output of a single 256-byte sector. Seek and retry operations are the responsibility of the calling microprogram.

At entry to SECTIO, R0 contains 0 to request a sector read, or +1 to request a sector write. R1 contains the I/O head number in its upper byte. The I/O track number is split between the lower byte of R1 and the upper byte of R2, while the lower byte of R2 contains the I/O sector number. R3 contains the buffer memory start address.

SECTIO first checks to see whether (R0) = +1 and, if so, uses the Am9520 to calculate the 56-bit modified Fire Code check bits that are to be appended during write. The check bits are stored in buffer memory immediately following the data.

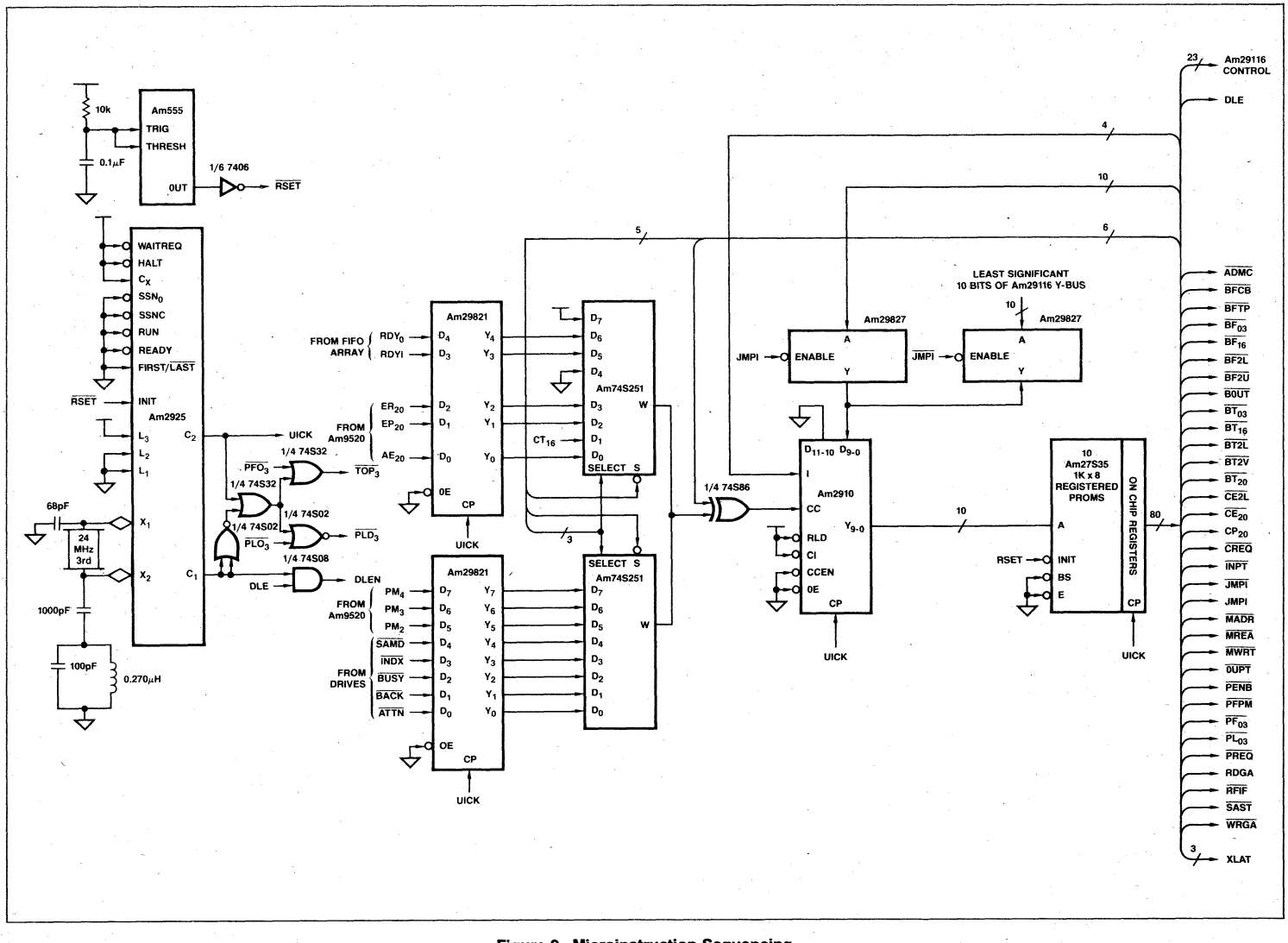


Figure 9. Microinstruction Sequencing

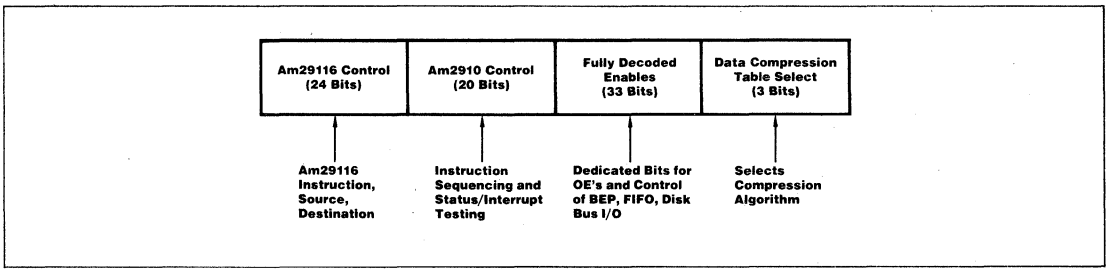


Figure 10. Microinstruction Format

TABLE 3. MICROINSTRUCTION FIELDS

MICROINSTRUCTION FIELD BITS	WIDTH (BITS)		MNEMONIC
79-64	16	I15-I0	Am29116 Instruction
63-60	4	T4-T1	Am29116 Conditional Test Select
59	1	SRE	Am29116 Status Register Enable
58	1	OEY	Am29116 Output Enable Y-Bus
57	1	IEN	Am29116 Instruction Enable
56	1	DLE	Am29116 Data Latch Enable
55-52	4	I3-I0	Am2910 Instruction
51-42	10	D9-D0	Am2910 Direct Input
41-36	6	-	Test Multiplexer Condition and True/False Select
35	1	$\overline{\text{ADMC}}$	Address Mark Control (Table 1)
34	1	$\overline{\text{BFCB}}$	(Enable Memory) Bus From (Disk Drive) Control Bus
33	1	$\overline{\text{BFTP}}$	(Enable Memory) Bus From Translate PROM
32	1	$\overline{\text{BFO3}}$	(Enable Memory) Bus From 9403A FIFO Array
31	1	$\overline{\text{BF16}}$	(Enable Memory) Bus From Am29116 Y-Bus
30	1	$\overline{\text{BF2L}}$	(Enable Memory) Bus Lower Byte From Am9520 Q-Bus
29	1	$\overline{\text{BF2U}}$	(Enable Memory) Bus Upper Byte From Am9520 Q-Bus
28	1	$\overline{\text{BOUT}}$	Bus Direction OUT (Table 1)
27	1	$\overline{\text{BTO3}}$	(Enable Memory) Bus To 9403A FIFO Array
26	1	$\overline{\text{BT16}}$	(Enable Memory) Bus To Am29116 Y-Bus
25	1	$\overline{\text{BT2L}}$	(Enable Memory) Bus Lower Byte To Am9520 D-Bus
24	1	$\overline{\text{BT2U}}$	(Enable Memory) Bus Upper Byte To Am9520 D-Bus
23	1	$\overline{\text{BT20}}$	(Enable Memory) Bus To Am9520 REP, P3-P0, & C2-C0
22	1	$\overline{\text{CE2L}}$	Clock Enable Am9520 To Lower-Byte Bus Interface Register
21	1	$\overline{\text{CE20}}$	Clock Enable Memory Bus To Am9520 Interface Registers
20	1	$\overline{\text{CP20}}$	Clock Pulse For Am9520 (Microcoded Waveform)

TABLE 3. MICROINSTRUCTION FIELDS (Cont.)

MICROINSTRUCTION BITS	FIELD WIDTH (BITS)	MNEMONIC	DESCRIPTION
19	1	$\overline{\text{CREQ}}$	Command Request (Table 1)
18	1	$\overline{\text{INPT}}$	(Enable Serial Data) Input To 9403A FIFO Array
17-16	2	$\overline{\text{JMPI}}$	(Enable) Jump Indirect Am29116 Y-Bus (Double-Rail)
15	1	$\overline{\text{MADR}}$	(Enable Loading Of Buffer) Memory Address Register
14	1	$\overline{\text{MREA}}$	(Enable Buffer) Memory Read
13	1	$\overline{\text{MWRT}}$	(Enable) Memory Write Operation
12	1	$\overline{\text{OUPT}}$	(Enable Serial Data) Output From 9403A FIFO Array
11	1	$\overline{\text{PENB}}$	Parameter Enable (Table 1)
10	1	$\overline{\text{PFPM}}$	(Enable Setting Of Am9520) P Bits From Am9520 PM Bits
09	1	$\overline{\text{PFO3}}$	(Enable) Parallel Fetch From 9403A FIFO Array
08	1	$\overline{\text{PLO3}}$	(Enable) Parallel Load Of 9403A FIFO Array
07	1	$\overline{\text{PREQ}}$	Parameter Request (Table 1)
06	1	$\overline{\text{RDGA}}$	Read Gate (Table 1)
05	1	$\overline{\text{RFIF}}$	Reset 9403A FIFO Array
04	1	$\overline{\text{SAST}}$	Select/Attention Strobe (Table 1)
03	1	$\overline{\text{WRGA}}$	Write Gate (Table 1)
02-0	3	XLAT	Translate Table Select For Data Compression PROM

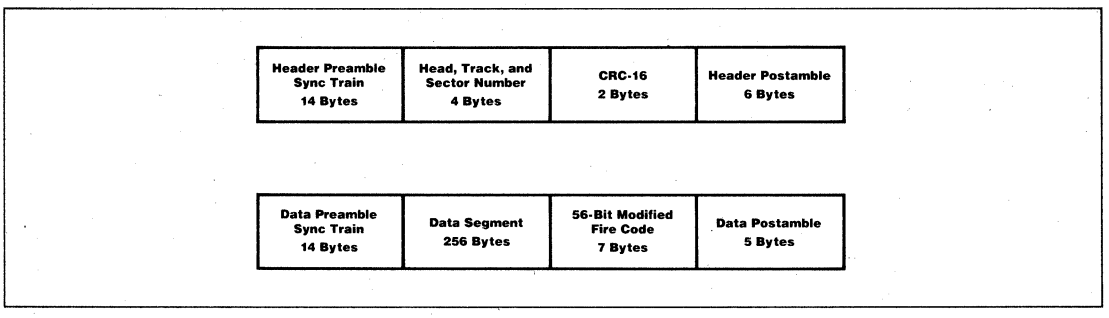


Figure 11. Header and Data Segments

SECTIO then (both for reads and for writes) uses the Am29116 to calculate the CRC of the header contained in R1 and R2. This CRC is saved in R4.

A search is then made of the entire track for a header whose head, track, sector, and CRC fields match the contents of R1, R2, and R4. If the search fails, R0 is loaded with +1 (defective or missing header) and control is returned to the calling microprogram. If the search is successful, control is passed (via (R0) and table BRTABL) to either the read sector (RDSEC1) or the write sector (WRSEC1) microcode module.

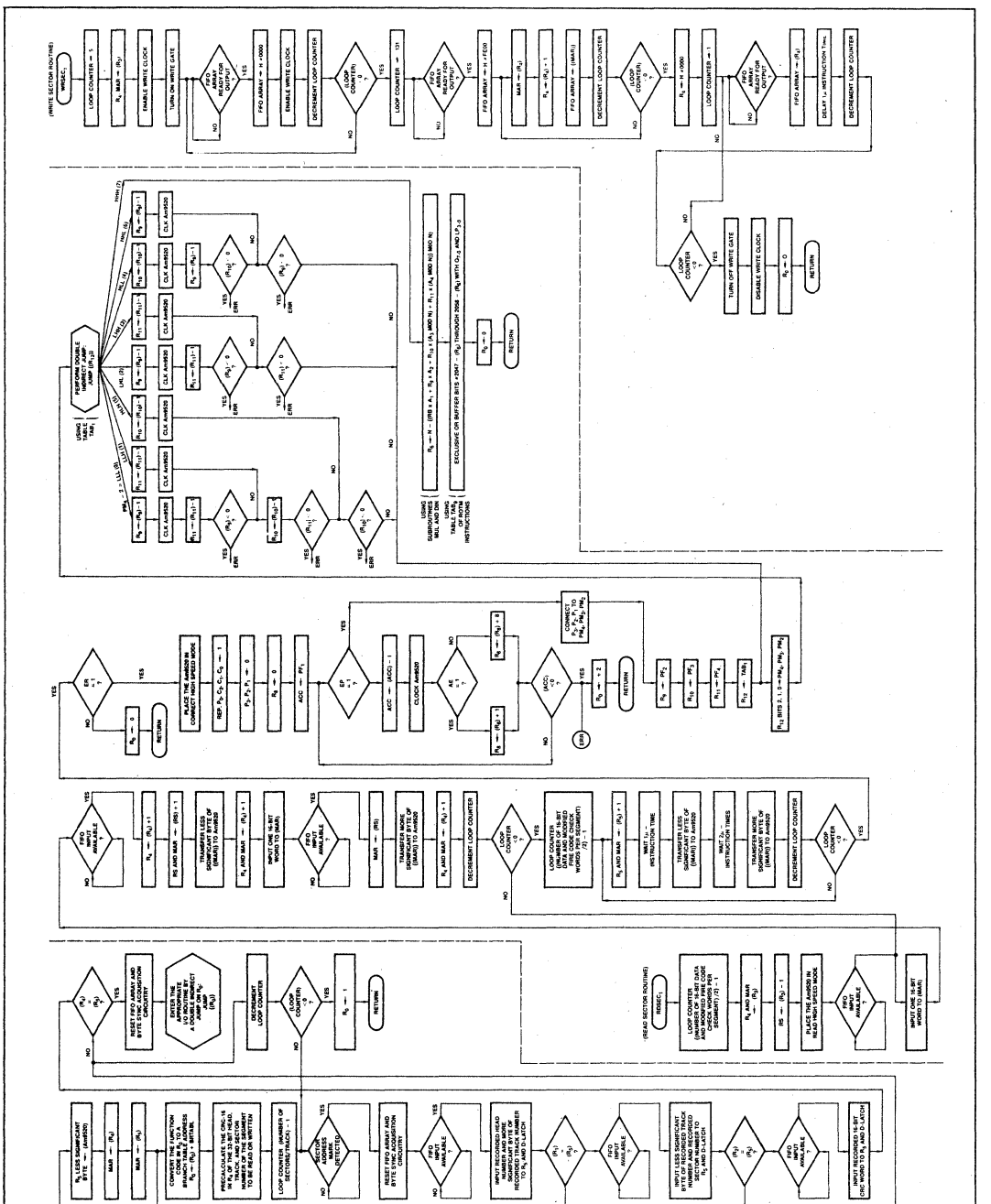


Figure 12. Microcode Logic

Read Sector Microcode Module (RDSEC1)

This module transfers synchronized information, a 16-bit word at a time, from the 9403A FIFO array to buffer memory and from buffer memory to the Am9520 operating in Read High-Speed mode. Since the current Am9520 data sheet only guarantees operation at 20MHz, some form of buffering must be used between the 30MHz disk and the Am9520. This is accomplished by using R4 as a memory buffer pointer for transfer in from the 9403A's and R5 as a pointer for transfer out to the Am9520. For simplicity in the microcode loop, R5 increments at half (rather than two-thirds) the rate at which R4 increments.

At the end of the read loop, R5 has advanced halfway through the data read in and a second loop is executed to process the remaining half of the data through the Am9520.

When all the data have been processed by the Am9520 Read High-Speed operation, the Am9520 error (ER) flag is tested to determine whether an error was detected. If ER is low (no error), R0 is loaded with 0 (operation completed successfully) and control is returned to the calling program.

If ER is high, error correction is performed using the Am9520's correct high speed mode. This uses the Chinese Remainder Theorem method to calculate the error location (as a bit displacement from the end of the data segment) and error pattern (a 12-bit mask). The error is corrected by exclusive or-ing the error pattern with the 12-bit data field beginning at the error location. The capabilities of the Am9520 and the properties of the 56-bit modified Fire Code polynomial make this correction technique extremely fast. Less than 200 microseconds are required for a worst-case error location and correction using the microcode shown.

The location of an error burst is calculated by:

$$L = N \times K - (M_1 \times A_1 + M_2 \times A_2 + M_3 \times A_3 + M_4 \times A_4)$$

where:

L is the difference in position between the last bit transferred and the beginning of the burst error.

N is the composite period of the 56-bit polynomial and is equal to 585,442.

K is the smallest integer such that L is positive.

A_1, A_2, A_3, and A_4 are Chinese Remainder Theorem coefficients:

$A_1 = 452,387$
$A_2 = 2,521,904$
$A_3 = 578,864$
$A_4 = 2,647,216$

M_1, M_2, M_3, and M_4 are factor match clock counts that are accumulated by the microcode while clocking the Am9520 in Correct High-Speed mode. For burst errors of length not exceeding 11 bits, it can be shown that M_1 will never exceed 22 (the period of the first factor of the 56-bit polynomial); M_2 will never exceed 13 (period of the second

factor); M_3 will never exceed 89 (period of the third factor); and M_4 will never exceed 23 (period of the fourth factor).

Consequently, the maximum number of Am9520 clock cycles needed to locate an 11-bit (or shorter) error burst is the sum of the first period and the maximum of the remaining three periods:

$$22 + MAX\ (13, 89, 23) = 22 + 89 = 111$$

It should be noted that the above number of Am9520 clock cycles is far less than the composite period, 585,442, which is the upper limit for correct normal operations and is representative of how long a less sophisticated part would require to locate and correct the error burst.

To perform error location and correction, the Am9520 is placed in correct high-speed mode and its clock enable P0 is set high for factor match clock count M_1 accumulation. R8 is initialized to 0 to serve as the M_1 counter. PF_1 (the maximum permissible value for M_1, which will be exceeded only for multiple bursts or bursts longer than 11 bits) is loaded into the accumulator (ACC). The EP output is tested. If EP is low, alignment exception (AE) is tested while the ACC is decremented and the Am9520 is clocked. If AE is high, the burst error is not on a byte boundary and R8 is incremented by 1. If AE is low, R8 is incremented by 8. The ACC is now tested. If positive, PF1 is not exceeded and a loop back to the EP test is performed. If negative, an uncorrectable error exists; R0 is set to +2; and control is returned to the calling microprogram. If EP is high, the M_1 calculation is complete; the error pattern is available; and M_2 through M_4 can now be accumulated.

The inherent parallelism of the Am9520 is then exploited by concurrently accumulating M_2 through M_4. This reduces the number of Am9520 clocks required from the sum of the three periods (125) to their maximum (89). R9 through R11 serve as the counters for M_2 through M_4. The microprogram flow of control reflects the completeness or incompleteness of each factor match by looping through a jump table indexed by the Am9520 Pattern Match (PM_2 through PM_4) outputs, and by selectively disabling the P_1 through P_3 clock enables with the same PM_2 through PM_4 outputs. This yields eight possible paths (Figure 12), in each of which the appropriate combination of R9 through R11 can be operated upon and tested to see if it exceeds period factor limits (i.e., a multiple-burst error or an error burst longer than 11 bits has been encountered).

Once M_1 through M_4 have been obtained, the expression:

$$(M_1 \times A_1 + M_2 \times A_2 + M_3 \times A_3 + M_4 \times A_4)$$

is evaluated by calling a specialized multiply subroutine (MUL) four times. This subroutine utilizes the special nature both of the period factor values and of the Chinese Remainder Theorem coefficients to maximize throughput. A specially optimized divide subroutine (DIV) is then called to calculate:

$$(M_1 \times A_1 + M_2 \times A_2 + M_3 \times A_3 + M_4 \times A_4) / N$$

leaving a remainder of (-L + N). One additional subtract obtains L*.

The word-boundary address of the error burst in buffer memory is extracted from L using the Am29116 Rotate and Merge instruction. A 16-way branch on the low-order 4 bits of L is used to enter a table (TAB2) of Rotate and Merge instructions.

These align the error pattern (using a single ROTM instruction if the error burst does not cross a word boundary and two instructions if it does). The error burst is then exclusive OR-ed with the aligned error pattern; R0 is loaded with 0 (operation completed successfully); and control is returned to the calling microprogram.

Write Sector Microcode Module (WRSEC1)

This module transfers information one 16-bit word at a time to the 9403A FIFO array. The information transferred comprises a data preamble (13 all-zero bytes), data sync byte (hexadecimal FE), 256 data bytes, 7 check bytes, and a data postamble (5 all-zero bytes). Both the data bytes and the check bytes are located in buffer memory, beginning at word (R3). (Calculation of the check bytes has already occurred at the beginning of SECTIO).

R0 is loaded with 0 (operation completed successfully) and control is returned to the calling program.

Conclusion

The high-speed and parallel architecture of the Am29116 and Am9520-based controller allows handling of high data transfer rate disk drives and complex data manipulation and management. The availability of cost-effective microprogrammable building blocks in the Am2900 Family has led to systems with increasingly distributed control. This allows functions to be performed at system locations that optimize overall cost/performance.

Significant improvements in host computer system performance can be realized by down-loading many time-consuming operating system tasks into the controller firmware. This allows mainstream processing of the application programs to proceed with minimal I/O overhead. System response is enhanced and main storage usage, software requirements and system overhead are reduced.

* The method used here to obtain the error location is not the only one possible. One alternative is to subtract some form of the Chinese Remainder Theorem coefficients iteratively instead of multiplying and dividing. With each subtraction L would be tested. If negative, N would be added to L. This approach still exploits the parallel nature of the Am9520.

```
AMDOS/29 AMDASM MICRO ASSEMBLER, V1.4
AM29116 / AM9520 DISK CONTROLLER 9/81 TABLER-KITSON

 ;
 ; This .DEF file (DISKCTLR.DEF) was created by editing CONTROLR.DEF;
 ; by adding DEF and EQU statements, deleting some others, and by
 ; changing the basic microword format.  The bulk of the effort required
 ; to create such a file was considerably reduced by beginning from the
 ; "master" file (CONTROLR.DEF) rather than typing a new file from scratch.
 ;
 ; This particular .DEF file was created for a specific Am29116-Am9520
 ; disk controller, described in the AMD application note:
 ; "A High-Performance Intelligent Disk Controller," by Otis Tabler and
 ; Brad Kitson, to be released by AMD in early 1982.  The source file
 ; is DISKCTLR.SRC.
 ;
 ; The major difference between this DEF file and the CONTROLR.DEF file is
 ; the approach to the microprogramming.  This file makes heavy use of
 ; DEF statement overlays while the other uses the comma-positional
 ; notation.  The choice is a matter of preference. THE Am29116 MNEMONICS
 ; AND INSTRUCTION LAYOUT ARE IDENTICAL IN THESE FILES.
 ;
 ;
 ; This file may also be used as a master file which the user can edit to
 ; suit his/her application.
 ;
 ; Anyone finding an error in this file is requested to send a marked listing
 ; or portion thereof to: AMD APPLICATIONS      or  AMD CUSTOMER EDUCATION CENTER
 ;                        PO BOX 453  MS#70         PO BOX 453  MS#71
 ;                        SUNNYVALE, CA 94086       490-A LAKESIDE DRIVE
 ;                                                  SUNNYVALE, CA 94086
 ;
 ; Advanced Micro Devices reserves the right to make changes in its product
 ; without notice in order to improve design or performance characteristics.
 ; The company assumes no responsibility for the use of any circuits or
 ; programs described herein.
 ;
 ;
 ; Am29116 Mnemonics Copyright (c) 1982 Advanced Micro Devices, Inc.
 ;
 ;
 ;
 ;
 WORD    80
 ;
 ; ************************************************
 ; GENERAL MNEMONICS
 ; ************************************************
 ;
 ; BYTE - WORD MODE SELECT [M] <---------- referenced by DEF statements
 ;
 B:              EQU             1B#0    ; BYTE MODE
 W:              EQU             1B#1    ; WORD MODE
 ;
 ;
 ; ************************************************
 ; N SELECT [N]
 ;
 N0:             EQU             H#0     ; 0
 N1:             EQU             H#1     ;
 N2:             EQU             H#2     ;
 N3:             EQU             H#3     ;
 N4:             EQU             H#4     ;
 N5:             EQU             H#5     ;
 N6:             EQU             H#6     ;
 N7:             EQU             H#7     ;
 N8:             EQU             H#8     ;
 N9:             EQU             H#9     ;
 NA:             EQU             H#A     ;
 NB:             EQU             H#B     ;
 NC:             EQU             H#C     ;
 ND:             EQU             H#D     ;
 NE:             EQU             H#E     ;
 NF:             EQU             H#F     ;
```

```
;
; ****************************************************
; 32 RAM REGISTERS [R]
;
R0:            EQU          5D#0     ; 00000
R1:            EQU          5D#1     ;
R2:            EQU          5D#2     ;
R3:            EQU          5D#3     ;
R4:            EQU          5D#4     ;
R5:            EQU          5D#5     ;
R6:            EQU          5D#6     ;
R7:            EQU          5D#7     ;
R8:            EQU          5D#8     ;
R9:            EQU          5D#9     ;
R10:           EQU          5D#10    ;
R11:           EQU          5D#11    ;
R12:           EQU          5D#12    ;
R13:           EQU          5D#13    ;
R14:           EQU          5D#14    ;
R15:           EQU          5D#15    ;
R16:           EQU          5D#16    ;
R17:           EQU          5D#17    ;
R18:           EQU          5D#18    ;
R19:           EQU          5D#19    ;
R20:           EQU          5D#20    ;
R21:           EQU          5D#21    ;
R22:           EQU          5D#22    ;
R23:           EQU          5D#23    ;
R24:           EQU          5D#24    ;
R25:           EQU          5D#25    ;
R26:           EQU          5D#26    ;
R27:           EQU          5D#27    ;
R28:           EQU          5D#28    ;
R29:           EQU          5D#29    ;
R30:           EQU          5D#30    ;
R31:           EQU          5D#31    ;
;
;
;
; *****************************
; SINGLE OPERAND INSTRUCTIONS
; *****************************
;
; OPCODES [1]
;
MOVE:          EQU          H#C      ; 1100 MOVE
COMP:          EQU          H#D      ; 1101 COMP
INC:           EQU          H#E      ; 1110 INC      INCREMENT
NEG:           EQU          H#F      ; 1111 NEG      INCREMENT COMP
;
; SOURCE-DESTINATION SELECT [2]
;
SORA:          EQU          H#0      ; RAM    ACC
SORY:          EQU          H#2      ; RAM    Y BUS
SORS:          EQU          H#3      ; RAM    STATUS
SOAR:          EQU          H#4      ; ACC    RAM
SODR:          EQU          H#6      ; D      RAM
SOIR:          EQU          H#7      ; I      RAM
SOZR:          EQU          H#8      ; 0      RAM
SOZER:         EQU          H#9      ; D(OE)  RAM
SOSER:         EQU          H#A      ; D(SE)  RAM
SORR:          EQU          H#B      ; RAM    RAM
;
; ***********************************************************
SOR: DEF 1V,  B#10,4V%D#,    4V%D#,         5V%D#,64X    ; SINGLE OPERAND RAM
;            \             \          \              \
;              MODE,QUAD,OPCODE,SOURCE-DEST,REGISTER
;              [M]          [1]        [2]         [R]      <---- refer to proper EQU groups
; ***********************************************************
```

```
;
; SOURCE (R/S) [3]
;
SOA:            EQU             H#4     ; ACC
SOD:            EQU             H#6     ; D
SOI:            EQU             H#7     ; I
SOZ:            EQU             H#8     ; 0
SOZE:           EQU             H#9     ; D(0E)
SOSE:           EQU             H#A     ; D(SE)
;
; DESTINATION [4]
;
NRY:            EQU             D#0     ; Y BUS
NRA:            EQU             D#1     ; ACC
NRS:            EQU             D#4     ; STATUS
NRAS:           EQU             D#5     ; ACC,STATUS
;
; ***************************************************************
SONR: DEF 1V,  B#11,4V%D#,    4V%D#,    5V%D#,64X        ; SINGLE OPERAND NON-RAM
;
;               MODE,QUAD,OPCODE,SOURCE,DESTINATION
;               [M]         [1]    [3]      [4]
; ***************************************************************
;
;
;
; ***********************************
; TWO OPERAND INSTRUCTIONS
; ***********************************
;
; OPCODES [5]
;
SUBR:           EQU             H#0     ; S minus R
SUBRC:          EQU             H#1     ; S minus R with carry
SUBS:           EQU             H#2     ; R minus S
SUBSC:          EQU             H#3     ; R minus S with carry
ADD:            EQU             H#4     ; R plus S
ADDC:           EQU             H#5     ; R plus S with carry
AND:            EQU             H#6     ; R . S
NAND:           EQU             H#7     ; R . S
EXOR:           EQU             H#8     ; R   S
NOR:            EQU             H#9     ; R + S
OR:             EQU             H#A     ; R + S
EXNOR:          EQU             H#B     ; R   S
;
;
; SOURCE-DESTINATION [6]                  ; R     S       DEST
;
TORAA:          EQU             H#0     ; RAM   ACC     ACC
TORIA:          EQU             H#2     ; RAM   I       ACC
TODRA:          EQU             H#3     ; D     RAM     ACC
TORAY:          EQU             H#8     ; RAM   ACC     Y BUS
TORIY:          EQU             H#A     ; RAM   I       Y BUS
TODRY:          EQU             H#B     ; D     RAM     Y BUS
TORAR:          EQU             H#C     ; RAM   ACC     RAM
TORIR:          EQU             H#E     ; RAM   I       RAM
TODRR:          EQU             H#F     ; D     RAM     RAM
;
; ***************************************************************
TOR1: DEF 1V,  B#00,4V%D#,          4V%D#,    5V%D#,64X   ; TWO OPERAND RAM (1)
;
;               MODE,QUAD,SOURCE-DEST,OPCODE,REGISTER
;               [M]         [6]       [5]     [R]
; ***************************************************************
```

```
;
;
; SOURCE-DESTINATION [7]                          R     S       DEST
;
TODAR:          EQU             H#1     ; D     ACC     RAM
TOAIR:          EQU             H#2     ; ACC   I       RAM
TODIR:          EQU             H#5     ; D     I       RAM
;
; ************************************************************
TOR2: DEF 1V,  B#10,4V%D#,          4V%D#,     5V%D#,64X   ; TWO OPERAND RAM (2)
;
;               MODE,QUAD,SOURCE-DEST,OPCODE,REGISTER
;               [M]           [7]       [5]    [R]
; ************************************************************
;
; SOURCE   [8]                                  R     S
;
TODA:           EQU             H#1     ; D     ACC
TOAI:           EQU             H#2     ; ACC   I
TODI:           EQU             H#5     ; D     I
;
; ************************************************************
TONR: DEF 1V,   B#11,4V%D#,     4V%D#,     5V%D#,64X       ; TWO OPERAND NON-RAM
;
;               MODE, QUAD,SOURCE,OPCODE,DESTINATION
;               [M]           [8]     [5]     [4]
; ************************************************************
; ****************************************************
; SHIFT INSTRUCTIONS
; ****************************************************
;
; DIRECTION AND INPUT [9]
;
SHUPZ:          EQU             H#0     ; UP 0
SHUP1:          EQU             H#1     ; UP 1
SHUPL:          EQU             H#2     ; UP QLINK
SHDNZ:          EQU             H#4     ; DOWN 0
SHDN1:          EQU             H#5     ; DOWN 1
SHDNL:          EQU             H#6     ; DOWN QLINK
SHDNC:          EQU             H#7     ; DOWN QC
SHDNOV:         EQU             H#8     ; DOWN QN QOVR
;
;
; SOURCE [10]
;
SHRR:           EQU             H#6     ; RAM   RAM
SHDR:           EQU             H#7     ; D     RAM
;
;
; ****************************************************
SHFTR: DEF 1V,  B#10,4V%D#,         4V%D#,     5V%D#,64X  ; SHIFT RAM
;
;               MODE,QUAD,SOURCE,DIRECT-INPT,REGISTER
;               [M]         [10]        [9]     [R]
; ****************************************************
;
;
; SOURCE [11]
;
SHA:            EQU             H#6     ; ACC
SHD:            EQU             H#7     ; D
;
;
; ****************************************************
SHFTNR: DEF 1V,  B#11,4V%D#,    4V%D#,     5V%D#,64X      ; SHIFT NON-RAM
;
;               MODE,QUAD,SOURCE,DIRECT-INP,DESTINATION
;               [M]         [11]    [9]         [4](NRY; NRA ONLY)
; ****************************************************
```

```
;
; ***************************************************
;ROTATE INSTRUCTIONS
; ***************************************************
;
; SOURCE-DESTINATION [12]
;
RTRA:           EQU             H#C     ; RAM   ACC
RTRY:           EQU             H#E     ; RAM   Y BUS
RTRR:           EQU             H#F     ; RAM   RAM
;
;
; ***************************************************
ROTR1: DEF  1V,  B#00,4V%D#,4V%D#,        5V%D#,64X      ; ROTATE RAM (1)
;
;               MODE,QUAD,N,SOURCE-DEST,REGISTER
;               [M]     [N]     [12]    [R]
; ***************************************************
;
; SOURCE-DESTINATION [13]
;
RTAR:           EQU             H#0     ; ACC   RAM
RTDR:           EQU             H#1     ; D     RAM
;
;
; ***************************************************
ROTR2: DEF  1V,  B#01,4V%D#,4V%D#,        5V%D#,64X      ; ROTATE RAM (2)
;
;               MODE,QUAD,N,SOURCE-DEST,REGISTER
;               [M]     [N]     [13]    [R]
; ***************************************************
;
; SOURCE DESTINATION [14]
;
RTDY:           EQU             D#24    ; D     Y BUS
RTDA:           EQU             D#25    ; D     ACC
RTAY:           EQU             D#28    ; ACC   Y BUS
RTAA:           EQU             D#29    ; ACC   ACC
;
;
; ***************************************************
ROTNR: DEF  1V,  B#11,4V%D#,H#C,      5V%D#,64X  ; ROTATE NON-RAM
;
;               MODE,QUAD,N,FIXED CODE,DESTINATION
;               [M]     [N]             [14]
; ***************************************************
```

6

```
; ******************************************************
; BIT ORIENTED INSTRUCTIONS
; ******************************************************
;
; OPCODES [15]
;
SETNR:          EQU             H#D     ; SET RAM, BIT N
RSTNR:          EQU             H#E     ; RESET RAM, BIT N
TSTNR:          EQU             H#F     ; TEST RAM, BIT N
;
;
; ************************************************************
BOR1: DEF 1V,  B#11,4V%D#,4V%D#,   5V%D#,64X     ; BIT ORIENTED RAM (1)
;
;               MODE,QUAD,N,OPCODE,REGISTER
;               [M]     [N]  [15]    [R]
; ************************************************************
;
;
; OPCODES [16]
;
LD2NR:          EQU             H#C     ; 2^N --- RAM
LDC2NR:         EQU             H#D     ; 2^N --- RAM
A2NR:           EQU             H#E     ; RAM + 2^N - RAM
S2NR:           EQU             H#F     ; RAM - 2^N - RAM
;
;
; ************************************************************
BOR2: DEF 1V,  B#10,4V%D#,4V%D#,   5V%D#,64X     ; BIT ORIENTED RAM (2)
;
;               MODE,QUAD,N,OPCODE,REGISTER
;               [M]     [N]  [16]    [R]
; ************************************************************
;
; OPCODES [17]
;
TSTNA:          EQU             D#0     ; TEST ACC, BIT N
RSTNA:          EQU             D#1     ; RESET ACC, BIT N
SETNA:          EQU             D#2     ; SET ACC, BIT N
A2NA:           EQU             D#4     ; ACC + 2^N -- ACC
S2NA:           EQU             D#5     ; ACC - 2^N --ACC
LD2NA:          EQU             H#6     ; 2^N -- ACC
LDC2NA:         EQU             D#7     ; 2^N -- ACC
TSTND:          EQU             D#16    ; TEST D, BIT N
RSTND:          EQU             D#17    ; RESET D, BIT N
SETND:          EQU             D#18    ; SET D, BIT N
A2NDY:          EQU             D#20    ; D + 2^N -- Y BUS
S2NDY:          EQU             D#21    ; D - 2^N -- Y BUS
LD2NY:          EQU             D#22    ; 2^N -- Y BUS
LDC2NY:         EQU             D#23    ; 2^N -- Y BUS
;
;
; ************************************************************
BONR: DEF 1V,  B#11,4V%D#,B#1100,    5V%D#,64X   ; BIT ORIENTED NON-RAM
;
;               MODE,QUAD,N,FIXED CODE,OPCODE
;               [M]     [N]             [17]
; ************************************************************
```

```
; ************************************************
; ROTATE AND MERGE
; ************************************************
;
; SOURCE-DEST SELECT [U,S,MASK-DEST] [18]
;
;                                        ROT    NON-ROT  MASK-DEST
MDAI:           EQU             H#7     ; D     ACC     I
MDAR:           EQU             H#8     ; D     ACC     RAM
MDRI:           EQU             H#9     ; D     RAM     I
MDRA:           EQU             H#A     ; D     RAM     ACC
MARI:           EQU             H#C     ; ACC   RAM     I
MRAI:           EQU             H#E     ; RAM   ACC     I
;
; ************************************************************
ROTM: DEF 1V,  B#01,4V%D#,4V%D#,        5V%D#,64X       ;ROTATE AND MERGE
;
;               MODE,QUAD,N,SOURCE-DEST,REGISTER
;               [M]     [N]     [18]        [R]
; ************************************************************
;
; ************************************************
; ROTATE AND COMPARE
; ************************************************
;
; ROT.SRC(U)-NON ROT.SRC(S)/DEST-MASK(S)[19]
;
CDAI:           EQU             H#2     ; D     ACC     I
CDRI:           EQU             H#3     ; D     RAM     I
CDRA:           EQU             H#4     ; D     RAM     ACC
CRAI:           EQU             H#5     ; RAM   ACC     I
;
; ********************************************
ROTC: DEF 1V,  B#01,4V%D#,4V%D#,            5V%D#,64X   ; ROTATE AND COMPARE
;
;               MODE,QUAD,N,SOURCE-DEST-MASK,REGISTER
;               [M]     [N]     [19]        [R]
; ********************************************
; ************************************************
; PRIORITIZE
; ************************************************
;
; SOURCE [20]
;
PRT1A:          EQU             H#7     ; ACC
PR1D:           EQU             H#9     ; D
;
;
; DESTINATION [21]
;
PR1A:           EQU             H#8     ; ACC
PR1Y:           EQU             H#A     ; Y BUS
PR1R:           EQU             H#B     ; RAM
;
; ********************************************
PRT1: DEF 1V,  B#10,4V%D#,          4V%D#,    5V%D#,64X       ; RAM ADDR MASK(S)
;
;               MODE,QUAD,DESTINATION,SOURCE,REG-MASK
;               [M]         [21]    [20]    [R]
; ********************************************
;
;
; DESTINATION [23]
;
PR2A:           EQU             H#0     ; ACC
PR2Y:           EQU             H#2     ; Y BUS
;
; MASK (S) [22]
;
PRA:            EQU             H#8     ; ACC
PRZ:            EQU             H#A     ; 0
PRI:            EQU             H#B     ; I
;
;
; ********************************************
PRT2: DEF 1V,  B#10,4V%D#,  4V%D#,  5V%D#,64X   ; PRIORITIZE RAM
;
;               MODE,QUAD,MASK,DEST,REG-SOURCE
;               [M]       [22] [23]   [R]
; ********************************************
```

```
; SOURCE (R) [24]
;
PR3R:           EQU             H#3     ; RAM
PR3A:           EQU             H#4     ; ACC
PR3D:           EQU             H#6     ; D
;
;
; ***********************************************
PRT3: DEF 1V,  B#10,4V%D#,  4V%D#,    5V%D#,64X  ; PRIORITIZE RAM
;
;               MODE,QUAD,MASK,SOURCE,REG-DEST
;               [M]       [22]  [24]    [R]
; ***********************************************
;
;
; SOURCE (R) [25]
;
PRTA:           EQU             H#4     ; ACC
PRTD:           EQU             H#6     ; D
;
;
; ***********************************************
PRTNR: DEF  1V,  B#11,4V%D#,  4V%D#,    5V%D#,64X        ; PRIORITIZE NON-RAM
;
;                  MODE,QUAD,MASK,SOURCE,DESTINATION
;                  [M]       [22]  [25]    [4](NRY,NRA ONLY)
; ***********************************************
;
; ***********************************************
; CYCLIC REDUNDANCY CHECK
; ***********************************************
;
; *****************************************
CRCF: DEF B#11001100011,5V%D#,64X         ; FORWARD
; *****************************************
;
; *****************************************
CRCR: DEF B#11001101001,5V%D#,64X         ; REVERSE
; *****************************************
;
; *****************************************
;
; NOOP
;
; *****************************************
NOOP: DEF H#7140,64X    ; NO OPERATION
; *****************************************
```

```
;
; ************************************************
; STATUS
; ************************************************
;
; OPCODE [26]
;
SONZC:          EQU             5D#3    ; SET OVR,N,C,Z
SL:             EQU             5D#5    ; SET LINK
SF1:            EQU             5D#6    ; SET FLAG 1
SF2:            EQU             5D#9    ; SET FLAG 2
SF3:            EQU             5D#10   ; SET FLAG 3
;
; ************************************************
SETST: DEF B#011,H#BA,5V%D#,64X  ; SET STATUS
;
;                           OPCODE
;                            [26]
; ************************************************
;
; OPCODE [27]
;
RONCZ:          EQU             D#3     ; RESET OVR,N,C,Z
RL:             EQU             D#5     ; RESET LINK
RF1:            EQU             D#6     ; RESET FLAG 1
RF2:            EQU             D#9     ; RESET FLAG 2
RF3:            EQU             D#10    ; RESET FLAG 3
;
;************************************************
RSTST: DEF B#011,H#AA,5V%D#,64X         ; RESET STATUS
;
;                           OPCODE
;                           [27]
; ************************************************
;
; ************************************************
SVSTR: DEF  1V,  B#10,H#7A, 5V%D#,64X   ; SAVE STATUS-RAM
;
;                  MODE,QUAD,FIXED,RAM ADDRESS/DEST
;                   [M]                [R]
; ************************************************
;
;
;************************************************
SVSTNR: DEF  1V, B#11,H#7A, 5V%D#,64X    ; SAVE STATUS NON-RAM
;
;                  MODE,QUAD,FIXED,DESTINATION
;                  [M]             [4](NRY,NRA ONLY)
; ************************************************
```

6

```
;
; ************************************************
; TEST STATUS
; ************************************************
;
; OPCODE (CT)
;
TNOZ:           EQU             D#0     ; TEST (N OVR) + Z
TNO:            EQU             D#2     ; TEST N OVR
TZ:             EQU             D#4     ; TEST Z
TOVR:           EQU             D#6     ; TEST OVR
TLOW:           EQU             D#8     ; TEST LOW
TC:             EQU             D#10    ; TEST C
TZC:            EQU             D#12    ; TEST Z + C
TN:             EQU             D#14    ; TEST N
TL:             EQU             D#16    ; TEST LINK
TF1:            EQU             D#18    ; TEST FLAG 1
TF2:            EQU             D#20    ; TEST FLAG 2
TF3:            EQU             D#22    ; TEST FLAG 3
;
;
; ******************************************************
TEST: DEF B#011,H#9A,5V%D#,64X   ;  TEST STATUS
;
;                FIXED,     OPCODE
;                           [CT]
; ******************************************************

;
; added DEF and EQU statements
;*********************************
;
;       IMMEDIATE OPERAND
;
IMME:   DEF     16V%D#, 64X
;
;       CT MULTIPLEXER CONTROL
;
CT:     DEF     16X, 4V%D#, 60X
NOZ:    EQU     H#0
NO:     EQU     H#1
Z:      EQU     H#2
OVR:    EQU     H#3
LOW:    EQU     H#4
C:      EQU     H#5
ZC:     EQU     H#6
N:      EQU     H#7
L:      EQU     H#8
F1:     EQU     H#9
F2:     EQU     H#A
F3:     EQU     H#B
;
;       STATUS REGISTER ENABLE
;
SRE:    DEF     20X, B#1, 59X
NOSRE:  DEF     20X, B#0, 59X
;
;       OUTPUT ENABLE Y
;
OEY:    DEF     21X, B#0, 58X
NOOEY:  DEF     21X, B#1, 58X
;
;       INSTRUCTION ENABLE
;
IEN:    DEF     22X, B#0, 57X
NOIEN:  DEF     22X, B#1, 57X
;
;       D-I-LATCH ENABLE
;
DLE:    DEF     23X, B#1, 56X
NODLE:  DEF     23X, B#0, 56X
```

```
;
;
;
;-------------------------------------------------
;     Am2910 COMMANDS AND BRANCH ADDRESSES
; note use of DEF statements - overlay in SRC file
;-------------------------------------------------
JZ:     DEF     24X, H#0, 10V$D#1023, 42X
CJS:    DEF     24X, H#1, 10V$D#1023, 42X
JS:     DEF     24X, H#1, 10V$D#1023, 6Q#36, 36X        ;  UNCONDITIONAL JUMP TO SUBR.
JMAP:   DEF     24X, H#2, 10V$D#1023, 42X
CJP:    DEF     24X, H#3, 10V$D#1023, 42X
JP:     DEF     24X, H#3, 10V$D#1023, 6Q#36, 36X        ;  UNCONDITIONAL JUMP
PUSH:   DEF     24X, H#4, 10V$D#1023, 42X
JSRP:   DEF     24X, H#5, 10V$D#1023, 42X
CJV:    DEF     24X, H#6, 10V$D#1023, 42X
JRP:    DEF     24X, H#7, 10V$D#1023, 42X
RFCT:   DEF     24X, H#8, 10V$D#1023, 42X
RPCT:   DEF     24X, H#9, 10V$D#1023, 42X
CRTN:   DEF     24X, H#A, 10V$D#1023, 42X
RTN:    DEF     24X, H#A, 10V$D#1023, 6Q#36, 36X        ;  UNCONDITIONAL RETURN
CJPP:   DEF     24X, H#B, 10V$D#1023, 42X
LDCT:   DEF     24X, H#C, 10V$D#1023, 42X
LOOP:   DEF     24X, H#D, 10V$D#1023, 42X
CONT:   DEF     24X, H#E, 10V$D#1023, 42X
TWB:    DEF     24X, H#F, 10V$D#1023, 42X
;                           ^
;                           |
; NOTE: For proper assembly, a "$" must be used in any field which
; will be used to accept a symbolic address in the SRC file.
;
;
;
;
;
;
;     Am2910 CONDITION CODE SELECTIONS
;
IF:     DEF     38X, 5V%D#, B#0, 36X
IFNOT:  DEF     38X, 5V%D#, B#1, 36X
;
;
AE20:   EQU     5Q#10:          ; AM9520 ALIGNMENT ERROR FLAG
CT16:   EQU     5Q#11:          ; AM29116 CONDITIONAL TEST FLAG
EP20:   EQU     5Q#12:          ; AM9520 ERROR PATTERN FLAG
ER20:   EQU     5Q#13:          ; AM9520 ERROR DETECTED FLAG
FAIL:   EQU     5Q#14:          ; UNCONDITIONAL FAILURE OF "TEST"
RDYI:   EQU     5Q#15:          ; NOT READY INPUT (DATA UNAVAILABLE FROM FIFOS)
RDYO:   EQU     5Q#16:          ; NOT READY OUTPUT (FIFOS FULL)
SUCC:   EQU     5Q#17:          ; UNCONDITIONAL SUCCESS OF "TEST"
ATTN:   EQU     5Q#20:          ; ATTENTION
BACK:   EQU     5Q#21:          ; BUS ACKNOWLEDGE
BUSY:   EQU     5Q#22:          ; BUSY
INDX:   EQU     5Q#23:          ; INDEX
SAMD:   EQU     5Q#24:          ; SECTOR / ADDRESS MARK DETECTED
PM2:    EQU     5Q#25:          ; AM9520 PATTERN MATCH 2 FLAG
PM3:    EQU     5Q#26:          ; AM9520 PATTERN MATCH 3 FLAG
PM4:    EQU     5Q#27:          ; AM9520 PATTERN MATCH 4 FLAG
```

```
;
;       MISCELLANEOUS CONTROL SIGNALS
;
ADMC:   DEF     44X, B#0, 35X   ; ADDRESS MARK CONTROL
BFCB:   DEF     45X, B#0, 34X   ; MEMORY BUS FROM DRIVE CONTROL BUS
BFTP:   DEF     46X, B#0, 33X   ; MEMORY BUS FROM TRANSLATE PROM
BF03:   DEF     47X, B#0, 32X   ; MEMORY BUS FROM 9403AS
BF16:   DEF     48X, B#0, 31X   ; MEMORY BUS FROM AM29116
BF2L:   DEF     49X, B#0, 30X   ; MEMORY BUS FROM AM9520 - LOWER BYTE
BF2U:   DEF     50X, B#0, 29X   ; MEMORY BUS FROM AM9520 - UPPER BYTE
BOUT:   DEF     51X, B#0, 28X   ; (DISK) BUS DIRECTION OUT (FROM CONTROLLER)
BT03:   DEF     52X, B#0, 27X   ; MEMORY BUS TO 9403AS
BT16:   DEF     53X, B#0, 26X   ; MEMORY BUS TO AM29116
BT2L:   DEF     54X, B#0, 25X   ; MEMORY BUS TO AM9520 - LOWER BYTE
BT2U:   DEF     55X, B#0, 24X   ; MEMORY BUS TO AM9520 - UPPER BYTE
BT20:   DEF     56X, B#0, 23X   ; MEMORY BUS TO AM9520 - CONTROL INFORMATION
CE2L:   DEF     57X, B#0, 22X   ; CLOCK ENABLE AM9520 TO LOWER-BYTE BUS INT.
CE20:   DEF     58X, B#0, 21X   ; CLOCK ENABLE MEMORY BUS TO AM9520 TRANSFER
CP20:   DEF     59X, B#0, 20X   ; CLOCK PULSE (ACTUAL WAVEFORM) FOR AM9520
CREQ:   DEF     60X, B#0, 19X   ; COMMAND REQUEST
INPT:   DEF     61X, B#0, 18X   ; INPUT SERIAL DATA TO 9403AS
JMPI:   DEF     62X, B#01, 16X  ; JUMP INDIRECT AM29116 REGISTER
NOJMPI: DEF     62X, B#10, 16X  ; NO INDIRECT JUMP
MADR:   DEF     64X, B#0, 15X   ; MEMORY ACCESS
MREA:   DEF     65X, B#0, 14X   ; MEMORY ADDRESS
MWRT:   DEF     66X, B#0, 13X   ; MEMORY WRITE
OUPT:   DEF     67X, B#0, 12X   ; OUTPUT SERIAL DATA FROM 9403AS
PENB:   DEF     68X, B#0, 11X   ; PARAMETER ENABLE
PFPM:   DEF     69X, B#0, 10X   ; SET 9520 P BITS FROM 9520 PM BITS
PF03:   DEF     70X, B#0, 9X    ; PARALLEL FETCH FROM 9403AS
PL03:   DEF     71X, B#0, 8X    ; PARALLEL LOAD INTO 9403AS
PREQ:   DEF     72X, B#0, 7X    ; PARAMETER REQUEST
RDGA:   DEF     73X, B#0, 6X    ; READ GATE
RFIF:   DEF     74X, B#0, 5X    ; RESET FIFO
SAST:   DEF     75X, B#0, 4X    ; SELECT / ATTENTION STROBE
WRGA:   DEF     76X, B#0, 3X    ; WRITE GATE
;
ASCEBC: EQU     Q#0             ; ASCII TO EBCDIC SUBSET PREFIX
BCDEBC: EQU     Q#1             ; BCD TO EBCDIC SUBSET PREFIX
EBCASC: EQU     Q#2             ; EBCDIC SUBSET TO ASCII PREFIX
EBCBCD: EQU     Q#3             ; EBCDIC SUBSET TO BCD PREFIX
;
XLAT:   DEF     77X, 3V%D#      ; TRANSLATE PREFIX
;
;
        END

TOTAL PHASE 1 ERRORS =   0
```

```
;
; CREATED 9/81 TABLER-KITSON
;
;
;
; This SRC file was created for the AMD application note:
; "A High-Performance Intelligent Disk Controller"
; by Otis Tabler and Brad Kitson.
;
; Mnemonics and word format are defined in DISKCTLR.DEF
;
; Advanced Micro Devices reserves the right to make changes in its
; product without notice in order to improve design or performance
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; use of any circuits or programs described herein.
;
; Am29116 Mnemonics Copyright (c) 1982 Advanced Micro Devices
;
;
;
;
;    SECTOR READ / WRITE SUBROUTINE
;*****************************************
;
;       INPUTS:
;
;               FUNCTION CODE IN R0:
;
;                       0 TO READ SECTOR
;
;                       +1 TO WRITE SECTOR
;
;               HEAD NUMBER IN MSB OF R1
;
;               MSB OF TRACK NUMBER IN LSB OF R1
;
;               LSB OF TRACK NUMBER IN MSB OF R2
;
;               SECTOR NUMBER IN LSB OF R2
;
;               START ADDRESS OF RAM SECTOR BUFFER IN R3
;
```

```
     ;
     ;       OUTPUT:
     ;
     ;               R0 CONTAINS:
     ;
     ;                       0       IF THE FUNCTION SPECIFIED WAS COMPLETED
     ;                               EITHER WITHOUT ERROR OR WITH A
     ;                               SUCCESSFULLY CORRECTED READ ERROR
     ;
     ;                       +1      IF THE SECTOR'S HEADER IS BAD
     ;
     ;                       +2      IF AN UNCORRECTABLE ERROR WAS DETECTED IN
     ;                               READING THE SECTOR'S DATA SEGMENT
     ;
     ;  ADDITIONAL MNEMONICS
     ; **********************
     ;
     ;
C001 CRCMSK: EQU     16H#8005   ; CRCF POLYNOMIAL MASK
0010 CRCNIT: EQU     16         ; CRCF NUMBER OF ITERATIONS (D#16 <-- default bas
     NSPASS: EQU     64         ; NUMBER OF SECTOR PASSES (SET THIS EQUAL
0040 ;                            TO THE NUMBER OF SECTORS PER TRACK.)
     RDITCT: EQU     65         ; READ ITERATION COUNT, EQUAL TO THE NUMBER
     ;                          ; OF 16-BIT WORDS (DATA PLUS MODIFIED FIRE
0041 ;                          ; CODE) PER SECTOR, DIVIDED BY TWO, MINUS 1.
0016 PF1:    EQU     22         ; PERIOD FACTOR ONE
000D PF2:    EQU     13         ; PERIOD FACTOR TWO
0059 PF3:    EQU     89         ; PERIOD FACTOR THREE
     PF4:    EQU     23         ; PERIOD FACTOR FOUR
0017 ;
E723 A1LSW:  EQU     H#E723     ; A1 CONSTANT(LEAST SIG. WORD)
0006 A1MSW:  EQU     6          ; A1 CONS.(MOST SIG. WORD)
BFA8 A2LSW:  EQU     H#BFA8     ; A2 CONS.(LEAST SIG. WORD)
D530 A3LSW:  EQU     H#D530     ; A3' CONS.(LEAST SIG. WORD)
     A4LSW:  EQU     H#A928     ; A4' CONS.(LEAST SIG. WORD)
A928 ;
7100 KL128:  EQU     H#7100     ; K(LEAST SIG. WORD) SHIFTED UP
                                ; BY SEVEN PLACES
0477 KM128:  EQU     H#0477     ; K(MOST SIG. WORD) SHIFTED UP
                                ; BY SEVEN PLACES.
EEE2 KLSW:   EQU     H#EEE2     ; K(LEAST SIG. WORD)
     KMSW:   EQU     8          ; K(MOST SIG. WORD)
0008 ;
```

```
     ;
     ;
     ;       IF THE FUNCTION CODE IN R0 EQUALS +1 (WRITE SECTOR), PRECALCULATE
     ;       THE MODIFIED FIRE CODE'S PARTIAL CHECKSUM FOR THE FIRST HALF OF
     ;       THE DATA SEGMENT TO BE WRITTEN.
     ;
0000 SECTIO: BOR2    W,0,S2NR,R0
     /       &NODLE  &NOIEN  &NOOEY  &NOSRE ;<------  note use of overlayed
     /       &CT     Z       &NOJMPI        ;         DEF statements
     /       &IFNOT  CT16    &CJP    CFCODE ;         signified by "&"
     ;
     ;
     ;       RESET THE AM9520 AND THEN PLACE IT IN COMPUTE CHECK BITS MODE.
     ;       INITIALIZE COUNTER FOR CHECK BITS PRECALCULATION LOOP.
     ;
0001         SONR    W,MOVE,SOI,NRY
     /       &NODLE  &NOIEN  &OEY    &NOSRE
     /       &NOJMPI
     /       &CONT
     ;
0002         IMME    H@0000
     /       &NODLE  &NOIEN  &OEY    &NOSRE
     /       &BT20   &NOJMPI
     /       &CONT
     ;
0003         SONR    W,MOVE,SOI,NRY
     /       &NODLE  &NOIEN  &OEY    &NOSRE
     /       &NOJMPI
     /       &CONT
     ;
0004         IMME    H@0010
     /       &NODLE  &NOIEN  &OEY    &NOSRE
     /       &BT20   &NOJMPI
     /       &LDCT   127
     ;
     ;
     ;       (R3) TO R4
     ;
0005         SOR     W,MOVE,SORY,R3
     /       &DLE    &NOIEN  &OEY    &NOSRE
     /       &NOJMPI
     /       &CONT
     ;
0006         SOR     W,MOVE,SODR,R4
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &NOJMPI
     /       &CONT
     ;
     ;       BEGIN CHECK BITS PRECALCULATION LOOP.
     ;       (R4) TO THE MAR.
     ;
0007 PCPREL: SOR     W,MOVE,SORY,R4
     /       &NODLE  &NOIEN  &OEY    &NOSRE
     /       &MADR   &NOJMPI
     /       &CONT
     ;
     ;
     ;       CLOCK THE LESS SIGNIFICANT BYTE OF ((MAR)) INTO THE AM9520.
     ;
             NOOP
0008 /       &NODLE  &NOIEN  &NOOEY  &NOSRE
     /       &BT2L   &NOJMPI
     /       &CONT
     ;
             NOOP
0009 /       &NODLE  &NOIEN  &NOOEY  &NOSRE
     /       &CP20   &NOJMPI
     /       &CONT
     ;
     ;
     ;       NOOP FOR TIMING PURPOSES
     ;
             NOOP
000A /       &NODLE  &NOIEN  &NOOEY  &NOSRE
     /       &NOJMPI
     /       &CONT
     ;
     ;
     ;       CLOCK THE MORE SIGNIFICANT BYTE OF ((MAR)) INTO THE AM9520.
     ;
             NOOP
000B /       &NODLE  &NOIEN  &NOOEY  &NOSRE
     /       &BT2U   &NOJMPI
     /       &CONT
     ;
     ;
     ;       INCREMENT (R4).
     ;       END CHECK BITS PRECALCULATION LOOP.
     ;
000C         SOR     W,INC,SORR,R4
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &CP20   &NOJMPI
     /       &RPCT   PCPREL
```

6

```
      ;
      ;       PLACE THE AM9520 IN WRITE CHECK BITS MODE.
      ;       INITIALIZE COUNTER FOR STORE CHECK BITS IN BUFFER LOOP.
      ;
000D          SONR    W,MOVE,SOI,NRY
      /       &NODLE  &NOIEN  &OEY    &NOSRE
      /       &NOJMPI
      /       &CONT
      ;
000E          IMME    H#0011
      /       &NODLE  &NOIEN  &OEY    &NOSRE
      /       &BT20   &NOJMPI
      /       &LDCT   2
      ;
      ;
      ;       BEGIN STORE CHECK BITS IN BUFFER LOOP.
      ;       (R4) TO THE MAR.
      ;       CLOCK OUT NEXT MODIFIED FIRE CODE BYTE TO THE
      ;       LESS-SIGNIFICANT MEMORY BUS INTERFACE REGISTER.
      ;
000F SCBIBL:  SOR     W,MOVE,SORY,R4
      /       &NODLE  &NOIEN  &OEY    &NOSRE
      /       &CP20   &MADR   &NOJMPI
      /       &CONT
      ;
              NOOP
0010  /       &NODLE  &NOIEN  &NOOEY  &NOSRE
      /       &CE2L   &NOJMPI
      /       &CONT
      ;
      ;
      ;       NOOP FOR TIMING PURPOSES
      ;
              NOOP
0011  /       &NODLE  &NOIEN  &NOOEY  &NOSRE
      /       &NOJMPI
      /       &CONT
      ;
      ;
      ;       CLOCK OUT NEXT MODIFIED FIRE CODE BYTE TO THE
      ;       MORE-SIGNIFICANT MEMORY BUS INTERFACE REGISTER.
      ;
              NOOP
0012  /       &NODLE  &NOIEN  &NOOEY  &NOSRE
      /       &CP20   &NOJMPI
      /       &CONT
      ;
      ;
      ;       NOOP FOR TIMING PURPOSES
      ;
              NOOP
0013  /       &NODLE  &NOIEN  &NOOEY  &NOSRE
      /       &NOJMPI
      /       &CONT
      ;
      ;       (BUS INTERFACE REGISTER PAIR) TO (MAR).
      ;       INCREMENT (R4).
      ;       END STORE CHECK BITS IN BUFFER LOOP.
      ;
0014          SOR     W,INC,SORR,R4
      /       &NODLE  &IEN    &NOOEY  &NOSRE
      /       &BF2L   &BF2U   &MWRT   &NOJMPI
      /       &RPCT   SCBIBL
      ;
      ;
      ;       ZERO THE UPPER BYTE OF (R5) AND THEN CLOCK THE 7TH AND LAST
      ;       BYTE OF THE MODIFIED FIRE CODE INTO ITS LOWER BYTE.
      ;
0015          SOR     W,MOVE,SOZR,R5
      /       &NODLE  &IEN    &NOOEY  &NOSRE
      /       &CP20   &NOJMPI
      /       &CONT
      ;
              NOOP
0016  /       &NODLE  &NOIEN  &NOOEY  &NOSRE
      /       &CE2L   &NOJMPI
      /       &CONT
      ;
0017          SOR     B,MOVE,SODR,R5
      /       &DLE    &IEN    &NOOEY  &NOSRE
      /       &BF2L   &BT16   &NOJMPI
      /       &CONT
      ;
      ;
      ;       (R4) TO MAR.
      ;
0018          SOR     W,MOVE,SORY,R4
      /       &NODLE  &NOIEN  &OEY    &NOSRE
      /       &MADR   &NOJMPI
      /       &CONT
      ;
      ;
      ;       (R5) TO (MAR).
      ;
0019          SOR     W,MOVE,SORY,R5
      /       &NODLE  &NOIEN  &OEY    &NOSRE
      /       &BF16   &MWRT   &NOJMPI
      /       &CONT
      ;
```

```
        ;
        ;       CONVERT THE FUNCTION CODE IN R0 TO A MICROCODE BRANCH ADDRESS.
        ;
001A CFCODE: SONR    W,MOVE,SOI,NRA
        /       &NODLE  &IEN    &NOOEY  &NOSRE
        /       &NOJMPI
        /       &CONT
        ;
001B            IMME    BRTABL
        /       &NODLE  &IEN    &NOOEY  &NOSRE
        /       &NOJMPI
        /       &CONT
        ;
001C            TOR1    W,ADD,TORAA,R0
        /       &NODLE  &IEN    &NOOEY  &NOSRE
        /       &NOJMPI
        /       &CONT
        ;
        ;
        ;       CRCF POLYNOMIAL MASK TO ACC.
        ;
001D            SONR    W,MOVE,SOI,NRA
        /       &NODLE  &IEN    &NOOEY  &NOSRE
        /       &NOJMPI
        /       &CONT
        ;
001E            IMME    CRCMSK
        /       &NODLE  &IEN    &NOOEY  &NOSRE
        /       &NOJMPI
        /       &CONT
        ;
        ;
        ;       CLEAR REGISTER USED TO ACCUMULATE CRCF.
        ;
001F            SOR     W,MOVE,SOZR,R4
        /       &NODLE  &IEN    &NOOEY  &NOSRE
        /       &NOJMPI
        /       &CONT
        ;
        ;
        ;       COPY HEAD BYTE AND TRACK BYTE 1 TO R5.
        ;       SET CRCF LOOP COUNTER.
        ;
0020            SOR     W,MOVE,SORY,R1
        /       &DLE    &IEN    &NOOEY  &NOSRE
        /       &NOJMPI
        /       &LDCT   CRCNIT
        ;
0021            SOR     W,MOVE,SODR,R5
        /       &NODLE  &IEN    &NOOEY  &NOSRE
        /       &NOJMPI
        /       &CONT
        ;
        ;       SHIFT R5 AND SET QLINK.
        ;
0022 CRCFL1: SHFTR   W,SHUPZ,SHRR,R5
        /       &NODLE  &IEN    &NOOEY  &NOSRE
        /       &NOJMPI
        /       &CONT
        ;
        ;
        ;       ACCUMULATE CRCF.
        ;
0023            CRCF    R4
        /       &NODLE  &IEN    &NOOEY  &NOSRE
        /       &NOJMPI
        /       &RPCT   CRCFL1
        ;
        ;
        ;       COPY TRACK BYTE 2 AND SECTOR BYTE TO R5.
        ;       SET CRCF LOOP COUNTER.
        ;
0024            SOR     W,MOVE,SORY,R2
        /       &DLE    &IEN    &NOOEY  &NOSRE
        /       &NOJMPI
        /       &LDCT   CRCNIT
        ;
0025            SOR     W,MOVE,SODR,R5
        /       &NODLE  &IEN    &NOOEY  &NOSRE
        /       &NOJMPI
        /       &CONT
        ;
        ;
        ;       SHIFT R5 AND SET QLINK.
        ;
0026 CRCFL2: SHFTR   W,SHUPZ,SHRR,R5
        /       &NODLE  &IEN    &NOOEY  &NOSRE
        /       &NOJMPI
        /       &CONT
        ;
        ;
        ;       ACCUMULATE CRCF.
        ;
0027            CRCF    R4
        /       &NODLE  &IEN    &NOOEY  &NOSRE
        /       &NOJMPI
        /       &RPCT   CRCFL2
```

```
        ;
        ;       INITIALIZE SECTOR PASS LOOP COUNTER.
        ;       ENTER INPUT MODE.
        ;       TURN ON READ GATE.
        ;
        ;
                NOOP
0028 /          &NODLE  &NOIEN  &NOOEY  &NOSRE
     /          &INPT   &NOJMPI &RDGA
     /          &LDCT   NSPASS
        ;
        ;
        ;       BEGIN SECTOR PASS LOOP.
        ;       TURN ON ADDRESS MARK CONTROL.
        ;       RESET BYTE SYNC ACQUISITION CIRCUITRY AND FIFO ARRAY.
        ;
        SECTL1: NOOP
0029 /          &NODLE  &NOIEN  &NOOEY  &NOSRE
     /          &ADMC   &INPT   &NOJMPI &RDGA   &RFIF
     /          &CONT
        ;
        ;
        ;       PASS WHEN ADDRESS MARK DETECTED.
        ;
                NOOP
002A /          &NODLE  &NOIEN  &NOOEY  &NOSRE
     /          &ADMC   &INPT   &NOJMPI &RDGA
     /          &IFNOT  SAMD    &CJP    $
        ;
        ;
        ;       TURN OFF ADDRESS MARK CONTROL.
        ;       PASS WHEN INPUT AVAILABLE FROM FIFO ARRAY.
        ;
                NOOP
002B /          &NODLE  &NOIEN  &NOOEY  &NOSRE
     /          &INPT   &NOJMPI &RDGA
     /          &IFNOT  RDYI    &CJP    $
        ;
        ;       INPUT RECORDED HEAD NUMBER AND MSB OF RECORDED TRACK NUMBER
        ;       TO R5 AND D-LATCH.
        ;       PASS WHEN INPUT AVAILABLE FROM FIFO ARRAY.
        ;
002C            SOR     W,MOVE,SODR,R5
     /          &DLE    &IEN    &NOOEY  &NOSRE
     /          &BF03   &BT16   &INPT   &NOJMPI &RDGA
     /          &IFNOT  RDYI    &CJP    $
        ;
        ;
        ;       COMPARE THE CONTENTS OF R1 AND R5.
        ;       IF THEY DISAGREE, EXAMINE THE NEXT SECTOR.
        ;
002D            TOR1    W,EXOR,TODRR,R1
     /          &NODLE  &NOIEN  &NOOEY  &SRE    &CT     Z
     /          &INPT   &NOJMPI &RDGA
     /          &IF     CT16    &CJP    SECTL2
        ;
        ;
        ;       INPUT LSB OF RECORDED TRACK NUMBER AND RECORDED SECTOR NUMBER
        ;       TO R5 AND D-LATCH.
        ;       PASS WHEN INPUT AVAILABLE FROM FIFO ARRAY.
        ;
                NOOP
002E /          &NODLE  &NOIEN  &NOOEY  &NOSRE
     /          &PF03   &INPT   &NOJMPI &RDGA
     /          &CONT
        ;
002F            SOR     W,MOVE,SODR,R5
     /          &DLE    &IEN    &NOOEY  &NOSRE
     /          &BF03   &BT16   &INPT   &NOJMPI &RDGA
     /          &IFNOT  RDYI    &CJP    $
```

```
      ;
      ;       COMPARE THE CONTENTS OF R2 AND R5;
      ;       IF THEY DISAGREE, EXAMINE THE NEXT SECTOR.
      ;
0030          TOR1    W,EXOR,TODRR,R2
      /       &NODLE  &NOIEN  &NOOEY  &SRE    &CT     Z
      /       &PF03   &INPT   &NOJMPI &RDGA
      /       &IF     CT16    &CJP    SECTL2
      ;
      ;
      ;       INPUT RECORDED CRCF BYTES 1 AND 0 TO R5 AND D-LATCH.
      ;
0031          SOR     W,MOVE,SODR,R5
      /       &DLE    &IEN    &NOOEY  &NOSRE
      /       &BF03   &BT16   &INPT   &NOJMPI &RDGA
      /       &CONT
      ;
      ;
      ;       COMPARE THE TWO CRCFS.
      ;       IF THEY AGREE, PROCEED TO READ OR WRITE AS SPECIFIED BY R0.
      ;       OTHERWISE, ASSUME BAD HEADER, TRUE ID UNKNOWN,
      ;       AND CONTINUE LOOP.
      ;
0032          TOR1    W,EXOR,TODRR,R4
      /       &NODLE  &NOIEN  &NOOEY  &SRE    &CT     Z
      /       &INPT   &NOJMPI &RDGA
      /       &IF     CT16    &CJP    MATCH1
      ;
      ;
      ;       TURN OFF READ GATE.
      ;       LEAVE INPUT MODE.
      ;       END SECTOR PASS LOOP.
      ;       NOTICE WE HAVE THREE MICROINSTRUCTION CLOCKS LEFT BEFORE
      ;       IT IS TIME TO BEGIN WRITING OR RE-SYNC AND BEGIN READING.
      ;
0033 SECTL2:  SOR     W,MOVE,SORY,R0
      /       &NODLE  &NOIEN  &NOOEY  &NOSRE
      /       &NOJMPI
      /       &RPCT   SECTL1
      ;
      ;
      ;       IF SECTOR SEARCH COUNT EXHAUSTED, LOAD +1 INTO R0 AND RETURN
      ;
0034          BOR2    W,LD2NR,0,R0
      /       &NODLE  &IEN    &NOOEY  &NOSRE
      /       &NOJMPI
      /       &RTN
      ;
      ;       SUCCESSFUL MATCH.
      ;
0035 MATCH1:  SOR     W,MOVE,SORY,R0
      /       &NODLE  &NOIEN  &OEY    &NOSRE
      /       &JMPI
      /       &CONT
      ;
0036 BRTABL:  SOR     W,NEG,SORA,R3
      /       &NODLE  &IEN    &NOOEY  &NOSRE
      /       &NOJMPI &RFIF
      /       &JP     RDSEC1
      ;
0037          SOR     W,NEG,SORA,R3
      /       &NODLE  &IEN    &NOOEY  &NOSRE
      /       &NOJMPI &RFIF
      /       &JP     WRSEC1
```

```
     ;
     ;       READ SECTOR
     ;
     ;       (R3) TO R4 AND MAR.
     ;       ENTER INPUT MODE AGAIN.
     ;       TURN READ GATE BACK ON.
     ;       INITIALIZE COUNTER FOR READ DATA SEGMENT LOOP.
     ;       DURING THAT LOOP, AM9520 READ HIGH SPEED IS PERFORMED ON THE
     ;       FIRST HALF OF THE SEGMENT BUFFER.  THE SECOND HALF OF THE BUFFER
     ;       IS PROCESSED BY THE AM9520 IN THE READ HIGH SPEED COMPLETION LOOP.
     ;
0038 RDSEC1: SOR     W,NEG,SOAR,R4
     /       &NODLE  &IEN    &OEY    &NOSRE
     /       &INPT   &NOJMPI &MADR   &RDGA   &RFIF
     /       &LDCT   RDITCT
     ;
     ;
     ;       (R3) - 1 TO R5.
     ;       PASS WHEN INPUT AVAILABLE FROM FIFO ARRAY.
     ;
0039         SOR     W,COMP,SOAR,R5
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &INPT   &NOJMPI &RDGA
     /       &IFNOT  RDYI    &CJP    $
     ;
     ;       RESET THE AM9520 AND THEN PLACE IT IN READ HIGH SPEED MODE.
     ;
003A         SONR    W,MOVE,SOI,NRY
     /       &NODLE  &NOIEN  &OEY    &NOSRE
     /       &INPT   &NOJMPI &RDGA
     /       &CONT
     ;
003B         IMME    H#0003
     /       &NODLE  &NOIEN  &OEY    &NOSRE
     /       &INPT   &NOJMPI &RDGA
     /       &CONT
     ;
003C         SONR    W,MOVE,SOI,NRY
     /       &NODLE  &NOIEN  &OEY    &NOSRE
     /       &INPT   &NOJMPI &RDGA
     /       &CONT
     ;
003D         IMME    H#0013
     /       &NODLE  &NOIEN  &OEY    &NOSRE
     /       &BT20   &INPT   &NOJMPI &RDGA
     /       &CONT
     ;
             NOOP
003E /       &NODLE  &NOIEN  &NOOEY  &NOSRE
     /       &INPT   &NOJMPI &PF03   &RDGA
     /       &CONT
```

```
        ;
        ;       BEGIN READ DATA SEGMENT LOOP.
        ;       TRANSFER NEXT WORD FROM FIFO ARRAY TO (MAR).
        ;       PASS WHEN FIFO INPUT AGAIN BECOMES AVAILABLE.
        ;
        RDSEC2: NOOP
003F    /       &NODLE  &NOIEN  &NOOEY  &NOSRE
        /       &BF03   &INPT   &NOJMPI &MWRT   &RDGA
        /       &IFNOT  RDYI    &CJP    $
        ;
        ;
        ;       INCREMENT (R5) AND TRANSFER THIS TO THE MAR.
        ;
0040            SOR     W,INC,SORR,R5
        /       &NODLE  &IEN    &OEY    &NOSRE
        /       &INPT   &NOJMPI &MADR   &RDGA
        /       &CONT
        ;
        ;
        ;       CLOCK LESS SIGNIFICANT BYTE OF ((MAR)) INTO THE AM9520.
        ;       INCREMENT (R4) AND TRANSFER THIS TO THE MAR.
        ;
0041            SOR     W,INC,SORR,R4
        /       &NODLE  &IEN    &OEY    &NOSRE
        /       &BT2L   &CP20   &INPT   &NOJMPI &MADR   &MREA   &PF03   &RDGA
        /       &CONT
        ;
        ;
        ;       TRANSFER NEXT WORD FROM FIFO ARRAY TO (MAR).
        ;       PASS WHEN FIFO INPUT AGAIN BECOMES AVAILABLE.
        ;
                NOOP
0042    /       &NODLE  &NOIEN  &NOOEY  &NOSRE
        /       &BF03   &INPT   &NOJMPI &MWRT   &RDGA
        /       &IFNOT  RDYI    &CJP    $
        ;
        ;       TRANSFER (R5) TO THE MAR AGAIN.
        ;
0043            SOR     W,MOVE,SORR,R5
        /       &NODLE  &IEN    &OEY    &NOSRE
        /       &INPT   &NOJMPI &MADR   &RDGA
        /       &CONT
        ;
        ;
        ;       THIS TIME, CLOCK THE MORE SIGNIFICANT BYTE OF ((MAR))
        ;       INTO THE AM9520.
        ;       END READ DATA SEGMENT LOOP.
        ;
0044            SOR     W,INC,SORR,R4
        /       &NODLE  &IEN    &OEY    &NOSRE
        /       &BT2U   &CP20   &INPT   &NOJMPI &MADR   &MREA   &PF03   &RDGA
        /       &RPCT   RDSEC2
        ;
        ;
        ;       INITIALIZE COUNTER FOR READ HIGH SPEED COMPLETION LOOP.
        ;
                NOOP
0045    /       &NODLE  &NOIEN  &NOOEY  &NOSRE
        /       &NOJMPI
        /       &LDCT   RDITCT
```

```
      ;
      ;       BEGIN READ HIGH SPEED COMPLETION LOOP.
      ;       INCREMENT (R5) AND TRANSFER THIS TO THE MAR.
      ;
0046 RDSEC3: SOR     W,INC,SORR,R5
      /       &NODLE  &IEN     &OEY    &NOSRE
      /       &NOJMPI &MADR
      /       &CONT
      ;
      ;
      ;       NOOP FOR TIMING PURPOSES
      ;
              NOOP
0047 /        &NODLE  &NOIEN  &NOOEY  &NOSRE
      /       &NOJMPI
      /       &CONT
      ;
      ;
      ;       CLOCK LESS SIGNIFICANT BYTE OF ((MAR)) INTO THE AM9520.
      ;
              NOOP
0048 /        &NODLE  &NOIEN  &NOOEY  &NOSRE
      /       &BT2L   &CP20   &NOJMPI &MREA
      /       &CONT
      ;
      ;
      ;       NOOP FOR TIMING PURPOSES
      ;
              NOOP
0049 /        &NODLE  &NOIEN  &NOOEY  &NOSRE
      /       &NOJMPI
      /       &CONT
      ;
      ;
      ;       NOOP FOR TIMING PURPOSES
      ;
              NOOP
004A /        &NODLE  &NOIEN  &NOOEY  &NOSRE
      /       &NOJMPI
      /       &CONT
      ;
      ;       CLOCK MORE SIGNIFICANT BYTE OF ((MAR)) INTO THE AM9520.
      ;       END READ HIGH SPEED COMPLETION LOOP.
      ;
              NOOP
004B /        &NODLE  &NOIEN  &NOOEY  &NOSRE
      /       &BT2U   &CP20   &NOJMPI &MREA
      /       &RPCT   RDSEC3
      ;
      ;
      ;       WAS AN ERROR DETECTED BY THE AM9520?
      ;
              NOOP
004C /        &NODLE  &NOIEN  &NOOEY  &NOSRE
      /       &NOJMPI
      /       &IF     ER20    &CJP    RDSEC4
      ;
      ;
      ;       NO; LOAD 0 INTO R0 AND RETURN.
      ;
004D          SOR     W,MOVE,SOZR,R0
      /       &NODLE  &IEN    &NOOEY  &NOSRE
      /       &NOJMPI
      /       &RTN
      ;
      ;
      ;       YES; IF THE ERROR IS A CORRECTABLE ONE, LOCATE AND CORRECT IT.
      ;       THE ERROR IS LOCATED USING THE CORRECT HIGH SPEED EQUATION:
      ;
      ;               L=NK - (M1A1 + M2A2 + M3A3 + M4A4)
      ;
      ;       WHERE  K,A1,A2,A3,A4 ARE CONSTANTS
      ;       AND  M1,M2,M3,M4 MUST BE CALCULATED.
      ;
      ;       THE ERROR IS CORRECTED BY PERFORMING AN EXOR
      ;       FUNCTION ON THE BURST ERROR IN MEMORY WITH AN
      ;       ERROR PATTERN(EP) PROVIDED BY THE BEP(9520).
      ;
      ;       INITIALIZE CORRECT HIGH SPEED,SET P0=1,& REP=1
```

```
004E RDSEC4: SONR    W,MOVE,SOI,NRY
     /       &NODLE  &NOIEN  &OEY    &NOSRE
     /       &NOJMPI
     /       &CONT
     ;
004F         IMME    H#001F
     /       &NODLE  &NOIEN  &OEY    &NOSRE
     /       &NOJMPI &BT20   &BF16
     /       &CONT
     ;
     ;
     ;       CLEAR R8(M1).
     ;
0050         SOR     W,MOVE,SOZR,R8
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &NOJMPI
     /       &CONT
     ;
     ;
     ;       PERIOD FACTOR 1(PF1) TO ACC.
     ;
0051         SONR    W,MOVE,SOI,NRA
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &NOJMPI
     /       &CONT
     ;
0052         IMME    PF1
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &NOJMPI
     /       &CONT
     ;
     ;       TEST FOR ERROR PATTERN PRESENT.
     ;
     M1:     NOOP
0053 /       &NODLE  &NOIEN  &NOOEY  &NOSRE
     /       &NOJMPI
     /       &IF     EP20    &CJP    M234I
     ;
     ;
     ;       EP NOT PRESENT,
     ;       DECREMENT ACC.
     ;       TEST FOR ALIGNMENT EXCEPTION(AE).
     ;
0054         BONR    W,0,S2NA
     /       &NODLE  &IEN    &NOOEY  &SRE
     /       &NOJMPI &CP20
     /       &IF     AE20    &CJP    AE
     ;
     ;
     ;       AE NOT PRESENT,
     ;       ADD 8 TO R8.
     ;
0055         BOR2    W,3,A2NR,R8
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &NOJMPI
     /       &JP     LINK
     ;
     ;
     ;       AE PRESENT;
     ;       INC R8.
     ;
0056 AE:     BOR2    W,0,A2NR,R8
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &NOJMPI
     /       &CONT
```

```
     ;
     ;       TEST FOR PERIOD FACTOR EXCEEDED (UNCORRECTABLE ERROR).
     ;
     LINK:   NOOP
0057 /       &NODLE  &NOIEN  &NOOEY  &NOSRE  &CT     N
     /       &NOJMPI
     /       &IFNOT  CT16    &CJP    M1
     ;
     ;
     ;       PERIOD FACTOR EXCEEDED (UNCORRECTABLE ERROR);
     ;       SET R0 = 2.
     ;       RETURN.
     ;
0058 ERR:    BOR2    W,1,LD2NR,R0
     /       &NODLE  &IEN    &OEY    &NOSRE
     /       &NOJMPI &BT20   &BF16
     /       &RTN
     ;
     ;
     ;       EP PRESENT, CALCULATE M2,M3,M4.
     ;
     ;       PERIOD FACTOR 2(PF2) TO R9(M2).
     ;       PERIOD FACTOR 3(PF3) TO R10(M3).
     ;       PERIOD FACTOR 4(PF4) TO R11(M4).
     ;
0059 M234I:  SOR     W,MOVE,SOI,R9
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &NOJMPI
     /       &CONT
     ;
005A         IMME    PF2
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &NOJMPI
     /       &CONT
005B         SOR     W,MOVE,SOI,R10
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &NOJMPI
     /       &CONT
     ;
005C         IMME    PF3
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &NOJMPI
     /       &CONT
     ;
005D         SOR     W,MOVE,SOI,R11
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &NOJMPI
     /       &CONT
     ;
005E         IMME    PF4
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &NOJMPI
     /       &CONT
     ;
     ;
     ;       JUMP TABLE ADDRESS(TAB1) TO R12.
     ;
005F         SOR     W,MOVE,SOI,R12
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &NOJMPI
     /       &CONT
     ;
0060         IMME    TAB1
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &NOJMPI
     /       &CONT
     ;
     ;
     ;       JUMP INDIRECT TO TAB1 VIA PM2-4.
     ;
0061         ROTM    W,15,MDRI,R12
     /       &DLE    &IEN    &NOOEY  &NOSRE
     /       &NOJMPI &PFPM   &BF2U   &BT16
     /       &CONT
     ;
0062         IMME    H#0007
     /       &NODLE  &IEN    &OEY    &NOSRE
     /       &JMPI   &PFPM   &BF2U   &BT16
     /       &JP     $
```

```
        ;
        ;       R9 = PF2 - R9.
        ;
0063 MFIX:  TOR1    W,TORIR,SUBR,R9
        /       &NODLE  &IEN    &NOOEY  &NOSRE
        /       &NOJMPI
        /       &CONT
        ;
0064            IMME    PF2
        /       &NODLE  &IEN    &NOOEY  &NOSRE
        /       &NOJMPI
        /       &CONT
        ;
        ;
        ;       R10 = PF3 - R10.
        ;
0065            TOR1    W,TORIR,SUBR,R10
        /       &NODLE  &IEN    &NOOEY  &NOSRE
        /       &NOJMPI
        /       &CONT
        ;
0066            IMME    PF3
        /       &NODLE  &IEN    &NOOEY  &NOSRE
        /       &NOJMPI
        /       &CONT
        ;
        ;
        ;       R11 = PF4 - R11.
        ;
0067            TOR1    W,TORIR,SUBR,R11
        /       &NODLE  &IEN    &NOOEY  &NOSRE
        /       &NOJMPI
        /       &CONT
        ;
0068            IMME    PF4
        /       &NODLE  &IEN    &NOOEY  &NOSRE
        /       &NOJMPI
        /       &CONT
        ;
        ;       0 TO R7 (LOCATION ACC MSW,LAC).
        ;
0069 M1A1:  SOR     W,MOVE,SOZR,R7
        /       &NODLE  &IEN    &NOOEY  &NOSRE
        /       &NOJMPI
        /       &CONT
        ;
        ;
        ;       A1 TO R12(LSW),R13(MSW).
        ;
006A            SOR     W,MOVE,SOI,R12
        /       &NODLE  &IEN    &NOOEY  &NOSRE
        /       &NOJMPI
        /       &CONT
        ;
006B            IMME    A1LSW
        /       &NODLE  &IEN    &NOOEY  &NOSRE
        /       &NOJMPI
        /       &CONT
        ;
006C            SOR     W,MOVE,SOI,R13
        /       &NODLE  &IEN    &NOOEY  &NOSRE
        /       &NOJMPI
        /       &CONT
        ;
006D            IMME    A1MSW
        /       &NODLE  &IEN    &NOOEY  &NOSRE
        /       &NOJMPI
        /       &LDCT   4
        ;
        ;
        ;       R8 TO D.
        ;       LAC = M1A1, MULTIPLY M1A1.
        ;
006E            SOR     W,MOVE,SORY,R8
        /       &DLE    &NOIEN  &OEY    &NOSRE
        /       &NOJMPI
        /       &JS     MUL
```

```
     ;
     ;       A2 TO R12,R13.
     ;
006F M2A2:   IMME    A2LSW
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &NOJMPI
     /       &CONT
     ;
0070         BOR2    W,3,LD2NR,R13
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &NOJMPI
     /       &LDCT   3
     ;
     ;
     ;       R9 TO D.
     ;       LAC = LAC + M2A2.
     ;
0071         SOR     W,MOVE,SORY,R9
     /       &DLE    &NOIEN  &OEY    &NOSRE
     /       &NOJMPI
     /       &JS     MUL
     ;
     ;
     ;       A3'(A3 - 4K) TO R12,R13.
     ;
0072 M3A3:   IMME    A3LSW
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &NOJMPI
     /       &CONT
     ;
0073         BOR2    W,1,LD2NR,R13
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &NOJMPI
     /       &LDCT   6
     ;
     ;
     ;       R10 TO D.
     ;       LAC = LAC + M3A3.
     ;
0074         SOR     W,MOVE,SORY,R10
     /       &DLE    &NOIEN  &OEY    &NOSRE
     /       &NOJMPI
     /       &JS     MUL
     ;
     ;       A4'(A4 - 4K) TO R12,R13.
     ;
0075 M4A4:   IMME    A4LSW
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &NOJMPI
     /       &CONT
     ;
0076         BOR2    W,3,LD2NR,R13
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &NOJMPI
     /       &LDCT   4
     ;
     ;
     ;       R11 TO D.
     ;       LAC = LAC + M4A4.
     ;
0077         SOR     W,MOVE,SORY,R11
     /       &DLE    &NOIEN  &OEY    &NOSRE
     /       &NOJMPI
     /       &JS     MUL
     ;
     ;
     ;       PRESHIFTED DIVISOR(K) TO R12,R13,D.
     ;       LAC = REM(M1A1 + M2A2 + M3A3 + M4A4) / K.
     ;       LAC = -L + K.
     ;
0078         IMME    KL128
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &NOJMPI
     /       &CONT
     ;
0079         SOR     W,MOVE,SOI,R13
     /       &DLE    &IEN    &OEY    &NOSRE
     /       &NOJMPI
     /       &LDCT   6
     ;
007A         IMME    KM128
     /       &DLE    &IEN    &OEY    &NOSRE
     /       &NOJMPI
     /       &JS     DIV
```

```
      ;
      ;       L = LAC = K - LAC.
      ;
007B SUBK:    IMME    KLSW
      /       &NODLE  &IEN    &NOOEY  &NOSRE
      /       &NOJMPI
      /       &CONT
      ;
007C          TOR1    W,TORIR,SUBRC,R7
      /       &NODLE  &IEN    &NOOEY  &NOSRE
      /       &NOJMPI
      /       &CONT
      ;
007D          IMME    KMSW
      /       &NODLE  &IEN    &NOOEY  &NOSRE
      /       &NOJMPI
      /       &CONT
      ;
      ;
      ;       0 TO R8.
      ;
007E XORMEM:  SOR     W,MOVE,SOZR,R8
      /       &NODLE  &IEN    &NOOEY  &NOSRE
      /       &NOJMPI
      /       &CONT
      ;
      ;
      ;       0 TO R9.
      ;
007F          SOR     W,MOVE,SOZR,R9
      /       &NODLE  &IEN    &NOOEY  &NOSRE
      /       &NOJMPI
      /       &CONT
      ;
      ;
      ;       0 TO ACC.
      ;
0080          SOR     W,MOVE,SORA,R9
      /       &NODLE  &IEN    &NOOEY  &NOSRE
      /       &NOJMPI
      /       &CONT
      ;
      ;       ROTATE R6 DOWN BY FOUR TO OBTAIN WORD ADDRESS
      ;       AND STORE IN ACC.
      ;
0081          ROTM    W,12,MRAI,R6
      /       &NODLE  &IEN    &NOOEY  &NOSRE
      /       &NOJMPI
      /       &CONT
      ;
0082          IMME    H#0FFF
      /       &NODLE  &IEN    &NOOEY  &NOSRE
      /       &NOJMPI
      /       &CONT
      ;
      ;
      ;       MASK UPPER 12 BITS OF R6 TO OBTAIN FIRST BIT OF
      ;       BURST ERROR AND STORE IN R6.
      ;
0083          TOR1    W,TORIR,AND,R6
      /       &NODLE  &IEN    &NOOEY  &NOSRE
      /       &NOJMPI
      /       &CONT
      ;
0084          IMME    H#000F
      /       &NODLE  &IEN    &NOOEY  &NOSRE
      /       &NOJMPI
      /       &CONT
      ;
      ;
      ;       JUMP INDIRECT TO TAB2 VIA R6.
      ;
0085          TOR1    W,TORIR,ADD,R6
      /       &NODLE  &IEN    &NOOEY  &NOSRE
      /       &NOJMPI
      /       &CONT
      ;
0086          IMME    TAB2
      /       &NODLE  &IEN    &OEY    &NOSRE
      /       &JMPI
      /       &CONT
```

```
      ;
      ;       MADR = ACC = R4 - ACC.
      ;
0087  XOR:    TOR1    W,TORAA,SUBS,R4
      /       &NODLE  &IEN    &NOOEY  &NOSRE
      /       &NOJMPI
      /       &CONT
      ;
0088          BONR    W,0,S2NA
      /       &NODLE  &IEN    &OEY    &NOSRE
      /       &MADR   &NOJMPI
      /       &CONT
      ;
      ;
      ;       R8 = R8 XOR MEM.
      ;
0089          TOR1    W,TODRR,EXOR,R8
      /       &DLE    &IEN    &NOOEY  &NOSRE
      /       &NOJMPI &BT16
      /       &CONT
      ;
      ;
      ;       R8 TO MEMORY.
      ;
008A          SOR     W,MOVE,SORY,R8
      /       &NODLE  &NOIEN  &OEY    &NOSRE
      /       &NOJMPI &MWRT   &BF16
      /       &CONT
      ;
      ;
      ;       MADR = ACC + 1.
      ;
008B          SONR    W,INC,SOA,NRY
      /       &NODLE  &NOIEN  &OEY    &NOSRE
      /       &NOJMPI &MADR
      /       &CONT
      ;
      ;
      ;       R9 = R9 XOR MEM.
      ;
008C          TOR1    W,TODRR,EXOR,R9
      /       &DLE    &IEN    &NOOEY  &NOSRE
      /       &NOJMPI &BT16
      /       &CONT
      ;
      ;       R9 TO MEMORY.
      ;
008D          SOR     W,MOVE,SORY,R9
      /       &NODLE  &NOIEN  &OEY    &NOSRE
      /       &NOJMPI &MWRT   &BF16
      /       &CONT
      ;
      ;
      ;       0 TO R0 (ERROR CORRECTED FLAG).
      ;       RETURN.
      ;
008E          SOR     W,MOVE,SOZR,R0
      /       &NODLE  &IEN    &OEY    &NOSRE
      /       &NOJMPI &BT20   &BF16
      /       &RTN
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      ;
      ;       TABLE 1 IS USED TO CALCULATE
      ;       M2,M3,M4 AND DETECT UNCORRECTABLE ERRORS.
      ;       EACH MICROINSTRUCTION PATH DECREMENTS THE
      ;       APPROPRIATE REGISTER(S) AND CHECKS FOR VALUES
      ;       EXCEEDING THE 56-BIT POLYNOMIAL PERIOD
      ;       FACTOR LIMITS.
      ;
              ALIGN   8
0090  ;
0090  TAB1:   BOR2    W,0,S2NR,R9
      /       &NODLE  &IEN    &NOOEY  &SRE
      /       &NOJMPI &CP20   &PFPM
      /       &JP     PM234
      ;
0091          BOR2    W,0,S2NR,R11
      /       &NODLE  &IEN    &NOOEY  &SRE
      /       &NOJMPI &CP20   &PFPM
      /       &JP     TM34
      ;
0092          BOR2    W,0,S2NR,R9
      /       &NODLE  &IEN    &NOOEY  &SRE
      /       &NOJMPI &CP20   &PFPM
      /       &JP     TM24
      ;
0093          BOR2    W,0,S2NR,R11
      /       &NODLE  &IEN    &NOOEY  &SRE
      /       &NOJMPI &CP20   &PFPM
      /       &JP     TM1
      ;
0094          BOR2    W,0,S2NR,R10
      /       &NODLE  &IEN    &NOOEY  &SRE
      /       &NOJMPI &CP20   &PFPM
      /       &JP     TM23
      ;
0095          BOR2    W,0,S2NR,R10
      /       &NODLE  &IEN    &NOOEY  &SRE
      /       &NOJMPI &CP20   &PFPM
      /       &JP     TM1
      ;
0096          BOR2    W,0,S2NR,R9
      /       &NODLE  &IEN    &NOOEY  &SRE
      /       &NOJMPI &CP20   &PFPM
      /       &JP     TM1
      ;
0097          SOR     W,MOVE,SOZR,R6
      /       &NODLE  &IEN    &NOOEY  &SRE
      /       &NOJMPI &PFPM
      /       &JP     MFIX
      TM34:   NOOP
0098  /       &NODLE  &NOIEN  &NOOEY  &NOSRE
      /       &NOJMPI &CP20   &PFPM
      /       &JP     PM34
      ;
      TM24:   NOOP
0099  /       &NODLE  &NOIEN  &NOOEY  &NOSRE
      /       &NOJMPI &CP20   &PFPM
      /       &JP     PM24
      ;
      TM23:   NOOP
009A  /       &NODLE  &NOIEN  &NOOEY  &NOSRE
      /       &NOJMPI &CP20   &PFPM
      /       &JP     PM23
      ;
      TM1:    NOOP
009B  /       &NODLE  &NOIEN  &NOOEY  &NOSRE
      /       &NOJMPI &CP20   &PFPM
      /       &CONT
      ;
              NOOP
009C  /       &NODLE  &NOIEN  &NOOEY  &NOSRE
      /       &NOJMPI &CP20   &PFPM
      /       &JP     PM1
      ;
009D  PM234:  BOR2    W,0,S2NR,R11
      /       &NODLE  &IEN    &NOOEY  &SRE    &CT     N
      /       &NOJMPI &CP20   &PFPM
      /       &IF     CT16    &CJP    ERR
      ;
009E  PM34:   BOR2    W,0,S2NR,R10
      /       &NODLE  &IEN    &NOOEY  &SRE    &CT     N
      /       &NOJMPI &CP20   &PFPM
      /       &IF     CT16    &CJP    ERR
      ;
009F  PM1:    ROTM    W,15,MDRI,R12
      /       &DLE    &IEN    &NOOEY  &NOSRE  &CT     N
      /       &NOJMPI &PFPM   &BT16   &BF2U
      /       &IF     CT16    &CJP    LINK
      ;
00A0          IMME    H#0007
      /       &NODLE  &IEN    &OEY    &NOSRE
      /       &JMPI   &PFPM   &BT16   &BF2U
      /       &JP     $
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00A1 PM24:   BOR2    W,0,S2NR,R11
     /       &NODLE  &IEN     &NOOEY  &SRE     &CT     N
     /       &NOJMPI &CP20    &PFPM
     /       &IFNOT  CT16     &CJP    PM1
     ;
             NOOP
00A2 /       &NODLE  &NOIEN   &NOOEY  &NOSRE
     /       &NOJMPI
     /       &JP     ERR
     ;
00A3 PM23:   BOR2    W,0,S2NR,R9
     /       &NODLE  &IEN     &NOOEY  &SRE     &CT     N
     /       &NOJMPI &CP20    &PFPM
     /       &IFNOT  CT16     &CJP    PM1
     ;
             NOOP
00A4 /       &NODLE  &NOIEN   &NOOEY  &NOSRE
     /       &NOJMPI
     /       &JP     ERR
     ;
     ;
     ;       TABLE 2 IS USED FOR ROTATING MEMORY WORD(S)
     ;       VIA ROTATE AND MERGE INSTRUCTION(S) SO THAT
     ;       BURST ERRORS CAN BE ALIGNED WITH THE ERROR
     ;       PATTERN PROVIDED BY THE BEP(9520).
     ;
00A5 TAB2:   ROTM    W,9,MDRI,R8
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     REP1
     ;
00A6         ROTM    W,10,MDRI,R8
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     REP2
     ;
00A7         ROTM    W,11,MDRI,R8
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     REP3
     ;
00A8         ROTM    W,12,MDRI,R8
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     REP4

00A9         ROTM    W,13,MDRI,R8
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     REP5
     ;
00AA         ROTM    W,14,MDRI,R8
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     REP6
     ;
00AB         ROTM    W,15,MDRI,R8
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     REP7
     ;
00AC         ROTM    W,0,MDRI,R8
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     REP8
     ;
00AD         ROTM    W,1,MDRI,R8
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     REP9
     ;
00AE         ROTM    W,2,MDRI,R8
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     REP10
     ;
00AF         ROTM    W,3,MDRI,R8
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     REP11
     ;
00B0         ROTM    W,4,MDRI,R8
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     REP12
     ;
00B1         ROTM    W,5,MDRI,R8
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     REP13
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```
00B2            ROTM    W,6,MDRI,R8
      /         &DLE    &IEN     &NOOEY  &NOSRE
      /         &NOJMPI &BT16    &BF2U   &BF2L
      /         &JP     REP14
      ;
00B3            ROTM    W,7,MDRI,R8
      /         &DLE    &IEN     &NOOEY  &NOSRE
      /         &NOJMPI &BT16    &BF2U   &BF2L
      /         &JP     REP15
      ;
00B4            ROTM    W,8,MDRI,R8
      /         &DLE    &IEN     &NOOEY  &NOSRE
      /         &NOJMPI &BT16    &BF2U   &BF2L
      /         &JP     REP16
00B5 REP1:      IMME    H#0001
      /         &DLE    &IEN     &NOOEY  &NOSRE
      /         &NOJMPI &BT16    &BF2U   &BF2L
      /         &JP     RM1
      ;
00B6 REP2:      IMME    H#0003
      /         &DLE    &IEN     &NOOEY  &NOSRE
      /         &NOJMPI &BT16    &BF2U   &BF2L
      /         &JP     RM2
      ;
00B7 REP3:      IMME    H#0007
      /         &DLE    &IEN     &NOOEY  &NOSRE
      /         &NOJMPI &BT16    &BF2U   &BF2L
      /         &JP     RM3
      ;
00B8 REP4:      IMME    H#000F
      /         &DLE    &IEN     &NOOEY  &NOSRE
      /         &NOJMPI &BT16    &BF2U   &BF2L
      /         &JP     RM4
      ;
00B9 REP5:      IMME    H#001F
      /         &DLE    &IEN     &NOOEY  &NOSRE
      /         &NOJMPI &BT16    &BF2U   &BF2L
      /         &JP     RM5
      ;
00BA REP6:      IMME    H#003F
      /         &DLE    &IEN     &NOOEY  &NOSRE
      /         &NOJMPI &BT16    &BF2U   &BF2L
      /         &JP     RM6

00BB REP7:      IMME    H#007F
      /         &DLE    &IEN     &NOOEY  &NOSRE
      /         &NOJMPI &BT16    &BF2U   &BF2L
      /         &JP     RM7
      ;
00BC REP8:      IMME    H#00FF
      /         &DLE    &IEN     &NOOEY  &NOSRE
      /         &NOJMPI &BT16    &BF2U   &BF2L
      /         &JP     RM8
      ;
00BD REP9:      IMME    H#01FF
      /         &DLE    &IEN     &NOOEY  &NOSRE
      /         &NOJMPI &BT16    &BF2U   &BF2L
      /         &JP     RM9
      ;
00BE REP10:     IMME    H#03FF
      /         &DLE    &IEN     &NOOEY  &NOSRE
      /         &NOJMPI &BT16    &BF2U   &BF2L
      /         &JP     RM10
      ;
00BF REP11:     IMME    H#07FF
      /         &DLE    &IEN     &NOOEY  &NOSRE
      /         &NOJMPI &BT16    &BF2U   &BF2L
      /         &JP     RM11
      ;
00C0 REP12:     IMME    H#0FFF
      /         &DLE    &IEN     &NOOEY  &NOSRE
      /         &NOJMPI &BT16    &BF2U   &BF2L
      /         &JP     XOR
      ;
00C1 REP13:     IMME    H#1FFE
      /         &DLE    &IEN     &NOOEY  &NOSRE
      /         &NOJMPI &BT16    &BF2U   &BF2L
      /         &JP     XOR
      ;
00C2 REP14:     IMME    H#3FFC
      /         &DLE    &IEN     &NOOEY  &NOSRE
      /         &NOJMPI &BT16    &BF2U   &BF2L
      /         &JP     XOR
      ;
00C3 REP15:     IMME    H#7FF8
      /         &DLE    &IEN     &NOOEY  &NOSRE
      /         &NOJMPI &BT16    &BF2U   &BF2L
      /         &JP     XOR
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```
00C4 REP16:  IMME    H#FFF0
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     XOR
     ;
00C5 RM1:    ROTM    W,9,MDRI,R9
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     REP17
     ;
00C6 RM2:    ROTM    W,10,MDRI,R9
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     REP18
     ;
00C7 RM3:    ROTM    W,11,MDRI,R9
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     REP19
     ;
00C8 RM4:    ROTM    W,12,MDRI,R9
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     REP20
     ;
00C9 RM5:    ROTM    W,13,MDRI,R9
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     REP21
     ;
00CA RM6:    ROTM    W,14,MDRI,R9
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     REP22
     ;
00CB RM7:    ROTM    W,15,MDRI,R9
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     REP23
     ;
00CC RM8:    ROTM    W,0,MDRI,R9
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     REP24

00CD RM9:    ROTM    W,1,MDRI,R9
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     REP25
     ;
00CE RM10:   ROTM    W,2,MDRI,R9
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     REP26
     ;
00CF RM11:   ROTM    W,3,MDRI,R9
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     REP27
     ;
00D0 REP17:  IMME    H#FFE0
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     XOR
     ;
00D1 REP18:  IMME    H#FFC0
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     XOR
     ;
00D2 REP19:  IMME    H#FF80
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     XOR
     ;
00D3 REP20:  IMME    H#FF00
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     XOR
     ;
00D4 REP21:  IMME    H#FE00
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     XOR
     ;
00D5 REP22:  IMME    H#FC00
     /       &DLE    &IEN     &NOOEY  &NOSRE
     /       &NOJMPI &BT16    &BF2U   &BF2L
     /       &JP     XOR
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```
00D6 REP23:  IMME     H#F800
     /       &DLE     &IEN     &NOOEY   &NOSRE
     /       &NOJMPI  &BT16    &BF2U    &BF2L
     /       &JP      XOR
     ;
00D7 REP24:  IMME     H#F000
     /       &DLE     &IEN     &NOOEY   &NOSRE
     /       &NOJMPI  &BT16    &BF2U    &BF2L
     /       &JP      XOR
     ;
00D8 REP25:  IMME     H#E000
     /       &DLE     &IEN     &NOOEY   &NOSRE
     /       &NOJMPI  &BT16    &BF2U    &BF2L
     /       &JP      XOR
     ;
00D9 REP26:  IMME     H#C000
     /       &DLE     &IEN     &NOOEY   &NOSRE
     /       &NOJMPI  &BT16    &BF2U    &BF2L
     /       &JP      XOR
     ;
00DA REP27:  IMME     H#8000
     /       &DLE     &IEN     &NOOEY   &NOSRE
     /       &NOJMPI  &BT16    &BF2U    &BF2L
     /       &JP      XOR
     ;
     ;       SUBROUTINE MULTIPLY
     ;
     ;       THIS SUBROUTINE MULTIPLIES A DOUBLE PRECISION
     ;       WORD BY A SINGLE PRECISION WORD AND ASSUMES
     ;       A DOUBLE PRECISION ANSWER.  THE MULTIPLIER
     ;       IS IN D, THE MULTIPLICAND IS IN R12,R13, AND
     ;       THE ANSWER APPEARS IN R6,R7(LAC). NOTE, UPON
     ;       RETURNING TO THE MAIN PROGRAM THE SUBROUTINE
     ;       INITIATES AN IMMEDIATE MOVE TO R12.
     ;
00DB MUL:    SHFTR    W,SHDR,SHDNZ,R8
     /       &NODLE   &IEN     &NOOEY   &SRE
     /       &NOJMPI
     /       &CONT
     ;
00DC         SOR      W,MOVE,SORY,R13
     /       &DLE     &NOIEN   &OEY     &NOSRE
     /       &NOJMPI
     /       &CONT
     ;
00DD CYC:    SOR      W,MOVE,SORA,R12
     /       &NODLE   &IEN     &NOOEY   &NOSRE   &CT      L
     /       &NOJMPI
     /       &IFNOT   CT16     &CJP     NOTQ
     ;
00DE         TOR1     W,TORAR,ADD,R6
     /       &NODLE   &IEN     &NOOEY   &SRE
     /       &NOJMPI
     /       &CONT
     ;
00DF         TOR1     W,TODRR,ADDC,R7
     /       &NODLE   &IEN     &NOOEY   &NOSRE
     /       &NOJMPI
     /       &CONT
```

```
00E0 NOTQ:   SHFTR   W,SHRR,SHUPZ,R12
     /       &NODLE  &IEN    &NOOEY  &SRE
     /       &NOJMPI
     /       &CONT
     ;
00E1         SHFTR   W,SHRR,SHUPL,R13
     /       &DLE    &IEN    &OEY    &NOSRE
     /       &NOJMPI
     /       &CONT
     ;
00E2         SHFTR   W,SHRR,SHDNZ,R8
     /       &NODLE  &IEN    &NOOEY  &SRE
     /       &NOJMPI
     /       &RPCT   CYC
     ;
00E3         SOR     W,MOVE,SOI,R12
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &NOJMPI
     /       &RTN
     ;
     ;       SUBROUTINE DIVIDE
     ;       THIS SUBROUTINE DIVIDES A DOUBLE PRECISION
     ;       NUMBER BY A DOUBLE PRECISION NUMBER LEAVING
     ;       ONLY A REMAINDER.  THE DIVISOR IS IN R12,R13,D
     ;       AND THE DIVIDEND/REMAINDER APPEARS IN R6,R7.
     ;       NOTE, UPON RETURN AN IMMEDIATE SUBTRACT IS
     ;       INITIATED.
     ;
00E4 DIV:    SOR     W,MOVE,SORA,R12
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &NOJMPI
     /       &CONT
     ;
00E5 CYC1:   TOR1    W,TORAR,SUBS,R6
     /       &NODLE  &IEN    &NOOEY  &SRE
     /       &NOJMPI
     /       &CONT
     ;
00E6         TOR1    W,TODRR,SUBSC,R7
     /       &NODLE  &IEN    &NOOEY  &SRE
     /       &NOJMPI
     /       &CONT
     ;
             NOOP
00E7 /       &NODLE  &IEN    &NOOEY  &NOSRE  &CT     N
     /       &NOJMPI
     /       &IFNOT  CT16    &CJP    POS
     ;
00E8         TOR1    W,TORAR,ADD,R6
     /       &NODLE  &IEN    &NOOEY  &SRE
     /       &NOJMPI
     /       &CONT
     ;
00E9         TOR1    W,TODRR,ADDC,R7
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &NOJMPI
     /       &CONT
```

```
00EA POS:    SHFTR   W,SHRR,SHDNZ,R13
     /       &DLE    &IEN    &OEY    &SRE
     /       &NOJMPI
     /       &CONT
     ;
00EB         SHFTR   W,SHA,SHDNL,R12
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &NOJMPI
     /       &RPCT   CYC1
     ;
00EC         TOR1    W,TORIR,SUBR,R6
     /       &NODLE  &IEN    &NOOEY  &SRE
     /       &NOJMPI
     /       &RTN

     ;
     ;       WRITE SECTOR
     ;
     ;       (R3) TO R4 AND MAR.
     ;       ENTER OUTPUT MODE. (TURNS ON WRITE CLOCK.)
     ;       INITIALIZE COUNTER FOR OUTPUT DATA PREAMBLE LOOP.
     ;
00ED WRSEC1: SOR     W,NEG,SOAR,R4
     /       &NODLE  &IEN    &NOOEY  &NOSRE
     /       &MADR   &NOJMPI &OUPT
     /       &LDCT   5
     ;
     ;
     ;       BEGIN WRITE DATA PREAMBLE LOOP.
     ;       TURN ON WRITE GATE.
     ;       PASS WHEN FIFO ARRAY READY FOR OUTPUT.
     ;
     WRSEC2: NOOP
00EE /       &NODLE  &NOIEN  &NOOEY  &NOSRE
     /       &NOJMPI &OUPT   &WRGA
     /       &IFNOT  RDYO    &CJP    $
     ;
     ;
     ;       OUTPUT H#0000 TO FIFO ARRAY.
     ;
00EF         SONR    W,MOVE,SOZ,NRY
     /       &NODLE  &NOIEN  &OEY    &NOSRE
     /       &NOJMPI &OUPT   &WRGA
     /       &CONT
     ;
     ;
     ;       END WRITE DATA PREAMBLE LOOP.
     ;
00F0         SONR    W,MOVE,SOZ,NRY
     /       &NODLE  &NOIEN  &OEY    &NOSRE
     /       &BF16   &BT03   &NOJMPI &OUPT   &PL03   &WRGA
     /       &RPCT   WRSEC2
     ;
     ;
     ;       OUTPUT LAST DATA PREAMBLE BYTE AND THE H#FE DATA SYNC BYTE.
     ;       INITIALIZE COUNTER FOR WRITE DATA SEGMENT LOOP.
     ;       PASS WHEN FIFO ARRAY AGAIN READY FOR OUTPUT.
     ;
00F1 WRSEC3: SONR    W,MOVE,SOI,NRY
     /       &DLE    &NOIEN  &OEY    &NOSRE
     /       &NOJMPI &OUPT   &WRGA
     /       &LDCT   131
     ;
00F2         IMME    H#FE00
     /       &DLE    &NOIEN  &OEY    &NOSRE
     /       &NOJMPI &OUPT   &WRGA
     /       &IFNOT  RDYO    &CJP    WRSEC3
     ;
00F3         SONR    W,MOVE,SOD,NRY
     /       &NODLE  &NOIEN  &OEY    &NOSRE
     /       &BF16   &BT03   &NOJMPI &OUPT   &PL03   &WRGA
     /       &CONT
```

```
                ;
                ;       BEGIN WRITE DATA SEGMENT LOOP.
                ;       (R4) TO MAR.
                ;
00F4 WRSEC4:    SOR     W,MOVE,SORY,R4
                /       &NODLE  &NOIEN  &OEY    &NOSRE
                /       &MADR   &NOJMPI &OUPT   &WRGA
                /       &CONT
                ;
                ;
                ;       INCREMENT (R4).
                ;
00F5            SOR     W,INC,SORR,R4
                /       &NODLE  &IEN    &NOOEY  &NOSRE
                /       &NOJMPI &OUPT   &WRGA
                /       &CONT
                ;
                ;
                ;       ((MAR)) TO FIFO ARRAY.
                ;       END WRITE DATA SEGMENT LOOP.
                ;
                NOOP
00F6            /       &NODLE  &NOIEN  &NOOEY  &NOSRE
                /       &BT03   &MREA   &NOJMPI &OUPT   &PL03   &WRGA
                /       &RPCT   WRSEC4
                ;
                ;
                ;       CLEAR (R4).
                ;       INITIALIZE COUNTER FOR WRITE DATA POSTAMBLE LOOP.
                ;
00F7            SOR     W,MOVE,SOZR,R4
                /       &NODLE  &IEN    &NOOEY  &NOSRE
                /       &NOJMPI &OUPT   &WRGA
                /       &LDCT   1
                ;
                ;       BEGIN WRITE DATA POSTAMBLE LOOP.
                ;       OUTPUT H#0000 TO FIFO ARRAY.
                ;
00F8 WRSEC5:    SOR     W,MOVE,SORY,R4
                /       &NODLE  &NOIEN  &OEY    &NOSRE
                /       &NOJMPI &OUPT   &WRGA
                /       &IFNOT  RDYO    &CJP    $
                ;
00F9            SOR     W,MOVE,SORY,R4
                /       &NODLE  &NOIEN  &OEY    &NOSRE
                /       &BF16   &BT03   &NOJMPI &OUPT   &PL03   &WRGA
                /       &CONT
                ;
                ;
                ;       (NOOP FOR TIMING PURPOSES)
                ;       END WRITE DATA POSTAMBLE LOOP.
                ;
                NOOP
00FA            /       &NODLE  &NOIEN  &NOOEY  &NOSRE
                /       &NOJMPI &OUPT   &WRGA
                /       &RPCT   WRSEC5
                ;
                ;
                ;       TURN OFF WRITE GATE.
                ;
                NOOP
00FB            /       &NODLE  &NOIEN  &NOOEY  &NOSRE
                /       &NOJMPI &OUPT
                /       &CONT
                ;
                ;
                ;       THEN LEAVE OUTPUT MODE. (TURNS OFF WRITE CLOCK.)
                ;       LOAD 0 INTO R0.
                ;       RETURN.
                ;
00FC            SOR     W,MOVE,SOZR,R0
                /       &NODLE  &IEN    &NOOEY  &NOSRE
                /       &NOJMPI
                /       &RTN
                ;
                END
```

0000	1100000111100000	0010011000110000	0110100100111XXXX	XXXXXXXXXXXXXX10	XXXXXXXXXXXXXXXX
0001	1111100011100000	XXXX001011101111	111111XXXXXXXXXX	XXXXXXXXXXXXXX10	XXXXXXXXXXXXXXXX
0002	0000000000000000	XXXX001011101111	111111XXXXXXXXXX	XXXXXXXX0XXXXX10	XXXXXXXXXXXXXXXX
0003	1111100011100000	XXXX001011101111	111111XXXXXXXXXX	XXXXXXXXXXXXXX10	XXXXXXXXXXXXXXXX
0004	0000000000010000	XXXX001011000001	111111XXXXXXXXXX	XXXXXXXX0XXXXX10	XXXXXXXXXXXXXXXX
0005	1101100001000011	XXXX001111101111	111111XXXXXXXXXX	XXXXXXXXXXXXXX10	XXXXXXXXXXXXXXXX
0006	1101100011000100	XXXX010011101111	111111XXXXXXXXXX	XXXXXXXXXXXXXX10	XXXXXXXXXXXXXXXX
0007	1101100001000100	XXXX001011101111	111111XXXXXXXXXX	XXXXXXXXXXXXXX10	0XXXXXXXXXXXXXXX
0008	0111000101000000	XXXX011011101111	111111XXXXXXXXXX	XXXXXX0XXXXXX10	XXXXXXXXXXXXXXXX
0009	0111000101000000	XXXX011011101111	111111XXXXXXXXXX	XXXXXXXXXX0XX10	XXXXXXXXXXXXXXXX
000A	0111000101000000	XXXX011011101111	111111XXXXXXXXXX	XXXXXXXXXXXXXX10	XXXXXXXXXXXXXXXX
000B	0111000101000000	XXXX011011101111	111111XXXXXXXXXX	XXXXXX0XXXXXX10	XXXXXXXXXXXXXXXX
000C	1101110101100100	XXXX010010010000	000111XXXXXXXXXX	XXXXXXXXXX0XX10	XXXXXXXXXXXXXXXX
000D	1111100011100000	XXXX001011101111	111111XXXXXXXXXX	XXXXXXXXXXXXXX10	XXXXXXXXXXXXXXXX
000E	0000000000010001	XXXX001011000000	000010XXXXXXXXXX	XXXXXXX0XXXXX10	XXXXXXXXXXXXXXXX
000F	1101100001000100	XXXX001011101111	111111XXXXXXXXXX	XXXXXXXXXX0XX10	0XXXXXXXXXXXXXXX
0010	0111000101000000	XXXX011011101111	111111XXXXXXXXXX	XXXXXXXX0XXXX10	XXXXXXXXXXXXXXXX
0011	0111000101000000	XXXX011011101111	111111XXXXXXXXXX	XXXXXXXXXXXXXX10	XXXXXXXXXXXXXXXX
0012	0111000101000000	XXXX011011101111	111111XXXXXXXXXX	XXXXXXXXXX0XX10	XXXXXXXXXXXXXXXX
0013	0111000101000000	XXXX011011101111	111111XXXXXXXXXX	XXXXXXXXXXXXXX10	XXXXXXXXXXXXXXXX
0014	1101110101100100	XXXX010010010000	001111XXXXXXXXXX	X00XXXXXXXXXXX10	XX0XXXXXXXXXXXXX
0015	1101100100000101	XXXX010011101111	111111XXXXXXXXXX	XXXXXXXXXX0XX10	XXXXXXXXXXXXXXXX
0016	0111000101000000	XXXX011011101111	111111XXXXXXXXXX	XXXXXXXX0XXXX10	XXXXXXXXXXXXXXXX
0017	0101100011000101	XXXX010111101111	111111XXXXXXXXXX	X0XXX0XXXXXXX10	XXXXXXXXXXXXXXXX
0018	1101100001000100	XXXX001011101111	111111XXXXXXXXXX	XXXXXXXXXXXXXX10	0XXXXXXXXXXXXXXX
0019	1101100001000101	XXXX001011101111	111111XXXXXXXXXX	0XXXXXXXXXXXX10	XX0XXXXXXXXXXXXX
001A	1111100011100001	XXXX010011101111	111111XXXXXXXXXX	XXXXXXXXXXXXXX10	XXXXXXXXXXXXXXXX
001B	0000000000110110	XXXX010011101111	111111XXXXXXXXXX	XXXXXXXXXXXXXX10	XXXXXXXXXXXXXXXX
001C	1000100000000000	XXXX010011101111	111111XXXXXXXXXX	XXXXXXXXXXXXXX10	XXXXXXXXXXXXXXXX
001D	1111100011100001	XXXX010011101111	111111XXXXXXXXXX	XXXXXXXXXXXXXX10	XXXXXXXXXXXXXXXX
001E	1100000000000001	XXXX010011101111	111111XXXXXXXXXX	XXXXXXXXXXXXXX10	XXXXXXXXXXXXXXXX
001F	1101100100000100	XXXX010011101111	111111XXXXXXXXXX	XXXXXXXXXXXXXX10	XXXXXXXXXXXXXXXX
0020	1101100001000001	XXXX010111000000	010000XXXXXXXXXX	XXXXXXXXXXXXXX10	XXXXXXXXXXXXXXXX
0021	1101100011000101	XXXX010011101111	111111XXXXXXXXXX	XXXXXXXXXXXXXX10	XXXXXXXXXXXXXXXX
0022	1100000011000101	XXXX010011101111	111111XXXXXXXXXX	XXXXXXXXXXXXXX10	XXXXXXXXXXXXXXXX
0023	1100110001100100	XXXX010010010000	100010XXXXXXXXXX	XXXXXXXXXXXXXX10	XXXXXXXXXXXXXXXX
0024	1101100001000010	XXXX010111000000	010000XXXXXXXXXX	XXXXXXXXXXXXXX10	XXXXXXXXXXXXXXXX
0025	1101100011000101	XXXX010011101111	111111XXXXXXXXXX	XXXXXXXXXXXXXX10	XXXXXXXXXXXXXXXX
0026	1100000011000101	XXXX010011101111	111111XXXXXXXXXX	XXXXXXXXXXXXXX10	XXXXXXXXXXXXXXXX
0027	1100110001100100	XXXX010010010000	100110XXXXXXXXXX	XXXXXXXXXXXXXX10	XXXXXXXXXXXXXXXX
0028	0111000101000000	XXXX011011000001	000000XXXXXXXXXX	XXXXXXXXXXXX010	XXXXXXXX0XXXXX
0029	0111000101000000	XXXX011011101111	111111XXXXX0XXX	XXXXXXXXXXXX010	XXXXXXXX00XXXX
002A	0111000101000000	XXXX011000110000	101010101001OXXX	XXXXXXXXXXXX010	XXXXXXXX0XXXXX
002B	0111000101000000	XXXX011000110000	101011011011XXXX	XXXXXXXXXXXX010	XXXXXXXX0XXXXX
002C	1101100011000101	XXXX010100110000	101100011011XXX0	XXXXX0XXXXXX010	XXXXXXXX0XXXXX
002D	1001000111100001	0010111000110000	110011010010XXXX	XXXXXXXXXXXX010	XXXXXXXX0XXXXX
002E	0111000101000000	XXXX011011101111	111111XXXXXXXXXX	XXXXXXXXXXXX010	XXXXXX0XX0XXXXX
002F	1101100011000101	XXXX010100110000	101111011011XXX0	XXXXX0XXXXXX010	XXXXXXXX0XXXXX
0030	1001000111100010	0010111000110000	110011010010XXXX	XXXXXXXXXXXX010	XXXXXX0XX0XXXXX
0031	1101100011000101	XXXX010111101111	111111XXXXXXXX0	XXXXX0XXXXXX010	XXXXXXXX0XXXXX
0032	1001000111100100	0010111000110000	110101010010XXXX	XXXXXXXXXXXX010	XXXXXXXX0XXXXX
0033	1101100001000000	XXXX011010010000	101001XXXXXXXXXX	XXXXXXXXXXXXXX10	XXXXXXXXXXXXXXXX
0034	1101100000000000	XXXX010010101111	111111011110XXXX	XXXXXXXXXXXX10	XXXXXXXXXXXXXXXX
0035	1101100001000000	XXXX001011101111	111111XXXXXXXXXX	XXXXXXXXXXXXXX01	XXXXXXXXXXXXXXXX
0036	1101111000000011	XXXX010000110000	111000011110XXXX	XXXXXXXXXXXXXX10	XXXXXXXXX0XXXXX
0037	1101111000000011	XXXX010000110011	101101011110XXXX	XXXXXXXXXXXXXX10	XXXXXXXXX0XXXXX
0038	1101111010000100	XXXX000011000001	000001XXXXXXXXXX	XXXXXXXXXXXX010	0XXXXXXXX00XXXXX
0039	1101101010000101	XXXX010000110000	111001011011XXXX	XXXXXXXXXXXX010	XXXXXXXX0XXXXXX

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003A 1111100011100000 XXXX001011101111 111111XXXXXXXXXX XXXXXXXXXXXXX010 XXXXXXXXX0XXXXXX
003B 0000000000000011 XXXX001011101111 111111XXXXXXXXXX XXXXXXXXXXXXX010 XXXXXXXXX0XXXXXX
003C 1111100011100000 XXXX001011101111 111111XXXXXXXXXX XXXXXXXXXXXXX010 XXXXXXXXX0XXXXXX
003D 0000000000010011 XXXX001011101111 111111XXXXXXXXXX XXXXXXXX0XXXX010 XXXXXXXXX0XXXXXX
003E 0111000101000000 XXXX011011101111 111111XXXXXXXXXX XXXXXXXXXXXXX010 XXXXXX0XX0XXXXXX
003F 0111000101000000 XXXX011000110000 111111011011XXX0 XXXXXXXXXXXXX010 XX0XXXXXX0XXXXXX
0040 1101110101100101 XXXX000011101111 111111XXXXXXXXXX XXXXXXXXXXXXX010 0XXXXXXXX0XXXXXX
0041 1101110101100100 XXXX000011101111 111111XXXXXXXXXX XXXXXX0XXXX0X010 00XXXX0XX0XXXXXX
0042 0111000101000000 XXXX011000110001 000010011011XXX0 XXXXXXXXXXXXX010 XX0XXXXXX0XXXXXX
0043 1101100101100101 XXXX000011101111 111111XXXXXXXXXX XXXXXXXXXXXXX010 0XXXXXXXX0XXXXXX
0044 1101110101100100 XXXX000010010000 111111XXXXXXXXXX XXXXXXX0XXX0X010 00XXXX0XX0XXXXXX
0045 0111000101000000 XXXX011011000001 000001XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0046 1101110101100101 XXXX000011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 0XXXXXXXXXXXXXXX
0047 0111000101000000 XXXX011011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0048 0111000101000000 XXXX011011101111 111111XXXXXXXXXX XXXXXX0XXXX0XX10 X0XXXXXXXXXXXXXX
0049 0111000101000000 XXXX011011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
004A 0111000101000000 XXXX011011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
004B 0111000101000000 XXXX011010010001 000110XXXXXXXXXX XXXXXXX0XXX0XX10 X0XXXXXXXXXXXXXX
004C 0111000101000000 XXXX011000110001 001110010110XXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
004D 1101100100000000 XXXX010010101111 111111011110XXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
004E 1111100011100000 XXXX001011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
004F 0000000000011111 XXXX001011101111 111111XXXXXXXXXX 0XXXXXX0XXXXX10 XXXXXXXXXXXXXXXX
0050 1101100100001000 XXXX010011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0051 1111100011100001 XXXX010011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0052 0000000000010110 XXXX010011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0053 0111000101000000 XXXX011000110001 011001010100XXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0054 1110000110000101 XXXX110000110001 010110010000XXXX XXXXXXXXXX0XX10 XXXXXXXXXXXXXXXX
0055 1100011111001000 XXXX010000110001 010111011110XXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0056 1100000111001000 XXXX010011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0057 0111000101000000 0111011000110001 010011010011XXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0058 1100001110000000 XXXX000010101111 111111011110XXXX 0XXXXXX0XXXXX10 XXXXXXXXXXXXXXXX
0059 1101100011101001 XXXX010011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
005A 0000000000001101 XXXX010011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
005B 1101100011101010 XXXX010011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
005C 0000000001011001 XXXX010011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
005D 1101100011101011 XXXX010011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
005E 0000000000010111 XXXX010011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
005F 1101100011101100 XXXX010011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0060 0000000010010000 XXXX010011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0061 1011111100101100 XXXX010111101111 111111XXXXXXXXXX XX0XX0XXXXXXXX10 XXXXX0XXXXXXXXXX
0062 0000000000000111 XXXX000000110001 100010011110XXXX XX0XX0XXXXXXXX01 XXXXX0XXXXXXXXXX
0063 1001110000001001 XXXX010011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0064 0000000000001101 XXXX010011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0065 1001110000001010 XXXX010011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0066 0000000001011001 XXXX010011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0067 1001110000001011 XXXX010011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0068 0000000000010111 XXXX010011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0069 1101100100000111 XXXX010011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
006A 1101100011101100 XXXX010011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
006B 1110011100100011 XXXX010011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
006C 1101100011101101 XXXX010011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
006D 0000000000000110 XXXX010011000000 000100XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
006E 1101100001001000 XXXX001100010011 011011011110XXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
006F 1011111110101000 XXXX010011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0070 1100011110001101 XXXX010011000000 000011XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0071 1101100001001001 XXXX001100010011 011011011110XXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0072 1101010100110000 XXXX010011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0073 1100001110001101 XXXX010011000000 000110XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
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0074 1101100001001010 XXXX001100010011 0110110111110XXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0075 1010100100101000 XXXX010011101111 1111111XXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0076 1100011110001101 XXXX010011000000 0001100XXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0077 1101100001001011 XXXX001100010011 0110110111110XXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0078 0111000100000000 XXXX010011101111 1111111XXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0079 1101100011101101 XXXX000111000000 0001110XXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
007A 0000010001110111 XXXX000100010011 1001000111110XXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
007B 1110111011100010 XXXX010011101111 1111111XXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
007C 1001110000100111 XXXX010011101111 1111111XXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
007D 0000000000001000 XXXX010011101111 1111111XXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
007E 1101100100001000 XXXX010011101111 1111111XXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
007F 1101100100001001 XXXX010011101111 1111111XXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0080 1101100000001001 XXXX010011101111 1111111XXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0081 1011100111000110 XXXX010011101111 1111111XXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0082 0000111111111111 XXXX010011101111 1111111XXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0083 1001110011000110 XXXX010011101111 1111111XXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0084 0000000000001111 XXXX010011101111 1111111XXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0085 1001110010000110 XXXX010011101111 1111111XXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0086 0000000010100101 XXXX000011101111 1111111XXXXXXXXX XXXXXXXXXXXXXX01 XXXXXXXXXXXXXXXX
0087 1000000001000100 XXXX010011101111 1111111XXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
0088 1110000110000101 XXXX000011101111 1111111XXXXXXXXX XXXXXXXXXXXXXX10 0XXXXXXXXXXXXXXX
0089 1001111100001000 XXXX010111101111 1111111XXXXXXXXX XXXXX0XXXXXXXX10 XXXXXXXXXXXXXXXX
008A 1101100001001000 XXXX001011101111 1111111XXXXXXXXX 0XXXXXXXXXXXXX10 XX0XXXXXXXXXXXXX
008B 1111110010000000 XXXX001011101111 1111111XXXXXXXXX XXXXXXXXXXXXXX10 0XXXXXXXXXXXXXXX
008C 1001111100001001 XXXX010111101111 1111111XXXXXXXXX XXXXX0XXXXXXXX10 XXXXXXXXXXXXXXXX
008D 1101100001001001 XXXX001011101111 1111111XXXXXXXXX 0XXXXXXXXXXXXX10 XX0XXXXXXXXXXXXX
008E 1101100100000000 XXXX000010101111 1111110111110XXXX 0XXXXXXX0XXXXX10 XXXXXX0XXXXXXXXX
0090 1100000111101001 XXXX110000110010 0111010111110XXXX XXXXXXXXXX0XX10 XXXXX0XXXXXXXXX
0091 1100000111101011 XXXX110000110010 0110000111110XXXX XXXXXXXXXX0XX10 XXXXX0XXXXXXXXX
0092 1100000111101001 XXXX110000110010 0110010111110XXXX XXXXXXXXXX0XX10 XXXXX0XXXXXXXXX
0093 1100000111101011 XXXX110000110010 0110110111110XXXX XXXXXXXXXX0XX10 XXXXX0XXXXXXXXX
0094 1100000111101010 XXXX110000110010 0110100111110XXXX XXXXXXXXXX0XX10 XXXXX0XXXXXXXXX
0095 1100000111101010 XXXX110000110010 0110110111110XXXX XXXXXXXXXX0XX10 XXXXX0XXXXXXXXX
0096 1100000111101001 XXXX110000110010 0110110111110XXXX XXXXXXXXXX0XX10 XXXXX0XXXXXXXXX
0097 1101100100000110 XXXX110000110001 1000110111110XXXX XXXXXXXXXXXXX10 XXXXX0XXXXXXXXX
0098 0111000101000000 XXXX011000110010 0111100111110XXXX XXXXXXXXXX0XX10 XXXXX0XXXXXXXXX
0099 0111000101000000 XXXX011000110010 1000010111110XXXX XXXXXXXXXX0XX10 XXXXX0XXXXXXXXX
009A 0111000101000000 XXXX011000110010 1000110111110XXXX XXXXXXXXXX0XX10 XXXXX0XXXXXXXXX
009B 0111000101000000 XXXX011011101111 1111111XXXXXXXXX XXXXXXXXXX0XX10 XXXXX0XXXXXXXXX
009C 0111000101000000 XXXX011000110010 0111110111110XXXX XXXXXXXXXX0XX10 XXXXX0XXXXXXXXX
009D 1100000111101011 0111110000110001 0110000100110XXXX XXXXXXXXXX0XX10 XXXXX0XXXXXXXXX
009E 1100000111101010 0111110000110001 0110000100110XXXX XXXXXXXXXX0XX10 XXXXX0XXXXXXXXX
009F 1011111100101100 0111010100110001 0101110100110XXXX XX0XX0XXXXXXXX10 XXXXX0XXXXXXXXX
00A0 0000000000000111 XXXX000000110010 1000000111110XXXX XX0XX0XXXXXXXX01 XXXXX0XXXXXXXXX
00A1 1100000111101011 0111110000110010 0111110100110XXXX XXXXXXXXXX0XX10 XXXXX0XXXXXXXXX
00A2 0111000101000000 XXXX011000110001 0110000111110XXXX XXXXXXXXXXXXX10 XXXXXXXXXXXXXXX
00A3 1100000111101001 0111110000110010 0111110100110XXXX XXXXXXXXXX0XX10 XXXXX0XXXXXXXXX
00A4 0111000101000000 XXXX011000110001 0110000111110XXXX XXXXXXXXXXXXX10 XXXXXXXXXXXXXXX
00A5 1011001100101000 XXXX010100110010 1101010111110XXXX X00XX0XXXXXXX10 XXXXXXXXXXXXXXX
00A6 1011010100101000 XXXX010100110010 1101100111110XXXX X00XX0XXXXXXX10 XXXXXXXXXXXXXXX
00A7 1011011100101000 XXXX010100110010 1101110111110XXXX X00XX0XXXXXXX10 XXXXXXXXXXXXXXX
00A8 1011100100101000 XXXX010100110010 1110000111110XXXX X00XX0XXXXXXX10 XXXXXXXXXXXXXXX
00A9 1011101100101000 XXXX010100110010 1110010111110XXXX X00XX0XXXXXXX10 XXXXXXXXXXXXXXX
00AA 1011110100101000 XXXX010100110010 1110100111110XXXX X00XX0XXXXXXX10 XXXXXXXXXXXXXXX
00AB 1011111100101000 XXXX010100110010 1110110111110XXXX X00XX0XXXXXXX10 XXXXXXXXXXXXXXX
00AC 1010000100101000 XXXX010100110010 1111000111110XXXX X00XX0XXXXXXX10 XXXXXXXXXXXXXXX
00AD 1010001100101000 XXXX010100110010 1111010111110XXXX X00XX0XXXXXXX10 XXXXXXXXXXXXXXX
00AE 1010010100101000 XXXX010100110010 1111100111110XXXX X00XX0XXXXXXX10 XXXXXXXXXXXXXXX
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00AF 1010011100101000 XXXX0101001100l0 1111110111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00B0 1010100100101000 XXXX0101001100l1 0000000111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00B1 1010101100101000 XXXX0101001100l1 0000010111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00B2 1010110100101000 XXXX0101001100l1 0000100111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00B3 1010111100101000 XXXX0101001100l1 0000110111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00B4 1011000100101000 XXXX0101001100l1 0001000111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00B5 0000000000000001 XXXX0101001100l1 0001010111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00B6 0000000000000011 XXXX0101001100l1 0001100111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00B7 0000000000000111 XXXX0101001100l1 0001110111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00B8 0000000000001111 XXXX0101001100l1 0010000111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00B9 0000000000011111 XXXX0101001100l1 0010010111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00BA 0000000000111111 XXXX0101001100l1 0010100111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00BB 0000000001111111 XXXX0101001100l1 0010110111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00BC 0000000011111111 XXXX0101001100l1 0011000111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00BD 0000000111111111 XXXX0101001100l1 0011010111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00BE 0000001111111111 XXXX0101001100l1 0011100111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00BF 0000011111111111 XXXX0101001100l1 0011110111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00C0 0000111111111111 XXXX0101001100l0 0001110111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00C1 0001111111111110 XXXX0101001100l0 0001110111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00C2 0011111111111100 XXXX0101001100l0 0001110111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00C3 0111111111111000 XXXX0101001100l0 0001110111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00C4 1111111111110000 XXXX0101001100l0 0001110111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00C5 1011001100101001 XXXX0101001100l1 0100000111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00C6 1011010100101001 XXXX0101001100l1 0100010111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00C7 1011011100101001 XXXX0101001100l1 0100100111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00C8 1011100100101001 XXXX0101001100l1 0100110111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00C9 1011101100101001 XXXX0101001100l1 0101000111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00CA 1011110100101001 XXXX0101001100l1 0101010111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00CB 1011111100101001 XXXX0101001100l1 0101100111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00CC 1010000100101001 XXXX0101001100l1 0101110111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00CD 1010001100101001 XXXX0101001100l1 0110000111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00CE 1010010100101001 XXXX0101001100l1 0110010111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00CF 1010011100101001 XXXX0101001100l1 0110100111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00D0 1111111111100000 XXXX0101001100l0 0001110111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00D1 1111111111000000 XXXX0101001100l0 0001110111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00D2 1111111110000000 XXXX0101001100l0 0001110111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00D3 1111111100000000 XXXX0101001100l0 0001110111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00D4 1111111000000000 XXXX0101001100l0 0001110111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00D5 1111110000000000 XXXX0101001100l0 0001110111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00D6 1111100000000000 XXXX0101001100l0 0001110111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00D7 1111000000000000 XXXX0101001100l0 0001110111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00D8 1110000000000000 XXXX0101001100l0 0001110111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00D9 1100000000000000 XXXX0101001100l0 0001110111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00DA 1000000000000000 XXXX0101001100l0 0001110111l0XXXX X00XX0XXXXXXXX10 XXXXXXXXXXXXXXXX
00DB 1100111010001000 XXXX1100111011111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
00DC 1101100001001101 XXXX0011111011111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
00DD 1101100000001100 1000010000110011 1000000100llXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
00DE 1001100010000110 XXXX1100111011111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
00DF 1001111010100111 XXXX0100111011111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
00E0 1100110000001100 XXXX1100111011111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
00E1 1100110001001101 XXXX0001111011111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
00E2 1100110010001000 XXXX1100100100011 011101XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
00E3 1101100011101100 XXXX0100101011111 1111110111l0XXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
00E4 1101100000001100 XXXX0100111011111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
00E5 1001100001000110 XXXX1100111011111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
00E6 1001111001100111 XXXX1100111011111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
00E7 0111000101000000 0111010000110011 1010100100llXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
00E8 1001100010000110 XXXX1100111011111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
```

```
00E9 1001111010100111 XXXX010011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
00EA 1100110010001101 XXXX100111101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
00EB 1100110011001100 XXXX010010010011 100101XXXXXXXXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
00EC 1001110000000110 XXXX110010101111 111111011110XXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
00ED 1101111010000100 XXXX010011000000 000101XXXXXXXXXX XXXXXXXXXXXXXX10 0XX0XXXXXXXXXXXX
00EE 0111000101000000 XXXX011000110011 101110011101XXXX XXXXXXXXXXXXXX10 XXX0XXXXXXXX0XXX
00EF 1111100100000000 XXXX001011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXX0XXXXXXXX0XXX
00F0 1111100100000000 XXXX001010010011 101110XXXXXXXXXX 0XXX0XXXXXXXXX10 XXX0XXX0XXXX0XXX
00F1 1111100011100000 XXXX001111000010 000011XXXXXXXXXX XXXXXXXXXXXXXX10 XXX0XXXXXXXX0XXX
00F2 1111111000000000 XXXX001100110011 110001011101XXXX XXXXXXXXXXXXXX10 XXX0XXXXXXXX0XXX
00F3 1111100011000000 XXXX001011101111 111111XXXXXXXXXX 0XXX0XXXXXXXXX10 XXX0XXX0XXXX0XXX
00F4 1101100001000100 XXXX001011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 0XX0XXXXXXXX0XXX
00F5 1101110101100100 XXXX010011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXX0XXXXXXXX0XXX
00F6 0111000101000000 XXXX011010010011 110100XXXXXXXXXX XXXX0XXXXXXXXX10 X0X0XXX0XXXX0XXX
00F7 1101100100000100 XXXX010011000000 000001XXXXXXXXXX XXXXXXXXXXXXXX10 XXX0XXXXXXXX0XXX
00F8 1101100001000100 XXXX001000110011 111000011101XXXX XXXXXXXXXXXXXX10 XXX0XXXXXXXX0XXX
00F9 1101100001000100 XXXX001011101111 111111XXXXXXXXXX 0XXX0XXXXXXXXX10 XXX0XXX0XXXX0XXX
00FA 0111000101000000 XXXX011010010011 111000XXXXXXXXXX XXXXXXXXXXXXXX10 XXX0XXXXXXXX0XXX
00FB 0111000101000000 XXXX011011101111 111111XXXXXXXXXX XXXXXXXXXXXXXX10 XXX0XXXXXXXXXXXX
00FC 1101100100000000 XXXX010010101111 111111011110XXXX XXXXXXXXXXXXXX10 XXXXXXXXXXXXXXXX
```

SYMBOLS

A1LSW	E723	L	0008
A1MSW	0006	LD2NA	0006
A2LSW	BFA8	LD2NR	000C
A2NA	0004	LD2NY	0016
A2NDY	0014	LDC2NA	0007
A2NR	000E	LDC2NR	000D
A3LSW	D530	LDC2NY	0017
A4LSW	A928	LINK	0057
ADD	0004	LOW	0004
ADDC	0005	M1	0053
AE	0056	M1A1	0069
AE20	0008	M234I	0059
AND	0006	M2A2	006F
ASCEBC	0000	M3A3	0072
ATTN	0010	M4A4	0075
B	0000	MARI	000C
BACK	0011	MATCH1	0035
BCDEBC	0001	MDAI	0007
BRTABL	0036	MDAR	0008
BUSY	0012	MDRA	000A
C	0005	MDRI	0009
CDAI	0002	MFIX	0063
CDRA	0004	MOVE	000C
CDRI	0003	MRAI	000E
CFCODE	001A	MUL	00DB
COMP	000D	N	0007
CRAI	0005	N0	0000
CRCFL1	0022	N1	0001
CRCFL2	0026	N2	0002
CRCMSK	C001	N3	0003
CRCNIT	0010	N4	0004
CT16	0009	N5	0005
CYC	00DD	N6	0006
CYC1	00E5	N7	0007
DIV	00E4	N8	0008
EBCASC	0002	N9	0009
EBCBCD	0003	NA	000A
EP20	000A	NAND	0007
ER20	000B	NB	000B
ERR	0058	NC	000C
EXNOR	000B	ND	000D
EXOR	0008	NE	000E
F1	0009	NEG	000F
F2	000A	NF	000F
F3	000B	NO	0001
FAIL	000C	NOR	0009
INC	000E	NOTQ	00E0
INDX	0013	NOZ	0000
KL128	7100	NRA	0001
KLSW	EEE2	NRAS	0005
KM128	0477	NRS	0004
KMSW	0008	NRY	0000

NSPASS	0040
OR	000A
OVR	0003
PCPREL	0007
PF1	0016
PF2	000D
PF3	0059
PF4	0017
PM1	009F
PM2	0015
PM23	00A3
PM234	009D
PM24	00A1
PM3	0016
PM34	009E
PM4	0017
POS	00EA
PR1A	0008
PR1D	0009
PR1R	000B
PR1Y	000A
PR2A	0000
PR2Y	0002
PR3A	0004
PR3D	0006
PR3R	0003
PRA	0008
PRI	000B
PRT1A	0007
PRTA	0004
PRTD	0006
PRZ	000A
R0	0000
R1	0001
R10	000A
R11	000B
R12	000C
R13	000D
R14	000E
R15	000F
R16	0010
R17	0011
R18	0012
R19	0013
R2	0002
R20	0014
R21	0015
R22	0016
R23	0017
R24	0018
R25	0019
R26	001A
R27	001B
R28	001C
R29	001D
R3	0003
R30	001E
R31	001F
R4	0004
R5	0005
R6	0006
R7	0007
R8	0008
R9	0009
RDITCT	0041
RDSEC1	0038
RDSEC2	003F
RDSEC3	0046
RDSEC4	004E
RDYI	000D
RDYO	000E
REP1	00B5
REP10	00BE
REP11	00BF
REP12	00C0
REP13	00C1
REP14	00C2
REP15	00C3
REP16	00C4
REP17	00D0
REP18	00D1
REP19	00D2
REP2	00B6
REP20	00D3
REP21	00D4
REP22	00D5
REP23	00D6
REP24	00D7
REP25	00D8
REP26	00D9
REP27	00DA
REP3	00B7
REP4	00B8
REP5	00B9
REP6	00BA
REP7	00BB
REP8	00BC
REP9	00BD
RF1	0006
RF2	0009
RF3	000A
RL	0005
RM1	00C5
RM10	00CE
RM11	00CF
RM2	00C6
RM3	00C7
RM4	00C8
RM5	00C9
RM6	00CA
RM7	00CB
RM8	00CC
RM9	00CD
RONCZ	0003
RSTNA	0001
RSTND	0011
RSTNR	000E
RTAA	001D
RTAR	0000
RTAY	001C
RTDA	0019
RTDR	0001
RTDY	0018
RTRA	000C
RTRR	000F
RTRY	000E

```
S2NA      0005
S2NDY     0015
S2NR      000F
SAMD      0014
SCBIBL    000F
SECTIO    0000
SECTL1    0029
SECTL2    0033
SETNA     0002
SETND     0012
SETNR     000D
SF1       0006
SF2       0009
SF3       000A
SHA       0006
SHD       0007
SHDN1     0005
SHDNC     0007
SHDNL     0006
SHDNOV    0008
SHDNZ     0004
SHDR      0007
SHRR      0006
SHUP1     0001
SHUPL     0002
SHUPZ     0000
SL        0005
SOA       0004
SOAR      0004
SOD       0006
SODR      0006
SOI       0007
SOIR      0007
SONZC     0003
SORA      0000
SORR      000B
SORS      0003
SORY      0002
SOSE      000A
SOSER     000A
SOZ       0008
SOZE      0009
SOZER     0009
SOZR      0008
SUBK      007B
SUBR      0000
SUBRC     0001
SUBS      0002
SUBSC     0003
SUCC      000F
TAB1      0090
TAB2      00A5
TC        000A
TF1       0012
TF2       0014
TF3       0016
TL        0010
TLOW      0008
TM1       009B
TM23      009A
TM24      0099
TM34      0098
TN        000E
TNO       0002
TNOZ      0000
TOAI      0002
TOAIR     0002
TODA      0001
TODAR     0001
TODI      0005
TODIR     0005
TODRA     0003
TODRR     000F
TODRY     000B
TORAA     0000
TORAR     000C
TORAY     0008
TORIA     0002
TORIR     000E
TORIY     000A
TOVR      0006
TSTNA     0000
TSTND     0010
TSTNR     000F
TZ        0004
TZC       000C
W         0001
WRSEC1    00ED
WRSEC2    00EE
WRSEC3    00F1
WRSEC4    00F4
WRSEC5    00F8
XOR       0087
XORMEM    007E
Z         0002
ZC        0006

TOTAL PHASE 2 ERRORS =    0
```

Am29116 Architecture Speeds Pixel Manipulation In Interactive Bit-Mapped Graphics

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Advanced Micro Devices

6

	Advantages	Disadvantages
Stroke System	High resolution Inexpensive video generation electronics Fast image update	Expensive deflection circuitry – tube Fast redraw requirement (flicker complexity of image) DVST (no selective erasure)
Raster Scan Conversion System	Lower cost than stroke system	Complex scan conversion circuits
Raster Scan Bit-Mapped System	Traditional TV approach Used for years in alphanumerics Support graphics with bit maps Support complex flicker free display	Lower resolution than stroke Lots of memory

Figure 1. Comparison of Display Technologies

INTRODUCTION

Bit-mapped raster scan technology is becoming increasingly popular due to the decreasing costs of high density random access memory and the availability of high spped, cost effective VLSI building blocks for implementing complex, flicker free images. This article shows how the Am29116 can be used in a bit-mapped graphics processor to draw vectors, characters and filled polygons at high speed and to support high bandwidth display update and motion dynamics interactively.

There are traditionally three basic cathode ray tube (CRT) graphics technologies – the stroke system, the raster scan conversion system and the raster scan bit-mapped system. (Figure 1). In a stroke system, vectors are represented by point coordinates and point-to-point plotting instructions. These instructions are used to randomly deflect an electron writing beam on the CRT. A line can also be moved or rotated very fast by re-calculating only the end-point coordinates. Very high resolution can be achieved; vector systems with 4096 x 4096 pixel spatial resolution are not uncommon; however, the complex deflection circuitry also make them expensive. Since the vector image has to be redrawn continuously (at least 30 times/second), there is an upper bound on the complexity of the image based on drawing speed of the stroke system to produce a flicker free display. The direct view storage tube (DVST) retains the image without the fast redraw requirement. However, the image cannot be manipulated and selectively erased without a complete redraw, thus making the DVST unsuitable for interactive designs. The raster scan conversion systems convert a vector into X, Y coordinates for display by a raster scan beam, therefore allowing a standard tube to be used. The complexity of the scan conversion circuits limits its popularity. The raster scan display technology uses the traditional television's approach and has been the dominant display technology used in most alphanumeric terminals. For graphics applications, a bit-mapped approach is used.

In a bit-mapped system, the image is made up of an X-Y matrix of picture elements (pixels) which are stored in a display memory commonly known as frame buffer. The image is refreshed one raster line at a time by turning on the appropriate pixel at the right time on the display. The widespread acceptance of bit-mapped graphics has been limited in the past due to the density/cost of RAM. Figure 2 depicts the dramatic shrinkage of memory component requirement for various screen size displays for a black and white display; for color, these numbers increase by a factor of 3 to 4. Thus, a 1024 x 1024 color display requiring thousands of chips in the early 70s takes only tens of chips today. An advantage of the raster scan bit-mapped display is that the refresh rate of the image is independent of the complexity of the image; whereas in vector systems, there is more chance that complex images might flicker since they take longer to be refreshed.

		Memory Size			
Screen Size	**Bits**	**1K's**	**4K's**	**16K's**	**64K's**
256 x 256	64K	64	16	4	1
512 x 512	256K	256	64	16	4
1024 x 1024	1M	1	256	64	16

Figure 2. Bit-Mapped Memory Requirements

INTERACTIVE

Bit-Mapped Design Approach

Bit-mapped displays range in applications from business graphics and office workstations to CAD/CAM and image processing. The performance requirements of a graphics system are determined by the needed resolution and the degree of real time interaction, or in other words, the amount of update and motion dynamics. Update dynamics is the ability to change color, shape or proportions of the displayed object, while motion dynamics is the ability to change the perspective between the object and the observer, perhaps by rotation, tumble or other movement. A bit-mapped graphics system has to **handle a large memory array**, especially when a color display is needed; a display with 1024 x 1024 spatial resolution and 16 colors requires 4 Megabits of storage. The frame buffer is often larger, to provide additional storage for multiple fonts, which vary in size and style, and display lists, containing host commands. A 1024 x 1024 picture, refreshed 30 times/second, requires one pixel to be read from the buffer and presented to the CRT, through video processing circuits, every 24ns. Interactive use means updating the display rapidly, even for some conceptually fairly simple operations. For example, an office automation display might contain windows of different text, much like papers on a physical desk. These windows can be individually scrolled, or can overlap and can be dragged across the screen. Updating such a display requires the manipulation of hundreds of thousands of pixels within one frame time. The upper limit is obtained by computing the bandwidth required to update the whole screen in one frame time. A smooth scrolling of a 1024 x 1024 screen requires a bandwidth of 60 Megabits/second because both a read and a write has to be performed for every pixel within 1/30 of a second. Therefore, an interactive bit-mapped graphics system needs *very high speed bit*

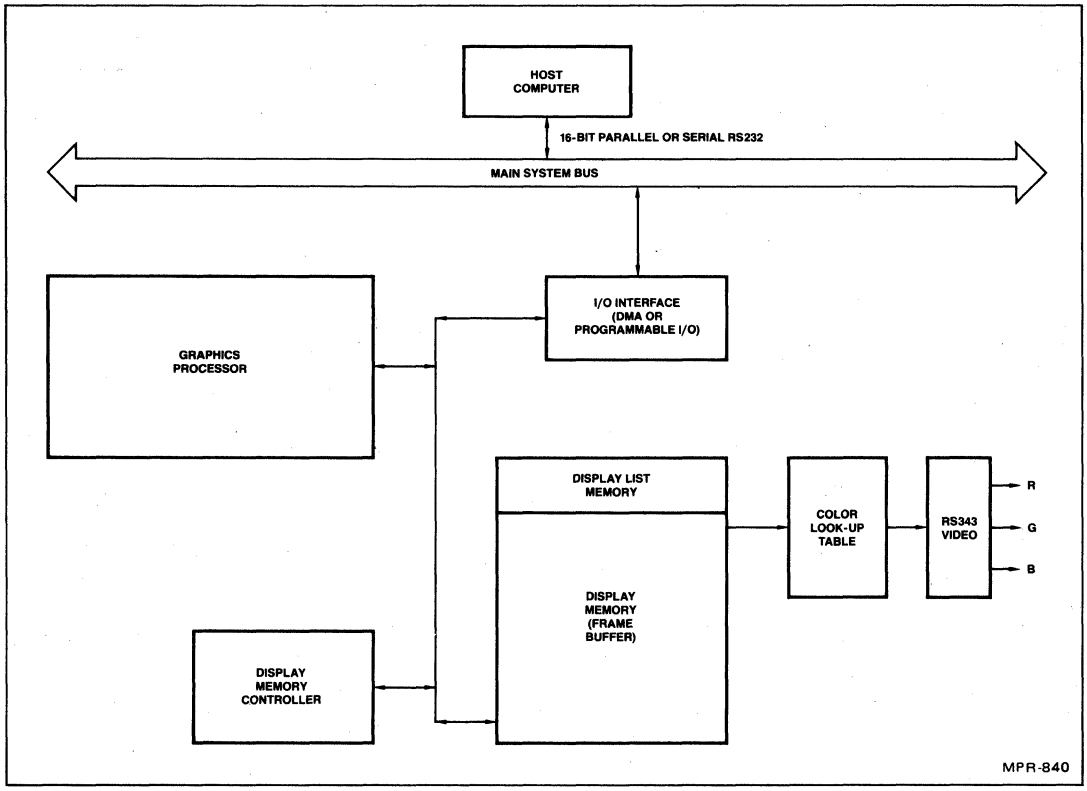


Figure 3. Intelligent Bit-Mapped Graphics Control Architecture

level data movement ability. These problems are solved by putting the appropriate capabilities in a high performance graphics processor, as shown in Figure 3, thereby offloading the host computer with some of the time consuming graphical operations. Commands, in the form of higher level program primitives, are sent by the host to the graphics processor through a display list memory. They are in turn interpreted by the graphics processor to perform the desired functions. Real time interaction also means that the graphics processor has enough intelligence to decode the course of action (update/ motion dynamics) without much intervention of the host. The display memory, also called frame buffer, is typically a 3 dimensional memory where the X, Y coordinates are the resolution (e.g., 512 x 512 or 1024 x 1024), and the Z coordinates contain intensities or colors (e.g., a 4 (8) plane frame buffer allows 16 (256) colors to be simultaneously displayed). Furthermore, the frame buffer outputs are usually connected to a color look-up table, allowing the choice of colors from the palette. For example, a look-up table with 3 channels, each with 8-bit outputs form a palette with 16.7 million colors.

The outputs of the color table are then converted to analog signals to drive the color video outputs. The display memory controler addresses the frame buffer and performs three functions – video refresh, video update and dynamic memory refresh. Video refresh requires the adjustment of the displayed image format at various update rates and the shifting out of the bit-map contents to the CRT fast enough to provide a flicker free display. Video update takes place during retrace blanking for writing information into the bit-map to modify the display. Memory refresh takes place at regular intervals to refresh the dynamic RAMs used to implement the frame buffer.

The graphics processor is the heart of the system. Some of the required functions and desirable features of a graphic processor are:

1. Direct addressing of the frame buffer memory so that rapid update is possible. Display generation and display list management should be performed interactively.
2. Powerful data movement and bit level manipulation capability such as drawing vectors, characters and filling polygons.
3. Real time response to conditional tests such as Horizontal sync, since pixels are drawn only during display retrace blanking in order to avoid memory contention.
4. Distributed intelligence to respond to the operator and update the display interactively without intervention of the host.
5. Microprogrammable so that the flexibility of meeting the requirements of various macro commands, instruction set primitives, and I/O interfaces is possible in firmware.
6. Built-in diagnostics to insure reliable operations and serviceability demanded by most systems.

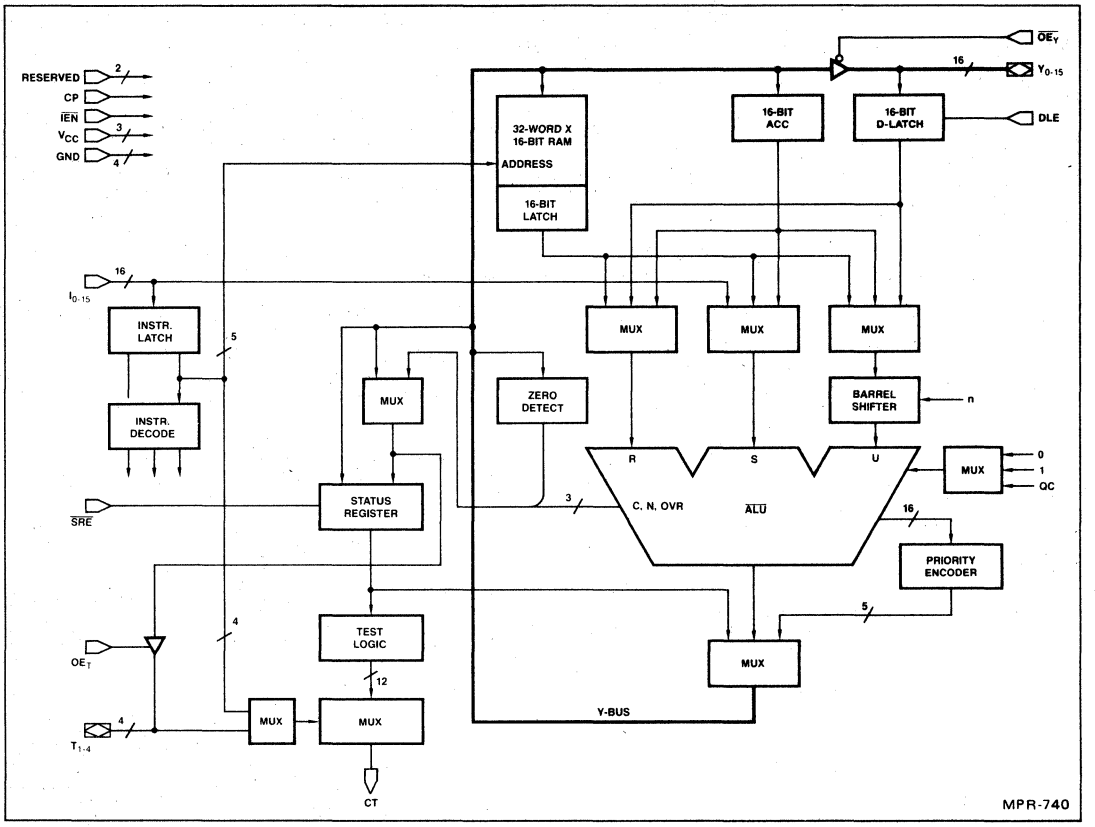


Figure 4. Am29116 Block Diagram

A very high performance, microprogrammable graphics controller can be implemented using a handful of Am2900 Family devices, the key member of which is the Am29116 16-bit microprocessor.

Am29116 ARCHITECTURE

The Am29116 is a powerful 16-bit microprocessor capable of supporting 100nsec microinstruction cycle time. It contains features particularly suitable for the rapid data movement and bit level manipulation necessary in bit-mapped graphics applications.

The Am29116 includes an on-chip 32 x 16 RAM with latched outputs, a 16-bit accumulator, a 16-bit priority encoder, a status register, a condition-code generator/multiplexer, 16 three-state output buffers and a 16-bit instruction latch and decoder (Figure 4).

The single-port RAM has output latches which are transparent when the clock input CP is HIGH and latched when CP is LOW. Data is written into the RAM while the clock is low if the $\overline{IEN}$ input is LOW and the instruction being executed selects the RAM as destination. Data is written into the low-order 8 bits of the addressed word for byte instructions. Separate read and write RAM addresses may be used by supplying a multiplexer on instruction inputs $I_4 - I_0$, using CP as the select signal.

The accumulator, which is edge-triggered, accepts data on the LOW-to-HIGH transition of CP if $\overline{IEN}$ is LOW and the instruction being executed selects it as the destination. As with RAM locations, byte instructions modify only the lower half of the accumulator, while word instructions modify the full register.

The data input latch (D-latch) holds the data input to the ALU on the bidirectional Y bus. The latch is transparent when the DLE input is HIGH and latched when the DLE input is LOW. The sources of the ALU operation are the RAM, the accumulator, the D-latch and the instruction inputs during IMMEDIATE instructions, and the 16-bit barrel shifter is one of the ALU inputs. This permits rotating source data up to 15 positions in both byte and word modes.

The ALU, which can operate on one, two, or three operands depending upon the instruction being executed, contains full carry lookahead across all 16-bits. All ALU operations can be performed in either word or byte mode. Status outputs Carry (C), Negative (N), and Overflow (OVR) are generated at the byte level for byte-mode operations and at the word level for word mode operations. A fourth flag, Zero (Z), is generated outside the ALU and also operates in either byte or word mode. The Stored Carry (QC) bit of the status register may be selected (along with 0 and 1) as the ALU carry input to support multi-precision arithmetic operations.

The Priority Encoder produces a binary-weighted code to indicate the location of the highest order ONE at its input. The input to the Priority Encoder is generated by the ALU which performs an AND operation on the operand to be prioritized and a mask. The mask determines the bit locations to be eliminated from prioritization. In the word mode, if no bit is HIGH, the output is a binary zero, if bit 15 is HIGH, the output is a binary one, bit 14 produces a binary two, etc. Finally, if only bit 0 is HIGH, a binary 16 is produced.

The 8-bit status register and the condition code generator/multiplexer contain the information and logic necessary to develop 12 condition-code test signals. The multiplexer selects one test signal and places it on the condition-code test (CT) output for use by the microprogram sequencer. The multiplexer is addressed in two ways. In the first, which is used to maximize throughput, the T-bus is used in input-only mode to specify the multiplexer select position directly. In the second, the CT output is selected through a test instruction.

The output enable Y-bus ($\overline{OEY}$) input enables the 16 three-state output buffers when it is LOW. When $\overline{OEY}$ is HIGH, the output buffers are put in the high-impedance state (allowing data to be applied to the D-latch from the controller's 16-bit data bus).

The 16-bit instruction latch is normally transparent to allow decoding of the 16 instruction inputs, $I_{15}-I_0$, into internal control signals for the Am29116, and the execution of the instruction within a single clock cycle. The only exceptions to this rule are the immediate-operand instructions, which execute in two clock cycles rather than one. These are captured in the instruction latch during the first clock and executed during the second. It is during the second clock that the immediate operand, which resides in the $I_{15}-I_0$ field of the next microinstruction, is fetched and execution is completed. Immediate instructions are useful whenever masks and special arithmetic constants are needed. (The Am29116 allows the addition or subtraction of 2^N, and the use of 2^N and its complement as a mask, for any N between 0 and 15 within a single clock, so that for these 16 common numbers and 32 common masks, an immediate instruction is not required).

Am29116 Instructions

The 16-bit instructions of the Am29116 can be grouped into eleven types, which correspond in a natural way with the Am29116's internal instruction decoding logic: single operand, two operand, single bit shift, rotate and merge, bit oriented, rotate by n bits, rotate and compare, prioritize, cyclic redundancy check, status and no-op. A system 29 AMDASM DEF file is available to provide the user with pre-defined mnemonics to microcode the Am29116.

For example, the AMDASM SRC file line

```
SOR    W,INC,SORY,R1
```

increments the full 16-bit contents of Am29116 RAM location 1 by one and places it onto the Y-bus and

```
TOR1   B,SUBR,TORAR,R2
```

subtracts the low-order byte of the accumulator from the low-order byte of RAM location 2 while leaving the high-order byte of location 2 unchanged.

Table 1 summarizes the basic operations that Am29116 instructions can perform within a single cycle. (Two cycles are used if one operand is immediate data.) Note that for a typical line of this table, there are several Am29116 mnemonic operation codes, depending upon the choice of operand source(s) and destination. Many of the operations prove particularly useful when implementing an intelligent graphics controller. For example, the manipulation of the arbitrary length, arbitrarily-aligned pixel data field is facilitated by the rotate and merge instruction. A 16-bit operand is rotated by N bits and combined with a second 16-bit operand under mask within a single cycle. The instructions which add and subtract 2^N, load 2^N and its complement, allows creation of commonly used masks in a simple and efficient manner. Inverse video, image exclusive OR'ed with background requires bit level set, reset and test instructions. Detecting edge boundary in polygon filling requires the prioritize instructions.

TABLE 1. SINGLE-CLOCK Am29116 OPERATION

Add
Add with Carry
Add 2^N
AND
Complement
Accumulate forward CRC
Accumulate reverse CRC
Exclusive NOR
Exclusive OR
Increment
Load 2^N
Load 2^N Complemented
Move
NAND
Negate (2's complement)
NOR
OR
Prioritize under mask
Reset bit N
Reset status bit
Rotate N bits
Rotate N bits and compare under mask
Rotate N bits and merge according to mask
Set bit N
Set status bit
Single bit shift
Subtract
Subtract with Carry
Subtract 2^N
Test bit N
Test status bit

Am29116 BASED BIT-MAPPED SYSTEM ARCHITECTURE

Figure 5 is a simplified system block diagram of the Am29116 based bit-mapped graphics processor, and shows all of the required function and desirable features previously discussed. The Am29116 provides the capability of drawing graphics primitives into the frame buffer at high speed with minimal host computer involvement. The processor can draw vectors, characters and fill polygons at the rate of one pixel every 100nsecs, with an average drawing speed of 2 million pixels per second.

The microprogrammed graphics processor contains a control section and a data path section. The control section consists of a microprogram sequencer (Am2910A) to produce the next microprogram address for the registered control memory (Am27S35), and ALU status flags, horizontal sync and other system test conditions are examined by the sequencer to determine the program flow. The macro commands are stored in some sort of display list memory and are interpreted by the sequencer. These commands are downloaded from the host

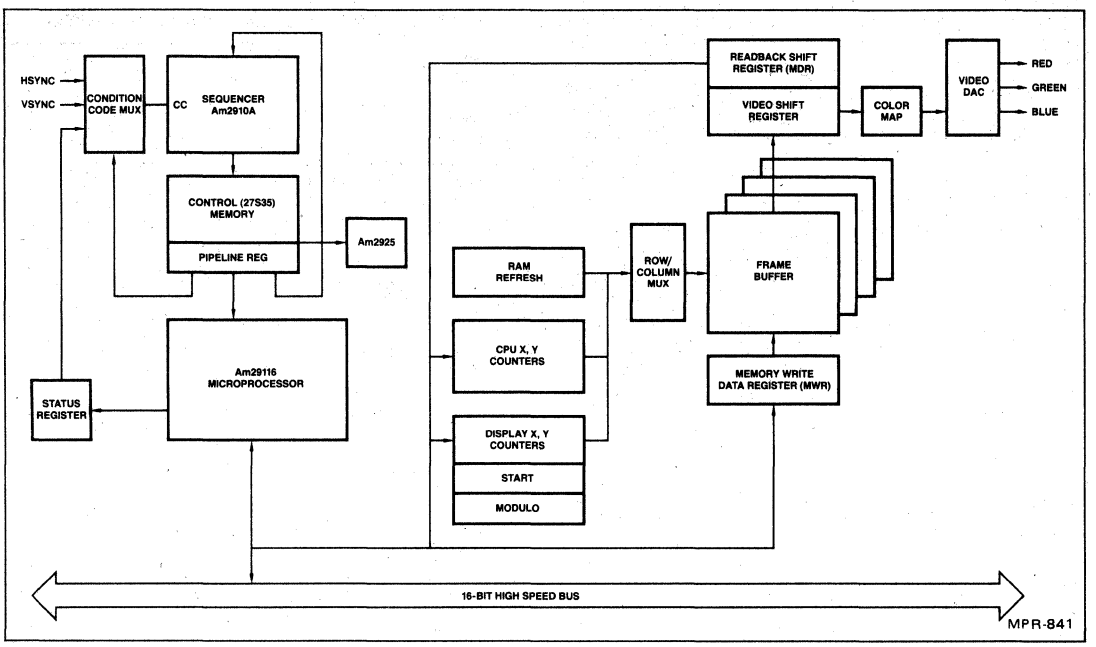


Figure 5.

CPU through either programmed I/O or a DMA interface, readily implemented using the Am2940 DMA address generator and the Am2950 parallel I/O data port.

The display controller consists of three sections: dynamic memory refresh, video update and video refresh. Video update occurs during retrace blanking and is accomplished by writing pixels into the locations pointed to by the CPU X, Y counters. There is also a memory write data register (MWR) for the Am29116 so that the Am29116 does not have to wait a full memory cycle during write. Video refresh is performed through the display X, Y counters with logic for automatic starting address reload. The frame buffer data is sent to a video shift register, and in conjunction with the color look-up table allows 16 colors to be displayed simultaneously from a palette of 16.7 million. There is also a readback path for the frame buffer data to be examined by the Am29116. The architecture shown uses one Am29116 to control multiple bit planes. There is associated with the display memory a write mask register which functions with the pattern circuitry in selectively modifying individual memory planes. The Am29116 is the heart of the system, providing the intelligent, high performance, high resolution color graphics capabilities through its controller oriented architecture and instruction set optimized for data movement and bit manipulation.

GRAPHICS OPERATIONS

The architecture of the Am29116 is ideally suited for implementing the primitive graphics operations necessary in a bit-mapped graphics processor. An example of a graphics processor instruction set (courtesy of Metheus) is given in Table 2. Most operations reference two pointer registers (P_1 and P_2) resident in the graphics processor. For example the command MOV_{P1} X, Y will load P_1 with the bit location specified by X, Y. The DRAW instruction will draw a line between P_1 and P_2.The use of these two dedicated registers reduces the number of bits necessary to define an instruction; this allows the graphics processor to be easily interfaced to any 16-bit microprocessor bus, either as an I/O port or via DMA operation.

DEFINE POINT

The most primitive graphics operation draws an individual point on the display, and when iterated, can be used to build more complex structures. Graphics structures such as lines, rectangles and polygons can be constructed out of individual points, and characters can also be drawn by plotting individual points using a technique similar to that used by dot matrix displays and printers. Additionally some of the more complicated algorithms require individual points to be added or removed. For example, line smoothing techniques (anti-aliasing) require individual points to be added adjacent to some lines to minimize their jagged appearance.

The algorithm for drawing a point on the display is a single address translation operation. The display processor is given the point in the form of an absolute coordinate (addresses relative to the cursor registers P_1 and P_2 are possible also, and easily implemented by computing an absolute address) on the display memory and must map that bit location into the bit-map memory. This logical-to-physical-address mapping is required because 1K by 1K logical display memory is actually implemented with 16 bits of 64K memory chips.

Figure 6 shows the two memory organizations, and the different address formats. The translation operation simply takes the two 10-bit addresses and generates a 16-bit word address and the 4-bit bit address.

As shown in Figure 7, the rotate and merge instruction can be used to construct the new 16-bit word in two cycles. The first cycle left-justifies the 10-bit Y address by rotating it up 6 bit

TABLE 2. DISPLAY CONTROLLER INSTRUCTION SET

Initialization
INIT – reset and initialize

Display Pointer Move
MOVP1 x,y – move pointer 1 to x,y
MOVP2 x,y – move pointer 2 to x,y
RMOVP1 dx,dy – relative move pointer 1 by dx,dy
RMOVP2 dx,dy – relative move pointer 2 by dx,dy
POLYS – begin polygon define
POLYV x,y – add polygon vertex

Drawing Commands
DRAW – vector draw
CHAR – draw character at P1
ARC n – draw arc or circle using center P1 and initial point P2; arc length or circle circumference is n pixels
RECT-1 – outline rectangle defined by P1 and P2
RECT-2 – fill rectangle defined by P1 and P2
FFILL – FLASH-fill of rectangle defined by P1 and P2
CLEAR – clear image memory (also clear or set individual planes)
POLYF – polygon fill
POLYO – outline polygon
AFILL-1 – random area "seed" fill
RLFILL n – runlength fill from P1

Drawing Control Commands
SETD d – set drawing data register
SETM d – set drawing mask register
PATT d – select drawing pattern and mode
SETC-1 d – select character size
SETC-2 d – select character rotation and mirror

Display Control Commands
ZOOM d – select horizontal and vertical zoom factors
PPAN x,y – pan to origin at x,y
CMAP a,d – load color map address a with data
BLNKON – turn on blink mode
BLNKOF – turn off blink mode

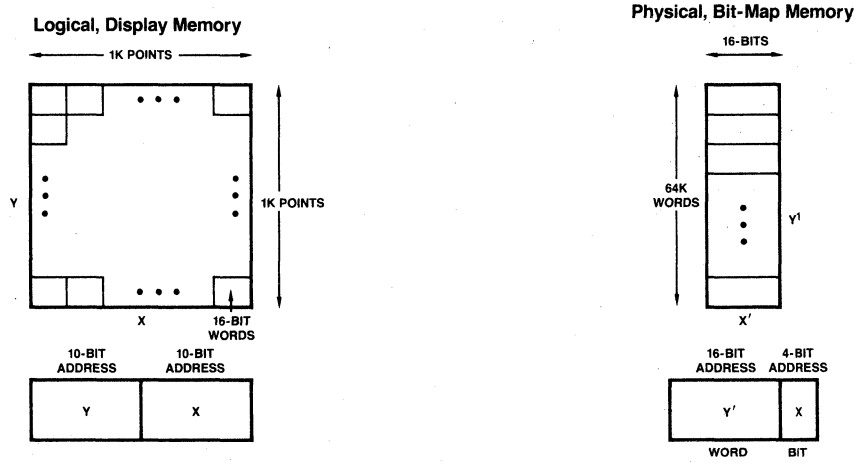
Data Transfer Commands
WRR d . . . – block write rectangle defined by P1 and P2
RDR – block read rectangle defined by P1 and P2
PIXBLT w,h,f – block pixel move from P1 to P2 of rectangle of width w, height h and direction f
READP – read pixel color at P1
WRITEP c – write pixel at P1 in defined color

Cursor Commands
CURS – enable cursor display at P1

Utility Commands
CRCRD – read CRC data register
SYNCH – wait for vertical retrace (for animation)
READC – reads hardware configuration and microcode version

6

Courtesy Metheus



MPR-842

Figure 6. Memory Organization and Address Translation

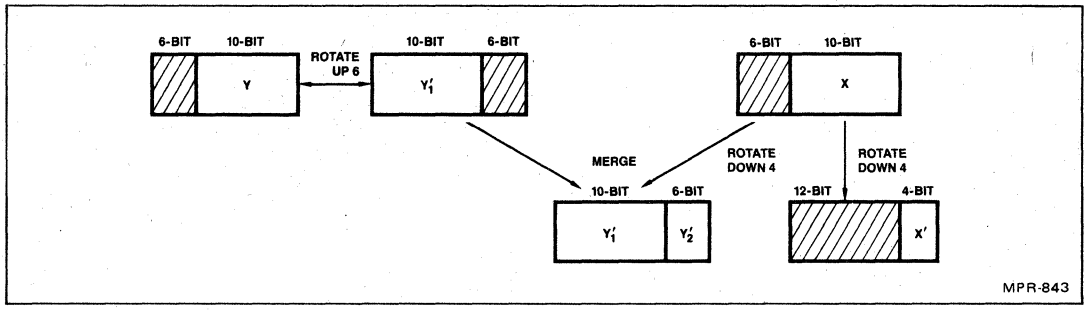


Figure 7. Simplified Am29116 Graphics Processor System Diagram

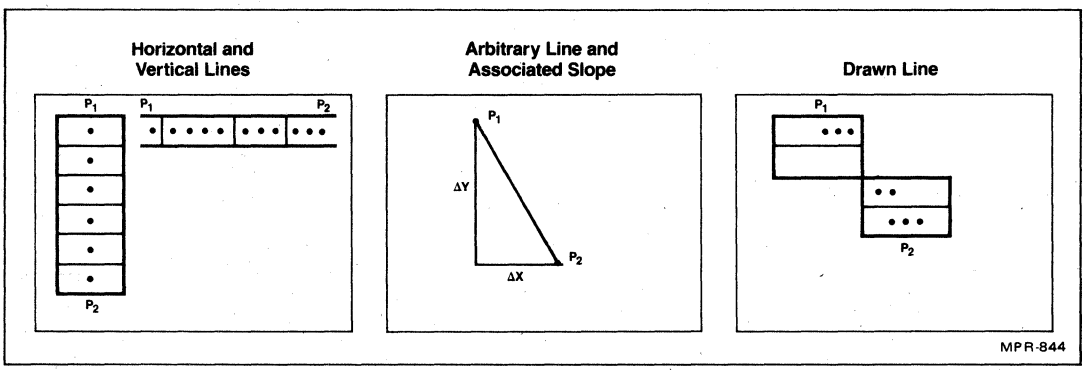


Figure 8. Line Draw Operation

positions. The upper 6 X address bits are then rotated down, and merged onto the 6 vacant bit positions to form the desired 16-bit quantity. The remaining task of setting a single bit in the 16-bit word can be easily accomplished by reading the word from the display memory and using the set 2^N instruction, with the 4-bit X_1 quantity as the index (either thru a jump table, or via an N bit register). The modified word is then written back resulting in the desired bit being set in the display. Alternate implementations could do the mapping in hardware, but would be more difficult to change when upgrading memory. As seen in Figure 8, a horizontal line can result in 2 main cases: end points inside the 16-bit word, and zero or more words separating end points. In the first case the bits between P_1 and P_2 must be set. This can be accomplished in the Am29116 by first setting all the bits above P_1 and then resetting the bits above P_2. These operations can be easily implemented in the Am29116 by generating a mask word (either in microcode or hardware) to allow setting or resetting of the upper or lower bits of a word. The multiple word horizontal line can be handled by using the set instructions on the lower word, selectively setting all whole words (if any) between P_1 and P_2, and finally setting all bits below P_2.

Vertical lines are very easy. The lower 4 bits of the address specify which bit in the 16-bit word is to be set; this operation is then iterated over the range between Y_1 and Y_2. The set 2^N operation in the Am29116 is ideal.

A more complicated situation exists when P_1 and P_2 are not orthogonal. In this situation a slope exists between P_1 and P_2 (Y/X), and it is necessary to calculate the succession of points needed to draw the line. Calculation of the slope requires a divide operation, a 10-bit divisor and a 20-bit dividend with a 10-bit quotient.

Once the slope is calculated the line drawing algorithm uses successive add operations to compute dot locations. The X location is incremented by 1, and the Y location by the slope (the Y location count is a 20-bit count to allow for the worst case slope of 1/1024). As long as the upper 10 bits of the Y counter don't change, the dot at the X location is set. When the upper 10 bits of the Y counter increment, the word is written into memory and the next word fetched. This algorithm terminates when P_2 is set.

The Am29116 contains all the resources and instructions necessary to implement the line drawing algorithm. The slope divide can be implemented in the Am29116 as a succession of subtract and shift operations; at 4 cycles per bit and 20 bits this will take about 80 cycles (at 100ns per cycle, this is only 8 microseconds). The slope only needs to be computed once per line, and can be overlapped with the memory access time, resulting in almost no overhead.

The 20-bit counter can be implemented with 2 of the 32 16-bit scratch pad storage registers. The increment with carry instruction is used to cascade to a 20-bit address. More complicated draw instructions are possible, and one that is very useful is the draw rectangle instruction. It uses P_1 and P_2 to define a rectangle, and implementation is easy when the draw horizontal and draw vertical line instructions are implemented.

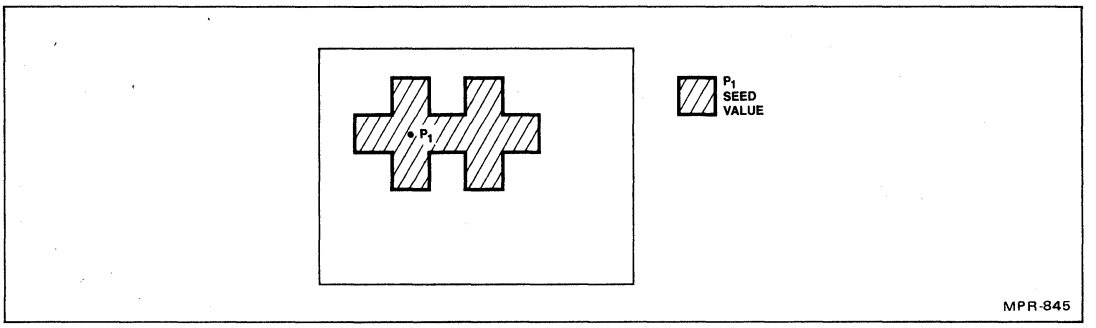


Figure 9. Polygon Fill Operation

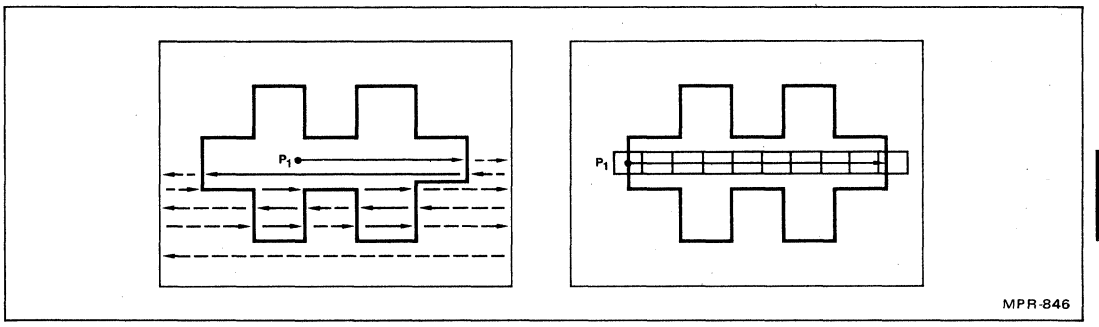


Figure 10. Polygon Fill Algorithm

The locations of intermediate points A and B can be computed and calls to the appropriate horizontal or vertical line drawing routines executed.

FILL OPERATIONS

One of the more complicated graphics functions is the FILL operation. This operation is used to replace the inside of a closed figure with a new value. Figure 9 illustrates how the FILL command, FILL POLYGON, would work. FILL POLYGON (P_1) would replace the POLYGON enclosing P_1 with the seed value. This operation is used most often to "highlight" a particular structure of the display. For example, in a VLSI CAD system, a polygon might represent a particular diffusion pattern or metalization layer. Different areas need a different pattern or color to make it easy for the designer to distinguish one structure from another.

Nothing more than an interior point needs to be specified for the FILL POLYGON command. The algorithm is smart enough to figure out all internal points (or conversely all exterior points). The advantage of moving this intelligence to the drawing processor is a reduction in the host overhead. The host contains all the logical information about the polygon (verticles, line segments, etc.) in the figure data base. Computation of all the interior (or exterior) points from this information is possible, but the drawing processor can implement it much quicker by accessing the raw data and processing it. This is the main reason for the migration of intelligence from the process or to peripherals. In many cases a small amount of intelligence located at the data can provide sufficient processing capability to dramatically reduce the overhead on the central processor.

POLYGON FILL ALGORITHM

As illustrated in Figure 10 the algorithm consists of scanning from the seed point (P_1) to the edge of the display (or alternately an enclosing rectangle, bounded by X and Y in Figure 10). Each time a line is crossed, the inside-flag is toggled, indicating a change from inside to outside or vice versa. (This is a topological tautology. Everytime a line of a closed figure is crossed the point changes from being enclosed to being outside, or from being outside to being inside). This is terminated when a line contains no inside portion. Once the "bottom" is detected, a scan from P_1 is generated upwards until a "blank" line is encountered. These two scans result in a completely filled polygon.

The Am29116 contains two special instructions which make it easy to implement the POLYGON FILL operation. The priority encode instruction and the N bit set instruction combine to implement a set-to-boundary primitive which can be used to construct the FILL POLYGON instruction. The set-to-boundary instruction takes a starting point and sets all elements to the right of the point (or left, depending on the direction specified) until a boundary is discovered. The words are fetched in 16-bit increments. The priority encode instruction will return a value associated with the location of the first non-zero bit in the word. If no 1 is discovered the entire word is set and written to the display memory. The next word is read and the process is repeated until a 1 is discovered, at which time the output of the priority encoder indicates the address of the bit. The set instruction can then be used to set all bits up to the addressed bit. Once a perimeter point is discovered the inside/outside flag

is toggled. Outside the polygon, a search-to-boundary instruction is used to find the next boundary (it terminates on the display boundary). This instruction is a simple modification to the set-to-boundary instruction; the set operation is deleted.

BIT BLOCK TRANSFER (BITBLT)

One powerful basic operation commonly used in graphics involves the manipulation of a rectangular array of bits. Typically, the bit block transfer (BITBLT) operation accesses bits from a source rectangle, performs a function on them, and stores the result in the destination rectangle. Figure 11 illustrates a possible configuration of the source and destination rectangle, embedded in separate bit maps. Successive bit pairs are taken from the source and destination bit stream respectively. The operation is iterated over all corresponding pixels of width W, and repeated again on a line by line basis to height H.

The BITBLT operation can be used to implement various functions. For example, the frame buffer memory is generally larger than the visible screen, and the invisible parts typically contain libraries of character fonts, menus, and various symbols. The particular text and symbols can be displayed by being specified as the source rectangle for the BITBLT operation, and moved to any part of the screen. Similarly, windows can be scrolled smoothly by copying them to the new location and clearing the reclaimed area.

To implement BITBLT effectively, parallel bits of data need to be accessed from and stored to the frame buffer memory. However, the source and destination rectangles can lie anywhere within the frame buffer and they are often not located conveniently along the arbitrary word boundaries. If it is necessary to write 16 non-aligned pixels into the frame buffer memory, the write might have to be split up as two separate writes into adjacent words of memory. The inner loop of BITBLT reads 16 bits from the source and destination rectangles, operates on them and writes the result back to the destination. Neither of these rectangles need to be word-aligned; however, by handling the end conditions appropriately, the inner loop can be modified such that the destination word is aligned with the word boundary; the source can be across two words, as shown in Figure 12. A 16-bit object is extracted from two adjacent words of the source rectangle and combined with the destination word to form the result. The two source words have to be rotated to allow the extraction of the desired 16 bits; the rotation count is the alignment difference between the source and destination rectangles. The two rotated words are then masked and combined to yield the destination word. The rotate count and required mask can be precomputed for each BITBLT operation.

Figure 13 illustrates an often used BITBLT variation – copy and the corresponding inner loop implemented by the Am29116. The mask is precomputed and stored in RAM_0 of the Am29116. The rotate count, r, is also precomputed. It can be stored in an external N-register for instruction modification of the rotate instruction, or alternatively, the precomputed rotate count can be used as an index to a branch table with 16 separate instructions for each appropriate rotate count. Here, the tradeoff is between cycle time (having an N-count register externally will add a multiplexer stage delay to the Am29116 instruction path) and control memory (since each inner loop has to be repeated 16 times in memory with different rotate count). While the inner loop takes only three microcycles and two Am29116 microinstructions, two memory cycles from the frame buffer memory (one read and one write) are performed. The Am2925 can be used to stretch the microinstruction cycles during these times, or a frame buffer memory with a higher bandwidth can be designed to allow the inner loop to proceed at maximum speed.

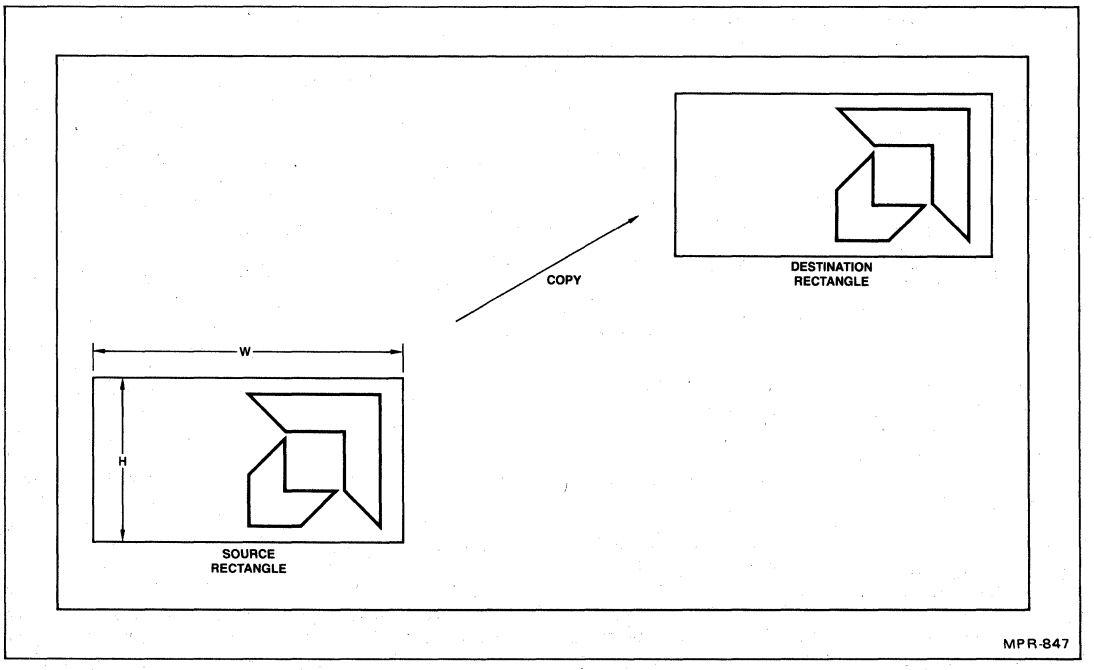


Figure 11. BITBLT Operation

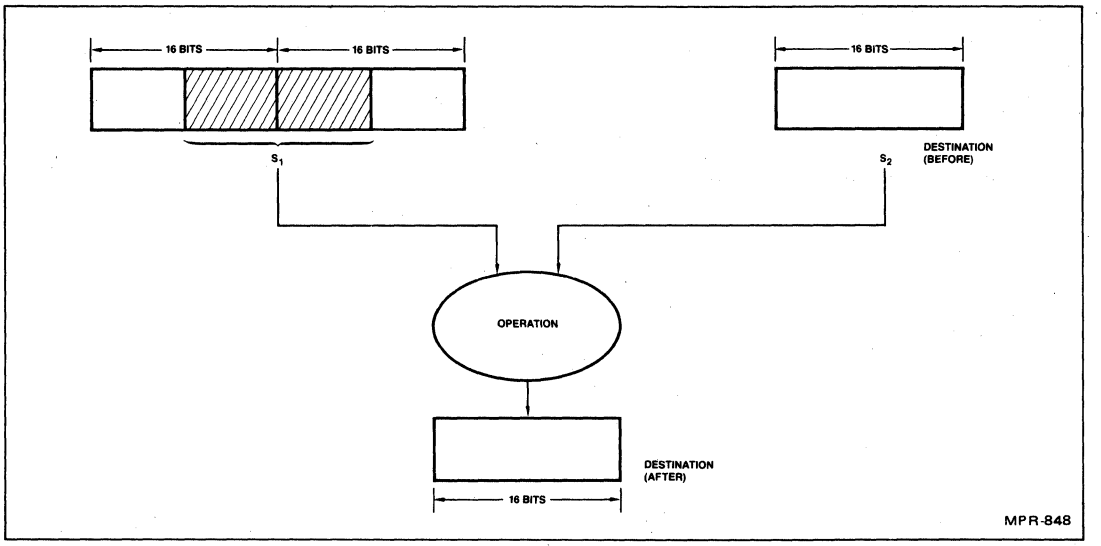


Figure 12. Modified Inner Loop of BITBLT

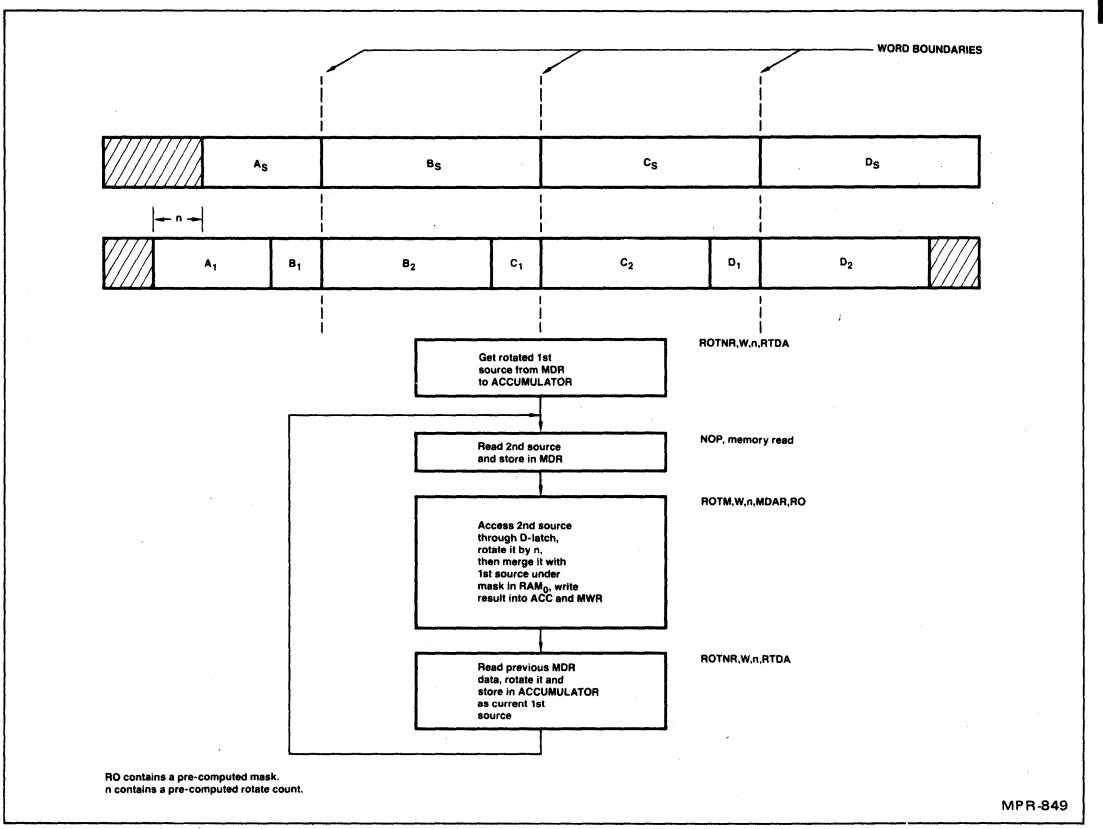


Figure 13. Inner Loop of Copy Operation

ADDITIONAL OPERATIONS

More complex operations can be implemented with the same primitives discussed previously. Polygon rotation allows a graphics object to be positioned in any orientation. For example, in a Computer Aided Design environment for mechanical equipment, a metal plate could be defined, then placed with a different orientation on the assembled structure. Windowing opens a viewport on the display to show a portion of a different diagram. This allows many multiple displays to be shown on the screen at a time, as in Defender, where a window showing a global, strategic view is placed above the more detailed tactical display. Finally zoom (magnification of a section of a display) and pan (moving a window to select a view from a larger display) allow the user greater flexibility in large graphics environments.

Up to this point the discussion has been limited to two dimensional graphics objects. The extension to three dimensional objects requires additional number crunching capabilities, and a hardware multiplier is necessary. The Am29116 combined with the Am29516/517 16-by-16 multiplier will allow some three dimensional graphics operations to be implemented. Three dimensional rotation algorithms are very multiply intensive and the 65ns multiply time of the Am29516/517 is fast enough to do the necessary calculations in real time. Two dimensional projections of three dimensional objects are also very useful in Computer Aided Machining applications, but are also very multiply intensive and the hardware multiply capability is a necessity in an interactive environment.

Am29118

Eight-Bit Am29116 I/O Support

DISTINCTIVE CHARACTERISTICS

- Reads both registers on A-port
- Noninverting outputs
- Eight-bit bidirectional I/O port
- Separate clock, clock enable and three-state output enable to synchronize data between two bidirectional buses
- 24mA output current sink capability
- 24-pin slim package
- Additional accumulator to support certain Am29116 applications

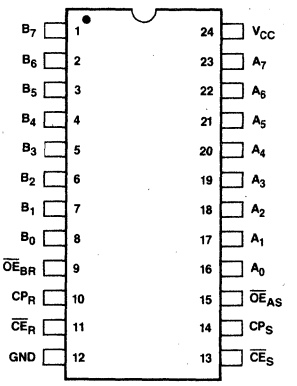
GENERAL DESCRIPTION

The Am29118 is an eight-bit wide bidirectional parallel data input/output port designed to provide an additional accumulator when used with the Am29116 or with any microprocessor with single bidirectional data port. In addition, it can be used as a parallel data input/output port, like the Am2952. The Am29118 is a metal mask option of the Am2952A, and so requires no additional pins to support the Am29116 input/output structure.

RELATED PRODUCTS

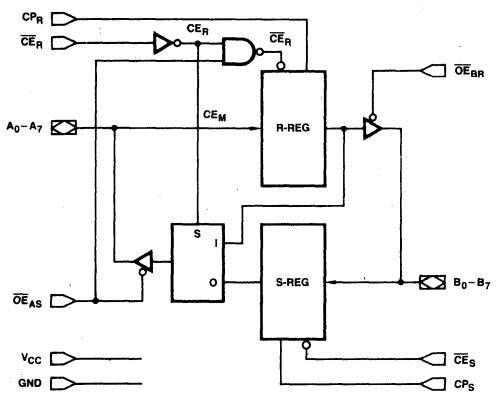
Part No.	Description
Am29116	High Performance 16-Bit Bipolar Microprocessor
Am2910A	Microprogram Controller
Am2914	Vectored Priority Interrupt Controller
Am2925	System Clock Generator and Driver
Am2940/2	DMA Address Generator
Am2950-3	8-Bit Bidirectional I/O Ports
Am29800 Family	High Performance Bus Interface

CONNECTION DIAGRAM
Top View



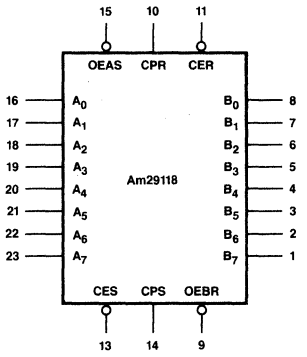
Note: Pin 1 is marked for orientation.

Figure 1. The Am29118 Block Diagram



$\overline{OE}_{AS}$	$\overline{CE}_R$	Function
0	0	Read R, Disable CP_R
0	1	Read S, Disable CP_R
1	0	Enable CP_R
1	1	Disable CP_R

LOGIC SYMBOLS



FUNCTIONAL DESCRIPTION

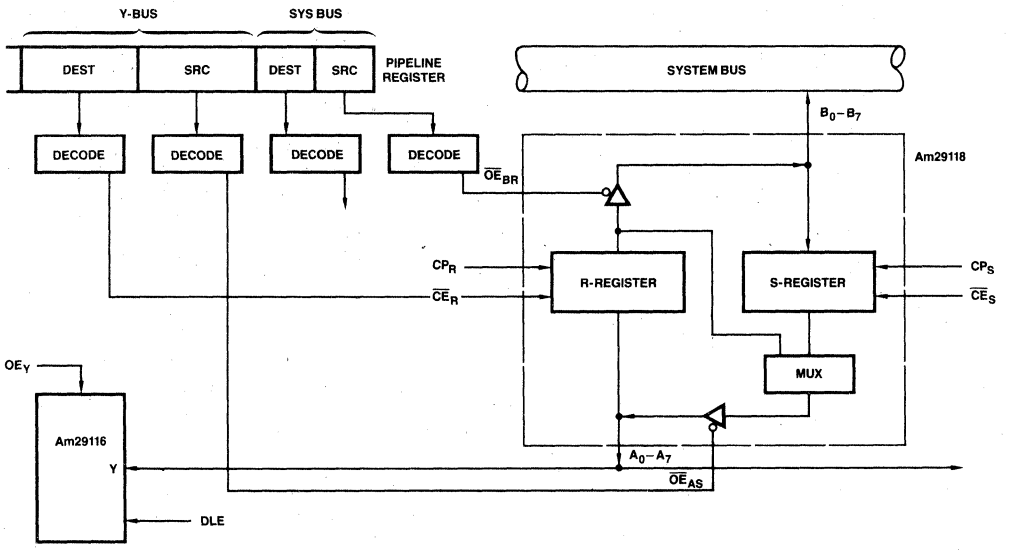
The Am29118 has two eight-bit wide registers (R-Register and S-Register) connected back to back for moving data in both directions between two buses. The R-Register serves the dual purpose of transmitting data from one bus (device's internal bus) to another (system bus), and serving as an additional accumulator for the Am29116.

The accumulator function is implemented by allowing the A-port to provide read and write data from the R-Register and read data from the S-Register; the B-port provides read data for the R-Register and write data for the S-Register (similar to the Am2952). This additional function in the Am29118 is implemented with a two-input multiplexer, as shown in Figure 1. Each register has an individual clock (CP_R and CP_S), a Clock Enable, ($\overline{CE}_R$ and $\overline{CE}_S$), and a three-state Output Enable ($\overline{OE}_{AS}$ and $\overline{OE}_{BR}$). The clock enable signal for the R-Register ($\overline{CE}_R$) and the Output Enable Signal for the S-Register ($\overline{OE}_{AS}$) are encoded to make the R-Register an accumulator, in addition to all the Am2952 functions as shown in Table 1. Because of this encoding, transferring data from the S-Register to the R-Register is not permissible.

TABLE 1.

$\overline{OE}_{AS}$	$\overline{CE}_R$	Function
0	0	Read R, Disable CP_R
0	1	Read S, Disable CP_R
1	0	Enable CP_R
1	1	Disable CP_R

Figure 2. System Configuration



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) under Bias	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5 to +V_{CC} MAX
DC Input Voltage	−0.5 to +5.5V
DC Output Current, into Outputs	
DC Input Current	

OPERATING RANGE

Part Number	Range	Temperature	V_{CC}	
Am29118DC	COM'L	T_A = 0 to +70°C	V_{CC} = 5.0V ±5%	(MIN = 4.75V, MAX = 5.25V)
Am29118DM	MIL	T_C = −55 to +125°C	V_{CC} = 5.0V ±10%	(MIN = 4.50V, MAX = 5.50V)

Am29118
DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions			Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	A_{0-7}, B_{0-7}	MIL, I_{OH} = −2mA				Volts
				COM'L, I_{OL} = −6.5mA				
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	A_{0-7}, B_{0-7}	MIL, I_{OL} = 16mA				Volts
				COM'L, I_{OL} = 24mA				
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs						Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs						Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA						Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V		A_{0-7}, B_{0-7}				μA
				Others				μA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		A_{0-7}, B_{0-7}				μA
				Others				
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V						mA
I_O	Output Off-state Leakage Current	V_{CC} = MAX	A_{0-7}, B_{0-7}	V_O = 2.4V				μA
				V_O = 0.4V				
I_{SC}	Output Short Circuit Current	V_{CC} = MAX						mA
I_{CC}	Power Supply Current	V_{CC} = MAX		T_A = 25°C				mA
			COM'L	T_A = 0 to +70°C				
				T_A = +70°C				
			MIL	T_C = −55 to +125°C				
				T_C = +125°C				

SWITCHING CHARACTERISTICS

The tables below define the Am29118 switching characteristics. Tables A are setup and hold times relative to a clock LOW-to-HIGH transition. Tables B are propagational delays. Tables C are pulse-width requirements. Tables D are enable/disable times. All measurements are made at 1.5V with input levels at 0 or 3V. All values are in ns with R_L on A_i and B_i = 220Ω and R_L on FS and FR = 300Ω. C_L = 50pF except output disable times which are specified at C_L = 5pF.

GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE

(T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25V, C_L = 50pF)

A. Setup and Hold Times

Input	With Respect to	t_s	t_h
A_{0-7}	CPR ↓		
B_{0-7}	CPS ↓		
$\overline{CE}_S$	CPS ↓		
$\overline{CE}_R$	CPR ↓		

B. Propagation Delays

Input	A_{0-7}	B_{0-7}
CPS ↓		
CPR		

C. Pulse-Width Requirements

Input	Min LOW Pulse Width	Min HIGH Pulse Width
CPS		
CPR		

D. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}_{AS}$	A_{0-7}		
$\overline{OE}_{BR}$	B_{0-7}		

GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE

(T_C = −55 to +125°C, V_{CC} = 4.5 to 5.5V, C_L = 50pF)

A. Setup and Hold Times

Input	With Respect to	t_s	t_h
A_{0-7}	CPR ↓		
B_{0-7}	CPS ↓		
$\overline{CE}_S$	CPS ↓		
$\overline{CE}_R$	CPR ↓		

B. Propagation Delays

Input	A_{0-7}	B_{0-7}
CPS ↓		
CPR ↓		

C. Pulse-Width Requirements

Input	Min LOW Pulse Width	Min HIGH Pulse Width
CPS		
CPR		

D. Enable/Disable Times

From	To	Disable	Enable
$\overline{OE}_{AS}$	A_{0-7}		
$\overline{OE}_{BR}$	B_{0-7}		

Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5−8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

APPLICATIONS

In the Am29116 system, there is only one I/O port available for data communication with the ALU. In such a system, the Am29118 acts as an additional accumulator (temporary storage) to increase performance, and also provides capability of a bidirectional I/O port (like the Am2952).

Figure 2 shows the connections necessary for the Am29118 to be used as an accumulator as well as a bidirectional I/O port. The A-port is connected to the Y-bus (internal bus) of the Am29116, and B-port is connected to the system data bus. Four microcode bits are used for source and destination control for the Y-bus and the system data bus. Figure 3 shows the timing waveforms to modify an accumulator (R-Register) in two microcycles. During the first cycle, data is read from the R-Register, modified in the Am29116 and stored in one of the internal registers. A two-address architecture is required if the second operand to modify the R-Register is in one of the RAM registers, and the result has to be stored in another RAM register. For stable operation, data from the R-Register is latched in the D-Latch halfway through the clock during the first cycle. The instruction is executed and the result stored into a scratchpad register. In the second cycle, data is moved from the internal result register to the R-Register of the Am29118. Figure 4 shows the timing waveforms to modify an accumulator (R-Register) in a single microcycle. In the first half of the cycle the source register is enable on the Y-bus into the D-Latch of the Am29116. The D-Latch is transparent during the first half of the cycle. In the second half of the cycle, data is latched in the D-Latch and the bus source is disabled. During the second half of the cycle, the output buffer of the Am29116 is enabled to bring the result on the Y-bus to be loaded into the destination. These two techniques provide different advantages and disadvantages to modify the external accumulator using the Am29116. The first technique (Figure 3) takes two microcycles but allow a shorter microcycle time. The second technique (Figure 4) takes only one microcycle but needs a longer microcycle time. There is also a requirement for the system bus to transfer data as input to the Am29116. The S-Register is used in this case to receive data from the system bus (like the Am2952).

Figure 3. Timing Waveforms for Modifying R-Register in Two Microcycle using the Am29116

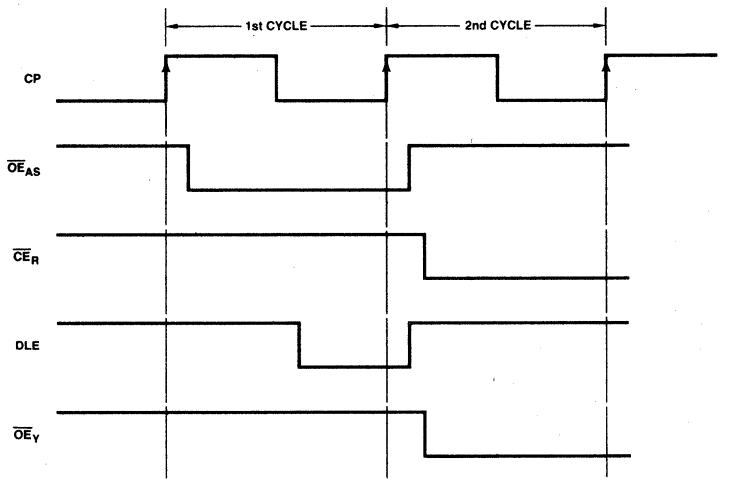
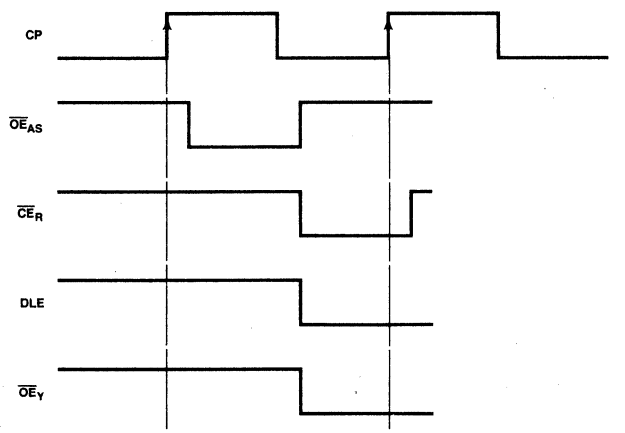


Figure 4. Timing Waveforms for Modifying R-Register using the Am29116



ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Am29118 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM29118DC	D-24	C	C-1
AM29118DC-B	D-24	C	B-2 (Note 4)
AM29118DM	D-24	M	C-3
AM29118DM-B	D-24	M	B-3
AM29118XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM29118XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to 70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 96 hour burn-in.

METALLIZATION AND PAD LAYOUT

Am29500
Array Processing and
Digital Signal Processing Index

The Am29500 Family

A New High-Performance Architecture for Digital Signal/Array Processing

The new system designs of the '80s will continue to press the performance limits of technology. Parallel processing and pipelined architectures will become the standard approach. The new architectures are best implemented with a chip set that has been designed from the ground up with high speed array processing in mind.

The Am29500 Family is designed specifically for these new architectures. Every key product feature supports the system end objective of maximum performance and flexibility. These include:

- Microprogrammable, parallel functions
- Pipelined organization used throughout
- IMOX™ process and ECL internal structures
- TTL I/O for easy interfacing

The first members of the family are targeted for the efficient execution of DSP and array processing algorithms. The most common include Infinite Impulse Response (IIR) and Finite Impulse Response (FIR) digital filters and Fast Fourier Transform (FFT) processors.

The first major building blocks are designed to support maximum performance signal processing applications.

Included are:

- **Am29501 Multi-Port Pipelined Processor**

  A specialized parallel processor which executes multiple simultaneous data operations. Its Register/ALU structure provides the key functional element for a high performance signal processing system. Eight-bit slice!

- **Am29540 FFT Address Sequencer**

  This algorithm-specific VLSI chip generates data and coefficient addresses for the Fast Fourier Transform. It supports a wide variety of FFT algorithms in either radix-2 or radix-4.

- **Am29516/29517 High Speed 16 x 16-Bit Parallel Multipliers**

  Both are 16 x 16-bit Parallel Multipliers. The Am29516 is pin and functionally compatible with the MPY-16HJ, but with an added multiplexer to output the LSP at the MSP port. The Am29517 is the same function, but with clock enables for microprogrammed applications.

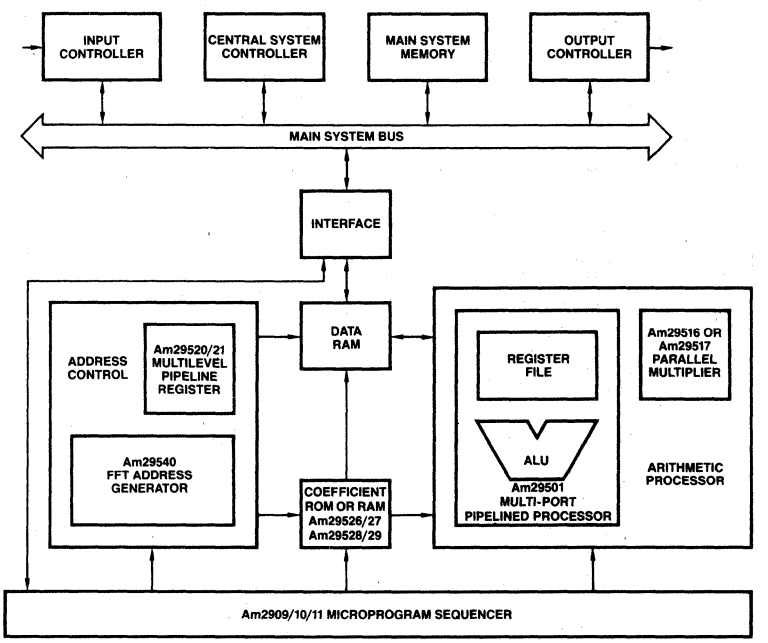
- **Am29520/29521 Multilevel Pipeline Registers**

  Both devices contain four 8-bit registers for dual two-stage (FFT butterfly) or single four-stage (general purpose) data or address pipelining. Combined load-and-shift (Am29520) or separate load-and-shift (Am29521) control options are available.

- **Am29526/29527/29528/29529 High-Speed Sine/Cosine Function Generators**

  The sine and cosine functions are necessary for Fast Fourier Transforms (FFT). The Am29526/527 generate the most significant and least significant byte of the 16-bit sine function and the Am29528/529 generate the most significant and least significant byte of the 16-bit cosine function. The sine and cosine functions are generated to provide a range of θ for a half cycle, $0 \leq \theta \leq \pi$, in increments of $\pi/2048$. All four units have a 50ns maximum commercial generation time.

HIGH PERFORMANCE SIGNAL PROCESSOR



MPL-025

7

A high-performance signal processor may be constructed as shown in the diagram. The processor is built entirely with new Am29500 digital signal processing and Am2900 devices. Such a processor is attached as a slave to the main system bus to perform the multitude of arithmetic operations which prevail in DSP algorithms.

Using this architecture it is possible to implement a radix-2FFT butterfly in four instruction cycles. This allows a 1024-point complex FFT to be performed in approximately 2ms.

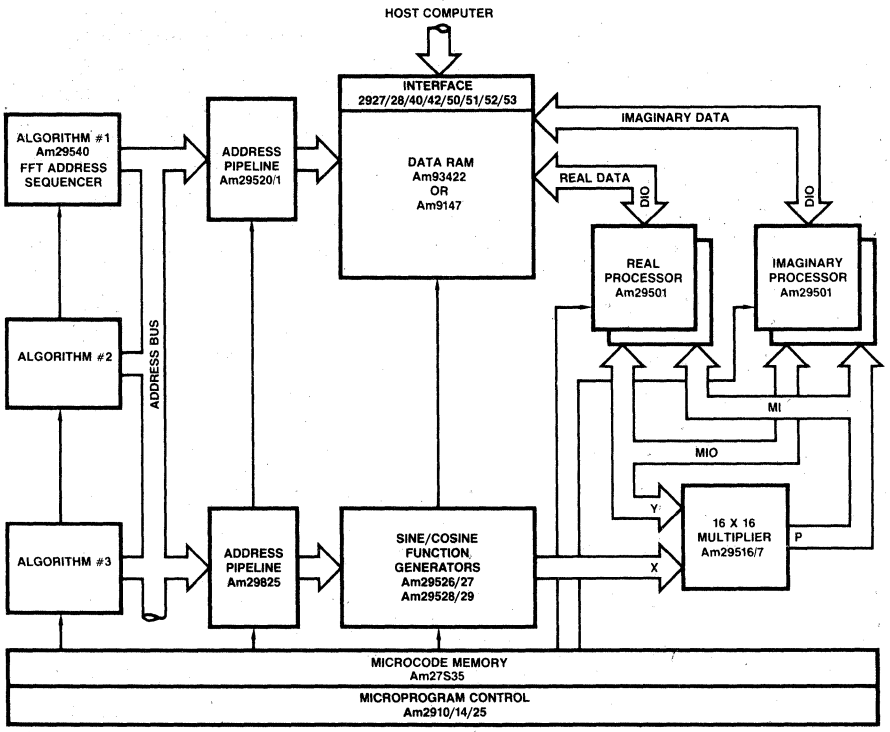
Fast multiplication is the key to high-speed digital-signal processing and high-speed array processing. In addition to the Am29516 and Am29517, Advanced Micro Devices is developing an extensive family of multipliers. The first addition to the high-performance multiplier group:

- Am29510 High-Performance 16 x 16 Bit Multiply Accumulator

The multiply accumulator provides single cycle multiply accumulation or subtraction. The Am29510 is a pin- and function-compatible alternate source for the TRW TDC1010J. As illustrated with the Am29516/517, the multiply accumulator will have a speed improvement over existing multiply accumulators.

- Am295XX to be announced.
  - *More Multipliers*
    A proliferation of the existing multiplier architectures will generate a complete family of multipliers and multiplier accumulators.
  - *Floating Point Processors* (FPP)
    A 32-bit FPP capable of performing single-cycle double-precision floating-point addition, subtraction, and multiplication. The FPP performs the arithmetic operations in DEC or IEEE format. Available 1984.

Am29500 ARRAY PROCESSOR



MPL-026

Electronics

Record signal-processing rates spring from chip refinements

Improved buses, reconfigurability, pipelining, and parallelism unite in a bipolar family for building array and signal processors

by Bernard New and Lyle Pittroff, *Advanced Micro Devices Inc., Sunnyvale, Calif.*

☐ The number-crunching microprocessor requirements of the 1980s are ill-served by today's comparatively slow, conventional central processing units. Instead, the algorithms executed by both general-purpose array processors and the more specialized digital-signal processors require highly individual architectures for maximum speed and performance. Jumping on the fast track is a new group of bipolar devices—the AM29500 family—that combines internal emitter-coupled-logic circuit design for speed with TTL outputs for compatibility with the outside world.

The family is able to overcome such speed-retarding problems as inadequate data-bus memory and bandwidths and slow execution times through a redesigned bus structure and parallel and pipelined processing. In fact, the bus structure is designed so that there are enough parallel buses to keep a device's multiplier or its arithmetic processing unit, or both, busy during each cycle. These features, plus programmable reconfigurability, make the 29500 family the fastest group of large-scale integrated parts for signal processors to be commercially available. In one series of tests, a 29500-based system had three times the speed achieved by the older 2900 family.

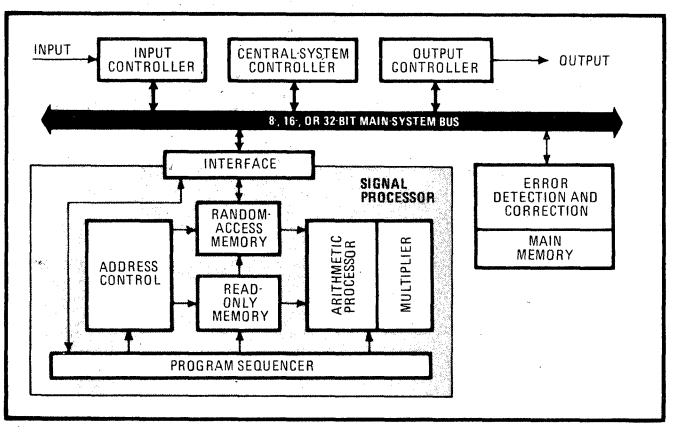
The 29500 series are general-purpose building blocks. They include a byte-slice, multiple-port programmable signal processor (the 29501), a 16-by-16-bit parallel multiplier with programmable input/output (the 29516/17), a multilevel pipeline register for data and address pipelining (the 29520/21), and a fast-Fourier-transform address sequencer (the 29540).

To increase processor speed, architectural enhancements had to be made to the older 2900 device designs. That family took some steps in the right direction because it provides many of the peripheral building blocks, like interface devices and direct-memory-access chips, needed for real-time signal processing. But the 2900's arithmetic devices are targeted at general-purpose computing. They do not have the parallel channels that are required for a high-speed array or signal processor environment.

One way of satisfying this need was to upgrade the 2900 family's bus structure, number organization, and resource management. The new bus structure can support addition or subtraction and multiplication on every cycle because of extra parallel buses. Number organization can now handle complex numbers in parallel quickly. In addition, flexibility of resource management permits the building blocks to be interconnected in enough ways to support all algorithms of interest efficiently.

For dedicated-function and multiple-algorithm processing (Fig. 1), a special-purpose processor like the 29501 operates under the control of a host computer system that switches large blocks of data between its main memory and temporary slave through DMA transfer. Once this transfer is complete, the special-purpose processor operates under local program control. Each algorithm is executed by its own software routine, which is stored in its own local memory independently of the host computer and its high-level language.

Although the precise architecture of Fig. 1 varies with the algorithm used, all array- and signal-processing algorithms have similar needs for



1. Dual-purpose. In a typical array- or digital-signal-processor architecture, both dedicated and multiple algorithm functions can be implemented. A host computer provides overall guidance and a large memory.

arithmetic and addressing—short, repetitive calculation loops requiring parallelism and pipelining. In addition, in digital-signal processing, arithmetic operations using complex numbers may be necessary, whereupon the computational load increases to twice as many additions or subtractions and four times as many multiplications as for real numbers.

Because calculation loops for arithmetic operations are short, the 29500 family surrounds the additions with continuous memory accesses—data is fetched, the calculation loop performed, and the results written back into memory. Hence there are many times more memory accesses than there are data points. For FFTs, the number of repetitive memory accesses is multiplied by the number of passes through the data. Fortunately, although the memory-access sequence is long, it is well structured, making it possible as a result to design dedicated address sequencers.

Divide and rule

The purpose of pipelining is to allow lengthy operations to be divided into suboperations, so that when one piece of data has completed a suboperation, the same hardware can start on the next piece. In this way, the 29501 allows up to a 500% speed improvement.

For example, because a typical processor handles a set number of algorithms, its architecture can be very specific concerning arithmetic and address generation—no longer does the CPU have to mix addressing with arithmetic computations. Also, separate sections can be streamlined to calculate each type in parallel and fast.

A significant feature of the data path for the 29500 family is the fact that the devices handle only data and do no address calculations. The data path can, therefore, be optimized for arithmetic.

The 29501 multiport parallel processor also represents the current thinking about multiport organization. It has a data-bus port, an output port to a multiplier, and an input port from a multiplier. The chip can process an FFT fast because of its highly parallel internal bus structure. In this structure, six registers operate as pipelines and are connected to the I/O ports and an arithmetic and logic unit by 10 separate byte-wide internal buses.

A typical cycle on the 29501 consists of data input from memory, data output to the multiplier, retrieving a previous product from the multiplier, and register-to-register ALU operations and data moves. Because these operations can occur during the same cycle, data manipulation is limited only by the designer's creativity. This flexibility, plus the possibility of parallel processors operating on complex numbers, is what makes high-speed operation possible.

Twice as fast

The 29500 family uses two high-speed parallel 16-by-16-bit multipliers—the 29516 and 29517. The 29516 is compatible with TRW's MPY-16HJ multiplier but is more than twice as fast and has an output multiplexer. Either the least or the most significant product can be selected at this multiplexer output for use in many pipelined architecture calculations.

On the other hand, the 29517 multiplier incorporates all the features of the 29516 but has a modified I/O-register clocking structure to provide a single-clock input with register enables. This approach is preferred to the older clock-gating method, which suffers from skews.

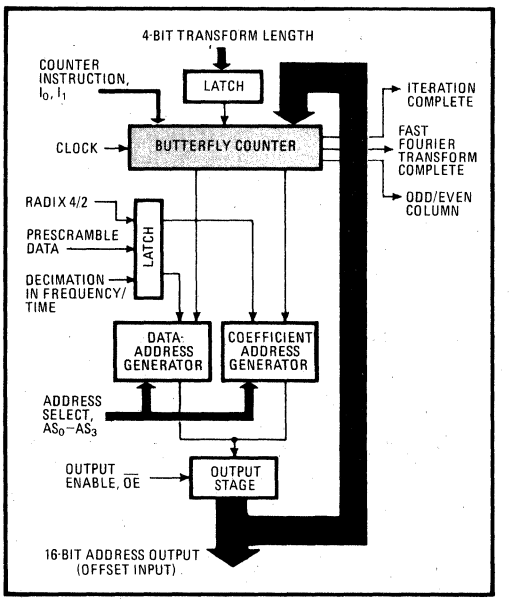
Dedicated addressing

Address-sequencing complexity for array and signal processors can range from integer counting to the complicated number patterns of FFTs. To keep addressing speeds high, the 29500 series generates addresses in parallel to the data path. However, other architectural considerations must also be weighed.

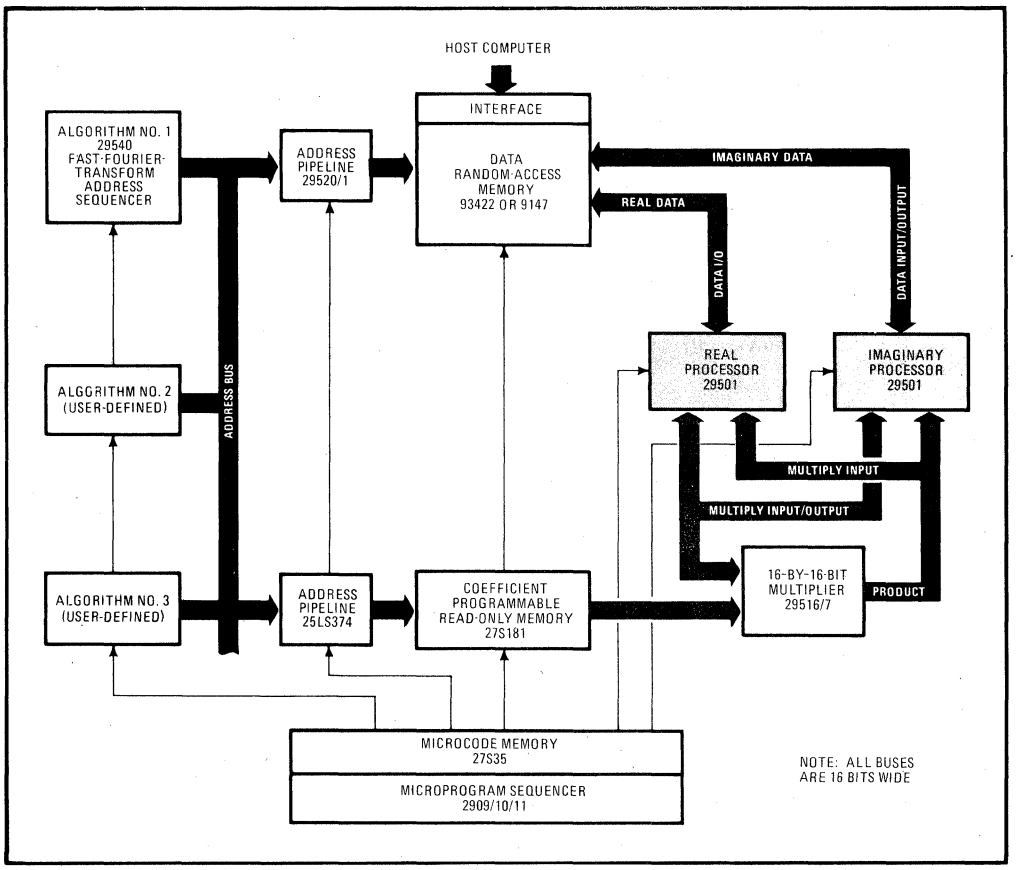
For a specific application, several system implications affect the choice of algorithm from the diversity of FFTs available. This choice, together with the transform length (or lengths) to be implemented, determines the address sequence to be generated. Usually, the nested-count nature of these sequences has forced the designer to use many medium-scale integrated-circuit packages.

The 29540 is a single-chip solution to the address-sequencing problem (Fig. 2). Four control inputs allow programmed or hardwired control of the actual number of data points in the transform. From this and other control-input commands, the 29540 can be sequenced through the entire transform while providing output flags. These flags indicate when each data pass is over and when the entire transform is complete.

For their part, the 29540's control inputs accept the most common FFT formats. The designer can opt for bit-reversed output order or bit-reversed input order, radix-2 or radix-4 address sequences, and decimation-



2. Multiple sequences. Fast Fourier transforms may have unusual address sequences, and with its four control inputs, the address-sequencing 29540 chip is designed to handle all of them. It provides output flags when a calculation is complete.



3. Complete. A typical signal-processing system provides separate, parallel paths for complex data. But in the 29500 setup, address pipelining handles both data and coefficient addressing operations for fast Fourier and other common transforms.

in-frequency or decimation-in-time sequences.

The 16-bit output port of the address sequencer is controlled by the counter and transform-length–input instructions. Any transform from 2 to 65,536 points long can be selected. The higher-order bits not required for the specified transforms (a 1,024-point transform only requires 10-bit addresses) can be preloaded through a bidirectional address port to access the next data block.

Easy address pipelining

Because the primary objective of this architecture is to operate on array- or signal-processor systems in a highly parallel manner, addresses must also be pipelined. As a result, each address must be tracked, which requires a pipeline register—such as the 29520 or 29521. These are byte-slice pipelining registers configurable as a dual two-level or a single four-level pipeline. In both devices, the single four-level configuration operates as a push-only stack. The selection of register is determined by the designer's choice of system timing and data movement.

The architecture of a typical 29500 signal-processing system (Fig. 3) can employ separate parallel data paths for complex data. Three possible address-generator blocks are shown, and together they represent a general-purpose processor. Address sequences for other than FFTs might be configured from programmable read-only memory or 2901-based designs. Address pipelining is shown for both data and coefficient addresses.

In this design, either bipolar or MOS static random-access memories store data temporarily, and high-speed bipolar PROMs and RAMs or MOS ROMs are used for coefficient look-up tables. The local-control store may be either a PROM or a writable control-store RAM and can be controlled by a 2910 program sequencer.

A common benchmark for signal processing is the execution speed of an FFT. The 29500 processor, operating at a 10-megahertz clock rate, can perform the transform in 400 nanoseconds. This speed allows a 1,024-point complex radix-2 butterfly to be completed in 2.0 milliseconds. Compared with the best throughput available in current bit-slice CPU architectures, this figure is more than a twentyfold improvement. □

Am29501

Multi-Port Pipelined Processor (Byte-Slice™)
Advanced Bipolar VLSI
ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- Expandable Byte-Slice™ Register-ALU
- Eight instruction ALU
  - Four arithmetic operations
  - Four logic operations
  - Force/Inhibit carry modes
  - Flexible expansion – has carry and $\overline{P}/\overline{G}$
- Ten internal data paths
  - Highly parallel architectures
  - Multiple simultaneous data manipulations
- Pipelining register file has six 8-bit registers
  - Multilevel pipelining
  - Multiple register-to-register moves
- Completely microprogrammable
  - No instruction encoding
  - All operation combinations available
- Three I/O ports for maximum system interconnect flexibility
- 64-pin DIP
- Single 5V supply with TTL I/O
- IMOX™ process with internal ECL

GENERAL DESCRIPTION

The Am29501 is an expandable Byte-Slice™ register-ALU designed to bring maximum speed to array processor and digital signal processor systems. It provides a flexible processor building block for implementing highly pipelined, highly parallel architectures where speed is achieved by a combination of optimized integrated circuit technology (IMOX™ process and internal ECL circuitry) and customized system architecture. I/O port flexibility and multiple concurrent data moves make it possible to construct processors capable of very high throughput. Parallel processors are especially efficient for array/vector operations or signal processing algorithms requiring complex number arithmetic (e.g. FFT, convolution, correlation, etc.).

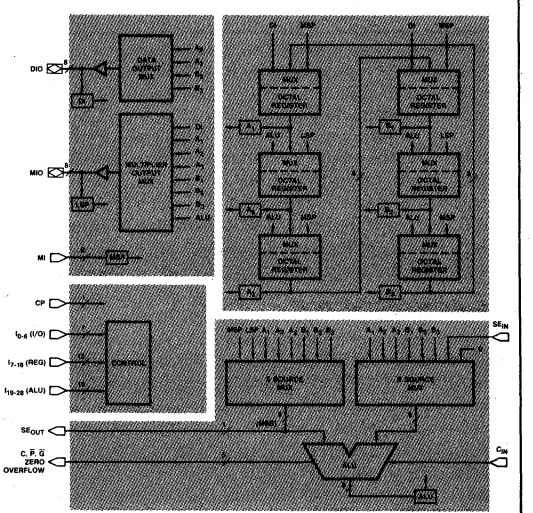
The Am29501's Pipeline Register File provides data storage and pipelining flexibility. Any combination of register instructions, ALU instructions, and I/O instructions can be microprogrammed to occur in the same cycle. This allows overlap of external multiplication, ALU operations, and memory I/O.

Three I/O ports support a wide variety of parallel, pipelined architectures by providing separate I/O ports for the multiplier and the memory data bus. Either of two bidirectional I/O ports, DIO and MIO, can interface to the data bus or multiplier Y-input port and a separate MI port connects to the multiplier output port.

RELATED PRODUCTS

Part No.	Description
Am2902	Carry look-ahead generator
Am29516/17	16 x 16 bit high speed multipliers
Am25S558	8 x 8 bit multiplier

SIMPLIFIED BLOCK DIAGRAM



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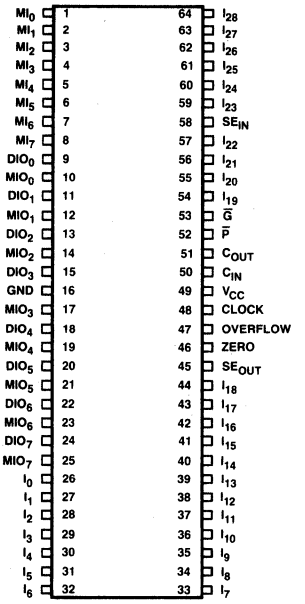
CONNECTION DIAGRAMS
Top Views

D-64-3



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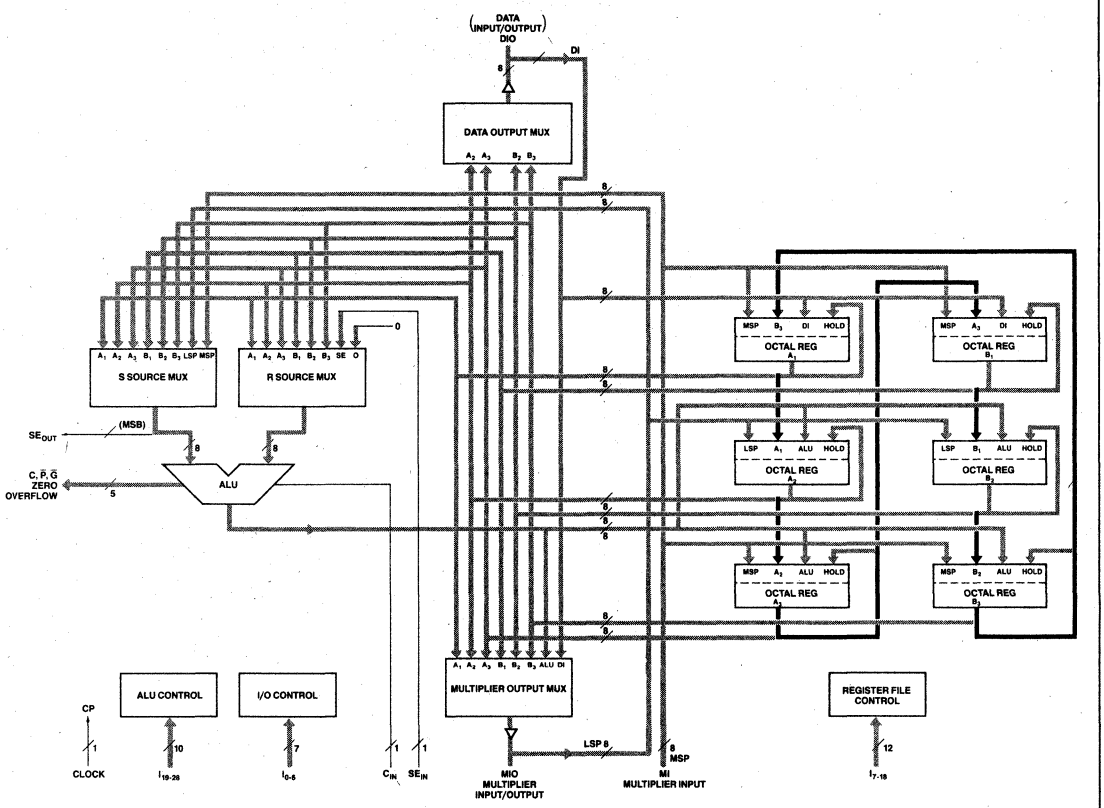
Chip-Pak™

L-68-1

DETAILED Am29501 BLOCK DIAGRAM



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PIN DESCRIPTIONS

C_{IN} Carry-in input to the internal 8-bit ALU.

C_{OUT} Carry-out output from the internal 8-bit ALU.

CP Clock input for the internal pipeline register file. Data selected by $I_7 - I_{18}$ meeting the setup and hold time requirements of the respective register is clocked into the register on the clock LOW-to-HIGH transition.

$DIO_0 - DIO_7$ Bidirectional data I/O port. (see Note)

$\overline{G}$, $\overline{P}$ The carry generate and propagate outputs of the internal ALU. These signals are used with the Am2902A for carry-lookahead.

$I_0 - I_{28}$ Instruction inputs designed to be driven under microprogram control. All instruction inputs control multiplexers, or drivers or the ALU directly. There is no instruction encoding. See Control Input Function Tables for operating modes.

$MI_0 - MI_7$ Data Input port. (Multiplier Input – see Note)

$MIO_0 - MIO_7$ Bidirectional data I/O port. (Multiplier I/O – see Note)

OVR Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.

SE_{OUT} The most significant bit of the S-operand. This is used in multiple precision arithmetic operations for sign extension of two's complement numbers.

SE_{IN} A single bit input which generates an 8-bit sign extension R-operand for multiple precision two's complement arithmetic operations.

ZERO This is an open collector output which goes HIGH if the data on the ALU outputs are all LOW.

Note: This is a general purpose data port. The names are derived from the typical usage in a typical Am29500 system but are not restricted to this interconnection scheme.

Am29501
ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise specified:

COM'L	T_A = 0 to +70°C	V_{CC} = 5.0V ±5%	(MIN = 4.75V	MAX = 5.25V)
MIL	T_C = −55 to +125°C	V_{CC} = 5.0V ±10%	(MIN = 4.50V	MAX = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}		I_{OH} = −2.6mA (COM'L)	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	COM'L	I_{OL} = 24mA DIO, MIO			0.5	Volts
				I_{OL} = 8mA Others			0.5	
			MIL	I_{OL} = 16mA DIO, MIO				
				I_{OL} = 8mA Others			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V					−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V					20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					0.1	mA
I_{OZH}	Off-State (High Impedance) Output Current	V_{CC} = MAX		V_O = 0.5V			−55	μA
I_{OZL}				V_O = 2.4V			100	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−30		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX	COM'L and MIL	T_A = 25°C		300		mA
			COM'L Only	T_A = 0 to +70°C			400	
				T_A = +70°C			375	
			MIL Only	T_C = −55 to +125°C				
				T_C = +125°C				

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature under Bias − T_C	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5 to +5.5V
DC Output Current, into Outputs	30mA
DC Input Current	−30 to +5.0mA

Am29501

SWITCHING CHARACTERISTICS AT ROOM TEMPERATURE

Typical Setup/Hold Times and Propagation Delays
V_{CC} = 5.0V, T_A = +25°C, C_L = 50pF

To Output / From Input	Setup, t_S/Hold, t_H		Propagation Delay Times, t_{PD}									
	Register Input	Reg via ALU	MIO Port	MIO via ALU	DIO Port	C_{OUT}	P	G	Z	Overflow	SE_{OUT}	Units
CLK			17	27	17	23	23	23	27	34	18	ns
DIO			12									ns
MIO						22	22	22	25	22	17	ns
MI				24		22	22	22	25	22	17	ns
C_{IN}				16		10			17	13		ns
SE_{IN}				23		19	19	16	22	19		ns
I_{2-3} (DIO)					14							ns
I_{4-6} (MIO)			15									ns
I_{7-18} (REG)												ns
I_{19-22} (ALU OP)			25			19	19	19	22	19		ns
I_{23-28} (ALU SEL)				31		20	20	20	25	22	14	ns

Minimum Setup/Hold Times and Maximum Propagation Delays
V_{CC} = 5.0V, T_A = +25°C, C_L = 50pF

To Output / From Input	Setup, t_S/Hold, t_H		Propagation Delay Times, t_{PD}									
	Register Input	Reg via ALU	MIO Port	MIO via ALU	DIO Port	C_{OUT}	P	G	Z	Overflow	SE_{OUT}	Units
CLK												ns
DIO												ns
MIO												ns
MI												ns
C_{IN}												ns
SE_{IN}												ns
I_{2-3} (DIO)												ns
I_{4-6} (MIO)												ns
I_{7-18} (REG)												ns
I_{19-22} (ALU OP)												ns
I_{23-28} (ALU SEL)												ns

Am29501 Three-State Timing

Parameters	Description	Typ V_{CC} = 5V T_A = 25°C	Max V_{CC} = 5V T_A = 25°C	COM'L Max V_{CC} = 5V ±5% T_A = 0 to −70°C	MIL Max V_{CC} = 5V ±10% T_A = −55 to −125°C	Units	Test Conditions
t_{LZ}	$I_0 \rightarrow DIO_{0-7}$					ns	C_L = 5P, R_L = 667Ω
	$I_1 \rightarrow MIO_{0-7}$						
t_{HZ}	$I_0 \rightarrow DIO_{0-7}$					ns	
	$I_1 \rightarrow MIO_{0-7}$						
t_{ZL}	$I_0 \rightarrow DIO_{0-7}$					ns	C_L = 50P, R_L = 667Ω
	$I_1 \rightarrow MIO_{0-7}$						
t_{ZH}	$I_0 \rightarrow DIO_{0-7}$					ns	
	$I_1 \rightarrow MIO_{0-4}$						

Am29501
SWITCHING CHARACTERISTICS, COMMERCIAL

Minimum Setup/Hold Times and Maximum Propagation Delays
V_{CC} = 5V ±5%, T_A = 0 to +70°C, C_L = 50pF

To Output / From Input	Setup, t_S/Hold, t_H		Propagation Delay Times, t_{PD}									
	Register Input	Reg via ALU	MIO Port	MIO via ALU	DIO Port	C_{OUT}	P	G	Z	Overflow	SE_{OUT}	Units
CLK			23	35	24	31	31	31	39	34	26	ns
DIO	10/5		17									ns
MIO	10/5	20/0				29	29	29	34	29	24	ns
MI	10/5	20/0		32		30	29	29	34	29	24	ns
C_{IN}		10/5		25		15			26	19		ns
SE_{IN}		20/0		29		27	27	22	32	27		ns
I_{2-3} (DIO)					21							ns
I_{4-6} (MIO)			22									ns
I_{7-18} (REG)	10/5											ns
I_{19-22} (ALU OP)		20/0	32			27	27	27	32	29		ns
I_{23-28} (ALU SEL)		20/0				29	29	29	35	32	22	ns

Am29501
SWITCHING CHARACTERISTICS, MILITARY

Minimum Setup/Hold Times and Maximum Propagation Delays
V_{CC} = 5V ±10%, T_C = −55 to +125°C, C_L = 50pF

To Output / From Input	Setup, t_S/Hold, t_H		Propagation Delay Times, t_{PD}									
	Register Input	Reg via ALU	MIO Port	MIO via ALU	DIO Port	C_{OUT}	P	G	Z	Overflow	SE_{OUT}	Units
CLK												ns
DIO												ns
MIO												ns
MI												ns
C_{IN}												ns
SE_{IN}												ns
I_{2-3} (DIO)												ns
I_{4-6} (MIO)												ns
I_{7-18} (REG)												ns
I_{19-22} (ALU OP)												ns
I_{23-28} (ALU SEL)												ns

Note: Please refer to *Guidelines for Testing Am2900 Family Devices* in section 13 of this data book.

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Am29501 Minimum Clock Pulse Widths

Parameter	Description		COM'L: V_{CC} = 5V, T_A = 25°C	COM'L: V_{CC} = 5V ±5%, T_A = 0 to −70°C	MIL: V_{CC} = 5V ±10%, T_A = −55 to −125°C	Units
t_{PW}	Clock Pulse Width	High				ns
		Low				ns

CONTROL INPUT FUNCTION TABLES

1. Data I/O Port (DIO) Output Select

I_3	I_2	I_0	Source
L	L	L	A_2
L	H	L	A_3
H	L	L	B_2
H	H	L	B_3
X	X	H	Output Disabled

2. Multiplier I/O Port (MIO) Output Select

I_6	I_5	I_4	I_1	Source
L	L	L	L	A_1
L	L	H	L	A_2
L	H	L	L	A_3
L	H	H	L	B_1
H	L	L	L	B_2
H	L	H	L	B_3
H	H	L	L	ALU
H	H	H	L	DI
X	X	X	H	Output Disabled

3. Register A_1 Data Source Select

I_8	I_7	Source
L	L	MSP (MI)
L	H	DI (DIO)
H	L	B_3
H	H	A_1 (Hold)

4. Register A_2 Data Source Select

I_{10}	I_9	Source
L	L	LSP (MIO)
L	H	ALU
H	L	A_1
H	H	A_2 (Hold)

5. Register A_3 Data Source Select

I_{12}	I_{11}	Source
L	L	MSP (MI)
L	H	ALU
H	L	A_2
H	H	A_3 (Hold)

6. Register B_1 Data Source Select

I_{14}	I_{13}	Source
L	L	MSP (MI)
L	H	DI (DIO)
H	L	A_3
H	H	B_1 (Hold)

7. Register B_2 Data Source Select

I_{16}	I_{15}	Source
L	L	LSP (MIO)
L	H	ALU
H	L	B_1
H	H	B_2 (Hold)

8. Register B_3 Data Source Select

I_{18}	I_{17}	Source
L	L	MSP (MI)
L	H	ALU
H	L	B_2
H	H	B_3 (Hold)

CONTROL INPUT FUNCTION TABLES (Cont.)

9. ALU Operating Instructions

I_{22}	I_{21}	I_{20}	I_{19}	OP	C_{OUT}	$\overline{P}$	$\overline{G}$	
L	L	L	L	R + S + C_{IN}	Carry	$\overline{P}$	$\overline{G}$	Normal Operating Mode Usually Carry Used for 16-Bit Expansion and $\overline{P}/\overline{G}$ Used with a Am2902A Carry-Lookahead for Larger Expansion
L	H			R − S − C_{IN}				
H	L			R + C_{IN}				
H	H			−R + S − C_{IN}				
L	L	L	H	R + S + C_{IN}	L	H	H	Inhibit Carry Mode
L	H			R − S − C_{IN}				
H	L			R + C_{IN}				
H	H			−R + S − C_{IN}				
L	L	H	L	R + S + C_{IN}	H	$\overline{P}$	L	Force Carry Mode
L	H			R − S − C_{IN}				
H	L			R + C_{IN}				
H	H			−R + S − C_{IN}				
L	L	H	H	R XOR S	(L)*	(H)*	(H)*	Logic Operations
L	H			R AND S				
H	L			$\overline{R}$				
H	H			R OR S				

*C_{OUT}, P and G are not applicable to logic operation, Am29501 functions as shown.

10. ALU R Operand Selection

I_{25}	I_{24}	I_{23}	Source
L	L	L	A_1
L	L	H	A_2
L	H	L	A_3
L	H	H	B_1
H	L	L	B_2
H	L	H	B_3
H	H	L	Sign Extend Input Bussed to All Bits
H	H	H	Arithmetic Zero (All Inputs LOW)

11. ALU S Operand Selection

I_{28}	I_{27}	I_{26}	Source
L	L	L	A_1
L	L	H	A_2
L	H	L	A_3
L	H	H	B_1
H	L	L	B_2
H	L	H	B_3
H	H	L	MSP (MI)
H	H	H	LSP (MIO)

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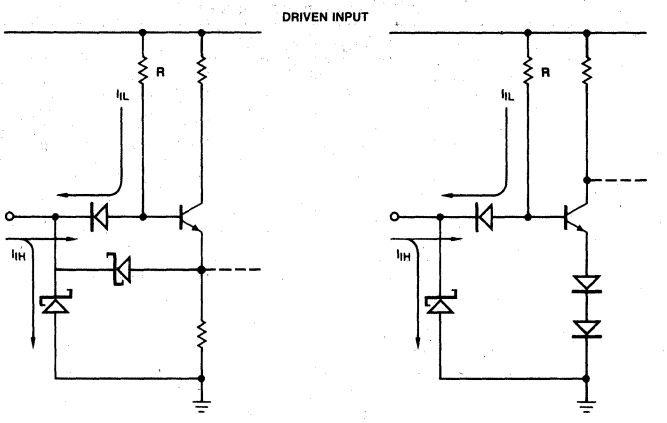
Am29501 μProgramming Worksheet

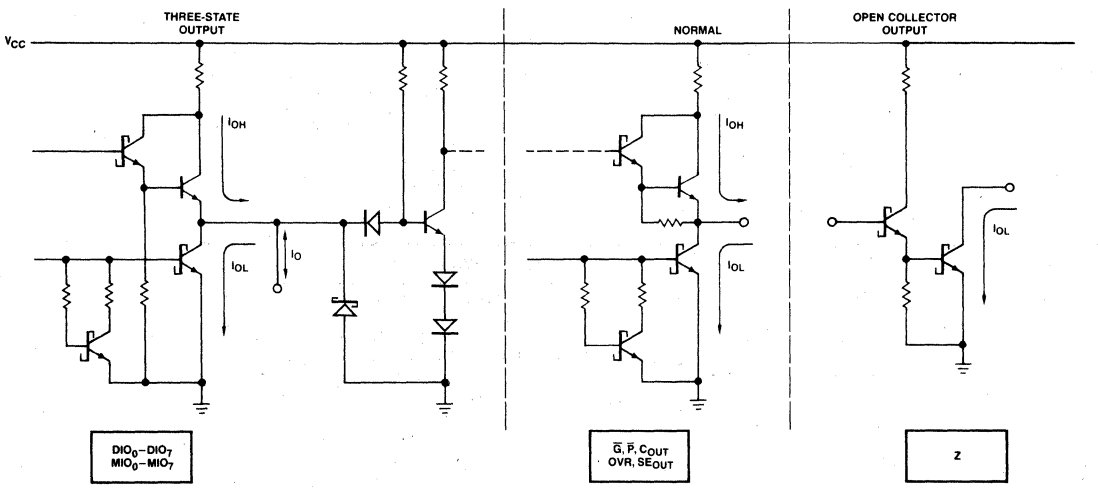
Line No	ALU Instruction			Register Instruction						MIO	DIO	MIO	DIO
	S Input	R Input	Operation	B_3	B_2	B_1	A_3	A_2	A_1	Output	Output	$\overline{OE}$	$\overline{OE}$
	I_{28} I_{27} I_{26}	I_{25} I_{24} I_{23}	I_{22} I_{21} I_{20} I_{19}	I_{18} I_{17}	I_{16} I_{15}	I_{14} I_{13}	I_{12} I_{11}	I_{10} I_9	I_8 I_7	I_6 I_5 I_4	I_3 I_2	I_1	I_0

INPUT/OUTPUT CURRENT INTERFACE CONDITION



$C_I \approx 5.0pF$, all inputs

MPL-026



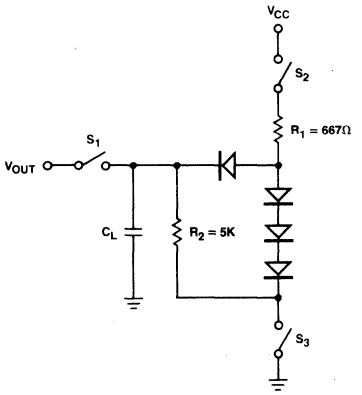
$C_O \approx 5.0pF$, all outputs

Note: Actual current flow direction shown.

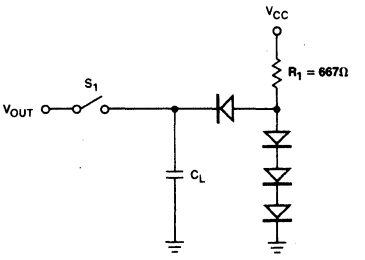
MPL-029

TEST LOADS FOR DELAY MEASUREMENTS

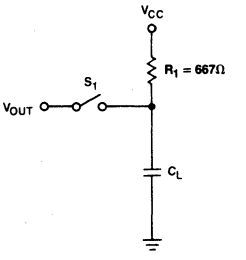
A. THREE-STATE OUTPUTS



B. NORMAL OUTPUTS



C. OPEN-COLLECTOR OUTPUTS

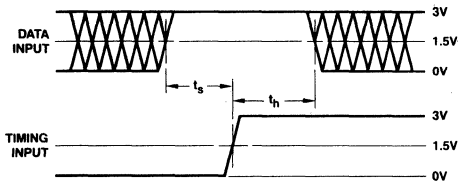


Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

MPL-030

7

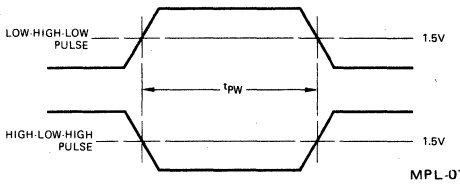
SET UP, HOLD, AND RELEASE TIMES



Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

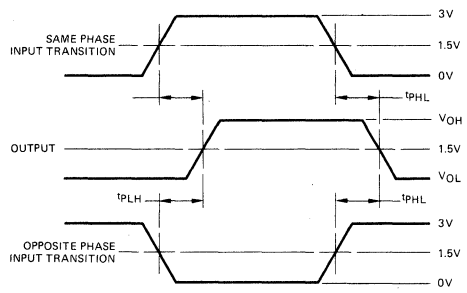
MPL-031

PULSE WIDTH



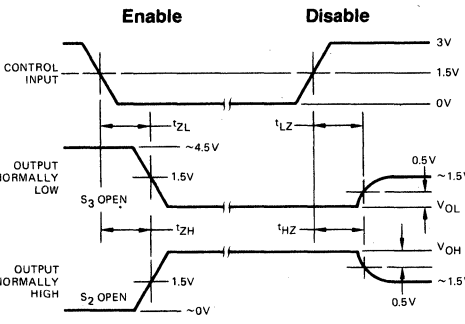
MPL-073

PROPAGATION DELAY



MPL-032

ENABLE AND DISABLE TIMES



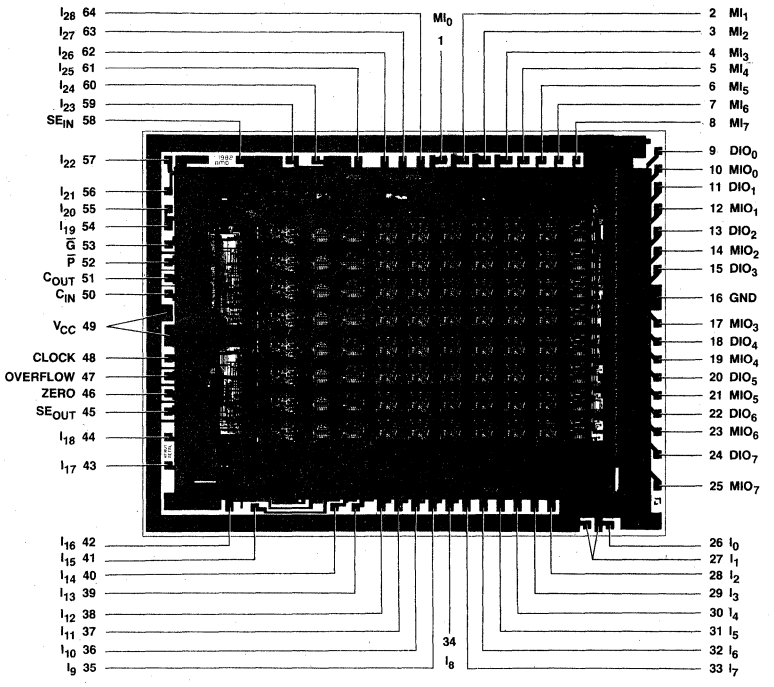
Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1, S_2 and S_3 of Load Circuit are closed except where shown.

MPL-074

Note: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_o = 50Ω; t_r ≤ 2.5ns; t_f ≤ 2.5ns.

CHIP TOPOGRAPHY

Am29501



MPL-075

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Am29501 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM29501DC	D-64-	C	C-1
AM29501DCB	D-64-	C	B-2 (Note 4)
AM29501DM	D-64-	M	C-3
AM29501DMB	D-64-	M	B-3
AM29501LC	D-68-	C	C-1
AM29501LM	D-68-	M	C-3
AM29501LMB	D-68-	M	B-3

Notes: 1. D = Hermetic DIP, L = Chip-Pak. Number following letter is number of leads.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 160 hour burn-in.

Am29510

16 x 16 Multiply Accumulator

DISTINCTIVE CHARACTERISTICS

- High speed 16 x 16-bit multiplication and product accumulation
- Performs subtraction and double precision addition and multiplication
- Uses two's complement or unsigned inputs
- Round control
- 35-bit product accumulation result
  - 32-bit multiply
  - 3-bit extended product
- Output register preload
- Three-state output control
- IMOX™ processing
  - ECL internal circuitry for speed
  - TTL I/O
- Single 5V power

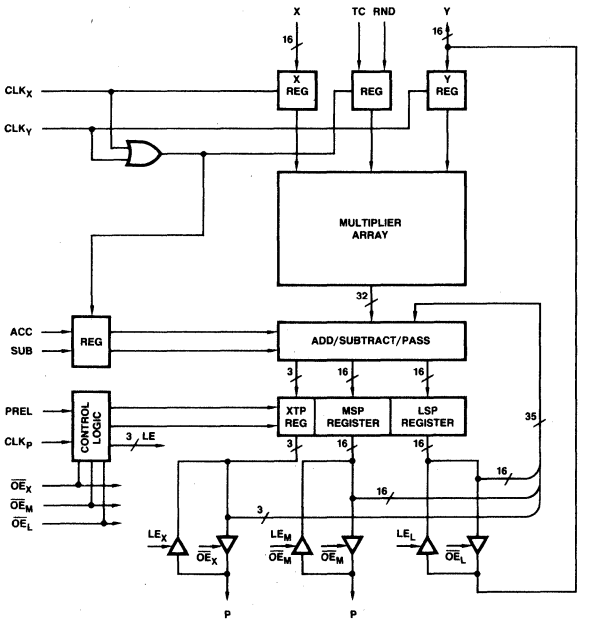
FUNCTIONAL DESCRIPTION

The Am29510 is a high-speed 16 x 16-bit multiplier/accumulator (MAC). It comprises a 16-bit parallel multiplier followed by a 35-bit accumulator. Two 16-bit input registers are provided for the X and Y operands. A third register is used to store two control bits, TC and RND. TC specifies that the input are two's complement signed numbers (High) or unsigned numbers (Low). The RND control, when high, causes a bit to be added to the multiplier product with the weight of P_{15}. This causes the most significant 16 bits of product to be rounded to the value nearest to the full 32-bit product. Using the RND control once during an accumulation causes the most significant 19 bits of the accumulator to be rounded to the value nearest the full 35-bit accumulation. The TC/RND register is clocked whenever the X or Y input registers are clocked. The X, Y, TC/RND, and accumulator registers are all positive edge triggered.

The 32-bit multiplier output is zero-filled or sign-extended as appropriate to provide a 35-bit input to the accumulator.

The accumulator has four functions; the product may be loaded into the accumulator, the product may be added into the accumulator value, the previous accumulator value may be subtracted from the product and the result stored in the accumulator or the accumulator may be preloaded from an extended source. The operation of the accumulator is controlled by the signals ACC, SUB, and PREL. For output and preloading purposes the accumulator is considered in three sections; least significant product (LSP, $P_0 - P_{15}$) controlled by $\overline{OE}_X$. When PREL is low these controls are active low enables for the three-state output buffers. When PREL is high the output buffers automatically become high impedance, and the controls operate as active low load enables to the three sections of the accumulator to permit loading of data applied to the bidirectional P port. The P port has 35 bits, the least significant 16 of which share pins with the Y input.

BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise specified:

COM'L $T_A = 0$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN = 4.75V MAX = 5.25V)
MIL $T_C = -55$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN = 4.50V MAX = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, $V_{IN} = V_{IH}$ or V_{IL}	V_{IL} = .8V, V_{IH} = 2.0V	$I_{OH} = -0.4mA$	2.4	2.7		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, $V_{IN} = V_{IH}$ or V_{IL}	V_{IL} = .8V, V_{IH} = 2.0V, I_{OL} = 4.0mA			.3	.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			.8	Volts
				COM'L			.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, $I_{IN} = 18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, $V_{IN} = 0.4V$					−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, $V_{IN} = 2.4V$					75	μA
I_I	Input HIGH Current	V_{CC} = MAX, $V_{IN} = 5.5V$					1	mA
I_{OZH}	Off State (High Impedance) Output Current	V_{CC} = MAX	Product	$V_O = 2.4V$			25	μA
I_{OZL}				$V_O = 0.4V$			−25	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX	Y	$V_O = 0V$	−3		−85	mA
			Product	$V_O = 0V$	−3		−85	
I_{CC}	Power Supply Current	V_{CC} = MAX	COM'L and MIL	$T_A = 25°C$				mA
			COM'L Only	$T_A = 0$ to $+70°C$				
				$T_A = +70°C$				
			MIL Only	$T_C = -55$ to $+125°C$				
				$T_C = +125°C$				

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature under Bias − T_C	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to $+V_{CC}$ max
DC Input Voltage	−0.5 to +5.5V
DC Output Current, into Outputs	30mA
DC Input Current	−30 to +5.0mA

RELATED PRODUCTS

Part No.	Description	Page
Am29526/527	High speed Sine function generator	
Am29528/529	High speed Cosine function generator	

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM29510DC	D-64	C	C-1
AM29510DC-B	D-64	C	B-1
AM29510DM	D-64	M	C-3
AM29510DM-B	D-64	M	B-3

Notes: 1. D = Hermetic DIP.
2. C = 0 to +70°C, $V_{CC} = 5V \pm 5\%$, M = −55 to +125°C, $V_{CC} = 5V \pm 10\%$.
3. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Levels B-1 and B-3 conform to MIL-STD-883, Class B.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		$T_A = 25°C$, $V_{CC} = 5.0V$ Typ	COM'L: $T_A = 0$ to $+70°C$, $V_{CC} = 5V \pm 5\%$ Min	COM'L Max	MIL: $T_C = -55$ to $+125°C$, $V_{CC} = 5V \pm 10\%$ Min	MIL Max	Units	Test Conditions
t_{MA}	Multiply Accumulate Time							ns	
t_S	X_i, Y_i, RND, TC, ACC, SUB Setup Time							ns	
t_H	X_i, Y_i, RND, TC, ACC, SUB Hold Time							ns	
t_S	PREI Setup Time							ns	
t_H	PREI Hold Time							ns	
t_{PWH}	Clock Pulse Width High							ns	
t_{PWL}	Clock Pulse Width Low							ns	
t_{PDP}	Output Clock to P							ns	
t_{PDY}	Output Clock to Y							ns	
t_{PHZ}	$\overline{OE}_X$, $\overline{OE}_M$ to P Disable Time	High to Z						ns	
t_{PLZ}		Low to Z						ns	
t_{PZH}	$\overline{OE}_X$, $\overline{OE}_M$ to P Disable Time	Z to High						ns	
t_{PZL}		Z to Low						ns	
t_{PHZ}	$\overline{OE}_L$ to Y Disable Time	High to Z						ns	
t_{PLZ}		Low to Z						ns	
t_{PZH}	$\overline{OE}_L$ to Y Disable Time	Z to High						ns	
t_{PZL}		Z to Low						ns	

7

DEFINITION OF FUNCTIONAL TERMS

RND — **Round**
Adds a bit with a weight of P_{15} to the multiplier product (High) the RND control is loaded on the rising edge of CLK_X or CLK_Y.

TC — **Two's Complement**
The X and Y data inputs are defined as two's complement signed data (High) or unsigned data (Low). The TC control is loaded on the rising edge of CLK_X or CLK_Y.

PREL — **(Preload)**
Data is preloaded into the specific output register when $\overline{OE}_X$, $\overline{OE}_Y$ and $\overline{OE}_L$ are high (High). (See Preload Truth Table.) The contents of the register will be loaded on the rising edge of CLK_P.

$\overline{OE}_X$ — **TSX***
Three-state control for the XTP port. Enabled (Low), disabled (High).

$\overline{OE}_M$ — **TSM***
Three-state control for the MSP port. Enabled (Low), disabled (High).

$\overline{OE}_L$ — **TSL***
Three-state control for the LSP port. Enabled (Low), disabled (High).

CLK_X, CLK_Y — Loads X and Y data respectively and TC, RND ACC and SUB on the rising edge.

CLK_P — Load data into XTP, MSP and LSP after ACC, SUB, PASS and for preload on rising edge.

$X_0 - X_{15}$ — **Multiplier Data Input**
Data I loaded in X-register on the rising edge of CLK_X.

$Y_0 - Y_{15}$, $P_0 - P_{15}$ — **Bidirectional Port**
Multiplier data input or Least Significant Product (LSP) output (OE_L = Low) or LSP Register Preload Input (PREI = High, and OE_L = High).

$P_{15} - P_{31}$ — **Bidirectional Port**
Product output for the Most Significant Product (MSP) and input to preload MSP register.

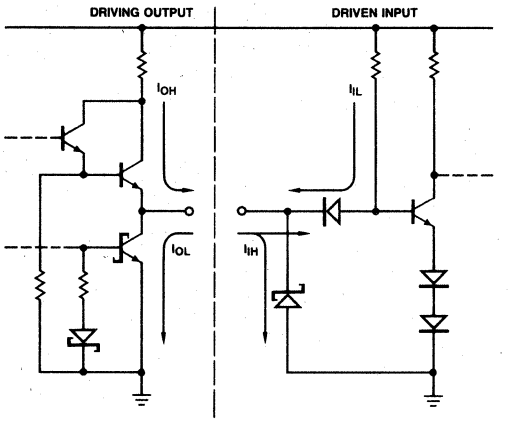
$P_{32} - P_{34}$ — **Bidirectional Port**
Product output for Extended Product (XTP) and input to preload XTP register.

ACC — **Accumulate**
Controls the addition of a multiply product to the contents of the XTP, MSP and LSP registers (High), or performs a multiply only (Low).

SUB — **Subtraction**
Controls the subtraction of the XTP, MSP and LSP registers from the multiply product (High and ACC = High). Both the ACC and SUB controls are loaded on the rising edge of CLK_X or CLK_Y.

*TRW TDC1010J pin description.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



MPL-015

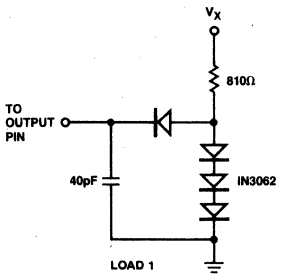
TEST WAVEFORMS

Test	V_X	Output Waveform – Measurement Level
All t_{PD}s	V_{CC}	V_{OH}, V_{OL}, 1.5V
t_{PHZ}	0.0V	V_{OH}, 0.5V, 0.0V
t_{PLZ}	2.6V	2.6V, V_{OL}, 0.5V
t_{PZH}	0.0V	V_{OH}, .5V, 0.0V
t_{PZL}	2.6V	2.6V, .5V, V_{OL}

MPL-016

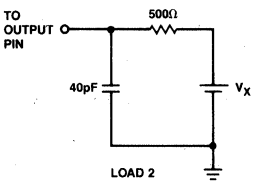
TEST LOADS FOR DELAY MEASUREMENTS

Normal Load



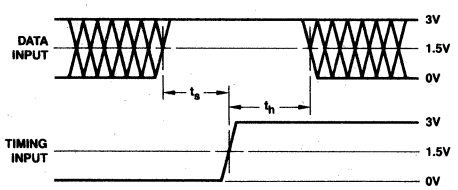
MPL-017

Three-State Delay Load



MPL-018

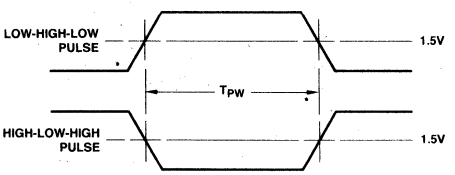
SET-UP AND HOLD TIME



Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

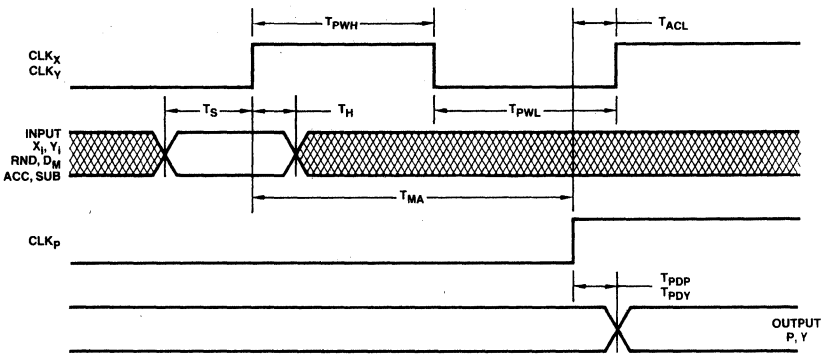
MPL-013

PULSE WIDTH



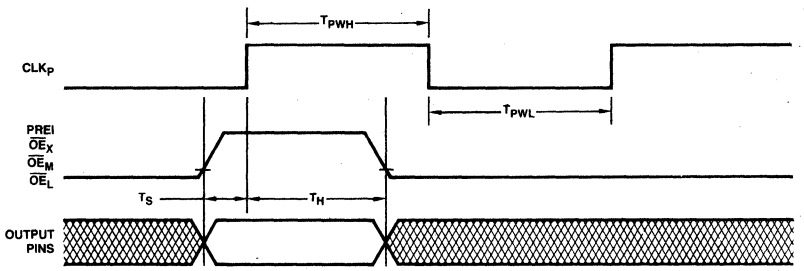
MPL-014

Am29510
TIMING DIAGRAMS



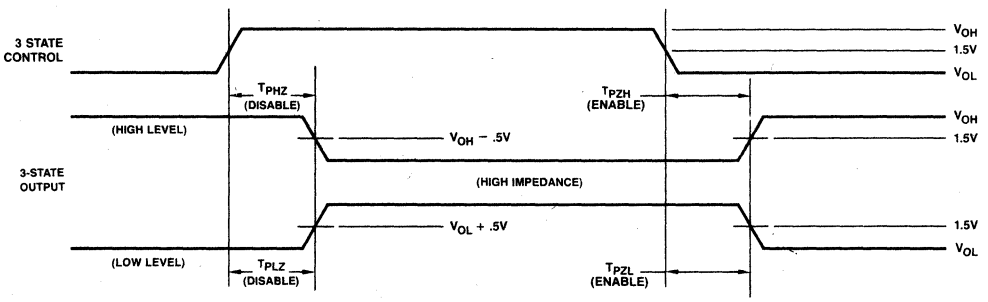
ABL-002

Am29510
PRELOAD TIMING DIAGRAM



ABL-003

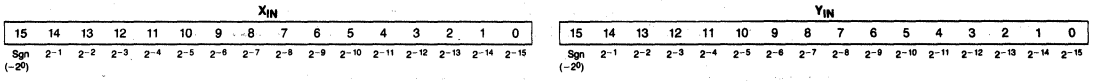
Am29510
THREE-STATE
TIMING DIAGRAM



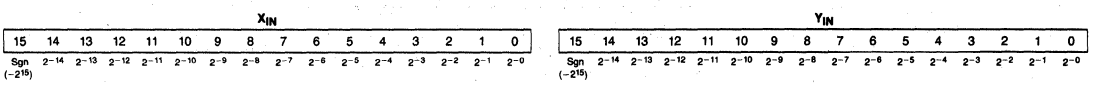
MPL-021

Am29510
INPUT FORMATS

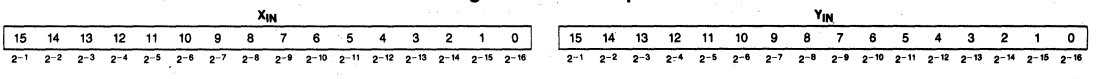
Fractional Two's Complement Input



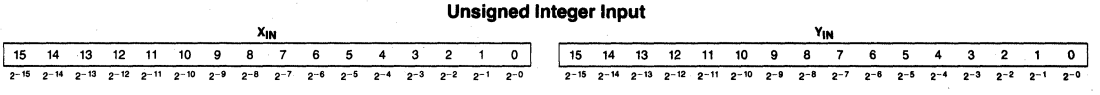
Integer Two's Complement Input



Unsigned Fractional Input

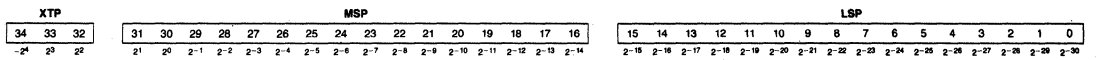


Unsigned Integer Input

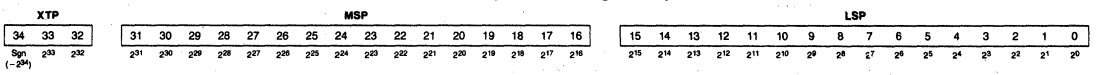


Am29510
OUTPUT FORMATS

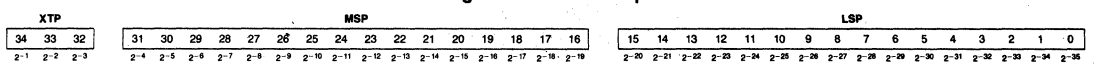
Two's Complement Fractional Output



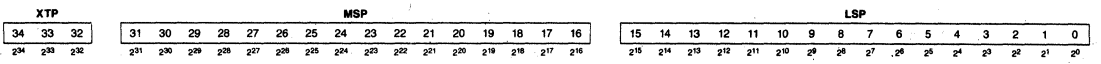
Two's Complement Integer Output



Unsigned Fractional Output



Unsigned Integer Output



ABL-004

PRELOAD FUNCTION

				Output Register		
PREI	OE_X	OE_M	OE_L	XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Z
0	0	1	0	Q	Z	Q
0	0	1	1	Q	Z	Z
0	1	0	0	Z	Q	Q
0	1	0	1	Z	Q	Z
0	1	1	0	Z	Z	Q
0	1	1	1	Z	Z	Z
1	0	0	0	Z	Z	Z
1	0	0	1	Z	Z	PL
1	0	1	0	Z	PL	Z
1	0	1	1	Z	PL	PL
1	1	0	0	PL	Z	Z
1	1	0	1	PL	Z	PL
1	1	1	0	PL	PL	Z
1	1	1	1	PL	PL	PL

Z = output buffers at High impedance (disabled).

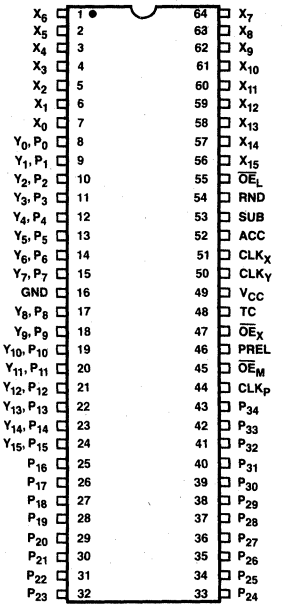
Q = output buffers at Low impedance. Contents of output register available through output ports.

PL = output disabled. Preload data supplied to the output pins will be loaded into the output register at the rising edge of CLK_P.

CHIP TOPOGRAPHY

CONNECTION DIAGRAMS
Top Views

Dual In-Line



Note: Pin 1 is marked for orientation.

ABL-005

Leadless Chip Carrier

Am29516 • Am29517
Am29516A • Am29517A

16 x 16-Bit Parallel Multipliers

DISTINCTIVE CHARACTERISTICS

- High speed 16 x 16 parallel multiplier
- Two's complement, unsigned or mixed operands
- Full product multiplexed at output
- Am29516 pin and functionally compatible with TRW MPY-16HJ
- Am29517 optimized for microprogramming, single clock with register enables
- Am29516A and Am29517A are % faster than the Am29516 and Am29517 respectively
- The Am29516A and Am29517A meet or exceed all of the specifications for the Am29516 and Am29517 respectively
- IMOX™ oxide isolated process
- ECL multiplier array provides 40ns typical multiply time
- TTL I/O-single +5V supply
- 64-pin package

RELATED PRODUCTS

Part No.	Description
Am29501	Multiport pipelined processor
Am29526/27	Sine function generator
Am29528/29	Cosine function generator

FUNCTIONAL DESCRIPTION

The Am29516/16A and Am29517/17A are high speed parallel 16 x 16-bit multipliers utilizing internal ECL logic to generate a 32-bit product. 17-bit input registers are provided for the X and Y operands and their associated mode controls X_M and Y_M. These mode controls are used to specify the operands as two's complement or unsigned numbers.

At the output of the multiplier array a format adjust control (FA) allows the user to select either a full 32-bit product or a left shifted 31-bit product suitable for two's complement only.

Two 16-bit output registers are provided to hold the most and least significant halves of the product (MSP and LSP) as defined by FA. For asynchronous output these registers may be made transparent by taking the feed through control (FT) high. A round control (RND) allows the rounding of the MSP. This control is registered, and is entered whenever either input register is clocked.

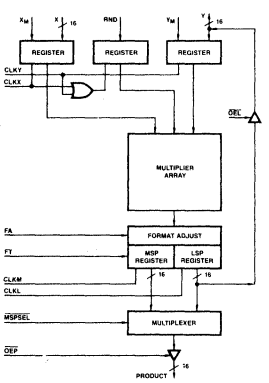
The two halves of the product may be routed to a 16-bit 3-state output port (P) via a multiplexer. In addition the LSP is connected to the Y-input port through a separate 3-state buffer.

In the Am29516/16A the X, Y, MSP and LSP registers have independent clocks (CLKX, CLKY, CLKM, CLKL). The output multiplexer control ($\overline{\text{MSPSEL}}$) uses a pin which is a supply ground in the TRW MPY 16HJ. When this control is LOW the function is that of the MPY16HJ, thus allowing full compatibility.

The Am29517/17A differs in that it has a single clock input (CLK) and three register enables (ENX, ENY, ENP) for the two input registers and the entire product. This facilitates the use of the part in microprogrammed systems. In both parts data is entered into the registers on the positive edge of the clock.

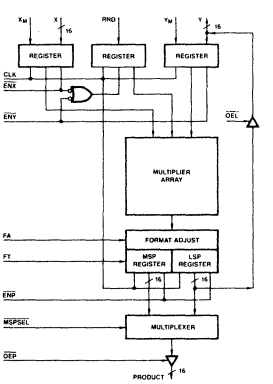
LOGIC DIAGRAMS

Am29516/29516A



MPL-011

Am29517/29517A



MPL-012

IMOX is a trademark of Advanced Micro Devices.

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0 to +70°C V_{CC} = 5.0V ±5% (MIN = 4.75V MAX = 5.25V)
MIL T_C = −55 to +125°C V_{CC} = 5.0V ±10% (MIN = 4.50V MAX = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	V_{IL} = .8V, V_{IH} = 2.0V	I_{OH} = −0.4mA	2.4	2.7		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	V_{IL} = .8V, V_{IH} = 2.0V, I_{OL} = 4.0mA			.3	.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			.8	Volts
				COM'L			.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V					−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.4V					75	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1	mA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = MAX	Product	V_O = 2.4V			25	μA
				V_O = 0.4V			−25	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX	Y	V_O = 0V	−3		−30	mA
			Product	V_O = 0V	−3		−30	
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX	COM'L and MIL	T_A = 25°C		600	(Note 5)	mA
			COM'L Only	T_A = 0 to +70°C			800	
				T_A = +70°C			750	
			MIL Only	T_C = −55 to +125°C			900	
				T_C = +125°C			800	

Notes:
1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $\overline{OEP}$ and $\overline{OEL}$ LOW with all product (MSP and LSP) bits LOW.
5. Low power multiplier, Am29L516/L517 also available.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature Under Bias − T_C	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

Am29516/517
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description		29516/517 T_A = 25°C V_{CC} = 5.0V Typ	29516/517 T_A = 0 to +70°C V_{CC} = 5V ±5% (Note 1) Min	Max	29516/517 MIL T_C = −55 to +125°C V_{CC} = 5V ± 10% Min	Max	29516-1/517-1 29516A/517A T_A = 0 to +70°C V_{CC} = 5V ±5% (Note 1) Min	Max	Units	Test Conditions
t_{MUC}	Unclocked Multiply Time		50		85		95			ns	
t_{MC}	Clocked Multiply Time		40		65		75			ns	
t_S	X_i, Y_i, RND Setup Time		10	20		25				ns	
t_H	X_i, Y_i, RND Hold Time		0	3		3				ns	
t_{PWH}	Clock Pulse Width High		10	15		15				ns	Load 1
t_{PWL}	Clock Pulse Width Low		10	20		15				ns	
t_{PDSEL}	$\overline{MSPSEL}$ to Product Out		20		30		35			ns	
t_{PDP}	Output Clock to P		20		30		35			ns	
t_{PDY}	Output Clock to Y		20		30		35			ns	
t_{PHZ}	$\overline{OEP}$ Disable Time	High to Z	12		23		28			ns	
t_{PLZ}		Low to Z	15		23		28			ns	
t_{PZH}	$\overline{OEP}$ Enable Time	Z to High	25		40		45			ns	
t_{PZL}		Z to Low	25		40		45			ns	Load 2
t_{PHZ}	$\overline{OEL}$ Disable Time	High to Z	12		20		22			ns	
t_{PLZ}		Low to Z	15		23		28			ns	
t_{PZH}	$\overline{OEL}$ Enable Time	Z to High	25		40		45			ns	
t_{PZL}		Z to Low	25		40		45			ns	
t_S	Clock Enable Setup Time (Am29517 Only)		5	10		15				ns	
t_H	Clock Enable Hold Time (Am29517 Only)		0	3		3				ns	Load 1
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML (see Note 2) (Am29516 Only)		0	0		0				ns	

Notes: 1. Switching Characteristics are measured and guaranteed for T_A as specified with 200 Lf/min flowing across the device.
2. To ensure that the correct product is entered in the output registers, new data may not be entered into the input registers before the output registers have been clocked.

DEFINITION OF TERMS

$X_{15}-X_0$ Multiplicand Data inputs.

$Y_{15}-Y_0$ Multiplier Data inputs or least significant product (LSP) output.

P_0-P_{15} LSP product port when $\overline{MSPSEL}$ is (High).

$P_{16}-P_{31}$ MSP product port when $\overline{MSPSEL}$ is (Low).

X_M, Y_M (TCX, TCY)* Mode control inputs for each data word; LOW for unsigned data and HIGH for two's complement data.

FA (RS)* Format adjust control selects either a full 32-bit product (HIGH) or a left shifted 31-bit product with the sign bit replicated in the LSP (LOW). This control is normally high, except for certain fractional two's complement applications. (See Multiplier output formats table).

FT Feedthrough control (HIGH) makes both MSP and LSP registers transparent.

$\overline{MSPSEL}$ Selects either MSP (LOW) or LSP (HIGH) to be available at the product output port.

*TRW MPY 16HJ pin designation.

RND Control for rounding the MSP. Adds a binary one to the most significant bit of the LSP for two's complement and unsigned numbers. Rounding occurs before format adjust. (RND = High).

$\overline{OEP}$ (TRIM)* Three-state enable for product output port.

$\overline{OEL}$ (TRIL)* Three-state enable for routing LSP through Y input/output port.

Am29516 ONLY

CLKX Register Clock, X_{15-0}, X_M, RND

CLKY Register Clock, Y_{15-0}, Y_M, RND

CLKM MSP Register Clock

CLKL LSP Register Clock

Am29517 ONLY

CLK Clock, All Registers

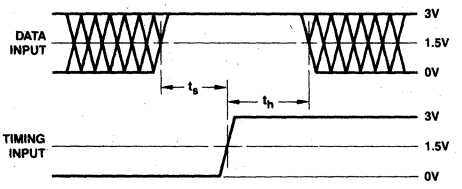
$\overline{ENX}$ Register Enable, X_{15-0}, X_M, RND

$\overline{ENY}$ Register Enable, Y_{15-0}, Y_M, RND

$\overline{ENP}$ Register Enable MSP, LSP

7

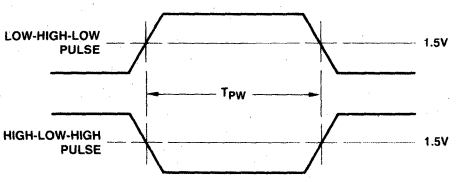
SET-UP AND HOLD TIME



MPL-013

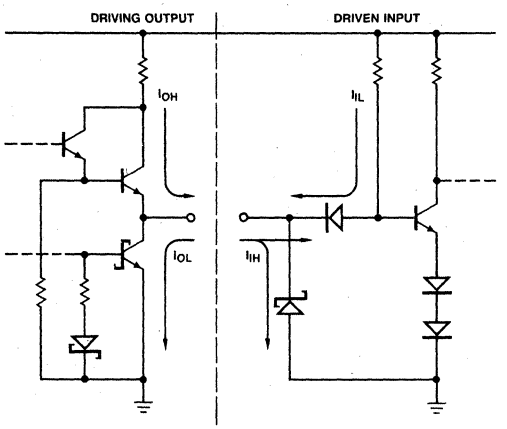
Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

PULSE WIDTH



MPL-014

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



MPL-015

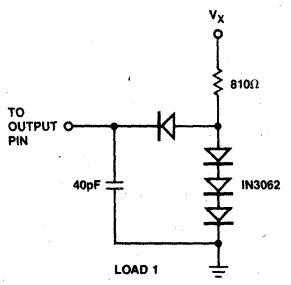
TEST WAVEFORMS

Test	V_X	Output Waveform – Measurement Level
All t_{PD}s	V_{CC}	V_{OH}, V_{OL}, 1.5V
t_{PHZ}	0.0V	V_{OH}, 0.5V, 0.0V
t_{PLZ}	2.6V	2.6V, 0.5V, V_{OL}
t_{PZH}	0.0V	V_{OH}, .5V, 0.0V
t_{PZL}	2.6V	2.6V, .5V, V_{OL}

MPL-016

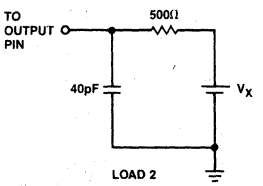
TEST LOADS FOR DELAY MEASUREMENTS

Normal Load



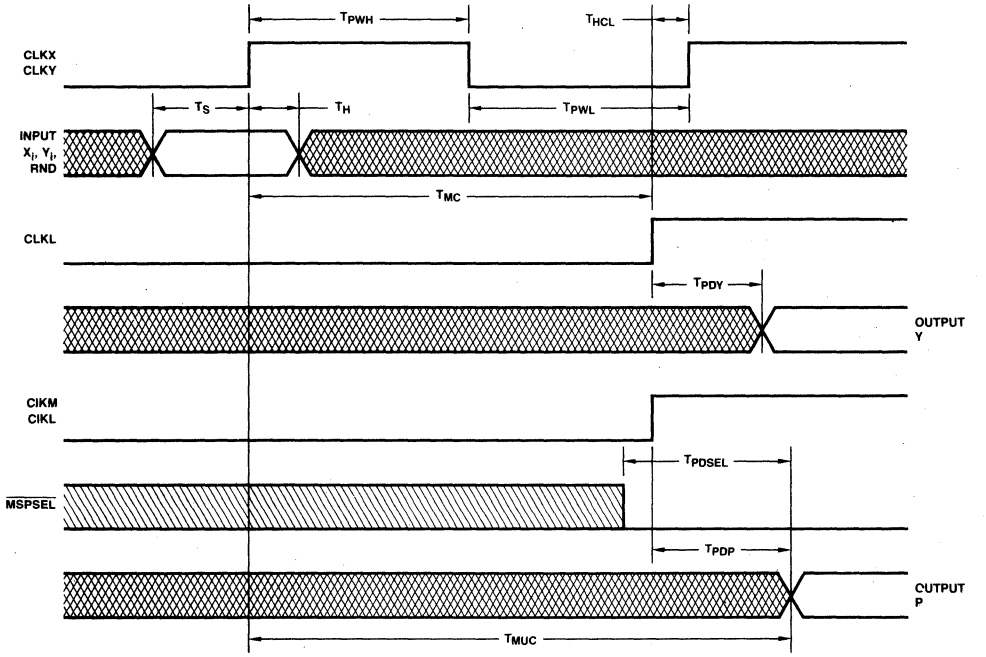
MPL-017

Three-State Delay Load



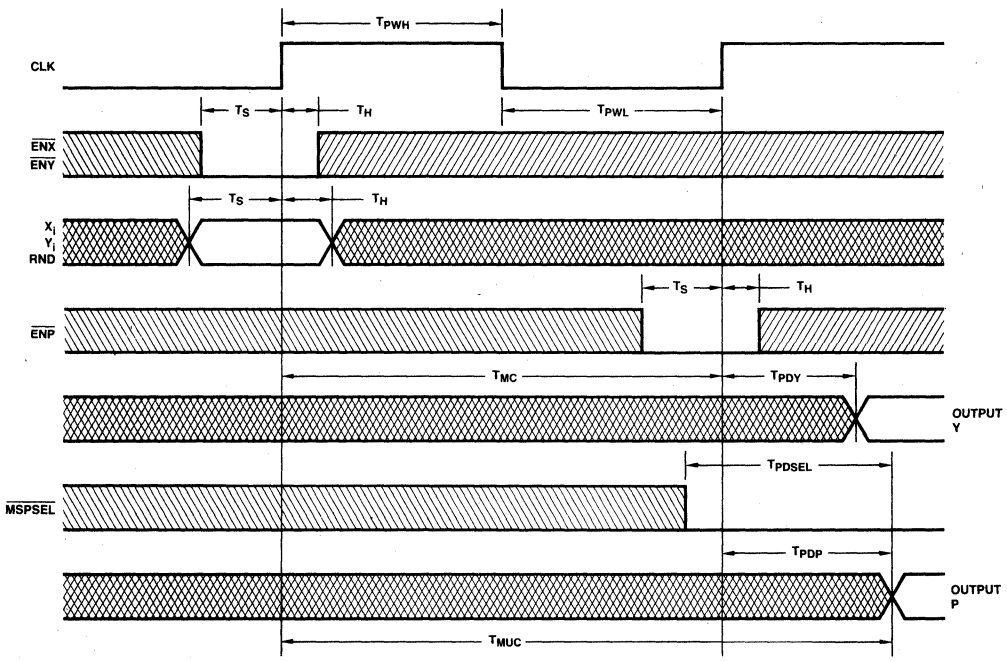
MPL-018

Am29516/29516A TIMING DIAGRAM



MPL-019

Am29517/29517A TIMING DIAGRAM



MPL-020

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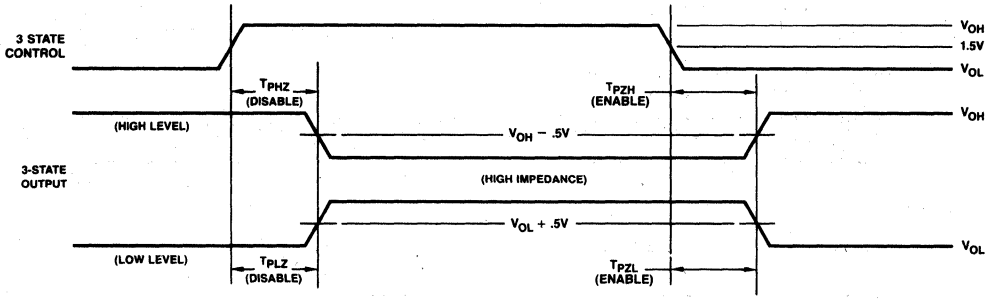
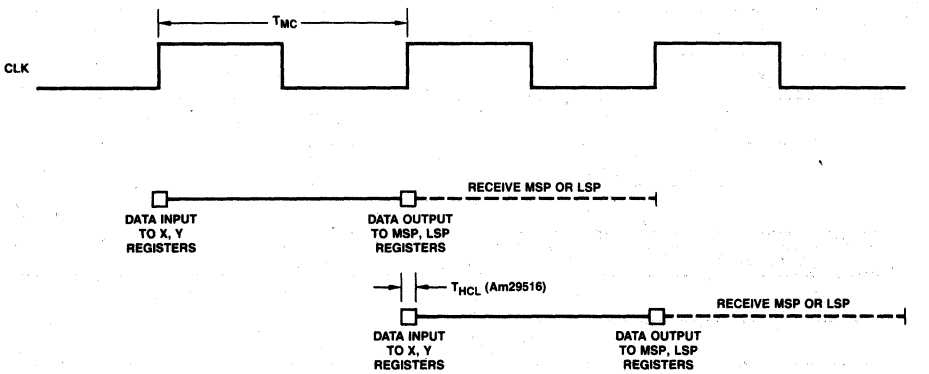
Am29516/29516A
Am29517/29517A
3-STATE
TIMING DIAGRAM



MPL-021

Am29516/29516A
Am29517/29517A
SIMPLIFIED TIMING DIAGRAM
TYPICAL APPLICATION

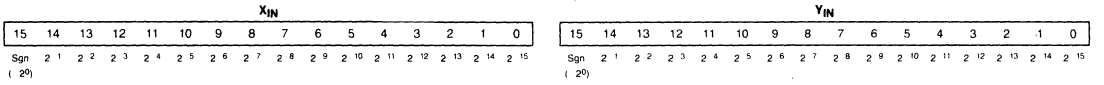


MPL-022

Am29516 • Am29517
INPUT FORMATS

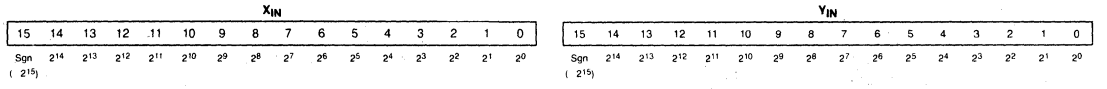
$X_M, Y_M = 1$

Fractional Two's Complement Input Format



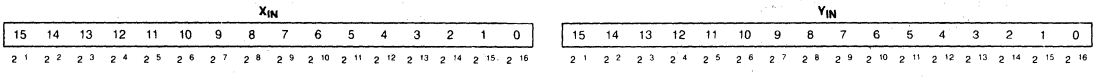
$X_M, Y_M = 1$

Integer Two's Complement Input Format



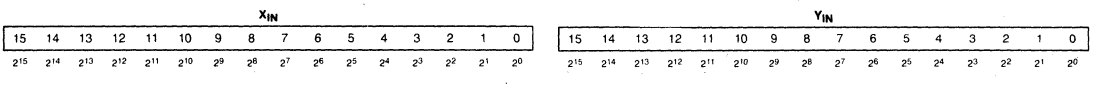
$X_M, Y_M = 0$

Unsigned Fractional Input Format



$X_M, Y_M = 0$

Unsigned Integer Input Format



MPL-023

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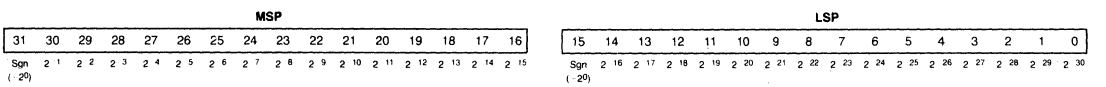
Am29516 • Am29517
OUTPUT FORMATS

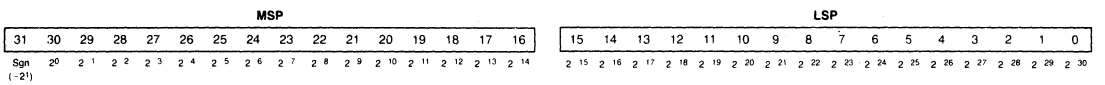
FA = 0

Fractional 2's Complement (Shifted)* Output



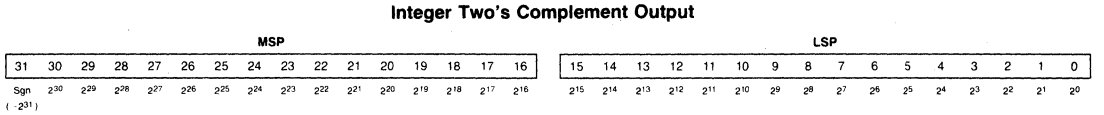
FA = 1

Fractional 2's Complement Output



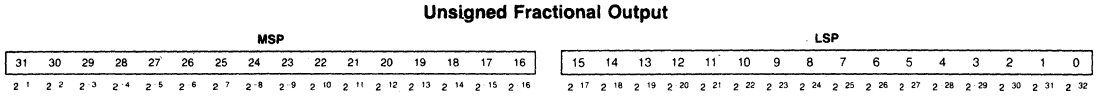
FA = 1

Integer Two's Complement Output



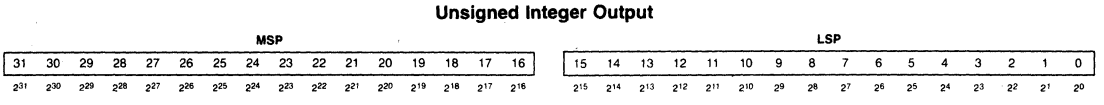
FA = 1

Unsigned Fractional Output



FA = 1

Unsigned Integer Output

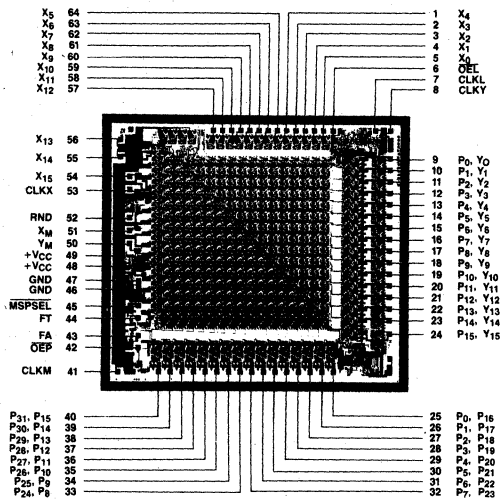


*In this format an overflow occurs in the attemped multiplication of the two's complement number 1.000 ... (−1) with itself, yielding a product of 1.000 ... or −1

MPL-024

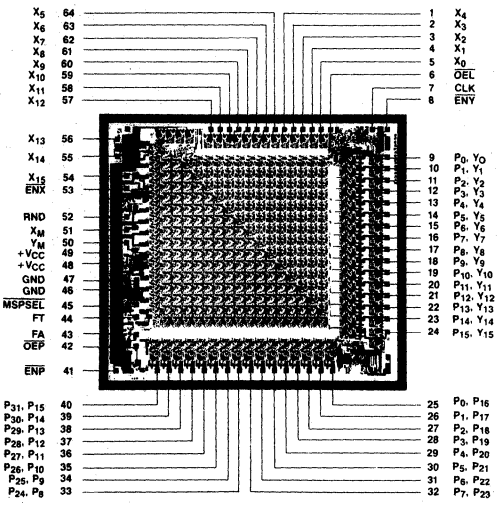
METALLIZATION AND PAD LAYOUTS

Am29516



MPL-069

Am29517



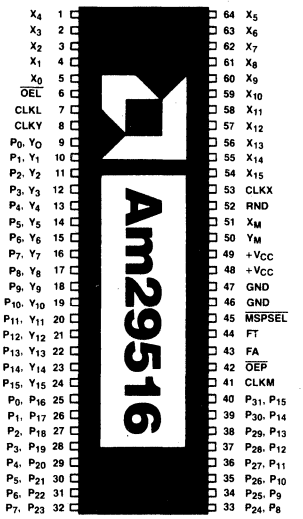
MPL-070

DIE SIZE: 250 X 222 Mils

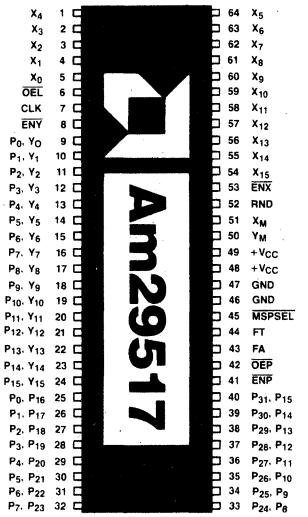
Am29516A

Am29517A

CONNECTION DIAGRAMS
Top Views
D-64-3



MPL 071



MPL-072

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ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Am29516 Order Number	Am29517 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM29516DC	AM29517DC	D-64	C	C-1
AM29516ADC	AM29517ADC	D-64	C	C-1
AM29516DCB	AM29517DCB	D-64	C	B-2 (Note 4)
AM29516ADCB	AM29517ADCB	D-64	C	B-2 (Note 4)
AM29516DM	AM29517DM	D-64	M	C-3
AM29516ADM	AM29517ADM	D-64	M	C-3
AM29516DMB	AM29517DMB	D-64	M	B-3
AM29516ADMB	AM29517ADMB	D-64	M	B-3
AM29516LC	AM29517LC	L-68	C	C-1
AM29516ALC	AM29517ALC	L-68	C	C-1
AM29516LM	AM29517LM	L-68	M	C-3
AM29516ALM	AM29517ALM	L-68	M	C-3
AM29516LMB	AM29517LMB	L-68	M	B-3
AM29516ALMB	AM29517ALMB	L-68	M	B-3

Notes: 1. D = Hermetic DIP, L = Chip-Pak. Number following letter is number of leads.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 160 hour burn-in.

Am29516/17 Application Note

32 x 32 Multiplier

The Am29516/17 is 16 x 16-bit High-Speed Multiplier. Many applications, however, require larger word widths, thus larger multipliers. A 32 x 32-bit multiplier can be constructed using 16 x 16-bit multipliers.

To multiply two 32-bit data words, each data word is divided into two 16-bit portions. The two 16-bit halves represent the most significant and least significant halves of the full 32-bit data words.

Let

x = 32-bit data word

y = 32-bit data word

$x = 2^{16}A + 2^{0}B$

$y = 2^{16}C + 2^{0}D$

The product of the two 32-bit words is a cross product of x and y:

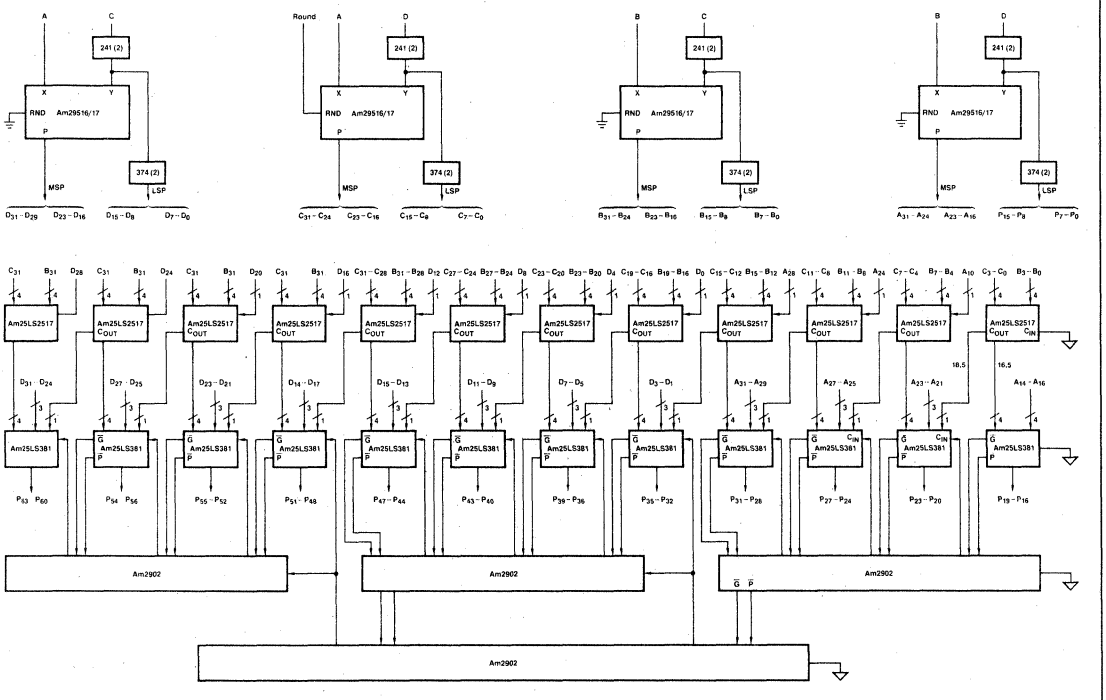
$$x * y = (2^{16}A + 2^{0}B) * (2^{16}C + 2^{0}D)$$

$$= 2^{32}(AC) + 2^{16}(AD) + 2^{16}(BD) + 2^{0}(BD)$$

Performing this algorithm using 16 x 16-bit multipliers is as simple as multiplying each of the partial products separately and then adding them.

A primary characteristic of many applications is speed. Figure 1 shows the architecture for a single cycle 32 x 32-bit multiplier using four Am29516/17s and an array of adders and carry-lookahead generators. This system performs a full 32 x 32-bit two's complement or unsigned multiply in a single clock cycle. Simpler architectures can be used to perform the same algorithm but would require multiple clock cycles.

Figure 1.



ABL-034

Am29520 • Am29521

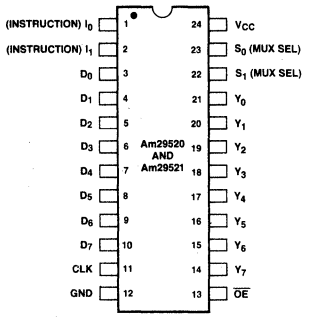
Multilevel Pipeline Registers

DISTINCTIVE CHARACTERISTICS

- Four 8-bit high speed registers
- Dual two-level or single four-level push-only stack operation
- All registers available at multiplexed output
- Hold, transfer and load instructions
- Provides temporary address or data storage
- 24-pin 0.3" package

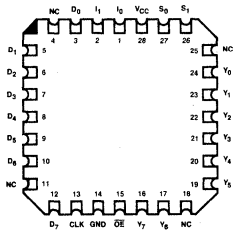
CONNECTION DIAGRAMS
Am29520/21

D-24-Slim



MPL-003

Chip-Pak™ L-28-1



Note: Pin 1 is marked for orientation

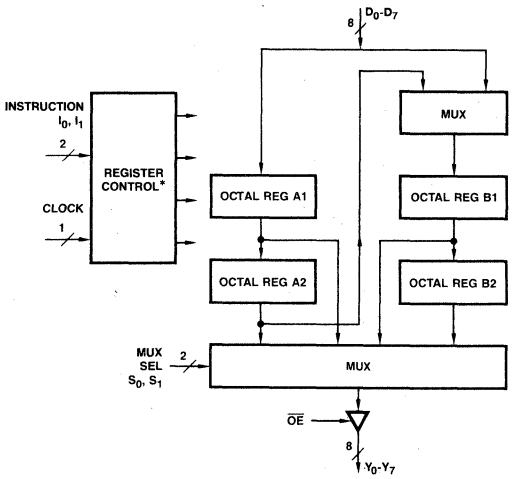
MPL-061

FUNCTIONAL DESCRIPTION

The Am29520 and Am29521 each contain four 8-bit positive edge-triggered registers. These may be operated as a dual 2-level pipeline or as a single 4-level pipeline. A single 8-bit input is provided and all four registers are available at the 8-bit, 3-state output.

The Am29520 and Am29521 differ only in the way data is loaded into and between the registers in dual 2-level operation. This difference is illustrated in Figure 1. In the Am29520 when data is entered into the first level (I=2 or I=1) the existing data in the first level is moved to the second level. In the Am29521 these instructions simply cause the data in the first level to be overwritten. Transfer of data to the second level is achieved using the 4-level shift instruction (I=0). This transfer also causes the first level to change. In either part I=3 is a NO-OP.

LOGIC DIAGRAM



*Multilevel Pipeline Register

MPL-001

RELATED PRODUCTS

Part No.	Description
Am29540	FFT Address Sequencer
Am29116	16-bit Bipolar Microprocessor
Am2925	System Clock Generator and Driver
Am29517	16 x 16-bit High Speed Multiplier
Am29510	16 x 16-bit Multiply Accumulator
Am6108	8-bit Microprocessor Compatible A/D Converter
Am9128-70	2K x 8 Static RAM
Am21L47-55	4K x 1 Static RAM

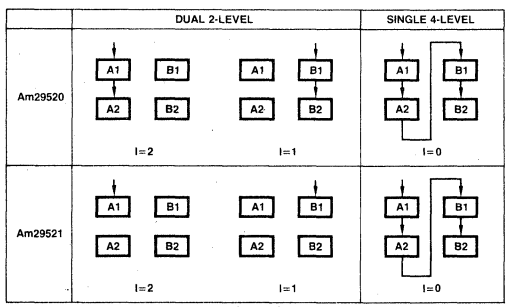


Figure 1. **I=3 NO-OP**

MPL-002

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Am29520/521

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0 to +70°C V_{CC} = 5.0V ±5% (MIN = 4.75V MAX = 5.25V)
MIL T_C = −55 to +125°C V_{CC} = 5.0V ±10% (MIN = 4.50V MAX = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −6.5mA (COM'L)		2.4			Volts
			I_{OH} = −2.0mA (MIL)		2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA				0.45	Volts
			I_{OL} = 20mA				0.50	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V	$\overline{OE}$				−2.0	mA
			Other Inputs				−0.4	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V					50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = MAX		V_O = 2.7V			50	μA
				V_O = 0.4V			−50	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−30		−100	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX	COM'L and MIL	T_A = 25°C		125		mA
			COM'L Only	T_A = 0 to +70°C			185	
				T_A = +70°C			155	
			MIL Only	T_C = −55 to +125°C			200	
				T_C = +125°C			150	

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All inputs LOW.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature Under Bias − T_C	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

DEFINITION OF TERMS

D_0-D_7 Register input port

CLK Clock input enter data into registers on LOW-to-HIGH transitions

I_0, I_1 Instruction inputs. See Figure 1 and Instruction Control Tables.

S_0, S_1 Multiplexer select inputs select either register A_1, A_2, B_1 or B_2 data to be available at the output port

$\overline{OE}$ Output enable for 3-state output port

Y_0-Y_7 Register output port

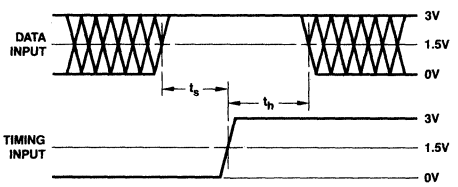
Am29520/29521
SWITCHING CHARACTERISTICS
OVER OPERATING RANGE

						COM'L		MIL			
			T_A = 25°C V_{CC} = 5.0V			T_A = 0 to 70°C V_{CC} = 5V ±5%		T_C = −55 to +125°C V_{CC} = 5V ±10%			
Parameters		**Description**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Test Conditions**
t_{PD}	t_{PLH}	Clock to Data Output		12	18		21		24	ns	R_L = 280Ω C_L = 50pF
	t_{PHL}			12	20		22		24	ns	
t_{PDSEL}	t_{PLH}	S_0, S_1 to Data		12	18		20		22	ns	
	t_{PHL}	Output		12	18		20		22	ns	
t_S		Input Data to Clock	10			10		10		ns	
t_H			3			3		3			
t_S		Instruction (Register	10			10		10		ns	
t_H		Enable) to Clock	3			3		3			
t_{PHZ}		$\overline{OE}$ to Output		5	11		13		14	ns	C_L = 5pF
t_{PLZ}		$\overline{OE}$ to Output		6	13		15		16	ns	C_L = 5pF
t_{PZH}		$\overline{OE}$ to Output		12	18		20		22	ns	R_L = 280Ω C_L = 50pF
t_{PZL}		$\overline{OE}$ to Output		13	20		21		22	ns	
t_{PWH}		Clock Pulse Width HIGH	10			10		10		ns	
t_{PWL}		Clock Pulse Width LOW	10			10		10		ns	

Note: Please refer to *Guidelines for Testing Am2900 Family Devices* in Section 13 of this data book.

7

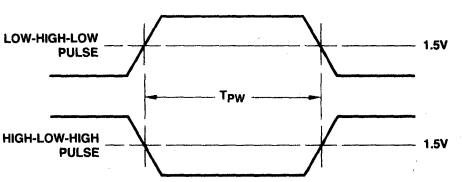
SET-UP AND HOLD TIME



Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

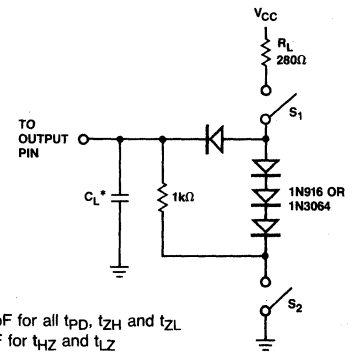
MPL-004

PULSE WIDTH



MPL-005

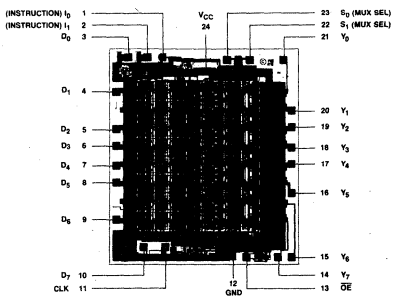
TEST LOADS FOR DELAY MEASUREMENTS



*C_L = 50pF for all t_{PD}, t_{ZH} and t_{ZL}
C_L = 5pF for t_{HZ} and t_{LZ}

MPL-008

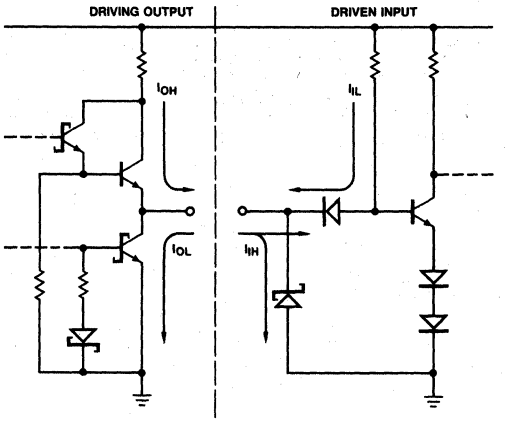
CHIP TOPOGRAPHY
Am29520/21



DIE SIZE: 0.117" X 0.131"

MPL-062

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



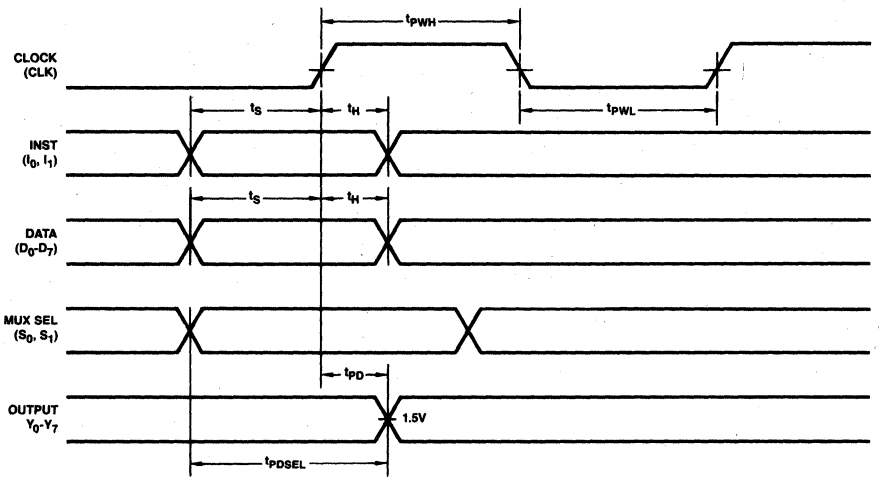
MPL-006

TEST WAVEFORMS

Test	Output Waveform – Measurement Level	
All t_{PDS}	V_{OH}, V_{OL}, 1.5V	S_1 Closed S_2 Closed
t_{PHZ}	V_{OH}, 0.5V, ≈ 1.5V	S_1 Closed S_2 Closed
t_{PLZ}	≈ 1.5V, 0.5V, V_{OL}	S_1 Closed S_2 Closed
t_{PZH}	V_{OH}, 1.5V, 0.0V	S_1 Open S_2 Closed
t_{PZL}	V_{CC}, 1.5V, V_{OL}	S_1 Closed S_2 Open

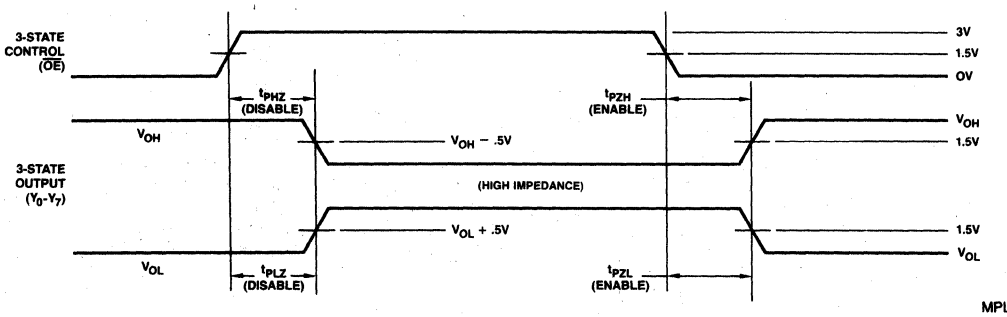
MPL-007

Am29520/21 TIMING DIAGRAM



MPL-009

Am29520/21 THREE-STATE TIMING



MPL-010

DATA OUTPUT SELECT

S_1	S_0	OUTPUT
H	H	A1
H	L	A2
L	H	B1
L	L	B2

Am29520 INSTRUCTIONS

				Register Contents After Clock t_n			
Inst	**Mnemonic**	I_1	I_0	$A1_n$	$A2_n$	$B1_n$	$B2_n$
0	SHFT	L	L	D	$A1_{n-1}$	$A2_{n-1}$	$B1_{n-1}$
1	LDB	L	H	$A1_{n-1}$	$A2_{n-1}$	D	$B1_{n-1}$
2	LDA	H	L	D	$A1_{n-1}$	$B1_{n-1}$	$B2_{n-1}$
3	HLD	H	H	$A1_{n-1}$	$A2_{n-1}$	$B1_{n-1}$	$B2_{n-1}$

Am29521 INSTRUCTIONS

				Register Contents After Clock t_n			
Inst	**Mnemonic**	I_1	I_0	$A1_n$	$A2_n$	$B1_n$	$B2_n$
0	SHFT	L	L	D	$A1_{n-1}$	$A2_{n-1}$	$B1_{n-1}$
1	LDB	L	H	$A1_{n-1}$	$A2_{n-1}$	D	$B2_{n-1}$
2	LDA	H	L	D	$A2_{n-1}$	$B1_{n-1}$	$B2_{n-1}$
3	HLD	H	H	$A1_{n-1}$	$A2_{n-1}$	$B1_{n-1}$	$B2_{n-1}$

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ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Am29520 Order Number	Am29521 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM29520DC	AM29521DC	D-24-SLIM	C	C-1
AM29520DCB	AM29521DCB	D-24-SLIM	C	B-2 (Note 4)
AM29520DM	AM29521DM	D-24-SLIM	M	C-3
AM29520DMB	AM29521DMB	D-24-SLIM	M	B-3
AM29520LC	AM29521LC	L-28	C	C-1
AM29520LM	AM29521LM	L-28	M	C-3
AM29520LMB	AM29521LMB	L-28	M	B-3

Notes: 1. D = Hermetic DIP, L = Chip-Pak. Number following letter is number of leads.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 160 hour burn-in.

APPLICATIONS

The IMOX™ Am29520 and Am29521 multilevel pipeline registers are specifically designed as a temporary address storing register for array processing and digital signal processing applications using the Am29500 Family.

In AP/DSP applications a single data address may be used a multiple number of times. The multilevel pipeline register allows saving addresses within its registers for use at a later time.

Below are a number of applications where the use of a multilevel pipeline register can be implemented.

CLOCK CONTROLLER, BYTE-WIDE DELAY LINE/SHIFT REGISTER

The Am29520/21 can be utilized as a byte-wide shaft register (Figure 1a) capable of delaying a byte of data from one to four clock cycles. The number of delay cycles is controlled by the S_0, S_1 control inputs and can be changed by the user without interrupting the data flow.

Figure 1b shows the contents of all Am29520/21 registers during each clock cycle. With the instruction input set at I = 0, the operation performed is that of a byte-wide shift register. The contents of any register can be accessed by appropriately setting S_0, S_1. In this example, D_1 input data is presented after the clock 0 rising edge. At the clock 1 rising edge, the D_1 data is loaded into A_1. At the clock 2 rising edge, the D_2 data is loaded in A_1 and the D_1 data is pushed into A_2. This action continues as long as clocks are provided (this is a static part; therefore, interrupting the clock does not cause data to be lost). Data pushed out of B_2 is lost. The user determines the delay by setting the output MUX to one of the four registers via S_0, S_1 controls. In this example, register B_1 was selected (S_0, S_1 = 10). The data at the Am29520/21 output is delayed by three clock cycles.

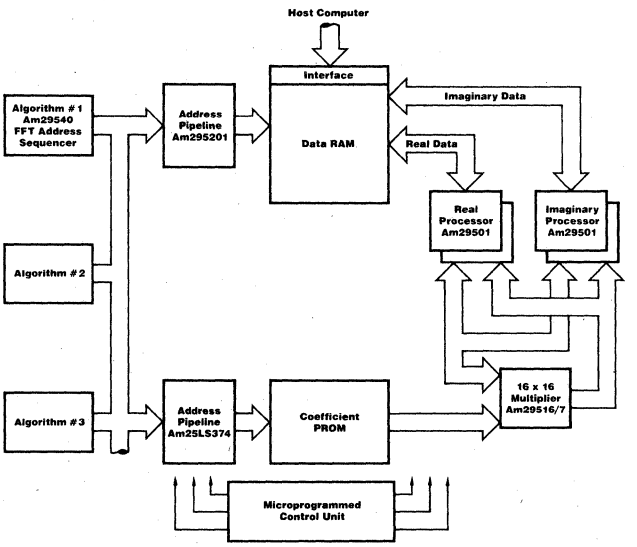


Figure 1a. Block Diagram

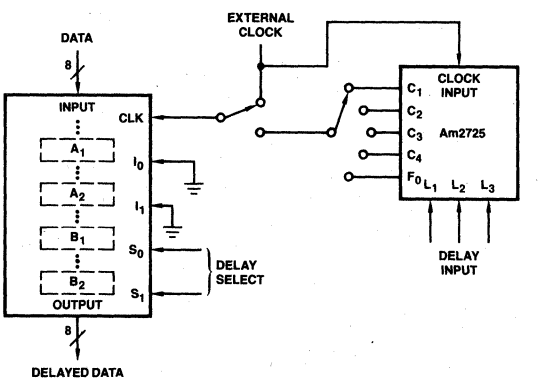
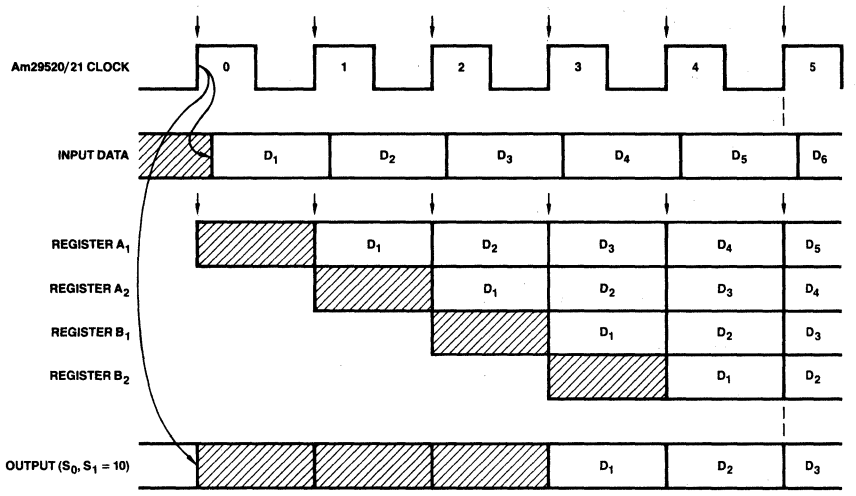
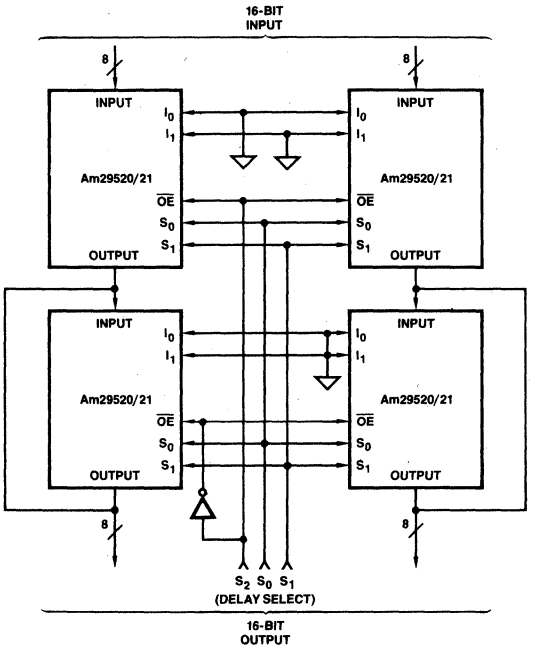


Figure 1b. Timing Diagram



MPL-065

Figure 2. Am29520/21 Expansion in Width and Depth



MPL-066

Since the output is capable of three-state, a no-delay operation occurs if the input is tied to the output and OE = 1.

The Am29520/21 is easily expandable to accommodate data widths of 16, 24, 32, etc. bits and delays of 8, 12, 16, etc. clock cycles as shown in Figure 2.

If greater delays are required by cascading devices are not acceptable, then consider controlling the clock input to the Am29520/21. An example of this is shown in Figure 1a. In this case, an Am2925 clock generator provides the clock inputs to the Am29520/21 (see Am2925 Data Sheet). The Am2925 digital control inputs (L_1, L_2, L_3) allows the user to program the clock outputs to vary from $F_{0/3}$ to $F_{0/10}$ in eight steps (F_0 = input fundamental clock frequency input to the Am2925). The Am2925 provides four duty cycle outputs (C_1, C_2, C_3, C_4) for each of the eight multiples of the fundamental period. Table 1 is a matrix showing all combinations of the Am2925 L_1, L_2, L_3 and the Am29520/21 S_0, S_1 controls. Twenty-four meaningful combinations are available providing from 1 to 40 clock delays.

TABLE 1. CLOCK DELAY SELECT MATRIX

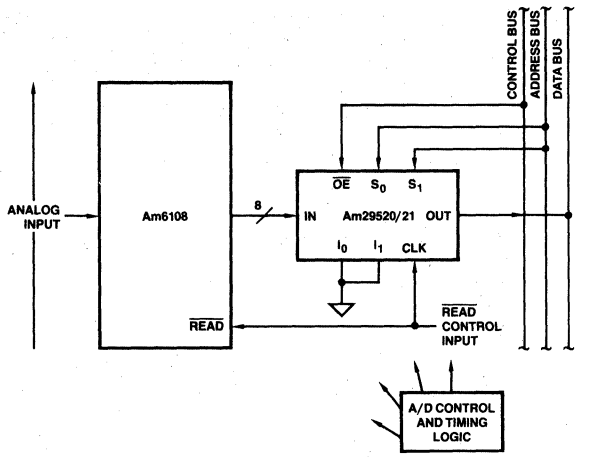
Am2925 Select Input		F_0	F_3	F_4	F_5	F_6	F_7	F_8	F_9	F_{10}
	L_1	X	0	1	1	1	1	0	0	0
Am29520/21	L_2	X	0	0	0	1	1	1	1	0
S_0, S_1 Input	L_3	X	0	0	1	1	0	0	1	1
1, 1 (A_1)		1	3	4	5	6	7	8	9	10
0, 1 (A_2)		2	6	8	10	12	14	16	18	20
1, 0 (B_1)		3	9	12	15	18	21	24	27	30
0, 0 (B_2)		4	12	16	20	24	28	32	36	40

ANALOG/DIGITAL BUFFER

In the example shown in Figure 7 the Am29520/21 acts as a 4-byte buffer between an A/D converter and a controller (or microprocessor). Four digitized samples are sequentially stored in the Am29520/21 from the A/D converter. This is accomplished by applying a READ control input to the clock input of the Am29520/21 as well as to the READ input of the A/D. Since I = 0, the data output from the A/D will be stored in the Am29520/21 as shown in Figure 8.

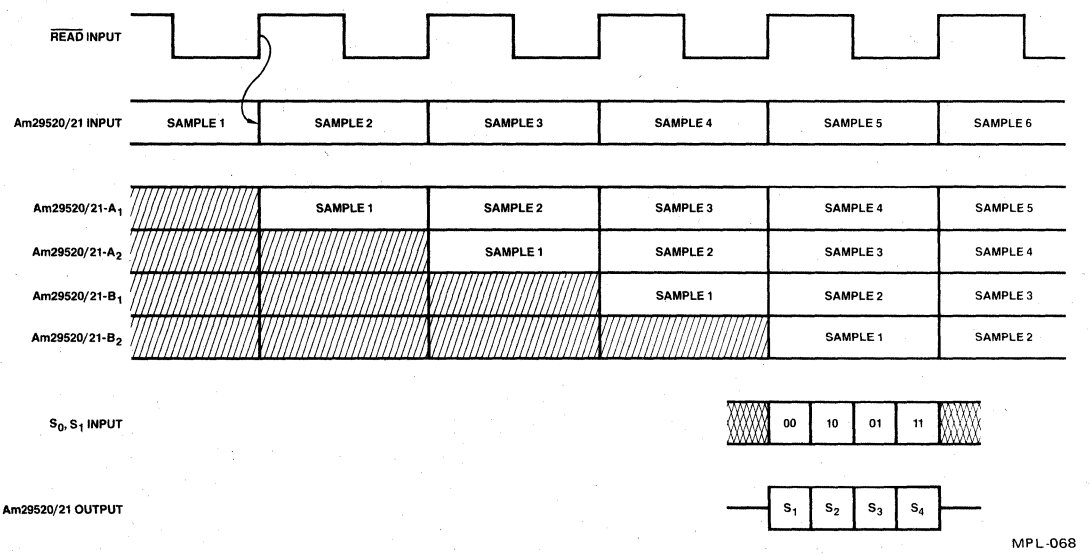
While the fifth sample is being acquired by the A/D, the controller will read all registers of the Am29520/21 by manipulating S_0, S_1. Note that the three-state output (controlled by OE) can be tied directly to a microprocessor bus and that the registers of the Am29520/21 can be easily memory mapped.

Figure 3. A/D Buffer



MPL-067

Figure 4. A/D Buffer Timing



MPL-068

The A/D will acquire four more samples before the Am29520/21 registers need to be read.

Note that the Am29520/21 can be simultaneously written and read. A two byte ping-pong memory is realizable by switching between I modes 1 and 2. While the A/D is writing registers B_1 and B_2, the microprocessor can be reading registers A_1 and A_2.

Also, note that the Am29520/21 is easily cascadable in width (as previously described) for applications involving 12-bit and 16-bit A/D converters.

Am29526 • Am29527
Am29528 • Am29529

High Speed Sine, Cosine Generators

DISTINCTIVE CHARACTERISTICS

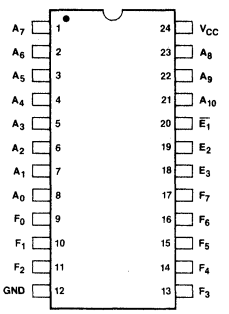
- Provides values for sine/cosine functions in $\pi/2048$ increments
- Outputs are 16-bit two's complement fractions
- Fast generation time of 50ns max Com'l
- S/LS compatible
- Three-state outputs
- IMOX™ processing

RELATED PRODUCTS

Part No.	Description
Am29516/17	16 x 16-Bit High Speed Multipliers
Am29510	16 x 16-Bit Multiply Accumulator
Am29540	FFT Address Sequencer
Am29825	High Performance 8-Bit Register

CONNECTION DIAGRAMS – Top Views

DIP



Chip-Pak™

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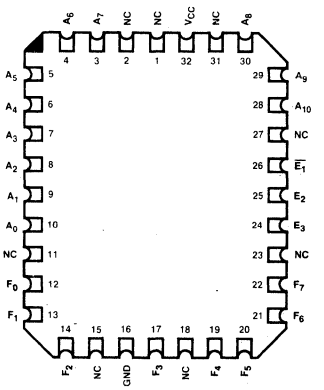


ABL-007

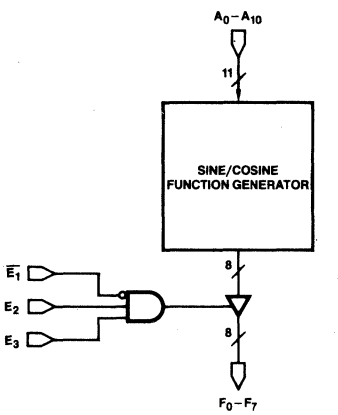
FUNCTIONAL DESCRIPTION

The Am29526/27 and Am29528/29 provide high speed generation of sine and cosine functions over the range $0 \leq \theta < \pi$ in increments of $\pi/2048$. θ is determined by an 11-bit input word. Each device provides an 8-bit output and two are used to give the full 16-bit value. The Am29526 and Am29527 generate the MS and LS bytes respectively for the sine function. Similarly, the Am29528 and Am29529 generate the cosine functions.

The outputs are fractional two's complement numbers with the radix point located immediately to the right of the sign bit (in between the bits weighted -2^{0} and 2^{-1}). As this format does not allow for the representation of $+1$ the functions generated are $-\sin\theta$ and $-\cos\theta$. In this way the output values are restricted to the range $-1 \leq f(\theta) < +1$ which is representable. The outputs are three-state with one active Low enable and two active High enable.

While providing general purpose sine and cosine function capability, the Am29526/27/28/29 satisfy the requirements of the Am29540 FFT Address Sequencer.

BLOCK DIAGRAM



ABL-008

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Am29526/27/28/29

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise specified:

COM'L T_A = 0 to +70°C V_{CC} = 5.0V ±5% (MIN = 4.75V MAX = 5.25V)
MIL T_C = −55 to +125°C V_{CC} = 5.0V ±10% (MIN = 4.50V MAX = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}				0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.45V			−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				25	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 2)	MIL	−15	−40	−90	mA
			COM'L	−20	−40	−90	
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX			115	185	mA
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX V_{CS} = 2.4V	V_O = V_{CC}			40	μA
			V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 3)			4.0		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 3)			8.0		

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = +25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) under Bias	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs	−0.5V to +V_{CC} max
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

DEFINITION OF FUNCTIONAL TERMS

$A_{10}-A_0$ **Data Input Values**
Input, θ, corresponding to θ = 0 (000) to 2047π/2048 (3FF). A_{10} is MSB.

$\overline{E}_1$, E_2, E_3 **Output Enables**
When $\overline{E}_1$ is Low and E_2 and E_3 are High, the outputs F_0-F_7 are enabled. Otherwise the outputs are in the high impedance state or off.

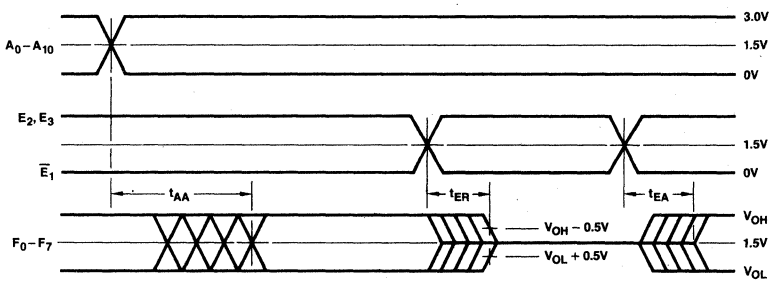
F_7-F_0 **Data Output Values**
The outputs corresponding to −sinθ or −cosθ. F_7 is MSB.

Am29526/27/28/29
SWITCHING CHARACTERISTICS
OVER OPERATING RANGE

Parameters	Description		COM'L $T_A = +25°C$, $V_{CC} = 5V$ Typ	COM'L $T_A = 0$ to $+70°C$, $V_{CC} = 5V \pm 5\%$ Max	MIL $T_C = -55$ to $+125°C$, $V_{CC} = 5V \pm 10\%$ Max	Units	Test Conditions
t_{PLH}	Sin/Cos Generation Time A_i to F_i		30	50	65	ns	$R_L = 600\Omega$, $C_L = 30pF$ (Notes 1 and 2)
t_{PHL}			30	50	65	ns	
t_{PHZ}	$\overline{E}_1, E_2, E_3$ Disable Time	High to Z	10	25	30	ns	
t_{PLZ}		Low to Z	10	25	30	ns	
t_{PZH}	$\overline{E}_1, E_2, E_3$ Enable Time	Z to High	10	25	30	ns	
t_{PZL}		Z to Low	10	25	30	ns	

Notes: 1. t_{PLH} and t_{PHL} are tested with switch S_1 closed and $C_L = 30pF$.
2. For three-state outputs, the disables time is tested with $C_L = 30pF$ to the 1.5V level; S_1 is open for Z to High test and closed for Z to Low test. The enable time is tested with $C_L = 5pF$. High to Z tests are made to an output voltage to $V_{OH} - 0.5V$ with S_1 open; Low to Z tests are made to the $V_{OL} - 0.5V$ level with S_1 closed.

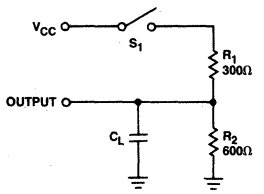
SWITCHING WAVEFORMS



Note: Level on output while chip is disabled is determined externally.

ABL-009

AC TEST LOAD



ABL-010

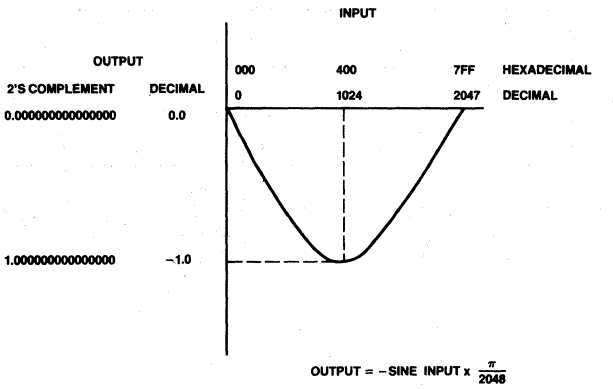
TABLE 1. $-COS(\theta)$ TABLE

Decimal Input	Actual Hexadecimal Input	Angle in Radians	Decimal Value of $-Cos(\theta)$	Hex Value of $-Cos(\theta)$	Am29526 MS Device	Am29527 LS Device
0	0	0	−1.000000	1000	10	00
512	200	$\pi/4$	−0.707107	A57E	A5	7E
1024	400	$\pi/2$	0.000000	0000	00	00
1536	600	$3\pi/4$	+0.707107	5A82	5A	82
2047	7FF	$2047\pi/2048$	+0.999999	7FFF	7F	FF

TABLE 2. $-SIN(\theta)$ TABLE

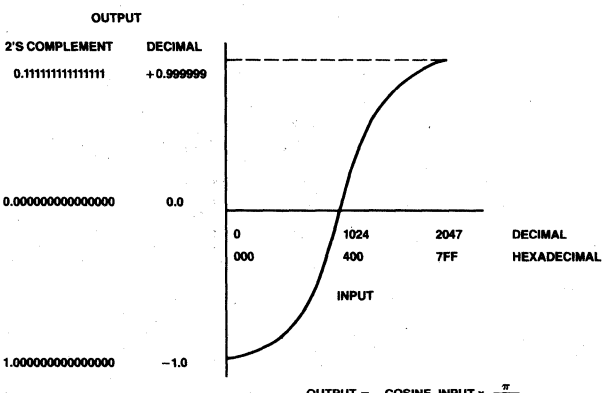
Decimal Input	Actual Hexadecimal Input	Angle in Radians	Decimal Value of $-Sin(\theta)$	Hex Value of $-Sin(\theta)$	Am29528 MS Device	Am29529 LS Device
0	000	0	0	0000	00	00
512	200	$\pi/4$	−0.707107	A57E	A5	7E
1024	400	$\pi/2$	−1.00000	8000	80	00
1536	600	$3\pi/4$	−0.707107	A57E	A5	7E
2047	7FF	$2047\pi/2048$	−0.001534	FFCE	FF	CE

Figure 1. The Minus Sine Function



ABL-011

Figure 2. The Minus Cosine Function



ABL-012

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 3)	Screening Level (Note 2)
AM29526PC	P-24-1AA	C	C-1
AM29527PC	P-24-1AA	C	C-1
AM29528PC	P-24-1AA	C	C-1
AM29529PC	P-24-1AA	C	C-1
AM29526PC-B	P-24-1AA	C	B-1
AM29527PC-B	P-24-1AA	C	B-1
AM29528PC-B	P-24-1AA	C	B-1
AM29529PC-B	P-24-1AA	C	B-1
AM29526DC	D-24-1AA	C	C-1
AM29527DC	D-24-1AA	C	C-1
AM29528DC	D-24-1AA	C	C-1
AM29529DC	D-24-1AA	C	C-1
AM29526DC-B	D-24-1AA	C	B-1
AM29527DC-B	D-24-1AA	C	B-1
AM29528DC-B	D-24-1AA	C	B-1
AM29529DC-B	D-24-1AA	C	B-1
AM29526DM	D-24-1AA	M	C-3
AM29527DM	D-24-1AA	M	C-3
AM29528DM	D-24-1AA	M	C-3
AM29529DM	D-24-1AA	M	C-3
AM29526DM-B	D-24-1AA	M	B-3
AM29527DM-B	D-24-1AA	M	B-3
AM29528DM-B	D-24-1AA	M	B-3
AM29529DM-B	D-24-1AA	M	B-3
AM29526LC	L-32-2	C	C-1
AM29527LC	L-32-2	C	C-1
AM29528LC	L-32-2	C	C-1
AM29529LC	L-32-2	C	C-1
AM29526LM	L-32-2	M	C-3
AM29527LM	L-32-2	M	C-3
AM29528LM	L-32-2	M	C-3
AM29529LM	L-32-2	M	C-3
AM29526LM-B	L-32-2	M	B-3
AM29527LM-B	L-32-2	M	B-3
AM29528LM-B	L-32-2	M	B-3
AM29529LM-B	L-32-2	M	B-3

Notes: 1. P = Molded DIP, D = Hermetic DIP, L = Chip-Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
3. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.

7

Am29540

Programmable FFT Address Sequencer

ADVANCED DATA

DISTINCTIVE CHARACTERISTICS

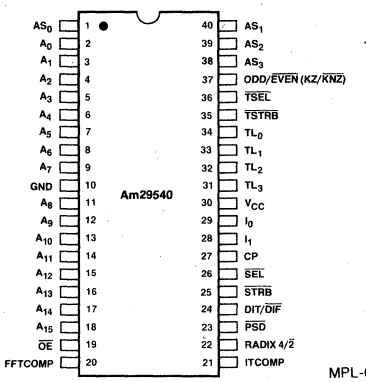
- Generates data and coefficient addresses
- Programmable transform length 2 to 65,536 points
- Radix-2 or Radix-4
- Decimation in frequency (DIF) or decimation in time (DIT) FFT algorithms supported
- In-place or non-in-place transformation
- 40-pin DIP package
- 5 volt single supply

RELATED PRODUCTS

Am29520/521 – Multilevel pipeline register
Am29825 – High performance 8-bit register

CONNECTION DIAGRAM

Top View



MPL-046

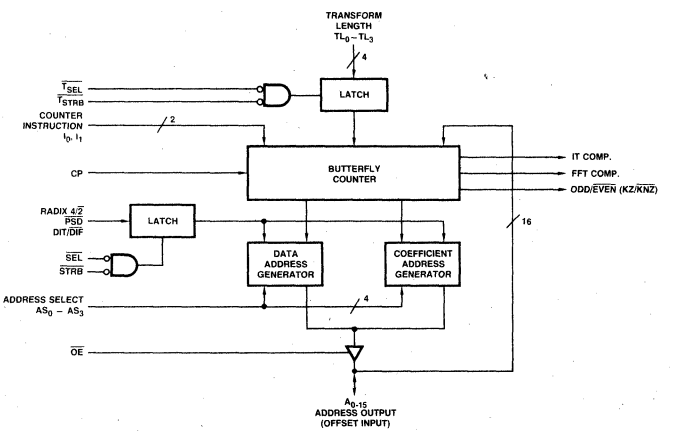
FUNCTIONAL DESCRIPTION

The Am29540 Fast Fourier Transform Address Sequencer generates all the data (RAM) and coefficient (ROM) addresses necessary to perform the repetitive butterfly operations of the FFT. Decimation in time and decimation in frequency algorithms are supported (control DIT/$\overline{\text{DIF}}$) in radix-2 or radix-4 (RADIX 4/$\overline{2}$). A radix-2 real valued input (RVI) transform is also supported. For radix-2 operation the transform length is programmable in powers of 2 from 2 to 65,536 points. In radix-4 the range is 4 to 65,536 in powers of 4.

Address sequences can be selected to be compatible with data which may or may not have been pre-scrambled ("bit-reversed"). If the data has been pre-scrambled the control $\overline{\text{PSD}}$ must be LOW to select the correct sequence. If the data is not pre-scrambled ($\overline{\text{PSD}}$ HIGH) and an in-place transform is performed, the output data will necessarily be in bit-reversed order. If this is not desirable, alternate addresses are available for a non-in-place, non-bit-reversing algorithm.

The butterfly counter operates on the positive clock edge and responds to four instructions. COUNT causes the counter to increment to the next butterfly. RESET causes the counter to initialize for the specified transform length. RESET/LOAD causes the counter to initialize and a data address offset to be loaded into the part via the bi-directional 3-state ADDRESS port. This offset is effectively OR-ed onto the higher significance bits of the address which are unused for the selected transform length. A HOLD instruction is also provided. Three status lines are provided. ODD/EVEN (KZ/$\overline{\text{KNZ}}$) controls the alternation of read and write memories for non-in-place transforms and determines the butterfly structure in the RVI transform. The flag has the function KZ/$\overline{\text{KNZ}}$ when RVI data addresses are selected (AS = 12 to 15). Iteration complete (IT COMP) flags the bottom of a "column" of butterflies and is used in conjunction with block floating point schemes. FFT COMP identifies the last butterfly of the transform.

LOGIC DIAGRAM



FFT Address Sequencer

MPL-033

Am29540

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0 to +70°C V_{CC} = 5.0V ±5% (MIN = 4.75V MAX = 5.25V)
MIL T_C = −55 to +125°C V_{CC} = 5.0V ±10% (MIN = 4.50V MAX = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}		I_{OH} = −2.6mA, COM'L	2.4			Volts
				I_{OH} = −1mA, MIL				
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}		I_{OL} = 12mA			0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.8	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V					−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V					20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V (See Note 5)					100	μA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = MAX		V_O = 3V				μA
				V_O = 0.5V				
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−30		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX	COM'L and MIL	T_A = 25°C				mA
			COM'L Only	T_A = 0 to +70°C				
				T_A = +70°C				
			MIL Only	T_C = −55 to +125°C				
				T_C = +125°C				

Notes:
1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $\overline{OE}$ LOW and all inputs LOW.
5. It is limited to 5.5V because A_0 to A_{15} inputs also connect to output transistors.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature Under Bias − T_C	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

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Am29540
SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

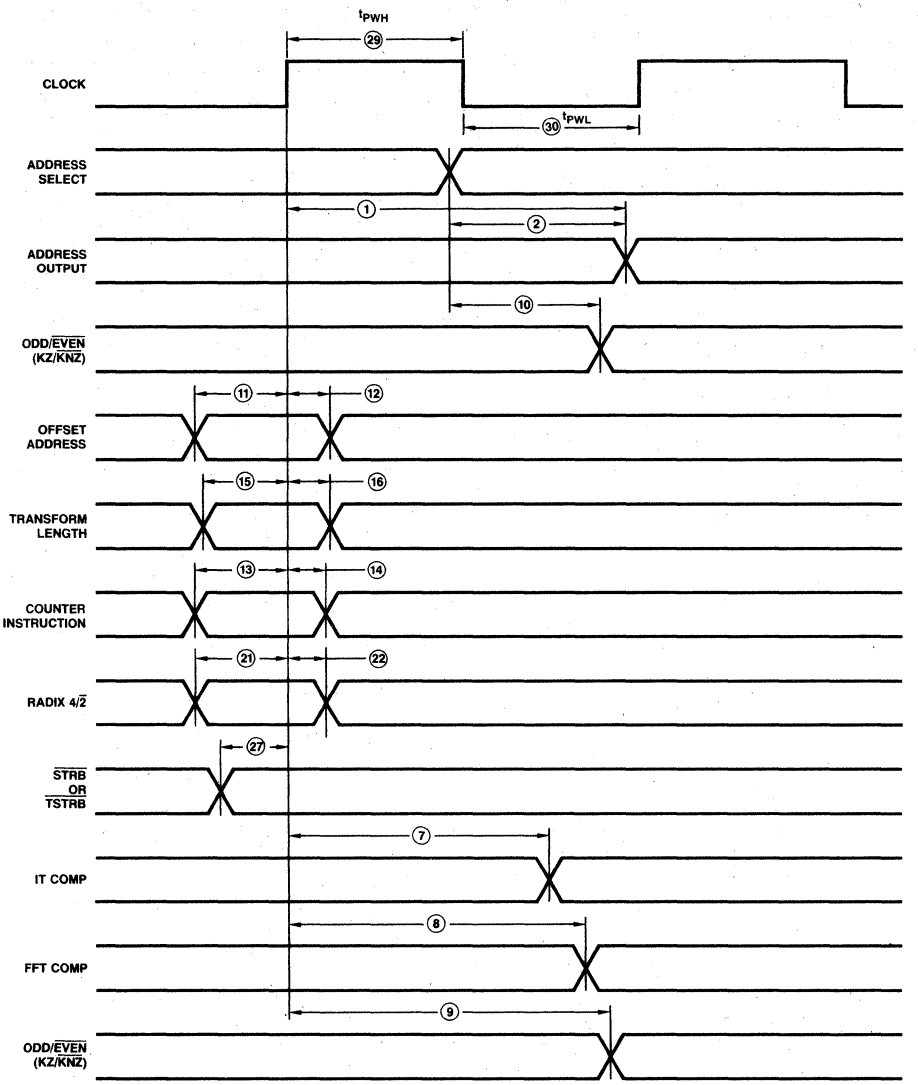
Parameters		Description	COM'L T_A = 0 to 70°C V_{CC} = 5V ±5% Min	COM'L Max	MIL T_C = −55 to +125°C V_{CC} = 5V ± 10% Min	MIL Max	Units	Test Conditions
1	t_{PD}	CP to A_{0-15} (AS = 0)						C_L = 50pF See Test Circuits
1	t_{PD}	CP to A_{0-15} (AS = 1)						
1	t_{PD}	CP to A_{0-15} (AS = 2)						
1	t_{PD}	CP to A_{0-15} (AS = 3)						
1	t_{PD}	CP to A_{0-15} (AS = 4)						
1	t_{PD}	CP to A_{0-15} (AS = 5)						
1	t_{PD}	CP to A_{0-15} (AS = 6)						
1	t_{PD}	CP to A_{0-15} (AS = 7)						
1	t_{PD}	CP to A_{0-15} (AS = 8)						
1	t_{PD}	CP to A_{0-15} (AS = 9)						
1	t_{PD}	CP to A_{0-15} (AS = 10)						
1	t_{PD}	CP to A_{0-15} (AS = 11)						
1	t_{PD}	CP to A_{0-15} (AS = 12)						
1	t_{PD}	CP to A_{0-15} (AS = 13)						
1	t_{PD}	CP to A_{0-15} (AS = 14)						
1	t_{PD}	CP to A_{0-15} (AS = 15)						
2	t_{PD}	Address Select to A_{0-15}						
3	t_{PHZ}	$\overline{OE}$ to A_{0-15} Disable Time						
4	t_{PLZ}	$\overline{OE}$ to A_{0-15} Disable Time						
5	t_{PZH}	$\overline{OE}$ to A_{0-15} Enable Time						
6	t_{PZL}	$\overline{OE}$ to A_{0-15} Enable Time						
7	t_{PD}	CP to IT COMP						
8	t_{PD}	CP to FFT COMP						
9	t_{PD}	CP to ODD/$\overline{EVEN}$/ (KZ/$\overline{KNZ}$)						
10	t_{PD}	Address Select to ODD/$\overline{EVEN}$/ (KZ/$\overline{KNZ}$)						
11	t_S	Offset Address Input A_{0-15} to CP Setup Time						
12	t_H	Offset Address Input A_{0-15} to CP Hold Time						
13	t_S	Counter Instruction to CP Setup Time						
14	t_H	Counter Instruction to CP Hold Time						
15	t_S	Transform Length Select to CP Setup Time						
16	t_H	Transform Length Select to CP Hold Time						
17	t_S	Transform Length Select to $\overline{TSTRB}$ ↑ Setup Time						
18	t_H	Transform Length Select to $\overline{TSTRB}$ ↑ Hold Time						
19	t_S	$\overline{TSEL}$ (HIGH to LOW) to $\overline{TSTRB}$ ↑ Setup Time						
20	t_H	$\overline{TSEL}$ to $\overline{TSTRB}$ ↑ Hold Time						
21	t_S	RADIX 4/$\overline{2}$ to CP Setup Time						
22	t_H	RADIX 4/$\overline{2}$ to CP Hold Time						
23	t_S	RADIX 4/$\overline{2}$, $\overline{PSD}$, DIT/$\overline{DIF}$ to $\overline{STRB}$ ↑ Setup Time						
24	t_H	RADIX 4/$\overline{2}$, $\overline{PSD}$, DIT/$\overline{DIF}$ to $\overline{STRB}$ ↑ Hold Time						
25	t_S	$\overline{SEL}$ (HIGH to LOW) to $\overline{STRB}$ ↑						
26	t_H	$\overline{SEL}$ Hold Time to $\overline{STRB}$ ↑						
27	t_S	$\overline{STRB}$ or $\overline{TSTRB}$ to CP Setup Time						
28	t_{PWSL}	Minimum Strobe Pulse Width LOW						
29	t_{PWH}	CP Pulse Width HIGH						
30	t_{PWL}	CP Pulse Width LOW						

Am29540 SWITCHING CHARACTERISTICS

Parameters		Description	T_A = +25°C V_{CC} = 5.0V Min	Typ	Max	Units	Test Conditions
1	t_{PD}	CP to A_{0-15} (AS = 0)					
1	t_{PD}	CP to A_{0-15} (AS = 1)					
1	t_{PD}	CP to A_{0-15} (AS = 2)					
1	t_{PD}	CP to A_{0-15} (AS = 3)					
1	t_{PD}	CP to A_{0-15} (AS = 4)					
1	t_{PD}	CP to A_{0-15} (AS = 5)					
1	t_{PD}	CP to A_{0-15} (AS = 6)					
1	t_{PD}	CP to A_{0-15} (AS = 7)					
1	t_{PD}	CP to A_{0-15} (AS = 8)					
1	t_{PD}	CP to A_{0-15} (AS = 9)					
1	t_{PD}	CP to A_{0-15} (AS = 10)					
1	t_{PD}	CP to A_{0-15} (AS = 11)					
1	t_{PD}	CP to A_{0-15} (AS = 12)					
1	t_{PD}	CP to A_{0-15} (AS = 13)					
1	t_{PD}	CP to A_{0-15} (AS = 14)					
1	t_{PD}	CP to A_{0-15} (AS = 15)					
2	t_{PD}	Address Select to A_{0-15}					
3	t_{PHZ}	$\overline{OE}$ to A_{0-15} Disable Time					
4	t_{PLZ}	$\overline{OE}$ to A_{0-15} Disable Time					
5	t_{PZH}	$\overline{OE}$ to A_{0-15} Enable Time					
6	t_{PZL}	$\overline{OE}$ to A_{0-15} Enable Time					
7	t_{PD}	CP to IT COMP					C_L = 50pF See Test Circuits
8	t_{PD}	CP to FFT COMP					
9	t_{PD}	CP to ODD/$\overline{EVEN}$/ (KZ/$\overline{KNZ}$)					
10	t_{PD}	Address Select to ODD/$\overline{EVEN}$/ (KZ/$\overline{KNZ}$)					
11	t_S	Offset Address Input A_{0-15} to CP Setup Time					
12	t_H	Offset Address Input A_{0-15} to CP Hold Time					
13	t_S	Counter Instruction to CP Setup Time					
14	t_H	Counter Instruction to CP Hold Time					
15	t_S	Transform Length Select to CP Setup Time					
16	t_H	Transform Length Select to CP Hold Time					
17	t_S	Transform Length Select to $\overline{TSTRB}$ ↑ Setup Time					
18	t_H	Transform Length Select to $\overline{TSTRB}$ ↑ Hold Time					
19	t_S	$\overline{TSEL}$ (HIGH to LOW) to $\overline{TSTRB}$ ↑ Setup Time					
20	t_H	$\overline{TSEL}$ to $\overline{TSTRB}$ ↑ Hold Time					
21	t_S	RADIX 4/$\overline{2}$ to CP Setup Time					
22	t_H	RADIX 4/$\overline{2}$ to CP Hold Time					
23	t_S	RADIX 4/$\overline{2}$, $\overline{PSD}$, DIT/$\overline{DIF}$ to $\overline{STRB}$ ↑ Setup Time					
24	t_H	RADIX 4/$\overline{2}$, $\overline{PSD}$, DIT/$\overline{DIF}$ to $\overline{STRB}$ ↑ Hold Time					
25	t_S	$\overline{SEL}$ (HIGH to LOW) to $\overline{STRB}$ ↑					
26	t_H	$\overline{SEL}$ Hold Time to $\overline{STRB}$ ↑					
27	t_S	$\overline{STRB}$ or $\overline{TSTRB}$ to CP Setup Time					
28	t_{PWSL}	Minimum Strobe Pulse Width LOW					
29	t_{PWH}	CP Pulse Width HIGH					
30	t_{PWL}	CP Pulse Width LOW					

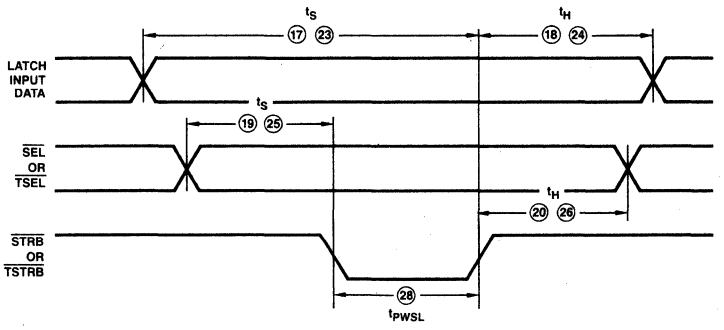
7

TIMING DIAGRAM



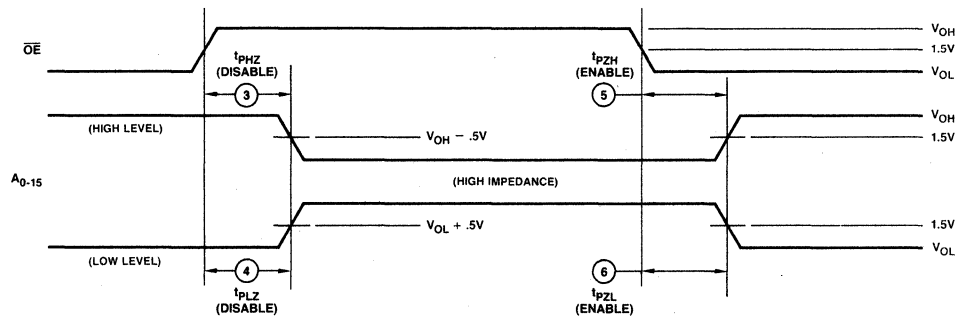
MPL-034

LATCH TIMING DIAGRAM



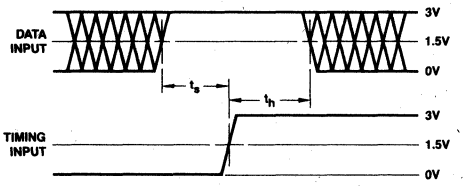
MPL-035

Am29540 3-STATE TIMING DIAGRAM



MPL-036

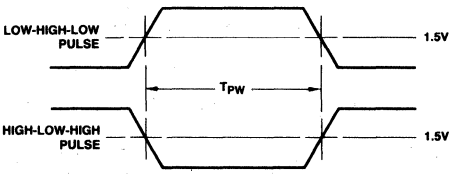
SET-UP AND HOLD TIME



Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

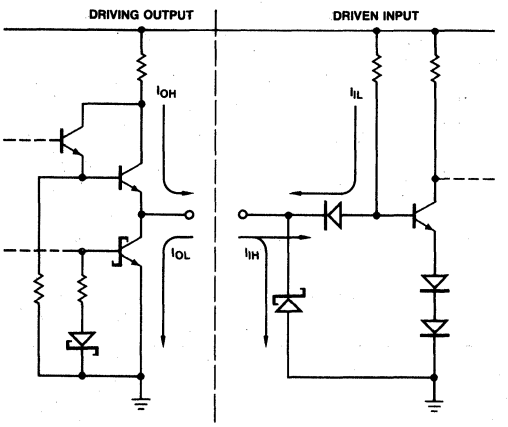
MPL-037

PULSE WIDTH



MPL-038

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



MPL-039

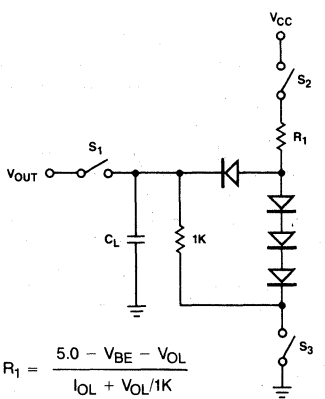
TEST WAVEFORMS

Test	V_X	Output Waveform – Measurement Level
All t_{PD}s	5.0V	V_{OH}, V_{OL}, 1.5V
t_{PHZ}	0.0V	V_{OH}, 0.5V, 0.0V
t_{PLZ}	5.0V	3V, 0.5V, V_{OL}
t_{PZH}	0.0V	V_{OH}, 1.5V, 0.0V
t_{PZL}	5.0V	3V, 1.5V, V_{OL}

MPL-040

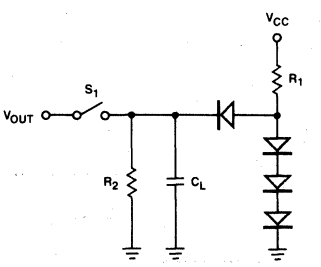
TEST LOADS FOR DELAY MEASUREMENTS

A. THREE-STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

B. NORMAL OUTPUTS



$$R_2 = \frac{2.4V}{I_{OH}} \qquad R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

Am29540 DEFINITION OF FUNCTIONAL TERMS

TL_0, TL_1 TL_2, TL_3 — Transform length control determines the number of points to be transformed. (See Figure 1)

$\overline{TSEL}$, $\overline{TSTRB}$ — Transform length latch enables. These active LOW inputs are ANDed to control the latch. The latch is transparent when both $\overline{TSEL}$ and $\overline{TSTRB}$ are LOW.

I_0, I_1 — Counter Instruction inputs determine one of four available butterfly counter instructions Hold, Reset, Reset/Load and Count. (See Figure 2)

CP — Butterfly counter clock (positive edge active).

Radix 4/$\overline{2}$ — The Radix control determines whether addresses will be generated for Radix-4 (HIGH) for Radix-2 (LOW) transforms.

$\overline{PSD}$ — The Pre-Scrambled Data, $\overline{PSD}$, input is used to select an appropriate transform for input data which has previously been digit reversed. $\overline{PSD}$ must be LOW for pre-scrambled input data. For in-place transforms with normally ordered input data, $\overline{PSD}$ should be HIGH. Refer to individual transform flow charts (p. to) for other cases.

DIT/$\overline{DIF}$ — Control input for selection of the Decimation In Frequency algorithm (LOW) or Decimation In Time algorithm (HIGH).

$\overline{SEL}$, $\overline{STRB}$ — Transform type (Radix 4/$\overline{2}$, PSD, DIF/$\overline{T}$) latch enables. These active LOW inputs are ANDed to control the latch. The latch is transparent when both $\overline{SEL}$ and $\overline{STRB}$ are LOW.

AS_0, AS_1, AS_2, AS_3 — Address Select control determines address selection. (See Figure 3)

$\overline{OE}$ — Three-state output enable. The 3-state output is controlled solely by $\overline{OE}$. The output does not automatically become high impedance during the Reset/Load instruction.

$A_{0\text{-}15}$ Address Output (offset input) — Bidirectional 16-bit port to output selected addresses or to input an address offset.

ODD/$\overline{EVEN}$, (KZ/$\overline{KNZ}$) — For address select 0 to 11 the ODD/$\overline{EVEN}$ output controls the alternation of separate read and write memories for non-in-place transforms. For Address select 12 to 15 KZ/$\overline{KNZ}$ = (HIGH) indicates that the rotational constant to be used in the RVI transform is W^0 and that an alternative butterfly must be implemented.

FFT COMP — FFT Complete = HIGH identifies the last butterfly (or end) of the transform. (See Figure 4)

IT COMP — Iteration Complete = HIGH flags the bottom of a "column" of butterflies. (See Figure 4.)

7

TL_3	TL_2	TL_1	TL_0	Transform Length		
				Radix-2	Radix-4	RVI
L	L	L	L	2	4	4
L	L	L	H	4	4	8
L	L	H	L	8	16	16
L	L	H	H	16	16	32
L	H	L	L	32	64	64
L	H	L	H	64	64	128
L	H	H	L	128	256	256
L	H	H	H	256	256	512
H	L	L	L	512	1024	1024
H	L	L	H	1024	1024	2048
H	L	H	L	2048	4096	4096
H	L	H	H	4096	4096	8192
H	H	L	L	8192	16384	16384
H	H	L	H	16384	16384	32768
H	H	H	L	32768	65536	65536
H	H	H	H	65536	65536	Not Used

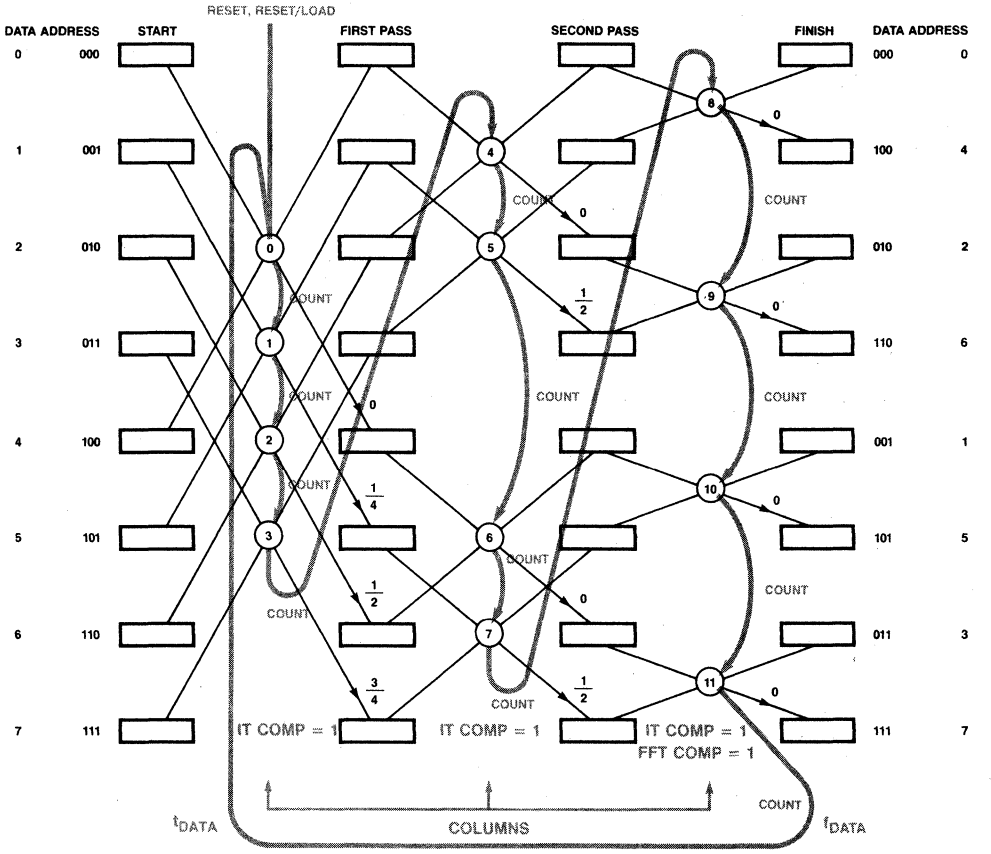
Figure 1. Transform Length Control

I_1	I_0	Counter Function
L	L	Hold, No-Op
L	H	Reset, Reset counter to start of transform with unused address outputs set to 0.
H	L	Reset/Load, Reset counter to start of transform with unused address outputs set to the current value of the address bus.
H	H	Count, increment butterfly counter.

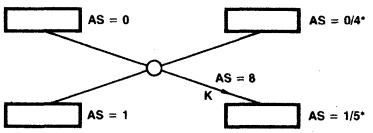
Figure 2. Counter Instruction Control

AS =	AS_3	AS_2	AS_1	AS_0	Description	Usage
0	L	L	L	L	Data Address 1	Radix 2/4
1	L	L	L	H	Data Address 2	Radix 2/4
2	L	L	H	L	Data Address 3	Radix 4
3	L	L	H	H	Data Address 4	Radix 4
4	L	H	L	L	Alt. Data Address 1	Radix 2/4
5	L	H	L	H	Alt. Data Address 2	Radix 2/4
6	L	H	H	L	Alt. Data Address 3	Radix 4
7	L	H	H	H	Alt. Data Address 4	Radix 4
8	H	L	L	L	Const Address 1	Radix 2/4, Shading
9	H	L	L	H	Const Address 2	Radix 4
10	H	L	H	L	Const Address 3	Radix 4
11	H	L	H	H	Const Address 1	Shading
12	H	H	L	L	RVI Data Address 1	RVI
13	H	H	L	H	RVI Data Address 2	RVI
14	H	H	H	L	RVI Data Address 3	RVI
15	H	H	H	H	RVI Data Address 4	RVI

Figure 3. Address Select Control



a) Sequence of Operations for Typical FFT



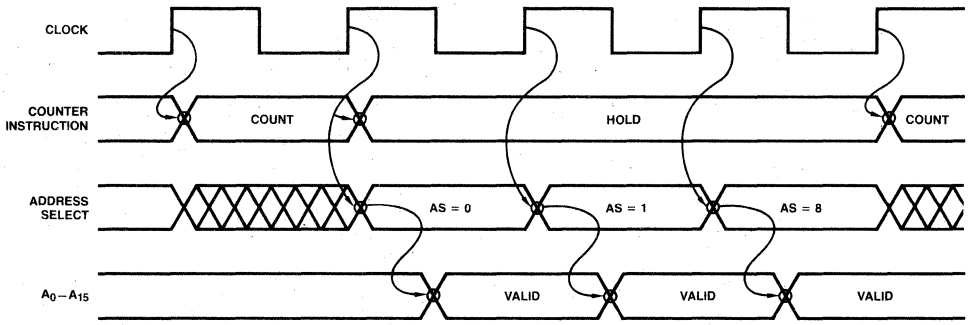
*Note: AS = 4 and AS = 5 are alternate addresses used in non-in-place transformations.

b) Single RADIX-2 Butterfly

Figure 4.

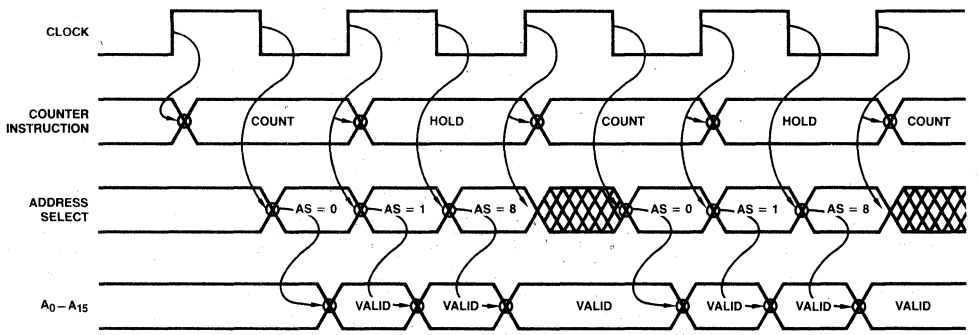
MPL-043

TYPICAL 4-CYCLE RADIX-2 ADDRESS GENERATION



MPL-044

TYPICAL HIGH PERFORMANCE RADIX-2 ADDRESS GENERATION



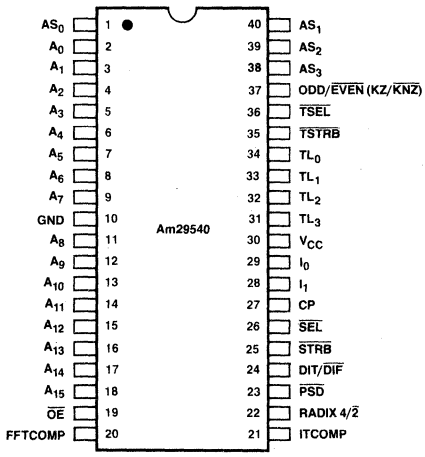
MPL-045

METALLIZATION AND PAD LAYOUT

Am29540

CONNECTION DIAGRAM

Top View



MPL-046

7

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

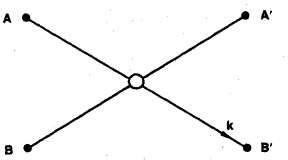
Am29540 Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM29540DC	D-40-1	C	C-1
AM29540DCB	D-40-1	C	B-2 (Note 4)
AM29540DM	D-40-1	M	C-3
AM29540DMB	D-40-1	M	B-3
AM29540LC	L-44	C	C-1
AM29540LM	L-44	M	C-3
AM29540LMB	L-44	M	B-3

Notes: 1. D = Hermetic DIP, L = Chip-Pak. Number following letter is number of leads.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 160 hour burn-in.

TRANSFORM CHARACTERISTICS

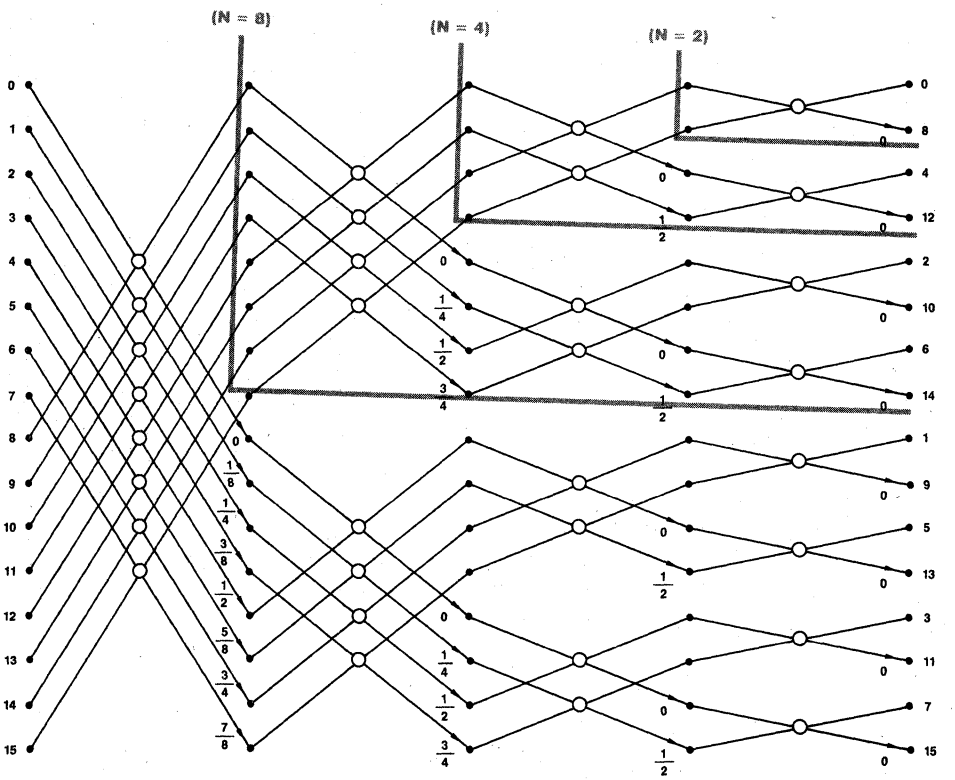
- 16-Point (N = 16)
- RADIX-2
- DIF
- Normally ordered input data (Bit-reversed output data order)
- In-place
- Complex valued input data

TYPICAL BUTTERFLY



FORWARD TRANSFORM	INVERSE TRANSFORM
$A' = A + B$	$A' = A + B$
$B' = (A - B)W^k$	$B' = (A - B)W^{-k}$

$$W = e^{-j\pi}$$



DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/$\overline{2}$
L	H	L

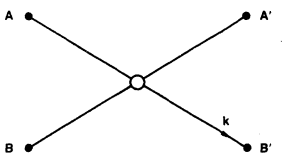
Address of	A	B	A'	B'	W^k
AS =	0	1	0	1	8

MPL-047

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-2
- DIF
- Normally ordered output data (Bit-reversed input data order)
- In-place
- Complex valued input data

TYPICAL BUTTERFLY



FORWARD TRANSFORM

$A' = A + B$

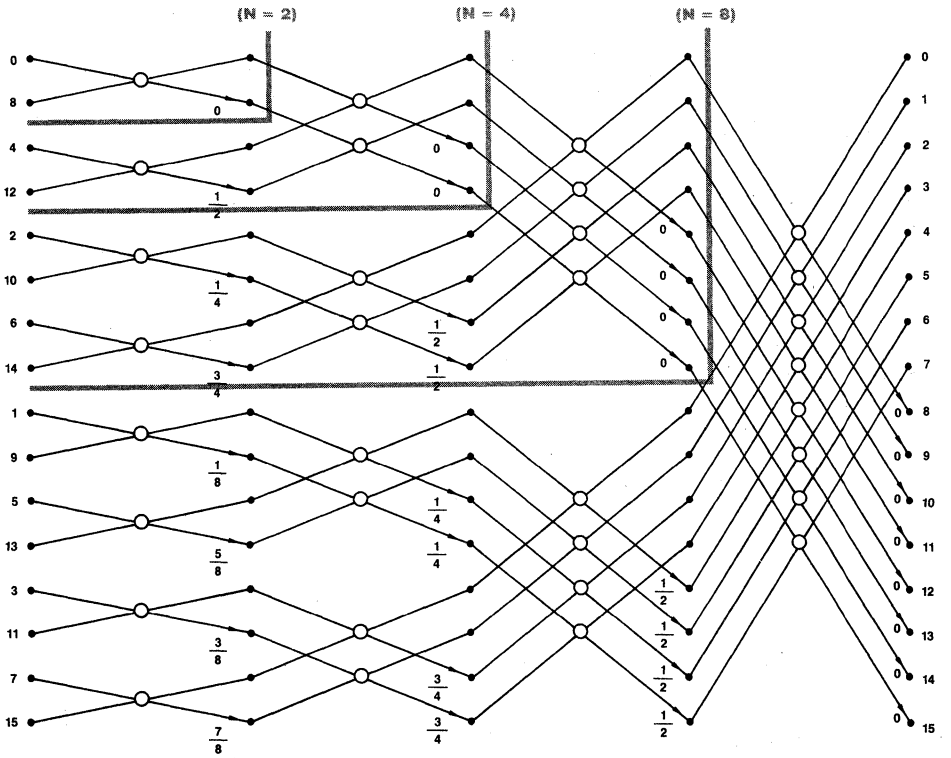
$B' = (A - B)W^k$

INVERSE TRANSFORM

$A' = A + B$

$B' = (A - B)W^{-k}$

$W = e^{-j\pi}$



DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/$\overline{2}$
L	L	L

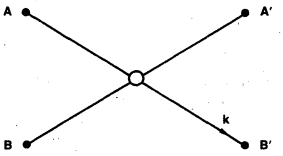
Address of	A	B	A'	B	W_k
AS =	0	1	0	1	8

MPL-048

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-2
- DIF
- Normally ordered input and output data (Non-bit-reversing)
- Non-in-place
- Complex valued input data

TYPICAL BUTTERFLY



FORWARD TRANSFORM

$A' = A + B$

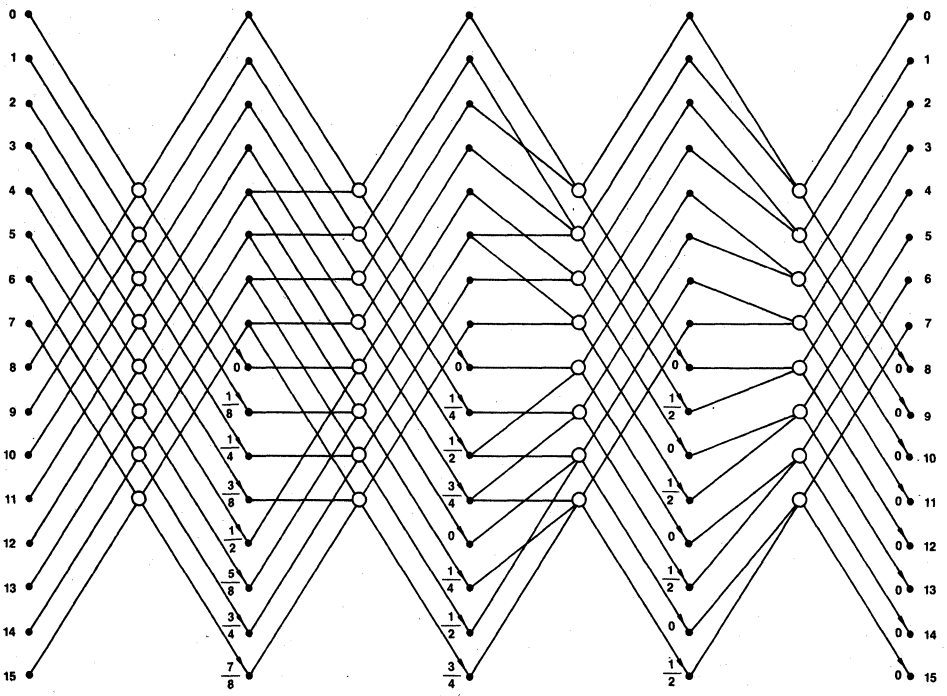
$B' = (A - B)W^k$

INVERSE TRANSFORM

$A' = A + B$

$B' = (A - B)W^{-k}$

$W = e^{-j\pi}$



DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/$\overline{2}$
L	H	L

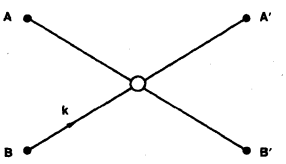
Address of	A	B	A'	B'	W^k
AS =	0	1	4	5	8

MPL-049

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-2
- DIT
- Normally ordered input data (Bit-reversed output data order)
- In-place
- Complex valued input data

TYPICAL BUTTERFLY



FORWARD TRANSFORM

$A' = A + BW^k$

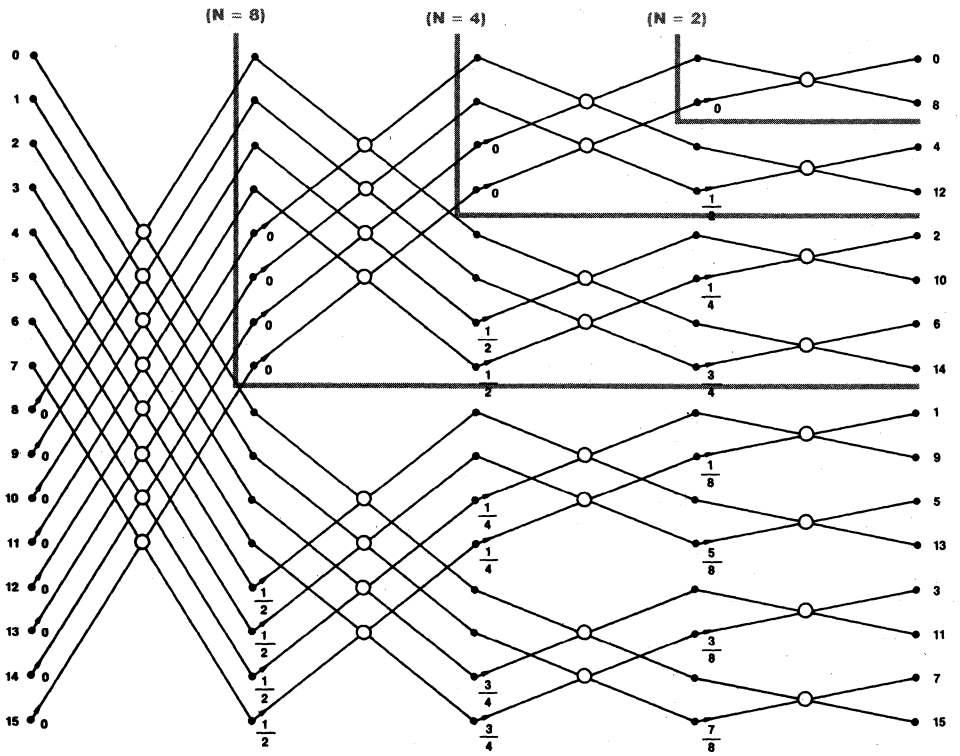
$B' = A - BW^k$

INVERSE TRANSFORM

$A' = A + BW^{-k}$

$B' = A - BW^{-k}$

$W = e^{-j\pi}$



DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/$\overline{2}$
H	H	L

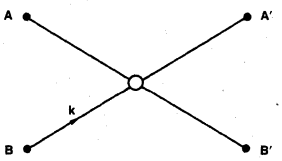
Address of	A	B	A'	B'	W^k
AS =	0	1	0	1	8

MPL-050

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-2
- DIT
- Normally ordered input and output data (Non-bit-reversing)
- Non-in-place
- Complex valued input data

TYPICAL BUTTERFLY



FORWARD TRANSFORM

$A' = A + BW^k$

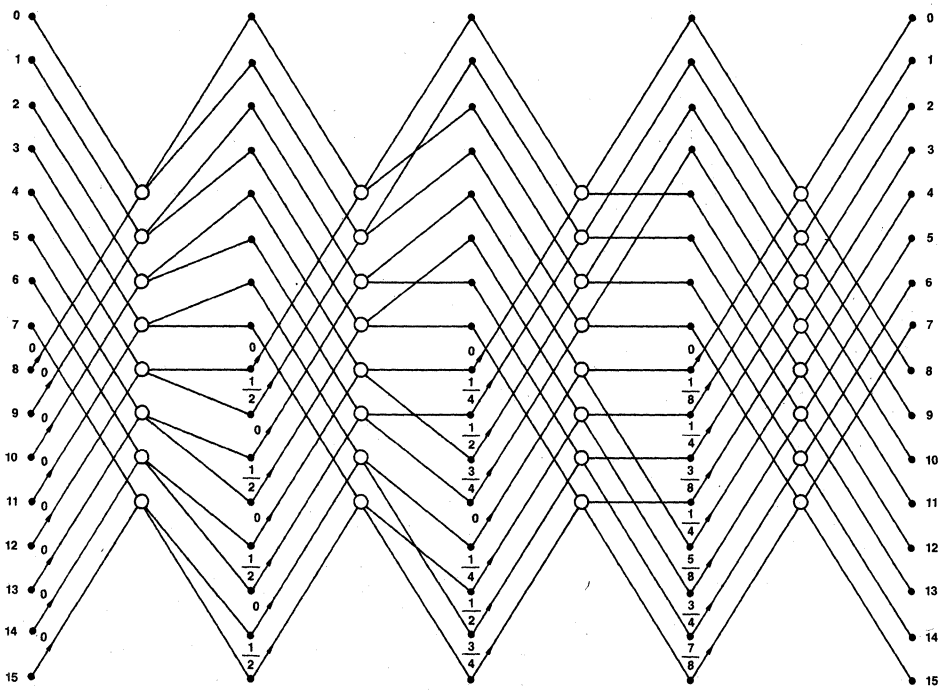
$B' = A - BW^k$

INVERSE TRANSFORM

$A' = A + BW^{-k}$

$B' = A - BW^{-k}$

$W = e^{-j\pi}$



DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/$\overline{2}$
H	L	L

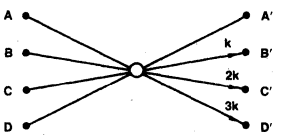
Address of	A	B	A′	B′	W^k
AS =	4	5	0	1	8

MPL-051

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-4
- DIF
- Normally ordered input data (Digit-reversed output data order)
- In-place
- Complex valued input data

TYPICAL BUTTERFLY



FORWARD TRANSFORM

$A' = A + B + C + D$

$B' = (A - jB - C + jD)W^{k}$

$C' = (A - B + C - D)W^{2k}$

$D' = (A + jB - C - jD)W^{3k}$

INVERSE TRANSFORM

$A' = A + B + C + D$

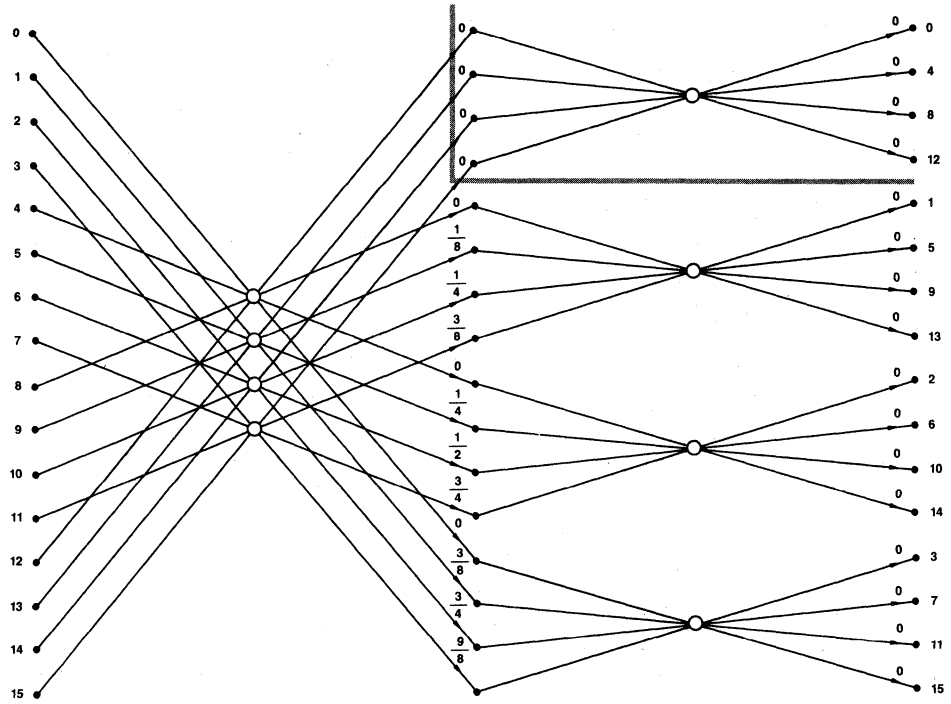
$B' = (A + jB - C - jD)W^{-k}$

$C' = (A - B + C - D)W^{-2k}$

$D' = (A - jB - C + jD)W^{-3k}$

$W = e^{-j\pi}$

(N = 4)



DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/$\overline{2}$
L	H	H

Address of	A	B	C	D	A'	B'	C'	D'	W^{k}	W^{2k}	W^{3k}
AS =	0	1	2	3	0	1	2	3	8	9	10

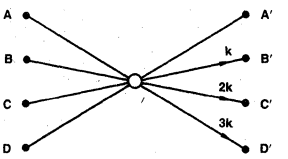
MPL-052

7

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-4
- DIF
- Normally ordered input and output data (Non-digit reversing)
- Non-in-place
- Complex valued input data

TYPICAL BUTTERFLY



FORWARD TRANSFORM

$A' = A + B + C + D$

$B' = (A - jB - C + jD)W^{k}$

$C' = (A - B + C - D)W^{2k}$

$D' = (A + jB - C - jD)W^{3k}$

INVERSE TRANSFORM

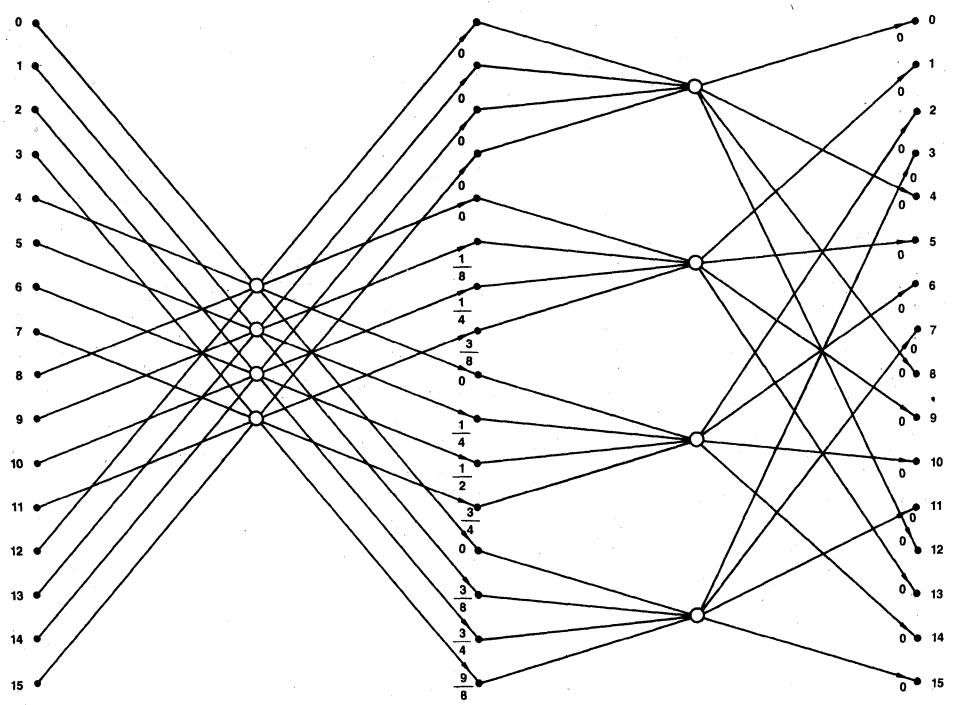
$A' = A + B + C + D$

$B' = (A + jB - C - jD)W^{-k}$

$C' = (A - B + C - D)W^{-2k}$

$D' = (A - jB - C + jD)W^{-3k}$

$W = e^{-j\pi}$



DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/$\overline{2}$
L	H	H

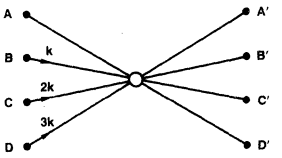
Address of	A	B	C	D	A'	B'	C'	D'	W^{k}	W^{2k}	W^{3k}
AS =	0	1	2	3	4	5	6	7	8	9	10

MPL-053

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-4
- DIT
- Normally ordered input data (Digit-reversed output data order)
- In-place
- Complex valued input data

TYPICAL BUTTERFLY



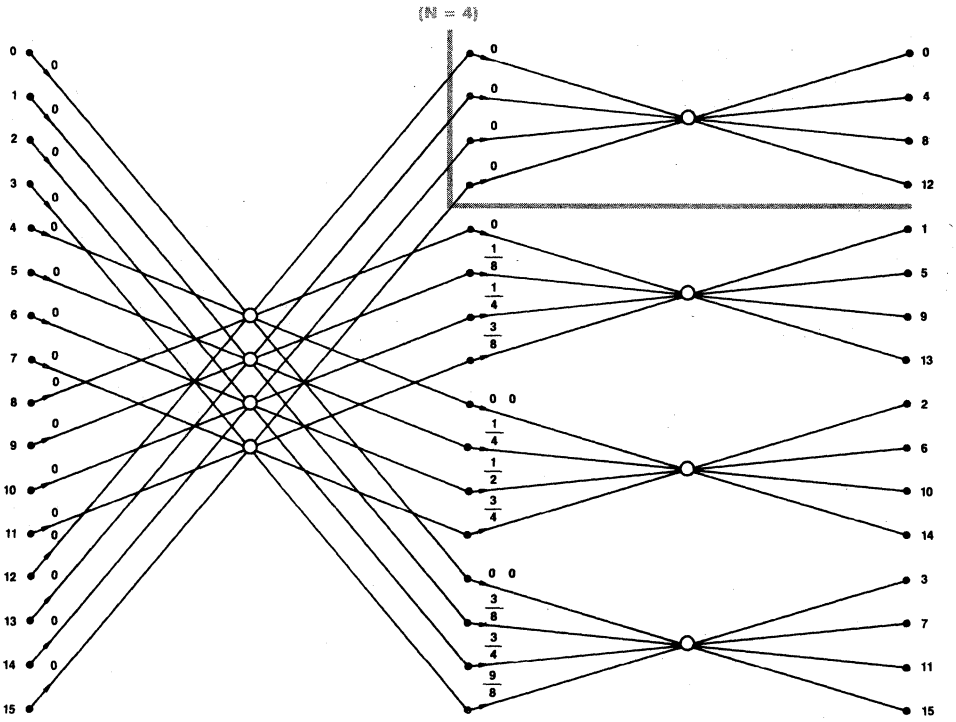
FORWARD TRANSFORM

$$A' = A + BW^{k} + CW^{2k} + DW^{3k}$$
$$B' = A - jBW^{k} - CW^{2k} + jDW^{3k}$$
$$C' = A - BW^{k} + CW^{2k} - DW^{3k}$$
$$D' = A + jBW^{k} - CW^{2k} - jDW^{3k}$$

INVERSE TRANSFORM

$$A' = A + BW^{-k} + CW^{-2k} + DW^{-3k}$$
$$B' = A + jBW^{-k} - CW^{-2k} - jDW^{-3k}$$
$$C' = A - BW^{-k} + CW^{-2k} - DW^{-3k}$$
$$D' = A - jBW^{-k} - CW^{-2k} + jDW^{-3k}$$

$$W = e^{-j\pi}$$



DIT/$\overline{DIF}$	$\overline{PSD}$	RADIX 4/$\overline{2}$
H	H	H

Address of	A	B	C	D	A'	B'	C'	D'	W^{k}	W^{2k}	W^{3k}
AS =	0	1	2	3	0	1	2	3	8	9	10

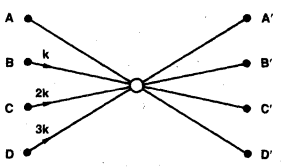
MPL-054

7

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-4
- DIT
- Normally ordered output data (Digit-reversed input data order)
- In-place
- Complex valued input data

TYPICAL BUTTERFLY



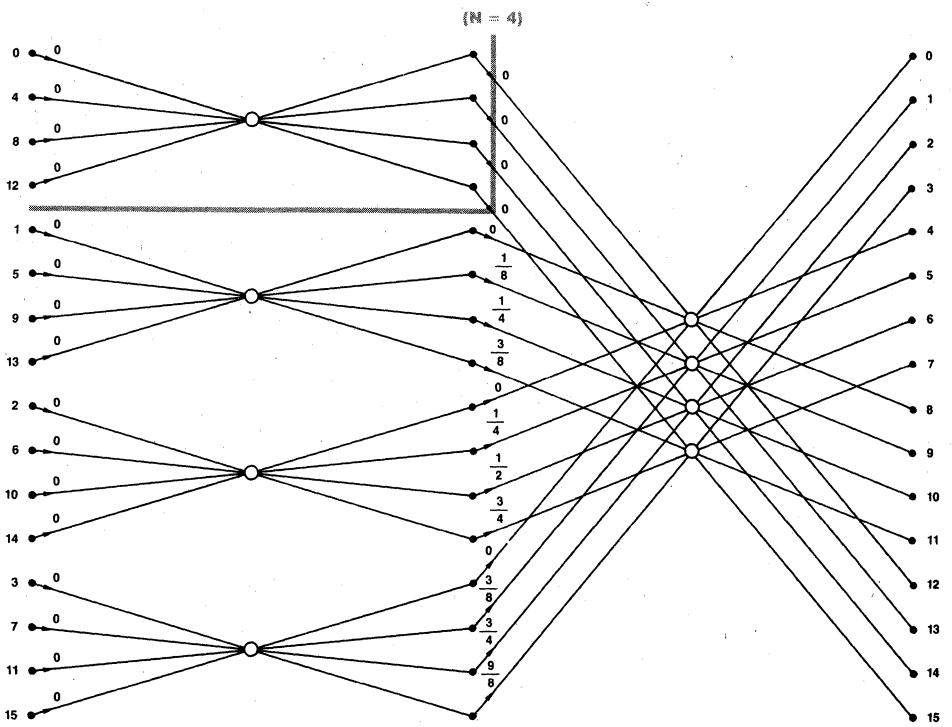
FORWARD TRANSFORM

$$A' = A + BW^{k} + CW^{2k} + DW^{3k}$$
$$B' = A - jBW^{k} - CW^{2k} + jDW^{3k}$$
$$C' = A - BW^{k} + CW^{2k} - DW^{3k}$$
$$D' = A + jBW^{k} - CW^{2k} - jDW^{3k}$$

INVERSE TRANSFORM

$$A' = A + BW^{-k} + CW^{-2k} + DW^{-3k}$$
$$B' = A + jBW^{-k} - CW^{-2k} - jDW^{-3k}$$
$$C' = A - BW^{-k} + CW^{-2k} - DW^{-3k}$$
$$D' = A - jBW^{-k} - CW^{-2k} + jDW^{-3k}$$

$$W = e^{-j\pi}$$



DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/$\overline{2}$
H	L	H

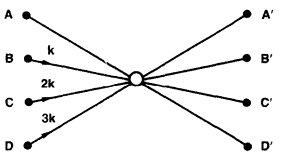
Address of	A	B	C	D	A′	B′	C′	D′	W^{k}	W^{2k}	W^{3k}
AS =	0	1	2	3	0	1	2	3	8	9	10

MPL-055

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-4
- DIT
- Normally ordered input and output data (Non-digit reversing)
- Non-in-place
- Complex valued input data

TYPICAL BUTTERFLY



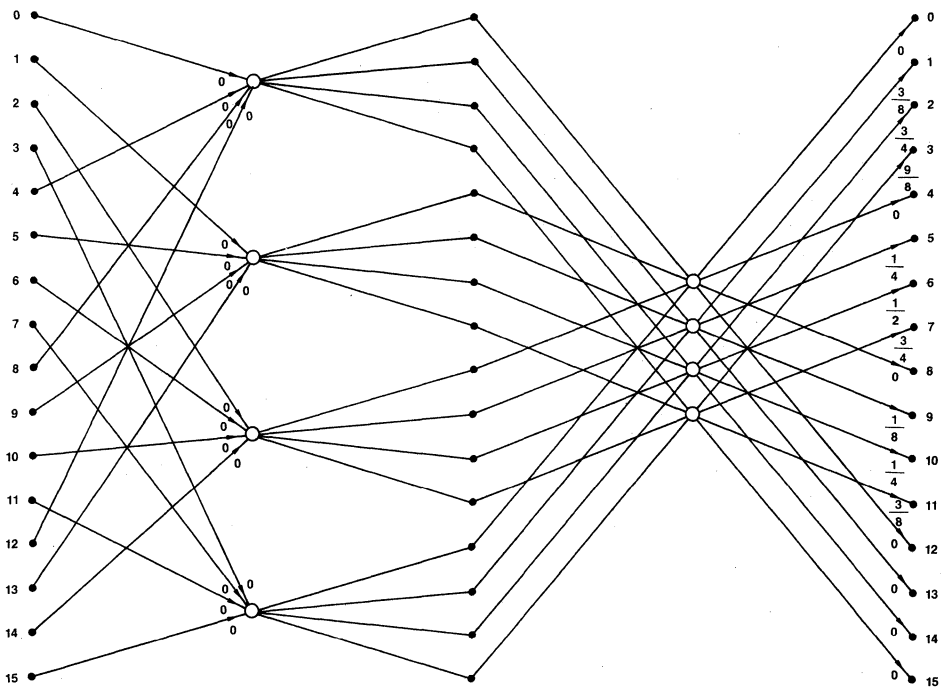
FORWARD TRANSFORM

$$A' = A + BW^{k} + CW^{2k} + DW^{3k}$$
$$B' = A - jBW^{k} - CW^{2k} + jDW^{3k}$$
$$C' = A - BW^{k} + CW^{2k} - DW^{3k}$$
$$D' = A + jBW^{k} - CW^{2k} - jDW^{3k}$$

INVERSE TRANSFORM

$$A' = A + BW^{-k} + CW^{-2k} + DW^{-3k}$$
$$B' = A + jBW^{-k} - CW^{-2k} - jDW^{-3k}$$
$$C' = A - BW^{-k} + CW^{-2k} - DW^{-3k}$$
$$D' = A - jBW^{-k} - CW^{-2k} + jDW^{-3k}$$

$$W = e^{-j\pi}$$



DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/$\overline{2}$
H	L	H

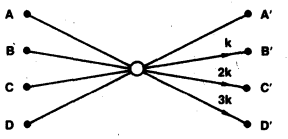
Address of	A	B	C	D	A′	B′	C′	D′	W^{k}	W^{2k}	W^{3k}
AS =	4	5	6	7	0	1	2	3	8	9	10

MPL-056

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-4
- DIF
- Normally ordered output data (Digit-reversed input data order)
- In-place
- Complex valued input data

TYPICAL BUTTERFLY



FORWARD TRANSFORM

$A' = A + B + C + D$

$B' = (A - jB - C + jD)W^{k}$

$C' = (A - B + C - D)W^{2k}$

$D' = (A + jB - C - jD)W^{3k}$

INVERSE TRANSFORM

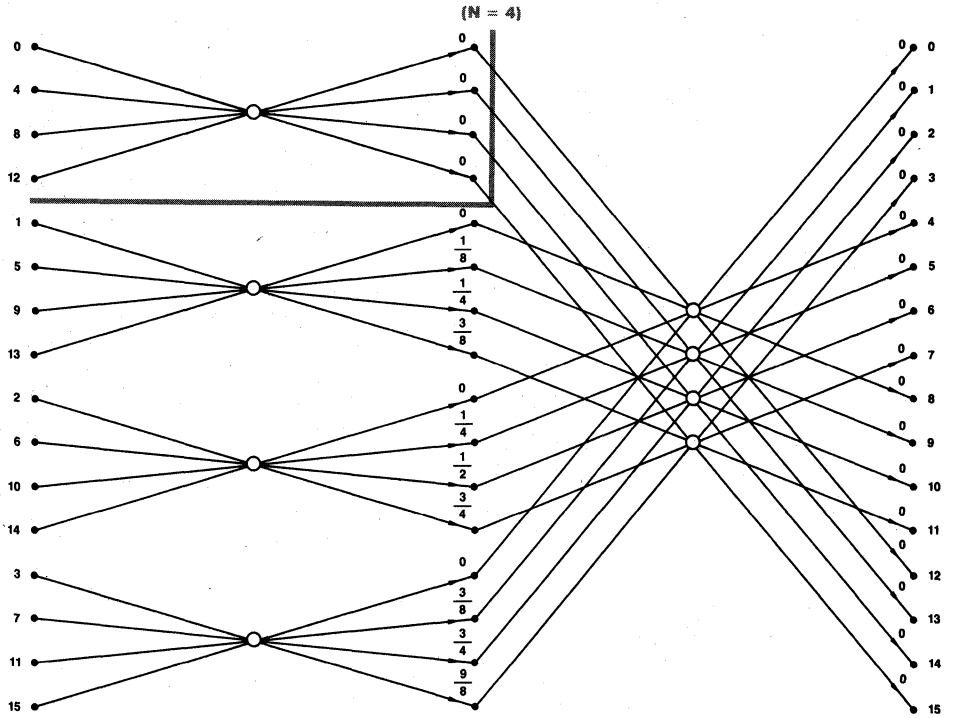
$A' = A + B + C + D$

$B' = (A + jB - C - jD)W^{-k}$

$C' = (A - B + C - D)W^{-2k}$

$D' = (A - jB - C + jD)W^{-3k}$

$W = e^{-j\pi}$



DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/2
L	L	H

Address of	A	B	C	D	A'	B'	C'	D'	W^{k}	W^{2k}	W^{3k}
AS =	0	1	2	3	0	1	2	3	8	9	10

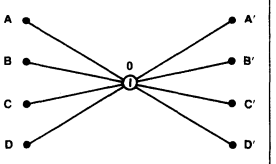
MPL-057

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-2
- DIT
- Normally ordered input data (Unique output data order)
- In-place
- Real Valued Input (RVI) data
- Forward transform

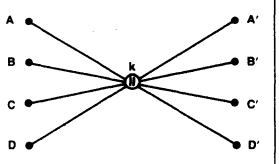
TYPICAL BUTTERFLIES

$KZ/\overline{KNZ}$ = HIGH (k = 0)



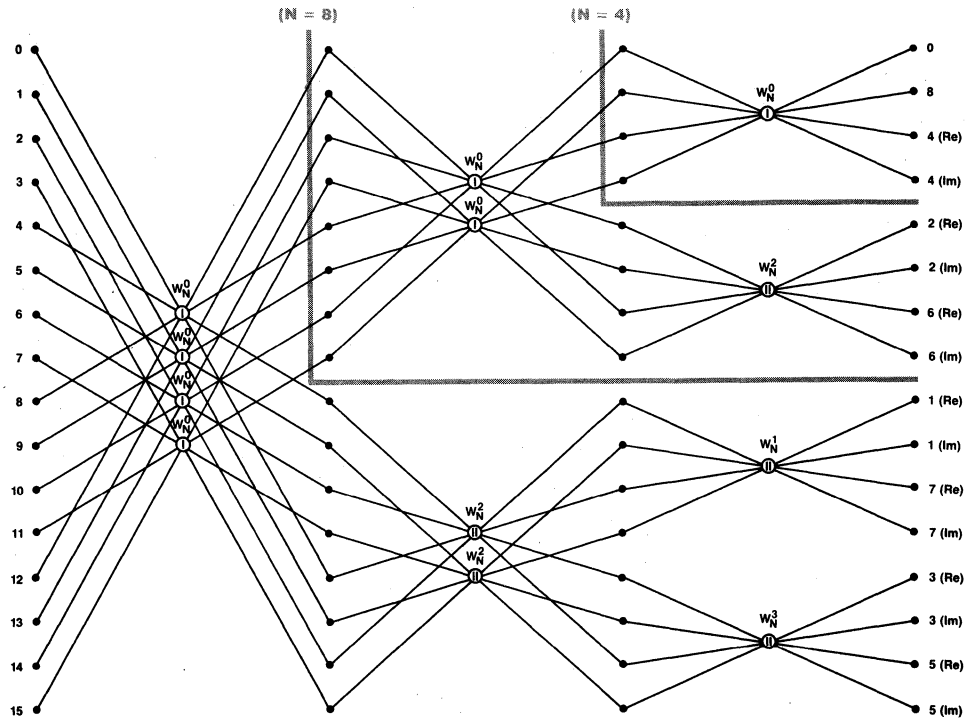
$A' = Re[A + jB + (C + jD)W_N^0]$
$B' = Im[A + jB + (C + jD)W_N^0]$
$C' = Re[A + jB - (C + jD)W_N^0]$
$D' = Im[-A - jB + (C - jD)W_N^0]$

$KZ/\overline{KNZ}$ = LOW ($k \neq 0$)



$A' = Re[A + jC + (B + jD)W_N^k]$
$B' = Im[A + jC + (B + jD)W_N^k]$
$C' = Re[A + jC - (B + jD)W_N^k]$
$D' = Im[-A - jC + (B + jD)W_N^k]$

$W_N = e^{-j\frac{2\pi}{N}}$



DIT/$\overline{DIF}$	$\overline{PSD}$	RADIX 4/$\overline{2}$
H	H	L

Address of	A	B	C	D	A'	B'	C'	D'	W_N^k
AS =	12	13	14	15	12	13	14	15	8

MPL-058

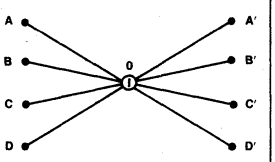
7

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-2
- DIF
- Normally ordered output data (Unique input data order)
- In-place
- Real valued output data
- Inverse transform

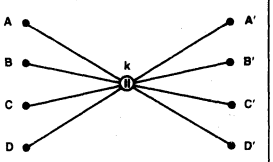
TYPICAL BUTTERFLIES

$KZ/\overline{KNZ}$ = HIGH
(k = 0)



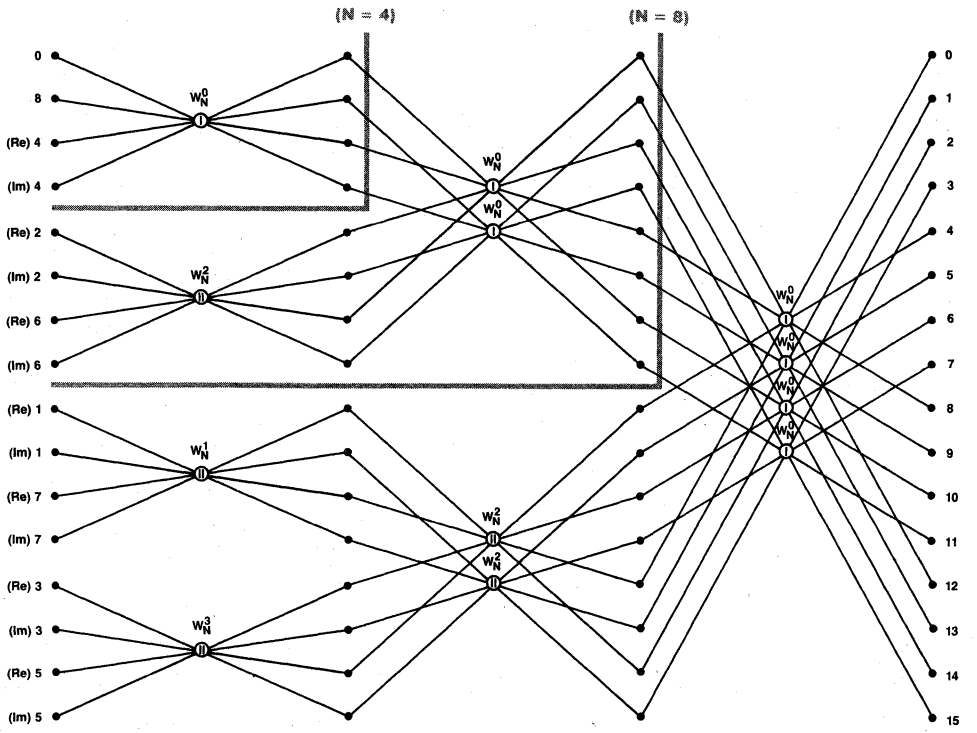
$A' = Re\,[A + jB + C - jD]$
$B' = Im\,[A + jB + C - jD]$
$C' = Re\,[(A + jB - C + jD)W_N^0]$
$D' = Im\,[(A + jB - C + jD)W_N^0]$

$KZ/\overline{KNZ}$ = LOW
(k ≠ 0)



$A' = Re\,[A + jB + C - jD]$
$B' = Re\,[(A + jB - C + jD)W_N^k]$
$C' = Im\,[A + jB + C - jD]$
$D' = Im\,[(A + jB - C + jD)W_N^k]$

$W_N = e^{j\frac{2\pi}{N}}$



DIT/$\overline{DIF}$	$\overline{PSD}$	RADIX 4/$\overline{2}$
L	L	L

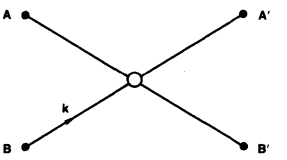
Address of	A	B	C	D	A'	B'	C'	D'	W_N^k
AS =	12	13	14	15	12	13	14	15	8

MPL-059

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-2
- DIT
- Normally ordered output data (Bit-reversed input data order)
- In-place
- Complex valued input data

TYPICAL BUTTERFLY



FORWARD TRANSFORM

$A' = A + BW^k$

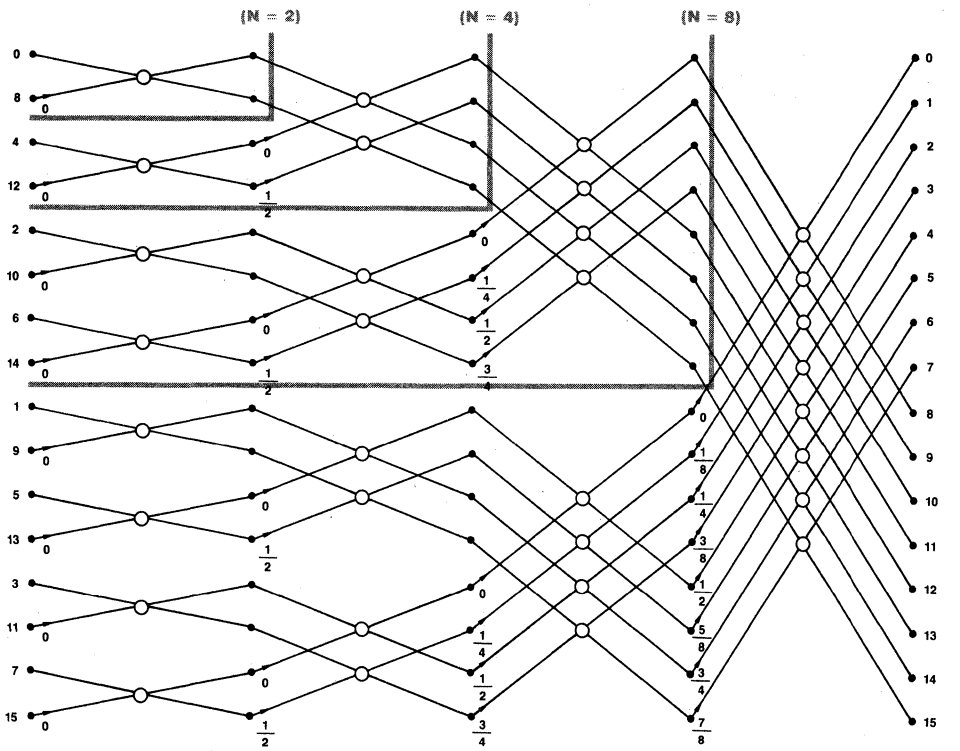
$B' = A - BW^k$

INVERSE TRANSFORM

$A' = A + BW^{-k}$

$B' = A - BW^{-k}$

$W = e^{-j\pi}$



DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/$\overline{2}$
H	L	L

Address of	A	B	A'	B'	W^k
AS =	0	1	0	1	8

MPL-060

Am29800
High Performance Bus Interface and Logic Index

High Performance Bus Interface Family Standardizes Around Slim 24-Pin Package

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Advanced Micro Devices, Inc.
Sunnyvale, CA

Most IC designers tend to focus their attention on ever more complex VLSI solutions to improve the package count, cost and reliability of microprocessor based systems. In many cases, however, greater impact could be achieved with much less effort by designing a more efficient bus interface. The last major innovation in this area was the advent of the popular 20-pin octal interface, which occurred not so coincidentally with the boom in 8-bit microprocessor sales.

The Octal Explosion

The 20-pin package was ideal for 8-bit interface elements as it allowed for eight input lines, eight output lines, two control inputs, power supply and ground. Octal configurations of registers, latches and transceivers, appeared in Schottky, low-power Schottky and CMOS technologies from every major integrated circuit supplier, and as technology improved, a proliferation of polarity, pin rotation, high current drive and low power options became available to meet every conceivable 8-bit need.

However, as the designers' world became more complex, it became apparent that modular sizes larger than 8 bits were needed. For example, systems that use a parity check scheme need 9 bits for each byte, and if a clock line is added, a 10-bit part is needed. The 10-bit part also fits nicely with the 20-bit addressing schemes used with many 16-bit microprocessors.

A 9- or 10-bit function previously required the one octal and one 4-bit part, which left the designer with two packages and potential problems. Clearly, the answer was a new approach.

The 24-Pin Solution

Two factors contributed to the 24-pin solution. First was the development of a more compact 24-pin package. Until recently the only package available for this pin count was a 600-mil wide DIP. Now a slimline, 24-pin 300-mil wide package, called Thin-DIP by AMD, is entering production at a number of package manufacturers. Second, advanced Schottky technologies made it possible to pack increased functional complexity onto chips small enough to fit into the narrow cavities of these new packages. AMD calls its version of this process IMOX™, an acronym which means ion-implanted and oxide-isolated.

The fabrication and packaging problems overcome, AMD proceeded to define a complete family of functions from the ground up. While the previous 20-pin octal interface devices had been a great improvement over their predecessors, the piecemeal approach to their conception had led to a bewildering array of inconsistent configurations. So before starting design on any one device, AMD applications engineers looked at all the essential interface functions required by a system. The result is the new Am29800 series.

The Am29800 family includes registers, latches, buffers and transceivers; most functions are supplied in 8- or 9- and 10-bit wide configurations. De facto standards have determined that most systems are noninverting internally, while most bus configurations are inverting. To meet all these needs, both inverting and noninverting versions of the Am29800 devices are available to the designer.

Now that two-layer metal interconnect is an established manufacturing process, it is possible to give careful consideration to the physical location of input and output pins. All inputs on the new Am29800 family have been placed on one side of the package with corresponding outputs on the other, so data can flow in a direct physical path from the microprocessor CPU through the interface unit and onto the bus. This permits a much cleaner board layout. In addition, power supply, ground and control function pins are always in the same position.

AMD also decided to standardize pinouts between logic functions. For example, all 10-bit elements, i.e., latches, registers or transceivers, have the same input and output pin assignment, as do all 9- and 8-bit devices.

Electrical Performance

For many years, TTL devices, such as the 'S240 series, employed PNP inputs to achieve very low input current characteristics. Unfortunately, while the DC input current is indeed low, the dynamic performance of the device is severely downgraded because of the large capacitance associated with the PNPs. The Am29800 devices were designed with low capacitance loading at the inputs and outputs.

Most IC data sheets specify AC performance at 15pF test conditions only. While this is adequate for general purpose logic applications, a realistic bus structure will typically see much higher loading, and all Am29800 series devices are designed to provide optimum performance under more realistic system conditions. Specified sink currents of 48mA over the commercial temperature operating range (0 to 70°C) and 32mA over the military temperature range (−55 to +125°C) ensure adequate capacitance drive and fan-out for bus systems. And since drivers must charge load capacitance in both falling and rising directions, source current is also fully characterized at both 2.0 and 2.4V.

Critical AC specifications such as propagation delays and disable times for the three-state outputs are specified for 300pF load conditions both at 25°C and over the full operating temperature range and power supply tolerance; specific delays depend on the function being considered. Typical values for a D-type register at 50pF are 6 to 7ns, comparable to those achieved with AS or FAST devices under the same conditions and an improvement over higher power Schottky products. At 350pF, loading delays increase to the 12 to 14ns range. Simple buffers and inverters exhibit typical values of 4ns.

Registers

The Am29821-26 Bus Interface Registers are specifically designed to provide extra width for wide address or data paths and buses carrying parity.

The Am29821 is a 10-bit wide version of the popular '374 8-bit register. It has ten inputs, ten outputs, common buffered clock enable and three status Output Enable lines. The inverting version, Am29822, is comparable with the '534 8-bit device.

The 9-bit registers, Am29823 and Am29824, give up one bit to gain two additional control lines which are used for Clock Enable ($\overline{EN}$), and Clear ($\overline{CLR}$). This combines '273, '374 and '377 functions in one single package. The extra pins available on the 8-bit parts, Am29825 and Am29826, provide gate output enable capability, which eliminates the need for external gate packages when used in DMA or Multibus® control applications. The Am29825 can also be used to implement high source/sink drive on the data port

for the AmZ8000™ or 8086 16-bit CPUs. The registers can be controlled from WR and CS, can be cleared and can be disabled for DMA operations. The two 24-pin parts replace four of the earlier octal devices plus one gate package and system performance is improved up to three or four times because of the reduced number of gate delays and shorter wiring traces.

Metastable Operation

The Am29800 Family registers provide an additional bonus; they recover extremely fast from a metastable condition.

The metastable condition occurs in all flip-flops any time the active clock edge interrogates the input at exactly the same time the input changes state. When this happens the cross coupled latch at the output can reach a balanced, symmetrical condition which it will hold for some microseconds or even milliseconds before returning to its proper state. Previously, the designer of asynchronous system had only one remedy for the metastable problem. Two or even three synchronizer flip-flops could be cascaded. This reduced probability of a metastable output but increased throughput delay.

The Am29800 registers, while not totally immune to this problem are "metastable hardened" by means of a unique circuit design that reduces both the probability **and** the delay of any metastable condition under test. Artificially induced, a metastable condition failed to produce any output oscillations and increased the clock-to-input delay by a mere 6ns. This is an improvement of many orders of magnitude over previously available designs.

Other Functions

Other functions in the Am29800 family include latches, buffers and transceivers, comparators and special parity transceivers.

The Am29841 through Am29846 latches follow the pattern as the registers. The 10-bit device is similar in function to the popular 'S373 octal latch; control lines available are latch enable (LE) and three-state output enable (OE). The noninverting device is analogous to the '533 element. The 9-bit latches add preset (PRE) and clear (CLR) and the 8-bit options have added gated output enable controls.

Buffers and inverters, Am29827 and Am29828, are 10-bit wide high performance versions of the '240 and '244 devices, while the transceivers emulate the '245 and 8304B octal elements. For improved operation in a noisy bus environment, all data inputs have 200mV minimum input hysteresis.

The Metastable Problem

One problem faced by designers is the interfacing of asynchronous digital signals. Although most difficulties can be overcome somewhat easily, there is also a more fundamental problem that defies a perfect solution. The following is a general overview of the metastable problem.

Latches and flip-flops are normally considered bistable devices, since they have two unconditionally stable operating points, either HIGH or LOW. There is, however, a third operating point when the cross-coupled arrangement is exactly balanced. This operating point is stable only if there is no noise in the system and the system is perfectly balanced. The condition is called metastable (meta = Greek for "between"). A metastable condition will last only long enough for the circuit to fall into one of the two stable operating points. This time can be many microseconds, even milliseconds, for devices as fast as a 74S74 flip-flop. In other words, if a flip-flop has reached the balanced, metastable condition, it may remain in this state for an undetermined time, perhaps 1000 times longer than its normal response speed.

When Does This Cause A Problem?

In almost every digital system certain asynchronous events (key-strokes, incoming data, interrupts), must be synchronized to the computer clock. The textbook solution is a fast, clocked flip-flop, like the 74S74, in which the asynchronous signal is applied to the D input and clocked with the system clock. This results in a perfectly synchronized output (usually).

Let's analyze the timing more carefully: the data sheet specified a setup time requirement (for this device, t_S = 3ns). This means that any signal that arrives at least 3ns before the clock edge will achieve the intended result, i.e., an H will set, an L will reset the flip-flop. Great for synchronous systems. But what happens when the asynchronous input violates this setup time requirement and changes less than 3ns before the clock edge? Well, most of the time nothing. The actual moment where the flip-flop samples the D input is somewhere in the guaranteed range, i.e., somewhere less than 3ns before the clock. So the flip-flop makes the decision. It either senses the change on the asynchronous input and therefore changes its Q output, or it ignores the change and doesn't change the Q output. So the only thing lost is one clock cycle. Unfortunately that's not always true.

It is Now Necessary to Look Beyond the Data Sheet

If the D input changes exactly at the same moment that the flip-flop makes its decision, it might transfer exactly the amount of energy to kick the output latch into the metastable balanced condition, from which it will recover after an unpredictable delay (measured in nanoseconds, microseconds or even milliseconds).

In other words: any latch, flip-flop or register has a "moment of truth" somewhere inside the guaranteed range of setup time where it actually makes up its mind, and if the input changes at that very moment, the output is no longer synchronous. This "moment of truth" is a very short window. For TTL flip-flops it is of the order of 10ps, for MOS devices it is more like 50ps to 100ps. For purposes of this discussion this timing window will be called "t."

How often does this happen?

Here are two extreme examples. In each case there is a need to synchronize asynchronous inputs that have **no phase or frequency relationship** with the computer clock.

- Date signal derived from a disk, roughly 6MHz with enough frequency modulation and jitter to make it totally asynchronous to the 10MHz computer clock. How often will the TTL synchronizer go metastable?

  The answer is, every time the Data Signal falls into the "window." The probability of hitting the window is t divided by the clock period, or even simpler: clock frequency times t.

  M = Metastable Rate $= f_D \cdot f_C \cdot t$
  $= 6MHz \cdot 10MHz \cdot 10ps$
  $= 600Hz$

  f_D = Device Frequency

  f_C = Clock Frequency

  The synchronizer goes metastable **600 times per second.**

- Keyboard entry: one keystroke per second synchronized with a 100KHz clock.

  M = Metastable Rate $= 1Hz \cdot 10^5Hz \cdot 10ps = 10^{-6}Hz$

  The synchronizer goes metastable with a statistical probability of once per 10^6 sec, i.e., **once every six weeks** (assuming 5 eight-hour days/week).

"Going metastable" here means that the synchronizer output is within a mid-level or oscillation range for an unpredictable time. Most occurrences will last less than 50ns, but may occasionally last much longer – perhaps many microseconds. This certainly can upset the timing chain.

A metastable latch or flip-flop has an unpredictable delay and will therefore change its output at a time that differs from the value obtained from the worst case timing analysis. In a slow system this usually doesn't matter, but in a fast system it can lead to a "crash."

The AMD Am29821–26 registers have been "metastable-hardened" by means of a new circuit design approach. They show no oscillations and only a minimal increase in output delay when hit right in the window.

In Conclusion:

Metastable operation is an inherent, so far incurable disease of all asynchronous interfaces. Once understood, the problem can be handled by reducing its probability to an acceptable level. AMD's Am29821-26 registers vastly minimize this problem.

29800 Design Guidelines

The 29800 Family offers short delay and setup times, high drive capability (fan-out), and low input capacitance – attractive features for modern high performance TTL systems.

As in any high speed bus interface ('S240 series, FAST or Advanced Schottky), high edge rates and high drive capability mean that a certain amount of care must be exercised in the design of both signal paths and the grounding system. Since every data path is really a transmission line, the relationships between loading, termination, noise margins and ringing must be given more than cursory consideration.

Similarly, the grounding network may require either heavier busing or a grid approach depending on the number of drivers in a given area. 48mA per bit, plus the AC impact of charging bus lines can cause large ground currents. Distributed supply decoupling is required to provide local charging current for bus drive.

Here are some general suggestions to minimize the potential for system induced grounding and noise problems. These suggestions, in conjunction with the designer's own practical experience handling similar problems with high performance S, AS or FAST logic families, will result in an optimum Am29800 design.

- **Minimize Crosstalk**
  Provide Tight Ground
  - Use topside links to create a ground "grid"
  - In multi-layer boards use a ground plane
  - In flat cables make every other wire a ground
  - Minimize spacing between signal lines and ground
  - Maximize spacing between signal lines

  For backplane or wire-wrap systems use a twisted pair for sensitive functions – clock, asynchronous set/clear lines.

  Use of 4 layer boards is recommended.

- **Increase Decoupling**
  Distribute System Capacitance
  - Provide one bypass cap close to each buffer package
  - Provide one bypass cap for every two logic packages

  Use High Frequency Capacitors
  - Take care in the selection of decoupling capacitor materials. Good choices include high frequency tantalum and ceramic types.
  - Do not use low frequency capacitors or aluminum electrolytics

- **Be Sure All Lines Are Terminated**

Am29806/Am29809

6-Bit Chip Select Decoder
9-Bit Equal-to Comparator
ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- High-speed, expandable, 9-bit "equal-to" comparator (Am29809)
- High-speed comparator with chip select decoder (Am29806)
- Multibus™ compatible, open-collector acknowledge output
- Internal pull-up resistors on all B inputs
- Acknowledge timing control input
- 24-pin, 0.3″ space-saving package
- Fully TTL-compatible inputs and outputs
- IMOX™ high-performance IMplanted OXide isolated process

Multibus is a trademark of Intel Corporation.
IMOX is a trademark of Advanced Micro Devices, Inc.

FUNCTIONAL DESCRIPTION

Am29809 9-Bit Comparator

The Am29809 is a 9-bit "equal-to" comparator. Its combinatorial, active LOW output, $\overline{E}_{OUT}$, responds to the combination of a LOW input on the enable input $\overline{G}$ and a match between input words A and B.

Am29806 Chip Select Decoder

The Am29806 combines a 6-bit "equal-to" comparator with a 2- to 4-line decoder to select one-of-four active LOW chip select outputs. The selected output becomes active in response to the select inputs S_0, S_1 and is enabled by an active LOW input on the enable input $\overline{G}$ and a match between comparator inputs A and B. The active LOW output, Any Enable ($\overline{ANYE}$), responds to a valid comparison of A and B and is intended for use as an output enable control for data path buffers associated with the selected peripheral or board.

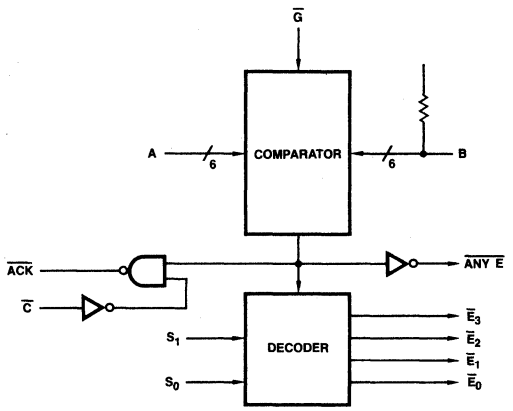
Both devices have open collector, active LOW acknowledge outputs with a conditional timing input $\overline{C}$ that may be driven by a timing circuit or wait state generator. The acknowledge output responds to a valid comparison, $\overline{G}$ = LOW and $\overline{C}$ = LOW.

Both devices have internal pull-up resistors on the comparator B-inputs for easy connection to SPST switches to ground selected input lines. The comparator function is described by:

$$\overline{E}_{OUT} = \overline{(A_0 \cdot B_0)\,(A_1 \cdot B_1)\,(A_2 \cdot B_2) \ldots (A_i \cdot B_i)\,\overline{G}}$$

BLOCK DIAGRAM

Am29806 (6-Bit)



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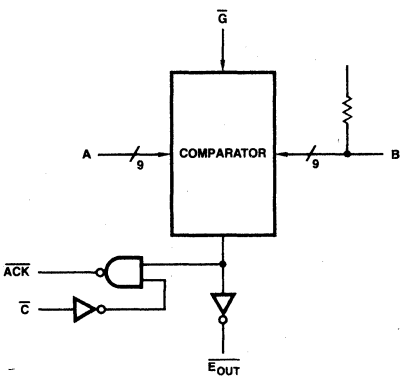
Am29809 (9-Bit)



ABL-035

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0 to +70°C V_{CC} = 5.0V ±10% MIN = 4.50V MAX = 5.5
MIL T_C = −55 to +125°C V_{CC} = 5.0V ±10% MIN = 4.50V MAX = 5.5

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage (Note 3)	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}		MIL I_{OH} = −2.0mA	2.5			Volts
				COM'L I_{OH} = −6.5mA	2.7			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}		$\overline{ACK}$ I_{OL} = 32mA			0.5	Volts
				All Others I_{OL} = 24mA				
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V		A_i			−0.4	mA
				B_i			−0.8	
				All Others			−0.8	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		A_i			20	µA
				B_i (Note 5)			−150	
				All Others			40	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V		A_i			0.1	mA
				B_i			0.2	
				All Others			0.2	
I_{SC}	Output Short Circuit Current (Note 3, 4)	V_{CC} = MAX			−60		−150	mA
I_{CC}	Power Supply Current (Note 6)	V_{CC} = MAX	Am29806	0 to 70°C				mA
				+70°C				
				−55 to +125°C			54	
				+125°C				
			Am29809	0 to 70°C				
				+70°C				
				−55 to +125°C			63	
				+125°C				

Notes: 1. For conditions shown as MIN or MAX, use the applicable value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Except open-collector acknowledge output.
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Due to internal pull-up resistor; 27KΩ nominal.
6. 29806: Worst-case is with all inputs LOW.
29809: Worst-case is with A = $\overline{G}$ = $\overline{C}$ = HIGH; B = LOW.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential Conditions	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} Max
DC Input Voltage (Note 7)	−0.5 to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30 to +5.0mA

Note: 7. B_i input voltage must not exceed V_{CC}.

Am29806
SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions (See Figure 2)	Min	Typ	Max	Units
t_{PLH}	A_i or B_i to $\overline{E}_i$ and $\overline{ANYE}$	C_L = 50pF, R_L = 1KΩ				ns
t_{PHL}						
t_{PLH}	$\overline{G}$ to $\overline{E}_i$ and $\overline{ANYE}$					ns
t_{PHL}						
t_{PLH} (Note 1)	$\overline{C}$ to $\overline{ACK}$	C_L = 50pF, R_L = 375Ω				ns
t_{PHL}						
t_{PLH} (Note 1)	$\overline{G}$ to $\overline{ACK}$					ns
t_{PHL}						
t_{PLH}	S_i to $\overline{E}_i$ (Two-Level Delay)	C_L = 50pF, R_L = 1KΩ				ns
t_{PHL}						
t_{PLH}	S_i to $\overline{E}_i$ (Three-Level Delay)					ns
t_{PHL}						
						ns

Am29806
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (See Figure 2)	COM'L T_A = 0 to +70°C, V_{CC} = 5.0V ±10% Min	COM'L Max	MIL T_A = −55 to +125°C, V_{CC} = 5.0V ±10% Min	MIL Max	Units
t_{PLH}	A_i or B_i to $\overline{E}_i$ and $\overline{ANYE}$	C_L = 50pF, R_L = 1KΩ					ns
t_{PHL}							
t_{PLH}	$\overline{G}$ to $\overline{E}_i$ and $\overline{ANYE}$						ns
t_{PHL}							
t_{PLH} (Note 1)	$\overline{C}$ to $\overline{ACK}$	C_L = 50pF, R_L = 375Ω					ns
t_{PHL}							
t_{PLH} (Note 1)	$\overline{G}$ to $\overline{ACK}$						ns
t_{PHL}							
t_{PLH}	S_i to $\overline{E}_i$ (Two-Level Delay)	C_L = 50pF, R_L = 1KΩ					ns
t_{PHL}							
t_{PLH}	S_i to $\overline{E}_i$ (Three-Level Delay)						ns
t_{PHL}							
							ns
							ns
							ns
							ns

Note: 1. This propagation time is dependent on the R_C time constant of the external load applied.

Am29806/809
Am29809
SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions (See Figure 2)	Min	Typ	Max	Units
t_{PLH}	A_i or B_i to $\overline{E_{OUT}}$	C_L = 50pF, R_L = 1KΩ				ns
t_{PHL}						
t_{PLH}	$\overline{G}$ to $\overline{E_{OUT}}$					ns
t_{PHL}						
t_{PLH} (Note 1)	$\overline{C}$ to $\overline{ACK}$	C_L = 50pF, R_L = 375Ω				ns
t_{PHL}						
t_{PLH} (Note 1)	$\overline{G}$ to $\overline{ACK}$					ns
t_{PHL}						
						ns
						ns
						ns

Am29809
SWITCHING CHARACTERISTICS
OVER OPERATING RANGE

Parameters	Description	Test Conditions (See Figure 2)	COM'L T_A = 0 to +70°C, V_{CC} = 5.0V ±10% Min	COM'L Max	MIL T_A = −55 to +125°C, V_{CC} = 5.0V ±10% Min	MIL Max	Units
t_{PLH}	A_i or B_i to $\overline{E_{OUT}}$	C_L = 50pF, R_L = 1KΩ					ns
t_{PHL}							
t_{PLH}	$\overline{G}$ to $\overline{E_{OUT}}$						ns
t_{PHL}							
t_{PLH} (Note 1)	$\overline{C}$ to $\overline{ACK}$	C_L = 50pF, R_L = 375Ω					ns
t_{PHL}							
t_{PLH} (Note 1)	$\overline{G}$ to $\overline{ACK}$						ns
t_{PHL}							
							ns
							ns
							ns
							ns
							ns

Note: 1. This propagation time is dependent on the R_C time constant of the external load applied.

DEFINITION OF FUNCTIONAL TERMS

A_i, B_i — Comparator data inputs. Each A_i is compared with each B_i on a bit basis. The comparator output is valid when all A_i bits match all B_i bits.

$\overline{ACK}$ — Active LOW open collector acknowledge output. This output acknowledges memory or I/O transfers when A and B match and $\overline{C}$ and $\overline{G}$ are LOW.

$\overline{ANYE}$ (Am29806) — Active LOW output. Any Enable ($\overline{ANYE}$) is LOW when $\overline{G}$ = LOW and there is a match between A and B.

$\overline{C}$ — Active LOW input. This input is used to control when $\overline{ACK}$ is active. It will normally be connected to GND when no wait states or timing delays need to be inserted. It may be connected to a wait state generator or timer.

$\overline{E_{OUT}}$ (Am29809) — Active LOW output. The comparator output is active for $\overline{G}$ = LOW and a match between A and B.

$\overline{G}$ — Active LOW input. The comparator's input enable determines if the comparator's output is valid. $\overline{G}$ is normally used as an expansion input (connected to Am29809 $\overline{E_{OUT}}$).

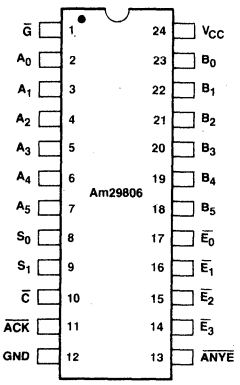
Am29806 Only

S_1, S_0 — Decoder select inputs. These inputs are decoded to produce a 1-of-4 selection of the $\overline{E_i}$ outputs.

$\overline{E_0}$, $\overline{E_1}$, $\overline{E_2}$, $\overline{E_3}$ — Active LOW outputs. 1-of-4 outputs is active as selected by S_1 and S_0.

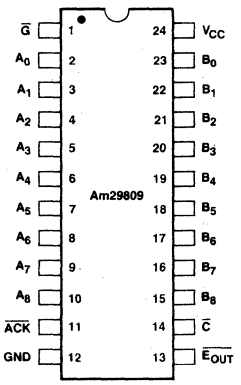
CONNECTION DIAGRAMS

Am29806



ABL-036

Am29809

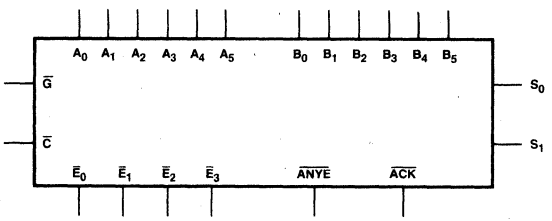


ABL-037

Note: Pin 1 is marked for orientation.

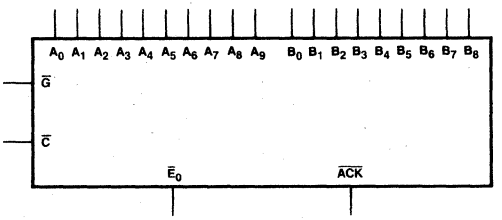
LOGIC SYMBOL

Am29806



ABL-038

Am29809



ABL-039

DECODER FUNCTION TABLE

$\overline{ANYE}$	S_0	S_1	E_0	E_1	E_2	E_3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
	L	H	H	L	H	H
	H	L	H	H	L	H
	H	H	H	H	H	L

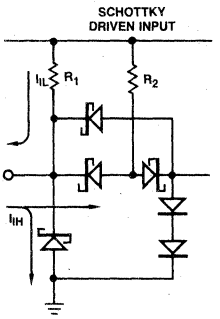
ACKNOWLEDGE FUNCTION TABLE

$\overline{ANYE}$ OR $\overline{E_{OUT}}$	$\overline{C}$	$\overline{ACK}$
H	X	H
X	H	H
L	L	L

COMPARATOR FUNCTION TABLE

$\overline{G}$	A	B	$\overline{E_{OUT}}$ or $\overline{ANYE}$
H	X	X	H
L	A = B		L
	A ≠ B		H

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



$C_I \approx 5.0pF$, all inputs
R_1* = 27K nominal
R_2 = 10K nominal

*Used only on B_i inputs.

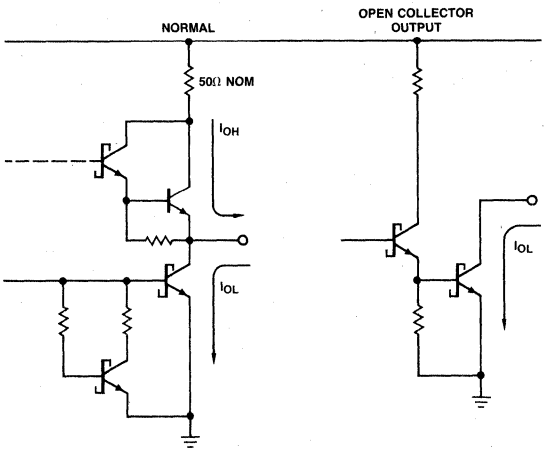
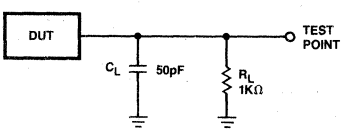


Figure 1.

ABL-041

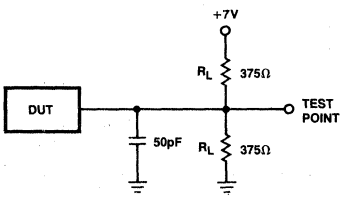
LOAD TEST CIRCUIT

Normal Output



ABL-042

Open-Collector Output



ABL-043

Note: C_L includes scope probe, wiring and stray capacitances without device in test fixture.

Figure 2.

Am29818

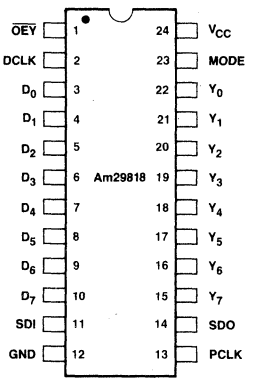
SSR™ Diagnostics/WCS Pipeline Register

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- High-speed noninverting 8-bit parallel register for any data path or pipelining application
- High-speed 8-bit "shadow register" with serial shift mode for Serial Shadow Register (SSR) Diagnostics
  - Controllability: serial scan in new machine state
  - Observability: serial scan out diagnostics routine results
- WCS (Writable Control Store) pipeline register
  - Load WCS from serial register
  - Read WCS via serial scan
- IMOX™ high performance IMplanted OXide isolated process
- 24-pin, 0.3" space saving package
- Alternate sourced as SN54/74S818

CONNECTION DIAGRAM



ABL-013

Leadless Chip Carrier
L-28-1

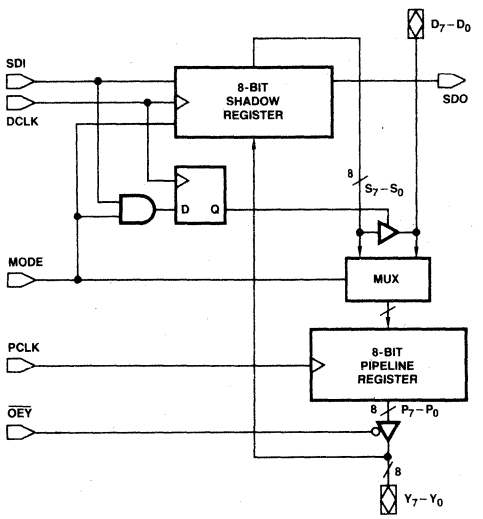
GENERAL DESCRIPTION

The Am29818 is a high-speed, general-purpose pipeline register with an on-board shadow register for performing Serial Shadow Register (SSR) Diagnostics and/or Writable Control Store loading.

The D-to-Y path provides an 8-bit parallel data path pipeline register for *normal* system operation. The shadow register can load parallel data to or from the pipeline register and can output data through the D input port (as in WCS loading).

The 8-bit shadow register has multiplexer inputs that select parallel inputs from the Y-port or adjacent bits in the shadow register to operate as a right-shift-only shift register. This register can then participate in a serial loop throughout the system where normal data, address, status and control registers are replaced with Am29818 Diagnostic Pipeline Registers. The loop can be used to scan in a complete test routine starting point (data, address, etc.). Then after a specified number of machine cycles scan out the results to be inspected for the expected results. WCS loading can be accomplished using the same technique. An instruction word can be serially shifted into the shadow register and written into the WCS RAM by enabling the D output.

BLOCK DIAGRAM



ABL-014

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ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise specified:

COM'L T_A = 0 to +70°C V_{CC} = 5.0V ±10% (MIN = 4.50V, MAX = 5.50V)
MIL T_C = −55 to +125°C V_{CC} = 5.0V ±10% (MIN = 4.50V, MAX = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	Y_0-Y_7: I_{OH} = −3mA D_0-D_7, SDO: I_{OH} = −1mA	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	Y_0-Y_7: I_{OL} = 16mA D_0-D_7, SDO: I_{OL} = 4mA			0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for all Inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for all Inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V	PCLK			−2.0	mA
			DCLK			−0.6	
			MODE, SDI, $\overline{OEY}$			−0.4	
			Y_0-Y_7, D_0-D_7			−0.45	
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.4V	DCLK, $\overline{OEY}$, MODE, SDI			50	µA
			PCLK, Y_0-Y_7, D_0-D_7			100	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX	V_O = 0.5V			−450	µA
			V_O = 2.4V			100	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX	Y_0-Y_7	−30		−100	mA
			D_0-D_7, SDO	−15		−50	
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX	0 to +70°C		120	155	mA
			+70°C			140	
			−55 to +125°C		120	165	
			+125°C			130	

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All three-state outputs are in the HIGH impedance state.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) under Bias	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5 to +V_{CC} max
DC Input Voltage	−0.5 to +5.5V
DC Output Current, into Outputs	25mA
DC Input Current	−30 to +5.0mA

Am29818
SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Test Conditions	COM'L T_A = 0 to +70°C, V_{CC} = 5V ±10% Min	COM'L Max	MIL T_C = −55 to +125°C, V_{CC} = 5V ±10% Min	MIL Max	Units
t_{PD}	PCLK → Y_x	See Test Output Load Conditions		13		18	ns
	MODE → SDO			16		18	ns
	SDI → SDO			16		18	ns
	DCLK → SDO			25		30	ns
t_S	D_x → PCLK		8		10		ns
	MODE → PCLK		15		15		ns
	Y_x → DCLK		5		5		ns
	MODE → DCLK		10		12		ns
	SDI → DCLK		10		12		ns
	DCLK → PCLK		15		15		ns
	DCLK → DCLK		40		45		ns
t_H	D_x → PCLK		0		0		ns
	MODE → PCLK		0		0		ns
	Y_x → DCLK		5		5		ns
	MODE → DCLK		0		0		ns
	SDI → DCLK		0		0		ns
t_{LZ}	$\overline{OEY}$ → Y_x			15		20	ns
	DCLK → D_x			45		45	ns
t_{HZ}	$\overline{OEY}$ → Y_x			25		30	ns
	DCLK → D_x			80		90	ns
t_{ZL}	$\overline{OEY}$ → Y_x			15		20	ns
	DCLK → D_x			25		35	ns
t_{ZH}	$\overline{OEY}$ → Y_x			15		20	ns
	DCLK → D_x			25		30	ns
t_{PW}	PCLK (HIGH and LOW)		15		15		ns
	DCLK (HIGH and LOW)		25		25		ns

*AC performance over the operating range is guaranteed by testing defined in Group A, Subgroup 9.

Am29818

SWITCHING CHARACTERISTICS

Parameters	Description	Test Conditions	T_A = +25°C, V_{CC} = 5.0V Min	Typ	Max	Units
t_{PD}	PCLK → Y_x	See Test Output Load Conditions		10	12	ns
	MODE → SDO			10	14	ns
	SDI → SDO			10	14	ns
	DCLK → SDO			17	22	ns
t_S	D_x → PCLK		8			ns
	MODE → PCLK		12			ns
	Y_x → DCLK		5			ns
	MODE → DCLK		10			ns
	SDI → DCLK		10			ns
	DCLK → PCLK		12			ns
	DCLK → DCLK		35			ns
t_H	D_x → PCLK		0			ns
	MODE → PCLK		0			ns
	Y_x → DCLK		5			ns
	MODE → DCLK		0			ns
	SDI → DCLK		0			ns
t_{LZ}	$\overline{OEY}$ → Y_x				12	ns
	DCLK → D_x				35	ns
t_{HZ}	$\overline{OEY}$ → Y_x				22	ns
	DCLK → D_x				80	ns
t_{ZL}	$\overline{OEY}$ → Y_x				15	ns
	DCLK → D_x				25	ns
t_{ZH}	$\overline{OEY}$ → Y_x				15	ns
	DCLK → D_x				20	ns
t_{PW}	PCLK (HIGH and LOW)		15			ns
	DCLK (HIGH and LOW)		25			ns

ORDERING INFORMATION

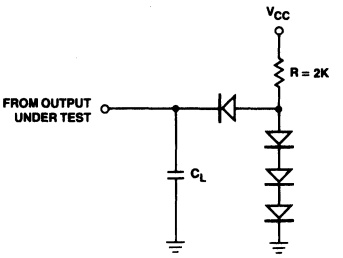
Order the part number according to the table below to obtain the desired package, temperature range and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM29818DC	D-24-SLIM	C	C-1
AM29818DC-B	D-24-SLIM	C	B-2 (Note 4)
AM29818DM	D-24-SLIM	M	C-3
AM29818DM-B	D-24-SLIM	M	B-3
AM29818LC	L-28-1	C	C-1
AM29818LC-B	L-28-1	C	B-2 (Note 4)
AM29818LM	L-28-1	M	C-3
AM29818LM-B	L-28-1	M	B-3
AM29818XC	Dice	C	Visual inspection to MIL-STD-883. Method 2010B.
AM29818XM	Dice	M	

Notes: 1. D = Hermetic DIP, L = Chip-Pak, Number following letter is number of leads.
2. C = 0 to +70°C, V_{CC} = 4.5 to 5.5V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 160 hour burn-in.

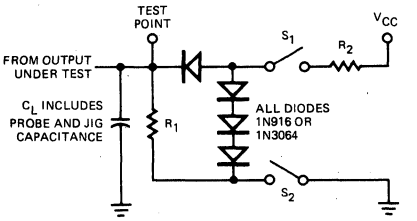
TEST OUTPUT LOAD CONFIGURATIONS FOR Am29818

SDO OUTPUT



ABL-015

THREE-STATE OUTPUTS

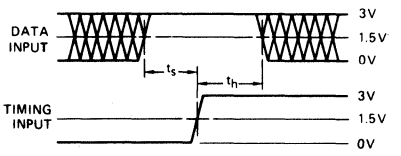


ABL-016

	R_1	R_2
$Y_0 - Y_7$	1K	280
$D_0 - D_7$	5K	2K

Note 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.

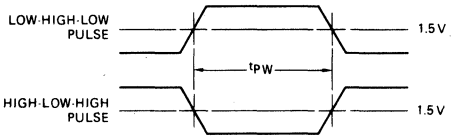
SET UP, HOLD, AND RELEASE TIMES



ABL-017

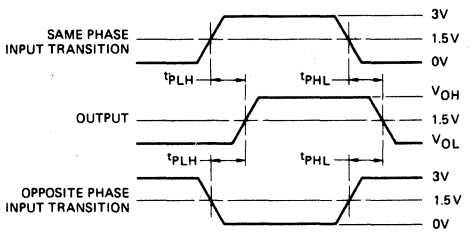
Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

PULSE WIDTH



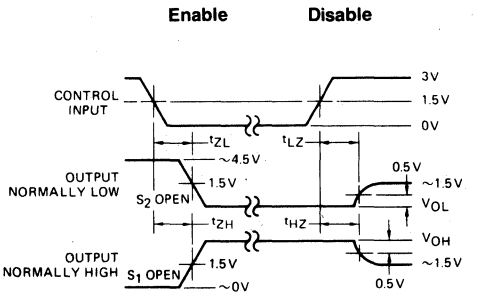
ABL-018

PROPAGATION DELAY



ABL-019

ENABLE AND DISABLE TIMES



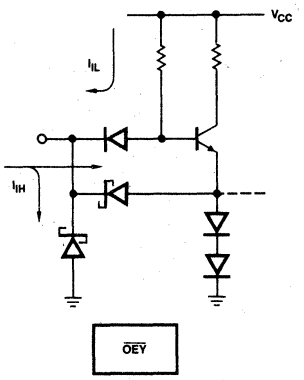
ABL-020

Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1 and S_2 of Load Circuit are closed except where shown.

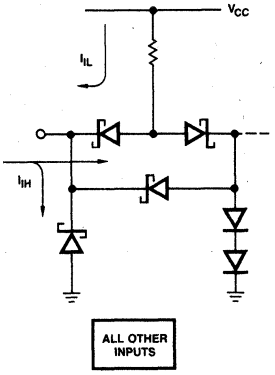
Note: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_o = 50Ω; t_r ≤ 2.5ns; t_f ≤ 2.5ns.

8

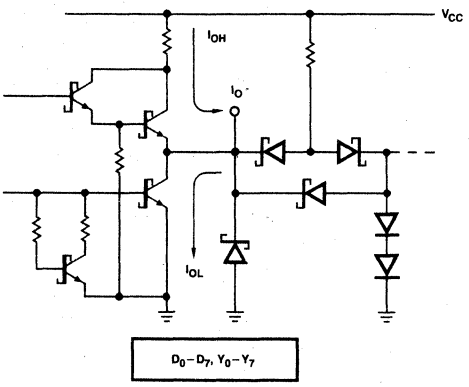
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



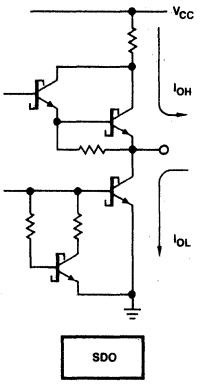
ABL-021



ABL-022

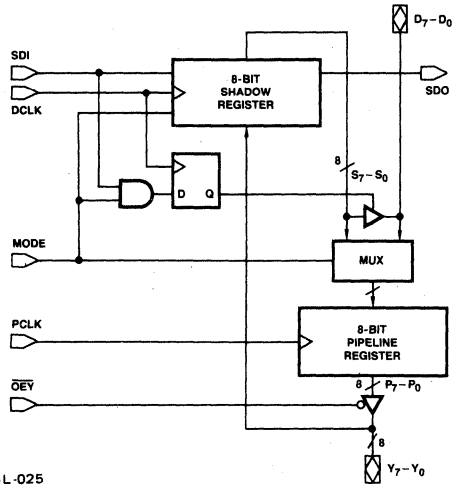


ABL-023



ABL-024

BLOCK DIAGRAM



ABL-025

DEFINITION OF FUNCTIONAL TERMS

D_7-D_0 Parallel data input to the pipeline register or parallel data output from the shadow register (see Function Table for control modes).

DCLK Diagnostics/WCS clock for loading shadow register (serial or parallel modes – see Function Table).

MODE Control input for pipeline register multiplexer and shadow register control (see Function Table).

$\overline{OEY}$ Active LOW output enable for Y-port.

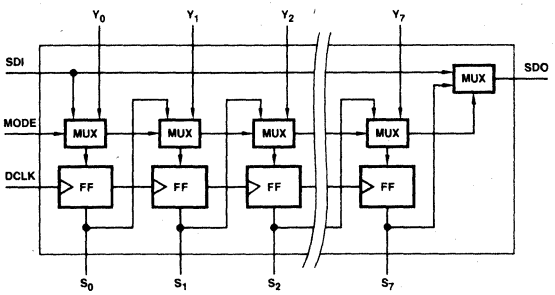
PCLK Pipeline register clock input loads D-port or shadow register contents on LOW-to-HIGH transition.

SDI Serial Data Input to shadow register. (See Function Table.)

SDO Serial Data Output from shadow register.

Y_7-Y_0 Data Outputs from the pipeline register and parallel inputs to the shadow register.

SHADOW REGISTER



ABL-026

Am29818 FUNCTION TABLE DESCRIPTION

Data transfers into the shadow register occur on the LOW-to-HIGH transition of DCLK. MODE and SDI determines what data source will be loaded. The pipeline register is loaded on the LOW-to-HIGH transition of PCLK. MODE selects whether the data source is the data input or the shadow register output. Because of the independence of the clock inputs data can be shifted in the shadow register via DCLK and loaded into the pipeline register from the data input via PCLK simultaneously. As long as no set-up or hold times are violated, this simultaneous operation is legal.

Inputs				Outputs			
SDI	MODE	DCLK	PCLK	SDO	Shadow Register	Pipeline Register	Operation
X	L	↑	X	S_7	$S_i \leftarrow S_{i-1}$ $S_o \leftarrow$ SDI	NA	Serial Shift; D_7-D_0 Disabled
X	L	X	↑	S_7	NA	$P_i \leftarrow D_i$	Normal Load Pipeline Register
L	H	↑	X	L	$S_i \leftarrow Y_i$	NA	Load Shadow Register from Y; D_7-D_0 Disabled
X	H	X	↑	SDI	NA	$P_i \leftarrow S_i$	Load Pipeline Register from Shadow Register
H	H	↑	X	H	Hold	NA	Hold Shadow Register; D_7-D_0 Enabled

FUNCTION TABLE DEFINITIONS

INPUTS

H = HIGH
L = LOW
X = Don't Care
↑ = LOW-to-HIGH transition

OUTPUTS

S_7-S_0 = Shadow Register outputs
P_7-P_0 = Pipeline Register outputs
D_7-D_0 = Data I/O port
Y_7-Y_0 = Y I/O port
NA = Not applicable; output is not a function of the specified input combinations.

AN INTRODUCTION TO SERIAL SHADOW REGISTER (SSR) DIAGNOSTICS

DIAGNOSTICS

A diagnostics capability provides the necessary functionality as well as a systematic method for detecting and pin-pointing hardware related failures in a system. This capability must be able to both *observe* intermediate test points and *control* intermediate signals – address, data, control and status – to exercise all portions of the system under test. These two capabilities, observability and controllability, provide the ability to establish a desired set of input conditions and state register values, sample the necessary outputs, and determine whether the system is functioning correctly.

TESTING COMBINATIONAL AND SEQUENTIAL NETWORKS

The problem of testing a combinational logic network is well understood (Figure 1). Sets of input signals (test vectors) are applied to the network and the network outputs are compared to the set of computed outputs (result vectors). In some cases sets of test vectors and result vectors can be generated in a computer-aided environment, minimizing engineering effort. Additionally, fault coverage analysis can be automated to provide a measure of how efficient a set of test vectors is at pin-pointing hardware failures. For example, a popular measure of fault coverage computes the percentage of stuck-at-ones (nodes with outputs always HIGH) and stuck-at-zeros (nodes with outputs always LOW) a given set of test vectors will discover.

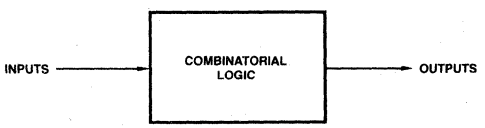
A sequential network (Figure 2) is much more difficult to test systematically. The outputs of a sequential network depend not only on the present inputs but also on the internal state of the network. Initializing the internal state register to the value necessary to test a given set of inputs is difficult at best, and not easily automated. Additionally, observing the internal state of a sequential network can be very difficult and time consuming if the state information is not directly available. For example, consider the problem of determining the value of an internal 16-bit counter if only a carry-out signal is available. The counter must be clocked until it reaches the carry-out state and the starting value computed. Up to 65,535 clock cycles may be necessary! An easier method must exist. Serial Shadow Register diagnostics provides this method.

SERIAL SHADOW REGISTER DIAGNOSTICS

Serial Shadow Register diagnostics provides sufficient observability and controllability to turn any sequential network into a combinational network. This is accomplished by providing the means to both initialize (control) and sample (observe) the state elements of a sequential network. Figure 3 shows the method by which serial shadow register diagnostics accomplishes these two functions.

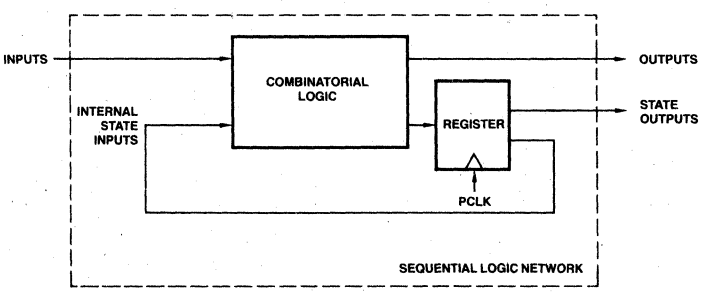
Serial Shadow Register diagnostics utilizes an extra multiplexer on the input of each state register and a duplicate or shadow of each state flip/flop in an additional register. The shadow register can be loaded serially via the serial data input (thus the name

Figure 1.



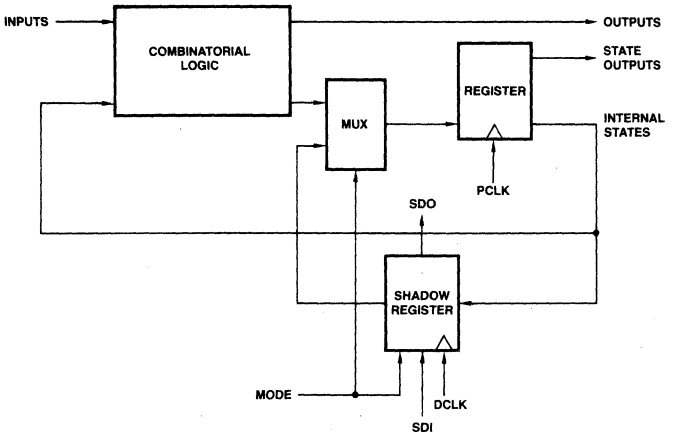
ABL-027

Figure 2.



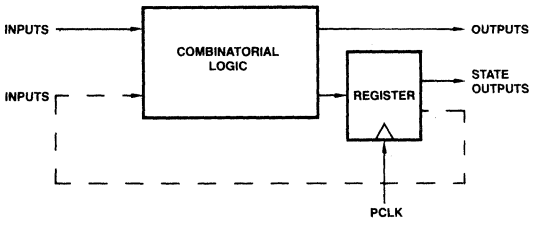
ABL-028

Figure 3.



ABL-029

Figure 4.



ABL-030

Serial Shadow Register diagnostics) for controllability. Once the desired state information is loaded into the serial register it can be transferred into the internal state register by selecting the multiplexer and clocking the state register with PLCK. This allows any internal state to be set to a desired state in a simple, quick, and systematic manner.

Internal state information can be sampled by loading the serial register from the state register outputs. This state information can then be shifted out via the serial data output to provide observability. Notice that the serial data inputs and outputs can be cascaded to make long chains of state information available on a minimum number of connections.

In effect, Serial Shadow Register diagnostics breaks the normal feedback path of the sequential network and establishes a logical path with which inputs can be defined and outputs sampled (Figure 4). This means that those techniques which have been developed to test combinational networks can be applied to any sequential network in which Serial Shadow Register diagnostics is utilized.

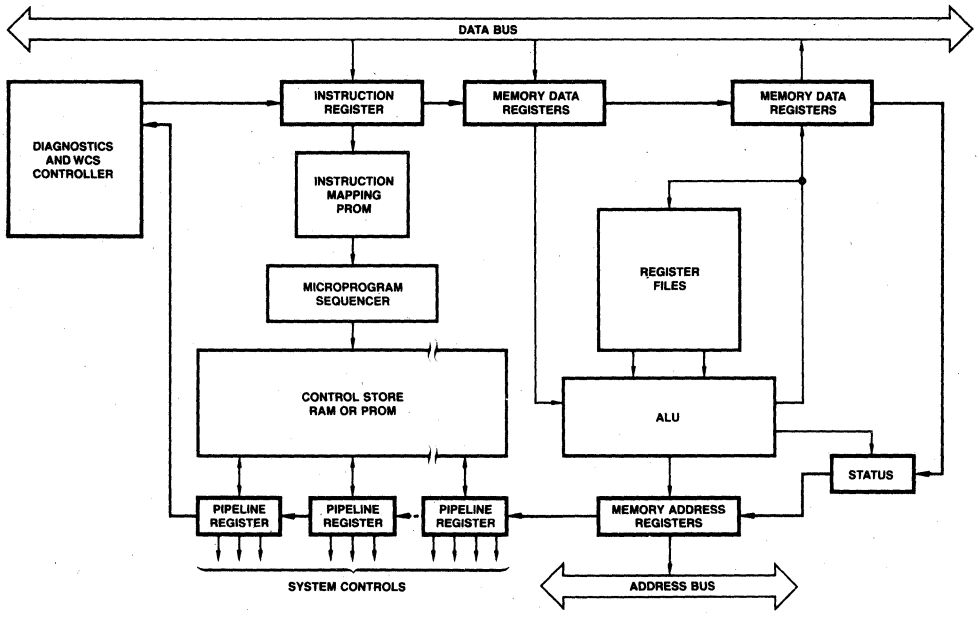
A TYPICAL COMPUTER ARCHITECTURE WITH SSR DIAGNOSTICS

When normal pipeline registers are replaced by SSR diagnostics pipeline registers system debug and diagnostics are easily implemented. State information which was inaccessible is now both observable and controllable. Figure 5 shows a typical computer system using the Am29818.

Serial paths have been added to all the important state registers (macro instruction, data, status, address, and micro instruction registers). This extra path will make it easier to diagnose system failures by breaking the feed-back paths and turning sequential state machines into combinatorial logic blocks. For example, the status outputs of the ALU may be checked by loading the micro instruction register with the necessary micro instruction. The desired ALU function is then executed and the status outputs captured in the status register. The status bits can then be serially shifted out and checked for validity.

A single diagnostic loop was shown in Figure 5 for simplicity, but several loops can be employed in more complicated systems to reduce scan time. Additionally, the Am29818's can be used to sample intermediate test points not associated with normal state information. These additional test points can further ease diagnostics, testability and debug.

Figure 5. Typical System Configuration



SSR DIAGNOSTICS/WCS PIPELINE REGISTERS
REPLACE NORMAL REGISTERS WITH DIAGNOSTICS LOOP

ABL-031

USE OF THE Am29818 PIPELINE REGISTER IN WRITABLE CONTROL STORE (WCS) DESIGNS

The Am29818 SSR diagnostics/WCS Pipeline Register was designed specifically to support writable control store designs. In the past, designers of WCS based systems needed to use an excessive amount of support circuitry to implement a WCS. As shown in Figure 7 additional input and output buffers are necessary to provide paths from the parallel input data bus to the memory, and from the instruction register to the output data bus. The input port is necessary to write data to the control store, initializing the micromemory. The output port provides the access to the instruction register, indirectly allowing the RAM to be read. Additionally, access to the instruction register is useful during system debugging and system diagnostics.

The Am29818 supports all of the above operations (and more) without any support circuitry. Figure 6 shows a typical WCS design with the Am29818. Access to memory is now possible over the serial diagnostics port. The instruction register contents may be read by serially shifting the information out on the diagnostics port. Additionally, the instruction register may be written from the serial port via the shadow register. This simplifies system debug and diagnostics operations considerably.

CONCLUSION

Serial Shadow Register diagnostics provides the observability and controllability necessary to take any sequential network and turn it into a combinational network. This provides a method for pin-pointing digital system hardware failures in a systematic and well understood fashion.

Figure 6. Am29818 Based WCS Application.

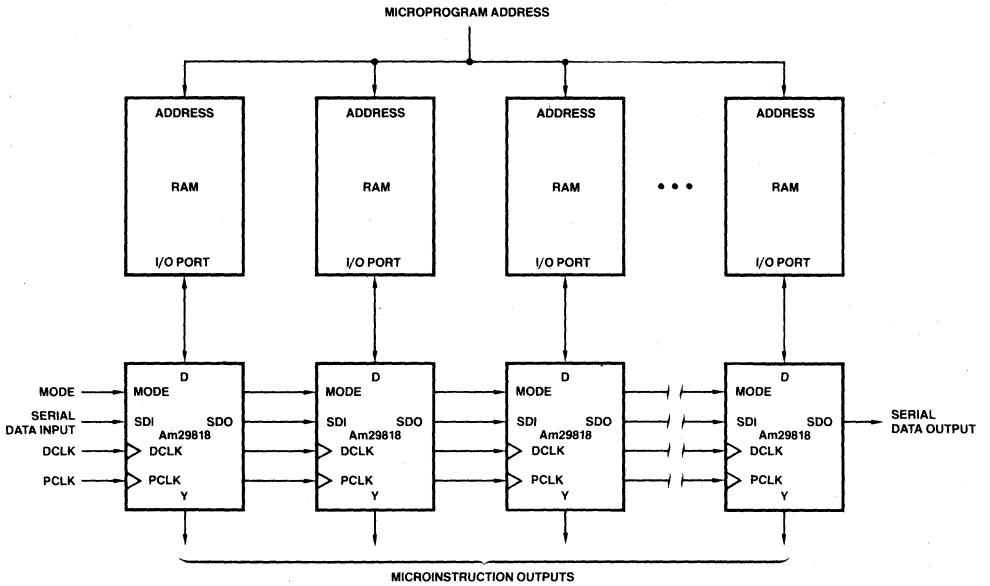


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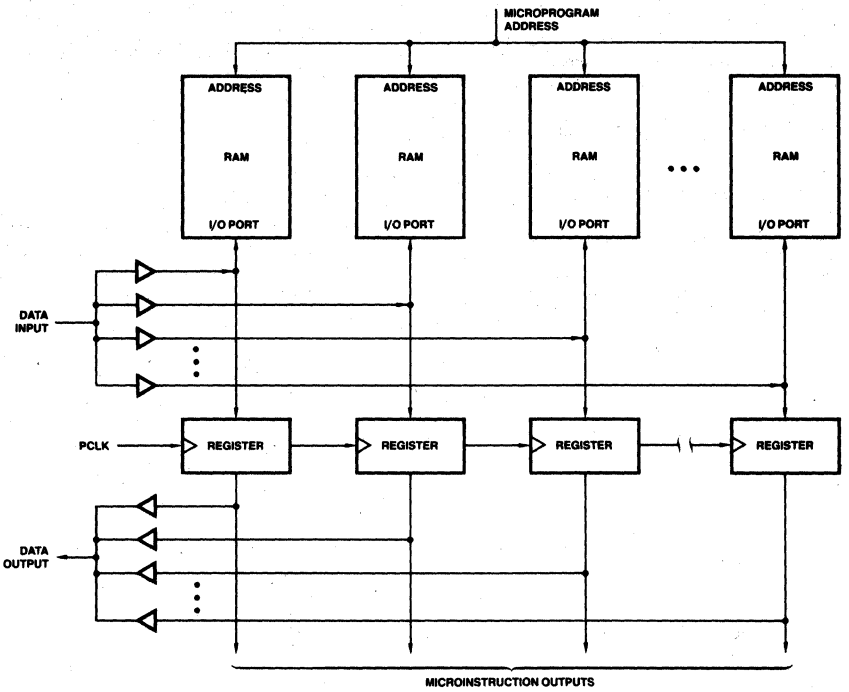
Figure 7. WCS Application without Am29818s.



ABL-033

Am29821/822 • Am29823/824 • Am29825/826

High Performance Bus Interface Registers

DISTINCTIVE CHARACTERISTICS

- High-speed parallel registers with positive edge-triggered D-type flip-flops
  - Noninverting CP-Y t_{PD} = 7.5ns typ
  - Inverting CP-Y t_{PD} = 7.5ns typ
- Buffered common Clock Enable ($\overline{EN}$)
- Buffered common asynchronous Clear input ($\overline{CLR}$)
- Three-state outputs glitch free during power-up and down
- Outputs have Schottky clamp to ground
- 48mA Commercial I_{OL}, 32mA MIL I_{OL}
- Low input/output capacitance
  - 6pF inputs (typical)
  - 8pF outputs (typical)
- Metastable "Hardened" Registers
- I_{OH} specified at 2.0V and 2.4V
- 24-pin 0.3" space saving package
- IMOX™ high performance IMplanted OXide isolated process

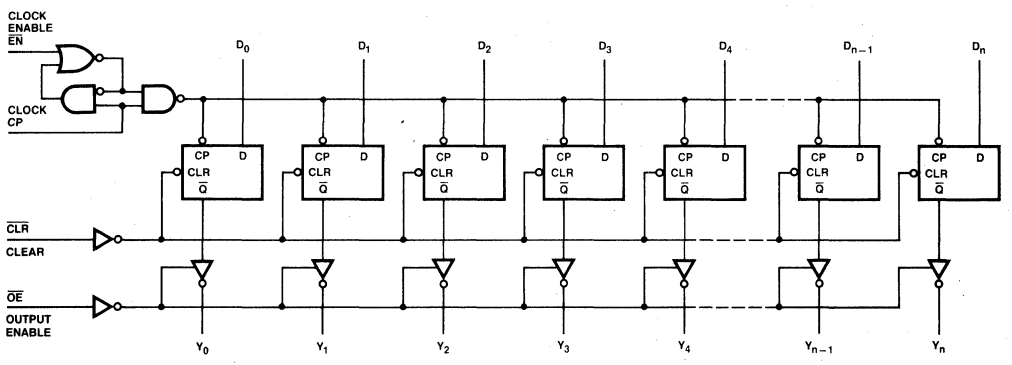
FUNCTIONAL DESCRIPTION

The Am29820 Series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The Am29821 and Am29822 are buffered, 10-bit wide versions of the popular '374/'534 functions. The Am29823 and Am29824 are 9-bit wide buffered registers with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high performance microprogrammed systems. The Am29825 and Am29826 are 8-bit buffered registers with all the '823/4 controls plus multiple enables ($\overline{OE_1}$, $\overline{OE_2}$, $\overline{OE_3}$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the Am29800 high performance interface family are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

	Device		
	10-Bit	**9-Bit**	**8-Bit**
Noninverting	Am29821	Am29823	Am29825
Inverting	Am29822	Am29824	Am29826

LOGIC DIAGRAM



LBI-001

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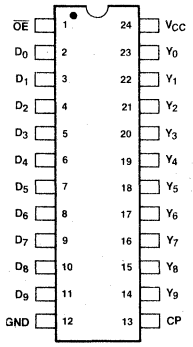
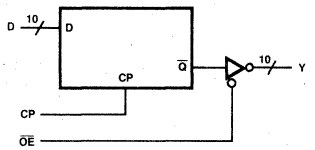
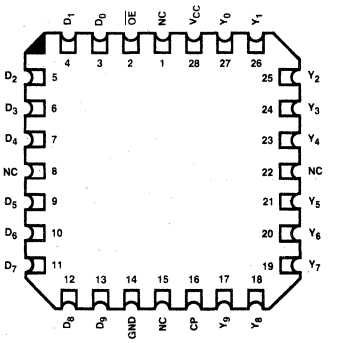
Am29821/Am29822
10-BIT REGISTERS
Top Views

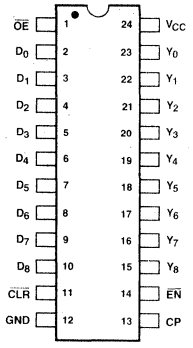


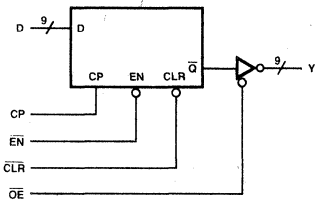


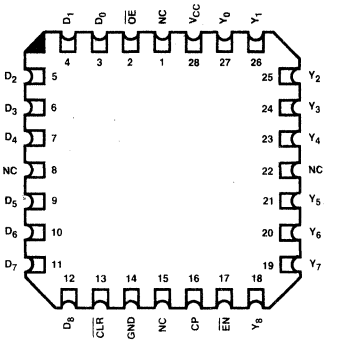


LBI-002

Am29823/Am29824
9-BIT REGISTERS
Top Views

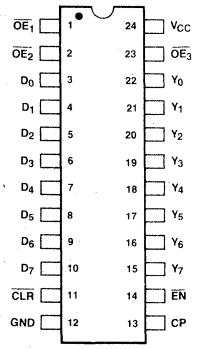


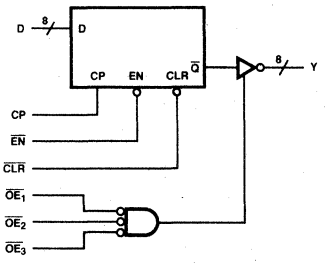


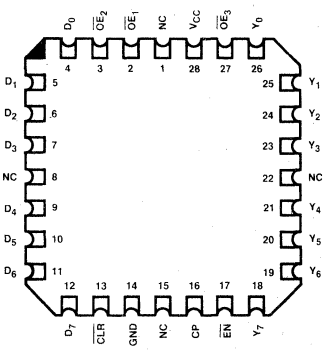


LBI-003

Am29825/Am29826
8-BIT REGISTERS
Top Views







LBI-004

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	T_A = 0 to +70°C	V_{CC} = 5.0V ±10%	MIN = 4.50V	MAX = 5.50V
MIL	T_C = −55 to +125°C	V_{CC} = 5.0V ±10%	MIN = 4.50V	MAX = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15mA		2.4	3.3		Volts
			I_{OH} = −24mA		2.0	3.1		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OL} = 32mA			0.31	0.5	Volts
			COM'L, I_{OL} = 48mA			0.38	0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−0.7	−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V	Data, $\overline{CLR}$			−0.3	−1.0	mA
			$\overline{OE}$, $\overline{EN}$, CP			−1.2	−2.0	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V					50	µA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_{OZ}	Output Off-state (High Impedance) Output Current	V_{CC} = MAX	V_O = 0.4V				−50	µA
			V_O = 2.4V				50	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX			−75	−160	−250	mA
I_{CC}	Supply Current (Note 4)	V_{CC} = MAX, Outputs Open, $\overline{EN}$ = LOW	Outputs Enabled ($\overline{OE}$ = LOW)	0 to +70°C		86	125	mA
				+70°C		65	105	mA
				−55 to +125°C		86	125	mA
				+125°C		65	105	mA
			Outputs Disabled ($\overline{OE}$ = HIGH)	0 to +70°C		97	140	mA
				+70°C		83	120	mA
				−55 to +125°C		97	140	mA
				+125°C		83	120	mA

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
2. All typical values are V_{CC} = 5.0V, T_A = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
4. Clock input, CP, is HIGH after clocking in data to produce outputs = LOW.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5 to +V_{CC} max
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	100mA
DC Input Current	−30 to +5.0mA

8

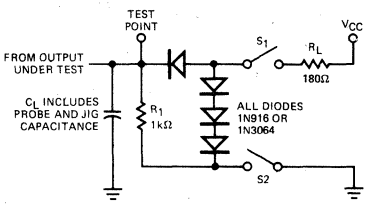
SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions (Note 4)	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Clock to Y_i ($\overline{OE}$ = LOW)	C_L = 50pF	3.5		7.5	ns
t_{PHL}			3.5		9.5	ns
t_{PLH}		C_L = 300pF			14	ns
t_{PHL}					14	ns
t_S	Data to $\overline{CP}$ Setup Time	C_L = 50pF	2.0	0		ns
t_H	Data to $\overline{CP}$ Hold Time		2.0	0.5		ns
t_S	Enable ($\overline{EN}$ ↑) to CP Setup Time		3.0	1.5		ns
t_S	Enable ($\overline{EN}$ ↓) to CP Setup Time		3.0	1.5		ns
t_H	Enable ($\overline{EN}$) Hold Time		0	−1.5		ns
t_{PHL}	Propagation Delay, Clear to Y_i			12.9	15.0	ns
t_S	Clear Recovery ($\overline{CLR}$ ↓) Time		5.0	1.1		ns
t_{PWH}	Clock Pulse Width HIGH	C_L = 50pF	5.0	6.5		ns
t_{PWL}	Clock Pulse Width LOW		5.0	3.0		ns
t_{PWL}	Clear ($\overline{CLR}$ = LOW) Pulse Width		5.0	5.7		ns
t_{ZH}	Output Enable Time $\overline{OE}$ ↓ to Y_i	C_L = 300pF			17	ns
t_{ZL}					17	ns
t_{ZH}		C_L = 50pF		11.5	12	ns
t_{ZL}				11.0	12	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ↓ to Y_i	C_L = 50pF			9	ns
t_{LZ}					9	ns
t_{HZ}		C_L = 5pF		5.2	8	ns
t_{LZ}				5.5	8	ns

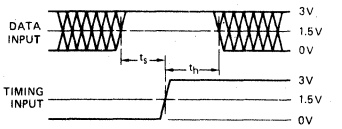
Note: 4. See test circuit and waveforms.

LOAD TEST CIRCUIT



LBI-005

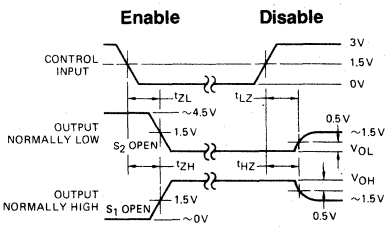
SET UP, HOLD, AND RELEASE TIMES



LBI-007

Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

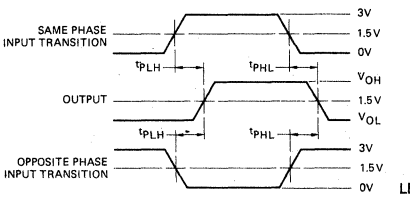
ENABLE AND DISABLE TIMES



LBI-006

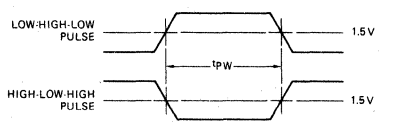
Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1 and S_2 of Load Circuit are closed except where shown.

PROPAGATION DELAY



LBI-008

PULSE WIDTH



LBI-009

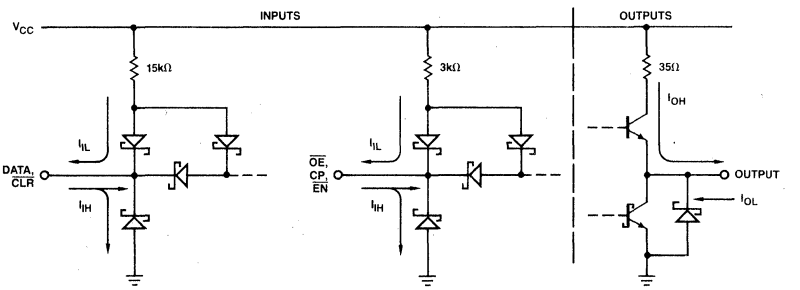
Note: Pulse Generator for All Pulses: Rate ≤ 10MHz; Z_O = 50Ω; t_r ≤ 2.5ns; t_f ≤ 2.5ns.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description		Test Conditions (Note 4)	Commercial T_A = 0 to +70°C, V_{CC} = 5.0V ±10% Min	Commercial Max	Military T_C = −55 to +125°C, V_{CC} = 5.0V ±10% Min	Military Max	Units
t_{PLH}	Propagation Delay Clock to Y_i ($\overline{OE}$ = LOW)		C_L = 50pF	3.5	8.5	3.5	10	ns
t_{PHL}				3.5	11	3.5	12	ns
t_{PLH}			C_L = 300pF		13		15	ns
t_{PHL}					15		17	ns
t_S	Data to CP Setup Time			4		4		ns
t_H	Data to CP Hold Time			2		2		ns
t_S	Enable ($\overline{EN}$ ↓) to CP Setup Time			5		5		ns
t_S	Enable ($\overline{EN}$ ↑) to CP Setup Time			5		5		ns
t_H	Enable ($\overline{EN}$) Hold Time			0		0		ns
t_{PHL}	Propagation Delay, Clear to Y		C_L = 50pF		20		20	ns
t_S	Clear Recovery ($\overline{CLR}$ ↑) Time			7		7		ns
t_{PWH}	Clock Pulse Width	HIGH		7		7		ns
t_{PWL}		LOW		7		7		ns
t_{PWH}	Enable ($\overline{EN}$) Pulse Width	HIGH						ns
t_{PWL}		LOW						ns
t_{PWL}	Clear ($\overline{CLR}$ = LOW) Pulse Width			7				ns
t_{ZH}	Output Enable Time $\overline{OE}$ ↓ to Y_i		C_L = 300pF		20		22	ns
t_{ZL}					20		22	ns
t_{ZH}			C_L = 50pF		14		15	ns
t_{ZL}					14		15	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ↑ to Y_i		C_L = 50pF		16		18	ns
t_{LZ}					12		12	ns
t_{HZ}			C_L = 5pF		9		10	ns
t_{LZ}					9		10	ns

Note: 4. See test circuit and waveforms.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



LBI-010

DEFINITION OF FUNCTIONAL TERMS

D_i The D flip-flop data inputs.

$\overline{CLR}$ For both inverting and noninverting registers, when the clear input is LOW and $\overline{OE}$ is LOW, the Q_i outputs are LOW. When the clear input is HIGH, data can be entered into the register.

CP Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.

Y_i, $\overline{Y}_i$ The register three-state outputs.

$\overline{EN}$ Clock Enable. When the clock enable is LOW, data on the D_i input is transferred to the Q_i output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_i outputs do not change state, regardless of the data or clock input transitions. (Note 5.)

$\overline{OE}$ Output Control. When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

FUNCTION TABLE Am29821/29823/29825

	Inputs					Internal	Outputs
Function	$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_i	CP	Q_i	Y_i
Hi-Z	H	X	L	L	↑	L	Z
	H	X	L	H	↑	H	Z
Clear	H	L	X	X	X	L	Z
	L	L	X	X	X	L	L
Hold	H	H	H	X	X	NC	Z
	L	H	H	X	X	NC	NC
Load	H	H	L	L	↑	L	Z
	H	H	L	H	↑	H	Z
	L	H	L	L	↑	L	L
	L	H	L	H	↑	H	H

H = HIGH NC = No Change
L = LOW ↑ = LOW-to-HIGH Transition
X = Don't Care Z = High Impedance

FUNCTION TABLE Am29822/29824/29826

	Inputs					Internal	Outputs
Function	$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_i	CP	Q_i	$\overline{Y}_i$
Hi-Z	H	X	L	L	↑	H	Z
	H	X	L	H	↑	L	Z
Clear	H	L	X	X	X	L	Z
	L	L	X	X	X	L	L
Hold	H	H	H	X	X	NC	Z
	L	H	H	X	X	NC	NC
Load	H	H	L	L	↑	H	Z
	H	H	L	H	↑	L	Z
	L	H	L	L	↑	H	H
	L	H	L	H	↑	L	L

H = HIGH NC = No Change
L = LOW ↑ = LOW-to-HIGH Transition
X = Don't Care Z = High Impedance

Note 5: The Am29823 thru Am29826 registers achieve short throughput delay and setup time and reduced power consumption by means of a clock gating and latching circuit. This circuit is sensitive to very short (<3ns) HIGH-to-LOW-to-HIGH going spikes on $\overline{EN}$ while CP is HIGH. The designer should be aware of this and avoid the use of decoders or other potentially glitching devices in the $\overline{EN}$ logic.

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

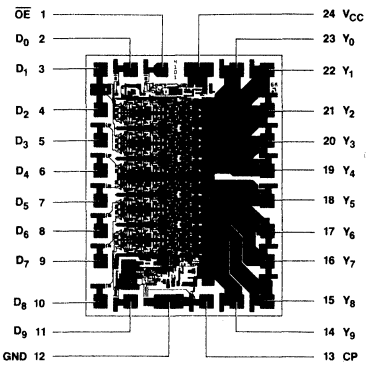
Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2982_DC	D-24-SLIM	C	C-1
AM2982_DCB	D-24-SLIM	C	B-2 (Note 4)
AM2982_DM	D-24-SLIM	M	C-3
AM2982_DMB	D-24-SLIM	M	B-3
AM2982_LC	L-28-1	C	C-1
AM2982_LCB	L-28-1	C	B-2 (Note 4)
AM2982_LM	L-28-1	M	C-3
AM2982_LMB	L-28-1	M	B-3
AM2982_XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2982_XM	Dice	M	

Notes: 1. D = Hermetic DIP, L = Chip-Pak. Number following letter is number of leads.
2. C = 0 to +70°C, V_{CC} = 4.5 to 5.5V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 160 hour burn-in.

METALLIZATION AND PAD LAYOUTS

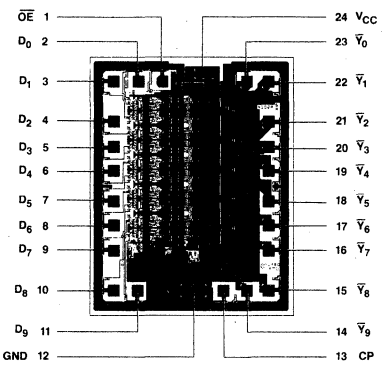
10-Bit Registers

Am29821



LBI-011

Am29822

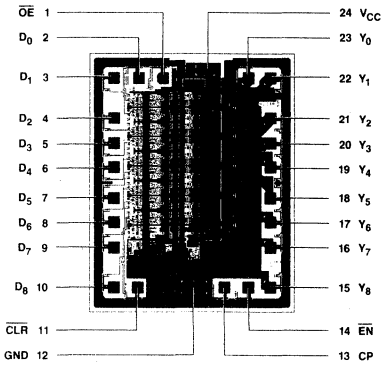


LBI-012

DIE SIZE 0.084" X 0.064"

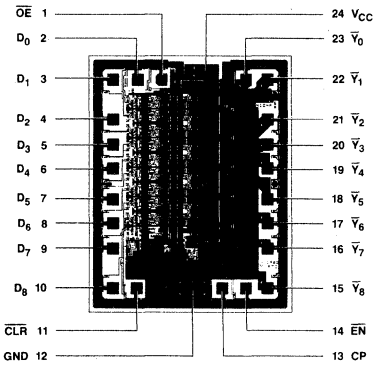
9-Bit Registers

Am29823



LBI-013

Am29824

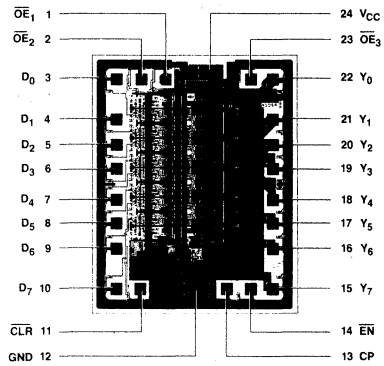


LBI-014

DIE SIZE 0.084" X 0.064"

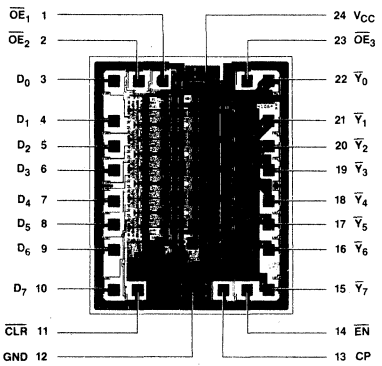
8-Bit Registers

Am29825



LBI-015

Am29826



LBI-016

DIE SIZE 0.084" X 0.064"

8

Am29827/Am29828

High Performance Buffers

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

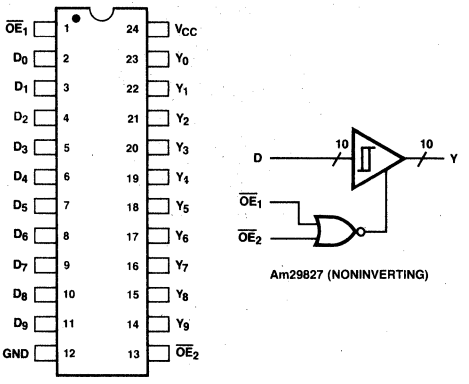
- High-speed buffers and inverters
  - Noninverting t_{PD} = 4.5ns typ
  - Inverting t_{PD} = 4.0ns typ
- 200mV minimum input hysteresis on input data ports
- Three-state outputs glitch-free during power-up and -down
- Outputs have Schottky clamp to ground
- 48mA commercial I_{OL}, 32mA military I_{OL}
- High capacitance load capability
- Low capacitance inputs and outputs
- I_{OH} specified 2.0V and 2.4V
- 24-pin 0.3" space saving package
- Fully TTL compatible inputs and outputs
- IMOX™ high performance IMplanted OXide isolated process

FUNCTIONAL DESCRIPTION

The Am29827 and Am29828 10-bit bus buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NOR-ed output enables for maximum control flexibility. All buffer data inputs have 200mV minimum input hysteresis to provide improved noise rejection.

All of the Am29800 high performance interface family are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

Am29827/Am29828
10-BIT BUS DRIVERS



Am29827 (NONINVERTING)

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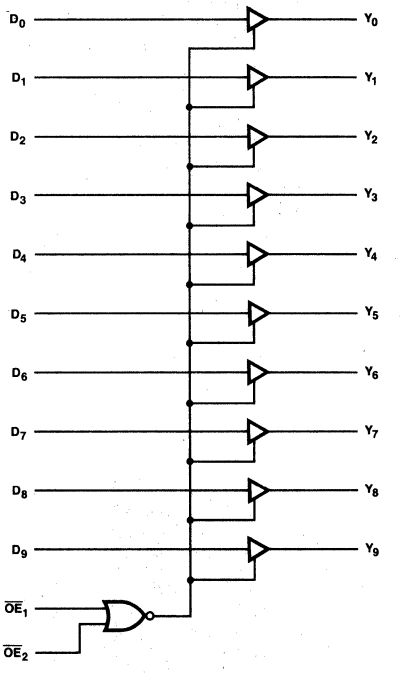
Am29827/Am29828
10-BIT BUFFERS



ABI-127

IMOX is a trademark of Advanced Micro Devices, Inc.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Output for High Output State	−1.5 to V_{CC} max
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	100mA
DC Input Current	−30 to +5.0mA

ELECTRICAL CHARACTERISTICS

COM'L T_A = 0 to +70°C, V_{CC} = 5.0V ± 10% (MIN = 4.5V, MAX = 5.5V)
MIL T_C = −55 to +125°C, V_{CC} = 5.0V ± 10% (MIN = 4.5V, MAX = 5.5V)

Parameter	Description	Test Conditions		Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15mA	2.4			V
			I_{OH} = −24mA	2.0			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OL} = 32mA			0.5	V
			COM'L, I_{OL} = 48mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	V
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	V
V_{HYST}	Input Hysteresis	V_{CC} = MIN		200			mV
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V				−1.0	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{OZH}	Output Off-state Output Current (HI-Z)	V_{CC} = MAX, V_O = 2.4V				50	μA
I_{OZL}	Output Off-state Output Current (HI-Z)	V_{CC} = MAX, V_O = 0.4V				−50	μA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX		−75		−250	mA
I_{CC}	Supply Current	V_{CC} = MAX, Outputs Open	Outputs Enabled			145	mA
			Outputs Disabled			155	

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2982_DC	D-24-SLIM	C	C-1
AM2982_DCB	D-24-SLIM	C	B-2 (Note 4)
AM2982_DM	D-24-SLIM	M	C-3
AM2982_DMB	D-24-SLIM	M	B-3
AM2982_LC	L-28-1	C	C-1
AM2982_LCB	L-28-1	C	B-2 (Note 4)
AM2982_LM	L-28-1	M	C-3
AM2982_LMB	L-28-1	M	B-3
AM2982_XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2982_XM	Dice	M	

Notes: 1. D = Hermetic DIP, L = Chip-Pak. Number following letter is number of leads.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 160 hour burn-in.

Am29827/Am29828 SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameter	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Data (D_i) to Output (Y_i) Am29827 (Noninverting)	C_L = 50pF		4.5	5.5	ns
t_{PHL}				4.5	5.5	ns
t_{PLH}		C_L = 300pF			11	ns
t_{PHL}					11	ns
t_{PLH}	Data (D_i) to Output (Y_i) Am29828 (Inverting)	C_L = 50pF		4.0	5	ns
t_{PHL}				4.0	5	ns
t_{PLH}		C_L = 300pF			10	ns
t_{PHL}					10	ns
t_{ZH}	Output Enable Time $\overline{OE}$ to Y_i	C_L = 50pF		6.5		ns
t_{ZL}				9.5		ns
t_{ZH}		C_L = 300pF				ns
t_{ZL}						ns
t_{HZ}	Output Disable Time $\overline{OE}$ to Y_i	C_L = 5pF				ns
t_{LZ}						ns
t_{HZ}		C_L = 50pF		11.2		ns
t_{LZ}				4.2		ns

Am29827/Am29828 SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			COM'L		MIL		
			T_A = 0 to +70°C V_{CC} = 5.0V ± 10%		T_C = −55 to +125°C V_{CC} = 5.0V ± 10%		
Parameters	Description	Test Conditions	Min	Max	Min	Max	Units
t_{PLH}	Data (D_i) to Output (Y_i) Am29827 (Noninverting)	C_L = 50pF		10		12	ns
t_{PHL}				10		12	ns
t_{PLH}		C_L = 300pF		15		17	ns
t_{PHL}				15		17	ns
t_{PLH}	Data (D_i) to Output (Y_i) Am29828 (Inverting)	C_L = 50pF		9		11	ns
t_{PHL}				9		11	ns
t_{PLH}		C_L = 300pF		14		16	ns
t_{PHL}				14		16	ns
t_{ZH}	Output Enable Time $\overline{OE}$ to Y_i	C_L = 50pF		15		17	ns
t_{ZL}				15		17	ns
t_{ZH}		C_L = 300pF		18.5		20.5	ns
t_{ZL}				18.5		20.5	ns
t_{HZ}	Output Disable Time $\overline{OE}$ to Y_i	C_L = 5pF		10		12	ns
t_{LZ}				10		12	ns
t_{HZ}		C_L = 50pF		13.5		20	ns
t_{LZ}				13.5		20	ns

DEFINITION OF FUNCTIONAL TERMS

$\overline{OE}_i$ When both are LOW the outputs are enabled. When either one or both are HIGH the outputs are HI-Z.

D_i 10-bit data input.

Y_i 10-bit data output.

FUNCTION TABLES

Am29827 (Noninverting)

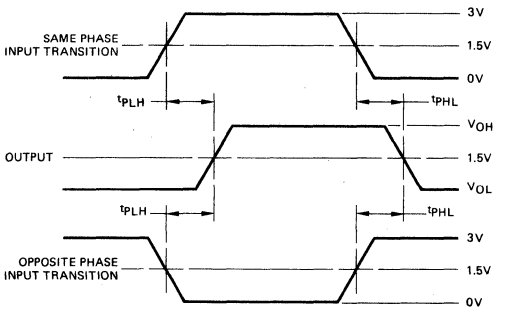
Inputs		Outputs	
$\overline{OE}$	D_i	Y_i	Function
L	H	H	Transparent
L	L	L	Transparent
H	X	Z	HI-Z

Am29828 (Inverting)

Inputs		Outputs	
$\overline{OE}$	D_i	$\overline{Y}_i$	Function
L	H	L	Transparent
L	L	H	Transparent
H	X	Z	HI-Z

SWITCHING TIME WAVEFORMS AND AC TEST CIRCUITS

PROPAGATION DELAY



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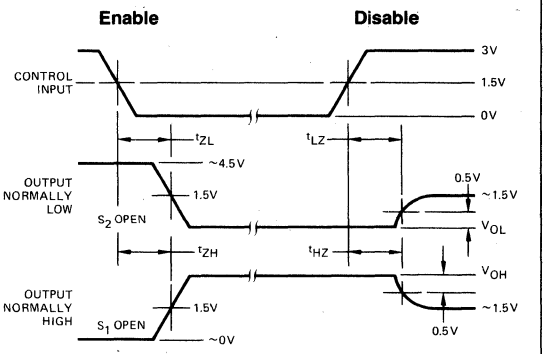
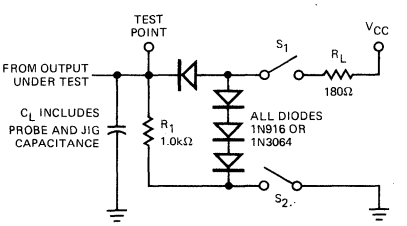
ENABLE AND DISABLE TIMES



Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1 and S_2 of Load Circuit are closed except where shown.

ABI-129

LOAD TEST CIRCUIT



Note: Pulse Generator for All Pulses: Rate ≤ 10MHz; $Z_o = 50\Omega$; $t_r \leq 2.5$ns; $t_f \leq 2.5$ns.

ABI-130

Am29833/34 • Am29853/54

Parity Bus Transceivers

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

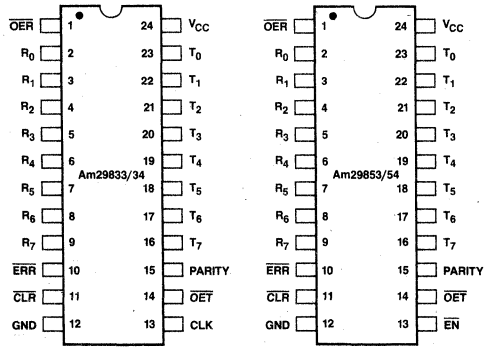
- High-speed bidirectional bus transceiver for processor organized devices
- Error flag with open-collector output
- Generates odd parity for all-zero protection
- Buffered direction three-state control
- Separate Transmit and Receive enable controls
- Output short-circuit protected to V_{CC} limits
- 200mV minimum input hysteresis on input data ports
- High-capacitance drive capability
  - 48mA commercial I_{OL}
  - 32mA military I_{OL}
- 24-pin 0.3″ slim DIP package
- 100% product assurance screening to MIL-STD-883 requirements

CONNECTION DIAGRAMS – Top Views

Leadless Chip Carrier
L-28-1

ABI-105

8-BIT TO 9-BIT PARITY TRANSCEIVERS



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FUNCTIONAL DESCRIPTION

The Am29833/34/53/54 are high-performance bus transceivers designed for two-way communications. They each contain an 8-bit data path from the A (port) to the B (port), a 9-bit data path from the B (port) to the A (port), and a 9-bit parity checker/generator. Two options are available. The Am29833/34 register option, and the Am29853/54 latch option. With the register option, the error flag can be clocked and stored in a register and read at the open-collector $\overline{ERR}$ output. The clear ($\overline{CLR}$) input is used to clear the error flag register. With the latch option, the error can be either passed, stored, sampled or cleared at the error flag output by using the $\overline{EN}$ and $\overline{CLR}$ controls.

The output enables $\overline{OET}$ and $\overline{OER}$ are used to force the port outputs to the high-impedance state so that the device can drive bus lines directly. In addition, the $\overline{OER}$ and $\overline{OET}$ can be used to force a parity error by enabling both lines simultaneously. This transmission of inverted parity gives the designer more system diagnostic capability. The Am29833 and Am29853 are noninverting, while the Am29834 and Am29854 present inverting data at the outputs. The devices are specified at 48mA output sink current over the commercial range and 32mA over the military range.

ORDERING INFORMATION

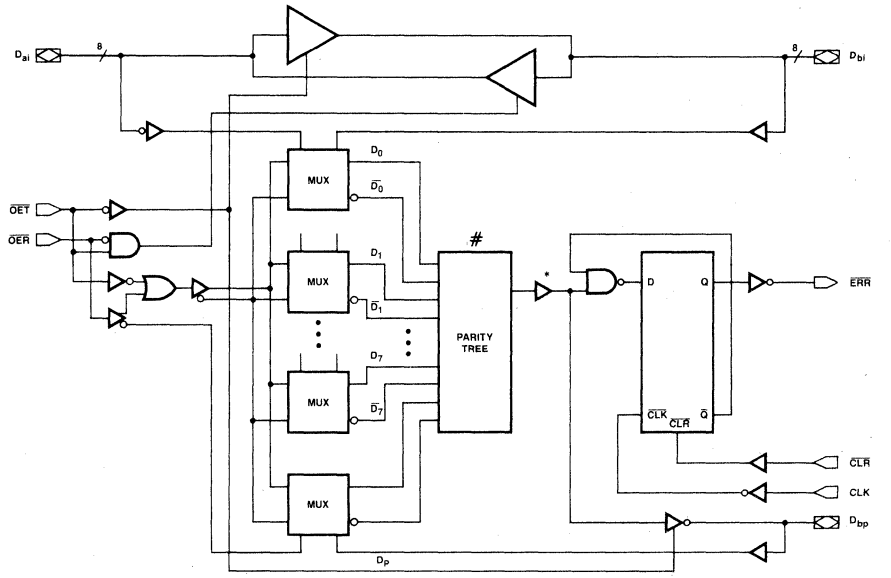
Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2983_/5_DC	D-24-SLIM	C	C-1
AM2983_/5_DCB	D-24-SLIM	C	B-2 (Note 4)
AM2983_/5_DM	D-24-SLIM	M	C-3
AM2983_/5_DMB	D-24-SLIM	M	B-3
AM2983_/5_LC	L-28-1	C	C-1
AM2983_/5_LCB	L-28-1	C	B-2 (Note 4)
AM2983_/5_LM	L-28-1	M	C-3
AM2983_/5_LMB	L-28-1	M	B-3
AM2983_/5_XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2983_/5_XM	Dice	M	

Notes: 1. D = Hermetic DIP, L = Chip-Pak. Number following letter is number of leads.
2. C = 0 to +70°C, V_{CC} = 4.75 to 5.25V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 160 hour burn-in.

TABLE OF CONTENTS

Am29833
FUNCTION BLOCK DIAGRAM
(Device Shown Noninverting)



*Am29833 shown; for Am29834, buffer replaced with inverter.

$\# = D_0 \oplus D_1 \oplus D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_p$

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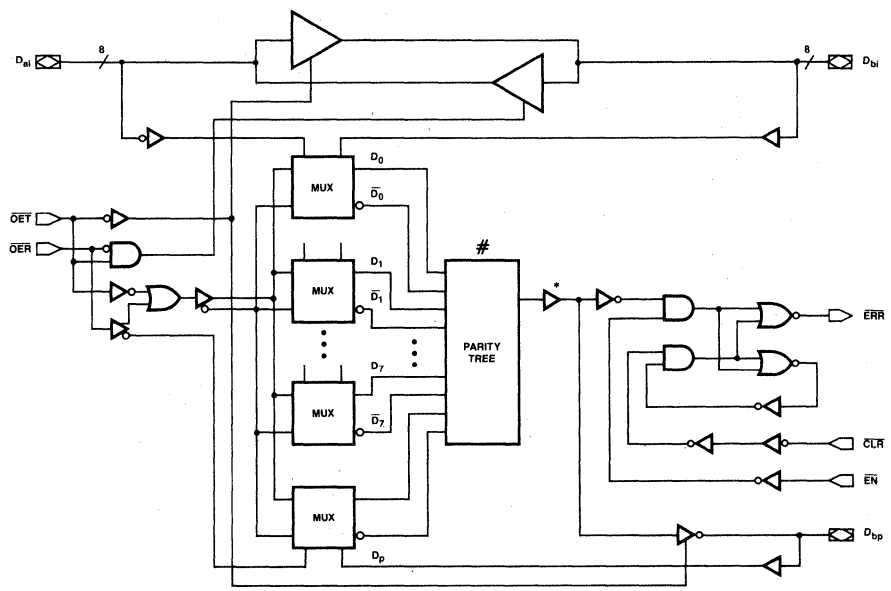
Am29853
FUNCTION BLOCK DIAGRAM
(Device Shown Noninverting)



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*Am29853 shown; for Am29854, buffer replaced with inverter.

$\# = D_0 \oplus D_1 \oplus D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_p$

*Note that the inverting device converts the positive logic "A" bus levels to negative logic levels on the "B" bus.

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MAXIMUM RATINGS

Supply Voltage	7.0V
Common Mode Range	0 to V_{CC}
Logic Inputs	5.5V
Storage Temperature Range	−65 to +150°C

OPERATING RANGE

Part No.	Temperature	V_{CC}
Am2983X/5XDC	T_A = 0 to +70°C	5.0 ±10%
Am2983X/5XDM	T_C = −55 to +125°C	5.0 ±10%

ELECTRICAL CHARACTERISTICS

COM'L T_A = 0 to +70°C V_{CC} = 5.0V ±10% (Min = 4.5V Max = 5.5V)
MIL T_C = −55 to +125°C V_{CC} = 5.0V ±10% (Min = 4.5V Max = 5.5V)

Parameters	Description	Test Conditions			Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage (Except $\overline{ERR}$)	V_{CC} = Min		I_{OH} = −15mA	2.4			V
				I_{OH} = −24mA	2.0			
V_{OL}	Output LOW Voltage	V_{CC} = Min	$\overline{ERR}$	I_{OL} = 48mA			0.5	V
			All Other Outputs	I_{OL} = 32mA MIL			0.5	
				I_{OL} = 48mA COM'L			0.5	
V_{IH}	Input HIGH Voltage				2.0			V
V_{IL}	Input LOW Voltage						0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max, V_{IN} = 0.4V		Data			−1.0	mA
				Control			−2.0	
I_{IH}	Input HIGH Current	V_{CC} = Max		Control V_{IN} = 2.7V			50	µA
				Data V_{IN} = 2.4V			50	
I_{SC}	Output Short Circuit Current				−75		−250	mA
I_I	Input Leakage Current	V_{CC} = Max, V_{IN} = 5.5V					1.0	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18mA					−1.2	V
I_{OZH}	Output Leakage Current (High Impedance)	V_{CC} = Max		V_O = 2.4V			50	µA
I_{OZL}				V_O = 0.4V			−1.0	mA
I_{CC}	Power Supply Current	V_{CC} = Max (All Outputs Are Passive)						mA
V_{HYST}	Hysteresis for Inputs D_{ai}, D_{bi}				200			mV

DEFINITION OF FUNCTIONAL TERMS
Am29833/34

$\overline{OER}$	RECEIVE enable input.
R_i	8-bit RECEIVE data input.
$\overline{ERR}$	Output from fault registers. Registers detection of odd parity fault on using clock edge (CLK). A registered $\overline{ERR}$ output remains LOW until cleared.
$\overline{CLR}$	Clears the fault register output.
T_i	8-bit TRANSMIT data input.
PARITY	1-bit PARITY output.
$\overline{OET}$	TRANSMIT enable input.
CLK	External clock pulse input for fault register flag.

DEFINITION OF FUNCTIONAL TERMS
Am29853/54

$\overline{OER}$	RECEIVE enable input.
R_i	8-bit RECEIVE data input.
$\overline{ERR}$	Output from fault latches. Latches detection of odd parity fault on active enable $\overline{EN}$. A latched $\overline{ERR}$ output remains LOW until cleared.
$\overline{CLR}$	Clears the fault latch output.
T_i	8-bit TRANSMIT data output.
PARITY	1-bit PARITY output.
$\overline{OET}$	TRANSMIT enable input.
$\overline{EN}$	Enable latch input for fault flag.

Am29833/34/53/54
SWITCHING CHARACTERISTICS

COM'L $T_A = 0$ to $+70°C$ $V_{CC} = 5.0V \pm 10\%$

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay D_{ai} to D_{bi}, D_{bi} to D_{ai}	$C_L = 50pF$			12	ns
t_{PHL}					12	ns
t_{PLH}		$C_L = 300pF$			16	ns
t_{PHL}					16	ns
t_{PLH}	Propagation Delay D_{ai} to D_{bp}	$C_L = 50pF$			15	ns
t_{PHL}					15	ns
t_{PLH}		$C_L = 300pF$			22	ns
t_{PHL}					22	ns
t_{ZH}	Output Enable Time $\overline{OER}$, $\overline{OET}$ to D_{ai}, D_{bi}	$C_L = 50pF$			15	ns
t_{ZL}					15	ns
t_{ZH}		$C_L = 300pF$			22	ns
t_{ZL}					22	ns
t_{HZ}	Output Disable Time $\overline{OER}$, $\overline{OET}$ to D_{ai}, D_{bi}	$C_L = 5pF$			10	ns
t_{LZ}					10	ns
t_{HZ}		$C_L = 50pF$			17	ns
t_{LZ}					17	ns
t_S	D_{bi}, D_{bp} to CLK Setup Time	$C_L = 50pF$	15			ns
t_H	D_{bi}, D_{bp} to CLK Hold Time		0			ns
t_S	Clear Recovery Time $\overline{CLR}$ to CLK		15			ns
t_{PWH}	Clock Pulse Width HIGH		10			ns
t_{PWL}	Clock Pulse Width LOW		10			ns
t_{PWL}	Clear Pulse Width LOW		10			ns
t_{PHL}	Propagation Delay CLK to $\overline{ERR}$	$C_L = 50pF$			15	ns
t_{PLH}	Propagation Delay $\overline{CLR}$ to $\overline{ERR}$ (Am29833/34)	$C_L = 50pF$			15	ns
t_{PLH}	Propagation Delay $\overline{CLR}$ to $\overline{ERR}$ (Am29853/54)	$C_L = 50pF$			15	ns
t_{PLH}	Propagation Delay D_{bi}, D_{bp} to $\overline{ERR}$ (PASS Mode Only) Am29853/54	$C_L = 50pF$			22	ns
t_{PHL}					18	ns
t_{PLH}	Propagation Delay $\overline{OER}$ to D_{bp}	$C_L = 50pF$ Test Ckt #1			15	ns
t_{PHL}					15	ns
t_{PLH}		$C_L = 300pF$ Test Ckt #1			22	ns
t_{PHL}					22	ns

Note: For Am29853/54 replace CLK with $\overline{EN}$.

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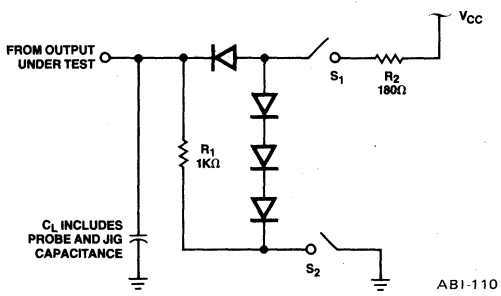
TEST LOAD CIRCUITS

CIRCUIT NO. 1



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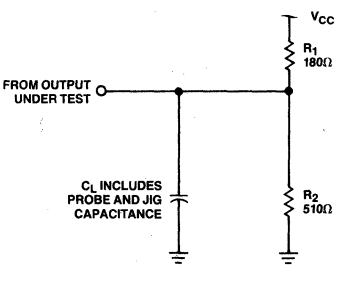
CIRCUIT NO. 2



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Note: Test Circuit No. 1 is used with Propagation delay on the Data Lines, $\overline{OER}$ and $\overline{OET}$ tests. Test Circuit No. 2 is used with all parameters involving CLK, $\overline{CLR}$, $\overline{EN}$ and $\overline{ERR}$.

ERROR FLAG OUTPUT TRUTH TABLE

Am29833/Am29834 (REGISTER OPTION)

Inputs		Internal to Device	Output's Pre-State	Output	
CLR	CLK	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	Function
H	↑	H	H	H	Sample* (1's Capture)
H	↑	–	L	L	
H	↑	L	–	L	
L	–	–	–	H	Clear

Am29853/Am29854 (LATCH OPTION)

Inputs		Internal to Device	Output's Pre-State	Output	
$\overline{EN}$	$\overline{CLR}$	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	Function
L	L	L	–	L	Pass
L	L	H	–	H	
L	H	L	–	L	Sample* (1's Capture)
L	H	–	L	L	
L	H	H	H	H	
H	L	–	–	H	Clear
H	H	–	L	L	Store*
H	H	–	H	H	

*Enable is used as strobe for the latch in sampled operation.

FUNCTION TABLES

Am29833 NONINVERTING OPTION

Inputs						Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	CLK	D_{ai} (Σ of H's)	D_{bi} Incl D_{bp} (Σ of H's)	D_{ai}	D_{bi}	D_{bp}	$\overline{ERR}$	Function
L	H	–	–	H (Odd)	NA	NA	H	L	NA	Transmit data from A Port to B Port with parity, receiving path is disabled
L	H	–	–	H (Even)	NA	NA	H	H	NA	
L	H	–	–	L (Odd)	NA	NA	L	L	NA	
L	H	–	–	L (Even)	NA	NA	L	H	NA	
H	L	H	↑	NA	H (Odd)	H	NA	NA	H	Receive data from B Port to A Port with parity test resulting in flag, transmitting path is disabled
H	L	H	↑	NA	H (Even)	H	NA	NA	L	
H	L	H	↑	NA	L (Odd)	L	NA	NA	H	
H	L	H	↑	NA	L (Even)	L	NA	NA	L	
–	–	L	–	–	–	–	NA	NA	H	Clear the state of error flag register
H	H	–	–	–	–	Z	Z	Z	–	Both transmitting and receiving paths are disabled
L	L	–	–	H (Odd)	NA	NA	H	H	NA	Forced-error checking
L	L	–	–	H (Even)	NA	NA	H	L	NA	
L	L	–	–	L (Odd)	NA	NA	L	H	NA	
L	L	–	–	L (Even)	NA	NA	L	L	NA	

Am29834 INVERTING OPTION*

Inputs						Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	CLK	D_{ai} (Σ of H's)	D_{bi} Incl D_{bp} (Σ of L's)	D_{ai}	D_{bi}	D_{bp}	$\overline{ERR}$	Function
L	H	–	–	H (Odd)	NA	NA	L	H	NA	Transmit data from A Port to B Port with parity, receiving path is disabled
L	H	–	–	H (Even)	NA	NA	L	L	NA	
L	H	–	–	L (Odd)	NA	NA	H	H	NA	
L	H	–	–	L (Even)	NA	NA	H	L	NA	
H	L	H	↑	NA	H (Odd)	L	NA	NA	H	Receive data from B Port to A Port with parity test resulting in flag, transmitting path is disabled
H	L	H	↑	NA	H (Even)	L	NA	NA	L	
H	L	H	↑	NA	L (Odd)	H	NA	NA	H	
H	L	H	↑	NA	L (Even)	H	NA	NA	L	
–	–	L	–	–	–	–	–	–	H	Clear the state of error flag register
H	H	–	–	–	–	Z	Z	Z	–	Both transmitting and receiving paths are disabled
L	L	–	–	H (Odd)	NA	NA	L	L	NA	Forced-error checking
L	L	–	–	H (Even)	NA	NA	L	H	NA	
L	L	–	–	L (Odd)	NA	NA	H	L	NA	
L	L	–	–	L (Even)	NA	NA	H	H	NA	

H = High
L = Low
↑ = Low to high transition of clock
Z = High impedance
NA = Not applicable
– = Don't care or irrelevant
Odd = Odd number of logic one's
Even = Even number of logic one's
i = 0, 1, 2, 3, 4, 5, 6, 7

*Note that for the negative logic levels on the B Port, an "H" represents a logic "0" while an "L" represents a logic "1."

FUNCTION TABLES (Cont.)

Am29853 NONINVERTING OPTION

Inputs						Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	$\overline{EN}$	D_{ai} (Σ of H's)	D_{bi} Incl D_{bp} (Σ of H's)	D_{ai}	D_{bi}	D_{bp}	$\overline{ERR}$	Function
L	H	–	–	H (Odd)	NA	NA	H	L	NA	Transmit data from A Port to B Port with parity, receiving path is disabled
L	H	–	–	H (Even)	NA	NA	H	H	NA	
L	H	–	–	L (Odd)	NA	NA	L	L	NA	
L	H	–	–	L (Even)	NA	NA	L	H	NA	
H	L	L	L	NA	H (Odd)	H	NA	NA	H	Receive data from B Port to A Port with parity test resulting in flag, transmitting path is disabled
H	L	L	L	NA	H (Even)	H	NA	NA	L	
H	L	L	L	NA	L (Odd)	L	NA	NA	H	
H	L	L	L	NA	L (Even)	L	NA	NA	L	
H	L	H	L	NA	H (Odd)	H	NA	NA	H	Receive data from B Port to A Port, pass the error test resulting to error flag, transmitting path is disabled
H	L	H	L	NA	H (Even)	H	NA	NA	L	
H	L	H	L	NA	L (Odd)	L	NA	NA	H	
H	L	H	L	NA	L (Even)	L	NA	NA	L	
H	L	H	H	NA	–	–	NA	NA	$\overline{ERR}_{n-1}$	Store the state of error flag register
–	–	L	H	–	–	–	NA	NA	H	Clear the state of error flag register
H	H	–	–	–	–	Z	Z	Z	–	Both transmitting and receiving paths are disabled
L	L	–	–	H (Odd)	NA	NA	H	H	NA	Forced-error checking
L	L	–	–	H (Even)	NA	NA	H	L	NA	
L	L	–	–	L (Odd)	NA	NA	L	H	NA	
L	L	–	–	L (Even)	NA	NA	L	L	NA	

Am29854 INVERTING OPTION*

Inputs						Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	$\overline{EN}$	D_{ai} (Σ of H's)	D_{bi} Incl D_{bp} (Σ of L's)	D_{ai}	D_{bi}	D_{bp}	$\overline{ERR}$	Function
L	H	–	–	H (Odd)	NA	NA	L	H	NA	Transmit data from A Port to B Port with parity, receiving path is disabled
L	H	–	–	H (Even)	NA	NA	L	L	NA	
L	H	–	–	L (Odd)	NA	NA	H	H	NA	
L	H	–	–	L (Even)	NA	NA	H	L	NA	
H	L	L	L	NA	H (Odd)	L	NA	NA	H	Receive data from B Port to A Port with parity test resulting in flag, transmitting path is disabled
H	L	L	L	NA	H (Even)	L	NA	NA	L	
H	L	L	L	NA	L (Odd)	H	NA	NA	H	
H	L	L	L	NA	L (Even)	H	NA	NA	L	
H	L	H	L	NA	H (Odd)	L	NA	NA	H	Receive data from B Port to A Port, pass the error test resulting to error flag, transmitting path is disabled
H	L	H	L	NA	H (Even)	L	NA	NA	L	
H	L	H	L	NA	L (Odd)	H	NA	NA	H	
H	L	H	L	NA	L (Even)	H	NA	NA	L	
H	L	H	H	NA	–	–	NA	NA	$\overline{ERR}_{n-1}$	Store the state of error flag register
–	–	L	H	–	–	–	NA	NA	H	Clear the state of error flag register
H	H	–	–	–	–	Z	Z	Z	–	Both transmitting and receiving paths are disabled
L	L	–	–	H (Odd)	NA	NA	L	L	NA	Forced-error checking
L	L	–	–	H (Even)	NA	NA	L	H	NA	
L	L	–	–	L (Odd)	NA	NA	H	L	NA	
L	L	–	–	L (Even)	NA	NA	H	H	NA	

H = High
L = Low
Z = High impedance

NA = Not applicable
$\overline{ERR}_{n-1}$ = Pre-state of $\overline{ERR}$
– = Don't care or irrelevant

Odd = Odd number of logic one's
Even = Even number of logic one's
i = 0, 1, 2, 3, 4, 5, 6, 7

*Note that for the negative logic levels on the B port, an "H" represents a logic "0" while an "L" represents a logic "1."

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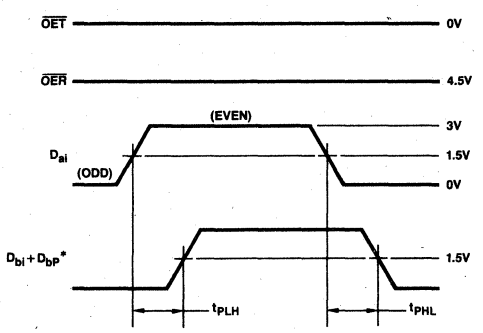
Am29833/53 SWITCHING WAVEFORMS (NONINVERTING OPTION)



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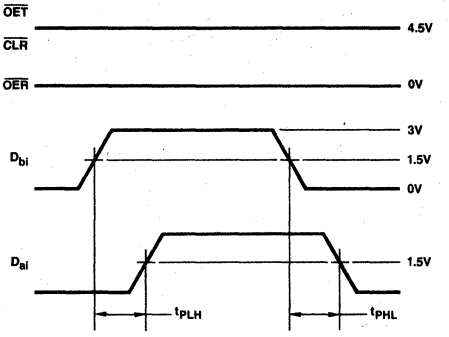
a) D_{ai} to D_{bi}, D_{bp}



b) D_{bi} to D_{ai}

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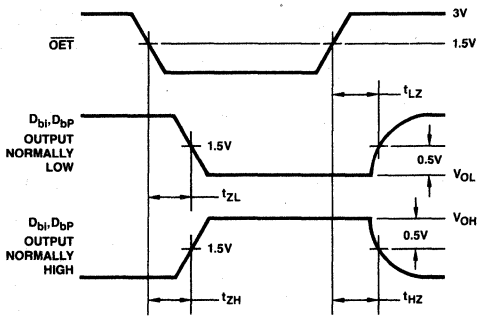

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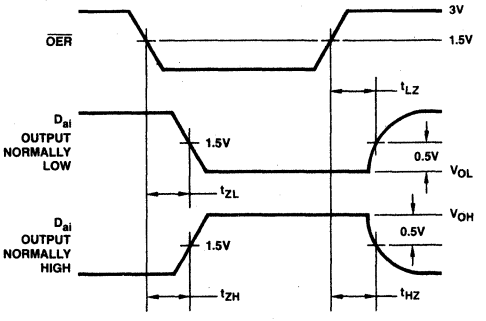
c) $\overline{OET}$ to D_{bi}, D_{bp}



d) $\overline{OER}$ to D_{ai}

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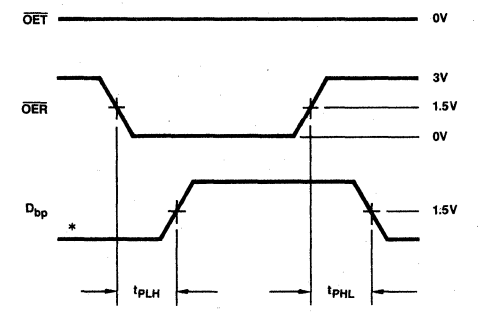

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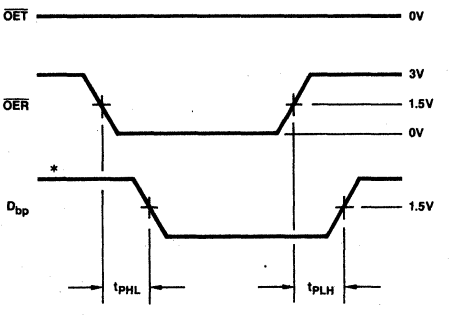
*Σ of H's of D_{ai} = ODD



*Σ of H's of D_{ai} = EVEN

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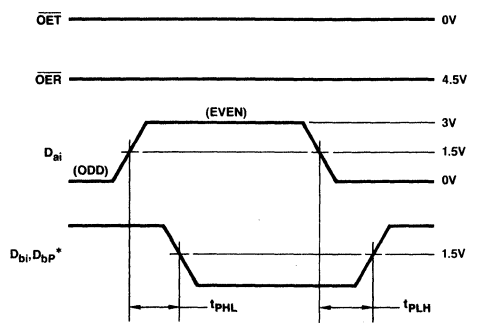
*Calculation must be done from last arriving signal.

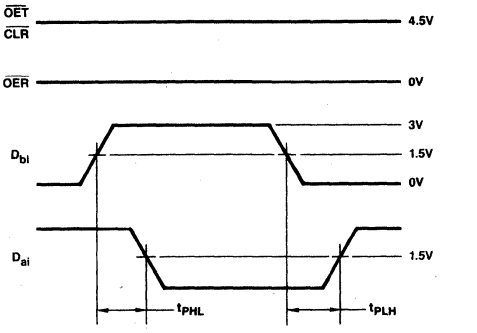
e) $\overline{OER}$ to D_{bp}

Am29834/54 SWITCHING WAVEFORMS (INVERTING OPTION)



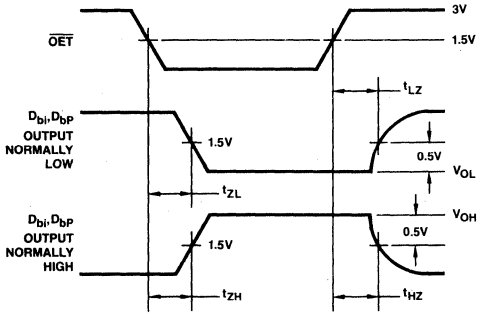
ABI-118

a) D_{ai} to D_{bi}, D_{bp}



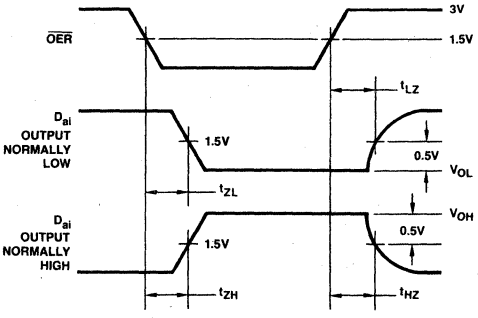
b) D_{bi} to D_{ai}

ABI-119



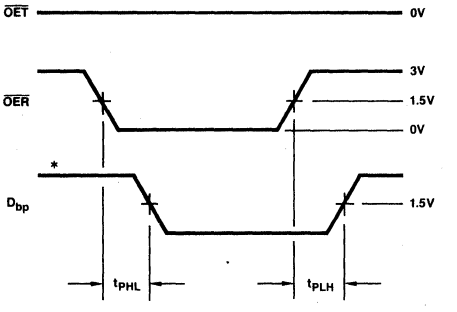
ABI-120

c) $\overline{OET}$ to D_{bi}, D_{bp}



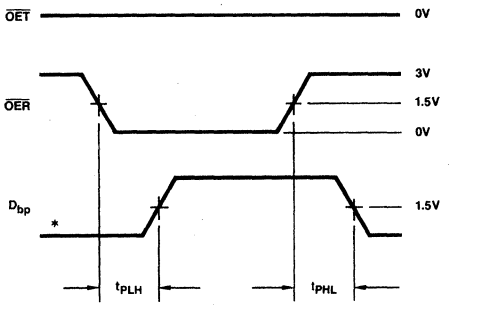
d) $\overline{OER}$ to D_{ai}

ABI-121



ABI-122

*Σ of H's of D_{ai} = ODD



*Σ of H's of D_{ai} = EVEN

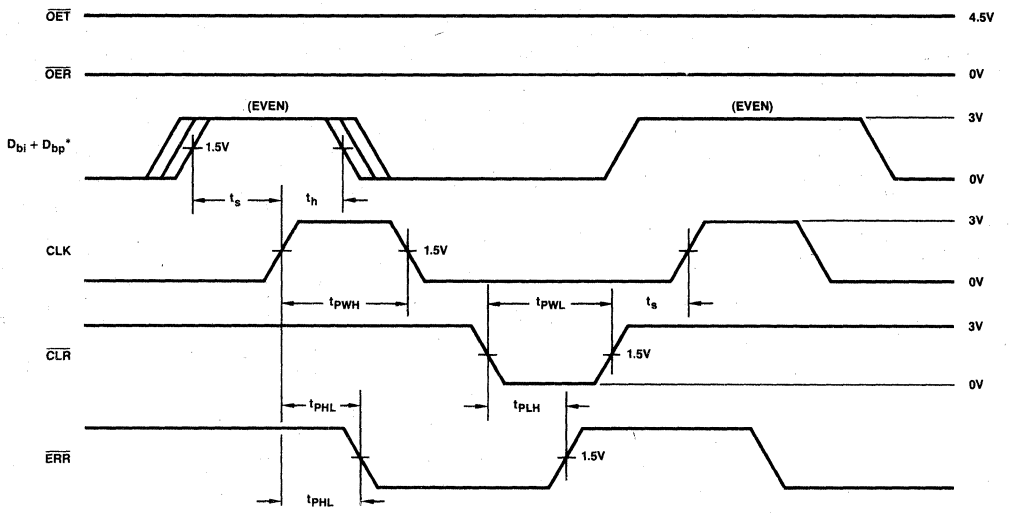
ABI-123

*Calculation must be done from last arriving signal.

e) $\overline{OER}$ to D_{bp}

8

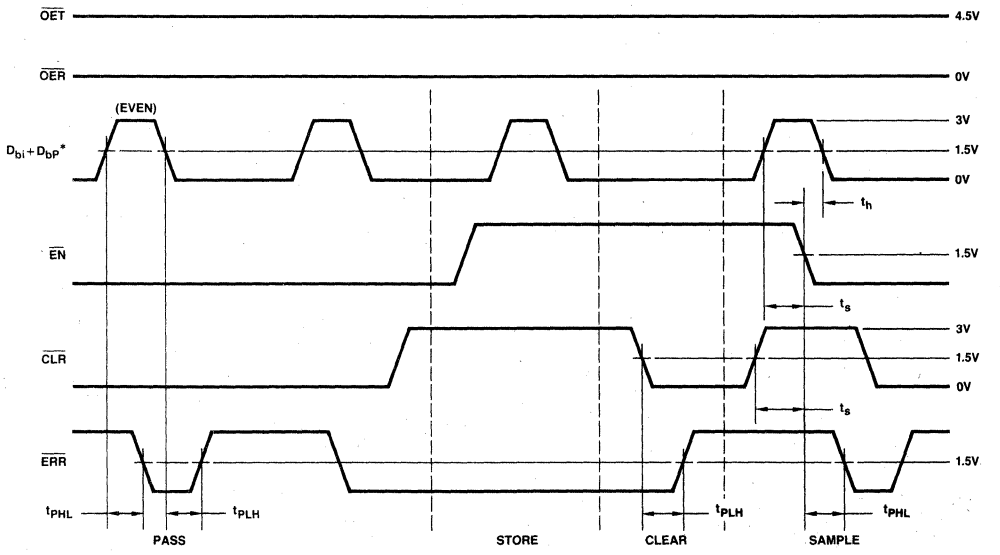
SWITCHING WAVEFORMS (REGISTER OPTION, Am29833/34)



a) CLK, $\overline{CLR}$ to $\overline{ERR}$

ABI-124

SWITCHING WAVEFORMS (LATCH OPTION, Am29853/54)



b) D_{bi}, D_{bp}, $\overline{EN}$, $\overline{CLR}$ to $\overline{ERR}$

ABI-125

*Calculation must be done from last arriving signal.

Am29841/842 • Am29843/844 • Am29845/846

High Performance Bus Interface Latches

DISTINCTIVE CHARACTERISTICS

- High-speed parallel latches
  - Noninverting transparent t_{PD} = 5.25ns typ
  - Inverting transparent t_{PD} = 6.0ns typ
- Buffered common latch enable, clear and preset input
- Three-state outputs glitch-free during power-up and down
- Outputs have Schottky clamp to ground
- 48mA Commercial I_{OL}, 32mA MIL I_{OL}
- Low input/output capacitance
  - 6pF inputs (typical)
  - 8pF outputs (typical)
- I_{OH} specified 2.0V and 2.4V
- 24-pin 0.3" space saving package
- Fully TTL compatible inputs and outputs
- IMOX™ high performance IMplanted OXide isolated process

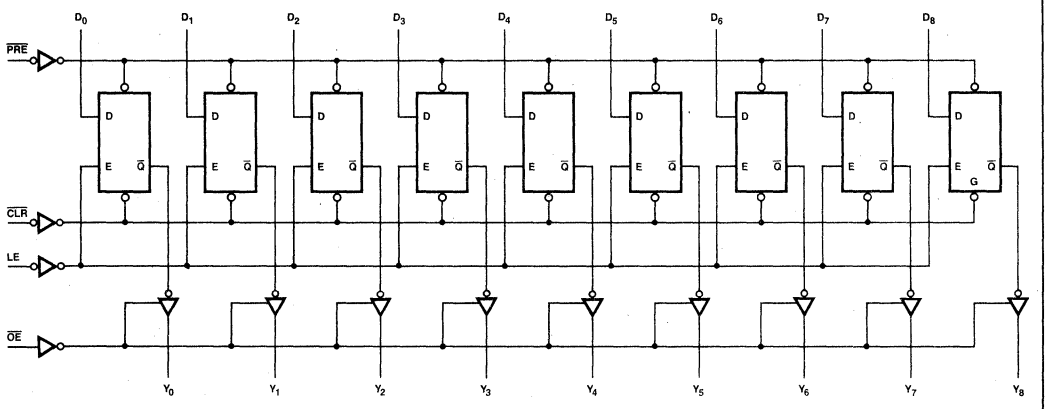
FUNCTIONAL DESCRIPTION

The Am29840 Series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The Am29841 and Am29842 are buffered, 10-bit wide versions of the popular '373 function. The Am29843 and Am29844 are 9-bit wide buffered latches with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high performance systems. The Am29845 and Am29846 are 8-bit buffered latches with all the '843/4 controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the Am29800 high performance interface family are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

	Device		
	10-Bit	**9-Bit**	**8-Bit**
Noninverting	Am29841	Am29843	Am29845
Inverting	Am29842	Am29844	Am29846

LOGIC DIAGRAM
Am29843



ABI-010

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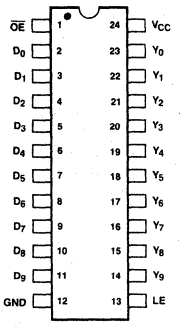
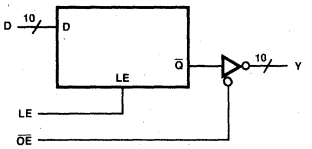
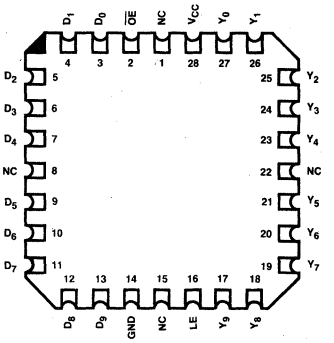
8

CONNECTION DIAGRAMS

Am29841/Am29842
10-BIT LATCHES
Top Views

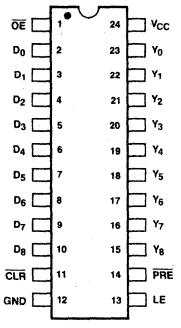


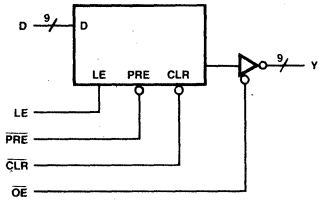


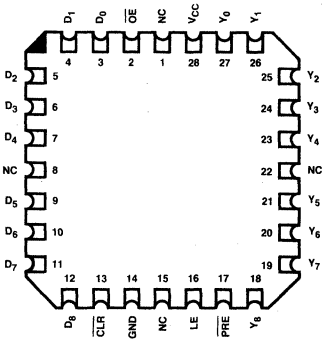


ABI-011

Am29843/Am29844
9-BIT LATCHES
Top Views

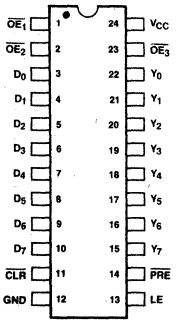


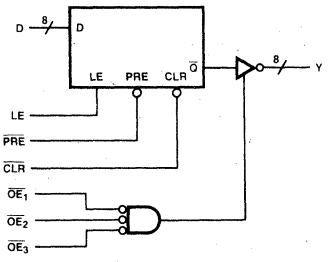


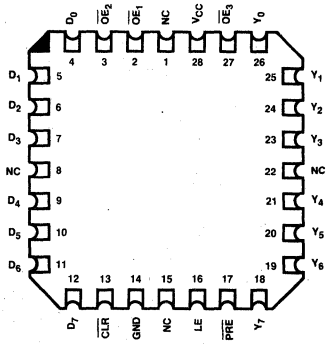


ABI-012

Am29845/Am29846
8-BIT LATCHES
Top Views







ABI-013

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5 to +V_{CC} max
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	100mA
DC Input Current	−30 to +5.0mA

ELECTRICAL CHARACTERISTICS The following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0 to +70°C V_{CC} = 5.0V ±10% MIN = 4.50V MAX = 5.50V

MIL T_C = −55 to +125°C V_{CC} = 5.0V ±10% MIN = 4.50V MAX = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions[1]			Min	Typ[2]	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15mA		2.4	3.3		Volts
			I_{OH} = −24mA		2.0	3.1		
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OL} = 32mA				0.5	Volts
			COM'L, I_{OL} = 48mA				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA					−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V					−1.0	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V					50	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_{OZ}	Output Off-state (High Impedance) Output Current	V_{CC} = MAX	V_O = 0.4V				−50	μA
			V_O = 2.4V				50	
I_{SC}	Output Short Circuit Current[3]	V_{CC} = MAX			−75		−250	mA
I_{CC}	Supply Current	V_{CC} = MAX, Outputs Open	Outputs Enabled ($\overline{OE}$ = LOW)	0 to +70°C		60	120	mA
				+70°C		60	120	mA
				−55 to +125°C		60	120	mA
				+125°C		60	120	mA
			Outputs Disabled ($\overline{OE}$ = HIGH)	0 to +70°C		70	120	mA
				+70°C		70	100	mA
				−55 to +125°C		70	120	mA
				+125°C		70	100	mA

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
2. All typical values are V_{CC} = 5.0V, T_A = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

8

Am29841/42/43/44/45/46
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description		Test Conditions (Note 4)	Commercial T_A = 0 to +70°C, V_{CC} = 5.0V ±10% Min	Commercial Max	Military T_C = −55 to +125°C, V_{CC} = 5.0V ±10% Min	Military Max	Units
t_{PLH} (Am29841, 3, 5)	Data (D_i) to Output Y_i (LE = HIGH)		C_L = 50pF	3.5	9.5	3.5	11	ns
t_{PHL}				3.5	9.5	3.5	11	ns
t_{PLH}			C_L = 300pF		12.5		14	ns
t_{PHL}					13		15	ns
t_S	Data to LE Setup Time		C_L = 50pF	2.5		2.5		ns
t_H	Data to LE Hold Time			2.5		3		ns
t_{PLH} (Am29842, 4, 6)	Data (D_i) to Output ($\overline{Y_i}$) (LE = HIGH)		C_L = 50pF	3.5	10		12	ns
t_{PHL}				3.5	10		12	ns
t_{PLH}			C_L = 300pF		12.5		14	ns
t_{PHL}					13		15	ns
t_{PLH}	Data to LE Setup Time		C_L = 50pF	2.5		2.5		ns
t_{PHL}	Data to LE Hold Time			2.5		3		ns
t_{PLH}	Latch Enable (LE) to Y_i		C_L = 50pF		12		16	ns
t_{PHL}					12		16	ns
t_{PLH}			C_L = 300pF		16		20	ns
t_{PHL}					16		20	ns
								ns
								ns
t_{PLH}	Propagation Delay, Preset to Y_i		C_L = 50pF		12		14	ns
t_S	Preset Recovery ($\overline{PRE}$ ↓) Time				14		17	ns
t_{PHL}	Propagation Delay, Clear to Y_i				21		23	ns
t_S	Clear Recovery ($\overline{CLR}$ ↓) Time				14		17	ns
t_{PWH}	LE Pulse Width	HIGH	C_L = 50pF	6		6		ns
t_{PWL}	Preset Pulse Width	LOW		8		9		ns
t_{PWL}	Clear Pulse Width	LOW		8		9		ns
t_{ZH}	Output Enable Time $\overline{OE}$ ↑ to Y_i		C_L = 300pF		20		22	ns
t_{ZL}					20		22	ns
t_{ZH}			C_L = 50pF		14		15	ns
t_{ZL}					14		15	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ↓ to Y_i		C_L = 50pF		15		15	ns
t_{LZ}					12		12	ns
t_{HZ}			C_L = 5pF		9		10	ns
t_{LZ}					9		10	ns

Note: 4. See test circuit and waveforms.

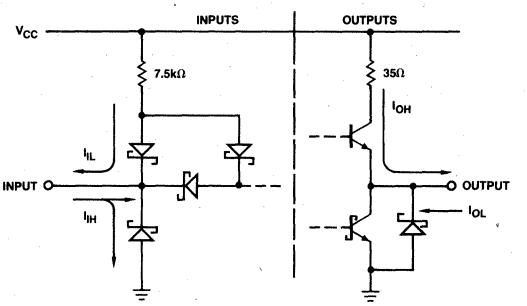
SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Test Conditions (Note 4)	Min	Typ	Max	Units
t_{PLH} (Am29841, 3, 5)	Data (D_i) to Output Y_i (LE = HIGH)		C_L = 50pF	3.5	5.7	8	ns
t_{PHL}				3.5	6.2	8	ns
t_{PLH}			C_L = 300pF		10	13	ns
t_{PHL}					10	13	ns
t_S	Data to LE Setup Time		C_L = 50pF	2.0	−0.2		ns
t_H	Data to LE Hold Time			2.5	0.7		ns
t_{PLH} (Am29842, 4, 6)	Data (D_i) to Output ($\overline{Y_i}$) (LE = HIGH)		C_L = 50pF	3.5	6.2	8.5	ns
t_{PHL}				3.5	6.5	8.5	ns
t_{PLH}			C_L = 300pF		10	13	ns
t_{PHL}					10	13	ns
t_S	Data to LE Setup Time		C_L = 50pF	2.5	0.3		ns
t_H	Data to LE Hold Time			2.5	0.2		ns
t_{PLH}	Latch Enable (LE) to Y_i		C_L = 50pF		8	10.5	ns
t_{PHL}					7.5	10	ns
t_{PLH}			C_L = 300pF			15	ns
t_{PHL}						15	ns
			C_L = 50pF				ns
							ns
t_{PLH}	Propagation Delay, Preset to Y_i				6.5	9	ns
t_S	Preset Recovery (PRE ↓) Time				7.3	12	ns
t_{PHL}	Propagation Delay, Clear to Y_i				15	18	ns
t_S	Clear Recovery ($\overline{CLR}$ ↓) Time				7.8	12	ns
t_{PWH}	LE Pulse Width	HIGH	C_L = 50pF	4	2.5		ns
t_{PWL}	Preset Pulse Width	LOW		5			ns
t_{PWL}	Clear Pulse Width	LOW		6			ns
t_{ZH}	Output Enable Time $\overline{OE}$ ↑ to Y_i		C_L = 300pF			17	ns
t_{ZL}						17	ns
t_{ZH}			C_L = 50pF		7.3	12	ns
t_{ZL}					9.7	12	ns
t_{HZ}	Output Disable Time $\overline{OE}$ ↓ to Y_i		C_L = 50pF		10.4	14	ns
t_{LZ}					4.7	11	ns
t_{HZ}			C_L = 5pF (Note 5)		3.4	8	ns
t_{LZ}					3.8	8	ns

Notes: 4. See test circuit and waveforms.
5. Not tested.

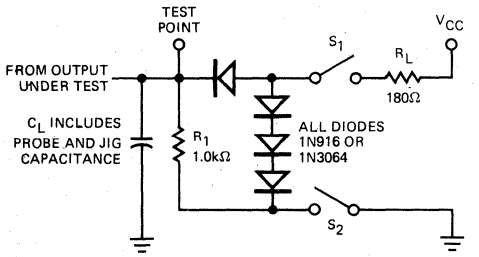
8

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



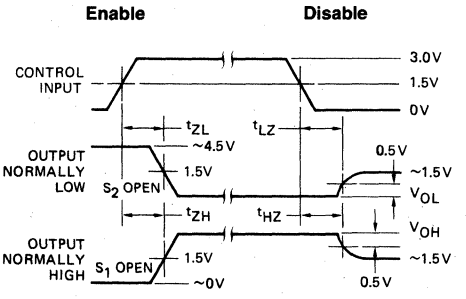
ABI-019

LOAD TEST CIRCUIT



ABI-014

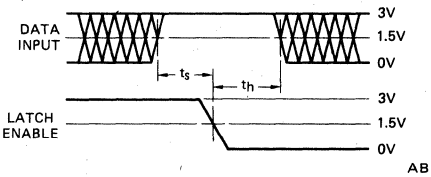
ENABLE AND DISABLE TIMES



ABI-015

Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1 and S_2 of Load Circuit are closed except where shown.

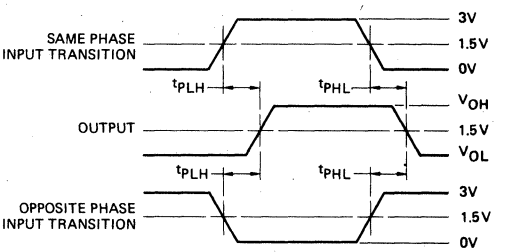
SET UP, HOLD, AND RELEASE TIMES



ABI-016

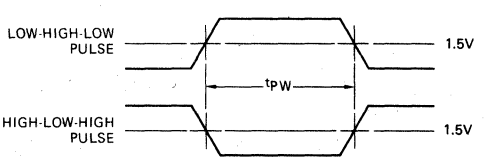
Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

PROPAGATION DELAY



ABI-017

PULSE WIDTH



ABI-018

Note: Pulse Generator for All Pulses: Rate ≤ 10MHz; $Z_O = 50\Omega$; $t_r \leq 2.5$ns; $t_f \leq 2.5$ns.

DEFINITION OF FUNCTION TERMS

Am29841/43/45 (Noninverting)

$\overline{CLR}$ When $\overline{CLR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.

D_i The latch data inputs.

LE The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.

Y_i The 3-state latch outputs.

$\overline{OE}$ The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When OE is HIGH, the outputs Y_i are in the high-impedance (off) state.

$\overline{PRE}$ Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.

FUNCTION TABLE

Inputs					Internal	Outputs	
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_i	Q_i	Y_i	Function
H	H	H	X	X	X	Z	Hi-Z
H	H	H	H	L	L	Z	Hi-Z
H	H	H	H	H	H	Z	Hi-Z
H	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (Hi-Z)
H	L	H	L	X	H	Z	Latched (Hi-Z)

DEFINITION OF FUNCTION TERMS

Am29842/44/46 (Inverting)

$\overline{CLR}$ When $\overline{CLR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.

D_i The latch inverting data inputs.

LE The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.

Y_i The 3-state latch outputs.

$\overline{OE}$ The output enable control. When OE is LOW, the outputs are enabled. When OE is HIGH, the outputs Y_i are in the high-impedance (off) state.

$\overline{PRE}$ Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.

FUNCTION TABLE

Inputs					Internal	Outputs	
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_i	Q_i	Y_i	Function
H	H	H	X	X	X	Z	Hi-Z
H	H	H	H	H	L	Z	Hi-Z
H	H	H	H	L	H	Z	Hi-Z
H	H	H	L	X	NC	Z	Latched (Hi-Z)
H	H	L	H	H	L	L	Transparent
H	H	L	H	L	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (Hi-Z)
H	L	H	L	X	H	Z	Latched (Hi-Z)

8

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

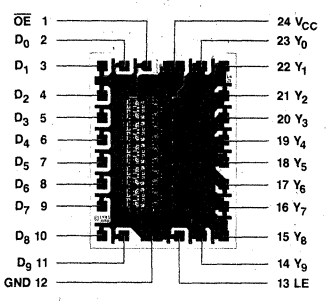
Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2984_DC	D-24-SLIM	C	C-1
AM2984_DCB	D-24-SLIM	C	B-2 (Note 4)
AM2984_DM	D-24-SLIM	M	C-3
AM2984_DMB	D-24-SLIM	M	B-3
AM2984_LC	L-28-1	C	C-1
AM2984_LCB	L-28-1	C	B-2 (Note 4)
AM2984_LM	L-28-1	M	C-3
AM2984_LMB	L-28-1	M	B-3
AM2984_XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2984_XM	Dice	M	

Notes: 1. D = Hermetic DIP, L = Chip-Pak. Number following letter is number of leads.
2. C = 0 to +70°C, V_{CC} = 4.5 to 5.5V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 160 hour burn-in.

METALLIZATION AND PAD LAYOUTS

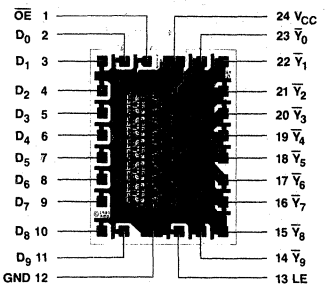
10-Bit Latches

Am29841



ABI-099

Am29842

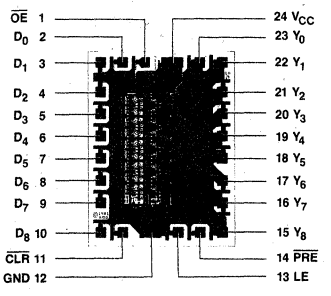


ABI-100

DIE SIZE 0.084" X 0.064"

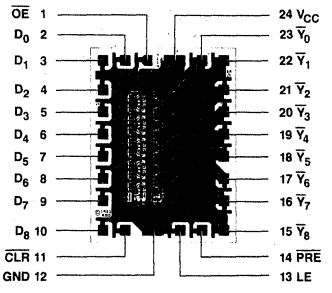
9-Bit Latches

Am29843



ABI-101

Am29844

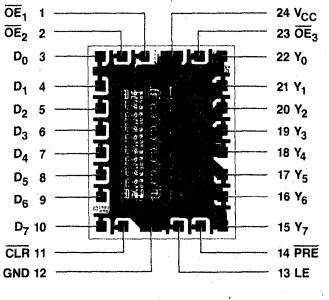


ABI-102

DIE SIZE 0.084" X 0.064"

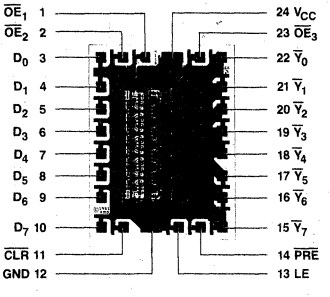
8-Bit Latches

Am29845



ABI-103

Am29846



ABI-104

DIE SIZE 0.084" X 0.064"

Am29861 • Am29862
Am29863 • Am29864

High Performance Bus Transceivers
ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

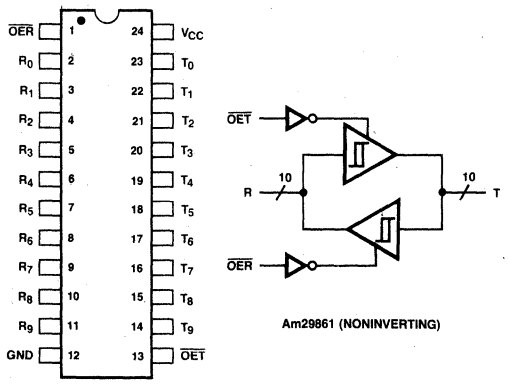
- High-speed symmetrical bidirectional transceivers
  - Noninverting t_{PD} = 4.5ns typ
  - Inverting t_{PD} = 4.0ns typ
- 200mV minimum input hysteresis on input data ports
- Three-state outputs glitch-free during power-up and -down
- Outputs have Schottky clamp to ground
- 48mA commercial I_{OL}, 32mA military I_{OL}
- Low input/output capacitance
  - 6pF inputs (typical)
  - 8pF outputs (typical)
- I_{OH} specified 2.0V and 2.4V
- 24-pin 0.3″ space saving package
- Fully TTL compatible inputs and outputs
- IMOX™ high performance IMplanted OXide isolated process

FUNCTIONAL DESCRIPTION

The Am29860 Series bus transceivers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. The Am29863/64 9-bit transceivers have NOR-ed output enables for maximum control flexibility. All transceiver data inputs have 200mV minimum input hysteresis to provide improved noise rejection.

All of the Am29800 high performance interface family are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

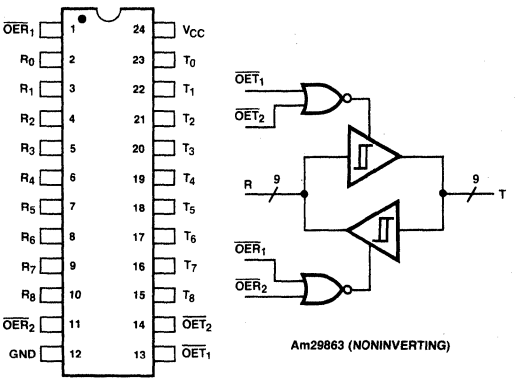
Am29861/Am29862
10-BIT TRANSCEIVERS



Am29861 (NONINVERTING)

ABI-092

Am29863/Am29864
9-BIT TRANSCEIVERS



Am29863 (NONINVERTING)

ABI-093

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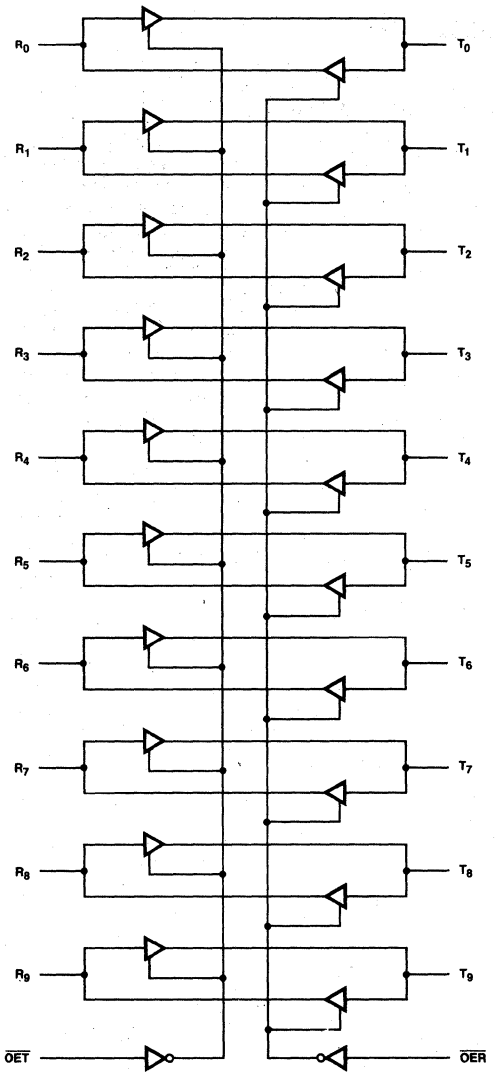
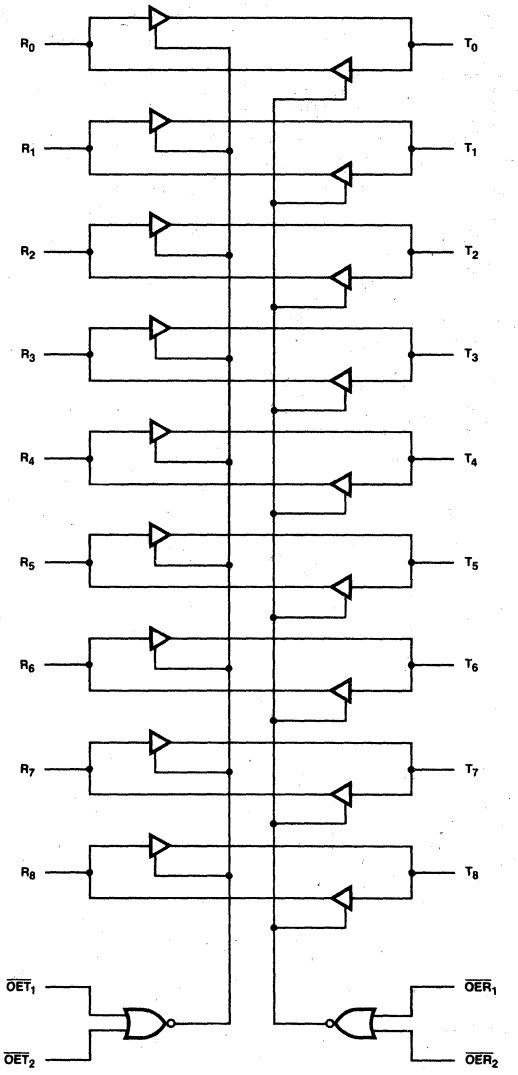
IMOX is a trademark of Advanced Micro Devices, Inc.

Am29861/Am29862
10-BIT TRANSCEIVERS



ABI-094

Am29863/Am29864
9-BIT TRANSCEIVERS



ABI-095

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 to +7.0V
DC Voltage Applied to Output for High Output State	−1.5 to V_{CC} max
DC Input Voltage	−0.5 to +5.5V
DC Output Current, Into Outputs	100mA
DC Input Current	−30 to +5.0mA

ELECTRICAL CHARACTERISTICS

COM'L T_A = 0 to +70°C, V_{CC} = 5.0V ± 10% (MIN = 4.5V, MAX = 5.5V)
MIL T_C = −55 to +125°C, V_{CC} = 5.0V ± 10% (MIN = 4.5V, MAX = 5.5V)

Parameter	Description	Test Conditions		Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15mA	2.4			V
			I_{OH} = −24mA	2.0			
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	MIL, I_{OL} = 32mA			0.5	V
			COM'L, I_{OL} = 48mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	V
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	V
V_{HYST}	Input Hysteresis	V_{CC} = MIN		200			mV
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V				−1.0	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				100	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{OZH}	Output Off-state Output Current (HI-Z)	V_{CC} = MAX, V_O = 2.4V				100	μA
I_{OZL}	Output Off-state Output Current (HI-Z)	V_{CC} = MAX, V_O = 0.4V				−1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX		−75		−250	mA
I_{CC}	Supply Current	V_{CC} = MAX, Outputs Open	Outputs Enabled			145	mA
			Outputs Disabled			155	

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ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2982_DC	D-24-SLIM	C	C-1
AM2982_DCB	D-24-SLIM	C	B-2 (Note 4)
AM2982_DM	D-24-SLIM	M	C-3
AM2982_DMB	D-24-SLIM	M	B-3
AM2982_LC	L-28-1	C	C-1
AM2982_LCB	L-28-1	C	B-2 (Note 4)
AM2982_LM	L-28-1	M	C-3
AM2982_LMB	L-28-1	M	B-3
AM2982_XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2982_XM	Dice	M	

Notes: 1. D = Hermetic DIP, L = Chip-Pak™. Number following letter is number of leads.
2. C = 0 to +70°C, V_{CC} = 4.50 to 5.50V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 160 hour burn-in.

Am29861/62/63/64
Am29861/Am29862/Am29863/Am29864
SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameter	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay from R_i to T_i or T_i to R_i Am29861/Am29863 (Noninverting)	C_L = 50pF		4.5	5.5	ns
t_{PHL}				4.5	5.5	ns
t_{PLH}		C_L = 300pF			11	ns
t_{PHL}					11	ns
t_{PLH}	Propagation Delay from R_i to $\overline{T_i}$ or $\overline{T_i}$ to R_i Am29862/Am29864 (Inverting)	C_L = 50pF		4.0	5	ns
t_{PHL}				4.0	5	ns
t_{PLH}		C_L = 300pF			10	ns
t_{PHL}					10	ns
t_{ZH}	Output Enable Time $\overline{OET}$ to T_i and $\overline{OER}$ to R_i	C_L = 50pF		6.5		ns
t_{ZL}				9.5		ns
t_{ZH}		C_L = 300pF				ns
t_{ZL}						ns
t_{HZ}	Output Disable Time OET to T_i and OER to R_i	C_L = 5pF				ns
t_{LZ}						ns
t_{HZ}		C_L = 50pF		11.2		ns
t_{LZ}				4.2		ns

Am29861/Am29862/Am29863/Am29864
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			COM'L		MIL		
			T_A = 0 to +70°C, V_{CC} = 5.0V ± 10%		T_C = −55 to +125°C, V_{CC} = 5.0V ± 10%		
Parameters	Description	Test Conditions	Min	Max	Min	Max	Units
t_{PLH}	Propagation Delay from R_i to $\overline{T_i}$ or $\overline{T_i}$ to R_i Am29861/Am29863 (Noninverting)	C_L = 50pF		10		12	ns
t_{PHL}				10		12	ns
t_{PLH}		C_L = 300pF		15		17	ns
t_{PHL}				15		17	ns
t_{PLH}	Propagation Delay from R_i to $\overline{T_i}$ or $\overline{T_i}$ to R_i Am29862/Am29864 (Inverting)	C_L = 50pF		9		11	ns
t_{PHL}				9		11	ns
t_{PLH}		C_L = 300pF		14		16	ns
t_{PHL}				14		16	ns
t_{ZH}	Output Enable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i	C_L = 50pF		15		17	ns
t_{ZL}				15		17	ns
t_{ZH}		C_L = 300pF		18.5		20.5	ns
t_{ZL}				18.5		20.5	ns
t_{HZ}	Output Disable Time $\overline{OET}$ to T_i or $\overline{OER}$ to R_i	C_L = 5pF		10		12	ns
t_{LZ}				10		12	ns
t_{HZ}		C_L = 50pF		18.5		20.5	ns
t_{LZ}				18.5		20.5	ns

DEFINITION OF FUNCTIONAL TERMS

Am29861/Am29862

$\overline{OER}$ When LOW is in conjunction with $\overline{OET}$ HIGH indicates the RECEIVE mode.

$\overline{OET}$ When LOW in conjunction with $\overline{OER}$ HIGH indicates the TRANSMIT mode.

R_i 10-bit RECEIVE input/output.

T_i 10-bit TRANSMIT input/output.

Am29863/Am29864

$\overline{OER}_i$ When both are LOW in conjunction with $\overline{OET}_i$ both HIGH indicates the RECEIVE mode.

$\overline{OET}_i$ When both are LOW in conjunction with $\overline{OER}_i$ both HIGH indicates the TRANSMIT mode.

R_i 9-bit RECEIVE input/output.

T_i 9-bit TRANSMIT input/output.

FUNCTION TABLES

Am29861/Am29863 (Noninverting)

Inputs				Outputs		
$\overline{OET}$	$\overline{OER}$	R_i	T_i	R_i	T_i	Function
L	H	L	N/A	N/A	L	Transmitting
L	H	H	N/A	N/A	H	Transmitting
H	L	N/A	L	L	N/A	Receiving
H	L	N/A	H	H	N/A	Receiving
H	H	X	X	Z	Z	HI-Z

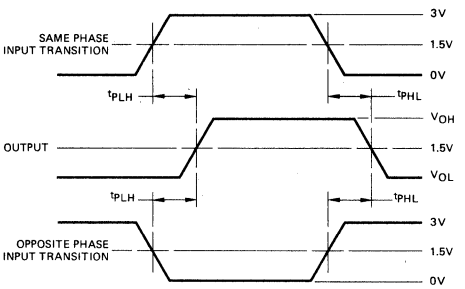
Am29862/Am29864 (Inverting)

Inputs				Outputs		
$\overline{OET}$	$\overline{OER}$	R_i	$\overline{T}_i$	R_i	$\overline{T}_i$	Function
L	H	L	N/A	N/A	H	Transmitting
L	H	H	N/A	N/A	L	Transmitting
H	L	N/A	L	H	N/A	Receiving
H	L	N/A	H	L	N/A	Receiving
H	H	X	X	Z	Z	HI-Z

H = HIGH X = Don't Care
L = LOW N/A = Not Applicable
Z = High Impedance

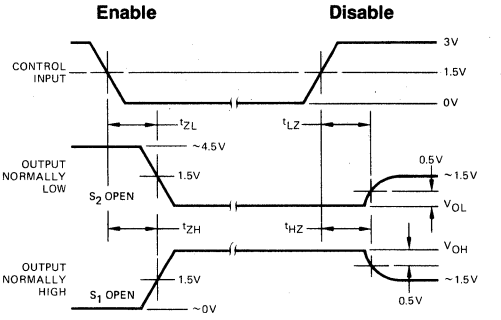
SWITCHING TIME WAVEFORMS AND AC TEST CIRCUITS

PROPAGATION DELAY



ABI-096

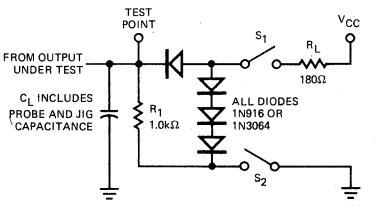
ENABLE AND DISABLE TIMES



Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1 and S_2 of Load Circuit are closed except where shown.

ABI-097

LOAD TEST CIRCUIT



ABI-098

Note: Pulse Generator for All Pulses: Rate ≤ 10MHz; $Z_o = 50\Omega$; $t_r \leq 2.5$ns; $t_f \leq 2.5$ns.

Am25S and Am25LS Logic Family Index

Am25S05

Four-Bit by Two-Bit Two's Complement Multiplier

Distinctive Characteristics

- Provides 2's complement multiplication at high speed without correction.
- Can be used in a combinatorial array or in a time sequenced mode.
- Multiplies two 12-bit signed numbers in typically 115 ns.
- Multiplies in active HIGH (positive logic) or active LOW (negative logic) representations.
- Reduced input loading as compared to Am2505.
- 100% reliability assurance testing in compliance with MIL-STD-883.

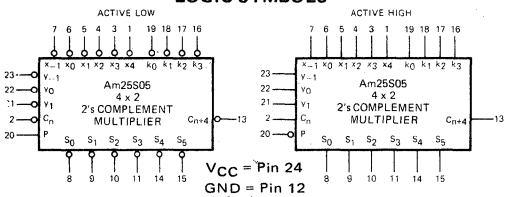
FUNCTIONAL DESCRIPTION

The Am25S05 is a high-speed digital multiplier that can multiply numbers represented in the 2's complement notation and produce a 2's complement product without correction. The device consists of a 4x2 multiplier that can be connected to form iterative arrays able to multiply numbers either directly, or in a time sequenced arrangement. The device assumes that the most significant digit in a word carries a negative weight, and can therefore be used in arrays where the multiplicand and multiplier have different word lengths. The multiplier uses the quaternary algorithm and performs the function $S = XY + K$ where K is the input field used to add partial products generated in the array. At the beginning of the array the K inputs are available to add a signed constant to the least significant part of the product. Multiplication of an m bit number by an n bit number in an array results in a product having m+n bits so that all possible combinations of product are accounted for. If a conventional 2's complement product is required the most significant bit can be ignored, and overflow conditions can be detected by comparing the last two product digits.

A number of connection schemes are possible. Figure 1 shows the connection scheme that results in the fastest multiply. If higher speed is required an array can be split into several parts, and the parts added with high-speed look-ahead carry adders.

Provision is made in the design for multiplication in the active high (positive logic) or active low (negative logic) representations simply by reinterpreting the active level of the input operands, the product, and a polarity control $\overline{P}$.

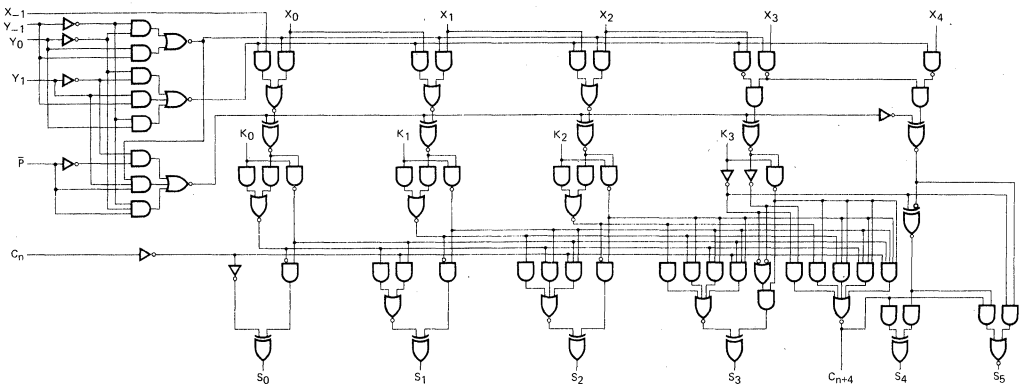
LOGIC SYMBOLS



RELATED PRODUCTS

Part No.	Description
Am25LS14A	8-Bit Serial/Parallel Multiplier
Am25LS557/8	8-Bit by 8-Bit Multiplier
Am29516/7	16-Bit by 16-Bit Multiplier

LOGIC DIAGRAM

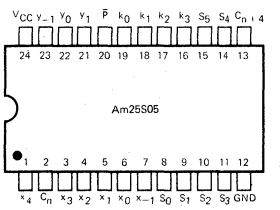


Am25S05 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	AM25S05PC
Hermetic DIP	0°C to +75°C	AM25S05DC
Dice	0°C to +75°C	AM25S05XC
Hermetic DIP	-55°C to +125°C	AM25S05DM
Hermetic Flat Pak	-55°C to +125°C	AM25S05FM
Dice	-55°C to +125°C	AM25S05XM

DIP package is 24 pin 0.6" wide.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am25S05XC, DC, PC	T_A = 0°C to +75°C	V_{CC} = 4.75 V to 5.25 V
Am25S05XM, DM	T_A = −55°C to +125°C	V_{CC} = 4.50 V to 5.50 V
Am25S05FM	T_C = −55°C to +125°C	V_{CC} = 4.50 V to 5.50 V

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1.0mA V_{IN} = V_{IH} or V_{IL}	XM	2.5	3.3		Volts
			XC	2.7	3.3		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}			0.3	0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V				−2.0	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				50	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., Y_1 = 0V			120	175	mA

Note 1. Typical Limits are at V_{CC} = 5.0V, 25°C Ambient and maximum loading.
Note 2. Actual input currents are obtained by multiplying unit load current by the input load factor. (See loading rules)

Switching Characteristics (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 280Ω)

Parameters	From (Input)	To (Output)	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH} t_{PHL}	C_n	C_{n+4}	See Test Table	4 4	8 9	12 14	ns
t_{PLH} t_{PHL}	C_n	$S_{0,1,2,3}$		6 5	12 10	18 15	ns
t_{PLH} t_{PHL}	C_n	$S_{4,5}$		7 6	15 13	22 20	ns
t_{PLH} t_{PHL}	Any k	C_{n+4}		3 5	6.5 10	12 15	ns
t_{PLH} t_{PHL}	Any k	$S_{0,1,2,3}$		6 4	13.5 9.5	20 14	ns
t_{PLH} t_{PHL}	Any k	$S_{4,5}$		3 3	15.5 12.5	23 19	ns
t_{PLH} t_{PHL}	Any x	C_{n+4}		8 9	17 18	26 27	ns
t_{PLH} t_{PHL}	Any x	$S_{0,1,2,3}$		10 10	21 21	32 32	ns
t_{PLH} t_{PHL}	Any x	$S_{4,5}$		6 5	23.5 21.5	35 32	ns
t_{PLH} t_{PHL}	Any y	C_{n+4}		11 10	23 20	34 30	ns
t_{PLH} t_{PHL}	Any y	$S_{0,1,2,3}$		11 11	23 23	34 34	ns
t_{PLH} t_{PHL}	Any y	$S_{4,5}$		12 12	25 25	37 37	ns

SWITCHING TIME TEST TABLE

Input	Outputs	Inputs at 0V (remaining inputs at 4.5V)
C_n	C_{n+4}, S_{0123}, S_{45}	P, Y_{-1}, Y_1, All X
k_0	C_{n+4}, S_{0123}, S_{45}	P, Y_{-1}, Y_1, All X
k_1	C_{n+4}, S_{123}, S_{45}	P, Y_{-1}, Y_1, All X
k_2	C_{n+4}, S_{23}, S_{45}	P, Y_{-1}, Y_1, All X
k_3	S_3	P, Y_{-1}, Y_1, All X
k_3	S_{45}	P, Y_{-1}, Y_1, All X, C_n
x_{-1}	C_{n+4}, S_{0123}, S_{45}	P, Y_1, All k
x_0	C_{n+4}, S_{0123}, S_{45}	P, Y_{-1}, Y_1, All k
x_1	C_{n+4}, S_{123}, S_{45}	P, Y_{-1}, Y_1, All k
x_2	C_{n+4}, S_{123}, S_{45}	P, Y_{-1}, Y_1, All k
x_3	S_3	P, Y_{-1}, Y_1, All k
x_3	S_{45}	P, Y_{-1}, Y_1, All k, C_n
x_4	S_{45}	P, Y_1, All k, C_n
y_{-1}	C_{n+4}, S_{0123}, S_{45}	P, X_1, X_2, X_3, X_4, All k
y_0	C_{n+4}, S_{0123}, S_{45}	P, X_1, X_2, X_3, X_4, All k
y_1	C_{n+4}, S_{0123}, S_{45}	X_0, X_1, X_2, X_3, X_4, All k

9

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS

C_n The carry input to the high-speed adder.

C_{n+4} The carry output from the high-speed adder.

k_i The constant field used for accumulating partial products.
i = 0, 1, 2, 3. At the beginning of the array the K field can be used to add a 2's complement number to the least significant half of the double length product.

$\overline{P}$ The polarity control input. This input must be at a low-logic level for numbers in the active high logic representation, and held high for numbers in the active low logic representation.

S_i The product outputs. i = 0, 1, 2, 3, 4, 5.

x_i The multiplicand inputs. i = –1, 0, 1, 2, 3, 4. At the first column of the array x_{-1} must be held at logic '0', and at the last column of the array x_4 is connected to x_3.

y_i The multiplier inputs. i = –1, 0, 1.
At the first row of the array y_{-1} must be held at logic '0'.

OPERATIONAL TERMS:

I_{IL} Forward input load current.

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{CC} The current drawn by the device from V_{CC} power supply with input and output terminals open.

I_{IH} Reverse input load current.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{IN} Input voltage applied in I_{IL}, I_{IH} tests.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} flowing into output.

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 54/7400 Series	1.25	1.25
Advanced Micro Devices 9300/2500 Series	1.25	1.25
FSC Series 9300	1.25	1.25
TI Series 54/7400	1.25	1.25
Signetics Series 8200	2.5	2.5
National Series DM 75/85	1.25	1.25
DTL Series 930	15	1.25

OPERATION TABLE

Y Multiplier y_{-1}	y_0	y_1	Operation X Multiplicand
0	0	0	K + 0
1	0	0	K + X
0	1	0	K + X
1	1	0	K + 2X
0	0	1	K – 2X
1	0	1	K – X
0	1	1	K – X
1	1	1	K – 0

Active Low Inputs and Outputs
'1' = Low, '0' = High, P = High
Active High Inputs and Outputs
'1' = High, '0' = Low, $\overline{P}$ = Low

Am25S05 LOADING RULES IN UNIT LOADS

Input/Output	Pin No.'s	Input Unit Load Input HIGH	Input LOW	Fanout Output HIGH	Output LOW
x_4	1	0.2	0.2	–	–
C_n	2	0.2	0.2	–	–
x_3	3	0.2	0.2	–	–
x_2	4	0.4	0.4	–	–
x_1	5	0.4	0.4	–	–
x_0	6	0.4	0.4	–	–
x_{-1}	7	0.2	0.2	–	–
S_0	8	–	–	20	10
S_1	9	–	–	20	10
S_2	10	–	–	20	10
S_3	11	–	–	20	10
GND	12	–	–	–	–
C_{n+4}	13	–	–	20	10
S_4	14	–	–	20	10
S_5	15	–	–	20	10
k_3	16	2	2	–	–
k_2	17	2	2	–	–
k_1	18	2	2	–	–
k_0	19	2	2	–	–
$\overline{P}$	20	1	1	–	–
y_1	21	0.6	0.6	–	–
y_0	22	0.6	0.6	–	–
y_{-1}	23	0.6	0.6	–	–
V_{CC}	24	–	–	–	–

A Schottky TTL Unit Load is defined as 50μA at 2.7V at the HIGH Logic Level and –2.0 mA at 0.5 V at the LOW Logic Level.

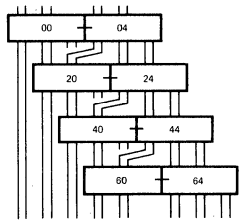
USER NOTES

1. Arithmetic in the multiplier is performed in the 2's complement notation, which requires a carry in at the first stage. This is accomplished by connecting the y_i multiplier bit to the appropriate carry input terminal i = 1, 3, 5 . . .
2. The multiplier can perform multiplication in either the active high (positive logic) or active low (negative logic) representations by reinterpreting the active logic level and by grounding or leaving the polarity control pin $\overline{P}$ open circuit respectively.
3. Multiplication can be performed in number representations other than 2's complement by either correcting the 2's complement product or adding in a correction at the beginning of the multiplication at the K inputs. 2's complement numbers are represented as: $X_2 = x - x_s 2^{n-1}$.

Number representation	Correction
2's complement	None
1's complement	Add $x_s Y_2 + y_s X_2 + x_s y_s$ at k inputs
Unsigned (magnitude)	Extend multiplier and multiplicand one bit at the least significant end. Form $x_0 y_0 + y_0 x + x_0 y$ with conditional adder and add to array shifted two places up at k inputs. Force $k_s, y_s, x_s = 0$.
Sign magnitude	$x_s = 0, y_s = 0$ None
	$x_s = 1, y_s = 0$ Form $[(XY)_2 + 2^{n-1} y]$
	$x_s = 0, y_s = 1$ Form $[(XY)_2 + 2^{n-1} x]$
	$x_s = 1, y_s = 1$ Add $2^{n-1}(x + y) - 2^{2n-2}$

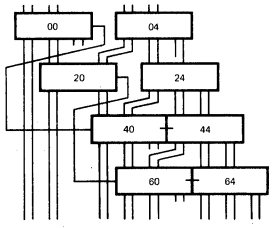
4. For the highest speed array with the multipliers arranged in a parallelogram structure carries between certain multipliers are exchanged with the y carry-ins needed for 2's complement subtract. The delays in the array are then equalized as best possible as shown in Figure 1.
5. For higher speed multiplication the array can be split into several parts that can be added together with high-speed adders.
6. Rounding off to a single length product can be achieved by adding a '1' to the array at the most significant positive k input of the array, ignoring the most significant product digit, and using the remainder of the most significant part of the product.
7. Truncation of a product without round off enables some of the multipliers in the array to be removed.

CONNECTION SCHEMES



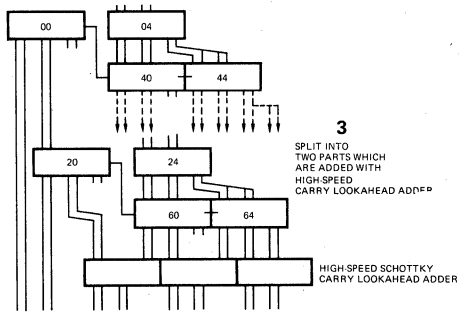
1

PARALLELOGRAM CARRIES STAY IN SAME ROW



2

PARALLELOGRAM CARRIES FROM LOWER ORDER MULTIPLIERS SKIP TO ALTERNATE ROWS WHERE POSSIBLE

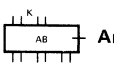


3

SPLIT INTO TWO PARTS WHICH ARE ADDED WITH HIGH-SPEED CARRY LOOKAHEAD ADDER

TYPICAL MULTIPLICATION TIMES

Array Size Bits	Total Multiplication Time (ns)	Package Count	
		Am25S05	Am54S/74S181
4x4	35	2	
8x8	75	8	
12x12	115	18	
12x12	82	18	5
16x16	155	32	
16x16	111	32	7
16x16	98	32	16
20x20	195	50	
20x20	130	50	9
24x24	235	72	
24x24	149	72	11
24x24	125	72	24
28x28	275	98	
28x28	168	98	13
32x32	315	128	
32x32	187	128	15
32x32	152	128	32



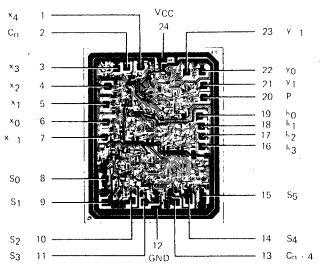
Am25S05

$Y = (Y_{-1}\, Y_0\, Y_1)\, 2^A$

$X = (X_{-1}\, X_0\, X_1\, X_2\, X_3)\, 2^B$

Fig. 2

METALLIZATION AND PAD LAYOUT



9

Am25LS07 • Am25LS08

Hex/Quad Parallel D Registers with Register Enable

DISTINCTIVE CHARACTERISTICS

- 4-bit and 6-bit parallel registers
- Common Clock and Common Enable
- Positive edge triggered D flip flops
- Am25LS d. c. parameters including:
  V_{OL} = 0.45V at I_{OL} = 8mA
  Fan-out over military range = 22
  440μA source current
- Second sourced by TI as 54LS/74LS378 and 379

RELATED PRODUCTS

Part No.	Description
Am2918	Quad D Register
Am2919	Quad D Register

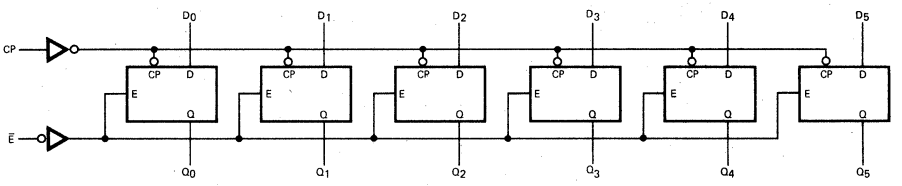
FUNCTIONAL DESCRIPTION

The Am25LS07 is a 6-bit Low Power Schottky register with a buffered common register enable. The Am25LS08 is a 4-bit register with a buffered common register enable. The devices are similar to the Am54LS/74LS174 and Am54LS/74LS175 but feature the common register enable rather than common clear.

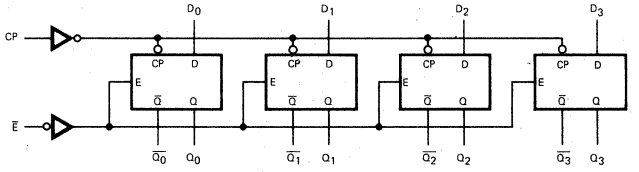
Both registers will find application in digital systems where information is associated with a logic gating signal. When the enable is LOW, data on the D inputs is stored in the register on the positive going edge of the clock pulse. When the enable is HIGH, the register will not change state regardless of the clock or data input transitions.

LOGIC DIAGRAMS

Am25LS07

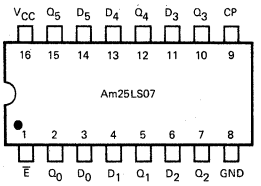


Am25LS08

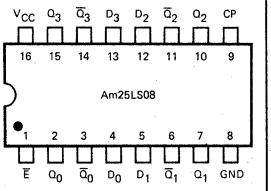


CONNECTION DIAGRAMS
Top Views

Am25LS07



Am25LS08



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0 to +70°C	AM25LS07/08PC
Hermetic DIP	0 to +70°C	AM25LS07/08DC
Dice	0 to +70°C	AM25LS07/08XC
Hermetic DIP	−55 to +125°C	AM25LS07/08DM
Hermetic Flat Pack	−55 to +125°C	AM25LS07/08FM
Dice	−55 to +125°C	AM25LS07/08XM

Am25LS07 • Am25LS08

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -440\mu A$, $V_{IN} = V_{IH}$ or V_{IL}	COM'L	2.7	3.4		Volts
			MIL	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 4mA			0.4	Volts
			I_{OL} = 8mA			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	COM'L			0.8	Volts
			MIL			0.7	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$	Clock, $\overline{E}$			−0.36	mA
			Others			−0.24	
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$	Clock, $\overline{E}$			20	μA
			Others			14	
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$				0.1	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 4)	LS07		16	22	mA
			LS08		11	18	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Outputs open; enable grounded; data inputs at 4.5V, measured after a momentary ground, then 4.5V applied to the clock input.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to $+V_{CC}$ max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

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SWITCHING CHARACTERISTICS

($T_A = +25°C$, $V_{CC} = 5.0V$)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Output		13	20	ns	$C_L = 15pF$, $R_L = 2.0k\Omega$
t_{PHL}	Clock to Output		13	20	ns	
t_{pw}	Clock Pulse Width	17			ns	
t_s	Data	20			ns	
t_s	Enable	30			ns	
t_h	Data	5.0			ns	
t_h	Enable	5.0			ns	
f_{max} (Note 1)	Maximum Clock Frequency	40	65		MHz	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

Am25LS07 • Am25LS08
SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Clock to Output		30		35	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}	Clock to Output		30		35	ns	
t_{pw}	Clock Pulse Width	26		30		ns	
t_s	Data	30		35		ns	
t_s	Enable	43		50		ns	
t_h	Data	11		12		ns	
t_h	Enable	11		12		ns	
f_{max} (Note 1)	Maximum Clock Frequency	30		25		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

D_i The D flip-flop data inputs.

$\overline{E}$ Enable. When the enable is LOW, data on the D_i inputs is transferred to the Q_i outputs on the LOW-to-HIGH clock transition. When the enable is HIGH, the Q_i outputs do not change regardless of the data or clock input transitions.

CP Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.

Q_i The TRUE register outputs.

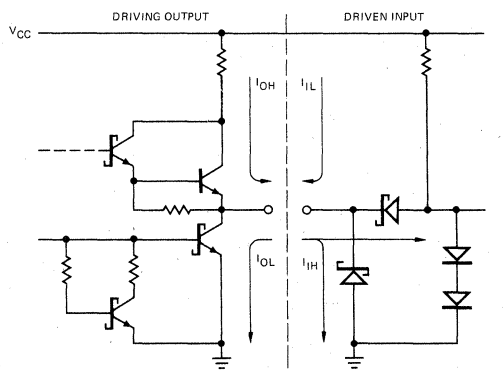
$\overline{Q}_i$ The complement register outputs

FUNCTION TABLE

Inputs $\overline{E}$	Inputs D_i	Inputs CP	Outputs Q_i	Outputs $\overline{Q}_i$
H	X	X	NC	NC
L	X	H	NC	NC
L	X	L	NC	NC
L	L	↑	L	H
L	H	↑	H	L

H = HIGH NC = No Change
L = LOW X = Don't Care
↑ = LOW-to-HIGH Transition
$\overline{Q}_i$ on Am25LS08 Only

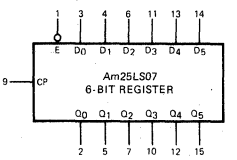
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



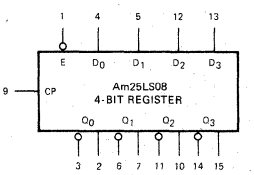
Note: Actual current flow direction shown.

LOGIC SYMBOLS

Am25LS07



Am25LS08



V_{CC} = Pin 16
GND = Pin 8

Am25S07 • Am25S08

Hex/Quad Parallel D Registers with Register Enable

Distinctive Characteristics

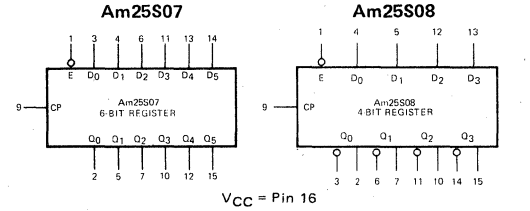
- 4-bit and 6-bit high-speed parallel registers
- Common clock and common enable
- Positive edge triggered D flip-flops

FUNCTIONAL DESCRIPTION

The Am25S07 is a 6-bit, high-speed Schottky register with a buffered common register enable. The Am25S08 is a 4-bit register with a buffered common register enable. The devices are similiar to the Am54S/74S174 and Am54S/74S175 but feature the common register enable rather than common clear.

Both registers will find application in digital systems where information is associated with a logic gating signal. When the enable is LOW, data on the D inputs is stored in the register on the positive going edge of the clock pulse. When the enable is HIGH, the register will not change state regardless of the clock or data input transitions.

LOGIC SYMBOLS



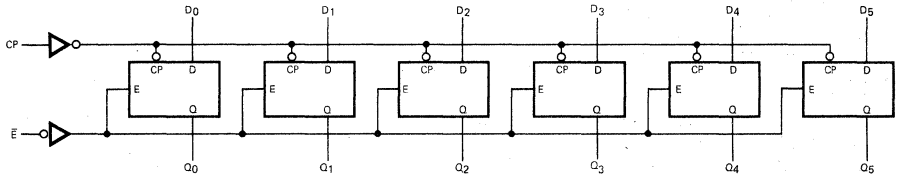
MPR-343 MPR-344

RELATED PRODUCTS

Part No.	Description
Am25LS07/08	Low Power Versions
Am2918	Quad D Register
Am2919	Quad Register
Am29821-26	8, 9, 10-Bit Register

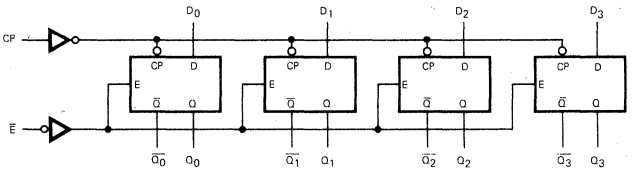
LOGIC DIAGRAMS

Am25S07



MPR-345

Am25S08



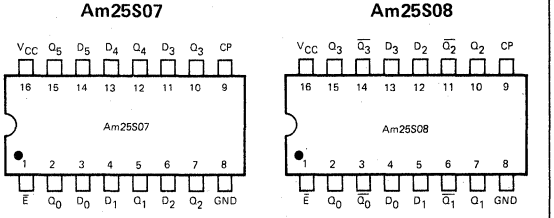
MPR-346

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0 to +70°C	AM25S07/08PC
Hermetic DIP	0 to +70°C	AM25S07/08DC
Dice	0 to +70°C	AM25S07/08XC
Hermetic DIP	−55 to +125°C	AM25S07/08DM
Hermetic Flat Pack	−55 to +125°C	AM25S07/08FM
Dice	−55 to +125°C	AM25S07/08XM

CONNECTION DIAGRAMS

Top Views



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Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am25S07XC, Am25S08XC T_A = 0°C to +70°C V_{CC} = 5.0 V ±5% (COM'L) MIN. = 4.75 V MAX. = 5.25 V
Am25S07XM, Am25S08XM T_A = −55°C to +125°C V_{CC} = 5.0 V ±10% (MIL) MIN. = 4.5 V MAX. = 5.5 V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1 mA V_{IN} = V_{IH} or V_{IL}	XC	2.7	3.4		Volts
			XM	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20 mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18 mA				−1.2	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5 V				−2	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7 V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.		−40		−100	mA
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX.	S07		90	144	mA
			S08		60	96	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Outputs open; enable grounded; data inputs at 4.5V, measured after a momentary ground, then 4.5V applied to the clock input.

Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Clock to Output	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 280Ω	4	8	12	ns
t_{PHL}	Clock to Output		4	11.5	17	ns
t_{pw}	Clock Pulse Width		7			ns
t_s	Data		5.5			ns
t_s	Enable		9			ns
t_h	Data		3			ns
t_h	Enable		3			ns

Am25S07 LOADING RULES (In STTL Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{E}$	1	1	–	–
Q_0	2	–	20	10
D_0	3	1	–	–
D_1	4	1	–	–
Q_1	5	–	20	10
D_2	6	1	–	–
Q_2	7	–	20	10
GND	8	–	–	–
CP	9	1	–	–
Q_3	10	–	20	10
D_3	11	1	–	–
Q_4	12	–	20	10
D_4	13	1	–	–
D_5	14	1	–	–
Q_5	15	–	20	10
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

Am25S08 LOADING RULES (In STTL Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{E}$	1	1	–	–
Q_0	2	–	20	10
$\overline{Q}_0$	3	–	20	10
D_0	4	1	–	–
D_1	5	1	–	–
$\overline{Q}_1$	6	–	20	10
Q_1	7	–	20	10
GND	8	–	–	–
CP	9	1	–	–
Q_2	10	–	20	10
$\overline{Q}_2$	11	–	20	10
D_2	12	1	–	–
D_3	13	1	–	–
$\overline{Q}_3$	14	–	20	10
Q_3	15	–	20	10
V_{CC}	16	–	–	–

DEFINITION OF FUNCTIONAL TERMS

D_i The D flip-flop data inputs.

$\overline{E}$ Enable. When the enable is LOW, data on the D_i inputs is transferred to the Q_i outputs on the LOW-to-HIGH clock transition. When the enable is HIGH, the Q_i outputs do not change regardless of the data or clock input transitions.

CP Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.

Q_i The TRUE register outputs.

$\overline{Q}_i$ The complement register outputs

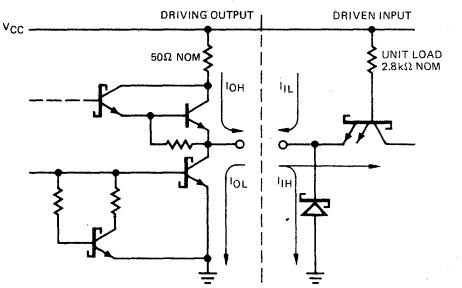
FUNCTION TABLE

Inputs			Outputs	
$\overline{E}$	D_i	CP	Q_i	$\overline{Q}_i$
H	X	X	NC	NC
L	X	H	NC	NC
L	X	L	NC	NC
L	L	↑	L	H
L	H	↑	H	L

H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition
$\overline{Q}_i$ on Am25S08 Only

NC = No Change
X = Don't Care

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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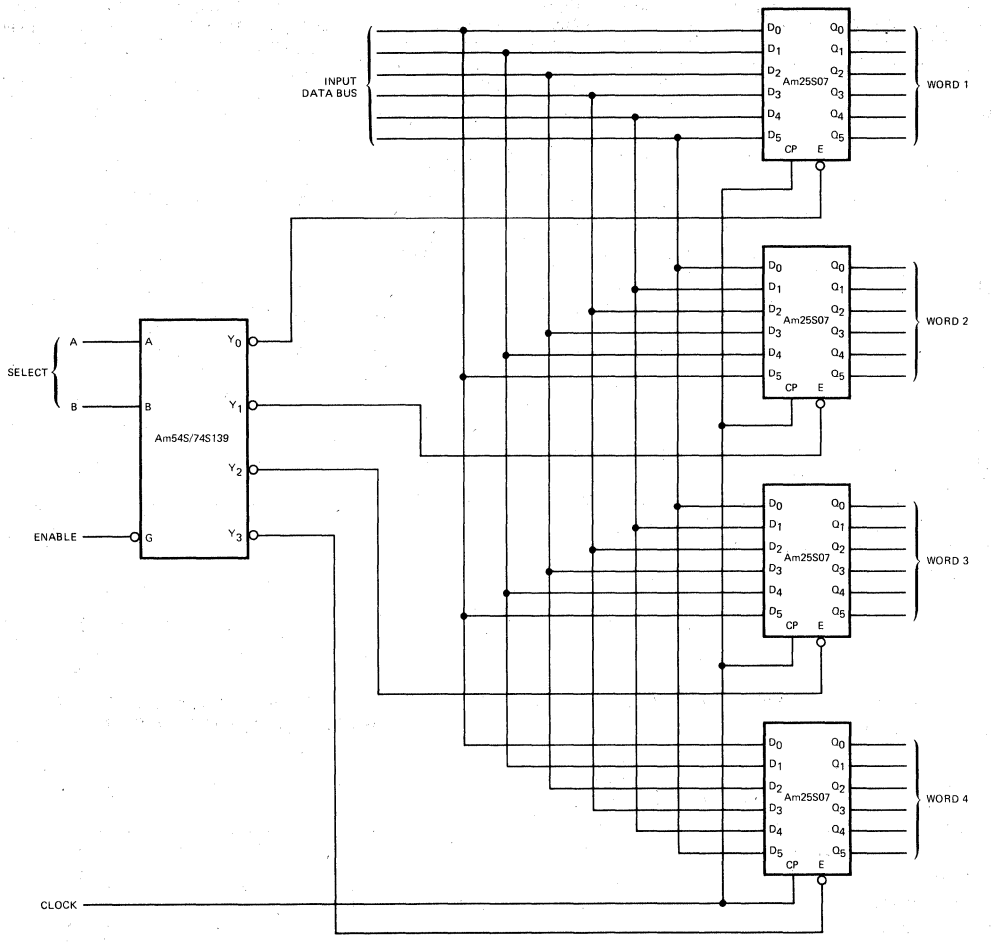
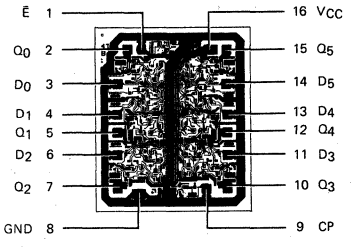
APPLICATIONS



Selective Register Loading of Data on Synchronous Clock.

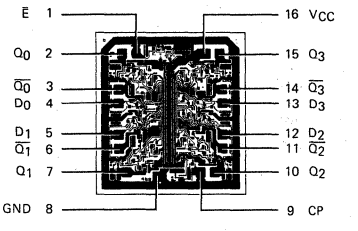
Metallization and Pad Layout

Am25S07



DIE SIZE: 0.070" X 0.083"

Am25S08



DIE SIZE: 0.067" X 0.073"

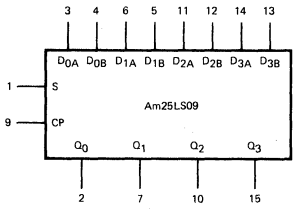
Am25LS09

Quad Two-Input, High-Speed Register

DISTINCTIVE CHARACTERISTICS

- 4-bit register accepts data from one-of-two 4-bit input fields
- Edge triggered clock action
- Second sourced by T.I. as 54LS/74LS399
- Am25LS d.c. parameters including:
  - V_{OL} = 0.45V at I_{OL} = 8mA
  - Fan-out over military range = 22
  - 440μA source current

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

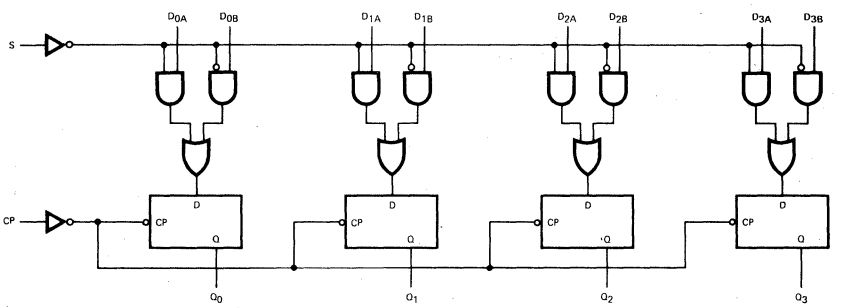
FUNCTIONAL DESCRIPTION

The Am25LS09 is a dual port four-bit register using advanced Low Power Schottky technology to reduce the effect of transistor storage time. The register consists of four D flip-flops with a buffered common clock, and a two-input multiplexer at the input of each flip-flop. A common select line, S, controls the four multiplexers. Data on the four inputs selected by the S line is stored in the four flip-flops at the clock LOW-to-HIGH transition. When the S input is LOW, the D_{iA} input data will be stored in the register. When the S input is HIGH, the D_{iB} input data will be stored in the register.

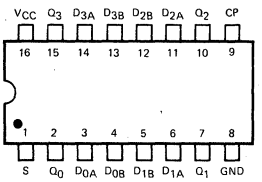
RELATED PRODUCTS

Part No.	Description
Am25S09	High Speed Register
Am25S07/08	6/4-Bit Registers
Am25LS07/08	6/4-Bit Low Power Registers

LOGIC DIAGRAM



CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0 to +70°C	AM25LS09PC
Hermetic DIP	0 to +70°C	AM25LS09DC
Chip-Pak	0 to +70°C	
Dice	0 to +70°C	AM25LS09XC
Hermetic DIP	−55 to +125°C	AM25LS09DM
Hermetic Flat Pack	−55 to +125°C	AM25LS09FM
Chip-Pak	−55 to +125°C	
Dice	−55 to +125°C	AM25LS09XM

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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5%	(MIN. = 4.75V MAX. = 5.25V)
MIL	T_A = −55°C to +125°C	V_{CC} = 5.0V ± 10%	(MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −440µA V_{IN} = V_{IH} or V_{IL}	COM'L	2.7	3.4		Volts
			MIL	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4mA			0.4	Volts
			I_{OL} = 8mA			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	Clock, S			−0.36	mA
			Others			−0.24	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	Clock, S			20	µA
			Others			14	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V				0.1	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 4)			11	18	mA

Notes: 1. For conditions shown as MIN. or MAX. use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Measured with Select and Clock inputs at 4.5V; all data inputs at 0V; all outputs open.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Q HIGH		13	20	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}	Clock to Q LOW		13	20	ns	
t_{pw}	Clock Pulse Width	17			ns	
t_s	Data Set-up Time	20			ns	
t_s	Select Input Set-up Time	30			ns	
t_h	Data Hold Time	5			ns	
t_h	Select Input Hold Time	0			ns	
f_{max} (Note 1)	Maximum Clock Frequency	40	65		MHz	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Clock to Q HIGH		30		35	ns	C_L = 50pF R_L = 2.0kΩ
t_{PHL}	Clock to Q LOW		30		35	ns	
t_{pw}	Clock Pulse Width	26		30		ns	
t_s	Data Set-up Time	30		35		ns	
t_s	Select Input Set-up Time	43		50		ns	
t_h	Data Hold Time	11		12		ns	
t_h	Select Input Hold Time	4		5		ns	
f_{max} (Note 1)	Maximum Clock Frequency	30		25		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

D_{0A}, D_{1A}, D_{2A}, D_{3A} The "A" word into the two-input multiplexer of the D flip-flops.

D_{0B}, D_{1B}, D_{2B}, D_{3B} The "B" word into the two-input multiplexer of the D flip-flops.

Q_0, Q_1, Q_2, Q_3 The outputs of the four D-type flip-flops of the register.

S Select. When the select is LOW, the A word is applied to the D inputs of the flip-flops. When the select is HIGH the B word is applied to the D inputs of the flip-flops.

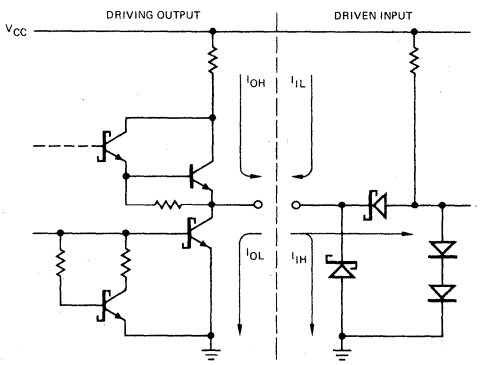
CP Clock Pulse. Clock pulse for the register. Enters data on the LOW-to-HIGH transition of the clock line.

FUNCTION TABLE

SELECT S	CLOCK CP	DATA D_{iA}	INPUTS D_{iB}	OUTPUT Q_i
L	↑	L	X	L
L	↑	H	X	H
H	↑	X	L	L
H	↑	X	H	H

H = HIGH Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition
L = LOW Voltage Level
i = 0, 1, 2, or 3

Am25LS • Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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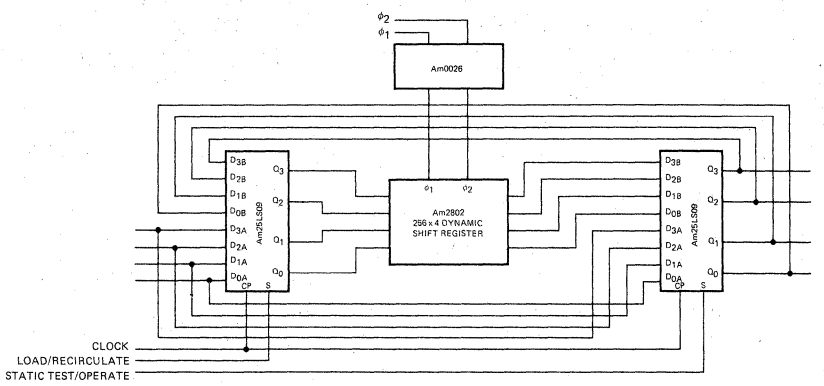
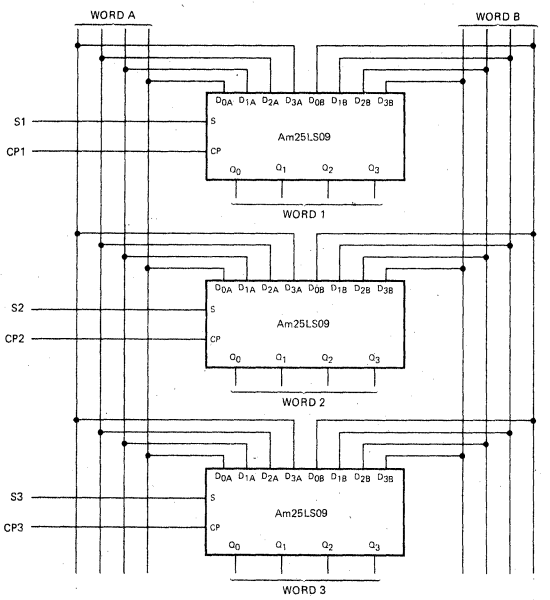
APPLICATIONS

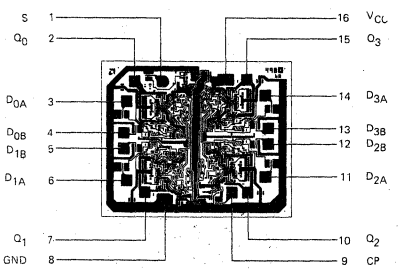


Am25LS09 used in 258 x 4 memory system with load/recirculate control, and 1 x 4 static test capability for the system. MOS interface is one load at each end. This circuit is especially useful in digital filtering where special algorithms require a static single step operation for testing purposes.



Am25LS09 used to store a word from either data bus A or data bus B.

Metallization and Pad Layout



DIE SIZE 0.075" X 0.061"

Am25S09

Quad Two-Input, High-Speed Register

Distinctive Characteristics

- Four-bit register accepts data from one of two 4-bit input fields.
- Edge triggered clock action
- High-speed Schottky technology.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

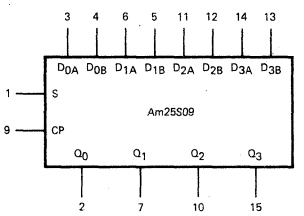
FUNCTIONAL DESCRIPTION

The Am25S09 is a dual port high-speed, four-bit register using advanced Schottky technology to reduce the effect of transistor storage time. The register consists of four D flip-flops with a buffered common clock, and a two-input multiplexer at the input of each flip-flop. A common select line, S, controls the four multiplexers. Data on the four inputs selected by the S line is stored in the four flip-flops at the clock LOW-to-HIGH transition. When the S input is LOW, the D_{iA} input data will be stored in the register. When the S input is HIGH, the D_{iB} input data will be stored in the register.

RELATED PRODUCTS

Part No.	Description
Am25LS09	Low Power Version
Am25S07/08	6/4-Bit Register
Am25LS07/08	6/4-Bit Low Power Register

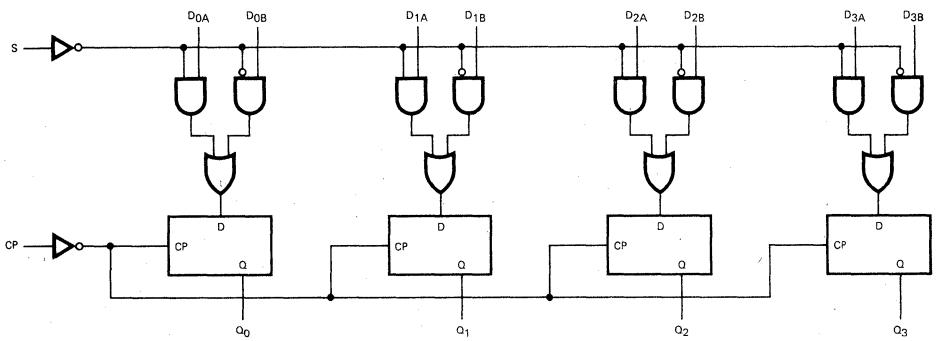
LOGIC SYMBOL



MPR-349

V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM

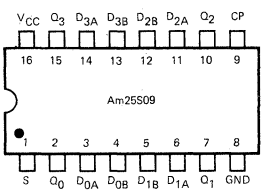


MPR-350

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0 to +70°C	AM25S09PC
Hermetic DIP	0 to +70°C	AM25S09DC
Chip-Pak	0 to +70°C	
Dice	0 to +70°C	AM25S09XC
Hermetic DIP	−55 to +125°C	AM25S09DM
Hermetic Flat Pack	−55 to +125°C	AM25S09FM
Chip-Pak	−55 to +125°C	
Dice	−55 to +125°C	AM25S09XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am25S09XC T_A = 0°C to +70°C V_{CC} = 5.0 V ±5% (COM'L) MIN. = 4.75 V MAX. = 5.25 V
Am25S09XM T_A = −55°C to +125°C V_{CC} = 5.0 V ±10% (MIL) MIN. = 4.5 V MAX. = 5.5 V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1.0mA V_{IN} = V_{IH} or V_{IL}	COM'L	2.7	3.4		Volts
			MIL	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20.0mA V_{IN} = V_{IH} or V_{IL}			0.3	0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5 V				−2.0	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7 V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)			75	120	mA

Notes: 1. For conditions shown as MIN. or MAX. use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Measured with Select and Clock inputs at 4.5V; all data inputs at 0V; all outputs open.

Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Clock to Q HIGH	V_{CC} = 5.0V, C_L = 15pF, R_L = 280Ω		8	12	ns
t_{PHL}	Clock to Q LOW			11.5	17	ns
t_{pw}	Clock Pulse Width		7			ns
t_s	Data Set-up Time		5.5			ns
t_s	Select Input Set-up Time		10			ns
t_h	Data Hold Time		3			ns
t_h	Select Input Hold Time		3			ns

FUNCTION TABLE

SELECT S	CLOCK CP	DATA D_{iA}	INPUTS D_{iB}	OUTPUT Q_i
L	↑	L	X	L
L	↑	H	X	H
H	↑	X	L	L
H	↑	X	H	H

H = HIGH Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition
L = LOW Voltage Level
i = 0, 1, 2, or 3

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
S	1	1	–	–
Q_0	2	–	20	10
D_{0A}	3	1	–	–
D_{0B}	4	1	–	–
D_{1B}	5	1	–	–
D_{1A}	6	1	–	–
Q_1	7	–	20	10
GND	8	–	–	–
CP	9	1	–	–
Q_2	10	–	20	10
D_{2A}	11	1	–	–
D_{2B}	12	1	–	–
D_{3B}	13	1	–	–
D_{3A}	14	1	–	–
Q_3	15	–	20	10
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50 μA measured at 2.7 V HIGH and –2.0 mA measured at 0.5 V LOW.

DEFINITION OF FUNCTIONAL TERMS

D_{0A}, D_{1A}, D_{2A}, D_{3A} The "A" word into the two-input multiplexer of the D flip-flops.

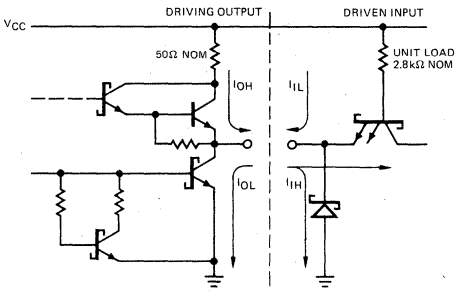
D_{0B}, D_{1B}, D_{2B}, D_{3B} The "B" word into the two-input multiplexer of the D flip-flops.

Q_0, Q_1, Q_2, Q_3 The outputs of the four D-type flip-flops of the register.

S Select. When the select is LOW, the A word is applied to the D inputs of the flip-flops. When the select is HIGH the B word is applied to the D inputs of the flip-flops.

CP Clock Pulse. Clock pulse for the register. Enters data on the LOW-to-HIGH transition of the clock line.

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown

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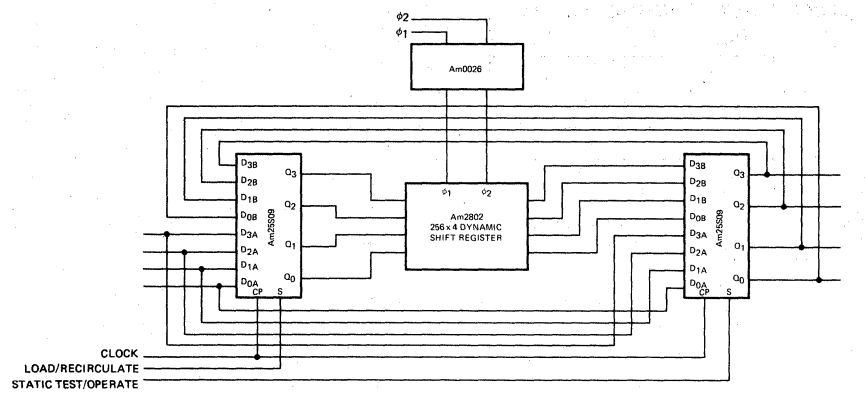
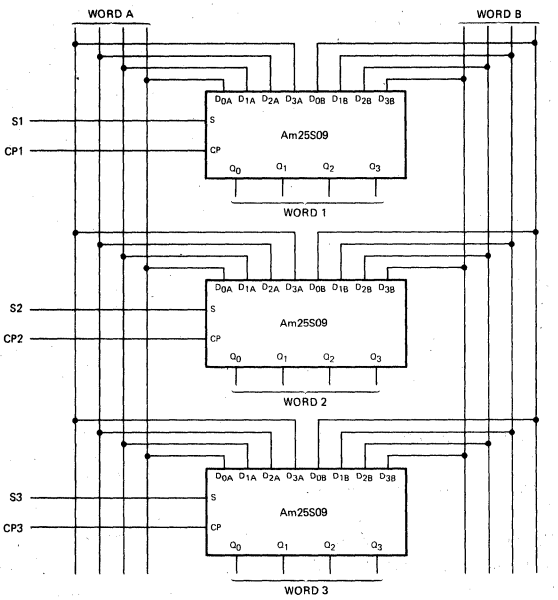
APPLICATIONS

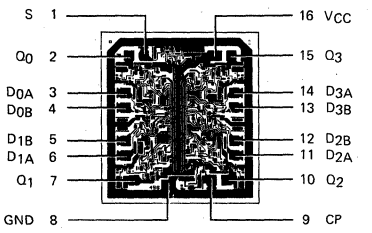


Am25S09 used in 258 x 4 memory system with load/recirculate control, and 1 x 4 static test capability for the system. MOS interface is one load at each end. This circuit is especially useful in digital filtering where special algorithms require a static single step operation for testing purposes.



Am25S09 used to store a word from either data bus A or data bus B.

Metallization and Pad Layout



DIE SIZE: 0.067" X 0.073"

Am25S10

Four-Bit Shifter with Three-State Outputs

Distinctive Characteristics

- Shifts 4-bits of data to 0, 1, 2 or 3 places under control of two select lines.
- Three-state outputs for bus organized systems.
- 6.5 ns typical data propagation delay
- Alternate source is 54S/74S350

FUNCTIONAL DESCRIPTION

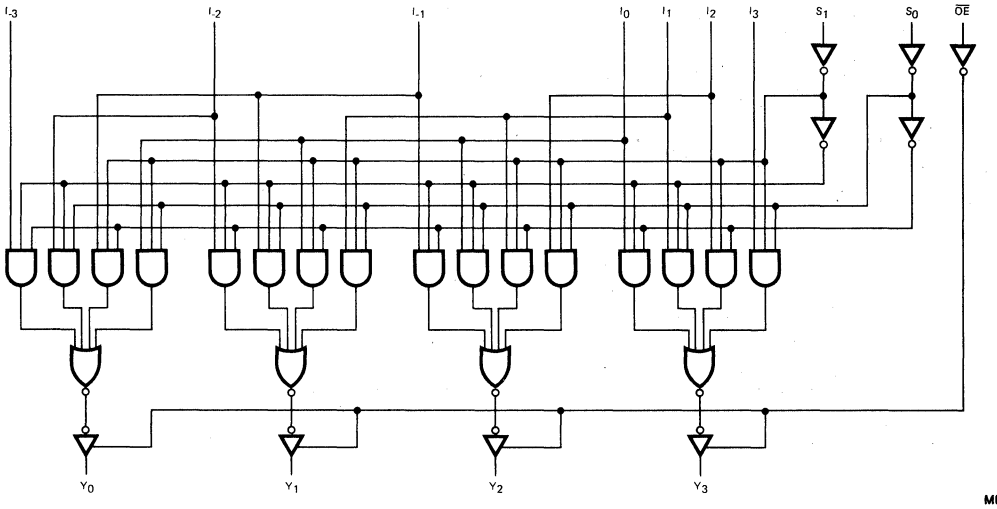
The Am25S10 is a combinatorial logic circuit that accepts a four-bit data word and shifts the word 0, 1, 2 or 3 places. The number of places to be shifted is determined by a two-bit select field S_0 and S_1. An active-LOW enable controls the three-state outputs. This feature allows expansion of shifting over a larger number of places with one delay.

By suitable interconnection, the Am25S10 can be used to shift any number of bits any number of places up or down. Shifting can be logical, with logic zeroes pulled in at either or both ends of the shifting field; arithmetic, where the sign bit is repeated during a shift down; or end around, where the data word forms a continuous loop.

RELATED PRODUCTS

Part No.	Description
Am2901	Bit Slice ALU
Am2903	Superslice
Am29501	Multiport Pipeline Processor

LOGIC DIAGRAM



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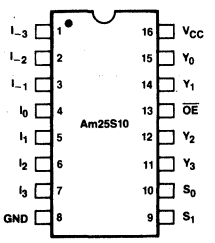
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0 to +70°C	AM25S10PC
Hermetic DIP	0 to +70°C	AM25S10DC
Chip-Pak	0 to +70°C	AM25S10LC
Dice	0 to +70°C	AM25S10XC
Hermetic DIP	−55 to +125°C	AM25S10DM
Hermetic Flat-Pak	−55 to +125°C	AM25S10FM
Chip-Pak	−55 to +125°C	AM25S10LM
Dice	−55 to +125°C	AM25S10XM

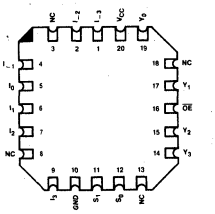
CONNECTION DIAGRAMS — Top Views

D-16, P-16



MPR-354

Leadless Chip Carrier L-20-1



Note: Pin 1 is marked for orientation.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am25S10XC T_A = 0°C to +70°C V_{CC} = 5.0 V ±5% (COM'L) MIN. = 4.75 V MAX. = 5.25 V
Am25S10XM T_A = −55°C to +125°C V_{CC} = 5.0 V ±10% (MIL) MIN. = 4.5 V MAX. = 5.5 V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	XM I_{OH} = −2mA	2.4	3.4		Volts
			XC I_{OH} = −6.5mA	2.4	3.2		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5 V				−2.0	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7 V				50	µA
I_O	Off State (High Impedance) Output Current	V_{CC} = MAX.	V_O = 2.4 V			50	µA
			V_O = 0.5 V			−50	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0 V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All outputs open, All inputs = GND			60	85	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Data Input to Output	V_{CC} = 5.0 V, C_L = 15pF, R_L = 280Ω		5	7.5	ns
t_{PHL}				8	12	
t_{PLH}	Select to Output			11	17	ns
t_{PHL}				13	20	
t_{ZH}	Output Control $\overline{OE}$ to Output				19.5	ns
t_{ZL}					21	
t_{HZ}	Output Control $\overline{OE}$ to Output	V_{CC} = 5 V, C_L = 5pF, R_L = 280Ω		5	8	ns
t_{LZ}				10	15	

DEFINITION OF FUNCTIONAL TERMS

I_i The seven data inputs of the shifter.

$\overline{OE}$ Enable. When the enable is HIGH, the four outputs are in the high impedance state. When the enable is LOW, the selected I_i inputs are present at the outputs.

S_0, S_1 Select inputs. Controls the number of places the inputs are shifted.

Y_i The four outputs of the shifter.

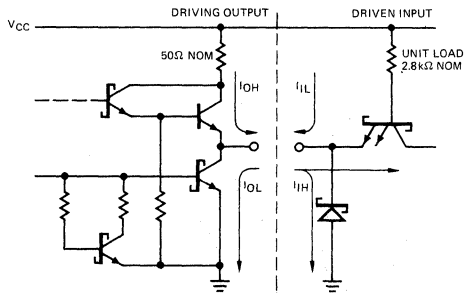
LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load (Note 1)	Fan-out Output HIGH XM	Fan-out Output HIGH XC	Fan-out Output LOW
I_{-3}	1	1	–	–	–
I_{-2}	2	1.5	–	–	–
I_{-1}	3	1.5	–	–	–
I_0	4	1.5	–	–	–
I_1	5	1.5	–	–	–
I_2	6	1.5	–	–	–
I_3	7	1	–	–	–
GND	8	–	–	–	–
S_1	9	1	–	–	–
S_0	10	1	–	–	–
Y_3	11	–	40	130	10
Y_2	12	–	40	130	10
$\overline{OE}$	13	1	–	–	–
Y_1	14	–	40	130	10
Y_0	15	–	40	130	10
V_{CC}	16	–	–	–	–

A Schottky TTL Unit Load is defined as 50 μA measured at 2.7 V HIGH and −2.0mA measured at 0.5 V LOW.

Note: 1. The fan-in on I_{-2}, I_{-1}, I_0, I_1 and I_2 will not exceed 1.5 Unit Loads when measured at V_{IL} = 0.5 V. As V_{IL} is decreased to 0 V, the input current I_{IL} MAX. increases to −4, −6, −8, −6 and −4 mA respectively due to the decrease in current sharing with the internal select buffer outputs.

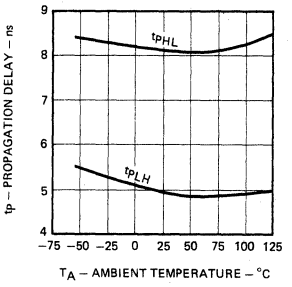
SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



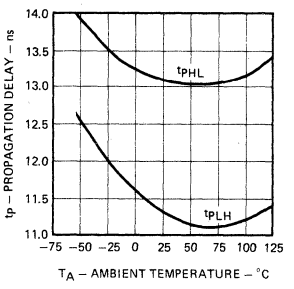
Note: Actual current flow direction shown.

PERFORMANCE CURVES
SWITCHING CHARACTERISTICS

Data to Output (Typical)



Select to Output (Typical)



LOGIC EQUATIONS

$$Y_0 = \overline{S}_0\,\overline{S}_1\,I_0 + S_0\,\overline{S}_1\,I_{-1} + \overline{S}_0\,S_1\,I_{-2} + S_0\,S_1\,I_{-3}$$
$$Y_1 = \overline{S}_0\,\overline{S}_1\,I_1 + S_0\,\overline{S}_1\,I_0 + \overline{S}_0\,S_1\,I_{-1} + S_0\,S_1\,I_{-2}$$
$$Y_2 = \overline{S}_0\,\overline{S}_1\,I_2 + S_0\,\overline{S}_1\,I_1 + \overline{S}_0\,S_1\,I_0 + S_0\,S_1\,I_{-1}$$
$$Y_3 = \overline{S}_0\,\overline{S}_1\,I_3 + S_0\,\overline{S}_1\,I_2 + \overline{S}_0\,S_1\,I_1 + S_0\,S_1\,I_0$$

Note: For additional information, see page 5-54

TRUTH TABLE

$\overline{OE}$	S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_3	Y_2	Y_1	Y_0
H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z
L	L	L	D_3	D_2	D_1	D_0	X	X	X	D_3	D_2	D_1	D_0
L	L	H	X	D_2	D_1	D_0	D_{-1}	X	X	D_2	D_1	D_0	D_{-1}
L	H	L	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_1	D_0	D_{-1}	D_{-2}
L	H	H	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_0	D_{-1}	D_{-2}	D_{-3}

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance State
D_n at input I_n may be either HIGH or LOW and output Y_m will follow the selected D_n input level.

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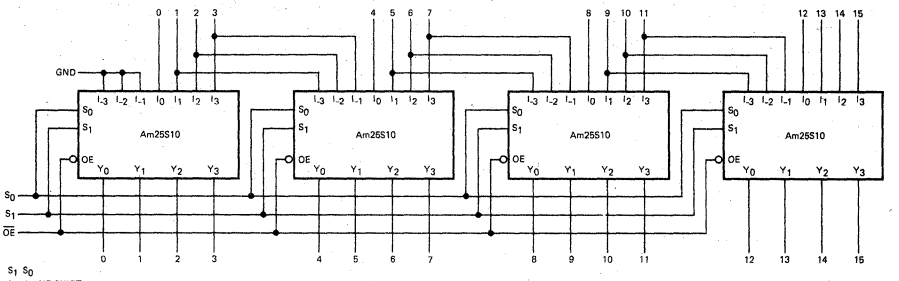
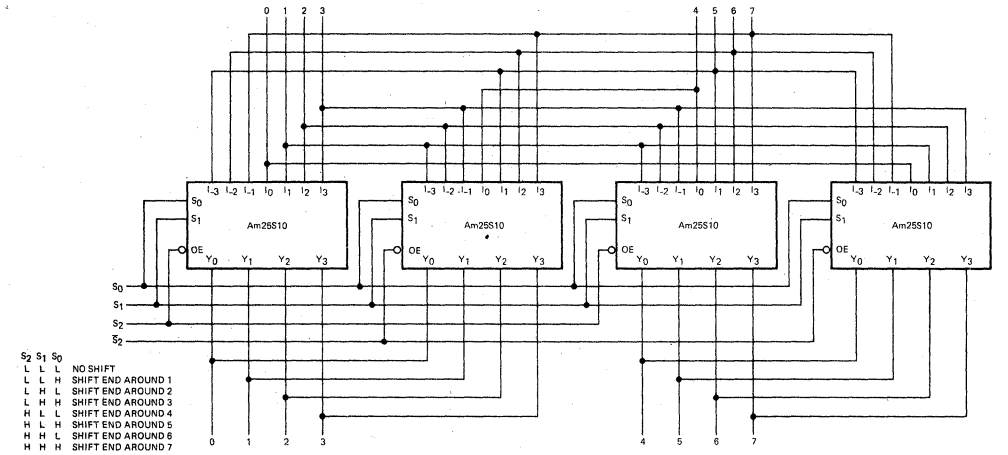
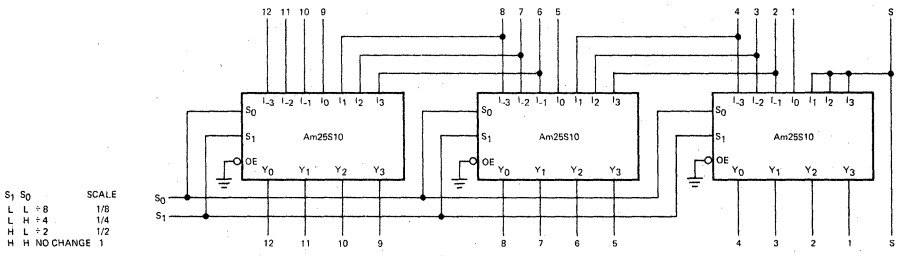
APPLICATIONS



16-Bit Shift-Up 0, 1, 2, or 3 Places

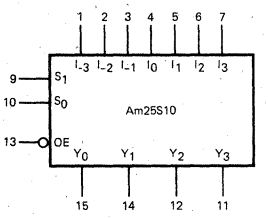


8-Bit End Around Shift 0, 1, 2, 3, 4, 5, 6, 7 Places

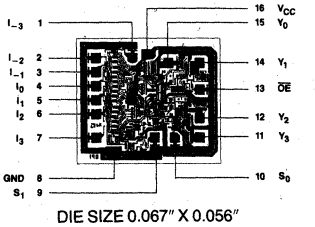


13-Bit 2's Complement Scaler

LOGIC SYMBOL



METALLIZATION AND PAD LAYOUT



Am25S10
Four-Bit Shifter

By John R. Mick

INTRODUCTION

The Am25S10 is a high-speed MSI combinatorial logic block built using advanced Schottky technology. The device has the ability to shift four bits of data 0, 1, 2 or 3 places. The Am25S10 has two select lines that are decoded internally to determine the number of places the data is shifted. The device has seven data inputs I_{-3}, I_{-2}, I_{-1}, I_0, I_1, I_2, and I_3 and 4 three-state data outputs Y_0, Y_1, Y_2, and Y_3 as shown in the logic symbol diagram of Figure 1. The three-state outputs allow several devices to be bus organized for shifts of more than three places with a single level device propagation delay time. The three-state outputs are controlled by a single buffered active-LOW output control $\overline{OE}$. When the output control is LOW, the data outputs will follow the selected data inputs. When the output control is HIGH, the data outputs offer a high-impedance to the data bus.

FUNCTIONAL DESCRIPTION

The logic equations describing the output shifting capability of the Am25S10 when the output control is LOW are:

$$Y_0 = \overline{S}_0\ \overline{S}_1\ I_0 + S_0\ \overline{S}_1\ I_{-1} + \overline{S}_0\ S_1\ I_{-2} + S_0\ S_1\ I_{-3}$$
$$Y_1 = \overline{S}_0\ \overline{S}_1\ I_1 + S_0\ \overline{S}_1\ I_0 + \overline{S}_0\ S_1\ I_{-1} + S_0\ S_1\ I_{-2}$$
$$Y_2 = \overline{S}_0\ \overline{S}_1\ I_2 + S_0\ \overline{S}_1\ I_1 + \overline{S}_0\ S_1\ I_0 + S_0\ S_1\ I_{-1}$$
$$Y_3 = \overline{S}_0\ \overline{S}_1\ I_3 + S_0\ \overline{S}_1\ I_2 + \overline{S}_0\ S_1\ I_1 + S_0\ S_1\ I_0$$

From these equations it is seen that each output is operationally equivalent to a four-input multiplexer with the inputs connected such that the select code generates successive one-bit shifts of the input data word. The logic diagram of Figure 2 shows the internal connection of each multiplexer with respect to the seven data inputs. Because of this internal connection scheme, several devices can be connected to perform shifts of 0, 1, 2, or 3 places on words of any length.

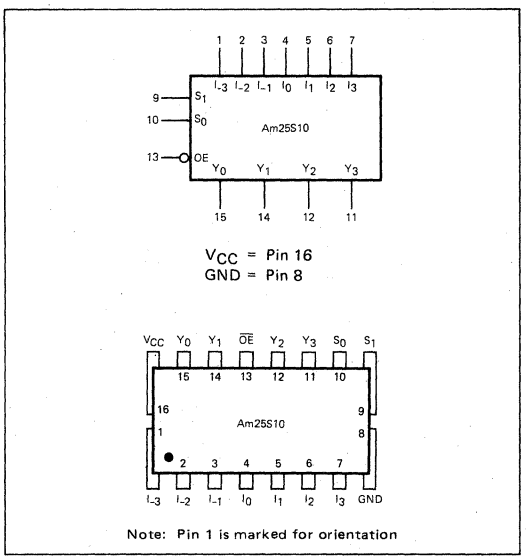


Figure 1. Logic Symbol and Connection Diagram.

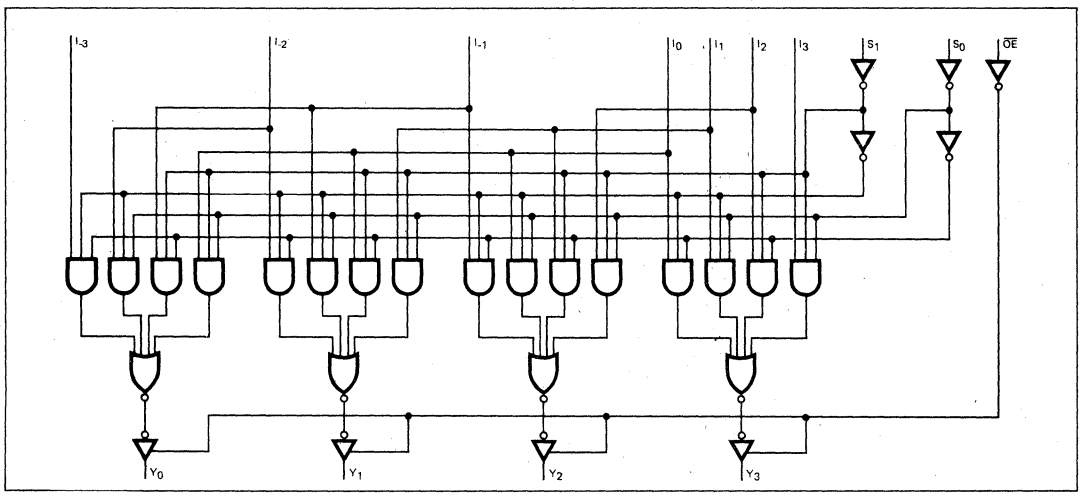


Figure 2. Logic Diagram of the Am25S10.

The operation of the Am25S10 is pictorially depicted in Figure 3. Here, the four shift positions of the data outputs with respect to the data inputs are shown via the dashed lines for the four possible select codes. Figure 4 shows a similiar operation only the notation now represents a seven-bit input word A_0 through A_6. The output code for each of the select field combinations applied to the S_0 and S_1 inputs is shown in the accompanying Function Table. In addition, the four outputs Y_0 through Y_3 can be forced to the high-impedance state by applying a HIGH to the "output control" input. This allows additional shifters to be cascaded on the same output lines, or the shifter array to be connected to a common data bus.

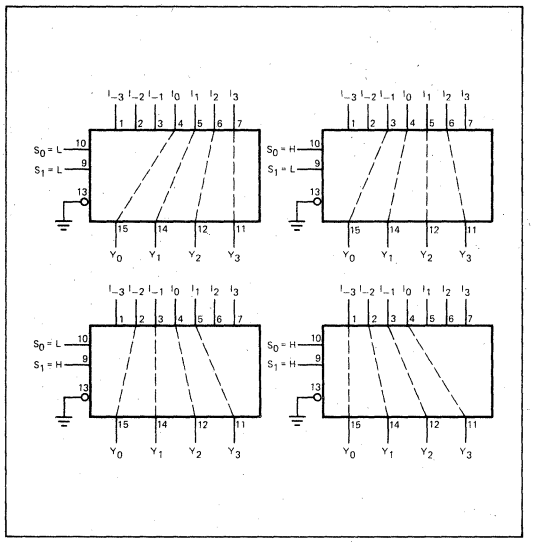
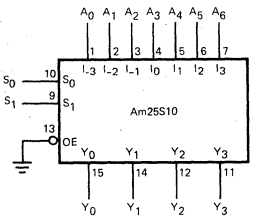


Figure 3. The Four Shift Positions of the Am25S10.



FUNCTION TABLE

S_1	S_0	Y_0	Y_1	Y_2	Y_3
0	0	A_3	A_4	A_5	A_6
0	1	A_2	A_3	A_4	A_5
1	0	A_1	A_2	A_3	A_4
1	1	A_0	A_1	A_2	A_3

Positive Logic

Figure 4. The Am25S10 4-Bit Shifter Operation.

INPUT LOADING

The logic diagram of Figure 2 shows the input connection scheme for the seven data inputs of the Am25S10. Table I shows the number of multiplexer inputs connected to each data input as well as the expected an actual Unit Load weighting on each input.

TABLE I

Pin #	Data Input	Number of Multiplexer Inputs Connected	Expected Unit Loads	Actual Unit Loads
1	I_{-3}	1	1	1
2	I_{-2}	2	2	1.5
3	I_{-1}	3	3	1.5
4	I_0	4	4	1.5
5	I_1	3	3	1.5
6	I_2	2	2	1.5
7	I_3	1	1	1

Since the number of gate inputs for I_{-2}, I_{-1}, I_0, I_1 and I_2 data inputs is 2, 3, 4, 3, and 2 respectively, this could be expected to be the unit load fan-in for these data inputs. However, I_{IL} current sharing occurs internally with the select buffer outputs to reduce the external fan-in. Since a Schottky TTL unit load is defined as −2.0mA measured at 0.5V LOW, the maximum I_{IL} when measured at V_{IL} = 0.5V is −3mA or 1.5 STTL unit loads. As the measure voltage V_{IL} on these data inputs is decreased to 0V, the measured input current on I_{-2}, I_{-1}, I_0, I_1, and I_2 can increase to an I_{IL} maximum of −4, −6, −8, −6 and −4 mA respectively because of the decrease in current sharing with the internal select buffer outputs.

A plot of the typical input voltage versus input current for the data inputs is shown in Figure 5. This Figure shows the increased input current flow (negative current) as the input voltage is decreased. It also shows the effect of the input clamp diode as forward bias in applied.

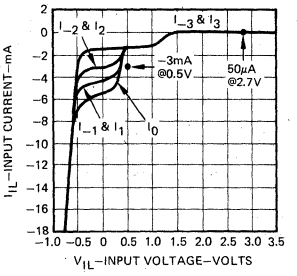
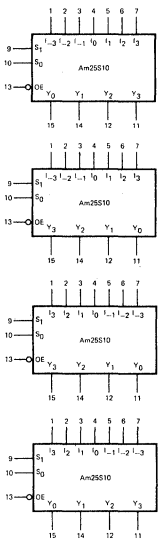


Figure 5. Typical Input Current Characteristics.

LOGIC EQUIVALENTS OF THE Am25S10

The Am25S10 exhibits several symmetrical properties that may be of advantage in some designs. These symmetrical properties involve the labeling of the inputs and outputs and the polarity of the select inputs. By relabeling the inputs in reverse order, labeling the outputs in reverse order, and considering the select inputs in positive logic (active-HIGH) or negative logic (active-LOW), eight logic equivalents for the device are possible. Figure 6 shows the operation of the device for the four combinations of input and output definitions for the positive logic notation while Figure 7 shows the operation of the device for the four combinations for the negative logic notation. The logic symbol for each set of definitions for the input pins and output pins is shown adjacent to the truth table.

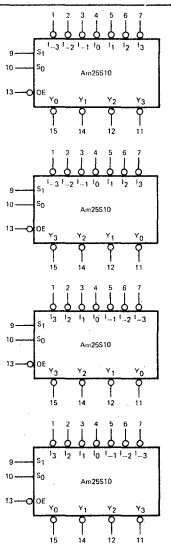
This relabeling of pins can provide the designer with some flexibility in printed circuit board layout. Likewise, the select code can be either positive logic or negative logic and the input data will be passed non-inverted. In some cases, the redefinition allows the designer to visualize shifting up versus shifting down for the same select code.



SELECT PINS		DATA INPUT PINS							DATA OUTPUT PINS			
9	10	1	2	3	4	5	6	7	11	12	14	15
S_1	S_0	I_{-3}	I_{-2}	I_{-1}	I_0	I_1	I_2	I_3	Y_3	Y_2	Y_1	Y_0
0	0	X	X	X	D_0	D_1	D_2	D_3	D_3	D_2	D_1	D_0
0	1	X	X	D_{-1}	D_0	D_1	D_2	X	D_2	D_1	D_0	D_{-1}
1	0	X	D_{-2}	D_{-1}	D_0	D_1	X	X	D_1	D_0	D_{-1}	D_{-2}
1	1	D_{-3}	D_{-2}	D_{-1}	D_0	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}
S_1	S_0	I_{-3}	I_{-2}	I_{-1}	I_0	I_1	I_2	I_3	Y_0	Y_1	Y_2	Y_3
0	0	X	X	X	D_0	D_1	D_2	D_3	D_3	D_2	D_1	D_0
0	1	X	X	D_{-1}	D_0	D_1	D_2	X	D_2	D_1	D_0	D_{-1}
1	0	X	D_{-2}	D_{-1}	D_0	D_1	X	X	D_1	D_0	D_{-1}	D_{-2}
1	1	D_{-3}	D_{-2}	D_{-1}	D_0	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}
S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_0	Y_1	Y_2	Y_3
0	0	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_{-3}	D_{-2}	D_{-1}	D_0
0	1	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_{-2}	D_{-1}	D_0	D_1
1	0	X	D_2	D_1	D_0	D_{-1}	X	X	D_{-1}	D_0	D_1	D_2
1	1	D_3	D_2	D_1	D_0	X	X	X	D_0	D_1	D_2	D_3
S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_3	Y_2	Y_1	Y_0
0	0	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_{-3}	D_{-2}	D_{-1}	D_0
0	1	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_{-2}	D_{-1}	D_0	D_1
1	0	X	D_2	D_1	D_0	D_{-1}	X	X	D_{-1}	D_0	D_1	D_2
1	1	D_3	D_2	D_1	D_0	X	X	X	D_0	D_1	D_2	D_3

Positive Logic (HIGH = 1, LOW = 0) for the select inputs.

Figure 6. Four Possible Input and Output Combinations for the Positive Logic Definition.



SELECT PINS		DATA INPUT PINS							DATA OUTPUT PINS			
9	10	1	2	3	4	5	6	7	11	12	14	15
S_1	S_0	I_{-3}	I_{-2}	I_{-1}	I_0	I_1	I_2	I_3	Y_3	Y_2	Y_1	Y_0
0	0	D_{-3}	D_{-2}	D_{-1}	D_0	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}
0	1	X	D_{-2}	D_{-1}	D_0	D_1	X	X	D_1	D_0	D_{-1}	D_{-2}
1	0	X	X	D_{-1}	D_0	D_1	D_2	X	D_2	D_1	D_0	D_{-1}
1	1	X	X	X	D_0	D_1	D_2	D_3	D_3	D_2	D_1	D_0
S_1	S_0	I_{-3}	I_{-2}	I_{-1}	I_0	I_1	I_2	I_3	Y_0	Y_1	Y_2	Y_3
0	0	D_{-3}	D_{-2}	D_{-1}	D_0	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}
0	1	X	D_{-2}	D_{-1}	D_0	D_1	X	X	D_1	D_0	D_{-1}	D_{-2}
1	0	X	X	D_{-1}	D_0	D_1	D_2	X	D_2	D_1	D_0	D_{-1}
1	1	X	X	X	D_0	D_1	D_2	D_3	D_3	D_2	D_1	D_0
S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_0	Y_1	Y_2	Y_3
0	0	D_3	D_2	D_1	D_0	X	X	X	D_0	D_1	D_2	D_3
0	1	X	D_2	D_1	D_0	D_{-1}	X	X	D_{-1}	D_0	D_1	D_2
1	0	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_{-2}	D_{-1}	D_0	D_1
1	1	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_{-3}	D_{-2}	D_{-1}	D_0
S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_3	Y_2	Y_1	Y_0
0	0	D_3	D_2	D_1	D_0	X	X	X	D_0	D_1	D_2	D_3
0	1	X	D_2	D_1	D_0	D_{-1}	X	X	D_{-1}	D_0	D_1	D_2
1	0	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_{-2}	D_{-1}	D_0	D_1
1	1	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_{-3}	D_{-2}	D_{-1}	D_0

Negative Logic (LOW = 1, HIGH = 0) for the select inputs.

Figure 7. Four Possible Input and Output Combinations for the Negative Logic Definition.

Am25S10 APPLICATIONS

The four-bit shifter is an ideal MSI element for high-speed shifting and scaling in digital systems. By suitable interconnection of the inputs and outputs, shifts of any number of places up or down can be made with a propagation delay of only one device. Shifting can be logical, with zeroes pulled in at either or both ends of the shifting field; arithmetic, where the sign bit is repeated during a shift down; or end around, where the data word forms a continuous loop. The three-state outputs can be used to increase the number of places shifted and also facilitate rapid data bus access in bus organized systems.

The Connection Diagram and Function Table of Figure 8 show a 16-bit word shifted up 0, 1, 2 or 3 places. In this example, the most significant bits (A_{13}, A_{14}, A_{15}) are discarded and logic zeroes are shifted in at the least significant end.

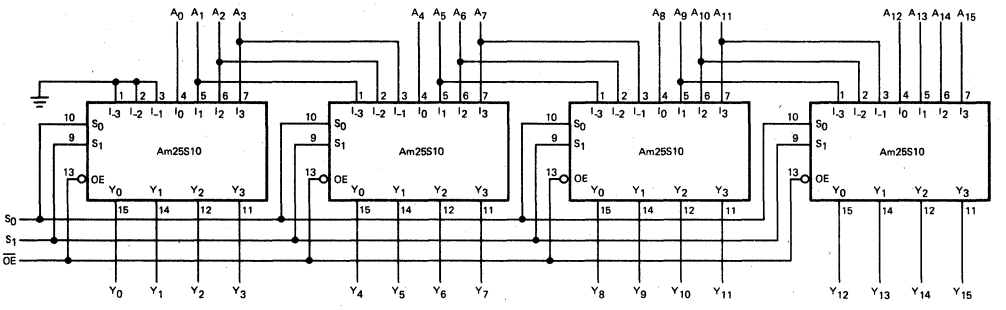
Figure 9 shows a Connection Diagram and Function Table for a 12-bit word shifted down 0, 1, 2 or 3 places. In this example, zeroes are shifted into the most significant bits and the least significant bits are discarded. Notice that one of the alternate definitions and pin assignments has been used to define the Am25S10.

A complete end-around barrel shift of 0, 1, 2, 3, 4, 5, 6 or 7 places is shown in Figure 10. In this configuration, the three-state capability of the outputs is used to connect one of two Am25S10's to the data output under the control of the S_2 and $\overline{S}_2$ select inputs. This technique can be expanded for longer word lengths by using one-of-four or one-of-eight decoders to control the active-LOW "output control" input.

A 13-bit two's complement scaler is shown in Figure 11. For this connection, the sign bit is pulled in at the most significant end and the least significant bits are truncated. Thus, the 13-bit two's complement binary output number is scaled to 1, 1/2, 1/4, or 1/8 of its input value.

A two-level 16-bit barrel shifter and its associated Function Table are shown in Figure 12. Only eight Am25S10's are required to perform this function. For clarity, the intermediate level of inputs and outputs have been labeled B_i. The sixteen-bit output word can be bus connected and controlled via the $\overline{OE}$ input.

Figure 13 demonstrates a unique way to convert a fixed point positive number to a floating-point mantissa and exponent. The priority encoder is used to determine the most significant bit position of the input word with a binary "1". The priority encoder output is a binary weighted code representing the number of places the input word is to be shifted up. This code controls the Am25S10 shifting array and shifts the input word such that the Y_7-bit of the mantisa is always a binary one (except for A = 0). The exponent is of the form 2^{-n} where n is the value of the binary weighted code from the priority encoder. Thus, the output of this functional block is of the form $Y2^{-n}$.

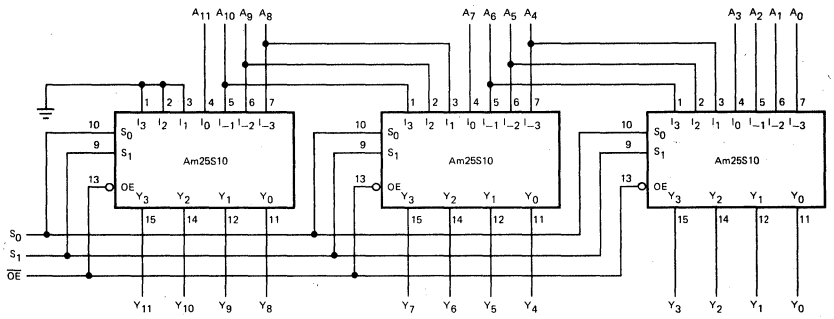


FUNCTION TABLE

S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9	Y_{10}	Y_{11}	Y_{12}	Y_{13}	Y_{14}	Y_{15}
0	0	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}
0	1	0	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}
1	0	0	0	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}
1	1	0	0	0	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}

Positive Logic

Figure 8. 16-Bit Shift-Up 0, 1, 2 or 3 Places.

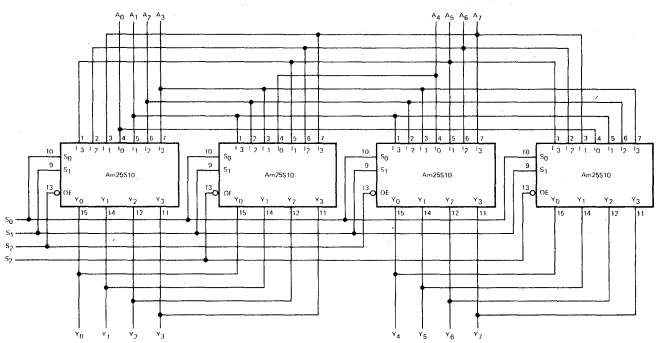


FUNCTION TABLE

S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9	Y_{10}	Y_{11}
0	0	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}
0	1	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	0
1	0	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	0	0
1	1	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	0	0	0

Positive Logic (Alternate Definitions)

Figure 9. 12-Bit Shift-Down 0, 1, 2 or 3 Places.

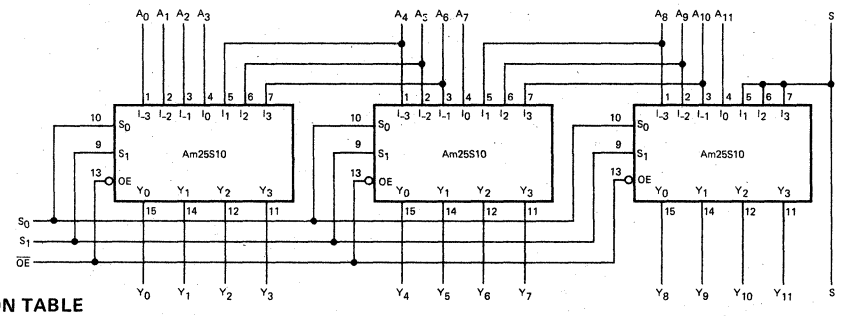


FUNCTION TABLE

S_2	S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
0	0	0	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7
0	0	1	A_7	A_0	A_1	A_2	A_3	A_4	A_5	A_6
0	1	0	A_6	A_7	A_0	A_1	A_2	A_3	A_4	A_5
0	1	1	A_5	A_6	A_7	A_0	A_1	A_2	A_3	A_4
1	0	0	A_4	A_5	A_6	A_7	A_0	A_1	A_2	A_3
1	0	1	A_3	A_4	A_5	A_6	A_7	A_0	A_1	A_2
1	1	0	A_2	A_3	A_4	A_5	A_6	A_7	A_0	A_1
1	1	1	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_0

Positive Logic

Figure 10. Eight-Bit End Around Shift 0, 1, 2, 3, 4, 5, 6 or 7 Places.

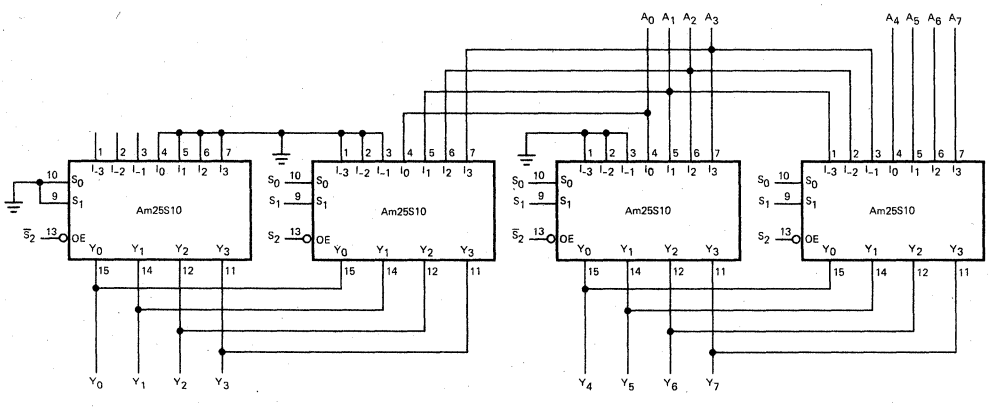


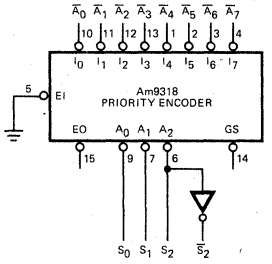
FUNCTION TABLE

SCALE	S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9	Y_{10}	Y_{11}	S
1/8	0	0	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	S	S	S	S
1/4	0	1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	S	S	S
1/2	1	0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	S	S
1	1	1	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	S

Positive Logic

Figure 11. 13-Bit 2's Complement Scaler.



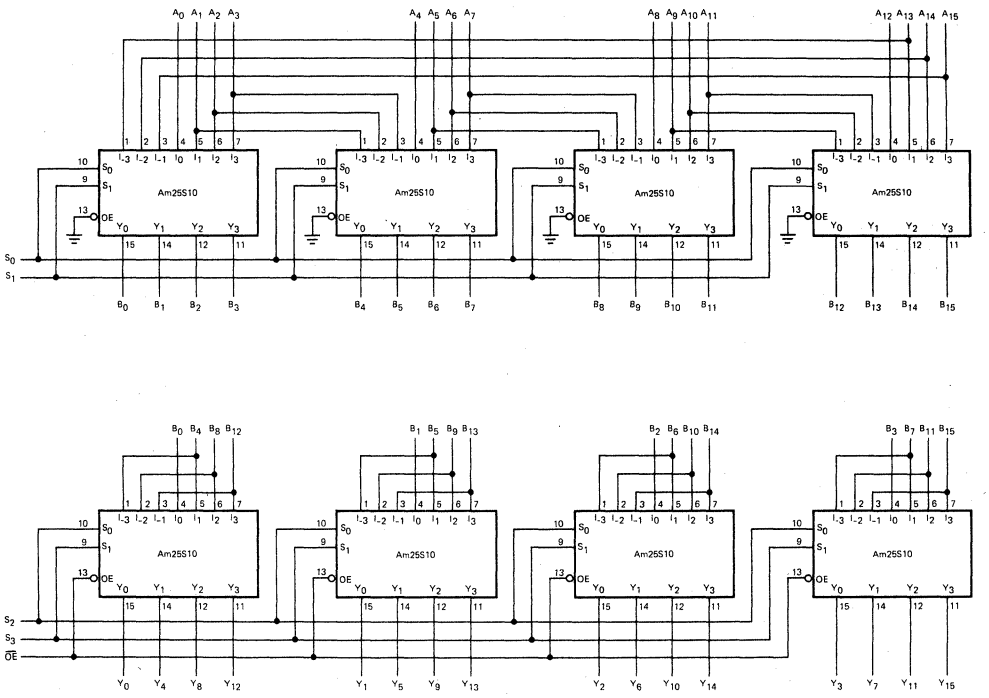


FUNCTION TABLE

EXPONENT			MANTISSA							
S_2	S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
0	0	0	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7
0	0	1	0	A_0	A_1	A_2	A_3	A_4	A_5	A_6
0	1	0	0	0	A_0	A_1	A_2	A_3	A_4	A_5
0	1	1	0	0	0	A_0	A_1	A_2	A_3	A_4
1	0	0	0	0	0	0	A_0	A_1	A_2	A_3
1	0	1	0	0	0	0	0	A_0	A_1	A_2
1	1	0	0	0	0	0	0	0	A_0	A_1
1	1	1	0	0	0	0	0	0	0	A_0

Positive Logic

Figure 13. Binary Scaling to Give Mantissa and Exponent.



FUNCTION TABLE

S_3	S_2	S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9	Y_{10}	Y_{11}	Y_{12}	Y_{13}	Y_{14}	Y_{15}
0	0	0	0	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}
0	0	0	1	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}
0	0	1	0	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}
0	0	1	1	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}
0	1	0	0	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}
0	1	0	1	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}
0	1	1	0	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9
0	1	1	1	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8
1	0	0	0	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7
1	0	0	1	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5	A_6
1	0	1	0	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5
1	0	1	1	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4
1	1	0	0	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3
1	1	0	1	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2
1	1	1	0	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1
1	1	1	1	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0

Positive Logic

Figure 12. Full 16-Bit Barrel Shifter.

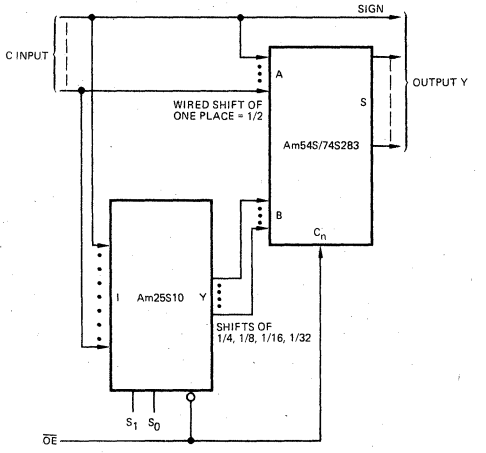
FIXED MULTIPLIERS

Digital systems requiring multiplication by a constant interger or constant fraction can make effective use of the Am25S10 if the constant must be varied over several values. By using four-bit shifters and high-speed adders, very high-speed "constant coefficient" or fixed multipliers can be built. The technique is shown diagrammatically in Figure 14. Here, the input word C is wired to the adder A inputs such that a shift of $\frac{1}{2}$ C is "built-in". The Am25S10 shifter is wired to the B inputs of the adder such that its four select states represent prescaling of $\frac{1}{4}$C, $\frac{1}{8}$C, $\frac{1}{16}$C, and $\frac{1}{32}$C of the C input word. If the $\overline{OE}$ input is used to disable the outputs (high impedance), the adder B inputs will assume the logical one state (HIGH). By adding a "one" at the adder carry input least significant end, the contribution of the B inputs to the sum output is zero and the adder A input will be passed to the output. Thus, the $\overline{OE}$ input can be used to generate a zero C value from the shifter.

Figure 15 shows the actual connection diagram for a 12-bit two's complement fixed multiplier using the scheme of Figure 14. The Y output weighting is the same as shown in the Function Table of Figure 14. The $\overline{OE}$ input is tied directly to the adder least significant C_n input to complete the shifter "zero" output function.

Figure 16 shows two shifter arrays used in conjunction with one adder. For the shifter A and shifter B select codes shown, twenty multiplication constants are realized with seventeen constants being unique. Other combinations could be used to realize different outputs. The combinations possible can be extended greatly by using multiple adders and multiple shifting arrays. For the example of Figure 16, the zero shifter output (high-impedance state) is used with only one shifter since only one C_n input is available.

This technique for fixed constant multipliers can be applied to two's complement, one's complement, sign-magnitude, or magnitude only arithmetic. In so doing, the sign must be handled appropriately and the adder output word size and number range must be considered. For the one's complement case, the all ones representation for zero must be handled separately.



FUNCTION TABLE

			4-BIT SHIFTER		A INPUT OF ADDER	OUTPUT Y
$\overline{OE}$	S_1	S_0	#SHIFTS	B INPUT OF ADDER		
0	0	0	Two	$\frac{1}{4}$C	$\frac{1}{2}$C	$\frac{3}{4}$C
0	0	1	Three	$\frac{1}{8}$C	$\frac{1}{2}$C	$\frac{5}{8}$C
0	1	0	Four	$\frac{1}{16}$C	$\frac{1}{2}$C	$\frac{9}{16}$C
0	1	1	Five	$\frac{1}{32}$C	$\frac{1}{2}$C	$\frac{17}{32}$C
1	X	X	Hi-Z	0C	$\frac{1}{2}$C	$\frac{1}{2}$C

Positive Logic

Figure 14. Parallel "Constant Coefficient" Multiplier Block Diagram and Function Table.

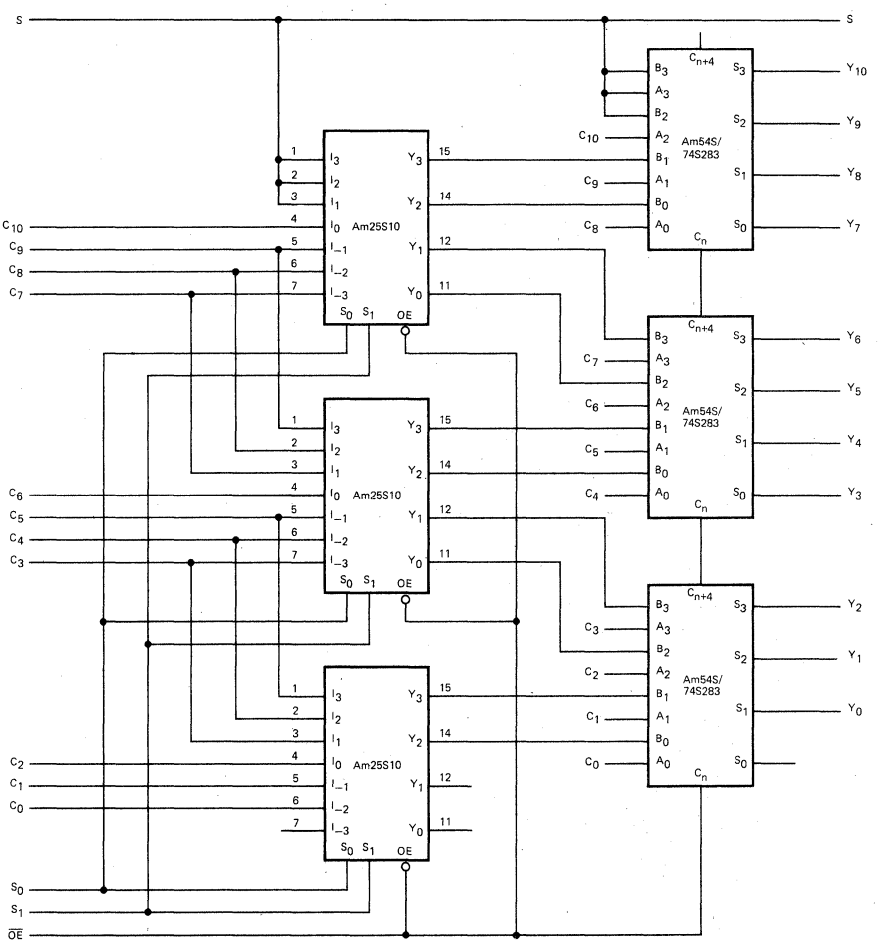
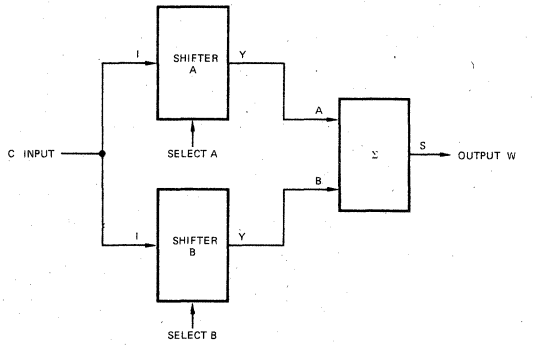


Figure 15. 12-Bit 2's Complement "Constant Coefficient" Multiplier.



SHIFTER A = $C, \frac{C}{2}, \frac{C}{4}, \frac{C}{8}$

SHIFTER B = $\frac{C}{4}, \frac{C}{8}, \frac{C}{16}, \frac{C}{32}, 0$

FIXED MULTIPLIER OUTPUT W

SHIFTER A \ SHIFTER B	$\frac{C}{4}$	$\frac{C}{8}$	$\frac{C}{16}$	$\frac{C}{32}$	0
C	$\frac{5}{4}C$	$\frac{9}{8}C$	$\frac{17}{16}C$	$\frac{33}{32}C$	C
$\frac{C}{2}$	$\frac{3}{4}C$	$\frac{5}{8}C$	$\frac{9}{16}C$	$\frac{17}{32}C$	$\frac{1}{2}C$
$\frac{C}{4}$	$\frac{1}{2}C$	$\frac{3}{8}C$	$\frac{5}{16}C$	$\frac{9}{32}C$	$\frac{1}{4}C$
$\frac{C}{8}$	$\frac{3}{8}C$	$\frac{1}{4}C$	$\frac{3}{16}C$	$\frac{5}{32}C$	$\frac{1}{8}C$

Figure 16. Two Shifter Arrays and One Adder Array in a Fixed Multiplier Connection.

CONCLUSION

The Am25S10 four-bit shifter is a new unique combinatorial logic element offering the system designer new shifting and scaling capability not previously available in a single package. The three-state output design of the Am25S10 provides increased flexibility in its use and the advanced Schottky construction offers minimum propagation delay. The device can be used to shift any number of bits any number of places; up, down or end-around.

Am25LS14A

8-Bit Serial/Parallel Two's Complement Multiplier

DISTINCTIVE CHARACTERISTICS

- Two's complement multiplication without correction
- Magnitude only multiplication
- Cascadable for any number of bits
- 8-bit parallel multiplicand data input
- 50MHz minimum clock frequency
- Second sourced by T.I. as the SN54LS/74LS384
- IMOX™ process with ECL internal

FUNCTIONAL DESCRIPTION

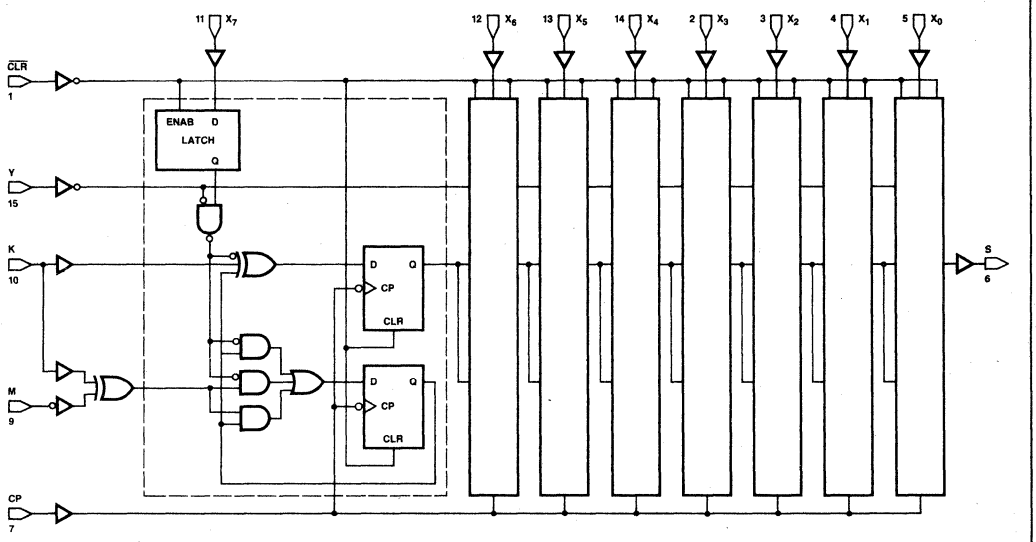
The Am25LS14A is an 8-bit by 1-bit sequential logic element that performs digital multiplication of two numbers represented in two's complement form to produce a two's complement product without correction. The device accepts an 8-bit multiplicand (X input) and stores this data in eight internal latches. The X latches are controlled via the clear input. When the clear input is LOW, all internal flip-flops are cleared and the X latches are opened to accept new multiplicand data. When the clear input is HIGH, the latches are closed and are insensitive to X input changes.

The multiplier word data is passed by the Y input in a serial bit stream – least significant bit first. The product is clocked out the S output least significant bit first.

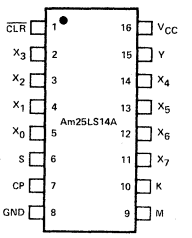
The multiplication of an m-bit multiplicand by an n-bit multiplier results in an m + n bit product. The Am25LS14A must be clocked for m + n clock cycles to produce this two's complement product. Likewise, the n-bit multiplier (Y-input) sign bit data must be extended for the remaining m-bits to complete the multiplication cycle.

The device also contains a K input so that devices can be cascaded for longer length X words. The sum (S) output of one device is connected to the K input of the succeeding device when cascading. Likewise, a mode input (M) is used to indicate which device contains the most significant bit. The mode input is wired HIGH or LOW depending on the position of the 8-bit slice in the total X word length.

LOGIC DIAGRAM



CONNECTION DIAGRAM – Top View



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0 to +70°C	AM25LS14APC
Hermetic DIP	0 to +70°C	AM25LS14ADC
Dice	0 to +70°C	AM25LS14AXC
Hermetic DIP	−55 to +125°C	AM25LS14ADM
Hermetic Flat Pak	−55 to +125°C	AM25LS14AFM
Dice	−55 to +125°C	AM25LS14AXM

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Am25LS14A

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am25LS14AXC	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5% (COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am25LS14AXM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10% (MIL)	MIN. = 4.5V	MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1.0mA, V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8.0mA			0.4	Volts
			I_{OL} = 12mA			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	X, M			−0.48	mA
			K, $\overline{CLR}$			−1.2	
			CP			−1.6	
			Y			−3.2	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	X, M			20	µA
			K, $\overline{CLR}$			30	
			CP			40	
			Y			80	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.			45	65	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Duration of the short circuit test should not exceed one second.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Output		8	14	ns	C_L = 15pF R_L = 2.0kΩ
t_{PHL}			10	18		
t_{PHL}	Clear to Output		9	17	ns	
t_s	Y to Clock	15			ns	
t_h		0				
t_s	K to Clock	15			ns	
t_h		0				
t_s	X_i to Clear	13			ns	
t_h		0				
t_{pw}	Clock (HIGH)	10			ns	
	Clock (LOW)	10				
t_{pw}	Clear Pulse Width	10			ns	
t_s	Clear Recovery Time (Inactive State)	5			ns	
f_{max} (Note 1)	Maximum Clock Frequency	50	60		MHz	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ± 5%		Am25LS MIL T_A = –55°C to +125°C V_{CC} = 5.0V ± 10%		Units	Test Conditions
		Min.	Max.	Min.	Max.		
t_{PLH}	Clock to Output		18		20	ns	C_L = 50pF R_L = 2.0kΩ
t_{PHL}			22		25		
t_{PHL}	Clear to Output		22		25	ns	
t_s	Y to Clock	22		25		ns	
t_h		0		0			
t_s	K to Clock	20		22		ns	
t_h		0		0			
t_s	X_i to Clear	20		22		ns	
t_h		0		0			
t_{pw}	Clock (HIGH)	10		10		ns	
	Clock (LOW)	10		10			
t_{pw}	Clear Pulse Width	10		10		ns	
t_s	Clear Recovery Time (Inactive State)	5		5		ns	
f_{max} (Note 1)	Maximum Clock Frequency	50		50		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

X_0, X_1, X_2, X_3, X_4, X_5, X_6, X_7 The eight data inputs for the multiplicand (X) data.

Y The serial input for the multiplier (Y) data—least significant bit first.

S The serial output for the product of X • Y—least significant bit first.

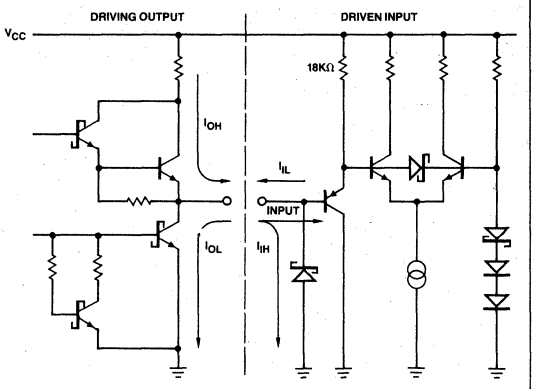
CP Clock. The buffered common clock input for the serial/parallel multiplier. All functions occur on the LOW-to-HIGH transition of the clock.

CLR Clear. The buffered common clear for all flip-flops within the device. When the clear is LOW all flip-flops are cleared. Also the buffered X-input latch enable. When the clear input is LOW, the X latches will accept new X-input data.

K The sum expansion input to the serial/parallel multiplier. Allows for cascading devices.

M The mode control input for the most significant bit of the multiplier. It is used in conjunction with cascading to determine the most significant bit.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



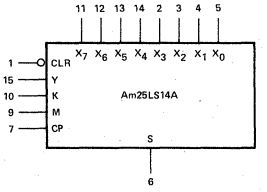
Note: Actual current flow direction shown.

FUNCTION TABLE

INPUTS						INTERNAL	OUTPUT	FUNCTION
$\overline{CLR}$	CP	K	M	X_i	Y	Y_{-1}	S	
–	–	L	L	–	–	–	–	Most Significant Multiplier Device
–	–	CS	H	–	–	–	–	Devices Cascaded in Multiplier String
L	–	–	–	OP	–	L	L	Load New Multiplicand and Clear Internal Sum and Carry Registers
H	–	–	–	–	–	–	–	Device Enabled
H	↑	–	–	–	L	L	AR	Shift Sum Register
H	↑	–	–	–	L	H	AR	Add Multiplicand to Sum Register and Shift
H	↑	–	–	–	H	L	AR	Subtract Multiplicand from Sum Register and Shift
H	↑	–	–	–	H	H	AR	Shift Sum Register

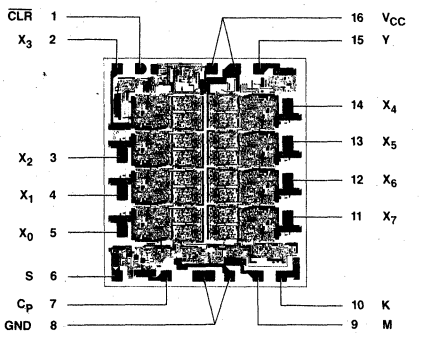
H = HIGH
L = LOW
↑ = LOW-to-HIGH transition
CS = Connected to S output of higher order device
OP = X_i latches open for new data (i = 0, 7)
AR = Output as required.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

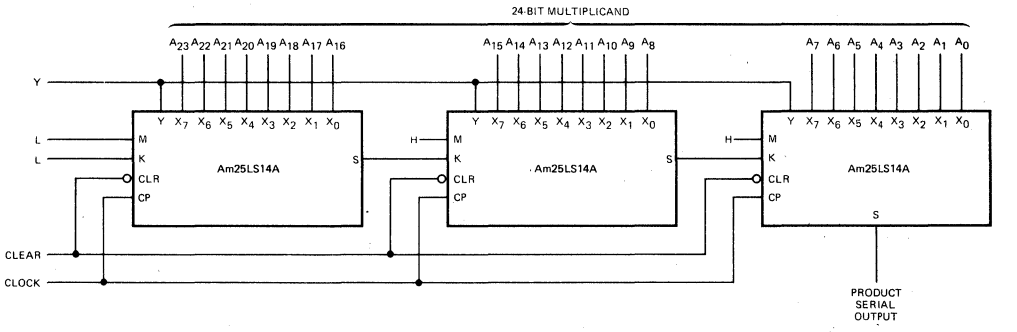
METALLIZATION AND PAD LAYOUT



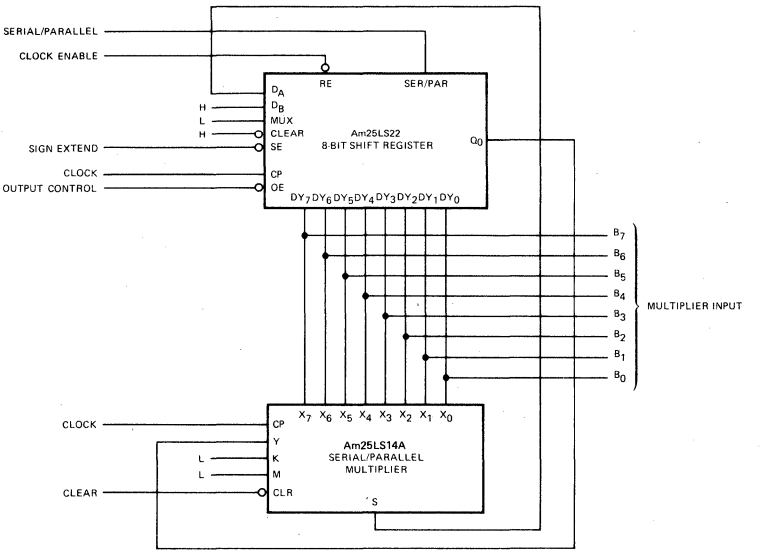
DIE SIZE 0.084" X 0.095"

APPLICATIONS

See also Digital Signal Processing Applications Section for more information.

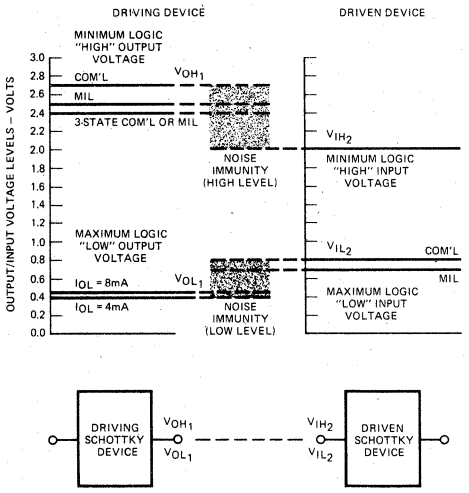


Basic 24-Bit Serial/Parallel Connection MPR-817



8-Bit by 8-Bit Multiplier, Bus Organized, with 8-Bit Truncated Product MPR-818

LOW CURRENT SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Refer to Electrical Characteristics for measure currents.

DEFINITION OF STANDARD TERMS

H HIGH, applying to a HIGH voltage level.

L LOW, applying to a LOW voltage level.

I Input.

O Output.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

I_{IL} LOW-level input current with a specified LOW-level voltage applied.

I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.

I_{OL} LOW-level output current.

I_{OH} HIGH-level output current.

I_{SC} Output short-circuit source current.

I_{CC} The supply current drawn by the device from the V_{CC} power supply.

V_{IL} Logic LOW input voltage.

V_{IH} Logic HIGH input voltage.

V_{OL} LOW-level output voltage with I_{OL} applied.

V_{OH} HIGH-level output voltage with I_{OH} applied.

A High-Speed Serial/Parallel Multiplier The Am25LS14A*

By John Mick, John Springer and Clive Ghest

INTRODUCTION

The Am25LS14A is a complete 8-bit Serial/Parallel Multiplier fabricated as a single 16-pin LSI chip. The device accepts a parallel two's complement or unsigned multiplicand and multiplies it by any arbitrary length serial two's complement or unsigned multiplier. The resulting product is a correct and complete serial two's complement or unsigned product. The complete product of an 8 x 8 multiplication can be performed in 16 clock cycles. Any number of Am25LS14A devices can be cascaded with no additional logic, so that the parallel multiplicand can be easily expanded to any number of bits. Mixed signed (two's complement) and unsigned multiplication is possible, generating a product in signed two's-complement form.

MULTIPLIER CHARACTERISTICS

The requirements for a good general purpose IC multiplier for use in a wide range of commercial applications are as follows:

- It should be inexpensive
- It should be fast
- It should be easy to use
- It should be adaptable to any word length
- It should handle signed numbers in two's complement notation without correction.

The first two of these requirements tend to be incompatible and in the past have required two types of circuits: one which was designed to be as fast as possible and another which compromised speed for cost. The last two requirements limit the method used to perform the multiplication to an algorithm which works in two's complement notation and is the same for all bits, so that the "sign bit" is treated identically with the other bits.

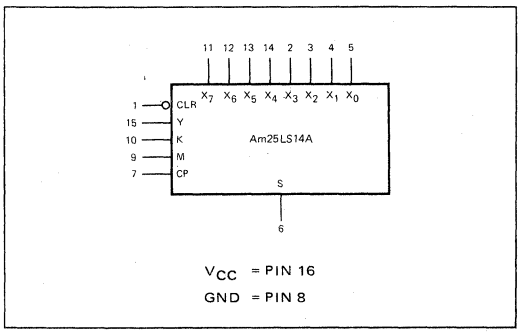


Figure 2. Logic Symbol for the Am25LS14A (16-Pin Device)

The Am25LS14A offers an optimum solution to these requirements. It operates by taking the whole multiplicand in parallel and utilizing a single bit at a time of the multiplier word to form partial products in an internal register. The output is a serial bit stream representing the product of the parallel multiplicand word and the serial multiplier word.

THE LOGIC FUNCTION

A simplified logic diagram of the Am25LS14A Serial/Parallel multiplier is shown in Figure 1 and the 16-pin logic symbol for the device is shown in Figure 2. The multiplier consists of four basic parts; a storage register used to hold the multiplicand word during the multiplication, the adder/subtractor logic containing both a partial product register and a carry/borrow register, a flip-flop and exclusive-NOR gate operating on the serial multiplier string presented at the Y input to provide a

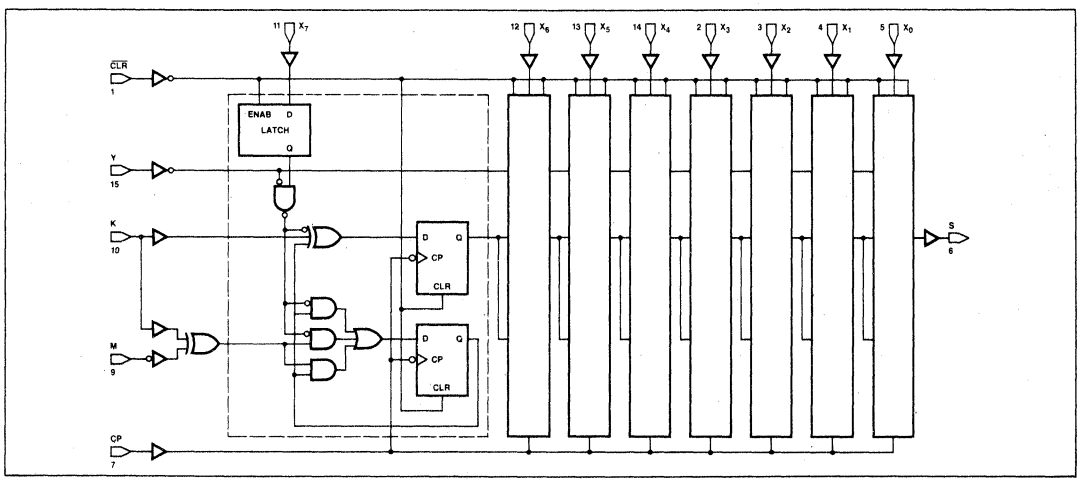


Figure 1. Functional Logic Diagram for the Am25LS14A

*The Am25LS14A is manufactured under U.S. Patent No. 3,878,985 issued April 22, 1975.

control signal to the adder/subtractor logic, and a logic mode circuit to alter the multiplicand from two's complement to unsigned notation as controlled by the M input. The adder/subtractor logic and product and carry/borrow register is iterative; that is, it consists of eight identical cells with a small change in the eighth cell to efficiently incorporate the multiplicand word sign logic. For a detailed description of the logic design of the Serial/Parallel multiplier, refer to the application note "Mechanization of the Serial/Parallel Multiplier" by John R. Mick.

Prior to a multiplication, the internal multiplier sum and carry registers are reset by applying a LOW to the clear input. The 8-bit multiplicand data is applied to the X inputs and is latched into the multiplicand register as the clear input goes HIGH. This internal multiplicand storage is useful because the multiplicand need not be held constant during the multiplication allowing these inputs to be bus organized. The Serial/Parallel multiplier is now ready to receive the first least significant multiplier bit. The least significant bit of the multiplier word is presented at the Y serial input and when the clock changes from LOW to HIGH, the multiplier produces the first least significant product bit at the serial data output, S. In each succeeding clock period, the next more significant multiplier bit is presented at the Y input and the next more significant product bit is present at the S output. After 8 clock periods, the multiplier serial input string has been exhausted but the most significant half of the product is still in the internal registers of the Am25LS14A Serial/Parallel multiplier and must be clocked out. If the multiplier is an unsigned word, then during the extraction of the most significant half of the product, the multiplier Y input must be held at logic zero. If, however, the multiplier is a two's-complement signed word, then the most significant bit (sign bit) of the multiplier word must be repeated at the Y input until the complete product has been obtained. The multiplicand can be either an unsigned number or a two's-complement number depending upon the logic polarity of the mode input, M. This mode input should be held at a LOW logic level (ground) if the multiplicand is in two's-complement notation and the X_7 input is a two's complement sign bit, and it should be held at a HIGH logic level (pulled up through a register to V_{CC}) if the 8-bit multiplicand is unsigned (magnitude only number).

The K input is used for expansion purposes. To increase the length of the multiplicand word by using multiple devices, the S output of a higher order device is connected to the K input of the next lower order devices. The clear lines are connected together and the clock lines are connected together. All the mode inputs except the one on the most significant device are held at a HIGH logic level. Whether the multiplicand is signed or unsigned is determined only by the M input of the most significant device. A 24-bit by n-bit multiplier is shown in Figure 3. The K input is held LOW at the most significant device indicating a two's complement multiplicand. The multiplier input can be any length, with n + 24 clock periods required for the multiplication. The resulting product is n + 24 bits long.

If the multiplicand is not an even multiple of 8 bits, then for an unsigned multiplicand the remaining most significant multiplicand inputs are held LOW at logic zero, while for a two's-complement multiplicand, the remaining multiplicand inputs must be connected to the multiplicand sign bit so that the sign is extended and can be interpreted correctly. Figure 4 shows a 12 x n Serial/Parallel multiplier connection for a two's-complement signed multiplicand. The resulting product is n + 12 bits long and only n + 12 clock periods are required to generate the correct product.

The Function Table for the Am25LS14A multiplier operation is given in Figure 5. As shown, the K input is the sum expansion input and allows for the cascading of devices. The mode input, M, is used in conjuction with cascading to determine the most significant bit of the multiplicand and controls the multiplicand sign definition.

TIMING

Although the Serial/Parallel multiplier requires only m + n clock periods to produce a full length product, (where m is the multiplicand word length and n is the multiplier word length) a practical system may use two additional clock periods. The first additional clock period is used to reset the multiplier at the beginning of a multiplication by using the clear input. This is shown in the timing diagram of Figure 6. This clears the partial product register, the carry/borrow register and the

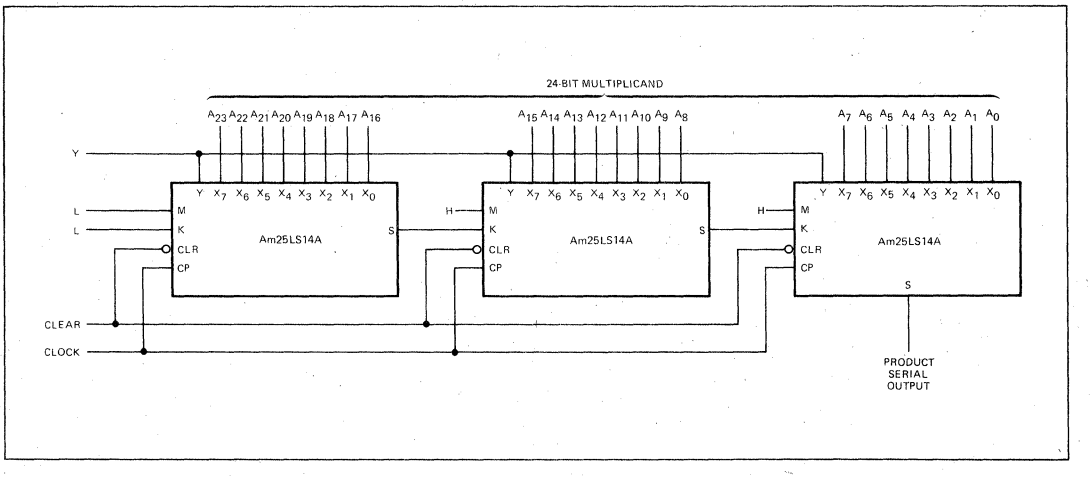


Figure 3. Three Am25LS14A's Cascaded to Make a 1-Bit by 24-Bit Serial-Parallel Multiplier

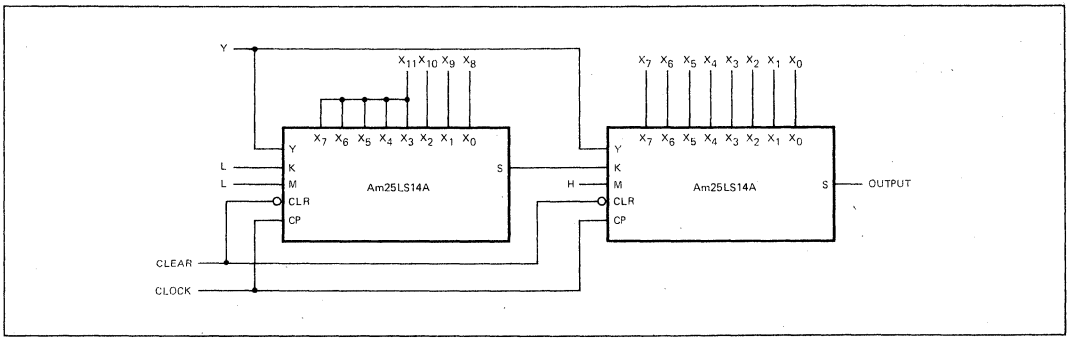


Figure 4. A 12-Bit by N-Bit Two's Complement Multiplier Using Two Am25LS14A's.

INPUTS						INTERNAL	OUTPUT	FUNCTION
$\overline{CLR}$	CP	K	M	X_i	Y	Y_{-1}	S	
–	–	L	L	–	–	–	–	Most Significant Multiplier Device
–	–	CS	H	–	–	–	–	Devices Cascaded in Multiplier String
L	–	–	–	OP	–	L	L	Load New Multiplicand and Clear Internal Sum and Carry Registers
H	–	–	–	–	–	–	–	Device Enabled
H	↑	–	–	–	L	L	AR	Shift Sum Register
H	↑	–	–	–	L	H	AR	Add Multiplicand to Sum Register and Shift
H	↑	–	–	–	H	L	AR	Subtract Multiplicand from Sum Register and Shift
H	↑	–	–	–	H	H	AR	Shift Sum Register

H = HIGH
L = LOW
↑ = LOW-to-HIGH transition
CS = Connected to S output of higher order device
OP = X_i latches open for new data (i = 0, 7)
AR = Output as required per Booth's algorithm

Figure 5. Function Table Showing the Operation of the Am25LS14A

control flip flop, and loads the new multiplicand into the X holding latch. At this same time, the multiplier word can be loaded into a Parallel-to-Serial converter (such as the Am25LS22) ready for presenting to the Serial/Parallel multiplier Y input. During the first time period after the clear signal, the least significant bit of the multiplier is presented to the Y input of the Am25LS14A and in the next clock period the first bit of the product, S_0, is available at the S output of the device. For the next n–1 clock periods, the multiplier bits are presented one at a time to the multiplier Y input and the

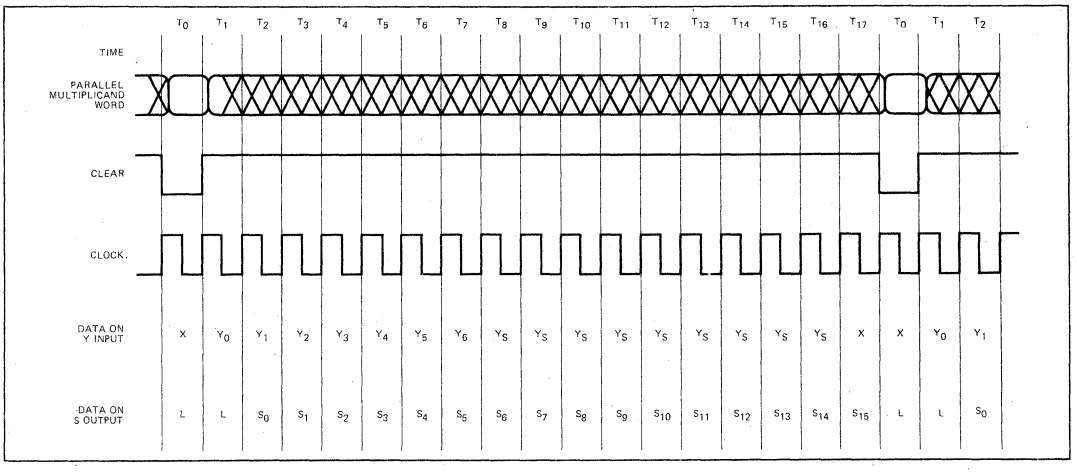


Figure 6. Timing Diagram Showing 18 Clock Cycle Operation of 8 x 8 Multiplication

product bits are available one at a time from the S output. For the remaining m clock periods, the Serial/Parallel multiplier requires that either the most significant bit of the multiplier word, Y, be repeated (two's complement operation) or a string of zeroes be applied (if the multiplier is to be treated as an unsigned number) to the Y input.

It is possible to perform an m + n multiplication using only one additional clock cycle. This requires that the clear pulse is presented at the same time as Y_0, the least significant Y multiplier bit. Since the minimum clear pulse width is 20ns and the clear recovery time is 18ns, the time duration must be at least 38ns minimum for this clock period. A timing diagram for this mode of operation is shown in Figure 7.

Many applications, especially when using two's complement operands, do not required a full n + m bit product but only an m + n−1 bit product. For example, if fractional operands in the number range of −1 to $1-2^{-(n-1)}$ and −1 to $1-2^{-(m-1)}$ are assumed, only the case of −1 times −1 requires m + n bits to represent the product. All other combinations can be represented correctly in two's complement notation by m + n −1 bits. That is, when dealing with fractions, only one bit to the left of the binary point carrying a weight of −1 is required except for the one special case. This can be used to remove one additional clock cycle from the multiplication process as shown in Figure 8. The same reasoning applies to integer representations where the largest negative numbers are $-2^{(m-1)}$ and $-2^{(n-1)}$. Only m + n bits are required to handle the case of $(-2^{(m-1)})$ $(-2^{(n-1)})$. All other products require only m + n−1 bits for a correct two's complement product. Let's take an example. If m = 4 and n = 3, then seven bits are required to represent (−8)• (−4) = (+32) in two's complement. All other products for a 3-bit and 4-bit multiplicand and multiplier can be represented correctly in two's complement form with a 6-bit representation.

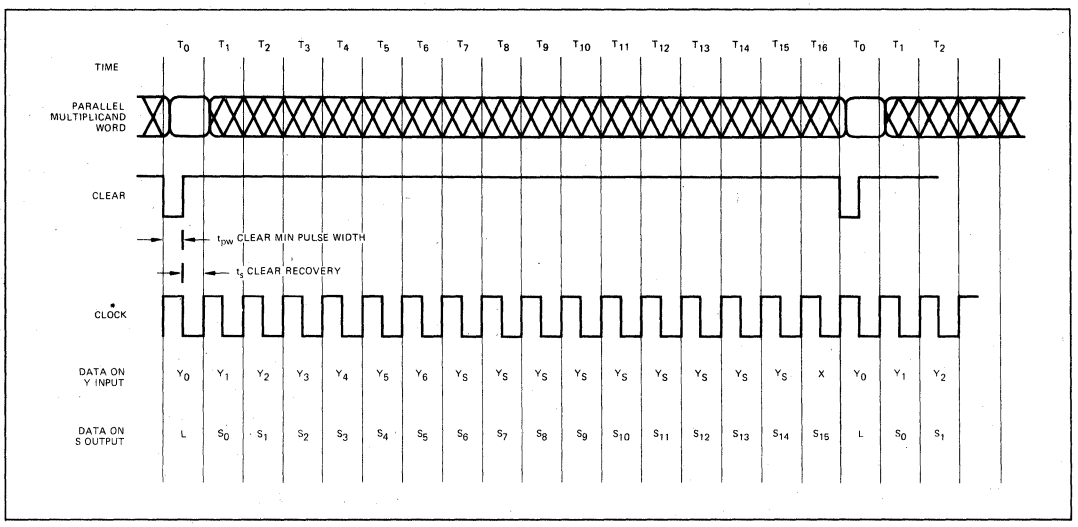


Figure 7. Timing Diagram Showing 17 Clock Cycle Operation of 8 x 8 Multiplication

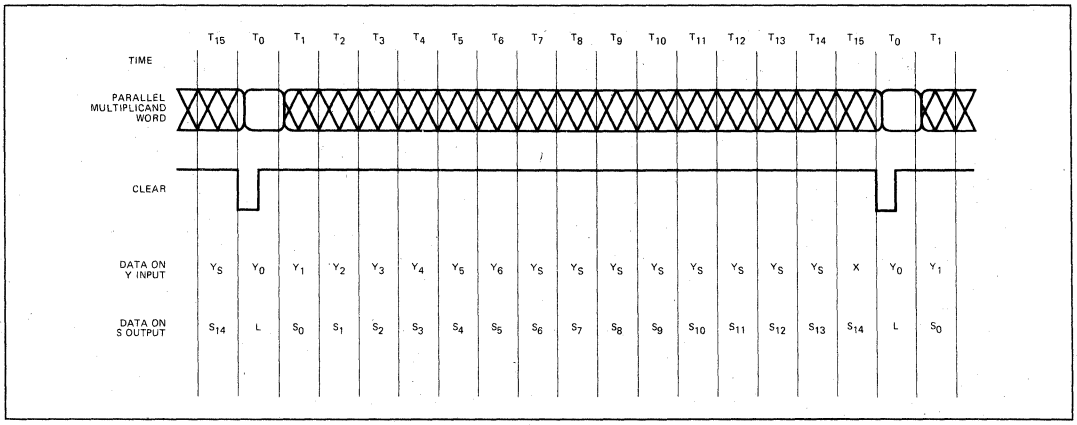


Figure 8. Timing Diagram Showing 16 Clock Cycle Operation for an 8 x 8 Multiplication (Assumes a 15-Bit Product Representation)

ROUNDING AND TRUNCATION

Truncation is performed in the Am25LS14A by ignoring the appropriate number of least significant bits (LSB's). Unfortunately, no clock cycles can be saved when truncating because the product is being developed LSB first. Therefore, the truncated bits are the first bits out of the Am25LS14A multiplier. The subsystem must be clocked the total number of times (m + n) to develop the two's complement product. This does have the advantage of saving register bits to hold the product from the device.

To date, the recommended method of rounding is to use one-fourth of an Am25LS15 to perform rounding. This technique involves adding a one at the bit prior to the LSB of the final product using one input of the Am25LS15. The product from the multiplier is connected to the other input. This does require one extra clock cycle to implement rounding. This technique works for any combination of multiplicand bits, multiplier bits and desired product bits.

APPLICATIONS

Eight-Bit by Eight-Bit Multiplier

A circuit which generates a 16-bit product from an 8-bit by 8-bit multiplication is depicted in Figure 9. This sub-system consists of one Am25LS14A serial/parallel multiplier and two Am25LS22 8-bit registers. This configuration accepts an 8-bit multiplicand and an 8-bit multiplier from an 8-bit data bus. It will return a 16-bit product (8-bit upper byte and 8-bit lower byte) using the same 8-bit bus.

The Am25LS22 is an 8-bit register designed for performing various functions with the Am25LS14A. It can be used to hold the multiplier word initially, perform the sign-extend function and then hold part of the product. It has separate serial input/output capability as well as shared parallel input/outputs.

The timing sequence for controlling this circuit is shown in Figure 10. Twenty-two clock cycles are used in this example to fully load, multiply and unload the multiplier subsystem. Thus, such an arrangement can be used with any of the popular 8-bit MOS microprocessors such as the 8080, 6800, 2650, F8 and others. This allows the multiplication to be performed outside of the MOS microprocessor with about two to three orders of magnitude improvement in speed.

Referring to the timing sequence of Figure 10, the multiplier word is loaded into the Am25LS22 register at time T_1 and the multiplicand word is loaded in the Am25LS14A latches during time T_1. The multiplicand and multiplier words must be loaded in this order since there is no hold function on the Am25LS14A multiplier.

During time T_2 through T_{10}, the least significant product bits are generated and clocked into holding register B. Meanwhile the multiplier sign bit is being extended in Register A. The sign extend is performed only for the eight clock cycles T_2 through T_9. During time T_{11} through T_{18}, the most significant 8-bits of the product are developed in the Am25LS14A multiplier. T_8 is used to load the product sign bit from the multiplier into the Am25LS22 B register. During the time T_1 through T_8, the least significant half of the product is transferred from register B to register A. The remaining two clock cycles, T_{19} and T_{20} are used to unload the product upper and lower byte back onto the 8-bit data bus.

The control signals required for this multiplier are shown in Figures 9 and 10. Notice that the clear input to the Am25LS14A and the Serial/Parallel (S/P) input to the Am25LS22 can be connected together with the appropriate don't cares eliminated. Other control signals to the Am25LS22 include the register enable (RE), sign extend (SE), and the three-state control ($\overline{OE}$). These signals can be generated using a counter and combinatorial logic gates or a counter and small PROM.

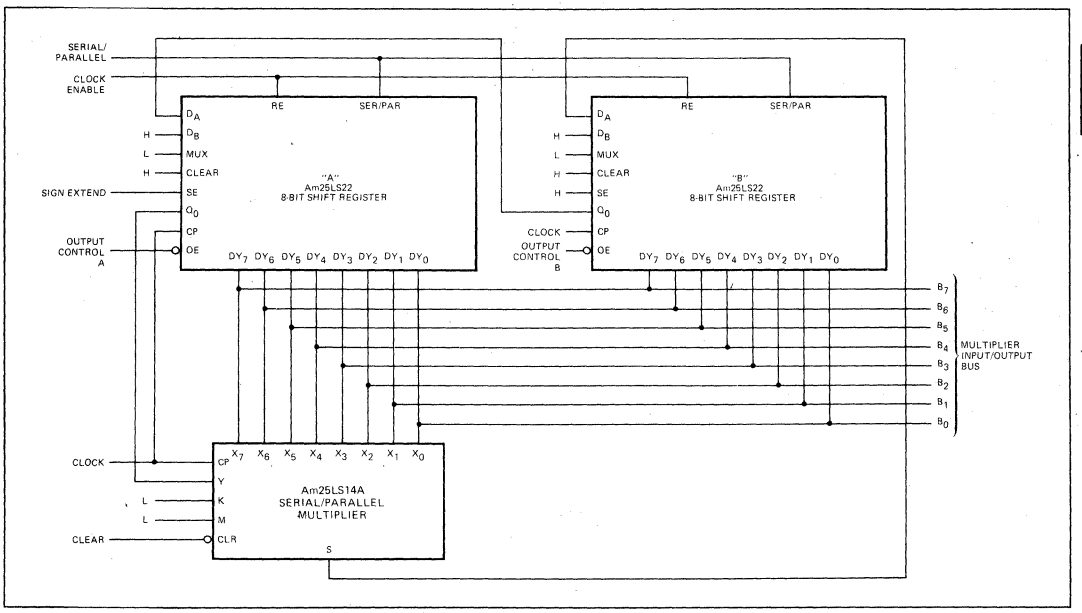


Figure 9. An 8-Bit by 8-Bit Multiplier with a Full 16-Bit Product Store. The Inputs and Outputs are Bus Organized on an 8-Bit Bus

		Am25LS14A			Am25LS22's					
TIME	I/O BUS	Y	CLR	S	S/P	RE	SE	$\overline{OE}$ A	$\overline{OE}$ B	FUNCTION
T_0	Multiplier	X	X	X	L	L	X	H	H	Load Multiplier (Y)
T_1	Multiplicand	X	L	X	X	H	X	H	H	Load Multiplicand (X)
T_2	X	Y_0	H	L	H	L	L	H	H	
T_3	X	Y_1	H	S_0	H	L	L	H	H	
T_4	X	Y_2	H	S_1	H	L	L	H	H	
T_5	X	Y_3	H	S_2	H	L	L	H	H	Present Y_i to multiplier. Read S_i into Register B.
T_6	X	Y_4	H	S_3	H	L	L	H	H	Extend Y sign.
T_7	X	Y_5	H	S_4	H	L	L	H	H	
T_8	X	Y_6	H	S_5	H	L	L	H	H	
T_9	X	Y_S	H	S_6	H	L	L	H	H	
T_{10}	X	Y_S	H	S_7	H	L	H	H	H	
T_{11}	X	Y_S	H	S_8	H	L	H	H	H	
T_{12}	X	Y_S	H	S_9	H	L	H	H	H	
T_{13}	X	Y_S	H	S_{10}	H	L	H	H	H	Continue Multiplication using Y_S in register. Load
T_{14}	X	Y_S	H	S_{11}	H	L	H	H	H	least significant part of product into Register A
T_{15}	X	Y_S	H	S_{12}	H	L	H	H	H	and most significant in Register B.
T_{16}	X	Y_S	H	S_{13}	H	L	H	H	H	
T_{17}	X	Y_S	H	S_{14}	H	L	H	H	H	
T_{18}	X	X	H	S_{15}	H	L	H	H	H	Load MSB into Register.
T_{19}	Product Lower Byte	X	X	X	X	H	X	L	H	Unload product Lower byte onto bus.
T_{20}	Product Upper Byte	X	X	X	X	H	X	H	L	Unload product Upper byte onto bus.

H = HIGH L = LOW X = Don't Care

Figure 10. Timing Sequence for an 8 x 8 Multiplier with Full 16-Bit Product Register

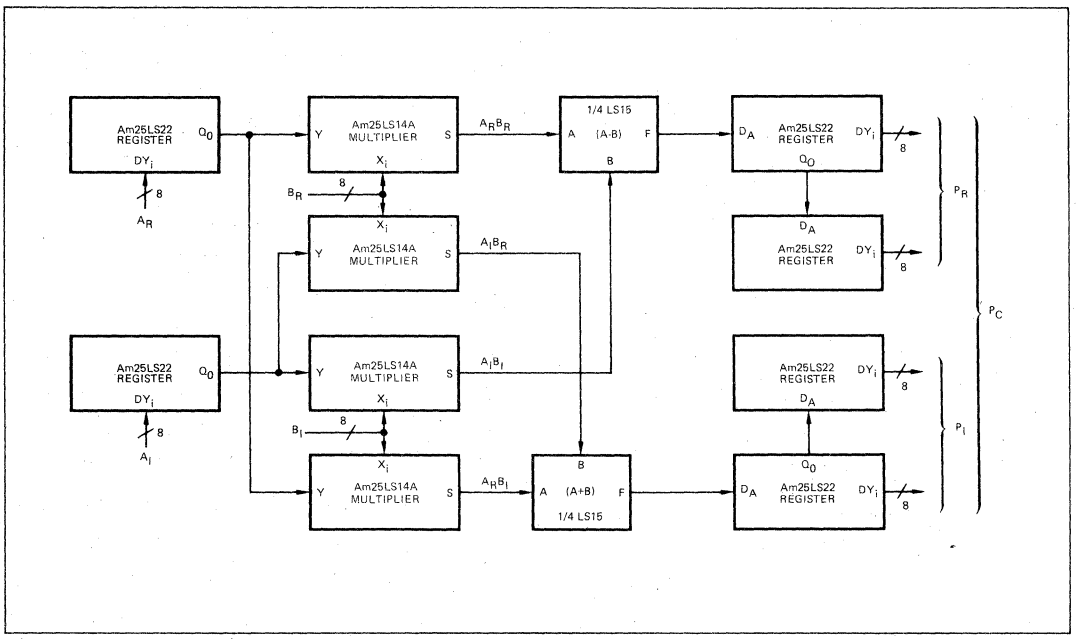


Figure 11. Complex Arithmetic Multiply $P_C = (A_RB_R - A_IB_I) + j(A_RB_I + A_IB_R)$

COMPLEX ARITHMETIC MULTIPLIER

The Am25LS14A serial/parallel multiplier, the Am25LS15 adder/subtractor, and the Am25LS22 eight-bit register can be used to perform rapid multiplication in complex arithmetic processors. In complex arithmetic notation, each variable is assumed to have a real part and an imaginary part. Thus, complex variables A_C and B_C may be represented as:

$$A_C = A_R + jA_I$$
$$B_C = B_R + jB_I$$

The product of A_C and B_C is, of course, complex product P_C where:

$$P_C = P_R + jP_I = A_C B_C$$
$$P_C = (A_R + jA_I)(B_R + jB_I)$$
$$P_C = (A_R B_R - A_I B_I) + j(A_R B_I + A_I B_R)$$

From this discussion, the real and imaginary values of the product P_C are readily identified. These are:

$$P_R = A_R B_R - A_I B_I$$
$$P_I = A_R B_I + A_I B_R$$

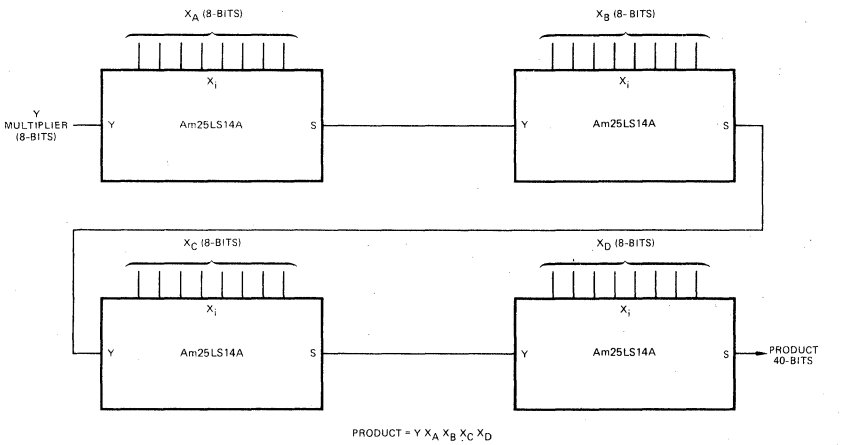
The circuitry required to implement this complex multiplier is shown in Figure 11. In this example, the real and imaginary values of the A_C variable are loaded into the two Am25LS22 registers. The real and imaginary values of the B_C variable are loaded into the latches of the Am25LS14A. This loading of the data could be performed simultaneously using all four inputs A_R, A_I, B_R and B_I or it could be performed sequentially using a pair of inputs or a single input at a time.

Once the incoming A_C and B_C data have been loaded, the devices are clocked such that the four intermediate products are formed as shown in Figure 11. Then, two of the four adder/subtractors in the Am25LS15 are used to complete the generation of real product term P_R and the imaginary product term P_I.

These product terms P_R and P_I can be loaded into four additional Am25LS22 registers to hold the double length product terms P_R and P_I (assume least significant bit truncation). After the complex multiplication has been completed, the P_R and P_I variables can be returned to the processor, memory or other destination by using the parallel bus outputs of the Am25LS22.

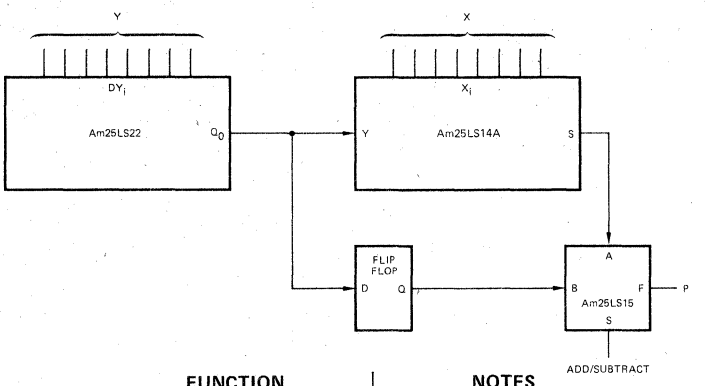
OTHER APPLICATIONS

Other examples of applications using the Am25LS14A as well as the Am25LS15 and Am25LS22 are shown in Figures 12 through 15. Each of these applications is intended to give the design engineer a new approach to solving numerical problems involving digital multiplication.



Four Am25LS14A's can be used to implement the product of five variables Y, X_A, X_B, X_C and X_D. If each input variable is eight bits, a 40-bit product results and the multiplier array must be clocked 40 times. This requires the 8-bit Y variable to be sign extended for 32 additional clock cycles.

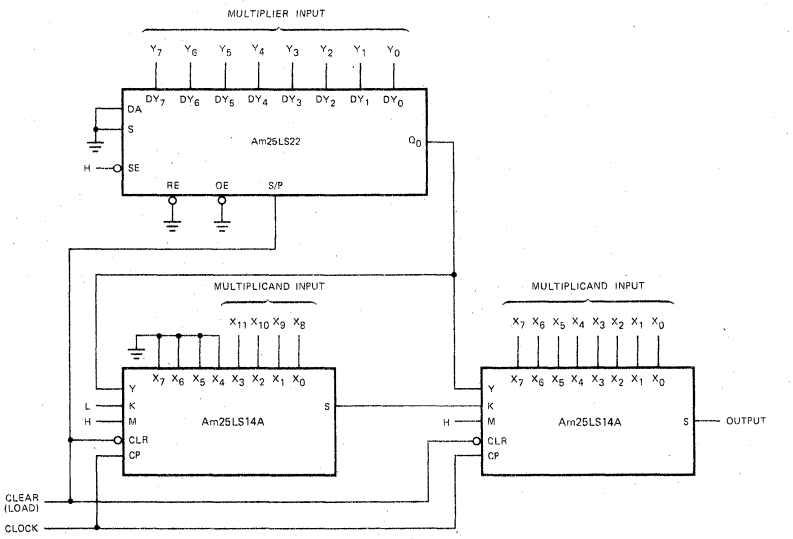
Figure 12. Multiple Operand Multiplications



	FUNCTION		NOTES
1	$P = X \cdot Y + Y$	$= Y(X + 1)$	'LS15 in add mode
2	$P = X \cdot Y - Y$	$= Y(X - 1)$	'LS15 in subtract mode
3	$P = X \cdot Y + Y + 1$	$= Y(X + 1) + 1$	'LS15 is subtract mode for clear and add mode for multiply
4	$P = Y - X \cdot Y$	$= Y(1 - X)$	'LS15 A & B inputs reversed

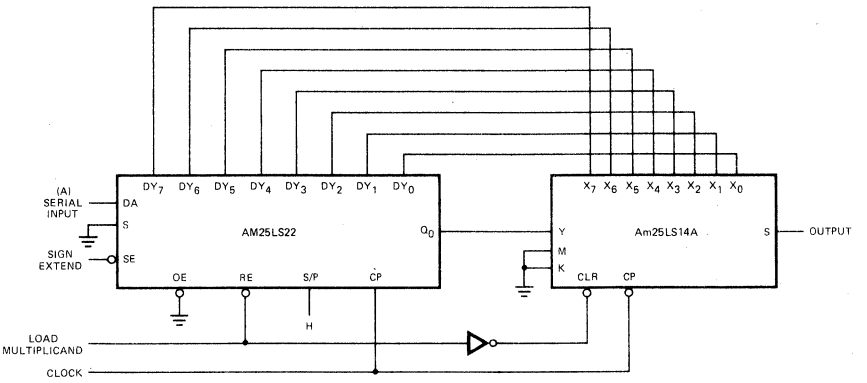
One Am25LS14A, Am25LS15 and Am25LS22 can be used to perform several arithmetic functions. Four such functions are shown above. All use a product equal to the multiplicand times the multiplier in combination with a function of the multiplier. Additional combinations are possible, especially if more flip-flops are used to change the relative weight of the multiplier or product function.

Figure 13.



A 12-bit by 8-bit unsigned multiplication is performed by tying the four most significant multiplicand bits LOW to logic zero. The Am25LS22 is loaded with the 8-bit unsigned multiplier. As the multiplier is shifted, a "zero-fill" is accomplished using the D_A input on the Am25LS22. Note the MSB M-input is HIGH on the most significant Am25LS14A.

Figure 14.



One Am25LS14A and Am25LS22 can be used to perform the function A^2 on an input variable A. The 8-bit value for A is loaded into the Am25LS22 register in serial form using the D_A input. Once loaded, the A value can be transferred to the Am25LS14A multiplicand latches via the DY_i outputs. Then the product of A·A is formed resulting in A^2 at the Am25LS14A output.

Figure 15.

9

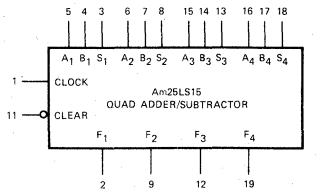
Am25LS15

Quad Serial Adder/Subtractor

DISTINCTIVE CHARACTERISTICS

- Four independent adder/subtractors
- Use with two's complement arithmetic
- Magnitude only addition/subtraction
- Second sourced by T.I. as Am54LS/74LS385

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

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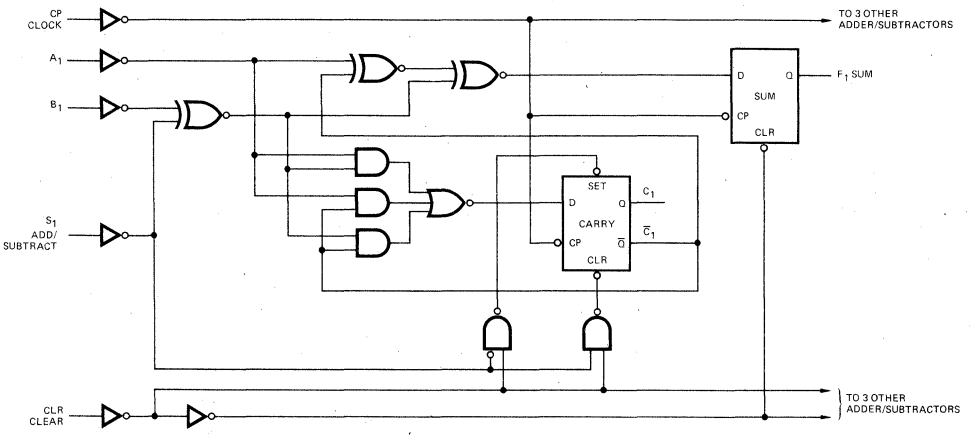
FUNCTIONAL DESCRIPTION

The Am25LS15 is a serial two's complement adder/subtractor designed for use in association with the Am25LS14 serial/parallel two's complement multiplier. This device can also be used for magnitude only or one's complement addition or subtraction.

Four independent adder/subtractors are provided with common clock and clear inputs. The add function is A plus B and the subtract function is A minus B. The clear function sets the internal carry function to logic zero in the add mode and to logic one in subtract mode. This least significant carry is self propagating in the subtract mode as long as zeroes are applied to the A and B inputs at the LSB's. All internal flip-flops change state on the LOW-to-HIGH clock transition.

The Am25LS15 is particularly useful for recursive or non-recursive digital filtering or butterfly networks in Fast Fourier Transforms.

LOGIC DIAGRAM
(One of Four Similar Functions)



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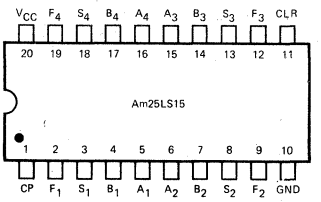
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-331

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0 to +70°C	AM25LS15PC
Hermetic DIP	0 to +70°C	AM25LS15DC
Dice	0 to +70°C	AM25LS15XC
Hermetic DIP	−55 to +125°C	AM25LS15DM
Hermetic Flat-Pak	−55 to +125°C	AM25LS15FM
Dice	−55 to +125°C	AM25LS15XM

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5%	(MIN. = 4.75V MAX. = 5.25V)
MIL	T_A = −55°C to +125°C	V_{CC} = 5.0V ± 10%	(MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −440μA V_{IN} = V_{IH} or V_{IL}	MIL	2.5			Volts
			COM'L	2.7			
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V				0.1	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			48	75	mA

Notes: 1. For conditions shown as Min. or Max., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All inputs HIGH, measured after a LOW-to-HIGH clock transition.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

9

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Output			14	22	ns	C_L = 15pF R_L = 2.0kΩ
t_{PHL}				14	22		
t_{PHL}	Clear to Output			20	30	ns	
t_s	A, B, S		10			ns	
t_h			0				
t_s	Clear Recovery		25			ns	
t_h	Clear Hold Time		0			ns	
t_{pw}	Clock	HIGH	17			ns	
		LOW	17				
t_{pw}	Clear LOW		20			ns	
f_{max} (Note 1)	Maximum Clock Frequency		30	40		MHz	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on the t_r, t_f, pulse width or duty cycle.

Am25LS15
SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am25LS COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Clock to Output			33		38	ns	C_L = 50pF R_L = 2.0kΩ
t_{PHL}				33		38		
t_{PHL}	Clear to Output			43		50	ns	
t_s	A, B, S		17		20		ns	
t_h			4		5			
t_s	Clear Recovery		37		42		ns	
t_h	Clear Hold Time		4		5		ns	
t_{pw}	Clock	HIGH	26		30		ns	
		LOW	26		30			
t_{pw}	Clear LOW		30		35		ns	
f_{max} (Note 1)	Maximum Clock Frequency		23		20		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

A_1, A_2, A_3, A_4 The "A" input into each adder/subtractor

B_1, B_2, B_3, B_4 The "B" input into each adder/subtractor

S_1, S_2, S_3, S_4 The add subtract control for each adder/subtractor. When S is LOW, the F function is A+B. When S is HIGH, the F function is A−B.

F_1, F_2, F_3, F_4 The four independent serial outputs of the adder/subtractor.

CP Clock The clock input for the device. All internal flip-flops change state on the LOW-to-HIGH transition.

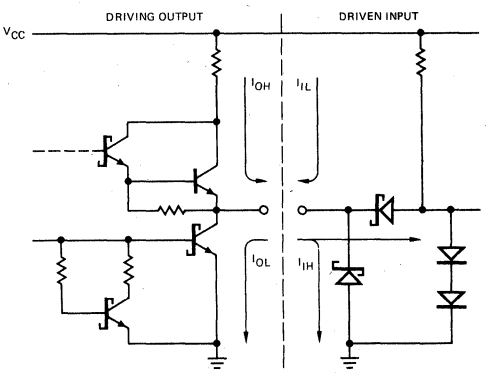
CLR Clear When the clear input is LOW, the four independent adder/subtractors are asynchronously reset. The sum flip-flop is always set to logic "0". The carry flip-flop is set to logic "0" in the add mode and logic "1" in the subtract mode.

FUNCTION TABLE

External Inputs					Internal Point		Output	
CP	CLR	S	A	B	C	C_1	F	Function
X	L	L	X	X	L	L	L	Clear
X	L	H	X	X	H	H	L	
L	H	X	X	X	NC	NC	NC	
H	H	X	X	X	NC	NC	NC	
↑	H	L	L	L	L	L	L	Add
↑	H	L	L	L	H	L	H	
↑	H	L	L	H	L	L	H	
↑	H	L	L	H	H	H	L	
↑	H	L	H	L	L	L	H	
↑	H	L	H	L	H	H	L	
↑	H	L	H	H	L	H	L	
↑	H	L	H	H	H	H	H	
↑	H	H	L	L	L	L	H	Subtract
↑	H	H	L	L	H	H	L	
↑	H	H	L	H	L	L	L	
↑	H	H	L	H	H	L	H	
↑	H	H	H	L	L	H	L	
↑	H	H	H	L	H	H	H	
↑	H	H	H	H	L	L	H	
↑	H	H	H	H	H	H	L	

C = Data In the Carry Flip-Flop Before the Clock Transition
C_1 = Data In the Carry Flip-Flop After the Clock
X = Don't Care
NC = No Change
H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition

Am25LS • Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

APPLICATIONS

The normal butterfly network associated with the Cooley-Tukey Fast Fourier Transform (FFT) algorithm is shown below. Here we assume A, B, C, D and W are all complex numbers such that:

$A = A_R + jA_I$

$B = B_R + jB_I$

$W = W_R + jW_I$

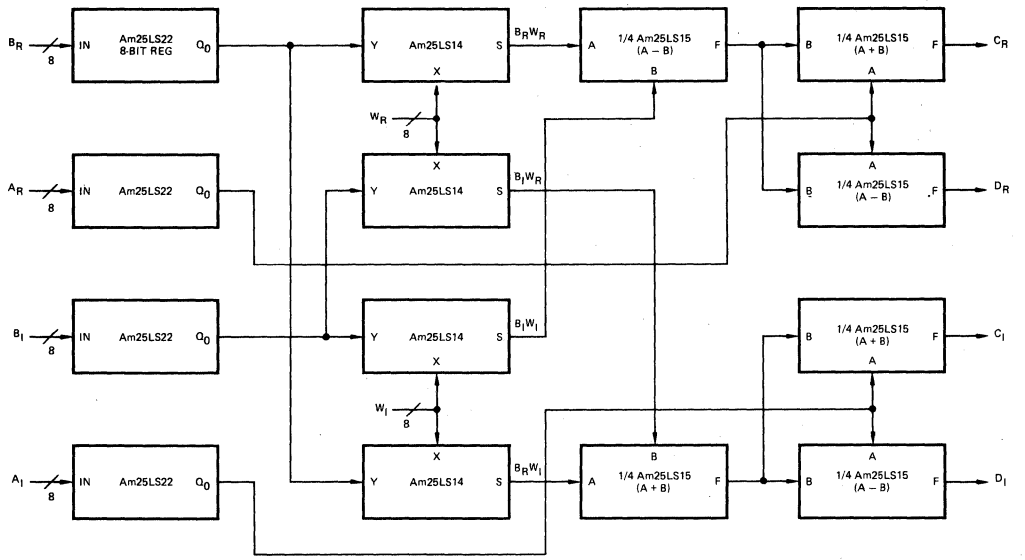
The outputs C and D are also complex numbers and are evaluated as:

$C = C_R + jC_I = (A_R + B_R W_R - B_I W_I) + j(A_I + B_R W_I + B_I W_R)$

$D = C_R + jD_I = (A_R - B_R W_R + B_I W_I) + j(A_I - B_R W_I - B_I W_R)$

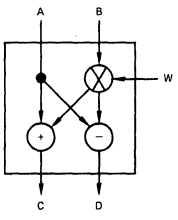
The four multiplications can be implemented using four Am25LS14 serial-parallel multipliers (the appropriate number of bits must, of course, be used). The additions and the subtractions are implemented using the Am25LS15 quad serial adder/subtractors. This diagram depicts only the basic data flow; binary weighting of the numbers, rounding, truncation, etc. must be handled as required by the individual design parameters.

FAST FOURIER TRANSFORM (FFT) BUTTERFLY

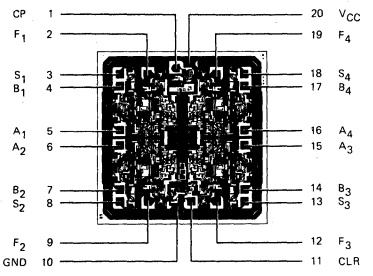


An FFT butterfly connection for complex arithmetic inputs and outputs.

Functional Diagram for FFT Butterfly Connection



Metallization and Pad Layout



DIE SIZE 0.095" X 0.095"

9

Am25S18

Quad D Register with Standard and Three-State Outputs

Distinctive Characteristics

- Advanced Schottky technology
- Four D-type flip-flops
- Four standard totem-pole outputs
- Four three-state outputs
- 75 MHz clock frequency

FUNCTIONAL DESCRIPTION

The Am25S18 consists of four D-type flip-flops with a buffered common clock. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

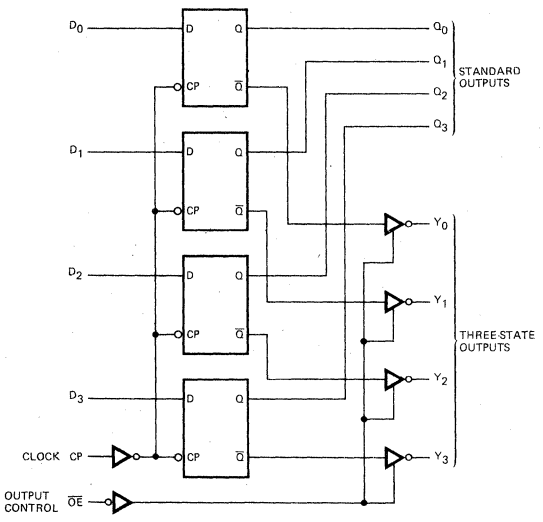
The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" ($\overline{OE}$) input is LOW. When the $\overline{OE}$ input is HIGH, the Y outputs are in the high-impedance state.

The Am25S18 is a 4-bit, high speed Schottky register intended for use in real-time signal processing systems where the standard outputs are used in a recursive algorithm and the three state outputs provide access to a data bus to dump the results after a number of iterations.

The device can also be used as an address register or status register in computers or computer peripherals.

Likewise, the Am25S18 is also useful in certain display applications where the standard outputs can be decoded to drive LED's (or equivalent) and the three-state outputs are bus organized for occasional interrogation of the data as displayed.

LOGIC DIAGRAM



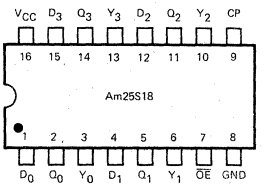
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0 to +70°C	AM25S18PC
Hermetic DIP	0 to +70°C	AM25S18DC
Dice	0 to +70°C	AM25S18XC
Hermetic DIP	−55 to +125°C	AM25S18DM
Hermetic Flat-Pak	−55 to +125°C	AM25S18FM
Dice	−55 to +125°C	AM25S18XM

RELATED PRODUCTS

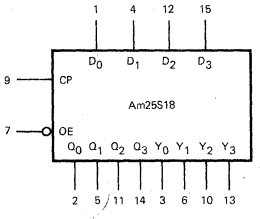
Part No.	Description
Am25S07	Register
Am25S08	Register
Am25S09	Register
Am25S374	Register
Am29821-26	Register

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am25S18XC T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am25S18XM T_A = −55°C to +125°C V_{CC} = 5.0V ± 10% (MIL) MIN. = 4.5V MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Q	I_{OH} = −1mA MIL	2.5	3.4		Volts
				I_{OH} = −1mA COM'L	2.7	3.4		
			Y	XM, I_{OH} = −2mA	2.4	3.4		
				XC, I_{OH} = −6.5mA	2.4	3.2		
V_{OL}	Output LOW Voltage (Note 6)	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = V_{IH} or V_{IL}					0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V					−2.0	mA
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V					50	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_O	Y Output Off-State Leakage Current	V_{CC} = MAX.		V_O = 2.4V			50	µA
				V_O = 0.4V			−50	
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.			−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)				80	130	mA

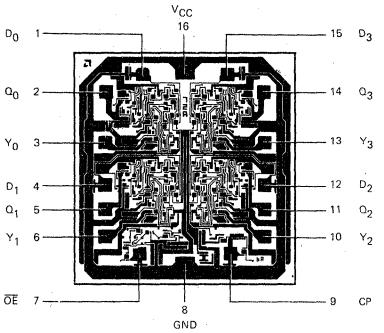
Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, T_A = 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (see Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test shoud not exceed one second.
5. I_{CC} is measured with all inputs at 4.5V and all outputs open.
6. Measured on Q outputs with Y outputs open. Measured on Y outputs with Q outputs open.

Am25S18

Switching Characteristics (T_A = +25°C, V_{CC} = 5.0V, R_L = 280Ω)

Parameters	Description		Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Clock to Q Output		C_L = 15pF		6.0	9.0	ns
t_{PHL}					8.5	13	
t_{pw}	Clock Pulse Width	HIGH		7.0			ns
		LOW		9.0			
t_s	Data			5.0			ns
t_h	Data			3.0			ns
t_{PLH}	Clock to Y Output ($\overline{OE}$ LOW)				6.0	9.0	ns
t_{PHL}					8.5	13	
t_{ZH}	Output Control to Output		C_L = 15pF		12.5	19	ns
t_{ZL}					12	18	
t_{HZ}			C_L = 5.0pF		4.0	6.0	
t_{LZ}					7.0	10.5	
f_{max}	Maximum Clock Frequency		C_L = 15pF	75	100		MHz

Metallization and Pad Layout



DIE SIZE 0.077" X 0.079"

TRUTH TABLE

INPUTS			OUTPUTS		NOTES
$\overline{OE}$	CLOCK CP	D	Q	Y	
H	L	X	NC	Z	—
H	H	X	NC	Z	—
H	↑	L	L	Z	—
H	↑	H	H	Z	—
L	↑	L	L	L	—
L	↑	H	H	H	—
L	—	—	L	L	1
L	—	—	H	H	1

L = LOW
H = HIGH
X = Don't care

NC = No change
↑ = LOW to HIGH transition
Z = High impedance

Note: 1. When $\overline{OE}$ is LOW, the Y output will be in the same logic state as the Q output.

DEFINITION OF FUNCTIONAL TERMS

D_i The four data inputs to the register.

Q_i The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.

Y_i The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the Y_i outputs to the high-impedance state.

CP Clock. The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.

$\overline{OE}$ Output Control. When the $\overline{OE}$ input is HIGH, the Yi outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

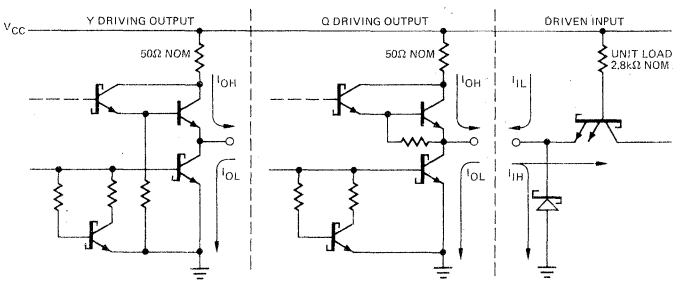
LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
D_0	1	1	—	—
Q_0	2	—	20	10*
Y_0	3	—	40/130	10*
D_1	4	1	—	—
Q_1	5	—	20	10*
Y_1	6	—	40/130	10*
$\overline{OE}$	7	1	—	—
GND	8	—	—	—
CP	9	1	—	—
Y_2	10	—	40/130	10*
Q_2	11	—	20	10*
D_2	12	1	—	—
Y_3	13	—	40/130	10*
Q_3	14	—	20	10*
D_3	15	1	—	—
V_{CC}	16	—	—	—

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

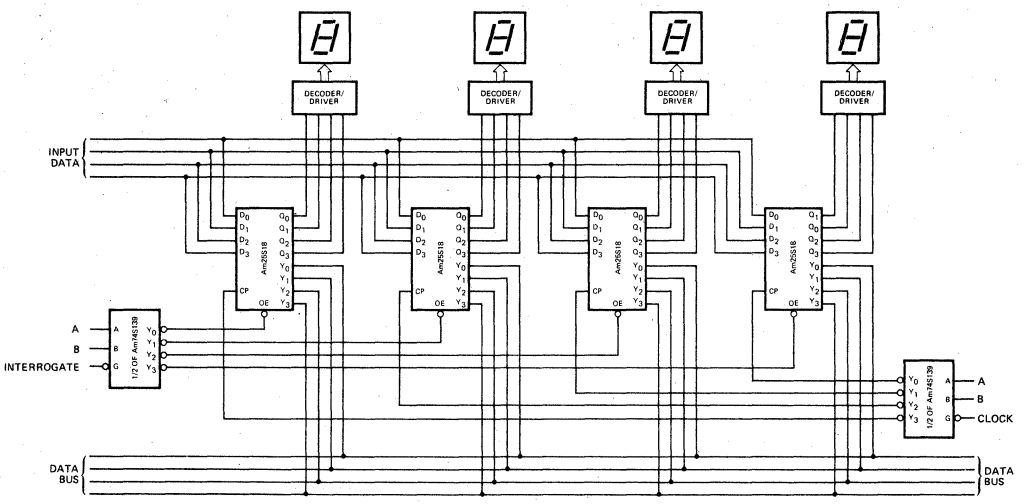
*Fan-out on each Q_i and Y_i output pair should not exceed 15 unit loads (30mA) for i = 0, 1, 2, 3.

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

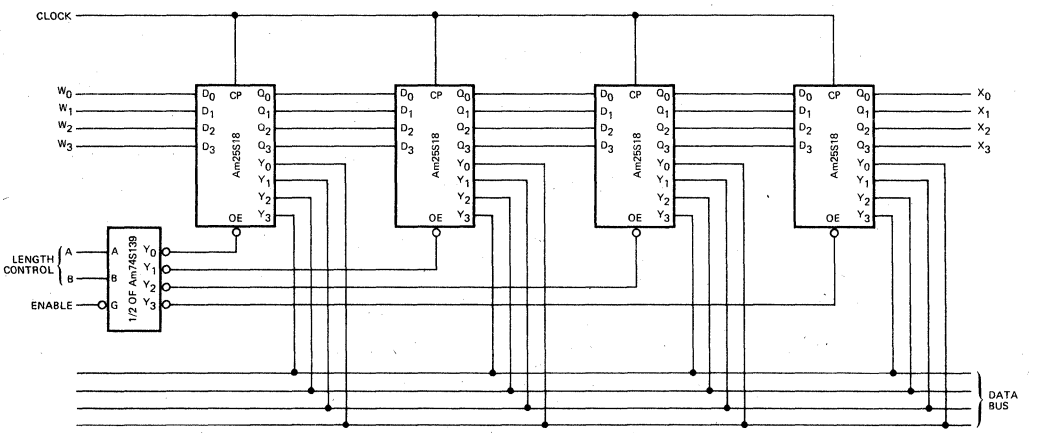


Note: Actual current flow direction shown.

APPLICATIONS



THE Am25S18 USED AS DISPLAY REGISTER WITH BUS INTERROGATE CAPABILITY.



THE Am25S18 AS A VARIABLE LENGTH (1, 2, 3 or 4 WORD) SHIFT REGISTER.

Am25LS22

8-Bit Serial/Parallel Register with Sign Extend

DISTINCTIVE CHARACTERISTICS

- Three-state outputs with multiplexed input
- Multiplexed serial data input
- Sign extend function
- Second sourced by T.I. as Am54LS/74LS322

RELATED PRODUCTS

Part No.	Description
Am25LS23	8-Bit Shift/Storage Register

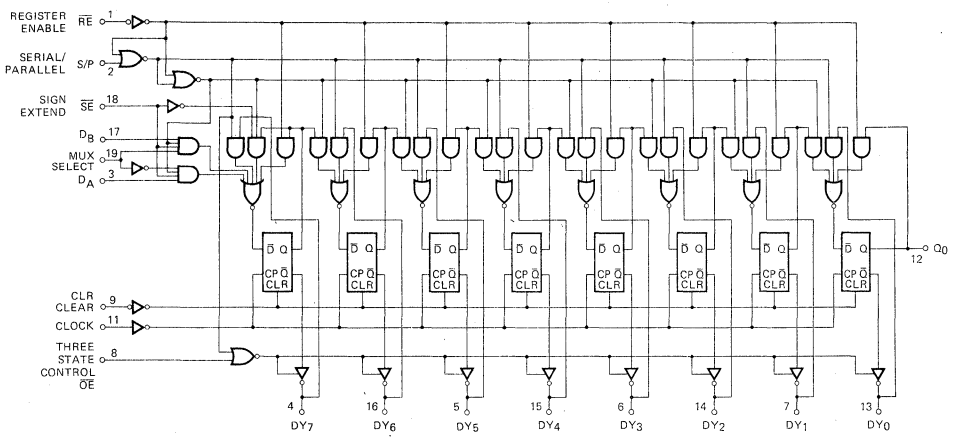
FUNCTIONAL DESCRIPTION

The Am25LS22 is an eight-bit serial/parallel register built using advanced Low-Power Schottky processing. The device features an eight-bit parallel multiplexed input/output port to provide improved bit density in a 20-pin package. Data may also be loaded into the device in a serial manner from either input D_A or D_B. A serial output, Q_0, is also provided.

The Am25LS22 is specifically designed for operation with the Am25LS14 serial/parallel two's complement multiplier and provides the sign extend function required for this device.

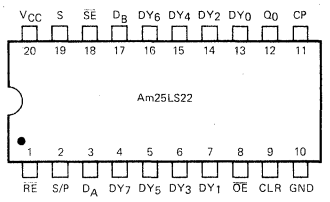
When the Register Enable ($\overline{RE}$) input is HIGH, the register will retain its current contents. Synchronous parallel loading is accomplished by applying a LOW to $\overline{RE}$ and applying a LOW to the Serial/Parallel (S/P) input. This places the three-state outputs in the high-impedance state independent of $\overline{OE}$ and allows data that is applied on the input/output lines (DY_i) to be clocked into the register. When the S/P input is HIGH, the device will shift right. The Sign Extend ($\overline{SE}$) input is used to repeat the sign in the Q_7 flip-flop. This occurs whenever $\overline{SE}$ is LOW when the SHIFT mode is selected. When $\overline{SE}$ is high, the serial two-input multiplexer is enabled. Thus, either D_A or D_B can be selected to load data serially. The register changes state on the LOW-to-HIGH transition of the clock. A clear input (CLR) is used to asynchronously reset all flip-flops when a LOW is applied.

LOGIC DIAGRAM



MPR-333

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-334

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0 to +70°C	AM25LS22PC
Hermetic DIP	0 to +70°C	AM25LS22DC
Dice	0 to +70°C	AM25LS22XC
Hermetic DIP	−55 to +125°C	AM25LS22DM
Hermetic Flat-Pak	−55 to +125°C	AM25LS22FM
Dice	−55 to +125°C	AM25LS22XM

Am25LS22
ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)				Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	Q_0, $I_{OH} = -440\mu A$		MIL	2.5			Volts
					COM'L	2.7			
			DY_i, $I_{OH} = -1.0mA$		MIL	2.4			
			DY_i, $I_{OH} = -2.6mA$		COM'L	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}		$I_{OL} = 4.0mA$				0.4	Volts
				$I_{OL} = 8.0mA$				0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs				2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			MIL			0.7	Volts
					COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$						−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$			$\overline{SE}$			−1.08	mA
					S			−0.72	
					Others			−0.36	
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$ (Except DY_i)			$\overline{SE}$			60	μA
					S			40	
					Others			20	
I_I	Input HIGH Current	V_{CC} = MAX., (Except DY_i)	$V_{IN} = 7.0V$	$\overline{OE}$, S/P, RE, CP, CLR				0.1	mA
			$V_{IN} = 5.5V$	$\overline{SE}$				0.3	
				S				0.2	
				Others				0.1	
I_{OZ}	Off State (High Impedance) Output Current (DY_i)	V_{CC} = MAX.			$V_O = 2.4V$			40	μA
					$V_O = 0.4V$			−100	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.				−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.					40	65	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25° C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage ($\overline{OE}$, S/P, RE, CP, CLR)	−0.5V to +7.0V
DC Input Voltage (Others)	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to DY_i			16.5	24	ns	R_L = 2.0kΩ, C_L = 15pF
t_{PHL}				18	26		
t_{PHL}	Clear to DY_i			23	30	ns	
t_{PLH}	Clock to Q_0			16.5	24	ns	
t_{PHL}				18	26		
t_{PHL}	Clear to Q_0			23	30	ns	
t_{ZH}	$\overline{OE}$ to DY_i			13	21	ns	
t_{ZL}				18	26		
t_{HZ}				13	21		R_L = 2.0kΩ, C_L = 5pF
t_{LZ}				18	26		
t_{ZH}	SER/PAR to DY_i			18	26	ns	R_L = 2.0kΩ, C_L = 15pF
t_{ZL}				23	32		
t_{HZ}				18	26		R_L = 2.0kΩ, C_L = 5pF
t_{LZ}				23	32		
t_s	RE to Clock		20			ns	R_L = 2.0kΩ, C_L = 15pF
t_s	SE to Clock		10				
t_s	S to Clock		15				
t_s	D_A and D_B to Clock		15				
t_s	DY_i (Load) to Clock		15				
t_s	Clear Recovery to Clock		8.0				
t_s	S/P to Clock		15			ns	
t_h	Any Input		0				
t_h	Clear Hold		0			ns	
t_{pw}	Clock	HIGH	8.0			ns	
		LOW	8.0				
t_{pw}	Clear		20			ns	
f_{max} (Note 1)	Maximum Clock Frequency		35	50		MHz	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

FUNCTION TABLE

Mode	INPUTS							OUTPUTS								
	Clear	Register Enable	Serial/ Parallel	Sign Extend	Mux Select	$\overline{OE}$*	Clock	DY_7	DY_6	DY_5	DY_4	DY_3	DY_2	DY_1	DY_0	Q_0
Clear	L	H	X	X	X	L	X	L	L	L	L	L	L	L	L	L
	L	L	H	X	X	L	X	L	L	L	L	L	L	L	L	L
	L	L	L	X	X	L	X	Z	Z	Z	Z	Z	Z	Z	Z	L
	L	X	X	X	X	H	X	Z	Z	Z	Z	Z	Z	Z	Z	L
Parallel Load	H	L	L	X	X	X	↑	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_0
Shift Right	H	L	H	H	L	L	↑	D_A	Y_{7n}	Y_{6n}	Y_{5n}	Y_{4n}	Y_{3n}	Y_{2n}	Y_{1n}	Y_{1n}
	H	L	H	H	H	L	↑	D_B	Y_{7n}	Y_{6n}	Y_{5n}	Y_{4n}	Y_{3n}	Y_{2n}	Y_{1n}	Y_{1n}
Sign Extend	H	L	H	L	X	L	↑	Y_{7n}	Y_{7n}	Y_{6n}	Y_{5n}	Y_{4n}	Y_{3n}	Y_{2n}	Y_{1n}	Y_{1n}
Hold	H	H	X	X	X	L	↑	NC	NC	NC	NC	NC	NC	NC	NC	NC

L = LOW
H = HIGH
↑ = Clock LOW-to-HIGH Transition
NC = No Change
X = Don't Care
Z = High-Impedance Output State

*When the OE input is HIGH, all input/output terminals are at the high-impedance state; sequential operation or clearing of the register is not affected.

D_7, D_6. . . D_0 = the level of the steady-state input at the respective DY_n terminal is loaded into the flip-flop while the flip-flop outputs (except Q_0) are isolated from the DY_n terminal.

D_A, D_B = the level of the steady-state inputs to the serial multiplexer input.

Y_{7n}, Y_{6n}. . . Y_{0n} = the level of the respective Q_n flip-flop prior to the last Clock LOW-to-HIGH transition.

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Am25LS22
SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Clock to DY_i			35		41	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}				38		44		
t_{PHL}	Clear to DY_i			43		50	ns	
t_{PLH}	Clock to Q_0			35		41	ns	
t_{PHL}				38		44		
t_{PHL}	Clear to Q_0			43		50	ns	
t_{ZH}	OE to DY_i			32		36	ns	
t_{ZL}				38		44		
t_{HZ}				28		31		C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				34		39		
t_{ZH}	SER/PAR to DY_i			38		44	ns	C_L = 50pF, R_L = 2.0kΩ
t_{ZL}				46		53		
t_{HZ}				34		39		C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				42		48		
t_S	RE to Clock		30		35			C_L = 50pF, R_L = 2.0kΩ
t_S	SE to Clock		17		20			
t_S	S to Clock		24		27		ns	
t_S	D_A and D_B to Clock		24		27			
t_S	DY_i (Load) to Clock		24		27			
t_S	Clear Recovery to Clock		15		17			
t_S	S/P to Clock		24		27		ns	
t_h	Any Input		4		5			
t_h	Clear Hold		4		5		ns	
t_{pw}	Clock	HIGH	15		17		ns	
		LOW	15		17			
t_{pw}	Clear		30		35		ns	
f_{max} (Note 1)	Maximum Clock Frequency		26		23		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

DY_i The multiplexed parallel input/output port to the device. Data may be parallel loaded into the register or data can be read in parallel from the register on these pins. These outputs can be forced to the high-impedance state, i = 0 through 7.

Q_0 The continuous output from the Q_0 flip-flop of the register. This output is used for serial shifting.

$\overline{RE}$ Register Enable. When $\overline{RE}$ is LOW, the register functions are enabled. When $\overline{RE}$ is HIGH, the register functions (parallel load, shift right and sign extend) are inhibited.

S/P Serial/Parallel. When S/P is LOW, the register can be synchronously parallel loaded. This input forces the register output buffers to the high-impedance state independent of the $\overline{OE}$ input. When S/P is HIGH, the register contents are shifted right on the clock LOW-to-HIGH transition.

$\overline{SE}$ Sign Extend. When the $\overline{SE}$ input is LOW, the contents of the Q_7 flip-flop will be repeated in the Q_7 flip-flop as the register is shifted right. When $\overline{SE}$ is HIGH, the two-input multiplexer (D_A and D_B) is enabled to enter data during the serial shift right. The Q_7 flip-flop (DY_7) is normally considered the MSB of the register for arithmetic definitions.

D_A, D_B The serial inputs to the device.

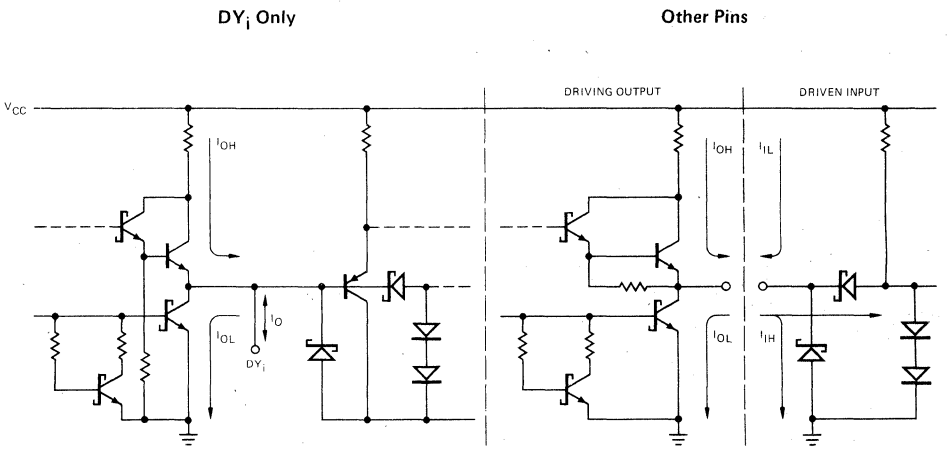
S Multiplexer Select. When S is LOW, the D_A serial input is selected. When S is HIGH, the D_B serial input is selected.

CLR Clear. The asynchronous clear to the register. When the clear is LOW, the outputs of the flip-flops are set LOW independent of all other inputs. When the clear is HIGH, the register will perform the selected function.

CP Clock. The clock pulse for the register. Register operations occur on the LOW-to-HIGH transition of the clock pulse.

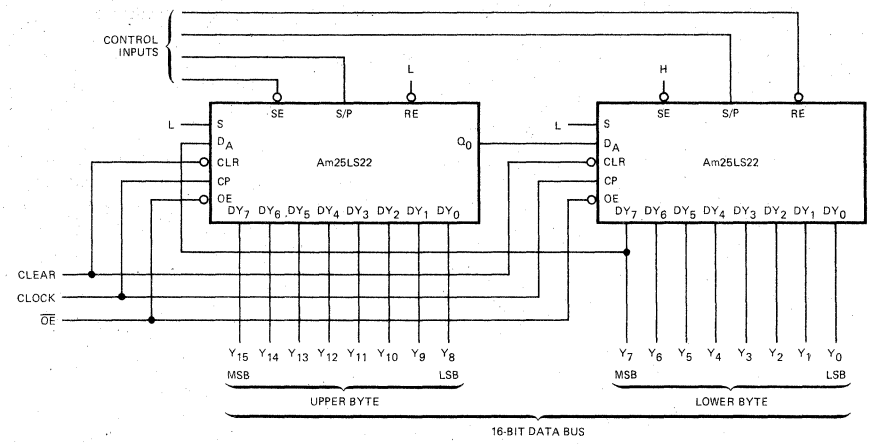
$\overline{OE}$ Output Control. When the $\overline{OE}$ input is HIGH, the eight DY_i outputs are in the high-impedance state. When $\overline{OE}$ is LOW, data in the eight flip-flops will be present at the register parallel outputs unless S/P is LOW.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

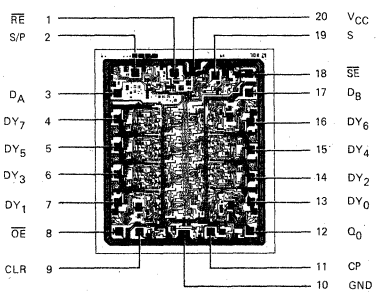
APPLICATION



SYSTEM OPERATION	Am25LS22 UPPER BYTE				Am25LS22 LOWER BYTE				FUNCTION
	$\overline{SE}$	S/P	$\overline{RE}$	$\overline{OE}$	$\overline{SE}$	S/P	$\overline{RE}$	$\overline{OE}$	Description
Load lower byte and extend lower byte sign to upper byte	H	H	L	X	X	L	L	X	Load from Bus
	L	H	L	H	X	X	H	H	7 clock cycles to extend sign
Load upper byte and extend upper byte sign while shifting value to lower byte position	X	L	L	X	X	X	X	X	Load from Bus
	H	H	L	H	H	H	L	H	8 clock cycles to extend upper byte sign and shift upper byte into lower byte position
Read 16-bit word to Bus	X	X	X	L	X	X	X	L	Unload

Two Am25LS22 8-bit registers can be used to perform the sign extend associated with two's complement 8-bit bytes for arithmetic operations in a 16-bit machine. If the upper byte value is to be used, it is shifted to the lower bit positions and its sign is extended. If the lower byte value is to be used, it is held in place while the sign is extended downward from the MSB position of the upper byte.

Metallization and Pad Layout



DIE SIZE 0.096" X 0.112"

Am25LS23

8-Bit Shift/Storage Register with Synchronous Clear

DISTINCTIVE CHARACTERISTICS

- Synchronous clear
- Three-state outputs
- Common input/output pins
- Cascadable shifting
- Second sourced by T.I. as 54LS/74LS323

RELATED PRODUCTS

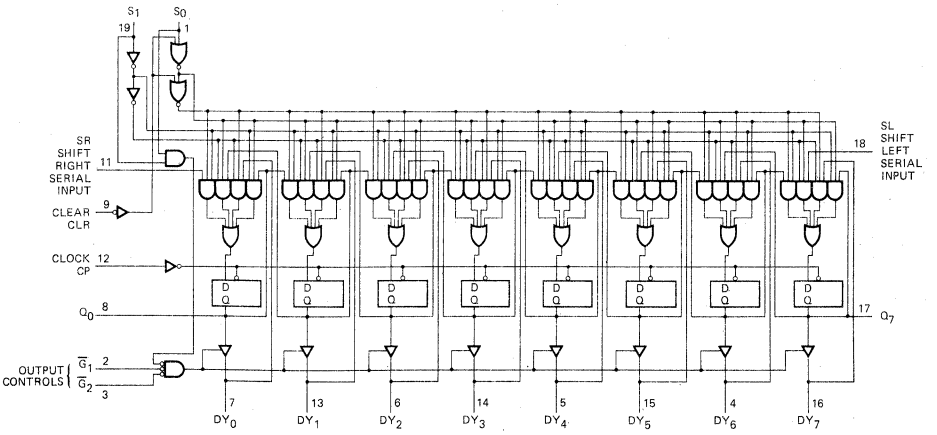
Part No.	Description
Am25LS22	8-Bit Serial/Parallel Register

FUNCTIONAL DESCRIPTION

The Am25LS23 is an 8-bit universal shift/storage register with 3-state outputs. The function is similar to the Am25LS299 with the exception of a synchronous clear function. Parallel load inputs and register outputs are multiplexed to allow the use of a 20-pin package. Separate continuous outputs are also provided for flip-flops Q_0 and Q_7.

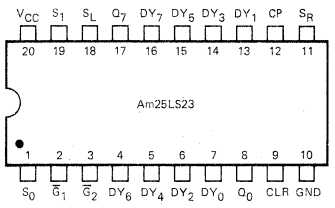
Four modes of operation are possible – Hold (store), Shift-left, Shift-right and Load Data. The Am25LS23 has a typical shift frequency of 50MHz. The Am25LS23 is packaged in a standard 20-pin package.

LOGIC DIAGRAM



CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0 to +70°C	AM25LS23PC
Hermetic DIP	0 to +70°C	AM25LS23DC
Dice	0 to +70°C	AM25LS23XC
Hermetic DIP	−55 to +125°C	AM25LS23DM
Hermetic Flat-Pak	−55 to +125°C	AM25LS23FM
Dice	−55 to +125°C	AM25LS23XM

ELECTRICAL CHARACTERISTICS The following conditions apply unless otherwise specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)				Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{OL}	Q_0, Q_7	$I_{OH} = -440\mu A$	MIL	2.5			Volts
					COM'L	2.7			
			DY_0-DY_7	MIL, $I_{OH} = -1.0mA$		2.4			
				COM'L, $I_{OH} = -2.6mA$		2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}		$I_{OL} = 4.0mA$			0.25	0.4	Volts
				$I_{OL} = 8.0mA$			0.35	0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs				2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			MIL			0.7	Volts
					COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$						−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$			S_0, S_1			−0.8	mA
					All others			−0.4	
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$ (Except DY_i)			S_0, S_1			40	µA
					All others			20	
I_I	Input HIGH Current	V_{CC} = MAX., (Except DY_i)	$V_{IN} = 7V$		S_0, S_1			0.2	mA
					$\overline{G}_1, \overline{G}_2$, CLR, CP			0.1	
			$V_{IN} = 5.5V$		Others			0.1	
I_{OZ}	Off-State (High Impedance) Output Current	V_{CC} = MAX.			$V_O = 0.4V$			−100	µA
					$V_O = 2.4V$			40	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.				−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 4)					38	60	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time.
4. I_{CC} – measured with clock input HIGH and output controls HIGH.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to $+V_{CC}$ max.
DC Input Voltage ($S_0, S_1, \overline{G}_1, \overline{G}_2$, CLR, CP)	−0.5V to +7.0V
DC Input Voltage (Others)	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

SWITCHING CHARACTERISTICS ($T_A = +25°C$, $V_{CC} = 5.0V$)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Q_0 or Q_7		18	26	ns	$C_L = 15pF$ $R_L = 2.0k\Omega$
t_{PHL}			23	28		
t_{PLH}	Clock to DY_i		18	26	ns	
t_{PHL}			21	28		
t_s	S_1, S_0 Set-up Prior to Clock	12			ns	
t_s	DY_i or S_R, S_L Set-up Prior to Clock	12			ns	
t_{PW}	Pulse Width (Clock)	15			ns	
t_s	Clear to Clock	15			ns	
t_{ZH}	$S_1, S_0, \overline{G}_1, \overline{G}_2$ to DY_i		18	30	ns	
t_{ZL}			20	30		
t_{LZ}	$S_1, S_0, \overline{G}_1, \overline{G}_2$, to DY_i		22	33	ns	$C_L = 5.0pF$ $R_L = 2.0k\Omega$
t_{HZ}			16	23		
f_{max}	Maximum Clock Frequency (Note 1)	35	50		MHz	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Clock to Q_0 or Q_7		38		44	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}			40		47		
t_{PLH}	Clock to DY_i		38		44	ns	
t_{PHL}			40		47		
t_s	S_1, S_0 Set-up Prior to Clock	20		23		ns	
t_s	DY_i or S_R, S_L Set-up Prior to Clock	20		23		ns	
t_{pw}	Pulse Width (Clock)	24		27		ns	
t_s	Clear to Clock	24		27		ns	
t_{ZH}	S_1, S_0, $\overline{G}_1$, $\overline{G}_2$ to DY_i		43		50	ns	
t_{ZL}			43		50		
t_{LZ}	S_1, S_0, $\overline{G}_1$, $\overline{G}_2$ to DY_i		43		50	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{HZ}			30		35		
f_{max}	Maximum Clock Frequency (Note 1)	26		23		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

S_R Shift right data input to Q_7

S_L Shift left data input to Q_0

Clear Active LOW synchronous input forcing the Q_0 through Q_7 register to see LOW conditions, visable only if outputs are enabled

Clock A LOW-to-HIGH transition will result in the register changing state to next state as described by mode and input data condition

S_0, S_1 Mode selection control lines used to control input (output during load) conditions

$\overline{G}_1$, $\overline{G}_2$ Active LOW input to control three-state output in active LOW AND configuration

Q_0, Q_7 The only two direct outputs; used to cascade shift operations

DY_0–DY_7 Input/Output line dependent on mode and output control. Input only with mode select LOAD. Output in all other modes but subject to output select ($\overline{G}_1$, $\overline{G}_2$).

TRUTH TABLE

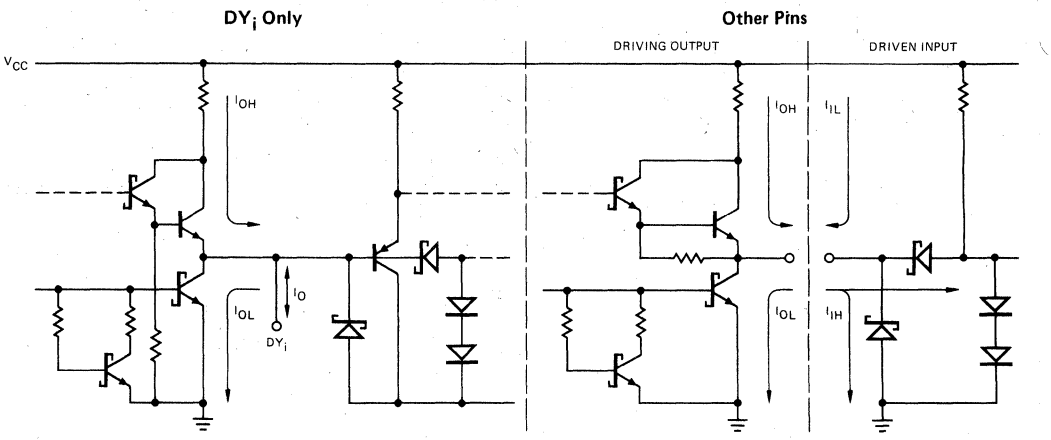
FUNCTION		INPUTS S_R	S_L	CLEAR	CLOCK	S_0	S_1	$\overline{G}_1$	$\overline{G}_2$	OUTPUTS Q_0	Q_7	INPUTS/OUTPUTS DY_0	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6	DY_7
Clear		X	X	L	↑	(Note 1)		L	L	L	L	L	L	L	L	L	L	L	L
Output Control		X	X	X	X	X	X	H	L	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
		X	X	X	X	X	X	L	H	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
		X	X	X	X	X	X	H	H	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
	Hold	X	X	H	X	L	L	L	L	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
M	Load (Note 2)	X	X	H	↑	H	H	L	L	A	H	A	B	C	D	E	F	G	H
O	Shift Right	L	X	H	↑	H	L	L	L	L	DY_6	L	DY_0	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6
D	Shift Right	H	X	H	↑	H	L	L	L	H	DY_6	H	DY_0	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6
E	Shift Left	X	L	H	↑	L	H	L	L	DY_1	L	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6	DY_7	L
	Shift Left	X	H	H	↑	L	H	L	L	DY_1	H	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6	DY_7	H

L = LOW, H = HIGH, Z = High Impedance, X = Don't Care, ↑ = Transition LOW-to-HIGH, NC = No Change

Notes: 1. Either LOW to observe outputs.
2. In this mode DY_i are inputs.

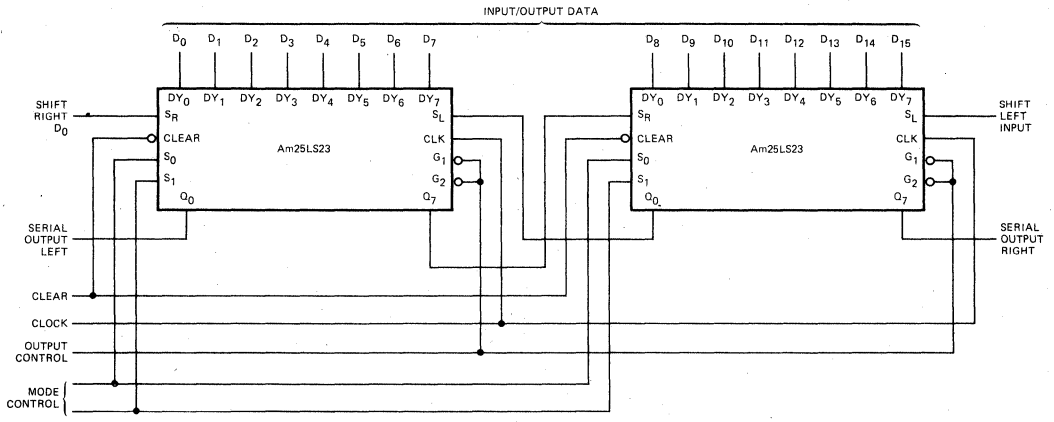
9

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



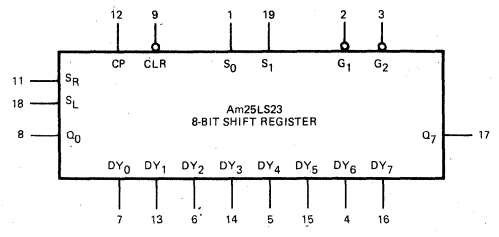
Note: Actual current flow direction shown.

APPLICATION



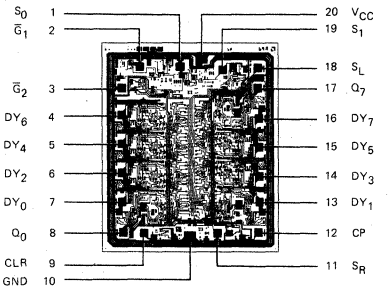
16-Bit Cascaded Parallel Load/Unload Shift Right/Left Register.

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

Metallization and Pad Layout



DIE SIZE: 0.096" X 0.112"

Am25S557 • Am25S558

Eight-Bit by Eight-Bit Combinatorial Multiplier

DISTINCTIVE CHARACTERISTICS

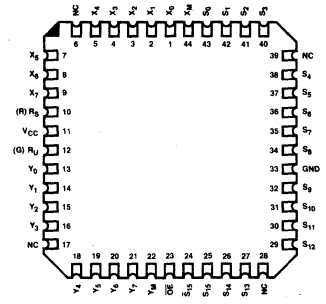
- Multiplies two 8-bit numbers – 16-bit output
- Combinatorial – no clocks required
- Full 8 x 8 multiply in 45ns typ.
- Cascades to 16 x 16 in 110ns typ.
- Expandable to multiples of 8 bits
- MSB and $\overline{\text{MSB}}$ outputs for easy expansion
- Unsigned, two's complement or mixed operands
- Implements common rounding algorithms with additional logic
- Three-state outputs
- Transparent 16-bit latch in Am25S557
- Industry standard pin-outs

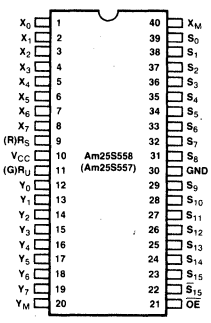
RELATED PRODUCTS

Part No.	Description
Am29516/7	16 by 16-Bit Multiplier
Am25S05	4 by 2-Bit Multiplier
Am25LS14A	8-Bit Serial/Parallel Multiplier
Am25LS2516	8 by 8-Bit Serial/Parallel Multiplier

CONNECTION DIAGRAMS – Top Views

Leadless Chip Carrier
L-44-1





Pin assignments shown are for Am25S558. G and R shown in parentheses are pin assignments for Am25S557.

BLI-036

FUNCTIONAL DESCRIPTION

The Am25S557 and Am25S558 are high-speed, combinatorial, 8 x 8-bit multipliers. Both use an array of full adders to form and add partial products in a single unclocked operation, resulting in a 16-bit parallel output product.

Mode control inputs X_M and Y_M allow the multiplier to accept either unsigned or two's complement numbers from either respective input to provide an unsigned or signed output. The mode control lines are held LOW for unsigned input words and HIGH for two's complement.

The Am25S557 and Am25S558 are easily expandable to longer work lengths. Both S_{15} and $\overline{S}_{15}$ are available to allow expansion in either signed or unsigned modes without external inverters. In the 16-bit by 16-bit configuration (32-bit output) the typical multiply time is 110ns.

Both configurations offer three-state output flexibility and the Am25S557 adds a 16-bit transparent latch between the multiplier array and the three-state output buffers (including $\overline{S}_{15}$).

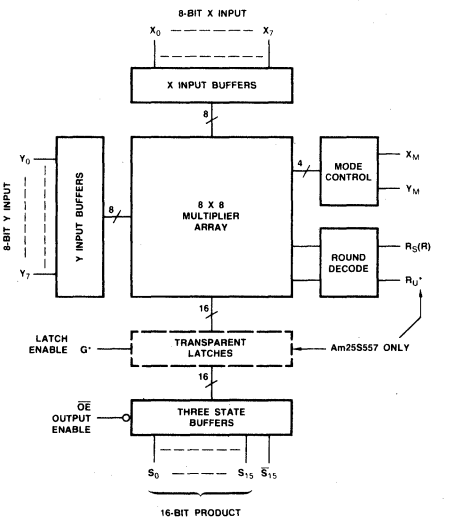
Rounding provisions for 8-bit truncated output configurations are particularly optimized for maximum flexibility. The Am25S557 internally develops proper rounding for either signed or unsigned numbers by combining rounding input R with X_M, Y_M, $\overline{X}_M$ and $\overline{Y}_M$ as follows:

$R_U = \overline{X}_M \cdot \overline{Y}_M \cdot R$ = Unsigned Rounding input to 2^7 adder.

$R_S = (X_M + Y_M)\ R$ = Signed Rounding input to 2^6 adder.

Since the Am25S558 does not require the use of pin 9 for the latch enable input, (G), R_S and R_U are brought out separately.

LOGIC DIAGRAM



*Pin 11 is G for Am25S557 and R_U for Am25S558.

BLI-037

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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (MIN. = 4.75V MAX. = 5.25V)
MIL T_C = −55°C to +125°C V_{CC} = 5.0V ±10% (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	V_{IL} = 0.8V V_{IH} = 2.0V	I_{OH} = −2.0mA	2.4	3.0		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	V_{IL} = 0.8V V_{IH} = 2.0V I_{OL} = 8.0mA			0.3	0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.8	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V					−1.0	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V					100	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	V_O = 0.5V				−100	μA
			V_O = 2.4V				+100	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−20		−90	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.					280	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test with pin 21 at 4.5V, all other input pins at GND, all outputs open Am25S557 conditions the same except initialize with G (pin 11) at 4.5V, then GND.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

Am25S557 SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

		Am25S COM'L T_A = 0 to 70°C V_{CC} = 5V ±5%			Am25S MIL T_A = −55 to +125°C V_{CC} = 5V ±10%				
Parameters	Description	Min	Typ	Max	Min	Typ	Max	Units	Test Conditions
t_{PD}	X_i, Y_i to S_0 to S_7		45	60		55	70	ns	C_L = 30pF R_L = 560Ω (See test figures)
t_{PD}	X_i, Y_i to S_8 to S_{15} or $\overline{S}_{15}$		50	80		60	90	ns	
t_s	X_i, Y_i to G Set-up Time	65			75			ns	
t_h	X_i, Y_i to G Hold Time	−5			−5			ns	
t_{PD}	G to S_i		30	45		30	50	ns	
t_{PW}	Latch Enable Pulse Width	25	15		30	15		ns	
t_{PHZ}	$\overline{OE}$ to S_0 to S_{15}		15	30		15	40	ns	
t_{PHZ}	$\overline{OE}$ to $\overline{S}_{15}$		25	40		25	50	ns	
t_{PLZ}	$\overline{OE}$ to S_i		15	30		15	40	ns	
t_{PZH}	$\overline{OE}$ to S_i		20	35		20	40	ns	
t_{PZL}	$\overline{OE}$ to S_i		20	35		20	40	ns	

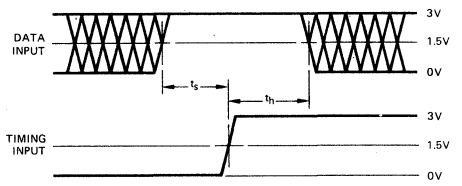
*AC performance over the operating temperature range is guaranteed by testing defined in Group A, subgroup 9.

Am25S557 • Am25S558
SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

		Am25S COM'L T_A = 0 to 70°C V_{CC} = 5V ±5%			Am25S MIL T_A = −55 to +125°C V_{CC} = 5V ±10%				
Parameters	**Description**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
t_{PD}	X_i, Y_i to S_0 to S_7		35	55		35	65	ns	C_L = 30pF R_L = 560Ω (See test figures)
t_{PD}	X_i, Y_i to S_8 to S_{15} or $\overline{S}_{15}$		55	75		55	85	ns	
t_{PHZ}	$\overline{OE}$ to S_0 to S_{15}		15	30		15	40	ns	
t_{PHZ}	$\overline{OE}$ to $\overline{S}_{15}$		25	40		25	50	ns	
t_{PLZ}	$\overline{OE}$ to S_i		15	30		15	40	ns	
t_{PZH}	$\overline{OE}$ to S_i		20	35		20	40	ns	
t_{PZL}	$\overline{OE}$ to S_i		20	35		20	40	ns	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, subgroup 9.

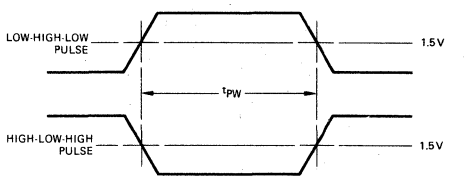
SET-UP AND HOLD TIMES



BLI-057

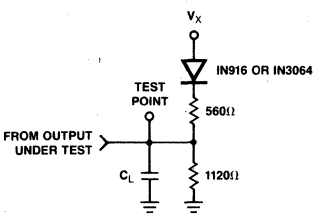
Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

PULSE WIDTH



BLI-058

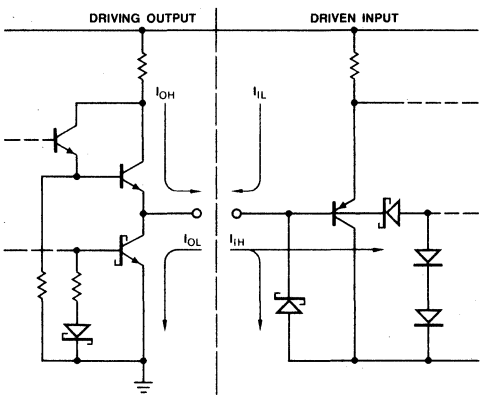
LOAD TEST CIRCUIT



BLI-059

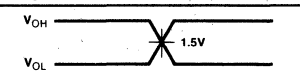
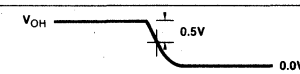
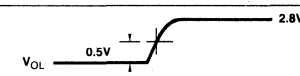
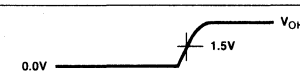
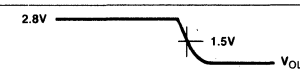
C_L Includes probe and jig capacitance.

Am25S557 • Am25S558
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



BLI-038

TEST WAVEFORMS

Test	V_X	Output Waveform – Measurement Level
All t_{PD}s	5.0V	
t_{PHZ}	0.0V	
t_{PLZ}	5.0V	
t_{PZH}	0.0V	
t_{PZL}	5.0V	

9

DEFINITION OF TERMS

X_0-X_7	Multiplicand 8-bit data inputs
Y_0-Y_7	Multiplier 8-bit data inputs
X_M, Y_M	Mode control inputs for each data word; LOW for unsigned data and HIGH for two's complement data
S_0-S_{15}	Product 16-bit output
$\overline{S_{15}}$	Inverted MSB for expansion
R_S, R_U	Rounding inputs for signed and unsigned data, respectively (Am25S558 only)
G	Transparent Latch Enable (Am25S557 only)
$\overline{OE}$	Three-state enable for S_0-S_{15} outputs
R	Rounding input for signed or unsigned data (combined internally with X_M, Y_M in Am25S557 only)

MODE CONTROL INPUTS

Operating Mode	Input Data		Mode Control Inputs	
	X_0-X_7	Y_0-Y_7	X_M	Y_M
UNSIGNED	UNSIGNED	UNSIGNED	L	L
MIXED	UNSIGNED	2's COMP	L	H
	2's COMP	UNSIGNED	H	L
SIGNED	2's COMP	2's COMP	H	H

ROUNDING INPUTS

Am25S557

Inputs			Adds	
X_M	Y_M	R	2^7	2^6
L	L	H	YES	NO
L	H	H	NO	YES
H	L	H	NO	YES
H	H	H	NO	YES
X	X	L	NO	NO

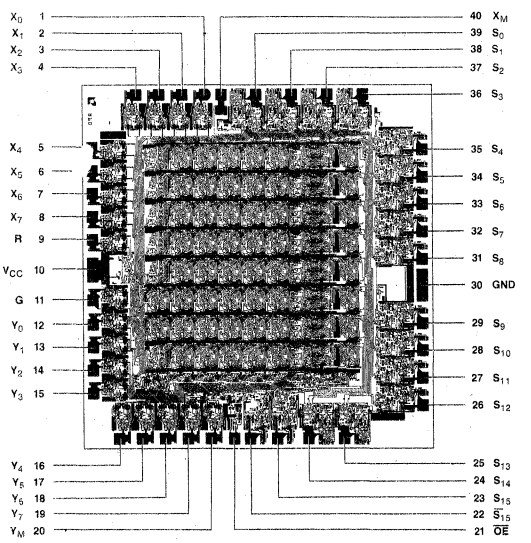
Am25S558

Inputs		Adds		Normally Used With	
R_U	R_S	2^7	2^6	X_M	Y_M
L	L	NO	NO	X	X
L	H	NO	YES	$X_M + Y_M = H$	
H	L	YES	NO	L	L
H	H	YES	YES	*	*

* Most rounding applications require a HIGH level for R_U or R_S, but not both.

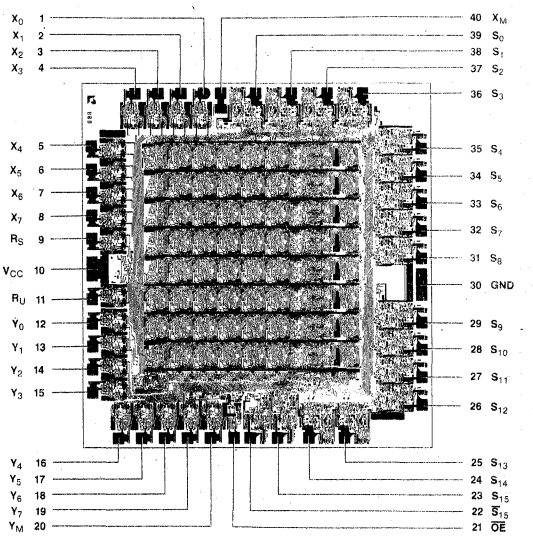
Metallization and Pad Layouts

Am25S557



DIE SIZE 0.171" X 0.165"

Am25S558



DIE SIZE 0.171" X 0.165"

APPLICATION

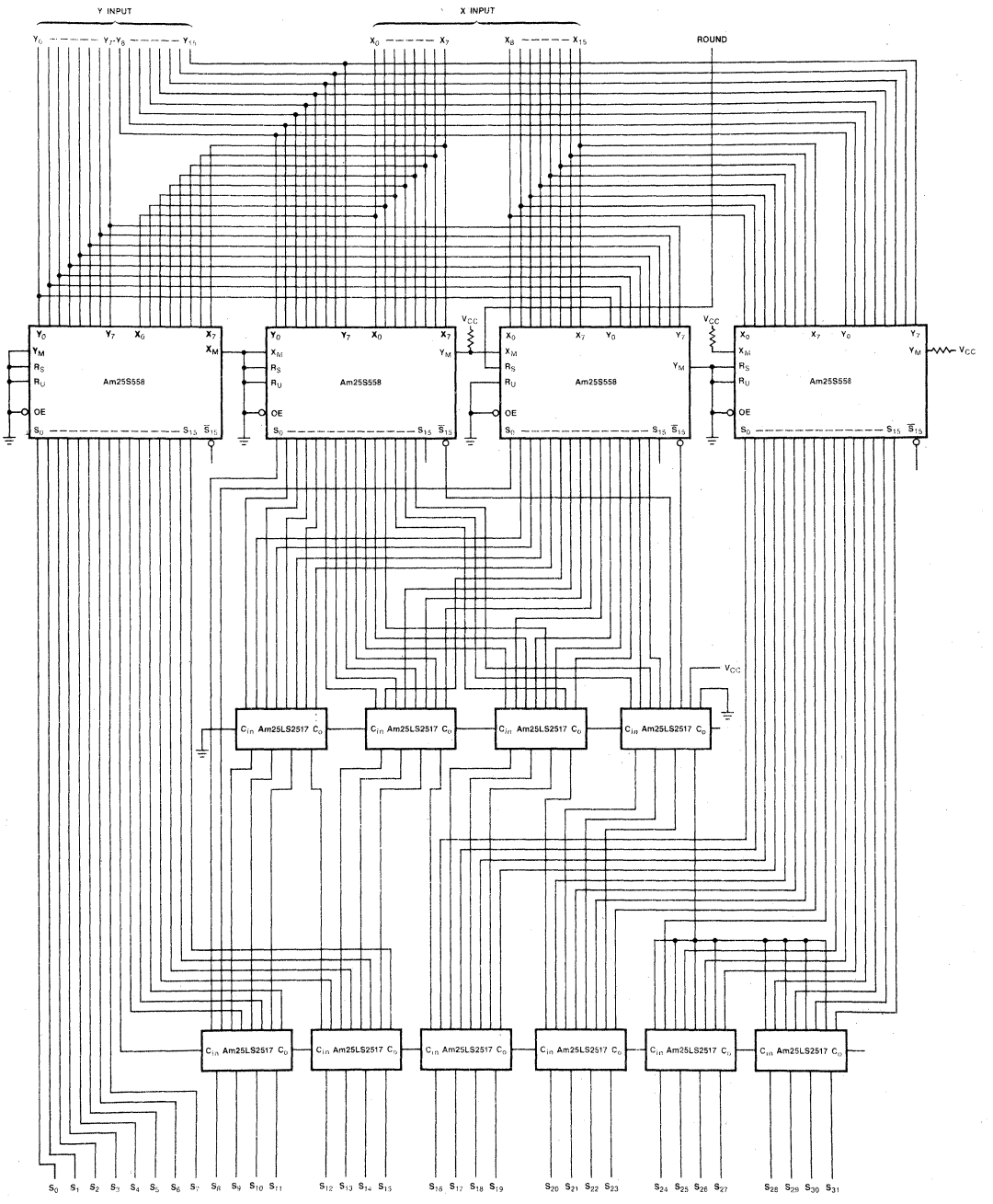
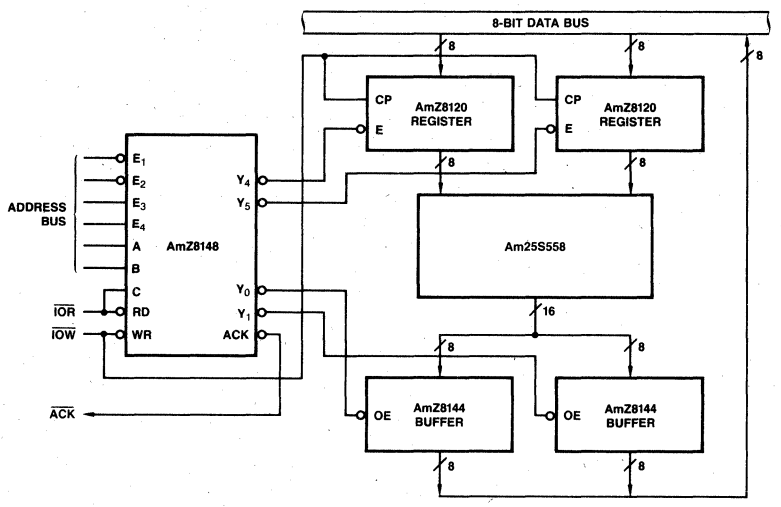


Figure 2. High-Speed 16 x 16 2's Complement Multiplication.

BLI-040

I/O MAPPED INTERFACE WITH MOS MICROPROCESSOR



BLI-060

ORDERING INFORMATION

Package Type	Temperature Range	Am25S557 Order Number	Am25S558 Order Number
Hermetic DIP	0 to +70°C	AM25S557DC	AM25S558DC
	−55 to +125°C	AM25S557DM	AM25S558DM
Leadless	0 to +70°C	AM25S557LC	AM25S558LC
	−55 to +125°C	AM25S557LM	AM25S558LM

Am25S557 • Am25S558 Multipliers in Expanded Arrays

By Bernie New and David Anderson

GENERAL DESCRIPTION

The Am25S557 and Am25S558 are high-speed, combinatorial, 8 x 8-bit multipliers. Both use an array of gated full adders to form and add simultaneously the partial products necessary to generate a parallel product.

Both devices have two Mode Control inputs X_m and Y_m. These controls allow multiplying any of the four combinations of unsigned or two's complement numbers.

The availability of $\overline{S}_{15}$ (inverted MSB) and the capability of operating with either signed or unsigned inputs means the Am25S557 and Am25S558 can be easily expanded to larger array sizes which can similarly multiply signed or unsigned numbers.

In addition to the three-state output flexibility of both devices the Am25S557 adds a transparent latch between the multiplier array and the output buffers.

Both multipliers incorporate rounding provisions; both use a standard 40-pin package; and both are available in commercial or military version.

INTRODUCTION

There are various methods of implementing large number multiplication by using the Am25S557 and Am25S558 multipliers. In high-speed applications a parallel array of multipliers will generate an output product in the shortest time. However, this approach also requires a large parts count. A partial parallel expansion sacrifices some speed for a reduced parts count, while a single multiplier performing repetitive multiplications requires the smaller number of parts but is slow when multiplying large numbers.

The Am25S557 includes a transparent product output latch useful in pipelined applications (Figure 1). In such an application, the result of a current multiply may be held for use by other parts of the system while the next multiply is already in progress.

This application note explains how to implement both parallel and partial parallel expansion to form large multiplier arrays using the Am25S557 or Am25S558 as the basic building block. A brief discussion on multiplier arithmetic is first presented to clarify operation of the part. For a complete functional description see the Am25S557/558 data sheet.

ARITHMETIC

Mode control inputs X_m and Y_m (Figure 1) allow the multiplier to accept either unsigned or two's complement numbers at either X or Y input. These controls are necessary to tell the part how to interpret the input data since the multiplier can't tell from the number alone. If either input is in two's complement form, the result will necessarily be two's complement. Only if both operands are unsigned will the product be unsigned.

For example, the binary number 11111111 may be interpreted as 255 or −1 depending on the number convention used − unsigned or two's complement. Similarly, 11111110 is 254 or −2. The mode controls tell the multiplier which one is appropriate.

If these inputs are used, the following four interpretations are possible:

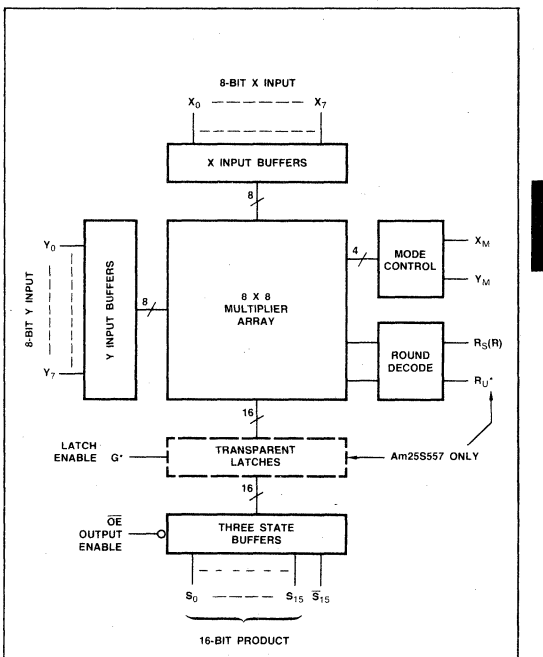
255 x 254 = +64770, 1111110100000010 (unsigned)
(−1) x 254 = −254, 1111111100000010 (2's complement)
255 x (−2) = −510, 1111111000000010 (2's complement)
(−1) x (−2) = +2, 0000000000000010 (2's complement)

All four of these different answers are correct.

Two round controls (R_s and R_u) are provided on the Am25S558. R_s indicates signed number rounding and R_u indicates unsigned number rounding. In signed number rounding a bit is added with the same weight as S_6. This allows S_{14-7} to be used as the rounded 8-bit output (Figure 2). In unsigned multiplication, R_u adds a bit with the weight of S_7. S_{15-8} may then be used as the 8-bit unsigned output (Figure 3). The Am25S557 internally develops the appropriate rounding control R_s or R_u by combining rounding input R with X_m and Y_m as follows:

$$R_u = \overline{X_m} \cdot \overline{Y_m} \cdot R$$
$$R_s = (X_m + Y_m) \cdot R$$

This frees a pin for use as the latch enable (G).



*Pin 11 is G for Am25S557 and R_u for Am25S558.

Figure 1. Logic Diagram

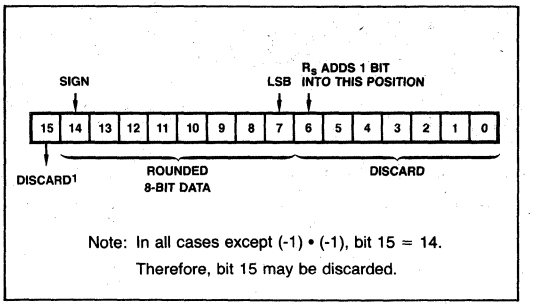


Figure 2. Rounding 16-Bit Signed Number for 8-Bit Signed Output Data

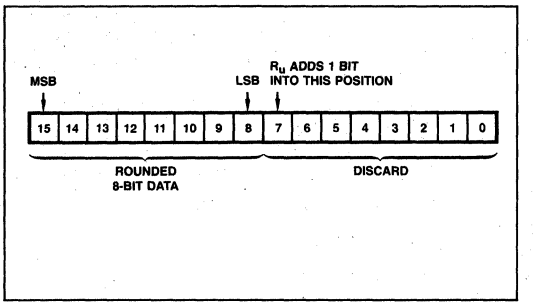


Figure 3. Rounding 16-Bit Unsigned Number for 8-Bit Unsigned Output Data

PARALLEL EXPANSION

The Am25S558 is specifically designed for ease of expansion. To multiply 8n bits by 8m bits requires n • m multiplications. These may either be performed successively in a single multiplier or n • m multipliers may be used in parallel. A combination of the two approaches, partial parallel expansion, is also possible. A 24 x 24-bit unsigned product using parallel multipliers can be fabricated as follows:

1. Split each of the 24-bit inputs into 8-bit groups. X would split into XA, XB, XC where
   $XA_{0-7} = X_{16-23}$
   $XB_{0-7} = X_{8-15}$
   $XC_{0-7} = X_{0-7}$

   The relationship between X and the groups is
   $X = 2^{16} XA + 2^{8} XB + XC$

2. Treating Y in the same way
   $Y = 2^{16} YA + 2^{8} YB + YC$

3. The required multiplication is
   $XY = (2^{16} XA + 2^{8} XB + XC) \cdot (2^{16} YA + 2^{8} YB + YC)$
   $= 2^{32} XA \cdot YA + 2^{24} XA \cdot YB + 2^{16} XA \cdot YC + 2^{24} XB \cdot YA + 2^{16} XB \cdot YB + 2^{8} XB \cdot YC + 2^{16} XC \cdot YA + 2^{8} XC \cdot YB + XC \cdot YC$

   This requires nine multiplies.

4. Shift the partial products to weight them with the appropriate power of 2 and sum them.

Slower, low-cost systems can be implemented with a single multiplier but the fastest approach uses nine multipliers in a parallel array (Figure 4).

A signed 24 by 24-bit multiplier is configured basically the same way, but consideration must be given to which of the 8-bit groups are signed or unsigned. In the 24-bit word, the sign is weighted negatively and the other bits are weighted positively. In the 8-bit groups only XA and YA have negatively weighted most significant bits (MSBs); the other groups are all positive (unsigned). It follows, therefore, the XA and YA are signed two's complement numbers and XB, XC, YB and YC are positive unsigned numbers.

When generating the partial products, the mode controls must be connected appropriately. If either or both of the groups multiplied to form a partial product are a signed number, then the partial product is also a signed number and must be sign extended in any addition.

Partial Parallel Expansion

Another way to perform multiplications of numbers with more than 8 bits is to use partial parallel expansion. Here the multiplier array is expanded for only one operand. The following example constructs a 32 x 32-bit multiplier using a four-step sequence of 8 x 32 multiplies. An 8 by 32-bit multiply is performed using four Am25S558s (Figure 5).

X is split into XA, XB, XC, XD where

$XA = X_{24-31}$
$XB = X_{16-23}$
$XC = X_{8-15}$
$XD = X_{0-7}$

The relationship between them is

$X = 2^{24}XA + 2^{16}XB + 2^{8}XC + XD$

Y is treated the same way

$Y = 2^{24}YA + 2^{16}YB + 2^{8}YC + YD$

In this example the multiplier array can only accept 8 bits on the Y inputs. Therefore, the partial Y operands are applied to the multiplier array sequentially. The multiplication performed at each step is as follows:

Sequence

St1	$YD \cdot (2^{24}XA + 2^{16}XB + 2^{8}XC + XD)$
St2	$2^{8}YC \cdot (2^{24}XA + 2^{16}XB + 2^{8}XC + XD)$
St3	$2^{16}YB \cdot (2^{24}XA + 2^{16}XB + 2^{8}XC + XD)$
St4	$2^{24}YA \cdot (2^{24}XA + 2^{16}XB + 2^{8}XC + XD)$

The partial products from each step are next shifted to weight them with the appropriate power of 2. They are then summed to form the final 64-bit product (Figure 6).

Multiplexing

For extremely fast 8 x 8 multiplication, two or more Am25S558s may be multiplexed as shown in Figure 7. Input latches hold both the X and Y input data for each multiplier until a combinatorial product output is generated. The product from each multiplier is multiplexed onto the output bus, using the three-state enable control, $\overline{OE}$, on the multiplier.

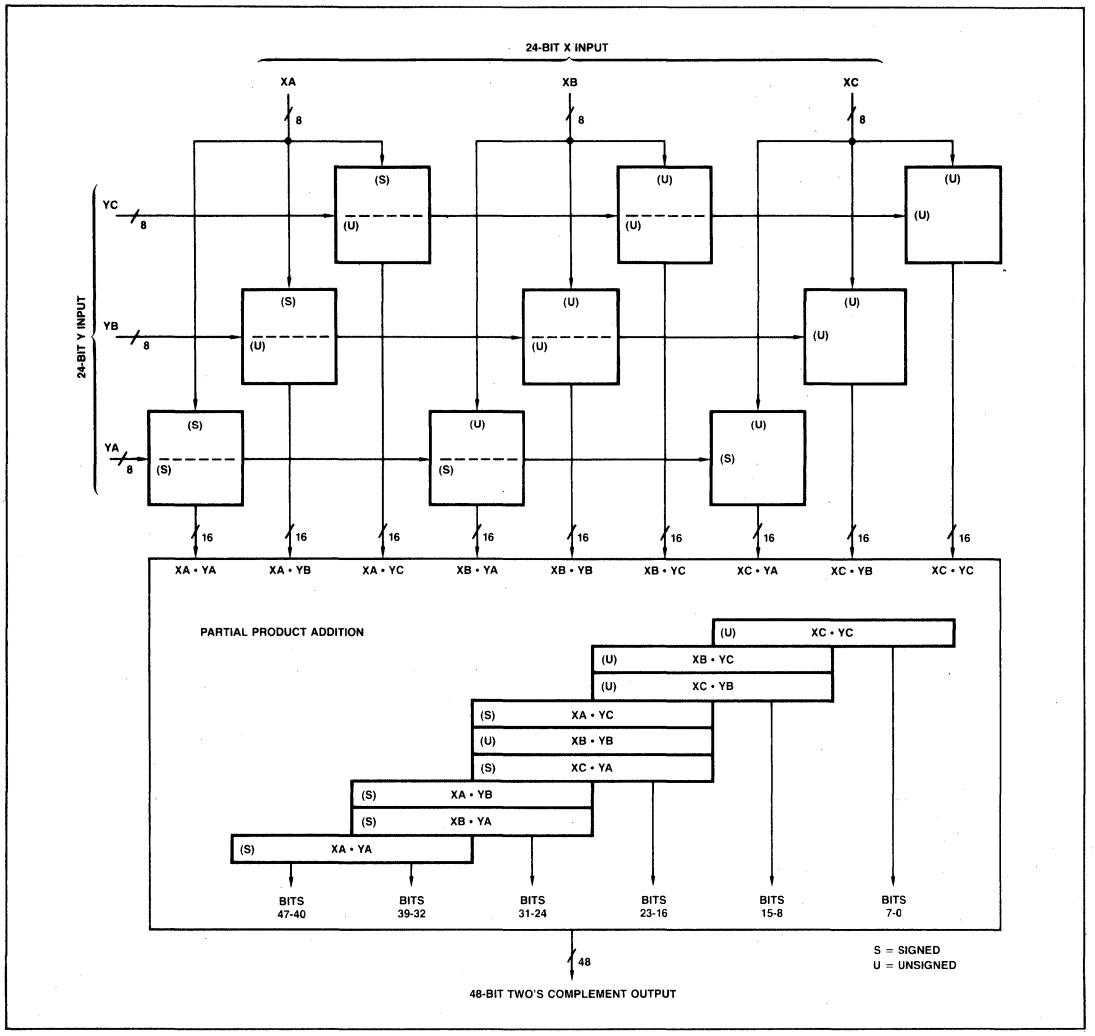
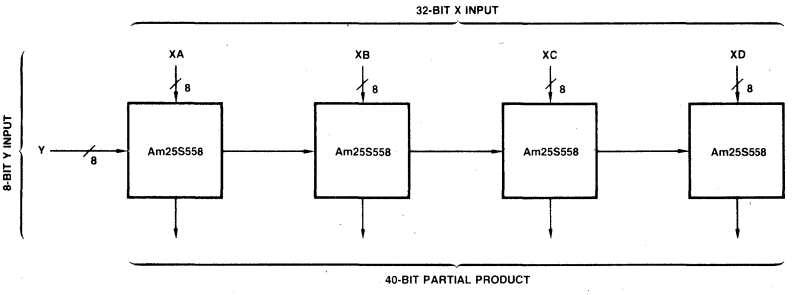


Figure 4. Two's Complement 24-Bit by 24-Bit Multiplier Array



The Y 8-bit partial operands YA, YB, YC, YD are loaded and multiplied by the entire 32-bit operand X in four steps to obtain a full 64-bit product.

Figure 5. 32 x 32-Bit Multiplier Array Partial Parallel Expansion

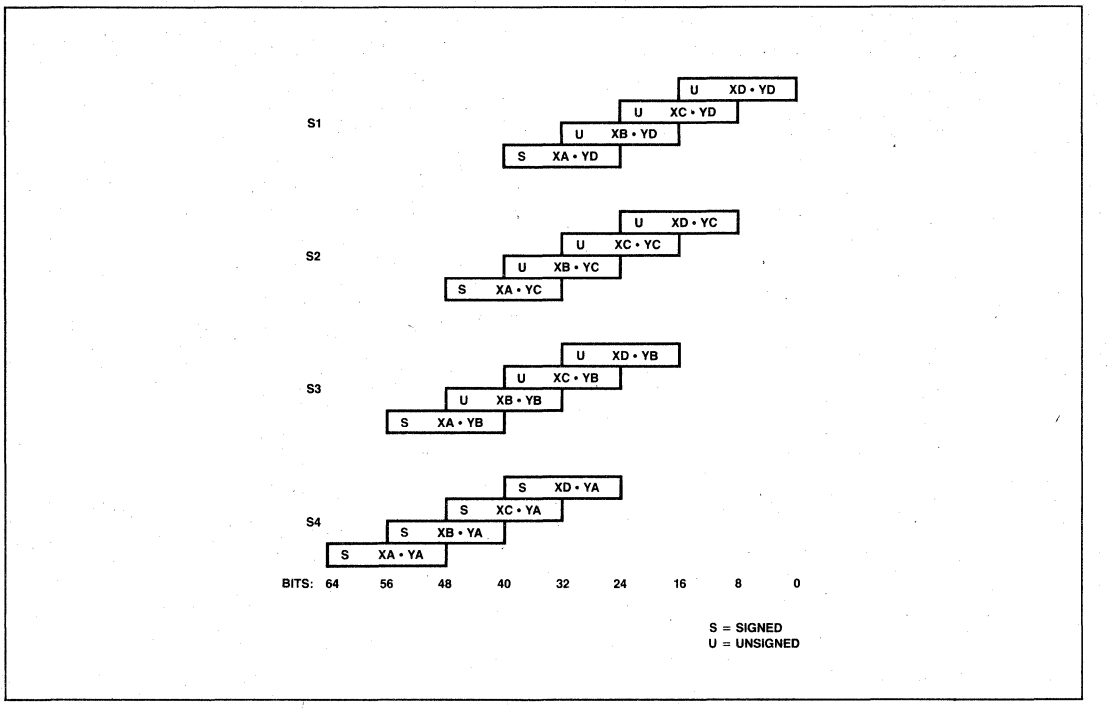


Figure 6. 32 x 32-Bit Serial/Parallel Expansion

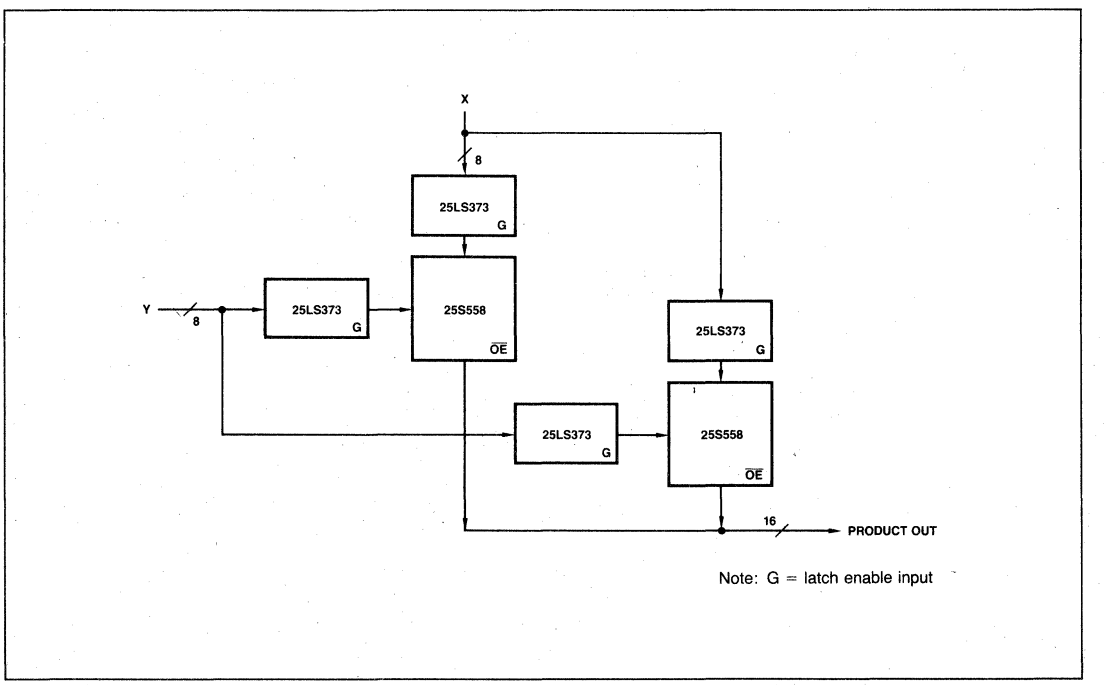


Figure 7. High-Speed Multiplexed 8 x 8-Bit Multiplication

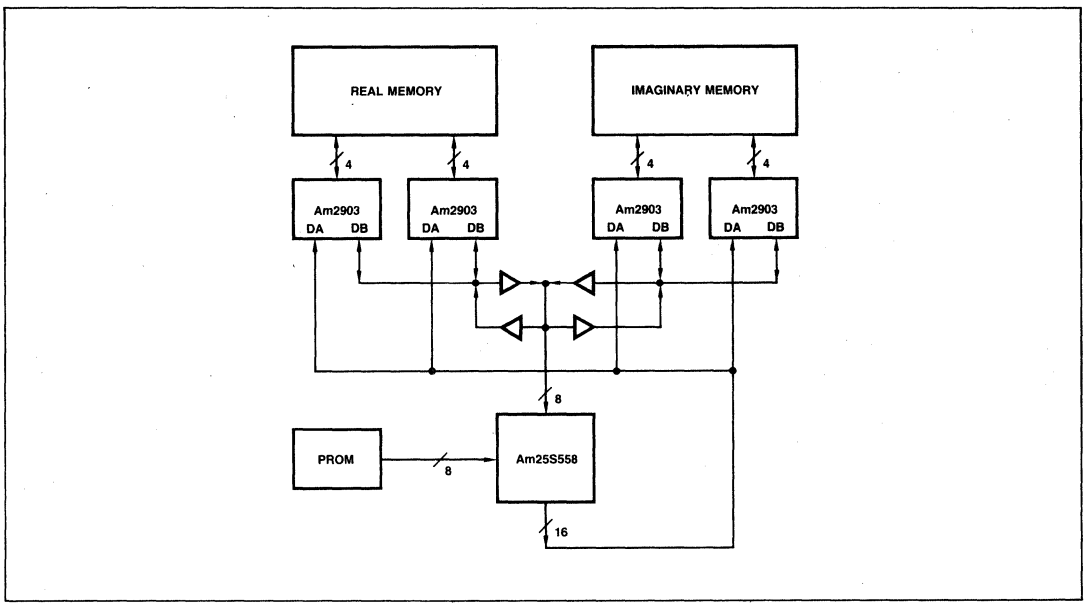


Figure 8. Block Diagram of a High-Performance Signal Processing System

Application

In many signal processing algorithms such as fast Fourier transforms (FFTs), finite impulse response (FIR) and infinite impulse response (IIR) digital filters, there is a need to perform fast repetitive multiplication. For off-line or low bandwidth applications, these computations could be performed in a general-purpose computer or even microcomputer. However, in any high-performance system, a dedicated, or at least an optimized processor must be constructed. Only microprogrammed, bipolar bit-slice devices provide the speed and flexibility necessary for such a processor.

Figure 8 is a block diagram of a typical high-performance system. The diagram shows how two pairs of Am2903s can be used in conjunction with a single Am25S558 Multiplier. The real or imaginary data may be entered into the multiplier, multiplied by a real or imaginary constant from the PROM and returned to the real or imaginary ALU as appropriate. The link between the DB ports also allows for a simple transfer of data which represents a multiplication by $\sqrt{-1}$.

Am25LS2513

Three-State Priority Encoder

DISTINCTIVE CHARACTERISTICS

- Encodes eight lines to three-line binary
- Expandable
- Cascadable
- Three State inverted output version of Am54LS/74LS/25LS148
- Gated three-state output
- Advanced Low-Power Schottky processing

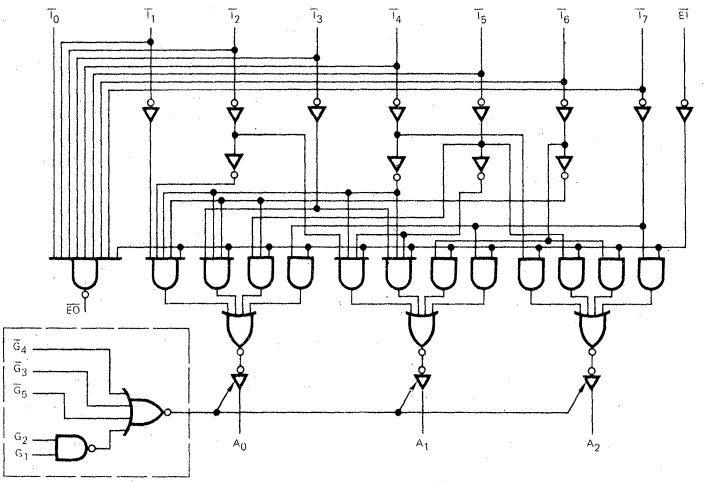
RELATED PRODUCTS

Part No.	Description
Am2913	Priority Interrupt Expander
Am2914	Vectored Priority Interrupt Controller

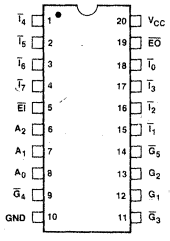
FUNCTIONAL DESCRIPTION

The Am25LS2513 Low-Power Schottky Priority Encoder performs priority encoding of 8 inputs to provide a binary-weighted code of the priority order of the 3 tri-state active HIGH outputs A_0, A_1, A_2. Three active LOW and two active HIGH inputs in AND-OR configuration allow control of the tri-state outputs. The use of the input enable ($\overline{EI}$) combined with the enable output ($\overline{EO}$) permits cascading without additional circuitry. Enable input ($\overline{EI}$) HIGH will force all outputs LOW subject to the tri-state control. The enable output is LOW when all inputs $\overline{I_0}$ through $\overline{I_7}$ are HIGH and the enable input is LOW.

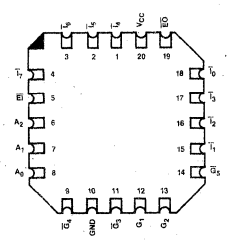
LOGIC DIAGRAM



CONNECTION DIAGRAMS – Top Views

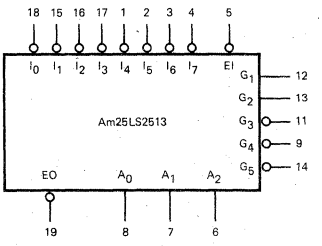


Leadless Chip Carrier
L-20-1



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



Am25LS2513

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75V MAX. = 5.25V

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50V MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	A_i	MIL, $I_{OH} = -1.0mA$	2.4	3.4		Volts
				COM'L, $I_{OH} = -2.6mA$	2.4	3.2		
			$\overline{EO}$, $I_{OH} = -440\mu A$	MIL	2.5	3.4		
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$				0.4	Volts
			$I_{OL} = 8.0mA$				0.45	
			$I_{OL} = 12mA (A_n$ Outputs)				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$	$\overline{E1}, G_1, G_2, \overline{G_3}, \overline{G_4}, \overline{G_5}, \overline{I_0}$				−0.4	mA
			All others				−0.8	
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$	$\overline{E1}, G_1, G_2, \overline{G_3}, \overline{G_4}, \overline{G_5}, \overline{I_0}$				20	μA
			All others				40	
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$	$\overline{E1}, G_1, G_2, \overline{G_3}, \overline{G_4}, \overline{G_5}, \overline{I_0}$				0.1	mA
			All others				0.2	
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$				−20	μA
			$V_O = 2.4V$				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				15	24	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All inputs and outputs open.

9

Am25LS

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to $+V_{CC}$ max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

Am25LS13
SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	$\overline{I}_i$ to A_n (In-phase)		17	25	ns	C_L = 15pF R_L = 2.0kΩ
t_{PHL}			17	25		
t_{PLH}	$\overline{I}_i$ to A_n (Out-phase)		11	17	ns	
t_{PHL}			12	18		
t_{PLH}	$\overline{I}_i$ to $\overline{EO}$		7.0	11	ns	
t_{PHL}			24	36		
t_{PLH}	$\overline{EI}$ to $\overline{EO}$		11	17	ns	
t_{PHL}			23	34		
t_{PLH}	$\overline{EI}$ to A_n		12	18	ns	
t_{PHL}			14	21		
t_{ZH}	G_1 or G_2 to A_n		23	40	ns	
t_{ZL}			20	37		
t_{ZH}	$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to A_n		20	30	ns	
t_{ZL}			18	27		
t_{HZ}	G_1 or G_2 to A_n		17	27	ns	C_L = 5.0pF R_L = 2.0kΩ
t_{LZ}			19	28		
t_{HZ}	$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to A_n		16	24	ns	
t_{LZ}			18	27		

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5%		Am25LS MIL T_A = –55°C to +125°C V_{CC} = 5.0V ±10%		Units	Test Conditions
		Min.	Max.	Min.	Max.		
t_{PLH}	$\overline{I}_i$ to A_n (In-phase)		31		37	ns	C_L = 50pF R_L = 2.0kΩ
t_{PHL}			30		34		
t_{PLH}	$\overline{I}_i$ to A_n (Out-phase)		22		27	ns	
t_{PHL}			22		25		
t_{PLH}	$\overline{I}_i$ to $\overline{EO}$		15		18	ns	
t_{PHL}			48		60		
t_{PLH}	$\overline{EI}$ to $\overline{EO}$		19		21	ns	
t_{PHL}			46		57		
t_{PLH}	$\overline{EI}$ to A_n		22		25	ns	
t_{PHL}			27		32		
t_{ZH}	G_1 or G_2 to A_n		42		49	ns	
t_{ZL}			43		49		
t_{ZH}	$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to A_n		36		43	ns	
t_{ZL}			35		43		
t_{HZ}	G_1 or G_2 to A_n		34		40	ns	C_L = 5.0pF R_L = 2.0kΩ
t_{LZ}			34		40		
t_{HZ}	$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$ to A_n		30		35	ns	
t_{LZ}			31		35		

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Note: i = 0 to 7
n = 0 to 2

DEFINITIONS OF FUNCTIONAL TERMS

A0, A1, A2	Three-state, active high encoder outputs
$\overline{EI}$	Enable input provided to allow cascaded operation
$\overline{EO}$	Enable output provided to enable the next lower order priority chip
G_1, G_2	Active high three-state output controls
$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$	Active low three-state output controls
$\overline{I}_{0\text{-}7}$	Active low encoder inputs

TRUTH TABLE

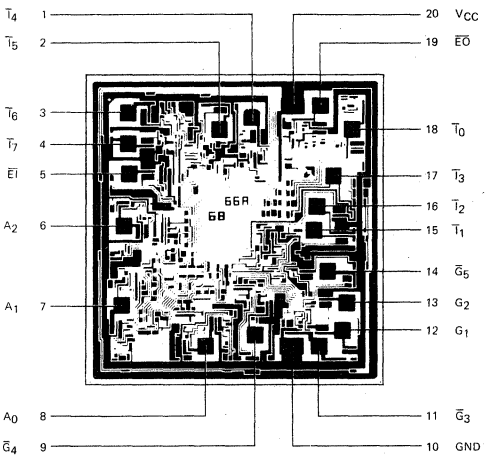
Inputs								Outputs			
$\overline{EI}$	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	A_0	A_1	A_2	$\overline{EO}$
H	X	X	X	X	X	X	X	X	L	L	L	H
L	H	H	H	H	H	H	H	H	L	L	L	L
L	X	X	X	X	X	X	X	L	H	H	H	H
L	X	X	X	X	X	X	L	H	L	H	H	H
L	X	X	X	X	X	L	H	H	H	L	H	H
L	X	X	X	X	L	H	H	H	L	L	H	H
L	X	X	X	L	H	H	H	H	H	H	L	H
L	X	X	L	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
For G_1 = H, G_2 = H, G_3 = L, G_4 = L, G_5 = L

G1	G2	$\overline{G3}$	$\overline{G4}$	$\overline{G5}$	A_0	A_1	A_2
H	H	L	L	L	Enabled		
L	X	X	X	X	Z	Z	Z
X	L	X	X	X	Z	Z	Z
X	X	H	X	X	Z	Z	Z
X	X	X	H	X	Z	Z	Z
X	X	X	X	H	Z	Z	Z

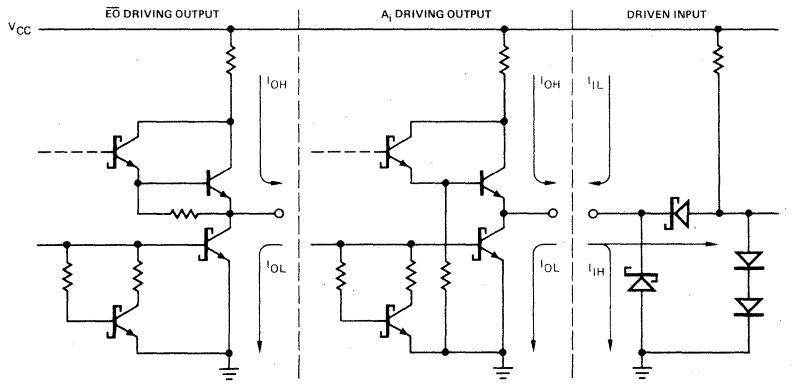
Z = HIGH Impedance

Metallization and Pad Layout



DIE SIZE 0.082 X 0.085

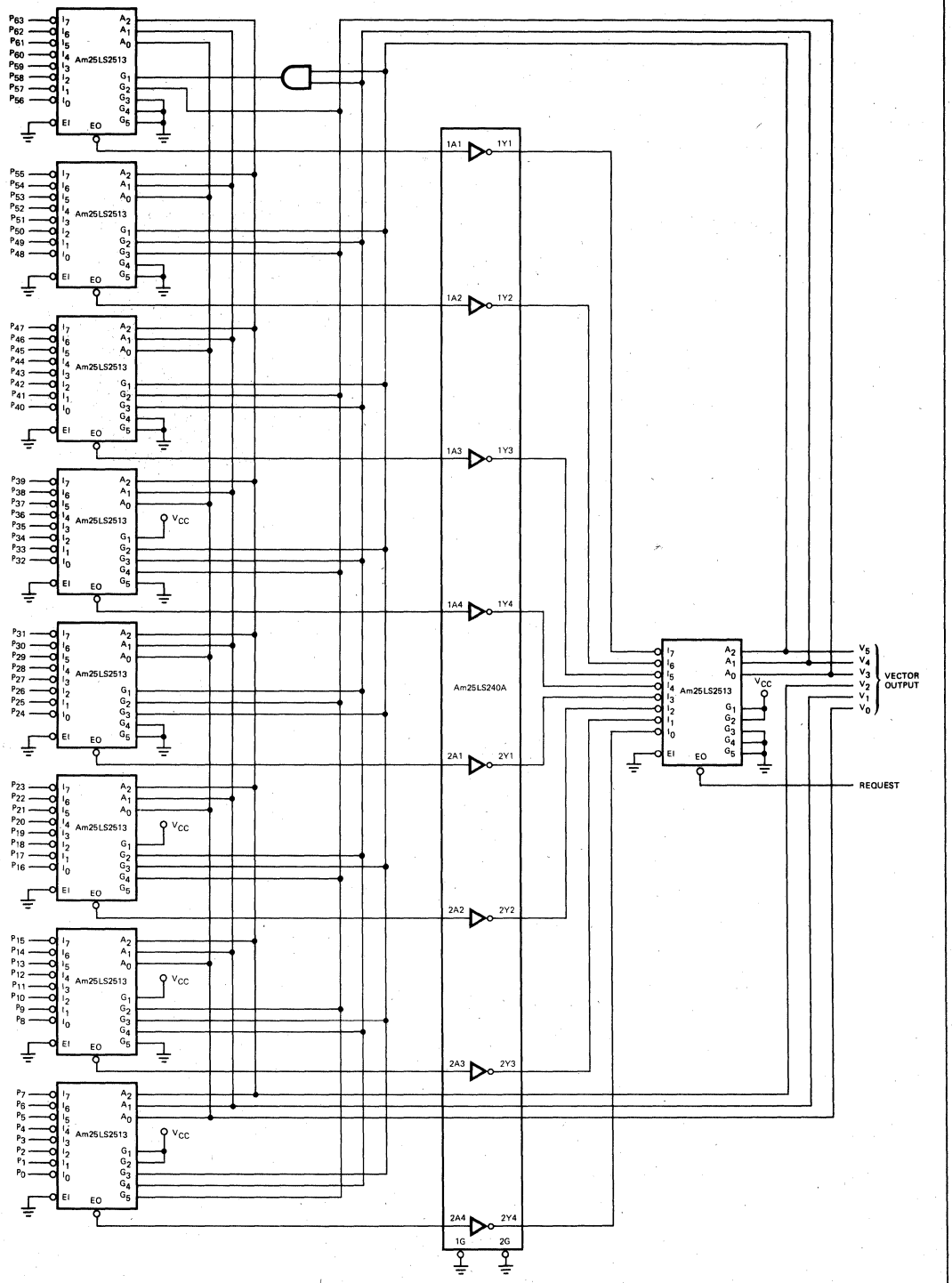
Am25LS
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

9

APPLICATION

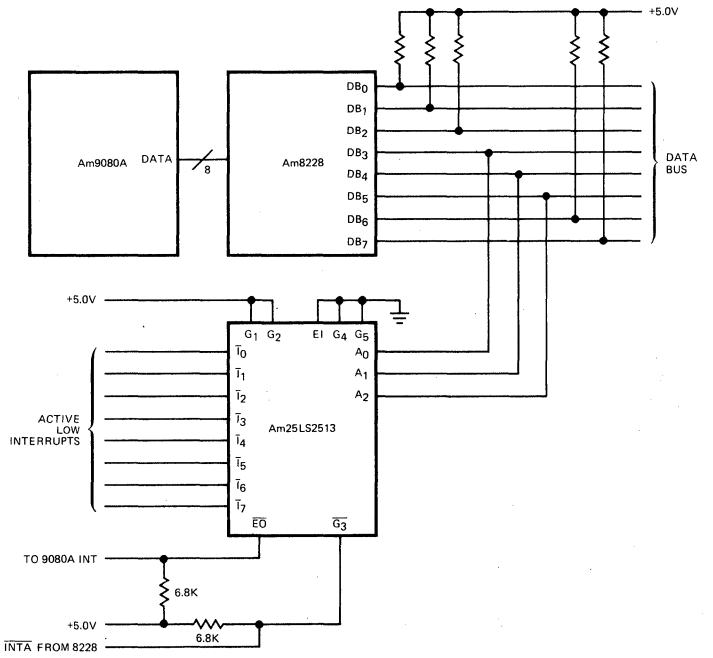


64 Input Priority Encoder Connected for Parallel Enable

ORDERING INFORMATION

Package Type	Temperature Range	Am25LS2513 Order Number
Molded DIP	0 to +70°C	AM25LS2513PC
Hermetic DIP	0 to +70°C	AM25LS2513DC
Chip-Pak	0 to +70°C	AM25LS2513LC
Dice	0 to +70°C	AM25LS2513XC
Hermetic DIP	−55 to +125°C	AM25LS2513DM
Hermetic Flat-Pak	−55 to +125°C	AM25LS2513FM
Chip-Pak	−55 to +125°C	AM25LS2513LM
Dice	−55 to +125°C	AM25LS2513XM

PRIORITY ENCODED RST INTERRUPT INSTRUCTION FOR THE Am9080A



Am25LS2516

Eight-Bit by Eight-Bit Serial/Parallel Multiplier with Accumulator

DISTINCTIVE CHARACTERISTICS

- Two's complement, two-bit lookahead carry-save arithmetic
- Microprogrammable — four-bit instruction code for load, multiply, and read operations
- Cascadable, two devices perform full 16-bit multiplication without additional hardware
- Eight-bit byte parallel, bidirectional, bussed I/O
- On-chip registers and double length accumulator
- Overflow indicator
- Three-state shared bus input/output lines
- High-speed architecture provides clock rates of 20MHz (Typ)

RELATED PRODUCTS

Part No.	Description	Page
Am25S05		
Am25LS14A		
Am25S557/8		
Am29516/7		

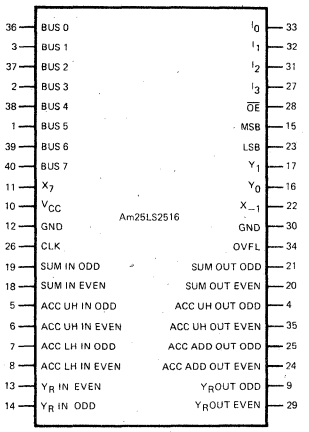
FUNCTIONAL DESCRIPTION

The Am25LS2516 is an eight-bit by eight-bit multiplier and accumulator employing serial/parallel, two's complement, carry-save arithmetic to deliver a 16-bit product in eight clock cycles. The device is fully cascadable for use in high-speed, real-time, digital signal processing applications.

The device includes an eight-bit X Register prior to the X latch providing X hold for chain or overlapping calculations. The X and Y registers are loaded by clocking prior to the beginning of a multiply cycle, the data supplied by the bidirectional bus or the accumulator register. The double length, 16-bit output is multiplexed onto the eight-bit bus; either the upper or lower halves of the result can be read at any one time.

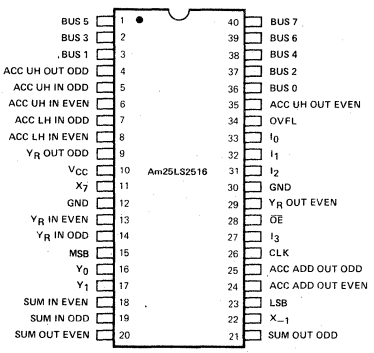
The accumulator and the Y register are both organized as dual-rank shift registers, allowing them to shift two bits at a time. The serial inputs and outputs of the Y register, the low and high order halves of the accumulator and the two-bit serial accumulator adder output, both serially and in parallel, are all available at external pins to provide cascadability.

LOGIC SYMBOL



MPR-336

CONNECTION DIAGRAM



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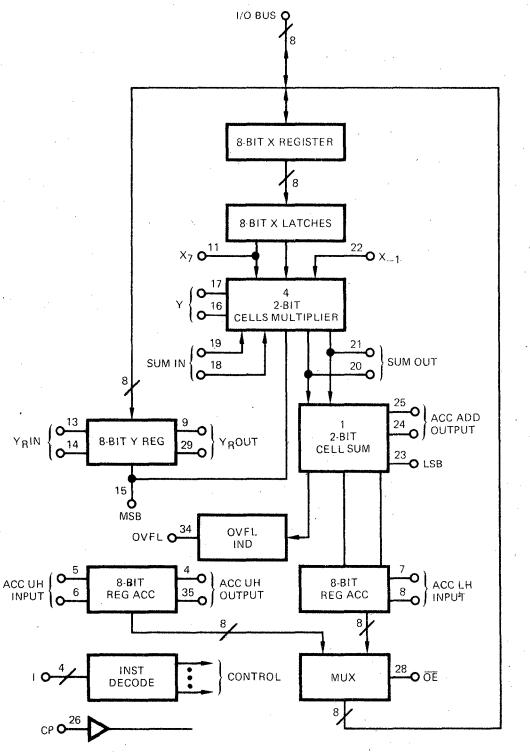
LOGIC DIAGRAM



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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5%	MIN. = 4.75V	MAX. = 5.25V
MIL	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%	MIN. = 4.50V	MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

(Bus Inputs/Outputs)

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.0mA		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA				0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V					−0.8	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V					60	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					0.2	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−30		−100	mA
I_{OZ}	Off-State (HIGH Impedance) Output Current	V_{CC} = MAX.	V_O = 2.4V				60	μA
			V_O = 0.4V				−800	

Non-Bus Inputs/Outputs

V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −440μA	MIL	2.5			Volts
				COM'L	2.7			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Y_R OUT, I_{OL} = 15mA				0.5	Volts
			Others I_{OL} = 4.0mA				0.4	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		Y_0, Y_1			0.8	Volts
				Others, MIL			0.7	
				Others, COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V				See Table 1		mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				See Table 1		μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				See Table 1		mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				285	390	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Pins 28 and 31 HIGH, all other inputs at GND. Test after one full clock cycle of LOW-HIGH-LOW.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Case) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +6.3V
DC Voltage Applied to Outputs for High Output State	−0.5V to + V_{CC} max.
DC Input Voltage (Pins 5, 6, 7, 8, 18, 19, 26)	−0.5V to +5.5V
DC Input Voltage (Other pins)	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

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TABLE I.

Terminals	I_{IL}	I_{IH}	I_I
Y IN	−.3mA	20μA	.1mA
I_0, I_1, I_3, OE	−.45mA	20μA	.1mA
Bus 0-7	−.6mA	90μA	.3mA
CP	−.8mA	80μA	.4mA
I_2, X_{-1}	−.9mA	40μA	.1mA
SUM IN	−1.4mA	80μA	.5mA
LSB	−1.6mA	80μA	.4mA
ACC IN all	−2mA	50μA	1mA
MSB	−3mA	150μA	1.5mA
Y_0, Y_1	−7.5mA	200μA	2mA

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	0°C to +70°C	AM25LS2516DC
	−55°C to +125°C	AM25LS2516DM (Note 1)

Note 1. Military temperature range product in development.

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Y_R Register OUT		12	18	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}			15	23		
t_{PLH}	SUM OUT		13	20	ns	
t_{PHL}			15	23		
t_{PLH}	ACC ADDER OUT		27	41	ns	
t_{PHL}			27	41		
t_{PLH}	ACC UH OUT		11	17	ns	
t_{PHL}			13	20		
t_{PLH}	ACC Bus		23	34	ns	
t_{PHL}			17	26		
t_{PLH}	$\overline{OVFL}$		12	18	ns	
t_{PHL}			15	23		
t_{PLH}	X_7		13	20	ns	
t_{PHL}			17	26		
t_{ZH}	$\overline{OE}$ to Bus		12	18	ns	
t_{ZL}			9	14		
t_{HZ}			24	36	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			12	18		
t_S	X Register (Bus)	20			ns	C_L = 15pF, R_L = 2.0kΩ
t_S	Y Register (Bus)	15			ns	
t_S	X_{-1}	35			ns	
t_S	SUM IN	37			ns	
t_S	Y Register (Serial)	20			ns	
t_S	ACC LH or UH IN	8			ns	
t_S	Multiplier Y_0 and Y_1	33			ns	
t_S	Instruction	25			ns	
t_h	SUM IN, X_{-1}, Multiplier Y_0 and Y_1	0			ns	
t_h	I_{0-3} Hold Time	10			ns	
t_h	Hold Time on All Other Inputs	5			ns	
f_{max} (Note 1)	Maximum Clock Frequency	17			MHz	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

TIMING DIAGRAMS

	HOLD			SHIFT								SHIFT								HOLD			
FUNCTION	NOP	LDX	LDY CLA	MPY	MPY	MPY	MPY	MPY	LDX	MPY	LDY	MPY	MPY	MPY	MPY	MPY	MPY	MPY	MPY	NOP	RUH	RLH	NOP
CP	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
I_3																							
I_2																							
I_1																							
I_0																							
BUS	Z	X_1	Y_1	Z	Z	Z	Z	Z	X_2	Z	Y_2	Z	Z	Z	Z	Z	Z	Z	Z	Z	A_U	A_L	Z
X_7	X_{07}	X_{07}	X_{07}	X_{17}	X_{17}	X_{17}	X_{17}	X_{17}	X_{17}	X_{17}	X_{17}	X_{27}	X_{27}	X_{27}	X_{27}	X_{27}	X_{27}	X_{27}	X_{27}	X_{27}	X_{27}	X_{27}	X_{27}
Y OUT EVEN	Y_{07}	Y_{07}	Y_{07}	Y_{10}	Y_{12}	Y_{14}	Y_{16}	Y_{17}	Y_{17}	Y_{17}	Y_{17}	Y_{20}	Y_{22}	Y_{24}	Y_{26}	Y_{27}	Y_{27}	Y_{27}	Y_{27}	Y_{27}	Y_{27}	Y_{27}	Y_{27}
Y OUT ODD	Y_{07}	Y_{07}	Y_{07}	Y_{11}	Y_{13}	Y_{15}	Y_{17}	Y_{17}	Y_{17}	Y_{17}	Y_{17}	Y_{21}	Y_{23}	Y_{25}	Y_{27}	Y_{27}	Y_{27}	Y_{27}	Y_{27}	Y_{27}	Y_{27}	Y_{27}	Y_{27}
SUM OUT EVEN					P_{10}	P_{12}	P_{14}	P_{16}	P_{18}	P_{110}	P_{112}	P_{114}	P_{20}	P_{22}	P_{24}	P_{26}	P_{28}	P_{210}	P_{212}	P_{214}			
SUM OUT ODD					P_{11}	P_{13}	P_{15}	P_{17}	P_{19}	P_{111}	P_{113}	P_{115}	P_{21}	P_{23}	P_{25}	P_{27}	P_{29}	P_{211}	P_{213}	P_{215}			
ACC ADD OUT EVEN					A_{10}	A_{12}	A_{14}	A_{16}	A_{18}	A_{110}	A_{112}	A_{114}	A_{20}	A_{22}	A_{24}	A_{26}	A_{28}	A_{210}	A_{212}	A_{214}			
ACC ADD OUT ODD					A_{11}	A_{13}	A_{15}	A_{17}	A_{19}	A_{111}	A_{113}	A_{115}	A_{21}	A_{23}	A_{25}	A_{27}	A_{29}	A_{211}	A_{213}	A_{215}			
ACC UH OUT EVEN	A_{08}	A_{08}	A_{08}	A_{08}	0	0	0	0	A_{10}	A_{12}	A_{14}	A_{16}	A_{18}	A_{110}	A_{112}	A_{114}	A_{20}	A_{22}	A_{24}	A_{26}	A_{28}	A_{28}	A_{28}
ACC UH OUT ODD	A_{09}	A_{09}	A_{09}	A_{09}	0	0	0	0	A_{11}	A_{13}	A_{15}	A_{17}	A_{19}	A_{111}	A_{113}	A_{115}	A_{21}	A_{23}	A_{25}	A_{27}	A_{29}	A_{29}	A_{29}
$\overline{OVFL}$	F_0	F_0	F_0	F_0	0	0	0	0	0	0	0	0	F_1	F_1	F_1	F_1	F_1	F_1	F_1	F_1	F_2	F_2	F_2

CP																							
LOAD X																							
LOAD Y																							
$\overline{STROBE\ X}$																							
$\overline{TCL}$																							
SHIFT ACC																							
$\overline{CLEAR\ ACC}$																							
MUX																							
OEN																							
OVFLEN																							
$\overline{CSAV\ ACC}$					1	C_{12}	C_{14}	C_{16}	C_{18}	C_{110}	C_{112}	C_{114}	1	C_{22}	C_{24}	C_{26}	C_{28}	C_{210}	C_{212}	C_{214}			
A_{14}	A_{014}	A_{014}	A_{014}	A_{014}	0	A_{10}	A_{12}	A_{14}	A_{16}	A_{18}	A_{110}	A_{112}	A_{114}	A_{20}	A_{22}	A_{24}	A_{26}	A_{28}	A_{210}	A_{212}	A_{214}	A_{214}	A_{214}
A_{15}	A_{015}	A_{015}	A_{015}	A_{015}	0	A_{11}	A_{13}	A_{15}	A_{17}	A_{19}	A_{111}	A_{113}	A_{115}	A_{21}	A_{23}	A_{25}	A_{27}	A_{29}	A_{211}	A_{213}	A_{215}	A_{215}	A_{215}
A_6	A_{06}	A_{06}	A_{06}	A_{06}	0	0	0	0	0	A_{10}	A_{12}	A_{14}	A_{16}	A_{18}	A_{110}	A_{112}	A_{114}	A_{20}	A_{22}	A_{24}	A_{26}	A_{26}	A_{26}
A_5	A_{07}	A_{07}	A_{07}	A_{07}	0	0	0	0	0	A_{11}	A_{13}	A_{15}	A_{17}	A_{19}	A_{111}	A_{113}	A_{115}	A_{21}	A_{23}	A_{25}	A_{17}	A_{27}	A_{27}
A_0	A_{00}	A_{00}	A_{00}	A_{00}	0	0	0	0	0	0	0	0	A_{10}	A_{12}	A_{14}	A_{16}	A_{18}	A_{110}	A_{112}	A_{114}	A_{20}	A_{20}	A_{20}
A_1	A_{01}	A_{01}	A_{01}	A_{01}	0	0	0	0	0	0	0	0	A_{11}	A_{13}	A_{15}	A_{17}	A_{19}	A_{111}	A_{113}	A_{115}	A_{21}	A_{21}	A_{21}

KEY:

▨ Data invalid

Note: Variables shown are general.
For this example:

$P_1 = X_1Y_1$ $A_1 = P_1$ $F_1 = 0$

$P_2 = X_2Y_2$ $A_2 = P_1 + P_2$

Am25LS2516
SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	YR Register OUT		24		26	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}			33		37		
t_{PLH}	SUM OUT		27		27	ns	
t_{PHL}			34		34		
t_{PLH}	ACC ADDER OUT		50		52	ns	
t_{PHL}			57		60		
t_{PLH}	ACC UH OUT		23		23	ns	
t_{PHL}			30		30		
t_{PLH}	ACC Bus		42		45	ns	
t_{PHL}			38		39		
t_{PLH}	$\overline{OVFL}$		26		26	ns	
t_{PHL}			33		33		
t_{PLH}	X_7		30		33	ns	
t_{PHL}			39		42		
t_{ZH}	$\overline{OE}$ to Bus		30		33	ns	C_L = 50pF, R_L = 2.0kΩ
t_{ZL}			21		23	ns	
t_{HZ}			45		55	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			21		30	ns	
t_S	X Register (Bus)	20		22		ns	C_L = 50pF, R_L = 2.0kΩ
t_S	Y Register (Bus)	15		17		ns	
t_S	X_{-1}	45		51		ns	
t_S	SUM IN	52		62		ns	
t_S	Y Register (Serial)	20		20		ns	
t_S	ACC LH or UH IN	10		14		ns	
t_S	Multiplier Y_0 and Y_1	44		51		ns	
t_S	Instruction	27		30		ns	
t_H	SUM IN, X_{-1}, Multiplier and Y_1	0		0		ns	
t_H	I_{0-3} Hold Time	10		10		ns	
t_H	All Other Inputs	5		5		ns	
f_{max} (Note 1)	Maximum Clock Frequency	15.5		10		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

The following table provides a guide to the improvement in performance which may be obtained by control of the V_{CC} power supply.

	V_{CC} = 5.0V	V_{CC} = 5.0V ±5%	V_{CC} = 5.0V ±10%
T_A = 25°C	17MHz	16MHz	15MHz
T_A = 0°C to +70°C	16MHz	15.5MHz	–
T_C = −55°C to +125°C	12MHz	–	10MHz

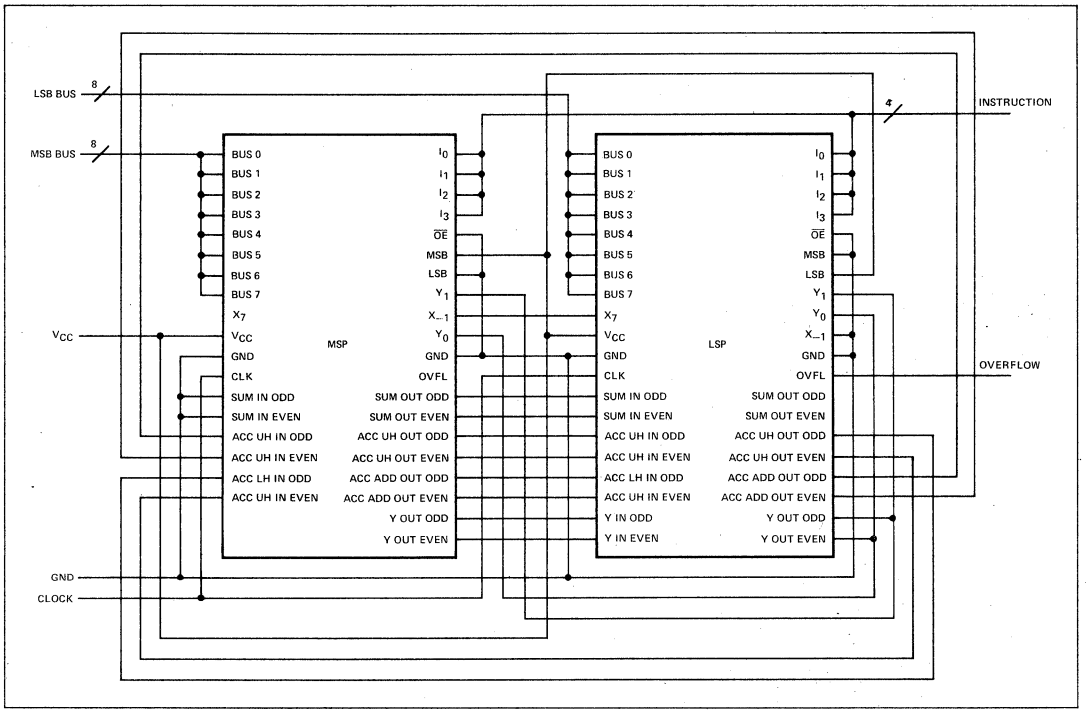


Figure 5b. Two Devices Cascaded in 16-Bit by 16-Bit Multiplier Application with 32-Bit Accumulated Product.

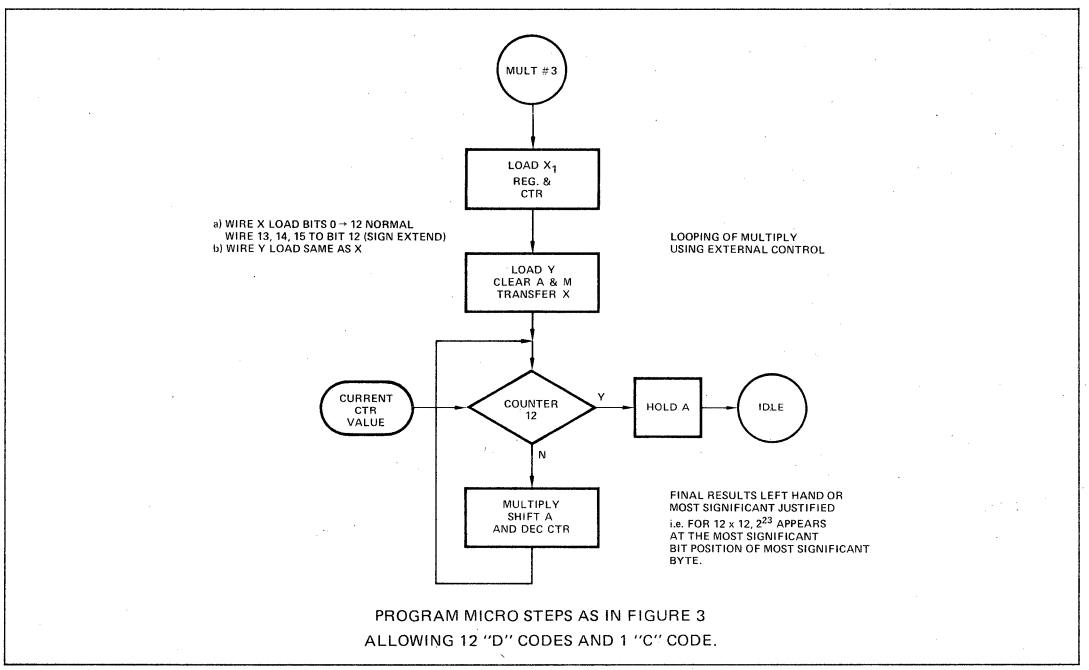


Figure 6. 16 Bit Two's Complement Multiply without Accumulate Modified to 12 x 12 (Using Two Am25LS2516 Devices Interconnected).

PROGRAM MICRO STEPS

#	INST IN HEX
1	E
2	4
3	D
4	D
5	D
6	F
7	D
8	D
9	D
10	7
11	D
12	D
13	D
14	D
15	D
16	D
17	D
18	D
19	C
20	C IDLE
21	C
IDLE	

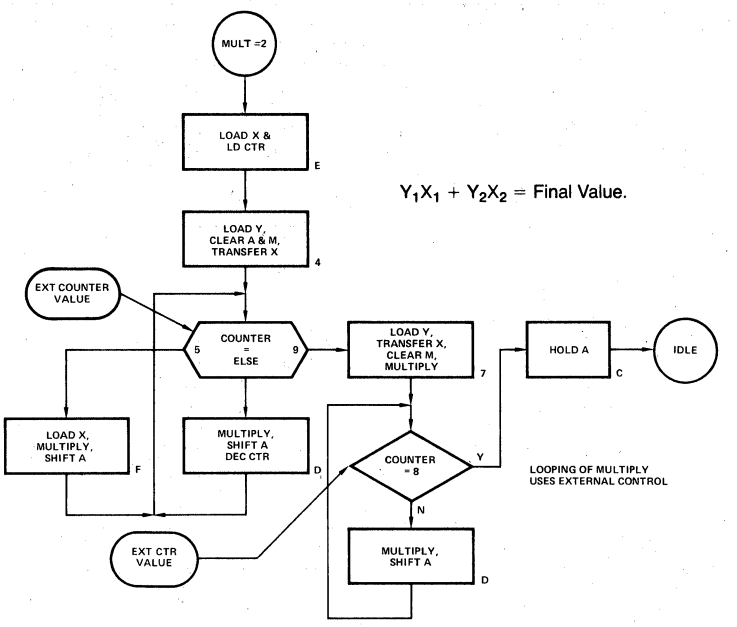


Figure 4. 8-Bit Two's Complement Multiply with Accumulate, Intermediate Load and Chain Calculations.

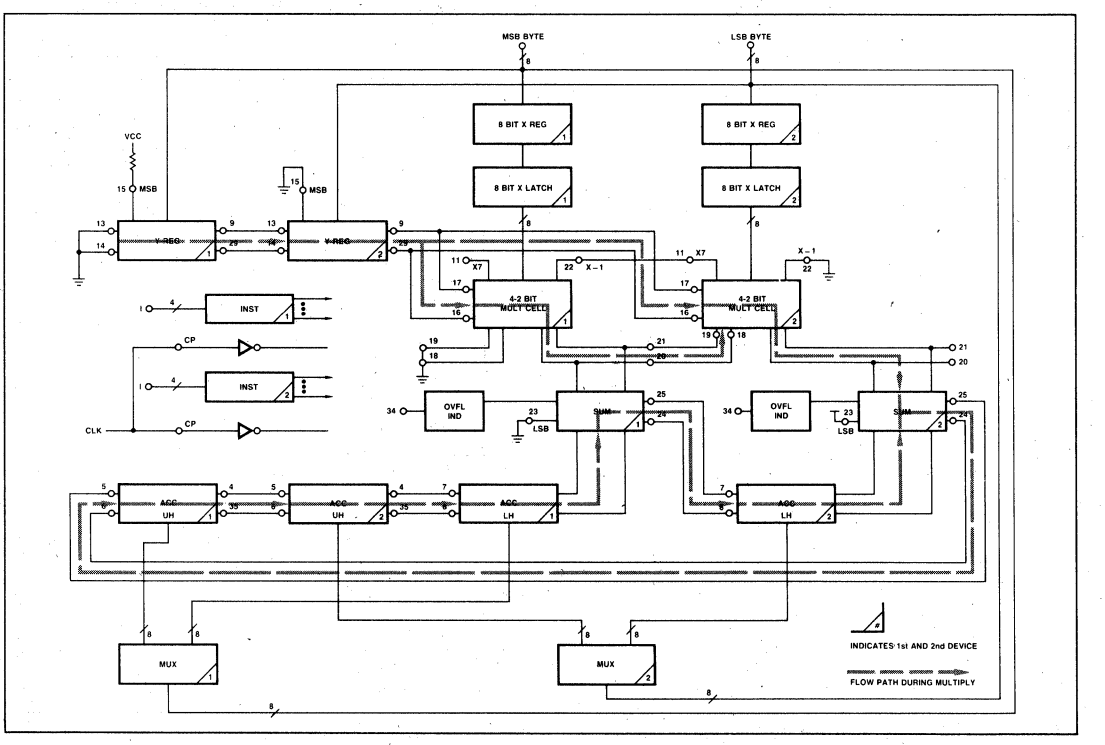


Figure 5a. Interconnection of Two Am25LS2516 (8 x 8 Multiplier) Devices to Execute a 16 x 16 Multiply.

FUNCTION TABLE

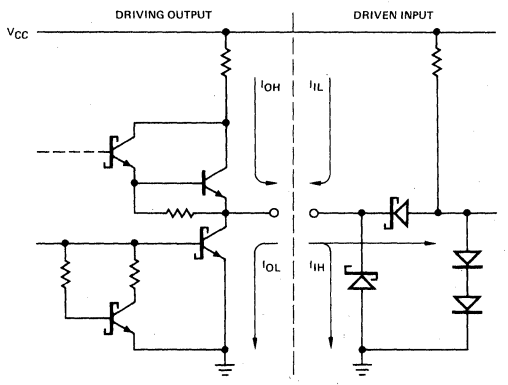
Mnemonic	I_3 I_2 I_1 I_0	Function	CLR M	LOAD X	LOAD Y	XFER X	CLR A*	SHFT A	MUX	OE	Remarks
YLHC	0 0 0 0	LHA → Y, XFER X, CLR A CLR M, READ OVFL	1	0	1	1	0	0	0	1	
YUHC	0 0 0 1	UHA → Y, XFER X, CLR A CLR M, READ OVFL	1	0	1	1	0	0	1	1	
YLHA	0 0 1 0	LHA → Y, XFER X CLR M, READ OVFL	1	0	1	1	1	0	0	1	
YUHA	0 0 1 1	UHA → Y, XFER X CLR M, READ OVFL	1	0	1	1	1	0	1	1	
LYCA	0 1 0 0	LOAD Y, XFER X, CLR A, CLR M	1	0	1	1	0	0	0	0	Same Func. as 0101
LYCA	0 1 0 1	CLR A LOAD Y, XFER X, CLR M	1	0	1	1	0	1	1	0	Same Func. as 0100
LYHA	0 1 1 0	LOAD Y, XFER X, HOLD A, CLR M	1	0	1	1	1	0	0	0	
LYSA	0 1 1 1	LOAD Y, XFER X, SHIFT A CLR M, MULTIPLY	1	0	1	1	1	1	1	0	OVFLEN in Next State
RLHA	1 0 0 0	READ LHA READ OVFL	0	0	0	0	1	0	0	1	
RUHA	1 0 0 1	READ UHA READ OVFL	0	0	0	0	1	0	1	1	
XLHA	1 0 1 0	LHA → X READ OVFL	0	1	0	0	1	0	0	1	
XUHA	1 0 1 1	UHA → X READ OVFL	0	1	0	0	1	0	1	1	
HLDA	1 1 0 0	HOLD A OVFLEN AFTER MULT	0	0	0	0	1	0	0	0	Must Prc'd Any Output
MULT	1 1 0 1	MULTIPLY SHIFT A	0	0	0	0	1	1	1	0	
LXHA	1 1 1 0	LOAD X, HOLD A	0	1	0	0	1	0	0	0	
LXSA	1 1 1 1	LOAD X, SHIFT A MULTIPLY	0	1	0	0	1	1	1	0	

*Active LOW

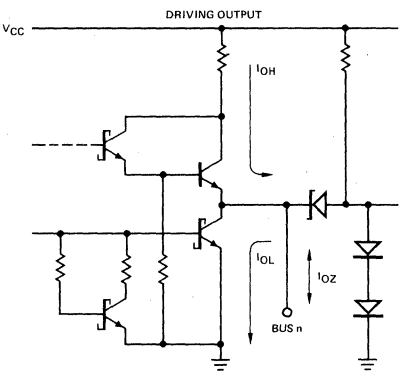
Am25LS
LOW-POWER SCHOTTKY INPUT/OUTPUT
CURRENT INTERFACE CONDITIONS

9

Other Outputs



Bus Outputs



Note: Actual current flow direction shown

DEFINITION OF FUNCTIONAL TERMS

Bus 0-Bus 7 – Bi-directional 8-bit data bus.

X_7 – Interconnection link to more significant byte if cascading (output).

X_{-1} – Interconnecting link between devices to least significant byte if cascading (input) link X7 to X1 to cascade – must be ground if not used.

Accum Upper Half out, even – Accumulator output upper byte, even bit.

Accum Upper Half out, odd – Accumulator output upper byte, odd bit.

Accum Upper Half input even – Accumulator input, upper byte, even bit.

Accum Upper Half input odd – Accumulator input, upper byte, odd bit.

Accum Lower Half input even – Accumulator input, lower byte, even bit.

Accum Lower Half input odd – Accumulator input, lower byte, odd bit.

YR out even – "Y" register output, even (link to "Y0").

YR out odd – "Y" register output, odd (link to "Y1").

YR in even – "Y" register input, even (link for cascading) ground when not used.

YR in odd – "Y" register input, odd (link for cascading) ground when not used.

Y_1 – Multiplier odd input (link to Y register odd).

Y_0 – Multiplier even input (link to Y register even).

Sum in even – Multiplier input even for cascading link to more significant byte, for standalone, ground.

Sum in odd – Multiplier input odd for cascading link to more significant byte, for standalone, ground.

Sum out even – Multiplier output even (link to sum in even for cascading) can be used directly.

Sum out odd – Multiplier output odd (link to sum output odd for cascading) can be used directly.

Acc Add out, even – Adder output even, for LSB (Hi) output equal sum of Accum and multiplier, for LSB (low) output equal sum of accumulator and zero.

Acc Add out, odd – Same as above except odd bit instead of even.

LSB – Control for summing adder – See Accumulator Add outputs for definition.

I_0-I_3 – 4-bit instruction field – provide cycle for cycle control of device function.

OVFL – Stored overflow indicator used only on least significant byte. Requires proper execution of instruction to operate.

MSB – Control for "Y" reg. and multiplier to indicate Most Significant Byte – Activates sign extension and negative waiting for 2's compliment – Low for lesser significant bytes and High for Most Significant Byte only.

CP – Clock Pulse.

$\overline{OE}$ – 3 state enable for Bus 0-Bus 7 outputs.

The Am25LS2516 LSI Multiplier/Accumulator

By Roy Levy

The Am25LS2516 is an 8-bit Multiplier/Accumulator designed for medium performance, minimum power, real time signal processing applications such as digital filtering, Fast Fourier Transforms, and statistical correlation. Using two's complement carry-save arithmetic, this 40-pin LSI device delivers a 16-bit product in eight clock cycles. This will permit two devices to be cascaded to achieve a 16-bit by 16-bit multiplication in 940ns when used over the full military operating range.

A functional block diagram of the Am25LS2516 is shown in Figure 1. The key elements are an 8-bit X input register followed by an 8-bit X latch, an 8-bit Y register, four 2-bit multipliers, a 2-bit adder, two 8-bit accumulators (high order and low order), a byte selecting multiplexer and instruction decode logic. These components, equivalent to approximately 625 gate elements, are integrated onto a single chip fabricated using Advanced Micro Devices' high-performance, Low-Power Schottky technology. The on-chip accumulator is provided to minimize component count and power dissipation in a high density system. It also allows completion of a multiply and accumulate operation in the same time normally required for a multiply only. Other LSI multipliers currently available require the accumulator function to be provided externally.

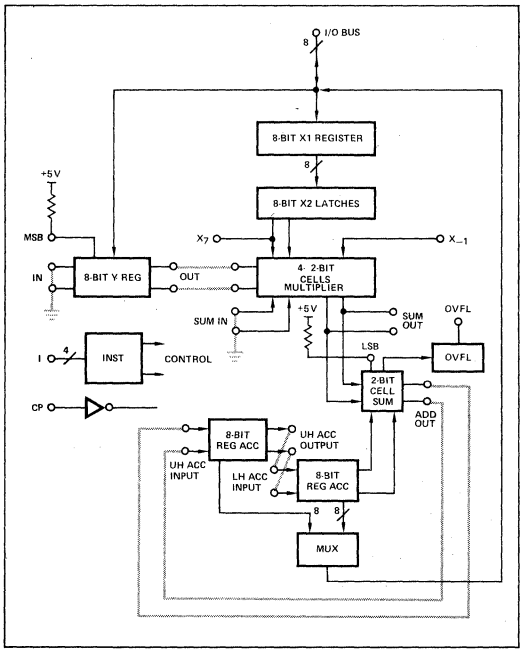


Figure 1. 8-Bit by 8-Bit Multiplier Block Diagram with External Connections Required to Accumulate A 16-Bit Product.

MULTIPLIER OPERATION

The Am25LS2516 is configured around an eight-line common input/output bidirectional bus. X and Y input and accumulator output data are routed via these bus lines. A two-rank register/latch combination is used for the X input to allow chaining of successive multiplies without losing a clock pulse; i.e., multiply and load vs. multiply. The latch holds the "X" data for the multiplier, allowing the X register to be loaded during any remaining multiply cycles. The "Y" Register can be parallel loaded, by command, from the 8-bit, on-chip bus from either the incoming 8 bits, or the Accumulator High or Accumulator Low Register (separate commands). The "Y" Register provides the 2-bit-at-a-time shift and the sign extend which allows the four 2-bit cells to operate in a serial by parallel mode. The multiplier produces a 2-bit product for each clock, LSB's first. Its output is accepted by the 2-bit adder as well as presented to external pins for expansion. A control gating array is provided to test for overflow during the last add cycle of the operation; i.e., cycle 8 for 8-bit multiply and cycle 16 for 16-bit multiply. The timing and control of this specific cycle is accomplished by the microcode chosen. The "HLDA" and "LYSA" instructions are provided for this purpose. The first cycle of a HOLD A following a multiply will cause the results of the overflow test to be stored. Two 8-bit accumulators are provided which must be externally connected in either an 8-bit, 16-bit, or greater configuration.

These accumulators as well as the Y Register, are both organized as dual-rank shift registers, which allow them to shift two bits at a time. The serial inputs and outputs of the Y Register and the low and high order halves of the accumulator are all brought out to external pins for cascading the device.

The accumulator output is available both serially and in parallel. The accumulator results are available one bit later than the multiply cycle and the accumulator stops shifting during read cycles. If the device is used to compute X • Y products without accumulation, a minimum of two overhead cycles must accompany each multiply – one for reading the upper (lower) half of the accumulator and one for clearing of the accumulator during the loading of the X or Y Registers. An output multiplexer selects the high or low order accumulator contents for presentation to the bus in parallel 8 bits at a time.

The heart of this device is an 8-bit multiplier (Figure 2) made up of four 2-bit cells. Each cell has three inputs (2 bits wide), two dual carry-save full adders, with four flip-flops for temporary storage (two for carry-save and two for partial product). The multiplier is actually subdivided into two separate adders with appropriate carry-save. The first adder forms a partial sum representing 0, 1X, 2X, or 3X by using combinations of X and 2X. The control of this combination of Y_0 and Y_1, respectively, to form $Y_0X_n + Y_1X_n + 1$. This sum (nX) is the input for the second adder. The second adder combines the first adder (nX) sum with the stored partial product shifted two places plus carry to form a new partial product.

$$P_{0MSB} + nX_0 + C = P_{0LSB}$$
$$P_{1MSB} + nX_1 + C = P_{1LSB}$$

The two partial product bits of the least significant cell are made available to the SUMmer and the SUM out terminals. The LSB input controls the SUM out providing a pass through or add dependent on polarity.

PROGRAMMING THE MULTIPLIER

The Am25LS2516 is an externally programmed device controlled by four instruction lines. This programmability provides a key to its flexibility. Sixteen microinstructions (see Table 1) are provided, which can be grouped into three major functions: Data Move, Read, and Multiply.

Instruction 0-3: The first instructions ("0", "1", "2", "3") load the "Y" Register from the Accumulator (high or low) and load the "X" Register while either clearing or not clearing, respectively, the Accumulator.

The next four instructions ("4", "5", "6", "7") load the "Y" Register from external "bus" and Holds on the accumulators and multiplier.

Instruction "7" is unique and is used to execute a chain multiply. It provides the last multiply operation while loading the "Y" Register, transferring the "X", and clearing the multiplier.

Instrucitons "8" and "9" provide the read-out (upper and lower halves) of the Accumulator.

Instructions "A" and "B" internally transfer the respective halves of the Accumulator to the "X" Register – another method of chain calculating.

Instruction "C" is used as an idling instruction after multiplication in order to hold the product in the accumulator until a read instruction can be performed. NOTE: The operations of the instruction are in some cases stored by clocking the instructions into an instruction register, accounting for a clocked delay in operations. Specifically, the shifting of the Accumulator is an internally stored command and as such is started and stopped one clock cycle late, allowing the Accumulator to complete its data shifting during the first HOLD A cycle following a multiply and starting it one clock cycle after the multiplying cycle is started.

Instruction "D" is a single iteration of the multiply and must be used for each bit in the multiplier minus one. The last bit of the multiplier will be handled by a HOLD A ("C") or a load Y and multiply (7).

Instruction "E" provides a load "X" Register and Hold.

Instruction "F" provides an intermediate instruction which can be executed during a multiply. It allows the "X" Register to load without disturbing the "X" Latch, while continuing the iteration of the multiply.

Instructions "C" and "7" also provide sampling and storage of the overflow condition.

TABLE I

MNEMONIC	INSTRUCTION $I_3I_2I_1I_0$ IN HEX	FUNCTION	REMARKS	
YLHC	0	LHA→Y, XFER X, CLR A CLR M, READ OVFL		
YUHC	1	UHA→Y, XFER X, CLR A CLR M, READ OVFL		
YLHA	2	LHA→Y, XFER X CLR M, READ OVFL		
YUHA	3	UHA→Y, XFER X CLR M, READ OVFL		
LYCA	4	LOAD Y, XFER X, CLR A CLR M	Same function as 5	
LYCA	5	CLR A LOAD Y, XFER X, CLR M	Same function as 4	
LYHA	6	LOAD Y, XFER X, HOLD A CLR M		
LYSA	7	LOAD Y, XFER X, SHIFT A CLR M, MULTIPLY	Enables overflow store in next state	*
RLHA	8	READ LHA READ OVFL		
RUHA	9	READ UHA READ OVFL		
XLHA	A	LHA→X READ OVFL		
XUHA	B	UHA→Y READ OVFL		
HLDA	C	HOLD A	Enable overflow store	
MULT	D	MULTIPLY SHIFT A		*
LXHA	E	LOAD X, HOLD A		
LXSA	F	LOAD X, SHIFT A MULTIPLY		*

*Continue multiplying instructions.

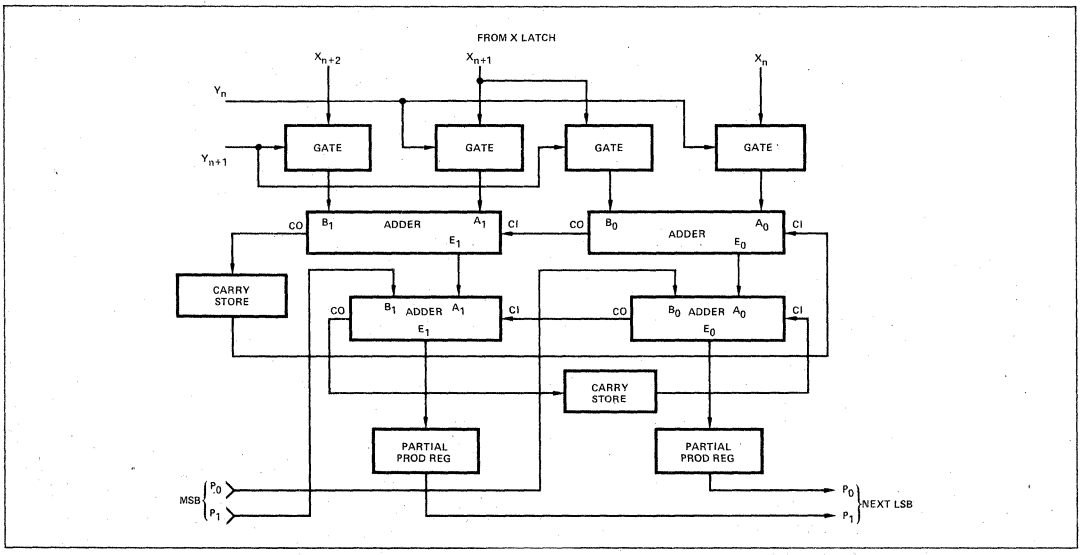
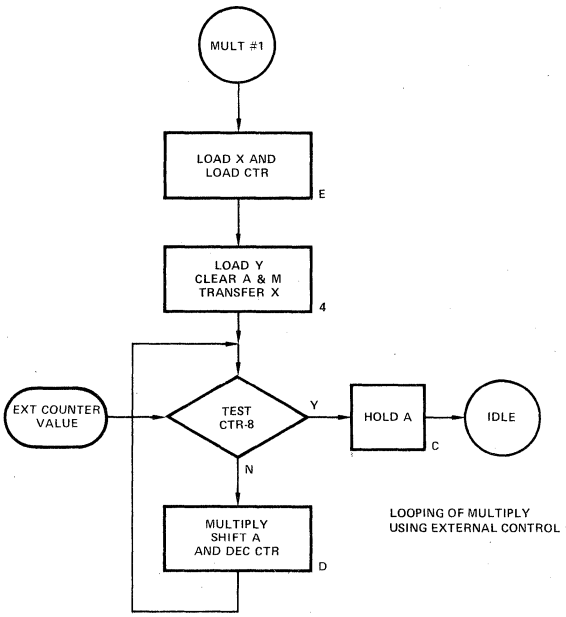


Figure 2. Am25LS2516 Multiplier Cell.

APPLICATION OF THE MULTIPLIER

The flow diagram for an 8-bit two's complement multiply is shown in Figure 3, together with the required program micro-steps. Figure 4 extends this to include accumulate, intermediate load of X and chain calculations. Figures 5a and b show the external connection of two Am25LS2516 devices to execute a 16-bit by 16-bit multiplication. A 32-bit product is completed in 16 clock cycles. This same technique may be extended in a similar fashion to longer word lengths. The flowchart of Figure 6 demonstrates a 16-bit two's complement multiply without accumulate, modified to a 12-bit by 12-bit function.

The Am25LS2516 Multiplier/Accumulator is the most complex LSI product manufactured to date with Low-Power Schottky technology. It will be extremely useful in high-density applications where minimum package count is a primary consideration. The device itself performs an 8 x 8 or 16 x 16 multiplication in approximately twice the time of parallel multipliers currently available, but using only one quarter the power in the multiplier portion of the function. In a fully configured system using both techniques, the Am25LS2516 performance begins to approach that of the parallel multiplier plus supporting devices.



PROGRAM MICRO STEPS

#	INST IN HEX
1	E
2	4
3	D
4	D
5	D
6	D
7	D
8	D
9	D
10	D
11	C
	IDLE

Figure 3. 8-Bit Two's Complement Multiply without Accumulate or Chain.

Am25LS381 • Am54LS/74LS381
Am25LS2517

Arithmetic Logic Unit/Function Generator
Low-Power Schottky Integrated Circuits

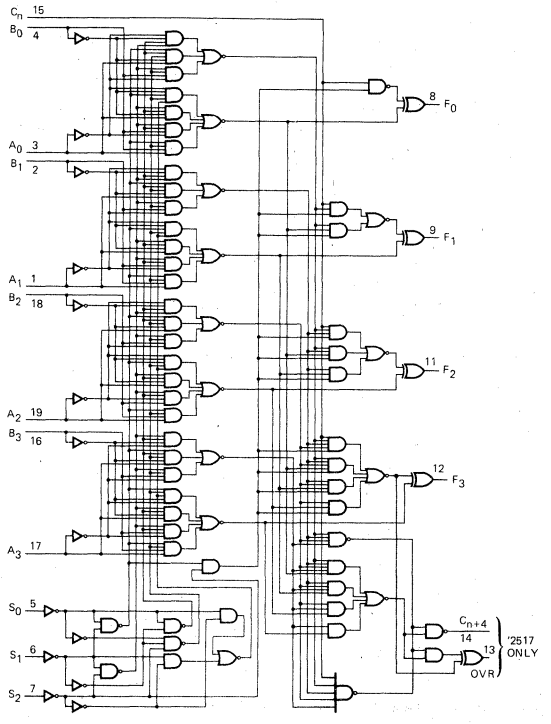
DISTINCTIVE CHARACTERISTICS

- Three arithmetic functions
- Three logic functions
- Preset and clear functions
- Carry output (C_{n+4}) and overflow (OVR) outputs on Am25LS2517
- Generate and propagate outputs for full lookahead carry on Am25LS381
- 8mA sink current over the military temperature range on Am25LS
- 50mV improved V_{OL} on Am25LS compared to Am54LS/74LS
- 440μA source current at HIGH output

RELATED PRODUCTS

Part No.	Description
Am2901	Bit Slice
Am2903	Bit Slice
Am29203	Super Slice
Am29501	Multiport Pipeline Processor

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

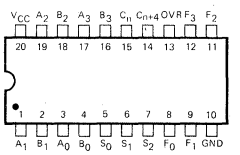
The Am25LS381 and Am54LS/74LS381 are arithmetic logic units (ALU)/function generators that perform three arithmetic operations and three logic operations on two 4-bit words. The device can also output forced 0000 (clear) or 1111 (preset). These eight operations are selected using three function select inputs S_0, S_1 and S_2 as shown in the function table. Full carry look ahead is used over the four-bit field within the device. When devices are cascaded, multi-level full carry look-ahead is implemented using a '182 carry look ahead generator and the $\overline{G}$ and $\overline{P}$ outputs on the Am25LS381 or Am54LS/74LS381. The device is packaged in a space-saving (0.3-inch row spacing) 20-pin package. If the C_{n+4} carry output function is required, the Am25LS2517 should be used.

The Am25LS381 is a high-performance version of the Am54LS/74LS381. Improvements include faster a. c. specifications, higher noise margin and twice the fan-out over the military temperature range.

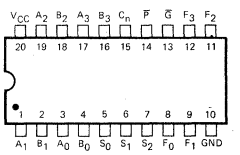
The Am25LS2517 is an arithmetic logic unit (ALU)/function generator that performs three arithmetic operations and three logic operations on two 4-bit words. The device can also force output 0000 (clear) or 1111 (preset). These eight operations are selected using three function select inputs S_0, S_1 and S_2 as shown in the function table. Full carry look-ahead is used over the four-bit field within the device. When devices are cascaded, the carry output (C_{n+4}) is connected to the carry input (C_n) of the next device. The Am25LS2517 can also detect two's complement overflow. The overflow output (OVR) is defined logically as $C_{n+3} \oplus C_{n+4}$.

CONNECTION DIAGRAMS
Top Views

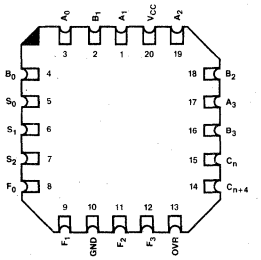
Am25LS2517



Am25LS381
Am54LS/74LS381



Leadless Chip Carrier
L-20-1



Note: Pin 1 is marked for orientation.

Am25LS381•Am25LS2517
ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −440μA, V_{IN} = V_{IH} or V_{IL}		MIL	2.5	3.4		Volts
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
			$\overline{G}$, I_{OL} = 16mA				0.55	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V		Any S			−0.36	mA
				Any A or B			−1.44	
				'LS381, C_n			−1.08	
				'LS2517, C_n			−1.44	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V		Any S			20	μA
				Any A or B			80	
				'LS381, C_n			60	
				'LS2517, C_n			80	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V		Any S			0.1	mA
				Any A or B			0.4	
				'LS381, C_n			0.3	
		V_{CC} = MAX., V_{IN} = 5.5V		'LS2517, C_n			0.4	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.	MIL	Am25LS381			40	mA
				Am25LS2517			43	
			COM'L	Am25LS381		25	43	
				Am25LS2517		27	47	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: LS381: $S_0 = S_1 = S_2$ = GND, all other inputs open.
LS2517: $S_0 = C_n$ = open, all other inputs = GND.

Am25LS • Am54LS/74LS

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage (Except Am25LS2517, C_n input = 5.5V)	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −400μA, V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4mA			0.4	Volts
			74LS only, I_{OL} = 8mA			0.5	
			$\overline{P}$, I_{OL} = 8.0mA			0.5	
			$\overline{G}$, I_{OL} = 16mA			0.65	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current (Note 5)	V_{CC} = MAX., V_{IN} = 0.4 V	Any S			−0.4	mA
			Others			−1.6	
I_{IH}	Input HIGH Current (Note 5)	V_{CC} = MAX., V_{IN} = 2.7 V	Any S			20	μA
			Others			80	
I_I	Input HIGH Current (Note 5)	V_{CC} = MAX., V_{IN} = 7.0 V	Any S			0.1	mA
			Others			0.4	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−100	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			25	43	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: LS381: $S_0 = S_1 = S_2$ = GND, all other inputs open.
LS2517: $S_0 = C_n$ = open, all other inputs = GND.
5. Limits chosen by AMD based on SN54S/74S381, T.I. LS data unavailable.

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3	The A data inputs.
B_0, B_1, B_2, B_3	The B data inputs.
S_0, S_1, S_2, S_3	The control inputs used to determine the arithmetic or logic function performed.
F_0, F_1, F_2, F_3	The data outputs of the ALU.
C_n	The carry-in input of the ALU.
C_{n+4}	The carry-look-ahead output of the four-bit input field.
$\overline{G}$	The carry-generate output for use in multi-level look-ahead schemes.
$\overline{P}$	The carry-propagate output for use in multi-level look-ahead schemes.
OVR	Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.

FUNCTION TABLE

Selection			Arithmetic/Logic Operation
S_2	S_1	S_0	
L	L	L	Clear
L	L	H	B Minus A
L	H	L	A Minus B
L	H	H	A Plus B
H	L	L	A ⊕ B
H	L	H	A + B
H	H	L	AB
H	H	H	Preset

H = High Level, L = Low Level
See Truth Table for full description.

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Am25LS Min	Am25LS Typ	Am25LS Max	Am54LS/74LS Min	Am54LS/74LS Typ	Am54LS/74LS Max	Units
t_{PLH}	C_n to F_i	C_L = 15pF, R_L = 2.0kΩ		14	21			26	ns
t_{PHL}				16	24			30	
t_{PLH}	A_i or B_i to F_i			16	24			30	ns
t_{PHL}				23	35			40	
t_{PLH}	S_i to F_i			20	30			35	ns
t_{PHL}				25	37			40	
t_{PLH}	A_i or B_i to $\overline{G}$ ('LS381 Only)			20	30			35	ns
t_{PHL}				15	23			30	
t_{PLH}	A_i or B_i to $\overline{P}$ ('LS381 Only)			17	26			34	ns
t_{PHL}				15	23			30	
t_{PLH}	S_i to $\overline{G}$ or $\overline{P}$ ('LS381 Only)			32	48			55	ns
t_{PHL}				23	35			42	
t_{PLH}	A_i or B_i to OVR ('LS2517 Only)			23	34			–	ns
t_{PHL}				24	36			–	
t_{PLH}	A_i or B_i to C_{n+4} ('LS2517 Only)			21	32			–	ns
t_{PHL}				24	36			–	
t_{PLH}	S_i to OVR or C_{n+4} ('LS2517 Only)			27	41			–	ns
t_{PHL}				37	55			–	
t_{PLH}	C_n to C_{n+4} ('LS2517 Only)			14	21			–	ns
t_{PHL}				15	22			–	
t_{PLH}	C_n to OVR ('LS2517 Only)			15	22			–	ns
t_{PHL}				15	22			–	

Am25LS ONLY
SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Test Conditions	Am25LS COM'L: T_A = 0 to +70°C, V_{CC} = 5.0V ±5% Min	Am25LS COM'L Max	Am25LS MIL: T_A = −55 to +125°C, V_{CC} = 5.0V ±10% Min	Am25LS MIL Max	Units
t_{PLH}	C_n to F_i	C_L = 50pF, R_L = 2.0kΩ		27		30	ns
t_{PHL}				35		42	
t_{PLH}	A_i or B_i to F_i			32		36	ns
t_{PHL}				44		50	
t_{PLH}	S_i to F_i			38		42	ns
t_{PHL}				48		55	
t_{PLH}	A_i or B_i to $\overline{G}$ ('LS381 Only)			37		40	ns
t_{PHL}				31		36	
t_{PLH}	A_i or B_i to $\overline{P}$ ('LS381 Only)			34		39	ns
t_{PHL}				34		42	
t_{PLH}	S_i to $\overline{G}$ or $\overline{P}$ ('LS381 Only)			57		63	ns
t_{PHL}				47		55	
t_{PLH}	A_i or B_i to OVR ('LS2517 Only)			41		45	ns
t_{PHL}				47		55	
t_{PLH}	A_i or B_i to C_{n+4} ('LS2517 Only)			38		40	ns
t_{PHL}				46		52	
t_{PLH}	S_i to OVR or C_{n+4} ('LS2517 Only)			52		60	
t_{PHL}				66		75	
t_{PLH}	C_n to C_{n+4} ('LS2517 Only)			28		32	ns
t_{PHL}				28		30	
t_{PLH}	C_n to OVR ('LS2517 Only)			30		35	ns
t_{PHL}				28		30	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

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Am25LS/54LS/74LS381
TEST TABLE

Path						Same Bit		Other Data Bits		Output
In	Out	S_0	S_1	S_2	C_n	4.5 V	GND	4.5 V	GND	Waveform
C_n	Any F	1	0	0	–	–	–	All A's & B's	–	out-of-phase
C_n	F_i	1	0	0	–	B_i	A_i	All A's & B's	–	in-phase
A_i	$\overline{G}$	1	1	0	X	B_i	–	All B's	All A's	out-of-phase
B_i	$\overline{G}$	1	1	0	X	A_i	–	All B's	All A's	out-of-phase
A_i	$\overline{P}$	X	X	1	X	B_i	–	All A's & B's	–	out-of-phase
B_i	$\overline{P}$	1	1	0	X	–	A_i	All B's	All A's	out-of-phase
A_i	F_i	0	1	0	0	–	B_i	–	A's & B's	out-of-phase
A_i	F_i	0	1	0	1	–	B_i	–	A's & B's	in-phase
B_i	F_i	0	1	0	0	–	A_i	–	A's & B's	out-of-phase
B_i	F_i	0	1	0	1	–	A_i	–	A's & B's	in-phase
A_i	F_{i+1}	0	1	0	1	B_i	–	A's & B's	–	out-of-phase
B_i	F_{i+1}	1	0	0	1	A_i	–	A's & B's	–	out-of-phase
S_0	F_i	–	0	0	1	B_i	A_i	All B's	All A's	in-phase
S_0	$\overline{G}$	–	1	0	X	–	–	A's & B's	–	out-of-phase
S_0	$\overline{P}$	–	1	0	X	–	–	All B's	All A's	out-of-phase
S_1	F_i	0	–	0	1	A_i	B_i	All A's	All B's	in-phase
S_1	$\overline{G}$	1	–	0	X	–	–	A's & B's	–	out-of-phase
S_1	$\overline{P}$	1	–	0	X	–	–	All A's	All B's	out-of-phase
S_2	F_i	0	1	–	1	A_i	B_i	All A's	All B's	out-of-phase
S_2	$\overline{G}$	1	1	–	X	–	–	A's & B's	–	in-phase
S_2	$\overline{P}$	1	1	–	X	–	–	All A's	All B's	in-phase

X = Don't care

TRUTH TABLE

	INPUTS						OUTPUTS					
FUNCTION	S_0	S_1	S_2	C_n	A_n	B_n	F_0	F_1	F_2	F_3	$\overline{G}$	$\overline{P}$
CLEAR	0	0	0	X	X	X	0	0	0	0	0	0
B MINUS A	1	0	0	0	0	0	1	1	1	1	1	0
				0	0	1	0	1	1	1	0	0
				0	1	0	0	0	0	0	1	1
				0	1	1	1	1	1	1	1	0
				1	0	0	0	0	0	0	1	0
				1	0	1	1	1	1	1	0	0
				1	1	0	1	0	0	0	1	1
				1	1	1	0	0	0	0	1	0
A MINUS B	0	1	0	0	0	0	1	1	1	1	1	0
				0	0	1	0	0	0	0	1	1
				0	1	0	0	1	1	1	0	0
				0	1	1	1	1	1	1	1	0
				1	0	0	0	0	0	0	1	0
				1	0	1	1	0	0	0	1	1
				1	1	0	1	1	1	1	0	0
				1	1	1	0	0	0	0	1	0
A PLUS B	1	1	0	0	0	0	0	0	0	0	1	1
				0	0	1	1	1	1	1	1	0
				0	1	0	1	1	1	1	1	0
				0	1	1	0	1	1	1	0	0
				1	0	0	1	0	0	0	1	1
				1	0	1	0	0	0	0	1	0
				1	1	0	0	0	0	0	1	0
				1	1	1	1	1	1	1	0	0
A ⊕ B	0	0	1	X	0	0	0	0	0	0	1	1
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	0
				X	1	1	0	0	0	0	0	0
A + B	1	0	1	X	0	0	0	0	0	0	1	1
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	1
				X	1	1	1	1	1	1	1	0
AB	0	1	1	X	0	0	0	0	0	0	0	0
				X	0	1	0	0	0	0	1	1
				X	1	0	0	0	0	0	0	0
				X	1	1	1	1	1	1	1	0
PRESET	1	1	1	X	0	0	1	1	1	1	1	1
				X	0	1	1	1	1	1	1	1
				X	1	0	1	1	1	1	1	1
				X	1	1	1	1	1	1	1	0

Am25LS2517
TEST TABLE

Path						Same Bit		Other Data Bits		Output
In	Out	S_0	S_1	S_2	C_n	4.5 V	GND	4.5 V	GND	Waveform
C_n	Any F	1	0	0	–	–	–	A's & B's	None	out-of-phase
C_n	F_i	1	0	0	–	B_i	A_i	A's & B's	None	in-phase
A_i	F_i	0	1	0	0	–	B_j	None	A's & B's	out-of-phase
A_i	F_i	0	1	0	1	–	B_i	None	A's & B's	in-phase
A_i	OVRF	0	1	1	1	B_i	–	A's & B's	None	in-phase
A_i	C_{n+4}	0	1	1	1	B_i	–	A's & B's	None	in-phase
B_i	F_i	0	1	0	0	–	A_i	None	A's & B's	out-of-phase
B_i	F_i	0	1	0	1	–	A_i	–	A's & B's	in-phase
B_i	OVRF	0	1	1	0	A_i	–	A's & B's	None	out-of-phase
B_i	C_{n+4}	0	1	1	0	A_i	–	A's & B's	None	out-of-phase
A_i	F_{i+1}	0	1	0	1	B_i	–	A's & B's	None	out-of-phase
B_i	F_{i+1}	1	0	0	1	A_i	–	A's & B's	None	out-of-phase
S_0	F_i	–	0	0	1	B_i	A_i	All B's	All A's	in-phase
S_0	OVRF	–	1	1	0	–	–	None	A's & B's	out-of-phase
S_0	C_{n+4}	–	1	1	0	–	–	None	A's & B's	out-of-phase
S_1	F_i	0	–	0	1	A_i	B_i	All A's	All B's	in-phase
S_1	OVRF	0	–	1	X	–	–	None	A's & B's	in-phase
S_1	C_{n+4}	0	–	1	X	–	–	None	A's & B's	in-phase
S_2	F_i	0	1	–	1	A_i	B_i	All A's	All B's	in-phase
S_2	OVRF	0	1	–	0	–	–	None	A's & B's	out-of-phase
S_2	C_{n+4}	0	1	–	0	–	–	None	A's & B's	in-phase

X = Don't care

TRUTH TABLE

	INPUTS						OUTPUTS					
FUNCTION	S_0	S_1	S_2	C_n	A_n	B_n	F_0	F_1	F_2	F_3	OVR	C_{n+4}
CLEAR	0	0	0	0	X	X	0	0	0	0	1	1
				1	X	X	0	0	0	0	1	1
B MINUS A	1	0	0	0	0	0	1	1	1	1	0	0
				0	0	1	0	1	1	1	0	1
				0	1	0	0	0	0	0	0	0
				0	1	1	1	1	1	0	0	0
				1	0	0	0	0	0	0	0	1
				1	0	1	1	1	1	0	0	1
				1	1	0	1	0	0	0	0	1
				1	1	1	0	0	0	0	0	1
A MINUS B	0	1	0	0	0	0	1	1	1	1	0	0
				0	0	1	0	0	0	0	0	0
				0	1	0	1	1	1	1	0	1
				0	1	1	0	0	0	0	0	1
				1	0	0	1	1	1	1	0	1
				1	0	1	0	0	0	0	0	1
				1	1	0	1	1	1	1	0	1
				1	1	1	0	0	0	0	0	1
A PLUS B	1	1	0	0	0	0	0	0	0	0	0	0
				0	0	1	1	1	1	1	0	0
				0	1	0	1	1	1	1	0	0
				0	1	1	0	1	1	1	0	1
				1	0	0	1	0	0	0	0	0
				1	0	1	0	1	1	1	0	1
				1	1	0	0	0	0	0	0	1
				1	1	1	1	1	1	1	0	1
A ⊕ B	0	0	1	0	0	0	0	1	1	1	0	0
				0	0	1	1	1	1	1	0	0
				0	1	0	1	0	0	0	0	1
				0	1	1	0	0	0	0	0	1
				1	0	0	0	0	0	0	0	1
				1	0	1	1	1	1	1	0	1
				1	1	0	1	1	1	1	0	1
				1	1	1	0	0	0	0	1	1
A + B	1	0	1	0	0	0	0	1	1	1	0	0
				0	0	1	1	1	1	1	0	0
				0	1	0	1	1	1	1	0	0
				0	1	1	1	1	1	1	0	0
				1	0	0	0	0	0	0	0	0
				1	0	1	1	1	1	1	0	0
				1	1	0	1	1	1	1	0	0
				1	1	1	1	1	1	1	1	1
AB	0	1	1	0	0	0	0	0	0	0	0	0
				0	0	1	0	0	0	0	1	0
				0	1	0	0	0	0	0	0	1
				0	1	1	1	1	1	1	0	1
				1	0	0	0	0	0	0	1	0
				1	0	1	0	0	0	0	0	1
				1	1	0	0	0	0	0	1	0
				1	1	1	1	1	1	1	1	1
PRESET	1	1	1	0	0	0	1	1	1	1	0	0
				0	0	1	1	1	1	1	0	0
				0	1	0	1	1	1	1	0	0
				0	1	1	1	1	1	1	0	0
				1	0	0	1	1	1	1	0	0
				1	0	1	1	1	1	1	0	0
				1	1	0	1	1	1	1	0	0
				1	1	1	1	1	1	1	1	1

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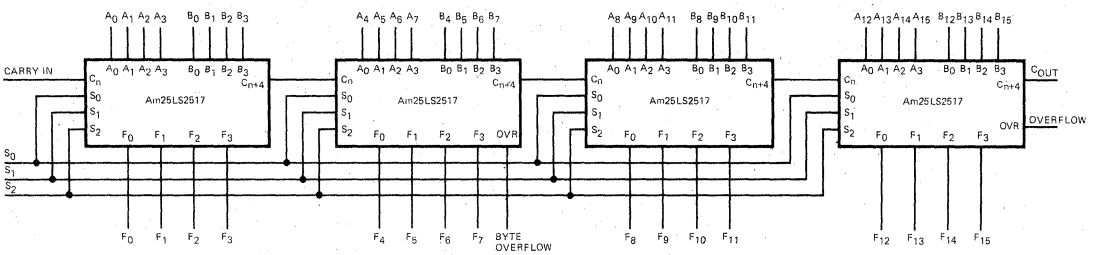
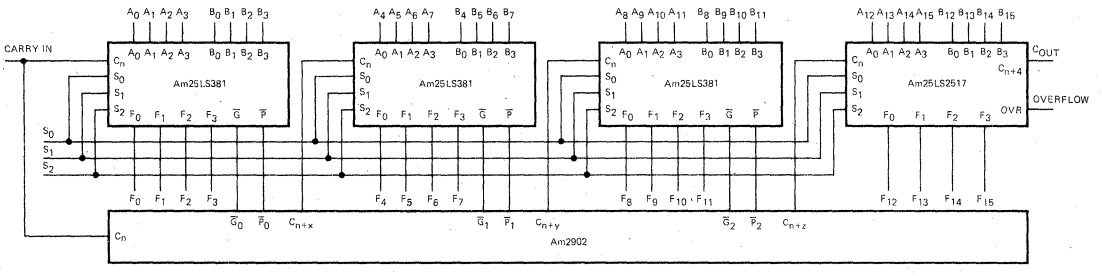
APPLICATIONS



TYPICAL SPEED CALCULATIONS

	Output	
Path	**F**	**C_{n+4}, OVR**
A_i or B_i to C_{n+4}	24 ns	24 ns
C_n to C_{n+4}	15 ns	15 ns
C_n to C_{n+4}	15 ns	15 ns
C_n to F_i	16 ns	—
C_n to C_{n+4}, OVR	—	15 ns
16-Bit Speed	70 ns	69 ns

The Am25LS2517 in a 16-Bit Ripple Carry ALU Connection.



TYPICAL SPEED CALCULATIONS

	Output	
Path	**F**	**C_{n+4}, OVR**
A_i or B_i to $\overline{G}$ or $\overline{P}$	20 ns*	20 ns*
$\overline{G}_i$ or $\overline{P}_i$ to C_{i+j} (Am 2902)	8 ns	8 ns
C_n to F	16 ns	—
C_n to C_{n+4}, OVR	—	15 ns
16-Bit Speed	44 ns	43 ns

* Note that S_i to G or P may be longer path.

The Am25LS2517 and Am25LS381 in a 16-Bit Carry Lookahead ALU Connection.

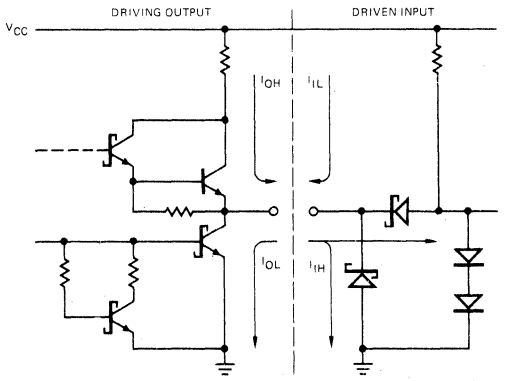
GUARANTEED LOADING RULES OVER OPERATING RANGE
(In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

		Am25LS				Am54LS/74LS			
			Output HIGH	Output LOW			Output HIGH	Output LOW	
Pin No.'s	Input/Output	Input Load	−440μA	MIL	COM'L	Input Load	−400μA	MIL	COM'L
1	A_1	4.0	–	–	–	4.4	–	–	–
2	B_1	4.0	–	–	–	4.4	–	–	–
3	A_0	4.0	–	–	–	4.4	–	–	–
4	B_0	4.0	–	–	–	4.4	–	–	–
5	S_0	1.0	–	–	–	1.1	–	–	–
6	S_1	1.0	–	–	–	1.1	–	–	–
7	S_2	1.0	–	–	–	1.1	–	–	–
8	F_0	–	22	22	22	–	20	11	22
9	F_1	–	22	22	22	–	20	11	22
10	GND	–	–	–	–	–	–	–	–
11	F_2	–	22	22	22	–	20	11	22
12	F_3	–	22	22	22	–	20	11	22
13	$\overline{G}$ or OVR*	–	22	44	44	–	20	44	44
14	$\overline{P}$ or C_{n+4}	–	22	22	22	–	20	11	22
15	C_n	3.0**	–	–	–	4.4	–	–	–
16	B_3	4.0	–	–	–	4.4	–	–	–
17	A_3	4.0	–	–	–	4.4	–	–	–
18	B_2	4.0	–	–	–	4.4	–	–	–
19	A_2	4.0	–	–	–	4.4	–	–	–
20	V_{CC}	–	–	–	–	–	–	–	–

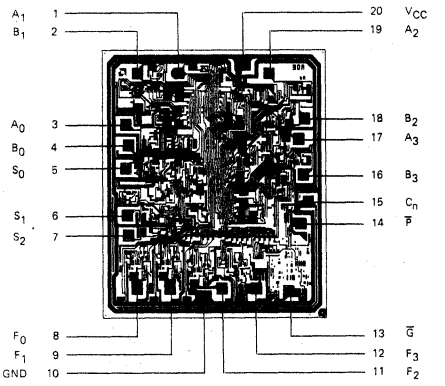
*OVR Drive is 22 Unit Loads.
**4.0 for Am25LS2517.

Am25LS • Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

Metallization and Pad Layout



DIE SIZE 0.091" X 0.108"

USER NOTES

1. Throughout this data sheet, the active HIGH input and output terminology has been used.
2. Arithmetic operations are performed on a word basis.
3. Logic operations are performed on a bit basis.
4. Arithmetic in 1's complement notation requires an end around carry.
5. Subtraction in 2's complement notation requires a carry in (C_n = HIGH) for the active HIGH case.

Understanding the Am25LS2517 and the Am25LS381

By John R. Mick

INTRODUCTION

The heart of most digital arighmetic processors is the arithmetic logic unit (ALU). The ALU can be thought of as a digital subsystem that performs various arithmetic and logic operations on two digital input variables. The Am25LS2517 and the Am25LS381 are Schottky TTL arithmetic logic units/function generators that perform eight arithmetic/logic operations on two four-bit input variables. In most ALU's, speed is generally a key ingredient. Therefore, as much parallelism in the operation of the arithmetic logic unit as possible is desired.

The Am25LS381 ALU is designed to operate with a '182 carry lookahead generator to perform multi-level full carry lookahead over any number of bits. Therefore, the Am25LS381 has both the carry generate and carry propagate outputs required by the '182 carry lookahead generator. The Am25LS2517, on the other hand, does not have the carry generate and carry propagate functions, but rather has the carry output (C_{n+4}) and a two's complement overflow detection signal (OVR) available at the output. The net result is that a very high-speed 16-bit arithmetic logic unit/function generator can be designed and assembled using three Am25LS381's, one Am25LS2517, and one Am2902 (the Am2902 is a high-speed version of the '182 carry lookahead generator).

UNDERSTANDING THE FULL ADDER

The results of an arithmetic operation in any position in a word depends not only on the two-input operand bits at that position, but also on all the lesser significant operand bits of the two input variables. The final result for any bit, therefore, is not available until the carries of all the previous bits have rippled through the logic array starting from the least significant bit and propagating through to the most significant bit. A full adder is a device that accepts two individual operand bits at the same binary weight, and also accepts a carry input bit from the next lesser significant weight full adder. The full adder then produces the sum bit for this bit position and also produces a carry bit to be used in the next more significant weight full adder carry input. The truth table for a full adder is shown in Figure 1. From this truth table, the equations for the full adder:

$S = A \oplus B \oplus C$

$C_0 = AB + BC + AC,$

where A and B are the input operands to the full adder and C is the carry input into the adder.

The sum output, S, represents the sum of the A and B operand inputs and the carry input. The carry output, C_0, represents the carry out of this cell and can be used in the next more significant cell of the adder. Full adder cells can be cascaded as depicted in Figure 2 to form a four-bit ripple carry parallel adder.

Inputs			Outputs	
A	B	C	S	C_0
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 1. Full Adder Truth Table.

Note that once we have cascaded devices as shown in Figure 2, we may wish to discuss the equations for the i-th bit of the adder. In so doing, we might describe the equations of the full adder as follows:

$S_i = A_i \oplus B_i \oplus C_i$

$C_{i+1} = A_iB_i + B_iC_i + A_iC_i$

where the A_i and B_i are the input operands at the i-th bit, and the C_i is the carry input to the i-th bit. (Note that the equations for this adder are iterative in nature and each depends on the result of the previous lesser significant bits of the adder array.)

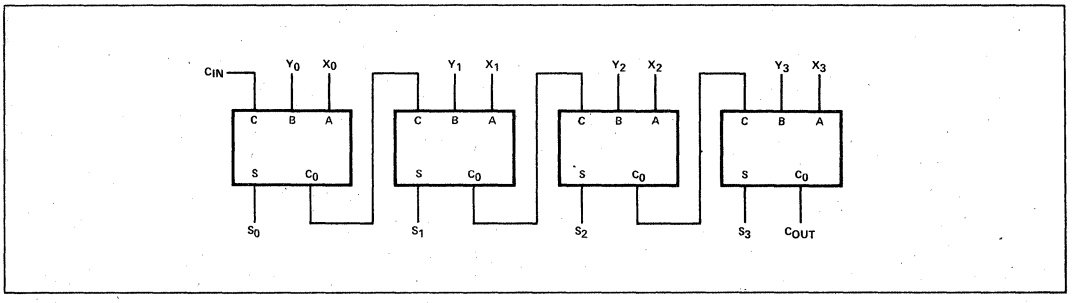


Figure 2. Cascaded Full Adder Cells Connected as a Four-Bit Ripple-Carry Full Adder.

The connection scheme shown in Figure 2 requires a ripple propagation time through each full adder cell. If a 16-bit adder is to be assembled, the carry will have to propagate through all 16 full adder cells. What is desired is some technique for anticipating the carry such that we will not have to wait for a ripple carry to progagate through the entire network. By using some additional logic, such an adder array can be constructed. This type of adder is usually called a carry lookahead adder.

A FOUR-BIT CARRY LOOKAHEAD ADDER

Looking back to the equations developed for i-th bit of an adder, let us now rewrite the carry equation in a slightly different form. When we factor the C_i in this equation, the new equation becomes:

$$C_{i+1} = A_iB_i + C_i (A_i + B_i)$$

From the above equation, let us now define two additional equations. These are:

$$G_i = A_iB_i$$

$$P_i = A_i + B_i$$

With these two new auxiliary equations, we can now rewrite the carry equation for the i-th bit as follows:

$$C_{i+1} = G_i + P_iC_i$$

Note that we have now developed two terms: the P_i term is known as carry propagate and the G_i term is known as carry generate. An anticipated carry can be generated at any stage of the adder by implementing the above equations and using the auxiliary functions P_i and G_i as required.

It is interesting to note that the sum equation can also be written in terms of these two auxiliary equations, P_i and G_i. For this case, the equation is:

$$S_i = (A_i + B_i) (A_iB_i) \oplus C_i$$

The auxiliary function G_i is called carry generate, because if it is true, then a carry is immediately produced for the next adder stage. The function P_i is called carry propagate because it implies there will be a carry into the next stage of the adder if there is a carry into this stage of the adder. That is, G_i causes a carry signal at the i-th stage of the adder to be generated and presented to the next stage of the adder while P_i causes an existing carry at the input to the i-th stage of the adder to propagate to the next stage of the adder.

Let us now write all of the sum and carry equations required for a full four-bit lookahead carry adder.

$$S_0 = A_0 \oplus B_0 \oplus C_0$$
$$S_1 = A_1 \oplus B_1 \oplus [G_0 + P_0C_0]$$
$$S_2 = A_2 \oplus B_2 \oplus [G_1 + P_1G_0 + P_1P_0C_0]$$
$$S_3 = A_3 \oplus B_2 \oplus [G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_0]$$
$$C_{i+4} = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_0$$

An important point to note is that all of the sum equations and the final carry output equation, C_{i+4}, can be written in terms of the A_i, B_i, and C_0 inputs to the four-bit adder. The configuration as described above is shown in Figure 3. This figure is divided into two parts — the upper blocks show the auxiliary function generator circuitry required to implement the P_i and G_i equations while the lower block implements the logic required to generate the sum output at each bit position.

A serious drawback to the lookahead carry adder is that as the word length is increased, the carry functions become more and more complex, eventually becoming impractical due to the large number of interconnections and heavy loading of the G_i and P_i functions. The auxiliary function concept can be extended, however, by dividing the word length into fairly small increments and defining blocks of auxiliary functions G and P.

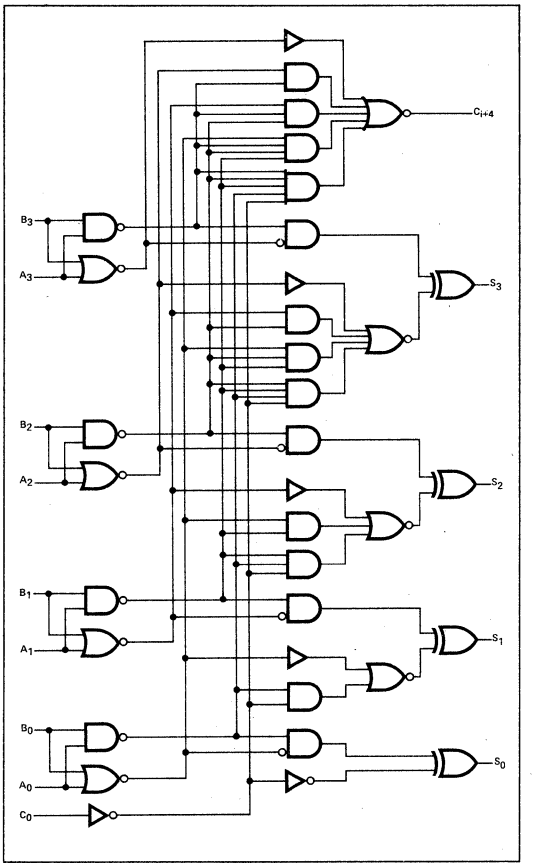


Figure 3. Full Four-Bit Carry-Lookahead Adder.

It is possible for a given block, to define a function G as the carry out generated with the block; and P can be defined as the carry propagate over the block. If the block size is set at four bits, then the functions for G and P for this block can be defined as follows:

$$G = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$$

$$P = P_3P_2P_1P_0$$

It is important to note that neither of these terms involves a carry-in (C_0) to the block, so no matter how many blocks are tied in an adder, all the blocks have stable G and P functions available in a minimum number of gate delays.

The G and P functions can be gated to produce a carry-in to each four-bit block, as a function of the lesser significant blocks. The carry-in to a block in is therefore:

$$C_n = G_{n-1} + P_{n-1}G_{n-2} + P_{n-1}P_{n-2}G_{n-3} + \ldots + P_{n-1}P_{n-2}P_{n-3} \ldots P_2P_1P_0C_0$$

Finally, the carry-in to each of the bits in a four-bit block must include a term for the actual least significant carry-in; note, therefore, that the equations for the four-bit full adder presented above include a term for carry-in at each bit position. Figure 4 shows the logic diagram for the Am25LS381 arithmetic logic unit/function generator while Figure 5 shows the logic diagram for the Am25LS2517 arithmetic logic unit/function generator. Note the generate and propagate outputs

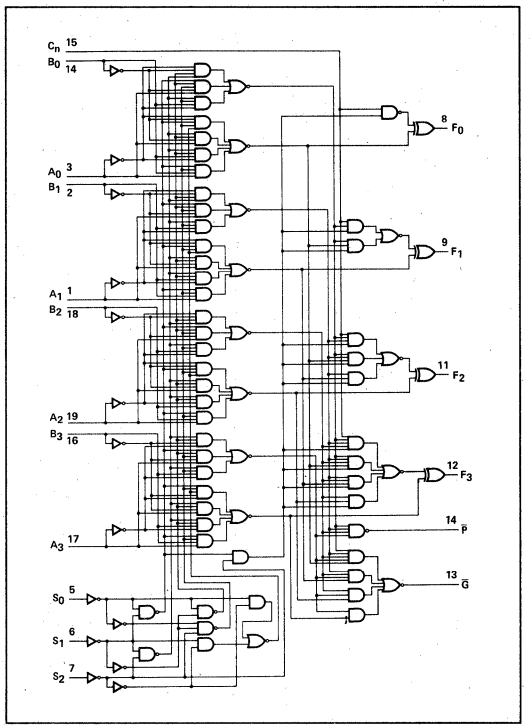


Figure 4. Logic Diagram of The Am25LS381.

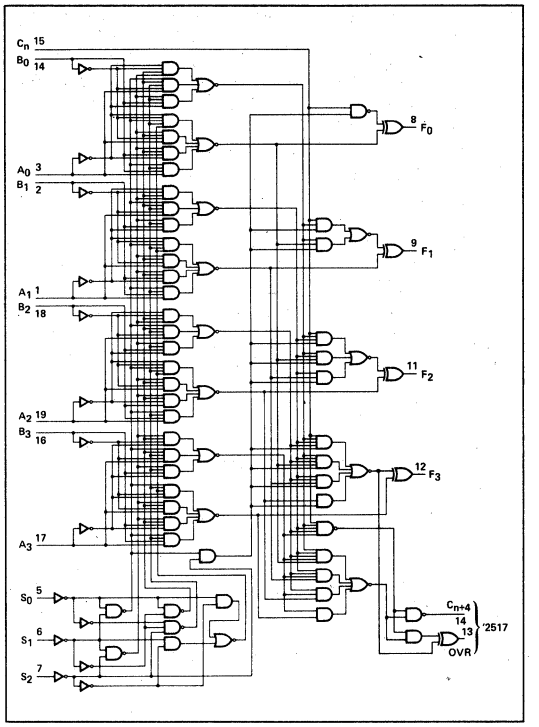


Figure 5. Logic Diagram of the Am25LS2517.

on the Am25LS381, and the carry output and overflow output on the Am25LS2517. Figure 6 gives the function table for both the Am25LS2517 and Am25LS381. Figure 7 shows the technique for cascading three Am25LS381's, one Am25LS2517, and one Am2902 in a full 16-bit high-speed carry lookahead connection. Figure 8 shows a connection scheme using only four Am25LS2517's in a 16-bit arithmetic logic unit connection where the carries are rippled between the devices. Each Am25LS2517 does use internal carry lookahead over the four-bit block.

In summary, the ripple carry method can be used in conjunction with the lookahead technique in several ways.

1. Lookahead carry over sections of the adder and ripple carry between these sections of the adder can be used. This method is often the most efficient in terms of hardware for

Selection			Arithmetic/Logic Operation
S_2	S_1	S_0	
L	L	L	Clear
L	L	H	B Minus A
L	H	L	A Minus B
L	H	H	A Plus B
H	L	L	A ⊕ B
H	L	H	A + B
H	H	L	AB
H	H	H	Preset

H = High Level, L = Low Level

Figure 6. Function Table for the Am25LS2517 and Am25LS381.

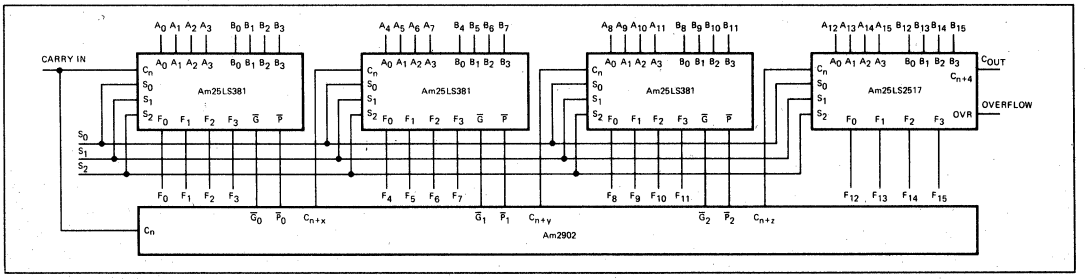


Figure 7. Full Lookahead Carry 16-Bit Adder.

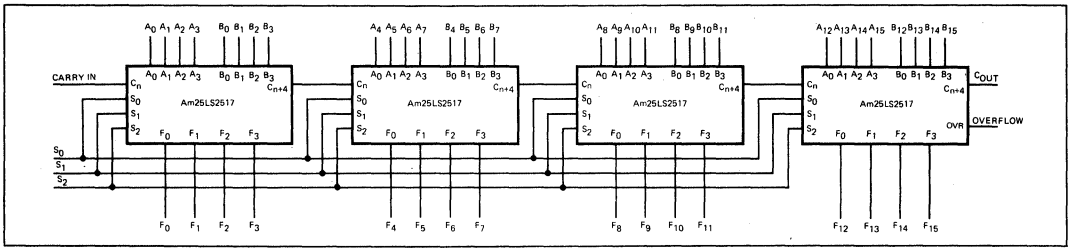


Figure 8. Connection of 16-Bit ALU Using Ripple Carry.

a given speed requirement. It does not require the use of a lookahead carry generator such as the Am2902.

2. Lookahead carry across 16-bit blocks with a ripple carry between 16-bit blocks can be used. This technique is usually called two-level carry lookahead addition. This technique results in very high-speed arithmetic function generation and makes a reasonable tradeoff between the speed and hardware for word lengths greater than 16 bits.
3. Full lookahead carry across all levels and all block sizes can be used. This is the highest speed arithmetic logic unit connection scheme. For word sizes up to 64 bits, it is referred to as three-level lookahead carry addition. Such a 64-bit ALU requires the use of five Am2902 carry lookahead generator units in addition to the 15 Am25LS381 devices and one Am25LS2517 as shown in Figure 9.

OVERFLOW

When two's complement numbers are added or subtracted, the result must lie within the range of the numbers that can be handled by the operand word length. Numbers are normally represented either as fractions with a binary point between the sign bit and the rest of the word, or as integers where the binary point is after the least significant bit. The actual choice for the location of the binary point is really up to the design engineer, as the hardware configuration required for either technique is identical. It is also possible to use number notations that include both integer and fractional representations in the same numbering scheme. Overflow is defined as the situation where the result of an arithmetic operation lies outside of the number range that can be represented by the number of bits in the word. For example, if two eight-bit numbers are added and the result does not lie within the number range that can be represented by an eight-bit word, we say that an overflow has occured. This can happen at either the positive end of the number range or at the negative end of the number range. The logic function that indicates that the result of an operation is outside of the representable number range is:

$$OVR = C_S \oplus C_{S+1}$$

where C_S is the carry-in to the sign bit and C_{S+1} is the carry-out of the sign bit.

Thus, for a four-bit ALU with the sign bit in the most significant bit position, the overflow can be defined as the C_{n+4} term exclusive OR'ed with the C_{n+3} term.

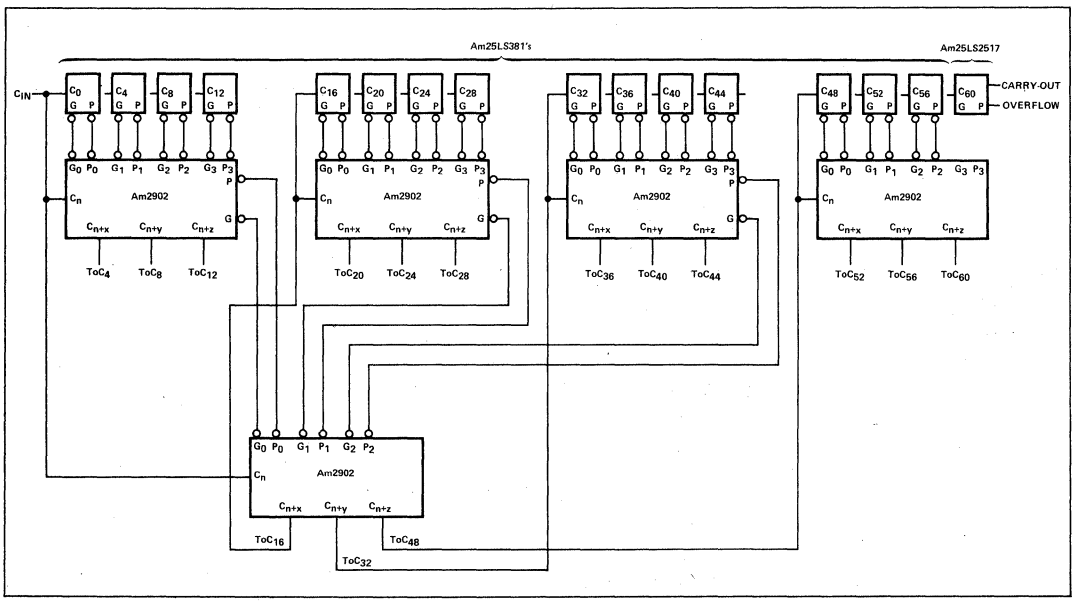


Figure 9. 64-Bit ALU with Full Carry Lookahead Using 5 Am2902's, 15 Am25LS381's and 1 Am25LS2517.

SPEED OR DELAY

Usually, the most important parameter in the design of any arithmetic logic unit is speed. How fast can two numbers be added? Is ripple carry sufficient or should carry lookahead over the entire adder array be used? In order to answer these questions, the design engineer must first evaluate the speed of the ALU required in his system. Then he can evaluate the various alternatives based on the number of bits in the word being used in the design.

The calculation of the speed (add or subtract time) of a 16-bit adder is straightforward and will be discussed in detail. It should be mentioned that the speed of the adder while in the logic mode is simply the propagation delay from the A_i or B_i inputs to the F_i outputs (35ns maximum at 25°C and 5V for the Am25LS2517).

LOOKAHEAD CARRY

The typical method for building 16-bit ALU's is to employ a carry lookahead generator such as the Am2902. Such a 16-bit design would incorporate three Am25LS381's, one Am25LS 2517, and one Am2902. For the 16-bit full carry lookahead adder in the add or subtract mode as shown in Figure 7, the maximum propagation delay for data-in to data-out is calculated as follows:

DATA PATH DELAY
16-BIT LOOKAHEAD ADDER/SUBTRACTOR
(+5V and 25°C Maximum Delays)

Path	Output			Units
	F_i	C_{n+4}	OVR	
A_i or B_i to $\overline{G}$ or $\overline{P}$	27	27	27	ns
G_i or P_i to C_{i+j} (Am2902)	10	10	10	ns
C_n to F_i	23	–	–	ns
C_n to C_{n+4} or OVR	–	22	22	ns
TOTAL 16-bit delay	60	59	59	ns

The data path for this computation begins at the least significant 4-bit device, propagates through the Am2902, and then ends at the most significant 4-bit device. Actually, the delay to the outputs of the most significant device (MSD), then second MSD, or third MSD is identical.

Thus, the above speed is identical if a 12-bit ALU is fabricated. This results because the same types of combinatorial propagation delays are involved.

We should also investigate the delay of this adder with regard to the select inputs as shown in Figure 7. Again, we may calculate the 16-bit full carry lookahead add/subtract delay as follows:

16-BIT LOOKAHEAD ADDER DELAY
FOR SELECT INPUTS
(+5V and 25°C Maximum Delays)

Path	Output			Units
	F_i	C_{n+4}	OVR	
S_i to $\overline{G}$ or $\overline{P}$	48	48	48	ns
G_i or P_i to C_{i+j} (Am2902)	10	10	10	ns
C_n to F_i	23	–	–	ns
C_n to C_{n+4} or OVR	–	22	22	ns
TOTAL 16-bit delay	81	80	80	ns

Let us examine the speed of a 64-bit arithmetic logic unit fabricated as shown in Figure 9. The worst case path for this design is as follows:

DATA PATH DELAY
64-BIT LOOKAHEAD ADDER/SUBTRACTOR
(+5V and 25°C Maximum Delays)

Path	Output			Units
	F_i	C_{n+4}	OVR	
A_i or B_i to $\overline{G}$ or $\overline{P}$	27	27	27	ns
G_i or P_i to G_i or P_i (Am2902)	14	14	14	ns
G_i or P_i to C_{i+j} (Am2902)	10	10	10	ns
C_n to C_{i+j} (Am2902)	14	14	14	ns
C_n to F_i	23	–	–	ns
C_n to C_{n+4} or OVR	–	22	22	ns
TOTAL 16-bit delay	88	87	87	ns

The above example demonstrates the speed improvement when using carry lookahead over the entire array. When this 64-bit example is compared with the previous 16-bit example, it will be found that the only difference is the addition of two Am2902 delays.

RIPPLE CARRY

The slowest speed ALU design employs the ripple carry technique. When four-bit devices such as the Am25LS2517 are employed in such an ALU, the speed is usually computed using the combinatorial delay terms in the following manner.

1. Select the longest combinatorial delay in the least significant device from any input to the carry output, C_{n+4}. This is usually from the A or B inputs to the carry output.
2. Add the carry input to carry output propagation delay as many times as required to represent each of the intermediate four-bit ALU's.
3. Finally, take the propagation delay from the carry input to the ALU adder outputs.

When the above rules are followed, the total worst case propagation delay over the entire ALU bit width is derived.

If we consider the ripple carry adder/subtractor configuration as shown in Figure 8, the propagation delay for the data input to data output path is computed as follows:

DATA PATH DELAY
16-BIT RIPPLE CARRY ADDER/SUBTRACTOR
(+5V and +25°C Maximum Delays)

Path	Output			Units
	F_i	C_{n+4}	OVR	
A_i or B_i to C_{n+4}	36	36	36	ns
C_n to C_{n+4}	22	22	22	ns
C_n to C_{n+4}	22	22	22	ns
C_n to F_i	23	–	–	ns
C_n to C_{n+4} or OVR	–	22	22	ns
TOTAL 16-bit delay	103	102	102	ns

In this connection, the maximum delay begins at the least significant device and propagates through the most significant device via the ripple carry path.

The select to output delay is computed in a similar manner using S_i to C_{n+4} as the first term and is found to be:

S_i to F_i = 122ns; S_i to C_{n+4} = 12ns; S_i to OVR = 121ns

The ripple carry computational examples show the speed of a 16-bit ALU function/generator built using four Am25LS 2517's.

COMPARING THE '2517/'381 WITH THE '181

To compare the performance of the Am25LS2517 and LS381, we should evaluate the various '181 ALU's connected in a 16-bit configuration with the Am2902 carry lookahead generator used in all configurations as shown in Figure 7. The comparison for the A_i or B_i to F_i add/subtract time is as follows:

COMPARISON OF 16-BIT ADDER/SUBTRACTOR DATA DELAY USING 4 ALU's AND 1 Am2902

ALU Device	Maximum Add/Subtract Delay +5V and 25°C	Maximum Power* V_{CC} = +5.25V
Am74S181	37ns	914mA
Am74181	64ns	694mA
Am74LS181	69ns	242mA
Am25LS181	55ns	242mA
Am25LS381/Am25LS2517	60ns	266mA

*Note: Of this power, 94mA is the Am2902

Even more important is the comparison of "System Speed" normally associated with the ALU function. If we assume the system configuration as shown in Figure 10, then a reasonable comparison of speed for A_i or B_i to OVERFLOW can be made as follows:

SPEED AND POWER FOR ALU SYSTEMS OF FIGURE 10

Path	All "S"	All 25LS	All 74LS	All Gold Doped	'LS381 'LS2517	Units
A_i or B_i to G or P	15	26	33	25	27	ns
G or P to C_{i+j} (Am2902)	10	10	10	10	10	ns
C_n to OVR	–	–	–	–	22	ns
C_n to F_3	12	19	26	19	–	ns
C_{out} to OVR	21	–	60	60	–	ns
TOTAL	58	55	129	114	59	ns
POWER	998		253	748	266	mA

*no 25LS

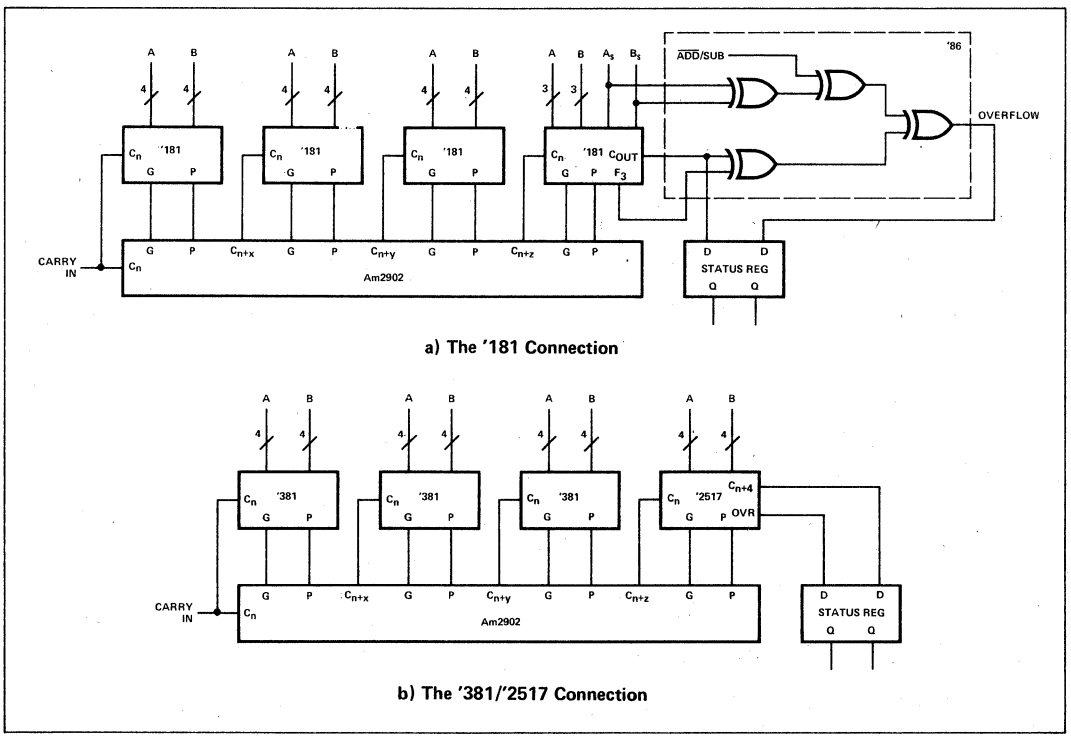


Figure 10. The Normal ALU System.

SUMMARY

The Am25LS381 and Am25LS2517 offer superior performance utilizing the space saving 20-pin package. The data add/subtract time compares very favorably with the 74181 and 74S181 with a considerable reduction (1/3 to 1/4) in dissipated power. The Am25LS381 and Am25LS2517 combination provide the OVR function not currently available or easily to implement on any '181 configuration. The 20-pin package configuration offers at least a 2:1 saving in PC board area compared to the '181 24-pin package approach.

Am25LS2518

Quad D Register with Standard and Three-State Outputs

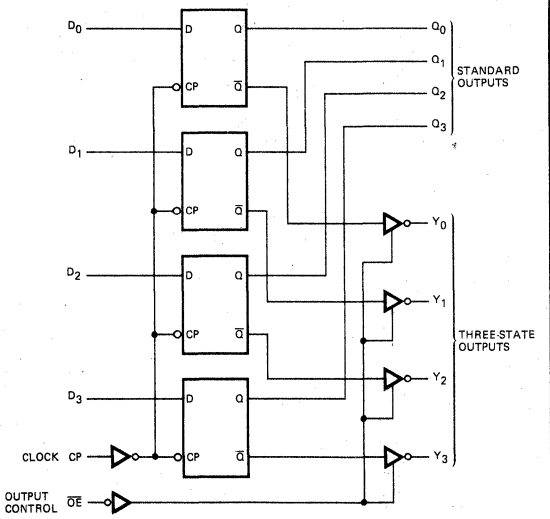
DISTINCTIVE CHARACTERISTICS

- Low-power Schottky version of the popular Am2918 and Am25S18
- Four standard totem-pole outputs
- Four three-state outputs
- Four D-type flip-flops
- Second sourced by T. I. as the SN54/74LS388

RELATED PRODUCTS

Part No.	Description
Am25S18	Quad D Register
Am2918	Quad D Register
Am29LS18	Quad D Low Power Register
Am29LS2519	Quad D Low Power Register

LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0 to +70°C	AM25LS2518PC
Hermetic DIP	0 to +70°C	AM25LS2518DC
Chip-Pak	0 to +70°C	AM25LS2518LC
Dice	0 to +70°C	AM25LS2518XC
Hermetic DIP	−55 to +125°C	AM25LS2518DM
Hermetic Flat Pak	−55 to +125°C	AM25LS2518FM
Chip-Pak	−55 to +125°C	AM25LS2518LM
Dice	−55 to +125°C	AM25LS2518XM

FUNCTIONAL DESCRIPTION

The Am25LS2518 consists of four D-type flip-flops with a buffered common clock. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

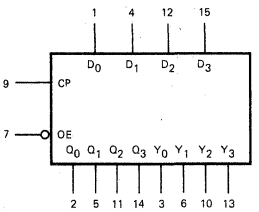
The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" ($\overline{OE}$) input is LOW. When the $\overline{OE}$ input is HIGH, the Y outputs are in the high-impedance state.

The Am25LS2518 is a 4-bit, high-speed register intended for use in real-time signal processing systems where the standard outputs are used in a recursive algorithm and the three-state outputs provide access to a data bus to dump the results after a number of iterations.

The device can also be used as an address register or status register in computers or computer peripherals.

Likewise, the Am25LS2518 is also useful in certain display applications where the standard outputs can be decoded to drive LED's (or equivalent) and the three-state outputs are bus organized for occasional interrogation of the data as displayed.

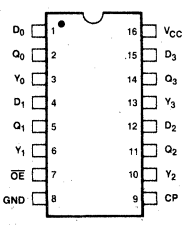
LOGIC SYMBOL



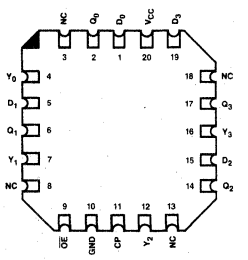
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
Top Views

D16, P16



Leadless Chip Carrier L-20-1



Note: Pin 1 is marked for orientation.

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	T_A = 0°C to +70°C	V_{CC} = 5.0 V ±5%	MIN. = 4.75 V	MAX. = 5.25 V
MIL	T_A = −55°C to +125°C	V_{CC} = 5.0 V ±10%	MIN. = 4.50 V	MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Q, I_{OH} = −660μA	MIL	2.5	3.4		Volts
				COM'L	2.7	3.4		
			Y	MIL, I_{OH} = −1.0mA	2.4	3.4		
				COM'L, I_{OH} = −2.6mA	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
			I_{OL} = 12mA				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V					−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7 V					20	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0 V					0.1	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	V_O = 0.4 V				−20	μA
			V_O = 2.4 V				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				17	28	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} is measured with all inputs at 4.5V and all outputs open.

9

Am25LS

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

Am25LS2518
SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Q_i			18	27	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}				18	27		
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)			18	27	ns	
t_{PHL}				18	27		
t_{pw}	Clock Pulse Width	LOW	18			ns	
		HIGH	15				
t_s	Data		15			ns	
t_h	Data		5.0			ns	
t_{ZH}	$\overline{OE}$ to Y_i			7.0	11	ns	
t_{ZL}				8	12		
t_{HZ}	$\overline{OE}$ to Y_i			14	21	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				12	18		
f_{max}	Maximum Clock Frequency (Note 1)		35	50		MHz	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%		Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%		Units	Test Conditions
			Min.	Max.	Min.	Max.		
t_{PLH}	Clock to Q_i			38		45	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}				38		45		
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)			35		40	ns	
t_{PHL}				35		40		
t_{pw}	Clock Pulse Width	LOW	20		20		ns	
		HIGH	20		20			
t_s	Data		15		15		ns	
t_h	Data		5.0		5.0		ns	
t_{ZH}	$\overline{OE}$ to Y_i			15		17	ns	
t_{ZL}				16		17		
t_{HZ}	$\overline{OE}$ to Y_i			27		30	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				24		30		
f_{max}	Maximum Clock Frequency (Note 1)		30		25		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

D_i The four data inputs to the register.

Q_i The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.

Y_i The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the Y_i outputs to the high-impedance state.

CP Clock. The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.

$\overline{OE}$ Output Control. When the $\overline{OE}$ input is HIGH, the Yi outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

TRUTH TABLE

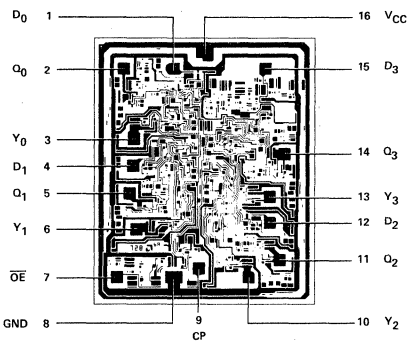
INPUTS			OUTPUTS		NOTES
$\overline{OE}$	CLOCK CP	D	Q	Y	
H	L	X	NC	Z	–
H	H	X	NC	Z	–
H	↑	L	L	Z	–
H	↑	H	H	Z	–
L	↑	L	L	L	–
L	↑	H	H	H	–
L	–	–	L	L	1
L	–	–	H	H	1

L = LOW
H = HIGH
X = Don't care

NC = No change
↑ = LOW to HIGH transition
Z = High impedance

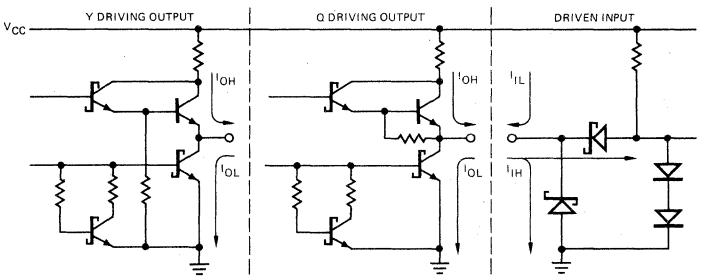
Note: 1. When $\overline{OE}$ is LOW, the Y output will be in the same logic state as the Q output.

Metallization and Pad Layout



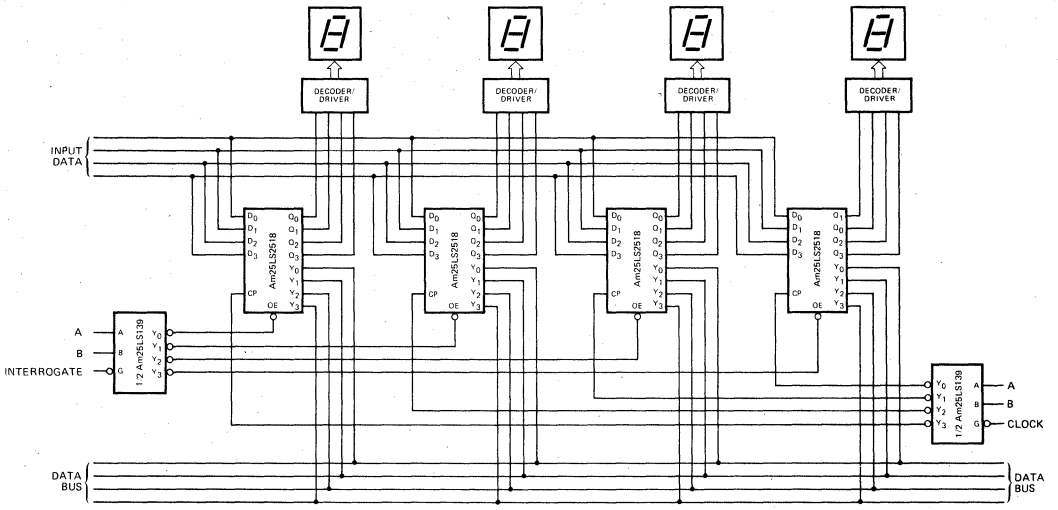
DIE SIZE 0.083" X 0.099"

Am25LS
LOW-POWER SCHOTTKY INPUT/OUTPUT
CURRENT INTERFACE CONDITIONS

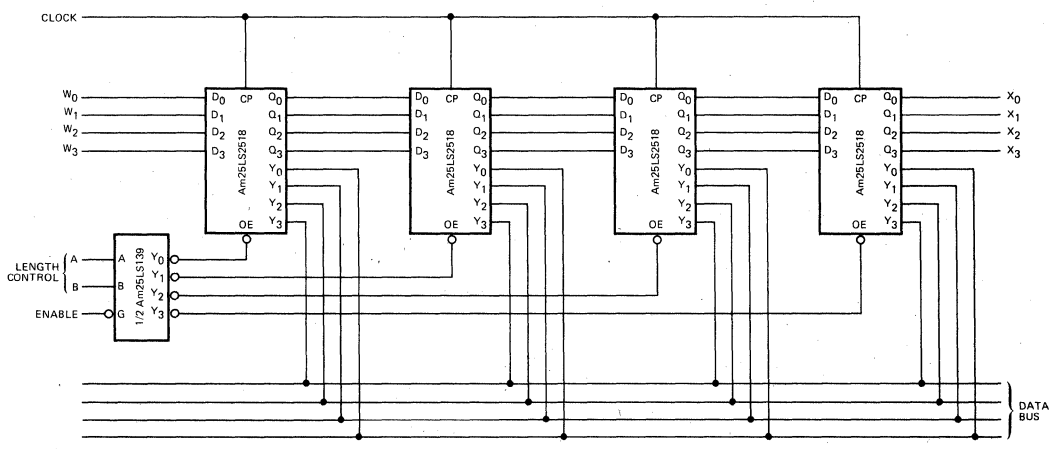


Note: Actual current flow direction shown.

APPLICATIONS



The Am25LS2518 used as display register with bus interrogate capability.



The Am25LS2518 as a variable length (1, 2, 3 or 4 word)shift register.

Am25LS2519

Quad Register with Two Independently Controlled Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Two sets of fully buffered three-state outputs
- Four D-type flip-flops
- Polarity control on W outputs
- Buffered common clock enable
- Buffered common asynchronous clear
- Separate buffered common output enable for each set of outputs

RELATED PRODUCTS

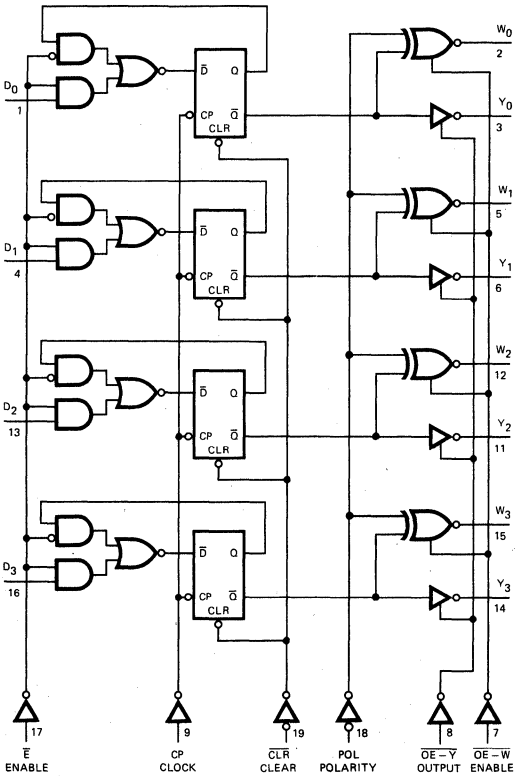
Part No.	Description
Am25S18, Am2918	Quad D Register
Am25LS2518	Quad D Register

FUNCTIONAL DESCRIPTION

The Am25LS2519 consists of four D-type flip-flops with a buffered common clock enable. Information meeting the set-up and hold time requirements of the D inputs is transferred to the flip-flop outputs on the LOW-to-HIGH transition of the clock. Data on the Q outputs of the flip-flops is enabled at the three-state outputs when the output control ($\overline{OE}$) input is LOW. When the appropriate $\overline{OE}$ input is HIGH, the outputs are in the high impedance state. Two independent sets of outputs – W and Y – are provided such that the register can simultaneously and independently drive two buses. One set of outputs contains a polarity control such that the outputs can either be inverting or non-inverting.

The device also features an active LOW asynchronous clear. When the clear input is LOW, the Q output of the internal flip-flops are forced LOW independent of the other inputs. The Am25LS2519 is packaged in a space saving (0.3-inch row spacing) 20-pin package.

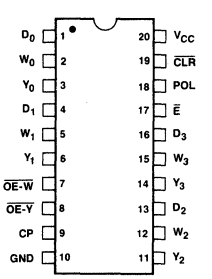
LOGIC DIAGRAM



ORDERING INFORMATION

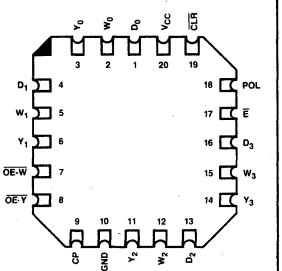
Package Type	Temperature Range	Order Number
Molded DIP	0 to +70°C	AM25LS2519PC
Hermetic DIP	0 to +70°C	AM25LS2519DC
Chip-Pak	0 to +70°C	AM25LS2519LC
Dice	0 to +70°C	AM25LS2519XC
Hermetic DIP	−55 to +125°C	AM25LS2519DM
Hermetic Flat-Pak	−55 to +125°C	AM25LS2519FM
Chip-Pak	−55 to +125°C	AM25LS2519LM
Dice	−55 to +125°C	AM25LS2519XM

CONNECTION DIAGRAMS – Top Views



Leadless Chip Carrier

L-20-1



Note: Pin 1 is marked for orientation.

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Am25LS2519

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	MIL, $I_{OH} = -1.0mA$		2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6mA$		2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$				0.4	Volts
			$I_{OL} = 8.0mA$				0.45	
			$I_{OL} = 12mA$				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$					−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$					20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$					0.1	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$				−20	μA
			$V_O = 2.4V$				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.		MIL		24	36	mA
				COM'L		24	39	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Inputs grounded; outputs open.

Am25LS

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PHL}	Clock to Y_i			22	33	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}				20	30		
t_{PLH}	Clock to W_i (Either Polarity)			24	36	ns	
t_{PHL}				24	36		
t_{PHL}	Clear to Y_i			29	43	ns	
t_{PLH}	Clear to W_i			25	37	ns	
t_{PHL}				30	45		
t_{PLH}	Polarity to W_i			23	34	ns	
t_{PHL}				25	37		
t_{pw}	Clear		18			ns	
t_{pw}	Clock Pulse Width	LOW	15			ns	
		HIGH	18				
t_s	Data		15			ns	
t_h	Data		5			ns	
t_s	Data Enable		20			ns	
t_h	Data Enable		0			ns	
t_s	Set-up Time, Clear Recovery (Inactive) to Clock		20	15		ns	
t_{ZH}	Output Enable to W or Y			11	17	ns	
t_{ZL}				13	20		
t_{HZ}	Output Enable to W or Y			13	20	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				11	17		
f_{max}	Maximum Clock Frequency (Note 1)		35	45		MHz	C_L = 15pF, R_L = 2.0kΩ

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Clock to Y_i			39		42	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}				39		45		
t_{PLH}	Clock to W_i (Either Polarity)			41		43	ns	
t_{PHL}				44		48		
t_{PHL}	Clear to Y_i			52		58	ns	
t_{PLH}	Clear to W_i			42		43	ns	
t_{PHL}				51		53		
t_{PLH}	Polarity to W_i			41		45	ns	
t_{PHL}				42		44		
t_{pw}	Clear		20		20		ns	
t_{pw}	Clock	LOW	20		20		ns	
		HIGH	20		20			
t_s	Data		15		15		ns	
t_h	Data		10		10		ns	
t_s	Data Enable		25		25		ns	
t_h	Data Enable		0		0		ns	
t_s	Set-up Time, Clear Recovery (Inactive) to Clock		23		24		ns	
t_{ZH}	Output Enable to W_i or Y_i			24		27	ns	
t_{ZL}				29		35		
t_{HZ}	Output Enable to W_i or Y_i			33		45	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				22		26		
f_{max}	Maximum Clock Frequency (Note 1)		30		25		MHz	C_L = 50pF, R_L = 2.0kΩ

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

FUNCTION TABLE

FUNCTION	INPUTS							INTERNAL	OUTPUTS	
	CP	D_i	$\overline{E}$	$\overline{CLR}$	POL	$\overline{OE\text{-}W}$	$\overline{OE\text{-}Y}$	Q	W_i	Y_i
Output Three-State Control	X	X	X	X	X	H	L	NC	Z	Enabled
	X	X	X	X	X	L	H	NC	Enabled	Z
	X	X	X	X	X	H	H	NC	Z	Z
	X	X	X	X	X	L	L	NC	Enabled	Enabled
W_i Polarity	X	X	X	X	L	L	L	NC	Non-Inverting	Non-Inverting
	X	X	X	X	H	L	L	NC	Inverting	Non-Inverting
Asynchronous Clear	X	X	X	L	L	L	L	L	L	L
	X	X	X	L	H	L	L	L	H	L
Clock Enabled	↑	X	H	H	X	X	X	NC	NC	NC
	↑	L	L	H	L	L	L	L	L	L
	↑	L	L	H	H	L	L	L	H	L
	↑	H	L	H	L	L	L	H	H	H
	↑	H	L	H	H	L	L	H	L	H

L = LOW
H = HIGH
Z = High Impedance
X = Don't Care
NC = No Change
↑ = LOW to HIGH Transition

DEFINITION OF FUNCTIONAL TERMS

D_i — Any of the four D flip-flop data lines.

$\overline{E}$ — Clock Enable. When LOW, the data is entered into the register on the next clock LOW-to-HIGH transition. When HIGH, the data in the register remains unchanged, regardless of the data in.

CP — Clock Pulse. Data is entered into the register on the LOW-to-HIGH transition.

$\overline{OE\text{-}W}$, $\overline{OE\text{-}Y}$ — Output Enable. When $\overline{OE}$ is LOW, the register is enable to the output. When HIGH, the output is in the high-impedance state. The $\overline{OE\text{-}W}$ controls the W set of outputs, and $\overline{OE\text{-}Y}$ controls the Y set.

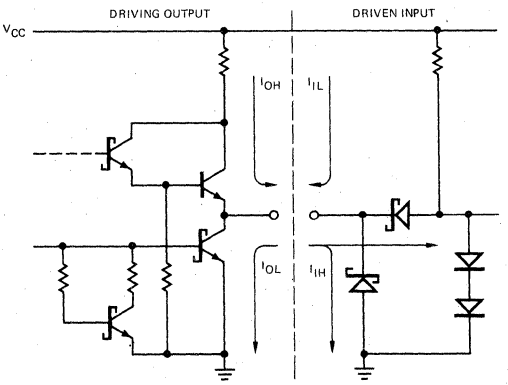
Y_i — Any of the four non-inverting three-state output lines.

W_i — Any of the four three-state outputs with polarity control.

POL — Polarity Control. The W_i outputs will be non-inverting when POL is LOW, and when it is HIGH, the outputs are inverting.

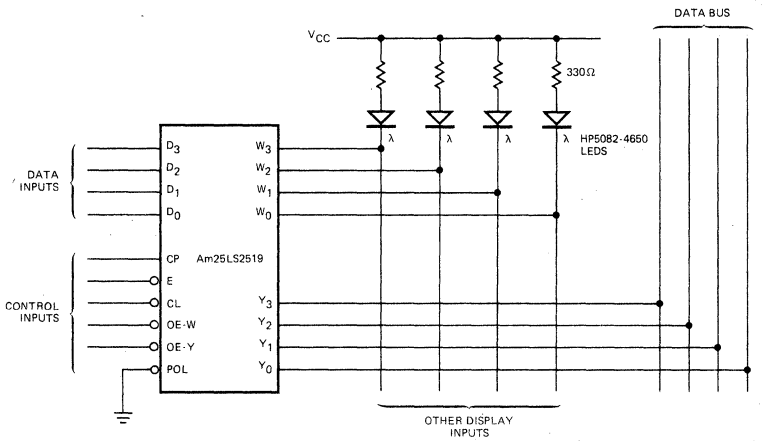
$\overline{CLR}$ — Asynchronous Clear. When $\overline{CLR}$ is LOW, the internal Q flip-flops are reset to LOW.

Am25LS
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



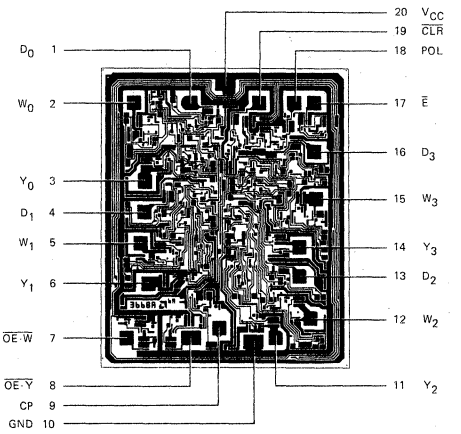
Note: Actual current flow direction shown.

APPLICATION



Convenient Register Content Monitor or Test Point

Metallization and Pad Layout



DIE SIZE 0.083" X 0.099"

Am25LS2520

Octal D-Type Flip-Flop with Clear, Clock Enable and Three-State Control

DISTINCTIVE CHARACTERISTICS

- Buffered common clock enable input
- Buffered common asynchronous clear input
- Three-state outputs
- 8-bit, high-speed parallel register with positive edge-triggered, D-type flip-flops
- Am25LS Family offers improved sink current, source current and noise margin

RELATED PRODUCTS

Part No.	Description
Am25S18	Quad D Register
Am2920	Octal D-Type Flip-Flop
Am2954/5	Octal D Registers

FUNCTIONAL DESCRIPTION

The Am25LS2520 is an 8-bit register built using advanced Low-Power Schottky technology. The register consists of eight D-type flip-flops with a buffered common clock, a buffered common clock enable, a buffered asynchronous clear input, and three-state outputs.

When the clear input is LOW, the internal flip-flops of the register are reset to logic 0 (LOW), independent of all other inputs. When the clear input is HIGH, the register operates in the normal fashion.

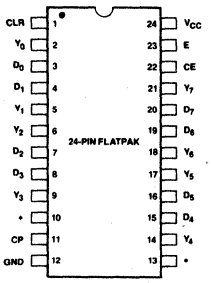
When the three-state output enable ($\overline{OE}$) input is LOW, the Y outputs are enabled and appear as normal TTL outputs. When the output enable ($\overline{OE}$) input is HIGH, the Y outputs are in the high impedance (three-state) condition. This does not affect the internal state of the flip-flop Q output.

The clock enable input ($\overline{E}$) is used to selectively load data into the register. When the $\overline{E}$ input is HIGH, the register will retain its current data. When the $\overline{E}$ is LOW, new data is entered into the register on the LOW-to-HIGH transition of the clock input.

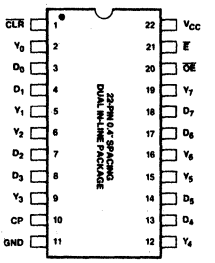
This device is packaged in a space-saving (0.4-inch row spacing) 22-pin package and in a 24-pin flatpack.

CONNECTION DIAGRAMS – Top Views

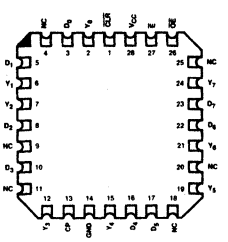
F-24



D-22, P-22

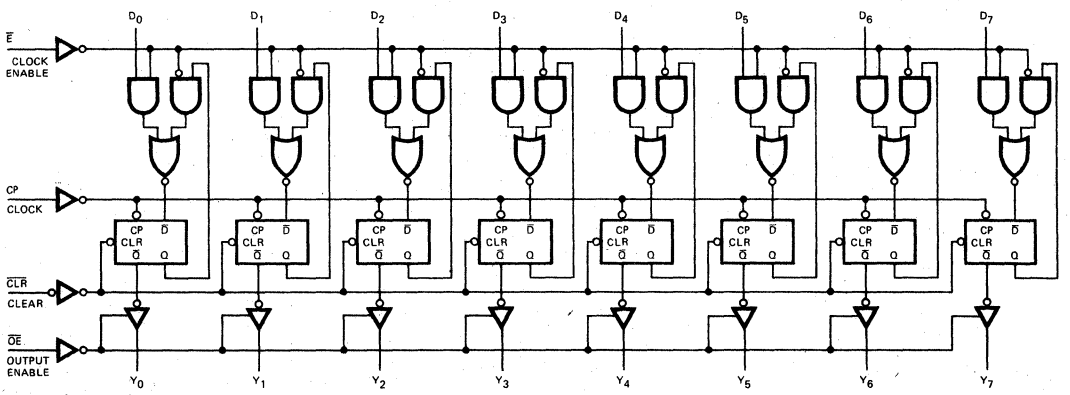


Leadless Chip Carrier
L-28-1



Note: Pin 1 is marked for orientation *Reserved – do not use.

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	MIL, $I_{OH} = -1.0mA$	2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6mA$	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$			0.4	Volts
			$I_{OL} = 8.0mA$			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$				0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$			−20	μA
			$V_O = 2.4V$			20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			24	37	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All outputs open; $\overline{E}$ = GND, Di inputs = CLR = $\overline{OE}$ = 4.5V. Apply momentary ground, then 4.5V to clock input.

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Am25LS

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

Am25LS2520
SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)			18	27	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}				24	36		
t_{PHL}	Clear to Y			22	35	ns	
t_s	Data (D_i)		10	3		ns	
t_h	Data (D_i)		10	3		ns	
t_s	Enable ($\overline{E}$)	Active	15	10		ns	
		Inactive	20	12			
t_h	Enable ($\overline{E}$)		0	0		ns	
t_s	Clear Recovery (In-Active) to Clock		11	7		ns	
t_{pw}	Clock	HIGH	20	14		ns	
		LOW	25	13			
t_{pw}	Clear		20	13		ns	
t_{ZH}	$\overline{OE}$ to Y_i			9	13	ns	
t_{ZL}				14	21		
t_{HZ}	$\overline{OE}$ to Y_i			20	30	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				24	36		
f_{max}	Maximum Clock Frequency (Note 1)			40		MHz	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)			33		39	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}				45		54		
t_{PHL}	Clear to Y			43		51	ns	
t_s	Data (D_i)		12		15		ns	
t_h	Data (D_i)		12		15		ns	
t_s	Enable ($\overline{E}$)	Active	17		20		ns	
		Inactive	20		23			
t_h	Enable ($\overline{E}$)		0		0		ns	
t_s	Clear Recovery (In-Active) to Clock		13		15		ns	
t_{pw}	Clock	HIGH	25		30		ns	
		LOW	30		35			
t_{pw}	Clear		22		25		ns	
t_{ZH}	$\overline{OE}$ to Y_i			19		25	ns	
t_{ZL}				30		39		
t_{HZ}	$\overline{OE}$ to Y_i			35		40	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				39		42		
f_{max}	Maximum Clock Frequency (Note 1)		25		20		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

D_i The D flip-flop data inputs.

$\overline{CLR}$ When the clear input is LOW, the Q_i outputs are LOW, regardless of the other inputs. When the clear input is HIGH, data can be entered into the register.

CP Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.

Y_i The register three-state outputs.

$\overline{E}$ Clock Enable, When the clock enable is LOW, data on the D_i input is transferred to the Q_i output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_i outputs do not change state, regardless of the data or clock input transitions.

$\overline{OE}$ Output Control. When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

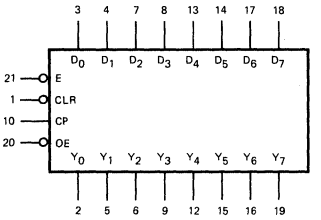
FUNCTION TABLE

	Inputs					Internal	Outputs
Function	$\overline{OE}$	$\overline{CLR}$	$\overline{E}$	D_i	CP	Q_i	Y_i
Hi-Z	H	X	X	X	X	X	Z
Clear	H	L	X	X	X	L	Z
	L	L	X	X	X	L	L
Hold	H	H	H	X	X	NC	Z
	L	H	H	X	X	NC	NC
Load	H	H	L	L	↑	L	Z
	H	H	L	H	↑	H	Z
	L	H	L	L	↑	L	L
	L	H	L	H	↑	H	H

H = HIGH
L = LOW
X = Don't Care

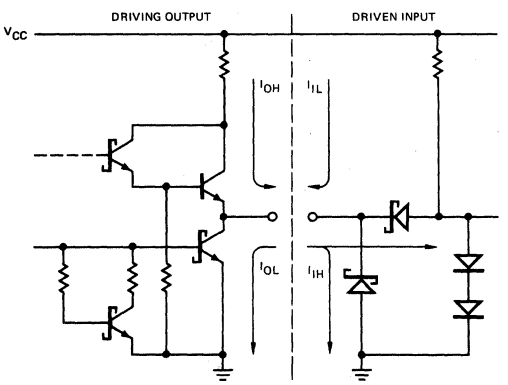
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

LOGIC SYMBOL



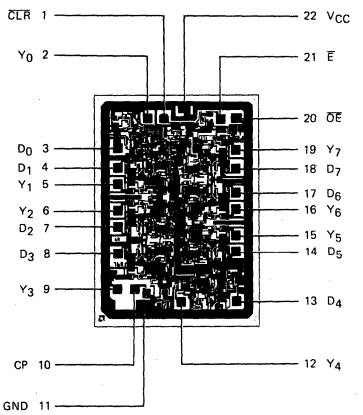
V_{CC} = Pin 22
GND = Pin 11

Am25LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

Metallization and Pad Layout



DIE SIZE 0.080" x 0.111"

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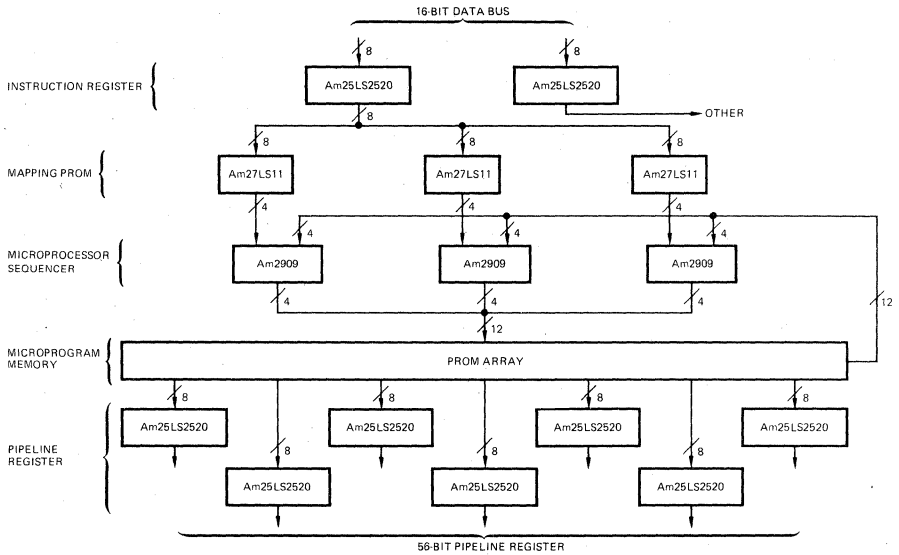
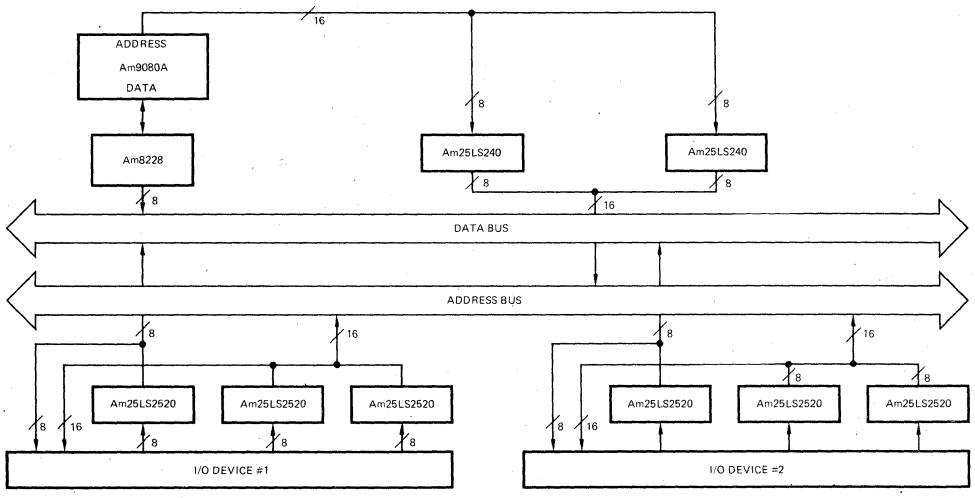
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0 to +70°C	AM25LS2520PC
Hermetic DIP	0 to +70°C	AM25LS2520DC
Chip-Pak	0 to +70°C	AM25LS2520LC
Dice	0 to +70°C	AM25LS2520XC
Hermetic DIP	−55 to +125°C	AM25LS2520DM
Hermetic Flat Pack	−55 to +125°C	AM25LS2520FM
Chip-Pak	−55 to +125°C	AM25LS2520LM
Dice	−55 to +125°C	AM25LS2520XM

APPLICATIONS



A typical Computer Control Unit for a microprogrammed machine.



The Am25LS2520 is a useful device in interfacing with the Am9080A system buses.

Am25LS2521

Eight-Bit Equal-to Comparator

DISTINCTIVE CHARACTERISTICS

- 8-bit byte oriented equal comparator
- Cascadable using $\overline{E}_{IN}$
- High-speed, Low-Power Schottky technology
- t_{pd} A • B to $\overline{E}_{OUT}$ in 9ns
- Standard 20-pin package

RELATED PRODUCTS

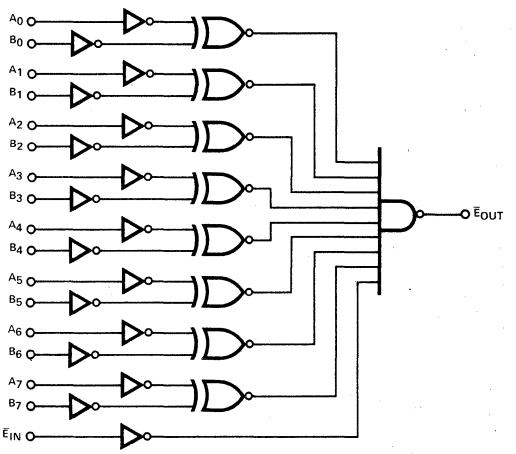
Part No.	Description
Am29806	Chip Select Decoder
Am29809	9-Bit Comparator

FUNCTIONAL DESCRIPTION

The Am25LS2521 is an 8-bit "equal to" comparator capable of comparing two 8-bit words for "equal to" with provision for expansion or external enabling. The matching of the two 8-bit inputs plus a logic LOW on the $\overline{E}_{IN}$ produces an active LOW on the output $\overline{E}_{OUT}$.

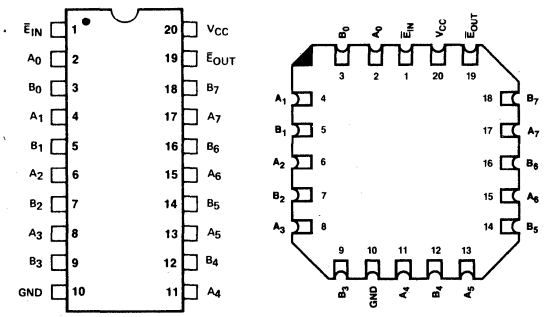
The logic expression for the device can be expressed as: $\overline{E}_{OUT} = \overline{(A_0 \odot B_0)\ (A_1 \odot B_1)\ (A_2 \odot B_2)\ (A_3 \odot B_3)\ (A_4 \odot B_4)\ (A_5 \odot B_5)\ (A_7 \odot B_7)\ E_{IN}}$. It is obvious that the expression is valid where $A_0 - A_7$ and $B_0 - B_7$ are expressed as either assertions or negations. This is also true for pair of terms i.e. A_0 can be compared with B_0 at the same time $\overline{A}_1$ is compared with $\overline{B}_1$. It is only essential that the polarity of the paired terms be maintained.

LOGIC DIAGRAM



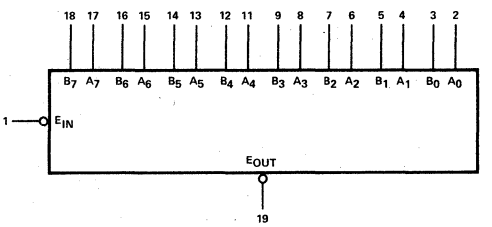
CONNECTION DIAGRAMS – Top Views

Leadless Chip Carrier
L-20-1



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



VCC = Pin 20
GND = Pin 10

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Am25LS2521

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -440\mu A$	MIL	2.5			Volts
				COM'L	2.7			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$				0.4	Volts
			$I_{OL} = 8.0mA$				0.45	
			$I_{OL} = 12mA$				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$		A_i, B_i			−0.36	mA
				$\overline{E}$			−0.72	
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$		A_i, B_i			20	μA
				$\overline{E}$			40	
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$		A_i, B_i			0.1	mA
				$\overline{E}$			0.2	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				27	40	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $\overline{E}$ = GND, all other inputs and outputs open.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to $+V_{CC}$ max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	A_i or B_i to $\overline{Equal}$		9	15	ns	C_L = 15pF R_L = 2.0kΩ
t_{PHL}			9	15		
t_{PLH}	$\overline{E}$ to $\overline{Equal}$		5	7	ns	
t_{PHL}			6	8		

SWITCHING CHARACTERISTICS OVER OPERATING RANGE *

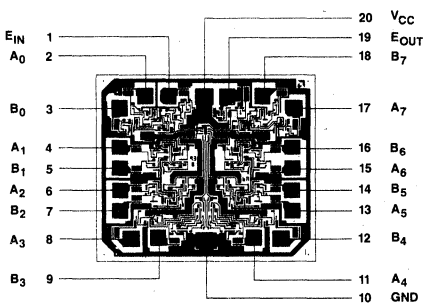
Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5% Min.	Max.	Am25LS MIL T_A = −55°C to +125°C V_{CC} = 5.0V ±10% Min.	Max.	Units	Test Conditions
t_{PLH}	A_i or B_i to $\overline{Equal}$ Output		20		22	ns	C_L = 50pF R_L = 2.0kΩ
t_{PHL}			19		21		
t_{PLH}	$\overline{E}$ to $\overline{Equal}$ Output		10.5		12	ns	
t_{PHL}			12.5		15		

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

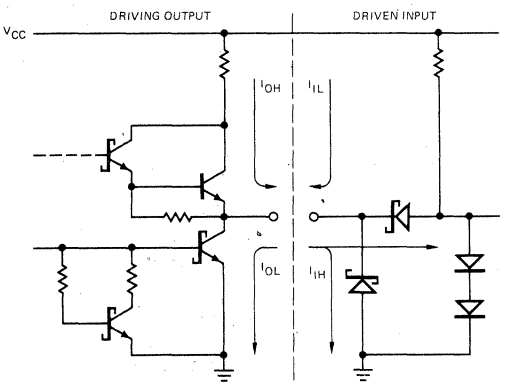
A_0–A_7	A input to comparator
B_0–B_7	B input to comparator
$\overline{E}_{IN}$	Enable active LOW
$\overline{E}_{OUT}$	$\overline{EQUAL}$ output active LOW

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.068" X 0.058"

Am25LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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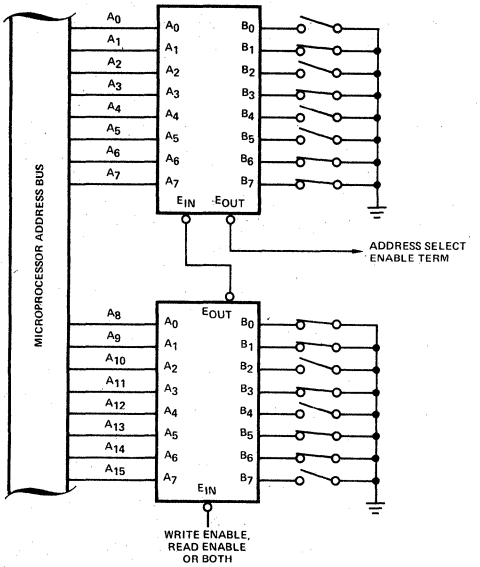
APPLICATION



MAX. $\overline{\text{ENABLE}}$ (HIGH-to-LOW) DELAY OVER 16-BITS
(Commercial Range)

t_{PHL}	A_i or B_i to $\overline{E}_{OUT}$	19ns
t_{PHL}	$\overline{E}_{IN}$ to $\overline{E}_{OUT}$	12.5ns
Total		31.5ns

MICROPROCESSOR ENABLE CONTROLLED, SELECTABLE, ADDRESS DECODER

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0 to +70°C	AM25LS2521PC
Hermetic DIP	0 to +70°C	AM25LS2521DC
Dice	0 to +70°C	AM25LS2521XC
Chip-Pak	0 to +70°C	AM25LS2521LC
Hermetic DIP	−55 to +125°C	AM25LS2521DM
Hermetic Flat-Pak	−55 to +125°C	AM25LS2521FM
Dice	−55 to +125°C	AM25LS2521XM
Chip-Pak	−55 to +125°C	AM25LS2521LM

Am25LS2535

Eight Input Multiplexer with Control Register

DISTINCTIVE CHARACTERISTICS

- High speed eight-input multiplexer
- On-chip Multiplexer Select and Polarity Control Register
- Output polarity control for inverting or non-inverting output
- Common register enable
- Asynchronous register clear
- Three-state output for expansion
- Am25LS features improved noise margin, higher drive, and faster operation

FUNCTIONAL DESCRIPTION

The Am25LS2535 is an eight-input Multiplexer with Control Register. The device features high speed from clock to output and is intended for use in high speed computer control units or structured state machine designs.

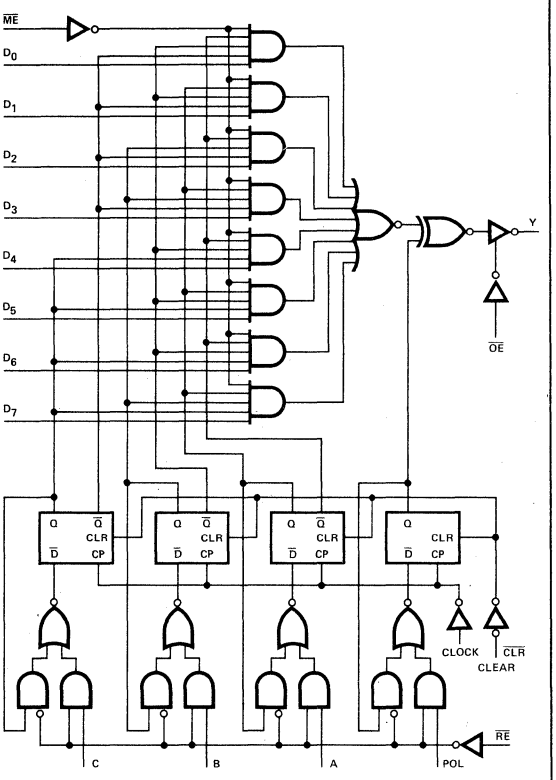
The Am25LS2535 contains an internal register which holds the A, B and C multiplexer select lines as well as the POL (polarity) control bit. When the Register Enable input ($\overline{RE}$) is LOW, new data is entered into the register on the LOW-to-HIGH, transition of the clock. When $\overline{RE}$ is HIGH, the register retains its current data. An asynchronous clear input ($\overline{CLR}$) is used to reset the register to a logic LOW level.

The A, B and C register outputs select one of eight multiplexer data inputs. A HIGH on the Polarity Control flip-flop output causes a true (non-inverting) multiplexer output, and a LOW causes the output to be inverted. In a computer control unit, this allows testing of either true or complemented flag data at the microprogram sequencer test input.

An active LOW Multiplexer Enable input ($\overline{ME}$) allows the selected multiplexer input to be passed to the output. When $\overline{ME}$ is HIGH, the output is determined only by the Polarity Control bit.

The Am25LS2535 also features a three-state Output Enable control ($\overline{OE}$) for expansion. When $\overline{OE}$ is LOW, the output is enabled. When $\overline{OE}$ is HIGH, the output is in the high impedance state.

LOGIC DIAGRAM

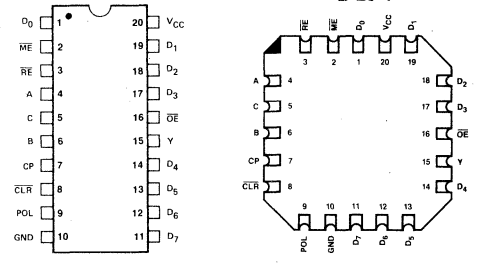


RELATED PRODUCTS

Part No.	Description
Am2922	8 Input Multiplexer
Am2923	8 Input Multiplexer

CONNECTION DIAGRAMS – Top Views

Leadless Chip Carrier
L-20-1



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0 to +70°C	AM25LS2535PC
Hermetic DIP	0 to +70°C	AM25LS2535DC
Chip-Pak	0 to +70°C	AM25LS2535LC
Dice	0 to +70°C	AM25LS2535XC
Hermetic DIP	−55 to +125°C	AM25LS2535DM
Hermetic Flat Pack	−55 to +125°C	AM25LS2535FM
Chip-Pak	−55 to +125°C	AM25LS2535LM
Dice	−55 to +125°C	AM25LS2535XM

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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$	MIN. = 4.75 V	MAX. = 5.25 V
MIL	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$	MIN. = 4.50 V	MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	MIL, $I_{OH} = -2.0mA$	2.4	3.4		Volts
			COM'L, $I_{OH} = -6.5mA$	2.4	3.2		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$			0.4	Volts
			$I_{OL} = 8.0mA$			0.45	
			$I_{OL} = 20mA$			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$	$\overline{ME}$, $\overline{OE}$, $\overline{RE}$			−0.72	mA
			D_N, A, B, C, POL, CP, $\overline{CLR}$			−2.0	
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$	$\overline{ME}$, $\overline{OE}$, $\overline{RE}$			40	μA
			D_N, A, B, C, POL, CP, $\overline{CLR}$			50	
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 5.5V$	$\overline{ME}$, $\overline{OE}$, $\overline{RE}$			0.1	mA
			D_N, A, B, C, POL, CP, $\overline{CLR}$			1.0	
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$			−50	μA
			$V_O = 2.4V$			50	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−40		−100	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			97	148	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $D_1 - D_7$, A, B, C, POL, $\overline{ME}$, CLR at GND. All other inputs and outputs open.
Measured after a momentary ground then 4.5 V applied to clock input.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Y POL – LOW		21	32	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}			19	29		
t_{PLH}	Clock to Y POL – HIGH		16	24	ns	
t_{PHL}			19	29		
t_{PLH}	D_n to Y		10	16	ns	
t_{PHL}			13	19		
t_{PLH}	$\overline{CLR}$ to Y		22	33	ns	
t_{PHL}			22	33		
t_{PLH}	$\overline{ME}$ to Y		12	18	ns	
t_{PHL}			12	18		
t_{ZL}	$\overline{OE}$ to Y		8	14	ns	
t_{ZH}			8	14		
t_{LZ}			10	17	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{HZ}			10	17		
t_s	A, B, C, POL	10			ns	C_L = 15pF, R_L = 2.0kΩ
	$\overline{RE}$	15				
t_s	$\overline{CLR}$ Recovery	5			ns	
t_{pw}	Clock	10			ns	
	$\overline{Clear}$ (LOW)	10				
t_h	A, B, C, POL, $\overline{RE}$	0			ns	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Clock to Y, POL-L		40		47	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}			34		38		
t_{PLH}	Clock to Y, POL-H		29		33	ns	
t_{PHL}			35		41		
t_{PLH}	D_N to Y		19		21	ns	
t_{PHL}			22		24		
t_{PLH}	$\overline{CLR}$ to Y		39		45	ns	
t_{PHL}			39		45		
t_{PLH}	$\overline{ME}$ to Y		22		26	ns	
t_{PHL}			19		20		
t_{ZL}	$\overline{OE}$ to Y		19		24	ns	
t_{ZH}			22		29		
t_{LZ}	OE to Y		24		30	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{HZ}			24		30		
t_s	A, B, C POL	11		12		ns	C_L = 50pF, R_L = 2.0kΩ
	$\overline{RE}$	18		20			
t_s	$\overline{CLR}$ Recovery	6		7		ns	
t_{pw}	Clock	11		12		ns	
	$\overline{Clear}$ (LOW)	11		12			
t_H	A, B, C, POL, $\overline{RE}$	3		3		ns	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

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FUNCTION TABLE

MODE	INPUTS							INTERNAL				INPUTS		OUTPUT
	C	B	A	POL	$\overline{RE}$	$\overline{CLR}$	CP	Q_C	Q_B	Q_A	Q_{POL}	$\overline{ME}$	$\overline{OE}$	Y
Clear	X	X	X	X	X	L	X	L	L	L	L	H	L	H
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	L	L	$\overline{D}_0$
												X	H	Z
Reg. Disable	X	X	X	X	H	H	X	NC	NC	NC	NC	L	L	D_i/D_i (Note 1)
Select (Multiplex)	L	L	L	L/H	L	H	↑	L	L	L	L/H	L	L	$\overline{D}_0/D_0$
	L	L	H	↓	↓	↓	↓	L	L	H	↓	↓	↓	$\overline{D}_1/D_1$
	L	H	L					L	H	L				$\overline{D}_2/D_2$
	L	H	H					L	H	H				$\overline{D}_3/D_3$
	H	L	L					H	L	L				$\overline{D}_4/D_4$
	H	L	H					H	L	H				$\overline{D}_5/D_5$
	H	H	L					H	H	L				$\overline{D}_6/D_6$
	H	H	H	↓	↓	↓	↓	H	H	H	↓	↓	↓	$\overline{D}_7/D_7$
Multiplexer Disable	X	X	X	X	X	H	X	X	X	X	L	H	L	H
	↓	↓	↓	↓	↓	↓	↓	X	X	X	H	H	L	L
Tri-state Output Disable	↓	↓	↓	↓	↓	↓	↓	X	X	X	X	X	H	Z

NC = No Change
X = Don't Care

Note 1: The output will follow the selected input, D_i, or its complement depending on the state of the POL flip-flop.

DEFINITION OF FUNCTIONAL TERMS

A, B, C Multiplexer Select Lines. One of eight multiplexer data inputs is selected by the A, B and C register outputs.

POL Polarity Control Bit. A HIGH register output causes a true (non-inverted) output and a LOW causes the output to be inverted.

$\overline{ME}$ Multiplexer Enable. When LOW, it enabled the 8-input multiplexer. When HIGH, the Y output is determined by only the Polarity Control bit.

$\overline{RE}$ Register Enable. When LOW, the Multiplexer Select and Polarity Control Register is enabled for loading. When HIGH, the register holds its current data.

$\overline{CLR}$ Clear. A LOW asynchronously resets the Multiplexer Select and Polarity Control Register.

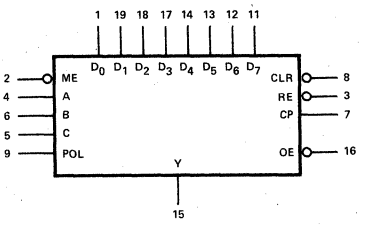
D_1-D_8 Data Inputs to the 8-input multiplexer.

CP Clock Pulse. When $\overline{RE}$ is LOW, the Multiplexer Select and Polarity Control Register changes state on the LOW-to-HIGH transition of CP.

$\overline{OE}$ Output Enable. When LOW, the output is enabled. When HIGH, the output is in the high impedance state.

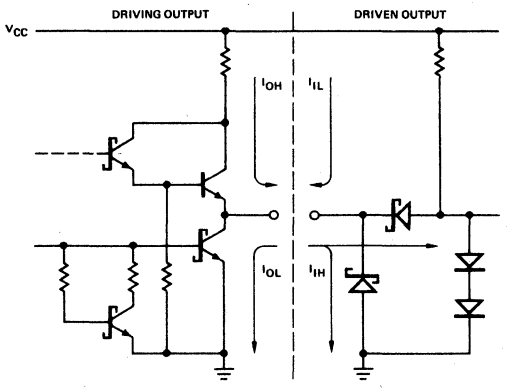
Y The chip output.

LOGIC SYMBOL



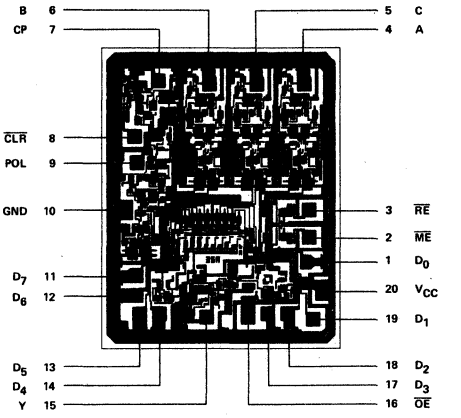
V_{CC} = Pin 20
GND = Pin 10

Am25LS
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



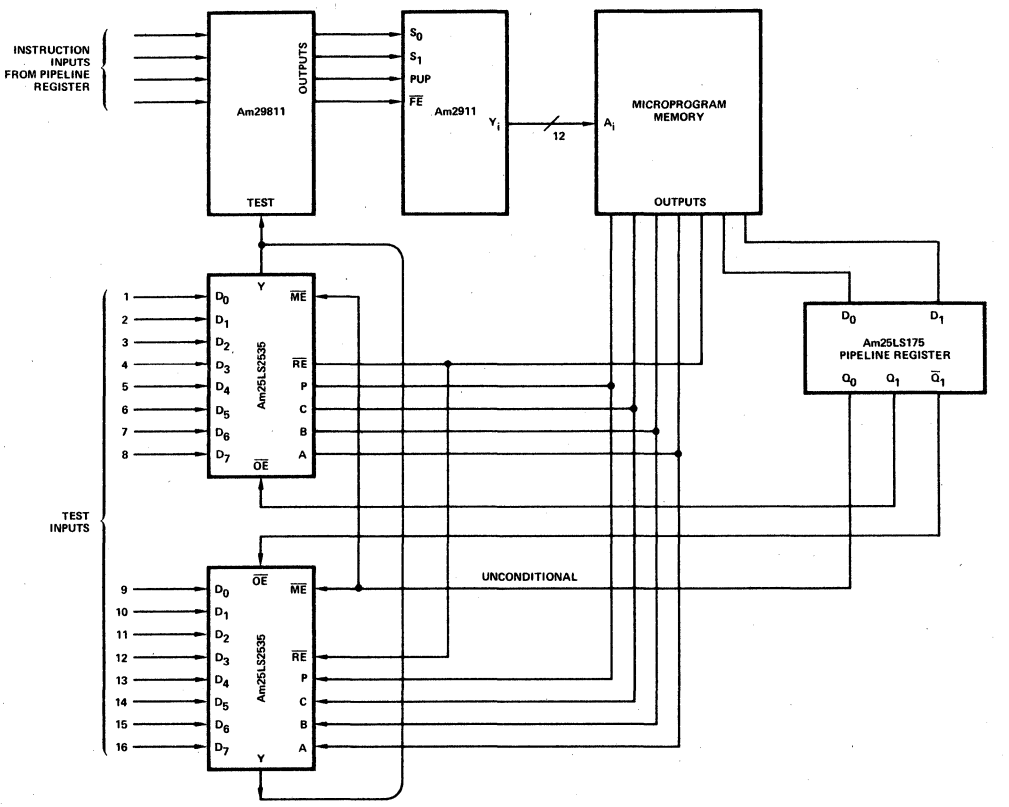
Note: Actual current flow direction shown.

Metallization and Pad Layout



DIE SIZE 0.080" X 0.099"

APPLICATION



A versatile one-of-sixteen Test Select with Polarity Control and Test Select Hold.

Am25LS2536

Eight-Bit Decoder with Control Storage

DISTINCTIVE CHARACTERISTICS

- 8-bit decoder/demultiplexer with control storage
- 3-state outputs
- Common clock enable
- Common clear
- Polarity control
- Advanced Low Power Schottky Process

RELATED PRODUCTS

Part No.	Description
Am25LS2537	1 of 10 Decoder
Am25LS2538	1 of 8 Decoder
Am25LS2539	Dual 1 of 4 Decoder
Am25LS2548	Chip Select Address Decoder
Am2921	1 of 8 Decoder
Am2924	3 to 8 Line Decoder/Demultiplexer

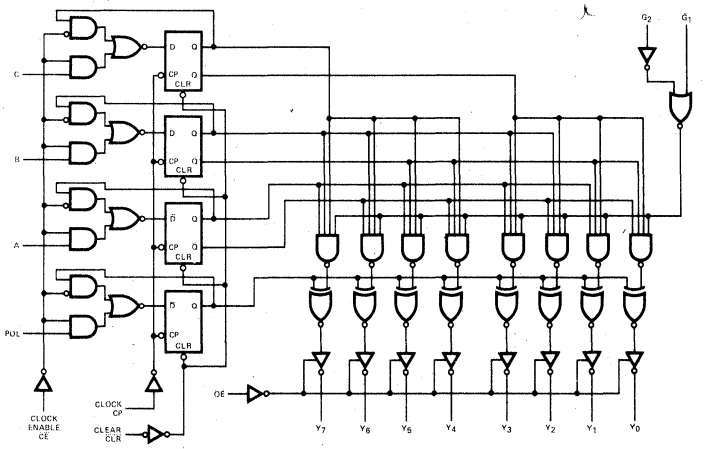
FUNCTIONAL DESCRIPTION

The Am25LS2536 is an eight-bit decoder with control storage. It provides a conventional 8-bit decoder function with two enable inputs which may also be used for data input. This can be used to implement a demultiplexer function. In addition, the exclusive "OR" gate allows for polarity control of the selected output. The 3-state outputs are enabled by a LOW on the ($\overline{OE}$) output enable.

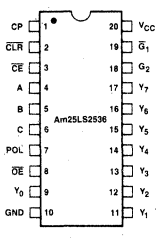
The three control bits representing the output selection and the single bit polarity control are stored in "D" type flip-flops. These flip-flops have both Clear, Clock, and Clock Enable functions provided. The $\overline{G_1}$ and G_2 input provide either polarity for input control or data.

LOGIC DIAGRAM

8-Bit Decoder/Demultiplexer with Control Storage

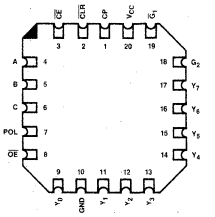


CONNECTION DIAGRAMS – Top Views



Note: Pin 1 is marked for orientation.

Leadless Chip Carrier
L-20-1



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0 to +70°C	AM25LS2536PC
Hermetic DIP	0 to +70°C	AM25LS2536DC
Chip-Pak	0 to +70°C	AM25LS2536LC
Dice	0 to +70°C	AM25LS2536XC
Hermetic DIP	−55 to +125°C	AM25LS2536DM
Hermetic Flat-Pak	−55 to +125°C	AM25LS2536FM
Chip-Pak	−55 to +125°C	AM25LS2536LM
Dice	−55 to +125°C	AM25LS2536XM

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75V MAX. = 5.25V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50V MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -2.6mA$, COM'L		2.4	3.2		Volts
			$I_{OH} = -1.0mA$, MIL		2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 24mA$, COM'L			0.4	0.5	Volts
			$I_{OL} = 12mA$, MIL			0.35	0.4	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$					−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$					20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$					0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$				−20	μA
			$V_O = 2.4V$				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				37	56	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test Conditions: A = B = C = $\overline{G_1}$ = G_2 = $\overline{OE}$ = $\overline{CE}$ = GND; CLK = $\overline{CLR}$ = POL = 4.5V.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

Am25LS2536
SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	G_1 to Y_0 – Y_7			17	25	ns	C_L = 45pF, R_L = 667Ω
t_{PHL}				23	34		
t_{PLH}	G_2 to Y_0 – Y_7			20	30	ns	
t_{PHL}				26	39		
t_{PLH}	CP to Y_0 – Y_7			24	36	ns	
t_{PHL}				30	45		
t_{PLH}	CLR to Y_0 – Y_7			24	36	ns	
t_{PHL}				31	46		
t_s	Clock Enable to CP		25			ns	
t_h			0				
t_s	A, B, C, POL to CP		15			ns	
t_h			0				
t_{HZ}	OE to Y_0 – Y_7			9	14	ns	C_L = 5pF, R_L = 667Ω
t_{LZ}				11	17		
t_{ZH}	OE to Y_0 – Y_7			15	22	ns	C_L = 45pF, R_L = 667Ω
t_{ZL}				16	24		
t_s	Set-up Time, Clear Recovery to CP		20			ns	
t_{pw}	Pulse Width	Clock	15			ns	
		Clear	15				

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	G_1 to Y_0 – Y_7			29		31	ns	C_L = 45pF, R_L = 667Ω
t_{PHL}				39		42		
t_{PLH}	G_2 to Y_0 – Y_7			34		37	ns	
t_{PHL}				44		48		
t_{PLH}	CP to Y_0 – Y_7			40		42	ns	
t_{PHL}				51		55		
t_{PLH}	CLR to Y_0 – Y_7			47		54	ns	
t_{PHL}				58		66		
t_s	Clock Enable to CP		27		30		ns	
t_h			0		0			
t_s	A, B, C, POL to CP		17		20		ns	
t_h			0		0			
t_{HZ}	OE to Y_0 – Y_7			17		18	ns	C_L = 5.0pF, R_L = 667Ω
t_{LZ}				27		34		
t_{ZH}	OE to Y_0 – Y_7			25		27	ns	C_L = 5.0pF, R_L = 667Ω
t_{ZL}				28		30		
t_s	Set-up Time, Clear Recovery to CP		23		25		ns	
t_{pw}	Pulse Width	Clock	17		20		ns	
		Clear	15		15			

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

FUNCTION TABLE

Mode	Inputs									Internal Registers				Three-State Outputs							
	C	B	A	POL	$\overline{CE}$	$\overline{CLR}$	G*	$\overline{OE}$	CP	Q_C	Q_B	Q_A	Q_{POL}	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
Clear	X	X	X	X	X	L	L	L	X	L	L	L	L	H	H	H	H	H	H	H	H
	X	X	X	X	X	L	H	L	X	L	L	L	L	L	H	H	H	H	H	H	H	H
Hold	X	X	X	X	H	H	NC	L	↑	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
Select	L	L	L	H	L	H	H	L	↑	L	L	L	H	H	L	L	L	L	L	L	L
	L	L	H	H	L	H	H	L	↑	L	L	H	H	L	H	L	L	L	L	L	L
	L	H	L	H	L	H	H	L	↑	L	H	L	H	L	L	H	L	L	L	L	L
	L	H	H	H	L	H	H	L	↑	L	H	H	H	L	L	L	H	L	L	L	L
	H	L	L	H	L	H	H	L	↑	H	L	L	H	L	L	L	L	H	L	L	L
	H	L	H	H	L	H	H	L	↑	H	L	H	H	L	L	L	L	L	H	L	L
	H	H	L	H	L	H	H	L	↑	H	H	L	H	L	L	L	L	L	L	H	L
	H	H	H	H	L	H	H	L	↑	H	H	H	H	L	L	L	L	L	L	L	H
	L	L	L	L	L	H	H	L	↑	L	L	L	L	L	H	H	H	H	H	H	H
	L	L	H	L	L	H	H	L	↑	L	L	H	L	H	L	H	H	H	H	H	H
	L	H	L	L	L	H	H	L	↑	L	H	L	L	H	H	L	H	H	H	H	H
	L	H	H	L	L	H	H	L	↑	L	H	H	L	H	H	H	L	H	H	H	H
	H	L	L	L	L	H	H	L	↑	H	L	L	L	H	H	H	H	L	H	H	H
	H	L	H	L	L	H	H	L	↑	H	L	H	L	H	H	H	H	H	L	H	H
	H	H	L	L	L	H	H	L	↑	H	H	L	L	H	H	H	H	H	H	L	H
	H	H	H	L	L	H	H	L	↑	H	H	H	L	H	H	H	H	H	H	H	L
	X	X	X	H	L	H	L	L	↑	X	X	X	H	L	L	L	L	L	L	L	L
	X	X	X	L	L	H	L	L	↑	X	X	X	L	H	H	H	H	H	H	H	H
Output Disable	X	X	X	X	X	X	X	H	X	NC	NC	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z

*

$\overline{G}_1$	G_2	G
L	L	L
L	H	H
H	L	L
H	H	L

NC = No Change X = Don't Care Z = High-Impedance ↑ = Low-to-High Transition

DEFINITION OF TERMS

$\overline{CLR}$ CLEAR – When the CLEAR input is LOW, the control register outputs (Q_A, Q_B, Q_C, Q_{POL}) are set LOW regardless of any other inputs.

CP CLOCK – Enters data into the control register on the LOW-to-HIGH transition.

$\overline{CE}$ CLOCK ENABLE – Allows data to enter the control register when $\overline{CE}$ is LOW. When $\overline{CE}$ is HIGH, the Q_i outputs do not change state, regardless of data or clock input transitions.

A, B, C Inputs to the control register which are entered on the LOW-to-HIGH clock transition if $\overline{CE}$ is LOW.

POL Input to the control register bit used for determining the polarity of the selected output.

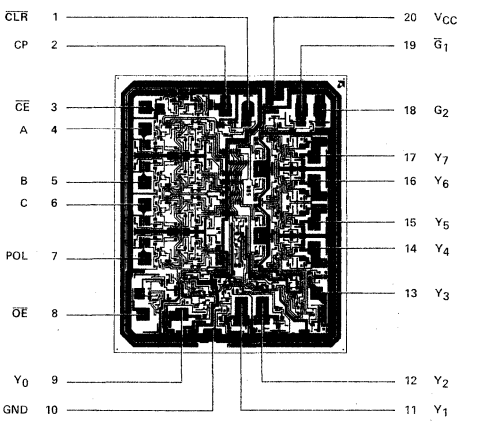
$\overline{G}_1$ Active LOW part of the expression $G = G_1G_2$ [or $G = (\overline{G}_1)\,G_2$] where G is either data input for the selected Y_n or is used as an input enable.

G_2 Active HIGH part of the expression $G = G_1G_2$.

Y_n The three-state outputs. When active ($\overline{OE}$ = LOW), one of eight outputs is selected by the code stored in the control register, with the polarity of all eight determined by the bit stored in the POL flip-flop of the control register. The selected output can further be controlled by G according to the expression $Y_{SELECTED} = \overline{G \oplus Q_{POL}}$.

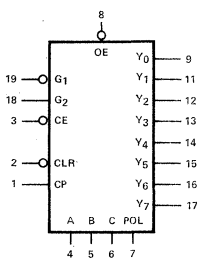
$\overline{OE}$ OUTPUT ENABLE. When $\overline{OE}$ is HIGH the Y_n outputs are in the high impedance state; when $\overline{OE}$ is LOW the Y_n's are in their active state as determined by the other control logic. The $\overline{OE}$ input affects the Y_n output buffers only and has no effect on the control register or any other logic.

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.084" X 0.099"

LOGIC SYMBOL



VCC = 20
GND = 10

9

Am25LS2537

One-of-Ten Decoder with Three-State Outputs and Polarity Control

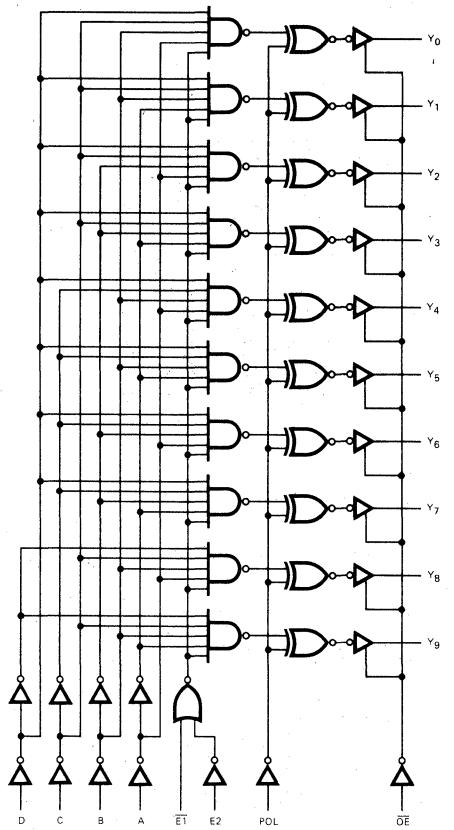
DISTINCTIVE CHARACTERISTICS

- Three-state outputs
- Separate output polarity control
- Inverting and non-inverting enable inputs
- Does not respond to codes above nine
- A.C. parameters specified over operating temperature and power supply ranges

RELATED PRODUCTS

Part No.	Description
Am25LS2536	8-Bit Decoder
Am25LS2538	1 of 8 Decoder
Am25LS2539	Dual 1 of 4 Decoder
Am25LS2548	Chip Select Address Decoder
Am2921	1 of 8 Decoder
Am2924	3 to 8 Line Decoder/Demultiplexer

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The Am25LS2537 is a demultiplexer/one-of-ten decoder that accepts four active high BCD inputs and selects one-of-ten mutually exclusive outputs. The device features three-state outputs as well as a buffered common polarity control such that the outputs are mutually exclusive active-low or mutually exclusive active-high. The logic design of the Am25LS2537 ensures that all outputs are unselected when the binary codes greater than nine are applied to the inputs. The inputs A, B, C, and D of the Am25LS2537 correspond to the respective binary weight of 1, 2, 4, and 8.

The output enable ($\overline{OE}$) input controls the three-state outputs. When the $\overline{OE}$ input is HIGH, the outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the outputs are enabled. The polarity (POL) input is used to drive the Y outputs to either the active-HIGH state or the active-LOW state. When the POL input is LOW, the outputs are active-HIGH. When the POL input is HIGH, the Y outputs are active-LOW. The device features one active-HIGH and one active-LOW enable input which can be used for gating the decoder or can be used with incoming data for demultiplexing applications.

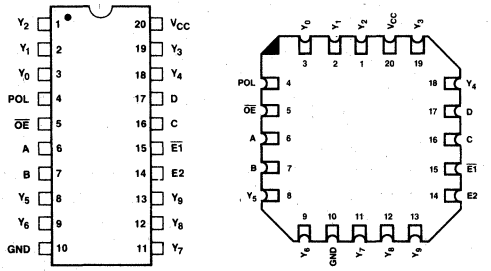
The Am25LS2537 is packaged in a space saving (0.3-inch row spacing) 20-pin package. The device also features Am25LS family faster switching specifications, higher noise margin, and twice the fan-out over the military temperature range when compared with Am54LS/74LS devices.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0 to +70°C	AM25LS2537PC
Hermetic DIP	0 to +70°C	AM25LS2537DC
Chip-Pak	0 to +70°C	AM25LS2537LC
Dice	0 to +70°C	AM25LS2537XC
Hermetic DIP	−55 to +125°C	AM25LS2537DM
Hermetic Flat-Pak	−55 to +125°C	AM25LS2537FM
Chip-Pak	−55 to +125°C	AM25LS2537LM
Dice	−55 to +125°C	AM25LS2537XM

CONNECTION DIAGRAMS – Top Views

Leadless Chip Carrier
L-20-1



Note: Pin 1 is marked for orientation.

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L = T_A = 0°C to +70°C V_{CC} = 5.0 V ±5% MIN. = 4.75 V MAX. = 5.25 V
MIL = T_A = −55°C to +125°C V_{CC} = 5.0 V ±10% MIN. = 4.50 V MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −1.0mA		2.4	3.4		Volts
			COM'L, I_{OH} = −2.6mA		2.4	3.4		
V_{OL}	Output LOW Voltage (Note 5)	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
			I_{OL} = 12mA				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V					−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7 V					20	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0 V					0.1	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	V_O = 0.4 V				−20	µA
			V_O = 2.4 V				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				25	40	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: A = B = C = D = E1 = GND; E2 = POL = $\overline{OE}$ = 4.5 V.
5. V_{OL} is specified with total device I_{OL} = 60mA (max.).

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

Am25LS2537
SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	A, B, C, D to Y_i		22	33	ns	C_L = 15pF R_L = 2.0kΩ
t_{PHL}			17	25		
t_{PLH}	E_1 to Y_i		19	28	ns	
t_{PHL}			21	31		
t_{PLH}	$\overline{E_2}$ to Y_i		21	31	ns	
t_{PHL}			23	34		
t_{PLH}	POL to Y_i		18	27	ns	
t_{PHL}			21	31		
t_{ZH}	$\overline{OE}$ Control to Y_i		22	33	ns	
t_{ZL}			14	21		
t_{HZ}	$\overline{OE}$ Control to Y_i		19	28	ns	C_L = 5.0pF R_L = 2.0kΩ
t_{LZ}			23	34		

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ± 5%		Am25LS MIL T_A = −55°C to +125°C V_{CC} = 5.0V ± 10%		Units	Test Conditions
		Min.	Max.	Min.	Max.		
t_{PLH}	A, B, C, D to Y_i		41		48	ns	C_L = 50pF R_L = 2.0kΩ
t_{PHL}			32		39		
t_{PLH}	E_1 to Y_i		34		40	ns	
t_{PHL}			38		45		
t_{PLH}	$\overline{E_2}$ to Y_i		38		45	ns	
t_{PHL}			42		49		
t_{PLH}	POL to Y_i		32		37	ns	
t_{PHL}			42		52		
t_{ZH}	$\overline{OE}$ Control to Y_i		44		55	ns	
t_{ZL}			23		25		
t_{HZ}	$\overline{OE}$ Control to Y_i		33		37	ns	C_L = 5.0pF R_L = 2.0kΩ
t_{LZ}			38		42		

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

FUNCTION TABLE

FUNCTION	INPUTS								OUTPUTS									
	$\overline{OE}$	$\overline{E_1}$	E_2	POL	D	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9
3-State	H	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
Disable	L	H	X	L	X	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	X	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H
	L	X	L	L	X	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	X	L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H
Active-HIGH Output	L	L	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L
	L	L	H	L	L	L	L	H	L	H	L	L	L	L	L	L	L	L
	L	L	H	L	L	L	H	L	L	L	H	L	L	L	L	L	L	L
	L	L	H	L	L	L	H	H	L	L	L	H	L	L	L	L	L	L
	L	L	H	L	L	H	L	L	L	L	L	L	H	L	L	L	L	L
	L	L	H	L	L	H	L	H	L	L	L	L	L	H	L	L	L	L
	L	L	H	L	L	H	H	L	L	L	L	L	L	L	H	L	L	L
	L	L	H	L	L	H	H	H	L	L	L	L	L	L	L	H	L	L
	L	L	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L
	L	L	H	L	H	L	L	H	L	L	L	L	L	L	L	L	L	H
	L	L	H	L	H	L	H	L	L	L	L	L	L	L	L	L	L	L
	L	L	H	L	H	L	H	H	L	L	L	L	L	L	L	L	L	L
	L	L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L
	L	L	H	L	H	H	L	H	L	L	L	L	L	L	L	L	L	L
	L	L	H	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L
	L	L	H	L	H	H	H	H	L	L	L	L	L	L	L	L	L	L
Active-LOW Output	L	L	H	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H
	L	L	H	H	L	L	L	H	H	L	H	H	H	H	H	H	H	H
	L	L	H	H	L	L	H	L	H	H	L	H	H	H	H	H	H	H
	L	L	H	H	L	L	H	H	H	H	H	L	H	H	H	H	H	H
	L	L	H	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H
	L	L	H	H	L	H	L	H	H	H	H	H	H	L	H	H	H	H
	L	L	H	H	L	H	H	L	H	H	H	H	H	H	L	H	H	H
	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H
	L	L	H	H	H	L	L	L	H	H	H	H	H	H	H	H	L	H
	L	L	H	H	H	L	L	H	H	H	H	H	H	H	H	H	H	L
	L	L	H	H	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	L	L	H	H	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH
L = LOW

X = Don't Care
Z = High Impedance

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DEFINITION OF FUNCTIONAL TERMS

A, B, C, D To select inputs to the decoder.

E1 The active-LOW enable input. A HIGH on the E1 input inhibits the decoder function regardless of any other inputs.

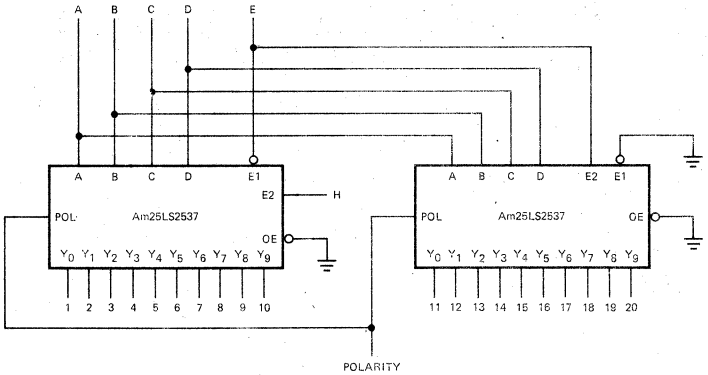
$\overline{E2}$ The active-HIGH enable input. A LOW on the $\overline{E2}$ input forces all the decoder functions to the inactive state regardless of any other inputs.

POL The polarity control for the output function. When the polarity control is HIGH, the outputs are active-LOW. When the POL input is LOW, the outputs are active-HIGH.

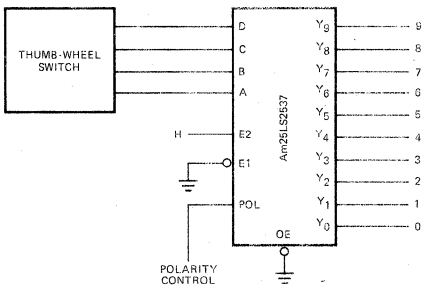
$\overline{OE}$ Output Enable. An active-LOW three-state control used to enable the outputs. A HIGH level input forces the output to the high impedance (off) state.

Y_i Decoder outputs. The ten outputs of the decoder.

APPLICATIONS



One-of-Twenty Decoder with Active-High or Active-Low Output Polarity.
Could be used for I/O Decoding in an Am9080A system.



BCD to Decimal (One-of-Ten) Decoder.

Am25LS2538

One-of-Eight Decoder with Three-State Outputs and Polarity Control

DISTINCTIVE CHARACTERISTICS

- Three-state decoder outputs
- Buffered common output polarity control
- Inverting and non-inverting enable inputs
- A. C. parameters specified over operating temperature and power supply ranges

RELATED PRODUCTS

Part No.	Description
Am25LS2536	8-Bit Decoder
Am25LS2537	1 of 10 Decoder
Am25LS2539	Dual 1 of 4 Decoder
Am25LS2548	Chip Select Address Decoder
Am2921	1 of 8 Decoder
Am2924	3 to 8 Line Decoder/Demultiplexer

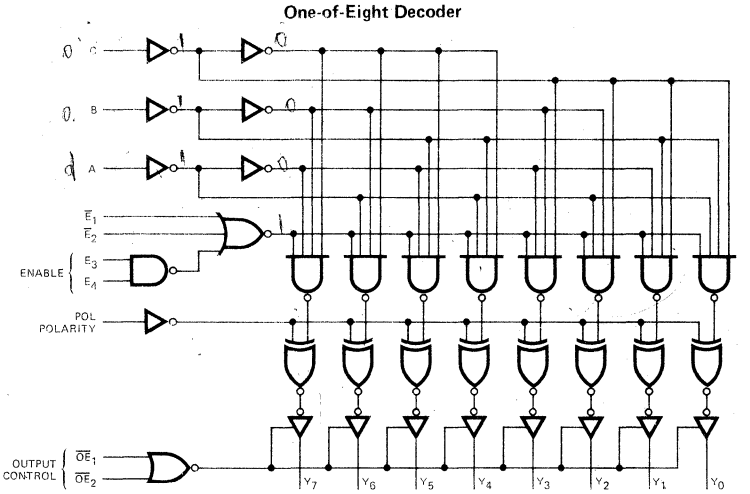
FUNCTIONAL DESCRIPTION

The Am25LS2538 is a three-line to eight-line decoder/demultiplexer fabricated using advanced Low-Power Schottky technology. The decoder has three buffered select inputs—A, B, and C—that are decoded to one-of-eight Y outputs. Two active-HIGH and two active-LOW enables can be used for gating the decoder or can be used with incoming data for demultiplexing applications.

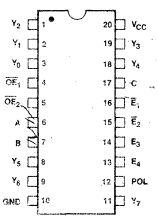
A separate polarity (POL) input can be used to force the function active-HIGH or active-LOW at the output. Two separate active-LOW output enables ($\overline{OE}$) inputs are provided. If either $\overline{OE}$ input is HIGH, the output is in the high impedance (off) state. When the POL input is LOW, the Y outputs are active-HIGH and when the POL input is HIGH, the Y outputs are active-LOW.

The device is packaged in a space saving (0.3-inch row spacing) 20-pin package. It also features Am25LS family improved switching specifications, higher noise margin, and twice the fan-out over the military temperature range when compared with Am54LS/74LS devices.

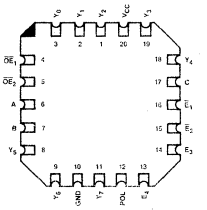
LOGIC DIAGRAM
One-of-Eight Decoder



CONNECTION DIAGRAMS – Top Views



Leadless Chip Carrier
L-20-1



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0 to +70°C	AM25LS2538PC
Hermetic DIP	0 to +70°C	AM25LS2538DC
Chip-Pak	0 to +70°C	AM25LS2538LC
Dice	0 to +70°C	AM25LS2538XC
Hermetic DIP	−55 to +125°C	AM25LS2538DM
Hermetic Flat Pack	−55 to +125°C	AM25LS2538FM
Chip-Pak	−55 to +125°C	AM25LS2538LM
Dice	−55 to +125°C	AM25LS2538XM

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Am25LS2538

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$	MIN. = 4.75 V	MAX. = 5.25 V
MIL	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$	MIN. = 4.50 V	MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -1.0mA$ (MIL)		2.4	3.4		Volts
			$I_{OH} = -2.6mA$ (COM'L)		2.4	3.4		
V_{OL}	Output LOW Voltage (Note 5)	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$				0.4	Volts
			$I_{OL} = 8.0mA$				0.45	
			$I_{OL} = 12mA$				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$					−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$					20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$					0.1	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$				−20	μA
			$V_O = 2.4V$				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				21	34	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: A = B = C = $\overline{E}_1 = \overline{E}_2$ = GND : $E_3 = E_4$ = POL = $\overline{OE}_1 = \overline{OE}_2 = 4.5V$.
5. V_{OL} is specified with total device $I_{OL} = 60mA$ (max.).

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	A, B, C to Y_i		20	30	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}			15	22		
t_{PLH}	$\overline{E_1}$, $\overline{E_2}$ to Y_i		19	28	ns	
t_{PHL}			20	30		
t_{PLH}	E_3, E_4 to Y_i		21	31	ns	
t_{PHL}			23	34		
t_{PLH}	POL to Y_i		16	24	ns	
t_{PHL}			20	30		
t_{ZH}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i		17	25	ns	
t_{ZL}			14	21		
t_{HZ}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i		17	25	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			20	30		

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

		Am25LS COM'L		Am25LS MIL			
		T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%		T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%			
Parameters	Description	Min.	Max.	Min.	Max.	Units	Test Conditions
t_{PLH}	A, B, C to Y_i		36		42	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}			29		37		
t_{PLH}	$\overline{E_1}$, $\overline{E_2}$ to Y_i		34		39	ns	
t_{PHL}			38		45		
t_{PLH}	E_3, E_4 to Y_i		38		45	ns	
t_{PHL}			43		52		
t_{PLH}	POL to Y_i		29		34	ns	
t_{PHL}			39		49		
t_{ZH}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i		38		45	ns	
t_{ZL}			23		25		
t_{HZ}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i		29		33	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			33		36		

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

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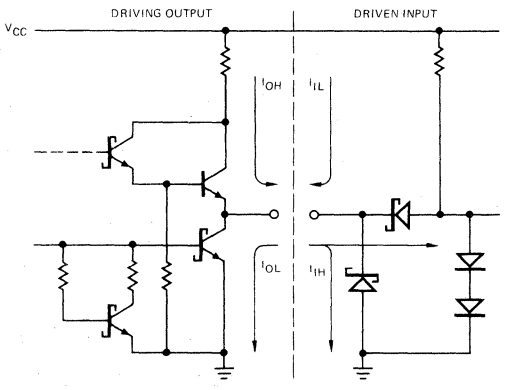
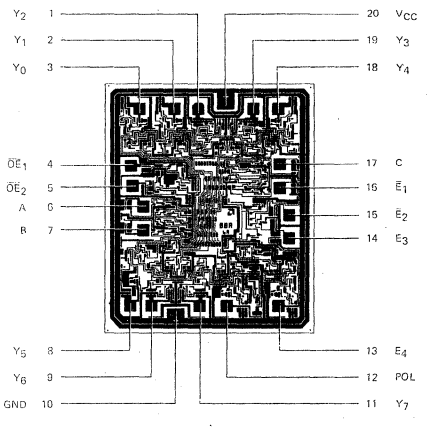
Am25LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

Metallization and Pad Layout



DIE SIZE 0.081" X 0.096"

DEFINITION OF FUNCTIONAL TERMS

A, B, C, D The three select inputs to the decoder/demultiplexer.

$\overline{E}_1$, $\overline{E}_2$ The active LOW enable inputs. A HIGH on either the $\overline{E}_1$ or $\overline{E}_2$ input forces all decoded functions to be disabled.

E_3, E_4 The active HIGH enable inputs. A LOW on either E_3 or E_4 inputs forces all the decoded functions to be inhibited.

POL Polarity Control. A LOW on the polarity control input forces the output to the active-HIGH state while a HIGH on the polarity control input forces the Y outputs to the active-LOW state.

$\overline{OE}_1$, $\overline{OE}_2$ Output Enable. When both the $\overline{OE}_1$ and $\overline{OE}_2$ inputs are LOW, the Y outputs are enabled. If either $\overline{OE}_1$ or $\overline{OE}_2$ input is HIGH, the Y outputs are in the high impedance state.

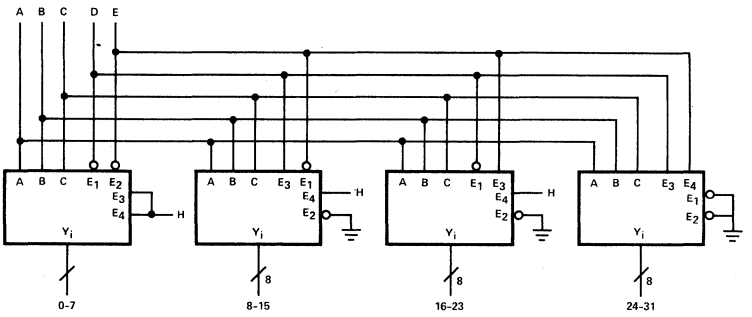
Y_i The eight outputs for the decoder/demultiplexer.

FUNCTION TABLE

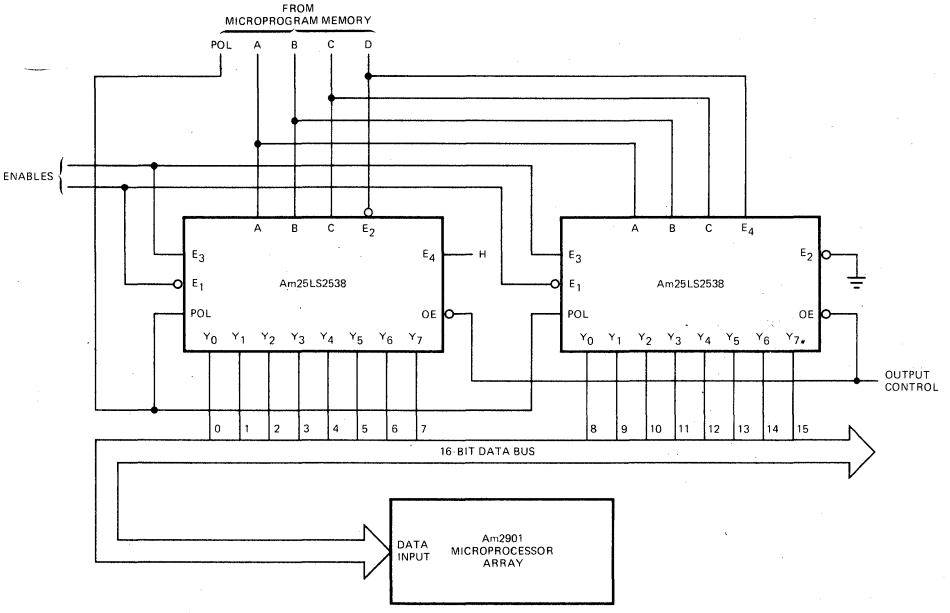
FUNCTION	INPUTS										OUTPUTS							
	$\overline{OE}_1$	$\overline{OE}_2$	$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	POL	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
High Impedance	H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
	X	H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
Disable	L	L	H	X	X	X	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	H	X	X	X	H	X	X	X	H	H	H	H	H	H	H	H
	L	L	X	H	X	X	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	X	H	X	X	H	X	X	X	H	H	H	H	H	H	H	H
	L	L	X	X	L	X	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	X	X	L	X	H	X	X	X	H	H	H	H	H	H	H	H
	L	L	X	X	X	L	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	X	X	X	L	H	X	X	X	H	H	H	H	H	H	H	H
Active-HIGH Output	L	L	L	L	H	H	L	L	L	L	H	L	L	L	L	L	L	L
	L	L	L	L	H	H	L	L	L	H	L	H	L	L	L	L	L	L
	L	L	L	L	H	H	L	L	H	L	L	L	H	L	L	L	L	L
	L	L	L	L	H	H	L	L	H	H	L	L	L	H	L	L	L	L
	L	L	L	L	H	H	L	H	L	L	L	L	L	L	H	L	L	L
	L	L	L	L	H	H	L	H	L	H	L	L	L	L	L	H	L	L
	L	L	L	L	H	H	L	H	H	L	L	L	L	L	L	L	H	L
	L	L	L	L	H	H	L	H	H	H	L	L	L	L	L	L	L	H
Active-LOW Output	L	L	L	L	H	H	H	L	L	L	L	H	H	H	H	H	H	H
	L	L	L	L	H	H	H	L	L	H	H	L	H	H	H	H	H	H
	L	L	L	L	H	H	H	L	H	L	H	H	L	H	H	H	H	H
	L	L	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	L	L	L	L	H	H	H	H	L	L	H	H	H	H	L	H	H	H
	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	L	H	H
	L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	L	H
	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH L = LOW X = Don't Care Z = High Impedance

APPLICATIONS



One-of-thirty two decoder without additional decoding devices.
Can be used for I/O decoding in an Am9080A system.



Two Am25LS2538s can be used to perform a one-of-sixteen-bit mask function or a one-of-sixteen-bit select function to perform bit manipulation in a microprocessor system.

Examples:

D	C	B	A	POL	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Function
0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	Bit Select
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	Bit Select
0	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	Bit Mask
1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	Bit Mask

Am25LS2539

Dual One-of-Four Decoder with Three-State Outputs and Polarity Control

DISTINCTIVE CHARACTERISTICS

- Two independent decoders/demultiplexers
- Three-state outputs
- Buffered common polarity control
- A. C. parameters specified over operating temperature and power supply ranges

RELATED PRODUCTS

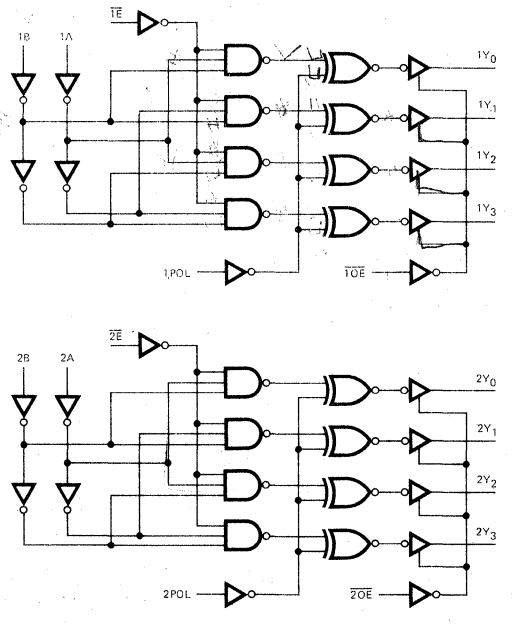
Part No.	Description
Am25LS2536	8-Bit Decoder
Am25LS2537	1 of 10 Decoder
Am25LS2538	1 of 8 Decoder
Am25LS2548	Chip Select Address Decoder
Am2921	1 of 8 Decoder
Am2924	3 to 8 Line Decoder/Demultiplexer

FUNCTIONAL DESCRIPTION

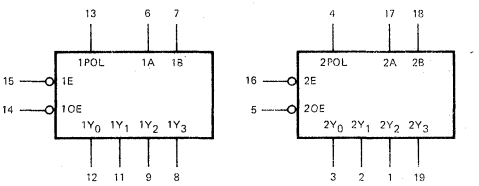
The Am25LS2539 is a dual two-line to four-line decoder/demultiplexer fabricated using advanced Low-Power Schottky technology. Each decoder has two buffered select inputs—A and B which are decoded to one-of-four Y outputs. An enable input ($\overline{E}$) is used for gating or can be used as a data input for demultiplexing applications. When the enable input goes HIGH, all four decoder functions are inhibited.

An output enable ($\overline{OE}$) input is used to control the three-state outputs of the device. When the $\overline{OE}$ input is LOW, the outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the high impedance (off) state. The device also has separate buffered polarity (POL) inputs to force the outputs to either an active-HIGH state or an active-LOW state. When the POL input is LOW, the outputs are active-HIGH and when the POL input is HIGH, the outputs are active-LOW. The device is packaged in a space saving (0.3 inch row spacing) 20-pin package. The device features Am25LS family improved switching specification, higher noise margin, and twice the fan-out over the military temperature range when compared with Am54LS/74LS devices.

LOGIC DIAGRAM



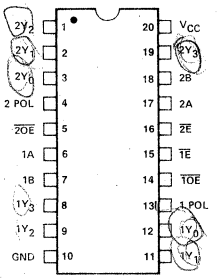
LOGIC SYMBOLS



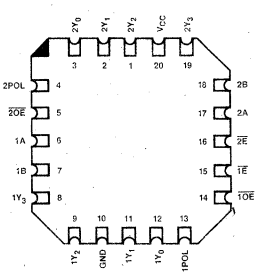
V_{CC} = Pin 20
GND = Pin 10

CONNECTION DIAGRAMS – Top Views

DIP



Leadless Chip Carrier
L-20-1



Note: Pin 1 is marked for orientation.

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$	MIN. = 4.75 V	MAX. = 5.25 V
MIL	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$	MIN. = 4.50 V	MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	MIL, $I_{OH} = -1.0mA$	2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6mA$	2.4	3.4		
V_{OL}	Output LOW Voltage (Note 5)	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$			0.4	Volts
			$I_{OL} = 8.0mA$			0.45	
			$I_{OL} = 12mA$			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$				0.1	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$			−20	μA
			$V_O = 2.4V$			20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			22	37	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: A = B = $\overline{E}$ = GND; POL = $\overline{OE}$ = 4.5V.
5. V_{OL} is specified with total device I_{OL} = 60mA (max.).

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

Am25LS2539

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

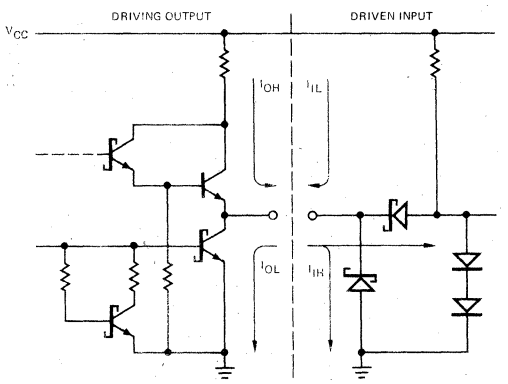
Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	A, B to Y_i		22	33	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}			17	25		
t_{PLH}	$\overline{E}$ to Y_i		19	28	ns	
t_{PHL}			21	31		
t_{PLH}	POL to Y_i		16	24	ns	
t_{PHL}			19	28		
t_{ZH}	$\overline{OE}$ to Y_i		15	23	ns	
t_{ZL}			15	22		
t_{HZ}	$\overline{OE}$ to Y_i		19	28	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			23	34		

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%		Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%		Units	Test Conditions
		Min.	Max.	Min.	Max.		
t_{PLH}	A, B, to Y_i		41		48	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}			34		42		
t_{PLH}	$\overline{E}$ to Y_i		34		40	ns	
t_{PHL}			38		45		
t_{PLH}	POL to Y_i		29		34	ns	
t_{PHL}			39		49		
t_{ZH}	$\overline{OE}$ to Y_i		38		45	ns	
t_{ZL}			24		25		
t_{HZ}	$\overline{OE}$ to Y_i		33		37	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			36		37		

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Am25LS • Am54LS/74LS LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

DEFINITION OF FUNCTIONAL TERMS

A, B — Select the two select inputs to the decoder/demultiplexer.

$\overline{E}$ Enable — The enable input to the decoder. A HIGH input forces the decoding functions to be inhibited regardless of the A and B inputs.

POL — Polarity Input. The polarity input forces the outputs either an active-HIGH state or an active-LOW state. A LOW on the polarity input forces the output active-HIGH. A HIGH on the polarity input forces the outputs active-LOW.

$\overline{OE}$ — Output Enable. A LOW on the $\overline{OE}$ input enables the outputs. A HIGH on the $\overline{OE}$ inputs forces the outputs to the high impedance (off) state.

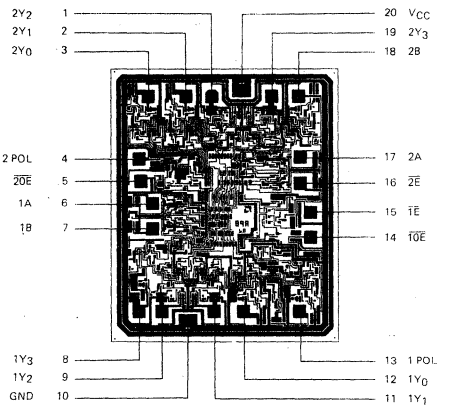
Y_0, Y_1, Y_2, Y_3 — The four decoder/demultiplexer outputs.

FUNCTION TABLE

Function	Inputs					Outputs			
	$\overline{OE}$	$\overline{E}$	POL	B	A	Y_0	Y_1	Y_2	Y_3
High Impedance	H	X	X	X	X	Z	Z	Z	Z
Disable	L	H	L	X	X	L	L	L	L
	L	H	H	X	X	H	H	H	H
Active-High Output	L	L	L	L	L	H	L	L	L
	L	L	L	L	H	L	H	L	L
	L	L	L	H	L	L	L	H	L
	L	L	L	H	H	L	L	L	H
Active-Low Output	L	L	H	L	L	L	H	H	H
	L	L	H	L	H	H	L	H	H
	L	L	H	H	L	H	H	L	H
	L	L	H	H	H	H	H	H	L

H = HIGH X = Don't Care
L = LOW Z = High Impedance

Metallization and Pad Layout

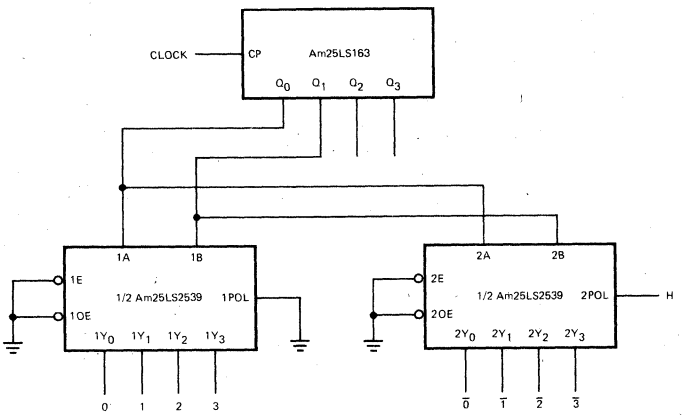


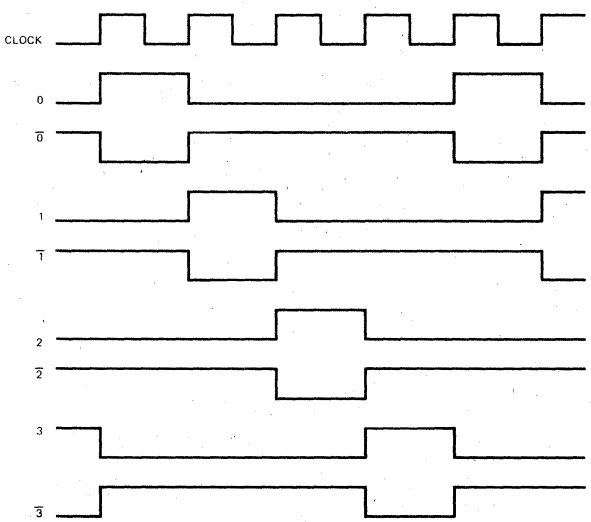
DIE SIZE 0.081" X 0.096"

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0 to +70°C	AM25LS2539PC
Hermetic DIP	0 to +70°C	AM25LS2539DC
Chip-Pak	0 to +70°C	AM25LS2539LC
Dice	0 to +70°C	AM25LS2539XC
Hermetic DIP	−55 to +125°C	AM25LS2539DM
Hermetic Flat-Pak	−55 to +125°C	AM25LS2539FM
Chip-Pak	−55 to +125°C	AM25LS2539LM
Dice	−55 to +125°C	AM25LS2539XM

APPLICATIONS





FOUR PHASE CLOCK GENERATOR

Am25LS2548

Chip Select Address Decoder with Acknowledge

DISTINCTIVE CHARACTERISTICS

- One-of-Eight Decoder provides eight chip select outputs
- Acknowledge output responds to enables and read or write command
- Open-collector Acknowledge output for wired-OR application
- Inverting and non-inverting enable inputs for upper address decoding

RELATED PRODUCTS

Part No.	Description
Am25LS2536	8-Bit Decoder
Am25LS2537	1 of 10 Decoder
Am25LS2538	1 of 8 Decoder
Am25LS2539	Dual 1 of 4 Decoder
Am2921	1 of 8 Decoder
Am2924	3 to 8 Line Decoder/Demultiplexer

FUNCTIONAL DESCRIPTION

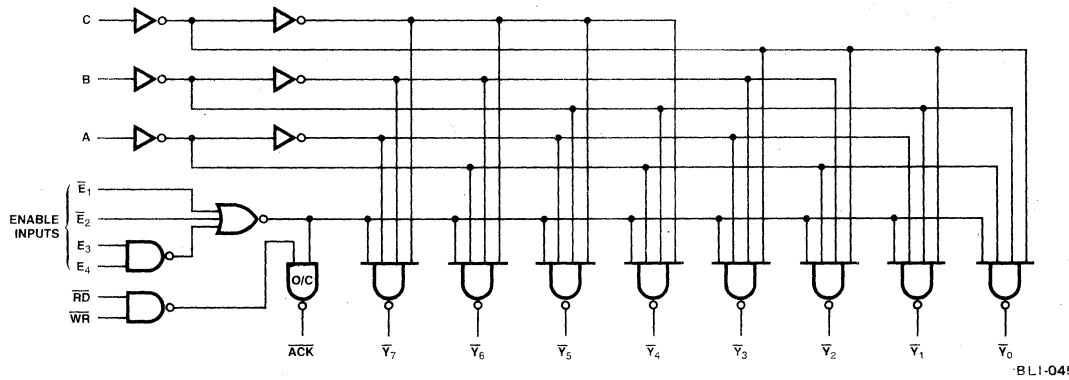
The Am25LS2548 Address Decoder combines a three-line to eight-line decoder with four qualifying enable inputs (two active HIGH and two active LOW) and the acknowledge output required for "ready" or "wait state" control of all popular MOS microprocessors.

The acknowledge output, $\overline{ACK}$, is active LOW and responds to the combination of all enables active and a read ($\overline{RD}$) or write ($\overline{WR}$) input command.

The eight chip select outputs are individually active LOW in response to the combination of all enables active and the corresponding 3-bit input code at inputs A, B, and C.

The Am25LS2548 is intended for chip select decoding in small, medium or large systems where multiple chip selects must be generated and address space must be allocated conservatively.

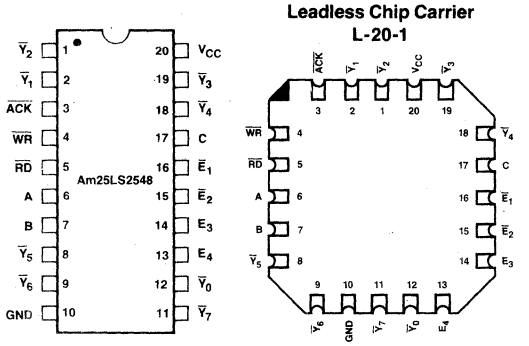
LOGIC DIAGRAM



BLI-045

CONNECTION DIAGRAMS – Top Views

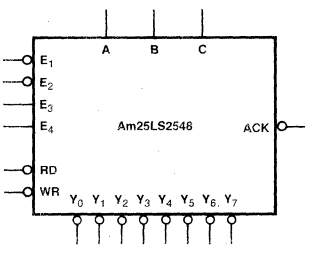
Leadless Chip Carrier
L-20-1



Note: Pin 1 is marked for orientation.

BLI-046

LOGIC SYMBOL



BLI-047

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (MIN. = 4.75V MAX. = 5.25V)

MIL T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −440μA	2.4	3.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V				0.1	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			15	20	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. TEST CONDITIONS: A = B = C = $\overline{E}_1$ = $\overline{E}_2$ = GND: RD = WR = E_3 = E_4 = 4.5V.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	A, B or C to $\overline{Y}_i$ (Three Level Delay)		14	20	ns	C_L = 15pF R_L = 2.0kΩ
t_{PHL}			19	27	ns	
t_{PLH}	A, B, or C to $\overline{Y}_i$ (Two Level Delay)		13	18	ns	
t_{PHL}			15	21	ns	
t_{PLH}	$\overline{E}_1$, $\overline{E}_2$ to $\overline{Y}_i$		13	18	ns	
t_{PHL}			16	23	ns	
t_{PLH}	E_3, E_4 to $\overline{Y}_i$		15	21	ns	
t_{PHL}			19	27	ns	
t_{PLH}	$\overline{WR}$, $\overline{RD}$ to $\overline{ACK}$		25	35	ns	
t_{PHL}			16	22	ns	
t_{PLH}	$\overline{E}_1$, $\overline{E}_2$ to $\overline{ACK}$		29	40	ns	
t_{PHL}			25	35	ns	
t_{PLH}	E_3, E_4 to $\overline{ACK}$		29	40	ns	
t_{PHL}			25	35	ns	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

		Am25LS COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5%		Am25LS MIL T_A = −55°C to +125°C V_{CC} = 5.0V ±10%			
Parameters	Description	Min.	Max.	Min.	Max.	Units	Test Conditions
t_{PLH}	A, B or C to Y_i (Three Level Delay)		27		30	ns	C_L = 50pF R_L = 2.0kΩ
t_{PHL}			34		36	ns	
t_{PLH}	A, B or C to Y_i (Two Level Delay)		23		25	ns	
t_{PHL}			28		31	ns	
t_{PLH}	$\overline{E}_1$, $\overline{E}_2$ to $\overline{Y}_i$		23		25	ns	
t_{PHL}			29		31	ns	
t_{PLH}	E_3, E_4 to $\overline{Y}_i$		27		28	ns	
t_{PHL}			34		36	ns	
t_{PLH}	$\overline{WR}$, $\overline{RD}$ to $\overline{ACK}$		45		45	ns	
t_{PHL}			31		35	ns	
t_{PLH}	$\overline{E}_1$, $\overline{E}_2$ to $\overline{ACK}$		45		45	ns	
t_{PHL}			39		40	ns	
t_{PLH}	E_3, E_4 to $\overline{ACK}$		45		45	ns	
t_{PHL}			39		40	ns	

9

DEFINITION OF FUNCTIONAL TERMS

A, B, C Three-line to eight-line chip select decoder inputs.

$\overline{E}_1$, $\overline{E}_2$ The active LOW enable inputs. A HIGH on either the $\overline{E}_1$ or $\overline{E}_2$ input forces all decoded functions to be disabled, and forces $\overline{ACK}$ HIGH.

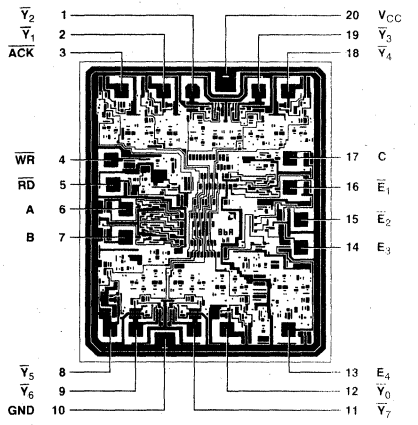
E_3, E_4 The active HIGH enable inputs. A LOW on either E_3 or E_4 inputs forces all the decoded functions to be inhibited, and forces $\overline{ACK}$ HIGH.

$\overline{WR}$, $\overline{RD}$ The write input, $\overline{WR}$, and read input, $\overline{RD}$, are active LOW inputs used as conditions for an active LOW output at the acknowledge, $\overline{ACK}$, output.

$\overline{ACK}$ The acknowledge output, $\overline{ACK}$, is an active LOW output used to signal the microprocessor that specific devices have been selected. $\overline{ACK}$ goes LOW only when $\overline{E}_1$ and $\overline{E}_2$ are LOW, E_3 and E_4 are HIGH and $\overline{WR}$ or $\overline{RD}$ is LOW.

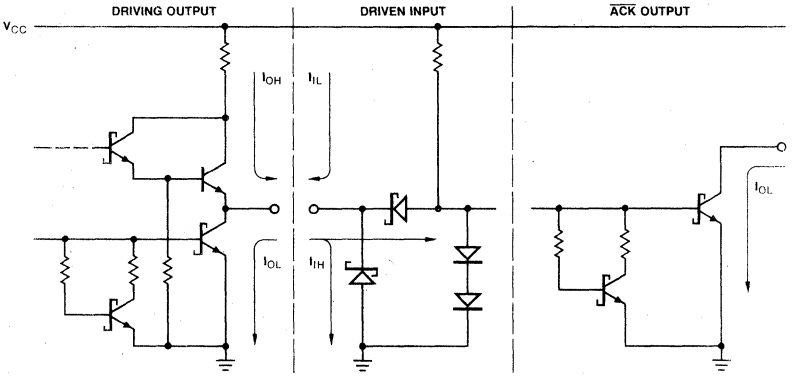
$\overline{Y}_i$ The eight active LOW chip select outputs.

METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.081" X 0.096"

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



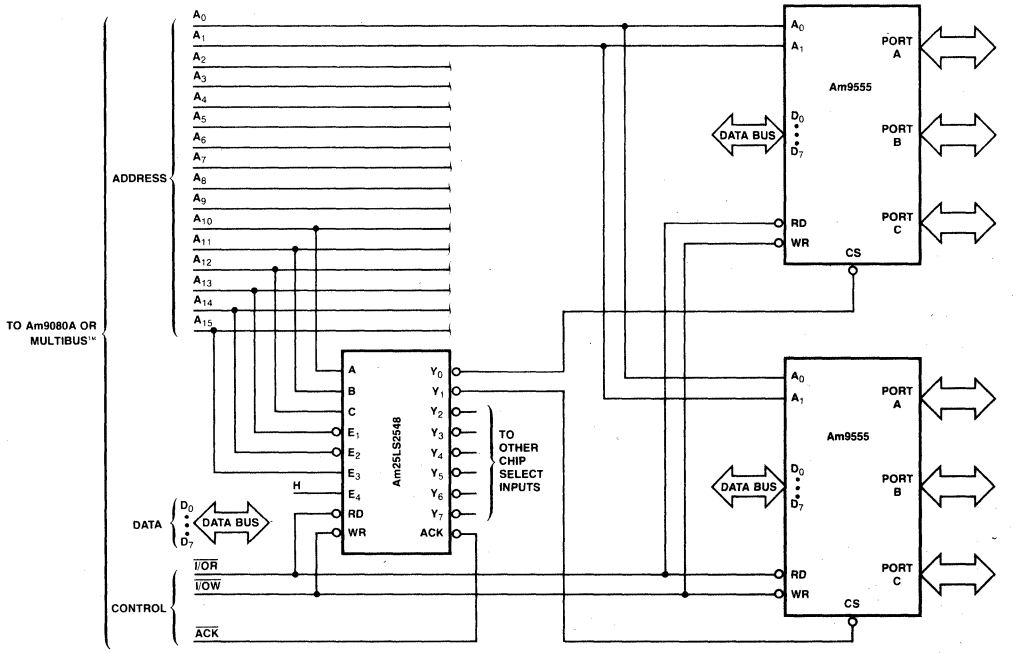
Note: Actual current flow direction shown.

BLI-048

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0 to +70°C	AM25LS2548PC
Hermetic DIP	0 to +70°C	AM25LS2548DC
Chip-Pak	0 to +70°C	AM25LS2548LC
Dice	0 to +70°C	AM25LS2548XC
Hermetic DIP	−55 to +125°C	AM25LS2548DM
Hermetic Flat-Pak	−55 to +125°C	AM25LS2548FM
Chip-Pak	−55 to +125°C	AM25LS2548LM
Dice	−55 to +125°C	AM25LS2548XM

APPLICATION DIAGRAM



BLI-049

FUNCTION TABLES

CHIP SELECT OUTPUTS Y_i

C	B	A	$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	H	L	H	H	H	H	H
L	H	H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	L	L	H	H	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	H	H	L	H	H
H	H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	H	H	L
X	X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	X	X	X	H	X	X	H	H	H	H	H	H	H	H
X	X	X	X	X	L	X	H	H	H	H	H	H	H	H
X	X	X	X	X	X	L	H	H	H	H	H	H	H	H

ACKNOWLEDGE OUTPUT $\overline{ACK}$

$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	$\overline{RD}$	$\overline{WR}$	$\overline{ACK}$
H	X	X	X	X	X	H
X	H	X	X	X	X	H
X	X	L	X	X	X	H
X	X	X	L	X	X	H
L	L	H	H	L	X	L
L	L	H	H	X	L	L

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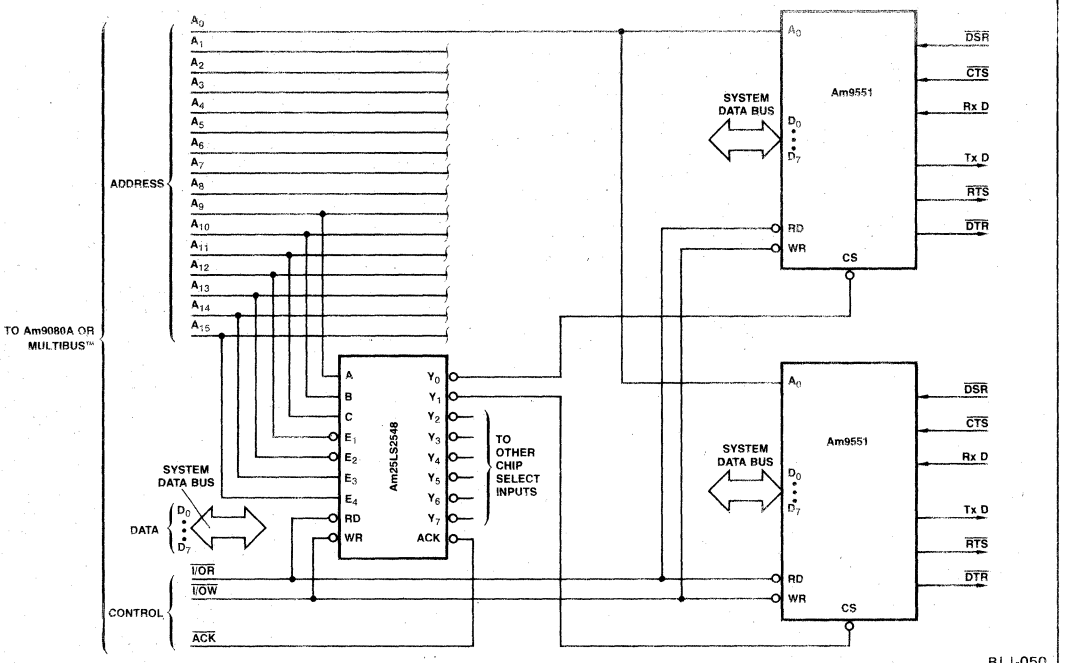
APPLICATION DIAGRAM



Am25LS2568 • Am25LS2569

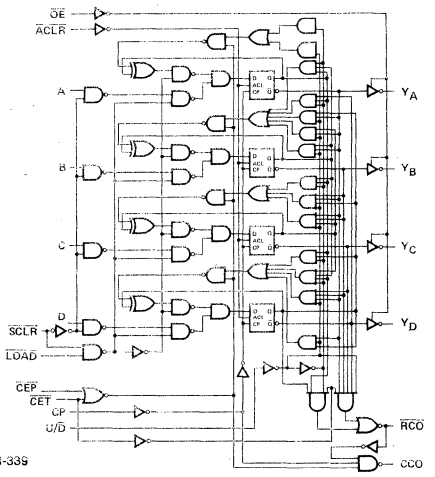
Four-Bit Up/Down Counters with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- 4-bit synchronous counter, synchronously programmable
- Both synchronous and asynchronous clear inputs
- Three-state counter outputs interface directly with bus organized systems
- Internal look-ahead carry logic and two count enable lines for high speed cascaded operation
- Ripple carry output for cascading
- Clock carry output for convenient modulo configuration
- Fully buffered outputs
- Second sourced as the 54LS/74LS568 and LS569
- Advanced low-power Schottky technology

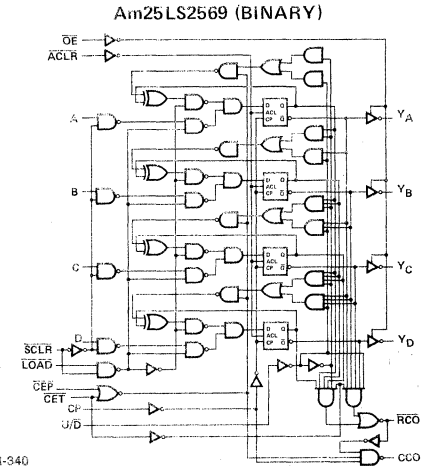
LOGIC DIAGRAMS

Am25LS2568 (BCD)



MPR-339

Am25LS2569 (BINARY)



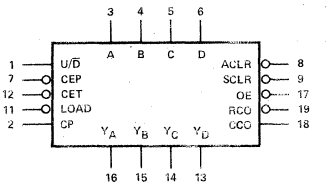
MPR-340

FUNCTIONAL DESCRIPTION

The Am25LS2568 and Am25LS2569 are programmable up/down BCD and Binary counters respectively with three-state outputs for bus organized systems. All functions except output enable ($\overline{OE}$) and asynchronous clear ($\overline{ACLR}$) occur on the positive edge of the clock input (CP).

With the $\overline{LOAD}$ input LOW, the outputs will be programmed by the parallel data inputs (A, B, C, D) on the next clock edge. Counting is enabled only when $\overline{CEP}$ and $\overline{CET}$ are LOW and LOAD is HIGH. The up-down input ($U/\overline{D}$) controls the direction of count, HIGH counts up and LOW counts down. Internal look-ahead carry logic and an active LOW ripple carry output ($\overline{RCO}$) allows for high-speed counting and cascading. During up-count, the $\overline{RCO}$ is LOW at binary 9 for the LS2568 (binary 15 for the LS2569) and upon down-count, it is LOW at binary 0. Normal cascaded operations requires only the $\overline{RCO}$ to be connected to the succeeding block at $\overline{CET}$. When counting, the clocked carry output (CCO) provides a HIGH-LOW-HIGH pulse for a duration equal to the LOW time of the clock pulse and only when $\overline{RCO}$ is LOW. Two active LOW reset lines are available, synchronous clear ($\overline{SCLR}$) and a master reset asynchronous clear ($\overline{ACLR}$). The output control ($\overline{OE}$) input forces the counter output into the high impedance state when HIGH and when LOW, the counter outputs are enabled.

LOGIC SYMBOL



V_{CC} = Pin 20

GND = Pin 10

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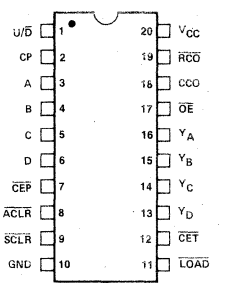
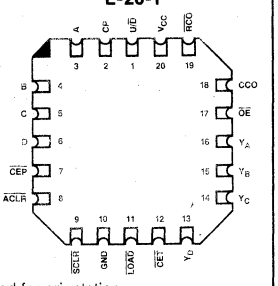
CONNECTION DIAGRAMS — Top Views

DIP



Leadless Chip Carrier L-20-1



Note: Pin 1 is marked for orientation.

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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$	MIN. = 4.75 V	MAX. = 5.25 V
MIL	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$	MIN. = 4.50 V	MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)				Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	Y_i	MIL, $I_{OH} = -1.0mA$		2.4	3.4		Volts
				COM'L, $I_{OH} = -2.6mA$		2.4	3.2		
			$\overline{RCO}$, CCO	$I_{OH} = -440\mu A$	MIL	2.5	3.4		
					COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}		$I_{OL} = 4.0mA$				0.4	Volts
				$I_{OL} = 8.0mA$				0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs				2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			MIL			0.7	Volts
					COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$						−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$	$\overline{ACLR}$, $\overline{OE}$, $U/\overline{D}$, $\overline{Load}$					−0.3	mA
			A, B, C, D, CP, $\overline{CEP}$					−0.4	
			$\overline{CET}$, $\overline{SCLR}$					−0.65	
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$						20	µA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$						0.1	mA
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$					−20	µA
			$V_O = 2.4V$					20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.				−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.					28	43	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $\overline{OE}$ = HIGH, all other inputs = GND, all outputs open.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Any Q; $\overline{Load}$ = LOW			12	18	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}				14	21		
t_{PLH}	Clock to Any Q; $\overline{Load}$ = HIGH			12	18	ns	
t_{PHL}				14	21		
t_{PLH}	$\overline{CET}$ to $\overline{RCO}$			11	16	ns	
t_{PHL}				6	10		
t_{PLH}	U/$\overline{D}$ to $\overline{RCO}$			15	23	ns	
t_{PHL}				13	20		
t_{PLH}	Clock to $\overline{RCO}$			24	35	ns	
t_{PHL}				18	26		
t_{PLH}	Clock to CCO			10	15	ns	
t_{PHL}				10	15		
t_{PLH}	$\overline{CET}$ or $\overline{CEP}$ to CCO			10	15	ns	
t_{PHL}				17	25		
t_{PLH}	$\overline{ACLR}$ to Any Q			N.A.	N.A.	ns	
t_{PHL}				17	26		
t_s	Set-up	A, B, C, D	22			ns	
		$\overline{SCLR}$	20				
		$\overline{Load}$	30				
		U/$\overline{D}$	30				
		$\overline{CET}$, $\overline{CEP}$	25				
t_s	$\overline{SCLR}$ Recovery (inactive) to Clock		30			ns	
t_h	Data Hold		0			ns	
f_{max}	Maximum Clock Frequency (Note 1)		25	40		MHz	
t_{pw}	Clock Pulse Width		25			ns	
t_{PZH}	$\overline{OE}$ to Any Q; Enable				11	ns	
t_{PZL}					19		
t_{PHZ}	$\overline{OE}$ to Any Q; Disable				18	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{PLZ}					24		

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

Am25LS2568/2569
FUNCTION TABLE

	INPUTS												OUTPUTS					
MODE	LOAD	CEP	CET	U/$\overline{D}$	ASYNC CLEAR	SYNC CLEAR	$\overline{OE}$(1)	D_0	D_1	D_2	D_3	CP	Q_0	Q_1	Q_2	Q_3	RC	CLOCK CARRY
Clear (ASYNC)	X	X	X	1	0	X	0	X	X	X	X	X	0	0	0	0	1	1
	X	X	X	0	0	X	0	X	X	X	X	X	0	0	0	0	0	⊓(2)
Clear (SYNC)	X	X	X	1	1	0	0	X	X	X	X	↑	0	0	0	0	1	1
	X	X	X	0	1	0	0	X	X	X	X	↑	0	0	0	0	0	⊓(2)
Load	0	X	1	X	1	1	0	X	X	X	X	↑	$Q_n = D_n$				1	1
	0	X	0	0	1	1	0	0	0	0	0	↑	0	0	0	0	0	⊓(2)
	0	X	0	1	1	1	0	1	1	1	1(3)	↑	1	1	1	1(3)	0	⊓(2)
Count Up	1	0	0	1	1	1	0	X	X	X	X	↑	Q_{n+1}				(4)	(5)
Count Down	1	0	0	0	1	1	0	X	X	X	X	↑	Q_{n-1}				(6)	(5)
Inhibit	1	0	1	X	1	1	0	X	X	X	X	↑	N.C.				N.C.	1
	1	1	0	X	1	1	0	X	X	X	X	↑	N.C.				N.C.	1
	1	1	1	X	1	1	0	X	X	X	X	↑	N.C.				N.C.	1
Output Disable	X	X	X	X	X	X	1	X	X	X	X	X	Z	Z	Z	Z	N.C.	N.C.

↑ = CLOCK LOW-to-HIGH transition
X = Don't Care
D_n = D_0 thru D_3 input level prior to clock transition
Q_{n+1} = Next higher count in binary sequence
Q_{n-1} = Next lower count in binary sequence
N.C. = No change

Notes: 1. Register performs all correct logic for any state of $\overline{OE}$, but $\overline{OE}$ = 0 to view outputs.
2. Follows CLOCK if CET = CEP = 0, otherwise remains HIGH.
3. 1001 for LS68.
4. LOW for one full CLOCK cycle when maximum count is reached, otherwise remains HIGH.
5. Follows CLOCK when RC = 0.
6. LOW for one full CLOCK cycle when minimum count is reached, otherwise remains HIGH.

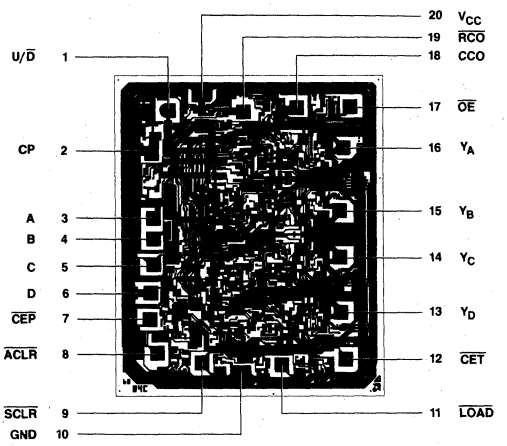
Am25LS2568 • Am25LS2569
SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am25LS COM'L $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$ Min.	Am25LS COM'L Max.	Am25LS MIL $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$ Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Clock to Any Q; $\overline{Load}$ = LOW			22		24	ns	$C_L = 50pF$, $R_L = 2.0k\Omega$
t_{PHL}				29		35		
t_{PLH}	Clock to Any Q; $\overline{Load}$ = HIGH			22		24	ns	
t_{PHL}				29		35		
t_{PLH}	$\overline{CET}$ to $\overline{RCO}$			18		19	ns	
t_{PHL}				17		21		
t_{PLH}	U/$\overline{D}$ to $\overline{RCO}$			26		28	ns	
t_{PHL}				26		30		
t_{PLH}	Clock to $\overline{RCO}$			39		40	ns	
t_{PHL}				34		39		
t_{PLH}	Clock to CCO			17		18	ns	
t_{PHL}				22		27		
t_{PLH}	$\overline{CET}$ or $\overline{CEP}$ to CCO			16		17	ns	
t_{PHL}				36		45		
t_{PLH}	$\overline{ACLR}$ to Any Q			N.A.		N.A.	ns	
t_{PHL}				37		45		
t_s	Set-up	A, B, C, D	29		35		ns	
		$\overline{SCLR}$	25		30			
		$\overline{Load}$	38		45			
		U/$\overline{D}$	38		45			
		$\overline{CET}$, $\overline{CEP}$	33		40			
t_s	SCLR Recovery (inactive) to Clock		39		50		ns	
t_h	Data Hold		0		5		ns	
f_{max}	Maximum Clock Frequency (Note 1)		20		18		MHz	
t_{pw}	Clock Pulse Width		31		37		ns	
t_{ZH}	$\overline{OE}$ to Any Q; Enable			16		20	ns	
t_{ZL}				26		34		
t_{HZ}	$\overline{OE}$ to Any Q; Disable			20		22	ns	$C_L = 5.0pF$, $R_L = 2.0k\Omega$
t_{LZ}				30		36		

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.
N.A. not applicable.

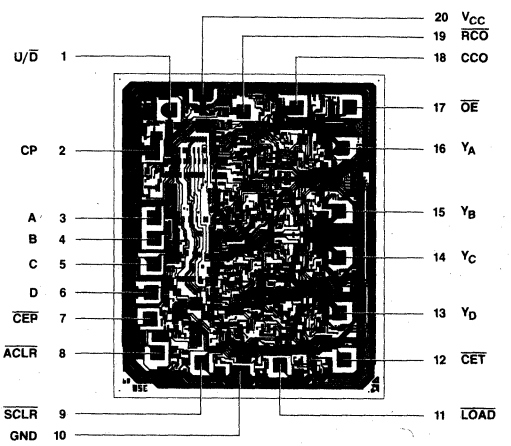
METALLIZATION AND PAD LAYOUTS

Am25LS2568



DIE SIZE 0.087" X 0.103"

Am25LS2569

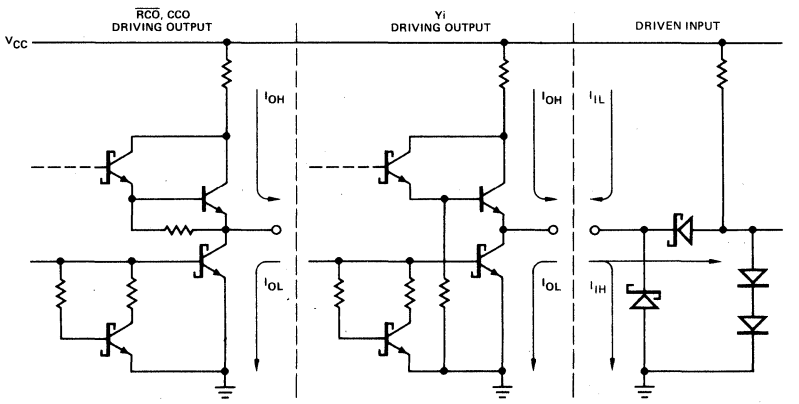


DIE SIZE 0.087" X 0.103"

DEFINITION OF FUNCTIONAL TERMS

A, B, C, D	The four programmable data inputs.
$\overline{CEP}$	Count Enable Parallel. Can be used to enable and inhibit counting in high speed cascaded operation. $\overline{CEP}$ must be LOW to count.
$\overline{CET}$	Count Enable Trickle. Enables the ripple carry output for cascaded operation. Must be LOW to count.
CP	Clock Pulse. All synchronous functions occur on the LOW-to-HIGH transition of the clock.
$\overline{LOAD}$	Enables parallel load of counter outputs from data inputs on the next clock edge. Must be HIGH to count.
U/$\overline{D}$	Up/Down Count Control. HIGH counts up and LOW counts down.
$\overline{ACLR}$	Asynchronous Clear. Master reset of counters to zero when $\overline{ACLR}$ is LOW, independent of the clock.
$\overline{SCLR}$	Synchronous clear of counters to zero on the next clock edge when $\overline{SCLR}$ is LOW.
$\overline{OE}$	A HIGH on the output control sets the four counter outputs in the high impedance, and a LOW, enables the output.
Y_A, Y_B, Y_C, Y_D	The four counter outputs.
$\overline{RCO}$	Ripple Carry Output. Output will be LOW on the maximum count on up-count. Upon down-count, $\overline{RCO}$ is LOW at 0000.
CCO	Clock Carry Output. While counting and $\overline{RCO}$ is LOW, CCO will follow the clock HIGH-LOW-HIGH transition.

Am25LS
LOW-POWER SCHOTTKY INPUT/OUTPUT
CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

Am26S and Am26LS Interface Family Index

Am26S02

Schottky Dual Retriggerable, Resettable Monostable Multivibrator

Distinctive Characteristics

- Advanced Schottky technology with PNP inputs
- Retriggerable 0% to 100% duty cycle
- 28ns to ∞ output pulse width range
- 100kΩ maximum timing resistor value
- Am26S02XM typical pulse width change of only 1.0% over −55°C to +125°C with R_X = 100kΩ.
- Am26S02XC typical pulse width change of only 0.4% over 0°C to +70°C with R_X = 100kΩ

FUNCTIONAL DESCRIPTION

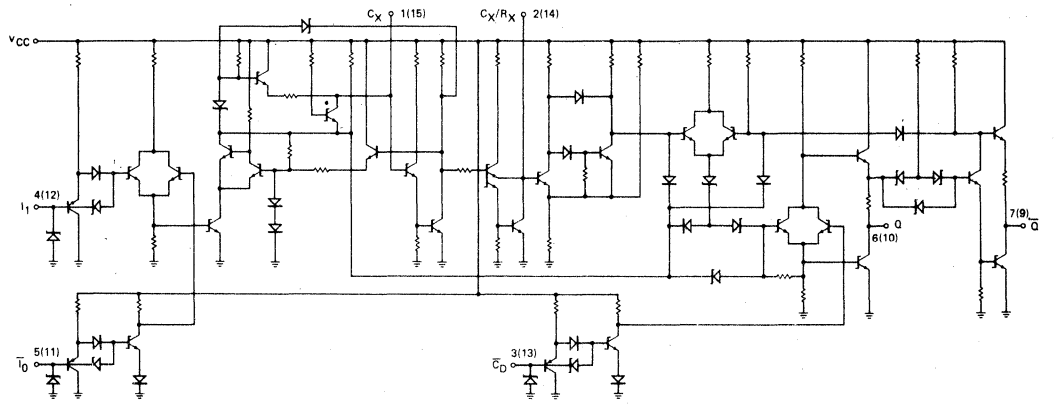
The Am26S02 is a dual DC level sensitive, retriggerable, resettable monostable multivibrator built using advanced Schottky technology. The output pulse duration and accuracy depend on the external timing components of each multivibrator. The Am26S02 features PNP inputs to reduce the input loading.

Provision is made on each multivibrator circuit for triggering the PNP inputs on either the rising or falling edge of an input signal by including an inverting and non-inverting trigger input. These PNP inputs are DC coupled making triggering independent of the input rise or fall time. Each time the monostable trigger input is activated from the OR trigger gate, full pulse length triggering occurs independent of the present state of the monostable.

The direct clear PNP input allows a timing cycle to be terminated at any time during the cycle. A LOW on the clear input forces the Q output LOW regardless of the $\overline{I_0}$ or I_1 inputs.

The Am26S02XM has a typical pulse width change of only 1.0% over the full military −55°C to +125°C temperature range and the Am26S02XC has a typical pulse width change of only 0.4% over the commercial 0°C to +70°C temperature range with a R_X = 100kΩ.

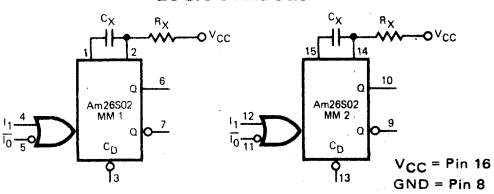
SCHEMATIC DIAGRAM
(One Monostable Multivibrator Shown)



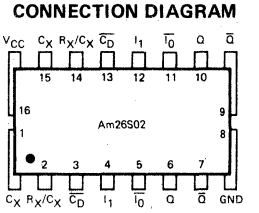
ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to + 70°C	AM26S02PC
Hermetic DIP	0°C to + 70°C	AM26S02DC
Dice	0°C to + 70°C	AM26S02XC
Hermetic DIP	−55°C to +125°C	AM26S02DM
Hermetic Flat Pak	−55°C to +125°C	AM26S02FM
Dice	−55°C to +125°C	AM26S02XM

LOGIC SYMBOLS



CONNECTION DIAGRAM



Note:
Pin 1 is marked for orientation.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am26S02XC	T_A = 0°C to +70°C	V_{CC} = 5.0 V ±5% (COM'L)	MIN. = 4.75 V	MAX. = 5.25 V
Am26S02XM	T_A = −55°C to +125°C	V_{CC} = 5.0 V ±10% (MIL)	MIN. = 4.5 V	MAX. = 5.5 V

Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2mA V_{IN} = V_{IH} or V_{IL}	2.5	2.8		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}		0.38	0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA		−0.8	−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V		−0.15	−0.4	mA
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V		0.1	20	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 1.0V T_A = 25°C Only	−8	−15	−35	mA
I_{CC}	Power Supply Current	V_{CC} = 5.0 V, I_{IX} = 0.33 mA (Notes 5 & 6)		48	69	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} is measured with pin 5 and 11 grounded and I_{IX} applied to pins 2 and 14.
6. I_{IX} is the current into the $R_X C_X$ node to simulate R_X.

Switching Characteristics (T_A = +25°C)

Parameters	Description		Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	$\overline{I_0}$ to Q		V_{CC} = 5.0 V, R_L = 280 Ω, C_L = 15 pF, R_X = 5kΩ, C_X = 0 pF		13	20	ns
t_{PHL}	$\overline{I_0}$ to $\overline{Q}$				15	23	ns
t_{PLH}	I_1 to Q				12	20	ns
t_{PHL}	I_1 to $\overline{Q}$				12	20	ns
t_{PLH}	Clear to $\overline{Q}$				21		ns
t_{PHL}	Clear to Q				9	13	ns
t_{pw}	Pulse Width	$\overline{I_0}$ HIGH or I_1 LOW		20	10		ns
		$\overline{I_0}$ LOW or I_1 HIGH		16	7		ns
		Clear LOW		24	16		ns
t_s	Clear Recovery (inactive) to Trigger			−10	−22		ns
t_{pwQ} (Min.)	Minimum Pulse Width Q Output		V_{CC} = 5.0 V, R_X = 5.0 kΩ, C_X = 0 pF, R_L = 1.0 kΩ	27	33	39	ns
t_{pwQ}	Pulse Width Q Output		V_{CC} = 5.0 V, R_L = 280 Ω, C_L = 15 pF, R_X = 10 kΩ, C_X = 1000 pF (CK05 Type)	3.23	3.42	3.61	μs
R_X	Timing Resistor		0°C to 70°C	5		100	kΩ
			−55°C to +125°C	5		50	

DEFINITION OF FUNCTIONAL TERMS:

$\overline{C_D}$ Asynchronous direct CLEAR. A LOW on the clear input resets the monostable regardless of the other inputs.

$\overline{I_0}$ Active-LOW input. With I_1 LOW, a HIGH-to-LOW transition will trigger the monostable.

I_1 Active-HIGH input. With $\overline{I_0}$ HIGH, a LOW-to-HIGH transition will trigger the monostable.

Q The TRUE monostable output.

$\overline{Q}$ The Complement monostable output.

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{C_D}$	I_1	$\overline{I_0}$	Q	$\overline{Q}$
L	X	X	L	H
H	H	X	L	H
H	L	↓	⎍	⎏
H	X	L	L	H
H	↑	H	⎍	⎏

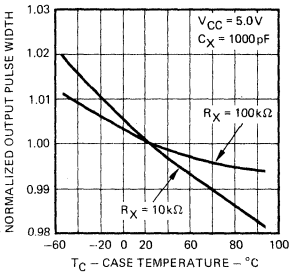
H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition
↓ = HIGH-to-LOW Transition
⎍ = LOW-HIGH-LOW Pulse
⎏ = HIGH-LOW-HIGH Pulse
X = Don't Care

LOADING RULES (In Unit Loads)

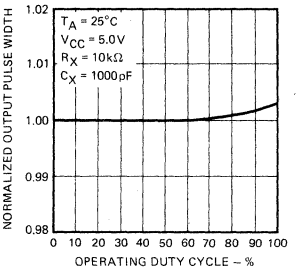
Input/Output	Pin No.'s		Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
C_X	Mono 1	1	–	–	–
R_X/C_X		2	–	–	–
$\overline{C_D}$		3	0.4	–	–
I_1		4	0.4	–	–
$\overline{I_0}$		5	0.4	–	–
Q		6	–	40	10
$\overline{Q}$		7	–	40	10
GND		8	–	–	–
$\overline{Q}$	Mono 2	9	–	40	10
Q		10	–	40	10
$\overline{I_0}$		11	0.4	–	–
I_1		12	0.4	–	–
$\overline{C_D}$		13	0.4	–	–
R_X/C_X		14	–	–	–
C_X		15	–	–	–
V_{CC}		16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and –2.0mA measured at 0.5V LOW.

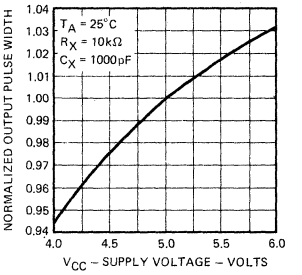
Typical Normalized Output Pulse Width Versus Case Temperature



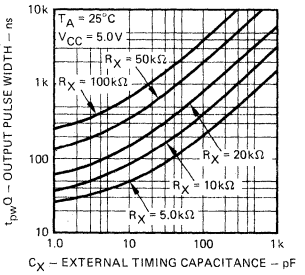
Normalized Output Pulse Width Versus Operating Duty Cycle



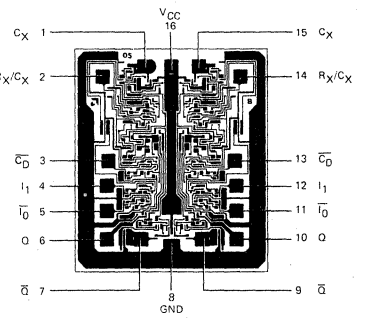
Typical Normalized Output Pulse Width Versus Supply Voltage



Output Pulse Width Versus External Timing Capacitance



Metallization and Pad Layout



DIE SIZE 0.062" X 0.071"

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OPERATION RULES

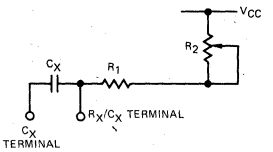
TIMING

1. Timing components C_X and R_X values.

Operating Temperature Range

	0°C to 70°C	-55°C to +125°C
R_X MIN.	5kΩ	5kΩ
R_X MAX.	100kΩ	50kΩ
C_X	any value	any value

2. Remote adjustment of timing.



$R_1 + R_2 = R_X$

$R_1 \geq R_X$ MIN.

$R_2 < R_X$ MAX. $- R_1$

In the above arrangement, R_1 and C_X should be as close as possible to the device pins to minimize stray capacitance and external noise pickup. The variable resistor R_2 can be located remotely from the device if reasonable care is used.

3. Pulse width change measurements.

The pulse width $t_{pw}Q$ is specified and measured with components of better than 0.1% accuracy. If measurements are made with reduced component tolerances, the expected accuracy should be adjusted accordingly. Note that pulse width temperature stability improves as R_X increases.

4. Timing for $C_X \leq 1000$ pF.

When using capacitor of less than or equal to 1000 pF in value, the output pulse width should be determined from the output pulse width versus external timing capacitance graph.

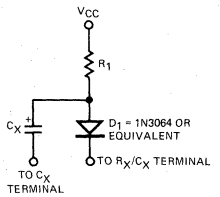
5. Timing for $C_X > 1000$ pF.

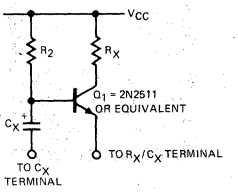
For capacitors of greater than 1000 pF in value, the output pulse width, $t_{pw}Q$, is determined by

$$t_{pw}Q = 0.30\, C_X R_X \left(1 + \frac{0.11}{R_X}\right)$$

where

R_X is in kilohms
C_X is in picofarads
$t_{pw}Q$ is in nanoseconds





$R_1 \leq 0.6 \times R_X$ MAX.

$R_2 < 0.7 \times h_{FEQ1} \times R_X$

6. Protection of electrolytic timing capacitors.

If the electrolytic capacitor to be used as C_X cannot withstand 1.0 volt reverse bias, one of the two circuit techniques shown below should be used to protect the electrolytic capacitor from the reverse voltage. The accuracy of the pulse width may be dependent on the diode (transistor) characteristics.

The output pulse width, $t_{pw}Q$ for the diode circuit modifies the previous timing equation as follows:

$$t_{pw}Q = 0.26\, C_X R_X \left(1 + \frac{0.13}{R_X}\right)$$

The output pulse width for the transistor circuit is

$$t_{pw}Q = 0.21\, C_X R_X \left(1 + \frac{0.16}{R_X}\right)$$

Notice that the transistor circuit allows values of timing resistor R_2 larger than the R_X MIN. $< R_X <$ R_X MAX. to obtain longer output pulse widths for a given C_X.

TRIGGER AND RETRIGGER

1. Triggering.

The minimum pulse width signal into input $\overline{I}_0$ or input I_1 to cause the device to trigger is 20ns. Refer to the truth table for the appropriate input conditions.

2. Retriggering.

The retriggered pulse width, $t_{pwr}Q$, is the time during which the output is active after the device is retriggered during a timing cycle. It differs from the initial pulse width $t_{pw}Q$ timing equation as follows.

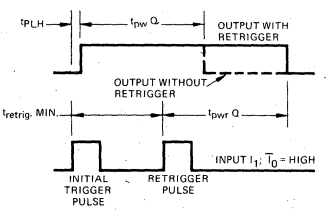
$$t_{pwr}Q = t_{pw}Q + t_{PLH}$$

where t_{PLH} is the propagation delay time from the $\overline{I}_0$ or I_1 input to the output. Note that t_{PLH} is typically 14ns and therefore becomes relatively unimportant as $t_{pw}Q$ increases.

3. Rapid retriggering.

A minimum retriggering time does exist. That is, the device cannot be retriggered until a minimum recovery time has elapsed. The minimum retrigger time is approximately.

t_{retrig} MIN. $= 0.2\, C_X$
C is in picofarads
t is in nanoseconds



CLEAR

A LOW on the clear inputs terminates the timing cycle. A new trigger cycle cannot be initiated while the clear is LOW. With the clear HIGH, the device is under the command of the I_1 and $\overline{I}_0$ inputs.

Am26S10 • Am26S11

Quad Bus Transceivers

Distinctive Characteristics

- Input to bus is inverting on Am26S10
- Input to bus is non-inverting on Am26S11
- Quad high-speed open collector bus transceivers
- Driver outputs can sink 100mA at 0.8V maximum
- Bus compatible with Am2905, Am2906, Am2907
- Advanced Schottky processing
- PNP inputs to reduce input loading

FUNCTIONAL DESCRIPTION

The Am26S10 and Am26S11 are quad Bus Transceivers consisting of four high-speed bus drivers with open-collector outputs capable of sinking 100mA at 0.8 volts and four high-speed bus receivers. Each driver output is connected internally to the high-speed bus receiver in addition to being connected to the package pin. The receiver has a Schottky TTL output capable of driving ten Schottky TTL unit loads.

An active LOW enable gate controls the four drivers so that outputs of different device drivers can be connected together for party-line operation. The enable input can be conveniently driven by active LOW decoders such as the Am25LS139.

The bus output high-drive capability in the LOW state allows party-line operation with a line impedance as low as 100Ω. The line can be terminated at both ends, and still give considerable noise margin at the receiver. The receiver typical switching point is 2.0 volts.

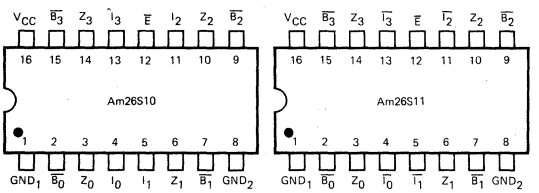
The Am26S10 and Am26S11 feature advanced Schottky processing to minimize propagation delay. The device package also has two ground pins to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both GND_1 and GND_2 should be tied to the ground bus external to the device package.

ORDERING INFORMATION

Package Type	Temperature Range	Am26S10 Order Number	Am26S11 Order Number
Molded DIP	0°C to +70°C	AM26S10PC	AM26S11PC
Hermetic DIP	0°C to +70°C	AM26S10DC	AM26S11DC
Dice	0°C to +70°C	AM26S10XC	AM26S11XC
Hermetic DIP	−55°C to +125°C	AM26S10DM	AM26S11DM
Hermetic Flat Pack	−55°C to +125°C	AM26S10FM	AM26S11FM
Dice	−55°C to +125°C	AM26S10XM	AM26S11XM

CONNECTION DIAGRAMS

Top Views

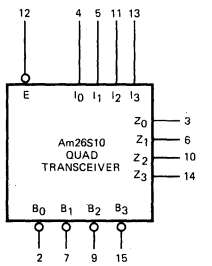


LIC-368

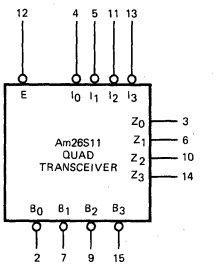
Note: Pin 1 is marked for orientation.

LIC-369

LOGIC SYMBOLS



LIC-370

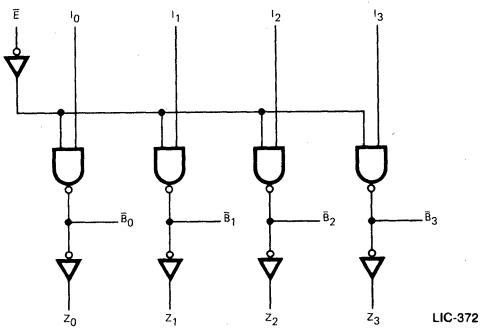


LIC-371

V_{CC} = Pin 16
GND_1 = Pin 1
GND_2 = Pin 8

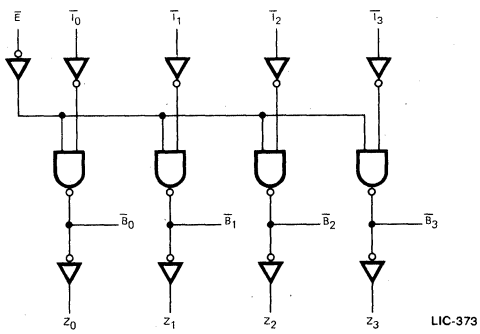
LOGIC DIAGRAMS

Am26S10



LIC-372

Am26S11



LIC-373

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Bus	200 mA
Output Current, Into Outputs (Except Bus)	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Am26S10XC, Am26S11XC	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5% (COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am26S10XM, Am26S11XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10% (MIL)	MIN. = 4.5V	MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage (Receiver Outputs)	V_{CC} = MIN., I_{OH} = −1.0mA V_{IN} = V_{IL} or V_{IH}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Receiver Outputs)	V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IL} or V_{IH}				0.5	Volts
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs				0.8	Volts
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4V	Enable			−0.36	mA
			Data			−0.54	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7V	Enable			20	µA
			Data			30	
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 5.5V				100	µA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX. (Note 3)	MIL	−20		−55	mA
			COM'L	−18		−60	
I_{CCL}	Power Supply Current (All Bus Outputs LOW)	V_{CC} = MAX. Enable = GND	Am26S10		45	70	mA
			Am26S11			80	

Bus Input/Output Characteristics

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Output LOW Voltage	V_{CC} = MIN.	MIL	I_{OL} = 40mA		0.33	0.5	Volts
				I_{OL} = 70mA		0.42	0.7	
				I_{OL} = 100mA		0.51	0.8	
			COM'L	I_{OL} = 40mA		0.33	0.5	
				I_{OL} = 70mA		0.42	0.7	
				I_{OL} = 100mA		0.51	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.		V_O = 0.8V			−50	µA
			MIL	V_O = 4.5V			200	
			COM'L	V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power Off)	V_O = 4.5V					100	µA
V_{TH}	Receiver Input HIGH Threshold	Bus Enable = 2.4V V_{CC} = MAX	MIL		2.4	2.0		Volts
			COM'L		2.25	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus Enable = 2.4V V_{CC} = MIN	MIL			2.0	1.6	Volts
			COM'L			2.0	1.75	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Switching Characteristics (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Data Input to Bus	Am26S10	R_B = 50Ω C_B = 50pF (Note 1)		10	15	ns
t_{PHL}					10	15	
t_{PLH}		Am26S11			12	19	
t_{PHL}					12	19	
t_{PLH}	Enable Input to Bus	Am26S10			14	18	ns
t_{PHL}					13	18	
t_{PLH}		Am26S11			15	20	
t_{PHL}					14	20	
t_{PLH}	Bus to Receiver Out		R_B = 50Ω, R_L = 280Ω C_B = 50pF (Note 1), C_L = 15pF		10	15	ns
t_{PHL}					10	15	
t_r	Bus		R_B = 50Ω C_B = 50pF (Note 1)	4.0	10		ns
t_f	Bus			2.0	4.0		ns

Note 1. Includes probe and jig capacitance.

TRUTH TABLES

Am26S10

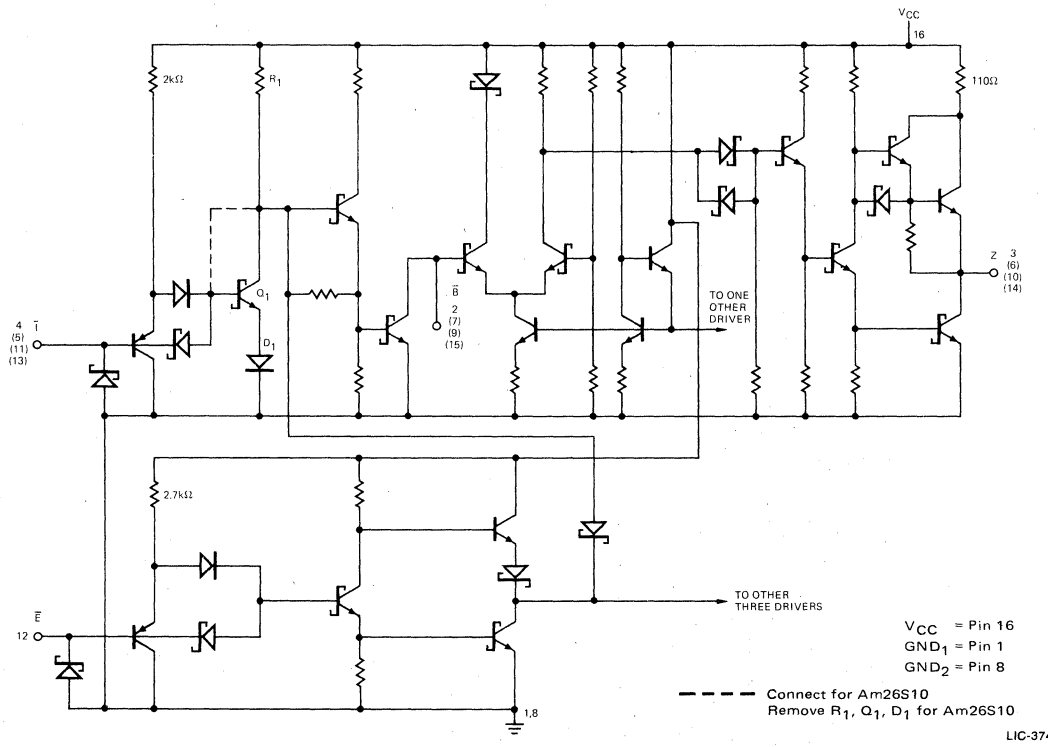
Inputs		Outputs	
$\overline{E}$	I	$\overline{B}$	Z
L	L	H	L
L	H	L	H
H	X	Y	$\overline{Y}$

Am26S11

Inputs		Outputs	
$\overline{E}$	$\overline{I}$	$\overline{B}$	Z
L	L	L	H
L	H	H	L
H	X	Y	$\overline{Y}$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Y = Voltage Level of Bus (Assumes Control by Another Bus Transceiver)

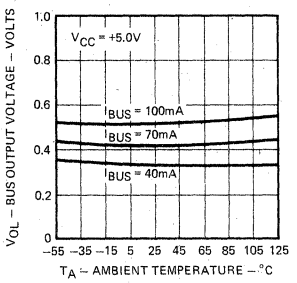
Am26S10/Am26S11 SCHEMATIC DIAGRAM



10

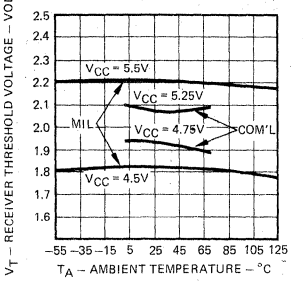
TYPICAL PERFORMANCE CURVES

Typical Bus Output Low Voltage Versus Ambient Temperature



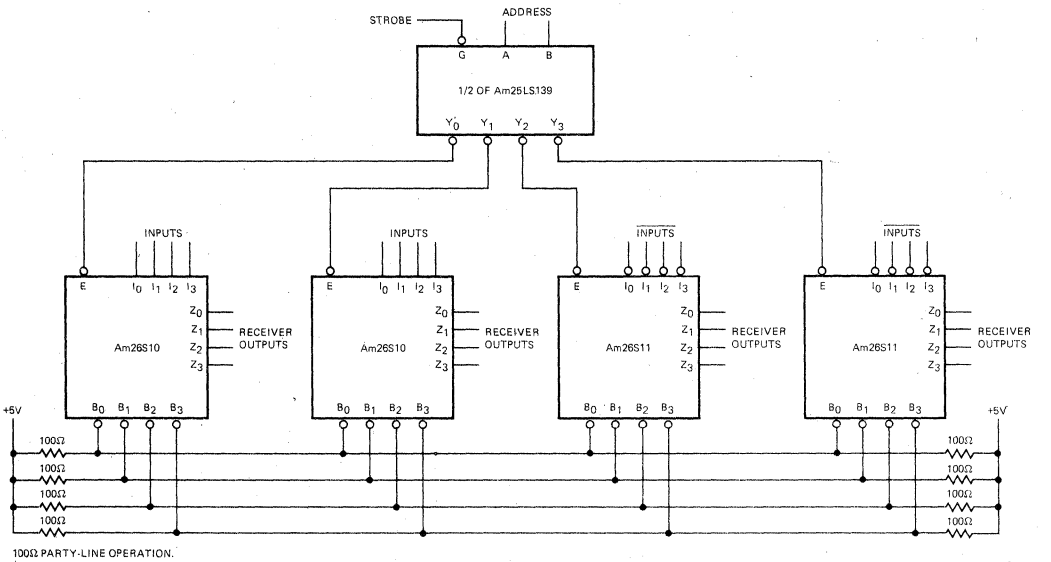
LIC-375

Receiver Threshold Variation Versus Ambient Temperature



LIC-376

TYPICAL APPLICATION

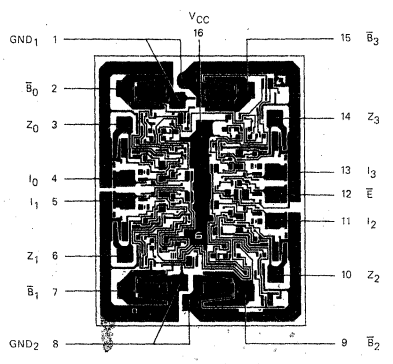


100Ω PARTY-LINE OPERATION.

LIC-377

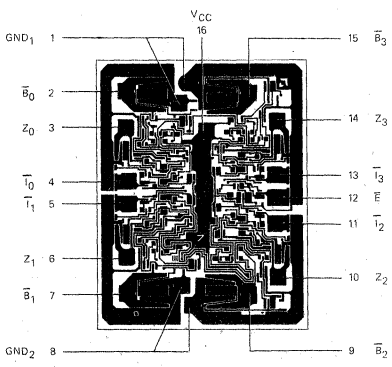
Metallization and Pad Layout

Am26S10



DIE SIZE 0.059" X 0.075"

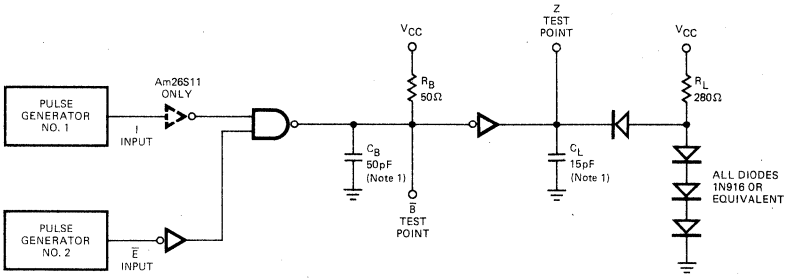
Am26S11



DIE SIZE 0.059" X 0.075"

SWITCHING CHARACTERISTICS

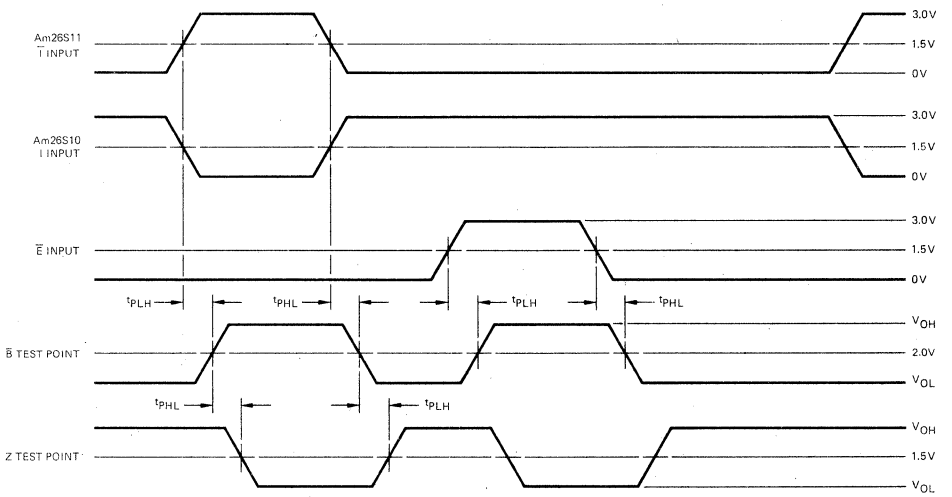
TEST CIRCUIT



LIC-378

Note 1. Includes Probe and Jig Capacitance.

WAVEFORMS



LIC-379

Am26S12 • Am26S12A

Quad Bus Transceiver

Distinctive Characteristics

- Quad high-speed bus transceivers
- Driver outputs can sink 100mA at 0.7V typically
- Choice of receiver hysteresis characteristics

FUNCTIONAL DESCRIPTION

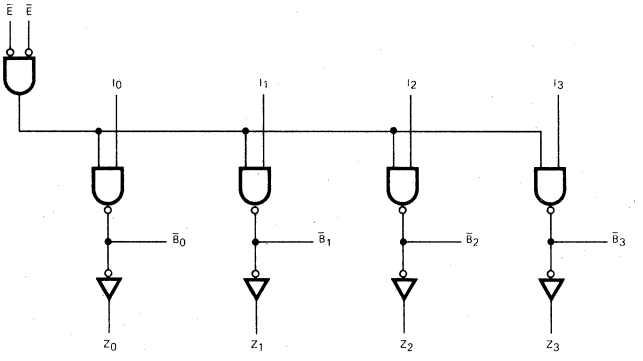
The Am26S12 • Am26S12A are high-speed quad Bus Transceivers consisting of four high-speed bus drivers with open-collector outputs capable of sinking 100mA at 0.7 volts and four high-speed bus receivers. Each driver output is brought out and also connected internally to the high-speed bus receiver. The receiver has an input hysteresis characteristic and a TTL output capable of driving ten TTL Loads.

An active LOW, two-input AND gate controls the four drivers so that outputs of different device drivers can be connected together for party-line operation. The enable inputs can be conveniently driven by active LOW decoders such as the Am54S/74S139.

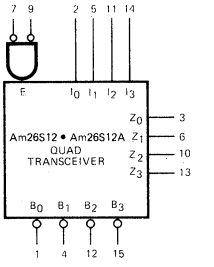
The high-drive capability in the LOW state allows party-line operation with a line impedance as low as 100Ω. The line can be terminated at both ends, and still give considerable noise margin at the receiver. The hysteresis characteristic of the Am26S12 receiver is chosen so that the receiver output switches to a HIGH logic level when the receiver input is at a HIGH logic level and moves to 1.4 volts typically, and switches to a LOW logic level when the receiver input is at a LOW logic level and moves to 2.0 volts typically. This hysteresis characteristic makes the receiver very insensitive to noise on the bus.

The Am26S12A is functionally identical to the Am26S12 but has a different hysteresis characteristic so that the output switches with the input being typically at 1.2 volts or 2.25 volts. In both devices the threshold margin, the difference between the switching points, is greater than 0.4 volts.

LOGIC DIAGRAM/SYMBOL



LIC-380



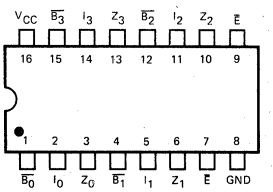
V_{CC} = PIN 16
GND = Pin 8

LIC-381

ORDERING INFORMATION

Package Type	Temperature Range	Am26S12 Order Number	Am26S12A Order Number
Molded DIP	0°C to +75°C	AM26S12PC	AM26S12APC
Hermetic DIP	0°C to +75°C	AM26S12DC	AM26S12ADC
Dice	0°C to +75°C	AM26S12XC	AM26S12AXC
Hermetic DIP	–55°C to +125°C	AM26S12DM	AM26S12ADM
Flat Pak	–55°C to +125°C	AM26S12FM	AM26S12AFM
Dice	–55°C to +125°C	AM26S12XM	AM26S12AXM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LIC-382

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Outputs (BUS)	200mA
Output Current, Into Outputs (Receiver)	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am26S12XC-Am26S12AXC $T_A = 0°C$ to $+75°C$ $V_{CC} = 5.0V \pm 5\%$ (COM Range)
Am26S12XM-Am26S12AXM $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIL Range) Note 1

Parameters	Description	Test Conditions	Min.	Typ. (Note 2)	Max.	Units
I_{CC}	Power Supply Current	V_{CC} = MAX.		46	70	mA
I_{BUS}	Bus Leakage Current	V_{CC} = MAX. or 0V; V_{BUS} = 4.0V; Driver in OFF State			100	µA

Driver Characteristics

V_{OL} (Note 1)	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	COM'L	I_{OL} = 100mA		0.7	0.8	Volts
			MIL	I_{OL} = 60mA		0.55	0.7	Volts
				I_{OL} = 100mA		0.7	0.85	
V_{IH}	Input HIGH Voltage				2.0			Volts
V_{IL}	Input LOW Voltage						0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_I	Input Current at Maximum Input Voltage	V_{CC} = MAX., V_I = 5.5V					1.0	mA
I_{IH}	Unit Load Input HIGH Current	V_{CC} = MAX., V_I = 2.4V				1.0	40	µA
I_{IL}	Unit Load Input LOW Current	V_{CC} = MAX., V_I = 0.4V				−0.4	−1.6	mA

Receiver Characteristics

V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −800µA, $V_{IN} = V_{IL}$ (Receiver)		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA, $V_{IN} = V_{IL}$ (Receiver)			0.4	0.5	Volts
V_{IH}	Input HIGH Level Threshold	$\overline{E}$ = H	Am26S12	1.8	2.0	2.2	Volts
			Am26S12A	2.05	2.25	2.45	
V_{IL}	Input LOW Level Threshold	$\overline{E}$ = H	Am26S12	1.2	1.4	1.6	Volts
			Am26S12A	1.0	1.2	1.4	
V_{TM}	Input Threshold Margin	$\overline{E}$ = H		0.4			Volts
I_{OS}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V		−20		−55	mA

Notes: 1. For the Am26S12FM, Am26S12AFM the output current must be limited at 60mA or the maximum case temperature limited to 125°C for correct operation.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

Switching Characteristics ($T_A = 25°C$, $V_{CC} = 5.0V$)

Parameters	Description	Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Turn Off Delay Input to Bus	C_{LB} = 15pF, R_{LB} = 100Ω		7	11	ns
t_{PHL}	Turn On Delay Input to Bus	C_{LB} = 300pF, R_{LB} = 50Ω		14	21	ns
t_{PLH}	Turn Off Delay Enable to Bus	C_{LB} = 15pF, R_{LB} = 50Ω		10	15	ns
t_{PHL}	Turn On Delay Enable to Bus	C_{LB} = 15pF, R_{LB} = 50Ω		10	15	ns
t_{PLH}	Turn Off Delay Bus to Output	C_L = 15pF		18	26	ns
t_{PHL}	Turn On Delay Bus to Output	C_L = 15pF		18	26	ns

Am26S12/26S12A APPLICATION

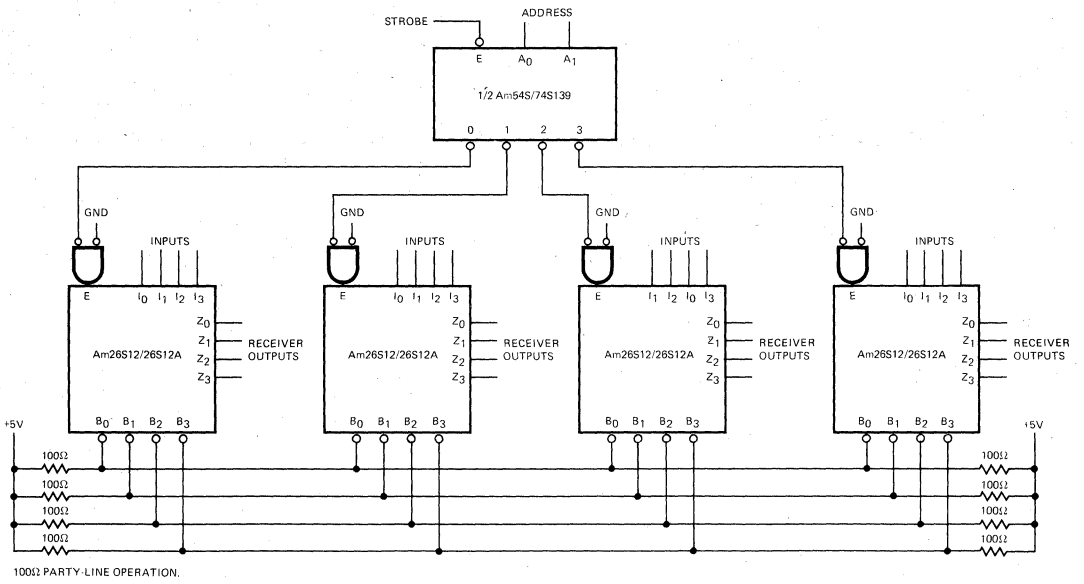
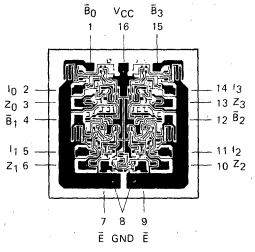


Figure 6

Metallization and Pad Layout



DIE SIZE: 0.071" x 0.072"

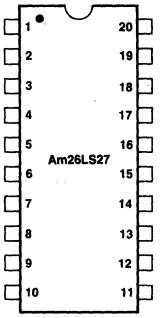
Am26LS27 • Am26LS28

Dual EIA RS-aaa Party Line Transceivers

Am26LS27 FEATURES

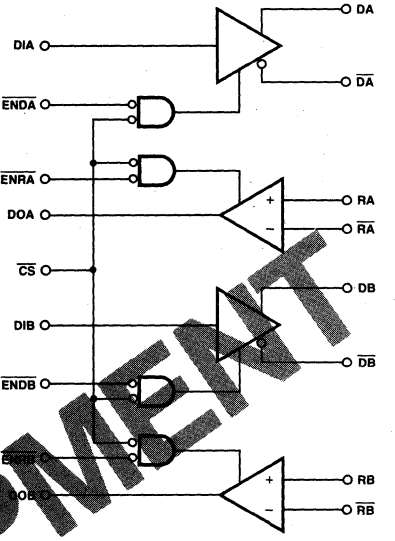
- Dual EIA RS-aaa party line transceiver
- 5MHz max. baud rate
- Drives dual terminated twisted pair line with up to 32 transceivers on line
- Output short circuit protected to V_{CM} limits
- High Z output at V_{CC} = max. and zero
- Separate enable gating for serial applications

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

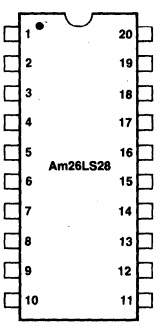
Am26LS27 LOGIC DIAGRAM



Am26LS28 FEATURES

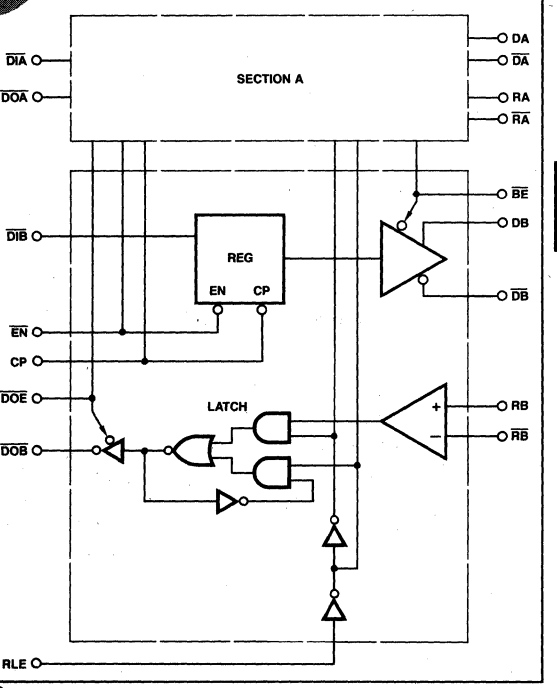
- Dual EIA RS-aaa party line transceiver
- 5MHz max. baud rate
- Drives dual terminated twisted pair line with up to 32 transceivers on line
- Output short circuit protected to V_{CM} limits
- High Z output at V_{CC} = max. and zero
- Latch on inputs and outputs with common enables for parallel application
- Three-state receiver outputs with common enable

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

Am26LS28 LOGIC DIAGRAM



10

Am26LS29

Quad Three-State Single Ended RS-423 Line Driver

DISTINCTIVE CHARACTERISTICS

- Four single ended line drivers in one package for maximum package density
- Output short-circuit protection
- Individual rise time control for each output
- High capacitive load drive capability
- Low I_{CC} and I_{EE} power consumption (26mW/driver typ.)
- Meets all requirements of RS-423
- Three-state outputs for bus oriented systems
- Outputs do not clamp line with power off or in hi-impedance state over entire transmission line voltage range of RS-423
- Low current PNP inputs compatible with TTL, MOS and CMOS
- Available in military and commercial temperature range
- Advanced low power Schottky processing

FUNCTIONAL DESCRIPTION

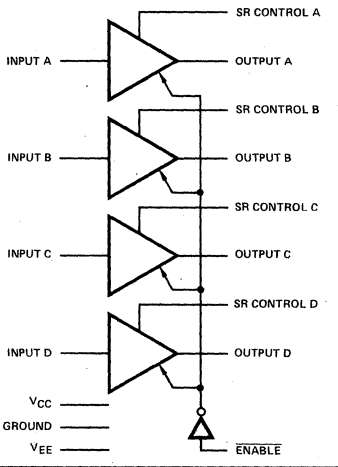
The Am26LS29 is a quad single ended line driver, designed for digital data transmission. The Am26LS29 meets all the requirements of EIA Standard RS-423 and Federal STD 1030. It features four buffered outputs with high source and sink current, and output short circuit protection.

A slew rate control pin allows the use of an external capacitor to control slew rate for suppression of near end cross talk to receivers in the cable.

The Am26LS29 has three-state outputs for bus oriented systems. The outputs in the hi-impedance state will not clamp the line over the transmission line voltage of RS-423. A typical full duplex system would use the Am26LS29 line driver and up to twelve Am26LS32 line receivers or an Am26LS32 line receiver and up to thirty-two Am26LS29 line drivers with only one enabled at a time and all others in the three-state mode.

The Am26LS29 is constructed using advanced low-power Schottky processing.

LOGIC DIAGRAM

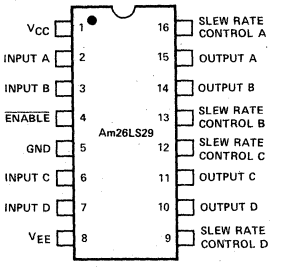


BLI-001

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	−55°C to +125°C	AM26LS29DM
Hermetic Flat Pak	−55°C to +125°C	AM26LS29FM
Dice	−55°C to +125°C	AM26LS29XM
Hermetic DIP	0°C to +70°C	AM26LS29DC
Molded DIP	0°C to +70°C	AM26LS29PC
Dice	0°C to +70°C	AM26LS29XC

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

BLI-004

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Supply Voltage	
V+	7.0V
V−	−7.0V
Power Dissipation	600mW
Input Voltage	−0.5 to +15.0V
Output Voltage (Power Off)	±15V
Lead Soldering Temperature (10 seconds)	300°C

ELECTRICAL CHARACTERISTICS over the operating temperature range

The following conditions apply unless otherwise specified:

Am26LS29XM (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V +10, -5\%, V_{EE} = -5.0V -10, +5\%$
Am26LS29XC (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%, V_{EE} = -5.0V \pm 5\%$

DC CHARACTERISTICS over the operating temperature range (Notes 1 and 2)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_O	Output Voltage	$R_L = \infty$ (Note 3)	$V_{IN} = 2.4V$	4.0	4.4	6.0	Volts
$\overline{V_O}$			$V_{IN} = 0.4V$	−4.0	−4.4	−6.0	Volts
V_T	Output Voltage	$R_L = 450\Omega$	$V_{IN} = 2.4V$	3.6	4.1		Volts
$\overline{V_T}$			$V_{IN} = 0.4V$	−3.6	−4.1		Volts
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Output Unbalance	$\lvert V_{CC} \rvert = \lvert V_{EE} \rvert$, $R_L = 450\Omega$			0.02	0.4	Volts
I_{X+}	Output Leakage Power Off	$V_{CC} = V_{EE} = 0V$	$V_O = 10V$		2.0	100	μA
I_{X-}			$V_O = -10V$		−2.0	−100	μA
I_{S+}	Output Short Circuit Current	$V_O = 0V$	$V_{IN} = 2.4V$		−70	−150	mA
I_{S-}			$V_{IN} = 0.4V$		60	150	mA
I_{Slew}	Slew Control Current	$V_{SLEW} = V_{EE} + 0.9V$			±110		μA
I_{CC}	Positive Supply Current	$V_{IN} = 0.4V$, $R_L = \infty$			18	30	mA
I_{EE}	Negative Supply Current	$V_{IN} = 0.4V$, $R_L = \infty$			−10	−22	mA
I_O	Off State (High Impedance) Output Current	V_{CC} = MAX.	$V_O = 10V$		2.0	100	μA
			$V_O = -10V$		−2.0	−100	μA
V_{IH}	High Level Input Voltage			2.0			Volts
V_{IL}	Low Level Input Voltage					0.8	Volts
I_{IH}	High Level Input Current	$V_{IN} = 2.4V$			1.0	40	μA
		$V_{IN} \leq 15V$			10	100	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0.4V$			−30	−200	μA
V_I	Input Clamp Voltage	$I_{IN} = -12mA$				−1.5	Volts

Notes: 1. Typical limits are at $V_{CC} = 5.0V$, $V_{EE} = -5.0V$, 25°C ambient and maximum loading.
2. Symbols and definitions correspond to EIA RS-423 where applicable.
3. Output voltage is +3.9V minimum and −3.9V minimum at −55°C.

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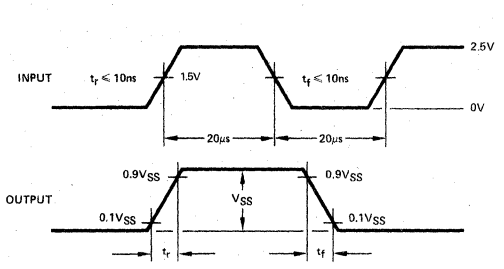
AC CHARACTERISTICS

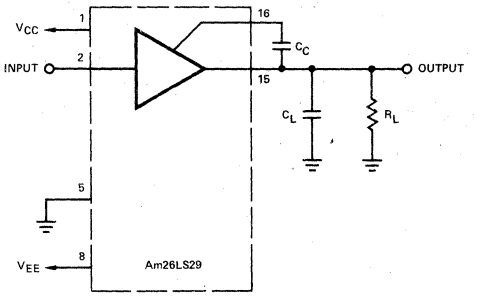
$V_{CC} = 5.0V$, $V_{EE} = -5.0V$, $T_A = 25°C$

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
t_r	Rise Time	$R_L = 450\Omega$, $C_L = 500pF$, Fig. 1	$C_C = 50pF$		3.0		μs
			$C_C = 0pF$		120	300	ns
t_f	Fall Time	$R_L = 450\Omega$, $C_L = 500pF$, Fig. 1	$C_C = 50pF$		3.0		μs
			$C_C = 0pF$		120	300	ns
Src	Slew Rate Coefficient	$R_L = 450\Omega$, $C_L = 500pF$, Fig. 1			.06		μs/pF
t_{LZ}	Output Enable to Output	$R_L = 450\Omega$, $C_L = 500pF$, $C_C = 0pF$, Fig. 2			180	300	ns
t_{HZ}					250	350	
t_{ZL}		$R_L = 450\Omega$, $C_L = 500pF$, $C_C = 0pF$, Fig. 2			250	350	
t_{ZH}					180	300	

SWITCHING TIME WAVEFORMS AND AC TEST CIRCUITS

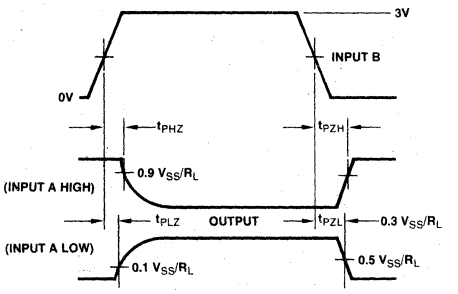


BLI-006

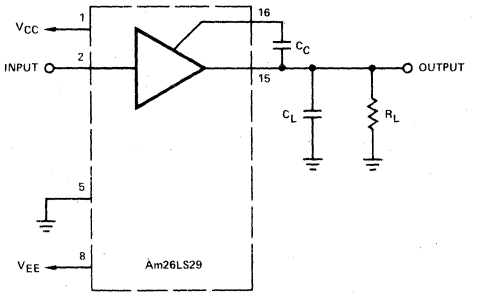


BLI-007

Figure 1. Rise Time Control.



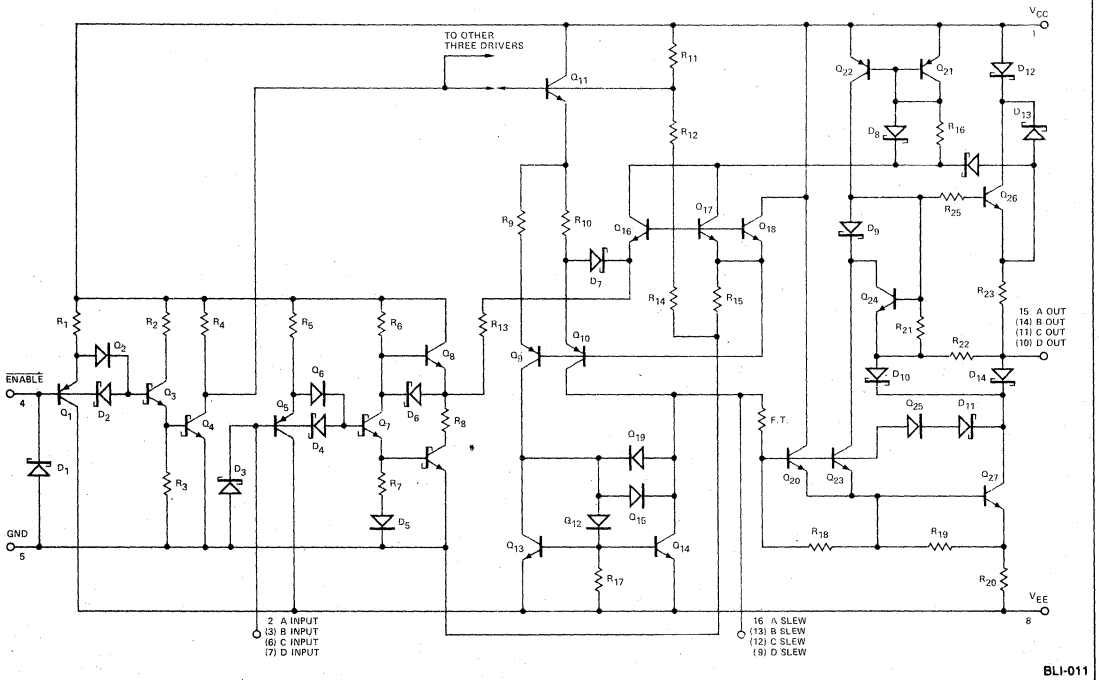
LIC-329



BLI-007

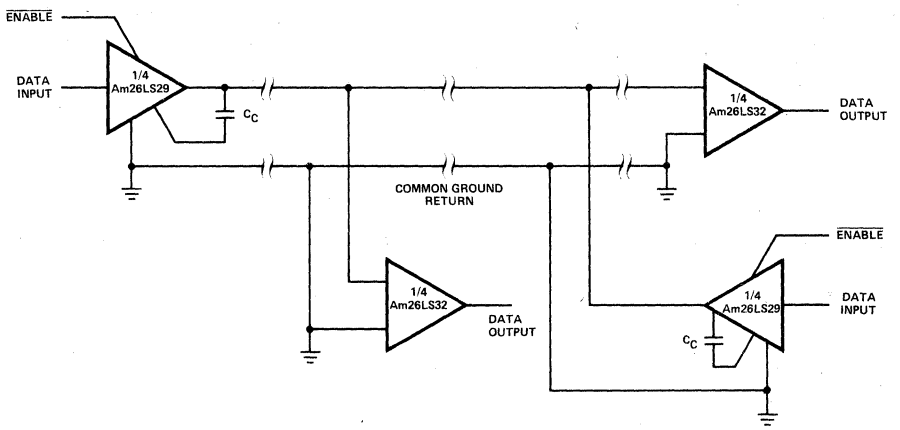
Figure 2. Three State Delays.

Am26LS29 EQUIVALENT CIRCUIT



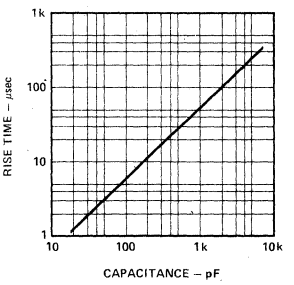
BLI-011

TYPICAL APPLICATION



BLI-012

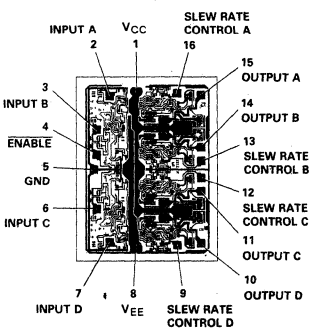
Slew Rate (Rise or Fall Time) Versus External Capacitor



BLI-010

10

Metallization and Pad Layout



DIE SIZE 0.070" X 0.094"

Am26LS30

Dual Differential RS-422 Party Line/Quad Single Ended RS-423 Line Driver

DISTINCTIVE CHARACTERISTICS

- Dual RS-422 line driver or quad RS-423 line driver
- Driver outputs do not clamp line with power off or in hi-impedance state
- Individually three-state drivers when used in differential mode
- Low I_{CC} and I_{EE} power consumption
  - RS-422 differential mode 35mW/driver typ.
  - RS-423 single-ended mode 26mW/driver typ.
- Individual slew rate control for each output
- 50Ω transmission line drive capability (RS-422 into virtual ground)
- Low current PNP inputs compatible with TTL, MOS and CMOS
- High capacitive load drive capability
- Exact replacement for DS16/3691
- Advanced low power Schottky processing

FUNCTIONAL DESCRIPTION

The Am26LS30 is a line driver designed for digital data transmission. A mode control input provides a choice of operation either as two differential line drivers which meet all of the requirements of EIA Standard RS-422 or four independent single-ended RS-423 line drivers.

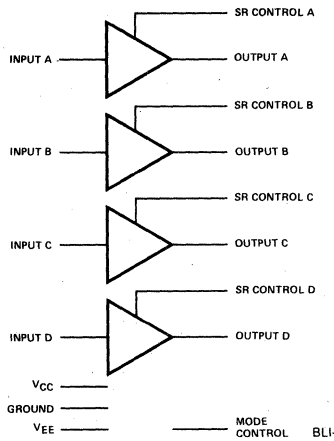
In the differential mode the outputs have individual three-state controls. In the hi-impedance state these outputs will not clamp the line over a common mode transmission line voltage of ±10V. A typical full duplex system would be the Am26LS30 differential line driver and up to twelve Am26LS32 line receivers or an Am26LS32 line receiver and up to thirty-two Am26LS30 differential drivers.

A slew rate control pin allows the use of an external capacitor to control slew rate for suppression of near end cross talk to receivers in the cable.

The Am26LS30 is constructed using Advanced Low Power Schottky processing.

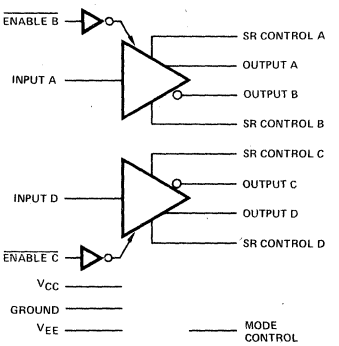
LOGIC DIAGRAMS

Logic for Am26LS30 with Mode Control HIGH (RS-423)



BLI-002

Logic for Am26LS30 with Mode Control LOW (RS-422)

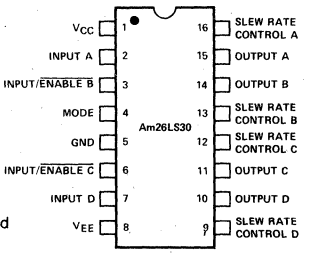


BLI-003

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	−55°C to +125°C	AM26LS30DM
Hermetic Flat Pak	−55°C to +125°C	AM26LS30FM
Dice	−55°C to +125°C	AM26LS30XM
Hermetic DIP	0°C to +70°C	AM26LS30DC
Molded DIP	0°C to +70°C	AM26LS30PC
Dice	0°C to +70°C	AM26LS30XC

CONNECTION DIAGRAM – Top View



Note:
Pin 1 is marked for orientation.

BLI-005

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Supply Voltage	
V+	7.0V
V−	−7.0V
Power Dissipation	600mW
Input Voltage	−0.5 to +15.0V
Output Voltage (Power Off)	±15V
Lead Soldering Temperature (10 seconds)	300°C

ELECTRICAL CHARACTERISTICS over the operating temperature range

The Following Conditions Apply Unless Otherwise Specified:

Am26LS30XM (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$, $V_{EE} = GND$
Am26LS30XC (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$, $V_{EE} = GND$
EIA RS-422 Connection, Mode Voltage = 0.8V

DC CHARACTERISTICS over the operating temperature range

Parameters	Description	Test Conditions (Note 3)		Min.	Typ. (Note 1)	Max.	Units
V_O	Differential Output Voltage, $V_{A, B}$	$R_L = \infty$	$V_{IN} = 2.0V$		3.6	6.0	Volts
$\overline{V_O}$			$V_{IN} = 0.8V$		−3.6	−6.0	Volts
V_T	Differential Output Voltage, $V_{A, B}$	$R_L = 100\Omega$	$V_{IN} = 2.0V$	2.0	2.4		Volts
$\overline{V_T}$			$V_{IN} = 0.8V$	−2.0	−2.4		Volts
V_{OS}, $\overline{V_{OS}}$	Common Mode Offset Voltage	$R_L = 100\Omega$			2.5	3.0	Volts
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Difference in Differential Output Voltage	$R_L = 100\Omega$			0.005	0.4	Volts
$\lvert V_{OS} \rvert - \lvert \overline{V_{OS}} \rvert$	Difference in Common Mode Offset Voltage	$R_L = 100\Omega$			0.005	0.4	Volts
V_{SS}	$\lvert V_T - \overline{V_T} \rvert$	$R_L = 100\Omega$		4.0	4.8		Volts
V_{CMR}	Output Voltage Common Mode Range	$V_{\overline{ENABLE}} = 2.4V$		±10			Volts
I_{XA}	Output Leakage Current	$V_{CC} = 0V$	$V_{CMR} = 10V$			100	μA
I_{XB}			$V_{CMR} = -10V$			−100	μA
I_{OX}	Off State (High Impedance) Output Current	$V_{CC} = MAX.$	$V_{CMR} \leq 10V$			100	μA
			$V_{CMR} \geq -10V$			−100	μA
I_{SA}, I_{SB}	Output Short Circuit Current	$V_{IN} = 2.4V$	$V_{OA} = 6.0V$		80	150	mA
			$V_{OB} = 0V$		−80	−150	mA
		$V_{IN} = 0.4V$	$V_{OA} = 0V$		−80	−150	mA
			$V_{OB} = 6.0V$		80	150	mA
I_{CC}	Supply Current				18	30	mA
V_{IH}	High Level Input Voltage			2.0			Volts
V_{IL}	Low Level Input Voltage					0.8	Volts
I_{IH}	High Level Input Current	$V_{IN} = 2.4V$			1.0	40	μA
		$V_{IN} \leq 15V$			10	100	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0.4V$			−30	−200	μA
V_I	Input Clamp Voltage	$I_{IN} = -12mA$				−1.5	Volts

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AC CHARACTERISTICS

EIA RS-422 Connection, $V_{CC} = 5.0V$, $V_{EE} = GND$, Mode = 0.4V, $T_A = 25°C$

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
t_r	Differential Output Rise Time	Fig. 2, $R_L = 100\Omega$, $C_L = 500pF$		120	200	ns
t_f	Differential Output Fall Time	Fig. 2, $R_L = 100\Omega$, $C_L = 500pF$		120	200	ns
t_{PDH}	Output Propagation Delay	Fig. 2, $R_L = 100\Omega$, $C_L = 500pF$		120	200	ns
t_{PDL}	Output Propagation Delay	Fig. 2, $R_L = 100\Omega$, $C_L = 500pF$		120	200	ns
t_{LZ}	Output Enable to Output	$R_L = 450\Omega$, $C_L = 500pF$, $C_C = 0pF$, Fig. 3		180	300	ns
t_{HZ}				250	350	
t_{ZL}		$R_L = 450\Omega$, $C_L = 500pF$, $C_C = 0pF$, Fig. 3		250	350	
t_{ZH}				180	300	

Notes: 1. Typical limits are at $V_{CC} = 5.0V$, $V_{EE} = GND$, 25°C ambient and maximum loading.
2. Symbols and definitions correspond to EIA RS-422 where applicable.
3. R_L connected between each output and its complement.

Am26LS30

ELECTRICAL CHARACTERISTICS over the operating temperature range

The following conditions apply unless otherwise specified:

Am26LS30XM (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$, $V_{EE} = -5.0V \pm 10\%$
Am26LS30XC (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$, $V_{EE} = -5.0V \pm 5\%$
RS-423 Connection, Mode Voltage $\geq 2.0V$

DC CHARACTERISTICS over the operating temperature range (Notes 1 and 2)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_O	Output Voltage	$R_L = \infty$, (Note 3)	$V_{IN} = 2.4V$	4.0	4.4	6.0	Volts
$\overline{V_O}$		$\lvert V_{CC}\rvert = \lvert V_{EE}\rvert = 4.75V$	$V_{IN} = 0.4V$	−4.0	−4.4	−6.0	Volts
V_T	Output Voltage	$R_L = 450\Omega$,	$V_{IN} = 2.4V$	3.6	4.1		Volts
$\overline{V_T}$		$\lvert V_{CC}\rvert = \lvert V_{EE}\rvert = 4.75V$	$V_{IN} = 0.4V$	−3.6	−4.1		Volts
$\lvert V_T\rvert - \lvert\overline{V_T}\rvert$	Output Unbalance	$\lvert V_{CC}\rvert = \lvert V_{EE}\rvert$, $R_L = 450\Omega$			0.02	0.4	Volts
I_{X+}	Output Leakage Power Off	$V_{CC} = V_{EE} = 0V$	$V_O = 6.0V$		2.0	100	μA
I_{X-}			$V_O = -6.0V$		−2.0	−100	μA
I_{S+}	Output Short Circuit Current	$V_O = 0V$	$V_{IN} = 2.4V$		−80	−150	mA
I_{S-}			$V_{IN} = 0.4V$		80	150	mA
I_{Slew}	Slew Control Current	$V_{SLEW} = V_{EE} + 0.9V$			±140		μA
I_{CC}	Positive Supply Current	$V_{IN} = 0.4V$, $R_L = \infty$			18	30	mA
I_{EE}	Negative Supply Current	$V_{IN} = 0.4V$, $R_L = \infty$			−10	−22	mA
V_{IH}	High Level Input Voltage			2.0			Volts
V_{IL}	Low Level Input Voltage					0.8	Volts
I_{IH}	High Level Input Current	$V_{IN} = 2.4V$			1.0	40	μA
		$V_{IN} \leq 15V$			10	100	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0.4V$			−30	−200	μA
V_I	Input Clamp Voltage	$I_{IN} = -12mA$				−1.5	Volts

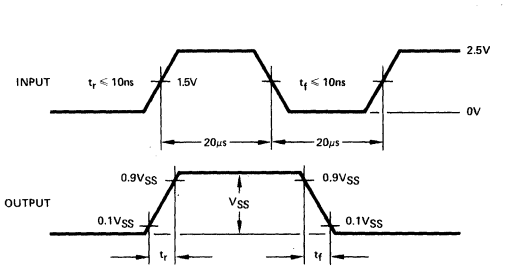
Notes: 1. Typical limits are at $V_{CC} = 5.0V$, $V_{EE} = -5.0V$, 25°C ambient and maximum loading.
2. Symbols and definitions correspond to EIA RS-423 where applicable.
3. Output voltage is +3.9V minimum and −3.9V minimum at −55°C.

AC CHARACTERISTICS

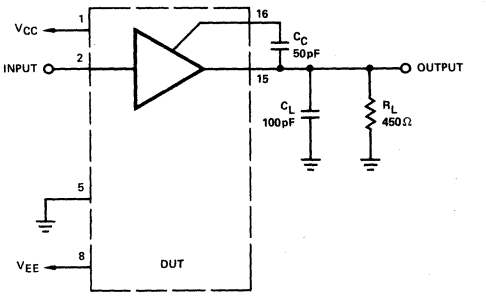
RS-423 Connection, $V_{CC} = 5.0V$, $V_{EE} = -5.0V$, Mode = 2.4V, $T_A = 25°C$

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
t_r	Rise Time	Fig. 1, $R_L = 450\Omega$, $C_L = 500pF$	$C_C = 50pF$		3.0		μs
			$C_C = 0$		120	300	ns
t_f	Fall Time	Fig. 1, $R_L = 450\Omega$, $C_L = 500pF$	$C_C = 50pF$		3.0		μs
			$C_C = 0$		120	300	ns
Src	Slew Rate Coefficient	Fig. 1, $R_L = 450\Omega$, $C_L = 500pF$			.06		μs/pF
t_{PDH}	Output Propagation Delay	Fig. 1, $R_L = 450\Omega$, $C_L = 500pF$, $C_C = 0$			180	300	ns
t_{PDL}	Output Propagation Delay	Fig. 1, $R_L = 450\Omega$, $C_L = 500pF$, $C_C = 0$			180	300	ns

SWITCHING TIME WAVEFORMS AND AC TEST CIRCUITS FOR EIA RS-423 CONNECTION



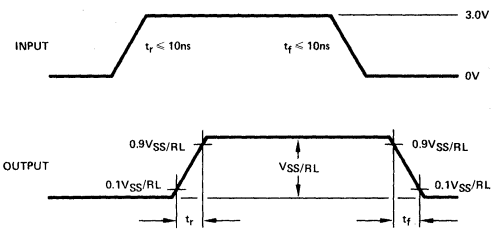
BLI-006



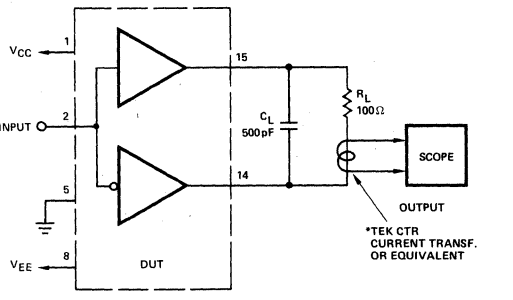
BLI-007

Figure 1. Rise Time Control for RS-423.

SWITCHING TIME WAVEFORMS AND AC TEST CIRCUIT FOR RS-422 CONNECTION



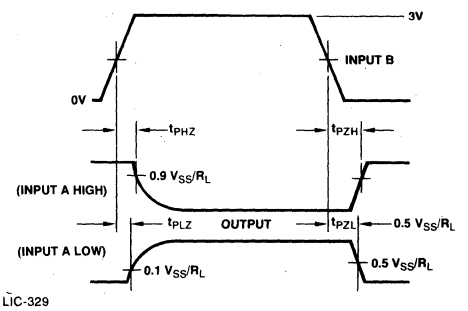
BLI-008



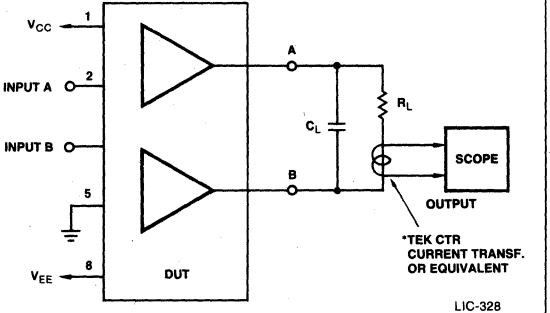
BLI-009

*Current probe is the easiest way to display a differential waveform.

Figure 2.



LIC-329



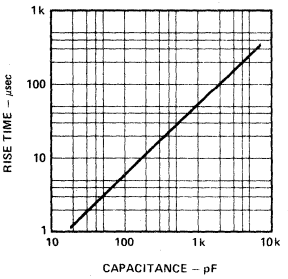
LIC-328

Figure 3. Three-State Delays.

Am26LS30 FUNCTION TABLE

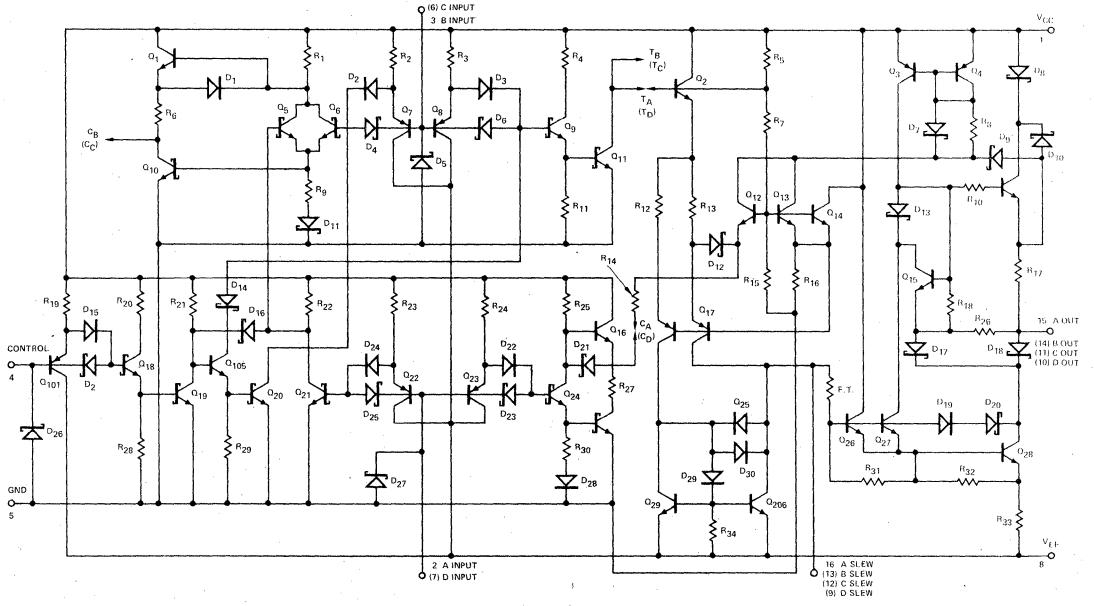
MODE	INPUTS		OUTPUTS	
	A(D)	B(C)	A(D)	B(C)
0	0	0	0	1
0	0	1	Z	Z
0	1	0	1	0
0	1	1	Z	Z
1	0	0	0	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

Slew Rate (Rise or Fall Time) Versus External Capacitor



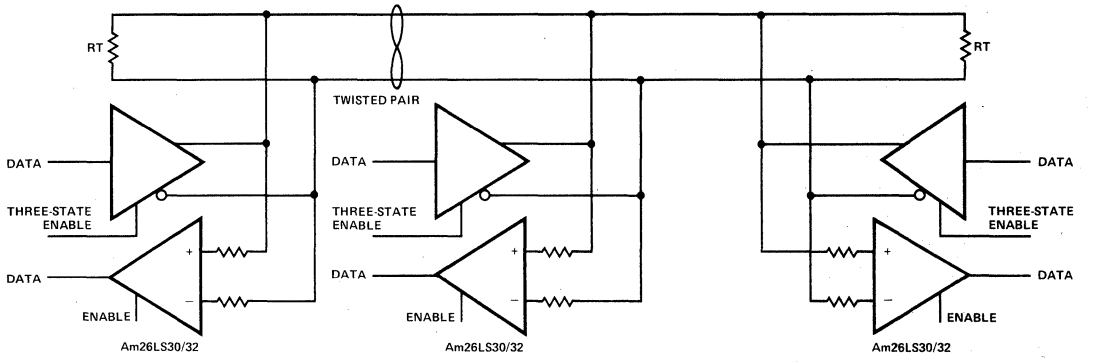
BLI-010

Am26LS30 EQUIVALENT CIRCUIT



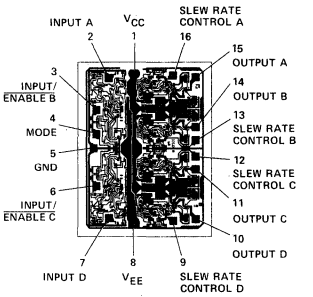
BLI-020

TYPICAL APPLICATION



BLI-032

Metallization and Pad Layout



DIE SIZE 0.070" X 0.094"

10

Am26LS31

Quad High Speed Differential Line Driver

DISTINCTIVE CHARACTERISTICS

- Output skew – 2.0ns typical
- Input to output delay – 12ns
- Operation from single +5V supply
- 16-pin hermetic and molded DIP package
- Outputs won't load line when $V_{CC} = 0$
- Four line drivers in one package for maximum package density
- Output short-circuit protection
- Complementary outputs
- Meets the requirements of EIA standard RS-422
- High output drive capability for 100Ω terminated transmission lines
- Available in military and commercial temperature range
- Advanced low-power Schottky processing

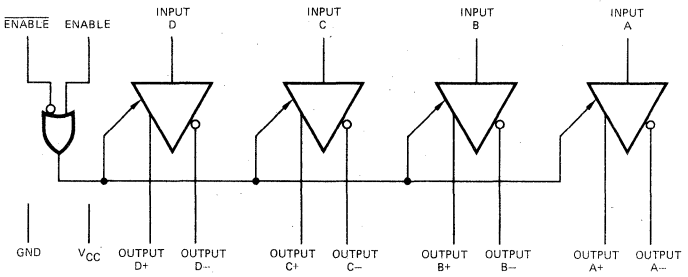
FUNCTIONAL DESCRIPTION

The Am26LS31 is a quad differential line driver, designed for digital data transmission over balanced lines. The Am26LS31 meets all the requirements of EIA standard RS-422 and federal standard 1020. Is is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

The circuit provides an enable and disable function common to all four drivers. The Am26LS31 features 3-state outputs and logical OR-ed complementary enable inputs. The inputs are all LS compatible and are all one unit load.

The Am26LS31 is constructed using advanced low-power Schottky processing.

LOGIC DIAGRAM

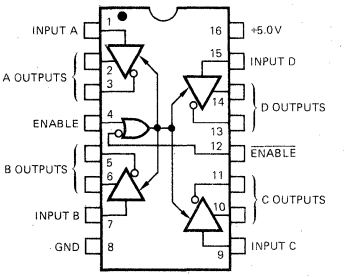


LIC-352

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	–55°C to +125°C	AM26LS31DM
Flat Pak	–55°C to +125°C	AM26LS31FM
Dice	–55°C to +125°C	AM26LS31XM
Hermetic DIP	0°C to +70°C	AM26LS31DC
Molded DIP	0°C to +70°C	AM26LS31PC
Dice	0°C to +70°C	AM26LS31XC

CONNECTION DIAGRAM
(Top View)



Note: Pin 1 is marked for orientation.

LIC-353

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Supply Voltage	7.0V
Input Voltage	7.0V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C

ELECTRICAL CHARACTERISTICS over the operating temperature range

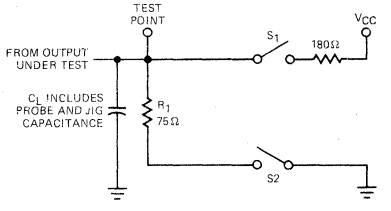
The following conditions apply unless otherwise specified:

Am26LS31XM (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5V \pm 10\%$
Am26LS31XC (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 5\%$

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −20mA		2.5	3.2		Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 20mA			0.32	0.5	Volts
V_{IH}	Input HIGH Voltage	V_{CC} = Min.		2.0			Volts
V_{IL}	Input LOW Voltage	V_{CC} = Max.				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.4V			−0.20	−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7V			0.5	20	μA
I_I	Input Reverse Current	V_{CC} = Max., V_{IN} = 7.0V			0.001	0.1	mA
I_O	Off-State (High Impedance) Output Current	V_{CC} = Max.	V_O = 2.5V		0.5	20	μA
			V_O = 0.5V		0.5	−20	
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = 18mA			−0.8	−1.5	Volts
I_{SC}	Output Short Circuit Current	V_{CC} = Max.		−30	−60	−150	mA
I_{CC}	Power Supply Current	V_{CC} = Max., all outputs disabled			60	80	mA
t_{PLH}	Input to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			12	20	ns
t_{PHL}	Input to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			12	20	ns
SKEW	Output to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			2.0	6.0	ns
t_{LZ}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, C_L = 10pF			23	35	ns
t_{HZ}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, C_L = 10pF			17	30	ns
t_{ZL}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			35	45	ns
t_{ZH}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 2			30	40	ns

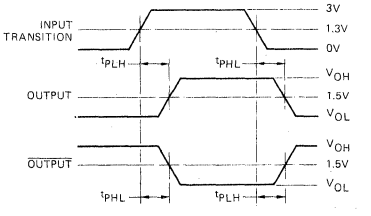
Notes: 1. All typical values are V_{CC} = 5.0V, T_A = 25°C.
2. C_L = 30pF, V_{IN} = 1.3V to V_{OUT} = 1.3V, V_{PULSE} = 0V to +3.0V, See Below.

AC LOAD TEST CIRCUIT FOR THREE-STATE OUTPUTS



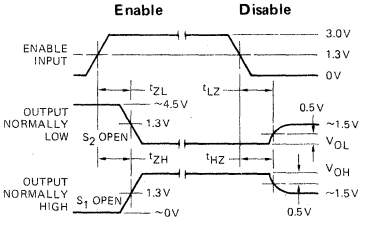
LIC-354

PROPAGATION DELAY (Notes 1 and 3)



LIC-355

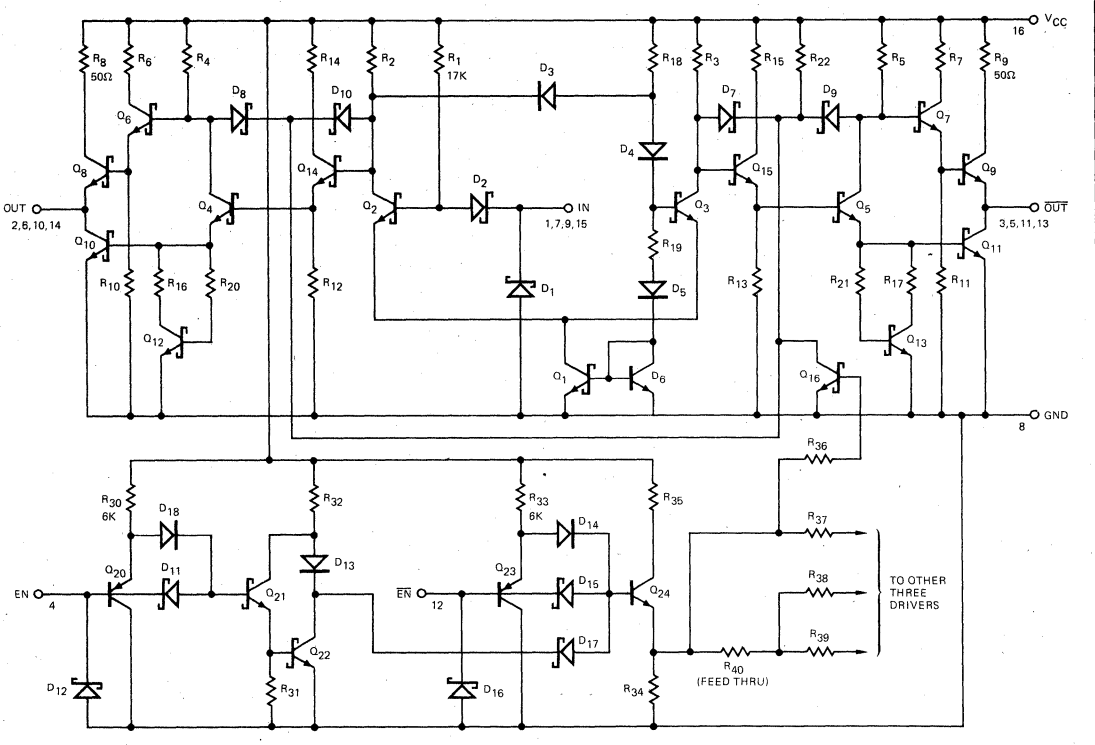
ENABLE AND DISABLE TIMES (Notes 2 and 3)



LIC-356

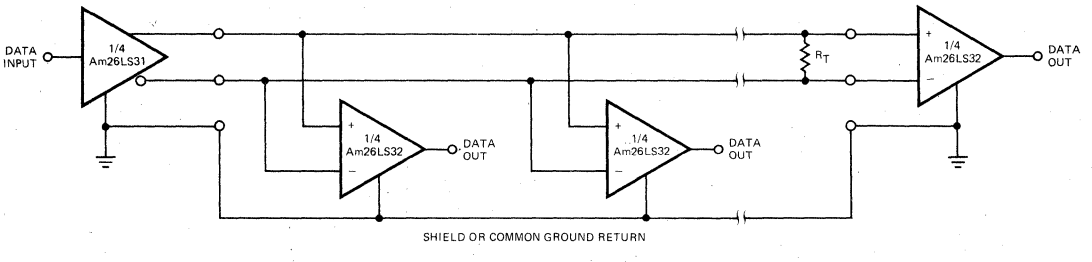
Notes: 1. Diagram shown for $\overline{\text{Enable}}$ LOW.
2. S_1 and S_2 of Load Circuit are closed except where shown.
3. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_o = 50Ω; t_r ≤ 15ns; t_f ≤ 6.0ns.

EQUIVALENT CIRCUIT (1/4 Am26LS31)



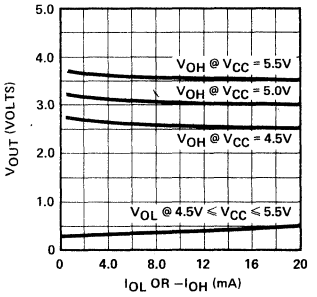
BLI-023

TYPICAL APPLICATION



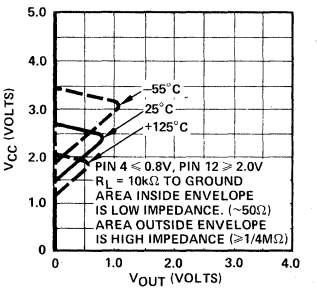
LIC-357

Guaranteed V_{OH} and V_{OL} (T_A = –55°C to +125°C)



LIC-358

V_{OUT} Versus V_{CC}



LIC-359

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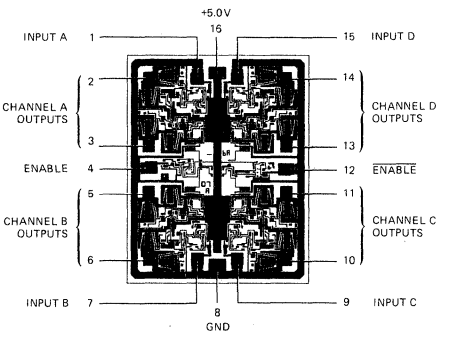
Metallization and Pad Layout



DIE SIZE 0.067" X 0.084"

Am26LS32 • Am26LS33

Quad Differential Line Receivers

DISTINCTIVE CHARACTERISTICS

- Input voltage range of 15V (differential or common mode) on Am26LS33; 7V (differential or common mode) on Am26LS32
- ±0.2V sensitivity over the input voltage range on Am26LS32; ±0.5V sensitivity on Am26LS33
- The Am26LS32 meets all the requirements of RS-422 and RS-423
- 6k minimum input impedance
- 30mV input hysteresis
- Operation from single +5V supply
- 16-pin hermetic and molded DIP package
- Fail safe input-output relationship. Output always high when inputs are open.
- Three-state drive, with choice of complementary output enables, for receiving directly onto a data bus.
- Propagation delay 17ns typical
- Available in military and commercial temperature range
- Advanced low-power Schottky processing

FUNCTIONAL DESCRIPTION

The Am26LS32 is a quad line receiver designed to meet the requirements of RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

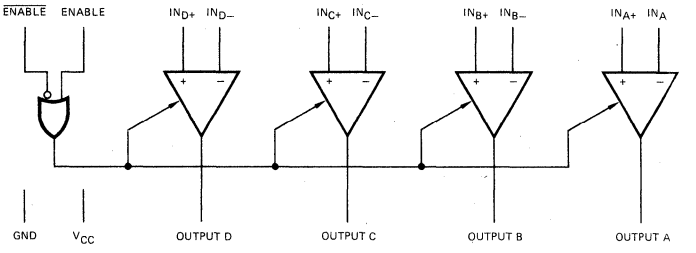
The Am26LS32 features an input sensitivity of 200mV over the input voltage range of ±7V.

The Am26LS33 features an input sensitivity of 500mV over the input voltage range of ±15V.

The Am26LS32 and Am26LS33 provide an enable and disable function common to all four receivers. Both parts feature 3-state outputs with 8mA sink capability and incorporate a fail safe input-output relationship which keeps the outputs high when the inputs are open.

The Am26LS32 and Am26LS33 are constructed using Advanced Low-Power Schottky processing.

LOGIC DIAGRAM

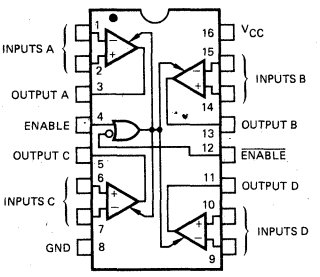


BLI-024

ORDERING INFORMATION

Package Type	Temperature Range	Am26LS32 Order Number	Am26LS33 Order Number
Hermetic DIP	−55°C to +125°C	AM26LS32DM	AM26LS33DM
Flat Pak	−55°C to +125°C	AM26LS32FM	AM26LS33FM
Dice	−55°C to +125°C	AM26LS32XM	AM26LS33XM
Hermetic DIP	0°C to +70°C	AM26LS32DC	AM26LS33DC
Molded DIP	0°C to +70°C	AM26LS32PC	AM26LS33PC
Dice	0°C to +70°C	AM26LS32XC	AM26LS33XC

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LIC-360

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Supply Voltage	7.0V
Common Mode Range	±25V
Differential Input Voltage	±25V
Enable Voltage	7.0V
Output Sink Current	50mA
Storage Temperature Range	−65°C to +165°C

ELECTRICAL CHARACTERISTICS Over the operating temperature range

The following conditions apply unless otherwise specified:

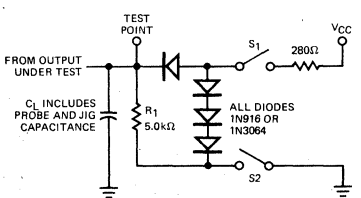
Am26LS32XM, Am26LS33XM (MIL) T_A = −55°C to +125°C V_{CC} = 5.0V ± 10%
Am26LS32XC, Am26LS33XC (COM'L) T_A = 0°C to +70°C V_{CC} = 5.0V ± 5%

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{TH}	Differential Input Voltage	$V_{OUT} = V_{OL}$ or V_{OH}	Am26LS32, −7V ≤ V_{CM} ≤ +7V	−0.2	±0.06	+0.2	Volts
			Am26LS33, −15V ≤ V_{CM} ≤ +15V	−0.5	±0.12	+0.5	
R_{IN}	Input Resistance	−15V ≤ V_{CM} ≤ +15V (One input AC ground)		6.0	9.8		kΩ
I_{IN}	Input Current (Under Test)	V_{IN} = +15V, Other Input −15V ≤ V_{IN} ≤ +15V				2.3	mA
I_{IN}	Input Current (Under Test)	V_{IN} = −15V, Other Input −15V ≤ V_{IN} ≤ +15V				−2.8	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., ΔV_{IN} = +1.0V, $V_{\overline{ENABLE}}$ = 0.8V, I_{OH} = −440μA	COM'L	2.7	3.4		Volts
			MIL	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min., ΔV_{IN} = −1.0V, $V_{\overline{ENABLE}}$ = 0.8V	I_{OL} = 4.0mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
V_{IL}	Enable LOW Voltage					0.8	Volts
V_{IH}	Enable HIGH Voltage			2.0			Volts
V_I	Enable Clamp Voltage	V_{CC} = Min., I_{IN} = −18mA				−1.5	Volts
I_O	Off-State (High Impedance) Output Current	V_{CC} = Max.	V_O = 2.4V			20	μA
			V_O = 0.4V			−20	
I_{IL}	Enable LOW Current	V_{IN} = 0.4V			−0.2	−0.36	mA
I_{IH}	Enable HIGH Current	V_{IN} = 2.7V			0.5	20	μA
I_I	Enable Input High Current	V_{IN} = 5.5V			1	100	μA
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{CC} = Max., ΔV_{IN} = +1.0V		−15	−50	−85	mA
I_{CC}	Power Supply Current	V_{CC} = Max., All V_{IN} = GND, Outputs Disabled			52	70	mA
V_{HYST}	Input Hysteresis	T_A = 25°C, V_{CC} = 5.0V, V_{CM} = 0V			30		mV
t_{PLH}	Input to Output	T_A = 25°C, V_{CC} = 5.0V, C_L = 15pF, see test cond. below			17	25	ns
t_{PHL}	Input to Output	T_A = 25°C, V_{CC} = 5.0V, C_L = 15pF, see test cond. below			17	25	ns
t_{LZ}	Enable to Output	T_A = 25°C, V_{CC} = 5.0V, C_L = 5pF, see test cond. below			20	30	ns
t_{HZ}	Enable to Output	T_A = 25°C, V_{CC} = 5.0V, C_L = 5pF, see test cond. below			15	22	ns
t_{ZL}	Enable to Output	T_A = 25°C, V_{CC} = 5.0V, C_L = 15pF, see test cond. below			15	22	ns
t_{ZH}	Enable to Output	T_A = 25°C, V_{CC} = 5.0V, C_L = 15pF, see test cond. below			15	22	ns

Note: 1. All typical values are V_{CC} = 5.0V, T_A = 25°C.

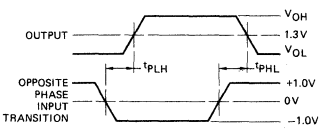
10

LOAD TEST CIRCUIT FOR THREE-STATE OUTPUTS



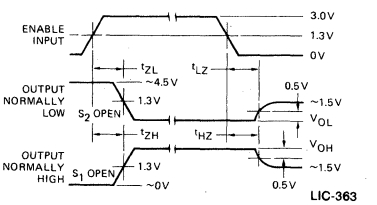
LIC-361

PROPAGATION DELAY (Notes 1 and 3)



LIC-362

ENABLE AND DISABLE TIMES (Notes 2 and 3)



LIC-363

Notes:

1. Diagram shown for $\overline{\text{Enable}}$ LOW.
2. S_1 and S_2 of Load Circuit are closed except where shown.
3. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_o = 50Ω; t_r ≤ 15ns; t_f ≤ 6.0ns.

Am26LS32B

Quad Differential Line Receiver

DISTINCTIVE CHARACTERISTICS

- ± 100mV sensitivity over V_{IN} range of 0V to 5V
- ± 200mV sensitivity over V_{CM} range
- −7V to +12V input voltage range – differential or common mode
- Guaranteed input voltage hysteresis limits
  - 80mV minimum
  - 200mV maximum
- 3V maximum open circuit input voltage
- Three-state outputs disabled during power-up and power down
- Maximum guarantees for t_{PD} skew
- All AC and DC parameters guaranteed over COM'L and MIL operating temperature ranges
- Single +5V supply
- Advanced low-power Schottky processing

FUNCTIONAL DESCRIPTION

The Am26LS32B is a quad line receiver designed to meet the requirements of RS-422 and RS-423, CCITT V.10 and V.11, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

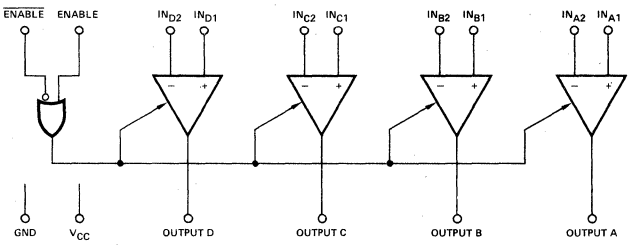
The Am26LS32B features an input sensitivity of 200mV over the common mode input voltage range of −7V to + 12V.

The Am26LS32B is the first device in the Am26LS32 configuration to guarantee minimum hysteresis and propagation delay skew while maintaining better propagation delay guarantees than the Am26LS32. This allows a more critical analysis of performance in high noise environments and better performance in terms of signal quality, resulting in better system performance.

The Am26LS32B provides an enable and disable function common to all four receivers. It features three-state outputs with 24mA sink capability and incorporates a fail safe input-output relationship which keeps the outputs high when the inputs are open.

The Am26LS32B is constructed using Advanced Low-Power Schottky processing.

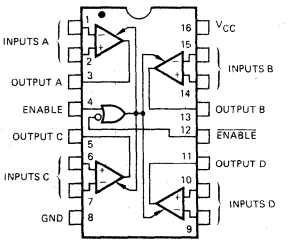
LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Am26LS32B Order Number
Hermetic DIP	−55 to +125°C	AM26LS32BDM
Flat Pak	−55 to +125°C	AM26LS32BFM
Dice	−55 to +125°C	AM26LS32BXM
Hermetic DIP	0 to +70°C	AM26LS32BDC
Molded DIP	0 to +70°C	AM26LS32BPC
Dice	0 to +70°C	AM26LS32BXC

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Supply Voltage	7.0V
Common Mode Range	±25V
Differential Input Voltage	±25V
Enable Voltage	7.0V
Output Sink Current	50mA
Storage Temperature Range	−65 to +165°C

ELECTRICAL CHARACTERISTICS over the operating temperature range

The following conditions apply unless otherwise specified:

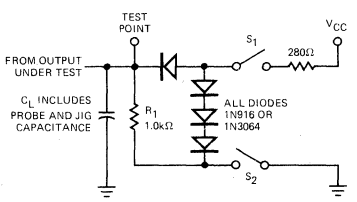
Am26LS32XM (MIL) T_A = −55 to +125°C V_{CC} = 5.0V ± 10%
Am26LS32XC (COM'L) T_A = 0 to +70°C V_{CC} = 5.0V ± 5%

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{TH}	Differential Input Voltage	$V_{OUT} = V_{OL}$ or V_{OH}	$0 \le V_{CM} \le +5V$	−100	±60	100	mV
			$-7V \le V_{CM} \le +12V$	−200		200	
V_{HYST}	Input Hysteresis			80	120	200	mV
V_{IOC}	Open Circuit Input Voltage			2.0		3.0	Volts
R_{IN}	Input Resistance	$-15V \le V_{CM} \le +15V$ (One input AC ground)		6.0	10		kΩ
I_{IN}	Input Current (Under Test)	V_{IN} = +15V, Other Input $-15V \le V_{IN} \le +15V$				2.3	mA
I_{IN}	Input Current (Under Test)	V_{IN} = −15V, Other Input $-15V \le V_{IN} \le +15V$				−2.8	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min, Δ V_{IN} = +1.0V, $V_{\overline{ENABLE}}$ = 0.8V	I_{OH} = −12mA	2.0			Volts
			I_{OH} = −1mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = Min, Δ V_{IN} = −1.0V, $V_{\overline{ENABLE}}$ = 0.8V	I_{OH} = 16mA			0.4	Volts
			I_{OL} = 24mA			0.5	
V_{IL}	Enable LOW Voltage					0.8	Volts
V_{IH}	Enable HIGH Voltage			2.0			Volts
V_I	Enable Clamp Voltage	V_{CC} = Min, I_{IN} = −18mA				−1.5	Volts
I_O	Off-State (High Impedance) Output Current	V_{CC} = Max	V_O = 2.4V			50	μA
			V_O = 0.4V			−50	
I_{IL}	Enable LOW Current	V_{IN} = 0.4V				−0.36	mA
I_{IH}	Enable HIGH Current	V_{IH} = 2.7V				20	μA
I_I	Input HIGH Current	V_{IN} = 5.5V				100	μA
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{CC} = Max, Δ V_{IN} = +1.0V		−30	−65	−120	mA
I_{CC}	Power Supply Current	V_{CC} = Max, All V_{IN} = GND, Outputs Disabled			52	70	mA

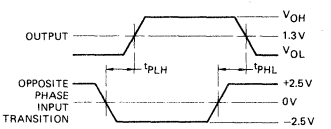
Note: 1. All typical values are V_{CC} = 5.0V, T_A = 25°C.

10

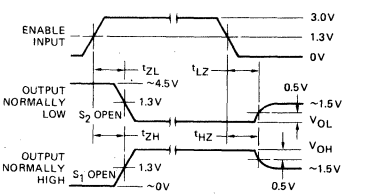
LOAD TEST CIRCUIT FOR THREE-STATE OUTPUTS



PROPAGATION DELAY (Notes 1 and 3)



ENABLE AND DISABLE TIMES (Notes 2 and 3)



Notes: 1. Diagram shown for Enable LOW.
2. S_1 and S_2 of Load Cricuit are closed except where shown.
3. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_o = 50Ω; t_r ≤ 2.5ns; t_f ≤ 2.5ns.

Am26LS32B
SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

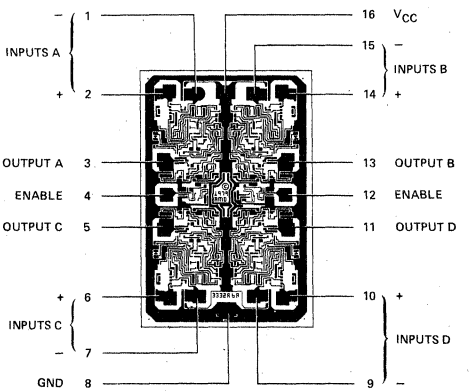
Parameters	Description	Min	Typ	Max	Units	Test Conditions
t_{PLH}	Propagation Delay, Input to Output		16	21	ns	C_L = 50pF See test circuit
t_{PHL}			17	21	ns	
t_{SKEW}	Propagation Delay Skew, $t_{PLH} - t_{PHL}$		1.5	3.0	ns	
t_{ZL}	Output Enable Time, ENABLE to Output		16	22	ns	
t_{ZH}			10	16	ns	
t_{LZ}	Output Disable Time, ENABLE to Output		11	18	ns	C_L = 5pF See test circuit
t_{HZ}			13	18	ns	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Am26LS32B COM'L T_A = 0 to +70°C V_{CC} = 5.0V ± 10% Min	Am26LS32B COM'L Max	Am26LS32B MIL T_A = −55 to +125°C V_{CC} = 5.0V ± 10% Min	Am26LS32B MIL Max	Units	Test Conditions
t_{PLH}	Propagation Delay, Input to Output		26		26	ns	C_L = 50pF See test circuit
t_{PHL}			26		26	ns	
t_{SKEW}	Propagation Delay Skew, $t_{PLH} - t_{PHL}$		4.0		4.0	ns	
t_{ZL}	Output Enable Time, ENABLE to Output		33		33	ns	
t_{ZH}			22		22	ns	
t_{LZ}	Output Disable Time, ENABLE to Output		27		27	ns	C_L = 5pF See test circuit
t_{HZ}			27		27	ns	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.056" X 0.084"

Use of the Am26LS29, 30, 31 and 32 Quad Driver/Receiver Family in EIA RS-422 and 423 Applications

By David A. Laws and Roy J. Levy

INTRODUCTION

Today's high-performance data processing systems demand significantly faster data communications rates than are possible with the EIA RS-232 specifications in use for the past ten years.

Two new standards prepared by the Electronic Industries Association address this need. EIA RS-423 is an unbalanced, bipolar voltage specification designed to interface with RS-232C, while greatly enhancing its operation. It permits the communication of digital information over distances of up to 2000 feet and at data rates of up to 300 Kilobaud. EIA RS-422 is a balanced voltage digital interface for communicaton of digital data over distances of 4000 feet or data rates of up to 10 megabaud.

Advanced Micro Devices has developed a family of monolithic Low-power Schottky quad line drivers and receivers to meet the requirements of these specifications.

The Am26LS29 and 30 line drivers and the Am26LS32 receiver meet all requirements of RS-423 while the Am26LS31 differential line driver and the Am26LS32 receiver meet the requirements of RS-422.

A second receiver element, the Am26LS33 is available for use in high common mode noise environments, exceeding the common mode voltage requirements of RS-422 and RS-423.

This application note reviews the use of these devices in implementing the new standards. Emphasis is given to the EIA RS-422 balanced interface.

EIA STANDARD SPECIFICATIONS

Two basic forms of operation are available for transmission of digital data over interconnecting lines. These are the single ended and differential techniques.

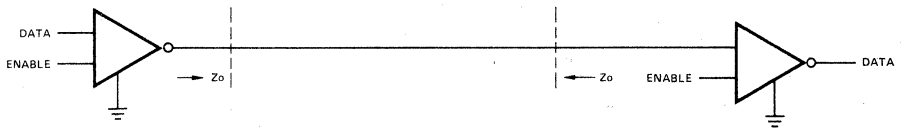
The single-ended form uses a single conductor to carry the signal with the voltage referenced to a single return conductor. This may also be the common return for other signal conductors. Figure 1a.

The single-ended form is the simplest way to send data as it requires only one signal line per circuit. This simplicity, however, is often offset by the inability of this form to allow discrimination between a valid signal produced by the driver, and the sum of the driver signal plus externally induced noise signals.

A solution to some of the problems inherent in the single-ended form of operation is offered by the differential form of operation. Figure 1b. This consists of a differential driver (essentially two single-ended drivers with one driver always producing the complementary output signal level to the other driver), a twisted pair transmission line and a differential line receiver. The driver signal appears as a differential voltage to the line receiver, while the noise signals appear as a common mode signal. The two signals, therefore, can be discriminated by a line receiver with a sufficient common mode voltage operating range.

The Electronic Industries Association, EIA, has defined a number of specifications standardizing the interface between data terminal equipment and data circuit terminating equipment based on both single-ended and differential operation.

a) Single Wire With Common Ground.



b) Two Wire Balanced System.

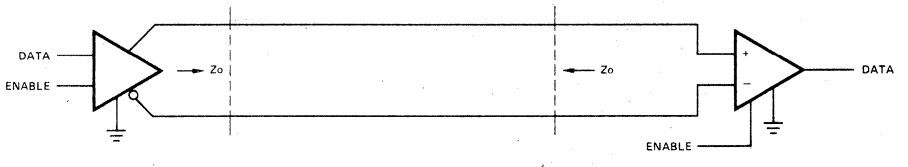


Figure 1. Data Communication Techniques.

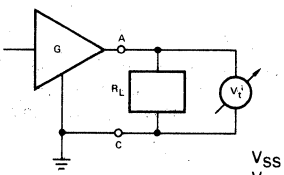
Quad Driver/Receiver Family

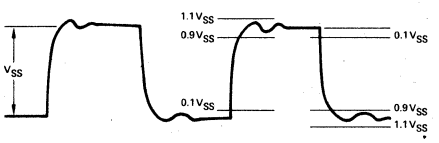
The most widely used standard for interfacing between data terminal equipment and data communications equipment today, is EIA RS-232C, issued in August 1969. The RS-232C electrical interface is a single-ended, bipolar-voltage, unterminated circuit. This specification is for serial binary data interchange over short distances (up to 50 feet) at low rates (up to 20 Kilobaud). It is a protocol standard as well as an electrical standard, specifying hand shaking signals and functions between terminal and the communications equipment. As already noted, single-ended circuits are susceptible to all forms of electromagnetic interference. Noise and cross talk susceptibility are proportional to length and bandwidth. RS-232C places restrictions on both. It limits slew rate of the drivers (30V/μs) to control radiated emission on neighboring circuits and allows bandwidth limiting on the receivers to reduce susceptibility to cross talk. The length and slew rate limits can adequately control reflections on unterminated lines, and the length and bandwidth limits are more than adequate to reduce susceptibility to noise.

Like EIA RS-232C, the new EIA RS-423 is also a single-ended, bipolar-voltage unterminated circuit. It extends the distance and data rate capabilities of this technique to distances of up to 4000 feet at data rates of 3000 baud, or at higher rates of up to 300 Kilobaud over a maximum distance of 40 feet.

EIA RS-422 is a differential, balanced voltage interface capable of significantly higher data rates over longer distances. It can accommodate rates of 100 Kilobaud over a distance of 4000 feet or rates of up to 10 megabaud. These performance improvements stem from the advantages of a balanced configuration which is isolated from ground noise currents. It is also immune to fluctuating voltage potentials between system ground references and to common mode electromagnetic interference. Figure 2 compares the driver output waveforms for the three EIA standard configurations, while Table I compares the key characteristics required by drivers and receivers intended for these applications. Since RS-232C has been in use for many years, RS-422 and 423 parameter values have been selected to facilitate an orderly transition from existing designs to new equipment.

a) EIA RS-232C Generator Output.

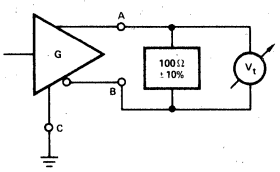


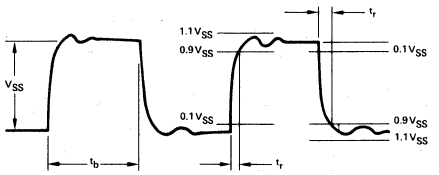


$V_{SS} = |V_t - \overline{V}_t|$
V_{SS} = Difference in steady state voltages
R_L = 3KΩ to 7KΩ
V_{SS} min. = ±5V; V_{SS} max. = ±25V

BLI-015

b) EIA RS-422 Generator Output.



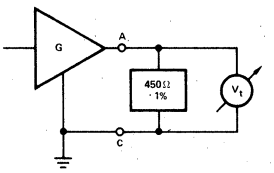


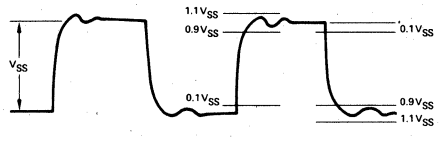
t_D = Time duration of the unit interval at the applicable modulation rate
$t_r \leq 0.1t_D$ when $t_D \geq 200ns$
$t_r \leq 20ns$ when $t_D < 200ns$

V_{SS} = Difference in steady state voltages
$V_{SS} = |V_t - \overline{V}_t|$
V_{SS} min. = 2V; V_{SS} max. = 6V

BLI-016

c) EIA RS-423 Generator Output.





$V_{SS} = |V_t - \overline{V}_t|$
V_{SS} = Difference in steady state voltages
V_{SS} min. = ±3.6V; V_{SS} max. = ±6V

BLI-017

Figure 2. Driver Output Waveforms.

TABLE I
KEY PARAMETERS OF EIA SPECIFICATIONS

Characteristics	EIA RS-232C	EIA RS-423	EIA RS-422	Units
Form of Operation	Single Ended	Single Ended	Differential	
Max. cable length	50	2000	4000	Feet
Max. data rate	20K	300K	10M	Baud
Driver output voltage, open circuit*	±25	±6	6 volts between outputs	Volts (Max.)
Driver output voltage, Loaded output*	±5 to ±15	±3.6	2 volts between outputs	Volts (Min.)
Driver output resistance power off	Ro = 300Ω	100μA between −6 to +6V	100μA between +6 and −.25V	Min.
Driver output short circuit current I_{SC}	±500	±150	±150	mA (Max.)
Driver output slew rate	30 V/μsec Max.	Slew rate must be controlled based upon cable length and modulation rate	No control necessary	
Receiver input resistance R_{in}	3K to 7K	≥4K	≥4K	Ω
Receiver input thresholds	−3 to +3	−0.2 to +0.2	−0.2 to +0.2	Volts (Max.)
Receiver input voltage	−25 to +25	−12 to +12	−12 to +12	Volts (Max.)

*± indicates polarity switched output.

INTEGRATED CIRCUIT CHARACTERISTICS

Most semiconductor manufacturers offer integrated circuits designed to satisfy the old RS-232C standard. A number of them have designs in progress to meet the new EIA specifications. Products available from Advanced Micro Devices to meet these needs are shown in Table II.

The Am26LS29, 30, 31 and 32 are a family of quad drivers and receivers designed specifically to meet the new EIA standards. These products utilize Low-Power Schottky technology to incorporate four drivers or four receivers, together with control logic, in the standard 16-pin package outlines.

The Am26LS29/30 and the Am26LS32 are driver and receiver pairs designed to implement the single-ended EIA RS-423 standard. The Am26LS31 is a differential line driver designed for use with the Am26LS32 receiver in a differential mode to meet EIA RS-422.

Am26LS29 AND Am26LS30 QUAD RS-423 LINE DRIVERS

The Am26LS29 and 30 consist of four single-ended line drivers designed to meet or exceed the requirements of RS-423. The buffered driver outputs are provided with sufficient source and sink current capability to drive 50 ohm to a virtual ground transmission line and high capacitive loads. The Am26LS29 has a three-state output control while the Am26LS30 has a Mode Control input that allows it to operate as a dual RS-422 driver (with suitable power supply changes), Figure 3.

Each of the four driver inputs, as well as the $\overline{\text{Enable}}$/Mode Control input is a PNP Low-Power Schottky input for reduced input loading, one-half the normal fan-in. Since there are two inverters from each input to output, the driver is non-inverting. When operating in the RS-423 mode, the Am26LS29 and 30 require both +5V and −5V nominal value power supplies. This allows the outputs to swing symmetrically about ground – producing a true bipolar output. The Mode Control (Pin 4) of the Am26LS30 should be HI or tied to

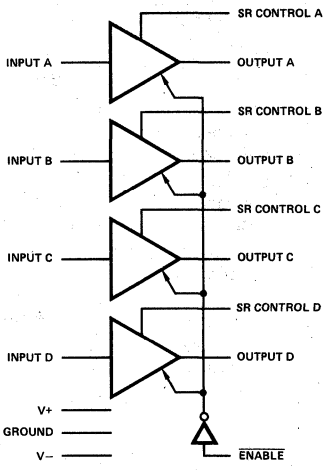
TABLE II
ADVANCED MICRO DEVICES' EIA COMPATIBLE DEVICES

EIA Standard	Drivers	Receivers
RS-232C	Am1488 Quad Driver	Am1489, 1489A Quad Receivers with response control pin
	Am9616 Triple Driver with logic control	Am9617 Triple Receiver with optional hysteresis
	Am2616 Quad Driver also specified for CCITT V.24 and MIL-188C	Am2617 Quad Receiver specified over MIL range
RS-422	Am26LS31 Quad Differential with three-state control gating	Am26LS32 Quad Differential Driver single-ended Receiver
RS-423	Am26LS29 Quad Driver with three-state output Am26LS30 Quad Driver with slew rate control	Am26LS32 Quad single-ended/ Differential Receiver

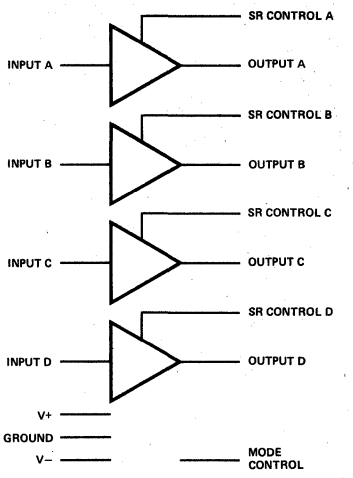
10

a) Logic Diagrams

Am26LS29



Am26LS30
RS-423 Operation (Mode Control HIGH)



b) Circuit Diagram for Am26LS30

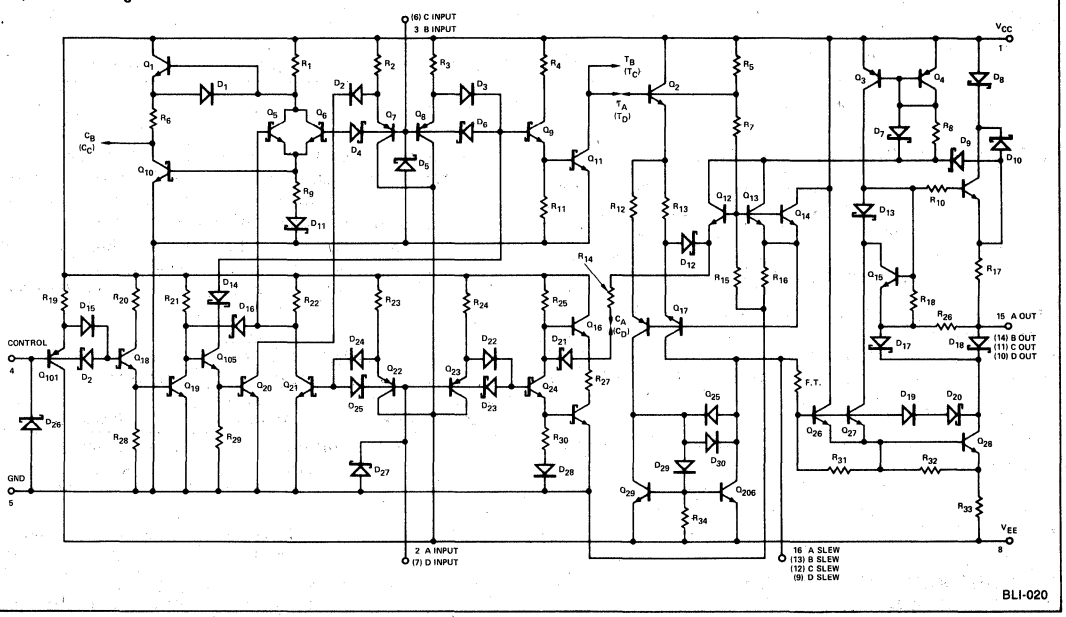


Figure 3. Am26LS29 and Am26LS30 Drivers.

V_{CC}. Each output is designed to drive the RS-423 load of 50 ohms with an output voltage equal or greater than +3.6 volts in the HI state and −3.6 volts in the LO state. Each output is current limited to 150mA max. in either logic state. A Slew Rate control pin is brought out separately for each output to allow output ramp rate (rise and fall time) control. This provides suppression of near end cross talk to other receivers in the cable. Connecting a capacitor from this node to that driver's respective output will produce a ramp (10% to 90%) of 50ns typical for each picofarad of capacitance in that capacitor. RS-423 establishes recommended ramp rates versus length of line driven and modulation rate, Figure 4.

The Am26LS30 can be used at low data rates as a dual EIA RS-422 driver with three-state outputs by connecting the V_{EE} supply and the mode control input to ground.

Am26LS31 QUAD RS-422 DRIVER

The Am26LS31 is a quad differential line driver designed to meet the RS-422 specification while operating with a single +5 volt supply. A common enable and disable function controls all four drivers, Figure 5. The driver features high speed, de-skewed differential outputs with typical propagation delays of 12ns and residual skew of 2ns. Both differential line outputs are designed for three-state operation to allow two-way half duplex and multiplex, data bus applications.

Table III is a summary of the essential requirements of the RS-422 standard. Section A describes the key characteristics satisfied by the Am26LS31 driver.

The balanced differential line driver consists of two halves, each of which is similar to a Low-power Schottky TTL gate with equal source and sink current capability. The two halves are emitter coupled in a differential input configuration. One side of the input circuit is tied to a fixed TTL bias threshold and the other side is tied to a sink diode in normal DTL/TTL fashion. This configuration offers complementary outputs with very low skew, dependent only upon component matching, a necessity to meet RS-422.

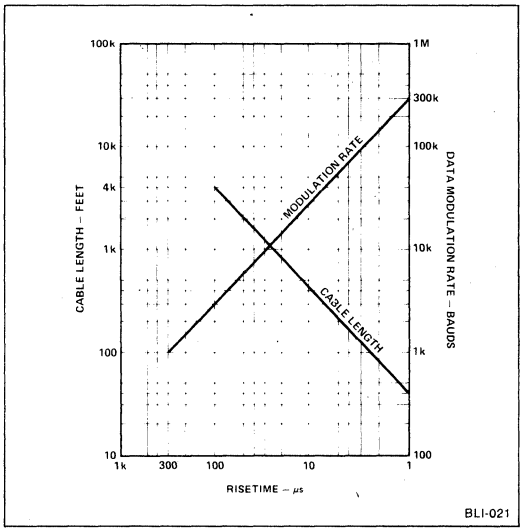


Figure 4. Data Modulation Rate or Cable Length Versus Risetime for EIA RS-423.

The circuit diagram of the driver is shown in Figure 6. The emitter-coupled input circuit is formed by Q2 and Q3, which are biased by a current source. This source is a current mirror, formed by Q1 which supplies the current, and D6 which is diode connected transistor matched to Q1. The fixed bias for Q3, formed by D5 and D6, is $2V_{BE}$. A $2V_{BE}$ bias, less the D2 Schottky diode drop, provides the normal Low-power Schottky TTL threshold, V_{IL} = 0.7V. R19 provides a boost to 0.8V for a full 400mV TTL noise margin. The differential outputs of the emitter coupled stage, A and $\overline{A}$, drive emitter followers Q14 and Q15, which provide the required speed and matching characteristics. The emitter followers, drive phase splitters Q4 and Q5, which in turn drive totem-pole outputs. The outputs at the line interface are of standard Low-power Schottky TTL configuration, except that circuit values are modified to provide high sourcing capability. The outputs are designed to source or sink 20mA each, so that they can generate a voltage of at least 2.0V across a 100 ohm load, as required by RS-422. Additional circuitry has been included to make the line outputs three-state for two-way bus applications. The Am26LS31 meets the RS-422 requirement that the driver not load the line in the powered down condition ($I_X \leq 100\mu A$) or if the power supply to that device should fail.

Am26LS32 QUAD RS-422 AND 423 RECEIVER

The Am26LS32 is a quad line receiver which, operating from a single 5 volt supply, can be used in either differential or single-ended modes to satisfy RS-422 and 423 applications respectively. A complementary enable and disable feature, similar to that on the driver, controls all four receivers, Figure 7. The device's three-state outputs, which can sink 8mA, incorporate a fail-safe input-output relationship which keeps the outputs high when the inputs are open.

The Am26LS32 meets the receiver input specification of Table III, a 200mV threshold sensitivity with common mode rejection exceeding the supply line potentials, (greater than 7 volts). The same design feature of the input circuit which provides the common mode rejection also insures excellent power supply ripple rejection, which is important when switching the high currents involved in a system's interfaces. Furthermore, unlike operational amplifiers, where the DC common mode and power supply rejection ratios roll off with open loop gain, the full rejection capability of this line receiver is maintained at high frequencies. The receiver hysteresis of typically 30mV, provides differential noise immunity. Signals received on long lines can have slow transition times, and without hysteresis, a small amount of noise around the switching threshold can cause errors in the receiver output.

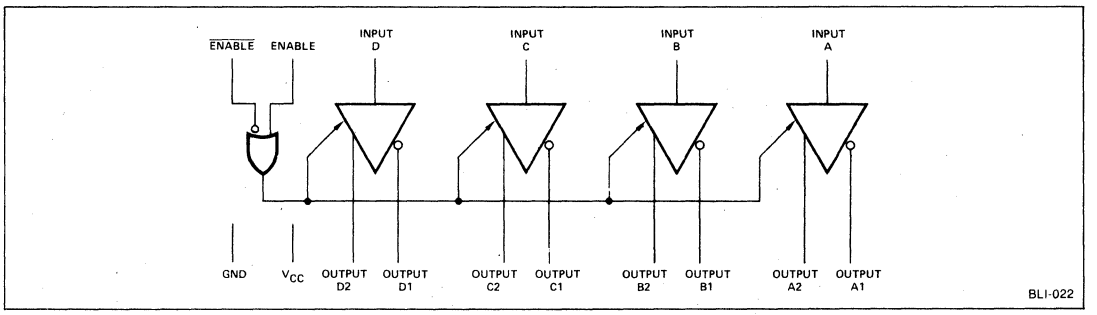


Figure 5. Am26LS31 Logic Diagram.

TABLE III
SUMMARY OF EIA RS-422 STANDARD FOR A BALANCED DIFFERENTIAL INTERFACE

A. Line Driver

Open Circuit Voltage (either logic state)
- Differential: $|V_{do}| \leq 6.0V$
- Common Mode: $|V_{cmo}| \leq 3.0V$

Differential Output Voltage (across 100 ohm load)
- Either logic state: $|V_d| \geq \max(0.5V_{do}, 2.0V)$

Output Impedance
- Either logic state: $R_G \leq 100$ ohms

Mark-Space Level Symmetry (across 100 ohm load)
- Differential: $|V_{dS}| - |V_{dM}| \leq 0.4V$
- Common Mode: $|V_{cmS}| - |V_{cmM}| \leq 0.4V$

Output Short Circuit Current (to ground)
- Either Output: $|I_{SC}| \leq 150mA$

Output Leakage Current (power off)
- Voltage Range: $-0.25V \leq V_x \leq +6.0V$
- Either Output at V_x: $|I_x| \leq 100\mu A$

Rise and Fall Times (across 100 ohm load)
- T = Baud Interval: $(t_r, t_f) \leq \max(0.1T, 20ns)$

Ringing (across 100 ohm load)
- Definitions
  - $V_{dSS} = V_d$ (steady state)
  - $V_{SS} = V_{dS} - V_{dM}$ (steady state)
- Limits (either logic state)
  - Percentage: $|V_d - V_{dSS}| \leq 0.1V_{SS}$
  - Absolute: $2.0V \leq |V_d| \leq 6.0V$

B. Line Receiver

Signal Voltage Range
- Differential: $|V_d| \leq 6.0V$
- Common Mode: $|V_{cM}| \leq 7.0V$

Single-Ended Input Current (power ON or OFF)
- Either Input at V_x: $|V_x| = 10V$
- Other Input Grounded: $|I_V| \leq 3.25mA$

Single-Ended Input Bias Voltage (other input grounded)
- Either Input Open Circuit: $|V_B| \leq 3.0V$

Single-Ended Input Impedance (other input grounded)
- Either Input: $R_L \geq 4000$ ohms

Differential Threshold Sensitivity
- Common Mode Voltage Range: $|V_{cm}| \leq 7.0V$
- Either Logic State: $|V_T| \leq 200mV$

Absolute Maximum Input Voltage
- Differential: $|V_d| \leq 12V$
- Single-Ended: $|V_x| \leq 10V$

Input Balance (threshold shift)
- Common Mode Voltage Range: $|V_{cm}| \leq 7.0V$
- Differential Threshold (500 ohms in series with each input)
  - Either Logic State: $|V_t| \leq 400mV$

Termination (optional)
- Total Load Resistance (differential): $R_T > 90$ ohms

Multiple Receivers (bus applications)

Up to 10 receivers allowed. Differential threshold sensitivity of 200mV must be maintained.

Hysteresis (optional)

As required for applications with slow rise/fall time at receiver, to control oscillations.

Fail Safe (optional)

As required by application to provide a steady MARK or SPACE condition under open connector or driver power OFF condition.

C. Interconnecting Cable

Type
- Twisted Pair Wire or Flat Cable Conductor Pair

Conductor Size
- Copper Wire (solid or stranded): 24 AWG or larger
- Other (per conductor): $R \leq 30$ ohms/1000 ft.

Capacitance
- Mutual Pair: $C \leq 20pF/ft.$
- Stray: $C \leq 40pF/ft.$

Pair-to-Pair Cross Talk (balanced)
- Attenuation at 150KHz: $A \geq 40dB$

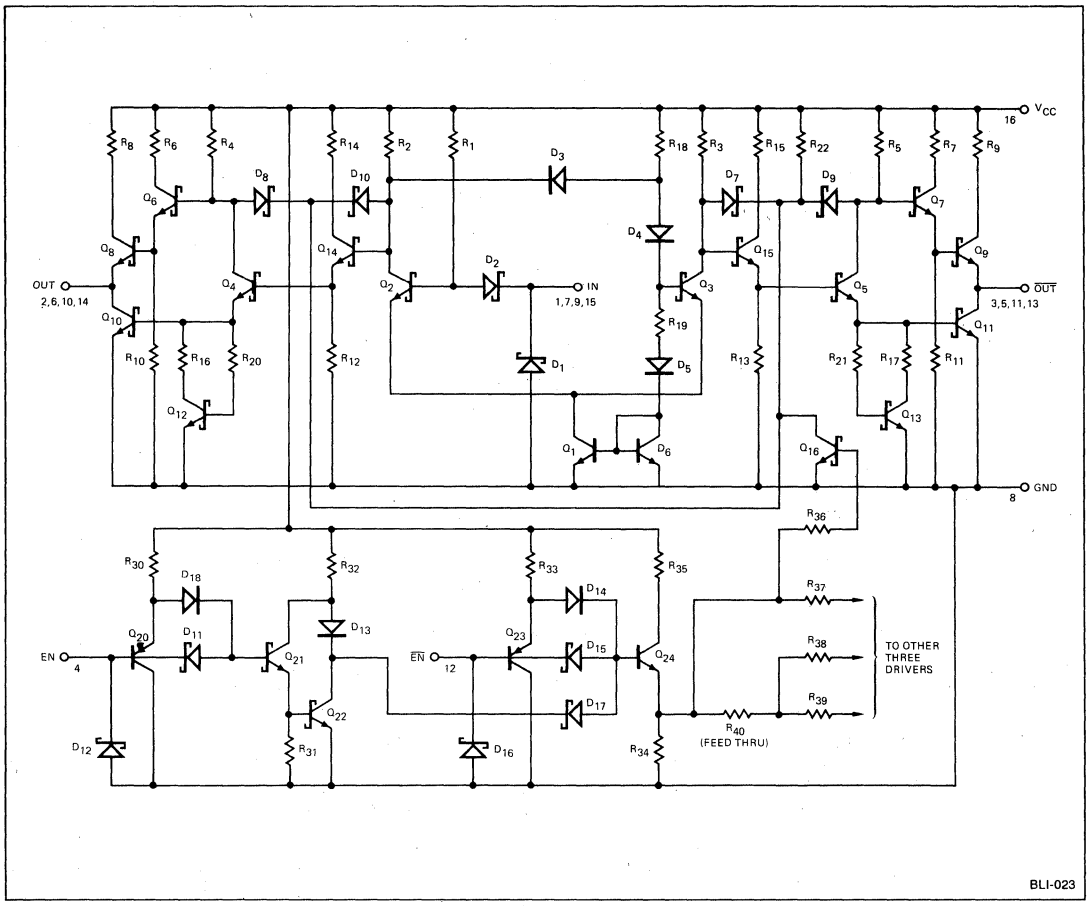


Figure 6. Am26LS31 Circuit Diagram (Only one driver shown).

The balanced differential line receiver is a three-stage circuit. The input stage consists of a low-impedance differential current amplifier with series resistor inputs to convert line signal voltage to current and provide a moderate input impedance. The input resistors provide an impedance greater than 6K on each input, power on or power off, which exceeds the requirements of RS-422 and RS-423. This is one advantage of the current amplifier input circuit. Another advantage is that is can operate with immunity to common mode voltages above V_{CC} and below ground. The differential threshold sensitivity of this circuit is 200mV, as required by RS-422. The second stage is a differential voltage amplifier, which interfaces to the single-ended output stage through an emitter follower. The output stage is a standard Low-power Schottky TTL totem-pole output with three-state capability.

The full circuit is shown in Figure 8. Resistors R_{20} and R_{21}, which connect the non-inverting input to V_{CC} and the inverting input to ground, provide the fail-safe feature, which guarantees a HIGH logic state for the receiver output when there is no signal on the line. The differential voltage amplifier in the second stage is formed by Q6 and Q3 which are biased by current source Q9. The hysteresis in the receiver switching characteristic is provided by Q4 and Q5, a differential pair biased by current source Q6, whose collectors are connected in positive feedback to the input pull-up circuits. A small amount of current is switched by Q4 and Q5, which must be overcome by the different voltage signal, resulting in the hysteresis. The output stage is driven from one side of the differential second stage by emitter follower Q17, which is a multiple emitter transistor. the second emitter is the control point for the three-state output.Q17 drives the phase splitter Q12, which in turn drives the three-state totempole output. The remainder of the circuit is the output enable control logic. This three-state capability on the receiver TTL side of the interface is a useful feature for modularizing two-way bus design.

A mask option of the input resistors (R_1, R_2, R_{20} and R_{21}) modifies the receiver characteristics to improve operation in high common mode noise environments. This device, known as the Am26LS33, has these resistors at twice the value of the Am26LS32. An input differential or common mode voltage range of ±15 volts is achieved at the expense of a minor decrease of input threshold sensitivity, to ±500mV from ±200mV.

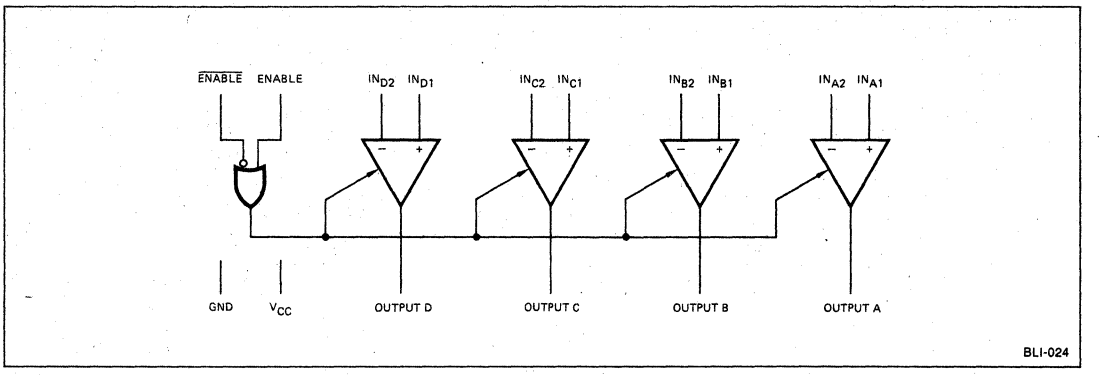


Figure 7. Am26LS32 Logic Diagram.

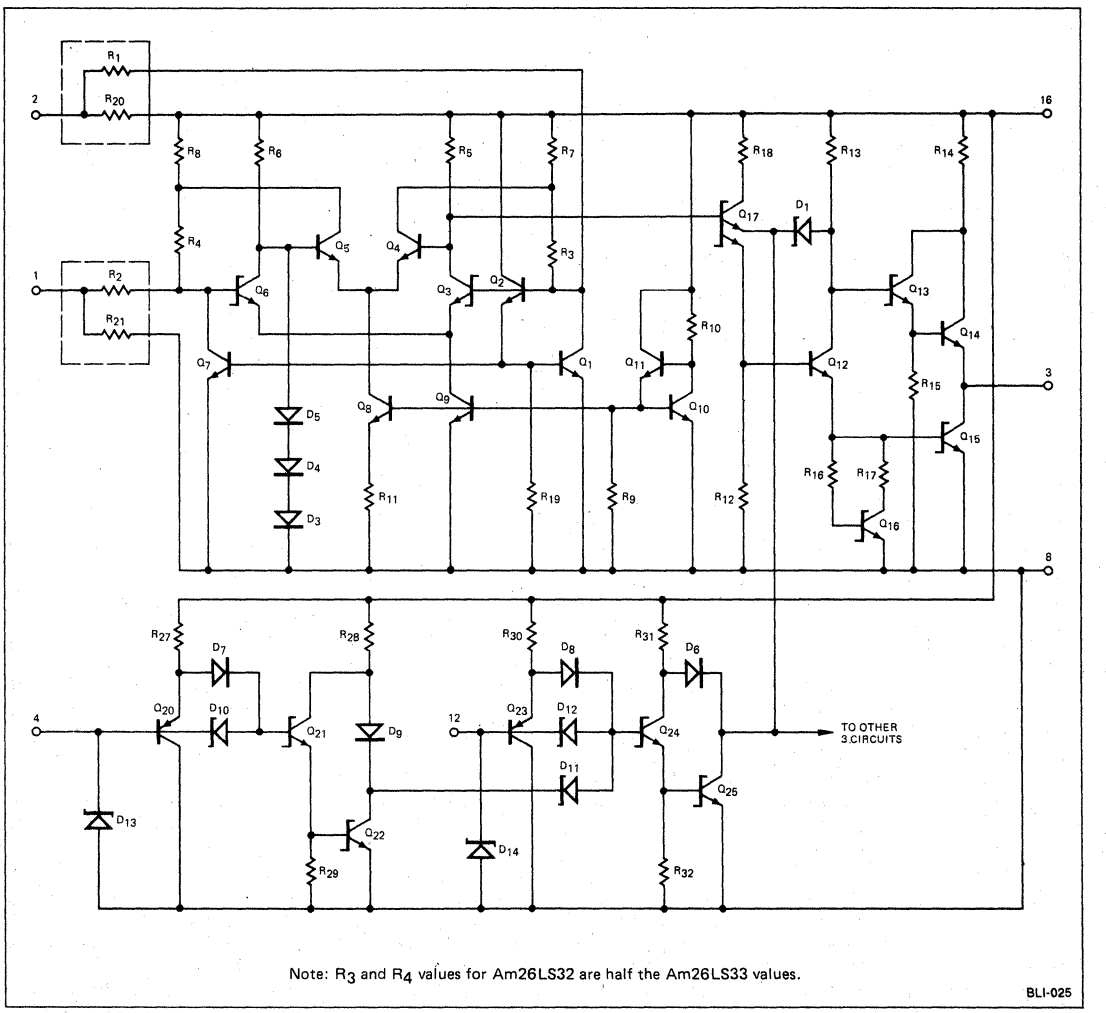


Figure 8. Am26LS32 and Am26LS33 Circuit Diagram (Only one receiver shown).

APPLICATIONS IN MIXED RS-232 AND 422/3 SYSTEMS

A system implemented with the RS-422 differential output cannot be used to drive an RS-232C system directly. An RS-423 single-ended driver, such as the Am26LS29 or Am26LS30, may be used provided certain precautions are observed.

1. Although the RS-423 driver output specification of between 4 to 5V does not meet the RS-232C specification of 6V, operation is usually satisfactory with RS-232C receivers. This is achieved because the short cable lengths permitted by RS-232C cause very little signal degredation and because of the low source impedance of the RS-423 driver.
2. RS-232C specifies that the rise time for the signal to pass through the ±3.0V transition region shall not exceed 4% of the signal element duration. RS-423 requires much slower rise times, specified from 10% to 90% of the total signal amplitude, to reduce cross talk for operation over longer distances. Therefore, the RS-423 driver in the equipment must be waveshaped. This is achieved by selection of a capacitor value for the Am26LS30 to simultaneously meet the requirements of both RS-423 and RS-232C for data rates covered by RS-232C.
3. RS-423 specifies one common return ground for each direction of transmission, RS-232C requires only one for both directions of transmission. Care must be taken to insure that a return ground path has been created when interfacing between the two systems.
4. RS-232C does not require termination, while it may be necessary for RS-422 and 423. Detailed consideration of termination is covered in the next section.

Note that RS-422 and RS-423 specifies that receivers should not be damaged by voltages up to 12V, while RS-232C allows drivers to produce output voltages up to 25V. The Am26LS32 receiver has been designed to avoid this hazard and can withstand input voltages of ±25 volts.

RS-422 TRANSMISSION LINE FEATURES

Any time a receiver and transmitter are connected with more than a few inches of a wire, problems due to reflections can arise if care is not exercised to terminate the line correctly. RS-422 describes the cable as a twisted pair of approximately 120Ω impedance terminated in a resistor R_T. R_T is not specified because there are two extreme values which may be chosen for the two following general classes of usage: (1) single direction transmission; and (2) multi-direction and multiple source transmission (party line). Considering the cable impedance only, the termination should equal the cable impedance of 120Ω. However this reduces the terminated cable resistance as seen by the driver to only 60Ω, with resulting loading of the output signal. This loading causes a reduction of S/N ratio at the received terminal due to the decrease in signal voltage swing. The solution lies in a compromise between an R_T of 120Ω which provides maximum power transfer at a reduced S/N ratio or R_T of 240Ω which causes a mis-match of 2-to-1 but no S/N reduction. The choice is left to the user as it is system dependent. Both schemes will work for an average line length and should only approach the margins at maximum line length and maximum bit rates.

Electronic Industries Association, when preparing EIA Standard RS-422 conducted their tests with 24 gauge twisted pair wire. The resulting length vs. data rate, is published as a guideline in RS-422 (Figure 9). This shows two important results: (1) Unmodulated baseband (NRZ) signalling is not recommended at distances greater than 4000 feet; (2) At data rates above about 100KHz, the maximum cable length for acceptable signal quality is inversely proportional to data rate.

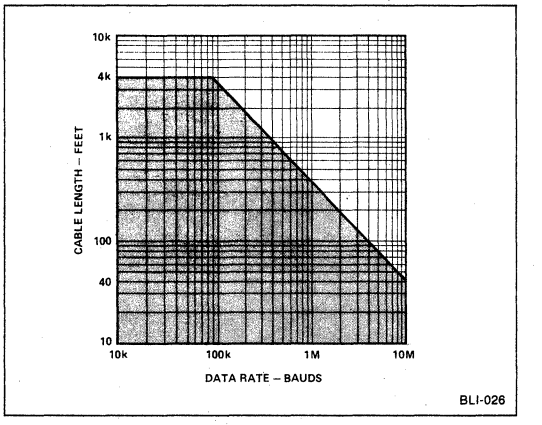


Figure 9. Data Rate Versus Cable Length for Balanced, Twisted Pair Cable (From EIA RS-422).

Result (1) above is due to the DC resistance of the cable. For a 4000 foot cable with a DC resistance of 30 ohms/1000 feet, the DC series loop resistance is 240Ω. The minimum allowable terminated differential load impedance is 90Ω. The DC voltage attentuation is 90/(90 – 240) = 1/4(6db), which is arbitrarily chosen as the maximum allowable limit.

Result (2) is due to line losses. Laboratory tests using the 26LS31 Line Driver connected to the 26LS32 Line Receiver by 800 feet of ordinary 20 AWG twisted pair (Beldon #8205 plastic-jacketed wire), terminated in its characteristic impedance of 100Ω were evaluated. The input waveform was a 500KHz square wave with (10% to 90%) rise and fall times of less than 10ns. The output waveform produced rise and fall times which together accounted for approximately one-half the period ($t_r + t_f$ = 500ns). This was due to line loss and constant capacity. The energy per cycle of the output waveform is approximately 25% lower than that of the input. The input rise and fall times are not a function of line length, assuming matching termination. The output rise and fall times are dependent upon length in a complex manner. Furthermore, it can be shown by observation that they build up along the line.

Many good reference sources are available on the subject of transmission lines (References 1, 2, 3 and 4). These will provide background information to the following discussion.

Seshadri in Reference (1) has analyzed a line with series resistance losses and has shown that rise time varies with the square of the length. This shows series resistance to be a function of the square root of frequency. However when one tries to use this result in combination with the previous result, it becomes apparent just how difficult the problem is. In Reference (2), the authors point out that skin depth implies a frequency dependent series inductance as well as resistance, and that one cannot be considered without the other.

They go on to show how this leads to the same result; namely that rise and fall times vary with the square of distance.

No attempt will be made to explain here why Figure 5 shows maximum length varying inversely with frequency rather than with the square of frequency. Certainly many complex factors are involved. Our laboratory observations showed a dependence somewhere in between linear and square law.

The Am26LS31 Quad Line Driver and the Am26LS32 Quad Line Receiver are capable of good, clean operation to the distance limits and data rate limits of RS-422.

SYSTEM APPLICATIONS

The Am26LS30, 31, 32 and 33 can be combined in various signaling networks. Using Am26LS29, Am26LS30 and Am26LS32, Figure 10, a unidirectional RS-423 communication can be constructed. Allowing for the voltage variation described earlier, RS-232C requirements can be satisfied. It should be noted that the Am26LS29 or Am26LS30 is used above to meet the bipolar requirements. If a single-ended line, Figure 11, is required without a bipolar requirement, the Am26LS31 can be used by biasing the reference terminal of the receiver to approximately 1.5 volts. Note that additional resistors will enhance fail safe operation.

Figure 12 shows the use of the Am26LS31 and Am26LS32 to meet a balanced line, single direction RS-422 application. If bidirectionality is required, an additional termination should be added as shown in Figure 13.

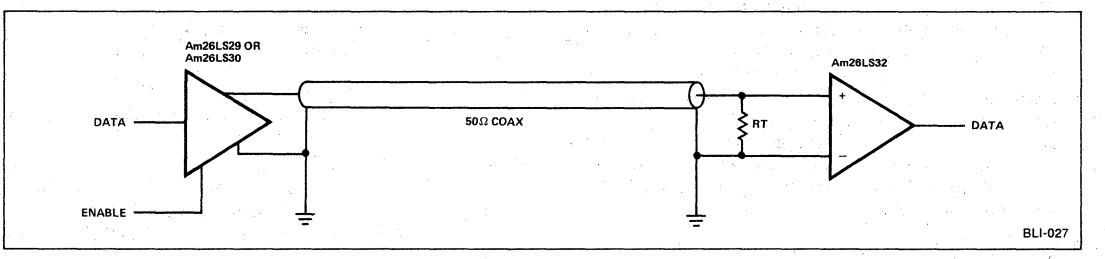


Figure 10. Unidirectional RS-423 (partial RS-232C).

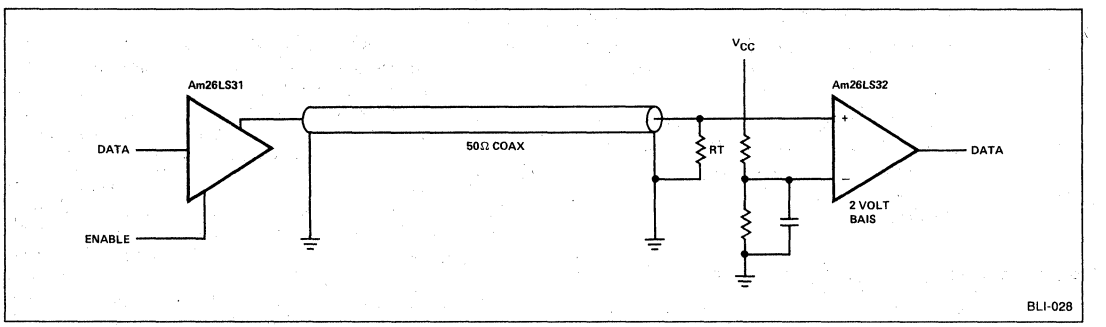


Figure 11. Single-Ended Line Without Bipolar Requirement.

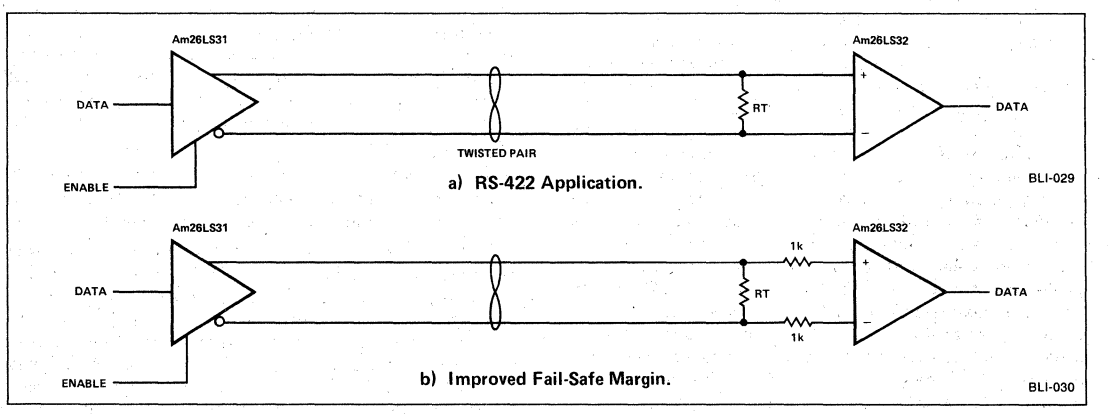


Figure 12.

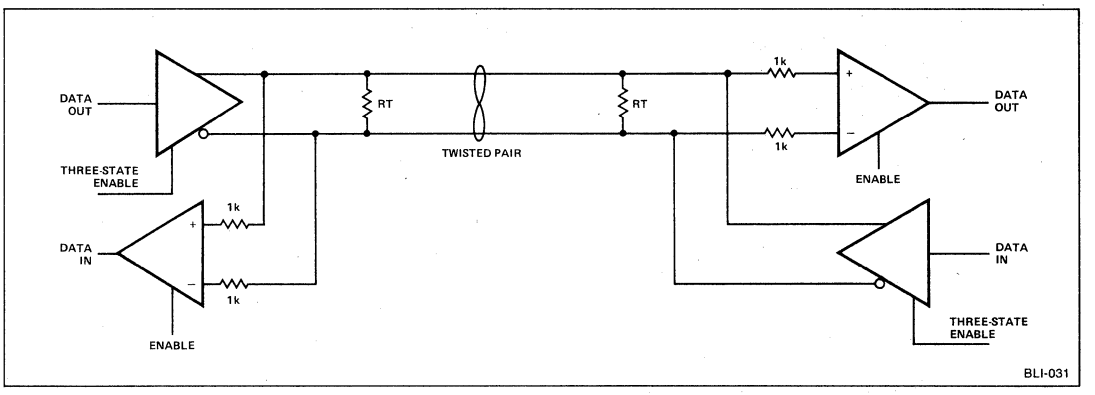


Figure 13. Bidirectional RS-422.

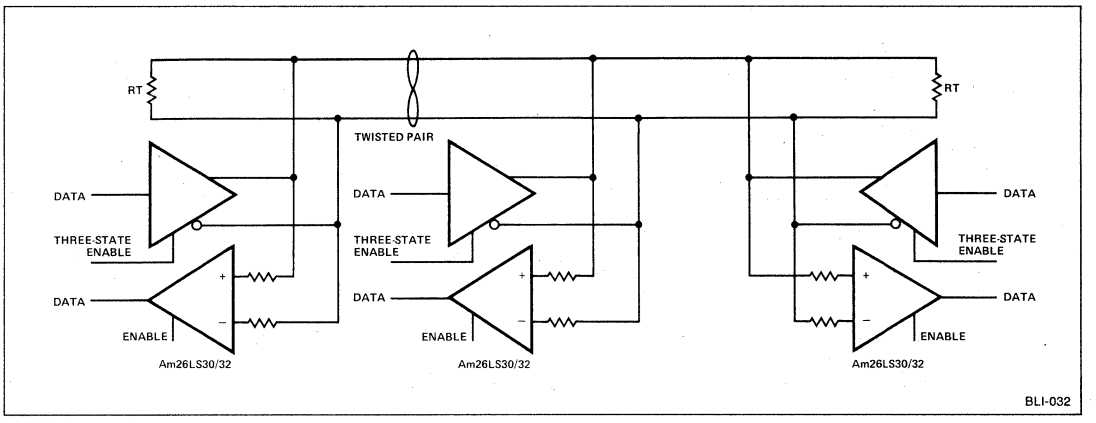


Figure 14. Party Line Configuration.

a) Full Duplex Four-Wire Data Communication RS-422 Interface (with Data Modem).

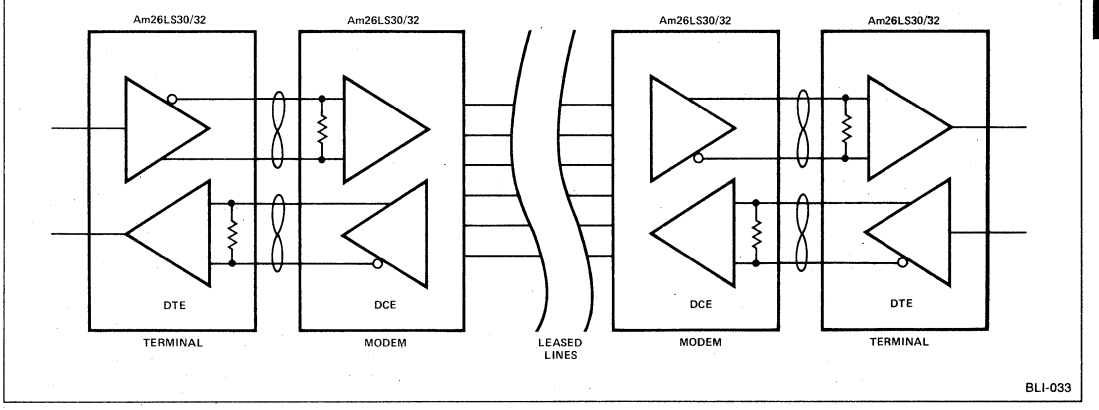


Figure 15.

b) Full Duplex Four-Wire Data Communication RS-422 Interface (without Data Modem).

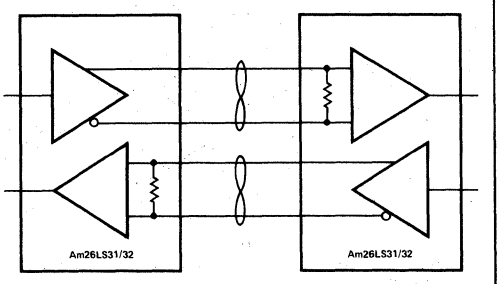


Figure 15. (Cont.)

The high speed capability of RS-422 has attracted the interest of many computer designers for use in the party line mode (Figure 14). The most common usage is that of a four wire full duplex exchange system (Figure 15). This mode of operation involves two pairs of wires each handling a single direction of traffic. The outgoing direction consists of one driver (Am26LS30 or Am26LS31) and n receivers (Am26LS32 or Am26LS33). The incoming direction consists of one receiver (Am26LS32 or Am26LS33) and n drivers (Am26LS30 or Am26LS31). This seems extremely simple to organize. However, problems arise when system ground is considered. If the network of receiver and driver span a moderate to long physical distance, ground loop noise or differences are developed changing the voltage that appears at the terminals of all receivers and drivers except for the one driver that is active. It remains the system reference as long as it is active. This induced or system developed voltage is referred to as Common Mode voltage (CMV) and as such must be considered as a device parameter. All manufacturers specify CMV capability of their receiver in compliance with RS-422 (approx. 7 volts plus signal) but there is no specification for drivers. If the dimensions of the system are short compared to 1/4 wave length of the maximum date rise and fall times, the CMV can be assumed to be minimal and drivers with single voltage supply and limited negative CMV can be used, i.e., Am26LS31. If the system dimensions are large, the CMV will cause problems in that the driver will clamp to the ground the moment the collective or apparent voltage swings below minus 0.5 volts relative to the driver ground, causing a short in the line and increasing level shift and noise. The clamping is caused in part by conduction of the I/C substrate diode. The problem can be avoided by using a driver with an output common mode range (Am26LS30). The Am26LS30 guarantees an output CMV range of ±10 volts about the driver ground reference. New international standards are under consideration to specify this mode of operation. In conclusion, a good system of 4 wire full duplex for data communication would use as an outgoing pair an Am26LS30 line driver and up to 12 – Am26LS32 line receivers, with a termination at the near and far ends of the cable. The same system would use as an incoming pair an Am26LS32 line receiver and up to 32 – Am26LS30 line drivers with only one enabled at a time and all others in three-state mode with cable termination at both near and far ends of the cable.

Many other applications are possible using this family of devices. Although the designs are based on the requirements of the EIA data communications specifications, they are not limited to these situations. Aircraft buses and internal equipment interconnections will benefit from the features offered by these products.

REFERENCES

1. Seshadri, S. R., Fundamental of Transmission Lines and Electromagnetic Fields, (U. of Wisconsin), Addison-Wesley, Reading, Mass., 1971.
2. Adler, R. B., L. J. Chu, and R. M. Fano, Electromagnetic Energy Transmission and Radiation, (MIT), John Wiley & Sons, New York, 1963.
3. Matick, R. E., Transmission Lines for Digital and Communication Networks, (IBM), McGraw-Hill, New York, 1969.
4. Reference Data for Radio Engineers, (ITT), Fifth Edition, Howard W. Sams & Company, Indianapolis, 1974.
5. Electronic Industries Association, 2001 Eye Street, N.W. Washington, D.C., RS Standard Proposal, RS-232C, August, 1969.
6. Electronic Industries Association, 2001 Eye Street, N.W. Washington, D.C., RS Standard Proposal 1220, Rev. RS-422, September 21, 1976.
7. Electronic Industries Association, 2001 Eye Street, N.W. Washington, D.C., RS Standard Proposal 1221, Rev. RS-423, September 21, 1976.

Am26LS34

Quad Differential Line Receiver

DISTINCTIVE CHARACTERISTICS

- Meets all requirements of EIA Standards RS-422, RS-423, CCITT V.10 and V.11, and the new party line standard in development under EIA Project Number 1360.
- ± 200mV sensitivity over input voltage range
- ± 150mV sensitivity for V_{CM} = 0
- −7V to +12V common mode input voltage range
- 12kΩ minimum input impedance
- Maximum guarantees for t_{PD} skew
- All AC and DC parameters guaranteed over MIL and COM'L temperature ranges
- Guaranteed input voltages hysteresis limits
  - 120mV minimum
  - 300mV maximum
- No internal failsafe
- Pin compatible with Am26LS32/32B/33

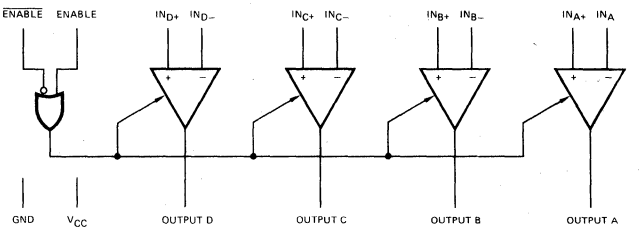
FUNCTIONAL DESCRIPTION

The Am26LS34 is a high performance, quad, differential line receiver. It has higher impedance and higher input voltage hysteresis than the similar Am26LS32B. The Am26LS34 also does not have internal fail-safe to allow greater user flexibility.

Input threshold sensitivity is specified for three different V_{CM} ranges. The improved sensitivity, guaranteed hysteresis and skew limits allow a more critical analysis of system performance in high noise environments and better system performance capability.

All performance parameters are guaranteed over ±10% supplies and over the operating temperature range. In addition, I_{OL} is specified to 24mA for easy system bus interfacing.

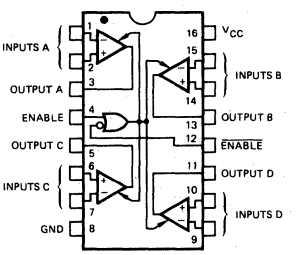
LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Am26LS34 Order Number
Hermetic DIP	−55 to +125°C	AM26LS34DM
Flat Pak	−55 to +125°C	AM26LS34FM
Dice	−55 to +125°C	AM26LS34XM
Hermetic DIP	0 to +70°C	AM26LS34DC
Molded DIP	0 to +70°C	AM26LS34PC
Dice	0 to +70°C	AM26LS34XC

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

Supply Voltage	7.0V
Common Mode Voltage	±25V
Differential Input Voltage	30V
Enable Voltage	7.0V
Output Sink Current	50mA
Storage Temperature Range	−65 to +165°C

ELECTRICAL CHARACTERISTICS over the operating temperature range

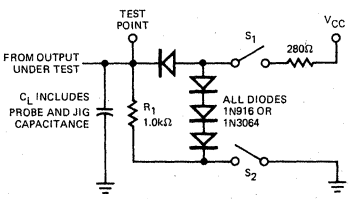
The following conditions apply unless otherwise specified:

(MIL) T_A = −55 to +125°C V_{CC} = 5.0V ± 10%
(COM'L) T_A = 0 to +70°C V_{CC} = 5.0V ± 5%

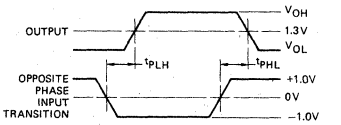
Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{TH}	Differential Input Voltage	$V_{OUT} = V_{OL}$ or V_{OH}	V_{CM} = 0V	−150	±90	+150	mV
			−7V ≤ V_{CM} ≤ +12V	−200		+200	
			−15V ≤ V_{CM} ≤ +15V	−400		+400	
V_{HYST}	Input Hysteresis			120	180	300	mV
R_{IN}	Input Resistance	−15V ≤ V_{CM} ≤ +15V (One input AC ground)		12k	20k	40k	Ω
I_{IN}	Input Current (Under Test)	V_{IN} = +12V			0.7	1.0	mA
I_{IN}	Input Current (Under Test)	V_{IN} = −7V			−0.5	−0.8	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min, Δ V_{IN} = +1.0V, $V_{\overline{ENABLE}}$ = 0.8V	−12mA	2.0			Volts
			−1mA	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min, Δ V_{IN} = −1.0V, $V_{\overline{ENABLE}}$ = 0.8V	I_{OH} = 16mA			0.4	Volts
			I_{OL} = 24mA			0.5	
V_{IL}	Enable LOW Voltage					0.8	Volts
V_{IH}	Enable HIGH Voltage			2.0			Volts
V_I	Enable Clamp Voltage	V_{CC} = Min, I_{IN} = −18mA				−1.5	Volts
V_{IOC}	Open Circuit Input Voltage			2.0		3.0	Volts
I_O	Off-State (High Impedance) Output Current	V_{CC} = Max	V_O = 2.4V			50	μA
			V_O = 0.4V			−50	
I_{IL}	Enable LOW Current	V_{IN} = 0.4V			−0.03	−0.2	mA
I_{IH}	Enable HIGH Current	V_{IH} = 2.7V			0.5	20	μA
I_I	Enable Input High Current	V_{IN} = 5.5V			1	100	μA
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{CC} = Max, Δ V_{IN} = +1.0V		−30	−65	−120	mA
I_{CC}	Power Supply Current	V_{CC} = Max, All V_{IN} = GND, Outputs Disabled			52	70	mA

Note: 1. All typical values are V_{CC} = 5.0V, T_A = 25°C.

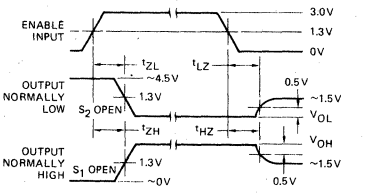
LOAD TEST CIRCUIT FOR THREE-STATE OUTPUTS



PROPAGATION DELAY (Notes 1 and 3)



ENABLE AND DISABLE TIMES (Notes 2 and 3)



Notes: 1. Diagram shown for $\overline{\text{Enable}}$ LOW.
2. S_1 and S_2 of Load Circuit are closed except where shown.
3. Pulse Generator Rate ≤ 1.0MHz; Z_o = 50Ω; t_r, t_f ≤ 2.5ns.

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

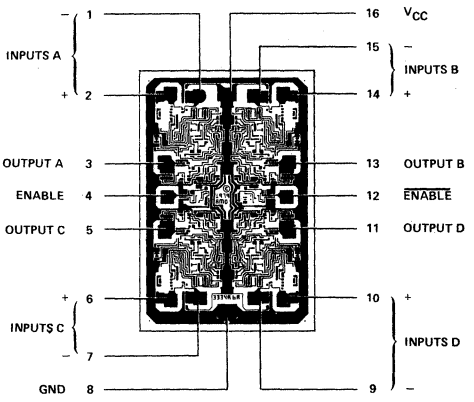
Parameters	Description	Min	Typ	Max	Units	Test Conditions
t_{PLH}	Propagation Delay, Input to Output		18	24	ns	C_L = 50pF See test circuit
t_{PHL}			20	24	ns	
t_{SKEW}	Propagation Delay Skew, $t_{PLH} - t_{PHL}$		2	4	ns	
t_{ZL}	Output Enable Time, ENABLE to Output		16	22	ns	
t_{ZH}			10	16	ns	
t_{LZ}	Output Disable Time, ENABLE to Output		11	18	ns	C_L = 5pF See test circuit
t_{HZ}			13	18	ns	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Am26LS34 COM'L T_A = 0 to +70°C V_{CC} = 5.0V ± 10% Min	Am26LS34 COM'L Max	Am26LS34 MIL T_A = −55 to +125°C V_{CC} = 5.0V ± 10% Min	Am26LS34 MIL Max	Units	Test Conditions
t_{PLH}	Propagation Delay, Input to Output		30		30	ns	C_L = 50pF See test circuit
t_{PHL}			30		30	ns	
t_{SKEW}	Propagation Delay Skew, $t_{PLH} - t_{PHL}$		±5		±5	ns	
t_{ZL}	Output Enable Time, ENABLE to Output		33		33	ns	
t_{ZH}			22		22	ns	
t_{LZ}	Output Disable Time, ENABLE to Output		27		27	ns	C_L = 5pF See test circuit
t_{HZ}			27		27	ns	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.056" X 0.084"

MOS Microprocessor Support Products (for 8080/8086/8088/Z8000) Index

Am8120

Octal D-Type Flip-Flop with Clear, Clock Enable and Three-State Control

DISTINCTIVE CHARACTERISTICS

- Buffered common clock enable input
- Buffered common asynchronous clear input
- Three-state outputs
- 8-bit, high-speed parallel register with positive edge-triggered, D-type flip-flops

RELATED PRODUCTS

Part No.	Description
Am25S18	Quad D Register
Am2920	Octal D Type Flip-Flop
Am2954/5	Octal D Registers

FUNCTIONAL DESCRIPTION

The Am8120 is an 8-bit register built using advanced Low-Power Schottky technology. The register consists of eight D-type flip-flops with a buffered common clock, a buffered common clock enable, a buffered asynchronous clear input, and three-state outputs.

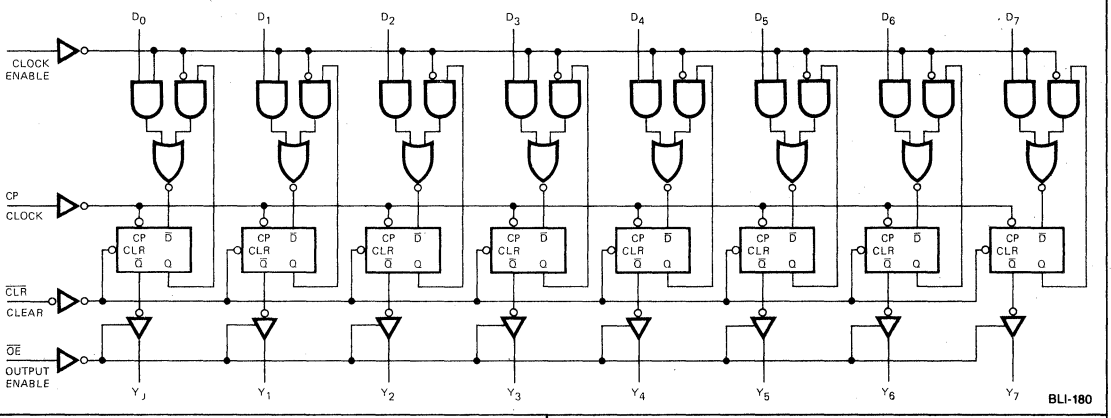
When the clear input is LOW, the internal flip-flops of the register are reset to logic 0 (LOW), independent of all other inputs. When the clear input is HIGH, the register operates in the normal fashion.

When the three-state output enable ($\overline{OE}$) input is LOW, the Y outputs are enabled and appear as normal TTL outputs. When the output enable ($\overline{OE}$) input is HIGH, the Y outputs are in the high impedance (three-state) condition. This does not affect the internal state of the flip-flop Q output.

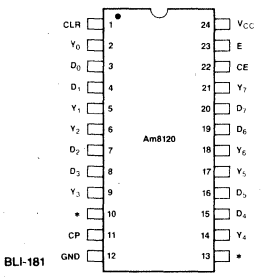
The clock enable input ($\overline{E}$) is used to selectively load data into the register. When the $\overline{E}$ input is HIGH, the register will retain its current data. When the $\overline{E}$ is LOW, new data is entered into the register on the LOW-to-HIGH transition of the clock input.

This device is packaged in a slim 24-pin package (0.3 inch row spacing).

LOGIC DIAGRAM

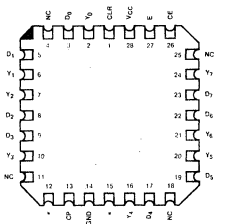


CONNECTION DIAGRAMS — Top Views



Note: Pin 1 is marked for orientation.

Leadless Chip Carrier
L-28-1



*Reserved — do not use.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0 to +70°C	AM8120PC
Hermetic DIP	0 to +70°C	AM8120DC
Chip-Pak	0 to +70°C	AM8120LC
Dice	0 to +70°C	AM8120XC
Hermetic DIP	−55 to +125°C	AM8120DM
Hermetic Flat Pack	−55 to +125°C	AM8120FM
Chip-Pak	−55 to +125°C	AM8120LM
Dice	−55 to +125°C	AM8120XM

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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75V MAX. = 5.25V

MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50V MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	MIL, $I_{OH} = -1.0mA$		2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6mA$		2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$				0.4	Volts
			$I_{OL} = 8.0mA$				0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$					−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$					20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$					0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$				−20	μA
			$V_O = 2.4V$				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				24	37	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All outputs open, $\overline{E}$ = GND, Di inputs = CLR = $\overline{OE}$ = 4.5V. Apply momentary ground, then 4.5V to clock input.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)			18	27	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}				24	36		
t_{PHL}	Clear to Y			22	35	ns	
t_s	Data (D_i)		10	3		ns	
t_h	Data (D_i)		10	3		ns	
t_s	Enable ($\overline{E}$)	Active	15	10		ns	
		Inactive	20	12			
t_h	Enable ($\overline{E}$)		0	0		ns	
t_s	Clear Recovery (In-Active) to Clock		11	7		ns	
t_{pw}	Clock	HIGH	20	14		ns	
		LOW	25	13			
t_{pw}	Clear		20	13		ns	
t_{ZH}	$\overline{OE}$ to Y_i			9	13	ns	
t_{ZL}				14	21		
t_{HZ}	$\overline{OE}$ to Y_i			20	30	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				24	36		
f_{max}	Maximum Clock Frequency (Note 1)			40		MHz	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5% Min.	COM'L Max.	MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10% Min.	MIL Max.	Units	Test Conditions
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)			33		39	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}				45		54		
t_{PHL}	Clear to Y			43		51	ns	
t_s	Data (D_i)		12		15		ns	
t_h	Data (D_i)		12		15		ns	
t_s	Enable ($\overline{E}$)	Active	17		20		ns	
		Inactive	20		23			
t_h	Enable ($\overline{E}$)		0		0		ns	
t_s	Clear Recovery (In-Active) to Clock		13		15		ns	
t_{pw}	Clock	HIGH	25		30		ns	
		LOW	30		35			
t_{pw}	Clear		22		25		ns	
t_{ZH}	$\overline{OE}$ to Y_i			19		25	ns	
t_{ZL}				30		39		
t_{HZ}	$\overline{OE}$ to Y_i			35		40	ns	C_L = 5.0 pF, R_L = 2.0 kΩ
t_{LZ}				39		42		
f_{max}	Maximum Clock Frequency (Note 1)		25		20		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

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DEFINITION OF FUNCTIONAL TERMS

D_i — The D flip-flop data inputs.

$\overline{CLR}$ — When the clear input is LOW, the Q_i outputs are LOW, regardless of the other inputs. When the clear input is HIGH, data can be entered into the register.

CP — Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.

Y_i — The register three-state outputs.

$\overline{E}$ — Clock Enable, When the clock enable is LOW, data on the D_i input is transferred to the Q_i output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_i outputs do not change state, regardless of the data or clock input transitions.

$\overline{OE}$ — Output Control. When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

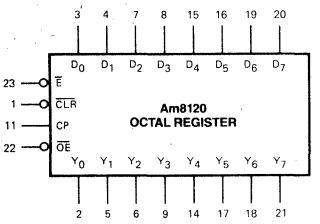
FUNCTION TABLE

	Inputs					Internal	Outputs
Function	$\overline{OE}$	$\overline{CLR}$	$\overline{E}$	D_i	CP	Q_i	Y_i
Hi-Z	H	X	X	X	X	X	Z
Clear	H	L	X	X	X	L	Z
	L	L	X	X	X	L	L
Hold	H	H	H	X	X	NC	Z
	L	H	H	X	X	NC	NC
Load	H	H	L	L	↑	L	Z
	H	H	L	H	↑	H	Z
	L	H	L	L	↑	L	L
	L	H	L	H	↑	H	H

H = HIGH
L = LOW
X = Don't Care

NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

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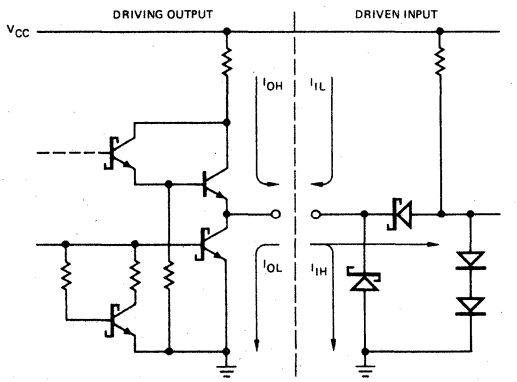
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

BLI-183

Am8127

AmZ8000 Clock Generator

DISTINCTIVE CHARACTERISTICS

- **High-drive high-level clock output**
  Special output provides clock signal matched to requirements of AmZ8000* CPU (4MHz and some 6MHz applications), MMU and DMA devices.
- **Four TTL-level clocks**
  Generates synchronized TTL compatible clocks at 16MHz, 2MHz and 1MHz to drive memory circuits and LSI peripheral devices. An additional TTL clock is synchronized with the CPU high-level clock for registers, latches and other peripherals.
- **Synchronized $\overline{\text{WAIT}}$ state and time-out controls**
  On-chip logic generates $\overline{\text{WAIT}}$ signal under control of Halt, Single-step, Status and Ready signals. Automatic time-out of peripheral wait requests.

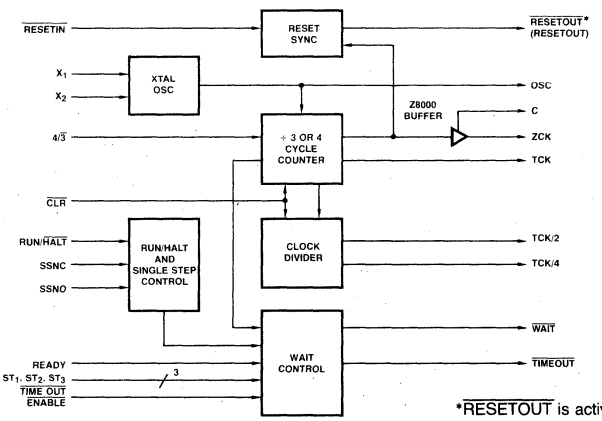
FUNCTIONAL DESCRIPTION

The Am8127 Clock Generator and Controller provides the clock oscillator, frequency dividers and clock drivers for the complete array of AmZ8000 CPUs, peripherals and memory system configurations. In addition to the special 4MHz output driver for the AmZ8001* and AmZ8002* CPUs, a standard buffered TTL 16MHz oscillator output is provided for a dynamic memory timing and control. In addition to 4MHz applications, the Am8127 will also function in some 6MHz Z8000 applications. The Am8127 forms an integral part of the dynamic memory support chip set including the Am8163 EDC and Refresh Controller, Am2964 Dynamic Memory Controller, Am2960 Error Detection and Correction Unit and Am2961/Am2962 EDC Bus Buffers. The oscillator is designed to operate with a 16MHz crystal or with external 16MHz drive. The Am8127 uses an internal divide-by-4 to provide 4MHz clock drive to the AmZ8001/AmZ8002 CPU. Additional dividers generate synchronous buffered 4, 2 and 1MHz clock outputs for use by peripheral devices. The clock divider counters are clearable to allow synchronizing the multiple clock outputs.

The controller functions include $\overline{\text{RESET}}$, RUN/$\overline{\text{HALT}}$, SINGLE-STEP, READY and a READY TIMEOUT counter which limits a peripheral's wait request to 16 clock cycles. The CPU's $\overline{\text{WAIT}}$ input is controlled by RUN/$\overline{\text{HALT}}$, Single-Step, Status and READY. When RUN/$\overline{\text{HALT}}$ is LOW the Am8127 drives the $\overline{\text{WAIT}}$ output LOW causing the CPU to add wait states (TW). The READY input is used by peripherals to request wait states. The active LOW input timeout enable, $\overline{\text{TOEN}}$, is used to force $\overline{\text{TIMEOUT}}$ LOW and WAIT HIGH 16 clock cycles after a peripheral has requested a wait but fails to release the request. The CPU status lines ST_1, ST_2 and ST_3 are decoded in the Am8127 to disable the $\overline{\text{TIMEOUT}}$ counter during CPU "Internal Operations" and during refresh.

The 4/3 input controls the clock duty cycle. An internal pull-up resistor pulls this input high for AmZ8000 CPUs. A LOW input causes the cycle counter to output a 33% duty cycle.

BLOCK DIAGRAM
CLOCK GENERATOR

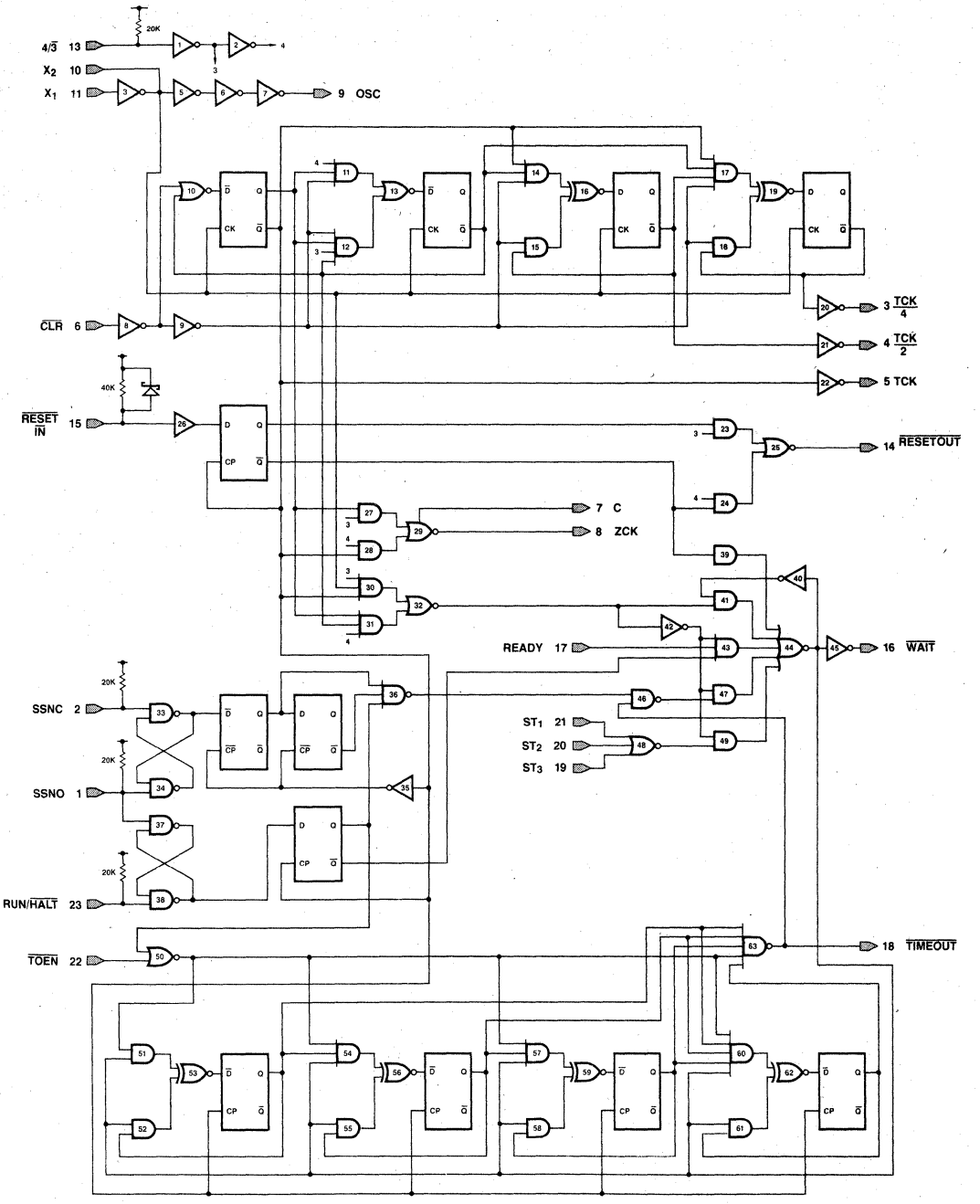


AMZ-017

*$\overline{\text{RESETOUT}}$ is active LOW when 4/3 = HIGH

*Z8000, Z8001 and Z8002 are trademarks of Zilog, Inc.

LOGIC DIAGRAM



AMZ-023

DEFINITION OF FUNCTIONAL TERMS

ZCK Buffered clock output for CPU and peripherals. This output has under/overshoot control and provides the high level output voltage required (V_{CC} – 0.4V). This output is capable of driving multiple CPU clock inputs (or DMA, MMU, etc).

C Bootstrap input. The capacitor C_B is connected from the ZCK clock output to C to provide faster ZCK risetime.

TCK TTL level buffered clock output. TCK is the same frequency as ZCK and is synchronized with ZCK. TCK is in phase with ZCK when the 4/$\overline{3}$ duty cycle control input is HIGH (50% duty cycle) and out of phase with ZCK when 4/$\overline{3}$ is LOW (33% ZCK duty cycle).

TCK/2, TCK/4 TTL buffered clocks for peripherals. TCK/2 and TCK/4 are 1/2 and 1/4 the TCK frequency and are synchronized with the rising edge of TCK.

OSC The clock oscillator TTL buffered output. This output provides a high speed clock for dynamic memory timing (e.g. AmZ8000 uses this output to generate $\overline{RAS}$/MUX-Select/$\overline{CAS}$ timing for dynamic RAMs) or other system application. The ZCK and TCK outputs are synchronized to the OSC rising edge.

4/$\overline{3}$ Clock duty cycle control for ZCK and TCK. A HIGH input (no connection – input has internal pull-up) will result in a 50% duty cycle for AmZ8000 application. A LOW input will cause a 33% duty cycle ZCK output.

$\overline{CLR}$ The clear active LOW input for internal counters. A LOW input meeting set-up and hold time requirements will clear the internal clock counters on the rising edge of OSC.

$\overline{WAIT}$ The $\overline{WAIT}$ output for connection to the CPU $\overline{WAIT}$ input. This latched output controls when the CPU enters wait states in response to the READY, ST_1, ST_2, ST_3, RUN/$\overline{HALT}$ and Single Step inputs.

READY The active HIGH READY input is used by peripherals to request wait states. Ready inputs must meet the wait latch set-up and hold time requirements.

$\overline{TIMEOUT}$ The Timeout Counter active LOW output. The Timeout Counter counts ZCK/TCK clock cycles and is used to force $\overline{WAIT}$ HIGH 15 clock cycles after a peripheral has requested a wait but has failed to release the request. This output is normally used to interrupt the CPU.

$\overline{TOEN}$ The Timeout Enable active LOW input. A LOW input allows the Timeout Counter to count, causes the $\overline{TIMEOUT}$ output to go LOW for one ZCK/TCK clock period after 15 cycles and forces $\overline{WAIT}$ HIGH at the rising edge of the 16th cycle. A HIGH input disables the counter and allows $\overline{WAIT}$ to be controlled by the READY, RUN/$\overline{HALT}$ and Single Step inputs.

$\overline{RESETOUT}$ (RESETOUT) The Reset Output to the CPU. It is active LOW when the 4/$\overline{3}$ input is HIGH and active HIGH when the 4/$\overline{3}$ input is LOW.

$\overline{RESETIN}$ The active LOW Reset Input. A LOW input will cause $\overline{RESETOUT}$ to go LOW synchronous with ZCK ⨍. Pushbutton reset is implemented by momentarily grounding $\overline{RESETIN}$. Power-up reset is implemented by connecting a capacitor from $\overline{RESETIN}$ to ground. Capacitor values from 10μF to 22μF will provide a power-up of less than one second.

RUN/$\overline{HALT}$ A debounced input to allow halt and Single Step control modes. A HIGH input allows the CPU to run. A LOW input forces the $\overline{WAIT}$ output LOW causing the CPU to enter continuous wait states until the ZCK period after RUN/$\overline{HALT}$ is returned to HIGH.

SSNO, SSNC Single Step control inputs. These debounced input allow the CPU to Single Step from one wait state to the next by momentarily disconnecting SSNC from ground and grounding SSNO. RUN/$\overline{HALT}$ must be LOW for Single Step operation.

ST_1, ST_2, ST_3 Status inputs from AmZ8000 CPU's and peripherals. Continuous LOW inputs indicate that the CPU is executing "internal operation" or "refresh." During this time the time out is disabled to avoid signaling an inappropriate interrupt. The status inputs are subject to the set-up and hold time requirements of the $\overline{WAIT}$ latch.

X_1, X_2 External crystal connections (see application section). X_1 may be driven directly by a TTL input.

*$\overline{RESETOUT}$ is active LOW when 4/$\overline{3}$ = HIGH.

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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0 to 70°C V_{CC} = 5.0V ±5% (MIN. = 4.75V MAX. = 5.25V)
MIL T_A = −55 to +125°C V_{CC} = 5.0V ±10% (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameter	Description	Test Conditions (Note 1)				Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN	ZCK	I_{OH} = −0.1mA		V_{CC}−0.4	V_{CC}−0.1		Volts
			TTL Outputs	I_{OH} = −1mA	MIL	2.4	3.4		Volts
				I_{OH} = −2.6mA	COM'L				
V_{OL}	Output LOW Voltage	V_{CC} = MIN		I_{OL} = 0.1mA, ZCK Output				0.4	Volts
				I_{OL} = 16mA, TTL Output				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input HIGH Voltage		$\overline{RESETIN}$		2.8	2.25		Volts
				ST_1, ST_2, ST_3, $\overline{CLR}$, $\overline{TOEN}$, X_1, READY		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input LOW voltage		ST_1, ST_2, ST_3, $\overline{CLR}$, $\overline{TOEN}$, X_1, READY				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA (Note 3)						−1.5	Volts
$V_{IN}-V_{IL}$	$\overline{RESETIN}$ Hysteresis	V_{CC} = MIN				400	650		mV
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V		SSNO				−1.6	mA
				SSNC, 4/$\overline{3}$, RUN/$\overline{HALT}$, READY				−1.2	mA
				$\overline{TOEN}$, $\overline{CLR}$, X_1				−0.72	mA
				$\overline{RESETIN}$, ST_1, ST_2, ST_3				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V		4/$\overline{3}$, SSNC, SSNO RUN/$\overline{HALT}$			(Note 4)	−300	μA
				$\overline{RESETIN}$			(Note 4)	−200	μA
				$\overline{CLR}$, READY, $\overline{TOEN}$ ST_1, ST_2, ST_3				+50	μA
				X_1				+600	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V		$\overline{CLR}$, READY, $\overline{TOEN}$ ST_1, ST_2, ST_3				+1.0	mA
I_{SC}	Output Short Circuit Current (Note 5)	V_{CC} = MAX		ZCK Output		−50		−240	mA
				Others		−40		−130	mA
I_{CC}	Power Supply Current	V_{CC} = MAX		X_1 = 2.4V, ZCK = TCK's = LOW			95	140	mA
				Operating, $f_{OSC} \leq$ 24MHz (Note 6)			120	180	

Notes:
1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not applicable to X_1.
4. Specification is negative because of internal input pull-up resistors.
5. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
6. For oscillator frequencies up to 24MHz, outputs open.

STATIC INPUT ELECTRICAL CHARACTERISTICS

The static control inputs, SSNO, SSNC (Single Step), RUN/$\overline{HALT}$ and 4/$\overline{3}$ (clock duty cycle control), are Low-Power Schottky TTL compatible inputs with internal pull-up resistors to the +5V supply. They may be left open for a HIGH input (e.g., 4/$\overline{3}$ is left open for operation with AmZ8001/8002), or grounded for a LOW input.

SSNO, SSNC and RUN/$\overline{HALT}$ are intended to be grounded or opened by switches. 4/$\overline{3}$ is normally left open for AmZ8001/8002. These inputs are specified at 0.4V/2.4V for test convenience.

Parameter	Description	Test Conditions		Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage	Guaranteed HIGH input voltage	RUN/$\overline{HALT}$, SSNO	2.4			Volts
V_{IL}	Input LOW Voltage	Guaranteed LOW input voltage	SSNC, 4/$\overline{3}$			0.4	Volts

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature		−65 to +150°C
Temperature (Ambient) Under Bias		−55 to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous		−0.5 to +7V
DC Voltage Applied to Outputs for HIGH Output State		−0.5V to +V_{CC} max
DC Input Voltage	X_1, 4/$\overline{3}$, SSNO, SSNC, RUN/$\overline{HALT}$	−0.5V to V_{CC} +0.5V
	Other Inputs	−0.5 to +5.5V
DC Voltage Applied to C		−0.5 to +8V
DC Output Current, Into Outputs		30 mA
DC Input Current		−30 to +5.0mA

SWITCHING CHARACTERISTICS – OSCILLATOR, $\overline{WAIT}$ AND ZCK OUTPUT

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min	Typ	Max	Units	Tests Conditions
f_{MAX}	Oscillator Frequency		24			MHz	See Test Circuits (Note 7)
t_{rC}	ZCK Rise Time	C_L = 80pF		9	12	ns	ZCK C_L = 80pF (Note 8)
t_{fC}	ZCK Fall Time			7.6	11	ns	
t_{rC}	ZCK Rise Time	C_L = 200pF		15.4	20	ns	ZCK C_L = 200pF (Note 8)
t_{fC}	ZCK Fall Time			14.0	20	ns	
t_{PLH}	READY to $\overline{WAIT}$			8	14	ns	See Test Circuits
t_{PHL}				11.5	16	ns	
t_{PLH}	Status ST_i to $\overline{WAIT}$			13	17	ns	
t_{PHL}				17.2	21	ns	
t_S	$\overline{CLR}$ to OSC (↓) Set-up Time			15	18	ns	
t_H	$\overline{CLR}$ to OSC (↓) Hold Time			−11	−6	ns	

Notes: 7. Specification is based on fundamental mode crystal. See application section.
8. ZCK rise and fall times are based on a bootstrap capacitor value of 27pF.

SWITCHING CHARACTERISTICS – 4/$\overline{3}$ = HIGH (AmZ8000 Mode)

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min	Typ	Max	Units	Test Conditions
t_S	READY to ZCK Set-up Time	(Note 9)	T/4 + 10	T/4 + 4.5		ns	See Test Circuits ZCK C_L = 80pF
t_H	READY to ZCK Hold Time		T/4 + 2	T/4		ns	
t_S	Status ST_i to ZCK Set-up Time		T/4 + 12	T/4 + 9.5		ns	
t_H	Status ST_i to ZCK Hold Time		T/4 − 3	T/4 −7.5		ns	
t_S	$\overline{TOEN}$ to ZCK Set-up Time		30	22		ns	
t_H	$\overline{TOEN}$ to ZCK Hold Time		−10	−16		ns	
t_{SKEW}	ZCK to OSC		3	6	10	ns	
t_{SKEW}	ZCK to TCK		0	4.0	7	ns	
t_{PLH}	ZCK to $\overline{RESETOUT}$ Propagation Delay			9.0	13	ns	
t_{PHL}				4	8	ns	

Note: 9. T = ZCK period.

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Am8127
SWITCHING CHARACTERISTICS OVER OPERATING RANGE – OSCILLATOR, $\overline{WAIT}$ AND ZCK OUTPUTS*

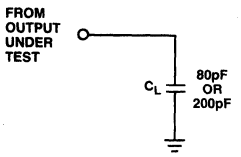
Parameters	Description		Test Conditions	Am8127 COM'L T_A = 0 to +70°C V_{CC} = 5.0V ±5% Min	Max 0°C	Max 70°C	Am8127 MIL T_A = −55 to +125°C V_{CC} = 5.0V ±10% Min	Max −55°C	Max 125°C	Units
t_{MAX}	Oscillator Frequency		(Note 7)	24			24			MHz
t_{rC}	ZCK Rise Time	C_L = 80pF	C_L = 80pF (Note 8)		15	15		20	15	ns
t_{fC}	ZCK Fall Time				14	14		20	14	ns
t_{rC}	ZCK Rise Time	C_L = 200pF	C_L = 200pF (Note 8)		25	20		32	20	ns
t_{fC}	ZCK Fall Time				25	20		32	20	ns
t_{PLH}	READY to WAIT Propagation Delay		See Test Circuits		17	17		19	19	ns
t_{PHL}					19	19		19	19	ns
t_{PLH}	Status ST_i to $\overline{WAIT}$ Propagation Delay				20	20		22	22	ns
t_{PHL}					25	25		25	25	ns
t_S	$\overline{CLR}$ to OSC (↓) Setup Time			21			30			ns
t_H	$\overline{CLR}$ to OSC (↓) Hold Time			−3			0			ns

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE – 4/$\overline{3}$ = HIGH (AmZ8000 Mode)

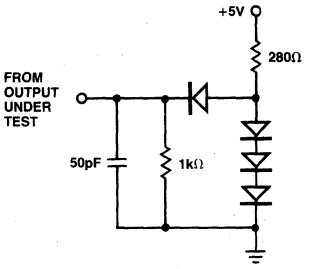
Parameters	Description	Test Conditions	Am8127 COM'L T_A = 0 to +70°C V_{CC} = 5.0V ±5% Min	Am8127 COM'L Max	Am8127 MIL T_A = −55 to +125°C V_{CC} = 5.0V ±10% Min	Am8127 MIL Max	Units
t_S	READY to ZCK Setup Time	See Test Circuits ZCK C_L = 80pF	T/4 + 14		T/4 + 17		ns
t_H	READY to ZCK Hold Time		T/4 + 5		T/4 + 5		ns
t_S	Status ST_i to ZCK Setup Time		T/4 + 15		T/4 + 20		ns
t_H	Status ST_i to ZCK Hold Time		T/4		T/4 + 5		ns
t_S	$\overline{TOEN}$ to ZCK Setup Time		35		40		ns
t_H	$\overline{TOEN}$ to ZCK Hold Time		−5		0		ns
t_{SKEW}	ZCK to OSC Skew		2	14	2	17	ns
t_{SKEW}	ZCK to TCK Skew		−2	10	−2	14	ns
t_{PLH}	ZCK to $\overline{RESETOUT}$ Propagation Delay			16		20	ns
t_{PHL}				16		20	ns

SWITCHING TEST CIRCUITS



AMZ-018

ZCK Output

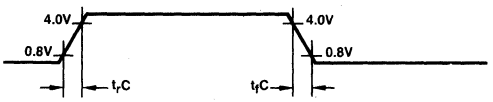


AMZ-019

TTL Outputs

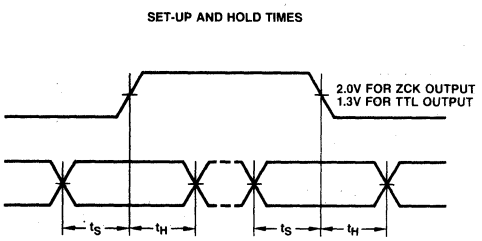
SWITCHING TEST WAVEFORMS

ZCK RISE AND FALL TIMES



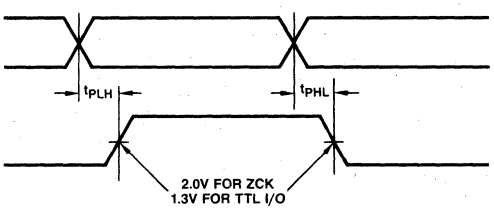
AMZ-020

SET-UP AND HOLD TIMES



AMZ-021

PROPAGATION DELAY TIMES



AMZ-022

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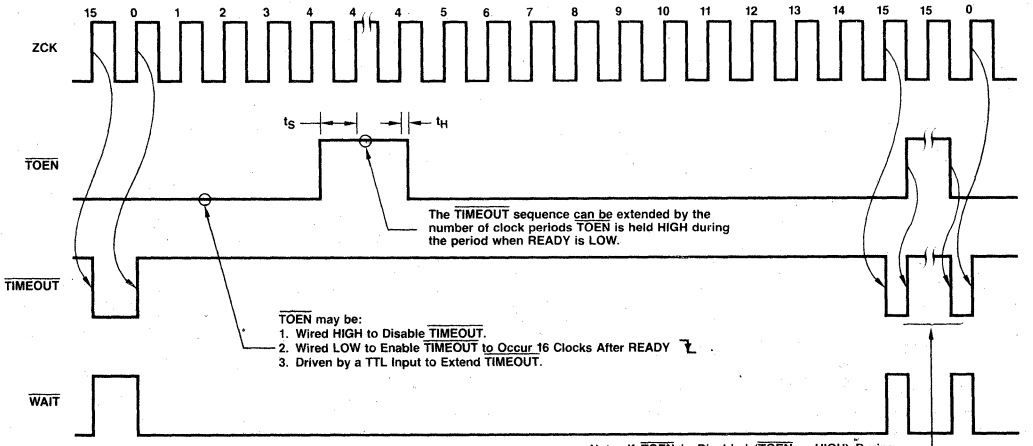
TYPICAL CRYSTAL SPEC

Mode	Fundamental AT cut
Resonance	Parallel or Series
Load	32pF (Net of 56pF C's shown + stray C)
Stability	±0.01% (or to user requirement)

$\overline{\text{WAIT}}$, $\overline{\text{TIMEOUT}}$ FUNCTION TABLE

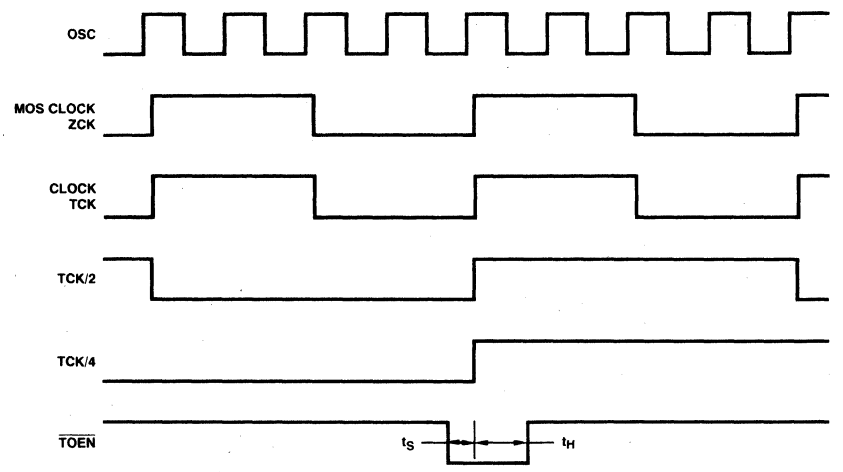
RUN/$\overline{\text{HALT}}$	SSNC	ST_3 ST_2 ST_1	READY	$\overline{\text{TOEN}}$	$\overline{\text{TIMEOUT}}$ COUNTER	$\overline{\text{TIMEOUT}}$	$\overline{\text{WAIT}}$
H	X	L L L	H	X	Cleared	H	H
		L L L	L	X	Cleared	H	H
		Any ST_i = H	H	L	Cleared	H	H
			L	H	Hold	H	L
			L	H	Count + 1 on ZCK ↓	H until 16 clocks after ready ↑, then LOW one ZCK period	L until 16 clocks after ready ↑, then LOW one ZCK period
L	L	X	X	X	Hold	H	L
	H						HIGH one ZCK period

$\overline{\text{TIMEOUT}}$ COUNTER TIMING



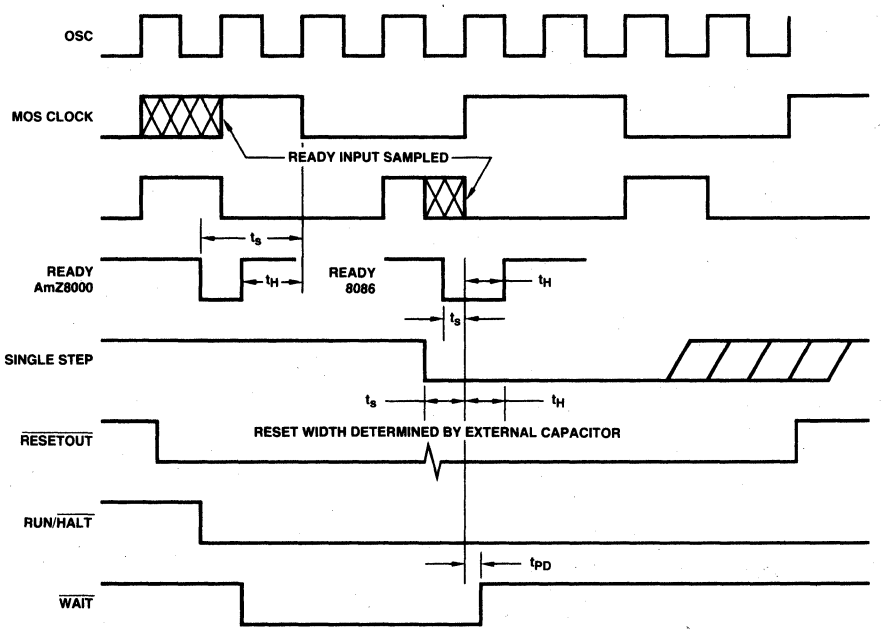
AMZ-027

Am8127 CLOCK OUTPUTS
DIVIDE BY 4 MODE (AmZ8000)



AMZ-024

Am8127 READY, WAIT, RESET, AND SINGLE STEP



AMZ-026

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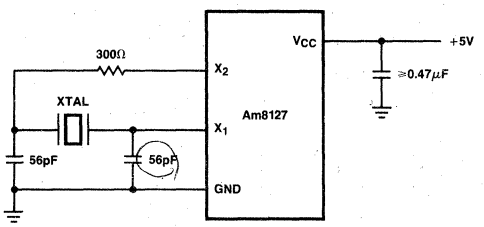
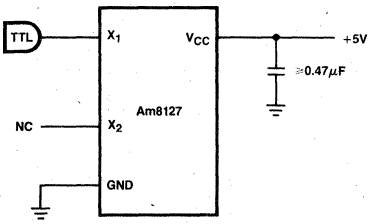
CRYSTAL CONTROLLED OSCILLATOR



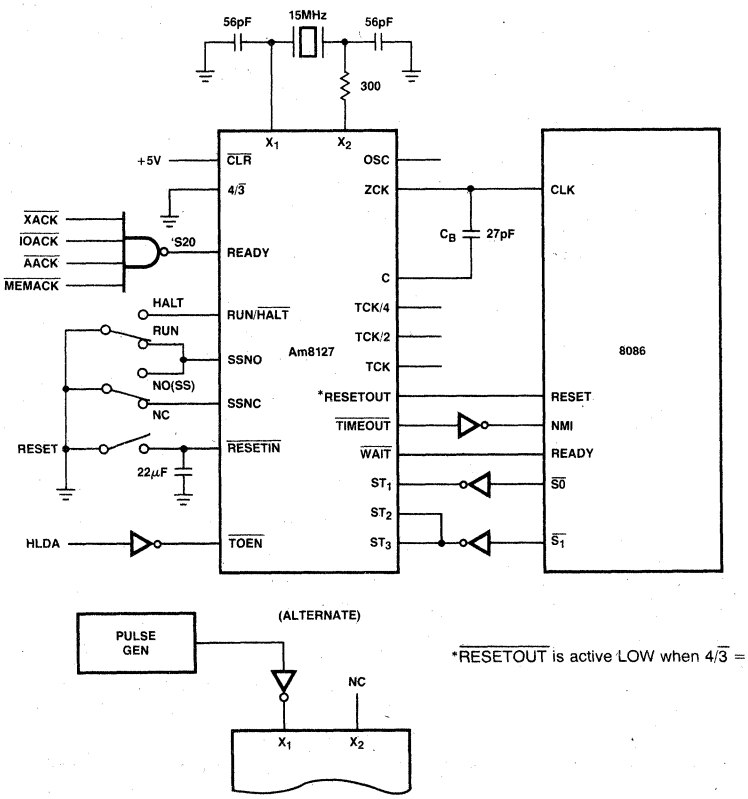
AMZ-028

EXTERNAL CLOCK DRIVE



AMZ-029

AmZ8000 APPLICATION
(50% Duty Cycle ZCK)

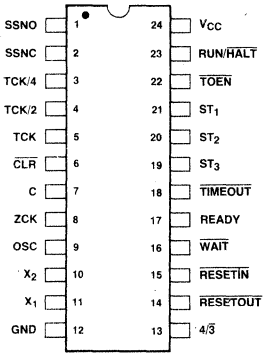


*$\overline{RESETOUT}$ is active LOW when 4/$\overline{3}$ = HIGH

AMZ-030

The typical operating configuration for Am8127 is shown above. The component values shown provide a 4MHz clock output for the AmZ8002 CPU. The 27pF capacitor from C to ZCK is a bootstrap to ensure clock rise to $V_{CC}-0.4V$ within the specified rise time. The 22μF reset capacitor is chosen to guarantee reset, plus adequate delay for reset during power-up with a slowly rising V_{CC} supply voltage. Ground SSNO if RUN/$\overline{HALT}$ or S-S isn't used.

CONNECTION DIAGRAM
Top View

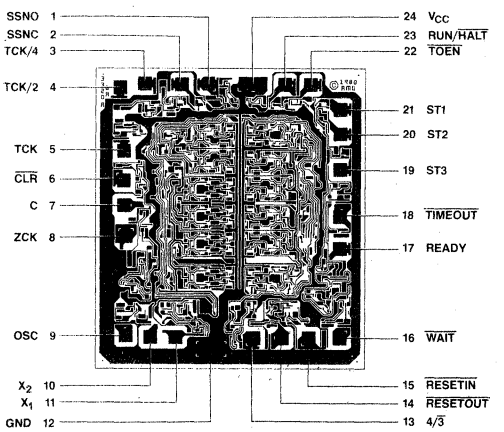


24 Pin 0.3" wide

Note: Pin 1 is marked for orientation.

AMZ-032

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.098" X 0.088"

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ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
Am8127DC	D-24-SLIM	C	C-1
Am8127DCB	D-24-SLIM	C	B-2 (Note 4)
Am8127DM	D-24-SLIM	M	C-3
Am8127DMB	D-24-SLIM	M	B-3
Am8127LC	L-28-1	C	C-1
Am8127LCB	L-28-1	C	B-2 (Note 4)
Am8127LM	L-28-1	M	C-3
Am8127LBM	L-28-1	M	B-3
Am8127XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
Am8127XM	Dice	M	

Notes: 1. D = Hermetic DIP, L = Chip Pak. Number following letter is number of leads.
2. C = 0 to +70°C, V_{CC} = 4.5 to 5.5V, M = −55 to +125°C, V_{CC} = 4.50 to 5.50V.
3. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.
4. 160 hour burn-in.

Am8212

Eight-Bit Input/Output Port

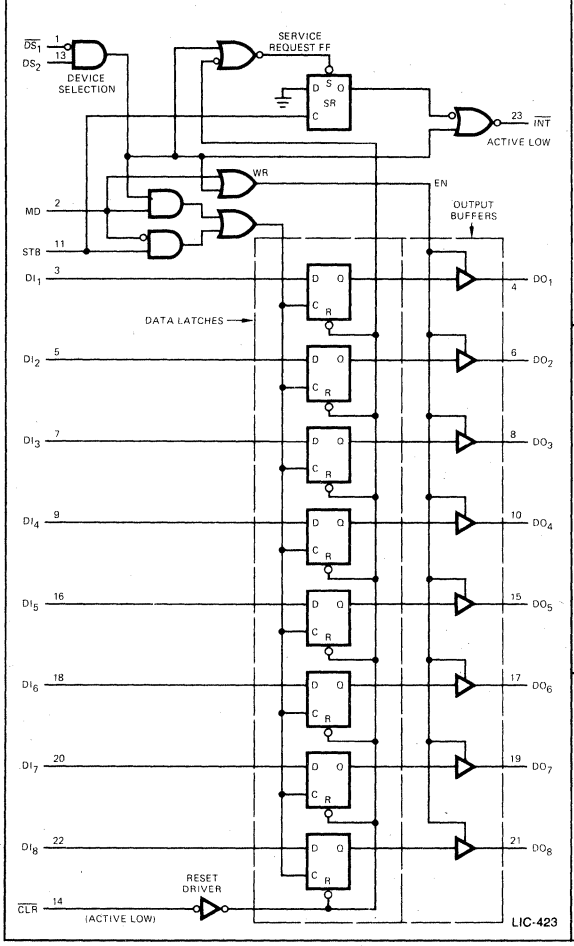
Distinctive Characteristics

- Fully parallel, 8-bit data register and buffer replacing latches, multiplexers and buffers needed in microprocessor systems.
- 4.0V output high voltage for direct interface to MOS microprocessors, such as the Am9080A family.
- Input load current 250μA max.
- Reduces system package count
- Available for operation over both commercial and military temperature ranges.
- Service request flip-flop for interrupt generation
- Three-state outputs sink 15mA
- Asynchronous register clear with clock over-ride

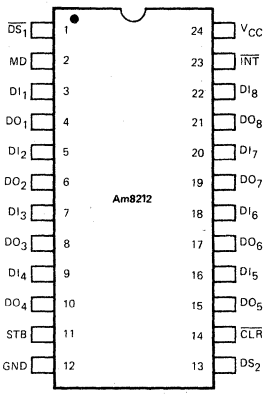
FUNCTIONAL DESCRIPTION

All of the principal peripheral and input/output functions of a Microcomputer System can be implemented with the Am8212. The Am8212 input/output port consists of an 8-latch with 3-state output buffers along with control and device selection logic, which can be used to implement latches, gated buffers or multiplexers.

LOGIC DIAGRAM



CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LIC-424

PIN DEFINITION

$DI_1 - DI_8$	DATA IN
$DO_1 - DO_8$	DATA OUT
$\overline{DS_1} - DS_2$	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	–55°C to +125°C	AM8212DM
Hermetic DIP	0°C to +70°C	D8212
Molded DIP	0°C to +70°C	P8212
Dice	0°C to +70°C	AM8212XC

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FUNCTIONAL DESCRIPTION (Cont'd)

Data Latch

The 8 flip-flops that make up the data latch are of a "D" type design. The output (Q) of the flip-flop will follow the data input (D) while the clock input (C) is high. Latching will occur when the clock (C) returns low.

The data latch is cleared by an asynchronous reset input ($\overline{CLR}$). (Note: Clock (C) Overrides Reset ($\overline{CLR}$)).

Output Buffer

The outputs of the data latch (Q) are connected to 3-state, non-inverting output buffers. These buffers have a common control line (EN); this control line either enables the buffer to transmit the data from the outputs of the data latch (Q) or disables the buffer, forcing the output into a high impedance state. (3-state). This high-impedance state allows the Am8212 to be connected directly onto the microprocessor bidirectional data bus.

Control Logic

The Am8212 has control inputs $\overline{DS_1}$, DS_2, MD and STB. These inputs are used to control device selection, data latching, output buffer state and service request flip-flop.

$\overline{DS_1}$, DS_2 (Device Select)

These 2 inputs are used for device selection. When $\overline{DS_1}$ is low and DS_2 is high ($\overline{DS_1} \cdot DS_2$) the device is selected. In the selected state the output buffer is enabled and the service request flip-flop (SR) is asynchronously set.

MD (Mode)

This input is used to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is high (output mode) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS_1} \cdot DS_2$).

When MD is low (input mode) the output buffer state is determined by the device selection logic ($\overline{DS_1} \cdot DS_2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

STB (Strobe)

This input is used as the clock (C) to the data latch for the input mode MD = 0) and to synchronously reset the service request flip-flop (SR).

Note that the SR flip-flop is negative edge triggered.

Service Request Flip-Flop

The SR flip-flop is used to generate and control interrupts in microcomputer systems. It is asynchronously set by the $\overline{CLR}$ input (active low). When the (SR) flip-flop is set it is in the non-interrupting state.

The output of the (SR) flip-flop (Q) is connected to an inverting input of a "NOR" gate. The other input to the "NOR" gate is non-inverting and is connected to the device selection logic ($\overline{DS_1} \cdot DS_2$). The output of the "NOR" gate ($\overline{INT}$) is active low (interrupting state) for connection to active low input priority generating circuits.

TRUTH TABLE

STB	MD	$\overline{DS_1} - DS_2$	Data Out Equals
0	0	0	Three-State
1	0	0	Three-State
0	1	0	Data Latch
1	1	0	Data Latch
0	0	1	Data Latch
1	0	1	Data In
0	1	1	Data In
1	1	1	Data In

CLR	$\overline{DS_1} - DS_2$	STB	SR*	$\overline{INT}$
0	0	0	1	1
0	1	0	1	0
1	1	↘	0	0
1	1	0	1	0
1	0	0	1	1
1	1	↘	1	0

$\overline{CLR}$ — Resets Data Latch
— Sets SR Flip-Flop (no effect on Output Buffer)
* Internal SR Flip-Flop

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage	−0.5V to +7.0V
Output Voltage	−0.5V to +7.0V
Input Voltages	−1.0V to +5.5V
Output Current (Each Output)	125mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

P8212, D8212 (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$
Am8212DM (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$

DC CHARACTERISTICS

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
I_F	Input Load Current ACK, DS_2, CR, $DI_1 - DI_8$ Inputs	$V_F = 0.45V$				−0.25	mA
I_F	Input Load Current MD Input	$V_F = 0.45V$				−0.75	mA
I_F	Input Load Current DS_1 Input	$V_F = 0.45V$				−1.0	mA
I_R	Input Leakage Current ACK, DS, CR, $DI_1 - DI_8$ Inputs	$V_R = 5.25V$				10	μA
I_R	Input Leakage Current MO Input	$V_R = 5.25V$				30	μA
I_R	Input Leakage Current DS_1 Input	$V_R = 5.25V$				40	μA
V_C	Input Forward Voltage Clamp	$I_C = -5.0mA$	COM'L			−1.0	Volts
			MIL			−1.2	
V_{IL}	Input LOW Voltage		COM'L			0.85	Volts
			MIL			0.80	
V_{IH}	Input HIGH Voltage			2.0			Volts
V_{OL}	Output LOW Voltage	$I_{OL} = 15mA$				0.45	Volts
V_{OH}	Output HIGH Voltage	$I_{OH} = -1.0mA$	COM'L	3.65	4.0		Volts
			MIL	3.3	4.0		
		$I_{OH} = -0.5mA$	MIL	3.4	4.0		
I_{SC}	Short Circuit Output Current	$V_O = 0V$		−15		−75	mA
$\|I_O\|$	Output Leakage Current High Impedance	$V_O = 0.45V/5.25V$				20	μA
I_{CC}	Power Supply Current	Note 2			90	130	mA

AC CHARACTERISTICS (Note 3)

Parameters	Description	Min.	Typ. (Note 1)	Max.	Units
t_{pw}	Pulse Width	30	8		ns
t_{pd}	Data to Output Delay		12	30	ns
t_{we}	Write Enable to Output Delay		18	40	ns
t_{set}	Data Set-up Time	15			ns
t_h	Data Hold Time	20			ns
t_r	Reset to Output Delay		18	40	ns
t_s	Set to Output Delay		15	30	ns
t_e	Output Enable/Disable Time		14	45	ns
t_c	Clear to Output Delay		25	55	ns

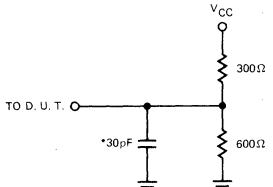
CAPACITANCE (Note 4)

$F = 1.0MHz$, $V_{BIAS} = 2.5V$, $V_{CC} = +5.0V$, $T_A = 25°C$

Parameters	Description	Typ.	Max.	Units
C_{IN}	DS_1 MD Input Capacitance	9.0	12	pF
C_{IN}	DS_2, CK, ACK, $DI_1 - DI_8$ Input Capacitance	5.0	9.0	pF
C_{OUT}	$DO_1 - DO_8$ Output Capacitance	8.0	12	pF

Notes: 1. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
2. CLR = STB = HIGH; $DS_1 = DS_2$ = MD = LOW; all data inputs are gound, all data outputs are open.
3. Conditions of Test: a) Input pulse amplitude = 2.5V
b) Input rise and fall times 5.0ns
c) Between 1.0V and 2.0V measurements made at 1.5V with 15mA and 30pF Test Load.
4. This parameter is sampled and not 100% tested.

TEST LOAD (15mA and 30pF)



*Including Jig and Probe Capacitance.

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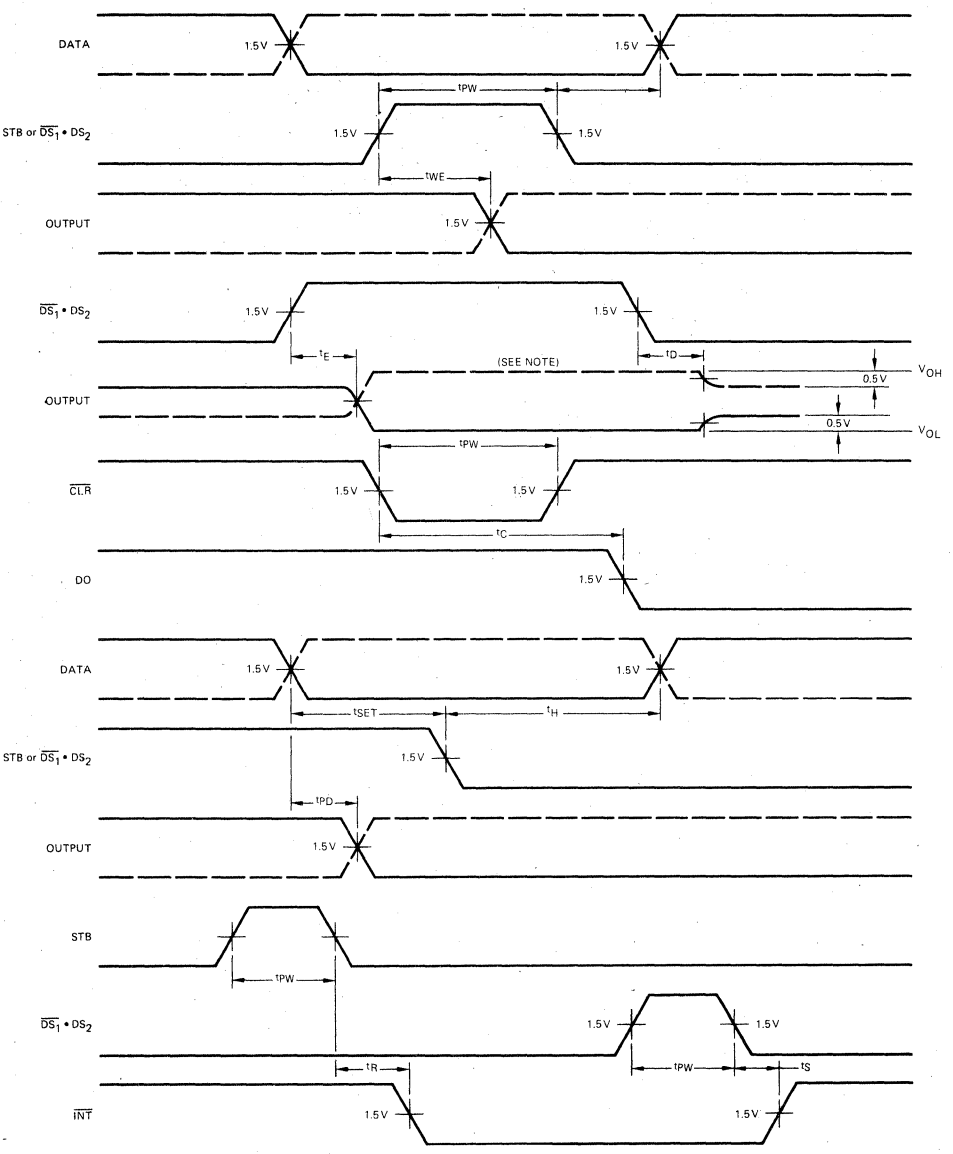
TIMING DIAGRAM



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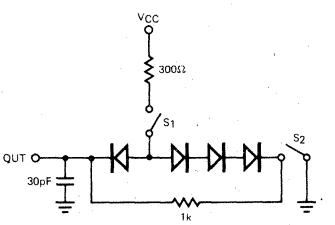
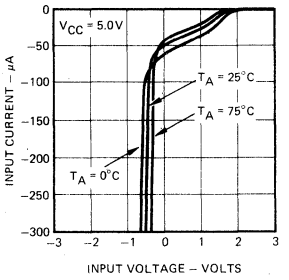
Note: Alternative Test Load.



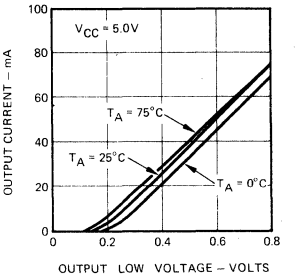
LIC-427

TYPICAL CHARACTERISTICS

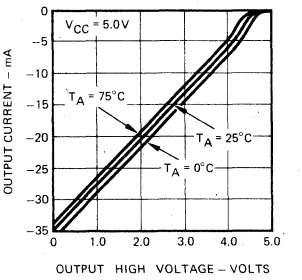
Input Current Versus Input Voltage



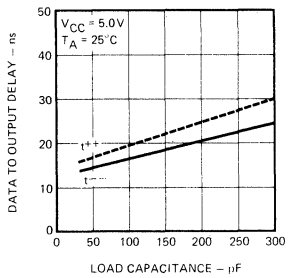
Output Current Versus Output LOW Voltage



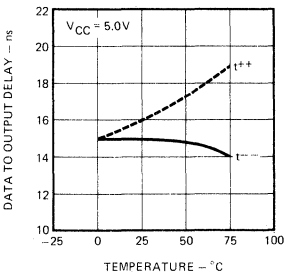
Output Current Versus Output HIGH Voltage



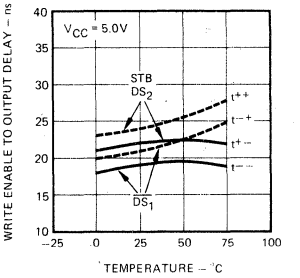
Data to Output Delay Versus Load Capacitance



Data to Output Delay Versus Temperature



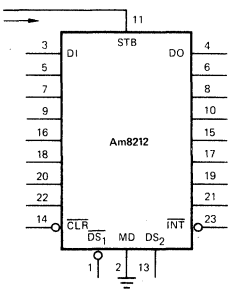
Write Enable to Output Delay Versus Temperature



LIC-428

LOGIC SYMBOLS

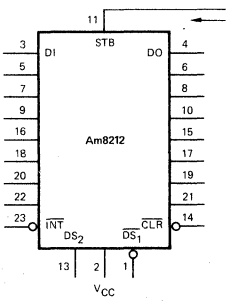
INPUT DEVICE



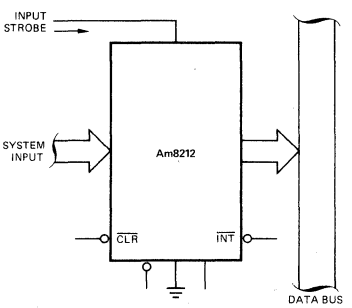
LIC-429

Detailed

OUTPUT DEVICE

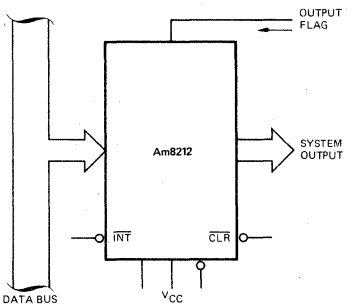


LIC-430



LIC-431

Symbolic



LIC-432

11

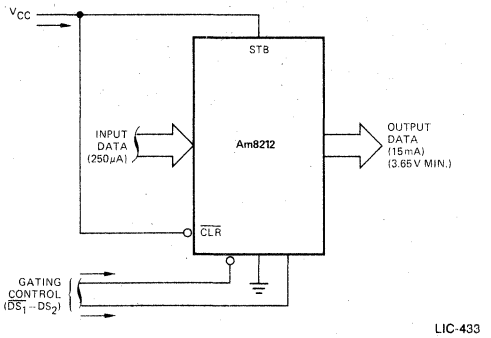
TYPICAL APPLICATIONS OF THE Am8212

GATED BUFFER (3-STATE)

By tying the mode signal low and the strobe input high, the data latch is acting as a straight through gate. The output buffers are then enabled from the device selection logic $\overline{DS_1}$ and DS_2.

When the device selection logic is false, the outputs are 3-state.

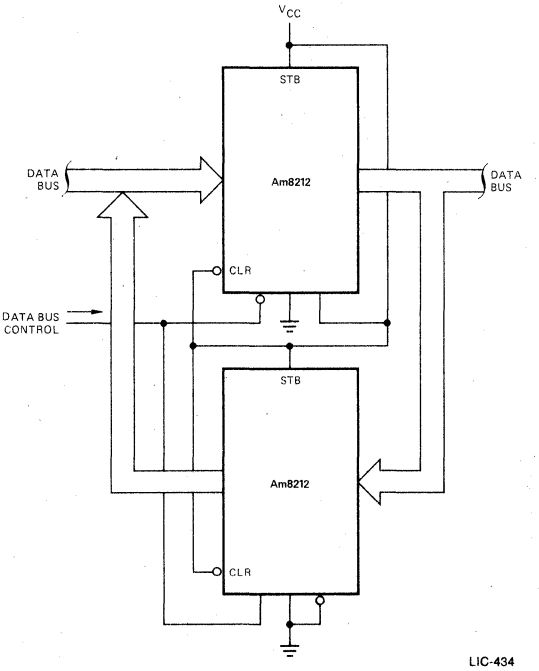
When the device selection logic is true, the input data from the system is directly transferred to the output.



LIC-433

Bi-Directional Bus Driver

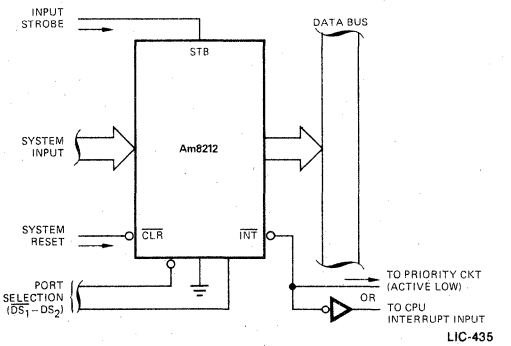
Two Am8212s wired back to back can be used as a symmetrical drive, bi-directional bus driver. The devices are controlled by the data bus input control which is connected to $\overline{DS_1}$ on the first Am8212 and to DS_2 on the second. While one device is active, and acting as a straight through buffer the other is in its 3-state mode.



LIC-434

Interrupting Input Port

The Am8212 accepts a strobe from the system input source, which in turn clears the service request flip-flop and interrupts the processor. The processor then goes through a service routine, identifies the port, and causes the device selection logic to go true – enabling the system input data onto the data bus.

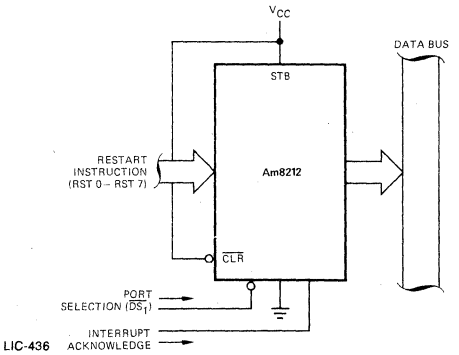


LIC-435

TYPICAL APPLICATIONS OF THE Am8212 (Cont'd)

Interrupt Instruction Port

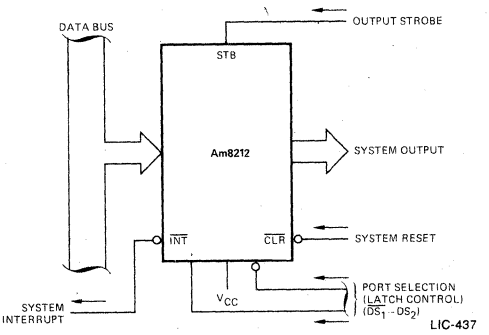
The Am8212 can be used to gate the interrupt instruction, normally RESTART instructions, onto the data bus. The device is enabled from the interrupt acknowledge signal from the microprocessor and from a port selection signal. This signal is normally tied to ground. ($\overline{DS_1}$ could be used to multiplex a variety of interrupt instruction ports onto a common bus.)



LIC-436

Output Port (With Hand-Shaking)

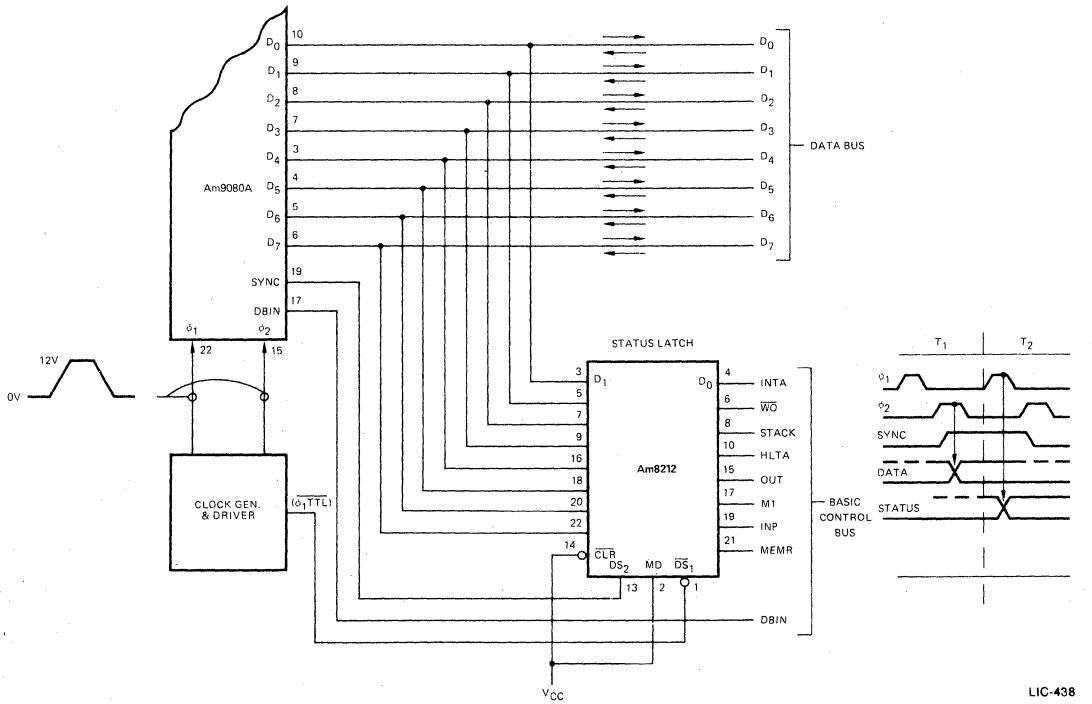
The Am8212 is used to transmit data from the data bus to a system output. The output strobe could be a hand-shaking signal such as "reception of data" from the device that the system is outputting to. It in turn, can interrupt the system signifying the reception of data. The selection of the port comes from the device selection logic. ($\overline{DS_1} - DS_2$.)



LIC-437

Am9080A Status Latch

The input to the Am8212 latch comes directly from the Am9080A data bus. Timing shows that when the SYNC signal is true ($\overline{DS_1}$ input), and $\phi 1$ is true, ($\overline{DS_1}$ input) then the status data will be latched into the Am8212. The mode signal is tied high so that the output on the latch is active and enabled all the time.



LIC-438

Am8216 • Am8226

Four-Bit Parallel Bidirectional Bus Driver

Distinctive Characteristics

- Data bus buffer driver for 8080 type CPU's
- Low input load current – 0.25mA maximum
- High output drive capability for driving system data bus – 50mA at 0.5V
- Am8216 has non-inverting outputs
- Output high voltage compatible with direct interface to MOS
- Three-state outputs
- Advanced Schottky processing
- Available in military and commercial temperature range
- Am8226 has inverting outputs

FUNCTIONAL DESCRIPTION

The Am8216 and Am8226 are four-bit, bi-directional bus drivers for use in bus oriented applications. The non-inverting Am8216, and inverting Am8226 drivers are provided for flexibility in system design.

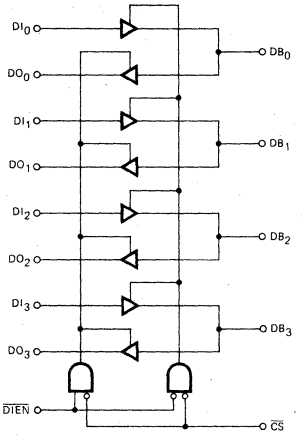
Each buffered line of the four bit driver consists of two separate buffers that are three-state to achieve direct bus interface and bi-directional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB), this side is used to interface to the system side components such as memories, I/O, etc., because its interface is TTL compatible and it has high drive (50mA). On the other side of the driver the inputs and outputs are separated to provide maximum flexibility. Of course, they can be tied together so that the driver can be used to buffer a true bi-directional bus. The DO outputs on this side of the driver have a special high voltage output drive capability so that direct interface to the 8080 type CPUs is achieved with an adequate amount of noise immunity.

The $\overline{CS}$ input is a device enable. When it is "high" the output drivers are all forced to their high-impedance state. When it is a "LOW" the device is enabled and the direction of the data flow is determined by the $\overline{DIEN}$ input.

The $\overline{DIEN}$ input controls the direction of data flow which is accomplished by forcing one of the pair of buffers into its high impedance state and allowing the other to transmit its data. A simple two gate circuit is used for this function.

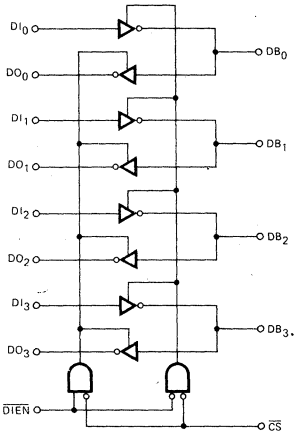
LOGIC DIAGRAMS

Am8216



LIC-439

Am8226



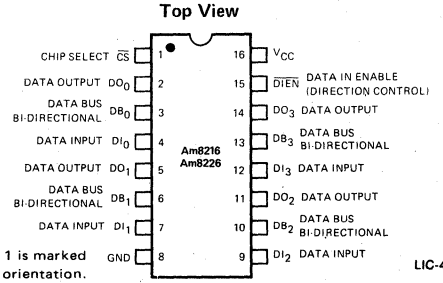
LIC-440

ORDERING INFORMATION

Package Type	Temperature Range	Am8216 Order Number	Am8226 Order Number
Hermetic DIP	–55°C to +125°C	MD8216	MD8226
Hermetic DIP	0°C to +70°C	D8216	D8226
Molded DIP	0°C to +70°C	P8216	P8226
Dice	0°C to +70°C	AM8216XC	AM8226XC

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

LIC-441

MAXIMUM RATINGS (Above which the useful life may be impaired)

Temperature (Ambient) Under Bias	–55°C to +125°C
Storage Temperature	–65°C to +150°C
All Output and Supply Voltages	–0.5 V to +7.0 V
All Input Voltages	–1.0 V to +5.5 V
Output Currents	125 mA

Am8216 AND Am8226 MILITARY ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (–55°C to +125°C)

The following conditions apply unless otherwise specified:

MD8216, MD8226 (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$

DC CHARACTERISTICS

Parameters	Description		Test Conditions		Min.	Typ. (Note 1)	Max.	Units
I_{F1}	Input Load Current $\overline{DIEN}$, $\overline{CS}$		$V_F = 0.45$			–0.15	–0.5	mA
I_{F2}	Input Load Current All Other Inputs		$V_F = 0.45$			–0.08	–0.25	mA
I_{R1}	Input Leakage Current $\overline{DIEN}$, $\overline{CS}$		$V_R = 5.5V$				80	μA
I_{R2}	Input Leakage Current DI Inputs		$V_R = 5.5V$				40	μA
V_C	Input Forward Voltage Clamp		$I_C = -5.0mA$				–1.2	Volts
V_{IL}	Input LOW Voltage	Am8216					0.95	Volts
		Am8226					0.9	
V_{IH}	Input HIGH Voltage				2.0			Volts
I_O	Output Leakage Current (Three-State)	DO	$V_O = 0.45V/5.5V$				20	μA
		DB					100	
I_{CC}	Power Supply Current	Am8216				95	130	mA
		Am8226				85	120	
V_{OL1}	Output LOW Voltage		DO Outputs $I_{OL} = 15mA$ DB Outputs $I_{OL} = 25mA$			0.3	0.45	Volts
V_{OL2}	Output LOW Voltage		DB Outputs $I_{OL} = 45mA$			0.5	0.6	Volts
V_{OH1}	Output HIGH Voltage		DO Outputs	$I_{OH} = -0.5mA$	3.4	4.0		Volts
				$I_{OH} = -2.0mA$	2.4			
V_{OH2}	Output HIGH Voltage		DB Outputs $I_{OH} = -5.0mA$		2.4	3.0		Volts
I_{OS}	Output Short Circuit Current		DO Outputs ≅ 0V, $V_{CC} = 5.0V$		–15	–35	–65	mA
			DB Outputs = 0V, $V_{CC} = 5.0V$		–30	–75	–120	

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AC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (–55°C to +125°C)

Parameters	Description		Test Conditions	Min.	Typ. (Note 1)	Max.	Units
t_{PD1}	Input to Output Delay DO Outputs		$C_L = 30pF$, $R_1 = 300\Omega$, $R_2 = 600\Omega$		15	25	ns
t_{PD2}	Input to Output Delay DB Outputs	Am8216	$C_L = 300pF$, $R_1 = 90\Omega$, $R_2 = 180\Omega$		20	33	ns
		Am8226			16	25	
t_E	Output Enable Time	Am8216	Note 2		45	75	ns
		Am8226	Note 3		35	62	
t_D	Output Disable Time	Am8216	Note 4		20	40	ns
		Am8226			16	38	

Am8216 AND Am8226 COMMERCIAL
ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (0°C to +70°C)

The following conditions apply unless otherwise specified:

D8216, D8226, P8216, P8226 (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$

DC CHARACTERISTICS

Parameters	Description		Test Conditions	Min.	Typ. (Note 1)	Max.	Units
I_{F1}	Input Load Current $\overline{DIEN}$, $\overline{CS}$		$V_F = 0.45$		−0.15	−0.5	mA
I_{F2}	Input Load Current All Other Inputs		$V_F = 0.45$		−0.08	−0.25	mA
I_{R1}	Input Leakage Current $\overline{DIEN}$, $\overline{CS}$		$V_R = 5.25V$			20	μA
I_{R2}	Input Leakage Current DI Inputs		$V_R = 5.25V$			10	μA
V_C	Input Forward Voltage Clamp		$I_C = -5.0mA$			−1.0	Volts
V_{IL}	Input LOW Voltage					0.95	Volts
V_{IH}	Input HIGH Voltage			2.0			Volts
$\|I_O\|$	Output Leakge Current (Three-State)	DO	$V_O = 0.45V/5.5V$			20	μA
		DB				100	
I_{CC}	Power Supply Current	Am8216			95	130	mA
		Am8226			85	120	
V_{OL1}	Output LOW Voltage		DB Outputs $I_{OL} = 15mA$ DB Outputs $I_{OL} = 25mA$		0.3	0.45	Volts
V_{OL2}	Output LOW Voltage	Am8216	DB Outputs $I_{OL} = 55mA$		0.5	0.6	Volts
		Am8226	DB Outputs $I_{OL} = 50mA$		0.5	0.6	
V_{OH1}	Output HIGH Voltage		DO Outputs $I_{OH} = -1.0mA$ COM'L	3.65	4.0		Volts
V_{OH2}	Output HIGH Voltage		DB Outputs $I_{OH} = -10mA$	2.4	3.0		Volts
I_{OS}	Output Short Circuit Current		DO Outputs ≅ 0V	−15	−35	−65	mA
			DB Outputs $V_{CC} = 5.0V$	−30	−75	−120	

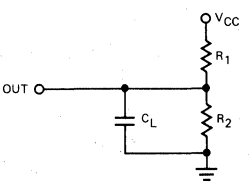
AC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (0°C to +70°C)

Parameters	Description		Test Conditions	Min.	Typ. (Note 1)	Max.	Units
t_{PD1}	Input to Output Delay DO Outputs		$C_L = 30pF$, $R_1 = 300\Omega$, $R_2 = 600\Omega$		15	25	ns
t_{PD2}	Input to Output Delay DB Outputs	Am8216	$C_L = 300pF$, $R_1 = 90\Omega$, $R_2 = 180\Omega$		20	30	ns
		Am8226			16	25	
t_E	Output Enable Time	Am8216	Note 2		45	65	ns
		Am8226	Note 3		35	54	
t_D	Output Disable Time		Note 4		20	35	ns

TEST CONDITIONS

Input pulse amplitude of 2.5V.
Input rise and fall times of 5.0ns between 1.0 and 2.0 volts.
Output loading is 5.0mA and 10pF.
Speed measurements are made at 1.5V levels.

TEST LOAD CIRCUIT



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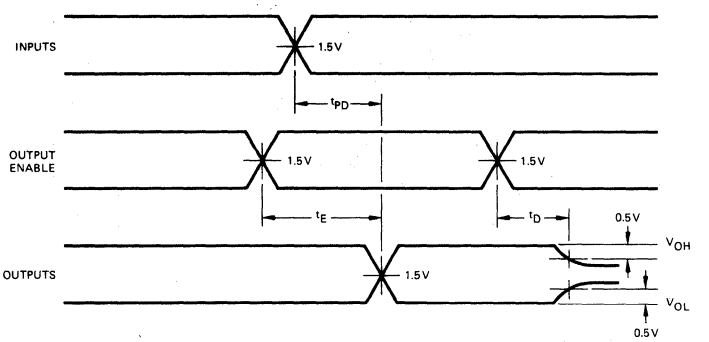
CAPACITANCE (Note 5)

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
C_{IN}	Input Capacitance	V_{BIAS} = 2.5V, V_{CC} = 5.0V T_A = 25°C, f = 1.0MHz		4.0	8.0	pF
C_{OUT1}	Output Capacitance			6.0	10	pF
C_{OUT2}	Output Capacitance			13	18	pF

Notes: 1. Typical values are for T_A = 25°C, V_{CC} = 5.0V.
2. DO outputs, C_L = 30pF, R_1 = 300/10kΩ, R_2 = 180/1.0kΩ; DB outputs, C_L = 300pF, R_1 = 90/10kΩ, R_2 = 180/1.0kΩ.
3. DO outputs, C_L = 30pF, R_1 = 300/10kΩ, R_2 = 600/1.0kΩ; DB outputs, C_L = 300pF, R_1 = 90/10kΩ, R_2 = 180/1.0kΩ.
4. DO outputs, C_L = 5.0pF, R_1 = 300/10kΩ, R_2 = 600/1.0kΩ; DB outputs, C_L = 5.0pF, R_1 = 90/10kΩ, R_2 = 180/1.0kΩ.
5. This parameter is periodically sampled and not 100% tested.

SWITCHING WAVEFORMS



LIC-443

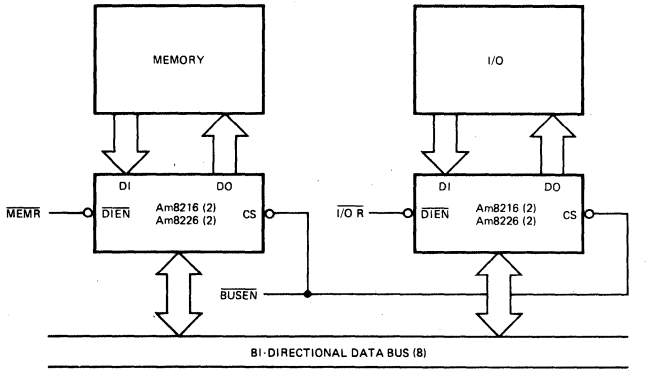
FUNCTION TABLE

$\overline{DIEN}$	$\overline{CS}$		8216 DB	8216 DO	8226 DB	8226 DO
L	L	DI ⇒ DB	DI	Z	$\overline{DI}$	Z
H	L	DB ⇒ DO	Z	DB	Z	$\overline{DB}$
L	H		Z	Z	Z	Z
H	H		Z	Z	Z	Z

H = HIGH
L = LOW

LIC-444

TYPICAL APPLICATION

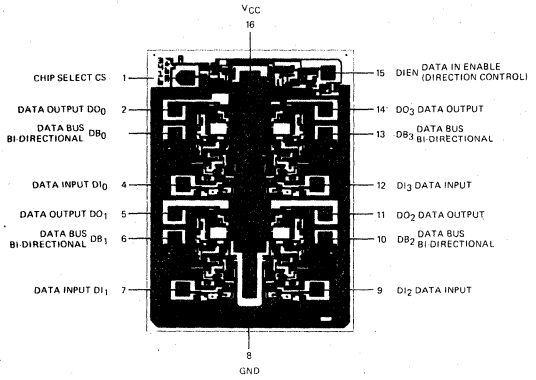


MEMORY AND I/O INTERFACE TO A BI-DIRECTIONAL BUS

LIC-445

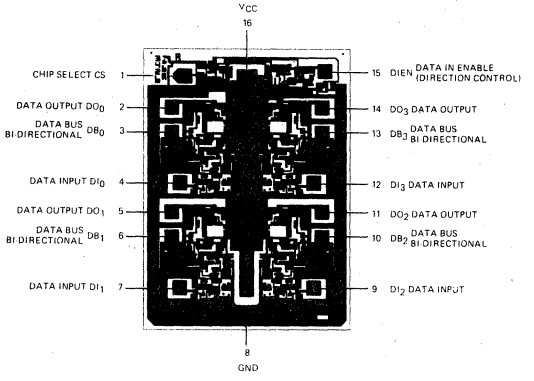
Metallization and Pad Layout

Am8216



DIE SIZE 0.066" X 0.090"

Am8226



DIE SIZE 0.066" X 0.090"

Am8224

Clock Generator and Driver for 8080A Compatible Microprocessors

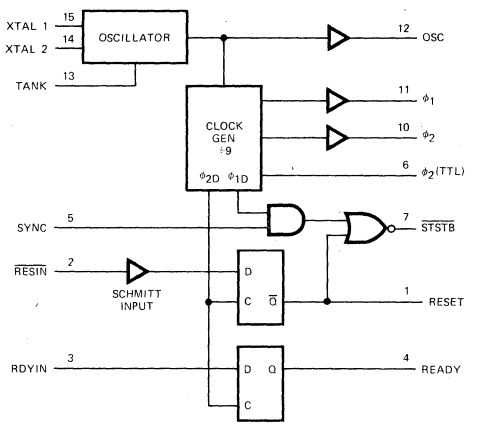
Distinctive Characteristics

- Single chip clock generator/driver for 8080A compatible CPU
- Power-up reset for CPU
- Ready synchronizing flip-flop
- Status strobe signal
- Oscillator output for external system timing
- Am8224-4 version available for use with 1μsec instruction cycle of Am9080A-4
- Available for operation over both commercial and military temperature ranges
- Crystal controlled for stable system operation
- Reduces system package count
- Advanced Schottky processing

FUNCTIONAL DESCRIPTION

The Am8224 is a single chip Clock Generator/Driver for the Am9080A and 8080A CPU. It contains a crystal-controlled oscillator, a "divide by nine" counter, two high-level drivers and several auxiliary logic functions, including a power-up reset, status strobe and synchronization of ready. Also provided are TTL compatible oscillator and ϕ_2 outputs for external system timing. The Am8224 provides the designer with a significant reduction of packages used to generate clocks and timing for the Am9080A or 8080A for both commercial and military temperature range applications. A high speed version, the Am8224-4, is available for use with the high speed Am9080A-4.

LOGIC DIAGRAM



LIC-619

ORDERING INFORMATION

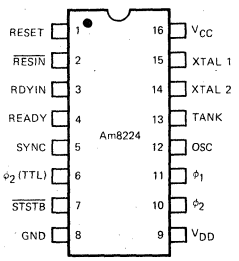
Package Type	Temperature Range	Order Number
Hermetic DIP	−55°C to +125°C	AM8224DM
Hermetic DIP	0°C to +70°C	D8224
Molded DIP	0°C to +70°C	AM8224PC
Dice	0°C to +70°C	AM8224XC
Hermetic DIP	0°C to +70°C	AM8224-4DC*

*For use with Am9080A-4 with clock period between 250ns and 320ns.

PIN DEFINITION

XTAL 1	CONNECTIONS FOR CRYSTAL
XTAL 2	
TANK	USED WITH OVERTONE XTAL
OSC	OSCILLATOR OUTPUT
ϕ_2(TTL)	ϕ_2 CLK (TTL LEVEL)
V_{CC}	+5.0V
V_{DD}	+12V
GND	0V
$\overline{\text{RESIN}}$	RESET INPUT
RESET	RESET OUTPUT
RDYIN	READY INPUT
READY	READY OUTPUT
SYNC	SYNC INPUT
$\overline{\text{STSTB}}$	STATUS STB (ACTIVE LOW)
ϕ_1	Am9080A/8080A CLOCKS
ϕ_2	

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation. LIC-620

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	
V_{CC}	7.5V
V_{DD}	15V
Maximum Output Current ϕ_1 and ϕ_2 (Note 1)	100mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

The Following Conditions Apply Unless Otherwise Noted:

Am8224XC, Am8224-4XC (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ $V_{DD} = 12V \pm 5\%$
Am8224XC (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ $V_{DD} = 12V \pm 10\%$

Parameters	Description	Test Conditions		Min.	Typ. (Note 2)	Max.	Units
I_F	Input Current Loading	$V_F = 0.45V$				−0.25	mA
I_R	Input Leakage Current	$V_R = 5.25V$				10	μA
V_C	Input Forward Clamp Voltage	$I_C = -5.0mA$	COM'L			−1.0	Volts
			MIL			−1.2	
V_{IL}	Input LOW Voltage	$V_{CC} = 5.0V$				0.8	Volts
V_{IH}	Input HIGH Voltage	Reset input	COM'L	2.6	2.2		Volts
			MIL	2.8	2.2		
		All other inputs		2.0			
V_{IH}-V_{IL}	$\overline{RESIN}$ Input Hysteresis	$V_{CC} = 5.0V$		0.25	0.5		Volts
V_{OL}	Output LOW Voltage	(ϕ_1, ϕ_2), Ready, Reset, $\overline{STSTB}$ $I_{OL} = 2.5mA$				0.45	Volts
		All other inputs $I_{OL} = 15mA$				0.45	
V_{OH}	Output HIGH Voltage	ϕ_1, ϕ_2; $I_{OH} = -100\mu A$	COM'L	9.4	11		Volts
			MIL	$V_{DD}-1.6V$	$V_{DD}-1.0V$		
		READY, RESET; $I_{OH} = -100\mu A$	COM'L	3.6	4.0		
			MIL	3.35	4.0		
		All other outputs; $I_{OH} = -1.0mA$		2.4	3.0		
I_{SC}	Output Short Circuit Current (All Low Voltage Outputs Only)	$V_O = 0V$ $V_{CC} = 5.0V$		−10		−60	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 3)			70	115	mA
I_{DD}	Power Supply Current	V_{DD} = MAX.			5.0	12	mA

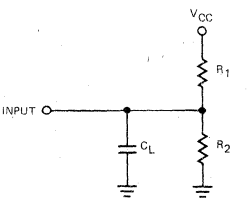
Notes: 1. Caution: ϕ_1 and ϕ_2 outputs do not have short circuit protection.
2. Typical limits are at $V_{CC} = 5.0V$, $V_{DD} = 12V$, 25°C ambient and maximum loading.
3. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.

CRYSTAL REQUIREMENTS

Tolerance: .005% at 0°C - 70°C
Resonance: Series (Fundamental)*
Load Capacitance: 20-35pF
Equivalent Resistance: 75-20 ohms
Power Dissipation (Min): 4mW

*With frequency in excess of 18MHz use 3rd overtone XTALs and tank circuit.

TEST CIRCUIT



LIC-621

AC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am8224XM Min.	Am8224XM Typ.	Am8224XM Max.	Am8224XC Min.	Am8224XC Typ.	Am8224XC Max.	Am8224-4XC (Note 2) Min.	Am8224-4XC (Note 2) Typ.	Am8224-4XC (Note 2) Max.	Units
$t_{\phi 1}$	ϕ_1 Pulse Width	C_L=20pF to 50pF	$\frac{2t_{CY}}{9}-23ns$			$\frac{2t_{CY}}{9}-20ns$			45			ns
$t_{\phi 2}$	ϕ_2 Pulse Width		$\frac{5t_{CY}}{9}-35ns$			$\frac{5t_{CY}}{9}-35ns$			110			
t_{D1}	ϕ_1 to ϕ_2 Delay		0			0			0			
t_{D2}	ϕ_2 to ϕ_1 Delay		$\frac{2t_{CY}}{9}-17ns$			$\frac{2t_{CY}}{9}-14ns$			35			
t_{D3}	ϕ_1 to ϕ_2 Delay		$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9}+22ns$	$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9}+20ns$	55		76	
t_r	ϕ_1 and ϕ_2 Rise Time				20			20			20	
t_f	ϕ_1 and ϕ_2 Fall Time				20			20			20	
$t_{D\phi 2}$	ϕ_2 to ϕ_2(TTL) Delay	ϕ_2(TTL), C_L = 30pF R_1 = 300Ω R_2 = 600Ω	−20		15	−20		15	−20		15	ns
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	$\overline{STSTB}$, C_L = 15pF, R_1 = 2.0kΩ R_2 = 4.0kΩ	$\frac{6t_{CY}}{9}-33ns$		$\frac{6t_{CY}}{9}$	$\frac{6t_{CY}}{9}-30ns$		$\frac{6t_{CY}}{9}$	137		167	ns
t_{PW}	$\overline{STSTB}$ Pulse Width		$\frac{t_{CY}}{9}-18ns$			$\frac{t_{CY}}{9}-15ns$			18			
t_{DRS}	RDYIN Set-up Time to Status Strobe		$50ns-\frac{4t_{CY}}{9}$			$50ns-\frac{4t_{CY}}{9}$			−61			
t_{DRH}	RDYIN Hold Time After STSTB		$\frac{4t_{CY}}{9}$			$\frac{4t_{CY}}{9}$			111			
t_{DR}	RDYIN or RESIN to ϕ_2 Delay	Ready and Reset C_L = 10pF R_1 = 2.0kΩ R_2 = 4.0kΩ	$\frac{4t_{CY}}{9}-25ns$			$\frac{4t_{CY}}{9}-25ns$			86			ns
t_{CLK}	CLK Period			$\frac{t_{CY}}{9}$			$\frac{t_{CY}}{9}$			28		
$f_{Max.}$	Maximum Oscillating Frequency		27			28.12			36			MHz
C_{in}	Input Capacitance	V_{CC} = 5.0V V_{DD} = 12V V_{BIAS} = 2.5V f = 1.0MHz			8.0			8.0			8.0	pF

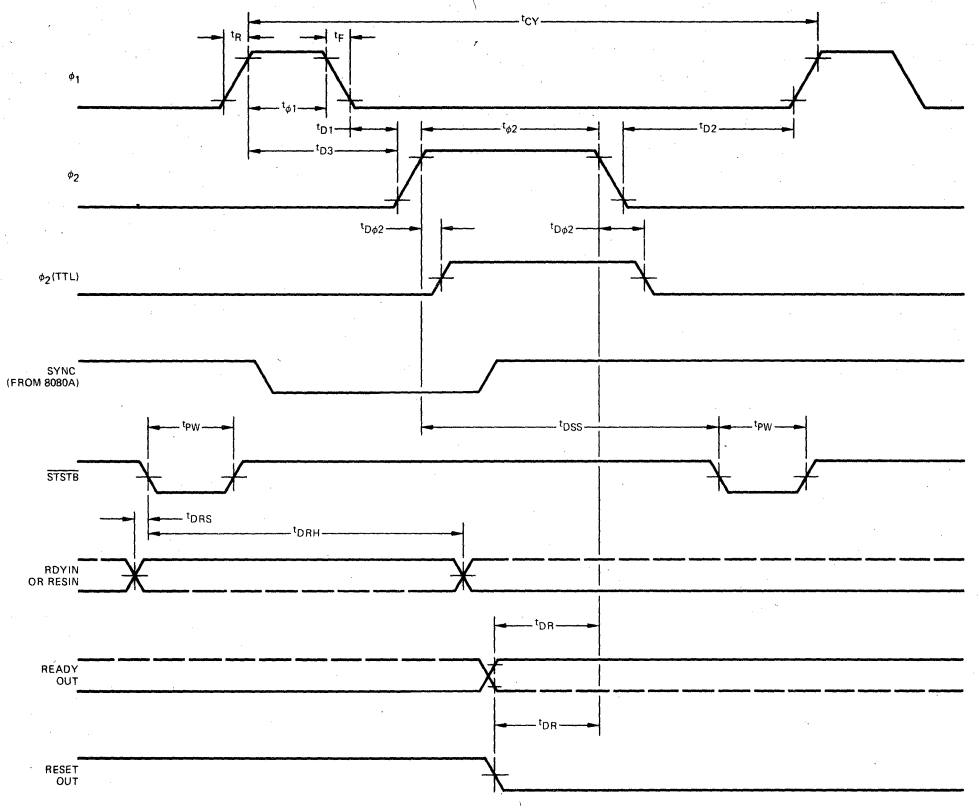
AC CHARACTERISTICS (For t_{CY} = 488.28ns)

T_A = 0°C to +70°C V_{CC} = +5.0V ±5% V_{DD} = +12V ±5%

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
$t_{\phi 1}$	ϕ_1 Pulse Width	ϕ_1 and ϕ_2 Loaded C_L = 20 to 50pF	89			ns
$t_{\phi 2}$	ϕ_2 Pulse Width		236			ns
t_{D1}	Delay ϕ_1 to ϕ_2		0			ns
t_{D2}	Delay ϕ_2 to ϕ_1		95			ns
t_{D3}	Delay ϕ_1 to ϕ_2 Leading Edges		109		129	ns
t_r	Output Rise Time				20	ns
t_f	Output Fall Time				20	ns
t_{DSS}	ϕ_2 to $\overline{STSTB}$ Delay	Ready and Reset Loaded C_L = 20 to 50pF R_1 = 2.0kΩ , R_2 = 4.0kΩ	296		326	ns
$t_{D\phi 2}$	ϕ_2 to ϕ_2(TTL) Delay		−20		15	ns
t_{PW}	Status Strobe Pulse Width		40			ns
t_{DRS}	RDYIN Set-up Time to $\overline{STSTB}$		−167			ns
t_{DRH}	RDYIN Hold Time After $\overline{STSTB}$		217			ns
t_{DR}	Ready or Reset to ϕ_2 Delay		192			ns
FREQ	Oscillator Frequency				18.432	MHz

Notes: 1. All measurements referenced to 1.5V unless specified otherwise.
2. Am8224-4 parameter limits are given for t_{CY} = 250ns or an oscillating frequency of 36MHz. Between 28.12MHz and 36MHz min. and max. limits should be ratioed between the calculated Am8224XC limits at 28.12MHz and the given 36MHz parameter limits.

SWITCHING WAVEFORMS



Voltage measurement points: ϕ_1, ϕ_2 Logic "0" = 1.0 V, Logic "1" = 8.0 V.
All other signals measured at 1.5 V.

LIC-622

Oscillator

The oscillator circuit derives its basic operating frequency from an external, series resonant, fundamental mode crystal. Two inputs are provided for the crystal connections (XTAL1, XTAL2).

The selection of the external crystal frequency depends mainly on the speed at which the CPU is to be run. Basically, the oscillator operates at 9 times the desired processor speed.

The formula to determine the crystal frequency is:

$$f(XTAL) = \frac{1}{t_{CY}} \text{ times } 9$$

When using crystals above 10MHz a small amount of frequency "trimming" is necessary to produce the desired frequency. The addition of a selected capacitance (20pF – 30pF) in series with the crystal will accomplish this function.

Another input to the oscillator is TANK. This input allows the use overtone mode crystals. This type of crystal generally has a much lower output at its rated frequency and has a tendency to oscillate at its fundamental.

To avoid the unwanted oscillation and increase the desired frequency output it is necessary to provide a parallel tuned resonant circuit of low impedance. The external LC network is connected to the TANK input and is AC coupled. See typical application with Am8228 and Am9080A in Figure 2.

The formula for the LC network is:

$$F = \frac{1}{2\pi\sqrt{LC}}$$

The output of the oscillator is buffered and brought out on OSC (pin 12) so that other system timing signals can be derived from this stable, crystal-controlled source.

Clock Generator

The Clock Generator consists of a synchronous "divide by nine" counter and the associated decode gating to create the waveforms of the two clocks and auxiliary timing signals.

The waveforms generated by the decode gating follow a simple 2-5-2 digital pattern. See Figure 2. The clocks generated; ϕ_1 and ϕ_2, can best be thought of as consisting of "units" based on the oscillator frequency. Assume that one "unit" equals the period of the oscillator frequency. By multiplying the number of "units" that are contained in a pulse width or delay, times the period of the oscillator frequency, the approximate time in nanoseconds can be derived.

The outputs of the clock generator are connected to two high level drivers for direct interface to the CPU. A TTL level phase 2 is also brought out ϕ_2 (TTL) for external timing purposes. It is especially useful in DMA dependent activities. This signal is used to gate the requesting device onto the bus once the CPU issues the Hold Acknowledgement (HLDA).

Several other signals are also generated internally so that optimum timing of the auxiliary flip-flops and status strobe ($\overline{\text{STSTB}}$) is achieved.

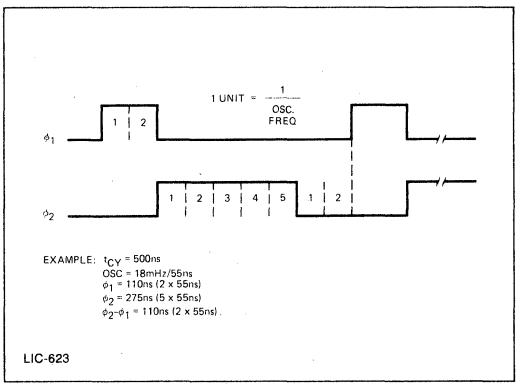


Figure 1. Clock Generator Waveforms.

$\overline{\text{STSTB}}$ (Status Strobe)

At the beginning of each machine cycle the CPU issues status information on its data bus. This information tells what type of action will take place during that machine cycle. By bringing in the SYNC signal from the CPU, and gating it with an internal timing signal (ϕ_{1A}), an active low strobe can be derived that occurs at the start of each machine cycle at the earliest possible moment that status data is stable on the bus. The $\overline{\text{STSTB}}$ signal connects directly to the Am8228 System Controller.

The power-on Reset also generates $\overline{\text{STSTB}}$, but of course, for a longer period of time. This feature allows the Am8228 to be automatically reset without additional pins devoted for this function.

Power-On Reset and Ready Flip-Flops

A common function in microcomputer systems is the generation of an automatic system reset and start-up upon initial power-on. The Am8224 has a built-in feature to accomplish this feature.

An external RC network is connected to the $\overline{\text{RESIN}}$ input. The slow transition of the power supply rise is sensed by an internal Schmitt Trigger. This circuit converts the slow transition into a clean, fast edge when its input level reaches a predetermined value. The output of the Schmitt Trigger is connected to a "D" type flip-flop that is clocked with ϕ_{2D} (an internal timing signal). The flip-flop is synchronously reset and an active high level that complies with the microprocessor input spec is generated. For manual switch type system Reset circuits, an active low switch closing can be connected to the RESIN input in addition to the power-on RC network.

The READY input to the CPU has certain timing specifications such as "set-up and hold" thus, an external synchronizing flip-flop is required. The Am8224 has this feature built-in. The RDYIN input presents the asynchronous "wait request" to the "D" type flip-flop. By clocking the flip-flop with ϕ_{2D}, a synchronized READY signal at the correct input level, can be connected directly to the CPU.

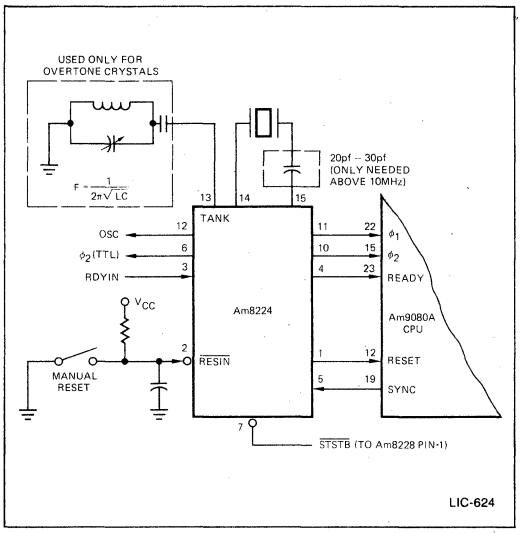


Figure 2. Typical Application with Am8224 and Am9080A.

APPLICATION PRECAUTIONS WHEN USING Am8224 UP TO 36MHz

Usage with Third Harmonic Crystal or Am9080A-4

The use of the Am8224 with a third harmonic crystal requires a minor modification to the external circuitry associated with the Am8224. The changes are as follows:

– Series capacitor in conjunction with the xtal
– Adding a tuned circuit in the "tank" lead
– Tuning of circuit to proper frequency

It is necessary to maintain the crystal activity to a proper level if an xtal controlled circuit is to operate properly. A 20-30pfd capacitor placed in series will help achieve this level in third overtone crystal, while helping to suppress the fundamental mode. The Am8224 has an auxiliary port provided to allow for a tuned circuit. This tuned circuit eliminates the tendency of the circuit to oscillate at the crystal's fundamental. The tank or tuned circuit must have the following properties:

1. It must be parallel resonant at the crystal frequency (third order).
2. The off resonance impedance must be low enough to spoil the AC gain of the Am8224.
3. The circuit must be DC decoupled (or returned to V_{CC}) at a low impedance (substantially below 100Ω).

All frequency determining components must be in close proximity to the Am8224. Insert crystal and tune tank for best waveform at Pin 12 (OSC). If counter is available, adjust for match of crystal marking. The circuit in Figure 3 will accomplish the above result for the 36MHz range.

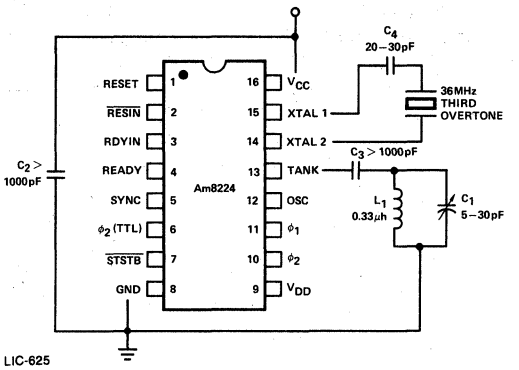


Figure 3.

C_1 = E.F. Johnson
275-0430-005
5-30pF Trimmer or Equiv.

L_1 = J.W. Miller Inductor
9230-08

V_{CC} Ground

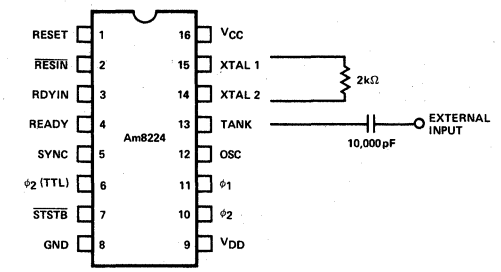
Due to the nature of our device (fast switching, higher voltage) it is necessary to provide a bypass capacitor from V_{CC} to ground in the immediate proximity of the Am8224. This insures proper operation of the device while reducing noise spiking on adjacent circuits.

Resin Bypass

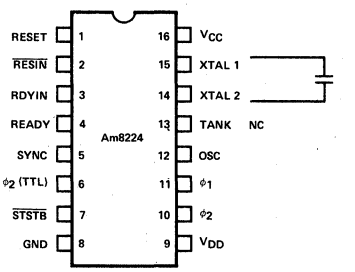
The use of a high impedance capacitor for timing R-C, and/or timing components remotely located from the Am8224 device may cause a disturbance to occur during the linear transition region. The capacitor for this function should be of the ceramic type and a value of 1000pF or greater.

This can be cured by placing a >1000pfd ceramic capacitor from Resin (Pin 2) to Ground (Pin 8) in the immediate proximity of the device. This will allow the timing R-C to be placed at will.

APPLICATIONS

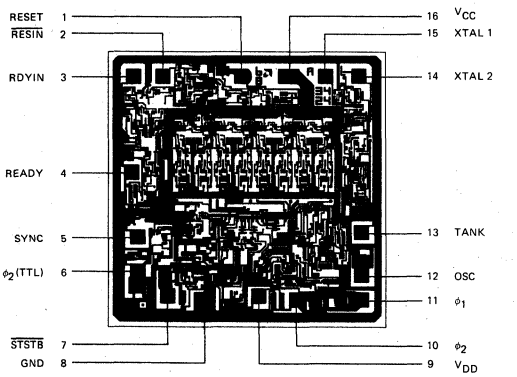


The Am8224 can be driven from an external source of frequency by connecting as shown and driven with approximately 500mV over a wide frequency range.



The Am8224 can oscillate without a xtal by placing a small value capacitor (10→200pF) in place of a crystal.

Metallization and Pad Layout



DIE SIZE 0.085" X 0.084"

Am8228 • Am8238

System Controller and Bus Driver for 8080A Compatible Microprocessors

Distinctive Characteristics

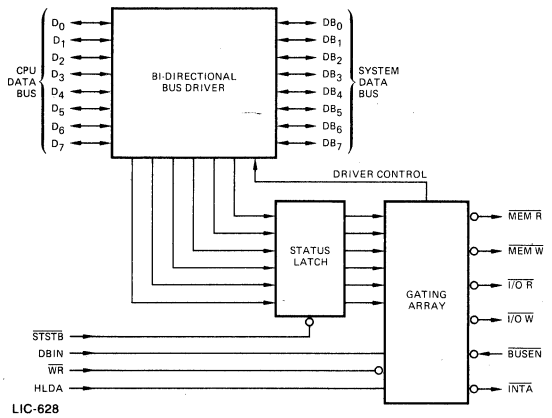
- Multi-byte instruction interrupt acknowledge
- Selectable single level vectored interrupt (RST-7)
- 28-pin molded or hermetic DIP package
- Single chip system controller and data bus driver for Am9080/8080A systems
- Am8238-4 high speed version available for use with 1μsec instruction cycle of Am9080A-4
- Bi-directional three-state bus driver for CPU independent operation
- Advanced low-power Schottky processing
- Available in military and commercial temperature range
- Am8238 has extended $\overline{IOW}/\overline{MEMW}$ pulse width

FUNCTIONAL DESCRIPTION

The Am8228 and Am8238 are single chip System Controller Data Bus drivers for the Am9080A Microcomputer System. They generate all control signals required to directly interface Am9080A/8080A compatible system circuits (memory and I/O) to the CPU.

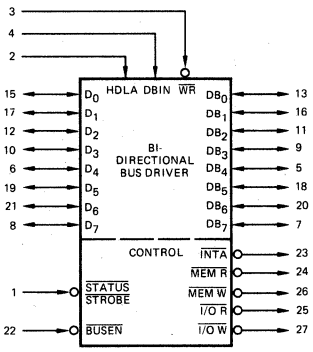
Bi-directional bus drivers with three-state outputs are provided for the system data bus, facilitating CPU independent bus operations such as direct memory access. Interrupt processing is accommodated by means of a single vectored interrupt or by means of the standard 8080A multiple byte interrupt vector operation.

LOGIC DIAGRAM



LIC-628

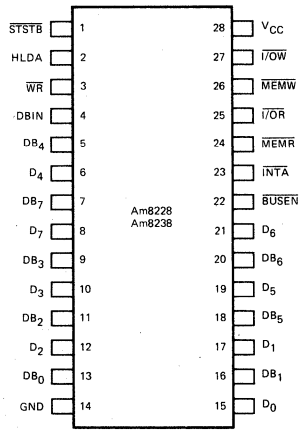
LOGIC SYMBOL



V_{CC} = Pin 28
GND = Pin 14

LIC-629

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LIC-630

ORDERING INFORMATION

Package Type	Temperature Range	Am8228 Order Number	Am8238 Order Number
Molded DIP	0°C to +70°C	AM8228PC	AM8238PC
Hermetic DIP	0°C to +70°C	D8228	D8238
Hermetic DIP	−55°C to +125°C	AM8228DM	AM8238DM
Dice	0°C to +70°C	AM8228XC	AM8238XC
Hermetic DIP	0°C to +70°C		AM8238-4DC*
Molded DIP	0°C to +70°C		AM8238-4PC*

*For use with Am9080A-4 with minimum clock period of 250ns.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Volatge to Ground Potential (Pin 28 to Pin 14) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−1.5V to +7.0V
DC Output Current, Into Outputs	50mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS The Following Conditions Apply Unless Otherwise Noted:

Am8228XM, Am8238XM T_A = −55°C to +125°C V_{CC}MIN. = 4.50V V_{CC}MAX. = 5.50V
Am8228XC, Am8238XC, Am8238-4XC T_A = 0°C to +70°C V_{CC}MIN. = 4.75V V_{CC}MAX. = 5.25V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 2)				Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN.	I_{OH} = −10μA	D_0–D_7	MIL	3.35	3.8		Volts
					COM'L	3.6	3.8		
			I_{OH} = −1.0mA	All other outputs		2.4			
V_{OL}	Output Low Voltage	V_{CC} = MIN.	I_{OL} = 2.0mA	D_0–D_7				0.45	Volts
			I_{OL} = 10mA	All other outputs				0.45	
V_C	Input Clamp Voltage (All Inputs)	V_{CC} = MIN., I_C = −5.0mA					−0.75	−1.0	Volts
V_{TH}	Input Threshold Voltage (All Inputs)	V_{CC} = 5.0V				0.8		2.0	Volts
I_F	Input Load Current	V_{CC} = MAX., V_F = 0.45V		$\overline{STSTB}$				−500	μA
				D_2 and D_6				−750	
				All other inputs				−250	
I_R	Input Leakage Current	V_{CC} = MAX., V_R = 5.25V		DB_0–DB_7				20	μA
				All other inputs				100	
I_{INT}	INTA Current	See INTA test circuit						5.0	mA
$I_{O(OFF)}$	Offstate Output Current (All Control Outputs)	V_{CC} = MAX., V_O = 5.25V						100	μA
		V_O = 0.45V						−100	
I_{OS}	Short Circuit Current (All Outputs)	V_{CC} = 5.0V				−15		−90	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.					140	190	mA

AC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

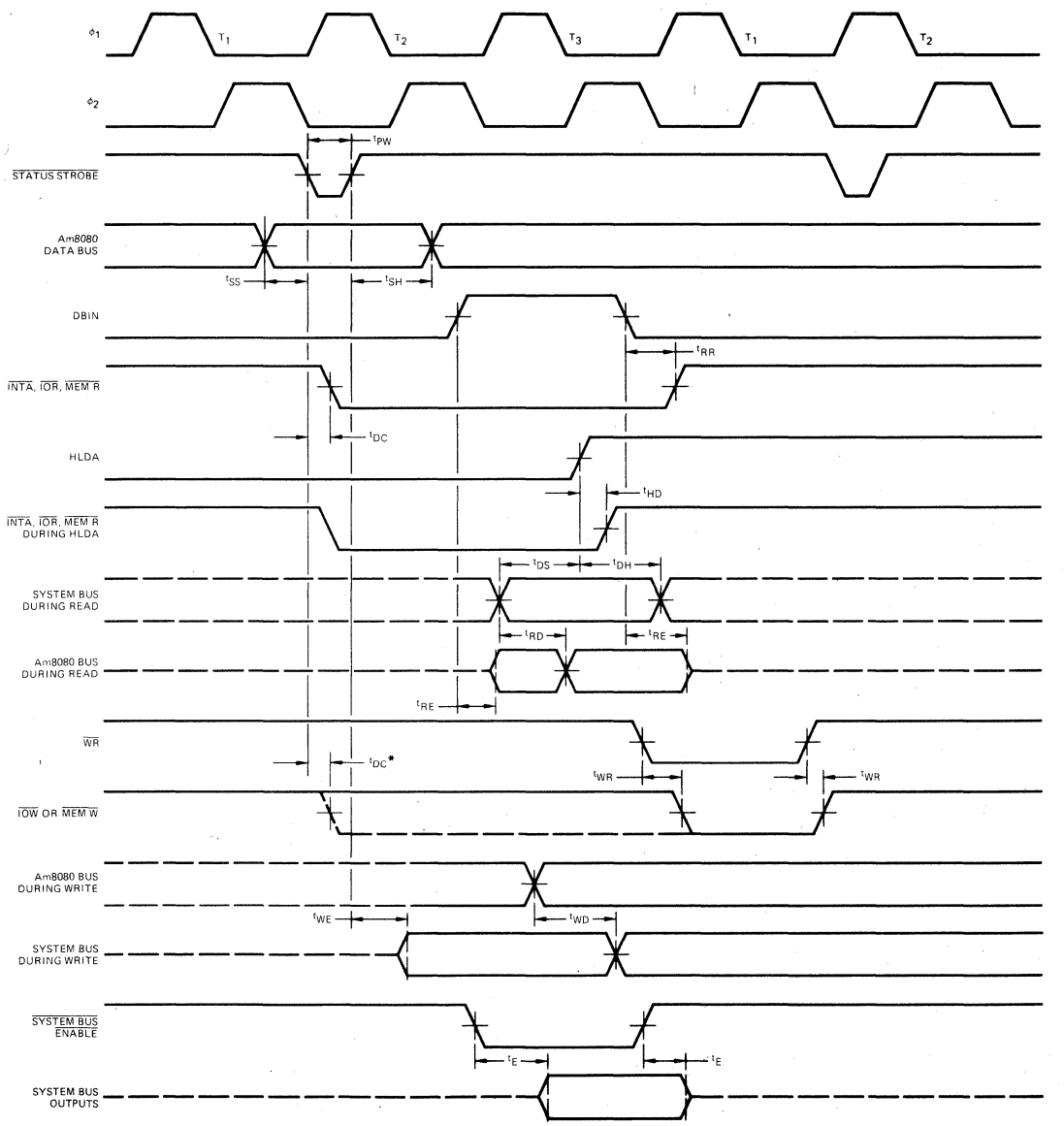
Parameters	Description	Test Conditions	Am8228XM/ Am8238XM Min.	Typ. (Note 1)	Max.	Am8228XC/ Am8238XC Min.	Typ. (Note 1)	Max.	Am8238-4XC Min.	Typ. (Note 1)	Max.	Units
t_{PW}	Width of Status Strobe		22			22			22			ns
t_{SS}	Set-up Time, Status Inputs D_0-D_7		12			8.0			8.0			ns
t_{SH}	Hold Time, Status Inputs D_0-D_7		5.0			5.0			5.0			ns
t_{DC}	Delay from $\overline{STSTB}$ to $\overline{MEMR}$	CL = 100pF	20	30	60	20	30	60	20	30	40	ns
	Delay from $\overline{STSTB}$ to $\overline{INTA}$, $\overline{IOR}$		20	30	60	20	30	60	20	30	45	
	Delay from $\overline{STSTB}$ to all other Control Signals		20	30	60	20	30	60	20	30	60	
t_{RR}	Delay from DBIN to Control Outputs			15	35		15	30		15	30	ns
t_{RE}	Delay from DBIN to 8080A Bus — Enable	C_L = 25pF		25	45		25	45		12	20	ns
	Delay from DBIN to 8080A Bus — Disable			25	45		25	45		25	35	
t_{RD}	Delay from System Bus to 8080A Bus During Read			15	30		15	30		15	20	ns
t_{WR}	Delay from $\overline{WR}$ to Control Outputs	C_L = 100pF	5.0	20	45	5.0	20	45	5.0	20	45	ns
t_{WE}	Delay to Enable System Bus DB_0-DB_7 After $\overline{STSTB}$			25	36		25	30		25	30	ns
t_{WD}	Delay from 8080A Bus D_0-D_7 to System Bus DB_0-DB_7 During Write		5.0	20	40	5.0	20	40	5.0	20	40	ns
t_E	Delay from $\overline{\text{System Bus Enable}}$ to System Bus DB_0-DB_7			25	35		25	30		20	30	ns
t_{HD}	HLDA to Read Status Outputs			15	28		15	25		15	25	ns
t_{DS}	Set-up Time, System Bus Inputs to HLDA		10			10			10			ns
t_{DH}	Hold Time, System Bus Inputs to HLDA		20			20			20			ns

Notes: 1. Typical values are for T_A = 25°C and nominal supply voltages.
2. For conditions shown as MIN. or MAX., use the appropriate value specified under electrical characteristics for the applicable device type.

CAPACITANCE (This parameter is periodically sampled and not 100% tested.)

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
C_{IN}	Input Capacitance	V_{BIAS} = 2.5V, V_{CC} = 5.0V T_A = 25°C, f = 1.0MHz		8.0	12	pF
C_{OUT}	Output Capacitance Control Signals			7.0	15	pF
I/O	I/O Capacitance (D or DB)			8.0	15	pF

SWITCHING WAVEFORMS



Voltage measurements points: $D_0 - D_7$ (when outputs) Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

*Extended $\overline{IOW}/\overline{MEMW}$ for Am8238 only.

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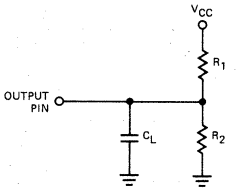
TEST CIRCUITS



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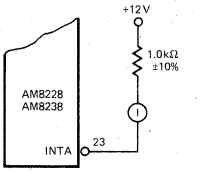
Note 1. For D_0-D_7: $R_1 = 4.0k\Omega$, $R_2 = \infty\Omega$, $C_L = 25pF$.
For all other outputs: $R_1 = 500\Omega$, $R_2 = 1.0k\Omega$, $C_L = 100pF$.



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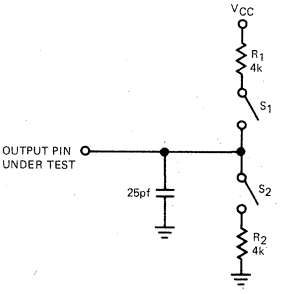
INTA (for RST 7)



LIC-634

Test Circuit for DBIN to 8080A BUS

t_{RE}	S_1	S_2
Enable 8080 bus, HIGH-Z to logic "0"	Closed	Open
Enable 8080 bus, HIGH-Z to logic "1"	Open	Closed
Disable 8080 bus, logic "0" to HIGH-Z	Closed	Open
Disable 8080 bus, logic "1" to HIGH-Z	Open	Closed

FUNCTIONAL DESCRIPTION

Bi-Directional Bus Driver: An eight-bit, bi-directional bus driver is provided to buffer the Am9080A/8080A data bus from Memory and I/O devices. The Am9080A data bus has an input requirement of *3.0 volts (min) and can drive (sink) a current of at least 3.2mA. The Am8228 • Am8238 data bus driver matches these input requirements and provides enhanced noise immunity. The output drive is set for 10mA typical for Memory and I/O devices.

The Bi-Directional Bus Drive is controlled by signals from the Gating Array for proper bus flow and the outputs can be forced to high impedance state (three-state) for DMA activities.

Status Latch: The Am8228 • Am8238 stores the status information in the Status Latch when the $\overline{STSTB}$ input goes "LOW". The output of the Status Latch is connected to the Gating Array and is part of the Control Signal generation.

Gating Array: The Gating Array generates control signals ($\overline{MEM\ R}$, $\overline{MEM\ W}$, $\overline{I/O\ R}$, $\overline{I/O\ W}$ and $\overline{INTA}$) by gating the outputs of the Status Latch Am9080A signals; i.e., DBIN, WE, and HLDA.

*The 8080A has an input requirement of 3.3V and can drive a maximum current of 1.9mA.

The "read" control signals (MEM R, I/O R and INTA) are derived by combinational logic from Status Bit and the DBIN input.

The "write" control signals (MEM W, I/O W) are similarly derived from the Status Bits and the WR input.

All Control Signals are "active LOW" and directly interface RAM, ROM and I/O components.

The $\overline{INTA}$ control signal is normally used to gate the "interrupt instruction port" onto the bus. It also provides a special feature in the Am8228 • Am8238. If only one basic vector is needed in the interrupt structure, the Am8228 • Am8238 can automatically insert a RST 7 instruction onto the bus. To use this option, connect the INTA output of the Am8228 • Am8238 (pin 23) to the +12 volt supply through a series resistor (1k ohms). The voltage is sensed internally by the Am8228 • Am8238 and logic is "set-up" so that when the DBIN input is active, a RST 7 instruction is gated on to the bus when an interrupt is acknowledged.

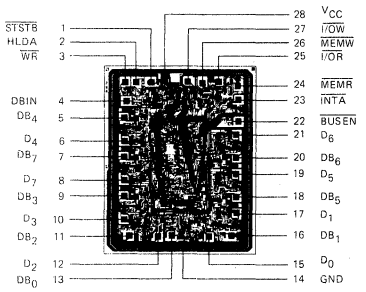
When using a multiple byte instruction as an Interrupt Instruction, the Am8228 • Am8238 will generate an INTA pulse for each of the instruction bytes.

The BUSEN (Bus Enable) input of the Gating Array is an asynchronous input that forces the data bus output buffers and control signal buffers into their high-impedance state if it is a "HIGH". If BUSEN is a "LOW", normal operation of the data buffer and control signals take place. This facilitates CPU independent bus operations such as direct memory access.

DEFINITION OF FUNCTIONAL TERMS

D_7-D_0	Data bus to-from Am9080A/8080A
DB_7-DB_0	Data bus to-from user system
$\overline{I/OR}$	Input/output read strobe output active LOW
$\overline{I/OW}$	Input/output write strobe output active LOW
$\overline{MEM\ R}$	Memory read strobe, output, active LOW
$\overline{MEM\ W}$	Memory write strobe, output, active LOW
DBIN	Data bus input strobe, input active HIGH
$\overline{INTA}$	Interrupt acknowledge strobe, input, active LOW
HLDA	Hold input from Am9080A/8080A active HIGH
$\overline{WR}$	Write input strobe, active HIGH
$\overline{BUSEN}$	BUS ENABLE INPUT, input, 3-state output control, active LOW for 3-state out
$\overline{STSTB}$	Status Strobe, input, strobes status on data bus into status latch, active LOW

Metallization and Pad Layout



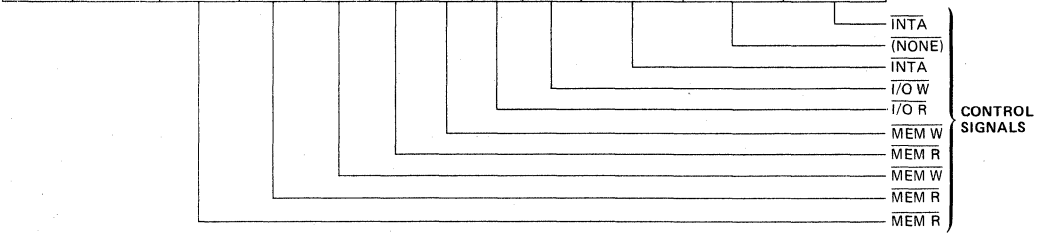
DIE SIZE 0.110" X 0.136"

LOADING RULES

Signal	Pin No.	Input Load	Output Sink	Output Source
D_0	15	250μA	2mA	−10μA
D_1	17	250μA	2mA	−10μA
D_2	12	750μA	2mA	−10μA
D_3	10	250μA	2mA	−10μA
D_4	6	250μA	2mA	−10μA
D_5	19	250μA	2mA	−10μA
D_6	21	750μA	2mA	−10μA
D_7	8	250μA	2mA	−10μA
DB_0	13	250μA	10mA	−1mA
DB_1	16	250μA	10mA	−1mA
DB_2	11	250μA	10mA	−1mA
DB_3	9	250μA	10mA	−1mA
DB_4	5	250μA	10mA	−1mA
DB_5	18	250μA	10mA	−1mA
DB_6	20	250μA	10mA	−1mA
DB_7	7	250μA	10mA	−1mA
$\overline{STSTB}$	1	500μA	–	–
DBIN	4	250μA	–	–
$\overline{WR}$	3	250μA	–	–
HLDA	2	250μA	–	–
$\overline{MEM\ R}$	24	–	10mA	−1mA
$\overline{MEM\ W}$	26	–	10mA	−1mA
$\overline{I/OR}$	25	–	10mA	−1mA
$\overline{IOW}$	27	–	10mA	−1mA
$\overline{BUSEN}$	22	250μA	–	–
$\overline{INTA}$	23	–	10mA	−1mA
GND	14			
V_{CC}	28			

STATUS WORD CHART

		TYPE OF MACHINE CYCLE										
Data Bus Bit	Status Information	Instruction Fetch	Memory Read	Memory Write	Stack Read	Stack Write	Input Read	Output Write	Interrupt Acknowledge	Halt Acknowledge	Interrupt Acknowledge While Halt	
		①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	Ⓝ STATUS WORD
D_0	INTA	0	0	0	0	0	0	0	1	0	1	
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1	
D_2	STACK	0	0	0	1	1	0	0	0	0	0	
D_3	HLTA	0	0	0	0	0	0	0	0	1	1	
D_4	OUT	0	0	0	0	0	0	1	0	0	0	
D_5	M_1	1	0	0	0	0	0	0	1	0	1	
D_6	INP	0	0	0	0	0	1	0	0	0	0	
D_7	MEM R	1	1	0	1	0	0	0	0	1	0	



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8284A

Clock Generator and Driver for 8086, 8088 Processors

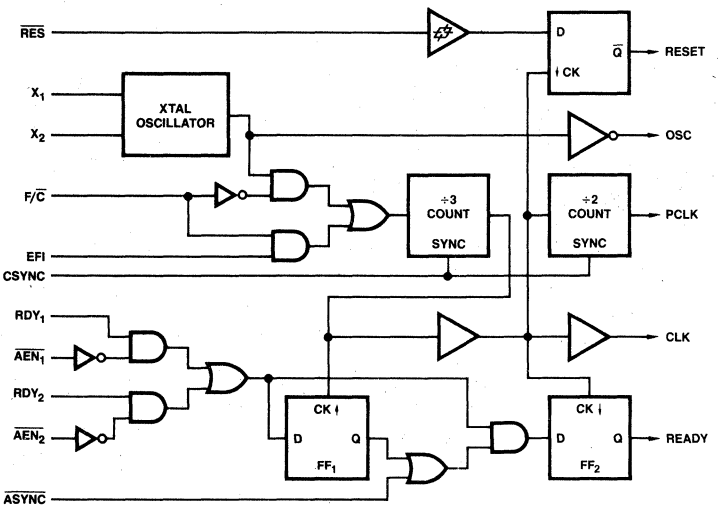
DISTINCTIVE CHARACTERISTICS

- Generates the System Clock for the 8086, 8088 Processors: 5MHz, 8MHz with 8284A
- Uses a crystal or a TTL signal for frequency source
- Provides local READY and Multibus* READY synchronization
- Generates system reset output from Schmitt trigger input
- Capable of clock synchronization with other 8284As

GENERAL DESCRIPTION

The 8284A is a single chip clock generator/driver for the 8086, 8088 processors. The chip contains a crystal-controlled oscillator, a divide-by-three counter, complete MULTIBUS* "Ready" synchronization and reset logic.

LOGIC DIAGRAM



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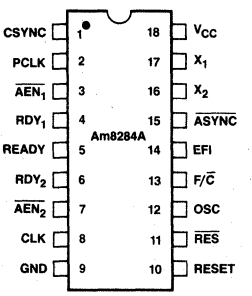
CONNECTION DIAGRAM
Top View



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Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

8284 Order Number	Package Type	Temperature Range
D8284	Hermetic DIP	0 to +70°C
8284XC	Dice	0 to +70°C
MD8284	Hermetic DIP	−55 to +125°C
8284XM	Dice	−55 to +125°C

TABLE OF CONTENTS

*Multibus is a registered trademark of Intel Corp.

DEFINITION OF FUNCTIONAL TERMS

$\overline{AEN_1}$, $\overline{AEN_2}$ **ADDRESS ENABLE (Input)**
The $\overline{AEN}$ signal is used to qualify the Bus Ready signal (RDY_1 or RDY_2). $\overline{AEN_1}$ validates RDY_1 while $\overline{AEN_2}$ validates RDY_2. It is possible for the processor to access two Multi-Master System Busses if you use both signals. Both signals are tied LOW in non Multi-Master Systems.

RDY_1, RDY_2 **BUS READY (Input)**
These signals are indications from a device located on the system bus that it is available or data has been received. RDY_1 and RDY_2 are qualified by $\overline{AEN_1}$ and $\overline{AEN_2}$ respectively.

ASYNC **READY SYNCHRONOUS SELECT (Input)**
The ASYNC signal defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is open (internal pull-up resistor is provided) or pulled HIGH there is one stage of READY Synchronization. When $\overline{ASYNC}$ is LOW there are two stages of READY Synchronization.

READY **READY (Input)**
READY is the synchronized RDY signal input. After the guaranteed hold time to the processor has been met, the READY signal is cleared.

X_1, X_2 **CRYSTAL IN (Inputs)**
These are the input pins for the attached crystal. The crystal frequency is 3 times the desired process clock frequency.

F/$\overline{C}$ **FREQUENCY/$\overline{CRYSTAL\ SELECT}$ (Input)**
When F/$\overline{C}$ is strapped HIGH, CLK is generated from the EFI input. When strapped LOW, the F/$\overline{C}$ allows the processor clock to be generated by the crystal.

EFI **EXTERNAL FREQUENCY (Input)**
Used in conjunction with a HIGH signal on F/$\overline{C}$, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output.

CLK **PROCESSOR CLOCK (Output)**
CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus (including bipolar support chips and other MOS devices). An output HIGH of 4.5V (V_{CC} = 5V) is provided on this pin to drive MOS devices. The output frequency of CLK is 1/3 of the crystal on EFI input frequency and a 1/3 duty cycle.

PCLK **PERIPHERAL CLOCK (Output)**
This signal is a TTL level peripheral clock signal whose output frequency is 1/2 that of CLK and has a 50% duty cycle.

OSC **OSCILLATOR OUTPUT (Output)**
This signal is the TTL level output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.

$\overline{RES}$ **$\overline{RESET}$ IN (Input)**
This signal is used to generate a RESET. The 8284A provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.

RESET **RESET (Output)**
This signal is used to reset the 8086 family processors.

CSYNC **CLOCK SYNCHRONIZATION (Input)**
This signal is designed to allow multiple 8284As to be synchronized to provide clocks that are in phase. CSYNC HIGH will reset the internal counters, when CSYNC goes LOW the counters will resume counting. CSYNC needs to be externally synchronized to EFI. When used with the internal oscillator, CSYNC should be hard wired to ground.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The oscillator circuit of the 8284A is designed primarily for use with a fundamental mode, series resonant crystal from which the operating frequency is derived.

The crystal frequency should be selected at three times the required CPU clock. X_1 and X_2 are the two crystal input crystal connections. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.

Two 510Ω series resistors are optional for systems which have a V_{CC} ramp time greater than (or equal to) 1V/ms and/or inherent board capacitance between X_1 or X_2 exceeding 10pF. This capacitance value should not include the 8284A's pin capacitance. By limiting the stray capacitance to less than 10pF on X_1 or X_2 the deviation from the desired fundamental frequency is minimized.

CLOCK GENERATOR

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input (CSYNC) allows the output clock to be synchronized with an external event (such as another 8284A clock). It is necessary to synchronize the CSYNC input to the EFI clock external to the 8284A (see Figure 1). This is accomplished with two Schottky flip-flops. The counter output is a 33% duty cycle clock at one-third the input frequency.

The F/$\overline{C}$ input is a strapping pin that selects either the EFI input or the crystal oscillator as the clock for the ÷ 3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source. Output is taken from OSC.

CLOCK OUTPUTS

The CLK output is a 33% duty cycle MOS clock driver designed to drive the 8086 or 8088 processors directly. PCLK is a TTL level peripheral clock signal whose output frequency is 1/2 that of CLK. PCLK has a 50% duty cycle.

RESET LOGIC

Reset logic for the 8284A is provided by a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate the reset timing. The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the 8284A.

READY SYNCHRONIZATION

Two READY inputs (RDY_1, RDY_2) are provided to accommodate two Multi-Master system busses. Each input has a qualifier ($\overline{AEN}_1$ and $\overline{AEN}_2$, respectively). The $\overline{AEN}$ signals validate their respective RDY signals. If a Multi-Master system is not being used the $\overline{AEN}$ pin should be tied LOW.

To assure RDY setup and hold times are met, synchronization is required for all asynchronous active going edges of either RDY input. Inactive-going edges of RDY in normally ready systems do not require synchronization but must satisfy RDY setup and hold as a matter of proper system design.

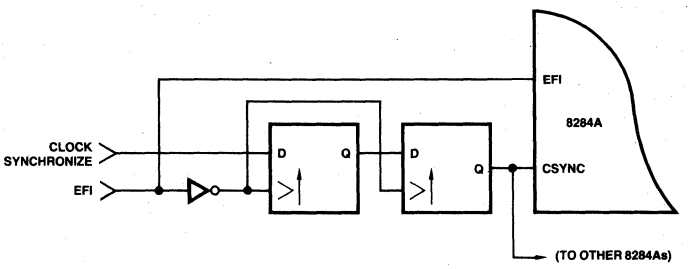
The two modes of READY synchronization operation are defined by the $\overline{ASYNC}$ input.

When $\overline{ASYNC}$ is LOW, two stages of synchronization are provided for active READY input signals. Positive-going asynchronous READY inputs will first be synchronized to flip-flop one at the rising edge of CLK and then synchronized to flip-flop two at the next falling edge of CLK, after which time the READY output will go active (HIGH). Negative-going asynchronous READY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which time the READY output will go inactive. This mode of operation is intended for use by asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing t_{R1VCL}, on each bus cycle.

When $\overline{ASYNC}$ is high or left open, the first READY flip-flop is bypassed in the READY synchronization logic. READY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time.

$\overline{ASYNC}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.

Figure 1. CSYNC Synchronization



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MAXIMUM RATINGS (Above which the useful life may be impaired)

Temperature Under Bias	0 to 70°C
Storage Temperature	−65 to +150°C
All Output and Supply Voltages	−0.5 to +7V
All Input Voltages	−1.0 to +5.5V
Power Dissipation	1W

DC CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Parameters	Description	Test Conditions	Min	Max	Units
I_F	Forward Input Current ($\overline{ASYNC}$)	V_F = 0.45V		−1.3	mA
	Other Inputs	V_F = 0.45V		−0.5	
I_R	Reverse Input Current ($\overline{ASYNC}$)	$V_R = V_{CC}$		50	μA
	Other Inputs	V_R = 5.25V		50	
V_C	Input Forward Clamp Voltage	I_C = −5mA		−1.0	V
I_{CC}	Power Supply Current			162	mA
V_{IL}	Input LOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		V
V_{IHR}	Reset Input HIGH Voltage		2.6		V
V_{OL}	Output LOW Voltage	5mA		0.45	V
V_{OH}	Output HIGH Voltage CLK	−1mA	4	2.5	V
	Other Outputs	−1mA	2.4		
$V_{IHR}-V_{ILR}$	$\overline{RES}$ Input Hysteresis		0.25		V

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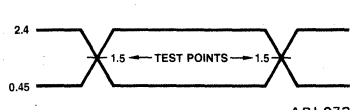
SWITCHING CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = 5V ± 10%)

Parameter	Description	Test Conditions	Min	Max	Units
TIMING REQUIREMENTS					
t_{EHEL}	External Frequency HIGH Time	90% – 90% V_{IN}	13		ns
t_{ELEH}	External Frequency LOW Time	10% – 10% V_{IN}	13		ns
t_{ELEL}	EFI Period	(Note 1)	33		ns
	XTAL Frequency		12	25	MHz
t_{R1VCL}	RDY_1, RDY_2 Active Setup to CLK	ASYNC = HIGH	35		ns
t_{R1VCH}	RDY_1, RDY_2 Active Setup to CLK	ASYNC = LOW	35		ns
t_{R1VCL}	RDY_1, RDY_2 Inactive Setup to CLK		35		ns
t_{CLR1X}	RDY_1, RDY_2 Hold to CLK		0		ns
t_{AYVCL}	$\overline{ASYNC}$ Setup to CLK		50		ns
t_{CLAYX}	$\overline{ASYNC}$ Hold to CLK		0		ns
t_{A1VR1V}	$\overline{AEN_1}$, $\overline{AEN_2}$ Setup to RDY_1, RDY_2		15		ns
t_{CLA1X}	$\overline{AEN_1}$, $\overline{AEN_2}$ Hold to CLK		0		ns
t_{YHEH}	CSYNC Setup to EFI		20		ns
t_{EHYL}	CSYNC Hold to EFI		10		ns
t_{YHYL}	CSYNC Width		$2 \cdot t_{ELEL}$		ns
t_{I1HCL}	$\overline{RES}$ Setup to CLK	(Note 1)	65		ns
t_{CLI1H}	$\overline{RES}$ Hold to CLK	(Note 1)	20		ns
t_{ILIH}	Input Rise Time	From 0.8 to 2.0V		20	ns
t_{ILIL}	Input Fall Time	From 2.0 to 0.8V		12	ns
TIMING RESPONSES					
t_{CLCL}	CLK Cycle Period		125		ns
t_{CHCL}	CLK HIGH Time		$(1/3\ t_{CLCL}) + 2$		ns
t_{CLCH}	CLK LOW Time		$(2/3\ t_{CLCL}) - 15$		ns
t_{CH1CH2}	CLK Rise or Fall Time	1.0V to 3.5V		10	ns
t_{CL2CL1}					
t_{PHPL}	PCLK HIGH Time		$t_{CLCL} - 20$		ns
t_{PLPH}	PCLK LOW Time		$t_{CLCL} - 20$		ns
t_{RYLCL}	Ready Inactive to CLK (See Note 3)		−8		ns
t_{RYHCH}	Ready Active to CLK (See Note 2)		$(2/3\ t_{CLCL}) - 15$		ns
t_{CLIL}	CLK to Reset Delay			40	ns
t_{CLPH}	CLK to PCLK HIGH Delay			22	ns
t_{CLPL}	CLK to PCLK LOW Delay			22	ns
t_{OLCH}	OSC to CLK HIGH Delay		−5	22	ns
t_{OLCL}	OSC to CLK LOW Delay		2	35	ns
t_{OLOH}	Output Rise Time (except CLK)	From 0.8 to 2.0V		20	ns
t_{OHOL}	Output Fall Time (except CLK)	From 2.0 to 0.8V		12	ns

Notes: 1. Setup and hold necessary only to guarantee recognition at next clock.
2. Applies only to T_3 and T_W states.
3. Applies only to T_2 states.

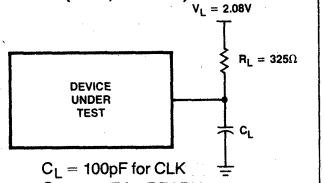
AC TESTING INPUT, OUTPUT WAVEFORM



ABI-073

AC testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". Timing measurements are made at 1.5V for both a logic "1" and "0".

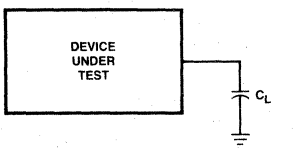
AC TESTING LOAD CIRCUIT (CLK, READY)



C_L = 100pF for CLK
C_L = 30pF for READY

ABI-074

AC TESTING LOAD CIRCUIT (PCLK, OSC, RESET)

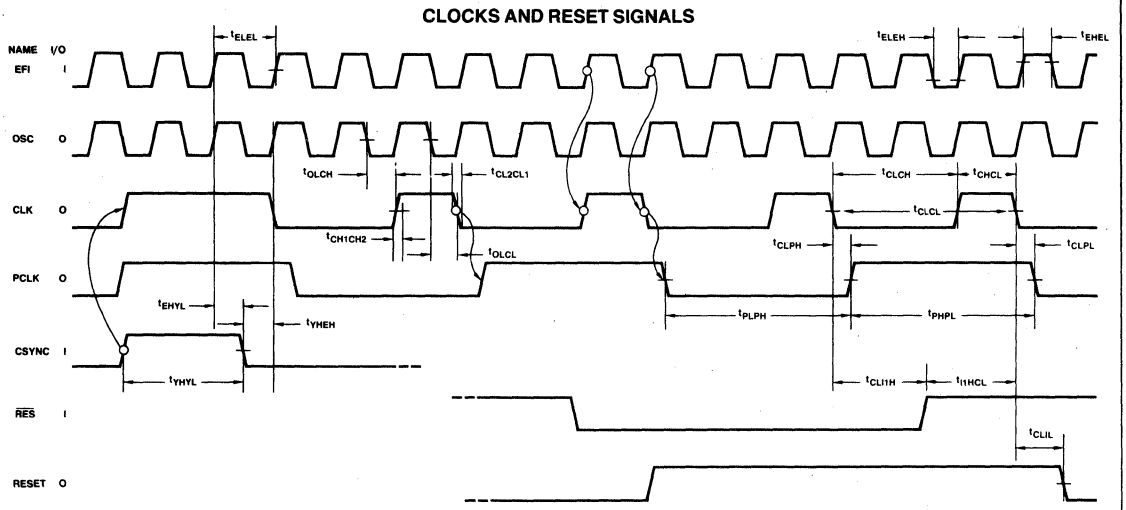


C_L = 100pF

ABI-075

WAVEFORMS

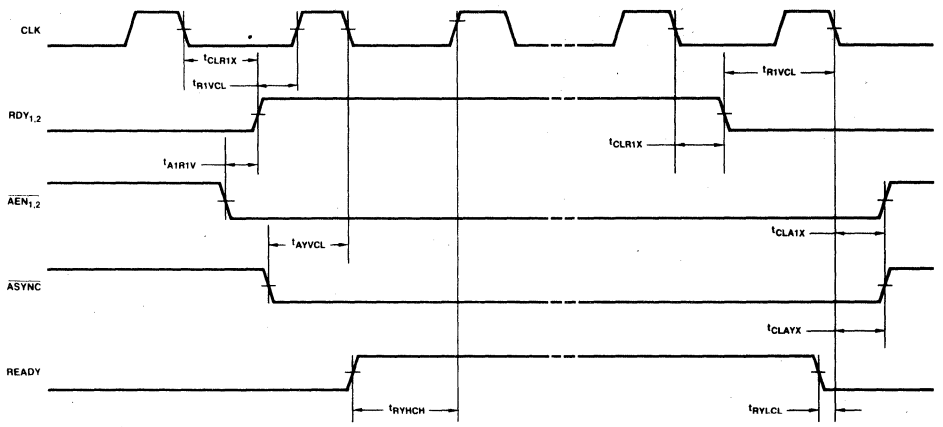
CLOCKS AND RESET SIGNALS



Note: All timing requirements are made at 1.5 volts, unless otherwise noted.

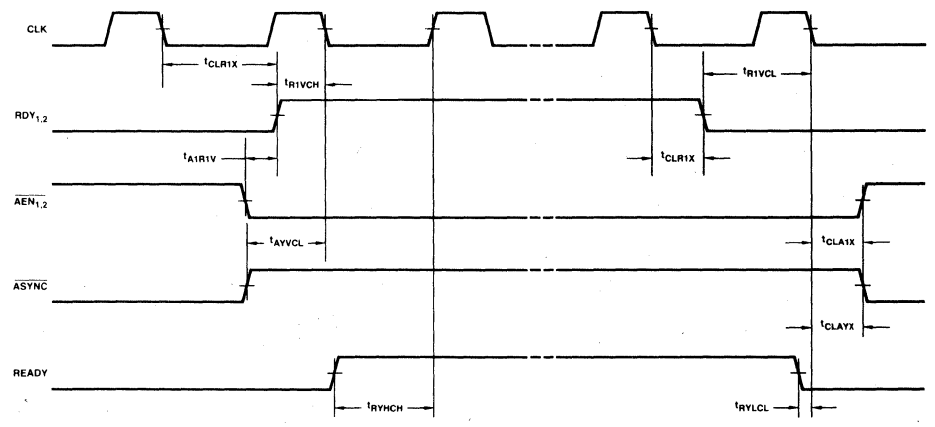
ABI-076

READY SIGNALS (FOR ASYNCHRONOUS DEVICES)



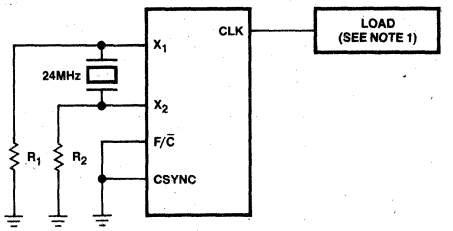
ABI-077

READY SIGNALS (FOR SYNCHRONOUS DEVICES)



ABI-078

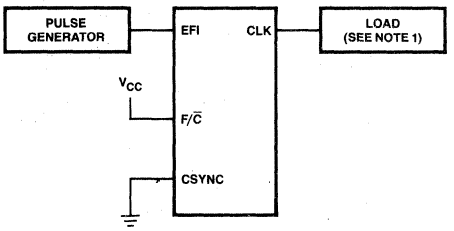
CLOCK HIGH AND LOW TIME (USING X_1, X_2)



$R_1 = R_2 = 510\Omega$.

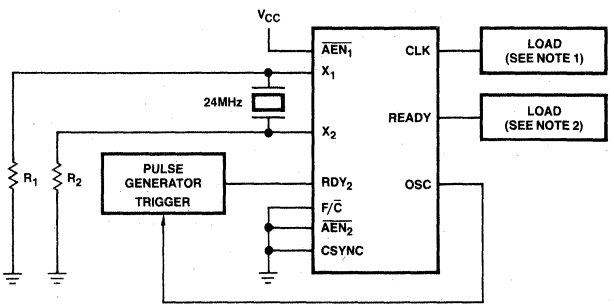
ABI-079

CLOCK HIGH AND LOW TIME (USING EFI)



ABI-080

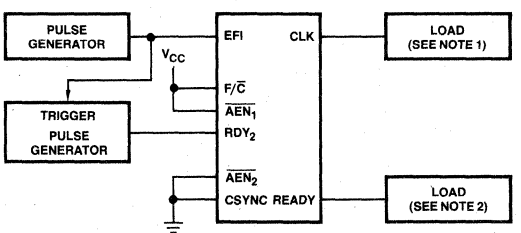
READY TO CLOCK (USING X_1, X_2)



$R_1 = R_2 = 510\Omega$.

ABI-081

READY TO CLOCK (USING EFI)



Notes: 1. $C_L = 100pF$
2. $C_L = 30pF$

ABI-082

8288
Bus Controller

DISTINCTIVE CHARACTERISTICS

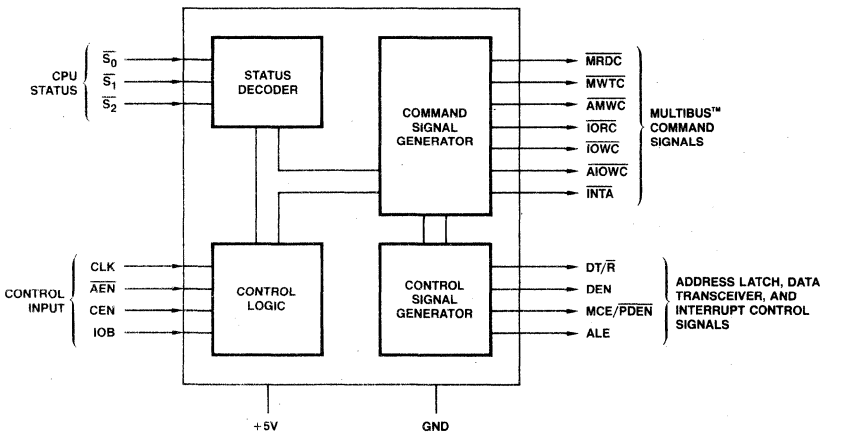
- Bipolar drive capability
- 3-state output drivers
- Multi-master or I/O bus interface
- Flexible system configurations

GENERAL DESCRIPTION

The 8288 optimizes 8086 or 8088 operations by providing command and control timing generation when the CPU is in maximum mode. It provides for highly flexible configurations for larger systems. It also adds powerful bipolar drive capability to the system.

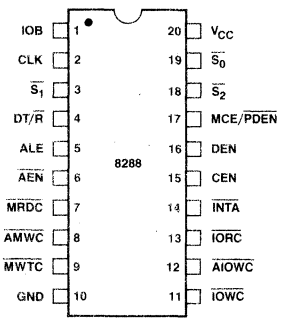
The 8288 is implemented in bipolar technology in a 20-pin DIP.

BLOCK DIAGRAM



ABI-083

CONNECTION DIAGRAM
Top View



ABI-084

Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

8288 Order Number	Package Type	Temperature Range
D8288	Hermetic DIP	0 to +70°C
8288XC	Dice	0 to +70°C

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DEFINITION OF FUNCTIONAL TERMS

$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$ **STATUS (Input)**
These signals are the status input pins from the microprocessor. The 8288 decodes these inputs to generate command and control signals.

CLK **CLOCK (Input)**
Clock signal from the clock generator.

ALE **ADDRESS LATCH ENABLE (Output)**
This signal strobes an address into the address latches. The latching occurs on the falling edge (HIGH to LOW) transition.

DEN **DATA ENABLE (Output)**
This signal enables the data transceivers onto the data bus (local or system).

DT/$\overline{R}$ **DATA TRANSMIT/$\overline{\text{RECEIVE}}$ (Output)**
This signal determines the direction of data flow through the transceivers.

$\overline{AEN}$ **$\overline{\text{ADDRESS ENABLE}}$ (Input)**
This signal enables the 8288 command outputs at least 115ns after it becomes active LOW. When this pin goes inactive, it 3-states the command output drivers.

CEN **COMMAND ENABLE (Input)**
This signal, when LOW, enables all command outputs and the DEN and $\overline{PDEN}$ control outputs are forced to their inactive states.

IOB **INPUT/OUTPUT BUS MODE (Input)**
When strapped HIGH the 8288 functions in the I/O Bus mode. When LOW the 8288 functions in the System Bus mode.

$\overline{AIOWC}$ **$\overline{\text{ADVANCED}}$ I/O $\overline{\text{WRITE COMMAND}}$ (Output)**
The $\overline{AIOWC}$ gives I/O devices early indication of a write instruction by issuing an I/O Write Command earlier in the machine cycle.

$\overline{IOWC}$ **$\overline{\text{I/O WRITE}}$ (Output)**
This signal tells an I/O device to read the data on the data bus.

$\overline{IORC}$ **$\overline{\text{I/O READ}}$ (Output)**
This signal tells an I/O device to drive its data onto the data bus.

$\overline{AMWC}$ **$\overline{\text{ADVANCED MEMORY WRITE}}$ (Output)**
The $\overline{AMWC}$ gives memory devices an early indication of a write instruction by issuing a memory write command earlier in the machine cycle.

$\overline{MWTC}$ **$\overline{\text{MEMORY WRITE}}$ (Output)**
This signal instructs the memory to record the data present on the data bus.

$\overline{MRDC}$ **$\overline{\text{MEMORY READ}}$ (Output)**
This signal instructs the memory to drive its data onto the data bus.

$\overline{INTA}$ **$\overline{\text{INTERRUPT ACKNOWLEDGE}}$ (Output)**
This signal informs the interrupting device that its interrupt has been acknowledged and to drive vectoring information onto the data bus.

MCE/$\overline{PDEN}$ **MASTER CASCADE ENABLE/ $\overline{\text{PERIPHERAL DATA ENABLE}}$ (Output)**
Dual Function pin:
MCE (IOB LOW): This signal occurs during an interrupt sequence. Its function is to read a Cascade Address from a master Priority Interrupt Controller onto the data bus.
$\overline{PDEN}$ (IOB HIGH): This signal enables the data bus transceiver for the I/O Bus during I/O instructions. It performs the same function for the I/O Bus that DEN performs for the system bus.

FUNCTIONAL DESCRIPTION

COMMAND AND CONTROL LOGIC

The command logic decodes the three CPU status lines ($\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$) to determine what command is to be issued.

This chart shows the meaning of each status "word."

$\overline{S}_2$	$\overline{S}_1$	$\overline{S}_0$	Processor State	8288 Command
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Code Access	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

I/O BUS MODE

The 8288 is put into the I/O Bus mode by strapping the IOB pin HIGH. This mode allows one 8288 Bus Controller to handle two external buses. This allows the CPU to access the I/O Bus with no waiting involved. In the I/O Bus Mode all I/O command lines ($\overline{INTA}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$) are always enabled. When the processor initiates an I/O Command, the 8288 immediately activates the command lines using $\overline{PDEN}$ and DT/$\overline{R}$ to control the I/O bus transceiver. There is no arbitration present in this system, so the I/O command lines should not be used to control the system bus. Normal memory access requires a "Bus Ready" signal ($\overline{AEN}$ LOW) before it will proceed. The IOB mode is recommended if I/O or peripherals dedicated to one processor exist in a multiprocessor based system.

SYSTEM BUS MODE

The 8288 is put into the System Bus mode by strapping the IOB pin LOW. This mode is used when only one bus exists. No command is issued until 115ns after the $\overline{AEN}$ line is activated. Bus arbitration is assumed, and this logic will inform the bus controller via the $\overline{AEN}$ line when the bus is free for use. Both I/O commands and memory wait for bus arbitration.

COMMAND OUTPUTS

To prevent the processor from entering unnecessary wait states, the advanced write commands initiate write procedures early in the machine cycle.

The command outputs are:

- $\overline{MRDC}$ – Memory Read Command
- $\overline{MWTC}$ – Memory Write Command
- $\overline{IORC}$ – I/O Read Command
- $\overline{IOWC}$ – I/O Write Command
- $\overline{AMWC}$ – Advanced Memory Write Command
- $\overline{AIOWC}$ – Advanced I/O Write Command
- $\overline{INTA}$ – Interrupt Acknowledge

$\overline{INTA}$ (Interrupt Acknowledge) acts as an I/O read during an interrupt cycle. Its purpose is to inform an interrupting device that its interrupt is being acknowledged and that it should place vectoring information onto the data bus.

CONTROL OUTPUTS

The Data Enable (DEN), Data Transmit/$\overline{Receive}$ (DT/$\overline{R}$) and Master Cascade Enable/Peripheral Data Enable (MCE/$\overline{PDEN}$) are the control outputs of the 8288. The DEN signal determines when the external bus should be enabled onto the local bus while the DT/$\overline{R}$ determines the direction of the data transfer. These two signals usually go to the chip select and direction pins of a transceiver.

The MCE/$\overline{PDEN}$ function is determined by the IOB selection. When IOB is HIGH the $\overline{PDEN}$ serves as a dedicated data enable signal for the I/O or Peripheral System Bus.

INTERRUPT ACKNOWLEDGE AND MCE

The MCE signal is used during an interrupt acknowledge cycle if the 8288 is in the System Bus mode (IOB Low). An interrupt sequence consists of two interrupt acknowledge cycles occurring back to back. No data or address transfers take place during the first cycle. Logic should be provided to mask off MCE during this cycle. Just before the second cycle begins the MCE signal gates a master Priority Interrupt Controller's (PIC) cascade address onto the processor's local bus where ALE (Address Latch Enable) strobes it into the address latches. On the leading edge of the second interrupt cycle the addressed slave PIC gates an interrupt vector onto the system data bus where it is read by the processor.

The MCE signal is not used if the system only contains one PIC. If this is the case the second Interrupt Acknowledge signal gates the interrupt vector onto the processor bus.

ADDRESS LATCH ENABLE AND HALT

Address Latch Enable (ALE) occurs during each machine cycle and serves to strobe the current address into the address latches. ALE also serves to strobe the status ($\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$) into a latch for halt state decoding.

COMMAND ENABLE

The Command Enable (CEN) input acts as a command qualifier for the 8288. If the CEN pin is HIGH the 8288 functions normally. If the CEN pin is pulled LOW, all command lines are held in their inactive state (not 3-state). This feature can be used to implement memory partitioning and to eliminate address conflicts between system bus devices and resident bus devices.

MAXIMUM RATINGS*

Temperature Under Bias	0 to 70°C
Storage Temperature	−65 to +150°C
All Output and Supply Voltages	−0.5 to +7.0V
All Input Voltages	−1.0 to +5.5V
Power Dissipation	1.5W

*Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0 to 70°C)

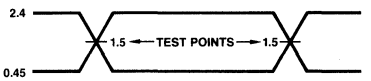
Parameter	Description	Test Conditions	Min	Max	Units
V_C	Input Clamp Voltage	I_C = −5mA		−1	V
I_{CC}	Power Supply Current			230	mA
I_F	Forward Input Current	V_F = 0.45V		−0.7	mA
I_R	Reverse Input Current	V_R = V_{CC}		50	μA
V_{OL}	Output Low Voltage Command Outputs	I_{OL} = 32mA		0.5	V
	Control Outputs	I_{OL} = 16mA		0.5	V
V_{OH}	Output High Voltage Command Outputs	I_{OH} = −5mA	2.4		V
	Control Outputs	I_{OH} = −1mA	2.4		V
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
I_{OFF}	Three-State Leakage	V_{OFF} = 0.4 to 5.25V		100	μA

AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0 to 70°C)

Parameters	Description	Test Conditions	Min	Max	Units
TIMING REQUIREMENTS					
TCLCL	CLK Cycle Period		100		ns
TCLCH	CLK Low Time		50		ns
TCHCL	CLK High Time		30		ns
TSVCH	Status Active Setup Time		35		ns
TCHSV	Status Active Hold Time		10		ns
TSHCL	Status Inactive Setup Time		35		ns
TCLSH	Status Inactive Hold Time		10		ns
TILIH	Input Rise Time	From 0.8V to 2.0V		20	ns
TIHIL	Input Fall Time	From 2.0V to 0.8V		12	ns
TIMING RESPONSES					
TCVNV	Control Active Delay		5.0	45	ns
TCVNX	Control Inactive Delay		10	45	ns
TCLLH, TCLMCH	ALE MCE Active Delay (from CLK)			20	ns
TSVLH, TSVMCH	ALE MCE Active Delay (from Status)			20	ns
TCHLL	ALE Inactive Delay	$\overline{MRDC}$	4.0	15	ns
TCLML	Command Active Delay	$\overline{IORC}$	10	35	ns
TCLMH	Command Inactive Delay	$\overline{MWTC}$	10	35	ns
TCHDTL	Direction Control Active Delay	$\overline{IOWC}$ (I_{OL} = 32mA, I_{OH} = −5mA, C_L = 300pF)		50	ns
TCHDTH	Direction Control Inactive Delay	$\overline{INTA}$		30	ns
TAELCH	Command Enable Time	$\overline{AMWC}$		40	ns
TAELCV	Enable Delay Time	$\overline{AIOWC}$		40	ns
TAEVNV	AEN to DEN	Other (I_{OL} = 16mA, I_{OH} = −1.0mA, C_L = 80pF.)	115	200	ns
TCEVNV	CEN to DEN, PDEN			20	ns
TCELRH	CEN to Command			25	ns
TOLOH	Output Rise Time	From 0.8V to 2.0V		TCLML	ns
TOHOL	Output Fall Time	From 2.0V to 0.8V		20	ns
				12	ns

AC TESTING INPUT, OUTPUT WAVEFORM

Input/Output

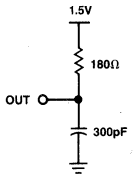


ABI-085

AC Testing: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0." The clock is driven at 4.3V and 0.25V. Timing measurements are made at 1.5V for both a logic "1" and "0."

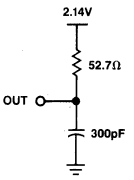
TEST LOAD CIRCUITS

3-State to High



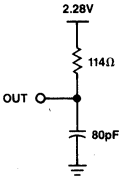
ABI-086

Command Output Test Load



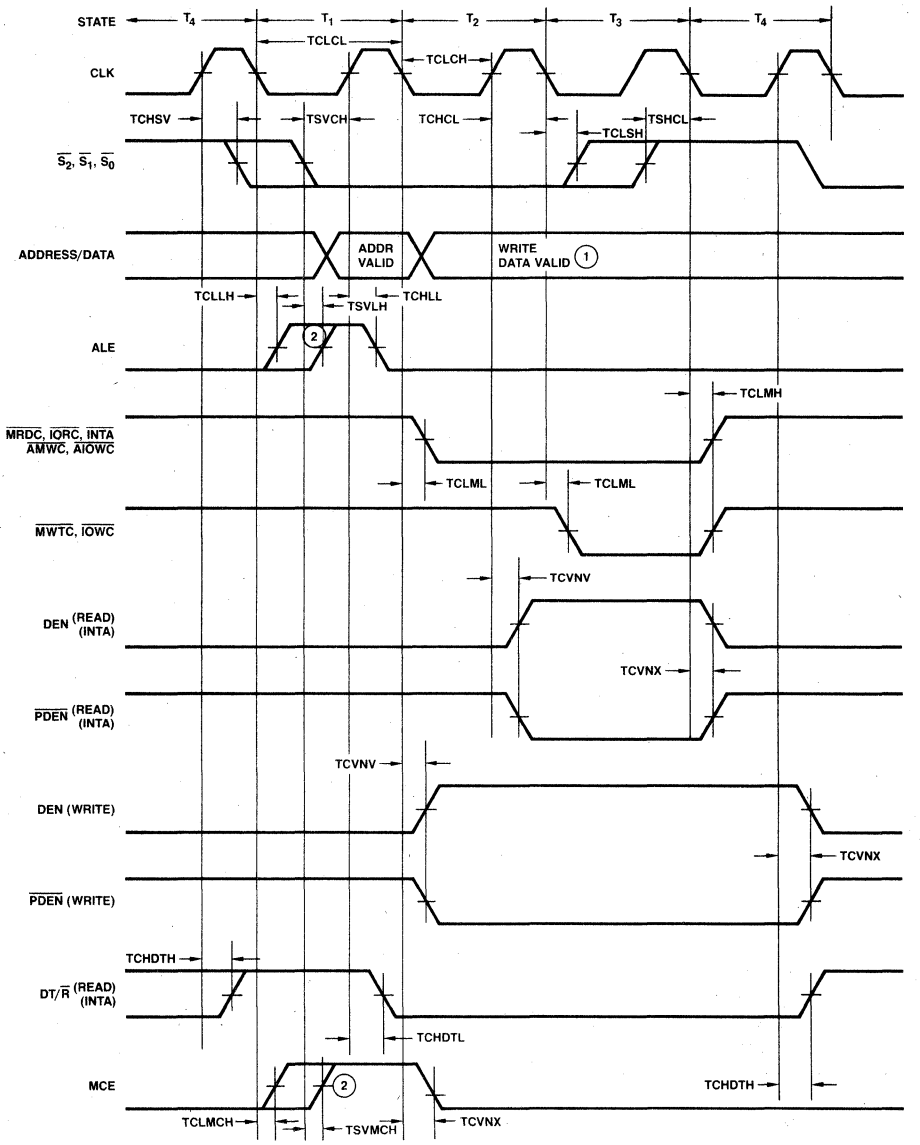
ABI-087

Control Output Test Load



ABI-088

WAVEFORMS

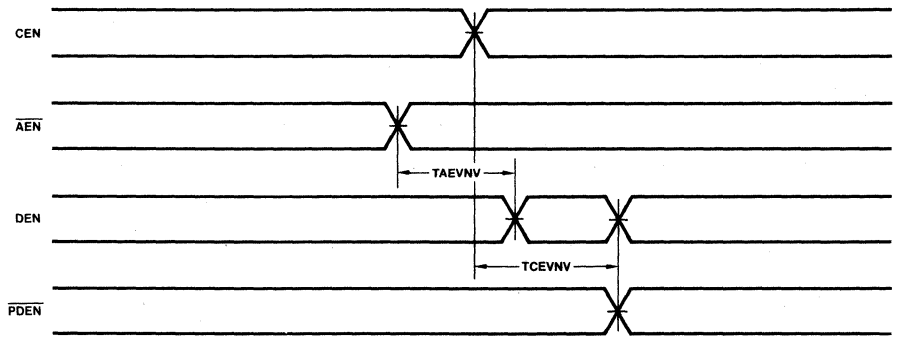


ABI-089

Notes: 1. Address/data bus is shown only for reference purposes.
2. Leading edge of ALE and MCE is determined by the falling edge of CLK or status going active, whichever occurs last.
3. All timing measurements are made at 1.5V unless specified otherwise.

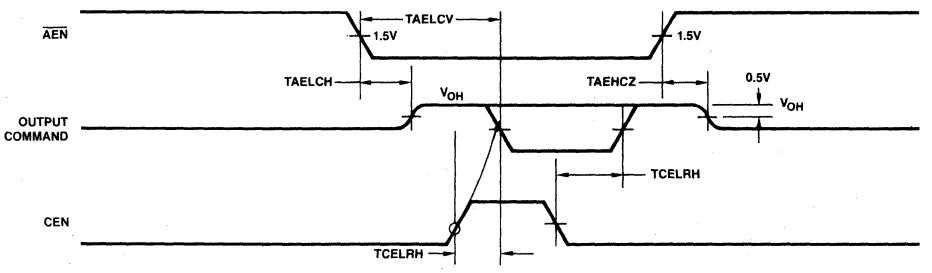
WAVEFORMS (Cont.)

DEN, PDEN QUALIFICATION TIMING



ABI-090

ADDRESS ENABLE (AEN) TIMING (3-STATE ENABLE/DISABLE)



Note: CEN must be low or valid prior to T_2 to prevent the command from being generated.

ABI-091

PALs, PROMs, MOS and Bipolar RAMs, MOS Peripherals, Analog and Data Acquisition Index

Bipolar PROM

Functional Index and Selection Guide

Part Number	Organization	Access Time COM'L/MIL Max	I_{CC} COM'L/MIL Max	Output	Number of Pins	Packages	Comments
Am27LS18[1]	32 x 8	50/65	80/80	OC	16	D, P, F, L	Low power
Am27LS19[1]	32 x 8	50/65	80/80	3S	16	D, P, F, L	
Am27S18	32 x 8	40/50	115/115	OC	16	D, P, F, L	
Am27S18A	32 x 8	25/35	115/115	OC	16	D, P, F, L	
Am27S19	32 x 8	40/50	115/115	3S	16	D, P, F, L	
Am27S19A	32 x 8	25/35	115/115	3S	16	D, P, F, L	
Am27S20	256 x 4	45/60	130/130	OC	16	D, P, F, L	
Am27S20A	256 x 4	30/40	130/130	OC	16	D, P, F, L	
Am27S21	256 x 4	45/60	130/130	3S	16	D, P, F, L	
Am27S21A	256 x 4	30/40	130/130	3S	16	D, P, F, L	
Am27S12	512 x 4	50/60	130/130	OC	16	D, P, F, L	
Am27S12A	512 x 4	30/40	130/130	OC	16	D, P, F, L	
Am27S13	512 x 4	50/60	130/130	3S	16	D, P, F, L	
Am27S13A	512 x 4	30/40	130/130	3S	16	D, P, F, L	
Am27S15	512 x 8	60/90	175/185	3S	24	D, P, F, L	
Am27S25	512 x 8	N.A.[2]/N.A.[2]	185/185	3S	24	D, P, F, L	Output registers, THINDIP Pkg[3]
Am27S25A	512 x 8	N.A.[4]/N.A.[4]	185/185	3S	24	D, P, F, L	Output registers, THINDIP Pkg[3]
Am27S27	512 x 8	N.A.[2]/N.A.[2]	185/185	3S	22	D, P, L	Output registers
Am27S28	512 x 8	55/70	160/160	OC	20	D, P, L	
Am27S28A	512 x 8	35/45	160/160	OC	20	D, P, L	
Am27S29	512 x 8	55/70	160/160	3S	20	D, P, L	
Am27S29A	512 x 8	35/45	160/160	3S	20	D, P, L	
Am27S30	512 x 8	55/70	175/175	OC	24	D, P, F, L	
Am27S30A	512 x 8	35/45	175/175	OC	24	D, P, F, L	
Am27S31	512 x 8	55/70	175/175	3S	24	D, P, F, L	
Am27S31A	512 x 8	35/45	175/175	3S	24	D, P, F, L	
Am27S32	1024 x 4	55/70	140/145	OC	18	D, P, F, L	
Am27S32A	1024 x 4	35/45	140/145	OC	18	D, P, F, L	Ultra fast
Am27S33	1024 x 4	55/70	140/145	3S	18	D, P, F, L	
Am27S33A	1024 x 4	35/45	140/145	3S	18	D, P, F, L	Ultra fast
Am27S35	1024 x 8	N.A.[2]/N.A.[2]	185	3S	24	D, P, F, L	Output registers, asynchronous initialize, THINDIP Pkg[3]
Am27S35A	1024 x 8	N.A.[4]/N.A.[4]	185	3S	24	D, P, F, L	Ultra fast, output registers, asynchronous initialize, THINDIP Pkg[3]
Am27S37	1024 x 8	N.A.[2]/N.A.[2]	185	3S	24	D, P, F, L	Output registers, synchronous initialize, THINDIP Pkg[3]

BIPOLAR PROM (Cont.)

Part Number	Organization	Access Time COM'L/MIL Max	I_{CC} COM'L/MIL Max	Output	Number of Pins	Packages	Comments
Am27S37A	1024 x 8	N.A.[4]/N.A.[4]	185	3S	24	D, P, F, L	Ultra fast, output registers, synchronous initialize, THINDIP Pkg[3]
Am27S180	1024 x 8	60/80	185/185	OC	24	D, P, F, L	
Am27S180A	1024 x 8	35/50	185/185	OC	24	D, P, F, L	Ultra fast
Am27S181	1024 x 8	60/80	185/185	3S	24	D, P, F, L	
Am27S181A	1024 x 8	35/50	185/185	3S	24	D, P, F, L	Ultra fast
Am27PS181	1024 x 8			3S	24	D, P, F, L	Power switched
Am27PS181A	1024 x 8			3S	24	D, P, F, L	Power switched
Am27S280	1024 x 8	60/80	185/185	OC	24	D, P, F, L	THINDIP Pkg[3]
Am27S280A	1024 x 8	35/50	185/185	OC	24	D, P, F, L	Ultra fast, THINDIP Pkg[3]
Am27S281	1024 x 8	60/80	185/185	3S	24	D, P, F, L	THINDIP Pkg[3]
Am27S281A	1024 x 8	35/50	185/185	3S	24	D, P, F, L	Ultra fast, THINDIP Pkg[3]
Am27PS281	1024 x 8			3S	24	D, P, F, L	Power switched, THINDIP Pkg[3]
Am27PS281A	1024 x 8			3S	24	D, P, F, L	Ultra fast, power switched, THINDIP Pkg[3]
Am27S184	2048 x 4	50/55	150/150	OC	18	D, P, F, L	
Am27S184A	2048 x 4	35/45	150/150	OC	18	D, P, F, L	Ultra fast
Am27S185	2048 x 4	50/55	150/150	3S	18	D, P, F, L	
Am27S185A	2048 x 4	35/45	150/150	3S	18	D, P, F, L	Ultra fast
Am27LS184	2048 x 4	60/65	120/125	OC	18	D, P, F, L	Low power
Am27LS185	2048 x 4	60/65	120/125	3S	18	D, P, F, L	Low power
Am27PS185	2048 x 4	60/65	150/75[5]	3S	18	D, P, F, L	Power switched
Am27S190	2048 x 8	50/65	185/185	OC	24	D, P, F, L	
Am27S190A	2048 x 8	35/50	185/185	OC	24	D, P, F, L	Ultra fast
Am27S191	2048 x 8	50/65	185/185	3S	24	D, P, F, L	
Am27S191A	2048 x 8	35/50	185/185	3S	24	D, P, F, L	Ultra fast
Am27PS191	2048 x 8	65/75	185/80[5]	3S	24	D, P, F, L	Power switched
Am27PS191A	2048 x 8	50/65	185/80[5]	3S	24	D, P, F, L	Ultra fast, power switched
Am27S290	2048 x 8	50/65	185/185	OC	24	D, P, F, L	THINDIP Pkg[3]
Am27S290A	2048 x 8	35/50	185/185	OC	24	D, P, F, L	Ultra fast, THINDIP Pkg[3]
Am27S291	2048 x 8	50/65	185/185	3S	24	D, P, F, L	THINDIP Pkg[3]
Am27S291A	2048 x 8	35/50	185/185	3S	24	D, P, F, L	Ultra fast, THINDIP Pkg[3]
Am27PS291	2048 x 8	65/75	185/80[5]	3S	24	D, P, F, L	Power switched, THINDIP Pkg[3]
Am27PS291A	2048 x 8	50/65	185/80[5]	3S	24	D, P, F, L	Ultra fast, power switched, THINDIP Pkg[3]
Am27S40	4096 x 4	50/65	165/170	OC	20	D, P, L	
Am27S40A	4096 x 4	35/50	165/170	OC	20	D, P, L	Ultra fast
Am27S41	4096 x 4	50/65	165/170	3S	20	D, P, L	
Am27S41A	4096 x 4	35/50	165/170	3S	20	D, P, L	Ultra fast
Am27PS41	4096 x 4	50/65	170/85[5]	3S	20	D, P, L	Power switched

BIPOLAR PROM (Cont.)

Part Number	Organization	Access Time COM'L/MIL Max	I_{CC} COM'L/MIL Max	Output	Number of Pins	Packages	Comments
Am27S43	4096 x 8	N.A.	185	3S	24	D, P, F, L	
Am27S43A	4096 x 8	N.A.	185	3S	24	D, P, F, L	Ultra fast
Am27PS43	4096 x 8	N.A.	N.A.	3S	24	D, P, F, L	Power switched
Am27S45	2048 x 8	N.A.[2]	185/185	3S	24	D, P, L	Output registers, asynchronous initialize, THINDIP Pkg[3]
Am27S45A	2048 x 8	N.A.[4]	185/185	3S	24	D, P, L	Ultra fast, output registers, asynchronous initialize, THINDIP Pkg[3]
Am27S47	2048 x 8	N.A.[2]	185/185	3S	24	D, P, L	Output registers, synchronous initialize, THINDIP Pkg[3]
Am27S47A	2048 x 8	N.A.[4]	185/185	3S	24	D, P, L	Ultra fast, output registers, synchronous initialize, THINDIP Pkg[3]

Notes: 1. Replaces Am27LS08/09
2. Contains built-in pipeline registers: nominal address to clock setup time = 35ns (typ), clock to output = 20ns (typ).
3. 300-mil lateral pin spacing.
4. Contains built-in pipeline registers: nominal address to clock setup time = 25ns (typ), clock to output = 15ns (typ).
5. I_{CC} are power up and power down current limits respectively.

Bipolar Memory RAM

Functional Index and Selection Guide

BIPOLAR ECL RAM

Part Number	Organization	Access Time COML/MIL Max	I_{EE} COML/MIL Max	ECL Series	Number of Pins	Packages	Comments
Am10415SA	1024 x 1	15/20	−150/−165	10K	16	D, P, F, L	
Am10415A	1024 x 1	20/25	−150/−165	10K	16	D, P, F, L	
Am10415	1024 x 1	35/40	−150/−165	10K	16	D, P, F, L	
Am100415A	1024 x 1	15/–	−150/–	100K	16	D, P, F, L	
Am100415	1024 x 1	20/–	−150/–	100K	16	D, P, F, L	
Am10470SA	4096 x 1	15/20	−230/−255	10K	18	D, F[1], L	
Am10470A	4096 x 1	25/30	−200/−220	10K	18	D, F[1], L	
Am10470	4096 x 1	35/40	−200/−220	10K	18	D, F[1], L	
Am100470SA	4096 x 1	15/–	−230/–	100K	18	D, F[1], L	
Am100470A	4096 x 1	25/–	−195/–	100K	18	D, F[1], L	
Am100470	4096 x 1	35/–	−195/–	100K	18	D, F[1], L	
Am10474A	1024 x 4	15/20	−230/−255	10K	24	D, F, L	
Am10474	1024 x 4	25/30	−230/−220	10K	24	D, F, L	
Am100474A	1024 x 4	15/–	−230/–	100K	24	D, F, L	
Am100474	1024 x 4	25/–	−200/–	100K	24	D, F, L	

Note: 1. For flat package consult factory.

BIPOLAR TTL RAM

Part Number	Organization	Access Time COML/MIL Max	I_{CC} COML/MIL Max	Output	Number of Pins	Packages (Note 1)	Comments
Am27S02A	16 x 4	25/30	100/105	OC	16	D, P, F, L	Ultra Fast
Am27S03A	16 x 4	25/30	100/105	3S	16	D, P, F, L	
Am27S02	16 x 4	35/50	105/105	OC	16	D, P, F, L	
Am27S03	16 x 4	35/50	125/125	3S	16	D, P, F, L	
Am27LS02	16 x 4	55/65	35/38	OC	16	D, P, F, L	Low Power
Am27LS03	16 x 4	55/65	35/38	3S	16	D, P, F, L	
Am74/54S289	16 x 4	35/50	105/105	OC	16	D, P, F, L	
Am74/54S189	16 x 4	35/50	125/125	3S	16	D, P, F, L	
Am27S06A	16 x 4	25/30	100/105	OC	16	D, P, F, L	Noninverting Outputs
Am27S07A	16 x 4	25/30	100/105	3S	16	D, P, F, L	
Am27S06	16 x 4	35/50	100/105	OC	16	D, P, F, L	
Am27S07	16 x 4	35/50	100/105	3S	16	D, P, F, L	
Am27LS06	16 x 4	55/65	35/38	OC	16	D, P, F, L	Noninverting Outputs, Low Power
Am27LS07	16 x 4	55/65	35/38	3S	16	D, P, F, L	
Am3101A	16 x 4	35/50	100/105	OC	16	D, P, F, L	
Am3101-1	16 x 4	35/50	100/105	OC	16	D, P, F, L	Write Transparent[2]
Am3101	16 x 4	50/60	100/105	OC	16	D, P, F, L	

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

BIPOLAR TTL RAM (Cont.)

Part Number	Organization	Access Time COM'L/MIL Max	I_{CC} COM'L/MIL Max	Output	Number of Pins	Packages (Note 1)	Comments
Am31L01A	16 x 4	55/65	35/38	OC	16	D, P, F, L	Low Power, Write Transparent[2]
Am31L01	16 x 4	80/90	35/38	OC	16	D, P, F, L	
Am74/5489-1	16 x 4	35/50	100/105	OC	16	D, P, F, L	Write Transparent[2]
Am74/5489	16 x 4	50/60	100/105	OC	16	D, P, F, L	
Am27LS00A	256 x 1	35/45	115/115	3S	16	D, P, F, L	Ultra Fast
Am27LS01A	256 x 1	35/45	115/115	OC	16	D, P, F, L	
Am27LS00	256 x 1	45/55	70/70	3S	16	D, P, F, L	Fast, Low Power
Am27LS01	256 x 1	45/55	70/70	OC	16	D, P, F, L	
Am27LS00-1A	256 x 1	35/45	115/115	3S	16	D, P, F, L	Noninverting Outputs
Am27LS01-1A	256 x 1	35/45	115/115	OC	16	D, P, F, L	
Am27LS00-1	256 x 1	45/55	70/70	3S	16	D, P, F, L	
Am27LS01-1	256 x 1	45/55	70/70	OC	16	D, P, F, L	
Am93415A	1024 x 1	30/40	155/170	OC	16	D, P, F, L	Ultra Fast
Am93425A	1024 x 1	30/40	155/170	3S	16	D, P, F, L	
Am93415	1024 x 1	45/65	155/170	OC	16	D, P, F, L	
Am93425	1024 x 1	45/65	155/170	3S	16	D, P, F, L	
Am93412A	256 x 4	35/45	155/170	OC	22[3]	D, P, F, L	Ultra Fast
Am93422A	256 x 4	35/45	155/170	3S	22[3]	D, P, F, L	
Am93412	256 x 4	45/60	155/170	OC	22[3]	D, P, F, L	
Am93422	256 x 4	45/60	155/170	3S	22[3]	D, P, F, L	
Am93L412A	256 x 4	45/55	80/90	OC	22[3]	D, P, F, L	Low Power
Am93L422A	256 x 4	45/55	80/90	3S	22[3]	D, P, F, L	
Am93L412	256 x 4	60/75	80/90	OC	22[3]	D, P, F, L	
Am93L422	256 x 4	60/75	80/90	3S	22[3]	D, P, F, L	

Notes: 1. D = Hermetic DIP, P = Molded DIP, F = Cerpak, L = Chip-Pak™.
2. Complement of data in is available on the outputs in the write mode when both $\overline{CS}$ and $\overline{WE}$ are low.
3. Cerpak (F) is 24 pin.

MOS Memory

1K STATIC RAMs *Functional Index and Selection Guide*

Part Number	Organization	Access Time (ns)	Power Dissipation (mW) Standby	Active	Pins	Supply Voltage (V)	Temp Range	Package
Am9101A	256 x 4	500	47	290	22	5	C, M	D, P
Am91L01A	256 x 4	500	38	173	22	5	C, M	D, P
Am9101B	256 x 4	400	47	290	22	5	C, M	D, P
Am91L01B	256 x 4	400	38	173	22	5	C, M	D, P
Am9101C	256 x 4	300	47	315	22	5	C, M	D, P
Am91L01C	256 x 4	300	38	189	22	5	C, M	D, P
Am9101D	256 x 4	250	47	315	22	5	C	D, P
Am9111A	256 x 4	500	47	290	18	5	C, M	D, P
Am91L11A	256 x 4	500	38	173	18	5	C, M	D, P
Am9111B	256 x 4	400	47	290	18	5	C, M	D, P
Am91L11B	256 x 4	400	38	173	18	5	C, M	D, P
Am9111C	256 x 4	300	47	315	18	5	C, M	D, P
Am91L11C	256 x 4	300	38	189	18	5	C, M	D, P
Am9111D	256 x 4	250	47	315	18	5	C	D, P
Am9112A	256 x 4	500	47	290	16	5	C, M	D, P
Am91L12A	256 x 4	500	38	173	16	5	C, M	D, P
Am9112B	256 x 4	400	47	290	16	5	C, M	D, P
Am91L12B	256 x 4	400	38	173	16	5	C, M	D, P
Am9112C	256 x 4	300	47	315	16	5	C, M	D, P
Am91L12C	256 x 4	300	38	189	16	5	C, M	D, P
Am9112D	256 x 4	250	47	315	16	5	C	D, P
Am9122-25	256 x 4	25	–	660	22	5	C	D, P
Am9122-35	256 x 4	35	–	660	22	5	C, M	D, P
Am91L22-35	256 x 4	35	–	440	22	5	C	D, P
Am91L22-45	256 x 4	45	–	440	22	5	C, M	D, P
Am91L22-60	256 x 4	60	–	248	22	5	C	D, P

4K STATIC RAMs

Am21L41-12	4096 x 1	120	25	200	18	5	C	D, P
Am21L41-15	4096 x 1	150	25	200	18	5	C	D, P
Am21L41-20	4096 x 1	200	25	200	18	5	C	D, P
Am21L41-25	4096 x 1	250	25	250	18	5	C	D, P
Am9044B	4096 x 1	450		350	18	5	C, M	D, P
Am90L44B	4096 x 1	450		250	18	5	C, M	D, P
Am9044C	4096 x 1	300		350	18	5	C, M	D, P
Am90L44C	4096 x 1	300		250	18	5	C, M	D, P
Am9044D	4096 x 1	250		350	18	5	C, M	D, P
Am90L44D	4096 x 1	250		250	18	5	C, M	D, P
Am9044E	4096 x 1	200		350	18	5	C	D, P
Am90L44E	4096 x 1	200		250	18	5	C	D, P
Am9244B	4096 x 1	450	150	350	18	5	C, M	D, P
Am92L44B	4096 x 1	450	100	250	18	5	C, M	D, P
Am9244C	4096 x 1	300	150	350	18	5	C, M	D, P
Am92L44C	4096 x 1	300	100	250	18	5	C, M	D, P
Am9244D	4096 x 1	250	150	350	18	5	C, M	D, P
Am92L44D	4096 x 1	250	100	250	18	5	C, M	D, P
Am9244E	4096 x 1	200	150	350	18	5	C	D, P
Am92L44E	4096 x 1	200	100	250	18	5	C	D, P
Am9114B	1024 x 4	450		350	18	5	C, M	D, P, F
Am91L14B	1024 x 4	450		250	18	5	C, M	D, P, F
Am9114C	1024 x 4	300		350	18	5	C, M	D, P, F
Am91L14C	1024 x 4	300		250	18	5	C, M	D, P, F
Am9114E	1024 x 4	200		350	18	5	C, M	D, P
Am91L14E	1024 x 4	200		250	18	5	C	D, P
Am9124B	1024 x 4	450	150	350	18	5	C, M	D, P, F
Am91L24B	1024 x 4	450	100	250	18	5	C, M	D, P, F
Am9124C	1024 x 4	300	150	350	18	5	C, M	D, P, F
Am91L24C	1024 x 4	300	100	250	18	5	C, M	D, P, F

4K STATIC RAMs (Cont.)

Part Number	Organization	Access Time (ns)	Power Dissipation (mW) Standby	Active	Pins	Supply Voltage (V)	Temp. Range	Package
Am2147-35	4096 x 1	35	165	990	18	5	C	D
Am2147-45	4096 x 1	45	165	990	18	5	M	D, L
Am2147-55	4096 x 1	55	165	990	18	5	C, M	D, L
Am2147-70	4096 x 1	70	110	880	18	5	C, M	D, L
Am21L47-45	4096 x 1	45	83	688	18	5	C	D
Am21L47-55	4096 x 1	55	83	688	18	5	C	D
Am2148-55	1024 x 4	55	165	990	18	5	C, M	D, L
Am2148-70	1024 x 4	70	165	990	18	5	C, M	D, L
Am2149-55	1024 x 4	55	–	990	18	5	C, M	D, L
Am2149-70	1024 x 4	70	–	990	18	5	C, M	D, L

16K STATIC RAMs

Part Number	Organization	Access Time (ns)	Power Dissipation (mW) Standby	Active	Pins	Supply Voltage (V)	Temp Range	Package
Am9128-10	2048 x 8	100	83	660	24	5	C	D, P
Am9128-15	2048 x 8	150	83	550	24	5	C, M	D, P
Am9128-20	2048 x 8	200	165	660	24	5	C, M	D, P
Am9128-70*	2048 x 8	70	165	770	24	5	C	D, P
Am9167-45*	16384 x 1	45	165	660	20	5	C	D
Am9167-55*	16384 x 1	55	165	660	20	5	C, M	D
Am9168-45*	4096 x 4	45	165	660	20	5	C	D
Am9168-55*	4096 x 4	55	165	660	20	5	C, M	D

*Available in 1983.

DYNAMIC RAMs

Part Number	Organization	Access Time (ns)	Power Dissipation (mW) Standby	Active	Pins	Supply Voltage (V)	Temp Range	Package
Am9016C	16384 x 1	300	20	420	16	+12 ±5	C, L	P, D, L
Am9016D	16384 x 1	250	20	420	16	+12 ±5	C, L	P, D, L
Am9016E	16384 x 1	200	20	420	16	+12 ±5	C, L	P, D, L
Am9016F	16384 x 1	150	20	420	16	+12 ±5	C	P, D, L

ROMs

Part Number	Organization	Access Time (ns)	Temp Range	Supply Voltage	Pins	Operating Power Max (mW)	Outputs
8316E	2048 x 8	450	C, M	+5	24	499	3-State
Am9218B	2048 x 8	450	C, M	+5	24	368	3-State
Am9218C	2048 x 8	350	C	+5	24	368	3-State
Am9232B	4096 x 8	450	C, M	+5	24	420	3-State
Am9232C	4096 x 8	300	C	+5	24	420	3-State
Am9232D	4096 x 8	250	C	+5	24	420	3-State
Am9233B	4096 x 8	450	C, M	+5	24	420	3-State
Am9233C	4096 x 8	300	C	+5	24	420	3-State
Am9233D	4096 x 8	250	C	+5	24	420	3-State
Am9264B	8192 x 8	450	C, M	+5	24	440	3-State
Am9264C	8192 x 8	300	C	+5	24	440	3-State
Am9264D	8192 x 8	250	C	+5	24	440	3-State
Am9265B	8192 x 8	450	C, M	+5	28	440, 110[1]	3-State
Am9265C	8192 x 8	300	C	+5	28	440, 110[1]	3-State
Am9265D	8192 x 8	250	C	+5	28	440, 110[1]	3-State
Am92128B	16384 x 8	450	C, M	+5	28	440, 137[1]	3-State
Am92128C	16384 x 8	300	C	+5	28	440, 137[1]	3-State
Am92128D	16384 x 8	250	C	+5	28	440, 137[1]	3-State
Am92256B	32768 x 8	450	C	+5	28	660, 165[1]	3-State
Am92256C	32768 x 8	300	C	+5	28	660, 165[1]	3-State
Am92256D	32768 x 8	250	C	+5	28	660, 165[1]	3-State

Note: 1. Standby

AMD 20-Pin PAL* Family

20-Pin IMOX™ Programmable Array Logic Elements

DISTINCTIVE CHARACTERISTICS

- **Fast**
  - High speed "A" versions (t_{pd} = 25ns, t_s = 20ns, t_{co} = 15ns, max)
  - Standard speed versions (t_{pd} = 35ns, t_s = 30ns, t_{co} = 25ns, max)
- **Flexible**
  - User programmability allows customized designs
  - Eases design updates in prototype or product
- **Low Cost**
  - Reduces board space/chip count
  - Reduces design time
  - Reduces inventory cost
- **Reliable**
  - Proven Platinum-Silicide fuse technology
  - Fully AC and DC tested
  - Preload of output registers allows full logical testing

FUNCTIONAL DESCRIPTION

AMD PALs are high speed electrically programmable array logic elements. They utilize the familiar sum-of-products (AND-OR) structure allowing users to program custom logic functions to fit most applications precisely.

Initially the AND gates are connected, via fuses, to both the true and complement of every input. By selective programming of fuses the AND gates may be "connected" to only the true input (by blowing the complement fuse), to only the complement input (by blowing the true fuse), or to neither type of input (by blowing both fuses) establishing a logical "don't care." When both the true and complement fuses are left intact a logical false results on the output of the AND gate. An AND gate with all fuses blown will assume the logical true state. The outputs of the AND gates are connected to fixed OR gates. The only limitations imposed are the number of inputs to the AND gates (up to 16) and the number of AND gates per OR (up to 8).

The part types in the AMD PAL family are differentiated by the allocation of registered (with internal feedback) and combinatorial (bi-directional and dedicated) outputs. All combinatorial AMD PALs are available in both active HIGH (AND-OR) and active LOW (AND-OR-INVERT) versions.

AMD PAL FAMILY CHARACTERISTICS

All members of the AMD PAL family have common electrical characteristics and programming procedures. All parts in this family are produced with a fusible link at each input to the AND gate array. Connections may be selectively removed by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming, highly reliable Platinum-Silicide Fuse technology. Utilizing an easily implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields (>98%), and provide extra test paths to achieve excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable, long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link programmable logic.

The AMD PAL family is manufactured using Advanced Micro Devices' selective oxidation process, IMOX. This advanced process permits an increase in density and a decrease in internal capacitance resulting in the fastest possible programmable logic devices.

The AMD PAL family also incorporates the unique capability of preloading the output registers during testing to any desired value. Preload is invaluable when testing the logical functionality of a programmed AMD PAL.

AMD PAL FAMILY TABLE

Part Number	Array Inputs	Logic	OE	Outputs	t_{pd} (MAX) STD	t_{pd} (MAX) A	t_s (MAX) STD	t_s (MAX) A	t_{co} (MAX) STD	t_{co} (MAX) A	
AmPAL16R8	(8) Dedicated (8) Feedback	(8) 8-Wide AND-OR	Dedicated	Registered Inverting	–	–	30	20	25	15	ns
AmPAL16R6	(8) Dedicated (6) Feedback (2) Bidirectional	(6) 8-Wide AND-OR	Dedicated	Registered Inverting	35	25	30	20	25	15	ns
		(2) 7-Wide AND-OR-INVERT	Programmable	Bidirectional							
AmPAL16R4	(8) Dedicated (4) Feedback (4) Bidirectional	(4) 8-Wide AND-OR	Dedicated	Registered Inverting	35	25	30	20	25	15	ns
		(4) 7-Wide AND-OR-INVERT	Programmable	Bidirectional							
AmPAL16L8	(10) Dedicated (6) Bidirectional	(8) 7-Wide AND-OR-INVERT	Programmable	(6) Bidirectional (2) Dedicated	35	25	–	–	–	–	ns
AmPAL16H8	(10) Dedicated (6) Bidirectional	(8) 7-Wide AND-OR	Programmable	(6) Bidirectional (2) Dedicated	35	25	–	–	–	–	ns
AmPAL16LD8	(10) Dedicated (6) Bidirectional	(8) 8-Wide AND-OR-INVERT	–	Dedicated	35	25	–	–	–	–	ns
AmPAL16HD8	(10) Dedicated (6) Bidirectional	(8) 8-Wide AND-OR	–	Dedicated	35	25	–	–	–	–	ns

*PAL is a registered trademark of Monolithic Memories, Inc.
IMOX is a trademark of Advanced Micro Devices, Inc.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65 to +150°C
Temperature (Ambient) Under Bias	−55 to +125°C
Supply Voltage to Ground Potential (Pin 20 to Pin 10) Continuous	−0.5 to +7V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max
DC Voltage Applied to Outputs During Programming	21V
Output Current Into Outputs During Programming (Max Duration of 1 sec)	200mA
DC Input Voltage	−0.5 to +5.5V
DC Input Current	−30 to +5mA

OPERATING RANGE

		Commercial		Military		
Parameters	**Description**	**Min**	**Max**	**Min**	**Max**	**Units**
V_{CC}	Supply Voltage	4.75	5.25	4.50	5.50	V
T_A	Operating Free Air Temperature	0	75	−55		°C
T_C	Operating Case Temperature				125	°C

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	**Description**	**Test Conditions**			**Min**	**Typ (Note 1)**	**Max**	**Units**
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2mA	COM'L	2.4	3.5		Volts
			I_{OH} = −2mA	MIL				
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	COM'L			0.50	Volts
			I_{OL} = 12mA	MIL				
V_{IH} (Note 2)	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL} (Note 2)	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.40V				−20	−250	μA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V					25	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.5V (Note 3)			−30	−60	−90	mA
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX	16L8, 16H8, 16HD8, 16LD8 16L8A, 16H8A, 16HD8A, 16LD8A			110	155	mA
			16R8, 16R6, 16R4 16R8A, 16R6A, 16R4A			120	180	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−0.9	−1.2	Volts
I_{OZH}	Output Leakage Current (Note 4)	V_{CC} = MAX, V_{IL} = 0.8V V_{IH} = 2.0V	V_O = 2.7V				100	μA
I_{OZL}			V_O = 0.4V				−100	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @f = 1MHz (Note 5)				6		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @f = 1MHz (Note 5)				9		

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. I/O pin leakage is the worst case of I_{OZX} or I_{IX} (where X = H or L).
5. These parameters are not 100% tested, but are periodically sampled.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)

HIGH SPEED

Parameters	Description	Test Conditions	Typ (Note 1)	COM'L Min	COM'L Max	MIL Min	MIL Max	Units
t_{PD}	Input or Feedback to Non-Registered Output 16L8A, 16R6A, 16R4A, 16LD8A, 16H8A, 16HD8A	COM'L $R_1 = 200$ $R_2 = 390$	12		25		30	ns
t_{EA}	Input to Output Enable 16L8A, 16R6A, 16R4A, 16H8A		12		25		30	ns
t_{ER}	Input to Output Disable 16L8A, 16R6A, 16R4A, 16H8A		12		25		30	ns
t_{PZX}	Pin 11 to Output Enable 16R8A, 16R6A, 16R4A		8		20		25	ns
t_{PXZ}	Pin 11 to Output Disable 16R8A, 16R6A, 16R4A		8		20		25	ns
t_{CO}	Clock to Output 16R8A, 16R6A, 16R4A		8		15		20	ns
t_S	Input or Feedback Setup Time 16R8A, 16R6A, 16R4A	MIL $R_1 = 390$ $R_2 = 750$	10	20		25		ns
t_H	Hold Time 16R8A, 16R6A, 16R4A		−10	0		0		ns
t_P	Clock Period			35		45		ns
t_W	Clock Width			15		20		ns
f_{MAX}	Maximum Frequency				28.5		22	MHz

Notes: 1. Typical limits are at $V_{CC} = 5.0V$ and $T_A = 25°C$.
2. t_{PD} is tested with switch S_1 closed and $C_L = 50pF$.
3. For three-state outputs, output enable times are tested with $C_L = 50pF$ to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with $C_L = 5pF$. HIGH to high impedance tests are made to an output voltage of $V_{OH} - 0.5V$ with S_1 open; LOW to high impedance tests are made to the $V_{OL} + 0.5V$ level with S_1 closed.

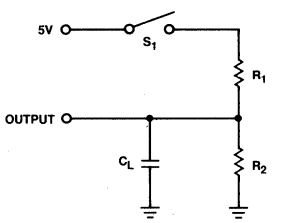
SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)

STANDARD SPEED

Parameters	Description	Test Conditions	Typ (Note 1)	COM'L Min	COM'L Max	MIL Min	MIL Max	Units
t_{PD}	Input or Feedback to Non-Registered Output 16L8, 16R6, 16R4, 16LD8, 16H8, 16HD8	COM'L $R_1 = 200$ $R_2 = 390$	17		35		40	ns
t_{EA}	Input to Output Enable 16L8, 16R6, 16R4, 16H8		17		35		40	ns
t_{ER}	Input to Output Disable 16L8, 16R6, 16R4, 16H8		17		35		40	ns
t_{PZX}	Pin 11 to Output Enable 16R8, 16R6, 16R4		12		25		25	ns
t_{PXZ}	Pin 11 to Output Disable 16R8, 16R6, 16R4		12		25		25	ns
t_{CO}	Clock to Output 16R8, 16R6, 16R4		12		25		25	ns
t_S	Input or Feedback Setup Time 16R8, 16R6, 16R4	MIL $R_1 = 390$ $R_2 = 750$	15	30		35		ns
t_H	Hold Time 16R8, 16R6, 16R4		−10	0		0		ns
t_P	Clock Period			55		60		ns
t_W	Clock Width			20		25		ns
f_{MAX}	Maximum Frequency				18		16.5	MHz

Notes: 1. Typical limits are at $V_{CC} = 5.0V$ and $T_A = 25°C$.
2. t_{PD} is tested with switch S_1 closed and $C_L = 50pF$.
3. For three-state outputs, output enable times are tested with $C_L = 50pF$ to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with $C_L = 5pF$. HIGH to high impedance tests are made to an output voltage of $V_{OH} - 0.5V$ with S_1 open; LOW to high impedance tests are made to the $V_{OL} + 0.5V$ level with S_1 closed.

AC TEST LOAD



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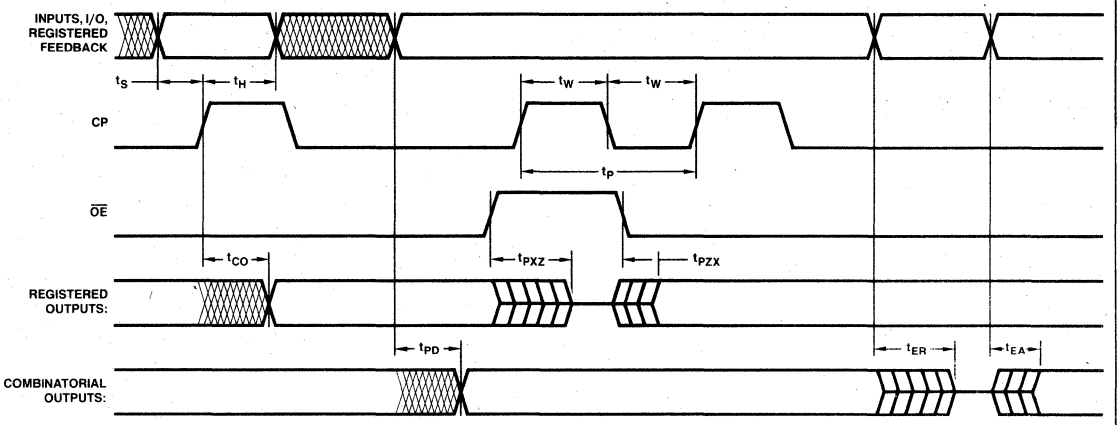
SWITCHING WAVEFORMS



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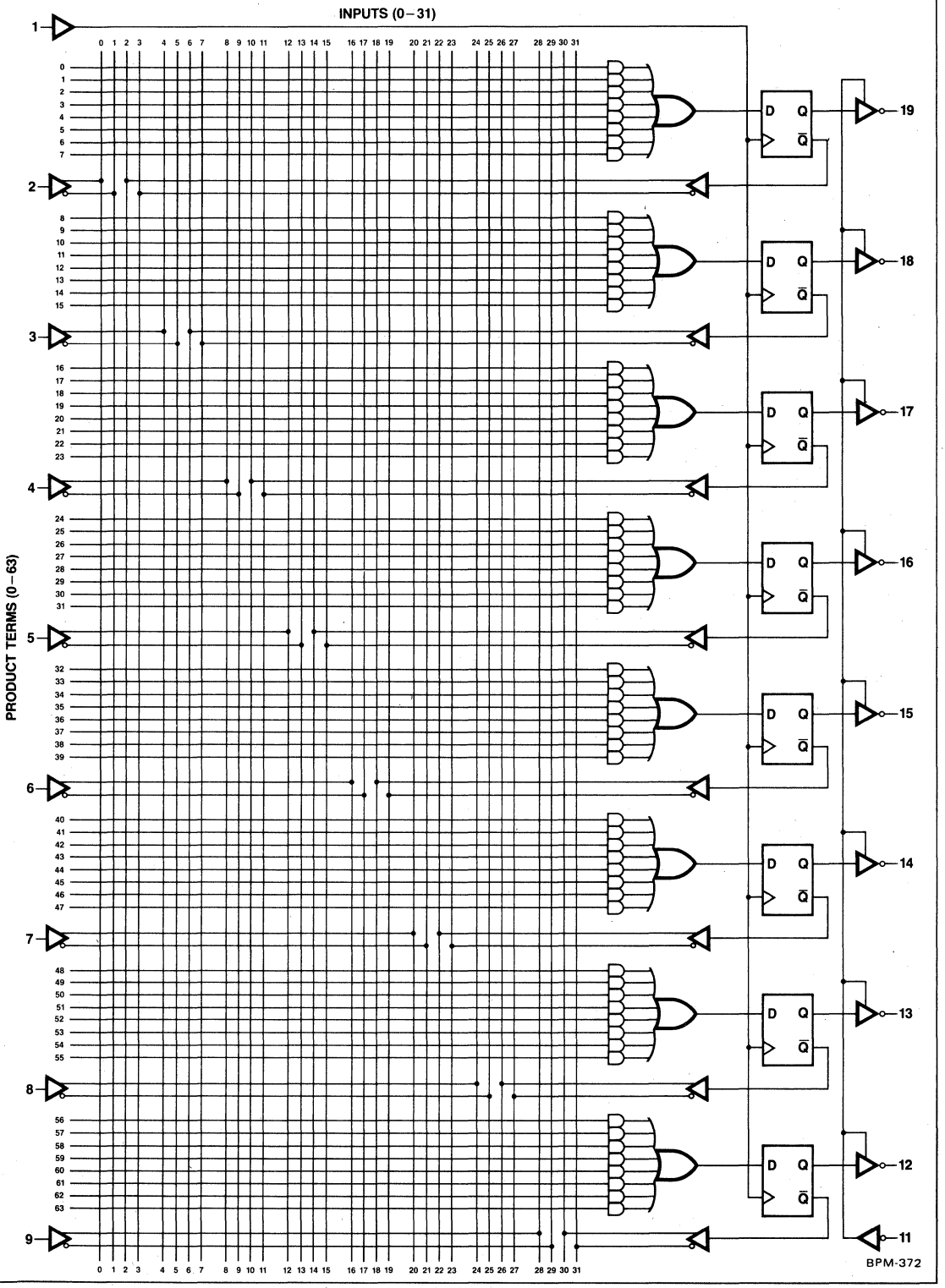
KEY TO TIMING DIAGRAM

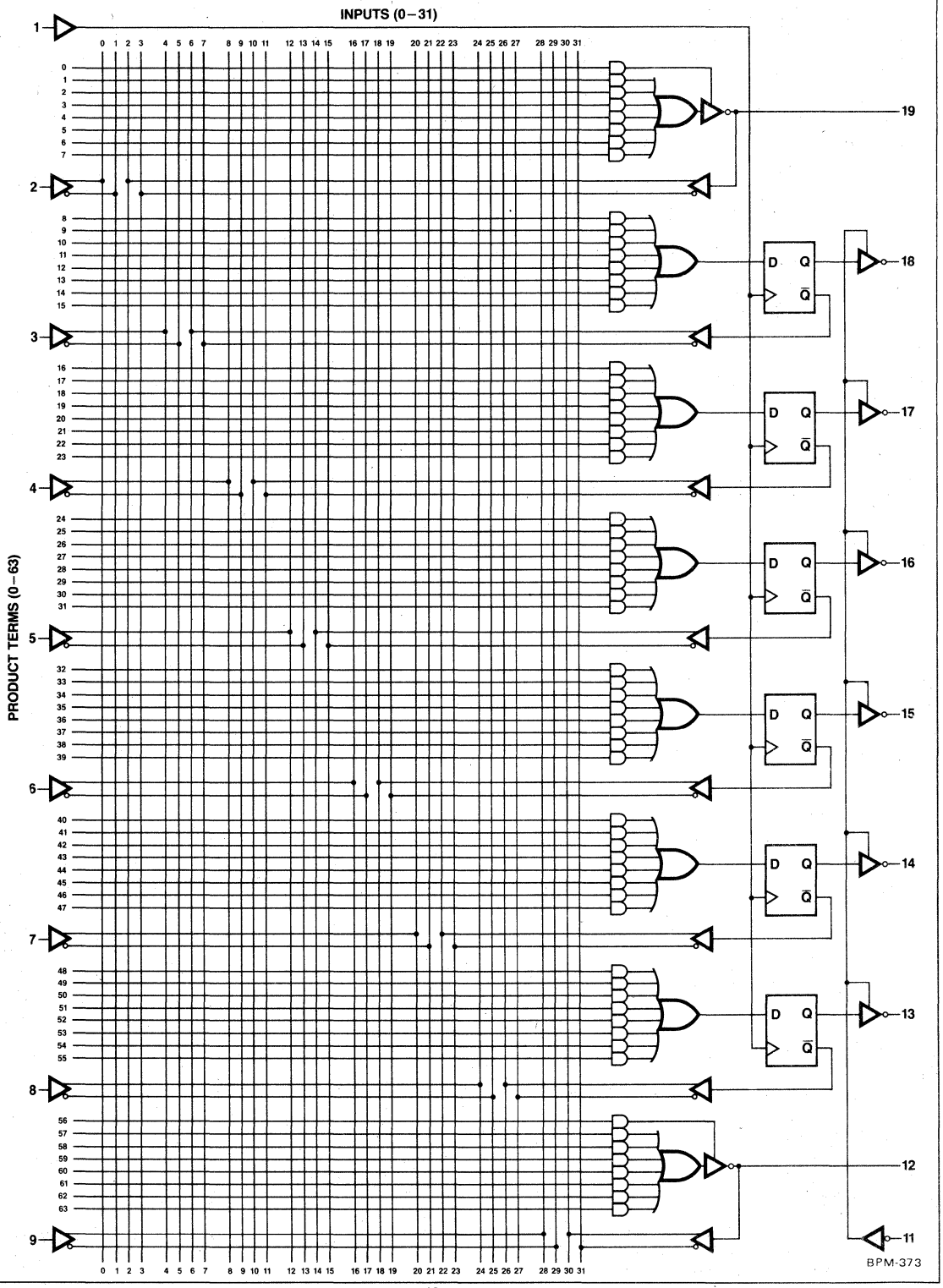
WAVEFORM	INPUTS	OUTPUTS
——— / ———	MUST BE STEADY	WILL BE STEADY

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

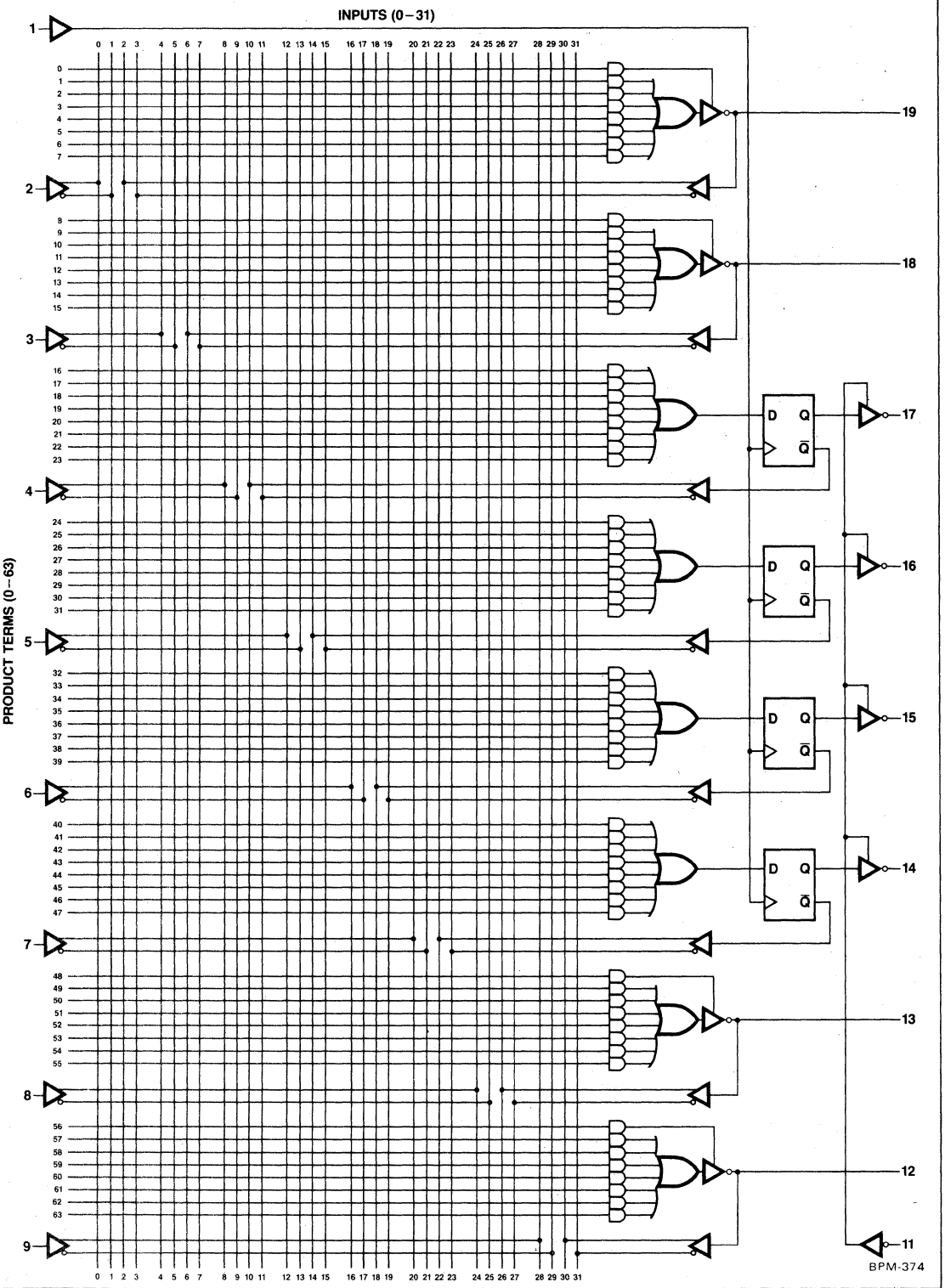
LOGIC DIAGRAM AmPAL16R8/AmPAL16R8A



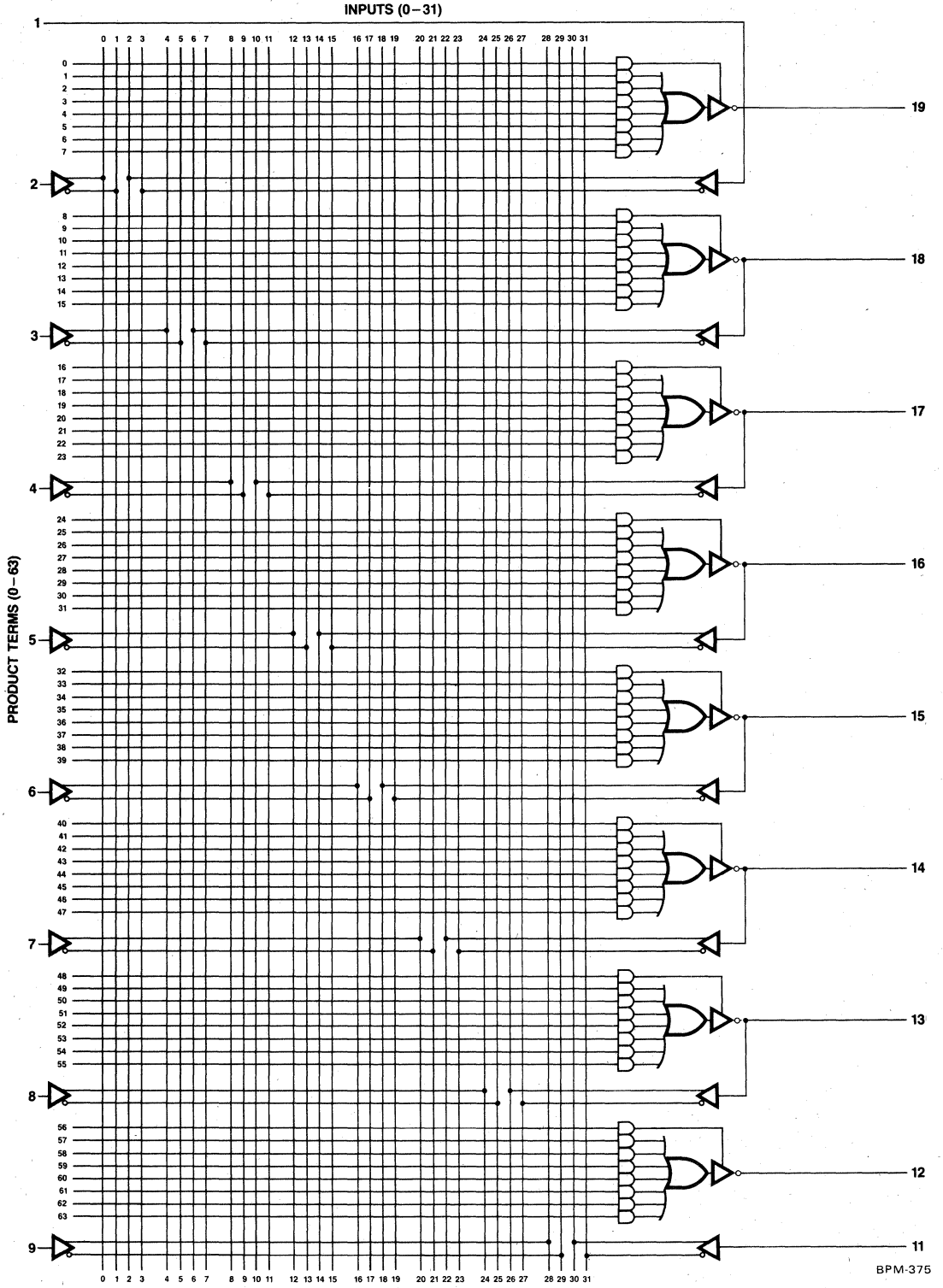
LOGIC DIAGRAM AmPAL16R6/AmPAL16R6A



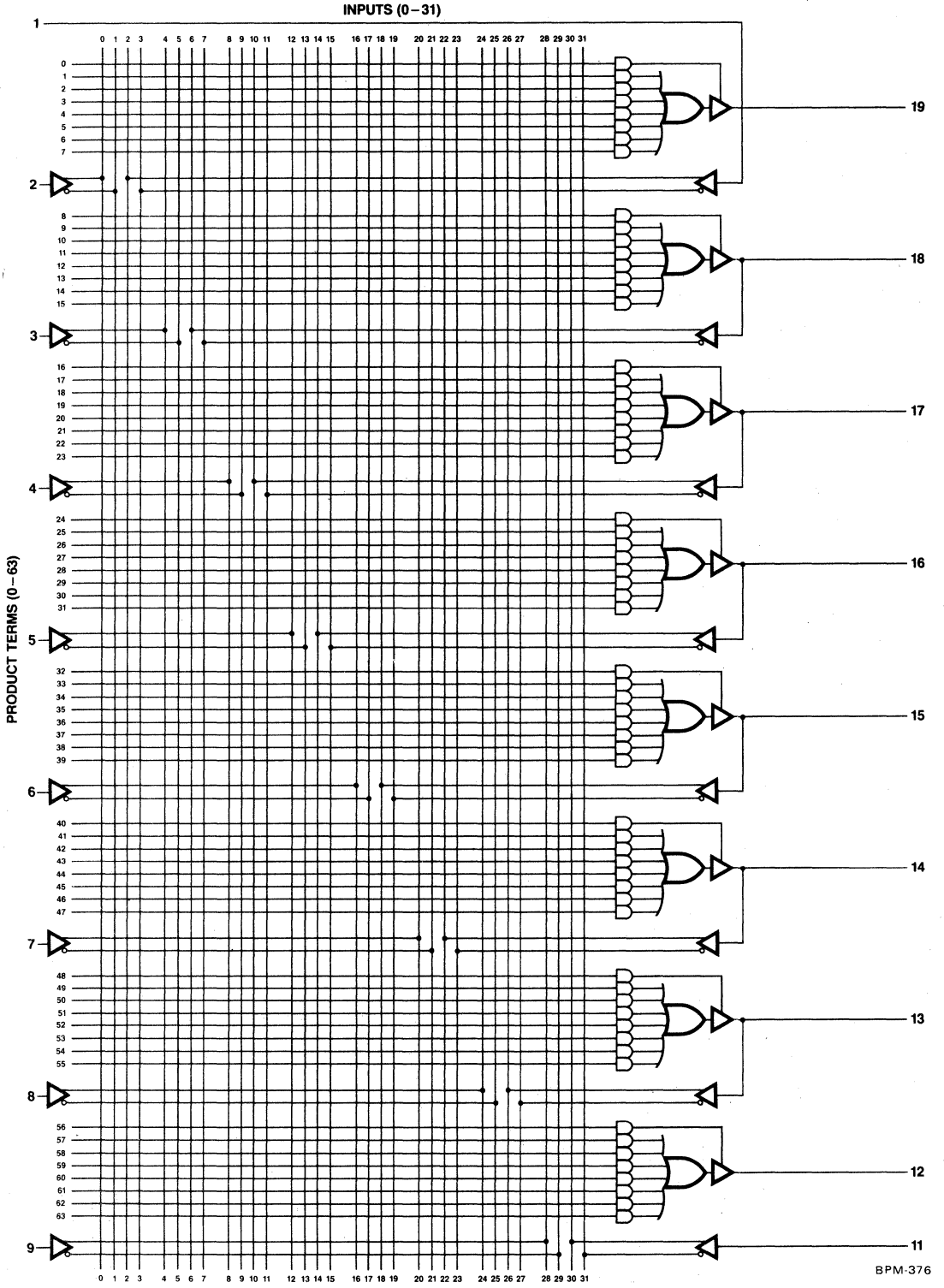
LOGIC DIAGRAM AmPAL16R4/AmPAL16R4A



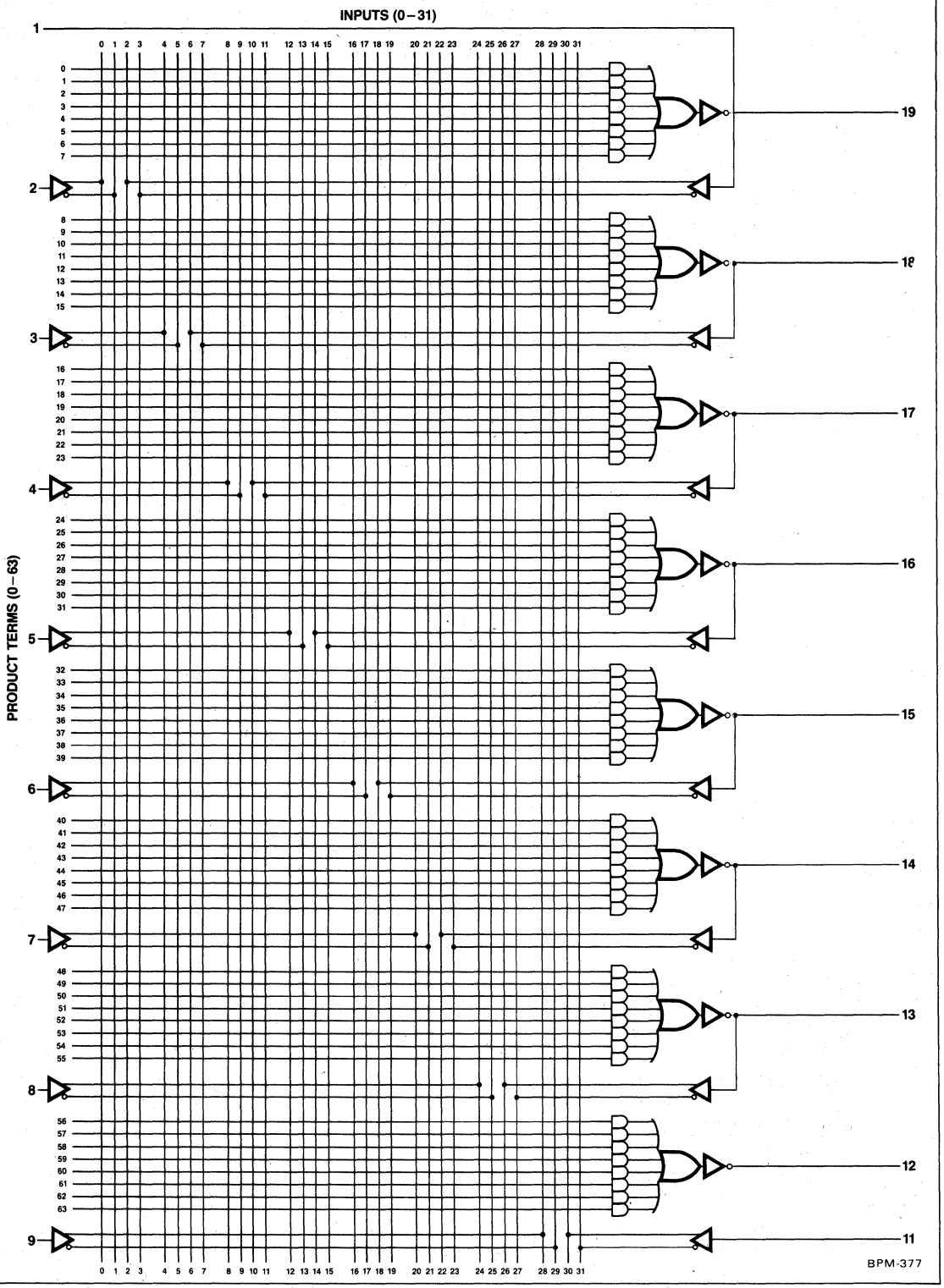
LOGIC DIAGRAM AmPAL16L8/AmPAL16L8A



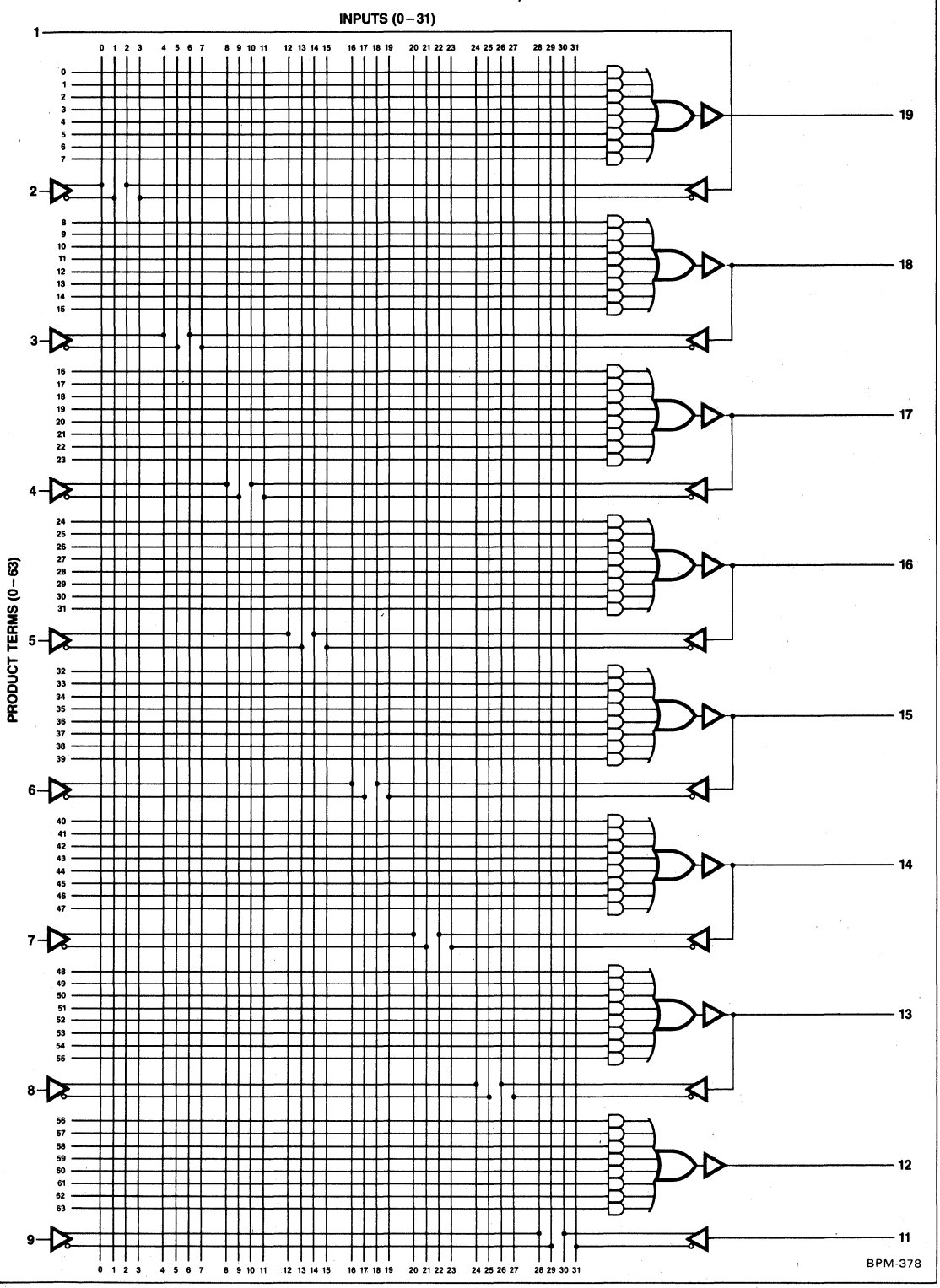
LOGIC DIAGRAM AmPAL16H8/AmPAL16H8A



LOGIC DIAGRAM AmPAL16LD8/AmPAL16LD8A



LOGIC DIAGRAM AmPAL16HD8/AmPAL16HD8A



PROGRAMMING

Each AMD PAL fuse is programmed with a simple sequence of voltages applied to two control pins (1 and 11) and a programming voltage pulse applied to the output under programming. Addressing of the 2048 element fuse array is accomplished with normal TTL levels on eight input pins (five select the input line number and three select the product term number). V_{CC} is maintained at a normal level throughout the programming and verify cycle – no extra high levels are required.

The necessary sequence of levels for programming any fuse is shown in the Programming Timing Diagram. The address of each fuse in terms of Input Line Number and Product Term Line Number is defined by the Fuse Address Tables 1 and 2. Current, voltage and timing requirements for each pin are specified in the Programming Parameter Table below.

The 16L8, 16R8, 16R6, 16R4, 16H8, 16LD8 and 16HD8 use identical programming conditions and sequences.

After all programming has been completed, the entire array should be reverified at V_{CCL} and again at V_{CCH}. Reverification can be accomplished by reading all eight outputs in parallel rather than one at a time. The array fuse verification cycle checks that the correct array fuses have been blown and can be sensed by the outputs.

AMD PALs have been designed with many internal test features that are used to assure high programming yield and correct logical operation for a correctly programmed part.

An additional fuse is provided on each AMD PAL circuit to prevent unauthorized copying of AMD PAL fuse patterns when design security is desired. Blowing the security fuse blocks entry to the fuse pattern verify mode.

To blow the security fuse:
1. Power up part to V_{CCP}
2. Raise Pin 5 to V_{HH}.
3. Pulse Pin 11 from ground to V_{OP} for a 50μsec duration.
4. Perform a normal end-of-programming verify cycle at V_{CCL} and V_{CCH}. All fuse locations should be sensed as blown if the security fuse has been successfully blown.

Note that parts with the security fuse blown may not be returned as programming rejects.

AMD PALs normally have high programming yields (>98%). Programming yield losses are frequently due to poor socket contact, equipment out of calibration or improperly used.

PROGRAMMING PARAMETERS T_A = 25°C

Parameters	Description		Min	Typ	Max	Units
V_{HH}	Control Pin Extra High Level	Pin 1 @ 10–40mA	10	11	12	Volts
		Pin 11 @ 10–40mA	10	11	12	
V_{OP}	Program Voltage Pins 12–19 @ 15–200mA		18	20	22	Volts
V_{IHP}	Input High Level During Programming and Verify		2.4	5	5.5	Volts
V_{ILP}	Input Low Level During Programming and Verify		0.0	0.3	0.5	Volts
V_{CCP}	V_{CC} During Programming @ I_{CC} = 50–200mA		5	5.2	5.5	Volts
V_{CCL}	V_{CC} During First Pass Verification @ I_{CC} = 50–200mA		4.1	4.3	4.5	Volts
V_{CCH}	V_{CC} During Second Pass Verification @ I_{CC} = 50–200mA		5.4	5.7	6.0	Volts
V_{Blown}	Successful Blown Fuse Sense Level @ Output	16L8, 16R8, 16R6, 16R4, 16LD8 16L8A, 16R8A, 16R6A, 16R4A, 16LD8A		0.3	0.5	Volts
		16H8, 16HD8, 16H8A, 16HD8A	2.4	3		
dV_{OP}/dt	Rate of Output Voltage Change		20		250	V/μsec
dV_{11}/dt	Rate of Fusing Enable Voltage Change (Pin 11 Rising Edge)		100		1000	V/μsec
t_P	Fusing Time First Attempt		40	50	100	μsec
	Subsequent Attempts		4	5	10	msec
t_D	Delays Between Various Level Changes		100	200	1000	ns
t_V	Period During which Output is Sensed for V_{Blown} Level				500	ns
V_{ONP}	Pull-Up Voltage On Outputs Not Being Programmed		V_{CCP} – 0.3	V_{CCP}	V_{CCP} + 0.3	Volts
R	Pull-Up Resistor On Outputs Not Being Programmed		1.9	2	2.1	KΩ

AMD PAL PROGRAMMING EQUIPMENT INFORMATION

Source and Location	Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052	Kontron Electronics, Inc. 630 Price Avenue Redwood City, CA 94063	Stag Microsystems 528-5 Weddel Drive Sunnyvale, CA 94086
Programmer Model(s)	Model-100, 29, 19 or 17	Model-MPP-80S or EPP80	Model-PPX
AMD PAL Personality Module	Logicpak 950-1942-001	MOD-33	PPM2200
Socket Adapter	715-1947-003	SA37	Am202S

PROGRAMMING WAVEFORMS

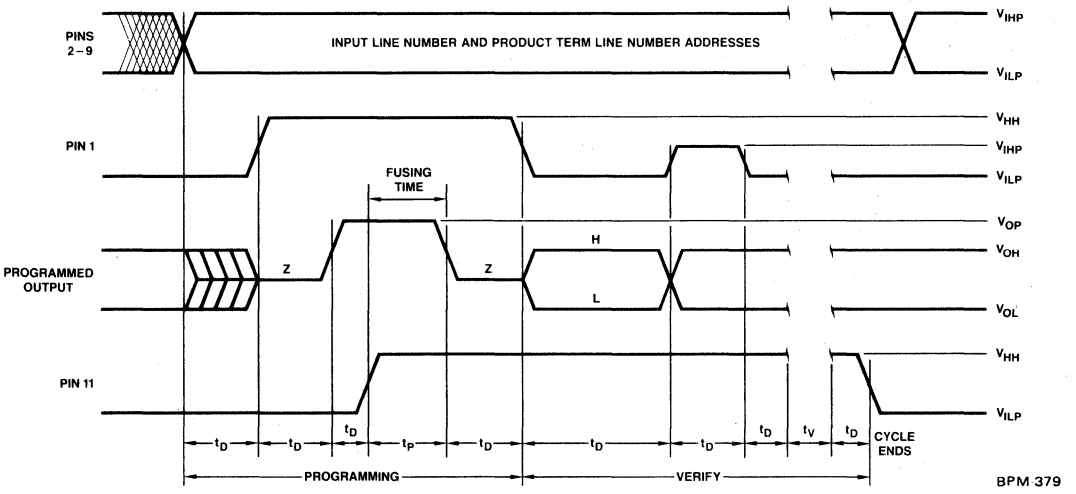


TABLE 1. INPUT ADDRESSING

Input Line Number	Input Line Number Address Pin States				
	9	8	7	6	5
0	L	L	L	L	L
1	L	L	L	L	H
2	L	L	L	H	L
3	L	L	L	H	H
4	L	L	H	L	L
5	L	L	H	L	H
6	L	L	H	H	L
7	L	L	H	H	H
8	L	H	L	L	L
9	L	H	L	L	H
10	L	H	L	H	L
11	L	H	L	H	H
12	L	H	H	L	L
13	L	H	H	L	H
14	L	H	H	H	L
15	L	H	H	H	H
16	H	L	L	L	L
17	H	L	L	L	H
18	H	L	L	H	L
19	H	L	L	H	H
20	H	L	H	L	L
21	H	L	H	L	H
22	H	L	H	H	L
23	H	L	H	H	H
24	H	H	L	L	L
25	H	H	L	L	H
26	H	H	L	H	L
27	H	H	L	H	H
28	H	H	H	L	L
29	H	H	H	L	H
30	H	H	H	H	L
31	H	H	H	H	H

L = V_{ILP}
H = V_{IHP}

SIMPLIFIED PROGRAMMING DIAGRAM

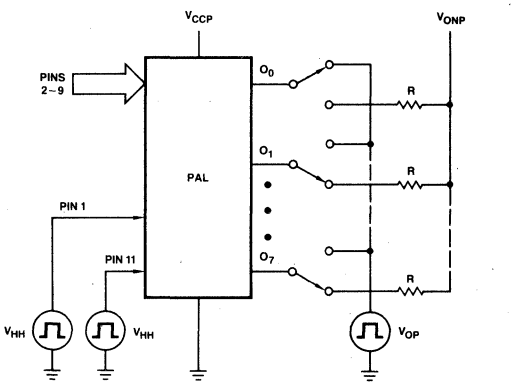


TABLE 2. PRODUCT TERM ADDRESSING

Product Term Line Number								Product Term Select Address Pin		
								4	3	2
0	8	16	24	32	40	48	56	L	L	L
1	9	17	25	33	41	49	57	L	L	H
2	10	18	26	34	42	50	58	L	H	L
3	11	19	27	35	43	51	59	L	H	H
4	12	20	28	36	44	52	60	H	L	L
5	13	21	29	37	45	53	61	H	L	H
6	14	22	30	38	46	54	62	H	H	L
7	15	23	31	39	47	55	63	H	H	H
Pin 19	Pin 18	Pin 17	Pin 16	Pin 15	Pin 14	Pin 13	Pin 12			
Programming Access and Verify Pin										

L = V_{ILP}
H = V_{IHP}

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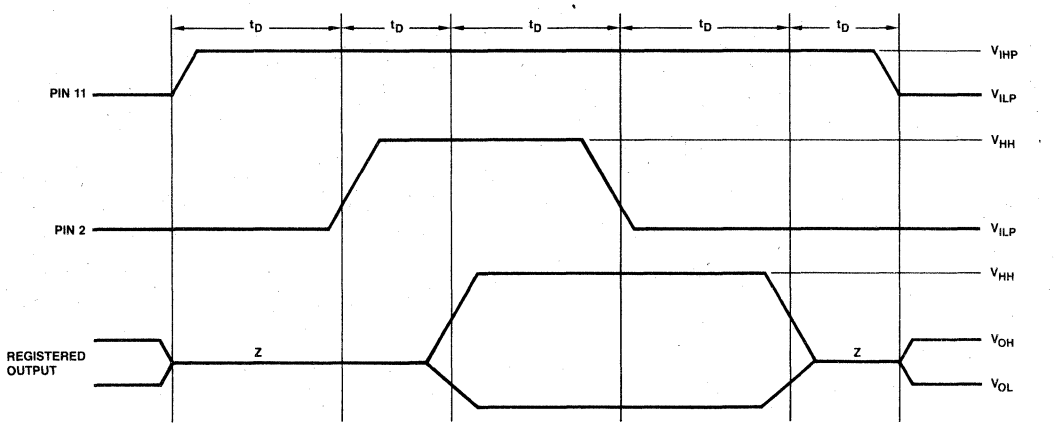
PRELOAD OF REGISTERED OUTPUTS

AMD PAL registered outputs are designed with extra circuitry to allow loading each register asynchronously to either a HIGH or LOW state. This feature simplifies testing since any initial state for the registers can be set to optimize test sequencing.

The pin levels and timing necessary to perform the PRELOAD function are detailed below:



Level forced on registered output pin during preload cycle	Output state at the output pin after cycle
V_{HH}	HIGH
0V to V_{CCH} or OPEN	LOW

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ORDERING INFORMATION

AmPAL XXXXX X X X X

Basic Device
16R8
16R6
16R4
16L8
16H8
16LD8
16HD8

Speed Selection
= Standard
A = High Speed

Screening
C = 883C Basic Flow
B = 883B (Burn-in)

Temperature Range
C = Commercial
M = Military

Package
P = Molded DIP (Commercial Only)
D = Hermetic DIP
L = Chip-Pak™*

*Chip-Paks are rated at maximum case temperature only.

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

MOS Microprocessor

Family Selector Guide

	8086/88	8085A	8085A-2	8080A	Z8001/2†	Z8001/2-A
Clock Period	200ns	320ns	200ns	480ns	250ns	165ns
Clock Generator	8284A	On-Chip	On-Chip	8224	8127	8127
Arithmetic Processing Unit	8087	9511A-1 9512-1	9511A-4 9512-1	9511A 9512	9511A-4 9512-1	9511A-4 9512-1
Interrupt Controller	8259A-5	9519A 8259A	9519A-4 8259A-5	9519A 8259A	9519A-1	9519A-1
DMA Controller	8089 9516A 9517A-5	9517A-4	9517A-5	9517A	8016 9517A-4	8016A
Dynamic Memory Controller	2964B	2964B	2964B	2964B	2964B	2964B
Serial I/O	8251A 8530A 8030A	8251A 8530	8251A 8530A	8251A	8030	8030A
Parallel I/O	8255A-5 8036A	8255A-5	8255A-5	8255A	8036	8036A
Counter Timer I/O	9513 8036A 8073	9513 8253-5	9513 8253-5	9513 8253	8073	8073
FIFO I/O	8038	8038	8038	8038	8038	8038
Data Ciphering Processor	8068	8068	8068	9518	8068	8068
Error Detection and Correction	2960	2960	2960	2960	2960	2960
Burst Error Processor	8065 9520	8065 9520	8065 9520	8065 9520	8065 9520	8065 9520
CRT Controller	8275 8052	8275	8275	8275	8052	8052A
I/O Processor	8089	N/A	N/A	N/A	N/A	N/A
RAM I/O	N/A	8155/6	8155/6-2	N/A	N/A	N/A
Memory Management Unit	N/A	N/A	N/A	N/A	8010	8010A
Bus Control/ Arbiter	8288 8289	N/A	N/A	N/A	N/A	N/A
Bus Latches	29841-6	29841-6	29841-6	29841-6	29841-6	29841-6
Bus Buffers	29827/28	29827/28	29827/28	29827/28	29827/28	29827/28
Bus Transceivers	29861-4	29861-4	29861-4	29861-4	29861-4	29861-4
EDC Buffers	2961/2	2961/2	2961/2	2961/2	2961/2	2961/2
RAM Drivers	2965/6	2965/6	2965/6	2965/6	2965/6	2965/6

†Z8000 is a trademark of Zilog, Inc.

Microprocessor

Microprocessor CPUs	**8001**	16-Bit CPU
	8002	16-Bit CPU
	8086	16-Bit CPU
	8080A	8-Bit CPU
	8085A,H	8-Bit CPU
	8088	8-Bit CPU*
Single-Chip Microcomputers	**8051/31**	8-Bit Microcomputer**
	8049/39	8-Bit Microcomputer
	8048/35	8-Bit Microcomputer
	8041A	Universal Peripheral Interface
Am9500 Advanced System Components	**9511A**	Arithmetic Processor
	9512	Arithmetic Processor
	9513	System Timing Controller
	9517A	DMA Controller
	9518	Data Ciphering Processor
	9519A	Universal Interrupt Controller
	9520	Burst Error Processor
	9521	32-, 35-Bit Burst Error Processor
8086/88/85/80 Family System Components	**8087**	Arithmetic Processor**
	8089	I/O Processor**
	8155,H	RAM with I/O Ports
	8156,H	RAM with I/O Ports
	8212	Octal I/O Port
	8216/26	Quad Bus Driver
	8224	Clock Generator for 8080A
	8228/38	Bus Driver for 8080A
	8231A	Arithmetic Processor
	8232	Arithmetic Processor
	8237A	DMA Controller
	8251A	Serial I/O USART*
	8253	Counter/Timer
	8255A	Programmable Peripheral Interface
	8259A	Interrupt Controller*
	8275	CRT Controller*
	8279	Keyboard/Display Interface
	8284A	Clock Generator**
	8286	Octal Transceiver
	8287	Octal Transceiver
	8288	Bus Controller**
	8289	Bus Arbiter**
	9516	Data Transfer Controller*
	8530	Serial Communications Controller*
	8036	Counter/Timer I/O
	8038	FIFO I/O Interface*

Components

Z8001/2 Family System Components	**8010**	Memory Management Unit*
	8016	Data Transfer Controller
	8030	Serial Communication Controller*
	8036	Counter I/O
	8038	FIFO I/O Interface
	8052	CRT Controller**
	8060	FIFO Buffer/FIO Expander*
	8065	Burst Error Processor
	8068	Data Ciphering Processor
	8073	System Timing Controller
	29861-4	High Performance Bus Transceivers*
	8121	Octal Comparator
	8127	Clock Generator and Controller
	29827/28	High Performance Bus Buffers*
	8163	Refresh and EDC Controller (16 MHz)
	8167	Refresh and EDC Controller (22 MHz)
	29821-6	High Performance Bus Registers
	29841-6	High Performance Bus Latches*
Bipolar Support Circuits	**25LS244**	Octal Buffer
	25LS2521	Octal Comparator
	25LS2536	Octal Address Decoder
	25LS2548	Octal Decoder with ACK
	29821-6	High Performance Bus Registers
	2925	Clock Generator
	29861-4	High Performance Bus Transceiver*
	2948/49	Octal Bus Transceiver
	2960	16-Bit Error Detection and Correction
	2961/62	EDC Buffers
	2964B	Dynamic Memory Controller
	2965/66	RAM Drivers
	29841-6	High Performance Bus Latches*

*Q3-4 '82 Introduction
**1983 Introduction

Analog Data Acquisition Product Guide and Cross Reference

DIGITAL-TO-ANALOG CONVERTERS

GENERAL PURPOSE 8-BIT

DAC-08	Industry Standard 8-Bit Multiplying D/A
Am1508/1408	Multiplying D/A
SSS1508A/1408A	Multiplying D/A

MICROPROCESSOR COMPATIBLE 8-BIT

Am6080	Contains 8-Bit Data Latch with Write, Chip Select and Data Enable Logic On-Chip
Am6081	Same as Am6080 Plus On-Chip Multiplexer

GENERAL PURPOSE 12-BIT

Am6012	Low Cost, 250ns Settling Time, Multiplying 12-Bit D/A
Am6022*	High-Speed Version of Am6012, 75ns Settling Time

MICROPROCESSOR COMPATIBLE 12-BIT

Am6082*	Contains Reference, Double Buffered Latch, Control Logic and High-Speed Op Amp. 150ns Current or 400ns Voltage Settling Time

GENERAL PURPOSE 14-BIT

Am6014*	14-Bit Plus Sign Multiplying D/A, 500ns Settling Time

COMPANDING

Am6070	8-Bit, 72dB of Dynamic Range for Control Systems
Am6072	8-Bit μ-Law for PCM Communication Systems

ANALOG-TO-DIGITAL CONVERTERS

HIGH-SPEED 4-BIT

Am6688	100MHz Sampling Rate, 8-Bit Accuracy, Flash Converter

HIGH-SPEED 6-BIT

Am6606*	100MHz Sampling Rate, 8-Bit Accuracy, Flash Converter

HIGH-SPEED MICROPROCESSOR COMPATIBLE 8-BIT

Am6108/6148**	1μs Conversion Time, Contains Reference, DAC, Comparator, SAR, Scale Resistors, 3-State Buffers and Control Logic

HIGH-SPEED MICROPROCESSOR COMPATIBLE 12-BIT

Am6112	3μs Conversion Time, Contains Reference, DAC, Comparator, SAR, Scale Resistors, 3-State Buffers and Control Logic

SAMPLE AND HOLD AMPLIFIERS

GENERAL PURPOSE

LF198/398	Less than 10μs Acquisition Time, Industry Standard Sample and Hold

HIGH-SPEED

Am6420*	500ns Acquisition Time, 10ns Aperture Delay, 0.01% Linearity Error

*In development.

**Am6148 is the slim 24-pin, 0.3" version of the Am6108.

VOLTAGE COMPARATORS

Am685	5ns Propagation Delay, ECL Output
Am686	12ns Propagation Delay, TTL Output
Am687	8ns Propagation Delay, Dual 685, ECL Output
Am1500/LH2111	Dual Precision
LM111/311	High Accuracy, Low Cost
LM119	Dual High Speed, ±5V to ±15V Supply
LM139	Quad, Low Power, High Accuracy

OPERATIONAL AMPLIFIERS

LF155/156	FET-Input, High Slew Rate and Fast Settling Time
LM108	Low Power, ±2V to ±20V Supply
LM118	High Speed, 15MHz Bandwidth
LM148	Quad, Low Power 741

CROSS REFERENCE

AMD	National	Fairchild	Signetics	PMI	Motorola	Raytheon	Analog Devices
DAC-08AQ	DAC0800LAJ	μA0801ADM	SE5009F	DAC-08AQ	DAC-08AQ	DAC-08ADM	ADDAC-08AD
DAC-08HQ	DAC0802LCJ	μA0801HDC	NE5009F	DAC-08HQ	DAC-08HQ	DAC-08HDM	ADDAC-08HD
DAC-08HN	DAC0802LCN	μA0801HPC	NE5009N	DAC-08HP	DAC-08HP	DAC-08HBM	–
DAC-08Q	DAC0800LJ	μA0801DM	SE5008F	DAC-08Q	DAC-08Q	DAC-08DM	ADDAC-08D
DAC-08EQ	DAC0800LCJ	μA0801EDC	NE5008F	DAC-08EQ	DAC-08EQ	DAC-08EDM	ADDAC-08ED
DAC-08EN	DAC0800LCN	μA0801EPC	NE5008N	DAC-08EP	DAC-08EP	DAC-08EBM	–
DAC-08CQ	DAC0801LCJ	μA0801CDC	NE5007F	DAC-08CQ	DAC-08CQ	DAC-08CDM	ADDAC-08CD
DAC-08CN	DAC0801LCN	μA0801CPC	NE5007N	DAC-08CP	DAC-08CP	DAC-08CBM	–
AM1508L8	DAC0808LJ	μA0802DM	MC1508-8F	–	MC1508L8	–	AD1508-8D
AM1408L8	DAC0808LCJ	μA0802ADC	MC1408-8F	–	MC1408L8	–	AD1408-8D
AM1408N8	DAC0808LCN	μA0802APC	MC1408-8N	–	MC1408P8	–	–
AM1408L7	DAC0807LCJ	μA0802BDC	MC1408-7F	–	MC1408L7	–	AD1408-7D
AM1408N7	DAC0807LCN	μA0802BPC	MC1408-7N	–	MC1408P7	–	–
AM1408L6	DAC0806LCJ	μA0802CDC	MC1408-6F	–	MC1408L8	–	–
AM1408N6	DAC0806LCN	μA0802CPC	MC1408-6N	–	MC1408P6	–	–
SSS1508A-8Q	–	–	–	SSS1508A-8Q	–	–	–
SSS1408A-8Q	–	–	–	SSS1408A-8Q	–	–	–
SSS1408A-7Q	–	–	–	SSS1408A-7Q	–	–	–
SSS1408A-6Q	–	–	–	SSS1408A-6Q	–	–	–
AM6012ADM	–	–	–	–	–	–	–
AM6012ADC	–	–	–	–	–	–	–
AM6012APC	–	–	–	–	–	–	–
AM6012DM	–	–	–	DAC312BR	–	–	–
AM6012DC	–	–	–	DAC312FR	–	–	–
AM6012PC	–	–	–	–	–	–	–
AM6070ADM	–	–	–	DAC-76BX	–	–	–
AM6070ADC	–	–	–	DAC-76EX	–	–	–
AM6070DM	–	–	–	DAC-76X	–	–	–
AM6070DC	–	–	–	DAC-76CX	–	–	–
AM6072DM	–	–	–	–	–	–	–
AM6072DC	–	–	–	DAC-86EX	–	–	–
AM6080	DAC0830/1/2†	–	NE5018/19†	DAC-808/888†	–	–	AD558†
AM6081	–	–	–	–	–	–	–
AM6688	–	–	–	–	MC6108	–	–
AM6108	ADC0820†	–	–	–	–	–	AD570† AND AD7574†
AM6148	ADC0820†	–	–	–	–	–	
LF198	LF198	μAF198	NE5537	–	–	–	–

†Functional equivalent only

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General Information Index

Guidelines on Testing Am2900 Family Devices

I. INTRODUCTION

The Am2900 Family represents a major step forward in bipolar technology, in that each device contains a number of MSI-type functions interconnected on one chip. The gate counts in the parts comprising the Am2900 Family are around 10 – 100 times the gate count of MSI functions. While this produces a number of advantages for manufacturing, such as reduced component count and lower costs, it complicates the incoming-inspection problem because test programs tend to be long and complex and must be carefully designed to insure that *all bad parts are rejected* and *most good parts are accepted.* While stating these two criteria is simple, reducing them to practice is not. LSI devices are not as "forgiving" of simplifications in test patterns and assumptions about forcing functions and noise levels, as their simpler counterparts. These notes are intended to point out some common areas of difficulty and their solutions.

II. THE PURPOSE OF TESTING

Testing is performed at most facilities during an inspection of purchased material. The reason, of course, is that it is much less expensive to screen parts then, than it is to troubleshoot and repair completed boards. Ideally, all the parts passed by incoming inspection will work in the system. This is insured through a specification which defines the way the part must behave in the system, and the incoming test should confirm that devices received meet the specification. The incoming test should not reject devices which meet the specification. When test programs are too tight or test for conditions not contained in the specification, delays in shipments occur and significant costs are incurred by both the vendor and the buyer trying to resolve "correlation problems."

III. GUARANTEEING THAT THE PARTS WORK

One step in testing devices is to perform DC parametric tests: I_{CC}, V_{OH}, V_{OL} and the like. These tests on bipolar LSI are not really different from those performed on simpler TTL devices, except that the number of pins involved is greater, and more complex set-ups may be required to put outputs in the proper state for testing. Another step is functional testing, and for bipolar LSI, function tests are significantly different than for MSI. The function tests must first insure that the device is capable of working, i.e., it's hooked up correctly inside. These kinds of tests can be described as "stuck-at-one, stuck-at-zero" tests, because they are designed to exercise each gate in the part. Even for a part as complex as the Am2901, the "stuck-at" tests can be performed quickly. Less than 400 test patterns must be applied to the part to exercise every gate.

But, "stuck-at" tests make an assumption: if a gate works, then it works regardless of the state of other gates in the circuit. Each gate is treated independently, but, in the integrated circuit, no gate is an island. The performance of one gate can, in fact, depend on the states of surrounding gates, because they share common inputs or common ground lines.

These possible faults are often not tested by "stuck-at" tests, because they are not independent of the state of surrounding logic. These potential faults depend on the physical and logical construction of the circuit. They are usually called "pattern sensitivities." Pattern-sensitive faults, like the two described above, are not something new. All digital products exhibit pattern sensitivities – even SSI. But, on simpler parts, either traditional "stuck-at" tests happen to find most of them, or the parts are easy enough to test that all possible data patterns are generated during testing. Neither of these circumstances is true for bipolar LSI. A special effort must be made to apply many data patterns to the devices to check for pattern-sensitive faults. This has been done for years with RAM patterns such as GALPAT. It must now be done with logic functions as well.

In the devices in the Am2900 Family, as with RAMs, testing all possible data patterns is not practical, but, the various MSI kinds of functions in the devices (register, ALU, multiplexer, etc.) can generally be logically isolated, and each of those functions should be checked independently for all possible data patterns. This principle works because (1) as a rule, it is possible to control the MSI functions in a 2900 part with some degree of independence, and (2) the MSI functions are usually physically separated on the die, so that a data pattern within one MSI block will not exhibit pattern sensitivity dependent on the data in another MSI block.

In the Am2901, for example, ALU tests using the two RAM ports as data sources are unlikely to be affected by the state of the data inputs or the Q register. The shift multiplexer at the input of the RAM is unlikely to be affected by the Q register or the ALU source-select multiplexers. The control logic for the ALU source multiplexers should not be affected by anything in the ALU. By applying these kinds of principles intelligently function tests can be constrained to a few thousand tests which provide a very high confidence level that the part is not subject to pattern-sensitive faults within its operating range.

As an example of the test philosophy used on these parts, the function tests for the Am2901 are described below.

Am2901 FUNCTION TEST DESCRIPTION

The following describes the function tests performed on the Am2901. The $\overline{OE}$ pin is low during the entire function tests and each test gets one clock pulse.

A-Port Galpat via ALU

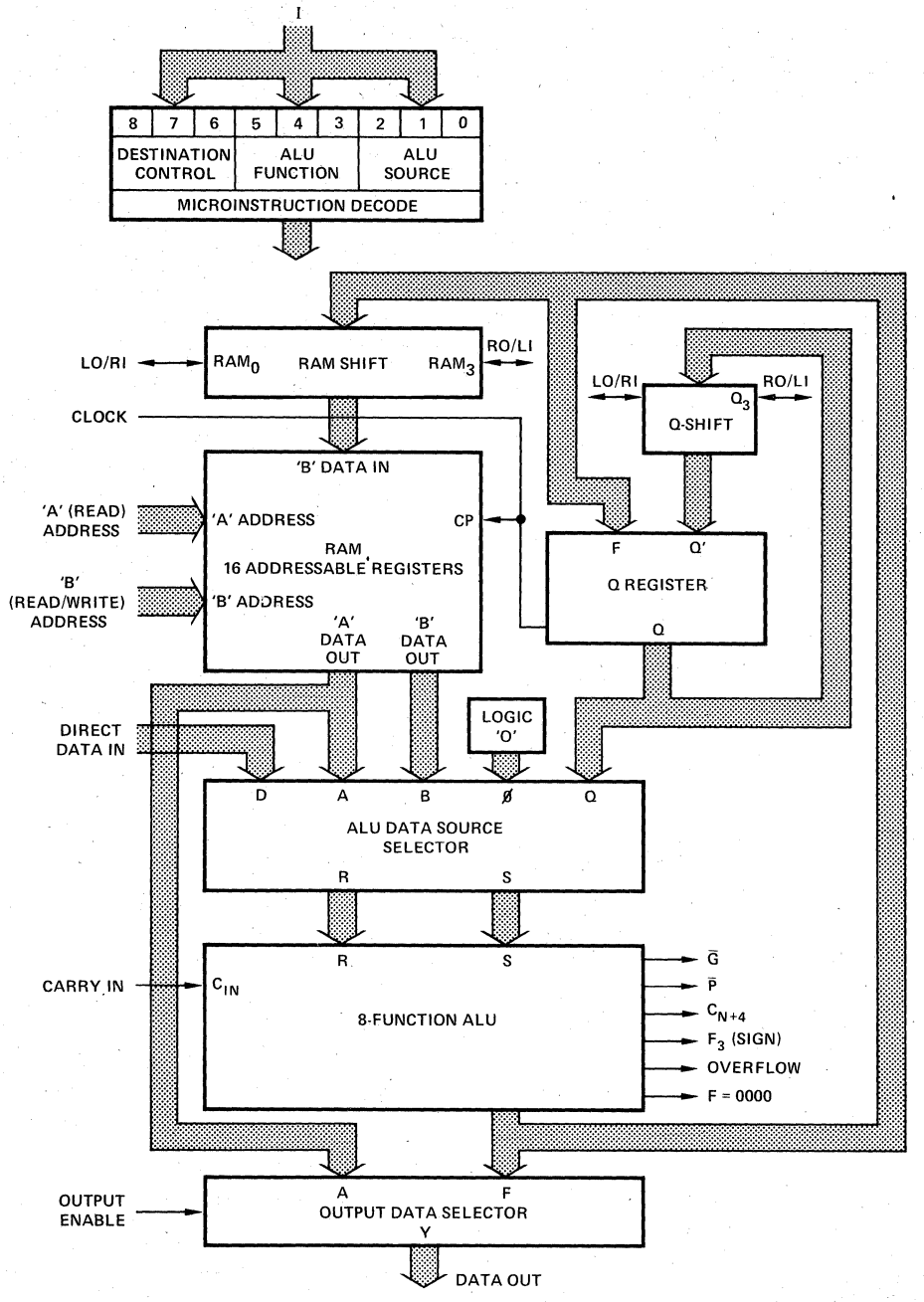
These are tests in which the A-address of the 2-port RAM is tested for Galloping "ones" in a field of "zeros." During these tests, the B-address is the same as the A-address and OP code 337 is used for a write operation, while OP code 134 is used for a write operation, while OP code 134 is used for a read operation. The four shift-operation pins, Q_0, Q_3, RAM_0 and RAM_3, are ignored.

B-Port Galpat via ALU

These are tests in which the B-address of the 2-port RAM is tested for Galloping "ones" in a field of "zeros." During these tests, the A-address is the inverse of the B-address and OP code 337 is used for a write operation while OP code 133 is used for a read operation. The four shift-operation pins, Q_0, Q_3, RAM_0 and RAM_3, are ignored.

A-Port Galpat Bypass ALU

These are tests in which the A-address of the 2-port RAM is tested for Galloping "ones" in a field of "zeros." During these tests, the B-address is the inverse of the A-address and OP code



THE Am2901 4-BIT MICROPROCESSOR SLICE

337 is used for a write operation while OP code 233 is used for a read operation. The four shift-operation pins, Q_0, Q_3, RAM_0 and RAM_3, are ignored.

Repeat 1 above by inverting the Data and Y output information on D_{3-0} and Y_{3-0}. All other outputs are ignored. This performs Galloping "zeros" in a field of "ones" for the A-Port via ALU.

Repeat Item 2 above by inverting the Data and Y output information on D_{3-0} and Y_{3-0}. All other outputs are ignored. This performs Galloping "zeros" in a field of "ones" for the A-Port via ALU.

Repeat Item 3 above by inverting Data and Y output information on D_{3-0} and Y_{3-0}. All the other outputs are ignored. This is Galloping "zeros" in a field of "ones" for A-Port bypass ALU.

ALU Source Code

During these tests, the A and B-addresses are at word locations preloaded with known values. The Q register is also preloaded. Then, with the ALU destination OP code = 1 (No-OP) and the ALU function code = 6 (exclusive OR), the source code is cycled through from 0-7. The function code is then modified to 7 (exclusive NOR) and the source code sequence is cycled through once more.

ALU Function Code

During these tests, the memory is preloaded with content equal to the address. In other words, word 0 is loaded with 0, word 1 with 1, and so on. Then, with A-address = B-address, a destination OP code of 1 (No OP), and a source OP code of 1 (A&B Port selected), the ALU function code is cycled through the sequence of 7, 5, 4, 0, 1, 3, 2, 6 for every set of A&B address. This whole sequence is then repeated with A-address equal to the inverse of the B-address.

Arithmetic Operation & Carry Generation

During these tests, the memory is preloaded with content address. With OP code 105, whereby D input is added to the A-Port of the memory, the tester cycles through every possible D input added to every word in memory with carry in being both one and zero.

Q Register Operation

During these tests, the Q register is first loaded with all zeros. Then, with Cn = 0 and with OP code 006, whereby Q register is loaded with the sum of data input and Q-register content on every clock cycle, the device is clocked through all possible data inputs. The Cn input is then changed to a ONE, and with OP code 016 whereby Q register is loaded with the difference of Q-D. The device is clocked through all possible data input again. This checks both the add and subtract modes of the ALU, the internal-carry-lookahead circuitry and the Q-register operation.

Q Register Shifting

During these tests, a unique string of data (11100001 010011011110) is shifted into the appropriate shift inputs. OP codes used in this group of tests are 432 for shift left, 532 for no shift, 632 for shift right and 732 for no shift.

RAM Shifting

During these tests, A and B-address are at word 0. A string of data (11100001010011011110) is shifted into the appropriate shift inputs. OP codes used are 434 and 533 for left shift, 634 and 733 for right shift.

IV. AVOIDING THE REJECTION OF GOOD DEVICES

Discrepancies in testing results between the vendor and the buyer result in much irritation and substantial costs for both. Some of the common sources of these discrepancies are discussed below.

Testing for Unspecified or "don't care" Conditions

The data sheet (or purchase specification) defines the characteristics of the part. It is hard enough to test for everything specified without adding additional tests for unspecified parameters. If the state of an output is not specified under certain conditions, then it should not be tested.

Noise

Many testing problems result from noise produced by the interactions of the device being tested and the test system. Typical test fixtures have lead inductances several times that of a PC board socket. This inductance, especially in the device ground path, is the source of these problems.

When the inputs to the device are changed there is a sequence of rapid changes in the devices ground currently as signals propagate through internal gates to the outputs. These appear as changes in the voltage drop across the device ground lead. This voltage drop can be as much as 2 volts across a few inches of wire. Rise times are on the order of 1nsec and pulse widths range from 2 to 10nsec. Output tranisient current during switching may be 50 to 100mA. The test systems input and output reference voltages are set with respect to tester ground and are not effected by these transients. Consequently the effective input voltages to the device will vary. If the ground pin goes up 1 volt, all the inputs effectively go down 1 volt.

This must be considered in selecting levels for V_{IL} and V_{IH}. The device data sheet says V_{IL} must be less than 0.8V and V_{IH} more than 2.0V. But this is as measured at the device package pins, between input and ground. This means that if the ground varies ± 0.5 volt the input levels must be $V_{IL} \leq 0.3V$ and $V_{IH} \leq 2.5V$. If this is not done, a noise pulse could, for example, make the clock input effectively go high in the middle of the clock low time, causing an extra clock pulse. A similar situation exists at the device outputs, requiring V_{OL} to be set higher, and V_{OH} lower, than the data sheet numbers. AMD uses $V_{IL} = OV$, $V_{IH} = 3V$, $V_{OL} = 1V$, $V_{OH} = 2V$ for functional tests.

Proper observations are important to the understanding and control of these problems. Small changes in timing, bypass capacitors, etc will have large effects on the noise. An oscilloscope of 200 MHz or greater bandwidth is essential. Noise voltage should be measured at the device ground pin (at the device package edge, not the bottom of the test socket). Connect the probe ground to the tester chassis. In order to see the peak noise voltage, cycle the tester through a long pattern. Trigger the scope internally from the noise waveform. Turn the trigger level slowly up until the trace is almost lost. The peak noise voltage will appear at the left side of the screen. Sweep speed should be about 10nsec/div. Repeat for the peak of the opposite polarity.

Another useful technique is to identify a particular test pattern location which causes significant noise. Sync the oscilloscope to this test cycle. Using a two channel scope, connect one channel to an input pin and the other channel to the device ground pin. Invert the channel on the ground pin and add the two channels. The waveform will show the effective input levels.

An additional problem is introduced by I/O pins. When output load circuits are connected to these pins the tester must drive the load and the device when the pins are inputs. If the tester has a driver impedance of 50ohms and the load supplies 16mA into V_{OL}, the input level produced will be 0.8V too high. This must be compensated by further reducing the programmed V_{IL} for only the I/O pins. Some devices are sensitive to input voltages below ground.

If the tester does not provide suitable alternate driver supplies, it may be necessary to provide resistor pullups for input-only pins.

The same ground lead inductance problems causes difficulties in DC testing. Many DC tests require some functional sequence to produce the correct device state. The input levels must be such to avoid false clocks, etc. DC tests may be used to verify input threshold levels. To do this, an output test such as V_{OL} or V_{OH} is selected where the outputs combinatorally depend on the inputs. Using non-threshold levels the appropriate input conditions are applied. The input levels are then reprogrammed to threshold levels. The outputs are then measured for V_{OL} or V_{OH}. It is not possible to do the functional set-up with threshold levels, even if it is only a single line, as oscillations may occur. Switching between alternate driven supplies also may generate sufficient noise to cause problems.

AC Testing

Many modern testers allow switching tests to be performed during the application of complex test sequences. The switching and function tests can then occur together. Unfortunately, this blurs the distinction between functional failure and switching-speed failure when a device is rejected, so, it is a good idea to do some preliminary function testing with "loose" AC limits before trying to do everything at once. When function and AC testing are combined, it is important to consider the *driving conditions* under which the AC parameters are tested. Switching measurements on Bipolar ICs are usually made with input levels switching between 0V and 3.0V (sometimes 0.4V and 2.4V are used). The output transition is measured at 1.5V (sometimes at 1.3V).

They are never specified at threshold levels (0.8V and 2.0V) because of noise problems.

Realistic AC tests require sequencing through many lines of test pattern to include a variety of data paterns. Unfortunately the AC accuracy of most modern logic testers is not as good as memory testers. There are often significant differences between different waveform formats. The position of an edge may depend on whether adjacent pins are switching and whether they are going up or down. This limits the accuracy of testing, especially for such parameters as hold times, where tester error usually exceeds the difference between device typical and data sheet maximum. This may be observed on an oscilloscope by cycling the tester and synchronizing the scope to a repetitive pulse, such as the device clock pin.* Do not trigger the scope on any particular tester cycle. Observing a device input on the second scope channel will show many overlapping transitions, positive and negative. The width of this band must be added to other error sources to determine tester accuracy.

Temperature Testing

Integrated circuits are specified to operate over either the commercial range of 0° to +70°C or the military range of −55°C to +125°C. Standard screening procedures (from MIL-STD-883) call for 100% testing at 25°C followed by sample testing at the high and low temperature. Many users duplicate this test sequence in their incoming inspection, and some test 100% at temperature.

Testing problems are rarely encountered at low temperatures, if care is taken to prevent ice formation on the test socket. At high temperature, difficulties may arise because of the difficulty in creating a test environment which is representative of the thermal conditions found in the system.

High temperature testing with a controlled ambient temperature is very difficult because the thermal coefficient between the package and the surrounding environment depends on humidity, rate of air flow, package color, connections to package pins, and position of surrounding devices. For testing purposes, only the case temperature can really be controlled. (Most systems' thermal engineering is also designed to control case temperatures.)

V. INCOMING INSPECTION AND TESTING SUPPORT PRODUCTS

AMD provides several products to assist in the development of incoming inspection testing for most Am2900 LSI devices. See the table on the following page for specifics by device.

Sentry Test Programs

These are complete data sheet function, DC and AC parameter programs. They run on a Fairchild Sentry VII with low voltage test heads, 4K local memory and SPM. Complete load board documentation is included. Programs are supplied on magnetic tape in TDX format. Source files in ASCII code on magnetic tape can be provided for those who wish to generate test programs for other testers. *Test programs require a licensing agreement.*

Correlation Kit

This consists of two devices and datalog from AMD's characterization program.

*Use a sweep speed of 1nsec/div.

ORDERING INFORMATION

Order Code	Description
AM29XX – SEN	Sentry Test Program
AM29XX – KIT	Correlation Kit

Test Aids for Am2900 Devices

AMD provides Sentry Test Tapes with Loadboard Documentation and Correlation Kits to assist in the development of incoming inspection for most Am2900 LSI/VLSI devices. These test aids may be ordered directly from Advanced Micro Devices, although Sentry test tapes require a pre-signed license agreement. For further ordering information contact your local AMD Sales Office or Sales Representative.

Current status of test aids by device is given below. For more information on testing Am2900 LSI/VLSI, see the note in this section: "Guidelines on Testing Am2900 Family Devices."

Part Number	Sentry Test Program (Am29XXX – SEN) (Note 1)	Correlation Kit (Am29XXX – KIT) (Note 2)
AM2901B	√	√
AM2901C	√	√
AM2903	√	√
AM2903A	Mid-1983	Mid-1983
AM2904	√	√
AM2909A	√	√
AM2910	√	√
AM2910A	Planned	Planned
AM2911A	√	√
AM2914	√	√
AM2925	Mid-1983	Mid-1983
AM2930	√	√
AM2932	Fall/1983	Fall/1983
AM2940	√	√
AM2942	√	√
AM2950	√	√
AM2950A	Planned	Planned
AM2951	√	√
AM2951A	Planned	Planned
AM2952	√	√
AM2952A	Planned	Planned
AM2953	√	√
AM2953A	Planned	Planned
AM2960	√	√
AM2960A	Planned	Planned

Part Number	Sentry Test Program (Am29XXX – SEN) (Note 1)	Correlation Kit (Am29XXX – KIT) (Note 2)
AM2964B	Mid-1983	Mid-1983
AM2968	Planned	Planned
AM2969	Planned	Planned
AM2970	Planned	Planned
AM29112	Planned	Planned
AM29116	√	√
AM29116A	Planned	Planned
AM29118	Planned	Planned
AM29203	Mid-1983	Mid-1983
AM29501	Planned	Planned
AM29510	Planned	Planned
AM29516	Mid-1983	Mid-1983
AM29516A	Planned	Planned
AM29517	Mid-1983	Mid-1983
AM29517A	Planned	Planned
AM29520	Mid-1983	Mid-1983
AM29521	Mid-1983	Mid-1983
AM29526	Planned	Planned
AM29527	Planned	Planned
AM29528	Planned	Planned
AM29529	Planned	Planned
AM29540	Planned	Planned
AM29705	√	√
AM29705A	Mid-1983	Mid-1983
AM29707	Mid-1983	Mid-1983

Notes: 1. Sentry Test Programs – these are complete data sheet function, DC and AC parameter programs. They run on a Fairchild Sentry VII with low voltage test heads, 4K local memory and SPM. Complete load board documentation is included. Programs are supplied on magnetic tape in TDX format. Source files in ASCII code on magnetic tape can be provided for those who wish to generate test programs for other testers. *Test programs require a licensing agreement.*

2. Correlation Kit – consists of two devices and datalog from AMD's characterization program.

IMOX™ Reliability Report

Advanced Micro Devices

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INTRODUCTION

This report is a comprehensive summary of reliability test data accumulated on AMD's IMOX process. IMOX is an acronym for ion-IMplanted/micro-OXide isolation. AMD presently uses this wafer fabrication process on all new Bipolar products, including Bipolar Memory, Interface, Logic and Microprocessor devices. We present not only the statistical data, but also discuss the process itself, typical failure mechanisms, and the test methodology behind the data. The results show experimental and statistical proof that the AMD IMOX process ensures system designers of long life and highly reliable Bipolar devices.

In line with Advanced Micro Devices' commitment to provide customers with high quality, high performance devices, we will continue to evaluate devices for reliability through ongoing HTOL (high temperature operating life) testing. This report will be updated at regular intervals as new reliability data is accumulated.

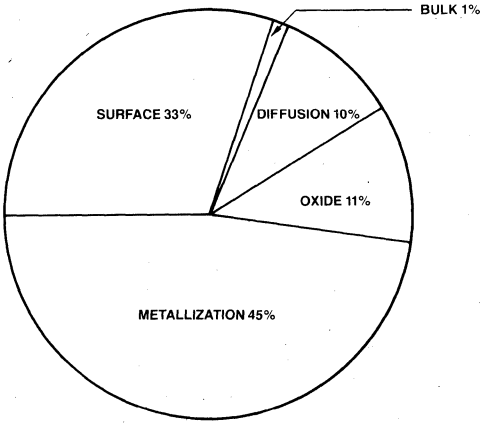
PROCESS

The IMOX process utilizes ion-implanted transistors, oxide isolation and dual-layer metal to create fast, high performance Bipolar devices that consume less power as well.

IMOX processing allows for reduction of transistor geometries and the amount of unused space surrounding a transistor, which means that individual transistors can be built significantly smaller and closer together. Since decreased geometries are obtained without a reduction in photolithographic line width, no increase in the process sensitivity occurs. Speed is one of the most vital characteristics of a Bipolar device. With the tighter layout and reduced capacitances of IMOX processing, we have improved the speed on many devices by as much as 25–30%. Tighter layouts have also allowed us to utilize previously unavailable die space for increased complexity. This is represented in two new AMD Bipolar VLSI devices, the Bipolar Microprocessor, Am29116 and the 16 x 16 Parallel Multiplier, Am29517.

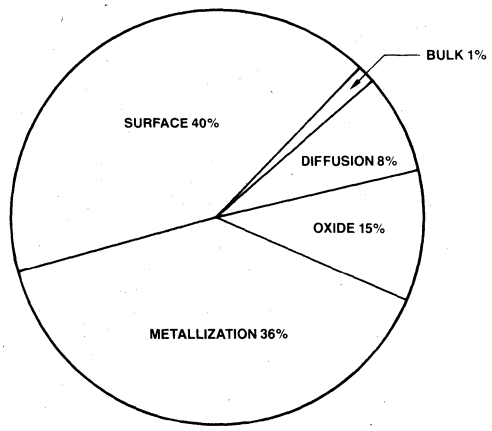
FAILURE MECHANISMS

Failures in integrated circuits are frequently categorized by the phase of manufacturing or the component of the part's structure that is associated with the determined failure mechanism. Failure distributions often are presented as pie charts with slices of the pie named for these categories (see Figures 1 and 2). The failure category distribution percentages are roughly those expected for Bipolar IMOX devices. Each of these categories may contain several distinct failure mechanisms – the basic physical or chemical process that results in a failure. The external indicators of a failure (the failure mode) are generally electrical in nature: opens, shorts, non-functional or parametric anomalies. There may be different mechanisms indicated by a single failure mode. The following is a discussion of the commonly observed failure mechanisms in integrated circuits.



Key: Failure type distribution for STTL/LSI Integrated Circuits (data derived from Reliability Analysis Center study, "Microcircuit Screening Effectiveness," 1978-Order No. TRS-1, 78). Data based on field failure information available to RAC, not life test data.

Figure 1. Normalized Distributions of STTL/LSI Malfunctions



Key: Failure percentages are averages based on past failure analysis studies performed by engineers at AMD.

Figure 2. AMD Observed Distributions of STTL/LSI Malfunctions

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DIFFUSION

Diffusion related mechanisms generally cause marginal device parameters which effect the performance of the device in certain operationally extreme situations. Electrical stresses induced during operation at elevated temperatures are effective in screening marginal diffusion problems. The activation energy associated with this general mechanism is difficult to assign without knowing more about the exact process, but it can be assumed to be 1.0eV for other than the dielectric breakdown.

OXIDE

Oxide related faults can be found in the thermally grown oxide regions or in the deposited passivation layers. Defects in the latter sometimes lead to chemical attack of the underlying layers if corrosive elements are present. Activation energies for these types of defects are very large (>1.0eV). Metal-to-metal or metal-to-semiconductor breakdown can also occur. These are often caused by pinholes, contaminants in the oxide or with photolithographic defects. Though the time dependence for oxide failure is more voltage than temperature related, life-tests are effective in electrically stressing oxide imperfections.

BULK

Bulk (silicon) defects are those associated with the silicon wafer or die itself, such as crystal imperfections, resistivity gradients, expitaxial layer defects, damage to the die, and foreign material percipitates. These defects in themselves do not change with time at even the highest die operating temperatures, but they can become part of the active region of the device when built-in charge changes occur. This failure mode is very rare. Of the total failure rate percentage, this type of failure occurs less than 1% of the time.

SURFACE

Ionic contamination inducing inversion and channeling are the most frequently detected surface related mechanisms. At elevated temperatures, ions become mobile in or on the oxide covering the die. If the device is powered, the ions will be attracted to high field regions that exist near reverse biased junctions. This accumulation of charge can induce a surface layer (channel) of a conduction type opposite to that of the adjacent region (inversion), i.e., an N-type channel on a P-type region. Additional modes of failure are altered parasitic device characteristics, parasitic capacitance and "leaky" bipolar junction characteristics. The effects of built-in charge may be very slow in appearing, showing up only after many hours under bias at elevated temperatures. The activation energy associated with charge migration in silicon dioxide has been found to be 0.5 to 1.0eV.

METALLIZATION

A familiar mechanism of metallization-related failures is metal migration. When high current densities on the order of hundreds of thousands of amps per square centimeter occur at elevated temperatures, the metal (aluminum) atoms are carried along by the electron flow, causing migration of the metallization opposite to the direction of current flow which results in wear out. This may be in the form of disconnects, breaks, metal lead opens, etc. AMD's design rules for a metallization stripe cross section provide for a maximum current density of 200,000 amperes per square centimeter, well within the MIL-M-38510 maximum allowable current density for glassivated aluminum conductors. The activation energy of electromigration has been determined to be 0.5 to 1.0eV.

Open metallization detected in failed devices may be due to metal migration. The high current condition required to cause metal migration is often found to be the result of a defective circuit element. Photolithographic or masking defects sometimes result in reduction of metallization cross-section which is sufficient to allow metal migration to occur. The mechanism by which a severely scratch-damaged metal stripe opens in a very localized area is probably metal migration. Open or short conditions will be easily detected during internal visual inspection. Subtle defects, such as reduced cross-sectional area, can be detected by a dynamic life test at high temperature.

INTERCONNECT, WIREBOND AND PACKAGE SEAL/LEAD DEFECTS

The interconnect category includes failures that result from the "flying" lead being damaged by nicking, by work-stressing during bonding and by handling subsequent to the wirebond operation. The wirebond category includes all types of bond failures, including intermetallic formation. The package seal/lead defect category includes hermeticity failures and hermeticity-related failures such as corrosion. None of these failure types are found in a life-test program. They are controlled by material selection, receiving inspection and extensive control of the assembly process. The success at these controls is verified by examining the results of quality conformance testing for military and "Hi-Rel" customers, specifically, the group B and group D tests (MIL-STD-883, method 5005). The group B test (lot acceptance test) includes a wirebond strength test. The group D test is a pure-package quality conformance test and includes tests for lead integrity, resistance to thermal shock, temperature cycling, moisture resistance, mechanical shock, vibration, centrifuge, and salt atmosphere exposure. Group B and D testing is periodically performed by AMD and is available for inspection.

ACCELERATED TESTING

Semiconductor devices fail as a consequence of certain physical, metallurgical and chemical processes, all of which have temperature-dependent rates. The rates may also be potential or current dependent, but these dependencies are generally second-order effects. Users of electronic components are aware of the thermal effect and have frequently borrowed the organic chemist's rule of thumb, that reaction rates double for a 10°C temperature rise, to estimate the effects of high temperature life testing. This procedure does not provide the proper acceleration factor if applied for more than a decade or two of temperature and is quite inaccurate in estimating a 70°C equivalence for a 125°C life test.

For most processes causing semiconductor failures, the Arrhenius equation enables us to determine realistic failure rates. Temperature variations and their corresponding reaction rates can also be calculated for semiconductor devices. The following equation can be used over the entire temperature range:

$$\lambda(T) = C_1 \exp(-E_a/KT)$$

where:

- $\lambda(T)$ = device failure rate (temperature-dependent)
- T = absolute temperature (°K)
- K = Boltzmann's constant (8.62×10^{-5}eV/°K)
- E_a = activation energy of the individual device failure mechanisms (eV)
- C_1 = a constant

The temperatures used are junction temperatures, and the ability to use higher temperatures to achieve acceleration is constrained by the maximum permissible junction temperature under bias. Junction temperatures can be computed using power dissipation and package thermal characteristics. The following equation shows how those temperatures were derived:

$$T_J = T_A + \theta_{JA}\left[(I_{CC_{max}})\,(V_{CC_{max}})\right]$$

To determine the acceleration factor for temperature, T_2, with reference to another temperature, T_1, simply divide the failure rate equations for the two temperatures:

$$\text{A.F.} = \frac{\lambda(T_1)}{\lambda(T_2)} = \exp\left[\frac{E_a}{K}\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right]$$

where:

A.F. = acceleration factor
$\lambda(T_1)/\lambda(T_2)$ = ratio of reaction rates (failure)

This equation contains one constant whose value is not known from physical theory: the activation energy, E_a. Activation energy reflects the temperature dependence of a particular failure mechanism or group of mechanisms. It has been determined experimentally for some specific processes. Various investigators disagree as to the exact value of E_a because such experiments are difficult to conduct and spurious failures occur to cloud the results. Table 1 shows the range of these values as determined by experimentation.

TABLE 1.
ACTIVATION ENERGIES FOR CERTAIN PROCESSES

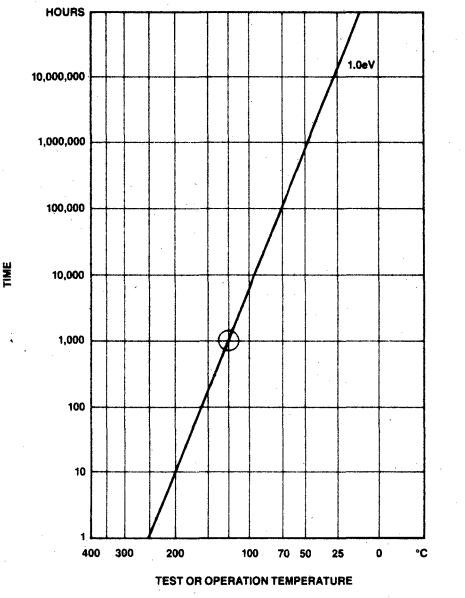
Surface Contamination	1.2 – 1.40eV
Electromigration	0.5 – 1.00eV
Oxide Defects (dielectric breakdown)	0.3 – 0.40eV
Corrosion	0.3 – 0.60eV
Intermetallic Growth (gold aluminum)	1.0 – 1.05eV
Slow Trapping	1.30eV

RELIABILITY TEST STUDY

The approach used in this report for evaluating reliability involves the concept of failure rates as a function of time. Life expectancy of devices can be categorized into three distinct intervals:

a. Infant Mortality
b. Operating Range
c. Old Age Mortality

An example of this distribution is shown in Figure 4. The results of this study are from long-term life tests. These tests are performed for 1000 hours or more without an initial burn-in. Therefore, "Infant Mortalities" are included in the failure rates of the units tested. With the inclusion of a burn-in process, the failure rates of the IMOX devices are expected to be less than the failure rates calculated in this report.



An Arrhenius plot may be used to predict the effect of temperature shift for a particular population at a given average activation energy. This plot has been set up around a 1000-hour test at 125°C for two activation energies, 1.0eV and 0.466eV. Equivalent test times of other temperatures may be determined for either a 1.0eV or a 0.466eV process. For example, an equivalent test time for 0.466eV at any temperature may be determined by simply picking an appropriate temperature and reading the number of hours corresponding to the intersection of the temperature and the 0.466eV line.

Figure 3. Arrhenius Plot

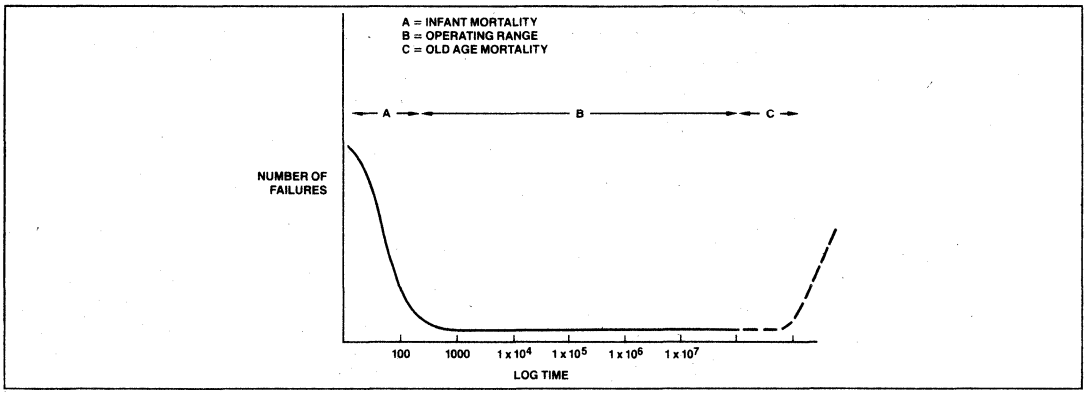


Figure 4. Life Expectancy of Devices

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Table 2 shows that units were subjected to HTOL (High Temperature Operating Life) testing at 125°C and 150°C per MIL-STD-883, method 1005 and 1015, conditions C and D. For an example of an HTOL circuit, see Figure 5. Data was collected on the SN54LS374A and the Am27S184/185 (cerdip and plastic) devices. The testing yielded 10,864,000 device hours worth of data. In total, 20 failures were recorded indicating a failure rate range (at 60% confidence level) of 0.183 – 0.50 per 1000 hours at 125°C using the chi-squared distribution.

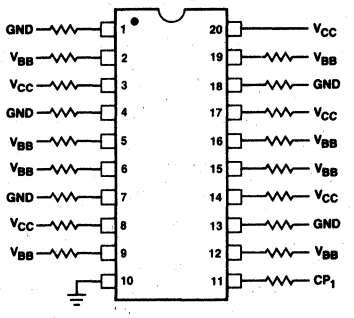
This table also includes corresponding calculated failure rates at lower temperatures using an activation energy level of 1.0eV. The failure rate for the IMOX processed SN54LS374A is less than .0025% per Khr at 70°C (cerdip) and less than .0045 per Khr at 70°C (plastic). The failure rate for the Am27S184/185 is less than .0120 per Khr. The lower temperatures (70°C and 25°C) are chosen to give users reliability predictions at the high end of the commercial operating temperature range and at the average "room temperature" operating temperature of a commercial system.

Other IMOX Bipolar devices which are presently undergoing HTOL testing are: Am2901C, Am29116 and Am29516. After recently completing 1000 cumulative hours of dynamic life testing (condition D) at 125°C, the 94-piece lot of Am2901C's resulted in a zero reject rate. Preliminary data has been gathered on each device type. At this time, statistically calculated rates would not accurately reflect the products' failure rate. After further testing is complete, failure rates will be calculated for each product and supplied in an addendum to this report.

SUMMARY

This report summarizes the actual reliability testing of AMD's proprietary process, IMOX. The statistical data and charts are presented to provide accurate comparative information. The demonstrated failure rates of the devices at 70°C reflect the high reliability of IMOX processed products. The design rules for IMOX processing are the same for all Bipolar products. Therefore, similar testing performed on other Bipolar devices, i.e., Am29116, would also result in very low failure rates as seen in this study.

Analysis of the various failures have shown that the device failures were of a random mode and their degree of occurrence was inconsistent. No inherent process failure mechanism has been found in the IMOX process. In conclusion, IMOX is the superior method for Bipolar wafer fabrication and for building high reliability into AMD devices.



POWER SUPPLY SETTINGS

Supply No.	Signal	Voltage
1	V_{BB}	+5.0V ±
2	V_{CC}	+5.0V ±

Conditions: 1. Pin 10: Device Ground
2. Pin 11: CP_1 – 100KHz ± 10%
High levels: +3.0V to +5.0V
Low levels: −0.2V to −1.2V

MIL-STD-883 Method 1015 Condition C
C – Steady state, power and reverse bias.
Inputs reverse biased.
This circuit was used for testing the SN54LS374A.

Figure 5. HTOL Circuit Configuration

TABLE 2. IMOX RELIABILITY OPERATING LIFE TEST DATA SUMMARY

Device	Number of Units	Device Khrs	Number of Rejects	%Fail Per Khr	λ 125°C	λ 70°C	λ 25°C	Fits 70°C	Fits 25°C
54LS374A									
Cerdip	1435	6856	11	0.160	0.183	0.002	.00001	17	0.1
Plastic	1110	3825	9	0.235	0.274	0.003	.000015	26	0.15
27S184/185	263	183	0	0	0.50	0.0046	.000028	46	0.28
29116	**Life Test in Progress**								
29516	**Life Test in Progress**								
IMOX Total	2808	10864	20	0.184	0.20	0.0018	.0000114	18	0.114

Notes: 1. All calculated failure rates and Fits Nos. use the Arrhenius Equation with 1.0VeV activation energy.
2. Fits = Failure in 10^9 hrs at 70°C and 25°C using a 60% confidence level.

References

IMOX Reliability Report by Beverly Henry. In preparation of this report, Chris King, Wisty Olsson, Ann Rosser, Chris Schmidt and Pauline Seales provided valuable assistance.

Gate Counts and Die Sizes by Device

The following data is useful for hybrid design and for MIL-STD reliability calculations. The gate counts are only an approximation for LSI devices because the circuit implementation often uses multi-level gates and unique logic structures, not just NAND and NOR gates.

Am25S/25LS

Part Number	Equivalent Number of Gates (Approximate)	Die Area (in Mils^2 = .001 x .001 in.)	Die Dimensions (in Mils = .001 in.)
AM25S05	86	9680	88 x 110
AM25LS07	26	6300	75 x 84
AM25S07	26	5810	70 x 83
AM25LS08	18	4575	75 x 61
AM25S08	18	4891	67 x 73
AM25LS09	30	4575	75 x 61
AM25S09	30	4891	67 x 73
AM25S10	29	3696	56 x 66
AM25LS14	Replaced by Am25LS14A		
AM25LS14A	167	7980	84 x 95
AM25LS15	92	9025	95 x 95
AM25S18	30	6083	77 x 79
AM25LS22	82	10,752	96 x 112
AM25LS23	88	10,752	96 x 112
AM25S557	1115	28,215	171 x 165
AM25S558	1115	28,215	171 x 165
AM25LS2513	33	6970	82 x 85
AM25LS2517	89	9828	91 x 108
AM25LS2518	30	8217	83 x 99
AM25LS2519	59	8217	83 x 99
AM25LS2520	84	8880	80 x 111
AM25LS2521	26	4662	63 x 74
AM25LS2535	52	7920	80 x 99
AM25LS2536	66	8316	84 x 99
AM25LS2537	42	7776	81 x 96
AM25LS2538	34	7776	81 x 96
AM25LS2539	38	7776	81 x 96
AM25LS2548	18	7776	81 x 96
AM25LS2568	87	8549	87 x 103
AM25LS2569	79	8549	87 x 103

Gate Counts and Die Sizes

Am26S/26LS

Part Number	Equivalent Number of Gates (Approximate)	Die Area (in Mils^2 = .001 x .001 in.)	Die Dimensions (in Mils = .001 in.)
AM26S02	N/A	4402	62 x 71
AM26S10	9	4425	59 x 75
AM26S11	13	4425	59 x 75
AM26S12	9	5112	71 x 72
AM26S12A	9	5112	71 x 72
AM26LS27	In development		
AM26LS28	In development		
AM26LS29	6	6580	70 x 94
AM26LS30	6	6580	70 x 94
AM26LS31	10	5628	67 x 84
AM26LS32	6	4704	56 x 84
AM26LS32B	6	4704	56 x 84
AM26LS33	6	4704	56 x 84
AM26LS34	6	4704	56 x 84
AM26LS38	72	6208	64 x 97

Am2900

Part Number	Equivalent Number of Gates (Approximate)	Die Area (in Mils^2 = .001 x .001 in.)	Die Dimensions (in Mils = .001 in.)
AM2901	Replaced by Am2901B and Am2901C		
AM2901A	Replaced by Am2901B and Am2901C		
AM2901B	538	14,976	117 x 128
AM2901C	550	15,990	130 x 123
AM2902	Replaced by Am2902A		
AM2902A	19	4154	62 x 67
AM2903	630	32,111	163 x 197
AM2903A	752	36,808	172 x 214
AM2904	283	22,540	140 x 161
AM2905	49	10,400	80 x 130
AM2906	56	10,400	80 x 130
AM2907	52	9064	88 x 103
AM2908	52	9064	88 x 103
AM2909	Replaced by Am2909A		
AM2909A	225	6831	69 x 99
AM2910	736	32,980	170 x 194
AM2910A	In development		
AM2911	Replaced by Am2911A		
AM2911A	221	6664	68 x 98
AM2912	9	4425	59 x 75
AM2913	33	6970	82 x 85
AM2914	335	24,871	133 x 187
AM2915A	49	9620	74 x 130
AM2916A	56	9620	74 x 130
AM2917A	52	9620	74 x 130
AM2918	30	6083	77 x 79

Am2900 (Cont.)

Part Number	Equivalent Number of Gates (Approximate)	Die Area (in Mils^2 = .001 x .001 in.)	Die Dimensions (in Mils = .001 in.)
AM29LS18	30	8217	83 x 99
AM2919	59	8217	83 x 99
AM2920	84	8880	80 x 111
AM2921	34	7776	81 x 96
AM2922	52	7920	80 x 99
AM2923	18	4288	64 x 67
AM2924	17	4550	65 x 70
AM2925	120	11,834	97 x 122
AM2926	10	5278	58 x 91
AM2927	72	12,096	87 x 144
AM2928	95	12,096	87 x 144
AM2929	10	5278	58 x 91
AM2930	548	26,600	133 x 200
AM2932	521	26,600	133 x 200
AM2940	415	32,037	177 x 181
AM2942	415	32,037	177 x 181
AM2946	18	6141	69 x 89
AM2947	18	6141	69 x 89
AM2948	18	6141	69 x 89
AM2949	18	6141	69 x 89
AM2950	175	14,766	107 x 138
AM2950A	In development		
AM2951	175	14,766	107 x 138
AM2951A	In development		
AM2952	102	14,873	107 x 139
AM2952A	In development		
AM2953	102	14,873	107 x 139
AM2953A	In development		
AM2954	50	7968	96 x 83
AM2955	50	7968	96 x 83
AM2956	50	7854	66 x 119
AM2957	50	7854	66 x 119
AM2958	10	5369	59 x 91
AM2959	10	5369	59 x 91
AM2960	450	13,056	102 x 128
AM2960A	In development		
AM2961	82	8874	102 x 87
AM2962	74	8874	102 x 87
AM2964B	170	22,308	156 x 143
AM2965	10	5640	94 x 60
AM2966	10	5640	94 x 60
AM2968	In development		
AM2969	In development		
AM2970	In development		
AM29112	In development		
AM29116	2500	78,061	251 x 311
AM29116A	In development		

Gate Counts and Die Sizes
Am2900 (Cont.)

Part Number	Equivalent Number of Gates (Approximate)	Die Area (in Mils^2 = .001 x .001 in.)	Die Dimensions (in Mils = .001 in.)
AM29203	752	36,808	172 x 214
AM29501	1000	64,158	289 x 222
AM29510	In development		
AM29516	2100	55,500	250 x 222
AM29516A	In development		
AM29517	2100	55,500	250 x 222
AM29517A	In development		
AM29520	362	15,327	117 x 131
AM29521	362	15,327	117 x 131
AM29526	N/A	N/A	N/A
AM29527	N/A	N/A	N/A
AM29528	N/A	N/A	N/A
AM29529	N/A	N/A	N/A
AM29540	1125	N/A	N/A
AM29705	258	13,056	102 x 128
AM29705A	206	9984	104 x 96
AM29707	207	9984	104 x 96
AM29803A	N/A	N/A	N/A
AM29806	42	6468	66 x 98
AM29809	42	6468	66 x 98
AM29811A	N/A	N/A	N/A
AM29818	152	11,328	96 x 118
AM29821	72	5376	64 x 84
AM29822	72	5376	64 x 84
AM29823	68	5376	64 x 84
AM29824	68	5376	64 x 84
AM29825	61	5376	64 x 84
AM29826	61	5376	64 x 84
AM29827	11	N/A	N/A
AM29828	11	N/A	N/A
AM29833	In development		
AM29834	In development		
AM29841	52	5376	84 x 64
AM29842	52	5376	84 x 64
AM29843	49	5376	84 x 64
AM29844	49	5376	84 x 64
AM29845	44	5376	84 x 64
AM29846	44	5376	84 x 64
AM29853	In development		
AM29854	In development		
AM29861	22	N/A	N/A
AM29862	22	N/A	N/A
AM29863	20	N/A	N/A
AM29864	20	N/A	N/A

8XXX MOS MPU Support

Part Number	Equivalent Number of Gates (Approximate)	Die Area (in Mils^2 = .001 x .001 in.)	Die Dimensions (in Mils = .001 in.)
AM8120	84	8880	80 x 111
AM8127	135	8624	98 x 88
AM8163	350	28,860	185 x 156
AM8167	350	28,860	185 x 156
AM8212	N/A	10,192	91 x 112
AM8216	10	5940	66 x 90
AM8224	47	7140	85 x 84
AM8226	10	5940	66 x 90
AM8228	N/A	14,960	110 x 136
AM8238	N/A	14,960	110 x 136

Package Material Configurations

	Multilayer Ceramic			Ceramic			
	Brazed Packages		Chip Carrier	Cerdip		Plastic	
Package Body Material	90% Alumina (Min)		90% Alumina (Min)	90% Alumina (Min)		Novolac Epoxy	
Die Attach Pad Metallization	Gold		Gold	Gold	Silver Palladium	Gold	Silver
Die Attach Material	Gold/Silicon		Gold/Silicon	Gold/ Silicon	Gold	Gold/ Silicon	Silver Epoxy
Die Attach Temperature	440°C Max		440°C Max	440°C Max		440°C Max	200°C (Curing Temp)
Bond Finger Metallization	Gold		Gold	Aluminum		Gold or Silver	
Bonding Wire	Aluminum/1% Silicon		Aluminum/1% Silicon	Aluminum/1% Silicon		Gold	
Bonding Method	Ultrasonic		Ultrasonic	Ultrasonic		Ball-bonding	
Seal Ring Metallization	Gold		Gold	None		N/A	
Seal Material	Gold/Tin	Lead/Tin/ Silver	Gold/Tin	Vitreous Glass		N/A	
Lid Material	Alloy 42 (Gold Plated)	Alloy 42 Tin Plated	Alloy 42 (Gold Plated)	90% Alumina (Min)		N/A	
Seal Temperature	370°C Max		370°C Max	470°C Max		175°C Max (Mold Temperature)	
Seal Ambient	Nitrogen		Nitrogen	Air		N/A	
Lead Material	Alloy 42		N/A	Alloy 42		Alloy 42	Copper
Lead Finish	Gold	Tin	N/A	Tin		Solder	

Thermal Characterization of Packaged Devices

AMD Technical Report TR-202
by J.L. Hayward

DEFINITION OF THERMAL RESISTANCE

The reliability of an integrated circuit is largely dependent on the maximum temperature which the device will attain during operation. Because the stability of a semiconductor junction declines with increasing temperature, knowledge of the thermal properties of the packaged device becomes an important factor during device design. In order to increase the operating lifetime of a given device, the junction temperatures must be minimized. This demands knowledge of the thermal resistance of the completed assembly and specification of the conditions in which the device will function properly. As devices become both smaller and more complex and the requirement for high speed operation becomes more important, heat dissipation will become an ever more critical parameter.

Thermal resistance is defined as the temperature rise per unit power dissipation above some referenced condition. The unit of measure is typically °C/watt. The relationship between junction temperature and thermal resistance is given by:

$$T_j = T_x + P_d R_{\theta JX} \quad (1)$$

where T_j = junction temperature
T_x = reference temperature
P_d = power dissipation
$R_{\theta JX}$ = thermal resistance
X = some defined test condition.

In general, one of three conditions is defined for measurement of thermal resistance:

$R_{\theta JC}$ – thermal resistance measured with reference to the temperature at some specified point on the package surface.

$R_{\theta JA}$ (still air) – thermal resistance measured with respect to the temperature of a specified volume of still air.

$R_{\theta JA}$ (moving air) – thermal resistance measured with respect to the temperature of air moving at a specified velocity.

The relationship between $R_{\theta JC}$ and $R_{\theta JA}$ is

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where $R_{\theta CA}$ is a measure of the heat dissipation due to natural convection (still air) or forced convection (moving air) and the effect of heat radiation and mounting techniques. $R_{\theta JC}$ is dependent solely on material properties and package geometry; $R_{\theta JA}$ includes the influence of the surface area of the package and environmental conditions. Each of these definitions of thermal resistance is an attempt to simulate some manner in which the package device may be used.

The thermal resistance of a packaged device, however measured, is a summation of the thermal resistances of the individual components of the assembly. These in turn are functions of the thermal conductivity of the component materials and the geometry of the heat flow paths. Like other material properties, thermal conductivity is usually temperature dependent. For alumina and silicon, two common package materials, this dependence can amount to a 30% variation in thermal conductivity over the operating temperature range of the device. The thermal resistance of a component is given by

$$R_\theta = \frac{L}{K(T)A} \quad (2)$$

where L = length of the heat flow path
A = cross sectional area of the heat flow path
K(T) = thermal conductivity as a function of temperature

and the overall thermal resistance of the assembly (discounting convective effects) will be:

$$R_\theta = \Sigma R_{\theta n} = \Sigma \frac{L}{K_n A}$$

But since the heat flow path through a component is influenced by the materials surrounding it, determination of L and A is not always straightforward.

A second factor that effects the thermal resistance of a packaged device is the power dissipation level and, more particularly, the relationship between power level and die geometry, i.e., power distribution and power density. By rearrangement of equation 1 to

$$P_d = \frac{1}{R_{\theta JX}}(T_j - T_x) = \frac{1}{\Sigma R_{\theta n}}(T_j - T_x) \quad (3)$$

the relationship between P_d and T_j can be more clearly seen. Thus, to dissipate a greater quantity of heat for a given geometry, T_j must increase and, since the individual $R_{\theta n}$ will also increase with temperature, the increase in T_j will not be a linear function of increasing power levels.

A third factor of concern is the quality of the material interfaces. In terms of package construction, this relates specifically to the die attach bond, and for those packages having a heatsink, the heatsink attach bond. The quality of the die attach bond will most severely influence the package thermal resistance as this is the area which first impedes the transfer of heat out of the silicon die. Indeed, it seems likely that the initial thermal response of a powered device can be directly related to the quality of the die attach bond.

EXPERIMENTAL METHOD

The technique for measurement of thermal resistance involves the identification of a temperature-sensitive parameter on the device and monitoring this parameter while the device is powered. For bipolar integrated circuits the forward voltage of the substrate isolation diode provides a convenient parameter to measure and has the advantage of a linear dependence on temperature. MOS devices which do not have an accessible substrate diode present greater measurement difficulties and may require simulation through use of a specially designed thermal test die. Choice of the parameter to be measured must be made with some care to insure that the results of the measurement are truly representative of the thermal state of the

device being investigated. Thus measurement of the substrate isolation diode which is generally diffused across the area of the die yields a weighted average of the condition of the individual junctions across the die surface. Measurement of a more local source would yield a less generalized result.

For those MOS devices for which no useful parameter is available, simulation is accomplished using the thermal test die. The basis for this test die is a 25 mil square cell containing an isolated diode and a 1KΩ resistor. The resistors are interconnected from cell to cell on the wafer before it is cut into multiple arrays of the basic unit cell. In use the device is powered via the resistors with voltage or current adjusted for the proper level and the voltage drop of the individual diodes is monitored as in the case of actual devices.

Prior to the thermal resistance test, the diode voltage/temperature calibration must be determined. This is done by measuring the forward voltage at 1mA current level at two different temperatures. The diode calibration factor is then:

$$K_f = \frac{T_2 - T_1}{V_2 - V_1} = \frac{\Delta T}{\Delta V} \qquad (4)$$

in units of °C/mV. For most diodes used for this test the voltage/temperature relationship is linear and these two measurement points are sufficient to determine the calibration.

The actual thermal resistance measurement has two alternating phases: measurement and power on. (See Figure 1.) The device under test is pulse powered with an ON duty cycle of 99% and a repetition rate of <100Hz. During the brief OFF states the device is reverse-biased with a 1mA current and the voltage drop is measured. The series of voltage readings are averaged over short periods and compared to the voltage reading obtained before the device was first powered ON. The thermal resistance is then computed as:

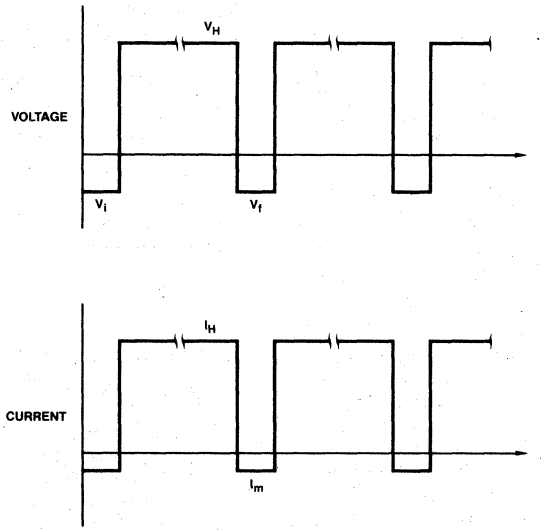
$$R_{\theta JX} = \frac{K_f (V_f - V_i)}{V_H I_H} = \frac{K_f \Delta V}{P_d} \qquad (5)$$

where K_f = calibration factor
V_i = initial forward voltage value
V_f = current forward voltage value
V_H = heating voltage
I_H = heating current

The pulsing measurement is continued until the device has reached thermal equilibrium and the final value measured is the equilibrium thermal resistance of the device under test.

When the end result desired is $R_{\theta JA}$ (still air), the device and the test fixture (typically a standard burn-in socket) are enclosed in a box containing approximately 1 cubic foot of air. For $R_{\theta JC}$ measurements the device is attached to a large metal heatsink. This insures that the reference point on the device surface is maintained at a constant temperature. Through the use of heaters attached to the metal fixture, the "case" temperature may be maintained at any specified value above ambient. The requirements for measurement of $R_{\theta JA}$ (moving air) are rather more complex. They involve the use of a small wind tunnel with capability for monitoring air pressure, temperature and velocity in the area immediately surrounding the device tested. Standardization of this last test requires much careful attention.

Figure 1. Waveforms for Pulsed Thermal Resistance Test



THERMAL CHARACTERIZATION DATA FOR CERDIPS[1]

Lead Count	Width (Inches)	Approximate $R_{\theta JA}$ Range (°C/W)	Approximate $R_{\theta JC}$ Range (°C/W)
16	0.300	66–89	22
20	0.300	68–78	N/A
24	0.300	55–57	13–14
24	0.600	49	11
28	0.600	29	N/A
40	0.600	36–37	7–9

THERMAL CHARACTERIZATION DATA FOR SIDE-BRAZE AND TOP-BRAZE PACKAGES

Lead Count	Type	Approximate $R_{\theta JA}$ Range (°C/W)	Approximate $R_{\theta JC}$ Range (°C/W)
40	Side-Braze	27–35	6–7
48	Side-Braze	37	10
52	Top-Braze with Heat-Spreader	19	4
64	Top-Braze with Heat-Spreader	20	7

THERMAL CHARACTERIZATION DATA FOR PLASTIC DIPs[1]

Lead Count	Width (Inches)	Approximate $R_{\theta JA}$ Range (°C/W)	Approximate $R_{\theta JC}$ Range (°C/W)
16	0.300	110*	N/A
20	0.300	81–123*	32*
24	0.600	99–115*	43–57*
28	0.600	85*	N/A
40	0.600	62–73*	27–34*

*In 1983 AMD will be introducing copper-lead-frame versions of all plastic packages. The copper-lead-frame versions will have better thermal characteristics than the current plastic packages measured above.

THERMAL CHARACTERIZATION DATA FOR LEADLESS CHIP CARRIERS (JEDEC TYPE C)[1]

Lead Count	Approximate $R_{\theta JA}$ Range (°C/W)	Approximate $R_{\theta JC}$ Range (°C/W)
20	66–72*	N/A
28	69*	N/A
44	52–57*	N/A
52	44*	N/A

*The $R_{\theta JA}$ values listed for leadless chip carriers were measured with the chip carriers mounted in the appropriate burn-in sockets. This restricts convection of heat from the package and results in θ values higher than might be expected in actual use.

THERMAL CHARACTERIZATION DATA FOR CERPAKS AND FLATPACKS[1]

Lead Count	Type	Approximate $R_{\theta JA}$ Range (°C/W)	Approximate $R_{\theta JC}$ Range (°C/W)
16	Cerpak	113–159	10–17
20	Cerpak	119	N/A
24	Cerpak	99	8
42	Brazed Flatpack	63	8

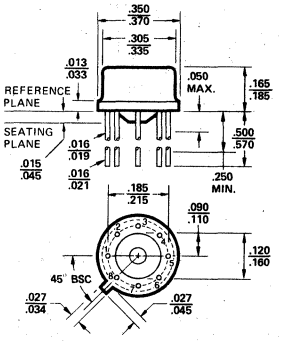
Note: 1. This data, while derived from actual measurements done on specific packaged devices, is only approximate and cannot be guaranteed because of the wide variation of die sizes and device power levels.

13

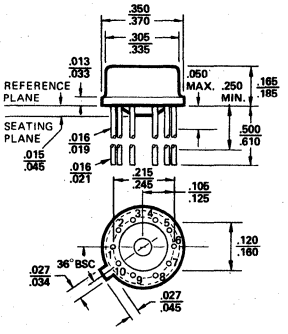
Package Outlines

METAL CAN PACKAGES

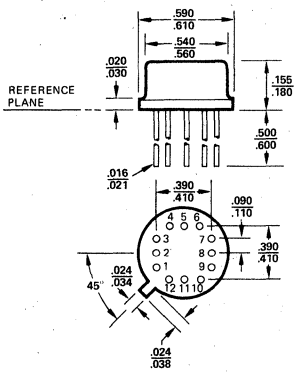
H-8-1



H-10-1



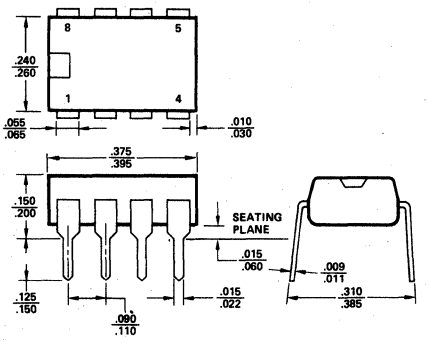
G-12-1



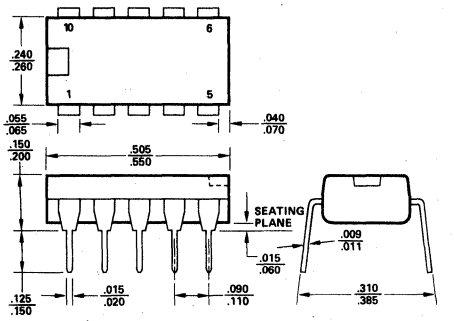
Note. Standard lead finish is bright acid tin plate or gold plate.

MOLDED DUAL IN-LINE PACKAGES

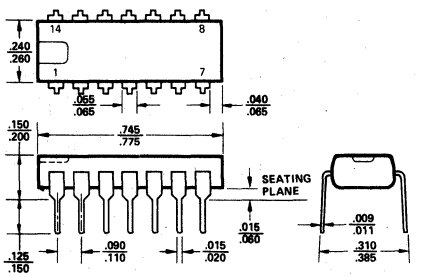
P-8-1



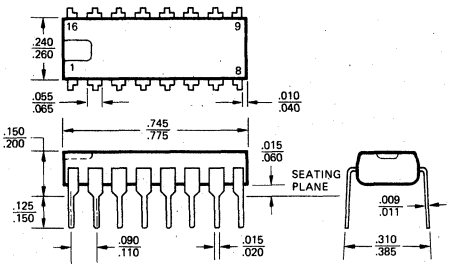
P-10-1



P-14-1



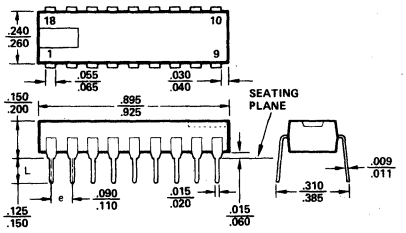
P-16-1



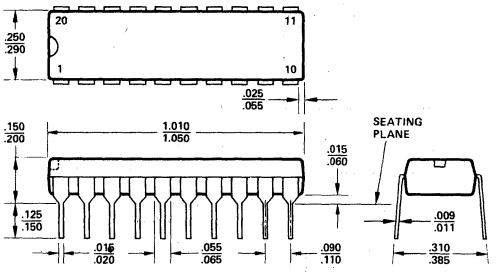
PACKAGE OUTLINES (Cont.)

MOLDED DUAL IN-LINE PACKAGES (Cont.)

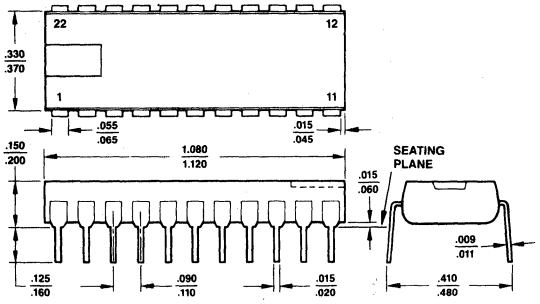
P-18-1



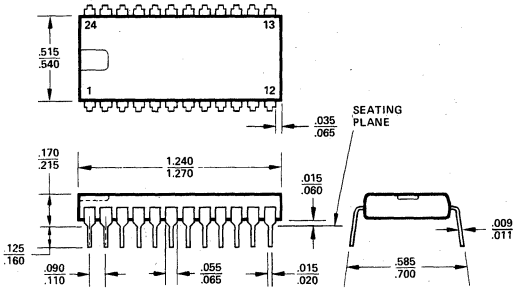
P-20-1



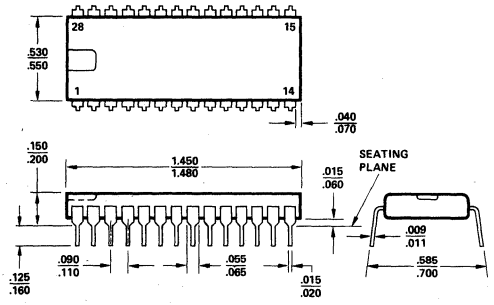
P-22-1



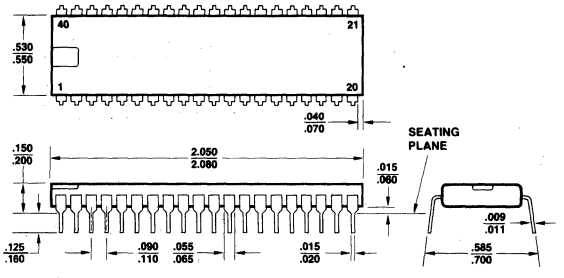
P-24-1



P-28-1



P-40-1

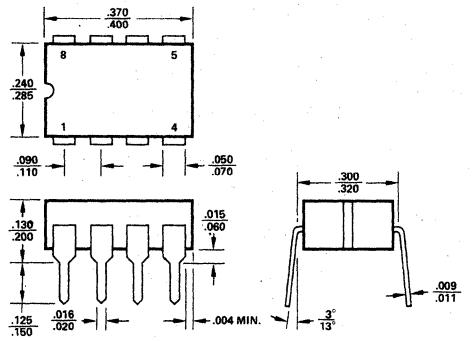


Note . Standard lead finish is tin plate or solder dip.

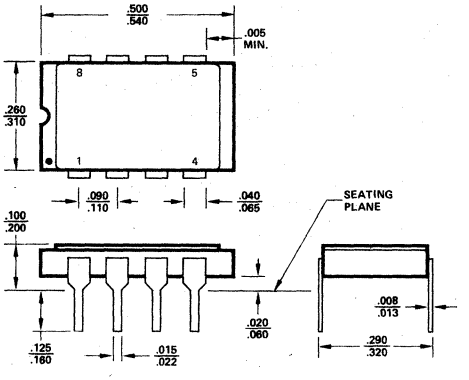
PACKAGE OUTLINES (Cont.)

HERMETIC DUAL IN-LINE PACKAGES

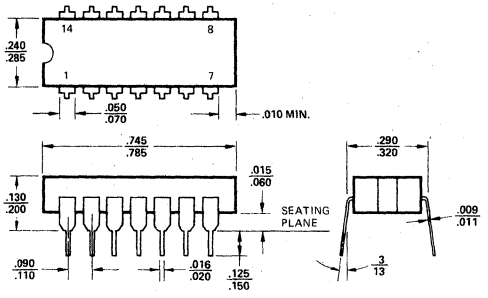
D-8-1



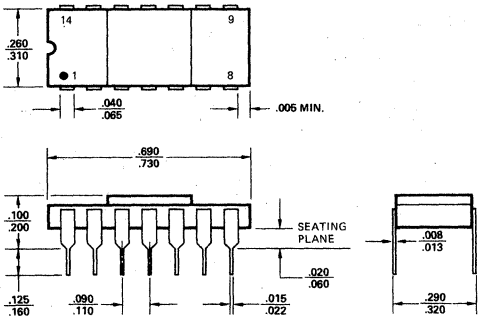
D-8-2



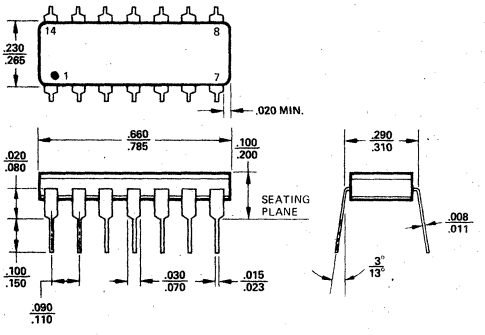
D-14-1



D-14-2



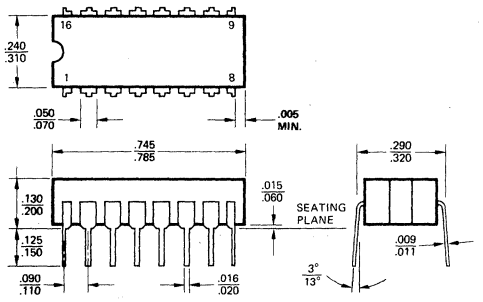
D-14-3



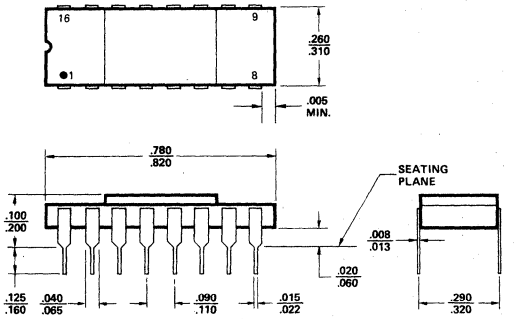
PACKAGE OUTLINES (Cont.)

HERMETIC DUAL IN-LINE PACKAGES (Cont.)

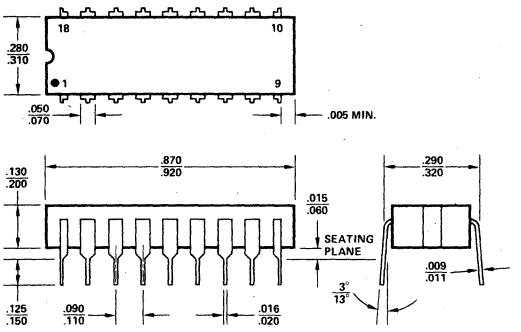
D-16-1



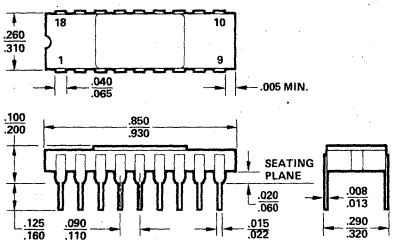
D-16-2



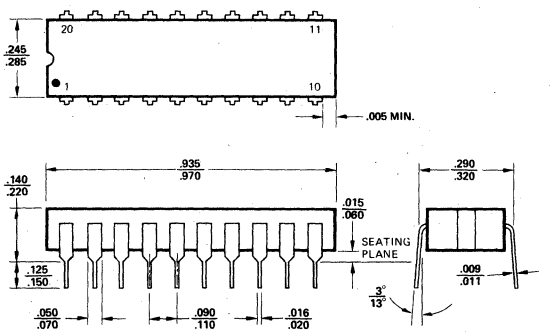
D-18-1



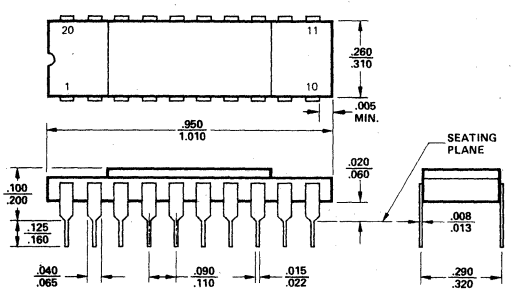
D-18-2



D-20-1



D-20-2

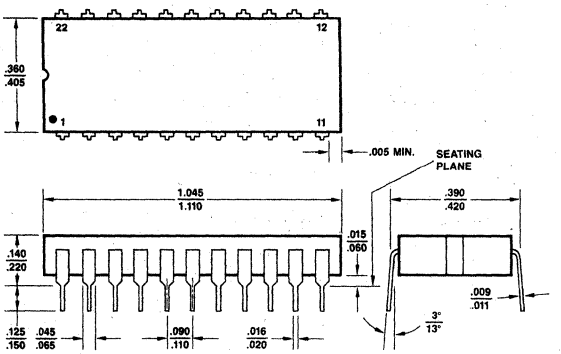


13

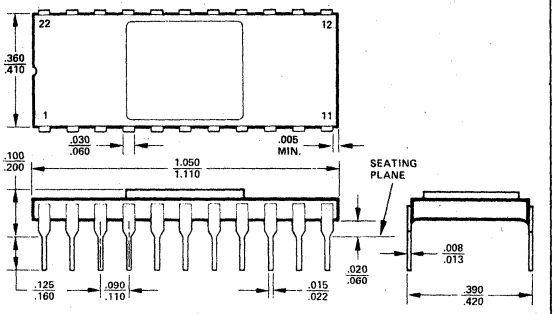
PACKAGE OUTLINES (Cont.)

HERMETIC DUAL IN-LINE PACKAGES (Cont.)

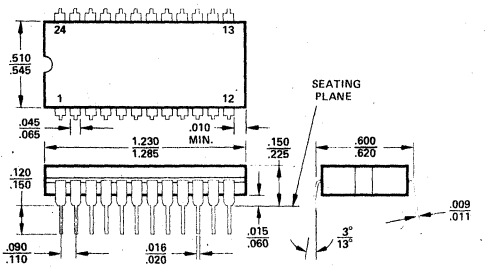
D-22-1



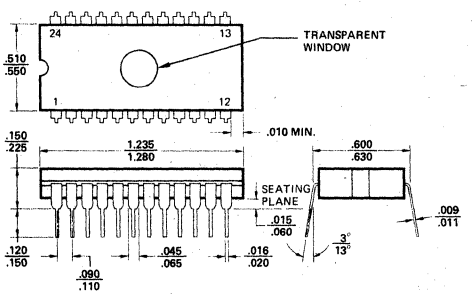
D-22-2



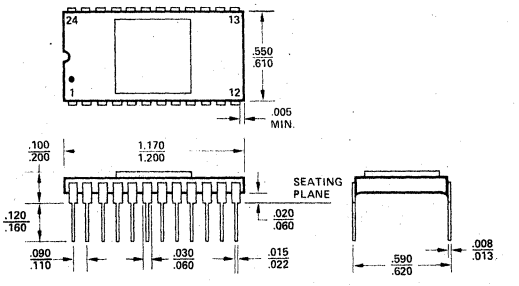
D-24-1 and D-24-4



D-24-4*



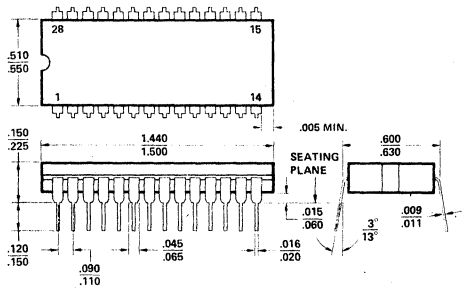
D-24-2



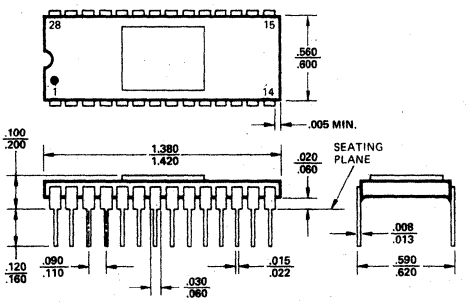
PACKAGE OUTLINES (Cont.)

HERMETIC DUAL IN-LINE PACKAGES (Cont.)

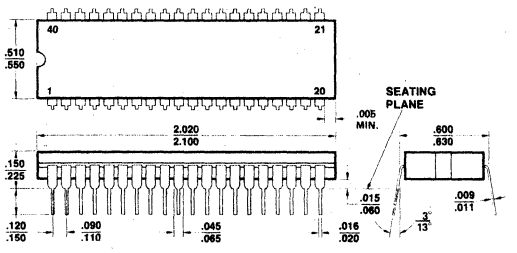
D-28-1



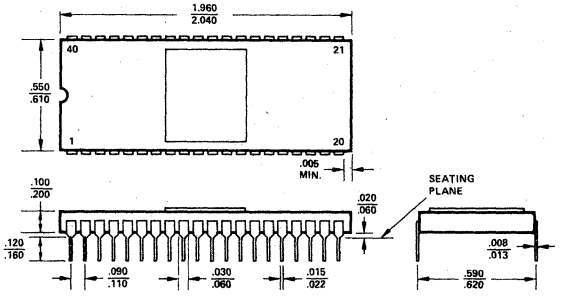
D-28-2



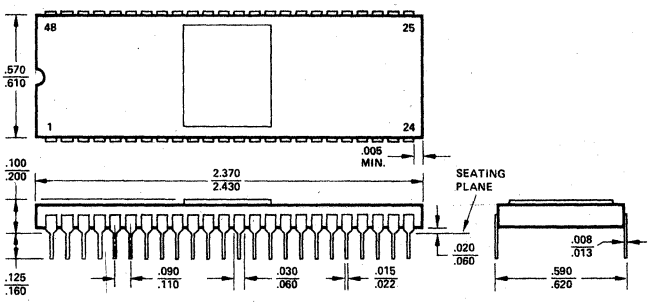
D-40-1



D-40-2



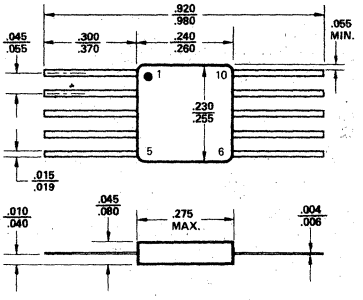
D-48-2



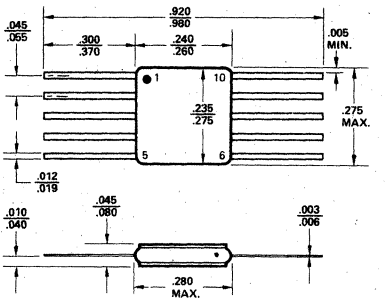
PACKAGE OUTLINES (Cont.)

FLAT PACKAGES

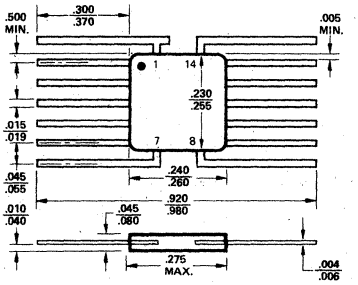
F-10-1



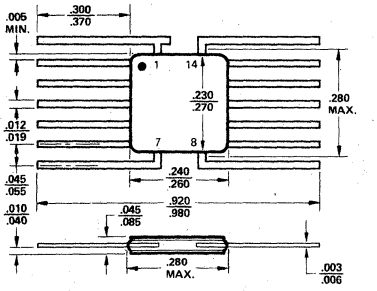
F-10-2



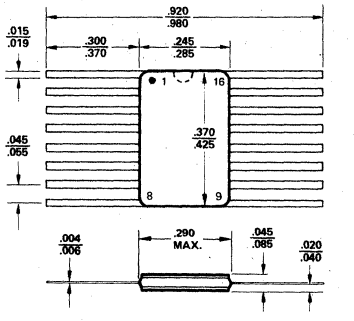
F-14-1



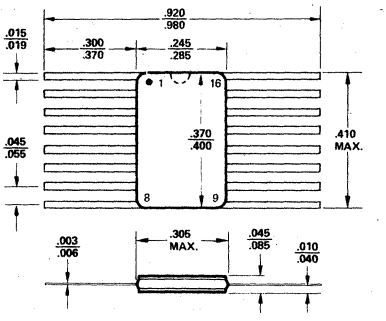
F-14-2



F-16-1

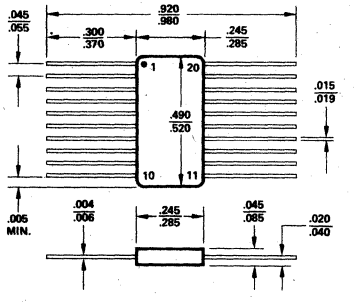


F-16-2

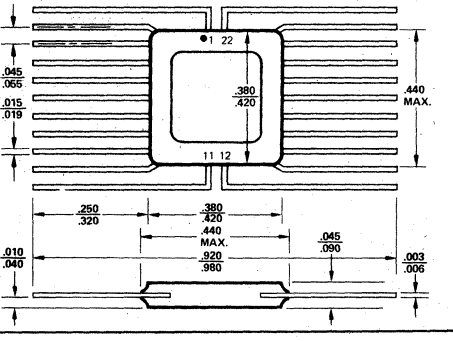


Note: Notch is pin 1 index on cerpack.

F-20-1



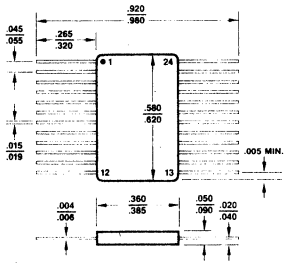
F-22-1



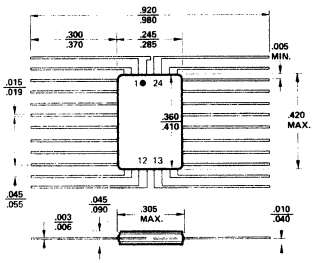
PACKAGE OUTLINES (Cont.)

FLAT PACKAGES (Cont.)

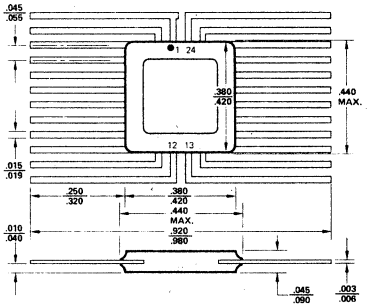
F-24-1



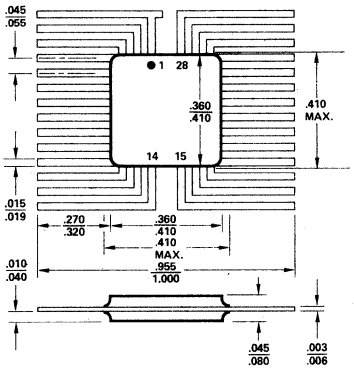
F-24-2



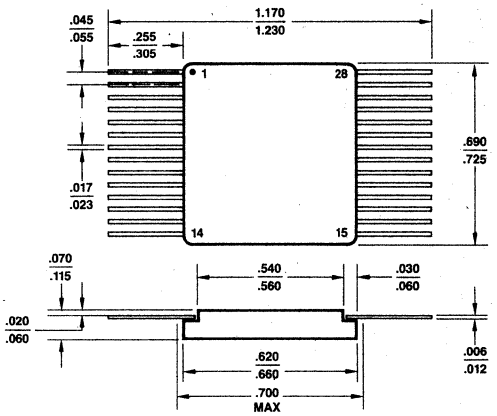
F-24-3



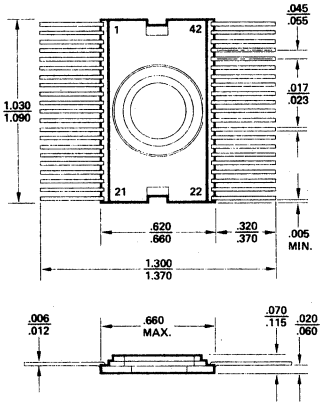
F-28-1



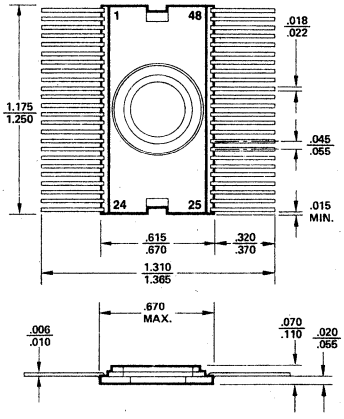
F-28-2 and F-28-3



F-42-1



F-48-2

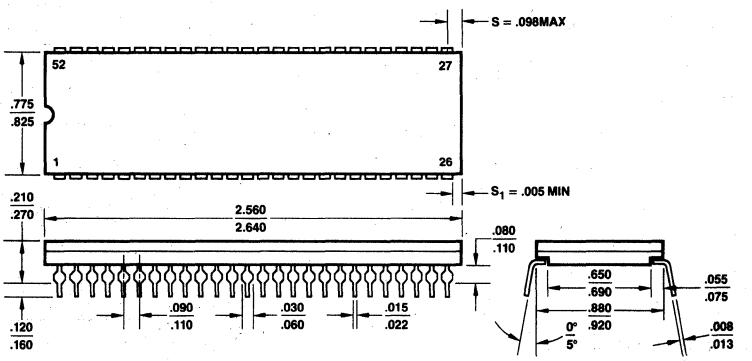


13

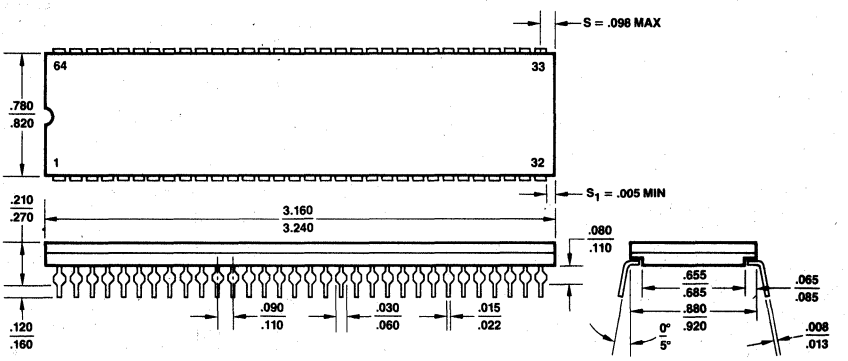
PACKAGE OUTLINES (Cont.)

HERMETIC DUAL IN-LINE PACKAGES (Cont.)

D-52-3



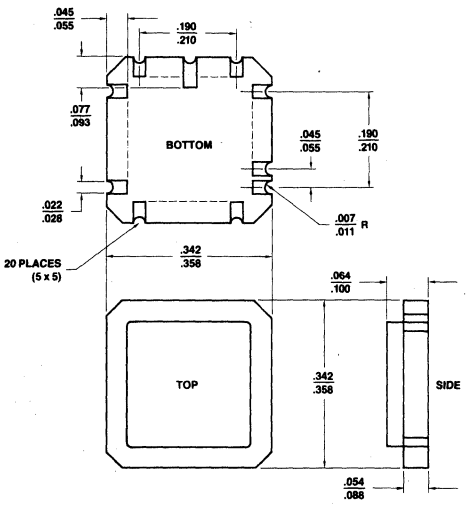
D-64-3



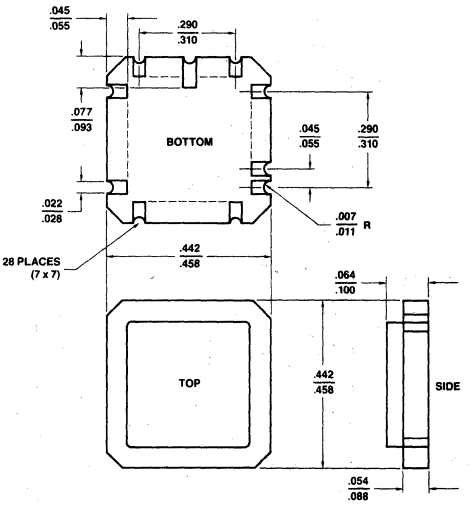
PACKAGE OUTLINES (Cont.)

SQUARE CHIP CARRIER FAMILY

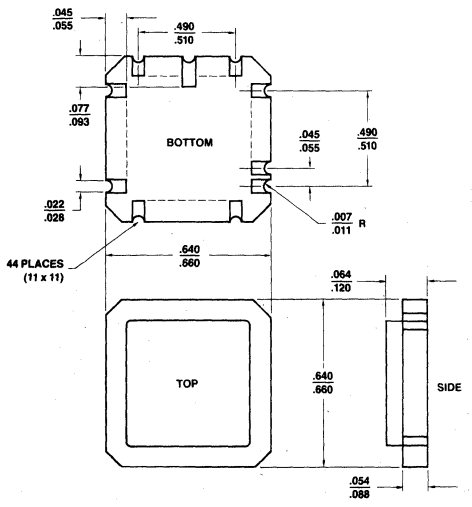
L-20-1



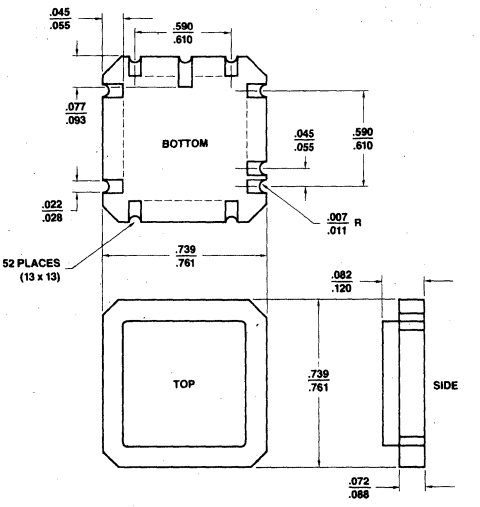
L-28-1



L-44-1



L-52-1

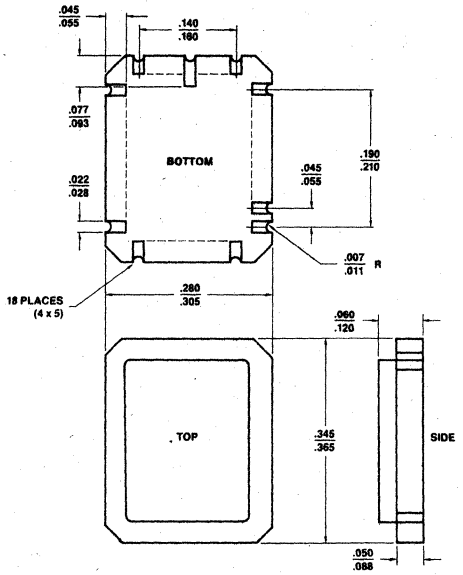


13

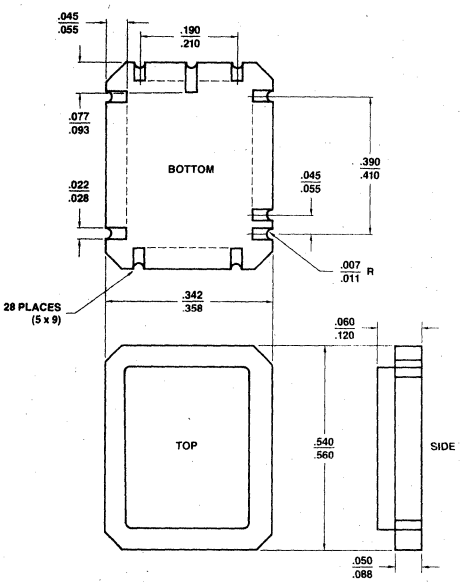
PACKAGE OUTLINES (Cont.)

RECTANGULAR CHIP CARRIER FAMILY

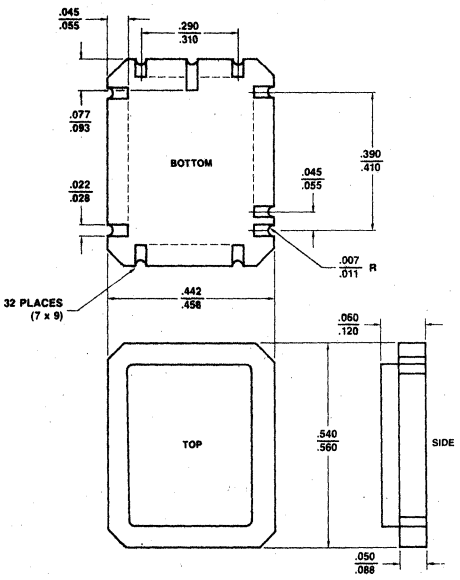
L-18-2



L-28-2



L-32-2



Ordering Information

All Advanced Micro Devices' products listed are stocked locally and distributed nationally by Franchised Distributors. See back of this book for the location nearest you. Please consult them for the latest price revisions. For direct factory orders, call local AMD Sales Office or Sales Representative. See the back of this book for the location nearest you.

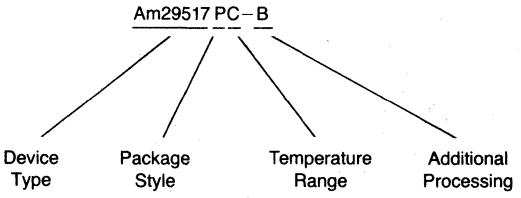
Minimum Order

The minimum direct factory order is $100.00 for a standard product.

The minimum direct factory order for Class B, burned-in, product is $250.00.

Proprietary Product Ordering, Package and Temperature Range Codes

The following scheme is used to identify Advanced Micro Devices' proprietary products.



Package Style

D = Hermetic DIP
F = Flat Package
P = Molded DIP
L = Leadless Chip Carrier
X = Dice

Temperature Range

C = Commercial
0°C to +70°C
M = Military
−55°C to +125°C

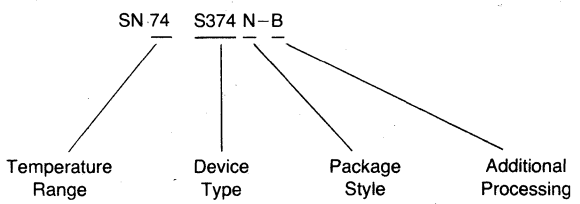
Additional Processing

B = Burn-in (Signifies full MIL-STD-883 Class B product for military temperature range devices)

Second Source Product Ordering, Package and Temperature Range Codes

An order number and marking system identical to the original manufacturer's is used for the Advanced Micro Devices' pin-for-pin and electrically equivalent circuit.

The following example is the ordering scheme for Advanced Micro Devices' second source to Texas Instruments' products.



Package Style

J = Hermetic DIP
N = Molded DIP
W = Flat Package
X = Dice

Temperature Range

74 = Commercial
0°C to +70°C
54 = Military
−55°C to +125°C

Additional Processing

B = Burn-in (Signifies full MIL-STD-883 Class B product for military temperature range devices)

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World-Wide Sales Offices

Advanced Micro Devices

Advanced Micro Devices maintains a network of representatives and distributors in the U.S. and around the world. For a sales agent nearest you, call one of the AMD offices listed below.

U.S. AND CANADIAN SALES OFFICES

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360 N. Sepulveda, Suite 2075
El Segundo, California 90245
Tel: (213) 640-3210

Advanced Micro Devices
10050 N. 25th Street
Suite 235
Phoenix, Arizona 85021
Tel: (602) 242-4400

Advanced Micro Devices
4000 MacArthur Boulevard
Suite 5000
Newport Beach, California 92660
Tel: (714) 752-6262

Advanced Micro Devices
5955 De Soto Avenue, Suite 241
Woodland Hills, California 91367
Tel: (213) 992-4155

Advanced Micro Devices
9455 Ridgehaven Court
Suite 230
San Diego, California 92123
Tel: (619) 560-7030

NORTHWEST AREA

Advanced Micro Devices
2700 Augustine Drive, Suite 109
Santa Clara, California 95051
Tel: (408) 727-1300

Advanced Micro Devices
1873 South Bellaire Street
Suite 920
Denver, Colorado 80222
Tel: (303) 691-5100

NORTHWEST AREA (Cont.)

Advanced Micro Devices
One Lincoln Center, Suite 230
10300 Southwest Greenburg Road
Portland, Oregon 97223
Tel: (503) 245-0080

Advanced Micro Devices
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600 108th Avenue N.E.
Bellevue, Washington 98004
Tel: (206) 455-3600

MID-AMERICA AREA

Advanced Micro Devices
500 Park Boulevard, Suite 940
Itasca, Illinois 60143
Tel: (312) 773-4422

Advanced Micro Devices
9900 Bren Road East, Suite 601
Minnetonka, Minnesota 55343
Tel: (612) 938-0001

Advanced Micro Devices
3592 Corporate Drive, Suite 108
Columbus, Ohio 43229
Tel: (614) 891-6455

Advanced Micro Devices
8240 MoPac Expressway
Two Park North, Suite 385
Austin, Texas 78759
Tel: (512) 346-7830

Advanced Micro Devices
6750 LBJ Freeway, Suite 1160
Dallas, Texas 75240
Tel: (214) 934-9099

MID-ATLANTIC AREA

Advanced Micro Devices
40 Crossways Park Way
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Tel: (516) 364-8020

Advanced Micro Devices
290 Elwood Davis Road
Suite 316
Liverpool, New York 13088
Tel: (315) 457-5400

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2 Kilmer Road
Edison, New Jersey 08817
Tel: (201) 985-6800

Advanced Micro Devices
107 Lakeside Drive
Horsham, Pennsylvania 19044
Tel: (215) 441-8210
TWX: 510-665-7572

Advanced Micro Devices
205 South Avenue
Poughkeepsie, New York 12601
Tel: (914) 471-8180
TWX: 510-248-4219

NORTHEAST AREA

Advanced Micro Devices
6 New England Executive Park
Burlington, Massachusetts 01803
Tel: (617) 273-3970

Advanced Micro Devices (Canada) Ltd.
2 Sheppard Avenue East
Suite 1610
Willowdale, Ontario
Canada M2N5Y7
Tel: (416) 224-5193

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Advanced Micro Devices
Parkway Center
One Parkway Drive Building
7257 Parkway Drive, Suite 204
Dorsey, Maryland 21076
Tel: (301) 796-9310

Advanced Micro Devices
7850 Ulmerton Road, Suite 1A
Largo, Florida 33541
Tel: (813) 535-9811

Advanced Micro Devices
4740 North State Road #7
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Ft. Lauderdale, Florida 33319
Tel: (305) 484-8600

Advanced Micro Devices
6755 Peachtree Industrial Boulevard
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Atlanta, Georgia 30360
Tel: (404) 449-7920

Advanced Micro Devices
8 Woodlawn Green, Suite 220
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Charlotte, North Carolina 28210
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INTERNATIONAL SALES OFFICES

BELGIUM
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TOLL FREE
(800) 538-8450

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