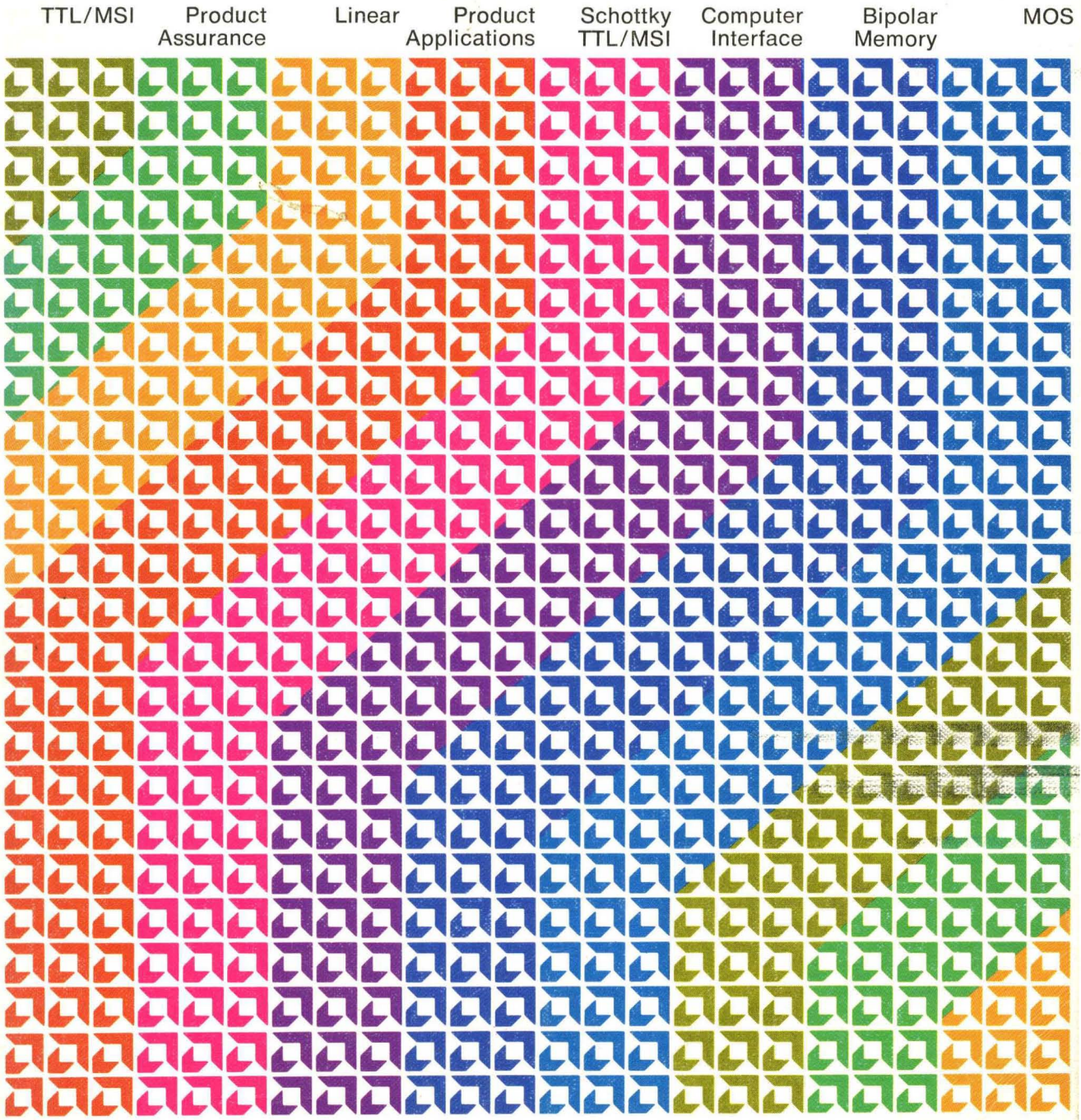

TTL/MSI
Product Assurance
Linear
Product Applications
Schottky TTL/MSI
Computer Interface
Bipolar Memory
MOS

Advanced Micro Devices

CATALOG SECTIONS

WE CALL IT A COMMITMENT TO EXCELLENCE

Five years ago Advanced Micro Devices was conceived on the premise that there was a place in the semiconductor community for a manufacturer dedicated to excellence. Excellence in engineering. Excellence in manufacturing.

In April, 1970, in the midst of the worst depression the industry has every experienced, this concept became reality with the introduction by Advanced Micro Devices of 18 Linear and MSI devices — all processed and tested to the rigid specifications of Military Standard 883.

Today, Advanced Micro Devices is acknowledged as one of the country's major manufacturers of complex, monolithic integrated circuits doing business at an annualized rate approaching $40 million. Our perfect record of sales growth (outlined in the per-quarter-performance chart) is unequaled in the semiconductor industry.

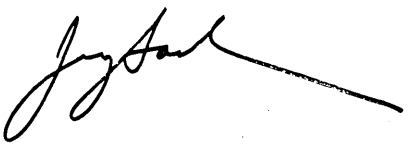
As a broad-line supplier of both commercial and aerospace circuits, we serve the manufacturers of computers, computer peripherals and instrumentation equipment. Our device portfolio numbers over 200 different Linear, MSI, MOS, Bipolar Memory and Computer Interface circuits.

Advanced Micro Devices has just started wafer fabrication in the first of two fab areas in our new 116,000-square-foot facility dedicated to the design and manufacture of the world's most technologically advanced MOS and Bipolar LSI circuits.

This index is a multiple cross-reference guide to familiarize you with our ever-growing product line, and help you locate by function or device type the circuits you need. If you don't find what you need, call — it's probably on the design boards. If you need more technical material on any of the circuits, send the attached card.

Advanced Micro Devices has grown from a concept to a major manufacturer in five years. This growth is attributed to our excellence in product development and manufacture. We process with excellence — we ship with pride.

Thank you for your support,



W. J. Sanders III
President and Chairman of the Board
June 3, 1974

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*Consult Factory

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PRODUCT SELECTION GUIDE

LINEAR INTEGRATED CIRCUITS

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	Very low input current precision	50pA I_B, 3mV Vos	Am216A	7-35
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VOLTAGE FOLLOWERS	Improved low input current, high-speed	3nA I_B, 4mV Vos 20V/μs slew rate	Am110	7-27

PRODUCT ASSURANCE
MIL-M-38510 • MIL-Q-9858A • MIL-STD-883
Complex Digital and Linear Circuits

The product assurance program at Advanced Micro Devices defines manufacturing flow, establishes standards and controls, and confirms the product quality at critical points. Standardization under this program assures that all products meet military and government agency specifications for reliable ground applications. Further screening for users desiring flight hardware and other higher reliability classes is simplified because starting product meets all initial requirements for high-reliability parts.

The quality standards and screening methods of this program are equally valuable for commercial parts where equipment must perform reliably with minimum field service.

Three military documents provide the foundation for this program. They are:

MIL-M-38510—General Specification for Microcircuits
MIL-Q-9858A—Quality Program Requirements
MIL-STD-883—Test Methods and Procedures for Microelectronics

MIL-M-38510 describes design, processing and assembly workmanship guidelines for military and space-grade integrated circuits. **All linear, MSI, and computer interface circuits manufactured by Advanced Micro Devices for full temperature range (−55°C to +125°C) operation meet these quality requirements of MIL-M-38510. There are no exceptions.**

MIL-Q-9858A identifies 28 elements of management, planning and control that are necessary in maintaining a quality program. **Advanced Micro Devices complies with all requirements of MIL-Q-9858A.**

MIL-STD-883 contains detail testing and inspection methods for integrated circuits. Three of the methods are quality and processing standards directly related to product assurance:

Test Method 2010.1 defines the visual inspection of integrated circuits before sealing. By confirming fabrication and assembly quality, inspection to this standard assures the user of reliable circuits in long-term field applications. Inspection at Advanced Micro Devices includes all the requirements of Method 2010.1, condition B. Further criteria have been added to cover omissions in the military specifications.

Test Method 5004.1 defines three reliability classes of parts. All must receive certain basic inspection, preconditioning and screening stresses. The classes are:

Class C — Used where replacement can be readily accomplished. Screening steps are given in the AMD processing flow chart.

Class B — Used where maintenance is difficult or expensive and where reliability is vital. Devices are upgraded from Class C to Class B by 168-hour burn-in at 125°C. All other process requirements are the same.

Class A — Used where replacement is extremely difficult and reliability is imperative. Class A screening selects extra reliability parts by expanded visual and X-ray inspection, further burn-in, and added mechanical and thermal shock stresses.

All hermetically sealed integrated circuits (military and commercial) manufactured by Advanced Micro Devices are screened to Class C. There are no exceptions. Electrical burn-in upgrades any product to a full Class B screened part on a short delivery cycle.

All molded integrated circuits receive applicable Class C screening (centrifuge and hermeticity steps are omitted for solid-package parts).

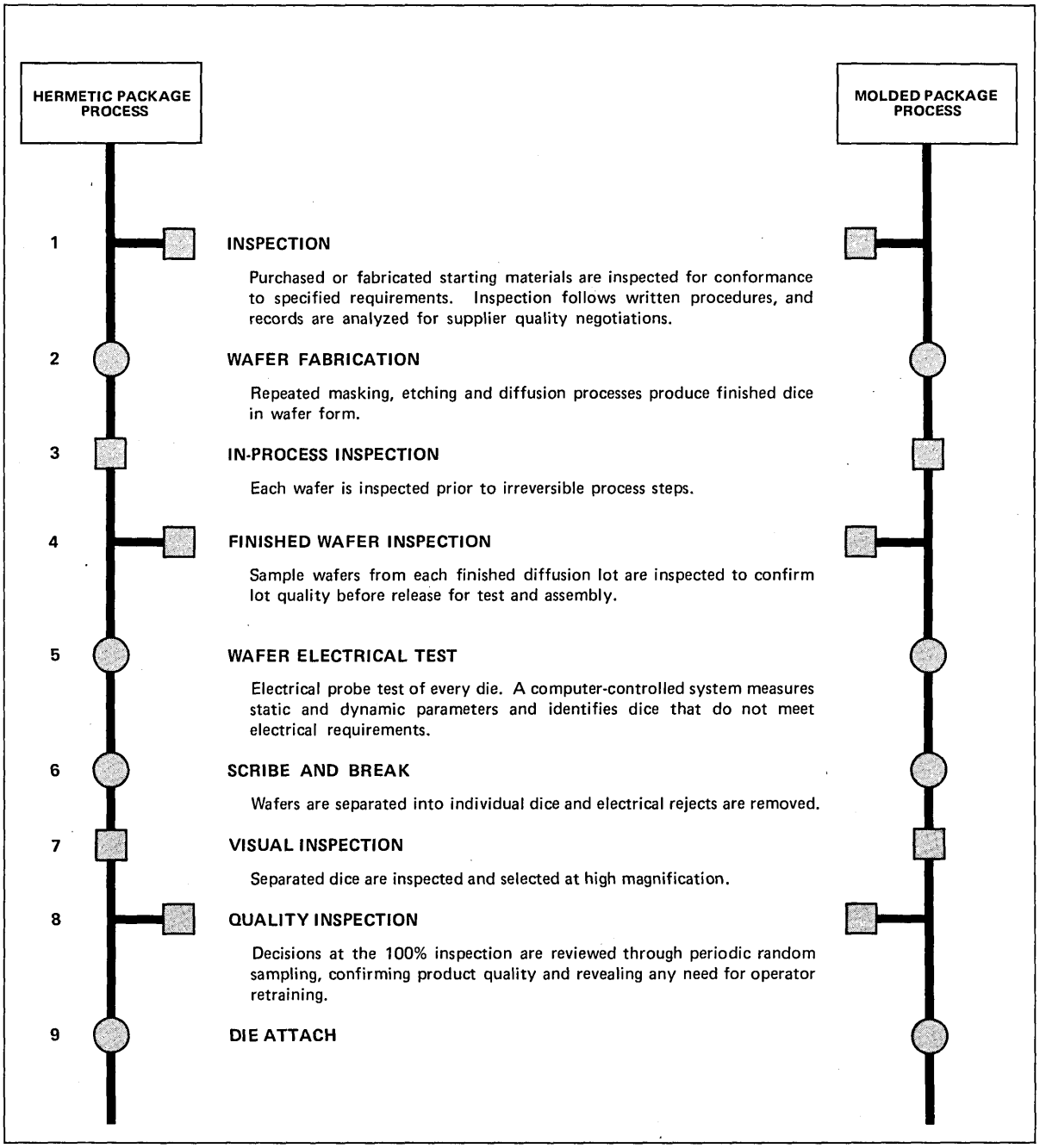
Test Method 5005.1 defines qualification and quality conformance procedures. Subgroups, tests and quality levels for each class are given for Group A (electrical), Group B (mechanical quality measurements related to the user's assembly environment), and Group C (long-term reliability and product design stress tests). Group A tests are always performed; Group B and C may be specified by the user. Tables I, II, and III give standard test groupings and quality levels for Class B screened devices. These quality levels are used as a minimum for all tests.

MANUFACTURING, SCREENING AND INSPECTION FOR INTEGRATED CIRCUITS

All integrated circuits are screened to MIL-STD-883, Method 5004.1, Class C; quality inspection is performed to Class B levels.

All full-temperature-range (–55°C to +125°C) linear, MSI and computer-interface circuits are manufactured to the workmanship requirements of MIL-M-38510.

The flow chart identifies processing steps as they relate to MIL-STD-883 and MIL-M-38510.



10 **QUALITY INSPECTION**

Strength of die attachment, position of die and visual quality of eutectic wetting are confirmed periodically by inspecting random samples and push-testing the attached dice.

11 **WIRE BOND**

Hermetic: Aluminum wires, ultrasonic bonding.
Molded: Gold wires, thermocompression bonding.

12 **QUALITY INSPECTION**

Weld strength, bond size and position, wire dress and general workmanship are confirmed periodically by comparing random samples with assembly instructions and quality standards. Bond strength is plotted on statistical control charts, providing early warning of process drifts.

13 **INTERNAL VISUAL INSPECTION**

Assembled but unsealed units are individually inspected at low and high power.

QUALITY STANDARDS:

All devices—MIL-STD-883, Method 2010.1 B.
Full temperature devices identified above—MIL-M-38510, Para. 3.7 for bonding workmanship.

14 **QUALITY INSPECTION**

Decisions at the 100% inspection are reviewed through periodic random sampling, providing confirmation of product quality and revealing any need for operator retraining.

15a **FINAL SEAL**

(Hermetic devices)

15b **ENCAPSULATE**

(Molded Devices)

16 **STABILIZATION BAKE**

MIL-STD-883, Method 1008, Cond. C: 150°C, 24 hr

17 **TEMPERATURE CYCLE**

MIL-STD-883, Method 1010, Cond. C: −65°C, +150°C, 10 cycles

18 **CENTRIFUGE**

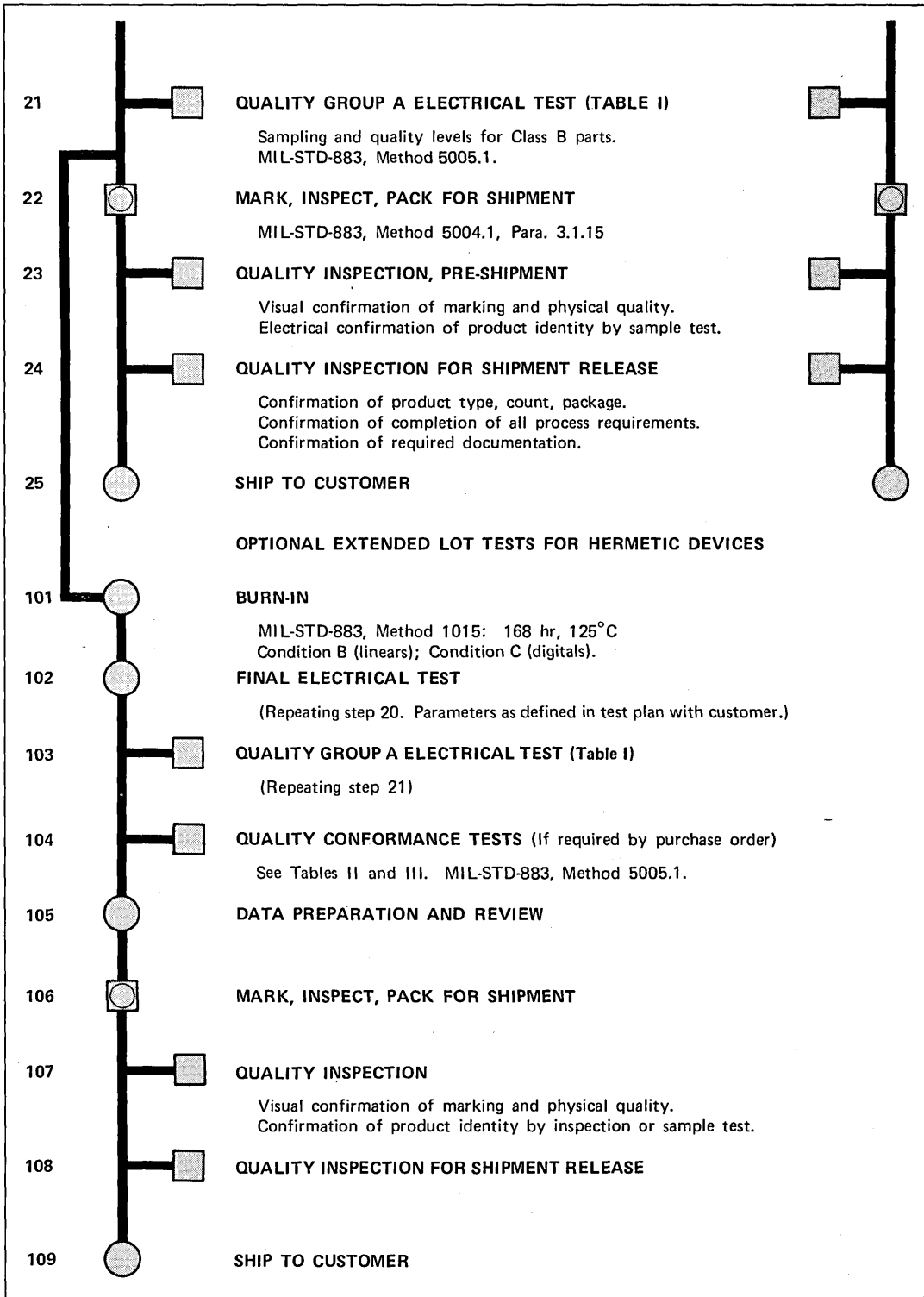
MIL-STD-883, Method 2001, Cond. E: 30,000 G

19 **HERMETICITY**

MIL-STD-883, Method 1014, Cond. A: Fine Leak
MIL-STD-883, Method 1014, Cond. C2: Gross Leak

20 **ELECTRICAL TEST**

MIL-STD-883, Method 5004.1, Para. 3.1.1.2: Static, dynamic, functional tests at 25°C.



21 **QUALITY GROUP A ELECTRICAL TEST (TABLE I)**

Sampling and quality levels for Class B parts.
MIL-STD-883, Method 5005.1.

22 **MARK, INSPECT, PACK FOR SHIPMENT**

MIL-STD-883, Method 5004.1, Para. 3.1.15

23 **QUALITY INSPECTION, PRE-SHIPMENT**

Visual confirmation of marking and physical quality.
Electrical confirmation of product identity by sample test.

24 **QUALITY INSPECTION FOR SHIPMENT RELEASE**

Confirmation of product type, count, package.
Confirmation of completion of all process requirements.
Confirmation of required documentation.

25 **SHIP TO CUSTOMER**

OPTIONAL EXTENDED LOT TESTS FOR HERMETIC DEVICES

101 **BURN-IN**

MIL-STD-883, Method 1015: 168 hr, 125°C
Condition B (linears); Condition C (digitals).

102 **FINAL ELECTRICAL TEST**

(Repeating step 20. Parameters as defined in test plan with customer.)

103 **QUALITY GROUP A ELECTRICAL TEST (Table I)**

(Repeating step 21)

104 **QUALITY CONFORMANCE TESTS** (If required by purchase order)

See Tables II and III. MIL-STD-883, Method 5005.1.

105 **DATA PREPARATION AND REVIEW**

106 **MARK, INSPECT, PACK FOR SHIPMENT**

107 **QUALITY INSPECTION**

Visual confirmation of marking and physical quality.
Confirmation of product identity by inspection or sample test.

108 **QUALITY INSPECTION FOR SHIPMENT RELEASE**

109 **SHIP TO CUSTOMER**

QUALIFICATION AND QUALITY CONFORMANCE INSPECTION

Subgroups and LTPD levels as given in MIL-STD-883, Method 5005.1, for Class B parts

Table I. Group A Electrical Tests

Subgroups	LTPD	Initial Sample Size*
Subgroup 1 — Static tests at 25°C	5	45
Subgroup 2 — Static tests at maximum rated operating temperature	7	32
Subgroup 3 — Static tests at minimum rated operating temperature	7	32
Subgroup 4 — Dynamic tests at 25°C	5	45
Subgroup 5 — Dynamic tests at maximum rated operating temperature	7	32
Subgroup 6 — Dynamic tests at minimum rated operating temperature	7	32
Subgroup 7 — Functional tests at 25°C	5	45
Subgroup 8 — Functional tests at maximum and minimum rated operating temperatures	10	22
Subgroup 9 — Switching tests at 25°C	7	32

Table II. Group B Tests

Test	Method	Conditions	LTPD	Initial Sample Size*
Subgroup 1 Physical dimensions	2008	Test Condition A	15	15
Subgroup 2 a) Marking permanency	2008	Test Condition B: trichloroethylene and alcohol/Freon solvents	4 devices no failures	
b) Visual and mechanical	2008	Test Condition B	1 device no failures	
c) Bond strength	2011	Test Condition D: 1 gram force minimum for aluminum wire, ultrasonic bonding	15	15 leads
Subgroup 3 Solderability	2003	Soldering Temp of 260°C ±10°C. 95% coverage, void concentration not to exceed 5% of area	15	15
Subgroup 4 a) Lead fatigue	2004	Test Condition B_2: 3 oz. for ribbon leads; 8 oz. for all others.	15	15
b) Hermeticity 1. Fine leak 2. Gross leak	1014 1014	Cond A Helium Tracer Gas 5×10^{-8} atm cc/sec Cond C Fluorcarbon Detection 10^{-5} atm cc/sec		

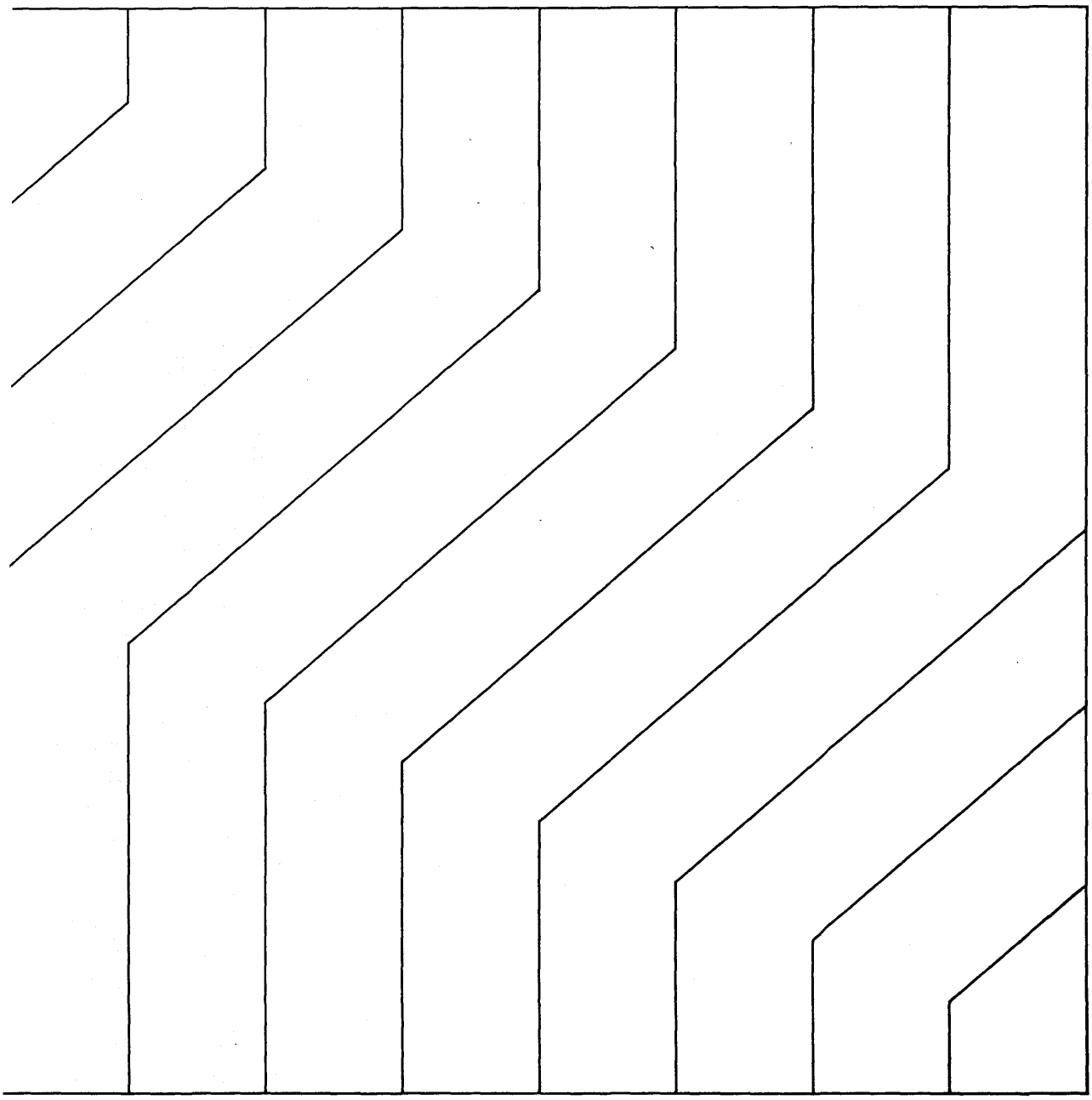
Table III. Group C tests

Test	Method	Conditions	LTPD	Initial Sample Size*
Subgroup 1				
a) Thermal shock	1011	Test Method B: liquid to liquid, 125°C to −55°C , 15 cycles		
b) Temperature cycling	1010	Test Condition C: air to air, −65°C to +150°C, 10 cycles	15	15
c) Moisture resistance	1004	Omit initial conditioning and vibration		
d) Seal (fine and gross)	1014	Helium and fluorocarbon tests		
Subgroup 2				
a) Mechanical shock	2002	Test Condition B: 5 shock pulses; 6 directions; 1,500 G		
b) Vibration variable frequency	2007	Test Condition A: 20 Hz-2 KHz; 20 G, X, Y, Z orientation	15	15
c) Constant acceleration (Centrifuge)	2001	Test Condition E: 30 KG centrifugal acceleration		
d) Seal (fine and gross)	1014	Helium and fluorocarbon tests		
Subgroup 3				
Salt atmosphere (corrosion)	1009	Test Condition A: 24 hr	15	15
Subgroup 4				
High temperature storage	1008	Test Condition C: 1,000 hr, 150°C	7	55 Acc = 1*
Subgroup 5				
Operating life test	1005	Steady state power: 1000 hr, 125°C. Digital devices: Test Condition C Linear devices: Test Condition B	5	77 Acc = 1*

* Groups A, B and C sampling plans are based on standard LTPD tables of MIL-M-38510. The smallest sample size, based on zero rejects allowed, has been chosen unless otherwise indicated. If necessary, the sample size will be increased once to the quantity corresponding to an acceptance number of 3 for Group A and 2 for Groups B and C.

End point electrical parameters, where required, are room temperature Group A DC or functional tests as specified for the device under test.

TTL/MSI



Am2502/2503/2504

Eight-Bit/Twelve-Bit Successive Approximation Registers

Distinctive Characteristics

- Contains all the storage and control for successive approximation A-to-D converters.
- Provision for register extension or truncation.
- Can be operated in START-STOP or continuous conversion mode.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Can be used as serial-to-parallel converter or ring counters.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

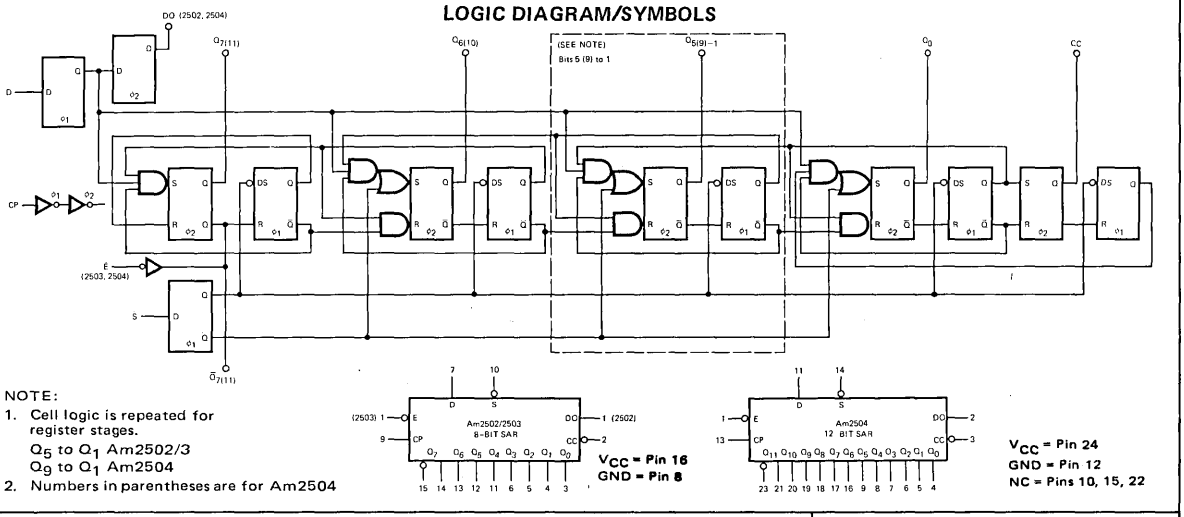
The Am2502, Am2503 and Am2504 are 8-bit and 12-bit TTL Successive Approximation Registers. The registers contain all the digital control and storage necessary for successive approximation analog-to-digital conversion. They can also be used in digital systems as the control and storage element in recursive digital routines.

The registers consist of a set of master latches that act as the control elements in the device and change state when the input clock is LOW, and a set of slave latches that hold the register data and change on the input clock LOW-to-HIGH transition. Externally the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the DO output on the Am2502 and Am2504 when the clock goes from LOW-to-HIGH. There are no restrictions on the data input; it can change state at any time except during the set-up time just prior to the clock transition. At the same time that data enters the register bit the next less significant bit is set to a LOW ready for the next iteration.

The register is reset by holding the $\overline{S}$ (Start) signal LOW during the clock LOW-to-HIGH transition. The register synchronously resets to the state $Q_7(11)$ LOW, (Note 2) and all the remaining register outputs HIGH. The $\overline{CC}$ (Conversion Complete) signal is also set HIGH at this time. The $\overline{S}$ signal should not be brought back HIGH until after the clock LOW-to-HIGH transition in order to guarantee correct resetting. After the clock has gone HIGH resetting the register, the $\overline{S}$ signal is removed. On the next clock LOW-to-HIGH transition the data on the D input is set into the $Q_7(11)$ register bit and the $Q_6(10)$ register bit is set to a LOW ready for the next clock cycle. On the next clock LOW-to-HIGH transition data enters the $Q_6(10)$ register bit and $Q_5(9)$ is set to a LOW. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q_0, the $\overline{CC}$ signal goes LOW, and the register is inhibited from further change until reset by a Start signal.

In order to allow complementary conversion the complementary output of the most significant register bit is made available. An active LOW enable input, $\overline{E}$, on the Am2503 and Am2504 allows devices to be connected together to form a longer register by connecting the clock, D, and $\overline{S}$ inputs together and connecting the $\overline{CC}$ output of one device to the $\overline{E}$ input of the next less significant device. When the Start signal resets the register, the $\overline{E}$ signal goes HIGH, forcing the $Q_7(11)$ bit HIGH and inhibiting the device from accepting data until the previous device is full and its $\overline{CC}$ goes LOW. If only one device is used the $\overline{E}$ input should be held at a LOW logic level (Ground). If all the bits are not required, the register may be truncated and conversion time saved by using a register output going LOW rather than the $\overline{CC}$ signal to indicate the end of conversion.

LOGIC DIAGRAM/SYMBOLS



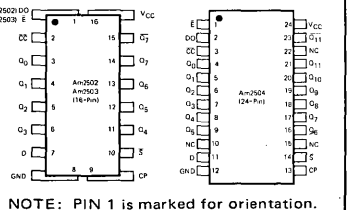
NOTE:
1. Cell logic is repeated for register stages.
   Q_5 to Q_1 Am2502/3
   Q_9 to Q_1 Am2504
2. Numbers in parentheses are for Am2504

ORDERING INFORMATION

Package Type	Temperature Range	Am2502 Order Number	Am2503 Order Number	Am2504 Order Number
Molded DIP	0°C to +75°C	AM2502PC	AM2503PC	AM2504PC
Hermetic DIP	0°C to +75°C	AM2502DC	AM2503DC	AM2504DC
Hermetic DIP	−55°C to +125°C	AM2502DM	AM2503DM	AM2504DM
Hermetic Flat Pak	−55°C to +125°C	AM2502FM	AM2503FM	AM2504FM
Dice	Note	AM2502XX	AM2503XX	AM2504XX

NOTE: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAMS
Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

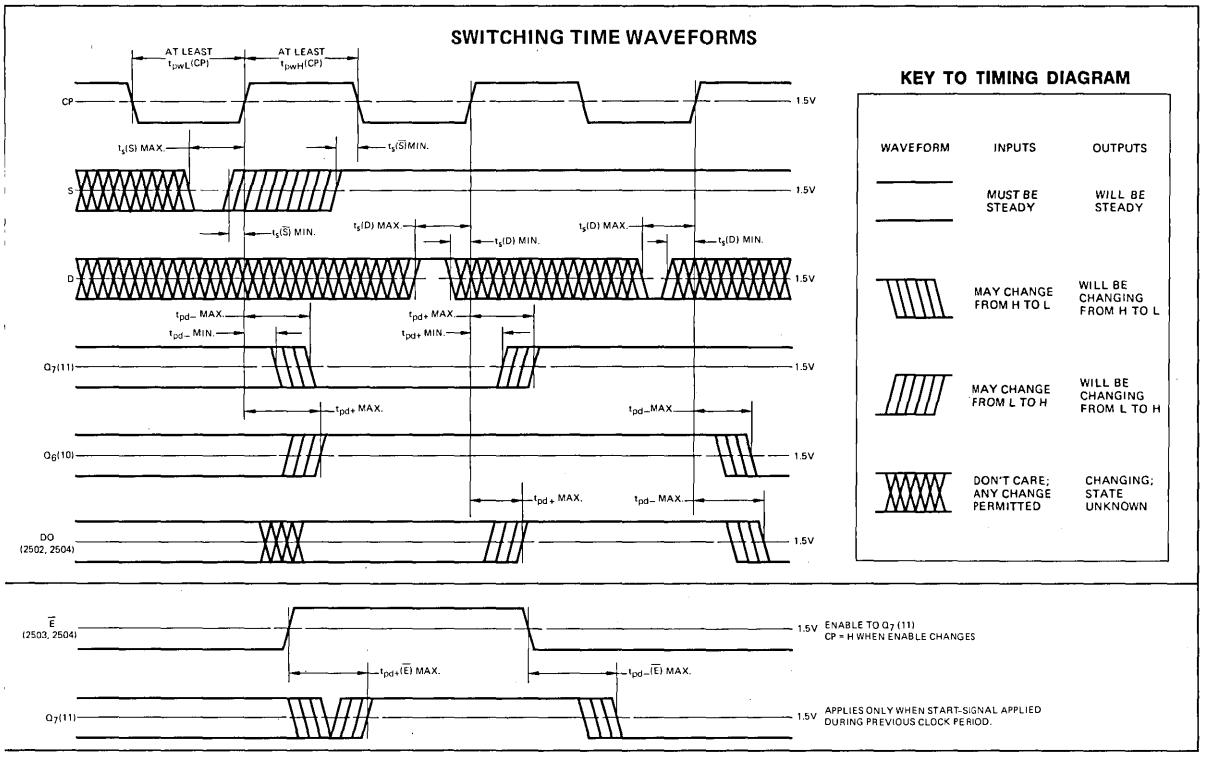
Am2502XC Am2503XC Am2504XC T_A = 0°C to +75°C V_{CC} = 5.0V ±5%
Am2502XM Am2503XM Am2504XM T_A = −55°C to +125°C V_{CC} = 5.0V ±10%

Parameters	Description	Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.48mA V_{IN} = V_{IH} or V_{IL}			2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 9.6mA V_{IN} = V_{IH} or V_{IL}				0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V				−1.0	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V				6.0	40	µA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V			−10	−25	−45	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.	Am2502	XM		65	85	mA
				XC		65	95	
			Am2503	XM		60	80	mA
				XC		60	90	
			Am2504	XM		90	110	mA
				XC		90	124	

Note 1. Typical Limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. Actual input currents are obtained by multiplying unit load current by input load factor (See Loading Rules).

Switching Characteristics T_A = 25°C, V_{CC} = 5.0V, C_L = 15pF

Parameters	Description		Min.	Typ.	Max.	Units
t_{pd+}	Turn Off Delay CP to Output HIGH		10	26	38	ns
t_{pd-}	Turn On Delay CP to Output LOW		10	18	28	ns
t_s(D)	Set-up Time Data Input		−10	4	8	ns
t_s(S)	Set-up Time Start Input		0	9	16	ns
t_{pd+}(E)	Turn Off Delay E to Q_7(11) HIGH	(Am2503/4) C_P = H, $\overline{S}$ = L		13	19	ns
t_{pd-}(E)	Turn On Delay E to Q_7(11) LOW			16	24	ns
t_{pwL}(CP)	Minimum LOW Clock Pulse Width			28	46	ns
t_{pwH}(CP)	Minimum HIGH Clock Pulse Width			12	20	ns
f_{max}	Maximum Clock Frequency		15	25		MHz



DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output

FUNCTIONAL TERMS:

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

Input Unit Load One T^2 L gate input load. In the HIGH state it is equal to I_{IH} and in the LOW state it is equal to I_{IL}.

CP The clock input of the register.

$\overline{CC}$ The conversion complete output. This output remains HIGH during a conversion and goes LOW when a conversion is complete.

D The serial data input of the register.

$\overline{E}$ The register enable. This input is used to expand the length of the register and when HIGH forces the $Q_7(11)$ register output HIGH and inhibits conversion. When not used for expansion the enable is held at a LOW logic level (Ground).

$Q_7(11)$ The true output of the MSB of the register.

$\overline{Q_7}(11)$ The complement output of the MSB of the register.

Q_i i = 7(11) to 0 The outputs of the register.

$\overline{S}$ The start input. If the start input is held LOW for at least a clock period the register will be reset to $Q_7(11)$ LOW and all the remaining outputs HIGH. A start pulse that is LOW for a shorter period of time can be used if it meets the set-up time requirements of the $\overline{S}$ input.

DO The serial data output. (The D input delayed one bit).

OPERATIONAL TERMS:

I_{IL} Forward input load current.

I_{OH} Output HIGH current, forced out of output V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{IH} Reverse input load current.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} flowing into output.

SWITCHING TERMS: (Measured at the 1.5V logic level).

t_{pd-} The propagation delay from the clock signal LOW-HIGH transition to an output signal HIGH-LOW transition.

t_{pd+} The propagation delay from the clock signal LOW-HIGH transition to an output signal LOW-HIGH transition.

$t_{pd-}(\overline{E})$ The propagation delay from the Enable signal HIGH-LOW transition to the $Q_7(11)$ output signal HIGH-LOW transition.

$t_{pd+}(\overline{E})$ The propagation delay from the Enable signal LOW-HIGH transition to $Q_7(11)$ output signal LOW-HIGH transition.

$t_s(D)$ Set-up time required for the logic level to be present at the data input prior to the clock transition from LOW to HIGH in order for the register to respond. The data input should remain steady between t_s max. and t_s min. before the clock.

$t_s(\overline{S})$ Set-up time required for a LOW level to be present at the $\overline{S}$ input prior to the clock transition from LOW to HIGH in order for the register to be reset, or time required for a HIGH level to be present on S before the HIGH to LOW clock transition to prevent resetting.

$t_{pw}(CP)$ The minimum clock pulse width (LOW or HIGH) required for proper register operation.

Am2502/3 TRUTH TABLE

Time	Inputs			Outputs									
t_n	D	$\overline{S}$	$\overline{E}$	D_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	$\overline{CC}$
0	X	L	L	X	X	X	X	X	X	X	X	X	X
1	D_7	H	L	X	L	H	H	H	H	H	H	H	H
2	D_6	H	L	D_7	D_7	L	H	H	H	H	H	H	H
3	D_5	H	L	D_6	D_7	D_6	L	H	H	H	H	H	H
4	D_4	H	L	D_5	D_7	D_6	D_5	L	H	H	H	H	H
5	D_3	H	L	D_4	D_7	D_6	D_5	D_4	L	H	H	H	H
6	D_2	H	L	D_3	D_7	D_6	D_5	D_4	D_3	L	H	H	H
7	D_1	H	L	D_2	D_7	D_6	D_5	D_4	D_3	D_2	L	H	H
8	D_0	H	L	D_1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	L	H
9	X	H	L	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
10	X	X	L	X	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC

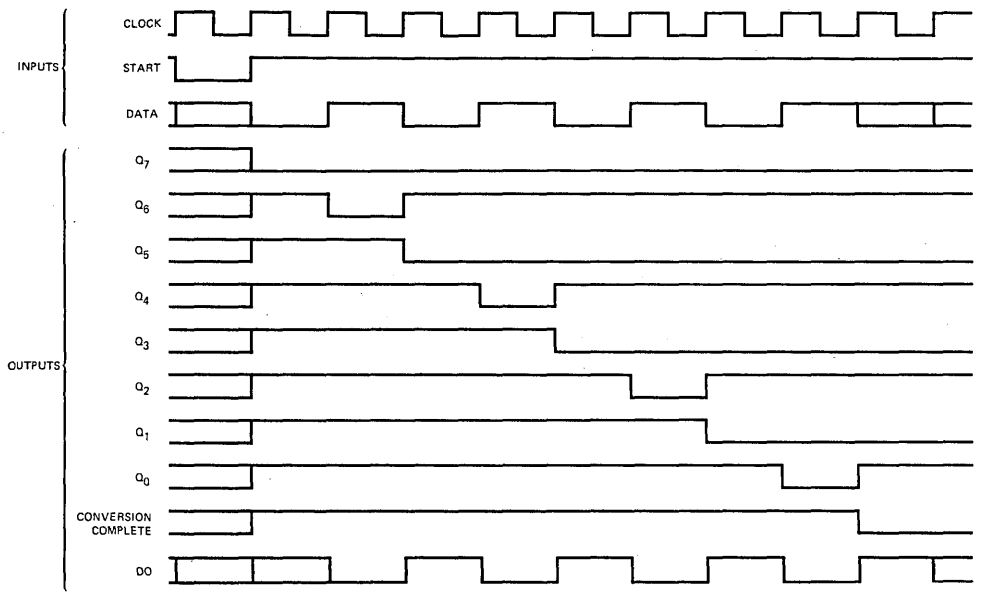
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
NC = No Change

Note: Truth Table for Am2504 is extended to include 12 outputs.

USER NOTES FOR A/D CONVERSION

1. The register can be used with either current switches that require a low voltage level to turn the switch on, or current switches that require a high voltage level to turn the current switch on. If current switches are used which turn on with a low logic level the resulting digital output from the register is active LOW. That is, a logic "1" is represented as a low voltage level. If current switches are used that turn on with a high logic level then the digital output is active HIGH; a logic "1" is represented as a high voltage level.
2. For a maximum digital error of ±½LSB the comparator must be biased. If current switches that require a high voltage level to turn on are used, the comparator should be biased +½LSB and if the current switches require a high logic level to turn on then the comparator must be biased −½LSB.
3. The register, by suitable selection of resistor ladder network, can be used to perform either binary or BCD conversion.
4. The register can be used to perform 2's complement conversion by offsetting the comparator ½ full range +½ LSB and using the complement of the MSB Q_7 (11) as the sign bit.
5. If the register is truncated and operated in the continuous conversion mode a lock-up condition may occur on power-on. This situation can be overcome by making the START input the OR function of $\overline{CC}$ and the appropriate register output.

Am2502/3 TIMING CHART



Am2502/3 LOADING RULES (IN UNIT LOADS)

Input/Output	Pin No.'s	Input Unit Load LOW	Input Unit Load HIGH	Fanout Output HIGH	Fanout Output LOW
$\overline{E}$ (2503)	1	2	2	–	–
DO (2502)	1	–	–	12	6
$\overline{CC}$	2	–	–	12	6
Q_0	3	–	–	12	6
Q_1	4	–	–	12	6
Q_2	5	–	–	12	6
Q_3	6	–	–	12	6
D	7	2	2	–	–
GND	8	–	–	–	–
CP	9	1	1	–	–
$\overline{S}$	10	1	2	–	–
Q_4	11	–	–	12	6
Q_5	12	–	–	12	6
Q_6	13	–	–	12	6
Q_7	14	–	–	12	6
$\overline{Q_7}$	15	–	–	12	6
V_{CC}	16	–	–	–	–

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	Equivalent Input Unit Load LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
Advanced Micro Devices 54/7400	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

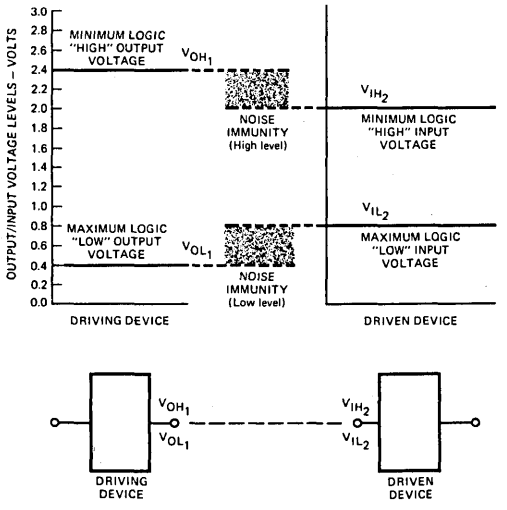
Am2504 LOADING RULES (IN UNIT LOADS)

Input/Output	Pin No.'s	Input Unit Load LOW	Input Unit Load HIGH	Fanout Output HIGH	Fanout Output LOW
$\overline{E}$	1	2	2	–	–
DO	2	–	–	12	6
$\overline{CC}$	3	–	–	12	6
Q_0	4	–	–	12	6
Q_1	5	–	–	12	6
Q_2	6	–	–	12	6
Q_3	7	–	–	12	6
Q_4	8	–	–	12	6
Q_5	9	–	–	12	6
NC	10	–	–	–	–
D	11	2	2	–	–
GND	12	–	–	–	–
CP	13	1	1	–	–
$\overline{S}$	14	1	2	–	–
NC	15	–	–	–	–
Q_6	16	–	–	12	6
Q_7	17	–	–	12	6
Q_8	18	–	–	12	6
Q_9	19	–	–	12	6
Q_{10}	20	–	–	12	6
Q_{11}	21	–	–	12	6
NC	22	–	–	–	–
$\overline{Q_{11}}$	23	–	–	12	6
V_{CC}	24	–	–	–	–

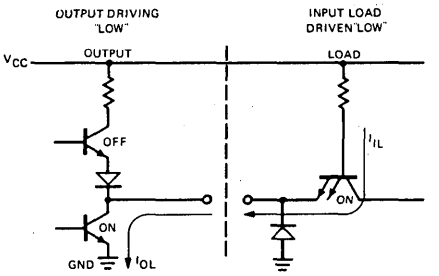
NC = No Connection

INPUT/OUTPUT INTERFACE CONDITIONS

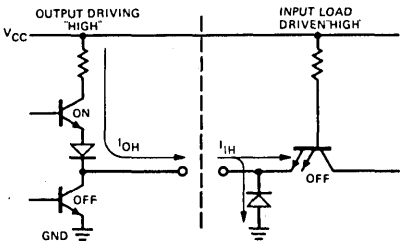
Voltage Interface Conditions – LOW & HIGH



Current Interface Conditions – LOW

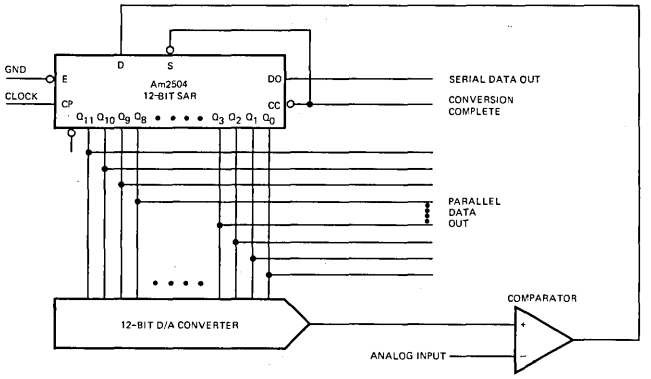


Current Interface Conditions – HIGH



Am2502/3/4 APPLICATION

Continuous Conversion Analog-to-Digital Converter

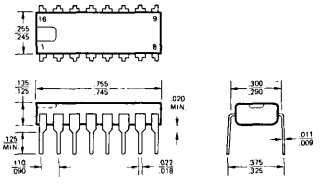


This shows how the Am2502/3/4 registers are used with a Digital-to-Analog converter and a comparator to form a very high-speed continuous conversion Analog-to-Digital converter. Conversion time is limited mainly by the speed of the D/A converter and comparator with typical conversion rates of 100,000 conversions per second.

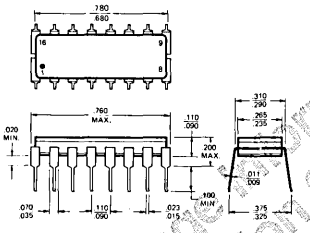
PHYSICAL DIMENSIONS

Am2502/3

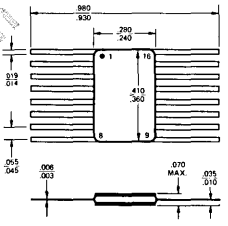
16-Pin Molded DIP



16-Pin Hermetic DIP

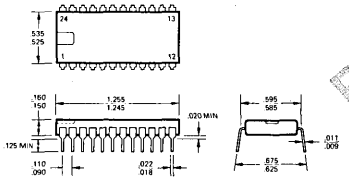


16-Pin Flat Pak

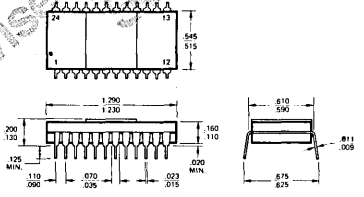


Am2504

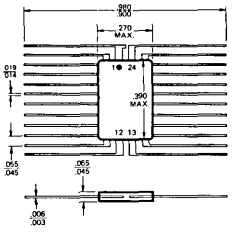
24-Pin Molded DIP



24-Pin Hermetic DIP

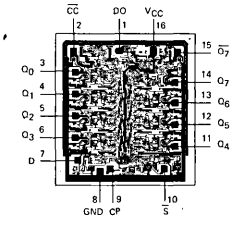


24-Pin Flat Pak



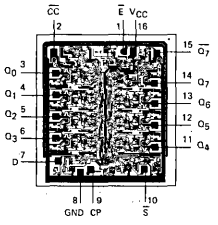
Metallization and Pad Layout

Am2502



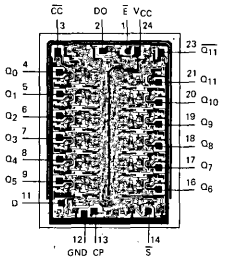
DIE SIZE 0.087" x 0.096"

Am2503



DIE SIZE 0.087" x 0.096"

Am2504



DIE SIZE 0.087" x 0.124"

ADVANCED MICRO DEVICES INC.
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Am25L02/25L03/25L04

Low-Power, Eight-Bit/Twelve-Bit Successive Approximation Registers

Distinctive Characteristics

- Contains all the storage and control for successive approximation A-to-D converters.
- Can be operated in START-STOP or continuous conversion mode.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Can be used as serial-to-parallel converter or ring counters.

FUNCTIONAL DESCRIPTION

The Am25L02, Am25L03 and Am25L04 are 8-bit and 12-bit TTL Successive Approximation Registers. The registers contain all the digital control and storage necessary for successive approximation analog-to-digital conversion. They can also be used in digital systems as the control and storage element in recursive digital routines.

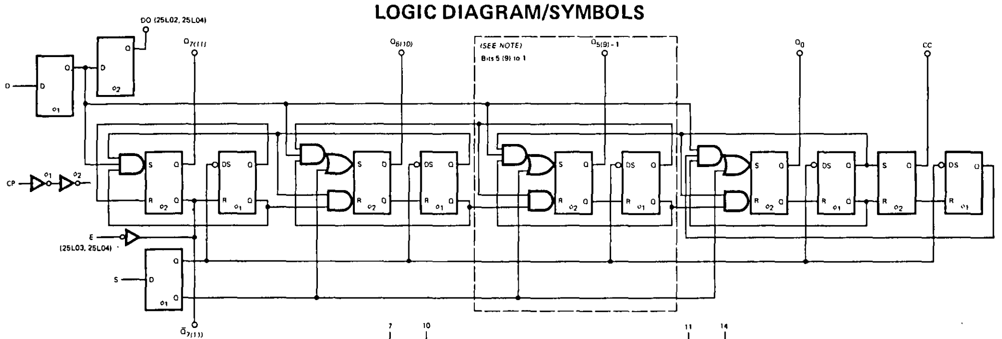
The registers consist of a set of master latches that act as the control elements in the device and change state when the input clock is LOW, and a set of slave latches that hold the register data and change on the input clock LOW-to-HIGH transition. Externally the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the DO output on the Am25L02 and Am25L04 when the clock goes from LOW-to-HIGH. There are no restrictions on the data input; it can change state at any time except during the set-up time just prior to the clock transition. At the same time that data enters the register bit the next less significant bit is set to a LOW ready for the next iteration.

The register is reset by holding the $\overline{S}$ (Start) signal LOW during the clock LOW-to-HIGH transition. The register synchronously resets to the state $Q_7(11)$ LOW, (Note 2) and all the remaining register outputs HIGH. The $\overline{CC}$ (Conversion Complete) signal is also set HIGH at this time. The $\overline{S}$ signal should not be brought back HIGH until after the clock LOW-to-HIGH transition in order to guarantee correct resetting.

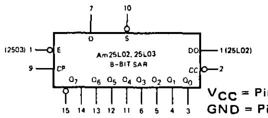
After the clock has gone HIGH resetting the register, the $\overline{S}$ signal is removed. On the next clock LOW-to-HIGH transition the data on the D input is set into the $Q_7(11)$ register bit and the $Q_6(10)$ register bit is set to a LOW ready for the next clock cycle. On the next clock LOW-to-HIGH transition data enters the $Q_6(10)$ register bit and $Q_5(9)$ is set to a LOW. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q_0, the $\overline{CC}$ signal goes LOW, and the register is inhibited from further change until reset by a Start signal.

In order to allow complementary conversion the complementary output of the most significant register bit is made available. An active LOW enable input, $\overline{E}$, on the Am25L03 and Am25L04 allows devices to be connected together to form a longer register by connecting the clock, D, and $\overline{S}$ inputs together and connecting the $\overline{CC}$ output of one device to the $\overline{E}$ input of the next less significant device. When the Start signal resets the register, the E signal goes HIGH, forcing the $Q_7(11)$ bit HIGH and inhibiting the device from accepting data until the previous device is full and its $\overline{CC}$ goes LOW. If only one device is used the $\overline{E}$ input should be held at a LOW logic level (Ground). For continuous conversion the $\overline{CC}$ output is connected to the $\overline{S}$ input so that the device automatically restarts at the end of a conversion. If all the bits are not required, the register may be truncated and conversion time saved by using a register output going LOW rather than the $\overline{CC}$ signal to indicate the end of conversion.

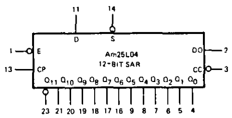
LOGIC DIAGRAM/SYMBOLS



NOTE:
1. Cell logic is repeated for register stages. Q_5 to Q_1 Am25L02/3; Q_9 to Q_1 Am25L04
2. Numbers in parentheses are for Am25L04



V_{CC} = Pin 16
GND = Pin 8



V_{CC} = Pin 24
GND = Pin 12
NC = Pins 10, 15, 22

ORDERING INFORMATION

Package Type	Temperature Range	Am25L02 Order Number	Am25L03 Order Number	Am25L04 Order Number
Molded DIP	0°C to +75°C	AM25L02PC	AM25L03PC	AM25L04PC
Hermetic DIP	0°C to +75°C	AM25L02DC	AM25L03DC	AM25L04DC
Hermetic DIP	−55°C to +125°C	AM25L02DM	AM25L03DM	AM25L04DM
Hermetic Flat Pak	−55°C to +125°C	AM25L02FM	AM25L03FM	AM25L04FM
Dice	Note	AM25L02XX	AM25L03XX	AM25L04XX

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

LOADING RULES

In Unit Loads (Notes)

Input Load Factor	TTL LOADS HIGH	TTL LOADS LOW	25L, 93L LOADS HIGH	25L, 93L LOADS LOW
CP	0.5	0.25	1.0	1.0
$\overline{E}$, D, $\overline{S}$	1.0	0.5	2.0	2.0
Output Drive	**HIGH**	**LOW**	**HIGH**	**LOW**
All Outputs	10	3	20	12

Notes 1. A TTL unit load is specified as 0.4V at −1.6mA LOW, 2.4V at 40μA HIGH.
2. A 25L, 93L unit load is specified as 0.3V at −400μA LOW, 2.4V at 20μA HIGH.
3. Enough output LOW current is available to mix TTL and 25L, 93L loads and still meet the 25L, 93L requirement of a V_{OL} of 0.3V.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am25L02XC Am25L03XC Am25L04XC T_A = 0°C to +75°C V_{CC} = 5.0V ±5%
Am25L02XM Am25L03XM Am25L04XM T_A = −55°C to +125°C V_{CC} = 5.0V ±10%

Parameters	Description	Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.4mA V_{IN} = V_{IH} or V_{IL}			2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 4.92mA V_{IN} = V_{IH} or V_{IL}				0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.7	Volts
I_{IL} (Note 2)	25L, 93L Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.3V				−0.25	−0.4	mA
I_{IH} (Note 2)	25L, 93L Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V				2.0	20	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V			3	7	16	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.	Am25L02	XM		25	33	mA
				XC		25	35	
			Am25L03	XM		22	31	mA
				XC		22	33	
			Am25L04	XM		30	42	mA
				XC		30	45	

Note 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
Note 2. Actual input currents are obtained by multiplying unit load current by the 25L, 93L input load factor. (See loading rules)

Switching Characteristics (T_A = 25°C, V_{CC} = 5.0V, C_L = 15pF)

Parameters	Description		Min.	Typ.	Max.	Units
t_{pd+}	Turn Off Delay CP to Output HIGH		30	95	140	ns
t_{pd-}	Turn On Delay CP to Output LOW		20	70	100	ns
t_s(D)	Set-up Time Data Input		−15	4	20	ns
$t_s(\overline{S})$	Set-up Time Start Input		0	6	25	ns
$t_{pd+}(\overline{E})$	Turn Off Delay $\overline{E}$ to Q_7(11) HIGH	(Am25L03/4)		50	75	ns
$t_{pd-}(\overline{E})$	Turn On Delay $\overline{E}$ to Q_7(11) LOW	Cp = H, $\overline{S}$ = L		50	75	ns
t_{pwL}(CP)	Minimum LOW Clock Pulse Width			130	180	ns
t_{pwH}(CP)	Minimum HIGH Clock Pulse Width			70	100	ns
f_{max}	Maximum Clock Frequency		3.5	5		MHz

Am2505

Four-Bit by Two-Bit 2's Complement Multiplier

istinctive Characteristics:

Provides 2's complement multiplication at high speed without correction.

Can be used in an iterative scheme or time sequenced mode.

Multiplies two 12-bit signed numbers in typically 175ns.

- Multiplies in active HIGH (positive logic) or active LOW (negative logic) representations.
- Easy correction for unsigned, sign-magnitude or 1's complement multiplication.
- 100% reliability assurance testing in compliance with MIL STD 883.

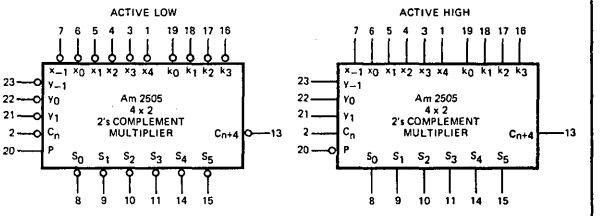
FUNCTIONAL DESCRIPTION:

The Am2505 is a high-speed digital multiplier that can multiply numbers represented in the 2's complement notation and produce a 2's complement product without correction. The device consists of a 4x2 multiplier that can be connected to form iterative arrays able to multiply numbers either directly, or in a time sequenced arrangement. The device assumes that the most significant digit in a word carries a negative weight, and can therefore be used in arrays where the multiplicand and multiplier have different word lengths. The multiplier uses the quaternary algorithm and performs the function S = XY + K where K is the input field used to add partial products generated in the array. At the beginning of the array the K inputs are available to add a signed constant to the least significant part of the product. Multiplication of an m bit number by an n bit number in an array results in a product having m+n bits so that all possible combinations of product are accounted for. If a conventional 2's complement product is required the most significant bit can be ignored, and overflow conditions can be detected by comparing the last two product digits.

Figure 2 shows how multipliers are connected together in an array. A number of connection schemes are possible. Figure 4 shows diagramatically the connection scheme that results in the fastest multiply. If higher speed is required an array can be split into several parts, and the parts added with high-speed look-ahead carry adders such as the Am9340.

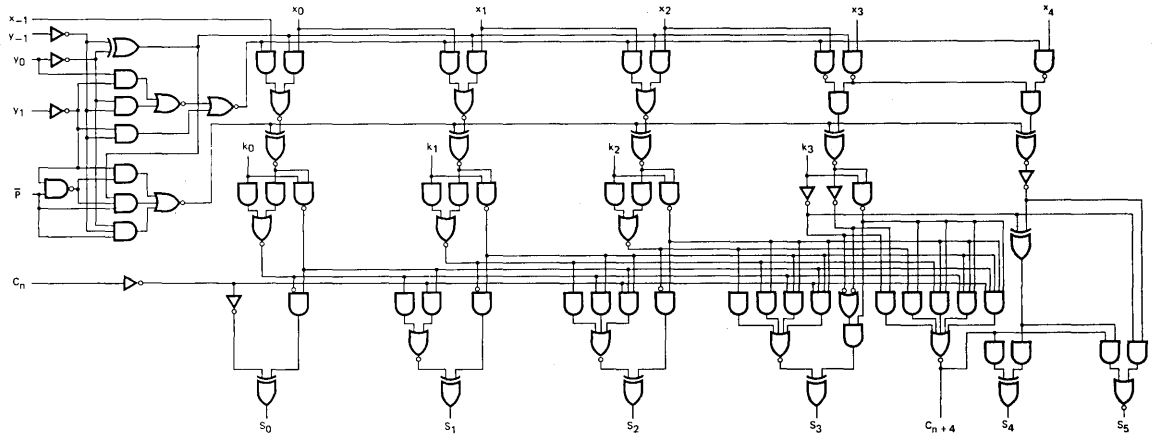
Provision is made in the design for multiplication in the active high (positive logic) or active low (negative logic) representations simply by reinterpreting the active level of the input operands, the product, and a polarity control P. For a more complete description and applications the user is referred to the Am2505 Application Note.

LOGIC SYMBOLS



V_{CC} = PIN 24
GND = PIN 12

LOGIC DIAGRAM

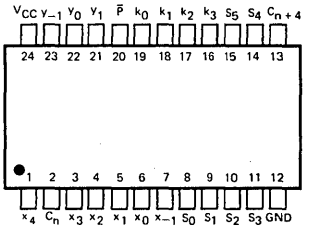


Am2505 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	AM250559C
Hermetic DIP	0°C to +75°C	AM250559G
Hermetic DIP	−55°C to +125°C	AM250551G
Hermetic Flat Pak	−55°C to +125°C	AM250551P
Dice	Note	AM2505XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5 V to +7
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} ma
DC Input Voltage	−0.5 V to +5.5
Output Current, Into Outputs	30 m
DC Input Current	−30 mA to +5 m

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am250559X — T_A = 0°C to +75°C V_{CC} = 4.75 V to 5.25 V
Am250551X — T_A = −55°C to +125°C V_{CC} = 4.50 V to 5.50 V

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.48 mA V_{IN} = V_{IH} or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 9.6 mA V_{IN} = V_{IH} or V_{IL}		0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V		−1.1	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V		4.0	40	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V	20	40	85	mA
I_{CC}	Power Supply Current Am250551X	V_{CC} = MAX., Y_i = 0 V		90	130	mA
I_{CC}	Power Supply Current Am250559X	V_{CC} = MAX., Y_i = 0 V		90	145	mA

Notes: 1 Typical Limits are at V_{CC} = 5.0 V, 25°C Ambient and maximum loading.
2 Actual Input currents are obtained by multiplying unit load current by the input load factor. (See loading rules)

SWITCHING CHARACTERISTICS V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF

Parameters	From (Input)	To (Output)	Test Conditions	Min	Typ	Max	Units
t_{pd+} t_{pd-}	C_n	C_{n+4}	See Test Table	6 7	13 14	20 21	ns
t_{pd+} t_{pd-}	C_n	$S_{0,1,2,3}$	See Test Table	9 7	18 15	27 23	ns
t_{pd+} t_{pd-}	C_n	$S_{4,5}$	See Test Table	11 8	22 17	31 26	ns
t_{pd+} t_{pd-}	Any k	C_{n+4}	See Test Table	6 7	12 15	18 23	ns
t_{pd+} t_{pd-}	Any k	$S_{0,1,2,3}$	See Test Table	9 7	18 15	27 23	ns
t_{pd+} t_{pd-}	Any k	$S_{4,5}$	See Test Table	5 4	22 21	31 30	ns
t_{pd+} t_{pd-}	Any x	C_{n+4}	See Test Table	10 11	20 22	30 31	ns
t_{pd+} t_{pd-}	Any x	$S_{0,1,2,3}$	See Test Table	13 12	26 24	37 38	ns
t_{pd+} t_{pd-}	Any x	$S_{4,5}$	See Test Table	16 10	32 27	45 38	ns
t_{pd+} t_{pd-}	Any y	C_{n+4}	See Test Table	14 19	28 38	39 53	ns
t_{pd+} t_{pd-}	Any y	$S_{0,1,2,3}$	See Test Table	20 14	41 29	58 41	ns
t_{pd+} t_{pd-}	Any y	$S_{4,5}$	See Test Table	22 16	45 32	63 45	ns

SWITCHING TIME TEST TABLE

Input	Outputs	Inputs at 0V (remaining inputs at 4.5V)
C_n	C_{n+4}, S_{0123}, S_{45}	P, Y_{-1}, Y_1, All X
k_0	C_{n+4}, S_{0123}, S_{45}	P, Y_{-1}, Y_1, All X
k_1	C_{n+4}, S_{123}, S_{45}	P, Y_{-1}, Y_1, All X
k_2	C_{n+4}, S_{23}, S_{45}	P, Y_{-1}, Y_1, All X
k_3	S_3	P, Y_{-1}, Y_1, All X
k_3	S_{45}	P, Y_{-1}, Y_1, All X, C_n
x_{-1}	C_{n+4}, S_{0123}, S_{45}	P, Y_1, All k
x_0	C_{n+4}, S_{0123}, S_{45}	P, Y_{-1}, Y_1, All k
x_1	C_{n+4}, S_{123}, S_{45}	P, Y_{-1}, Y_1, All k
x_2	C_{n+4}, S_{23}, S_{45}	P, Y_{-1}, Y_1, All k
x_3	S_3	P, Y_{-1}, Y_1, All k
x_3	S_{45}	P, Y_{-1}, Y_1, All k, C_n
x_4	S_{45}	P, Y_1, All k, C_n
y_{-1}	C_{n+4}, S_{0123}, S_{45}	P, X_1, X_2, X_3, X_4, All k
y_0	C_{n+4}, S_{0123}, S_{45}	P, X_1, X_2, X_3, X_4, All k
y_1	C_{n+4}, S_{0123}, S_{45}	X_0, X_1, X_2, X_3, X_4, All k

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS

C_n The carry input to the high-speed adder.

C_{n+4} The carry output from the high-speed adder.

k_i The constant field used for accumulating partial products. i=0, 1, 2, 3. At the beginning of the array the K field can be used to add a 2's complement number to the least significant half of the double length product.

$\overline{P}$ The polarity control input. This input must be at a low-logic level for numbers in the active high logic representation, and held high for numbers in the active low logic representation.

S_i The product outputs. i = 0,1,2,3,4,5.

x_i The multiplicand inputs. i = −1, 0, 1, 2, 3, 4. At the first column of the array x_{-1} must be held at logic '0', and at the last column of the array x_4 is connected to x_3.

y_i The multiplier inputs. i = −1, 0, 1.
At the first row of the array y_{-1} must be held at logic '0'.

OPERATIONAL TERMS:

I_{IL} Forward input load current.

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{CC} The current drawn by the device from V_{CC} power supply with input and output terminals open.

I_{IH} Reverse input load current.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{IN} Input voltage applied in I_{IL}, I_{IH} tests.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} flowing into output.

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 54/7400 Series	1	1
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

OPERATION TABLE

Y Multiplier			Operation X Multiplicand
y_{-1}	y_0	y_1	
0	0	0	K + 0
1	0	0	K + X
0	1	0	K + X
1	1	0	K + 2X
0	0	1	K − 2X
1	0	1	K − X
0	1	1	K − X
1	1	1	K − 0

Active Low Inputs and Outputs
'1' = Low, '0' = High, P = High
Active High Inputs and Outputs
'1' = High, '0' = Low, $\overline{P}$ = Low

Am2505 LOADING RULES IN UNIT LOADS

Input/Output	Pin No.'s	Input Unit Load Input HIGH	Input LOW	Fanout Output HIGH	Output LOW
x_4	1	1	1	—	—
C_n	2	1	1	—	—
x_3	3	1	1	—	—
x_2	4	2	1	—	—
x_1	5	2	1	—	—
x_0	6	2	1	—	—
x_{-1}	7	1	1	—	—
S_0	8	—	—	12	6
S_1	9	—	—	12	6
S_2	10	—	—	12	6
S_3	11	—	—	12	6
GND	12	—	—	—	—
C_{n+4}	13	—	—	12	6
S_4	14	—	—	12	6
S_5	15	—	—	12	6
k_3	16	2	2	—	—
k_2	17	2	2	—	—
k_1	18	2	2	—	—
k_0	19	2	2	—	—
$\overline{P}$	20	3	3	—	—
y_1	21	0.9	0.9	—	—
y_0	22	2	2	—	—
y_{-1}	23	0.9	0.9	—	—
V_{CC}	24	—	—	—	—

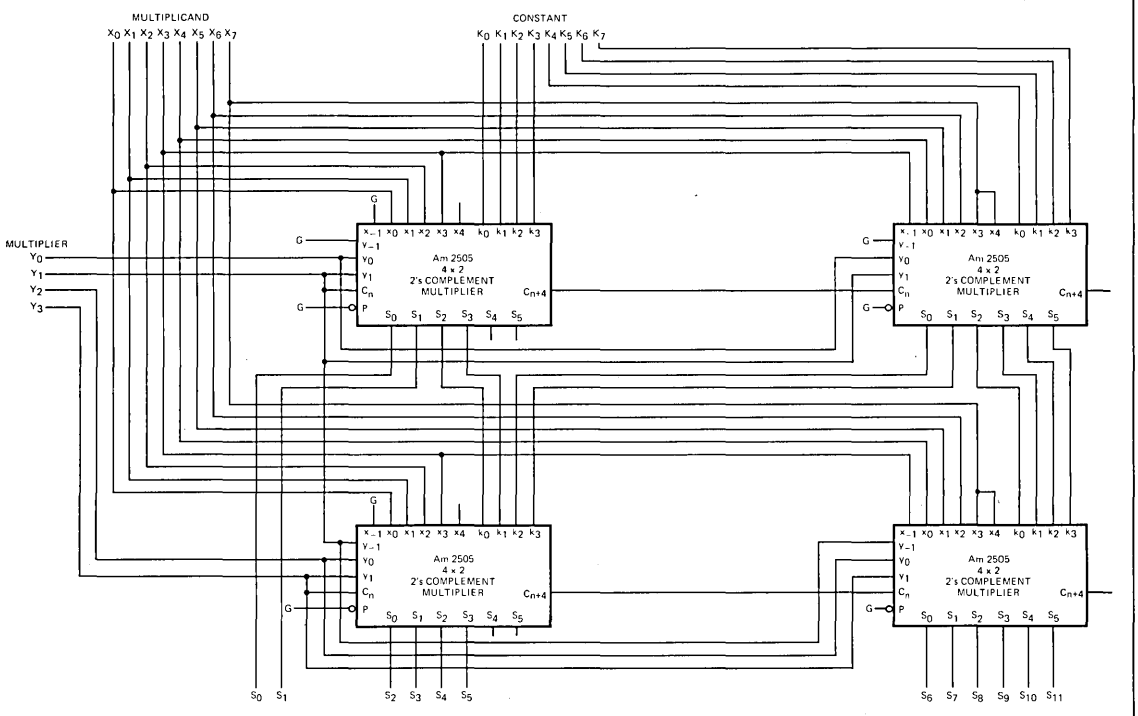
USER NOTES

1. Arithmetic in the multiplier is performed in the 2's complement notation, which requires a carry in at the first stage. This is accomplished by connecting the y_i multiplier bit to the appropriate carry input terminal $i = 1, 3, 5 \ldots$
2. The multiplier can perform multiplication in either the active high (positive logic) or active low (negative logic) representations by reinterpreting the active logic level and by grounding or leaving the polarity control pin $\overline{P}$ open circuit respectively.
3. Multiplication can be performed in number representations other than 2's complement by either correcting the 2's complement product or adding in a correction at the beginning of the multiplication at the K inputs. 2's complement numbers are represented as: $X_2 = x - x_s 2^{n-1}$.

Number representation	Correction
2's complement	None
1's complement	Add $x_s Y_2 + y_s X_2 + x_s y_s$ at k inputs
Unsigned (magnitude)	Extend multiplier and multiplicand one bit at the least significant end. Form $x_0 y_0 + y_0 x + x_0 y$ with conditional adder and add to array shifted two places up at k inputs. Force $k_s, y_s, x_s = 0$.
Sign magnitude	$x_s = 0, y_s = 0$ None
	$x_s = 1, y_s = 0$ Form $[(XY)_2 + 2^{n-1}y]$
	$x_s = 0, y_s = 1$ Form $[(XY)_2 + 2^{n-1}x]$
	$x_s = 1, y_s = 1$ Add $2^{n-1}(x + y) - 2^{2n-2}$

4. The parallelogram structure resulting from connecting multipliers in an array is not the arrangement that makes for the fastest speed. Multiplication is no more than a series of conditional additions and subtractions, and it makes no difference to the final product in what order the operations occur. A multiplier can be moved in the array as long as the arithmetic weight associated with the multiplier is not changed. When multipliers are moved the x and y lines must go with the device; only the carry in, carry out, and k input lines can be broken. The fastest array arrangement has usually a triangular shape.
5. For higher speed multiplication the array can be split into several parts that can be added together with high-speed adders.
6. Rounding off to a single length product can be achieved by adding a '1' to the array at the most significant positive k input of the array, ignoring the most significant product digit, and using the remainder of the most significant part of the product.
7. Truncation of a product without round off enables some of the multipliers in the array to be removed.

APPLICATIONS



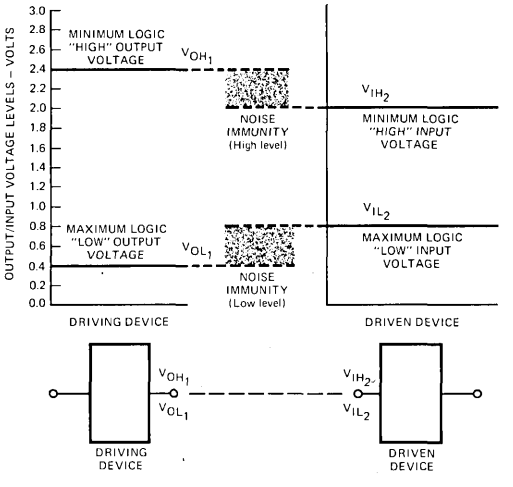
2's Complement 8 x 4 Multiplication Active High Levels

This diagram shows how the multiplier can be expanded in both the multiplier and multiplicand directions. (G = ground)

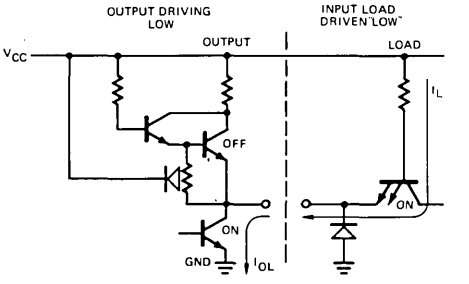
Figure 2

INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH



Current Interface Conditions — LOW



Current Interface Conditions — HIGH

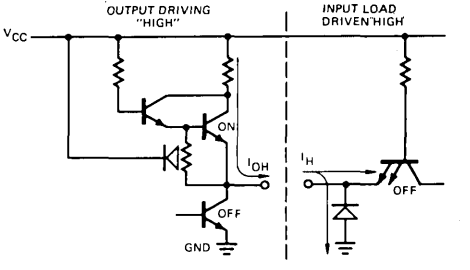
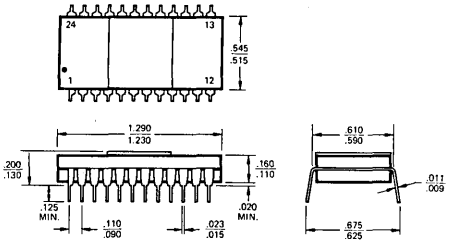


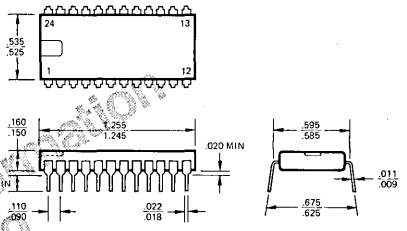
Figure 3

PHYSICAL DIMENSIONS

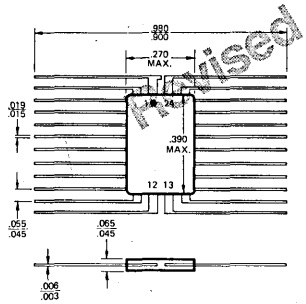
Hermetic Dual-In-Line



Molded

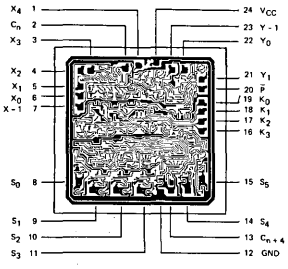


Flat Package



Metallization and Pad Layout

101 x 101 Mils



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Am25L05

Low Power Four-Bit by Two-Bit 2's Complement Multiplier

Distinctive Characteristics

- Provides 2's complement multiplication at high speed without correction.
- Can be used in a combinatorial array or in a time sequenced mode.
- Multiplies two 12-bit signed numbers typically in 335 ns.
- Multiplies in active HIGH (positive logic) or active LOW (negative logic) representations.
- Easy correction for unsigned, sign-magnitude or 1's complement multiplication.
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

The Am25L05 is a high-speed digital multiplier that can multiply numbers represented in the 2's complement notation and produce a 2's complement product without correction. The device consists of a 4x2 multiplier that can be connected to form iterative arrays able to multiply numbers either directly, or in a time sequenced arrangement. The device assumes that the most significant digit in a word carries a negative weight, and can therefore be used in arrays where the multiplicand and multiplier have different word lengths. The multiplier uses the quaternary algorithm and performs the function $S = XY + K$ where K is the input field used to add partial products generated in the array. At the beginning of the array the K inputs are available to add a signed constant to the least significant part of the product. Multiplication of an m bit number by an n bit number in an array results in a product having m+n bits so that all possible combinations of product are accounted for. If a conventional 2's complement product is required the most significant bit can be ignored, and overflow conditions can be detected by comparing the last two product digits.

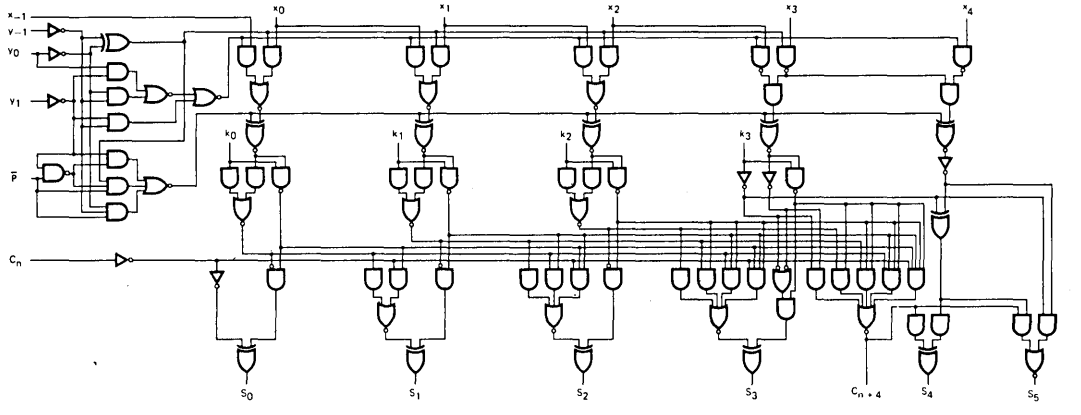
Provision is made in the design for multiplication in the active high (positive logic) or active low (negative logic) representations simply by reinterpreting the active level of the input operands, the product, and a polarity control $\overline{P}$. For a more complete description and applications, the user is referred to the Am2505 Application Note.

LOADING RULES In Unit Loads (Notes)

	TTL LOADS		93L LOADS	
Input Load Factor	HIGH	LOW	HIGH	LOW
Y_1, Y_{-1}	0.45	0.25	0.9	0.9
x_{-1}, x_3, x_4, C_n	0.5	0.25	1.0	1.0
x_0, x_1, x_2	1.0	0.25	2.0	1.0
Y_0, k_0, k_1, k_2, k_3	1.0	0.5	2.0	2.0
$\overline{P}$	1.5	0.75	3.0	3.0
Output Drive	HIGH	LOW	HIGH	LOW
All Outputs	9	3	18	12

Notes:
1. A TTL unit load is specified as 0.4V at −1.6mA LOW, 2.4V at 40μA HIGH.
2. A 93L unit load is specified as 0.3V at −400μA LOW, 2.4V at 20μA HIGH.
3. Enough output LOW current is available to mix TTL and 93L loads and still meet the 93L requirement of a V_{OL} of 0.3V.

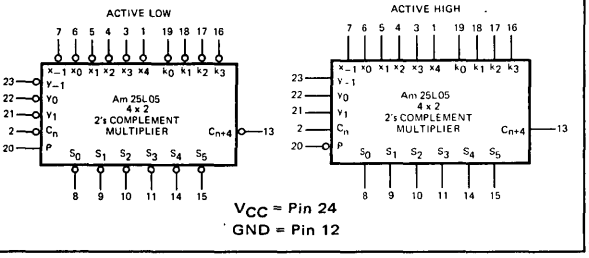
LOGIC DIAGRAM



Am25L05 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	AM25L05PC
Hermetic DIP	0°C to +75°C	AM25L05DC
Dice	0°C to +75°C	AM25L05XC
Hermetic DIP	−55°C to +125°C	AM25L05DM
Hermetic Flat Pak	−55°C to +125°C	AM25L05FM
Dice	−55°C to +125°C	AM25L05XM

LOGIC SYMBOLS



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150
Temperature (Ambient) Under Bias	−55°C to +125
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} m
DC Input Voltage	−0.5 V to +5.5
Output Current, Into Outputs	30m
DC Input Current	−30 mA to +5.0m

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am25L05XC T_A = 0°C to +75°C V_{CC} = 4.75 V to 5.25 V
Am25L05XM T_A = −55°C to +125°C V_{CC} = 4.50 V to 5.50 V

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 4.92 mA V_{IN} = V_{IH} = or V_{IL}		0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.7	Volts
I_{IL} (Note 2)	93L Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.3 V		−0.25	−0.4	mA
I_{IH} (Note 2)	93L Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V		2.0	20	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V	−5	−17	−40	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., Y_1 = 0.0 V		30	45	mA

Notes: 1. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2. Actual input currents are obtained by multiplying unit load current by the 93L input load factor. (See loading rules)

Switching Characteristics (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF)

Parameters	From (Input)	To (Output)	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH} t_{PHL}	C_n	C_{n+4}	See Test Table	15 17	30 35	45 53	ns
t_{PLH} t_{PHL}	C_n	$S_{0,1,2,3}$	See Test Table	17 18	35 37	53 56	ns
t_{PLH} t_{PHL}	C_n	$S_{4,5}$	See Test Table	23 21	46 42	70 63	ns
t_{PLH} t_{PHL}	Any k	C_{n+4}	See Test Table	13 18	26 36	39 54	ns
t_{PLH} t_{PHL}	Any k	$S_{0,1,2,3}$	See Test Table	18 18	36 37	54 56	ns
t_{PLH} t_{PHL}	Any k	$S_{4,5}$	See Test Table	13 15	45 58	68 87	ns
t_{PLH} t_{PHL}	Any x	C_{n+4}	See Test Table	36 27	72 55	108 83	ns
t_{PLH} t_{PHL}	Any x	$S_{0,1,2,3}$	See Test Table	25 45	50 90	75 135	ns
t_{PLH} t_{PHL}	Any x	$S_{4,5}$	See Test Table	45 40	90 80	135 120	ns
t_{PLH} t_{PHL}	Any y	C_{n+4}	See Test Table	40 35	80 70	120 105	ns
t_{PLH} t_{PHL}	Any y	$S_{0,1,2,3}$	See Test Table	36 47	72 95	108 142	ns
t_{PLH} t_{PHL}	Any y	$S_{4,5}$	See Test Table	47 46	95 92	142 138	ns

SWITCHING TIME TEST TABLE

Input	Outputs	Inputs at 0V (remaining inputs at 4.5V)
C_n	C_{n+4}, S_{0123}, S_{45}	P, Y_{-1}, Y_1, All X
k_0	C_{n+4}, S_{0123}, S_{45}	P, Y_{-1}, Y_1, All X
k_1	C_{n+4}, S_{123}, S_{45}	P, Y_{-1}, Y_1, All X
k_2	C_{n+4}, S_{23}, S_{45}	P, Y_{-1}, Y_1, All X
k_3	S_3	P, Y_{-1}, Y_1, All X
k_3	S_{45}	P, Y_{-1}, Y_1, All X, C_n
x_{-1}	C_{n+4}, S_{0123}, S_{45}	P, Y_1, All k
x_0	C_{n+4}, S_{0123}, S_{45}	P, Y_{-1}, Y_1, All k
x_1	C_{n+4}, S_{123}, S_{45}	P, Y_{-1}, Y_1, All k
x_2	C_{n+4}, S_{123}, S_{45}	P, Y_{-1}, Y_1, All k
x_3	S_3	P, Y_{-1}, Y_1, All k
x_3	S_{45}	P, Y_{-1}, Y_1, All k, C_n
x_4	S_{45}	P, Y_1, All k, C_n
y_{-1}	C_{n+4}, S_{0123}, S_{45}	P, X_1, X_2, X_3, X_4, All k
y_0	C_{n+4}, S_{0123}, S_{45}	P, X_1, X_2, X_3, X_4, All k
y_1	C_{n+4}, S_{0123}, S_{45}	X_0, X_1, X_2, X_3, X_4, All k

USER NOTES

1. Arithmetic in the multiplier is performed in the 2's complement notation, which requires a carry in at the first stage. This is accomplished by connecting the y_i multiplier bit to the appropriate carry input terminal $i = 1, 3, 5 \ldots$
2. The multiplier can perform multiplication in either the active high (positive logic) or active low (negative logic) representations by reinterpreting the active logic level and by grounding or leaving the polarity control pin $\overline{P}$ open circuit respectively.
3. Multiplication can be performed in number representations other than 2's complement by either correcting the 2's complement product or adding in a correction at the beginning of the multiplication at the K inputs. 2's complement numbers are represented as: $X_2 = x - x_s 2^{n-1}$.

Number representation	Correction
2's complement	None
1's complement	Add $x_s Y_2 + y_s X_2 + x_s y_s$ at k inputs
Unsigned (magnitude)	Extend multiplier and multiplicand one bit at the least significant end. Form $x_0 y_0 + y_0 x + x_0 y$ with conditional adder and add to array shifted two places up at k inputs. Force $k_s, y_s, x_s = 0$.
Sign magnitude	$x_s = 0, y_s = 0$ None
	$x_s = 1, y_s = 0$ Form $[(XY)_2 + 2^{n-1} y]$
	$x_s = 0, y_s = 1$ Form $[(XY)_2 + 2^{n-1} x]$
	$x_s = 1, y_s = 1$ Add $2^{n-1}(x + y) - 2^{2n-2}$

4. For the highest speed array with the multipliers arranged in a parallelogram structure carries between certain multipliers are exchanged with the y carry-ins needed for 2's complement subtract. The delays in the array are then equalized as best possible as shown in Figure 1.
5. For higher speed multiplication the array can be split into several parts that can be added together with high-speed adders.
6. Rounding off to a single length product can be achieved by adding a '1' to the array at the most significant positive k input of the array, ignoring the most significant product digit, and using the remainder of the most significant part of the product.
7. Truncation of a product without round off enables some of the multipliers in the array to be removed.

APPLICATION

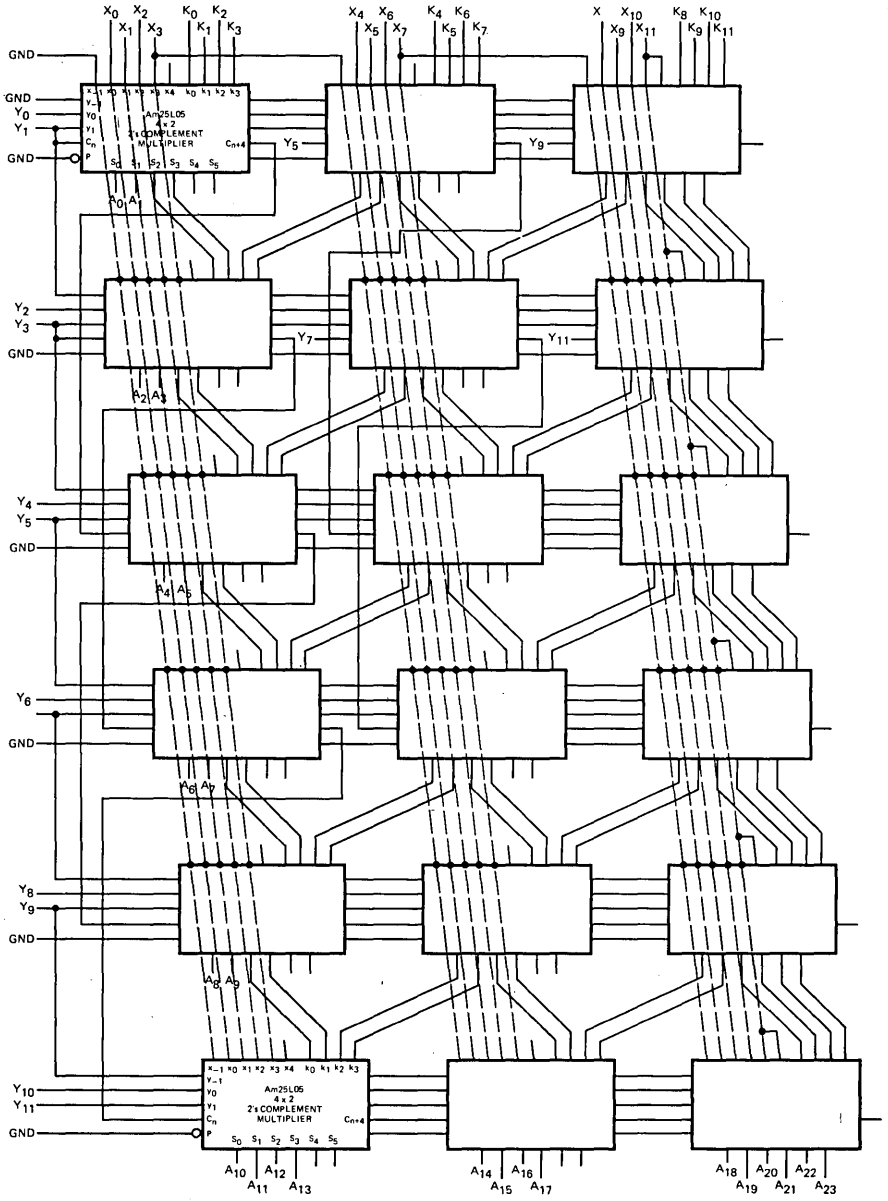


Figure 1. 12 x 12 Low-Power Signed Multiplier

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Am2506

Four-Bit Arithmetic Logic Unit/Function Generator with Output Latch

Distinctive Characteristics:

Provides 16 arithmetic operations including add, subtract, double and compare.

Provides ALL 16 possible logic operations of two variables in typically 22 ns.

Output latch provided to hold contents of operation.

Typical add time for 4 bits of only 22 ns, and typical carry time of 12 ns.

- Full Look-ahead for high-speed arithmetic operation on long words.
- 100% reliability assurance testing in compliance with MIL STD 883.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

The Am2506 is a 4-bit high-speed parallel Arithmeic Logic Unit (ALU)/ Digital Function Generator with Output Latch. When the mode control (M) is held LOW the circuit performs under control of four function select lines 16 arithmetic operations, the most important being add and subtract, on two 4-bit parallel binary words. When the mode control is held HIGH the circuit performs, under control of the four function select lines sixteen logic operations on an individual bit basis between the two four-bit parallel words.

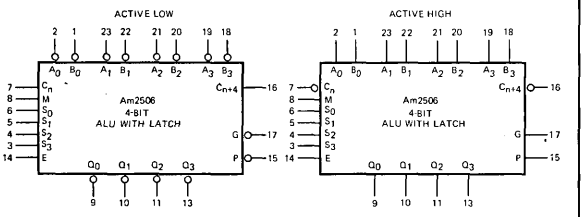
If the latch enable E is held HIGH the result of an operation appears at the outputs $\overline{Q}_0$ to $\overline{Q}_3$ and is stored in the latch when E goes LOW.

An internal full look-ahead carry scheme is used for high-speed arithmetic operations and provision made for further look-ahead by providing carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs. These carry signals can be used as inputs to the Am54/74182 look-ahead carry generator to form long word length high-speed parallel arithmetic logic units. Addition time for sixteen-bit words with four Am2506 ALU's and one Am54/74182 look-ahead generator is only 34 ns.

For systems where *ultra high-speed is not required, the carry output* signal (C_{n+4}) can be used to provide ripple-block arithmetic operations.

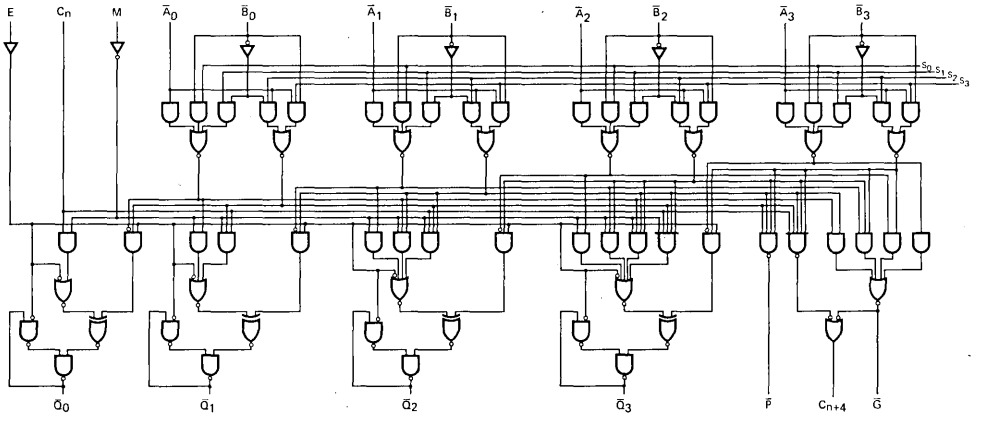
The ALU can be used with either active HIGH or active LOW inputs and can also be expanded with the Am54/74182 look-ahead carry generator in either mode by reinterpreting the carry signals.

LOGIC SYMBOLS



V_{CC} = PIN 24
GND = PIN 12

LOGIC DIAGRAM

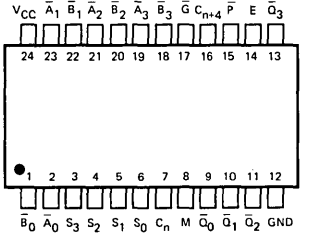


Am2506 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	AM250659C
Hermetic DIP	0°C to +75°C	AM250659G
Hermetic DIP	−55°C to +125°C	AM250651G
Hermetic Flat Pak	−55°C to +125°C	AM250651P
Dice	Note	AM2506XXD

NOTE: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am250659X — T_A = 0°C to +75°C V_{CC} = 4.75 V to 5.25 V
Am250651X — T_A = −55°C to +125°C V_{CC} = 4.5 V to 5.50 V

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.8 mA V_{IN} = V_{IH} or V_{IL}		2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16.0 mA V_{IN} = V_{IH} or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V			−1.0	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V			4.0	40	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current Am250659X	V_{CC} = MAX., V_{OUT} = 0.0 V		−18		−57	mA
I_{SC}	Output Short Circuit Current Am250651X	V_{CC} = MAX., V_{OUT} = 0.0 V		−20		−55	mA
I_{CC}	Power Supply Current Am250651X	V_{CC} = MAX.	$A_{0,3}$ = 4.5 V $B_{0,3}$, C_n = 0 V		88	127	mA
			A_{0-3}, B_{0-3}, C_n = 0 V		94	135	
I_{CC}	Power Supply Current Am250659X	V_{CC} = MAX.	$A_{0,3}$ = 4.5 V $B_{0,3}$, C_n = 0 V		88	140	mA
			A_{0-3}, B_{0-3}, C_n = 0 V		94	150	

Note 1. Typical limits are at Vcc = 5.0 V, 25°C ambient and maximum loading.
Note 2. For other input currents use Am2506 loading rules.

SWITCHING CHARACTERISTICS V_{CC} = 5 V, T_A = 25°C, N = 10 (C_L = 15 pF, R_L = 400 Ω)

Parameter	From	To	Test Conditions See also Tables 1, 2, 3	Min	Typ	Max	Units
t_{pd+}	C_n	C_{n+4}		8	12	18	ns
t_{pd-}				8	13	19	
t_{pd+}	C_n	$\overline{Q}_i$	M = 0 V, E = 4.5 V (SUM or DIFF mode)	8	15	19	ns
t_{pd-}				8	13	18	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{G}$	M = 0 V, S_0 = S_3 = 4.5 V, S_1 = S_2 = 0 V (SUM mode)	8	13	19	ns
t_{pd-}				8	13	19	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{G}$	M = 0 V, S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (DIFF mode)	11	17	25	ns
t_{pd-}				11	17	25	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{P}$	M = 0 V, S_0 = S_3 = 4.5 V, S_1 = S_2 = 0 V (SUM mode)	8	15	19	ns
t_{pd-}				8	15	22	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{P}$	M = 0 V, S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (DIFF mode)	11	17	25	ns
t_{pd-}				11	17	25	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{Q}_{i+1}$	M = 0 V, S_0 = S_3 = 4.5 V, E = 4.5 V S_1 = S_2 = 0 V (SUM mode)	14	22	29	ns
t_{pd-}				14	21	30	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{Q}_{i+1}$	M = 0 V, S_0 = S_3 = 0 V, E = 4.5 V S_1 = S_2 = 4.5 V (DIFF mode)	17	27	36	ns
t_{pd-}				15	23	32	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{Q}_i$	M = 4.5 V (LOGIC mode), E = 4.5 V	14	22	29	ns
t_{pd-}				14	22	29	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	C_{n+4}	M = 0 V, S_0 = S_3 = 4.5 V, S_1 = S_2 = 0 V (SUM mode)	11	17	25	ns
t_{pd-}				14	20	30	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	C_{n+4}	M = 0 V, S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (DIFF mode)	14	21	32	ns
t_{pd-}				14	20	30	
t_{pd+}	Enable LOW to HIGH	$\overline{Q}_i$	M = 0 V, S_0 = S_3 = 4.5 V S_1 = S_2 = 0 V (SUM mode)	8	15	23	ns
t_{pd-}				7	14	21	
t_{pw}(E)	Minimum Enable HIGH Time		M = 0 V, S_0 = S_3 = 4.5 V S_1 = S_2 = 0 V (SUM mode)		5	10	ns
t_s(E)	Set Up Time, Q Outputs to enable HIGH to LOW			−18		− 8	ns

TEST TABLES

DIFF MODE TEST TABLE

FUNCTION INPUTS: $S_1 = S_2 = E = 4.5$ V, $S_0 = S_3 = M = 0$ V

Parameter	Input Under Test	Other Input Same Bit: Apply 4.5 V	Other Input Same Bit: Apply 0 V	Other Data Inputs: Apply 4.5 V	Other Data Inputs: Apply 0 V	Output Under Test	Output Waveform
t_{pd+} / t_{pd-}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{Q}_{i+1}$	1
t_{pd+} / t_{pd-}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{Q}_{i+1}$	2
t_{pd+} / t_{pd-}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	1
t_{pd+} / t_{pd-}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	2
t_{pd+} / t_{pd-}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	1
t_{pd+} / t_{pd-}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	2
t_{pd+} / t_{pd-}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}	2
t_{pd+} / t_{pd-}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}	1
t_{pd+} / t_{pd-}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4}	1

Table 1

SUM MODE TEST TABLE

FUNCTION INPUTS: $S_0 = S_3 = E = 4.5$ V, $S_1 = S_2 = M = 0$ V

Parameter	Input Under Test	Other Input Same Bit: Apply 4.5 V	Other Input Same Bit: Apply 0 V	Other Data Inputs: Apply 4.5 V	Other Data Inputs: Apply 0 V	Output Under Test	Output Waveform
t_{pd+} / t_{pd-}	$\overline{A}_i$	$\overline{B}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{Q}_{i+1}$	1
t_{pd+} / t_{pd-}	$\overline{B}_i$	$\overline{A}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{Q}_{i+1}$	1
t_{pd+} / t_{pd-}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	1
t_{pd+} / t_{pd-}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	1
t_{pd+} / t_{pd-}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	1
t_{pd+} / t_{pd-}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	1
t_{pd+} / t_{pd-}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	2
t_{pd+} / t_{pd-}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	2
t_{pd+} / t_{pd-}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{Q}$ or C_{n+4}	1

Table 2

LOGIC MODE TEST TABLE

FUNCTION INPUTS: $S_1 = S_2 = M = 4.5$ V, $S_0 = S_3 = 0$ V

Parameter	Input Under Test	Other Input Same Bit: Apply 4.5 V	Other Input Same Bit: Apply 0 V	Other Data Inputs: Apply 4.5 V	Other Data Inputs: Apply 0 V	Output Under Test	Output Waveform
t_{pd+} / t_{pd-}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{Q}_i$	1
t_{pd+} / t_{pd-}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{Q}_i$	1

Table 3

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS:

$\overline{A}_i$ Active LOW Data A inputs i = 0, 1, 2, 3.

$\overline{B}_i$ Active LOW Data B inputs i = 0, 1, 2, 3.

C_n Active HIGH Carry In to nth ALU bit.

C_{n+4} Active HIGH Carry Out of n+4th ALU bit.

E Active HIGH output latch enable. The result of an operation is stored when the Enable goes from a HIGH Logic level to a LOW Logic level.

$\overline{Q}_i$ Active LOW Data Outputs of ALU latch i = 0, 1, 2, 3.

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

$\overline{G}$ Active LOW carry generate output for use in multi-level look-ahead schemes.

M Mode Input controls whether arithmetic or logic operation.

$\overline{P}$ Active LOW carry propagate output for use in multi-level look-ahead schemes.

S_i Control inputs determine the arithmetic or logic function obeyed i = 0, 1, 2, 3.

Unit Load One T^2L gate input load. In the HIGH state it is equal to I_{IH} and in the LOW state it is equal to I_{IL}.

OPERATIONAL TERMS:

I_{IL} Forward input load current.

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{IH} Reverse input load current.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 54/7400 Series	1	1
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Table 4

USER NOTES

1. Arithmetic operations are performed on a word basis.
2. Logic operations are performed on a bit basis.
3. Arithmetic in 1's complement requires an end around carry.
4. Subtraction in 2's complement arithmetic requires a carry in (C_n = HIGH) active LOW case, ($\overline{C}_n$ = LOW) active HIGH case.
5. In the active HIGH case the B field can be complemented, and in the active LOW case the A field can be complemented. The operation table is changed by complementing the appropriate variable for each operation.

Am2506 LOADING RULES

Input/Output	Pin No.'s	Input Unit Load	Fanout Output HIGH	Output LOW
$\overline{B}_0$	1	3	—	—
$\overline{A}_0$	2	3	—	—
S_3	3	4	—	—
S_2	4	4	—	—
S_1	5	4	—	—
S_0	6	4	—	—
C_n	7	5	—	—
M	8	1	—	—
$\overline{Q}_0$	9	—	20	10
$\overline{Q}_1$	10	—	20	10
$\overline{Q}_2$	11	—	20	10
GND	12	—	—	—
$\overline{Q}_3$	13	—	20	10
E	14	1	—	—
$\overline{P}$	15	—	20	10
C_{n+4}	16	—	20	10
$\overline{G}$	17	—	20	10
$\overline{B}_3$	18	3	—	—
$\overline{A}_3$	19	3	—	—
$\overline{B}_2$	20	3	—	—
$\overline{A}_2$	21	3	—	—
$\overline{B}_1$	22	3	—	—
$\overline{A}_1$	23	3	—	—
V_{CC}	24	—	—	—

Table 5

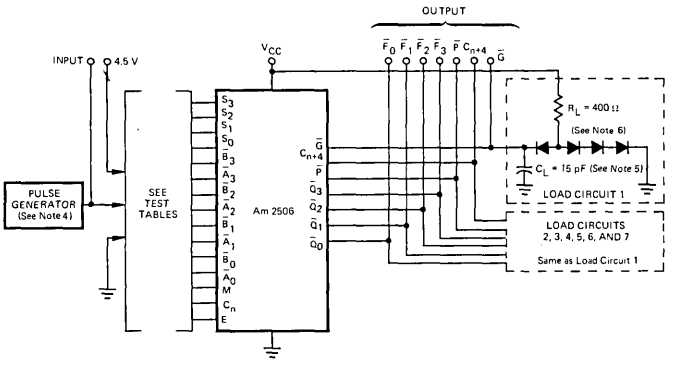
OPERATION TABLE

Control Inputs				Active LOW Inputs and Outputs		Active HIGH Inputs and Outputs	
S_0	S_1	S_2	S_3	Arithmetic (M = L, C_n = L)	Logic (M = H)	Arithmetic (M = L, $\overline{C}_n$ = H)	Logic (M = H)
L	L	L	L	A minus 1	$\overline{A}$	A	$\overline{A}$
H	L	L	L	AB minus 1	$\overline{AB}$	A + B	$\overline{A + B}$
L	H	L	L	$A\overline{B}$ minus 1	$\overline{A} + B$	$A + \overline{B}$	$\overline{AB}$
H	H	L	L	minus 1 (2's comp.)	Logic '1'	minus 1 (2's comp.)	Logic '0'
L	L	H	L	A plus [A + $\overline{B}$]	$\overline{A + B}$	A plus $A\overline{B}$	$\overline{AB}$
H	L	H	L	AB plus [A + $\overline{B}$]	$\overline{B}$	$A\overline{B}$ plus [A + B]	$\overline{B}$
L	H	H	L	A minus B minus 1	$\overline{A \oplus B}$	A minus B minus 1	$A \oplus B$
H	H	H	L	A + $\overline{B}$	A + $\overline{B}$	$A\overline{B}$ minus 1	$A\overline{B}$
L	L	L	H	A plus [A + B]	$\overline{AB}$	A plus AB	$\overline{A} + B$
H	L	L	H	A plus B	$A \oplus B$	A plus B	$\overline{A \oplus B}$
L	H	L	H	$A\overline{B}$ plus [A + B]	B	AB plus [A + $\overline{B}$]	B
H	H	L	H	A + B	A + B	AB minus 1	AB
L	L	H	H	A plus A (2 x A)	Logic '0'	A plus A (2 x A)	Logic '1'
H	L	H	H	A plus AB	$A\overline{B}$	A plus [A + B]	A + $\overline{B}$
L	H	H	H	A plus $A\overline{B}$	AB	A plus [A + $\overline{B}$]	A + B
H	H	H	H	A	A	A minus 1	A

L = LOW Voltage Level
H = HIGH Voltage Level

Table 6

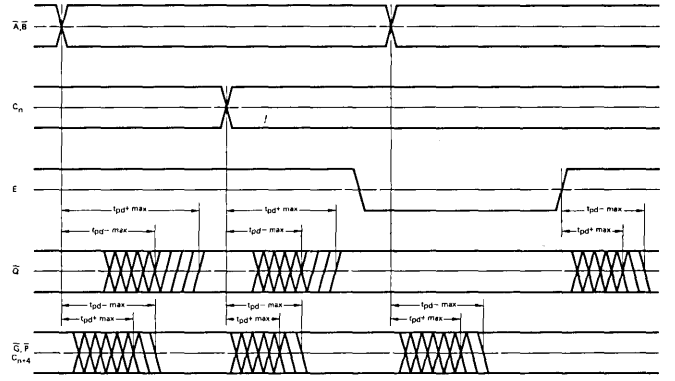
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

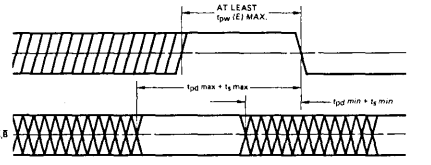


Note 4. The pulse generator has the following characteristics: frequency = 1 MHz, $Z_{out} \approx 50\ \Omega$.
5. C_L includes probe and jig capacitance.
6. All diodes are 1N3064.

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN



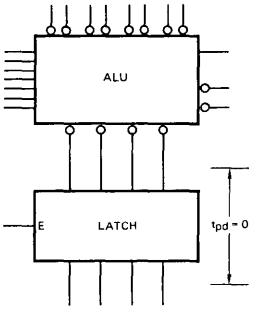


Timing Requirements – 2506
Changes are permitted only during periods marked with diagonal lines.

Am2506 SET-UP and RELEASE TIMES

To determine the timing requirements for the enable input of the Am2506, it is helpful to consider the device as consisting of two parts, an ALU followed by a latch on the outputs. See the Figure. (In fact, the latch is an integral part of the ALU and does not contribute delay between the Am2506 inputs and outputs. The latch in the model therefore has a propagation delay of zero.) The delay between input changes on the ALU and steady data on the inputs of the latch is defined by the tpd's of the Am2506. In the model, a signal change on an ALU input will cause the data at the latch input to change sometime between t_{pd} min and t_{pd} max for that path in the Am2506 switching specification. The set-up and release times for the enable input may be defined in the ordinary manner; they are the maximum and minimum set-up times for the data inputs relative to the end of the enable pulse. To guarantee storing data, the data must be present at the latch input for at least t_s max before the end of the enable. To guarantee not storing data, the latch inputs must not change until after t_s min before the end of the enable. The maximum and minimum set-up times for the Am2506 are defined in this fashion for the latch in the model shown.

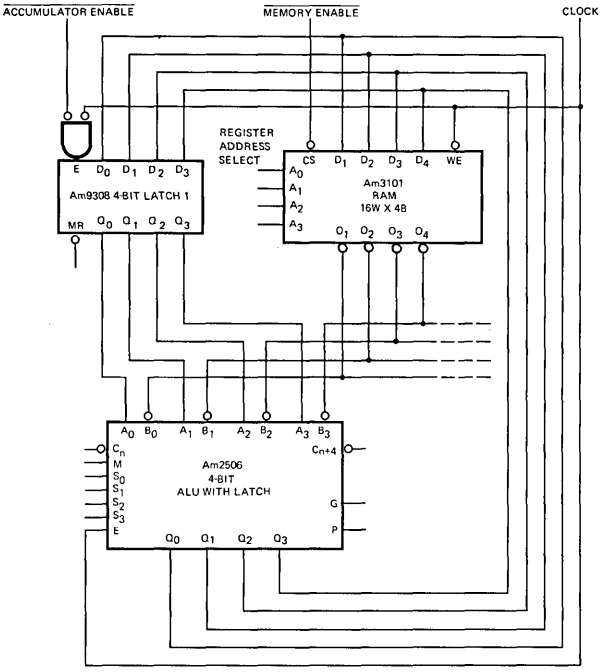
The timing requirements for the Am2506 can then be stated as follows: To guarantee storing data, the time between the application of steady data to the Am2506 inputs and the end of the latch enable must be at least t_{pd} max plus t_s max. To guarantee not storing data, the delay between a change on the Am2506 inputs and the end of the latch enable must be less than t_{pd} min plus t_s min. Since the set-up times are negative, the algebraic addition allows the latch enable to end before the data actually appears at the Am2506 output.



Model of Am2506 With Separate Latch On ALU Outputs

Am2506 APPLICATION

16-WORD 4-BIT ARITHMETIC REGISTER SLICE



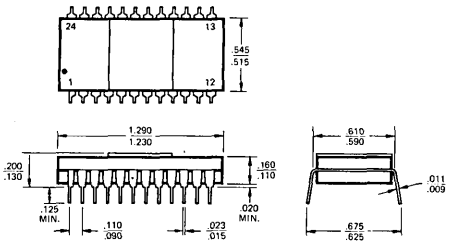
FUNCTION TABLE

S_0	S_1	S_2	S_3	Arithmetic (M = L, $\overline{C}_n$ = H)	Logic (M = H)
L	L	L	L	A	$\overline{A}$
H	L	L	L	$A + \overline{B}$	$\overline{A}B$
L	H	L	L	A + B	$\overline{A}\overline{B}$
H	H	L	L	minus 1 (2's comp.)	Logic '0'
L	L	H	L	A plus AB	AB
H	L	H	L	AB plus $[A + \overline{B}]$	B
L	H	H	L	A plus B	$\overline{A \oplus B}$
H	H	H	L	AB minus 1	AB
L	L	L	H	A plus $A\overline{B}$	$\overline{A} + \overline{B}$
H	L	L	H	A minus B minus 1	$A \oplus B$
L	H	L	H	$A\overline{B}$ plus $[A + B]$	$\overline{B}$
H	H	L	H	$A\overline{B}$ minus 1	$A\overline{B}$
L	L	H	H	A plus A (2 x A)	Logic '1'
H	L	H	H	A plus $[A + \overline{B}]$	A + B
L	H	H	H	A plus [A + B]	$A + \overline{B}$
H	H	H	H	A minus 1	A

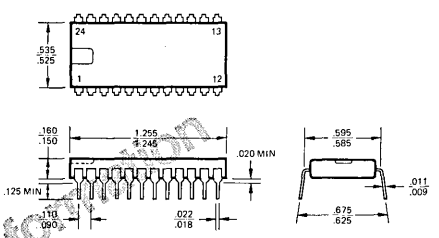
L = Low Voltage Level
H = High Voltage Level

PHYSICAL DIMENSIONS
Dual-In-Line

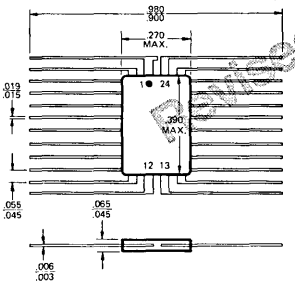
Hermetic



Molded

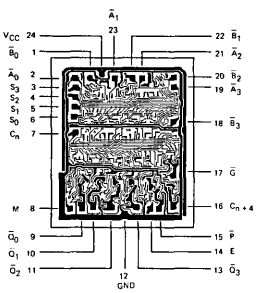


Flat Package



Metallization and Pad Layout

90 x 108 Mils



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Am25L06

Low-Power Four-Bit Arithmetic Logic Unit/ Function Generator with Output Latch

stinctive Characteristics

125 mw typical power dissipation.

Includes four-bit latch on outputs.

Typical add time for 4 bits of only 47 ns.

- 100% reliability assurance testing in compliance with MIL STD 883.
- Provides all 16 possible logic operations of two variables typically in 42 ns.

FUNCTIONAL DESCRIPTION

The Am25L06 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU)/ Digital Function Generator with Output Latch. When the mode control (M) is held LOW the circuit performs under control of four function select lines 16 arithmetic operations, the most important being add and subtract, on two 4-bit parallel binary words. When the mode control is held HIGH the circuit performs, under control of the four function select lines sixteen logic operations on an individual bit basis between the two four-bit parallel words.

If the latch enable E is held HIGH the result of an operation appears at the outputs $\overline{Q}_0$ to $\overline{Q}_3$ and is stored in the latch when E goes LOW.

An internal full look-ahead carry scheme is used for high-speed arithmetic operations and provision made for further look-ahead by providing carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs. These carry signals can be used as inputs to the Am54/74182 look-ahead carry generator to form long word length high-speed parallel arithmetic logic units. Addition time for sixteen-bit words with four Am25L06 ALU's and one Am54/74182 look-ahead generator is only 34 ns.

For systems where ultra high-speed is not required, the carry output signal (C_{n+4}) can be used to provide ripple-block arithmetic operations.

The ALU can be used with either active HIGH or active LOW inputs and can also be expanded with the Am54/74182 look-ahead carry generator in either mode by reinterpreting the carry signals.

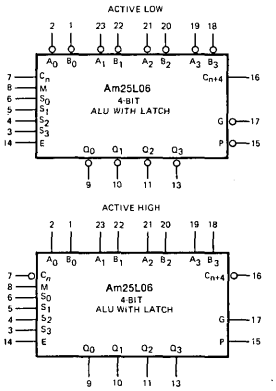
LOADING RULES

In Unit Loads (Notes)

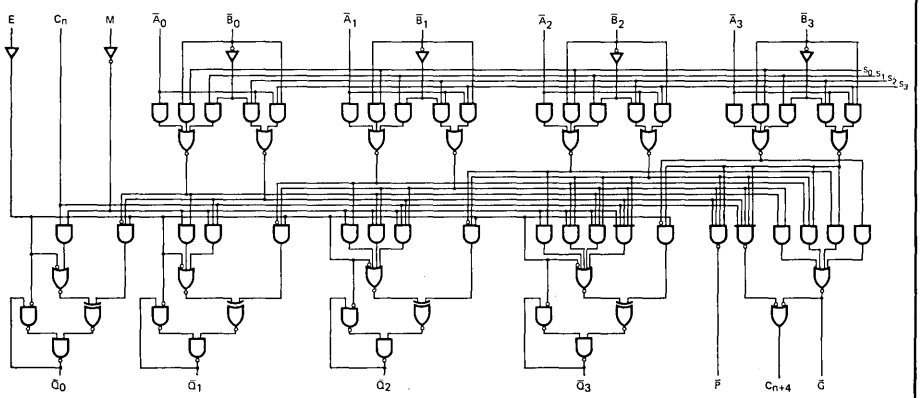
	TTL LOADS		93L LOADS	
Input Load Factor	HIGH	LOW	HIGH	LOW
M, E	0.5	0.25	1.0	1.0
all $\overline{A}$, all $\overline{B}$	1.5	0.75	3.0	3.0
S_0, S_1, S_2, S_3	2.0	1.0	4.0	4.0
C_n	2.5	1.25	5.0	5.0
Output Drive	HIGH	LOW	HIGH	LOW
$\overline{F}_0$, $\overline{F}_1$, $\overline{F}_2$, $\overline{F}_3$, $\overline{G}$, $\overline{P}$, C_{n+4}	10	3	20	12

NOTES:
1) A TTL unit load is specified as 0.4 V at −1.6 mA LOW, 2.4 V at 40 μA HIGH.
2) A 93L unit load is specified as 0.3 V at −400 μA LOW, 2.4 V at 20 μA HIGH.
3) Enough output LOW current is available to mix TTL and 93L loads and still meet the 93L requirement of a V_{OL} of 0.3 V.

LOGIC SYMBOLS



LOGIC DIAGRAM



Am25L06 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
24-Pin Molded DIP	0°C to +75°C	AM25L0659C
24-Pin Hermetic DIP	0°C to +75°C	AM25L0659G
24-Pin Hermetic DIP	−55°C to +125°C	AM25L0651G
24-Pin Hermetic Flat Pak	−55°C to +125°C	AM25L0651P
Dice	Note	AM25L06XXD

NOTE: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current (Note 1)	−30 mA to +5.0 mA

Note 1. Maximum current defined by DC input voltage.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am25L0659X — T_A = 0°C to +75°C V_{CC} = 4.75 V to 5.25 V Am25L0651X — T_A = −55°C to +125°C V_{CC} = 4.5 V to 5.50 V

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 4.92 mA V_{IN} = V_{IH} or V_{IL}		0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.7	Volts
I_{IL} (Note 2)	93L Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.3 V		−0.25	−0.4	mA
I_{IH} (Note 2)	93L Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V		2.0	20	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V	−4.5	−10	−15	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		25	40	mA

Notes: 1) Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by the 93L input load factor. (See loading rules)

SWITCHING CHARACTERISTICS V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF

Parameter	From (Input)	To (Output)	Test Conditions	Min	Typ	Max	Units
t_{pd+}	C_n	C_{n+4}		12	36	54	ns
t_{pd-}				12	23	35	
t_{pd+}	C_n	$\overline{Q}_i$	M = 0 V, E = 4.5 V (SUM or DIFF mode)	12	31	47	ns
t_{pd-}				12	24	36	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{G}$	M = 0 V, S_0 = S_3 = 4.5 V, S_1 = S_2 = 0 V (SUM mode)	12	31	47	ns
t_{pd-}				12	23	50	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{G}$	M = 0 V, S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (DIFF mode)	12	35	53	ns
t_{pd-}				12	26	54	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{P}$	M = 0 V, S_0 = S_3 = 4.5 V, S_1 = S_2 = 0 V (SUM mode)	12	35	53	ns
t_{pd-}				12	26	39	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{P}$	M = 0 V, S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (DIFF mode)	12	37	56	ns
t_{pd-}				12	34	51	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{Q}_{i+1}$	M = 0 V, S_0 = S_3 = 4.5 V, E = 4.5 V S_1 = S_2 = 0 V (SUM mode)	12	48	72	ns
t_{pd-}				12	47	71	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{Q}_{i+1}$	M = 0 V, S_0 = S_3 = 0 V, E = 4.5 V S_1 = S_2 = 4.5 V (DIFF mode)	12	53	80	ns
t_{pd-}				12	52	79	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{Q}_i$	M = 4.5 V (LOGIC mode), E = 4.5 V	12	38	57	ns
t_{pd-}				12	46	69	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	C_{n+4}	M = 0 V, S_0 = S_3 = 4.5 V, S_1 = S_2 = 0 V (SUM mode)	20	40	60	ns
t_{pd-}				20	44	66	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	C_{n+4}	M = 0 V, S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (DIFF mode)	20	44	70	ns
t_{pd-}				20	49	74	
t_{pd+}	Enable LOW to HIGH	$\overline{Q}_i$	M = 0 V, S_0 = S_3 = 4.5 V S_1 = S_2 = 0 V (SUM mode)	20	53	80	ns
t_{pd-}				20	50	75	
t_{pw}(E)	Minimum Enable HIGH Time		M = 0 V, S_0 = S_3 = 4.5 V S_1 = S_2 = 0 V (SUM mode)	5	14	21	ns
t_s(E)	Set Up Time, Q Outputs to enable HIGH to LOW		See Am2506 data sheet for explanation	−18		−8	ns

OPERATION TABLE

Control Inputs	Active LOW Inputs and Outputs		Active HIGH Inputs and Outputs	
S_0 S_1 S_2 S_3	Arithmetic (M = L, C_n = L)	Logic (M = H)	Arithmetic (M = L, $\overline{C}_n$ = H)	Logic (M = H)
L L L L	A minus 1	$\overline{A}$	A	$\overline{A}$
H L L L	AB minus 1	$\overline{AB}$	A + B	$\overline{A+B}$
L H L L	$A\overline{B}$ minus 1	$\overline{A}$ + B	A + $\overline{B}$	$\overline{AB}$
H H L L	minus 1 (2's comp.)	Logic '1'	minus 1 (2's comp.)	Logic '0'
L L H L	A plus [A + $\overline{B}$]	$\overline{A+B}$	A plus $A\overline{B}$	$\overline{AB}$
H L H L	AB plus [A + $\overline{B}$]	$\overline{B}$	$A\overline{B}$ plus [A + B]	$\overline{B}$
L H H L	A minus B minus 1	$\overline{A \oplus B}$	A minus B minus 1	A ⊕ B
H H H L	A + $\overline{B}$	A + $\overline{B}$	$A\overline{B}$ minus 1	$A\overline{B}$
L L L H	A plus [A + B]	$\overline{AB}$	A plus AB	$\overline{A}$ + B
H L L H	A plus B	A ⊕ B	A plus B	$\overline{A \oplus B}$
L H L H	$A\overline{B}$ plus [A + B]	B	AB plus [A + $\overline{B}$]	B
H H L H	A + B	A + B	AB minus 1	AB
L L H H	A plus A (2 x A)	Logic '0'	A plus A (2 x A)	Logic '1'
H L H H	A plus AB	$A\overline{B}$	A plus [A + B]	A + $\overline{B}$
L H H H	A plus $A\overline{B}$	AB	A plus [A + $\overline{B}$]	A + B
H H H H	A	A	A minus 1	A

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Am8284/8285

Binary Hexadecimal/BCD Decade Synchronous Up-Down Counters

Description: The Am8284 Binary Hexadecimal and the Am8285 BCD Decade Synchronous Up/Down Counters are functionally, electrically, and pin-for-pin an equivalent to the Signetics 8284 and 8285. They are available in the hermetic dual-in-line package.

Distinctive Characteristics: 100% reliability assurance testing including high temperature bake, temperature cycling, centrifuge and package hermeticity testing in compliance with MIL STD 883.

Mixing privileges for obtaining price discounts. Refer to price list.

Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

The Am8284 and Am8285 Up/Down Counters consist of four "T" (trigger) flip flops driven synchronously by a buffered clock pulse (CP) input. The flip flop outputs Q_1, Q_2, Q_3, Q_4 and $\overline{Q}_4$ are available.

The outputs change states synchronously on the falling edge of the CP input. Count direction is controlled by a single Up/Down (U/D) input. Count Enable (CE) input, when LOW, inhibits the count mode. Carry In (CI) input, when LOW, inhibits the count mode and forces the Carry Out (CO) output to a LOW state.

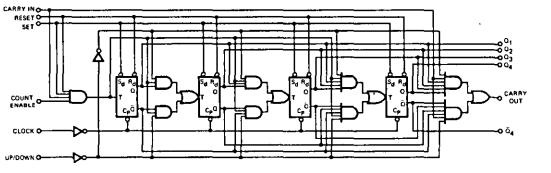
The Am8284 output is in the 8-4-2-1 weighted binary code of 0 through 15. The Am8285 output is in the 8-4-2-1 BCD code of 0 through 9. A HIGH terminal count output, Carry Out (CO), is available when the following conditions are satisfied:

$$CO_{8284} = (CI) \cdot (Q_1Q_2Q_3Q_4UP + \overline{Q}_1\overline{Q}_2\overline{Q}_3\overline{Q}_4\overline{UP})$$
$$CO_{8285} = (CI) \cdot (Q_1\overline{Q}_2\overline{Q}_3Q_4UP + \overline{Q}_1\overline{Q}_2\overline{Q}_3\overline{Q}_4\overline{UP})$$

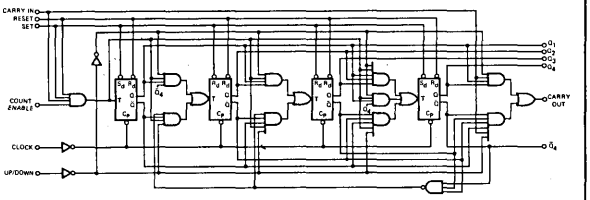
The Set Input LOW sets the Am8284 and Am8285 asynchronously to their respective maximum counts of fifteen (15) and nine (9). Reset Input LOW sets both counters asynchronously to minimum count zero (0). Truth Table I describes the asynchronous and synchronous operating modes for both counters.

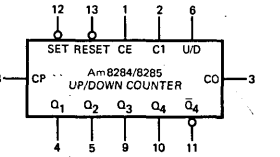
LOGIC DIAGRAMS/SYMBOL

Am8284



Am8285





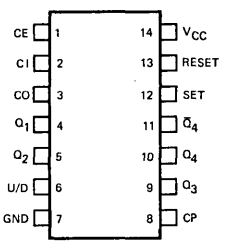
V_{CC} = PIN 8
GND = PIN 7

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
N8284	Hermetic DIP	0°C to +75°C	N8284A
S8284	Hermetic DIP	−55°C to +125°C	S8284A
8284	Dice	Note 10	X8284D
N8285	Hermetic DIP	0°C to +75°C	N8285A
S8285	Hermetic DIP	−55°C to +125°C	S8285A
8285	Dice	Note 10	X8285D

Note 10: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage and Junction Temperature	−65°C to +175°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 14 to Pin 7) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +6.0 V
Output Current, Into Outputs	100 mA
DC Input Current (Note 1)	±30 mA

ELECTRICAL CHARACTERISTICS

N8284/N8285 T_A = 0°C to +75°C
S8284/S8285 T_A = −55°C to +125°C

DC Characteristics (Notes 2, 3, 4)

Parameters	Part No.	Test Conditions	LIMITS −55°C Min	−55°C Max	0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	+125°C Min	+125°C Max	Units
V_{OH}("1") Output HIGH Voltage	All	V_{CC} = 5.0 V, I_{OH} = 20xI_R = −0.5 mA					2.8							
	S8284 S8285	V_{CCL} = 4.75 V, I_{OH} = 20xI_R = −0.5 mA (Refer to Notes 6 and 9)	2.6					3.0				2.6		Volts
	N8284 N8285				2.6			3.0		2.6				
V_{OL}("0") Output LOW Voltage	All	V_{CC} = 5.0 V, I_{OL} = 6xI_F = 9.6 mA							0.4					
	S8284 S8285	V_{CCL} = 4.75 V, I_{OL} = 6xI_F = 9.6 mA (Refer to Note 6)	0.4					0.2					0.4	Volts
	N8284 N8285					0.4		0.2			0.4			
V_{IH}("1") Input HIGH Voltage	S8284 S8285	V_{CCH} = 5.25 V, V_{CCL} = 4.75 V	2.0				2.0					2.0		Volts
	N8284 N8285				2.0		2.0			2.0				
V_{IL}("0") Input LOW Voltage	S8284 S8285	V_{CCH} = 5.25 V, V_{CCL} = 4.75 V		0.8					0.8				0.8	Volts
	N8284 N8285					0.8			0.8				0.8	
I_F("0") Input Load Current (CE,CP,U/D)	S8284 S8285	V_{CCH} = 5.25 V, V_F = 0.4 V		−1.6					−1.6				−1.6	mA
	N8284 N8285					−1.6			−1.6		−1.6			
I_F("0") Input Load Current (CI)	S8284 S8285	V_{CCH} = 5.25 V, V_I = 0.4 V		−3.2					−3.2				−3.2	mA
	N8284 N8285					−3.2					−3.2			
I_F("0") Input Load Current (SET, RESET)	S8284 S8285	V_{CCH} = 5.25 V, V_F = 0.4 V		−6.4					−6.4				−6.4	mA
	N8284 N8285					−6.4					−6.4			
I_R("1") Reverse Input Current (CE,CP,U/D)	S8284 S8285	V_{CCH} = 5.25 V, V_R = 4.5 V		25					25				25	nA
	N8284 N8285					25			25		25			
I_R("1") Reverse Input Current (CI)	S8284 S8285	V_{CCH} = 5.25 V, V_R = 4.5 V		75					75				75	nA
	N8284 N8285					75			75		75			
I_R("1") Reverse Input Current (SET, RESET)	S8284 S8285	V_{CCH} = 5.25 V, V_R = 4.5 V		125					125				125	nA
	N8284 N8285					125			125				125	
LV_{IN} Input Latch Voltage	S8284 S8285 N8284 N8285	V_{CC} = 5.0 V, I_{IN} = 10 mA (Refer to Note 8)					6.0							Volts
I_{SC} Output Short Circuit Current	S8284 S8285 N8284 N8285	V_{CC} = 5.0 V					−20		−70					mA
P_D Power Dissipation	S8284 S8285 N8284 N8285	V_{CCH} = 5.25 V						270	360					mW

Note 1. Maximum current defined by DC Input Voltage.
2. Pulse tested.
3. All voltage and capacitance measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
4. All measurements are taken with ground pin tied to zero volts.
5. Output source current is supplied through a resistor to ground.
6. Output sink current is supplied through a resistor to V_{CC}.
7. One DC fan-out is defined as 0.8 mA.
8. This test guarantees operation free of input latch-up over the specified operating supply voltage range.
9. To set Q_2 and Q_3 HIGH on the 8285, connect Q_4 to CE, momentarily ground SET, and count down. The counter will stop at BCD-7 (0111).

Switching Characteristics	Test Conditions	+25°C Min	Typ	Max	Units
t_{OFF} (Clock to Out) t_{ON} (Clock to Out)	V_{CC} = 5.0 V Refer to Figure 1		20 20		nA nA
t_{OFF} (Set/Reset to Out) t_{ON} (Set/Reset to Out)	V_{CC} = 5.0 V Refer to Figure 2		15 15		nA nA
t_{OFF} (CI to CO) t_{ON} (CI to CO)	V_{CC} = 5.0 V Refer to Figure 3		15 15		nA nA
Count Frequency Clock Min "1" Interval	V_{CC} = 5.0 V	20 20	30 15		MHz ns
Set-Up Time CI, CE, U/D	V_{CC} = 5.0 V		15	25	ns
CI, CE, U/D Release Time	V_{CC} = 5.0 V		0		ns
Set/Reset Hold Time	V_{CC} = 5.0 V		20		ns

DEFINITION OF TERMS

SUBSCRIPT TERMS:

F Forward, applying to LOW inputs.

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to a LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

R Reverse, applying to HIGH inputs.

FUNCTIONAL TERMS:

Asynchronous Inputs Outputs (flip flops) change state on command from these inputs independent of the clock pulse.

CE Count Enable LOW inhibits the counter. Outputs Q_1, Q_2, Q_3, Q_4 and Q_4 remain unchanged.

CI Carry In LOW inhibits the counter and forces Carry Out (CO) to LOW. Outputs Q_1, Q_2, Q_3, Q_4 and $\overline{Q}_4$ remain unchanged.

CO Carry Out output is HIGH whenever Carry In (CI) is HIGH and the counter is either in the "Up" count mode and at maximum count (9 for 8285; 15 for 8284) or in the "Down" count mode and at minimum count of zero.

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

Hold Time The minimum time required for the logic level to be present in order for the outputs to respond.

Input Unit Load In the HIGH state it is equal to I_R and in the LOW state it is equal one half I_F.

Maximum Count The highest number the counter can attain (9 for 8285 and 15 for 8284).

Minimum Count The lowest number the counter can attaain (zero for both counters).

Q_1, Q_2, Q_3, Q_4 Outputs The four TRUE outputs.

$\overline{Q}_4$ Output The FALSE output of the most significant bit.

Reset Input A LOW on this input causes the counter to reset asynchronously to zero. Simultaneous Set and Reset LOW is an undefined condition.

Rd Asynchronous direct Reset Input. A LOW on this input causes output Q to go LOW.

Sd Asynchronous direct Set Input. A LOW on this input causes output Q to go HIGH.

Synchronous Counter All outputs (flip flops) change state on command from the clock.

T (trigger) Flop Flop The flip flop output changes state on the clock pulse when the T input is HIGH. The output remains unchanged when the T input is LOW.

Set Input A low on this input causes the counter to preset asynchronously to maximum count (9 for 8285 and 15 for 8284). Simultaneous Set and Reset LOW is an undefined condition.

U/D (Up/Down) Input This input controls the count direction. A HIGH for up count and a LOW for down count.

OPERATIONAL TERMS:

I_F("0") Forward input load current for unit input load.

Input Latch Voltage The breakdown voltage of an input with other inputs of the same input transistor grounded.

I_{OH} Output HIGH current forced out of output in V_{OH} test.

I_{OL} Output LOW current forced into the output in V_{OL} test.

I_R("1") Reverse input load current with V_R applied to input.

Negative Current Current flowing out of the device.

Output Short Circuit Current The amount of current a HIGH output can source when shorted to ground.

Positive Current Current flowing into the device.

Power Dissipation The product of the worst case supply current and the maximum supply voltage.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{OH}("1") Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL}("0") Maximum logic LOW output voltage with output LOW current I_{OL} into output.

V_F Forward LOW input voltage, for forward input current (I_F) test.

V_R Input reverse HIGH voltage applied for input leakage current (I_R) test.

SWITCHING TERMS: (All switching times are measured at the 1.5 V logic level)

Clock Min "1" Interval The minimum clock pulse width required for proper counter operation.

Count Frequency The maximum clock input frequency allowed for proper counter operation.

Release Time The maximum time allowed for the logic level to be present at the input prior to the clock transition from HIGH to LOW in order for the counter not to respond.

Set Up Time Minimum time required for the logic level to be present at the input prior to the clock transition from HIGH to LOW in order for the counter to respond.

t_{OFF} (Clock to Out) The propagation delay from the clock signal HIGH-LOW transition to an output LOW-HIGH transition.

t_{ON} (Clock to Out) The propagation delay from the clock signal HIGH-LOW transition to an output HIGH-LOW transition.

t_{OFF} (Set/Reset to Out) The propagation delay from the Set or Reset signal HIGH-LOW transition to the output signal LOW-HIGH transition.

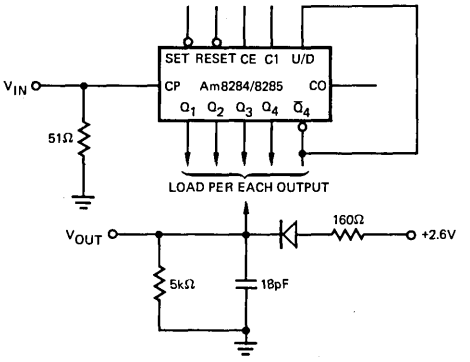
t_{ON} (Set/Reset to Out) The propagation delay from the Set or Reset signal HIGH-LOW transition to the output signal HIGH-LOW transition.

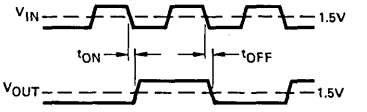
t_{OFF} (CI to CO) The propagation delay from the Carry In signal LOW-HIGH transition to the Carry Out signal transition.

t_{ON} (CI to CO) The propagation delay from the Carry In signal HIGH-LOW transition to the Carry Out signal HIGH-LOW transition.

SWITCHING TIME TEST CIRCUITS/WAVEFORMS

Clock Q Outputs Propagation Delay (t_{ON} and t_{OFF})

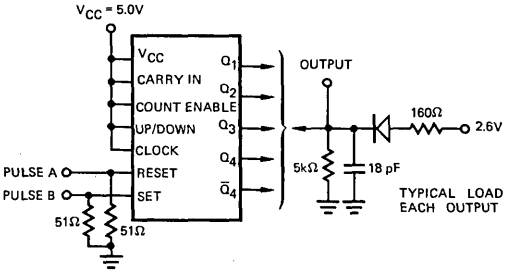


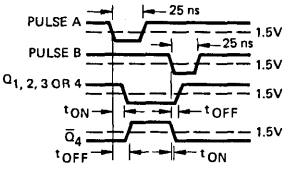


V_{IN} PULSE AMPLITUDE = 2.6V
PULSE WIDTH = 25 ns AT 1.5V
FREQUENCY = 5MHz

Figure 1

Set/Reset Mode (t_{ON} and t_{OFF})

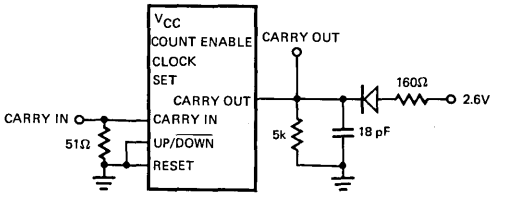


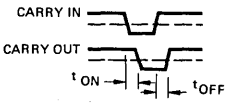


PULSE A AND B
PULSE AMPLITUDE = 2.6V
PULSE WIDTH $_{(0)}$ = 25 ns
FREQUENCY = 5 MHz
$t_R = t_F$ = 5 ns AT 10% TO 90% POINTS

Figure 2

Carry In/Carry Out (t_{ON} and t_{OFF})





CARRY IN PULSE
PULSE AMPLITUDE = 2.6V
PULSE WIDTH $_{(0)}$ = 50 ns
FREQUENCY = 10 MHz
$t_R = t_F$ = 5 ns AT 10% TO 90% POINTS

Figure 3

TRUTH TABLES

Asynchronous	Input Set	Input Reset	Output Q_1	Output Q_2	Output Q_3	Output Q_4
Am8284/8285	1	0	0	0	0	0
Am8284 only	0	1	1	1	1	1
Am8285 only	0	1	1	0	0	1

TABLE I

Synchronous	Input Set	Reset	CI	CE	U/D	Output Function
Am8284/8285	1	1	0	X	X	No Change
Am8284/8285	1	1	X	0	X	No Change
Am8284/8285	1	1	1	1	0	Count Down
Am8284/8285	1	1	1	1	1	Count Up

X = Don't Care

TABLE II

Am8284/85 LOADING RULES

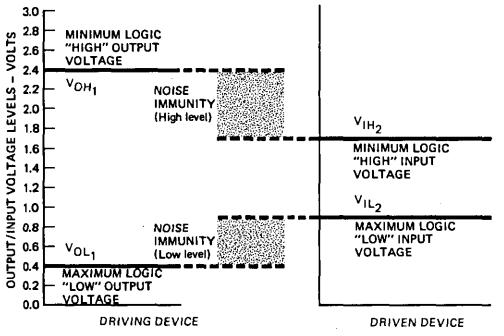
Input/Output	Pin No.'s	Input Unit Load LOW	Input Unit Load HIGH	Fanout Output HIGH	Fanout Output LOW
CE	1	2	1	—	—
CI	2	4	3	—	—
CO	3	—	—	20	12
Q_1	4	—	—	20	12
Q_2	5	—	—	20	12
U/D	6	2	1	—	—
GND	7	—	—	—	—
CP	8	2	1	—	—
Q_3	9	—	—	20	12
Q_4	10	—	—	20	12
Q_4	11	—	—	20	12
Set	12	8	5	—	—
Reset	13	8	5	—	—
V_{CC}	14	—	—	—	—

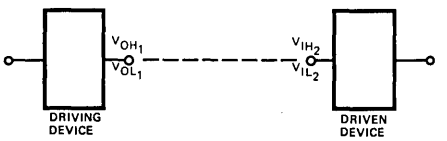
MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	Equivalent Input Unit Load LOW
Advanced Micro Devices Series 9300	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

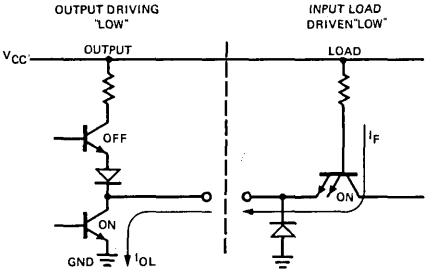
INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH

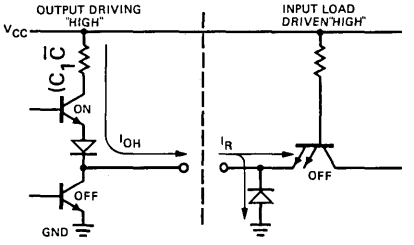




Current Interface Conditions — LOW

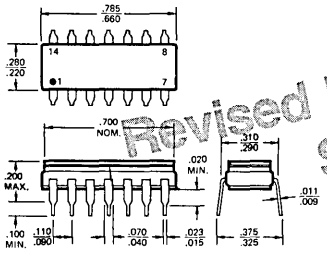


Current Interface Conditions — HIGH

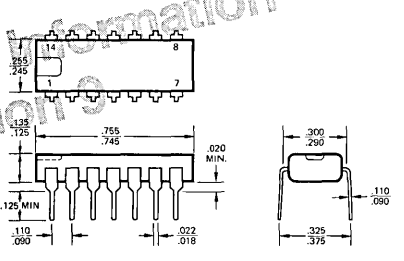


PHYSICAL DIMENSIONS
Dual-In-Line

Hermetic

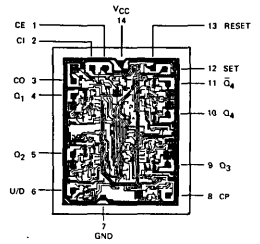


Molded



Metallization and Pad Layout

85 x 107 Mils



ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am9300

Four-Bit Shift Register

Distinctive Characteristics:

- 100% reliability assurance testing including high temperature bake, temperature cycling, centrifuge and package hermeticity testing in compliance with MIL-STD-883.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

The Am9300 Four-Bit Shift Register can be operated in serial or parallel shifting modes. Synchronous shift occurs after the LOW to HIGH transition of the clock pulse (CP) input.

An asynchronous Master Reset (MR) input allows the setting of the four TRUE outputs to LOW, independent of the state of the other inputs.

The Parallel Enable (PE) input selects the operating mode:

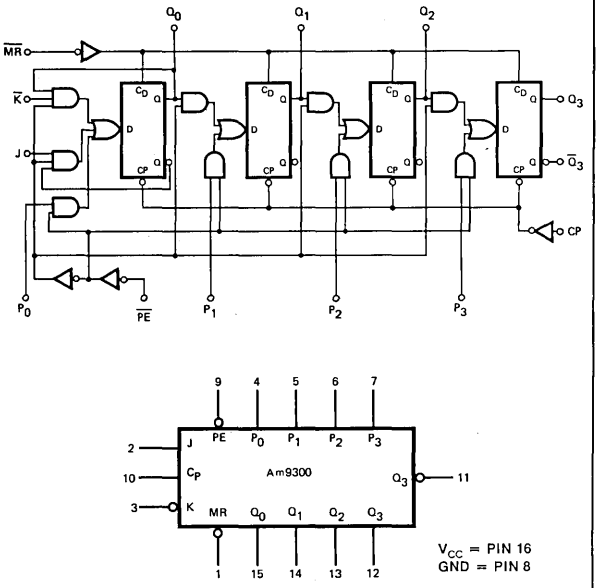
Serial Shifting (Parallel Enable—HIGH)

Data is entered to the register first bit location, Q_0, via the J and $\overline{K}$ inputs synchronous with the Clock Pulse (CP). Data is shifted on consecutive clock pulses to Q_1, to Q_2, to Q_3, and out of the register via Q_3. J and $\overline{K}$ inputs can be operated separately or together as shown in Truth Tables I and II. There are no restrictions of the J or $\overline{K}$ inputs for logic operation ("ones trapping" not possible).

Parallel Shifting (Parallel Enable—LOW)

The register is operated as four synchonous clocked D-type flip-flops as described in Truth Table III. The four D flip-flop inputs are P_0, P_1, P_2 and P_3 and the corresponding four TRUE outputs are Q_0, Q_1, Q_2 and Q_3. The FALSE output $\overline{Q}_3$ of bit four is also provided. Data is entered synchronous with the clock pulse.

LOGIC DIAGRAM/SYMBOL

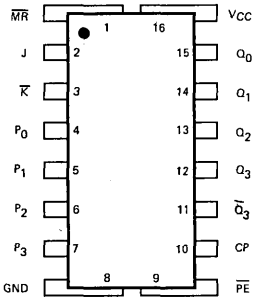


Am9300 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	U6M930059X
Hermetic DIP	0°C to +75°C	U7B930059X
Hermetic DIP	−55°C to +125°C	U7B930051X
Hermetic Flat Pak	−55°C to +125°C	U4L930051X
Dice	Note 1	UXX9300XXD

Note 1: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am930059X T_A = 0°C to +75°C V_{CC} = 4.75 V to 5.25 V
Am930051X T_A = −55°C to +125°C V_{CC} = 4.50 V to 5.50 V

Parameter	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.48 mA Q_{0-3} V_{IN} = V_{IH} or V_{IL} I_{OH} = −0.64 $\overline{Q}_3$		2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V			−1.0	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V			4.0	40	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V		−20		−80	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.	Am930051X		60	86	mA
			Am930059X		60	85	mA

Notes: 1) Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by the input load factor. (See loading rules)

SWITCHING CHARACTERISTICS (T_A = 25°C)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{pd+}	Turn Off Delay (Clock to Q HIGH)	V_{CC} = 5.0 V, C_L = 15 pF	10	20	35	ns
t_{pd-}	Turn On Delay (Clock to Q_{0-2} LOW)		10	20	35	ns
	Turn On Delay (Clock to Q_3 LOW)		12	25	45	ns
CP_{pw}	Min. Clock Pulse Width	V_{CC} = 5.0 V, C_L = 15 pF		15	35	ns
t_s "H"	HIGH Data Set-up Time (J, $\overline{K}$, or P)		0	17	35	ns
t_s "L"	LOW Data Set-up Time (J, $\overline{K}$, or P)		0	17	35	ns
t_s ($\overline{PE}$)	Set-up Time for $\overline{PE}$		10	26	45	ns
t_{pd-} ($\overline{MR}$)	Reset Time ($\overline{MR}$ to Q_3 LOW)		10	35	65	ns
t_{rec} ($\overline{MR}$)	Recovery Time for $\overline{MR}$			20	35	ns
$\overline{MR}_{pw}$	Min. Reset Pulse Width			15	35	ns
f_{sr}	Maximum Shift Right Frequency	V_{CC} = 5.0 V, C_L = 15 pF	15	25		MHz

Note: The "set-up time" is defined as the time required, relative to the clock, for a LOW to HIGH edge (tsH) or a HIGH to LOW edge (tsL) to propagate through internal delays. Logic transitions occurring before ts max are guaranteed to be detected; those occurring after ts min. are guaranteed not to be detected. Transitions between ts max and ts min. may or may not be detected. The minimum set up time for a LOW is sometimes called the "release time" for a HIGH.

)EFINITION OF TERMS

:UBSCRIPT TERMS:

HIGH, applying to a HIGH logic level or when used with V_{CC}) indicate high V_{CC} value.

Input.

LOW, applying to LOW logic level or when used with V_{CC} to dicate low V_{CC} value.

Output.

UNCTIONAL TERMS:

D Input Asynchronous direct clear input.

Input The logic input for the D-type flip-flop.

-Type Flip Flop A delay memory element having a single input nd an output equal to the input one bit-time earlier.

an-Out The logic HIGH or LOW output drive capability in terms f Input Unit Loads.

put Unit Load One T^2L gate input load. In the HIGH state it is qual to I_R and in the LOW state it is equal to I_F.

K Flip Flop Properties similar to an RS Flip Flop except that = K = 1 is allowed. Refer to Truth Table I.

$\overline{K}$ Inputs The logic inputs for setting the Q_0 flip flop of the gister in the JK Mode. Refer to Tables I and II.

$\overline{R}$ Input The master reset input.

$\overline{E}$ Input The input for selection of parallel or serial shifting of the gister. Parallel Enable (PE) LOW selects parallel shifting operation.

, P_1, P_2, P_3 Inputs The inputs for data entry into the four synchro- ous clocked D-Type Flip Flops. Refer to Table III.

$_0$, Q_1, Q_2, Q_3 Outputs The four outputs of the 9300 register flip ops.

$_0$ (t_n) The output after the n'th clock pulse.

$_0$ (t_{n+1}) The output after the (n + 1) clock pulse.

$_3$ Output The inverter output of the Q_3 register flip flop.

PERATIONAL TERMS:

Forward input load current, for unit input load.

H Output HIGH current, forced out of output in V_{OH} test.

L Output LOW current, forced into the output in V_{OL} test.

R Reverse input load current with V_{OH} applied to input.

Negative Current Current flowing out of the device.

I_{CC} The power dissipated within the circuit with input and output terminals open.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage. Refer to figure 4.

V_{IL} Maximum logic LOW input voltage. Refer to figure 4.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

SWITCHING TERMS: (All switching times are measured at the 1.5 V logic level)

CP Clock Pin, pulsed. The subscript, if any, refers to pulse waveshape.

CP_{pw} The minimum clock pulse width required for proper register operation.

f_{sr} The shift right frequency of the register.

$\overline{MR}_{pw}$ The minimum pulse width for resetting the register flip-flops.

t_{pd-} The propagation delay from the clock signal LOW-HIGH transition to an output signal HIGH-LOW transition.

t_{pd+} The propagation delay from the clock signal LOW-HIGH transition to an output signal LOW-HIGH transition.

$t_{pd-}(\overline{MR})$ The propagation delay from the master reset signal HIGH-LOW transition to the TRUE output signal HIGH-LOW transition. Refer to Figure 2.

$t_{rec}(\overline{MR})$ Recovery time for MR defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order for the flip flop(s) to respond to the clock.

t_s Set-up time defined as the time required for the logic level to be present at the data inputs prior to the clock transition from LOW to HIGH in order for the flip flop(s) to respond. Good data should be present at all times between t_s max and t_s min.

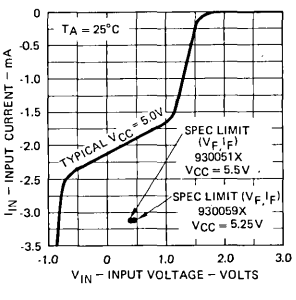
$t_s(\overline{PE})$ Set-up time for the Parallel Enable is defined as the time required for the logic level to be present at the Parallel Enable ($\overline{PE}$) prior to the clock transition from LOW to HIGH in order for the flip flop(s) to respond.

PERFORMANCE CURVES

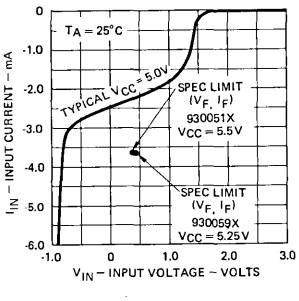
Input Characteristics

Input Current Versus Input Voltage

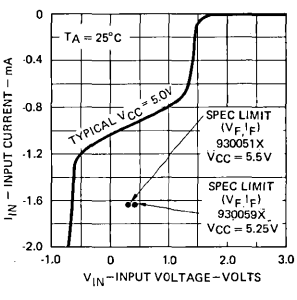
CP



$\overline{PE}$



$\overline{MR}$, J, $\overline{K}$, P_0, P_1, P_2, & P_3

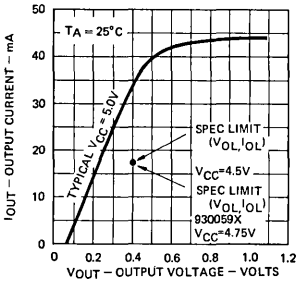


Output Characteristics

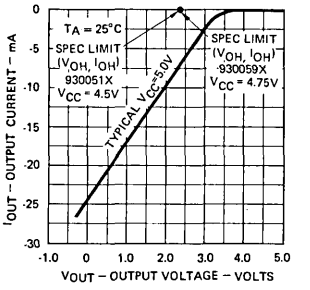
Output Current Versus Output Voltage

(Q_0, Q_1, Q_2, Q_3)

Low State

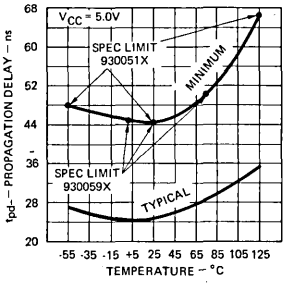


High State

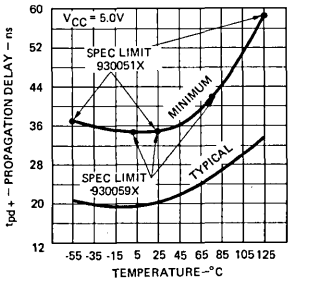


Switching Characteristics

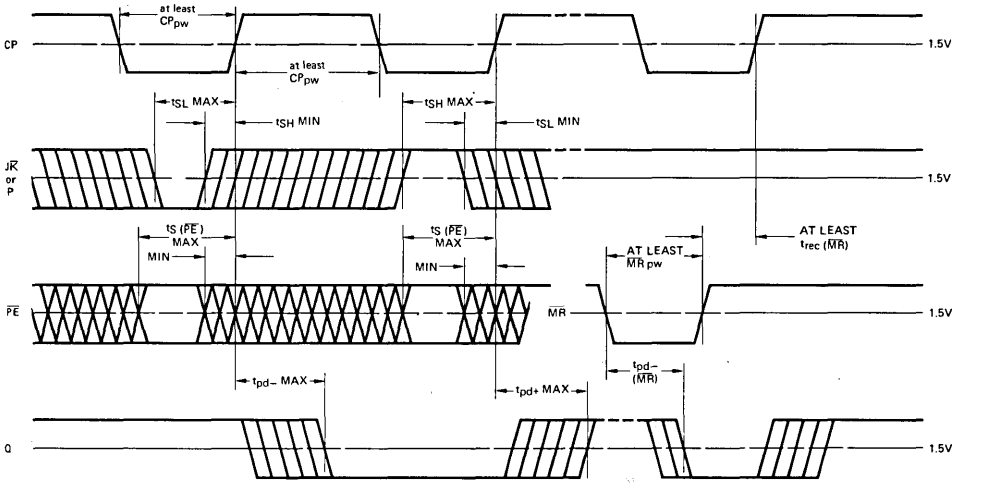
Turn On Delay Clock To Q_3 Output Vs Temperature



Turn Off Delay Clock To Q_3 Output Vs Temperature



SWITCHING TIME WAVEFORMS



TRUTH TABLES

Serial Shift (Parallel Enable — HIGH)
K Input — Active LOW

J	$\overline{K}$	Q_0 (t_{n+1})
L	L	L
L	H	Q_0 (t_n) no change
H	L	Q_0 (t_n) toggle
H	H	H

Table I

J&$\overline{K}$ Connected	$Q_0(t_{n+1})$
L	L
H	H

Table II

Parallel Shift (Parallel Enable — LOW)

D-Input (P_0, P_1, P_2 or P_3)	Output Q (t_{n+1}) (Q_0, Q_1, Q_2 or Q_3)
L	L
H	H

Table III

Mode Selection

	$\overline{PE}$	P_0	P_1	P_2	P_3	J	$\overline{K}$	$\overline{MR}$
Serial Shift	H	X	X	X	X	Refer to Table I & II		H
Parallel Shift	L	Refer to Table III				X	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Am9300 LOADING RULES (in unit loads)

Input/Output	Pin No.'s	Input Unit Load	Output Drive (Note) Output HIGH	Output LOW
$\overline{MR}$	1	1	—	—
J	2	1	—	—
$\overline{K}$	3	1	—	—
P_0	4	1	—	—
P_1	5	1	—	—
P_2	6	1	—	—
P_3	7	1	—	—
GND	8	—	—	—
$\overline{PE}$	9	2.3	—	—
CP	10	2	—	—
$\overline{Q}_3$(F)	11	—	16	10
Q_3	12	—	12	10
Q_2	13	—	12	10
Q_1	14	—	12	10
Q_0	15	—	12	10
V_{CC}	16	—	—	—

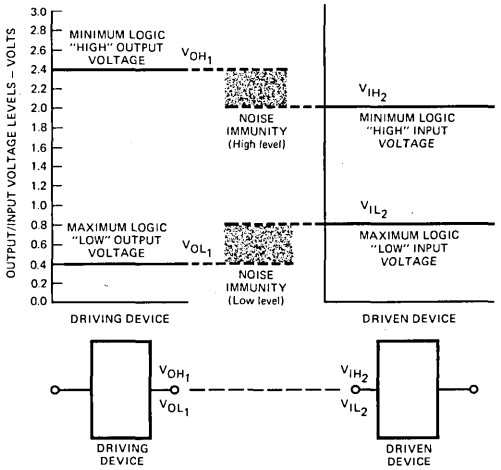
Note: 10 loads are allowed on any output, but the total number of loads on all outputs must not exceed 30. A unit load is defined as 40μA at 2.4V and 1.6mA at 0.4V.

MSI INTERFACING RULES

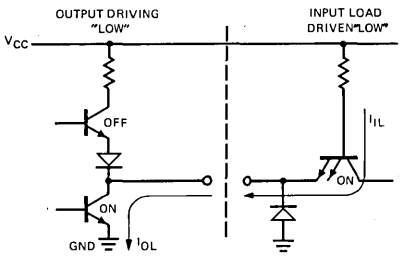
Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH



Current Interface Conditions — LOW



Current Interface Conditions — HIGH

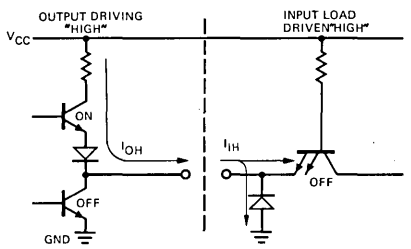
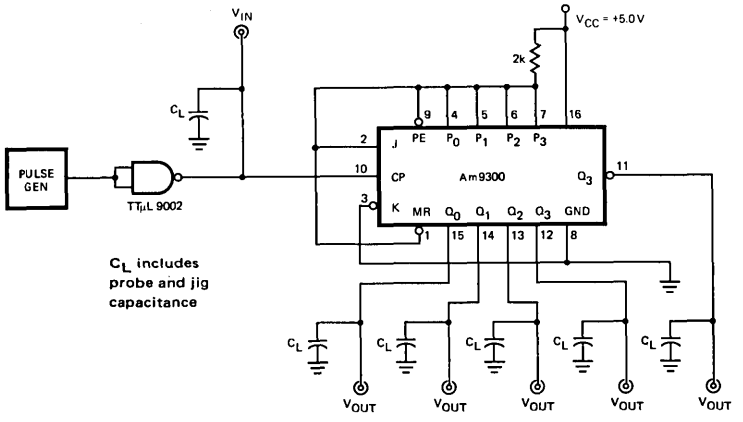


Figure 4

SWITCHING TIME & SHIFT RIGHT FREQUENCY TEST CIRCUIT



C_L includes probe and jig capacitance

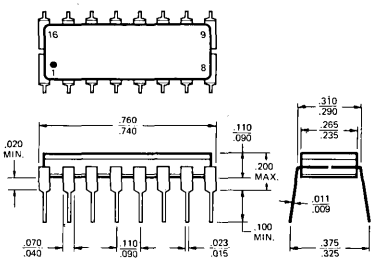
Pulse Generator Output

1. Switching Time (t_{pd+} & t_{pd-}) Tests
   Rise Time $<$15 ns
   Fall Time $<$15 ns
   Amplitude $\simeq$ 4V
   Freq. = 2 MHz with pulse width adjustment so that V_{IN} has duty cycle of approx. 50%.
2. Shift Right Frequency Test
   Rise Time $<$15 ns
   Fall Time $<$ 15 ns
   Amplitude $\simeq$ 4V
   Freq. = 15 MHz with pulse width adjustment so that V_{IN} has duty cycle of approx. 50%.

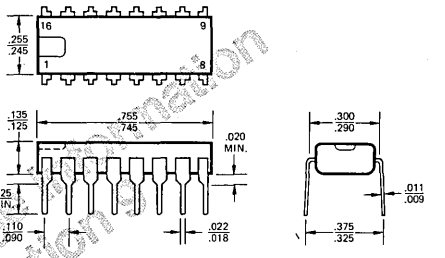
Figure 5

PHYSICAL DIMENSIONS
Dual-In-Line

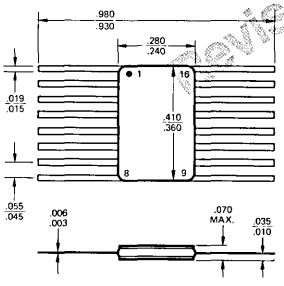
Hermetic



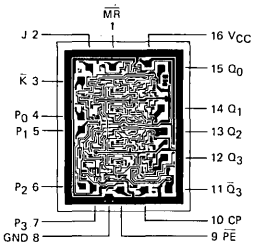
Molded



Flat Package



Metallization and Pad Layout



74 x 96 Mils

ADVANCED MICRO DEVICES INC.
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Am93L00
Low-Power Four-Bit Shift Register

Distinctive Characteristics

- 75 mW typical power dissipation
- 10 MHz typical shift rate
- 100% reliability assurance testing in compliance with MIL STD 883
- Fully synchronous shifting and loading

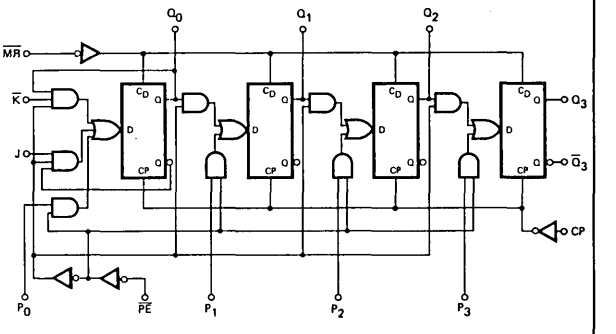
FUNCTIONAL DESCRIPTION

The Am93L00 is a four-bit universal register consisting of four D-type master-slave flip-flops. The flip-flops are all clocked by C_P, accepting data into the masters when C_P is LOW and transferring data to the slaves when C_P is HIGH.

The outputs of the four flip-flops are Q_0, Q_1, Q_2, and Q_3. A complemented output of Q_3 is also provided. Data enters the flip-flops synchronously from either of two sources, depending on the state of the parallel enable ($\overline{PE}$). When $\overline{PE}$ is LOW, then each flip-flop accepts data from its corresponding P input (P_0, P_1, P_2, and P_3). When $\overline{PE}$ is HIGH, a right shift occurs, with the last three flip-flops accepting data from the flip-flops on their left and the first flip-flop accepting data via the J and $\overline{K}$ inputs. The J and $\overline{K}$ inputs may be tied together to form a single D input to the first stage. A synchronous master reset ($\overline{MR}$) forces all flip-flops to the "0" state (outputs LOW) regardless of any other inputs.

The 93L00 may be used as a parallel to serial converter, a serial to parallel converter, a left/right shift register (by tying Q_n to P_{n-1}), a four-bit counter, or as four D flip-flops.

LOGIC DIAGRAM



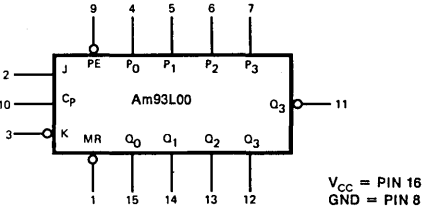
LOADING RULES

In Unit Loads (Notes)

Input Loading	TTL Loads HIGH	TTL Loads LOW	93L Loads HIGH	93L Loads LOW
J, $\overline{K}$, P_0, P_1, P_2, P_3, $\overline{MR}$	0.5	0.25	1.0	1.0
C_P	1.0	0.5	2.0	2.0
$\overline{PE}$	1.15	0.575	2.3	2.3
Output Drive	HIGH	LOW	HIGH	LOW
All Outputs	9	3	18	12

NOTES:
1) A TTL unit load is specified as 0.4 V at −1.6 mA LOW, 2.4 V at 40 μA HIGH.
2) A 93L unit load is specified as 0.3 V at −400 μA LOW, 2.4 V at 20 μA HIGH.
3) Enough output LOW current is available to mix TTL and 93L loads and still meet the 93L requirement of a V_{OL} of 0.3 V.

LOGIC SYMBOL



Am93L00 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
16-Pin Molded DIP	0°C to +75°C	U6M93L0059X
16-Pin Hermetic DIP	0°C to +75°C	U7B93L0059X
16-Pin Hermetic DIP	−55°C to +125°C	U7B93L0051X
16-Pin Hermetic Flat Pak	−55°C to +125°C	U4L93L0051X
Dice	Note	UXX93L00XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to $+V_{CC}$ max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current (Note 1)	−30 mA to +5.0 mA

Note 1. Maximum current defined by DC input voltage.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93L0059X T_A = 0°C to +75°C V_{CC} = 4.75 V to 5.25 V
Am93L0051X T_A = −55°C to +125°C V_{CC} = 4.50 V to 5.50 V

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.36 mA V_{IN} = V_{IH} or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 4.92 mA V_{IN} = V_{IH} or V_{IL}		0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.7	Volts
I_{IL} (Note 2)	93L Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.3 V		−0.25	−0.4	mA
I_{IH} (Note 2)	93L Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V		2.0	20	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V	−2.5	−16	−25	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		15	23	mA

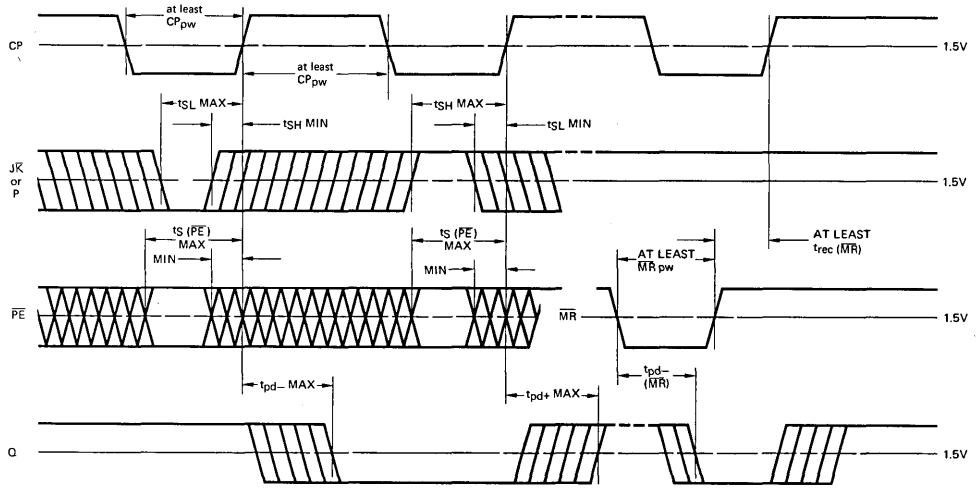
Notes: 1) Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by the 93L input load factor. (See loading rules)

SWITCHING CHARACTERISTICS (T_A = 25°C)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{pd+}	Turn Off Delay (Clock to Q_3 HIGH)	V_{CC} = 5.0 V, C_L = 15 pF	28	55	65	ns
t_{pd-}	Turn On Delay (Clock to Q_3 LOW)		33	65	75	ns
CP_{pw}	Min. Clock Pulse Width	V_{CC} = 5.0 V, C_L = 15 pF	25	50	60	ns
t_s "H"	HIGH Data Set-up Time (J, $\overline{K}$, or P)		35	55	85	ns
t_s "L"	LOW Data Set-up Time (J, $\overline{K}$, or P)		20	30	50	ns
t_s ($\overline{PE}$)	Set-up Time for $\overline{PE}$			70	110	ns
t_{pd-} ($\overline{MR}$)	Reset Time ($\overline{MR}$ to Q_3 LOW)		40	80	100	ns
t_{rec} ($\overline{MR}$)	Recovery Time for $\overline{MR}$		28	55	80	ns
$\overline{MR}_{pw}$	Min. Reset Pulse Width		25	50	70	ns
f_{sr}	Maximum Shift Right Frequency	V_{CC} = 5.0 V, C_L = 15 pF	5	10		MHz

Note: The "set-up time" is defined as the time required, relative to the clock, for a LOW to HIGH edge (tsH) or a HIGH to LOW edge (tsL) to propagate through internal delays. Logic transitions occurring before ts max are guaranteed to be detected; those occurring after ts min. are guaranteed not to be detected. Transitions between ts max and ts min. may or may not be detected. The minimum set up time for a LOW is sometimes called the "release time" for a HIGH.

SWITCHING TIME WAVEFORMS



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Am9301

Demultiplexer/One-of-Ten Decoder

Distinctive Characteristics:

- 22 ns typical propagation delay
- Does not respond to codes above 9
- 100% reliability assurance testing in compliance with MIL-STD-883
- Can be used as one-of-eight decoder with active LOW enable

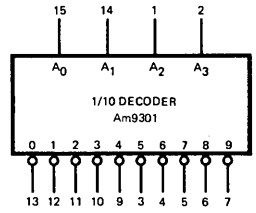
FUNCTIONAL DESCRIPTION

The Am9301 Demultiplexer/One-of-Ten Decoder accepts four active High BCD inputs and selects one-of-ten mutually exclusive active LOW outputs as shown in Truth Table II. The logic design of the 9301 insures that all outputs are HIGH (unselected) when binary codes greater than nine are applied to the inputs. The inputs A_0, A_1, A_2, and A_3 of the 9301 correspond to the respective binary weight of 2^0, 2^1, 2^2, and 2^3.

Incoming data on input A_3, can be demultiplexed to either of the eight outputs, zero through seven, with binary addressing at inputs A_0, A_1, and A_2. This demultiplexing capability is illustrated in figure 5.

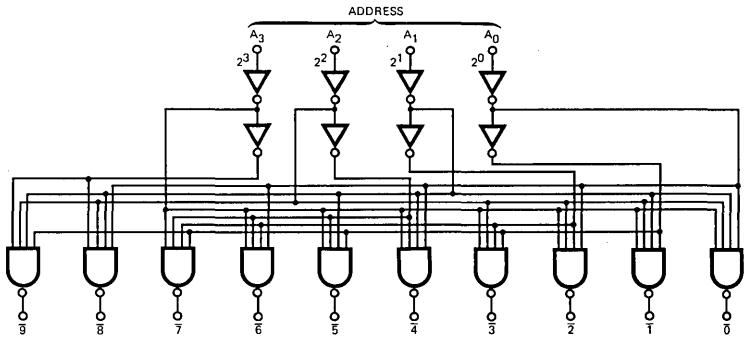
The most significant input, A_3, produces an inhibit function when the 9301 is used as a 1-of-8 decoder with binary addressing at inputs A_0, A_1, and A_2. The 1-of-32 decoder, in figure 6 illustrates the inhibit function.

LOGIC SYMBOL



V_{CC} = Pin 16
Gnd = Pin 8

LOGIC DIAGRAM



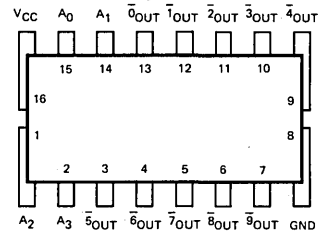
Am9301 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
16-pin Molded DIP	0°C to +75°C	U6M930159X
16-pin Hermetic DIP	0°C to +75°C	U7B930159X
16-pin Hermetic DIP	−55°C to +125°C	U7B930151X
16-pin Hermetic Flat Pak	−55°C to +125°C	U4L930151X
Dice	Note	UXX9301XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM

Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

930159X T_A = 0°C to +75°C V_{CC} = 5.0 V ±5%
930151X T_A = −55°C to +125°C V_{CC} = 5.0 V ±10%

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.8 mA V_{IN} = V_{IH} or V_{IL}		2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16.0 mA V_{IN} = V_{IH} or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V			−1.0	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V			6.0	40	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V		−20		−70	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.	930151X		27	44	mA
			930159X		27	42	

Notes: 1) Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by input load factor (see Loading Rules).

Switching Characteristics (+25°C)

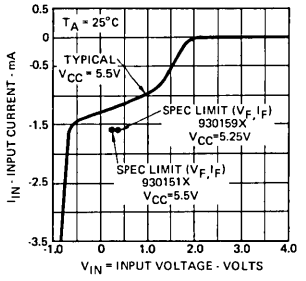
Parameters		Test Conditions	Min	Typ	Max	Units
t_{pd+}	Turn Off Delay	V_{CC} = 5.0, C_L = 15 pF	10	23	35	ns
t_{pd-}	Turn On Delay	Refer to figure 4.	10	20	30	ns

Note 1. Maximum current defined by DC Input Voltage.
2. Pulse tested.

PERFORMANCE CURVES

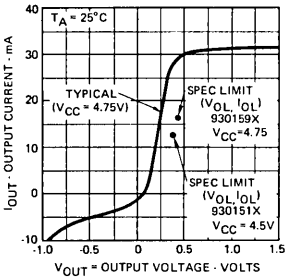
Input/Output Characteristics

Input

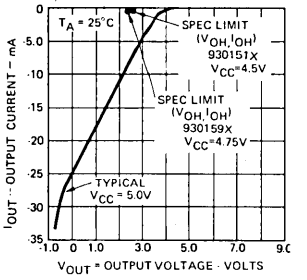


Output

Low State

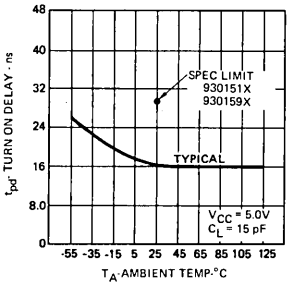


High State

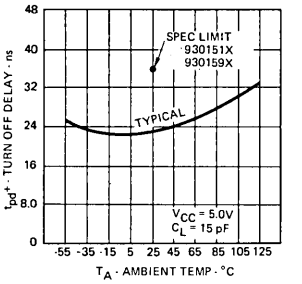


Switching Characteristics

Turn On Delay Time



Turn Off Delay Time



EFINITION OF TERMS

UBSCRIPT TERMS:

HIGH, applying to a HIGH-signal level or when used with V_{CC} indicate high V_{CC} value.

Input.

LOW, applying to a LOW signal level or when used with V_{CC} to dicate low V_{CC} value.

Output.

UNCTIONAL TERMS:

CD Binary coded decimal notation represents each of the ten ecimal digits by a code consisting of a group of four (4) binary igits.

ecoder/Demultiplexer On the basis of an applied instruction, hannels of communication are selected which connect certain ources of information to certain destinations e.g., the distribution f timing signals; the interconnection between arithmetic registers.

an-Out The logic HIGH or LOW output drive capability in terms f Input Unit Loads.

nit load One T^2L gate input load. In the HIGH state it is equal to 0μA at 2.4V and in the LOW state it is equal to −1.6mA at 0.4V.

OPERATIONAL TERMS:

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into output in V_{OL} test.

I_{CC} The current drawn by the device under a +5.0 V power supply, bias input terminals grounded and output terminals open.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

SWITCHING TERMS: (All switching times are measured at the 1.5V logic level).

t_{pd+} The propagation delay measured from the input address transition to a corresponding output signal LOW-HIGH transition.

t_{pd-} The propagation delay measured from the input address transition to a corresponding output signal HIGH-LOW transition.

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
Advanced Micro Devices 54/7400 Series	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

TRUTH TABLE

INPUTS				OUTPUTS									
A_4	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

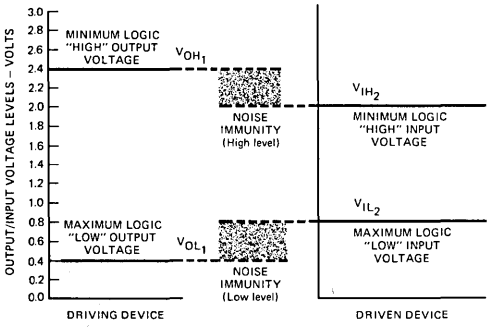
H = HIGH Logic Level
L = LOW Logic Level

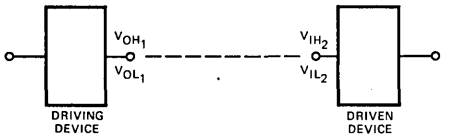
LOADING RULES

Input/Output	Pin No.'s	Input Unit Load	Fanout Output HIGH	Fanout Output LOW
A_2	1	1	—	—
A_3	2	1	—	—
$\overline{5}_{OUT}$	3	—	20	10
$\overline{6}_{OUT}$	4	—	20	10
$\overline{7}_{OUT}$	5	—	20	10
$\overline{8}_{OUT}$	6	—	20	10
$\overline{9}_{OUT}$	7	—	20	10
GND	8	—	—	—
$\overline{4}_{OUT}$	9	—	20	10
$\overline{3}_{OUT}$	10	—	20	10
$\overline{2}_{OUT}$	11	—	20	10
$\overline{1}_{OUT}$	12	—	20	10
$\overline{0}_{OUT}$	13	—	20	10
A_1	14	1	—	—
A_0	15	1	—	—
V_{CC}	16	—	—	—

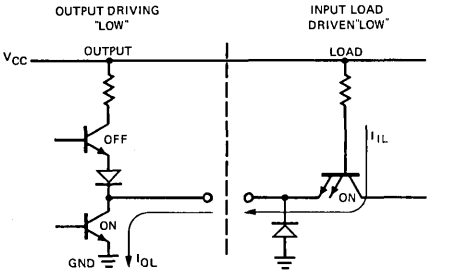
INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH

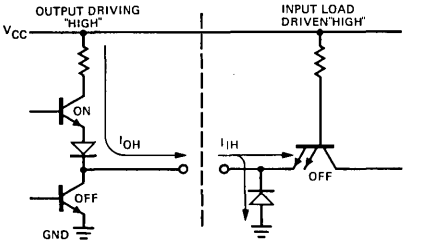




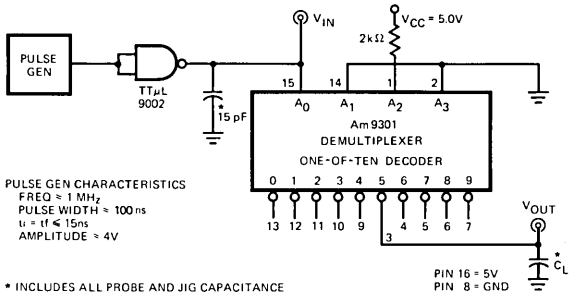
Current Interface Conditions — LOW



Current Interface Conditions — HIGH

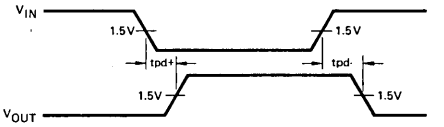


SWITCHING TIME TEST CIRCUITS & WAVEFORMS



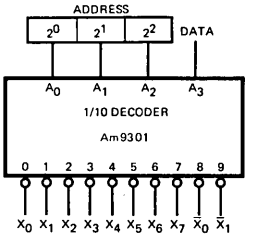
PULSE GEN CHARACTERISTICS
FREQ ≈ 1 MHz
PULSE WIDTH ≈ 100 ns
$t_r = t_f \leq 15$ns
AMPLITUDE ≈ 4V

* INCLUDES ALL PROBE AND JIG CAPACITANCE



BASIC DEMULTIPLEXER/DECODER APPLICATIONS

DIGITAL DEMULTIPLEXER



ADDRESS A_0 A_1 A_2	OUTPUT LINE
0 0 0	0
1 0 0	1
0 1 0	2
1 1 0	3
0 0 1	4
1 0 1	5
0 1 1	6
1 1 1	7

Data may be routed from a source to any of eight (0–7) outputs by addressing that output. The seven non-addressed outputs remain clear.

Figure 5

ADDITIONAL APPLICATIONS

ONE-OUT-OF-THIRTY-TWO DECODER

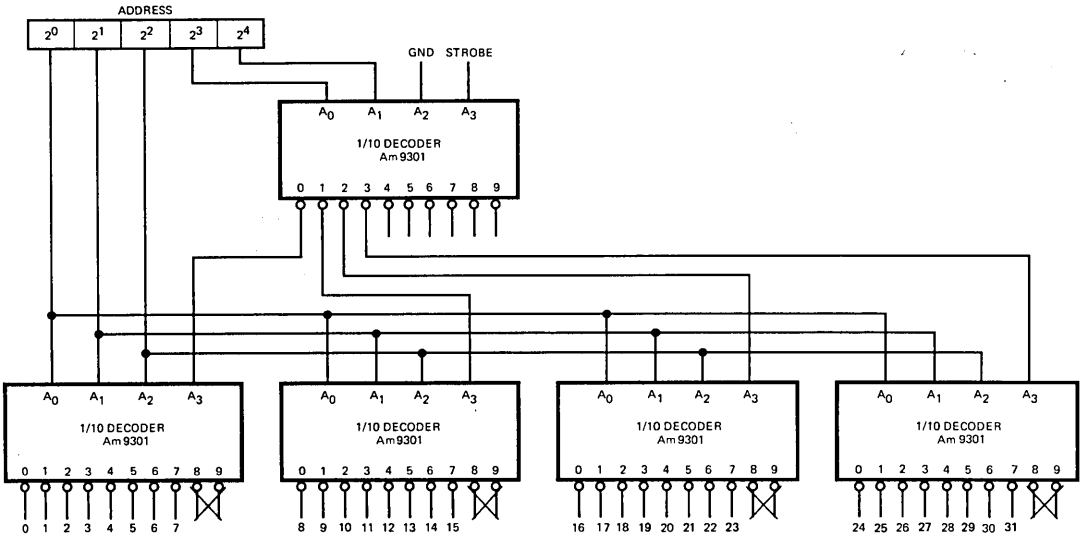
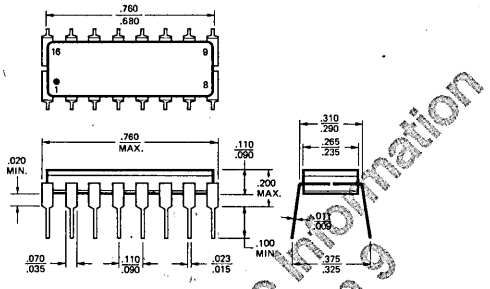


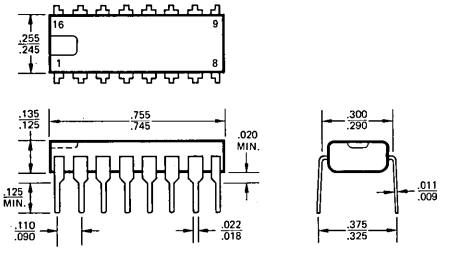
Figure 6

PHYSICAL DIMENSIONS

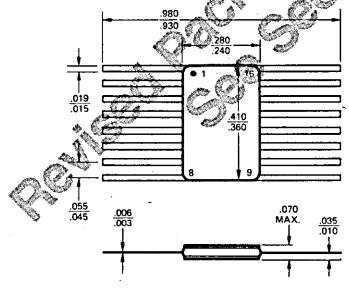
Hermetic Dual-In-Line



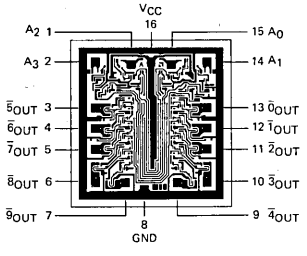
Molded



Flat Package



Metallization and Pad Layout



75 x 79 Mils

ADVANCED
MICRO
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TWX: 910-339-9280
TELEX: 34-6306

Am93L01

Low-Power Demultiplexer/One-of-Ten Decoder

Distinctive Characteristics

45 mw typical power dissipation.

50 ns typical propagation delay.

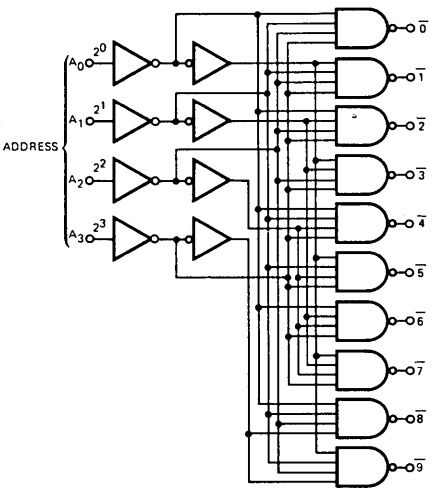
- 100% reliability assurance testing in compliance with MIL STD 883
- Fan-out of three to standard TTL circuits.

FUNCTIONAL DESCRIPTION

The Am93L01 low-power decoder accepts a four-bit binary address and selects one-of-ten mutually exclusive active LOW outputs. The outputs are designated by the decimal equivalent of the binary code which selects them. Non-selected outputs are HIGH, and if the input code is greater than nine all outputs are HIGH.

Since codes greater than nine do not select any output, the 93L01 can be used as a one-of-eight decoder with an enable. The three-bit code is applied to inputs A_0, A_1, and A_2. If A_3 is LOW, one of the outputs 0 through 7 will go LOW; if A_3 is HIGH, then either output 8 or 9, or none of the outputs will go LOW. Hence, input A_3 becomes an active LOW enable for a one-of-eight decoder. The device can also be used as a demultiplexer by applying data to input A_3 and an address to inputs A_0, A_1, and A_2. The addressed output will follow the data on A_3.

LOGIC DIAGRAM



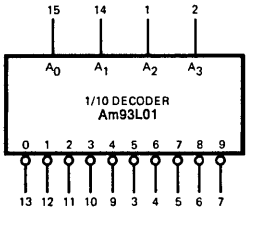
LOADING RULES

In Unit Loads (Notes)

Input loading	TTL loads HIGH	TTL loads LOW	93L loads HIGH	93L loads LOW
All Inputs	0.5	0.25	1.0	1.0
Output Drive	HIGH	LOW	HIGH	LOW
All Outputs	10	3	12	12

NOTES:
1) A TTL unit load is specified as 0.4 V at −1.6 mA LOW, 2.4 V at 40 μA HIGH.
2) A 93L unit load is specified as 0.3 V at −400 μA LOW, 2.4 V at 20 μA HIGH.
3) Enough output LOW current is available to mix TTL and 93L loads and still meet the 93L requirement of a V_{OL} of 0.3 V.

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

Am93L01 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
16-Pin Molded DIP	0°C to +75°C	U6M93L0159X
16-Pin Hermetic DIP	0°C to +75°C	U7B93L0159X
16-Pin Hermetic DIP	−55°C to +125°C	U7B93L0151X
16-Pin Hermetic Flatpak	−55°C to +125°C	U4L93L0151X
Dice	Note	UXX93L01XXD

Revised Ordering Information See Section 9

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current (Note 1)	−30 mA to +5.0 mA

Note 1. Maximum current defined by DC input voltage.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93L0159X T_A = 0°C to +75°C V_{CC} = 4.75 V to 5.25 V
Am93L0151X T_A = −55°C to +125°C V_{CC} = 4.50 V to 5.50 V

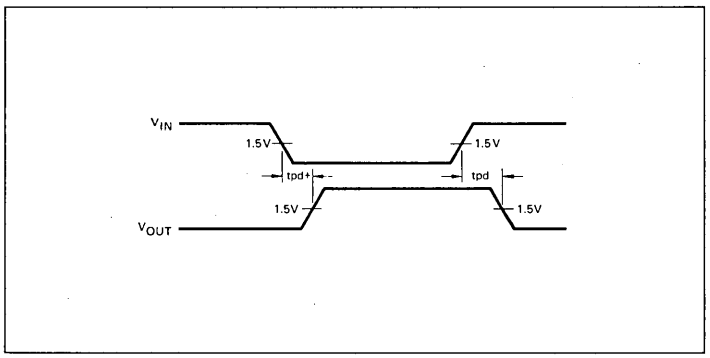
Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 4.92 mA V_{IN} = V_{IH} or V_{IL}		0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.7	Volts
I_{IL} (Note 2)	93L Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.3 V		−0.25	−0.4	mA
I_{IH} (Note 2)	93L Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V		2.0	20	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V	−2.5	−16	−25	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		9.0	13	mA

Notes: 1) Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by the 93L input load factor. (See loading rules)

SWITCHING CHARACTERISTICS (T_A = 25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{pd+}	Delay Address to Output HIGH	V_{CC} = 5.0 V	20	48	65	ns
t_{pd-}	Delay Address to Output LOW	C_L = 15 pF	20	50	70	ns

SWITCHING TIME WAVEFORMS



ADVANCED
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TELEX: 34-6306

Am9304
Dual Full Adder

Distinctive Characteristics: 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and package hermeticity testing in compliance with MIL-STD-883.

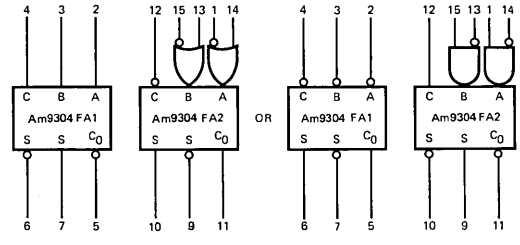
Mixing privileges for obtaining price discounts. Refer to price list.

Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

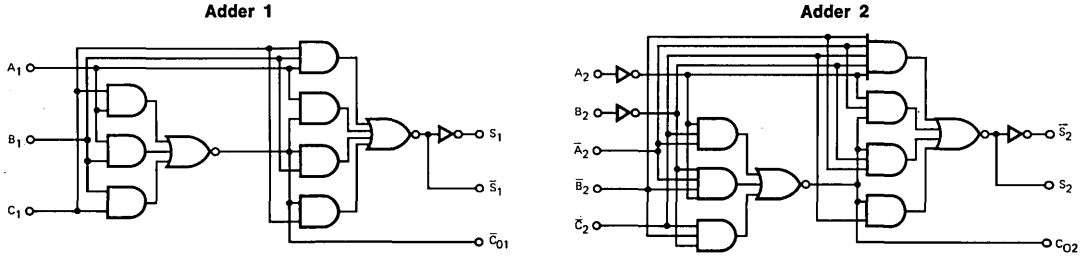
The Am9304 Dual Full Adder is two carry dependent sum full adders. In ripple-carry applications the propagation delay has been minimized. Adder FA2 has provision for active HIGH or active LOW inputs. The adders produce a LOW carry and both LOW and HIGH sum with active HIGH inputs. A HIGH carry and HIGH & LOW sum are produced when active LOW inputs are used. This duality is shown in the logic symbols. The Am9304 is also a logically powerful gating element as illustrated under applications. The logical representation of the Am9304 is shown in Truth Tables I and II.

LOGIC SYMBOLS



V_{CC} = PIN 16
GND = PIN 8

LOGIC DIAGRAM

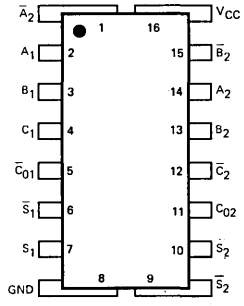


Am9304 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	U6M930459X
Hermetic DIP	0°C to +75°C	U7B930459X
Hermetic DIP	−55°C to +125°C	U7B930451X
Flat Pak	−55°C to +125°C	U4L930451X
Dice	Note	UXX9304XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs for Low Output State	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am930459X $T_A = 0°C$ to $+75°C$ $V_{CC} = 5.0\ V \pm 5\%$
Am930451X $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0\ V \pm 10\%$

Parameters	Description	Test Conditions	Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.8 mA $\overline{S}$, S $V_{IN} = V_{IH}$ or V_{IL}, I_{OH} = −0.56 mA $\overline{C}$, C	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16.0 mA $\overline{S}$, S $V_{IN} = V_{IH}$ or V_{IL}, I_{OL} = 11.2 mA $\overline{C}$, C		0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V		−1.0	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V		6.0	40	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V	−30	− 60	−100	mA
I_{CC}	Power Supply Current	A_2, B_2 (Pins 13, 14 = 0.0 V) V_{CC} = MAX.		34	55	mA

Notes: 1) Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by input load factor (See Loading Rules).

SWITCHING CHARACTERISTICS (T_A = 25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
$t_{pd+}(C_1\overline{C}_{01})$	C_1 to $\overline{C}_{01}$ (see definitions)	V_{CC} = 5.0V, C_L = 15 pF	4	8	15	ns
$t_{pd-}(C_1\overline{C}_{01})$	C_1 to $\overline{C}_{01}$ (see definitions)		4	8	15	ns
$t_{pd+}(A_1\overline{S}_1)$	A_1 to $\overline{S}_1$ (see definitions)		4	16	25	ns
$t_{pd-}(A_1\overline{S}_1)$	A_1 to $\overline{S}_1$ (see definitions)		4	16	25	ns
$t_{pd+}(A_1S_1)$	A_1 to S_1 (see definitions)		8	21	30	ns
$t_{pd-}(A_1S_1)$	A_1 to S_1 (see definitions)		8	21	30	ns
$t_{pd+}(\overline{A}_2S_2)$	$\overline{A}_2$ to S_2 (see definitions)		4	16	25	ns
$t_{pd-}(\overline{A}_2S_2)$	$\overline{A}_2$ to S_2 (see definitions)		4	16	25	ns
$t_{pd+}(A_2\overline{S}_2)$	A_2 to $\overline{S}_2$ (see definitions)		12	26	40	ns
$t_{pd-}(A_2\overline{S}_2)$	A_2 to $\overline{S}_2$ (see definitions)		12	26	40	ns
$t_{pd+}(A_2S_2)$	A_2 to S_2 (see definitions)		8	21	30	ns
$t_{pd-}(A_2S_2)$	A_2 to S_2 (see definitions)		8	21	30	ns
$t_{pd+}(C_2C_{02})$	$\overline{C}_2$ to C_{02} (see definitions)		4	8	15	ns
$t_{pd-}(C_2C_{02})$	$\overline{C}_2$ to C_{02} (see definitions)		4	8	15	ns

)EFINITION OF TERMS

UBSCRIPT TERMS:

Forward, applying to LOW inputs.

HIGH, applying to a HIGH logic level or when used with V_{CC} to idicate high V_{CC} value.

Input.

LOW, applying to LOW logic level or when used with V_{CC} to dicate low V_{CC} value.

Output.

Reverse, applying to HIGH inputs.

UNCTIONAL TERMS:

$_1$, B_1 **Inputs** The TRUE data inputs for Adder FA1.

$_2$, $\overline{A}_2$, B_2, $\overline{B}_2$ **Inputs** The TRUE and FALSE data inputs for Adder A2.

$_1$, $\overline{C}_2$ **Inputs** The Carry or 3rd data input for Adders FA1 and A2.

$_{01}$ **Output** The FALSE Carry Output for Adder FA1.

$_{02}$ **Output** The TRUE Carry Output for Adder FA2.

an-Out The logic HIGH or LOW output drive capability in terms Input Unit Loads.

put Unit Load One T^2L gate input load. In the HIGH state it is qual to I_R and in the LOW state it is equal to I_F.

ipple Carry Parallel Adder The sum of two binary numbers is rmed one bit time after the presence of these data at the adder puts. The bit time is chosen to allow the carry term to propagate om the least significant addition to the most significant addition. efer to Figure

$_1$, S_2 **Output** The TRUE Sum Outputs for Adders FA1 and FA2.

$_1$, $\overline{S}_2$ **Output** The FALSE Sum Outputs for Adders FA1 and FA2.

PERATIONAL TERMS:

Forward input load current, for unit input load.

$_{IH}$ Output HIGH current, forced out of output in V_{OH} test.

$_{IL}$ Output LOW current, forced into the output in V_{OL} test.

Reverse input current with V_R applied to input.

$_D$ The current drawn by the device under maximum power supply perating voltage and current conditions.

egative Current Current flowing out of the device.

ositive Current Current flowing into the device.

$_F$ Forward LOW input voltage, for forward input current (I_F) test.

$_{IH}$ Minimum logic HIGH input voltage.

$_{IL}$ Maximum logic LOW input voltage.

$_{OH}$ Minimum logic HIGH output voltage with output HIGH current $_{OH}$ flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

V_R Input reverse HIGH voltage applied for input leakage current, (I_R) test.

SWITCHING TERMS: (All switching times are measured at the 1.5 V logic level)

$t_{pd+}(CC_0)$ The propagation delay measured from the Carry Input signal transition of either adder to the corresponding LOW-HIGH transition of the Carry Output signal.

$t_{pd-}(CC_0)$ The propagation delay measured from the Carry Input signal transition of either adder to the corresponding HIGH-LOW transition of the Carry Output signal.

$t_{pd+}(A_1\overline{S}_1)$ The propagation delay measured from Adder 1 A or B Data Input signal transition to the LOW-HIGH transition of the FALSE Sum Output signal.

$t_{pd-}(A_1\overline{S}_1)$ The propagation delay measured from Adder 1 A or B Data Input signal transition to the HIGH-LOW transition of the FALSE Sum Output signal.

$t_{pd+}(A_1S_1)$ The propagation delay measured from Adder 1 A or B Data Input signal transition to the LOW-HIGH transition of the TRUE Sum Output signal.

$t_{pd-}(A_1S_1)$ The propagation delay measured from Adder 1 A or B Data Input signal transition to the HIGH-LOW transition of the TRUE Sum Output signal.

$t_{pd+}(\overline{A}_2S_2)$ The propagation delay measured from Adder 2 A or B FALSE Data Input signal transition to the LOW-HIGH transition of the TRUE Sum Output signal.

$t_{pd-}(\overline{A}_2S_2)$ The propagation delay measured from Adder 2 A or B FALSE Data Input signal transition to the HIGH-LOW transition of the TRUE Sum Output signal.

$t_{pd+}(A_2\overline{S}_2)$ The propagation delay measured from Adder 2 A or B Data Input signal transition to the HIGH-LOW transition of the FALSE Sum Output signal.

$t_{pd-}(A_2\overline{S}_2)$ The propagation delay measured from Adder 2 A or B Data Input signal transition to the LOW-HIGH transition of the FALSE Sum Output signal.

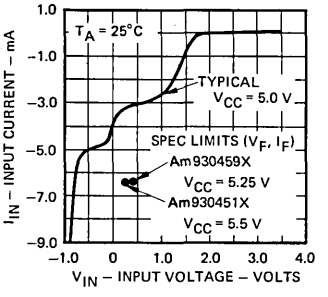
$t_{pd+}(A_2S_2)$ The propagation delay measured from Adder 2 A or B Data Input signal transition to the LOW-HIGH transition of the TRUE Sum Output signal.

$t_{pd-}(A_2S_2)$ The propagation delay measured from Adder 2 A or B Data Input signal transition to the HIGH-LOW transition of the TRUE Sum Output signal.

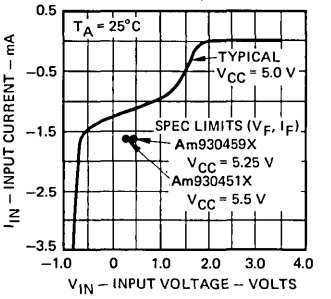
PERFORMANCE CURVES

Input Characteristics

Input Current Versus Input Voltage Pins 1, 2, 3, 4, 12, 15

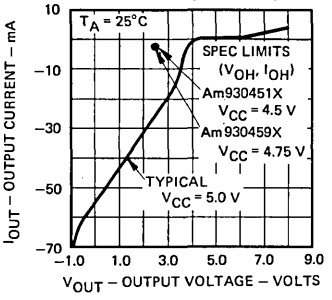


Input Current Versus Input Voltage Pins 13, 14

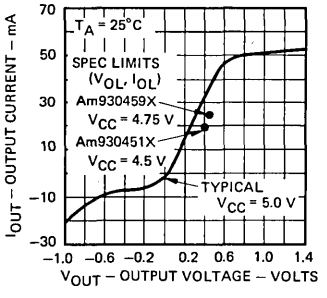


Output Characteristics

Output HIGH Current Versus Output Voltage

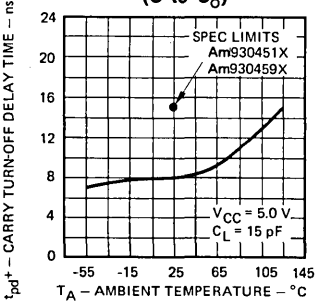


Output LOW Curent Versus Output Voltage

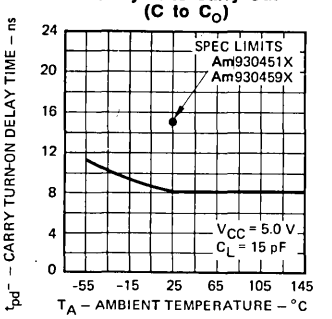


Switching Characteristics

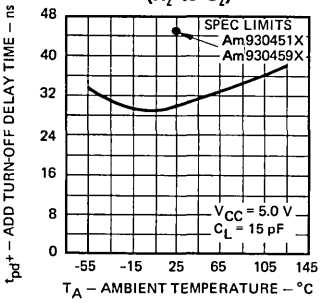
Turn Off Delay Carry In to Carry Out (C to C_O)



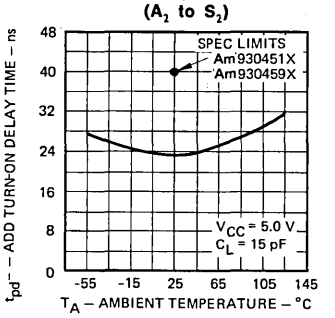
Turn On Delay Carry In to Carry Out (C to C_O)



Turn Off Delay Data In to Sum Output (A_2 to S_2)



Turn On Delay Data In to Sum Out (A_1 to S_2)



TRUTH TABLES

Adder 1

Inputs			Outputs		
C_1	B_1	A_1	$\overline{C}_{O1}$	$\overline{S}_1$	S_1
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	L
H	H	H	L	L	H

Table I

Adder 2

Inputs					Outputs		
$\overline{C}_2$	B_2	A_2	$\overline{B}_2$	$\overline{A}_2$	C_{O2}	S_2	$\overline{S}_2$
L	L	L	L	L	H	H	L
L	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H
L	L	L	H	H	L	H	L
L	L	H	L	L	H	H	L
L	L	H	L	H	H	H	L
L	L	H	H	L	H	L	H
L	L	H	H	H	H	L	H
L	H	L	L	L	H	H	L
L	H	L	L	H	H	L	H
L	H	L	H	L	H	H	L
L	H	L	H	H	H	L	H
L	H	H	L	L	H	H	L
L	H	H	L	H	H	H	L
L	H	H	H	L	H	H	L
L	H	H	H	H	H	H	L
H	L	L	L	L	H	L	H
H	L	L	L	H	L	H	L
H	L	L	H	L	L	H	L
H	L	L	H	H	L	L	H
H	L	H	L	L	H	L	H
H	L	H	L	H	H	L	H
H	L	H	H	L	L	H	L
H	L	H	H	H	L	H	L
H	H	L	L	L	H	L	H
H	H	L	L	H	L	H	L
H	H	L	H	L	H	L	H
H	H	L	H	H	L	H	L
H	H	H	L	L	H	L	H
H	H	H	L	H	H	L	H
H	H	H	H	L	H	L	H
H	H	H	H	H	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level

Table II

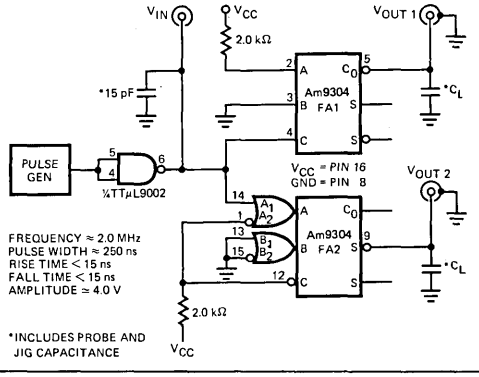
Am9304 LOADING RULES (in unit loads)

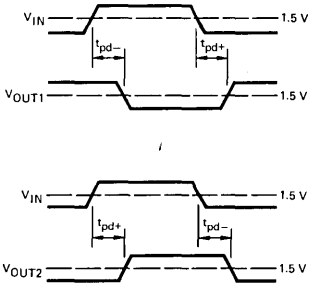
Input/Output	Pin No.s	Input Unit Load	Output Drive HIGH	Output Drive LOW
A_1	2	4	—	—
B_1	3	4	—	—
C_1	4	4	—	—
A_2	14	1	—	—
$\overline{A}_2$	1	4	—	—
B_2	13	1	—	—
$\overline{B}_2$	15	4	—	—
$\overline{C}_2$	12	4	—	—
S_1	7		20	10
$\overline{S}_1$	6		20	10
$\overline{C}_{01}$	5	—	14	7
$\overline{S}_2$	9	—	20	10
S_2	10	—	20	10
C_{02}	11	—	14	7
GND	8	—	—	—
V_{CC}	16	—	—	—

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





Am9304 APPLICATIONS

GATING ELEMENTS

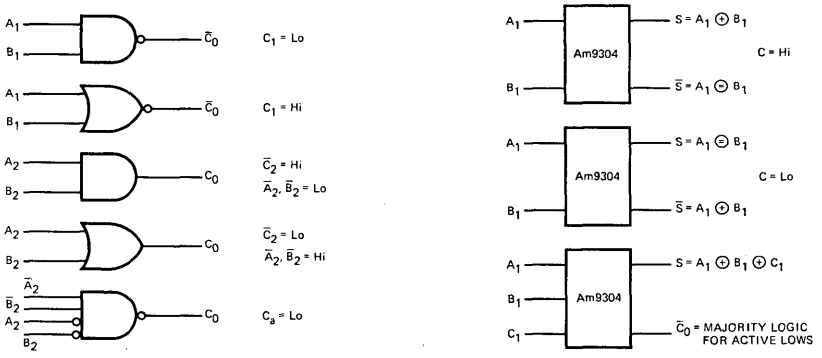
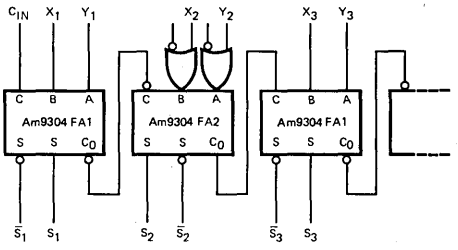
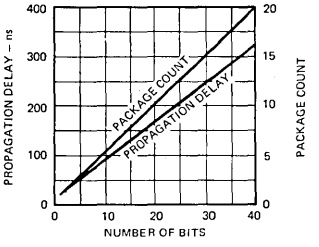


Figure 5 RIPPLE CARRY PARALLEL ADDITION



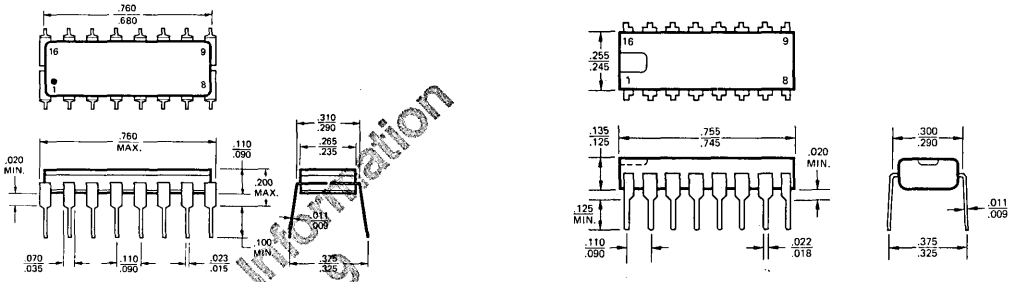
PROPAGATION DELAY AND PACKAGE COUNT AGAINST WORD LENGTH FOR RIPPLE CARRY ADDITION



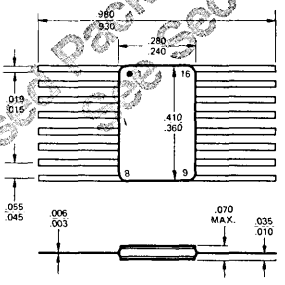
Shown above is a high-speed ripple carry parallel addition scheme. Only one and-or-not gate delay is incurred at each stage allowing a typical addition speed of (N + 1) x 8 ns, where N is the number of bits in the word. The curve shows propagation delay of the ripple-Carry Adder drawn in Figure 5. Plotted on the same diagram is a curve showing the low package count resulting from this Ripple Scheme.

PHYSICAL DIMENSIONS

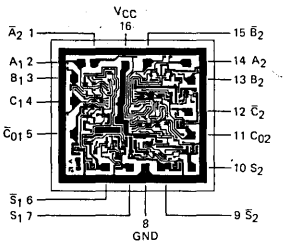
Hermetic — **Dual-In-Line** — **Molded**



Flat Package



Metallization and Pad Layout



77 x 71 Mils

ADVANCED MICRO DEVICES INC.
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California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am9306/2501

BCD Decade/Binary Hexadecimal Synchronous Up-Down Counters

Distinctive Characteristics:

- 100% reliability assurance testing including high - temperature bake, temperature cycling, centrifuge and package hermeticity testing in compliance with MIL STD 883.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

The Am9306 BCD Synchronous Up-Down Decade Counter is functionally, electrically, and pin-for-pin equivalent to the Fairchild 9306. The Am2501 is a Binary Hexidecimal version of the 9306. They are both available in the hermetic dual-in-line package. These counters consist of four master-slave JK flip-flops driven synchronously by a buffered clock pulse (CP) input.

During the CP LOW-to-HIGH transition the master flip-flop stage is inhibited from further change. Following master flip-flop lock out, data is transferred from the master to the slave flip-flop outputs, Q_0, Q_1, Q_2 and Q_3. With CP HIGH the master flip-flop is inhibited from data entry and the master slave data transfer path remains established. The data entry/transfer procedure is reversed during the CP HIGH-to-LOW transition.

The $\overline{CD}$ input is a single line up/down control. When the $\overline{CD}$ input is LOW, and if counting is not inhibited the counter will count down on the next clock pulse and if the $\overline{CD}$ input is HIGH the counter will count up on the next clock pulse.

The parallel enable ($\overline{PE}$), when LOW, allows the counters to be synchronously preset from the four parallel inputs, P_0, P_1, P_2 and P_3. $\overline{PE}$ HIGH inhibits presetting. The state diagrams in Figure 7 indicate the count sequence of the counters after presetting to any of sixteen (16) possible states. The circuits count on the LOW-to-HIGH transition of the clock input. The 9306 counts in a 8-4-2-1 binary coded decimal (BCD) code; the 9306B counts in a 8-4-2-1 binary code.

The terminal count (TC) output is active HIGH when the counters are at terminal count. The terminal count logic equations are:

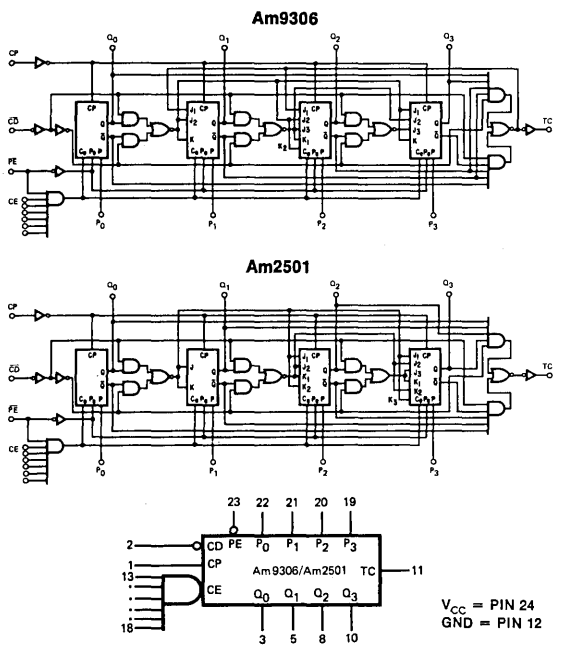
Am9306 $TC = (CD \bullet \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 + \overline{CD} \bullet Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3)$

Am2501 $TC = (CD \bullet \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 + \overline{CD} \bullet Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3)$

The count mode is enabled when all six CE inputs are in the HIGH state. The multistage counter in Figure 9 illustrates the high-speed look-ahead carry technique made available by the six CE inputs.

The clock pulse must be HIGH during the HIGH-to-LOW transition of a CE input with all remaining CE inputs HIGH and during the LOW-to-HIGH transition of $\overline{PE}$ for correct logic operation. Any change of $\overline{CD}$ must be made only when CP is HIGH. The Am2501 is also available in a 16-pin package with only two count enables.

LOGIC DIAGRAMS/SYMBOL



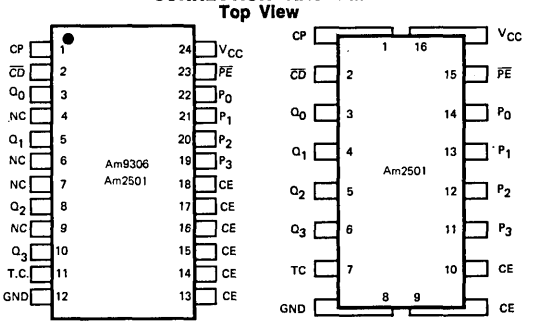
The basic cell for the Am9306 and Am2501 is illustrated in Figure 8.

Am9306/2501 ORDERING INFORMATION

Package Type	Temperature Range	Am9306 Order Number	Am2501 Order Number
24-pin Hermetic DIP	0°C to +75°C	U6N9306659X	AM250159G
24-pin Hermetic DIP	−55°C to +125°C	U6N9306651X	AM250151G
16-pin Hermetic DIP	0°C to +75°C		AM250159F
16-pin Hermetic DIP	−55°C to +125°C		AM250151F
Dice	Note 4	UXX9306XXD	AM2501XXD

Note 4: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current (Note 1)	−30 mA to +5 mA

ELECTRICAL CHARACTERISTICS

U6N930659X/AM250159X T_A = 0°C to +75°C
U6N930651X/AM250151 T_A = −55°C to +125°C

DC Characteristics (Note 2)

Parameters	Part No.	Test Conditions	LIMITS −55°C Min	−55°C Max	0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	+125°C Min	+125°C Max	Units
V_{OH} Output HIGH Voltage	Am930651X Am250151	V_{CCL} = 4.5 V, $I_{OH} = 6xI_R = -0.36$ mA	2.40				2.40	2.7				2.40		Volts
	Am930659X Am250159	V_{CCL} = 4.75 V, $I_{OH} = 6xI_R = -0.36$ mA			2.40		2.40	3.0		2.40				
V_{OL} Output LOW Voltage	Am930651X Am250151	V_{CCH} = 5.5 V, $I_{OL} = 6xI_F$ = 9.6 mA V_{CCL} = 4.5 V, $I_{OL} = 6xI_F$ = 7.44 mA		0.40				0.2	0.40				0.40	Volts
	Am930659X Am250159	V_{CCH} = 5.25 V, $I_{OL} = 6xI_F$ = 9.6 mA V_{CCL} = 4.75 V, $I_{OL} = 6xI_F$ = 8.5 mA				0.45		0.2	0.45		0.45			
V_{IH} Input HIGH Voltage	Am930651X Am250151	V_{CCH} = 5.5 V V_{CCL} = 4.5 V	2.00				1.70					1.40		Volts
	Am930659X Am250159	V_{CCH} = 5.25 V V_{CCL} = 4.75 V			1.90		1.80			1.60				
V_{IL} Input LOW Voltage	Am930651X Am250151	V_{CCH} = 5.5 V V_{CCL} = 4.5 V		0.80					0.90				0.80	Volts
	Am930659X Am250159	V_{CCH} = 5.25 V V_{CCL} = 4.75 V				0.85			0.85		0.85			
I_F (Note 3) Input Load Current ($\overline{CD}$, CE)	Am930651X Am250151	V_{CCH} = 5.5 V, V_F = 0.4 V V_{CCL} = 4.5 V		−1.60 −1.24				−1.10 −0.97	−1.60 −1.24				−1.60 −1.24	mA
	Am930659X Am250159	V_{CCH} = 5.25 V, V_F = 0.45 V V_{CCL} = 4.75 V				−1.60 −1.41		−1.00 −0.90	−1.60 −1.41		−1.60 −1.41			
I_R (Note 3) Reverse Input Current ($\overline{CD}$, CE)	Am930651X Am250151	V_{CCH} = 5.5 V, V_R = 4.5 V		60				15	60				60	μA
	Am930659X Am250159	V_{CCH} = 5.25 V, V_R = 4.5 V				60		15	60		60			
I_{PD} Power Supply Current	Am930651X Am250151	V_{CC} = 5.0 V						91						mA
	Am930659X Am250159	V_{CC} = 5.0 V						96						

Switching Characteristics (T_A = 25°C)

		Test Conditions	Min	Typ	Max	Units
t_{pd+}	Turn Off Delay — Q Outputs	V_{CC} = 5.0 V, C_L = 15 pF (Refer to Figure 1)	10	20	30	ns
t_{pd-}	Turn On Delay — Q Outputs		10	20	30	ns
t_{pd+}(TC)	Turn Off Delay TC		20	40	60	ns
t_{pd-}(TC)	Turn On Delay TC		15	30	45	ns
t_s(CE)	Set-up Time CE	V_{CC} = 5.0 V, C_L = 15 pF (Refer to Figure 2)		25	40	ns
t_r(CE)	ReleaseTime CE		10			ns
t_s	Set-up Time P-Inputs	V_{CC} = 5.0 V, C_L = 15 pF (Refer to Figure 3)		15	40	ns
t_r	Release Time P-Inputs		0	15		ns
$t_s(\overline{PE})$	Set-up Time $\overline{PE}$			20	40	ns
$t_r(\overline{PE})$	Release Time $\overline{PE}$		0	20		ns
$t_s(\overline{CD})$	Set-up Time $\overline{CD}$	V_{CC} = 5.0 V, C_L = 15 pF (Refer to Figure 4, 5)		7		ns
$t_r(\overline{CD})$	Release Time $\overline{CD}$			20		ns
Count Frequency		V_{CC} = 5.0 V, C_L = 15 pF	20	27		MHz

Note 1. Max current defined by D.C. input voltage
2. Pulse tested
3. For CP, $\overline{PE}$, P_0, P_1, P_2 and P_3 input currents use Am9306/2501 loading rules.

)EFINITION OF TERMS

·UBSCRIPT TERMS:

Forward, applying to LOW inputs.

HIGH, applying to a HIGH logic level or when used with V_{CC} to ıdicate high V_{CC} value.

Input.

LOW, applying to LOW logic level or when used with V_{CC} to ıdicate low V_{CC} value.

Output.

Reverse, applying to HIGH inputs.

UNCTIONAL TERMS:

ısynchronous (ripple) Counter All outputs (flip flops) change state n command from a preceding stage.

D Input The Up/Down control. A LOW on this input forces the ounter to count DOWN on receipt of a clock pulse. A HIGH on this ıput forces the counter to count UP on receipt of a clock pulse.

E Inputs The count mode is inhibited by a LOW on any of the ix CE inputs. Outputs TC, Q_0, Q_1, Q_2 and Q_3 remain unchanged. ·efer to Truth Table II.

an-Out The logic HIGH or LOW output drive capability in terms f Input Unit Loads.

ıput Unit Load One T^2L gate input load. In the HIGH state it is ·qual to I_R and in the LOW state it is equal to I_F.

K Flip Flop *Properties similar to an RS Flip Flop except that* = K = 1 is allowed. Refer to Truth Table I.

, K Inputs The logic inputs for setting the JK flip flop of the egister. Refer to Table I.

'E Input The input for selection of parallel data entry to the egister. Parallel Enable ($\overline{PE}$) LOW allows parallel data entry.

'0, P1, P2, P3 Inputs The inputs for data entry into the four synchro- ıous clocked JK Flip Flops. Refer to Table II.

ı0, Q1, Q2, Q3 Outputs The four outputs of the 9306/Am2501 egister *flip flops.*

ı0 (t_n) The output after the n'th clock pulse.

ı0 (t_{n+1}) *The output after the* (n+1) clock pulse.

ynchronous Counter All outputs (flip flops) change state on ommand from the clock.

'erminal Count The highest number a counter can attain when ıperated in the count mode and counting up or the lowest number ı counter can attain when operated in the count mode and count- ng down.

'C Output This output is *HIGH when CD is LOW and the counter* s in state 0 (Q_0, Q_1, Q_2, Q_3 are all LOW), or when CD is HIGH and n the case of the 9306, the counter is in state 9 (Q_0, Q_3 are HIGH, ı, Q_2 are LOW), or when CD is HIGH and in the case of the \m2501 the counter is in the state 15 (Q_0, Q_1, Q_2, Q_3 are all HIGH).

)PERATIONAL TERMS:

F Forward input load current for unit input load.

OH Output HIGH current forced out of output in V_{OH} test.

OL *Output LOW current forced into the output in* V_{OL} test.

R Reverse input load current with V_R applied to input.

Negative Current Current flowing out of the device.

Positive Current *Current flowing into the device.*

V_{IH} Minimum logic HIGH input voltage. Refer to Figure 6.

V_{IL} Maximum logic LOW input voltage. Refer to Figure 6.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

V_F Forward LOW input voltage, for forward input current (I_F) test.

V_R Input reverse HIGH voltage applied for input leakage current, (I_R) test.

SWITCHING TERMS: (All switching times are measured at the 1.5 V logic level)

CP Clock Pin, pulsed. The subscript, if any, refers to pulse wave- shape.

t_{pd-} The propagation delay from the clock signal LOW-HIGH transition to an output signal HIGH-LOW transition. Refer to Figure 1.

t_{pd+} The propagation delay from the clock signal LOW-HIGH transition to an output signal LOW-HIGH transition. Refer to Figure 1.

t_{pd+}(TC) The propagation delay from the clock signal LOW-HIGH transition to the TC output LOW-HIGH transition. Refer to Figure 1.

t_{pd-}(TC) *The propagation delay from the clock signal* LOW-HIGH transition to the TC output HIGH-LOW transition. Refer to Figure 1.

t_s Set-up time defined as the minimum time required for the logic level to be present at the data inputs prior to the clock transition from LOW to HIGH in order for the flip flop(s) to respond. Refer to Figure 3.

t_r Release time defined as the maximum time allowed for the logic level to be present at the data inputs *prior to the clock transition* from LOW to HIGH in order for the flip flop(s) not to respond. Refer to Figure 3.

t_s(CE) The minimum time required for the logic level to be present at a CE input prior to the clock transition from LOW to HIGH in order for the flip flop(s) not to respond. Refer to Figure 2.

t_r(CE) The maximum time allowed for the logic level to be present at a CE input *prior to the clock transition from* LOW to HIGH in order for the flip flop(s) not to respond. Refer to Figure 2.

$t_s(\overline{PE})$ Set-up time for the Parallel Enable is defined as the mini- mum time required for the logic level to be present at the Parallel Enable (PE) prior to the clock transition from LOW to HIGH in order for the flip flop(s) to respond. Refer to Figure 3.

$t_r(\overline{PE})$ Release time for the Parallel Enable is defined as the maxi- mum time *allowed for the logic level to be present at the* Parallel Enable logic input prior to the clock transition from LOW to HIGH in order for the flip flop(s) not to respond. Refer to Figure 3.

$t_s(\overline{CD})$ The minimum time which must elapse between any change of state of $\overline{CD}$ and the CP HIGH to LOW transition in order to ensure correct counter operation. Refer to Figure 4, 5.

$t_r(\overline{CD})$ The maximum time which must elapse between any change *of state of* $\overline{CD}$ *and the* CP LOW to HIGH transition for correct counter operation. Refer to Figure 4, 5.

SWITCHING WAVEFORMS

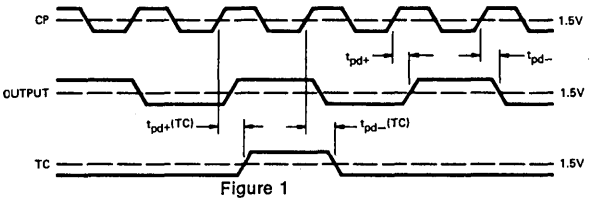


Figure 1

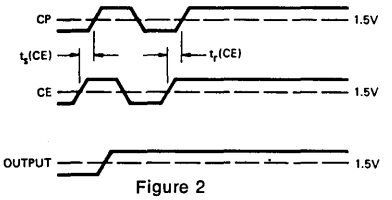


Figure 2

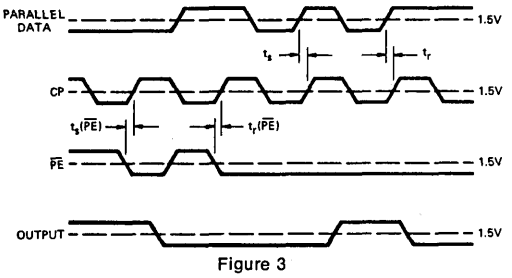


Figure 3

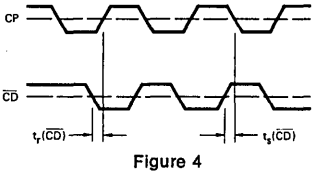


Figure 4

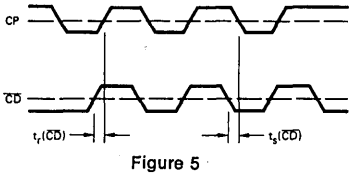


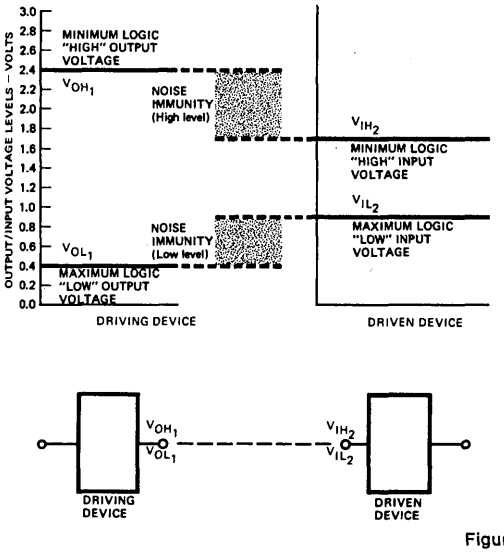
Figure 5

Switching tests are performed with CP input driven by a TTμL9002 gate and the outputs loaded by 15 pF capacitance to include jig capacitance. All unused inputs are tied to V_{CC}. The pulse generator driving the TTμL9002 is set up in the following condition:

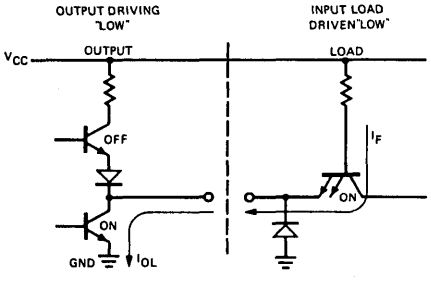
Rise Time $<$15 ns
Fall Time $<$15 ns
Amplitude $\approx$4 V
Frequency = 2 MHz $\pm$5% at 50% duty cycle

INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH



Current Interface Conditions — LOW



Current Interface Conditions — HIGH

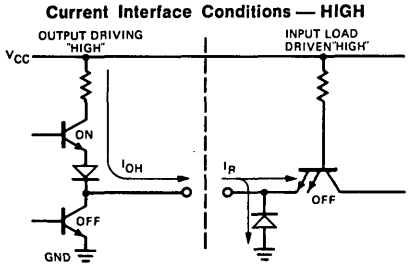
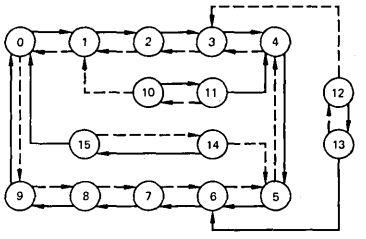


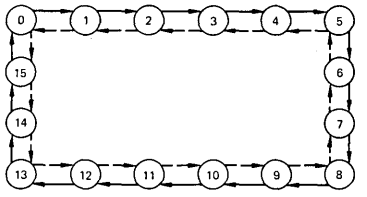
Figure 6

Am9306/2501 STATE DIAGRAMS

Am9306



Am2501



COUNT UP

COUNT DOWN

The state diagrams show the count sequence after the counters are preset to any one of the sixteen possible states.

Figure 7

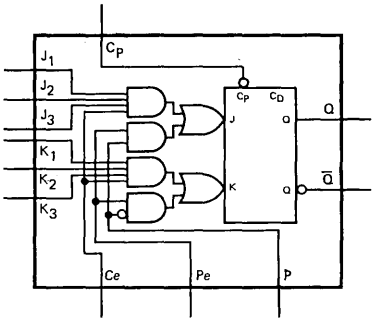
Am9306/2501 LOADING RULES

Input/Output	Pin No.'s	Input Unit Load	Fanout Output HIGH	Fanout Output LOW
CP	1	2	—	—
$\overline{CD}$	2	1	—	—
Q_0	3	—	6	6
Q_1	5	—	6	6
Q_2	8	—	6	6
Q_3	10	—	6	6
TC	11	—	6	6
GND	12	—	—	—
CE	13-18	1	—	—
P_3	19	2/3	—	—
P_2	20	2/3	—	—
P_1	21	2/3	—	—
P_0	22	2/3	—	—
$\overline{PE}$	23	2	—	—
V_{CC}	24	—	—	—

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	Equivalent Input Unit Load LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Am9306/2501 BASIC CELL



This basic cell illustrates how data is entered and controlled internally. Count enable gating is also shown.

Figure 8

TRUTH TABLES

Mode Selection

CE	$\overline{CD}$	$\overline{PE}$	Mode
H	H	H	Count Up
H	L	H	Count Down
L	X	H	Count Inhibited
X	X	L	Presetting

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

TABLE II

JK Flip Flop

J	K	Q_0 (tn+1)
L	L	Q_0(tn) No change
L	H	L
H	L	H
H	H	$\overline{Q}_0$(tn) Toggle

$J = J_1 \bullet J_2 \bullet J_3$
$K = K_1 \bullet K_2 \bullet K_3$ TABLE I

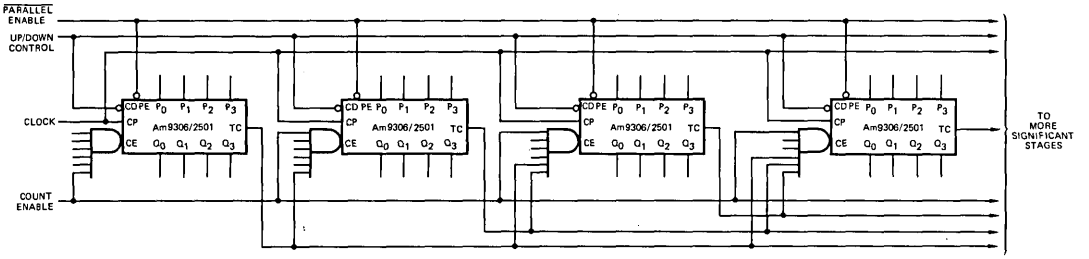


Figure 9

Multistage Counting

Counter stages can be cascaded, as shown above, to provide multiple stage BCD or binary synchronous counting by using the Am9306 or the Am2501 respectively. With a TC fan-out of six the above scheme allows seven stages to operate at the maximum frequency equivalent to a two stage counter. The $\overline{PE}$ control can be used as an additional count enable input by connecting counter outputs to the corresponding parallel inputs.

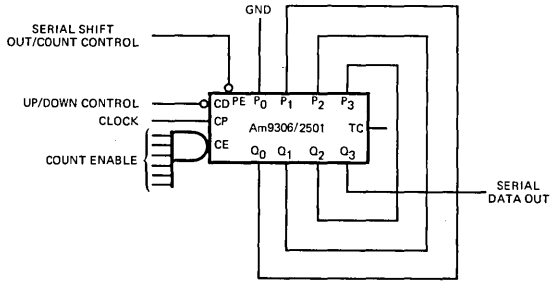


Figure 10

Serial Output

The counter can be connected as a shift register by using the parallel load facility and connecting the counter outputs to the corresponding higher stage input. Input P_0 is grounded so as to initialize the counter to zero during the shifting operation.

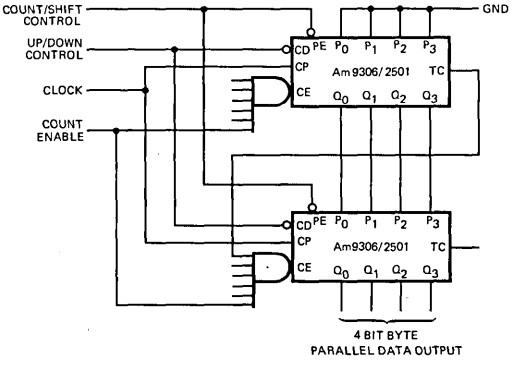
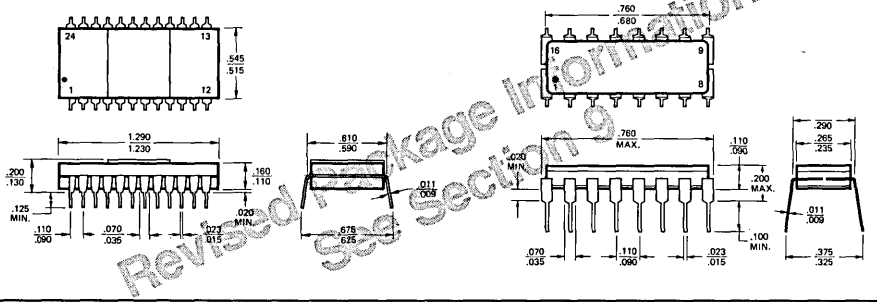


Figure 11

Parallel-Serial Output

Count results may be shifted out four bits at a time from cascaded counters for display in the case of the Am9306 BCD decade counter or for further parallel serial computation.

PHYSICAL DIMENSIONS
Hermetic Dual-In-Line



ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am9308
Dual Four-Bit Latch

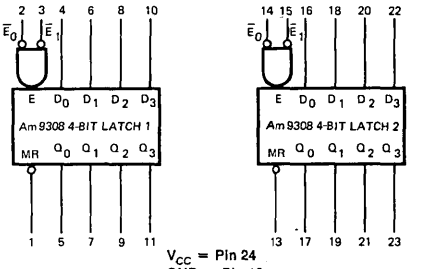
Distinctive Characteristics:

- 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and package hermeticity testing in compliance with MIL STD 883.
- Two independent enables on each latch.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

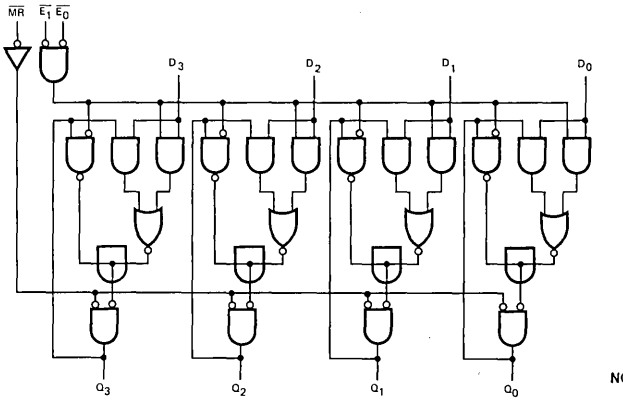
The Am 9308 provides 8 bits of latch storage divided into two blocks of 4 bits. Data enters into a latch when both enable inputs to the 4-bit latch block are LOW. While this condition exists the output of the latch follows the input. If either enable input goes HIGH the data present in the latch at that time is held in the latch and is no longer affected by the data input. An active LOW master reset is provided for each 4-bit latch. This reset overrides all other input conditions and when activated forces the outputs of all the latches LOW.

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM



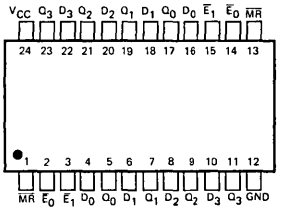
NOTE: Only one 4 Bit Latch shown.

Am9308 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	AM930859C
Hermetic DIP	0°C to +75°C	U6N930859X
Hermetic DIP	−55°C to +125°C	U6N930851X
Hermetic Flat Pak	−55°C to +125°C	U4M930851X
Dice	Note	UXX9308XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current (Note 1)	−30 mA to +5 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am930859X T_A = 0°C to +75°C V_{CC} = 5.0 V ±5%
Am930851X T_A = −55°C to +125°C V_{CC} = 5.0 V ±10%

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.72 mA V_{IN} = V_{IH} or V_{IL}		2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 14.4 mA V_{IN} = V_{IH} or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V			−1.0	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V			6.0	40	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V		−20		−70	mA
I_{CC}	Power Supply Current	All other inputs = 4.5 V V_{CC} = MAX.	Am930851X		65	100	mA

Notes: 1) Typical Limits are at V_{CC} = 5.0 V, 25°C Ambient and maximum loading.
2) Actual Input currents are obtained by multiplying unit load current by input load factor (See Loading Rules).

SWITCHING CHARACTERISTICS (T_A = 25°C)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{pd+} ($\overline{E}$)	Enable to Output HIGH	V_{CC} = 5.0 V C_L = 15 pF	10	19	30	ns
t_{pd-} ($\overline{E}$)	Enable to Output LOW		6	12	18	
t_{pd+} (D)	Data to Output HIGH		8	16	20	ns
t_{pd-} (D)	Data to Output LOW		6	12	18	
t_s "H"	HIGH Data Set-up Time		−4	0	6	ns
t_s "L"	LOW Data Set-up Time		4	7	10	
t_{pw} ($\overline{E}$)	Min. Enable Pulse Width			8	15	ns
t_{pw} ($\overline{MR}$)	Min. Master Reset Pulse Width			10	15	ns
t_{pd-} ($\overline{MR}$)	Master Reset to Output LOW		7	14	20	
t_{rec} ($\overline{MR}$)	Master Reset Recovery Time			−1	10	ns

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS:

D_0, D_1, D_2, D_3 Inputs The four data inputs of each of the 9308 latch blocks.

$\overline{E}_0$, $\overline{E}_1$ Inputs The two Enable inputs. Both of these inputs must be LOW for insertion of data into the latches.

Fan Out The logic HIGH or LOW output drive capability in terms of input unit loads.

Input Unit Load One T^2L gate input load. In the HIGH state it is equal to 40μA at 2.4V and in the LOW state it is equal to 1.6mA at 0.4V.

Latch A storage element which stores one bit of data on receipt of a single transition on an Enable signal.

$\overline{MR}$ Input The master reset input.

Q_0, Q_1, Q_2, Q_3 Outputs The four outputs of each of the 9308 latch blocks.

Q (t_n) The output of a latch at time t_n.

Q (t_{n+1}) The output of a latch at time t_{n+1} when input conditions at time t_n have been realized by the output.

OPERATIONAL TERMS:

I_{IL} Forward input load current for unit input load.

I_{OH} Output HIGH current forced out of output in V_{OH} test.

I_{OL} Output LOW current forced into the output in V_{OL} test.

I_{IH} Reverse input load current with V_{OH} applied to input.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage. Refer to Figure 6.

V_{IL} Maximum logic LOW input voltage. Refer to Figure 6.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

SWITCHING TERMS: (All switching times are measured at the 1.5 V logic level.)

t_{pw} **($\overline{E}$)** The minimum time that both Enable inputs $\overline{E}_0$ and $\overline{E}_1$ must be LOW in order for data to be correctly entered into the latches.

t_{pw}**($\overline{MR}$)** The minimum pulse width for resetting the latches.

t_{pd+} **(DQ)** The propagation delay from the D input LOW to HIGH transition to the Q output LOW to HIGH transition. Refer to Figure 1.

t_{pd-} **(DQ)** The propagation delay from the D input HIGH-LOW transition to the Q output HIGH to LOW transition. Refer to Figure 1.

t_{pd+} **($\overline{E}$Q)** The propagation delay from the Enable signal HIGH-LOW transition to the Q output LOW to HIGH transition. Refer to Figure 1.

t_{pd-} **($\overline{E}$Q)** The propagation delay from the Enable signal HIGH to LOW transition to the Q output HIGH to LOW transition. Refer to Figure 1.

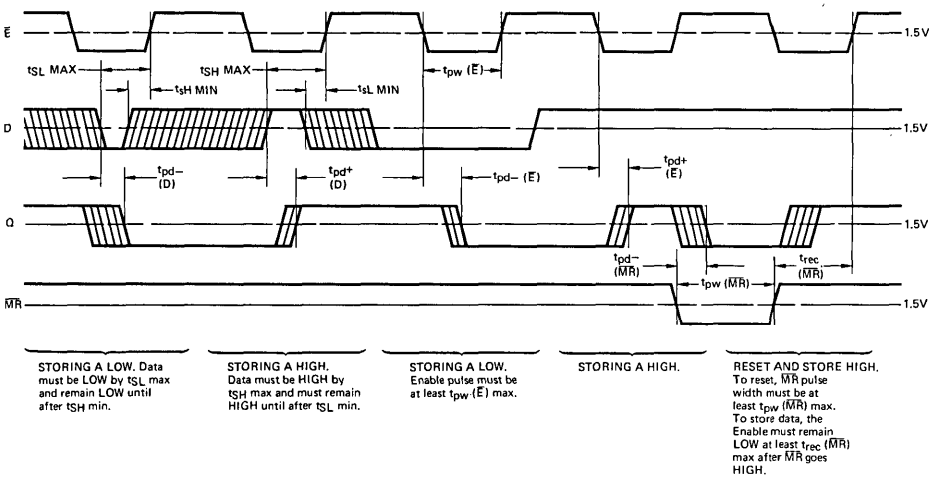
t_{s} "H" **($\overline{DE}$)** The time required for a HIGH logic level to be present and remain present at a data input prior to the Enable transition from LOW to HIGH in order for the latch to retain a HIGH logic level. Refer to Figure 1. HIGH data must be steady at all times between t_{sH} max and t_{sL} min.

t_{s} "L" **($\overline{DE}$)** The time required for a LOW logic level to be present and remain present at a data input prior to the Enable transition from LOW to HIGH in order for the latch to retain a LOW logic level. LOW data must be steady at all times between t_{sL} max and t_{sH} min.

t_{rec} **($\overline{MR}$)** Recovery time for MR is the minimum time required between the end of the reset pulse and the Enable transition from LOW to HIGH in order for the latches to respond to new data. Refer to Figure 1.

t_{pd-} **($\overline{MR}$)** The propagation delay from the master reset signal HIGH-LOW transition to the output HIGH-LOW transition. Refer to Figure 1.

SWITCHING WAVEFORMS



Note: The "set-up Time" is defined as the time required, relative to the enable, for a LOW to HIGH edge (tsH) or a HIGH to LOW edge (tsL) to propagate through internal delays. Logic transitions occurring before ts max are guaranteed to be detected; those occurring after ts min are guaranteed not to be detected. Transitions between ts max and ts min may or may not be detected. The minimum set up time for a LOW is sometimes called the "release time" for a HIGH.

KEY TO TIMING DIAGRAM

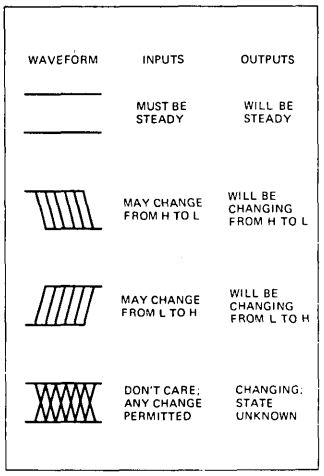


Figure 1

TRUTH TABLE

Inputs				Output
$\overline{MR}$	$\overline{E}_0$	$\overline{E}_1$	$D_{(n)}$	$Q_{(n+1)}$
L	X	X	X	L
H	L	L	L	L
H	L	L	H	H
H	H	X	X	$Q_{(n)}$ No change
H	X	H	X	$Q_{(n)}$ No change

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Table I

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Table II

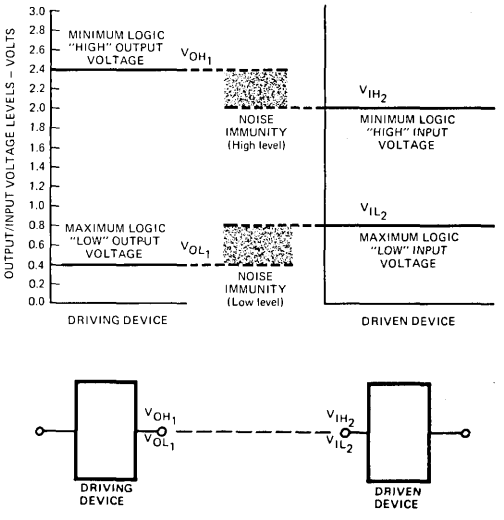
Am9308 LOADING RULES (in unit loads)

Input/Output	Pin No.'s	Input Unit Load	Output Drive HIGH	LOW
Latch 1 $\overline{MR}$	1	1	—	—
$\overline{E}_0$	2	1	—	—
$\overline{E}_1$	3	1	—	—
D_0	4	1.5	—	—
Q_0	5	—	18	9
D_1	6	1.5	—	—
Q_1	7	—	18	9
D_2	8	1.5	—	—
Q_2	9	—	18	9
D_3	10	1.5	—	—
Q_3	11	—	18	9
GND	12	—	—	—
Latch 2 $\overline{MR}$	13	1	—	—
$\overline{E}_0$	14	1	—	—
$\overline{E}_1$	15	1	—	—
D_0	16	1.5	—	—
Q_0	17	—	18	9
D_1	18	1.5	—	—
Q_1	19	—	18	9
D_2	20	1.5	—	—
Q_2	21	—	18	9
D_3	22	1.5	—	—
Q_3	23	—	18	9
V_{CC}	24	—	—	—

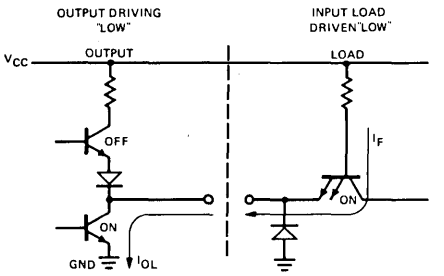
Table III

INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH



Current Interface Conditions — LOW



Current Interface Conditions — HIGH

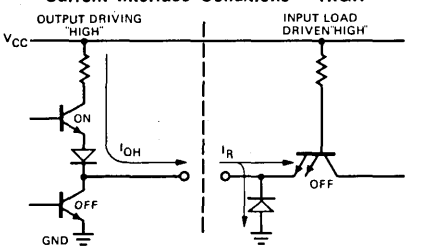


Figure 2

9308 APPLICATIONS

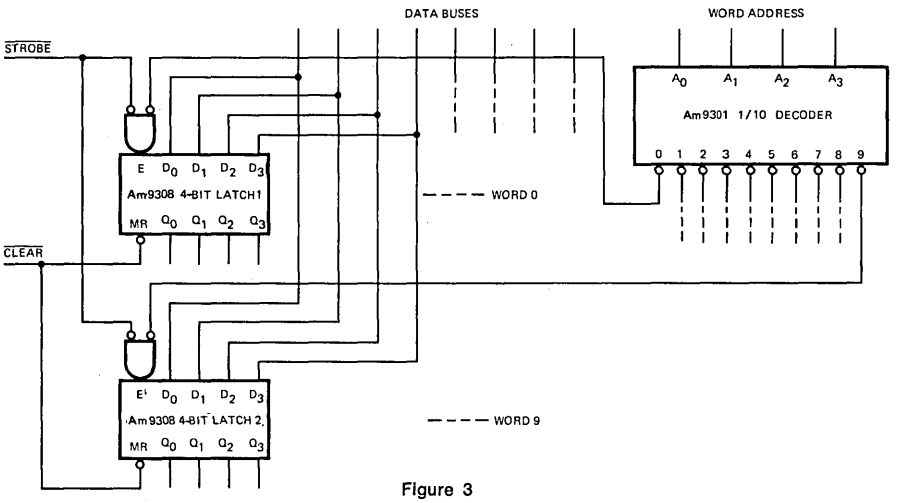


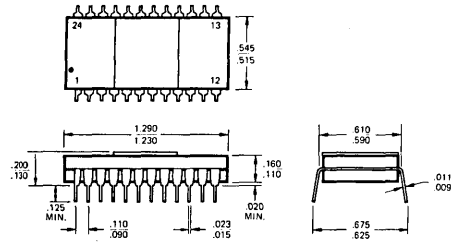
Figure 3

Latch Selection

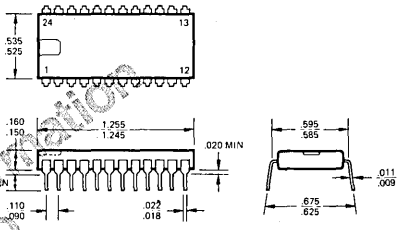
The Am9308 can be selected by using an Am9301 decoder. The active LOW outputs of the Decoder conform with the active LOW input enables of the latch blocks. The diagram shows one 4-bit latch being selected out of ten possible latch blocks.

PHYSICAL DIMENSIONS
Dual-In-Line

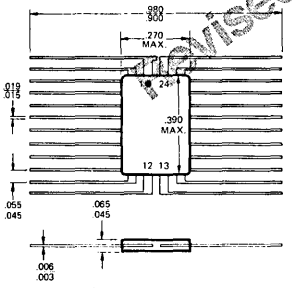
Hermetic



Molded

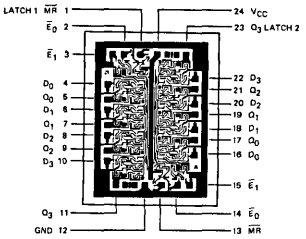


Flat Package



Metallization and Pad Layout

73 x 101 Mils



ADVANCED MICRO DEVICES INC.
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Am93L08
Low-Power Dual Four-Bit Latch

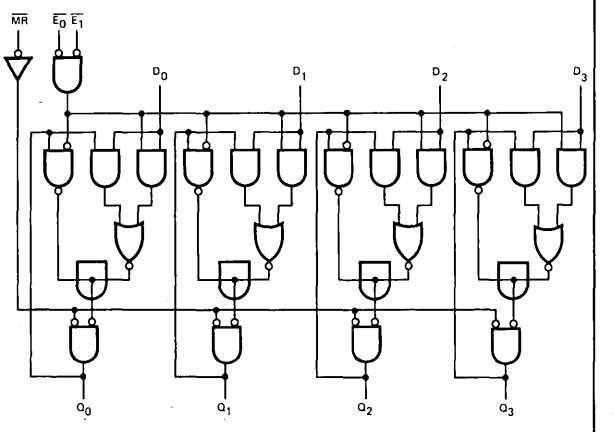
Distinctive Characteristics

- 100 mw typical power dissipation.
- 30 ns typical propagation delay.
- 100% reliability assurance testing in compliance with MIL STD 883.
- Compatible with 7400 and 9300 series devices.

FUNCTIONAL DESCRIPTION

The Am93L08 consists of two independent four-bit latches. Each latch has two active LOW enables. When both enables are LOW, data on the inputs (D_0, D_1, D_2, D_3) are fed through to the outputs (Q_0, Q_1, Q_2, Q_3). If either enable goes HIGH, then the four outputs are inhibited from further change and the last data on the inputs before the enable went HIGH are stored. Each latch also has an active LOW master reset input which forces all outputs to the LOW state regardless of any other inputs.

LOGIC DIAGRAM



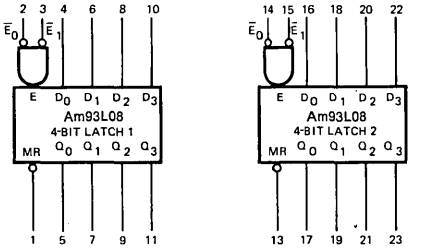
LOADING RULES

In Unit Loads (Notes)

Input Load Factor	TTL LOADS HIGH	TTL LOADS LOW	93L LOADS HIGH	93L LOADS LOW
D_0, D_1, D_2, D_3	0.75	0.375	1.5	1.5
$\overline{MR}$, $\overline{E}_0$, $\overline{E}_1$	0.5	0.25	1.0	1.0
Output Drive	HIGH	LOW	HIGH	LOW
All Outputs	10	3.0	20	12

NOTES:
1) A TTL unit load is specified as 0.4 V at −1.6 mA LOW, 2.4 V at 40 μA HIGH.
2) A 93L unit load is specified as 0.3 V at −400 μA LOW, 2.4 V at 20 μA HIGH.
3) Enough output LOW current is available to mix TTL and 93L loads and still meet the 93L requirement of a V_{OL} of 0.3 V.

LOGIC SYMBOL



V_{CC} = PIN 24
GND = PIN 12

Am93L08 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
24-Pin Molded DIP	0°C to +75°C	AM93L0859C
24-Pin Hermetic DIP	0°C to +75°C	U6N93L0859X
24-Pin Hermetic DIP	−55°C to +125°C	U6N93L0851X
24-Pin Hermetic Flat Pak	−55°C to +125°C	U4M93L0851X
Dice	Note	UXX93L08XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current Note 1	−30 mA to +5.0 mA

Note 1. Maximum current defined by DC input voltage.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93L0859X T_A = 0°C to +75°C V_{CC} = 4.75 V to 5.25 V
Am93L0851X T_A = −55°C to +125°C V_{CC} = 4.50 V to 5.50 V

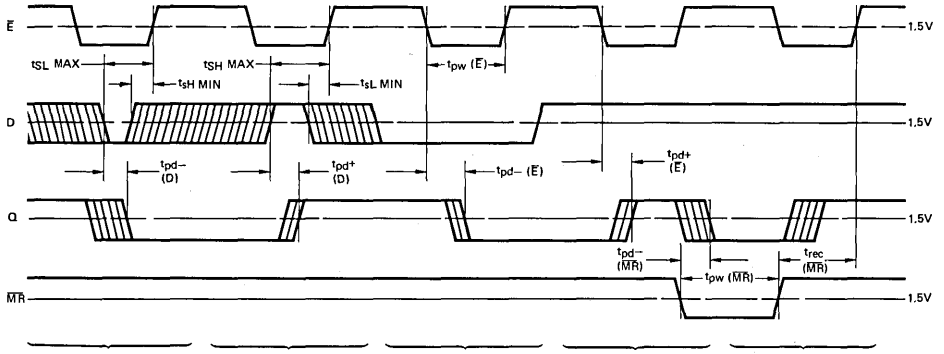
Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 4.92 mA V_{IN} = V_{IH} or V_{IL}		0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.7	Volts
I_{IL} (Note 2)	93L Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.3 V		−0.25	−0.4	mA
I_{IH} (Note 2)	93L Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V		2.0	20	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V	−2.5	−16	−25	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		20	33	mA

Notes: 1) Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by the 93L input load factor. (See loading rules)

SWITCHING CHARACTERISTICS (T_A = 25°C)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{pd+} ($\overline{E}$)	Enable to Output HIGH	V_{CC} = 5.0 V C_L = 15 pF	16	33	75	ns
t_{pd-} ($\overline{E}$)	Enable to Output LOW		15	30	60	
t_{pd+} (D)	Data to Output HIGH		12	25	55	ns
t_{pd-} (D)	Data to Output LOW		15	30	60	
t_s "H"	HIGH Data Set-up Time		2.0		20	ns
t_s "L"	LOW Data Set-up Time		3.0		35	
t_{pw} ($\overline{E}$)	Min. Enable Pulse Width			32	45	ns
t_{pw} ($\overline{MR}$)	Min. Master Reset Pulse Width			27	40	ns
t_{pd-} ($\overline{MR}$)	Master Reset to Output LOW		15	29	60	
t_{rec} ($\overline{MR}$)	Master Reset Recovery Time			20	30	ns

SWITCHING TIME WAVEFORMS



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Am9309
Dual Four-Input Multiplexer

Distinctive Characteristics:

- 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and package hermeticity testing in compliance with MIL-STD-883.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

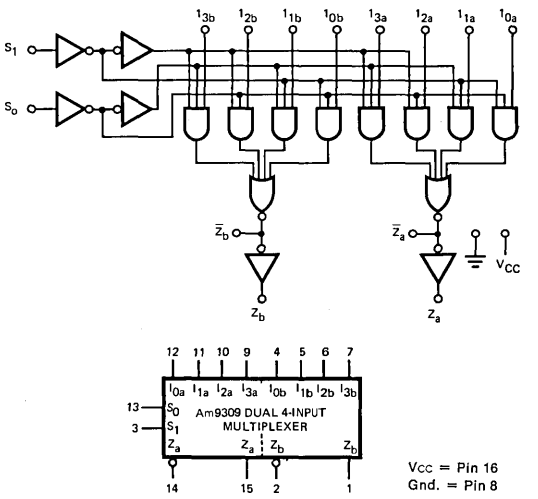
The 9309 Dual Four-Input Multiplexer is the logic implementation of a two-pole four-position switch with the position of the switch set by the logic levels supplied to the Select Inputs S_0 and S_1. Both TRUE and FALSE outputs are provided. The logic equations for each multiplexer output are given below:

$$Z_a = I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0$$
$$Z_b = I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0$$

The logical representation of the 9309 is shown in Truth Table I.

The 9309 will select and direct word data from multiple word registers to a common output buss. Multiple word data bussing using the 9309 is illustrated in Figure 4.

LOGIC DIAGRAM/SYMBOL

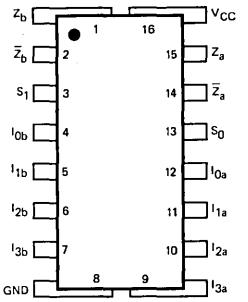


Am9309 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	U6M930959X
Hermetic DIP	0°C to +75°C	U7B930959X
Hermetic DIP	−55°C to +125°C	U7B930951X
Hermetic Flat Pak	−55°C to +125°C	U4L930951X
Dice	Note	UXX9309XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to + 125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

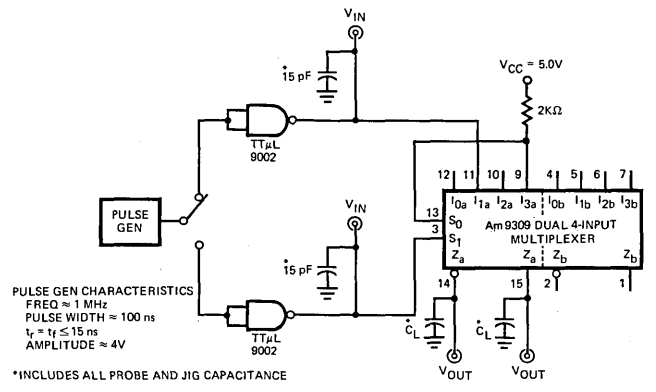
ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am930959X $T_A = 0°C$ to $+75°C$ $V_{CC} = 5.0\ V \pm 5\%$
Am930951X $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0\ V \pm 10\%$

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -0.8$ mA $V_{IN} = V_{IH}$ or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $I_{OL} = 16.0$ mA $V_{IN} = V_{IH}$ or V_{IL}		0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4$ V		−1.0	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.4$ V		6.0	40	μA
	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 5.5$ V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., $V_{OUT} = 0.0$ V	−30		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		30	44	mA

Notes: 1) Typical Limits are at $V_{CC} = 5.0$ V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by input load factor (See Loading Rules).

SWITCHING TIME TEST CIRCUIT



Switching Characteristics (T_A = 25°C)

Parameters		Description	Test Conditions	+25°C Min	Typ	Max	Units
t_{pd+}(ST)	Turn Off Delay	Select Input/TRUE Output	V_{CC} = 5.0 V, C_L = 15 pF (Refer to figures 1 & 3)	10	24	32	ns
t_{pd-}(ST)	Turn On Delay	Select Input/TRUE Output		10	24	32	ns
t_{pd+}(SF)	Turn Off Delay	Select Input/FALSE Output		5	16	21	ns
t_{pd-}(SF)	Turn On Delay	Select Input/FALSE Output		5	17	23	ns
t_{pd+}(DT)	Turn Off Delay	Data Input/TRUE Output		8	17	24	ns
t_{pd-}(DT)	Turn On Delay	Data Input/TRUE Output		8	17	24	ns
t_{pd+}(DF)	Turn Off Delay	Data Input/FALSE Output		2	9	14	ns
t_{pd-}(DF)	Turn On Delay	Data Input/FALSE Output		3	10	15	ns

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH-signal level or when used with V_{CC} to indicate HIGH V_{CC} value.

I Input.

L LOW, applying to a LOW signal level or when used with V_{CC} to indicate LOW V_{CC} value.

O Output.

FUNCTIONAL TERMS:

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

I_{ja}, I_{jb} Data Inputs One of the four multiplexer data inputs for multiplexers a or b, j = 0, 1, 2, 3.

Input Unit Load One T^2L gate input load. In the HIGH state it is equal to I_R and in the LOW state it is equal to I_F.

Z Output The logic TRUE output of the four input multiplexers.

$\overline{Z}$ Output The logic FALSE output of the four input multiplexers.

OPERATIONAL TERMS:

I_{IL} Forward input load current, for unit input load. Refer to Figure 2.

I_{OH} Output HIGH current, forced out of output in V_{OH} test. Refer to figure 2.

I_{OL} Output LOW current, forced into the output in V_{OL} test. Refer to Figure 2.

I_{PD} The current drawn by the device under a +5.0 V power supply bias with input and output terminals open.

I_{IH} Reverse input load current with V_{OH} applied to input. Refer to Figure 2.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage. Refer to Figure 2.

V_{IL} Maximum logic LOW input voltage. Refer to Figure 2.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output. Refer to Figure 2.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output. Refer to Figure 2.

SWITCHING TERMS: (All switching times are measured at the 1.5 V logic level).

t_{pd+}(ST) The propagation delay from a Select Input signal transition to the corresponding TRUE output LOW-HIGH transition. Refer to Figure 1.

t_{pd-}(ST) The propagation delay from a Select Input signal transition to the corresponding TRUE output HIGH-LOW transition. Refer to Figure 1.

t_{pd+}(SF) The propagation delay from a Select Input signal transition to the corresponding FALSE output LOW-HIGH transition. Refer to Figure 1.

t_{pd-}(SF) The propagation delay from a Select Input signal transition to the corresponding FALSE output HIGH-LOW transition. Refer to Figure 1.

t_{pd+}(DT) The propagation delay from a Data Input signal transition to the TRUE output LOW-HIGH transition. Refer to Figure 1.

t_{pd-}(DT) The propagation delay from a Data Input signal transition to the TRUE output HIGH-LOW transition. Refer to Figure 1.

t_{pd+}(DF) The propagation delay from a Data Input signal transition to the FALSE output LOW-HIGH transition. Refer to Figure 1.

t_{pd-}(DF) The propagation delay from a Data Input signal transition to the FALSE output HIGH-LOW transition. Refer to Figure 1.

SWITCHING TIME WAVEFORMS

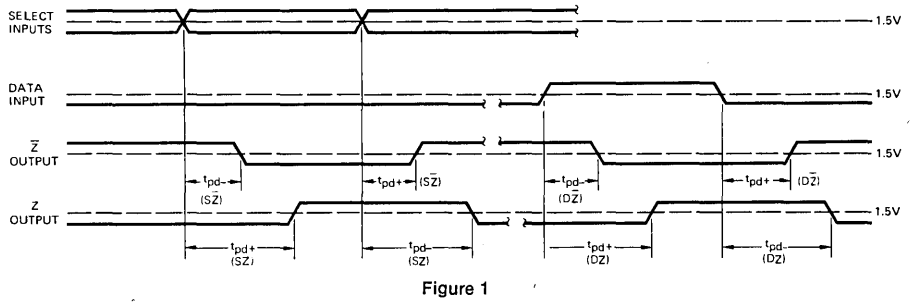
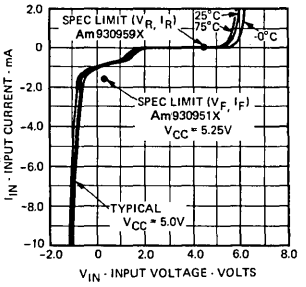


Figure 1

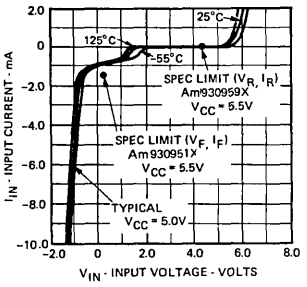
PERFORMANCE CURVES

Input Characteristics

Input Current Versus Input Voltage

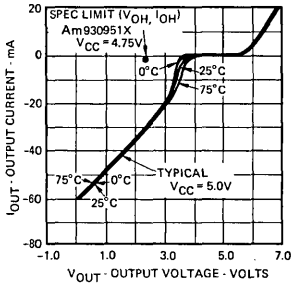


Input Current Versus Input Voltage

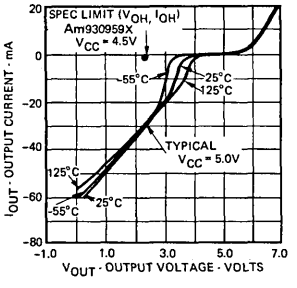


Output Characteristics

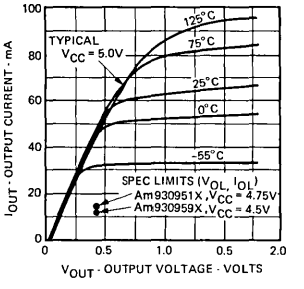
Output HIGH Current Versus Output Voltage



Output HIGH Current Versus Output Voltage

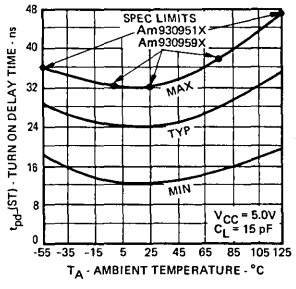


Output LOW Current Versus Output Voltage

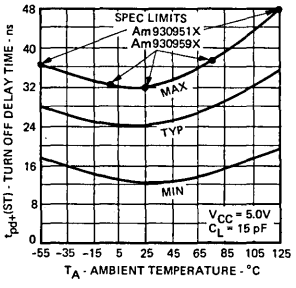


Switching Characteristics

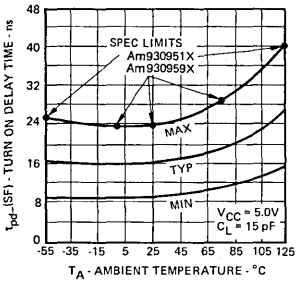
Turn On Delay Select Input to TRUE Output



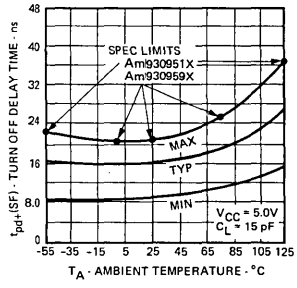
Turn Off Delay Select Input to TRUE Output



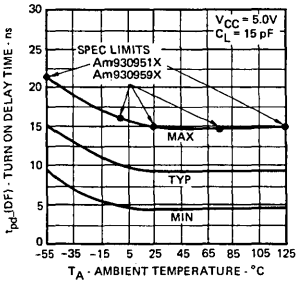
Turn On Delay Select Input to FALSE Output



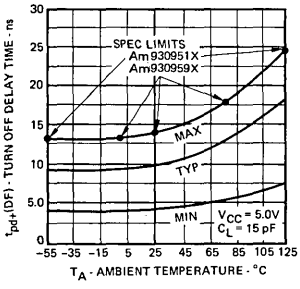
Turn Off Delay Select Input to FALSE Output



Turn On Delay Data Input to FALSE Output



Turn Off Delay Data Input to FALSE Output



TRUTH TABLE

Select Inputs		Data Inputs				Outputs	
S_0	S_1	I_{0a}	I_{1a}	I_{2a}	I_{3a}	Z_a	$\overline{Z}_a$(F)
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L
S_0	S_1	I_{0b}	I_{1b}	I_{2b}	I_{3b}	Z_b	$\overline{Z}_b$(F)
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

TABLE I

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300'	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

TABLE III

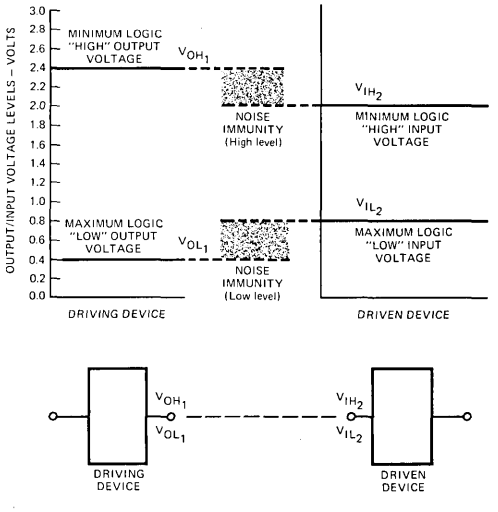
Am9309 LOADING RULES (in unit loads)

Input/Output	Pin No.s	Input Unit Load	Fanout Output HIGH	Fanout Output LOW
I_{0a}	12	1	—	—
I_{1a}	11	1	—	—
I_{2a}	10	1	—	—
I_{3a}	9	1	—	—
I_{0b}	4	1	—	—
I_{1b}	5	1	—	—
I_{2b}	6	1	—	—
I_{3b}	7	1	—	—
S_0	13	1	—	—
S_1	3	1	—	—
Z_a	15	—	20	10
Z_b	1	—	20	10
$\overline{Z}_a$	14	—	20	10
$\overline{Z}_b$	2	—	20	10
GND	8	—	—	—
V_{CC}	16	—	—	—

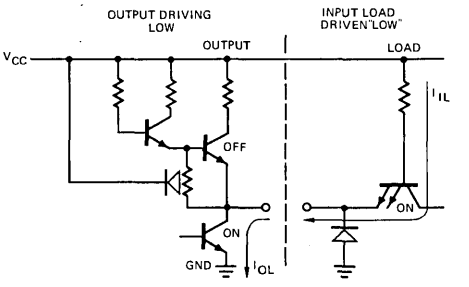
TABLE II

INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH



Current Interface Conditions — LOW



Current Interface Conditions — HIGH

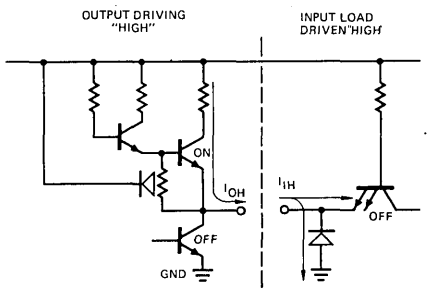


Figure 2

MULTIPLE WORD BUSSING

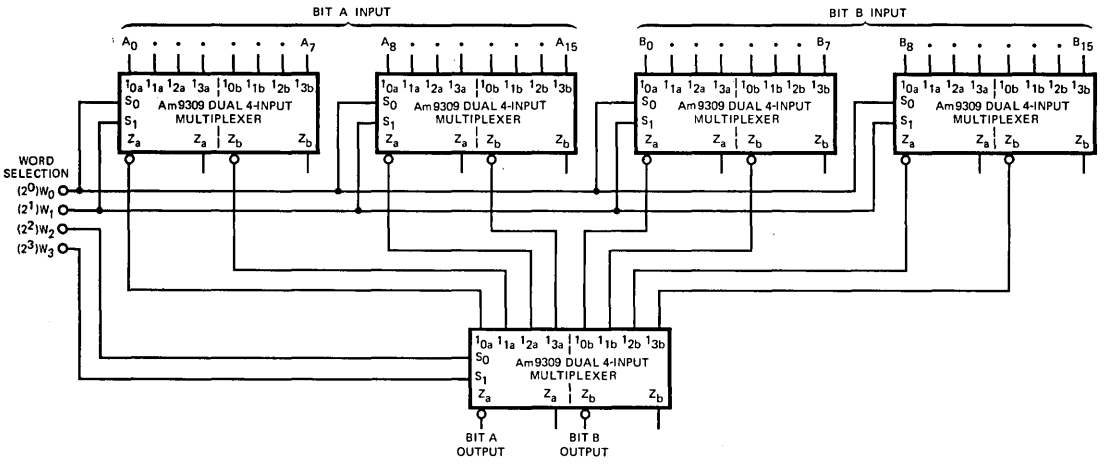
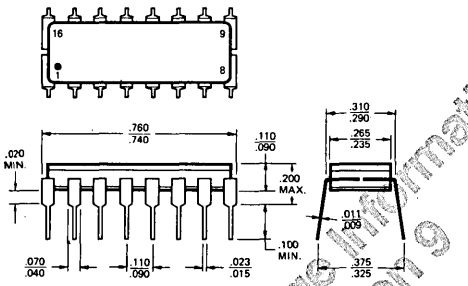


Figure 4

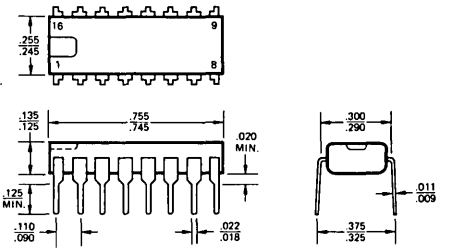
The interconnection of five 9309 Dual Four-Input Multiplexers will switch a two bit data word from one of sixteen two bit words onto a data buss. The selection of the word transferred to the buss is made by the address supplied to the W_0, W_1, W_2, and W_3 inputs.

PHYSICAL DIMENSIONS
Dual-In-Line

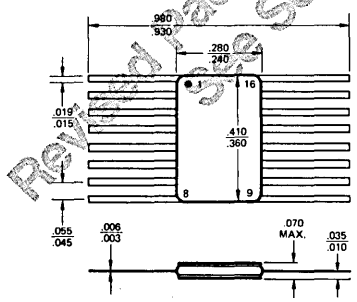
Hermetic



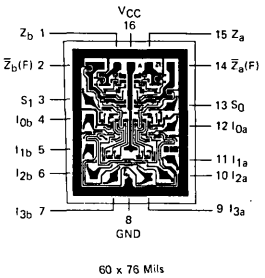
Molded



PHYSICAL DIMENSIONS
Flat Package



Metallization and Pad Layout



60 x 76 Mils

ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am93L09

Low-Power Dual Four-Input Multiplexer

Distinctive Characteristics

- 30 ns typical propagation delay.
- 38 mw typical power dissipation.
- 100% reliability assurance testing in compliance with MIL STD 883.
- Compatible with 7400 and 9300 series devices

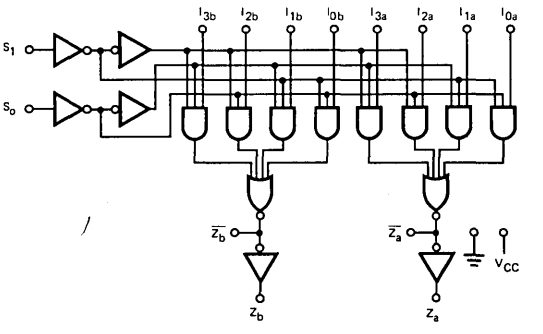
FUNCTIONAL DESCRIPTION

The Am93L09 consists of two four-input multiplexers controlled by two common select lines. The logic levels on the two select lines S_0 and S_1 determine which of the four inputs will be fed to the outputs of each multiplexer, so the device can select two bits of data from any one of four sources. Both assertion and negation outputs are provided for each multiplexer; the negation outputs are slightly faster. The Am93L09 can also be used to generate a random function of three variables by connecting two of the variables to the select inputs and connecting the multiplexer inputs HIGH or LOW or to the true or complement of the third variable.

DATA SELECTION TABLE

Select lines		Outputs			
S_0	S_1	Z_a	$\overline{Z_a}$	Z_b	$\overline{Z_b}$
L	L	I_{0a}	$\overline{I_{0a}}$	I_{0b}	$\overline{I_{0b}}$
H	L	I_{1a}	$\overline{I_{1a}}$	I_{1b}	$\overline{I_{1b}}$
L	H	I_{2a}	$\overline{I_{2a}}$	I_{2b}	$\overline{I_{2b}}$
H	H	I_{3a}	$\overline{I_{3a}}$	I_{3b}	$\overline{I_{3b}}$

LOGIC DIAGRAM



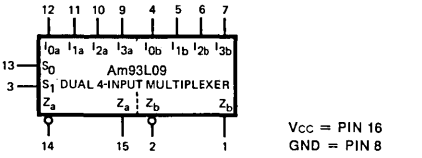
LOADING RULES

In Unit Loads (Notes)

Input Load Factor	TTL loads HIGH	TTL loads LOW	93L loads HIGH	93L loads LOW
All Inputs	0.5	0.25	1.0	1.0
Output Drive	HIGH	LOW	HIGH	LOW
All Outputs	10.0	3.0	20.0	12.0

NOTES:
1) A TTL unit load is specified as 0.4 V at −1.6 mA LOW, 2.4 V at 40 μA HIGH.
2) A 93L unit load is specified as 0.3 V at −400 μA LOW, 2.4 V at 20 μA HIGH.
3) Enough output LOW current is available to mix TTL and 93L loads and still meet the 93L requirement of a V_{OL} of 0.3 V.

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

Am93L09 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
16-Pin Molded DIP	0°C to +75°C	U6M93L0959X
16-Pin Hermetic DIP	0°C to +75°C	U7B93L0959X
16-Pin Hermetic DIP	−55°C to +125°C	U7B93L0951X
16-Pin Hermetic Flat Pak	−55°C to +125°C	U4L93L0951X
Dice	Note	UXX93L09XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current (Note 1)	−30 mA to +5.0 mA

Note 1. Maximum current defined by DC input voltage.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93L0959X T_A = 0°C to +75°C V_{CC} = 4.75 V to 5.25 V
Am93L0951X T_A = −55°C to +125°C V_{CC} = 4.50 V to 5.50 V

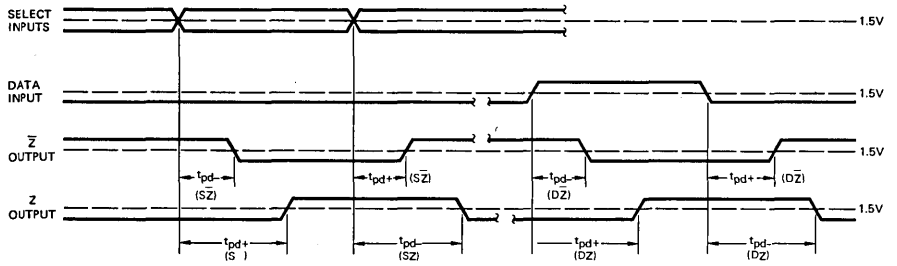
Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 4.92 mA V_{IN} = V_{IH} or V_{IL}		0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.7	Volts
I_{IL} (Note 2)	93L Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.3 V		−0.25	−0.4	mA
I_{IH} (Note 2)	93L Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V		2.0	20	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V	−10	−26	−40	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		7.5	11.5	mA

Notes: 1) Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by the 93L input load factor. (See loading rules)

SWITCHING CHARACTERISTICS (T_A = 25°C)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{pd+} (SZ)	Select to Z Output HIGH	V_{CC} = 5.0 V, C_L = 15 pF	19	38	70	ns
t_{pd-} (SZ)	Select to Z Output LOW		19	38	65	ns
t_{pd+} ($S\overline{Z}$)	Select to $\overline{Z}$ Output HIGH		12	24	50	ns
t_{pd-} ($S\overline{Z}$)	Select to $\overline{Z}$ Output LOW		14	27	55	ns
t_{pd+} (DZ)	Data Input to Z Output HIGH		22	43	70	ns
t_{pd-} (DZ)	Data Input to Z Output LOW		18	35	65	ns
t_{pd+} ($D\overline{Z}$)	Data Input to $\overline{Z}$ Output HIGH		11	22	40	ns
t_{pd-} ($D\overline{Z}$)	Data Input to $\overline{Z}$ Output LOW		15	30	60	ns

SWITCHING TIME WAVEFORMS



ADVANCED MICRO DEVICES INC.
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TELEX: 34-6306

Am9310/9316

BCD Decade Counter/Four-Bit Binary Counter

Distinctive Characteristics:

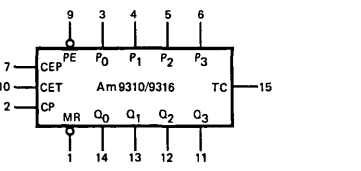
- Fully synchronous counting and parallel loading
- Electrically tested and optically inspected dice for the assemblers of hybrid products.
- Mixing privileges for obtaining price discounts. Refer to price list.
- 100% reliability assurance testing including high – temperature bake, temperature cycling, centrifuge and package hermeticity testing in compliance with MIL STD 883.

FUNCTIONAL DESCRIPTION

The Am9310 and Am9316 are four-bit synchronous up-counters. The 9310 is a modulo 10 counter and the 9316 is a hexadecimal counter. Each counter contains four master-slave flip-flops driven by a common clock input (CP). When CP is LOW, data is entered into the masters of the flip-flops. If the Parallel enable ($\overline{PE}$) is HIGH, then data is entered into each master from the slaves of the other flip-flops via J and K type inputs. If $\overline{PE}$ is LOW, then data is entered into the masters via the D-type parallel inputs (P_0, P_1, P_2, P_3). When the clock changes from LOW to HIGH, the data in the masters is transferred to the slaves and the outputs (Q_0, Q_1, Q_2, Q_3). The masters are inhibited from change as long as the clock is HIGH. In the count mode ($\overline{PE}$ HIGH), there are two count enables, count enable parallel (CEP) and count enable trickle (CET). Both must be HIGH for counting to occur. The terminal count state of each device (9 for the 9310 and 15 for the 9316) is decoded and ANDed with the CET input to produce a terminal count output (TC). Long synchronous counter systems are constructed by connecting the TC output of the first counter to the CEP inputs of all other counters and the TC output of each counter after the first to the CET input of the next counter. Both counters have an asynchronous master reset ($\overline{MR}$) which clears all four flip-flops independent of any other inputs.

For proper operation, the $\overline{PE}$ input must not change from LOW to HIGH during the clock LOW time unless the P_i inputs are identical to the Q_i outputs. If CEP and CET are both HIGH at any time during the clock LOW time, (and $\overline{PE}$ is HIGH), then the count will increment when the clock goes HIGH.

LOGIC SYMBOL

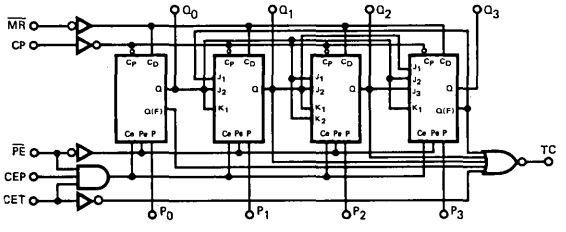


V_{CC} = PIN 16
GND = PIN 8

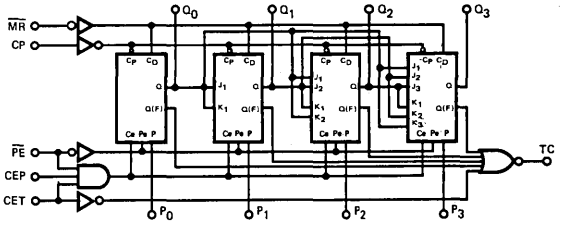
The basic cell for the Am9310/9316 is illustrated in Figure 8.

LOGIC DIAGRAMS

Am9310



Am9316

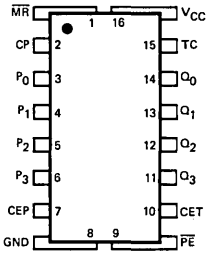


Am9310 ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am9310	Molded DIP	0°C to +75°C	U6M931059X
Am9310	Hermetic DIP	0°C to +75°C	U7B931059X
Am9310	Hermetic DIP	−55°C to +125°C	U7B931051X
Am9310	Hermetic Flat Pak	−55°C to +125°C	U4L931051X
Am9310	Dice	Note	UXX9310XXD
Am9316	Molded DIP	0°C to +75°C	U6M931659X
Am9316	Hermetic DIP	0°C to +75°C	U7B931659X
Am9316	Hermetic DIP	−55°C to +125°C	U7B931651X
Am9316	Hermetic Flat Pak	−55°C to +125°C	U4L931651X
Am9316	Dice	Note	UXX9316XXD

Note : The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current (Note 1)	−30 mA to +5 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am931059X/Am931659X T_A = 0°C to +75°C V_{CC} = 5.0 V ±5%
Am931051X/Am931651X T_A = −55°C to +125°C V_{CC} = 5.0 V ±10%

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.8 mA V_{IN} = V_{IH} or V_{IL}		2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16.0 mA V_{IN} = V_{IH} or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V			−1.0	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V			6.0	40	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V		−20		−80	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.	Am931051X Am931651X		65	100	mA
			Am931059X Am931659X		65	94	

Notes: 1) Typical Limits are at V_{CC} = 5.0 V, 25°C Ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by input load factor (See Loading Rules).

SWITCHING CHARACTERISTICS (T_A = 25°C)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{pd+}	Turn Off Delay—Q Outputs	V_{CC} = 5.0 V, C_L = 15 pF (Refer to Figure 1)	10	20	30	ns
t_{pd-}	Turn On Delay—Q Outputs		7	15	25	ns
t_{pd+}(TC)	Turn Off Delay TC		17	35	50	ns
t_{pd-}(TC)	Turn On Delay TC		10	20	30	ns
t_s(CE)	Set-up Time CEP or CET	V_{CC} = 5.0 V, C_L = 15 pF (Refer to Figure 2)	0	13	30	ns
t_s(P)	Set-up Time P-Inputs	V_{CC} = 5.0 V, C_L = 15 pF (Refer to Figure 3)	0	18	38	ns
$t_s(\overline{PE})$	Set-up Time $\overline{PE}$		7	29	45	ns
$t_{pd-}(\overline{MR})$	Turn-on Delay for $\overline{MR}$	V_{CC} = 5.0 V, C_L = 15 pF (Refer to Figure 1)	15	33	48	ns
t_{pd+}(CET to TC)	Turn Off Delay for CET to TC	V_{CC} = 5.0 V, C_L = 15 pF (Refer to Figure 4)	7	14	30	ns
t_{pd-}(CET to TC)	Turn On Delay for CET to TC		7	14	30	ns
f_c	Count Frequency	V_{CC} = 5.0 V, C_L = 15 pF	20	28		MHz

DEFINITION OF TERMS

SUBSCRIPT TERMS:

Forward, applying to LOW inputs.

HIGH, applying to a HIGH logic level or when used with V_{CC} to dicate high V_{CC} value.

Input.

LOW, applying to LOW logic level or when used with V_{CC} to dicate low V_{CC} value.

Output.

Reverse, applying to HIGH inputs.

JNCTIONAL TERMS:

synchronous (ripple) Counter All outputs (flip flops) change state command from a preceding stage.

Input Asynchronous direct clear input.

EP Input The count mode is inhibited by a LOW input. Outputs Q_0, Q_1, Q_2 and Q_3 remain unchanged. Refer to Truth Table II.

ET Input The count mode is inhibited and Terminal Count (TC) itput is forced LOW by a LOW input. Outputs Q_0, Q_1, Q_2 and Q_3 main unchanged. Refer to Truth Table II.

n-Out The logic HIGH or LOW output drive capability in terms Input Unit Loads.

put Unit Load One T^2L gate input load. In the HIGH state it is ual to I_R and in the LOW state it is equal to I_F.

Flip Flop Properties similar to an RS Flip Flop except that = K = 1 is allowed. Refer to Truth Table I.

K Inputs The logic inputs for setting the JK flip flop of the gister. Refer to Table I.

R Input The master reset input.

Input The input for selection of parallel data entry to the gister. Parallel Enable (PE) LOW allows parallel data entry.

P_1, P_2, P_3 Inputs The inputs for data entry into the four synchro- us clocked JK Flip Flops. Refer to Table II.

Q_1, Q_2, Q_3 Outputs The four outputs of the 9310/9316 register flops.

(t_n) The output after the n'th clock pulse.

(t_{n+1}) The output after the (n+1) clock pulse.

nchronous Counter All outputs (flip flops) change state on mmand from the clock.

rminal Count The highest number a counter can attain when erated in the count mode.

Output This output is HIGH when CET is HIGH and the counter at terminal count. The output is LOW when CET is LOW or the unter not at terminal count.

ERATIONAL TERMS:

Forward input load current for unit input load.

Output HIGH current forced out of output in V_{OH} test.

Output LOW current forced into the output in V_{OL} test.

I_{IL} Reverse input load current with V_{IL} applied to input.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage. Refer to Figure 6.

V_{IL} Maximum logic LOW input voltage. Refer to Figure 6.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

SWITCHING TERMS: (All switching times are measured at the 1.5 V logic level)

CP Clock Pin, pulsed. The subscript, if any, refers to pulse wave- shape.

t_{pd-} The propagation delay from the clock signal LOW-HIGH transition to an output signal HIGH-LOW transition. Refer to Figure 1.

t_{pd+} The propagation delay from the clock signal LOW-HIGH transition to an output signal LOW-HIGH transition. Refer to Figure 1.

t_{pd-}($\overline{MR}$) The propagation delay from the master reset signal HIGH-LOW transition to the TRUE output signal HIGH-LOW transi- tion. Refer to Figure 4.

t_{pd+}(CET to TC) The propagation delay from the CET input LOW- HIGH transition to the TC output LOW-HIGH transition. Refer to Figure 5.

t_{pd-}(CET to TC) The propagation delay from the CET input HIGH- LOW transition to the TC output HIGH-LOW transition. Refer to Figure 5.

t_{pd+}(TC) The propagation delay from the clock signal LOW-HIGH transition to the TC output LOW-HIGH transition. Refer to Figure 1.

t_{pd-}(TC) The propagation delay from the clock signal LOW-HIGH transition to the TC output HIGH-LOW transition. Refer to Figure 1.

t_s (CE) The set-up time of the count enable inputs (CET or CEP) relative to either edge of the clock. To inhibit counting, one of the count enables must be LOW by t_s (CE) max before the clock goes LOW and must remain LOW until after t_s (CE) min before the clock goes HIGH. To enable counting, both of the count enables must be HIGH before t_s (CE) max before the clock goes HIGH.

t_s (P) The set-up time for data on the P inputs, relative to the clock LOW to HIGH transition. In order to correctly load data into the counter, the P inputs must be steady between t_s (P) max and t_s (P) min before the clock goes HIGH.

t_s ($\overline{PE}$) The set-up time on the parallel enable input. To load data from the P inputs into the counter, the parallel enable must be LOW by t_s ($\overline{PE}$) max before the clock goes HIGH and must remain LOW until after t_s ($\overline{PE}$) min before the clock goes HIGH.

SWITCHING TIME WAVEFORMS

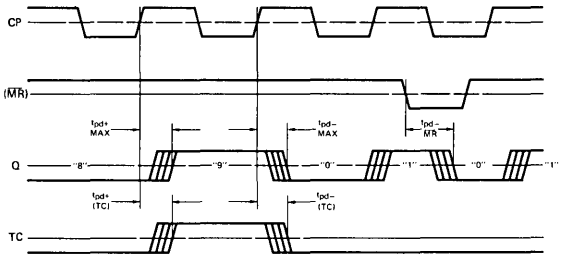


Figure 1

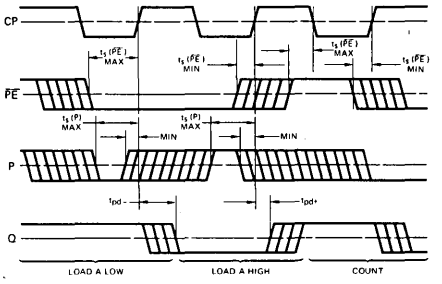


Figure 3

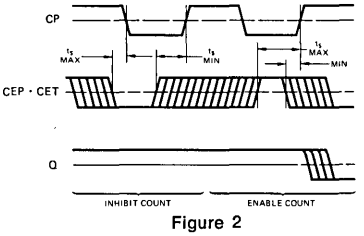


Figure 2

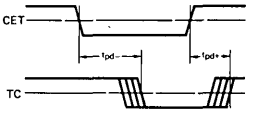


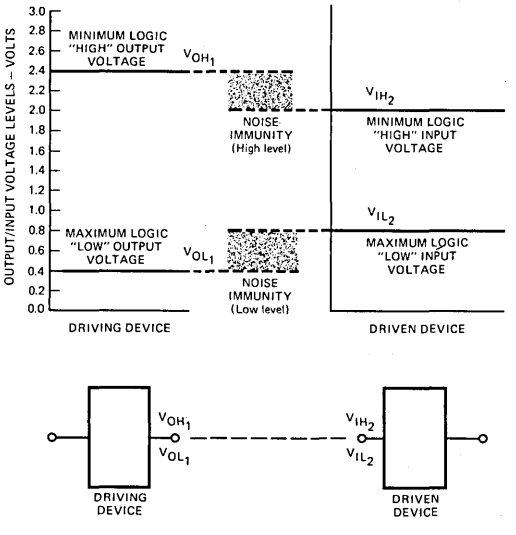
Figure 4

Switching tests are performed with CP input driven by a TTμL9002 gate and the outputs loaded by 15 pF capacitance to include jig capacitance. All unused inputs are tied to V_{CC}. The pulse generator driving the TTμL9002 is set up in the following condition:

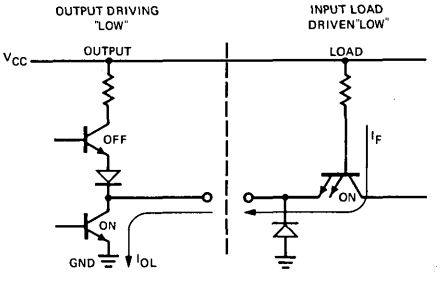
Rise Time <15 ns
Fall Time <15 ns
Amplitude ≈4 V
Frequency = 2 MHz ±5% at 50% duty cycle

INPUT/OUTPUT INTERFACE CONDITIONS

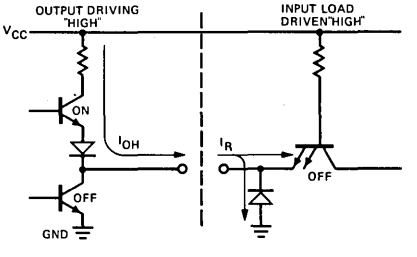
Voltage Interface Conditions — LOW & HIGH



Current Interface Conditions — LOW

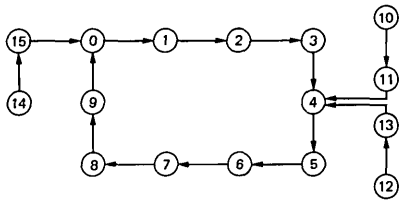


Current Interface Conditions — HIGH

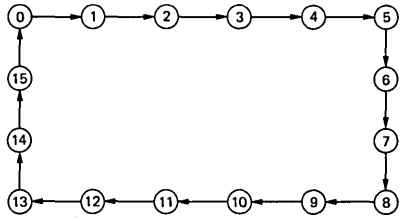


Am9310/16 STATE DIAGRAMS

Am9310



Am9316



The state diagrams show the count sequence after the counters are preset to any one of the sixteen possible states.

Figure 7

Am9310/16 LOADING RULES (in unit loads)

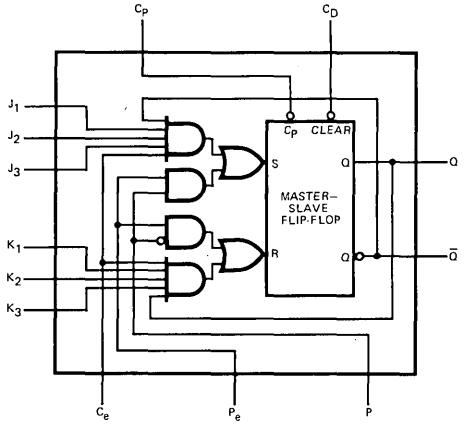
Input/Output	Pin No.'s	Input Unit Load	Output Drive (note) Output HIGH	Output LOW
$\overline{MR}$	1	1	—	—
CP	2	2	—	—
P_0	3	2/3	—	—
P_1	4	2/3	—	—
P_2	5	2/3	—	—
P_3	6	2/3	—	—
CEP	7	1	—	—
GND	8	—	—	—
$\overline{PE}$	9	2	—	—
CET	10	2	—	—
Q_3	11	—	20	10
Q_2	12	—	20	10
Q_1	13	—	20	10
Q_0	14	—	20	10
TC	15	—	20	10
V_{CC}	16	—	—	—

Note: 10 loads are allowed on any output, but the total number of loads on all outputs must not exceed 30. A unit load is defined as 40μA at 2.4V and 1.6mA at 0.4V.

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Am9310/16 BASIC CELL



This basic cell illustrates how data is entered and controlled internally. Count enable gating is also shown.

Figure 8

TRUTH TABLES

Mode Selection

CEP	CET	$\overline{PE}$	Mode
H	H	H	Count
L	X	H	Count Inhibited
X	L	H	Count Inhibited
X	X	L	Presetting

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

TABLE II

JK Flip Flop

J	K	Q_0 (tn+1)
L	L	Q_0(tn) No change
L	H	L
H	L	H
H	H	Q_0(tn) Toggle

$J = J_1 \bullet J_2 \bullet J_3$
$K = K_1 \bullet K_2 \bullet K_3$

TABLE I

MULTI-STAGE SYNCHRONOUS COUNTER

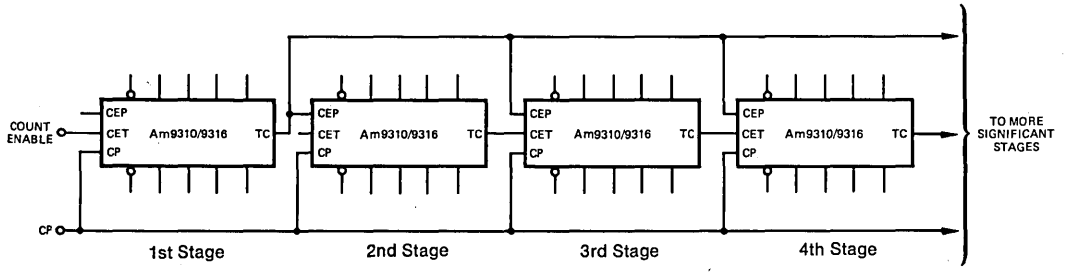


Figure 9

Am9310/9316 APPLICATION

Counter stages can be cascaded, as shown above, to provide multiple stage BCD or Binary synchronous counting by using the 9310 or the 9316 respectively. With a TC fan-out of six the above scheme allows seven stages to operate at the maximum frequency equivalent to a two stage counter.

Each stage is enabled for counting when both its CEP and CET inputs are HIGH. CEP of subsequent stages are HIGH when the first stage is at Terminal Count. CET of a stage is HIGH when all of its preceding stages (first stage not included) are at Terminal Count.

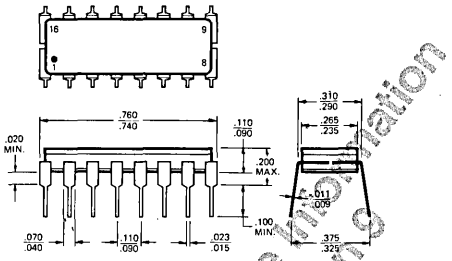
This indicates that CET_n is enabled by TC_{n-1}. TC_{n-1} in turn is HIGH when CET_{n-1} is enabled. CET_{n-1} is enabled by TC_{n-2}, until the second stage, where the CET_2 is always open (HIGH). This TC/CET look ahead ripple is initiated when the second stage reaches Terminal Count and must arrive at the CET input of the last stage before the first stage reaches Terminal Count again. This will happen ten clock pulses (sixteen for the 9316) after the look ahead ripple is initiated.

A multi stage counter as illustrated above can operate at a typical clock frequency of 20 MHz.

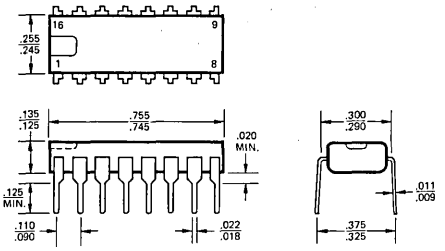
PHYSICAL DIMENSIONS

Dual-In-Line

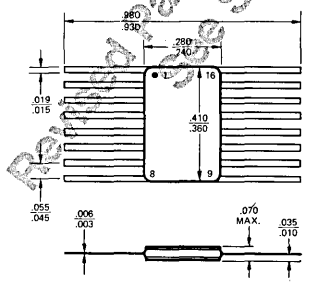
Hermetic



Molded

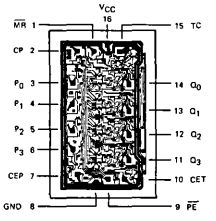


Flat Package



Metallization and Pad Layout

74 x 124 Mils



ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am93L10/93L16

Low-Power BCD Decade Counter/Four-Bit Binary Counter

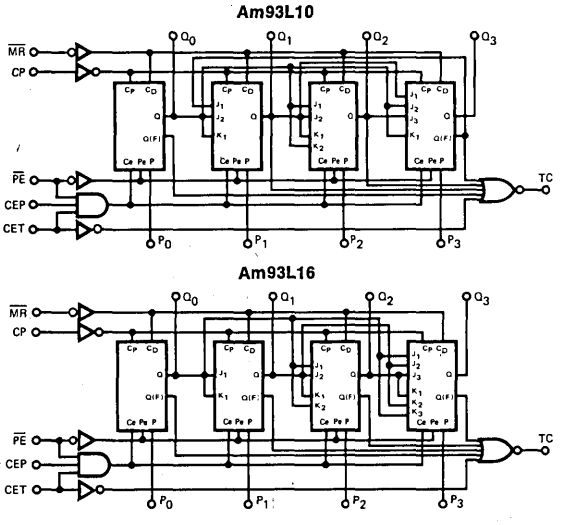
Distinctive Characteristics

- 75 mw typical power dissipation.
- 13 MHz typical count rate
- 100% reliability assurance testing in compliance with MIL STD 883
- Fully synchronous counting and parallel loading

FUNCTIONAL DESCRIPTION

The Am93L10 and Am93L16 are four-bit synchronous up-counters. The 93L10 *is a modulo 10 counter and the 93L16 is a hexadecimal counter.* Each counter contains four master-slave flip-flops driven by a common clock input (CP). When CP is LOW, data is entered into the masters of the flip-flops. If the parallel enable ($\overline{PE}$) is HIGH, then data is entered into each master from the slaves of the other flip-flops via J and K type inputs. If $\overline{PE}$ is LOW, then data is entered into the masters via the D-type parallel inputs (P_0, P_1, P_2, P_3). When the clock changes from LOW to HIGH, the data in the masters is transferred to the slaves and the outputs (Q_0, Q_1, Q_2, Q_3). The masters are inhibited from change as long as the clock is HIGH. *In the count mode ($\overline{PE}$ HIGH), there are two count enables, count* enable parallel (CEP) and count enable trickle (CET). Both must be HIGH for counting to occur. The terminal count state of each device (9 for the 93L10 and 15 for the 93L16) is decoded and ANDed with the CET input to produce a terminal count output (TC). Long synchronous counter systems are constructed by connecting the TC output of the first counter to the CEP inputs of all other counters and the TC output of each counter after the first to the CET input of the next counter. Both counters have an asynchronous master reset ($\overline{MR}$) which clears all four flip-flops independent of any other inputs.

For proper operation, the $\overline{PE}$ input must not change from LOW to HIGH during the clock LOW time unless the P_i inputs are identical to the Q_i outputs. If CEP and CET are both HIGH at any time during the clock LOW time, (and $\overline{PE}$ *is HIGH), then the count will increment when the clock goes HIGH.*



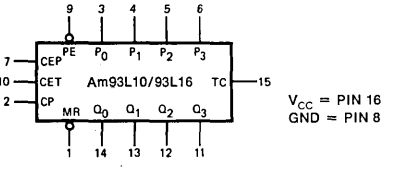
LOADING RULES

In Unit Loads (Notes)

	TTL LOADS		93L LOADS	
Input Load Factor	HIGH	LOW	HIGH	LOW
CEP, $\overline{MR}$	0.5	0.25	1.0	1.0
CET, CP, $\overline{PE}$	1.0	0.5	2.0	2.0
P_0, P_1, P_2, P_3	0.34	0.17	0.68	0.68
Output Drive	HIGH	LOW	HIGH	LOW
Q_0, Q_1, Q_2, Q_3, TC	9	3	18	12

NOTES:
1) A TTL *unit load is specified as* 0.4 V at −1.6 mA LOW, 2.4 V at 40 μA HIGH.
2) A 93L unit load is specified as 0.3 V at −400 μA LOW, 2.4 V at 20 μA HIGH.
3) Enough output LOW current is available to mix TTL and 93L loads and still meet the 93L requirement of a V_{OL} of 0.3 V.

LOGIC SYMBOL



ORDERING INFORMATION

Package Type	Temperature Range	Am93L10 Order Number	Am93L16 Order Number
16-Pin Molded DIP	0°C to +75°C	U6M93L1059X	U6M93L1659X
16-Pin Hermetic DIP	0°C to +75°C	U7B93L1059X	U7B93L1659X
16-Pin Hermetic DIP	−55°C to +125°C	U7B93L1051X	U7B93L1651X
16-Pin Hermetic Flat Pak	−55°C to +125°C	U4L93L1051X	U4L93L1651X
Dice	Note	UXX93L10XXD	UXX93L16XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to $+V_{CC}$ max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current (Note 1)	−30 mA to +5.0 mA

Note 1. Maximum current defined by DC input voltage.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93L1059X, Am93L1659X $T_A = 0°C$ to $+75°C$ $V_{CC} = 4.75$ V to 5.25 V
Am93L1051X, Am93L1651X $T_A = -55°C$ to $+125°C$ $V_{CC} = 4.50$ V to 5.50 V

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -0.36$ mA $V_{IN} = V_{IH}$ or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $I_{OL} = 4.92$ mA $V_{IN} = V_{IH}$ or V_{IL}		0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.7	Volts
I_{IL} (Note 2)	93L Unit Load Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.3$ V		−0.25	−0.4	mA
I_{IH} (Note 2)	93L Unit Load Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.4$ V		2.0	20	μA
	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 5.5$ V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., $V_{OUT} = 0.0$ V	−2.5	−16	−25	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		15	27.5	mA

Notes: 1) Typical limits are at $V_{CC} = 5.0$ V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by the 93L input load factor. (See loading rules)

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{pd+}	Turn Off Delay—Q Outputs	$V_{CC} = 5.0$ V, $C_L = 15$ pF (Refer to Figure 1)	18	35	50	ns
t_{pd-}	Turn On Delay—Q Outputs		20	40	55	ns
t_{pd+}(TC)	Turn Off Delay TC		40	80	95	ns
t_{pd-}(TC)	Turn On Delay TC		18	35	45	ns
t_s(CE)	Set-up Time CEP or CET	$V_{CC} = 5.0$ V, $C_L = 15$ pF (Refer to Figure 2)	10	50	80	ns
t_s(P)	Set-up Time P-Inputs	$V_{CC} = 5.0$ V, $C_L = 15$ pF (Refer to Figure 3)	30	70	110	ns
$t_s(\overline{PE})$	Set-up Time $\overline{PE}$		10	45	80	ns
$t_{pd-}(\overline{MR})$	Turn-on Delay for $\overline{MR}$	$V_{CC} = 5.0$ V, $C_L = 15$ pF (Refer to Figure 1)	26	52	95	ns
t_{pd+}(CET to TC)	Turn Off Delay for CET to TC	$V_{CC} = 5.0$ V, $C_L = 15$ pF (Refer to Figure 4)	18	35	55	ns
t_{pd-}(CET to TC)	Turn On Delay for CET to TC		20	40	60	ns
f_c	Count Frequency	$V_{CC} = 5.0$ V, $C_L = 15$ pF	8	13		MHz

SWITCHING TIME WAVEFORMS

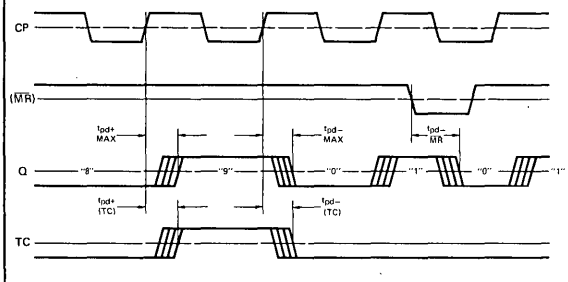


Figure 1

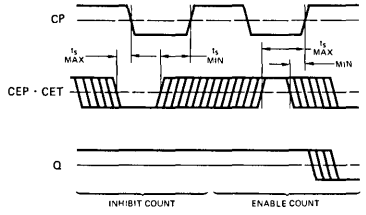


Figure 2

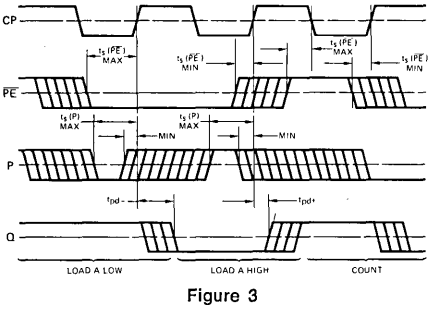


Figure 3

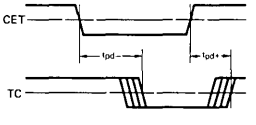


Figure 4

ADVANCED MICRO DEVICES INC.
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TELEX: 34-6306

Am9311 • Am54/74154
Demultiplexer/One of Sixteen Decoder

Distinctive Characteristics:

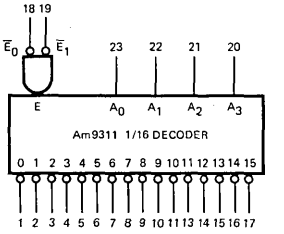
- 100% reliability assurance Testing including high-temperature bake, temperature cycling, centrifuge and package hermeticity testing in compliance with MIL-STD-883.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

The Am9311 Demultiplexer/One-of-Sixteen Decoder accepts four inputs and selects one of sixteen mutually exclusive active LOW outputs as shown in Table II. The Am9311 is enabled by a LOW signal on $\overline{E}_0$ and $\overline{E}_1$ inputs.

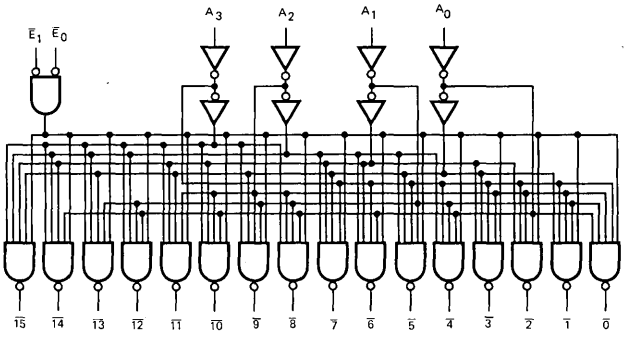
Incoming data on either $\overline{E}_0$ or $\overline{E}_1$ with the other enable input held LOW can be demultiplexed to any one of the sixteen outputs, zero through fifteen, with binary addressing at inputs A_0, A_1, A_2 and A_3. This demultiplexing capability is shown in Figure 9.

LOGIC SYMBOL



V_{CC} = PIN 24
GND = PIN 12

LOGIC DIAGRAM

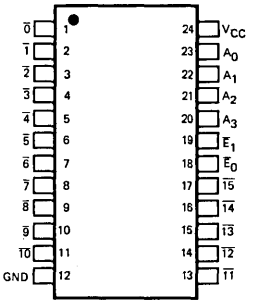


Am9311/Am54/74154 ORDERING INFORMATION

Package Type	Ambient Temperature	Am9311 Order Number	Am54/74154 Order Number
Molded DIP	0°C to +75°C	Am9311C	SN74154N
Hermetic DIP	0°C to +75°C	U6N931159X	SN74154J
Hermetic DIP	−55°C to +125°C	U6N931151X	SN54154J
Flat Pak	−55°C to +125°C	U4M931151X	SN54154W
Dice	Note	UXX9311XXD	SN74154D

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°
Temperature (Ambient) Under Bias	−55°C to +125°
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5 V to +7
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} m
DC Input Voltage	−0.5 V to +5.5
Output Current, Into Outputs	30 m
DC Input Current	−30 mA to +5 m

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am931159X Am74154 T_A = 0°C to +75°C V_{CC} = 5.0 V ±5%
Am931151X Am54154 T_A = −55°C to +125°C V_{CC} = 5.0 V ±10%

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.8 mA V_{IN} = V_{IH} or V_{IL}		2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16.0 mA V_{IN} = V_{IH} or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V			−1.0	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V			6.0	40	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V		−20		−70	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.	Am931151X Am54154		35	49	mA
			Am931159X Am74154		35	56	

Notes: 1) Typical Limits are at V_{CC} = 5.0 V, 25°C Ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by input load factor (See Loading Rules).

Switching Characteristics (T_A = 25°C)

Parameters		Test Conditions	Min	Typ	Max	Units
$t_{pd+}(A\overline{O})$	Turn Off Delay A input to output	V_{CC} = 5.0 V, C_L = 15 pF Refer to Figure 6	10	22	31	ns
$t_{pd-}(A\overline{O})$	Turn On Delay A input to output		7	21	28	ns
$t_{pd+}(\overline{E}\overline{O})$	Turn Off Delay Enable input to output		10	15	23	ns
$t_{pd-}(\overline{E}\overline{O})$	Turn On Delay Enable input to output		7	15	22	ns

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS:

Decoder/Demultiplexer On the basis of an applied instruction, channels of communication are selected which connect certain sources of information to certain destinations e.g., the distribution of timing signals; the interconnection between arithmetic registers.

$\overline{E}_0$, $\overline{E}_1$ Enable Inputs. The device is enabled when both the Enable inputs are LOW.

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

Input Unit Load One T^2L gate input load. In the HIGH state it is equal to 40μA at 2.4V and in the LOW state it is equal to 1.6mA at 0.4V.

$\overline{O}j$ Active LOW output of *Demultiplexer/Decoder* j = 0-15.

OPERATIONAL TERMS:

I_{OH} Output HIGH current forced out of output in V_{OH} test.

I_{OL} Output LOW current forced into the output in V_{OL} test.

I_{IH} Reverse input load current with V_{OH} applied to input.

Negative Current Current flowing out of the device.

Positive Current *Current flowing into the device.*

V_{IH} Minimum logic HIGH input voltage. Refer to Figure 7.

V_{IL} Maximum logic LOW input voltage. Refer to Figure 7.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

SWITCHING TERMS: (All switching times are measured at the 1.5 V logic level)

$t_{pd+}(A\overline{O})$ The propagation delay from input address transition to the output LOW to HIGH transition.

$t_{pd-}(A\overline{O})$ The propagation delay from input address transition to the output HIGH to LOW transition.

$t_{pd+}(\overline{E}\overline{O})$ The propagation delay from input Enable LOW to HIGH transition to the output LOW to HIGH transition.

$t_{pd-}(\overline{E}\overline{O})$ The propagation delay from input Enable HIGH to LOW transition to the output HIGH to LOW transition.

PERFORMANCE CURVES

Input/Output Characteristics

Input Current Versus Input Voltage

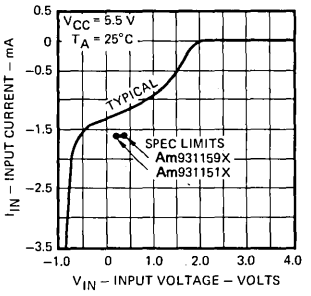


Figure 1

Output Current Versus Output Voltage Output Low

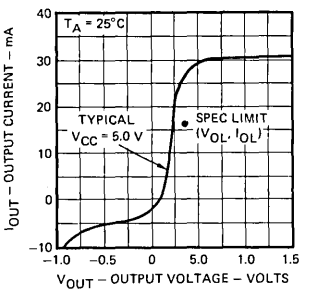


Figure 2

Output Current Versus Output Voltage Output High

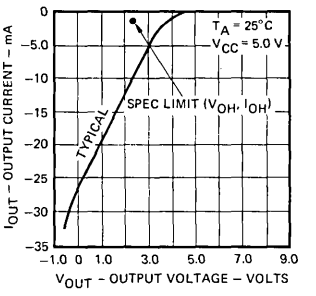


Figure 3

Switching Characteristics

Typical Turn On Delay Versus Temperature

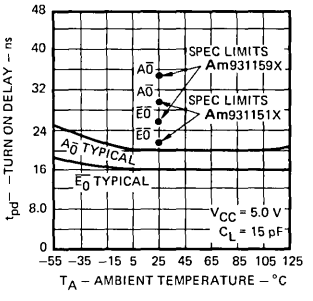


Figure 4

Typical Turn Off Delay Versus Temperature

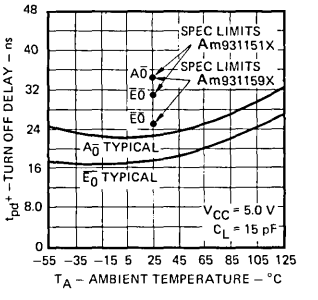
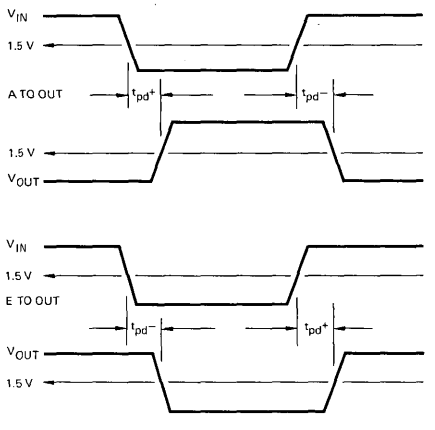


Figure 5

SWITCHING TIME TEST CIRCUIT & WAVEFORMS



PULSE GEN CHARACTERISTICS
Freq. ≈ 1 MHz
Pulse Width ≈ 100 ns
$t_r = t_f \leq 15$ ns
Amplitude ≈ 4 V
*Includes all probe and jig capacitance

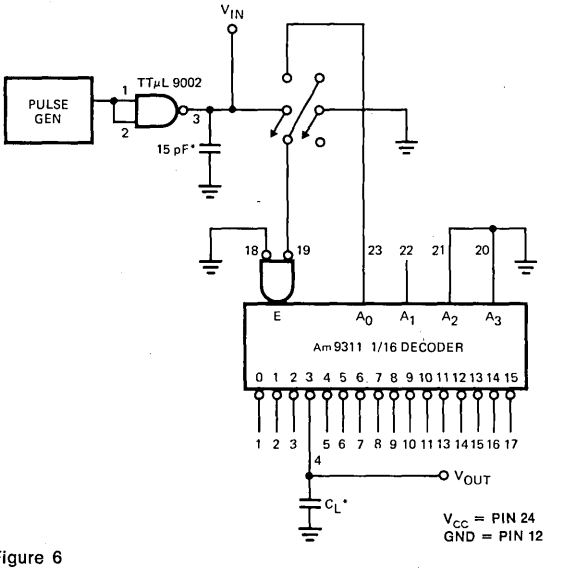


Figure 6

Am9311 LOADING RULES (in unit loads)

Input/Output	Pin No.'s	Input Unit Load	Fanout Output HIGH	Fanout Output LOW
$\overline{0}_{OUT}$	1	—	20	10
$\overline{1}_{OUT}$	2	—	20	10
$\overline{2}_{OUT}$	3	—	20	10
$\overline{3}_{OUT}$	4	—	20	10
$\overline{4}_{OUT}$	5	—	20	10
$\overline{5}_{OUT}$	6	—	20	10
$\overline{6}_{OUT}$	7	—	20	10
$\overline{7}_{OUT}$	8	—	20	10
$\overline{8}_{OUT}$	9	—	20	10
$\overline{9}_{OUT}$	10	—	20	10
$\overline{10}_{OUT}$	11	—	20	10
GND	12	—	—	—
$\overline{11}_{OUT}$	13	—	20	10
$\overline{12}_{OUT}$	14	—	20	10
$\overline{13}_{OUT}$	15	—	20	10
$\overline{14}_{OUT}$	16	—	20	10
$\overline{15}_{OUT}$	17	—	20	10
$\overline{E}_0$	18	1	—	—
$\overline{E}_1$	19	1	—	—
A_3	20	1	—	—
A_2	21	1	—	—
A_1	22	1	—	—
A_0	23	1	—	—
V_{CC}	24	—	—	—

Table I

TRUTH TABLE

INPUTS $\overline{E}_0$	$\overline{E}_1$	A_0	A_1	A_2	A_3	OUTPUTS $\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$	$\overline{10}$	$\overline{11}$	$\overline{12}$	$\overline{13}$	$\overline{14}$	$\overline{15}$
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Table II

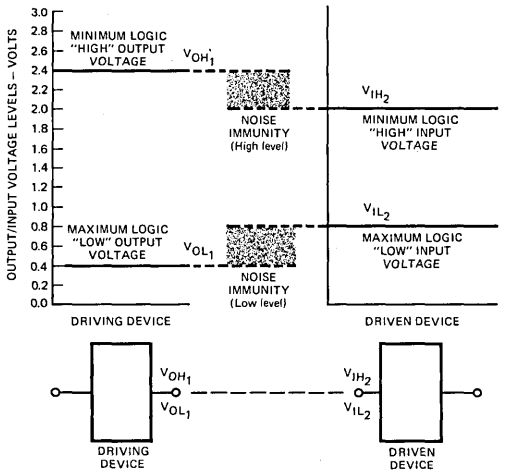
MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

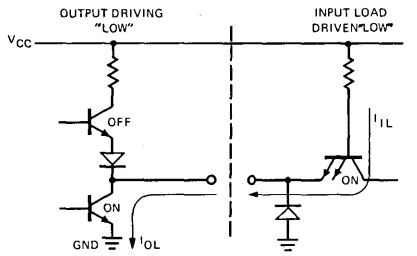
Table III

INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH



Current Interface Conditions — LOW



Current Interface Conditions — HIGH

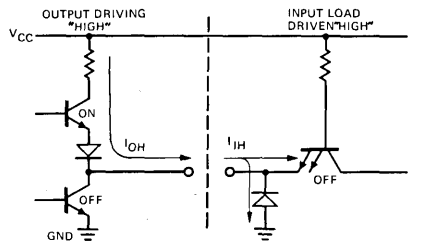
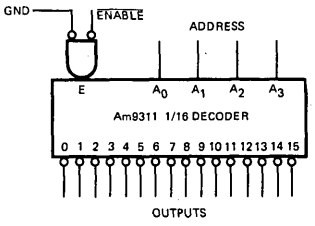


Figure 7

Am9311 APPLICATIONS

Decode any 4 bit BCD code

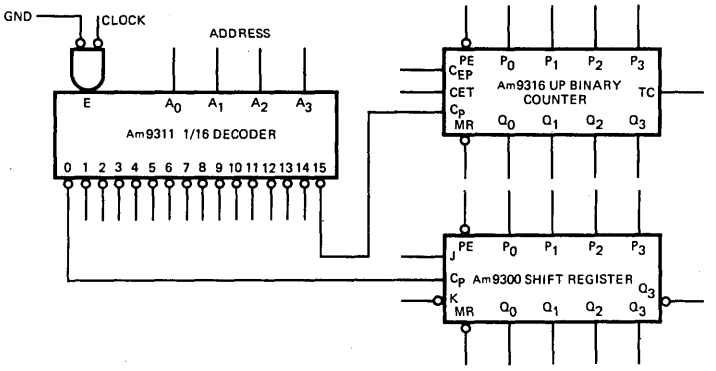


Decode any BCD code using a 9311 element. Any 4 bit BCD code may be decoded by selecting outputs, examples are shown in the table.

Figure 8

DECIMAL DIGIT	OUTPUT SELECTION: BCD CODE 8421	5421	EXCESS 3	GRAY
0	0	0	3	0
1	1	1	4	1
2	2	2	5	3
3	3	3	6	2
4	4	4	7	6
5	5	8	8	7
6	6	9	9	5
7	7	10	10	4
8	8	11	11	12
9	9	12	12	13

Clock Demultiplexing



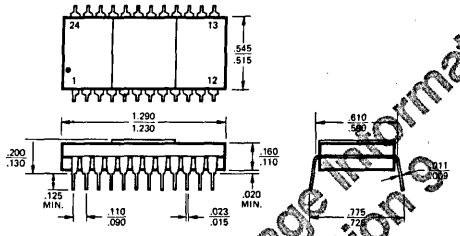
The Am9311 can be used as a clock demultiplexer. The binary address designates to which register or counter the clock is sent. Up to 5 register counter stages can be driven by one decoder output allowing word lengths of 20 bits to be controlled. Any sequential circuit in the 9300 MSI family can be used in this configuration.

Figure 9

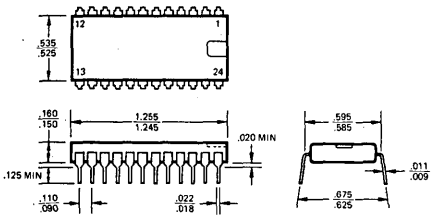
PHYSICAL DIMENSIONS

Dual-In-Line

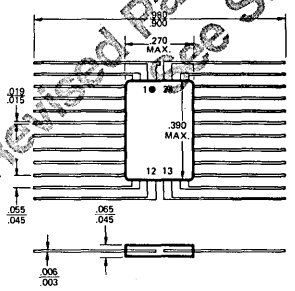
Hermetic



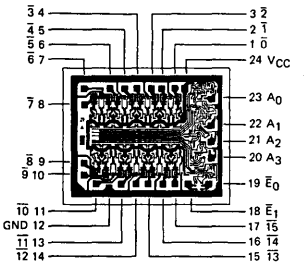
Molded



Flat Package



Metallization and Pad Layout



95 x 77 Mils

ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am93L11
Low-Power One-of-Sixteen Decoder

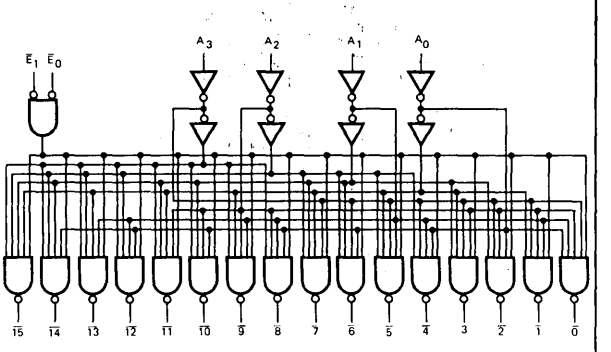
Distinctive Characteristics:

- 58 mw typical power dissipation.
- 50 ns typical propagation delay.
- 100% reliability assurance testing in compliance with MIL STD 883.
- Compatible with 7400 and 9300 series devices

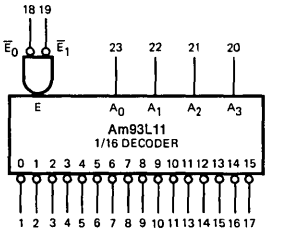
FUNCTIONAL DESCRIPTION

The AM93L11 one-of-sixteen decoder/demultiplexer accepts a four-bit code on the four address inputs A_0, A_1, A_2, A_3 and turns on a corresponding active LOW output. The outputs are designated by the decimal equivalent of the binary code which selects them. All non-selected outputs will be HIGH. The device is enabled by LOW levels on both enable pins $\overline{E}_0$ and $\overline{E}_1$. If either enable is HIGH, then all outputs will be HIGH. Data can be demultiplexed by applying an address to the address inputs and a data stream to one of the enable inputs, with the other enable held LOW. The output corresponding to the address will then follow the input data.

LOGIC DIAGRAM



LOGIC SYMBOL



V_{CC} = PIN 24
GND = PIN 12

LOADING RULES

In Unit Loads (Notes)

Input Load Factor	TTL loads HIGH	TTL loads LOW	93L loads HIGH	93L loads LOW
All Inputs	0.5	0.25	1.0	1.0
Output Drive	HIGH	LOW	HIGH	LOW
All Outputs	10.0	3.0	20.0	12.0

NOTES:
1) A TTL unit load is specified as 0.4 V at −1.6 mA LOW, 2.4 V at 40 μA HIGH.
2) A 93L unit load is specified as 0.3 V at −400 μA LOW, 2.4 V at 20 μA HIGH.
3) Enough output LOW current is available to mix TTL and 93L loads and still meet the 93L requirement of a V_{OL} of 0.3 V.

Am93L11 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
24-Pin Molded DIP	0°C to +75°C	Am93L1159C
24-Pin Hermetic DIP	0°C to +75°C	U6N93L1159X
24-Pin Hermetic DIP	−55°C to +125°C	U6N93L1151X
24-Pin Hermetic Flat Pak	−55°C to +125°C	U4M93L1159X
Dice	Note	UXX93L11XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current (Note 1)	−30 mA to +5.0 mA

Note 1. Maximum current defined by DC input voltage.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93L1159X T_A = 0°C to +75°C V_{CC} = 4.75 V to 5.25 V
Am93L1151X T_A = −55°C to +125°C V_{CC} = 4.50 V to 5.50 V

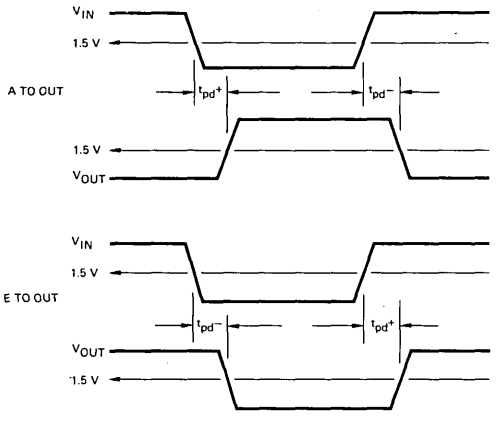
Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 4.92 mA V_{IN} = V_{IH} or V_{IL}		0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.7	Volts
I_{IL} (Note 2)	93L Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.3 V		−0.25	−0.4	mA
I_{IH} (Note 2)	93L Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V		2.0	20	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V	−2.5	−16	−25	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		11.5	16.5	mA

Notes: 1) Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by the 93L input load factor. (See loading rules)

SWITCHING CHARACTERISTICS (T_A = 25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{pd+} ($A\overline{O}$)	Address to Output HIGH	V_{CC} = 5.0 V C_L = 15pF	22	44	70	ns
t_{pd-} ($A\overline{O}$)	Address to Output LOW		25	50	75	ns
t_{pd+} ($\overline{EO}$)	Enable to Output HIGH		20	40	60	ns
t_{pd-} ($\overline{EO}$)	Enable to Output LOW		20	40	60	ns

SWITCHING TIME WAVEFORMS



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Am9312
Eight-Input Multiplexer

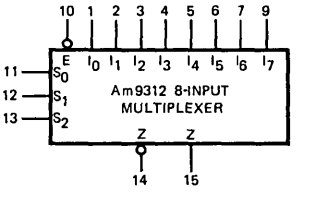
Distinctive Characteristics:

- 10 ns typical propagation delay
- Both true and complement outputs provided
- 100% reliability assurance testing in compliance with MIL-STD-883
- Can be used to generate any function of four variables

FUNCTIONAL DESCRIPTION

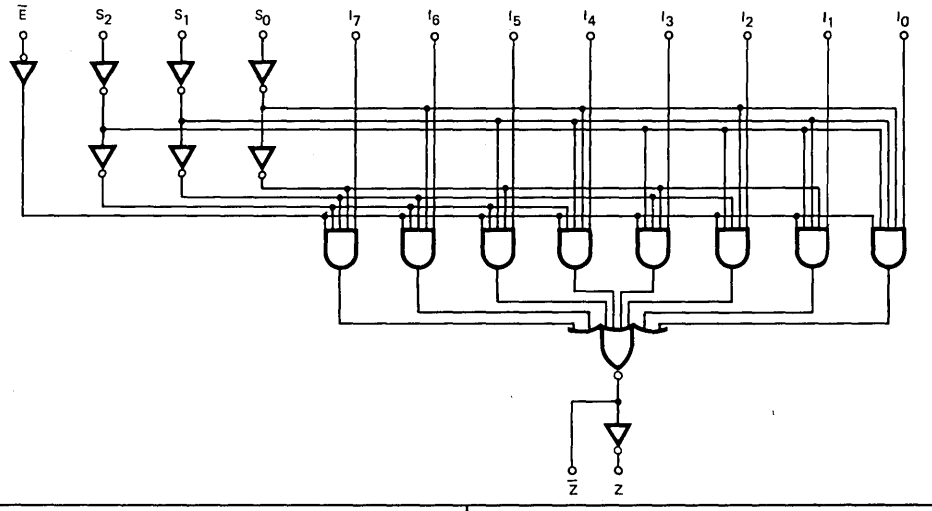
The Am9312 is a high-speed eight-input multiplexer or data selector. A three-bit select code, S_0 S_1 S_2, determines which one of the eight inputs, I_0 through I_7, will be routed through to the outputs. Both true and complement outputs are available; the complement output is slightly faster. An active LOW enable ($\overline{E}$) is provided. When the enable is HIGH, the two outputs go to their inactive levels, with the Z output LOW and the $\overline{Z}$ output HIGH. The device can also be used to generate any logic function of four variables.

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

LOGIC DIAGRAM

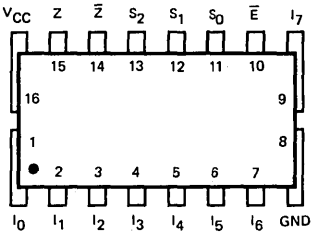


Am9312 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
16-pin Molded DIP	0°C to +75°C	U6M931259X
16-pin Hermetic DIP	0°C to +75°C	U7B931259X
16-pin Hermetic DIP	−55°C to +125°C	U7B931251X
16-pin Hermetic Flat Pak	−55°C to +125°C	U4L931251X
Dice	Note	UXX9312XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125° temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to + 125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am931259X T_A = 0°C to +75°C V_{CC} = 5.0 V ±5%
Am931251X T_A = −55°C to +125°C V_{CC} = 5.0 V ±10%

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.8 mA V_{IN} = V_{IH} or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16.0 mA V_{IN} = V_{IH} or V_{IL}		0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V		−1.0	−1.6	mA
I_{IH}	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V		6.0	40	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V	−35		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		27	44	mA

Notes: 1) Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.

SWITCHING CHARACTERISTICS (T_A = 25°C)

(V_{CC} = 5.0 V, C_L = 15 pF (Refer to table for test conditions)

		Min	Typ	Max	Units
t_{pd}+(ST)	Turn Off Delay—Select Input to TRUE Output	12	23	34	ns
t_{pd}−(ST)	Turn On Delay—Select Input to TRUE Output	13	25	34	ns
t_{pd}+(SF)	Turn Off Delay—Select Input to FALSE Output	9	18	24	ns
t_{pd}−(SF)	Turn On Delay—Select Input to FALSE Output	9	18	26	ns
t_{pd}+(DT)	Turn Off Delay—Data Input to TRUE Output	9	16	24	ns
t_{pd}−(DT)	Turn On Delay—Data Input to TRUE Output	9	16	24	ns
t_{pd+}(DF)	Turn Off Delay—Data Input to FALSE Output	3	9	14	ns
t_{pd}−(DF)	Turn On Delay—Data Input to FALSE Output	4	10	16	ns
t_{pd}+($\overline{ET}$)	Turn Off Delay—Enable Input to TRUE Output	11	23	30	ns
t_{pd}−($\overline{ET}$)	Turn On Delay—Enable Input to TRUE Output	10	22	31	ns
t_{pd}+($\overline{EF}$)	Turn Off Delay—Enable Input to FALSE Output	6	14	20	ns
t_{pd}−($\overline{EF}$)	Turn On Delay—Enable Input to FALSE Output	6	16	23	ns

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH-signal level or when used with V_{CC} to indicate HIGH V_{CC} value.
I Input.
L LOW, applying to a LOW signal level or when used with V_{CC} to indicate LOW V_{CC} value.
O Output.

FUNCTIONAL TERMS:

Enable Input ($\overline{E}$) Is active LOW to enable data selection from one of eight data inputs. Enable Input HIGH inhibits all data source selection. Refer to Truth Table.
Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.
I_j Data Inputs designates one of the eight multiplexer data inputs $j = 0, 7$.
Unit load One T^2L gate input load. In the HIGH state it is equal to $40\mu A$ at 2.4V and in the LOW state it is equal to $-1.6mA$ at 0.4V.
Z Output The logic TRUE output of the multiplexer.
$\overline{Z}$ Output The complement of the Z output.

OPERATIONAL TERMS:

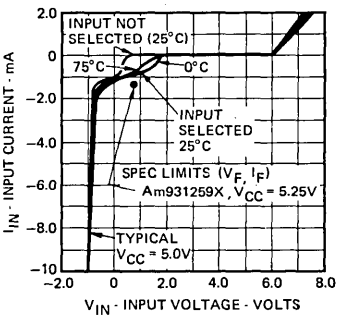
I_{OH} Output HIGH current, forced out of output in V_{OH} test.
I_{OL} Output LOW current, forced into the output in V_{OL} test.
I_{CC} The current drawn by the device under a +5.0 V power supply bias with input and output terminals open.
Negative Current Current flowing out of the device.
Positive Current Current flowing into the device.
V_{IH} Minimum logic HIGH input voltage.
V_{IL} Maximum logic LOW input voltage.
V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.
V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

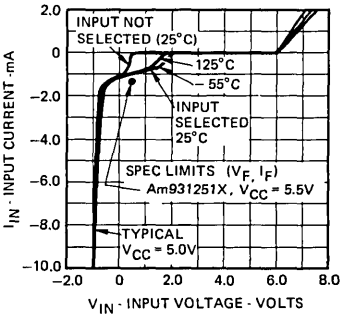
SWITCHING TERMS: (All switching times are measured at the 1.5 V logic level).

t_{pd+}(ST) The propagation delay from a Select Input signal transition to the corresponding TRUE output LOW-HIGH transition.
t_{pd-}(ST) The propagation delay from a Select Input signal transition to the corresponding TRUE output HIGH-LOW transition.
t_{pd+}(SF) The propagation delay from a Select Input signal transition to the corresponding FALSE output LOW-HIGH transition.
t_{pd-}(SF) The propagation delay from a Select Input signal transition to the corresponding FALSE output HIGH-LOW transition.
t_{pd+}(DT) The propagation delay from a Data Input signal transition to the TRUE output LOW-HIGH transition.
t_{pd-}(DT) The propagation delay from a Data Input signal transition to the TRUE output HIGH-LOW transition.
t_{pd+}(DF) The propagation delay from a Data Input signal transition to the FALSE output LOW-HIGH transition.
t_{pd-}(DF) The propagation delay from a Data Input signal transition to the FALSE output HIGH-LOW transition.
t_{pd+}($\overline{E}$T) The propagation delay from an Enable Input signal transition to the TRUE output LOW-HIGH transition.
t_{pd-}($\overline{E}$T) The propagation delay from an Enable Input signal transition to the TRUE output HIGH-LOW transition.
t_{pd+}($\overline{E}$F) The propagation delay from an Enable Input signal transition to the FALSE output LOW-HIGH transition.
t_{pd-}($\overline{E}$F) The propagation delay from an Enable Input signal transition to the FALSE output HIGH-LOW transition.

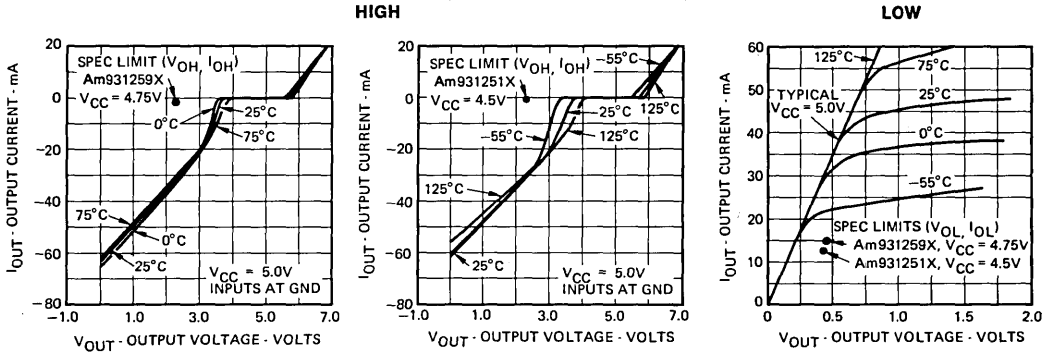
PERFORMANCE CURVES

Input Characteristics





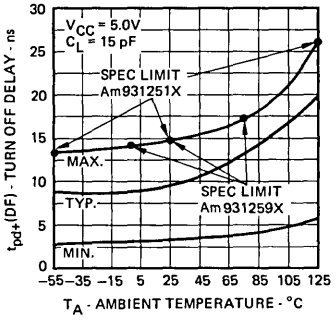
Output Characteristics



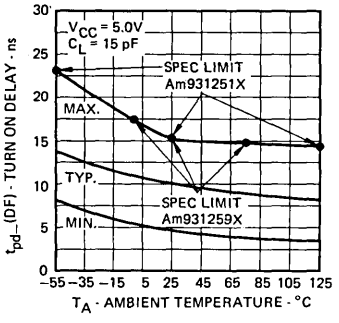
PERFORMANCE CURVES

Switching Characteristics

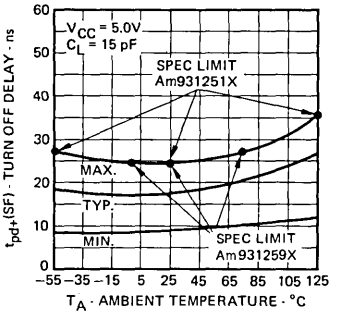
Turn Off Delay
Data Input to FALSE Output



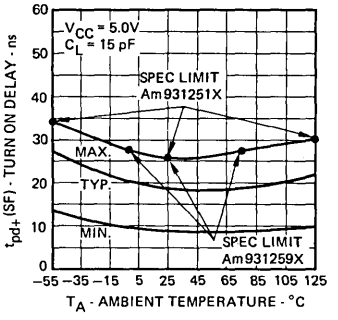
Turn On Delay
Data Input to FALSE Output



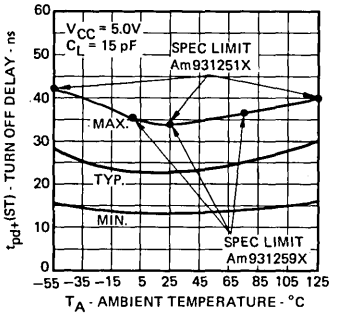
Turn Off Delay
Select Input to FALSE Output



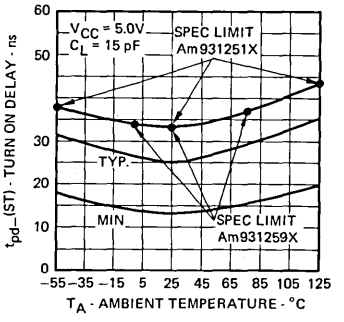
Turn On Delay
Select Input to FALSE Output



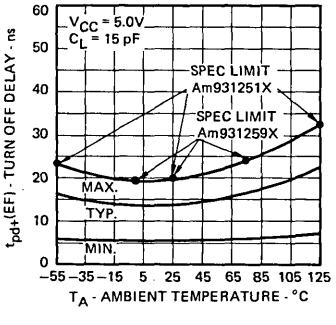
Turn Off Delay
Select Input to TRUE Output



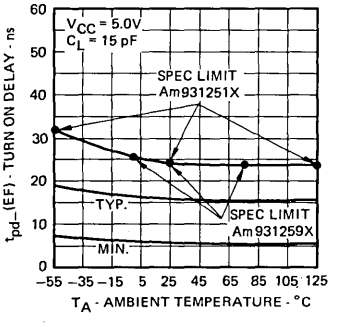
Turn On Delay
Select Input to TRUE Output



Turn Off Delay
Enable Input to FALSE Output



Turn On Delay
Enable Input to FALSE Output



MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 54/7400	1	1
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

TRUTH TABLE

Inputs												Outputs	
$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$(F)	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

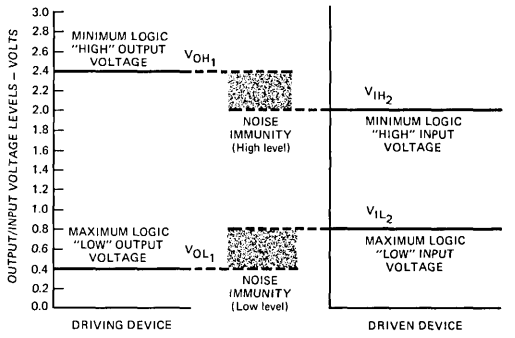
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't care

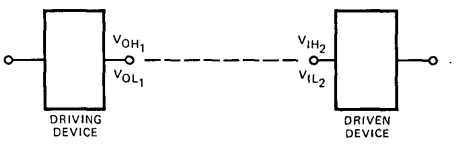
Am9312 LOADING RULES

Input/Output	Pin No.s	Input Unit Load	Fanout Output HIGH	Fanout Output LOW
I_0	1	1	—	—
I_1	2	1	—	—
I_2	3	1	—	—
I_3	4	1	—	—
I_4	5	1	—	—
I_5	6	1	—	—
I_6	7	1	—	—
GND	8	—	—	—
I_7	9	1	—	—
$\overline{E}$	10	1	—	—
S_0	11	1	—	—
S_1	12	1	—	—
S_2	13	1	—	—
$\overline{Z}$	14	—	20	10
Z	15	—	20	10
V_{CC}	16	—	—	—

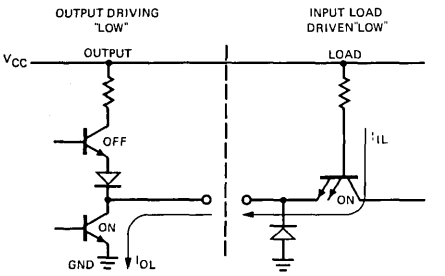
INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH

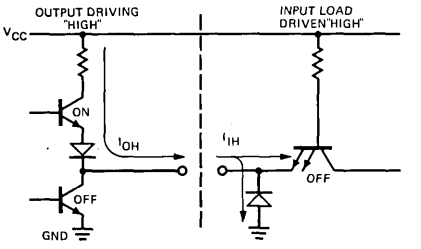




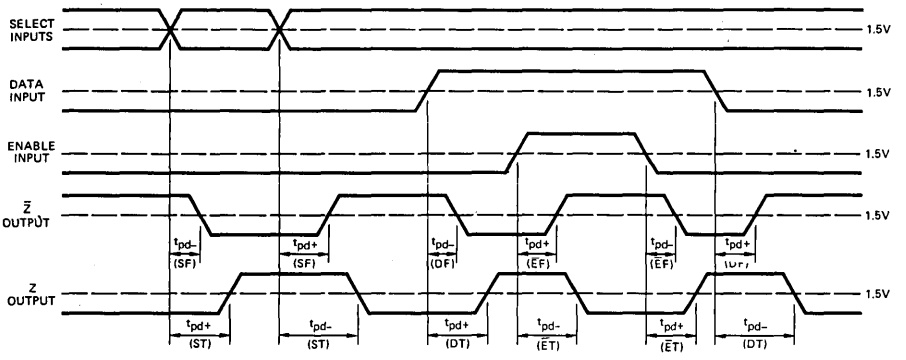
Current Interface Conditions — LOW



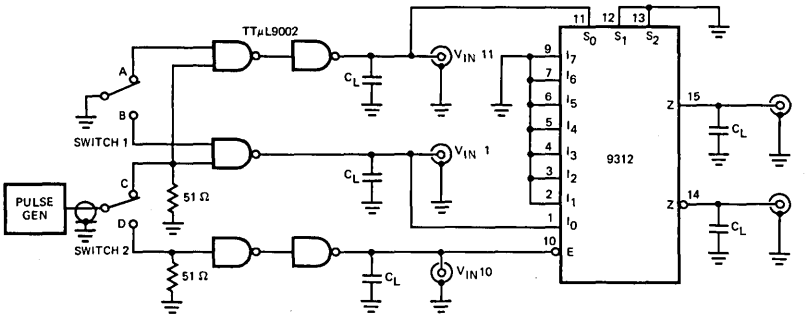
Current Interface Conditions — HIGH



SWITCHING TIME WAVEFORMS



SWITCHING TIME TEST CIRCUIT

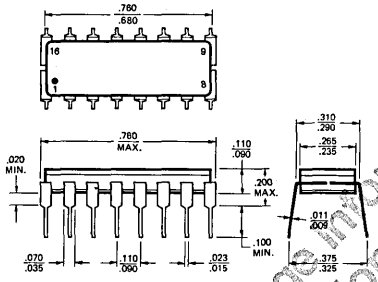


Switching Measurement Connection Table

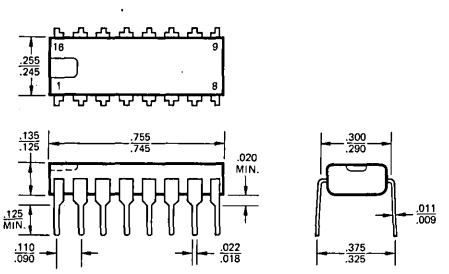
	$t_{pd}\pm$(DT) $t_{pd}\pm$(DF)	$t_{pd}\pm$(ST) $t_{pd}\pm$(SF)	$t_{pd}\pm(\overline{ET})$ $t_{pd}\pm(\overline{EF})$
Switch 1	A	B	B
Switch 2	C	C	D

PHYSICAL DIMENSIONS
Dual-In-Line

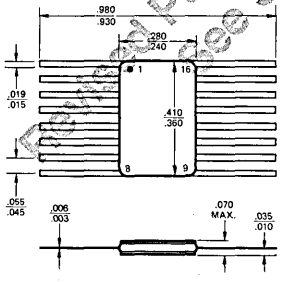
Hermetic



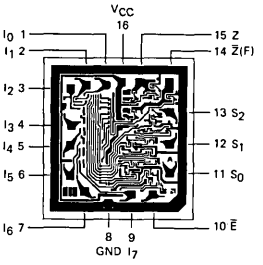
Molded



Flat Package



Metallization and Pad Layout



68 x 73 Mils

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TELEX: 34-6306

Am93L12
Low-Power Eight-Input Multiplexer

Distinctive Characteristics

- 45 mw typical power dissipation.
- 30 ns typical propagation delay.
- 100% reliability assurance testing in compliance with MIL STD 883
- Fan-out to three standard TTL loads.

FUNCTIONAL DESCRIPTION

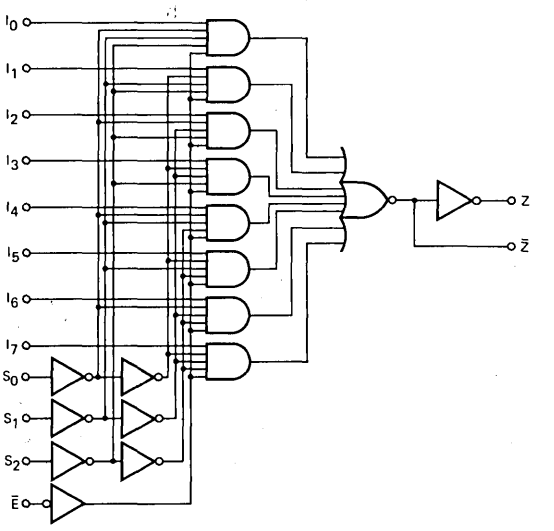
The Am93L12 is a low-power eight-input multiplexer or data selector. A three-bit select code, S_0 S_1 S_2, determines which one of the eight inputs, I_0 through I_7, will be routed through to the outputs. Both true and complement outputs are available; the complement output is slightly faster. An active LOW enable ($\overline{E}$) is provided. When the enable is HIGH, the two outputs go to their inactive levels, with the Z output LOW and the $\overline{Z}$ output HIGH. The device can also be used to generate any logic function of four variables.

OPERATION TABLE

$\overline{E}$	S_0	S_1	S_2	Z	$\overline{Z}$
H	X	X	X	L	H
L	L	L	L	I_0	$\overline{I}_0$
L	H	L	L	I_1	$\overline{I}_1$
L	L	H	L	I_2	$\overline{I}_2$
L	H	H	L	I_3	$\overline{I}_3$
L	L	L	H	I_4	$\overline{I}_4$
L	H	L	H	I_5	$\overline{I}_5$
L	L	H	H	I_6	$\overline{I}_6$
L	H	H	H	I_7	$\overline{I}_7$

H = HIGH voltage level
L = LOW voltage level
X = Don't Care

LOGIC DIAGRAM



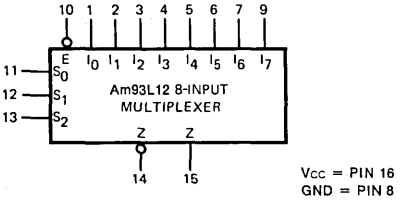
LOADING RULES

In Unit Loads (Notes)

Input Loading	TTL loads HIGH	TTL loads LOW	93L loads HIGH	93L loads LOW
All Inputs	0.5	0.25	1.0	1.0
Output Drive	HIGH	LOW	HIGH	LOW
All Outputs	10	3	20	12

NOTES:
1) A TTL unit load is specified as 0.4 V at −1.6 mA LOW, 2.4 V at 40 μA HIGH.
2) A 93L unit load is specified as 0.3 V at −400 μA LOW, 2.4 V at 20 μA HIGH.
3) Enough output LOW current is available to mix TTL and 93L loads and still meet the 93L requirement of a V_{OL} of 0.3 V.

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

Am93L12 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
16-Pin Molded DIP	0°C to +75°C	U6M93L1259X
16-Pin Hermetic DIP	0°C to +75°C	U7B93L1259X
16-Pin Hermetic DIP	−55°C to +125°C	U7B93L1251X
16-Pin Hermetic Flat Pak	−55°C to +125°C	U4L93L1251X
Dice	Note	UXX93L12XXD

Note : The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125° temperature ranges.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current (Note 1)	−30 mA to +5.0 mA

Note 1. Maximum current defined by DC input voltage.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93L1259X T_A = 0°C to +75°C V_{CC} = 4.75 V to 5.25 V
Am93L1251X T_A = −55°C to +125°C V_{CC} = 4.50 V to 5.50 V

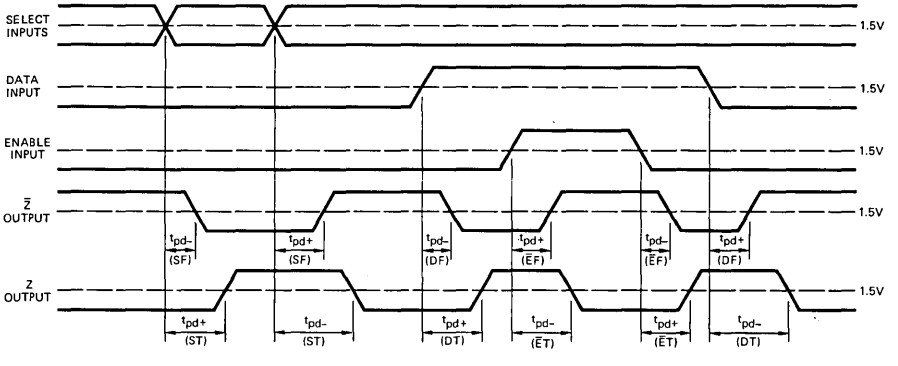
Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 4.92 mA V_{IN} = V_{IH} or V_{IL}		0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.7	Volts
I_{IL} (Note 2)	93L Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.3 V		−0.25	−0.4	mA
I_{IH} (Note 2)	93L Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V		2.0	20	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V	−10	−22	−40	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		9.0	13.3	mA

Notes: 1) Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by the 93L input load factor. (See loading rules)

SWITCHING CHARACTERISTICS (T_A = 25°C) (V_{CC} = 5.0 V, C_L = 15 pF)

Parameters	Description	Min	Typ	Max	Units
t_{pd}+(ST)	Turn Off Delay—Select Input to TRUE Output HIGH	26	53	105	ns
t_{pd}−(ST)	Turn On Delay—Select Input to TRUE Output LOW	28	56	110	ns
t_{pd}+(SF)	Turn Off Delay—Select Input to FALSE Output HIGH	23	45	100	ns
t_{pd}−(SF)	Turn On Delay—Select Input to FALSE Output LOW	23	45	90	ns
t_{pd}+(DT)	Turn Off Delay—Data Input to TRUE Output HIGH	20	40	90	ns
t_{pd}−(DT)	Turn On Delay—Data Input to TRUE Output LOW	18	36	80	ns
t_{pd+}(DF)	Turn Off Delay—Data Input to FALSE Output HIGH	11	22	55	ns
t_{pd}−(DF)	Turn On Delay—Data Input to FALSE Output LOW	16	31	70	ns
t_{pd}+(ET)	Turn Off Delay—Enable Input to TRUE Output HIGH	24	47	100	ns
t_{pd}−(ET)	Turn On Delay—Enable Input to TRUE Output LOW	23	45	100	ns
t_{pd}+(EF)	Turn Off Delay—Enable Input to FALSE Output HIGH	18	36	90	ns
t_{pd}−(EF)	Turn On Delay—Enable Input to FALSE Output LOW	19	38	80	ns

SWITCHING TIME WAVEFORMS



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Am9314
Four-Bit Latch

Distinctive Characteristics

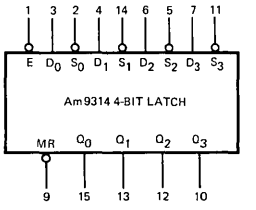
- Each latch can be used as single line "D" latch
- Each latch can be used as Set/Reset latch with reset override
- Overriding common master reset
- 100% reliability assurance testing in compliance with MIL STD 883
- Electrically tested and optically inspected die for the assemblers of hybrid products
- Mixing privileges for obtaining price discounts. Refer to price list
- Available in highly reliable molded epoxy, hermetic dual-in-line or hermetic flat package.

FUNCTIONAL DESCRIPTION

The 9314 is a four-bit latch with a common active LOW enable and overriding active LOW master reset. Each of the four latches can be used as a single line "D" latch by tying the appropriate $\overline{S}$ input LOW, or as an active LOW Set/Reset latch with Reset override with the D input as the reset input and the $\overline{S}$ input as the set input.

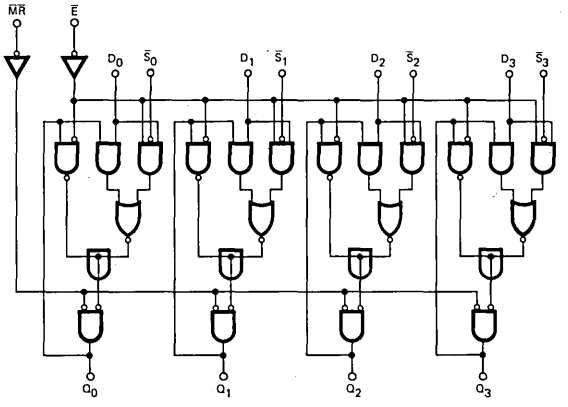
Data is transferred into the latch when the enable goes LOW and the latch stores the information when the enable goes HIGH. With the enable HIGH the latch is no longer affected by the $\overline{S}$ and D inputs. When the Master Reset goes LOW all latches are reset independent of all other input conditions.

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

LOGIC DIAGRAM

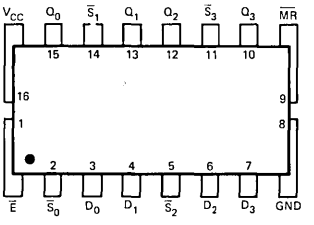


Am9314 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	U6M931459X
Hermetic DIP	0°C to +75°C	U7B931459X
Hermetic DIP	−55°C to +125°C	U7B931451X
Hermetic Flat Pak	−55°C to +125°C	U4L931451X
Dice	Note	UXX9314XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current	Note 1

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am931459X $T_A = 0°C$ to $+75°C$ $V_{CC} = 5.0\ V \pm 5\%$
Am931451X $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0\ V \pm 10\%$

Parameters	Description	Test Conditions	Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -0.8$ mA $V_{IN} = V_{IH}$ or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $I_{OL} = 16.0$ mA $V_{IN} = V_{IH}$ or V_{IL}		0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	$V_{CC} = MAX.$, $V_{IN} = 0.4$ V		−1.0	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	$V_{CC} = MAX.$, $V_{IN} = 2.4$ V		6.0	40	μA
	Input HIGH Current	$V_{CC} = MAX.$, $V_{IN} = 5.5$ V			1.0	mA
I_{SC}	Output Short Circuit Current	$V_{CC} = MAX.$, $V_{OUT} = 0.0$ V	−30		−100	mA
I_{CC}	Power Supply Current	$V_{CC} = MAX.$		35	55	mA

Notes: 1) Typical Limits are at $V_{CC} = 5.0$ V, 25°C Ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by input load factor (See Loading Rules).

SWITCHING CHARACTERISTICS ($T_A = 25°C$) ($V_{CC} = 5.0$ V, $C_L = 15$ pF)

Parameters	Description		Min	Typ	Max	Units
$t_{pd+}(\overline{E})$	Turn Off Delay Enable to Output	See Fig. 13	8	19	25	ns
$t_{pd-}(\overline{E})$	Turn On Delay Enable to Output		7	14	22	ns
$t_{pd+}(D)$	Turn Off Delay Data to Output	See Fig. 13	5	10	16	ns
$t_{pd-}(D)$	Turn On Delay Data to Output		7	14	22	ns
$t_{sL}(\overline{DE})$	Set Up Time LOW Data to Enable	See Fig. 14	0	10	16	ns
$t_{sH}(\overline{DE})$	Set Up Time HIGH Data to Enable		−5	−1	5	ns
$t_{pw}(\overline{E})$	Minimum Enable Pulse Width			11	18	ns
$t_{pw}(\overline{MR})$	Minimum Master Reset Pulse Width			13	18	ns
$t_{pd-}(\overline{MR})$	Turn On Delay Master Reset to Output		7	14	20	ns
$t_{rec}(\overline{MR})$	Master Reset Recovery Time			−4	0	ns
$t_{pd+}(\overline{S})$	Turn Off Delay $\overline{Set}$ Input to Output			13	22	ns
$t_s(D\overline{S})$	Set Up Time HIGH Data to $\overline{Set}$ Input	See Fig. 15	−6	1	8	ns

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS:

$\overline{E}$ Active LOW Common Enable. When this input goes HIGH information present in the four latches is stored.

D_i Active HIGH Data Inputs. Can also be used as active LOW Reset Input in Set/Reset Mode. i = 0-3.

$\overline{S}_i$ Active LOW Set Inputs. This input is held LOW for "D" operation. i = 0-3.

Fan Out The logic HIGH or LOW output drive capability in terms of input unit loads.

Input Unit Load One T^2L gate input load. In the HIGH state it is equal to 40μA at 2.4V and in the LOW state it is equal to 1.6mA at 0.4V.

Latch A storage element which stores one bit of data on receipt of a single transition on an Enable signal.

$\overline{MR}$ Input The master reset input.

Q_0, Q_1, Q_2, Q_3 Outputs The four outputs of the 9314 latch

Q (t_n) The output of a latch at time t_n.

Q (t_{n+1}) The output of a latch at time t_{n+1} when input conditions at time t_n have been realized by the output.

OPERATIONAL TERMS:

I_{IL} Forward input load current, for unit input load.

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{CC} The current drawn by the device under a +5.0 V power supply bias with input and output terminals open.

I_{IH} Reverse input load current with V_{OH} applied to input.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage. Refer to figure 13.

V_{IL} Maximum logic LOW input voltage. Refer to figure 13.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

SWITCHING TERMS

t_{pd+} **(D)** The propagation delay from the D input LOW to HIGH transition to the Q output LOW to HIGH transition. Refer to Figure 13.

t_{pd-} **(D)** The propagation delay from the D input HIGH to LOW transition to the Q output HIGH to LOW transition. Refer to Figure 13

t_s "L" **($\overline{DE}$)** The minimum time required for a LOW logic level to be present at a data input prior to the Enable transition from LOW to HIGH in order for the latch to retain a LOW logic level.

t_s "H" **($\overline{DE}$)** The minimum time required for a HIGH logic level to be present and remain present at a data input prior to the Enable transition from LOW to HIGH in order for the latch to retain a HIGH logic level. Refer to Figure 14.

t_s **($\overline{DS}$)** The time required for a HIGH logic level to be present at the D input prior to the Set input transition from LOW to HIGH in order for the latch to respond to the HIGH D input. Refer to Fig. 15.

This parameter indicates how long a set signal must remain after the over-riding reset signal is removed for the latch to respond to the set.

t_{pd+} **($\overline{E}$)** The propagation delay from the Enable input HIGH to LOW transition to the Q output LOW to HIGH transition. Refer to Figure 5.

t_{pd-} **($\overline{E}$)** The propagation delay from the Enable input HIGH to LOW transition to the Q output HIGH to LOW transition. Refer to Figure 5.

t_{pw} **($\overline{E}$)** The minimum time the Enable input must be LOW in order for data to be correctly entered into the latches. Refer to Figure 12.

t_{pd-} **($\overline{MR}$)** The propagation delay from the Master Reset input HIGH to LOW transition to the Q output HIGH to LOW transition. Refer to Figure 10.

t_{pw} **(MR)** The minimum time the Master Reset input must be LOW in order for the latches to be reset. Refer to Figure 10.

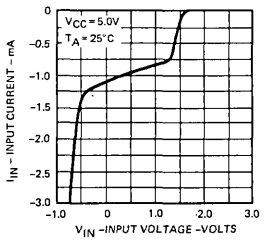
t_{rec} **($\overline{MR}$)** The time required between the Master Reset input LOW to HIGH transition and the Enable input LOW to HIGH transition in order for the latches to respond to new data. Refer to Figure 11.

t_{pd+} **($\overline{S}$)** The propagation delay from the HIGH to LOW Set input transition to the Q output LOW to HIGH transition. Refer to Fig. 9.

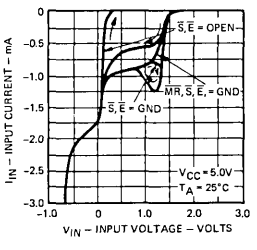
Typical Input/Output Characteristics

Input Current Versus Input Voltage

$\overline{MR}$, $\overline{E}$, $\overline{S}$ Figure 1

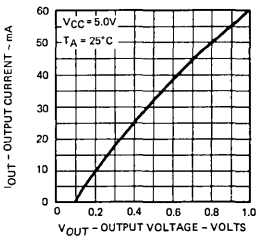


D Figure 2

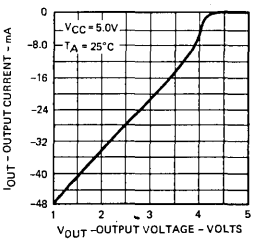


Output Current Versus Output Voltage

Low State Figure 3



High State Figure 4

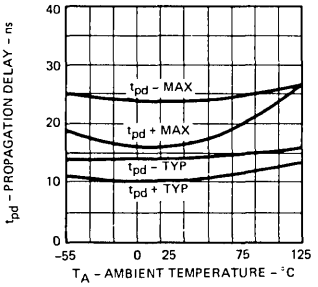


Switching Characteristics

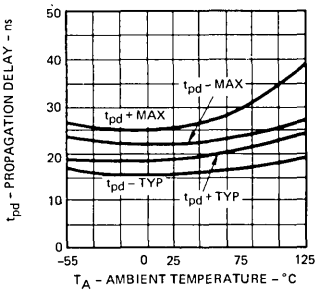
The active input is driven by a 9002 TTμL or equivalent gate with the output loaded with 15 pF (includes jig and probe). Outputs under test are loaded with 15 pF (includes jig and probe). Pins not reference are not connected.

The TYP curves are for both 51X and 59X grade devices. The MAX, MIN curves are for 51X grade devices only. The MAX, MIN curves for 59X grade are offset from the 51X grade curves by the parameter difference at 25°C.

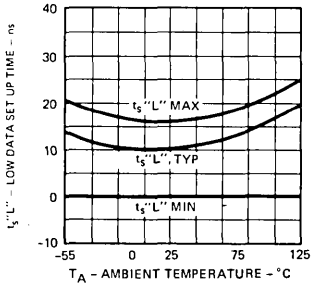
Enable Input to Output Figure 5



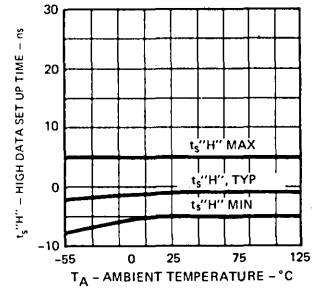
Data Input to Output Figure 6



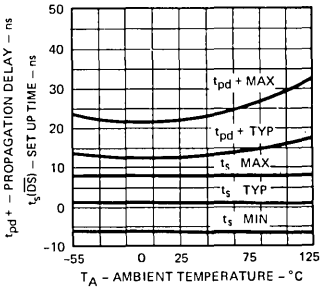
Data Input to Enable Input Figure 7



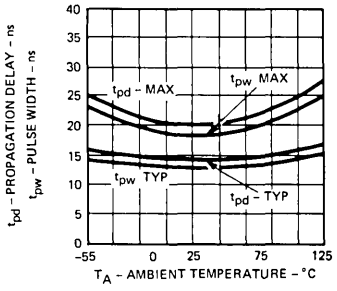
Data Input to Enable Input Figure 8



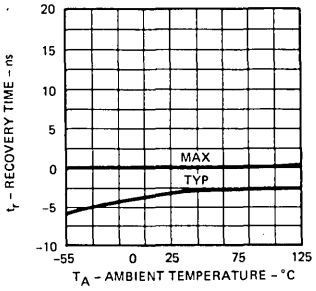
Set Input to Output
Set Input to Data Input Figure 9



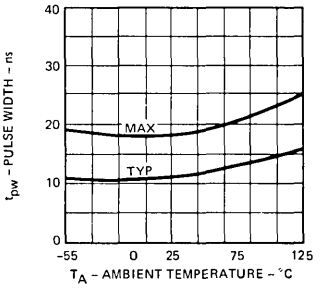
Master Reset Input Pulse Width
Master Reset Input to Output Figure 10



Master Reset Recovery Time Figure 11

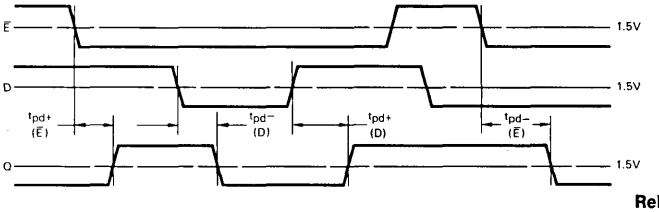


Enable Input Pulse Width Figure 12

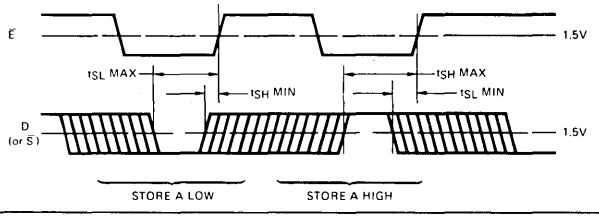


SWITCHING TIME WAVEFORMS

Switching Delays Figure 13



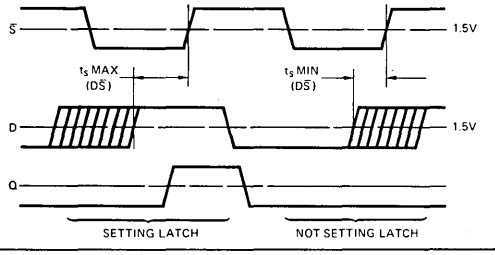
Input Timing Figure 14



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN

Release of D input to set latch with $\overline{S}$ input Figure 15



TRUTH TABLE

$\overline{MR}$	$\overline{E}$	D	$\overline{S}$	$Q_{(tn+1)}$	Operation
L	X	X	X	L	Reset
H	L	L	L	L	D Mode
H	L	H	L	H	
H	H	X	X	$Q_{(tn)}$	
H	L	L	L	L	R/S Mode
H	L	H	L	H	
H	L	L	H	L	
H	L	H	H	$Q_{(tn)}$	
H	H	X	X	$Q_{(tn)}$	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

TABLE I

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 54/7400	1	1
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

TABLE III

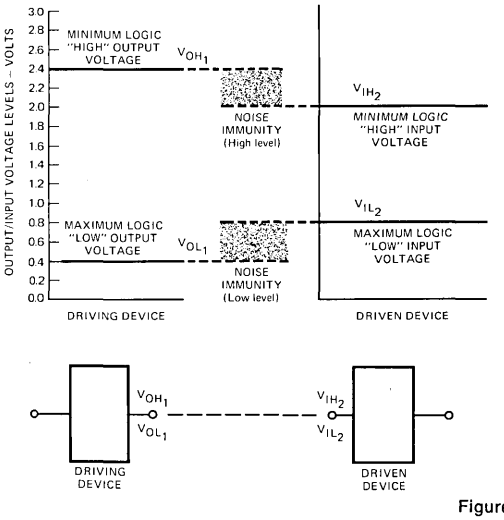
Am9314 LOADING RULES (in unit loads)

Input/Output	Pin No.'s	Input Unit Load	Output Drive Output HIGH	Output LOW
$\overline{E}$	1	1	—	—
$\overline{S}_0$	2	1	—	—
D_0	3	1.5	—	—
D_1	4	1.5	—	—
$\overline{S}_2$	5	1	—	—
D_2	6	1.5	—	—
D_3	7	1.5	—	—
GND	8	—	—	—
$\overline{MR}$	9	1	—	—
Q_3	10	—	20	10
$\overline{S}_3$	11	1	—	—
Q_2	12	—	20	10
Q_1	13	—	20	10
$\overline{S}_1$	14	1	—	—
Q_0	15	—	20	10
V_{CC}	16	—	—	—

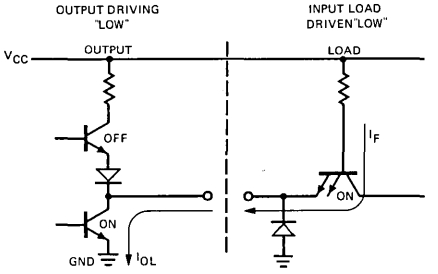
TABLE II

INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH



Current Interface Conditions — LOW



Current Interface Conditions — HIGH

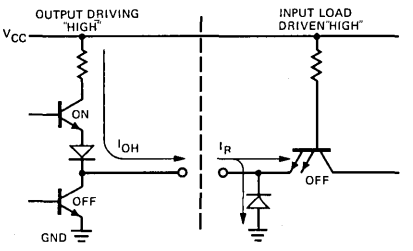
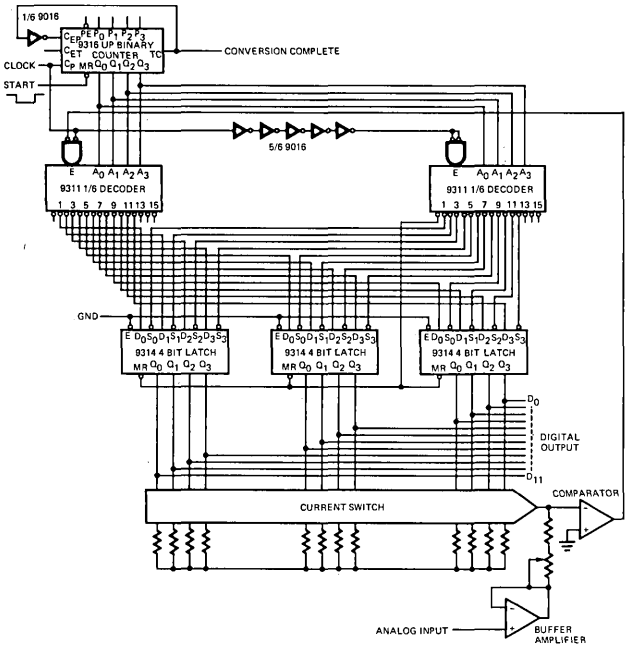


Figure 13

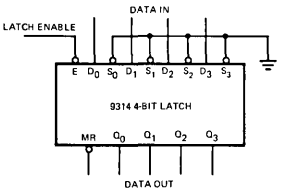
Am9314 APPLICATIONS



ANALOG TO DIGITAL CONVERSION

The figure illustrates a 12 bit high speed successive approximation A/D Converter using the 9314 Quad Latch.

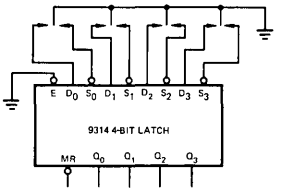
Figure 14



4-BIT STORAGE LATCH

The figure illustrates the use of the 9314 as a D type Storage Latch. Data is stored in the Latch when the enable line goes HIGH.

Figure 15

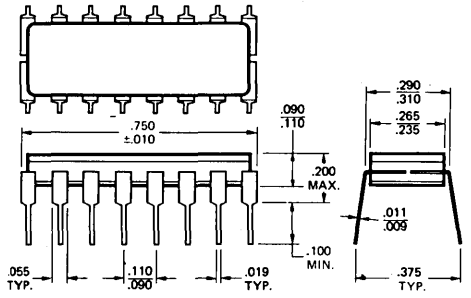


CONTACT BOUNCE ELIMINATOR

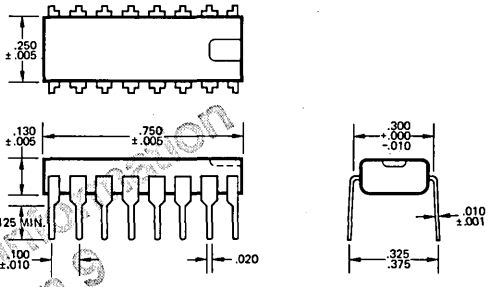
The 9314 can be used to eliminate mechanical switch bounce from a single pole double throw switch. The Latch operation is that of an active LOW input Set/Reset Latch.

Figure 16

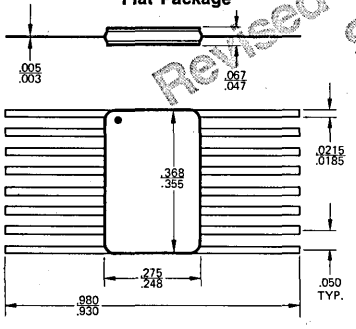
PHYSICAL DIMENSIONS
Hermetic Dual-In-Line



PHYSICAL DIMENSIONS
Molded Dual-In-Line

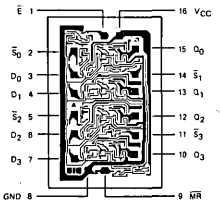


PHYSICAL DIMENSIONS
Flat Package



Metallization and Pad Layout

55 x 90 Mils



ADVANCED MICRO DEVICES INC.
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TELEX: 34-6306

Am93L14
Low-Power Four-Bit Latch

Distinctive Characteristics

- 50 mw typical power dissipation.
- 32 ns typical propagation delay.
- 100% reliability assurance testing in compliance with MIL STD 883
- Can be used as single line "D" latch or as set/reset latch

FUNCTIONAL DESCRIPTION

The Am93L14 is a four-bit latch with a common active LOW enable and overriding active LOW master reset. Each of the four latches can be used as a single line "D" latch by tying the appropriate $\overline{S}$ input LOW, or as an active LOW Set/Reset latch with reset override with the D input as the active LOW reset input and the $\overline{S}$ input as the set input.

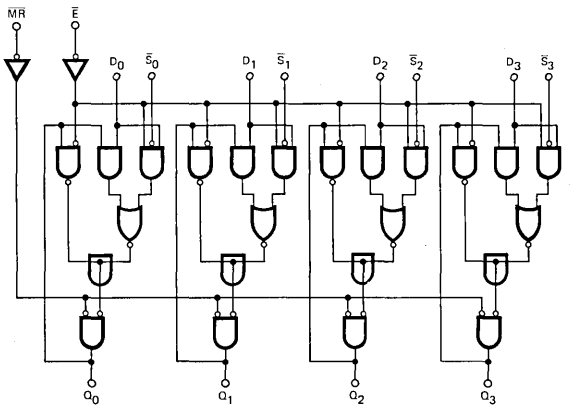
Data is transferred into the latch when the enable goes LOW and the latch stores the information when the enable goes HIGH. With the enable HIGH the latch is no longer affected by the $\overline{S}$ and D inputs. When the master reset goes LOW all latches are reset independent of all other input conditions.

TRUTH TABLE

$\overline{MR}$	$\overline{E}$	D	$\overline{S}$	$Q_{(tn+1)}$	Operation
L	X	X	X	L	Reset
H	L	L	L	L	D Mode
H	L	H	L	H	
H	H	X	X	$Q_{(tn)}$	
H	L	L	L	L	R/S Mode
H	L	H	L	H	
H	L	L	H	L	
H	L	H	H	$Q_{(tn)}$	
H	H	X	X	$Q_{(tn)}$	

H = HIGH Voltage Level L = LOW Voltage Level X = Don't Care

LOGIC DIAGRAM



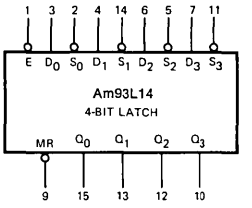
LOADING RULES

In Unit Loads (Notes)

	TTL LOADS		93L LOADS	
Input Load Factor	HIGH	LOW	HIGH	LOW
E, S_0, S_1, S_2, S_3	0.5	0.25	1.0	1.0
D_0, D_1, D_2, D_3	0.75	0.375	1.5	1.5
Output Drive	HIGH	LOW	HIGH	LOW
Q_0, Q_1, Q_2, Q_3	9	3	18	12

NOTES:
1) A TTL unit load is specified as 0.4 V at −1.6 mA LOW, 2.4 V at 40 μA HIGH.
2) A 93L unit load is specified as 0.3 V at −400 μA LOW, 2.4 V at 20 μA HIGH.
3) Enough output LOW current is available to mix TTL and 93L loads and still meet the 93L requirement of a V_{OL} of 0.3 V.

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

Am93L14 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
16-Pin Molded DIP	0°C to +75°C	U6M93L1459X
16-Pin Hermetic DIP	0°C to +75°C	U7B93L1459X
16-Pin Hermetic DIP	−55°C to +125°C	U7B93L1451X
16-Pin Hermetic Flat Pak	−55°C to +125°C	U4L93L1451X
Dice	Note	UXX93L14XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to $+V_{CC}$ max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current (Note 1)	−30 mA to +5.0 mA

Note 1. Maximum current defined by DC input voltage.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93L1459X $T_A = 0°C$ to $+75°C$ $V_{CC} = 4.75$ V to 5.25 V
Am93L1451X $T_A = -55°C$ to $+125°C$ $V_{CC} = 4.50$ V to 5.50 V

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -0.36$ mA $V_{IN} = V_{IH}$ or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $I_{OL} = 4.92$ mA $V_{IN} = V_{IH}$ or V_{IL}		0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.7	Volts
I_{IL} (Note 2)	93L Unit Load Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.3$ V		−0.25	−0.4	mA
I_{IH} (Note 2)	93L Unit Load Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.4$ V		2.0	20	μA
	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 5.5$ V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., $V_{OUT} = 0.0$ V	−10	−22	−40	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		10	16.5	mA

Notes: 1) Typical limits are at $V_{CC} = 5.0$ V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by the 93L input load factor. (See loading rules)

SWITCHING CHARACTERISTICS ($T_A = 25°C$) ($V_{CC} = 5.0$ V, $C_L = 15$ pF)

Parameters	Description		Min	Typ	Max	Units
$t_{pd+}(\overline{E})$	Turn Off Delay Enable to Output	See Fig. 1	21	43	90	ns
$t_{pd-}(\overline{E})$	Turn On Delay Enable to Output		19	38	80	ns
$t_{pd+}(D)$	Turn Off Delay Data to Output	See Fig. 1	10	19	45	ns
$t_{pd-}(D)$	Turn On Delay Data to Output		16	32	70	ns
$t_{sL}(\overline{DE})$	Set Up Time LOW Data to Enable	See Fig. 2	4		30	ns
$t_{sH}(\overline{DE})$	Set Up Time HIGH Data to Enable		−3		15	ns
$t_{pw}(\overline{E})$	Minimum Enable Pulse Width		13	26	50	ns
$t_{pw}(\overline{MR})$	Minimum Master Reset Pulse Width		12	24	45	ns
$t_{pd-}(\overline{MR})$	Turn On Delay Master Reset to Output		16	33	65	ns
$t_{rec}(\overline{MR})$	Master Reset Recovery Time		8	16	35	ns
$t_{pd+}(\overline{S})$	Turn Off Delay Set Input to Output		14	27	60	ns
$t_s(D\overline{S})$	Set Up Time HIGH Data to Set Input	See Fig. 3	1		15	ns

SWITCHING TIME WAVEFORMS

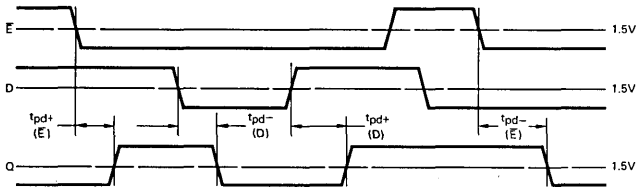


Fig. 1
Switching Delays

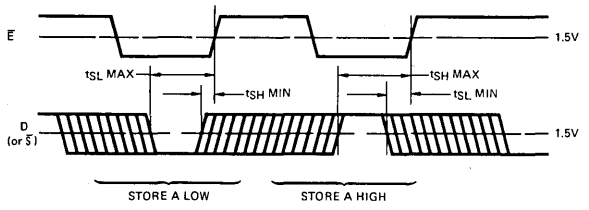


Fig. 2
Input Timing

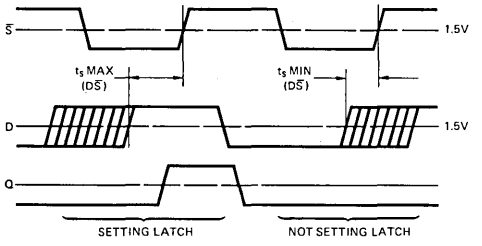


Fig. 3
Release of D input to set latch with S̄ input

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Am9318
Eight-Input Priority Encoder

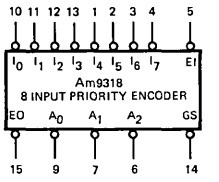
Distinctive Characteristics:

- Provides address of most significant active input.
- 100% reliability assurance testing including high temperature bake, temperature cycling, centrifuge and package hermeticity testing in compliance with MIL STD 883.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

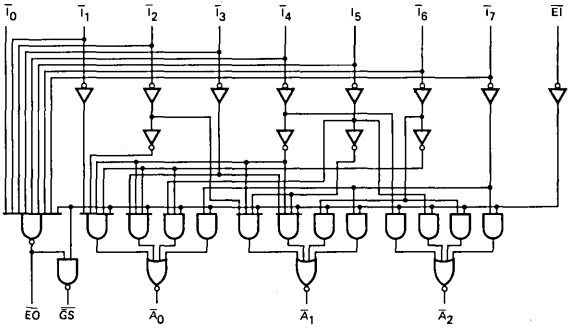
The Am9318 is an active LOW input Priority Encoder. The Encoder accepts 8 inputs and produces a binary weighted code of the highest order input on three active LOW outputs $\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$. When two or more inputs are simultaneously active the address of the input with the highest number is represented on the three outputs. Input seven ($\overline{I}_7$) has the highest priority. An active LOW Enable Input ($\overline{EI}$) and Enable Output ($\overline{EO}$) allow several encoders to be cascaded to allow encoding of more than 8 inputs. Enable Input HIGH will force all outputs HIGH. The Enable Output is LOW when all inputs ($\overline{I}_0$ to $\overline{I}_7$) are HIGH and the Enable Input is LOW. A LOW Group Signal ($\overline{GS}$) indicates that one of the 8 inputs is LOW. When the Enable Input is LOW, the Enable Output is the logic inverse of the Group Signal.

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

LOGIC DIAGRAM

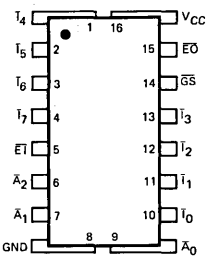


Am9318 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	U6M931859X
Hermetic DIP	−55°C to +125°C	U7B931851X
Hermetic DIP	0°C to 75°C	U7B931859X
Hermetic Flat Pak	−55°C to +125°C	U4L931851X
Dice	Note	UXX9318XXD

Note : The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} ma
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 m
DC Input Current	−30 mA to +5 m

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am931859X T_A = 0°C to +75°C V_{CC} = 5.0 V ±5%
Am931851X T_A = −55°C to +125°C V_{CC} = 5.0 V ±10%

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.8 mA V_{IN} = V_{IH} or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16.0 mA V_{IN} = V_{IH} or V_{IL}		0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V		−1.0	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V		4.0	40	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V	−30		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		50	77	mA

Notes: 1) Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by input load factor (see Loading Rules).

Switching Characteristics (T_A = 25°C)

Parameters			Test Conditions	Min	Typ	Max	Units
t_{pd+} ($\overline{I}$ $\overline{EO}$)	Turn Off Delay	Data Input to Enable Output	V_{CC} = 5.0 V, C_L = 15 pF	2	6	10(Note)	ns
t_{pd-} ($\overline{I}$ $\overline{EO}$)	Turn On Delay	Data Input to Enable Output	(Refer to Figure 4)	7	16	25	
t_{pd+} ($\overline{EI}$ $\overline{GS}$)	Turn Off Delay	Enable Input to Group Signal	V_{CC} = 5.0 V, C_L = 15 pF	4	10	15	ns
t_{pd-} ($\overline{EI}$ $\overline{GS}$)	Turn On Delay	Enable Input to Group Signal	(Refer to Figure 5)	12	16	25	
t_{pd+} ($\overline{EI}$ $\overline{EO}$)	Turn Off Delay	Enable Input to Enable Output	V_{CC} = 5.0 V, C_L = 15 pF	4	10	15	ns
t_{pd-} ($\overline{EI}$ $\overline{EO}$)	Turn On Delay	Enable Input to Enable Output	(Refer to Figure 6)	14	21	32	
t_{pd+} ($\overline{EI}$ $\overline{A}$)	Turn Off Delay	Enable Input to Data Output	V_{CC} = 5.0 V, C_L = 15 pF	4	11	18	ns
t_{pd-} ($\overline{EI}$ $\overline{A}$)	Turn On Delay	Enable Input to Data Output	(Refer to Figure 7)	10	15	25	
t_{pd+} ($\overline{I}$ $\overline{GS}$)	Turn Off Delay	Data Input to Group Signal	V_{CC} = 5.0 V, C_L = 15 pF	12	20	35	ns
t_{pd-} ($\overline{I}$ $\overline{GS}$)	Turn On Delay	Data Input to Group Signal	(Refer to Figure 8)	10	15	23	
t_{pd+} ($\overline{I}$ $\overline{A}$)	Turn Off Delay	Data Input to Data Output	V_{CC} = 5.0 V, C_L = 15 pF	5	16	25	ns
t_{pd-} ($\overline{I}$ $\overline{A}$)	Turn On Delay	Data Input to Data Output	(Refer to Figure 9)	5	17	27	

Note. Maximum for Industrial Grade, Am931859X, is 12 ns.

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH-signal level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to a LOW signal level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS:

$\overline{A}_j$ Address Data Outputs. LOW address of most significant LOW Data Input (j = 0-3.)

$\overline{EI}$ LOW Enable Input. Enable Input HIGH forces all outputs HIGH.

$\overline{EO}$ LOW Enable Output indicates that Enable Input is LOW and no input is active.

FANOUT The logic HIGH or LOW output drive capability in terms of input Unit Loads.

$\overline{GS}$ LOW Group Signal if Enable Input is LOW indicates when any input is active.

$\overline{I}_j$ Data Inputs designates one of the eight active LOW Inputs (j = 0-7.)

UNIT LOAD One T^2L gate input load. In the HIGH state it is equal to I_R and in the LOW state it is equal to I_F.

OPERATIONAL TERMS:

I_{IL} Forward input load current, for unit input load.

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into output in V_{OL} test.

I_{IH} Reverse input load current with V_{OH} applied to input.

I_{CC} The current drawn by the device with input terminals grounded and output terminals open.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

SWITCHING TERMS:

$t_{pd+}(\overline{IEO})$ The propagation delay from a Data Input signal HIGH to LOW transition to the $\overline{EO}$ output LOW to HIGH transition.

$t_{pd-}(\overline{IEO})$ The propagation delay from a Data Input signal LOW to HIGH transition to the $\overline{EO}$ output HIGH to LOW transition.

$t_{pd+}(\overline{EIGS})$ The propagation delay from the $\overline{EI}$ input signal LOW to HIGH transition to the $\overline{GS}$ output LOW to HIGH transition.

$t_{pd-}(\overline{EIGS})$ The propagation delay from the $\overline{EI}$ input signal HIGH to LOW transition to the $\overline{GS}$ output HIGH to LOW transition.

$t_{pd+}(\overline{EIEO})$ The propagation delay from the $\overline{EI}$ input LOW to HIGH transition to the $\overline{EO}$ output LOW to HIGH transition.

$t_{pd-}(\overline{EIEO})$ The propagation delay from the $\overline{EI}$ input HIGH to LOW transition to the $\overline{EO}$ output HIGH to LOW transition.

$t_{pd+}(\overline{EI}\overline{A})$ The propagation delay from the $\overline{EI}$ input LOW to HIGH transition to the Data $\overline{A}$ output LOW to HIGH transition.

$t_{pd-}(\overline{EI}\overline{A})$ The propagation delay from the $\overline{EI}$ input HIGH to LOW transition to the Data $\overline{A}$ output HIGH to LOW transition.

$t_{pd+}(\overline{IGS})$ The propagation delay from the Data Input signal LOW to HIGH transition to the $\overline{GS}$ output LOW to HIGH transition.

$t_{pd-}(\overline{IGS})$ The propagation delay from the Data Input signal HIGH to LOW transition to the $\overline{GS}$ output HIGH to LOW transition.

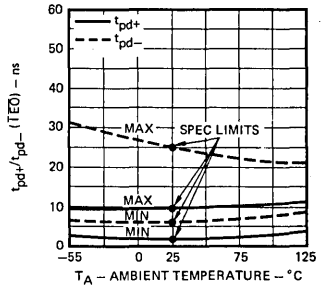
$t_{pd+}(\overline{I}\,\overline{A})$ The propagation delay from the Data Input signal transition to the LOW to HIGH Data $\overline{A}$ output transition.

$t_{pd-}(\overline{I}\,\overline{A})$ The propagation delay from the Data Input signal transition to the HIGH to LOW Data $\overline{A}$ output transition.

Switching Characteristics

The active input is driven by a 9002 TTμL gate. The input and output pins under test are loaded with a 15 pF capacitance. (This includes probe and jig capacitance.)

Data Input To Enable Output



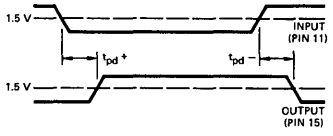
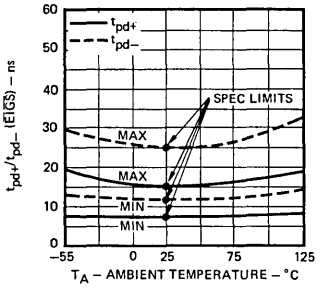


Figure 1

Enable Input To Group Signal



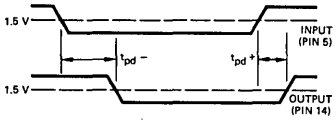
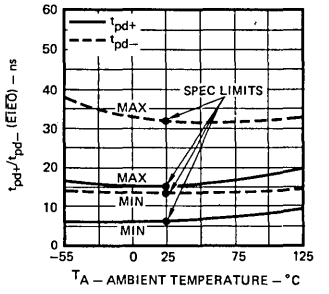


Figure 2

Enable Input To Enable Output



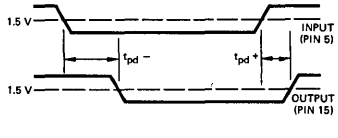
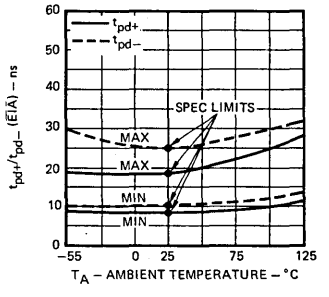


Figure 3

Enable Input To Data Output



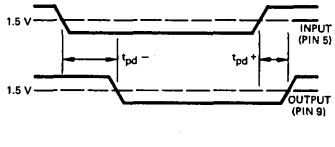
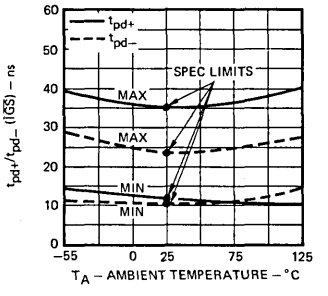


Figure 4

Data Input To Group Signal



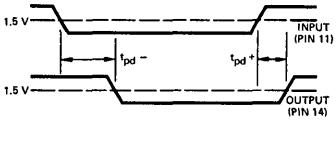
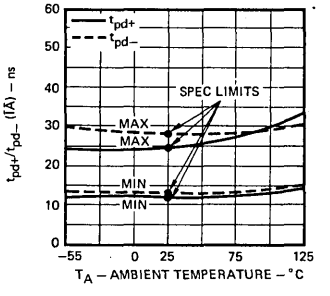


Figure 5

Data Input To Data Output



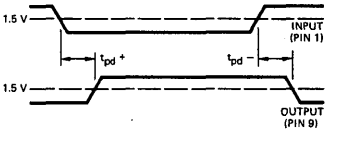


Figure 6

TRUTH TABLE

Inputs									Outputs				
$\overline{EI}$	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	$\overline{GS}$	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't care

Table I

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Table II

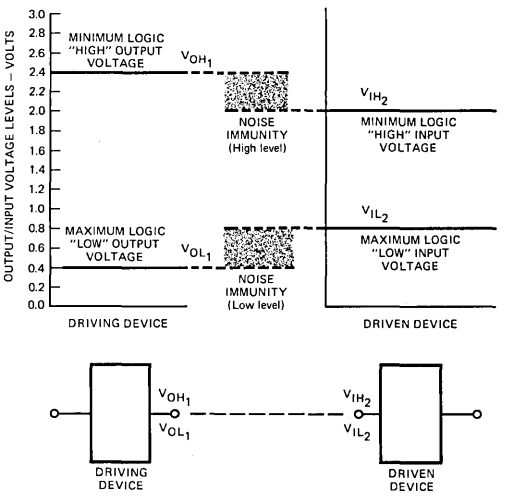
Am9318 LOADING RULES (in unit loads)

Input/Output	Pin No.s	Input Load	Output Drive HIGH	LOW
$\overline{I}_4$	1	2	—	—
$\overline{I}_5$	2	2	—	—
$\overline{I}_6$	3	2	—	—
$\overline{I}_7$	4	2	—	—
$\overline{EI}$	5	2	—	—
$\overline{A}_2$	6	—	20	10
$\overline{A}_1$	7	—	20	10
GND	8	—	—	—
$\overline{A}_0$	9	—	20	10
$\overline{I}_0$	10	1	—	—
$\overline{I}_1$	11	2	—	—
$\overline{I}_2$	12	2	—	—
$\overline{I}_3$	13	2	—	—
$\overline{GS}$	14	—	20	10
$\overline{EO}$	15	—	20	10
V_{CC}	16	—	—	—

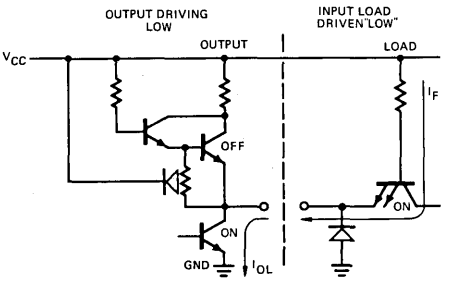
Table III

INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH



Current Interface Conditions — LOW



Current Interface Conditions — HIGH

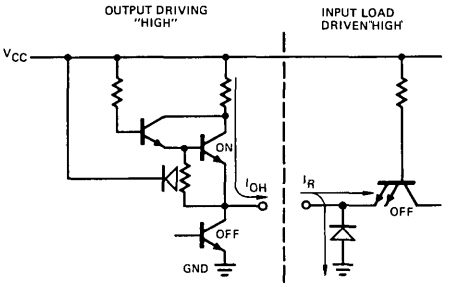


Figure 7

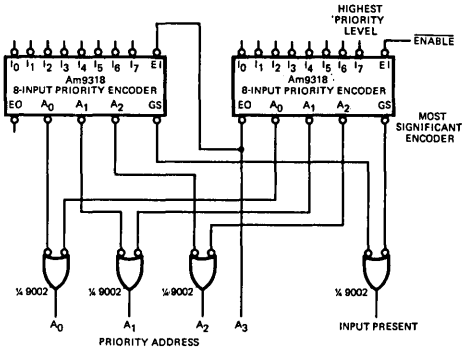


Figure 8

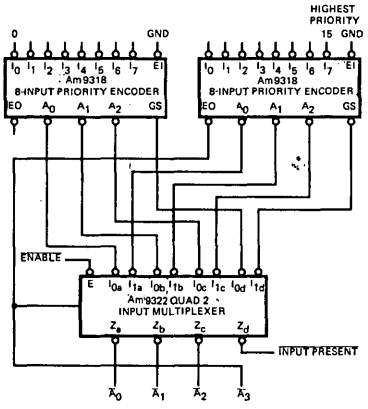


Figure 9

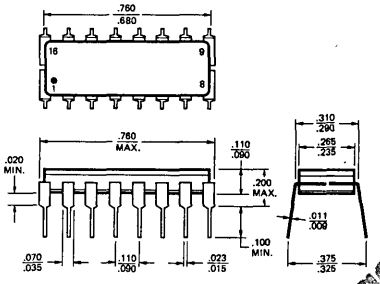
16-INPUT PRIORITY ENCODER

The number of priority levels can be increased by cascading 9318 encoders. This may be accomplished by connecting the most significant encoder's enable output ($\overline{EO}$) to the next most significant encoder's enable input ($\overline{EI}$) and using OR gates to combine outputs. A higher speed expansion method is to use multiplexers to combine output signals as shown in Figure 9 .

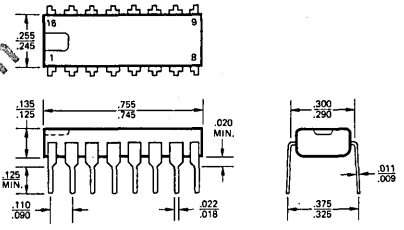
PHYSICAL DIMENSIONS

Dual-In-Line

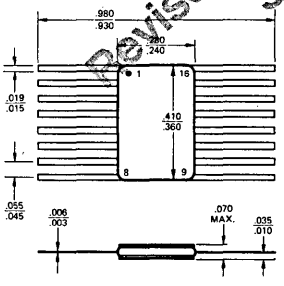
Hermetic



Molded

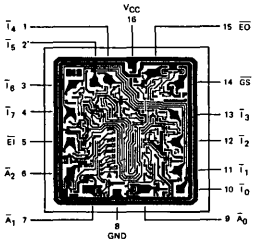


Flat Package



Metallization and Pad Layout

77 x 80 Mils



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(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am93L18

Low-Power Eight-Input Priority Encoder

Distinctive Characteristics

- 75 mw typical power dissipation.
- 29 ns typical propagation delay.
- 100% reliability assurance testing in compliance with MIL STD 883
- Fan-out of three to standard TTL devices.

FUNCTIONAL DESCRIPTION

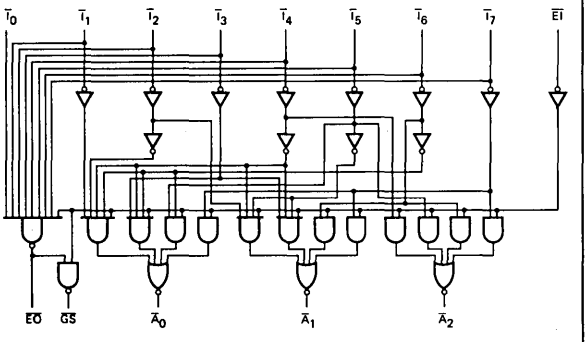
The 93L18 is a low-power eight-input priority encoder. There are eight active LOW data inputs, $\overline{I}_0$ through $\overline{I}_7$, with $\overline{I}_7$ assigned the highest priority and $\overline{I}_0$ the lowest. When any of the inputs are LOW, the active LOW address outputs, $\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$, will indicate the binary address of the active input of highest priority, as shown in the truth table below. The group signal output, $\overline{GS}$, goes LOW if at least one input is active. An enable input ($\overline{EI}$) and an enable output ($\overline{EO}$) are provided to make possible cascading of 93L18's for encoding more than eight inputs. If the enable input is HIGH, then the device is disabled and all outputs are forced HIGH. The enable output goes LOW when the enable input is LOW and all the data inputs are HIGH. The 93L18's are cascaded by connecting the enable output of one 93L18 to the enable input of the 93L18 of next lower priority. A lower priority device can then produce an output only if all higher priority devices are enabled and have no active data inputs.

TRUTH TABLE

Inputs									Outputs				
$\overline{EI}$	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	$\overline{GS}$	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = HIGH Voltage Level L = LOW Voltage Level X = Don't care

LOGIC DIAGRAM



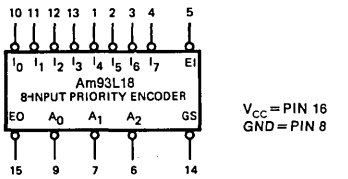
LOADING RULES

In Unit Loads (Notes)

Input Load Factor	TTL LOADS HIGH	TTL LOADS LOW	93L LOADS HIGH	93L LOADS LOW
$\overline{I}_0$	0.5	0.25	1.0	1.0
$\overline{I}_1$, $\overline{I}_2$, $\overline{I}_3$, $\overline{I}_4$, $\overline{I}_5$, $\overline{I}_6$, $\overline{I}_7$, $\overline{EI}$	1.0	0.5	2.0	2.0
Output Drive	HIGH	LOW	HIGH	LOW
$\overline{EO}$, $\overline{GS}$	10	2	20	8
$\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$	10	3	20	12

NOTES:
1) A TTL unit load is specified as 0.4 V at −1.6 mA LOW, 2.4 V at 40 μA HIGH.
2) A 93L unit load is specified as 0.3 V at −400 μA LOW, 2.4 V at 20 μA HIGH.
3) Enough output LOW current is available to mix TTL and 93L loads and still meet the 93L requirement of a V_{OL} of 0.3 V.

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

Am93L18 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
16-Pin Molded DIP	0°C to +75°C	U6M93L1859X
16-Pin Hermetic DIP	0°C to +75°C	U7B93L1859X
16-Pin Hermetic DIP	−55°C to +125°C	U7B93L1851X
16-Pin Hermetic Flat Pak	−55°C to +125°C	U4L93L1851X
Dice	Note	UXX93L18XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current (Note 1)	−30 mA to +5.0 mA

Note 1. Maximum current defined by DC input voltage.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93L1859X T_A = 0°C to +75°C V_{CC} = 4.75 V to 5.25 V
Am93L1851X T_A = −55°C to +125°C V_{CC} = 4.50 V to 5.50 V

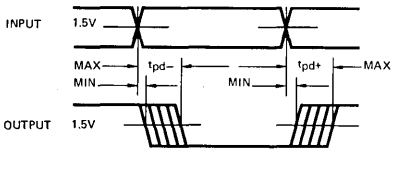
Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 4.92 mA V_{IN} = V_{IH} or V_{IL}		0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.7	Volts
I_{IL} (Note 2)	93L Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.3 V		−0.25	−0.4	mA
I_{IH} (Note 2)	93L Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V		2.0	20	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V	−10	−22	−40	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		15	22	mA

Notes: 1) Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by the 93L input load factor. (See loading rules)

SWITCHING CHARACTERISTICS (T_A = 25°C)

Parameters			Test Conditions	Min	Typ	Max	Units
t_{pd+} ($\overline{I}$ $\overline{EO}$)	Turn Off Delay	Data Input to Enable Output HIGH	V_{CC} = 5.0 V, C_L = 15 pF	5	10	15	ns
t_{pd-} ($\overline{I}$ $\overline{EO}$)	Turn On Delay	Data Input to Enable Output LOW		20	40	60	
t_{pd+} ($\overline{EI}$ $\overline{GS}$)	Turn Off Delay	Enable Input to Group Signal HIGH		5	18	27	ns
t_{pd-} ($\overline{EI}$ $\overline{GS}$)	Turn On Delay	Enable Input to Group Signal LOW		14	28	42	
t_{pd+} ($\overline{EI}$ $\overline{EO}$)	Turn Off Delay	Enable Input to Enable Output HIGH		5	18	27	ns
t_{pd-} ($\overline{EI}$ $\overline{EO}$)	Turn On Delay	Enable Input to Enable Output LOW		21	42	63	
t_{pd+} ($\overline{EI}$ $\overline{A}$)	Turn Off Delay	Enable Input to Data Output HIGH		5	19	28	ns
t_{pd-} ($\overline{EI}$ $\overline{A}$)	Turn On Delay	Enable Input to Data Output LOW		13	26	39	
t_{pd+} ($\overline{I}$ $\overline{GS}$)	Turn Off Delay	Data Input to Group Signal HIGH		24	48	72	ns
t_{pd-} ($\overline{I}$ $\overline{GS}$)	Turn On Delay	Data Input to Group Signal LOW		13	27	40	
t_{pd+} ($\overline{I}$ $\overline{A}$)	Turn Off Delay	Data Input to Data Output HIGH		9	29	43	ns
t_{pd-} ($\overline{I}$ $\overline{A}$)	Turn On Delay	Data Input to Data Output LOW		9	29	43	

SWITCHING TIME WAVEFORMS



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Am9321
Dual Demultiplexer/One-of-Four Decoder

Distinctive Characteristics

- Dual 1-of-4 Decoder
- Active LOW enable for each decoder
- Can be used as dual four channel Demultiplexer
- 100% reliability assurance testing in compliance with MIL-STD-883

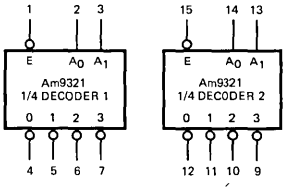
FUNCTIONAL DESCRIPTION

The Am9321 dual demultiplexer/one-of-four decoder consists of two identical independent decoders. Each decoder accepts two address inputs which select one-of-four mutually exclusive outputs. An active LOW enable is also provided on each decoder for expansion and demultiplexing applications. When this enable is at a HIGH logic level all the decoder outputs are forced HIGH.

In the demultiplexing mode data is presented at the enable input and appears noninverted at the selected output.

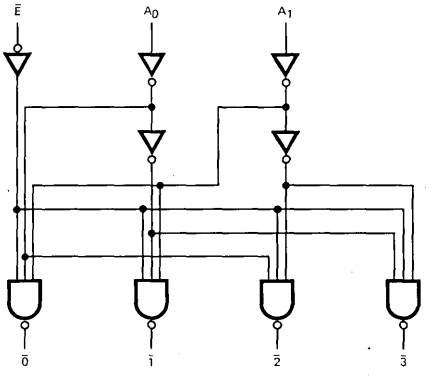
The Am9321 is an ideal MSI element for use in decoding in high-speed memory systems.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM

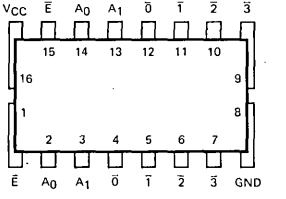


Note: Only one decoder shown.

Am9321 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	9321PC
Hermetic DIP	0°C to +75°C	9321DC
Dice	0°C to +75°C	9321XC
Hermetic DIP	–55°C to +125°C	9321DM
Hermetic Flat Pak	–55°C to +125°C	9321FM
Dice	–55°C to +125°C	9321XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

9321XC T_A = 0°C to +75°C V_{CC} = 5.0V ±5%
9321XM T_A = −55°C to +125°C V_{CC} = 5.0V ±10%

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.8mA V_{IN} = V_{IH} or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16.0mA V_{IN} = V_{IH} or V_{IL}		0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logic HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logic LOW voltage for all inputs			0.8	Volts
I_{IL}	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V		−1.0	−1.6	mA
I_{IH}	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V		6.0	40	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V	−20	−40	−70	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		30	50	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

Switching Characteristics (T_A = 25°C)

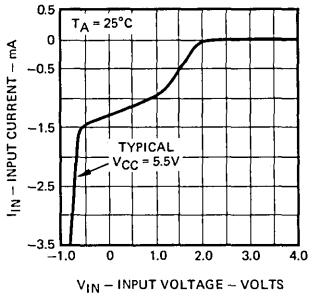
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Turn Off Delay A Input to Output	V_{CC} = 5.0V C_L = 15pF		13	20	ns
t_{PHL}	Turn On Delay A Input to Output			10	21	ns
t_{PLH}	Turn Off Delay $\overline{E}$ Input to Output			9	14	ns
t_{PHL}	Turn On Delay $\overline{E}$ Input to Output			10	18	ns

Notes: 1. Maximum current defined by DC Input Voltage.
2. Pulse tested.

PERFORMANCE CURVES

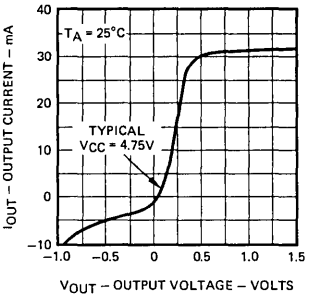
Input/Output Characteristics

Input

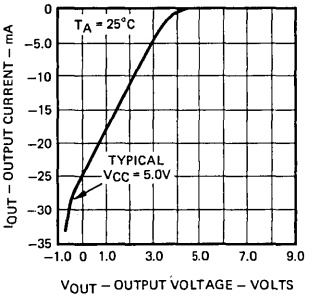


Output

Low State



High State



DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH-signal level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to a LOW signal level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS:

Decoder/Demultiplexer On the basis of an applied instruction, channels of communication are selected which connect certain sources of information to certain destinations e.g., the distribution of timing signals; the interconnection between arithmetic registers.

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

Unit load One T^2L gate input load. In the HIGH state it is equal to 40μA at 2.4V and in the LOW state it is equal to −1.6mA at 0.4V.

OPERATIONAL TERMS:

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into output in V_{OL} test.

I_{CC} The current drawn by the device under a +5.0V power supply, bias input terminals grounded and output terminals open.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

SWITCHING TERMS: (All switching times are measured at the 1.5V logic level).

t_{PLH} The propagation delay measured from the input transition to a corresponding output signal LOW-HIGH transition.

t_{PHL} The propagation delay measured from the input transition to a corresponding output signal HIGH-LOW transition.

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
Advanced Micro Devices 54/7400 Series	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

TRUTH TABLE

For Each Decoder

Inputs			Outputs			
$\overline{E}$	A_0	A_1	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

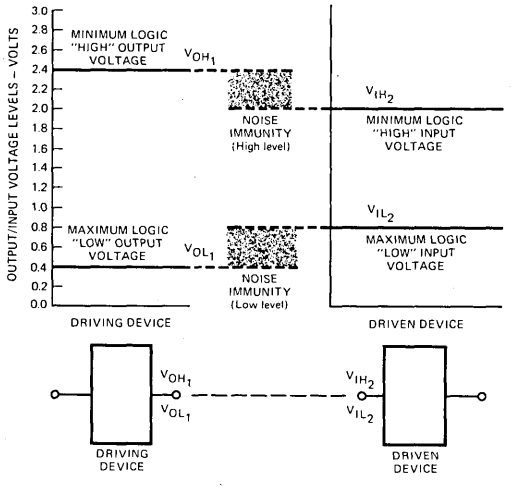
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

LOADING RULES

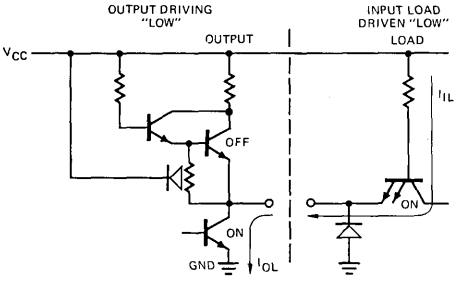
Input/Output	Pin No.'s	Input Unit Load	Fanout Output HIGH	Fanout Output LOW
$\overline{E}$ Decoder 1	1	1	–	–
A_0	2	1	–	–
A_1	3	1	–	–
$\overline{0}$	4	–	20	10
$\overline{1}$	5	–	20	10
$\overline{2}$	6	–	20	10
$\overline{3}$	7	–	20	10
GND	8	–	–	–
$\overline{3}_{out}$ Decoder 2	9	–	20	10
$\overline{2}$	10	–	20	10
$\overline{1}$	11	–	20	10
$\overline{0}$	12	–	20	10
A_1	13	1	–	–
A_0	14	1	–	–
$\overline{E}$	15	1	–	–
V_{CC}	16	–	–	–

INPUT/OUTPUT INTERFACE CONDITIONS

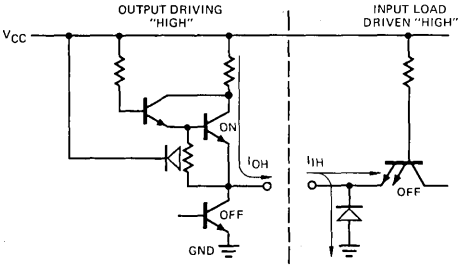
Voltage Interface Conditions – LOW & HIGH



Current Interface Conditions – LOW

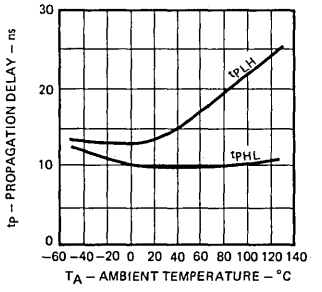


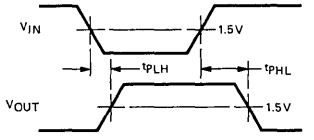
Current Interface Conditions – HIGH



SWITCHING CHARACTERISTICS
(Typical)

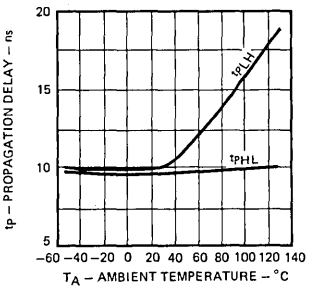
Address Input to Output

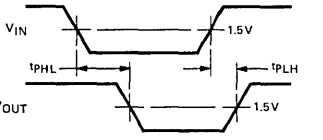




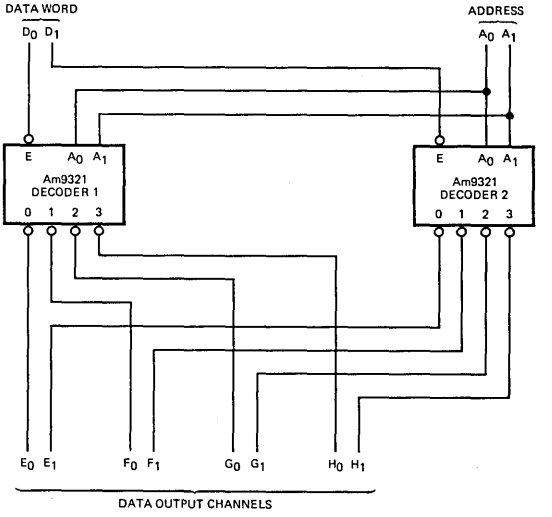
Other Conditions: $\overline{E}$ = LOW

Enable Input to Output





BASIC DEMULTIPLEXER/DECODER APPLICATIONS



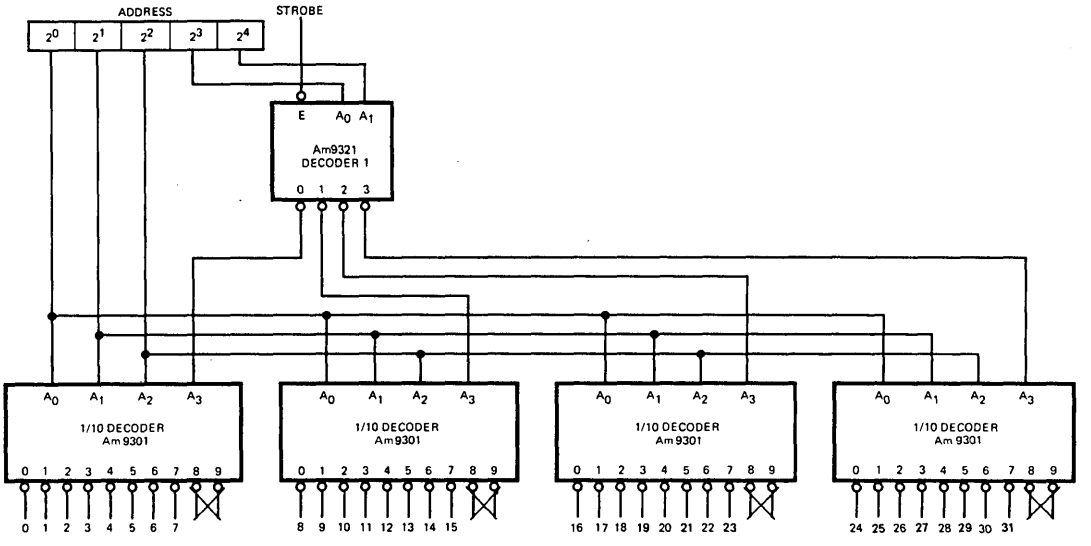
Address		Output Channel
A0	A1	
0	0	E
1	0	F
0	1	G
1	1	H

Dual 4 Output Demultiplexer

A 2-Bit Data Field D_0, D_1 is routed to one of four channels E, F, G, H under control of the address Field A.

ADDITIONAL APPLICATIONS

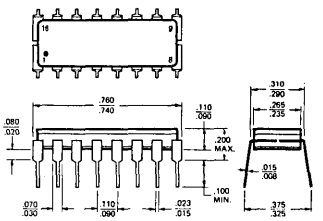
ONE-OUT-OF-THIRTY-TWO DECODER



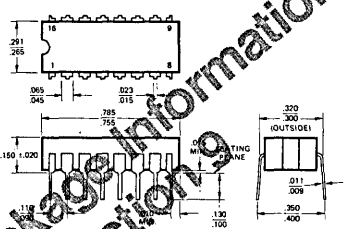
Am9321 Dual 1-of-4 Decoder can be used with other decoders such as the Am9301 1-of-10 Decoder or Am9311 1-of-16 Decoder to build large decoding trees or to form multi channel Demultiplexers.

PHYSICAL DIMENSIONS
Dual-In-Line

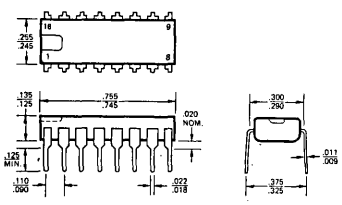
Hermetic



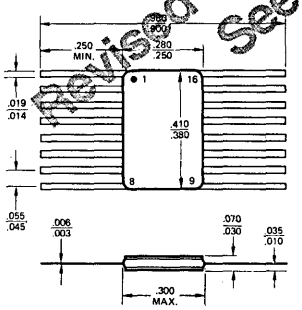
Ceramic



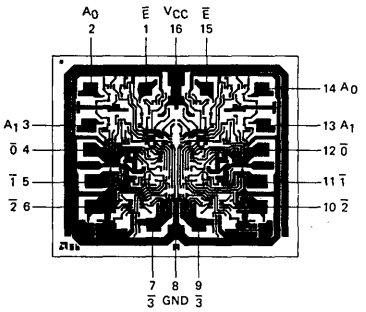
Molded



Flat Package



Metallization and Pad Layout



DIE SIZE 0.076" X 0.063"

ADVANCED
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TELEX: 34-6306

Am93L21

Low-Power Dual Demultiplexer/One-of-Four Decoder

Distinctive Characteristics

- 45 mW typical power dissipation.
- Can act as dual four way demultiplexer.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Fan-out of three standard TTL circuits.

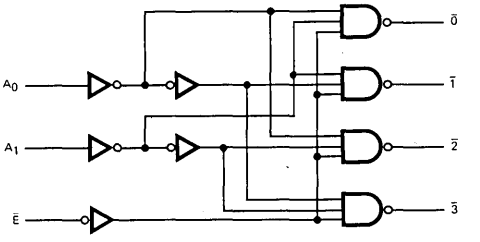
FUNCTIONAL DESCRIPTION

The Am93L21 low-power dual demultiplexer/one-of-four decoder consists of two identical independent decoders. Each decoder accepts two address inputs which select one-of-four mutually exclusive outputs. An active LOW enable is also provided on each decoder for expansion and demultiplexing applications. When this enable is at a HIGH logic level all the decoder outputs are forced HIGH.

In the demultiplexing mode data is presented at the enable input and appears noninverted at the selected output.

The Am93L21 is an ideal MSI element for use in decoding in high-speed memory systems.

LOGIC DIAGRAM



Note: Only one decoder shown.

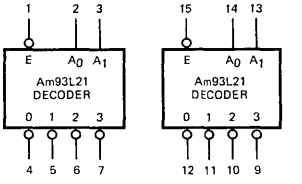
LOADING RULES

In Units Loads (Notes)

Input Loading	TTL Loads HIGH	TTL Loads LOW	93L Loads HIGH	93L Loads LOW
All Inputs	0.5	0.25	1.0	1.0
Output Drive	**HIGH**	**LOW**	**HIGH**	**LOW**
All Outputs	10	3	12	12

Notes:
1. A TTL unit load is specified as 0.4 V at −1.6 mA LOW, 2.4 V at 40 μA HIGH.
2. A 93L unit load is specified as 0.3 V at −400 μA LOW, 2.4 V at 20 μA HIGH.
3. Enough output LOW current is available to mix TTL and 93L loads and still meet the 93L requirement of a V_{OL} of 0.3 V.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

Am93L21 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	93L21PC
Hermetic DIP	0°C to +75°C	93L21DC
Dice	0°C to +75°C	93L21XC
Hermetic DIP	−55°C to +125°C	93L21DM
Hermetic Flat Pak	−55°C to +125°C	93L21FM
Dice	−55°C to +125°C	93L21XM

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Outputs	30mA
DC Input Current (Note 1)	−30mA to +5.0mA

Note 1. Maximum current defined by DC input voltage.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93L21XC T_A = 0°C to +75°C V_{CC} = 4.75V to 5.25V
Am93L21XM T_A = −55°C to +125°C V_{CC} = 4.50V to 5.50V

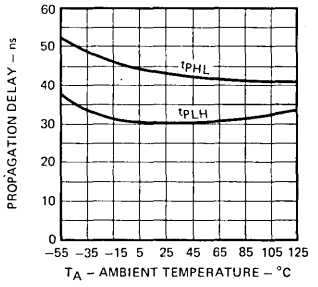
Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.4mA V_{IN} = V_{IH} or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 4.92mA V_{IN} = V_{IH} or V_{IL}		0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logic HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logic LOW voltage for all inputs			0.7	Volts
I_{IL} (Note 2)	93L Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.3V		−0.25	−0.4	mA
I_{IH} (Note 2)	93L Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V		2.0	20	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V	−2.5	−16	−25	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		9.0	13.2	mA

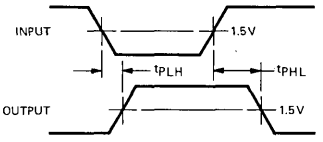
Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. Actual input currents are obtained by multiplying unit load current by the 93L input load factor. (See loading rules)

Switching Characteristics (T_A = 25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PHL}	Delay Address to Output HIGH	V_{CC} = 5.0V C_L = 15pF		30	50	ns
t_{PLH}	Delay Address to Output LOW			43	65	ns
t_{PHL}	Delay Enable to Output HIGH			23	40	ns
t_{PLH}	Delay Enable to Output LOW			34	52	ns

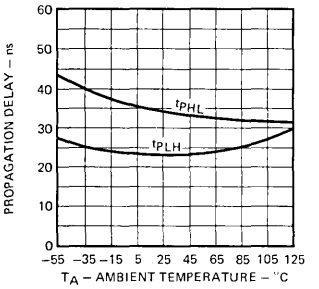
Address Input to Output

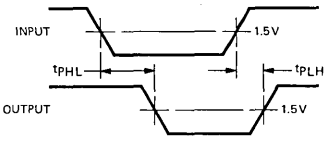




Other Conditions: Pins 15, 14 = GND

Enable Input to Output





Other Conditions: Pins 2, 3 = GND

ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am54/74157•Am9322

Quad Two-Input Multiplexer

Distinctive Characteristics:

- Selects four of eight data inputs with single select line and over-riding enable.
- 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and package hermeticity testing in compliance with MIL STD 883.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Available in highly reliable molded epoxy, hermetic dual-in-line or Hermetic flat package.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

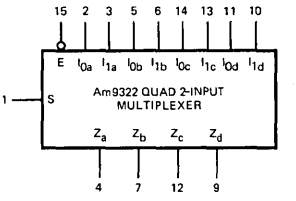
FUNCTIONAL DESCRIPTION

The Am9322 Quad Two-Input Multiplexer is the logic implementation of a four-pole, two-position switch with the position of the switch set by the logic level supplied to the select input. An active low enable is provided. The logic equations describing the device are given below.

$$Z_a = E\,(I_{0a}\overline{S} + I_{1a}S) \qquad Z_c = E\,(I_{0c}\overline{S} + I_{1c}S)$$
$$Z_b = E\,(I_{0b}\overline{S} + I_{1b}S) \qquad Z_d = E\,(I_{0d}\overline{S} + I_{1d}S)$$

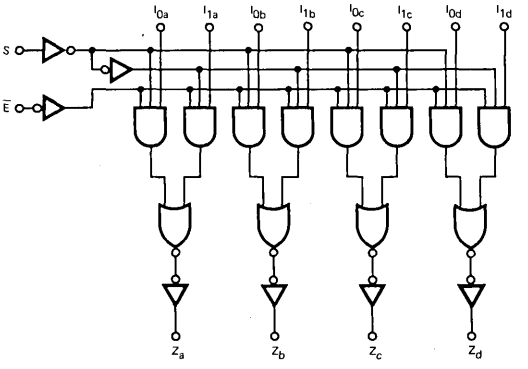
The Am9322 is useful for data bussing and general logic design. Some typical applications are shown in Figures 6 and 7.

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

LOGIC DIAGRAM

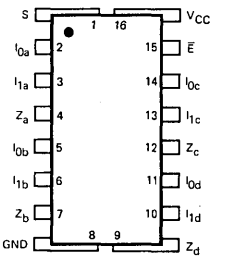


Am9322 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	U6M932259X
Hermetic DIP	0°C to +75°C	U7B932259X
Hermetic DIP	−55°C to +125°C	U7B932251X
Hermetic Flat Pak	−55°C to +125°C	U4L932251X
Dice	Note	UXX9322XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to + 125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am932259X T_A = 0°C to +75°C V_{CC} = 5.0 V ±5%
Am932251X T_A = −55°C to +125°C V_{CC} = 5.0 V ±10%

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.8 mA V_{IN} = V_{IH} or V_{IL}		2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16.0 mA V_{IN} = V_{IH} or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V			−1.0	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V			4.0	40	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V		−30		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. All inputs and outputs HIGH	Am932251X		30	47	mA
			Am932259X		30	47	mA

Notes: 1) Typical Limits are at V_{CC} = 5.0 V, 25°C Ambient and maximum loading.
2) Actual Input currents are obtained by multiplying unit load current by input load factor (See Loading Rules).

Am9322 Switching Characteristics (T_A = +25°C)

Parameters	Description		Test Conditions	Am932251X Min	Typ	Max	Am932259X Min	Typ	Max	Units
t_{pd+}(S)	Turn Off Delay	Select Input/Output		8	17	25	8	17	30	ns
t_{pd-}(S)	Turn On Delay	Select Input/Output	V_{CC} = 5.0 V	10	20	27	10	20	31	ns
t_{pd+}(D)	Turn Off Delay	Data Input/Output	C_L = 15 pF	4	10	17	5	10	22	ns
t_{pd-}(D)	Turn On Delay	Data Input/Output		4	11	16	5	11	18	ns
t_{pd+}($\overline{E}$)	Turn Off Delay	Enable Input/Output	(Refer to Figures 1 & 4)	6	12	20	6	12	24	ns
t_{pd-}($\overline{E}$)	Turn On Delay	Enable Input/Output		9	19	23	9	19	26	ns

Am54/74157 Switching Characteristics (T_A = +25°C)

Parameter	Description	Test Condition	Min.	Typ.	Max.	Units
t_{pd+}	Data to Output	V_{CC} = 5V, C_L = 15 pF, R_L = 400Ω			14	ns
t_{pd-}					14	
t_{pd+}	Strobe to Output				20	ns
t_{pd-}					21	
t_{pd+}	Select to Output				23	ns
t_{pd-}					27	

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH-signal level or when used with V_{CC} to indicate HIGH V_{CC} value.

I Input.

L LOW, applying to a LOW signal level or when used with V_{CC} to indicate LOW V_{CC} value.

O Output.

FUNCTIONAL TERMS:

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

Input Unit Load One T^2L gate input load. In the HIGH state it is equal to I_R and in the LOW state it is equal to I_F.

I_{ia}, I_{ib}, I_{ic}, I_{id} Data Inputs One of the two multiplexer data inputs for multiplexers a, b, c or d. i = 0, 1.

Z_j Output The logic output of the two input multiplexers.
j = a, b, c, d

OPERATIONAL TERMS:

I_{IL} Forward input load current, for unit input load. Refer to Figure 5.

I_{OH} Output HIGH current, forced out of output in V_{OH} test. Refer to figure 5.

I_{OL} Output LOW current, forced into the output in V_{OL} test. Refer to Figure 5.

I_{CC} The current drawn by the device with input and output terminals open.

I_{IH} Reverse input load current with V_{OH} applied to input. Refer to Figure 5.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage. Refer to Figure 5.

V_{IL} Maximum logic LOW input voltage. Refer to Figure 5.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output. Refer to Figure 5.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output. Refer to Figure 5.

SWITCHING TERMS: (All switching times are measured at the 1.5 V logic level).

t_{pd+}**(D)** The propagation delay from a Data Input signal transition to the output LOW-HIGH transition. Refer to Figure 1.

t_{pd-}**(D)** The propagation delay from a Data Input signal transition to the output HIGH-LOW transition. Refer to Figure 1.

t_{pd+}**($\bar{E}$)** The propagation delay from the Enable Signal transition to the Z_a output LOW-HIGH transition. Refer to Figure 1.

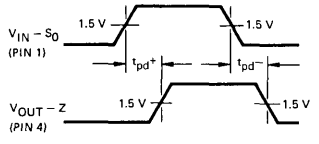
t_{pd-}**($\bar{E}$)** The propagation delay from the Enable Signal transition to the Z_a output HIGH-LOW transition. Refer to Figure 1.

t_{pd+}**(S)** The propagation delay from the Select Input signal transition to the Z_a output LOW-HIGH transition. Refer to Figure 1.

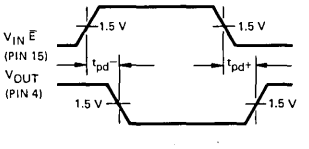
t_{pd-}**(S)** The propagation delay from the Select Input signal transition to the Z_a output HIGH-LOW transition. Refer to Figure 1.

SWITCHING TIME WAVEFORMS

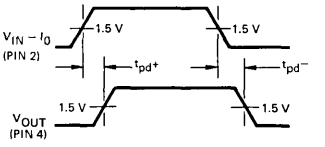
t_{pd}; S to Z_a
CONDITIONS
Pins 2, 15 = GND.
Pin 3 = V_{CC}



t_{pd}; $\bar{E}$ to Z_a
CONDITIONS
All Other Inputs High



t_{pd}; I_{0a} to Z_a
CONDITIONS
Pins 1, 15 = GND.



All inputs are outputs of TTμL series gates loaded with 15 pF. All outputs are loaded with the same capacitance (referred to as C_L) and only with capacitance.

Figure 1

PERFORMANCE CURVES

Input Characteristics

Input Current Versus Input Voltage

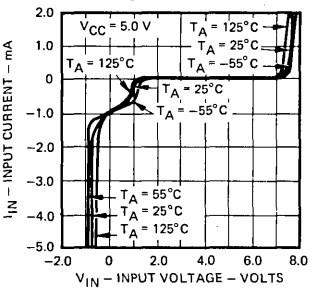
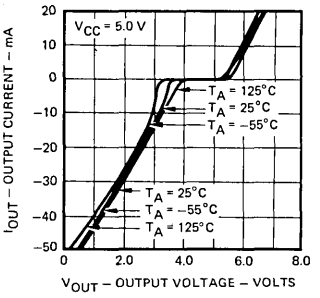


Figure 2

Output Characteristics

Output Current Versus Output Voltage (Output High)



Output Current Versus Output Voltage (Output Low)

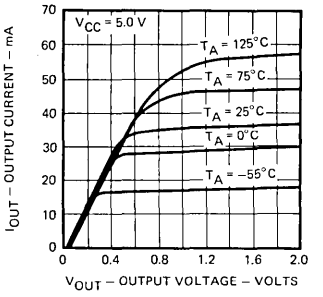
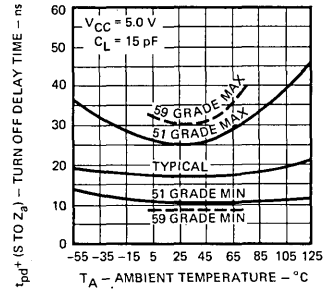


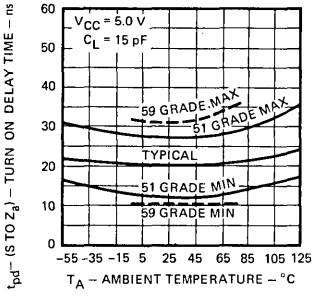
Figure 3

Switching Characteristics

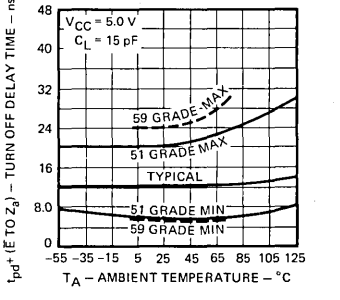
Turn Off Delay Time Versus Ambient Temperature (S to Z_a)



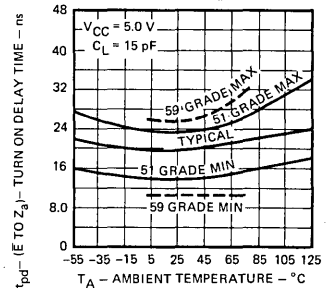
Turn On Delay Time Versus Ambient Temperature (S to Z_a)



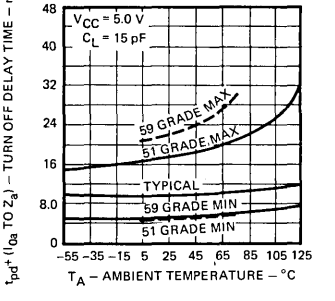
Turn Off Delay Time Versus Ambient Temperature ($\overline{E}$ to Z_a)



Turn On Delay Time Versus Ambient Temperature ($\overline{E}$ to Z_a)



Turn Off Delay Time Versus Ambient Temperature (I_{0a} to Z_a)



Turn On Delay Time Versus Ambient Temperature (I_{0a} to Z_a)

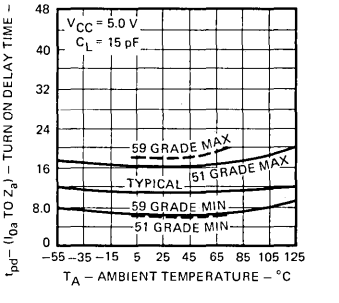


Figure 4

TRUTH TABLE

Enable	Select Input	Data Inputs		Output
$\overline{E}$	S	I_{0i}	I_{Ii}	Z_i
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
i = a, b, c, d

TABLE I

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

TABLE III

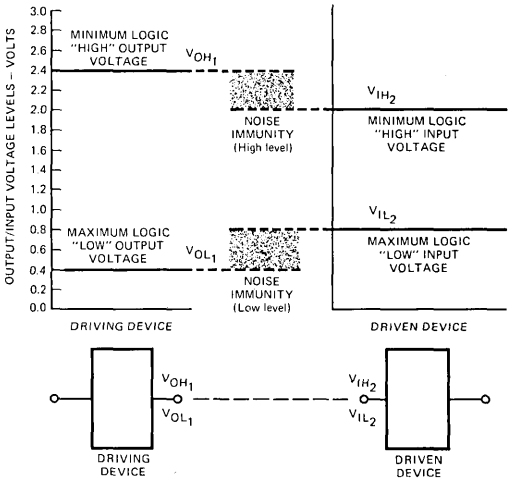
Am9322 LOADING RULES (in unit loads)

Input/Output	Pin Nos.	Input Load	Output Drive HIGH	LOW
S	1	1	—	—
I_{0a}	2	1	—	—
I_{Ia}	3	1	—	—
Z_a	4	—	20	10
I_{0b}	5	1	—	—
I_{Ib}	6	1	—	—
Z_b	7	—	20	10
GND	8	—	—	—
Z_d	9	—	20	10
I_{Id}	10	1	—	—
I_{0d}	11	1	—	—
Z_c	12	—	20	10
I_{Ic}	13	1	—	—
I_{0c}	14	1	—	—
$\overline{E}$	15	1	—	—
V_{CC}	16	—	—	—

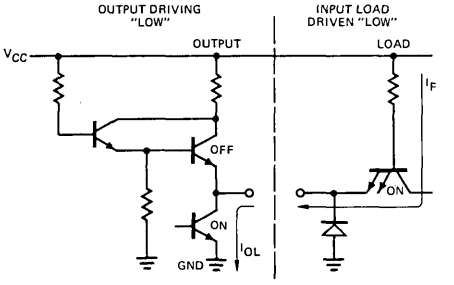
TABLE II

INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH



Current Interface Conditions — LOW



Current Interface Conditions — HIGH

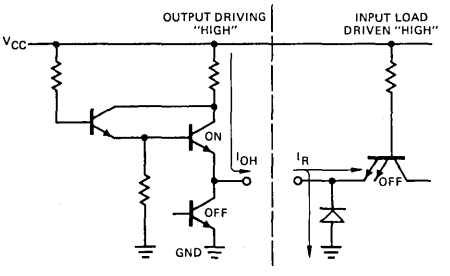
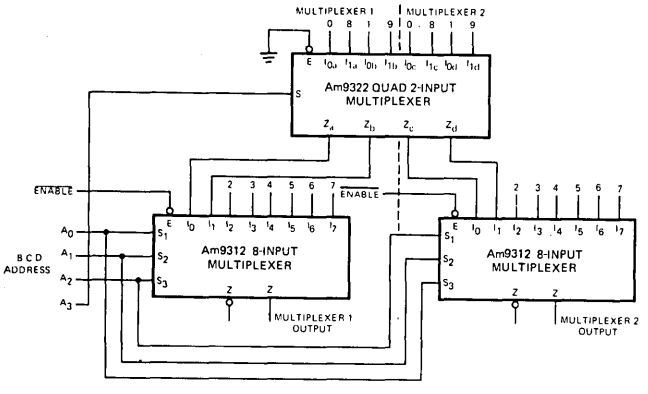


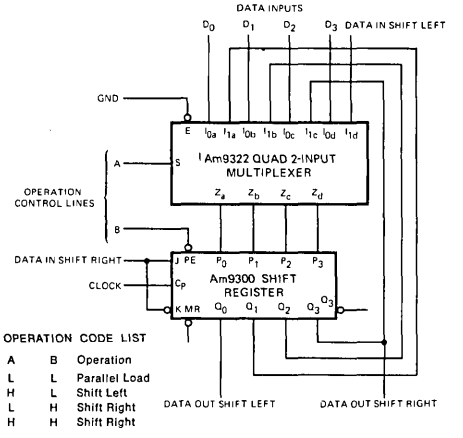
Figure 5

Am9322 APPLICATIONS



Dual 10-Input Multiplexer
Two 10-input Multiplexers are shown above with the select lines common to the two multiplexers. Inputs are selected by an 8421 BCD Address.

Figure 6

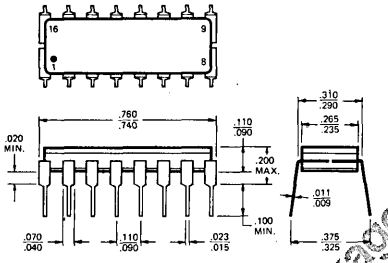


Shift Left, Shift Right, Parallel Load Register
This register will shift left, shift right, and load 4 bits of parallel data according to the operation code applied to A and B.

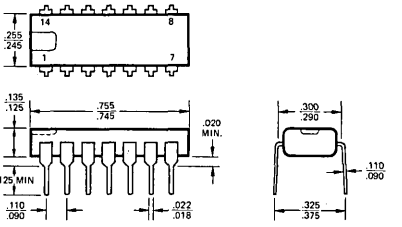
Figure 7

PHYSICAL DIMENSIONS
Dual-In-Line

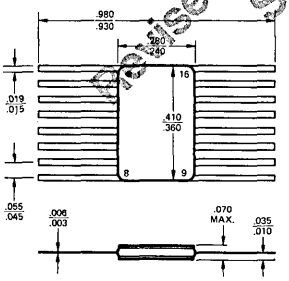
Hermetic



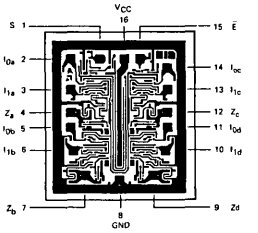
Molded



Flat Package



Metallization and Pad Layout
60 x 69 Mils



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Am93L22
Low-Power Quad Two-Input Multiplexer

Distinctive Characteristics

- 45 mw typical power dissipation.
- 31 ns typical propagation delay.
- 100% reliability assurance testing in compliance with MIL STD 883
- Guaranteed fan-out of three with standard TTL circuits

FUNCTIONAL DESCRIPTION

The Am93L22 Quad Two-Input Multiplexer is the logic implementation of a four-pole two-position switch with the position of the switch set by the logic level supplied to the select input. An active LOW enable is provided. The logic equations describing the device are given below.

$$Z_a = E\,(I_{0a}\overline{S} + I_{1a}S) \qquad Z_c = E\,(I_{0c}\overline{S} + I_{1c}S)$$
$$Z_b = E\,(I_{0b}\overline{S} + I_{1b}S) \qquad Z_d = E\,(I_{0d}\overline{S} + I_{1d}S)$$

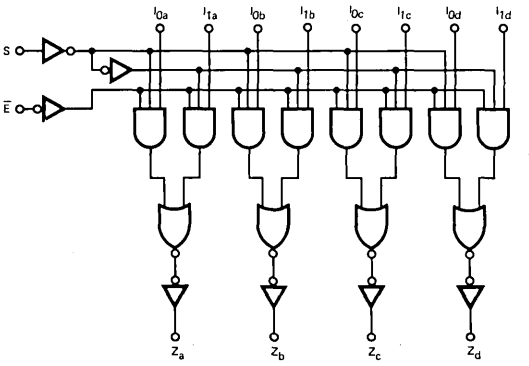
The Am93L22 is useful for data bussing and general logic design.

TRUTH TABLE

Enable	Select Input	Data Inputs		Output
$\overline{E}$	S	I_{0i}	I_{1i}	Z_i
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level X = Don't Care
L = LOW Voltage Level i = a, b, c, d

LOGIC DIAGRAM



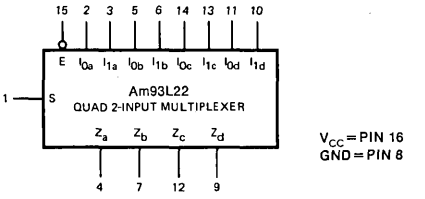
LOADING RULES

In Unit Loads (Notes)

	TTL LOADS		93L LOADS	
Input Load Factor	HIGH	LOW	HIGH	LOW
All inputs	0.5	0.25	1.0	1.0
Output Drive	HIGH	LOW	HIGH	LOW
All Outputs	10	3	20	12

NOTES:
1) A TTL unit load is specified as 0.4 V at −1.6 mA LOW, 2.4 V at 40 μA HIGH.
2) A 93L unit load is specified as 0.3 V at −400 μA LOW, 2.4 V at 20 μA HIGH.
3) Enough output LOW current is available to mix TTL and 93L loads and still meet the 93L requirement of a V_{OL} of 0.3 V.

LOGIC SYMBOL



Am93L22 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
16-Pin Molded DIP	0°C to +75°C	U6M93L2259X
16 Pin Hermetic DIP	0°C to +75°C	U7B93L2259X
16-Pin Hermetic DIP	−55°C to +125°C	U7B93L2251X
16-Pin Hermetic Flat Pak	−55°C to +125°C	U4L93L2251X
Dice	Note	UXX93L22XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current (Note 1)	−30 mA to +5.0 mA

Note 1. Maximum current defined by DC input voltage.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93L2259X $T_A = 0°C$ to $+75°C$ $V_{CC} = 4.75$ V to 5.25 V
Am93L2251X $T_A = -55°C$ to $+125°C$ $V_{CC} = 4.50$ V to 5.50 V

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -0.4$ mA $V_{IN} = V_{IH}$ or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $I_{OL} = 4.92$ mA $V_{IN} = V_{IH}$ or V_{IL}		0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all ihputs			0.7	Volts
I_{IL} (Note 2)	93L Unit Load Input LOW Current	$V_{CC} = MAX.$, $V_{IN} = 0.3$ V		−0.25	−0.4	mA
I_{IH} (Note 2)	93L Unit Load Input HIGH Current	$V_{CC} = MAX.$, $V_{IN} = 2.4$ V		2.0	20	μA
	Input HIGH Current	$V_{CC} = MAX.$, $V_{IN} = 5.5$ V			1.0	mA
I_{SC}	Output Short Circuit Current	$V_{CC} = MAX.$, $V_{OUT} = 0.0$ V	−10	−21	−40	mA
I_{CC}	Power Supply Current	$V_{CC} = MAX.$		9.0	13.2	mA

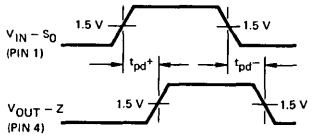
Notes: 1) Typical limits are at $V_{CC} = 5.0$ V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by the 93L input load factor. (See loading rules)

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

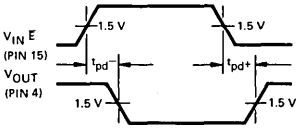
Parameters	Description		Test Conditions	Min.	Typ.	Max.	Units
$t_{pd+}(S)$	Turn Off Delay	Select Input/Output	$V_{CC} = 5.0$ V, $C_L = 15$ pF	12	24	36	ns
$t_{pd-}(S)$	Turn On Delay	Select Input/Output		17	33	49	ns
$t_{pd+}(D)$	Turn Off Delay	Data Input/Output		9	17	25	ns
$t_{pd-}(D)$	Turn On Delay	Data Input/Output		11	21	31	ns
$t_{pd+}(\overline{E})$	Turn Off Delay	Enable Input/Output		10	19	29	ns
$t_{pd-}(\overline{E})$	Turn On Delay	Enable Input/Output		14	28	42	ns

SWITCHING TIME WAVEFORMS

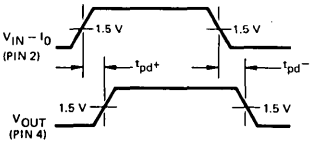
t_{pd}; S to Z_a
CONDITIONS
Pins 2, 15 = GND.
Pin 3 = V_{CC}



t_{pd}; $\overline{E}$ to Z_a
CONDITIONS
All Other Inputs High



t_{pd}; I_{0a} to Z_a
CONDITIONS
Pins 1, 15 = GND.



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Am9324
Five-Bit Comparator

Distinctive Characteristics:

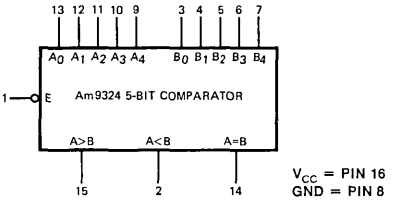
- Compares two 5-bit binary words and provides separate outputs: A > B, A = B, A < B
- Active LOW enable input controls all outputs
- Can be connected in series or parallel with additional comparators for comparing long words
- 100% reliability assurance testing in compliance with MIL-STD-883
- Electrically tested and optically inspected die for the assemblers of hybrid products
- Mixing privileges for obtaining price discounts. Refer to price list

FUNCTIONAL DESCRIPTION

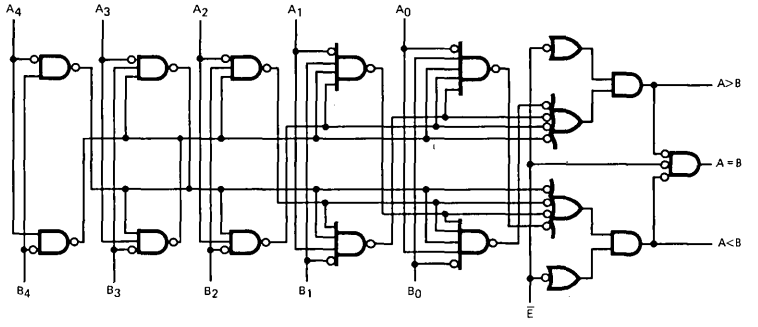
The Am9324 is a high-speed expandable comparator which compares two 5-bit words, A and B, and gives outputs of "A greater than B," "A equal to B" and "A less than B." An active LOW enable is provided which forces the three outputs LOW when the enable goes HIGH.

Comparators can be connected in series or parallel to obtain comparison over large word lengths. For series connection the A > B and A < B outputs are connected to the least significant A_0 and B_0 inputs of the next most significant comparator. Parallel connection uses the same number of devices as the series method and is considerably faster when comparing over large word lengths. Parallel connection is accomplished by comparing the A > B, A < B outputs of several comparators by additional comparators as shown in Figure 8.

LOGIC SYMBOL



LOGIC DIAGRAM

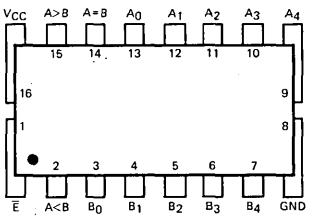


Am9324 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	U6M932459X
Hermetic DIP	0°C to +75°C	U7B932459X
Hermetic DIP	−55°C to +125°C	U7B932451X
Hermetic Flat Pak	−55°C to +125°C	U4L932451X
Dice	Note	UXX9324XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to + 125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current	−30mA to + 5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am932459X T_A = 0°C to +75°C V_{CC} = 5.0 V ±5%
Am932451X T_A = −55°C to +125°C V_{CC} = 5.0 V ±10%

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.8 mA V_{IN} = V_{IH} or V_{IL}		2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16.0 mA V_{IN} = V_{IH} or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL}	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V			−1.0	−1.6	mA
I_{IH}	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V			4.0	40	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V		−20	−25	−60	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. All Inputs HIGH	Am932451X		39	64	mA
			Am932459X		39	69	mA

Notes: 1) Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by input load factor (see Loading Rules).

Switching Characteristics (T_A = 25°C)

Parameters	Description		Test Conditions	Min	Typ	Max	Units
t_{pd+} ($\overline{E}$-A = B)	Turn Off Delay	Enable Input to A = B Output	V_{CC} = 5.0 V, C_L = 15 pF Refer to Figure 1		11	17	ns
t_{pd-} ($\overline{E}$-A = B)	Turn On Delay	Enable Input to A = B Output			11	17	ns
t_{pd+} ($\overline{E}$-A ≠ B)	Turn Off Delay	Enable to A ≠ B Output	V_{CC} = 5.0 V, C_L = 15 pF		10	16	ns
t_{pd-} ($\overline{E}$-A ≠ B)	Turn On Delay	Enable to A ≠ B Output			10	16	ns
t_{pd+} (A_2-A>B)	Turn Off Delay	A_2 Input to A > B Output	V_{CC} = 5.0 V, C_L = 15 pF Refer to Figure 2		17	25	ns
t_{pd-} (A_2-A>B)	Turn On Delay	A_2 Input to A > B Output			16	24	ns
t_{pd+} (A_2-A<B)	Turn Off Delay	A_2 Input to A < B Output	V_{CC} = 5.0 V, C_L = 15 pF Refer to Figure 3		21	31	ns
t_{pd-} (A_2-A<B)	Turn On Delay	A_2 Input to A < B Output			22	33	ns
t_{pd+} (A_2 or B_2	Turn Off Delay	Any Input to A = B Output	V_{CC} = 5.0 V, C_L = 15 pF Refer to Figure 4		30	45	ns
t_{pd-} to A=B)	Turn On Delay	Any Input to A = B Output			26	40	ns
t_{pd+} (A_4 or B_4	Turn Off Delay	Any Input to A<B Output	V_{CC} = 5.0 V, C_L = 15 pF Refer to Fig. 5 which shows input-output pins & conditions for worst case maximum propagation delay.		29	44	ns
t_{pd-} to A <B)	Turn On Delay	Any Input to A<B Output			33	49	ns
t_{pd+} (A_4 or B_4	Turn Off Delay	Any Input to A>B Output			29	44	ns
t_{pd-} to A >B)	Turn On Delay	Any Input to A>B Output			33	49	ns

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH-signal level or when used with V_{CC} to indicate HIGH V_{CC} value.

I Input.

L LOW, applying to a LOW signal level or when used with V_{CC} to indicate LOW V_{CC} value.

O Output.

FUNCTIONAL TERMS:

A > B Output HIGH when the A word is greater than the B word.

A < B Output HIGH when the A word is less than the B word.

A = B Output HIGH when the A word is the same as the B word.

A_i Data A inputs $i = 0, 1, 2, 3, 4$

B_i Data B inputs $i = 0, 1, 2, 3, 4$

$\overline{E}$ Active LOW Enable Input, all outputs are LOW when enable is HIGH.

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

Input Unit Load One T^2L gate input load. In the HIGH state it is equal to I_{IH} and in the LOW state it is equal to I_{IL}.

OPERATIONAL TERMS:

I_{IL} Forward input load current, for unit input load.

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{PD} The current drawn by the device under a +5.0 V power supply bias with input and output terminals open.

I_{IH} Reverse input load current with V_{OH} applied to input.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage. Refer to figure 5.

V_{IL} Maximum logic LOW input voltage. Refer to figure 5.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

SWITCHING TERMS: (All switching times are measured at the 1.5 V logic level).

t_{pd+} (A_i or B_i – A < B) The propagation delay from a transition on any A or B input to the A < B LOW to HIGH transition.

t_{pd-} (A_i or B_i – A < B) The propagation delay from a transition on any A or B input to the A < B HIGH to LOW transition.

t_{pd+}($\overline{E}$–A ≠ B) The propagation delay from HIGH to LOW Enable input transition to A > B (or B > A) output LOW to HIGH transition.

t_{pd-}($\overline{E}$–A ≠ B) The propagation delay from LOW to HIGH Enable input transition to A > B (or B > A) output HIGH to LOW transition.

t_{pd+} ($\overline{E}$–A = B) The propagation delay from a HIGH to LOW Enable input transition to the A = B output LOW to HIGH transition.

t_{pd-} ($\overline{E}$–A = B) The propagation delay from a LOW to HIGH Enable input transition to the A = B output HIGH to LOW transition.

t_{pd+} (A_4–A > B) The propagation delay from a LOW to HIGH A_4 input transition to the A > B output LOW to HIGH transition.

t_{pd-} (A_4–A < B) The propagation delay from a LOW to HIGH A_4 input transition to the A < B output HIGH to LOW transition.

t_{pd+} (A_2–A > B) The propagation delay from a LOW to HIGH A_2 input transition to the LOW to HIGH A > B output transition.

t_{pd-} (A_2–A > B) The propagation delay from a HIGH to LOW A_2 input transition to the HIGH to LOW A > B output transition.

t_{pd+} (A_2–A < B) The propagation delay from a HIGH to LOW A_2 input transition to a LOW to HIGH A < B output transition.

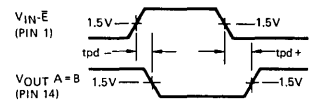
t_{pd-} (A_2–A < B) The propagation delay from a LOW to HIGH A_2 input transition to the HIGH to LOW A < B output transition.

t_{pd+} (A_i–A = B) The propagation delay from any input transition to the LOW to HIGH A = B output transition.

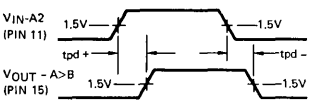
t_{pd-} (A_i–A = B) The propagation delay from any input transition to the HIGH to LOW A = B output transition.

SWITCHING TIME WAVEFORMS

All inputs and outputs loaded with 15 pF capacitance only. Output capacitance is referred to as C_L.

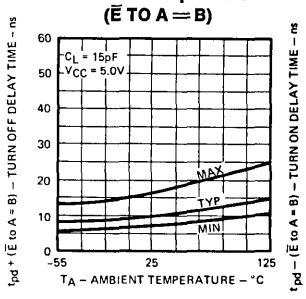


t_{pd}: $\bar{E}$ to A = B
Conditions
All other inputs high



t_{pd}: A_2 to A > B
Conditions
Pin 1, 5 = GND
All other inputs high

Turn Off Delay Time Versus Ambient Temperature ($\bar{E}$ TO A = B)



Turn On Delay Time Versus Ambient Temperature ($\bar{E}$ TO A = B)

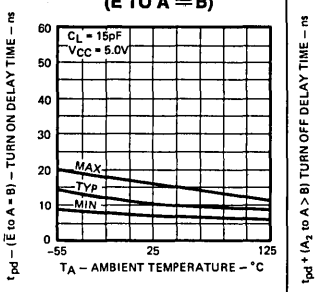
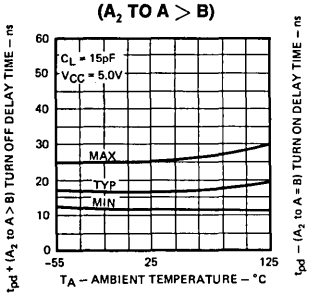


Figure 1

Turn Off Delay Time Versus Ambient Temperature (A_2 TO A > B)



Turn On Delay Time Versus Ambient Temperature (A_2 TO A > B)

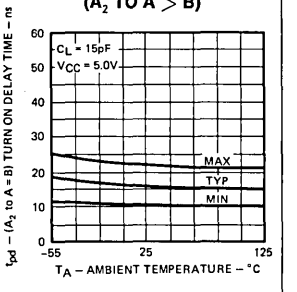
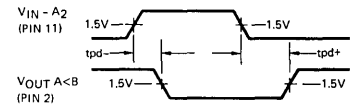
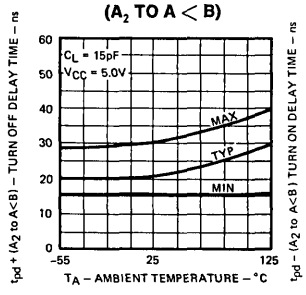


Figure 2



t_{pd}: A_2 to A < B
Conditions
Pin 1 = GND
All other inputs high

Turn Off Delay Time Versus Ambient Temperature (A_2 TO A < B)



Turn On Delay Time Versus Ambient Temperature (A_2 TO A < B)

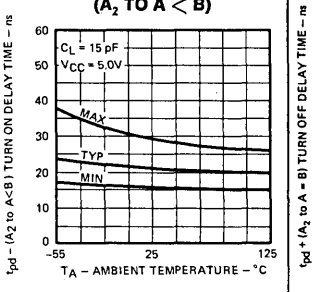
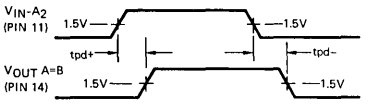
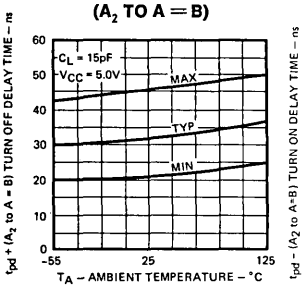


Figure 3



t_{pd}: A_2 to A = B
Conditions
Pin 1 = GND
All other inputs high

Turn Off Delay Time Versus Ambient Temperature (A_2 TO A = B)



Turn On Delay Time Versus Ambient Temperature (A_2 TO A = B)

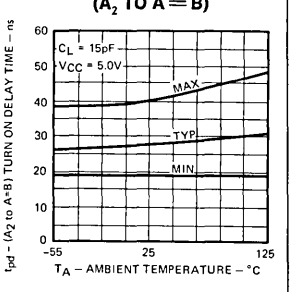
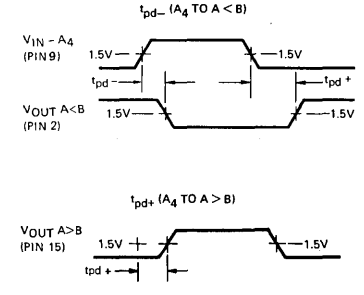


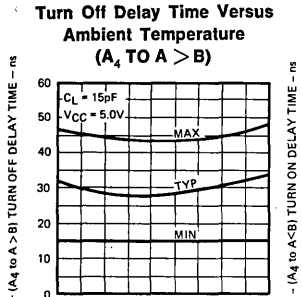
Figure 4



Conditions
Pin 1, 6, 11, 12, 13 = GND

All other inputs high

Turn Off Delay Time Versus Ambient Temperature (A_4 TO A > B)



Turn On Delay Time Versus Ambient Temperature (A_4 TO A < B)

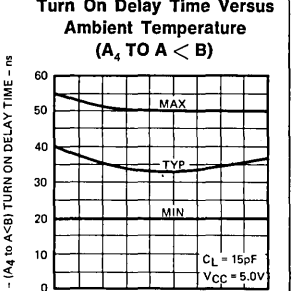


Figure 5

TRUTH TABLE

Inputs		Outputs		
Data	$\overline{E}$	A > B	A = B	A < B
X	H	L	L	L
A > B	L	H	L	L
A = B	L	L	H	L
A < B	L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Table I

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 54/7400	1	1
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Table II

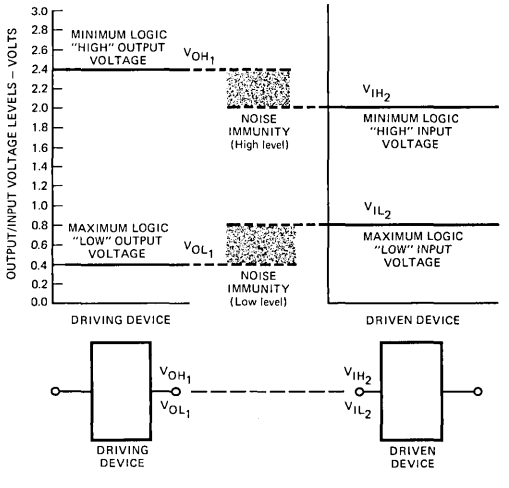
Am9324 LOADING RULES (in unit loads)

Input/Output	Pin No.'s	Input Load	Output Drive HIGH	LOW
$\overline{E}$	1	2	—	—
A < B	2	—	18	9
B_0	3	2	—	—
B_1	4	2	—	—
B_2	5	2	—	—
B_3	6	2	—	—
B_4	7	2	—	—
GND	8	—	—	—
A_4	9	2	—	—
A_3	10	2	—	—
A_2	11	2	—	—
A_1	12	2	—	—
A_0	13	2	—	—
A = B	14	—	20	10
A > B	15	—	20	10
V_{CC}	16	—	—	—

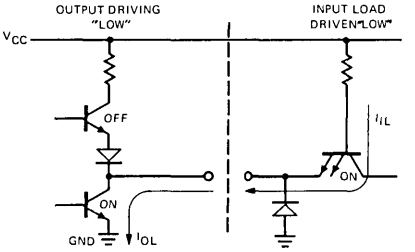
Table III

INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH



Current Interface Conditions — LOW



Current Interface Conditions — HIGH

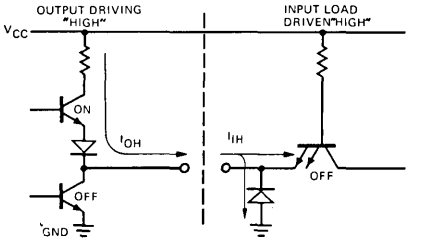
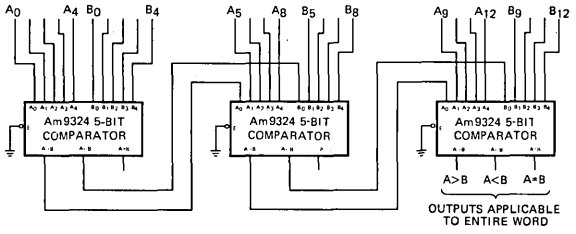


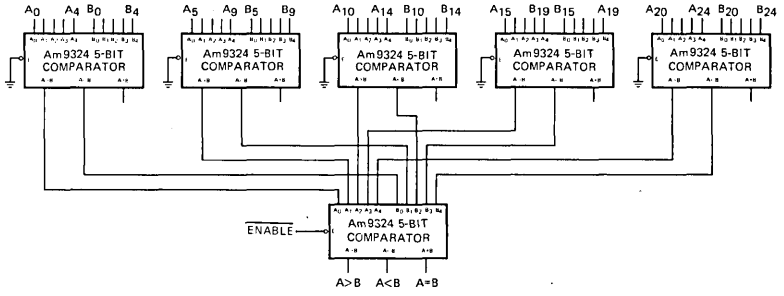
Figure 6

Am9324 APPLICATIONS



SERIAL EXPANSION

Figure 7



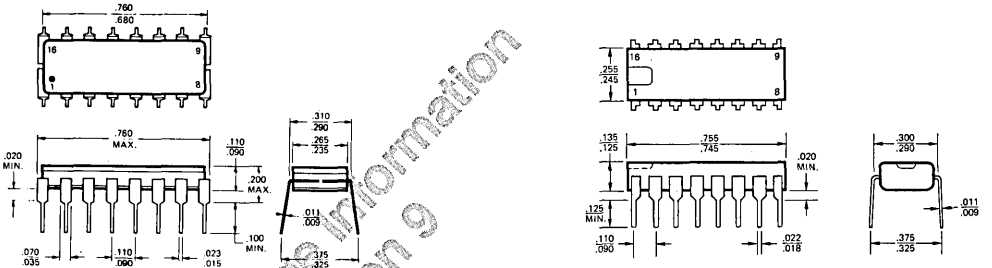
PARALLEL EXPANSION

This method of expansion is much faster than the serial method for large word lengths and uses the same number of packages.

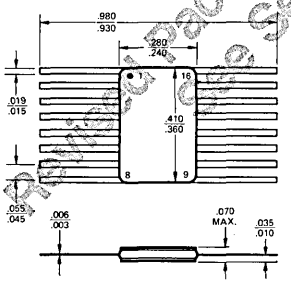
Figure 8

PHYSICAL DIMENSIONS

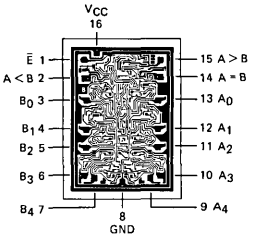
Hermetic — **Dual-In-Line** — **Molded**



Flat Package



Metallization and Pad Layout



72 x 99 Mils

ADVANCED MICRO DEVICES INC.
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Am93L24
Low-Power Five-Bit Comparator

Distinctive Characteristics

- 68 ns typical compare time.
- 52 mw typical power dissipation.
- 100% reliability assurance testing in compliance with MIL STD 883

FUNCTIONAL DESCRIPTION

The Am93L24 is a high-speed expandable comparator which compares two 5-bit words, A and B, and gives outputs of "A greater than B," "A equal to B" and "A less than B." An active LOW enable is provided which forces the three outputs LOW when the enable goes HIGH.

Comparators can be connected in series or parallel to obtain comparison over large word lengths. For series connection the $A > B$ and $A < B$ outputs are connected to the least significant A_0 and B_0 inputs of the next most significant comparator. Parallel connection uses the same number of devices as the series method and is considerably faster when comparing over large word lengths. Parallel connection is accomplished by comparing the $A > B$, $A < B$ outputs of several comparators by additional comparators.

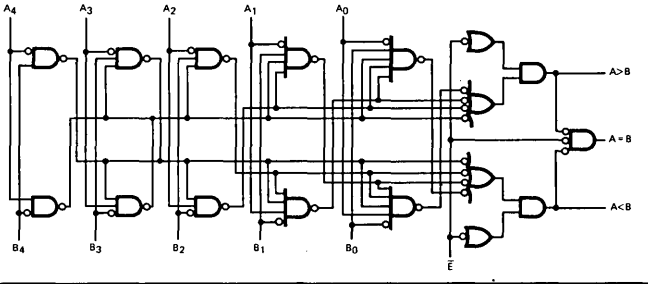
TRUTH TABLE

Inputs		Outputs		
Data	$\overline{E}$	$A > B$	$A = B$	$A < B$
X	H	L	L	L
$A > B$	L	H	L	L
$A = B$	L	L	H	L
$A < B$	L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Table I

LOGIC DIAGRAM



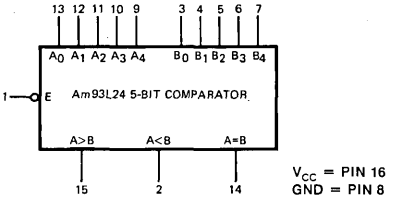
LOADING RULES

In Unit Loads (Notes)

	TTL LOADS		93L LOADS	
Input Load Factor	HIGH	LOW	HIGH	LOW
All inputs	1.0	0.5	2.0	2.0
Output Drive	HIGH	LOW	HIGH	LOW
$A > B$, $A < B$	10	3	20	12
$A = B$	9	3	18	12

NOTES:
1) A TTL unit load is specified as 0.4 V at −1.6 mA LOW, 2.4 V at 40 μA HIGH.
2) A 93L unit load is specified as 0.3 V at −400 μA LOW, 2.4 V at 20 μA HIGH.
3) Enough output LOW current is available to mix TTL and 93L loads and still meet the 93L requirement of a V_{OL} of 0.3 V.

LOGIC SYMBOL



Am93L24 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
16-Pin Molded DIP	0°C to +75°C	U6M93L2459X
16-Pin Hermetic DIP	0°C to +75°C	U7B93L2459X
16-Pin Hermetic DIP	−55°C to +125°C	U7B93L2451X
16-Pin Hermetic Flat Pak	−55°C to +125°C	U4L93L2451X
Dice	Note	UXX93L24XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to $+V_{CC}$ max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current (Note 1)	−30 mA to +5.0 mA

Note 1. Maximum current defined by DC input voltage.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93L2459X $T_A = 0°C$ to $+75°C$ $V_{CC} = 4.75$ V to 5.25 V
Am93L2451X $T_A = -55°C$ to $+125°C$ $V_{CC} = 4.50$ V to 5.50 V

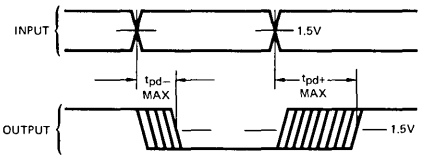
Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -0.4$ mA $V_{IN} = V_{IH}$ or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $I_{OL} = 4.92$ mA $V_{IN} = V_{IH}$ or V_{IL}		0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.7	Volts
I_{IL} (Note 2)	93L Unit Load Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.3$ V		−0.25	−0.4	mA
I_{IH} (Note 2)	93L Unit Load Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.4$ V		2.0	20	μA
	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 5.5$ V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., $V_{OUT} = 0.0$ V	−2.5		−25	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		10.4	21	mA

Notes: 1) Typical limits are at $V_{CC} = 5.0$ V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by the 93L input load factor. (See loading rules)

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

Parameters	Description		Test Conditions	Min	Typ	Max	Units
$t_{pd+}(\overline{E}\text{-}A = B)$	Turn Off Delay	Enable Input to A = B Output	$V_{CC} = 5.0$ V, $C_L = 15$ pF	10	21	32	ns
$t_{pd-}(\overline{E}\text{-}A = B)$	Turn On Delay	Enable Input to A = B Output		15	30	45	ns
$t_{pd+}(\overline{E}\text{-}A \neq B)$	Turn Off Delay	Enable to A < B and A > B	$V_{CC} = 5.0$ V, $C_L = 15$ pF	15	20	30	ns
$t_{pd-}(\overline{E}\text{-}A \neq B)$	Turn On Delay	Enable to A < B and A > B		12	24	36	ns
$t_{pd+}(A_2\text{-}A>B)$	Turn Off Delay	A_2 Input to A > B Output	$V_{CC} = 5.0$ V, $C_L = 15$ pF	18	36	54	ns
$t_{pd-}(A_2\text{-}A>B)$	Turn On Delay	A_2 Input to A > B Output		22	43	65	ns
$t_{pd+}(A_2\text{-}A<B)$	Turn Off Delay	A_2 Input to A < B Output	$V_{CC} = 5.0$ V, $C_L = 15$ pF	22	44	66	ns
$t_{pd-}(A_2\text{-}A<B)$	Turn On Delay	A_2 Input to A < B Output		25	49	74	ns
$t_{pd+}(A_2\text{-}A=B)$	Turn Off Delay	A_2 Input to A = B Output	$V_{CC} = 5.0$ V, $C_L = 15$ pF	34	68	102	ns
$t_{pd-}(A_2\text{-}A=B)$	Turn On Delay	A_2 Input to A = B Output		26	51	76	ns
t_{pd+} (A_4 or B_4) to A < B	Turn Off Delay	Any Input to A<B Output	Worst case maximum propagation delay.	23	45	67	ns
t_{pd-} to A < B	Turn On Delay	Any Input to A<B Output		34	67	90	ns
t_{pd+} (A_4 or B_4) to A > B	Turn Off Delay	Any Input to A>B Output		27	54	80	ns
t_{pd-} to A > B	Turn On Delay	Any Input to A>B Output		28	56	84	ns

SWITCHING TIME WAVEFORMS



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Am9328
Dual 8-Bit Shift Register

Distinctive Characteristics:

- 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and package hermeticity testing in compliance with MIL-STD-883.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

The Am9328 low-power dual 8-bit shift register provides 16 bits of high-speed serial storage in two identical shift registers, each consisting of 8 master slave RS flip-flops.

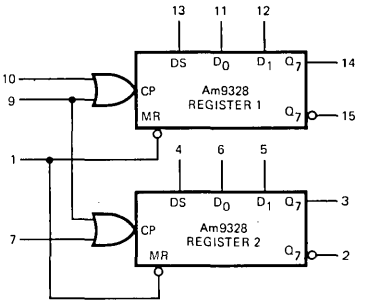
Data to each register is selected from one of two sources, D_0 and D_1, by a two input multiplexer controlled by DS (data select). When DS is HIGH, data is entered from the D_1 input; when DS is LOW data is entered from the D_0 input.

The two shift registers have separate clock inputs and a common clock input. The common clock is OR'ed with the separate clock inputs, so that for each register one clock input can be used as a clock line and the other as an active LOW shift enable. The registers can then be operated with a common clock and independent shift enables or with independent clocks and a common shift enable.

Data is entered into the masters of the flip-flops while the clock is LOW. During the clock pulse LOW-to-HIGH transition the masters are inhibited from further change, and the data is transferred to the slaves. As long as the clock is HIGH, the masters cannot change and the slaves are connected to the masters. When the clock goes from HIGH to LOW, the slaves are inhibited from changing and new data is entered into the masters.

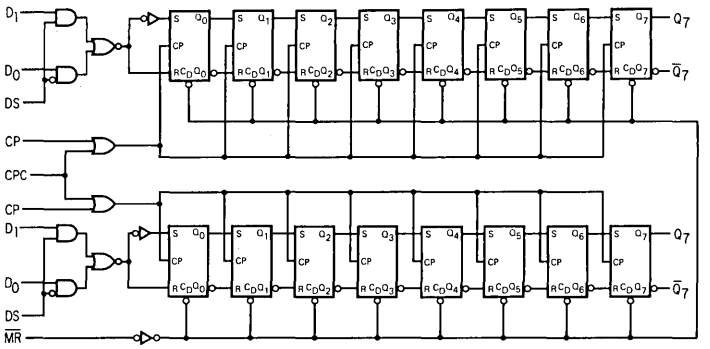
An asynchronous active LOW master reset ($\overline{MR}$) resets all 16 bits of shift register to the "0" state independent of any other inputs to the device.

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

LOGIC DIAGRAM

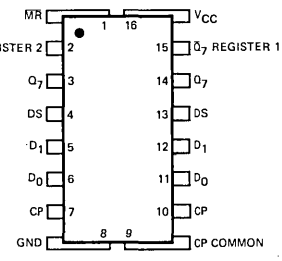


Am9328 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	U6M932859X
Hermetic DIP	0°C to +75°C	U7B932859X
Hermetic DIP	−55°C to +125°C	U7B932851X
Hermetic Flat Pak	−55°C to +125°C	U4L932851X
Dice	Note	UXX9328XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: Pin 1 is marked for orientation

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°
Temperature (Ambient) Under Bias	−55°C to +125°
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} ma
DC Input Voltage	−0.5 V to +5.5
Output Current, Into Outputs	30 m
DC Input Current	−30 mA to + 5.0m

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am932859X T_A = 0°C to +75°C V_{CC} = 5.0 V ±5%
Am932851X T_A = −55°C to +125°C V_{CC} = 5.0 V ±10%

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.8 mA V_{IN} = V_{IH} or V_{IL}		2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16.0 mA V_{IN} = V_{IH} or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V			−1.0	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V			6.0	40	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V		−20		−70	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.	932851X		60	77	mA
			932859X		60	88	

Notes: 1) Typical Limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by input load factor (See Loading Rules).

SWITCHING CHARACTERISTICS (T_A = 25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{pd+}	Turn Off Delay (Q_7, $\overline{Q_7}$)	V_{CC} = 5.0 V C_L = 15 pF	8	13	23	ns
t_{pd-}	Turn On Delay (Q_7, $\overline{Q_7}$)		14	22	39	ns
t_{pd-} ($\overline{MR}$)	Turn On Delay ($\overline{MR}$ to Q_7)			35	66	ns
CP_{pw}	Min. Clock LOW Pulse Width			14	22	ns
$\overline{MR}_{pw}$(CPH)	Min. Reset Pulse Width with CP HIGH			20	30	ns
$\overline{MR}_{pw}$(CPL)	Min. Reset Pulse Width with CP LOW			28	40	ns
t_s (D_0, D_1)	Data Set-up Time		0		16	ns
t_s (DS)	Set-up Time, Select Input		0		16	ns
f_s	Shift Frequency		20	30		MHz

EFINITION OF TERMS

JBSCRIPT TERMS:

Forward, applying to LOW inputs.

HIGH, applying to a HIGH logic level or when used with V_{CC} indicate high V_{CC} value.

Input.

LOW, applying to LOW logic level or when used with V_{CC} to dicate low V_{CC} value.

Output.

Reverse, applying to HIGH inputs.

INCTIONAL TERMS:

, Input Asynchronous direct clear input.

› Clock Pulse. The subscript, if any, to pulse waveshape.

›C The clock input common to the two shift registers.

in-Out The logic HIGH or LOW output drive capability in terms Input Unit Loads.

put Unit Load One T^2L gate input load. In the HIGH state it is jual to I_R and in the LOW state it is equal to I_F.

; FLIP FLOP Flip Flop which sets when S input is HIGH and R ɔut is LOW and is reset when S is LOW and R is HIGH. R=S= GH is undefined.

The D input to the 8 bit shift register selected when DS is LOW.

The D input to the 8 bit shift register selected when DS is HIGH.

; The input select control which determines whether data on D_0 D_1 enters the shift register.

$\overline{R}$ The common asychronous active LOW master reset input.

, The true output of the last stage of a shift register.

, The false output of the last stage of a shift register.

OPERATIONAL TERMS:

I_{IL} Forward input load current, for unit input load.

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{CC} The current drawn by the device with input and output terminals open.

I_{IH} Reverse input load current with V_{OH} applied to input.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage. Refer to figure 4.

V_{IL} Maximum logic LOW input voltage. Refer to figure 4.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

SWITCHING TERMS: (All switching times are measured at the 1.5 V logic level)

CP_{pw} The minimum clock pulse width required for proper register operation.

f_s The shift frequency of the register.

$\overline{MR}_{pw}$ The minimum pulse width for resetting the register flip-flops.

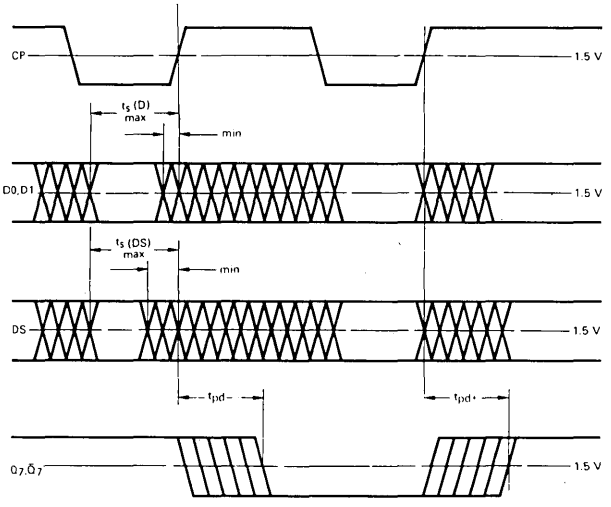
t_{pd-} The propagation delay from the clock signal LOW-HIGH transition to an output signal HIGH-LOW transition. Refer to Figure 1.

t_{pd+} The propagation delay from the clock signal LOW-HIGH transition to an output signal LOW-HIGH transition. Refer to Figure 1.

$t_{pd-}(\overline{MR})$ The propagation delay from the master reset signal HIGH-LOW transition to the TRUE output signal HIGH-LOW transition.

t_s Set-up time defined as the minimum time required for the logic level to be present at the data inputs prior to the clock transition from LOW to HIGH in order for the flip flop(s) to respond.

SWITCHING TIME WAVEFORMS



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
▨	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
▨	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
▨	DON'T CARE, ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN

Note: The "set-up time" is defined as the time required, relative to the clock, for a LOW to HIGH edge (tsH) or a HIGH to LOW edge (tsL) to propagate through internal delays. Logic transitions occurring before ts max are guaranteed to be detected; those occurring after ts min. are guaranteed not to be detected. Transitions between ts max and ts min. may or may not be detected. The minimum set up time for a LOW is sometimes called the "release time" for a HIGH.

TRUTH TABLE

Shift Selection

DS	D_0	D_1	$Q_0 (t_{n+1})$
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

TABLE I

MSI INTERFACING RULES

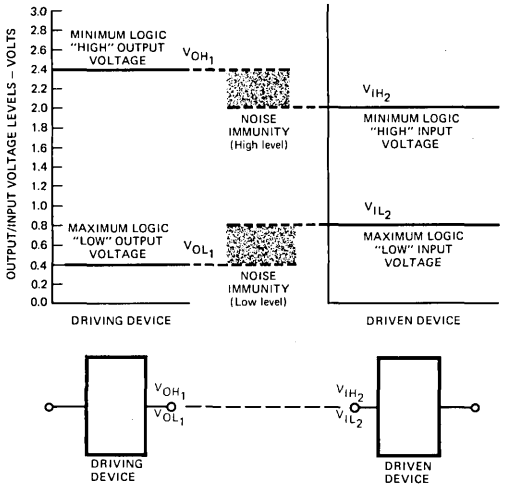
Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Am 9328 LOADING RULES (in unit loads)

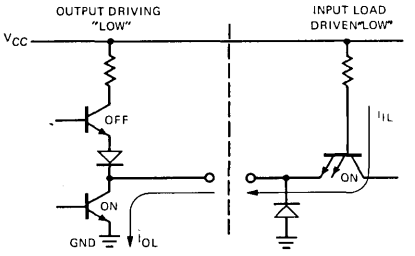
Input/Output		Pin No.'s	Input Load	Output Drive Output HIGH	Output LOW
Common	$\overline{MR}$	1	1	—	—
Register 2	$\overline{Q}_7$	2	—		
	Q_7	3	—		
	DS	4	2	—	—
	D_1	5	1	—	—
	D_0	6	1	—	—
	CP	7	1.5	—	—
GND		8	—	—	—
Common	CP	9	3	—	—
Register 1	CP	10	1.5	—	—
	D_0	11	1	—	—
	D_1	12	1	—	—
	DS	13	2	—	—
	Q_7	14	—	20	10
	$\overline{Q}_7$	15	—	20	10
V_{CC}		16	—	—	—

INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH



Current Interface Conditions — LOW



Current Interface Conditions — HIGH

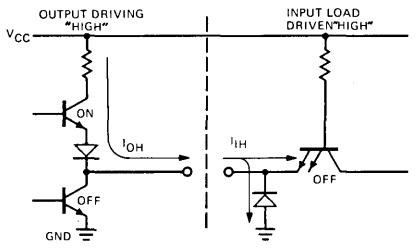
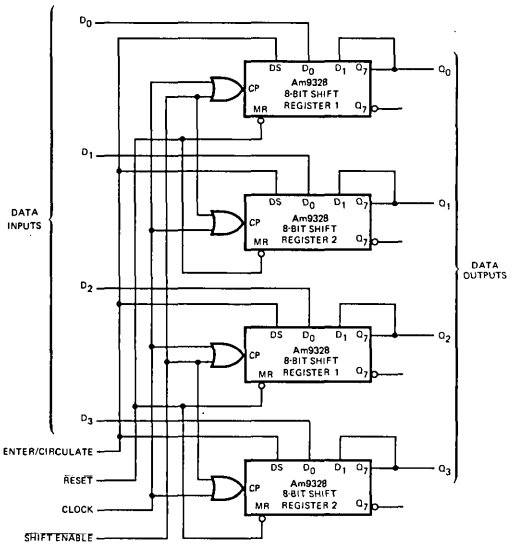


Figure 4

Am9328 APPLICATIONS



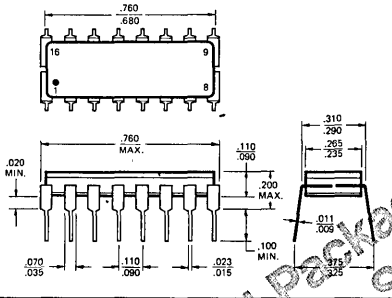
PARALLEL/SERIAL MEMORY

The Am9328 can be used as a high speed parallel/serial memory. Parallel data enters the memory under control of the DS input, acting as an ENTER/CIRCULATE control, and at a later time appears in parallel at the outputs. A typical use for such a memory would be in multiplex display systems where the four parallel outputs represent an 8421 BCD decade of information.

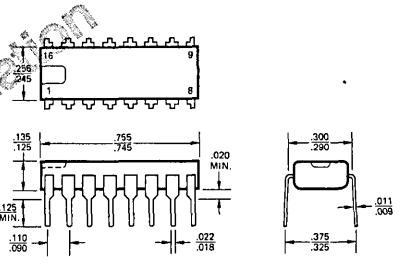
PHYSICAL DIMENSIONS

Dual-In-Line

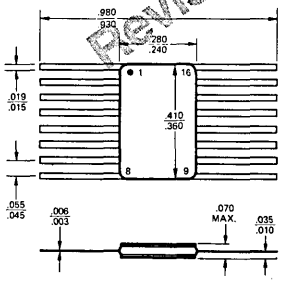
Hermetic



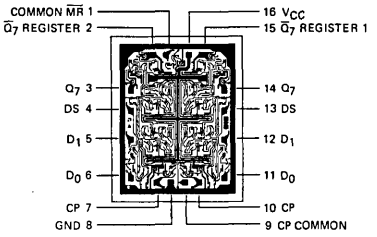
Molded



Flat Package



Metallization and Pad Layout



79 x 102 Mils

ADVANCED MICRO DEVICES INC.
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TELEX: 34-6306

Am93L28
Low-Power Dual 8-Bit Shift Register

Distinctive Characteristics

- 80 mW typical power dissipation
- 16 MHz typical shift frequency
- 100% reliability assurance testing in compliance with MIL STD 883
- Guaranteed fan-out of three with standard TTL circuits

FUNCTIONAL DESCRIPTION

The Am93L28 low-power dual 8-bit shift register provides 16 bits of high-speed serial storage in two identical shift registers, each consisting of 8 master slave RS flip-flops.

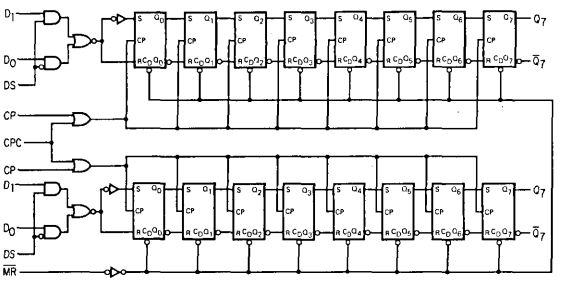
Data to each register is selected from one of two sources, D_0 and D_1, by a two input multiplexer controlled by DS (data select). When DS is HIGH, data is entered from the D_1 input; when DS is LOW data is entered from the D_0 input.

The two shift registers have separate clock inputs and a common clock input. The common clock is OR'ed with the separate clock inputs, so that for each register one clock input can be used as a clock line and the other as an active LOW shift enable. The registers can then be operated with a common clock and independent shift enables or with independent clocks and a common shift enable.

Data is entered into the masters of the flip-flops while the clock is LOW. During the clock pulse LOW-to-HIGH transition the masters are inhibited from further change, and the data is transferred to the slaves. As long as the clock is HIGH, the masters cannot change and the slaves are connected to the masters. When the clock goes from HIGH to LOW, the slaves are inhibited from changing and new data is entered into the masters.

An asynchronous active LOW master reset ($\overline{MR}$) resets all 16 bits of shift register to the "0" state independent of any other inputs to the device.

LOGIC DIAGRAM



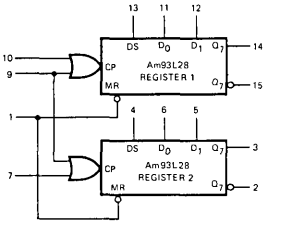
LOADING RULES

In Unit Loads (Notes)

	TTL LOADS		93L LOADS	
Input Load Factor	HIGH	LOW	HIGH	LOW
$\overline{MR}$, D_0, D_1	0.5	0.25	1.0	1.0
Separate CP (Pin 7 & 10)	0.75	0.375	1.5	1.5
D_S	1.0	0.5	2.0	2.0
Common CP (Pin 2)	1.5	0.75	3.0	3.0
Output Drive	HIGH	LOW	HIGH	LOW
Q_7, $\overline{Q}_7$	8	3	16	12

NOTES:
1) A TTL unit load is specified as 0.4 V at −1.6 mA LOW, 2.4 V at 40 μA HIGH.
2) A 93L unit load is specified as 0.3 V at −400 μA LOW, 2.4 V at 20 μA HIGH.
3) Enough output LOW current is available to mix TTL and 93L loads and still meet the 93L requirement of a V_{OL} of 0.3 V.

LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

Am93L28 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
16-pin Molded DIP	0°C to +75°C	U6M93L2859X
16-pin Hermetic DIP	0°C to +75°C	U7B93L2859X
16-pin Hermetic DIP	−55°C to +125°C	U7B93L2851X
16-pin Hermetic Flat Pak	−55°C to +125°C	U4L93L2851X
Dice	Note	UXX93L28XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to $+V_{CC}$ max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current (Note 1)	−30 mA to +5.0 mA

Note 1. Maximum current defined by DC input voltage.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93L2859X $T_A = 0°C$ to $+75°C$ $V_{CC} = 4.75$ V to 5.25 V
Am93L2851X $T_A = -55°C$ to $+125°C$ $V_{CC} = 4.50$ V to 5.50 V

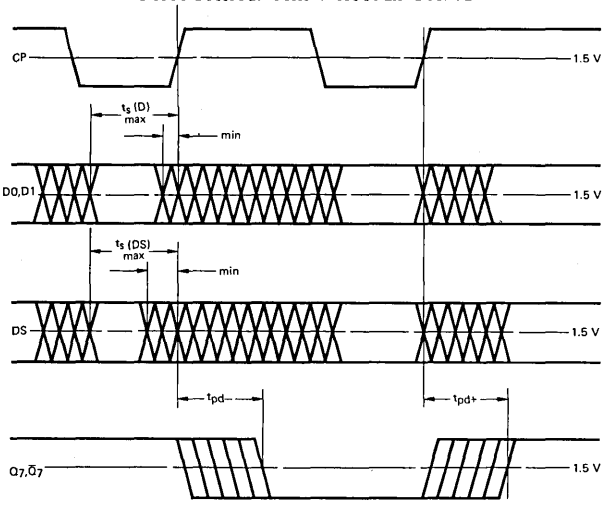
Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -0.32$ mA $V_{IN} = V_{IH}$ or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $I_{OL} = 4.92$ mA $V_{IN} = V_{IH}$ or V_{IL}		0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.7	Volts
I_{IL} (Note 2)	93L Unit Load, Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.3$ V		−0.25	−0.4	mA
I_{IH} (Note 2)	93L Unit Load Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.4$ V		2.0	20	μA
	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 5.5$ V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., $V_{OUT} = 0.0$ V	−2.5	−16	−25	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		16	25.3	mA

Notes: 1) Typical limits are at $V_{CC} = 5.0$ V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by the 93L input load factor. (see loading rules)

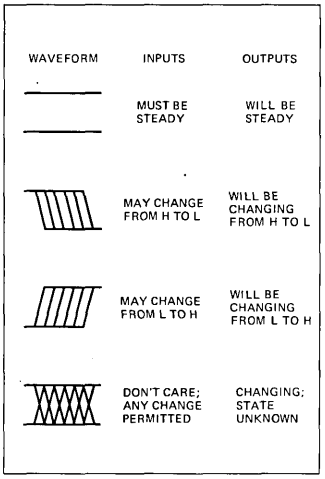
SWITCHING CHARACTERISTICS ($T_A = 25°C$)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{pd+} t_{pd-}	Turn Off Delay (Q_7, $\overline{Q_7}$) Turn On Delay (Q_7, $\overline{Q_7}$)	$V_{CC} = 5.0$ V $C_L = 15$ pF		20 43	45 80	ns ns
$t_{pd-}(\overline{MR})$	Turn On Delay ($\overline{MR}$ to Q_7)			50	110	ns
CP_{pw}	Min. Clock LOW Pulse Width			30	55	ns
$\overline{MR}_{pw}$(CPH)	Min. Reset Pulse Width with CP HIGH			28	60	ns
$\overline{MR}_{pw}$(CPL)	Min. Reset Pulse Width with CP LOW			38	70	ns
t_s (D_0, D_1)	Data Set-up Time		0		30	ns
t_s (DS)	Set-up Time, Select Input		−1		30	ns
f_s	Shift Frequency		10	16		MHz

SWITCHING TIME WAVEFORMS



KEY TO TIMING DIAGRAM



Note: The "set-up Time" is defined as the time required, relative to the clock, for a LOW to HIGH edge (tsH) or a HIGH to LOW edge (tsL) to propagate through internal delays. Logic transitions occurring before ts max are guaranteed to be detected; those occurring after ts min are guaranteed not to be detected. Transitions between ts max and ts min may or may not be detected. The minimum set up time for a LOW is sometimes called the "release time" for a HIGH.

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Am9334

8-Bit Addressable Latch

Distinctive Characteristics

- All eight outputs available
- Serial-to-parallel storage
- Addressable data entry
- Active LOW common clear
- One-of-eight decoder
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

The Am9334 is an 8-bit addressable latch featuring four separate modes of operation. These are: addressable latch, memory, eight-channel demultiplexer and clear. The Am9334 contains eight separate latches with active-LOW common clear and active-LOW input enable on the single data input.

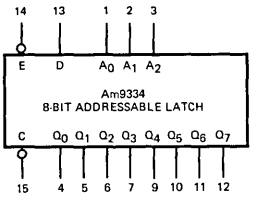
ADDRESSABLE LATCH: When the enable is LOW and the clear is HIGH, the addressed latch output follows the data input. The addressed latch stores the last data input when the enable goes HIGH. The seven non-addressed latches remain unchanged. The three address lines should remain unchanged while the enable is LOW in this mode.

MEMORY: When the enable and clear are HIGH, all eight latches retain their previous state and are unaffected by either the data or address inputs. To avoid transient wrong address codes, this mode should be used while changing the address inputs when operating the Am9334 as an addressable latch.

DEMULTIPLEXER: With the enable and clear both LOW, the addressed latch output follows the data input. The seven non-addressed outputs remain LOW. Thus, when the data input is HIGH, the addressed latch output is uniquely HIGH.

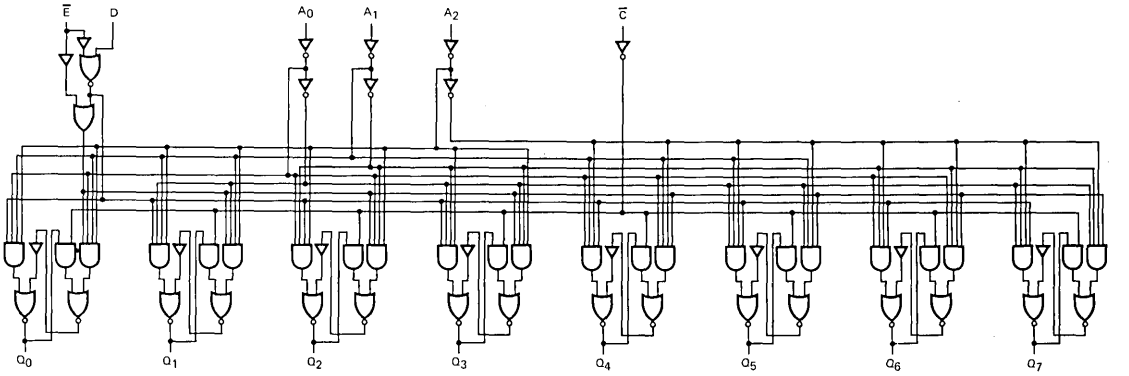
CLEAR: When the enable is HIGH and the clear is brought LOW, all eight latch outputs are forced LOW regardless of other inputs.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

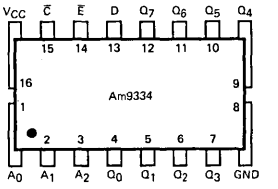
LOGIC DIAGRAM



Am9334 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded Plastic DIP	0°C to +75°C	9334PC
Hermetic DIP	0°C to +75°C	9334DC
Dice	0°C to +75°C	9334XC
Hermetic DIP	−55°C to +125°C	9334DM
Hermetic Flat Pak	−55°C to +125°C	9334FM
Dice	−55°C to +125°C	9334XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am9334XC T_A = 0°C to +75°C V_{CC} = 5.0 V ±5%
Am9334XM T_A = −55°C to +125°C V_{CC} = 5.0 V ±10%

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.72 mA V_{IN} = V_{IH} or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 9.6 mA V_{IN} = V_{IH} or V_{IL}		0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V		−1.0	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V		4.0	40	µA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V	−30	−65	−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		56	86	mA

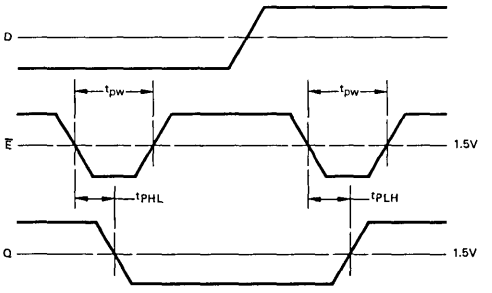
Notes: 1. Typical Limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2. Actual input currents are obtained by multiplying unit load current by input load factor (See Loading Rules).

Switching Characteristics (T_A = 25°C)

Parameters	Description	Test Conditions	Limits Min.	Typ.	Max.	Units
t_{PLH} t_{PHL}	Turn-Off Delay Enable to Output Turn-On Delay Enable to Output	V_{CC} = 5.0 V, C_L = 15 pF, (See Figure 1)		16 15	23 24	ns
t_{PLH} t_{PHL}	Turn-Off Delay Data to Output Turn-On Delay Data to Output	V_{CC} = 5.0 V, C_L = 15 pF, (See Figure 2)		28 16	35 24	ns
t_{PLH} t_{PHL}	Turn-Off Delay Address to Output Turn-On Delay Address to Output	V_{CC} = 5.0 V, C_L = 15 pF, (See Figure 3)			35 35	ns
t_{PHL}	Turn-On Delay Clear to Output	V_{CC} = 5.0 V, C_L = 15 pF, (See Figure 5)		21		ns
t_s(H) t_h(H)	Set-up Time HIGH Data to Enable Hold Time HIGH Data to Enable (See Note 5)	V_{CC} = 5.0 V, (See Figure 4)	20 0	13 −10		ns
t_s(L) t_h(L)	Set-up Time LOW Data to Enable Hold Time LOW Data to Enable (See Note 5)		17 0	10 −13		ns
t_s(A-$\bar{E}$)	Set-up Time Address to Enable (See Note 3)	V_{CC} = 5.0 V, (See Figure 6)	5	0		ns
t_{pw}($\bar{E}$)	Enable Pulse Width	V_{CC} = 5.0 V, (See Figure 1)	17	11		ns

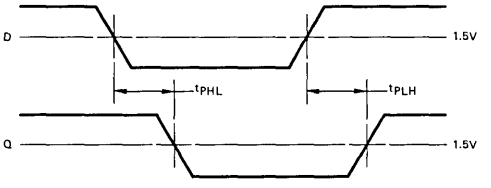
Notes: 3. The Address to enable set-up time is the time before the HIGH-to-LOW enable transition that the address must be stable so that the correct latch is addressed and the other latches are not affected.
4. The cross hatched areas indicate when the inputs are permitted to change for predictable output performance.
5. Another way of specifying a negative hold time is to specify a positive release time. When specified, the release time falls within the set-up interval time thereby giving the equivalent of a negative hold time.

SWITCHING TEST TIME WAVEFORMS



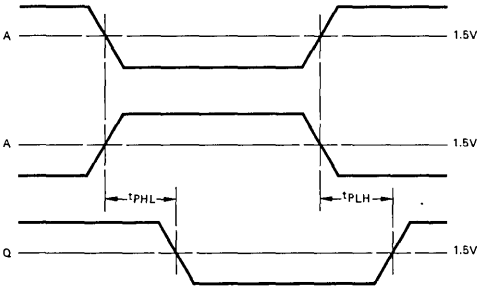
Other Conditions: $\overline{C}$ = H, A = Stable

Figure 1. Turn-On & Turn-Off Delays Enable to Output and Enable Pulse Width



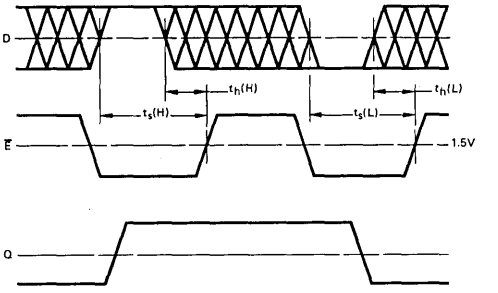
Other Conditions: $\overline{E}$ = L, $\overline{C}$ = H, A = Stable

Figure 2. Turn-On & Turn-Off Delays Data to Output



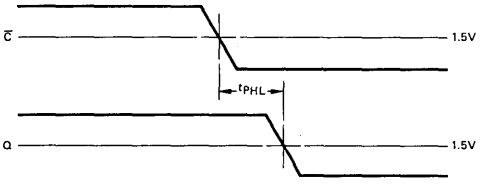
Other Conditions: $\overline{E}$ = L, $\overline{C}$ = L, D = H

Figure 3. Turn-On & Turn-Off Delays Address to Output



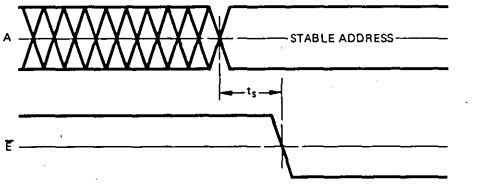
Other Conditions: $\overline{C}$ = H, A = Stable

Figure 4. Set-up & Hold Time Data to Enable (See Notes 4 & 5)



Other Conditions: $\overline{E}$ = H

Figure 5. Turn-On Delay Clear to Output



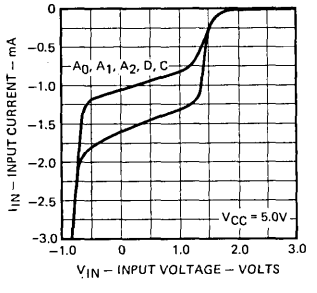
Other Conditions: $\overline{C}$ = H

Figure 6. Set-up Time Address to Enable (See Note 4)

PERFORMANCE CURVES

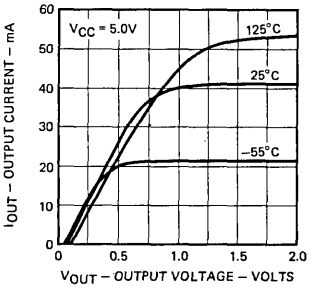
INPUT/OUTPUT CHARACTERISTICS

Input

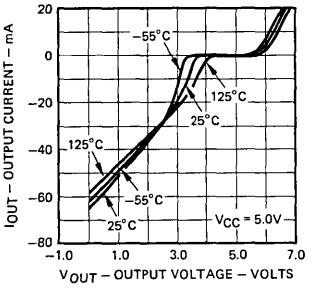


Output

Low State



High State



DEFINITION OF TERMS

SUBSCRIPT TERMS

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS

A_{0-2} Write address field. Data on D is written into the location specified by the A address field.

$\overline{E}$ On going from a HIGH logic level to a LOW logic level (clear HIGH), the addressed latch output will follow the information on the D input. When the enable input goes from a LOW logic level to a HIGH logic level, the data on the D input is stored in the addressed latch.

$\overline{C}$ The clear input is used in conjunction with the enable input to select the operating mode of the device. See the mode selection table for definition of states.

D Information on the D input is written into the latch specified by the A address field when the enable goes from a LOW logic level to a HIGH logic level.

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

Input Unit Load One T^2L gate input load. In the HIGH state it is equal to 40μA at 2.4 V and in the LOW state it is equal to −1.6mA at 0.4 V.

Q_{0-7} The eight individual latch outputs.

OPERATIONAL TERMS

I_{IL} Forward input load current.

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{CC} The current drawn by the device from V_{CC} power supply with input and output terminals open.

I_{IH} Reverse input load current.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{IN} Input voltage applied in I_{IL}, I_{IH} tests.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} flowing into output.

SWITCHING TERMS

t_{PLH} Propagation delay time for LOW-to-HIGH output transition. The time between the specified reference points on the input and output voltage waveforms (TTL = 1.5 volts) with the output changing from the LOW level to the HIGH level.

t_{PHL} Propagation delay time for HIGH-to-LOW output transition. The time between the specified reference points on the input and output voltage waveforms (TTL = 1.5 volts) with the output changing from the HIGH level to the LOW level.

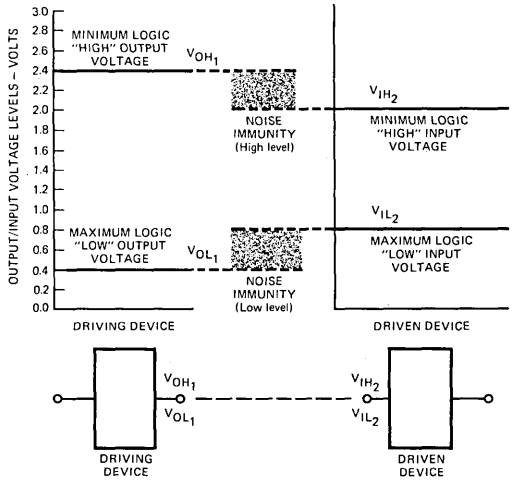
t_h Hold time. The time interval for which a signal is retained at a specified level for a specified input terminal after an active transition occurs at another specified input terminal.

t_s Set-up time. The time interval for which a signal must be applied and maintained at a specified level for a specified input terminal before an active transition occurs at another specified input terminal.

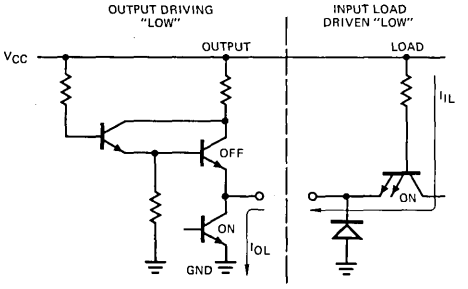
t_{pw} The minimum LOW enable pulse width required to write data into the addressed latch. Refer to Figure 1.

INPUT/OUTPUT INTERFACE CONDITIONS

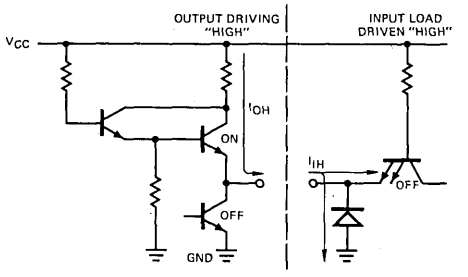
Voltage Interface Conditions – LOW & HIGH



Current Interface Conditions – LOW



Current Interface Conditions – HIGH



MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
Advanced Micro Devices 54/7400 Series	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

LOADING RULES

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Output LOW
A_0	1	1	–	–
A_1	2	1	–	–
A_2	3	1	–	–
Q_0	4	–	18	6
Q_1	5	–	18	6
Q_2	6	–	18	6
Q_3	7	–	18	6
GND	8	–	–	–
Q_4	9	–	18	6
Q_5	10	–	18	6
Q_6	11	–	18	6
Q_7	12	–	18	6
D	13	1	–	–
$\overline{E}$	14	1.5	–	–
$\overline{C}$	15	1	–	–
V_{CC}	16	–	–	–

FUNCTION TABLE

$\overline{E}$	$\overline{C}$	Mode
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH Eight-Channel Demultiplexer
H	L	Clear

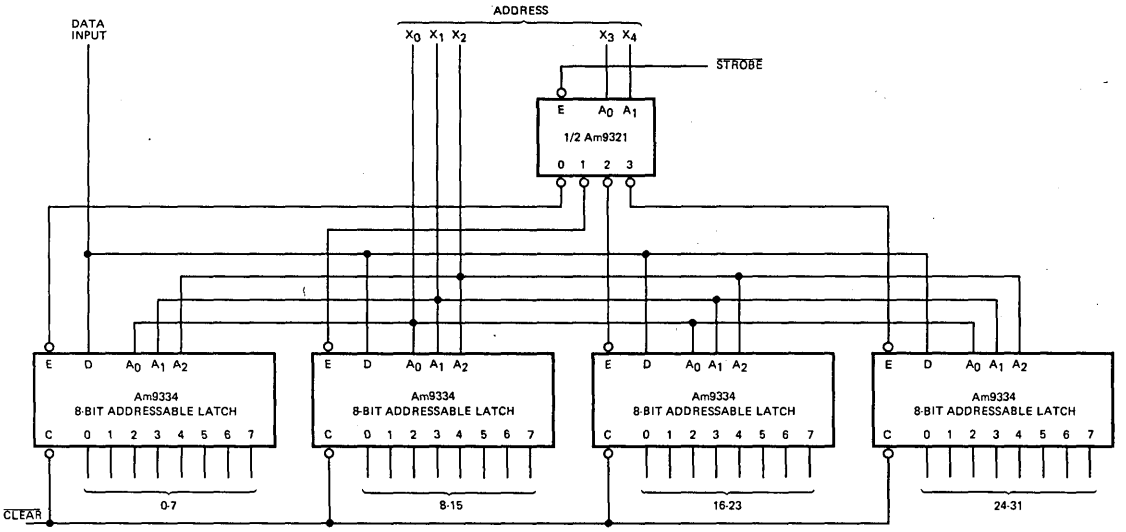
TRUTH TABLE

Input States						Present Output States								
$\overline{C}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	MODE
L	H	X	X	X	X	L	L	L	L	L	L	L	L	CLEAR
L	L	L	L	L	L	L	L	L	L	L	L	L	L	DEMULTIPLEX
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
.	.	.		.					.					
.	.	.		.					.					
L	L	L	H	H	H	L	L	L	L	L	L	L	L	
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{N-1} →								MEMORY
H	L	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1} →					ADDRESSABLE
H	L	H	L	L	L	H	Q_{N-1}	Q_{N-1} →						LATCH
H	L	L	H	L	L	Q_{N-1}	L	Q_{N-1} →						
H	L	H	H	L	L	Q_{N-1}	H	Q_{N-1} →						
.	.	.		.										
.	.	.		.										
.	.	.		.										
H	L	L	H	H	H	Q_{N-1} →						Q_{N-1}	L	
H	L	H	H	H	H	Q_{N-1} →						Q_{N-1}	H	

X = Dont't Care Condition
L = LOW Voltage Level
H = HIGH Voltage Level
Q_{N-1} = Previous Output State

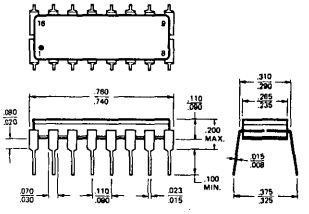
APPLICATIONS

32-BIT ADDRESSABLE LATCH AND 1-OF-32 DECODER/DEMULTIPLEXER

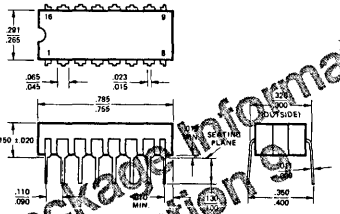


PHYSICAL DIMENSIONS
Dual-In-Line

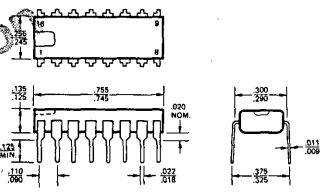
Hermetic



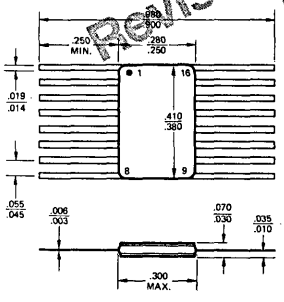
Ceramic



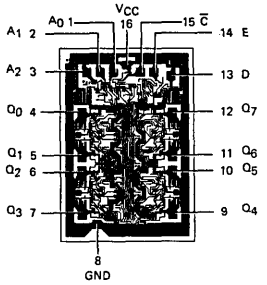
Molded



Flat Package



Metallization and Pad Layout



DIE SIZE 0.065" x 0.096"

ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am9338
8-Bit Multiple Port Register

Distinctive Characteristics:

- 8 word x 1 bit simultaneous read-write three address register.
- Access time of 48 ns typical.
- Slave enable allows scanning of memory contents.
- 100% reliability assurance testing in compliance with MIL STD 883
- Electrically tested and optically inspected die for the assemblers of hybrid products
- Mixing privileges for obtaining price discounts. Refer to price list
- Available in highly reliable molded, hermetic dual in-line or hermetic flat package

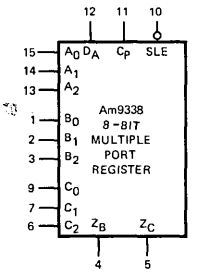
FUNCTIONAL DESCRIPTION

The Am9338 is a three-address eight-bit register organized as eight words of one bit per word. The register is designed for high-speed memory applications and is particularly suitable as the high-speed scratch pad memory in military and commercial three-address computers. Data can be written into one location and simultaneously read from any two locations.

The register is organized in a master slave arrangement where there are eight master latches and two slave latches. Data on the D_A input is stored in the master latch selected by the write address field A during the clock LOW time. Data from the eight masters is then selected by the two independent read address fields B, C and stored in the two slave latches during the clock HIGH time. This eight master two slave arrangement makes the register indistinguishable from an eight master eight slave system and allows both the two read addresses B and C and the write address A to be simultaneously applied to the register at the start of a clock cycle.

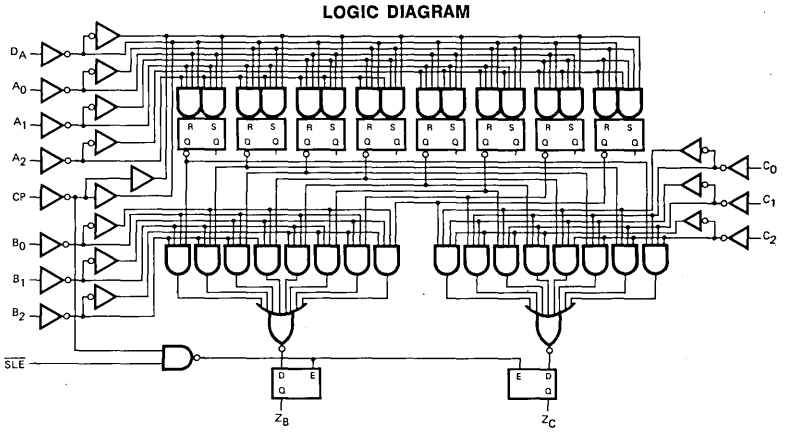
A slave enable is provided which if held LOW continuously enables the two slave latches and immediately transfers information from the master latches to the outputs so that the memory contents can be scanned asynchronously.

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

LOGIC DIAGRAM

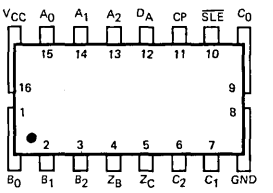


Am9338 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	U6M933859X
Hermetic DIP	0°C to +75°C	U7B933859X
Hermetic DIP	−55°C to +125°C	U7B933851X
Hermetic Flat Pak	−55°C to +125°C	U4L933851X
Dice	Note	UXX9338XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am933859X T_A = 0°C to +75°C V_{CC} = 5.0 V ±5%
Am933851X T_A = −55°C to +125°C V_{CC} = 5.0 V ±10%

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.8 mA V_{IN} = V_{IH} or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16.0 mA V_{IN} = V_{IH} or V_{IL}		0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V		−1.0	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V		4.0	40	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V	−10	−35	−70	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		64	99	mA

Notes: 1) Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by input load factor (see Loading Rules).

SWITCHING CHARACTERISTICS (T_A = 25°C) (V_{CC} = 5.0 V, C_L = 15 pF)

Parameters		Test Conditions	Min	Typ	Max	Units
t_{pd+}	Turn Off Delay CP to Output	$A_{0,1,2}$ = $B_{0,1,2}$ = $C_{0,1,2}$	12	24	42	ns
t_{pd-}	Turn On Delay CP to Output	$\overline{SLE}$ = H	10	19	40	ns
t_{pd+} (D_A-Z)	Turn Off Delay Data to Output	$\overline{SLE}$ = L, C_P = L	17	35	75	ns
t_{pd-} (D_A-Z)	Turn On Delay Data to Output		20	42	68	ns
t_{pd+} (B,C-Z)	Turn Off Delay Address to Output	C_P = H	13	26	43	ns
t_{pd-} (B,C-Z)	Turn On Delay Address to Output		24	48	81	ns
t_{sH} (D_A)	Set Up Time HIGH Data		7	15	23	ns
t_{sL} (D_A)	Set Up Time LOW Data		3	8	13	ns
t_s (A)	Set Up Time, Address Inputs		3	10	23	
CP_{pw} 'L'	Minimum LOW Clock Pulse Width			11	16	ns
CP_{pw} 'H'	Minimum HIGH Clock Pulse Width			10	15	

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

Input Current Versus Input Voltage
$D_A A_0 A_1 A_2 C_0 C_1 C_2 B_0 B_1 B_2$

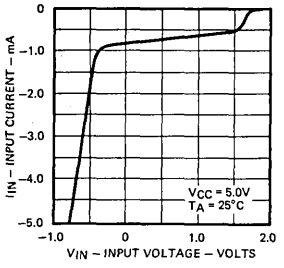


Figure 1

Input Current Versus Input Voltage $\overline{SLE}$

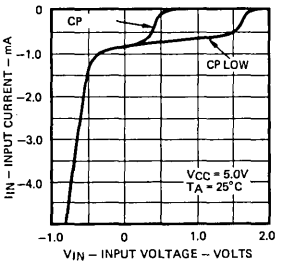


Figure 2

Output Current Versus Output Voltage Z_B and Z_C (Low State)

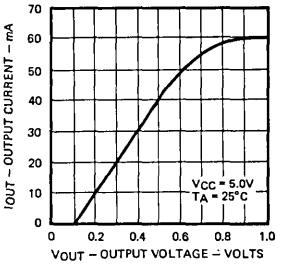


Figure 3

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS:

A_{0-2} Write address field. Data on D_A is written into the location specified by the A address field.

B_{0-2} Read address field. Data stored in the master latch specified by the B Read Address Field is transferred to the B slave latch and appears at the Z_B output when the clock pulse goes from a LOW logic level to a HIGH logic level.

C_{0-2} Read Address Field. Data stored in the master latch specified by the C Read Address Field is transferred to the C slave latch and appears at the Z_C output when the clock pulse goes from a LOW logic level to a HIGH logic level.

CP Clock Pulse. On going from a HIGH logic level to a LOW logic level the information on the D_A input is stored in the master latch specified by the Write A Address Field. When the clock pulse goes from a LOW logic level to a HIGH logic level information from the master latch or latches specified by the B and C Read Address Fields are stored in the two slave latches and appears at the outputs Z_B, Z_C.

D_A Information on the D_A input is written into the master latch specified by the A Address Field when the clock goes from a HIGH logic level to a LOW logic level.

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

Input Unit Load One T^2L gate input load. In the HIGH state it is equal to I_{IH} and in the LOW state it is equal to I_{IL}.

$\overline{SLE}$ Slave Enable. When LOW continuously allows information from the master latch addressed by the two read fields B, C to appear at the outputs Z_B, Z_C.

Z_B The B read address output.

Z_C The C read address output.

OPERATIONAL TERMS:

I_{IL} Forward input load current.

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{CC} The current drawn by the device from V_{CC} power supply with input and output terminals open.

I_{IH} Reverse input load current.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{IN} Input voltage applied in I_{IL}, I_{IH} tests.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} flowing into output.

SWITCHING TERMS

t_{pd+} The propagation delay from the clock input LOW to HIGH transition to the Z output LOW to HIGH transition. Refer to Figure 4.

t_{pd-} The propagation delay from the clock input HIGH to LOW transition to the Z output HIGH to LOW transition. Refer to Figure 4.

t_{sL} (D_A) The time required for a LOW logic level to be present at the D_A input prior to the clock input transition from LOW to HIGH in order for the master latch to retain a LOW logic level. Refer to Figure 7. LOW data must be present at all times between t_{sL} max. and t_{sH} min.

t_{sH} (D_A) The time required for a HIGH logic level to be present at the D_A input prior to the clock input transition from LOW to HIGH in order for the master latch to retain a HIGH logic level. Refer to Figure 7. HIGH data must be present at all times between t_{sH} max. and t_{sL} min.

t_s(A) The time, relative to either clock edge, required for the device to respond to changes on the A address inputs.

t_{pd+} (D_A) The propagation delay from the data input LOW to HIGH transition to the Z output LOW to HIGH transition. Refer to Figure 5.

t_{pd-} (D_A) The propagation delay from the data input HIGH to LOW transition to the Z output HIGH to LOW transition. Refer to Figure 5.

t_{pd+}(B,C-Z) The propagation delay from the B or C address input transition to the Z output LOW to HIGH transition. Refer to Figure 6.

t_{pd-}(B,C-Z) The propagation delay from the B, C address input transition to the Z output HIGH to LOW transition. Refer to Figure 6.

CP_{pw} 'L' The minimum LOW clock pulse width required to write data into the master latch. Refer to Figure 8.

CP_{pw} 'H' The minimum HIGH clock pulse width required to store information into the slave latch. Refer to Figure 9.

TYPICAL SWITCHING TIME CHARACTERISTICS

All inputs and outputs loaded with 15 pF capacitance only. Output capacitance is referred to as C_L.

Propagation Delay Versus Ambient Temperature (CP to Z)

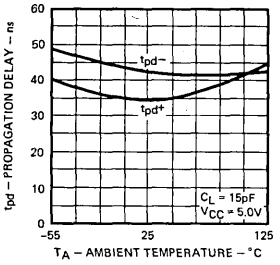


Figure 4

Propagation Delay Versus Ambient Temperature (D_A to Z)

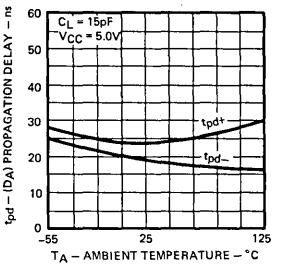


Figure 5

Propagation Delay Versus Ambient Temperature (Read Address to Z)

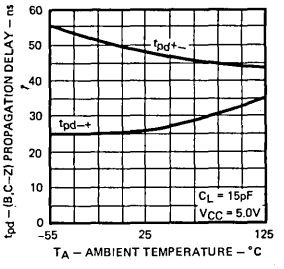


Figure 6

Set Up, Release Time Versus Ambient Temperature

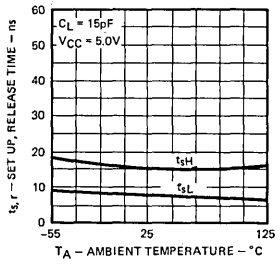


Figure 7

Minimum LOW Clock Pulse Width

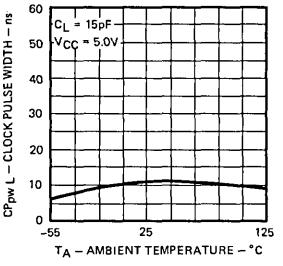


Figure 8

Minimum HIGH Clock Pulse Width

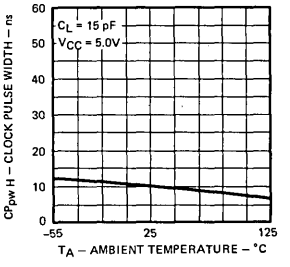
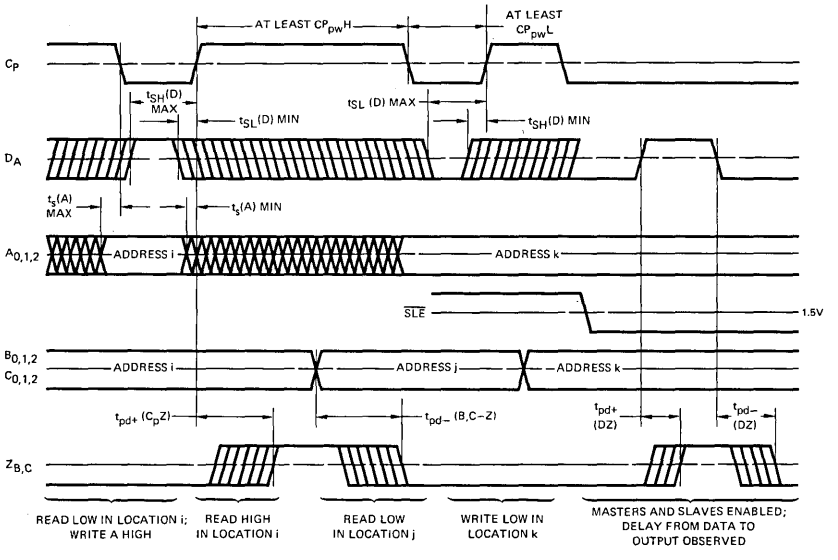


Figure 9

SWITCHING TIME WAVEFORMS



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
——— ———	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN

MSI INTERFACING RULES

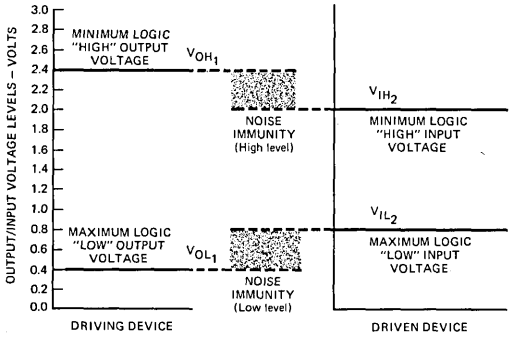
Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
Advanced Micro Devices 54/7400	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

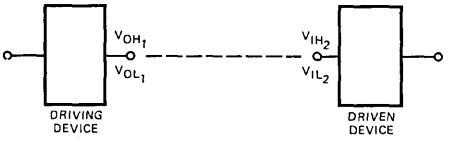
Am9338 LOADING RULES (in unit loads)

Input/Output	Pin No.'s	Input Unit Load	Output Drive HIGH	LOW
B_0	1	0.625	—	—
B_1	2	0.625	—	—
B_2	3	0.625	—	—
Z_B	4	—	20	10
Z_C	5	—	20	10
C_2	6	0.625	—	—
C_1	7	0.625	—	—
GND	8	—	—	—
C_0	9	0.625	—	—
$\overline{SLE}$	10	0.625	—	—
CP	11	0.625	—	—
DA	12	0.625	—	—
A_2	13	0.625	—	—
A_1	14	0.625	—	—
A_0	15	0.625	—	—
V_{CC}	16	—	—	—

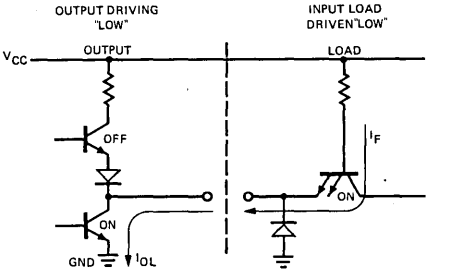
INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH

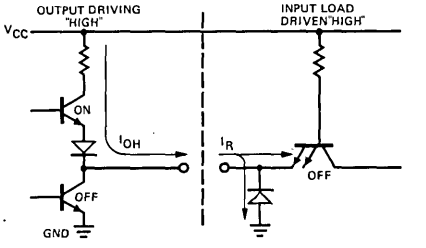




Current Interface Conditions — LOW

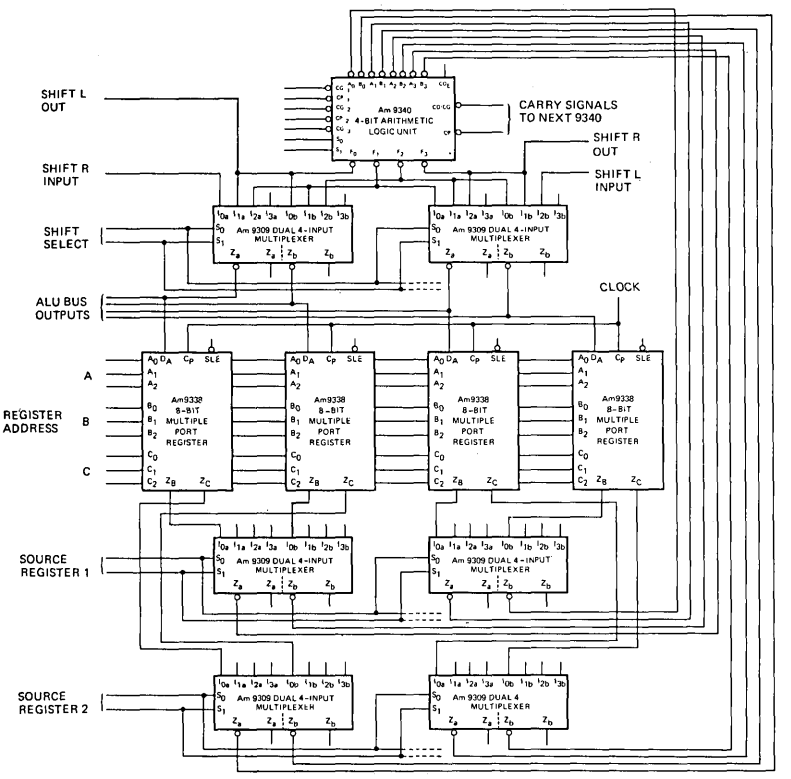


Current Interface Conditions — HIGH



Am9338 APPLICATION

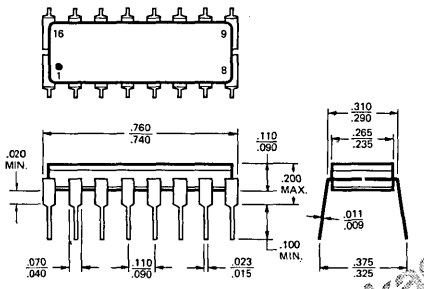
THREE ADDRESS ARITHMETIC REGISTER 4-BIT SLICE



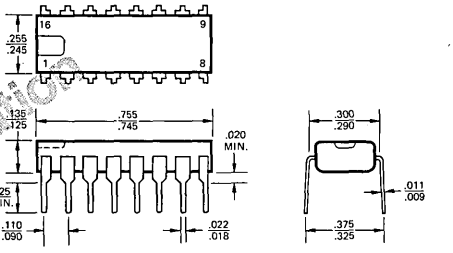
A typical three address arithmetic register system where two operands can be taken from any two registers, operated upon, and the result written in to any register in the system.

PHYSICAL DIMENSIONS
Dual-In-Line

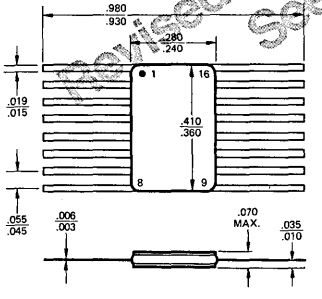
Hermetic



Molded

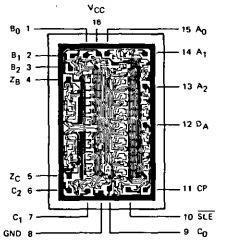


PHYSICAL DIMENSIONS
Flat Package



Metallization and Pad Layout

77 x 125 Mils



ADVANCED MICRO DEVICES INC.
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TELEX: 34-6306

Am93L38
Low-Power 8-Bit Multiple Port Register

Distinctive Characteristics:

- Three address register
- Synchronous or asynchronous operation
- 100% reliability assurance testing in compliance with MIL STD 883
- 80 mW typical power dissipation.

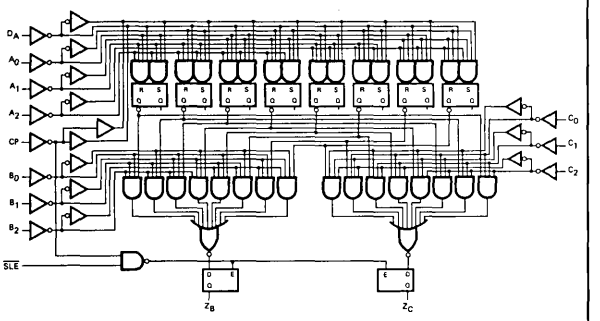
FUNCTIONAL DESCRIPTION

The Am93L38 is a three-address eight-bit register organized as eight words of one bit per word. The register is designed for high-speed memory applications and is particularly suitable as the high-speed scratch pad memory in military and commercial three-address computers. Data can be written into one location and simultaneously read from any two locations.

The register is organized in a master slave arrangement where there are eight master latches and two slave latches. Data on the D_A input is stored in the master latch selected by the write address field A during the clock LOW time. Data from the eight masters is then selected by the two independent read address fields B, C and stored in the two slave latches during the clock HIGH time. This eight master two slave arrangement makes the register indistinguishable from an eight master eight slave system and allows both the two read addresses B and C and the write address A to be simultaneously applied to the register at the start of a clock cycle.

A slave enable is provided which if held LOW continuously enables the two slave latches and immediately transfers information from the master latches to the outputs so that the memory contents can be scanned asynchronously.

LOGIC DIAGRAM



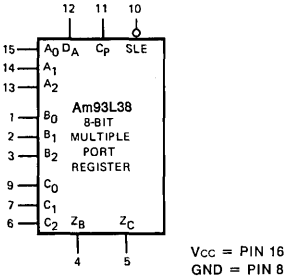
LOADING RULES

In Unit Loads (Notes)

Input Load Factor	TTL LOADS HIGH	TTL LOADS LOW	93L LOADS HIGH	93L LOADS LOW
All Inputs	.313	.156	.625	.625
Output Drive	HIGH	LOW	HIGH	LOW
Z_B, Z_C	6	3	12	12

NOTES:
1) A TTL unit load is specified as 0.4 V at −1.6 mA LOW, 2.4 V at 40 μA HIGH.
2) A 93L unit load is specified as 0.3 V at −400 μA LOW, 2.4 V at 20 μA HIGH.
3) Enough output LOW current is available to mix TTL and 93L loads and still meet the 93L requirement of a V_{OL} of 0.3 V.

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

Am93L38 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
16-Pin Molded DIP	0°C to +75°C	U6M93L3859X
16-Pin Hermetic DIP	0°C to +75°C	U7B93L3859X
16-Pin Hermetic DIP	−55°C to +125°C	U7B93L3851X
16-Pin Hermetic Flat Pak	−55°C to +125°C	U4L93L3851X
Dice	Note	UXX93L38XXD

Note The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current (Note 1)	−30 mA to +5.0 mA

Note 1. Maximum current defined by DC input voltage.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93L4059X $T_A = 0°C$ to $+75°C$ $V_{CC} = 4.75$ V to 5.25 V
Am93L4051X $T_A = -55°C$ to $+125°C$ $V_{CC} = 4.50$ V to 5.50 V

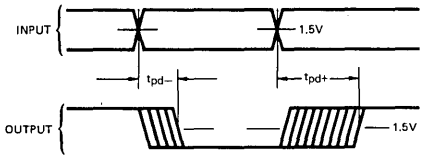
Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -0.4$ mA $V_{IN} = V_{IH}$ or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $I_{OL} = 4.92$ mA $V_{IN} = V_{IH}$ or V_{IL}		0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.7	Volts
I_{IL} (Note 2)	93L Unit Load Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.3$ V		−0.25	−0.4	mA
I_{IH} (Note 2)	93L Unit Load Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.4$ V		2.0	20	μA
	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 5.5$ V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., $V_{OUT} = 0.0$ V	−10	−22	−40	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		22	37	mA

Notes: 1) Typical limits are at $V_{CC} = 5.0$ V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by the 93L input load factor. (See loading rules)

SWITCHING CHARACTERISTICS ($T_A = 25°C$) ($V_{CC} = 5.0$ V, $C_L = 15$ pF)

Parameters		Test Conditions	Min	Typ	Max	Units
t_{pd+}	Turn Off Delay CP to Output	$A_{0,1,2} = B_{0,1,2} = C_{0,1,2}$	23	45	100	ns
t_{pd-}	Turn On Delay CP to Output		22	41	90	ns
t_{pd+} (D_A-Z)	Turn Off Delay Data to Output	$\overline{SLE} = L$	45	85	175	ns
t_{pd-} (D_A-Z)	Turn On Delay Data to Output		55	100	202	ns
t_{pd+} (B,C-Z)	Turn Off Delay Address to Output	$C_P = H$	20	50	111	ns
t_{pd-} (B,C-Z)	Turn On Delay Address to Output		50	125	254	ns
t_{sH} (D_A)	Set Up Time HIGH Data		20	49	75	ns
t_{sL} (D_A)	Set Up Time LOW Data		18	31	47	ns
t_s (A)	Set Up Time, Address Inputs		18	38	75	
CP_{pw} 'L'	Minimum LOW Clock Pulse Width			24	37	ns
CP_{pw} 'H'	Minimum HIGH Clock Pulse Width			22	34	

SWITCHING TIME WAVEFORMS



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TELEX: 34-6306

Am9340
Four-Bit Arithmetic Logic Unit

Distinctive Characteristics

- Provides addition and subtraction and two logic functions.
- Typical add time of only 20ns and subtract time of only 25ns for 4 bits.
- Provision made for full look-ahead arithmetic over 16-bit words without additional carry package.
- Can be operated in ripple-block mode to give typical addition time of only 47ns for 28-bit words without additional carry packages.
- 100% reliability assurance testing in compliance with MIL-STD-883
- Electrically tested and optically inspected die for the assemblers of hybrid products
- Mixing privileges for obtaining price discounts. Refer to price list

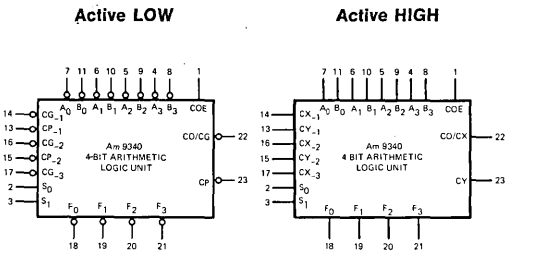
FUNCTIONAL DESCRIPTION

The Am9340 is a high speed Arithmetic Logic Unit which can perform two arithmetic operations and two logic functions on two binary 4-bit words. The arithmetic operations are add and subtract and the logic functions are AND and EXCLUSIVE OR for active LOW data inputs and OR and EQUIVALENCE for active HIGH data inputs. The operation performed by the Arithmetic Logic Unit is determined by two select inputs S_0 and S_1. The Am9340 can perform arithmetic operations in 1's or 2's complement arithmetic and incorporates full internal look-ahead for high-speed operations.

Provision is made for external look-ahead by using the ($\overline{CP}$) carry propagate and ($\overline{CO/CG}$) carry out/carry generate functions. An input carry network on the Arithmetic Logic Unit allows full look-ahead over the first sixteen bits of a word and ripple-block carry between subsequent word increments of 12 bits. This ripple-block carry method of cascading units is accomplished by having the (COE) carry out enable input HIGH at the most significant unit in each block so as to give a carry-out signal from the carry out/carry generate output. This carry-out signal is then used as the carry-in signal to the next block. The COE inputs for all other units are tied to ground as shown in Figure 3. This ripple-block method of addition and subtraction gives high-speed operation 60ns typical addition time for 40-bit words, without additional carry packages.

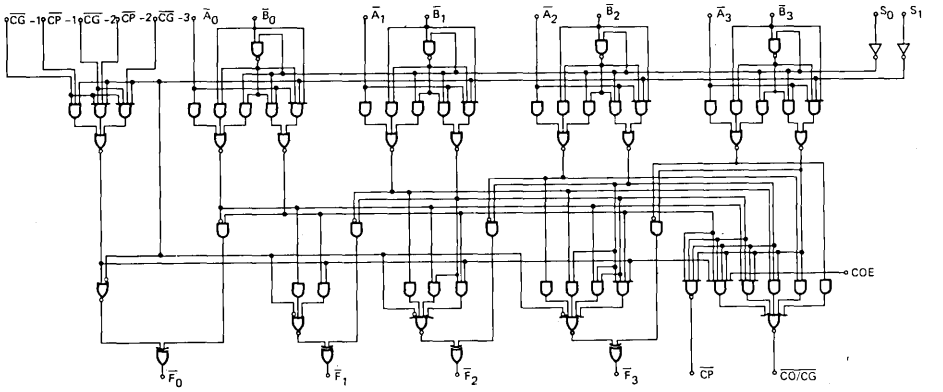
The Am9340 can be used with either active LOW or active HIGH data inputs. In the active HIGH case although the look-ahead carry inputs and outputs are not carry generate and carry propagate, but are labelled Cx and Cy respectively they are still connected in the same manner as the active LOW case.

LOGIC SYMBOL



V_{CC} = PIN 24
GND = PIN 12

LOGIC DIAGRAM

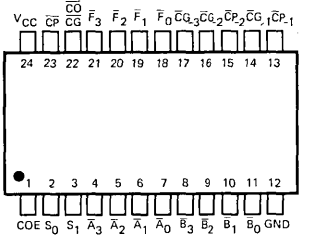


Am9340 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	AM934059C
Hermetic DIP	0°C to +75°C	U6N934059X
Hermetic DIP	−55°C to +125°C	U6N934051X
Hermetic Flat Pak	−55°C to +125°C	U4M934051X
Dice	Note	UXX9340XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature range.

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to + 5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am934059X $T_A = 0°C$ to $+75°C$ $V_{CC} = 5.0\ V \pm 5\%$
Am934051X $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0\ V \pm 10\%$

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -0.8$ mA $V_{IN} = V_{IH}$ or V_{IL}		2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $I_{OL} = 16.0$ mA $V_{IN} = V_{IH}$ or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4$ V			−1.0	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.4$ V			6.0	40	μA
	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 5.5$ V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., $V_{OUT} = 0.0$ V	Am934051X	−30		−100	mA
			Am934059X	−30		−100	
I_{CC}	Power Supply Current	$S_O = B_{0-3} = 0$ V All other inputs = 4.5 V V_{CC} = MAX.	Am934051X		85	127	mA
			Am934059X		85	128	

Notes: 1) Typical limits are at $V_{CC} = 5.0$ V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by input load factor (See Loading Rules).

Switching Characteristics ($T_A = 25°C$)

		Test Conditions	Min	Typ	Max	Units
t_{pd+}	Turn Off Delay ($\overline{B}_0$ to $\overline{F}_3$) Add Mode	$V_{CC} = 5.0$ V, $C_L = 15$ pF Refer to test Table and Figure 1	10	20	30	ns
t_{pd-}	Turn On Delay ($\overline{B}_0$ to $\overline{F}_3$) Add Mode		10	20	30	ns
t_{pd+}	Turn Off Delay ($\overline{B}_0$ to $\overline{F}_3$) Subtract Mode		12	25	38	ns
t_{pd-}	Turn On Delay ($\overline{B}_0$ to $\overline{F}_3$) Subtract Mode		12	24	36	ns
t_{pd+}	Turn Off Delay ($\overline{B}_0$ to $\overline{CO/CG}$) Add Mode		7	13	19	ns
t_{pd-}	Turn On Delay ($\overline{B}_0$ to $\overline{CO/CG}$) Add Mode		7	13	19	ns
t_{pd+}	Turn Off Delay ($\overline{B}_0$ to $\overline{CO/CG}$) Subtract Mode		9	17	25	ns
t_{pd-}	Turn On Delay ($\overline{B}_0$ to $\overline{CO/CG}$) Subtract Mode		9	17	25	ns
t_{pd+}	Turn Off Delay ($\overline{CG}_{-3}$ to $\overline{CO/CG}$)		7	13	19	ns
t_{pd-}	Turn On Delay ($\overline{CG}_{-3}$ to $\overline{CO/CG}$)		7	13	19	ns
t_{pd+}	Turn Off Delay ($\overline{CG}_{-3}$ to $\overline{F}_3$)		11	23	35	ns
t_{pd-}	Turn On Delay ($\overline{CG}_{-3}$ to $\overline{F}_3$)		10	19	29	ns

)EFINITION OF TERMS

UBSCRIPT TERMS:

Forward, applying to LOW inputs.

HIGH, applying to a HIGH logic level or when used with V_{CC} to ıdicate high V_{CC} value.

Input.

LOW, applying to LOW logic level or when used with V_{CC} to ıdicate low V_{CC} value.

Output.

Reverse, applying to HIGH inputs.

UNCTIONAL TERMS:

$_i$ Active LOW Data A inputs i = 0, 1, 2, 3.

$_i$ Active LOW Data B inputs i = 0, 1, 2, 3.

$\overline{G}_{-i}$ Active LOW Carry Generate input from i'th previous ALU = 1, 2, 3.

$\overline{P}_{-i}$ Active LOW Carry Propagate input from i'th previous ALU = 1, 2.

OE Carry Out Enable Input. When this input is HIGH the $\overline{CO/CG}$ utput is a carry out signal and can be used to form a block ripple arry ALU. When the COE input is LOW $\overline{CO/CG}$ output is the carry enerate signal which is used for lookahead operation.

$\overline{O/CG}$ Active LOW Carry Out/Carry Generate output. A HIGH ›gic level on COE input gives Carry Out, a LOW level Carry Generate.

$\overline{P}$ Active LOW Carry Propagate output used in conjunction with ther $\overline{CG}$ and $\overline{CP}$ signals for lookahead operation.

$_i$ Active LOW Data Outputs of ALU i = 0, 1, 2, 3.

an-Out The logic HIGH or LOW output drive capability in terms f Input Unit Loads.

$_i$ Control inputs determine the arithmetic or logic function obeyed = 0, 1.

Init Load One T^2L gate input load. In the HIGH state it is equal to .2 μA at 2.4 V and in the LOW state it is equal to 1.6 mA at 0.4 V.

OPERATIONAL TERMS:

I_{IL} Forward input load current.

I_{OH} Output HIGH current forced out of output in V_{OH} test.

I_{OL} Output LOW current forced into the output in V_{OL} test.

I_{IH} Reverse input load current.

I_{CC} *The current drawn by the device under a +5.0 V power supply* bias with inputs S_0, $\overline{B}_0$, $\overline{B}_1$, $\overline{B}_2$, $\overline{B}_3$ at 0 V and all other inputs and outputs open circuit.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage. Refer to Figure 2.

V_{IL} Maximum logic LOW input voltage. Refer to Figure 2.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

SWITCHING TERMS: (All switching times are measured at the 1.5 V logic level.)

$t_{pd+}(\overline{B}_0\ \overline{F}_3)$ The propagation delay from the $\overline{B}_0$ input transition to the $\overline{F}_3$ output LOW to HIGH transition.

$t_{pd-}(\overline{B}_0\ \overline{F}_3)$ The propagation delay from the $\overline{B}_0$ input transition to the $\overline{F}_3$ output HIGH to LOW transition.

$t_{pd+}(\overline{B}_0\ \overline{CO/CG})$ The propagation delay from the $\overline{B}_0$ input transition to the $\overline{CO/CG}$ output LOW to HIGH transition.

$t_{pd-}(\overline{B}_0\ \overline{CO/CG})$ The propagation delay from the $\overline{B}_0$ input transition to the $\overline{CO/CG}$ output HIGH to LOW transition.

$t_{pd+}(\overline{CG}_{-3}\ \overline{CO/CG})$ The propagation delay from the $\overline{CG}_{-3}$ input transition to the $\overline{CO/CG}$ LOW to HIGH transition.

$t_{pd-}(\overline{CG}_{-3}\ \overline{CO/CG})$ The propagation delay from the $\overline{CG}_{-3}$ input transition to the $\overline{CO/CG}$ HIGH to LOW transition.

$t_{pd+}(\overline{CG}_{-3}\ \overline{F}_3)$ The propagation delay from the $\overline{CG}_{-3}$ input transition to the $\overline{F}_3$ output LOW to HIGH transition.

$t_{pd-}(\overline{CG}_{-3}\ \overline{F}_3)$ The propagation delay from the $\overline{CG}_{-3}$ input transition to the $\overline{F}_3$ output HIGH to LOW transition.

SWITCHING TEST TABLE

Parameter	Operation	Inputs at 4.5 V	Inputs at GND	Waveform
t_{pd+} $(\overline{B}_0\ \overline{F}_3)$ t_{pd-} $(\overline{B}_0\ \overline{F}_3)$	Add	S_0, $\overline{CG}_{-1}$, $\overline{CP}_{-1}$, $\overline{B}_1$ $\overline{B}_2$	S_1, $\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$, $\overline{A}_3$, $\overline{B}_3$	1
t_{pd+} $(\overline{B}_0\ \overline{F}_3)$ t_{pd-} $(\overline{B}_0\ \overline{F}_3)$	Subtract	$\overline{CG}_{-1}$, $\overline{CP}_{-1}$, $\overline{B}_3$	S_0, S_1, $\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$, $\overline{A}_3$ $\overline{B}_1$, $\overline{B}_2$	2
t_{pd+} $(\overline{B}_0\ \overline{CO/CG})$ t_{pd-} $(\overline{B}_0\ \overline{CO/CG})$	Add	S_0, $\overline{CG}_{-1}$, $\overline{CP}_{-1}$, $\overline{B}_1$, $\overline{B}_2$, $\overline{B}_3$	S_1, COE, $\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$, $\overline{A}_3$	1
t_{pd+} $(\overline{B}_0\ \overline{CO/CG})$ t_{pd-} $(\overline{B}_0\ \overline{CO/CG})$	Subtract	$\overline{CG}_{-1}$, $\overline{CP}_{-1}$	S_0, S_1, COE, $\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$, $\overline{A}_3$ $\overline{B}_1$, $\overline{B}_2$, $\overline{B}_3$	2
t_{pd+} $(\overline{CG}_{-3}\ \overline{CO/CG})$ t_{pd-} $(\overline{CG}_{-3}\ \overline{CO/CG})$	Add	S_0, $\overline{CG}_{-1}$, $\overline{CG}_{-2}$, COE, $\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$, $\overline{A}_3$	S_1, $\overline{B}_0$, $\overline{B}_1$, $\overline{B}_2$, $\overline{B}_3$ $\overline{CP}_{-1}$, $\overline{CP}_{-2}$	1
t_{pd+} $(\overline{CG}_{-3}\ \overline{F}_3)$ t_{pd-} $(\overline{CG}_{-3}\ \overline{F}_3)$	Add	S_0, $\overline{CG}_{-1}$, $\overline{CG}_{-2}$, $\overline{B}_3$ $\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$, $\overline{A}_3$	S_1, $\overline{B}_0$, $\overline{B}_1$, $\overline{B}_2$, $\overline{CP}_{-1}$, $\overline{CP}_{-2}$	1

SWITCHING WAVEFORMS

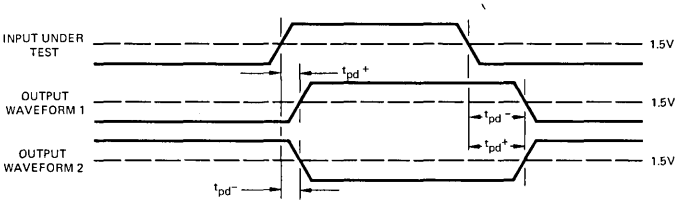
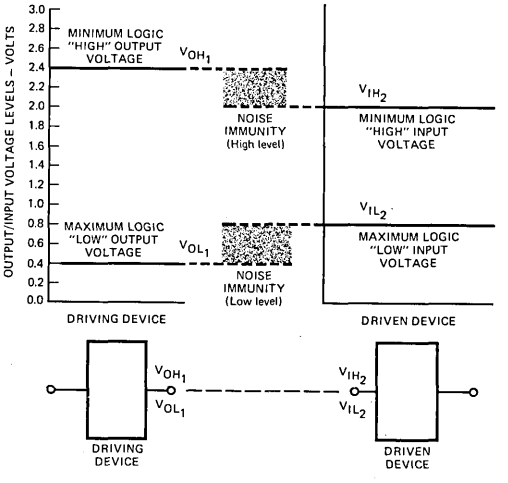


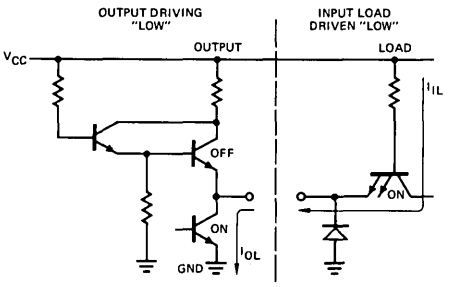
Figure 1

INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH



Current Interface Conditions — LOW



Current Interface Conditions — HIGH

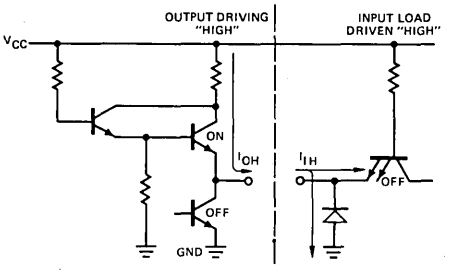


Figure 2

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Table I

USER NOTES

1. Arithmetic operations are performed on a word basis.
2. Logic operations are performed on a bit basis.
3. Arithmetic in 1's complement requires an end-around carry. This is obtained by connecting the $\overline{CO}/\overline{CG}$ output of the last ALU to the $\overline{CG}_{-1}$ input of the first ALU.
4. Subtraction in 2's complement requires a carry-in ($\overline{CG}_{-1}$ = LOW) active LOW case, (CX_{-1} = HIGH) active HIGH case. This is obtained by connecting S_0 to $\overline{CG}_{-1}$ for the active LOW case and S_0 through an inverter to CX_{-1} for the active HIGH case.

Am9340 LOADING RULES (in unit loads)

Input/Output	Pin No.'s	Input Unit Load	Output Drive HIGH	LOW
COE	1	1.5	—	—
S_0	2	1	—	—
S_1	3	1	—	—
$\overline{A}_3$	4	3	—	—
$\overline{A}_2$	5	3	—	—
$\overline{A}_1$	6	3	—	—
$\overline{A}_0$	7	3	—	—
$\overline{B}_3$	8	3	—	—
$\overline{B}_2$	9	3	—	—
$\overline{B}_1$	10	3	—	—
$\overline{B}_0$	11	3	—	—
GND	12	—	—	—
$\overline{CP}_{-1}$	13	1	—	—
$\overline{CG}_{-1}$	14	3	—	—
$\overline{CP}_{-2}$	15	1	—	—
$\overline{CG}_{-2}$	16	2	—	—
$\overline{CG}_{-3}$	17	1	—	—
$\overline{F}_0$	18	—	20	10
$\overline{F}_1$	19	—	20	10
$\overline{F}_2$	20	—	20	10
$\overline{F}_3$	21	—	20	10
$\overline{CO}/\overline{CG}$	22	—	20	10
$\overline{CP}$	23	—	20	10
V_{CC}	24	—	—	—

Table II

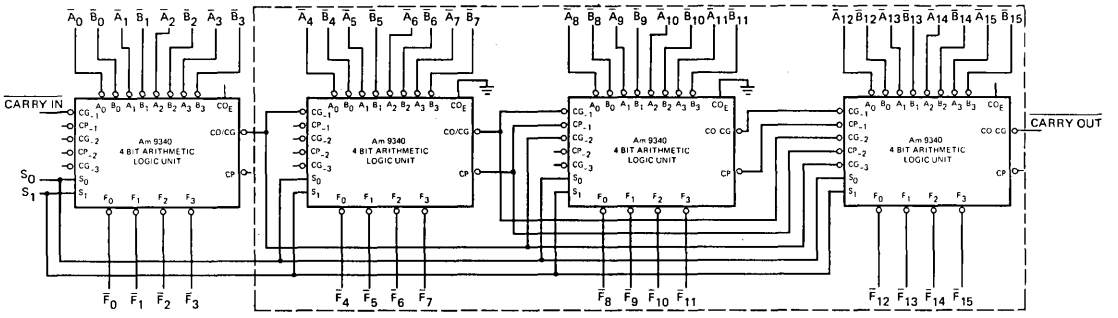
OPERATION TABLE

Control Inputs		Active LOW Inputs and Outputs			Active HIGH Inputs and Outputs		
S_0	S_1	Function			Function		
L	L	A	SUBTRACT	B	A	SUBTRACT	B
H	L	A	ADD	B	A	ADD	B
L	H	A	EXCLUSIVE OR	B	A	EQUIVALENCE	B
H	H	A	AND	B	A	OR	B

H = HIGH Voltage Level
L = LOW Voltage Level

Table III

Am9340 APPLICATION



16-Bit Full Look-ahead ALU

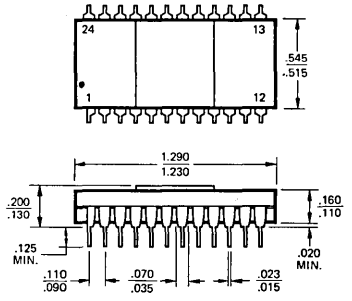
Four Am9340 ALU's can be connected together to form a 16-bit full look-ahead ALU. This ALU can work in 1's or 2's complement arithmetic representations and in the active LOW or active HIGH logic representations. If longer word lengths are required 12-bit ALU blocks connected as shown in the dashed portion of the diagram can be cascaded at the end of the 16-bit full look-ahead portion.

TYPICAL DELAY TABLE

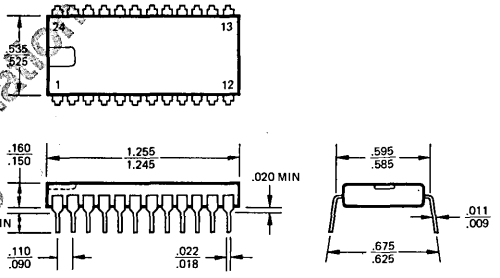
WORD LENGTH (in bits)	ADD (in ns)	SUBTRACT (in ns)
1-4	20	25
5-16	34	39
17-28	47	52
29-40	60	65
41-52	73	78
53-64	86	91
65-76	99	104
77-88	114	127
89-100	127	140

Figure 3

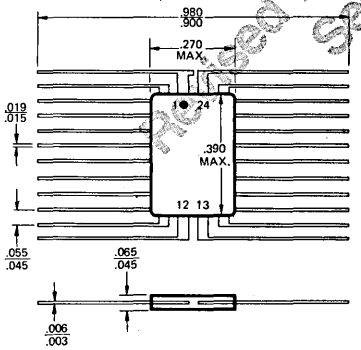
PHYSICAL DIMENSIONS
Hermetic Dual In-Line



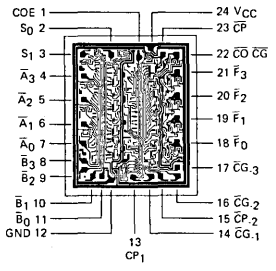
PHYSICAL DIMENSIONS
Molded Dual-In-Line



PHYSICAL DIMENSIONS
Flat Package



Metallization and Pad Layout



90 x 111 Mils

ADVANCED MICRO DEVICES INC.
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Sunnyvale
California 94086
(408) 732-2400
TLX: 34-6306
TWX: 910-339-9280

Am93L40

Low-Power Four-Bit Arithmetic Logic Unit

Distinctive Characteristics

- 110 mw typical power dissipation.
- 56 ns typical four bit add time.
- 100% reliability assurance testing in compliance with MIL STD 883
- Look-ahead carry between packages with no other components.

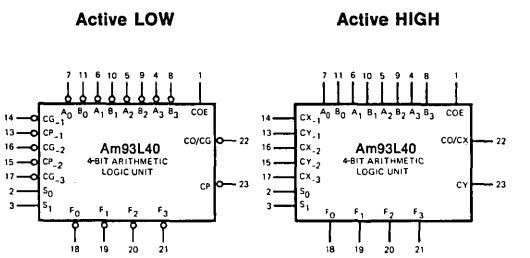
FUNCTIONAL DESCRIPTION

The Am93L40 is a high-speed arithmetic logic unit which can perform two arithmetic operations and two logic functions on two binary 4-bit words. The arithmetic operations are add and subtract and the logic functions are AND and EXCLUSIVE OR for active LOW data inputs and OR and EQUIVALENCE for active HIGH data inputs. The operation performed by the Arithmetic Logic Unit is determined by two select inputs S_0 and S_1. The Am93L40 can perform arithmetic operations in 1's or 2's complement arithmetic and incorporates full internal look-ahead for high-speed operations.

Provision is made for external look-ahead by using the ($\overline{CP}$) carry propagate and ($\overline{CO}/\overline{CG}$) carry out/carry generate functions. An input carry network on the Arithmetic Logic Unit allows full look-ahead over the first sixteen bits of a word and ripple block carry between subsequent word increments of 12 bits. This ripple block carry method of cascading units is accomplished by having the ($\overline{COE}$) carry out enable input HIGH at the most significant unit in each block so as to give a carry out signal from the carry out/carry generate output. This carry out signal is then used as the carry in signal to the next block. The COE inputs for all other units are tied to ground.

The Am93L40 can be used with either active LOW or active HIGH data inputs. In the active HIGH case the look-ahead carry inputs and outputs are not carry generate and carry propagate, but are labelled C_X and C_Y respectively. They are still connected in the same manner as the active LOW case.

LOGIC SYMBOL



V_{CC} = PIN 24
GND = PIN 12

LOADING RULES

In Unit Loads (Notes)

	TTL LOADS		93L LOADS	
Input Load Factor	HIGH	LOW	HIGH	LOW
S_0, S_1, $\overline{CP}_{-1}$, $\overline{CP}_{-2}$, $\overline{CG}_{-3}$	0.5	0.25	1.0	1.0
$\overline{COE}$	0.5	0.375	1.0	1.5
$\overline{CG}_{-2}$	1.0	0.5	2.0	2.0
All $\overline{A}$, all $\overline{B}$, $\overline{CG}_{-1}$	1.5	0.75	3.0	3.0
Output Drive	HIGH	LOW	HIGH	LOW
All outputs	10	3	20	12

NOTES:
1) A TTL unit load is specified as 0.4 V at −1.6 mA LOW, 2.4 V at 40 μA HIGH.
2) A 93L unit load is specified as 0.3 V at −400 μA LOW, 2.4 V at 20 μA HIGH.
3) Enough output LOW current is available to mix TTL and 93L loads and still meet the 93L requirement of a V_{OL} of 0.3 V.

OPERATION TABLE

Control Inputs		Active LOW Inputs and Outputs	Active HIGH Inputs and Outputs
S_0	S_1	Function	Function
L	L	A SUBTRACT B	A SUBTRACT B
H	L	A ADD B	A ADD B
L	H	A EXCLUSIVE OR B	A EQUIVALENCE B
H	H	A AND B	A OR B

Note: Arithmetic operations (S_1 = L) are performed on a word basis; logic operations (S_1 = H) are performed on a bit basis.

Am93L40 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
24-Pin Molded DIP	0°C to +75°C	AM93L4059C
24-Pin Hermetic DIP	0°C to +75°C	U6N93L4059X
24-Pin Hermetic DIP	−55°C to +125°C	U6N93L4051X
24-Pin Hermetic Flat Pak	−55°C to +125°C	U4M93L4051X
Dice	Note	UXX93L40XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature range.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current (Note 1)	−30 mA to +5.0 mA

Note 1. Maximum current defined by DC input voltage.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93L3859X $T_A = 0°C$ to $+75°C$ $V_{CC} = 4.75$ V to 5.25 V
Am93L3851X $T_A = -55°C$ to $+125°C$ $V_{CC} = 4.50$ V to 5.50 V

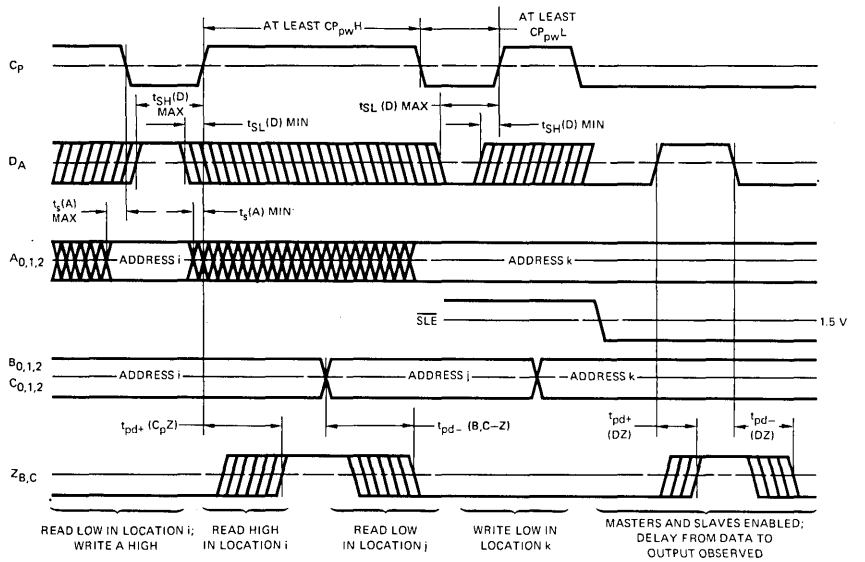
Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -0.24$ mA $V_{IN} = V_{IH}$ or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $I_{OL} = 4.92$ mA $V_{IN} = V_{IH}$ or V_{IL}		0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.7	Volts
I_{IL} (Note 2)	93L Unit Load Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.3$ V		−0.25	−0.4	mA
I_{IH} (Note 2)	93L Unit Load Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.4$ V		2.0	20	μA
	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 5.5$ V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., $V_{OUT} = 0.0$ V	−2.5		−25	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		16	33	mA

Notes: 1) Typical limits are at $V_{CC} = 5.0$ V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by the 93L input load factor. (See loading rules)

SWITCHING CHARACTERISTICS ($T_A = 25°C$) ($V_{CC} = 5.0$ V, $C_L = 15$ pF)

Parameters		Test Conditions	Min	Typ	Max	Units
t_{pd+}	Turn Off Delay CP to Output	$A_{0,1,2} = B_{0,1,2} = C_{0,1,2}$	23	45	68	ns
t_{pd-}	Turn On Delay CP to Output		22	41	63	ns
t_{pd+} (D_A-Z)	Turn Off Delay Data to Output	$\overline{SLE}$ = L	45	85	130	ns
t_{pd-} (D_A-Z)	Turn On Delay Data to Output		55	100	156	ns
t_{pd+} (B,C-Z)	Turn Off Delay Address to Output	C_P = H	20	50	78	ns
t_{pd-} (B,C-Z)	Turn On Delay Address to Output		50	125	195	ns
t_{sH} (D_A)	Set Up Time HIGH Data		20	49	75	ns
t_{sL} (D_A)	Set Up Time LOW Data		18	31	47	ns
t_s (A)	Set Up Time, Address Inputs		18	38	75	
CP_{pw} 'L'	Minimum LOW Clock Pulse Width			24	37	ns
CP_{pw} 'H'	Minimum HIGH Clock Pulse Width			22	34	

SWITCHING TIME WAVEFORMS



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Am9341-Am54/74181

Four Bit Arithmetic Logic Unit/Function Generator

Distinctive Characteristics:

- Provides 16 arithmetic operations including add, subtract, double and compare.
- Provides ALL 16 possible logic operations of two variables in typically 19 ns.
- Typical add time for 4 bits of only 19 ns, and typical carry time of 12 ns.
- Full look-ahead for high-speed arithmetic operation on long words.
- 100% reliability assurance testing in compliance with MIL STD 883.
- Mixing privileges for obtaining price discounts. Refer to price list.

FUNCTIONAL DESCRIPTION

The Am54/74181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU)/Digital Function Generator. When the mode control (M) is held LOW the circuit performs under control of four function select lines 16 arithmetic operations, the most important being add and subtract, on two 4-bit parallel binary words. When the mode control is held HIGH the circuit performs, under control of the four function select lines sixteen logic operations on an individual bit basis between the two four-bit parallel words.

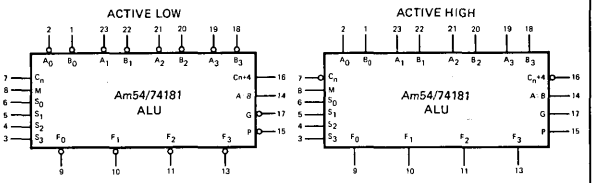
An open collector A = B output is provided so that equivalence of two parallel words can be made by connecting A = B outputs of several ALU's together.

An internal full look-ahead carry scheme is used for high-speed arithmetic operations and provision made for further look-ahead by providing carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs. These carry signals can be used as inputs to the Am54/74182 look-ahead carry generator to form long word length high-speed parallel arithmetic logic units. Addition time for sixteen-bit words with four Am54/74181 ALU's and one Am 54/74182 look-ahead generator is only 31 ns.

For systems where ultra high-speed is not required, the carry output signal (C_{n+4}) can be used to provide ripple-block arithmetic operations.

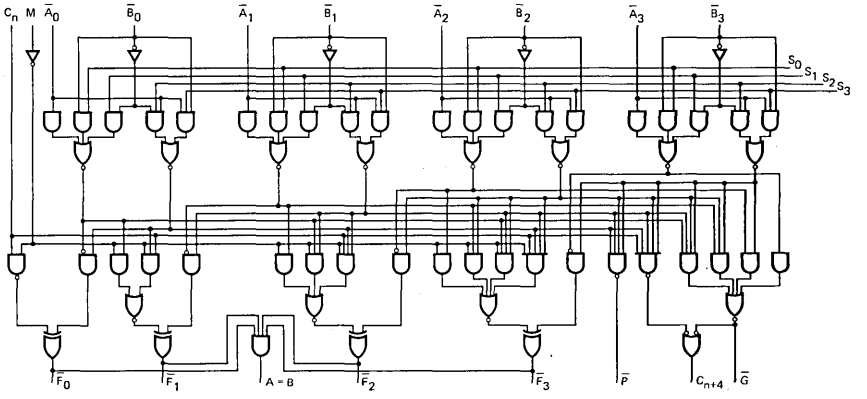
The ALU can be used with either active HIGH or active LOW inputs and can also be expanded with the Am54/74182 look-ahead carry generator in either mode. The interconnection patterns are identical for both cases.

LOGIC SYMBOLS



V_{CC} = PIN 24
GND = PIN 12

LOGIC DIAGRAM

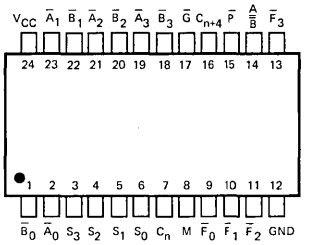


Am54/74181-Am9341 ORDERING INFORMATION

Package Type	Temperature Range	54/74181 Order Number	9341 Order Number
Molded DIP	0°C to +75°C	SN74181N	Am9341C
Hermetic DIP	0°C to +75°C	SN74181J	U6N934159X
Hermetic DIP	−55°C to +125°C	SN54181J	U6N934151X
Hermetic Flat Pak	−55°C to +125°C	SN54181W	U4M934151X
Dice	Note	SN54181D	UXX9341XXD

NOTE: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise noted)

Am74181	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5% (COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am54181	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10% (MIL)	MIN. = 4.5V	MAX. = 5.5V

Parameters	Description		Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage (Except A=B Output)		V_{CC} = MIN., I_{OH} = −800μA V_{IN} = V_{IH} or V_{IL}			2.4	3.4		Volts
V_{OL}	Output LOW Voltage		V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}				0.2	0.4	Volts
V_{IH}	Input HIGH Level		Guaranteed input logical HIGH voltage for all inputs			2			Volts
V_{IL}	Input LOW Level		Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage		V_{CC} = MIN., I_{IN} = −12mA					−1.5	Volts
I_{OH}	Output HIGH Current for A=B Output		V_{CC} = MIN., V_{OH} = 5.5V V_{IN} = V_{IH} or V_{IL}					250	μA
I_{IL} (Note 3)	Input LOW Current	M	V_{CC} = MAX., V_{IN} = 0.5V					−1.6	mA
		$\overline{A_i}$ or $\overline{B_i}$						−4.8	
		S_i						−6.4	
		C_n						−8	
I_{IH} (Note 3)	Input HIGH Current	M	V_{CC} = MAX., V_{IN} = 2.7V					40	μA
		$\overline{A_i}$ or $\overline{B_i}$						120	
		S_i						160	
		C_n						200	
I_I	Input HIGH Current		V_{CC} = MAX., V_{IN} = 5.5V					1	mA
I_{SC}	Output Short Circuit Current (Note 4) (Except A=B Output)		V_{CC} = MAX.		Am54	−20		−55	mA
					Am74	−18		−57	
I_{CC}	Power Supply Current		V_{CC} = MAX.	Note 5 A	Am54		88	127	mA
					Am74		88	140	
				Note 5 B	Am54		94	135	
					Am74		94	150	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25° C ambient and maximum loading.
3. Actual input currents = United Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} is measured under two conditions.
   A. S_i, M, A_i at 4.5V; all other inputs grounded; outputs open
   B. S_i, M at 4.5V; all other inputs grounded; outputs open.

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS:

$\overline{A}_i$ Active LOW Data A inputs i = 0, 1, 2, 3.

A = B Open collector output. This output can be 'AND tied' to other A = B outputs to form equivalence over complete word length.

$\overline{B}_i$ Active LOW Data B inputs i = 0, 1, 2, 3.

C_n Active HIGH Carry In to nth ALU bit.

C_{n+4} Active HIGH Carry Out of n+4th ALU bit.

$\overline{F}_i$ Active LOW Data Outputs of ALU i = 0, 1, 2, 3.

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

$\overline{G}$ Active LOW carry generate output for use in multi-level look-ahead schemes.

M Mode input controls whether arithmetic or logic operation.

$\overline{P}$ Active LOW carry propagate output for use in multi-level look-ahead schemes.

S_i Control inputs determine the arithmetic or logic function obeyed i = 0, 1, 2, 3.

Unit Load One T^2L gate input load. In the HIGH state it is equal to 40μA at 2.4V and in the LOW state it is equal to 1.6mA at 0.4V

OPERATIONAL TERMS:

I_{IL} Forward input load current, for unit input load.

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{IH} Reverse input load current with V_{OH} applied to input.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage. Refer to figure 3.

V_{IL} Maximum logic LOW input voltage. Refer to figure 3.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

TEST TABLES

DIFF MODE TEST TABLE

FUNCTION INPUTS: $S_1 = S_2 = 4.5$ V, $S_0 = S_3 = M = 0$ V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5 V	Apply 0 V	Apply 4.5 V	Apply 0 V		
t_{pd+} / t_{pd-}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$F_j (j \geq i)$	1
t_{pd+} / t_{pd-}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$F_j (j \geq i)$	2
t_{pd+} / t_{pd-}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_{i+1}$	1
t_{pd+} / t_{pd-}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_{i+1}$	2
t_{pd+} / t_{pd-}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	1
t_{pd+} / t_{pd-}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	2
t_{pd+} / t_{pd-}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	1
t_{pd+} / t_{pd-}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	2
t_{pd+} / t_{pd-}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	1
t_{pd+} / t_{pd-}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	2
t_{pd+} / t_{pd-}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}	2
t_{pd+} / t_{pd-}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}	1
t_{pd+} / t_{pd-}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4}	1

Table 1

SUM MODE TEST TABLE

FUNCTION INPUTS: $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = M = 0$ V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5 V	Apply 0 V	Apply 4.5 V	Apply 0 V		
t_{pd+} / t_{pd-}	A_i	B_i	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$F_j (j \geq i)$	1
t_{pd+} / t_{pd-}	B_i	A_i	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$F_j (j \geq i)$	1
t_{pd+} / t_{pd-}	$\overline{A}_i$	$\overline{B}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_{i+1}$	1
t_{pd+} / t_{pd-}	$\overline{B}_i$	$\overline{A}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_{i+1}$	1
t_{pd+} / t_{pd-}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	1
t_{pd+} / t_{pd-}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	1
t_{pd+} / t_{pd-}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	1
t_{pd+} / t_{pd-}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	1
t_{pd+} / t_{pd-}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	2
t_{pd+} / t_{pd-}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	2
t_{pd+} / t_{pd-}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}	1

Table 2

LOGIC MODE TEST TABLE

FUNCTION INPUTS: $S_1 = S_2 = M = 4.5$ V, $S_0 = S_3 = 0$ V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5 V	Apply 0 V	Apply 4.5 V	Apply 0 V		
t_{pd+} / t_{pd-}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	1
t_{pd+} / t_{pd-}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	1

Table 3

SWITCHING CHARACTERISTICS $V_{CC} = 5$ V, $T_A = 25°C$, N = 10 ($C_L = 15$ pF, $R_L = 400\ \Omega$)

Parameter	From (Input)	To (Output)	Test Figure	Test Conditions See also Tables 1, 2, 3	Min	Typ	Max	Units
t_{pd+} / t_{pd-}	C_n	C_{n+4}	1 and 2			12 13	18 19	ns
t_{pd+} / t_{pd-}	C_n	$\overline{F}_i$		M = 0 V (SUM or DIFF mode)		13 12	19 18	ns
t_{pd+} / t_{pd-}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{G}$		M = 0 V, $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = 0$ V (SUM mode)		13 13	19 19	ns
t_{pd+} / t_{pd-}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{G}$		M = 0 V, $S_0 = S_3 = 0$ V, $S_1 = S_2 = 4.5$ V (DIFF mode)		17 17	25 25	ns
t_{pd+} / t_{pd-}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{P}$		M = 0 V, $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = 0$ V (SUM mode)		13 15	19 22	ns
t_{pd+} / t_{pd-}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{P}$		M = 0 V, $S_0 = S_3 = 0$ V, $S_1 = S_2 = 4.5$ V (DIFF mode)		17 17	25 25	ns
t_{pd+} / t_{pd-}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_j$ ($j \geq i$)		M = 0 V, $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = 0$ V (SUM mode)		18 12	27 18	ns
t_{pd+} / t_{pd-}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_j$ ($j \geq i$)		M = 0 V, $S_0 = S_3 = 0$ V, $S_1 = S_2 = 4.5$ V (DIFF mode)		20 16	30 24	ns
t_{pd+} / t_{pd-}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_{i+1}$		M = 0 V, $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = 0$ V (SUM mode)		19 20	29 30	ns
t_{pd+} / t_{pd-}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_{i+1}$		M = 0 V, $S_0 = S_3 = 0$ V, $S_1 = S_2 = 4.5$ V (DIFF mode)		24 21	36 32	ns
t_{pd+} / t_{pd-}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$		M = 4.5 V (LOGIC mode)		19 19	29 29	ns
t_{pd+} / t_{pd-}	$\overline{A}_i$ or $\overline{B}_i$	C_{n+4}		M = 0 V, $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = 0$ V (SUM mode)		17 20	25 30	ns
t_{pd+} / t_{pd-}	$\overline{A}_i$ or $\overline{B}_i$	C_{n+4}		M = 0 V, $S_0 = S_3 = 0$ V, $S_1 = S_2 = 4.5$ V (DIFF mode)		21 20	32 30	ns
t_{pd+} / t_{pd-}	$\overline{A}_i$ or $\overline{B}_i$	A = B		M = 0 V, $S_0 = S_3 = 0$ V, $S_1 = S_2 = 4.5$ V (DIFF mode)		25 21	37 32	ns

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

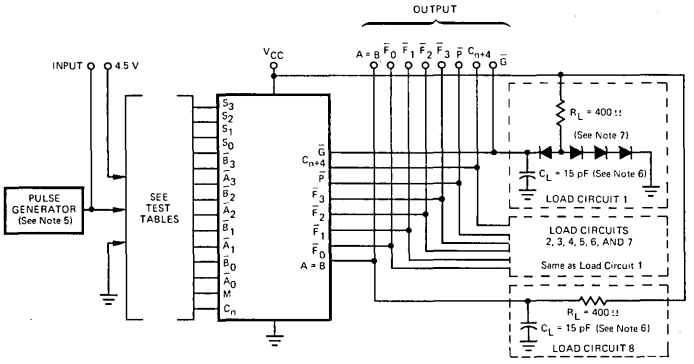


Figure 1

Note 5. The pulse generator has the following characteristics: frequency = 1 MHz, $Z_{out} \approx 50\ \Omega$.
6. C_L includes probe and jig capacitance.
7. All diodes are 1N3064.

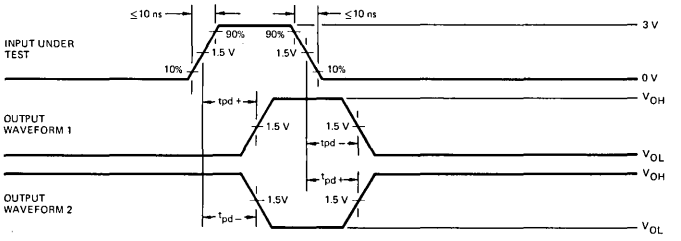
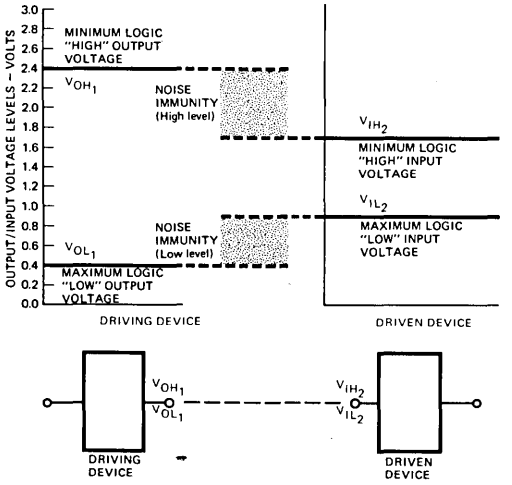


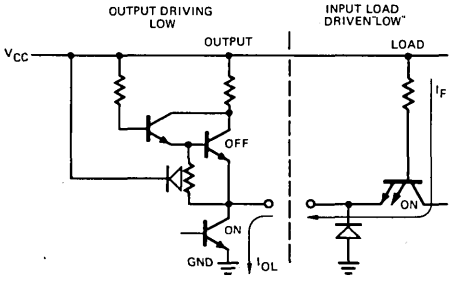
Figure 2

INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH



Current Interface Conditions — LOW



Current Interface Conditions — HIGH

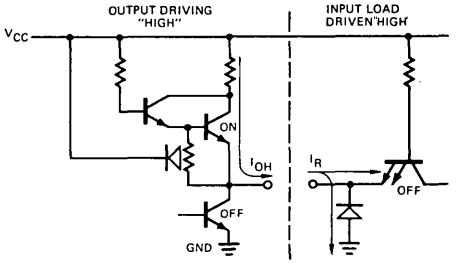


Figure 3

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 54/7400 Series	1	1
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Table 4

USER NOTES

1. Arithmetic operations are performed on a word basis.
2. Logic operations are performed on a bit basis.
3. Arithmetic in 1's complement arithmetic requires an end around carry.
4. Subtraction in 2's complement arithmetic requires a carry in (C_n = HIGH) active LOW case, ($\overline{C}_n$ = LOW) active HIGH case.

Am54/74181 LOADING RULES (in unit loads)

Input/Output	Pin No.'s	Input Unit Load	Output Drive Output HIGH	Output LOW
$\overline{B}_0$	1	3	—	—
$\overline{A}_0$	2	3	—	—
S_3	3	4	—	—
S_2	4	4	—	—
S_1	5	4	—	—
S_0	6	4	—	—
C_n	7	5	—	—
M	8	1	—	—
$\overline{F}_0$	9	—	20	10
$\overline{F}_1$	10	—	20	10
$\overline{F}_2$	11	—	20	10
GND	12	—	—	—
$\overline{F}_3$	13	—	20	10
A = B	14	—	O/C	10
$\overline{P}$	15	—	20	10
C_{n+4}	16	—	20	10
$\overline{G}$	17	—	20	10
$\overline{B}_3$	18	3	—	—
$\overline{A}_3$	19	3	—	—
$\overline{B}_2$	20	3	—	—
$\overline{A}_2$	21	3	—	—
$\overline{B}_1$	22	3	—	—
$\overline{A}_1$	23	3	—	—
V_{CC}	24	—	—	—

O/C = Open Collector

A unit load is defined as 40μA at 2.4V and 1.6mA at 0.4V.

Table 5

OPERATION TABLE

Control Inputs				Active LOW Inputs and Outputs		Active HIGH Inputs and Outputs	
S_0	S_1	S_2	S_3	Arithmetic (M = L, C_n = L)	Logic (M = H)	Arithmetic (M = L, $\overline{C}_n$ = H)	Logic (M = H)
L	L	L	L	A minus 1	$\overline{A}$	A	$\overline{A}$
H	L	L	L	AB minus 1	$\overline{AB}$	A + B	$\overline{A+B}$
L	H	L	L	A$\overline{B}$ minus 1	$\overline{A}+B$	A + $\overline{B}$	$\overline{A}B$
H	H	L	L	minus 1 (2's comp.)	Logic '1'	minus 1 (2's comp.)	Logic '0'
L	L	H	L	A plus [A + $\overline{B}$]	$\overline{A+B}$	A plus A$\overline{B}$	$\overline{AB}$
H	L	H	L	AB plus [A + $\overline{B}$]	$\overline{B}$	A$\overline{B}$ plus [A + B]	$\overline{B}$
L	H	H	L	A minus B minus 1	$\overline{A \oplus B}$	A minus B minus 1	A $\oplus$ B
H	H	H	L	A + $\overline{B}$	A + $\overline{B}$	A$\overline{B}$ minus 1	A$\overline{B}$
L	L	L	H	A plus [A + B]	$\overline{A}B$	A plus AB	$\overline{A}+B$
H	L	L	H	A plus B	A $\oplus$ B	A plus B	$\overline{A \oplus B}$
L	H	L	H	A$\overline{B}$ plus [A + B]	B	AB plus [A + $\overline{B}$]	B
H	H	L	H	A + B	A + B	AB minus 1	AB
L	L	H	H	A plus A (2 x A)	Logic '0'	A plus A (2 x A)	Logic '1'
H	L	H	H	A plus AB	A$\overline{B}$	A plus [A + B]	A + $\overline{B}$
L	H	H	H	A plus A$\overline{B}$	AB	A plus [A + $\overline{B}$]	A + B
H	H	H	H	A	A	A minus 1	A

L = LOW Voltage Level
H = HIGH Voltage Level

Table 6

Am54/74181 APPLICATIONS

16-Bit ALU Ripple Carry

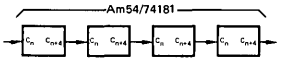


Figure 4

32-Bit ALU Two-Level Look-Ahead Over 16-Bit Groups

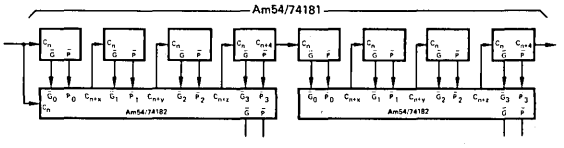


Figure 5

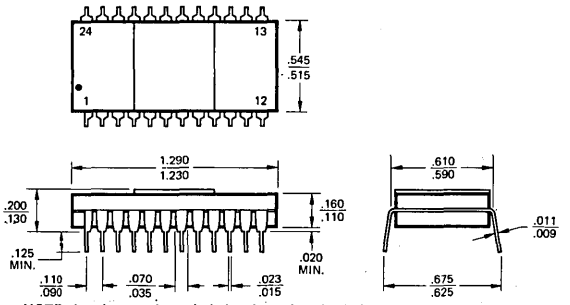
Typical addition times for various configurations are given in the table below. Subtraction times are approximately 5 ns longer.

TYPICAL ADDITION TIMES

No. of Bits	Total Addition Time (ns)	Add Time Per Bit (ns)	Package Count	
			Am 54/74181	Am 54/74182
4	19	4.8	1	
8	31	3.9	2	
12	43	3.6	3	
12	31	2.6	3	1
16	55	3.5	4	
16	31	2.0	4	1
32	103	3.2	8	
32	79	2.5	8	1
32	56	1.8	8	2
48	151	3.2	12	
48	127	2.6	12	1
48	104	2.2	12	2
48	81	1.7	12	3
48	57	1.2	12	4
64	199	3.1	16	
64	152	2.4	16	2
64	129	2.0	16	3
64	106	1.7	16	4
64	57	0.9	16	5

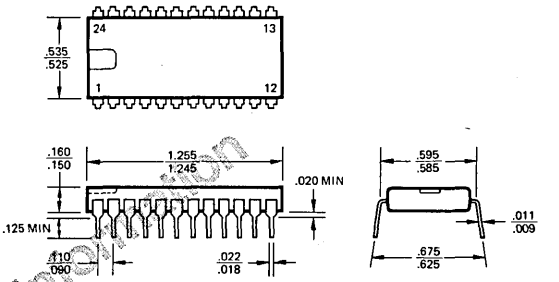
Table 7

PHYSICAL DIMENSIONS
Hermetic Dual-In-Line

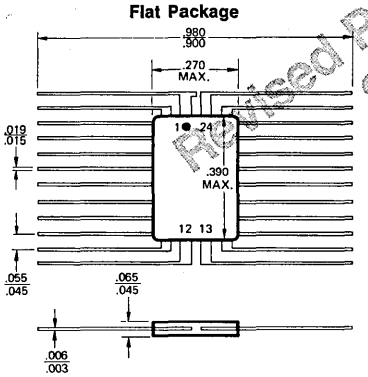


NOTE: Leads are intended for insertion in hole rows on .600" centers and are misaligned to facilitate insertion.

PHYSICAL DIMENSIONS
Molded Dual-In-Line



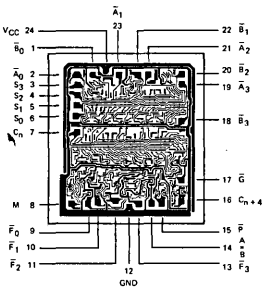
PHYSICAL DIMENSIONS
Flat Package



NOTE: Leads are gold plated kovar.

Metallization and Pad Layout

90 x 102 Mils



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Am93L41

Low-Power Four Bit Arithmetic Logic Unit/Function Generator

Distinctive Characteristics

125 mw typical power dissipation.

Typical add time for 4 bits of only 48 ns.

- 100% reliability assurance testing in compliance with MIL STD 883.
- Provides all 16 possible logic operations of two variables typically in 42 ns.

FUNCTIONAL DESCRIPTION

The Am93L41 is a 4-bit high-speed parallel arithmetic logic unit (ALU)/digital function generator. When the mode control (M) is held LOW the circuit performs under control of four function select lines 16 arithmetic operations, the most important being add and subtract, on two 4-bit parallel binary words. When the mode control is held HIGH the circuit performs, under control of the four function select lines sixteen logic operations on an individual bit basis between the two four-bit parallel words.

An open collector A = B output is provided so that equivalence of two parallel words can be made by connecting A = B outputs of several ALU's together.

An internal full look-ahead carry scheme is used for high-speed arithmetic operations and provision is made for further look-ahead by providing carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs. These carry signals can be used as inputs to the Am9342 look-ahead carry generator to form long word length high speed parallel arithmetic logic units.

For systems where ultra high speed is not required, the carry output signal (C_{n+4}) can be used to provide ripple block arithmetic operations. The ALU can be used with either Active HIGH or Active LOW inputs and can be expanded with the Am9342 look-ahead carry generator in either mode. The interconnection patterns are identical for both cases.

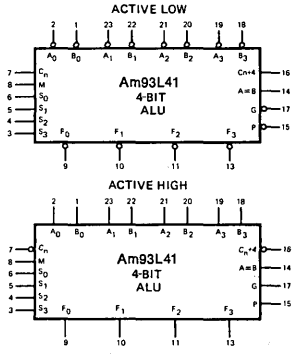
LOADING RULES

In Unit Loads (Notes)

	TTL LOADS		93L LOADS	
Input Load Factor	HIGH	LOW	HIGH	LOW
M	0.5	0.25	1.0	1.0
all $\overline{A}$, all $\overline{B}$	1.5	0.75	3.0	3.0
S_0, S_1, S_2, S_3	2.0	1.0	4.0	4.0
C_n	2.5	1.25	5.0	5.0
Output Drive	HIGH	LOW	HIGH	LOW
$\overline{F}_0$, $\overline{F}_1$, $\overline{F}_2$, $\overline{F}_3$, $\overline{G}$, $\overline{P}$, C_{n+4}	10	3	20	12
A = B	O/C	3	O/C	12

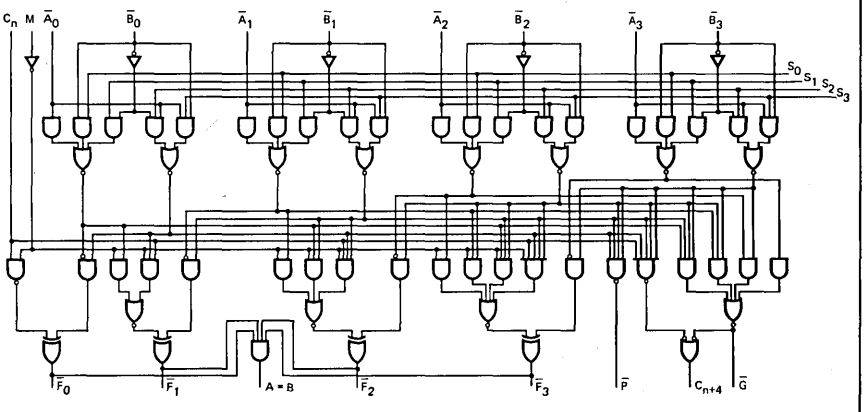
NOTES:
1) A TTL unit load is specified as 0.4 V at −1.6 mA LOW, 2.4 V at 40 μA HIGH.
2) A 93L unit load is specified as 0.3 V at −400 μA LOW, 2.4 V at 20 μA HIGH.
3) Enough output LOW current is available to mix TTL and 93L loads and still meet the 93L requirement of a V_{OL} of 0.3 V.

LOGIC SYMBOL



V_{CC} = PIN 24
GND = PIN 12

LOGIC DIAGRAM



Am93L41 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
24-Pin Molded DIP	0°C to +75°C	Am93L4159C
24-Pin Hermetic DIP	0°C to +75°C	U6N93L4159X
24-Pin Hermetic DIP	−55°C to +125°C	U6N93L4151X
24-Pin Hermetic Flat Pak	−55°C to +125°C	U4M93L4151X
Dice	Note	UXX93L41XXD

Revised Ordering Information See Note 9

NOTE: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current (Note 1)	−30 mA to +5.0 mA

Note 1. Maximum current defined by DC input voltage.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93L4159X $T_A = 0°C$ to $+75°C$ $V_{CC} = 4.75$ V to 5.25 V
Am93L4151X $T_A = -55°C$ to $+125°C$ $V_{CC} = 4.50$ V to 5.50 V

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -0.4$ mA $V_{IN} = V_{IH}$ or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $I_{OL} = 4.92$ mA $V_{IN} = V_{IH}$ or V_{IL}		0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.7	Volts
I_{IL} (Note 2)	93L Unit Load Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.3$ V		−0.25	−0.4	mA
I_{IH} (Note 2)	93L Unit Load Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.4$ V		2.0	20	μA
	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 5.5$ V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., $V_{OUT} = 0.0$ V	−4.5	−10	−15	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		25	40	mA

Notes: 1) Typical limits are at $V_{CC} = 5.0$ V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by the 93L input load factor. (See loading rules)

SWITCHING CHARACTERISTICS $V_{CC} = 5$ V, $T_A = 25°C$,

Parameter	From (Input)	To (Output)	Test Conditions	Min	Typ	Max	Units
t_{pd+}	C_n	C_{n+4}		18	36	54	ns
t_{pd-}				12	23	35	
t_{pd+}	C_n	any $\overline{F}$ (Note 3)	M = 0 V (SUM or DIFF mode)	16	31	47	ns
t_{pd-}				12	34	36	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{G}$	M = 0 V, $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = 0$ V (SUM mode)	16	31	47	ns
t_{pd-}				12	23	35	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{G}$	M = 0 V, $S_0 = S_3 = 0$ V, $S_1 = S_2 = 4.5$ V (DIFF mode)	18	35	53	ns
t_{pd-}				13	26	39	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{P}$	M = 0 V, $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = 0$ V (SUM mode)	18	35	53	ns
t_{pd-}				13	26	39	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{P}$	M = 0 V, $S_0 = S_3 = 0$ V, $S_1 = S_2 = 4.5$ V (DIFF mode)	19	37	56	ns
t_{pd-}				17	34	51	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}$ (Note 3)	M = 0 V, $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = 0$ V (SUM mode)	24	48	72	ns
t_{pd-}				24	47	71	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}$ (Note 3)	M = 0 V, $S_0 = S_3 = 0$ V, $S_1 = S_2 = 4.5$ V (DIFF mode)	27	53	80	ns
t_{pd-}				27	52	79	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$	M = 4.5 V (LOGIC mode)	19	38	57	ns
t_{pd-}				23	46	69	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	C_{n+4}	M = 0 V, $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = 0$ V (SUM mode)	20	40	60	ns
t_{pd-}				22	44	66	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	C_{n+4}	M = 0 V, $S_0 = S_3 = 0$ V, $S_1 = S_2 = 4.5$ V (DIFF mode)	22	44	66	ns
t_{pd-}				25	49	74	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	A = B	M = 0 V, $S_0 = S_3 = 0$ V, $S_1 = S_2 = 4.5$ V (DIFF mode)	27	53	80	ns
t_{pd-}				25	50	75	

Note 3: F_3 output is worst case.

OPERATION TABLE

Control Inputs	Active LOW Inputs and Outputs		Active HIGH Inputs and Outputs	
S_0 S_1 S_2 S_3	Arithmetic (M = L, C_n = L)	Logic (M = H)	Arithmetic (M = L, $\overline{C}_n$ = H)	Logic (M = H)
L L L L	A minus 1	$\overline{A}$	A	$\overline{A}$
H L L L	AB minus 1	$\overline{AB}$	A + B	$\overline{A+B}$
L H L L	$A\overline{B}$ minus 1	$\overline{A}+B$	$A+\overline{B}$	$\overline{AB}$
H H L L	minus 1 (2's comp.)	Logic '1'	minus 1 (2's comp.)	Logic '0'
L L H L	A plus $[A+\overline{B}]$	$\overline{A}+B$	A plus $A\overline{B}$	$\overline{AB}$
H L H L	AB plus $[A+\overline{B}]$	$\overline{B}$	$A\overline{B}$ plus [A + B]	$\overline{B}$
L H H L	A minus B minus 1	$\overline{A \oplus B}$	A minus B minus 1	$A \oplus B$
H H H L	$A+\overline{B}$	$A+\overline{B}$	$A\overline{B}$ minus 1	$A\overline{B}$
L L L H	A plus [A + B]	$\overline{AB}$	A plus AB	$\overline{A}+B$
H L L H	A plus B	$A \oplus B$	A plus B	$\overline{A \oplus B}$
L H L H	$A\overline{B}$ plus [A + B]	B	AB plus $[A+\overline{B}]$	B
H H L H	A + B	A + B	AB minus 1	AB
L L H H	A plus A (2 x A)	Logic '0'	A plus A (2 x A)	Logic '1'
H L H H	A plus AB	$A\overline{B}$	A plus $[A+\overline{B}]$	$A+\overline{B}$
L H H H	A plus $A\overline{B}$	AB	A plus $[A+\overline{B}]$	A + B
H H H H	A	A	A minus 1	A

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Am9342-Am54/74182
Look-Ahead Carry Generator

Distinctive Characteristics:

- Provides look-ahead carries across a group of four ALU's
- Capability of multi-level look-ahead for high-speed arithmetic operation over large word lengths
- Typical carry propagation delay of 13 ns
- 100% reliability assurance testing in compliance with MIL STD 883.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Available in highly reliable molded epoxy, hermetic dual-in-line or Hermetic flat package.

FUNCTIONAL DESCRIPTION

The Am54/74182 is a high-speed look-ahead carry generator which accepts up to four pairs of active LOW carry propagate and carry generate signals and an active HIGH carry input and provides anticipated active HIGH carries across four groups of binary adders. The device also has active LOW carry propagate and carry generate outputs which may be used for further levels of look-ahead.

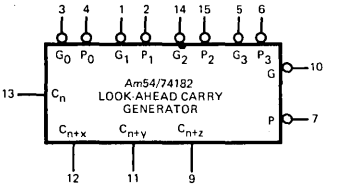
The Am54/74182 is generally used with the Am54/74181 arithmetic logic unit to provide look-ahead over word lengths of more than four bits.

The look-ahead carry generator can be used with binary ALUs in an active LOW or active HIGH input operand mode by reinterpreting the carry functions. The connections to and from the ALU to the look-ahead carry generator are identical in both cases.

The logic equations provided at the outputs are:

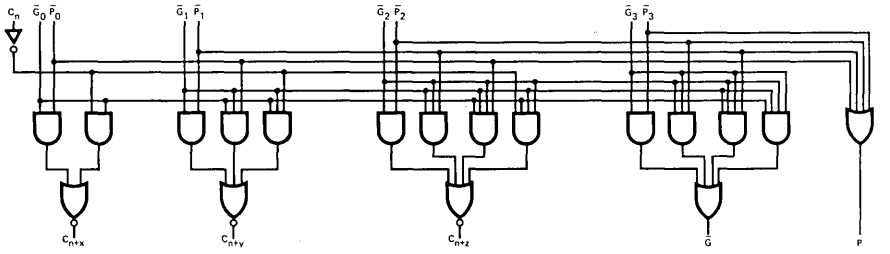
$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + + P_2P_1P_0C_n$$
$$G = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$$
$$P = P_3P_2P_1P_0$$

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

LOGIC DIAGRAM

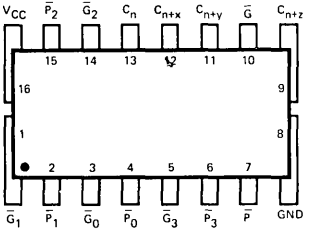


Am54/74182 Am9342 ORDERING INFORMATION

Package Type	Temperature Range	Am54/74182 Order Number	9342 Order Number
Molded DIP	0°C to +75°C	SN74182N	Am9342C
Hermetic DIP	0°C to +75°C	SN74182J	U6N934259X
Hermetic DIP	−55°C to +125°C	SN54182J	U7B934251X
Hermetic Flat Pak	−55°C to +125°C	SN54182S	U4L934251X
Dice	Note	SN54182D	UXX9342XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am74182, Am934259X T_A = 0°C to +75°C V_{CC} = 5.0 V ±5%
Am54182, Am934251X T_A = −55°C to +125°C V_{CC} = 5.0 V ±10%

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.8 mA V_{IN} = V_{IH} or V_{IL}		2.4	2.9		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16.0 mA V_{IN} = V_{IH} or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V			−1.0	−1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V			10	40	µA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX All outputs LOW	Am54182		45	65	mA
			Am74182		45	72	
		V_{CC} = MAX All outputs HIGH	Am54182		27		mA
			Am74182		27		

Notes: 1) Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by input load factor (See Loading Rules).

SWITCHING CHARACTERISTICS V_{CC} = 5 V, T_A = 25°C, N = 10 (C_L = 15 pF, R_L = 400 Ω)

Parameter	From (Input)	To (Output)	Test Figure	Test Conditions	Min	Typ	Max	Units
t_{pd+}	C_n	C_{n+i}	2	$\overline{P}_0 = \overline{P}_1 = \overline{P}_2 = 0$ V $\overline{G}_0 = \overline{G}_1 = \overline{G}_2 = 4.5$ V		12	17	ns
t_{pd-}						15	22	
t_{pd+}	$\overline{P}_i$	C_{n+i}	3	$\overline{P}_j = 0$ V (j < i) $C_n = \overline{G}_0 = \overline{G}_1 = \overline{G}_2 = 4.5$ V		8	12	ns
t_{pd-}						9	13	
t_{pd+}	$\overline{G}_i$	C_{n+i}	3	$\overline{G}_j = 0$ V (j < i) $C_n = \overline{P}_0 = \overline{P}_1 = \overline{P}_2 = 4.5$ V		8	12	ns
t_{pd-}						9	13	
t_{pd+}	$\overline{P}_i$	$\overline{G}$ or $\overline{P}$	2	$\overline{P}_j = 0$ V (j < i) $C_n = \overline{G}_0 = \overline{G}_1 = \overline{G}_2 = 4.5$ V		12	17	ns
t_{pd-}						15	22	
t_{pd+}	$\overline{G}_i$	$\overline{G}$	2	$\overline{G}_j = 0$ V (j < i) $C_n = \overline{P}_0 = \overline{P}_1 = \overline{P}_2 = 4.5$ V		12	17	ns
t_{pd-}						15	22	

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS:

C_n Active HIGH Carry In to the n'th ALU.

C_{n+i} Active HIGH Carry Out to the (n+i)th ALU; i = x, y, z.

FANOUT The logic HIGH or LOW output drive capability in terms of input Unit Loads.

$\overline{G}$ Active LOW Carry Generate over the $\overline{P}_i$, $\overline{G}_i$ inputs. This output is used with $\overline{P}$ at the next level of look-ahead.

$\overline{G}_i$ Active LOW Carry Generate inputs to the look-ahead generator; i = 0,1,2,3.

$\overline{P}$ Active LOW Carry Propagate output over the $\overline{P}_i\overline{G}_i$ inputs. This output is used with $\overline{G}$ at the next level of look-ahead.

$\overline{P}_i$ Active LOW Carry Propagate inputs to the look-ahead generator; i = 0,1,2,3.

OPERATIONAL TERMS:

I_{IL} Forward input load current, for unit input load.

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{IH} Reverse input current with V_{OH} applied to input.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

SWITCHING TERMS:

t_{pd+} The propagation delay from a LOW to HIGH C_n or $\overline{P}_3$ input transition to a LOW to HIGH C_{n+x}, C_{n+y}, C_{n+z}, $\overline{G}$ or $\overline{P}$ output transition.

t_{pd-} The propagation delay from a HIGH to LOW C_n or $\overline{P}_3$ input transition to a HIGH to LOW C_{n+x}, C_{n+y}, C_{n+z}, $\overline{G}$ or $\overline{P}$ output transition.

SWITCHING TIME TEST CIRCUIT & WAVEFORMS

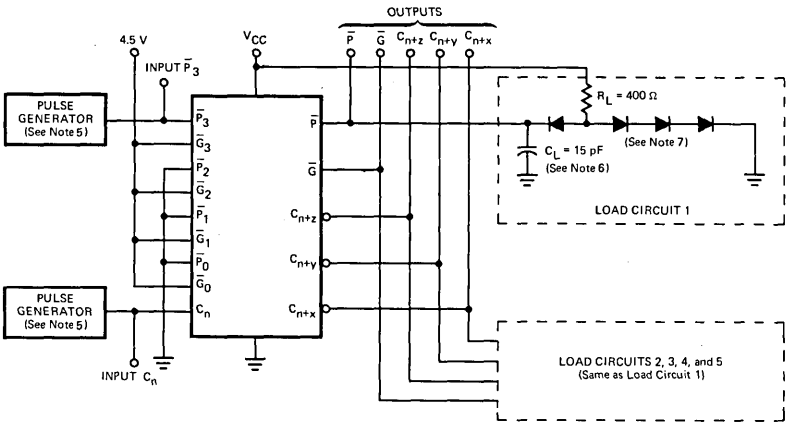


Figure 1

Note 5. The pulse generator has the following characteristics: Frequency = 1 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle = 50%.
6. C_L includes probe and jig capacitance.
7. All diodes are 1N3064.

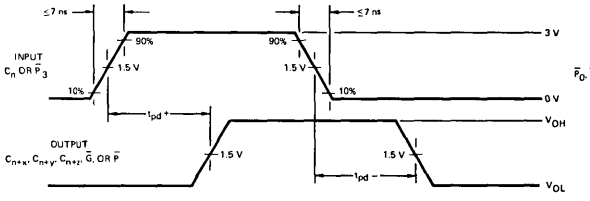


Figure 2

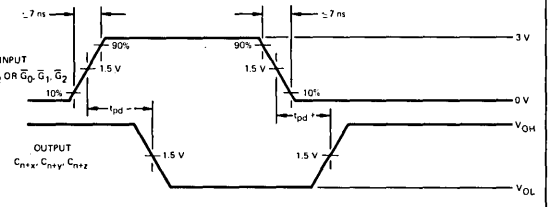
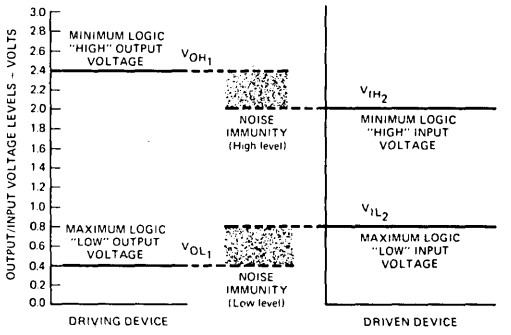
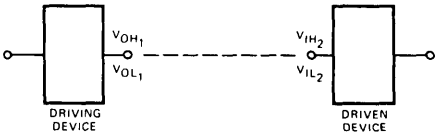


Figure 3

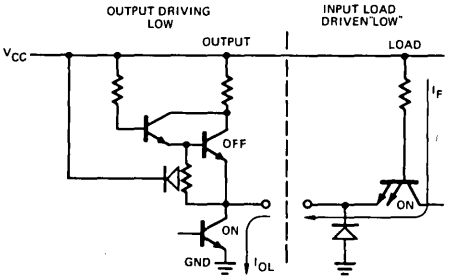
INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH





Current Interface Conditions — LOW



Current Interface Conditions — HIGH

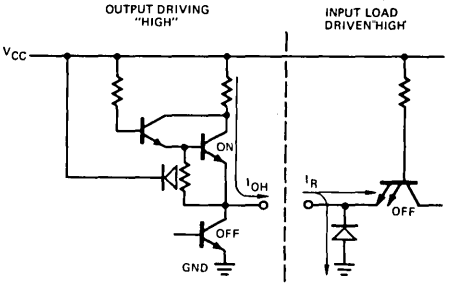


Figure 4

Am54/74182 TRUTH TABLE

Inputs									Outputs			
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	X	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	H	H	H					L		
X	X	H	H	H	H	X					L		
X	H	H	X	X	H	X					L		
L	H	X	H	X	L	X					L		
X	X	X	X	L	X	L					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	H	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		X	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

TABLE I

Am54/74182 LOADING RULES (in unit loads)

Input/Output	Pin No.'s	Input Unit Load	Output Drive HIGH	Output Drive LOW
$\overline{G}_1$	1	10	—	—
$\overline{P}_1$	2	5	—	—
$\overline{G}_0$	3	9	—	—
$\overline{P}_0$	4	5	—	—
$\overline{G}_3$	5	5	—	—
$\overline{P}_3$	6	3	—	—
$\overline{P}$	7	—	20	10
GND	8	—	—	—
C_{n+z}	9	—	20	10
$\overline{G}$	10	—	20	10
C_{n+y}	11	—	20	10
C_{n+x}	12	—	20	10
C_n	13	2	—	—
$\overline{G}_2$	14	9	—	—
$\overline{P}_2$	15	4	—	—
V_{CC}	16	—	—	—

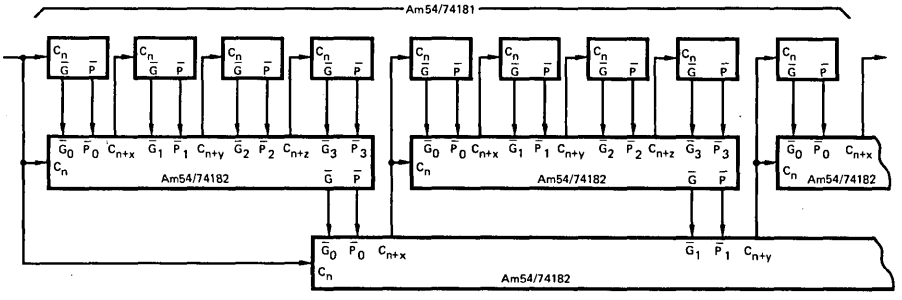
TABLE II

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	Equivalent Input Unit Load LOW
Advanced Micro Devices 54/7400	1	1
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

TABLE III

Am54/74182 APPLICATION

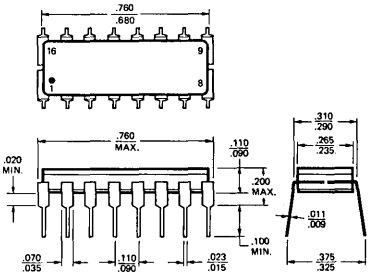


64-Bit ALU, Three Level Carry Look-Ahead

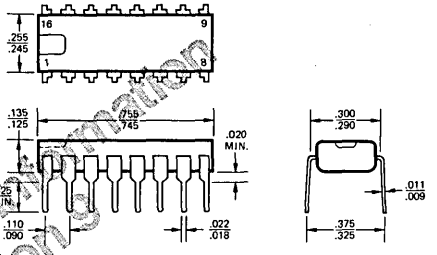
Figure 5

PHYSICAL DIMENSIONS
Dual-In-Line

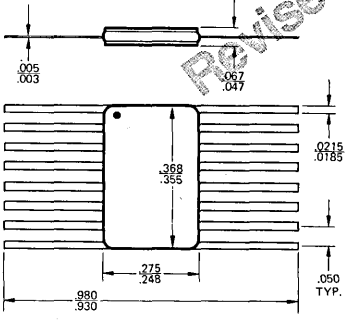
Hermetic



Molded

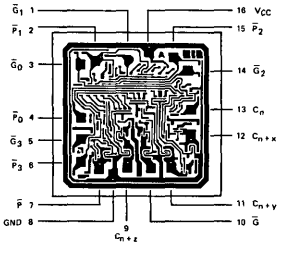


Flat Package



Metallization and Pad Layout

68 x 68 Mils



ADVANCED
MICRO
DEVICES INC.
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Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am9360 • Am54/74192
Am9366 • Am54/74193
Decimal and Hexadecimal Up/Down Counters

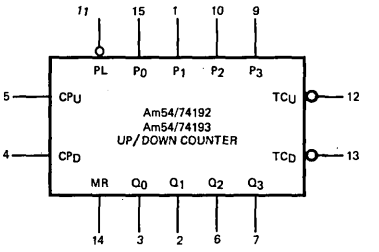
Distinctive Characteristics

- Separate up and down clocks
- Asynchronous parallel load
- 32 MHz typical count rate
- 100% reliability assurance testing in compliance with MIL STD 883

FUNCTIONAL DESCRIPTION

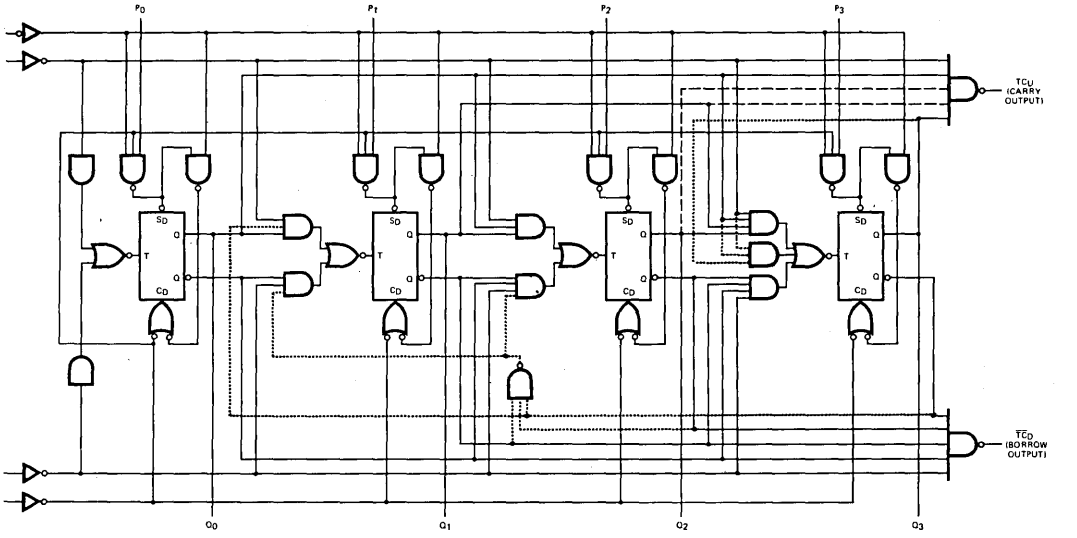
The Am54/74192 (Am9360) and Am54/74193 (Am9366) are 4-bit up-down counters. The 54/74192 counts in BCD code, and the 54/74193 in binary. The counters have separate count-up and count-down clock inputs (CP_U and CP_D). The outputs (Q_{0-3}) change synchronously following a LOW to HIGH transition on either clock input. Only one clock input can be LOW at a time or erroneous counting will result. Each of the four flip-flops can be preset to HIGH or LOW by means of the four parallel inputs, P_{0-3}. When the parallel load input ($\overline{PL}$) goes LOW, all four flip-flops set to the state of their P inputs irrespective of the clock inputs. An active HIGH master reset (MR) is provided that overrides both the clock and parallel load inputs, forcing all Q outputs LOW. Two terminal count outputs are gated with the clock inputs to provide clock signals to other counters. The $\overline{TC}_D$ output goes LOW when the counter is in state 0000 and the count-down clock goes LOW. The $\overline{TC}_U$ output goes LOW when the count-up clock goes LOW and the counter is in state 1001 (74192) or state 1111 (74193). The signals can drive directly the count-up and count-down clocks on the next counter in a series.

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

LOGIC DIAGRAM



Am54/74192 or Am9360 Decade Counter only .....
Am54/74193 or Am9366 Hexadecimal Counter only — — — — —

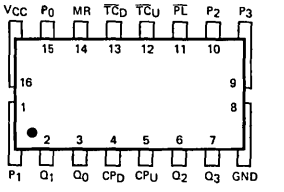
Am54/74192, 3 ORDERING INFORMATION

Package Type	Temperature Range	Am54/74192 Order Number	Am54/74193 Order Number	Am9360 Order Number	Am9366 Order Number
Molded DIP	0°C to +75°C	SN74192N	SN74193N	U6M936059X	U6M936659X
Hermetic DIP	0°C to +75°C	SN74192J	SN74193J	U7B936059X	U7B936659X
Hermetic DIP	−55°C to +125°C	SN54192J	SN54193J	U7B936051X	U7B936651X
Hermetic Flat Pak	−55°C to +125°C	SN54192W	SN54193W	U4L936051X	U4L936651X
Dice	Note	SN74192	SN74193	UXX9360XXD	UXX9366XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

Low-power versions of these circuits are available

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

SWITCHING CHARACTERISTICS V_{CC} = 5 V, T_A = 25°C,

Parameter	From (Input)	To (Output)	Test Conditions	Min	Typ	Max	Units
t_{pd+}	C_n	C_{n+4}		12	36	54	ns
t_{pd-}				12	23	35	
t_{pd+}	C_n	any $\overline{F}$ (Note 3)	M = 0 V (SUM or DIFF mode)	12	31	47	ns
t_{pd-}				12	34	36	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{G}$	M = 0 V, $S_0 = S_3$ = 4.5 V, $S_1 = S_2$ = 0 V (SUM mode)	12	31	47	ns
t_{pd-}				12	23	50	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{G}$	M = 0 V, $S_0 = S_3$ = 0 V, $S_1 = S_2$ = 4.5 V (DIFF mode)	12	35	53	ns
t_{pd-}				12	26	54	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{P}$	M = 0 V, $S_0 = S_3$ = 4.5 V, $S_1 = S_2$ = 0 V (SUM mode)	12	35	53	ns
t_{pd-}				12	26	39	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{P}$	M = 0 V, $S_0 = S_3$ = 0 V, $S_1 = S_2$ = 4.5 V (DIFF mode)	12	37	56	ns
t_{pd-}				12	34	51	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}$ (Note 3)	M = 0 V, $S_0 = S_3$ = 4.5 V, $S_1 = S_2$ = 0 V (SUM mode)	12	48	72	ns
t_{pd-}				12	47	71	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}$ (Note 3)	M = 0 V, $S_0 = S_3$ = 0 V, $S_1 = S_2$ = 4.5 V (DIFF mode)	12	53	80	ns
t_{pd-}				12	52	79	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$	M = 4.5 V (LOGIC mode)	12	38	57	ns
t_{pd-}				12	46	69	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	C_{n+4}	M = 0 V, $S_0 = S_3$ = 4.5 V, $S_1 = S_2$ = 0 V (SUM mode)	20	40	60	ns
t_{pd-}				20	44	66	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	C_{n+4}	M = 0 V, $S_0 = S_3$ = 0 V, $S_1 = S_2$ = 4.5 V (DIFF mode)	20	44	70	ns
t_{pd-}				20	49	74	
t_{pd+}	$\overline{A}_i$ or $\overline{B}_i$	A = B	M = 0 V, $S_0 = S_3$ = 0 V, $S_1 = S_2$ = 4.5 V (DIFF mode)	20	53	80	ns
t_{pd-}				20	50	75	

Note 3: F_3 output is worst case.

Switching Characteristics (T_A = 25°C)

Parameters	Definition	Test Conditions	Min	Typ	Max	Units
t_{pd+} (Q)	Delay from clock to Q output HIGH	C_L = 15 pF See Fig. 1	12	25	38	ns
t_{pd-} (Q)	Delay from clock to Q output LOW		15	31	47	ns
t_{pd+} ($\overline{TC}$)	Delay from up or down clock to corresponding TC output HIGH	C_L = 15 pF See Fig. 1	8	16	26	ns
t_{pd-} ($\overline{TC}$)	Delay from up or down clock to corresponding TC output LOW		8	16	24	ns
t_{pw} (CP)	Minimum clock LOW or HIGH time (Note 1)				20	ns
t_{pw} ($\overline{PL}$)	Minimum LOW time on $\overline{PL}$ input	See Fig. 2			25	ns
t_s (P)	Set up time, P inputs		0		20	ns
t_{pw} (MR)	Minimum HIGH time on master reset input	See Fig. 3			20	ns
t_{rec} (MR)	Master reset recovery time				20	ns
f_{max}	Maximum count frequency		25	32		MHz
t_{pd-} (MR)	Delay, master reset to outputs LOW	See Fig. 3		25	38	ns
t_{rec} ($\overline{PL}$)	Recovery time, parallel load input	See Fig. 2			20	ns

Notes 1) Either input must be LOW for t_{pw} (CP) and both inputs must be HIGH for t_{pw} (CP) between clocks.

DEFINITION OF TERMS

SUBSCRIPT TERMS

FUNCTIONAL TERMS

CP_U Count-up clock input. A LOW-to-HIGH edge on this input causes the contents of the counter to increment by one.

CP_D Count-down input. A LOW-to-HIGH edge on this input causes the contents of the counter to decrement by one.

Q_{0-3} The outputs of the four internal flip-flops. Q_0 is the least significant bit of the counter.

$\overline{PL}$ The parallel load control. When this input is LOW, the four flip-flops are forced into the states defined by the P inputs. The $\overline{PL}$ input overrides the clock, and causes a direct set or clear of the flip-flops.

P_{0-3} The parallel data inputs. When $\overline{PL}$ is LOW, each flip-flop is immediately SET if its P input is HIGH and RESET if its P input is LOW.

MR Master Reset. If this input is HIGH, all four flip-flops are forced to the 0 state irrespective of any other input.

$\overline{TC}_D$ Terminal Count Down. This output is the CP_D input gated by the all 0's state in the counter. If the Q outputs are all LOW, the $\overline{TC}_D$ follows CP_D.

$\overline{TC}_U$ Terminal Count Up. This output is the CP_U input gated by the maximum count state of the counter. For the 54/74192, the TC_U output follows CP_U input if the Q outputs are H L L H (= 9). For the 54/74193 the $\overline{TC}_U$ output follows the CP_U input if the Q outputs are all HIGH (= 15).

Fanout The driving capability of the outputs, in terms of TTL unit loads.

Input Unit Load The loading represented by a TTL gate input, as defined in the "electrical characteristics."

OPERATIONAL TERMS

SWITCHING TERMS

t_{pd+} (Q) The delay from a LOW-to-HIGH transition on either clock input to a LOW-to-HIGH transition on a Q output.

t_{pd-} (Q) The delay from a LOW-to-HIGH transition on either clock input to a HIGH-to-LOW transition on a Q output.

t_{pd+} ($\overline{TC}$) The delay from a LOW-to-HIGH transition on either clock input to a LOW-to-HIGH transition on the corresponding $\overline{TC}$ output.

t_{pd-} ($\overline{TC}$) The delay from a HIGH-to-LOW transition on either clock input to a HIGH-to-LOW transition on the corresponding $\overline{TC}$ output.

t_{pw} (CP) The minimum time that a clock signal can reside in either logic level for reliable operation.

t_{pw} ($\overline{PL}$) The shortest LOW time on the $\overline{PL}$ input that will cause all four flip-flops to be set to the proper state.

t_s (P) The time before the $\overline{PL}$ input goes HIGH at which the flip-flop samples the P input. Data on the P inputs must not change between t_s (P) max and t_s (P) min.

t_{pw} (MR) The shortest HIGH time on the MR input that will reset all four flip-flops.

t_{rec} (MR) Master Reset recovery time. The time that must lapse between the end of a reset signal and a clock LOW-to-HIGH transition for the counter to accept the clock.

t_{rec} ($\overline{PL}$) The parallel load recovery time. The time that must lapse between the end of a parallel load command and a clock LOW-to-HIGH transition for the counter to accept the clock.

t_{pd-} (MR) The delay from a LOW-to-HIGH transition on the MR input to a HIGH-to-LOW transition on a Q output.

f_{max} The maximum frequency at which the counter can be operated.

SWITCHING WAVEFORMS

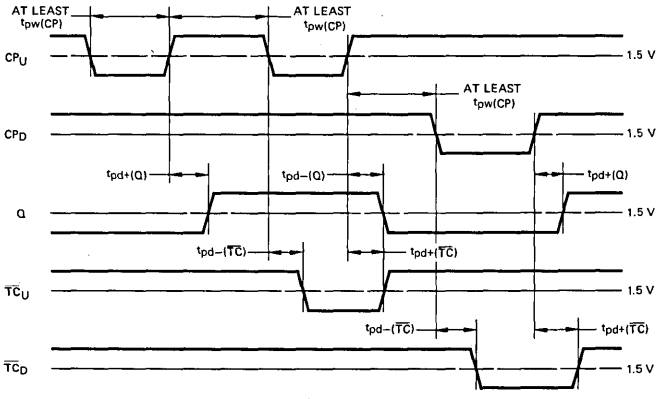


Fig. 1

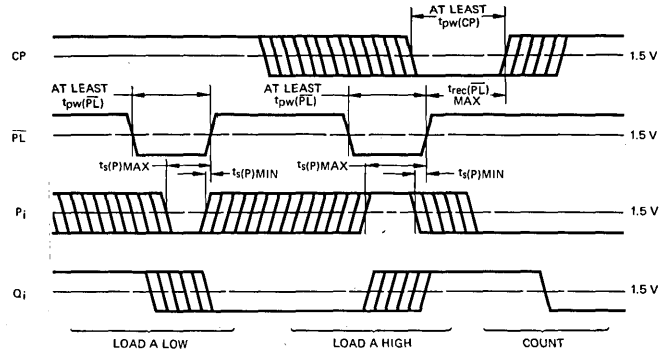


Fig. 2 Input Timing Requirements for Parallel Load

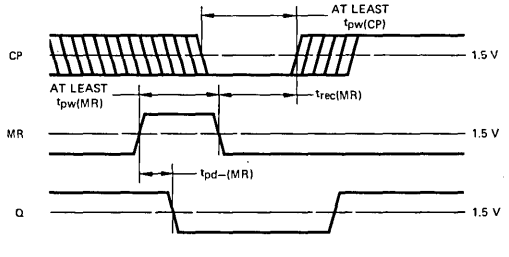


Fig. 3 Master Reset Timing

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN

MSI INTERFACING RULES

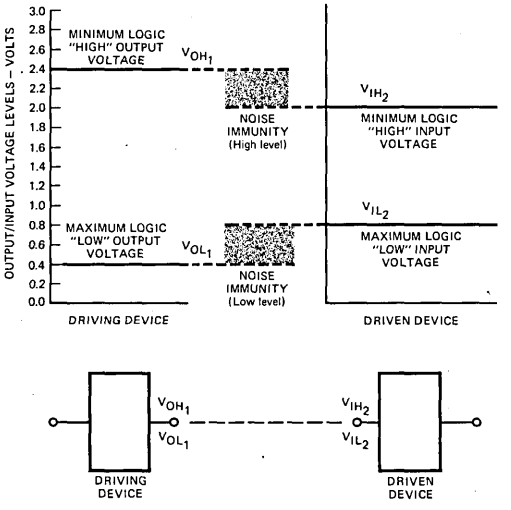
Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
Advanced Micro Devices 54/7400	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

LOADING RULES

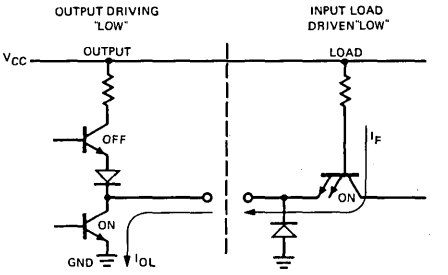
Input/Output	Pin No.'s	Input Unit Load	Fanout Output HIGH	Fanout Output Low
P_1	1	1	—	—
Q_1	2	—	20	10
Q_0	3	—	20	10
CP_D	4	1	—	—
CP_U	5	1	—	—
Q_2	6	—	20	10
Q_3	7	—	20	10
GND	8	—	—	—
P_3	9	1	—	—
P_2	10	1	—	—
$\overline{PL}$	11	1	—	—
$\overline{TC}_U$	12	—	20	10
$\overline{TC}_D$	13	—	20	10
MR	14	1	—	—
P_0	15	1	—	—
V_{CC}	16	—	—	—

INPUT/OUTPUT INTERFACE CONDITIONS

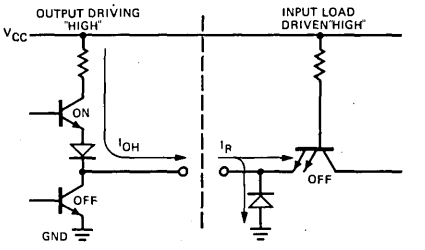
Voltage Interface Conditions — LOW & HIGH



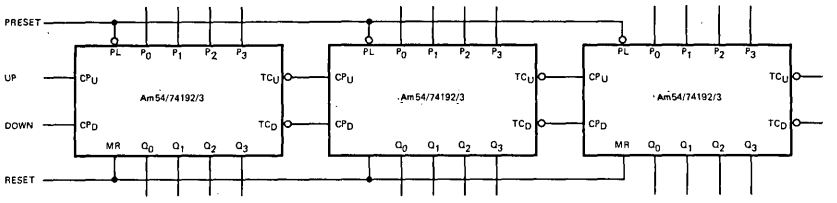
Current Interface Conditions — LOW



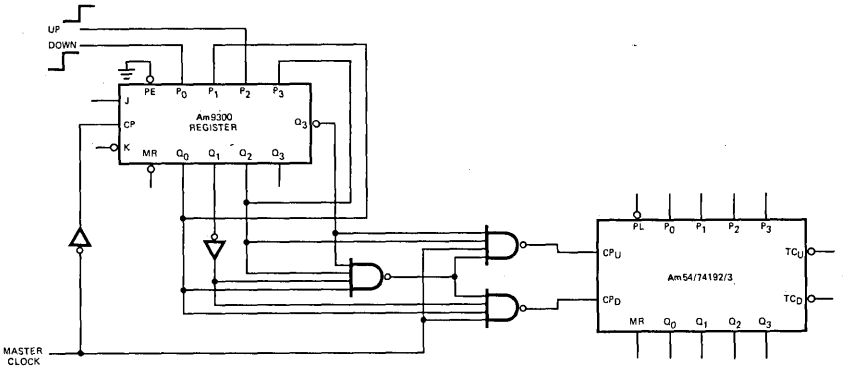
Current Interface Conditions — HIGH



APPLICATIONS



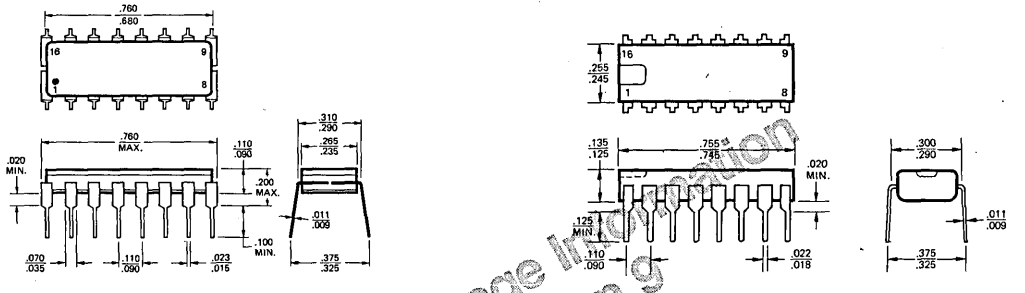
CASCADING UP-DOWN COUNTERS



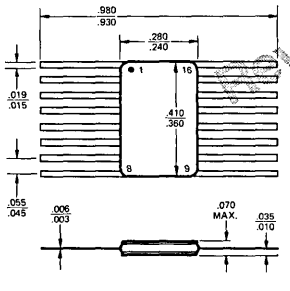
Asynchronous up and down clocks can be synchronized by the circuit shown. The master clock rate must be at least twice the rate of the up and down clocks. The circuit shown detects changes in the up and down inputs and supplies the appropriate clock to the counter. If both signals occur simultaneously, no clocks are produced.

PHYSICAL DIMENSIONS

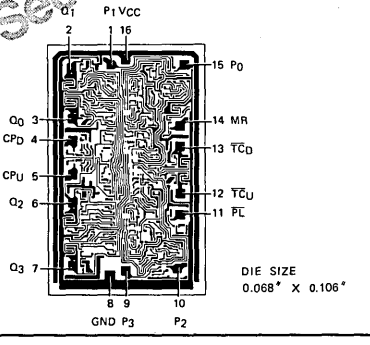
Hermetic — **Dual-In-Line** — **Molded**



Flat Package



Metallization and Pad Layout



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Am93L60•Am93L66

Low-Power Binary and Decimal Up/Down Counters

Distinctive Characteristics

- 85 mw typical power dissipation.
- 23 MHz typical count rate.
- 100% reliability assurance testing in compliance with MIL STD 883.
- Separate count up and count down clocks.

FUNCTIONAL DESCRIPTION

The Am93L60 and Am93L66 are 4-bit up-down counters. The Am93L60 counts in BCD code, and the Am93L66 in binary. The counters have separate count-up and count-down clock inputs (CP_U and CP_D). The outputs (Q_{0-3}) change synchronously following a LOW to HIGH transition on either clock input. Only one clock input can be LOW at a time or erroneous counting will result. Each of the four flip-flops can be preset to HIGH or LOW by means of the four parallel inputs, P_{0-3}. When the parallel load input ($\overline{PL}$) goes LOW, all four flip-flops set to the state of their P inputs irrespective of the clock inputs. An active HIGH master reset (MR) is provided that overrides both the clock and parallel load inputs, forcing all Q outputs LOW. Two terminal count outputs are gated with the clock inputs to provide clock signals to other counters. The $\overline{TC}_D$ output goes LOW when the counter is in state 0000 and the count-down clock goes LOW. The $\overline{TC}_U$ output goes LOW when the count-up clock goes LOW and the counter is in state 1001 (93L60) or state 1111 (93L66). The signals can drive directly the count-up and count-down clocks on the next counter in a series.

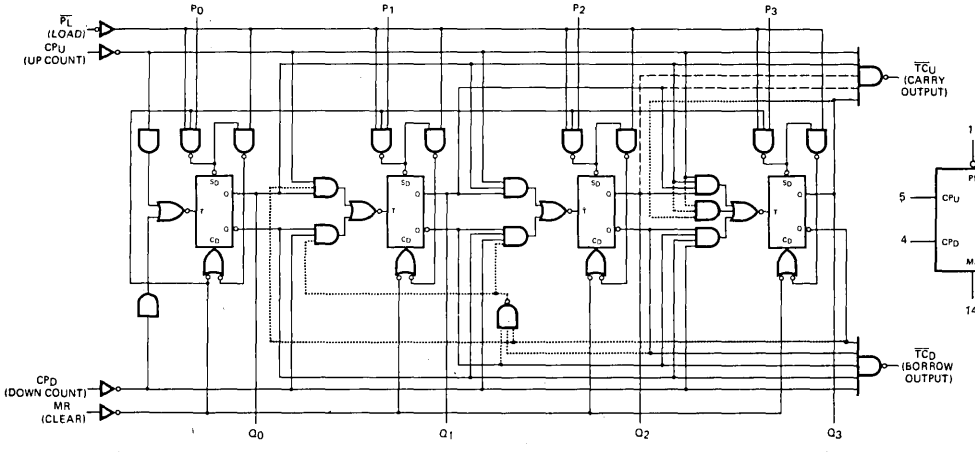
LOADING RULES

In Unit Loads (Notes)

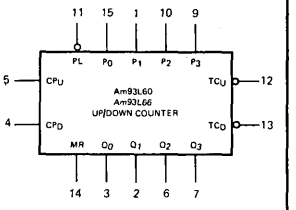
Input Loading	TTL loads HIGH	TTL loads LOW	93L loads HIGH	93L loads LOW
All Inputs	0.5	0.25	1.0	1.0
Output Drive	HIGH	LOW	HIGH	LOW
All Outputs	10	3	20	12

NOTES:
1) A TTL unit load is specified as 0.4 V at −1.6 mA LOW, 2.4 V at 40 μA HIGH.
2) A 93L unit load is specified as 0.3 V at −400 μA LOW, 2.4 V at 20 μA HIGH.
3) Enough output LOW current is available to mix TTL and 93L loads and still meet the 93L requirement of a V_{OL} of 0.3 V.

LOGIC DIAGRAM



LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

Am93L60 Decade Counter .....
Am93L66 Hexadecimal Counter _ _ _ _ _

ORDERING INFORMATION

Package Type	Temperature Range	Am93L60 Order Number	93L66 Order Number
16-Pin Molded DIP	0°C to +75°C	U6M93L6059X	U6M93L6659X
16-Pin Hermetic DIP	0°C to +75°C	U7B93L6059X	U7B93L6659X
16-Pin Hermetic DIP	−55°C to +125°C	U7B93L6051X	U7B93L6651X
16-Pin Hermetic Flat Pak	−55°C to +125°C	U4L93L6051X	U4L93L6651X
Dice	Note	UXX93L60XXD	UXX93L66XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current (Note 1)	−30 mA to +5.0 mA

Note 1. Maximum current defined by DC input voltage.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93L6059X, Am93L6659X T_A = 0°C to +75°C V_{CC} = 4.75 V to 5.25 V
Am93L6051X, Am93L6651X T_A = −55°C to +125°C V_{CC} = 4.50 V to 5.50 V

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 4.92 mA V_{IN} = V_{IH} or V_{IL}		0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.7	Volts
I_{IL} (Note 2)	93L Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.3 V		−0.25	−0.4	mA
I_{IH} (Note 2)	93L Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V		2.0	20	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V	−4	−12	−25	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		17	28	mA

Notes: 1) Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by the 93L input load factor. (See loading rules)

SWITCHING CHARACTERISTICS (T_A = 25°C) (V_{CC} = 5.0 V, C_L = 15 pF)

Parameters	Definition	Test Conditions	Min	Typ	Max	Units
t_{pd+} (Q)	Delay from clock to Q output HIGH	C_L = 15 pF See Fig. 1		40	60	ns
t_{pd-} (Q)	Delay from clock to Q output LOW			31	75	ns
t_{pd+} ($\overline{TC}$)	Delay from up or down clock to corresponding TC output HIGH	C_L = 15 pF See Fig. 1		25	38	ns
t_{pd-} ($\overline{TC}$)	Delay from up or down clock to corresponding TC output LOW			30	45	ns
t_{pw} (CP)	Minimum clock LOW or HIGH time (Note 1)			27	40	ns
t_{pw} ($\overline{PL}$)	Minimum LOW time on $\overline{PL}$ input	See Fig. 2		32	55	ns
t_s (P)	Set up time, P inputs		8	23	35	ns
t_{pw} (MR)	Minimum HIGH time on master reset input	See Fig. 3		30	45	ns
t_{rec} (MR)	Master reset recovery time			22	35	ns
f_{max}	Maximum count frequency		12	23		MHz
t_{pd-} (MR)	Delay, master reset to outputs LOW	See Fig. 3		55	83	ns
t_{rec} ($\overline{PL}$)	Recovery time, parallel load input	See Fig. 2		30	45	ns

Notes 1) Either input must be LOW for t_{pw} (CP) and both inputs must be HIGH for t_{pw} (CP) between clocks.

SWITCHING TIME WAVEFORMS

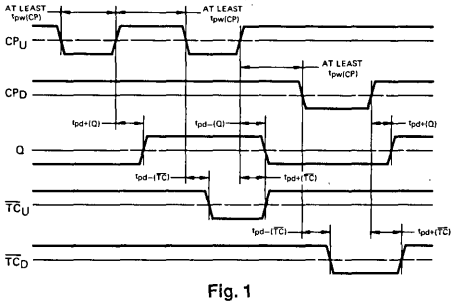


Fig. 1

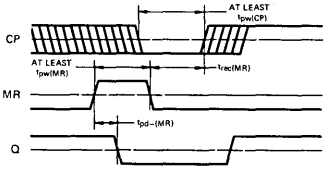
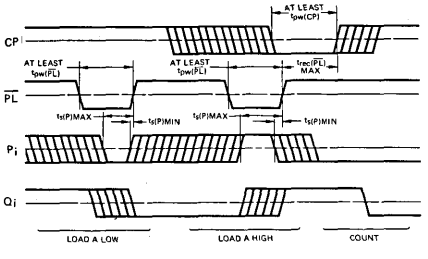
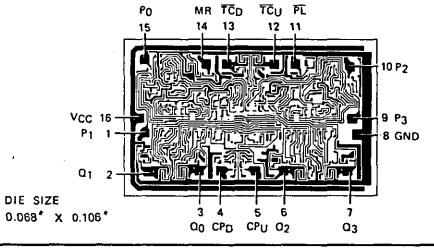


Fig. 3 Master Reset Timing

Fig. 2 Input Timing Requirements for Parallel Load



Metallization and Pad Layout



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Am54/74153

Dual 4-Line To 1-Line Data Selector / Multiplexer

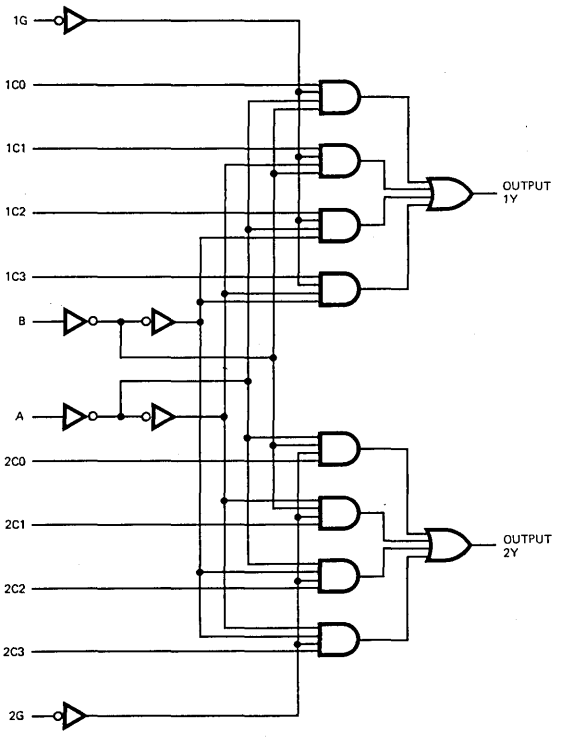
Distinctive Characteristics

- Permits multiplexing from N lines to 1 line.
- Performs parallel-to-serial conversion.
- Separate strobe input for each data selector section.
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

This dual four-input multiplexer provides the digital equivalent of a two-pole, four position switch with the position of both switches set by the logic levels supplied to the select inputs A and B. Each section of the Am54/74153 has a separate active-LOW enable (strobe) input that forces the output of that section LOW when a HIGH level is applied regardless of the other inputs.

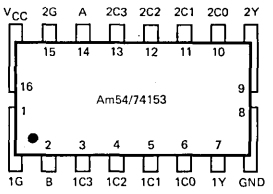
LOGIC DIAGRAM



ORDERING INFORMATION

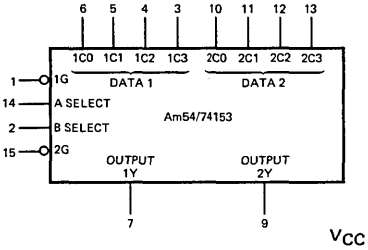
Package Type	Temperature Range	Am54/74153 Order Number
Molded DIP	0°C to +70°C	SN74153N
Hermetic DIP	0°C to +70°C	SN74153J
Dice	0°C to +70°C	SN74153X
Hermetic DIP	−55°C to +125°C	SN54153J
Hermetic Flat Pak	−55°C to +125°C	SN54153W
Dice	−55°C to +125°C	SN54153X

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to + V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am74153	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5% (COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am54153	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10% (MIL)	MIN. = 4.5V	MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −800μA V_{IN} = V_{IH} or V_{IL}		2.4	3.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −12mA				−1.5	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V				−1.6	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V				40	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0V	Am54	−20		−55	mA
			Am74	−18		−57	
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)	Am54		36	52	mA
			Am74		36	60	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Data to Output	V_{CC} = 5.0V, R_L = 400Ω, C_L = 30 pF		12	18	ns
t_{PHL}				15	23	
t_{PLH}	Select to Output			22	34	ns
t_{PHL}				22	34	
t_{PLH}	Strobe to Output			19	30	ns
t_{PHL}				15	23	

FUNCTION TABLE

INPUTS							OUTPUTS
Select		Data				Strobe	Output
B	A	C_0	C_1	C_2	C_3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH
L = LOW
X = Don't Care

Note: A & B are common to both 4 input multiplexers.

DEFINITION OF FUNCTIONAL TERMS

$1C_i$, $2C_i$ Data Inputs. The four data inputs to each multiplexer i = 0, 1, 2, and 3.

1Y, 2Y Multiplexer Outputs. The output of each four-input multiplexer.

A, B Select Inputs. The inputs used to determine which of the four inputs are selected for the output.

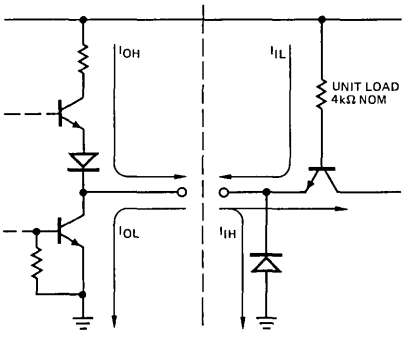
G Enable (Strobe). An active-LOW strobe used to enable the output. A HIGH level input forces the output LOW regardless of the other inputs.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Unit Load	Fan-out Output HIGH	Fan-out Output LOW
1G	1	1	–	–
B	2	1	–	–
1C3	3	1	–	–
1C2	4	1	–	–
1C1	5	1	–	–
1C0	6	1	–	–
1Y	7	–	20	10
GND	8	–	–	–
2Y	9	–	20	10
2C0	10	1	–	–
2C1	11	1	–	–
2C2	12	1	–	–
2C3	13	1	–	–
A	14	1	–	–
2G	15	1	–	–
V_{CC}	16	–	–	–

A TTL Unit Load is defined as +40μA measured at 2.4V HIGH and −1.6mA measured at 0.4V LOW.

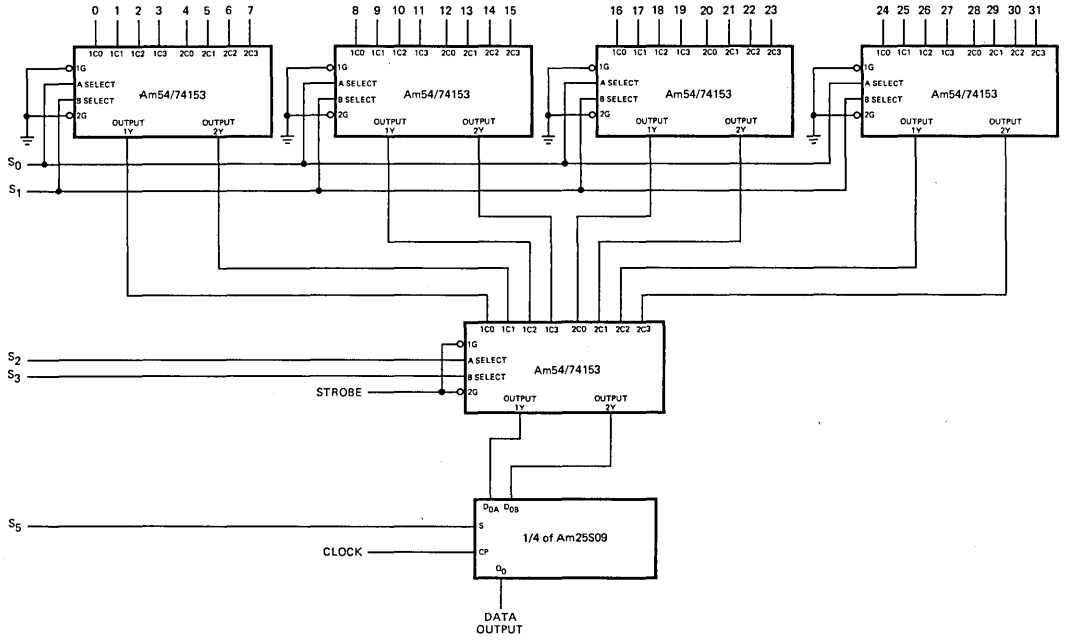
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



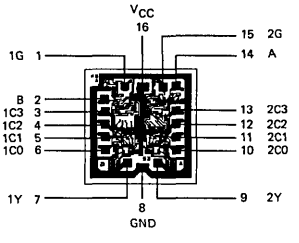
Note: Actual current flow direction shown.

APPLICATION

32-LINE TO 1-LINE DATA SELECTOR WITH REGISTER STORAGE



Metallization and Pad Layout



DIE SIZE 0.054" X 0.056"

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

f_{MAX} The highest operating clock frequency.

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{PW} Pulse width. The time between the leading and trailing edges of a pulse.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

t_s Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

t_h Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.

t_R Release time. The time interval for which a signal may be indeterminant at one input terminal before an active transition occurs at another input terminal. (The release time falls within the set-up time interval and is specified by some manufacturers as a negative hold time).

UNIT LOAD DEFINITIONS

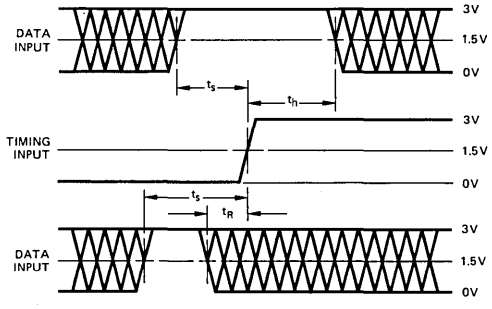
	HIGH		LOW	
SERIES	Current	Measure Voltage	Current	Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0 mA	0.5 V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

Note: 1. 54L/74L has two different types of standard inputs.

PARAMETER MEASUREMENTS

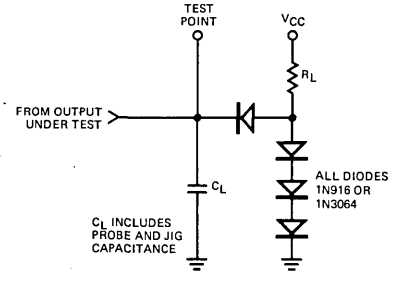
FOR STANDARD ACTIVE-PULLUP TOTEM-POLE OUTPUTS

SET-UP, HOLD, AND RELEASE TIMES

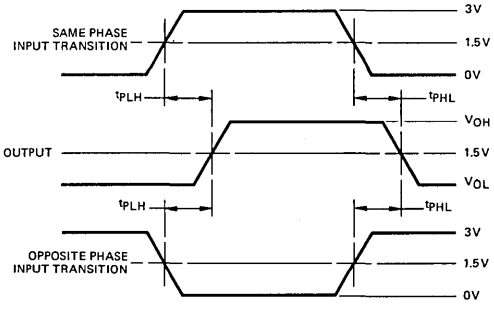


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched area is don't care condition.

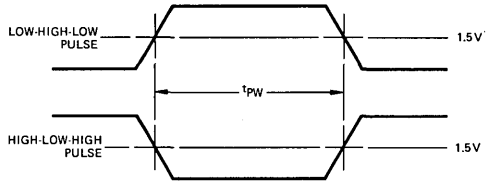
LOAD TEST CIRCUIT



PROPAGATION DELAY

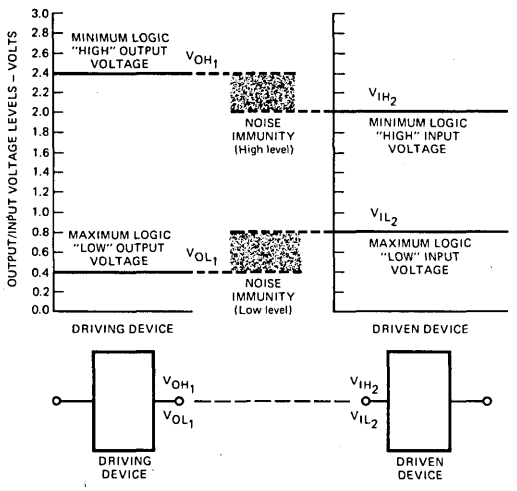


PULSE WIDTH



Notes: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_o = 50\Omega$; $t_r \leq 10$ns; $t_f \leq 10$ns.

INPUT/OUTPUT VOLTAGE INTERFACE CONDITIONS



Note: Refer to Electrical Characteristics for measure current.

DEFINITION OF STANDARD TERMS

H HIGH, applying to a HIGH voltage level.

L LOW, applying to a LOW voltage level.

I Input.

O Output.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

I_{IL} LOW-level input current with a specified LOW-level voltage applied.

I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.

I_{OL} LOW-level output current.

I_{OH} HIGH-level output current.

I_{SC} Output short-circuit source current.

I_{CC} The supply current drawn by the device from the V_{CC} power supply.

V_{IL} Logic LOW input voltage.

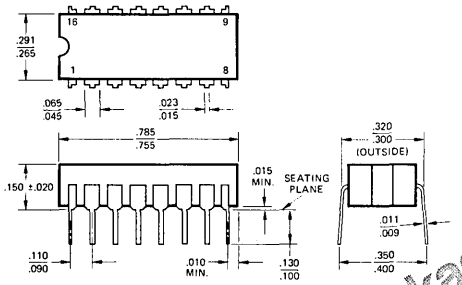
V_{IH} Logic HIGH input voltage.

V_{OL} LOW-level output voltage with I_{OL} applied.

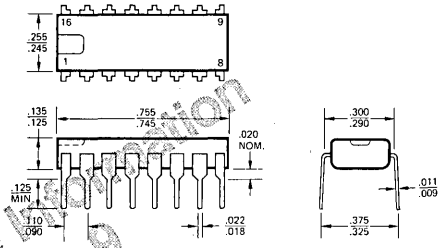
V_{OH} HIGH-level output voltage with I_{OH} applied.

PHYSICAL DIMENSIONS
Dual-In-Line

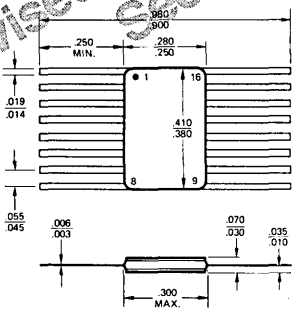
Ceramic



Molded



Flat Package



ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am54/74160 • Am54/74161
Am54/74162 • Am54/74163
Synchronous Four-Bit Counters

Distinctive Characteristics

- 4-bit synchronous counters
- Synchronously programable
- Internal look-ahead counting
- Carry output for n-bit cascading
- Synchronous or asynchronous clear
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

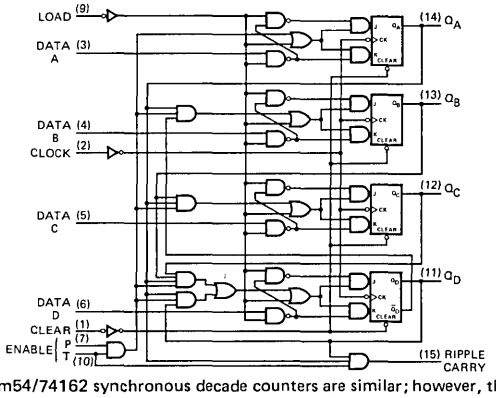
The Am54/74160, Am54/74161, Am54/74162 and Am54/74163 synchronous, presettable counters have internal look-ahead carry and ripple carry output for high-speed counting applications. The Am54/74160 and Am54/74162 are decade counters and the Am54/74161 and Am54/74163 are 4-bit binary counters. Counting or loading occurs on the positive transition of the clock pulse. A LOW level on the load input causes the data on the A, B, C and D inputs to be shifted to the appropriate Q outputs on the next positive clock transition. LOW-to-HIGH transitions of the load input should not occur when the clock is LOW if the enable inputs are HIGH at or before the transition.

The Am54/74160 and Am54/74161 feature an asynchronous clear. A LOW level at the clear input sets the Q outputs LOW regardless of the other inputs. The Am54/74162 and Am54/74163 have a synchronous clear. A LOW level at the clear input sets the Q outputs LOW after the next positive clock transition regardless of the enable inputs.

Both count-enable inputs P and T must be HIGH to count. Count enable T is included in the ripple carry output gate for cascading connection. HIGH-to-LOW level transitions on the enable P or T inputs should occur only when the clock is HIGH.

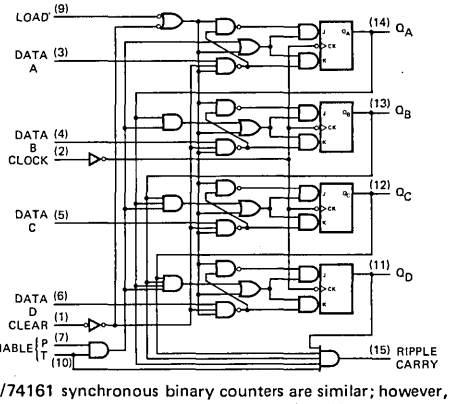
LOGIC DIAGRAMS

Am54/74160 Synchronous Decade Counter



Am54/74162 synchronous decade counters are similar; however, the clear is synchronous as shown for the Am54/74163 binary counters.

Am54/74163 Synchronous Binary Counter

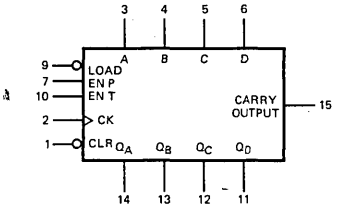


Am54/74161 synchronous binary counters are similar; however, the clear is asynchronous as shown for the Am54/74160 decade counters.

ORDERING INFORMATION

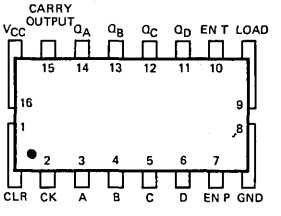
Part Number	Package Type	Temperature Range	Order Number
Am54/74160	Molded DIP	0°C to +70°C	SN74160N
	Hermetic DIP	0°C to +70°C	SN74160J
	Dice	0°C to +70°C	SN74160X
	Hermetic DIP	−55°C to +125°C	SN54160J
	Hermetic Flat Pak	−55°C to +125°C	SN54160W
	Dice	−55°C to +125°C	SN54160X
Am54/74161	Molded DIP	0°C to +70°C	SN74161N
	Hermetic DIP	0°C to +70°C	SN74161J
	Dice	0°C to +70°C	SN74161X
	Hermetic DIP	−55°C to +125°C	SN54161J
	Hermetic Flat Pak	−55°C to +125°C	SN54161W
	Dice	−55°C to +125°C	SN54161X
Am54/74162	Molded DIP	0°C to +70°C	SN74162N
	Hermetic DIP	0°C to +70°C	SN74162J
	Dice	0°C to +70°C	SN74162X
	Hermetic DIP	−55°C to +125°C	SN54162J
	Hermetic Flat Pak	−55°C to +125°C	SN54162W
	Dice	−55°C to +125°C	SN54162X
Am54/74163	Molded DIP	0°C to +70°C	SN74163N
	Hermetic DIP	0°C to +70°C	SN74163J
	Dice	0°C to +70°C	SN74163X
	Hermetic DIP	−55°C to +125°C	SN54163J
	Hermetic Flat Pak	−55°C to +125°C	SN54163W
	Dice	−55°C to +125°C	SN54163X

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am74160, Am74161, Am74162, Am74163 T_A = 0°C to +70°C V_{CC} = 5.0 V ±5% (COM'L) MIN. = 4.75 V MAX. = 5.25 V

Am54160, Am54161, Am54162, Am54163 T_A = −55°C to +125°C V_{CC} = 5.0 V ±10% (MIL) MIN. = 4.5 V MAX. = 5.5 V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −800μA V_{IN} = V_{IH} or V_{IL}		2.4	3.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −12mA				−1.5	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V	CK or EN T			−3.2	mA
			Others			−1.6	
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V	CK or EN T			80	μA
			Others			40	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0 V	54 Series	−20		−57	mA
			74 Series	−18		−57	
I_{CCH}	Power Supply Current All Outputs HIGH	V_{CC} = MAX. (Note 5)	54 Series		59	85	mA
			74 Series		59	94	
I_{CCL}	Power Supply Current All Outputs LOW	V_{CC} = MAX. (Note 6)	54 Series		63	91	mA
			74 Series		63	101	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CCH} is measured with the load input HIGH, then again with the load input LOW, with all other inputs HIGH and all outputs open.
6. I_{CCL} is measured with the clock input HIGH, then again with the clock input LOW, with all other inputs LOW and all outputs open.

Switching Characteristics (T_A = +25°C)

Parameters	Description		Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Clock to Carry Output		V_{CC} = 5.0 V, C_L = 15pF, R_L = 400Ω		23	35	ns
t_{PHL}					23	35	
t_{PLH}	Clock to Q Output with Load Input HIGH				13	20	ns
t_{PHL}					15	23	
t_{PLH}	Enable T to Carry Output				10	14	ns
t_{PHL}					10	14	
t_{PLH}	Clock to Q Output with Load Input LOW				17	25	ns
t_{PHL}					19	29	
t_{PHL}	Clear to Q Output (Note 1)				20	30	ns
t_{pw}	Pulse Width	Clock		25			ns
		Clear		20			
t_s	Set-up Time	Data − A, B, C, D		15			ns
		Enable P		20			
		Load		25			
		Clear (Note 2)		20			
t_h	Hold Time − Any Input			0			ns
$f_{MAX.}$	Maximum Clock Frequency			25	32		MHz

Notes: 1. Measured from clear input on Am54/74160 and Am54/74161. Measured from clock input on Am54/74162 and Am54/74163.
2. Applies to Am54/74162 and Am54/74163 only.

DEFINITION OF FUNCTIONAL TERMS

CK Clock pulse. Enters data or counts on the positive-going edge.

CLR Clear. On the Am54/74160 and Am54/74161, the clear is asynchronous. A LOW on the clear sets all four flip-flops LOW. On the Am54/74162 and Am54/74163 the clear is synchronous. A LOW on the clear sets all four flip-flops LOW after the next positive-going clock edge.

LOAD Load. When the load is LOW, data on the A, B, C and D inputs is transferred to the output on the positive-going clock edge. When the load is HIGH, the counter is enabled.

EN P Enable P. Parallel count enable. Must be HIGH to count.

EN T Enable T. Serial trickle count enable. Must be HIGH to count.

A, B, C, D The four counter parallel inputs.

Q_A, Q_B, Q_C, Q_D The four counter outputs.

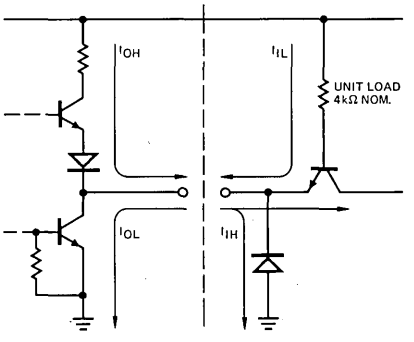
Carry Output Carry look-ahead circuitry for cascading. Will be HIGH when the four-bit counter is maximum (1001 for BCD and 1111 for binary).

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
Clear	1	1	–	–
Clock	2	2	–	–
A	3	1	–	–
B	4	1	–	–
C	5	1	–	–
D	6	1	–	–
Enable P	7	1	–	–
GND	8	–	–	–
Load	9	1	–	–
Enable T	10	2	–	–
Q_D	11	–	20	10
Q_C	12	–	20	10
Q_B	13	–	20	10
Q_A	14	–	20	10
Carry Out	15	–	20	10
V_{CC}	16	–	–	–

A TTL unit load is defined as 40μA measured at 2.4V HIGH and −1.6mA measured at 0.4V LOW.

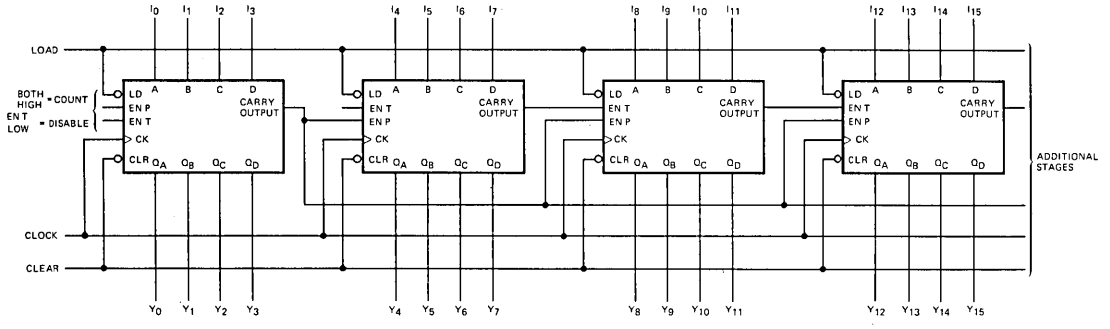
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

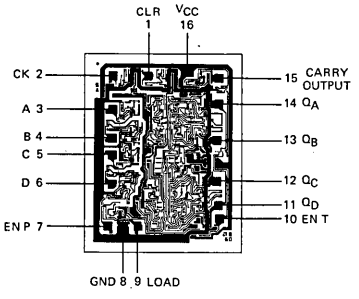
APPLICATIONS

Am54/74160 thru Am54/74163



High-speed, look-ahead carry counter for BCD (Am54/74160 or Am54/74162) or binary (Am54/74161 or Am54/74163). Can count modulo N, N_1-to-N_2, or N_1-to-N maximum.

Pad Layout



DIE SIZE 0.074" X 0.095"

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

f_{MAX} The highest operating clock frequency.

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{PW} Pulse width. The time between the leading and trailing edges of a pulse.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

t_s Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

t_h Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.

t_R Release time. The time interval for which a signal may be indeterminant at one input terminal before an active transition occurs at another input terminal. (The release time falls within the set-up time interval and is specified by some manufacturers as a negative hold time).

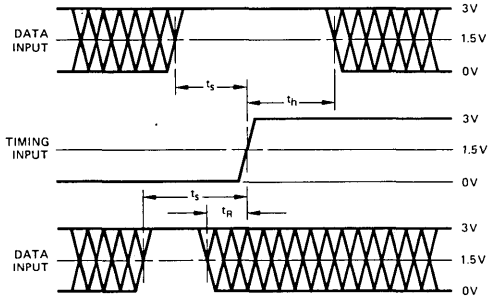
UNIT LOAD DEFINITIONS

	HIGH		LOW	
SERIES	Current	Measure Voltage	Current	Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0 mA	0.5 V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

Note: 1. 54L/74L has two different types of standard inputs.

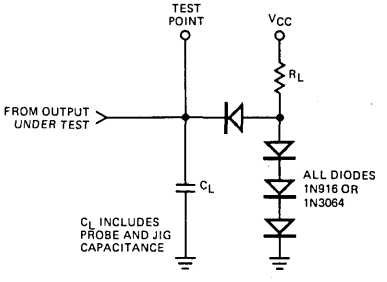
PARAMETER MEASUREMENTS
FOR STANDARD ACTIVE-PULLUP TOTEM-POLE OUTPUTS

SET-UP, HOLD, AND RELEASE TIMES

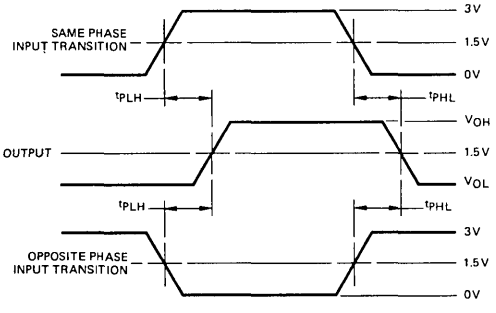


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched area is don't care condition.

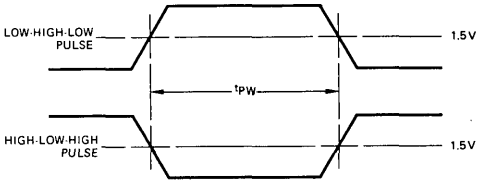
LOAD TEST CIRCUIT



PROPAGATION DELAY

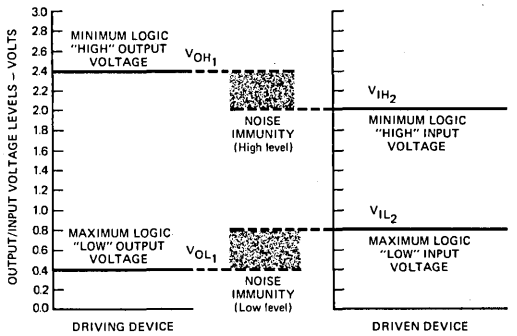


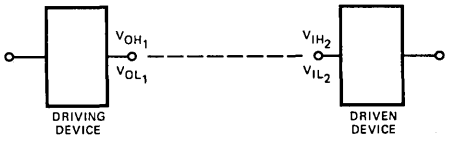
PULSE WIDTH



Note: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_0 = 50\Omega$; $t_r \leq 10$ns; $t_f \leq 10$ns.

INPUT/OUTPUT VOLTAGE INTERFACE CONDITIONS





Note: Refer to Electrical Characteristics for measure currents.

DEFINITION OF STANDARD TERMS

H HIGH, applying to a HIGH voltage level.

L LOW, applying to a LOW voltage level.

I Input.

O Output.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

I_{IL} LOW-level input current with a specified LOW-level voltage applied.

I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.

I_{OL} LOW-level output current.

I_{OH} HIGH-level output current.

I_{SC} Output short-circuit source current.

I_{CC} The supply current drawn by the device from the V_{CC} power supply.

V_{IL} Logic LOW input voltage.

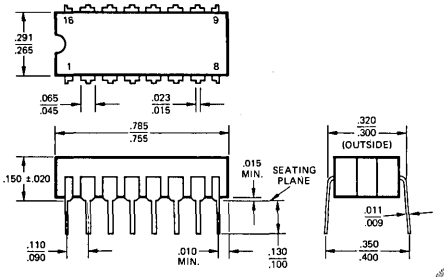
V_{IH} Logic HIGH input voltage.

V_{OL} Low-level output voltage with I_{OL} applied.

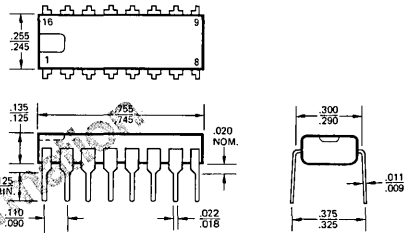
V_{OH} HIGH-level output voltage with I_{OH} applied.

PHYSICAL DIMENSIONS
Dual-In-Line

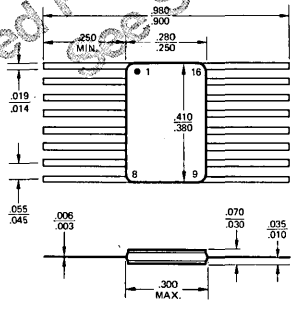
Ceramic



Molded



Flat Package



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Am54/74174 • Am54/74175

Hex/Quadruple D-Type Flip-Flops with Clear

Distinctive Characteristics

- Buffered clock and direct clear inputs.
- Individual data input to each flip-flop.
- 35 MHz typical clock frequency.
- 100% reliability assurance testing in compliance with MIL-STD-883.

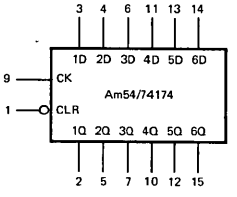
FUNCTIONAL DESCRIPTION

The Am54/74174 is a hex positive-edge-triggered D-type parallel register. The Am54/74175 is a quad positive-edge-triggered D-type parallel register with both Q and $\overline{Q}$ outputs available. Both registers feature a single common clock line and a single common clear line.

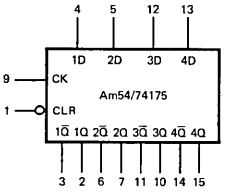
When the clear input is LOW, the Q outputs are LOW regardless of the other inputs. When the clear input is HIGH, the clock will transfer data on the D_i inputs to the Q_i outputs on the LOW-to-HIGH transition of the clock. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going edge. When the clock is at either a HIGH or a LOW, the D_i inputs have no effect on the Q_i outputs.

LOGIC SYMBOLS

Am54/74174



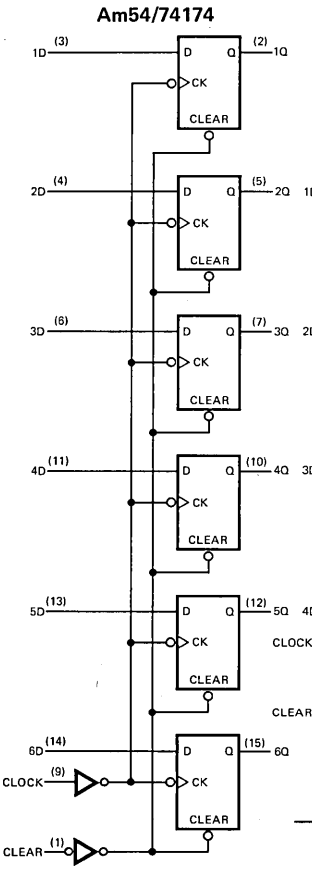
Am54/74175



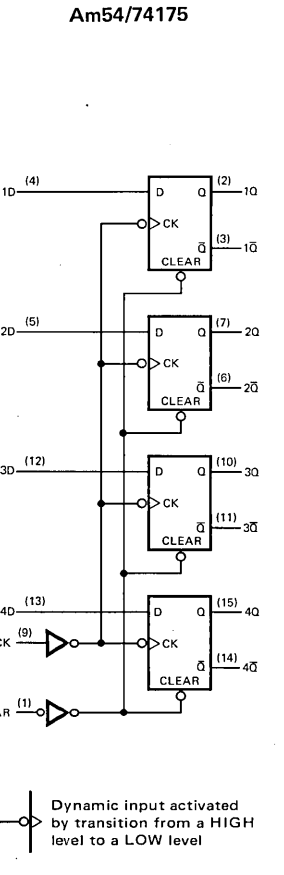
V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL BLOCK DIAGRAMS

Am54/74174



Am54/74175



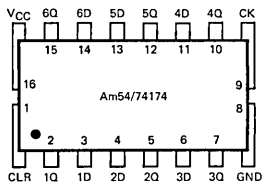
Dynamic input activated by transition from a HIGH level to a LOW level

Am54/74174, Am54/74175 ORDERING INFORMATION

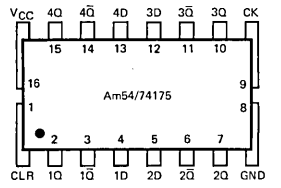
Package Type	Temperature Range	Am54/74174 Order Number	Am54/74175 Order Number
Molded DIP	0°C to 70°C	SN74174N	SN74175N
Hermetic DIP	0°C to 70°C	SN74174J	SN74175J
Dice	0°C to 70°C	SN74174X	SN74175X
Hermetic DIP	−55°C to +125°C	SN54174J	SN54175J
Hermetic Flat Pack	−55°C to +125°C	SN54174W	SN54175W
Dice	−55°C to +125°C	SN54174X	SN54175X

CONNECTION DIAGRAMS
Top View

Am54/74174



Am54/74175



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°
Temperature (Ambient) Under Bias	−55°C to +125°
Supply Voltage to Ground Potential Continuous	−0.5 V to +7
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} ma
DC Input Voltage	−0.5 V to +5.5
Output Current, Into Outputs	30 m
DC Input Current	−30 mA to +5.0 m

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am74174, Am74175 T_A = 0°C to 70°C V_{CC} = 5.0 V ±5% (COM) MIN. = 4.75 V MAX. = 5.25 V
Am54174, Am54175 T_A = −55°C to +125°C V_{CC} = 5.0 V ±10% (MIL) MIN. = 4.5 V MAX. = 5.5 V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.8mA V_{IN} = V_{IH} or V_{IL}		2.4	3.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4				−1.6	mA
I_{IH} (Note 3	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V				40	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.	54174, 5	−20		−57	mA
			74174, 5	−18		−57	
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX.	54/74174		45	65	mA
			54/74175		30	45	

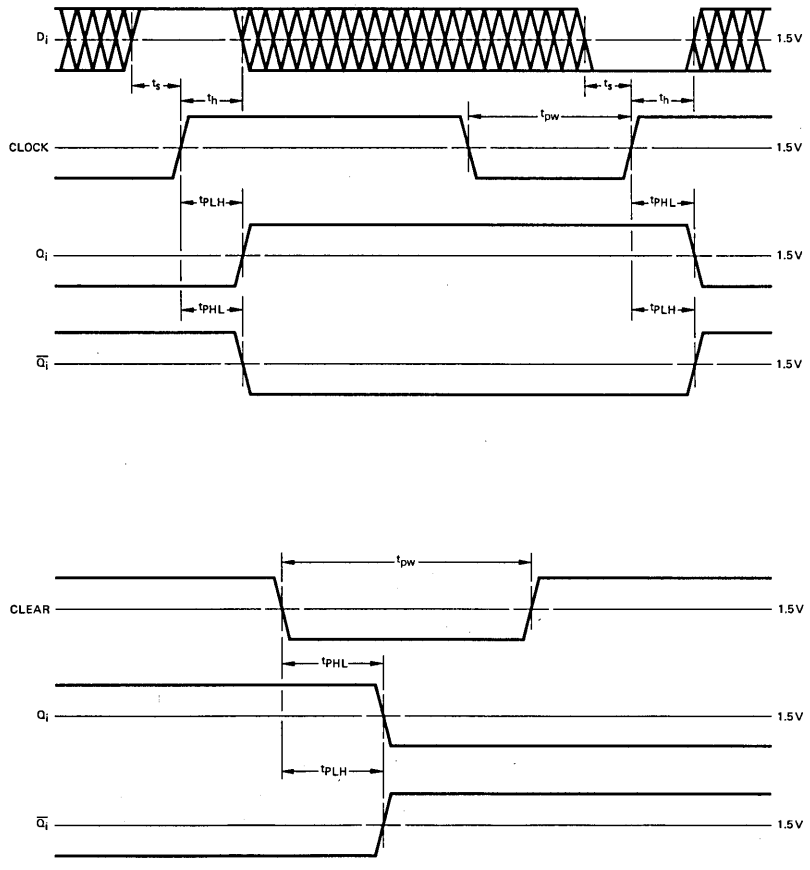
Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input current = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. All outputs open. Data and clear inputs at 4.5 V. Measured after a momentary ground, then 4.5 V applied to the clock.

Switching Characteristics (T_A = 25°C)

Parameters	Description		Test Conditions	Limits Min.	Typ.	Max.	Units
$f_{max.}$	Maximum Clock Frequency		V_{CC} = 5.0 V C_L = 15 pF, R_L = 400 Ω (See Switching Waveforms)	25	35		MHz
t_{PLH}	Propagation Delay Time, LOW-to-HIGH Level Output from Clear (Am54/74175 Only)				16	25	ns
t_{PHL}	Propagation Delay Time, HIGH-to-LOW Level Output from Clear				23	35	ns
t_{PLH}	Propagation Delay Time, LOW-to-HIGH Level Output from Clock				20	30	ns
t_{PHL}	Propagation Delay Time, HIGH-to-LOW Level Output from Clock				21	30	ns
t_{pw}	Pulse Width	Clock		20			ns
		Clear		20			
t_s	Set-up Time	Data		20			ns
		Clear		25			
t_h	Hold Time - Data			5			ns

SWITCHING WAVEFORMS

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



DEFINITION OF TERMS

SUBSCRIPT TERMS

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS

D Information on the D input is written into the flip-flop on the positive going clock transition.

Q, $\overline{Q}$ The flip-flop outputs.

CK Clock. The clock input is common to all flip-flops and transfers data on the D input to the Q output on its LOW-to-HIGH transition.

CLR Clear. The clear input is common to all flip-flops. A LOW input sets the Q outputs to a LOW.

OPERATIONAL TERMS

I_L Forward input load current for unit input load.

I_{OH} Output HIGH current forced out of output in V_{OH} test.

I_{OL} Output LOW current forced into the output in V_{OL} test.

I_H Reverse input load current.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

SWITCHING TERMS: (All switching times are measured at the logic level)

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{pw} The minimum time between the 1.5V points on the leading and trailing edges of a pulse.

t_s Set-up-time. The time interval for which a signal must be applied and maintained at a specified level for a specified input terminal before an active transition occurs at another specified input terminal.

t_h Hold time. The time interval for which a signal is retained at a specified level for a specified input terminal after an active transition occurs at another specified input terminal.

FUNCTION TABLE
(Each Flip-Flop)

INPUTS			OUTPUTS	
Clear	Clock	D	Q	$\bar{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

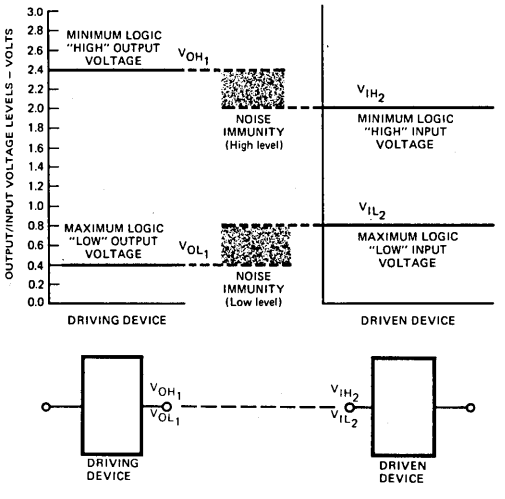
H = HIGH Level (Steady State)
L = LOW Level (Steady State)
X = Irrelevant
↑ = Transition from Low-to-High Level
Q_0 = The Level of Q before the Indicated Steady-State Input Conditions were Established.
† = Am54/74175 Only.

MSI INTERFACING RULES

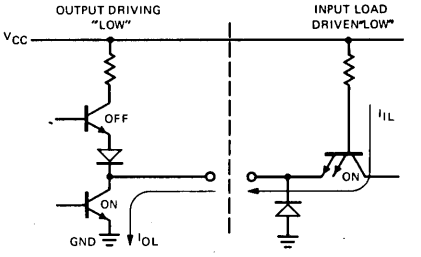
Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
Advanced Micro Devices 54/7400	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

INPUT/OUTPUT INTERFACE CONDITIONS

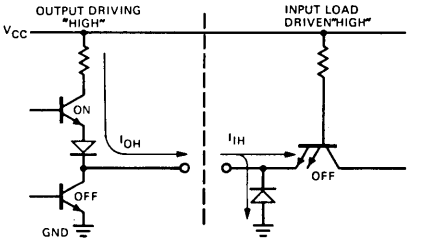
Voltage Interface Conditions — LOW & HIGH



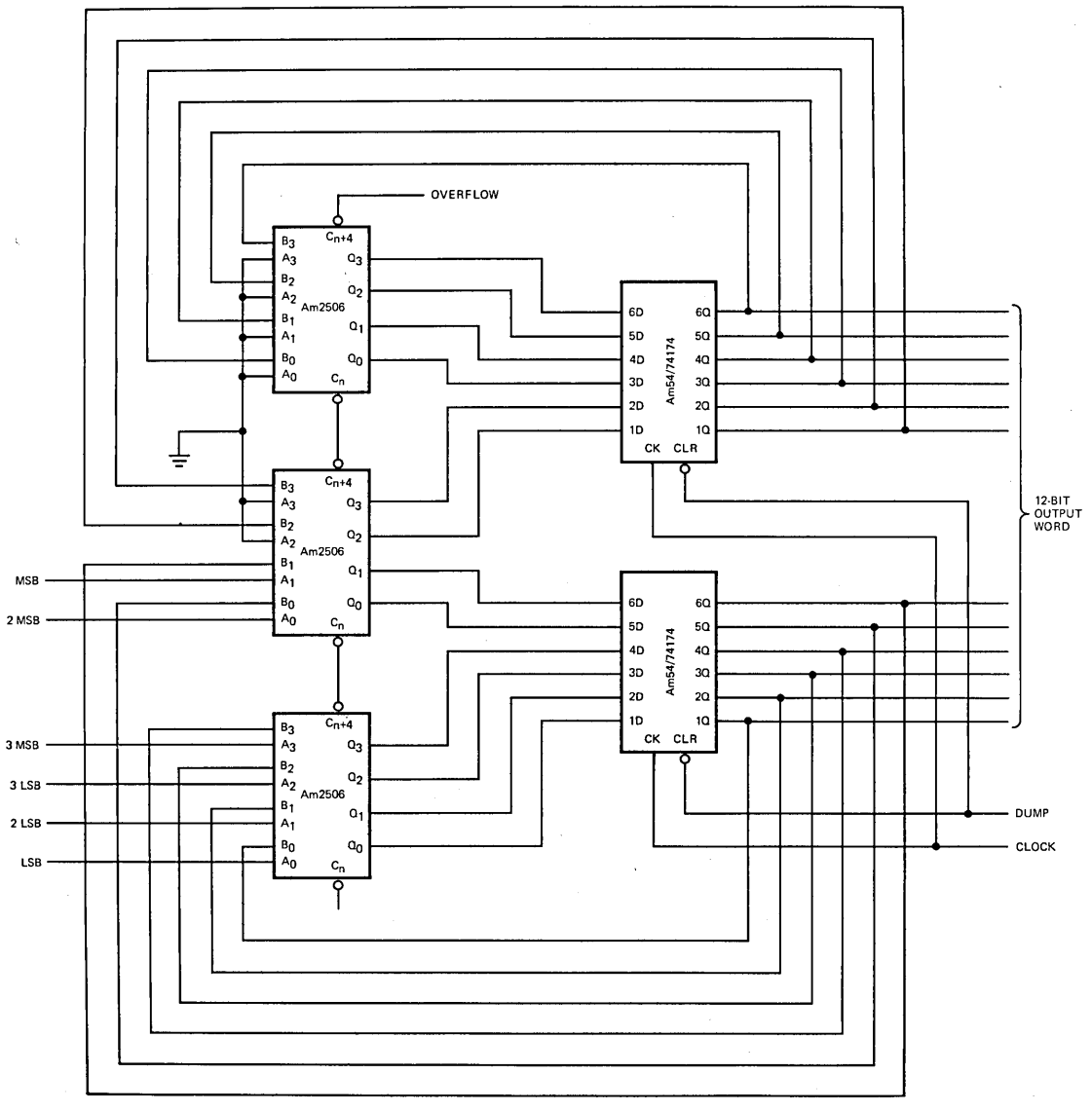
Current Interface Conditions — LOW



Current Interface Conditions — HIGH



APPLICATION



(Am2506 E = S_0 = HIGH; M = S_1 = S_2 = S_3 = LOW)

6-Bit Input, Integrate and Dump for Magnitude-Only Arithmetic (65 samples min. before overflow)

Am54/74174 LOADING RULES (In Unit Loads)

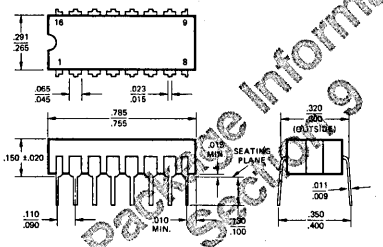
Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
Clear	1	1	–	–
1Q	2	–	20	10
1D	3	1	–	–
2D	4	1	–	–
2Q	5	–	20	10
3D	6	1	–	–
3Q	7	–	20	10
GND	8	–	–	–
CK	9	1	–	–
4Q	10	–	20	10
4D	11	1	–	–
5Q	12	–	20	10
5D	13	1	–	–
6D	14	1	–	–
6Q	15	–	20	10
V_{CC}	16	–	–	–

Am54/74175 LOADING RULES (In Unit Loads)

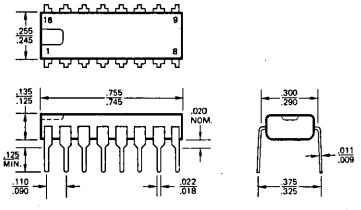
Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
Clear	1	1	–	–
1Q	2	–	20	10
$1\overline{Q}$	3	–	20	10
1D	4	1	–	–
2D	5	1	–	–
$2\overline{Q}$	6	–	20	10
2Q	7	–	20	10
GND	8	–	–	–
CK	9	1	–	–
3Q	10	–	20	10
$3\overline{Q}$	11	–	20	10
3D	12	1	–	–
4D	13	1	–	–
$4\overline{Q}$	14	–	20	10
4Q	15	–	20	10
V_{CC}	16	–	–	–

PHYSICAL DIMENSIONS
Dual-In-Line

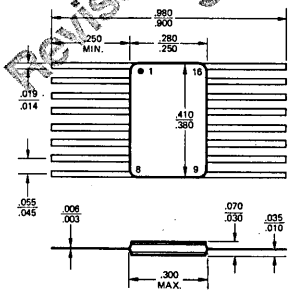
Ceramic



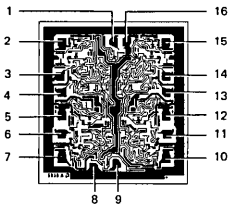
Molded



Flat Package



Metallization and Pad Layout



DIE SIZE .075" x .082"

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Am54/74194•Am54/74195

Four-Bit Shift Registers

Distinctive Characteristics

- Positive edge-triggered clocking
- Direct overriding clear
- Parallel inputs and outputs
- 100% reliability assurance testing in compliance with MIL-STD-883.

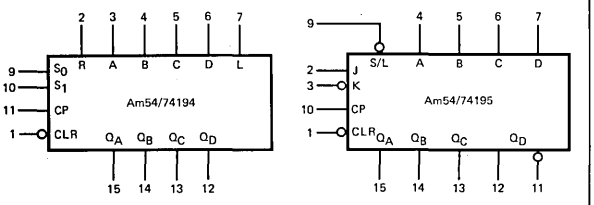
FUNCTIONAL DESCRIPTION

The Am54/74194 features four separate operating modes: Synchronous parallel load, right shift, left shift and inhibit. With S_0 and S_1 HIGH, data is synchronously parallel loaded into the register on the positive transition of the clock. The register will shift right with S_0 HIGH and S_1 LOW and will shift left with S_0 LOW and S_1 HIGH. All shifting occurs on the positive transition of the clock input. With S_0 and S_1 LOW, all register functions are inhibited. The mode control inputs S_0 and S_1 should be changed only when the clock is HIGH.

The Am54/74195 can be operated in either the synchronous parallel load or shift right modes. With the shift/load control LOW, data is synchronously loaded into the register on the positive going transition of the clock input. With the shift/load control HIGH, data on the J-$\overline{K}$ inputs is serially shifted right. This register provides both the Q_D and $\overline{Q}_D$ outputs.

Both registers provide a direct overriding active-LOW clear input.

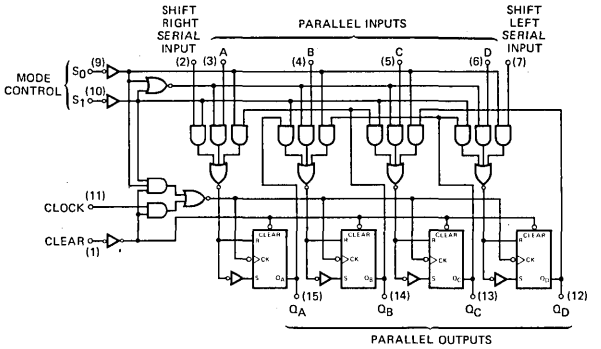
LOGIC SYMBOLS



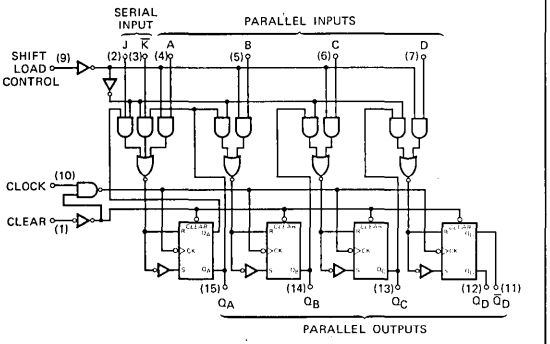
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAMS

Am54/74194



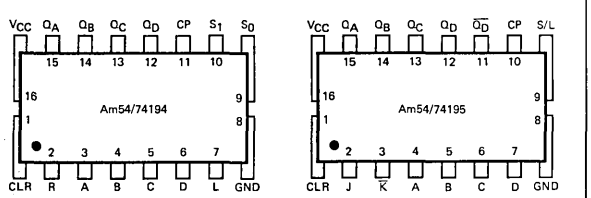
Am54/74195



ORDERING INFORMATION

Package Type	Temperature Range	Am54/74194 Order Number	Am54/74195 Order Number
Molded DIP	0°C to +70°C	SN74194N	SN74195N
Hermetic DIP	0°C to +70°C	SN74194J	SN74195J
Dice	0°C to +70°C	SN74194X	SN74195X
Hermetic DIP	−55°C to +125°C	SN54194J	SN54195J
Hermetic Flat Pak	−55°C to +125°C	SN54194W	SN54195W
Dice	−55°C to +125°C	SN54194X	SN54195X

CONNECTION DIAGRAMS
Top Views



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am74194, Am74195 T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am54194, Am54195 T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL) MIN. = 4.5V MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −800μA V_{IN} = V_{IH} or V_{IL}		2.4	3.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −12mA				−1.5	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V				−1.6	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V				40	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0V	Am54	−20		−57	mA
			Am74	−18		−57	
I_{CC}	Power Supply Current	V_{CC} = MAX.	Am54/74194 (Note 5)		39	63	mA
			Am54/74195 (Note 6)				

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Outputs open. Inputs A, B, C, D grounded. Inputs S_0, S_1, Clear, L, R, at 4.5V. Measured after a momentary ground, then 4.5V applied to clock.
6. Outputs open. S/L grounded. A, B, C, D, J, $\overline{K}$ at 4.5V. Measured after applying a momentary ground then 4.5V to the clear followed by ground then 4.5V to clock.

Switching Characteristics (T_A = +25°C)

Parameters	Description		Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Clock to Output	194	V_{CC} = 5.0V, C_L = 15pF, R_L = 400Ω	7	14	22	ns
		195		6	14	22	
t_{PHL}	Clock to Output			7	17	26	ns
t_{PHL}	Clear to Output				19	30	ns
t_{pw}	Clock Pulse Width	194		20			ns
		195		16			
t_{pw}	Clear Pulse Width	194		20			ns
		195		12			
t_s	Mode Control Set-up Time	194		30			ns
		195		25			
t_s	Data Input Set-up Time	194		20			ns
		195		15			
t_s	Clear Recovery (in-active) to Clock Set-up Time			25			ns
t_h	Data Hold Time			0			ns
t_R	Shift/Load Release-Time Am54/74195					10	ns
$f_{MAX.}$	Maximum Clock Frequency	194		25	36		MHz
		195		30	39		

DEFINITION OF FUNCTIONAL TERMS

J, $\overline{K}$ The logic inputs use for Controlling the Q_A flip-flop of the Am54/74195 register when S/L is HIGH.

CLR Clear. The asynchronous master reset input.

CP Clock pulse for the register. Enters data on the LOW-to-HIGH transition.

S/L Shift/Load. The input for selection of parallel or serial shifting for the Am54/74195 register. S/L LOW selects parallel entry.

S_0, S_1 The mode select inputs of the Am54/74194.

A, B, C, D The four parallel data inputs for the register.

R The serial input to the Q_A flip-flop of the Am54/74194 in the right shift mode.

L The serial input to the Q_D flip-flop of the Am54/74194 in the left shift mode.

Q_A, Q_B, Q_C, Q_D The four true outputs of the register.

$\overline{Q}_D$ The complement output of the Q_D flip-flop. (Am54/74195 only).

LOADING RULES (In Unit Loads)

Am54/74195 Input/Output	Am54/74194 Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
CLR	CLR	1	1	–	–
J	R	2	1	–	–
$\overline{K}$	A	3	1	–	–
A	B	4	1	–	–
B	C	5	1	–	–
C	D	6	1	–	–
D	L	7	1	–	–
GND	GND	8	–	–	–
Shift/Load	S_0	9	1	–	–
CP	S_1	10	1	–	–
$\overline{Q}_D$	–	11	–	20	10
–	CP		1	–	–
Q_D	Q_D	12	–	20	10
Q_C	Q_C	13	–	20	10
Q_B	Q_B	14	–	20	10
Q_A	Q_A	15	–	20	10
V_{CC}	V_{CC}	16	–	–	–

FUNCTION TABLES

Am54/74194

FUNCTION	INPUTS Clear	Mode S_1	Mode S_0	Clock	Serial Left	Serial Right	Parallel A	B	C	D	OUTPUTS Q_A	Q_B	Q_C	Q_D
Clear	L	X	X	X	X	X	X	X	X	X	L	L	L	L
No Change	H	NC	NC	L	X	X	X	X	X	X	NC	NC	NC	NC
	H	X	X	H	X	X	X	X	X	X	NC	NC	NC	NC
Parallel Load	H	H	H	↑	X	X	D_0	D_1	D_2	D_3	D_0	D_1	D_2	D_3
Shift Right	H	L	H	↑	X	L	X	X	X	X	L	Q_A	Q_B	Q_C
	H	L	H	↑	X	H	X	X	X	X	H	Q_A	Q_B	Q_C
Shift Left	H	H	L	↑	L	X	X	X	X	X	Q_B	Q_C	Q_D	L
	H	H	L	↑	H	X	X	X	X	X	Q_B	Q_C	Q_D	H
Hold	H	L	L	X	X	X	X	X	X	X	NC	NC	NC	NC

H = HIGH X = Don't Care
L = LOW NC = No Change
↑ = LOW-to-HIGH transition.
D_i = May be a HIGH or a LOW and the respective output will assume the same state.

Am54/74195

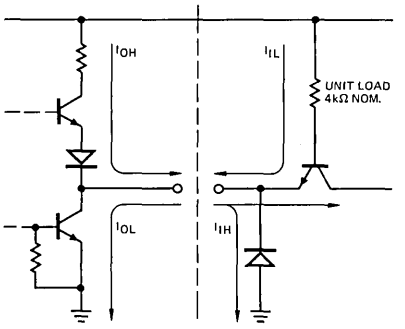
Master Reset	Shift/Load	Clock	INPUTS Serial J	Serial $\overline{K}$	Parallel A	B	C	D	OUTPUTS Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	X	L	X	X	X	X	X	X	NC	NC	NC	NC	NC
H	X	H	X	X	X	X	X	X	NC	NC	NC	NC	NC
H	L	↑	X	X	D_0	D_1	D_2	D_3	D_0	D_1	D_2	D_3	$\overline{D}_3$
H	H	↑	L	H	X	X	X	X	Q_A	Q_A	Q_B	Q_C	$\overline{Q}_C$
H	H	↑	L	L	X	X	X	X	L	Q_A	Q_B	Q_C	$\overline{Q}_C$
H	H	↑	H	H	X	X	X	X	H	Q_A	Q_B	Q_C	$\overline{Q}_C$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_A$	Q_A	Q_B	Q_C	$\overline{Q}_C$

H = HIGH X = Don't Care
L = LOW NC = No Change
↑ = LOW-to-HIGH transition.
D_i = May be a HIGH or a LOW and the respective output will assume the same state.

Note 1: If the J and $\overline{K}$ inputs are tied together, the common line becomes a D-Type input to the first bit in the shift mode.

2: Linear feedback shift counters can be made by connecting the Q_D and $\overline{Q}_D$ outputs to the $\overline{K}$ and J inputs, respectively.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

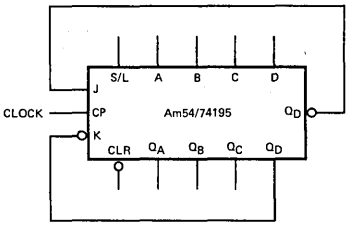


Note: Actual current flow direction shown.

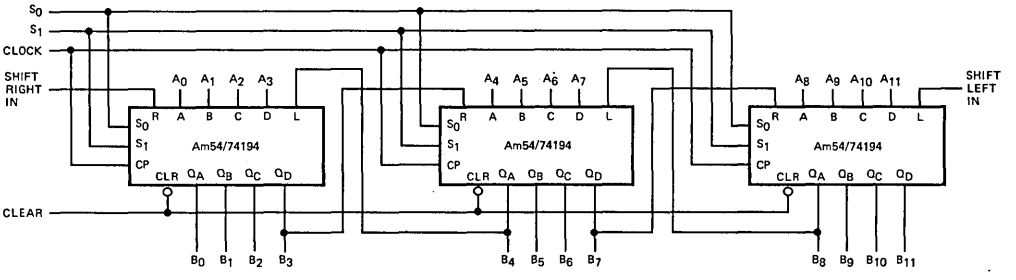
APPLICATIONS

HIGH-SPEED MOD 15 LINEAR FEEDBACK SHIFT REGISTER

Sequence is 0, 1, 2, 5, 10, 4, 9, 3, 6, 13, 11, 7, 14, 12, 8, 0 (15 is non-self correcting; use clear to initialize)

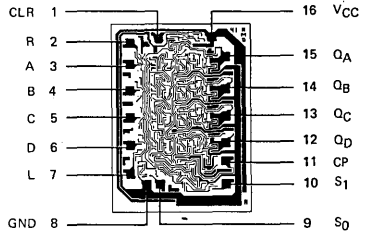


12-BIT SHIFT-LEFT, SHIFT-RIGHT, PARALLEL-LOAD REGISTER



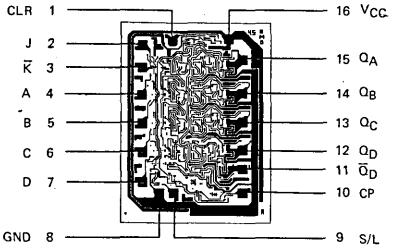
Metallization and Pad Layouts

Am54/74194



DIE SIZE 0.069" X 0.091"

Am54/74195



DIE SIZE 0.069" X 0.091"

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

f_{MAX} The highest operating clock frequency.

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{PW} Pulse width. The time between the leading and trailing edges of a pulse.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

t_s Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

t_h Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.

t_R *Release time. The time interval for which a signal may* be indeterminant at one input terminal before an active transition occurs at another input terminal. (The release time *falls within the set-up time interval* and is specified by some manufacturers as a negative hold time).

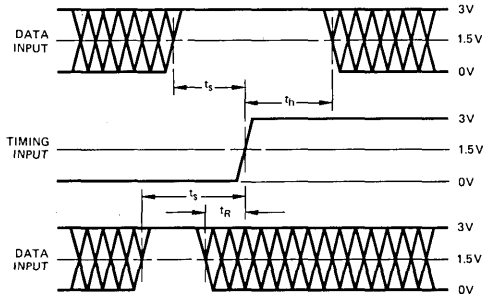
UNIT LOAD DEFINITIONS

	HIGH		LOW	
SERIES	Current	Measure Voltage	Current	Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0mA	0.5V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

Note: 1. 54L/74L has two different types of standard inputs.

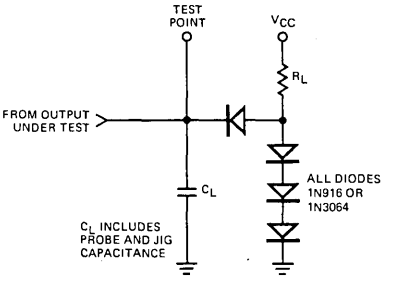
PARAMETER MEASUREMENTS
FOR STANDARD ACTIVE-PULLUP TOTEM-POLE OUTPUTS

SET-UP, HOLD, AND RELEASE TIMES

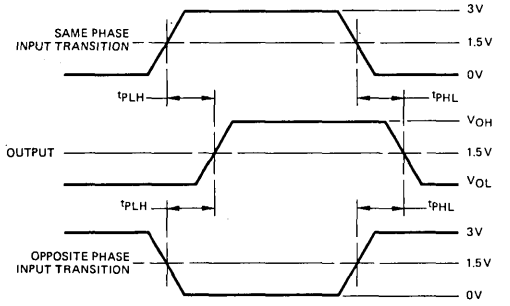


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched area is don't care condition.

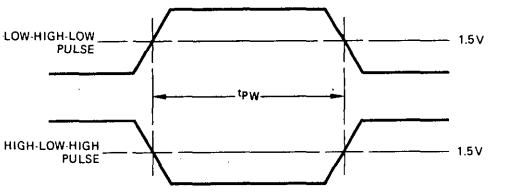
LOAD TEST CIRCUIT



PROPAGATION DELAY

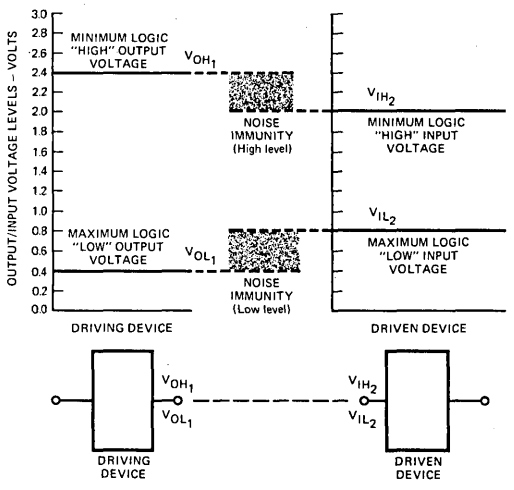


PULSE WIDTH



Notes: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_o = 50\Omega$; $t_r \leq 10$ns; $t_f \leq 10$ns.

INPUT/OUTPUT VOLTAGE INTERFACE CONDITIONS



Note: Refer to Electrical Characteristics for measure current.

DEFINITION OF STANDARD TERMS

H HIGH, applying to a HIGH voltage level.

L LOW, applying to a LOW voltage level.

I Input.

O Output.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

I_{IL} LOW-level input current with a specified LOW-level voltage applied.

I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.

I_{OL} LOW-level output current.

I_{OH} HIGH-level output current.

I_{SC} Output short-circuit source current.

I_{CC} The supply current drawn by the device from the V_{CC} power supply.

V_{IL} Logic LOW input voltage.

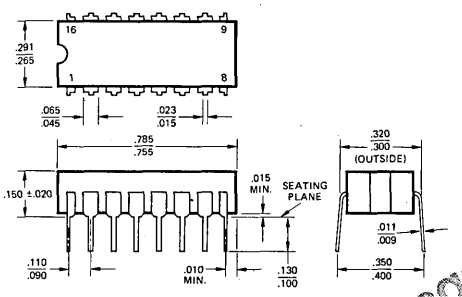
V_{IH} Logic HIGH input voltage.

V_{OL} LOW-level output voltage with I_{OL} applied.

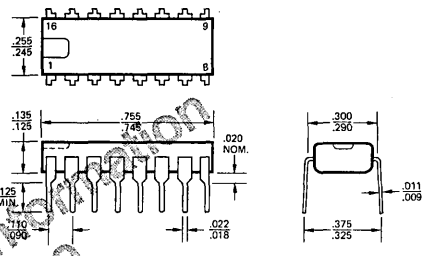
V_{OH} HIGH-level output voltage with I_{OH} applied.

PHYSICAL DIMENSIONS
Dual-In-Line

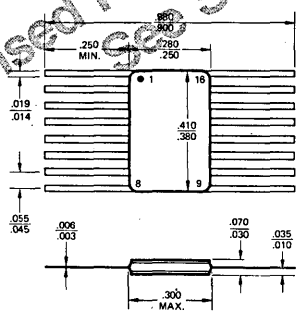
Ceramic



Molded



Flat Package



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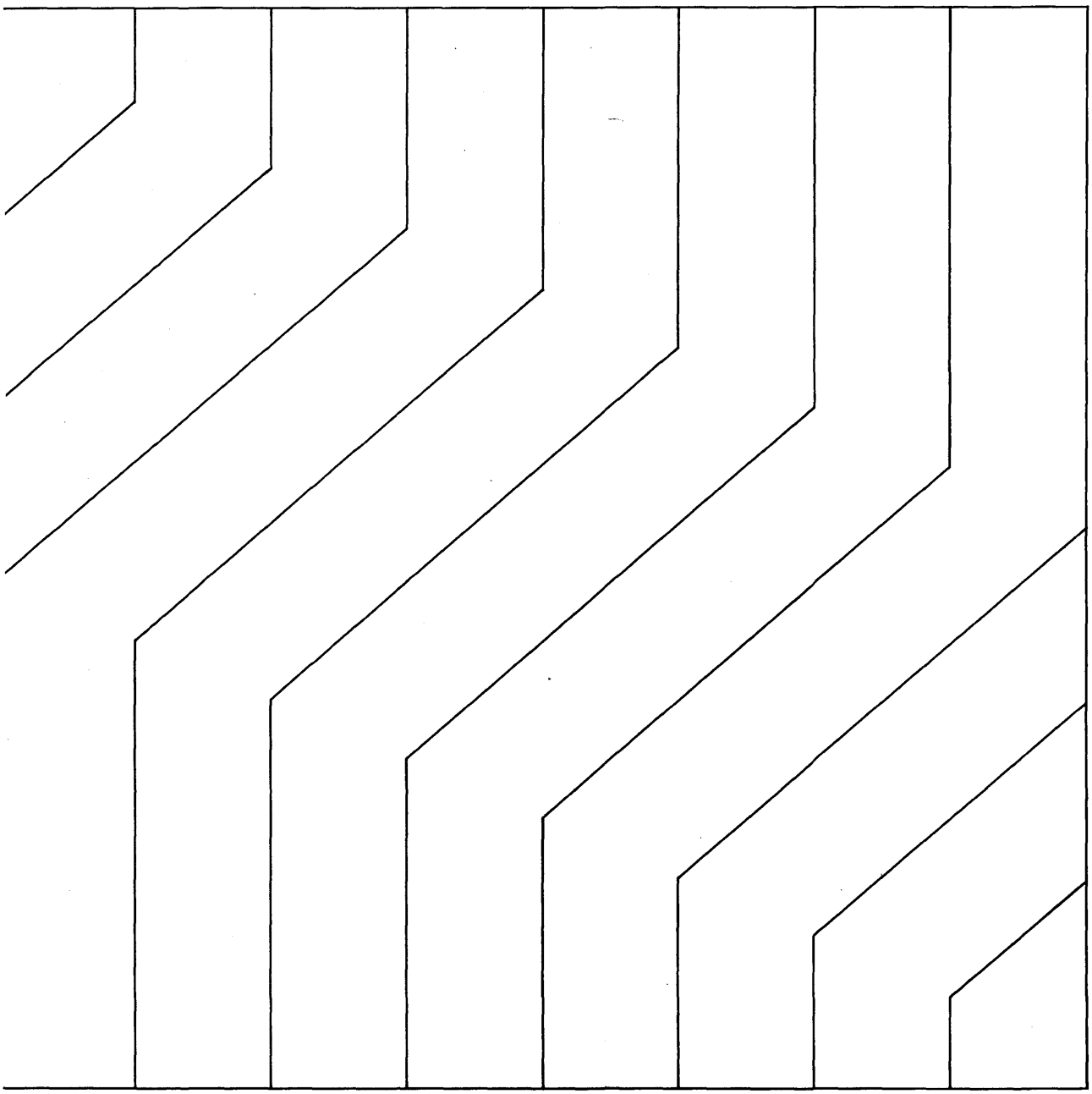


Am25S05

Four-Bit by Two-Bit 2's Complement Multiplier

Distinctive Characteristics

- Provides 2's complement multiplication at high speed without correction.
- Can be used in a combinatorial array or in a time sequenced mode.
- Multiplies two 12-bit signed numbers in typically 115ns.
- Multiplies in active HIGH (positive logic) or active LOW (negative logic) representations.
- Reduced input loading as compared to Am2505.
- 100% reliability assurance testing in compliance with MIL-STD-883.

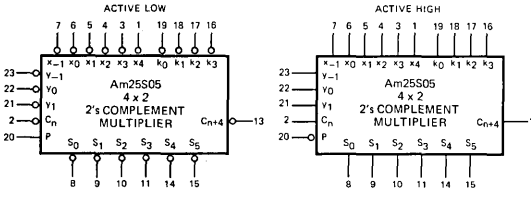
FUNCTIONAL DESCRIPTION:

The Am25S05 is a high-speed digital multiplier that can multiply numbers represented in the 2's complement notation and produce a 2's complement product without correction. The device consists of a 4x2 multiplier that can be connected to form iterative arrays able to multiply numbers either directly, or in a time sequenced arrangement. The device assumes that the most significant digit in a word carries a negative weight, and can therefore be used in arrays where the multiplicand and multiplier have different word lengths. The multiplier uses the quaternary algorithm and performs the function S = XY + K where K is the input field used to add partial products generated in the array. At the beginning of the array the K inputs are available to add a signed constant to the least significant part of the product. Multiplication of an m bit number by an n bit number in an array results in a product having m+n bits so that all possible combinations of product are accounted for. If a conventional 2's complement product is required the most significant bit can be ignored, and overflow conditions can be detected by comparing the last two product digits.

A number of connection schemes are possible. Figure 1 shows the connection scheme that results in the fastest multiply. If higher speed is required an array can be split into several parts, and the parts added with high-speed look-ahead carry adders.

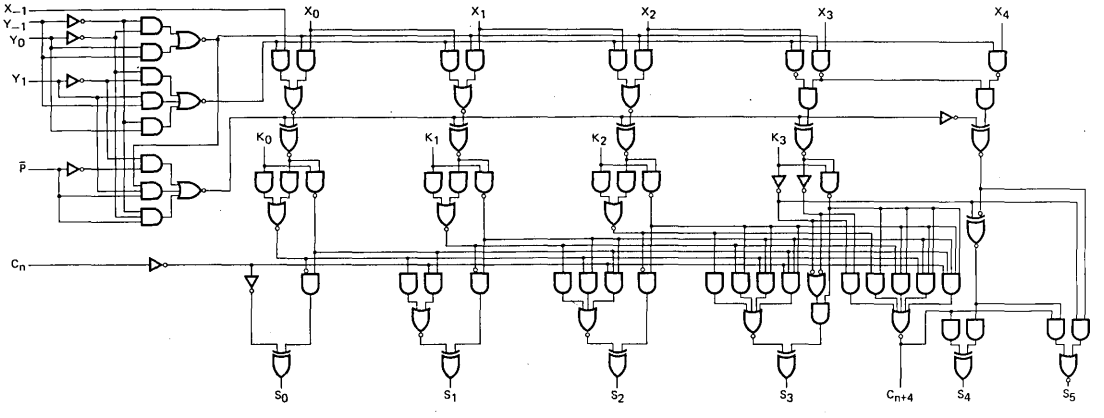
Provision is made in the design for multiplication in the active high (positive logic) or active low (negative logic) representations simply by reinterpreting the active level of the input operands, the product, and a polarity control $\overline{P}$. For a more complete description and applications the user is referred to the Am2505 Application Note.

LOGIC SYMBOLS



V_{CC} = Pin 24
GND = Pin 12

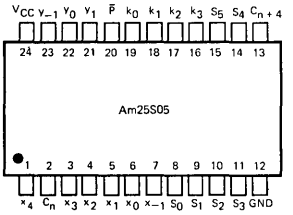
LOGIC DIAGRAM



Am25S05 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	AM25S05PC
Hermetic DIP	0°C to +75°C	AM25S05DC
Dice	0°C to +75°C	AM25S05XC
Hermetic DIP	−55°C to +125°C	AM25S05DM
Hermetic Flat Pak	−55°C to +125°C	AM25S05FM
Dice	−55°C to +125°C	AM25S05XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am25S05XC, DC, PC	T_A = 0°C to +75°C	V_{CC} = 4.75 V to 5.25 V
Am25S05XM, DM	T_A = −55°C to +125°C	V_{CC} = 4.50 V to 5.50 V
Am25S05FM	T_C = −55°C to +125°C	V_{CC} = 4.50 V to 5.50 V

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1.0mA V_{IN} = V_{IH} or V_{IL}	2.5	3.3		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}		0.3	0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V			−2.0	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			50	µA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V	−40		−100	mA
I_{CC}	Power Supply Current Am25S05XM	V_{CC} = MAX., y 1 = 0V		120	187	mA
I_{CC}	Power Supply Current Am25S05XC	V_{CC} = MAX., y 1 = 0V		120	187	mA

Note 1. Typical Limits are at V_{CC} = 5.0V, 25°C Ambient and maximum loading.
Note 2. Actual input currents are obtained by multiplying unit load current by the input load factor. (See loading rules)

Switching Characteristics (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF)

Parameters	From (Input)	To (Output)	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH} t_{PHL}	C_n	C_{n+4}	See Test Table	4 4	8 9	12 14	ns
t_{PLH} t_{PHL}	C_n	$S_{0,1,2,3}$		6 5	12 10	18 15	ns
t_{PLH} t_{PHL}	C_n	$S_{4,5}$		7 6	15 13	22 20	ns
t_{PLH} t_{PHL}	Any k	C_{n+4}		3 5	6.5 10	9 15	ns
t_{PLH} t_{PHL}	Any k	$S_{0,1,2,3}$		6 4	13.5 9.5	20 14	ns
t_{PLH} t_{PHL}	Any k	$S_{4,5}$		3 3	15.5 12.5	23 19	ns
t_{PLH} t_{PHL}	Any x	C_{n+4}		8 9	17 18	26 27	ns
t_{PLH} t_{PHL}	Any x	$S_{0,1,2,3}$		10 10	21 21	32 32	ns
t_{PLH} t_{PHL}	Any x	$S_{4,5}$		11 10	23.5 21.5	35 32	ns
t_{PLH} t_{PHL}	Any y	C_{n+4}		11 10	23 20	34 30	ns
t_{PLH} t_{PHL}	Any y	$S_{0,1,2,3}$		11 11	23 23	34 34	ns
t_{PLH} t_{PHL}	Any y	$S_{4,5}$		12 12	25 25	37 37	ns

SWITCHING TIME TEST TABLE

Input	Outputs	Inputs at 0V (remaining inputs at 4.5V)
C_n	C_{n+4}, S_{0123}, S_{45}	P, Y_{-1}, Y_1, All X
k_0	C_{n+4}, S_{0123}, S_{45}	P, Y_{-1}, Y_1, All X
k_1	C_{n+4}, S_{123}, S_{45}	P, Y_{-1}, Y_1, All X
k_2	C_{n+4}, S_{23}, S_{45}	P, Y_{-1}, Y_1, All X
k_3	S_3	P, Y_{-1}, Y_1, All X
k_3	S_{45}	P, Y_{-1}, Y_1, All X, C_n
x_{-1}	C_{n+4}, S_{0123}, S_{45}	P, Y_1, All k
x_0	C_{n+4}, S_{0123}, S_{45}	P, Y_{-1}, Y_1, All k
x_1	C_{n+4}, S_{123}, S_{45}	P, Y_{-1}, Y_1, All k
x_2	C_{n+4}, S_{123}, S_{45}	P, Y_{-1}, Y_1, All k
x_3	S_3	P, Y_{-1}, Y_1, All k
x_3	S_{45}	P, Y_{-1}, Y_1, All k, C_n
x_4	S_{45}	P, Y_1, All k, C_n
y_{-1}	C_{n+4}, S_{0123}, S_{45}	P, X_1, X_2, X_3, X_4, All k
y_0	C_{n+4}, S_{0123}, S_{45}	P, X_1, X_2, X_3, X_4, All k
y_1	C_{n+4}, S_{0123}, S_{45}	X_0, X_1, X_2, X_3, X_4, All k

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS

C_n The carry input to the high-speed adder.

C_{n+4} The carry output from the high-speed adder.

k_i The constant field used for accumulating partial products.

$i = 0, 1, 2, 3$. At the beginning of the array the K field can be used to add a 2's complement number to the least significant half of the double length product.

$\overline{P}$ The polarity control input. This input must be at a low-logic level for numbers in the active high logic representation, and held high for numbers in the active low logic representation.

S_i The product outputs. $i = 0, 1, 2, 3, 4, 5$.

x_i The multiplicand inputs. $i = -1, 0, 1, 2, 3, 4$. At the first column of the array x_{-1} must be held at logic '0', and at the last column of the array x_4 is connected to x_3.

y_i The multiplier inputs. $i = -1, 0, 1$.
At the first row of the array y_{-1} must be held at logic '0'.

OPERATIONAL TERMS:

I_{IL} Forward input load current.

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{CC} The current drawn by the device from V_{CC} power supply with input and output terminals open.

I_{IH} Reverse input load current.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{IN} Input voltage applied in I_{IL}, I_{IH} tests.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} flowing into output.

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 54/7400 Series	1.25	1.25
Advanced Micro Devices 9300/2500 Series	1.25	1.25
FSC Series 9300	1.25	1.25
TI Series 54/7400	1.25	1.25
Signetics Series 8200	2.5	2.5
National Series DM 75/85	1.25	1.25
DTL Series 930	15	1.25

OPERATION TABLE

Y Multiplier			Operation X Multiplicand
y_{-1}	y_0	y_1	
0	0	0	K + 0
1	0	0	K + X
0	1	0	K + X
1	1	0	K + 2X
0	0	1	K – 2X
1	0	1	K – X
0	1	1	K – X
1	1	1	K – 0

Active Low Inputs and Outputs
'1' = Low, '0' = High, P = High
Active High Inputs and Outputs
'1' = High, '0' = Low, $\overline{P}$ = Low

Am25S05 LOADING RULES IN UNIT LOADS

Input/Output	Pin No.'s	Input Unit Load Input HIGH	Input LOW	Fanout Output HIGH	Output LOW
x_4	1	0.2	0.2	–	–
C_n	2	0.2	0.2	–	–
x_3	3	0.2	0.2	–	–
x_2	4	0.4	0.4	–	–
x_1	5	0.4	0.4	–	–
x_0	6	0.4	0.4	–	–
x_{-1}	7	0.2	0.2	–	–
S_0	8	–	–	20	10
S_1	9	–	–	20	10
S_2	10	–	–	20	10
S_3	11	–	–	20	10
GND	12	–	–	–	–
C_{n+4}	13	–	–	20	10
S_4	14	–	–	20	10
S_5	15	–	–	20	10
k_3	16	2	2	–	–
k_2	17	2	2	–	–
k_1	18	2	2	–	–
k_0	19	2	2	–	–
$\overline{P}$	20	1	1	–	–
y_1	21	0.6	0.6	–	–
y_0	22	0.6	0.6	–	–
y_{-1}	23	0.6	0.6	–	–
V_{CC}	24	–	–	–	–

A Schottky TTL Unit Load is defined as 50μA at 2.7V at the HIGH Logic Level and –2.0 mA at 0.5 V at the LOW Logic Level.

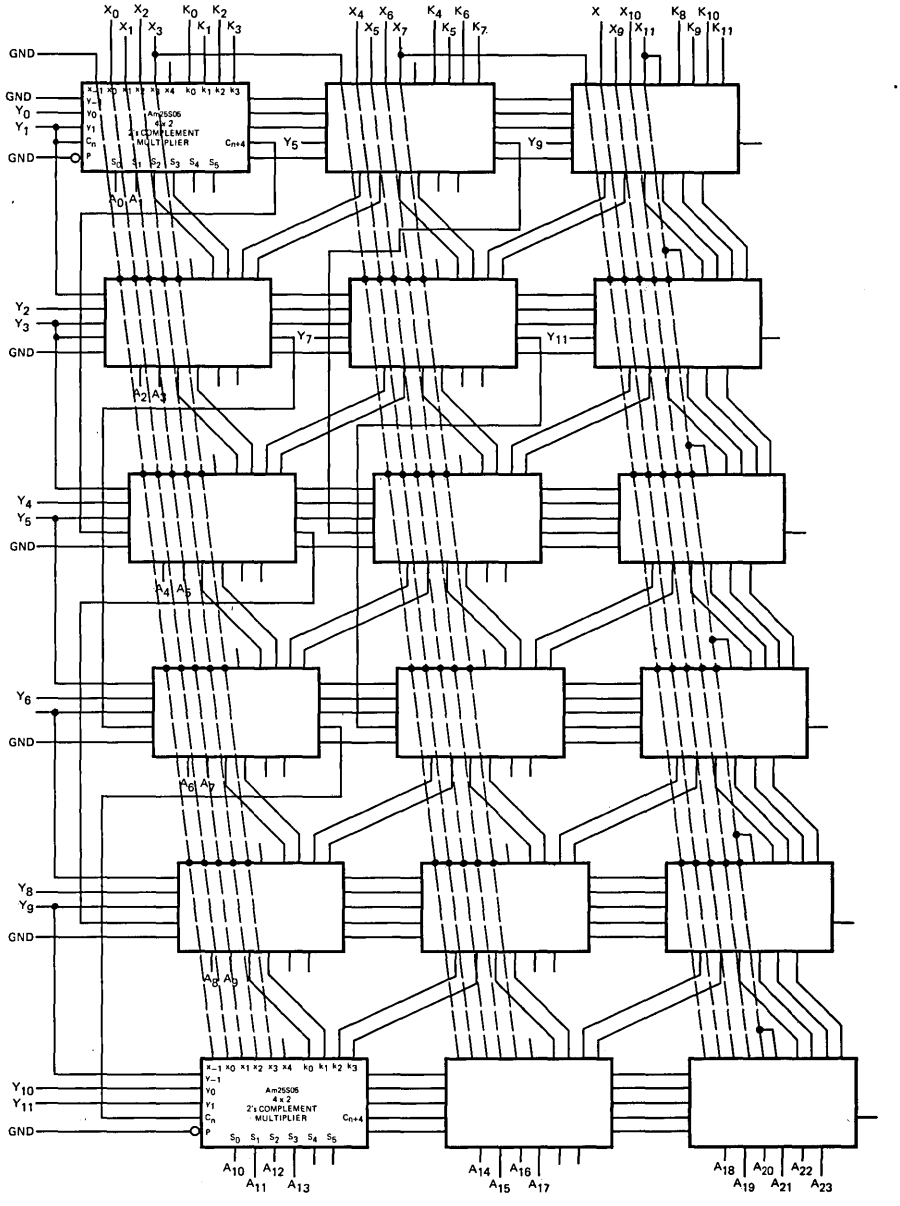
USER NOTES

1. Arithmetic in the multiplier is performed in the 2's complement notation, which requires a carry in at the first stage. This is accomplished by connecting the y_i multiplier bit to the appropriate carry input terminal i = 1, 3, 5 . . .
2. The multiplier can perform multiplication in either the active high (positive logic) or active low (negative logic) representations by reinterpreting the active logic level and by grounding or leaving the polarity control pin $\overline{P}$ open circuit respectively.
3. Multiplication can be performed in number representations other than 2's complement by either correcting the 2's complement product or adding in a correction at the beginning of the multiplication at the K inputs. 2's complement numbers are represented as: $X_2 = x - x_s 2^{n-1}$.

Number representation	Correction
2's complement	None
1's complement	Add $x_s Y_2 + y_s X_2 + x_s y_s$ at k inputs
Unsigned (magnitude)	Extend multiplier and multiplicand one bit at the least significant end. Form $x_0 y_0 + y_0 x + x_0 y$ with conditional adder and add to array shifted two places up at k inputs. Force $k_s, y_s, x_s = 0$.
Sign magnitude	$x_s = 0, y_s = 0$ None
	$x_s = 1, y_s = 0$ Form $[(XY)_2 + 2^{n-1} y]$
	$x_s = 0, y_s = 1$ Form $[(XY)_2 + 2^{n-1} x]$
	$x_s = 1, y_s = 1$ Add $2^{n-1}(x + y) - 2^{2n-2}$

4. For the highest speed array with the multipliers arranged in a parallelogram structure carries between certain multipliers are exchanged with the y carry-ins needed for 2's complement subtract. The delays in the array are then equalized as best possible as shown in Figure 1.
5. For higher speed multiplication the array can be split into several parts that can be added together with high-speed adders.
6. Rounding off to a single length product can be achieved by adding a '1' to the array at the most significant positive k input of the array, ignoring the most significant product digit, and using the remainder of the most significant part of the product.
7. Truncation of a product without round off enables some of the multipliers in the array to be removed.

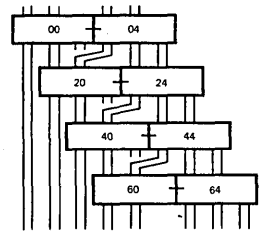
APPLICATION



Critical speed carries between columns have been interchanged with 2's complement carry-ins Y_5, Y_7, Y_9, Y_{11} for highest speed.

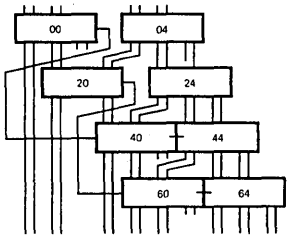
Figure 1. High Speed 12x12 2's Complement Multiplication

CONNECTION SCHEMES



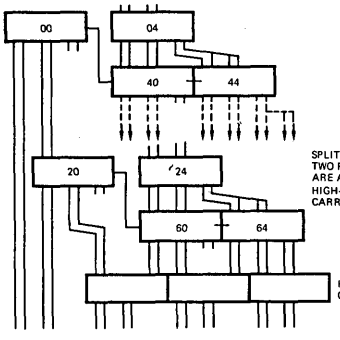
1

PARALLELOGRAM CARRIES STAY IN SAME ROW



2

PARALLELOGRAM CARRIES FROM LOWER ORDER MULTIPLIERS SKIP TO ALTERNATE ROWS WHERE POSSIBLE



3

SPLIT INTO TWO PARTS WHICH ARE ADDED WITH HIGH-SPEED CARRY LOOKAHEAD ADDER

HIGH-SPEED SCHOTTKY CARRY LOOKAHEAD ADDER

TYPICAL MULTIPLICATION TIMES

Array Size Bits	Total Multiplication Time (ns)	Package Count	
		Am25S05	Am54S/74S181
4x4	35	2	
8x8	75	8	
12x12	115	18	
12x12	82	18	5
16x16	155	32	
16x16	111	32	7
16x16	98	32	16
20x20	195	50	
20x20	130	50	9
24x24	235	72	
24x24	149	72	11
24x24	125	72	24
28x28	275	98	
28x28	168	98	13
32x32	315	128	
32x32	187	128	15
32x32	152	128	32

Am25S05

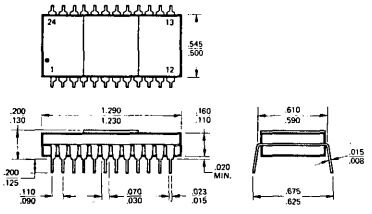
$Y = (y_{-1}\, y_0\, y_1)\, 2^A$

$X = (x_{-1}\, x_0\, x_1\, x_2\, x_3)\, 2^B$

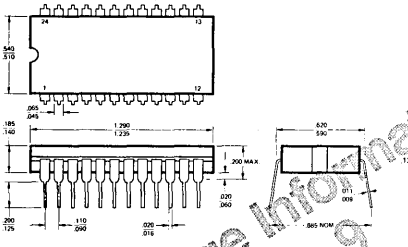
Fig. 2

PHYSICAL DIMENSIONS
Dual-In-Line

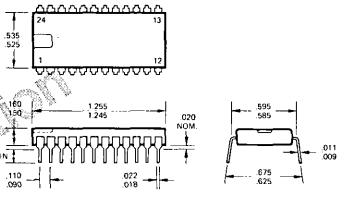
Hermetic



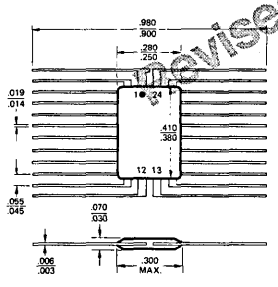
Ceramic



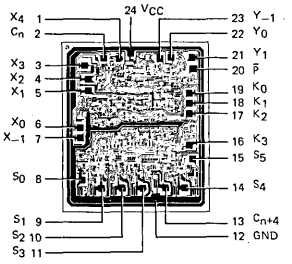
Molded



Flat Package



Metallization and Pad Layout



DIE SIZE 0.095" x 0.110"

ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am25S07•Am25S08

Hex/Quad Parallel D Registers With Register Enable

Distinctive Characteristics

- 4-bit and 6-bit high-speed parallel registers
- Common clock and common enable
- Positive edge triggered D flip-flops
- 100% reliability assurance testing in compliance with MIL-STD-883.

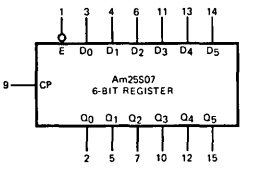
FUNCTIONAL DESCRIPTION

The Am25S07 is a 6-bit, high-speed Schottky register with a buffered common register enable. The Am25S08 is a 4-bit register with a buffered common register enable. The devices are similiar to the Am54S/74S174 and Am54S/74S175 but feature the common register enable rather than common clear.

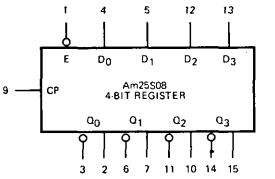
Both registers will find application in digital systems where information is associated with a logic gating signal. When the enable is LOW, data on the D inputs is stored in the register on the positive going edge of the clock pulse. When the enable is HIGH, the register will not change state regardless of the clock or data input transitions.

LOGIC SYMBOLS

Am25S07



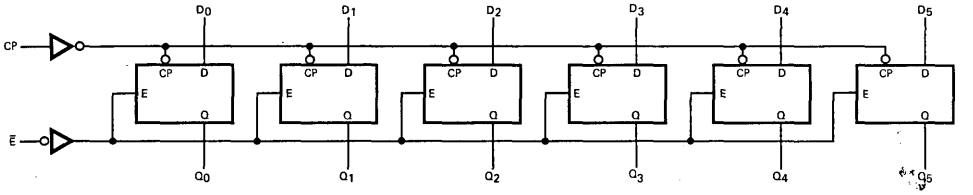
Am25S08



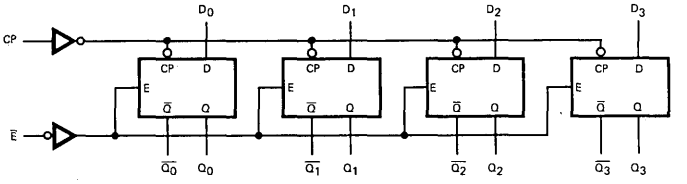
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAMS

Am25S07



Am25S08

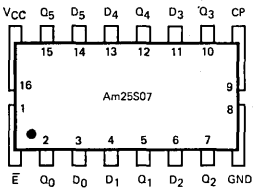


ORDERING INFORMATION

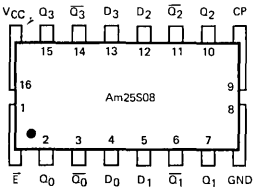
Package Type	Temperature Range	Am25S07 Order Number	Am25S08 Order Number
Molded DIP	0°C to +70°C	AM25S07PC	AM25S08PC
Hermetic DIP	0°C to +70°C	AM25S07DC	AM25S08DC
Dice	0°C to +70°C	AM25S07XC	AM25S08XC
Hermetic DIP	–55°C to +125°C	AM25S07DM	AM25S08DM
Hermetic Flat Pak	–55°C to +125°C	AM25S07FM	AM25S08FM
Dice	–55°C to +125°C	AM25S07XM	AM25S08XM

CONNECTION DIAGRAMS
Top Views

Am25S07



Am25S08



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am25S07XC, Am25S08XC T_A = 0°C to +70°C V_{CC} = 5.0 V ±5% (COM'L) MIN. = 4.75 V MAX. = 5.25 V
Am25S07XM, Am25S08XM T_A = −55°C to +125°C V_{CC} = 5.0 V ±10% (MIL) MIN. = 4.5 V MAX. = 5.5 V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1 mA V_{IN} = V_{IH} or V_{IL}	XC	2.7	3.4		Volts
			XM	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20 mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18 mA				−1.2	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5 V				−2	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7 V				50	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0 V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.	S07		90	144	mA
			S08		60	96	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Outputs open; enable grounded; data inputs at 4.5V, measured after a momentary ground, then 4.5V applied to the clock input.

Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Clock to Output	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 280 Ω	4	8	12	ns
t_{PHL}	Clock to Output		4	11.5	17	ns
t_{pw}	Clock Pulse Width		7			ns
t_s	Data		5.5			ns
t_s	Enable			7		ns
t_h	Data		3	0		ns
t_h	Enable		3	0		ns

Am25S07 LOADING RULES
(In STTL Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{E}$	1	1	–	–
Q_0	2	–	20	10
D_0	3	1	–	–
D_1	4	1	–	–
Q_1	5	–	20	10
D_2	6	1	–	–
Q_2	7	–	20	10
GND	8	–	–	–
CP	9	1	–	–
Q_3	10	–	20	10
D_3	11	1	–	–
Q_4	12	–	20	10
D_4	13	1	–	–
D_5	14	1	–	–
Q_5	15	–	20	10
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and –2.0mA measured at 0.5V LOW.

Am25S08 LOADING RULES
(In STTL Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{E}$	1	1	–	–
Q_0	2	–	20	10
$\overline{Q}_0$	3	–	20	10
D_0	4	1	–	–
D_1	5	1	–	–
$\overline{Q}_1$	6	–	20	10
Q_1	7	–	20	10
GND	8	–	–	–
CP	9	1	–	–
Q_2	10	–	20	10
$\overline{Q}_2$	11	–	20	10
D_2	12	1	–	–
D_3	13	1	–	–
$\overline{Q}_3$	14	–	20	10
Q_3	15	–	20	10
V_{CC}	16	–	–	–

DEFINITION OF FUNCTIONAL TERMS

D_i The D flip-flop data inputs.

$\overline{E}$ Enable. When the enable is LOW, data on the D_i inputs is transferred to the Q_i outputs on the LOW-to-HIGH clock transition. When the enable is HIGH, the Q_i outputs do not change regardless of the data or clock input transitions.

CP Clock Pulse for the register. Enters data on the LOW-to-HIGH transition.

Q_i The TRUE register outputs.

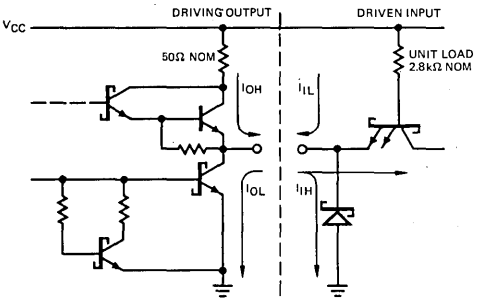
$\overline{Q}_i$ The complement register outputs

FUNCTION TABLE

Inputs			Outputs	
$\overline{E}$	D_i	CP	Q_i	$\overline{Q}_i$
H	X	X	NC	NC
L	X	H	NC	NC
L	X	L	NC	NC
L	L	↑	L	H
L	H	↑	H	L

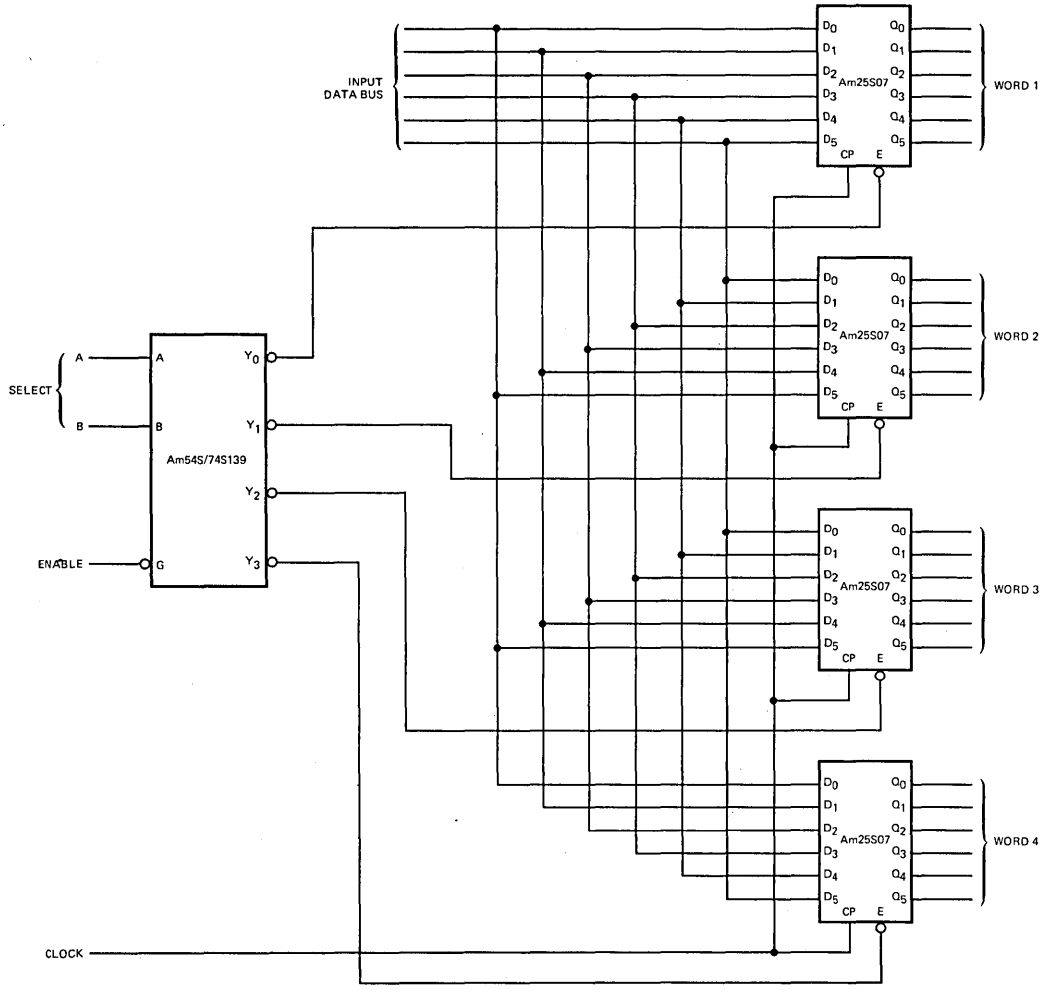
H = HIGH NC = No Change
L = LOW X = Don't Care
↑ = LOW-to-HIGH Transition
$\overline{Q}_i$ on Am25S08 Only

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



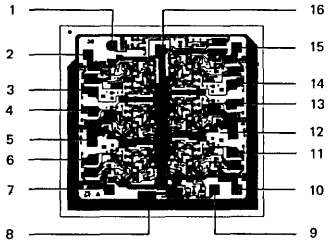
Note: Actual current flow direction shown.

APPLICATIONS



Selective Register Loading of Data on Synchronous Clock.

Pad Layout



DIE SIZE 0.085" X 0.081"

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

f_{MAX} The highest operating clock frequency.

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{PW} Pulse width. The time between the leading and trailing edges of a pulse.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

t_s Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

t_h Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.

t_R Release time. The time interval for which a signal may be indeterminant at one input terminal before an active transition occurs at another input terminal. (The release time falls within the set-up time interval and is specified by some manufacturers as a negative hold time).

UNIT LOAD DEFINITIONS

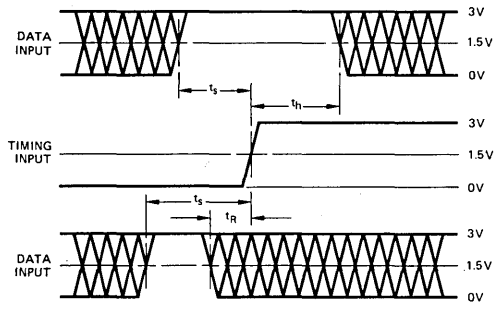
	HIGH		LOW	
SERIES	Current	Measure Voltage	Current	Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0mA	0.5V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

Note: 1. 54L/74L has two different types of standard inputs.

SCHOTTKY PARAMETER MEASUREMENTS

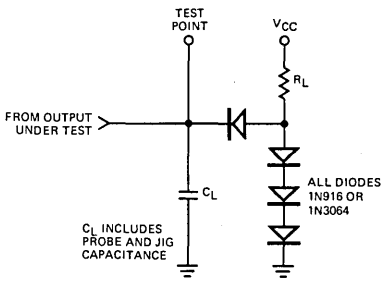
FOR STANDARD ACTIVE-PULLUP TOTEM-POLE OUTPUTS

SET-UP, HOLD, AND RELEASE TIMES

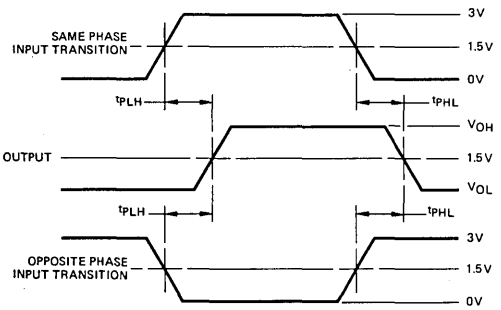


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched area is don't care condition.

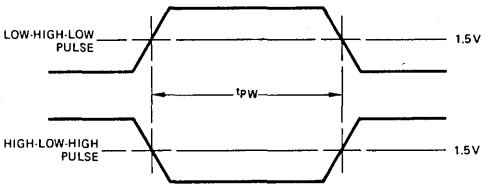
LOAD TEST CIRCUIT



PROPAGATION DELAY

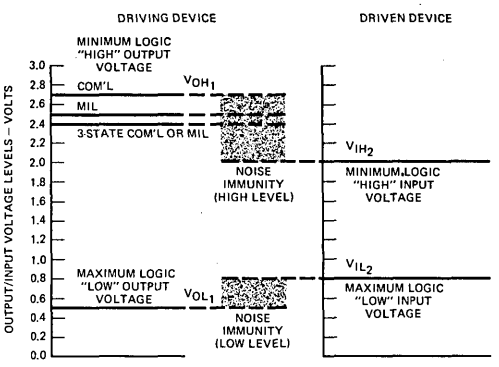


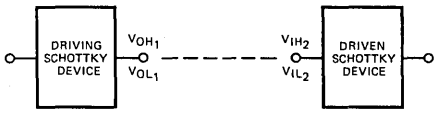
PULSE WIDTH



Note: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_o = 50\Omega$, $t_r \leq 2.5$ns; $t_f \leq 2.5$ns.

SCHOTTKY INPUT/OUTPUT VOLTAGE INTERFACE CONDITIONS





Note: Refer to Electrical Characteristics for measure currents.

DEFINITION OF STANDARD TERMS

H HIGH, applying to a HIGH voltage level.

L LOW, applying to a LOW voltage level.

I Input.

O Output.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

I_{IL} LOW-level input current with a specified LOW-level voltage applied.

I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.

I_{OL} LOW-level output current.

I_{OH} HIGH-level output current.

I_{SC} Output short-circuit source current.

I_{CC} The supply current drawn by the device from the V_{CC} power supply.

V_{IL} Logic LOW input voltage.

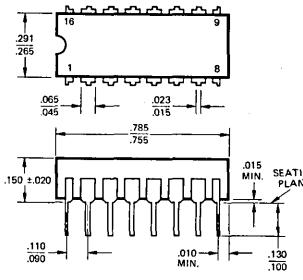
V_{IH} Logic HIGH input voltage.

V_{OL} LOW-level output voltage with I_{OL} applied.

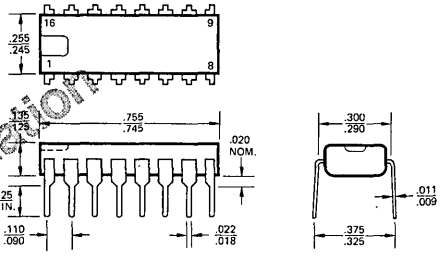
V_{OH} HIGH-level output voltage with I_{OH} applied.

PHYSICAL DIMENSIONS
Dual-In-Line

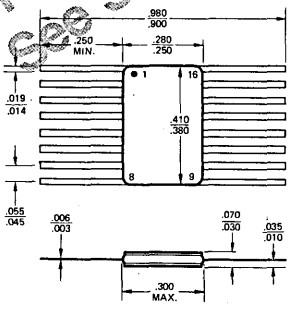
Molded



Ceramic



Flat Package



ADVANCED MICRO DEVICES INC.
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Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am25S09

Quad Two-Input, High-Speed Register

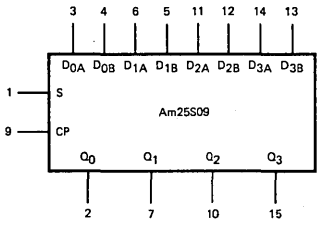
Distinctive Characteristics

- Four-bit register accepts data from one of two 4-bit input fields.
- Edge triggered clock action
- High-speed Schottky technology.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

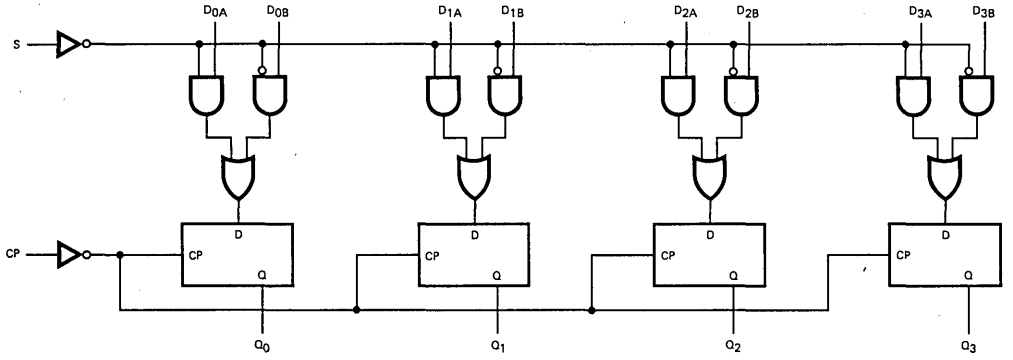
The Am25S09 is a dual port high-speed, four-bit register using advanced Schottky technology to reduce the effect of transistor storage time. The register consists of four D flip-flops with a buffered common clock, and a two-input multiplexer at the input of each flip-flop. A common select line, S, controls the four multiplexers. Data on the four inputs selected by the S line is stored in the four flip-flops at the clock LOW-to-HIGH transition. When the S input is LOW, the D_{iA} input data will be stored in the register. When the S input is HIGH, the D_{iB} input data will be stored in the register.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

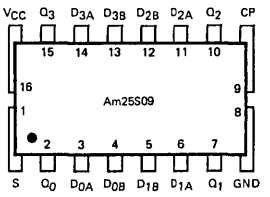
LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM25S09PC
Hermetic DIP	0°C to +70°C	AM25S09DC
Dice	0°C to +70°C	AM25S09XC
Hermetic DIP	−55°C to +125°C	AM25S09DM
Hermetic Flat Pak	−55°C to +125°C	AM25S09FM
Dice	−55°C to +125°C	AM25S09XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am25S09XC T_A = 0°C to +70°C V_{CC} = 5.0 V ± 5% (COM'L) MIN. = 4.75 V MAX. = 5.25 V
Am25S09XM T_A = −55°C to +125°C V_{CC} = 5.0 V ± 10% (MIL) MIN. = 4.5 V MAX. = 5.5 V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1.0mA V_{IN} = V_{IH} or V_{IL}	COM'L	2.7	3.4		Volts
			MIL	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20.0mA V_{IN} = V_{IH} or V_{IL}			0.3	0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5 V				−2.0	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7 V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0 V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)			75	120	mA

Notes: 1. For conditions shown as MIN. or MAX. use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Measured with Select and Clock inputs at 4.5V; all data inputs at 0V; all outputs open.

Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Clock to Q HIGH	V_{CC} = 5.0 V, C_L = 15pF, R_L = 280Ω		8	12	ns
t_{PHL}	Clock to Q LOW			11.5	17	ns
t_{pw}	Clock Pulse Width		7			ns
t_s	Data Set-up Time		5.5			ns
t_s	Select Input Set-up Time			7		ns
t_h	Data Hold Time		3			ns
t_h	Select Input Hold Time		3			ns

FUNCTION TABLE

SELECT S	CLOCK CP	DATA D_{iA}	INPUTS D_{iB}	OUTPUT Q_i
L	↑	L	X	L
L	↑	H	X	H
H	↑	X	L	L
H	↑	X	H	H

H = HIGH Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition

L = LOW Voltage Level
i = 0, 1, 2, or 3

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
S	1	1	–	–
Q_0	2	–	20	10
D_{0A}	3	1	–	–
D_{0B}	4	1	–	–
D_{1B}	5	1	–	–
D_{1A}	6	1	–	–
Q_1	7	–	20	10
GND	8	–	–	–
CP	9	1	–	–
Q_2	10	–	20	10
D_{2A}	11	1	–	–
D_{2B}	12	1	–	–
D_{3B}	13	1	–	–
D_{3A}	14	1	–	–
Q_3	15	–	20	10
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50 μA measured at 2.7 V HIGH and −2.0 mA measured at 0.5 V LOW.

DEFINITION OF FUNCTIONAL TERMS

D_{0A}, D_{1A}, D_{2A}, D_{3A} The "A" word into the two-input multiplexer of the D flip-flops.

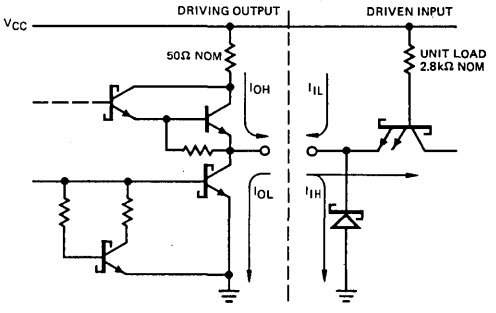
D_{0B}, D_{1B}, D_{2B}, D_{3B} The "B" word into the two-input multiplexer of the D flip-flops.

Q_0, Q_1, Q_2, Q_3 The outputs of the four D-type flip-flops of the register.

S Select. When the select is LOW, the A word is applied to the D inputs of the flip-flops. When the select is HIGH the B word is applied to the D inputs of the flip-flops.

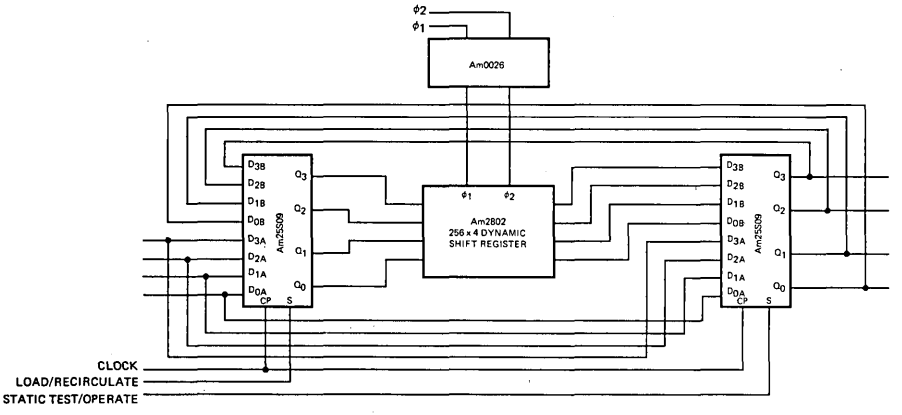
CP Clock Pulse. Clock pulse for the register. Enters data on the LOW-to-HIGH transition of the clock line.

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

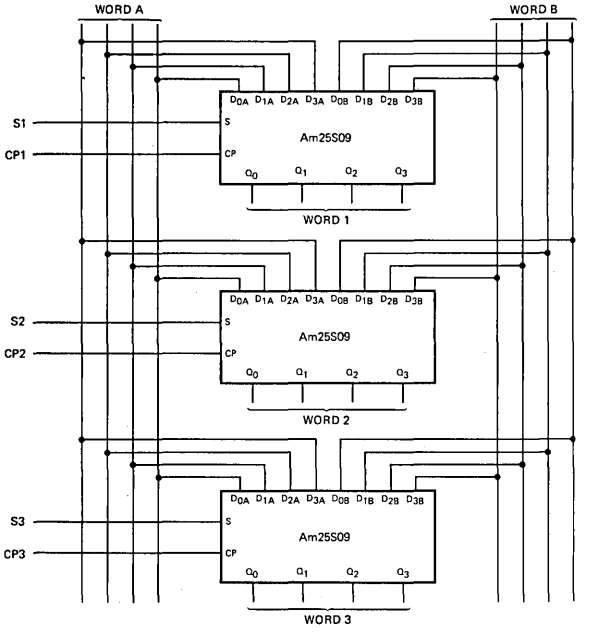


Note: Actual current flow direction shown

APPLICATIONS

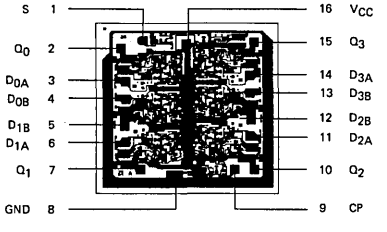


Am25S09 used in 258 x 4 memory system with load/recirculate control, and 1 x 4 static test capability for the system. MOS interface is one load at each end. This circuit is especially useful in digital filtering where special algorithms require a static single step operation for testing purposes.



Am25S09 used to store a word from either data bus A or data bus B.

Metallization and Pad Layout



DIE SIZE 0.085" X 0.081"

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

f_{MAX} The highest operating clock frequency.

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{PW} Pulse width. The time between the leading and trailing edges of a pulse.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

t_s Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

t_h Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.

t_R Release time. The time interval for which a signal may be indeterminant at one input terminal before an active transition occurs at another input terminal. (The release time falls within the set-up time interval and is specified by some manufacturers as a negative hold time).

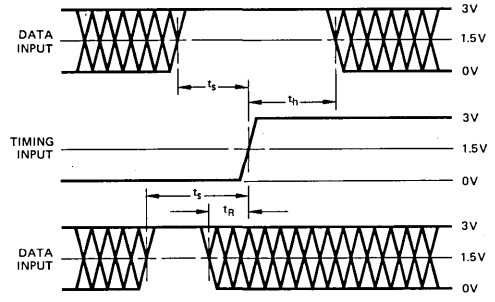
UNIT LOAD DEFINITIONS

	HIGH		LOW	
SERIES	Current	Measure Voltage	Current	Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0 mA	0.5 V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

Note: 1. 54L/74L has two different types of standard inputs.

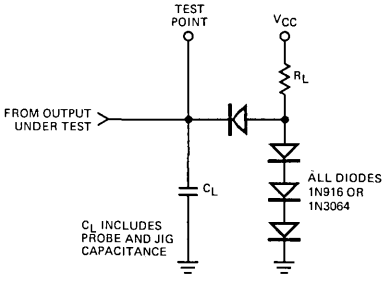
SCHOTTKY PARAMETER MEASUREMENTS
FOR STANDARD ACTIVE-PULLUP TOTEM-POLE OUTPUTS

SET-UP, HOLD, AND RELEASE TIMES

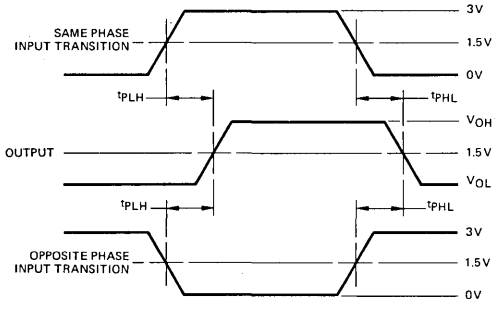


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched area is don't care condition.

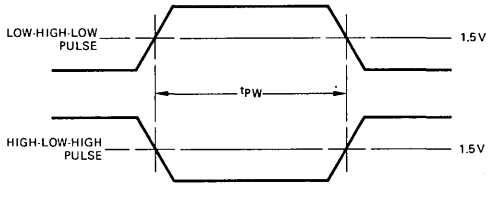
LOAD TEST CIRCUIT



PROPAGATION DELAY

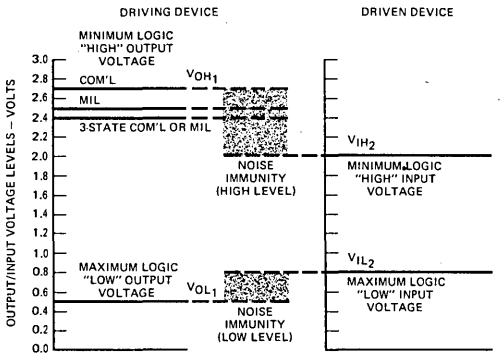


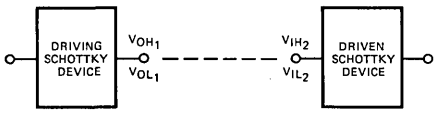
PULSE WIDTH



Notes: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_o = 50Ω; t_r ≤ 2.5ns; t_f ≤ 2.5ns.

SCHOTTKY INPUT/OUTPUT VOLTAGE INTERFACE CONDITIONS





Note: Refer to Electrical Characteristics for measure currents.

DEFINITION OF STANDARD TERMS

H HIGH, applying to a HIGH voltage level.

L LOW, applying to a LOW voltage level.

I Input.

O Output.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

I_{IL} LOW-level input current with a specified LOW-level voltage applied.

I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.

I_{OL} LOW-level output current.

I_{OH} HIGH-level output current.

I_{SC} Output short-circuit source current.

I_{CC} The supply current drawn by the device from the V_{CC} power supply.

V_{IL} Logic LOW input voltage.

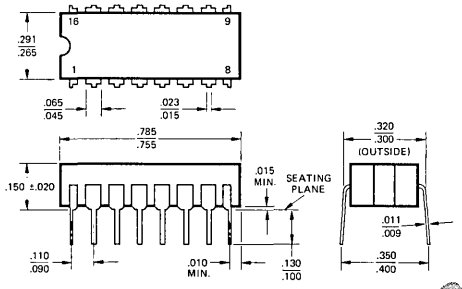
V_{IH} Logic HIGH input voltage.

V_{OL} LOW-level output voltage with I_{OL} applied.

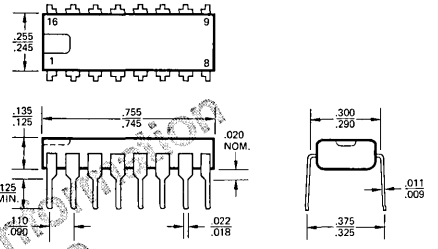
V_{OH} HIGH-level output voltage with I_{OH} applied.

PHYSICAL DIMENSIONS
Dual-In-Line

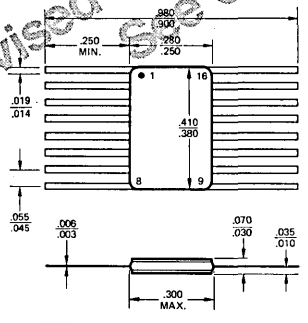
Ceramic



Molded



Flat Package



ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am25S10

Four-Bit Shifter With Three-State Outputs

Distinctive Characteristics

Shifts 4-bits of data to 0, 1, 2 or 3 places under control of two select lines.

Three-state outputs for bus organized systems.

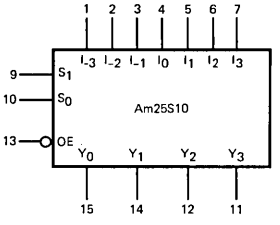
- 6.5ns typical data propagation delay.
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

The Am25S10 is a combinatorial logic circuit that accepts a four-bit data word and shifts the word 0, 1, 2 or 3 places. The number of places to be shifted is determined by a two-bit select field S_0 and S_1. An active-LOW enable controls the three-state outputs. This feature allows expansion of shifting over a larger number of places with one delay.

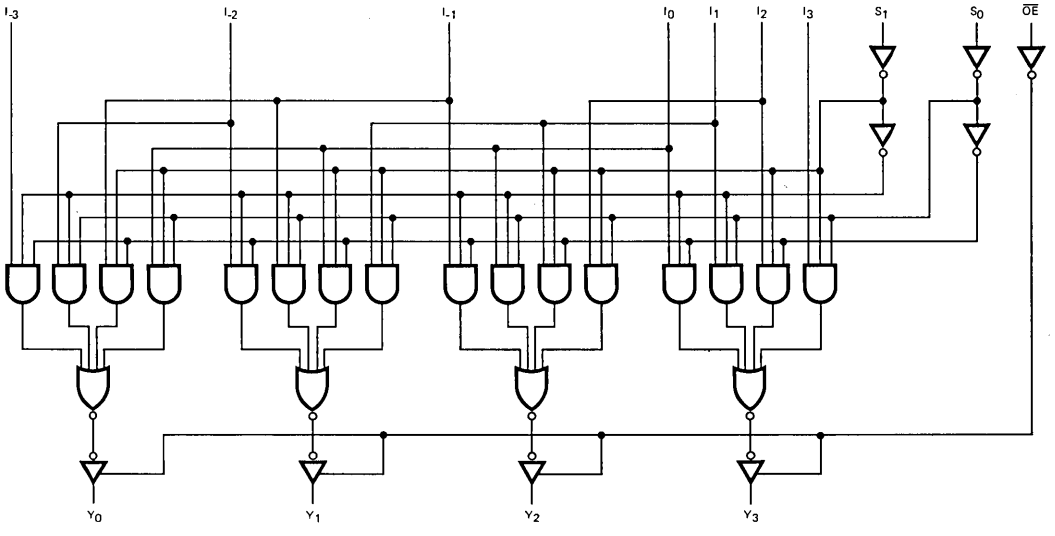
By suitable interconnection, the Am25S10 can be used to shift any number of bits any number of places up or down. Shifting can be logical, with logic zeroes pulled in at either or both ends of the shifting field; arithmetic, where the sign bit is repeated during a shift down; or end around, where the data word forms a continuous loop.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

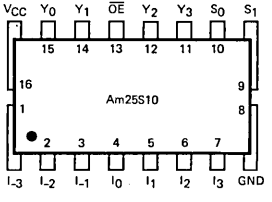
LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM25S10PC
Hermetic DIP	0°C to +70°C	AM25S10DC
Dice	0°C to +70°C	AM25S10XC
Hermetic DIP	−55°C to +125°C	AM25S10DM
Hermetic Flat Pak	−55°C to +125°C	AM25S10FM
Dice	−55°C to +125°C	AM25S10XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am25S10XC T_A = 0°C to +70°C V_{CC} = 5.0 V ±5% (COM'L) MIN. = 4.75 V MAX. = 5.25 V
Am25S10XM T_A = −55°C to +125°C V_{CC} = 5.0 V ±10% (MIL) MIN. = 4.5 V MAX. = 5.5 V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	XM I_{OH} = −2mA	2.4	3.4		Volts
			XC I_{OH} = −6.5mA	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5 V				−2.0	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7 V				50	µA
I_O	Off State (High Impedance) Output Current	V_{CC} = MAX.	V_O = 2.4 V			50	µA
			V_O = 0.5 V			−50	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0 V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All outputs open, All inputs = GND			60	85	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Data Input to Output	V_{CC} = 5.0 V, C_L = 15pF, R_L = 280Ω		5	7.5	ns
t_{PHL}				8	12	
t_{PLH}	Select to Output			11	17	ns
t_{PHL}				13	20	
t_{ZH}	Output Control $\overline{OE}$ to Output				19.5	ns
t_{ZL}					21	
t_{HZ}	Output Control $\overline{OE}$ to Output	V_{CC} = 5 V, C_L = 5pF, R_L = 280Ω		5	8	ns
t_{LZ}				10	15	

DEFINITION OF FUNCTIONAL TERMS

I_i The seven data inputs of the shifter.

$\overline{OE}$ Enable. When the enable is HIGH, the four outputs are in the high impedance state. When the enable is LOW, the selected I_i inputs are present at the outputs.

S_0, S_1 Select inputs. Controls the number of places the inputs are shifted.

Y_i The four outputs of the shifter.

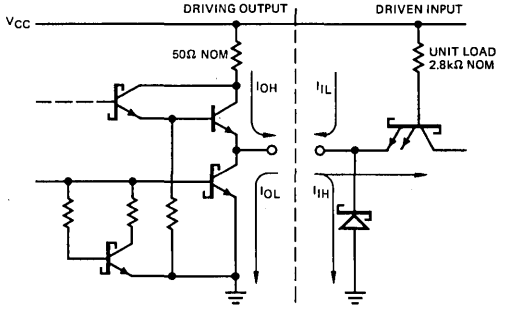
LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load (Note 1)	Fan-out Output HIGH XM	Fan-out Output HIGH XC	Fan-out Output LOW
I_{-3}	1	1	–	–	–
I_{-2}	2	1.5	–	–	–
I_{-1}	3	1.5	–	–	–
I_0	4	1.5	–	–	–
I_1	5	1.5	–	–	–
I_2	6	1.5	–	–	–
I_3	7	1	–	–	–
GND	8	–	–	–	–
S_1	9	1	–	–	–
S_0	10	1	–	–	–
Y_3	11	–	40	130	10
Y_2	12	–	40	130	10
$\overline{OE}$	13	1	–	–	–
Y_1	14	–	40	130	10
Y_0	15	–	40	130	10
V_{CC}	16	–	–	–	–

A Schottky TTL Unit Load is defined as 50 μA measured at 2.7 V HIGH and −2.0mA measured at 0.5V LOW.

Note: 1. The fan-in on I_{-2}, I_{-1}, I_0, I_1 and I_2 will not exceed 1.5 Unit Loads when measured at V_{IL} = 0.5 V. As V_{IL} is decreased to 0 V, the input current I_{IL} MAX. increases to −4, −6, −8, −6 and −4 mA respectively due to the decrease in current sharing with the internal select buffer outputs.

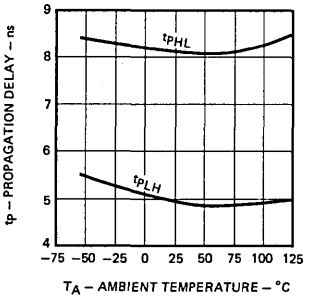
SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



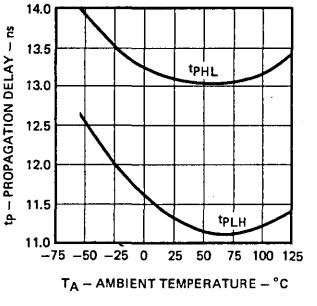
Note: Actual current flow direction shown.

PERFORMANCE CURVES
SWITCHING CHARACTERISTICS

Data to Output (Typical)



Select to Output (Typical)



LOGIC EQUATIONS

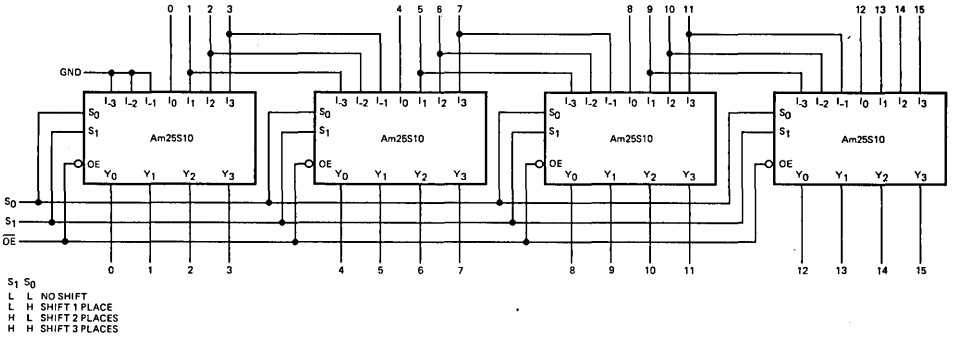
$$Y_0 = \overline{S}_0 \overline{S}_1 I_0 + S_0 \overline{S}_1 I_{-1} + \overline{S}_0 S_1 I_{-2} + S_0 S_1 I_{-3}$$
$$Y_1 = \overline{S}_0 \overline{S}_1 I_1 + S_0 \overline{S}_1 I_0 + \overline{S}_0 S_1 I_{-1} + S_0 S_1 I_{-2}$$
$$Y_2 = \overline{S}_0 \overline{S}_1 I_2 + S_0 \overline{S}_1 I_1 + \overline{S}_0 S_1 I_0 + S_0 S_1 I_{-1}$$
$$Y_3 = \overline{S}_0 \overline{S}_1 I_3 + S_0 \overline{S}_1 I_2 + \overline{S}_0 S_1 I_1 + S_0 S_1 I_0$$

TRUTH TABLE

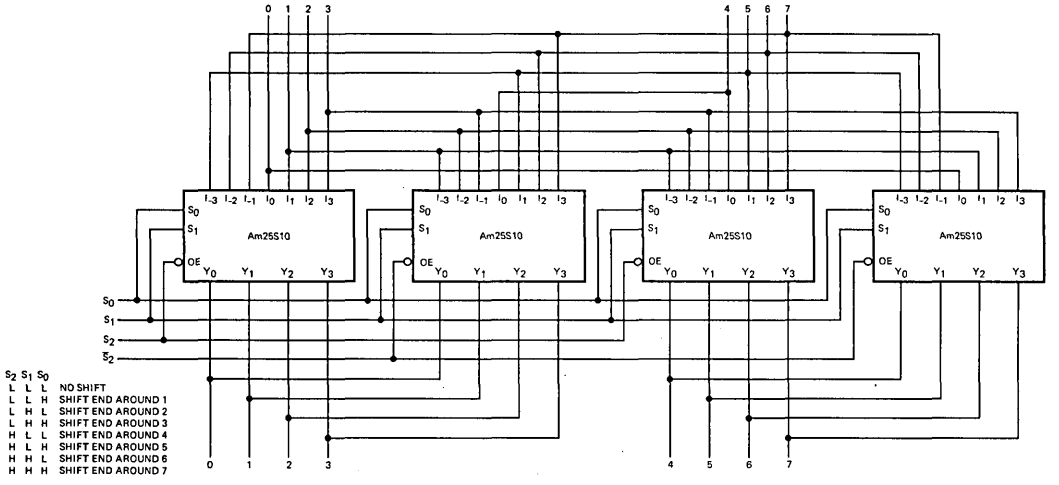
$\overline{OE}$	S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_3	Y_2	Y_1	Y_0
H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z
L	L	L	D_3	D_2	D_1	D_0	X	X	X	D_3	D_2	D_1	D_0
L	L	H	X	D_2	D_1	D_0	D_{-1}	X	X	D_2	D_1	D_0	D_{-1}
L	H	L	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_1	D_0	D_{-1}	D_{-2}
L	H	H	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_0	D_{-1}	D_{-2}	D_{-3}

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance State
D_n at input I_n may be either HIGH or LOW and output Y_m will follow the selected D_n input level.

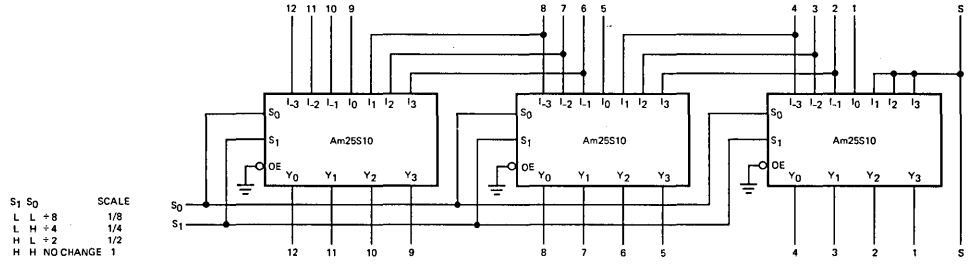
APPLICATIONS



16-Bit Shift-Up 0, 1, 2, or 3 Places

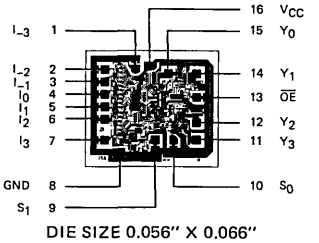


8-Bit End Around Shift 0, 1, 2, 3, 4, 5, 6, 7 Places



13-Bit 2's Complement Scaler

Metallization and Pad Layout



DIE SIZE 0.056" X 0.066"

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

f_{MAX} The highest operating clock frequency.

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{PW} Pulse width. The time between the leading and trailing edges of a pulse.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

t_s Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

t_h Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.

t_R Release time. The time interval for which a signal may be indeterminant at one input terminal before an active transition occurs at another input terminal. (The release time falls within the set-up time interval and is specified by some manufacturers as a negative hold time).

t_{HZ} HIGH to disable. The delay time from a control input change to the three-state output HIGH-level to high-impedance transition (measured at 0.5 V change).

t_{LZ} LOW to disable. The delay time from a control input change to the three-state output LOW-level to high-impedance transition (measured at 0.5 V change).

t_{ZH} Enable HIGH. The delay time from a control input change to the three-state output high-impedance to HIGH-level transition.

t_{ZL} Enable LOW. The delay time from a control input change to the three-state output high-impedance to LOW-level transition.

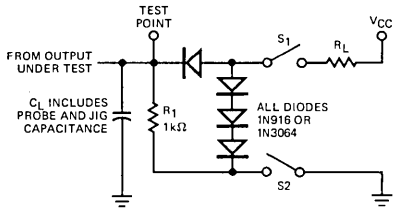
UNIT LOAD DEFINITIONS

	HIGH		LOW	
SERIES	Current	Measure Voltage	Current	Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0mA	0.5V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

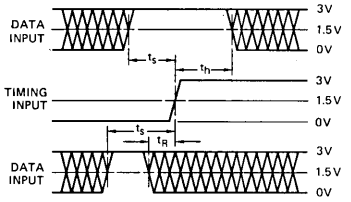
Note: 1. 54L/74L has two different types of standard inputs.

SCHOTTKY PARAMETER MEASUREMENTS FOR THREE-STATE OUTPUTS

LOAD TEST CIRCUIT

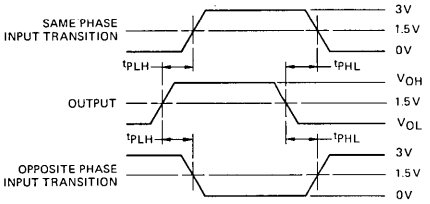


SET-UP, HOLD, AND RELEASE TIMES

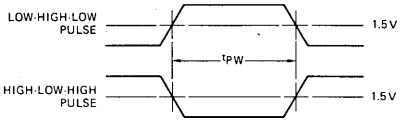


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

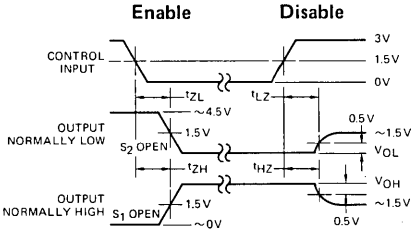
PROPAGATION DELAY



PULSE WIDTH



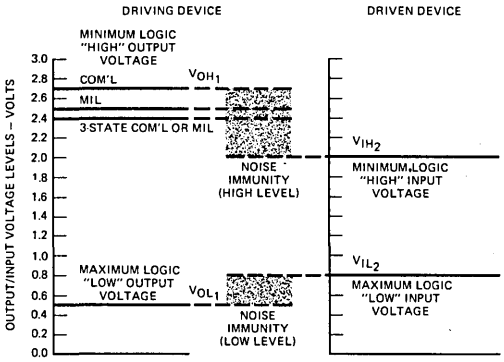
ENABLE AND DISABLE TIMES

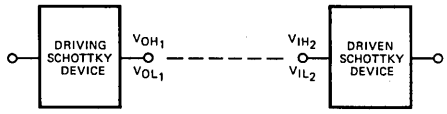


Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1 and S_2 of Load Circuit are closed except where shown.

Note: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_o = 50Ω; t_r ≤ 2.5 ns; t_f ≤ 2.5 ns.

SCHOTTKY INPUT/OUTPUT VOLTAGE INTERFACE CONDITIONS





Note: Refer to Electrical Characteristics for measure current.

DEFINITION OF STANDARD TERMS

H HIGH, applying to a HIGH voltage level.

L LOW, applying to a LOW voltage level.

I Input.

O Output.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

I_{IL} LOW-level input current with a specified LOW-level voltage applied.

I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.

I_{OL} LOW-level output current.

I_{OH} HIGH-level output current.

I_{SC} Output short-circuit source current.

I_{CC} The supply current drawn by the device from the V_{CC} power supply.

V_{IL} Logic LOW input voltage.

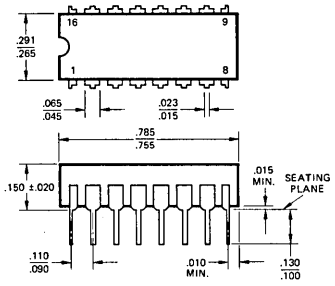
V_{IH} Logic HIGH input voltage.

V_{OL} LOW-level output voltage with I_{OL} applied.

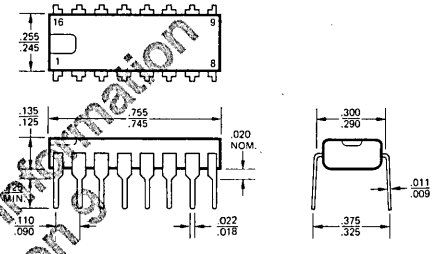
V_{OH} HIGH-level output voltage with I_{OH} applied.

PHYSICAL DIMENSIONS
Dual-In-Line

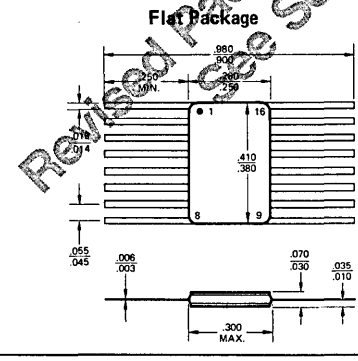
Ceramic



Molded



Flat Package



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Am82S62
Nine-Input Parity Checker/Generator

Distinctive Characteristics

- ODD/EVEN parity outputs
- Inhibit input to disable both outputs
- High-speed expansion input – P_9
- PNP inputs
- Advanced Schottky technology
- 100% reliability assurance testing in compliance with MIL-STD-883.

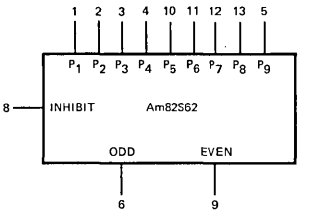
FUNCTIONAL DESCRIPTION

The Am82S62 is a 9-bit parity generator/parity checker with both an ODD parity output and an EVEN parity output. The device can be used to detect errors in data transmission or data retrieval systems as well as to generate this parity check bit.

The Am82S62 features one special high-speed input (P_9) to facilitate expansion. The propagation delay to the outputs through this path is considerably reduced when compared to the P_1 through P_8 paths. This short delay path allows parity checkers/generators of larger size than 9-bits to be built with a minimum of additional delay.

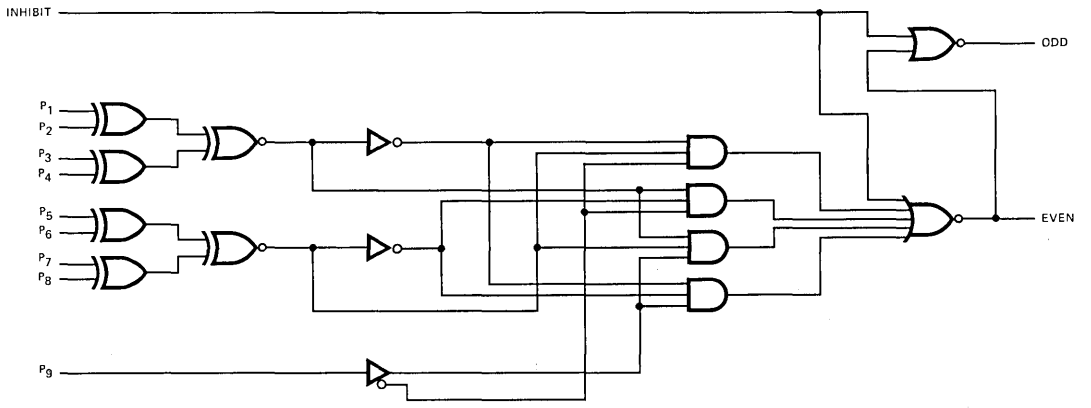
The device is built using advanced Schottky technology and incorporates PNP input transistors to reduce input loading to 0.4 STTL unit loads. The EVEN output is one gate propagation delay time shorter than the ODD output.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

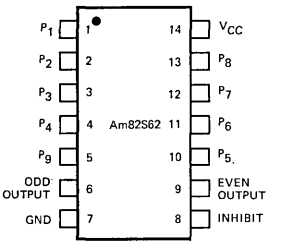
LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	N82S62A
Hermetic DIP	0°C to +75°C	N82S62F
Dice	0°C to +75°C	N82S62X
Hermetic DIP	−55°C to +125°C	S82S62F
Dice	−55°C to +125°C	S82S62X

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 14 to Pin 7) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise noted)

N82S62 T_A = 0°C to +75°C
S82S62 T_A = −55°C to +125°C V_{CC} = 5.0V ±5% MIN. = 4.75V MAX. = 5.25V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1mA V_{IN} = V_{IH} or V_{IL}		2.7			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V	P9			−0.4	mA
			Others			−0.8	
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 4.5V				10	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)				67	mA

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. P_1 through P_9 grounded; inhibit at 4.5V; outputs open.

Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH} t_{PHL}	P_1 through P_8 to Even Output	V_{CC} = 5.0V, R_L = 280Ω, C_L = 15 pF			23	ns
t_{PLH} t_{PHL}	P_1 through P_8 to Odd Output				28	ns
t_{PLH} t_{PHL}	P_9 to Even Output				12	ns
t_{PLH} t_{PHL}	P_9 to Odd Output				18	ns
t_{PLH} t_{PHL}	Inhibit to Even Output				9	ns
t_{PLH} t_{PHL}	Inhibit to Odd Output				9	ns

TRUTH TABLE

INHIBIT	NUMBER OF P INPUTS		OUTPUT	
	LOW	HIGH	ODD	EVEN
L	0	9	H	L
L	1	8	L	H
L	2	7	H	L
L	3	6	L	H
L	4	5	H	L
L	5	4	L	H
L	6	3	H	L
L	7	2	L	H
L	8	1	H	L
L	9	0	L	H
H	X	X	L	L

H = HIGH
L = LOW
X = Don't Care

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
P_1	1	0.4	–	–
P_2	2	0.4	–	–
P_3	3	0.4	–	–
P_4	4	0.4	–	–
P_9	5	0.2	–	–
ODD	6	–	20	10
GND	7	–	–	–
INHIBIT	8	0.4	–	–
EVEN	9	–	20	10
P_5	10	0.4	–	–
P_6	11	0.4	–	–
P_7	12	0.4	–	–
P_8	13	0.4	–	–
V_{CC}	14	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

DEFINITION OF FUNCTIONAL TERMS

P_1 through P_9 The nine inputs to the parity tree.

INHIBIT A HIGH on the inhibit input forces both the odd output and even output LOW regardless of the P inputs. When the inhibit is LOW, the odd and even outputs will always be of opposite phase.

ODD The odd parity output of the device. When an odd number of P inputs are at a HIGH level, the odd output will be HIGH.

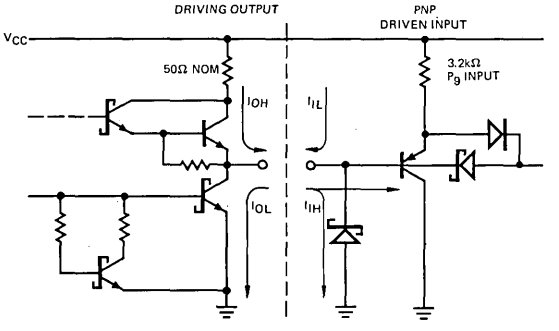
EVEN The even parity output of the device. When an even number of P inputs are at a HIGH level, the even output will be HIGH.

LOGIC EQUATIONS

ODD Output = $P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9$

EVEN Output = $\overline{P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9}$

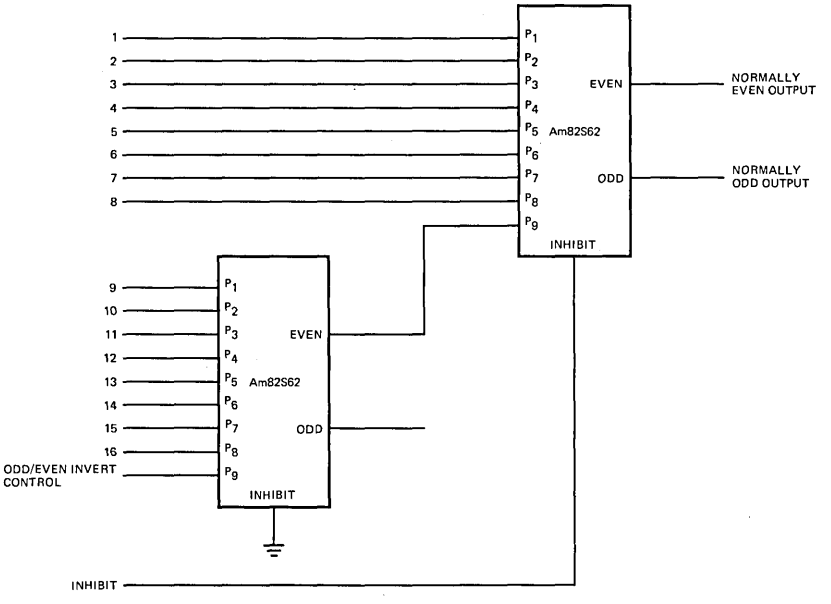
SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



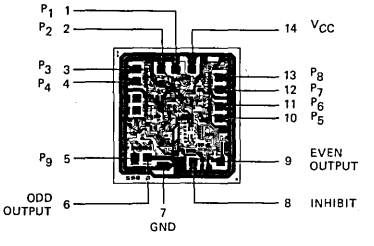
Note: Actual current flow direction shown.

APPLICATION

16-BIT PARITY GENERATOR WITH INVERT CONTROL



Metallization and Pad Layout



DIE SIZE 0.067" X 0.072"

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

f_{MAX} The highest operating clock frequency.

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{PW} Pulse width. The time between the leading and trailing edges of a pulse.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

t_s Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

t_h Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.

t_R Release time. The time interval for which a signal may be indeterminant at one input terminal before an active transition occurs at another input terminal. (The release time falls within the set-up time interval and is specified by some manufacturers as a negative hold time).

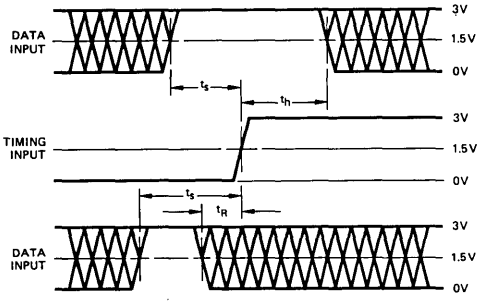
UNIT LOAD DEFINITIONS

	HIGH		LOW	
SERIES	Current	Measure Voltage	Current	Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0 mA	0.5 V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

Note: 1. 54L/74L has two different types of standard inputs.

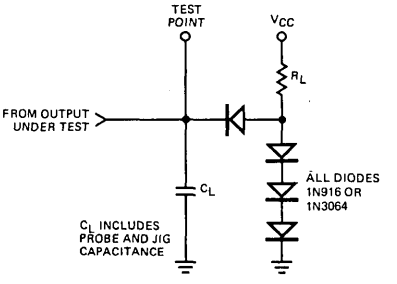
SCHOTTKY PARAMETER MEASUREMENTS
FOR STANDARD ACTIVE-PULLUP TOTEM-POLE OUTPUTS

SET-UP, HOLD, AND RELEASE TIMES

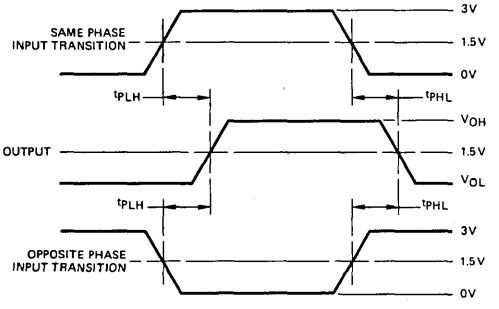


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched area is don't care condition.

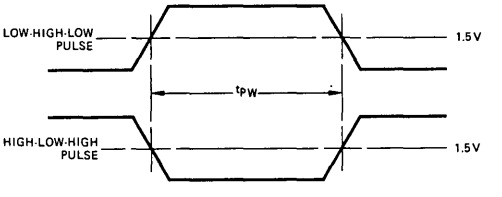
LOAD TEST CIRCUIT



PROPAGATION DELAY

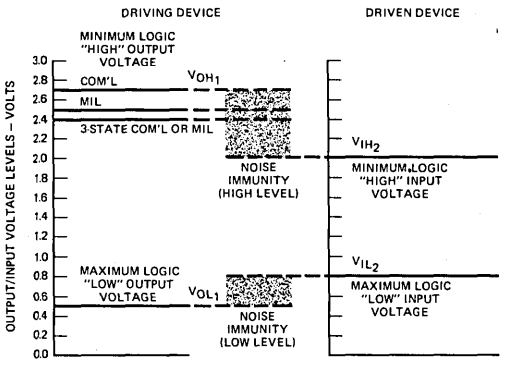


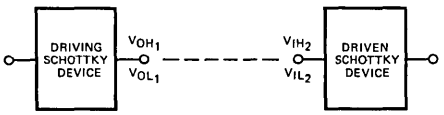
PULSE WIDTH



Notes: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_o = 50Ω; t_r ≤ 2.5ns; t_f ≤ 2.5ns.

SCHOTTKY INPUT/OUTPUT VOLTAGE INTERFACE CONDITIONS





Note: Refer to Electrical Characteristics for measure currents.

DEFINITION OF STANDARD TERMS

H HIGH, applying to a HIGH voltage level.

L LOW, applying to a LOW voltage level.

I Input.

O Output.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

I_{IL} LOW-level input current with a specified LOW-level voltage applied.

I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.

I_{OL} LOW-level output current.

I_{OH} HIGH-level output current.

I_{SC} Output short-circuit source current.

I_{CC} The supply current drawn by the device from the V_{CC} power supply.

V_{IL} Logic LOW input voltage.

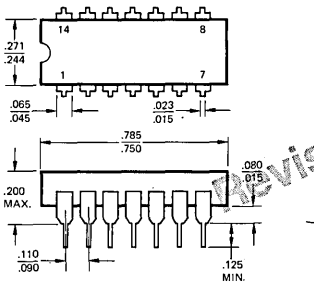
V_{IH} Logic HIGH input voltage.

V_{OL} LOW-level output voltage with I_{OL} applied.

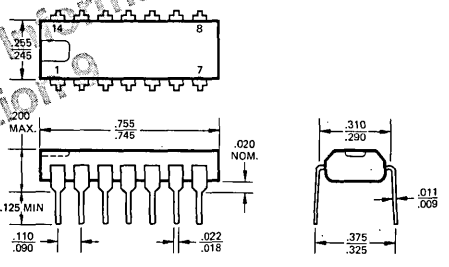
V_{OH} HIGH-level output voltage with I_{OH} applied.

PHYSICAL DIMENSIONS
Dual-In-Line

Ceramic



Molded



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TELEX: 34-6306

Am93S10 • Am93S16
BCD Decade/Four-Bit Binary Counters

Distinctive Characteristics

- Fully synchronous counting
- Fully synchronous parallel loading
- Edge-triggered clock action
- Advanced Schottky technology
- 100% reliability assurance testing in compliance with MIL-STD-883.

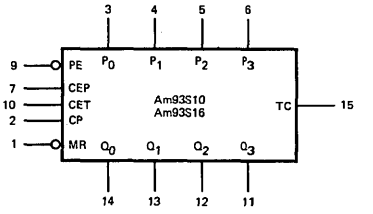
FUNCTIONAL DESCRIPTION

The Am93S10 and Am93S16 are fully synchronous 4-bit decimal and binary counters. With the parallel enable ($\overline{PE}$) LOW, data on the P_0–P_3 inputs is parallel loaded on the positive clock transition. When $\overline{PE}$ is HIGH and both count enables CEP and CET are also HIGH, counting will occur on the LOW-to-HIGH clock transition.

The terminal count state (1001 for the Am93S10 and 1111 for the Am93S16) is decoded and ANDed with CET in the terminal count (TC) output. If CET is HIGH and the counter is in its terminal count state, then TC is HIGH.

Both counters have an asynchronous master reset ($\overline{MR}$). A LOW on the $\overline{MR}$ input forces the Q outputs LOW independent of all other inputs. The only requirements on the $\overline{PE}$, CEP, CET and P_0–P_3 inputs is that they meet the set-up time requirements before the clock LOW-to-HIGH transition.

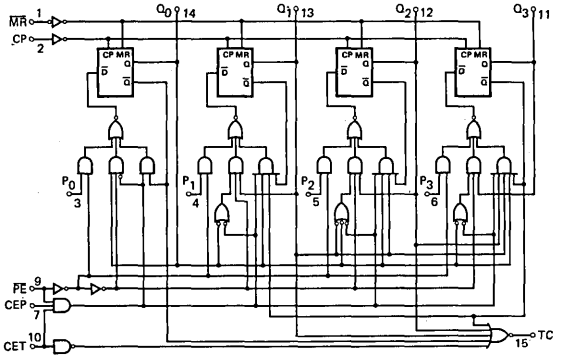
LOGIC SYMBOL



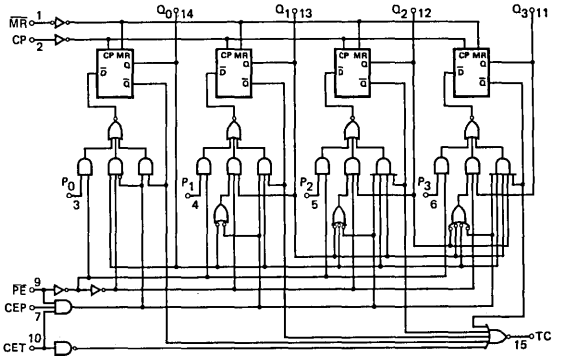
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAMS

Am93S10



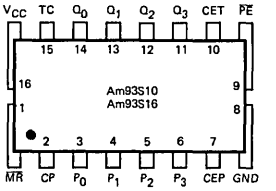
Am93S16



ORDERING INFORMATION

Package Type	Temperature Range	Am93S10 Order Number	Am93S16 Order Number
Molded DIP	0°C to +75°C	93S10PC	93S16PC
Hermetic DIP	0°C to +75°C	93S10DC	93S16DC
Dice	0°C to +75°C	93S10XC	93S16XC
Hermetic DIP	−55°C to +125°C	93S10DM	93S16DM
Hermetic Flat Pak	−55°C to +125°C	93S10FM	93S16FM
Dice	−55°C to +125°C	93S10XM	93S16XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

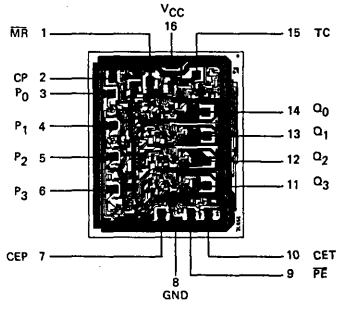
Am93S10XC, Am93S16XC	T_A = 0°C to 75°C	V_{CC} = 5.0V ±5% (COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am93S10XM, Am93S16XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10% (MIL)	MIN. = 4.5V	MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1mA V_{IN} = V_{IH} or V_{IL}	XM	2.5	3.4		Volts
			XC	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}			0.35	0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V	P; MR; CEP			−2.0	mA
			CET			−3.0	
			$\overline{PE}$			−4.0	
			CP			−5.0	
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	P; $\overline{MR}$; CEP			50	µA
			CET			75	
			$\overline{PE}$			100	
			CP			125	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0V		−40	−65	−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)			82	127	mA

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Outputs open; $\overline{MR}$ = 0V; all other inputs HIGH.

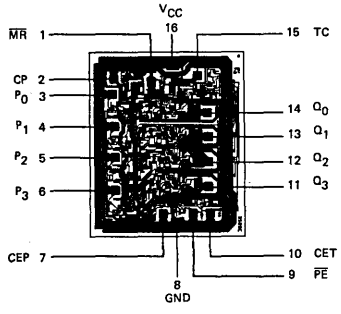
Metallization and Pad Layouts

Am93S10



DIE SIZE 0.078" X 0.096"

Am93S16



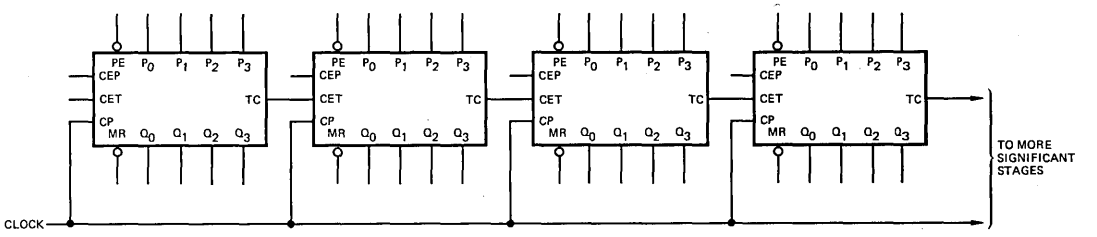
DIE SIZE 0.078" X 0.096"

SWITCHING CHARACTERISTICS ($T_A = +25°$)

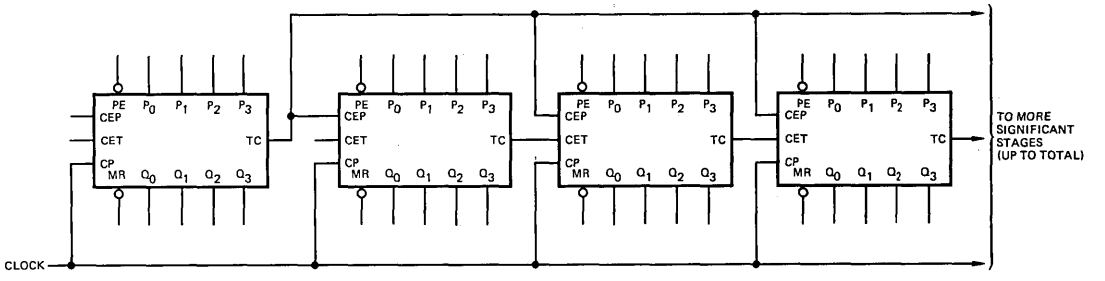
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
f_{MAX}	Count Frequency	$V_{CC} = 5.0V$, $C_L = 15$ pF, $R_L = 280\Omega$	70	100		MHz
t_{PLH}	Clock to Q			6	9	ns
t_{PHL}				8.5	13	
t_{PLH}	Clock to TC			12	18	ns
t_{PHL}				8	12	
t_{PLH}	CET to TC			6.5	10	ns
t_{PHL}				6.5	10	
t_{PHL}	$\overline{MR}$ to Q			14	20	ns
t_s	Recovery Time for MR (inactive)			3.0		ns
t_{pw}	Master Reset Pulse Width			8.5		ns
t_{pw}	Clock Pulse Width HIGH			4.0		ns
	Clock Pulse Width LOW			6.0		
t_s	Data to Clock			6.5		ns
t_R				3.0		
t_s	$\overline{PE}$ to Clock			10.0		ns
t_R				3.5		
t_s	CEP or CET to Clock			6.0		ns
t_R				3.5		

APPLICATIONS

SYNCHRONOUS MULTISTAGE COUNTING USING CET INPUT ONLY



FASTER SYNCHRONOUS MULTISTAGE COUNTING USING CET AND CEP INPUTS



DEFINITION OF FUNCTIONAL TERMS

$\overline{PE}$ Parallel Enable. When $\overline{PE}$ is LOW, the parallel inputs, P_0 through P_3, are enabled. When $\overline{PE}$ is HIGH, the count function is possible.

CEP Count Enable Parallel. CEP is one of the count enable inputs that must be HIGH for the counter to count.

CET Count Enable Trickle. CET is one of the count enable inputs that must be HIGH for the counter to count. In addition, CET is included in the TC output gate and must be HIGH for TC to be HIGH.

CP Clock Pulse. Causes the required output change on the LOW-to-HIGH transition (Edge-triggered).

$\overline{MR}$ Master Reset. When the asynchronous master reset is LOW, the Q_0 through Q_3 outputs will be LOW regardless of the other inputs.

P_0, P_1, P_2, P_3 The parallel data inputs for the four internal flip-flops.

Q_0, Q_1, Q_2, Q_3 The four parallel outputs from the counter.

TC Terminal Count. The terminal count output will be HIGH for CET HIGH and binary nine on the Am93S10 or CET HIGH and binary 15 on the Am93S16.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{MR}$	1	1	–	–
CP	2	2.5	–	–
P_0	3	1	–	–
P_1	4	1	–	–
P_2	5	1	–	–
P_3	6	1	–	–
CEP	7	1	–	–
GND	8	–	–	–
$\overline{PE}$	9	2	–	–
CET	10	1.5	–	–
Q_3	11	–	20	10
Q_2	12	–	20	10
Q_1	13	–	20	10
Q_0	14	–	20	10
TC	15	–	20	10
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and –2.0mA measured at 0.5V LOW.

FUNCTION TABLE

INPUTS									OUTPUTS			
CP	$\overline{MR}$	$\overline{PE}$	CEP	CET	P_0	P_1	P_2	P_3	Q_0	Q_1	Q_2	Q_3
X	L	X	X	X	X	X	X	X	L	L	L	L
↑	H	L	X	X	D_0	D_1	D_2	D_3	D_0	D_1	D_2	D_3
↑	H	H	L	L	X	X	X	X	NC	NC	NC	NC
↑	H	H	L	H	X	X	X	X	NC	NC	NC	NC
↑	H	H	H	L	X	X	X	X	NC	NC	NC	NC
↑	H	H	H	H	X	X	X	X	COUNT			

H = HIGH
L = LOW
X = Don't Care

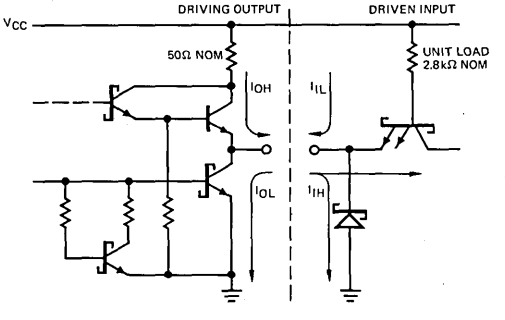
NC = No Change
D_i may be either HIGH or LOW
↑ LOW-to-HIGH Transition

TERMINAL COUNT (TC) TRUTH TABLE

Am93S10					Am93S16					TC
CET	Q_0	Q_1	Q_2	Q_3	CET	Q_0	Q_1	Q_2	Q_3	
H	H	L	L	H	H	H	H	H	H	H
L	X	X	X	X	L	X	X	X	X	L
X	L	X	X	X	X	L	X	X	X	L
X	X	H	X	X	X	X	L	X	X	L
X	X	X	H	X	X	X	X	L	X	L
X	X	X	X	L	X	X	X	X	L	L

H = HIGH
L = LOW
X = Don't Care

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

f_{MAX} *The highest operating clock frequency.*

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{PW} Pulse width. The time between the leading and trailing edges of a pulse.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

t_s Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

t_h Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.

t_R Release time. The time interval for which a signal may be indeterminant at one input terminal before an active transition occurs at another input terminal. (*The release time falls within the set-up time interval and is specified by some manufacturers as a negative hold time).*

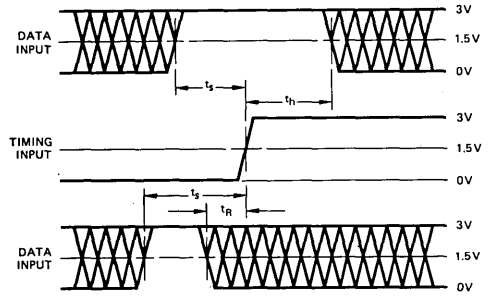
UNIT LOAD DEFINITIONS

	HIGH		LOW	
SERIES	Current	Measure Voltage	Current	Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0 mA	0.5 V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

Note: 1. 54L/74L has two different types of standard inputs.

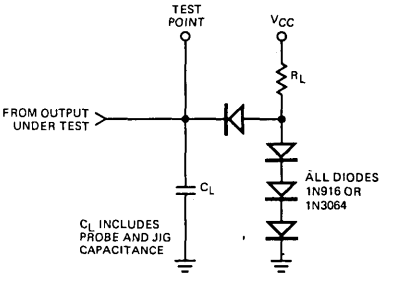
SCHOTTKY PARAMETER MEASUREMENTS
FOR STANDARD ACTIVE-PULLUP TOTEM-POLE OUTPUTS

SET-UP, HOLD, AND RELEASE TIMES

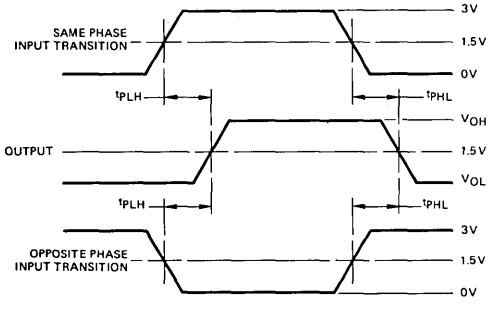


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched area is don't care condition.

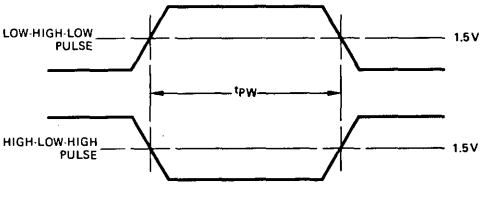
LOAD TEST CIRCUIT



PROPAGATION DELAY

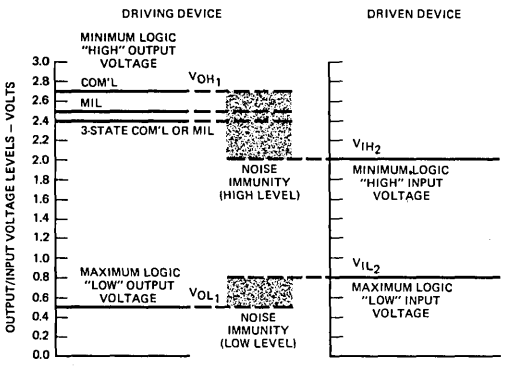


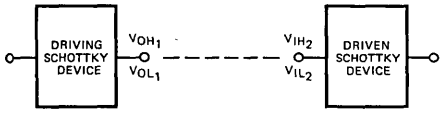
PULSEWIDTH



Notes: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_o = 50\Omega$; $t_r \leq 2.5$ns; $t_f \leq 2.5$ns.

SCHOTTKY INPUT/OUTPUT VOLTAGE INTERFACE CONDITIONS





Note: Refer to Electrical Characteristics for measure currents.

DEFINITION OF STANDARD TERMS

H HIGH, applying to a HIGH voltage level.

L LOW, applying to a LOW voltage level.

I Input.

O Output.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

I_{IL} LOW-level input current with a specified LOW-level voltage applied.

I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.

I_{OL} LOW-level output current.

I_{OH} HIGH-level output current.

I_{SC} Output short-circuit source current.

I_{CC} The supply current drawn by the device from the V_{CC} power supply.

V_{IL} Logic LOW input voltage.

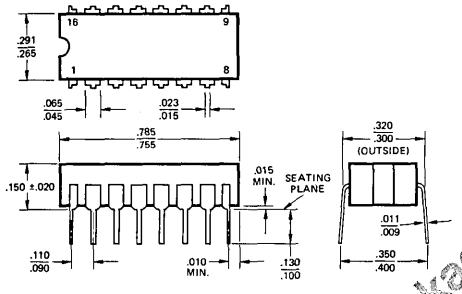
V_{IH} Logic HIGH input voltage.

V_{OL} LOW-level output voltage with I_{OL} applied.

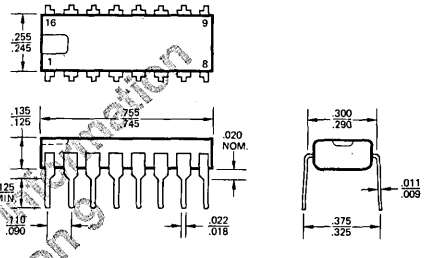
V_{OH} HIGH-level output voltage with I_{OH} applied.

PHYSICAL DIMENSIONS
Dual-In-Line

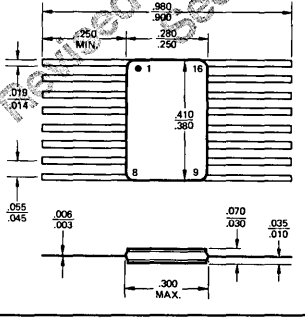
Ceramic



Molded



Flat Package



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(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am93S48

Twelve-Input Parity Checker/Generator

Distinctive Characteristics

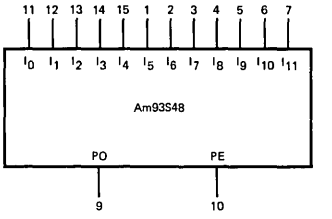
- Generates or checks parity over 12 bits
- Advanced Schottky technology
- Same delay to EVEN and ODD parity outputs
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

The Am93S48 is a high-speed, 12-input parity checker or parity generator. The device is built using advanced Schottky technology and also incorporates PNP input transistors to reduce the input loading to only 0.4 STTL Unit Loads.

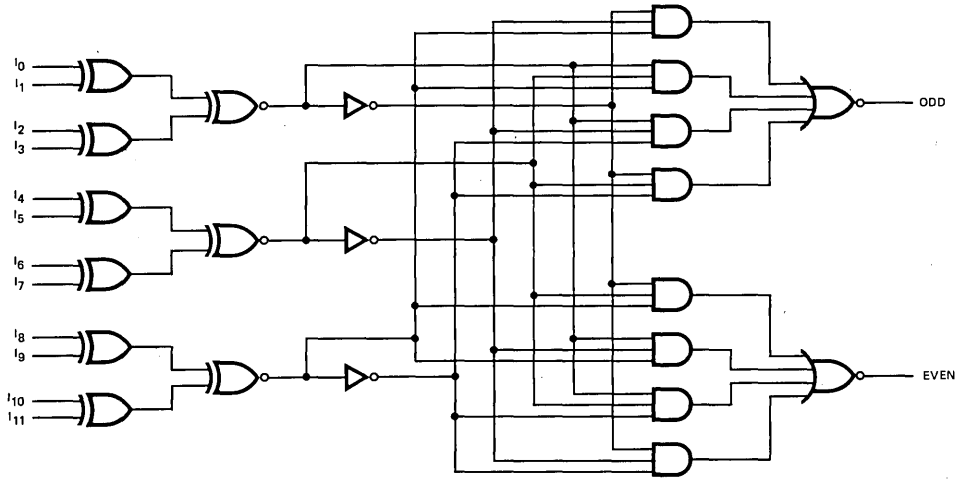
Both an ODD parity output and an EVEN parity output are obtained with the same propagation delay. This is accomplished by using an output structure that looks at the input as three 4-bit parity trees.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

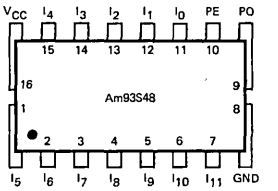
LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	93S48PC
Hermetic DIP	0°C to +70°C	93S48DC
Dice	0°C to +70°C	93S48XC
Hermetic DIP	−55°C to +125°C	93S48DM
Hermetic Flat Pak	−55°C to +125°C	93S48FM
Dice	−55°C to +125°C	93S48XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93S48XC	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5% (COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am93S48XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10% (MIL)	MIN. = 4.5V	MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1mA V_{IN} = V_{IH} or V_{IL}	XC	2.7			Volts
			XM	2.5			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V				−0.8	mA
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)			57	80	mA

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Both outputs open; all inputs at 4.5V.

Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	I_0 through I_{11} to Even Output	V_{CC} = 5.0V, C_L = 15 pF, R_L = 280Ω		19	28	ns
t_{PHL}				19	28	ns
t_{PLH}	I_0 through I_{11} to Odd Output			19	28	ns
t_{PHL}				19	28	ns

TRUTH TABLE

NUMBER OF I INPUTS		OUTPUT	
LOW	HIGH	ODD	EVEN
0	12	L	H
1	11	H	L
2	10	L	H
3	9	H	L
4	8	L	H
5	7	H	L
6	6	L	H
7	5	H	L
8	4	L	H
9	3	H	L
10	2	L	H
11	1	H	L
12	0	L	H

H = HIGH
L = LOW
X = Don't Care

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
I_5	1	0.4	–	–
I_6	2	0.4	–	–
I_7	3	0.4	–	–
I_8	4	0.4	–	–
I_9	5	0.4	–	–
I_{10}	6	0.4	–	–
I_{11}	7	0.4	–	–
GND	8	–	–	–
PO	9	–	20	10
PE	10	–	20	10
I_0	11	0.4	–	–
I_1	12	0.4	–	–
I_2	13	0.4	–	–
I_3	14	0.4	–	–
I_4	15	0.4	–	–
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and –2.0mA measured at 0.5V LOW.

DEFINITION OF FUNCTIONAL TERMS

I_0 through I_{11} The twelve inputs to the parity tree.

ODD The ODD parity output of the device. When an ODD number of I inputs are at a HIGH level, the ODD output will be HIGH.

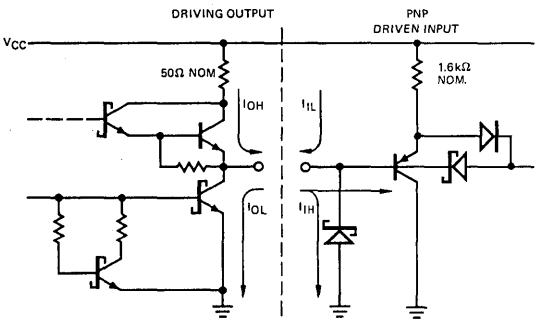
EVEN The EVEN parity output of the device. When an EVEN number of I inputs are at a HIGH level, the EVEN output will be HIGH.

LOGIC EQUATIONS

Odd Output = $I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8 \oplus I_9 \oplus I_{10} \oplus I_{11}$

Even Output = $\overline{I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8 \oplus I_9 \oplus I_{10} \oplus I_{11}}$

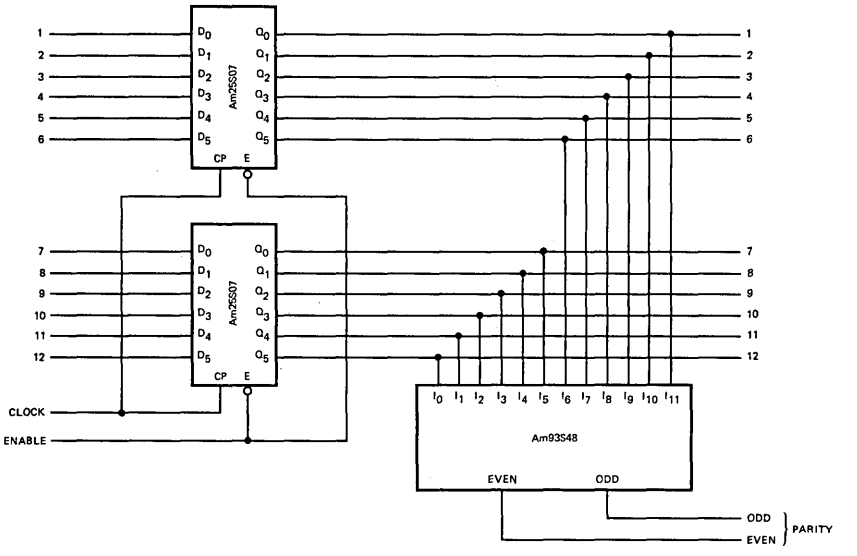
SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



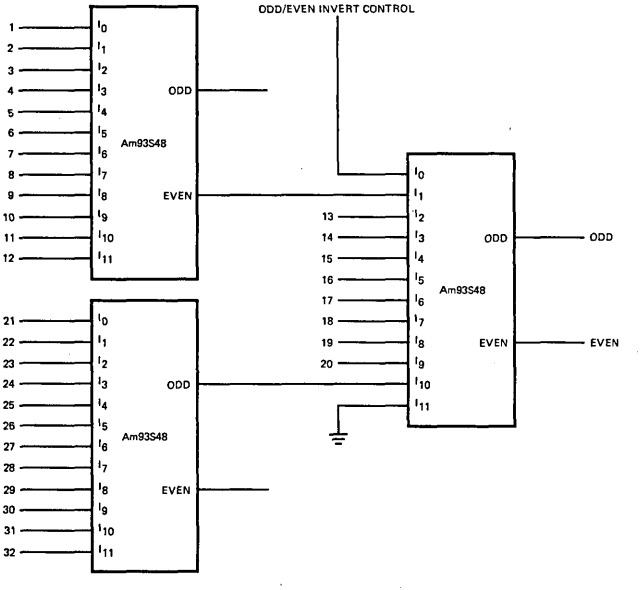
Note: Actual current flow direction shown.

APPLICATIONS

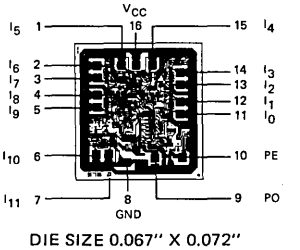
12-BIT PARALLEL ODD/EVEN PARITY CHECKER/GENERATOR



32-BIT PARITY CHECKER/GENERATOR



Metallization and Pad Layout



DIE SIZE 0.067" X 0.072"

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

f_{MAX} The highest operating clock frequency.

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{PW} Pulse width. The time between the leading and trailing edges of a pulse.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

t_s Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

t_h Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.

t_R Release time. The time interval for which a signal may be indeterminant at one input terminal before an active transition occurs at another input terminal. (The release time falls within the set-up time interval and is specified by some manufacturers as a negative hold time).

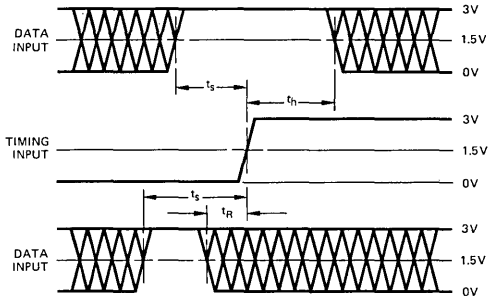
UNIT LOAD DEFINITIONS

SERIES	HIGH Current	HIGH Measure Voltage	LOW Current	LOW Measure Voltage
Am25/26/2700	40μA	2.4 V	−1.6mA	0.4 V
Am25S/26S/27S	50μA	2.7 V	−2.0mA	0.5 V
Am25L/26L/27L	20μA	2.4 V	−0.4mA	0.3 V
Am25LS/26LS/27LS	20μA	2.7 V	−0.36mA	0.4 V
Am54/74	40μA	2.4 V	−1.6mA	0.4 V
54H/74H	50μA	2.4 V	−2.0mA	0.4 V
Am54S/74S	50μA	2.7 V	−2.0mA	0.5 V
54L/74L (Note 1)	20μA	2.4 V	−0.8mA	0.4 V
54L/74L (Note 1)	10μA	2.4 V	−0.18mA	0.3 V
Am54LS/74LS	20μA	2.7 V	−0.36mA	0.4 V
Am9300	40μA	2.4 V	−1.6mA	0.4 V
Am93L00	20μA	2.4 V	−0.4mA	0.3 V
Am93S00	50μA	2.7 V	−2.0mA	0.5 V
Am75/85	40μA	2.4 V	−1.6mA	0.4 V
Am8200	40μA	4.5 V	−1.6mA	0.4 V

Note: 1. 54L/74L has two different types of standard inputs.

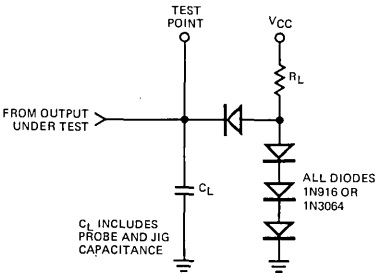
SCHOTKY PARAMETER MEASUREMENTS
FOR STANDARD ACTIVE-PULLUP TOTEM-POLE OUTPUTS

SET-UP, HOLD, AND RELEASE TIMES

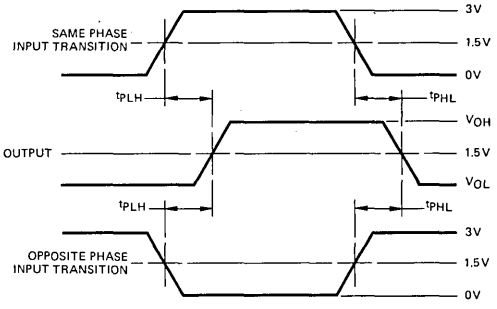


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched area is don't care condition.

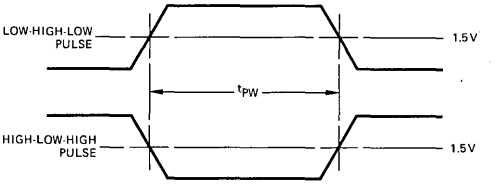
LOAD TEST CIRCUIT



PROPAGATION DELAY

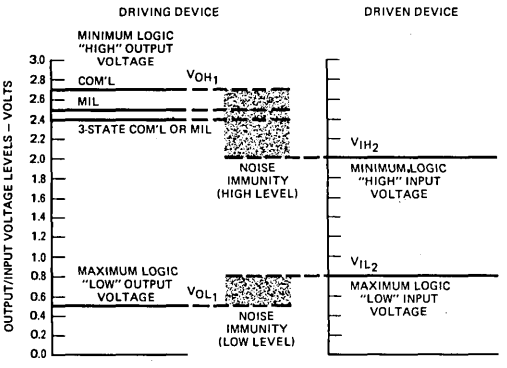


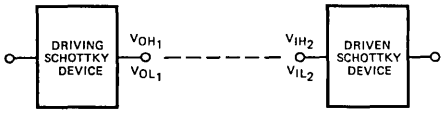
PULSE WIDTH



Notes: 1. Pulse Generator for All Pulses: Rate ≤1.0MHz; Z_o = 50Ω; t_r ≤2.5ns; t_f ≤2.5ns.

SCHOTTKY INPUT/OUTPUT VOLTAGE INTERFACE CONDITIONS





Note: Refer to Electrical Characteristics for measure currents.

DEFINITION OF STANDARD TERMS

H HIGH, applying to a HIGH voltage level.

L LOW, applying to a LOW voltage level.

I Input.

O Output.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

I_{IL} LOW-level input current with a specified LOW-level voltage applied.

I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.

I_{OL} LOW-level output current.

I_{OH} HIGH-level output current.

I_{SC} Output short-circuit source current.

I_{CC} The supply current drawn by the device from the V_{CC} power supply.

V_{IL} Logic LOW input voltage.

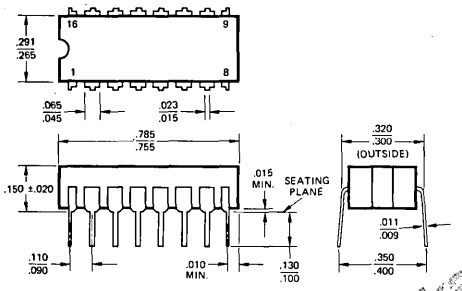
V_{IH} Logic HIGH input voltage.

V_{OL} LOW-level output voltage with I_{OL} applied.

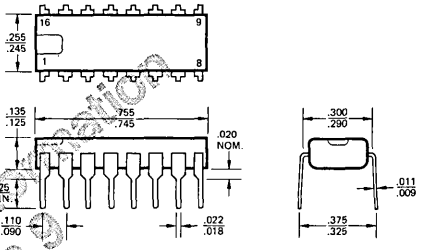
V_{OH} HIGH-level output voltage with I_{OH} applied.

PHYSICAL DIMENSIONS
Dual-In-Line

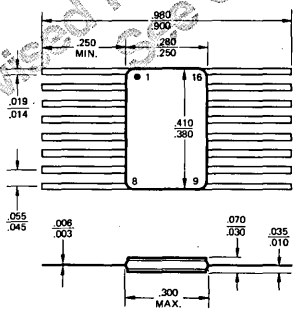
Ceramic



Molded



Flat Package



ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am54S/74S139 • Am93S21

Dual 2-Line to 4-Line Decoder/Demultiplexer

Distinctive Characteristics

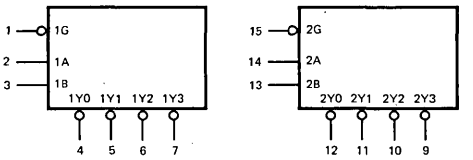
- Advanced Schottky technology
- 7.5ns typical propagation delay
- Two independent decoders/demultiplexers
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

The Am54S/74S139 and Am93S21 are dual 2-line to 4-line decoder/demultiplexer units fabricated using advanced Schottky technology. Each decoder has two buffered select inputs A and B which are decoded to one of four Y outputs.

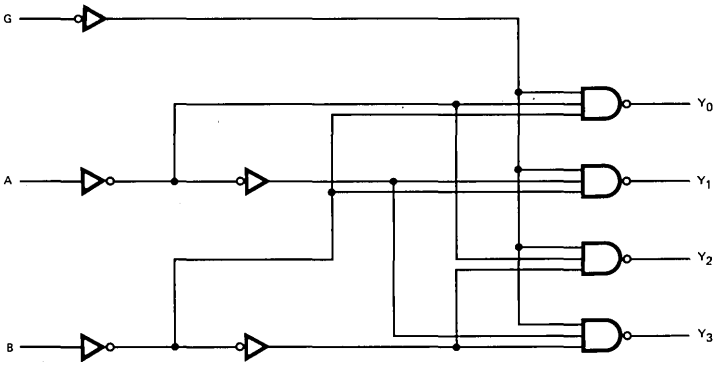
An active LOW enable can be used for gating or can be used as a data input for demultiplexing applications. When the enable is HIGH, all four Y outputs are HIGH, regardless of the A and B inputs.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

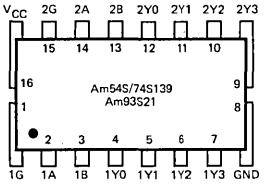
LOGIC DIAGRAM
(One Decoder Shown)



ORDERING INFORMATION

Package Type	Temperature Range	Am54S/74S139 Order Number	Am93S21 Order Number
Molded DIP	0°C to +70°C	SN74S139N	93S21PC
Hermetic DIP	0°C to +70°C	SN74S139J	93S21DC
Dice	0°C to +70°C	SN74S139X	93S21XC
Hermetic DIP	−55°C to +125°C	SN54S139J	93S21DM
Hermetic Flat Pak	−55°C to +125°C	SN54S139W	93S21FM
Dice	−55°C to +125°C	SN54S139X	93S21XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−5.0V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am74S139, Am93S21XC	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5% (COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am54S139, Am93S21XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10% (MIL)	MIN. = 4.5V	MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1mA V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = − 18mA				−1.2	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5 V				−2	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7 V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0 V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)			60	90	mA

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current X Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} is measured with all outputs enabled and open.

Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Select to Output, 2 Levels of Delay	V_{CC} = 5.0V, R_L = 280Ω, C_L = 15 pF		5	7.5	ns
t_{PHL}				6.5	10	
t_{PLH}	Select to Output, 3 Levels of Delay			7	12	ns
t_{PHL}				8	12	
t_{PLH}	Enable to Output, 2 Levels of Delay			5	8	ns
t_{PHL}				6.5	10	

FUNCTION TABLE

INPUTS			OUTPUTS			
ENABLE G	SELECT B	A	Y_0	Y_1	Y_2	Y_3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = HIGH
L = LOW
X = Don't Care

DEFINITION OF FUNCTIONAL TERMS

A, B Select. The two select inputs to the decoder.

G Enable. The enable input to the decoder. A HIGH input forces all four Y outputs HIGH regardless of the A and B inputs.

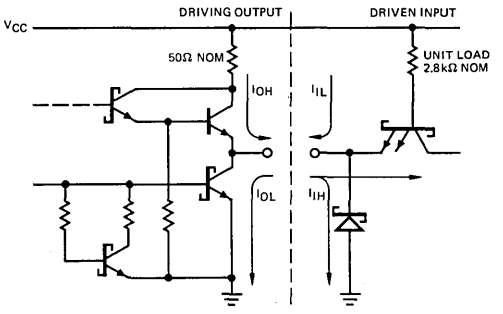
Y_0, Y_1, Y_2, Y_3 The four decoder outputs.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Unit Load	Fan-out Output HIGH	Fan-out Output LOW
1G	1	1	–	–
1A	2	1	–	–
1B	3	1	–	–
1Y0	4	–	20	10
1Y1	5	–	20	10
1Y2	6	–	20	10
1Y3	7	–	20	10
GND	8	–	–	–
2Y3	9	–	20	10
2Y2	10	–	20	10
2Y1	11	–	20	10
2Y0	12	–	20	10
2B	13	1	–	–
2A	14	1	–	–
2G	15	1	–	–
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

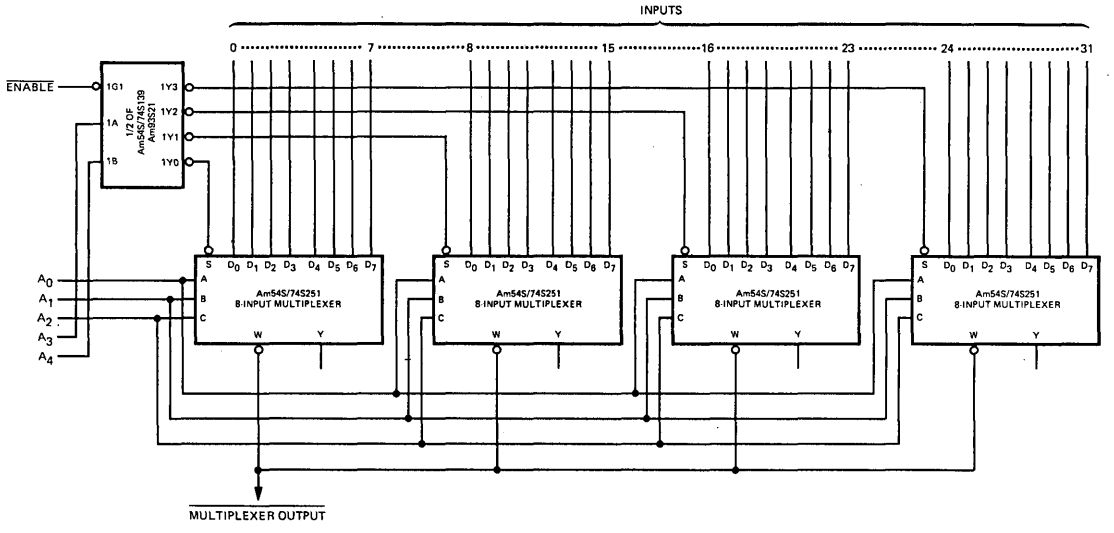
SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

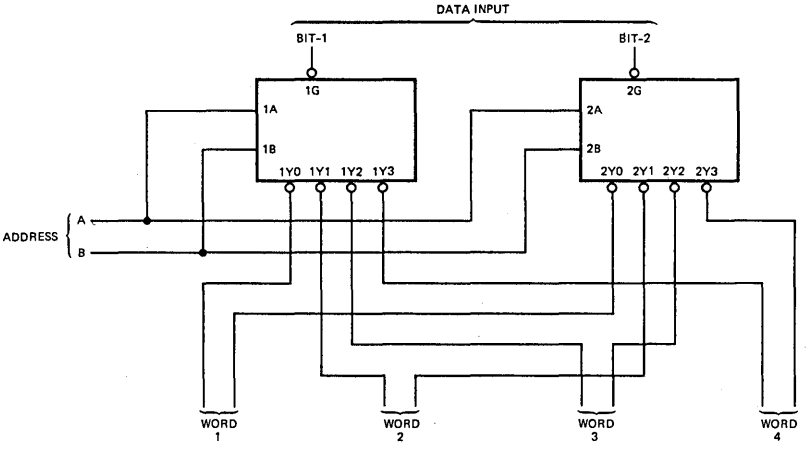


Note: Actual current flow direction shown.

APPLICATIONS

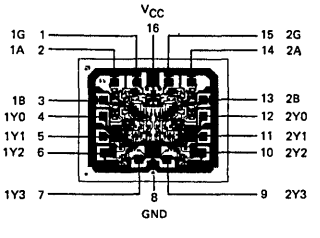
32-Input Multiplexer





Data routing using one Am54S/74S139 as a demultiplexer for two bits.

Metallization and Pad Layout



DIE SIZE 0.073" X 0.060"

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

f_{MAX} The highest operating clock frequency.

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{PW} Pulse width. The time between the leading and trailing edges of a pulse.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

t_s Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

t_h Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.

t_R Release time. The time interval for which a signal may be indeterminant at one input terminal before an active transition occurs at another input terminal. (The release time falls within the set-up time interval and is specified by some manufacturers as a negative hold time).

UNIT LOAD DEFINITIONS

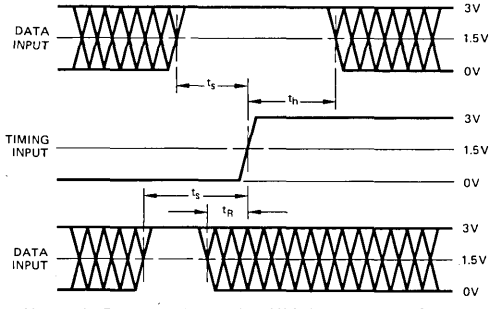
SERIES	HIGH Current	HIGH Measure Voltage	LOW Current	LOW Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0mA	0.5V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

Note: 1. 54L/74L has two different types of standard inputs.

SCHOTTKY PARAMETER MEASUREMENTS

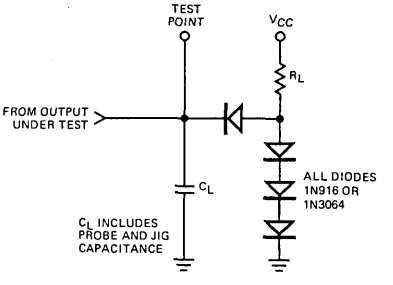
FOR STANDARD ACTIVE-PULLUP TOTEM-POLE OUTPUTS

SET-UP, HOLD, AND RELEASE TIMES

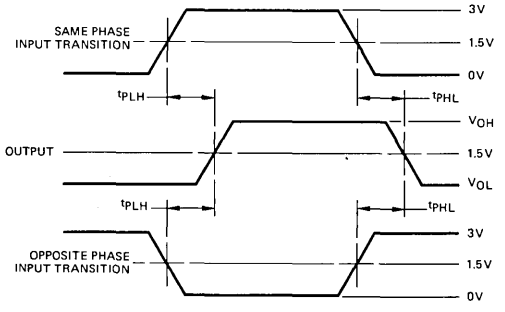


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched area is don't care condition.

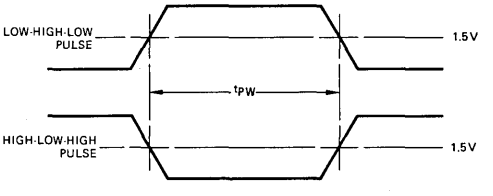
LOAD TEST CIRCUIT



PROPAGATION DELAY

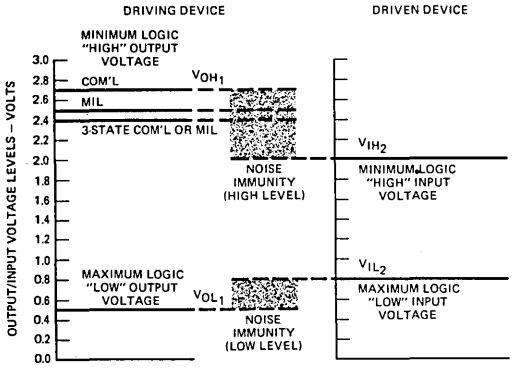


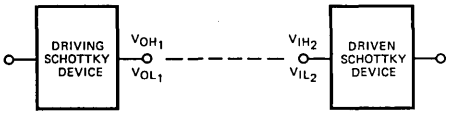
PULSE WIDTH



Note: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_o = 50\Omega$, $t_r \leq 2.5$ns; $t_f \leq 2.5$ns.

SCHOTTKY INPUT/OUTPUT VOLTAGE INTERFACE CONDITIONS





Note: Refer to Electrical Characteristics for measure currents.

DEFINITION OF STANDARD TERMS

H HIGH, applying to a HIGH voltage level.

L LOW, applying to a LOW voltage level.

I Input.

O Output.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

I_{IL} LOW-level input current with a specified LOW-level voltage applied.

I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.

I_{OL} LOW-level output current.

I_{OH} HIGH-level output current.

I_{SC} Output short-circuit source current.

I_{CC} The supply current drawn by the device from the V_{CC} power supply.

V_{IL} Logic LOW input voltage.

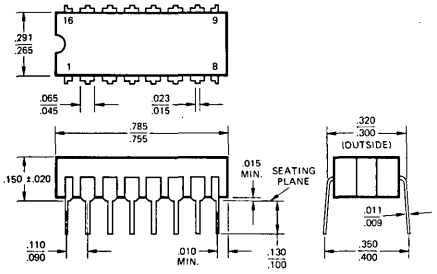
V_{IH} Logic HIGH input voltage.

V_{OL} LOW-level output voltage with I_{OL} applied.

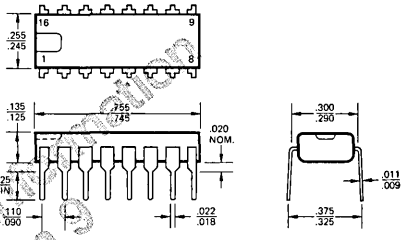
V_{OH} HIGH-level output voltage with I_{OH} applied.

PHYSICAL DIMENSIONS
Dual-In-Line

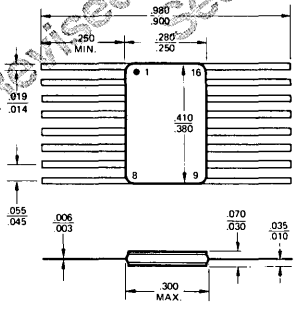
Ceramic



Molded



Flat Package



ADVANCED MICRO DEVICES INC.
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TELEX: 34-6306

Am54S/74S151•Am54S/74S251

Eight-Input Multiplexers

Distinctive Characteristics

- Advanced Schottky technology
- Switches one of eight inputs to two complementary outputs
- Three-state output on Am54S/74S251 for bus organized systems
- 100% reliability assurance testing in compliance with MIL-STD-883

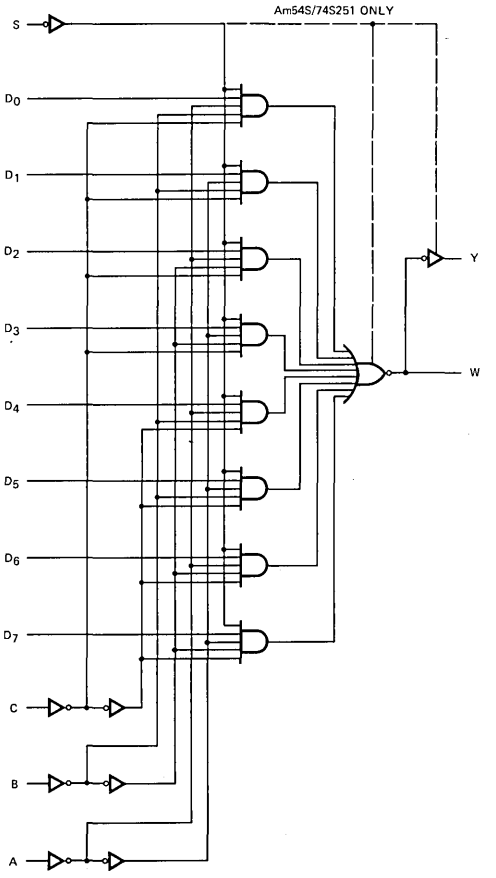
FUNCTIONAL DESCRIPTION

The Am54S/74S151 and the Am54S/74S251 are eight-input multiplexers that switch one of eight inputs onto the inverting and non-inverting outputs under the control of a three-bit select code. The inverting output is one gate delay faster than the non-inverting output.

The Am54S/74S151 provides an active-LOW strobe. When the strobe is HIGH, the inverting output (W) is HIGH and the non-inverting output (Y) is LOW.

The Am54S/74S251 features a three-state output for data bus organization. The active-LOW strobe, or "output control" applies to both the inverting and non-inverting output. When the output control is HIGH, the outputs are in the high-impedance state. When the output control is LOW, the active pull-up output is enabled.

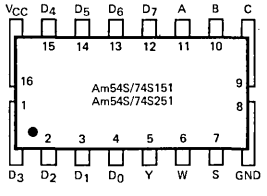
LOGIC DIAGRAM



ORDERING INFORMATION

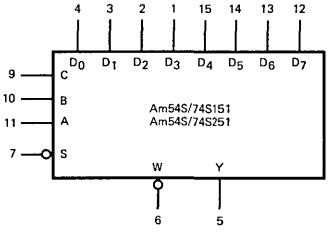
Package Type	Temperature Range	Am54S/74S151 Order Number	Am54S/74S251 Order Number
Molded DIP	0°C to +70°C	SN74S151N	SN74S251N
Hermetic DIP	0°C to +70°C	SN74S151J	SN74S251J
Dice	0°C to +70°C	SN74S151X	SN74S251X
Hermetic DIP	−55°C to +125°C	SN54S151J	SN54S251J
Hermetic Flat Pak	−55°C to +125°C	SN54S151W	SN54S251W
Dice	−55°C to +125°C	SN54S151X	SN54S251X

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

MAXIMUM RATINGS (Above which the useful life may be impaired).

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to + V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Output	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am74S151, Am74S251 T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V

Am54S151, Am54S251 T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL) MIN. = 4.5V MAX. = 5.5V

Parameters	Description		Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	54S151	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1mA	2.5	3.4		Volts
		74S151			2.7	3.4		
		54S251		I_{OH} = −2mA	2.4	3.4		
		74S251		I_{OH} = −6.5mA	2.4	3.2		
V_{OL}	Output LOW Voltage		V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level		Guaranteed input logical HIGH voltage for all inputs		2			Volts
V_{IL}	Input LOW Level		Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage		V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current		V_{CC} = MAX., V_{IN} = 0.5				−2	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current		V_{CC} = MAX., V_{IN} = 2.7V				50	µA
I_I	Input HIGH Current		V_{CC} = MAX., V_{IN} = 5.5V				1	mA
$I_{O(off)}$	Off-State (High-Impedance) Output Current (S251 only)		V_{CC} = MAX. V_{IN} = V_{IH} or V_{IL}	V_O = 2.4V			50	µA
				V_O = 0.5V			−50	
I_{SC}	Output Short Circuit Current (Note 4)		V_{CC} = MAX., V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current		V_{CC} = MAX. (Note 5)	S151		45	70	mA
				S251		55	85	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} is measured with all outputs open and all inputs at 4.5V.

Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	A, B, or C to Y; 4 Levels of Delay (S151 only)	V_{CC} = 5.0V, R_L = 280Ω, C_L = 15 pF		12	18	ns
t_{PHL}				12	18	
t_{PLH}	A, B, or C to Y; 4 Levels of Delay (S251 only)			12	18	ns
t_{PHL}				13	19.5	
t_{PLH}	A, B, or C to W; 3 Levels of Delay			10	15	ns
t_{PHL}				9	13.5	
t_{PLH}	Any D to Y			8	12	ns
t_{PHL}				8	12	
t_{PLH}	Any D to W			4.5	7	ns
t_{PHL}				4.5	7	
t_{PLH}	Strobe to Y (S151 only)			11	16.5	ns
t_{PHL}				12	18	
t_{PLH}	Strobe to W (S151 only)			9	13	ns
t_{PHL}				8.5	12	
t_{ZH}	Output Enable to Y (S251 only)	V_{CC} = 5.0V, R_L = 280Ω, C_L = 50 pF		13	19.5	ns
t_{ZL}				14	21	
t_{ZH}	Output Enable to W (S251 only)			13	19.5	ns
t_{ZL}				14	21	
t_{HZ}	Output Enable to Y (S251 only)	V_{CC} = 5.0V, R_L = 280Ω, C_L = 5 pF		5.5	8.5	ns
t_{LZ}				9	14	
t_{HZ}	Output Enable to W (S251 only)			5.5	8.5	ns
t_{LZ}				9	14	

FUNCTION TABLE

INPUTS					OUTPUTS			
SELECT			S151 Strobe	S251 Output Control	S151 Output		S251 Output	
C	B	A	S	S	Y	W	Y	W
X	X	X	H	H	L	H	Z	Z
L	L	L	L	L	D_0	$\overline{D}_0$	D_0	$\overline{D}_0$
L	L	H	L	L	D_1	$\overline{D}_1$	D_1	$\overline{D}_1$
L	H	L	L	L	D_2	$\overline{D}_2$	D_2	$\overline{D}_2$
L	H	H	L	L	D_3	$\overline{D}_3$	D_3	$\overline{D}_3$
H	L	L	L	L	D_4	$\overline{D}_4$	D_4	$\overline{D}_4$
H	L	H	L	L	D_5	$\overline{D}_5$	D_5	$\overline{D}_5$
H	H	L	L	L	D_6	$\overline{D}_6$	D_6	$\overline{D}_6$
H	H	H	L	L	D_7	$\overline{D}_7$	D_7	$\overline{D}_7$

H = HIGH X = Don't Care
L = LOW Z = High Impedance

D_0–D_7 = The output will follow the HIGH-level or LOW-level of the selected input.

$\overline{D}_0$–$\overline{D}_7$ = The output will follow the complement of the HIGH-level or LOW-level of the selected input.

DEFINITION OF FUNCTIONAL TERMS

A, B, C The three select inputs of the multiplexer.

D_0, D_1, D_2, D_3, D_4, D_5, D_6, D_7 The eight data inputs of the multiplexer.

Y The true multiplexer output.

W The complement multiplexer output.

S Strobe. On the Am54S/74S151, a HIGH on the strobe forces the Y output LOW and the W output HIGH.

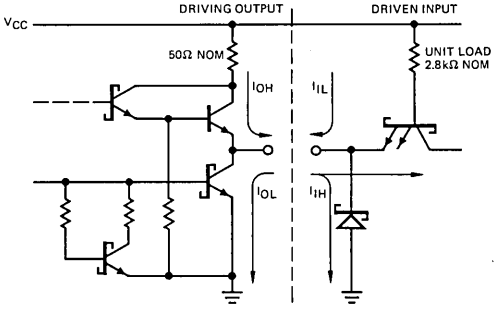
S Output Control. On the Am54S/74S251, a HIGH on the output control (or strobe) forces both the W and Y outputs to the high-impedance (off) state.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
D_3	1	1	–	–
D_2	2	1	–	–
D_1	3	1	–	–
D_0	4	1	–	–
Y	5	–	20	10
W	6	–	20	10
S	7	1	–	–
GND	8	–	–	–
C	9	1	–	–
B	10	1	–	–
A	11	1	–	–
D_7	12	1	–	–
D_6	13	1	–	–
D_5	14	1	–	–
D_4	15	1	–	–
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and –2.0mA measured at 0.5V LOW.

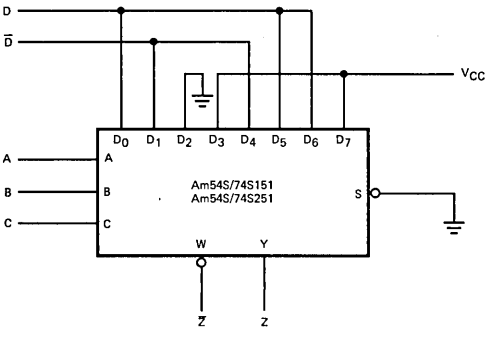
SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

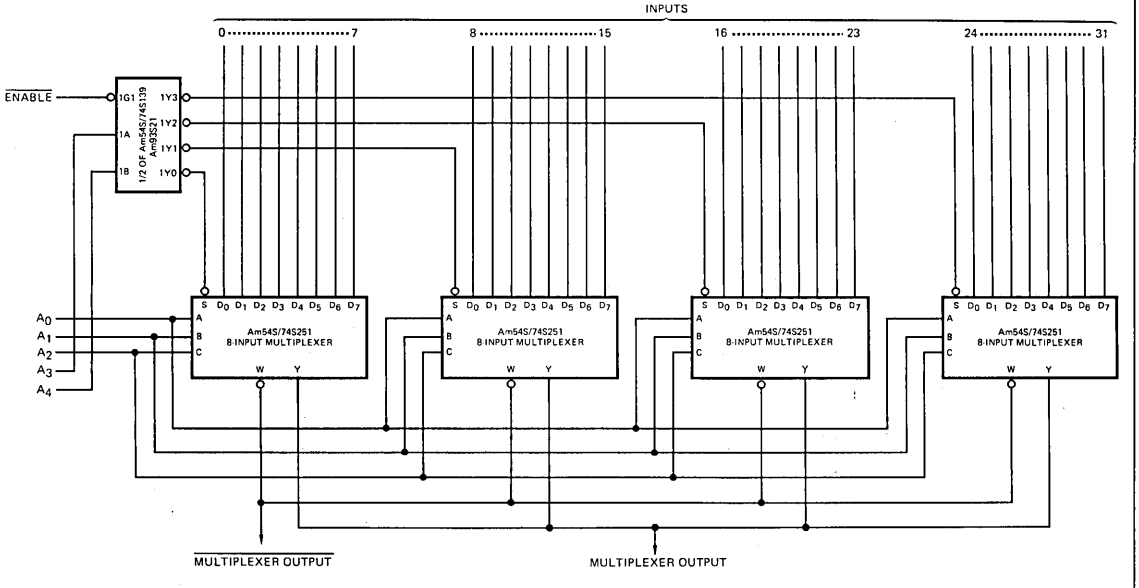
APPLICATIONS

LOGIC FUNCTION GENERATION

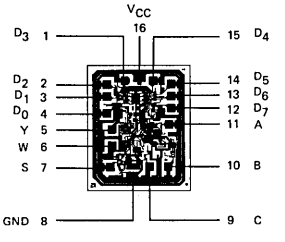


$$Z = \overline{A}\overline{B}CD + \overline{A}B\overline{C}\overline{D} + A\overline{C}D + AB + AC\overline{D} + BC\overline{D}$$

32-INPUT MULTIPLEXER



Metallization and Pad Layout



DIE SIZE: 0.055" X 0.068"

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

f_{MAX} The highest operating clock frequency.

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{PW} Pulse width. The time between the leading and trailing edges of a pulse.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

t_s Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

t_h Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.

t_R Release time. The time interval for which a signal may be indeterminant at one input terminal before an active transition occurs at another input terminal. (The release time falls within the set-up time interval and is specified by some manufacturers as a negative hold time).

t_{HZ} HIGH to disable. The delay time from a control input change to the three-state output HIGH-level to high-impedance transition (measured at 0.5 V change).

t_{LZ} LOW to disable. The delay time from a control input change to the three-state output LOW-level to high-impedance transition (measured at 0.5 V change).

t_{ZH} Enable HIGH. The delay time from a control input change to the three-state output high-impedance to HIGH-level transition.

t_{ZL} Enable LOW. The delay time from a control input change to the three-state output high-impedance to LOW-level transition.

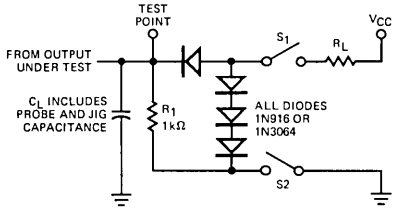
UNIT LOAD DEFINITIONS

SERIES	HIGH Current	HIGH Measure Voltage	LOW Current	LOW Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0 mA	0.5 V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

Note: 1. 54L/74L has two different types of standard inputs.

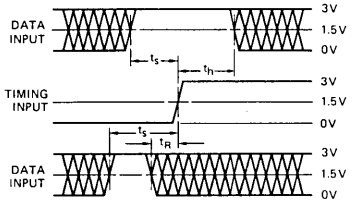
SCHOTTKY PARAMETER MEASUREMENTS
FOR THREE-STATE OUTPUTS

LOAD TEST CIRCUIT



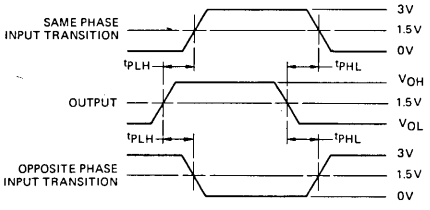
Note: For S151, remove, R_1; S_1 and S_2 closed.

SET-UP, HOLD, AND RELEASE TIMES

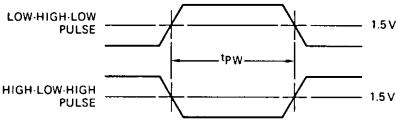


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

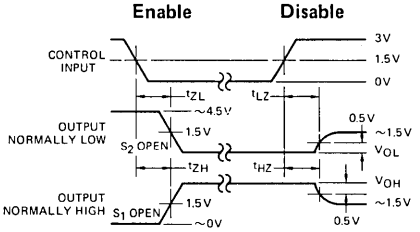
PROPAGATION DELAY



PULSE WIDTH



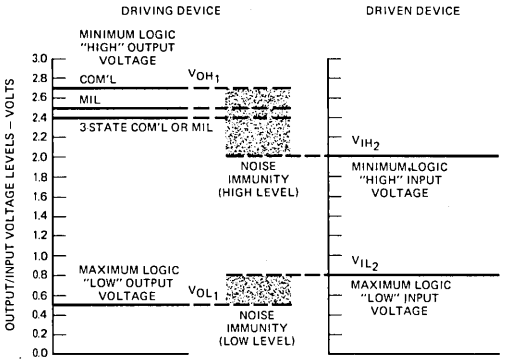
ENABLE AND DISABLE TIMES
S251 Only

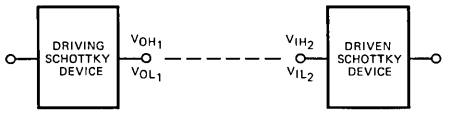


Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1 and S_2 of Load Circuit are closed except where shown.

Note: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_o = 50Ω; t_r ≤ 2.5 ns; t_f ≤ 2.5 ns.

SCHOTTKY INPUT/OUTPUT VOLTAGE INTERFACE CONDITIONS





Note: Refer to Electrical Characteristics for measure current.

DEFINITION OF STANDARD TERMS

H HIGH, applying to a HIGH voltage level.

L LOW, applying to a LOW voltage level.

I Input.

O Output.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

I_{IL} LOW-level input current with a specified LOW-level voltage applied.

I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.

I_{OL} LOW-level output current.

I_{OH} HIGH-level output current.

I_{SC} Output short-circuit source current.

I_{CC} The supply current drawn by the device from the V_{CC} power supply.

V_{IL} Logic LOW input voltage.

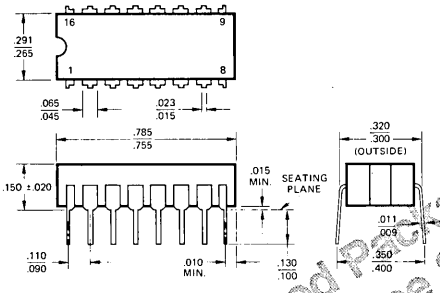
V_{IH} Logic HIGH input voltage.

V_{OL} LOW-level output voltage with I_{OL} applied.

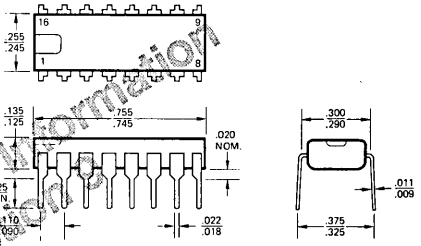
V_{OH} HIGH-level output voltage with I_{OH} applied.

PHYSICAL DIMENSIONS
Dual-In-Line

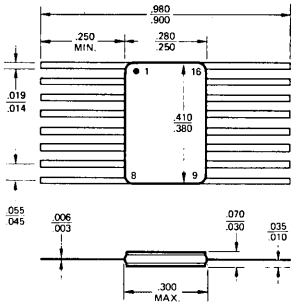
Ceramic



Molded



Flat Package



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Am54S/74S153•Am54S/74S253

Dual 4-Line-To-1-Line Data Selectors/Multiplexers

Distinctive Characteristics

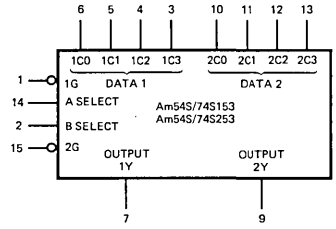
- Permits multiplexing from N lines to 1 line.
- Performs parallel-to-serial conversion.
- Am54S/74S253 provides three-state outputs for data bus organization.
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

These dual four-input multiplexers provide the digital equivalent of a two-pole, four position switch with the position of both switches set by the logic levels supplied to the select inputs A and B. Each section of the Am54S/74S153 has a separate active-LOW enable (storbe) input that forces the output of that section LOW when a HIGH level is applied regardless of the other inputs.

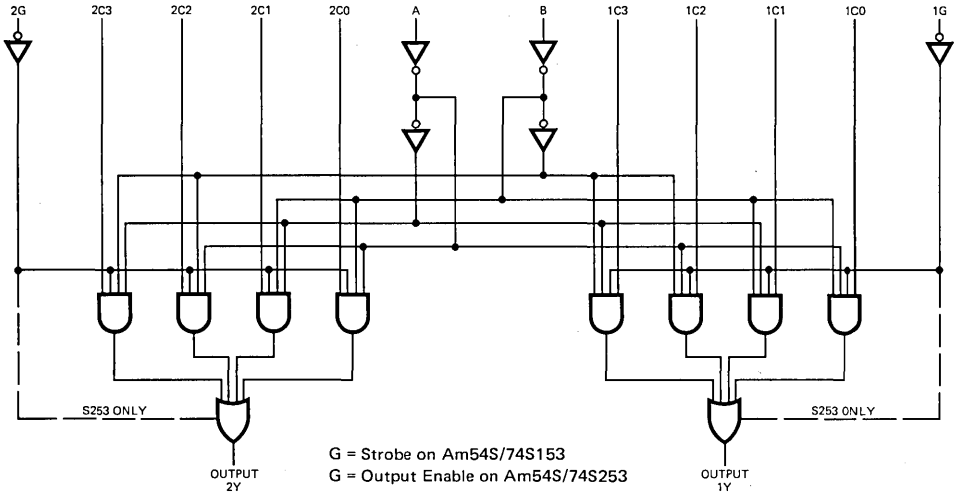
The Am54S/74S253 features a three-state output to interface with bus-organized systems. Each section of the Am54S/74S253 has a separate active-LOW output control that disables the output driver (high-impedance state) of that section when a HIGH logic level is applied regardless of the other inputs.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM

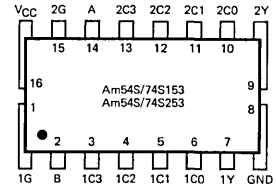


G = Strobe on Am54S/74S153
G = Output Enable on Am54S/74S253

ORDERING INFORMATION

Package Type	Temperature Range	Am54S/74S153 Order Number	Am54S/74S253 Order Number
Molded DIP	0°C to +70°C	SN74S153N	SN74S253N
Hermetic DIP	0°C to +70°C	SN74S153J	SN74S253J
Dice	0°C to +70°C	SN74S153X	SN74S253X
Hermetic DIP	−55°C to +125°C	SN54S153J	SN54S253J
Hermetic Flat Pak	−55°C to +125°C	SN54S153W	SN54S253W
Dice	−55°C to +125°C	SN54S153X	SN54S253X

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am74S153, Am74S253	T_A = 0°C to +70°C	V_{CC} = 5.0 V ±5% (COM'L)	MIN. = 4.75 V	MAX. = 5.25 V
Am54S153, Am54S253	T_A = −55°C to +125°C	V_{CC} = 5.0 V ±10% (MIL)	MIN. = 4.5 V	MAX. = 5.5 V

Parameters	Description		Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	54S153	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1 mA	2.5	3.4		Volts
		74S153			2.7	3.4		
		54S253		I_{OH} = −2 mA	2.4	3.4		
		74S253		I_{OH} = −6.5 mA	2.4	3.2		
V_{OL}	Output LOW Voltage		V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level		Guaranteed input logical HIGH voltage for all inputs		2			Volts
V_{IL}	Input LOW Level		Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage		V_{CC} = MIN., I_{IN} = −18 mA				−1.2	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current		V_{CC} = MAX., V_{IN} = 0.5 V				−2	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current		V_{CC} = MAX., V_{IN} = 2.7 V				50	µA
I_I	Input HIGH Current		V_{CC} = MAX., V_{IN} = 5.5 V				1	mA
I_O	Off-State (HIGH Impedance) Output Current Am54S/74S253 Only		V_{CC} = MAX.	V_O = 2.4 V			50	µA
				V_O = 0.5 V			−50	
I_{SC}	Output Short Circuit Current (Note 4)		V_{CC} = MAX., V_{OUT} = 0.0 V		−40		−100	mA
I_{CC}	Power Supply Current		V_{CC} = MAX. (Note 5)	S153		45	70	mA
				S253		55	70	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics (T_A = +25°C)

Parameters	Description		Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Data to Output		V_{CC} = 5.0 V, R_L = 280Ω, C_L = 15 pF		6	9	ns
t_{PHL}					6	9	
t_{PLH}	Select to Output				11.5	18	ns
t_{PHL}					12	18	
t_{PLH}	Strobe to Output	S153			10	15	ns
t_{PHL}		S153			9	13.5	
t_{ZH}	Output Control to Output	S253	V_{CC} = 5.0 V, R_L = 280Ω, C_L = 50 pF		13	19.5	ns
t_{ZL}		S253			14	21	
t_{HZ}	Output Control to Output	S253	V_{CC} = 5.0 V, R_L = 280Ω, C_L = 5 pF		5.5	8.5	ns
t_{LZ}		S253			9	14	

FUNCTION TABLE

INPUTS								OUTPUTS	
Select		Data				S153 Strobe	S253 Output Control	S153 Output	S253 Output
B	A	C_0	C_1	C_2	C_3	G	G	Y	Y
X	X	X	X	X	X	H	H	L	Z
L	L	L	X	X	X	L	L	L	L
L	L	H	X	X	X	L	L	H	H
L	H	X	L	X	X	L	L	L	L
L	H	X	H	X	X	L	L	H	H
H	L	X	X	L	X	L	L	L	L
H	L	X	X	H	X	L	L	H	H
H	H	X	X	X	L	L	L	L	L
H	H	X	X	X	H	L	L	H	H

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance
Note: A & B are common to both 4 input multiplexers.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
1G	1	1	–	–
B	2	1	–	–
1C3	3	1	–	–
1C2	4	1	–	–
1C1	5	1	–	–
1C0	6	1	–	–
1Y	7	–	20*	10
GND	8	–	–	–
2Y	9	–	20*	10
2C0	10	1	–	–
2C1	11	1	–	–
2C2	12	1	–	–
2C3	13	1	–	–
A	14	1	–	–
2G	15	1	–	–
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined at 50μA measured at 2.7V HIGH and -2.0 mA measured at 0.5V LOW.

* 20 for the Am54S/74S153
40 for the Am54S253
130 for the Am74S253

DEFINITION OF FUNCTIONAL TERMS:

$1C_i$, $2C_i$ Data Inputs. The four data inputs to each multiplexer; i = 0, 1, 2, and 3.

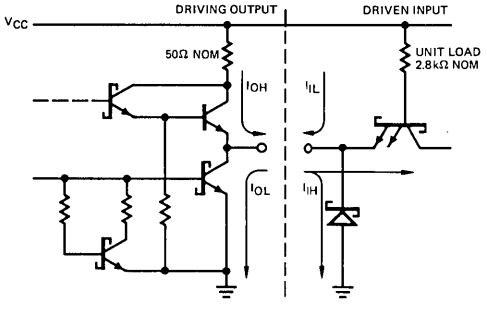
1Y, 2Y Multiplexer Outputs. The output of each four-input multiplexer.

A, B Select Inputs. The inputs used to determine which of the four data inputs are selected for the output.

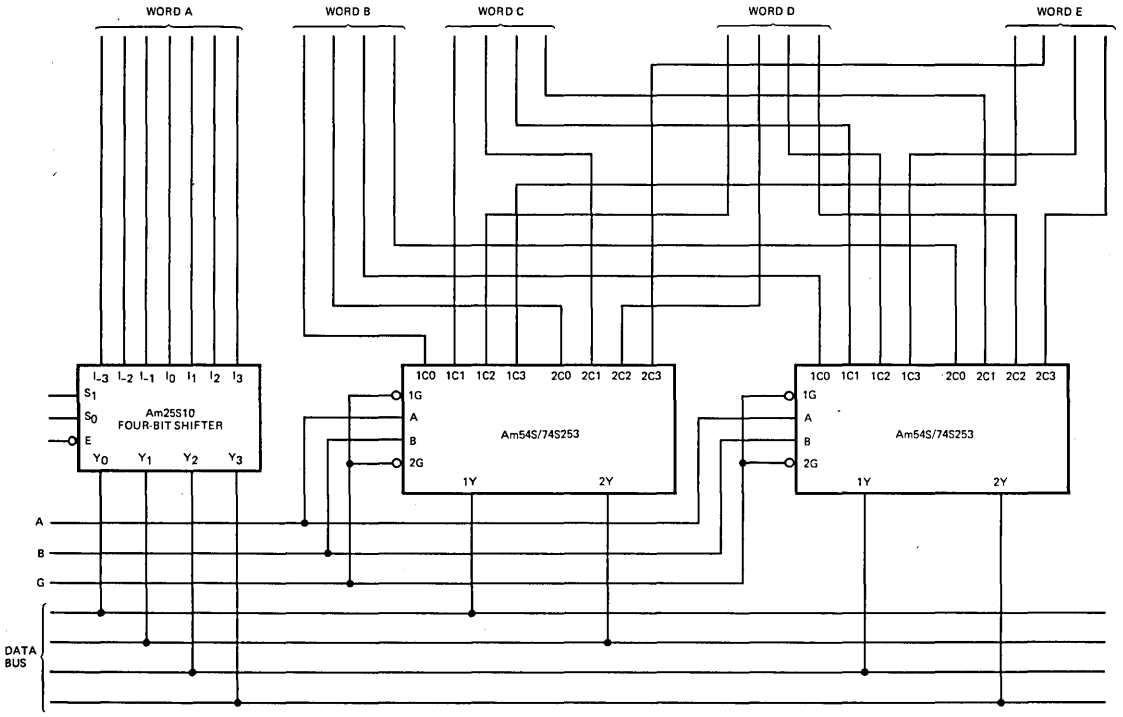
G (Am54S/74S153) Strobe. An active-LOW strobe used to enable the output. A HIGH level input forces the output LOW regardless of the other inputs.

G (Am54S/74S253) Output Control. An active-LOW three-state control used to enable the output. A HIGH level input forces the output to the high-impedance (off) state.

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown



Am54S/74S253 Dual 4-Input Multiplexer in a Bus-Organized System

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

f_{MAX} The highest operating clock frequency.

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{PW} Pulse width. The time between the leading and trailing edges of a pulse.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

t_s Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

t_h Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.

t_R Release time. The time interval for which a signal may be indeterminant at one input terminal before an active transition occurs at another input terminal. (The release time falls within the set-up time interval and is specified by some manufacturers as a negative hold time).

t_{HZ} HIGH to disable. The delay time from a control input change to the three-state output HIGH-level to high-impedance transition (measured at 0.5 V change).

t_{LZ} LOW to disable. The delay time from a control input change to the three-state output LOW-level to high-impedance transition (measured at 0.5V change).

t_{ZH} Enable HIGH. The delay time from a control input change to the three-state output high-impedance to HIGH-level transition.

t_{ZL} Enable LOW. The delay time from a control input change to the three-state output high-impedance to LOW-level transition.

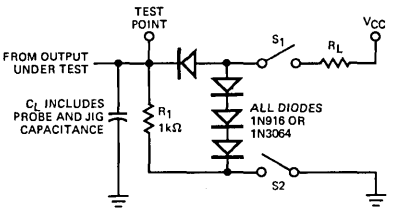
UNIT LOAD DEFINITIONS

SERIES	HIGH Current	HIGH Measure Voltage	LOW Current	LOW Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0 mA	0.5 V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

Note: 1. 54L/74L has two different types of standard inputs.

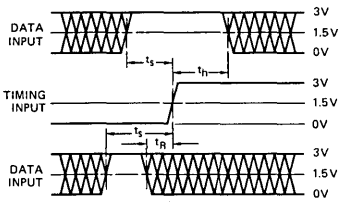
SCHOTTKY PARAMETER MEASUREMENTS
FOR THREE-STATE OUTPUTS

LOAD TEST CIRCUIT



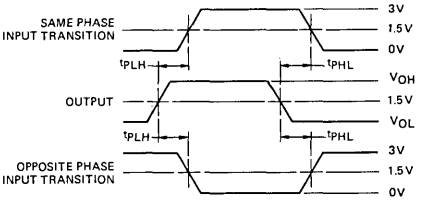
Note: For S153, Remove R_1; S_1 and S_2 closed.

SET-UP, HOLD, AND RELEASE TIMES

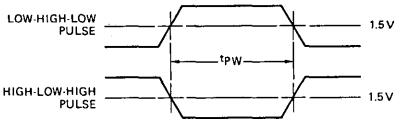


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

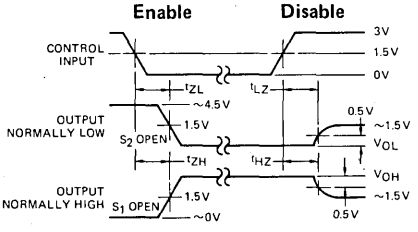
PROPAGATION DELAY



PULSE WIDTH



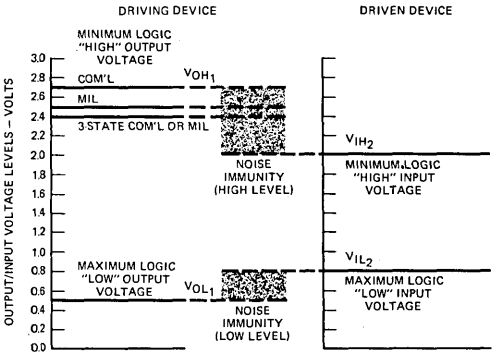
ENABLE AND DISABLE TIMES
S253 Only

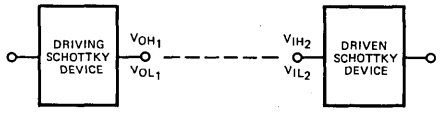


Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1 and S_2 of Load Circuit are closed except where shown.

Note: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_o = 50Ω; t_r ≤ 2.5 ns; t_f ≤ 2.5 ns.

SCHOTTKY INPUT/OUTPUT VOLTAGE INTERFACE CONDITIONS





Note: Refer to Electrical Characteristics for measure current.

DEFINITION OF STANDARD TERMS

H HIGH, applying to a HIGH voltage level.

L LOW, applying to a LOW voltage level.

I Input.

O Output.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

I_{IL} LOW-level input current with a specified LOW-level voltage applied.

I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.

I_{OL} LOW-level output current.

I_{OH} HIGH-level output current.

I_{SC} Output short-circuit source current.

I_{CC} The supply current drawn by the device from the V_{CC} power supply.

V_{IL} Logic LOW input voltage.

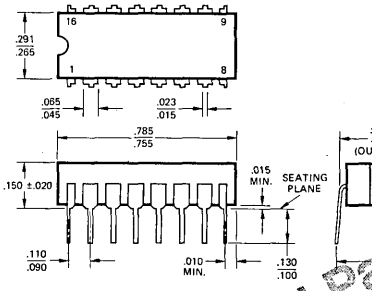
V_{IH} Logic HIGH input voltage.

V_{OL} LOW-level output voltage with I_{OL} applied.

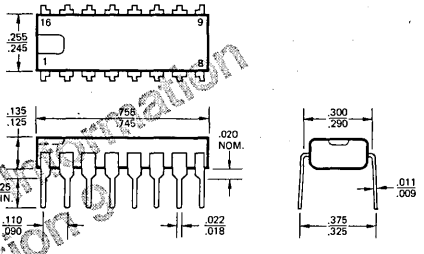
V_{OH} HIGH-level output voltage with I_{OH} applied.

PHYSICAL DIMENSIONS
Dual-In-Line

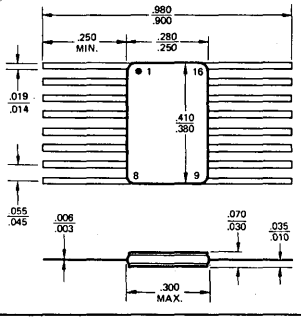
Ceramic



Molded



Flat Package



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Am54S/74S157 • Am54S/74S158 • Am93S22

Quadruple 2-Line-to-1-Line Data Selectors/ Multiplexers

Distinctive Characteristics

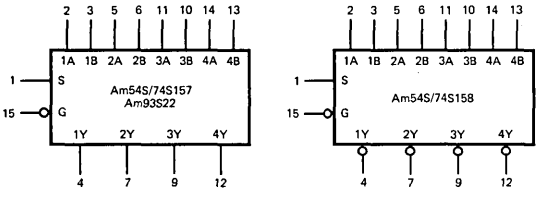
- Schottky clamp provides improved A-C performance.
- Selects four of eight data inputs with single select line and over-riding strobe.
- Inverting or non-inverting data output configurations.
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

These data selectors/multiplexers are used to select a 4-bit word from one of two sources. The four outputs at the Am54S/74S157 • Am93S22 present true data with respect to the input data. The four outputs of the Am54S/74S158 present inverted data with respect to the inputs and also minimize propagation delay. A common active-HIGH strobe (active-LOW enable) is provided on all devices.

A single select line, S, is used to select one of the two multiplexer input words. When the select is LOW, the A input word is present at the output. When the select is HIGH, the B input word is present at the output.

LOGIC SYMBOLS

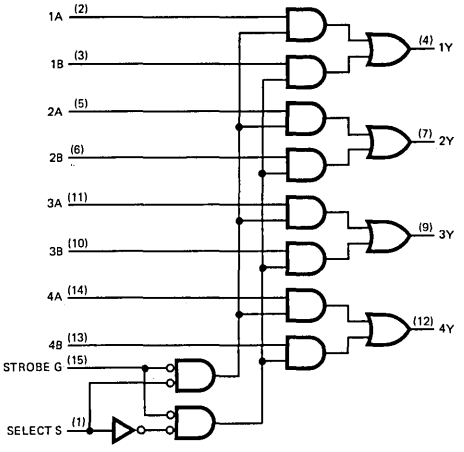


V_{CC} = Pin 16
GND = Pin 8

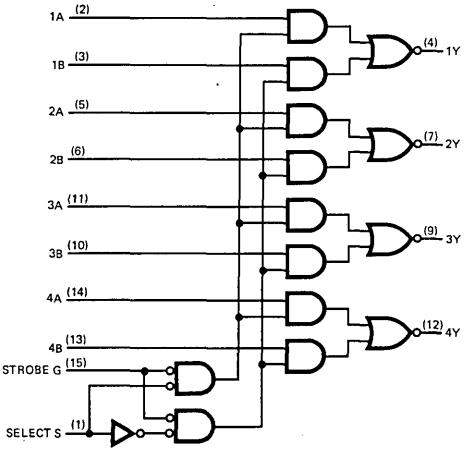
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAMS

Am54S/74S157 • Am93S22



Am54S/74S158

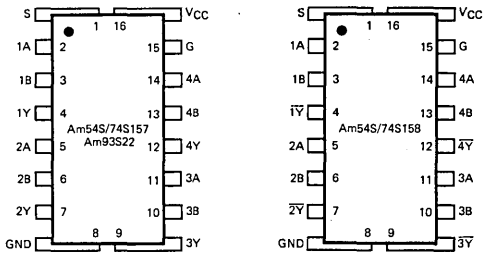


ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am54S/74S157	Molded DIP	0°C to +70°C	SN74S157N
	Hermetic DIP	0°C to +70°C	SN74S157J
	Dice	0°C to +70°C	SN74S157X
	Hermetic DIP	−55°C to +125°C	SN54S157J
	Hermetic Flat Pak	−55°C to +125°C	SN54S157W
	Dice	−55°C to +125°C	SN54S157X
Am54S/74S158	Molded DIP	0°C to +70°C	SN74S158N
	Hermetic DIP	0°C to +70°C	SN74S158J
	Dice	0°C to +70°C	SN74S158X
	Hermetic DIP	−55°C to +125°C	SN54S158J
	Hermetic Flat Pak	−55°C to +125°C	SN54S158W
	Dice	−55°C to +125°C	SN54S158X
Am93S22	Molded DIP	0°C to +70°C	93S22PC
	Hermetic DIP	0°C to +70°C	93S22DC
	Dice	0°C to +70°C	93S22XC
	Hermetic DIP	−55°C to +125°C	93S22DM
	Hermetic Flat Pak	−55°C to +125°C	93S22FM
	Dice	−55°C to +125°C	93S22XM

CONNECTIONS DIAGRAMS

Top Views



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am74S157, Am74S158, Am93S22XC T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am54S157, Am54S158, Am93S22XM T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL) MIN. = 4.5V MAX. = 5.5V

Parameters	Description		Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage		V_{CC} = MIN., I_{OH} = −1mA V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage		V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level		Guaranteed input logical HIGH voltage for all inputs		2			Volts
V_{IL}	Input LOW Level		Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage		V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	S or G	V_{CC} = MAX., V_{IN} = 0.5V				−4	mA
		A or B					−2	
I_{IH} (Note 3)	Input HIGH Current	S or G	V_{CC} = MAX., V_{IN} = 2.7V				100	µA
		A or B					50	
I_I	Input HIGH Current		V_{CC} = MAX., V_{IN} = 5.5V				1	mA
I_{SC}	Output Short Circuit Current (Note 4)		V_{CC} = MAX., V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current		V_{CC} = MAX. (Note 5)	S157		50	78	mA
				S158		39	61	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} is measured with all outputs open and 4.5V applied to all inputs.

Switching Characteristics (T_A = +25°C)

Parameters	Description		Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Data to Output	S157	V_{CC} = 5.0V, C_L = 15pF, R_L = 280Ω		5	7.5	ns
		S158			4	6	
t_{PHL}	Data to Output	S157			4.5	6.5	ns
		S158			4	6	
t_{PLH}	Strobe to Output	S157			8.5	12.5	ns
		S158			6.5	11.5	
t_{PHL}	Strobe to Output	S157			7.5	12	ns
		S158			7	12	
t_{PLH}	Select to Output	S157			9.5	15	ns
		S158			8	12	
t_{PHL}	Select to Output	S157			9.5	15	ns
		S158			8	12	

FUNCTION TABLE

INPUTS				OUTPUTS	
Strobe G	Select S	Data A	Data B	S157 Y	S158 Y
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = HIGH
L = LOW
X = Don't Care

LOADING RULES (In Unit Loads)

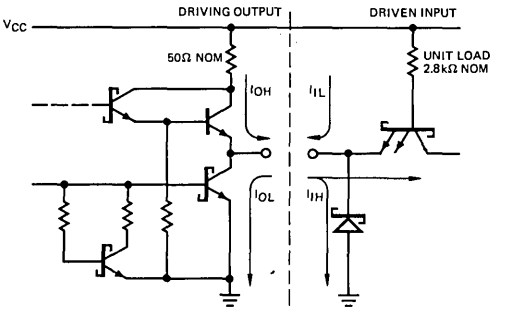
Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
S	1	2	–	–
1A	2	1	–	–
1B	3	1	–	–
1Y	4	–	20	10
2A	5	1	–	–
2B	6	1	–	–
2Y	7	–	20	10
GND	8	–	–	–
3Y	9	–	20	10
3B	10	1	–	–
3A	11	1	–	–
4Y	12	–	20	10
4B	13	1	–	–
4A	14	1	–	–
G	15	2	–	–
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and –2.0mA measured at 0.5V LOW.

DEFINITION OF FUNCTIONAL TERMS

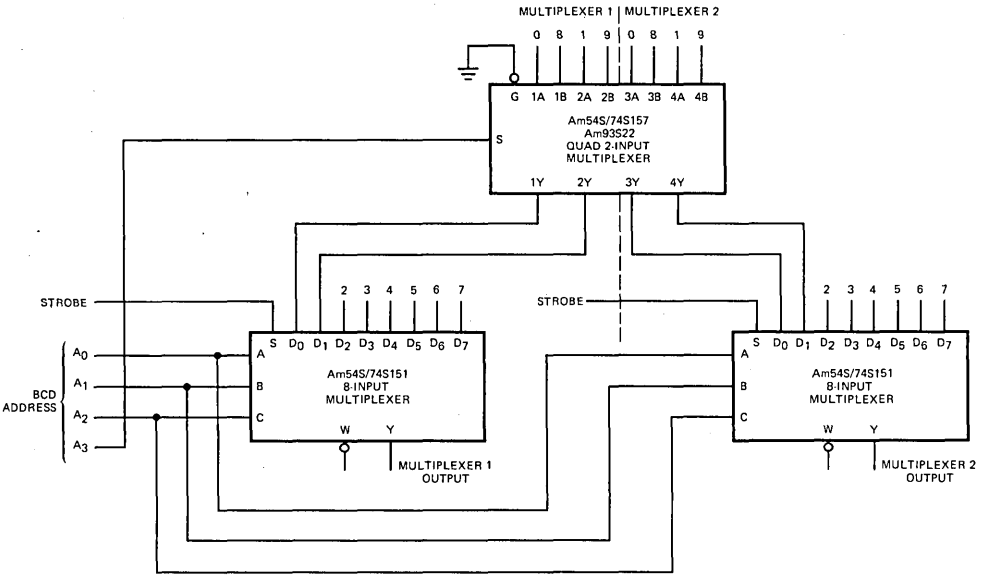
1A, 2A, 3A, 4A The data inputs for the 4-bits of the A word.
1B, 2B, 3B, 4B The data inputs for the 4-bits of the B word.
1Y, 2Y 3Y, 4Y The four outputs of the multiplexer.
G Strobe When the strobe is HIGH, the four outputs of the Am54S/74S157 (Am93S22) are LOW and the outputs of the Am54S/74S158 are HIGH. When the strobe is LOW, the devices are enable to pass data.
S Select When the select input is LOW, the A word is present at the output. When the select input is HIGH, the B word is present at the output.

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

APPLICATION

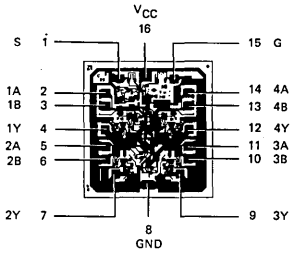


Dual 10-Input Multiplexer

Two 10-input multiplexers are shown above with the select lines common to the two multiplexers. Inputs are selected by an 8421 BCD Address.

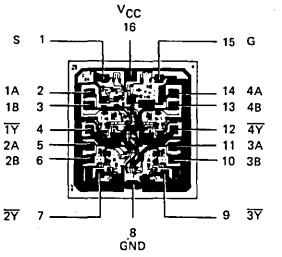
Metallization and Pad Layouts

Am54S/74S157



DIE SIZE 0.065" X 0.069"

Am54S/74S158



DIE SIZE 0.065" X 0.069"

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

f_{MAX} The highest operating clock frequency.

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{PW} Pulse width. The time between the leading and trailing edges of a pulse.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

t_s Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

t_h Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.

t_R Release time. The time interval for which a signal may be indeterminant at one input terminal before an active transition occurs at another input terminal. (The release time falls within the set-up time interval and is specified by some manufacturers as a negative hold time).

UNIT LOAD DEFINITIONS

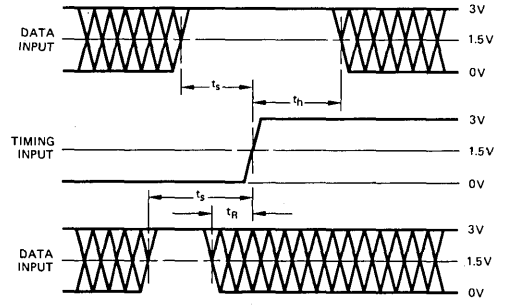
	HIGH		LOW	
SERIES	Current	Measure Voltage	Current	Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0mA	0.5V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

Note: 1. 54L/74L has two different types of standard inputs.

SCHOTTKY PARAMETER MEASUREMENTS

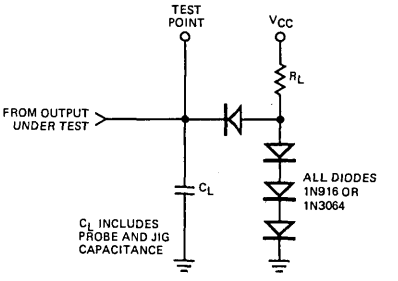
FOR STANDARD ACTIVE-PULLUP TOTEM-POLE OUTPUTS

SET-UP, HOLD, AND RELEASE TIMES

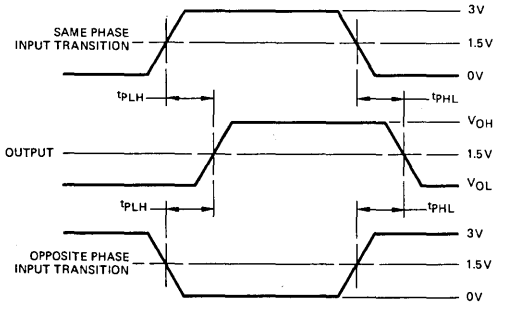


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched area is don't care condition.

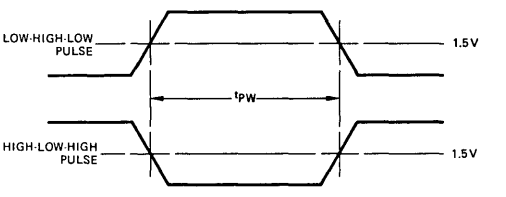
LOAD TEST CIRCUIT



PROPAGATION DELAY

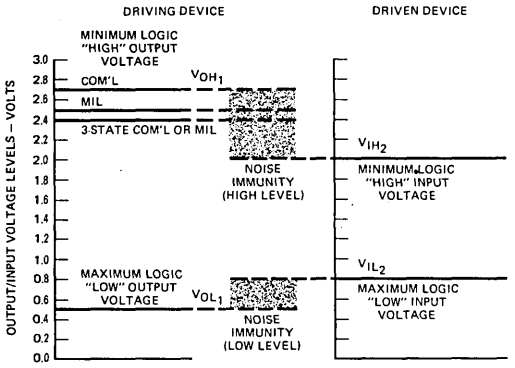


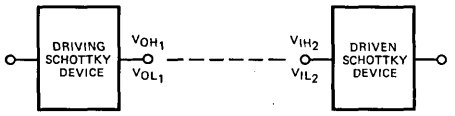
PULSE WIDTH



Note: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_o = 50\Omega$, $t_r \leq 2.5$ns; $t_f \leq 2.5$ns.

SCHOTTKY INPUT/OUTPUT VOLTAGE INTERFACE CONDITIONS





Note: Refer to Electrical Characteristics for measure currents.

DEFINITION OF STANDARD TERMS

H HIGH, applying to a HIGH voltage level.

L LOW, applying to a LOW voltage level.

I Input.

O Output.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

I_{IL} LOW-level input current with a specified LOW-level voltage applied.

I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.

I_{OL} LOW-level output current.

I_{OH} HIGH-level output current.

I_{SC} Output short-circuit source current.

I_{CC} The supply current drawn by the device from the V_{CC} power supply.

V_{IL} Logic LOW input voltage.

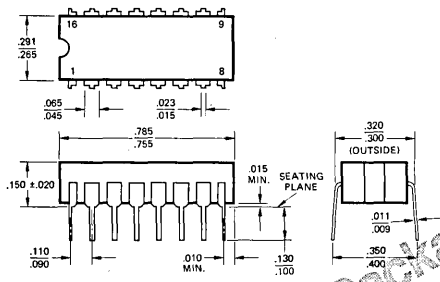
V_{IH} Logic HIGH input voltage.

V_{OL} LOW-level output voltage with I_{OL} applied.

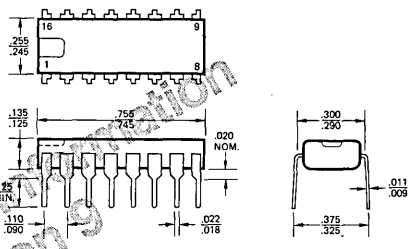
V_{OH} HIGH-level output voltage with I_{OH} applied.

PHYSICAL DIMENSIONS
Dual-In-Line

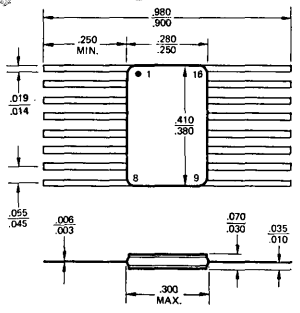
Ceramic



Molded



Flat Package



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California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am54S/74S174•Am54S/74S175

Hex/Quadruple D-Type Flip Flops With Clear

Distinctive Characteristics

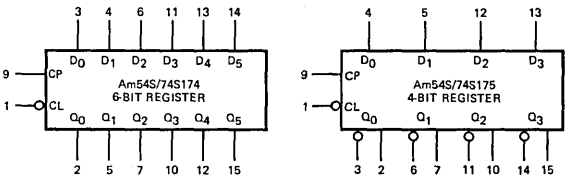
- 4-Bit and 6-Bit high-speed parallel registers.
- Common clock and common clear.
- Positive edge-triggered D flip-flops
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

The Am54S/74S174 is a six-bit, high-speed register and the Am54S/74S175 is a four-bit, high-speed register built using advanced Schottky technology. The registers consist of D-type flip-flops with a buffered common clock and an asynchronous active LOW buffered clear.

When the clear is LOW, the Q outputs are LOW independent of the other inputs. Information meeting the set-up requirements of the D inputs is transferred to the Q outputs on the positive-going edge of the clock pulse.

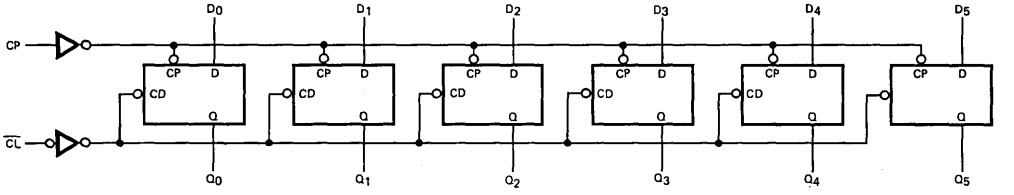
LOGIC SYMBOLS



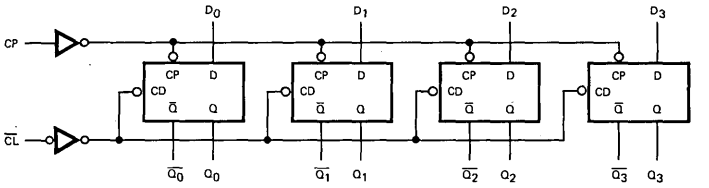
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAMS

Am54S/74S174



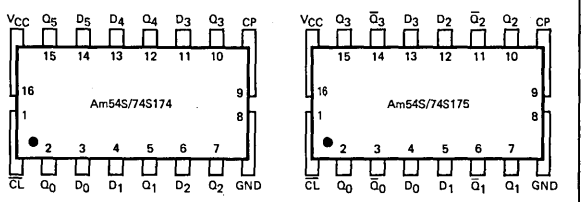
Am54S/74S175



ORDERING INFORMATION

Package Type	Temperature Range	Am54S/74S174 Order Number	Am54S/74S175 Order Number
Molded DIP	0°C to +70°C	SN74S174N	SN74S175N
Hermetic DIP	0°C to +70°C	SN74S174J	SN74S175J
Dice	0°C to +70°C	SN74S174X	SN74S175X
Hermetic DIP	−55°C to +125°C	SN54S174J	SN54S175J
Hermetic Flat Pak	−55°C to +125°C	SN54S174W	SN54S175W
Dice	−55°C to +125°C	SN54S174X	SN54S175X

CONNECTION DIAGRAMS
Top Views



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am74S174, Am74S175 T_A = 0°C to +70°C V_{CC} = 5.0 V ±5% (COM'L) MIN. = 4.75 V MAX. = 5.25 V
Am54S174, Am54S175 T_A = −55°C to +125°C V_{CC} = 5.0 V ±10% (MIL) MIN. = 4.5 V MAX. = 5.5 V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1 mA V_{IN} = V_{IH} or V_{IL}	74S	2.7	3.4		Volts
			54S	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20 mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18 mA				−1.2	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5 V				−2	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7 V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0 V		−40		−100	mA
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX.	S174		90	144	mA
			S175		60	96	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. All outputs open and 4.5 V applied to the data and clear inputs. Measured after a momentary ground, then 4.5 V applied to the clock input.

Switching Characteristics (T_A = +25°C)

Parameters	Description		Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Clock to Output		V_{CC} = 5.0 V, C_L = 15 pF, R_L = 280 Ω		8	12	ns
t_{PHL}					11.5	17	
t_{PLH}	Clear to Output				10	15	ns
t_{PHL}					13	22	
t_{pw}	Pulse Width	Clock		7			ns
		Clear		10			
t_s	Data Set-up Time			5			ns
t_s	Set-up Time. Clear Recovery (in-active) to Clock			5			ns
t_h	Data Hold Time			3			ns
f_{MAX}	Maximum Clock Frequency			75	110		MHz

Am54S/74S174 LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{CL}$	1	1	–	–
Q_0	2	–	20	10
D_0	3	1	–	–
D_1	4	1	–	–
Q_1	5	–	20	10
D_2	6	1	–	–
Q_2	7	–	20	10
GND	8	–	–	–
CP	9	1	–	–
Q_3	10	–	20	10
D_3	11	1	–	–
Q_4	12	–	20	10
D_4	13	1	–	–
D_5	14	1	–	–
Q_5	15	–	20	10
V_{CC}	16	–	–	–

Am54S/74S175 LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{CL}$	1	1	–	–
Q_0	2	–	20	10
$\overline{Q}_0$	3	–	20	10
D_0	4	1	–	–
D_1	5	1	–	–
$\overline{Q}_1$	6	–	20	10
Q_1	7	–	20	10
GND	8	–	–	–
CP	9	1	–	–
Q_2	10	–	20	10
$\overline{Q}_2$	11	–	20	10
D_2	12	1	–	–
D_3	13	1	–	–
$\overline{Q}_3$	14	–	20	10
Q_3	15	–	20	10
V_{CC}	16	–	–	–

FUNCTION TABLE

INPUTS			OUTPUTS	
Clear	Clock	D_i	Q_i	$\overline{Q}_i$
L	X	X	L	H
H	L	X	NC	NC
H	H	X	NC	NC
H	↑	L	L	H
H	↑	H	H	L

H = HIGH X = Don't Care
L = LOW NC = No Change
↑ = LOW-to-HIGH Transition

Note: $\overline{Q}_i$ on Am54S/74S175 only

DEFINITION OF FUNCTIONAL TERMS

D_i The D flip-flop data inputs.

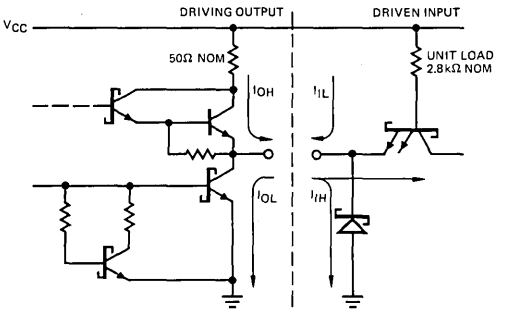
CL Clear. When the clear is LOW, the Qi outputs are LOW, regardless of the other inputs. When the clear is HIGH, data can be entered in the register.

CP Clock pulse for the register. Enters data on the positive transition.

Q_i The TRUE register outputs.

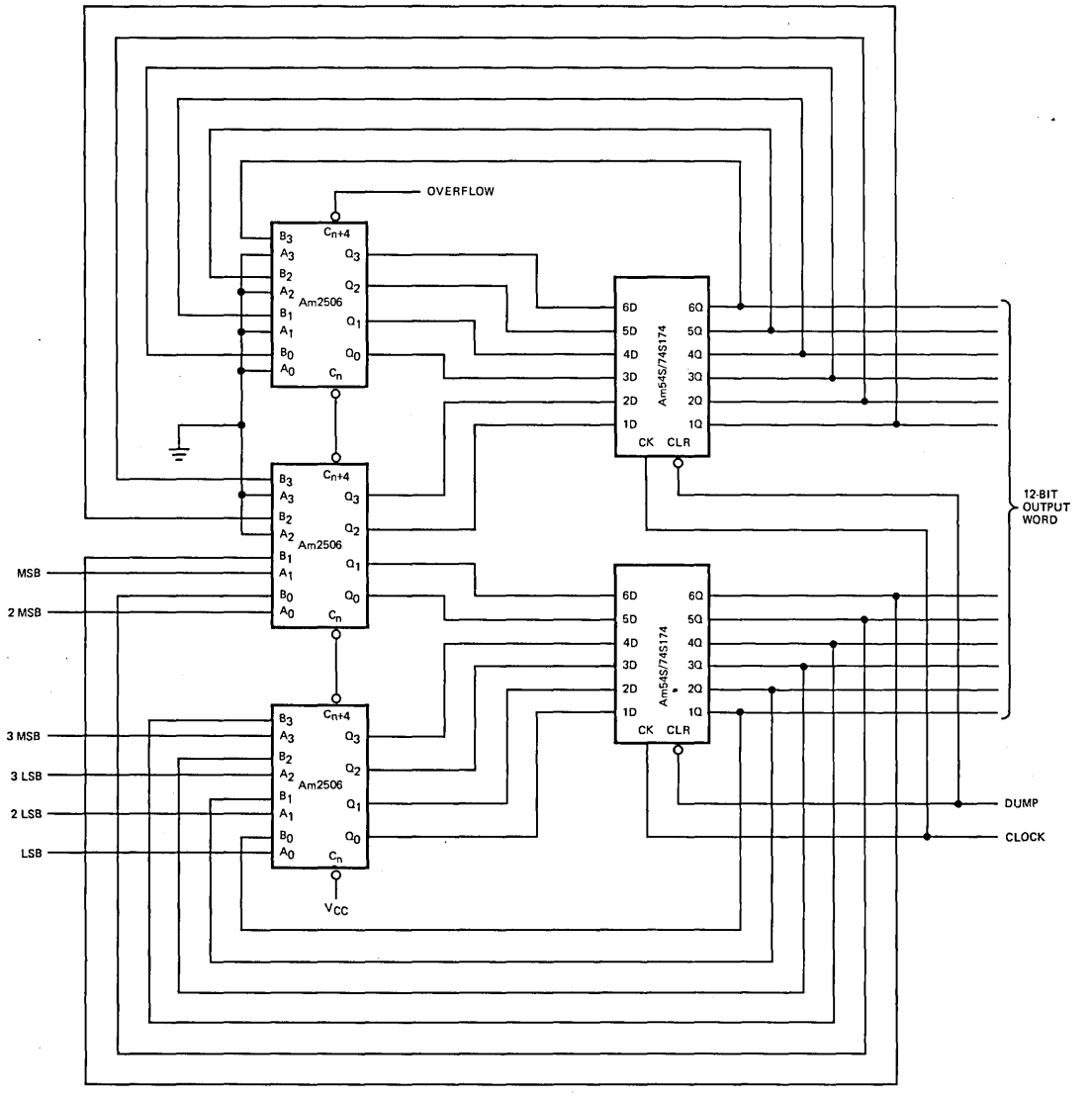
$\overline{Q}_i$ The complement register outputs.

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

APPLICATION

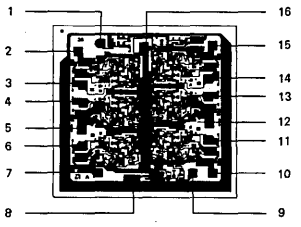


($Am2506\ E = S_0 = HIGH;\ M = S_1 = S_2 = S_3 = LOW$)

6-Bit Input, Integrate and Dump for Magnitude-Only Arithmetic (65 samples min. before overflow)

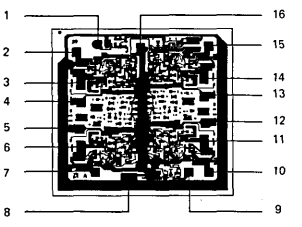
Metallization and Pad Layouts

Am54S/74S174



DIE SIZE 0.085" X 0.081"

Am54S/74S175



DIE SIZE 0.085" X 0.081"

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

f_{MAX} The highest operating clock frequency.

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{PW} Pulse width. The time between the leading and trailing edges of a pulse.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

t_s Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

t_h Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.

t_R Release time. The time interval for which a signal may be indeterminant at one input terminal before an active transition occurs at another input terminal. (The release time falls within the set-up time interval and is specified by some manufacturers as a negative hold time).

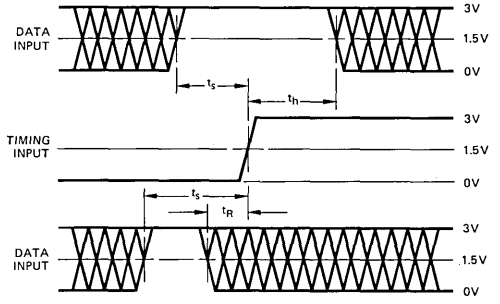
UNIT LOAD DEFINITIONS

	HIGH		LOW	
SERIES	Current	Measure Voltage	Current	Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0mA	0.5V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

Note: 1. 54L/74L has two different types of standard inputs.

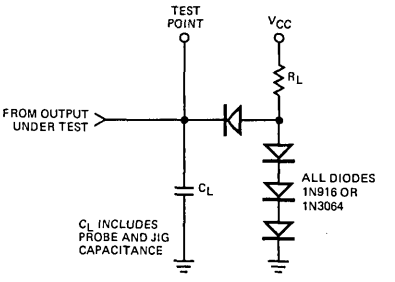
SCHOTTKY PARAMETER MEASUREMENTS
FOR STANDARD ACTIVE-PULLUP TOTEM-POLE OUTPUTS

SET-UP, HOLD, AND RELEASE TIMES

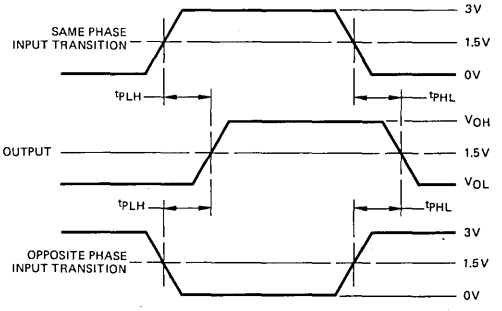


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched area is don't care condition.

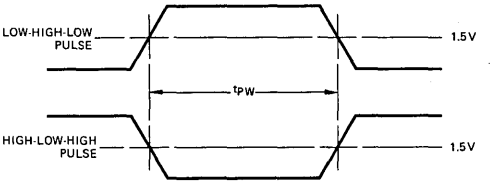
LOAD TEST CIRCUIT



PROPAGATION DELAY

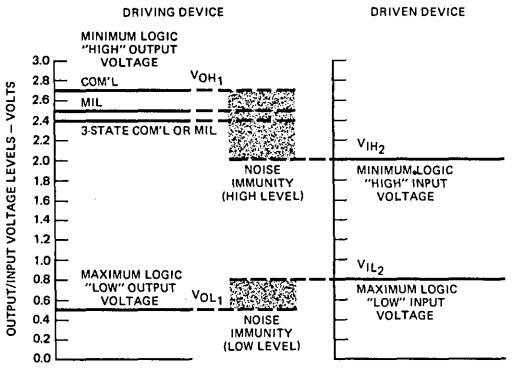


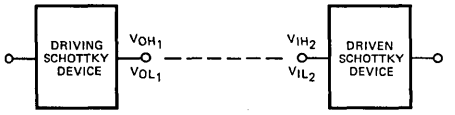
PULSE WIDTH



Note: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_o = 50\Omega$, $t_r \leq 2.5$ns; $t_f \leq 2.5$ns.

SCHOTTKY INPUT/OUTPUT VOLTAGE INTERFACE CONDITIONS





Note: Refer to Electrical Characteristics for measure currents.

DEFINITION OF STANDARD TERMS

H HIGH, applying to a HIGH voltage level.

L LOW, applying to a LOW voltage level.

I Input.

O Output.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

I_{IL} LOW-level input current with a specified LOW-level voltage applied.

I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.

I_{OL} LOW-level output current.

I_{OH} HIGH-level output current.

I_{SC} Output short-circuit source current.

I_{CC} The supply current drawn by the device from the V_{CC} power supply.

V_{IL} Logic LOW input voltage.

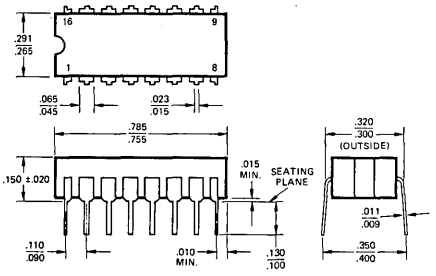
V_{IH} Logic HIGH input voltage.

V_{OL} LOW-level output voltage with I_{OL} applied.

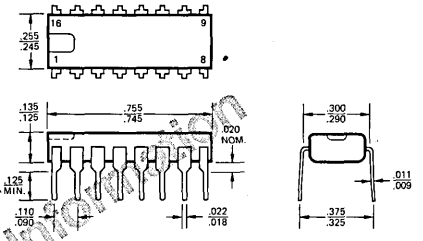
V_{OH} HIGH-level output voltage with I_{OH} applied.

PHYSICAL DIMENSIONS
Dual-In-Line

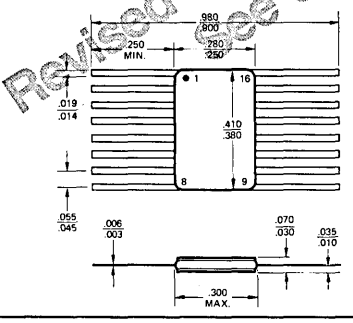
Ceramic



Molded



Flat Package



ADVANCED MICRO DEVICES INC.
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California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am54S/74S181

Four-Bit Arithmetic Logic Unit/Function Generator

Distinctive Characteristics

- Advanced Schottky technology
- Performs 16 arithmetic operations including add, subtract, double and compare.
- Performs all 16 possible logic operations of two variables in typically 11ns.
- Typical 4-bit add time is 11ns and carry time is 6ns.
- Full look-ahead capability for high-speed arithmetic operation on long words.
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

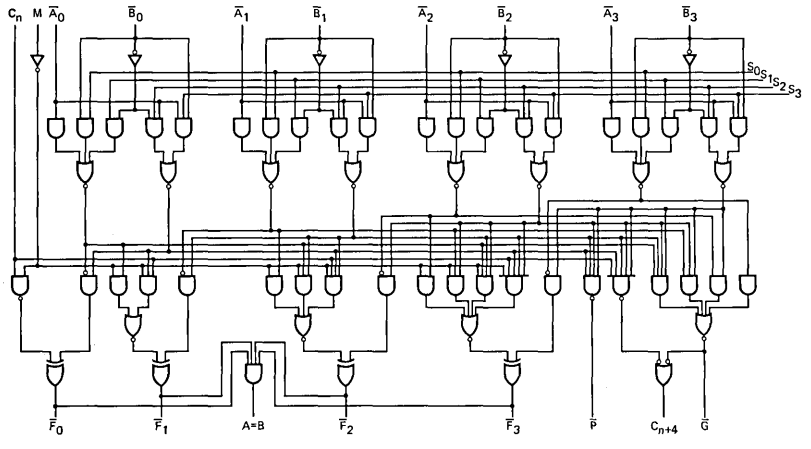
The Am54S/74S181 is a 4-bit, high-speed parallel Arithmetic Logic Unit (ALU)/Digital Function Generator. When the mode control (M) is LOW the 16 arithmetic operations are performed under the control of the four select inputs. When the mode control is HIGH the sixteen logic operations are performed on an individual bit basis between the two 4-bit parallel words under the control of the four select inputs.

An internal full look-ahead carry scheme is used for high-speed arithmetic operations and provision is made for further look-ahead by including both carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs.

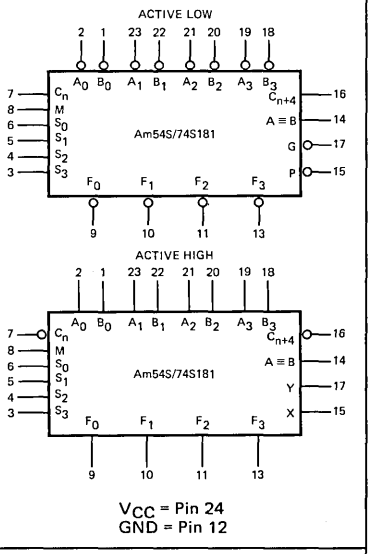
An open collector output A = B is used to signal the equivalence of the two parallel words. The open collector feature allows for the equivalence function to be expanded as a wired-AND connection for larger word lengths.

In many systems, the carry output C_{n+4} is connected to the next higher C_n to provide ripple block arithmetic. The ALU can be used with either active HIGH or active LOW inputs and can be ripple expanded or full look-ahead expanded in either mode. The connection pattern is identical for either logic representation.

LOGIC DIAGRAM



LOGIC SYMBOLS

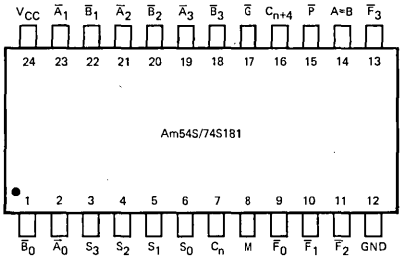


V_{CC} = Pin 24
GND = Pin 12

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	SN74S181N
Hermetic DIP	0°C to +70°C	SN74S181J
Dice	0°C to +70°C	SN74S181X
Hermetic DIP	−55°C to +125°C	SN54S181J
Hermetic Flat Pak	−55°C to +125°C	SN54S181W
Dice	−55°C to +125°C	SN54S181X

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise noted)

Am74S181	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5% (COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am54S181	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10% (MIL)	MIN. = 4.5V	MAX. = 5.5V

Parameters	Description		Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage (Except A=B Output)		V_{CC} = MIN., I_{OH} = −1mA V_{IN} = V_{IH} or V_{IL}	54S	2.5	3.4		Volts
				74S	2.7	3.4		
V_{OL}	Output LOW Voltage		V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level		Guaranteed input logical HIGH voltage for all inputs		2			Volts
V_{IL}	Input LOW Level		Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage		V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{OH}	Output HIGH Current for A=B Output		V_{CC} = MIN., V_{OH} = 5.5V V_{IN} = V_{IH} or V_{IL}				250	µA
I_{IL} (Note 3)	Input LOW Current	M	V_{CC} = MAX., V_{IN} = 0.5V				−2	mA
		$\overline{A_i}$ or $\overline{B_i}$					−6	
		S_i					−8	
		C_n					−10	
I_{IH} (Note 3)	Input HIGH Current	M	V_{CC} = MAX., V_{IN} = 2.7V				50	µA
		$\overline{A_i}$ or $\overline{B_i}$					150	
		S_i					200	
		C_n					250	
I_I	Input HIGH Current		V_{CC} = MAX., V_{IN} = 5.5V				1	mA
I_{SC}	Output Short Circuit Current (Note 4) (Except A = B Output)		V_{CC} = MAX.		−40		−100	mA
I_{CC}	Power Supply Current (Note 5)		V_{CC} = MAX.			120	180	mA
			V_{CC} = MAX., T_A = 125°C Am54S Flat Package (W) Only				159	mA

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} is measured under two conditions — typ. and max. apply to both.
   A. S_i, M, A_i at 4.5V; all other inputs grounded; outputs open.
   B. S_i, M at 4.5V; all other inputs grounded; outputs open.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 280Ω)

Parameter	From (Input)	To (Output)	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	C_n	C_{n+4}			5	10.5	ns
t_{PHL}					7	10.5	
t_{PLH}	C_n	$\overline{F}_i$	M = 0V		7	12	ns
t_{PHL}			(SUM or DIFF mode)		6	12	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{G}$	M = 0V, $S_0 = S_3$ = 4.5V,		8	12	ns
t_{PHL}			$S_1 = S_2$ = 0V (SUM mode)		7	12	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{G}$	M = 0V, $S_0 = S_3$ = 0V,		10	15	ns
t_{PHL}			$S_1 = S_2$ = 4.5V (DIFF mode)		10	15	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{P}$	M = 0V, $S_0 = S_3$ = 4.5V,		7.5	12	ns
t_{PHL}			$S_1 = S_2$ = 0V (SUM mode)		7.5	12	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{P}$	M = 0V, $S_0 = S_3$ = 0V,		10	15	ns
t_{PHL}			$S_1 = S_2$ = 4.5V (DIFF mode)		10.5	15	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$F_j (j \geq i)$	M = 0V, $S_0 = S_3$ = 4.5V,		10	16.5	ns
t_{PHL}			$S_1 = S_2$ = 0V (SUM mode)		7	16.5	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$F_j (j \geq i)$	M = 0V, $S_0 = S_3$ = 0V,		12	20	ns
t_{PHL}			$S_1 = S_2$ = 4.5V (DIFF mode)		9	22	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_{i+1}$	M = 0V, $S_0 = S_3$ = 4.5V,		11	16.5	ns
t_{PHL}			$S_1 = S_2$ = 0V (SUM mode)		11	16.5	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_{i+1}$	M = 0V, $S_0 = S_3$ = 0V,		14	20	ns
t_{PHL}			$S_1 = S_2$ = 4.5V (DIFF mode)		14	22	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	$\overline{F}_i$	M = 4.5V (LOGIC mode)		12	20	ns
t_{PHL}					9	22	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	C_{n+4}	M = 0V, $S_0 = S_3$ = 4.5V,		12.5	18.5	ns
t_{PHL}			$S_1 = S_2$ = 0V (SUM mode)		12.5	18.5	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	C_{n+4}	M = 0V, $S_0 = S_3$ = 0V,		14	23	ns
t_{PHL}			$S_1 = S_2$ = 4.5V (DIFF mode)		15	23	
t_{PLH}	$\overline{A}_i$ or $\overline{B}_i$	A = B	M = 0V, $S_0 = S_3$ = 0V,		15	23	ns
t_{PHL}			$S_1 = S_2$ = 4.5V (DIFF mode)		19	30	

OPERATION TABLE

CONTROL INPUTS				ACTIVE LOW INPUTS AND OUTPUTS		ACTIVE HIGH INPUTS AND OUTPUTS	
S_0	S_1	S_2	S_3	Arithmetic (M = L, C_n = L)	Logic (M = H)	Arithmetic (M = L, $\overline{C}_n$ = H)	Logic (M = H)
L	L	L	L	A minus 1	$\overline{A}$	A	$\overline{A}$
H	L	L	L	AB minus 1	$\overline{AB}$	A + B	$\overline{A+B}$
L	H	L	L	$A\overline{B}$ minus 1	$\overline{A}+B$	$A+\overline{B}$	$\overline{A}B$
H	H	L	L	minus 1 (2's comp.)	Logic '1'	minus 1 (2's comp.)	Logic '0'
L	L	H	L	A plus [A + $\overline{B}$]	$\overline{A}+\overline{B}$	A plus $A\overline{B}$	$\overline{AB}$
H	L	H	L	AB plus [A + $\overline{B}$]	$\overline{B}$	$A\overline{B}$ plus [A + B]	$\overline{B}$
L	H	H	L	A minus B minus 1	$\overline{A \oplus B}$	A minus B minus 1	A ⊕ B
H	H	H	L	A + $\overline{B}$	A + $\overline{B}$	$A\overline{B}$ minus 1	$A\overline{B}$
L	L	L	H	A plus [A + B]	$\overline{A}B$	A plus AB	$\overline{A}+B$
H	L	L	H	A plus B	A ⊕ B	A plus B	$\overline{A \oplus B}$
L	H	L	H	$A\overline{B}$ plus [A + B]	B	AB plus [A + $\overline{B}$]	B
H	H	L	H	A + B	A + B	AB minus 1	AB
L	L	H	H	A plus A (2 x A)	Logic '0'	A plus A (2 x A)	Logic '1'
H	L	H	H	A plus AB	$A\overline{B}$	A plus [A + B]	$A+\overline{B}$
L	H	H	H	A plus $A\overline{B}$	AB	A plus [A + $\overline{B}$]	A + B
H	H	H	H	A	A	A minus 1	A

L = LOW Voltage Level
H = HIGH Voltage Level

DEFINITION OF FUNCTIONAL TERMS

$\overline{A}_0, \overline{A}_1, \overline{A}_2, \overline{A}_3$ The A data inputs.

$\overline{B}_0, \overline{B}_1, \overline{B}_2, \overline{B}_3$ The B data inputs.

S_0, S_1, S_2, S_3 The control inputs used to determine the arithmetic or logic function performed.

$\overline{F}_0, \overline{F}_1, \overline{F}_2, \overline{F}_3$ The data outputs of the ALU.

M The mode control inputs used to select either the arithmetic or logic operations.

C_n The carry-in input of the ALU.

C_{n+4} The carry-look-ahead output of the four-bit input field.

$\overline{G}$ The carry-generate output for use in multi-level look-ahead schemes.

$\overline{P}$ The carry-propagate output for use in multi-level look-ahead schemes.

A = B The open collector comparator output that can be used to determine equivalence. This output is HIGH whenever the four $\overline{F}$ outputs are HIGH.

USER NOTES

1. Throughout this data sheet, the active LOW input and output terminology has been used. For the active HIGH definition, the nomenclautre shown under the active HIGH logic symbol should be substituted.
2. Arithmetic operations are performed on a word basis.
3. Logic operations are performed on a bit basis.
4. Arithmetic in 1's complement notation requires an end around carry.
5. Subtraction in 2's complement notation requires a carry in (C_n = HIGH) for the active LOW case and ($\overline{C}_n$ = LOW) for the active HIGH case.
6. The A = B output only indicates that the four $\overline{F}$ outputs are all HIGH.

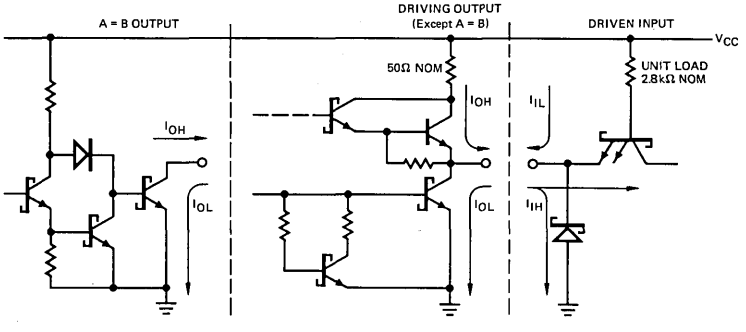
LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Output Drive Output HIGH	Output Drive Output LOW
$\overline{B}_0$	1	3	–	–
$\overline{A}_0$	2	3	–	–
S_3	3	4	–	–
S_2	4	4	–	–
S_1	5	4	–	–
S_0	6	4	–	–
C_n	7	5	–	–
M	8	1	–	–
$\overline{F}_0$	9	–	20	10
$\overline{F}_1$	10	–	20	10
$\overline{F}_2$	11	–	20	10
GND	12	–	–	–
$\overline{F}_3$	13	–	20	10
A = B	14	–	O/C	10
$\overline{P}$	15	–	20	10
C_{n+4}	16	–	20	10
$\overline{G}$	17	–	20	10
$\overline{B}_3$	18	3	–	–
$\overline{A}_3$	19	3	–	–
$\overline{B}_2$	20	3	–	–
$\overline{A}_2$	21	3	–	–
$\overline{B}_1$	22	3	–	–
$\overline{A}_1$	23	3	–	–
V_{CC}	24	–	–	–

O/C = Open Collector

A Schottky unit load is defined as 50μA measured at 2.7V HIGH and −2.0 mA measured at 0.5V LOW.

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

SUM MODE TEST TABLE

FUNCTION INPUTS: $S_0 = S_3 = 4.5V$, $S_1 = S_2 = M = 0V$

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply 0V	Apply 4.5V	Apply 0V		
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i (i \geq i)$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i (i \geq i)$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_{i+1}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_{i+1}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}	In-Phase

DIFF MODE TEST TABLE

FUNCTION INPUTS: $S_1 = S_2 = 4.5V$, $S_0 = S_3 = M = 0V$

Parameter	Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply 0V	Apply 4.5V	Apply 0V		
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i (i \geq i)$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i (i \geq i)$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_{i+1}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_{i+1}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	In-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}	In-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	Any $\overline{F}$ or C_{n+4}	In-Phase

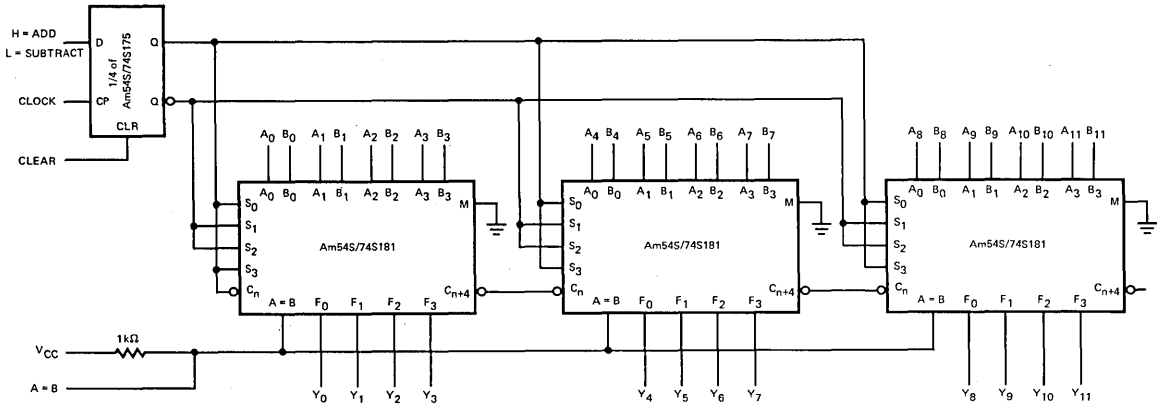
LOGIC MODE TEST TABLE

FUNCTION INPUTS: $S_1 = S_2 = M = 4.5V$, $S_0 = S_3 = 0V$

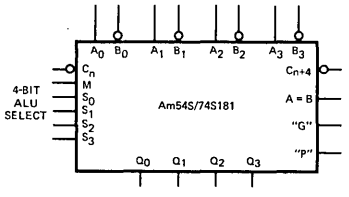
Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply 0V	Apply 4.5V	Apply 0V		
t_{PLH} / t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	Out-of-Phase
t_{PLH} / t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	Out-of-Phase

APPLICATIONS

12-Bit Adder/Subtractor (2's Complement)



If one input is defined active–HIGH and the second input is defined active–LOW, the sixteen arithmetic and logic functions of the ALU are reordered as shown in the function table.



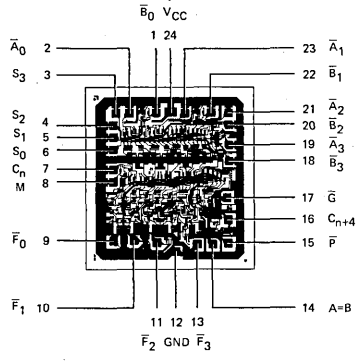
Function Table

A = Active HIGH B = Active LOW

S_0	S_1	S_2	S_3	Arithmetic (M = L, $\overline{C}_n$ = H)	Logic (M = H)
L	L	L	L	A	$\overline{A}$
H	L	L	L	A + $\overline{B}$	$\overline{A}$B
L	H	L	L	A + B	$\overline{A\overline{B}}$
H	H	L	L	minus 1 (2's comp.)	Logic '0'
L	L	H	L	A plus AB	AB
H	L	H	L	AB plus [A + $\overline{B}$]	B
L	H	H	L	A plus B	$\overline{A \oplus B}$
H	H	H	L	AB minus 1	AB
L	L	L	H	A plus A$\overline{B}$	$\overline{A} + \overline{B}$
H	L	L	H	A minus B minus 1	A $\oplus$ B
L	H	L	H	A$\overline{B}$ plus [A + B]	$\overline{B}$
H	H	L	H	A$\overline{B}$ minus 1	A$\overline{B}$
L	L	H	H	A plus A (2 x A)	Logic '1'
H	L	H	H	A plus [A + $\overline{B}$]	A + B
L	H	H	H	A plus [A + B]	A + $\overline{B}$
H	H	H	H	A minus 1	A

L = Low Voltage Level
H = High Voltage Level

Metallization and Pad Layout



DIE SIZE: = 0.083" X 0.091"

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

f_{MAX} The highest operating clock frequency.

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{PW} Pulse width. The time between the leading and trailing edges of a pulse.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

t_s Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

t_h Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.

t_R Release time. The time interval for which a signal may be indeterminant at one input terminal before an active transition occurs at another input terminal. (The release time falls within the set-up time interval and is specified by some manufacturers as a negative hold time).

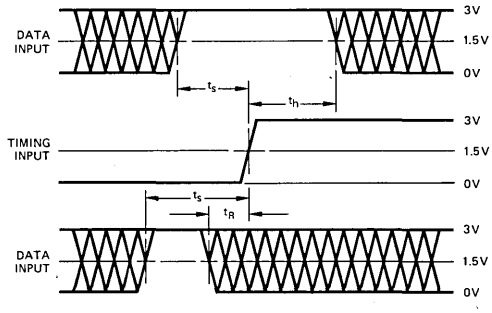
UNIT LOAD DEFINITIONS

	HIGH		LOW	
SERIES	Current	Measure Voltage	Current	Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0mA	0.5V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

Note: 1. 54L/74L has two different types of standard inputs.

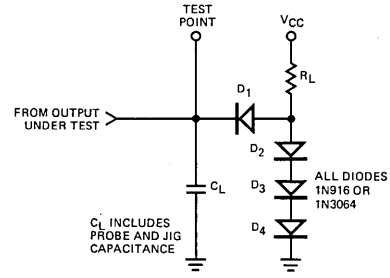
SCHOTTKY PARAMETER MEASUREMENTS
FOR STANDARD ACTIVE-PULLUP TOTEM-POLE OUTPTS

SET-UP, HOLD, AND RELEASE TIMES



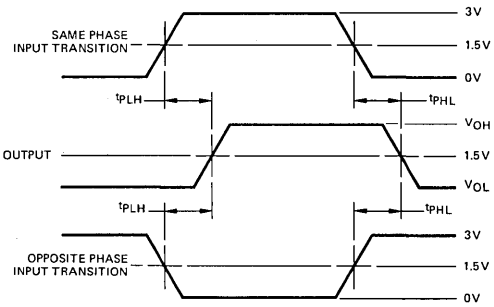
Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched area is don't care condition.

LOAD TEST CIRCUIT

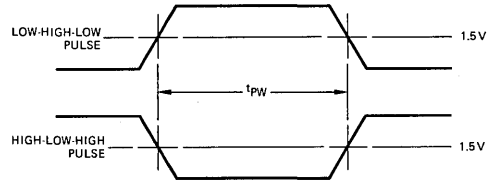


Note: For A = B Output, short D_1 and remove D_2, D_3 and D_4.

PROPAGATION DELAY

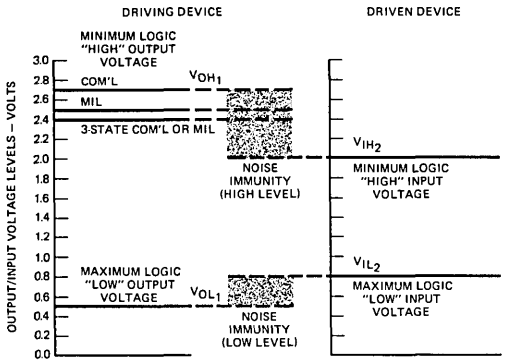


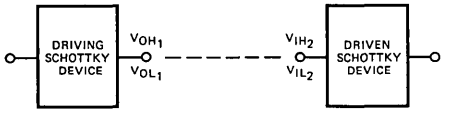
PULSEWIDTH



Note: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_o = 50\Omega$; $t_r \leq 2.5$ns; $t_f \leq 2.5$ns.

SCHOTTKY INPUT/OUTPUT VOLTAGE INTERFACE CONDITIONS





Note: Refer to Electrical Characteristics for measure currents.

DEFINITION OF STANDARD TERMS

H HIGH, applying to a HIGH voltage level.

L LOW, applying to a LOW voltage level.

I Input.

O Output.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

I_{IL} LOW-level input current with a specified LOW-level voltage applied.

I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.

I_{OL} LOW-level output current.

I_{OH} HIGH-level output current.

I_{SC} Output short-circuit source current.

I_{CC} The supply current drawn by the device from the V_{CC} power supply.

V_{IL} Logic LOW input voltage.

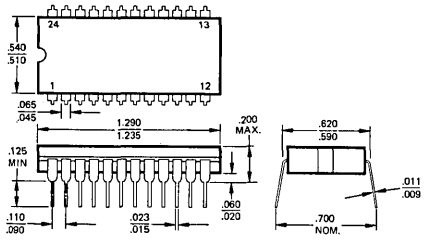
V_{IH} Logic HIGH input voltage.

V_{OL} LOW-level output voltage with I_{OL} applied.

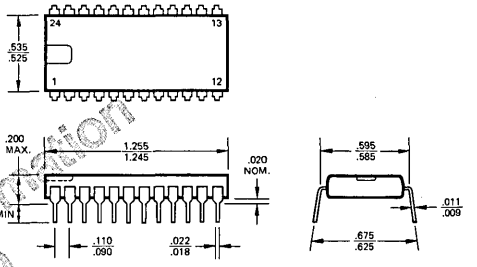
V_{OH} HIGH-level output voltage with I_{OH} applied.

PHYSICAL DIMENSIONS
Dual-In-Line

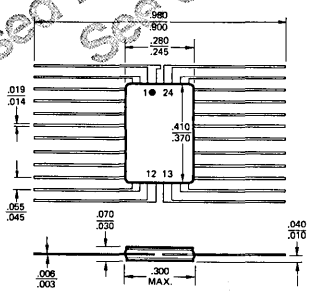
Ceramic



Molded



Flat Package



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Am54S/74S194•Am54S/74S195

Four-Bit High-Speed Shift Registers

Distinctive Characteristics

- Parallel load or shift right with J$\overline{K}$ inputs on Am54S/74S195
- Shift left, right, parallel load or do nothing on Am54S/74S194
- Fully synchronous shifting and parallel loading
- Buffered common clock
- Buffered common active-LOW clear
- 100% reliability assurance testing in compliance with MIL-STD-883

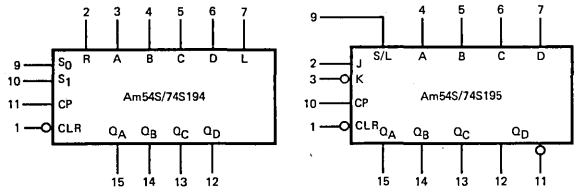
FUNCTIONAL DESCRIPTION

The Am54S/74S194 and Am54S/74S195 are 4-bit registers that exhibit fully synchronous operation in all operating modes. The Am54S/74S195 can either parallel load all four register bits via the parallel inputs (A, B, C, D) or shift each of the four register bits right one place. The shifting or parallel loading is under control of the shift/load input (S/L). When the shift/load input is LOW, data is loaded from the parallel data inputs; when the shift/load input is HIGH, data is loaded from the register bits on the left. The first bit, Q_A, is loaded via the J and $\overline{K}$ inputs in the shift mode.

The Am54S/74S194 operates in four modes under control of the two select inputs, S_0 and S_1. The four modes are parallel load (data comes from the parallel inputs), shift right (data comes from the flip-flop to the left, with the Q_A bit input from R), shift left (data comes from the flip-flop to the right, with the Q_D input from L), and hold or do nothing (each flip-flop receives data from its own output).

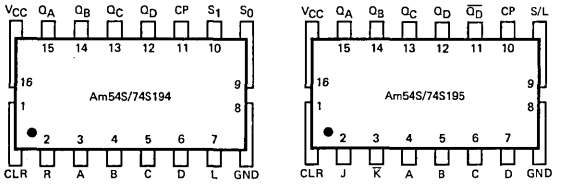
For both devices the outputs change state synchronously following a LOW-to-HIGH transition on the clock input, CP. Both devices have an active-LOW synchronous clear (CLR) which forces all outputs to the LOW state ($\overline{Q}_D$ HIGH) independent of any other inputs. All control inputs are buffered to present only one Schottky TTL load to the system, and all outputs can drive 10 Schottky loads in the LOW state and 20 in the HIGH state. Because all the flip-flops are D-type they do not catch 0's or 1's, and the only requirements on any inputs is that they meet the short set-up and hold time intervals with respect to the clock LOW-to-HIGH transition.

LOGIC SYMBOLS



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
Top Views



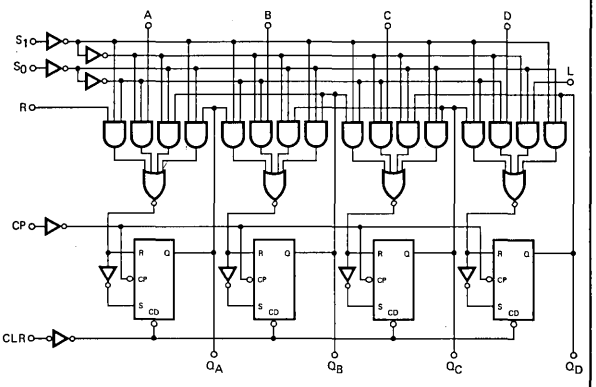
Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

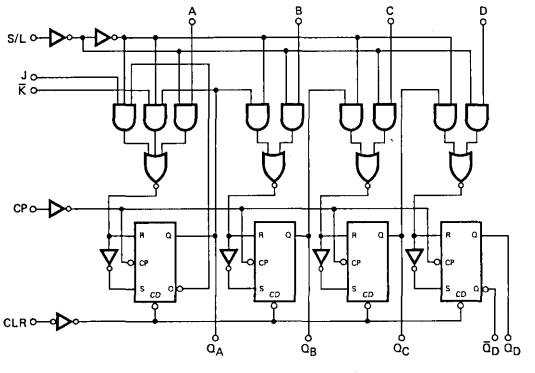
Package Type	Temperature Range	Am54S/74S194 Order Number	Am54S/74S195 Order Number
Molded DIP	0°C to +70°C	SN74S194N	SN74S195N
Hermetic DIP	0°C to +70°C	SN74S194J	SN74S195J
Dice	0°C to +70°C	SN74S194X	SN74S195X
Hermetic DIP	-55°C to +125°C	SN54S194J	SN54S195J
Hermetic Flat Pak	-55°C to +125°C	SN54S194W	SN54S195W
Dice	-55°C to +125°C	SN54S194X	SN54S195X

LOGIC DIAGRAMS

Am54S/74S194



Am54S/74S195



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am74S194, Am74S195 T_A = 0°C to +70°C V_{CC} = 5.0 V ±5% (COM'L) MIN. = 4.75 V MAX. 5.25 V
Am54S194, Am54S195 T_A = −55°C to +125°C V_{CC} = 5.0 V ±10% (MIL) MIN. = 4.5 V MAX. = 5.5 V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1 mA, V_{IN} = V_{IH} or V_{IL}	Am74	2.7	3.4		Volts
			Am54	2.5	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20 mA, V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18 mA				−1.2	Volts
I_{IL} (Note 3)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5 V				−2	mA
I_{IH} (Note 3)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7 V				50	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0 V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.	S194 (Note 5 & 7)		85	135	mA
			54S195 (Note 6)		70	99	
			74S195 (Note 6)		70	109	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Outputs open. Inputs A, B, C, D grounded. Inputs S_0, S_1, Clear, L, R, at 4.5 V. Measured after a momentary ground, then 4.5 V applied to clock
6. Outputs open. S/L grounded. A, B, C, D, J, $\overline{K}$ at 4.5 V. Measured after applying a momentary ground then 4.5 V to the clear followed by groun then 4.5 V to clock.
7. For T_A = 125°C; I_{CC} MAX. = 110 mA for Am54S194W.

Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Clock to Output	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 280 Ω	4	8	12	ns
t_{PHL}	Clock to Output		4	11	16.5	ns
t_{PHL}	Clear to Output			12.5	18.5	ns
t_{pw}	Clock Pulse Width		7			ns
t_{pw}	Clear Pulse Width		12			ns
t_s	Mode Control Set-up Time		8			ns
t_s	Data Input Set-up Time		5			ns
t_s	Clear Recovery to Clock		9			ns
t_h	Data Hold Time		3			ns
t_R	Shift/Load Release Time Am54S/74S195				6	ns
$f_{MAX.}$	Maximum Clock Frequency		70	105		MHz

DEFINITION OF FUNCTIONAL TERMS

J, $\overline{K}$ The logic inputs used for controlling the Q_A flip-flop of the Am54S/74S195 register when S/L is HIGH.

CLR Clear. The asynchronous master reset input.

CP Clock pulse for the register. Enters data on the LOW-to-HIGH transition.

S/L Shift/Load. The input for selection of parallel or serial shifting for the AM54S/74S195 register. S/L LOW selects parallel entry..

S_0, S_1 The mode select inputs of the Am54S/74S194.

A, B, C, D The four parallel data inputs for the register.

R The serial input to the Q_A flip-flop of the Am54S/74S194 in the right shift mode.

L The serial input to the Q_D flip-flop of the Am54S/74S194 in the left shift mode.

Q_A, Q_B, Q_C, Q_D The four true outputs of the register.

$\overline{Q}_D$ The complement output of the Q_D flip-flop. (Am54S/74S195 only).

LOADING RULES (In Unit Loads)

Am54S/74S195 Input/Output	Am54S/74S194 Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
CLR	CLR	1	1	–	–
J	R	2	1	–	–
$\overline{K}$	A	3	1	–	–
A	B	4	1	–	–
B	C	5	1	–	–
C	D	6	1	–	–
D	L	7	1	–	–
GND	GND	8	–	–	–
Shift/Load	S_0	9	1	–	–
CP	S_1	10	1	–	–
$\overline{Q}_D$	–	11	--	20	10
–	CP		1	–	–
Q_D	Q_D	12	--	20	10
Q_C	Q_C	13	--	20	10
Q_B	Q_B	14	--	20	10
Q_A	Q_A	15	--	20	10
V_{CC}	V_{CC}	16	--	–	–

FUNCTION TABLE
Am54S/74S194

FUNCTION	INPUTS Clear	Mode S_1	Mode S_0	Clock	Serial Left	Serial Right	Parallel A	Parallel B	Parallel C	Parallel D	OUTPUTS Q_A	Q_B	Q_C	Q_D
Clear	L	X	X	X	X	X	X	X	X	X	L	L	L	L
No Change	H	X	X	L	X	X	X	X	X	X	NC	NC	NC	NC
	H	X	X	H	X	X	X	X	X	X	NC	NC	NC	NC
Parallel Load	H	H	H	↑	X	X	D_0	D_1	D_2	D_3	D_0	D_1	D_2	D_3
Shift Right	H	L	H	↑	X	L	X	X	X	X	L	Q_A	Q_B	Q_C
	H	L	H	↑	X	H	X	X	X	X	H	Q_A	Q_B	Q_C
Shift Left	H	H	L	↑	L	X	X	X	X	X	Q_B	Q_C	Q_D	L
	H	H	L	↑	H	X	X	X	X	X	Q_B	Q_C	Q_D	H
Hold	H	L	L	X	X	X	X	X	X	X	NC	NC	NC	NC

H = HIGH X = Don't Care
L = LOW NC = No Change
↑ = LOW-to-HIGH transition.
D_i = May be a HIGH or a LOW and the respective output will assume the same state.

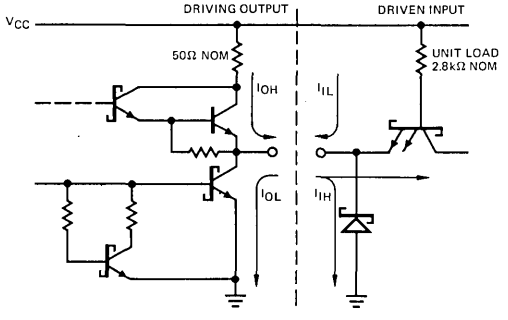
FUNCTION TABLE
Am54S/74S195

INPUTS Clear	Shift/Load	Clock	Serial J	Serial $\overline{K}$	Parallel A	Parallel B	Parallel C	Parallel D	OUTPUTS Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	X	L	X	X	X	X	X	X	NC	NC	NC	NC	NC
H	X	H	X	X	X	X	X	X	NC	NC	NC	NC	NC
H	L	↑	X	X	D_0	D_1	D_2	D_3	D_0	D_1	D_2	D_3	$\overline{D}_3$
H	H	↑	L	H	X	X	X	X	Q_A	Q_A	Q_B	Q_C	$\overline{Q}_C$
H	H	↑	L	L	X	X	X	X	L	Q_A	Q_B	Q_C	$\overline{Q}_C$
H	H	↑	H	H	X	X	X	X	H	Q_A	Q_B	Q_C	$\overline{Q}_C$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_A$	Q_A	Q_B	Q_C	$\overline{Q}_C$

H = HIGH X = Don't Care
L = LOW NC = No Change
↑ = LOW-to-HIGH transition.
D_i = May be a HIGH or a LOW and the respective output will assume the same state.

Notes: 1. If the J and $\overline{K}$ inputs are tied together, the common line becomes a D-Type input to the first bit in the shift mode.
2. Linear feedback shift counters can be made by connecting the Q_D and $\overline{Q}_D$ outputs to the $\overline{K}$ and J inputs, respectively.

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

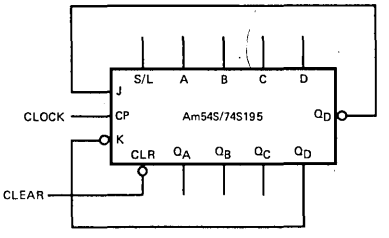


Note: Actual current flow direction shown

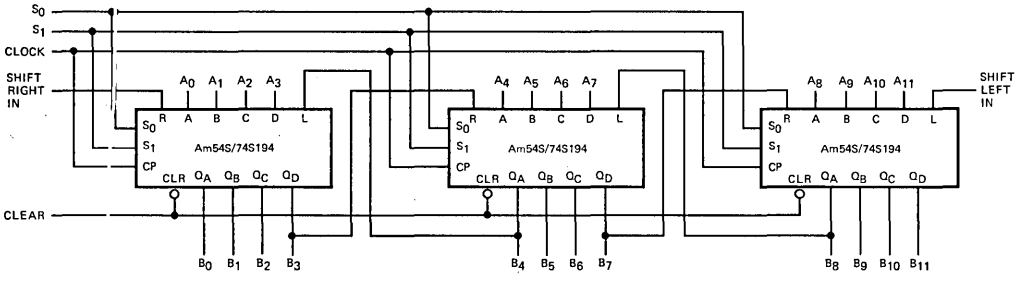
APPLICATIONS

HIGH-SPEED MOD 15 LINEAR FEEDBACK SHIFT REGISTER

Sequence is 0, 1, 2, 5, 10, 4, 9, 3, 6, 13, 11, 7, 14, 12, 8, 0 (15 is non-self correcting; use clear to initialize)

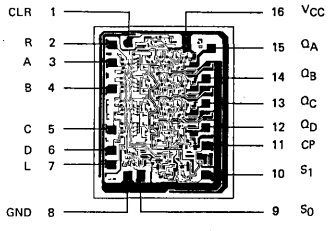


12-BIT SHIFT-LEFT, SHIFT-RIGHT, PARALLEL-LOAD REGISTER



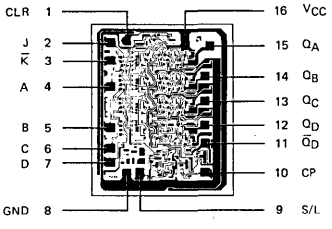
Metallization and Pad Layouts

Am54S/74S194



DIE SIZE 0.071" X 0.088"

Am54S/74S195



DIE SIZE 0.071" X 0.088"

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

f_{MAX} The highest operating clock frequency.

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{PW} Pulse width. The time between the leading and trailing edges of a pulse.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

t_s Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

t_h Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.

t_R Release time. The time interval for which a signal may be indeterminant at one input terminal before an active transition occurs at another input terminal. (The release time falls within the set-up time interval and is specified by some manufacturers as a negative hold time).

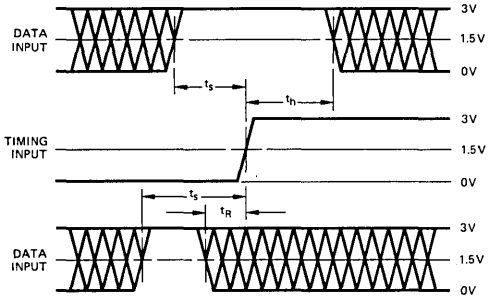
UNIT LOAD DEFINITIONS

	HIGH		LOW	
SERIES	Current	Measure Voltage	Current	Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0 mA	0.5 V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

Note: 1. 54L/74L has two different types of standard inputs.

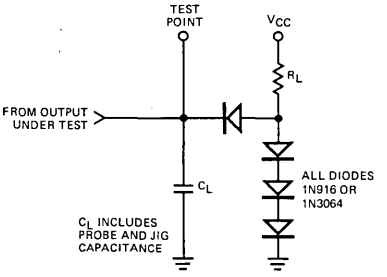
SCHOTTKY PARAMETER MEASUREMENTS
FOR STANDARD ACTIVE-PULLUP TOTEM-POLE OUTPUTS

SET-UP, HOLD, AND RELEASE TIMES

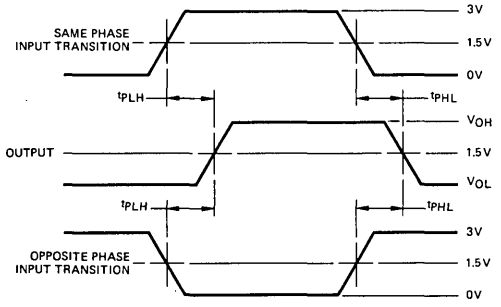


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched area is don't care condition.

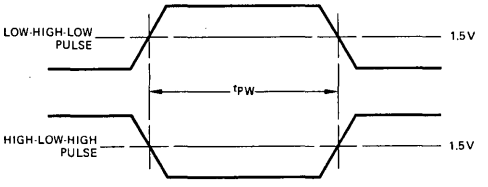
LOAD TEST CIRCUIT



PROPAGATION DELAY

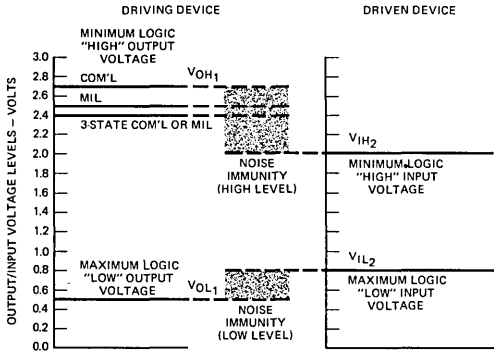


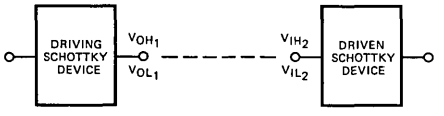
PULSE WIDTH



Notes: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_o = 50\Omega$; $t_r \leq 2.5$ns; $t_f \leq 2.5$ns.

SCHOTTKY INPUT/OUTPUT VOLTAGE INTERFACE CONDITIONS





Note: Refer to Electrical Characteristics for measure currents.

DEFINITION OF STANDARD TERMS

H HIGH, applying to a HIGH voltage level.

L LOW, applying to a LOW voltage level.

I Input.

O Output.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

I_{IL} LOW-level input current with a specified LOW-level voltage applied.

I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.

I_{OL} LOW-level output current.

I_{OH} HIGH-level output current.

I_{SC} Output short-circuit source current.

I_{CC} The supply current drawn by the device from the V_{CC} power supply.

V_{IL} Logic LOW input voltage.

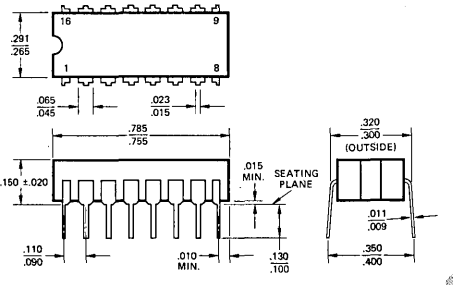
V_{IH} Logic HIGH input voltage.

V_{OL} LOW-level output voltage with I_{OL} applied.

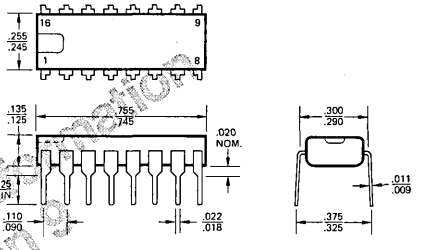
V_{OH} HIGH-level output voltage with I_{OH} applied.

PHYSICAL DIMENSIONS
Dual-In-Line

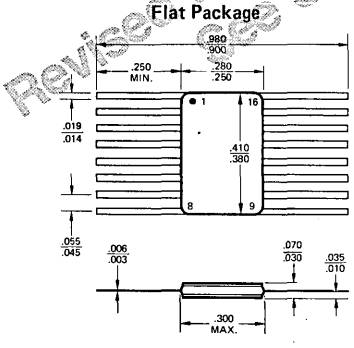
Ceramic



Molded



Flat Package



ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am54S/74S257 • Am54S/74S258

Quadruple 2-Line-To 1-Line Data Selectors/Multiplexers With 3-State Outputs

Distinctive Characteristics

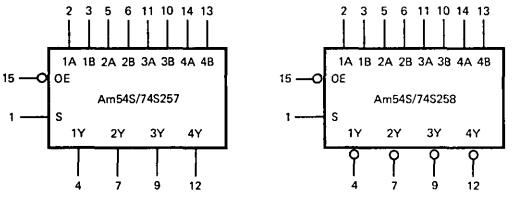
- Three-state outputs interface directly with bus organized systems
- Schottky clamp provides improved AC performance
- Pin assignments identical with Am54S/74S157 and Am54S/74S158
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The 2-line to 1-line data selector multiplexer can be used to transfer data to a common data bus directly by using the three-state capability of the device. With the output control ($\overline{OE}$) HIGH, the four outputs of the data selector are in the high impedance state. With the output control LOW, the selected four bits (A or B inputs) are bussed onto the four data lines.

The typical propagation delay times from data input to output average 4.8ns for the Am54S/74S257 and 4ns for the Am54S/74S258. Also, to minimize the possibility that two outputs will attempt to drive the common bus to opposite logic levels, the output enable circuitry is designed such that the output disable times are shorter than the output enable times.

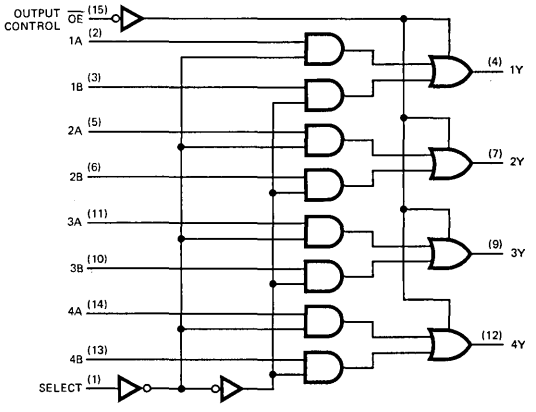
LOGIC SYMBOL



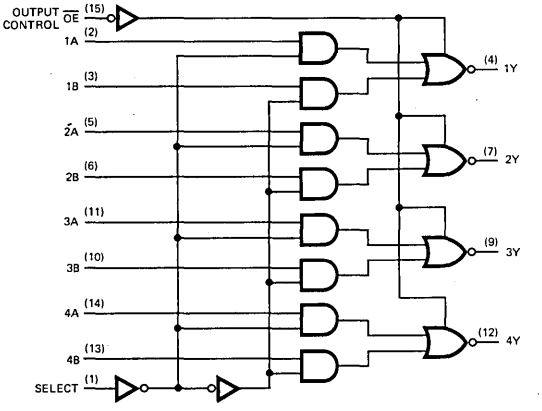
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAMS

Am54S257, Am74S257



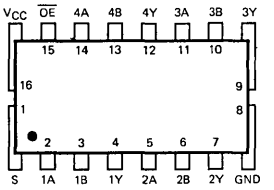
Am54S258, Am74S258



ORDERING INFORMATION

Package Type	Temperature Range	Am54S/74S257 Order Number	Am54S/74S258 Order Number
Molded DIP	0°C to +70°C	SN74S257N	SN74S258N
Hermetic DIP	0°C to +70°C	SN74S257J	SN74S258J
Dice	0°C to +70°C	SN74S257X	SN74S258X
Hermetic DIP	−55°C to +125°C	SN54S257J	SN54S258J
Hermetic Flat Pack	−55°C to +125°C	SN54S257W	SN54S258W
Dice	−55°C to +125°C	SN54S257X	SN54S258X

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am74S257/S258 T_A = 0°C to +70°C V_{CC} = 5.0 V ±5% (Com'l) Min = 4.75 V Max = 5.25 V
Am54S257/S258 T_A = −55°C to +125°C V_{CC} = 5.0 V ±10% (Mil) Min = 4.5 V Max = 5.5 V

Parameters	Description		Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage		V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	54S, I_{OH} = −2mA	2.4	3.4		Volts
				74S, I_{OH} = −6.5mA	2.4	3.2		
V_{OL}	Output LOW Voltage		V_{CC} = MIN., V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 20mA				0.5	Volts
V_{IH}	Input HIGH Level		Guaranteed input logical HIGH voltage for all inputs		2			Volts
V_{IL}	Input LOW Level		Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage		V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL}	Unit Load Input LOW Current	S Input	V_{CC} = MAX., V_{IN} = 0.5V				−4	mA
		Any Other					−2	
I_{IH} (Note 3)	Unit Load Input HIGH Current	S Input	V_{CC} = MAX., V_{IN} = 2.7V				100	µA
		Any Other					50	
I_I	Input HIGH Current		V_{CC} = MAX., V_{IN} = 5.5V				1	mA
I_O	Off-State (HIGH Impedance) Output Current		V_{CC} = MAX.	V_O = 2.4V			50	µA
				V_O = 0.5V			−50	
I_{SC}	Output Short Circuit Current (Note 4)		V_{CC} = MAX., V_{OUT} = 0.0 V		−40		−100	mA
I_{CC}	Power Supply Current	All Outputs HIGH	V_{CC} = MAX: (Note 5)	Am54S/74S257		44	68	mA
				Am54S/74S258		36	56	
		All Outputs LOW		Am54S/74S257		60	93	mA
				Am54S/74S258		52	81	
		All Outputs OFF		Am54S/74S257		64	99	mA
				Am54S/74S258		56	87	

Notes:
1. For conditions shown as MIN. or MAX. use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual Input Currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time and duration of the short circuit test should not exceed one second.
5. I_{CC} is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.

Switching Characteristics (T_A = 25°C)

Parameters	Description		Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Data to Output	S257	V_{CC} = 5 V, R_L = 280 Ω, C_L = 15 pF		5	7.5	ns
		S258			4	6	
t_{PHL}	Data to Output	S257			4.5	6.5	ns
		S258			4	6	
t_{PLH}	Select to Output	S257			8.5	15	ns
		S258			8	12	
t_{PHL}	Select to Output	S257			8.5	15	ns
		S258			7.5	12	
t_{ZH}	Control to Output				13	19.5	ns
t_{ZL}					14	21	
t_{HZ}	Control to Output		V_{CC} = 5 V, R_L = 280 Ω, C_L = 5 pF		5.5	8.5	ns
t_{LZ}					9	14	

FUNCTION TABLE

INPUTS				OUTPUTS	
Output Control	Select	A	B	Am54S/ 74S257	Am54S/ 74S258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = HIGH
L = LOW

X = Don't Care
Z = High Impedance

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH 54S	Fan-out Output HIGH 74S	Fan-out Output LOW
S	1	2	–	–	–
1A	2	1	–	–	–
1B	3	1	–	–	–
1Y	4	–	40	130	10
2A	5	1	–	–	–
2B	6	1	–	–	–
2Y	7	–	40	130	10
GND	8	–	–	–	–
3Y	9	–	40	130	10
3B	10	1	–	–	–
3A	11	1	–	–	–
4Y	12	–	40	130	10
4B	13	1	–	–	–
4A	14	1	–	–	–
$\overline{OE}$	15	1	–	–	–
V_{CC}	16	–	–	–	–

A Schottky TTL Unit Load is defined as 50 μA measured at 2.7 V HIGH and –2.0mA measured at 0.5 V LOW.

FUNCTIONAL TERMS

1A, 2A, 3A, 4A The data inputs for the 4-bits of the A word.

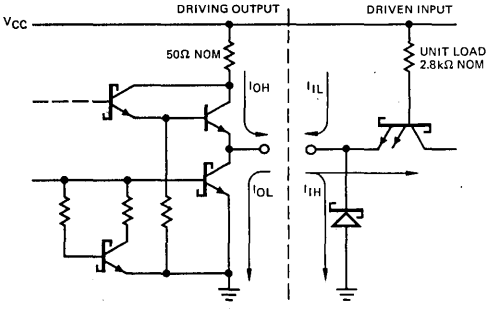
1B, 2B, 3B, 4B The data inputs for the 4-bits of the B word.

1Y, 2Y, 3Y, 4Y The four outputs of the multiplexer.

$\overline{OE}$ Output Control When the output control is HIGH, the four outputs are in the high impedance state. When the output control is LOW, the selected A or B input is present at the output.

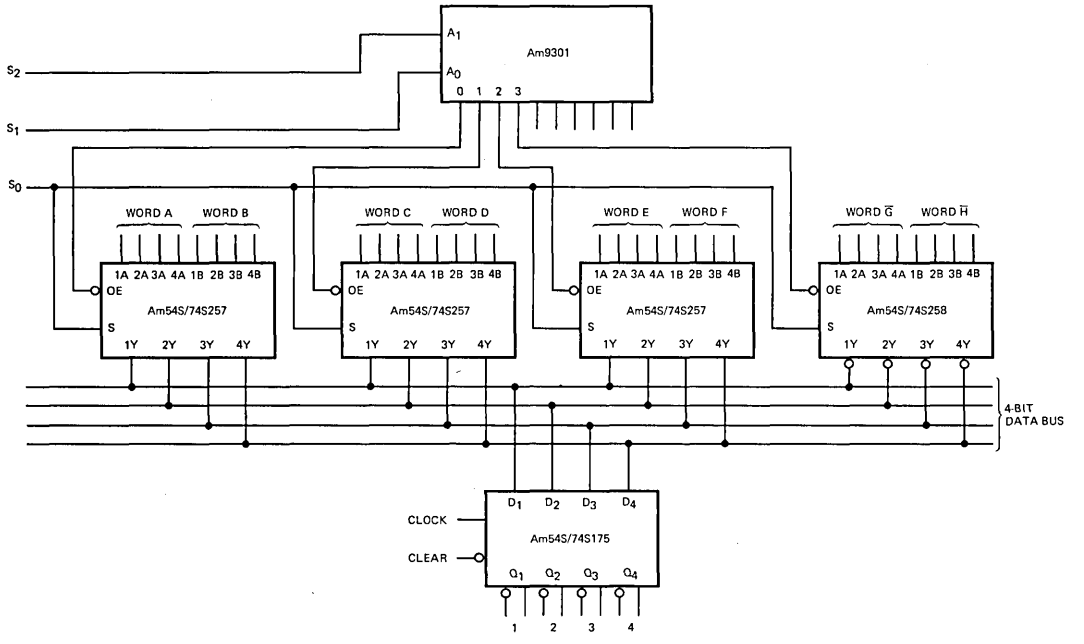
S Select When the select input is LOW, the A word is present at the output. When the select input is HIGH, the B word is present at the output.

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown

APPLICATIONS



8-Word, 4-Bit Multiplexer

APPLICATION BRIEF – THREE STATE OUTPUTS

When a three-state Schottky output is in the high-impedance state, the maximum off-state leakage current is specified as 50μA at 2.4V and −50μA at 0.5V. This leakage loading must be added to the input loading of the devices connected to the data bus for worst-case design. For this reason, the output HIGH source current of the three-state devices are specified with I_{OH} = −2mA for the Am54S series and I_{OH} = −6.5 mA for the Am74S series. The output LOW sink current for all Am54S/74S devices is specified as I_{OL} = 20mA at 0.5V.

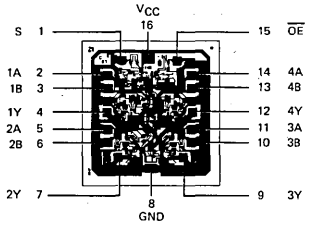
The high current sinking and sourcing capability allows many three-state outputs to be bus-organized and drive several TTL inputs reliably. An example of the I_{OH} and I_{OL} loading calculations is shown in Table I. The important factor for bus-organized three-state outputs is not to exceed either the HIGH-state or the LOW-state maximum loading.

TABLE I

NO. OF LOADING DEVICES ON BUS	TYPE LOAD	DATA BUS HIGH LOAD	DATA BUS LOW LOAD
36	54S/74S outputs Hi-Z	50μA x 36 = 1.8mA	−50μA x 36 = −1.8mA
4	54S/74S inputs	50μA x 4 = .2mA	−2mA x 4 = −8.0mA
		2.0mA	−9.8mA
OUTPUT LOADING USED	Am54S	MAXIMUM	~ 50%
	Am74S	~ 31%	~ 50%

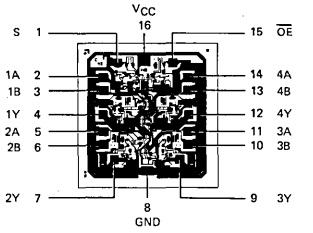
Metallization and Pad Layouts

Am54S/74S257



DIE SIZE 0.065" X 0.069"

Am54S/74S258



DIE SIZE 0.065" X 0.069"

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

f_{MAX} The highest operating clock frequency.

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{PW} Pulse width. The time between the leading and trailing edges of a pulse.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

t_s Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

t_h Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.

t_R Release time. The time interval for which a signal may be indeterminant at one input terminal before an active transition occurs at another input terminal. (The release time falls within the set-up time interval and is specified by some manufacturers as a negative hold time).

t_{HZ} HIGH to disable. The delay time from a control input change to the three-state output HIGH-level to high-impedance transition (measured at 0.5 V change).

t_{LZ} LOW to disable. The delay time from a control input change to the three-state output LOW-level to high-impedance transition (measured at 0.5V change).

t_{ZH} Enable HIGH. The delay time from a control input change to the three-state output high-impedance to HIGH-level transition.

t_{ZL} Enable LOW. The delay time from a control input change to the three-state output high-impedance to LOW-level transition.

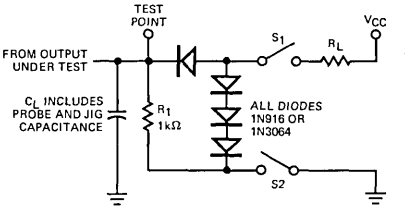
UNIT LOAD DEFINITIONS

SERIES	HIGH Current	HIGH Measure Voltage	LOW Current	LOW Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0 mA	0.5 V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

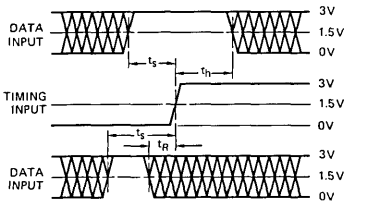
Note: 1. 54L/74L has two different types of standard inputs.

SCHOTTKY PARAMETER MEASUREMENTS
FOR THREE-STATE OUTPUTS

LOAD TEST CIRCUIT

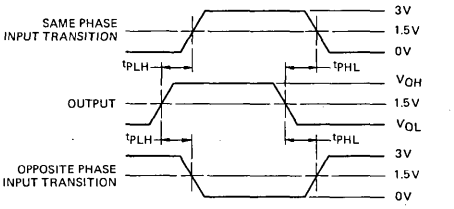


SET-UP, HOLD, AND RELEASE TIMES

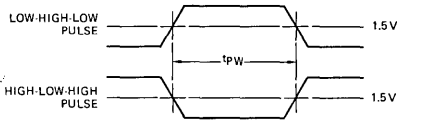


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

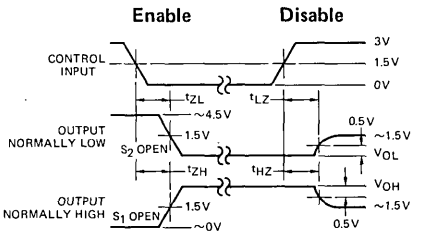
PROPAGATION DELAY



PULSE WIDTH



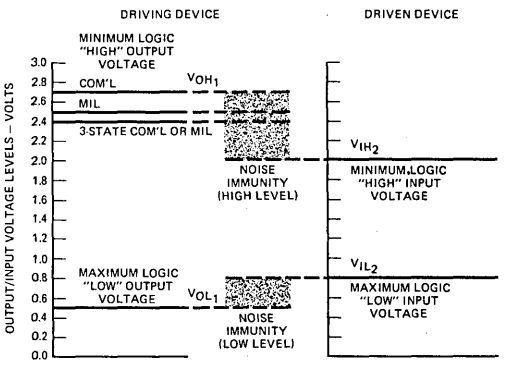
ENABLE AND DISABLE TIMES

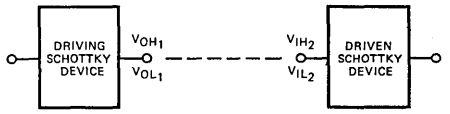


Notes: 1. Diagram shown for Input Control Enable-LOW and Input Control Disable-HIGH.
2. S_1 and S_2 of Load Circuit are closed except where shown.

Note: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_o = 50Ω; t_r ≤ 2.5 ns; t_f ≤ 2.5 ns.

SCHOTTKY INPUT/OUTPUT VOLTAGE INTERFACE CONDITIONS





Note: Refer to Electrical Characteristics for measure current.

DEFINITION OF STANDARD TERMS

H HIGH, applying to a HIGH voltage level.

L LOW, applying to a LOW voltage level.

I Input.

O Output.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

I_{IL} LOW-level input current with a specified LOW-level voltage applied.

I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.

I_{OL} LOW-level output current.

I_{OH} HIGH-level output current.

I_{SC} Output short-circuit source current.

I_{CC} The supply current drawn by the device from the V_{CC} power supply.

V_{IL} Logic LOW input voltage.

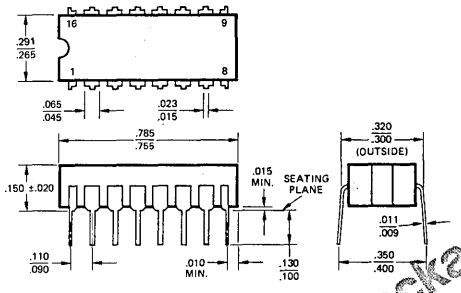
V_{IH} Logic HIGH input voltage.

V_{OL} LOW-level output voltage with I_{OL} applied.

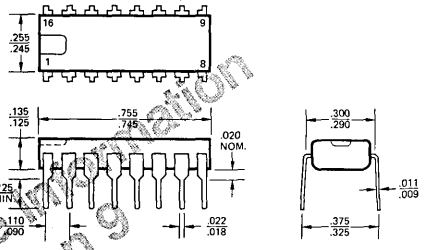
V_{OH} HIGH-level output voltage with I_{OH} applied.

PHYSICAL DIMENSIONS
Dual-In-Line

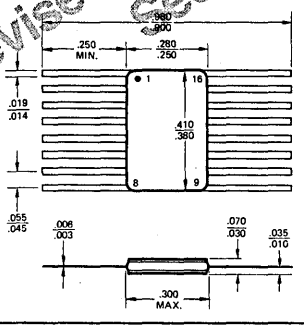
Ceramic



Molded

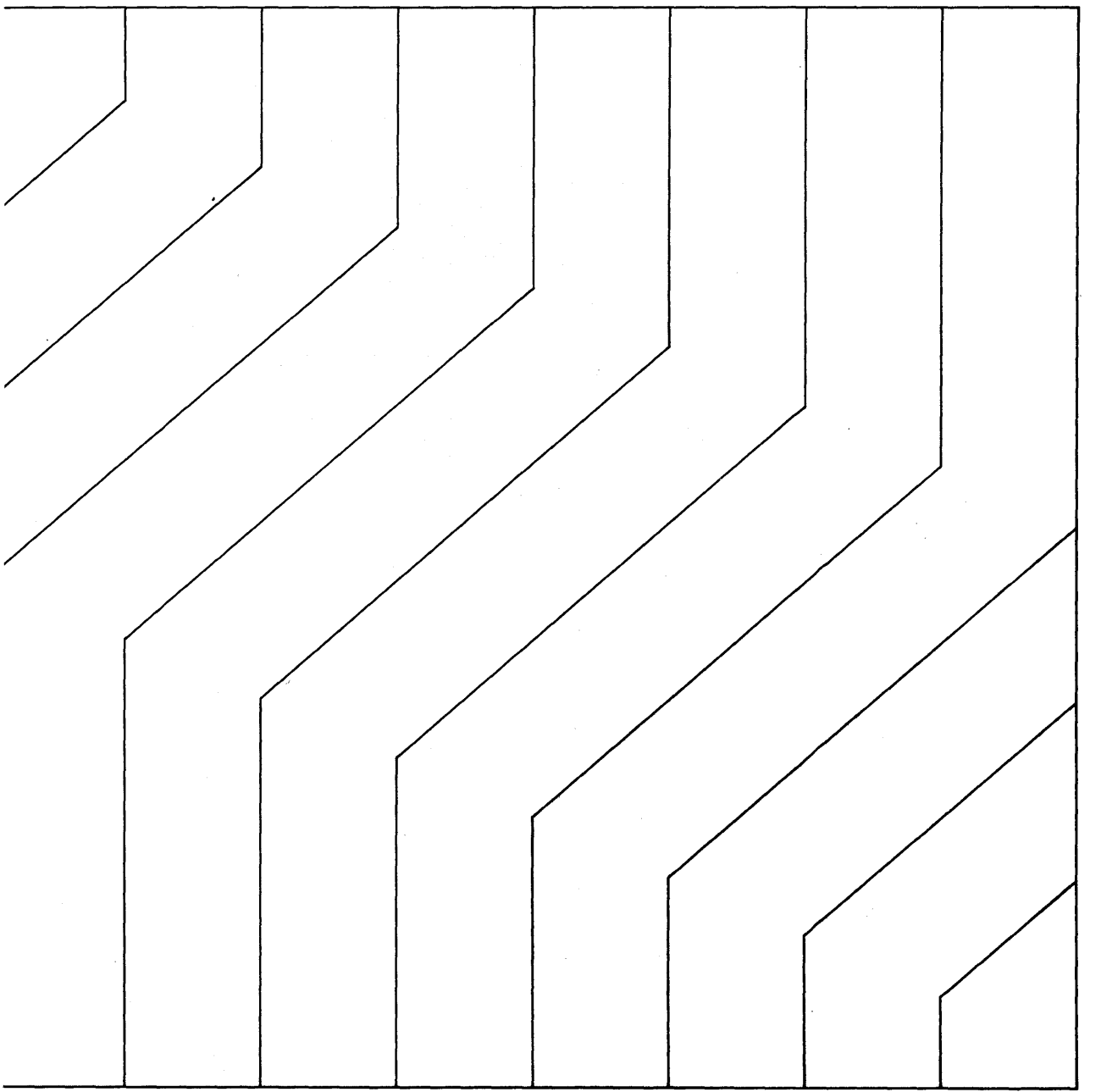


Flat Package



ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Computer Interface



Am0026/Am0026C

5MHz Two-Phase MOS Clock Driver

Distinctive Characteristics

- 20 ns rise and fall times with 1000 pF load
- 20 V output voltage swing
- ±1.5 amps output current drive
- High speed 5 to 10 MHz depending on load
- 100% reliability assurance testing in compliance with MIL-STD-883
- Mixing privileges for obtaining price discounts. Refer to price list.

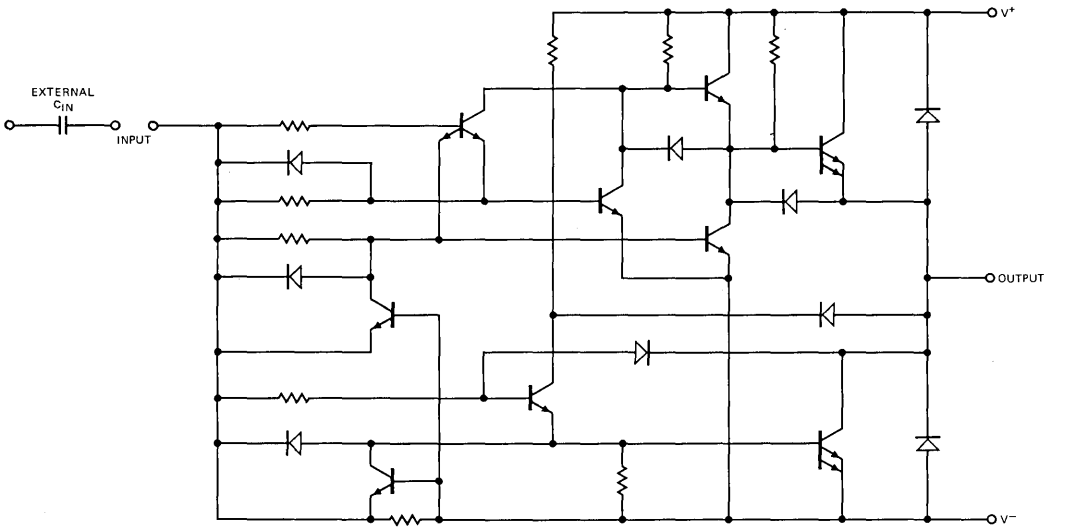
FUNCTIONAL DESCRIPTION

The Am0026 is a dual high speed MOS clock driver and interface circuit. The device is particularly suitable for driving two phase MOS circuits and can provide high speed operation even when driving into high capacitive loads. The device accepts standard TTL/DTL outputs and converts them to MOS logic levels. The output pulse width of the device is determined by the input pulse width.

The Am0026 can operate with a variety of MOS circuits. A popular application is a two-phase clock timer for driving long silicon gate shift registers such as the Am1402/3/4 series. A single clock driver is able to drive 10k bits at 5MHz. The device can also be used with standard dynamic MOS RAMS such as the 1103 to provide address and precharge drive for memories up to 8k by 16-bits.

The device is available in an 8-lead TO-5, one watt copper lead frame 8-pin mini-DIP, a one and one-half watt TO-8 package, and a 14-pin ceramic package.

SCHEMATIC DIAGRAM
(One Driver Shown)

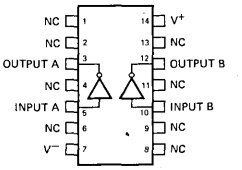


ORDERING INFORMATION

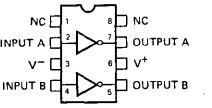
Package Type	Temperature Range	Order Number
8-Pin TO-5	0°C to 85°C	MH0026CH
8-Pin Mini-DIP	0°C to 85°C	MH0026CN
12-Pin TO-8	0°C to 85°C	MH0026CG
14-Pin Ceramic DIP	0°C to 85°C	MMH0026CL
Dice	0°C to 85°C	AM0026XC
8-Pin TO-5	−55°C to +125°C	MH0026H
12-Pin TO-8	−55°C to +125°C	MH0026G
14-Pin Ceramic DIP	−55°C to +125°C	MMH0026L
Dice	−55°C to +125°C	AM0026XM

CONNECTION DIAGRAMS
Top Views

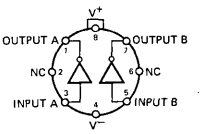
14-Pin Ceramic DIP



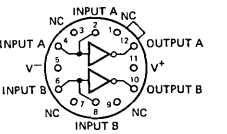
8-Pin Mini DIP



8-Lead TO-5



12-Lead TO-8



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
$V^+ - V^-$ Differential Voltage	22 V
Input Current	100 mA
Input Voltage ($V_{IN} - V^-$)	5.5 V
Peak Output Current	1.5 A
Power Dissipation	See curves

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am0026C T_A = 0°C to 85°C (COM Range) $V^+ - V^-$ = 10 V to 20 V
Am0026 T_A = −55°C to +125°C (MIL Range) Unless Otherwise Specified

Parameter	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V^+ = +5.0 V, V^- = −12.0 V, V_{IN} = −9.5 V		−11.5	−11.0	Volts
		$V_{IN} - V^-$ = 2.5 V		V^- +0.5	V^- +1.0	
V_{OL}	Output LOW Voltage	V^+ = +5.0 V, V^- = −12.0 V, V_{IN} = −11.6 V	4.0	4.3		Volts
		$V_{IN} - V^-$ = 0.4 V	V^+ −1.0	V^+ −0.7		
V_{IH}	Input HIGH Level	$V_{OUT} = V^-$ +1.0 V	2.5	1.5		Volts
V_{IL}	Input LOW Level	$V_{OUT} = V^+$ −1.0 V		0.6	0.4	Volts
I_{IL}	Input LOW Current	$V_{IN} - V^-$ = 0 V, $V_{OUT} = V^+$ −1.0 V		−0.005	−10	μA
I_{IH}	Input HIGH Current	$V_{IN} - V^-$ = 2.5 V, $V_{OUT} = V^-$ +1.0 V		10	15	mA
$I_{CC\ ON}$	"ON" Supply Current	$V^+ - V^-$ = 20 V, $V_{IN} - V^-$ = 2.5 V		30	40	mA
$I_{CC\ OFF}$	"OFF" Supply Current	$V^+ - V^-$ = 20 V, $V_{IN} - V^-$ = 0.0 V		1.0	100	μA

Notes: 1. These specifications apply for $V^+ - V^-$ = 10 V to 20 V, C_L = 1000 pF, over the temperature range −55°C to +125°C for the Am0026 and 0°C to +85°C for the Am0026C.
2. All typical values for T_A = 25°C.

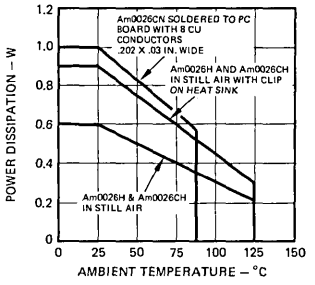
Switching Characteristics (Notes 1 and 2 Above)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PHL}	Turn On Delay		5.0	7.5	12	ns
t_{PLH}	Turn Off Delay		5.0	12	15	ns
t_r	Rise Time (Note 3)	$V^+ - V^-$ = 17 V, C_L = 250 pF		12		ns
		$V^+ - V^-$ = 17 V, C_L = 500 pF		15	18	
		$V^+ - V^-$ = 17 V, C_L = 1000 pF		20	35	
t_f	Fall Time (Note 3)	$V^+ - V^-$ = 17 V, C_L = 250 pF		10		ns
		$V^+ - V^-$ = 17 V, C_L = 500 pF		12	16	
		$V^+ - V^-$ = 17 V, C_L = 1000 pF		17	25	

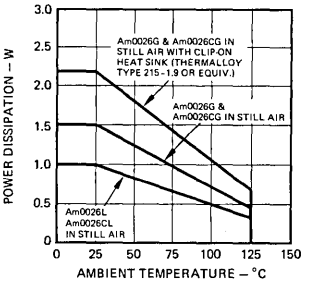
Note: 3. Rise and fall times are given for MOS logic levels; i.e., rise time is transition from logic "0" to logic "1" which is voltage fall. See switching time waveforms.

TYPICAL PERFORMANCE CHARACTERISTICS

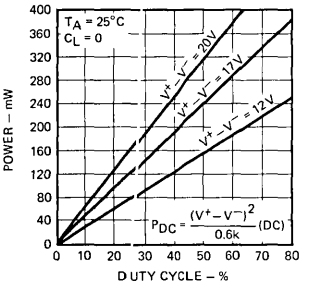
Power Ratings TO-5 & 8-Pin DIP



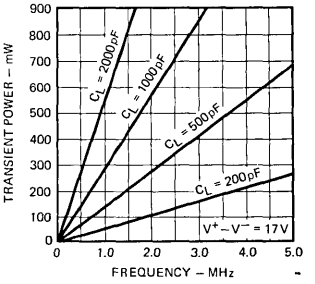
Power Rating TO-8 & 14-Pin DIP



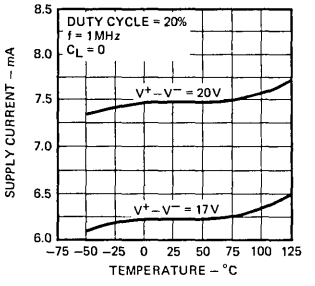
DC Power (P_{DC}) Versus Duty Cycle



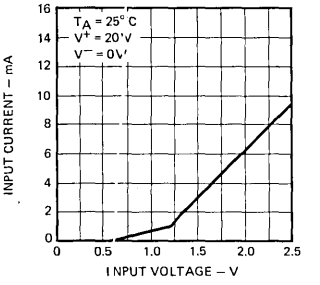
Transient Power (P_{AC}) Versus Frequency



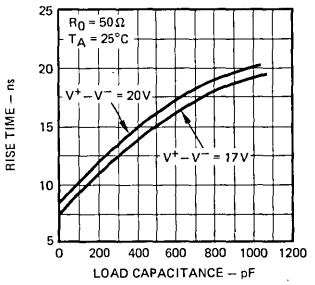
Supply Current Versus Temperature



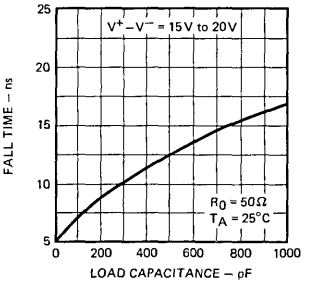
Input Current Versus Input Voltage



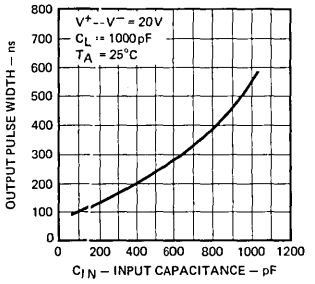
Rise Time Versus Load Capacitance



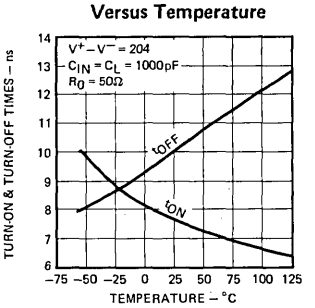
Fall Time Versus Load Capacitance



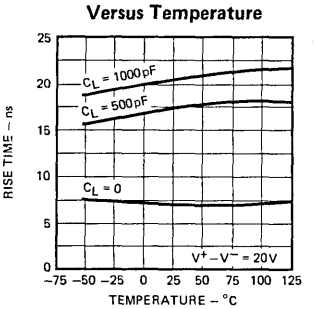
Optimum Input Capacitance Versus Output Pulse Width



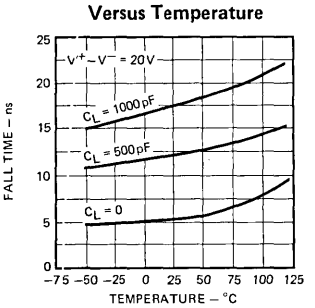
Turn-On & Turn-Off Time Versus Temperature



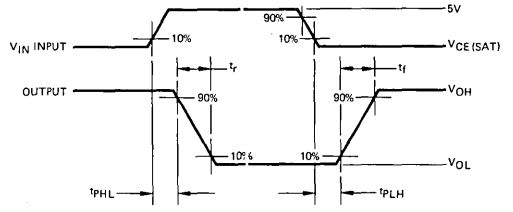
Rise Time Versus Temperature



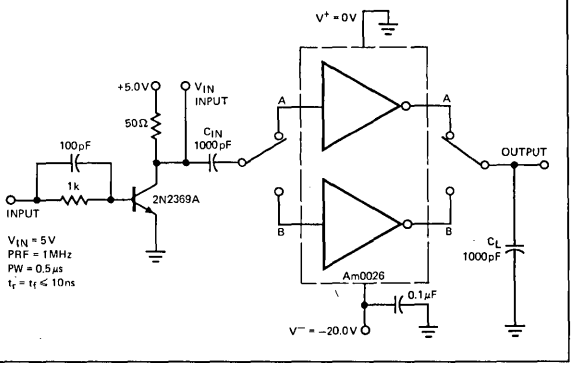
Fall Time Versus Temperature



SWITCHING TIME WAVEFORMS



AC TEST CIRCUIT



APPLICATION INFORMATION

POWER DISSIPATION

The total average power dissipation of the Am0026 is the sum of the DC power and AC transient power. This total must be less than the given package power rating.

$$P_{DISS} = P_{AC} + P_{DC} \leq P_{MAX.}$$

With the device dissipating only 2 mW when the output is at a HIGH voltage (MOS logic "0"), the dominant factor in average DC power is the duty cycle or fraction of the time the output is at a LOW voltage level (MOS logic "1"). For the shift register driving where the duty cycle is less than 25%, P_{DC} is usually negligible. For RAM address line driver applications P_{DC} dominates since duty cycle can exceed 50%.

DC Power per driver:

DC power is given by,

$$P_{DC} = (V^+ - V^-) \times I_{S(LOW)} \times \text{Duty Cycle}$$

where $I_{S(LOW)}$ is $I_{SUPPLY(ON)}$ at $(V^+ - V^-)$

$$I_{SUPPLY(ON)} \text{ is } 40\,mA \times \frac{(V^+ - V^-)}{20\,V} \text{ worst case}$$

$$\text{or } 30\,mA \times \frac{(V^+ - V^-)}{20\,V} \text{ typically}$$

AC transient power per driver:

AC transient power is given by,

$$P_{AC} = (V^+ - V^-)^2 \times C_L \times f \times 10^{-3} \text{ in mW}$$

where f = frequency of operation in MHz and C_L = load capacitance including all strays and wiring in pF.

PACKAGE SELECTION

Power ratings are based on a maximum junction rating of 175°C. The following guidelines are suggested for package selection. Graphs shown in the Performance Curves illustrate derating for various operating temperatures.

TO-5 ("H") Package: Rated at 600 mW in still air (derate at 4.0 mW/°C above 25°C) and rated at 900 mW with clip-on heat sink (derate at 6.0 mW/°C above 25°C). This popular hermetic package is recommended for small systems. Low cost (about 10¢) clip-on-heat sink increases driving power dissipation capability by 50%.

8-pin ("N") Molded Mini-DIP: Rated at 600 mW still air (derate at 4.0 mW/°C above 25°C) and rated at 1.0 watt soldered to PC board (derate at 6.6 mW/°C). Constructed with a special copper lead frame, this package is recommended for medium size commercial systems particularly where automatic insertion is used. (Please note for prototype work, that this package is only rated at 600 mW when mounted in a socket and not one watt until it is soldered down.)

$$C_L \text{ (max.)} = \frac{10^3}{n} \frac{(P_{max.} \text{ Req} - 10^3 (V^+ - V^-)^2 \text{ Duty Cycle})}{\text{Req } (V^+ - V^-)^2 \times f}$$

where n is the number of drivers used in the package.

$P_{max.}$ is the package power rating in milliwatts for given package, heat sink, and maximum ambient temperature.

Req is the equivalent resistance $(V^+ - V^-)/I_{S(LOW)} = 500\Omega$ (worst case over temperature or 600 Ω (typically).

Duty cycle is the fraction of the time that the output signal is in the LOW state.

f is the input signal frequency in MHz.

$C_{L(max.)}$ is the maximum load capacitance per driver in picofarads which can be driven without exceeding device power limits.

When used as a non-overlapping two phase driver with each side operating at the same frequency and duty cycle, and with $(V^+ - V^-) = 17$ V, the above equation simplifies to

$$C_L = \frac{10^3}{f}\left[\frac{P_{max.}}{578} - \text{Duty Cycle}\right]$$

Table I gives maximum drive capability for various system conditions using the above equation.

PULSE WIDTH CONTROL

The Am0026 is intended for applications in which the input pulse width sets the output pulse width; i.e., the output pulse width is logically controlled by the input pulse. The output pulse width is given by:

$$(PW)_{OUT} = (PW)_{IN} + t_r + t_f = PW_{IN} + 25\text{ ns}$$

Two external input coupling capacitors are required to perform the level translation between TTL/DTL and MOS logic levels. Selection of the capacitor size is determined by the desired output pulse width. Minimum delay and optimum performance is attained when the voltage at the input of the Am0026 discharges to just above the devices threshold (about 1.5 V). If the input is allowed to discharge below the threshold, t_r and t_f will be degraded. The graph in the Performance Curves shows optimum values for C_{IN} versus desired output pulse width. The value for C_{IN} may be roughly predicted by:

$$C_{IN} = (2 \times 10^{-3})\ (PW)_{OUT}$$

For an output pulse width of 500 ns, the optimum value for C_{IN} is:

$$C_{IN} = (2 \times 10^{-3})\ (500 \times 10^{-9}) = 1000\text{ pF}$$

RISE AND FALL TIME CONSIDERATIONS (Note 3)

The Am0026's peak output current is limited to 1.5 A. The peak current limitation restricts the maximum load capacitance which the device is capable of driving and is given by:

$$I = C_L \frac{dv}{dt} \leqslant 1.5\ A$$

The rise time, t_r, for various loads may be predicted by:

$$t_r = (\Delta V)\ \ (250 \times 10^{-12} + C_L)$$

Where: ΔV = the change in voltage across C_L

$$\cong V^+ - V^-$$

C_L = The load capacitance

for $V^+ - V^- = 20\ V$, $C_L = 1000\ pF$, t_r is:

$$t_r \cong (20\ V)\ \ (250 \times 10^{-12} + 1000 \times 10^{-12})$$

$$= 25\ ns$$

For small values of C_L, the equation above predicts optimistic values for t_r. The graph in the performance curves shows typical rise times for various load capacitances.

The output fall time (see Graph) may be predicted by:

$$t_f \cong 2.2\ R \left(C_S + \frac{C_L}{h_{FE} + 1} \right)$$

CLOCK OVERSHOOT

The output waveform of the Am0026 can overshoot. The overshoot is due to finite inductance of the clock lines. It occurs on the negative going edge when Q_7 saturates, and on the positive edge when Q_3 turns OFF as the output goes through $V^+ - V_{be}$. The problem can be eliminated by placing a small series resistor in the output of the Am0026. The critical valve for $R_S = 2L\ C_L$ where L is the self-inductance of the clock line. In practice, determination of a value for L is rather difficult. However, R_S is readily determined emperically, and values typically range between 10 and 51Ω. R_S does reduce rise and fall times as given by:

$$t_r = t_r \cong 2.2 R_S\ C_L$$

CLOCK LINE CROSS TALK

At the system level, voltage spikes from ϕ_1 may be transmitted to ϕ_2 (and vice-versa) during the transition of ϕ_1 to MOS logic "1". The spike is due to mutual capacitance between clock lines and is, in general, aggravated by long clock lines when numerous registers are being driven. Transistors Q_3 and Q_4 on the ϕ_2 side of the Am0026 are essentially "OFF" when ϕ_2 is in the MOS logic "0" state since only micro-amperes are drawn from the device. When the spike is coupled to ϕ_2, the output has to drop at least $2\ V_{BE}$ before Q_3 and Q_4 come on and pull the output back to V^+. A simple method for eliminating or minimizing this effect is to add bleed resistors between the Am0026 outputs and ground causing a current of a few milliamps to flow in Q_4. When a spike is coupled to the clock line Q_4 is already "ON" with a finite h_{fe}. The spike is quickly clamped by Q_4. Values for R depend on layout and the number of registers being driven and vary typically between 2 k and 10 kΩ.

POWER SUPPLY DECOUPLING

Adequate power supply decoupling is necessary for satisfactory operation. Decoupling of V^+ to V^- supply lines with at least 0.1 μF noninductive capacitors as close as possible to each Am0026 is strongly recommended. This decoupling is necessary because otherwise 1.5 ampere currents flow during logic transition in order to rapidly charge clock lines.

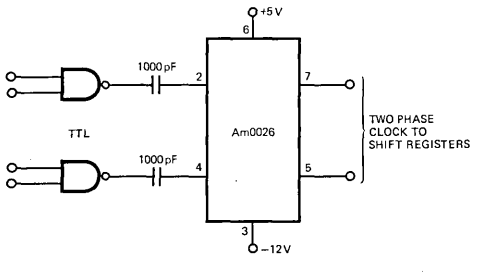
TABLE I – WORST CASE MAXIMUM DRIVE CAPABILITY FOR Am0026*

Package Type		TO-8 with Heat Sink		TO-8 Free Air		Mini-DIP Soldered Down		TO-5 and Mini-DIP Free Air		14-Pin DIP Soldered Down
Max. Operating Frequency	Duty Cycle / Max. Ambient Temp.	60°C	85°C	60°C	85°C	60°C	85°C	60°C	85°C	70°C
100 kHz	5%	30k	24k	19k	15k	13k	10k	7.5k	5.1k	11k
500 kHz	10%	6.5k	5.1k	4.1k	3.2k	2.5k	1.9k	1.4k	1.1k	2k
1 MHz	20%	2.9k	2.2k	1.8k	1.4k	1.1k	840	600	420	860
2 MHz	25%	1.4k	1.1k	850	650	540	400	280	190	390
5 MHz	25%	620	470	380	290	220	160	110	75	165
10 MHz	25%	280	220	170	130	110	79	55	37	90

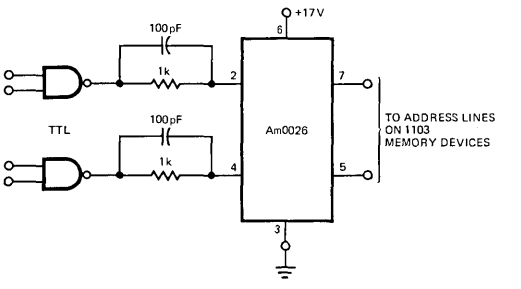
*Note: Values in pF and assume both sides in use as non-overlapping 2 phase driver; each side operating at same frequency and duty cycle with $(V^+ - V^-) = 17\ V$.

TYPICAL APPLICATIONS

AC Coupled MOS Clock Driver

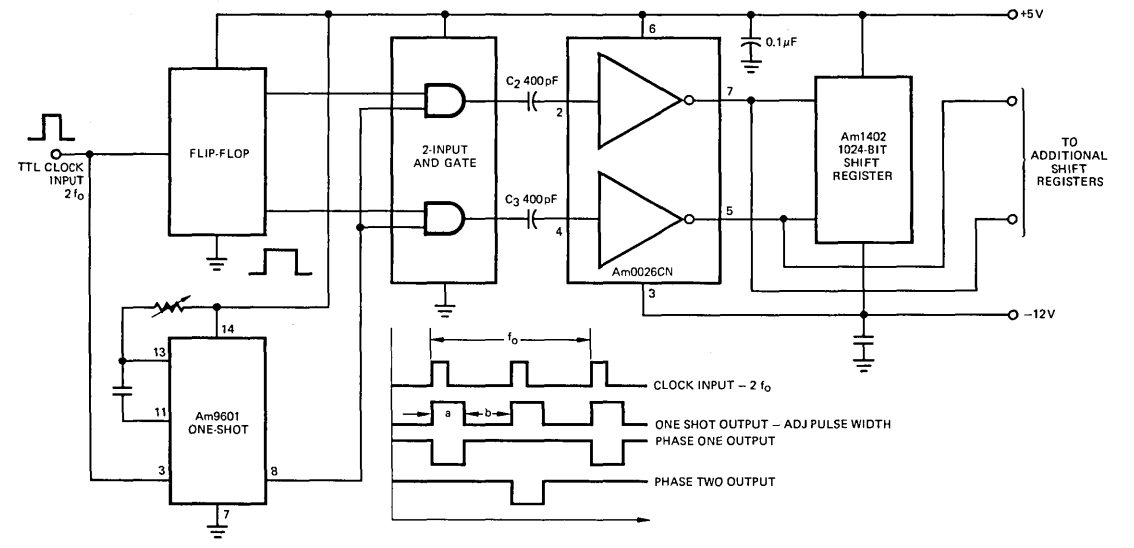


DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)

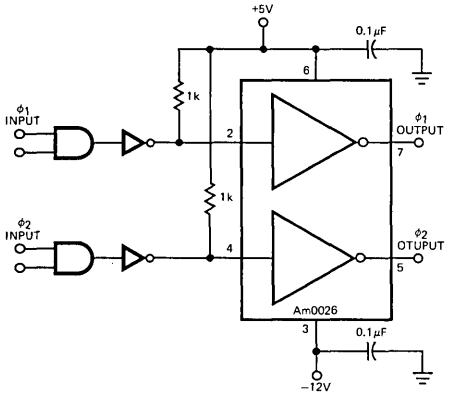


TYPICAL APPLICATIONS (Cont.)

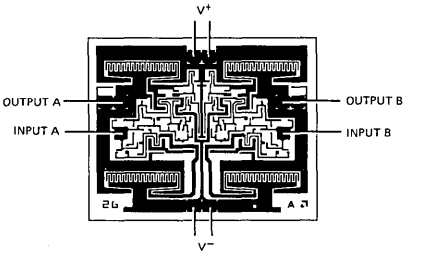
Logically Controlled AC Coupled Clock Driver



DC Coupled MOS Clock Driver



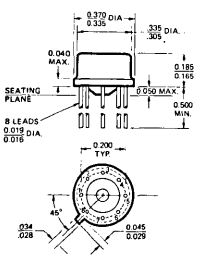
Metallization and Pad Layout



DIE SIZE 0.063" X 0.078"

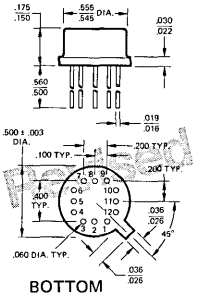
PHYSICAL DIMENSIONS

8-Lead Metal Can (H)



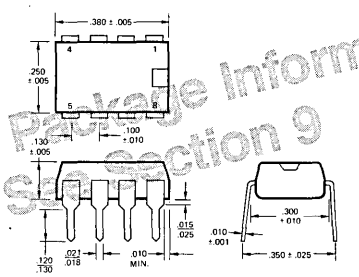
BOTTOM VIEW

12-Lead Metal Can (G)

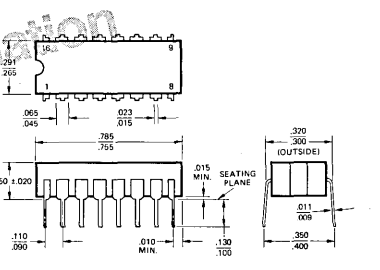


BOTTOM VIEW

8-Pin Molded Mini-Dual-In-Line (N)



14-Pin Ceramic Dual-In-Line (L)



Note: All dimensions in inches.

Am1488
Quad RS-232C Line Driver

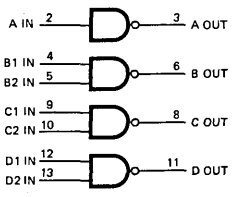
Distinctive Characteristics:

- Conforms to EIA specification RS-232C
- Short circuit protected output
- Simple slew rate control with external capacitor
- 100% reliability assurance testing in compliance with MIL STD 883
- TTL/DTL compatible input

FUNCTIONAL DESCRIPTION

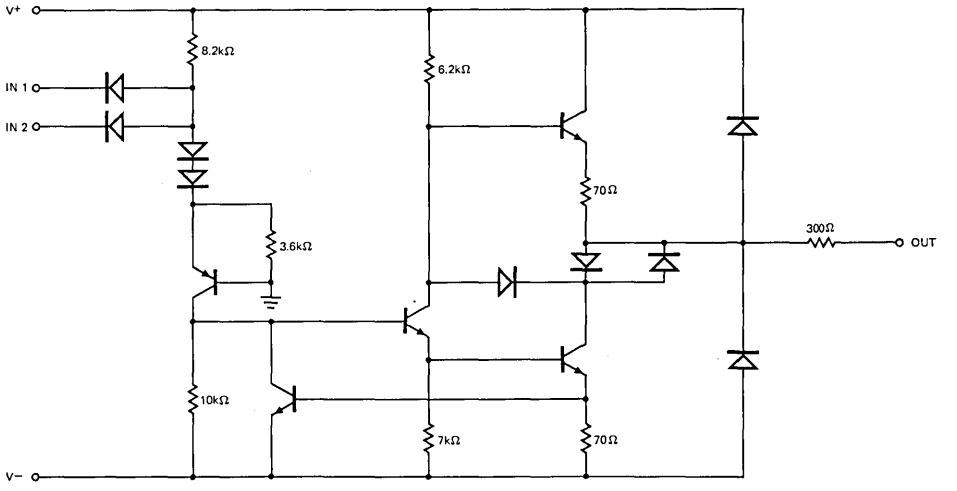
The Am1488 is a quad line driver that conforms to EIA specification RS-232C. Each driver accepts one or two TTL/DTL inputs and produces a high-level logic signal on its output. The HIGH and LOW logic levels on the output are defined by the positive and negative power supplies to the drivers. For power supplies of plus and minus nine volts, the output levels are guaranteed to meet the ±6-volt specification with a 3kΩ load. There is an internal 300Ω resistor in series with the output to provide current limiting in both the HIGH and LOW logic levels. The Am1488 driver is intended for use with the Am1489 or Am1489A quad line receivers.

LOGIC SYMBOL



V⁻ = Pin 1
V⁺ = Pin 14
GND = Pin 7

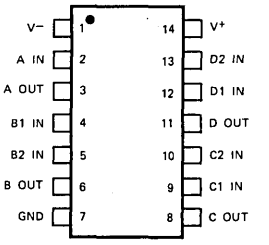
CIRCUIT DIAGRAM
(one driver shown)



Am1488 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
14-pin Hermetic DIP	0°C to +75°C	MC1488L
Dice	0°C to +75°C	AM1488D

CONNECTION DIAGRAM
Top View



NOTE: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +175°C
Temperature (Ambient) Under Bias	0°C to +75°C
Supply Voltage to Ground Potential	V^+ +15V V^- −15V
DC Voltage Applied to Outputs for High Output State	$(V^+ +5.0V) \geq V_o \geq (V^- -5.0V)$
DC Input Voltage	±30V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

T_A = 0°C to +75°C V^+ = +9.0 V V^- = −9.0 V

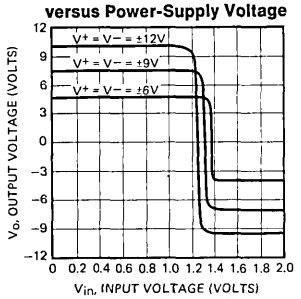
Parameters	Description	Test Conditions		Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	R_L = 3 kΩ V_{IN} = 0.8 V		+6.0	+7.0		Volts
V_{OL}	Output LOW Voltage	R_L = 3 kΩ V_{IN} = 1.9 V			−7.0	−6.0	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage		1.9			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage				0.8	Volts
I_{IL}	Input LOW Current	V_{IN} = 0 V			−1.0	−1.3	mA
I_{IH}	Input HIGH Current	V_{IN} = 5.0 V				10	μA
I_{SC}	Output Short Circuit Current	V_{OUT} = 0.0 V	V_{in} = 0.8 V		−8.0	−10.0	mA
			V_{in} = 1.9 V		+8.0	+12.0	
I_{CC}	Positive Power Supply Current	V_{IN} = 1.9 V	V^+ = 9.0 V		15	20	mA
			V^+ = 12.0 V		19	25	
I_{EE}	Negative Power Supply Current	V_{IN} = 1.9 V	V^- = −9.0 V		−13	−17	
			V^- = −12.0 V		−18	−23	
R_O	Output Resistance	$V^+ = V^- = 0.0$ V, V_{OUT} = ±2.0 V		300			Ω

Switching Characteristics (T_A = 25°C, V^+ = +9.0V, V^- = −9.0V)

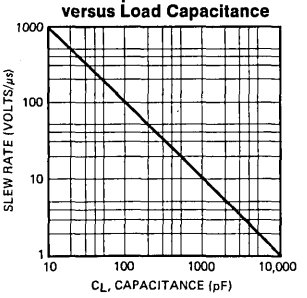
Parameters	Definition	Test Conditions	Min	Typ	Max	Units
t_{pd+}	Delay from input LOW to output HIGH	Z_L = 3.0 kΩ and 15 pF		150	200	ns
t_{pd-}	Delay from input HIGH to output LOW			65	120	ns
t_r	Output rise time			55	100	ns
t_f	Output fall time			45	75	ns

TYPICAL CHARACTERISTICS

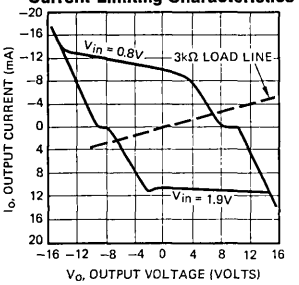
Transfer Characteristics versus Power-Supply Voltage

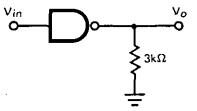


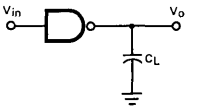
Output Slew Rate versus Load Capacitance

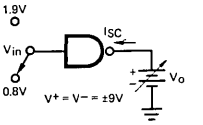


Output Voltage and Current-Limiting Characteristics

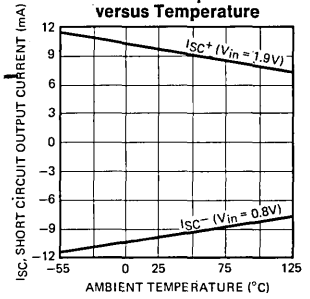




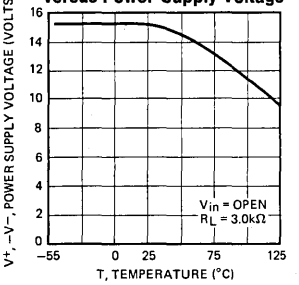




Short-Circuit Output Current versus Temperature



Maximum Operating Temperature versus Power-Supply Voltage



DEFINITION OF TERMS

FUNCTIONAL TERMS

RS-232C A specification of the Electronic Industries Association that defines the electrical characteristics of data signals transmitted between two pieces of digital equipment.

R_L Load resistance. The DC resistance between the driver output and ground.

ELECTRICAL TERMS

V_{OH} Output HIGH voltage. The voltage on the output when the output is HIGH.

V_{OL} Output LOW voltage. The voltage on the output when the output is LOW.

V_{IH} Input HIGH level. The voltage above which the driver is guaranteed to sense a HIGH level.

V_{IL} Input LOW level. The voltage below which the driver is guaranteed to sense a LOW logic level.

I_{IL} Input LOW current. The current that flows out of the input when the input is at a LOW logic level.

I_{IH} Input HIGH current. The current that flows into the input when the input is at a HIGH logic level.

I_{SC} Output short circuit current. The current that flows between the output and ground when the output is shorted to ground and the input is either HIGH or LOW.

I_{CC} The positive power supply current in the V^+ supply.

I_{EE} The negative power supply current in the V^- supply.

Slew Rate The rate, in volts per microsecond at which the output can change from one logic level to another.

SWITCHING TERMS

t_{pd+} The delay from a HIGH-to-LOW transition on an input to a LOW-to-HIGH transition on an output. Measured from the 1.5-volt level on the input to the 0-volt level on the output.

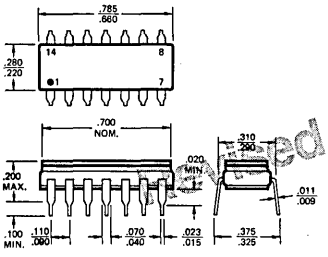
t_{pd-} The delay from a LOW-to-HIGH transition on the input(s) to a HIGH-to-LOW transition on the output. Measured from the 1.5-volt level on the input to the 0-volt level on the output.

t_r Output rise time. The time required for the output to change from 10% of $(V_{OH} - V_{OL})$ to 90% of $(V_{OH} - V_{OL})$, above V_{OL}.

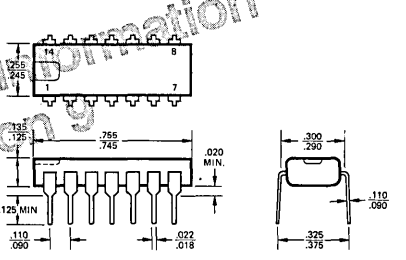
t_f Output fall time. The time required for the output to change from 90% of $(V_{OH} - V_{OL})$ to 10% of $(V_{OH} - V_{OL})$, above V_{OL}.

PHYSICAL DIMENSIONS
Dual-In-Line

Hermetic

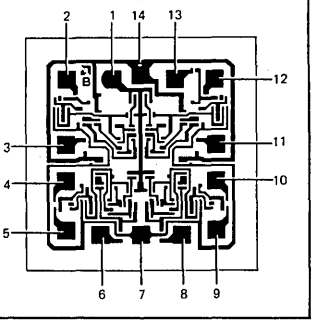


Molded



Metallization and Pad Layout

53 x 54 Mils



ADVANCED MICRO DEVICES INC.
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Sunnyvale
California 94086
(408) 732-2400
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TELEX: 34-6306

Am1489 • Am1489A
Quad RS-232C Line Receivers

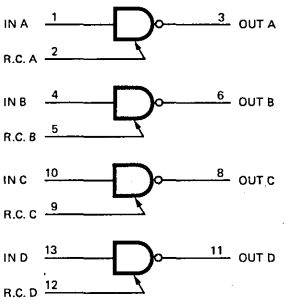
Distinctive Characteristics:

- Compatible with EIA specification RS-232C
- Input signal range ±30 volts
- 100% reliability assurance testing in compliance with MIL STD 883
- Includes response control input and built-in hysterisis

FUNCTIONAL DESCRIPTION:

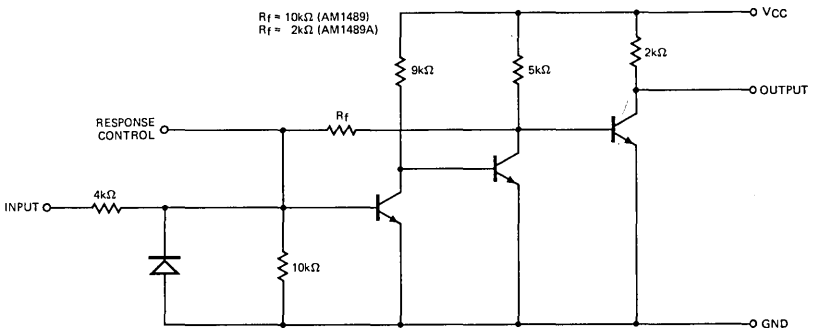
The Am1489 and Am1489A are quad line receivers whose electrical characteristics conform to EIA specification RS-232C. Each receiver has a single data input that can accept signal swings of up to ±30 V. The output of each receiver is TTL/DTL compatible, and includes a 2kΩ resistor pull-up to V_{CC}. An internal feedback resistor causes the input to exhibit hysterisis so that AC noise immunity is maintained at a high level even near the switching thresholds. For both devices, when a receiver is in a LOW state on the output, the input may drop as LOW as 1.25 volts without affecting the output. Both devices are guaranteed to switch to the HIGH state when the input voltage is below 0.75 V. Once the output has switched to the HIGH state, the input may rise to 1.0 V for the Am1489 or 1.75 V for the Am1489A without causing a change in the output. The Am1489 is guaranteed to switch to a LOW output when its input reaches 1.5 V and, the Am1489A is guaranteed to switch to a LOW output when its input reaches 2.25 V. Because of this hysterisis in switching thresholds, the devices can receive signals with superimposed noise or with slow rise and fall times without generating oscillations on the output. The threshold levels may be offset by a constant voltage by applying a DC bias to the response control input. A capacitor added to the response control input will reduce the frequency response of the receiver for applications in the presence of high frequency noise spikes. The companion line driver is the Am1488.

LOGIC SYMBOL



V_{CC} = PIN 14
GND = PIN 7

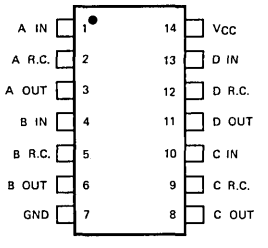
CIRCUIT DIAGRAM
(one receiver)



Am1489/Am1489A ORDERING INFORMATION

Package Type	Temperature Range	Am1489 Order Number	Am1489A Order Number
14-pin Molded DIP	0°C to +75°C	AM1489B	AM1489AB
14-pin Hermetic DIP	0°C to +75°C	MC1489L	MC1489AL
Dice	0°C to +75°C	MC1489D	MC1489AD

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +175°C
Temperature (Ambient) Under Bias	0°C to +75°C
Supply Voltage to Ground Potential (Pin 14 to Pin 7) Continuous	−0.5 V to +10 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
Input Signal Range	−30 V to +30 V
Output Current, Into Outputs	30 mA
DC Input Current	Defined by Input Voltage Limits

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

T_A = 0°C to +75°C V_{CC} = 5.0 V ±1% Response control pin open

Parameters	Description	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −0.5 mA V_{IN} = +0.75 V or open		2.6	4.0		Volts
V_{OL}	Output LOW Voltage	I_{OL} = 10 mA V_{IN} = 1.5 V			0.2	0.45	Volts
V_{IH}	Input HIGH Level Threshold	T_A = 25°C V_{OL} = 0.45 V	Am1489	1.0	1.25	1.5	Volts
			Am1489A	1.75	1.95	2.25	
V_{IL}	Input LOW Level Threshold	T_A = 25°C, V_{OH} = +2.5 V		0.75		1.25	Volts
I_{IL}	Input LOW Current	V_{IN} = −3.0 V		−0.43			mA
		V_{IN} = −25 V		−3.6		−8.3	
I_{IH}	Input HIGH Current	V_{IN} = +3.0 V		0.43			mA
		V_{IN} = +25 V		3.6		8.3	
I_{SC}	Output Short Circuit Current	V_{IN} = 0.0 V V_{OUT} = 0.0 V			3.0		mA
I_{CC}	Power Supply Current	V_{CC} = MAX.			20	26	mA

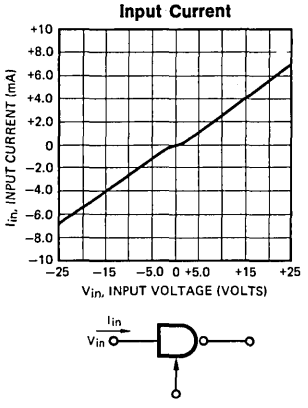
Note: 1) Typical Limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.

Switching Characteristics (T_A = 25°C, response control pin open, C_L = 15 pF)

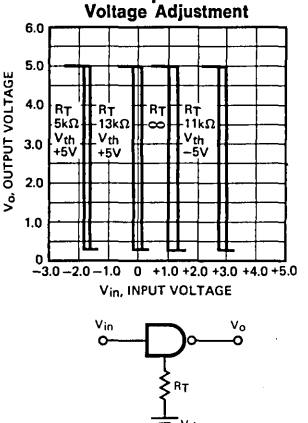
Parameters	Definition	Test Conditions	Min	Typ	Max	Units
t_{pd+}	Delay from Input LOW to Output HIGH	R_L = 3.9 kΩ		25	85	ns
t_{pd-}	Delay from Input HIGH to output LOW	R_L = 390 Ω		25	50	ns
t_r	Output Rise Time (10% to 90%)	R_L = 3.9 kΩ		120	175	ns
t_f	Output Fall Time (90% to 10%)	R_L = 390 Ω		10	20	ns

TYPICAL CHARACTERISTICS

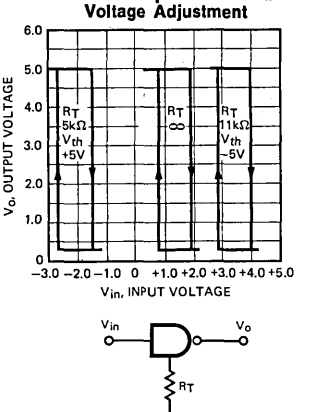
Input Current



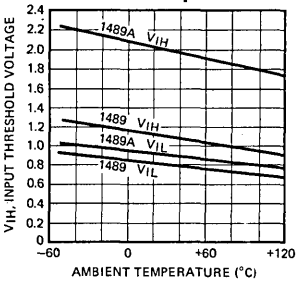
Am1489 Input Threshold Voltage Adjustment



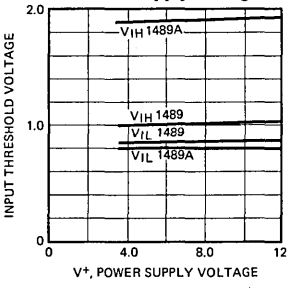
Am1489A Input Threshold Voltage Adjustment



Input Threshold Voltage versus Temperature



Input Threshold versus Power-Supply Voltage



DEFINITION OF TERMS

FUNCTIONAL TERMS

Response Control Pin A pin available on each receiver that allows the user to set the switching thresholds and frequency response of the receiver.

Threshold Voltage The voltage level on the input that will cause the output to change state. Because the device exhibits hysterisis, the LOW level input threshold is different from the HIGH level input threshold. Both thresholds can be moved by applying a bias to the response control pin.

RS-232C A specification of the Electronic Industries Association that defines the electrical characteristics of data signals transmitted between two pieces of digital equipment.

Input Signal Range *The permitted range of DC voltages that can* be applied to the receiver input without damage to the device.

ELECTRICAL TERMS

V_{OH} Output HIGH voltage. The voltage on the output when the output is HIGH.

V_{OL} Output LOW voltage. The voltage on the output when the output is LOW.

V_{IH} Input HIGH threshold. The voltage that must be applied to the input to cause the output to switch from a HIGH to a LOW.

V_{IL} Input LOW threshold. The voltage that must be applied to the input to cause the output to switch from a LOW to a HIGH.

I_{IH} Input HIGH current. The current that will flow into the input when a HIGH level is present on the input.

I_{IL} Input LOW current. The current that will flow out of the input when a LOW logic level is present on the input.

I_{OH} Output HIGH current. The current drawn out of the output when the output is HIGH.

I_{OL} Output LOW current. The current forced into the output when the output is LOW.

I_{SC} Output Short Circuit Current. The current that flows out of the output when the output and input are both grounded.

I_{CC} Current drawn from the V_{CC} power supply.

SWITCHING TERMS

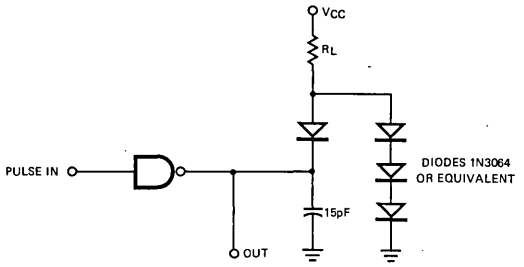
t_{pd+} The delay from a HIGH-to-LOW transition on the input to a LOW-to-HIGH transition on the output. Times are measured from the 1.5-volt levels on both pins.

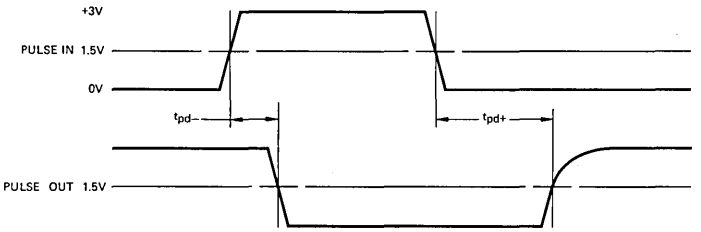
t_{pd-} The delay from a LOW-to-HIGH transition on the input to a HIGH-to-LOW transition on the output. Times are measured from the 1.5-volt level on both pins.

t_r Rise Time. The time required for the output to rise from 10% of the difference between V_{OL} and V_{OH} above V_{OL} to 90% of the difference between V_{OL} and V_{OH} above V_{OL}.

t_f Fall Time. The time required for the output to fall from 90% of the difference between V_{OL} and V_{OH} above V_{OL} to 10% of the difference between V_{OL} and V_{OH} above V_{OL}.

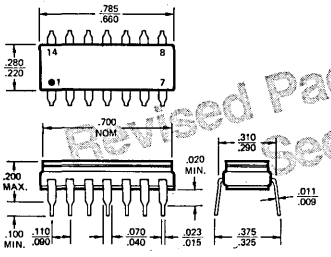
SWITCHING TIME TEST CIRCUIT & WAVEFORMS



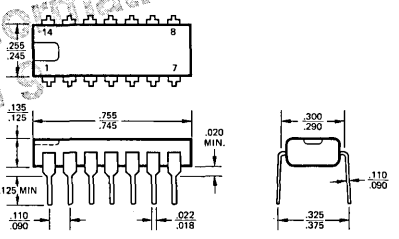


PHYSICAL DIMENSIONS
Dual-In-Line

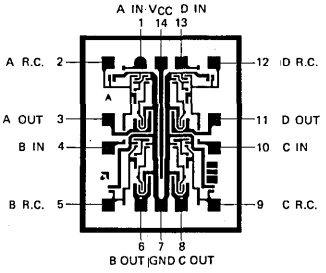
Hermetic



Molded



Metalization and Pad Layout



DIE SIZE 0.047" X 0.059"

ADVANCED
MICRO
DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am2600/9600/9601
Retriggerable Monostable Multivibrators

Distinctive Characteristics:

- Retriggerable 0 to 100% duty cycle.
- 50ns to ∞ output pulse width range.
- Am2600 guaranteed pulse width change of less than 1% over 0°C to +75°C temperature range.
- 100% reliability assurance testing including high temperature bake, temperature cycling, centrifuge and package hermeticity testing in compliance with MIL-STD-883.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.
- Mixing privileges for obtaining price discounts. Refer to price list.

FUNCTIONAL DESCRIPTION

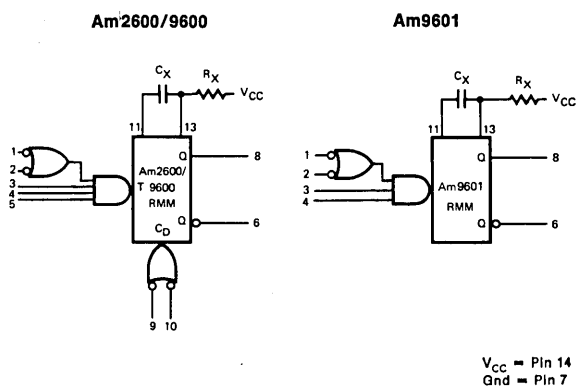
The Am2600, Am9600 and Am9601 are DC-level sensitive retriggerable monostable multivibrators which provide an output pulse whose duration and accuracy depend on external timing components.

Provision is made for triggering on the rising or falling edge of an input signal. All inputs are DC coupled making triggering independent of input rise and fall times. Each time the output of the logic network at the trigger input goes from a FALSE (LOW) condition to a TRUE (HIGH) condition triggering occurs independent of the state of the monostable.

The AM 2600 and 9600 are the equivalent of the 9601 with an additional active HIGH input and an active LOW reset facility. When a $\overline{C}_D$ input on the Am 2600 or 9600 goes LOW the multivibrator resets independent of its present state or input conditions.

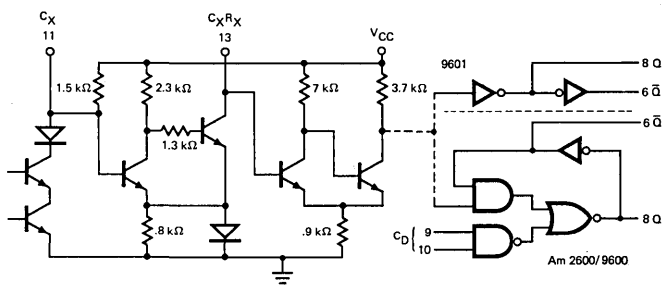
The Am2600 is a selected Am9600 with a guaranteed pulse width change of less than 1% over the temperature range 0°C to +75°C.

LOGIC DIAGRAMS



V_{CC} = Pin 14
Gnd = Pin 7

INTERNAL TIMING CIRCUITRY

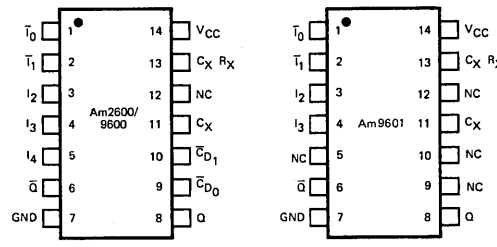


ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am2600	Molded DIP	0°C to +75°C	AM260059B
Am2600	Hermetic DIP	0°C to +75°C	AM260059F
Am2600	Hermetic DIP	−55°C to +125°C	AM260051F
Am2600	Hermetic Flat Pak	−55°C to +125°C	AM260051M
Am2600	Dice	Note	AM2600XXD
Am9600	Molded DIP	0°C to +75°C	U6E960059X
Am9600	Hermetic DIP	0°C to +75°C	U6A960059X
Am9600	Hermetic DIP	−55°C to +125°C	U6A960051X
Am9600	Hermetic Flat Pak	−55°C to +125°C	U3I960051X
Am9600	Dice	Note	UXX9600XXD
Am9601	Molded DIP	0°C to +75°C	U6E960159X
Am9601	Hermetic DIP	0°C to +75°C	U6A960159X
Am9601	Hermetic DIP	−55°C to +125°C	U6A960151X
Am9601	Hermetic Flat Pak	−55°C to +125°C	U3I960151X
Am9601	Dice	Note	UXX9601XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAMS
Top View



NC = No connection

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 14 to Pin 7) Continuous	−0.5 V to +8 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs LOW	50 mA
DC Input Current	−30 mA to +5 mA

ELECTRICAL CHARACTERISTICS

Am260059/960059X/960159X T_A = 0°C to +75°C (COM grade)
Am260051/960051X/960151X T_A = −55°C to +125°C (MIL grade)

Parameters	Operating Range	Test Conditions		LIMITS T_A = MIN Min	Max	T_A = +25°C Min	Typ	Max	T_A = MAX Min	Max	Units
V_{OH} Output HIGH Voltage	MIL or COM	V_{CC} = MIN., I_{OH} = −0.96 mA		2.40		2.40	3.6		2.40		Volts
V_{OL} Output LOW Voltage	MIL	I_{OL} = 8 x I_{IL} MAX.			0.40		0.2	0.40		0.40	Volts
	COM	I_{OL} = 8 x I_{IL} MAX.			0.45		0.2	0.45		0.45	
V_{IH} Input HIGH Voltage	MIL			2.00		1.70			1.50		Volts
	COM			1.90		1.80			1.60		
V_{IL} Input LOW Voltage	MIL				0.85			0.90		0.85	Volts
	COM				0.85			0.85		0.85	
I_{IL} Input Load Current	MIL	V_{IN} = 0.40 V	V_{CC} = MAX.		−1.60		−1.10	−1.60		−1.60	mA
			V_{CC} = MIN.		−1.24		−0.97	−1.24		−1.24	
	COM	V_{IN} = 0.45 V	V_{CC} = MAX.		−1.60		−1.00	−1.60		−1.60	
			V_{CC} = MIN.		−1.41		−0.90	−1.41		−1.41	
I_{IH} Reverse Input Current	MIL or COM	V_{CC} = MAX., V_{IN} = 4.5 V			60		2	60		60	µA
I_{SC} Short Circuit Current	MIL	V_{CC} = 5.0 V, V_O = 1.0 V	−9600, 2600			−10		−25			mA
	COM		V_O = 0.0V −9601			−10		−35			
I_{PD} Power Supply Current	2600 MIL / 9600 COM	V_{CC} = 5.0 V R_X = 10 kΩ			24		19	24		24	mA
					26		19	26		26	
	9601	V_{CC} = MAX. GND Pin 11 R_X = 10 kΩ			25		19	25		25	

Switching Characteristics (T_A = 25°C unless otherwise specified)

Parameters			Test Conditions	Am 2600/9601 Min	Typ	Max	Am9600 Min	Typ	Max	Units
t_{pd+}	Turn Off Delay Negative Trigger Input to True Output		V_{CC} = 5.0 V, C_L = 15 pF R_X = 5 kΩ, C_X = 0 pF		25	40		27	45	ns
t_{pd-}	Turn On Delay Negative Trigger Input to False Output				25	40		27	40	ns
$t_{pw(min)}$	Minimum Output Pulse Width	True (Q) Output	V_{CC} = 5.0 V, C_L = 15 pF R_X = 5 kΩ, C_X = 0 pF		45	65		50	70	ns
		False ($\overline{Q}$) Output			55	75		60	80	
t_{pw}	Output Pulse Width Variation	Mil	V_{CC} = 5.0 V, C_L = 15 pF R_X = 10 kΩ, C_X = 1000 pF	3.08	3.42	3.76	3.20	3.42	3.76	µs
		Com		3.08	3.42	3.76	3.08	3.42	3.76	
C_{STRAY}	Maximum Allowable Wiring Capacitance to Ground		Pin 13 = GND			50			50	pF
R_X	Timing Resistor over temperature range (Note 5)			5		50	5		50	kΩ
t_{pd-} ($\overline{C_D}$)	Delay from $\overline{C_D}$ to Q output LOW				11	17		11	17	ns

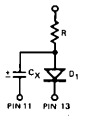
	Am 2600		Min	Typ	Max	
$\Delta t_{pw}(T)$	Maximum Output Pulse Width Percentage Change over temperature range 0°C to +75°C	V_{CC} = 5.0 V, C_L = 15 pF R_X = 10 kΩ, C_X = 1000 pF		0.5	1.0	%

Note 1. Maximum current defined by DC Input Voltage.
2. Pulse tested.
3. Unless otherwise noted, tests are conducted with a 10 kΩ resistor from V_{CC} to Pin 13 (R_X).
4. Limit for −55°C to +125°C operation is 25 kΩ.

OPERATION RULES

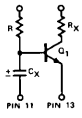
1. An external resistor R_X and an external capacitor C_X are required as shown in the logic diagram. The values of R_X may vary from 5.0 kΩ to 50 kΩ for 0°C to +75°C operation and 5.0 kΩ to 25 kΩ for −55°C to +125°C operation. C_X may vary from 0 to any value necessary and obtainable.
2. If a fixed value of R_X is used, the following values are recommended: R_X = 30 kΩ for 0°C to +75°C operation; R_X = 10 kΩ for −55°C to +125°C operation.
3. The output pulse width T is defined as follows:

   $T = 0.32\ R_X C_X\ [1 + \frac{0.7}{R_X}]$ (For C_X greater than 10^3 pF) Where: R_X is in kΩ, C_X is in pF, T is in ns. For $C_X < 10^3$ pF see Fig. 12.
4. If electrolytic type capacitors are to be used, it is recommended that they have low leakage. For capacitors with a high reverse leakage the following circuits can be used:



$R < 0.6\ R_X$ (Max)

D_1: any silicon type diode, such as FD700



This circuit also allows larger value of R to be used for longer output pulse width.

$R < R_X\ (0.7)\ (h_{FE}Q_1)$

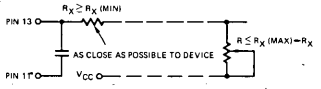
R_X (min) < R_X < R_X (max)

Q_1: Any NPN silicon device with sufficient h_{FE} at low currents, such as 2N2511

Both circuits prevent reverse voltage across C_X. The pulse width T for the circuits is defined as follows:

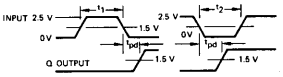
$T \approx 0.30\ RC_X\ [1 + \frac{0.7}{R}]$ Where: R is in kΩ, C_X is in pF, T is in ns.

5. To obtain variable pulse width, by remote trimming, the following circuit is recommended:

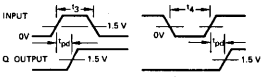


6. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
7. Input Trigger Pulse Rules. $t_1, t_2, t_3, t_4 > 40$ ns

Input to Pin 1
Pins 2, (1), 4 & 5 =High



Input to Pin 3 (4)(5)
Pin 4 (3)(5)=High Pins 1 or 2 =Low



8. The retriggerable pulse width is calculated as shown below:

$t_w = t_{pw} + t_{pd+} = 0.32\ R_X C_X\ (1 + \frac{0.7}{R_X}) + t_{pd+}$

The retrigger pulse width is equal to the pulse width t_{pw} plus a delay time. For pulse widths greater than 500 ns, t_w can be approximated as t_{pw}.

NOTE: Retriggering will not occur if the retrigger pulse comes within $0.32\ R_X C_X\ (\frac{0.7}{R_X})$ ns after the initial trigger pulse.

9. Reset Operation — The Am2600/9600 have an active LOW reset facility. By applying a low to either reset input, any timing cycle can be terminated or any new cycle inhibited until the low reset input is removed. Trigger inputs will not produce spikes in the output when a reset is held low.

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS:

$\overline{CD}_0$, $\overline{CD}_1$ The asychronous direct clear inputs of the 9600. A LOW on either of these inputs will reset the monostable independent of other conditions.

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

$\overline{I}_0$, $\overline{I}_1$ The active LOW inputs of the Am2600/9600/9601. With all other inputs HIGH a HIGH to LOW transition on either of these inputs will cause triggering.

I_2, I_3, I_4 The active HIGH inputs of the Am2600/9600/9601 with either $\overline{I}_0$ or $\overline{I}_1$ inputs LOW a LOW to HIGH transition on any input I_2, I_3, I_4 with the remaining inputs HIGH will cause triggering.

Input Unit Load One T^2L gate input load. In the HIGH state it is equal to I_R and in the LOW state it is equal to I_F.

Q The TRUE output of the monostable.

$\overline{Q}$ The FALSE output of the monostable.

Triggering The switching of the monostable from the stable state to the unstable state and start of the timing cycle.

SWITCHING TERMS:

t_{pd+} The propagation delay from a HIGH to LOW transition on $\overline{I}_0$ or $\overline{I}_1$ to the TRUE (Q) output LOW to HIGH transition.

t_{pd-} The propagation delay from a HIGH to LOW transition on $\overline{I}_0$ or $\overline{I}_1$ to the FALSE ($\overline{Q}$) output HIGH to LOW transition.

$t_{pw\ (min)}$ The minimum TRUE (Q) output pulse width with C_X = 0 pF, R_X = 5 kΩ.

Δt_{pw} The output pulse width variation with C_X=1000 pF, R_X=10 kΩ.

Δt_{pw} (T) The Am2600 maximum pulse width percentage change over the temperature range 0°C to +75°C of the TRUE (Q) output from the pulse width at 25°C.

OPERATIONAL TERMS:

I_{IL} Forward input load current, for unit input load.

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{IH} Reverse input load current with V_R applied to input.

I_{SC} Output current when output set to V_{OH} condition but forced low.

Negative Current Current flowing out of the device.

P_{DISS} The power dissipated within the circuit with input and output terminals open.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage. Refer to figure 14.

V_{IL} Maximum logic LOW input voltage. Refer to figure 14.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

PERFORMANCE CURVES

Input Characteristics

Input Load Current Versus Input Voltage

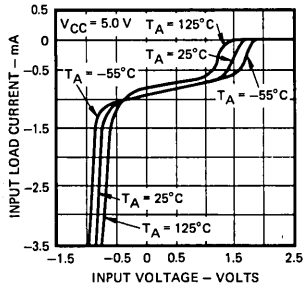


Figure 1

Input Leakage Current Versus Input Voltage

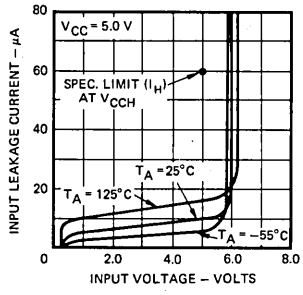


Figure 2

Power Dissipation

Power Dissipation Versus Ambient Temperature

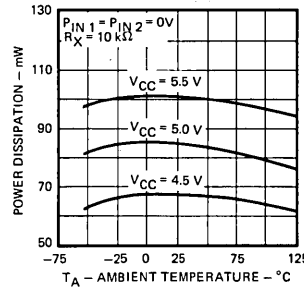


Figure 3

Output Characteristics

Output Current Versus Output Voltage (High State)

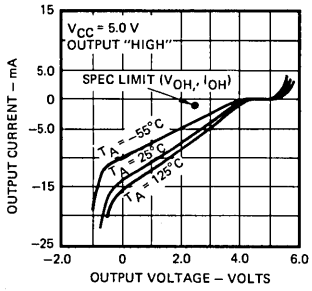


Figure 4

Output Current Versus Output Voltage (Low State)

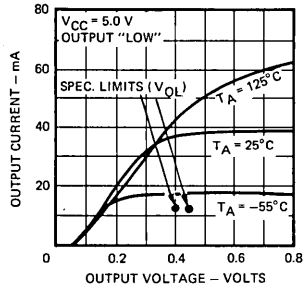


Figure 5

Switching Characteristics

Typical Negative Trigger Delay Time Versus Ambient Temperature

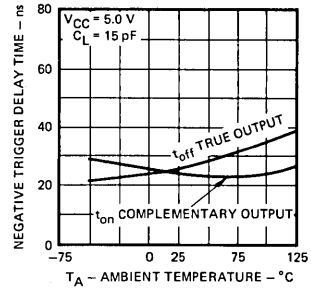


Figure 6

Pulse Width Characteristics

Normalized Output Pulse Width Versus Ambient Temperature

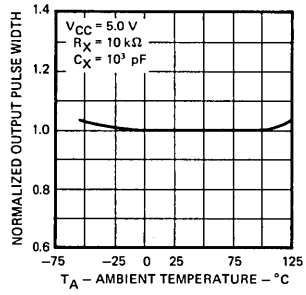


Figure 7

Normalized Output Pulse Width Versus Supply Voltage

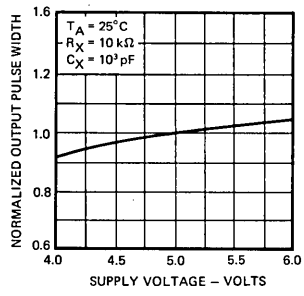


Figure 8

Normalized Output Pulse Width Versus Operating Duty Cycle

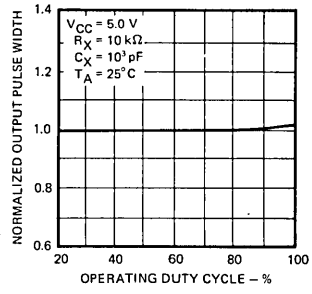


Figure 9

Pulse Width Versus Timing Resistance

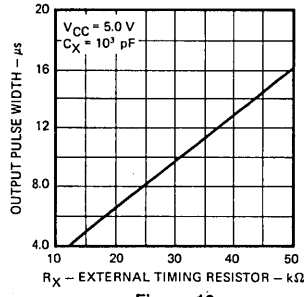


Figure 10

Typical Output Pulse Width Versus Ambient Temperature

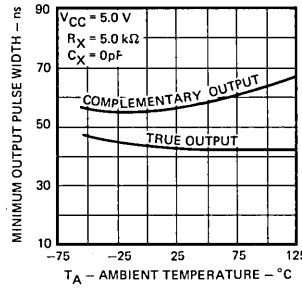


Figure 11

Output Pulse Width Versus Timing Resistance and Capacitance

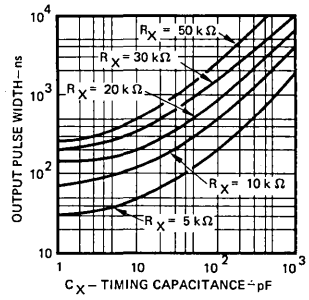


Figure 12

Am 2600 Normalized Output Pulse Width Versus Ambient Temperature

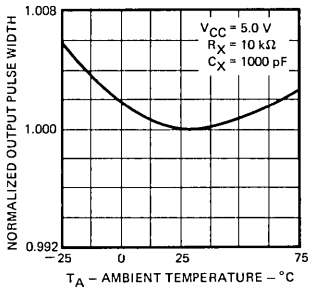


Figure 13

TRUTH TABLES Am 2600/9600

$\overline{I}_0$	$\overline{I}_1$	I_2	I_3	I_4	$\overline{CD}_0$	$\overline{CD}_1$	OPERATION
H→L	H	H	H	H	H	H	Trigger
H	H→L	H	H	H	H	H	Trigger
L	X	L→H	H	H	H	H	Trigger
X	L	L→H	H	H	H	H	Trigger
L	X	H	L→H	H	H	H	Trigger
X	L	H	L→H	H	H	H	Trigger
L	X	H	H	L→H	H	H	Trigger
X	L	H	H	L→H	H	H	Trigger
X	X	X	X	X	L	X	Reset
X	X	X	X	X	X	L	Reset

Am9601

$\overline{I}_0$	$\overline{I}_1$	I_2	I_3	OPERATION
H→L	H	H	H	Trigger
H	H→L	H	H	Trigger
L	X	L→H	H	Trigger
X	L	L→H	H	Trigger
L	X	H	L→H	Trigger
X	L	H	L→H	Trigger

H = HIGH Voltage Level H→L = Transition from HIGH to LOW Voltage Level
L = LOW Voltage Level L→H = Transition from LOW to HIGH Voltage Level
X = Don't Care

Table I

Am 2600/9600/9601 LOADING RULES

Input/Output Am 2600/9600	9601	Pin No.'s	Input Unit Load	Fanout Output HIGH	Fanout Output LOW
$\overline{I}_0$	$\overline{I}_0$	1	1		
$\overline{I}_1$	$\overline{I}_1$	2	1	—	—
I_2	I_2	3	1	—	—
I_3	I_3	4	1	—	—
I_4	NC	5	1	—	—
$\overline{Q}$	$\overline{Q}$	6	—	16	8
GND	GND	7	—	—	—
Q	Q	8		16	8
$\overline{C}_{D0}$	NC	9	1	—	—
$\overline{C}_{D1}$	NC	10	1	—	—
C_X	C_X	11	—	—	—
NC	NC	12	—	—	—
C_X R_X	C_X R_X	13	—	—	—
V_{CC}	V_{CC}	14	—	—	—

NC = No Connection

Table II

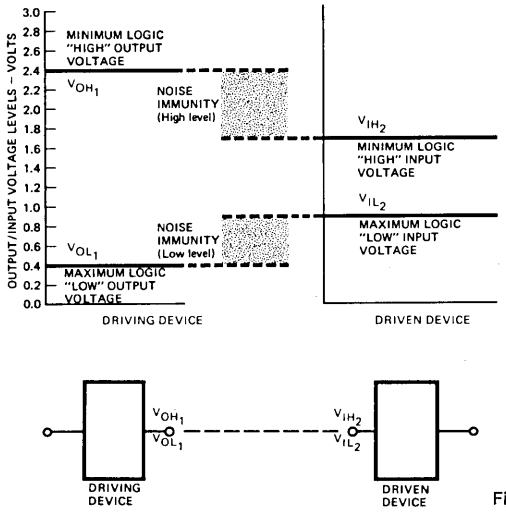
MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	Equivalent Input Unit Load LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

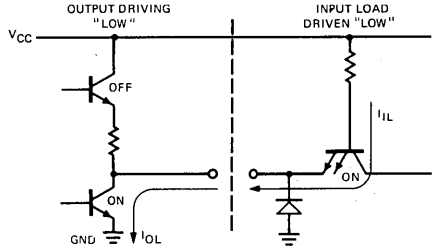
Table III

INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH



Current Interface Conditions — LOW



Current Interface Conditions — HIGH

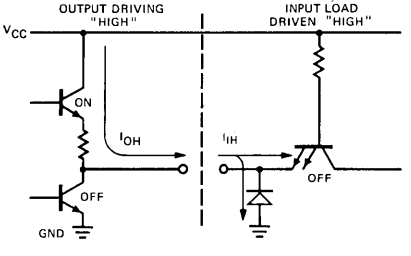
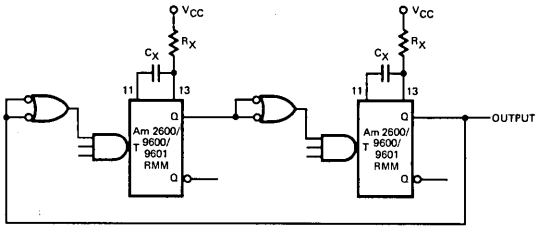


Figure 14

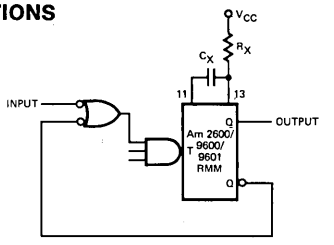
Am 2600/9600/9601 APPLICATIONS



Astable Multivibrator

Frequency of operation is dependent upon value of R_X and C_X.

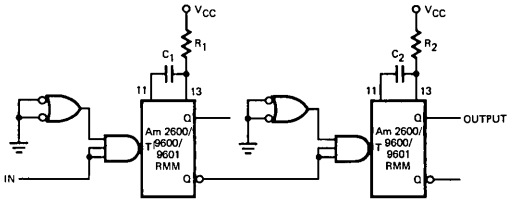
Figure 15



Frequency Division

This configuration makes the Am 2600/9600/9601 non-triggerable and capable of frequency division.

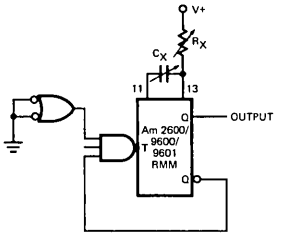
Figure 16



Delayed Pulse Generation

The first Am 2600/9600/9601 determines the time T_1 before the initiation of the output pulse. The second Am 2600/9600/9601 determines T_2, the output pulse width.

Figure 17



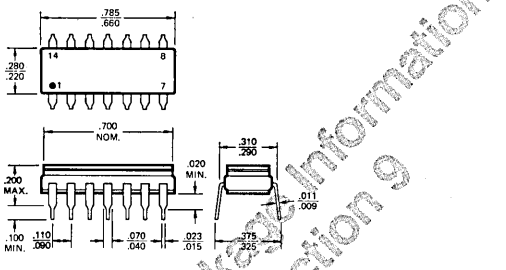
Resistance-to-Frequency Converter

The multivibrator is connected as an astable with the frequency controlled by a variable resistor or capacitor.

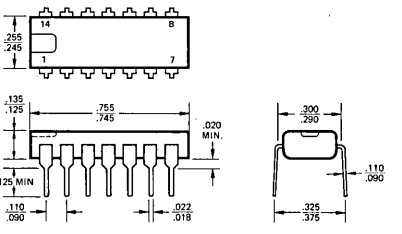
Figure 18

PHYSICAL DIMENSIONS

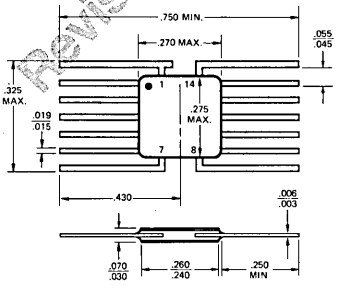
Hermetic Dual In-Line



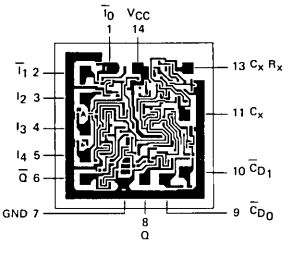
Molded



Flat Package



Metallization and Pad Layout



51 x 54 Mils

ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am2602/9602

Dual Retriggerable Resettable Monostable Multivibrator

Distinctive Characteristics:

- Retriggerable 0 to 100% duty cycle.
- 50ns to ∞ output pulse width range.
- Am2602 guaranteed pulse width change over temperature range.
- 100% reliability assurance testing including high temperature bake, temperature cycling, centrifuge and package hermeticity testing in compliance with MIL-STD-883.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

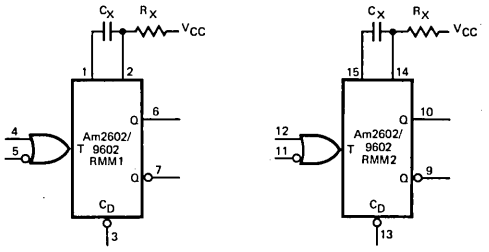
The Am2602 and Am9602 are dual DC-level sensitive resettable retriggerable monostable multivibrators which provide an output pulse whose duration and accuracy depend on external timing components.

Provision is made for triggering on the rising or falling edge of an input signal. All inputs are DC coupled making triggering independent of input rise and fall times. Each time the output from the OR trigger gate goes from a FALSE (LOW) to TRUE (HIGH) condition triggering occurs independent of the state of the monostable.

The direct clear facility allows a timing cycle to be terminated at any time during the cycle. A LOW signal on the $\overline{C_D}$ input resets the monostable independent of other conditions.

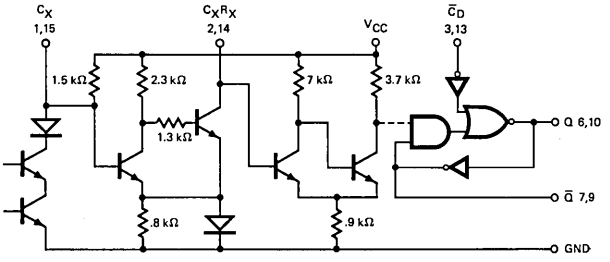
The Am2602 is a selected Am9602 with a guaranteed pulse width change of less than 1% over the temperature range of 0°C to +75°C.

LOGIC DIAGRAM



V_{CC} = Pin 16
Gnd. = Pin 8

INTERNAL TIMING CIRCUITRY

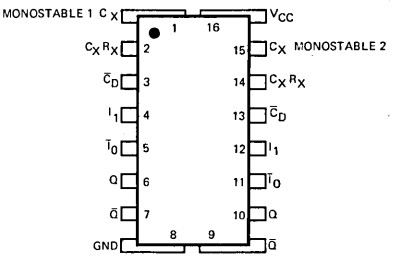


ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am2602	Molded DIP	0°C to +75°C	AM260259A
Am2602	Hermetic DIP	0°C to +75°C	AM260259E
Am2602	Hermetic DIP	−55°C to +125°C	AM260251E
Am2602	Hermetic Flat Pak	−55°C to +125°C	AM260251N
Am2602	Dice	Note	AM2602XXD
Am9602	Molded DIP	0°C to +75°C	U6M960259X
Am9602	Hermetic DIP	0°C to +75°C	U7B960259X
Am9602	Hermetic DIP	−55°C to +125°C	U7B960251X
Am9602	Hermetic Flat Pak	−55°C to +125°C	U4L960251X
Am9602	Dice	Note	UXX9602XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +8 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current Into Outputs When Output is LOW	50 mA
DC Input Current	−30 mA to +5 mA

ELECTRICAL CHARACTERISTICS

Am260259/960259X T_A = 0°C to +75°C V_{CC} = 4.75 to 5.25 V (COM grade)
Am260251/960251X T_A = −55°C to +125°C V_{CC} = 4.50 to 5.50 V (MIL grade)

DC Characteristics Over Operating Range (Note 1)

Parameters	Operating Range	Test Conditions		LIMITS T_A = MIN Min	Max	T_A = +25°C Min	Typ	Max	T_A = MAX Min	Max	Units
V_{OH} Output HIGH Voltage	MIL or COM	V_{CC} = MIN., I_{OH} = −0.96 mA		2.40		2.40	3.6		2.40		Volts
V_{OL} Output LOW Voltage	MIL	I_{OL} = 8 x I_{IL} MAX.			0.40		0.2	0.40		0.40	Volts
	COM	I_{OL} = 8 x I_{IL} MAX.			0.45		0.2	0.45		0.45	
V_{IH} Input HIGH Voltage	MIL			2.00		1.70			1.50		Volts
	COM			1.90		1.80			1.60		
V_{IL} Input LOW Voltage	MIL				0.85			0.90		0.85	Volts
	COM				0.85			0.85		0.85	
I_{IL} Input Load Current	MIL	V_{IN} = 0.40 V	V_{CC} = MAX.		−1.60		−1.10	−1.60		−1.60	mA
			V_{CC} = MIN.		−1.24		−0.97	−1.24		−1.24	
	COM	V_{IN} = 0.45 V	V_{CC} = MAX.		−1.60		−1.00	−1.60		−1.60	
			V_{CC} = MIN.		−1.41		−0.90	−1.41		−1.41	
I_{IH} Reverse Input Current	MIL or COM	V_{CC} = MAX., V_{IN} = 4.5 V			60		2	60		60	µA
I_{SC} Short Circuit Current	MIL	V_{CC} = 5.0 V, V_O = 1.0 V				−8		−25			mA
	COM	V_{CC} = 5.0 V, V_O = 1.0 V				−8		−35			
I_{PD} Power Supply Current	9602 MIL	V_{CC} = 5.0 V	GND Pins 5 and 11		45		35	45		45	mA
	9602 COM		R_X = 10 kΩ		52		35	50		52	
	2602 COM	V_{CC} = MAX.	GND Pins 5 and 11		56		35	56		56	
	2602 MIL		R_X = 10 kΩ								

Switching Characteristics (T_A = 25°C)

Parameters			Test Conditions	2602 9602 MIL Min	Typ	Max	9602 COM Min	Typ	Max	Units
t_{pd+}	Turn Off Delay Negative Trigger Input to True Output		V_{CC} = 5.0 V, C_L = 15 pF R_X = 5 kΩ, C_X = 0 pF		25	35		25	40	ns
t_{pd-}	Turn On Delay Negative Trigger Input to False Output				25	35		25	40	ns
t_{pw} (min)	Minimum Output Pulse Width	True Output (Q)			45	65		50	70	ns
		False Output ($\overline{Q}$)			55	75		60	80	
t_{pw}	Pulse Width		V_{CC} = 5.0 V, C_L = 15 pF R_X = 10 kΩ, C_X = 1000 pF	3.08	3.42	3.76	3.08	3.42	3.76	µs
R_X	Timing Resistor over Temperature Range (Note 2)			5		50	5		50	kΩ
t_{pd-} ($\overline{C_D}$)	Delay from $\overline{C_D}$ to Q output LOW				11	17		11	17	ns

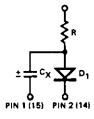
Am2602		Test Conditions	Min	Typ	Max	Units
Δt_{pw} (T)	Maximum change in Pulse Width True Output over temperature range 0°C to +75°C	V_{CC} = 5.0 V, C_L = 15 pF R_X = 10 kΩ, C_X = 1000 pF		0.5	1.0	%
	Maximum change in Pulse Width True Output over temperature range −55°C to +125°C (Am2602 MIL)			4.0	7.0	

Notes: 1. Tests are conducted with a 10 kΩ resistor placed between Pin 2 (14) and V_{CC} unless otherwise noted.
2. Maximum permissible R_X when used below 0°C is 25 kΩ.

OPERATION RULES

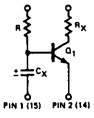
1. An external resistor R_X and an external capacitor C_X are required as shown in the logic diagram. The values of R_X may vary from 5.0 kΩ to 50 kΩ for 0°C to +75°C operation and 5.0 kΩ to 25 kΩ for −55°C to +125°C operation. C_X may vary from 0 to any value necessary and obtainable.
2. If a fixed value of R_X is used, the following values are recommended: R_X = 30 kΩ for 0°C to +75°C operation; R_X = 10 kΩ for −55°C to +125°C operation.
3. The output pulse width T is defined as follows:

   $T = 0.32\ R_X C_X\ [1 + \frac{0.7}{R_X}]$ (For C_X greater than 10^3 pF) Where: R_X is in kΩ, C_X is in pF, T is in ns. For $C_X < 10^3$ pF see Fig. 2.
4. If electrolytic type capacitors are to be used, it is recommended that they have low leakage. For capacitors with a high reverse leakage the following circuits can be used:



$R < 0.6\ R_X$ (Max)

D_1: any silicon type diode, such as FD700



This circuit also allows larger value of R to be used for longer output pulse width.

$R < R_X\ (0.7)\ (h_{FE}Q_1)$

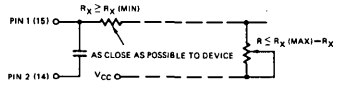
R_X (min) < R_X < R_X (max)

Q_1: Any NPN silicon device with sufficient h_{FE} at low currents, such as 2N2511

Both circuits prevent reverse voltage across C_X. The pulse width T for the circuits is defined as follows:

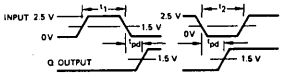
$T \approx 0.30\ RC_X\ [1 + \frac{0.7}{R}]$ Where: R is in kΩ, C_X is in pF, T is in ns.

5. To obtain variable pulse width, by remote trimming, the following circuit is recommended:

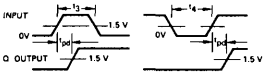


6. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
7. Input Trigger Pulse Rules. $t_1, t_2, t_3, t_4 > 40$ ns

Input to Pin 5 (11)
Pin 4 (12) = LOW
Pin 3 (13) = HIGH



Input to Pin 4 (12)
Pin 5 (11) = HIGH
Pin 3 (13) = HIGH



8. The retriggerable pulse width is calculated as shown below:

$t_w = t_{pw} + t_{pd+} = 0.32\ R_X C_X\ (1 + \frac{0.7}{R_X}) + t_{pd+}$

The retrigger pulse width is equal to the pulse width t_{pw} plus a delay time. For pulse widths greater than 500 ns, t_w can be approximated as t_{pw}.

NOTE: Retriggering will not occur if the retrigger pulse comes within $0.32\ R_X C_X (\frac{0.7}{R_X})$ ns after the initial trigger pulse.

9. Reset Operation — The Am2602/9602 have an active LOW reset facility. By applying a low to the reset input, any timing cycle can be terminated or any new cycle inhibited until the low reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held low.

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

OPERATIONAL TERMS:

I_{IL} Forward input load current.

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{IH} Reverse input load current.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage. Refer to figure 2.

V_{IL} Maximum logic LOW input voltage. Refer to figure 2.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

FUNCTIONAL TERMS:

$\overline{C_D}$ The asynchronous direct clear input. A LOW on this input resets the monostable independent of other conditions.

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

$\overline{I_0}$ The active LOW input of the monostables. With input I_1 LOW a HIGH to LOW transition on $\overline{I_0}$ will cause triggering.

I_1 The active HIGH input of the monostables. With $\overline{I_0}$ HIGH a LOW to HIGH transition on I_1 will cause triggering.

Input Unit Load One T^2L gate input load.

Q The TRUE output of the monostables.

$\overline{Q}$ The FALSE output of the monostables.

Triggering The switching of the monostable from the stable state to the unstable state and start of the timing cycle.

SWITCHING TERMS:

t_{pd+} The propagation delay from a HIGH to LOW transition on $\overline{I_0}$ to the true (Q) output LOW to HIGH transition.

t_{pd-} The propagation delay from a HIGH to LOW transition on $\overline{I_0}$ to the false ($\overline{Q}$) output HIGH to LOW transition.

t_{pw}**(min)** The minimum true (Q) output pulse width with $R_X = 5k\Omega$, $C_X = 0$ pF.

t_{pw} The pulse width obtained with $R_X = 10k\Omega$, $C_X = 1000$ pF.

Δt_{pw}**(T)** The maximum percentage change in pulse width of the true (Q) output for the Am2602 over the temperature range from the pulse width at 25°C.

Am 2602
Normalized Output Pulse Width Versus Ambient Temperature

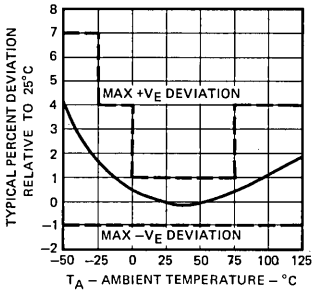
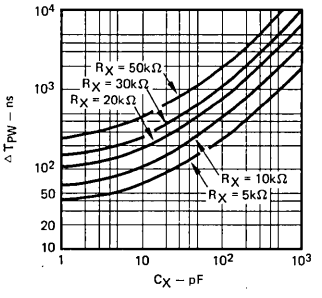


Figure 1

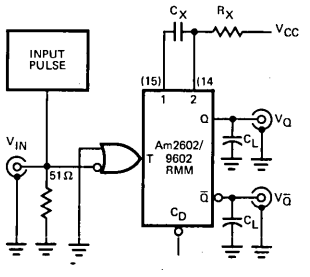
Output Pulse Width (ΔT_{pw}) Using Low Values of C_X



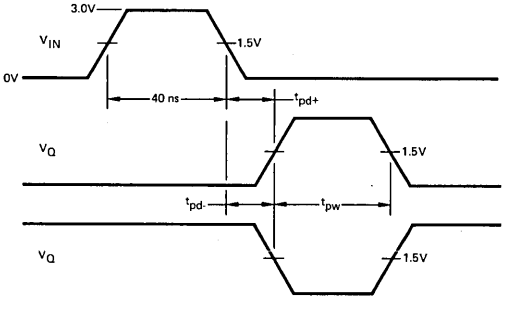
NOTE: Above $C_X = 10^3$ pF Use $\Delta T_{PW} = 0.32\, C_X\, R_X\, (1+0.7/R_X)$

Figure 2

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



V_{CC} = Pin 16
Gnd. = Pin 8



INPUT PULSE
f ≃ 100 kHz
Amp ≃ 3.0 V
Width ≃ 40 ns
$t_r = t_f \leq 10$ ns

Figure 3

TRUTH TABLE

Am2602/9602
For Each Monostable

$\overline{I}_0$	I_1	$\overline{C}_D$	Operation
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
H→L = HIGH to LOW Voltage Level transition
L→H = LOW to HIGH Voltage Level transition

Table I

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Table III

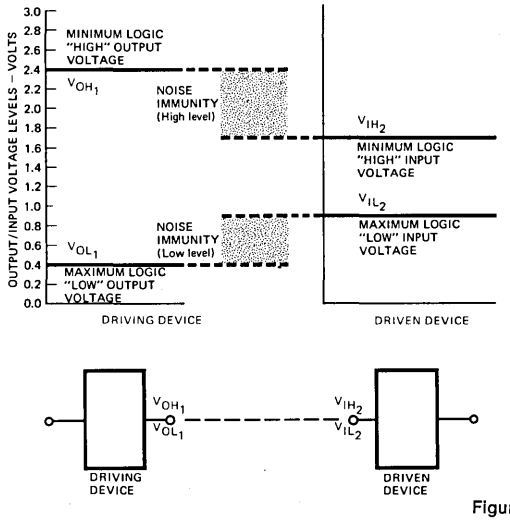
Am2602/9602 LOADING RULES

Input/Output	Pin No.'s	Input Unit Load	Fanout Output HIGH	Fanout Output LOW
Monostable 1 C_X	1	—	—	—
$C_X R_X$	2	—	—	—
$\overline{C}_D$	3	1	—	—
I_1	4	1	—	—
$\overline{I}_0$	5	1	—	—
Q	6	—	16	8
$\overline{Q}$	7	—	16	8
GND	8	—	—	—
Monostable 2 $\overline{Q}$	9	—	16	8
Q	10	—	16	8
$\overline{I}_0$	11	1	—	—
I_1	12	1	—	—
$\overline{C}_D$	13	1	—	—
$C_X R_X$	14	—	—	—
C_X	15	—	—	—
V_{CC}	16	—	—	—

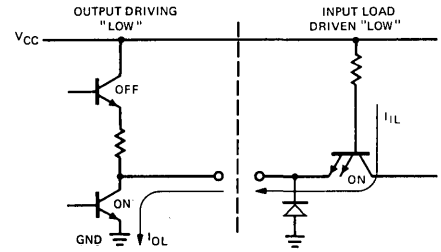
Table II

INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH



Current Interface Conditions — LOW



Current Interface Conditions — HIGH

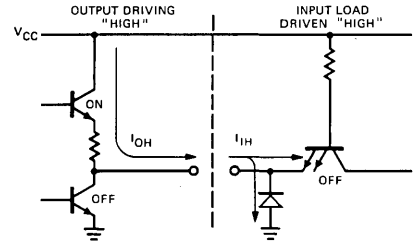
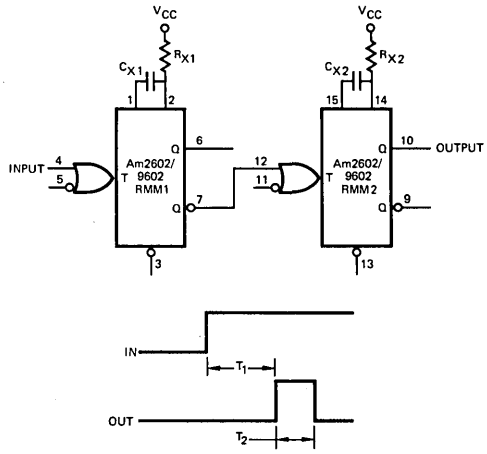


Figure 4

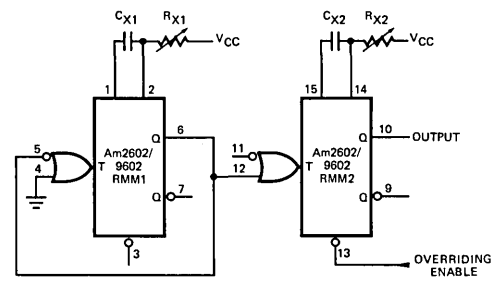
Am2602/9602 APPLICATIONS



Delayed Pulse Generation

Figure 5

The first monostable determines the time T_1 before the initiation of the output pulse. The second monostable determines T_2, the output pulse width.



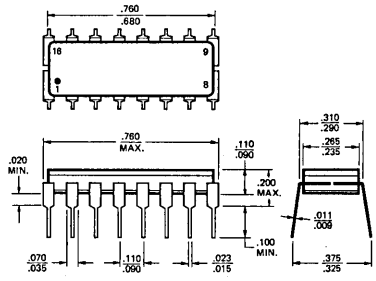
Pulse Generator

Figure 6

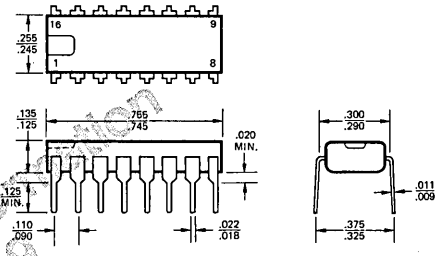
The output frequency produced with the above configuration is determined by C_{X1} and R_{X1}, while the pulse width is determined by C_{X2} and R_{X2}. Monostable 1 forms an astable multivibrator with an output pulse width of approximately 25 ns, while monostable 2 extends the pulse width to the required value.

PHYSICAL DIMENSIONS
Dual-In-Line

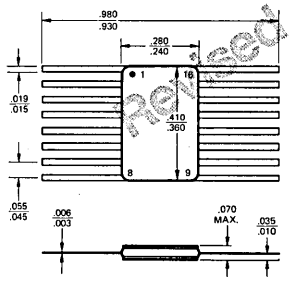
Hermetic



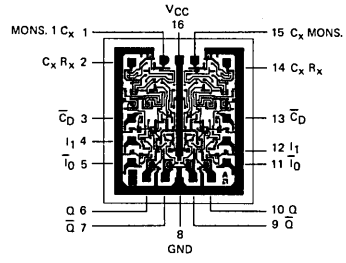
Molded



Flat Package



Metallization and Pad Layout



62 x 71 Mils

ADVANCED
MICRO
DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am26L02/96L02

Low Power Dual Retriggerable Resettable Monostable Multivibrators

Distinctive Characteristics:

- One-fourth the power of the equivalent Am2602/9602 dual single shots.
- 50 ns typical propagation delay.
- Fan-out of 3 with standard TTL circuits.
- Guaranteed pulse width variation versus temperature.
- 100% reliability assurance testing in compliance with MIL STD 883
- Electrically tested and optically inspected die for the assemblers of hybrid products
- Mixing privileges for obtaining price discounts. Refer to price list
- Available in highly reliable molded epoxy, hermetic dual-in-line or Hermetic flat package.

FUNCTIONAL DESCRIPTION

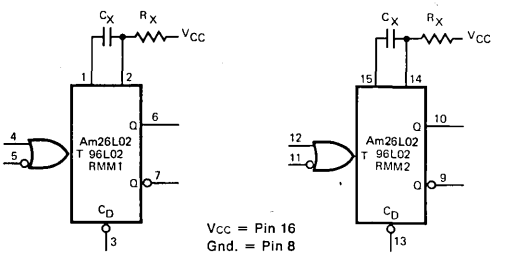
The Am 26L02 and 96L02 are low-power dual DC-level sensitive resettable retriggerable monostable multivibrators which provide an output pulse whose duration and accuracy depend on external timing components.

Provision is made for triggering on the rising or falling edge of an input signal. All inputs are DC coupled making triggering independent of input rise and fall times. Each time the output from the OR trigger gate goes from a FALSE (LOW) to TRUE (HIGH) condition triggering occurs independent of the state of the monostable.

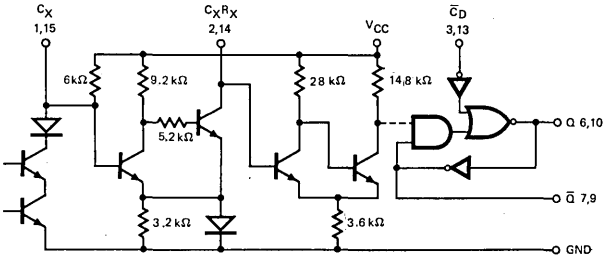
The direct clear facility allows a tuning cycle to be terminated at any time during the cycle. A LOW signal on the $\overline{C}_D$ input resets the monostable independent of other conditions.

The Am26L02 has a guaranteed pulse width variation versus temperature of only 1% over the temperature range 0°C to +75°C

LOGIC DIAGRAM



INTERNAL TIMING CIRCUITRY

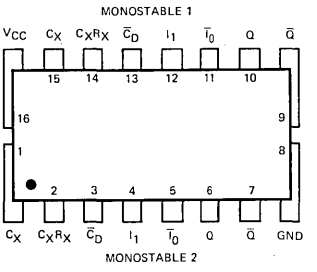


ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am26L02	Molded DIP	0°C to +75°C	Am26L0259A
Am26L02	Hermetic DIP	0°C to +75°C	Am26L0259E
Am26L02	Hermetic DIP	−55°C to +125°C	Am26L0251E
Am26L02	Hermetic Flat Pak	−55°C to +125°C	Am26L0251N
Am26L02	Dice	Note	Am26L02XXD
Am96L02	Molded DIP	0°C to +75°C	U6M96L0259X
Am96L02	Hermetic DIP	0°C to +75°C	U7B96L0259X
Am96L02	Hermetic DIP	−55°C to +125°C	U7B96L0251X
Am96L02	Hermetic Flat Pak	−55°C to +125°C	U4L96L0251X
Am96L02	Dice	Note	UXX96L02XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature range.

CONNECTION DIAGRAM
Top View



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current Into Outputs When Output is LOW	30 mA
DC Input Current	−30 mA to +5 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am96L0259X/26L0259X T_A = 0°C to +75°C V_{CC} = 4.75 V to 5.25 V
Am96L0251X/26L0251X T_A = −55°C to +125°C V_{CC} = 4.50 V to 5.50 V

Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.36 mA V_{IN} = V_{IH} or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 4.92 mA V_{IN} = V_{IH} or V_{IL}		0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.7	Volts
I_{IL} (Note 2)	93L Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.3 V		−0.25	−0.4	mA
I_{IH} (Note 2)	93L Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V		2.0	20	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 1.0 V	−2.0		−13	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		10	16	mA

Notes: 1: Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2: Actual input currents are obtained by multiplying unit load current by the 93L input load factor. (See loading rules)

Switching Characteristics (T_A = 25°C)

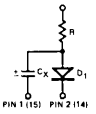
Parameters			Test Conditions	Min	Typ	Max	Units
t_{pd+}	Turn Off Delay Negative Trigger Input to True Output	Am26/96L0251X	V_{CC} = 5.0 V, C_L = 15 pF R_X = 20 kΩ, C_X = 0 pF		55	75	ns
		Am26/96L0259X			55	80	
t_{pd-}	Turn On Delay Negative Trigger Input to False Output				42	62	ns
t_{pw} (min)	Minimum True Output Pulse Width				110		ns
T	Pulse Width at True Output		V_{CC} = 5.0 V, C_L = 15 pF R_X = 39 kΩ, C_X = 1000 pF	12.4	13.8	15.2	μs
R_X	Timing Resistor (Note 2)	Am26/96L0251X		20		200	kΩ
		Am26/96L0259X		16		220	
t_{pd-} ($\overline{C_D}$)	Delay from $\overline{C_D}$ to Q output LOW				27	40	ns
ΔT	Maximum Change in Pulse Width True Output over operating temperature range	Am96L0259X	V_{CC} = 5.0 V, C_L = 15 pF R_X = 39 kΩ, C_X = 1000 pF	0	0.3	1.6	%
		Am96L0251X		0	1.3		
		Am26L0259X		0	0.3	1.0	
		Am26L0251X		0	1.0	4.0	

Notes: 1. Tests are conducted with a 39 kΩ resistor placed between Pin 2 (14) and V_{CC} unless otherwise noted.
2. Maximum permissible R_X when used below 0°C is 100 kΩ.

OPERATION RULES

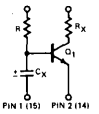
1. An external resistor R_X and an external capacitor C_X are required as shown in the logic diagram. The values of R_X may vary from 20 kΩ to 200 kΩ for 0°C to +75°C operation and 20 kΩ to 100 kΩ for −55°C to +125°C operation. C_X may vary from 0 to any value necessary and obtainable.
2. If a fixed value of R_X is used, the following values are recommended: R_X = 120 kΩ for 0°C to +75°C operation; R_X = 39 kΩ for −55°C to +125°C operation.
3. The output pulse width T is defined as follows:

   $T = 0.33\,R_XC_X\,[1 + \frac{3.0}{R_X}]$ (For C_X greater than 10^3 pF) Where: R_X is in kΩ, C_X is in pF, T is in ns. For $C_X < 10^3$ pF see Fig. 3.
4. If electrolytic type capacitors are to be used, the following two arrangements are recommended:



$R < 0.6\,R_X$ (Max)

D_1: any silicon type diode, such as FD700



This circuit also allows larger value of R to be used for longer output pulse width.

$R < R_X\,(0.7)\,(h_{FE}Q_1)$

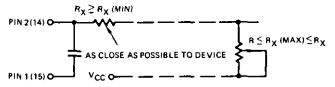
$R_X\,(min) < R_X < R_X\,(max)$

Q_1: Any NPN silicon device with sufficient h_{FE} at low currents, such as 2N2511

Both circuits prevent reverse voltage across C_X. The pulse width T for the circuits is defined as follows:

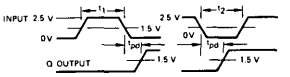
$T \approx 0.30\,RC_X\,[1 + \frac{3.0}{R}]$ Where: R is in kΩ, C_X is in pF, T is in ns.

5. To obtain variable pulse width, by remote trimming, the following circuit is recommended:

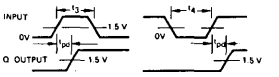


6. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
7. *Input Trigger Pulse Rules.* t_1, t_2, t_3, $t_4 > 60$ ns

Input to Pin 5 (11)
Pin 4 (12) = LOW
Pin 3 (13) = HIGH



Input to Pin 4 (12)
Pin 5 (11) = HIGH
Pin 3 (13) = HIGH



8. The retriggerable pulse width is calculated as shown below:

$t_w = t_{pw} + t_{pd+} \approx 0.33\,R_XC_X\,(1 + \frac{3.0}{R_X}) + t_{pd+}$

The retrigger pulse width is equal to the pulse width t_{pw} plus a delay time. For pulse widths greater than 500 ns, t_w can be approximated as t_{pw}.

NOTE: Retriggering will not occur if the retrigger pulse comes within $0.33\,R_XC_X(\frac{3.0}{R_X})$ ns after the initial trigger pulse.

9. Reset Operation — The Am26L02/96L02 have an active LOW reset facility. By applying a low to the reset input, any timing cycle can be terminated or any new cycle inhibited until the low reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held low.

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

OPERATIONAL TERMS:

I_{IL} Forward input load current.

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{IH} Reverse input load current.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage. Refer to figure 2.

V_{IL} Maximum logic LOW input voltage. Refer to figure 2.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

FUNCTIONAL TERMS:

$\overline{C}_D$ The asynchronous direct clear input. A LOW on this input resets the monostable independent of other conditions.

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

$\overline{I}_0$ The active LOW input of the monostables. With input I_1 LOW a HIGH to LOW transition on $\overline{I}_0$ will cause triggering.

I_1 The active HIGH input of the monostables. With $\overline{I}_0$ HIGH a LOW to HIGH transition on I_1 will cause triggering.

Input Unit Load One T^2L gate input load.

Q The TRUE output of the monostables.

$\overline{Q}$ The FALSE output of the monostables.

Triggering The switching of the monostable from the stable state to the unstable state and start of the timing cycle.

SWITCHING TERMS:

t_{pd+} The propagation delay from a HIGH to LOW transition on $\overline{I}_0$ to the true (Q) output LOW to HIGH transition.

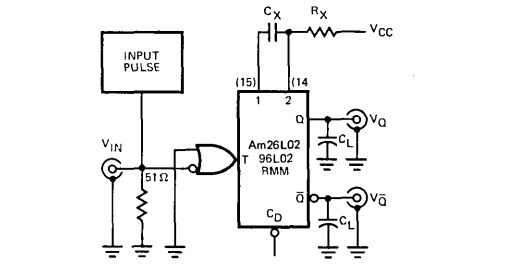
t_{pd-} The propagation delay from a HIGH to LOW transition on $\overline{I}_0$ to the false ($\overline{Q}$) output HIGH to LOW transition.

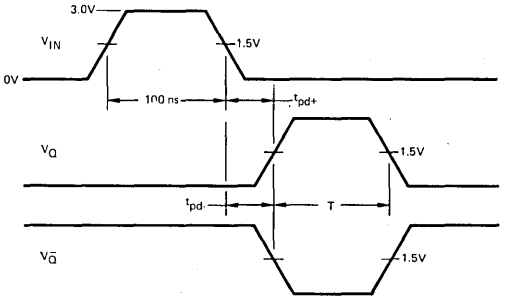
t_{pw}**(min)** The minimum true (Q) output pulse width with $R_X = 20$ kΩ, $C_X = 0$ pF.

T The pulse width obtained with $R_X = 39$ kΩ, $C_X = 1000$ pF.

ΔT The maximum percentage change in pulse width of the true (Q) output over the temperature range from the pulse width at 25°C.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





INPUT PULSE
f ≃ 25 kHz
Amp ≃ 3.0 V
Width ≃ 100 ns
$t_r = t_f \leq 10$ ns

Figure 1

TRUTH TABLE

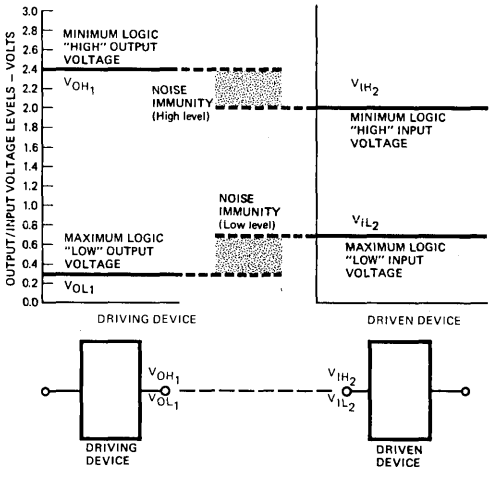
Am26L02/96L02
For Each Monostable

$\bar{I}_0$	I_1	$\bar{C}_D$	Operation
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

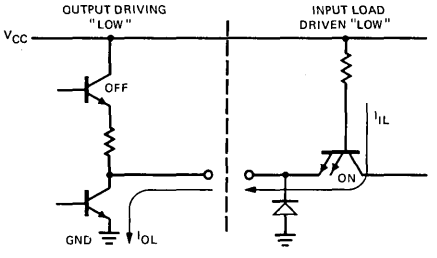
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
H→L = HIGH to LOW Voltage Level transition
L→H = LOW to HIGH Voltage Level transition

INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH



Current Interface Conditions — LOW



Current Interface Conditions — HIGH

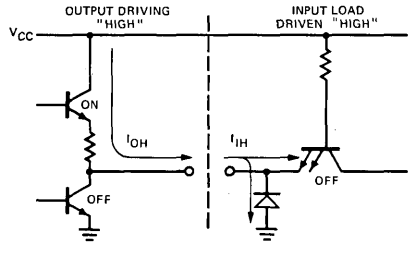


Figure 2

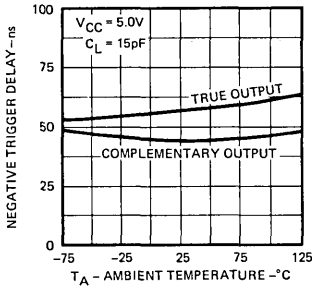
Am26L02/96L02 LOADING RULES

Input/Output	Pin No.'s	93L00 SERIES UNIT LOADS: Input Unit Load	Fanout: Output HIGH	Fanout: Output LOW	9300 SERIES UNIT LOADS: Input Unit Load: Input HIGH	Input Unit Load: Input LOW	Fanout: Output HIGH	Fanout: Output LOW
Monostable 1 C_X	1	—	—	—	—	—	—	—
C_XR_X	2	—	—	—	—	—	—	—
$\overline{C}_D$	3	1	—	—	0.5	0.25	—	—
I_I	4	1	—	—	0.5	0.25	—	—
$\overline{I}_0$	5	1	—	—	0.5	0.25	—	—
Q	6	—	12	12	—	—	6	3
$\overline{Q}$	7	—	12	12	—	—	6	3
GND	8	—	—	—	—	—	—	—
Monostable 2 $\overline{Q}$	9	—	12	12	—	—	6	3
Q	10	—	12	12	—	—	6	3
$\overline{I}_0$	11	1	—	—	0.5	0.25	—	—
I_I	12	1	—	—	0.5	0.25	—	—
$\overline{C}_D$	13	1	—	—	0.5	0.25	—	—
C_XR_X	14	—	—	—	—	—	—	—
C_X	15	—	—	—	—	—	—	—
V_{CC}	16	—	—	—	—	—	—	—

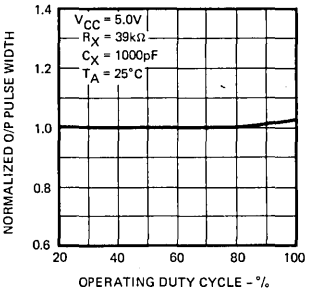
Table I

Typical Pulse Characteristics

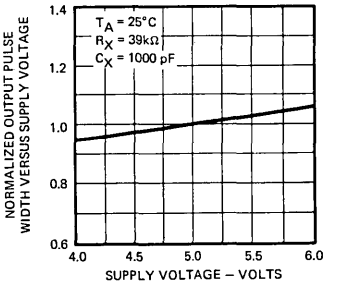
Negative Trigger Delay Time Versus Ambient Temperature



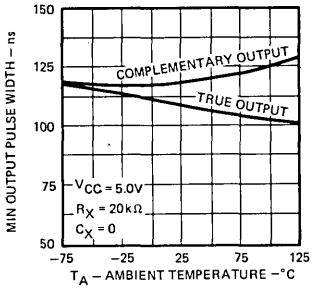
Normalized Output Pulse Width Versus Operating Duty Cycle



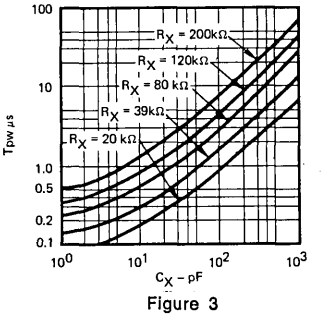
Normalized Output Pulse Width Versus Supply Voltage



Min. Output Pulse Width Versus Ambient Temperature



Output Pulse Width T Using Low Values Of C_X



Normalized Output Pulse Width Versus Ambient Temperature

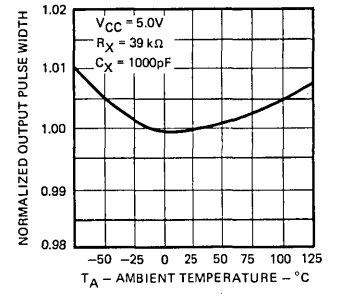
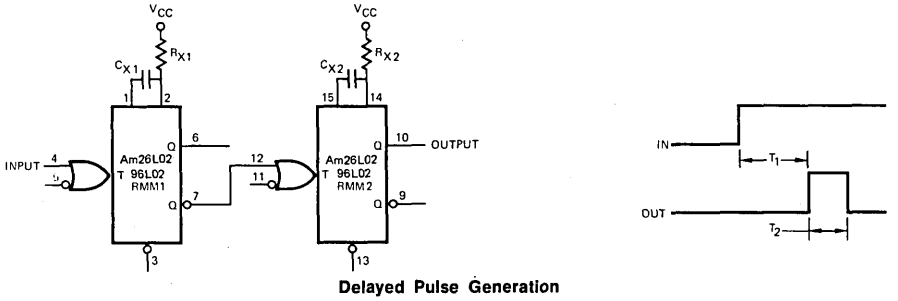


Figure 3

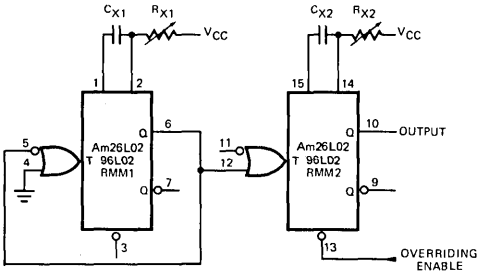
Am96L02 APPLICATIONS



Delayed Pulse Generation

The first monostable determines the time T_1 before the initiation of the output pulse. The second monostable determines T_2, the output pulse width.

Figure 5



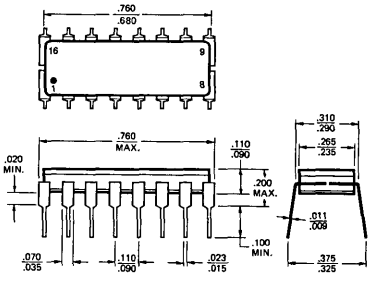
Pulse Generator

The output frequency produced with the above configuration is determined by C_{X1} and R_{X1}, while the pulse width is determined by C_{X2} and R_{X2}. Monostable 1 forms an astable multivibrator with an output pulse width of approximately 110 ns, while monostable 2 extends the pulse width to the required value.

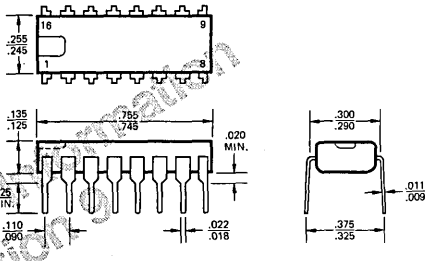
Figure 6

PHYSICAL DIMENSIONS
Dual-In-Line

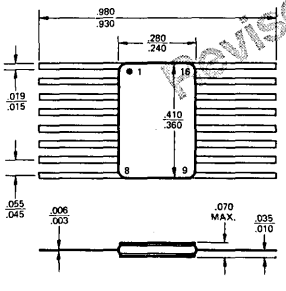
Hermetic



Molded



Flat Package



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Am26S02

Schottky Dual Retriggerable, Resettable Monostable Multivibrator

PRELIMINARY DATA

Distinctive Characteristics

- Advanced Schottky technology with PNP inputs
- Retriggerable 0% to 100% duty cycle
- 40ns to ∞ output pulse width range
- 100kΩ maximum timing resistor value
- Am26S02XM typical pulse width change of less than 0.7% over −55°C to +125°C
- Am26S02XC typical pulse width change of less than 0.35% over 0°C to +70°C

FUNCTIONAL DESCRIPTION

The Am26S02 is a dual DC level sensitive, retriggerable, resettable monostable multivibrator built using advanced Schottky technology. The output pulse duration and accuracy depend on the external timing components of each multivibrator. The Am26S02 features PNP inputs to reduce the input loading.

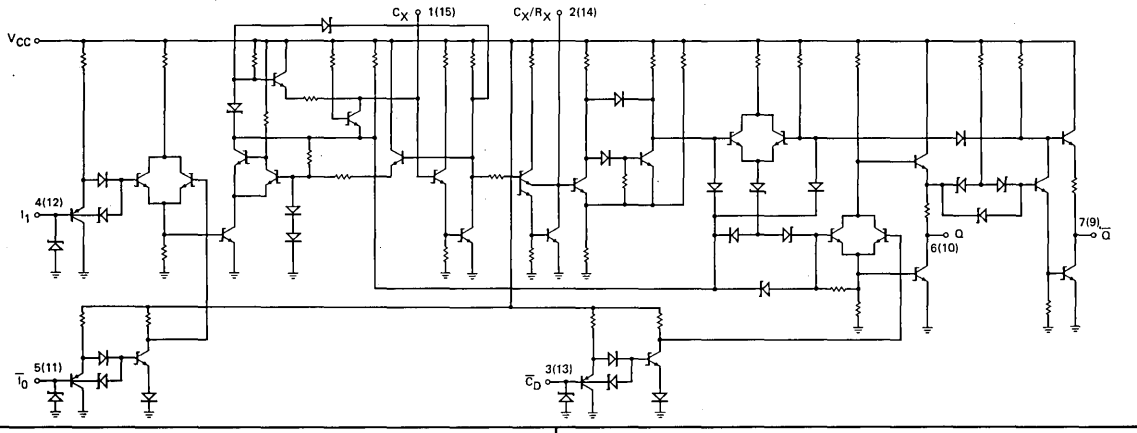
Provision is made on each multivibrator circuit for triggering the PNP inputs on either the rising or falling edge of an input signal by including an inverting and non-inverting trigger input. These PNP inputs are DC coupled making triggering independent of the input rise or fall time. Each time the monostable trigger input is activated from the OR trigger gate, full pulse length triggering occurs independent of the present state of the monostable.

The direct clear PNP input allows a timing cycle to be terminated at any time during the cycle. A LOW on the clear input forces the Q output LOW regardless of the $\overline{I_0}$ or I_1 inputs.

The Am26S02XM has a typical pulse width change of less than 0.7% over the full military −55°C to +125°C temperature range. The Am26S02XC has a typical pulse width change of less than 0.35% over the commercial 0°C to +70°C temperature range.

SCHEMATIC DIAGRAM

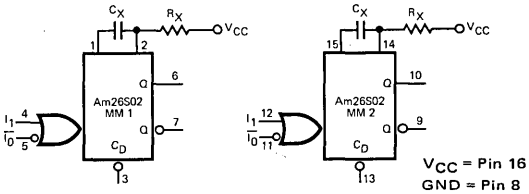
(One Monostable Multivibrator Shown)



ORDERING INFORMATION

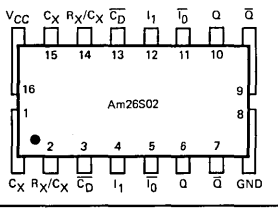
Package Type	Temperature Range	Order Number
Molded DIP	0°C to + 70°C	AM26S02PC
Hermetic DIP	0°C to + 70°C	AM26S02DC
Dice	0°C to + 70°C	AM26S02XC
Hermetic DIP	−55°C to +125°C	AM26S02DM
Hermetic Flat Pak	−55°C to +125°C	AM26S02FM
Dice	−55°C to +125°C	AM26S02XM

LOGIC SYMBOLS



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM



Note:
Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am26S02XC	T_A = 0°C to +70°C	V_{CC} = 5.0 V ±5% (COM'L)	MIN. = 4.75 V	MAX. = 5.25 V
Am26S02XM	T_A = −55°C to +125°C	V_{CC} = 5.0 V ±10% (MIL)	MIN. = 4.5 V	MAX. = 5.5 V

Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2mA V_{IN} = V_{IH} or V_{IL}	2.5			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA V_{IN} = V_{IH} or V_{IL}			0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V			−0.4	mA
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			20	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 1.0V T_A = 25°C Only	−8		−35	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)		53		mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. I_{CC} is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.

Switching Characteristics (T_A = +25°C)

Parameters	Description		Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	$\overline{I_0}$ to Q		V_{CC} = 5.0 V, R_L = 280 Ω, C_L = 15 pF, R_X = 5kΩ, C_X = 0 pF		14	20	ns
t_{PHL}	$\overline{I_0}$ to $\overline{Q}$				14	20	ns
t_{PLH}	I_1 to Q				13	20	ns
t_{PHL}	I_1 to $\overline{Q}$				12	20	ns
t_{PLH}	Clear to $\overline{Q}$				8	12	ns
t_{PHL}	Clear to Q				7	10	ns
t_{pw}	Pulse Width	$\overline{I_0}$ or I_1 HIGH		20			
		$\overline{I_0}$ or I_1 LOW		20			ns
		Clear LOW		20			
t_s	Clear Recovery (inactive) to Trigger						ns
t_{pwQ} (Min.)	Minimum Pulse Width Q Output				40		ns
t_{pwQ}	Pulse Width Q Output		V_{CC} = 5.0 V, R_L = 280 Ω, C_L = 15 pF, R_X = 10 k, C_L = 1000 pF		3.4		μs
R_X	Timing Resistor		0°C to 70°C	5		100	kΩ
			−55°C to +125°C	5		50	

DEFINITION OF FUNCTIONAL TERMS:

$\overline{C_D}$ Asynchronous direct CLEAR. A LOW on the clear input resets the monostable regardless of the other inputs.

$\overline{I_0}$ Active-LOW input. With I_1 LOW, a HIGH-to-LOW transition will trigger the monostable.

I_1 Active-HIGH input. With $\overline{I_0}$ HIGH, a LOW-to-HIGH transition will trigger the monostable.

Q The TRUE monostable output.

$\overline{Q}$ The Complement monostable output.

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{C_D}$	I_1	$\overline{I_0}$	Q	$\overline{Q}$
L	X	X	L	H
H	H	X	L	H
H	L	↓	⎍	⎏
H	X	L	L	H
H	↑	H	⎍	⎏

H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition
↓ = HIGH-to-LOW Transition
⎍ = LOW-HIGH-LOW Pulse
⎏ = HIGH-LOW-HIGH Pulse
X = Don't Care

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s		Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
C_X	Mono 1	1	–	–	–
R_X/C_X		2	–	–	–
$\overline{C_D}$		3	0.4	–	–
I_1		4	0.4	–	–
$\overline{I_0}$		5	0.4	–	–
Q		6	–	40	10
$\overline{Q}$		7	–	40	10
GND		8	–	–	–
$\overline{Q}$	Mono 2	9	–	40	10
Q		10	–	40	10
$\overline{I_0}$		11	0.4	–	–
I_1		12	0.4	–	–
$\overline{C_D}$		13	0.4	–	–
R_X/C_X		14	–	–	–
C_X		15	–	–	–
V_{CC}		16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

OPERATION RULES

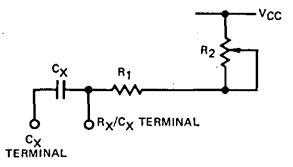
TIMING

1. Timing components C_X and R_X values.

Operating Temperature Range

	0°C to 70°C	-55°C to +125°C
R_X MIN.	5kΩ	5kΩ
R_X MAX.	100kΩ	50kΩ
C_X	any value	any value

2. Remote adjustment of timing.



$R_1 + R_2 = R_X$
$R_1 \geq R_X$ MIN.
$R_2 < R_X$ MAX. $- R_1$

In the above arrangement, R_1 and C_X should be as close as possible to the device pins to minimize stray capacitance and external noise pickup. The variable resistor R_2 can be located remotely from the device if reasonable care is used.

3. Pulse width change measurements.

The pulse width $t_{pw}Q$ is specified and measured with components of better than 0.1% accuracy. If measurements are made with reduced component tolerances, the expected accuracy should be adjusted accordingly.

4. Timing for $C_X \leq 1000$ pF.

When using capacitor of less than or equal to 1000 pF in value, the output pulse width should be determined from the output pulse width versus external timing capacitance graph.

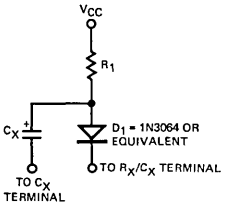
5. Timing for $C_X > 1000$ pF.

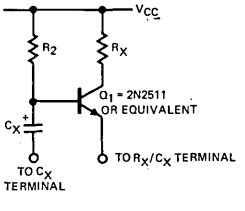
For capacitors of greater than 1000 pF in value, the output pulse width, $t_{pw}Q$, is determined by

$t_{pw}Q =$ (Consult Factory)

where

R_X is in kilohms
C_X is in picofarads
$t_{pw}Q$ is in nanoseconds





$R_1 \leq 0.6 \times R_X$ MAX. $\qquad R_2 < 0.7 \times h_{FEQ1} \times R_X$

6. Protection of electrolytic timing capacitors.

If the electrolytic capacitor to be used as C_X cannot withstand 1.0 volt reverse bias, one of the following two circuit techniques should be used to protect the electrolytic capacitor from the reverse voltage.

The output pulse width, $t_{pw}Q$ for the diode circuit modifies the previous timing equation as follows:

$t_{pw}Q =$ (Consult Factory)

The output pulse width for the transistor circuit is

$t_{pw}Q =$ (Consult Factory)

Notice that the transistor circuit allows values of timing resistor R_2 larger than the R_X MIN. $< R_X <$ R_X MAX. to obtain longer output pulse widths for a given C_X.

TRIGGER AND RETRIGGER

1. Triggering.

The minimum pulse width signal into input $\overline{I}_0$ or input I_1 to cause the device to trigger is 20ns. Refer to the truth table for the appropriate input conditions.

2. Retriggering.

The retriggered pulse width, $t_{pwr}Q$, is the time during which the output is active after the device is retriggered during a timing cycle. It differs from the initial pulse width $t_{pw}Q$ timing equation as follows.

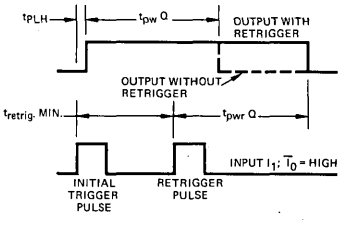
$t_{pwr}Q = t_{pw}Q + t_{PLH}$

where t_{PLH} is the propagation delay time from the $\overline{I}_0$ or I_1 input to the output. Note that t_{PLH} is typically 15ns and therefore becomes relatively unimportant as $t_{pw}Q$ increases.

3. Rapid retriggering.

A minimum retriggering time does exist. That is, the device cannot be retriggered until a minimum recovery time has elapsed. The minimum retrigger time is defined by

t_{retrig} MIN. $= 0.224\ C_X$
C is in picofarads
t is in nanoseconds



CLEAR

A LOW on the clear inputs terminates the timing cycle. A new trigger cycle cannot be initiated while the clear is LOW. With the clear HIGH, the device is under the command of the I_1 and $\overline{I}_0$ inputs.

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

f_{MAX} The highest operating clock frequency.

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{PW} Pulse width. The time between the leading and trailing edges of a pulse.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

t_s Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

t_h Hold time. The time interval for which a signal must be retained at one input after an active transition occurs at another input terminal.

t_R Release time. The time interval for which a signal may be indeterminant at one input terminal before an active transition occurs at another input terminal. (The release time falls within the set-up time interval and is specified by some manufacturers as a negative hold time).

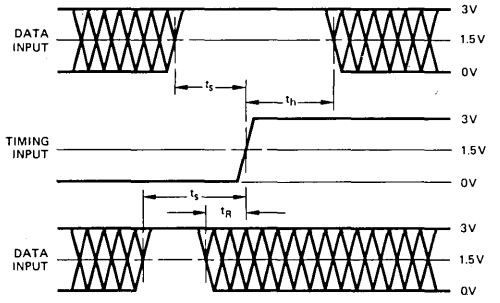
UNIT LOAD DEFINITIONS

	HIGH		LOW	
SERIES	Current	Measure Voltage	Current	Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0 mA	0.5 V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

Note: 1. 54L/74L has two different types of standard inputs.

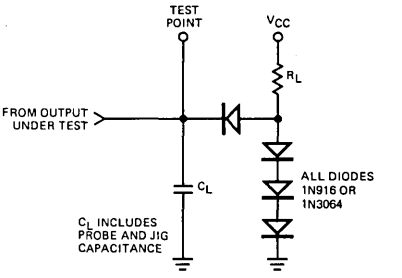
SCHOTTKY PARAMETER MEASUREMENTS
FOR STANDARD ACTIVE-PULLUP TOTEM-POLE OUTPUTS

SET-UP, HOLD, AND RELEASE TIMES

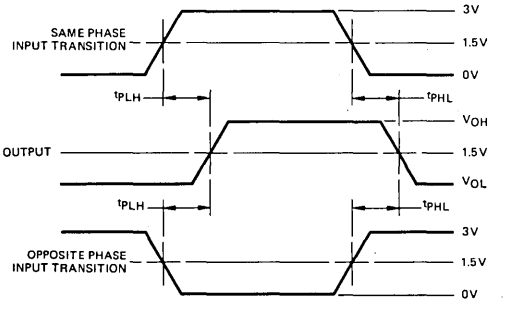


Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross-hatched area is don't care condition.

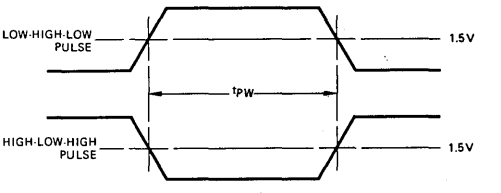
LOAD TEST CIRCUIT



PROPAGATION DELAY

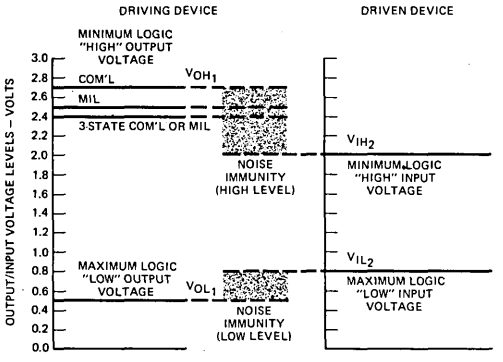


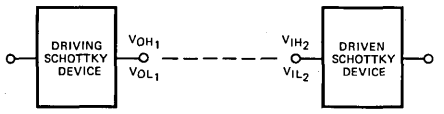
PULSE WIDTH



Notes: 1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_o = 50Ω; t_r ≤ 2.5ns; t_f ≤ 2.5ns.

SCHOTTKY INPUT/OUTPUT VOLTAGE INTERFACE CONDITIONS





Note: Refer to Electrical Characteristics for measure currents.

DEFINITION OF STANDARD TERMS

H HIGH, applying to a HIGH voltage level.

L LOW, applying to a LOW voltage level.

I Input.

O Output.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

I_{IL} LOW-level input current with a specified LOW-level voltage applied.

I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.

I_{OL} LOW-level output current.

I_{OH} HIGH-level output current.

I_{SC} Output short-circuit source current.

I_{CC} The supply current drawn by the device from the V_{CC} power supply.

V_{IL} Logic LOW input voltage.

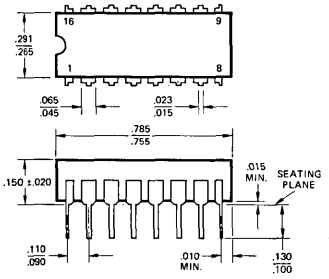
V_{IH} Logic HIGH input voltage.

V_{OL} LOW-level output voltage with I_{OL} applied.

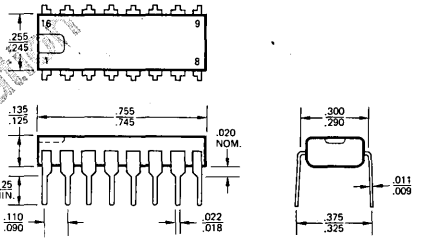
V_{OH} HIGH-level output voltage with I_{OH} applied.

PHYSICAL DIMENSIONS
Dual-In-Line

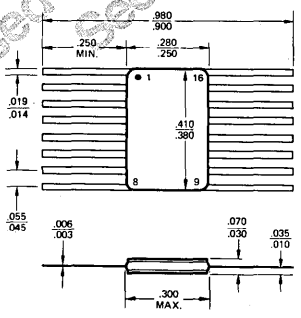
Ceramic



Molded



Flat Package



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Am26S12/26S12A
Quad Bus Transceiver

Distinctive Characteristics

- Quad high-speed bus transceivers
- Driver outputs can sink 100mA at 0.7V typically
- Choice of receiver hysteresis characteristics
- Electrically tested and optically inspected dice for the assemblers of hybrid products.
- 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and package hermeticity testing in compliance with MIL-STD-883.
- Mixing privileges for obtaining price discounts. Refer to price list.

FUNCTIONAL DESCRIPTION

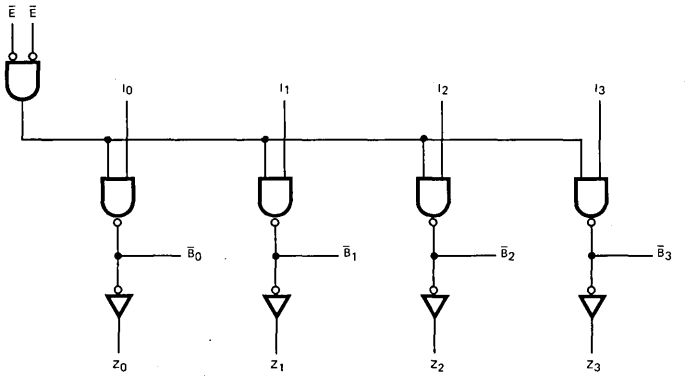
The Am26S12/26S12A are high-speed quad Bus Transceivers consisting of four high-speed bus drivers with open-collector outputs capable of sinking 100mA at 0.7 volts and four high-speed bus receivers. Each driver output is brought out and also connected internally to the high-speed bus receiver. The receiver has an input hysteresis characteristic and a TTL output capable of driving ten TTL Loads.

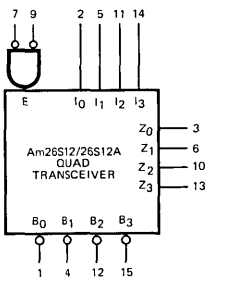
An active LOW, two-input AND gate controls the four drivers so that outputs of different device drivers can be connected together for party-line operation. The enable inputs can be conveniently driven by active LOW decoders such as the Am54S/74S139.

The high-drive capability in the LOW state allows party-line operation with a line impedance as low as 100Ω. The line can be terminated at both ends, and still give considerable noise margin at the receiver. The hysteresis characteristic of the Am26S12 receiver is chosen so that the receiver output switches to a HIGH logic level when the receiver input is at a HIGH logic level and moves to 1.4 volts typically, and switches to a LOW logic level when the receiver input is at a LOW logic level and moves to 2.0 volts typically. This hysteresis characteristic makes the receiver very insensitive to noise on the bus.

The Am26S12A is functionally identical to the Am26S12 but has a different hysteresis characteristic so that the output switches with the input being typically at 1.2 volts or 2.25 volts. In both devices the threshold margin, the difference between the switching points, is greater than 0.4 volts.

LOGIC DIAGRAM/SYMBOL





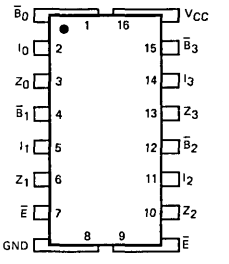
V_{CC} = PIN 16
GND = Pin 8

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am26S12	Molded DIP	0°C to +75°C	AM26S12PC
Am26S12	Ceramic DIP	0°C to +75°C	AM26S12DC
Am26S12	Hermetic DIP	−55°C to +125°C	AM26S12DM
Am26S12	Hermetic Flat Pak	−55°C to +125°C	AM26S12FM
Am26S12	Dice	Note	AM26S12XX
Am26S12A	Molded DIP	0°C to +75°C	AM26S12APC
Am26S12A	Ceramic DIP	0°C to +75°C	AM26S12ADC
Am26S12A	Hermetic DIP	−55°C to +125°C	AM26S12ADM
Am26S12A	Hermetic Flat Pak	−55°C to +125°C	AM26S12AFM
Am26S12A	Dice	Note	AM26S12AXX

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Outputs	200 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am26S12XC-Am26S12AXC T_A = 0°C to +75°C V_{CC} = 5.0V ±5% (COM Range)
Am26S12XM-Am26S12AXM T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL Range) Note 1

Parameters	Description	Test Conditions	Min.	Typ. (Note 2)	Max.	Units
I_{CC}	Power Supply Current	V_{CC} = MAX.		46	70	mA
I_{BUS}	Bus Leakage Current	V_{CC} = MAX. or 0V; V_{BUS} = 4.0V; Driver in OFF State			100	μA

Driver Characteristics

V_{OL} (Note 1)	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	COM I_{OL} = 100mA			0.7	0.8	Volts
			MIL	I_{OL} = 60mA		0.55	0.7	Volts
				I_{OL} = 100mA		0.7	0.85	
V_{IH}	Input HIGH Voltage				2.0			Volts
V_{IL}	Input LOW Voltage						0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_I	Input Current at Maximum Input Voltage	V_{CC} = MAX., V_I = 5.5V					1.0	mA
I_{IH}	Unit Load Input HIGH Current	V_{CC} = MAX., V_I = 2.4V				1.0	40	μA
I_{IL}	Unit Load Input LOW Current	V_{CC} = MAX., V_I = 0.4V				0.4	−1.6	mA

Receiver Characteristics

V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −800μA, V_{IN} = V_{IL} (Receiver)			2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = V_{IL} (Receiver)				0.4	0.5	Volts
V_{IH}	Input HIGH Level Threshold	$\overline{E}$ = H	Am26S12		1.8	2.0	2.2	Volts
			Am26S12A		2.05	2.25	2.45	
V_{IL}	Input LOW Level Threshold	$\overline{E}$ = H	Am26S12		1.2	1.4	1.6	Volts
			Am26S12A		1.0	1.2	1.4	
V_{TM}	Input Threshold Margin	$\overline{E}$ = H			0.4			Volts
I_{OS}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V			−20		−55	mA

Notes: 1. For the Am26S12FM, Am26S12AFM the output current must be limited at 60mA or the maximum case temperature limited to 125°C for correct operation.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.

Switching Characteristics (T_A = 25°C, V_{CC} = 5.0V)

Parameters	Description	Conditions	Min.	Typ.	Max.	Units
t_{pd+}	Turn Off Delay Input to Bus	C_{LB} = 15pF, R_{LB} = 100Ω		7	11	ns
t_{pd-}	Turn On Delay Input to Bus	C_{LB} = 300pF, R_{LB} = 50Ω		14	21	ns
t_{pd+}	Turn Off Delay Enable to Bus	C_{LB} = 15pF, R_{LB} = 50Ω		10	15	ns
t_{pd-}	Turn On Delay Enable to Bus	C_{LB} = 15pF, R_{LB} = 50Ω		10	15	ns
t_{pd+}	Turn Off Delay Bus to Output	C_L = 15pF		18	26	ns
t_{pd-}	Turn On Delay Bus to Output	C_L = 15pF		18	26	ns

DEFINITION OF TERMS

FUNCTIONAL TERMS

Threshold Voltage The voltage level on the input that will cause the output to change state. Because the receiver exhibits hysterisis, the LOW level receiver input threshold is different from the HIGH level input threshold.

ELECTRICAL TERMS

V_{OH} Output HIGH voltage. The voltage on the output when the output is HIGH.

V_{OL} Output LOW voltage. The voltage on the output when the output is LOW.

V_{IH} Input HIGH threshold. The voltage that must be applied to the input to cause the output to switch from a HIGH to a LOW.

V_{IL} Input LOW threshold. The voltage that must be applied to the input to cause the output to switch from a LOW to a HIGH.

V_{TM} Input Threshold Margin. The voltage margin between the V_{IL} and V_{IH} of a device.

I_{IH} Input HIGH current. The current that will flow into the input when a HIGH level is present on the input.

I_{IL} Input LOW current. The current that will flow out of the input when a LOW logic level is present on the input.

I_{OH} Output HIGH Current. The current drawn out of the output when the output is HIGH.

I_{OL} Output LOW Current. The current forced into the output when the output is LOW.

I_{OS} Output Short Circuit Current. The current that flows out of the output when the output and input are both grounded.

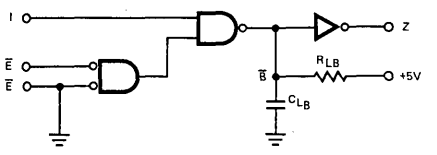
I_{CC} Current drawn from the V_{CC} power supply.

SWITCHING TERMS

t_{pd+} The propagation delay from an input transition to the output LOW-to-HIGH transition.

t_{pd-} The propagation delay from an input transition to the output HIGH-to-LOW transition.

SWITCHING CIRCUITS AND WAVEFORMS



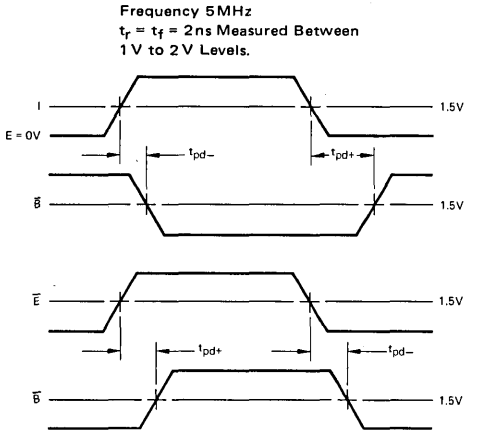


Figure 1. Bus Propagation Delays

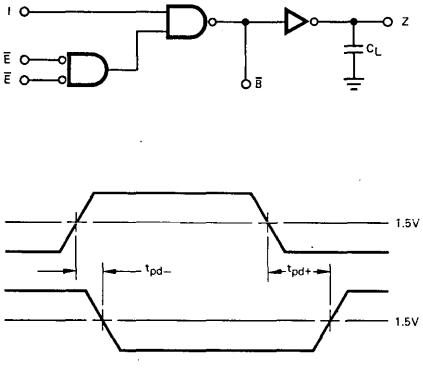


Figure 2. Receiver Propagation Delays

TRUTH TABLE
Am26S12/26S12A

Inputs		Outputs	
$\overline{E}$	I	$\overline{B}$	Z
L	L	H	L
L	H	L	H
H	X	Y	$\overline{Y}$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Y = Voltage Level of Bus

Table I

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

Table II

PERFORMANCE CURVES

Am26S12 Typical Receiver Input Characteristic

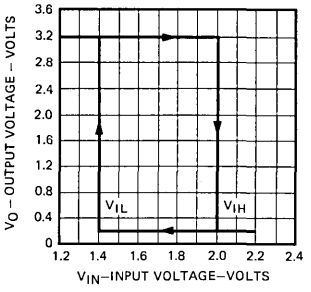


Fig. 3

Am26S12A Typical Receiver Input Characteristic

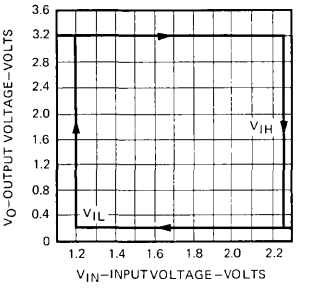


Fig. 4

INPUT/OUTPUT CIRCUITRY

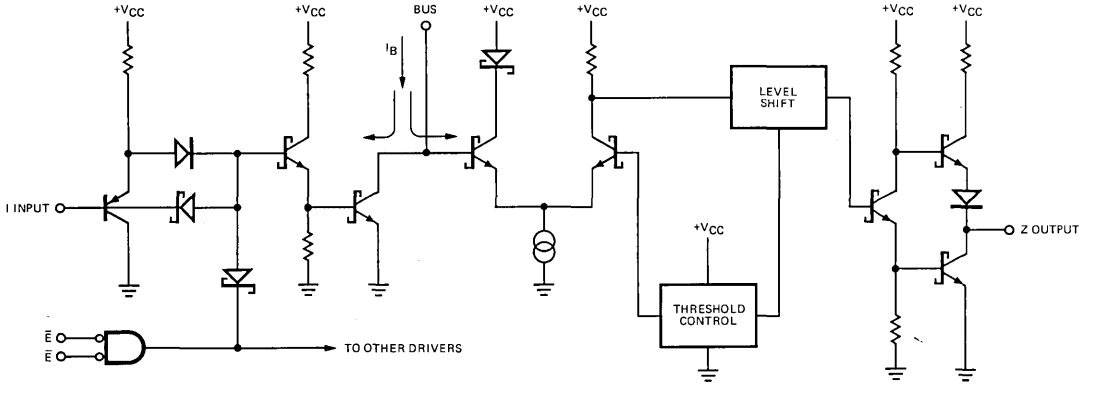


Fig. 5

Am26S12/26S12A APPLICATION

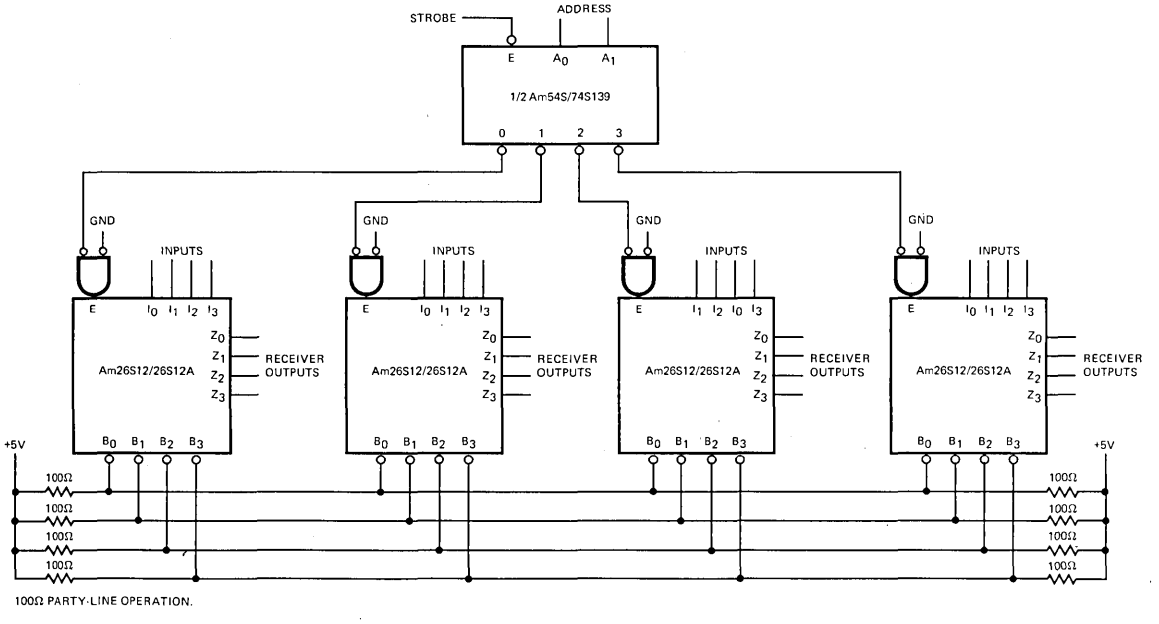
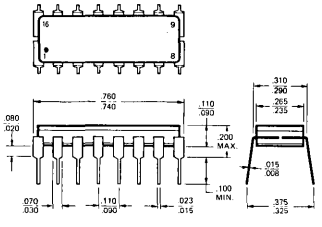


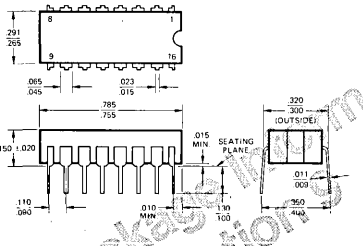
Fig. 6

PHYSICAL DIMENSIONS
Dual-In-Line

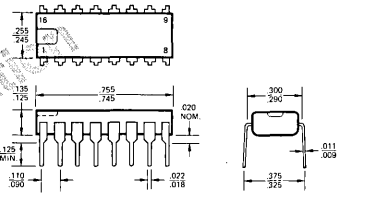
Hermetic



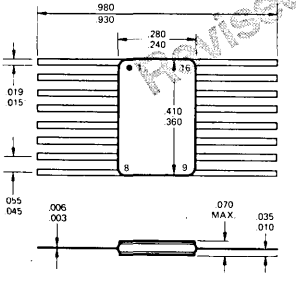
Ceramic



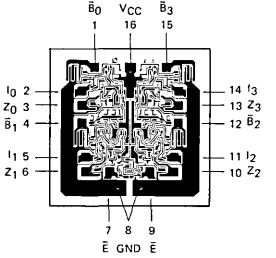
Molded



Flat Package



Metallization and Pad Layout



DIE SIZE 0.071" x 0.072"

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TELEX: 34-6306

Am2614/9614

Single-Ended and Differential Line Drivers

Distinctive Characteristics:

- Dual differential line driver with complementary outputs (Am9614)
- Quad single-ended driver for multi-channel common ground operation (Am2614)
- Single 5-volt supply
- DTL, TTL compatible
- Short-circuit protected outputs
- Able to drive 50Ω terminated transmission lines
- 100% eliability assurance testing in compliance with MIL STD 883.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.
- Available in highly reliable molded epoxy, hermetic dual-in-line, or hermetic flat package.

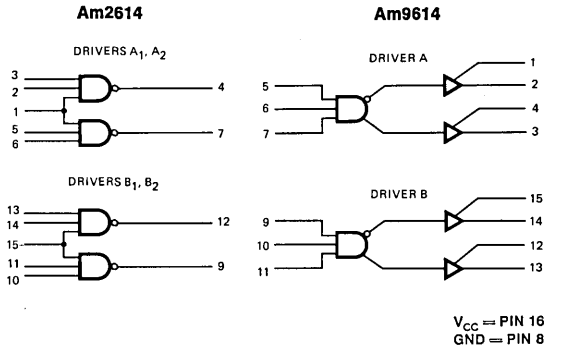
FUNCTIONAL DESCRIPTION

The Am2614 and Am9614 are DTL TTL compatible line drivers operating off a single 5V supply. The Am2614 is a quad inverting driver with two separate inputs and one common-strobe input for each pair of drivers. The device has active pull-up outputs for high speed and good capacitance drive. The Am2614 is ideal for single-ended transmission line driving, or as a high-speed, high-fan out driver for semiconductor memory decoding, buffering, clock driving and general logic use.

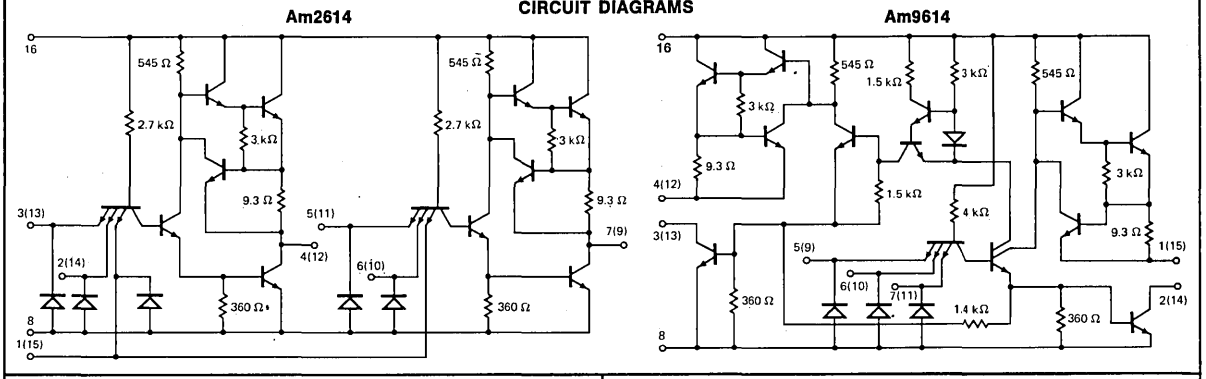
The Am9614 is designed to drive either differential single-ended, back-matched or terminated transmission lines. The device has the active pull-down and active pull-up circuits split and brought out to adjacent pins. This allows multiplex operation (wire AND) at the driving end in either the single-ended mode via the uncommitted collector or in the differential mode by use of the active pull-ups on one side and the uncommitted collectors on the other. The complementary outputs of the Am9614 give great application flexibility.

Both the Am2614 and Am9614 have short-circuit protected active pull-ups, and incorporate input clamp diodes to reduce the effect of line transients, and can drive into 50Ω terminated transmission lines.

LOGIC DIAGRAMS



CIRCUIT DIAGRAMS



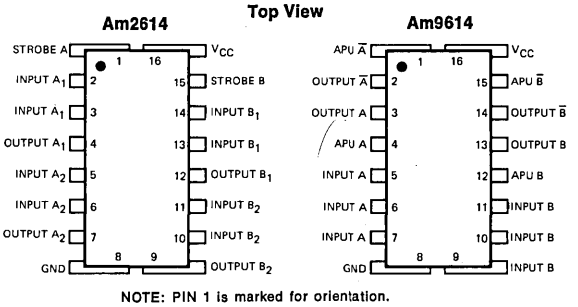
Am2614/9614 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	AM261459A
Hermetic DIP	0°C to +75°C	AM261459E
Hermetic DIP	−55°C to +125°C	AM261451E
Hermetic Flat Pak	−55°C to +125°C	AM261451N
Dice	Note	AM2614XXD
Molded DIP	0°C to +75°C	U6M961459X
Hermetic DIP	0°C to +75°C	U7B961459X
Hermetic DIP	−55°C to +125°C	U7B961451X
Hermetic Flat Pak	−55°C to +125°C	U4L961451X
Dice	Note	UXX9614XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAMS

Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	200 mA
DC Input Current	Note 1

ELECTRICAL CHARACTERISTICS

Am261459/961459 T_A = 0°C to +75°C
Am261451/961451 T_A = −55°C to +125°C

DC Characteristics (Note 2)

Parameters	Part No.	Test Conditions	LIMITS −55°C Min	−55°C Max	0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	+125°C Min	+125°C Max	Units
V_{OH} Output HIGH Voltage	Am261451 Am961451	V_{CCL} = 4.5 V, I_{OH} = −10 mA	2.40				2.40	3.2				2.40		Volts
	Am261459 Am961459	V_{CCL} = 4.75 V, I_{OH} = −10 mA			2.40		2.40	3.2		2.40				
V_{OL} Output LOW Voltage	Am261451 Am961451	V_{CCL} = 4.5 V, I_{OL} = 40 mA		0.40				0.2	0.40				0.40	Volts
	Am261459 Am961459	V_{CCL} = 4.75 V, I_{OL} = 40 mA				0.45		0.2	0.45		0.45			
V_{IH} Input HIGH Voltage	Am261451 Am961451	V_{CCL} = 4.5 V	2.00				1.70	1.5				1.40		Volts
	Am261459 Am961459	V_{CCL} = 4.75 V			1.90		1.80	1.5		1.60				
V_{IL} Input Low Voltage	Am261451 Am961451	V_{CCH} = 5.5 V		0.80				1.3	0.90				0.80	Volts
	Am261459 Am961459	V_{CCH} = 5.25 V				0.85		1.3	0.85		0.85			
I_F Input Load Current	Am261451	V_{CCH} = 5.5 V, V_F = 0.4 V		−2.40				−1.65	−2.40				−2.40	mA
	Am961451			−1.60				−1.10	−1.60				−1.60	
	Am261459	V_{CCH} = 5.25 V, V_F = 0.45 V				−2.40		−1.50	−2.40		−240			
	Am961459					−1.60		−1.00	−1.60		−1.60			
I_R Reverse Input Current	Am261451	V_{CCH} = 5.5 V, V_R = 4.5 V		90					90				90	μA
	Am961451			60					60				60	
	Am261459	V_{CCH} = 5.25 V, V_R = 4.5 V				90			90		90			
	Am961459					60			60		60			
I_{SC} Short Circuit Current	Am261451 Am961451	V_{CC} = 5.5 V, V_O = 0 V					−40	−90	−120					mA
	Am261459 Am961459	V_{CC} = 5.25 V, V_O = 0 V					−40	−90	−120					
I_{PD} Power Supply Current	Am261451 Am961451	V_{CC} = 5.5 V, Inputs = 0 V		48.7				34	48.7				48.7	mA
	Am261451 Am961451	V_{CC} = 7.0 V, Inputs = 0 V						46	65.7					
	Am261459 Am961459	V_{CC} = 5.25 V, Inputs = 0 V				48.7		33	48.7		48.7			
	Am261459 Am961459	V_{CC} = 7.0 V, Inputs = 0 V						46	70					
I_{CEX} Reverse Output Current	Am261451 Am961451	V_{CCH} = 5.5 V, V_{CEX} = 12 V		100				10	100				200	μA
	Am261459 Am961459	V_{CCH} = 5.25 V, V_{CEX} = 5.25 V					100	10	100		200			
V_{OLC} Output Low Clamp Voltage	Am261451 Am961451	V_{CCH} = 5.5 V, I_{OLC} = −40 mA						−0.8	−1.5					Volts
	Am261459 Am961459	V_{CCH} = 5.25 V, I_{OLC} = −40 mA						−0.8	−1.5					
V_{IC} Input Clamp Voltage	Am261451 Am961451	V_{CCL} = 4.5 V, I_{IC} = −12 mA						−1.0	−1.5					Volts
	Am261459 Am961459	V_{CCL} = 4.75 V, I_{IC} = −12 mA						−1.0	−1.5					

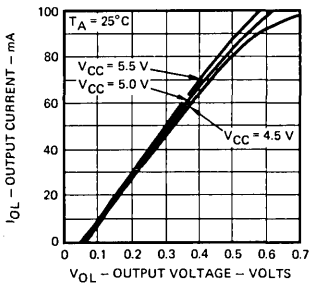
Switching Characteristics

Parameters			Test Conditions	51 Grade +25°C Min	51 Grade +25°C Typ	51 Grade +25°C Max	59 Grade +25°C Min	59 Grade +25°C Typ	59 Grade +25°C Max	Units
t_{pd+}	Turn Off Delay	Am9614	V_{CC} = 5.0 V, C_L = 30 pF V_M = 1.5 V, Refer to Fig. 1		14	20		14	30	ns
t_{pd-}	Turn On Delay	Am9614			18	20		18	30	ns
t_{pd+}	Turn Off Delay	Am2614	V_{CC} = 5.0 V, C_L = 30 pF V_M = 1.5 V, Refer to Fig. 92		8	12		8	15	ns
t_{pd-}	Turn On Delay	Am2614			7	10		7	12	ns

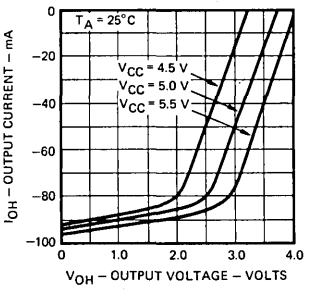
Note 1. Maximum current defined by DC input voltage.
2. Pulse tested.
3. For Am2614 strobe input currents use loading rules.

TYPICAL ELECTRICAL CHARACTERISTICS

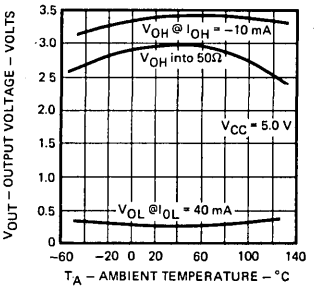
Output Low Current Versus Output Low Voltage



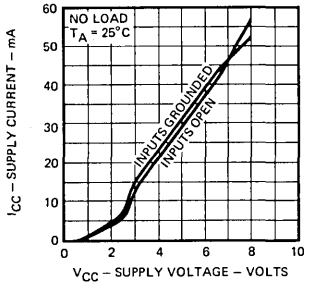
Output High Current Versus Output High Voltage



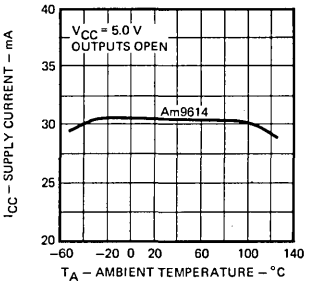
Logic Levels Versus Ambient Temperature



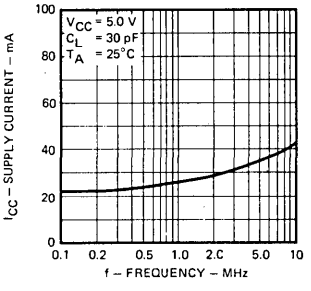
Supply Current Versus Supply Voltage



Supply Current Versus Temperature



Supply Current Versus Operating Frequency



DEFINITION OF TERMS

SUBSCRIPT TERMS:

F Forward, applying to LOW inputs.

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

R Reverse, applying to HIGH inputs.

FUNCTIONAL TERMS:

APU Active Pull-Up. The circuit network which presents a low impedance to the load when the device is switching from a LOW state to a HIGH state.

Fan-Out The logic HIGH or LOW output drive capability in terms of TTL Input Unit Loads.

R_M Back Matching Resistor. The resistor used to match the output impedance of the driver with the characteristic impedance of the transmission line.

SWITCHING TERMS:

t_{pd+} The propagation delay from a HIGH to LOW input transition to the LOW to HIGH output transition.

t_{pd-} The propagation delay from a LOW to HIGH input transition to the HIGH to LOW output transition.

OPERATIONAL TERMS:

I_F Forward input load current, for unit input load.

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{PD} The power supply current with the V_{CC} specified and inputs at 0 V.

I_R Reverse input load current with V_R applied to input.

I_{SC} Output current when output set to V_{OH} condition but forced low.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IC} Input clamp voltage. The voltage at the input with a negative input current of 12 mA.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

V_F Forward LOW input voltage, for forward input current (I_F) test.

V_R Input reverse HIGH voltage applied for input leakage current, (I_R) test.

SWITCHING CIRCUITS AND WAVEFORMS

Am2614

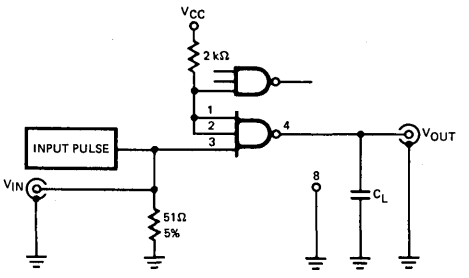


Figure 1

Am9614

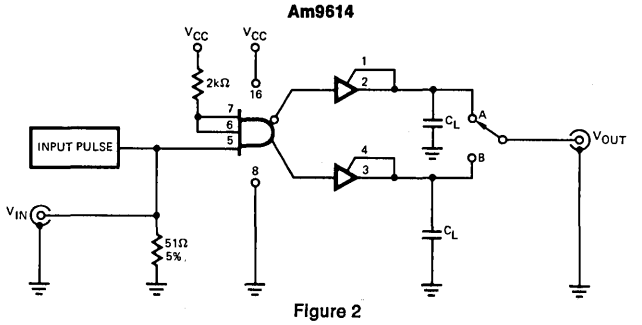
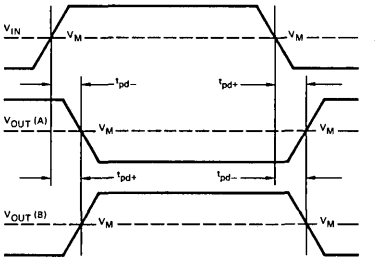


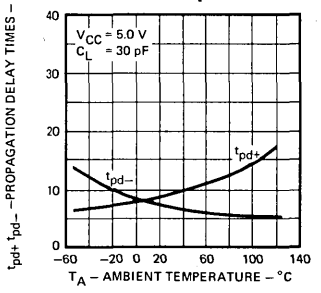
Figure 2



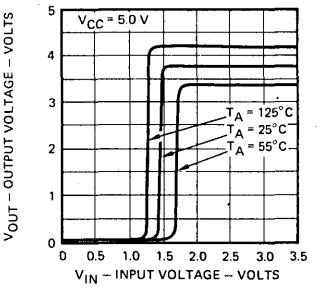
INPUT PULSE
Frequency = 500 kHz
Amplitude = 3.0 ±0.1 V
Pulse Width = 110 ±10 ns
$t_r = t_f \leq 5.0$ ns

TYPICAL ELECTRICAL CHARACTERISTICS

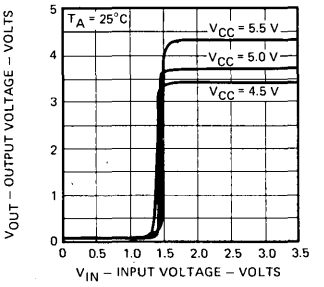
Am2614
Propagation Delay Time Versus Temperature



Transfer Characteristics Versus Temperature



Transfer Characteristics Versus Supply Voltage



USER NOTES

DIFFERENTIAL LINES The Am9614 dual differential line driver can be used with the Am9615 dual differential line receiver to form an interconnection system which can tolerate extremely noisy environments and interconnect equipments where there is a ±15V difference in voltage level of the equipment grounds. Two wires are used for each channel to form a balanced transmission line. This method of sending data between equipments offers extremely high protection from common mode noise and also gives excellent DC noise margins.

SINGLE ENDED LINES The Am2614 quad line driver and the Am2615 dual differential receiver allow data to be transmitted with only a single data wire per channel and a common ground for typically 8 data wires. This single ended mode of interconnection offers considerable savings in integrated circuit packages required and effectively halves the number of interconnections as compared to a balanced differential system. The method still gives ±15V common mode rejection and DC noise margin of interconnected TTL logic. The common ground wire should be twisted in with the data wires so that any injected noise is common to all wires. If a multiwire cable with screen is used one of the wires is used as the common ground line, and the screen is tied to ground at the driving end only.

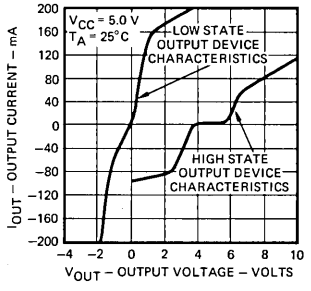
MATCHING Transmission lines can be matched in a number of ways. The most widely used method is to terminate the line at the receiving end in its characteristic impedance. This impedance is connected across the input terminals of the receiver. A 130Ω resistor is included at the + input of each receiver for matching twisted pairs and this resistor, or if the characteristic impedance is not 130Ω, a discrete resistor, is connected between the two receiver inputs. This method of matching causes a DC component in the signal. Power is dissipated in the resistor and the signal is attenuated. The DC component can be effectively removed by connecting a large capacitor in series with the terminating resistor.

The transmission line can also be terminated through the receiver power supply by placing equal value resistors from the + input of the receiver to V_{CC} and from the − input to ground. This method again has the disadvantage that a DC signal component exists, attenuation occurs, and power is dissipated in the terminating resistors but it does allow multiplexed operation in the balanced differential mode.

An alternate method to matching at the receiver is to back match at the driver. A resistor is placed in series with the line so that the signal from the driver which is reflected at the high input impedance of the receiver is absorbed at the driver. This method does not have a DC component and therefore no attenuation occurs and power is not dissipated in the resistor. For balanced differential driving a resistor is required in series with each line. The table below shows the value of each matching resistor required for lines of different characteristic impedance.

MULTIPLEXING When operating in the balanced differential mode the Am9614 driver can be OR tied with other devices to allow multiplexed operation. The open collector NAND outputs are connected together and the active pull up AND outputs are connected together. Selection of the active driver can be made by two of the three logic inputs on the driver. Multiplexed operation can only be performed with the lines terminated to the appropriate voltage level at the driver so that this method has a DC component and power is dissipated in the terminating resistors.

TYPICAL DC CHARACTERISTICS
FOR MATCHING TO TRANSMISSION LINE



BACK MATCHING TABLE

Z_O	R_M (ohms)	
	SINGLE ENDED	DIFFERENTIAL
50	24	12
75	51	24
92	68	33
100	75	36
130	110	54
300	280	140
600	580	290

LOADING RULES

Am2614

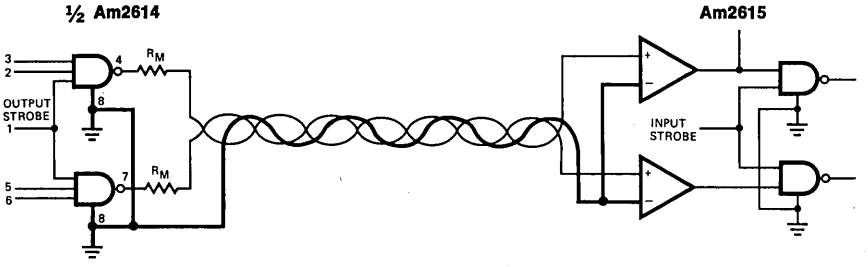
Input/Output	Pin No.'s	Input Unit Load	Fanout Output HIGH	Fanout Output LOW
Strobe A	1	3	—	—
Input A_1	2	1.5	—	—
Input A_1	3	1.5	—	—
Output A_1	4	—	166	25
Input A_2	5	1.5	—	—
Input A_2	6	1.5	—	—
Output A_2	7	—	166	25
GND	8	—	—	—
Output B_2	9	—	166	25
Input B_2	10	1.5	—	—
Input B_2	11	1.5	—	—
Output B_2	12	—	166	25
Input B_1	13	1.5	—	—
Input B_1	14	1.5	—	—
Strobe B	15	3	—	—
V_{CC}	16	—	—	—

Am9614

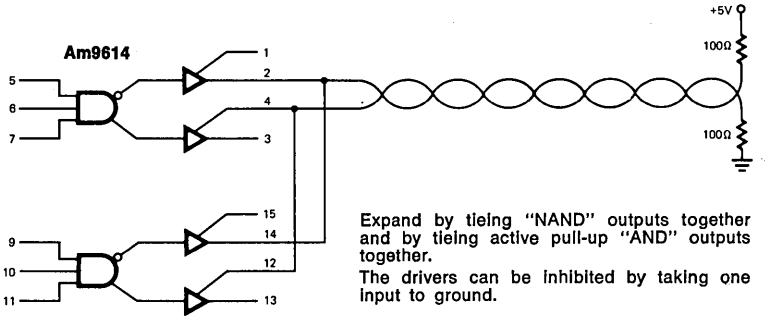
Input/Output	Pin No.'s	Input Unit Load	Fanout Output HIGH	Fanout Output LOW
APU A	1	—	166	—
Output A	2	—	—	25
Output A	3	—	—	25
APU A	4	—	166	—
Input A	5	1	—	—
Input A	6	1	—	—
Input A	7	1	—	—
GND	8	—	—	—
Input B	9	1	—	—
Input B	10	1	—	—
Input B	11	1	—	—
APU B	12	—	166	—
Output B	13	—	—	25
Output B	14	—	—	25
APU B	15	—	166	—
V_{CC}	16	—	—	—

Am2614/9614 APPLICATIONS

Single-Ended Back-Matched Operation With Common Ground



Differential Mode Expansion

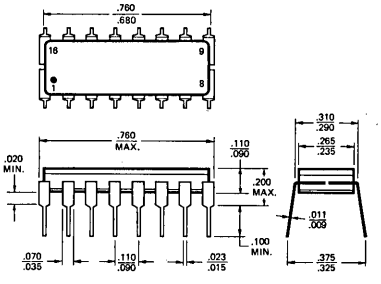


Expand by tieing "NAND" outputs together and by tieing active pull-up "AND" outputs together.

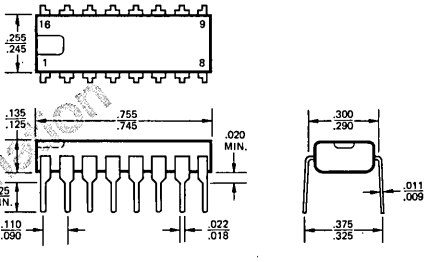
The drivers can be inhibited by taking one input to ground.

PHYSICAL DIMENSIONS
Dual-In-Line

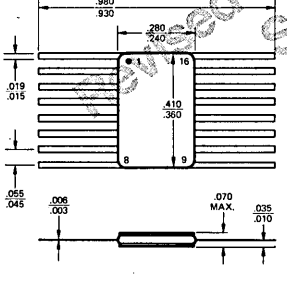
Hermetic



Molded

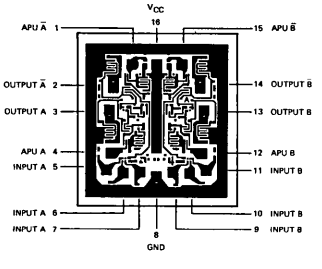


Flat Package



Metallization and Pad Layout

56 x 61 Mils



ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TLX: 34-6306
TWX: 910-339-9280

Am2615/9615
Dual Differential Line Receivers

Distinctive Characteristics:

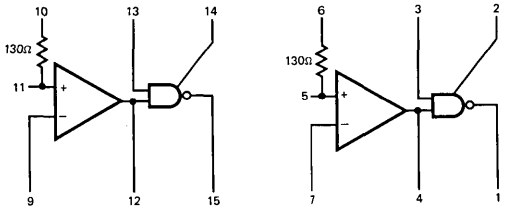
- Dual differential receiver (Am9615) pin-for-pin equivalent to the Fairchild 9615
- Dual differential receiver for single-ended data (Am2615)
- Single 5-volt supply
- High common-mode voltage range (±15 volts)
- Frequency response control, strobe, and internal terminating resistor
- Am2615 has fail safe capability
- Choice of uncommitted collector or active pull-up outputs
- 100% reliability assurance testing in compliance with MIL-STD-883
- Electrically tested and optically inspected die for the assemblers of hybrid products
- Mixing privileges for obtaining price discounts. Refer to price list
- Available in highly reliable molded, hermetic dual-in-line or hermetic flat package

FUNCTIONAL DESCRIPTION

The Am2615 and Am9615 are dual differential line receivers designed to receive digital data from transmission lines and operate over the military and industrial temperature ranges using a single 5 volt supply. The Am2615 can receive 3 volt single ended and the Am9615 ±500 mV differential data in the presence of zero common mode voltage, ±2.0V in the presence of ±15V common mode voltage and deliver undisturbed logic levels to the following DTL or TTL circuitry. The response time of each receiver and thereby immunity to AC noise can be controlled by an external capacitor. A strobe is provided for each receiver together with a 130Ω input terminating resistor. Each output has an uncommitted collector with an active pull-up network available on an adjacent pin.

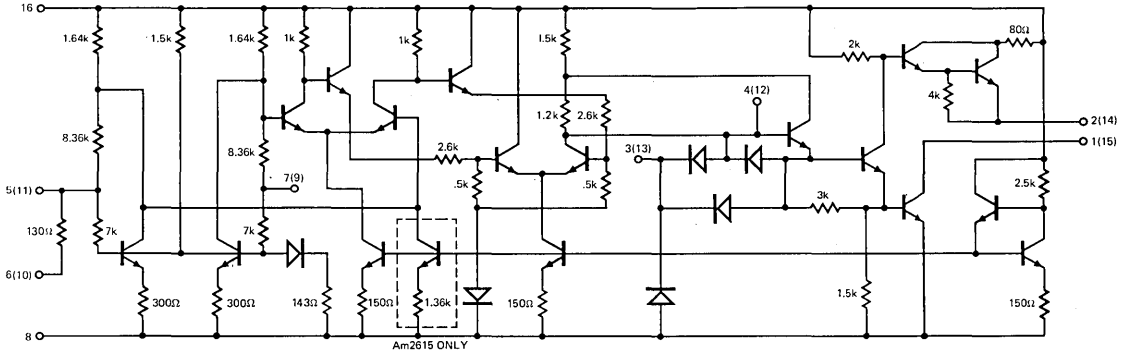
The Am2615 is identical to the Am9615 except for the input offset (threshold) voltage. The Am2615 has an input threshold of ~1.5V compatible with DTL & TTL logic. The Am9615 has an input threshold of ~0V. The Am2615 can directly replace the Am9615 and provides fail safe protection via the output going to a LOW state when the inputs are open or disconnected.

LOGIC DIAGRAM



V_{CC} = PIN 16
GND = PIN 8

CIRCUIT DIAGRAM

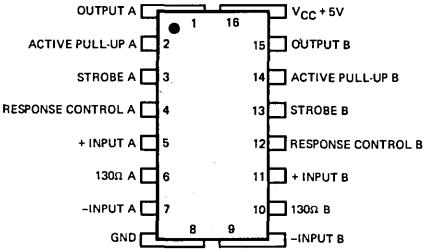


ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am2615	Molded DIP	0°C to +75°C	AM261559A
Am2615	Hermetic DIP	0°C to +75°C	AM261559E
Am2615	Hermetic DIP	−55°C to +125°C	AM261551E
Am2615	Hermetic Flat Pak	−55°C to +125°C	AM261551N
Am2615	Dice	See Note	AM2615XXD
Am9615	Molded DIP	0°C to +75°C	U6M961559X
Am9615	Hermetic DIP	0°C to +75°C	U7B961559X
Am9615	Hermetic DIP	−55°C to +125°C	U7B961551X
Am9615	Hermetic Flat Pak	−55°C to +125°C	U4L961551X
Am9615	Dice	Note	UXX9615XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +13.2 V
DC Strobe Input Voltage	−0.5 V to +5.5 V
DC Data Input Voltage	−20 V to + 20 V
Output Current, Into Outputs	30 mA
DC Input Current	maximum current is defined by DC Input Voltage

Am2615 ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Am261551X V_{CC} = 4.5 V to 5.5 V T_A = −55°C to +125°C (MIL grade)
Am261559X V_{CC} = 4.75 V to 5.25 V T_A = 0°C to +75°C (COM grade)

Parameters	Description	Test Conditions		LIMITS T_A = Min Min	Max	T_A = 25°C Min	Typ	Max	T_A = Max Min	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −5.0 mA V_{IN+} = +0.8 V, V_{IN-} = 0 V		2.4		2.4	3.2		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MAX I_{OH} = 15.0 mA V_{IN+} = +2.0 V, V_{IN-} = 0 V	MIL grade		0.40		.18	0.40		0.40	Volts
			COM grade		0.45		.25	0.45		0.45	
I_{CEX}	Output Leakage Current	V_{CC} = MIN V_{IN+} = 0 V V_{IN-} = 0 V	V_{CEX} = 12 V MIL grade V_{CEX} = 5.25 V COM grade		100			100		200	μA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX V_{OUT} = 0 V V_{IN+} = +0.8 V V_{IN-} = 0 V	MIL grade	−15	−80	−15	−39	−80	−15	−80	mA
			COM grade	−14	−100	−14	−39	−100	−14	−100	
I_{IL}	Input Load Current	V_{CC} = MAX V_{IN} = $V_{OL\ MAX}$, other input = V_{CC}			−0.9		−0.49	−0.7		−0.7	mA
$I_{IL(ST)}$	Strobe Input Low Current	V_{CC} = MAX V_{IN+} = +2.0 V V_{ST} = V_{OL} MAX V_{IN-} = 0 V			−2.4		−1.15	−2.4		−2.4	mA
$I_{IL(RC)}$	Response Control Input Load Current	V_{CC} = MAX V_{IN+} = +2.0 V V_{RC} = V_{OL} MAX V_{IN-} = 0 V					−1.2	−3.4			mA
V_{CM}	Common Mode Voltage	V_{CC} = 5.0 V V_{IN+} - V_{IN-} = 0.4 or 2.4 V		−15	+15	−15	±17.5	+15	−15	+15	V
$I_{IH(ST)}$	Strobe Input HIGH Current	V_{CC} = MIN V_{ST} = 4.5 V V_{IN+} = +0.8 V V_{IN-} = 0 V	MIL grade					2.0		5.0	μA
			COM grade					5.0		10.0	
R_{IN}	Input Resistor	V_{CC} = 5.0 V V_{IN+} = 0 V V_{RES} = 1.0 V	MIL grade			77	130	167			Ω
			COM grade			74	130	179			
V_{TH}	Differential Input Threshold Voltage	V_{CM} = 0 V		+0.8	+2.0	+0.8	+1.5	+2.0	+0.8	+2.0	V
I_{CC}	Power Supply Current	V_{CC} = MAX V_{IN+} = +2.0 V V_{IN-} = 0 V	MIL grade		50		28.7	50		50	mA
			COM grade		50		28.7	50		50	

Switching Characteristics (T_A = 25°C)

Parameters	Test Conditions	Am261551 Min	Typ	Max	Am261559 Min	Typ	Max	Units
t_{pd+} Turn Off Delay R_L = 3.9 kΩ	V_{CC} = 5.0 V, C_L = 30 pF Refer to figure 4		30	50		30	75	ns
t_{pd-} Turn On Delay R_L = 390 Ω			30	50		30	75	
t_{pd+} Turn Off Delay Strobe to Output	R_L = 3.9 kΩ, C_L = 30 pF		7	12		7	15	ns
t_{pd-} Turn On Delay Strobe to Output	R_L = 390 Ω		10	15		10	20	

Am9615 ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Am961551X V_{CC} = 4.5 V to 5.5 V T_A = −55°C to +125°C (MIL grade)
Am961559X V_{CC} = 4.75 V to 5.25 V T_A = 0°C to +75°C (COM grade)

Parameters	Description	Test Conditions			LIMITS T_A = Min Min	Max	T_A = 25°C Min	Typ	Max	T_A = Max Min	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −5.0 mA V_{IN+} = −0.5 V, V_{IN-} = 0 V			2.4		2.4	3.2		2.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MAX I_{OH} = 15.0 mA V_{IN+} = +0.5 V, V_{IN-} = 0		MIL grade		0.40		.18	0.40		0.40	Volts
				COM grade		0.45		.25	0.45		0.45	
I_{CEX}	Output Leakage Current	V_{CC} = MIN V_{IN+} = 0 V V_{IN-} = V_{CC}	V_{CEX} = 12 V	MIL grade		100			100		200	μA
			V_{CEX} = 5.25 V	COM grade								
I_{SC}	Output Short Circuit Current	V_{CC} = MAX V_{OUT} = 0 V V_{IN+} = −0.5 V V_{IN-} = 0 V		MIL grade	−15	−80	−15	−39	−80	−15	−80	mA
				COM grade	−14	−100	−14	−39	−100	−14	−100	
I_{IL}	Input Load Current	V_{CC} = MAX V_{IN} = $V_{OL\ MAX}$, other input = V_{CC}				−0.9		−0.49	−0.7		−0.7	mA
$I_{IL(ST)}$	Strobe Input Low Current	V_{CC} = MAX V_{ST} = $V_{OL\ MAX}$	V_{IN+} = +0.5 V V_{IN-} = 0 V			−2.4		−1.15	−2.4		−2.4	mA
$I_{IL(RC)}$	Response Control Input Load Current	V_{CC} = MAX V_{RC} = $V_{OL\ MAX}$	V_{IN+} = +0.5 V V_{IN-} = 0 V					−1.2	−3.4			mA
V_{CM}	Common Mode Voltage	V_{CC} = 5.0 V	V_{IN+} - V_{IN-} = ±2.0 V		−15	+15	−15	±17.5	+15	−15	+15	V
$I_{IH(ST)}$	Strobe Input HIGH Current	V_{CC} = MIN V_{ST} = 4.5 V V_{IN+} = −0.5 V V_{IN-} = 0 V		MIL grade					2.0		5.0	μA
				COM grade					5.0		10.0	
R_{IN}	Input Resistor	V_{CC} = 5.0 V V_{IN+} = 0 V V_{RES} = 1.0 V		MIL grade			77	130	167			Ω
				COM grade			74	130	179			
V_{TH}	Differential Input Threshold Voltage	V_{CM} = 0 V			−0.5	+0.5	−0.5	±0.02	+0.5	−0.5	+0.5	V
I_{CC}	Power Supply Current	V_{CC} = MAX V_{IN+} = +0.5 V V_{IN-} = 0 V		MIL grade		50		28.7	50		50	mA
				COM grade		50		28.7	50		50	

Switching Characteristics (T_A = 25°C)

Parameters	Test Conditions	Am961551X Min	Typ	Max	Am961559X Min	Typ	Max	Units
t_{pd+} Turn Off Delay R_L = 3.9 kΩ	V_{CC} = 5.0 V, C_L = 30 pF Refer to figure 4		30	50		30	75	ns
t_{pd-} Turn On Delay R_L = 390 Ω			30	50		30	75	
t_{pd+} Turn Off Delay Strobe to Output	R_L = 3.9 kΩ, C_L = 30 pF		7	12		7	15	ns
t_{pd-} Turn On Delay Strobe to Output	R_L = 390 Ω		10	15		10	20	

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH-signal level or when used with V_{CC} o indicate HIGH V_{CC} value.
Input.
L LOW, applying to a LOW signal level or when used with V_{CC} o indicate LOW V_{CC} value.
O Output.

OPERATIONAL TERMS:

I_{IL} Forward input load current, for unit input load.
I_{OH} Output HIGH current, forced out of output in V_{OH} test.
I_{OL} Output LOW current, forced into the output in V_{OL} test.
I_{IH} Reverse input load current.
Negative Current Current flowing out of the device.
I_{CC} The current drawn by the device under the maximum specified power supply.
Positive Current Current flowing into the device.
V_{IH} Minimum logic HIGH input voltage.
V_{IL} Maximum logic LOW input voltage.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

I_{CEX} Reverse output current with V_{CEX} applied to output.

I_{SC} Short circuit output current with V_{SC} applied to output.

V_{CM} Common mode voltage.

V_{TH} Input Differential Threshold Voltage referred from A+ to A− and from B+ to B−.

R_{IN} Internal Resistor available for terminataing 130 Ω transmission line.

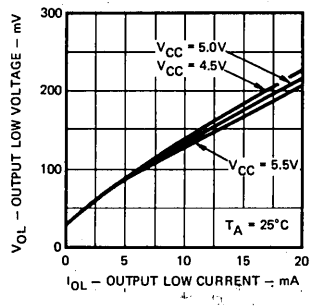
SWITCHING TERMS:

t_{pd+} The propagation delay from the differential voltage going below threshold to the LOW to HIGH output transition.

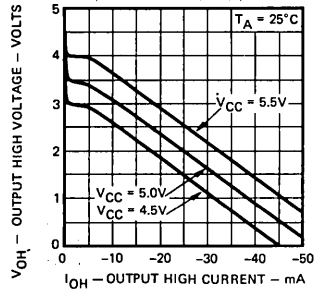
t_{pd-} The propagation delay from the differential voltage going above threshold to the HIGH to LOW output transition.

D. C. CHARACTERISTICS

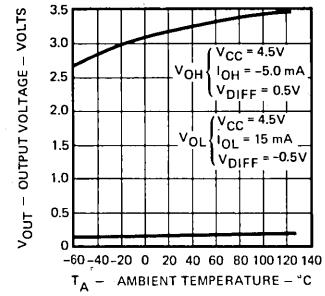
Output Low Voltage Versus Output Low Current



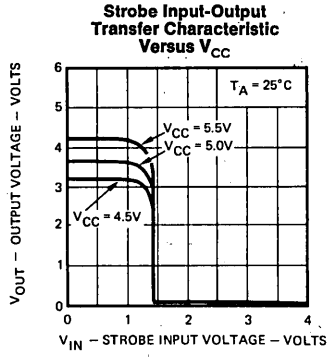
Output High Voltage Versus Output High Current



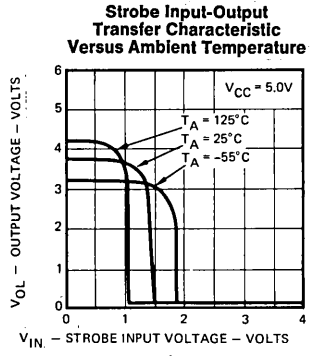
Output Voltage Versus Ambient Temperature



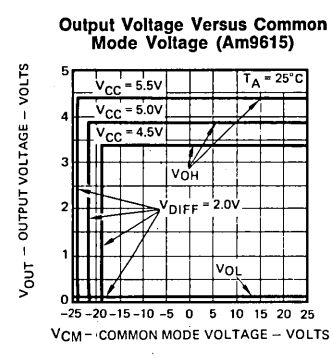
Strobe Input-Output Transfer Characteristic Versus V_{CC}



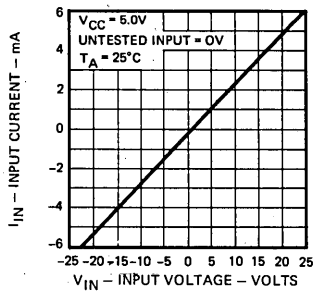
Strobe Input-Output Transfer Characteristic Versus Ambient Temperature



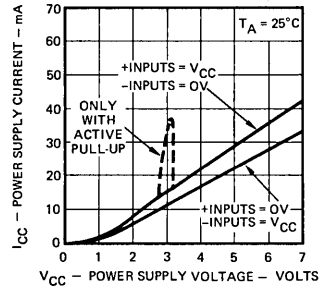
Output Voltage Versus Common Mode Voltage (Am9615)



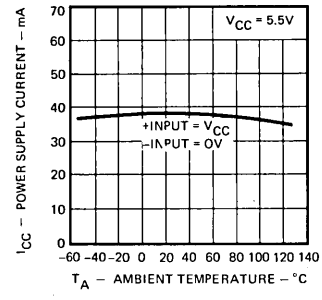
Input Current Versus Input Voltage



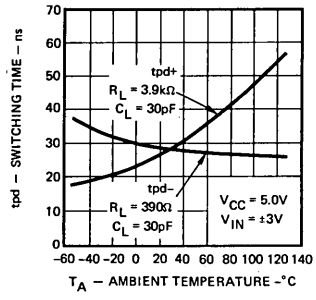
Power Supply Current Versus Power Supply Voltage



Power Supply Current Versus Ambient Temperature



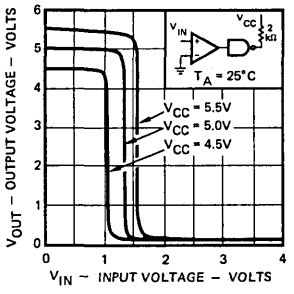
Switching Time Versus Ambient Temperature



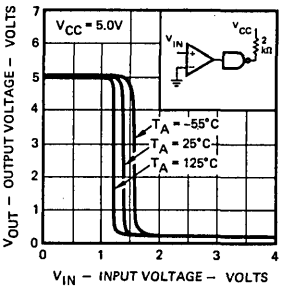
THRESHOLD CHARACTERISTICS

Am2615

Input-Output Transfer Characteristic Versus V_{CC}

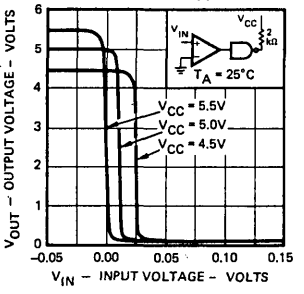


Input-Output Transfer Characteristic Versus Temperature

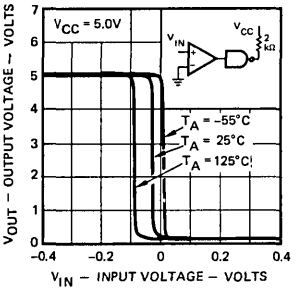


Am9615

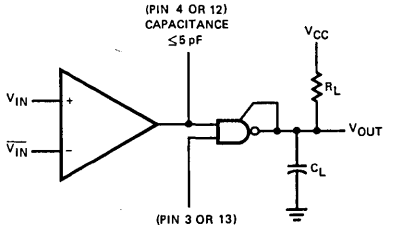
Input-Output Transfer Characteristic Versus V_{CC}



Input-Output Transfer Characteristic Versus Temperature



SWITCHING TIME TEST CIRCUIT & WAVEFORMS



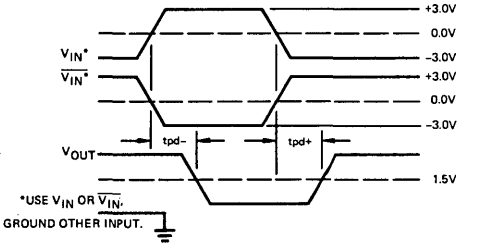
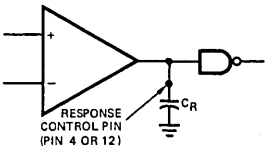
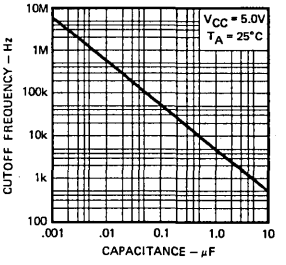


Figure 4

FREQUENCY RESPONSE CONTROL



Frequency Response Versus Capacitance

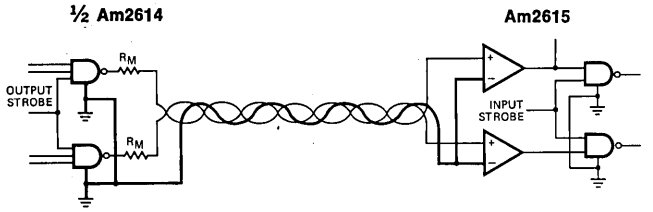


Am2615/9615 LOADING RULES

	Input/Output	Pin No.'s	Input Unit Load	Fanout Output HIGH	Fanout Output LOW
Receiver A	Out	1	—	o/c	10
	Active Pull-Up	2	—	83	—
	Response Control	3	—	—	—
	Strobe	4	1.5	—	—
	+ In	5	0.5	—	—
	130 Ω	6	—	—	—
	– In	7	0.5	—	—
Receiver B	GND	8	—	—	—
	– In	9	0.5	—	—
	130 Ω	10	—	—	—
	+ In	11	0.5	—	—
	Response Control	12	—	—	—
	Strobe	13	1.5	—	—
	Active Pull-Up	14	—	83	—
	Out	15	—	o/c	10
	V_{CC}	16	—	—	—

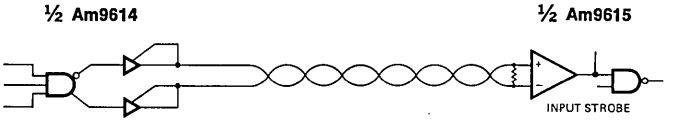
Am2615 STANDARD USAGE

Single-Ended-Back Matched Operation With Common Ground

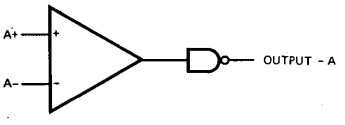


Am9615 STANDARD USAGE

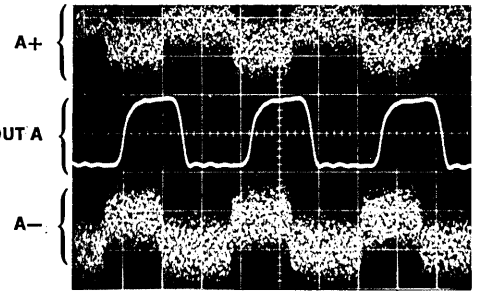
Differential Operation



Photograph of an Am9615 switching differential data in the presence of high common mode noise.



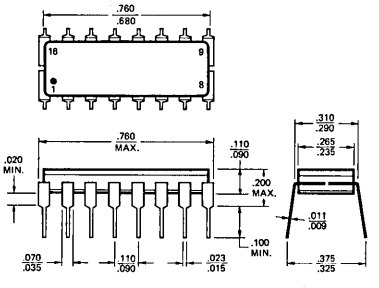
Vertical = 2.0 V/Div. Horizontal = 50 ns/Div.



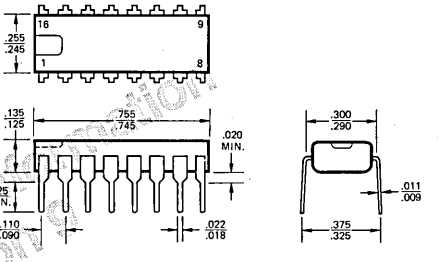
PHYSICAL DIMENSIONS

Dual-In-Line

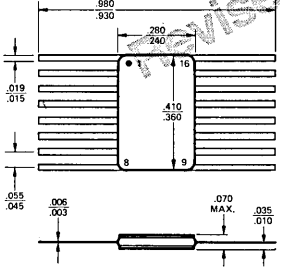
Hermetic



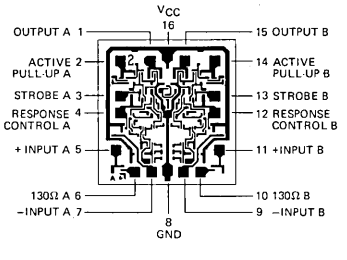
Molded



Flat Package



Metallization and Pad Layout



ADVANCED MICRO DEVICES INC.
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Am78/8831•Am78/8832
Three-State Line Driver

Distinctive Characteristics

- Three-State Line Drivers pin-for-pin equivalent to the DM78/8831 and DM78/8832
- Mode control for quad single-ended or dual differential operation
- Common bus operation
- High-drive capability
- 40mA sink and source current
- Series 54/74 compatible
- 13ns typical propagation delay
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

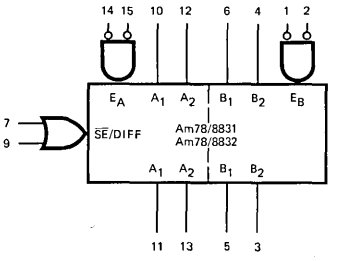
The Am78/8831 and Am78/8832 line drivers can be used either as a quad single-ended driver or as a dual differential driver. Each driver has a three-state output making the device particularly suitable for party-line operation where several drivers are directly connected to the same bus. The Am78/8832 does not have the V_{CC} clamp diodes found on the Am74/8831.

When used for single-ended operation the two differential/single-ended control inputs are held LOW. The device then operates as four independent non-inverting drivers. For differential working at least one differential/single-ended control input is held HIGH. The A-channel inputs are connected together and the B-channel inputs are connected together. Signal inputs will then pass non-inverted to the A_2 and B_2 outputs and inverted on the A_1 and B_1 outputs.

For party-line operation outputs of different channels are tied together, and outputs of all channels except one are forced into the third high impedance state by having at least one of the channel disable inputs HIGH. The channel that is enabled has both channel disable inputs LOW, and the low-output impedance of this output at both logic levels controls the level of the bus, provides good capacitance drive and insures good waveform integrity.

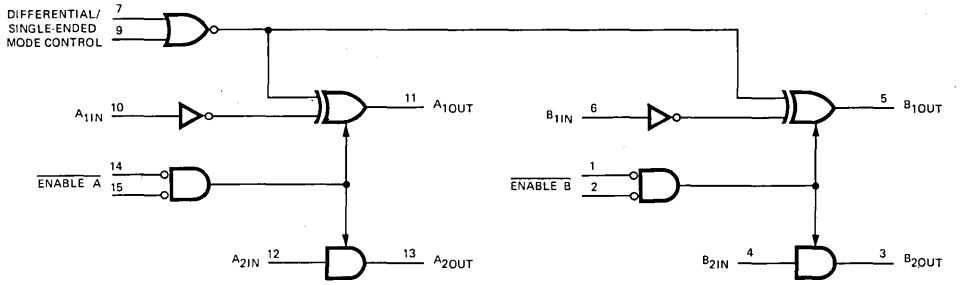
The channel which is enabled can conveniently be selected by a decoding matrix using Am9301 1-of-10 or Am9311 1-of-16 active LOW output decoders. The high drive capability at both logic levels enables drivers to drive a low impedance line and still supply the inverse leakage current of several disabled drivers.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

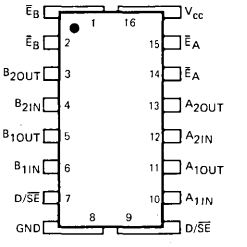
LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Am78/8831 Order Number	Am78/8832 Order Number
Molded DIP	0°C to +75°C	DM8831N	DM8832N
Hermetic DIP	0°C to +75°C	DM8831J	DM8832J
Dice	0°C to +75°C	AM8831XC	AM8832XC
Hermetic DIP	−55°C to +125°C	DM7831J	DM7832J
Hermetic Flat Pak	−55°C to +125°C	DM7831F	DM7832F
Dice	−55°C to +125°C	AM7831XM	AM8832XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA
Time that 2 Bus-Connected Devices May Be in Opposite Low Impedance States Simultaneously	∞

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am8831, Am8832 T_A = 0°C to +75°C V_{CC} = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am7831, Am7832 T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL) MIN. = 4.5V MAX. = 5.5V

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −40 mA	1.8	2.8		Volts
			Am7831, 32 I_{OH} = −2 mA	2.4	3.1		
			Am8831, 32 I_{OH} = −5.2 mA				
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 40 mA		0.29	0.5	Volts
			I_{OL} = 32 mA		0.2	0.4	
V_{IH}	Input HIGH Level Voltage	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level Voltage	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_L	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V			−1.0	−1.6	mA
I_{IH}	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V			6.0	40	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V				1.0	mA
I_{LK}	Output Leakage Current	V_{CC} = MAX., $\overline{E}$ = 2.4 V, V_{OUT} = 2.4 V			5	40	µA
		V_{CC} = MAX., $\overline{E}$ = 2.4 V, V_{OUT} = 0.4 V			−5	−40	
V_I	Input Clamp Diode Voltage	V_{CC} = 5.0 V, I_I = −12 mA, T_A = 25°C				−1.5	Volts
V_O	Output Clamp Diode Voltage	V_{CC} = 5.0 V, I_I = 12 mA, T_A = 25°C Am78/8831 Only				V_{CC} + 1.5V	Volts
V_O	Output Substrate Diode Voltage	V_{CC} = 5.0 V, I_I = −12 mA, T_A = 25°C				−1.5	Volts
I_{SC} (Note 2)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V, T_A = MAX.		−40		−120	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.			57	90	mA

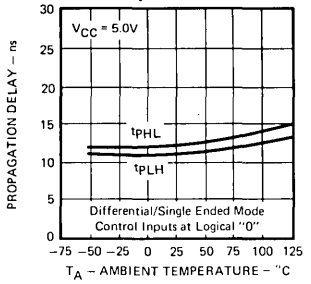
Notes: 1. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2. Only one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°)

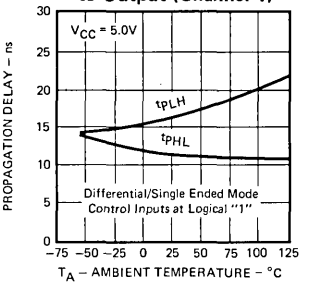
Parameters	Description	Min.	Typ.	Max.	Units
t_{PLH}	Delay from Inputs A_1, A_2, B_1, B_2 and Single-Ended/ Diff. Control to Output		13	25	ns
t_{PHL}			13	25	ns
t_{HZ}	Delay from Output Enable to Output		6	12	ns
t_{LZ}			14	22	ns
t_{ZH}	Delay from Output Enable to Output		14	22	ns
t_{ZL}			18	27	ns

TYPICAL PERFORMANCE CHARACTERISTICS

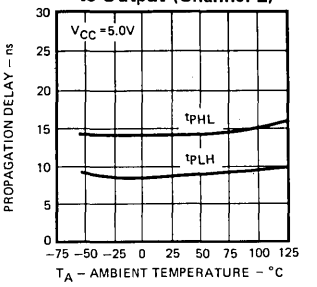
Propagation Delay from Input to Output (Channel 1)



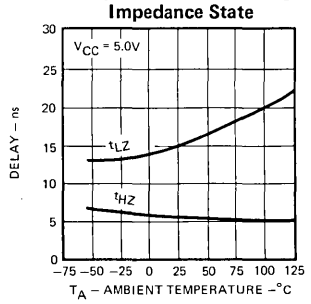
Propagation Delay from Input to Output (Channel 1)



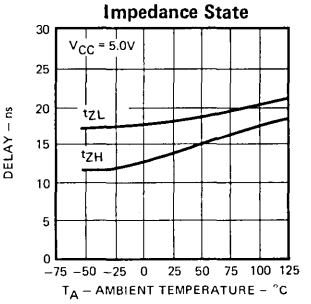
Propagation Delay from Input to Output (Channel 2)



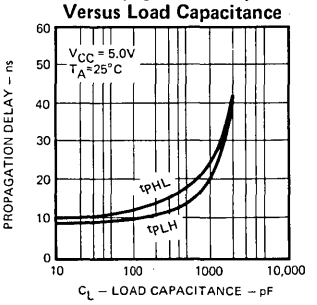
Delay from Disable to High Impedance State



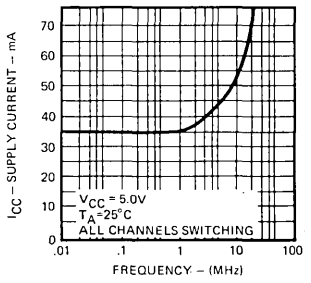
Delay from Disable to Low Impedance State



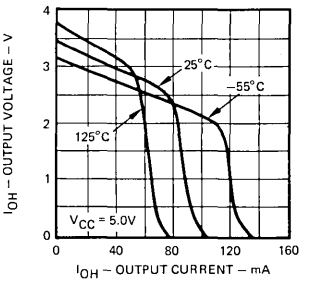
Propagation Delay Versus Load Capacitance



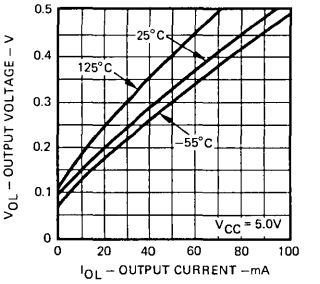
Total Supply Current Versus Frequency



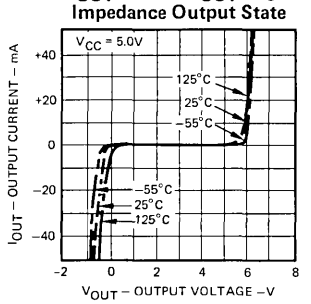
Logical "1" Output Voltage Versus Source Current



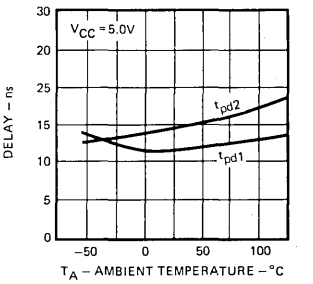
Logical "0" Output Voltage Versus Sink Current

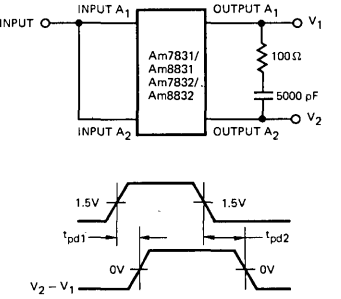


I_{OUT} Versus V_{OUT} High Impedance Output State

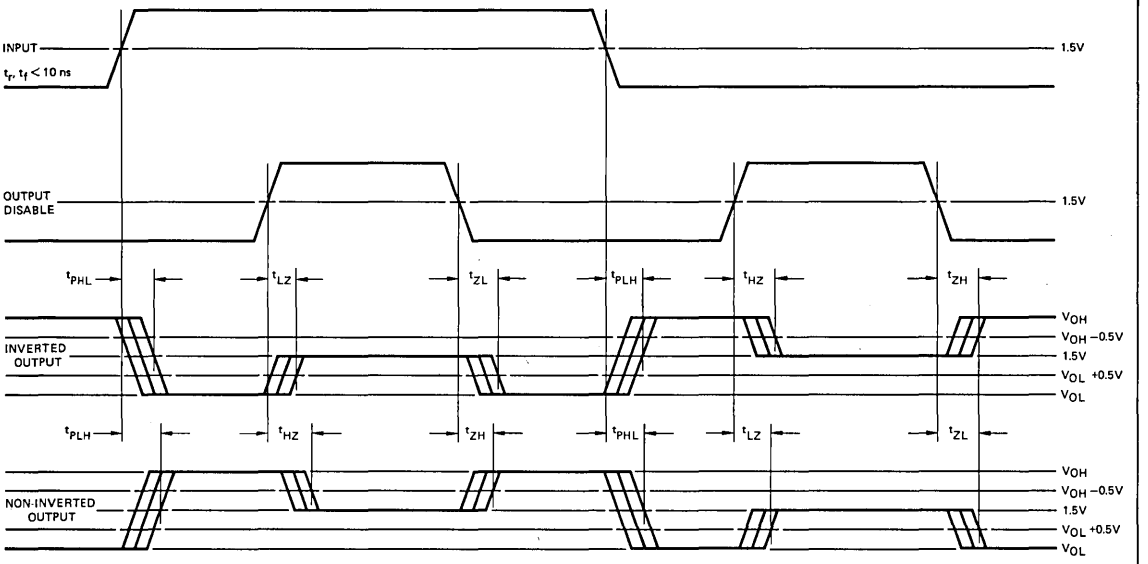


Propagation Delay in Differential Mode





SWITCHING TIME WAVEFORMS AND TEST CIRCUIT

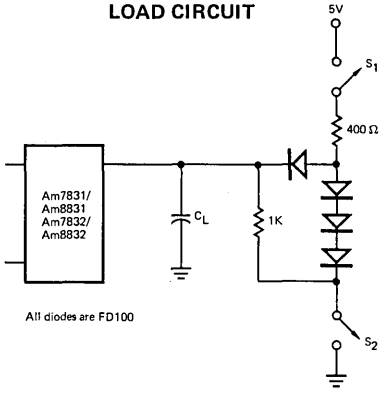


NOTE: V_{OL} and V_{OH} refer to actual voltages on output LOW and HIGH states.

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS	WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY		DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L		DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H			

LOAD CIRCUIT



All diodes are FD100

	Switch S_1	Switch S_2	C_L
t_{PLH}	closed	closed	50 pF
t_{PHL}	closed	closed	50 pF
t_{HZ}	closed	closed	* 5 pF
t_{LZ}	closed	closed	* 5 pF
t_{ZL}	closed	open	50 pF
t_{ZH}	open	closed	50 pF

*Jig Capacitance

DEFINITION OF SWITCHING TERMS

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{HZ} The delay time from a control input change to the three-state output HIGH-level to high-impedance transition.

t_{LZ} The delay time from a control input change to the three-state output LOW-level to high-impedance transition.

t_{ZH} The delay time from a control input change to the three-state output high impedance to HIGH-level transition.

t_{ZL} The delay time from a control input change to the three-state output high-impedance to LOW-level transition.

TRUTH TABLE
(Shown for A Channels Only)

SINGLE-ENDED/ DIFF CONTROL		A ENABLE		IN A_1	OUT A_1	IN A_2	OUT A_2
L	L	L	L	A_1	A_1	A_2	A_2
H	X	L	L	A_1	$\overline{A}_1$	A_2	A_2
X	H	L	L	A_1	$\overline{A}_1$	A_2	A_2
X	X	H	X	X	F	X	F
X	X	X	H	X	F	X	F

H = HIGH Voltage Level
X = Don't Care
L = LOW Voltage Level
F = Floating Output

TABLE I

MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 54/7400	1	1
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

TABLE III

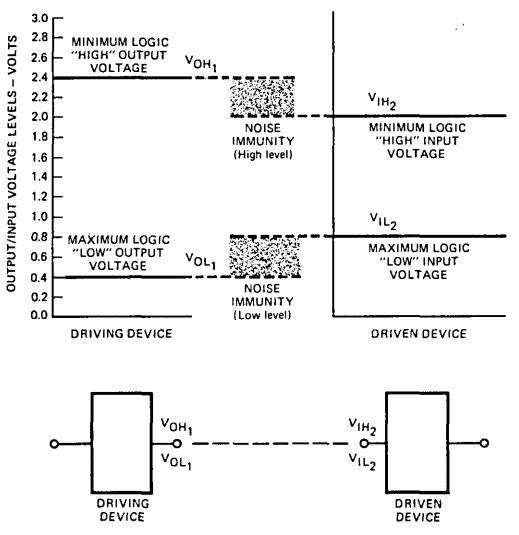
LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{\text{Enable B}}$	1	1	–	–
$\overline{\text{Enable B}}$	2	1	–	–
B_2 Out	3	–	1000	25
B_2 In	4	1	–	–
B_1 Out	5	–	1000	25
B_1 In	6	1	–	–
$\overline{\text{SE}}$/Diff	7	1	–	–
GND	8	–	–	–
$\overline{\text{SE}}$/Diff	9	1	–	–
A_1 In	10	1	–	–
A_1 Out	11	–	1000	25
A_2 In	12	1	–	–
A_2 Out	13	–	1000	25
$\overline{\text{Enable A}}$	14	1	–	–
$\overline{\text{Enable A}}$	15	1	–	–
V_{CC}	16	–	–	–

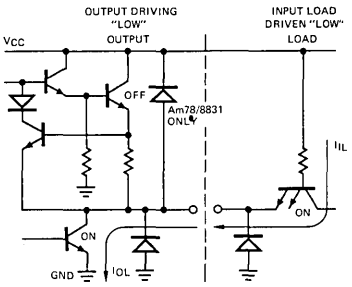
TABLE II

INPUT/OUTPUT INTERFACE CONDITIONS

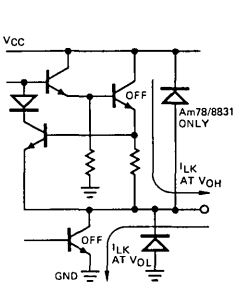
Voltage Interface Conditions – LOW & HIGH



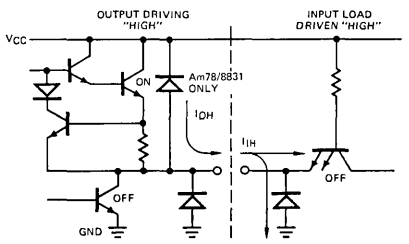
Current Interface Conditions – LOW



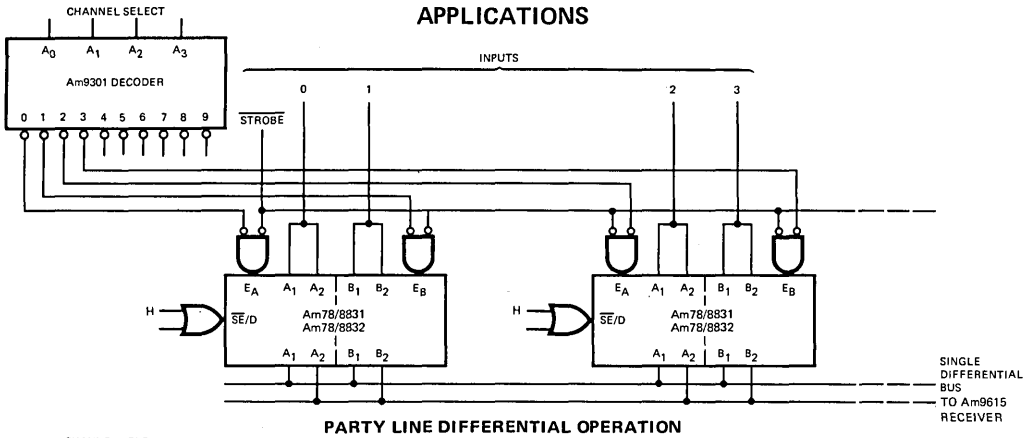
Current Interface Conditions – FLOATING



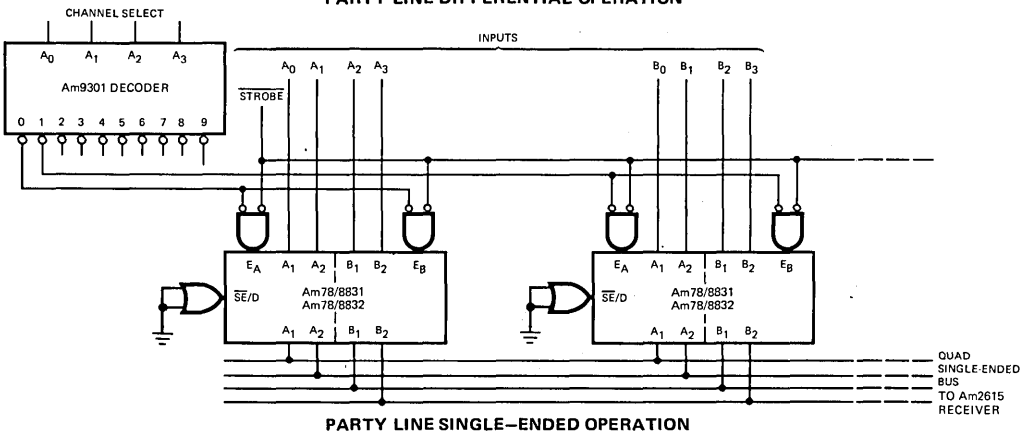
Current Interface Conditions – HIGH



APPLICATIONS



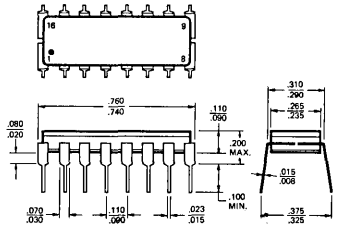
PARTY LINE DIFFERENTIAL OPERATION



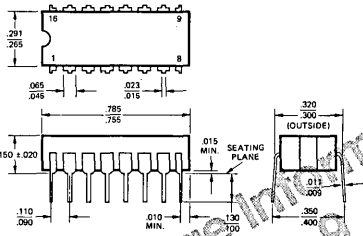
PARTY LINE SINGLE–ENDED OPERATION

PHYSICAL DIMENSIONS
Dual-In-Line

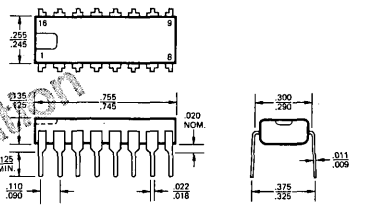
Hermetic



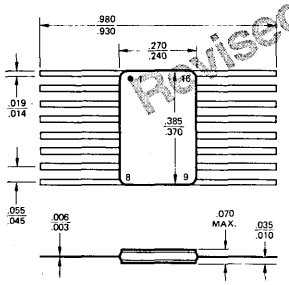
Ceramic



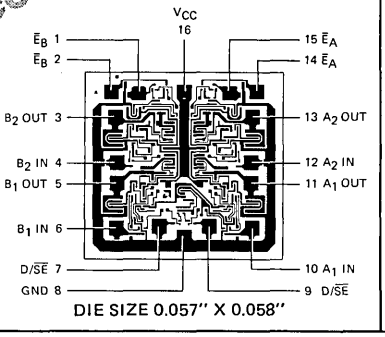
Molded



Flat Package



Metallization and Pad Layout



DIE SIZE 0.057" X 0.058"

ADVANCED MICRO DEVICES INC.
901 Thompson Place
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TWX: 910-339-9280
TELEX: 34-6306

Am9616
RS-232C Line Driver

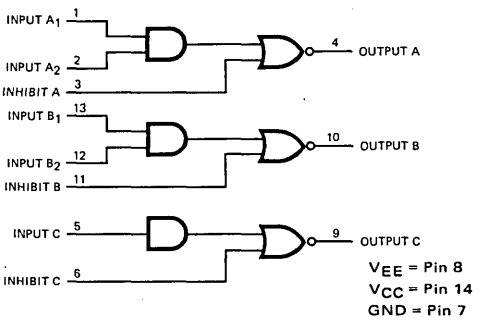
Distinctive Characteristics

- Conforms to EIA RS-232C and CCITT V.24 specifications
- Short circuit protected output
- Internal slew rate limiting
- Supply independent output swing
- 100% reliability assurance testing in compliance with MIL-STD-883
- TTL/DTL compatible input

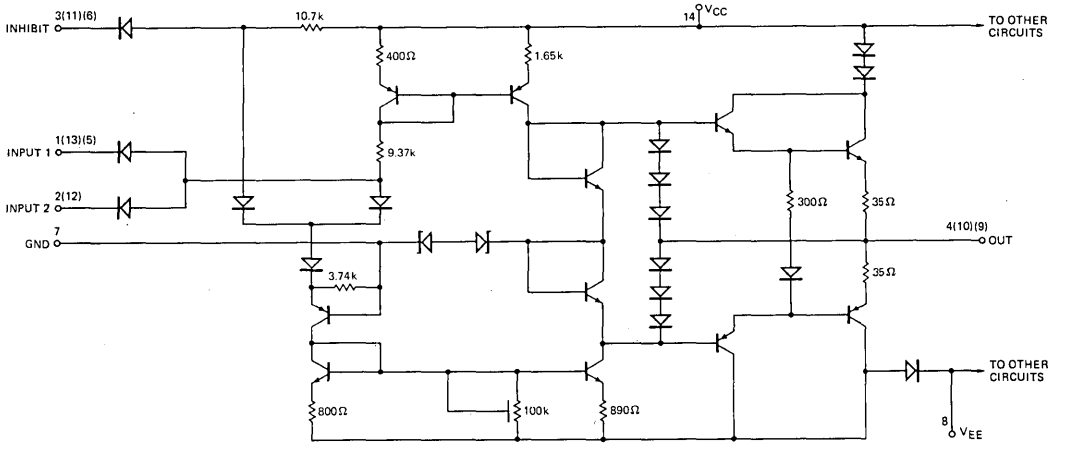
FUNCTIONAL DESCRIPTION

The Am9616 is a triple line driver specifically designed to meet the EIA RS-232C and CCITT V.24 electrical interface requirements. Each driver accepts DTL/TTL logic levels and converts them to EIA/CCITT levels for data transmission between equipment. The output slew rate of each driver is internally limited, but can be lowered by an external capacitor. All outputs are short circuit protected, and protected against fault conditions specified in RS-232C. A HIGH logic level on the inhibit input forces the driver output to V_{OL} or mark state.

LOGIC SYMBOL



CIRCUIT DIAGRAM
(One Driver Shown)

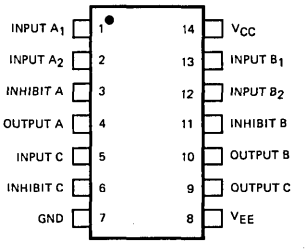


Am9616 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
14-Pin Hermetic DIP	0°C to +75°C	9616DC
14-Pin Molded DIP	0°C to +75°C	9616PC
Dice	0°C to +75°C	9616XC

Revised Ordering Information See section 9

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	0°C to +75°C
Supply Voltage to Ground Potential	
V_{CC}	+15 V
V_{EE}	−15 V
DC Voltage Applied to Outputs	±15 V
DC Input Voltage	−1.5 V to +6 V
Lead Temperature (Soldering, 30 sec.)	300°C

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

T_A = 0°C to +75°C, V_{CC} = +12 V ± 10%, V_{EE} = −12 V ± 10%, R_L = 3 kΩ unless otherwise noted.

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{IN_1} or V_{IN_2} = $V_{INHIBIT}$ = 0.8 V	+5.0	+6.0	+7.0	Volts
V_{OL}	Output LOW Voltage	V_{IN_1} = V_{IN_2} = $V_{INHIBIT}$ = 2.0 V	−7.0	−6.0	−5.0	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage			0.8	Volts
I_{IL}	Input LOW Current	V_{IN_1} = V_{IN_2} = 0.4 V or $V_{INHIBIT}$ = 0.4 V		−1.2	−1.6	mA
I_{IH}	Input HIGH Current	V_{IN_1} = V_{IN_2} = 2.4 V or $V_{INHIBIT}$ = 2.4 V			40	μA
I_{SC}	Output Short Circuit Current (Positive)	R_L = 0 Ω V_{IN_1} or V_{IN_2} = $V_{INHIBIT}$ = 0.8 V	−8	−17	−30	mA
I_{SE}	Output Short Circuit Current (Negative)	R_L = 0 Ω V_{IN_1} or V_{IN_2} = $V_{INHIBIT}$ = 2.0 V	+8	+17	+30	mA
I_{CC}	Total Positive Supply Current	V_{IN_1} = V_{IN_2} = $V_{INHIBIT}$ = 0.8 V		15	22	mA
		V_{IN_1} = V_{IN_2} = $V_{INHIBIT}$ = 2.0 V		7.5	13	
I_{EE}	Total Negative Supply Current	V_{IN_1} = V_{IN_2} = $V_{INHIBIT}$ = 0.8 V		0	−1	mA
		V_{IN_1} = V_{IN_2} = $V_{INHIBIT}$ = 2.0 V		−15	−22	

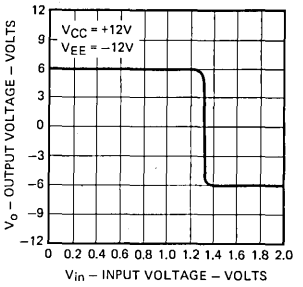
Note 1. Typical values are at V_{CC} = 12 V, V_{EE} = −12 V, T_A = 25°C

Switching Characteristics (T_A = 25°C, V_{CC} = +12.0 V, V_{EE} = −12.0 V)

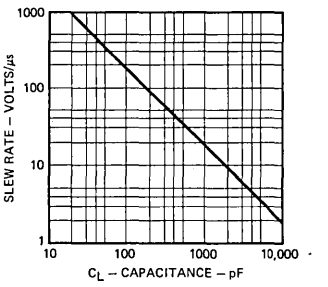
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Delay from Input LOW to Output HIGH	C_L = 15 pF, R_L = ∞		320	650	ns
t_{PHL}	Delay from Input HIGH to Output LOW			320	650	ns
	Positive Slew Rate	0 pF ≤ C_L ≤ 2500 pF, R_L ≥ 3 kΩ	4.0	15	30	V/μs
	Negative Slew Rate		−30	−15	−4.0	V/μs

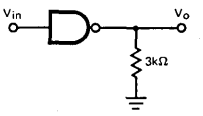
TYPICAL CHARACTERISTICS

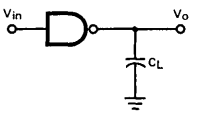
Transfer Characteristics



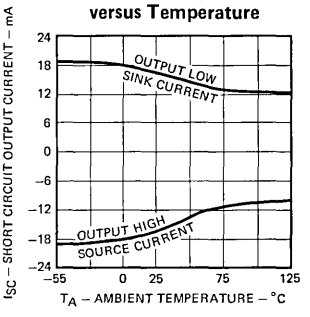
Output Slew Rate versus Load Capacitance



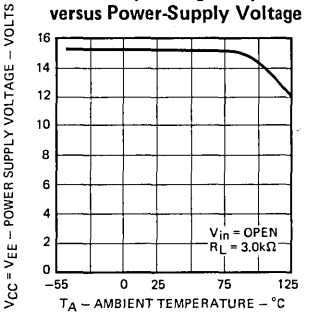




Short-Circuit Output Current versus Temperature



Maximum Operating Temperature versus Power-Supply Voltage



DEFINITION OF TERMS

FUNCTIONAL TERMS

RS-232C A specification of the Electronic Industries Association that defines the electrical characteristics of data signals transmitted between two pieces of digital equipment.

R_L Load resistance. The DC resistance between the driver output and ground.

MIL-188C A Military specification that defines the electrical interface and characteristics of data signals transmitted between two pieces of digital equipment.

CCITT V.24 A European specification similar to the MIL-188C and RS-232 specifications.

ELECTRICAL TERMS

V_{OH} Output HIGH voltage. The voltage on the output when the output is HIGH.

V_{OL} Output LOW voltage. The voltage on the output when the output is LOW.

V_{IH} Input HIGH level. The voltage above which the driver is guaranteed to sense a HIGH level.

V_{IL} Input LOW level. The voltage below which the driver is guaranteed to sense a LOW logic level.

I_{IL} Input LOW current. The current that flows out of the input when the input is at a LOW logic level.

I_{IH} Input HIGH current. The current that flows into the input when the input is at a HIGH logic level.

I_{SC} Output short circuit current. The current that flows between the output and ground when the output is shorted to ground and the input is either HIGH or LOW.

I_{CC} The positive power supply current in the V_{CC} supply.

I_{EE} The negative power supply current in the V_{EE} supply.

Slew Rate The rate, in volts per microsecond at which the output can change from one logic level to another.

SWITCHING TERMS

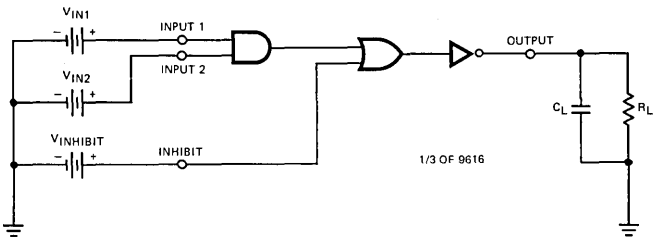
t_{PLH} The delay from a HIGH-to-LOW transition on an input to a LOW-to-HIGH transition on an output. Measured from the 1.5-volt level on the input to the 0-volt level on the output.

t_{PHL} The delay from a LOW-to-HIGH transition on the input(s) to a HIGH-to-LOW transition on the output. Measured from the 1.5-volt level on the input to the 0-volt level on the output.

t_r Output rise time. The time required for the output to change from 10% of (V_{OH} - V_{OL}) to 90% of (V_{OH} - V_{OL}), above V_{OL}.

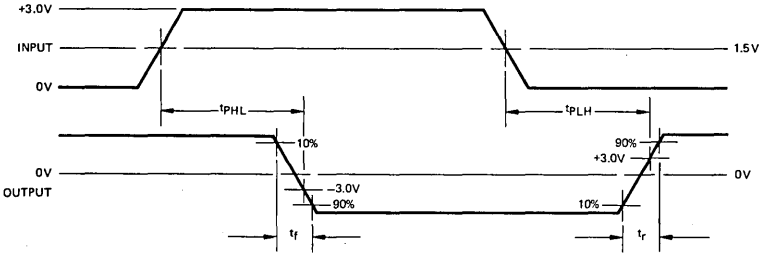
t_f Output fall time. The time required for the output to change from 90% of (V_{OH} - V_{OL}) to 10% of (V_{OH} - V_{OL}), above V_{OL}.

SWITCHING TEST CIRCUIT



Note: Omit V_{IN2} for channel "C".

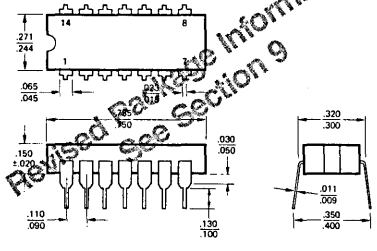
VOLTAGE WAVEFORMS



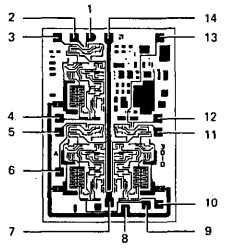
Pulse Generator Rise Time = 10 ± 5ns.

PHYSICAL DIMENSIONS

Ceramic DIP



Metallization and Pad Layout



DIE SIZE 0.069" x 0.103"

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Am9617
RS-232C Line Receiver

Distinctive Characteristics

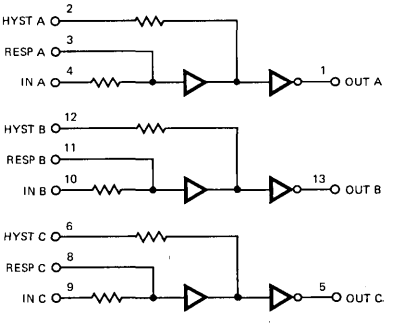
- Compatible with EIA RS-232C and CCITT V24 specifications.
- Input signal range ±30 volts.
- Variable hysterisis
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Includes response control input and built-in hysterisis.

FUNCTIONAL DESCRIPTION

The Am9617 is a triple line receiver that meets both the CCITT TV24 and EIA RS-232C specifications. Each receiver has a single data input that can accept signal swings of up to ±30V. The output of each receiver is TTL/DTL compatible, and includes a 2kΩ resistor pull-up to V_{CC}. Each receiver has a hysterisis input so that the hysterisis can be controlled by means of a series resistor between the HYST input and a response control input RESP.

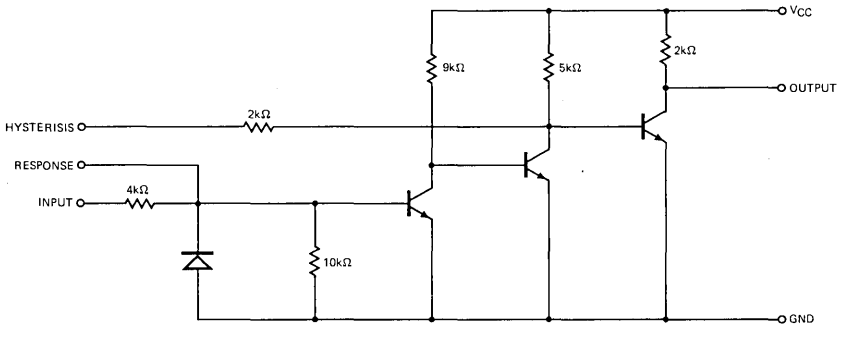
Because of this hysterisis in switching thresholds, the device can receive signals with superimposed noise or with slow rise and fall times without generating oscillations on the output. The threshold levels may be offset by a constant voltage by applying a DC bias to the response control input. A capacitor added to the response control input will reduce the frequency response of the receiver for applications in the presence of high frequency noise spikes. The companion line driver is the Am9616.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

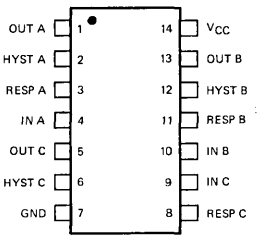
CIRCUIT DIAGRAM
(One Receiver)



Am9617 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
14-Pin Molded DIP	0°C to +75°C	9617PC
14-Pin Ceramic DIP	0°C to +75°C	9617DC
Dice	0°C to +75°C	9617XX

CONNECTION DIAGRAM
Top View



NOTE: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +175°C
Temperature (Ambient) Under Bias	0°C to +75°C
Supply Voltage to Ground Potential (Pin 14 to Pin 7) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
Input Signal Range	−30 V to +30 V
Output Current, Into Outputs	30 mA
DC Input Current	Defined by Input Voltage Limits

ELECTRICAL CHARACTERISTICS

T_A = 25°C V_{CC} = 5.0 V ±5% Response control pin open unless otherwise specified.

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
R_{IN}	Input Resistance	V_{IN} = ±25 V	3.0	4.0	7.0	kΩ
V_{IN}	Open Circuit Input Voltage			0.2	2.0	Volts
V_{OH}	Output HIGH Voltage	I_{OH} = −0.2 mA, V_{CC} = 4.5 V V_{IN} = −3.0 V, 0 V or Open Circuit	2.4	3.0		Volts
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA, V_{CC} = 4.5 V V_{IN} = +3.0 V		0.3	0.4	Volts
V_{IH}	Input HIGH Level Threshold	RESP-HYST Connected	1.75	2.0	2.25	Volts
V_{IL}	Input LOW Level Threshold	RESP-HYST Connected	0.75	0.85	1.25	Volts
V_{IO}	Open Loop Input Threshold		0.4	1.0	1.2	Volts
I_{IL}	Input LOW Current	V_{IN} = −25 V	−3.6		−8.0	mA
I_{IH}	Input HIGH Current	V_{IN} = +25 V	3.6		8.0	mA
I_{SC}	Output Short Circuit Current	V_{IN} = 0.0 V, V_{OUT} = 0.0 V		2.5		mA
I_{CC}	Power Supply Current	V_{IN} = 5.0 V, V_{CC} = 5.5 V		12	18	mA

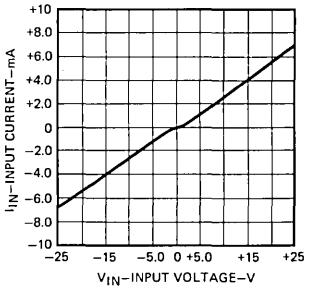
Note 1. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.

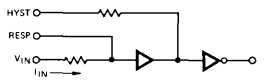
Switching Characteristics (T_A = 25°C, response control pin open, C_L = 15 pF)

Parameters	Definition	Test Conditions	Min.	Typ.	Max.	Units
t_{pd+}	Delay from Input LOW to Output HIGH	R_L = 3.9 kΩ		25	85	ns
t_{pd-}	Delay from Input HIGH to Output LOW	R_L = 390 Ω		25	50	ns
t_r	Output Rise Time (10% to 90%)	R_L = 3.9 kΩ		120	175	ns
t_f	Output Fall Time (90% to 10%)	R_L = 390 Ω		15	40	ns

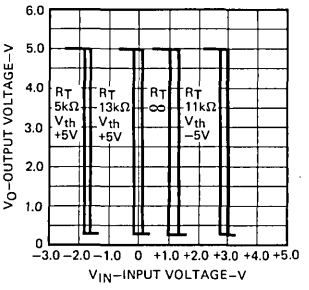
TYPICAL CHARACTERISTICS

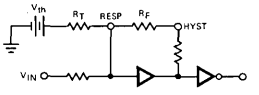
Input Current



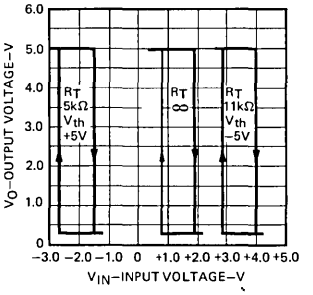


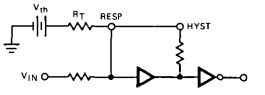
RF = 8k Input Threshold Voltage Adjustment



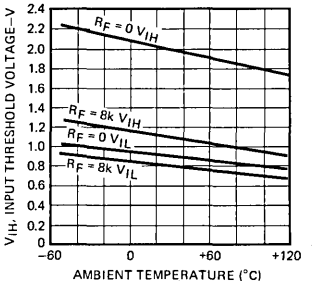


RF = 0 Input Threshold Voltage Adjustment

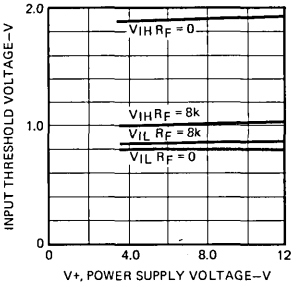




Input Threshold Voltage Versus Temperature



Input Threshold Versus Power-Supply Voltage



DEFINITION OF TERMS

FUNCTIONAL TERMS

Response Control Pin A pin available on each receiver that allows the user to set the switching thresholds and frequency response of the receiver.

Threshold Voltage The voltage level on the input that will cause the output to change state. Because the device exhibits hysterisis, the LOW level input threshold is different from the HIGH level input threshold. Both thresholds can be moved by applying a bias to the response control pin.

RS-232C A specification of the Electronic Industries Association that defines the electrical characteristics of data signals transmitted between two pieces of digital equipment.

Input Signal Range The permitted range of DC voltages that can be applied to the receiver input without damage to the device.

Hysterisis Control Pin This pin is available so that the amount of hysterisis in the receiver can be controlled by placing a series resistor between the RESP input and HYST input.

CCITTV 24 A European specification similar to the EIA RS-232 specification.

ELECTRICAL TERMS

V_{OH} Output HIGH voltage. The voltage on the output when the output is HIGH.

V_{OL} Output LOW voltage. The voltage on the output when the output is LOW.

V_{IH} Input HIGH threshold. The voltage that must be applied to the input to cause the output to switch from a HIGH to a LOW.

V_{IL} Input LOW threshold. The voltage that must be applied to the input to cause the output to switch from a LOW to a HIGH.

V_{IN} Input voltage.

V_{IO} Input Threshold Voltage with the RESP, HYST inputs *open circuit.*

I_{IH} Input HIGH current. The current that will flow into the input when a HIGH level is present on the input.

I_{IL} Input LOW current. The current that will flow out of the input when a LOW logic level is present on the input.

I_{OH} Output HIGH current. The current drawn out of the output when the output is HIGH.

I_{OL} Output LOW current. The current forced into the output when the output is LOW.

I_{SC} Output Short Circuit Current. The current that flows out of the output when the output is grounded.

I_{CC} Current drawn from the V_{CC} power supply.

R_{IN} Input Resistance measured over the input voltage range of ±25 volts.

SWITCHING TERMS

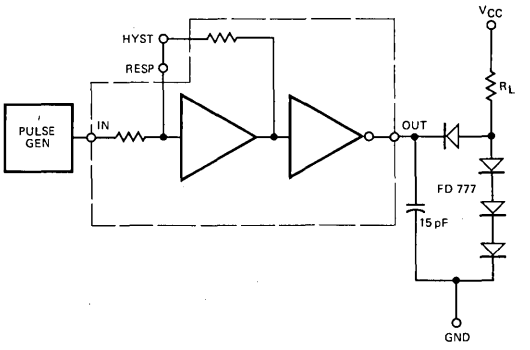
t_{pd+} The delay from a HIGH-to-LOW transition on the input to a LOW-to-HIGH transition on the output.

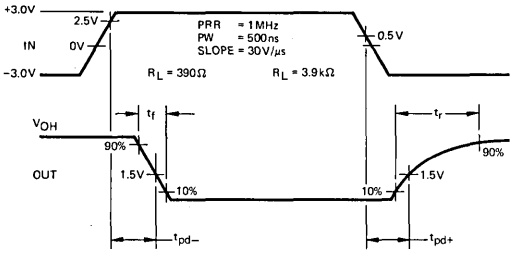
t_{pd-} The delay from a LOW-to-HIGH transition on the input to a HIGH-to-LOW transition on the output.

t_r Rise Time. The time required for the output to rise from 10% of the difference between V_{OL} and V_{OH} above V_{OL} to 90% of the difference between V_{OL} and V_{OH} above V_{OL}.

t_f Fall Time. The time required for the output to fall from 90% of the difference between V_{OL} and V_{OH} above V_{OL} to 10% of the difference between V_{OL} and V_{OH} above V_{OL}.

SWITCHING TIME TEST CIRCUIT & WAVEFORMS

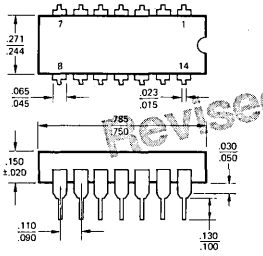




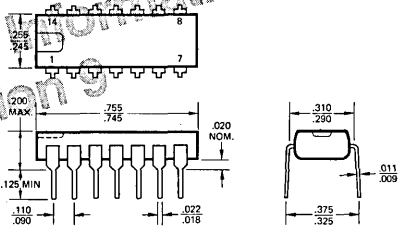
NOTE: Wiring capacitance should be minimized between Outputs, Hysterisis and Response Pins.

PHYSICAL DIMENSIONS
Dual-In-Line

Ceramic DIP

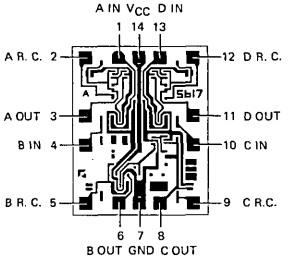


Molded DIP



Metallization and Pad Layout

DIE SIZE 0.047" x 0.059"



ADVANCED MICRO DEVICES INC.
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TELEX: 34-6306

Am9620
Dual Differential Line Receiver

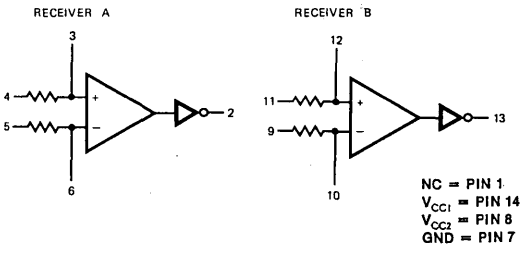
Distinctive Characteristics:

- Dual Differential Receiver
- DTL, TTL compatible
- High common-mode voltage range (±15 volts)
- Wire AND capability
- 100% reliability assurance testing in compliance with MIL STD 883.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Available in highly reliable molded, hermetic dual-in-line or hermetic flat package

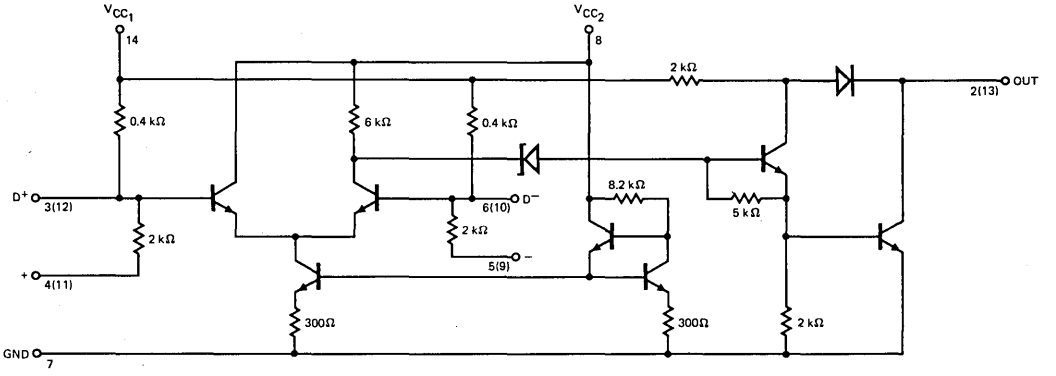
FUNCTIONAL DESCRIPTION

The Am9620 is a dual differential line receiver designed to receive digital data from transmission lines. The receiver produces an undisturbed output for ±500mV of differential data on the inputs in the presence of up to ±15V of common mode noise voltages. The device has a DTL, TTL compatible output which can be AND tied with other receiver outputs. In addition to attenuated inputs which are normally used, the receiver has direct inputs which allow the input attenuation and response time to be changed by use of external components.

LOGIC DIAGRAM



CIRCUIT DIAGRAM

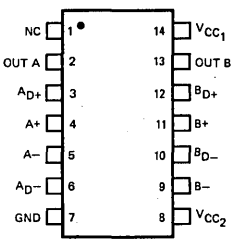


Am9620 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	U6E962059X
Hermetic DIP	0°C to +75°C	U6A962059X
Hermetic DIP	−55°C to +125°C	U6A962051X
Hermetic Flat Pak	−55°C to +125°C	U3I962051X
Dice	See Note	UXX9620XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC1} Pin Potential to Ground Pin	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +13.2 V
V_{CC2} Pin Potential to Ground Pin	V_{CC1} to +15 V
DC Data Input Voltage	−20 V to +20 V
Output Current, Into Outputs	30 mA
Input Voltage Referred to Ground (Attenuator Inputs)	±20 V

ELECTRICAL CHARACTERISTICS

Am962051X - T_A = −55°C to +125°C V_{CC1} = 5.0V ±10%, V_{CC2} = 12.0V ±10%
Am962059X - T_A = 0°C to +75°C V_{CC1} = 5.0V ±5%, V_{CC2} = 12.0V ±5%

DC Characteristics (Notes 1, 2)

Parameters	Part No.	Test Conditions	−55°C Min	−55°C Max	0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	+125°C Min	+125°C Max	Units
V_{OH} Output HIGH Voltage	Am962051X	V_{CC1} = 4.5 V, V_{DIFF} = −0.5 V, I_{OH} = −0.2 mA, V_{CC2} = 10.8 V	2.80				3.00	3.3				2.90		Volts
	Am962059X	V_{CC1} = 4.75 V, V_{DIFF} = −0.5 V, I_{OH} = −0.2 mA, V_{CC2} = −12.6 V			2.80		3.00	3.3		2.90				
V_{OL} Output LOW Voltage	Am962051X	V_{CC1} = 4.5 V, V_{DIFF} = +0.5 V, I_{OL} = 15.0 mA		0.40				0.25	0.40				0.45	Volts
	Am962059X	V_{CC1} = 4.75 V, I_{OL} = 15.0 mA				0.45		0.25	0.45		0.50			
I_{CEX} Output Leakage Current	Am962051X	V_{CC1} = 4.5 V, V_{DIFF} = −4.5 V, V_{CEX} = 12 V		50					100				200	μA
	Am962059X	V_{CC1} = 4.75 V, V_{CEX} = 5.25 V				50			100		200			
I_{SC} Output Short Circuit Current	Am962051X	V_{CC1} = 5.0 V, V_{SC} = 0 V					−1.4	−2.15	−3.1					mA
	Am962059X	V_{CC1} = 5.0 V, V_{SC} = 0 V					−1.4	−2.15	−3.1					
I_F Input Load Current	Am962051X	V_{CC1} = 5.0 V, V_{CC2} = 12 V		−3.1				−2.1	−3.0				−3.0	mA
	Am962059X	V_{CC1} = 5.0 V, V_{CC2} = 12 V				−3.1		−2.1	−3.0		−3.0			
V_{CM} Common Mode Voltage	Am962051X	V_{CC1} = 5.0 V, V_{DIFF} = 2.0 V, V_{CC2} = 12 V	−15	+15			−15	±17.5	+15			−15	+15	Volts
	Am962059X	V_{CC1} = 5.0 V, V_{DIFF} = 2.0 V, V_{CC2} = 12 V			−12	+12	−12	±17.5	+12	−12	+12			
V_{TH} Differential Input Threshold Voltage	Am962051X	V_{CC1} = 5.0 V, V_{CC2} = 12 V		500				120	500				500	mV
	Am962059X	V_{CC1} = 5.0 V, V_{CC2} = 12 V				500		120	500		500			mV
I_{CC1} Power Supply Current	Am962051X	V_{CC1} = 5.5 V, + Input = 5.5 V, V_{CC2} = 13.2 V, − Input = 0 V		13				8.2	13				13	mA
	Am962059X	V_{CC1} = 5.25 V, + Input = 5.25 V, V_{CC2} = 12.6 V, − Input = 0 V				13.5		8.2	13.5		13.5			
I_{CC2} Power Supply Current	Am962051X	V_{CC1} = 5.5 V, + Input = 5.5 V, V_{CC2} = 13.2 V, − Input = 0 V		8.0				5.6	8.0				8.0	mA
	Am962059X	V_{CC1} = 5.25 V, + Input = 5.25 V, V_{CC2} = −12.6 V, − Input = 0 V					8.5	5.6	8.5		8.5			

Switching Characteristics

Parameters			Am962051X +25°C Min	Typ	Max	Am962059X +25°C Min	Typ	Max	Units
t_{pd+}	Turn Off Delay R_L = 3.9 k	V_{CC} = 5.0 V, C_L = 30 pF Refer to figure 1		35	50		35	75	ns
t_{pd-}	Turn On Delay R_L = 390 Ω			20	50		20	75	

Note: 1. Pulse tested.
2. V_{DIFF} is the differential voltage referred from A+ to A− and from B+ to B−

SWITCHING TIME TEST CIRCUIT & WAVEFORMS

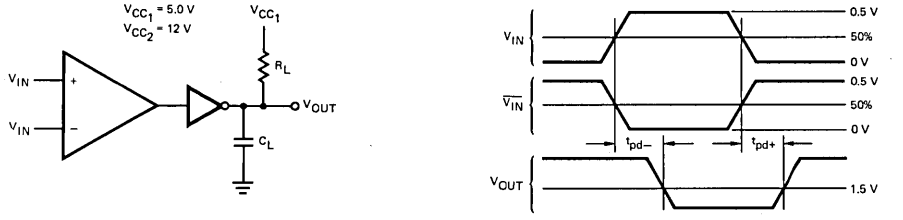
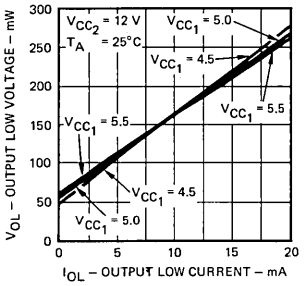


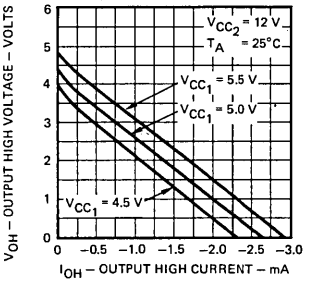
Figure 1.

TYPICAL ELECTRICAL CHARACTERISTICS

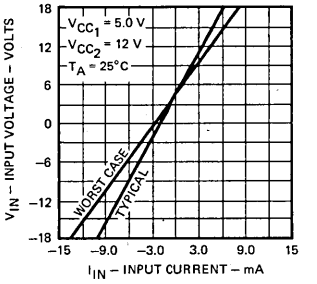
Output Low Voltage Versus Output Low Current



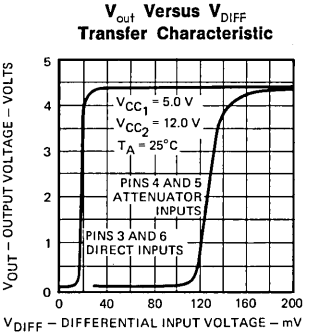
Output High Voltage Versus Output High Current



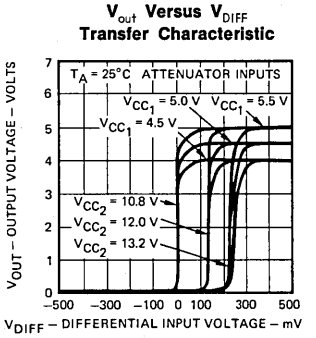
Input Voltage Versus Input Current



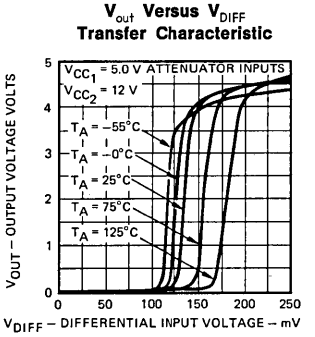
V_{out} Versus V_{DIFF} Transfer Characteristic



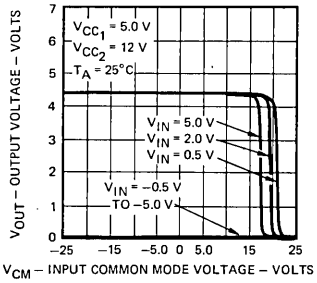
V_{out} Versus V_{DIFF} Transfer Characteristic



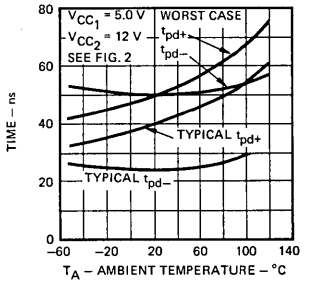
V_{out} Versus V_{DIFF} Transfer Characteristic



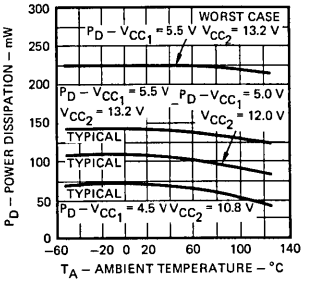
V_{out} Versus V_{CM} Characteristics



Switching Time Versus Ambient Temperature

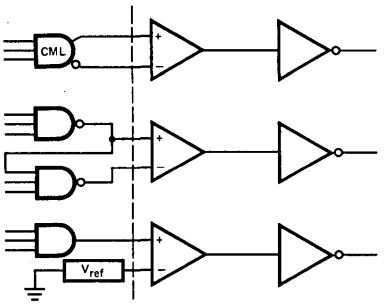


Power Dissipation Versus Ambient Temperature

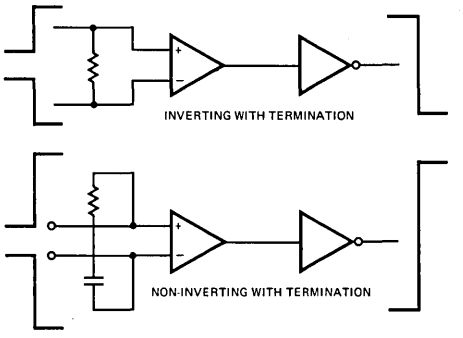


APPLICATIONS

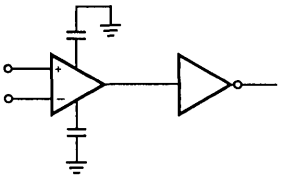
Interfacing Methods



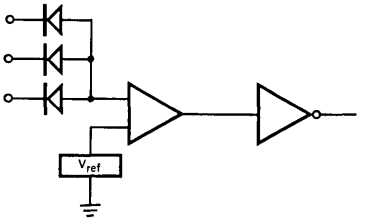
Digital Differential Amplifier (Line Receiver) Expanded Interface



Digital Differential Line Receiver With Inputs Rolled Off

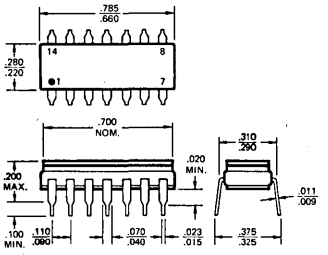


V_{ref} = Resistor, Diodes, or Supply

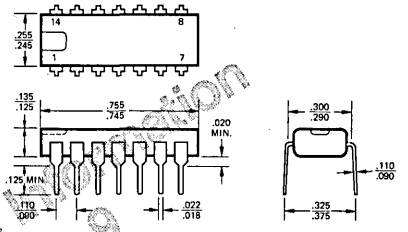


PHYSICAL DIMENSIONS
Dual-In-Line

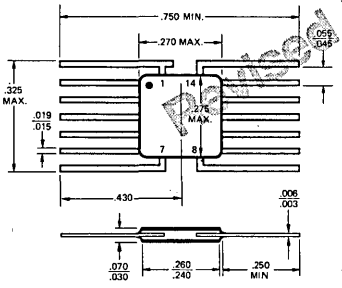
Hermetic



Molded

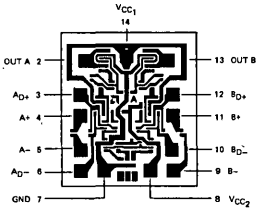


Flat Package



Metallization and Pad Layout

42 x 48 Mils



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TELEX: 34-6306

Am9621
Dual Line Driver

Distinctive Characteristics:

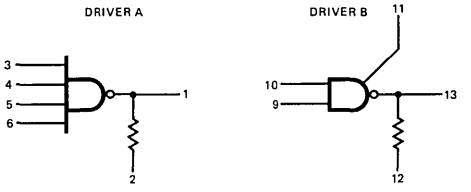
- Dual Differential Driver
- Transmission line back-matching.
- No supply current surges during power-on sequence.
- DTL, TTL compatible.
- Clamped outputs.
- 100% reliability assurance testing in compliance with MIL STD 883.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.
- Available in highly reliable molded epoxy, hermetic dual-in-line or hermetic flat package

FUNCTIONAL DESCRIPTION

The Am9621 is a dual line driver designed to drive transmission lines in either a differential or a single-ended mode. Output clamp diodes and back-matching resistors for 130Ω twisted pair lines are included. The device has the capability of driving high-capacitance loads being able to switch more than 200mA typically during transients.

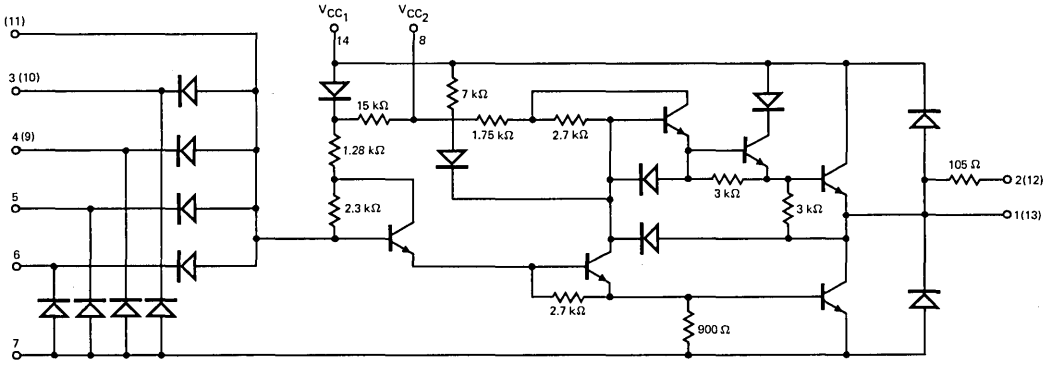
The Am9621 is designed so that power supplies can be switched on in any sequence without supply current surges.

LOGIC DIAGRAM



V_{CC1} = PIN 14
V_{CC2} = PIN 8
GND = PIN 7

CIRCUIT DIAGRAM

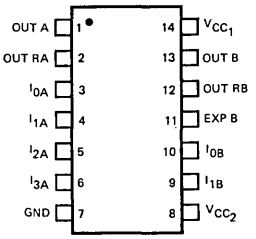


Am9621 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +75°C	U6E962159X
Hermetic DIP	0°C to +75°C	U6A962159X
Hermetic DIP	−55°C to +125°C	U6A962151X
Hermetic Flat Pak	−55°C to +125°C	U3I962151X
Dice	Note	UXX9621XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC1} Pin Potential to Ground Pin	+3.8 V to +8 V
DC Input Voltage	−0.5 V to +15 V
Voltage Applied to Outputs	−2.0 V to $+V_{CC1}$ +1.0 V
V_{CC2} Pin Potential to Ground Pin	V_{CC1} to +15 V

ELECTRICAL CHARACTERISTICS

Am962151X - T_A = −55°C to +125°C V_{CC1} = 5.0 V ±10%, V_{CC2} = 12.0 V ±10%
Am962159X - T_A = 0°C to +75°C V_{CC1} = 5.0 V ±5%, V_{CC2} = 12.0 V ±5%

DC Characteristics (Note 2)

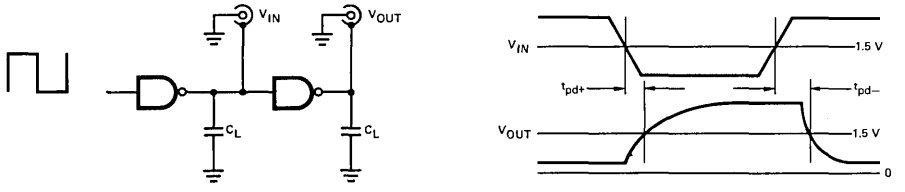
Parameters	Part No.	Test Conditions	LIMITS −55°C Min	−55°C Max	0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	+125°C Min	+125°C Max	Units
V_{OH} Output HIGH Voltage	Am962151X	V_{CC1} = 4.5 V, I_{OH} = −20 mA	4.00				4.00	4.3				4.00		Volts
	Am962159X	V_{CC1} = 4.75 V, I_{OH} = −20 mA			4.20		4.20	4.4		4.20				
V_{OL} Output LOW Voltage	Am962151X	V_{CC1} = 4.5 V, I_{OL} = 20 mA		0.35				0.2	0.35				0.40	Volts
	Am962159X	V_{CC1} = 4.75 V, I_{OL} = 20 mA				0.40		0.2	0.40		0.45			
V_{OLR} (Note 2) Resistive Output LOW Voltage	Am962151X	V_{CC1} = 5.0 V, V_{CC2} = 12 V, I_{OL} = 2.8 mA						380	500					mV
	Am962159X	V_{CC1} = 5.0 V, V_{CC2} = 12 V, I_{OL} = 2.8 mA						380	500					
V_{OHR} (Note 2) Resistive Output HIGH Voltage	Am962151X	V_{CC1} = 5.0 V, V_{CC2} = 12 V, I_{OH} = −2.3 mA					4.00	4.2						Volts
	Am962159X	V_{CC1} = 5.0 V, V_{CC2} = 12 V, I_{OH} = −2.3 mA					4.00	4.2						
I_{OL} (Note 1) Output LOW Current	Am962151X	V_{CC1} = 4.5 V, V_{CC2} = 10.8 V, V_O = 5.0 V					150	200						mA
	Am962159X	V_{CC1} = 4.75 V, V_{CC2} = 11.4 V, V_O = 5.0 V					75	200						
V_{IH} Input HIGH Voltage	Am962151X	V_{CC1} = 4.5 V, V_{CC2} = 13.2 V	2.20				2.00	1.7				1.80		Volts
	Am962159X	V_{CC1} = 4.75 V, V_{CC2} = 11.4 V			2.20		2.00	1.7		1.80				
V_{IL} Input LOW Voltage	Am962151X	V_{CC1} = 5.5 V, V_{CC2} = 10.8 V		1.30				1.5	1.00				0.70	Volts
	Am962159X	V_{CC1} = 5.25 V, V_{CC2} = 12.6 V				1.30		1.5	1.00		0.70			
I_F Input Load Current	Am962151X	V_{CC1} = 5.5 V, V_F = 0 V, V_{CC2} = 13.2 V		1.8				1.15	1.8				1.8	mA
	Am962159X	V_{CC1} = 5.25 V, V_F = 0 V, V_{CC2} = 12.6 V				1.8		1.15			1.8			
I_R Reverse Input Current	Am962151X	V_{CC1} = 5.5 V, V_R = 5.5 V, V_{CC2} = 13.2 V		2.0				<1.0	2.0				5.0	μA
	Am962159X	V_{CC1} = 5.25 V, V_R = 5.25 V, V_{CC2} = 12.6 V				5.0		<1.0	5.0		10.0			
I_{SC} (Note 1) Short Circuit Current	Am962151X	V_{CC1} = 4.5 V, V_{CC2} = 10.8 V, V_O = 0 V					−180	−300						mA
	Am962159X	V_{CC1} = 4.75 V, V_{CC2} = 11.4 V, V_O = 0 V					−100	−300						
I_{CC1} Power Supply Current	Am962151X	V_{CC1} = 5.5 V, V_{CC2} = 13.2 V, Inputs Open		7.0				4.7	7.0				7.3	mA
	Am962159X	V_{CC1} = 5.25 V, V_{CC2} = 12.6 V, Inputs Open				7.0		4.7	7.0		7.3			
I_{CC2} Power Supply Current	Am962151X	V_{CC1} = 5.5 V, V_{CC2} = 13.2 V, Inputs Open		9.8				6.5	9.8				9.8	
	Am962159X	V_{CC1} = 5.25 V, V_{CC2} = 12.6 V, Inputs Open				9.8		6.5	9.8		9.8			
V_{OLC} (Note 3) Output LOW Clamp Voltage	Am962151X	V_{CC1} = 5.0 V, V_{CC2} = 12 V, I_{OLC} = −20 mA						−1.0	−2.0					Volts
	Am962159X	V_{CC1} = 5.0 V, V_{CC2} = 12 V, I_{OLC} = −20 mA												
V_{OHC} (Note 3) Output HIGH Clamp Voltage	Am962151X	V_{CC1} = 5.0 V, V_{CC2} = 12 V, I_{OHC} = 20 mA						6.0	7.0					Volts
	Am962159X	V_{CC1} = 5.0 V, V_{CC2} = 12 V, I_{OHC} = 20 mA						6.0	7.0					

Note 1. Pulse tests to insure transient current handling (test time = 3 seconds maximum — one side only).
2. Test output resistance including 105Ω output resistor.
3. Tests output clamp diodes.
4. For Am962151X with both sides loaded at T_A = +125°C, maximum frequency = 500 kHz for dual-in-line package (θ_{JA} = 95°C/W) or 300 kHz for ceramic flat pak (θ_{JA} = 165°C/W).
5. For Am962159X with both sides loaded at T_A = +75°C, maximum frequency = 500 kHz for both dual-in-line package and ceramic flat pak.

Switching Characteristics

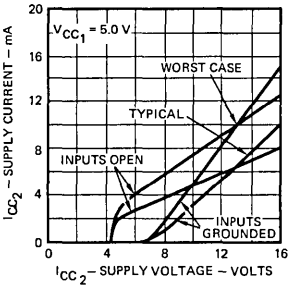
Parameters		Test Conditions	Am962151X +25°C Min	Typ	Max	Am962159X +25°C Min	Typ	Max	Units
t_{pd+}	Turn Off Delay	$V_{CC1} = 5.0$ V, $C_L = 30$ pF		13	25		13	40	ns
t_{pd-}	Turn On Delay	$V_{CC2} = 12$ V		9	25		9	40	ns
t_{pd+}	Turn Off Delay	$V_{CC1} = 5.0$ V, $C_L = 5000$ pF	(Note 4)	30	150	(Note 5)	30	200	ns
t_{pd-}	Turn On Delay	$V_{CC2} = 12$ V	(Note 4)	80	150	(Note 5)	80	200	ns

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

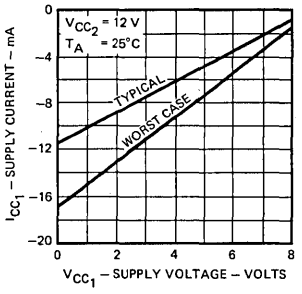


TYPICAL ELECTRICAL CHARACTERISTICS

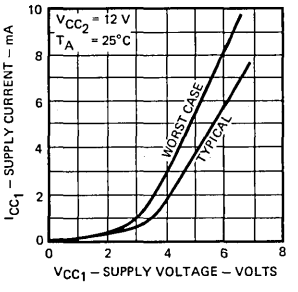
Supply Current Versus Supply Voltage



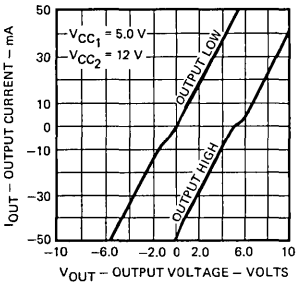
Supply Current Versus Supply Voltage Inputs Grounded



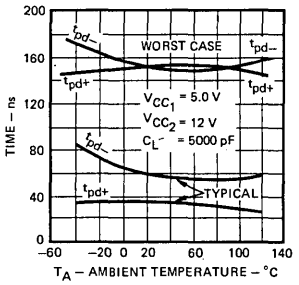
Supply Current Versus Supply Voltage Inputs Open



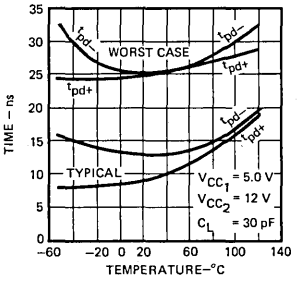
Typical Output Impedance With Back Matching Resistors



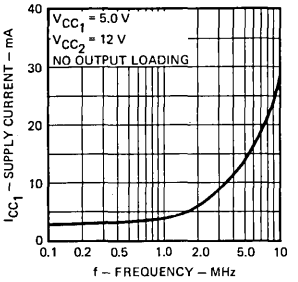
Switching Time Versus Temperature



Switching Time Versus Temperature

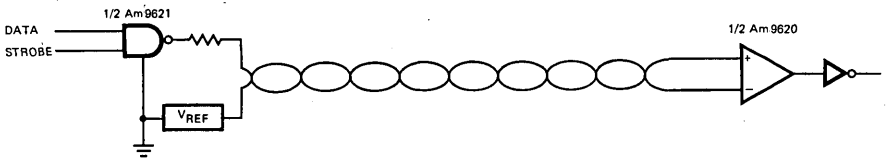


Typical Supply Current Versus Frequency

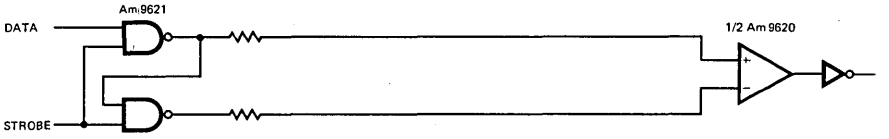


APPLICATIONS

SINGLE-ENDED DRIVING



DIFFERENTIAL DRIVING



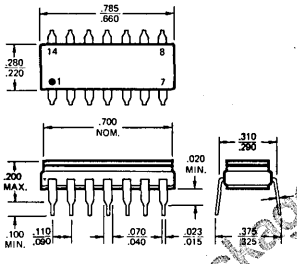
BACK-MATCHING TABLE

Z_O	R_M when used single ended	R_M when used differentially
50 Ω	32 Ω	16 Ω
75 Ω	62 Ω	30 Ω
92 Ω	82 Ω	41 Ω
100 Ω	90 Ω	45 Ω
130 Ω	120 Ω	60 Ω
300 Ω	290 Ω	145 Ω
600 Ω	590 Ω	295 Ω

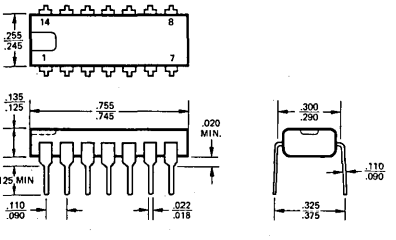
PHYSICAL DIMENSIONS

Dual-In-Line

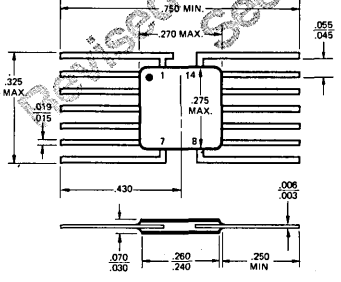
Hermetic



Molded

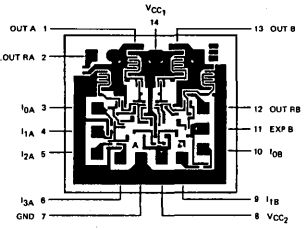


Flat Package



Metallization and Pad Layout

54 x 52 Mils



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Am26123•Am54/74123

Dual Retriggerable Resettable Monostable Multivibrator

Distinctive Characteristics

- Retriggerable 0 to 100% duty cycle.
- 50ns to ∞ output pulse width range.
- Am26123 guaranteed pulse width change of less than 1% over 0°C to +70°C temperature range.
- Am26123 outputs immune to noise triggering the monostable at the RC timing nodes.
- 100% reliability assurance testing in compliance with MIL-STD-883.

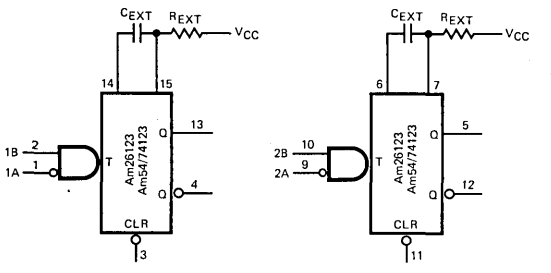
FUNCTIONAL DESCRIPTION

The Am26123 and the Am54/74123 are dual retriggerable resettable monostable multivibrators. The output pulse-width duration and accuracy are determined by external timing components. The Am26123 is pin compatible with the Am54/74123 but features two major improvements:

1. Pulse width stability of ±1% or better is guaranteed over 0°C to +70°C for the Am26123.
2. The Am26123 incorporates an output latch which offers immunity to spurious output changes in the quiescent state due to coupling of external noise at the timing capacitor nodes.

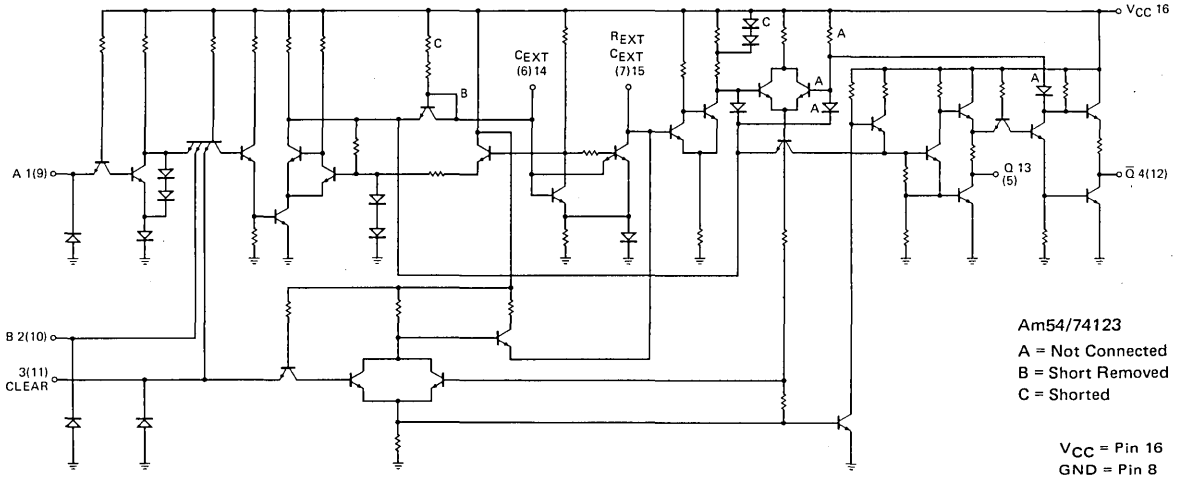
An active-LOW A input and an active-HIGH B input are logically coupled in an AND gate on the trigger input of each device. A LOW on the clear input resets the monostable to the normal Q LOW quiescent state regardless of the A and B inputs.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

Am26123 SCHEMATIC DIAGRAM



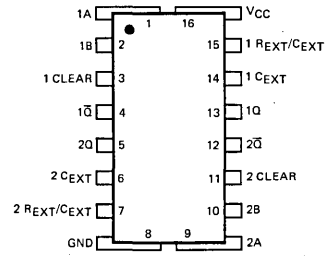
Am54/74123
A = Not Connected
B = Short Removed
C = Shorted

V_{CC} = Pin 16
GND = Pin 8

ORDERING INFORMATION

Package Type	Temperature Range	Am26123 Order Number	Am54/74123 Order Number
Molded DIP	0°C to +70°C	AM26123PC	SN74123N
Hermetic DIP	0°C to +70°C	AM26123DC	SN74123J
Dice	0°C to +70°C	AM26123XC	SN74123X
Hermetic DIP	−55°C to +125°C	AM26123DM	SN54123J
Hermetic Flat Pak	−55°C to +125°C	AM26123FM	SN54123W
Dice	−55°C to +125°C	AM26123XM	SN54123X

CONNECTION DIAGRAM Top View



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	–0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	–0.5 V to +V_{CC} max.
DC Input Voltage	–0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	–30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am26123XC, Am74123 T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am26123XM, Am54123 T_A = –55°C to +125°C V_{CC} = 5.0V ±10% (MIL) MIN. = 4.5V MAX. = 5.5V

Parameters	Description		Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{IH}	Input HIGH Voltage				2.0			V
V_{IL}	Input LOW Voltage						0.8	V
V_I	Input Clamp Voltage		V_{CC} = MIN., I_I = –12mA				–1.5	V
V_{OH}	Output HIGH Voltage		V_{CC} = MIN., I_{OH} = –800μA (Note 5)		2.4	4.0		V
V_{OL}	Output LOW Voltage		V_{CC} = MIN., I_{OL} = 16mA (Note 5)			0.22	0.4	V
I_I	Input Current at Maximum Input Voltage		V_{CC} = MAX., V_I = 5.5V				1.0	mA
I_{IH} (Note 3)	Input HIGH Current	A or B	V_{CC} = MAX., V_I = 2.4V			5	40	μA
		Clear				10	80	
I_{IL} (Note 3)	Input LOW Current	A or B	V_{CC} = MAX., V_I = 0.4V			–1.0	–1.6	mA
		Clear				–2.0	–3.2	
I_{OS}	Output Short Circuit Current (Note 4)		V_{CC} = MAX. (Note 5)	Am54/74123 V_{OUT} = 0.0V	–10		–40	mA
				Am26123 V_{OUT} = 1.0V, T_A = 25°C				
I_{CC}	Power Supply Current		V_{CC} = MAX. (Notes 6 & 7)			46	66	mA

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input load factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. Ground C_{ext} to measure V_{OH} at Q, V_{OL} at $\overline{Q}$, 0V I_{OS} at Q. C_{ext} is open to measure V_{OH} at $\overline{Q}$. V_{OL} at Q, 0V I_{OS} at $\overline{Q}$. (On the Am26123, the input must be triggered also.)
6. I_{CC} is measured in the triggered state with 2.4V applied to all clear and B inputs, A inputs grounded, all outputs open, C_{ext} = 0.02μF and R_{ext} = 25kΩ.
7. Quiescent I_{CC} is measured (after clearing) with 2.4V applied to all clear and A inputs, B inputs grounded, all outputs open, C_{ext} = 0.02μF, and R_{ext} = 25kΩ.

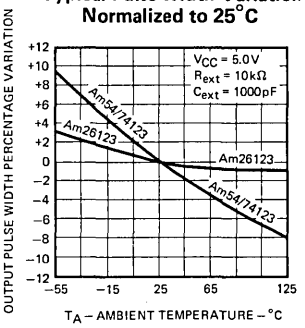
Switching Characteristics (T_A = 25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	A to Q	C_{ext} = 0, R_{ext} = 5kΩ C_L = 15pF, R_L = 400Ω		22	33	ns
t_{PHL}	A to $\overline{Q}$			30	40	ns
t_{PLH}	B to Q			19	28	ns
t_{PHL}	B to $\overline{Q}$			27	36	ns
t_{PLH}	Clear to $\overline{Q}$			30	40	ns
t_{PHL}	Clear to Q			18	27	ns
$t_{pw}Q$ (MIN.)	Minimum Pulse Width Q Output			45	65	ns
t_{pw}	A or B inputs HIGH		40			ns
t_{pw}	A or B inputs LOW		40			ns
t_{pw}	Clear LOW		40			ns
$t_{pw}Q$	Pulse Width Q Output	C_{ext} = 1000pF, R_{ext} = 10kΩ C_L = 15pF, R_L = 400Ω	3.08	3.42	3.76	μs

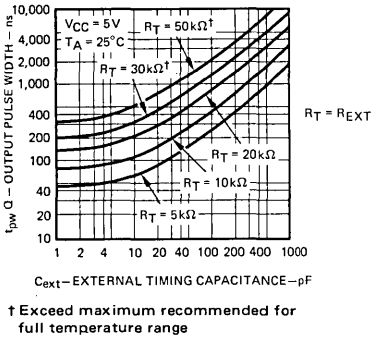
Am26123 Only

$\Delta t_{pw}(T)$	Maximum Change of t_{pw} Q Over Temperature Range 0°C to +70°C	C_{ext} = 1000pF, R_{ext} = 10kΩ C_L = 15pF, R_L = 400Ω		±0.5	±1.0	%

Typical Pulse-Width Variation Normalized to 25°C

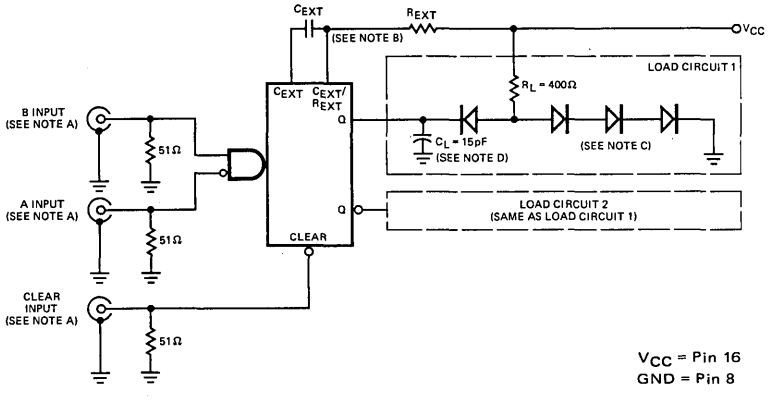


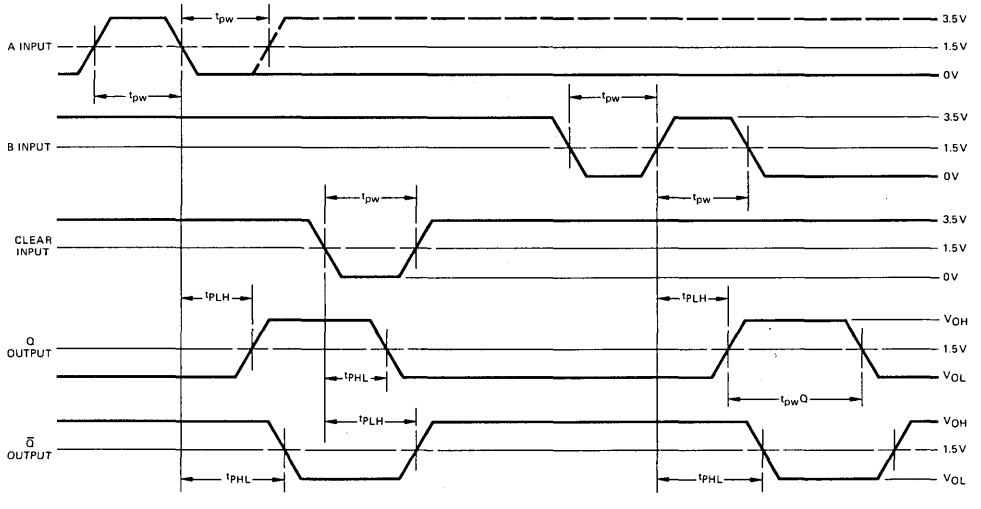
Output Pulse Width Versus External Timing Capacitance



† Exceed maximum recommended for full temperature range

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





Notes:
A. The pulse generators have the following characteristics: $t_r \leq 10$ns (10% to 90% level), $t_f \leq 10$ns, PRR $\leq$ 1MHz, duty cycle $\leq$ 50%, $Z_{out} \approx 50\Omega$.
B. See Test Conditions, switching characteristics table, for values of R_{ext} and C_{ext}.
C. All diodes are 1N3064
D. C_L includes probe and jig capacitance.

OPERATION RULES

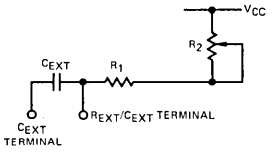
TIMING

1. Timing components C_{ext} and R_{ext} values.

Operating Temperature Range

	0°C to 70°C	-55°C to +125°C
R_{ext} MIN.	5kΩ	5kΩ
R_{ext} MAX.	50kΩ	25kΩ
C_{ext}	any value	any value

2. Remote adjustment of timing.



$R_1 + R_2 = R_{ext}$

$R_1 \geq R_{ext}$ MIN.

$R_2 < R_{ext}$ MAX. $- R_1$

In the above arrangement, R_1 and C_{ext} should be as close as possible to the device pins to minimize stray capacitance and external noise pickup. The variable resistor R_2 can be located remotely from the device if reasonable care is used.

3. Pulse width change measurements.

The pulse width $t_{pw}Q$ is specified and measured with components of better than 0.1% accuracy. If measurements are made with reduced component tolerances, the expected accuracy should be adjusted accordingly.

4. Timing for $C_{ext} \leq 1000pF$.

When using capacitor of less than or equal to 1000pF in value, the output pulse width should be determined from the output pulse width versus external timing capacitance graph.

5. Timing for $C_{ext} > 1000pF$.

For capacitors of greater than 1000pF in value, the output pulse width, $t_{pw}Q$, is determined by

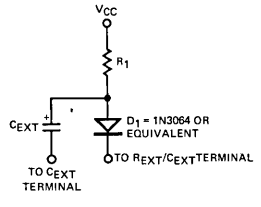
$$t_{pw}Q = 0.32\ R_{ext}\ C_{ext}\ (1 + \frac{0.7}{R_{ext}})$$

where

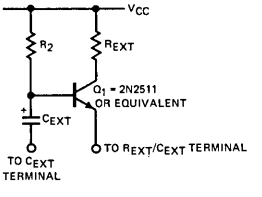
R_{ext} is in kilohms
C_{ext} is in picofarads
$t_{pw}Q$ is in nanoseconds

6. Protection of electrolytic timing capacitors.

If the electrolytic capacitor to be used as C_{ext} cannot withstand 1.0 volt reverse bias, one of the following two circuit techniques should be used to protect the electrolytic capacitor from the reverse voltage.



$R_1 \leq 0.6 \times R_{ext}$ MAX.



$R_2 < 0.7 \times h_{FEQ1} \times R_{ext}$

The output pulse width, $t_{pw}Q$, for the diode circuit modifies the previous timing equation as follows:

$$t_{pw}Q = 0.28\ R_1\ C_{ext}\ (1 + \frac{0.7}{R_1})$$

The output pulse width for the transistor circuit is

$$t_{pw}Q = 0.30 \times R_2 \times C_{ext}\ (1 + \frac{0.7}{R_2})$$

Notice that the transistor circuit allows values of timing resistor R_2 larger than the R_{ext} MIN $< R_{ext} <$ R_{ext} MAX. to obtain longer output pulse widths for a given C_{ext}.

TRIGGER AND RETRIGGER

1. Triggering.

The minimum pulse width signal into input A or input B to cause the device to trigger is 40ns. Refer to the truth table for the appropriate input conditions.

2. Retriggering.

The retriggered pulse width, $t_{pwr}Q$, is the time during which the output is active after the device is retriggered during a timing cycle. It differs from the initial pulse width $t_{pw}Q$ timing equation as follows.

$$t_{pwr}Q = t_{pw}Q + t_{PLH}$$

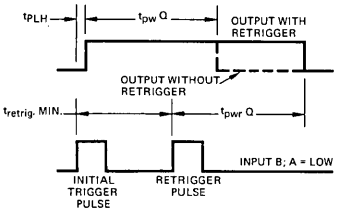
where t_{PLH} is the propagation delay time from the A or B input to the output.

For values of $t_{pw}Q$ greater than about 500ns, t_{PLH} can be ignored.

3. Rapid retriggering.

A minimum retriggering time does exist. That is, the device cannot be retriggered until a minimum recovery time has elapsed. The minimum retrigger time is defined by

t_{retrig} MIN. = 0.224 C_{ext}
C is in picofarads
t is in nanoseconds



4. Output Latch.

The Am26123 incorporates an output latch that can be triggered only by the input trigger gate via the A or B inputs. Thus, spurious output pulses caused by external noise on the C_{ext} nodes are eliminated during the quiescent state. This feature is extremely valuable in many high noise environment systems.

CLEAR

A LOW on the clear inputs terminates the timing cycle. It also resets the output latch on the Am26123. A new trigger cycle cannot be initiated while the clear is LOW. With the clear HIGH, the device is under the command of the A and B inputs.

TRUTH TABLE

Am26123 • Am54/74123
For Each Monostable

Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
H	H	X	L	H
H	L	↑	⎍	⎎
H	X	L	L	H
H	↓	H	⎍	⎎

H = HIGH X = Don't Care
L = LOW
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition
⎍ = LOW-HIGH-LOW pulse
⎎ = HIGH-LOW-HIGH pulse

MSI INTERFACING RULES

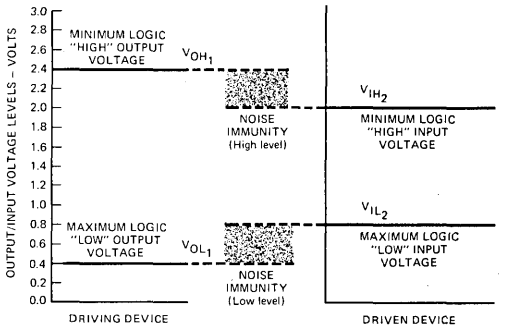
Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

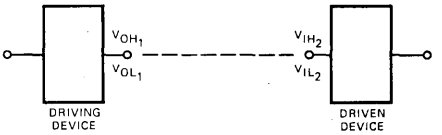
Am26123 • Am54/74123 LOADING RULES

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
1A	1	1	–	–
1B	2	1	–	–
1 CLEAR	3	2	–	–
$1\overline{Q}$	4	–	20	10
2Q	5	–	20	10
2 C_{ext}	6	–	–	–
2 R_{ext}/C_{ext}	7	–	–	–
GND	8	–	–	–
2A	9	1	–	–
2B	10	1	–	–
2 CLEAR	11	2	–	–
$2\overline{Q}$	12	–	20	10
1Q	13	–	20	10
1 C_{ext}	14	–	–	–
1 R_{ext}/C_{ext}	15	–	–	–
V_{CC}	16	–	–	–

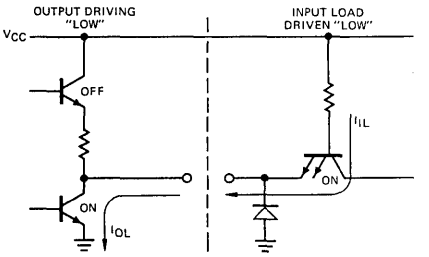
INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions – LOW & HIGH

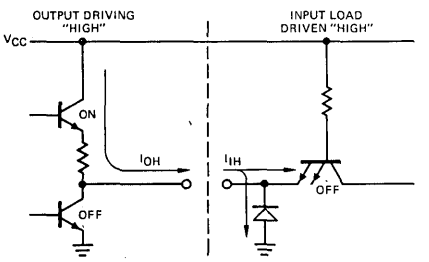




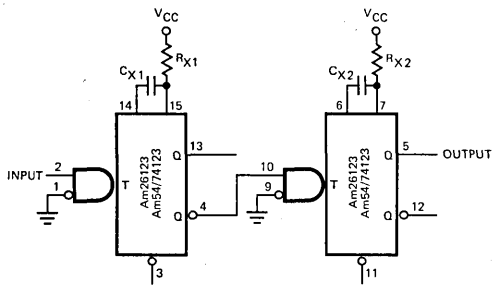
Current Interface Conditions – LOW

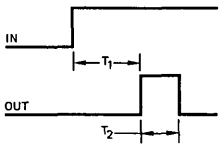


Current Interface Conditions – HIGH



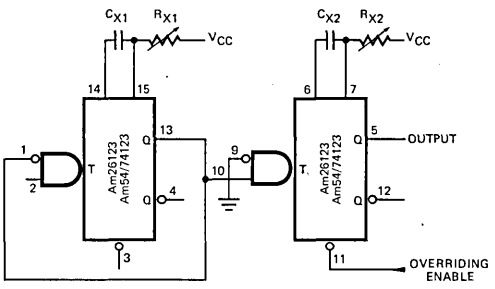
APPLICATIONS





Delayed Pulse Generation

The first monostable determines the time T_1 before the initiation of the output pulse. The second monostable determines T_2, the output pulse width.

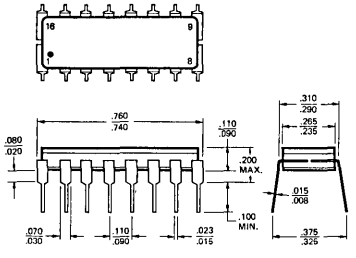


Pulse Generator

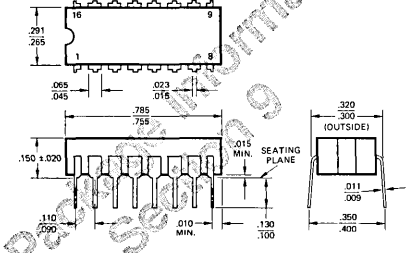
The output frequency produced with the above configuration is determined by C_{X1} and R_{X1}, while the pulse width is determined by C_{X2} and R_{X2}. Monostable 1 forms an astable multivibrator with an output pulse width of approximately 25 ns, while monostable 2 extends the pulse width to the required value.

PHYSICAL DIMENSIONS
Dual-In-Line

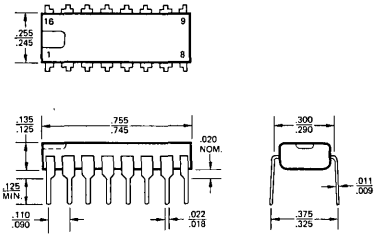
Hermetic



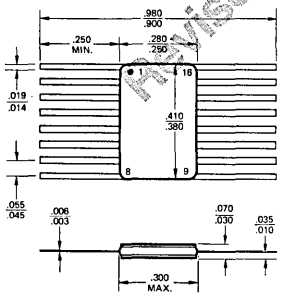
Ceramic DIP



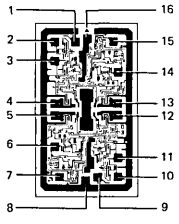
Molded



Flat Package



Metallization and Pad Layout



DIE SIZE 0.050" X 0.088"

ADVANCED
MICRO
DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am55/75107B • Am55/75108B
Am75207 • Am75208
Dual Line Receivers

Distinctive Characteristics

- Input sensitivity 3mV typical
- Common mode range of ±3V
- Common mode range of more than ±15V using external attenuator
- TTL compatible output
- High common mode rejection ratio
- Blocking diodes provide high input impedance
- Strobe and gate inputs for flexibility
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am55/75107B, Am55/75108B, Am75207, and Am75208 are high speed dual line receivers designed for use as data receivers in balanced, unbalanced or party-line transmission systems. The two line receivers in each package share the common voltage and ground busses. The Am55/75107B and Am75207 have a standard active pull-up totem-pole output while the Am55/75108B and Am75208 have an open collector output for bus organized systems.

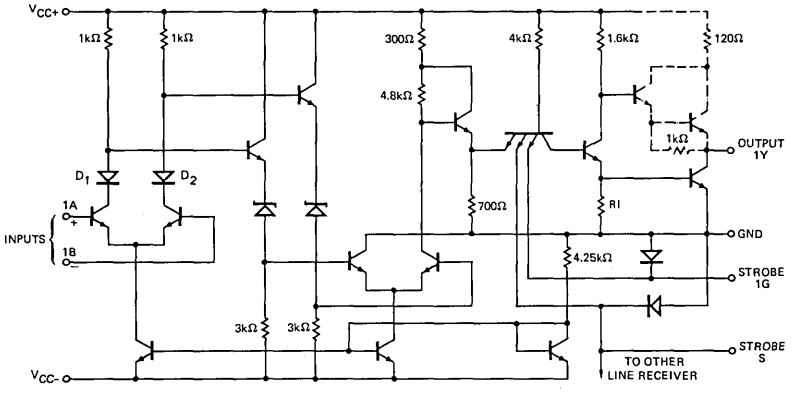
Each receiver has a high impedance differential input for minimum transmission line loading. The differential inputs of the Am55/75107B and Am55/75108B are designed to detect input signals of 25mV or greater and provide TTL compatible outputs. The differential inputs of the Am75207 and Am75208 are designed to detect input signals of 10mV or greater.

All devices contain blocking diodes in the input differential transistor pair collectors to provide high input impedance in the power-off condition. The SN55/75107A and SN55/75108A are identical devices except for these input protection diodes.

Each receiver has a separate gate input, G. When the gate is LOW, the output is HIGH regardless of the other inputs. The device also has a common strobe, S, which can be used to gate both receivers simultaneously. When the strobe is LOW, the output is HIGH regardless of the other inputs.

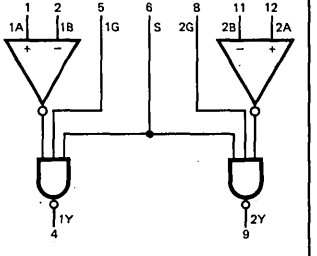
Note: Output HIGH on the Am55/75108B and Am75208 are high impedance conditions.

SCHEMATIC DIAGRAM
(One Receiver Shown)



Notes: 1. Components shown with dashed lines are applicable to the Am55/75107B and Am75207 only.
2. RI = 1kΩ for Am55/75107B and Am75207, 750Ω for Am55/75108B and Am75208.
3. D1 and D2 are the input protection diodes.

LOGIC SYMBOL

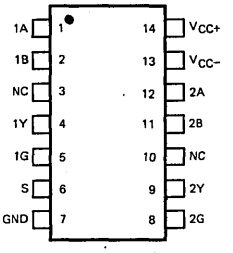


VCC− = Pin 13
VCC+ = Pin 14
GND = Pin 7

ORDERING INFORMATION

Package Type	Temperature Range	Am55/ 75107B Order Number	Am55/ 75108B Order Number	Am75207 Order Number	Am75208 Order Number
Molded DIP	0°C to +70°C	SN75107BN	SN75108BN	SN75207N	SN75208N
Hermetic DIP	0°C to +70°C	SN75107BJ	SN75108BJ	SN75207J	SN75208J
Dice	0°C to +70°C	SN75107BX	SN75108BX	SN75207X	SN75208X
Hermetic DIP	-55°C to +125°C	SN55107BJ	SN55108BJ		
Dice	-55°C to +125°C	SN55107BX	SN55108BX		

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.
NC = No connection.

MAXIMUM RATINGS (Above which the useful life may be impaired).

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Positive Supply Voltage V_{CC+} to Ground Potential Continuous	+7V
Negative Supply Voltage V_{CC-} to Ground Potential Continuous	−7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC+} max.
DC Input Voltage — Strobe	−0.5V to +5.5V
Differential Input Voltage	±6V
Common Mode Input Voltage (with Respect to GND Terminal)	±5V
Any Differential Input to Ground	−5V to +3V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Specified)

Am75107B, Am75108B, Am75207, Am75208 — T_A = 0°C to 70°C — V_{CC+} = 5.0V ±5% — V_{CC-} = −5.0V ±5% (COM L)

Am55107B, Am55108B — T_A = −55°C to +125°C — V_{CC+} = 5.0V ±10% — V_{CC-} = −5.0V ±5% (MIL)

Commercial	V_{CC+} MIN. = 4.75V	V_{CC+} MAX. = 5.25V	V_{CC-} MIN. = −4.75V	V_{CC-} MAX. = −5.25V
Military	V_{CC+} MIN. = 4.5V	V_{CC+} MAX. = 5.5V	V_{CC-} MIN. = −4.5V	V_{CC-} MAX. = −5.5V

Parameters	Description	Test Conditions (Notes 1, 4, & 5)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage Am55/75107B Only	V_{CC+} = MIN., V_{CC-} = MIN. I_{OH} = −400µA, V_{IC} = −3V to 3V		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC+} = MIN., V_{CC-} = MIN. I_{OL} = 16mA, V_{IC} = −3V to 3V				0.4	Volts
V_{IH}	Strobe or gate input HIGH Voltage	See Test Table		2			Volts
V_{IL}	Strobe or Gate Input LOW Voltage	See Test Table				0.8	Volts
V_{IDH}	Differential Input Voltage for Output HIGH	See Test Table	107B, 108B	0.025		5	Volts
			207, 208	0.010		5	
V_{IDL}	Differential Input Voltage for Output LOW	See Test Table	107B, 108B	−5		−0.025	Volts
			207, 208	−5		−0.010	
I_{IH}	Input HIGH Current into 1A or 2A	V_{CC+} = MAX., V_{CC-} = MAX. V_{ID} = 0.5V, V_{IC} = −3V to 3V			30	75	µA
I_{IL}	Input LOW Current into 1A or 2A	V_{CC+} = MAX., V_{CC-} = MAX. V_{ID} = −2V, V_{IC} = −3V to 3V				−10	µA
I_{IH}	Input HIGH Current	V_{CC+} = MAX., V_{CC-} = MAX. V_{IH} = 2.4V	S			80	µA
			G			40	
I_I	Input HIGH Current	V_{CC+} = MAX., V_{CC-} = MAX. V_{IH} = V_{CC+} MAX.	S			2	mA
			G			1	
I_{IL}	Input LOW Current	V_{CC+} = MAX., V_{CC-} = MAX. V_{IL} = 0.4V	S			−3.2	mA
			G			−1.6	
I_{OH}	HIGH Level Output Leakage Am55/75108B & Am75208 Only	V_{CC+} = MIN., V_{CC-} = MIN. V_{OH} = V_{CC+} MAX.				250	µA
I_{SC}	Output Short Circuit Current (Note 3) Am55/75107B and Am75207 Only	V_{CC+} = MAX., V_{CC-} = MAX.		−18		−70	mA
I_{CCH+}	Positive Power Supply Current	V_{CC+} = MAX., V_{CC-} = MAX. V_{ID} = 25mV, T_A = 25°C			18	30	mA
I_{CCH-}	Negative Power Supply Current	V_{CC+} = MAX., V_{CC-} = MAX. V_{ID} = 25mV, T_A = 25°C			−8.4	−15	mA
V_I	Input Clamp Voltage, S or G	V_{CC+} = MIN., V_{CC-} = MIN. I_{IN} = −12mA, T_A = 25°C			−1	−1.5	Volts

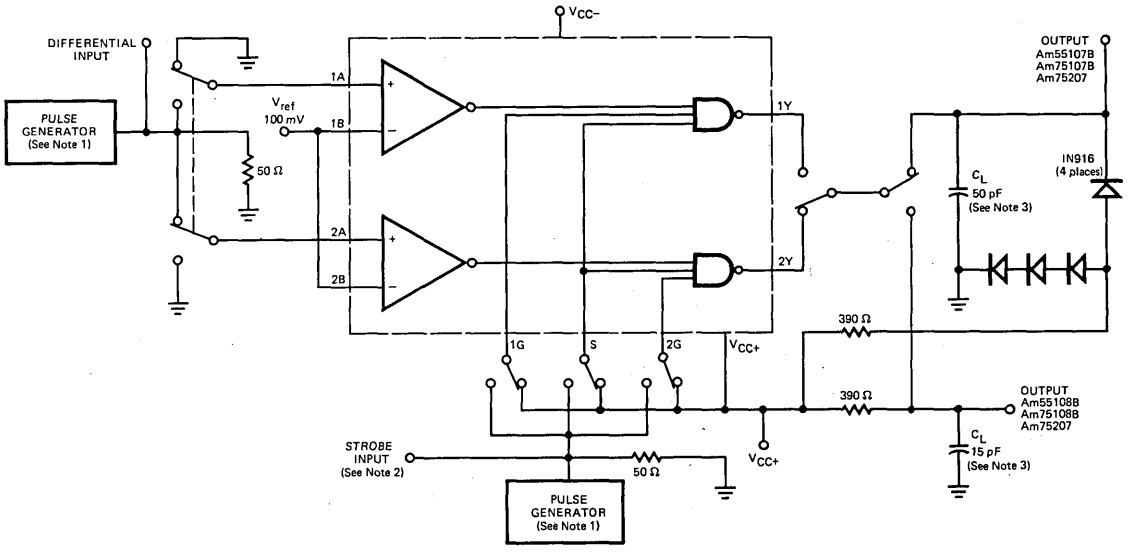
Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC+} = 5.0V, V_{CC-} = −5.0V, T_A = 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. For Am75207 and Am75208 replace 25mV with 10mV where specified.
5. V_{IC} = common mode voltage with respect to GND terminal.
   V_{ID} = differential voltage (V_A − V_B).

SWITCHING CHARACTERISTICS (T_A = +25°C)

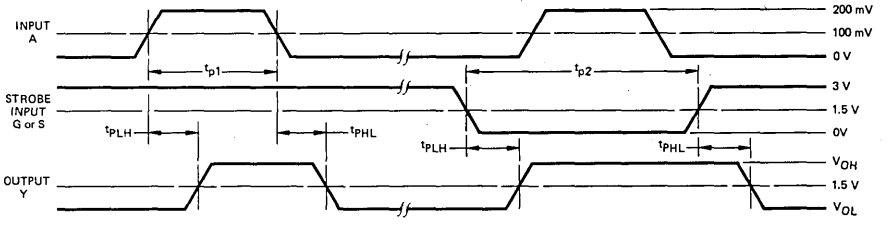
Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
Am55/75107B Only						
t_{PLH}	A and B to Output	V_{CC+} = 5V		17	25	ns
t_{PHL}	A and B to Output	V_{CC-} = −5V		17	25	ns
t_{PLH}	G or S to Output	R_L = 390Ω		10	15	ns
t_{PHL}	G or S to Output	C_L = 50 pF		8	15	ns
Am55/75108B Only						
t_{PLH}	A and B to Output	V_{CC+} = 5V		19	25	ns
t_{PHL}	A and B to Output	V_{CC-} = − 5V		19	25	ns
t_{PLH}	G or S to Output	R_L = 390Ω		13	20	ns
t_{PHL}	G or S to Output	C_L = 15 pF		13	20	ns
Am75207, Am75208 Only						
t_{PLH}	A and B to Output	V_{CC+} = 5V			35	ns
t_{PHL}	A and B to Output	V_{CC-} = -5V			20	ns
t_{PLH}	G or S to Output	R_L = 470Ω			17	ns
t_{PHL}	G or S to Output	C_L = 15 pF			17	ns

AC PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT



VOLTAGE WAVEFORMS



Notes: 1. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 10 ± 5 ns, t_{p1} = 500 ns, PRR = 1 MHz, t_{p2} = 1 ms, PRR = 500 kHz.

2. Strobe input pulse is applied to Strobe 1G when inputs 1A – 1B are being tested, to Strobe S when inputs 1A – 1B or 2A – 2B are being tested, and to Strobe 2G when inputs 2A – 2B are being tested.

3. C_L includes probe and jig capacitance.

FUNCTION TABLE

Differential Input Voltage $V_{ID} = V_A - V_B$	Inputs		Output
	Gate	Strobe	
	G	S	Y
$V_{ID} \geq +25mV$	X	X	H
$-25mV < V_{ID} < +25mV$	H	H	?
$V_{ID} \leq -25mV$	H	H	L
X	L	X	H
X	X	L	H

H = HIGH
L = LOW
X = Don't Care
? = Don't Know

Note: For Am75207 and Am75208 substitute 10mV for 25mV.

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

DEFINITION OF FUNCTIONAL TERMS

1A, 2A The non-inverting input of the line receivers.

1B, 2B The inverting input of the line receivers.

1Y, 2Y The output of each line receiver.

1G, 2G The gate input of each line receiver. A LOW on the gate input forces the output HIGH.

S The strobe input that is common to both line receivers. A LOW on the strobe forces both (1Y and 2Y) outputs HIGH.

V_{IC} Input Common Mode voltage with respect to ground terminal.

V_{ID} Differential Input voltage ($V_A - V_B$).

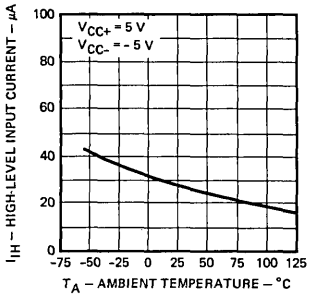
DC TEST TABLE (See Note 4)

Parameter	1A	2A	1B 2B	V_{IC} (Common Mode)	V_{ID} (Differential)	1Y 2Y	1G	2G	S	Note
V_{IDH}	–		–	–3V to 3V	Test	–400μA (Note 2)	+5V		+5V	1
V_{IDL}	–		–	–3V to 3V	Test	16mA	+5V		+5V	1
I_{IH} @ A	–		–	–3V to 3V	+0.5V	Open	Open		Open	1
I_{IL} @ A	–		–	–3V to 3V	–2V	Open	Open		Open	1
V_{OL} @ Y	–		–	–3V to 3V	–25mV	16mA	V_{IH}		V_{IH}	1
V_{OH} @ Y	–		–	–3V to 3V	+25mV	–400μA	V_{IH}		V_{IH}	1 & 2
V_{OH} @ Y	–		–	–3V to 3V	–25mV	–400μA	V_{IL}		V_{IH}	1 & 2
V_{OH} @ Y	–		–	–3V to 3V	–25mV	–400μA	V_{IH}		V_{IL}	1 & 2
I_{OH} @ Y	–		–	–3V to 3V	+25mV	V_{CC+}MAX.	V_{IH}		V_{IH}	1 & 3
I_{OH} @ Y	–		–	–3V to 3V	–25mV	V_{CC+}MAX.	V_{IL}		V_{IH}	1 & 3
I_{OH} @ Y	–		–	–3V to 3V	–25mV	V_{CC+}MAX.	V_{IH}		V_{IL}	1 & 3
I_{IH} @ 1G	+25mV	GND	GND	–	–	Open	V_{IH}	GND	GND	–
I_{IH} @ 2G	GND	+25mV	GND	–	–	Open	GND	V_{IH}	GND	–
I_{IH} @ S	+25mV	+25mV	GND	–	–	Open	GND	GND	V_{IH}	–
I_{IL} @ 1G	–25mV	GND	GND	–	–	Open	V_{IL}	GND	4.5V	–
I_{IL} @ 2G	GND	–25mV	GND	–	–	Open	GND	V_{IL}	4.5V	–
I_{IL} @ S	–25mV	–25mV	GND	–	–	Open	4.5V	4.5V	V_{IL}	–
I_{OS} @ Y	+25mV		GND	–	–	GND	GND		GND	–
I_{CC+}	+25mV		GND	–	–	Open	+5V		+5V	–
I_{CC-}	+25mV		GND	–	–	Open	+5V		+5V	–

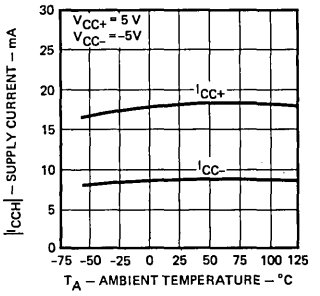
Notes: 1. When testing one channel, the inputs of the other channels are grounded.
2. Am55/75107B only.
3. Am55/75108B only.
4. Am75207 and Am75208 substitute 10mV for 25mV where required.

PERFORMANCE CURVES

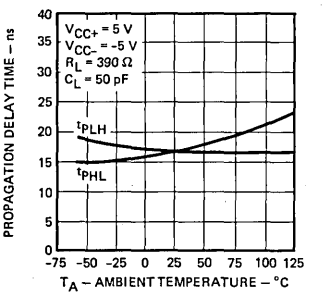
High-Level Input Current Into 1A or 2A Versus Ambient Temperature



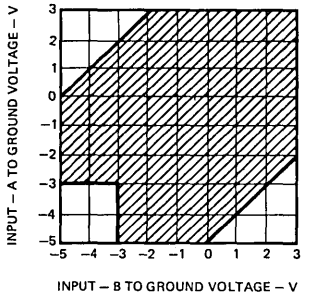
High-Logic-Level Supply Current Versus Ambient Temperature



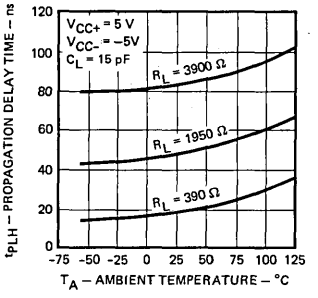
Am55107B, Am75107B Propagation Delay Time Differential Inputs Versus Ambient Temperature



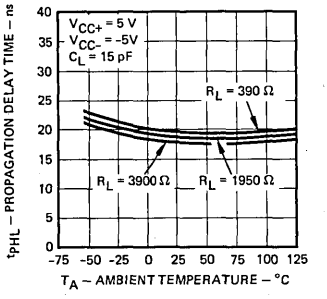
Recommended Combinations of Input Voltage for Line Receivers



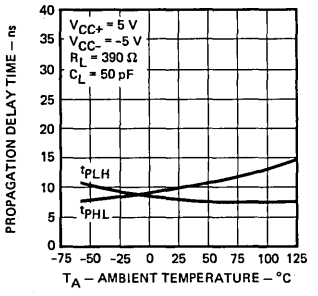
Am55108B, Am75108B Propagation Delay Time Low-to-High Level Differential Inputs Versus Ambient Temperature



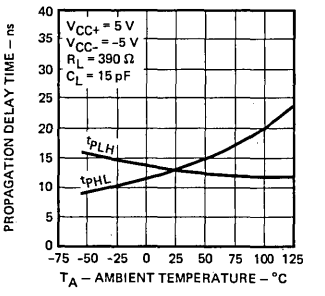
Am55108B, Am75108B Propagation Delay Time High-to-Low Level Differential Inputs Versus Ambient Temperature



Am55107B, Am75107B Propagation Delay Time Strobe Inputs Versus Ambient Temperature



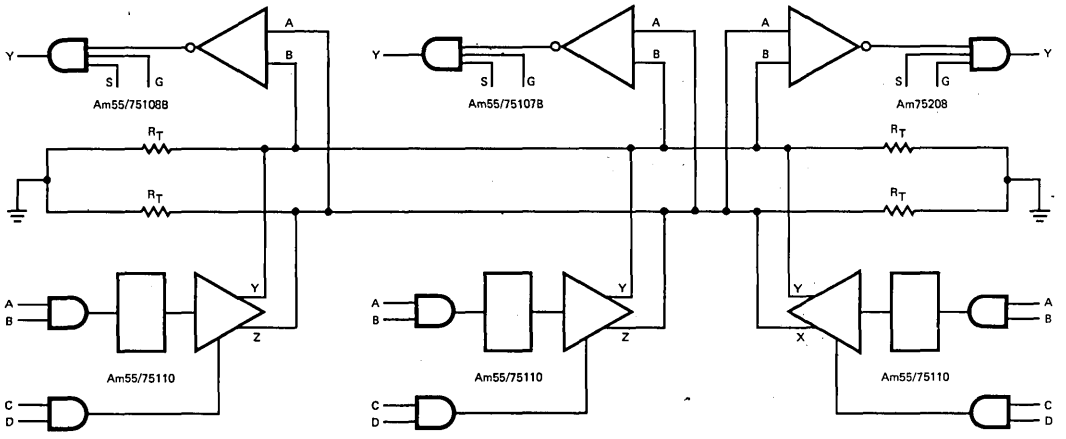
Am55108B, Am75108B Propagation Delay Time Strobe Inputs Versus Ambient Temperature



Note: Use 0°C to +70°C temperature range only for commercial (Am75 Series) devices.

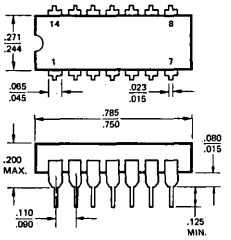
APPLICATIONS

BUS-ORGANIZED SYSTEM

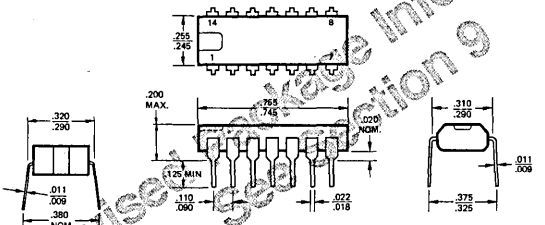


PHYSICAL DIMENSIONS
Dual-In-Line

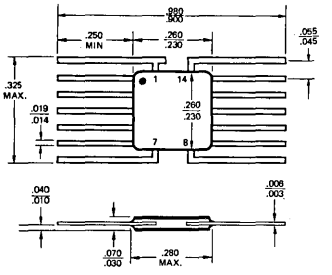
Ceramic



Molded

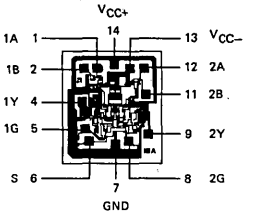


Flat Package



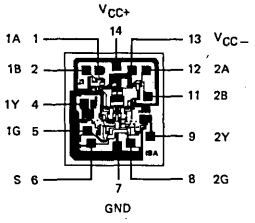
Metallization and Pad Layouts

Am55/75107B
Am75207



DIE SIZE: 0.049" X 0.056"

Am55/75108B
Am75208



DIE SIZE: 0.049" X 0.056"

ADVANCED
MICRO
DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am55/75109 • Am55/75110

Dual Line Drivers

Distinctive Characteristics

- Input is TTL compatible.
- High common-mode output range of −3V to +10V.
- Separate and common output inhibits.
- Open-collector differential outputs for bus-organized systems.
- 100% reliability assurance testing in compliance with MIL-STD-883.

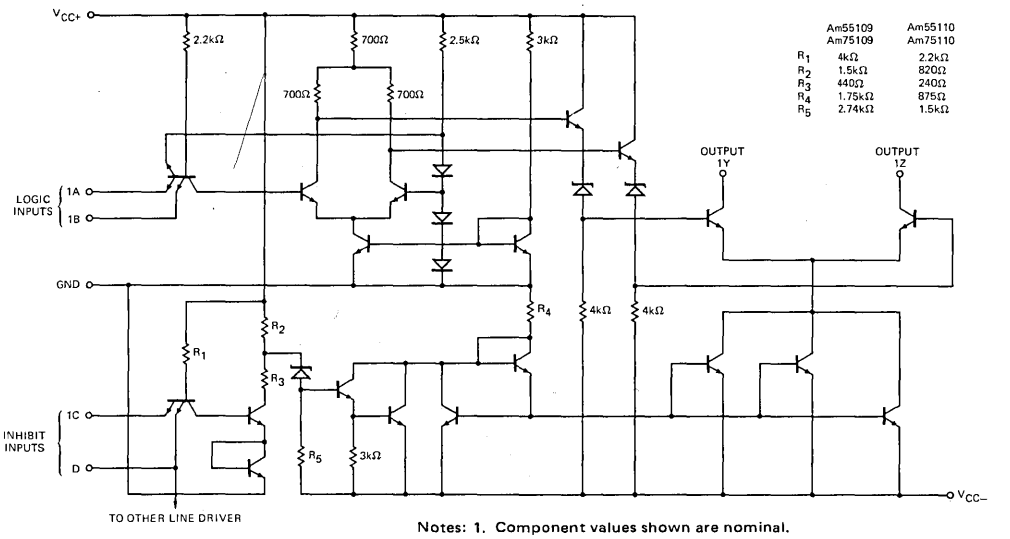
FUNCTIONAL DESCRIPTION

The Am55/75109 and Am55/75110 are dual line drivers characterized for applications in balanced, unbalanced, and party-line systems. The drivers provide a constant current output that is switched to either of the two differential output terminals under the control of the A and B inputs. When A and B are HIGH, the Y output is HIGH and Z output is LOW

These drivers feature a separate inhibit input, C, that is used to switch off the constant current output. This leaves the driver differential output in the high impedance state for use in bus organized systems. A LOW on the C input forces the driver to the OFF state by switching off the current source of the differential output transistor pair. Likewise, the two drivers have a common inhibit input, D, that forces both drivers to the OFF state. A LOW on the D inputs turns off the output current sources of both drivers such that both differential outputs are in the high impedance state.

The driver outputs have a common mode voltage range of −3V to +10V. The Am55/75109 output current is typically 6mA while the Am55/75110 output current is typically 12mA.

SCHEMATIC DIAGRAM
(One Driver Shown)



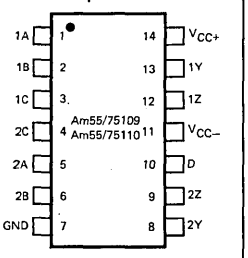
	Am55109 Am75109	Am55110 Am75110
R_1	4kΩ	2.2kΩ
R_2	1.5kΩ	820Ω
R_3	440Ω	240Ω
R_4	1.75kΩ	875Ω
R_5	2.74kΩ	1.5kΩ

Notes: 1. Component values shown are nominal.
2. Resistance values are in ohms.

ORDERING INFORMATION

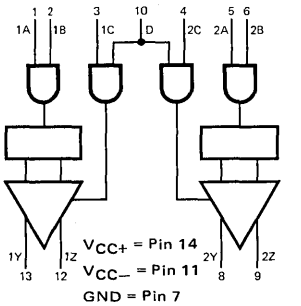
Package Type	Temperature Range	Am55/75109 Order Number	Am55/75110 Order Number
Molded DIP	0°C to +70°C	SN75109N	SN75110N
Hermetic DIP	0°C to +70°C	SN75109J	SN75110J
Dice	0°C to +70°C	SN75109X	SN75110X
Hermetic DIP	−55°C to +125°C	SN55109J	SN55110J
Dice	−55°C to +125°C	SN55109X	SN55110X

CONNECTION DIAGRAM
Top View



Note:
Pin 1 is marked for orientation.

LOGIC SYMBOL



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC+} Supply Voltage to Ground Potential	+7V
V_{CC-} Supply Voltage to Ground Potential	−7V
Common Mode DC Voltage Applied to Outputs	−5V to +12V
DC Input Voltage	−0.5V to $+V_{CC+}$max.
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am75109, Am75110 $T_A = 0°C$ to $+70°C$ $V_{CC+} = 5.0V \pm 5\%$ $V_{CC-} = -5.0V \pm 5\%$
Am55109, Am55110 $T_A = -55°C$ to $+125°C$ $V_{CC+} = 5.0V \pm 10\%$ $V_{CC-} = -5.0V \pm 10\%$
Am75109, Am75110 V_{CC+} MIN. = 4.75V V_{CC+} MAX. = 5.25V V_{CC-} MIN. = −4.75V V_{CC-} MAX. = −5.25V
Am55109, Am55110 V_{CC+} MIN. = 4.5V V_{CC+} MAX. = 5.5V V_{CC-} MIN. = −4.5V V_{CC-} MAX. = −5.5V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0		5.5	Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		0		0.8	Volts
I_{IL} (Note 3)	Input Low Current Am55/75109	V_{CC+} = MAX., V_{IN} = 0.4 V, V_{CC-} = MAX.	A, B			−3	mA
			C			−1.6	
			D			−3	
I_{IL} (Note 3)	Input LOW Current Am55/75110	V_{CC+} = MAX., V_{IN} = 0.4 V, V_{CC-} = MAX.	A, B, C			−3	mA
			D			−6	
I_{IH} (Note 3)	Input HIGH Current	V_{CC+} = MAX., V_{IN} = 2.4 V, V_{CC-} = MAX.	A, B, C			40	µA
			D			80	
I_I	Input HIGH Current	V_{CC+} = MAX., V_{IN} = MAX., V_{CC-} = MAX.	A, B, C			1	mA
			D			2	
I_O(on)	Output Current On-State	V_{CC+} = MAX., V_{CC-} = MAX.	109			7	mA
			110			15	
I_O(on)	Output Current On-State	V_{CC+} = MIN., V_{CC-} = MAX.	109	3.5			mA
			110	6.5			
I_O(off)	Output Current Off-State	V_{CC+} = MIN., V_{CC-} = MIN.				100	µA
I_{CC+}(on)	Positive Supply Current; Driver Enabled	A and B = 0.4V, C and D = 2.0V	109		18	30	mA
			110		23	35	
I_{CC-}(on)	Negative Supply Current; Driver Enabled	A and B = 0.4V, C and D = 2.0V	109		−18	−30	mA
			110		−34	−50	
I_{CC+}(off)	Positive Supply Current; Driver Disabled	All Inputs = 0.4V	109		18		mA
			110		21		
I_{CC-}(off)	Negative Supply Current; Driver Disabled	All Inputs = 0.4V	109		−10		mA
			110		−17		

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC+} = 5.0V$, $V_{CC-} = -5.0V$, $T_A = 25°C$ ambient and maximum loading.
3. Actual input currents = Unit Load Current X Input Load Factor (See Loading Rules).

Switching Characteristics ($T_A = +25°C$)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	A or B to Y or Z	$V_{CC+} = 5.0V$, $V_{CC-} = -5.0V$, $R_L = 50\Omega$, $C_L = 40$ pF		9	15	ns
t_{PHL}	A or B to Y or Z			9	15	ns
t_{PLH}	C or D to Y or Z			16	25	ns
t_{PHL}	C or D to Y or Z			13	25	ns

FUNCTION TABLE

LOGIC INPUTS		INHIBIT INPUTS		OUTPUTS	
A	B	C	D	Y	Z
X	X	L	X	OFF	OFF
X	X	X	L	OFF	OFF
L	X	H	H	ON	OFF
X	L	H	H	ON	OFF
H	H	H	H	OFF	ON

H = HIGH
L = LOW
ON = I_O(on) Current
OFF = I_O(off) Current
X = Don't Care

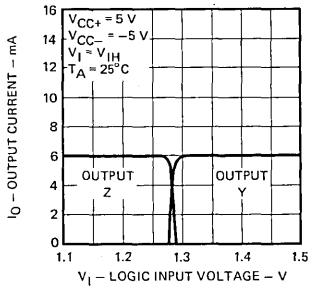
LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load Am55/75109	Input Unit Load Am55/75110	Fan-out Output HIGH	Fan-out Output LOW
1A	1	1-7/8	1-7/8	–	–
1B	2	1-7/8	1-7/8	–	–
1C	3	1	1-7/8	–	–
2C	4	1	1-7/8	–	–
2A	5	1-7/8	1-7/8	–	–
2B	6	1-7/8	1-7/8	–	–
GND	7	–	–	–	–
2Y	8	–	–	(Diff output)	
2Z	9	–	–		
D	10	1-7/8	3-3/4	–	–
V_{CC-}	11	–	–	–	–
1Z	12	–	–	(Diff output)	
1Y	13	–	–		
V_{CC+}	14	–	–	–	–

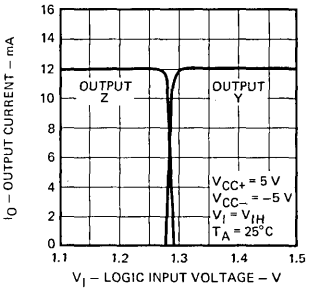
A TTL Unit Load is defined as 40 μA measured at 2.4 V HIGH and –1.6mA measured at 0.4 V LOW.

PERFORMANCE CURVES
(Typical)

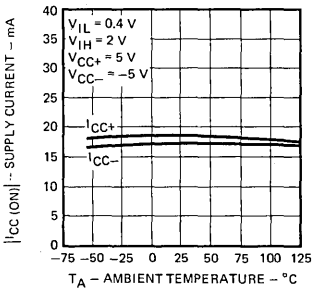
Am55109, Am75109
Output Current
Versus
Logic Input Voltage



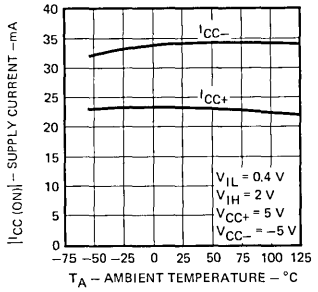
Am55110, Am75110
Output Current
Versus
Logic Input Voltage



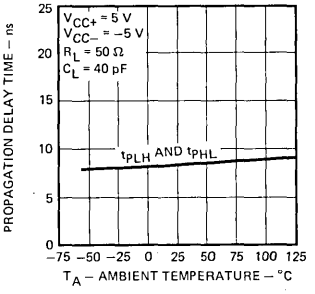
Am55109, Am75109
Supply Current With Driver Enabled
Versus
Ambient Temperature



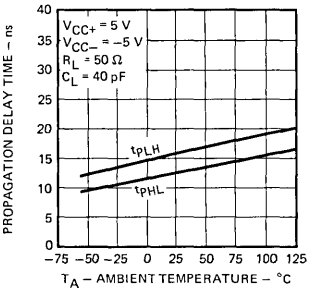
Am55110, Am75110
Supply Current With Driver Enabled
Versus
Ambient Temperature



Propagation Delay Time
Logic Inputs
Versus
Ambient Temperature



Propagation Delay Time
Inhibit Inputs
Versus
Ambient Temperature



Note: For Am75 Series use 0°C to +70°C temperature range only.

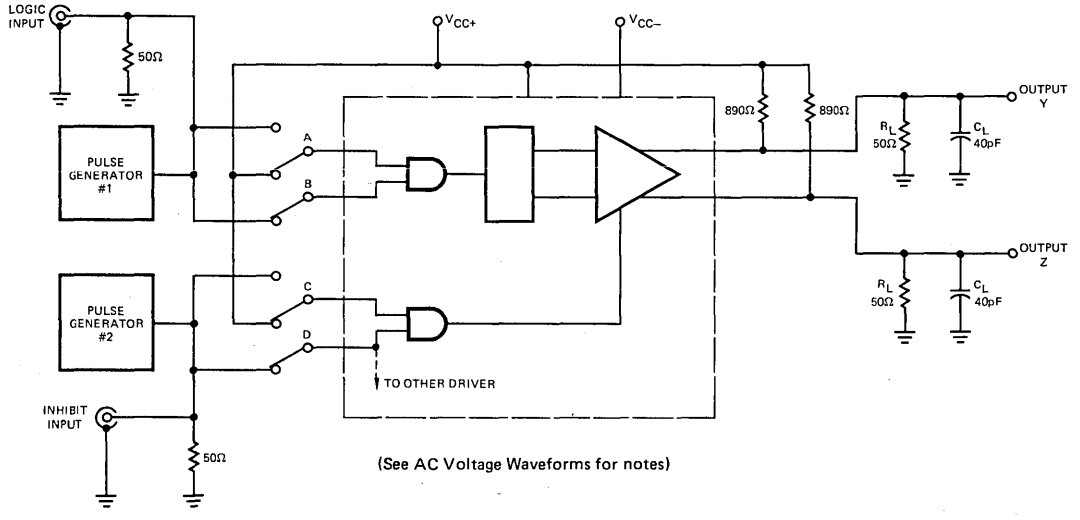
DC TEST TABLE

Parameter	INPUTS A	B	C	D	OUTPUTS Y	Z
V_{IH}	Test	Open	V_{IH}	V_{IH}	OFF	ON
V_{IH}	Open	Test	V_{IH}	V_{IH}	OFF	ON
V_{IL}	Test	V_{CC+}	V_{IH}	V_{IH}	ON	OFF
V_{IL}	V_{CC+}	Test	V_{IH}	V_{IH}	ON	OFF
I_{IH}	Test	GND	V_{IH}	V_{IH}	GND	GND
I_{IH}	GND	Test	V_{IH}	V_{IH}	GND	GND
I_{IL}	Test	4.5V	V_{IH}	V_{IH}	GND	GND
I_{IL}	4.5V	Test	V_{IH}	V_{IH}	GND	GND
V_{IH}	V_{IH}	V_{IH}	Test	Open	OFF	ON
V_{IH}	V_{IH}	V_{IH}	Open	Test	OFF	ON
V_{IH}	V_{IL}	V_{IL}	Test	Open	ON	OFF
V_{IH}	V_{IL}	V_{IL}	Open	Test	ON	OFF
V_{IL}	V_{IH}	V_{IH}	Test	Open	OFF	OFF
V_{IL}	V_{IH}	V_{IH}	Open	Test	OFF	OFF
V_{IL}	V_{IL}	V_{IL}	Test	V_{CC+}	OFF	OFF
V_{IL}	V_{IL}	V_{IL}	V_{CC+}	Test	OFF	OFF
I_{IH}	GND	GND	Test	GND	GND	GND
I_{IH}	GND	GND	GND	Test	GND	GND
I_{IL}	GND	GND	Test	4.5V	GND	GND
I_{IL}	GND	GND	4.5V	Test	GND	GND
$I_{O(on)}$	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Test	Note 1
$I_{O(on)}$	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Test	Note 1
$I_{O(on)}$	V_{IH}	V_{IL}	V_{IH}	V_{IH}	Test	Note 1
$I_{O(on)}$	V_{IH}	V_{IH}	V_{IH}	V_{IH}	Note 1	Test
$I_{O(off)}$	V_{IH}	V_{IH}	V_{IH}	V_{IH}	Test	Note 1
$I_{O(off)}$	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Note 1	Test
$I_{O(off)}$	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Note 1	Test
$I_{O(off)}$	V_{IH}	V_{IL}	V_{IH}	V_{IH}	Note 1	Test
$I_{O(off)}$	X	X	V_{IL}	V_{IL}	Test	Test
$I_{O(off)}$	X	X	V_{IL}	V_{IH}	Test	Test
$I_{O(off)}$	X	X	V_{IH}	V_{IL}	Test	Test
$I_{CC+(on)}$	V_{IL}	V_{IL}	V_{IH}	V_{IH}	GND	GND
$I_{CC-(on)}$	V_{IL}	V_{IL}	V_{IH}	V_{IH}	GND	GND
$I_{CC+(off)}$	V_{IL}	V_{IL}	V_{IL}	V_{IL}	GND	GND
$I_{CC-(off)}$	V_{IL}	V_{IL}	V_{IL}	V_{IL}	GND	GND

X = Don't Care; Note 1: Output not under test must have a low impedance (<50Ω) termination to GND.

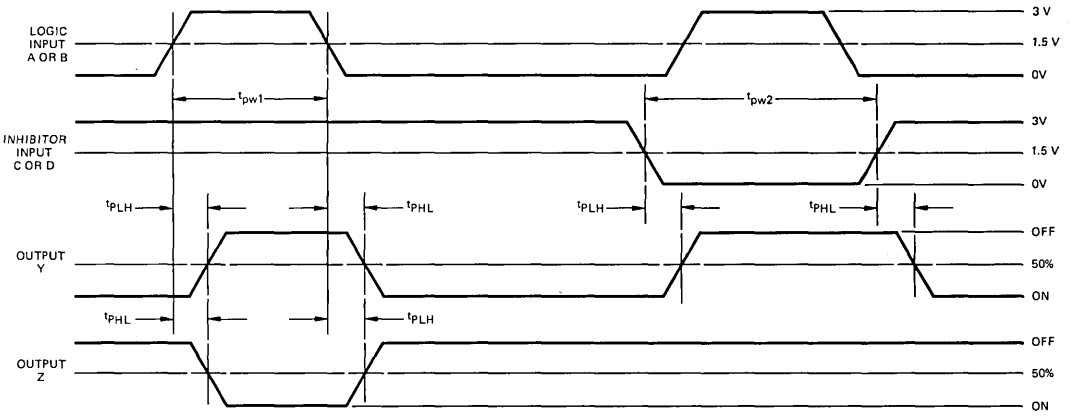
AC PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT



(See AC Voltage Waveforms for notes)

AC VOLTAGE WAVEFORMS



Notes: 1. The pulse generators have the following characteristics: $Z_{out} = 50\Omega$, $t_r = t_f = 10 \pm 5$ns; $t_{pw1} = 500$ns, PRR = 1 MHz; $t_{pw2} = 1$ms, PRR = 500kHz.

2. C_L includes probe and jig capacitance.

3. For simplicity, only one channel and the inhibitor connections are shown.

DEFINITION OF STANDARD TERMS

H HIGH, applying to a HIGH voltage level.

L LOW, applying to a LOW voltage level.

I Input.

O Output.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

I_{IL} LOW-level input current with a specified LOW-level voltage applied.

I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.

I_{OL} LOW-level output current.

I_{OH} HIGH-level output current.

I_{SC} Output short-circuit source current.

I_{CC} The supply current drawn by the device from the V_{CC} power supply.

V_{IL} Logic LOW input voltage.

V_{IH} Logic HIGH input voltage.

V_{OL} LOW-level output voltage with I_{OL} applied.

V_{OH} HIGH-level output voltage with I_{OH} applied

UNIT LOAD DEFINITIONS

	HIGH		LOW	
SERIES	Current	Measure Voltage	Current	Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0mA	0.5V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

Note: 1. 54L/74L has two different types of standard inputs.

DEFINITION OF FUNCTIONAL TERMS

1A, 2A, 1B, 2B The TTL data inputs to each driver.

1C, 2C The TTL inhibit inputs to each driver. A LOW input forces both outputs to the off-state.

D The common TTL inhibit input to both drivers. A LOW input forces all four outputs to the off-state.

1Y, 2Y, 1Z, 2Z The differential output of each driver.

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

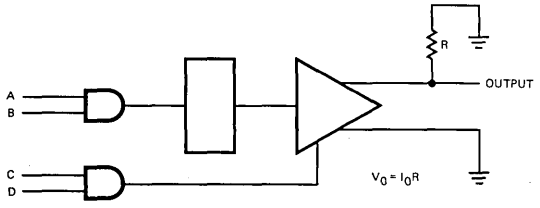
t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{PW} Pulse width. The time between the leading and trailing edges of a pulse.

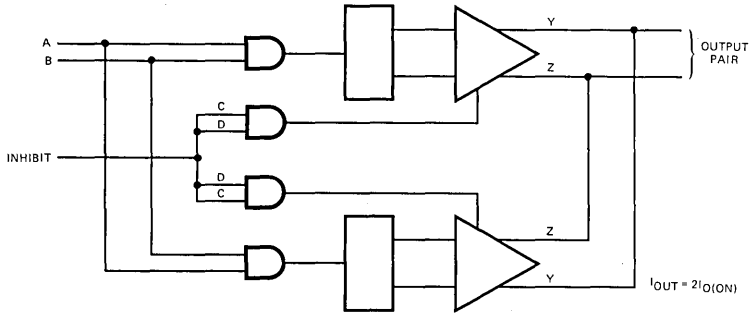
t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

APPLICATIONS



Am55/75109 or Am55/75110 in a unbalanced or single-ended connection.

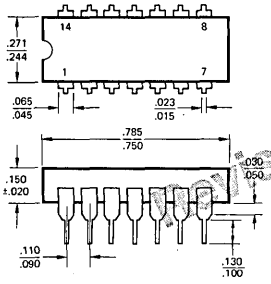


Two line drivers connected in parallel for higher current.

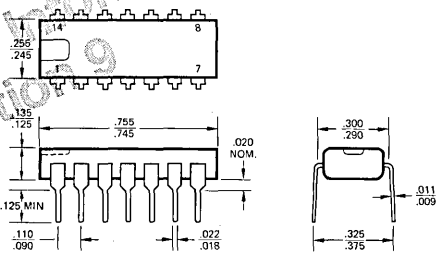
PHYSICAL DIMENSIONS

Dual-In-Line

Ceramic

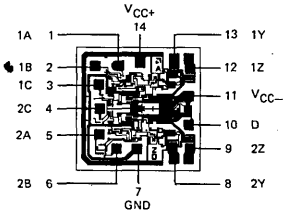


Molded



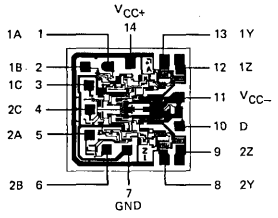
Metallization and Pad Layouts

Am55/75109



DIE SIZE 0.056" X 0.056"

Am55/75110



DIE SIZE 0.056" X 0.056"

ADVANCED
MICRO
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901 Thompson Place
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TELEX: 34-6306

Am54/74221

Dual Monostable Multivibrators with Schmitt-Trigger Inputs

Distinctive Characteristics

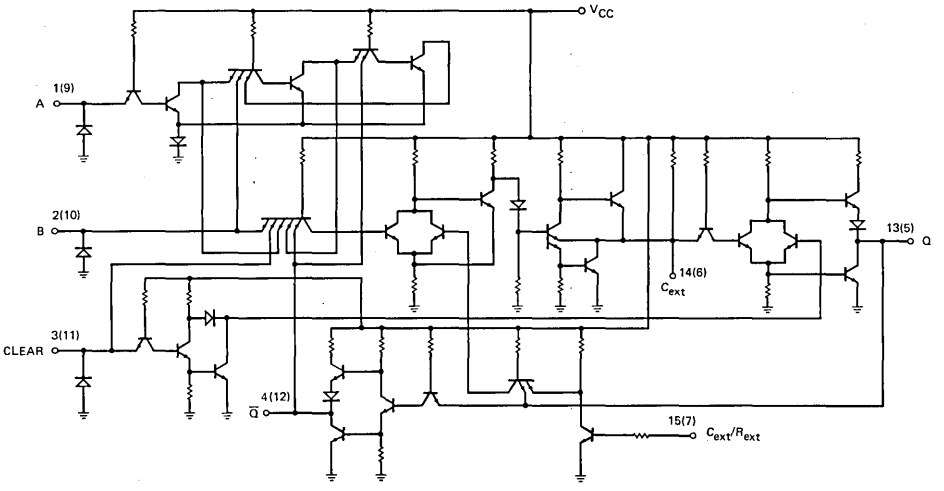
- Dual, highly stable, one-shot.
- Pin-out is identical to the Am54/74123.
- Overriding clear terminates the output pulse.
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

The Am54/74221 dual monostable multivibrators feature negative-transition and positive-transition trigger inputs. The negative-transition input (A) is a standard TTL input. The positive-transition input (B) incorporates a Schmitt-trigger circuit with sufficient hysteresis to allow jitter-free triggering from inputs with transition rates as slow as 1.0V per second while maintaining a typical noise immunity of 1.2V. For both the A and B inputs, triggering occurs a voltage level and is not a function of the input transition time.

Once triggered, the output pulse is independent of the A and B inputs and is a function of the external timing components R_{ext} and C_{ext}. The output pulse is terminated or further triggering inhibited when the direct overriding clear is LOW. The A or B input pulse may be of any duration relative to the output pulse. The device can be triggered from the clear input if the proper conditions are met as shown in the switching waveforms. The timing equation is: $t_{pw}Q \approx 0.7\ C_{ext}\ R_{ext}$.

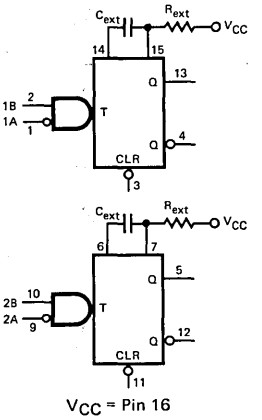
SCHEMATIC DIAGRAM
(One Multivibrator Shown)



ORDERING INFORMATION

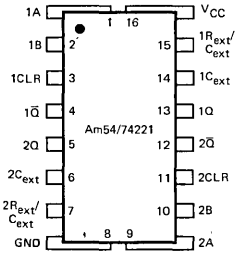
Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	SN74221N
Hermetic DIP	0°C to +70°C	SN74221J
Dice	0°C to +70°C	SN74221X
Hermetic DIP	−55°C to +125°C	SN54221J
Hermetic Flat Pak	−55°C to +125°C	SN54221W
Dice	−55°C to +125°C	SN54221X

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am74221 T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am54221 T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL) MIN. = 4.5V MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −800μA, V_{IN} = V_{IH} or V_{IL}		2.4	3.4		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA, V_{IN} = V_{IH} or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for A and Clear inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for A and Clear inputs				0.8	Volts
V_{T+}	B Input Positive – Going Threshold Voltage	V_{CC} = MIN.			1.55	2.0	Volts
V_{T-}	B Input Negative – Going Threshold Voltage	V_{CC} = MIN.		0.8	1.35		Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −12mA				−1.5	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	A			−1.6	mA
			B, Clear			−3.2	
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V	A			40	μA
			B, Clear			80	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1	mA
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0V	Am54221	−20		−55	mA
			Am74221	−18		−55	
I_{CC}	Power Supply Current	V_{CC} = MAX.	Quiescent		26	50	mA
			Triggered		46	80	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current X Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Switching Characteristics (T_A = +25°C, C_L = 15 pF, R_L = 400Ω)

Parameters	Description		Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	A to Q		R_{ext} = 2kΩ, C_{ext} = 80 pF		45	70	ns
t_{PHL}	A to $\overline{Q}$				50	80	
t_{PLH}	B to Q				35	55	ns
t_{PHL}	B to $\overline{Q}$				40	65	
t_{PHL}	Clear to Q				9	27	ns
t_{PLH}	Clear to $\overline{Q}$				19	40	
dv/dt	Rate of Rise or Fall of B Input			1			V/s
dv/dt	Rate of Rise or Fall of A Input			1			V/μs
t_{pw}	Pulse Width	A or B		50			ns
		Clear		20			
t_s	Clear Inactive State (Recovery) Set-up Time			15			ns
R_{ext}	External Timing Resistance	Am54221		1.4		30	kΩ
		Am74221		1.4		40	
C_{ext}	External Timing Capacitance			0		1000	μF
—	Output Duty Cycle	R_{ext} = 2kΩ				67	%
•		R_{ext} = R_{ext} MAX.				90	
$t_{pw}Q$	Triggered Output Pulse Width		R_{ext} = 2kΩ, C_{ext} = 80 pF	70	110	150	ns
$t_{pw}Q$	Triggered Output Pulse Width		R_{ext} = 2kΩ, C_{ext} = Open	20	30	50	ns
$t_{pw}Q$	Triggered Output Pulse Width		R_{ext} = 10kΩ, C_{ext} = 100 pF	650	700	750	ns
$t_{pw}Q$	Triggered Output Pulse Width		R_{ext} = 10kΩ, C_{ext} = 1μF	6.5	7	7.5	ms

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
1A	1	1	–	–
1B	2	2	–	–
1Clear	3	2	–	–
$1\overline{Q}$	4	–	20	10
1Q	5	–	20	10
$2C_{ext}$	6	–	–	–
$2R_{ext}/C_{ext}$	7	–	–	–
GND	8	–	–	–
2A	9	1	–	–
2B	10	2	–	–
2Clear	11	2	–	–
$2\overline{Q}$	12	–	20	10
2Q	13	–	20	10
$2C_{ext}$	14	–	–	–
$2R_{ext}/C_{ext}$	15	–	–	–
V_{CC}	16	–	–	–

A TTL Unit Load is defined as 40μA measured at 2.4V HIGH and −1.6mA measured at 0.4V LOW.

FUNCTION TABLE

INPUTS			OUTPUTS		NOTES
Clear	A	B	Q	$\overline{Q}$	
L	X	X	L	H	
X	H	X	L	H	2
X	X	L	L	H	2
H	L	↑	⎍	⎴	
H	↓	H	⎍	⎴	
↑	L	↑	⎍	⎴	1
↑	L	↑	L	H	1
↑	↓	H	⎍	⎴	1

L = LOW
H = HIGH
↑ = LOW-to-HIGH Transition
↓ = HIGH-to-LOW Transition
⎍ = LOW-HIGH-LOW Pulse
⎴ = HIGH-LOW-HIGH Pulse
X = Don't Care

Notes: 1. See switching waveforms for conditions.
2. Output in quiescent state initially.

DEFINITION OF FUNCTIONAL TERMS

A The active LOW trigger input. With the B input HIGH, a HIGH-to-LOW transition will trigger the monostable multivibrator.

B The active-HIGH trigger input. With the A input LOW, a LOW-to-HIGH transition will trigger the monostable multivibrator.

Clear The asynchronous direct clear input. A LOW on the clear input forces the Q output LOW and the $\overline{Q}$ output HIGH regardless of the other inputs. For certain A and B input conditions, the device will trigger when the clear is removed.

Q The TRUE monostable output.

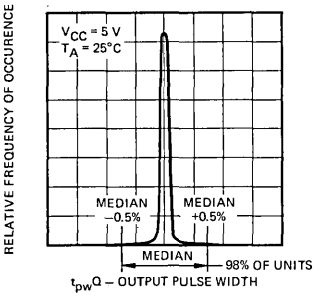
$\overline{Q}$ The complement monostable output.

C_{ext} One connection for the external timing capacitor.

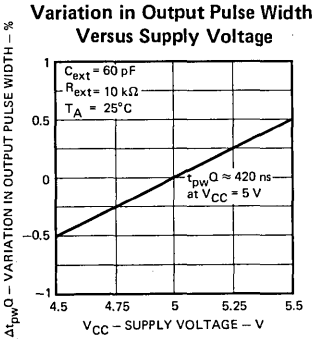
C_{ext}/R_{ext} The connection for the timing capacitor and timing resistor.

PERFORMANCE CURVES

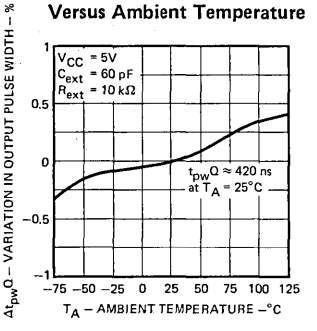
Distribution of Units for Output Pulse Width



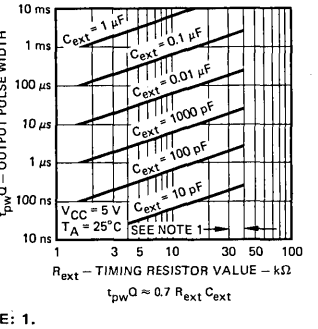
Variation in Output Pulse Width Versus Supply Voltage



Variation in Output Pulse Width Versus Ambient Temperature



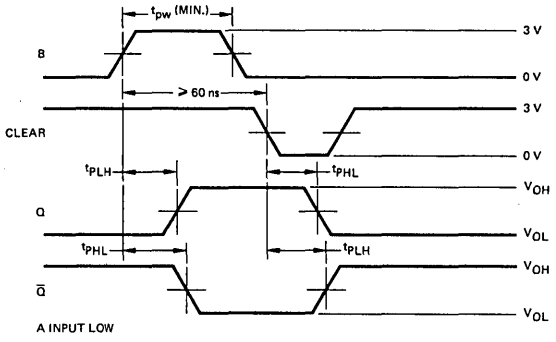
Output Pulse Width Versus Timing Resistor Value



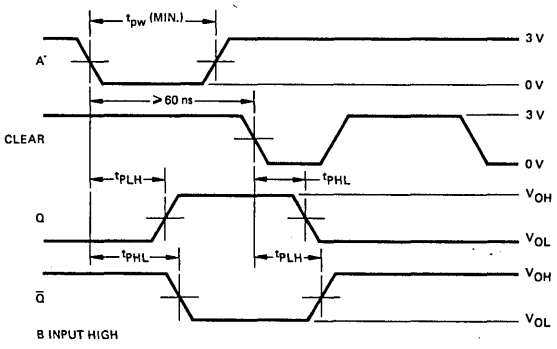
NOTE: 1.
These values of resistance exceed the maximum recommended for use over the full temperature range of the Am54221.

SWITCHING WAVEFORMS

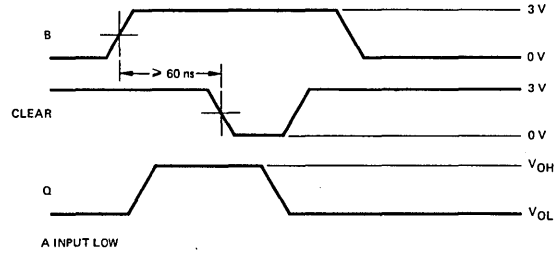
TRIGGER FROM B, THEN CLEAR–CONDITION 1



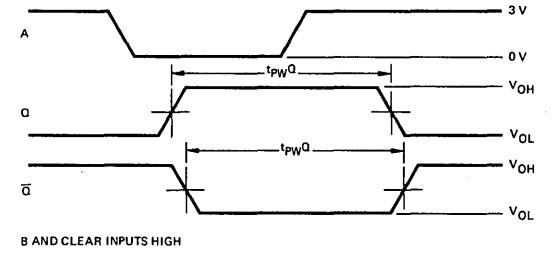
TRIGGER FROM A, THEN CLEAR



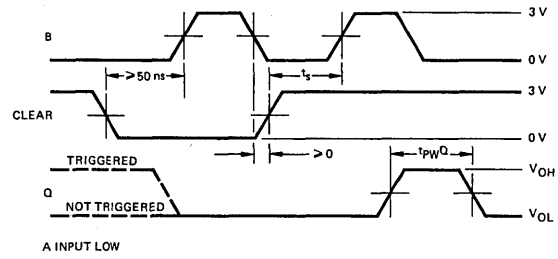
TRIGGER FROM B, THEN CLEAR–CONDITION 2



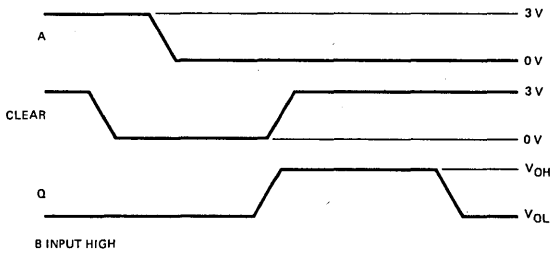
TRIGGER FROM A



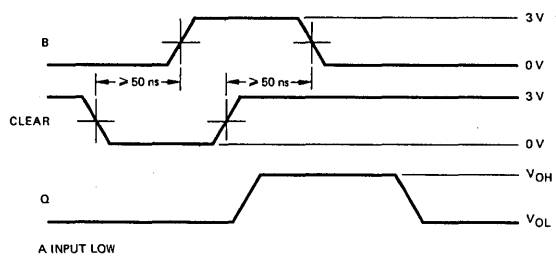
CLEAR OVERRIDING B, THEN TRIGGER FROM B



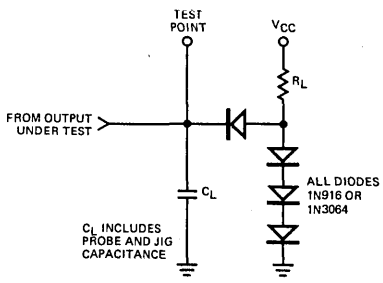
TRIGGER FROM POSITIVE TRANSITION OF CLEAR



TRIGGERING FROM POSITIVE TRANSITION OF CLEAR



LOAD TEST CIRCUIT



Notes: 1. Input pulse are supplied by generators having the following characteristics: $t_r \leq 7$ ns, $t_f \leq 7$ ns, PRR ≤ 1 MHz, and $Z_{out} \approx 50\ \Omega$.
2. All measurements are made between the 1.5 V points of the indicated transitions.

DEFINITION OF SWITCHING TERMS

(All switching times are measured at the 1.5V logic level unless otherwise noted.)

t_{PLH} The propagation delay time from an input change to an output LOW-to-HIGH transition.

t_{PHL} The propagation delay time from an input change to an output HIGH-to-LOW transition.

t_{PW} Pulse width. The time between the leading and trailing edges of a pulse.

t_r Rise time. The time required for a signal to change from 10% to 90% of its measured values.

t_f Fall time. The time required for a signal to change from 90% to 10% of its measured values.

t_s Set-up time. The time interval for which a signal must be applied and maintained at one input terminal before an active transition occurs at another input terminal.

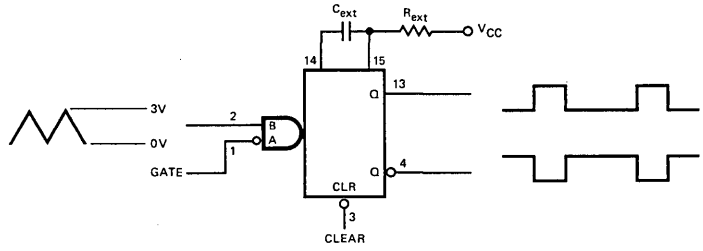
UNIT LOAD DEFINITIONS

	HIGH		LOW	
SERIES	Current	Measure Voltage	Current	Measure Voltage
Am25/26/2700	40μA	2.4V	−1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	−2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	−0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	−0.36mA	0.4V
Am54/74	40μA	2.4V	−1.6mA	0.4V
54H/74H	50μA	2.4V	−2.0mA	0.4V
Am54S/74S	50μA	2.7V	−2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	−0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	−0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	−0.36mA	0.4V
Am9300	40μA	2.4V	−1.6mA	0.4V
Am93L00	20μA	2.4V	−0.4mA	0.3V
Am93S00	50μA	2.7V	−2.0 mA	0.5 V
Am75/85	40μA	2.4V	−1.6mA	0.4V
Am8200	40μA	4.5V	−1.6mA	0.4V

Note: 1. 54L/74L has two different types of standard inputs.

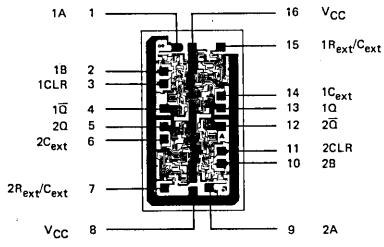
APPLICATION

Triangle (or Sine Wave) to Square-Wave Converter



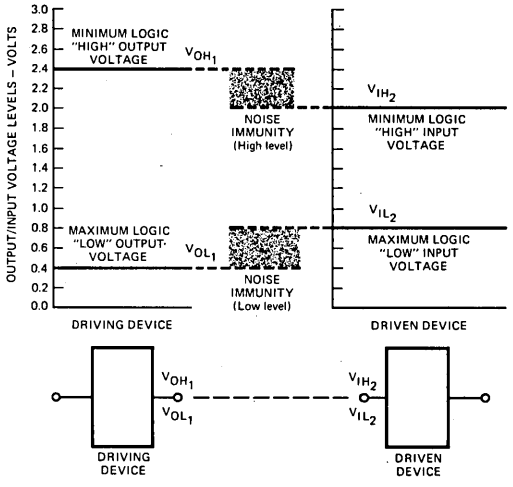
$t_{pw}Q \approx 0.7\ R_{ext}\ C_{ext}$

Metallization and Pad Layout



DIE SIZE 0.049" X 0.089"

INPUT/OUTPUT VOLTAGE INTERFACE CONDITIONS



Note: Refer to Electrical Characteristics for measure current.

DEFINITION OF STANDARD TERMS

H HIGH, applying to a HIGH voltage level.

L LOW, applying to a LOW voltage level.

I Input.

O Output.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

I_{IL} LOW-level input current with a specified LOW-level voltage applied.

I_{IH} HIGH-level input current with a specified HIGH-level voltage applied.

I_{OL} LOW-level output current.

I_{OH} HIGH-level output current.

I_{SC} Output short-circuit source current.

I_{CC} The supply current drawn by the device from the V_{CC} power supply.

V_{IL} Logic LOW input voltage.

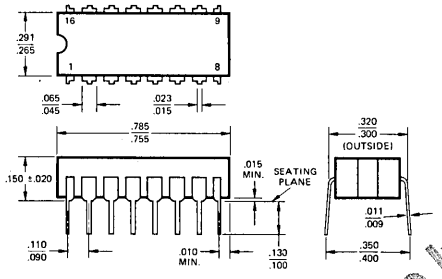
V_{IH} Logic HIGH input voltage.

V_{OL} LOW-level output voltage with I_{OL} applied.

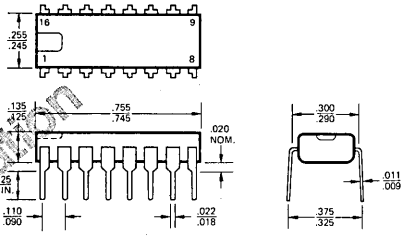
V_{OH} HIGH-level output voltage with I_{OH} applied.

PHYSICAL DIMENSIONS
Dual-In-Line

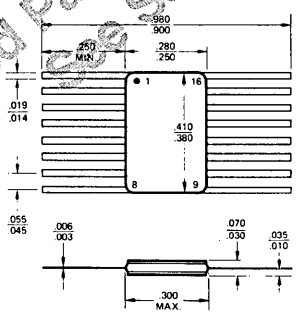
Ceramic



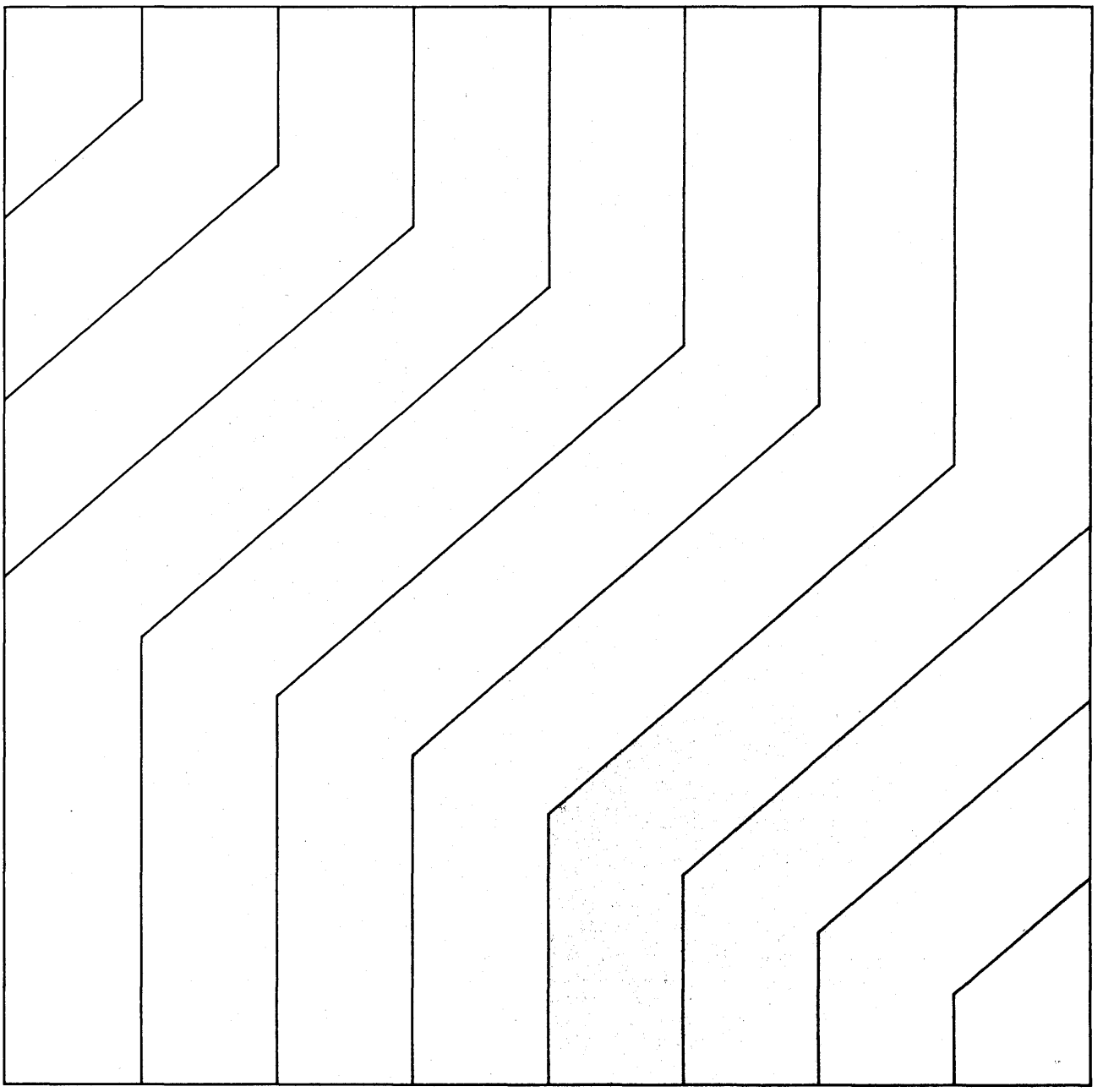
Molded



Flat Package



ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306



Am1101A/1101A1

256-Bit Fully Decoded Random Access Memories

Distinctive Characteristics

- 256-bit fully decoded silicon gate MOS static random access memories.
- Typical access time: 650 ns Am1101A1
  850 ns Am1101A
- Chip select and OR tieable outputs allow easy expansion to large memories.
- 100% reliability assurance testing in compliance with MIL STD 883.

FUNCTIONAL DESCRIPTION

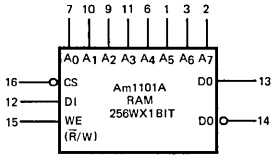
The Advanced Micro Devices' Am1101A and Am1101A1, are silicon gate MOS fully decoded random access 256-word by 1-bit memories. Low threshold silicon gate technology enables the devices to interface directly with standard DTL and TTL circuits. The memories use normally off P-channel MOS devices to form a static memory array that is ideal for use in small buffer memory applications. The Am1101A1 is a selected Am1101A for applications where higher speed is required and the Am1101ADM is a selected Am1101A which operates over the full military temperature range. The memories have an active LOW chip select input and OR tieable complementary outputs for ease of memory expansion. The chip select input can be driven by TTL MSI decoders such as the Am9301.

These memories are operated by applying DTL or TTL logic levels to the device inputs. For a read operation the chip select input, $\overline{CS}$, is held at a LOW logic level. The appropriate pattern is applied to the address inputs and the read/write input is held at a LOW logic level. The information stored in the addressed location is read out on complementary outputs, $\overline{DO}$ and DO, that can directly drive DTL or TTL circuitry. For a write operation, the chip select is held at a LOW logic level 300ns or more after the address has been selected and held HIGH for at least 400ns. This is to allow time for address decoding and to ensure writing data into the correct location. The data to be written into the addressed location must be present for at least 300ns before the end of the write command. During the write operation, if the chip is selected, the data outputs follow the data input line.

When the chip is unselected both the read/write and the data input leads are ineffective and both outputs go to a high impedance "OFF" state. The chip select, however, does not operate on the address decoders. This feature allows an effective increase in memory speed in some applications by using the faster delay from the chip select to the output.

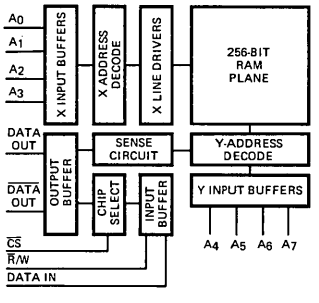
The memory can be operated in a low power standby mode by switching the periphery circuitry supply, V_D, to V_{CC} and maintaining only the cell power supply, V_{DD}, supply current. When a chip is selected, the V_D supply is separated from the V_{CC}. In this mode of operation the chip select and V_D pin can be tied together, allowing full power to be dissipated only in selected chips and considerably reducing the system power in a large memory system.

LOGIC SYMBOL



V_{CC} = PIN 5
V_{DD} = PIN 8
V_D = PIN 4

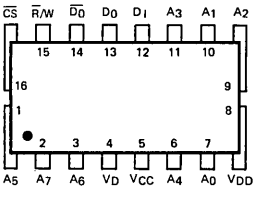
BLOCK DIAGRAM



Am1101A ORDERING INFORMATION

Package Type	Ambient Temperature Range	Order Number
Molded DIP	0°C to +75°C	P1101A
Hermetic DIP	0°C to +75°C	C1101A
Molded DIP	0°C to +75°C	P1101A1
Hermetic DIP	0°C to +75°C	C1101A1
Hermetic DIP	−55°C to +125°C	1101ADM

CONNECTION DIAGRAM
Top View



NOTE: Pin 1 is marked for orientation.

MAXIMUM RATINGS Above which the useful life may be impaired (Note 1)

Storage Temperature	−65°C to +160°C
Temperature (Case) Under Bias (Note 2)	−55°C to +125°C
Power Dissipation at Room Temperature	700 mW
All Input and Output Voltages with respect to the Most Positive Supply Voltage, V_{CC}	+0.3 V to −20 V
Supply Voltages V_{DD} and V_D with respect to V_{CC}	−20 V

OPERATING RANGE

Device	V_{CC}	V_D	V_{DD}	Temperature
1101A, 1101A1	+5.0 ±5%	−9.0 ±5%	−9.0 ±5%	0°C to +75°C
Am1101ADM	+5.0 ±5%	−10.0 ±5%	−10.0 ±5%	−55°C to +125°C

ELECTRICAL CHARACTERISTICS (over operating range unless otherwise specified)

		Am1101A, Am1101A1 (Note 3)			Am1101ADM (Note 3)			
Parameters	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
V_{OH} Output HIGH Voltage	$I_{OH} = -100\ \mu A$	3.5	4.9		3.5	4.9		Volts
V_{OL} Output LOW Voltage	$I_{OL} = -2.0$ mA			0.45				Volts
	$I_{OL} = -1.8$ mA						0.45	
V_{IH} (Note 4) Input HIGH Voltage		$V_{CC}-2$		$V_{CC}+0.3$	$V_{CC}-1$		$V_{CC}+0.3$	Volts
V_{IL} (Note 4) Input LOW Voltage		−10		$V_{CC}-4.5$	−10		$V_{CC}-4.5$	Volts
I_L Input Load Current	$V_{IN} = 0.0$ V		1.0	500		1.0	500	nA
I_{LO} Output Leakage Current	$V_{OUT} = 0.0$ V, $\overline{CS} = V_{IH}$ MIN.		1.0	500		1.0	500	nA
I_{OL} Output Sink Current	$V_{OUT} = 0.45$ V	2.0	8.0		1.8	8.0		mA
	$V_{OUT} = 0.45$ V, $T_A = +25°C$	3.0			3.0			
I_{OH} Output Source Current	$V_{OUT} = 0.0$ V	−2.0	−8.0		−1.8	−8.0		mA
	$V_{OUT} = 0.0$ V, $T_A = +25°C$	−3.0			−3.0			
I_{CEF} Output Clamp Current	$V_{OUT} = -1.0$ V		6	13		6	19	mA
I_{DD} DC Power Supply Current	$I_{OL} = 0.0$ mA, $T_A =$ MIN.			−16			−24	mA
	$I_{OL} = 0.0$ mA, $T_A = 25°C$		−9	−12		−11	−14	
I_D DC Power Supply Current	$I_{OL} = 0.0$ mA, $T_A =$ MIN.			−24			−35	mA
	$I_{OL} = 0.0$ mA, $T_A = 25°C$		−12	−18		−14	−21	
C_{IN} (Note 5) Input Capacitance	$V_{IN} = V_{CC}$, f = 1 MHz		7	10		7	10	pF
C_{OUT} (Note 5) Output Capacitance	$V_{OUT} = V_{CC}$, f = 1 MHz		7	10		7	10	pF
C_D (Note 5) Capacitance on V_D	$V_D = V_{CC}$, f = 1 MHz		20	35		20	35	pF

Note 1: Stresses above those listed in "MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress rating only and functional operation at these or at any other condition above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The thermal resistance θ_{CA} Case to Ambient is to a large extent dependent on ambient conditions such as velocity of air and the positions of packages and mounting boards relative to one another.

Note 3: Typical values are at normal voltage and $T_A = +25°C$.

Note 4: A TTL device driving the memory must have its output HIGH $\geq V_{IH}$ min and its output LOW $< V_{IL}$ max even when driving other circuitry.

Note 5: This parameter is periodically sampled and not 100% tested.

SWITCHING CHARACTERISTICS (Over operating range unless otherwise noted)

(Output load is 1 TTL gate and 20 pF)

Parameters	Description		Conditions	Min.	Typ. (Note 1)	Max.	Units
$t_{pd}(A)$	Access Time, Address to Output HIGH or LOW	Am1101A	$\overline{CS}$ = L See Fig. 1	0.05	0.85	1.5	μs
		Am1101A1		0.05	0.65	1.0	μs
$t_{pd\ on}(\overline{CS})$	Delay, Chip Select to Output Active		Fig. 1	0.05	0.2	0.3	μs
$t_{pd\ off}(\overline{CS})$	Delay, Chip Select to Output HIGH Impedance State		Fig. 1	0.05	0.1	0.3	μs
$t_{pw}(\overline{CS})$	Minimum Chip Select Pulse Width (Note 2)		Fig. 2			0.4	μs
$t_{pw}(W)$	Minimum Write Pulse Width (Note 2)		Fig. 2			0.4	μs
$t_s(A)$	Address Set-Up Time		Fig. 2			0.3	μs
$t_h(A)$	Address Hold Time		Fig. 2			0.1	μs
$t_s(D)$	Data Set-Up Time		Fig. 2			0.3	μs
$t_h(D)$	Data Hold Time		Fig. 2			0.1	μs
T_R	System Read Cycle (defined by $t_{pd}(A)$	Am1101A	Fig. 1	1.5			μs
		Am1101A1		1.0			
T_W	System Write Cycle (defined by t_s max + t_{pw} max + t_h max			0.8			μs

Note 1: Typical speeds are at 25°C ambient.

Note 2: To write, $\overline{CS}$ and W must both be active for at least 400 ns; either signal can be used as a 400 ns "write pulse" if the other one is active during the writing period.

SWITCHING WAVEFORMS

CONDITIONS OF TEST:

Input pulse amplitudes: 0 to 5V, Input pulse rise and fall time: 10 nsec. Speed measurements referenced to 1.5 V levels (unless otherwise noted). Output load is 1 TTL gate and $C_L = 20$ pF; measurements made at output of TTL gate ($t_{PD} \leq 10$ nsec).

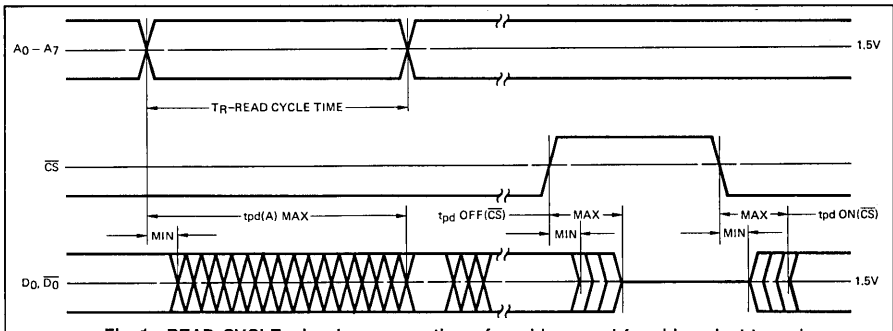


Fig. 1 READ CYCLE, showing access times for address and for chip select to and from the high impedance state.

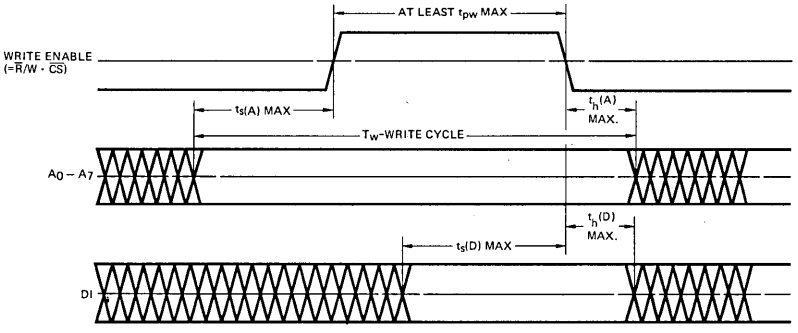


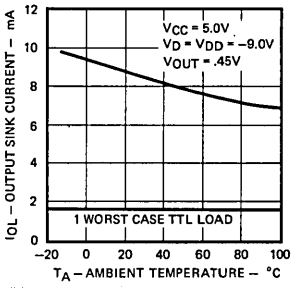
Fig. 2 WRITE CYCLE, showing required set-up times for address and data. The chip select and the write line are active. The data outputs will follow the data input during the write operation.

KEY TO TIMING DIAGRAM

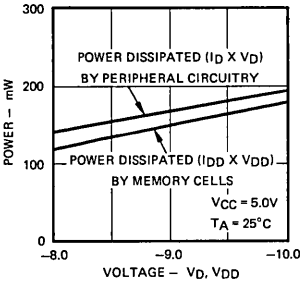
WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

TYPICAL CHARACTERISTICS

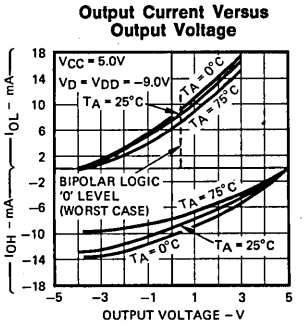
Output Sink Current Versus Temperature



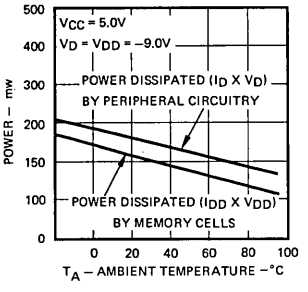
Power Dissipation Versus Voltage



Output Current Versus Output Voltage

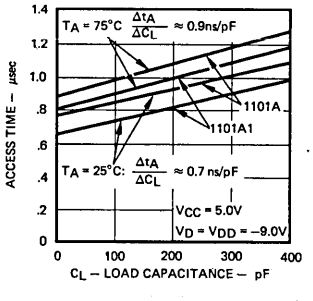


Power Dissipation Versus Ambient Temperature

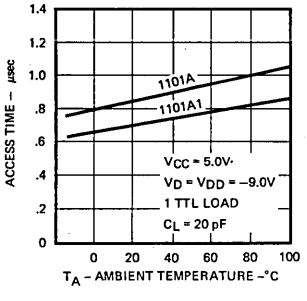


SWITCHING CHARACTERISTICS

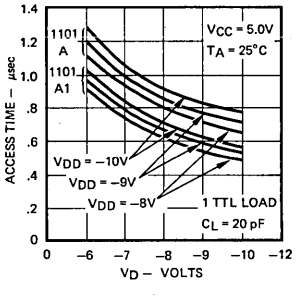
Access Time Versus Load Capacitance



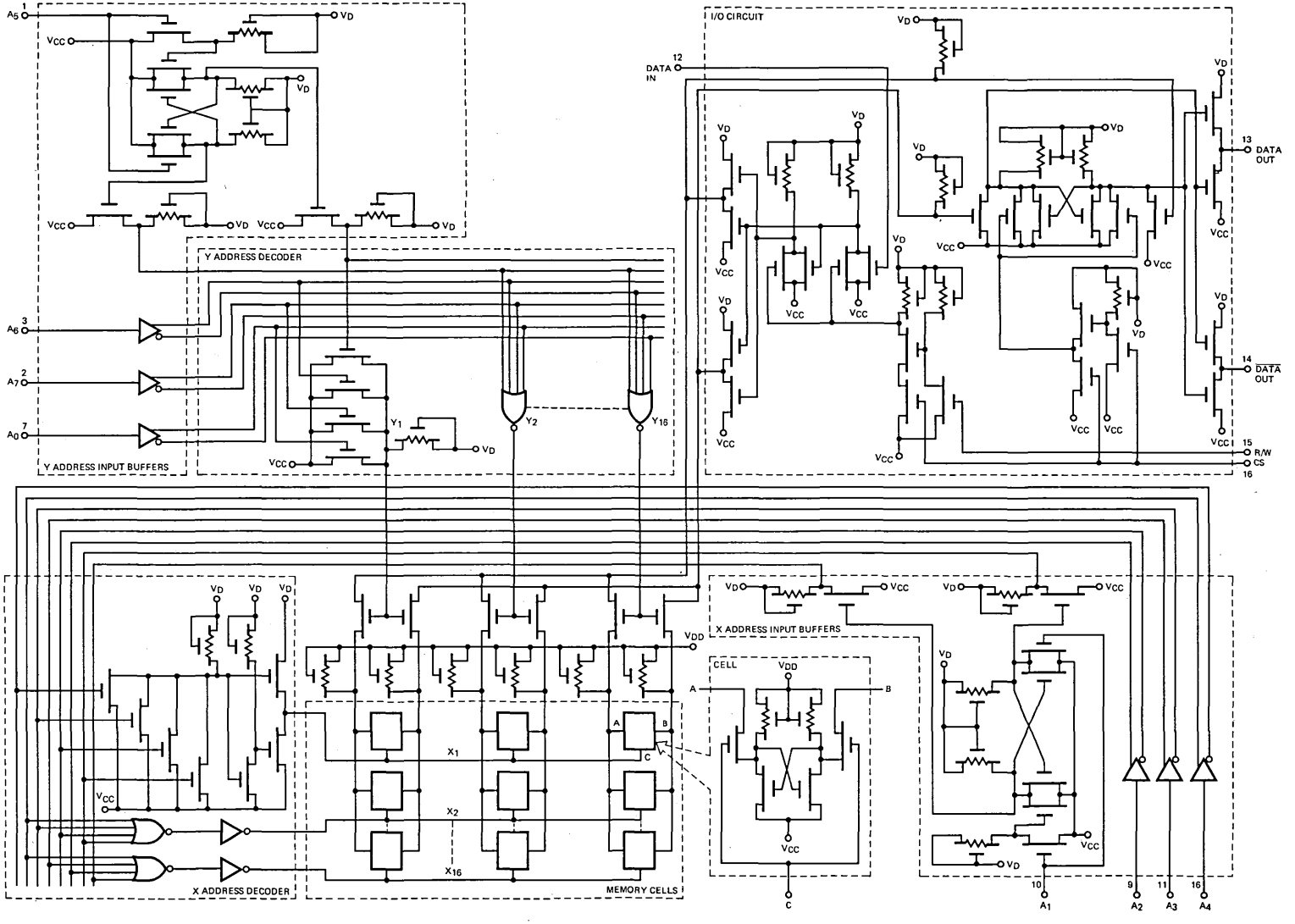
Access Time Versus Ambient Temperature



Access Time Versus Supply Voltage

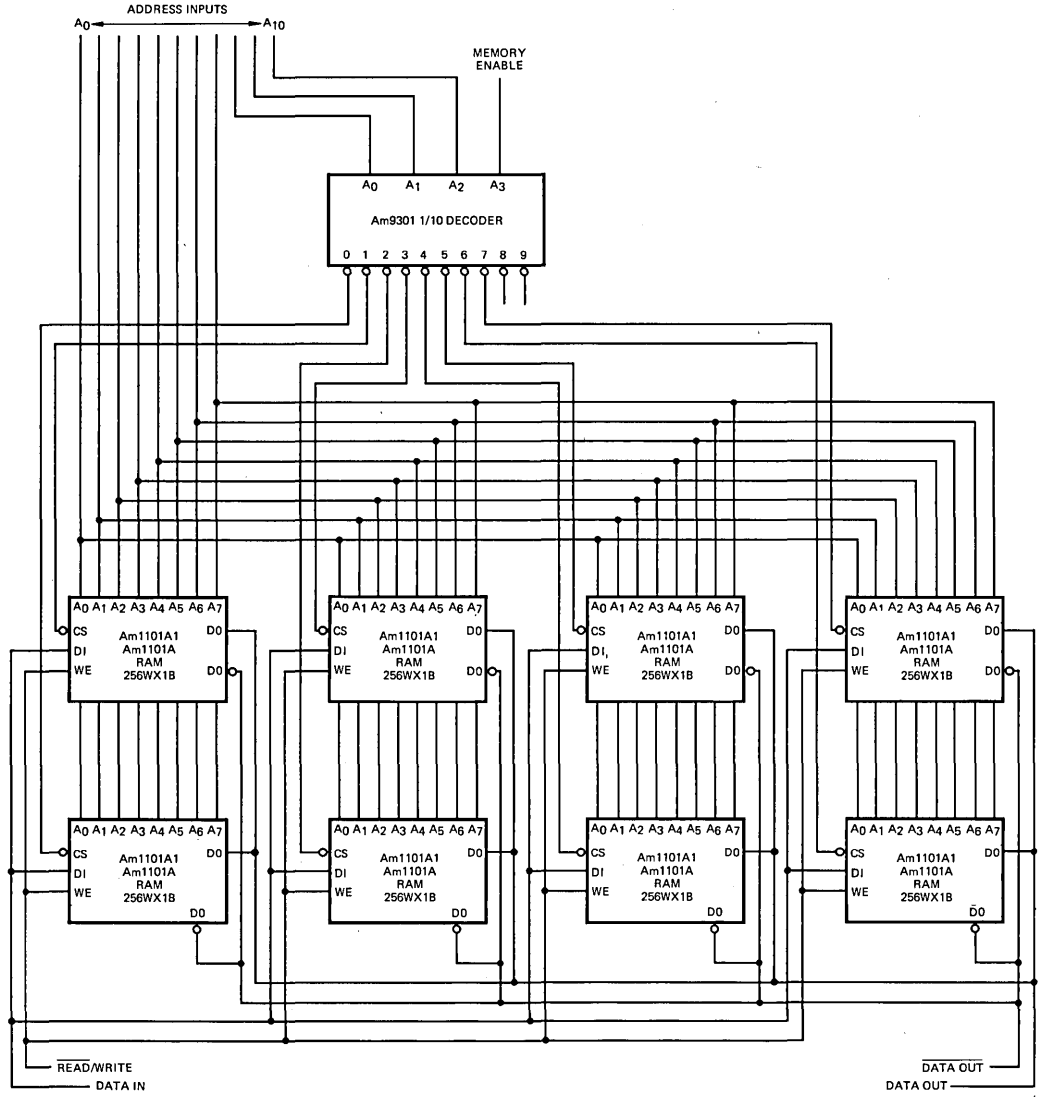


CIRCUIT DIAGRAM

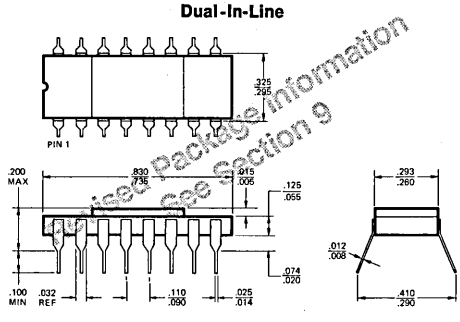


APPLICATION

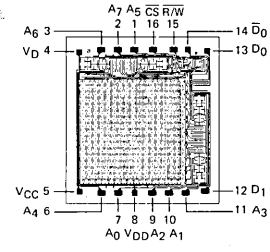
2048 Word x 1 Bit Memory



PHYSICAL DIMENSIONS
Dual-In-Line



Metallization and Pad Layout



112 x 124 Mils

ADVANCED MICRO DEVICES INC.
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TWX: 910-339-9280
TELEX: 34-6306

Am14/1506 Am14/1507
Dual 100-Bit Shift Registers

Distinctive Characteristics

- Dual 100-bit high-speed silicon gate MOS shift registers
- DTL and TTL compatible
- Low power dissipation of 0.4 mW/bit at 1 MHz
- 2 MHz frequency operation guaranteed
- 100% reliability assurance testing in compliance with MIL STD 883
- Electrically tested and optically inspected die for the assemblers of hybrid products
- Mixing privileges for obtaining price discounts. Refer to price list

FUNCTIONAL DESCRIPTION

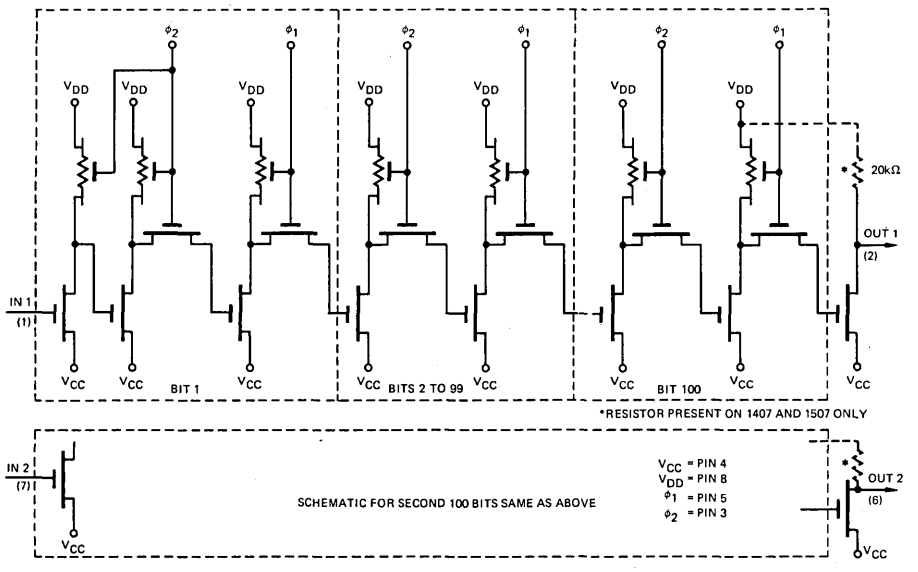
The Advanced Micro Devices dual 100-bit dynamic MOS shift registers are built using enhancement mode P-channel silicon gate MOS devices. The circuits use low-voltage circuitry for low-power dissipation and ease of interfacing into bipolar DTL and TTL circuits.

The shift registers can be driven by either DTL or TTL circuits or by MOS circuits and provide driving capability to MOS or bipolar circuits.

Silicon gate technology gives high-speed operation, low-power dissipation and low-clock input capacitance

The shift registers are ideal for low-cost buffer memories, long serial digital delay lines, etc. The devices are available in the commercial (0°C to +70°C) temperature range and the military (−55°C to +125°C) temperature range and are available with open drain output (Am14/1506), or with a 20kΩ pull-down resistor (Am14/1507) for easier interface to other circuitry.

CIRCUIT DIAGRAM

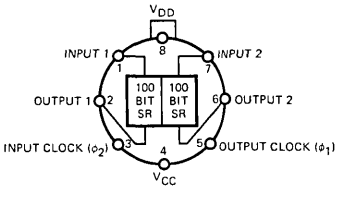


ORDERING INFORMATION

Part Number	Package Type	Ambient Temperature Range	Order Number
Am1406	TO-99	−55°C to +125°C	1406T
Am1506	TO-99	0°C to +70°C	1506T
Am14/1506	Dice	Note	1406D
Am1407	TO-99	−55°C to +125°C	1407T
Am1507	TO-99	0°C to +70°C	1507T
Am14/1507	Dice	Note	1407D

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +160°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Power Dissipation (Note 1)	500 mW
Data and Clock Input Voltages with respect to most Positive Supply Voltage, V_{CC}	+0.5 V to −25 V
Power Supply Voltage, V_{DD} with respect to V_{CC}	+0.5 V to −25 V

ELECTRICAL CHARACTERISTICS

Am1506/1507 T_A = 0°C to +70°C
Am1406/1407 T_A = −55°C to +125°C
} unless otherwise specified

DC Characteristics Over Operating Temperature Range (V_{DD} = −5.0 V ±5%, V_{CC} = +5.0 V ±5% unless otherwise specified)

Parameters	Test Conditions		Limits Over Specified Temperature Range Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Note 2) Output HIGH Voltage	I_{OH} = −2.5 mA Load = 20 kΩ		2.5	4.0		Volts
V_{OL} (Note 2) Output LOW Voltage	I_{OL} = 200 μA 1407, 1507 only			−1.2	0.4	Volts
V_{IH} Input HIGH Voltage	V_{DD} = −5.0 V V_{CC} = +5.0 V		2.5	5.0	5.3	Volts
V_{IL} Input LOW Voltage	V_{DD} = −5.0 V V_{CC} = +5.0 V		−10	0.2	0.8	Volts
V_{IHC} Clock Input HIGH Voltage	V_{DD} = −5.0 V V_{CC} = +5.0 V		3.5		5.3	Volts
V_{ILC} Clock Input LOW Voltage	V_{DD} = −5.0 V V_{CC} = +5.0 V		−13		−9.5	Volts
I_L Input Load Current	Input Pin 1 Pins 2, 3, 4, 5, 6, 7 = 0 V Pin 1 = −18 V Pin 8 = −8 V	T_A = 25°C			500	nA
	Input Pin 7 Pins 1, 2, 3, 4, 5, 6 = 0 V Pin 7 = −18 V Pin 8 = −8 V	T_A = 25°C				
I_{LC} Clock Input Current	Clock Input Pins 3, 5 = −18 V All Other Pins = 0 V	T_A = 25°C			500	nA
I_{LO} (Note 3) Output Leakage Current	Output Pin 2 Pins 1, 4, 6, 7, 8 = 0 V Pin 2 = −18 V Pins 3, 5 = −8 V				500	nA
	Output Pin 6 Pins 1, 2, 4, 7, 8 = 0 V Pin 6 = −18 V Pins 3, 5 = −8 V					
I_{DD} (See Graphs) Power Supply Current (Note 4)	f = 1MHz Duty Cycle = 60%	T_A = 25°C		4.0	8.0	mA
		T_A = 0°C		5.0	10	
		T_A = −55°C		8.0	13	
Z_{out} Output ON Impedance	V_{DD} = −5.0 V V_{CC} = +5.0 V I_{OH} = −2.5 mA			300	750	Ω
* C_{IN} Input Capacitance	Input Pins 1, 7 V_{IN} = V_{CC}				4	pF
* C_ϕ Clock Input Capacitance	Clock Input Pins 3, 5 V_ϕ = V_{CC}				40	pF
	Clock Input Pins 3, 5 V_ϕ = −20 V Bias				35	
* C_{out} (Note 4) Output Capacitance	Output Pins 2, 6 V_{out} = V_{CC}				5	pF

Note 1: Typical values are at V_{CC} - V_{DD} = 10 V and T_A = 25°C.

Note 2: In the logic HIGH level the MOS register output can supply 2.5 mA into the load combination of the internal pull-down resistor and the external load. In the logic LOW level, I_{OL} represents the current the internal 20 kΩ resistor will sink. In order to insure current sinking capability for one standard TTL load, an external pull-down resistor must be added. See applications.

Note 3: Leakage current for 1406 and 1506 only. For 1407 and 1507 the output on pins 2 and 6 will exhibit a resistance when measured with the following bias conditions: pins 1, 6, and 8 at GND; pins 3 and 5 at −16 V; pin 4 open; measure pins 2 and 6. 25 kΩ ≥ R_{OUT} ≥ 15 kΩ.

Note 4: Power dissipation is directly proportional to clock duty cycle. Duty cycle is defined as: clock frequency ($t\phi_1 pw + t\phi_2 pw + \frac{1}{2}$ [$t_r + t_f$]).

 *This paramenter is periodically sampled and is not 100% tested.

SWITCHING CHARACTERISTICS ($V_{DD} = -5\ V \pm 5\%$; $V_{CC} = +5\ V \pm 5\%$ unless otherwise specified)

Parameter	Description	Test Conditions	Limits Over Specified Temperature Range Min.	Max.	Units
f_c	Clock Frequency	$V_{IH} \geq 3.0\ V$	(Note 5)	2	MHz
		$V_{IH} \geq 2.5\ V$		1	
$t_{\phi PW}$	Clock Pulse Width	$V_{IH} \geq 3.0\ V$	130		ns
		$V_{IH} \geq 2.5\ V$	200		
$t_{\phi d}$	Clock Pulse Delay	$\phi_{1\ PW} = 0.4\ \mu s$ $\phi_{2\ PW} = 0.2\ \mu s$ $f_c = 1$ MHz	100		ns
t_f, t_r	Clock Pulse Rise/Fall Time	$f_c = 1$ MHz		50	ns
t_s	Input Data Set Up Time	$f_c = 2$ MHz	100		ns
		$f_c = 1$ MHz	200		
t_h	Input Data Hold Time		100		ns
t_{pd}	Propagation Delay ϕ_1 to Output	$V_{ILC} - V_{CC} = -16\ V$		100	ns

Note 5: See "Minimum Operating Frequency" graph for low limits on clock rate.

DESCRIPTION OF TERMS

OPERATIONAL TERMS

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

V_{IH} Logic HIGH input voltage.

V_{IL} Logic LOW input voltage.

V_{ILC} Clock LOW input voltage.

V_{IHC} Clock HIGH input voltage.

I_L Input load current.

I_{LO} Output leakage current.

I_{DD} Power supply current.

Z_{out} Output impedance with output sourcing 2.5 mA.

C_{IN} Input capacitance.

C_ϕ Input clock capacitance.

C_{OUT} Output capacitance.

FUNCTIONAL TERMS

ϕ_1, ϕ_2 The two clock phases required by the dynamic shift register.

f_c The clock frequency of the shift register.

SWITCHING TERMS

$t_{\phi d}$ The delay between the LOW to HIGH transition of a clock phase to the HIGH to LOW transition of the other clock phase.

$t_{\phi PW}$ The clock pulse widths necessary for correct operation.

t_f, t_r The clock pulse rise and fall times necessary for correct operation.

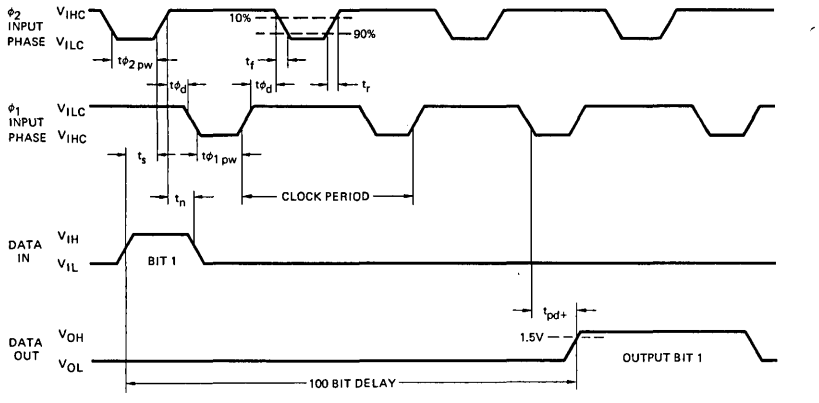
t_s The time required for the input data to be present prior to the LOW to HIGH transition of the clock phase ϕ_2 to ensure correct operation.

t_h The time required for the input data to remain present after the LOW to HIGH transition of the clock phase ϕ_2 to ensure correct operation.

t_{pd+} The propagation delay from the HIGH to LOW clock phase ϕ_1 transition to the output LOW to HIGH transition.

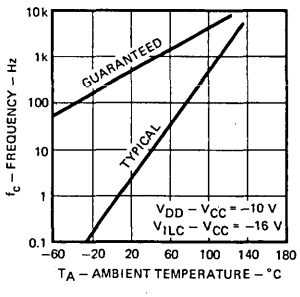
SWITCHING WAVEFORMS

Clock Rise Time 10 ns
Clock Fall Time 10 ns
Data Amplitude +0.8V to +2.5V
Output Load 1 TTL Unit Load

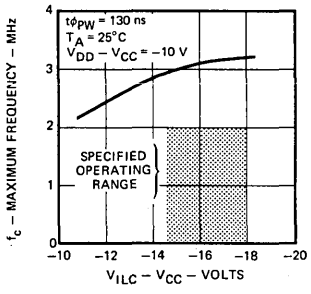


SWITCHING CHARACTERISTICS

Minimum Operating Frequency Versus Temperature

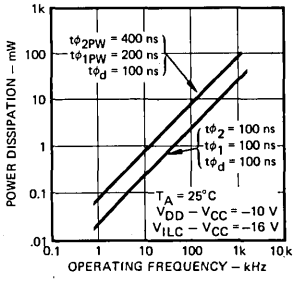


Maximum Frequency Versus Clock Amplitude

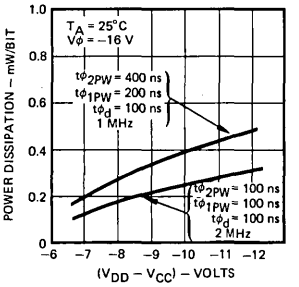


SWITCHING CHARACTERISTICS

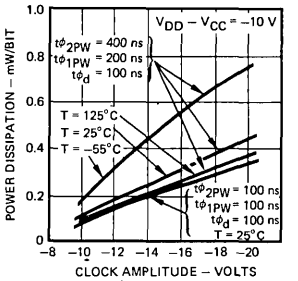
Power Dissipation Versus Frequency



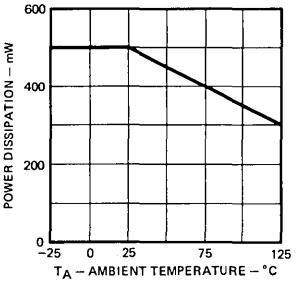
Power Dissipation/Bit Versus Supply Voltage



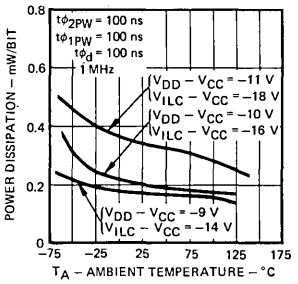
Power Dissipation/Bit Versus Clock Amplitude



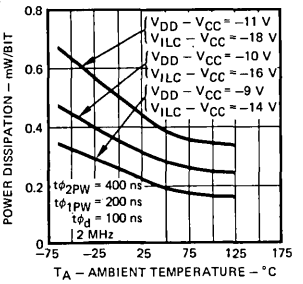
Maximum Package Power Dissipation Versus Temperature



Power Dissipation/Bit at 2 MHz Versus Temperature



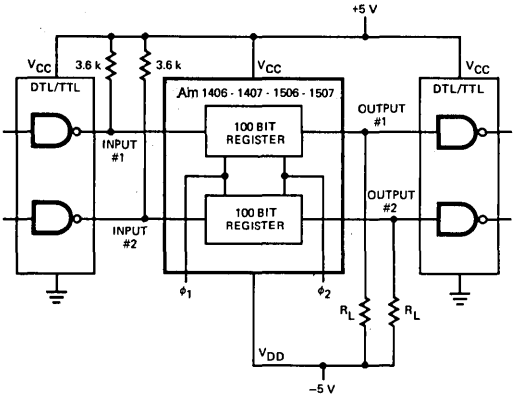
Power Dissipation/Bit at 1 MHz Versus Temperature



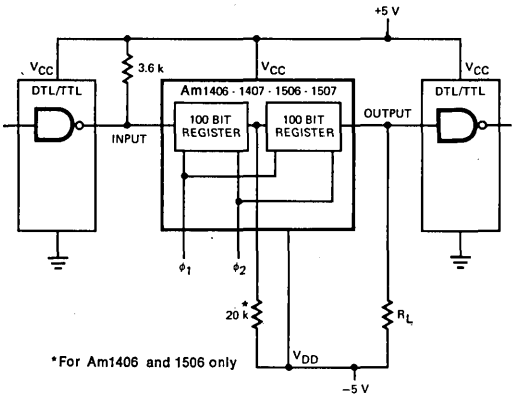
APPLICATIONS

DTL/TTL/MOS Interfaces

100-Bit Delay



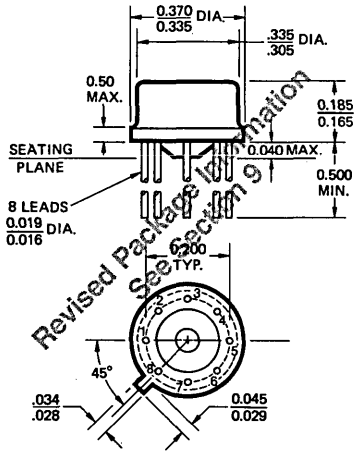
200-Bit Delay



Maximum Value of R_L ($V_{DD} = -5.0 \pm 5\%$)

Gate Type	1406, 1506	1407, 1507
Standard TTL	3.2k	3.8k
93L Low Power	12.8k	35k
74L Low Power	28k	none required

PHYSICAL DIMENSIONS
(In Accordance with JEDEC TO-99)

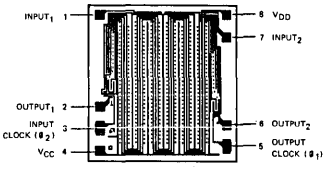


Revised Package Information
See Section 9

NOTES: (1) All dimensions in inches.
(2) Leads are gold-plated Kovar.

Metallization and Pad Layout

69 x 74 Mils



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Am2533/2833

1024-Bit Static Shift Registers

Distinctive Characteristics

- Second source to Signetics 2533
- All inputs are low-level DTL/TTL compatible
- Static operation with single clock input.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- DC to 2.0MHz operation with Am2833

FUNCTIONAL DESCRIPTION

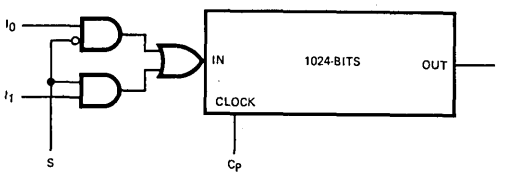
The Am2533/2833 is a quasi-static 1024-bit MOS shift register using low-threshold P-channel silicon gate technology.

The device has a single TTL/DTL compatible clock input, Cp. Data in the register is stored in static, cross-coupled latches while the clock is LOW, so that the clock may be stopped indefinitely in the LOW state. When the clock shifts from LOW to HIGH to LOW a dynamic transfer of data occurs from one static latch to the next. The input of the register is a two-input multiplexer with both data inputs available. A select line, S, determines whether data will be accepted from the I_0 input (S = LOW) or the I_1 input (S = HIGH). The register can be placed in the recirculate mode by tying the output, O, to one of the data inputs, and using the select line as a write/recirculate control. The Am2833 is functionally identical to the Am2533 but has superior performance over an extended temperature range.

LOGIC SYMBOL

V_{CC} = Pin 8
V_{GG} = Pin 2
V_{DD} = Pin 4

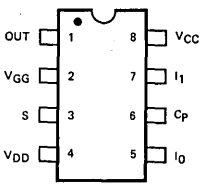
LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Am2533 Order Number	Am2833 Order Number
Molded DIP	0°C to +70°C	AM2533V	AM2833PC
Hermetic DIP	0°C to +70°C	AM2533DC	AM2833DC
Hermetic DIP	−55°C to +125°C		AM2833DM

CONNECTION DIAGRAM
Top View



Note: Pin 1 marked for orientation

MAXIMUM RATING (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{DD} Supply Voltage	V_{SS} −20V to V_{SS} +0.3V
V_{GG} Supply Voltage	V_{SS} −20V to V_{SS} +0.3V
DC Input Voltage	V_{SS} −20V to V_{SS} +0.3V

OPERATING RANGE

Part No.	Temperature	V_{CC}	V_{GG}
Am2533PC/Am2833PC Am2533DC/Am2833DC	0°C to 70°C	5.0V ±5%	−12.0V ±5%
Am2833DM	−55°C to +125°C	5.0V ±5%	−12.0V ±5%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −100µA		2.4	3.5		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 1.6mA			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	Am2533	V_{CC}−1.8		V_{CC}+0.3	Volts
			Am2833 (Note 3)	2.0		V_{CC}+0.3	
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		V_{GG}		0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0V, T_A = 25°C			10	500	nA
I_{IH}	Input HIGH Current	T_A = 25°C, V_{IN} = V_{CC} −1.0 (Note 3)		−150	−300	−500	µA
I_{IT}	Peak input transition current (Note 3)	2.5 ≤ V −V_{IN} ≤ 4.0, T_A = 25°C				−1.6	mA
V_{Imax}	Voltage at maximum input current	T_A = 25°C		V_{SS}−4.0	V_{SS}−3.0	V_{SS}−2.5	V
I_{CC}	V_{CC} Power Supply Current	f = 1.5MHz	Am2533		16	30	mA
		f = 2.0MHz	Am2833PC, DC		16	35	
			Am2833DM		20	42	
I_{GG}	V_{GG} Power Supply Current	f = 1.5MHz	Am2533		−5.0	−7.5	mA
		f = 2.0MHz	Am2833PC, DC		−5.0	−14	
			Am2833DM		−7.0	−18	

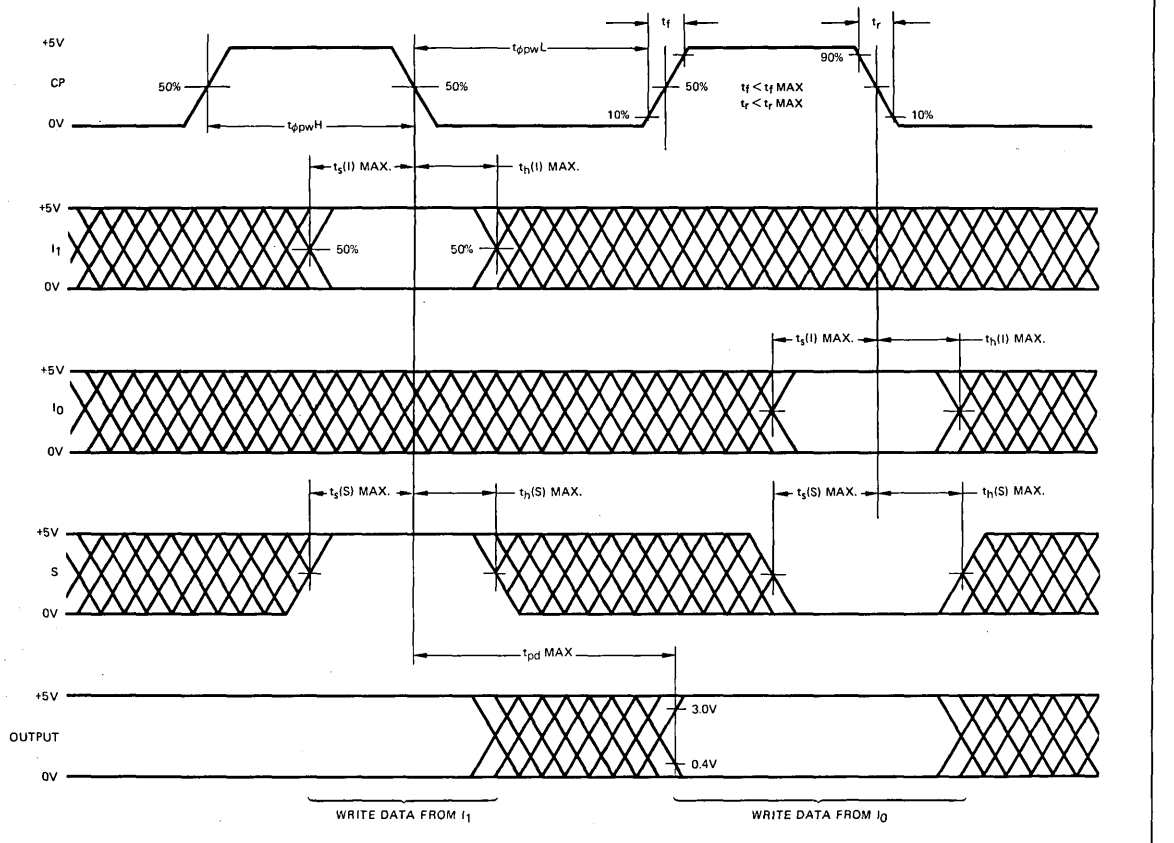
Notes: 1. Typical limits are at V_{CC} = 5.0V, V_{GG} = −12V, 25°C ambient.
2. Power supply currents are with inputs and outputs open.
3. A special input pull-up circuit becomes active at V_{IN} = V_{SS} −3.5V to pull the internal input node up to the MOS threshold. To return the internal node to the LOW state, current must be drawn from the MOS input. This current is maximum at approximately 2.0V.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions	Am2533 Min.	Am2533 Typ. (Note 1)	Am2533 Max.	Am2833 Min.	Am2833 Typ. (Note 1)	Am2833 Max.	Units
f_{max}	Maximum Clock Frequency		1.5	2.0		2.0	3.0		MHz
$t_{\phi pw}L$	Clock LOW Time		0.250		∞	0.200		∞	µs
$t_{\phi pw}H$	Clock HIGH Time		0.350		100	0.250		100	µs
t_r, t_f	Clock Rise and Fall Times				1			1	µs
t_s(I)	Set-up Time, I_0 or I_1 Input (see definitions)	t_r = t_f ≤ 25ns			50			50	ns
t_h(I)	Hold Time, I_0 or I_1 Input (see definitions)				50			50	ns
t_s(S)	Set-up Time, S Input (see definitions)				80			80	ns
t_h(S)	Hold Time, S Input (see definitions)				50			50	ns
t_{pd}	Delay, Clock to Output LOW or HIGH	R_L = 2.9k, C_L = 20pF			300			300	ns
t_{pr}, t_{pf}	Output Rise and Fall Times	10% to 90%			150			150	ns
C_{in}	Capacitance, Any Input (Note 2)	f = 1MHz, V_{IN} = V_{CC}		3	5		3	5	pF

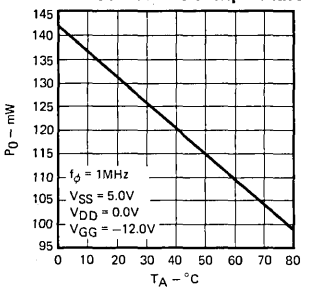
Notes: 1. Typical limits are at V_{CC} = 5.0V, V_{GG} = −12.0V and T_A = 25°C
2. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.

TIMING DIAGRAM

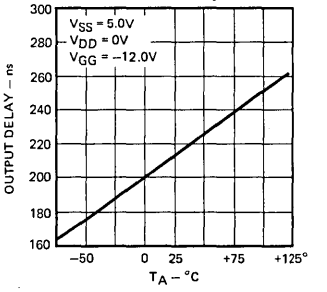


TYPICAL PERFORMANCE CURVES

Power Dissipation Versus Ambient Temperature



t_{pd} as a Function of Ambient Temperature

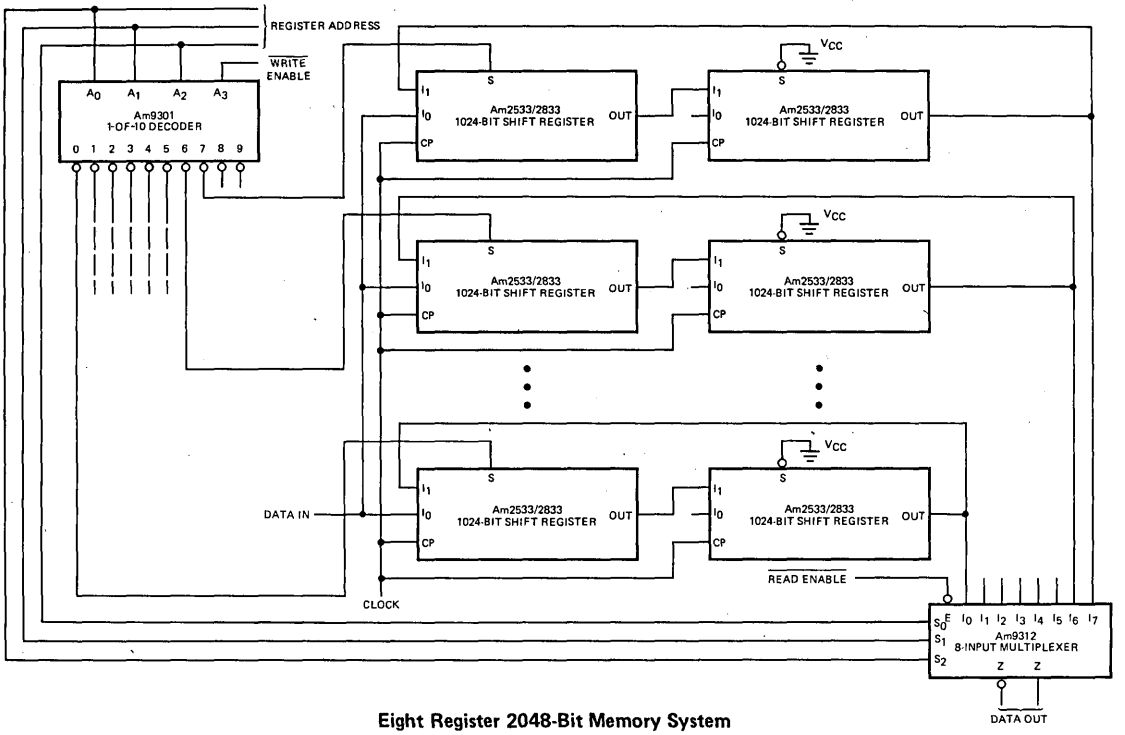


DEFINITION OF TERMS

STATIC SHIFT REGISTER A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is HIGH and is transferred to the static slaves while the clock is LOW. The clock may be stopped indefinitely in the LOW state, but there are limitations on the time it may reside in the HIGH state.

SET-UP and HOLD TIMES The shift register will accept the data that is present on its input around the time the clock goes from HIGH-to-LOW. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

APPLICATIONS

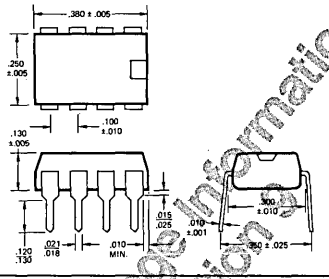


Eight Register 2048-Bit Memory System

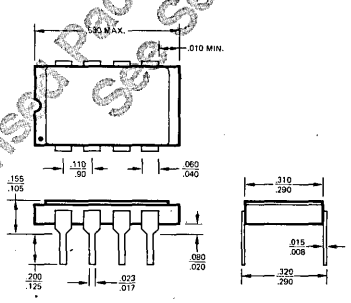
Data enters one of the eight 2048-bit registers when the write enable input to the decoder is LOW. The addressed register will accept the data on the data input; the other seven registers will recirculate their data. Outputs are driven directly into an Am9312 8-input multiplexer. Obviously, the read and write registers need not be the same.

PHYSICAL DIMENSIONS

Molded 8-Pin DIP



Hermetic 8-Pin DIP

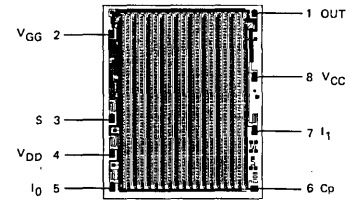


TRUTH TABLE

S	I_0	I_1	Data Entered
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

H = HIGH Voltage level
L = LOW Voltage Level
X = Don't Care

Metallization and Pad Layout



DIE SIZE: 0.133" X 0.163"

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Am2102/Am2102-1/Am2102-2

1024-Bit Static N-Channel RAM

Distinctive Characteristics

- Operates from single 5V power supply
- Three speed selections: 1μsec, 650ns, 500ns
- All inputs and outputs directly TTL compatible
- No clocks required
- 100% reliability testing in accordance with MIL-STD-883

FUNCTIONAL DESCRIPTION

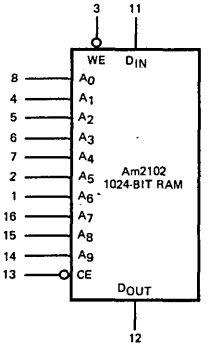
The Am2102 is a static N-channel 1024-bit random access memory. The device operates from a single +5 volt power supply and all inputs and outputs are directly TTL compatible with no external components required. The memory is addressed for reading or writing one bit by applying a binary code to the 10 address inputs A_0–A_9. Writing is accomplished by lowering the write enable ($\overline{WE}$) and the chip select ($\overline{CE}$); the data on the data input (D_{in}) will be stored in the addressed location. If the chip select is lowered while write enable is HIGH, then the data stored in the addressed location will be read out on the data output (D_{out}).

Any time the chip select is HIGH, the entire chip is disabled. Data cannot be written into the memory and the output will go to a high impedance OFF state. When chip select is LOW, the output will drive at least one TTL load in both the HIGH and LOW states. During the write operation, the data output follows the data input.

The chip select function and the three-state output make the construction of a large array using Am2102 chips very easy. Am2102 inputs and outputs can be tied together and chips selected by a standard TTL decoder such as the Am9321 or Am9301.

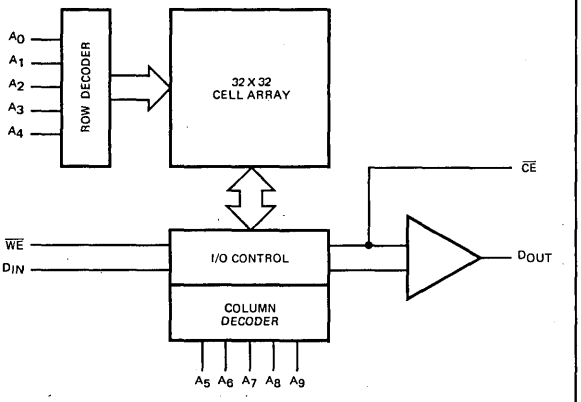
The Am2102 is available in three different cycle time selections. The Am2102 operates with a 1μsec minimum read or write cycle, the Am2102-1 requires a 500ns minimum read or write cycle, and the Am2102-2 requires a 650ns minimum read or write cycle.

LOGIC SYMBOL



V_{CC} = Pin 10
GND = Pin 9

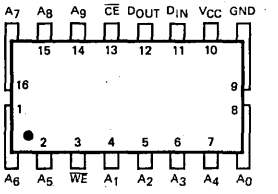
BLOCK DIAGRAM



Am2102 ORDERING INFORMATION

Package Type	Ambient Temperature Range	1μsec Order Number	500ns Order Number	650ns Order Number
Molded DIP	0°C to +70°C	P2102	P2102-1	P2102-2
Hermetic DIP	0°C to +70°C	C2102	C2102-1	C2102-2

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	0°C to +70°C
Supply Voltage to Ground Potential (Pin 10 to Pin 9) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs	−0.5V to +7V
DC Input Voltage	−0.5V to +7V

OPERATING RANGE

Part Number	V_{CC}	Ambient Temperature
Am2102, Am2102-1, Am2102-2	5.0V ±5%	0°C to +70°C

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min.	Typ.(Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −100μA		2.2			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 1.9mA				0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.2		V_{CC}	Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		−0.5		0.65	Volts
I_{LI}	Input Load Current	V_{CC} = MAX., V_{IN} = 0V to 5.25 V				10	μA
I_{CC1}	Power Supply Current	All inputs = V_{CC} Data out open V_{CC} = MAX.	T_A = 25°C		30	60	mA
I_{CC2}			T_A = 0°C to +70°C		30	70	
I_{LO}	Output Leakage Current	$V_{\overline{CE}}$ = 2.2V	V_{OUT} = 4.0V			10	μA
			V_{OUT} = 0.45V			−100	

Note 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C

CAPACITANCE (T_A = 25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance, Any Input	V_{IN} = 0V, f = 1MHz		3	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, f = 1MHz		7	10	pF

Am2102 SWITCHING CHARACTERISTICS AND OPERATING REQUIREMENTS (T_A = 0°C to 70°C, V_{CC} = 5V±5%)

Load = 1 TTL Gate and 100 pF, V_{IL} = 0.65V, V_{IH} = 2.2V, t_r = t_f = 20ns

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
t_{RC}	Read Cycle Time		1000			ns
t_A	Access Time			500	1000	ns
t_{CO}	$\overline{CE}$ LOW to Output				500	ns
t_{OH1}	Previous Read Data Valid with Respect to Address		50			ns
t_{OH2}	Previous Read Data Valid with Respect.to Chip Select		0			ns
t_{WC}	Write Cycle Time		1000			ns
t_{AW}	Address Set-Up Time		200			ns
t_{WP}	Write Pulse Width		750			ns
t_{WR}	Write Recovery Time		50			ns
t_{DW}	Data Set-Up Time		800			ns
t_{DH}	Data Hold Time		100			ns
t_{CW}	Chip Enable Hold Time		900			ns

Am2102-1 SWITCHING CHARACTERISTICS AND OPERATING REQUIREMENTS ($T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$)

Load = 1 TTL Gate and 100 pF, $V_{IL} = 0.65V$, $V_{IH} = 2.2V$, $t_r = t_f = 20ns$

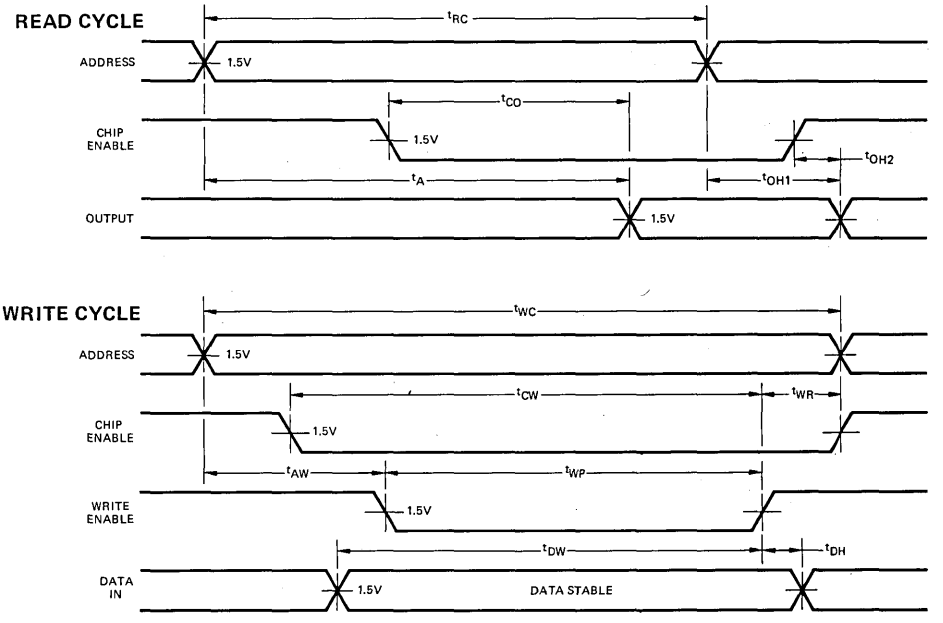
Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
t_{RC}	Read Cycle Time		500			ns
t_A	Access Time				500	ns
t_{CO}	$\overline{CE}$ LOW to Output				350	ns
t_{OH1}	Previous Read Data Valid with Respect to Address		50			ns
t_{OH2}	Previous Read Data Valid with Respect to Chip Select		0			ns
t_{WC}	Write Cycle Time		500			ns
t_{AW}	Address Set-Up Time		150			ns
t_{WP}	Write Pulse Width		300			ns
t_{WR}	Write Recovery Time		50			ns
t_{DW}	Data Set-Up Time		330			ns
t_{DH}	Data Hold Time		100			ns
t_{CW}	Chip Enable Hold Time		400			ns

Am2102-2 SWITCHING CHARACTERISTICS AND OPERATING REQUIREMENTS ($T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$)

Load = 1 TTL Gate and 100 pF, $V_{IL} = 0.65V$, $V_{IH} = 2.2V$, $t_r = t_f = 20ns$

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
t_{RC}	Read Cycle Time		650			ns
t_A	Access Time				650	ns
t_{CO}	$\overline{CE}$ LOW to Output				400	ns
t_{OH1}	Previous Read Data Valid with Respect to Address		50			ns
t_{OH2}	Previous Read Data Valid with Respect to Chip Select		0			ns
t_{WC}	Write Cycle Time		650			ns
t_{AW}	Address Set-Up Time		200			ns
t_{WP}	Write Pulse Width		400			ns
t_{WR}	Write Recovery Time		50			ns
t_{DW}	Data Set-Up Time		450			ns
t_{DH}	Data Hold Time		100			ns
t_{CW}	Chip Enable Hold Time		550			ns

SWITCHING WAVEFORMS



DEFINITION OF TERMS

FUNCTIONAL TERMS

$\overline{CE}$ Active LOW chip enable. Data can be read from or written into the memory only if $\overline{CE}$ is LOW.

$\overline{WE}$ Active LOW write enable. Data is written into the memory if $\overline{WE}$ is LOW and read from the memory if $\overline{WE}$ is HIGH.

Static RAM A random access memory in which data is stored in bistable latch circuits. A static memory will store data as long as power is supplied to the chip without requiring any special clocking or refreshing operations.

N-Channel An insulated gate field effect transistor technology in which the transistor source and drains are made of N-type material, and electrons serve as the carriers between the two regions. N-Channel transistors exhibit lower thresholds and faster switching speeds than P-Channel transistors.

SWITCHING TERMS

t_{RC} Read Cycle Time. The minimum time required between successive address changes while reading.

t_A Access Time. The time delay between application of an address and stable data on the output when the chip is enabled.

t_{CO} Access Time from Chip Enable. The minimum time during which the chip enable must be LOW prior to reading data on the output.

t_{OH1} Minimum Access Time. Minimum time which will elapse between change of address and any change on the data output.

t_{OH2} Minimum time which will elapse between a change on the chip enable and any change on the data output.

t_{WC} Write Cycle Time. The minimum time required between successive address changes while writing.

t_{AW} Address Set-Up Time. The minimum time prior to the falling edge of the write enable during which the address inputs must be correct and stable.

t_{WP} The minimum duration of a LOW level on the write enable guaranteed to write data.

t_{WR} Address Hold Time. The minimum time after the rising edge of the write enable during which the address must remain steady.

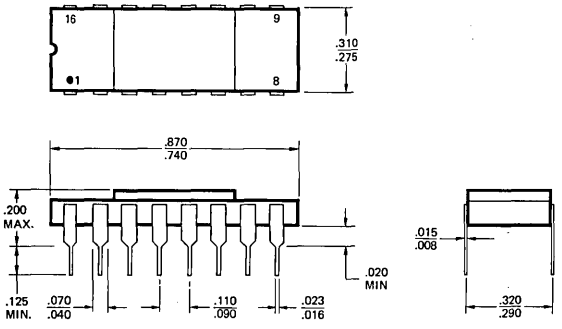
t_{DW} Data Set-Up Time. The minimum time that the data input must be steady prior to the rising edge of the write enable.

t_{DH} Data Hold Time. The minimum time that the data input must remain steady after the rising edge of the write enable.

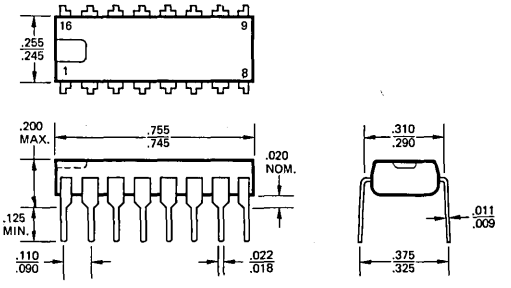
t_{CW} Chip Enable Time During Write. The minimum duration of a LOW level on the Chip Select while the write enable is LOW to guarantee writing.

PHYSICAL DIMENSIONS
Dual-In-Line

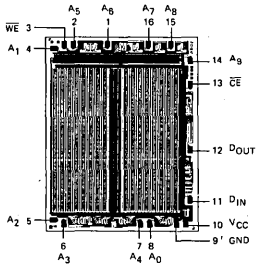
16-Pin Side Brazed



16-Pin Molded



Metallization and Pad Layout



DIE SIZE 0.126" X 0.164"

ADVANCED MICRO DEVICES INC.
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TWX: 910-339-9280
TELEX: 34-6306

Am2805/2806/2807/2808

512- and 1024-Bit Dynamic Shift Registers

Distinctive Characteristics

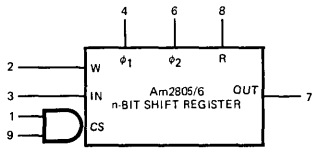
- Am2805 Plug-in Replacement Intel 1405A and Signetics 2505
  Am2806 Plug-in Replacement Signetics 2512
  Am2807 Plug-in Replacement Signetics 2524
  Am2808 Plug-in Replacement Signetics 2525
- On chip recirculate and chip select controls
- 100% reliability assurance testing in compliance with MIL-STD-883
- TTL and DTL compatible
- Full military temperature range devices available

FUNCTIONAL DESCRIPTION

The Am2805 and Am2807 are 512-bit dynamic shift registers with recirculate logic on chip. The Am2806 and Am2808 are 1024-bit dynamic shift registers which also have built-in recirculate logic. When the write input is HIGH, data on the data input enters the first bit of the register during the ϕ_2 clock time. If the write input is LOW, then the output of the register is written into the first bit instead. Data in the last bit of the register appears on the data output during the ϕ_1 clock time if the read line is HIGH. If the read line is LOW, the output is OFF (high impedance state). The outputs of all four devices are open drains; they pull the output to V_{CC} when ON and exhibit a very high impedance when OFF. An external pull-down resistor to ground or V_{DD} must be used to establish the LOW logic level.

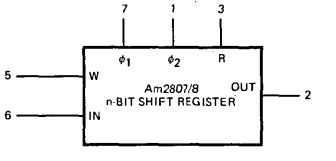
The Am2805 and Am2806 also have two chip select inputs, CS_1 and CS_2. If either of these inputs is LOW, the register recirculates and the output remains OFF, regardless of the state of the read and write lines. All inputs except the clocks are TTL/DTL compatible. A TTL input may be driven by the output if a 3k pull-down resistor to V_{DD} is used. The register outputs can be wire-ORed for expansion. The devices are guaranteed to operate at speeds up to 3MHz.

LOGIC SYMBOLS



Am2805 n = 512
Am2806 n = 1024

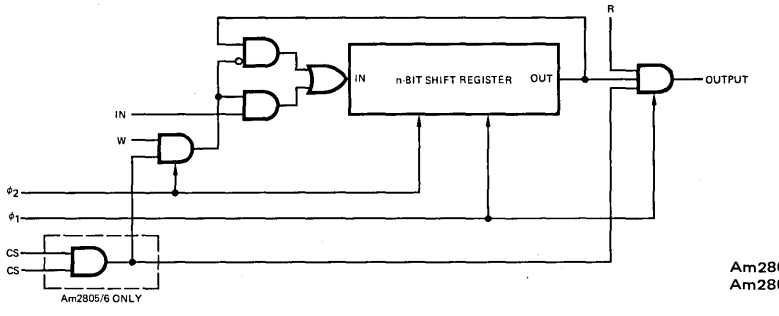
V_{CC} = Pin 5
V_{DD} = Pin 10



Am2807 n = 512
Am2808 n = 1024

V_{CC} = Pin 8
V_{DD} = Pin 4

LOGIC DIAGRAM



Am2805/7 n = 512
Am2806/8 n = 1024

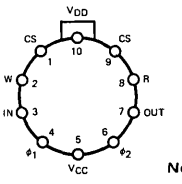
ORDERING INFORMATION

Package Type	Temperature Range	512-Bit Order Number	1024-Bit Order Number
10-Pin TO-100	0°C to +70°C	AM2805HC or 1405A	AM2806HC
10-Pin TO-100	−55°C to +125°C	AM2805HM	AM2806HM
Dice	Note	AM2805XX	AM2806XX
8-Pin Molded DIP	0°C to +70°C	AM2807PC	AM2808PC
Dice	Note	AM2807XX	AM2808XX

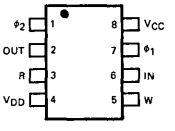
Note: The dice supplied will contain units which meet both 0°C to +70°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAMS
Top View

Am2805/6



Am2807/8



Note: PIN 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
DC Input Voltage with Respect to V_{CC}	−20V to +0.3V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

V_{DD} = −5V ±5%, V_{CC} = 5.0V ±5%
Am280XXM T_A = −55°C to +125°C
Am280XXC T_A = 0°C to +70°C

Parameters	Description	Test Conditions		Min.	Typ.(Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage (Notes 2 & 3)	V_{CC} = MIN.	I_{OH} = 1.6mA, (R_L = 5.6kΩ)	3.6	4.0		Volts
			I_{OH} = 2.6mA, (R_L = 3kΩ)	2.4	3.5		
I_{OL}	Output Leakage Current	V_0 = −5.5V, $V_{\phi1}$ = $V_{\phi2}$ = −12V			10	1000	nA
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs except clocks		V_{CC} −2.0		V_{CC} +0.3	Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs except clocks		V_{CC} −10		V_{CC} −4.2	Volts
I_I	Input Leakage Current	V_{IN} = −5.5V, T_A = 25°C			10	500	nA
I_ϕ	Clock Input Leakage Current	V_ϕ = −12V, T_A = 25°C			10	1000	nA
$V_{\phi H}$	Clock HIGH Level			V_{CC} −1.0		V_{CC} +0.3	V
$V_{\phi L}$	Clock LOW Level			V_{CC} −17		V_{CC} −14.5	V
I_{DD}	Power Supply Current (Note 4)	f = 1 MHz, T_A = 25°C Output Open V_{DD} = −5.5 V, $t_{\phi L}$ = 150ns	Am2805/7		7	12	mA
			Am2806/8		10	20	

Notes: 1. Typical Limits are at V_{CC} = 5.0 V, V_{DD} = −5.0 V, 25° C Ambient and maximum loading.
2. Variations in V_{CC} will be tracked directly by V_{OH} and input thresholds.
3. The output is open drain and the logic LOW level must be defined by an external pull-down resistor. A 3k resistor to V_{DD} provides TTL compatibility.
4. The power supply current flows only while one clock is LOW. Average power is therefore directly proportional to clock duty cycle (ratio of clock LOW time to total clock period.) See curves next page.

SWITCHING CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = +5.0 V ±5%, V_{DD} = −5.0 V ±5%, $V_{\phi L}$ = −11 V)

Parameters	Definition	Test Conditions		Min.	Typ.(Note 1)	Max.	Units
f_{max}	Clock and Data Rate Range	0°C to +70°C		0		4	MHz
		Am280XXM −55°C to +125°C		0		3	
$t_{\phi d}$	Delay Between clocks			5		Note 5	ns
$t_{\phi pw}$	Clock LOW Time			0.070		Note 8	μs
t_r, t_f	Clock Rise and Fall Times	10% to 90%				1.0	μs
t_s(D)	Set-up Time, Data Input (see definitions)	t_r = t_f = 50ns				150	ns
t_h(D)	Hold Time, Data Input (see definitions)	t_r = t_f = 50ns				0	ns
t_s(C)	Set-up Time, Read, Write and Recirculate Controls (see definitions)	t_r = t_f = 50ns				135	ns
t_h(C)	Hold Time, Read, Write and Recirculate Controls (see definitions)	t_r = t_f = 50ns				0	ns
t_{pd}	Delay, Clock to Data Out	R = HIGH	0°C to +70°C			100	ns
			−55°C to +125°C			150	
C_{in}, C_{out}	Capacitance, Any Input and Output (Note 6)	f = 1 MHz, V_{IN} = V_{CC}				5	pF
C_ϕ	Clock Input Capacitance (Note 6)	f = 1 MHz, V_{IN} = V_{CC}	Am2805/7			50	pF
			Am2806/8			100	

Notes: 5. The maximum delay between clocks (ϕ_1 and ϕ_2 both HIGH) is a function of junction temperature. The junction temperature is a function of ambient temperature and clock duty cycle. See curves for minimum frequency on page 3.
6. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.
7. For some reason known only to God and Intel, the convention for ϕ_1 and ϕ_2 for this device are reversed from the normal. ϕ_1 is the output clock and ϕ_2 is the input clock.
8. 100μsec or 50% duty cycle, whichever is less.

DEFINITION OF TERMS

Dynamic Shift Register A shift register in which data storage occurs on small capacitive nodes rather than in bistable logic circuits. Dynamic shift registers must be clocked continuously to maintain the charge stored on the nodes.

ϕ_1, ϕ_2 The two clock pulses applied to the register. The clock is ON when it is at its negative voltage level and OFF when it is at V_{SS} or V_{CC}. Data is accepted into the master of each bit during ϕ_2 and is transferred to the slave of each bit during ϕ_1.

f_{max} The maximum frequency at which the register will operate. This is the data rate through the register and also the frequency of each clock signal.

$t_{\phi d}$ Clock delay time. The time elapsing between the LOW-to-HIGH transition of one clock input and the HIGH-to-LOW transition of the other clock input. During $t_{\phi d}$ both clocks are HIGH and all data is stored on capacitive nodes.

$t_{\phi pw}$ Clock pulse width. The LOW time of each clock signal. During $t_{\phi pw}$ one of the clocks is ON, and data transfer between master and slave or slave and master occurs.

t_r, t_f Clock rise and fall times. The time required for the clock signals to change from 10% to 90% of the total level change occuring.

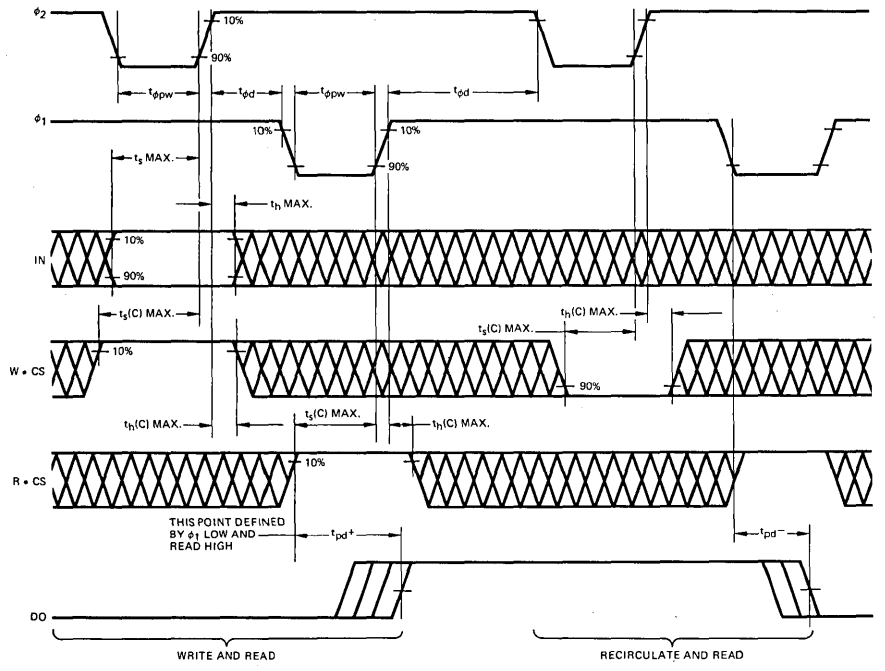
t_s(D) Data set-up time. The time prior to the LOW-to-HIGH transition of ϕ_2 during which the data on the data input must be steady to be correctly written into the memory.

t_h(D) Data hold time. The time following the LOW-to-HIGH transition of ϕ_2 during which the data must be steady. To correctly write data into the register, the data must be applied by t_s(D) before this transition and must not be changed until t_h(D) after this transition.

t_s(C), t_h(C) The set-up and hold times for the Read, Write, and Chip Select controls, relative to the LOW-to-HIGH transition of the appropriate clock phase.

t_{pd} The delay from the start of a read cycle to correct data present at the register output. A read cycle is begun when ϕ_1 is LOW AND Read is HIGH.

SWITCHING WAVEFORMS

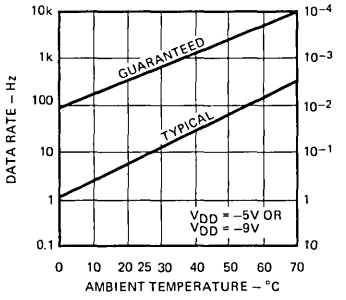


KEY TO TIMING DIAGRAM

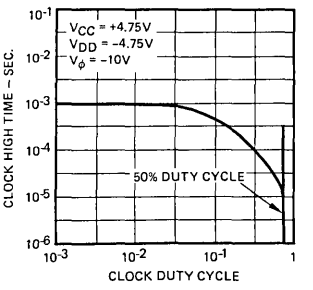
WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
▨	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
▨	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
▨	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN

OPERATING CHARACTERISTICS

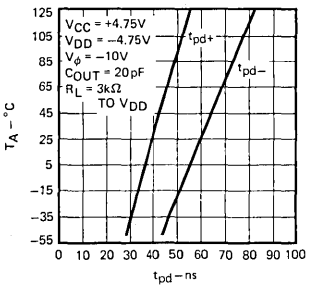
Minimum Operating Data Rate or Maximum Clock Pulse Delay Versus Temperature



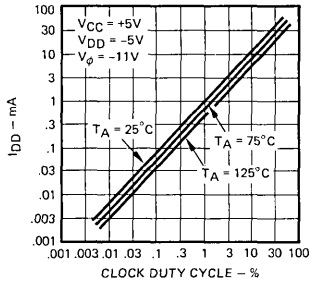
Maximum Clock High Time Versus Clock Duty Cycle



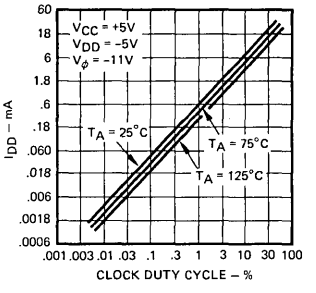
Propagation Delay Versus Ambient Temperature



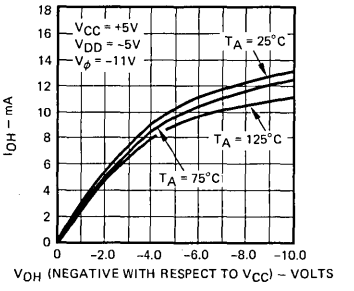
Am2806/8 I_{DD} Current Versus Clock Duty Cycle



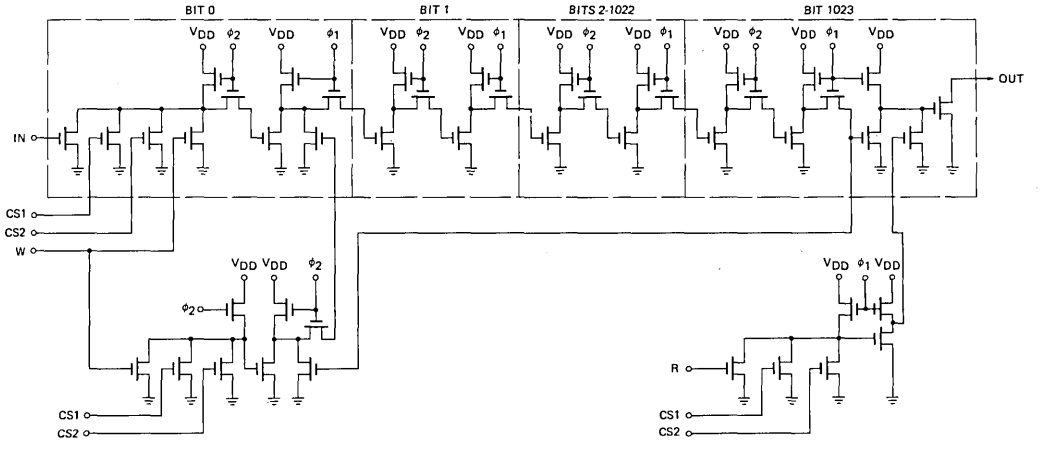
Am2805/7 I_{DD} Current Versus Clock Duty Cycle



V_{OH} Versus I_{OH}



SCHEMATIC DIAGRAM

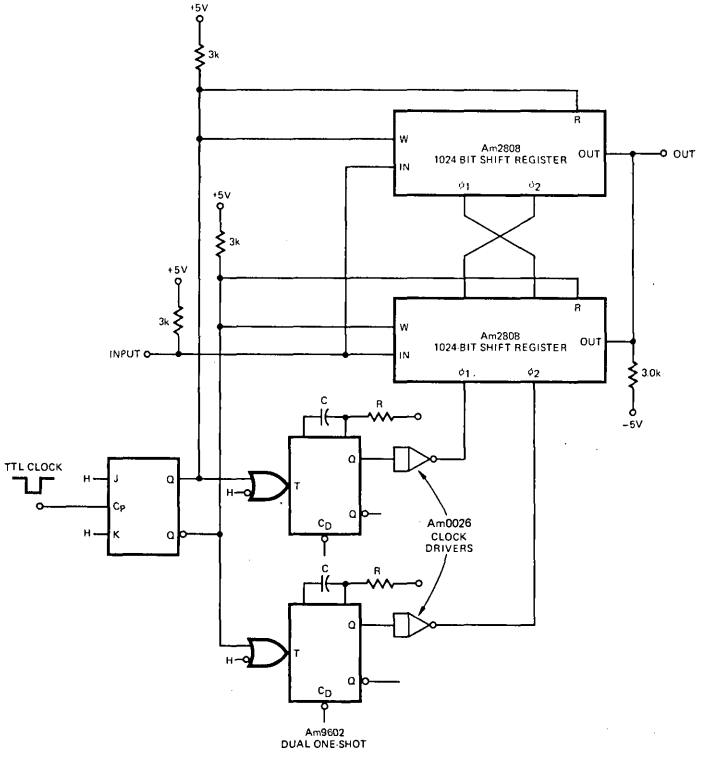


Note: No CS inputs on Am2807/8

⏚ = V_{CC}

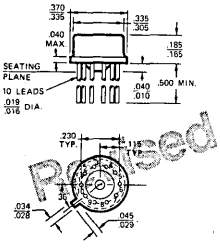
APPLICATIONS

Multiplexed 2048-Bit Recirculating Register
f_{max} = 6MHz

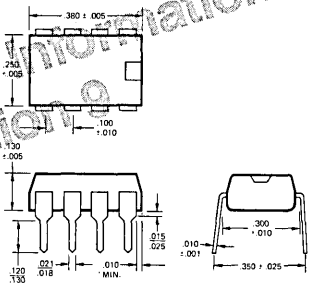


PHYSICAL DIMENSIONS

TO-100 Low

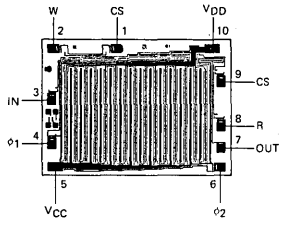


Molded Mini-DIP



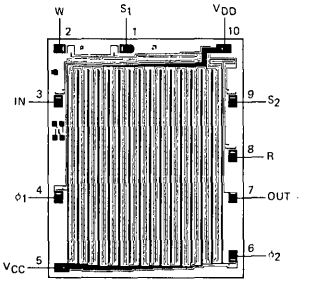
Metallization and Pad Layout
Am2805/7

106 x 78 Mils



Metalization and Pad Layout
Am2806/8

106 x 131 Mils



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Am1402A/1403A/1404A
Am2802/2803/2804
1024-Bit Dynamic Shift Registers

Distinctive Characteristics

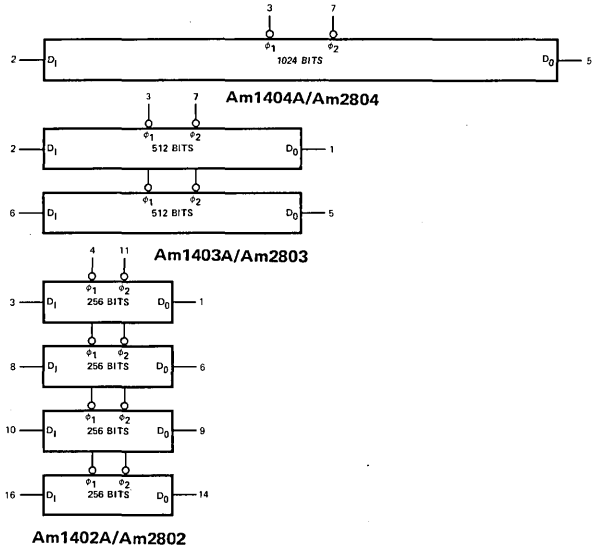
- Quad 256-bit, dual 512-bit, single 1024-bit
- 10 MHz frequency operation guaranteed for Am2802, Am2803 and Am2804.
- Low power dissipation of 0.1 mW/bit at 1 MHz
- DTL and TTL compatible
- Both military and commercial grade devices available
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically tested and optically inspected die for the assemblers of hybrid products

FUNCTIONAL DESCRIPTION

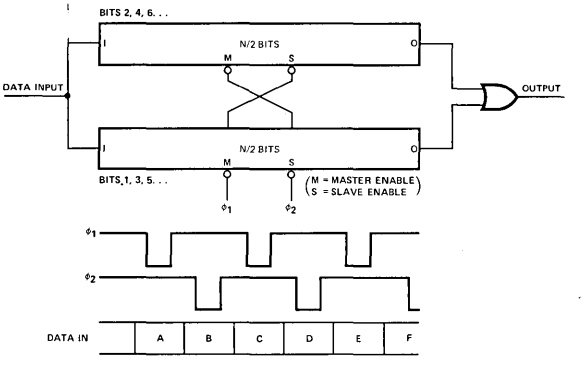
The Am1402A, 3A, and 4A are 1024-bit silicon gate dynamic shift registers. The low threshold characteristics of this technology allow high-speed operation and DTL and TTL compatibility. The Am1402A is a quad 256-bit device; the Am1403A is a dual 512-bit register; and the Am1404A is a single 1024-bit register. All three devices require two-phase non-overlapping clocks, and provide a one-bit shift on each clock pulse. The Am2802, 3, and 4 registers are functionally identical to the Am1402A, 3A, and 4A, but are guaranteed to operate over frequencies from 400 Hz to 10 MHz.

BLOCK DIAGRAMS

Am1402A/1403A/1404A Shift Registers



Functional Equivalent of Each Register



Since the two registers shift on opposite clock pulses, a new data bit is entered on both ϕ_1 and ϕ_2. Data entering the register on ϕ_1 will appear at the output on ϕ_1 (from the negative edge of ϕ_1 to the negative edge of ϕ_2).

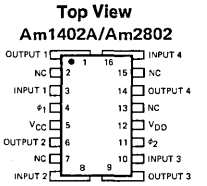
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Standard Speed Range Order Number	Extended Speed Range Order Number
Am1402A/ 2802	Hermetic DIP	0°C to +70°C	AM1402A	AM2802DC
	Hermetic DIP	−55°C to +125°C	AM1402ADM	AM2802DM
	Molded DIP	0°C to +70°C	AM1402APC	AM2802PC
Am1403A/ 2802	TO-99	0°C to +70°C	AM1403A	AM2803HC
	TO-99	−55°C to +125°C	AM1403AHM	AM2803HM
	Molded DIP	0°C to +70°C	AM1403APC	AM2803PC
AM1404A/ 2804	TO-99	0°C to +70°C	AM1404A	AM2804HC
	TO-99	−55°C to +125°C	AM1404AHM	AM2804HM
	Molded DIP	0°C to +70°C	AM1404APC	AM2804PC

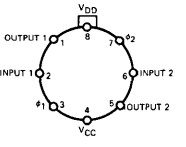
CONNECTION DIAGRAMS

Top View

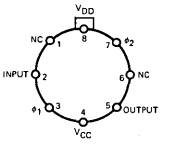
Am1402A/Am2802



Am1403A/Am2803



Am1404A/Am2804



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +160°C
Temperature Under Bias	−55°C to +125°C
Power Dissipation (Note 1)	600 mW
Data and Clock Input Voltages with respect to most Positive Supply Voltage, V_{CC}	0.3 V to −20 V
Power Supply Voltage, V_{DD} with respect to V_{CC}	0.3 V to −20 V

OPERATING RANGE

Part Number	V_{CC}	V_{DD}	Temperature Range
Am1402A, Am1403A, Am1404A	5V ±5%	−4.75V to −9.45V	0°C to +70°C
Am1402ADM, Am1403AHM, Am1404AHM	5V ±5%	−4.75V to −9.45V	−55°C to +125°C
Am2802DC, Am2803HC, Am2804HC	5V ±5%	−5V ±5%	0°C to +70°C
Am2802DM, Am2803HM, Am2804HM	5V ±5%	−5V ±5%	−55°C to +125°C

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Am1402A, 3A, 4A Min.	Typ.	Max.	Am2802, 3, 4 Min.	Typ.	Max.	Units
V_{IH}	Input HIGH Voltage			V_{CC}−2.0			V_{CC}−2.0			V
V_{IL}	Input LOW Voltage			V_{CC}−10		V_{CC}−4.2	V_{CC}−10		V_{CC}−4.2	V
I_I	Input Current	T_A = 25°C			<10	500		<10	500	nA
I_O	Output Leakage Current	T_A = 25°C, V_{OUT} = 0V			<10	1000		<10	1000	nA
$I_{\phi L}$	Clock Leakage Current	T_A = 25°C, V_ϕ = −12V			10	1000		10	1000	nA
V_{OH}	Output HIGH Voltage Driving TTL	R_L = 3k to V_{DD}, V_{DD} = −5V ±5%		2.4	3.5		V_{CC}−1.9	V_{CC}−1		V
	Output HIGH Voltage Driving MOS	R_L = 4.7k to V_{DD}, V_{DD} = −5V ±5%		V_{CC}−1.9	V_{CC}−1		V_{CC}−1.9 (Note 2)	V_{CC}−1 (Note 2)		V
	Output HIGH Voltage Driving TTL	R_L = 4.7k to V_{DD}, V_{DD} = −9V ±5%		2.4	3.5					
	Output HIGH Voltage Driving MOS	R_L = 6.2k to V_{DD}, 3.9k to V_{CC} V_{DD} = −9V ±5%		V_{CC}−1.9	V_{CC}−1					
V_{OL}	Output LOW Voltage	V_{DD} = −5V ±5%, R_L = 3k to V_{DD}, I_{OL} = −1.6mA			−0.3	0.5		−0.3	0.5	V
		R_L = 4.7k to V_{DD} V_{DD} = −9V ±5%, I_{OL} = −1.6mA			−0.3	0.5				
$V_{\phi H}$	Clock Input HIGH Level			V_{CC}−1		V_{CC}+0.3	V_{CC}−1		V_{CC}+0.3	V
$V_{\phi L}$	Clock Input LOW Level	V_{DD} = −5V ±5%		V_{CC}−15		V_{CC}−17	V_{CC}−15		V_{CC}−17	V
		V_{DD} = −9V ±5%		V_{CC}−12.6		V_{CC}−14.7				
I_{DD}(−5) (Note 1)	V_{DD} Current, V_{DD} = −5V ±5%	5MHz Data Rate 33% Duty Cycle $V_{\phi L}$ = V_{CC}−17V	T_A = 25°C		40	50		40	50	mA
			T_A = 0°C			56			56	
	V_{DD} Current, V_{DD} = −5V ±5%		T_A = −55°C						70	
		10MHz Data Rate 40% Duty Cycle $V_{\phi L}$ = V_{CC}−17	T_A = 25°C					50	60	mA
			T_A = 0°C						68	
			T_A = −55°C						80	
I_{DD}(−9) (Note 1)	V_{DD} Current, V_{DD} = −9V ±5%	3MHz Data Rate 26% Duty Cycle $V_{\phi L}$ = V_{CC}−14.7V	T_A = 25°C		30	40		30	40	mA
			T_A = 0°C			45			45	
			T_A = −55°C						60	

SWITCHING CHARACTERISTICS AND OPERATING CONDITIONS (Over Operating Range)

Am1402A/Am1403A/Am1404A

Parameter	Description	Test Conditions	$V_{DD} = -5\ V \pm 5\%$ (Test Load 1) Min.	Typ.	Max.	$V_{DD} = -9\ V \pm 5\%$ (Test Load 2) Min.	Typ.	Max.	Units
f_c	Clock Frequency Range		(Note 1)		2.5	(Note 1)		1.5	MHz
f_d	Data Repetition Rate		(Note 1)		5.0	(Note 1)		3.0	MHz
$t_{\phi PW}$	Clock Pulse Width		0.13	1.0		0.17		10	μs
$t_{\phi d}$	Clock Pulse Delay (Note 2)	$t_{\phi PW}$ = 130 ns	10		(Note 2)	10		(Note 2)	ns
t_f, t_r	Clock Pulse Rise/Fall Time				1000			1000	ns
t_s	Data Set Up Time	$t_r = t_f \leq 50$ ns	30		30	60		60	ns
t_h	Data Hold Time	$t_r = t_f \leq 50$ ns	20		20	20		20	ns
t_{pd+}, t_{pd-}	Clock to Data Out Delay				90			110	ns
C_{IN}*	Input Capacitance	@ 1 MHz, 250 mVPP		5	10		5	10	pF
C_{OUT}*	Output Capacitance	@ 1 MHz, 250 mVPP		5	10		5	10	pF
C_ϕ*	Clock Capacitance	@ 1 MHz, 250 mVPP		110	140		110	140	pF

SWITCHING CHARACTERISTICS AND OPERATING CONDITIONS (Over Operating Range)

Am2802/Am2803/Am2804

Clock Pulse Width = 70nsec
Clock LOW Level = (V_{CC}-15)

Parameter	Description	Test Conditions	$V_{DD} = -5\ V \pm 5\%$ (Test Load 1) Min.	Typ.	Max.	Units
f_c	Clock Frequency Range	$t_r = t_f = 10$ ns	(Note 1)		5.0 (Note 4)	MHz
f_d	Data Repetition Rate (Note 1)		(Note 3)		10.0 (Note 4)	MHz
$t_{\phi PW}$	Clock Pulse Width		0.07		10	μs
$t_{\phi d}$	Clock Pulse Delay	$t_{\phi PW}$ = 70 ns	10		(Note 2)	ns
t_f, t_r	Clock Pulse Rise/Fall Time				1000	ns
t_s	Data Set Up Time		30			ns
t_h	Data Hold Time		20			ns
t_{pd+}, t_{pd-}	Clock to Data Out Delay				90	ns

Notes:
1. See minimum operating frequency graph for low limits on data rep. rate.
2. Upper limit on $t_{\phi d}$ is determined by minimum frequency.
3. See max clock pulse delay graph for guarantee.
4. For additional information on 10MHz operation (5MHz clock rate) see AMD application note dated July 1973 on "Applications of Dynamic Shift Registers."

DESCRIPTION OF TERMS

OPERATIONAL TERMS

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into junction of output and load resistor.

V_{IH} Logic HIGH input voltage.

V_{IL} Logic LOW input voltage.

V_{OL} Clock LOW input voltage.

V_{OH} Clock HIGH input voltage.

I_I Input leakage current.

I_O Output leakage current.

I_{DD} Power supply current.

C_{IN} Input capacitance.

C_ϕ Input clock capacitance.

C_{OUT} Output capacitance.

FUNCTIONAL TERMS

ϕ_1, ϕ_2 The two clock phases required by the dynamic shift register.

f_c The clock frequency of the shift register.

f_d The input data repetition rate.

SWITCHING TERMS

t_{ϕ_d} The delay between the LOW to HIGH transition of a clock phase to the HIGH to LOW transition of the other clock phase.

$t_{\phi PW}$ The clock pulse widths necessary for correct operation.

t_r, t_f The clock pulse rise and fall times necessary for correct operation.

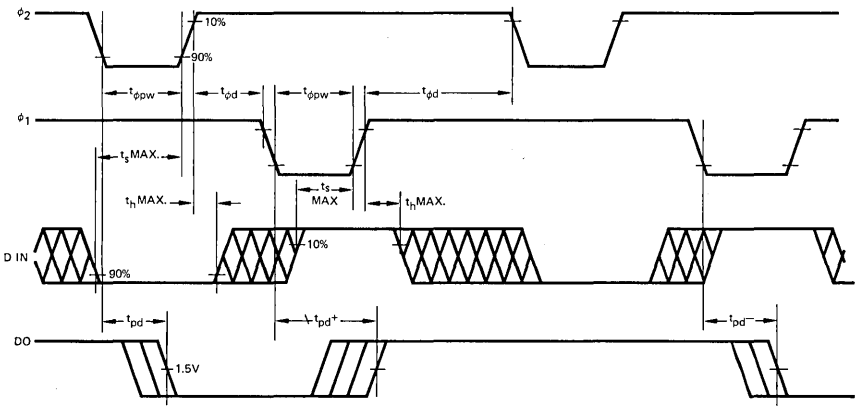
t_s The time required for the input data to be present prior to the LOW to HIGH transition of the clock phase to ensure correct operation.

t_h The time required for the input data to remain present after the LOW to HIGH transition of the clock phase to ensure correct operation.

t_{pd+} The propagation delay from the HIGH to LOW clock phase ϕ_1 transition to the output LOW to HIGH transition.

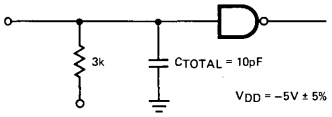
t_{pd-} The propagation delay from the HIGH to LOW clock phase ϕ_2 transition to the output HIGH to LOW transition.

SWITCHING WAVEFORMS

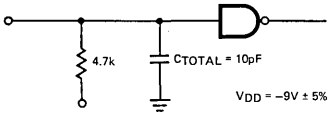


Clock Rise Time 10 ns
Clock Fall Time 10 ns
Output Load 1 TTL Load

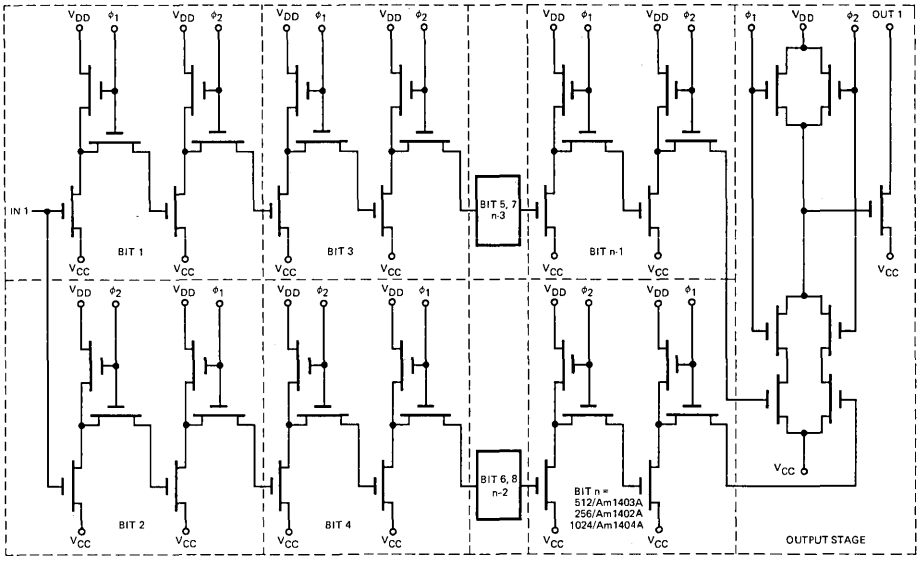
Test Load 1



Test Load 2

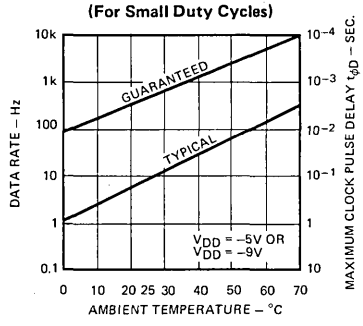


CIRCUIT DIAGRAM

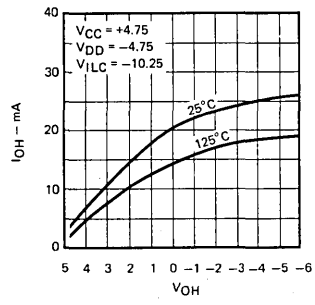


POWER CHARACTERISTICS

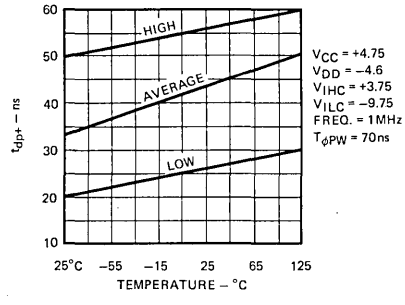
Minimum Operating Data Rate or Maximum Clock Pulse Delay Versus Temperature
(For Small Duty Cycles)



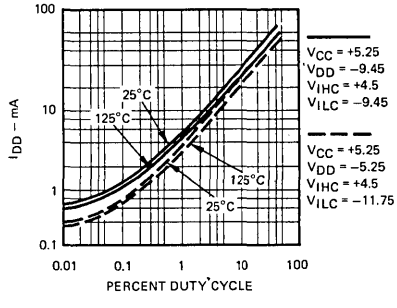
I_{OH} Versus V_{OH}



Typical Range of t_{pd+} Versus Temperature



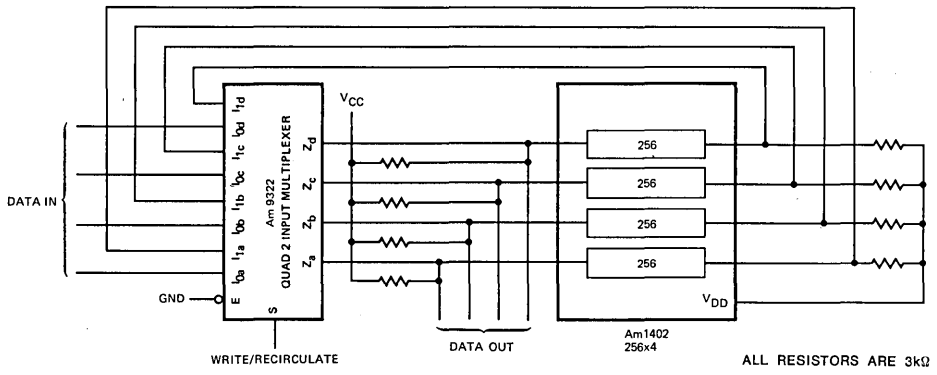
I_{DD} Versus Clock Duty Cycle



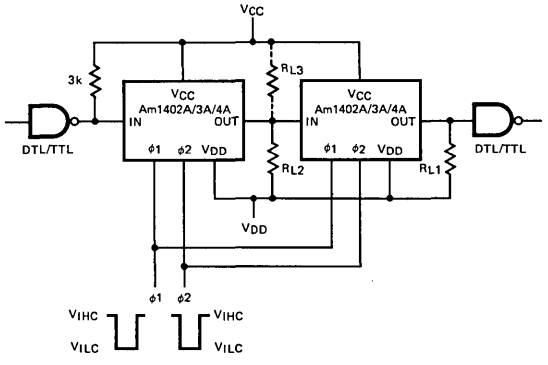
APPLICATIONS

256-Bit Delay

Write Recirculate Logic



DTL/TTL To MOS To DTL/TTL Interface

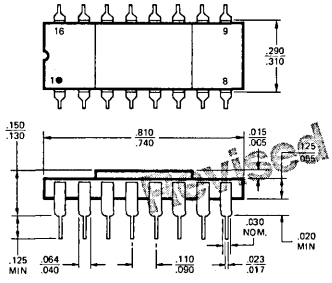


R_L Load Resistor Values for Different V_{DD} Supplies

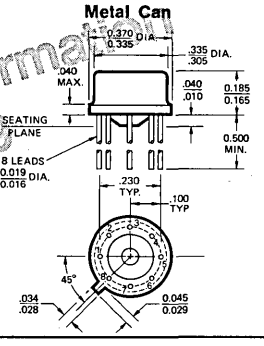
	$V_{CC} = 5$ V, $V_{DD} = -5$ V	$V_{CC} = 5$ V, $V_{DD} = -9$ V
R_{L1}	3.0 k	4.7 k
R_{L2}	4.7 k	6.2 k
R_{L3}	Not required	3.9 k

PHYSICAL DIMENSIONS

Dual-In-Line

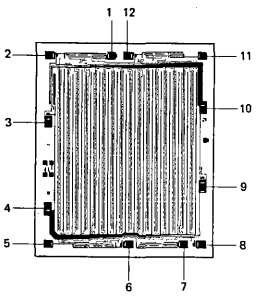


Metal Can



PAD	1402A/2802 PIN	1402A/2802 SIGNAL	1403A/2803 PIN	1403A/2803 SIGNAL	1404A/2804 PIN	1404A/2804 SIGNAL
1	1	OUT 1				
2	3	IN 1	2	IN 1	2	IN
3	4	$\phi 1$	3	$\phi 1$	3	$\phi 1$
4	5	V_{CC}	4	V_{CC}	4	V_{CC}
5	6	OUT 2	5	OUT 2	5	OUT
6	8	IN 2				
7	9	OUT 3				
8	10	IN 3	6	IN 2	7	$\phi 2$
9	11	$\phi 2$	7	$\phi 2$		
10	12	V_{DD}	8	V_{DD}		
11	14	OUT 4	1	OUT 1	8	V_{DD}
12	16	IN 4				

Metallization and Pad Layout



DIE SIZE .109" X .131"

ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
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(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am2809
Dual 128-Bit Static Shift Register

Distinctive Characteristics

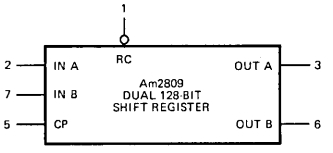
- Second source to Signetics 2521V.
- TTL compatible on clock and data inputs.
- Operation guaranteed from DC-to-2.5MHz.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Low capacitance on clock and data inputs.

FUNCTIONAL DESCRIPTION

The Am2809 is a dual 128-bit static shift register built using P-channel silicon gate MOS technology. The two registers have a common clock input which is low-threshold TTL compatible. The registers also have built-in recirculate feedback. When the recirculate control ($\overline{RC}$) is LOW, the data on the data output of each register is fed back to the corresponding register input. When $\overline{RC}$ is HIGH, each register accepts data from the data input. Each of the register outputs can drive one standard TTL load or three Am93L series low-power unit loads.

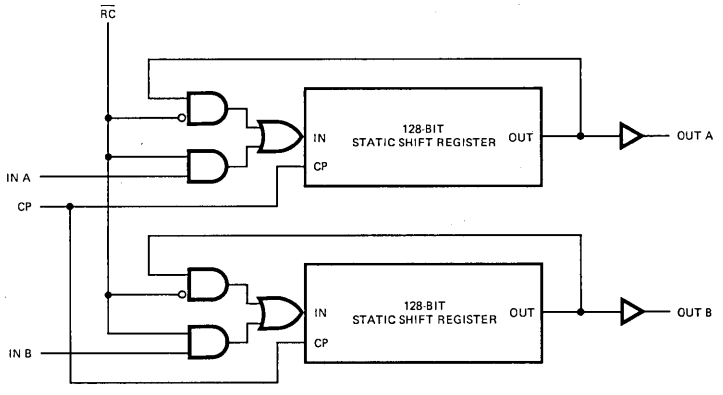
Data in the Am2809 is shifted on the LOW-to-HIGH edge of the input clock. Data on the data inputs must remain steady for a set-up time before and a hold time after this clock transition. Since storage in the register is static, the register may be halted indefinitely with the clock in the HIGH state.

LOGIC SYMBOL



V_{CC} = Pin 8
V_{GG} = Pin 4

LOGIC BLOCK DIAGRAM

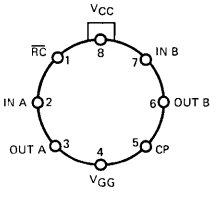


ORDERING INFORMATION

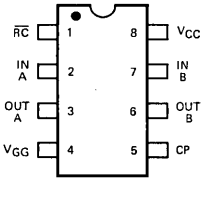
Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2809PC
TO-5	0°C to +70°C	AM2809HC
TO-5	−55°C to +125°C	AM2809HM

CONNECTION DIAGRAMS
Top Views

Am2809HC
Am2809HM



Am2809PC



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
DC Input Voltage with Respect to V_{CC}	−20V to +0.3V

OPERATING RANGE

Part Number	Ambient Temperature	V_{CC}	V_{GG}
Am2809PC Am2809HC	0°C to +70°C	5.0V ±5%	−12V ±5%
Am2809HM	−55°C to +125°C	5.0V ±5%	−12V ±5%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.1mA		V_{CC} −1.5			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 1.6mA			−4	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		V_{CC} −1.7		V_{CC} +0.3	Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				V_{CC} −3.95	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0	T_A = 25°C		10	500	nA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V, T_A = 25°C			10	500	nA
I_{GG}	Power Supply Current	f = 2.5MHz	T_A = 25°C		24	32	mA
		V_{CC} = MAX.	T_A = 0°C to +70°C			38	
		f = 2.0MHz	T_A = −55°C to +125°C			44	

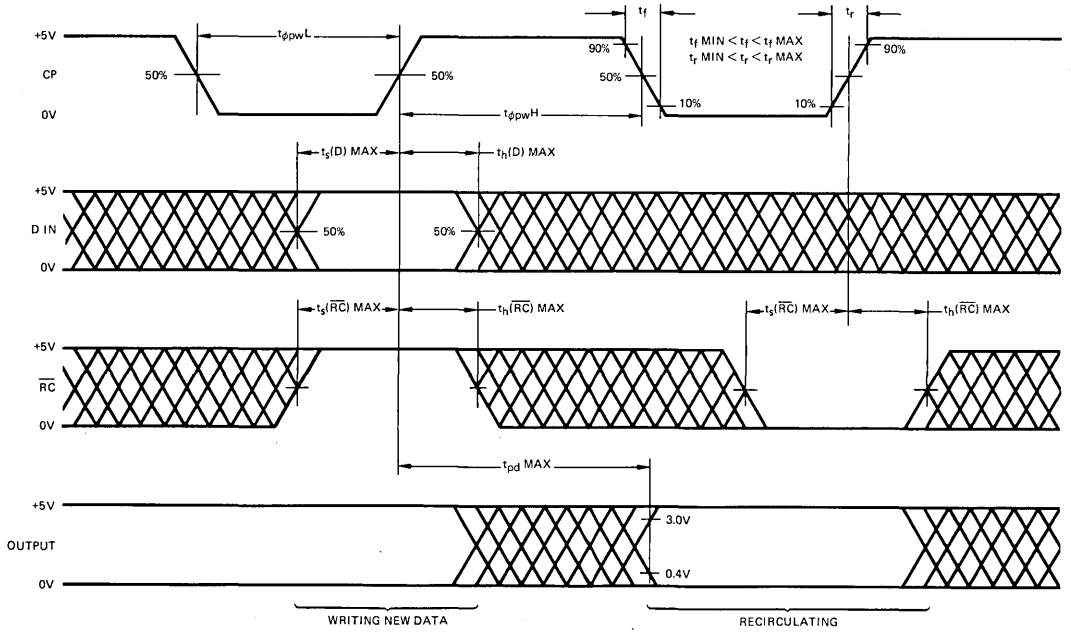
Note: 1. Typical Limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions	Am2809PC Am2809HC Min.	Typ.	Max.	Am2809HM Min.	Typ.	Max.	Units
f_c	Clock Frequency Range		0		2.5	0		2.0	MHz
$t_{\phi pw}H$	Clock HIGH Time		0.2		∞	0.4		∞	μs
$t_{\phi pw}L$	Clock LOW Time		0.2		100	0.25		100	μs
t_r, t_f	Clock Rise and Fall Times	10% to 90%			1.0			1.0	μs
t_s(D)	Set-up Time, Data Input (see definitions)	$t_r = t_f$ = 50ns			75			100	ns
t_h(D)	Hold Time, Data Input (see definitions)	$t_r = t_f$ = 50ns			50			65	ns
$t_s(\overline{RC})$	Set-up Time, Recirculate Control (see definitions)	$t_r = t_f$ = 50ns			50			100	ns
$t_h(\overline{RC})$	Hold Time, Recirculate Control (see definitions)	$t_r = t_f$ = 50ns			50			65	ns
t_{pd}	Delay, Clock to Data Out			170	300		170	350	ns
C_{in}	Capacitance, Any Input (Note 2)	f = 1MHz, V_{IN} = V_{CC}		3	7		3	7	pF

 Note: 2. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.

TIMING DIAGRAM

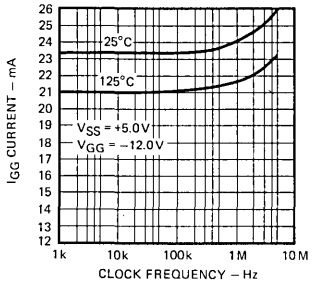


KEY TO TIMING DIAGRAM

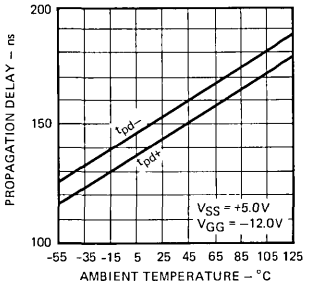
WAVEFORM	INPUTS	OUTPUTS	WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY		MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L		DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN

CHARACTERISTIC CURVES

Typical Power-Supply Currents Versus Frequency



Typical Propagation Delay Versus Ambient Temperature

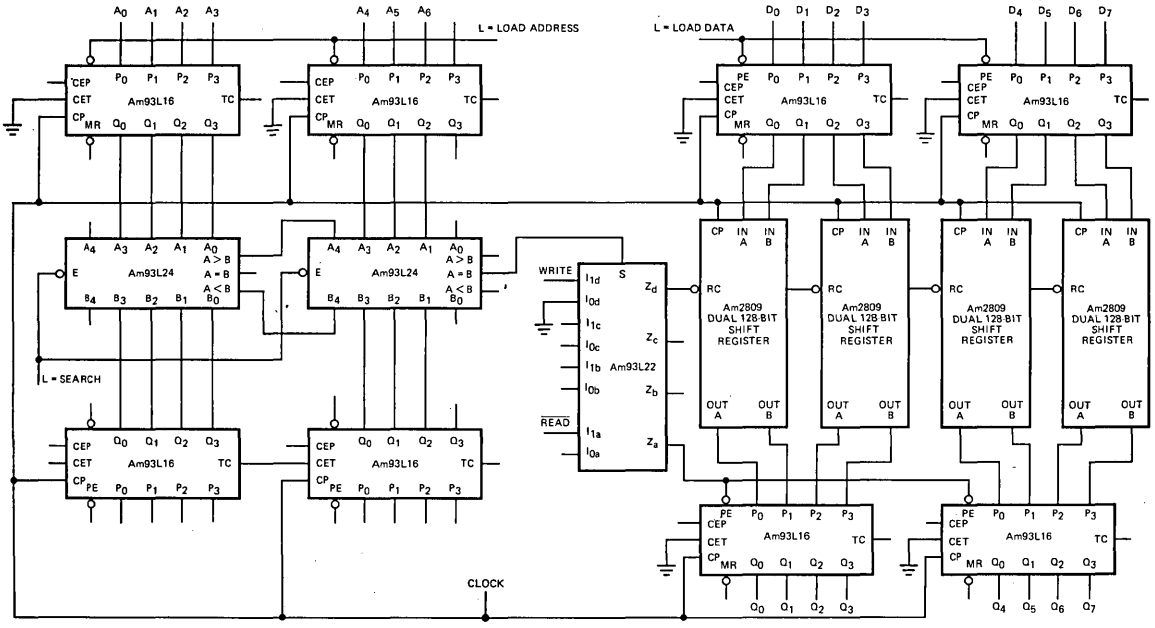


DEFINITION OF TERMS

STATIC SHIFT REGISTER A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is LOW and is transferred to the static slaves while the clock is HIGH. The clock may be stopped indefinitely in the HIGH state, but there are limitations on the time it may reside in the LOW state.

SET-UP and HOLD TIMES The shift register will accept the data that is present on its input around the time the clock goes from LOW-to-HIGH. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

APPLICATIONS

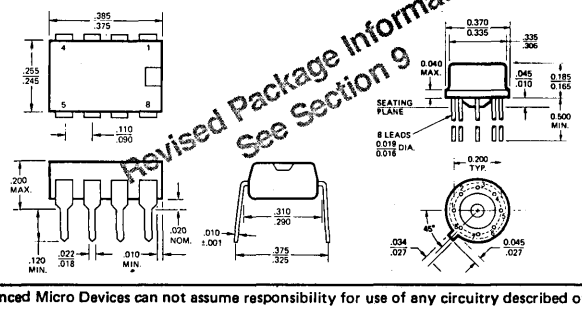


128-Word x 8-Bit Pseudo-Random Access Memory

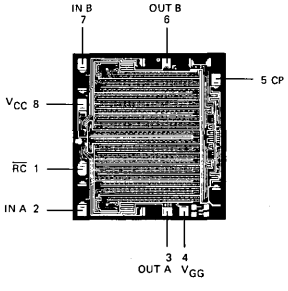
Data stored in the four dual 128-bit shift registers can be accessed randomly by comparing the desired address with the address currently available at the shift register I/O. A pair of Am93L16 low-power counters keeps track of data addresses as the data circulates around the memory. Other Am93L16 counters are used as 4-bit registers with enables by grounding the count enables. They are used to store the requested address, the new data to be written into the memory, and the data read from the memory. The Am93L24 comparators switch the memories from the recirculate mode to the write mode to enter new data in a write operation. Similarly, the output storage registers are enabled when the Am93L24s indicate comparison in a read operation.

PACKAGE OUTLINES

Molded DIP



Metallization and Pad Layout



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Am2810·Am1002P·Am1002L

Dual 128-Bit Static Shift Register

Distinctive Characteristics

- 2nd Source to Mostek 1002P and 1002L.
- Built-in pull-up resistors.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Operation guaranteed from DC to 2MHz.

FUNCTIONAL DESCRIPTION

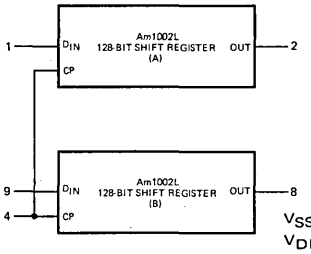
The Am2810/Am1002P is a dual 128-bit static shift register built using P-channel silicon gate MOS technology. The two registers each have a two-input multiplexer on their inputs, so that input data may be selected from one of two sources. Each register has a separate clock input, and operates with a low-voltage TTL clock signal. The registers shift on the LOW-to-HIGH edge of the clock signal. Data at the inputs must be steady for a set-up time before and a hold time after this clock transition. Since data storage is static, the clock may be halted indefinitely in the HIGH state. The outputs of each register can drive one TTL load or three Am93L low-power TTL loads.

The two-input multiplexer on the input of each register is controlled by the $\overline{RC}$ (recirculate control) input. When $\overline{RC}$ is LOW, data is accepted on the R_{in} input; when $\overline{RC}$ is HIGH, data is accepted on the D_{in} input. The inputs to the registers have built-in pull-up resistors to provide total TTL compatibility. The V_{RA} pin controls the pull-up resistors for register A D_{in} and $\overline{RC}$ inputs. The V_{RB} pin controls the pull-up resistors for the register B D_{in} and $\overline{RC}$ inputs. The $V_{R\phi}$ pin controls the resistor on the clock input to both registers. When the resistor control pins are tied to V_{GG} (−12V), the resistors are enabled and pull the inputs they affect up to V_{SS}. When the resistor control pins are tied to V_{SS} the resistors are all very high impedance and the inputs they affect all exhibit normal MOS characteristics. The R_{in} inputs are intended to be the recirculate inputs from an MOS output and these inputs do not have pull-up resistors associated with them.

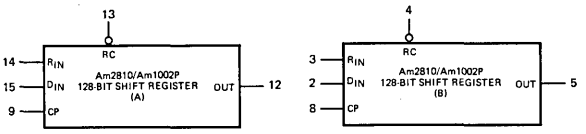
The Am1002L is the same device in a 10-lead TO-100 can with no recirculate controls and with all pull-up resistors disabled except those on the clock pin.

LOGIC SYMBOLS

1002L



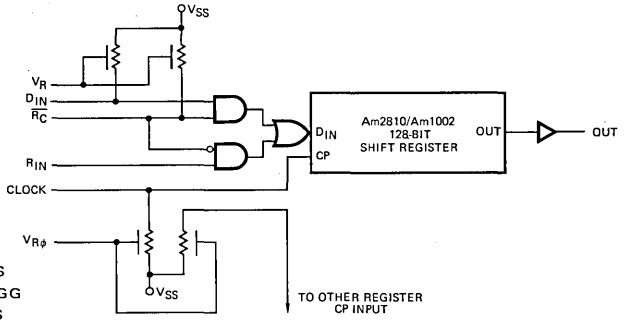
Am2810/1002P



V_{RA} = Pin 16
V_{RB} = Pin 1
$V_{R\phi}$ = Pin 10

V_{SS} = Pin 7
V_{DD} = Pin 6
V_{GG} = Pin 11

LOGIC BLOCK DIAGRAM (One Register Shown)

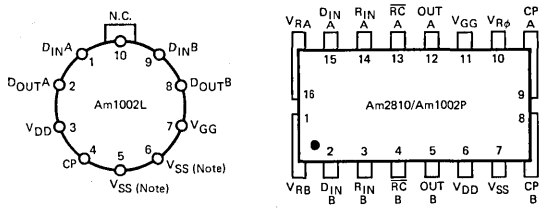


Note: On Am1002L:
V_R internally tied to V_{SS}
$V_{R\phi}$ internally tied to V_{GG}
$\overline{RC}$ internally tied to V_{SS}

ORDERING INFORMATION

Package Type	Temperature Range	Am2810 Order Number	1002P/ 1002L Order Number
Hermetic DIP	0°C to +75°C	Am2810DC	MK1002P
Hermetic DIP	−55°C to +125°C	Am2810DM	
TO-100	0°C to +75°C		MK1002L

CONNECTION DIAGRAMS



Notes: Pin 1 is marked for orientation.
Pins 5 and 6 on 1002L are tied together internally.

MAXIMUM RATING (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{DD} Supply Voltage	V_{SS} −10V to V_{SS} +0.3V
V_{GG} Supply Voltage	V_{SS} −20V to V_{SS} +0.3V
DC Input Voltage	V_{SS} −10V to V_{SS} +0.3V

OPERATING RANGE

Part Number	T_A	V_{SS}	V_{DD}	V_{GG}
Am2810XC Am1002P Am1002L	0°C to +75°C	5.0V ±5%	0 V	−12.0V ±5%
Am2810XM	−55°C to +125°C	5.0V ±5%	0 V	−12.0V ±5%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −100μA		V_{SS}−1			Volts
V_{OL}	Output LOW Voltage	I_{OL} = 1.6mA			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		V_{SS}−1			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				V_{SS}−4	Volts
I_{IL} (Note 2)	Resistors Disabled Input LOW Current	V_{SS} = MAX., V_{IN} = 0 V V_{RA} = V_{RB} = $V_{R\phi}$ = V_{SS}				−40	μA
$I_{IL(\Omega)}$ (Note 2)	Resistors Enabled Input LOW Current	V_{SS} = MAX., V_{IN} = 0.4V, Am2810/Am1002P only V_{RA} = V_{RB} = $V_{R\phi}$ = V_{GG}		−0.3		−2.0	mA
$I_{IL(\phi)}$	Input LOW Current Clock Input	1002L only		−0.6		−4.0	mA
I_{IH}	Input HIGH Current	V_{RA} = V_{RB} = $V_{R\phi}$ = V_{IN} = V_{SS}				40	μA
I_{SS}	V_{SS} Power Supply Current	f = 1MHz Inputs and Outputs Open	0°C to +75°C		14	25	mA
			−55°C to +125°C			35	
I_{GG}	V_{GG} Power Supply Current		0°C to +75°C		−4	−10	
			−55°C to +125°C			−15	

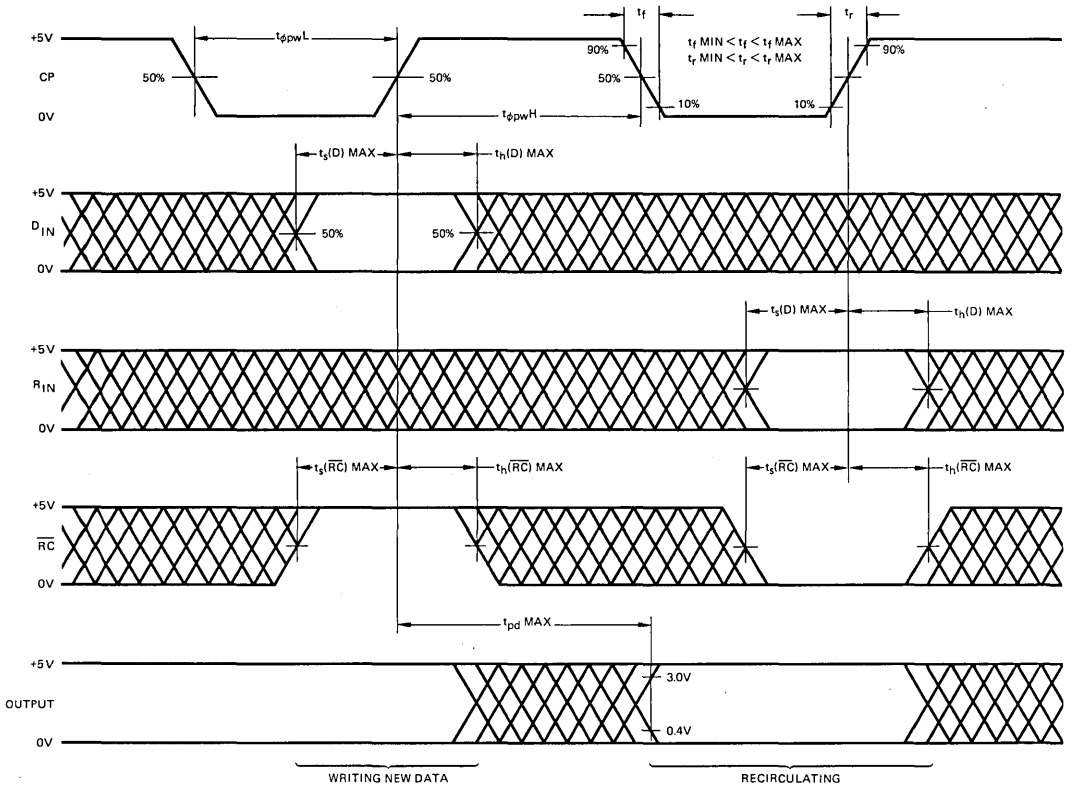
Notes: 1. Typical Limits are at V_{SS} = 5.0V, V_{GG} = −12V, 25°C ambient and maximum loading.
2. On chip pull-up resistors are provided for the clock and data inputs; they are enabled when the appropriate V_R input is at −12V. When the V_R inputs are at V_{SS}, the resistors are disabled and the inputs exhibit normal MOS characteristics (I_{IL} and I_{IH}), the recirculate data inputs have no pull-up resistors and always exhibit MOS characteristics. All pull-up resistors are disabled on the Am1002L except the one on the clock.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions	Am2810 Min.	Am2810 Typ.	Am2810 Max.	Am1002P/Am1002L Min.	Am1002P/Am1002L Typ.	Am1002P/Am1002L Max.	Units
f_{max}	Maximum Clock Frequency		2.0			1.0			MHz
$t_{\phi pw}H$	Clock HIGH Time		0.2		∞	0.4		∞	μs
$t_{\phi pw}L$	Clock LOW Time		0.2		100	0.3		10	μs
t_r, t_f	Clock Rise and Fall Times		10		200	10		200	ns
t_s(D)	Set-up Time, D or R Inputs (see definitions)	t_r = t_f = 50ns, V_R = −12V			100			50	ns
t_h(D)	Hold Time, D or R Inputs (see definitions)	t_r = t_f = 50ns, V_R = −12V			100			200	ns
$t_s(\overline{RC})$	Set-up Time, $\overline{RC}$ Input (see definitions)				100			100	ns
$t_h(\overline{RC})$	Hold Time, $\overline{RC}$ Input (see definitions)				200			300	ns
t_{pd}	Delay, Clock to Output LOW or HIGH	R_L = 2.9kΩ, C_L = 20pF	(Note 4)		250	(Note 4)		450	ns
t_{pr}, t_{pf}	Output Rise and Fall Times	10% to 90%			100			150	ns
C_{in}	Capacitance, Any Input (Note 3)	f = 1MHz, V_{IN} = V_{SS}		3	7		3	10	pF

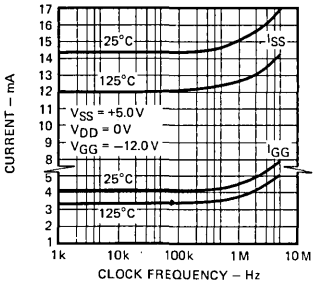
Notes: 3. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.
4. At any temperature, t_{pd} min. is always much greater than t_h(D) max.

TIMING DIAGRAM

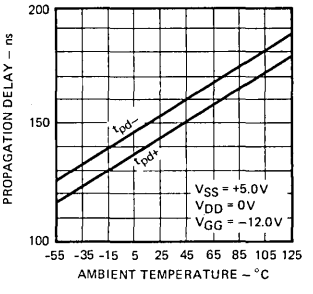


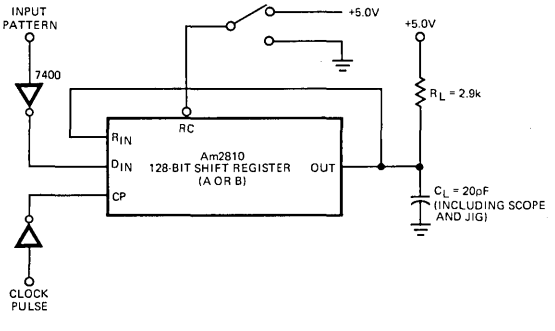
TEST CIRCUIT

Typical Power-Supply Currents Versus Frequency



Typical Propagation Delay Versus Ambient Temperature



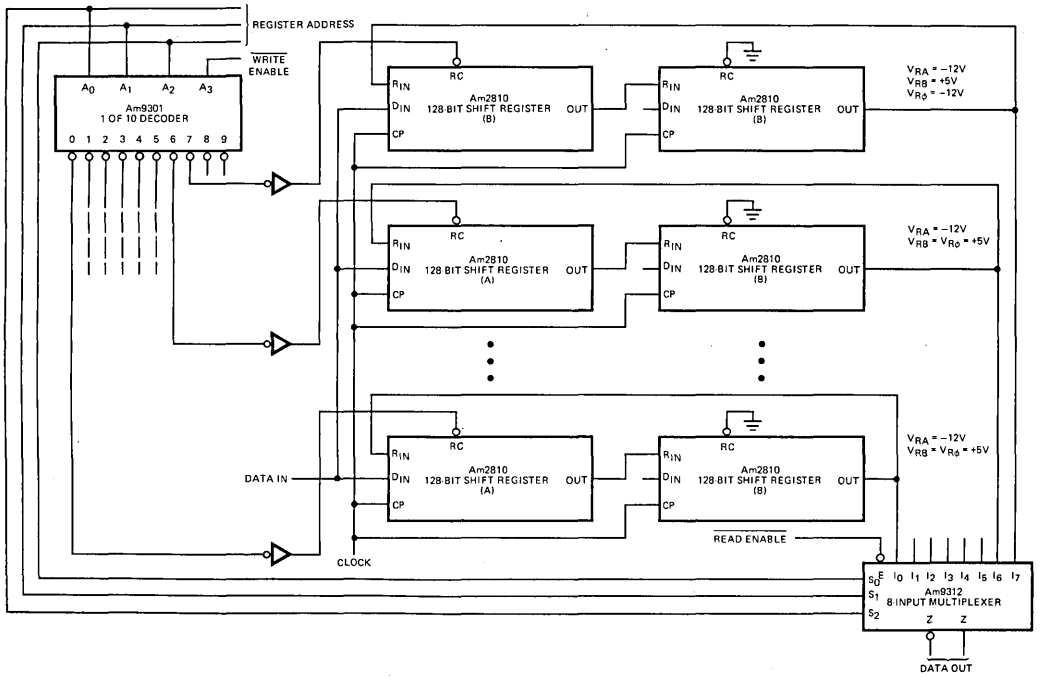


DEFINITION OF TERMS

STATIC SHIFT REGISTER A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is LOW and is transferred to the static slaves while the clock is HIGH. The clock may be stopped indefinitely in the HIGH state, but there are limitations on the time it may reside in the LOW state.

SET-UP and HOLD TIMES The shift register will accept the data that is present on its input around the time the clock goes from LOW-to-HIGH. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

APPLICATIONS

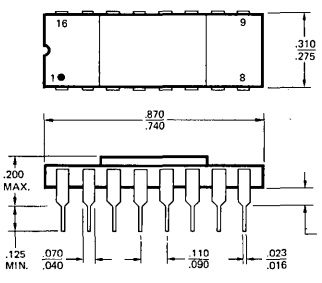


Eight Register 256-Bit Memory System

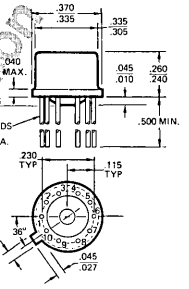
Data enters one of the eight 256-bit registers when the write enable input to the decoder is LOW. The addressed register will accept the data on the data input; the other seven registers will recirculate their data. Outputs are driven directly into an Am9312 8-input multiplexer. Obviously, the read and write registers need not be the same. Note that the $V_{R\phi}$ input is connected to V_{GG} on only one device; the pull-up resistor on this device will pull the line up for all the devices. The V_{RB} inputs are all connected to V_{SS}, since only MOS compatibility is needed. The V_{RA} inputs are all connected to V_{GG} because each recirculate input needs a separate pull-up. This also increases the loading on the data input.

PHYSICAL DIMENSIONS

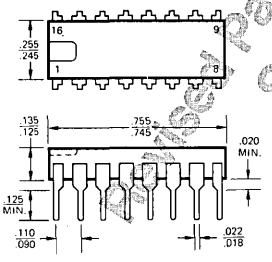
Side Brazed Dual-In-Line



TO-100



Molded



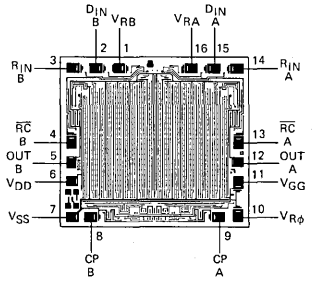
TRUTH TABLE

$\overline{RC}$	R_{IN}	D_{IN}	Data Entered
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

H = HIGH Voltage level
L = LOW Voltage Level
X = Don't Care

Am2810 Metallization and Pad Layout

86 x 95 MILS



ADVANCED MICRO DEVICES INC.
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TELEX: 34-6306

Am2812 / Am2812A • Am2813 / Am2813A

32 x 8 - Bit and 32 x 9 - Bit First-in First-out Memories

Distinctive Characteristics

- Completely independent read and write operations
- "Half-full" flag
- Am2812 has serial or parallel input and output
- Data rates up to 1 MHz

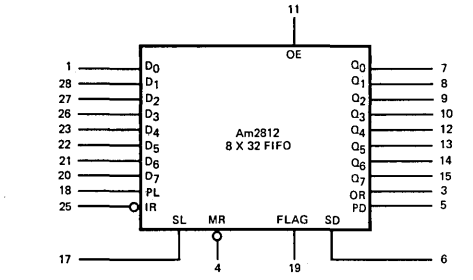
FUNCTIONAL DESCRIPTION

The Am2812 and Am2813 are 32 word by 8-bit and 9-bit first-in first-out memories, respectively. Both devices have completely independent read and write controls and have three-state outputs controlled by an output enable pin (OE). Data on the data inputs (D_i) are written into the memory by a pulse on load ($\overline{PL}$). The data word automatically ripples through the memory until it reaches the output or another data word. Data is read from the memory by applying a shift out pulse on PD. This dumps the word on the outputs (Q_i) and the next word in the buffer moves to the output. An output ready signal (OR) indicates that data is available at the output and also provides a memory empty signal. An input ready (IR) signal indicates that the device is ready to accept data and also provides a memory full signal. Both the Am2812 and Am2813 have master reset inputs which clear all data from the device (reset to all LOWs), and a FLAG signal which goes HIGH when the memory contains more than 15 words.

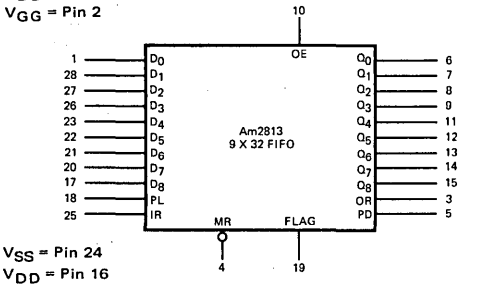
The Am2812 can perform input and output data transfer on a bit-serial basis as well as on 8-bit parallel words. The input buffer is in reality an 8-bit shift register which can be loaded in parallel by the PL command or can be loaded serially through the D_0 input by using the SL clock. When 8 bits have been shifted into the input buffer serially, the 8-bit word automatically moves in parallel through the memory. The output includes a built-in parallel-to-serial converter, so that data can be shifted out of the Q_7 output by using the SD clock. After 8 clock pulses a new 8-bit word appears at the outputs.

The timing and function of the four control signals, PL, IR, PD, and OR, are designed so that two FIFOs can be placed end to end, with OR of the first driving PL of the second and IR of the second driving PD of the first. With this simple interconnection, strings of FIFOs can control each other reliably to make a FIFO array any number of words deep.

LOGIC SYMBOLS



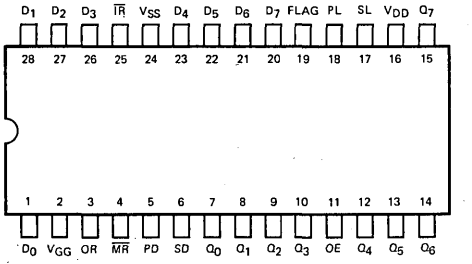
V_{SS} = Pin 24
V_{DD} = Pin 16
V_{GG} = Pin 2



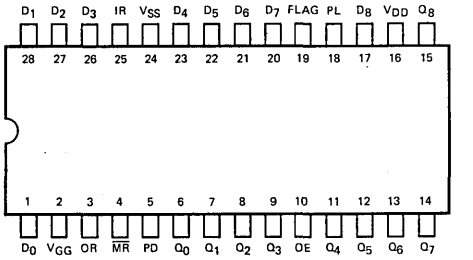
V_{SS} = Pin 24
V_{DD} = Pin 16
V_{GG} = Pin 2

CONNECTION DIAGRAMS
Top Views

Am2812



Am2813



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Frequency	Temperature Range	Am2812 Order Number	Am2813 Order Number
Hermetic DIP	500KHz	0°C to +70°C	AM2812DC	AM2813DC
Hermetic DIP	500KHz	–55°C to +125°C	AM2812DM	AM2813DM
Hermetic DIP	1MHz	0°C to +70°C	AM2812ADC	AM2813ADC
Hermetic DIP	1MHz	–55°C to +125°C	AM2812ADM	AM2813ADM

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°
Temperature (Ambient) Under Bias	−55°C to +125°
V_{DD} Supply Voltage	V_{SS} −7V to V_{SS} +0.3
V_{GG} Supply Voltage	V_{SS} −20V to V_{SS} +0.3
DC Input Voltage	V_{SS} −10V to V_{SS} +0.3

OPERATING RANGE

Part Number	Ambient Temperature	V_{SS}	V_{DD}	V_{GG}
Am2812DC, Am2812ADC	0°C to +70°C	5.0V ±5%	0V	−12V ±5%
Am2813DC, Am2813ADC				
Am2812DM, Am2812ADM	−55°C to +125°C	5.0V ±5%	0V	−12V ±5%
Am2813DM, Am2813ADM				

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = .300mA		V_{SS} −1.0			V
V_{OL}	Output LOW Voltage	I_{OL} = 1.6mA				0.4	V
V_{IH}	Input HIGH Level			V_{SS} −1.0			V
V_{IL}	Input LOW Level					0.8	V
I_{IL}	Input Leakage Current	V_{IN} = 0V				1.0	μA
I_{IH}	Input HIGH Current	V_{IN} = V_{SS} −1.0V		250			μA
V_{PUP}	Input Pull-up Initiation Voltage	(Note 2)	V_{SS} = MIN.			2.0	V
			V_{SS} = MAX.			2.2	V
V_{BAR}	Voltage at Peak Input Current	(Note 2)				V_{SS} −1.5	V
I_{BAR}	Maximum Input Current	(Note 2)				1.6	mA
I_{GG}	V_{GG} Current	T_A = 0°C to +70°C			14	22	mA
		T_A = −55°C to +125°C				27	
I_{DD}	V_{DD} Current	T_A = 0°C to +70°C			30	45	mA
		T_A = −55°C to +125°C				55	

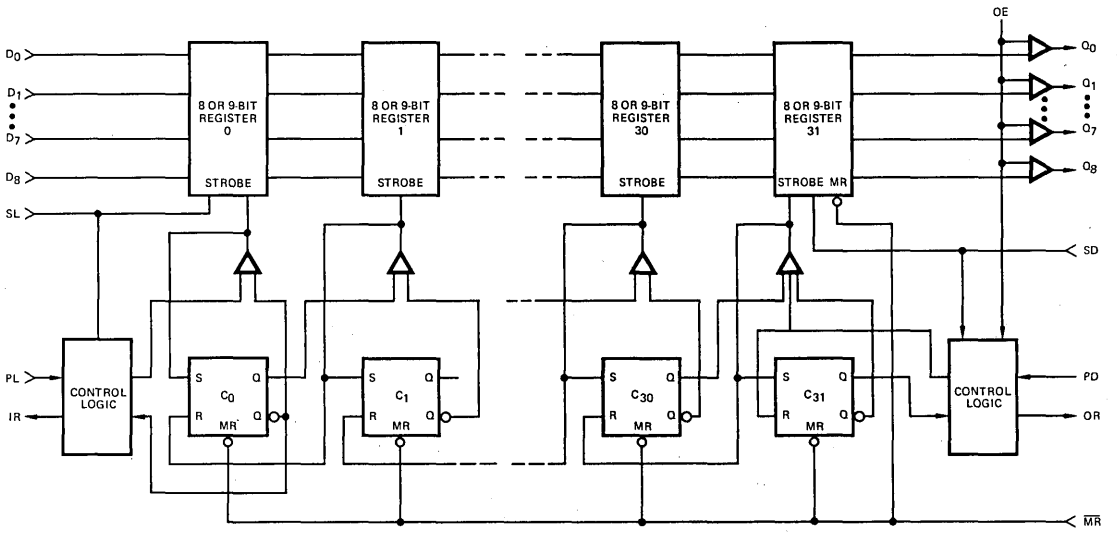
Notes: 1. Typical limits are at V_{SS} = 5.0V, V_{GG} = −12.0V, T_A = 25°C
2. Pull up circuit on Am2813 only. See graph of input V-I characteristics.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Conditions/Note	Test Conditions	Am2812 Am2813 Min.	Am2812 Am2813 Typ.	Am2812 Am2813 Max.	Am2812A Am2813A Min.	Am2812A Am2813A Typ.	Am2812A Am2813A Max.	Units
f_p	Maximum Parallel Load or Dump Frequency		0.5			1.0			MHz
t_{IR+}	Delay, PL or SL HIGH to IR In-Active		100	300	1100	80	300	450	ns
t_{IR-}	Delay, PL or SL LOW to IR Active		100	250	800	80	250	400	ns
$t_{pw}H(P)$	Minimum PL or PD HIGH Time				100			80	ns
$t_{pw}L(P)$	Minimum PL or PD LOW Time				100			80	ns
$t_{pw}H(S)$	Minimum SL or SD HIGH Time	Am2812 only			350			300	ns
$t_{pw}H(S)$	Minimum SL or SD LOW Time	Am2812 only			350			300	ns
$t_h(D)$	Data Hold Time			190	250		170	200	ns
$t_s(D)$	Data Set-Up Time	to PL			0			0	ns
		to SL			100			90	
t_{OR+}	Delay, PD or SD HIGH to OR LOW	OE HIGH	100	450	1100	100	350	520	ns
t_{OR-}	Delay, PD or SD LOW to OR HIGH	OE HIGH	100	400	850	100	300	470	ns
t_{PT}	Ripple through Time	FIFO Empty			10			8	μs
t_{DH}	Delay, OR LOW to Data Out Changing	PD = LOW	50	200		50	200		ns
t_{DA}	Delay, Data Out to OR HIGH	PD = HIGH	0	100		0	100		ns
t_{MRW}	Minimum Reset Pulse Width				400			400	ns
t_{DO}	Delay, OE LOW to Output OFF				400			400	ns
t_{EO}	Delay, OE HIGH to Output Active				400			400	ns
t_{DF}	Delay from PL or SL HIGH to Flag HIGH or PD or SD HIGH to Flag LOW			0.5	1.0		0.5	1.0	μs
CI	Input Capacitance				7			7	pF

Notes: 3. IR is active HIGH on Am2813 and active LOW on Am2812.
4. Minimum and maximum delays generally occur at opposite temperature extremes. Devices at approximately the same temperature will have compatible switching characteristics and will drive each other.

LOGIC BLOCK DIAGRAM



DESCRIPTION OF THE Am2812 and Am2813 FIFO OPERATION

The Am2812 and Am2813 FIFOs consist internally of 32 data registers and one 32-bit control register, as shown in the logic block diagram. A "1" in a bit of the control register indicates that a data word is stored in the corresponding data register. A "0" in a bit of the control register indicates that the corresponding data register does not contain valid data. The control register directs the movement of data through the data registers. Whenever the n^{th} bit of the control register contains a "1" and the (n+1)th bit contains a "0", then a strobe is generated causing the (n+1)th data register to read the contents of the n^{th} data register, simultaneously setting the (n+1)th control register bit and clearing the n^{th} control register bit, so that the control flag moves with the data. In this fashion data in the data register moves down the stack of data registers toward the output as long as there are "empty" locations ahead of it. The fall through operation stops when the data reaches a register n with a "1" in the (n+1)th control register bit, or the end of the register.

Data is initially loaded from the data inputs by applying a LOW-to-HIGH transition on the parallel load (PL) input. A "1" is placed in the first control register bit simultaneously. The first control register bit is returned buffered, to the input ready (IR) output, and this pin goes inactive indicating that data has been entered into the first data register and the input is now "busy", unable to accept more data. When PL next goes LOW, the fall-through process begins (assuming that at least the second location is empty). The data in the first register is copied into the second, and the first control register bit is cleared. This causes IR to go active, indicating the inputs are available for another data word.

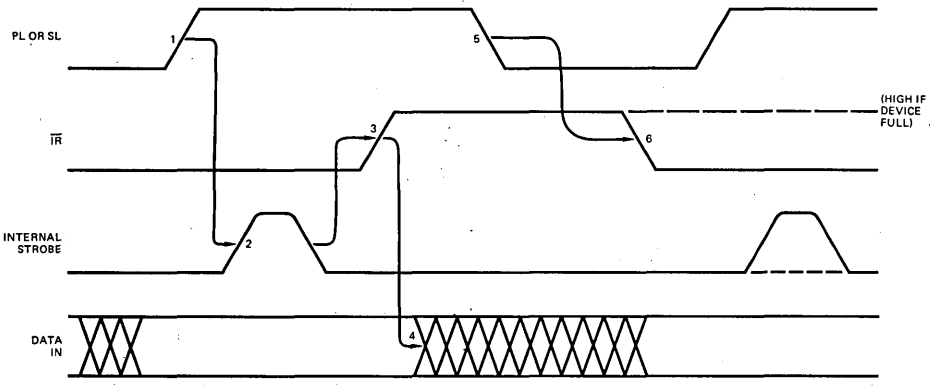
The data falling through the register stacks up at the output end. At the output the last control register bit is buffered and brought out as Output Ready (OR). A HIGH on OR indicates there is a "1" in the last control register bit and therefore there is valid data on the data outputs. A parallel dump command is used to shift the data word out of the FIFO. A LOW-to-HIGH transition on PD clears the last register bit, causing OR to go LOW, indicating that the data on the outputs may no longer be valid. When PD goes LOW, the "0" which is now present at the last control register bit allows the data in the next to the last register to move into the last register position and on to the outputs. The "0" in the control register then "bubbles" back toward the input as the data shifts toward the output.

If the memory is emptied by reading out all the data, then when the last word is being read out and PD goes HIGH, OR will go LOW as before, but when PD next goes LOW, there is no data to move into the last location, so OR remains LOW until more data arrives at the output. Similarly, when the memory is full data written into the first location will not shift into the second when PL goes LOW, and IR will remain inactive instead of returning to an active state.

The pairs of input and output control signals are designed so that the PD input of one FIFO can be driven by the IR output of another, and the OR output of the first FIFO can drive the PL input of the second, allowing simple expansion of the FIFO to any depth. Wider buffers are formed by allowing parallel rows of FIFOs to operate together, as shown in the application on the last page.

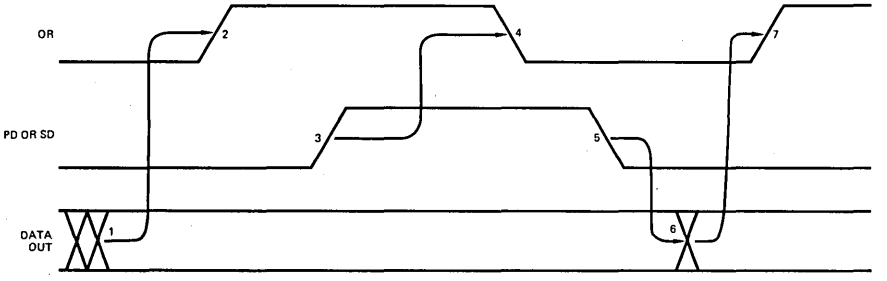
Because the input ready signal is active LOW on the Am2812 a peculiarity occurs when several devices are placed end-to-end. When the second unit of two Am2812's fills up, the data out of the first is not dumped immediately. That is, no shift out command occurs, so that the data last written into the second device remains on the output of the first until an empty location bubbles up from the output. The net effect is that n Am2812s connected end-to-end store 31n+1 words (instead of 32n). The Am2813 stores 32n words in this configuration, because IR is active HIGH and does dump the last word written into the second device.

Am2812 TIMING DIAGRAM



Am2812 INPUT TIMING

When data is steady PL is brought HIGH (1) causing internal data strobe to be generated (2). When data has been loaded, $\overline{IR}$ goes HIGH (3) and data may be changed (4). $\overline{IR}$ remains HIGH until PL is brought LOW (5); then $\overline{IR}$ goes LOW (6) indicating new data may be entered.



Am2812 OUTPUT TIMING

When data out is steady (1), OR goes HIGH (2). When PD goes HIGH (3), OR goes LOW (4). When PD goes LOW again (5), the output data changes (6) and OR returns HIGH (7).

The input and output timing diagrams above illustrate the sequence of control on the Am2812. Note that PL matches OR and $\overline{IR}$ matches PD in time, as though the signals were driving each other. The Am2813 pattern is similiar, but IR is active HIGH instead of active LOW (shown in timing diagram on next page).

FLAG OUTPUT

A flag output is available on the Am2812 and Am2813 to indicate whether the FIFO is more or less than half full. The flag signal is generated by summing the "1s" in the control flip-flops, and therefore is not affected by the movement of data through the register. The flag signal goes HIGH when the 13th, 14th, 15th, or 16th word is loaded into the FIFO. It will remain HIGH until there are less than $15^{+1}/_{-2}$ words in the memory. It is always HIGH if there are more than 16 words in the FIFO.

RESET

An over-riding master reset ($\overline{MR}$) is used to clear all control register bits and set all the outputs LOW.

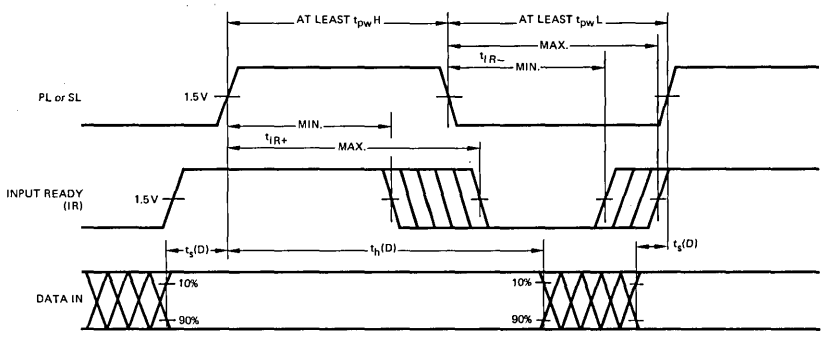
SERIAL INPUT AND OUTPUT (Am2812 ONLY)

The Am2812 also has the ability to read or write serial bit streams, rather than 8-bit words. The device then works like a 256 by 1-bit FIFO. A serial data stream can be loaded into the device by using the serial load input and applying data to D_0 input. Inputs D_1–D_7 must be grounded. The SL signal operates just like the PL input, causing IR to go HIGH and LOW as the bits are entered. The data is simply shifted across the 8-bit input register until 8 bits have been entered; the 8 bits then fall through the register as though they had been loaded in parallel. Following the 8th SL pulse, IR will remain inactive if the FIFO is full.

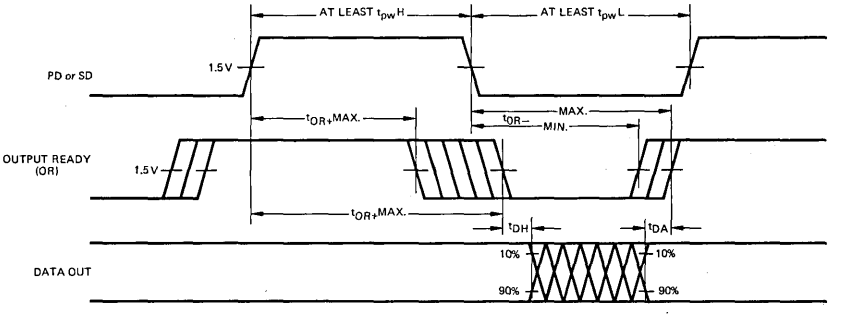
A corresponding operation occurs on the output, with clock pulses on SD causing successive bits of data to appear on the O_7 output. OR moves HIGH and LOW with SD exactly as it does with PD. When 8 bits have been shifted out, the next word appears at the output. If a PD command is applied after the 8 bits on the outputs have been partially shifted out, the remainder of the word is dumped and a new 8-bit word is brought to the output. OR will stay LOW if the FIFO is empty.

When the serial input or output clock is used, the corresponding parallel control line should be grounded and when the PD or PL controls are used the corresponding serial clocks should be grounded.

TIMING DIAGRAM



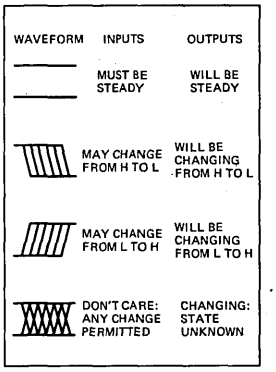
Note: IR inverted on Am2812.



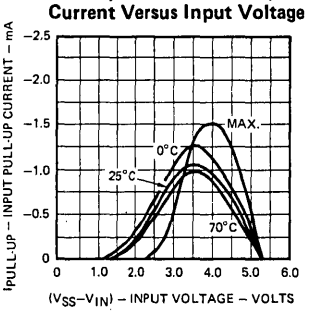
USER NOTES

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on PD, the OR signal always goes LOW before there is any change in output data and always stays LOW until after the new data has appeared on the outputs, so anytime OR is HIGH, there is good, stable data on the outputs.
3. If PD is held HIGH while the memory is empty and a word is written into the input, then that word will fall through the memory to the output. OR will go HIGH for one internal cycle (at least t_{OR+}) and then will go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until PD has been brought LOW.
4. When the master reset is brought LOW, the control register and the outputs are cleared. $\overline{IR}$ goes HIGH and OR goes LOW. If PL is HIGH when the master reset goes HIGH then the data on the inputs will be written into the memory and $\overline{IR}$ will return to the LOW state until PL is brought LOW. If PL is LOW when the master reset is ended, then $\overline{IR}$ will go HIGH but the data on the inputs will not enter the memory until PL goes HIGH.
5. The output enable pin inhibits dump commands while it is LOW and forces the Q outputs to a high impedance state.
6. The serial load and dump lines should not be used for interconnecting two FIFOs. Use the parallel interconnection instead.
7. If less than eight bits have been shifted in using the serial load command, a parallel load pulse will destroy the data in the partially filled input register.

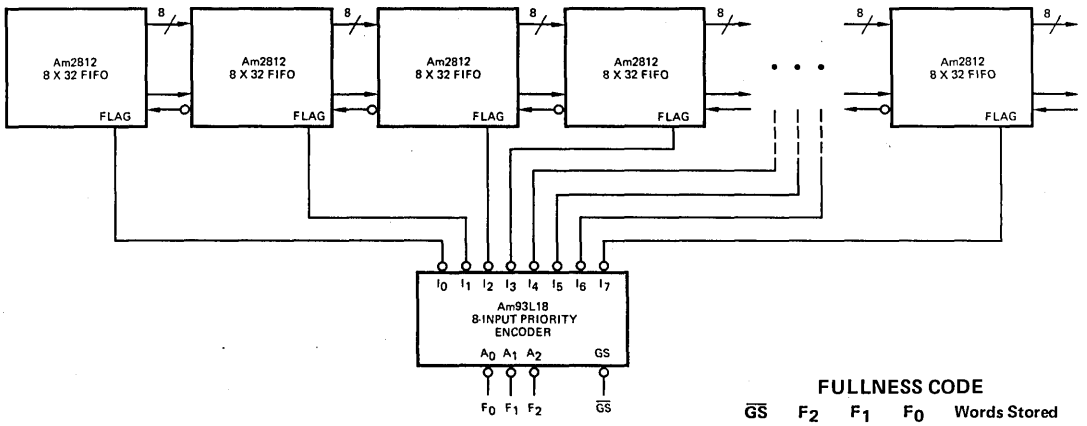
KEY TO TIMING DIAGRAM



Pull-up Characteristic Input Current Versus Input Voltage



APPLICATIONS



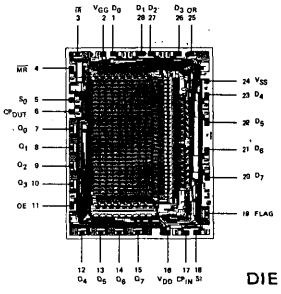
FULLNESS CODE

$\overline{GS}$	F_2	F_1	F_0	Words Stored
L	L	L	L	0 - 15
L	L	L	H	13 - 47
L	L	H	L	45 - 78
L	L	H	H	76 - 109
L	H	L	L	107 - 140
L	H	L	H	138 - 171
L	H	H	L	169 - 202
L	H	H	H	200 - 233
H	H	H	H	231 - 249

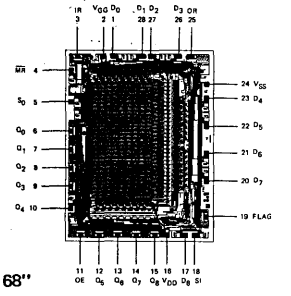
The Fullness Flags from Am2812 or Am2813 FIFOs can be encoded by an Am93L18 8-input priority encoder. The output code F_0-F_2 indicates the weight of the highest priority input which is LOW. GS is group signal; it is HIGH if all the inputs are HIGH.

Metallization and Pad Layouts

Am2812



Am2813



DIE SIZE .128" X 0.168"

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MICRO
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TWX: 910-339-9280
TELEX: 34-6306

Am3114/Am2814
Dual 128-Bit Static Shift Register

Distinctive Characteristics

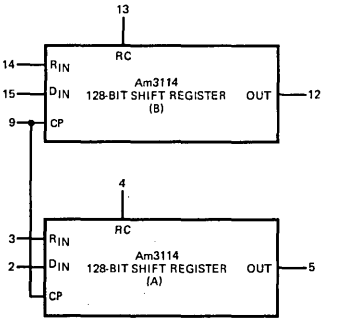
- 2nd Source to Texas Instruments 3114
- Operation guaranteed from DC to 2MHz
- 100% reliability assurance testing in compliance with MIL-STD-883
- Full military grade devices available

FUNCTIONAL DESCRIPTION

The Am3114 is a dual 128-bit static shift register built using P-channel silicon gate MOS technology. The two registers each have a two-input multiplexer on their inputs, so that input data may be selected from one of two sources. Both registers have a common clock input, and operate with a low-voltage TTL clock signal. The registers shift on the LOW-to-HIGH edge of the clock signal. Data at the inputs must be steady for a set-up time before and a hold time after this clock transition. Since data storage is static, the clock may be halted indefinitely in the HIGH state. The outputs of each register can drive one TTL load or three Am93L low-power TTL loads.

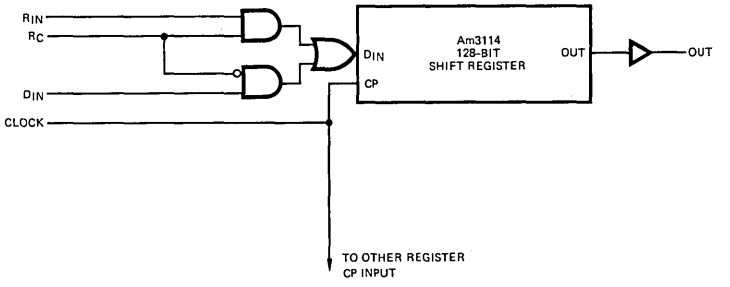
The two-input multiplexer on the input of each register is controlled by the RC (recirculate control) input. When RC is LOW, data is accepted on the D_{in} input; when RC is HIGH, data is accepted on the R_{in} input. The Am2814 is functionally identical to the Am3114, but is specified with higher performance.

LOGIC SYMBOL



V_{SS} = Pin 7
V_{DD} = Pin 6
V_{GG} = Pin 11

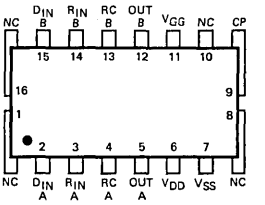
LOGIC BLOCK DIAGRAM (One Register Shown)



ORDERING INFORMATION

Package Type	Temperature Range	Am3114 Order Number	Am2814 Order Number
Molded DIP	−25°C to +85°C	TMS3114NC	AM2814PC
Hermetic DIP	−25°C to +85°C	TMS3114JC	AM2814DC
Hermetic DIP	−55°C to +125°C		AM2814DM

CONNECTION DIAGRAM



Notes: 1. Pin 1 is marked for orientation.
2. NC = No Connection.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{DD} Supply Voltage	V_{SS} −10V to V_{SS} +0.3V
V_{GG} Supply Voltage	V_{SS} −20V to V_{SS} +0.3V
DC Input Voltage	V_{SS} −15V to V_{SS} +0.3V

OPERATING RANGE

Part Number	T_A	V_{SS}	V_{GG}	V_{DD}
Am2814PC, DC Am3114JC, NC	−25°C to +85°C	5.0V ±5%	−11V to −13V	GND
Am2814DM	−55°C to +125°C	5.0V ±5%	−11.4V to −12.6V	GND

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −200μA		V_{SS}−1			Volts
V_{OH}	Output LOW Voltage	I_{OL} = 1.6mA			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	Am3114	3.5			Volts
			Am2814	V_{SS} −1.5			
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.6	Volts
I_{IL}	Input LOW Current	V_{SS} = MAX., V_{IN} = 0.6V				0.5	μA
I_{IH}	Input HIGH Current	V_{IN} = V_{SS}				0.5	μA
I_{SS}	V_{SS} Power Supply Current	Inputs and Outputs Open f = 1MHz	Am3114		15		mA
			Am2814XC		14	25	
			Am2814XM		14	35	
I_{GG}	V_{GG} Power Supply Current	Inputs and Outputs Open f = 1MHz	Am3114		−4		
			Am2814XC		−4	−10	
			Am2814XM		−4	−15	

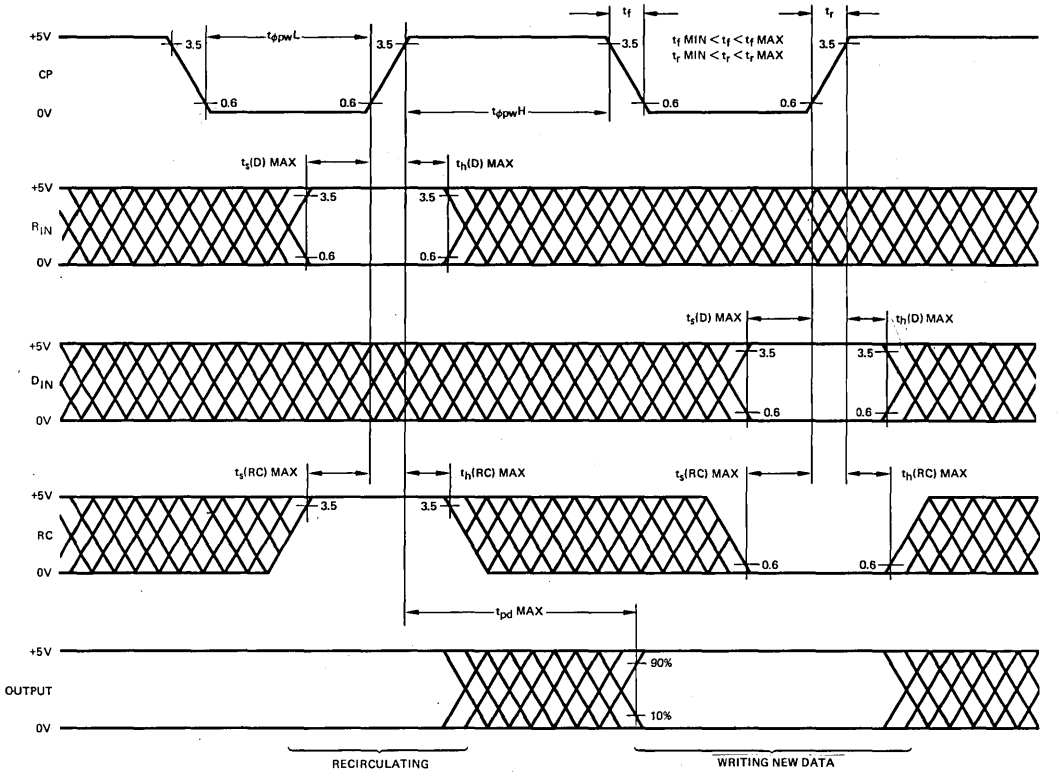
Note 1. Typical Limits are at V_{SS} = 5.0V, V_{GG} = −12V, 25°C ambient and maximum loading.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

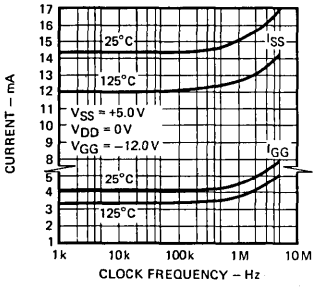
Parameters	Description	Test Conditions	Am3114 Min.	Am3114 Typ.	Am3114 Max.	Am2814 Min.	Am2814 Typ.	Am2814 Max.	Units
f_{max}	Maximum Clock Frequency		2.0			2.5			MHz
$t_{\phi pw}H$	Clock HIGH Time		.330		∞	.200		∞	μs
$t_{\phi pw}L$	Clock LOW Time		.130			.170		100	μs
t_r, t_f	Clock Rise and Fall Times				5			5	μs
t_s(D)	Set-up Time, D or R Inputs (see definitions)	t_r = t_f ≤ 50ns			100			100	ns
t_h(D)	Hold Time, D or R Inputs (see definitions)				100			100	ns
t_s(RC)	Set-up Time, RC Input (see definitions)				100			100	ns
t_h(RC)	Hold Time, RC Input (see definitions)				150			150	ns
t_{pd}	Delay, Clock to Output LOW or HIGH	R_L = 2.7k, C_L = 20pF			350	(Note 4)		250	ns
t_{pr}, t_{pF}	Output Rise and Fall Times	10% to 90%						100	ns
C_{in}	Capacitance, Any Input (Note 3)	f = 1MHz, V_{IN} = V_{SS}			13		3	7	pF

Notes: 3. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.
4. At any temperature, t_{pd} min. is always much greater than t_h(D) max.

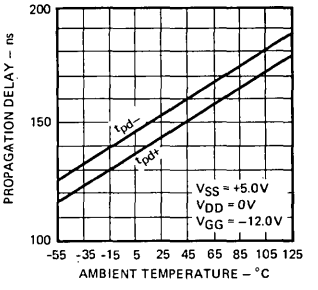
TIMING DIAGRAM



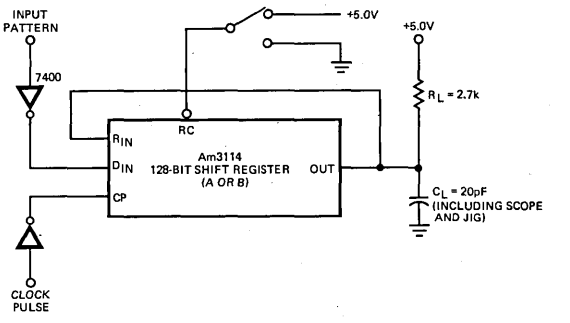
Typical Power-Supply Currents Versus Frequency



Typical Propagation Delay Versus Ambient Temperature



TEST CIRCUIT

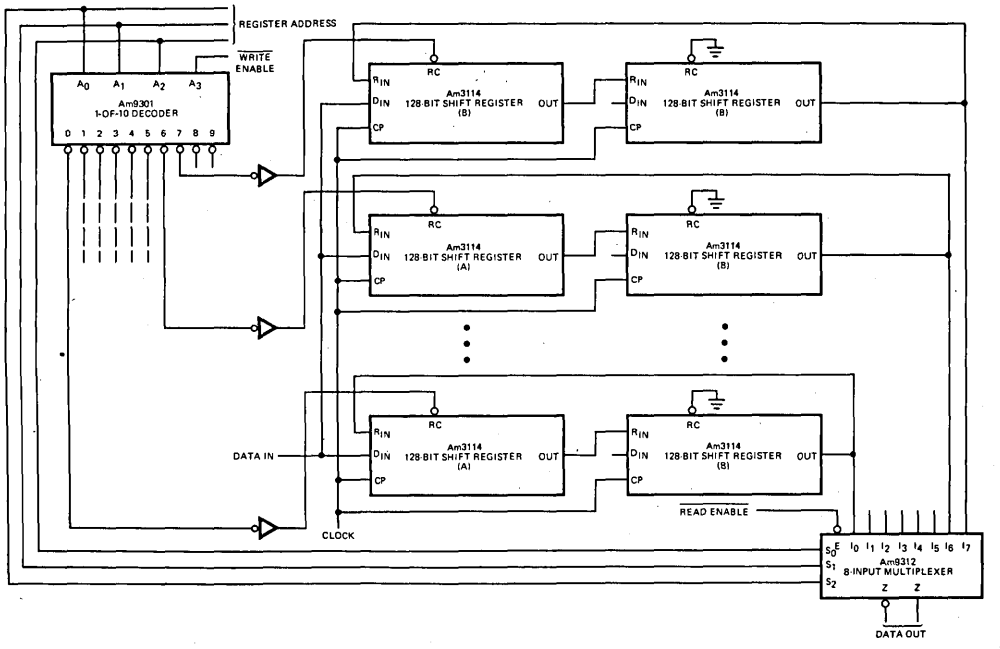


DEFINITION OF TERMS

STATIC SHIFT REGISTER A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is LOW and is transferred to the static slaves while the clock is HIGH. The clock may be stopped indefinitely in the HIGH state, but there are limitations on the time it may reside in the LOW state.

SET-UP and HOLD TIMES The shift register will accept the data that is present on its input around the time the clock goes from LOW-to-HIGH. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

APPLICATIONS



Eight Register 256-Bit Memory System

Data enters one of the eight 256-bit registers when the write enable input to the decoder is LOW. The addressed register will accept the data on the data input; the other seven registers will recirculate their data. Outputs are driven directly into an Am9312 8-input multiplexer. Obviously, the read and write registers need not be the same. Pull-up resistors are required on all register inputs driven from TTL.

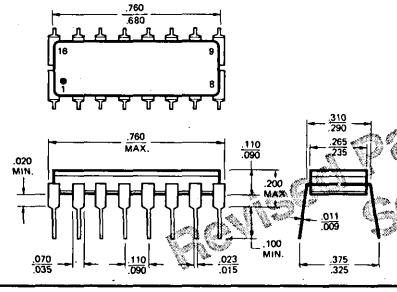
TRUTH TABLE

RC	D_{IN}	R_{IN}	Data Entered
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

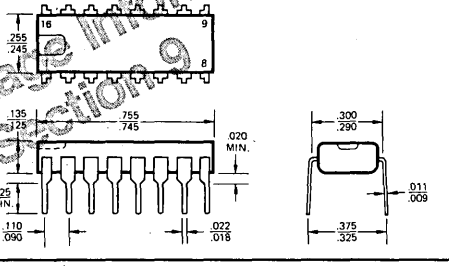
H = HIGH Voltage level
L = LOW Voltage Level
X = Don't Care

PHYSICAL DIMENSIONS
Dual-In-Line

Side Brazed



Molded



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TELEX: 34-6306

Am3341/2841

64 x 4 Bits First-In First-Out Memories

Distinctive Characteristics

- "Plug In" replacement for Fairchild 3341
- Asynchronous buffer for up to 64 four-bit words
- Easily expandable to larger buffers
- Am2841 has 1 MHz guaranteed data rate
- 100% reliability assurance testing in compliance with MIL-STD-883
- Special input circuit provides true TTL compatibility

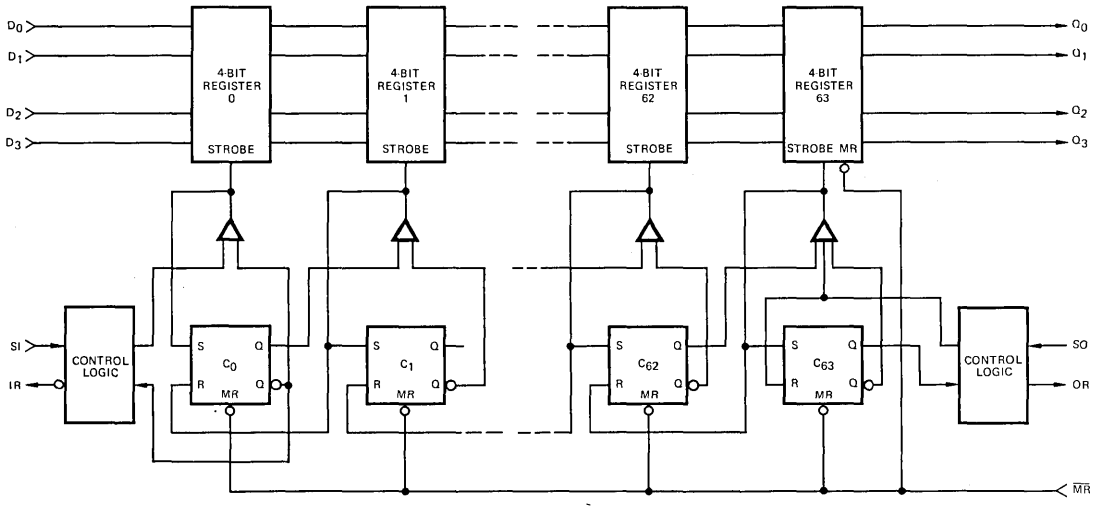
FUNCTIONAL DESCRIPTION

The Am3341/Am2841 is an asynchronous first-in first-out memory stack, organized as 64 four-bit words. The device accepts a four-bit parallel word D_0–D_3 under control of the shift in (SI) input. Data entered into the FIFO immediately ripples through the device to the outputs Q_0–Q_3. Up to 64 words may be entered before any words are read from the memory. The stored words line up at the output end in the order in which they were written. A read command on the shift out input (SO) causes the next to the last word of data to move to the output and all data shifts one place down the stack. Input ready (IR) and output ready (OR) signals act as memory full and memory empty flags and also provide the necessary pulses for interconnecting FIFOs to obtain deeper stacks.

Parallel expansion to wider words only requires that rows of FIFOs be placed side by side.

Reading and writing operations are completely independent, so the device can be used as a buffer between two digital machines operating asynchronously and at widely differing clock rates. Special input circuits are provided on all inputs to pull the input signals up to an MOS V_{IH} when a TTL V_{OH} is reached, providing true TTL compatibility without the inconvenience and extra power drain of external pull-up resistors. A detailed description of the operation is on pages 4 and 5 of this data sheet. The Am2841 is functionally identical to the Am3341, but is a higher performance device.

LOGIC BLOCK DIAGRAM

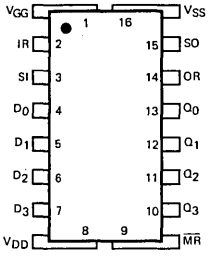


ORDERING INFORMATION

Package Type	Temperature Range	Am3341 Order Number	Am2841 Order Number
Hermetic DIP	0°C to +75°C	Am3341DC	Am2841DC
Hermetic DIP	−55°C to +125°C		Am2841DM
Dice	Note	Am3341XX	Am2841XX

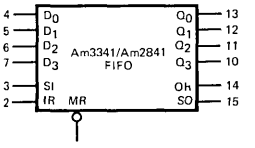
Note:
The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View



Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{SS} = Pin 16
V_{GG} = Pin 1
V_{DD} = GND = Pin 8

MAXIMUM RATING (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{DD} Supply Voltage	V_{SS} −7V to V_{SS} +0.3V
V_{GG} Supply Voltage	V_{SS} −20V to V_{SS} +0.3V
DC Input Voltage	V_{SS} −10V to V_{SS} +0.3V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am2841XM T_A = −55°C to +125°C
Am3341XC, Am2841XC T_A = 0°C to +70°C
V_{GG} = −12V ±5% V_{SS} = 5.0V ±5% V_{DD} = 0V

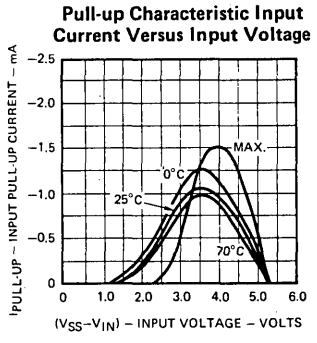
Parameters	Description	Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = .300mA		V_{SS} −1.0			V
V_{OL}	Output LOW Voltage	I_{OL} = 1.6mA				0.4	V
V_{IH}	Input HIGH Level			V_{SS} −1.0			V
V_{IL}	Input LOW Level					0.8	V
I_{IL}	Input Leakage Current	V_{IN} = 0V				1.0	μA
I_{IH}	Input HIGH Current	V_{IN} = V_{SS} −1.0V		250			μA
V_{PUP}	Input Pull-up Initiation Voltage	(Note 2)	V_{SS} = MIN.			2.0	V
			V_{SS} = MAX.			2.2	V
V_{BAR}	Voltage at Peak Input Current	(Note 2)				V_{SS} −1.5	V
I_{BAR}	Maximum Input Current	(Note 2)				1.6	mA
I_{GG}	V_{GG} Current	T_A = 0°C to +70°C			7	12	mA
		T_A = −55°C to +125°C				16	
I_{DD}	V_{DD} Current	T_A = 0°C to +70°C			30	45	mA
		T_A = −55°C to +125°C				60	

Notes: 1. Typical limits are at V_{SS} = 5.0V, V_{GG} = −12.0V, T_A = 25°C
2. See graph of input V-I characteristics.

Switching Characteristics

Parameters	Definition	Test Conditions	Am3341 Min.	Am3341 Typ.	Am3341 Max.	Am2841 Min.	Am2841 Typ.	Am2841 Max.	Units
t_{IR+}	Delay, SI HIGH to IR LOW		70	250	550	50		400	ns
t_{IR-}	Delay, SI LOW to IR HIGH		138	275	550	100		550	ns
t_{0V+}	Minimum Time SI and IR both HIGH				100			80	ns
t_{0V-}	Minimum Time SI and IR both LOW				100			80	ns
t_{DSI}	Data Release Time				400			200	ns
t_{DD}	Data Set-up Time		25			0			ns
t_{OR+}	Delay, SO HIGH to OR LOW		90	250	500	70	200	450	ns
t_{OR-}	Delay, SO LOW to OR HIGH		170	350	850	70	200	550	ns
t_{PT}	Ripple through Time	FIFO Empty		10	32		8	16	μs
t_{DH}	Delay, OR LOW to Data Out	SO = LOW	75			75			ns
t_{MRW}	Minimum Reset Pulse Width				400			400	ns
t_{DA}	Delay, Data Out to OR HIGH	SO = HIGH	0	30		0	20		ns
CI	Input Capacitance (Except $\overline{MR}$)				7			7	pF
C_{MR}	Input Capacitance $\overline{MR}$				15			7	pF

Note: Switching times over the entire temperature range are such that two devices at approximately the same ambient temperature can drive each other.



DESCRIPTION OF THE Am3341 FIFO OPERATION

The Am3341 FIFO consists internally of 64 four-bit data registers and one 64-bit control register, as shown in the logic block diagram. A "1" in a bit of the control register indicates that a four-bit data word is stored in the corresponding data register. A "0" in a bit of the control register indicates that the corresponding data register does not contain valid data. The control register directs the movement of data through the data registers. Whenever the n^{th} bit of the control register contains a "1" and the (n+1)th bit contains a "0", then a strobe is generated causing the (n+1)th data register to read the contents of the n^{th} data register, simultaneously setting the (n+1)th control register bit and clearing the n^{th} control register bit, so that the control flag moves with the data. In this fashion data in the data register moves down the stack of data registers toward the output as long as there are "empty" locations ahead of it. The fall through operation stops when the data reaches a register n with a "1" in the (n+1)th control register bit, or the end of the register.

Data is initially loaded from the four data inputs D_0–D_3 by applying a LOW-to-HIGH transition on the shift in (SI) input. A "1" is placed in the first control register bit simultaneously. The first control register bit is returned, buffered, to the input ready (IR) output, and this pin goes LOW indicating that data has been entered into the first data register and the input is now "busy", unable to accept more data. When SI next goes LOW, the fall-through process begins (assuming that at least the second location is empty). The data in the first register is copied into the second, and the first control register bit is cleared. This causes IR to go HIGH, indicating the inputs are available for another data word.

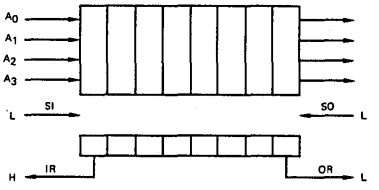
The data falling through the register stacks up at the output end. At the output the last control register bit is buffered and brought out as Output Ready (OR). A HIGH on OR indicates there is a "1" in the last control register bit and therefore there is valid data on the four data outputs Q_0–Q_3. An input signal, shift out (SO), is used to shift the data out of the FIFO. A LOW-to-HIGH transition on SO clears the last register bit, causing OR to go LOW, indicating that the data on the outputs may no longer be valid. When SO goes LOW, the "0" which is now present at the last control register bit allows the data in the next to the last register to move into the last register position and on to the outputs. The "0" in the control register then "bubbles" back toward the input as the data shifts toward the output.

If the memory is emptied by reading out all the data, then when the last word is being read out and SO goes HIGH, OR will go LOW as before, but when SO next goes LOW, there is no data to move into the last location, so OR remains LOW until more data arrives at the output. Similarly, when the memory is full data written into the first location will not shift into the second when SI goes LOW, and IR will remain LOW instead of returning to a HIGH state.

The pairs of input and output control signals are designed so that the SO input of one FIFO can be driven by the IR output of another, and the OR output of the first FIFO can drive the SI input of the second, allowing simple expansion of the FIFO to any depth. Wider buffers are formed by allowing parallel rows of FIFOs to operate together, as shown in the application on the last page.

An over-riding master reset ($\overline{MR}$) is used to reset all control register bits and remove the data from the output.

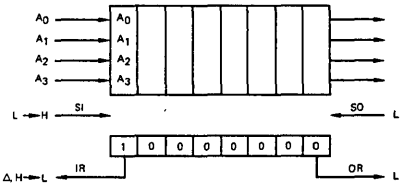
1



INITIAL CONDITION

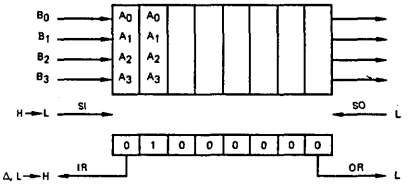
FIFO empty, SI LOW IR HIGH, word "A" on inputs.

2



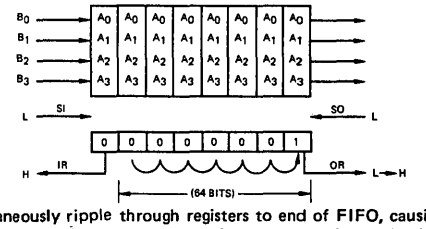
Write input into first stage by raising SI. (Δ = delay) IR goes LOW indicating data has been entered.

3



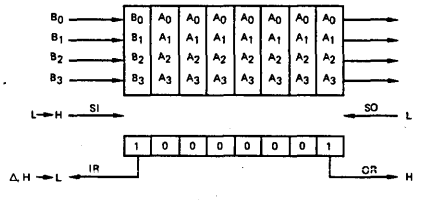
Release data into FIFO by lowering SI. After delay, data moves to second location, and IR goes HIGH indicating input available for new data word.

4



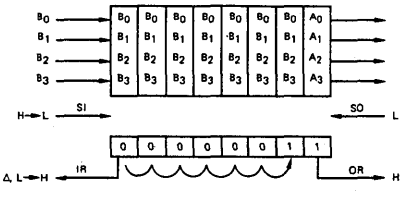
Data spontaneously ripple through registers to end of FIFO, causing OR to go HIGH. The time required for data to fall completely through the FIFO is the "Ripple-through Time".

5



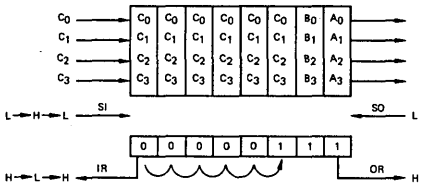
Word "B" written into FIFO

6



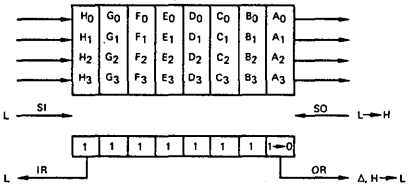
SI goes LOW allowing word "B" to fall through.

7



Word "C" written in same manner, and so on. When buffer is full, all control bits are 1's and IR stays LOW.

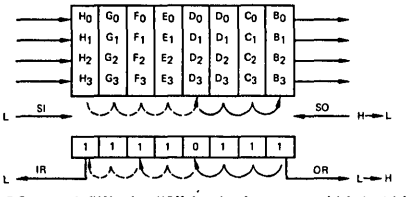
8



FIRST READ OPERATION

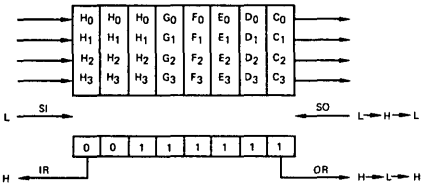
SO goes HIGH, indicating "Ready to Read". OR then goes LOW indicating "Data Read".

9



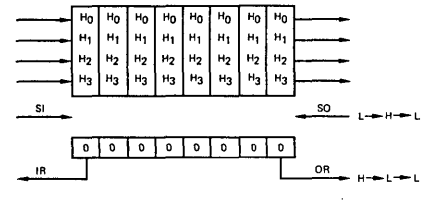
When SO goes LOW, the "0" in the last control bit bubbles toward the memory input. OR goes HIGH as the new word arrives at the output. IR goes HIGH when "0" reaches input.

10



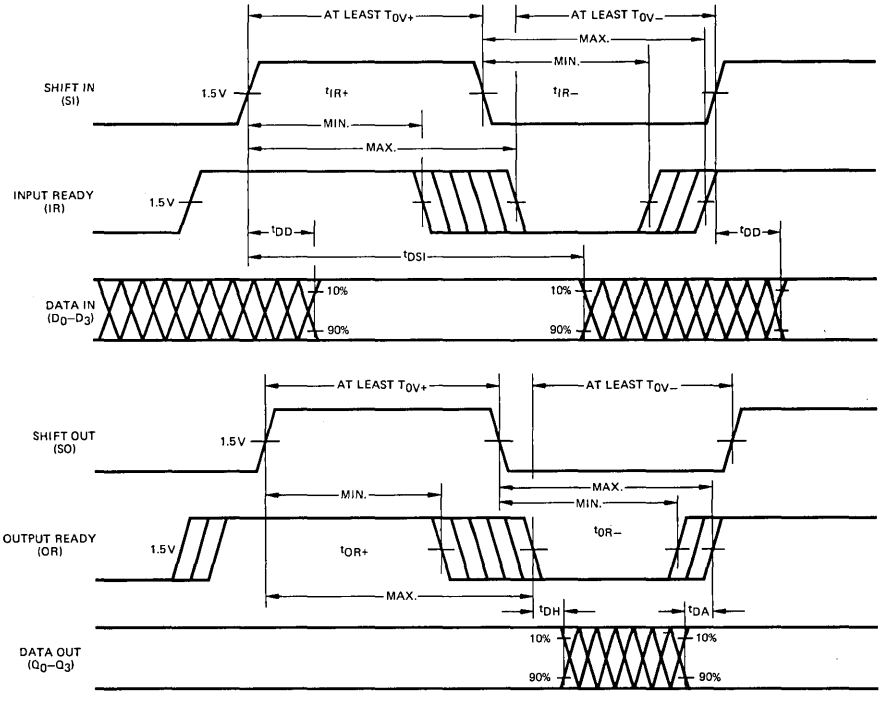
Read word "B" out, word "C" moves to output, and so on.

11



Read word "H". OR stays LOW because FIFO is empty. Word "H" remains in output until new word falls through.

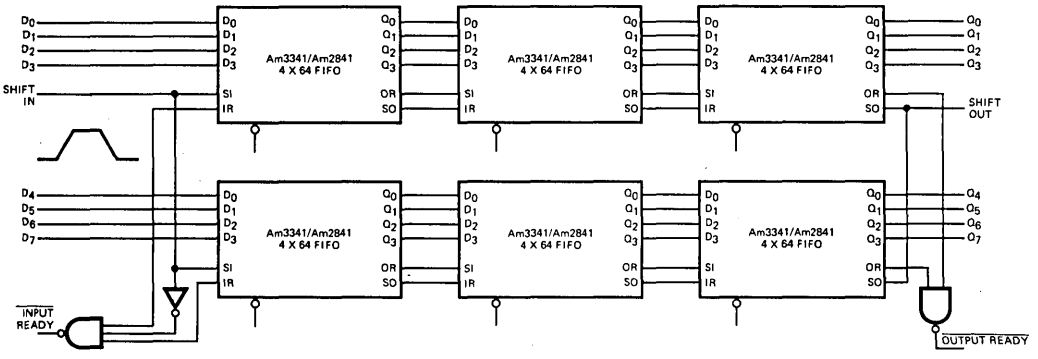
TIMING DIAGRAM



USER NOTES

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data and always stays LOW until after the new data has appeared on the outputs, so anytime OR is HIGH, there is good, stable data on the outputs.
3. If SO is held HIGH while the memory is empty and a word is written into the input, then that word will fall through the memory to the output. OR will go HIGH for one internal cycle (at least t_{OR+}) and then will go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
4. When the master reset is brought LOW, the control register and the outputs are cleared. IR goes HIGH and OR goes LOW. If SI is HIGH when the master reset goes HIGH then the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the master reset is ended, then IR will go HIGH, but the data on the inputs will not enter the memory until SI goes HIGH.

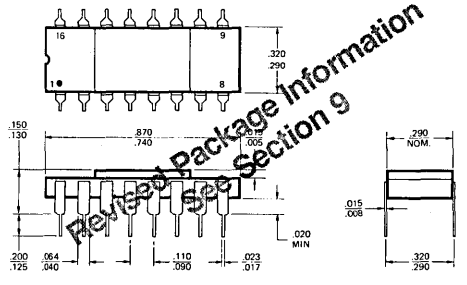
APPLICATIONS



The composite input ready indicates both devices are ready to receive data. The shift in pulse must be wide enough for all devices to load data under worst case conditions.

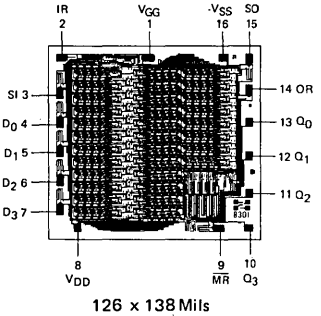
8 X 192 FIFO Buffer Using Am3341/Am2841

PHYSICAL DIMENSIONS
Dual-In-Line



Revised Package Information See Section 9

Metallization and Pad Layout



126 x 138 Mils

ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am4055/5055 • Am4056/5056 • Am4057/5057

Quad 128-Bit, Dual 256-Bit and Single 512-Bit Static Shift Registers

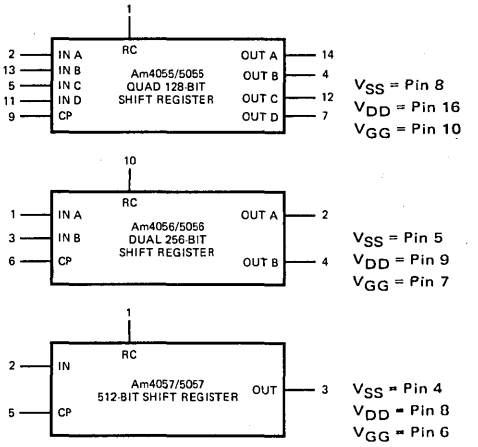
Distinctive Characteristics

- Internal recirculate
- Single TTL compatible clock
- Operation guaranteed from DC to 2.2MHz
- 100% reliability assurance testing in compliance with MIL-STD-883

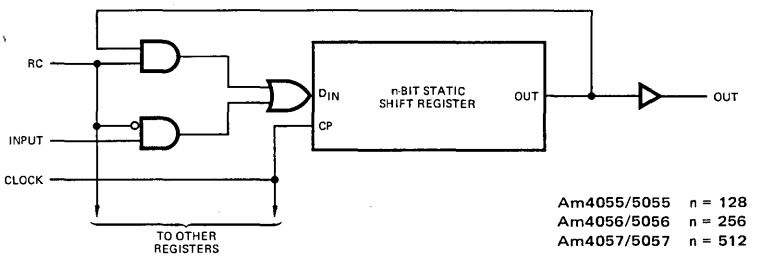
FUNCTIONAL DESCRIPTION

These devices are a family of static P-channel MOS shift registers in three configurations. The Am4055/5055 is a quad 128-bit register; the Am4056/5056 is a dual 256-bit register; and the Am4057/5057 is a single 512-bit register. All three devices include on chip recirculate. The registers are all clocked by a single low-level clock input. Because the registers are static, the clock may be stopped indefinitely in the LOW state without loss of data. Each of the registers has a single data input; data on the input is written into the register on the HIGH-to-LOW clock edge. A single recirculate control (RC) on each chip determines whether the registers on that chip are to write data in from the data inputs or recirculate the data appearing on the output. If RC is LOW, new data is written in; if RC is HIGH then the data on the output will be written back into the register input on the next clock pulse.

LOGIC SYMBOLS



LOGIC BLOCK DIAGRAM
(One Register Shown)

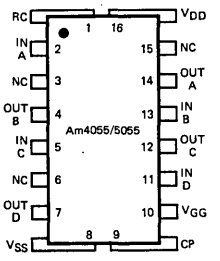


ORDERING INFORMATION

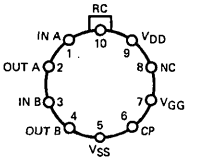
Package Type	Temperature Range	Order Number
16-Pin Molded DIP	0°C to +70°C	MM5055N
16-Pin Hermetic DIP	0°C to +70°C	MM5055D
16-Pin Hermetic DIP	−55°C to +125°C	MM4055D
TO-100 Can	0°C to +70°C	MM5056H
TO-100 Can	−55°C to +125°C	MM4056H
8-Pin Molded DIP	0°C to +70°C	MM5057N
8-Pin Hermetic DIP	0°C to +70°C	MM5057D
8-Pin Hermetic DIP	−55°C to +125°C	MM4057D

CONNECTION DIAGRAMS

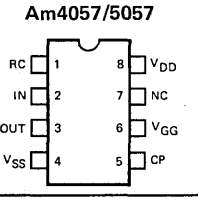
Am4055/5055



Am4056/5056



Am4057/5057



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +160°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{DD} Supply Voltage	V_{SS} −10V to V_{SS} +0.3V
V_{GG} Supply Voltage	V_{SS} −20V to V_{SS} +0.3V
DC Input Voltage	V_{SS} −20V to V_{SS} +0.3V

OPERATING RANGE

Part Number	Ambient Temperature	V_{SS}	V_{DD}	V_{GG}
Am4055 Am4056 Am4057	−55°C to +125°C	5.0V ±5%	0V	−12V ±5%
Am5055 Am5056 Am5057	0°C to +70°C	5.0V ±5%	0V	−12V ±5%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −0.5mA		2.4			Volts
V_{OL}	Output LOW Voltage	I_{OL} = 1.6mA				0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		V_{SS} −2.0		V_{SS} +0.3	Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		V_{SS} −18.5		V_{SS} −4.2	Volts
I_{IL}	Input Leakage Current	V_{IN} = −10.0V, all other pins GND, T_A = 25°C			0.01	0.5	µA
I_{DD}	V_{DD} Power Supply Current	T_A = 25°C, $t_{\phi pw}H$ = 160 ns Data = 1010. . . output open	f ≥ 1MHz		15.0	20.0	mA
			1MHz > f > 10kHz		13.0	18.0	
I_{GG}	V_{GG} Power Supply Current		f ≥ 1MHz		9.0	13.0	
			1MHz > f > 10kHz		6.5	9.0	

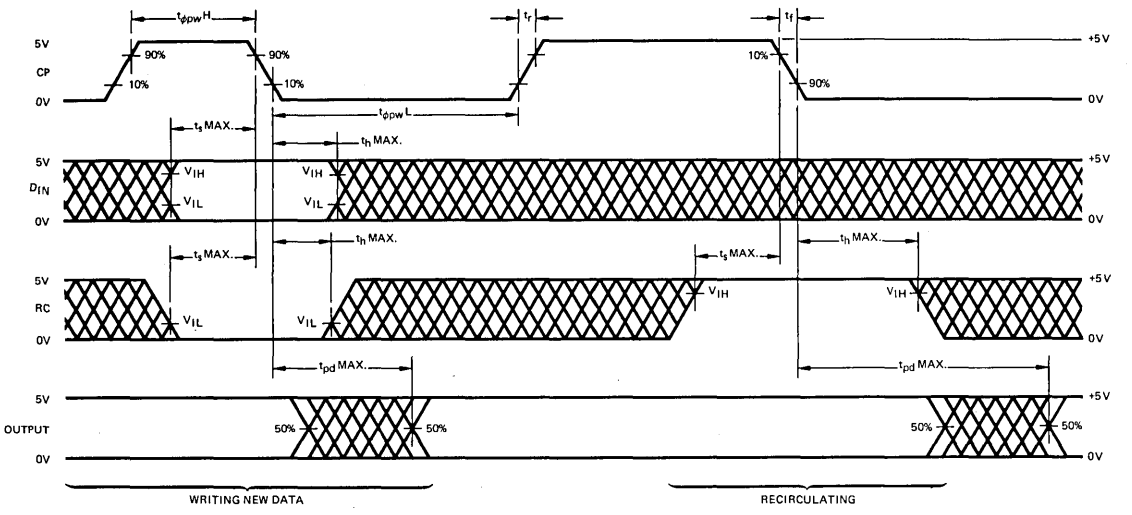
Note: 1. Typical Limits are at V_{SS} = 5.0V, V_{GG} = −12V, 25°C ambient and maximum loading.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
f	Clock Frequency		0		2.2	MHz
$t_{\phi pw}H$	Clock HIGH Time		0.16		10.0	µs
$t_{\phi pw}L$	Clock LOW Time		0.2		∞	µs
t_r, t_f	Clock Rise and Fall Times		10		200	ns
t_s	Set-up Time, D or RC Inputs (see definitions)	$t_r = t_f$ = 50ns			100	ns
t_h	Hold Time, D or RC Inputs (see definitions)	$t_r = t_f$ = 50ns			40	ns
t_{pd}	Delay, Clock to Output LOW or HIGH	R_L = 4k, C_L = 100pF	(Note 3)	250	350	ns
C_{in}	Capacitance, Data Clock and RC Inputs (Note 2)	f = 1MHz, V_{IN} = V_{SS}		3	7	pF
C_ϕ	Capacitance, Clock Input (Note 2)	f = 1MHz, V_{IN} = V_{SS}		3	7	pF

Notes: 2. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.
3. At any temperature, t_{pd} min. is always much greater than t_h(D) max.

TIMING DIAGRAM

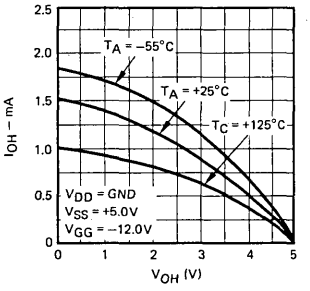


KEY TO TIMING DIAGRAM

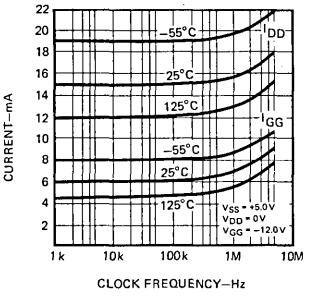
WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
▨	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
▨	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
▨	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN

PERFORMANCE CURVES

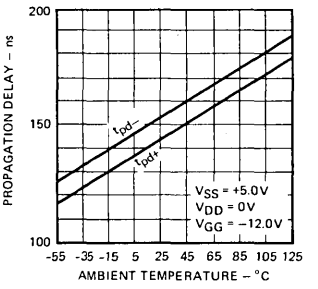
Typical Data Output HIGH Current Versus Data Output Voltage



Typical Power-Supply Currents Versus Frequency



Typical Propagation Delay Versus Ambient Temperature



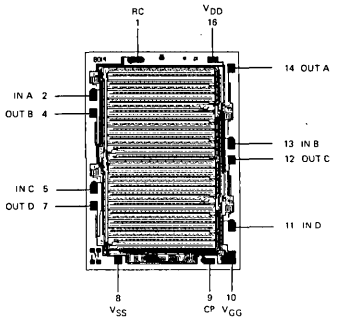
DEFINITION OF TERMS

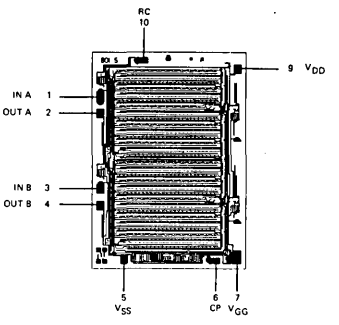
STATIC SHIFT REGISTER A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is HIGH and is transferred to the static slaves while the clock is LOW. The clock may be stopped indefinitely in the LOW state, but there are limitations on the time it may reside in the HIGH state.

SET-UP and HOLD TIMES The shift register will accept the data that is present on its input around the time the clock goes from HIGH-to-LOW. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

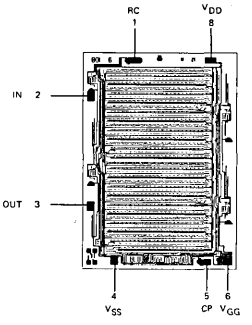
Metallization and Pad Layouts

4055/5055



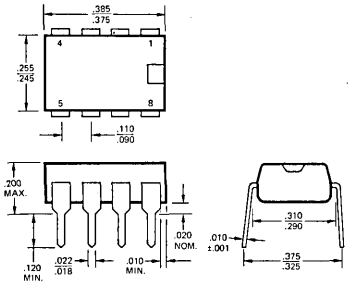


4057/5057



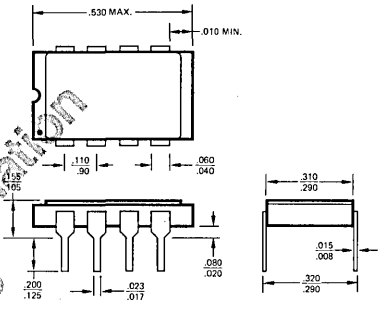
PHYSICAL DIMENSIONS

8-Pin Molded DIP

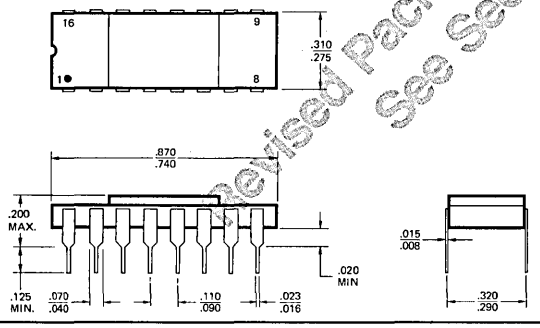


Top Views

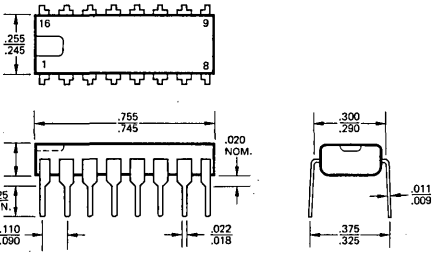
8-Pin Hermetic DIP



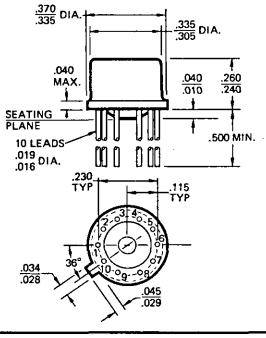
16-Pin Side Brazed DIP



16-Pin Molded DIP



TO-100 Can



ADVANCED
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TELEX: 34-6306

Am9102/Am9102A/Am9102B

1024-Bit Static N-Channel RAM

DISTINCTIVE CHARACTERISTICS

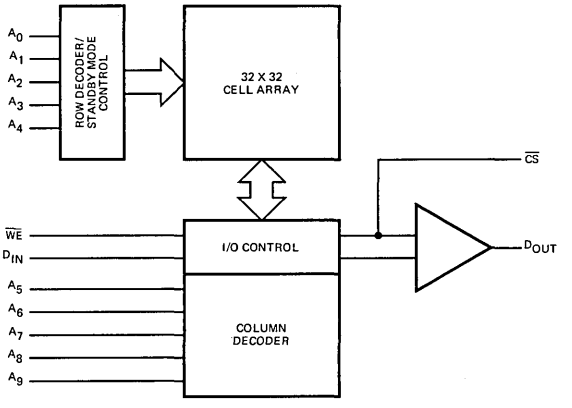
- High-Speed Operation
  Am9102 — 650 ns guaranteed read and write cycle times
  Am9102A — 500ns guaranteed read and write cycle times
  Am9102B — 400ns guaranteed read and write cycle times
- Low-Power Dissipation
  100 mw typical; 260 mw maximum
- Standby operating mode reduces power 75%
  16 mw typical; 64 mw maximum
- Input and output voltage levels identical to TTL
- High-Output Drive — Two full TTL loads guaranteed
- High Noise Immunity — 400 mV guaranteed
- Uniform Access Times
  Switching characteristics are insensitive to data patterns, addressing patterns, and power supply variations
- Single 5-Volt Power Supply
  10% tolerance for full temperature range devices
  5% tolerance for commercial range devices
- High-Performance Plug-In Replacement for: Intel 2102, Signetics 2602, Intersil IM7552, Mostek 4102, TI4033/4
- Available for operation over both commercial and military ranges
- 100% reliability assurance testing in accordance with MIL-STD-883

FUNCTIONAL DESCRIPTION

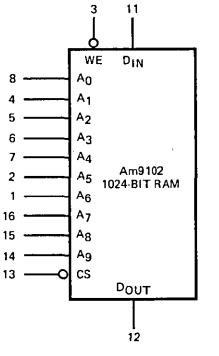
The Am9102 is a high-performance 1024-bit static N-channel random access memory, with a power-saving standby operating mode. The device has a chip select input ($\overline{CS}$) which controls a three-state output to make construction of large memory systems simple. Reading and writing are performed by enabling the chip and applying a LOW to write or a HIGH to read on the write enable input ($\overline{WE}$) while V_{CC} is at 5 volts. When a device is not being accessed for reading or writing, the standby mode may be entered by lowering V_{CC} to 1.6 volts. Stored data will be retained in the standby mode, but the power dissipation of the device will be reduced to about one quarter the normal operating power.

The devices are available in three speed selections. The Am9102 operates with a 650 ns cycle time, the Am9102A operates with a 500 ns cycle time, and the Am9102B requires only a 400 ns cycle time. The Am9102 and 9102A can directly replace the 2102-2 and 2102-1 to achieve higher drive and better noise immunity.

LOGIC BLOCK DIAGRAM



LOGIC SYMBOL

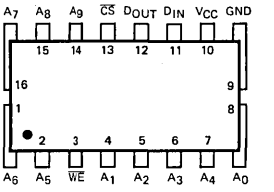


V_{CC} = Pin 10
GND = Pin 9

ORDERING INFORMATION

Package Type	Ambient Temperature	9102 Order Number	9102A Order Number	9102B Order Number
Molded DIP	0°C to +70°C	AM9102PC	AM9102APC	AM9102BPC
Hermetic DIP	0°C to +70°C	AM9102DC	AM9102ADC	AM9102BDC
Hermetic DIP	−55°C to +125°C	AM9102DM		

CONNECTION DIAGRAM
Top View



Note: Pin 1 marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 10 to Pin 9) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs	−0.5V to +7V
DC Input Voltage	−0.5V to +7V
Current into Output	50mA
Current from Output	−50mA

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Am9102PC, Am9102DC
Am9102APC, Am9102ADC $T_A = 0°C$ to $+70°C$ $V_{CC} = +5.0V \pm 5\%$
Am9102BPC, Am9102BDC

Parameters	Description	Test Conditions		Min.	Typ.(Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -200\mu A$		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN. I_{OL} = 3.2mA				0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0		V_{CC}	Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		−0.5		0.8	Volts
I_{IL}	Input Load Current	V_{CC} = MAX., V_{IN} = 0V to 5.25V				10	μA
I_{CC}	Power Supply Current	All inputs=V_{CC} Data out open V_{CC} = MAX.	$T_A = 25°C$		20	45	mA
			$T_A = 0°C$ to $+70°C$			50	
I_{CEX}	Output Leakage Current	$V_{\overline{CS}} = V_{IH}$	$V_{OUT} = V_{CC}$			10	μA
			$V_{OUT} = 0.4V$			−10	

Note 1. Typical limits are at $V_{CC} = 5.0V$ and $T_A = 25°C$

Am9102DM $T_A = -55°C$ to $+125°C$ $V_{CC} = +5.0V \pm 10\%$

Parameters	Description	Test Conditions		Min.	Typ.(Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	$I_{OH} = -200\mu A$	V_{CC} = 4.75V	2.4			Volts
			V_{CC} = 4.50V	2.2			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 3.2mA				0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0		V_{CC}	Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		−0.5		0.8	Volts
I_{IL}	Input Load Current	V_{CC} = MAX., V_{IN} = 0V to 5.25V				10	μA
I_{CC}	Power Supply Current	All inputs=V_{CC} Data out open V_{CC} = MAX.	$T_A = 25°C$		20	45	mA
			$T_A = -55°C$ to $+125°C$			55	
I_{CEX}	Output Leakage Current	$V_{\overline{CS}} = V_{IH}$	$V_{OUT} = V_{CC}$			10	μA
			$V_{OUT} = 0.4V$			−10	

Note 1. Typical limits are at $V_{CC} = 5.0V$ and $T_A = 25°C$

CAPACITANCE ($T_A = 25°C$)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance, Any Input	$V_{IN} = 0V$, f = 1MHz		3	5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$, f = 1MHz		7	10	pF

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE AND VOLTAGE RANGE

Load = 1 TTL Gate and 100 pF

Am9102B (400 ns Cycle Time)

Parameters	Description	Test Conditions	Min.	Typ.(Note 1)	Max.	Units
t_{CE}	Delay Chip Select LOW to Output HIGH or LOW	V_{IL} = 0.65V V_{IH} = 2.2V $t_r = t_f$ = 20ns Measure at 1.5V	0		200	ns
t_{CD}	Delay Chip Select HIGH to Output OFF		0		150	ns
t_{pd+}(A)	Delay Address to Output HIGH		50		400	ns
t_{pd-}(A)	Delay Address to Output LOW		50		400	ns
$t_{pw}(\overline{WE})$	Minimum Write Pulse Width				250	ns
t_s(D)	Data Set-up Time				150	ns
t_h(D)	Data Hold Time				100	ns
t_s(A)	Address Set-up Time				100	ns
t_h(A)	Address Hold Time				50	ns
$t_s(\overline{CS})$	Chip Select Set-up Time				250	ns
$t_h(\overline{CS})$	Chip Select Hold Time				50	ns
T_{CYCLE}	Read or Write Cycle Time		400			ns

Am9102A (500 ns Cycle Time)

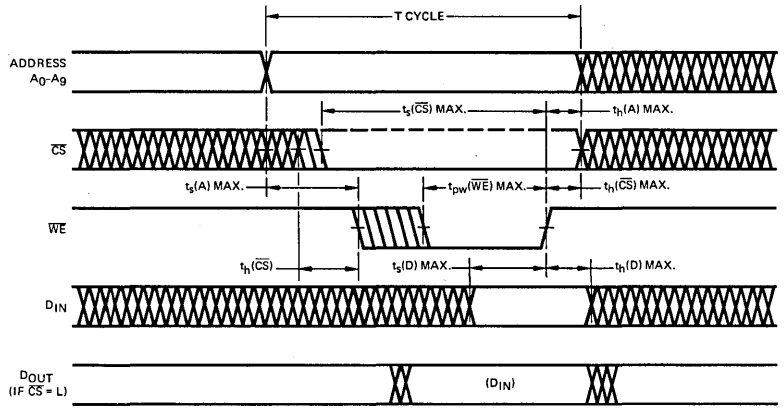
Parameters	Description	Test Conditions	Min.	Typ.(Note 1)	Max.	Units
t_{CE}	Delay Chip Select LOW to Output HIGH or LOW	V_{IL} = 0.65V V_{IH} = 2.2V $t_r = t_f$ = 20ns Measure at 1.5V	0		200	ns
t_{CD}	Delay Chip Select HIGH to Output OFF		0		150	ns
t_{pd+}(A)	Delay Address to Output HIGH		50		500	ns
t_{pd-}(A)	Delay Address to Output LOW		50		500	ns
$t_{pw}(\overline{WE})$	Minimum Write Pulse Width				300	ns
t_s(D)	Data Set-up Time				200	ns
t_h(D)	Data Hold Time				100	ns
t_s(A)	Address Set-up Time				150	ns
t_h(A)	Address Hold Time				50	ns
$t_s(\overline{CS})$	Chip Select Set-up Time				300	ns
$t_h(\overline{CS})$	Chip Select Hold Time				50	ns
T_{CYCLE}	Read or Write Cycle Time		500			ns

Am9102 (650 ns Cycle Time)

Parameters	Description	Test Conditions	Min.	Typ.(Note 1)	Max.	Units
t_{CE}	Delay Chip Select LOW to Output HIGH or LOW	V_{IL} = 0.65V V_{IH} = 2.2V $t_r = t_f$ = 20ns Measure at 1.5V	0		250	ns
t_{CD}	Delay Chip Select HIGH to Output OFF		0		200	ns
t_{pd+}(A)	Delay Address to Output HIGH		50		650	ns
t_{pd-}(A)	Delay Address to Output LOW		50		650	ns
$t_{pw}(\overline{WE})$	Minimum Write Pulse Width				400	ns
t_s(D)	Data Set-up Time				250	ns
t_h(D)	Data Hold Time				100	ns
t_s(A)	Address Set-up Time				200	ns
t_h(A)	Address Hold Time				50	ns
$t_s(\overline{CS})$	Chip Select Set-up Time				400	ns
$t_h(\overline{CS})$	Chip Select Hold Time				50	ns
T_{CYCLE}	Read or Write Cycle Time		650			ns

Switching limits are independent of data and addressing patterns.

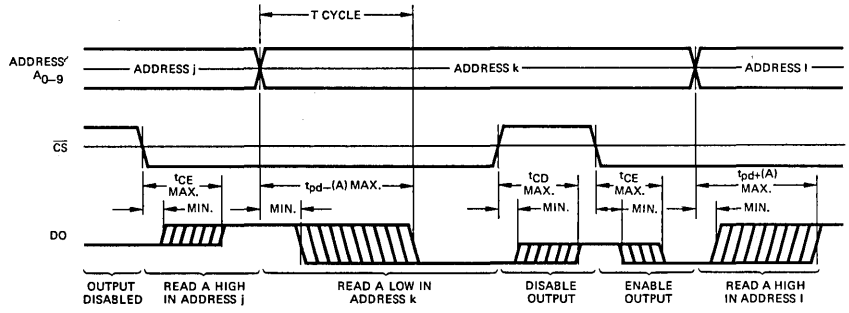
SWITCHING WAVEFORMS



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

Write Cycle Timing. The cycle is initiated by an address change. After t_s(A) max., the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, t_h(A) max. must be allowed before the address may be changed again. The output will follow the data input while the write enable is LOW. Chip select must be HIGH by $t_h(\overline{CS})$max. prior to the write pulse to prevent writing in a non-selected device.



Switching delays from address and chip select inputs to the data output.

DEFINITION OF TERMS

FUNCTIONAL TERMS

$\overline{CS}$ Active LOW chip select input. When the chip select is LOW data can be read from or written into the memory.

$\overline{WE}$ Active LOW Write Enable. When the write enable is LOW, data on the data input is written into the addressed memory location. When $\overline{WE}$ is HIGH data is read from the addressed location and appears at the data output.

SWITCHING TERMS

t_{CE} The delay from the chip select input going LOW to the output going active and to the correct state.

t_{CD} The delay from the chip select going HIGH to the output assuming an inactive high impedance level.

$t_{pd\pm}$(A) The delay from a change on the address inputs to a correct HIGH (t_{pd+}) or LOW (t_{pd-}) level on the outputs. Access time.

$t_s(\overline{CS})$ Chip select set-up time. The time prior to the end of the write pulse by which $\overline{CS}$ must be LOW to write.

$t_h(\overline{CS})$ Chip select hold time. The time after the end of the write pulse during which $\overline{CS}$ must remain LOW to write. Also the time prior to the write pulse at which $\overline{CS}$ must be HIGH to prevent writing.

$t_{pw}(\overline{WE})$ Minimum write pulse width. The shortest LOW time on the write enable input guaranteed to cause a write.

t_s(D) Data set-up time. The time, relative to the end of the write pulse (LOW-to-HIGH edge) at which the data on the data inputs may be written into the memory. To ensure writing the correct data, the data must be present before t_s(D) max.

t_h(D) Data hold time. The time relative to the end of the write pulse after which data will not be written. To ensure writing correct data, data must not be changed until after t_h(D) max.

t_s(A) Address set-up time. The time prior to the start of the write pulse (HIGH-to-LOW edge) at which the correct write address must be on the address inputs. An address change later than t_s(A) max. may cause writing in two addresses.

t_h(A) Address hold time. The time following the end of the write pulse (LOW-to-HIGH transition) at which a new address may be applied. An address change earlier than t_h(A) max. may cause writing into two addresses.

POWER DOWN STANDBY OPERATION

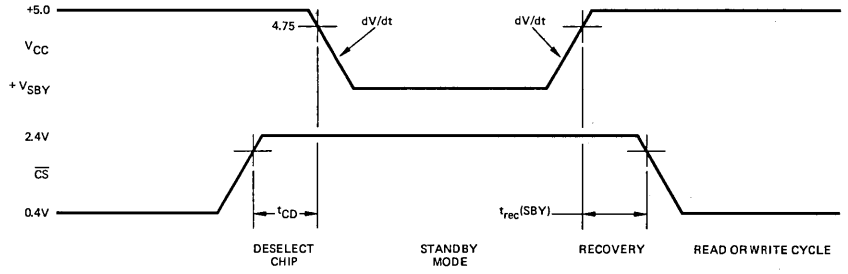
The Am9102 is designed to maintain storage in a standby mode. The standby mode is entered by lowering V_{CC} to around 1.6–2.0 volts (see table and graph below). When the voltage to the device is reduced, the storage cells are isolated from the data lines, so their contents will not change. The standby mode may be used by a battery operated back-up power supply system, or, in a large system, memory pages not being accessed can be placed in standby to save power.

A standby recovery time must elapse following restoration of normal power before the memory may be accessed.

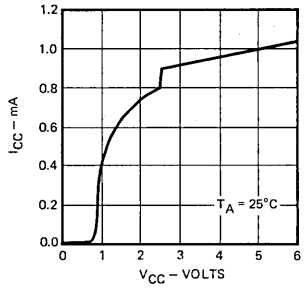
To ensure that the output of the device is in a high impedance OFF state during standby, the chip select should be raised for the chip disable time (t_{CD}) prior to entering the standby mode, and should be held at V_{IH} during the entire standby cycle.

STANDBY OPERATING CONDITIONS OVER TEMPERATURE RANGE

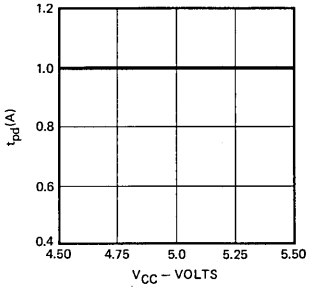
Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{SBY}	V_{CC} in Standby Mode		1.6			V
I_{SBY}/I_{OP}	I_{CC} in standby mode, as a percent of I_{CC} in operating mode.	V_{SBY} = 1.6V		65	80	%
dV/dt	Rate of Change of V_{CC}				1	V/μS
t_{rec}(SBY)	Standby Recovery Time		T_{CYCLE}			ns



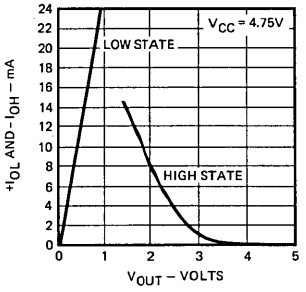
Power Supply Current Vs. Voltage Normalized to Current at V_{CC} = 5.0 Volts



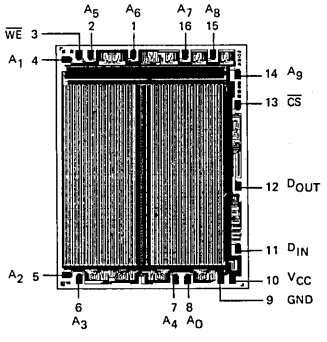
Access Time Vs. V_{CC} Normalized to V_{CC} = +5.0 Volts



Typical Output Current Vs. Voltage

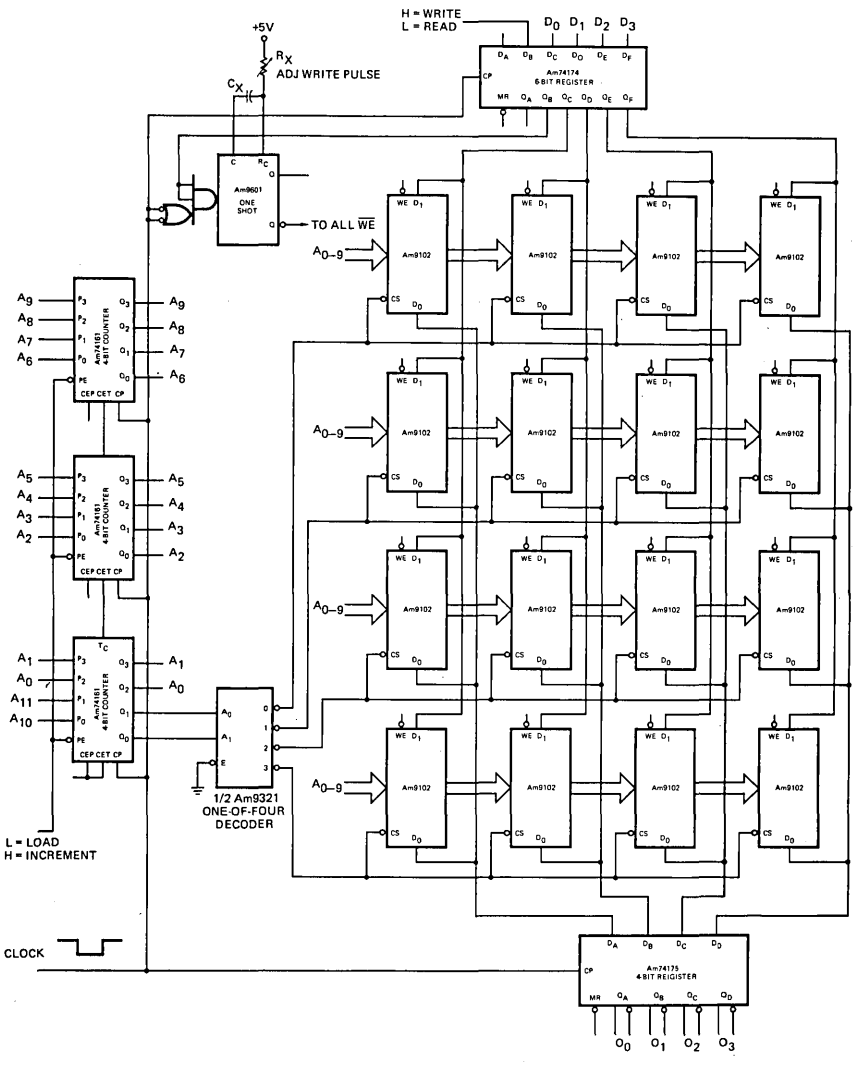


Metallization and Pad Layout



DIE SIZE
.126" X .164"

APPLICATIONS

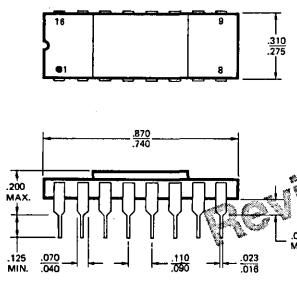


4 K Word by 4-Bit Memory System

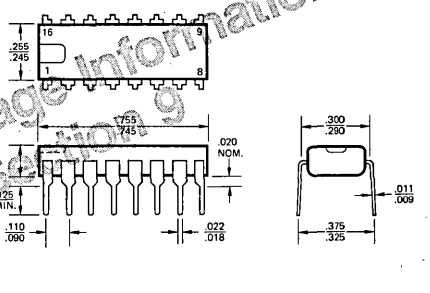
The clock signal HIGH-to-LOW transition fires the one-shot and initiates the write pulse. The write pulse should end 100ns prior to the next clock LOW-to-HIGH transition. On each clock pulse, the data input register is loaded with four bits of data and a read/write bit and the address register is either loaded or incremented. Output data is loaded on the next clock pulse.

PHYSICAL DIMENSIONS
Dual-In-Line

16-Pin Side-Brazed



16-Pin Molded



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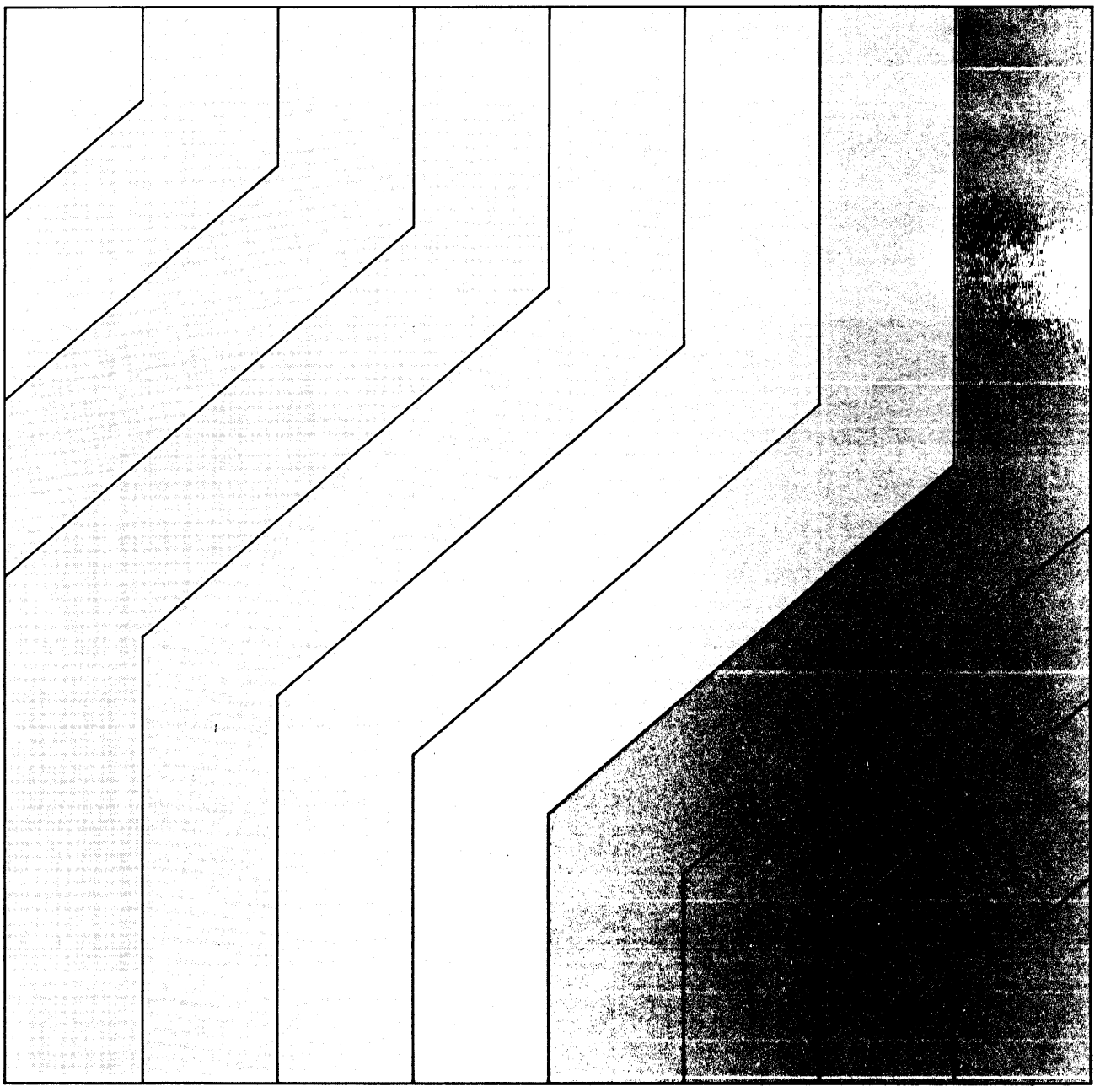
TELEX: 34-6306

Bipolar Memory



Am2700/2701
256-Bit Random Access Memories

Distinctive Characteristics

- High-speed 256-word x 1-bit fully decoded RAM
- Memory access time of 70 ns typical
- Choice of three-state (Am2700) or open-collector (Am2701) output.
- Output only active during read operation allows interleaving of memories and single bus operation
- 100% reliability assurance testing in compliance with MIL STD 883
- Electrically tested and optically inspected die for the assemblers of hybrid products
- Mixing privileges for obtaining price discounts Refer to price list

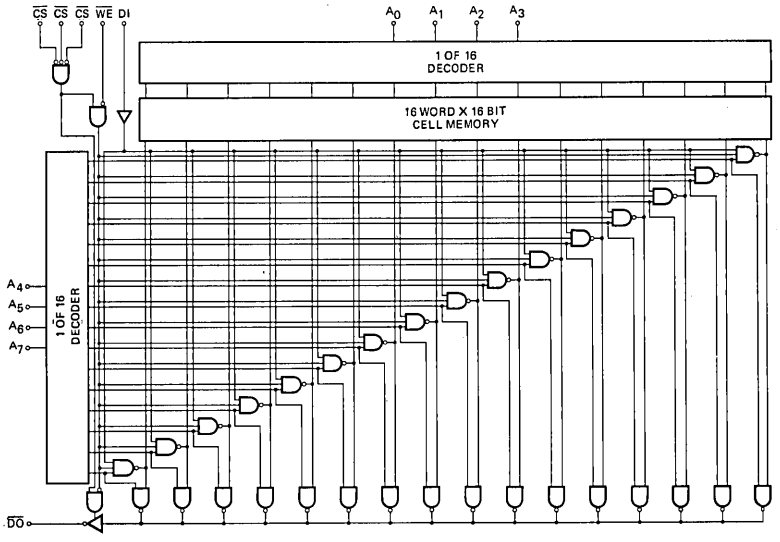
FUNCTIONAL DESCRIPTION

The Am2700 and Am2701 are fully decoded bipolar random access memories for use in high-speed buffer memories and as a replacement for high-speed core memories in digital systems. The memories are organized 256 words by 1 bit with an 8-bit binary address field and separate data in and data output lines. The memories have three active LOW chip select inputs and a three-state output (Am2700) or open-collector output (Am2701). All inputs are buffered to present an input load of only 0.5 TTL unit loads.

Read/write operation is controlled by an active LOW write enable input. When the write enable is LOW and the chip is selected the data on the data input is written into the location specified by the address inputs. During this operation the output floats allowing the data bus to be used by other memories or open-collector logic elements that are tied to the inverting data output. Reading is accomplished by having the chip selected and the write enable input HIGH. Data stored in the location specified by the address inputs is read out and appears on the data output inverted.

The chip is selected by three active LOW inputs all of which must be LOW in order for the data output to be active during the read operation and for data to be written into or from the memory. These three active LOW chip select inputs permit the Am9301 and Am9311 MSI decoders to select memories in either a linear select, two or three dimensional mode of operation when large memory systems are being built. The delay from the chip select to the output is considerably faster than from the address inputs and extra delay can be tolerated in the chip select path without affecting system performance.

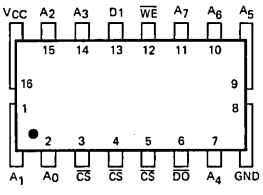
LOGIC DIAGRAM



ORDERING INFORMATION

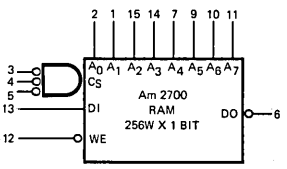
Part Number	Package Type	Temperature Range	Order Number
Am2700	Hermetic DIP	0°C to +75°C	AM270059E
Am2700	Hermetic Flat Pak	0°C to +75°C	AM270059F
Am2700	Dice	0°C to +75°C	AM2700XXD
Am2701	Hermetic DIP	0°C to +75°C	AM270159E
Am2701	Hermetic Flat Pak	0°C to +75°C	AM270159F
Am2701	Dice	0°C to +75°C	AM2701XXD

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +V_{CC}
Output Current, Into Outputs	30 mA
DC Input Current	−30mA to +50mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

T_A = 0°C to +75°C V_{CC} = 4.75 V to 5.25 V

Parameters	Test Conditions	Test Conditions	Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL} Am2700 only	2.4	3.1		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16.0 mA V_{IN} = V_{IH} or V_{IL}		0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V		−0.50	−0.80	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V		5	20	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.25 V			1.0	mA
I_{LK}	Output Leakage Current	V_{CC} = MAX., $\overline{CS}$ = 2.4 V, V_{OUT} = 2.4 V		5	30	μA
		V_{CC} = MAX., $\overline{CS}$ = 2.4 V, V_{OUT} = 0.4 V		−5	−30	
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V	−12.0	−30	−90	mA
I_{CC}	Power Supply Current	V_{CC} = 5.0 V		99	135	mA

Note 1. Typical Limits are at V_{CC} = 5.0 V, 25°C Ambient and maximum loading.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C, C_L = 30pF, R_L = 470Ω

Parameter	Definition	Figure	Min	Typ	Max	Units
t_{pd+} (A)	Delay from Address to Output	See Fig. 2	10	70	95	ns
t_{pd-} (A)			10	70	95	
t_{pd+} ($\overline{CS}$)	Delay from Chip Select to Active Output and Correct Data	Fig. 2	5	20	40	ns
t_{pd-} ($\overline{CS}$)			5	50	80	
t_{pd0} ($\overline{CS}$)	Delay from Chip Select to Inactive Output		10	20	40	ns
t_{rec} ($\overline{WE}$)	Delay from Write Enable (HIGH) to Correct Output Data	Fig. 1		60	90	ns
$t_{pd\pm}$ ($\overline{WE}$)	Delay from Write Enable (HIGH) to Active Output		10	25		
t_{pd0} ($\overline{WE}$)	Delay from Write Enable (LOW) to Inactive Output			25	40	ns
t_s (A)	Set Up Time Address	Fig. 1		0	15	ns
t_h (A)	Hold Time Address			−10	0	ns
t_s (DI)	Set Up Time Data Input	Fig. 1	−5		40	ns
t_{pw} ($\overline{WE}$)	Minimum Write Enable Pulse Width	Fig. 1		35	60	ns

DEFINITION OF TERMS

SUBSCRIPT TERMS:

F Forward, applying to LOW inputs.

H HIGH, applying to a HIGH-signal level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to a LOW signal level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

R Reverse, applying to HIGH inputs.

FUNCTIONAL TERMS:

Tri-State A tri-state output can exist in three possible states. Output LOW sinking current, output HIGH sourcing current, and output floating where the output level is determined by external circuitry connected to the output. This three state output allows AND tying of memory outputs for memory expansion and still keeps the inherent high speed of active pull-up circuitry.

Fully Decoded In a fully decoded memory every possible address combination of logic HIGH's and LOW's uniquely selects a memory word. This form of decoding requires no additional special purpose decoders for system operation and is the most efficient in terms of address inputs required and overall system speed.

Fan-Out The logic HIGH or LOW output drive capability in terms of input Unit Loads.

Input Unit Load One T^2L gate input load. In the HIGH state it is equal to I and in the LOW state it is equal to I_F.

SWITCHING TERMS: (All switching times are measured at the 1.5V logic level).

t_{pd+} The delay from a logic level change at an input to a HIGH level on an output.

t_{pd-} The delay from a logic level change at an input to a LOW level on an output.

t_{pd0} The delay from a logic level change at an input to a high impedance state on a tri-state output. Measured with a resistor pull-down or pull-up.

$t_{pd\Delta}$ **(A)** (Δ = + or −) The delay from an address input to the memory output.

$t_{pd\Delta}$ **($\overline{CS}$)** (Δ = +, −, or 0) The delay from a chip select input to the memory output.

t_{pd0} **($\overline{WE}$)** The delay from a HIGH to LOW transition on the write enable to a high impedance level on the memory output.

$t_{pd+,-}$ **($\overline{WE}$)** The delay from a LOW to HIGH transition on the write enable to an active level on the memory output.

t_{pw} **($\overline{WE}$)** The shortest LOW pulse on the write enable input which is guaranteed to cause the memory to write. Pulses shorter than t_{pw} ($\overline{WE}$) max may or may not cause a write to occur.

t_s **(DI)** The data input set-up time. A memory will store the logic level present on the write enable. Since t_s (DI) varies from device to device, reliable operation requires that the data input to a memory be steady at all times between t_s (DI) max and t_s (DI) min. A negative t_s indicates a time after the write enable has ended, and may be thought of as a "hold time."

t_s **(A)** The set up time of the address inputs relative to the HIGH to LOW edge of the write pulse. This is the time required for internal address decoding to settle. To avoid writing in spurious addresses, a stable address should be applied to the address inputs at least t_s (A) max before the write pulse begins.

t_h **(A)** The address hold time. This parameter is similar to t_s (A) but is measured relative to the end of the write pulse rather than the beginning. A stable address should be maintained on the address inputs for t_h (A) max after the write pulse has ended in order to prevent writing in spurious addresses.

OPERATIONAL TERMS:

I_{IL} Forward input load current.

I_{LK} Output leakage current with $\overline{CS}$ HIGH or $\overline{WE}$ LOW.

I_{OH} Output HIGH current, forced out of output in V_{OH} test.

I_{OL} Output LOW current, forced into output in V_{OL} test.

I_{IH} Reverse input load current with V_R applied to input.

I_{CC} The current drawn by the device under power supply, bias input terminals grounded and output terminals open.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IL} Forward LOW input voltage, for forward input current test.

V_{IH} Minimum logic HIGH input voltage.

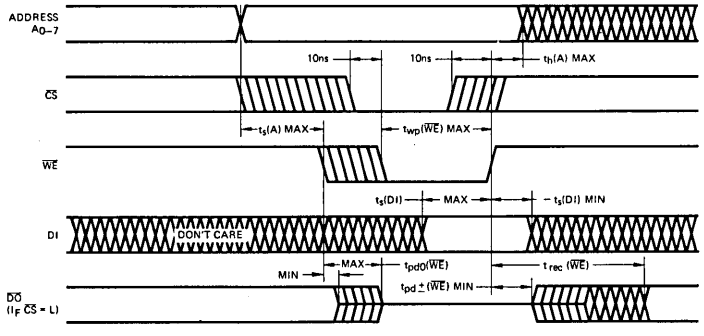
V_{IL} Maximum logic LOW input voltage.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into output.

V_{IH} Input reverse HIGH voltage applied for input leakage current, test.

SWITCHING WAVEFORMS

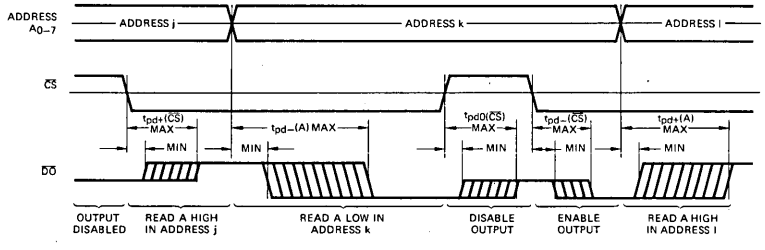


KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

Write Cycle Timing. The cycle is initiated by an address change. After t_s (A) max, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, t_h (A) max must be allowed before the address may be changed again. The output will be inactive (floating for the Am2700) while the write enable is LOW. Ordinarily, the chip select should be LOW during the entire write pulse.

Figure 1



Switching delays from address and chip select inputs to the data output. For the Am2700 a disabled output is "OFF," represented by a single center line. For the Am2701, a disabled output is HIGH.

Figure 2

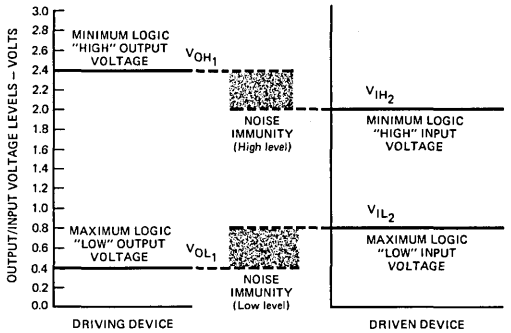
TRUTH TABLE

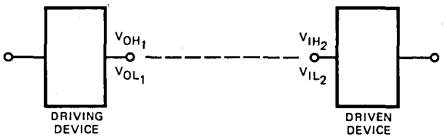
Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	DI	$\overline{DO}$ (t_{n+1})	
H	X	X	F	No Selection
L	L	L	F	Write '0'
L	L	H	F	Write '1'
L	H	X	$\overline{DO}$ (t_n)	Read

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
F = FLOATING Output Level is determined by external circuitry connected to the output

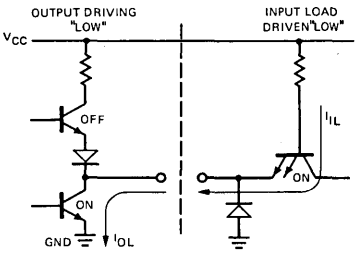
INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH

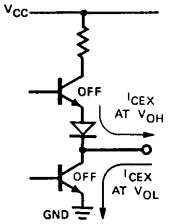




Current Interface Conditions — LOW

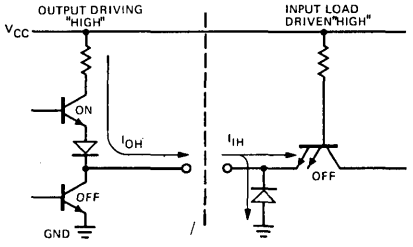


Current Interface Conditions — FLOATING



Current Interface Conditions — HIGH

(Note) Am2701 has open collector output



Am2700/2701 LOADING RULES

Input/Output	Pin No.s	Input Unit Load	Fanout Output HIGH	Fanout Output LOW
A_1	1	0.5	—	—
A_0	2	0.5	—	—
$\overline{CS}$	3	0.5	—	—
$\overline{CS}$	4	0.5	—	—
$\overline{CS}$	5	0.5	—	—
DO	6	—	(Note) 50	10
A_4	7	0.5	—	—
GND	8	—	—	—
A_5	9	0.5	—	—
A_6	10	0.5	—	—
A_7	11	0.5	—	—
$\overline{WE}$	12	0.5	—	—
DI	13	0.5	—	—
A_3	14	0.5	—	—
A_2	15	0.5	—	—
V_{CC}	16	—	—	—

Note: Am2701 has open collector output.

MSI INTERFACING RULES

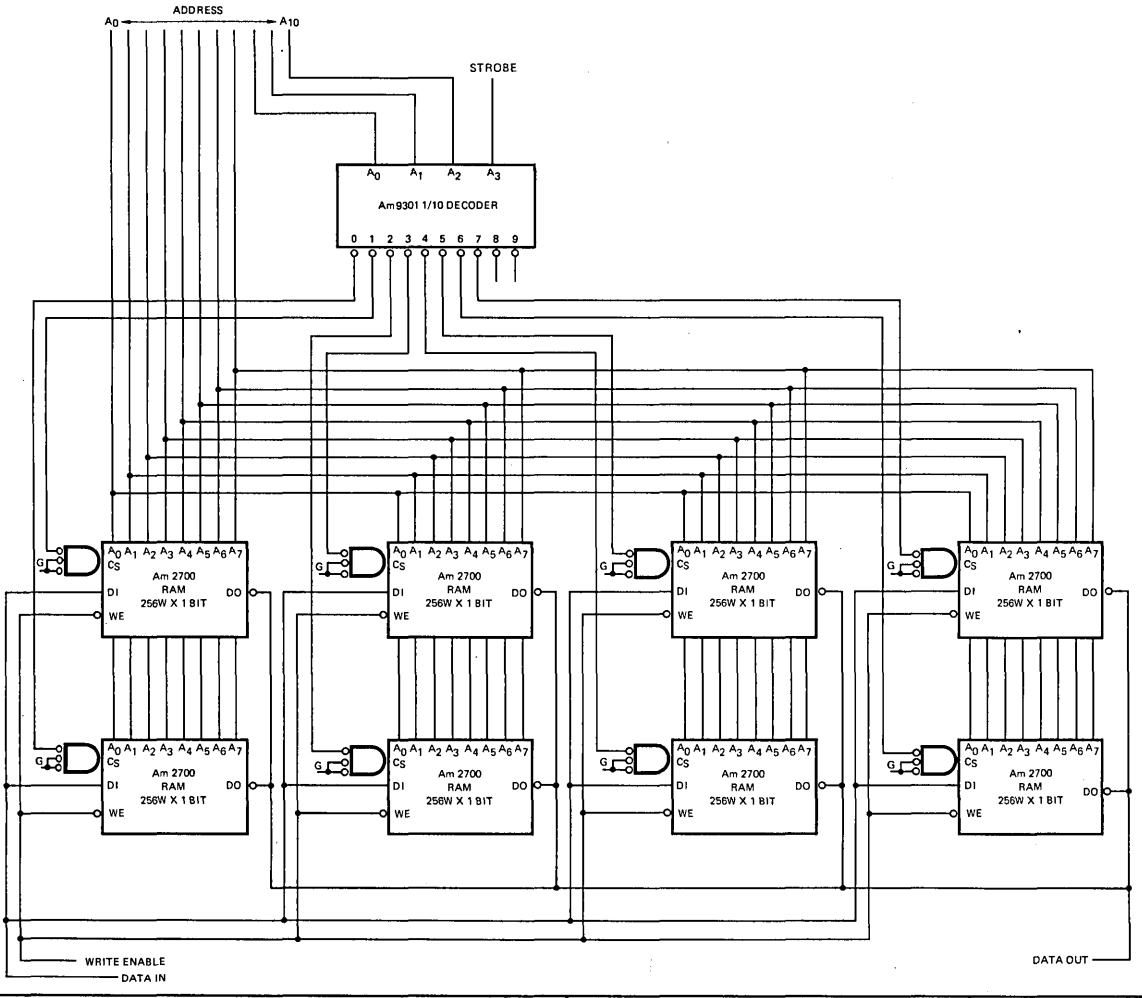
Interfacing Digital Family	Equivalent Input Unit Load HIGH	Equivalent Input Unit Load LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

USER NOTES

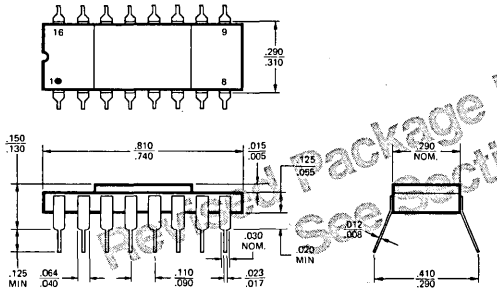
1. Address lines can be interchanged for ease of printed circuit layout without affecting functional operation.
2. Since for a given pattern on the address line reading and writing are performed on the same memory word, the address lines can be driven by any mixture of assertion or negation of the variables making up the address field.

APPLICATION

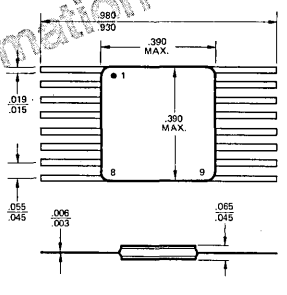
2048 WORD X 1 BIT MEMORY



PHYSICAL DIMENSIONS



Flat Package



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Am27LS00/01
Schottky 256-Bit Random Access Memories

Distinctive Characteristics

- High-speed, fully decoded 256-bit random access memory
- Internal ECL circuitry gives 35 ns access time
- Low power dissipation – 275 mw
- Low input loading – 0.5mA
- 100% reliability assurance testing in compliance with MIL-STD-883
- Three-State (Am27LS00) or open collector (Am27LS01) versions

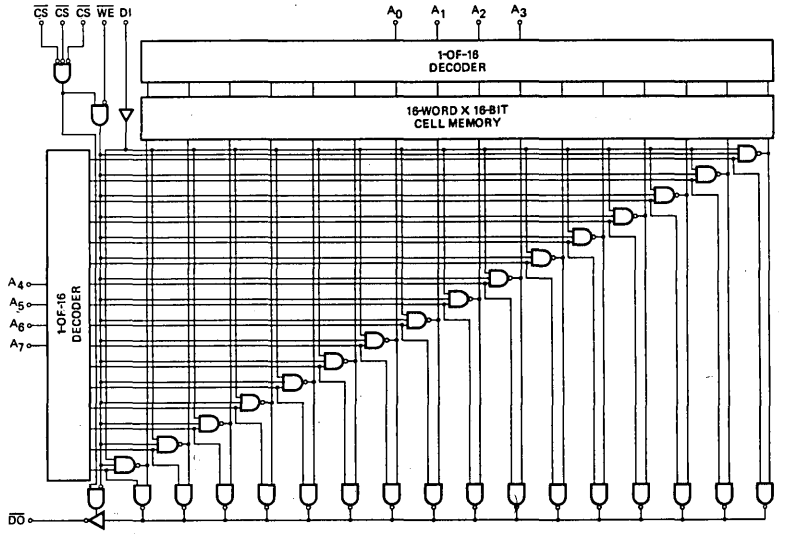
FUNCTIONAL DESCRIPTION

The Am27LS00 and Am27LS01 are fully decoded bipolar random access memories for use in high-speed buffer memories and as a replacement for high-speed core memories in digital systems. The memories are organized 256 words by 1 bit with an 8-bit binary address field and separate data in and data output lines. The memories have three active LOW chip select inputs and a three-state output (Am27LS00) or open-collector output (Am27LS01). All inputs are buffered to present an input load of only 0.5 TTL unit loads.

Read/write operation is controlled by an active LOW write enable input. When the write enable is LOW and the chip is selected the data on the data input is written into the location specified by the address inputs. During this operation the output floats allowing the data bus to be used by other memories or open-collector logic elements that are tied to the inverting data output. Reading is accomplished by having the chip selected and the write enable input HIGH. Data stored in the location specified by the address inputs is read out and appears on the data output inverted.

The chip is selected by three active LOW inputs all of which must be LOW in order for the data output to be active during the read operation and for data to be written into or from the memory. These three active LOW chip select inputs permit the Am9301 and Am9311 MSI decoders to select memories in either a linear select, two or three dimensional mode of operation when large memory systems are being built. The delay from the chip select to the output is considerably faster than from the address inputs and extra delay can be tolerated in the chip select path without affecting system performance.

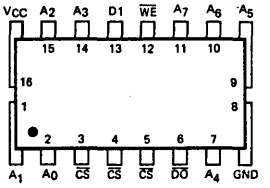
LOGIC DIAGRAM



ORDERING INFORMATION

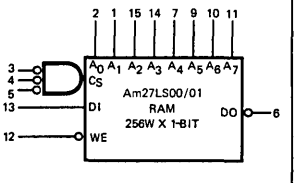
The specifications given in this data sheet are based on design objectives, and are subject to change following full characterization of the product.

CONNECTION DIAGRAM
Top View



NOTE: PIN 1 is marked for orientation.

LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +V_{CC}
Output Current, Into Outputs	30 mA
DC Input Current	−30mA to +50mA

Part No.	Ambient Operating Temperature	Power Supply Voltage
Am27LS00DC Am27LS01DC	0°C to +75°C	4.75 V to 5.25 V
Am27LS00DM Am27LS01DM	−55°C to +125°C	4.50 V to 5.50 V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Parameters	Test Conditions	Test Conditions	Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL} Am2700 only	2.4	3.1		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16.0 mA V_{IN} = V_{IH} or V_{IL}		0.3	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V		−0.50	−0.80	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V		5	20	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.25 V			1.0	mA
I_{LK}	Output Leakage Current	V_{CC} = MAX., $\overline{CS}$ = 2.4 V, V_{OUT} = 2.4 V		5	30	μA
		V_{CC} = MAX., $\overline{CS}$ = 2.4 V, V_{OUT} = 0.4 V		−5	−30	
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V		30		mA
I_{CC}	Power Supply Current	V_{CC} = 5.0 V		55		mA

Note 1. Typical Limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.

Typical Switching Characteristics V_{CC} = 5 V, C_L = 30pF, R_L = 470Ω

Parameter	Definition	Figure	T_A = 25°C	T_A = 0°C to 75°C	T_A = −55°C to 125°C	Units
t_{pd+} (A)	Delay from Address to Output	See Fig. 2	35	50	70	ns
t_{pd-} (A)			35	50	70	
t_{pd+} ($\overline{CS}$)	Delay from Chip Select to Active Output and Correct Data	Fig. 2	15	25	30	ns
t_{pd-} ($\overline{CS}$)			20	30	40	
t_{pd0} ($\overline{CS}$)	Delay from Chip Select to Inactive Output		20	30	40	ns
t_{rec} ($\overline{WE}$)	Delay from Write Enable (HIGH) to Correct Output Data	Fig. 1	30	45	60	ns
$t_{pd\pm}$ ($\overline{WE}$)	Delay from Write Enable (HIGH) to Active Output		20	30	40	
t_{pd0} ($\overline{WE}$)	Delay from Write Enable (LOW) to Inactive Output		20	30	40	ns
t_s (A)	Set Up Time Address	Fig. 1	10	15	20	ns
t_h (A)	Hold Time Address		5	10	15	ns
t_s (DI)	Set Up Time Data Input	Fig. 1	20	30	40	ns
t_{pw} ($\overline{WE}$)	Minimum Write Enable Pulse Width	Fig. 1	20	30	40	ns

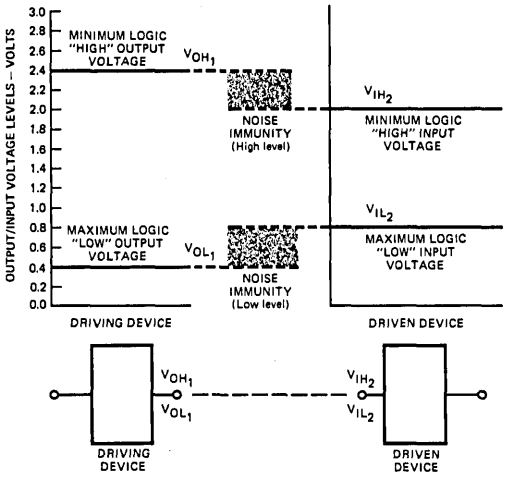
TRUTH TABLE

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	DI	$\overline{DO}$ (t_{n+1})	
H	X	X	F	No Selection
L	L	L	F	Write '0'
L	L	H	F	Write '1'
L	H	X	$\overline{DO}$ (t_n)	Read

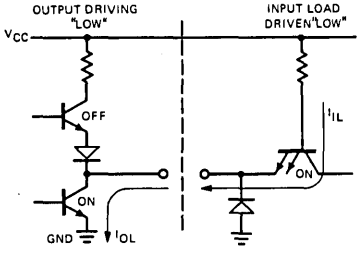
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
F = FLOATING Output Level is determined by external circuitry connected to the output

INPUT/OUTPUT INTERFACE CONDITIONS

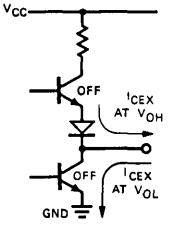
Voltage Interface Conditions — LOW & HIGH



Current Interface Conditions — LOW

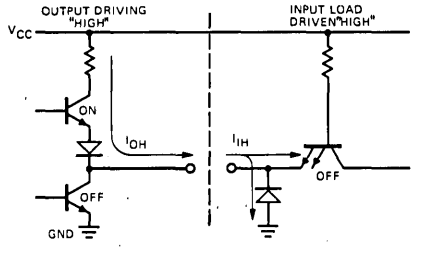


Current Interface Conditions — FLOATING



Current Interface Conditions — HIGH

(Note) Am2701 has open collector output



Am27LS00/27LS01 LOADING RULES (in TTL Unit Loads)

Input/Output	Pin No.s	Input Unit Load	Fanout Output HIGH	Fanout Output LOW
A_1	1	0.5	—	—
A_0	2	0.5	—	—
$\overline{CS}$	3	0.5	—	—
$\overline{CS}$	4	0.5	—	—
$\overline{CS}$	5	0.5	—	—
DO	6	—	(Note) 50	10
A_4	7	0.5	—	—
GND	8	—	—	—
A_5	9	0.5	—	—
A_6	10	0.5	—	—
A_7	11	0.5	—	—
$\overline{WE}$	12	0.5	—	—
DI	13	0.5	—	—
A_3	14	0.5	—	—
A_2	15	0.5	—	—
V_{CC}	16	—	—	—

Note: Am27LS01 has open collector output.

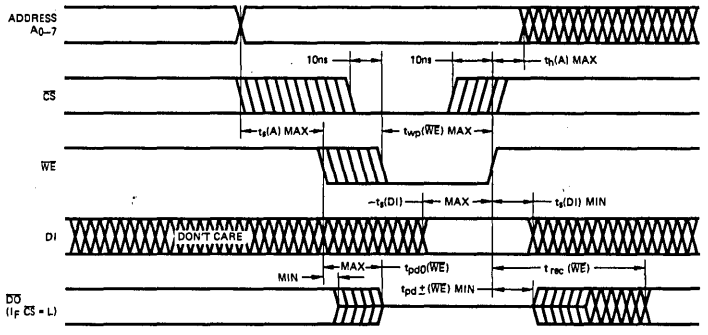
MSI INTERFACING RULES

Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

USER NOTES

1. The delay from chip select to the data output is considerably less than from the address inputs to the data output. Additional decoding delay can therefore be inserted into the chip select path without incurring any speed penalty.
2. The memory is organized internally as a 16 x 16 matrix with the A_{0-3} address lines selecting 16 words and the A_{4-7} address lines selecting the required bit in the word. The delay from the A_{4-7} address inputs to the data output is therefore faster than from the A_{0-3} address inputs. This together with the shorter chip select delay can be used to increase overall operational speed in a paged memory system.
3. Address lines can be interchanged for ease of printed circuit layout without affecting functional operation.
4. Since for a given pattern on the address line reading and writing are performed on the same memory word, the address lines can be driven by any mixture of assertion or negation of the variables making up the address field.

SWITCHING WAVEFORMS

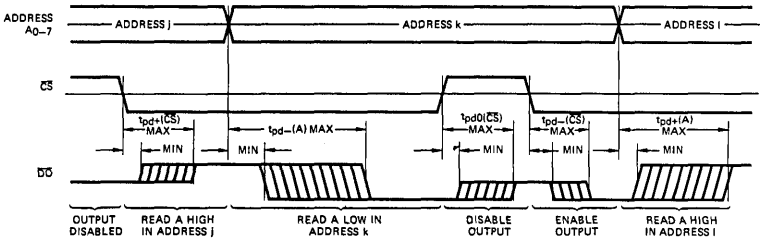


KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

Write Cycle Timing. The cycle is initiated by an address change. After t_s (A) max, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, t_h (A) max must be allowed before the address may be changed again. The output will be inactive (floating for the Am27LS00) while the write enable is LOW. Ordinarily, the chip select should be LOW during the entire write pulse.

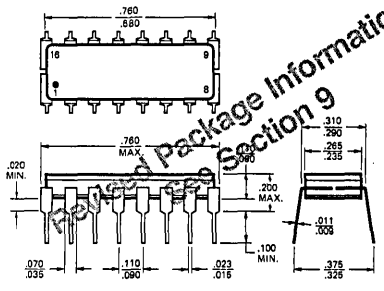
Figure 1



Switching delays from address and chip select inputs to the data output. For the Am27LS00 disabled output is "OFF," represented by a single center line. For the Am27LS01, a disabled output is HIGH.

Figure 2

PHYSICAL DIMENSIONS



ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am3101•Am54/7489•Am93403•Am31L01

Standard and Low-Power 64-Bit Random Access Memories

Distinctive Characteristics

- Fully decoded 16-word x 4-bit Schottky technology standard and low-power, high speed RAMS
- Access time typically 30 ns for standard and 70 ns for low-power device
- Chip select and open collector outputs for simple memory expansion
- Available in both the military and commercial ambient temperature ranges and in low-power version (Am31L01)
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Plug-in replacement for TI7489 and Fairchild 93403.

FUNCTIONAL DESCRIPTION

The Am3101 is a 64-bit RAM built using Schottky diode clamped transistors and is ideal for use in scratch pad and high-speed buffer memory applications. The memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW Chip Select ($\overline{CS}$) input and open collector OR tieable outputs. Chip selection for large memory systems can be controlled by active LOW output decoders such as the Am9301 and Am9311.

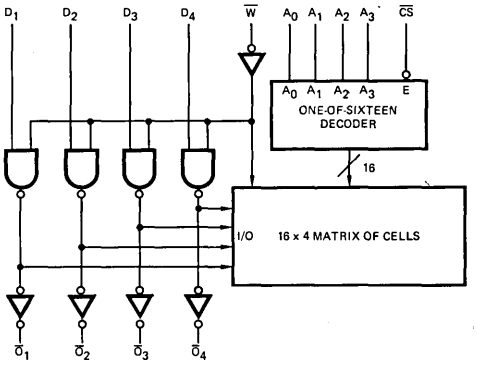
An active LOW write line ($\overline{W}$) controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs D_1 to D_4 is written into the addressed memory word.

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four inverting outputs $\overline{O}_1$ to $\overline{O}_4$.

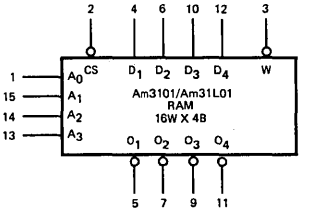
Whenever the write enable is LOW the four outputs of the memory may be either HIGH or LOW.

Any time the chip select is HIGH and the write enable is HIGH, all four outputs go HIGH.

LOGIC DIAGRAM



LOGIC SYMBOL

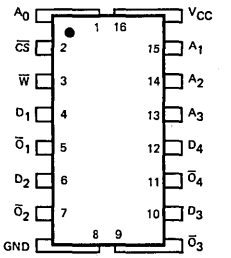


V_{CC} = Pin 16
GND = Pin 8

ORDERING INFORMATION

Package Type	Ambient Temperature Range	Am3101 Order Number	Am54/7489 Order Number	Am93403 Order Number	Am31L01 Order Number
Molded DIP	0°C to +75°C	P3101	SN7489N	93403PC	AM31L01PC
Hermetic DIP	0°C to +75°C	C3101	SN7489J	93403DC	AM31L01DC
Hermetic DIP	−55°C to +125°C	C31013	SN5489J	93403DM	AM31L01DM
Flat Pack	−55°C to +125°C	AM3101FM	SN5489W	93403FM	AM31L01FM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Outputs	30mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise noted)

Am3101 • Am54/7489 • Am93403

Am3101, Am7489, Am93403XC — T_A = 0°C to +75°C — V_{CC} = 5.0V ±5%
Am31013, Am5489, Am93403XM — T_A = −55°C to +125°C — V_{CC} = 5.0V ±10%

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
I_{CEX}	Output Leakage Current	V_{CC} = MAX., V_{OUT} = V_{CC} $\overline{CS}$ = 2.5V				100	µA
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.25	0.45	Volts
*V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
*V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V			−1.0	−1.6	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 4.5V			1.0	40	µA
V_C	Input Clamp Voltage	V_{CC} = MIN., I_C = −5.0mA				−1.0	Volts
I_{CC}	Power Supply Current	V_{CC} = MAX. All inputs = GND	0°C to 75°C			105	mA
			−55°C to +125°C			105	mA

Note: 1. Typical Limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

Am31L01

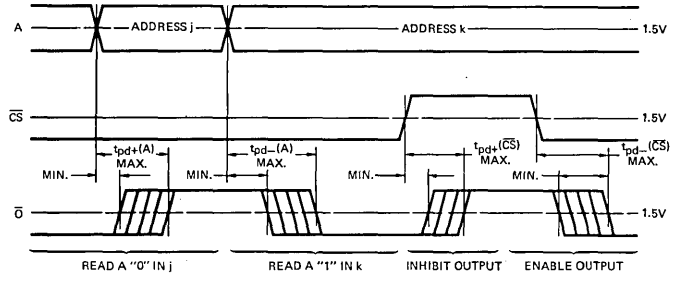
Am31L01XC — T_A = 0°C to +75°C — V_{CC} = 4.75V to 5.25V
Am31L01XM — T_A = −55°C to +125°C — V_{CC} = 4.50V to 5.50V

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
I_{CEX}	Output Leakage Current	V_{OUT} = V_{CC} = MAX.			40	µA
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 4.8mA V_{IN} = V_{IH} or V_{IL}		0.2	0.4	Volts
*V_{IH}	Input HIGH Voltage	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
*V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.7	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.3V		−0.25	−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V		2.0	20	µA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
V_C	Input Clamp Voltage	V_{CC} = MIN., I_C = −5.0mA			−1.0	Volts
I_{CC}	Power Supply Current	V_{CC} = MAX.		27	35	mA

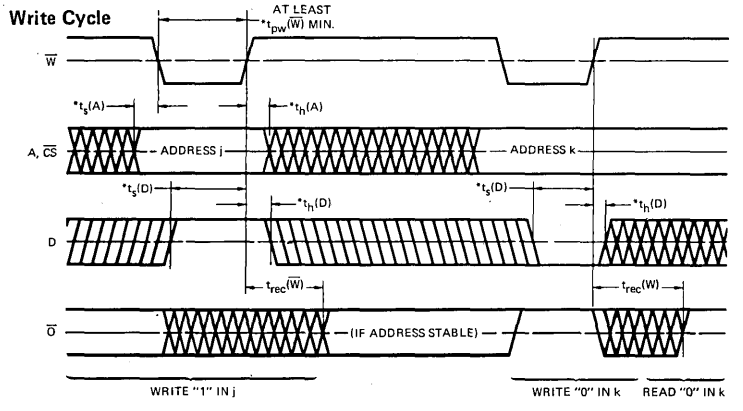
 *System requirement. Parameters preceeded by an asterisk are specified as system forcing requirements rather than device characteristics. In general, minimum system requirements result from maximum device characteristics. Typical values are not meaningful for system requirements.

SWITCHING WAVEFORMS

Read Cycle

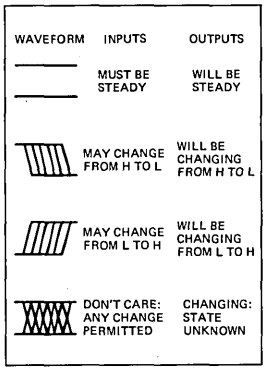


Write Cycle



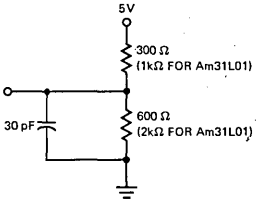
Two Write Cycles Followed by a Read

KEY TO TIMING DIAGRAM



TEST CONDITIONS:
RISE TIME < 10ns
FALL TIME < 10ns
AMPLITUDE ≈ 4V
MEASURE AT 1.5V

A.C. Test Load



Note: During the "write" cycle, input data lines are connected to the output sense amplifiers. Spurious signals may appear on the output data lines as the "write" input signal makes the transition from its LOW (write) state to its HIGH (read) state. This period of uncertainty is defined as $t_{rec}(\overline{W})$ in the specifications and since $t_{rec}(\overline{W})$ is well under the access time no difficulty will be encountered when the recommended timing sequence is used.

SWITCHING CHARACTERISTICS AND OPERATING REQUIREMENTS

Am3101 • Am54/7489 • Am93403

Parameters	Description	Test Conditions	Ambient Temperature 25°C Typ.	0°C to +75°C Min.	0°C to +75°C Max.	Units
$t_{pd+}(\overline{CS})$	Delay Chip Select to Output HIGH	V_{CC} = 5.0V, C_L = 30 pF, R_L = 300Ω to V_{CC} and 600Ω to GND	27	20	60	ns
$t_{pd-}(\overline{CS})$	Delay Chip Select to Output LOW		30	20	60	ns
$t_{pd+}(A)$	Delay Address to Output HIGH		28	20	60	ns
$t_{pd-}(A)$	Delay Address to Output LOW		31	20	60	ns
$*t_{pw}(\overline{W})$	Write Pulse Width			40		ns
$t_{rec}(\overline{W})$	Write Recovery Time		30		50	ns
$*t_s(D)$	Data Set-up Time			25		ns
$*t_h(D)$	Data Hold Time			0		ns
$*t_s(A)$	Address Set-up Time			0		ns
$*t_h(A)$	Address Hold Time			0		ns

Am31L01

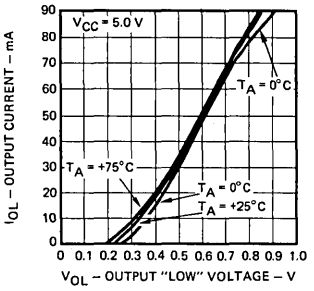
Parameters	Description	Test Conditions	Ambient Temperature T_A = 25°C Min.	Typ.	Max.	Units
$t_{pd+}(\overline{CS})$	Delay Chip Select to Output HIGH	V_{CC} = 5.0V, C_L = 30 pF, R_L = 1kΩ to V_{CC} and 2kΩ to GND	45	70	105	ns
$t_{pd-}(\overline{CS})$	Delay Chip Select to Output LOW		45	70	110	ns
$t_{pd+}(A)$	Delay Address to Output HIGH		40	70	105	ns
$t_{pd-}(A)$	Delay Address to Output LOW		50	75	110	ns
$*t_{pw}(\overline{W})$	Write Pulse Width		80			ns
$t_{rec}(\overline{W})$	Write Recovery Time		100			ns
$*t_s(D)$	Data Set-up Time		30			ns
$*t_h(D)$	Data Hold Time		0			ns
$*t_s(A)$	Address Set-up Time		0			ns
$*t_h(A)$	Address Hold Time		0			ns

*System requirement. Parameters preceeded by an asterisk are specified as system forcing requirements rather than device characteristics. In general, minimum system requirements result from maximum device characteristics. Typical values are not meaningful for system requirements.

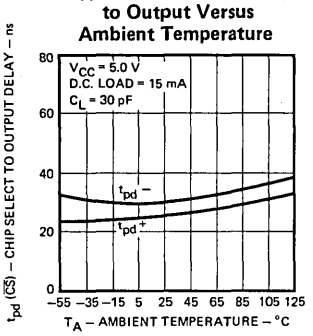
PERFORMANCE CURVES

Am3101 • Am54/7489 • Am93403

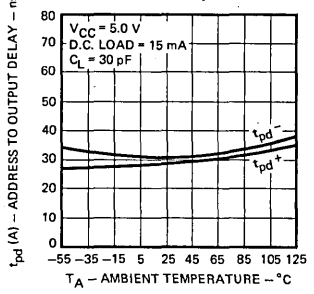
Output Current Versus Output "Low" Voltage



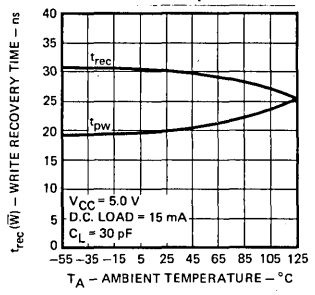
Typical Chip Select Delay to Output Versus Ambient Temperature



Typical Address Delay to Output Versus Ambient Temperature



Typical Write Pulse and Write Recovery Time Width Versus Ambient Temperature



DEFINITION OF TERMS

FUNCTIONAL TERMS

$\overline{CS}$ Active LOW chip select input. When the chip select is LOW data can be read from or written into the memory.

D_i The data inputs of the memory. i = 1 – 4

O_i The data outputs of the memory, i = 1 – 4

$O_i(t_n)$ The state of output i at time n.

$D_i(t_{n-x})$ The state of the D_i input at time t_{n-x}, where t_{n-x} is the time of the last write operation into a given address.

$\overline{W}$ Active LOW Write Enable. When the write enable is LOW, data on the data inputs is written into the addressed memory location. When $\overline{W}$ is HIGH data is read from the addressed location and appears, inverted, at the $\overline{O}$ outputs.

UNIT LOAD A TTL input unit load is defined as –1.6mA at 0.4V (LOW state) and 40μA at 2.4V (HIGH state).

SWITCHING TERMS

$t_{pd\pm}(\overline{CS})$ The delay from the chip select input going LOW to the output going active.

$t_{pdz}(\overline{CS})$ The delay from the chip select going HIGH to the output assuming an inactive high impedance level.

$t_{pd\pm}(A)$ The delay from a change on the address inputs to a correct HIGH (t_{pd+}) or LOW (t_{pd-}) level on the outputs. Access time.

$t_{rec}(\overline{W})$ Write recovery time. The delay from a LOW-to-HIGH transition on the write enable to the correct data on the outputs of the memory. This is the time required between the end of the write operation and a read operation in the same address.

*$t_{pw}(\overline{W})$ Minimum write pulse width. The LOW time on the write enable input required to cause a write.

$t_s(D)$,$t_h(D)$ Data set-up and hold times. The time, relative to the end of the write pulse (LOW-to-HIGH edge) after which the data on the data inputs will not be written into the memory. To ensure writing the correct data, the data must be present before *$t_s(D)$ min. and must remain until after *$t_h(D)$ min.

*$t_s(A)$ Address set-up time. The time prior to the start of the write pulse (HIGH-to-LOW edge) at which the correct write address must be on the address inputs. An address change later than *$t_s(A)$ max. may cause writing in two addresses.

*$t_h(A)$ Address hold time. The time following the end of the write pulse (LOW-to-HIGH transition) at which a new address may be applied. An address change earlier than *$t_h(A)$ min. may cause writing into two addresses.

$t_{pd\pm}(\overline{WE})$ The delay from a LOW-to-HIGH transition of the write enable to an active (but not necessarily correct) state on the data outputs. The correct state will be present after the write recovery time has elapsed.

$t_{pdo}(\overline{WE})$ The delay from a HIGH-to-LOW transition on the write enable to a high impedance level on the data outputs, if the chip is selected.

*System requirement. Parameters preceeded by an asterisk are specified as system forcing requirements rather than device characteristics. In general, minimum system requirements result from maximum device characteristics. Typical values are not meaningful for system requirements.

USER NOTES

1. For optimum system speed the memory output can be directly connected to following DTL or TTL circuitry without a pull up resistor.
2. For a good DC noise margin a pull up resistor can be used. Limits of R in kΩ are given by

$$\frac{V_{CC} - V_{OH}\text{ required}}{nI_{CEX} + NI_{IH}} > R_L > \frac{V_{CC} - V_{OL}\text{ required}}{I_{OL} - NI_{IL}}$$

Where n is number of OR tied outputs
N is the number of TTL unit loads driven.
I_{OL} is the maximum output LOW current.

3. Address and data lines can be interchanged within their respective groups for ease of P.C. layout without effecting device operation.
4. Since for a given pattern on the address lines reading and writing are performed on the same actual memory word, the address lines can be driven by any mixture of assertion or negation of the variables making up the address field.

MSI INTERFACING RULES

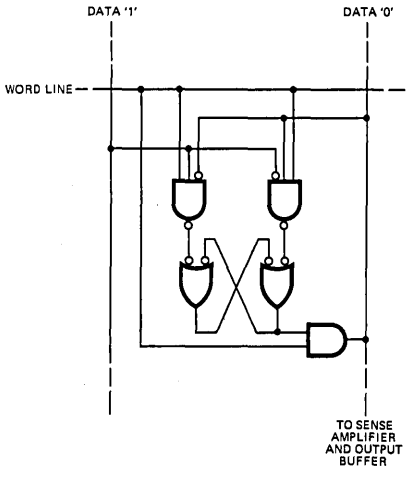
Interfacing Digital Family	Equivalent Input Unit Load HIGH	LOW
Advanced Micro Devices 54/7400	1	1
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

LOADING RULES

Input/ Output	Pin No.'s	Am3101 Am54/7489 • Am93403 Input Unit Load	Output LOW	Am31L01 Input Unit Load	Fan-out Output LOW
A_0	1	1	–	0.5	–
$\overline{CS}$	2	1	–	0.5	–
$\overline{W}$	3	1	–	0.5	–
D_1	4	1	–	0.5	–
$\overline{O}_1$	5	–	10	–	3
D_2	6	1	–	0.5	–
$\overline{O}_2$	7	–	10	–	3
GND	8	–	–	–	–
$\overline{O}_3$	9	–	10	–	–
D_3	10	1	–	0.5	–
$\overline{O}_4$	11	–	10	–	3
D_4	12	1	–	0.5	–
A_3	13	1	–	0.5	–
A_2	14	1	–	0.5	–
A_1	15	1	–	0.5	–
V_{CC}	16	–	–	–	–

Outputs are open collectors

Am3101/Am31L01 BASIC MEMORY CELL



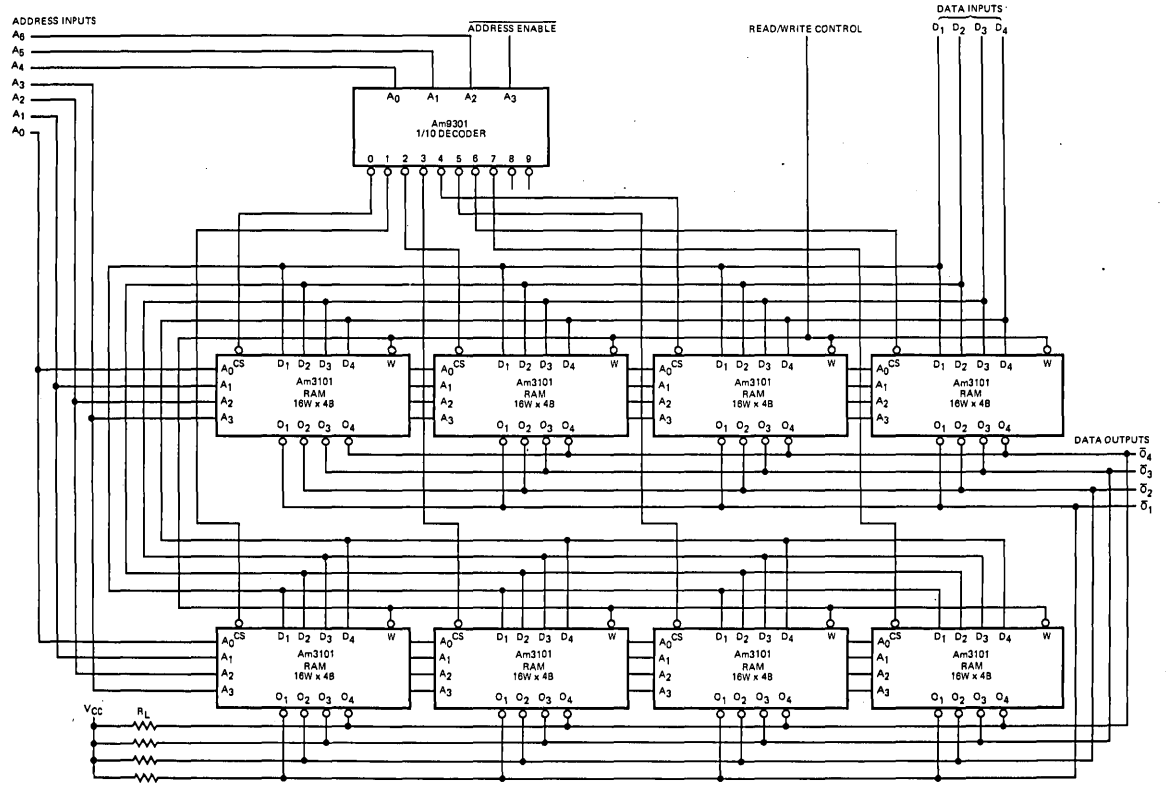
TRUTH TABLE

INPUTS $\overline{CS}$	INPUTS $\overline{W}$	INPUTS D_i	OUTPUTS $\overline{O}_i$	MODE	
H	L	L	X	No Selection	Note
H	L	H	X	No Selection	Note
H	H	X	H	No Selection	
L	L	L	H	Write '0'	
L	L	H	L	Write '1'	
L	H	X	$\overline{D}_i(t_{n-x})$	Read	

H = HIGH Voltage Level
L = LOW Voltage Level

Note: When the chip select $\overline{CS}$ input is HIGH and the Write Enable $\overline{W}$ is LOW data is not written into the memory. However, the data outputs may follow the data inputs inverted.

Am3101/Am31L01 APPLICATION

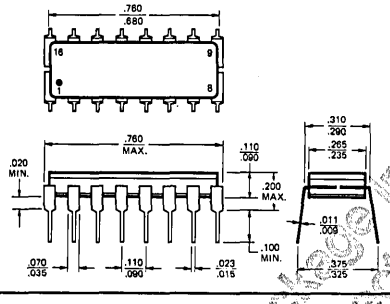


128-WORD x 4-BIT MEMORY

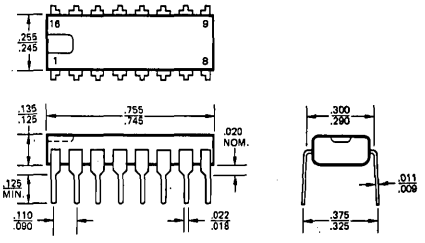
PHYSICAL DIMENSIONS

Dual-In-Line

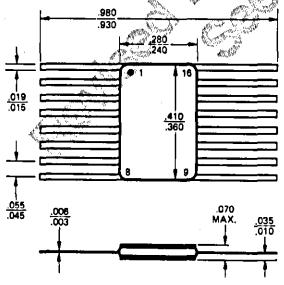
Hermetic



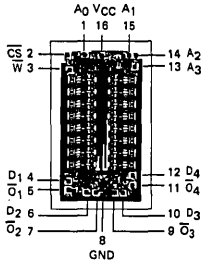
Molded



Flat Package



Metallization and Pad Layout



DIE SIZE 79 X 147 Mils

ADVANCED
MICRO
DEVICES INC.
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Sunnyvale
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Am3101A/Am27S02 • 27S03

64-Bit Random Access Memory

Distinctive Characteristics

- Fully decoded 16-word x 4-bit Schottky technology high-speed RAM.
- Access time typically 22ns.
- Available with three-state outputs (Am27S03) or with open collector outputs (Am27S02).
- Pin compatible high speed replacement for 3101, 93403, and 7489 (use Am27S02) and for DM 75/8599 (use Am27S03).
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

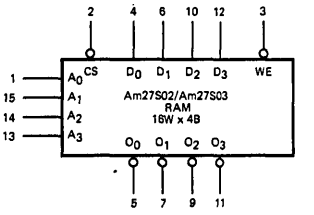
The Am27S02(Am3101A) and Am27S03 are 64-bit RAMs built using Schottky diode clamped transistors and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and open collector OR tieable outputs (Am3101A/Am27S02) or three-state outputs (Am27S03). Chip selection for large memory systems can be controlled by active LOW output decoders such as the Am9301 and Am9311.

An active LOW Write line $\overline{WE}$ controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs D_0 to D_3 is written into the addressed memory word.

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four inverting outputs $\overline{O}_0$ to $\overline{O}_3$.

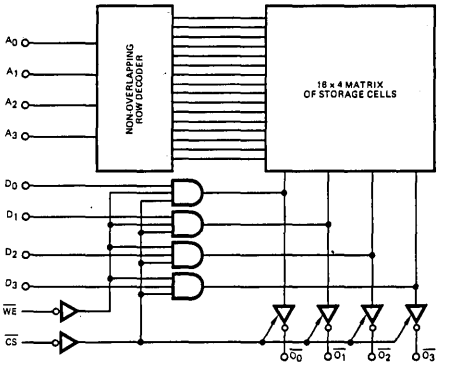
During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

LOGIC BLOCK DIAGRAM



ORDERING INFORMATION

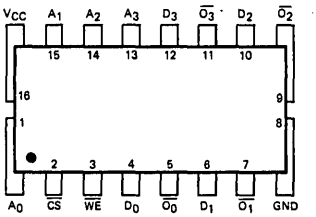
Open Collector Outputs

Package Type	Temperature Range	Order Number
Molded DIP	0°C to 75°C	AM27S02PC or P3101A
Hermetic DIP	0°C to 75°C	AM27S02DC or C3101A
Hermetic DIP	−55°C to +125°C	AM27S02DM
Hermetic Flat Pak	−55°C to +125°C	AM27S02FM

Three-State Outputs

Molded DIP	0°C to +75°C	AM27S03PC
Hermetic DIP	0°C to +75°C	AM27S03DC
Hermetic DIP	−55°C to +125°C	AM27S03DM
Hermetic Flat Pak	−55°C to +125°C	AM27S03FM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8)	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Outputs	100mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am27S02XC, Am27S03XC T_A = 0°C to +75°C V_{CC} = 5.0V ±5%
Am27S02XM, Am27S03XM T_A = −55°C to +125°C V_{CC} = 5.0V ±10%

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am27S03 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.8mA V_{IN} = V_{IH} or V_{IL}		2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA		0.3	0.45	Volts
			I_{OL} = 20mA			0.5	
*V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
*V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V	$\overline{WE}$, D_0–D_3, A_{0-3}		.030	0.25	mA
			$\overline{CS}$		.060	0.25	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V				10	µA
I_{SC} (Am27S03 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V		−12	−35	−90	mA
I_{CC}	Power Supply Current	All inputs = GND	Am27S02		76	105	mA
		V_{CC} = MAX.	Am27S03		87	125	
V_C	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −5.0mA				−1.0	Volts
I_{CEX}	Output Leakage Current	$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL} V_{OUT} = 2.4V	Am27S02			100	µA
			Am27S03			40	
		$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL} V_{OUT} = 0.4V, V_{CC} = MAX.	(Am27S03)	−40			µA

Note 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C

SWITCHING CHARACTERISTICS AND OPERATING REQUIREMENTS

Parameters	Description	Test Conditions		25°C Typ.	T_A = 0°C to 75°C Min.	Max.	Units
$t_{pd\pm}(\overline{CS})$	Delay Chip Select to Output HIGH or LOW	V_{CC} = 5.0V, C_L = 30 pF, R_L = 300Ω V_{CC} and 600Ω to GND (16mA Load) measure at 1.5V	Am27S02	12	5	17	ns
			Am27S03	15		25	
$t_{pdz}(\overline{CS})$	Delay Chip Select HIGH to Output OFF			12		20	ns
t_{pd+}(A)	Delay Address to Output HIGH			22	10	35	ns
t_{pd-}(A)	Delay Address to Output LOW			22	10	35	ns
$t_{rec}(\overline{WE})$	Write Recovery Time					35	ns
*$t_{pw}(\overline{WE})$	Write Pulse Width				25		ns
*t_s(D)	Data Set-up Time				25		ns
*t_h(D)	Data Hold Time				0		ns
*t_s(A)	Address Set-up Time				0		ns
*t_h(A)	Address Hold Time				0		ns
$t_{pd\pm}(\overline{WE})$	Delay $\overline{WE}$ HIGH to Output Active			12		25	ns
$t_{pdz}(\overline{WE})$	Delay $\overline{WE}$ LOW to Output OFF			12		25	ns

*System requirement. Parameters preceeded by an asterisk are specified as system forcing requirements rather than device characteristics. In general, minimum system requirements result from maximum device characteristics. Typical values are not meaningful for system requirements.

DEFINITION OF TERMS

FUNCTIONAL TERMS

$\overline{CS}$ Active LOW chip select input. When the chip select is LOW data can be read from or written into the memory.

D_i The data inputs of the memory. i = 1 – 4

O_i The data outputs of the memory, i = 1 – 4

$O_i(t_n)$ The state of output i at time n.

$D_i(t_{n-x})$ The state of the D_i input at time t_{n-x}, where t_{n-x} is the time of the last write operation into a given address.

$\overline{WE}$ Active LOW Write Enable. When the write enable is LOW, data on the data inputs is written into the addressed memory location. When $\overline{WE}$ is HIGH data is read from the addressed location and appears, inverted, at the $\overline{O}$ outputs.

UNIT LOAD A TTL input unit load is defined as −1.6mA at 0.4V (LOW state) and 40μA at 2.4V (HIGH state).

SWITCHING TERMS

$t_{pd\pm}(\overline{CS})$ The delay from the chip select input going LOW to the output going active.

$t_{pdz}(\overline{CS})$ The delay from the chip select going HIGH to the output assuming an inactive high impedance level.

$t_{pd\pm}(A)$ The delay from a change on the address inputs to a correct HIGH (t_{pd+}) or LOW (t_{pd-}) level on the outputs. Access time.

$t_{rec}(\overline{WE})$ Write recovery time. The delay from a LOW-to-HIGH transition on the write enable to the correct data on the outputs of the memory. This is the time required between the end of the write operation and a read operation in the same address.

* $t_{pw}(\overline{WE})$ Minimum write pulse width. The LOW time on the write enable input required to cause a write.

* $t_s(D)$,* $t_h(D)$ Data set-up and hold times. The time, relative to the end of the write pulse (LOW-to-HIGH edge) after which the data on the data inputs will not be written into the memory. To ensure writing the correct data, the data must be present before * $t_s(D)$ min. and must remain until after * $t_h(D)$ min.

* $t_s(A)$ Address set-up time. The time prior to the start of the write pulse (HIGH-to-LOW edge) at which the correct write address must be on the address inputs. An address change later than * $t_s(A)$ max. may cause writing in two addresses.

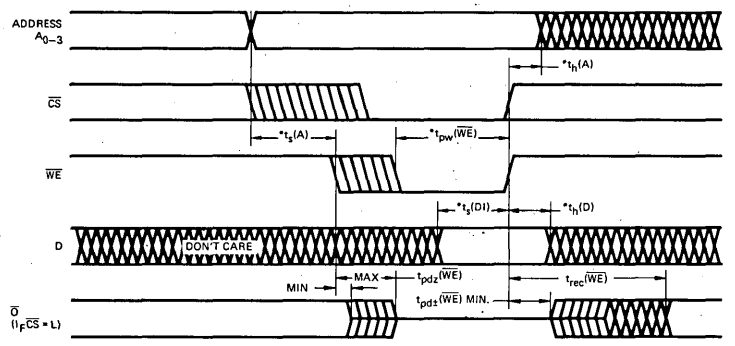
* $t_h(A)$ Address hold time. The time following the end of the write pulse (LOW-to-HIGH transition) at which a new address may be applied. An address change earlier than * $t_h(A)$ min. may cause writing into two addresses.

$t_{pd\pm}(\overline{WE})$ The delay from a LOW-to-HIGH transition of the write enable to an active (but not necessarily correct) state on the data outputs. The correct state will be present after the write recovery time has elapsed.

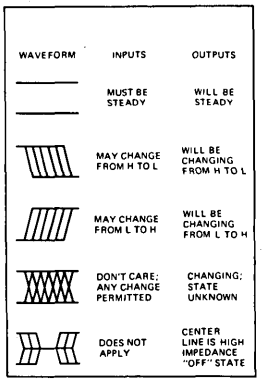
$t_{pdo}(\overline{WE})$ The delay from a HIGH-to-LOW transition on the write enable to a high impedance level on the data outputs, if the chip is selected.

*System requirement. Parameters preceeded by an asterisk are specified as system forcing requirements rather than device characteristics. In general, minimum system requirements result from maximum device characteristics. Typical values are not meaningful for system requirements.

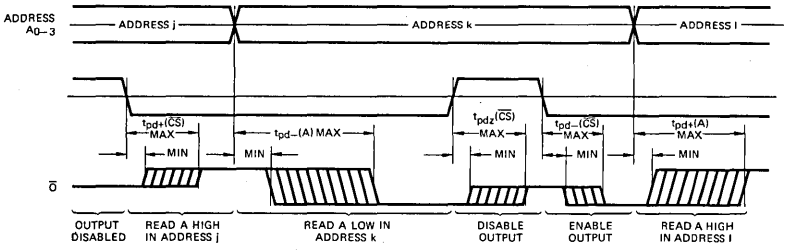
SWITCHING WAVEFORMS



KEY TO TIMING DIAGRAM



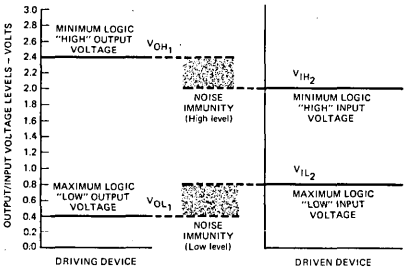
Write Cycle Timing. The cycle is initiated by an address change. After $^*t_s(A)$ min., the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, $^*t_h(A)$ min. must be allowed before the address may be changed again. The output will be inactive (floating for the Am27S03) while the write enable is LOW. The three parameters $t_s(A)$, $t_h(A)$ and $t_{pw}(WE)$ apply to the condition CS LOW AND WE LOW.

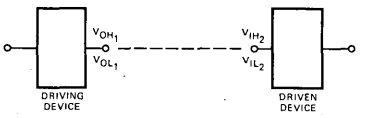


Switching delays from address and chip select inputs to the data output. For the Am27S03 disabled output is "OFF", represented by a single center line. For the Am27S02, a disabled output is HIGH.

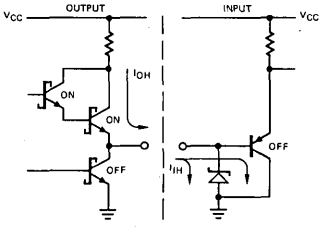
INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions – LOW & HIGH



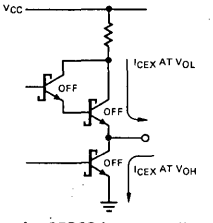


Current Conditions – HIGH State



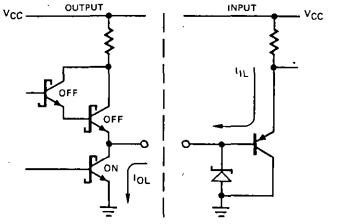
Note: Am27S02 is open collector

Currents Conditions – OFF State



Note: Am27S02 is open collector

Current Conditions – LOW State



USER NOTES

1. The Am27S03 output has active circuitry for both logic levels and requires no external pull-up resistor.
2. For a good DC noise margin with the Am3101A/27S02 a pull-up resistor can be used. Limits of R in kΩ are given by

$$\frac{V_{CC}-V_{OH}\text{ required}}{nI_{CEX}+NI_{IH}} > R_L > \frac{V_{CC}-V_{OL}\text{ required}}{I_{OL}-NI_{IL}}$$

   Where n is number of OR tied outputs
   N is the number of TTL units loads driven.

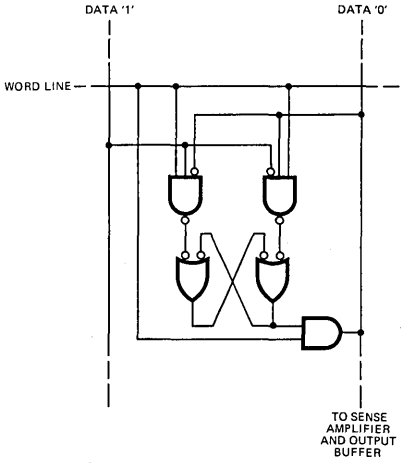
3. Address and data lines can be interchanged within their respective groups for ease of P. C. layout without effecting device operation.
4. Since for a given pattern on the address lines reading and writing are performed on the same actual memory word, the address lines can be driven by any mixture of assertion or negation of the variables making up the address field.

Am3101A LOADING RULES (In TTL Loads)

Input/Output	Pin No.'s	Input Loading	Output Drive (Am27S03) HIGH	LOW
A_0	1	.16	–	–
$\overline{CS}$	2	.16	–	–
$\overline{WE}$	3	.16	–	–
D_0	4	.16	–	–
$\overline{O}_0$	5	–	20	10
D_1	6	.16	–	–
$\overline{O}_1$	7	–	20	10
GND	8	–	–	–
$\overline{O}_2$	9	–	20	10
D_2	10	.16	–	–
$\overline{O}_3$	11	–	20	10
D_3	12	.16	–	–
A_3	13	.16	–	–
A_2	14	.16	–	–
A_1	15	.16	–	–
V_{CC}	16	–	–	–

A TTL unit load is −1.6mA at 0.4V and 40μA at 2.0V.
The Am27S02 has open collector outputs; the output drive in the HIGH state is determined by an external pull-up resistor.

BASIC MEMORY CELL



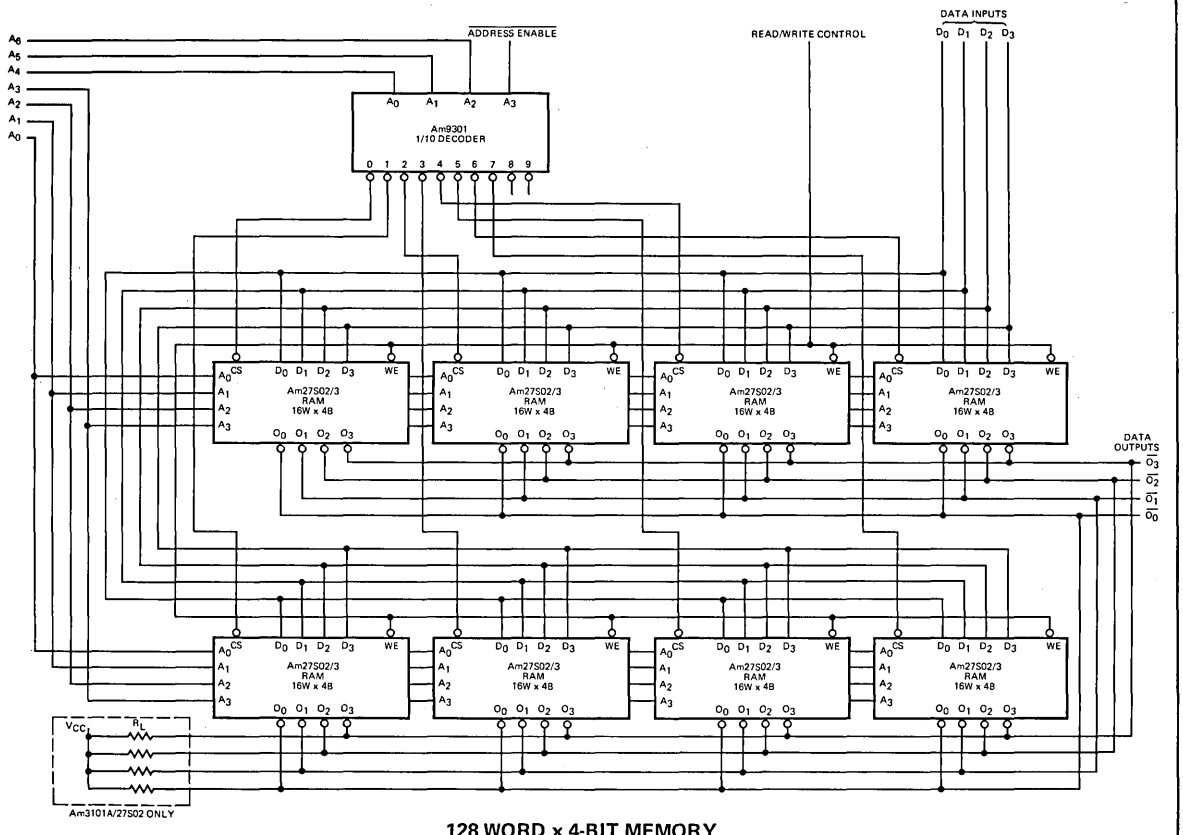
TRUTH TABLE

INPUTS			OUTPUTS	MODE
$\overline{CS}$	$\overline{WE}$	D_i	$\overline{O}_i(t_n)$	
H	L	L	Off	No Selection
H	L	H	Off	No Selection
H	H	X	Off	No Selection
L	L	L	Off	Write '0'
L	L	H	Off	Write '1'
L	H	X	$\overline{D}_i(t_{n-x})$	Read

H = HIGH Voltage Level
L = LOW Voltage Level
OFF = HIGH Impedance

Note: The Am27S02 output is at a high impedance level *at all times except when reading a LOW.*

Am3101A/27S02/27S03 APPLICATION

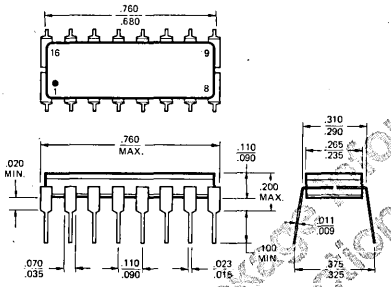


128 WORD x 4-BIT MEMORY

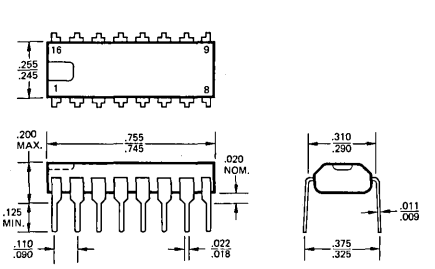
PHYSICAL DIMENSIONS

Dual-In-Line

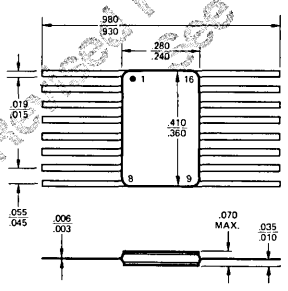
Hermetic



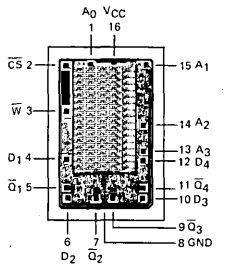
Molded



Flat Package



Metallization and Pad Layout



DIE SIZE 85 X 131 mils

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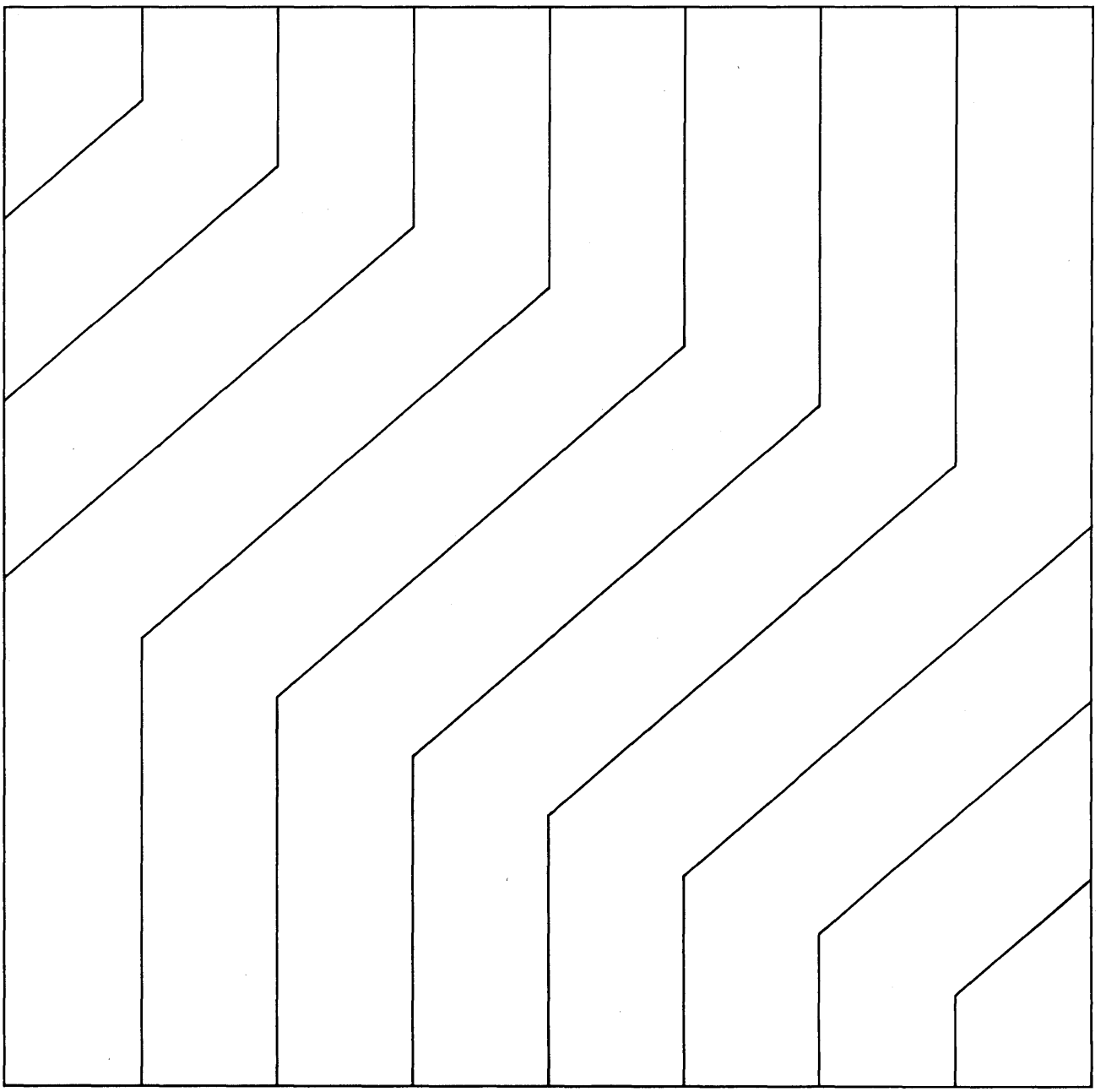
TWX: 910-339-9280
TELEX: 34-6306



Am101/201/301
Operational Amplifier

Description: The Am101/201/301 monolithic operational amplifiers are functionally, electrically and pin-for-pin equivalent to the National LM101, and LM201. They are available in the hermetic TO-99 metal can, dual-in-line packages, and flat packages.

Distinctive Characteristics: 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL STD 883 Class B.

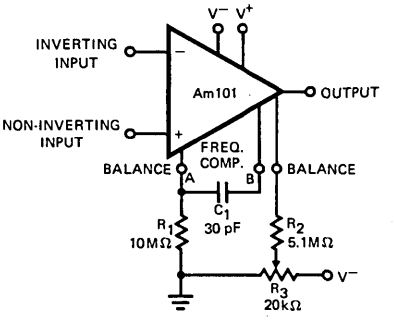
Mixing privileges for obtaining price discounts. Refer to price list.

Electrically tested and optically inspected dice for the assemblers of hybrid products.

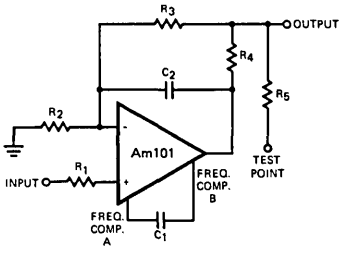
FUNCTIONAL DESCRIPTION

The Am101/201/301 are differential input, class AB output operational amplifiers. The inputs and outputs are protected against overload and the amplifiers may be frequency compensated with an external 30pF capacitor.

FUNCTIONAL DIAGRAM



APPLICATIONS



INPUT/OUTPUT OVERLOAD PROTECTION

If an input is driven from a low-impedance source, a series resistor, R_i should be used to limit the peak instantaneous output current of the source to less than 100 mA. A large capacitor (>0.1μF) is equivalent to a low source impedance and should be protected against by an isolation resistor.

The amplifier output is protected against damage from shorts to ground or to the power supplies by device design. Protection of the output from voltages exceeding the specified operating power supplies can be obtained by isolating the output via limiting resistors R_4 or R_5.

The power supplies must never become reversed, even under transient conditions. Reverse voltages as low as 1 volt can cause damage through excessive current. This hazard can be reduced by using clamp diodes of high peak current rating connected to the device supply lines.

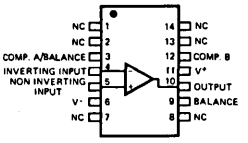
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am301	DIP	0°C - 70°C	LM301D
	Metal Can	0°C - 70°C	LM301
Am201	DIP	−25°C - 85°C	LM201D
	Metal Can	−25°C - 85°C	LM201
	Flat Pak	−25°C - 85°C	LM201F
Am101	DIP	−55°C - 125°C	LM101D
	Metal Can	−55°C - 125°C	LM101
	Flat Pak	−55°C - 125°C	LM101F
Am101	Dice	Note 4	LMD01

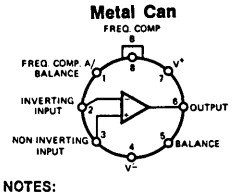
Note 4: The dice supplied will contain units which meet 0°C to +70°C, −25°C to +85°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAMS
Top Views

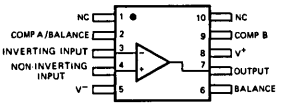
Dual-In-Line



Metal Can



Flat Package



NOTES:

(1) On Metal Can, pin 4 is connected to case.

(2) On DIP, pin 6 is connected to bottom of package.

(3) On Flat Package, pin 5 is connected to bottom of package.

MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
Am101	−55°C to +125°C
Am201	−25°C to +85°C
Am301	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 3)

Parameter (see definitions)	Conditions	Am301 Min	Am301 Typ	Am301 Max	Am101 Am201 Min	Am101 Am201 Typ	Am101 Am201 Max	Units
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	7.5		1.0	5.0	mV
Input Offset Current			100	500		40	200	nA
Input Bias Current			250	1500		120	500	nA
Input Resistance		0.1	0.4		0.3	0.8		MΩ
Supply Current	$V_S = \pm 20V$		1.8	3.0		1.8	3.0	mA
Large Signal Voltage Gain	$V_S = \pm 15V, V_{OUT} = \pm 10V$, $R_L > 2$ kΩ	20	150		50	160		V/mV
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 10$ kΩ			10			6.0	mV
Input Offset Current	$T_A = T_{A\,(min)}$ $T_A = T_{A\,(max)}$		150 50	750 400		100 10	500 200	nA nA
Input Bias Current	$T_A = T_{A\,(min)}$		0.32	2		0.28	1.5	μA
Large Signal Voltage Gain	$V_S = \pm 15$ V, $V_{OUT} = \pm 10$ V, $R_L > 2$ kΩ	15			25			V/mV
Input Voltage Range	$V_S = \pm 15$ V	±12			±12			V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	65	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Output Voltage Swing	$V_S = \pm 15$ V, $R_L = 10$ kΩ, $R_L = 2$ kΩ	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
Supply Current	$T_A = +125°C$ $V_S = \pm 20$ V					1.2	2.5	mA

DEFINITION OF TERMS

COMMON MODE REJECTION RATIO The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

INPUT BIAS CURRENT The average of the two input currents.

INPUT OFFSET CURRENT The difference in the currents into the two input terminals when the output is at zero.

INPUT OFFSET VOLTAGE That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

INPUT RESISTANCE The ratio of the change in input voltage to the change in input current on either input with the other grounded.

INPUT VOLTAGE RANGE The range of voltages on the input terminals for which the offset specifications apply.

LARGE-SIGNAL VOLTAGE GAIN The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT RESISTANCE The resistance seen looking into the output terminal with the output at null.

OUTPUT SHORT-CIRCUIT CURRENT The maximum output current available from the amplifier with the output shorted to ground or to either supply.

OUTPUT VOLTAGE SWING The peak output voltage swing, referred to zero, that can be obtained without clipping.

POWER SUPPLY REJECTION RATIO The ratio of the change in input offset voltage to the change in power supply voltages producing it.

SUPPLY CURRENT The current required from the power supply to operate the amplifier with no load and the output at zero.

Note 1: Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C and the Dual In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C, and the Flat Package at 5.4 mW/°C for operation at ambient temperatures above 57°C.

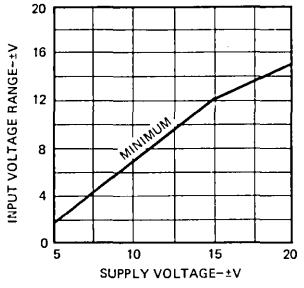
Note 2: For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.

Note 3: Unless otherwise specified, these specifications apply for supply voltages from ±5V to ±20V and C_i = 30pF.

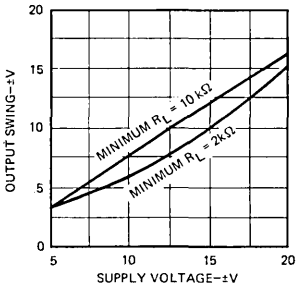
GUARANTEED PERFORMANCE CURVES

(Curves apply over the Operating Temperature Ranges)

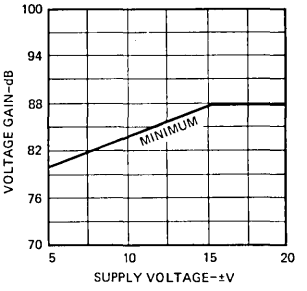
Input Voltage Range



Output Swing

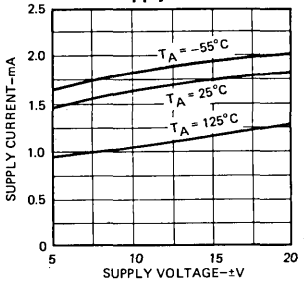


Voltage Gain

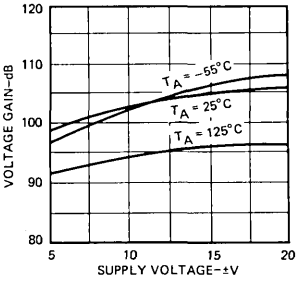


PERFORMANCE CURVES

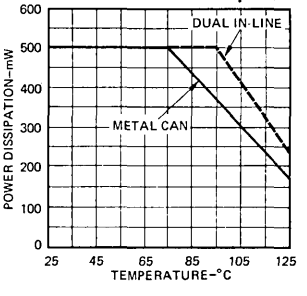
Supply Current



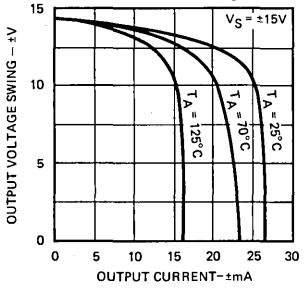
Voltage Gain



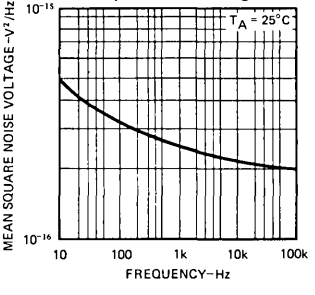
Maximum Power Dissipation



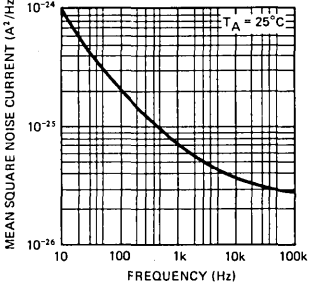
Current Limiting



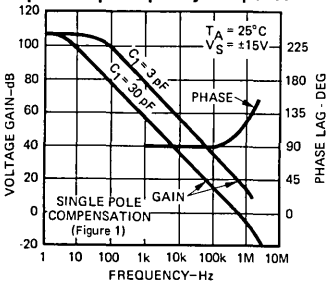
Input Noise Voltage



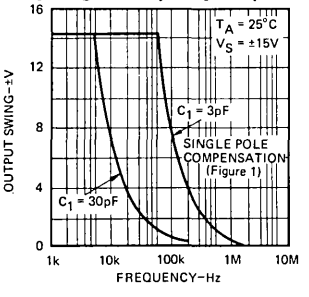
Input Noise Current



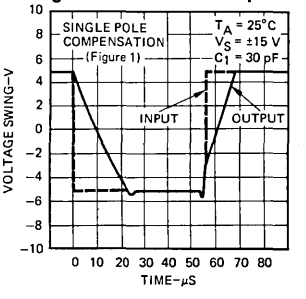
Open Loop Frequency Response



Large Signal Frequency Response

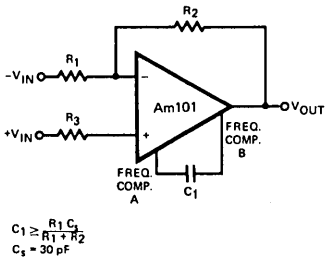


Voltage Follower Pulse Response



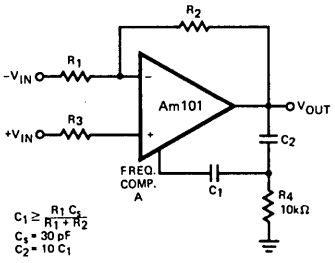
FREQUENCY COMPENSATION CIRCUITS

Single Pole Compensation



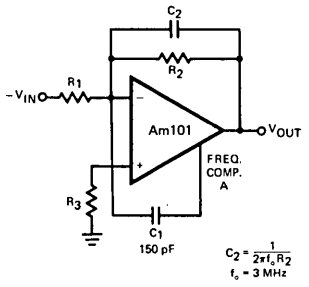
$C_1 \geq \frac{R_1 C_1}{R_1 + R_2}$
$C_S = 30$ pF

Two Pole Compensation



$C_1 \geq \frac{R_1 C_1}{R_1 + R_2}$
$C_S = 30$ pF
$C_2 = 10\,C_1$

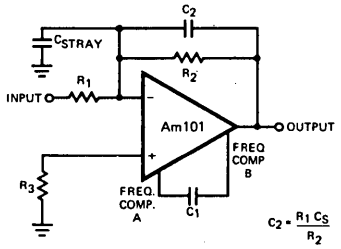
Feedforward Compensation



$C_2 = \frac{1}{2\pi f_o R_2}$
$f_o = 3$ MHz

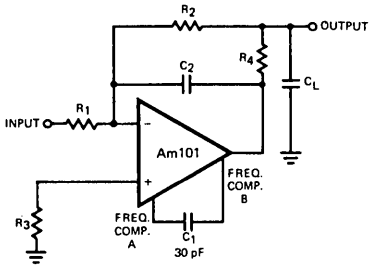
Power supplies should be bypassed to ground at one point, minimum, on each card. More bypass points should be considered for five or more amplifiers on a single card. For applications using feed-forward compensation, the power supply leads of each amplifier should be bypassed with low inductance capacitors.

Compensating for Stray Input Capacitance/Large Feedback Resistance



$C_2 = \frac{R_1 C_S}{R_2}$

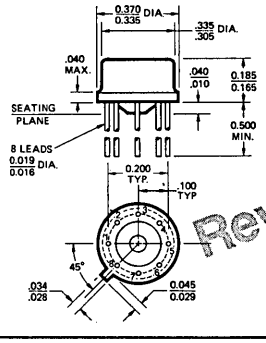
Isolating Large Capacitive Loads



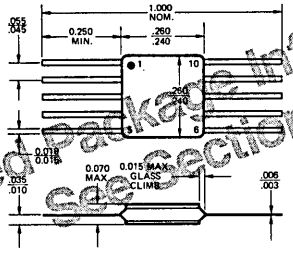
The values given for the frequency compensation capacitor guarantee stability only for source resistances less than 10kΩ, stray capacitances on the summing junction less than 5pF and capacitive loads smaller than 100pF. If any of these conditions is not met, it is necessary to use a larger compensation capacitor. Alternately, lead capacitors can be used in the feedback network to negate the effect of stray capacitance and large feedback resistors, or an RC network can be added to isolate capacitive loads.

PHYSICAL DIMENSIONS

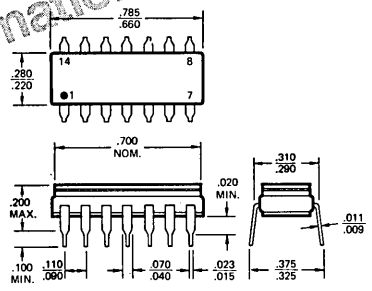
Metal Can



Flat Package



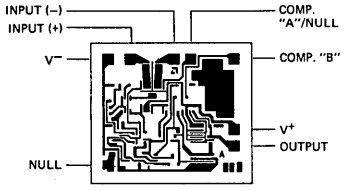
Dual-In-Line



Note: All dimensions are in inches.
Leads are gold plated Kovar.

Metallization and Pad Layout

49 x 56 Mils



ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am101A/201A/301A
Operational Amplifier

Description: The Am101A, Am201A and Am301A monolithic operational amplifiers are functionally, electrically and pin-for-pin equivalent to the National LM101A, LM201A, and LM301A. They are available in the hermetic TO-99 metal can, dual-in-line, and flat packages.

Distinctive Characteristics: 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL-STD-883.

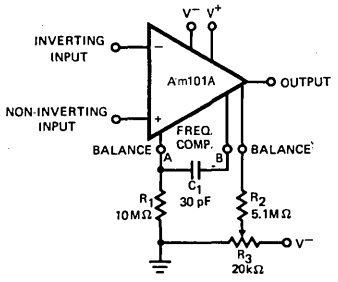
Mixing privileges for obtaining price discounts. Refer to price list.

Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

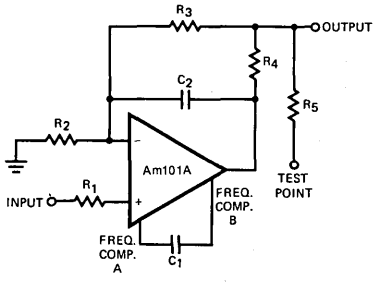
The Am101A/Am201A/Am301A are differential input, class AB output operational amplifiers. The inputs and outputs are protected against overload and the amplifiers may be frequency compensated with an external 30pF capacitor. The combination of low-input currents, low-offset voltage, low noise, and versatility of compensation classify the Am101A/Am201A/Am301A amplifiers for low level and general purpose applications.

FUNCTIONAL DIAGRAM



APPLICATIONS

INPUT/OUTPUT OVERLOAD PROTECTION



If an input is driven from a low-impedance source, a series resistor, R_1 should be used to limit the peak instantaneous output current of the source to less than 100 mA. A large capacitor (>0.1μF) is equivalent to a low-source impedance and should be protected against by an isolation resistor.

The amplifier output is protected against damage from shorts to ground or to the power supplies by device design. Protection of the output from voltages exceeding the specified operating power supplies can be obtained by isolating the output via limiting resistors R_4 or R_5.

The power supplies must never become reversed, even under transient conditions. Reverse voltages as low as 1 volt can cause damage through excessive current. This hazard can be reduced by using clamp diodes of high peak current rating connected to the device supply lines.

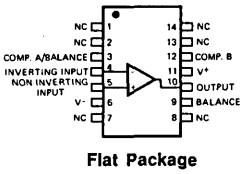
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am301A	DIP	0°C - 70°C	LM301AD
	Metal Can	0°C - 70°C	LM301A
Am201A	DIP	−25°C - 85°C	LM201AD
	Metal Can	−25°C - 85°C	LM201A
	Flat Pak	−25°C - 85°C	LM201AF
Am101A	DIP	−55°C - 125°C	LM101AD
	Metal Can	−55°C - 125°C	LM101A
	Flat Pak	−55°C - 125°C	LM101AF
Am101A	Dice	Note 4	LMD01A

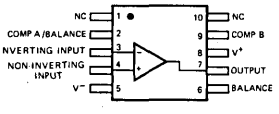
Note 4: The dice supplied will contain units which meet 0°C to +70°C, −25°C to +85°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAMS
Top Views

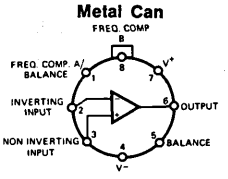
Dual-In-Line



Flat Package



Metal Can



NOTES:

(1) On Metal Can, pin 4 is connected to case.

(2) On DIP, pin 6 is connected to bottom of package.

(3) On Flat Package, pin 5 is connected to bottom of package.

MAXIMUM RATINGS

Supply Voltage	
Am101A, 201A	±22V
Am301A	±18V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
Am101A	−55°C to +125°C
Am201A	−25°C to +85°C
Am301A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 3)

Parameter (see definitions)	Conditions	Am301A Min	Am301A Typ	Am301A Max	Am101A Am201A Min	Am101A Am201A Typ	Am101A Am201A Max	Units
Input Offset Voltage	$R_S \leq 50\ k\Omega$		2.0	7.5		0.7	2.0	mV
Input Offset Current			3	50		1.5	10	nA
Input Bias Current			70	250		30	75	nA
Input Resistance		0.5	2		1.5	4		MΩ
Supply Current	$V_S = \pm 20V$ $V_S = \pm 15V$		1.8	3.0		1.8	3.0	mA mA
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $V_{OUT} = \pm 10\ V$, $R_L > 2\ k\Omega$	25	160		50	160		V/mV
Slew Rate	$V_S = \pm 20V$, $A_V = +1$	0.2	0.5		0.2	0.5		V/μs
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 50\ k\Omega$			10			3.0	mV
Input Offset Current				70			20	nA
Average Temperature Coefficient of Input Offset Voltage	$T_{A(min)} \leq T_A \leq T_{A(max)}$		6.0	30		3.0	15	μV/°C
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq T_{A\ (max)}$ $T_{A\ (min)} \leq T_A \leq 25°C$		0.01 0.02	0.3 0.6		0.01 0.02	0.1 0.2	nA/°C nA/°C
Input Bias Current				300			100	nA
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $V_{OUT} = \pm 10\ V$, $R_L > 2\ k\Omega$	25			25			V/mV
Input Voltage Range	$V_S = \pm 20\ V$ $V_S = \pm 15\ V$	+15, −12			±15			V V
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$	70	90		80	96		dB
Supply Voltage Rejection Ratio	$R_S \leq 50\ k\Omega$	70	96		80	96		dB
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$, $R_L = 2\ k\Omega$,	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
Supply Current	$T_A = +125°C$ $V_S = \pm 20\ V$					1.2	2.5	mA

DEFINITION OF TERMS

AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET CURRENT The ratio of the change in Input Offset Current over the operating temperature range to the temperature range.

AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET VOLTAGE The ratio of the change in Input Offset Voltage over the operating temperature range to the temperature range.

COMMON MODE REJECTION RATIO The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

INPUT BIAS CURRENT The average of the two input currents.

INPUT OFFSET CURRENT The difference in the currents into the two input terminals when the output is at zero.

INPUT OFFSET VOLTAGE That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

INPUT RESISTANCE The ratio of the change in input voltage to the change in input current on either input with the other grounded.

INPUT VOLTAGE RANGE The range of voltages on the input terminals for which the offset specifications apply.

LARGE-SIGNAL VOLTAGE GAIN The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT RESISTANCE The resistance seen looking into the output terminal with the output at null.

OUTPUT SHORT-CIRCUIT CURRENT The maximum output current available from the amplifier with the output shorted to ground or to either supply.

OUTPUT VOLTAGE SWING The peak output voltage swing, referred to zero, that can be obtained without clipping.

POWER SUPPLY REJECTION RATIO The ratio of the change in input offset voltage to the change in power supply voltages producing it.

SUPPLY CURRENT The current required from the power supply to operate the amplifier with no load and the output at zero.

NOTES

Note 1: Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C and the Dual In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C, and the Flat Package at 5.4 mW/°C for operation at ambient temperatures above 57°C.

Note 2: For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.

Note 3: Unless otherwise specified, these specifications apply for supply voltages from ±5V to ±20V for the 101A and 201A, and from ±5V to ±15V for the 301A.

FREQUENCY COMPENSATION CIRCUITS

Single Pole Compensation

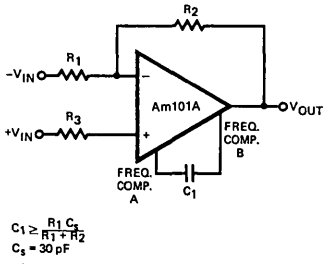


Figure 1

Two Pole Compensation

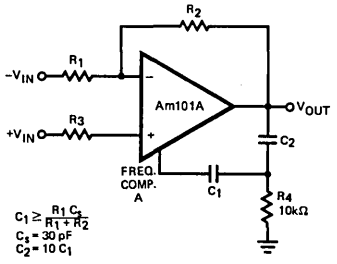


Figure 2

Feedforward Compensation

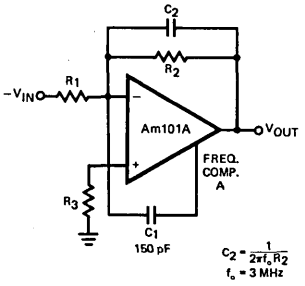


Figure 3

Power supplies should be bypassed to ground at one point, minimum, on each card. More bypass points should be considered for five or more amplifiers on a single card. For applications using feed-forward compensation, the power supply leads of each amplifier should be bypassed with low inductance capacitors.

Compensating for Stray Input Capacitance/Large Feedback Resistance

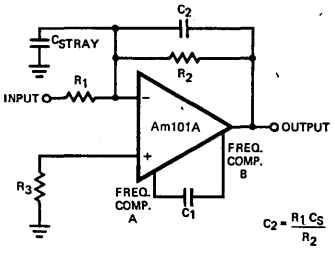


Figure 4

Isolating Large Capacitive Loads

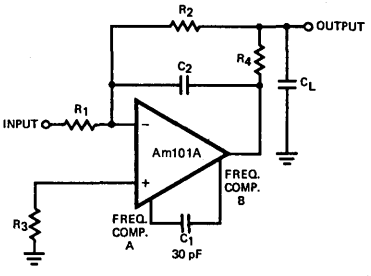
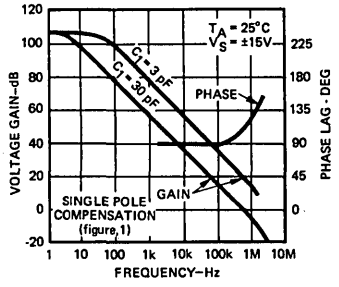


Figure 5

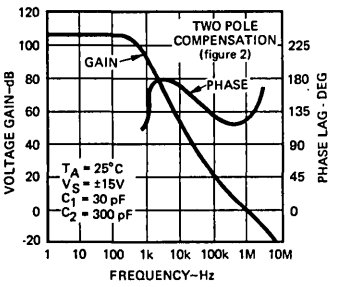
The values given for the frequency compensation capacitor guarantee stability only for source resistances less than 10kΩ, stray capacitances on the summing junction less than 5pF and capacitive loads smaller than 100pF. If any of these conditions is not met, it is necessary to use a larger compensation capacitor. Alternately, lead capacitors can be used in the feedback network to negate the effect of stray capacitance and large feedback resistors, or an RC network can be added to isolate capacitive loads.

PERFORMANCE CURVES (Note 3)

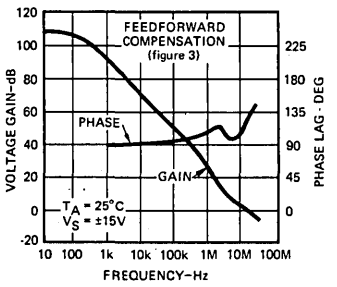
Open Loop Frequency Response



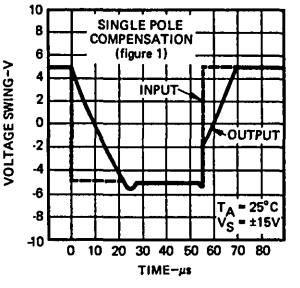
Open Loop Frequency Response



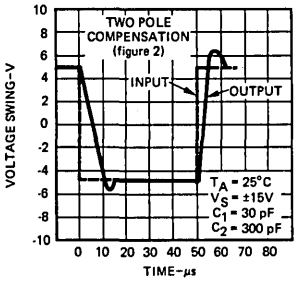
Open Loop Frequency Response



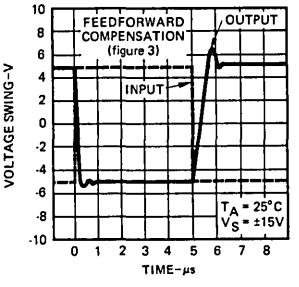
Voltage Follower Pulse Response



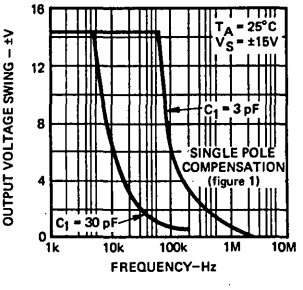
Voltage Follower Pulse Response



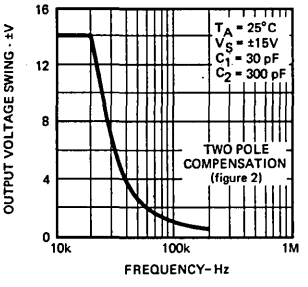
Inverter Pulse Response



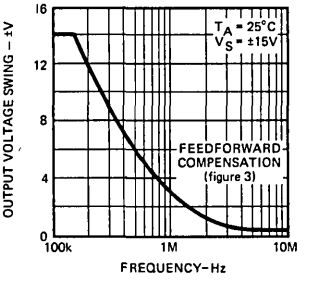
Large Signal Frequency Response



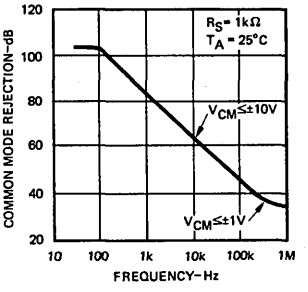
Large Signal Frequency Response



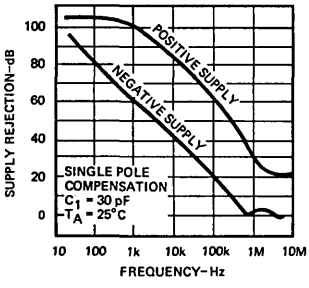
Large Signal Frequency Response



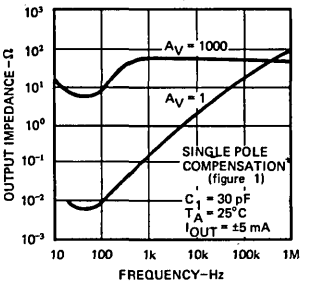
Common Mode Rejection



Power Supply Rejection



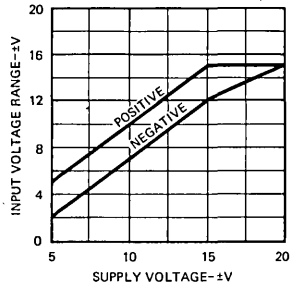
Closed Loop Output Impedance



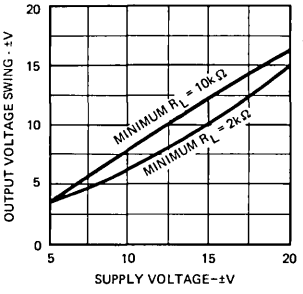
GUARANTEED PERFORMANCE CURVES (Note 3)

(Curves apply over the Operating Temperature Ranges)

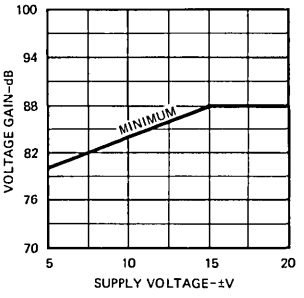
Input Voltage Range



Output Swing

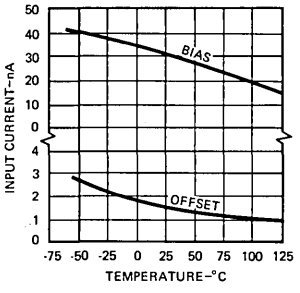


Voltage Gain

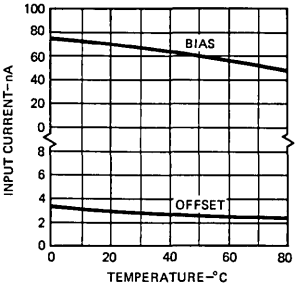


PERFORMANCE CURVES (Note 3)

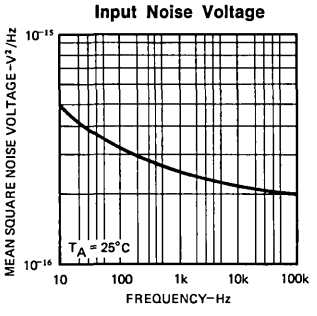
Input Current—101A, 201A



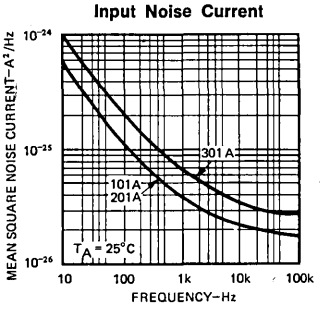
Input Current—301A



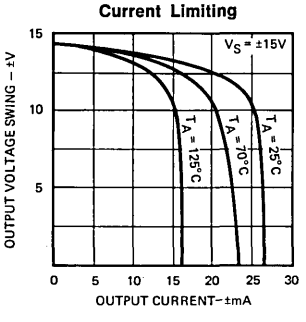
Input Noise Voltage



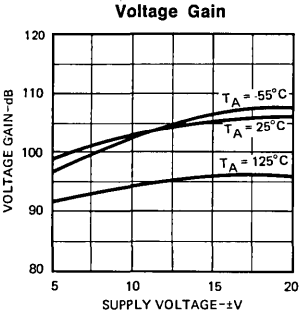
Input Noise Current



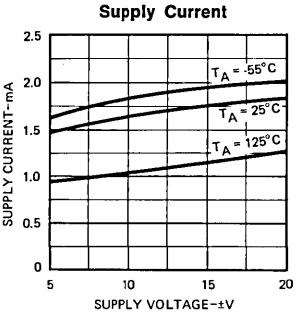
Current Limiting



Voltage Gain

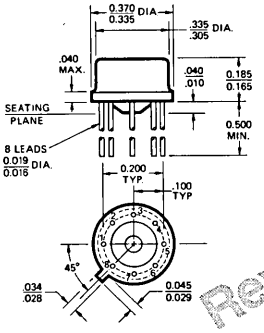


Supply Current

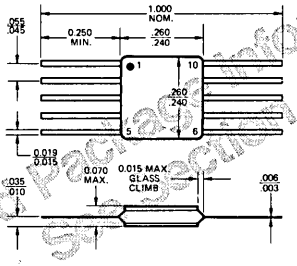


PHYSICAL DIMENSIONS

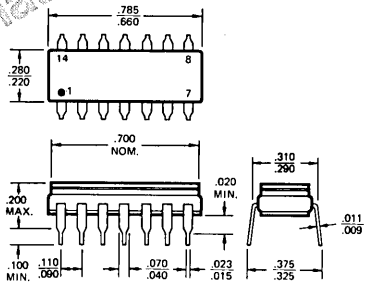
Metal Can



Flat Package

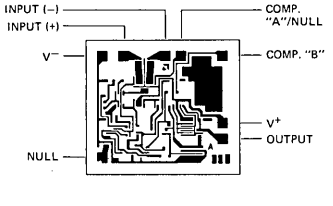


Dual-In-Line



Note: All dimensions are in inches.
Leads are gold plated Kovar.

Metallization and Pad Layout



49 x 56 Mils

ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am105/205/305/305A
Voltage Regulator

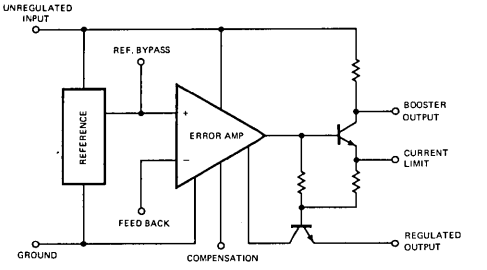
Distinctive Characteristics

- The Am105/205/305/305A are functionally, electrically, and pin-for-pin equivalent to the National LM 105/205/305/305A.
- Output voltage adjustable from 4.5V to 40V.
- Output currents in excess of 10A possible by adding external transistors.
- 100% reliability assurance testing in compliance with MIL STD 883.
- Electrically tested and optically inspected die for assemblers of hybrid products.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Available in metal can and hermetic flat package.

FUNCTIONAL DESCRIPTION

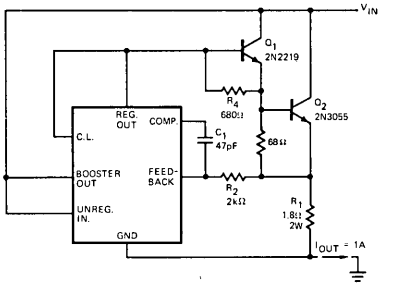
The Am105/205/305/305A is a positive voltage regulator which can be used in the series, shunt, linear or switching modes of operation. The circuits feature low stand-by current drain, operation under minimum load conditions and an output current capability of up to 20 mA.

FUNCTIONAL DIAGRAM

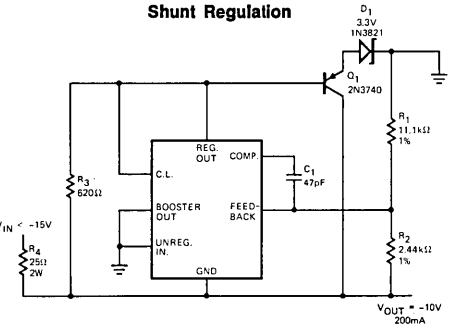


TYPICAL APPLICATIONS

Current Regulator



Shunt Regulation



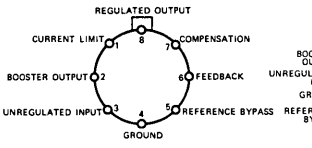
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am305A	Metal Can	0°C to 70°C	LM305A
Am305	Metal Can	0°C to 70°C	LM305
Am205	Metal Can	−25°C to 85°C	LM205
	Flat Pak	−25°C to 85°C	LM205F
Am105	Metal Can	−55°C to 125°C	LM105
	Flat Pak	−55°C to 125°C	LM105F
Am105	Dice	Note 4	LMD05

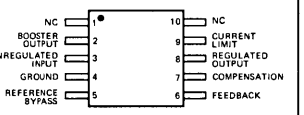
Note 4: The dice supplied will contain units which meet 0°C to +70°C, −25°C to +85°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top Views

Metal Can



Flat Package



NOTES: (1) On Metal Can, pin 4 is connected to case.
(2) On Flat Package, pin 4 is connected to bottom of package.

MAXIMUM RATINGS

Input Voltage Range	Am105/205/305A	50 V
	Am305	40 V
Input-Output Voltage Differential		40 V
Internal Power Dissipation (Note 1)		
Metal Can (Similar to TO-99) and Flatpak Am105/205/305		500 mW
Metal Can (Similar to TO-99) Am305A		800 mW
Operating Temperature Range		
Am105		−55°C to +125°C
Am205		−25°C to +85°C
Am305/305A		0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)		300°C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise specified) (Note 2)

Parameter (see definitions)	Conditions	Am305 Min	Am305 Typ	Am305 Max	Am305A Min	Am305A Typ	Am305A Max	Am105 Am205 Min	Am105 Am205 Typ	Am105 Am205 Max	Units
Input Voltage Range		8.5		40	8.5		50	8.5		50	V
Output Voltage Range		4.5		30	4.5		40	4.5		40	V
Input-Output Voltage Differential		3.0		30	3.0		30	3.0		30	V
Line Regulation (Note 3)	$V_{in} - V_{out} \leq 5$ V		0.025	0.06		0.025	0.06		0.025	0.06	%/V
	$V_{in} - V_{out} \geq 5$ V		0.015	0.03		0.015	0.03		0.015	0.03	%/V
Load Regulation (Note 3)	$0 \leq I_O \leq 12$ mA										
	$R_{SC} = 18\,\Omega$, $T_A = 25°C$		0.02	0.05					0.02	0.05	%
	$R_{SC} = 15\,\Omega$, $T_A = T_A$(max)		0.03	0.1							%
	$R_{SC} = 10\,\Omega$, $T_A = T_A$(max)								0.03	0.01	%
	$R_{SC} = 18\,\Omega$, $T_A = T_A$(min)		0.03	0.1					0.03	0.1	%
	$0 \leq I_O \leq 45$ mA										
	$R_{SC} = 0\,\Omega$, $T_A = 25°C$					0.02	0.2				%
	$R_{SC} = 0\,\Omega$, $T_A = T_A$ (max)					0.03	0.4				%
	$R_{SC} = 0\,\Omega$, $T_A = T_A$ (min)					0.03	0.4				%
Feedback Sense Voltage		1.63	1.70	1.81	1.55	1.70	1.85	1.63	1.70	1.81	V
Ripple Rejection	$C_{REF} = 10\,\mu$f, f = 120 Hz		0.003	0.01		0.003			0.003	0.01	%/V
Output Noise Voltage	10 Hz $\leq$ f $\leq$ 10 kHz										
	$C_{REF} = 0$		0.005			0.005			0.005		%
	$C_{REF} > 0.1\,\mu$f		0.002			0.002			0.002		%
Standby Current Drain	$V_{in} = 40$ V		0.8	2.0							
	$V_{in} = 50$ V					0.8	2.0		0.8	2.0	mA
Long Term Stability			0.1	1.0		0.1	1.0		0.1	1.0	%
Temperature Stability			0.3	1.0		0.3	1.0		0.3	1.0	%
Current Limit Sense Voltage (Note 4)	$R_{SC} = 10\,\Omega$, $T_A = 25°C$, $V_{out} = 0$ V	225	300	375							mV

DEFINITION OF TERMS

INPUT VOLTAGE RANGE The range of dc input voltages over which the regulator will operate within specifications.

OUTPUT VOLTAGE RANGE The range of regulated output voltages over which the specifications apply.

OUTPUT-INPUT VOLTAGE DIFFERENTIAL The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate within specifications.

LINE REGULATION The percentage change in regulated output voltage for a change in input voltage.

RIPPLE REJECTION The line regulation for ac input signals at or above a given frequency with a specified value of bypass capacitor on the reference bypass terminal.

LOAD REGULATION The percentage change in regulated output voltage for a change in load from zero to the maximum load current specified.

CURRENT-LIMIT SENSE VOLTAGE The voltage across the current limit terminals required to cause the regulator to current-limit with a short circuited output. This voltage is used to determine the value of the external current-limit resistor when external booster transistors are used.

TEMPERATURE STABILITY The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

FEEDBACK SENSE VOLTAGE The voltage, referred to ground, on the feedback terminal of the regulator while it is operating in regulation.

OUTPUT NOISE VOLTAGE The average ac voltage at the output with constant load and no input ripple.

STANDBY CURRENT DRAIN That part of the operating current of the regulator which does not contribute to the load current.

Note 1: Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 25°C and the Flat Package at 5.4 mW/°C for operation at ambient temperatures above 57°C.

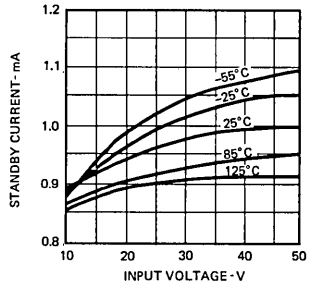
Note 2: These specifications apply over the operating temperature range , for input and output voltages within the ranges given, and for a divider impedance seen by the feedback terminal of 2 kΩ, unless otherwise specified. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

Note 3: The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.

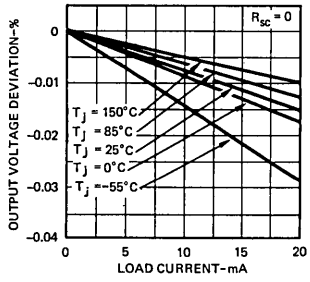
Note 4: With no external pass transistor.

PERFORMANCE CURVES

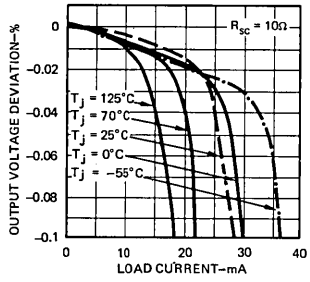
Standby Current Drain As A Function Of Input Voltage



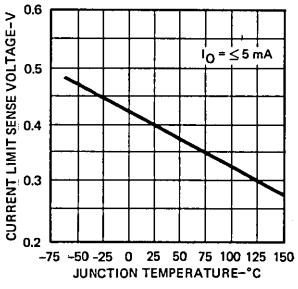
Load Regulation



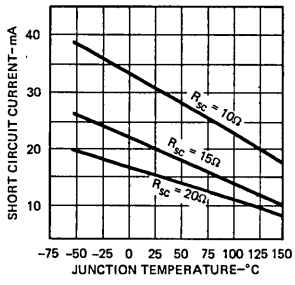
Load Regulation Characteristics With Current Limiting



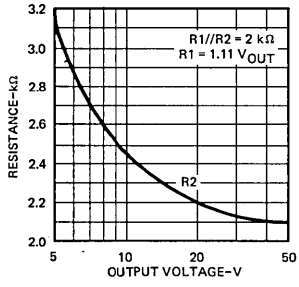
Current Limiting Sense Voltage As A Function of Junction Temperature



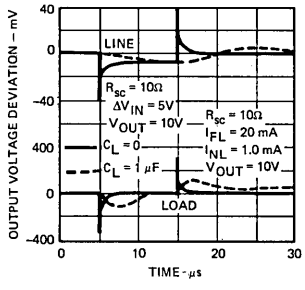
Short Circuit Current



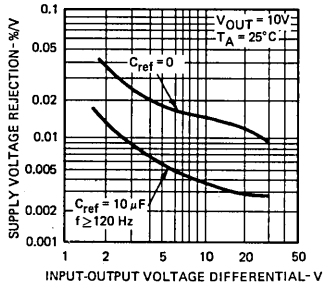
Optimum Divider Resistance Values



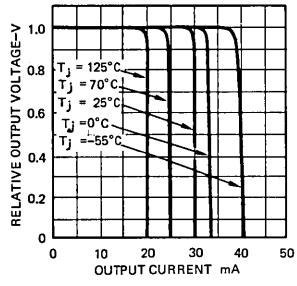
Transient Response



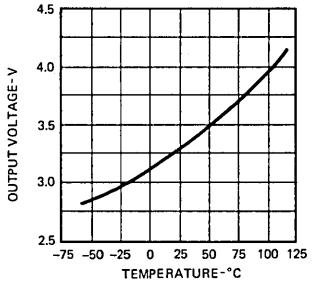
Supply Voltage Rejection



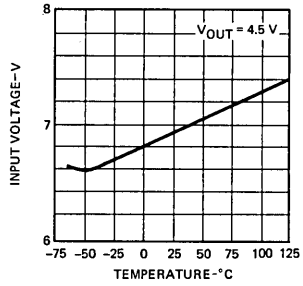
Current Limiting Characteristics



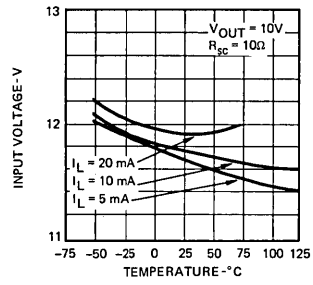
Minimum Output Voltage



Minimum Input Voltage

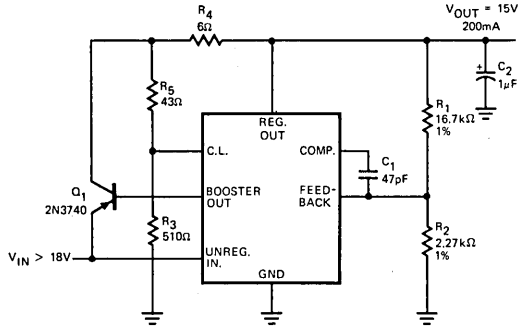


Regulator Dropout Voltage



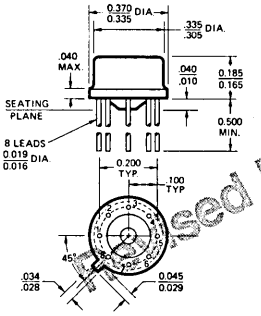
ADDITIONAL APPLICATIONS

Linear Regulator with Foldback Current Limiting

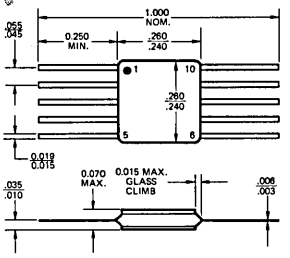


PHYSICAL DIMENSIONS

Metal Can



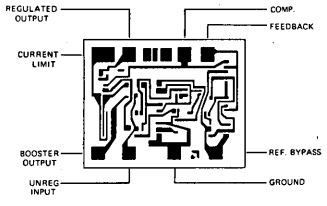
Flat Package



Note: All dimensions are in inches.
Leads are gold plated Kovar.

Metallization and Pad Layout

38 x 48 Mils



ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am106/206/306
Voltage Comparator/Buffer

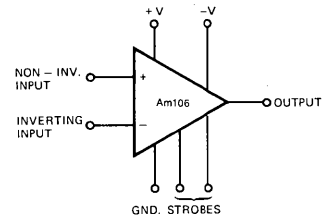
Distinctive Characteristics

- Functionally, electrically, and pin-for-pin equivalent to the National LM 106/206/306
- Drives RTL, DTL or TTL directly
- Output can switch voltages up to 24 V @ 100 mA
- Fan-out of 10 with DTL or TTL
- 100% reliability assurance testing in compliance with MIL STD 883.
- Electrically tested and optically inspected die for assemblers of hybrid products.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Available in metal can and hermetic flat package.

FUNCTIONAL DESCRIPTION

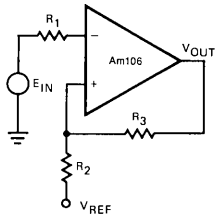
The Am106/206/306 are high-speed voltage comparators/buffers designed to be used in applications where high accuracy and fast response times are required. The device is useful as a pulse-height discriminator, relay or lamp driver or a line receiver.

FUNCTIONAL DIAGRAM



APPLICATION

Level Detector With Hysteresis



Upper and Lower Trip Points:

$$V_{UT} = V_{REF} + \frac{R_2 [V_{0\,MAX} - V_{REF}]}{R_2 + R_3}$$

and

$$V_{LT} = V_{REF} + \frac{R_2 [V_{0\,MIN} - V_{REF}]}{R_2 + R_3}$$

$$\text{Hysteresis} = V_H = V_{UT} - V_{LT} = \frac{R_2 [V_{0\,MAX} - V_{0\,MIN}]}{R_2 + R_3}$$

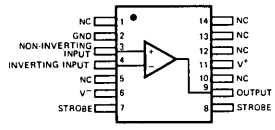
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am306	Metal Can	0°C to 70°C	LM306
Am206	Metal Can	−25°C to 85°C	LM206
Am106	Metal Can	−55°C to 125°C	LM106
	Flat Pak	−55°C to 125°C	LM106F
Am106	Dice	Note 4	LMD06

Note 4: The dice supplied will contain units which meet 0°C to +70°C, −25°C to +85°C and −55°C to +125°C temperature ranges.

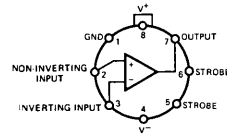
CONNECTION DIAGRAMS
Top Views

Flat Package



Note: Pin 6 connected to bottom of package.

Metal Can



Note: Pin 4 connected to case.

MAXIMUM RATINGS

Positive Supply Voltage	15 V
Negative Supply Voltage	−15 V
Output Voltage	24 V
Output to Negative Supply Voltage	30 V
Differential Input Voltage	±5 V
Input Voltage	±7 V
Power Dissipation (Note 1)	600 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	
Am106	−55°C to +125°C
Am206	−25°C to +85°C
Am306	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 60 sec)	300°C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise specified) (Note 2)

Parameter (see definitions)	Conditions	Am306 Min	Am306 Typ	Am306 Max	Am106 Am206 Min	Am106 Am206 Typ	Am106 Am206 Max	Units
Input Offset Voltage	Note 3		1.6	5.0		0.5	2.0	mV
Input Offset Current	Note 3		1.8	5.0		0.7	3.0	μA
Input Bias Current			16	25		10	20	μA
Voltage Gain			40			40		V/mV
Response Time	Note 4		40			40		ns
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{sink} = 100$ mA		0.8	2.0		1.0	1.5	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $8 V \leq V_{OUT} \leq 24 V$		0.02	2.0		0.02	1.0	μA
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	Note 3			6.5			3.0	mV
Average Temperature Coefficient of Input Offset Voltage	$T_{A(min)} \leq T_A \leq T_{A(max)}$		5.0	20		3.0	10	μV/°C
Input Offset Current	$T_A = T_{A(max)}$ Note 3, $T_A = T_{A(min)}$		0.6 2.4	5.0 7.5		0.25 1.8	3.0 7.0	μA μA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq T_{A(max)}$ $T_{A(min)} \leq T_A \leq 25°C$		15 24	50 100		5.0 15	25 75	nA/°C nA/°C
Input Bias Current				40			45	μA
Input Voltage Range	$-7 V \geq V^- \geq -12 V$	±5.0			±5.0			V
Differential Input Voltage Range		±5.0			±5.0			V
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{sink} = 50$ mA			1.0			1.0	V
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{sink} \leq 16$ mA			0.4			0.4	V
Positive Output Level	$V_{IN} \geq 5$ mV, $I_{OUT} = 400$ μA	2.5		5.5	2.5		5.5	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $8 V \leq V_{OUT} \leq 24 V$			100			100	μA
Strobe Current	$V_{strobe} = 0.4$ V		1.7	3.3		1.7	3.3	mA
Strobe ON Voltage		0.9	1.4		0.9	1.4		V
Strobe OFF Voltage	$I_{sink} \leq 16$ mA		1.4	2.5		1.4	2.5	V
Positive Supply Current	$V_{IN} = -5$ mV		5.5	10		5.5	10	mA
Negative Supply Current			1.5	3.6		1.5	3.6	mA

Note 1: Derate metal can package at 6.8 mW/°C for operation at ambient temperatures above 60°C; derate flat package at 5.4 mW/°C for operation at ambient temperatures above 40°C.

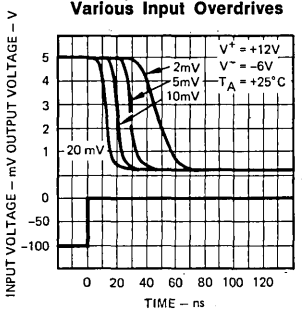
Note 2: These specifications apply for $-3 V \geq V^- \geq -12 V$, $V^+ = 12$ V and $T_A = 25°C$ unless otherwise specified.

Note 3: The offset voltages, offset currents, and bias currents given are the maximum values required to drive the output from the minimum output level up to the maximum output level. Thus, these parameters actually define an error band and take into account the worst-case effects of voltage gain and input impedance.

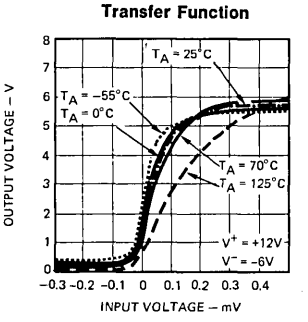
Note 4: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

PERFORMANCE CURVES

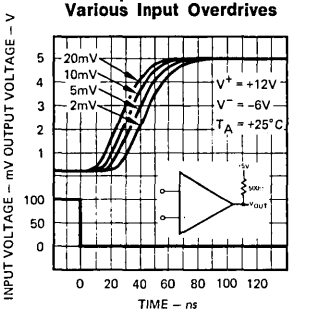
Response Time For Various Input Overdrives



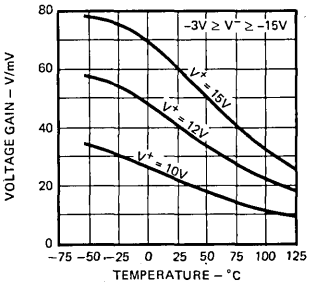
Transfer Function



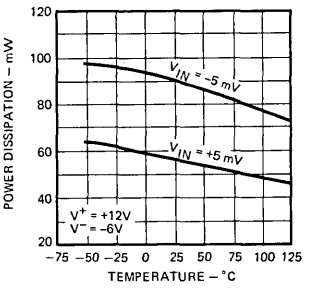
Response Time For Various Input Overdrives



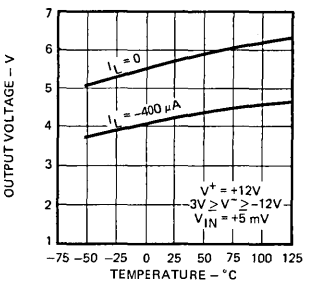
Voltage Gain



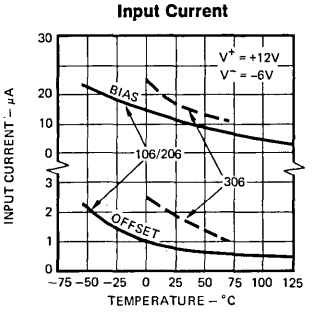
Power Consumption



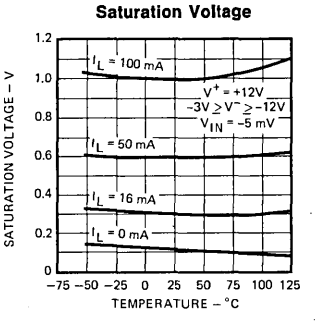
Positive Output Level



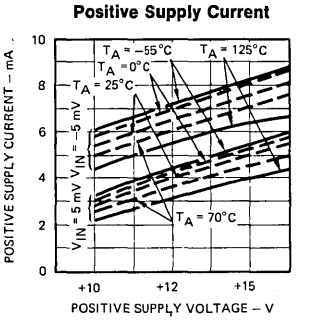
Input Current



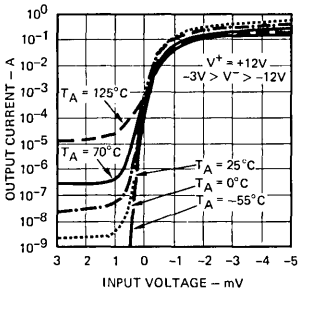
Saturation Voltage



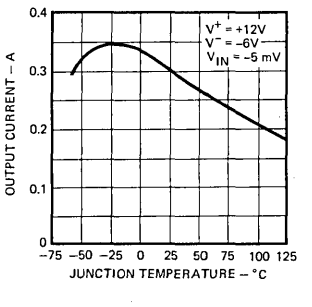
Positive Supply Current



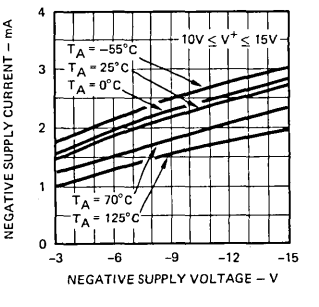
Transconductance



Short Circuit Output Current

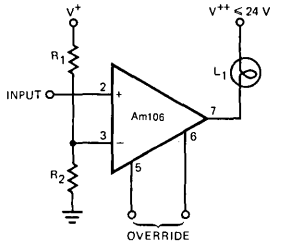


Negative Supply Current

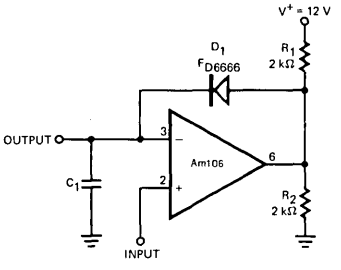


ADDITIONAL APPLICATIONS

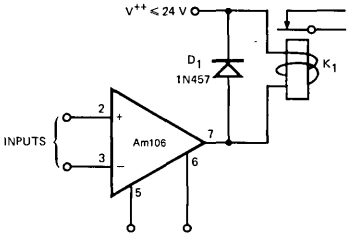
Level Detector and Lamp Driver



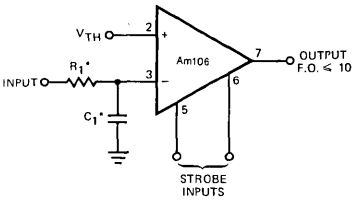
Fast Response Peak Detector



Relay Driver



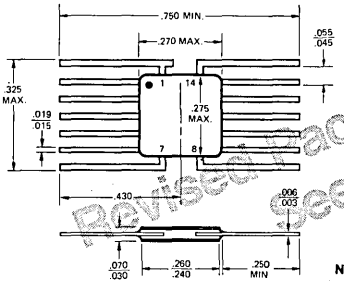
Adjustable Threshold Line Receiver



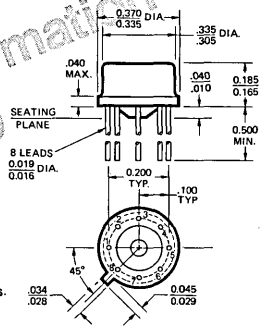
*Optional for response time control

PHYSICAL DIMENSIONS

Flat Package



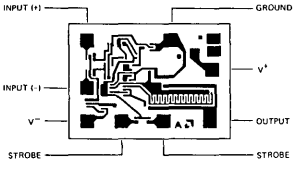
Metal Can



Note: All dimensions are in inches.
Leads are gold plated Kovar.

Metallization and Pad Layout

33 x 46 Mils



ADVANCED
MICRO
DEVICES INC.
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California 94086
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TELEX: 34-6306

Am107/207/307
Frequency Compensated Operational Amplifier

Description: The Am107/207/307 Operational Amplifiers are functionally, electrically, and pin-for-pin equivalent to the National LM107/207/307. They are available in the hermetic metal can, flat package, and dual-in-line packages.

Distinctive Characteristics: 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL STD 883.

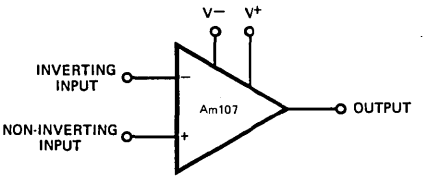
Mixing privileges for obtaining price discounts. Refer to price list.

Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

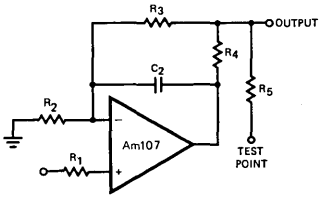
The Am107/207/307 monolithic operational amplifiers are internally frequency compensated and input/output overload protected. These differential input, class AB output amplifiers are intended to provide high accuracy and lower noise in high impedance applications. The Am107/207/307 provide improved electrical parameters and are pin-for-pin replacements for the 709, 101, 101A and 741 in most applications.

FUNCTIONAL DIAGRAM



APPLICATIONS

Input/Output Protection



If an input is driven from a low-impedance source, a series resistor, R_1 should be used to limit the peak instantaneous output current of the source to less than 100 mA. A large capacitor ($>0.1\mu F$) is equivalent to a low source impedance and should be protected against by an isolation resistor .

The amplifier output is protected against damage from shorts to ground or to the power supplies by device design. Protection of the output from voltages exceeding the specified operating power supplies can be obtained by isolating the output via limiting resistors R_4 or R_5.

The power supplies must never become reversed, even under transient conditions. Reverse voltages as low as 1 volt can cause damage through excessive current. This hazard can be reduced by using clamp diodes of high-peak current rating connected to the device supply lines.

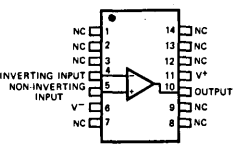
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am307	DIP	0°C to +70°C	LM307D
	Metal Can	0°C to +70°C	LM307
Am207	DIP	−25°C - +85°C	LM207D
	Metal Can	−25°C - +85°C	LM207
	Flat Pak	−25°C - +85°C	LM207F
Am107	DIP	−55°C - +125°C	LM107D
	Metal Can	−55°C - +125°C	LM107
	Flat Pak	−55°C - +125°C	LM107F
Am107	Dice	Note 4	LMD07

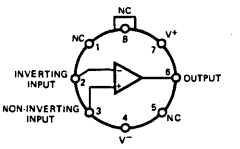
Note 4: The dice supplied will contain units which meet 0°C to +70°C, −25°C to +85°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAMS
Top View

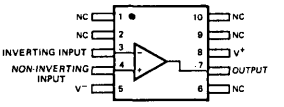
Dual-In-Line



Metal Can



Flat Package



NOTES:

(1) On Metal Can, pin 4 is connected to case.

(2) On DIP, pin 6 is connected to bottom of package.

(3) On Flat Package, pin 5 is connected to bottom of package.

MAXIMUM RATINGS

Supply Voltage Am107, Am207, Am307	 ±22V ±18V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range Am107 Am207 Am307	 −55°C to +125°C −25°C to +85°C 0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 3)

Parameter (see definitions)	Conditions	Am307 Min	Am307 Typ	Am307 Max	Am107 Am207 Min	Am107 Am207 Typ	Am107 Am207 Max	Units
Input Offset Voltage	$R_S \leq 50$ kΩ		2.0	7.5		0.7	2.0	mV
Input Offset Current			3	50		1.5	10	nA
Input Bias Current			70	250		30	75	nA
Input Resistance		0.5	2		1.5	4		MΩ
Supply Current	V_S = ±20V V_S = ±15V		 1.8	 3.0		1.8	3.0	mA mA
Large Signal Voltage Gain	V_S = ±15 V, V_{OUT} = ±10 V, $R_L \geq 2$ kΩ	25	160		50	160		V/mV
Slew Rate	$R_L \geq 2$ kΩ	0.2	0.5		0.2	0.5		V/μs
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 50$ kΩ			10			3.0	mV
Input Offset Current				70			20	nA
Average Temperature Coefficient of Input Offset Voltage	$T_{A(min)} \leq T_A \leq T_{A(max)}$		6.0	30		3.0	15	μV/°C
Average Temperature Coefficient of Input Offset Current	25°C ≤ $T_A \leq T_{A(max)}$ $T_{A(min)} \leq T_A \leq$ 25°C		0.01 0.02	0.3 0.6		0.01 0.02	0.1 0.2	nA/°C nA/°C
Input Bias Current				300			100	nA
Large Signal Voltage Gain	V_S = ±15 V, V_{OUT} = ±10 V, $R_L >$ 2 kΩ	25			25			V/mV
Input Voltage Range	V_S = ±20 V V_S = ±15 V	 +15, −12			±15			V V
Common Mode Rejection Ratio	$R_S \leq 50$ kΩ	70	90		80	96		dB
Supply Voltage Rejection Ratio	$R_S \leq 50$ kΩ	70	96		80	96		dB
Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ, R_L = 2 kΩ,	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
Supply Current	T_A = +125°C V_S = ±20 V					1.2	2.5	mA

DEFINITION OF TERMS

AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET CURRENT The ratio of the change in Input Offset Current over the operating temperature range to the temperature range.

AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET VOLTAGE The ratio of the change in Input Offset Voltage over the operating temperature range to the temperature range.

COMMON MODE REJECTION RATIO The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

INPUT BIAS CURRENT The average of the two input currents.

INPUT OFFSET CURRENT The difference in the currents into the two input terminals when the output is at zero.

INPUT OFFSET VOLTAGE That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

INPUT RESISTANCE The ratio of the change in input voltage to the change in input current on either input with the other grounded.

INPUT VOLTAGE RANGE The range of voltages on the input terminals for which the offset specifications apply.

LARGE-SIGNAL VOLTAGE GAIN The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT RESISTANCE The resistance seen looking into the output terminal with the output at null.

OUTPUT SHORT-CIRCUIT CURRENT The maximum output current available from the amplifier with the output shorted to ground or to either supply.

OUTPUT VOLTAGE SWING The peak output voltage swing, referred to zero, that can be obtained without clipping.

POWER SUPPLY REJECTION RATIO The ratio of the change in input offset voltage to the change in power supply voltages producing it.

SUPPLY CURRENT The current required from the power supply to operate the amplifier with no load and the output at zero.

SLEW RATE The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

Note 1: Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C, the Dual In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C, and the Flat Package at 5.4 mW/°C for operation at ambient temperatures above 57°C.

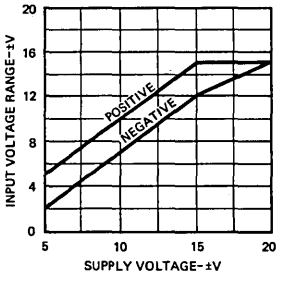
Note 2: For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.

Note 3: Unless otherwise specified, these specifications apply for supply voltages from ±5V to ±20V for the Am107 and Am207 and from ±5V to ±15V for the Am307.

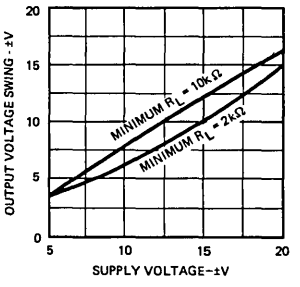
GUARANTEED PERFORMANCE CURVES (Note 3)

(Curves apply over the Operating Temperature Ranges)

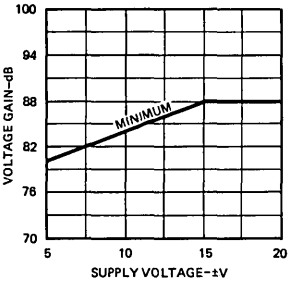
Input Voltage Range



Output Swing

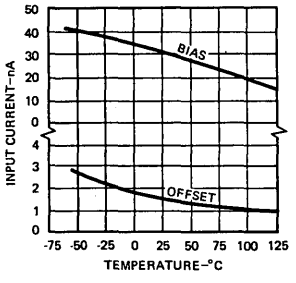


Voltage Gain

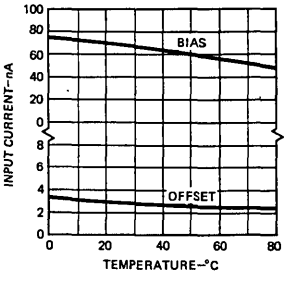


PERFORMANCE CURVES (Note 3)

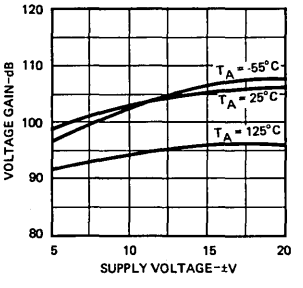
Input Current—Am107, Am207



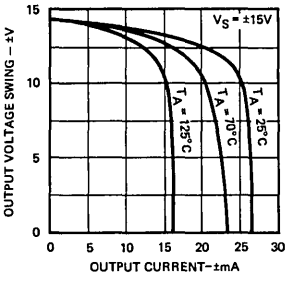
Input Current—Am307



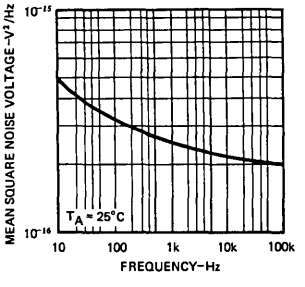
Voltage Gain



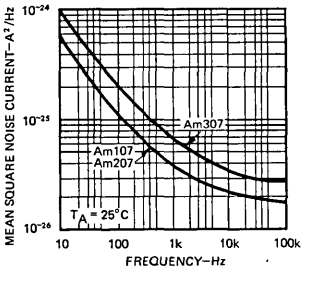
Current Limiting



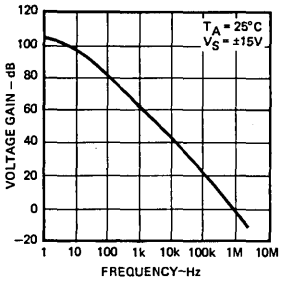
Input Noise Voltage



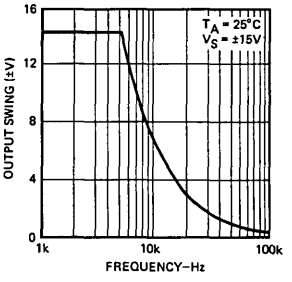
Input Noise Current



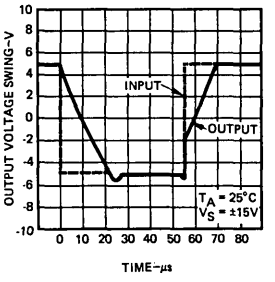
Open Loop Frequency Response



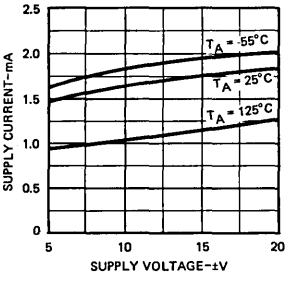
Large Signal Frequency Response



Voltage Follower Pulse Response

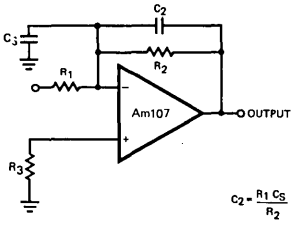


Supply Current

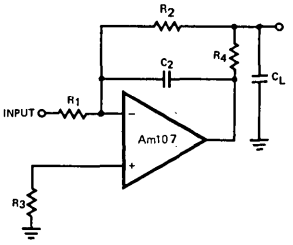


ADDITIONAL APPLICATION INFORMATION

Stray Input Capacitance/Large Feedback Resistance



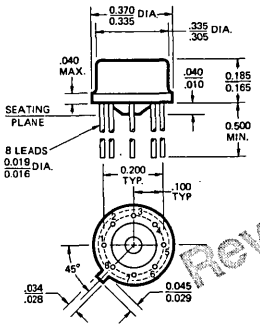
Large Capacitive Loads



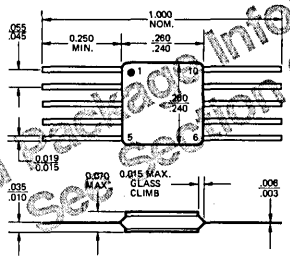
Stability is guaranteed for source resistances less than 10 kΩ, stray capacitances on the summing junction less than 5 pF, and capacitive loads smaller than 100 pF. If any of these conditions is not met, lead capacitors may be used in the feedback network to negate the effect of stray capacitance and large feedback resistors, or an RC network can be added to isolate capacitive loads. Power supplies should be bypassed to ground at one point, minimum, on each card. More bypass points should be considered for five or more amplifiers on a single card.

PHYSICAL DIMENSIONS

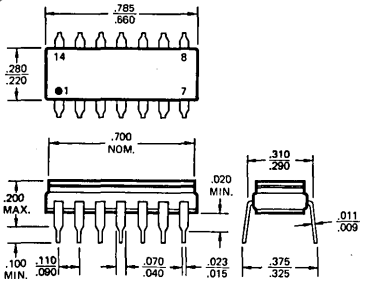
Metal Can



Flat Package



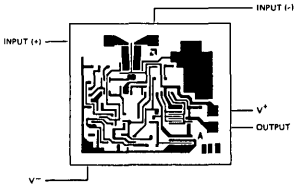
Dual-In-Line



Note: All dimensions are in inches.
Leads are gold plated Kovar.

Metallization and Pad Layout

49 x 56 Mils



ADVANCED MICRO DEVICES INC.
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TELEX: 34-6306

Am108/208/308
Am108A/208A/308A
Operational Amplifier

Description: The 108, 208, 308, 108A, 208A and 308A monolithic operational amplifiers are functionally, electrically and pin-for-pin equivalents to the National LM108, LM208, LM308, LM108A, LM208A and LM308A. They are available in the hermetic TO-99 metal can, dual-in-line, and flat packages.

Distinctive Characteristics: 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL STD 883

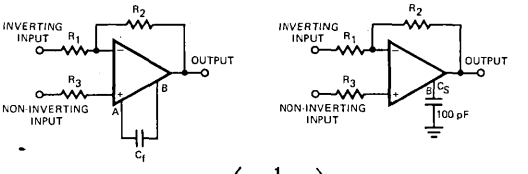
Mixing privileges for obtaining price discounts. Refer to price list.

Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

These differential input, precision amplifiers provide low input current and offset voltage competitive with FET and chopper stabilized amplifiers. They feature low power consumption over a supply voltage range of ±2V to ±20V. The amplifiers may be frequency compensated with a single external capacitor and are pin-for-pin interchangeable with the 101A/201A/301A. The 108A, 208A, and 308A are high performance selections from the 108/208/308 amplifier family.

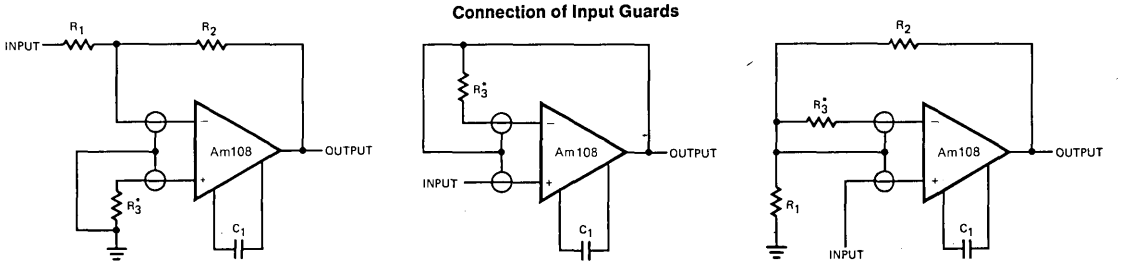
FUNCTIONAL DIAGRAM
Frequency Compensation Circuits



$$C_f \geq C_o\left(\frac{1}{1+\frac{R_2}{R_1}}\right)$$

C_o = 30 pF

APPLICATIONS
Connection of Input Guards



*Use to compensate for large source resistances.

NOTE: $\frac{R_1 R_2}{R_1 + R_2}$ Must be LOW impedance

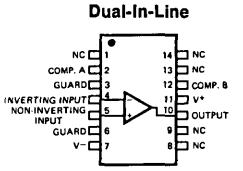
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am308	DIP	0°C - 70°C	LM308D
	Metal Can	0°C - 70°C	LM308
Am308A	DIP	0°C - 70°C	LM308AD
	Metal Can	0°C - 70°C	LM308A
Am208	DIP	−25°C - 85°C	LM208D
	Metal Can	−25°C - 85°C	LM208
	Flat Pak	−25°C - 85°C	LM208F
Am208A	DIP	−25°C - 85°C	LM208AD
	Metal Can	−25°C - 85°C	LM208A
	Flat Pak	−25°C - 85°C	LM208F
Am108	DIP	−55°C - 125°C	LM108D
	Metal Can	−55°C - 125°C	LM108
	Flat Pak	−55°C - 125°C	LM108F
Am108A	DIP	−55°C - 125°C	LM108AD
	Metal Can	−55°C - 125°C	LM108A
	Flat Pak	−55°C - 125°C	LM108F
Am108	Dice	Note 5	LMD08

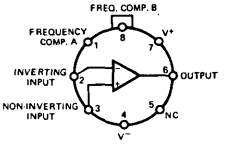
Note 5: The dice supplied will contain units which meet 0°C to +70°C, −25°C to +85°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAMS
Top Views

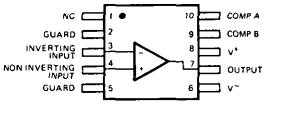
Dual-In-Line



Metal Can



Flat Package



NOTES:

(1) On Metal Can, pin 4 is connected to case.

(2) On DIP, pin 7 is connected to bottom of package.

(3) On Flat Package, pin 6 is connected to bottom of package.

MAXIMUM RATINGS

Supply Voltage Am108, 208, 108A, 208A, Am308, 308A	 ±20 V ±18 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15 V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range Am108, 108A Am208, 208A Am308, 308A	 −55°C to +125°C −25°C to +85°C 0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 4)

Parameter (see definitions)	Conditions	Am308 Min.	Am308 Typ.	Am308 Max.	Am308A Min.	Am308A Typ.	Am308A Max.	Am108 Am208 Min.	Am108 Am208 Typ.	Am108 Am208 Max.	Am108A Am208A Min.	Am108A Am208A Typ.	Am108A Am208A Max.	Units
Input Offset Voltage			2.0	7.5		0.3	0.5		0.7	2.0		0.3	0.5	mV
Input Offset Current			0.2	1.0		0.2	1.0		0.05	0.2		0.05	0.2	nA
Input Bias Current			1.5	7		1.5	7		0.8	2.0		0.8	2.0	nA
Input Resistance		10	40		10	40		30	70		30	70		MΩ
Supply Current	V_S = ±20 V V_S = ±15 V		0.3			0.3	0.8		0.3	0.6		0.3	0.6	mA
Large Signal Voltage Gain	V_S = ±15 V, V_{OUT} = ±10 V, $R_L \geq 10$ kΩ	25	300		80	300		50	300		80	300		V/mV
The Following Specifications Apply Over The Operating Temperature Ranges														
Input Offset Voltage				10			0.73			3.0			1.0	mV
Input Offset Current				1.5			1.5			0.4			0.4	nA
Average Temperature Coefficient of Input Offset Voltage			6.0	30		1.0	5.0		3.0	15		1.0	5.0	μV/°C
Average Temperature Coefficient of Input Offset Current			2	10		2.0	10		0.5	2.5		0.5	2.5	pA/°C
Input Bias Current				10			10			3.0			3.0	nA
Large Signal Voltage Gain	V_S = ±15 V, V_{OUT} = ±10 V, $R_L \geq 10$ kΩ	15			60			25			40			V/mV
Input Voltage Range	V_S = ±15 V	±13.5			±13.5			±13.5			±13.5			V
Common Mode Rejection Ratio		80	100		96	110		85	100		96	110		dB
Supply Voltage Rejection Ratio		80	96		96	110		80	96		96	110		dB
Output Voltage Swing	V_S = ±15 V, R_L = 10 kΩ,	±13	±14		±13	±14		±13	±14		±13	±14		V
Supply Current	T_A = +125°C V_S = ±20 V								0.15	0.4		0.15	0.4	mA

DEFINITION OF TERMS

AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET CURRENT The ratio of the change in Input Offset Current over the operating temperature range to the temperature range.

AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET VOLTAGE The ratio of the change in Input Offset Voltage over the operating temperature range to the temperature range.

COMMON MODE REJECTION RATIO The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

INPUT BIAS CURRENT The average of the two input currents.

INPUT OFFSET CURRENT The difference in the currents into the two input terminals when the output is at zero.

INPUT OFFSET VOLTAGE That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

INPUT RESISTANCE The ratio of the change in input voltage to the change in input current on either input with the other grounded.

INPUT VOLTAGE RANGE The range of voltages on the input terminals for which the offset specifications apply.

LARGE-SIGNAL VOLTAGE GAIN The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT RESISTANCE The resistance seen looking into the output terminal with the output at null.

OUTPUT SHORT-CIRCUIT CURRENT The maximum output current available from the amplifier with the output shorted to ground or to either supply.

OUTPUT VOLTAGE SWING The peak output voltage swing, referred to zero, that can be obtained without clipping.

POWER SUPPLY REJECTION RATIO The ratio of the change in input offset voltage to the change in power supply voltages producing it.

SUPPLY CURRENT The current required from the power supply to operate the amplifier with no load and the output at zero.

NOTES

Note 1: Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C and the Dual In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C, and the Flat Package at 5.4 mW/°C for operation at ambient temperatures above 57°C.

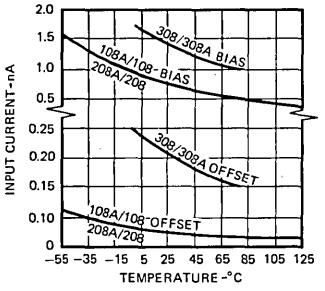
Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1 V is applied between the inputs unless some limiting resistance is used.

Note 3: For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.

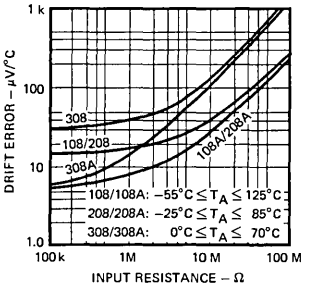
Note 4: Unless otherwise specified, these specifications apply for supply voltages from ±5 V to ±20 V for the Am108, Am208, Am108A and Am208A and from ±5 V to ±15 V for the Am308 and Am308A.

TYPICAL PERFORMANCE CURVES

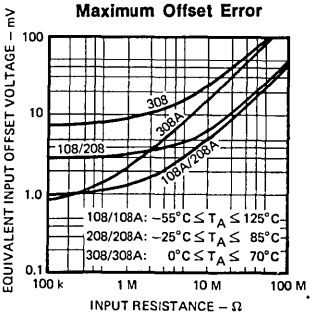
Input Currents



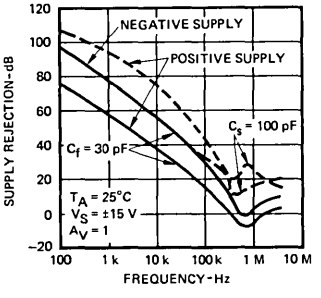
Maximum Drift Error



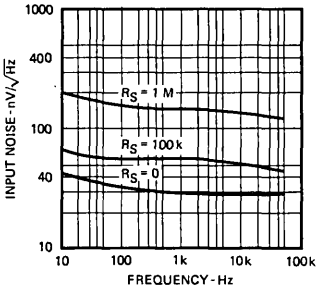
Maximum Offset Error



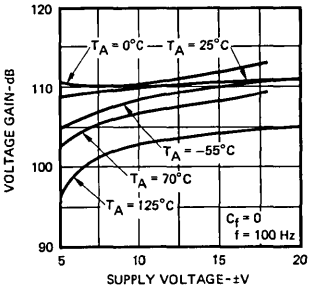
Power Supply Rejection



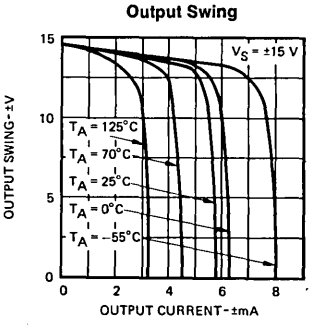
Input Noise Voltage



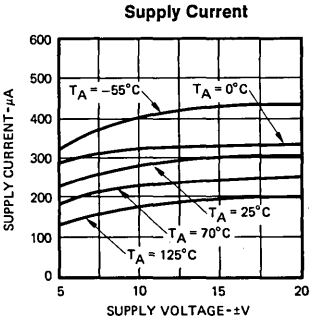
Voltage Gain



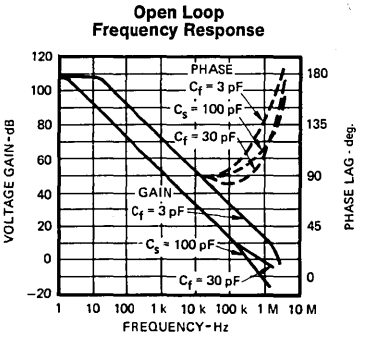
Output Swing



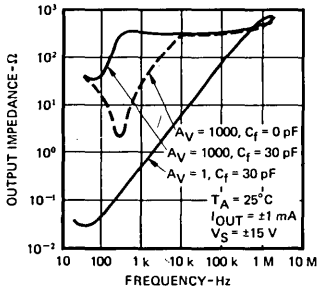
Supply Current



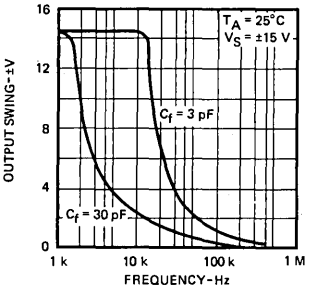
Open Loop Frequency Response



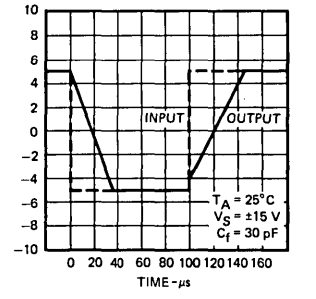
Closed Loop Output Impedance



Large Signal Frequency Response



Voltage Follower Pulse Response



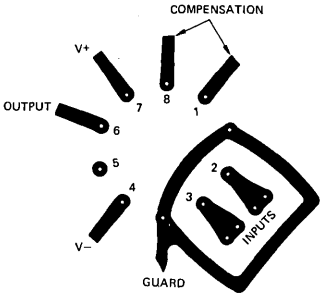
ADDITIONAL APPLICATION INFORMATION

GUARDING

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the 108 amplifier. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at 125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low-impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

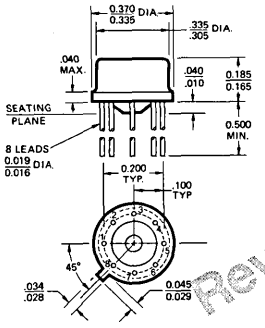
The pin configuration of the dual-in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration.)



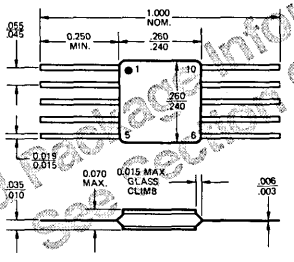
Board layout for Input Guarding with TO-99 package.

PHYSICAL DIMENSIONS

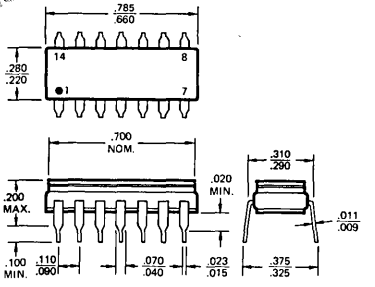
Metal Can



Flat Package



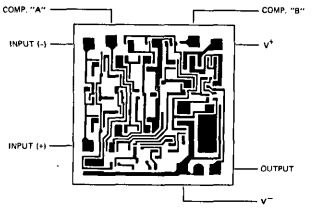
Dual-In-Line



Note: All dimensions are in inches.
Leads are gold plated Kovar.

Metallization and Pad Layout

56 x 56 Mils



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Am110/210/310
Voltage Follower

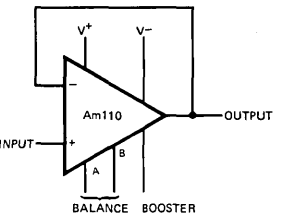
Distinctive Characteristics

- The Am110/210/310 are functionally, electrically, and pin-for-pin equivalent to the National LM 110/210/310
- Slew rate: 30V/μs
- Small signal bandwidth: 20 MHz
- Input current: 10 nA max. over temperature
- Supply voltage range: ±5V to ±18V
- 100% reliability assurance testing in compliance with MIL STD 883.
- Electrically tested and optically inspected dice for hybrid manufacturers.
- Mixing privilege for obtaining price discounts. Refer to price list.
- Available in metal can, hermetic dual-in-line or hermetic flat packages.

FUNCTIONAL DESCRIPTION

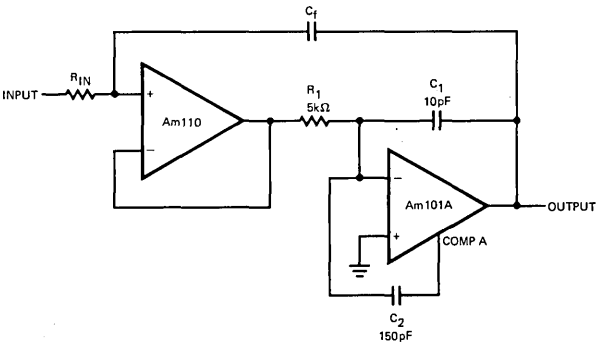
The Am110/210/310 are voltage followers featuring high-speed, low-input currents and large input voltage range. They are internally compensated with provision for external offset adjustment. Operation over wide supply voltages and temperature is possible.

FUNCTIONAL DIAGRAM



TYPICAL APPLICATION

Fast Integrator With Low-Input Current



ORDERING INFORMATION

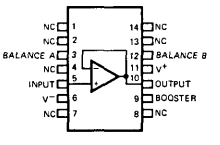
Part Number	Package Type	Temperature Range	Order Number
Am310	Metal Can	0°C - +70°C	LM310
	DIP	0°C - +70°C	LM310D
	Flat Pak	0°C - +70°C	LM310F
Am210	Metal Can	−25°C - +85°C	LM210
	DIP	−25°C - +85°C	LM210D
	Flat Pak	−25°C - +85°C	LM210F
Am110	Metal Can	−55°C - +125°C	LM110
	DIP	−55°C - +125°C	LM110D
	Flat Pak	−55°C - +125°C	LM110F
	Dice	Note	LMD10

Note: The dice supplied will contain units which meet 0° to 70°C, −25°C to +85°C and −55°C to +125°C temperature ranges.

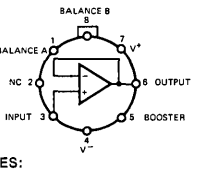
CONNECTION DIAGRAMS

Top Views

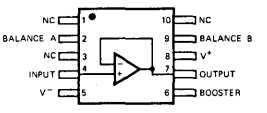
Dual-In-Line



Metal Can



Flat Package



NOTES:

(1) On Metal Can, pin 4 is connected to case.

(2) On DIP, pin 6 is connected to bottom of package.

(3) On Flat Package, pin 5 is connected to bottom of package.

MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	500 mW
Input Voltage (Note 2)	±15 V
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range Am110	−55°C to +125°C
Am210	−25°C to +85°C
Am310	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 60 sec)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 4)

Parameter (see definitions)	Conditions	Am310 Min	Am310 Typ	Am310 Max	Am110 Am210 Min	Am110 Am210 Typ	Am110 Am210 Max	Units
Input Offset Voltage			2.5	7.5		1.5	4.0	mV
Input Bias Current			2.0	7.0		1.0	3.0	nA
Input Resistance		10^4	10^6		10^4	10^6		MΩ
Input Capacitance			1.5			1.5		pF
Large-Signal Voltage Gain	R_L = 8 kΩ, V_{out} = ±10 V, V_S = ±15 V	0.999	0.9999		0.999	0.9999		V/V
Output Resistance			0.75	2.5		0.75	2.5	Ω
Supply Current			3.9	5.5		3.9	5.5	mA
Slew Rate	V_S = ±15 V, V_{IN} = ±10 V, R_L = 10 kΩ		30		20	30		V/μs
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage				10.0			6.0	mV
Input Bias Current				10.0			10.0	nA
Large-Signal Voltage Gain	R_L = 10 kΩ, V_{out} = ±10 V, V_S = ±15 V	0.999			0.999			V/V
Output Voltage Swing (Note 5)	R_L = 10 kΩ, V_S = ±15 V	±10			±10			V
Supply Current	T_A = +125°C					2.0	4.0	mA
Supply Voltage Rejection Ratio	±5 V ≤ V_S ≤ ±18 V	70			70			dB
Average Temperature Coefficient of Input Offset Voltage	0° ≤ T_A ≤ 70°C		10					μV/°C
	−55°C ≤ T_A ≤ 85°C +85°C ≤ T_A ≤ 125°C					6 12		μV/°C

DEFINITION OF TERMS

INPUT BIAS CURRENT The current flowing into the input of the amplifier with the input at zero.

INPUT OFFSET VOLTAGE The voltage measured at the output of the amplifier with the input at zero.

INPUT RESISTANCE The ratio of the rated output voltage swing to the change in the input current required to drive the output from zero to this voltage.

LARGE-SIGNAL VOLTAGE GAIN The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

SUPPLY CURRENT The DC current from the supplies required to operate the amplifier with the output at zero and with no load current.

OUTPUT RESISTANCE The ratio of the output voltage change to the change in the output current with constant input voltage.

SLEW RATE The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

SUPPLY VOLTAGE REJECTION RATIO The ratio of the change in input offset voltage to the change in supply voltage producing it.

OUTPUT VOLTAGE SWING The peak output swing, referred to zero, that can be obtained without clipping.

AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET VOLTAGE The ratio of the change in Input Offset Voltage over the operating temperature range to the temperature range.

NOTES

Note 1: Derate Metal Can package 6.8 mW/°C for operation at ambient temperatures above 75°C, the Dual In-Line at 9 mW/°C for operation at ambient temperatures above 95°C, and the Flat Packages at 5.4 mW/°C for operation at ambient temperatures above 57°C.

Note 2: For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.

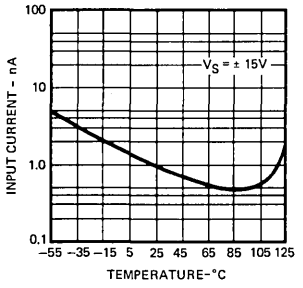
Note 3: To prevent damage when the output is shorted, it is necessary to insert a resistor larger than 2 kΩ in series with the input. Continuous short circuit is allowed for case temperatures to 125°C and ambient temperatures to 70°C for the 110/210. For 310, the corresponding temperatures are 70°C and 55°C respectively.

Note 4: Unless otherwise specified, these specifications apply for supply voltages from ±5 to ±18 V.

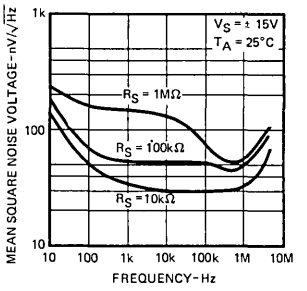
Note 5: Greater output voltage swing can be obtained by connecting a resistor from booster terminal to V−.

PERFORMANCE CURVES

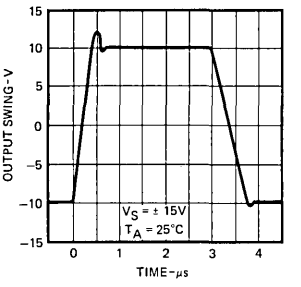
Input Current



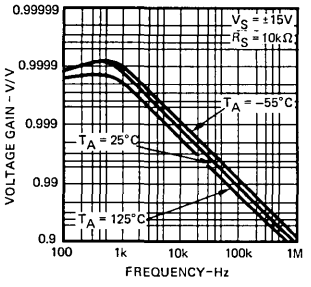
Output Noise Voltage



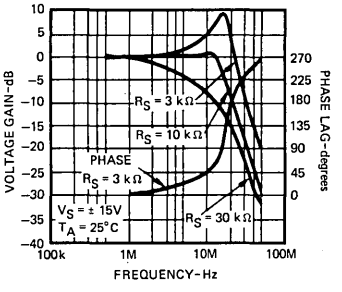
Large Signal Pulse Response



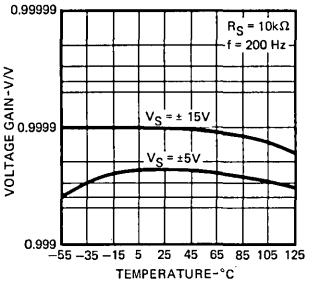
Voltage Gain



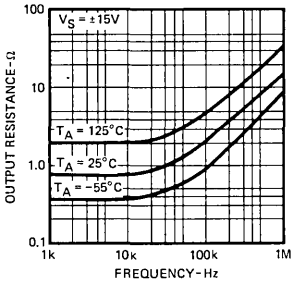
Voltage Gain



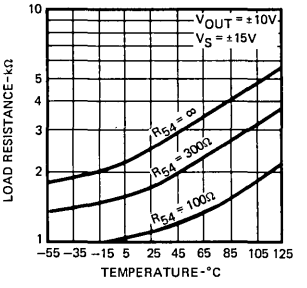
Voltage Gain



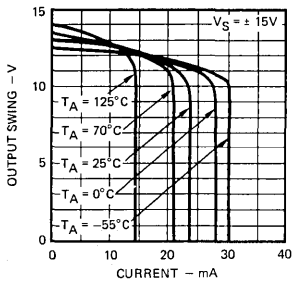
Output Resistance



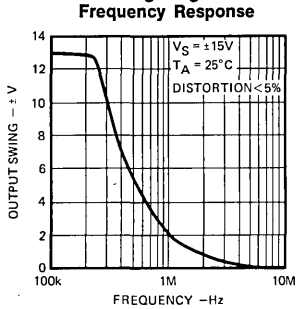
Symmetrical Output Swing



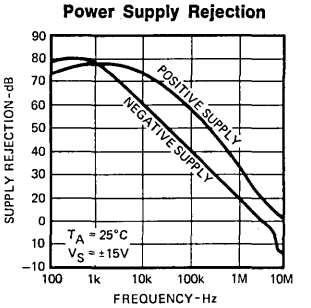
Positive Output Swing



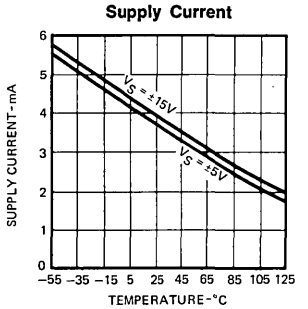
Large Signal Frequency Response



Power Supply Rejection

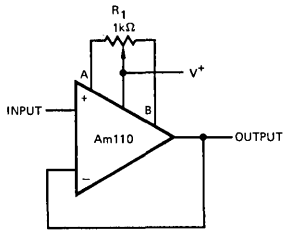


Supply Current

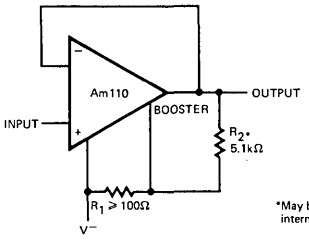


APPLICATIONS

Offset Nulling Circuit

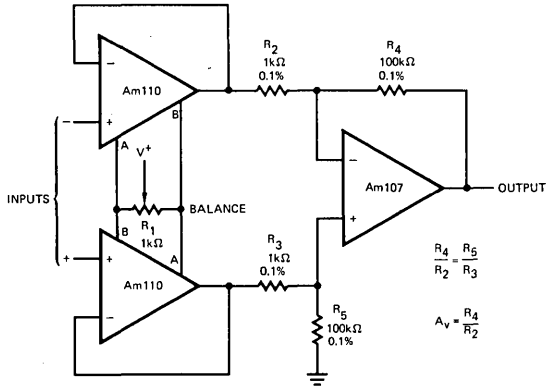


Increasing Negative Swing Under Load

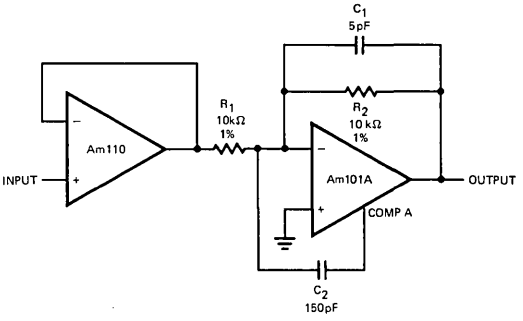


*May be added to reduce internal dissapation.

Differential Input Instrumentation Amplifier

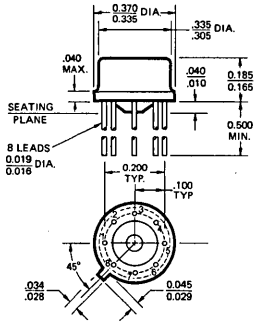


Fast Inverting Amplifier With High Input Impedance

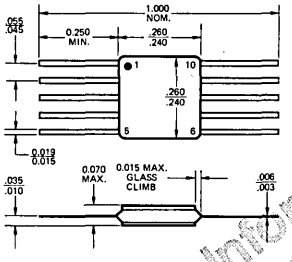


PHYSICAL DIMENSIONS

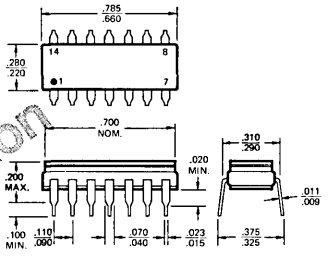
Metal Can



Flat Package



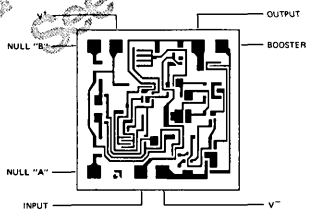
Dual-In-Line



Note: All dimensions are in inches.
Leads are gold plated Kovar.

Metallization and Pad Layout

40 x 40 Mils



ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am112/212/312
Compensated, High-Performance Operational Amplifier

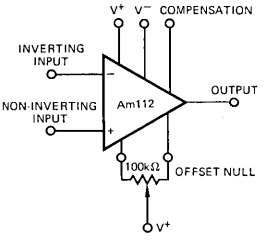
Distinctive Characteristics

- The Am112/212/312 are functionally, electrically, and pin-for-pin equivalents to the National LM112/212/312.
- Low input bias currents: 800pA
- Low input offset currents: 50pA
- Low power consumption: 3mW
- Internal frequency compensation.
- Offset nulling provisions.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically tested and optically inspected die for assemblers of hybrid products.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Available in metal can, hermetic dual-in-line or hermetic flat packages.

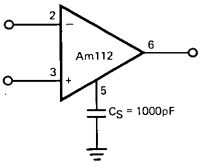
FUNCTIONAL DESCRIPTION

The Am112/212/312 are compensated high-performance operational amplifiers featuring very low offset voltage and input current errors competitive with FET and chopper-stabilized amplifiers. The devices will operate over a supply voltage range of ±2V to ±20V, drawing a typical quiescent current of only 300μA. The Am112/212/312 are internally frequency compensated and provision is made for offset adjustment with a single potentiometer. Overcompensation providing a greater stability margin is possible and the internal protection of the MOS capacitor makes it immune from overvoltage transients.

FUNCTIONAL DIAGRAM

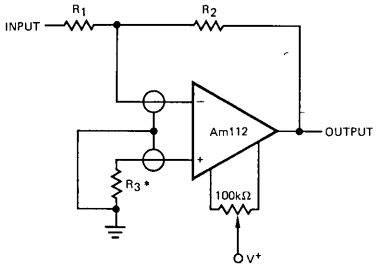


Overcompensation for Greater Stability Margin

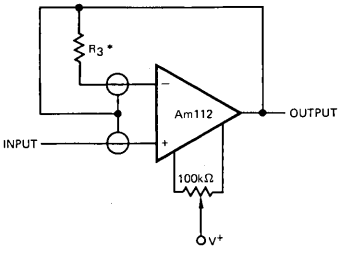


TYPICAL APPLICATIONS

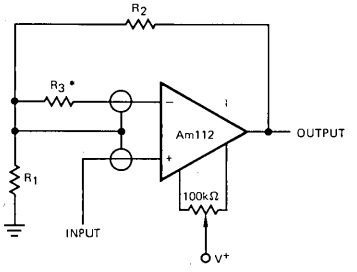
Connection of input guards and offset null



INVERTING AMPLIFIER



FOLLOWER



NON-INVERTING AMPLIFIER

*Use to compensate for large source resistances.

NOTE: $\frac{R_1R_2}{R_1+R_2}$ Must be LOW impedance

ORDERING INFORMATION

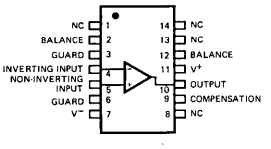
Part Number	Package Type	Temperature Range	Order Number
Am312	DIP	0°C - 70°C	LM312D
	Metal Can	0°C - 70°C	LM312
	Dice	Note 5	LMD 12
Am212	DIP	−25°C - 85°C	LM212D
	Metal Can	−25°C - 85°C	LM212
	Flat Pak	−25°C - 85°C	LM212F
Am112	DIP	−55°C - 125°C	LM112D
	Metal Can	−55°C - 125°C	LM112
	Flat Pak	−55°C - 125°C	LM112F
	Dice	Note 5	LD112

Note 5. The dice supplied have been electrically tested at 25°C to their respective device limits.

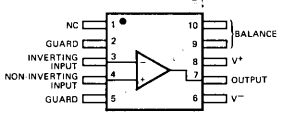
CONNECTION DIAGRAMS

Top Views

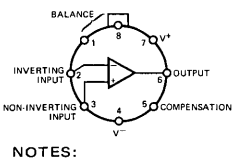
Dual-In-Line



Flat Package



Metal Can



NOTES:
(1) On metal can, pin 4 is connected to case.
(2) On DIP, pin 7 is connected to bottom of package.
(3) On flat package, pin 6 is connected to bottom of package. Compensation terminal is not brought out on the flat package.

MAXIMUM RATINGS

Supply Voltage	
Am112, 212	±20V
Am312	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Current (Note 2)	±10mA
Input Voltage (Note 3)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
Am112	–55°C to +125°C
Am212	–25°C to +85°C
Am312	0°C to +70°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 4)

Parameter (see definitions)	Conditions	Am312 Min.	Am312 Typ.	Am312 Max.	Am112 Am212 Min.	Am112 Am212 Typ.	Am112 Am212 Max.	Units
Input Offset Voltage			2.0	7.5		0.7	2.0	mV
Input Offset Current			0.2	1		0.05	0.2	nA
Input Bias Current			1.5	7		0.8	2.0	nA
Input Resistance		10	40		30	70		MΩ
Supply Current			0.3	0.8		0.3	0.6	mA
Large Signal Voltage Gain	V_{OUT} = ±10V, V_S = ±15V R_L > 10kΩ	25	300		50	300		V/mV
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage				10			3.0	mV
Average Temperature Coefficient of Input Offset Voltage			6.0	30		3.0	15	μV/°C
Input Offset Current				1.5			0.4	nA
Average Temperature Coefficient of Input Offset Current			2.0	10		0.5	2.5	pA/°C
Input Bias Current				10			3.0	nA
Supply Current	T_A = +125°C					0.15	0.4	mA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V R_L > 10kΩ	15			25			V/mV
Output Voltage Swing	V_S = ±15V, R_L = 10kΩ	±13	±14		±13	±14		V
Input Voltage Range	V_S = ±15V	±13.5			±13.5			V
Common Mode Rejection Ratio		80	100		85	100		dB
Supply Voltage Rejection Ratio		80	96		80	96		dB

DEFINITION OF TERMS

AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET CURRENT The ratio of the change in input offset current over the operating temperature range to the temperature range.

AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET VOLTAGE The ratio of the change in input offset voltage over the operating temperature range to the temperature range.

COMMON MODE REJECTION RATIO The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

INPUT BIAS CURRENT The average of the two input currents.

INPUT OFFSET CURRENT The difference in the currents into the two input terminals when the output is at zero.

INPUT OFFSET VOLTAGE That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

INPUT RESISTANCE The ratio of the change in input voltage to the change in input current on either input with the other grounded.

INPUT VOLTAGE RANGE The range of voltages on the input terminals for which the offset specifications apply.

OUTPUT RESISTANCE The resistance seen looking into the output terminal with the output at null.

OUTPUT SHORT-CIRCUIT CURRENT The maximum output current available from the amplifier with the output shorted to ground or to either supply.

OUTPUT VOLTAGE SWING The peak output voltage swing, referred to zero, that can be obtained without clipping.

POWER SUPPLY REJECTION RATIO The ratio of the change in input offset voltage to the change in power supply voltages producing it.

SUPPLY CURRENT The current required from the power supply to operate the amplifier with no load and the output at zero.

Note 1: Derate Metal Can package at 6.8mW/°C for operation at ambient temperatures above 75°C and the Dual-In-Line package at 9mW/°C for operation at ambient temperatures above 95°C, and the Flat Package at 5.4mW/°C for operation at ambient temperatures above 57°C.

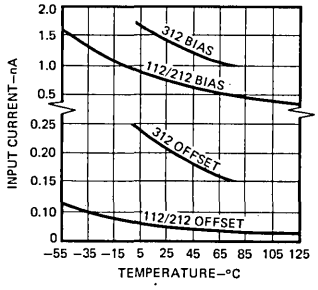
Note 2: The inputs are shunted with Shunt diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 3: For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.

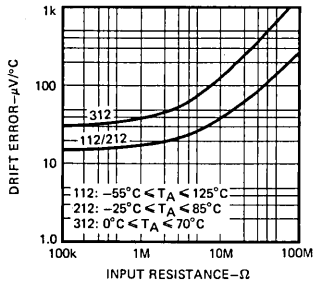
Note 4: Unless otherwise specified, these specifications apply for supply voltages from ±5V to ±20V for the Am112, Am212 and from ±5 to ±15V for the Am312.

TYPICAL PERFORMANCE CURVES

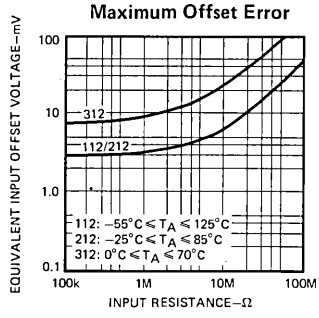
Input Currents



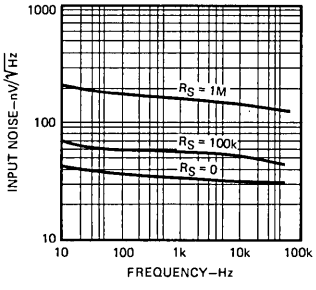
Maximum Drift Error



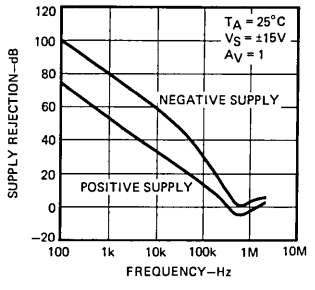
Maximum Offset Error



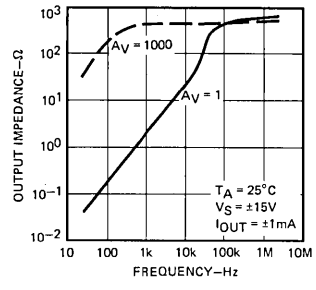
Input Noise Voltage



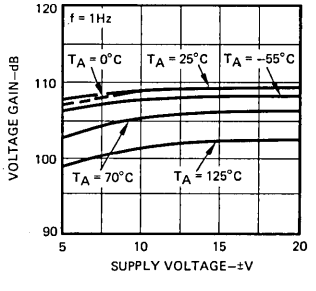
Power Supply Rejection



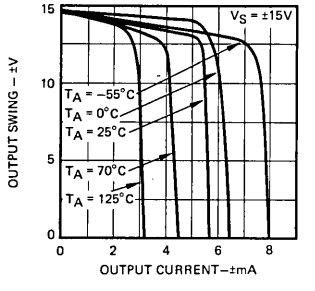
Closed Loop Output Impedance



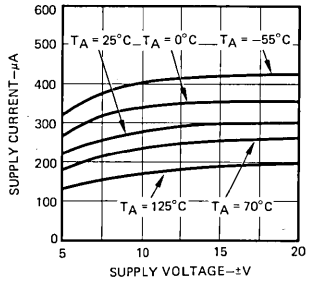
Voltage Gain



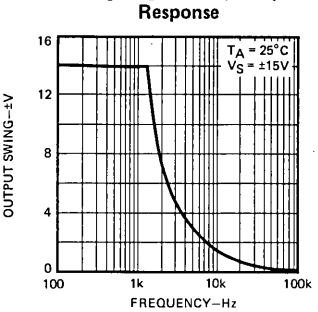
Output Swing



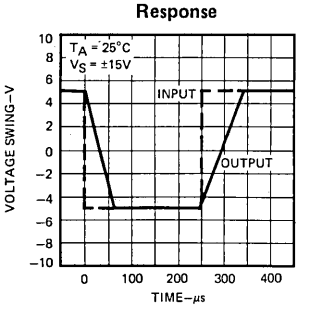
Supply Current



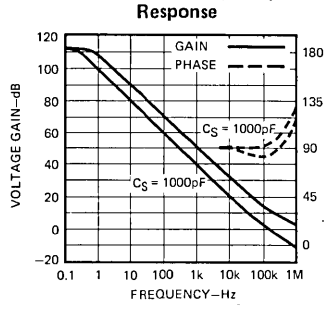
Large Signal Frequency Response



Voltage Follower Pulse Response



Open Loop Frequency Response



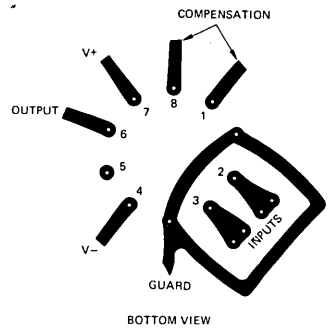
ADDITIONAL APPLICATION INFORMATION

GUARDING

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the 112 amplifier. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at 125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low-impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

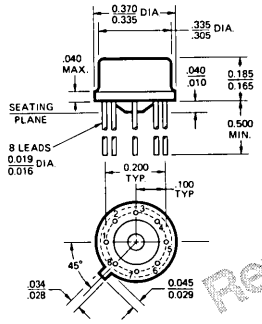
The pin configuration of the dual-in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard Am741 and Am101A pin configuration.)



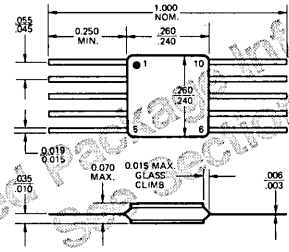
Note: Board layout for input Guarding with TO-99 package.

PHYSICAL DIMENSIONS

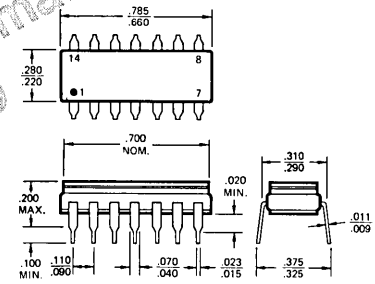
Metal Can



Flat Package



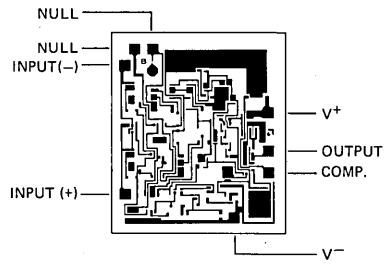
Dual-In-Line



Note: All dimensions are in inches.
Leads are gold plated Kovar.

Metallization and Pad Layout

62 x 72 Mils



ADVANCED MICRO DEVICES INC.
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Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am216/316•Am216A/316A

Compensated, High-Performance Operational Amplifier

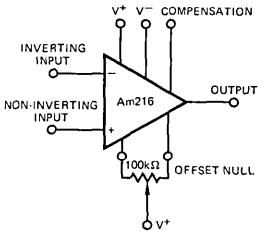
Distinctive Characteristics

- The Am216/Am216A/Am316/Am316A are functionally, electrically, and pin-for-pin equivalent to the National LM216/LM216A/LM316/LM316A.
- Low input bias currents: 50pA
- Low input offset currents: 15pA
- Low power consumption: 3mW
- Internal frequency compensation
- Offset nulling provisions
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically and optically inspected dice for assemblers of hybrid products.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Available in metal can, hermetic dual-in-line and flat packages.

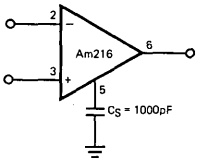
FUNCTIONAL DESCRIPTION

The Am216/Am216A/Am316/Am316A are compensated high performance operational amplifiers featuring extremely low input-current errors. High input impedance achieved using supergain transistors in a Darlington input stage produces input bias currents that are equal to high quality FET amplifiers. These devices are internally frequency compensated and provision is made for offset adjustment with a single potentiometer.

FUNCTIONAL DIAGRAM

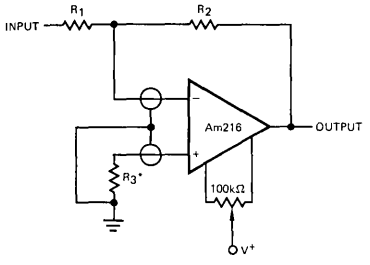


Overcompensation for Greater Stability Margin

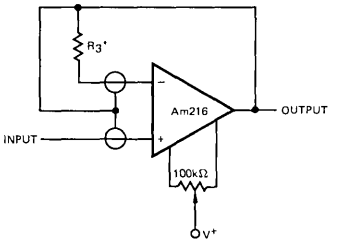


TYPICAL APPLICATIONS

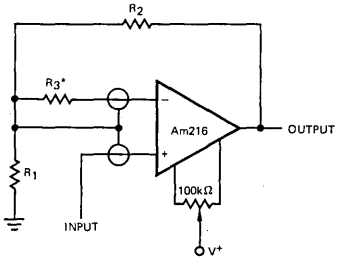
Connection of Input Guards and Offset Null



Inverting Amplifier



Follower



Non-Inverting Amplifier

*Use to compensate for large source resistances.

NOTE: $\frac{R_1 R_2}{R_1+R_2}$ Must be LOW impedance

ORDERING INFORMATION

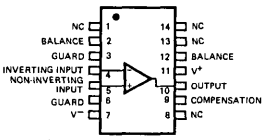
Part Number	Package Type	Temperature Range	Order Number
Am316	DIP	0°C - 70°C	LM316D
	Metal Can	0°C - 70°C	LM316
	Flat Pak	0°C - 70°C	LM316F
	Dice	Note 5	LMD16
Am316A	DIP	0°C - 70°C	LM316AD
	Metal Can	0°C - 70°C	LM316A
	Flat Pak	0°C - 70°C	LM316AF
	Dice	Note 5	LMD16A
Am216	DIP	−25°C - 85°C	LM216D
	Metal Can	−25°C - 85°C	LM216
	Flat Pak	−25°C - 85°C	LM216F
	Dice	Note 5	LD216
Am216A	DIP	−25°C - 85°C	LM216AD
	Metal Can	−25°C - 85°C	LM216A
	Flat Pak	−25°C - 85°C	LM216AF
	Dice	Note 5	LD216A

Note 5: The dice supplied have been electrically tested at 25°C to their respective device limits.

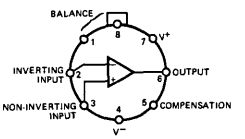
CONNECTION DIAGRAMS

Top Views

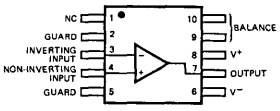
Dual-In-Line



Metal Can



Flat Package



Notes:
(1) On Metal Can, pin 4 is connected to case.
(2) On DIP, pin 7 is connected to bottom of package.
(3) On Flat Package, pin 6 is connected to bottom of package. Compensation terminal is not brought out on the flat package.

MAXIMUM RATINGS

Supply Voltage	±20 V
Power Dissipation (Note 1)	500 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15 V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
Am216/Am216A	−25°C to 85°C
Am316/Am316A	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 4)

Parameter (see definitions)	Conditions	Am216/Am216A		Am316/Am316A		Units
Input Offset Voltage		10	3	10	3	mV (MAX.)
Input Offset Current		50	15	50	15	pA (MAX.)
Input Bias Current		150	50	150	50	pA (MAX.)
Input Resistance		1	5	1	5	GΩ (MIN.)
Supply Current		0.8	0.6	0.8	0.6	mA (MAX.)
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V $R_L \geq 10k\Omega$	20	40	20	40	V/mV (MIN.)
The Following Specifications Apply Over The Operating Temperature Ranges						
Input Offset Voltage		15	6	15	6	mV (MAX.)
Input Offset Current		100	30	100	30	pA (MAX.)
Input Bias Current		250	100	250	100	pA (MAX.)
Supply Current	$T_A = T_{MAX.}$		0.5		0.5	mA (MAX.)
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V $R_L \geq 10k\Omega$	10	20	15	30	V/mV (MIN.)
Output Voltage Swing	V_S = ±15V, R_L = 10kΩ	±13	±13	±13	±13	V (MIN.)
Input Voltage Range	V_S = ±15V	±13	±13	±13	±13	V (MIN.)
Common Mode Rejection Ratio		80	80	80	80	dB (MIN.)
Supply Voltage Rejection Ratio		80	80	80	80	dB (MIN.)

DEFINITION OF TERMS

AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET CURRENT The ratio of the change in input offset current over the operating temperature range to the temperature range.

AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET VOLTAGE The ratio of the change in Input Offset Voltage over the operating temperature range to the temperature range.

COMMON MODE REJECTION RATIO The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

INPUT BIAS CURRENT The average of the two input currents.

INPUT OFFSET CURRENT The difference in the currents into the two input terminals when the output is at zero.

INPUT OFFSET VOLTAGE That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

INPUT RESISTANCE The ratio of the change in input voltage to the change in input current on either input with the other grounded.

INPUT VOLTAGE RANGE The range of voltages on the input terminals for which the offset specifications apply.

LARGE-SIGNAL VOLTAGE GAIN The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT RESISTANCE The resistance seen looking into the output terminal with the output at null.

OUTPUT SHORT-CIRCUIT CURRENT The maximum output current available from the amplifier with the output shorted to ground or to either supply.

OUTPUT VOLTAGE SWING The peak output voltage swing, referred to zero, that can be obtained without clipping.

POWER SUPPLY REJECTION RATIO The ratio of the change in input offset voltage to the change in power supply voltages producing it.

SUPPLY CURRENT The current required from the power supply to operate the amplifier with no load and the output at zero.

NOTES

Note 1: Derate Metal Can package at 6.8mW/°C for operation at ambient temperatures above 75°C and the Dual-in-Line package at 9mW/°C for operation at ambient temperatures above 95°C, and the Flat Package at 5.4mW/°C for operation at ambient temperatures above 57°C.

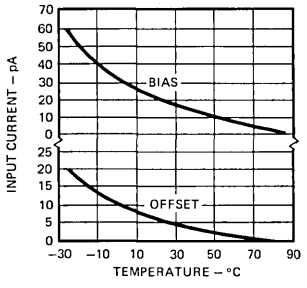
Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 3: For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.

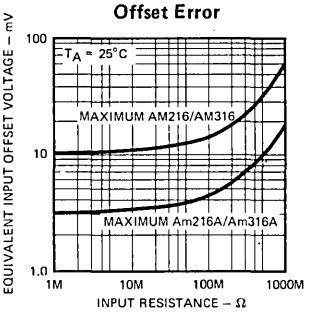
Note 4: Unless otherwise specified, these specifications apply for supply voltages from ±5V to ±20V.

TYPICAL PERFORMANCE CHARACTERISTICS

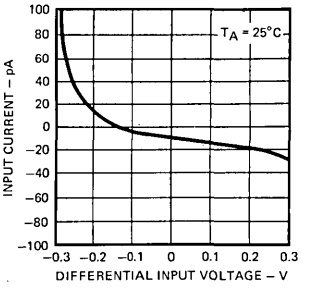
Input Currents



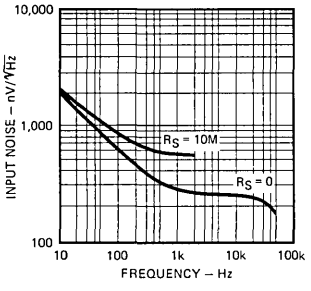
Offset Error



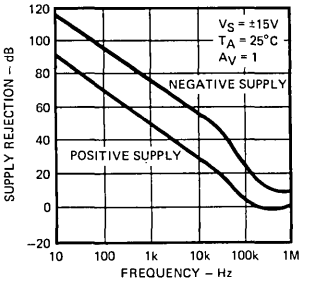
Input Current



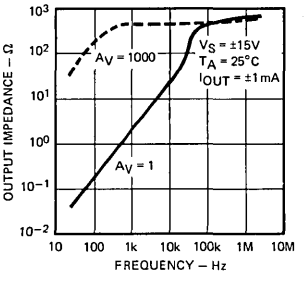
Input Noise Voltage



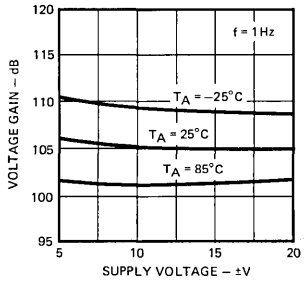
Power Supply Rejection



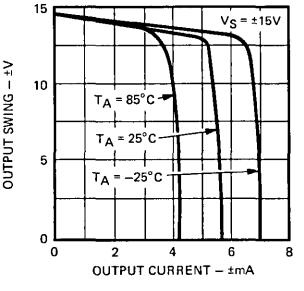
Closed Loop Output Impedance



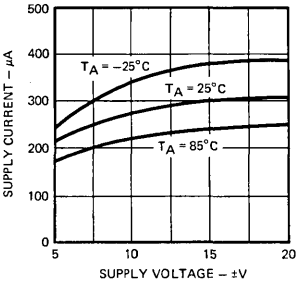
Voltage Gain



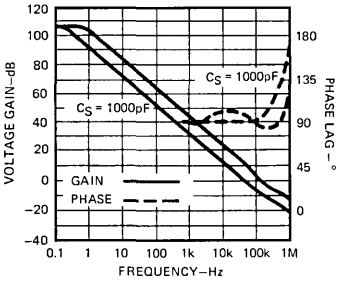
Output Swing



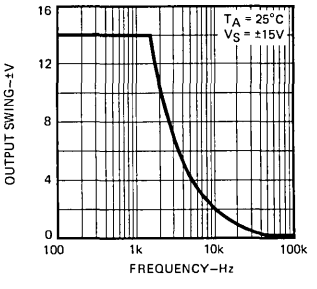
Supply Current



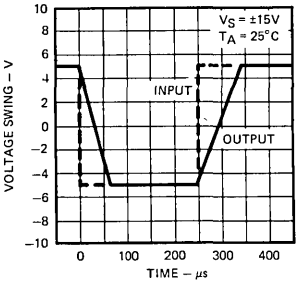
Open Loop Frequency Response



Large Signal Frequency Response



Voltage Follower Pulse Response



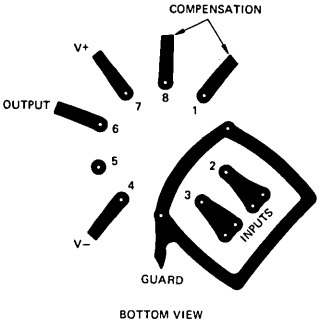
ADDITIONAL APPLICATION INFORMATION

GUARDING

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the Am216 amplifier. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

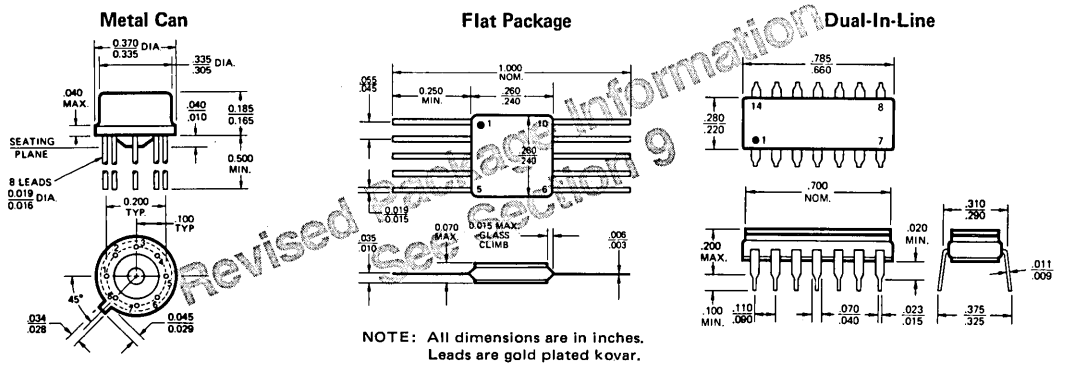
Even with properly cleaned and coated boards, leakage currents may cause trouble at 125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low-impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the dual-in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration.)



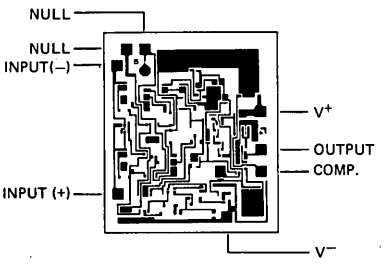
Note: Board layout for input Guarding with TO-99 package.

PHYSICAL DIMENSIONS



Metallization and Pad Layout

62 x 72 Mils



ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am118/218/318
High-Speed Operational Amplifier

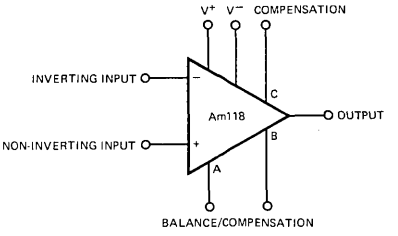
Distinctive Characteristics

- The Am118/218/318 are functionally, electrically, and pin-for-pin equivalent to the National LM118/218/318
- Slew rate: 70V/μs
- Small signal bandwidth: 15MHz
- Internal frequency compensation
- Supply voltage range: ±5V to ±20V
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically tested and optically inspected dice for hybrid manufacturers.
- Mixing privilege for obtaining price discounts. Refer to price list.
- Available in metal can, hermetic dual-in-line or hermetic flat packages.

FUNCTIONAL DESCRIPTION

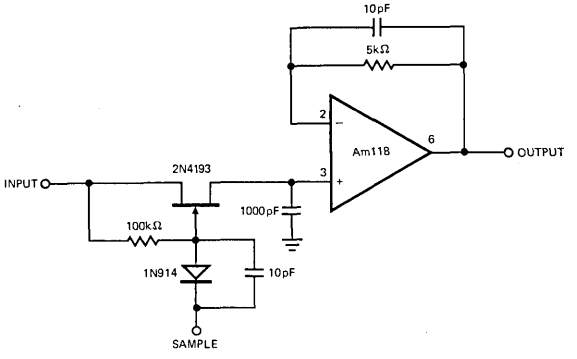
The Am118/218/318 are internally compensated high-speed operational amplifiers featuring minimum slew rate of 50V/μs, low input bias currents, large input voltage range and excellent performance over a wide range of supply voltages and temperature. They have provision for increased speeds when operating in the inverting mode.

FUNCTIONAL DIAGRAM



TYPICAL APPLICATION

Fast Sample and Hold



ORDERING INFORMATION

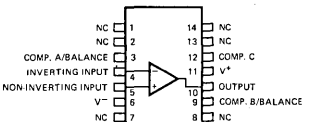
Part Number	Package Type	Temperature Range	Order Number
Am318	Metal Can	0°C - +70°C	LM318
	DIP	0°C - +70°C	LM318D
	Flat Pak	0°C - +70°C	LM318F
Am218	Metal Can	−25°C - +85°C	LM218
	DIP	−25°C - +85°C	LM218D
	Flat Pak	−25°C - +85°C	LM218F
Am118	Metal Can	−55°C - +125°C	LM118
	DIP	−55°C - +125°C	LM118D
	Flat Pak	−55°C - +125°C	LM118F
Am118	Dice	Note	LMD18

Note: The dice supplied will contain units which meet 0° to 70°C, −25°C to +85°C and −55°C to +125°C temperature ranges.

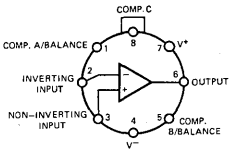
CONNECTION DIAGRAMS

Top Views

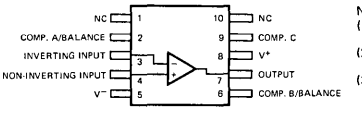
Dual-In-Line



Metal Can



Flat Package



Notes:
(1) On Metal Can, pin 4 is connected to case.
(2) On DIP, pin 6 is connected to bottom of package.
(3) On Flat Package, pin 5 is connected to bottom of package.

MAXIMUM RATINGS

Supply Voltage	±20V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage (Note 2)	±5V
Input Voltage (Note 3)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
Am118	–55°C to +125°C
Am218	–25°C to +85°C
Am318	0°C to +70°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 4)

Parameter (see definitions)	Conditions	Am318 Min.	Am318 Typ.	Am318 Max.	Am118 Am218 Min.	Am118 Am218 Typ.	Am118 Am218 Max.	Units
Input Offset Voltage	$R_S \leq 5k\Omega$		4	10		2	4	mV
Input Offset Current			30	200		6	50	nA
Input Bias Current			150	500		120	250	nA
Input Resistance		0.5	3		1.0	3		MΩ
Supply Current	V_S = ±20V		5	10		5	8	mA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V $R_L \geq 2k\Omega$	25	200		50	200		V/mV
Slew Rate	A_V = +1, V_S = ±15V (Fig.1) R_L = 2kΩ, C_L = 30pF	50	70		50	70		V/μs
Small Signal Bandwidth	V_S = ±15V		15			15		MHz
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 5k\Omega$			15			6	mV
Input Offset Current				300			100	nA
Input Bias Current				750			500	nA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V $R_L \geq 2k\Omega$	20			25			V/mV
Input Voltage Range	V_S = ±15V	±11.5			±11.5			V
Common Mode Rejection Ratio	$R_S \leq 5k\Omega$	70			80			dB
Supply Voltage Rejection Ratio	$R_S \leq 5k\Omega$	65			70			dB
Output Voltage Swing	V_S = ±15V, R_L = 2kΩ	±12	±13		±12	±13		V
Supply Current	V_S = ±20V, T_A = 125°C						7	mA

DEFINITION OF TERMS

SLEW RATE The internally limited rate of change in output voltage with a large amplitude step function applied to the input.

COMMON MODE REJECTION RATIO The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

INPUT BIAS CURRENT The average of the two input currents.

INPUT OFFSET CURRENT The difference in the currents into the two input terminals when the output is at zero.

INPUT OFFSET VOLTAGE That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

INPUT RESISTANCE The ratio of the change in input voltage to the change in input current on either input with the other grounded.

INPUT VOLTAGE RANGE The range of voltages on the input terminals for which the offset specifications apply.

LARGE-SIGNAL VOLTAGE GAIN The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING The peak output voltage swing, referred to zero, that can be obtained without clipping.

POWER SUPPLY REJECTION RATIO The ratio of the change in input offset voltage to the change in power supply voltages producing it.

SUPPLY CURRENT The current required from the power supply to operate the amplifier with no load and the output at zero.

NOTES

Note 1: Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C, the Dual-In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C, and the Flat Package at 5.4 mW/°C for operation at ambient temperatures above 57°C.

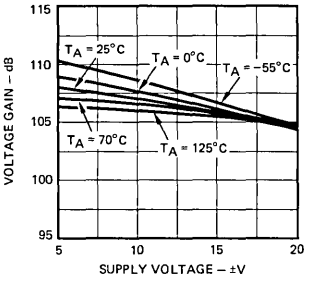
Note 2: The inputs are shunted with diodes for overvoltage protection. To limit the current in the protection diodes, resistances of 2kΩ or greater should be inserted in series with the input leads for differential input voltages greater than ±5V.

Note 3: For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.

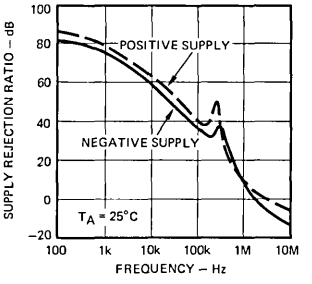
Note 4: Unless otherwise specified, these specifications apply for supply voltages from ±5V to ±20V.

PERFORMANCE CURVES

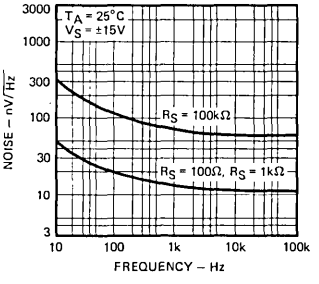
Voltage Gain



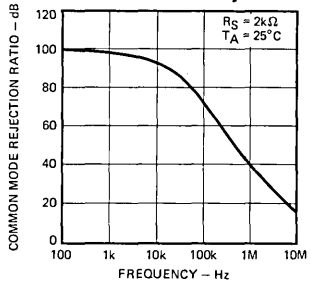
Power Supply Rejection



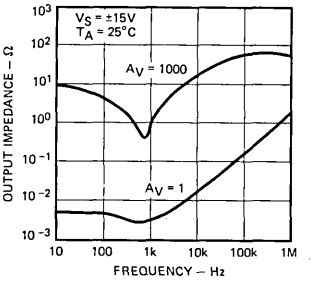
Input Noise Voltage



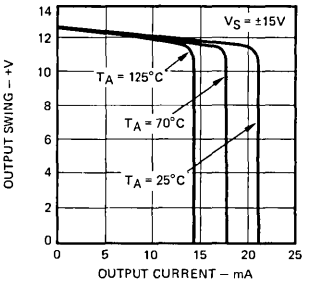
Common Mode Rejection



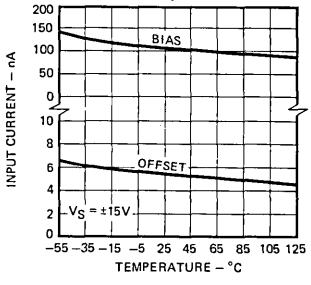
Closed Loop Output Impedance



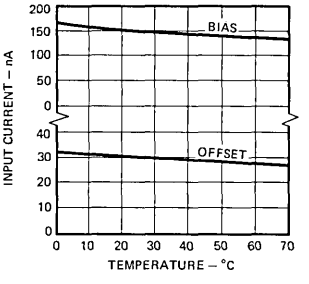
Current Limiting



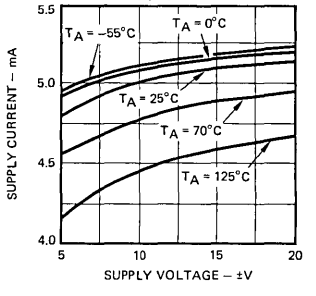
Input Current Am118, Am218



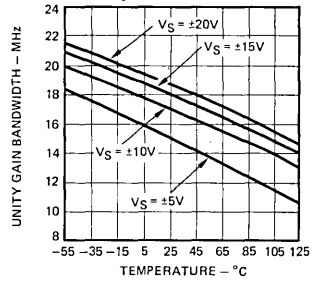
Input Current—Am318



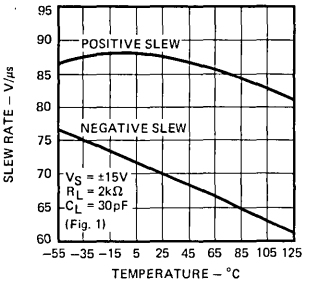
Supply Current



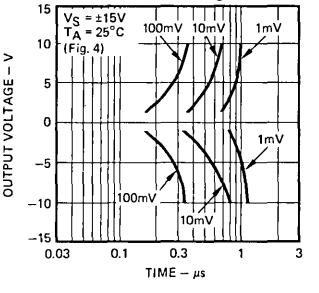
Unity Gain Bandwidth



Voltage Follower Slew Rate

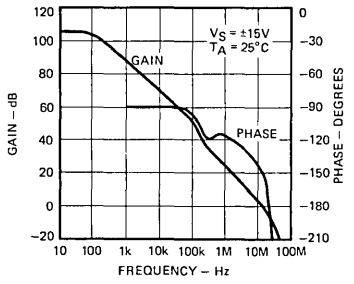


Inverter Settling Time

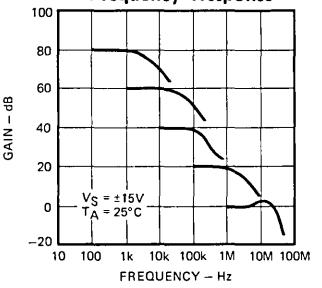


PERFORMANCE CURVES

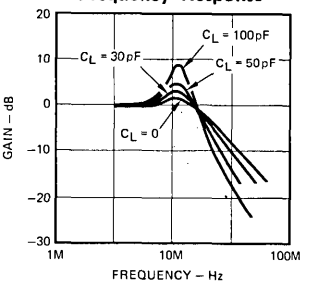
Open Loop Frequency Response



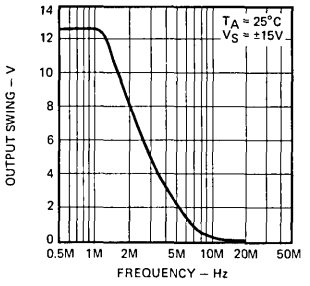
Closed Loop Frequency Response



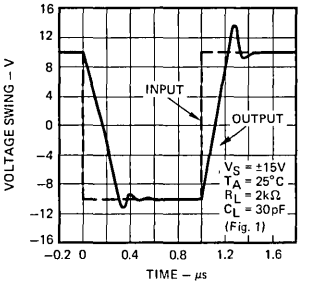
Effect of Capacitive Loading on Closed Loop Frequency Response



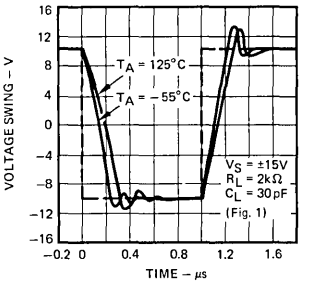
Large Signal Frequency Response



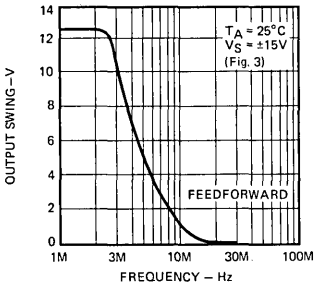
Voltage Follower Pulse Response



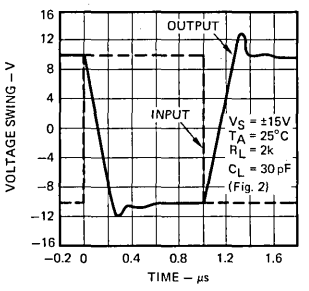
Voltage Follower Pulse Response Over Temperature



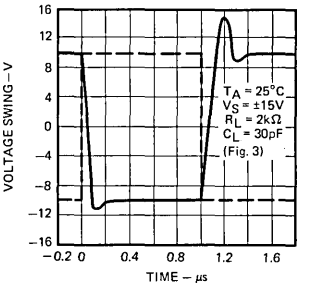
Large Signal Frequency Response with Feedforward



Inverter Pulse Response without Feedforward



Inverter Pulse Response with Feedforward



The high gain and large bandwidth of the Am118 make it mandatory to observe the following precautions in using the device, as is the case with any high-frequency amplifier. Circuit layout should be arranged to keep all lead lengths as short as possible and the output separated from the inputs. The values of the feedback and source impedances should be kept small to reduce the effect of stray capacitance at the inputs. The power supplies must be bypassed to ground at the supply leads of the amplifier with low inductance capacitors. Capacitive loading must be kept to minimum, or the amplifier must be isolated as shown in the applications.

APPLICATIONS

Voltage Follower (Slew Rate Test Circuit)

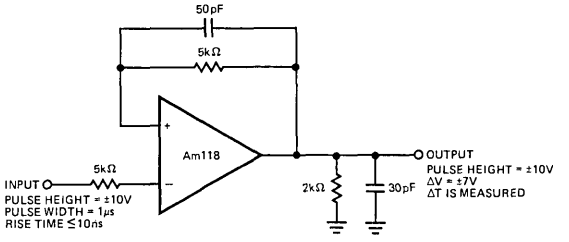


Figure 1

Inverter

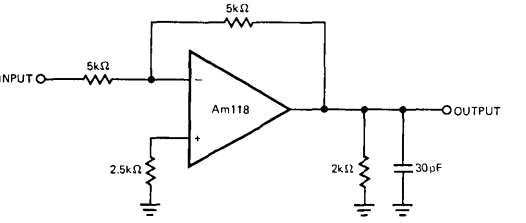


Figure 2

Inverter with Feedforward Compensation for Higher Slew Rate

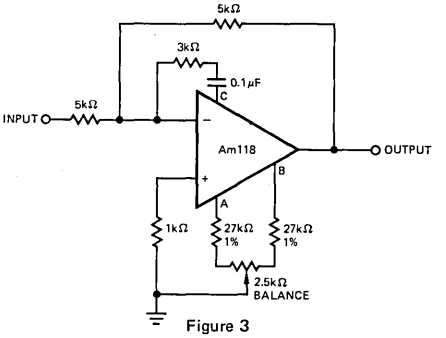


Figure 3

Compensation for Minimum Settling Time

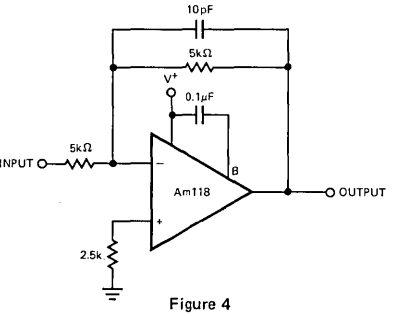


Figure 4

Offset Nulling

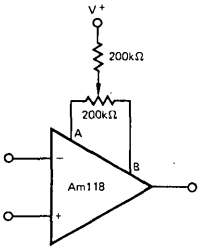


Figure 5

Isolating Large Capacitive Loads

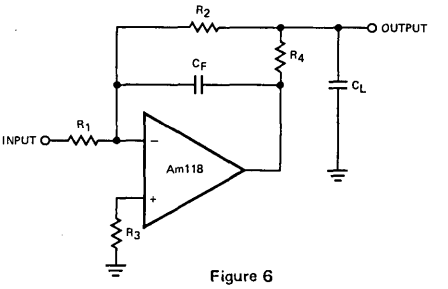


Figure 6

Over Compensation

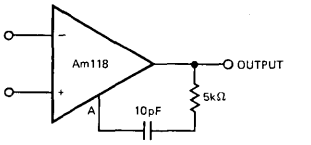


Figure 7

D/A Converter with Ladder Network

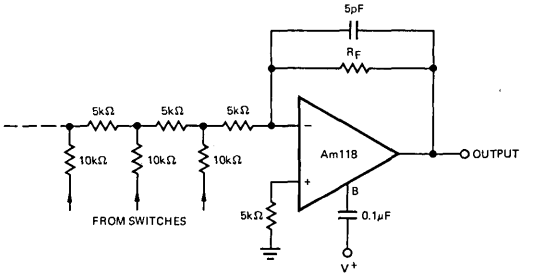


Figure 8

D/A Converter with Binary Network

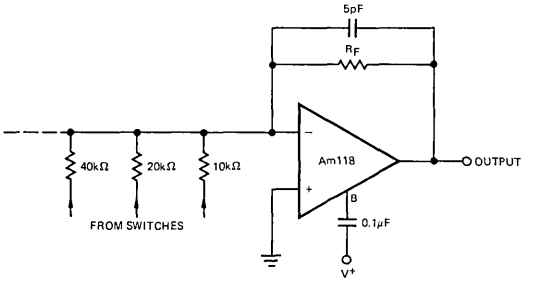


Figure 9

ADDITIONAL APPLICATIONS

High Speed Summing Amplifier with Low Input Bias Currents

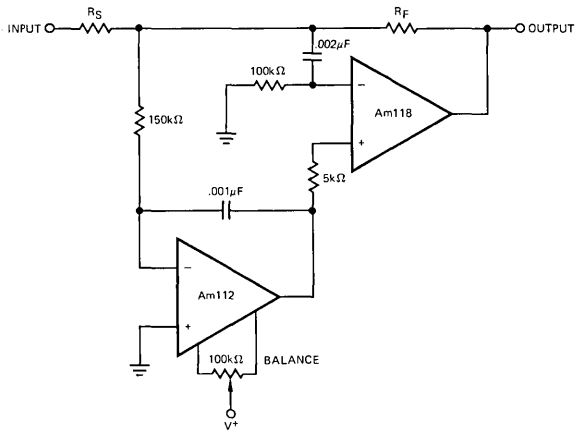
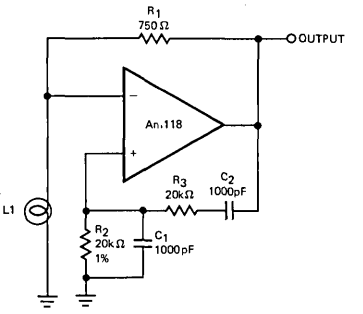


Figure 10

Wien Bridge Oscillator



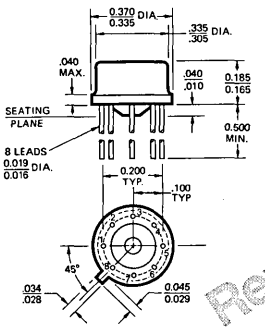
L1–10V–14mA
bulb ELDEMA 1869
$R_1 = R_2$
$C_1 = C_2$

$$f = \frac{1}{2\pi R1C1}$$

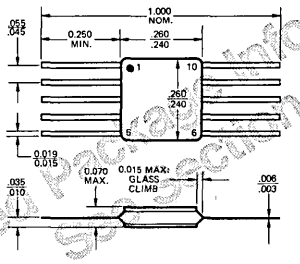
Figure 11

PHYSICAL DIMENSIONS

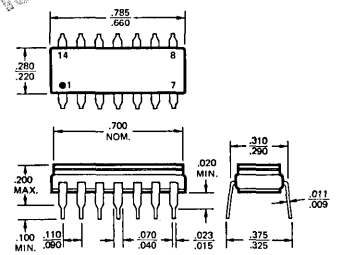
Metal Can



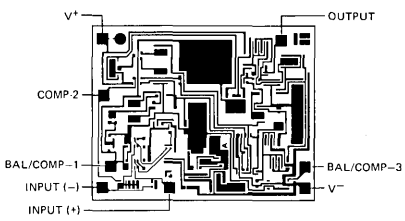
Flat Package



Dual-In-Line



Metallization and Pad Layout



ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am685
Voltage Comparator

Distinctive Characteristics:

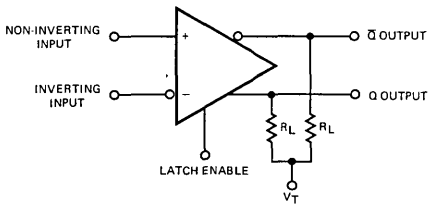
- 6.5 ns maximum propagation delay at 5 mV overdrive.
- 3.0 ns latch setup time.
- Complementary ECL outputs.
- 50Ω line driving capability
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically and optically inspected dice for assemblers of hybrid products.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Available in metal can and hermetic dual-in-line packages.

FUNCTIONAL DESCRIPTION

The Am685 is a fast voltage comparator manufactured with an advanced bipolar NPN, Schottky diode high-frequency process that makes possible very short propagation delays (6.5 ns) without sacrificing the excellent matching characteristics hitherto associated only with slow, high-performance linear IC's. The circuit has differential analog inputs and complementary logic outputs compatible with most forms of ECL. The output current capability is adequate for driving terminated 50Ω transmission lines. The low input offset and high resolution make this comparator especially suitable for high-speed precision analog-to-digital processing.

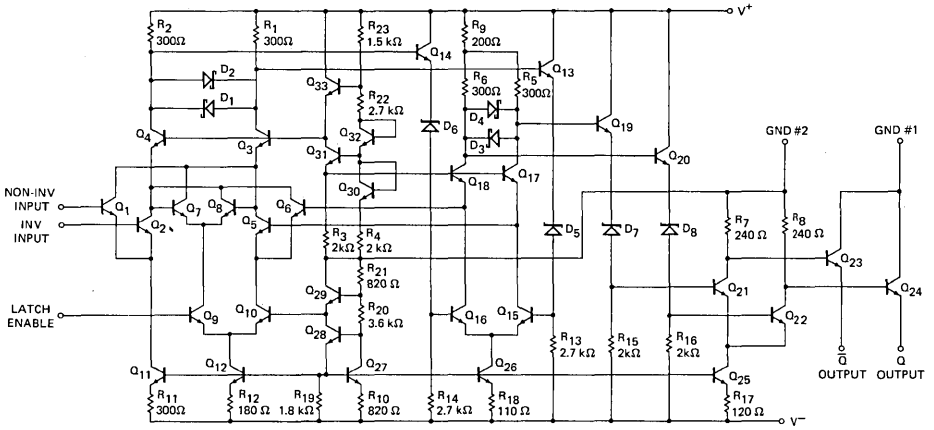
A latch function is provided to allow the comparator to be used in a sample-hold mode. If the Latch Enable input is HIGH, the comparator functions normally. When the Latch Enable is driven LOW, the comparator outputs are locked in their existing logical states. If the latch function is not used, the Latch Enable must be connected to ground.

FUNCTIONAL DIAGRAM



The outputs are open emitters, therefore external pull-down resistors are required. These resistors may be in the range of 50–200Ω connected to –2.0 V, or 200–2000Ω connected to –5.2 V.

CIRCUIT DIAGRAM



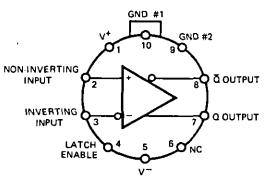
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am685	Metal Can	–30°C to +85°C	Am685HL
	DIP	–30°C to +85°C	Am685DL
Am685	Metal Can	–55°C to +125°C	Am685HM
	DIP	–55°C to +125°C	Am685DM
Am685	Dice	–30°C to +85°C	Am685XL
	Dice	–55°C to +125°C	Am685XM

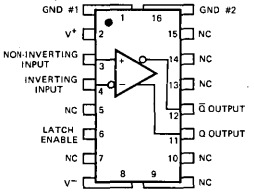
CONNECTION DIAGRAMS

Top Views

Metal Can



Dual-In-Line



NOTE 1: On metal package, pin 5 is connected to case. On DIP, pin 8 is connected to case.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Positive Supply Voltage	+7 V
Negative Supply Voltage	−7 V
Input Voltage	±4 V
Differential Input Voltage	±6 V
Output Current	30mA
Power Dissipation (Note 2)	500mW

Operating Temperature Range	
Am685-L	−30°C to +85°C
Am685-M	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 Sec.)	300°C

ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGES (Unless otherwise specified)

DC Characteristics

Symbol	Parameter (see definitions)	Conditions (Note 3)	Am685-L Min.	Am685-L Max.	Am685-M Min.	Am685-M Max.	Units
V_{OS}	Input Offset Voltage	$R_S \leq 100\,\Omega$, $T_A = 25°C$	−2.0	+2.0	−2.0	+2.0	mV
		$R_S \leq 100\,\Omega$	−2.5	+2.5	−3.0	+3.0	mV
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\,\Omega$	−10	+10	−10	+10	µV/°C
I_{OS}	Input Offset Current	$T_A = 25°C$	−1.0	+1.0	−1.0	+1.0	µA
			−1.3	+1.3	−1.6	+1.6	µA
I_B	Input Bias Current	$T_A = 25°C$		10		10	µA
				13		16	µA
R_{IN}	Input Resistance	$T_A = 25°C$	6.0		6.0		kΩ
C_{IN}	Input Capacitance	$T_A = 25°C$		3.0		3.0	pF
V_{CM}	Input Voltage Range		−3.3	+3.3	−3.3	+3.3	V
CMRR	Common Mode Rejection Ratio	$R_S \leq 100\,\Omega$, $-3.3 \leq V_{CM} \leq +3.3$ V	80		80		dB
SVRR	Supply Voltage Rejection Ratio	$R_S \leq 100\,\Omega$, $\Delta V_S = \pm 5\%$	67		67		dB
V_{OH}	Output HIGH Voltage	$T_A = 25°C$	−0.960	−0.810	−0.960	−0.810	V
		$T_A = T_{A(min.)}$	−1.060	−0.890	−1.100	−0.920	V
		$T_A = T_{A(max.)}$	−0.890	−0.700	−0.850	−0.620	V
V_{OL}	Output LOW Voltage	$T_A = 25°C$	−1.850	−1.650	−1.850	−1.650	V
		$T_A = T_{A(min.)}$	−1.890	−1.675	−1.910	−1.690	V
		$T_A = T_{A(max.)}$	−1.825	−1.625	−1.810	−1.575	V
I^+	Positive Supply Current			23		23	mA
I^-	Negative Supply Current			29		29	mA
P_{DISS}	Power Dissipation			325		325	mW

Switching Characteristics (V_{in} = 100 mV, V_{od} = 5 mV)

Symbol	Parameter	Conditions	Am685-L Min.	Am685-L Max.	Am685-M Min.	Am685-M Max.	Units
t_{pd+}	Input to Output HIGH	$T_{A(min.)} \leq T_A \leq 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	5.5	12	ns
t_{pd-}	Input to Output LOW	$T_{A(min.)} \leq T_A \leq 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	5.5	12	ns
$t_{pd+(E)}$	Latch Enable to Output HIGH (Note 4)	$T_{A(min.)} \leq T_A \leq 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	5.5	12	ns
$t_{pd-(E)}$	Latch Enable to Output LOW (Note 4)	$T_{A(min.)} \leq T_A \leq 25°C$	4.5	6.5	4.5	6.5	ns
		$T_A = T_{A(max.)}$	5.0	9.5	5.5	12	ns
t_s	Minimum Set-up Time (Note 4)	$T_{A(min.)} \leq T_A \leq 25°C$		3.0		3.0	ns
		$T_A = T_{A(max.)}$		4.0		6.0	ns
t_h	Minimum Hold Time (Note 4)	$T_{A(min)} \leq T_A \leq T_{A(max.)}$		1.0		1.0	ns
$t_{pw(E)}$	Minimum Latch Enable Pulse Width (Note 4)	$T_{A(min.)} \leq T_A \leq 25°C$		3.0		3.0	ns
		$T_A = T_{A(max.)}$		4.0		5.0	ns

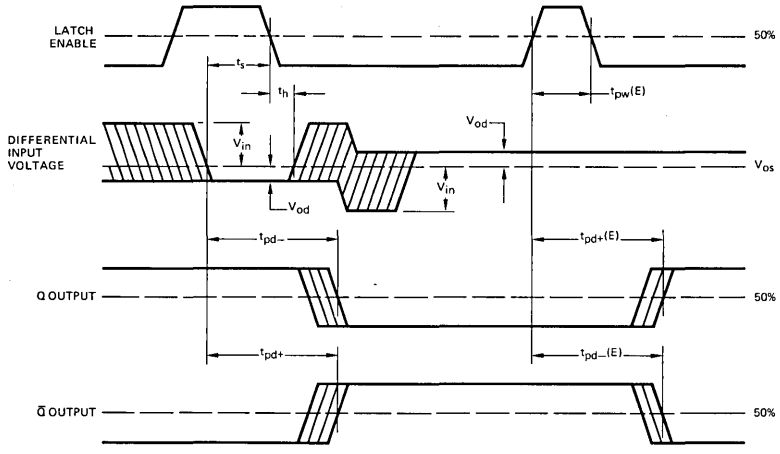
NOTES:

2: For the metal can package, derate at 6.8 mW/°C for operation at ambient temperatures above +100°C; for the dual-in-line package, derate at 9 mW/°C for operation at ambient temperatures above +105°C.

3: Unless otherwise specified $V^+ = 6.0$V, $V^- = -5.2$V, $V_T = -2.0$V, and $R_L = 50\Omega$; all switching characteristics are for a 100 mV input step with 5 mV overdrive. The specifications given for V_{os}, I_{os}, I_B, CMRR, SVRR, t_{pd+} and t_{pd-} apply over the full V_{CM} range and for ±5% supply voltages. The Am685 is designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 LFPM or greater.

4: Owing to the difficult and critical nature of switching measurements involving the latch, these parameters can not be tested in production. Engineering data indicates that at least 95% of the units will meet the specifications given.

TIMING DIAGRAM



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN

Figure 1

The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signal changes occurring before t_s will be detected and held; those occurring after t_h will not be detected. Changes between t_s and t_h may or may not be detected.

DEFINITION OF TERMS

V_{OS} **INPUT OFFSET VOLTAGE** – That voltage which must be applied between the two input terminals through two equal resistances to obtain zero voltage between the two outputs.

$\Delta V_{OS}/\Delta T$ **AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET VOLTAGE** – The ratio of the change in input offset voltage over the operating temperature range to the temperature range.

I_{OS} **INPUT OFFSET CURRENT** – The difference between the currents into the two input terminals when there is zero voltage between the two outputs.

I_B **INPUT BIAS CURRENT** – The average of the two input currents.

R_{IN} **INPUT RESISTANCE** – The resistance looking into either input terminal with the other grounded.

C_{IN} **INPUT CAPACITANCE** – The capacitance looking into either input terminal with the other grounded.

V_{CM} **INPUT VOLTAGE RANGE** – The range of voltages on the input terminals for which the offset and propagation delay specifications apply.

CMRR **COMMON MODE REJECTION RATIO** – The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

SVRR **SUPPLY VOLTAGE REJECTION RATIO** – The ratio of the change in input offset voltage to the change in power supply voltages producing it.

V_{OH} **OUTPUT HIGH VOLTAGE** – The logic HIGH output voltage with an external pull-down resistor returned to a negative supply.

V_{OL} **OUTPUT LOW VOLTAGE** – The logic LOW output voltage with an external pull-down resistor returned to a negative supply.

I^+ **POSITIVE SUPPLY CURRENT** – The current required from the positive supply to operate the comparator.

I^- **NEGATIVE SUPPLY CURRENT** – The current required from the negative supply to operate the comparator.

P_{DISS} **POWER DISSIPATION** – The power dissipated by the comparator with both outputs terminated in 50Ω to -2.0V.

SWITCHING TERMS (refer to Fig. 1)

t_{pd+} **INPUT TO OUTPUT HIGH DELAY** – The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output LOW to HIGH transition.

t_{pd-} **INPUT TO OUTPUT LOW DELAY** – The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

$t_{pd+(E)}$ **LATCH ENABLE TO OUTPUT HIGH DELAY** – The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output LOW to HIGH transition.

$t_{pd-(E)}$ **LATCH ENABLE TO OUTPUT LOW DELAY** – The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output HIGH to LOW transition.

t_s **MINIMUM SET-UP TIME** – The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

t_h **MINIMUM HOLD TIME** – The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

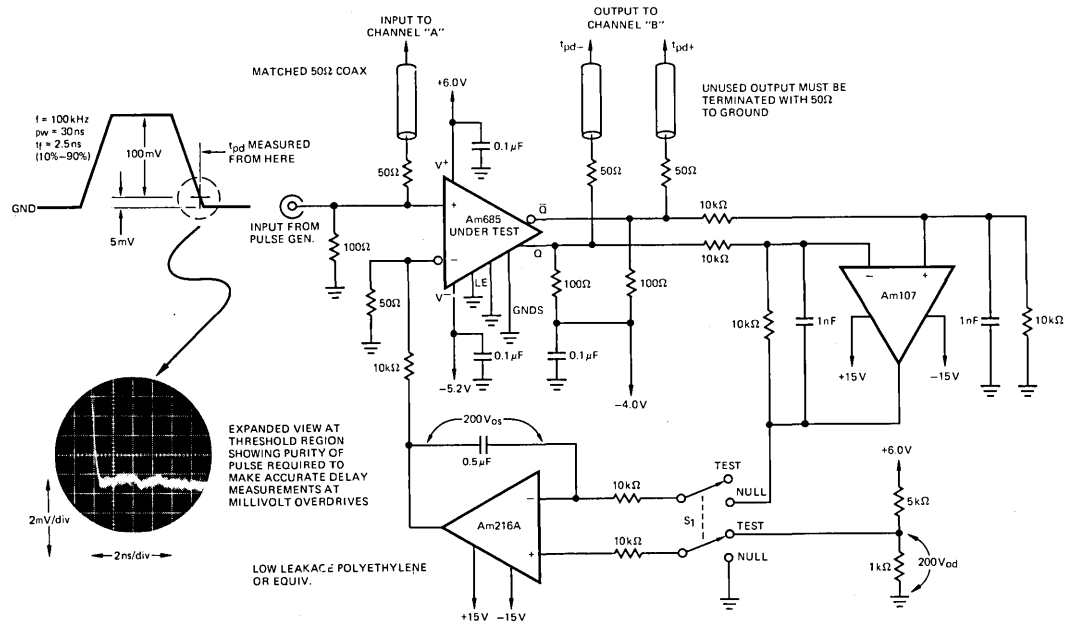
$t_{pw(E)}$ **MINIMUM LATCH ENABLE PULSE WIDTH** – The minimum time that the Latch Enable signal must be HIGH in order to acquire and hold an input signal change.

OTHER SYMBOLS

T_A Ambient temperature
R_S Input source resistance
V_S Supply voltages
V^+ Positive supply voltage
V^- Negative supply voltage
V_T Output load terminating voltage
R_L Output load resistance
V_{in} Input pulse amplitude
V_{od} Input overdrive
f Frequency

MEASUREMENT OF PROPAGATION DELAY

A voltage comparator must be able to respond to input signal levels ranging from a few millivolts to several volts, ideally with little variation in propagation delay. The most difficult condition is where the comparator has been driven hard into one state by a large signal, and the next input signal is just barely enough to make it switch to the other state. This forces the input stage of the circuit to swing from a full off (or on) state to a point somewhere near the center of its linear range, thus exercising both its large- and small-signal responses. If the comparator is fast for this condition, it should be as fast or faster for almost any other condition. The unofficial industry standard input signal is a 100mV step with an overdrive of 5mV (the overdrive is the voltage in excess of that needed to bring the output to the center of its dynamic range). The 100mV is more than enough to fully turn on the input stage, but not so large to make measurement a problem. Large pulses would require exceptionally good control on waveform purity, since only a few tenths of a percent of overshoot or ripple would be enough to affect the value of the overdrive and, for sensitive comparators, result in false switching. The propagation delay is measured from the time the input signal crosses the input threshold voltage (i.e., the offset voltage) to the 50% point of either output. This definition ensures that each unit is measured under equal conditions, and also makes the measurement relatively independent of the input rise and fall times.



The test circuit of Figure 2 provides a means of automatically nulling out the offset voltage and applying the overdrive. With S1 in the "NULL" position, the feedback loop around the Am685 via the two operational amplifiers corrects for the offset of the circuit including any dc shift in the ground level of the input signal. When switched to "TEST", the offset is held on the storage capacitor of the Am216A and the overdrive is added at the Am216A non-inverting input. The duty cycle of the signal is made low so that the presence of the input pulse during nulling will not disturb the offset. A solid ground plane is used for the test jig, and capacitors bypass the supply voltages. All power and signal leads are kept as short as possible. The Am685 input and output run directly into the 50Ω inputs of the sampling scope via equal lengths of 50Ω coaxial cable. For the conditions shown in the figure, t_{pd+} is measured at the $\overline{Q}$ output and t_{pd-} at the Q output. If it is desired to measure the opposite output polarities, the polarities of the input signal and overdrive must be reversed.

THERMAL CONSIDERATIONS

To achieve the high speed of the Am685, a certain amount of power must be dissipated as heat. This increases the temperature of the die relative to the ambient temperature. In order to be compatible with ECL III and ECL 10,000, which normally use air flow as a means of package cooling, the Am685 characteristics are specified when the device has an air flow across the package of 500 linear feet per minute or greater. Thus, even though different ECL circuits on a printed circuit board may have different power dissipations, all will have the same input and output levels, etc., provided each sees the same air flow and air temperature. This eases design, since the only change in characteristics between devices is due to the increase in ambient temperature of the air passing over the devices. If the Am685 is operated without air flow, the change in electrical characteristics due to the increased die temperature must be taken into account.

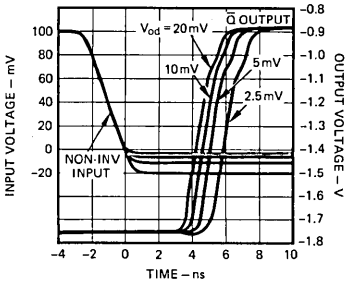
INTERCONNECTION TECHNIQUES

All high-speed ECL circuits require that special precautions be taken for optimum system performance. The Am685 is particularly critical because it features very high gain (60dB) at very high frequencies (100MHz). A ground plane must be provided for a good, low inductance, ground current return path. The impedance at the inputs should be as low as possible and lead lengths as short as practical. It is preferable to solder the device directly to the printed circuit board instead of using a socket. Open wiring on the outputs should be limited to less than one inch, since severe ringing occurs beyond this length. For longer lengths, the printed-circuit interconnections become microstrip transmission lines when backed up by a ground plane, with a characteristic impedance of 50 to 150Ω. Reflections will occur unless the line is terminated in its characteristic impedance. The termination resistors normally go to -2.0V, but a Thevenin equivalent to V^- can be used at some increase in power. Best results are usually obtained with the terminating resistor at the end of the driven line. The lower impedance lines are more suitable for driving capacitive loads. The supply voltages should be well decoupled with RF capacitors connected to the ground plane as close to the device supply pins as possible.

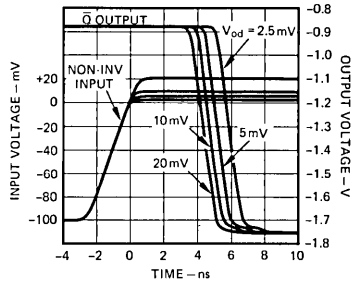
PERFORMANCE CURVES

(Unless otherwise specified, standard conditions for all curves are $T_A = 25°C$, $V^+ = 6.0V$, $V^- = -5.2V$, $V_T = -2.0V$, $R_L = 50\Omega$, and switching characteristics are for $V_{in} = 100mV$, $V_{od} = 5mV$.)

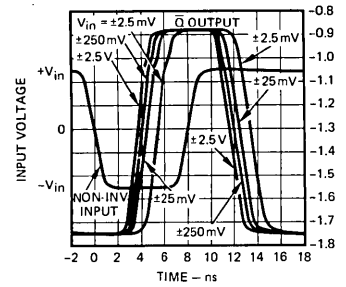
Response for Various Input Overdrives



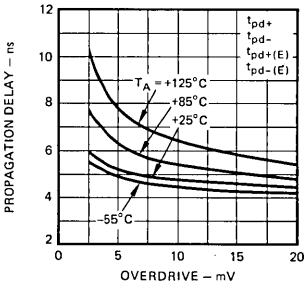
Response for Various Input Overdrives



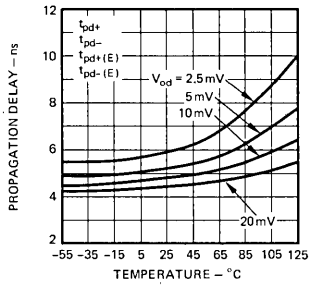
Response for Various Input Signal Levels



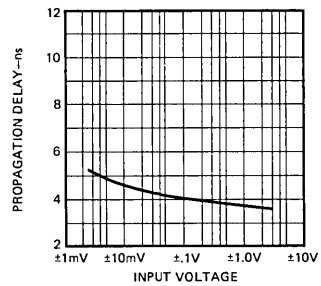
Propagation Delays as a Function of Input Overdrive



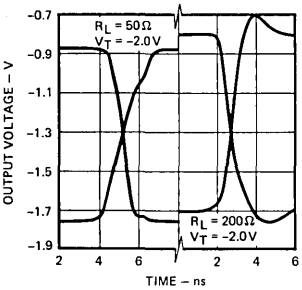
Propagation Delays as a Function of Temperature



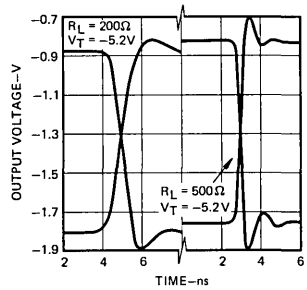
Propagation Delay as a Function of Input Signal Level



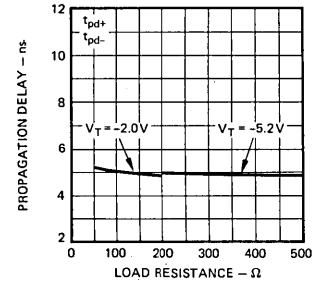
Response for Various Load Resistances



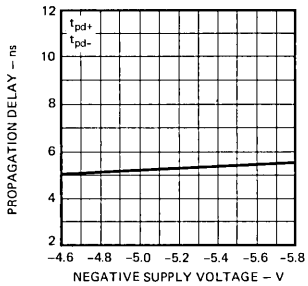
Response for Various Load Resistances



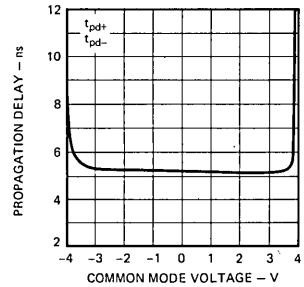
Propagation Delays as a Function of Load Resistance



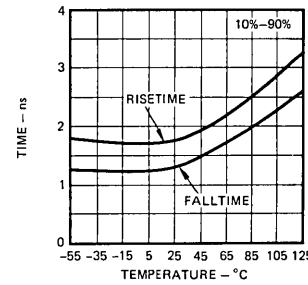
Propagation Delays as a Function of Negative Supply Voltage



Propagation Delays as a Function of Common Mode Voltage



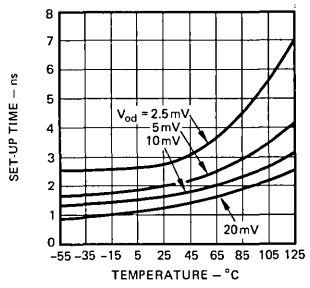
Output Rise and Fall Times as a Function of Temperature



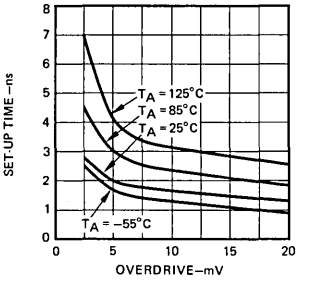
PERFORMANCE CURVES (Cont.)

(Unless otherwise specified, standard conditions for all curves are T_A = 25°C, V^+ = 6.0V, V^- = −5.2V, V_T = −2.0V, R_L = 50Ω, and switching characteristics are for V_{in} = 100mV, V_{od} = 5mV.)

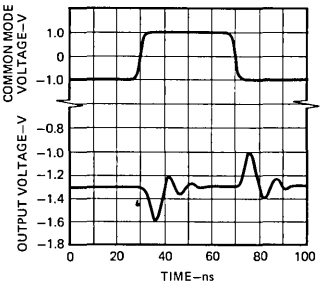
Set-up Time as a Function of Temperature



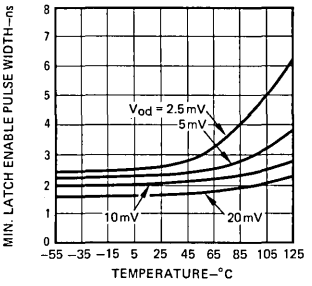
Set-up Time as a Function of Input Overdrive



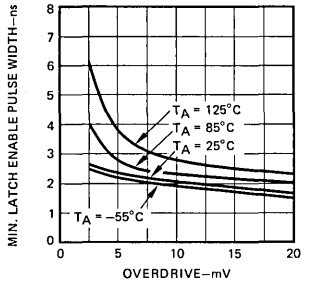
Common Mode Pulse Response



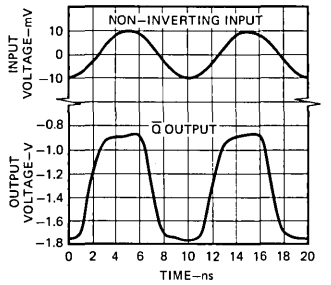
Min. Latch Enable Pulse Width as a Function of Temperature



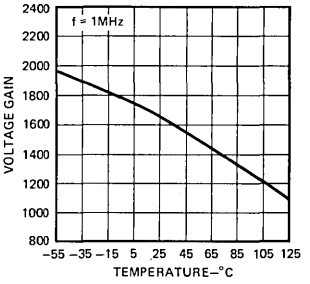
Min. Latch Enable Pulse Width as a Function of Input Overdrive



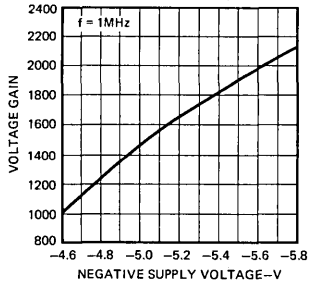
Response to 100MHz Sine Wave



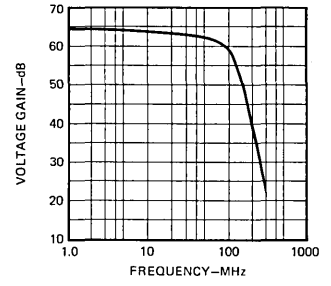
Voltage Gain as a Function of Temperature



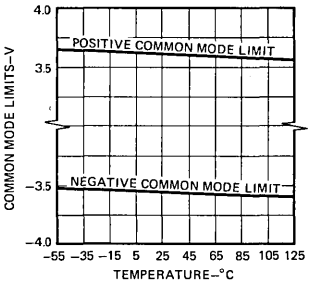
Voltage Gain as a Function of Negative Supply Voltage



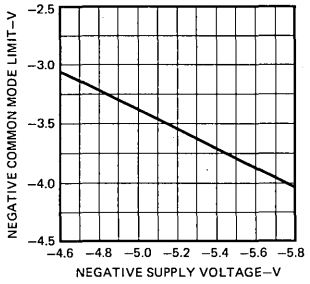
Voltage Gain as a Function of Frequency



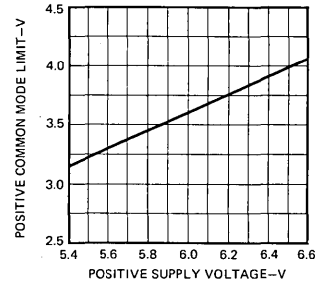
Common Mode Limits as a Function of Temperature



Negative Common Mode Limit as a Function of Negative Supply Voltage



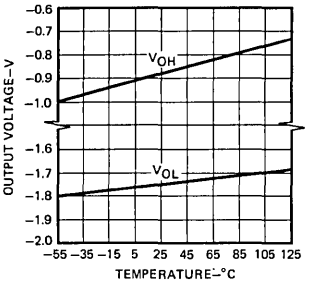
Positive Common Mode Limit as a Function of Positive Supply Voltage



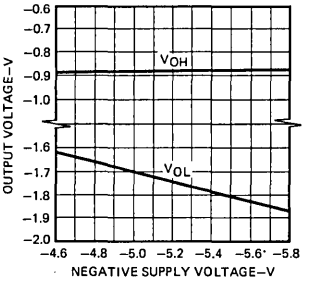
PERFORMANCE CURVES (Cont.)

(Unless otherwise specified, standard conditions for all curves are $T_A = 25°C$, $V^+ = 6.0V$, $V^- = -5.2V$, $V_T = -2.0V$, $R_L = 50\Omega$, and switching characteristics are for $V_{in} = 100mV$, $V_{od} = 5mV$.)

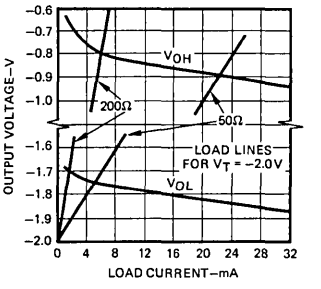
Output Levels as a Function of Temperature



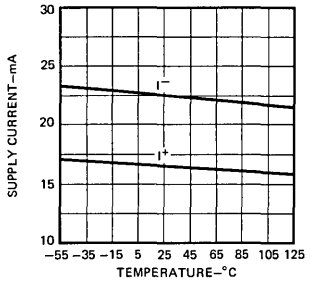
Output Levels As A Function Of Negative Supply Voltage



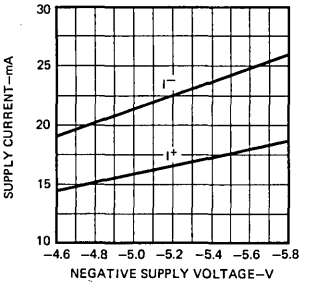
Output Levels As A Function Of DC Loading



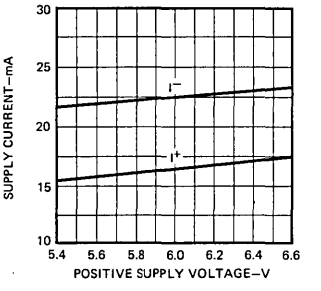
Supply Currents As A Function Of Temperature



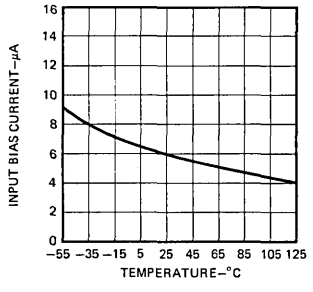
Supply Currents As A Function Of Negative Supply Voltage



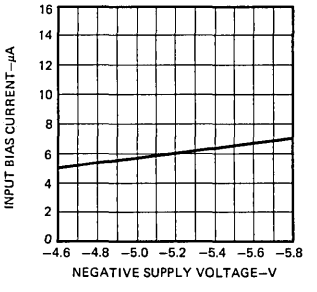
Supply Currents As A Function Of Positive Supply Voltage



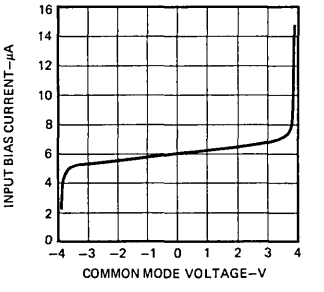
Input Bias Current As A Function Of Temperature



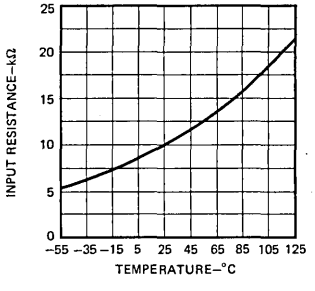
Input Bias Current As A Function Of Negative Supply Voltage



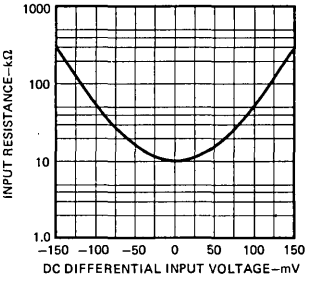
Input Bias Current As A Function Of Common Mode Voltage



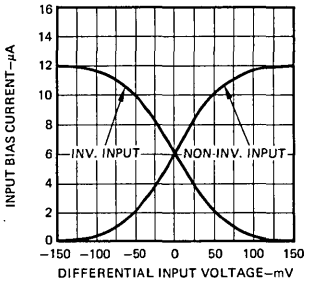
Input Resistance As A Function Of Temperature



Input Resistance As A Function Of DC Differential Input Voltage

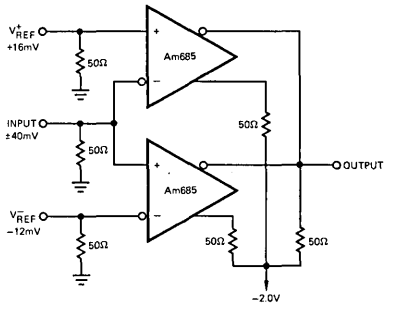


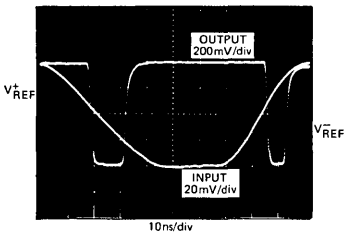
Input Current As A Function Of Differential Input Voltage



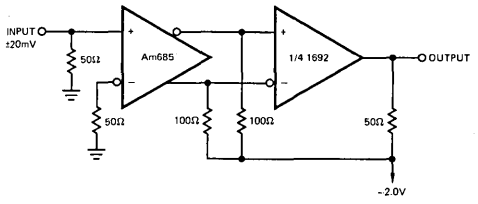
TYPICAL APPLICATIONS
($T_A = 25°C$)

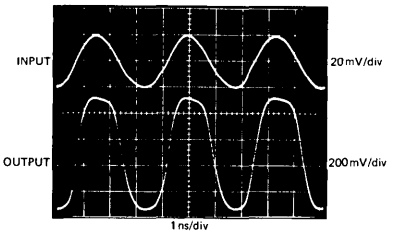
High-Speed Window Detector



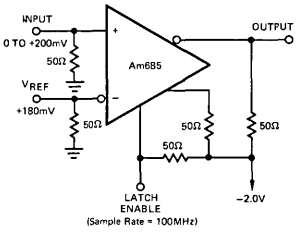


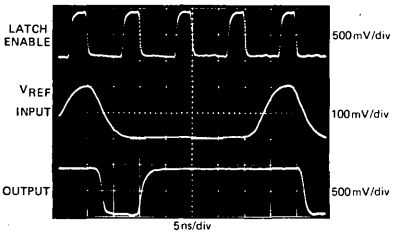
300MHz Line Receiver





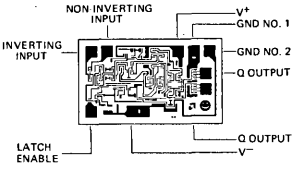
High-Speed Sampling





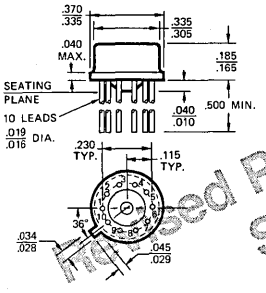
Metallization and Pad Layout

32 x 54 Mils

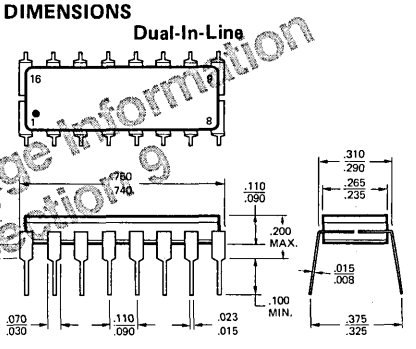


PHYSICAL DIMENSIONS

Metal Can



Dual-In-Line



ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am715/715C
High-Speed Operational Amplifier

Description: The Am715 and Am715C high-speed operational amplifiers are functionally, electrically, and pin-for-pin equivalent to the Fairchild μA715 and μA715C. Both are available in the hermetic metal can, dual-in-line, and flat packages.

Distinctive Characteristics: 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL-STD-883.

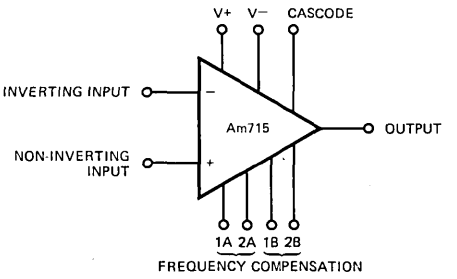
Mixing privileges for obtaining price discounts. Refer to price list.

Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

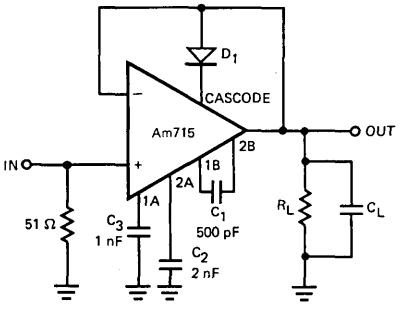
The Am715 is a differential input, single-ended output operational amplifier having wide bandwidth and high slew rate. It has internal lead compensation and four points for external lag compensation networks, providing many possible combinations of frequency compensation. In addition, a point is brought out for use with an external diode to prevent latch-up in voltage follower applications.

FUNCTIONAL DIAGRAM

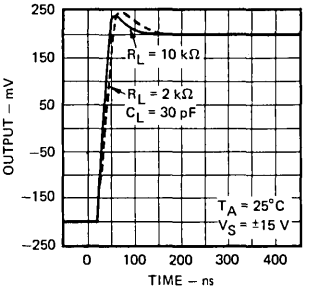


APPLICATIONS

Voltage Follower



Voltage Follower Small-Signal Pulse Response



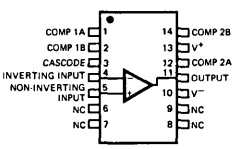
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am715C	Metal Can	0°C - 70°C	U5F7715393
	DIP	0°C - 70°C	U6W7715393
Am715	Metal Can	−55°C - +125°C	U5F7715312
	DIP	−55°C - +125°C	U6W7715312
	Flat Pak	−55°C - +125°C	U3F7715312
Am715	Dice	Note 4	UXX7715XXD

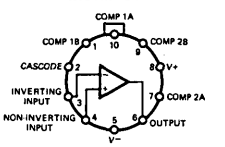
Note: The dice supplied will contain units which meet both 0°C to +70°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAMS
Top Views

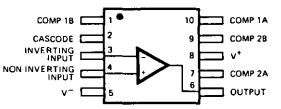
Dual-In-Line



Metal Can



Flat Package



NOTES:
(1) On Metal Can, pin 5 is connected to case.
(2) On DIP, pin10is connected to bottom of package.
(3) On Flat Package, pin 5 is connected to bottom of package.

MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±6 V
Input Voltage (Note 2)	±15 V
Operating Temperature Range	
Am715C	0°C to +70°C
Am715	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

Parameter (see definitions)	Conditions	Am715C Min	Am715C Typ	Am715C Max	Am715 Min	Am715 Typ	Am715 Max	Units
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	7.5		2.0	5.0	mV
Input Offset Current			70	250		70	250	nA
Input Bias Current			0.4	1.5		0.4	0.75	μA
Input Resistance			1.0			1.0		MΩ
Input Voltage Range		±10	±12		±10	±12		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	74	92		74	92		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		70	400		70	300	μV/V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	10	30		15	30		V/mV
Output Voltage Swing	$R_L \geq 2$ kΩ	±10	±13		±10	±13		V
Output Resistance			75			75		Ω
Supply Current			5.5	10		5.5	7.0	mA
Power Consumption			165	300		165	210	mW
Transient Response (Voltage Follower) Risetime	$V_{out} = \pm 200$ mV, $R_L = 2$ kΩ, $C_L = 30$ pF		30	75		30	60	ns
Overshoot			30	50		30	40	%
Slew Rate	Av = 100 (Fig. 8) $V_{out} = 0$ to +10 V,		65			65		V/μs
	Av = 10 (Fig. 7) $R_L = 2$ kΩ,		40			40		V/μs
	Av = 1 (Figs. 1 & 2) $C_L = 30$ pF	10	20		15	20		V/μs
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 10$ kΩ			10			7.5	mV
Input Offset Current	$T_A = T_{A\,max}$			250			250	nA
	$T_A = T_{A\,min}$			750			800	nA
Input Bias Current	$T_A = T_{A\,max}$			1.5			0.75	μA
	$T_A = T_{A\,min}$			7.5			4.0	μA
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	74			74			dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ			400			300	μV/V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	8.0			10			V/mV
Output Voltage Swing	$R_L \geq 2$ kΩ	±10			±10			V

PERFORMANCE CURVES

Voltage Follower

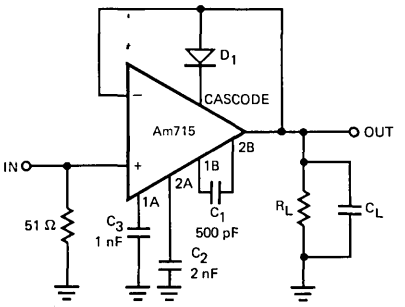


Figure 1

X1 Inverting Amplifier

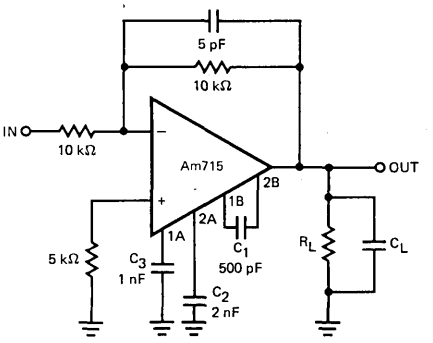
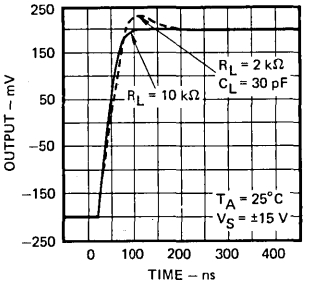


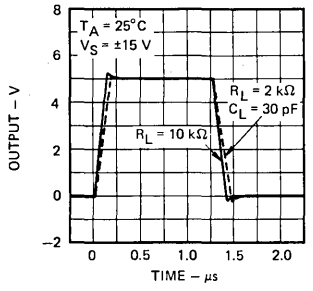
Figure 2

The high gain and large bandwidth of the Am715 make it mandatory to observe the following precautions in using the device, as is the case with any high frequency amplifier. Circuit layout should be arranged to keep all lead lengths as short as possible and the output separated from the inputs and frequency compensation pins. The values of the feedback and source impedances should be kept small to reduce the effect of stray capacitance of the inputs. The power supplies must be bypassed to ground at the supply leads of the amplifier with low inductance capacitors. Capacitive loading must be kept to an absolute minimum, since the amplifier cannot tolerate more than 30 pF directly at its output with full feedback.

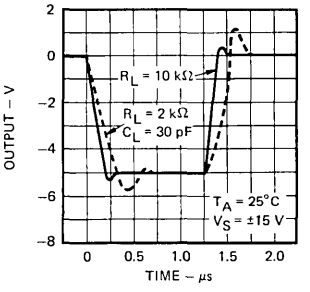
X1 Inverter Small-Signal Pulse Response



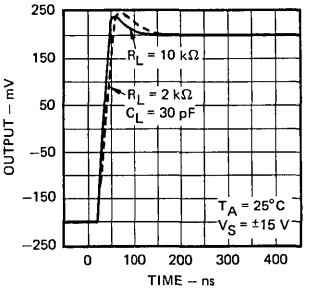
Follower & X1 Inverter Positive Large-Signal Pulse Response



Follower & X1 Inverter Negative Large-Signal Pulse Response



Voltage Follower Small-Signal Pulse Response



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT The difference in the currents into the two input terminals with the output at zero volts.

INPUT BIAS CURRENT The average of the two input currents.

INPUT RESISTANCE The resistance looking into either input terminal with the other grounded.

LARGE-SIGNAL VOLTAGE GAIN The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT RESISTANCE The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

SUPPLY CURRENT The DC current from the supplies required to operate the amplifier with the output at zero and with no load current.

POWER CONSUMPTION The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE The closed-loop step-function response of the amplifier under small-signal conditions.

SLEW RATE The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

INPUT VOLTAGE RANGE The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

COMMON MODE REJECTION RATIO The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO The ratio of the change in input offset voltage to the change in supply voltage producing it.

OUTPUT VOLTAGE SWING The peak output swing, referred to zero, that can be obtained without clipping.

NOTES

Note 1: Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C and the Dual In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C, the Flat Package at 5.4 mW/°C for operation at ambient temperatures above 57°C.

Note 2: For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.

X10 Amplifier

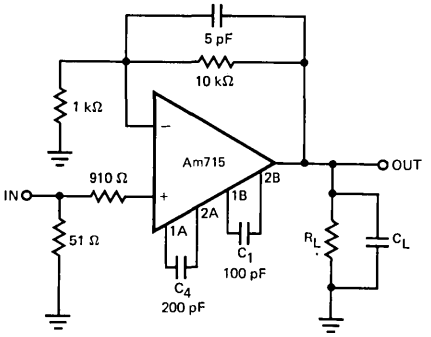


Figure 3

X100 Amplifier

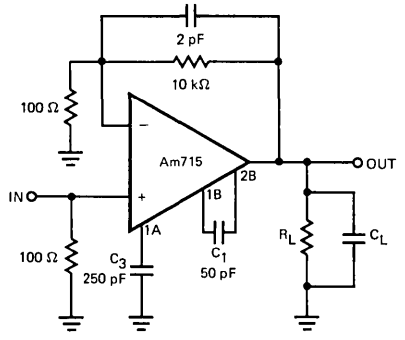
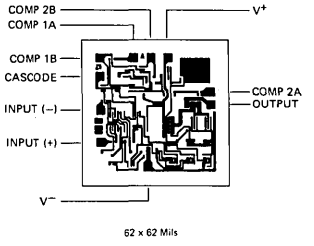


Figure 4

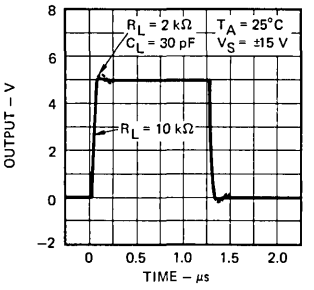
Metallization and Pad Layout



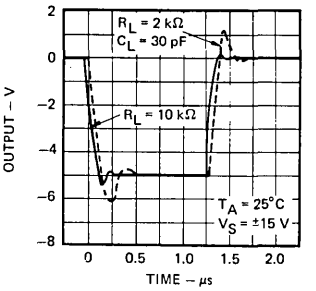
62 x 62 Mils

PERFORMANCE CURVES

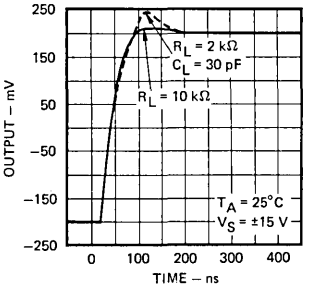
X10 Amplifier Positive Large-Signal Pulse Response



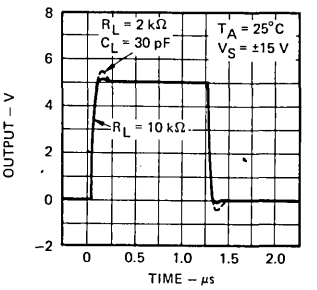
X10 Amplifier Negative Large-Signal Pulse Response



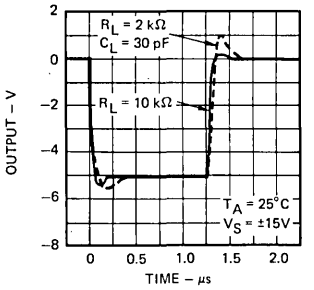
X10 Amplifier Small-Signal Pulse Response



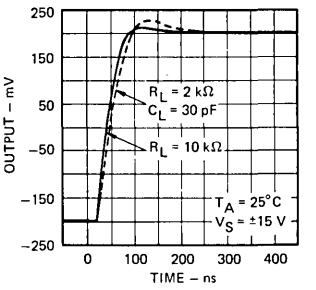
X100 Amplifier Positive Large-Signal Pulse Response



X100 Amplifier Negative Large-Signal Pulse Response

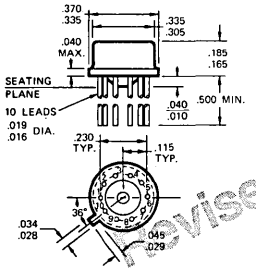


X100 Amplifier Small-Signal Pulse Response

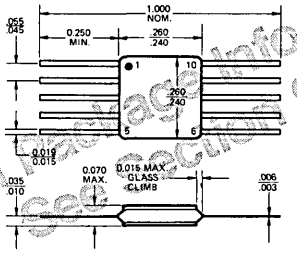


PHYSICAL DIMENSIONS

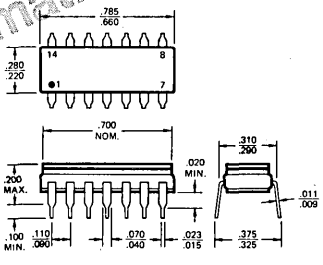
Metal Can



Flat Package



Dual-In-Line



ADVANCED
MICRO
DEVICES INC.
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California 94086
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TWX: 910-339-9280
TELEX: 34-6306

Am723/723C
Voltage Regulator

Description: The Am723 and Am723C monolithic voltage regulators are functionally and electrically equivalent to the Fairchild μA723 and μA723C. Both are available in the hermetic dual-in-line and metal can packages and are pin for pin replacements for the Fairchild μA723 and μA723C.

Distinctive Characteristics: 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL-STD-883.

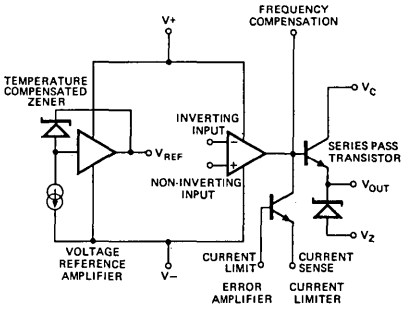
Mixing privileges for obtaining price discounts. Refer to price list.

Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

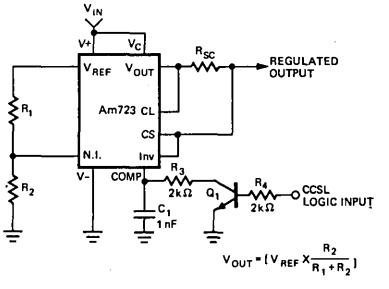
The Am723 is intended for use with positive or negative supplies as a series, shunt, switching or floating regulator. It is applicable to remote shutdown and current limiting operations and will accept either PNP or NPN external pass elements to increase output current capability.

FUNCTIONAL DIAGRAM



APPLICATIONS

REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING (V_{out} = 2 to 7 Volts)



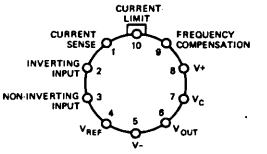
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am723C	DIP	0°C - 70°C	U6A7723393
	Metal Can	0°C - 70°C	U5R7723393
Am723	DIP	−55°C - 125°C	U6A7723312
	Metal Can	−55°C - 125°C	U5R7723312
Am723	Dice	Note	UXX7723XXD

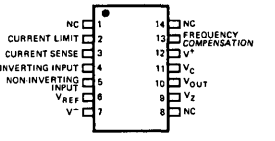
Note : The dice supplied will contain units which meet both 0°C to +70°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAMS
Top Views

Metal Can



Dual-In-Line



NOTES: (1) On Metal Can, pin 5 is connected to case.
(2) On DIP, pin 7 is connected to case.

MAXIMUM RATINGS

Pulse Voltage from V^+ to V^- (50 msec)	50 V
Continuous Voltage from V^+ to V^-	40 V
Input-Output Voltage Differential	40 V
Maximum Output Current	150 mA
Current from V_Z	25 mA
Current from V_{REF}	15 mA
Internal Power Dissipation (Note 1)	
Metal Can	850 mW
DIP	900 mW
Operating Temperature Range	
Am723C	0°C to +70°C
Am723	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 2)

Parameter (see definitions)	Conditions	Am723C Min	Am723C Typ	Am723C Max	Am723 Min	Am723 Typ	Am723 Max	Units
Line Regulation (Note 3)	V_{IN} = 12 V to V_{IN} = 15 V		0.01	0.1		0.01	0.1	% V_{OUT}
	V_{IN} = 12 V to V_{IN} = 40 V		0.1	0.5		0.02	0.2	% V_{OUT}
Load Regulation (Note 3)	I_L = 1 mA to I_L = 50 mA		0.03	0.2		0.03	0.15	% V_{OUT}
Ripple Rejection	f = 50 Hz to 10 kHz, C_{REF} = 0		74			74		dB
	f = 50 Hz to 10 kHz, C_{REF} = 5 μF		86			86		dB
Short Circuit Current Limit	R_{SC} = 10 Ω, V_{OUT} = 0		65			65		mA
Reference Voltage		6.80	7.15	7.50	6.95	7.15	7.35	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, C_{REF} = 0		20			20		μV_{rms}
	BW = 100 Hz to 10 kHz, C_{REF} = 5 μF		2.5			2.5		μV_{rms}
Long Term Stability			0.1			0.1		%/1000 hrs
Standby Current Drain	I_L = 0, V_{IN} = 30 V		2.3	4.0		2.3	3.5	mA
Input Voltage Range		9.5		40	9.5		40	V
Output Voltage Range		2.0		37	2.0		37	V
Input-Output Voltage Differential		3.0		38	3.0		38	V
The Following Specifications Apply Over The Operating Temperature Ranges								
Line Regulation	V_{IN} = 12 V to V_{IN} = 15 V			0.3			0.3	% V_{OUT}
Load Regulation	I_L = 1 mA to I_L = 50 mA			0.6			0.6	% V_{OUT}
Average Temperature Coefficient of Output Voltage			0.003	0.015		0.002	0.015	%/°C

DEFINITION OF TERMS

AVERAGE TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE The percentage change in output voltage for a specified change in ambient temperature.

CURRENT LIMIT SENSE VOLTAGE The voltage between current sense and current limit terminals necessary to cause current limiting.

INPUT-OUTPUT VOLTAGE DIFFERENTIAL The range of voltage difference between the supply voltage and the regulated output voltage over which the regulator will operate.

INPUT VOLTAGE RANGE The range of supply voltage over which the regulator will operate.

LINE REGULATION The percentage change in output voltage for a specified change in input voltage.

LOAD REGULATION The percentage change in output voltage for a specified change in load current.

OUTPUT NOISE VOLTAGE The rms output noise voltage with constant load and no input ripple.

OUTPUT VOLTAGE RANGE The range of output voltage over which the regulator will operate.

REFERENCE VOLTAGE The output of the reference amplifier measured with respect to the negative supply.

RIPPLE REJECTION The ratio of the peak to peak input ripple voltage to the peak to peak output ripple voltage.

SHORT CIRCUIT CURRENT LIMIT The output current of the regulator with the output shorted to the negative supply.

STANDBY CURRENT DRAIN The supply current drawn by the regulator with no output load and no reference voltage load.

TRANSIENT RESPONSE The closed-loop step function response of the regulator under small-signal conditions.

NOTES

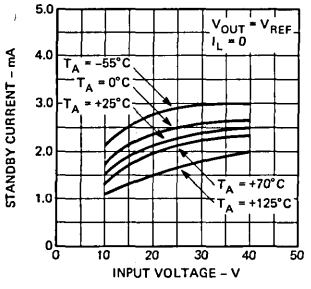
Note 1: Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 25°C and Dual-In-Line Package at 9 mW/°C for operation at ambient temperatures above 50°C.

Note 2: Unless otherwise specified, T_A = 25°C, V_{IN} = V+ = V_C = 12 V, V− = 0 V, V_{out} = 5 V, I_L = 1 mA, R_{SC} = 0, C_l = 100 pF, C_{REF} = 0 and divider impedance as seen by error amplifier ≤ 10 kΩ when connected as shown in Fig. 3 .

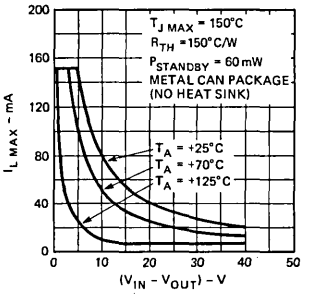
Note 3: The load & line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

PERFORMANCE CURVES

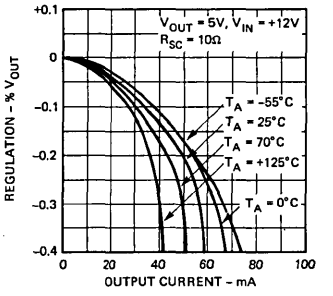
Standby Current Drain As A Function Of Input Voltage



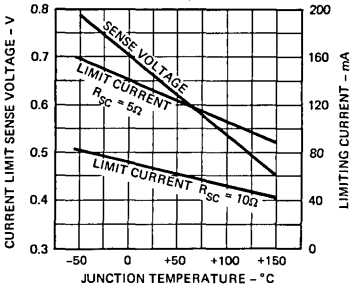
Maximum Load Current As A Function Of Input-Output Voltage Differential



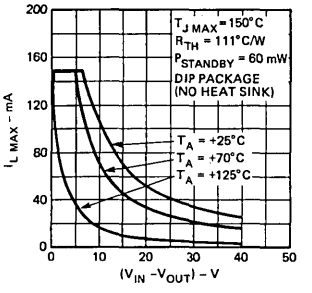
Load Regulation Characteristics With Current Limiting



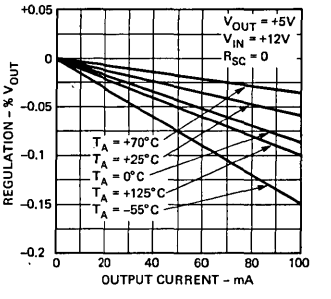
Current Limiting Characteristics As A Function of Junction Temperature



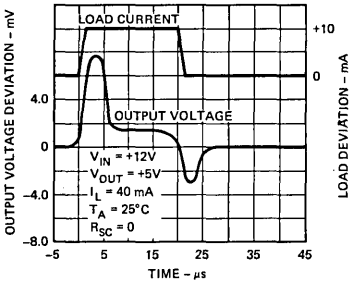
Maximum Load Current As A Function Of Input-Output Voltage Differential



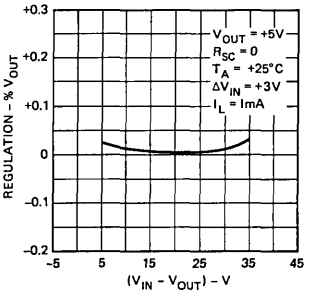
Load Regulation Characteristics Without Current Limiting



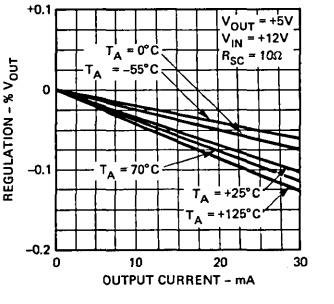
Load Transient Response



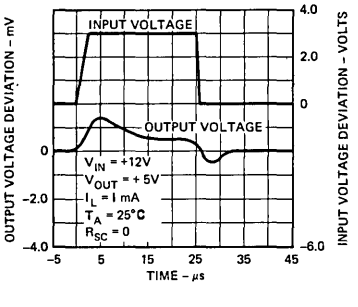
Line Regulation As A Function Of Input-Output Voltage Differential



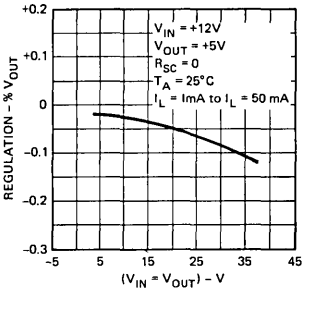
Load Regulation Characteristics With Current Limiting



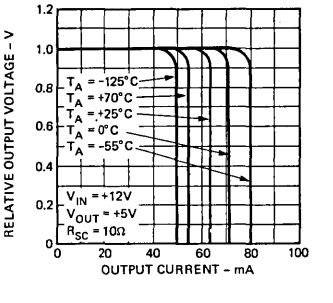
Line Transient Response



Load Regulation As A Function Of Input-Output Voltage Differential

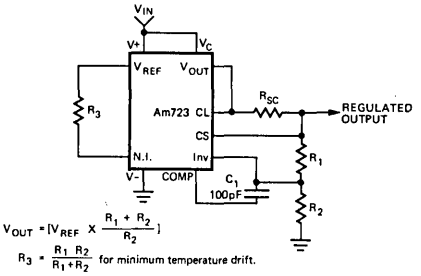


Current Limiting Characteristics



APPLICATIONS

HIGH VOLTAGE REGULATOR
(V_{out} = 7 to 37 Volts)



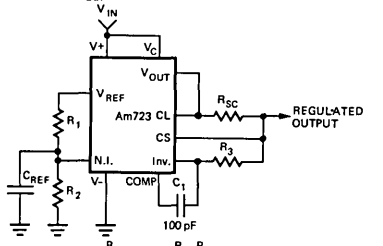
$V_{OUT} = [V_{REF} \times \frac{R_1 + R_2}{R_2}]$

$R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift.

R_3 may be eliminated for minimum component count.

Figure 1

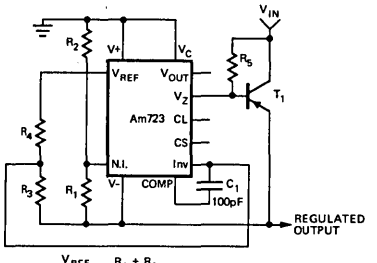
LOW VOLTAGE REGULATOR
(V_{out} = 2 to 7 Volts)



$V_{OUT} = [V_{REF} \times \frac{R_2}{R_1 + R_2}]$; $R_3 = \frac{R_1 R_2}{R_2 + R_2}$ for minimum temperature drift.

Figure 3

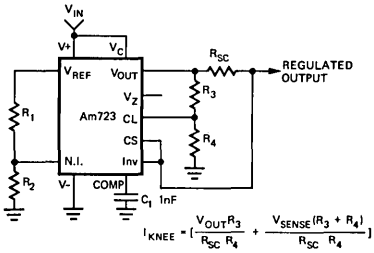
NEGATIVE VOLTAGE REGULATOR



$V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}]$; $R_3 = R_4$

Figure 2

FOLDBACK CURRENT LIMITING REGULATOR



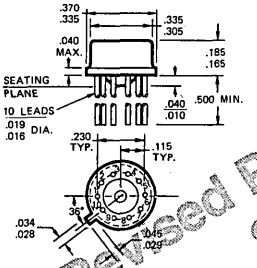
$I_{KNEE} = [\frac{V_{OUT} R_3}{R_{SC} R_4} + \frac{V_{SENSE}(R_3 + R_4)}{R_{SC} R_4}]$

$V_{OUT} = [V_{REF} \times \frac{R_2}{R_1 + R_2}]$; $I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{SC}} \times \frac{R_3 + R_4}{R_4}]$

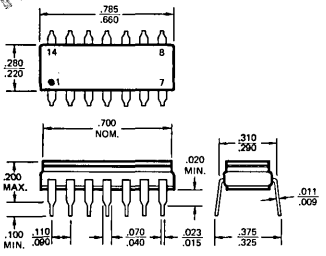
Figure 4

PHYSICAL DIMENSIONS

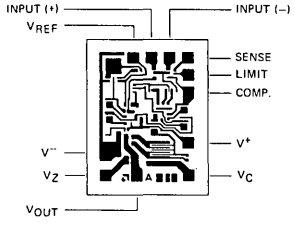
Metal Can



Hermetic Dual-In-Line



Metallization and Pad Layout



51 x 39 Mils

ADVANCED MICRO DEVICES INC.
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Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am725/725A/725B/725C
Instrumentation Operational Amplifiers

Description:

The Am725, Am725A, Am725B and Am725C monolithic operational amplifiers are functionally, electrically and pin-for-pin equivalent to the Fairchild μA725, μA725B and μA725C. They are available in the hermetic metal dual in-line, and flat packages.

Distinctive Characteristics: 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL STD 883.

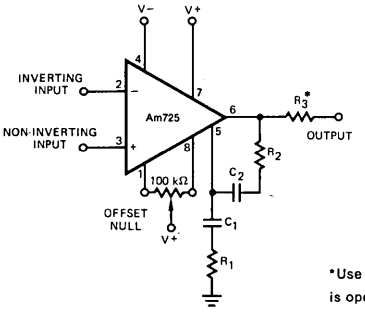
Mixing privileges for obtaining price discounts. Refer to price list.

Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

The Am725/725A/725B/725C are instrumentation operational amplifiers. Device design has been optimized to provide low noise voltage, low offset voltage, low offset voltage drift and high common mode rejection. The Am725 is offset voltage adjustable and is pin-for-pin compatible with the Am108 and Am101A amplifiers. However, additional frequency compensation components are required and should be determined by the desired closed loop gain.

FUNCTIONAL DIAGRAM



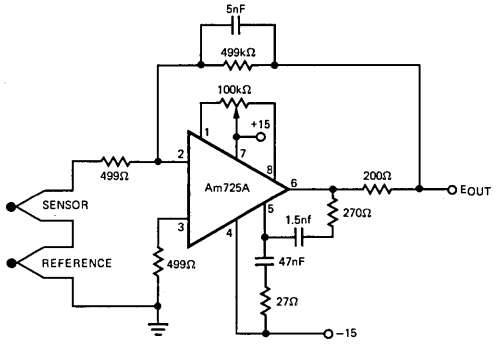
Compensation Component Values

A_{VCL}	R_1 (Ω)	C_1 (nF)	R_2 (Ω)	C_2 (nF)
1000	470	1.0	—	—
100	47	10	—	—
10	27	50	270	1.5
1	10	50	39	20

*Use R_3 = 51Ω when the amplifier is operated with capacitive loads.

APPLICATION

Thermocouple Amplifier



ORDERING INFORMATION

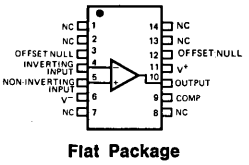
Part Number	Package Type	Temperature Range	Order Number
Am725C	Hermetic DIP	0°C - 70°C	U6A7725393
Am725B	Metal Can	−25°C - 85°C	U5T7725333
Am725	Metal Can	0°C - 70°C	U5T7725393
	Metal Can	−55°C - 125°C	U5T7725312
Am725	Hermetic DIP	−55°C - 125°C	U6A7725312
	Flat Pak	−55°C - 125°C	U3F7725312
Am725A	Metal Can	−55°C - 125°C	AM725A31T
Am725	Dice	Note	UXX7725XXD

Note: The dice supplied will contain units which meet 0°C to +70°C, −25°C to +85°C and −55°C to +125°C temperature ranges.

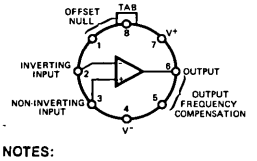
CONNECTION DIAGRAMS

Top Views

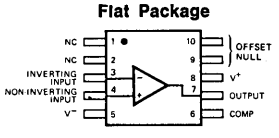
Dual-In-Line



Metal Can



Flat Package



NOTES:

(1) On Metal Can, pin 4 is connected to case.

(2) On DIP, pin 6 is connected to bottom of package.

(3) On Flat Package, pin 5 is connected to bottom of package.

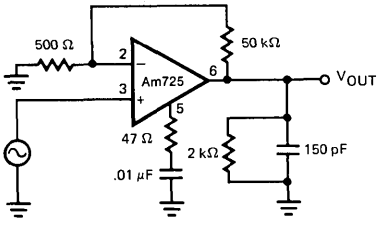
MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±5V
Input Voltage (Note 2)	±22V
Operating Temperature Range	
Am725, Am725A	−55°C to +125°C
Am725B	−25°C to +85°C
Am725C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15V$, $T_A = 25°C$ unless otherwise specified)

		Am725C			Am725B			Am725			Am725A			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	$R_S \leq 10\ k\Omega$		0.5	2.5		0.5	1.5		0.5	1.0				mV
(Without external trim)	$R_S \leq 20\ k\Omega$											0.06	0.1	mV
Input Offset Current			3.0	35		3.0	20		2.0	20		0.3	1.0	nA
Input Bias Current			50	125		50	100		42	100		30	70	nA
Input Noise Voltage	$f_o = 10$ Hz		15			15			15			9.0		nV/√Hz
	$f_o = 100$ Hz		12			12			9.0			8.0		nV/√Hz
	$f_o = 1$ kHz		8.0			8.0			8.0			7.0		nV/√Hz
Input Noise Current	$f_o = 10$ Hz		1.0			1.0			1.0			0.5		pA/√Hz
	$f_o = 100$ Hz		0.8			0.8			0.3			0.25		pA/√Hz
	$f_o = 1$ kHz		0.6			0.6			0.15			0.15		pA/√Hz
Input Resistance			3.0			3.0			1.5		0.8	1.8		MΩ
Input Voltage Range		±13.5	±14		±13.5	±14		±13.5	±14		±13.5	±14.0		V
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$, $V_{OUT} = \pm 10$ V	.25	3.0		.50	3.0		1.0	3.0		1.0	3.0		V/μV
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	96	120		100	120		110	120					dB
	$R_S \leq 20\ k\Omega$										120	126		dB
Power Supply Rejection Ratio	$R_S \leq 10\ k\Omega$		2.0	35		2.0	10		2.0	10				μV/V
	$R_S \leq 20\ k\Omega$											0.5	2.0	μV/V
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±12	±13		±12	±13		±12	±13.5		±12.5	±13.0		V
	$R_L \geq 2\ k\Omega$	±10	±13		±10	±13		±10	±13.5		±12.0	±12.8		V
	$R_L \leq 1\ k\Omega$										±11.0	±12.5		V
Output Resistance			150			150			150			150		Ω
Power Consumption			80	150		80	120		80	105		90	120	mW
The Following Specifications Apply Over The Operating Temperature Ranges														
Input Offset Voltage	$R_S \leq 10\ k\Omega$		0.8	3.5		0.8	2.5			1.5				mV
(Without external trim)	$R_S \leq 20\ k\Omega$											0.08	0.18	mV
Average Temperature Coefficient of Input Offset Voltage (Without external trim)	$R_S = 50\ \Omega$		2.0			2.0	10		2.0	5.0		0.3	0.8	μV/°C
Average Temperature Coefficient of Input Offset Voltage (With external trim)	$R_S = 50\ \Omega$		0.5			0.5			0.6			0.2	0.6	μV/°C
Input Offset Current	$T_{A\ (max)}$		2.0	35		2.0	20		1.2	20		0.25	1.0	nA
	$T_{A\ (min)}$		5.0	50		5.0	40		7.5	40		0.8	4.0	nA
Average Temperature Coefficient of Input Offset Current			10			10	300		35	150		3	20	pA/°C
Input Bias Current	$T_{A\ (max)}$		25	125		25	200		20	100		22	60	nA
	$T_{A\ (min)}$		100	250		100	400		80	200		40	120	nA
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$, $T_{A\ (max)}$	.125			.50			1.0			1.0	3.5		V/μV
	$R_L \geq 2\ k\Omega$, $T_{A\ (min)}$	.125			.25			.25			0.7	2.0		V/μV
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$		115		100			100						dB
	$R_S \leq 20\ k\Omega$										114	124		dB
Power Supply Rejection Ratio	$R_S \leq 10\ k\Omega$		20				20			20				μV/V
	$R_S \leq 20\ k\Omega$											1.0	5.0	μV/V
Output Voltage Swing	$R_L \geq 2\ k\Omega$	±10	±13		±10	±13		±10			±12.0	±12.6		V

Transient Response Test Circuit



DEFINITION OF TERMS

AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET CURRENT The ratio of the change in Input Offset Current over the operating temperature range to the temperature range.

AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET VOLTAGE The ratio of the change in Input Offset Voltage over the operating temperature range to the temperature range.

COMMON MODE REJECTION RATIO The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

DIFFERENTIAL INPUT VOLTAGE RANGE The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

EQUIVALENT INPUT COMMON MODE NOISE VOLTAGE The change in input offset voltage due to common mode input noise.

INPUT BIAS CURRENT The average of the two input currents.

INPUT NOISE CURRENT for $\Delta f = 1$ Hz $\quad \sqrt{\overline{i_n^2}} = \sqrt{\dfrac{\overline{e_{meas}^2} - 4kTR_S - \overline{e_n^2}}{R_S^2}}$

INPUT NOISE VOLTAGE The square root of the mean square narrow-band noise voltage at the output divided by the measurement system gain with low source resistance.

INPUT OFFSET CURRENT The difference in the currents into the two input terminals when the output is at zero.

INPUT OFFSET VOLTAGE That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

INPUT RESISTANCE The resistance looking into either input terminal with the other grounded.

INPUT VOLTAGE RANGE The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

LARGE-SIGNAL VOLTAGE GAIN The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT RESISTANCE The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

OUTPUT VOLTAGE SWING The peak output swing, referred to zero, that can be obtained without clipping.

POWER CONSUMPTION The DC power required to operate the amplifier with the output at zero and with no load current.

POWER SUPPLY REJECTION RATIO The ratio of the change in input offset voltage to the change in power supply voltages producing it.

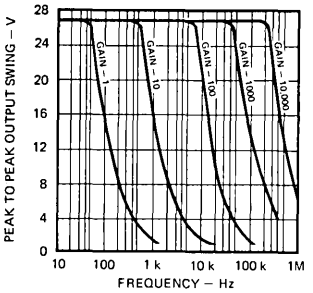
NOTES

Note 1: Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C, the Dual In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C, and the Flat Package at 5.4 mW/°C for operation at ambient temperatures above 57°C.

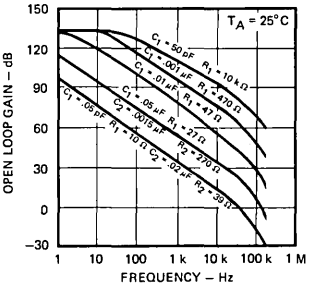
Note 2: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

PERFORMANCE CURVES

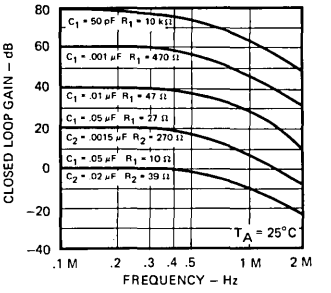
Maximum Undistorted Sinusoidal Output Versus Frequency



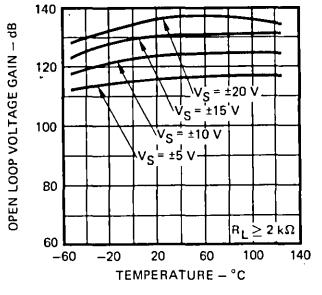
Open Loop Response For Various Values Of Compensation



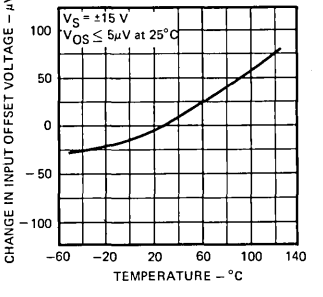
Frequency Response For Various Closed Loop Gains



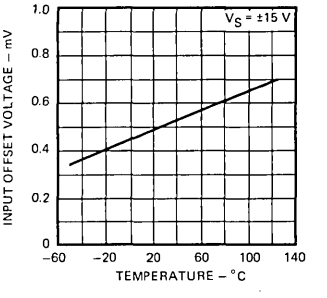
Open Loop Voltage Gain As A Function Of Temperature For Various Supply Voltages



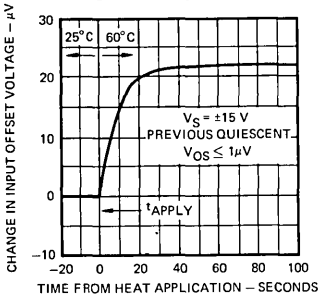
Nulled Input Offset Voltage As A Function Of Temperature



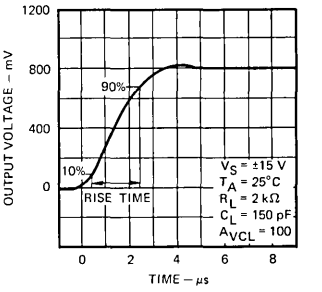
Unnulled Input Offset Voltage As A Function Of Temperature



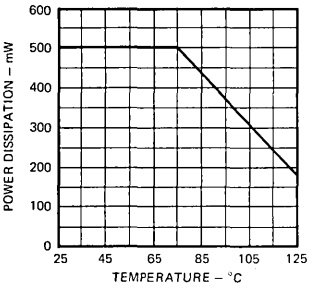
Change In Input Offset Voltage Due To Thermal Shock As A Function Of Time



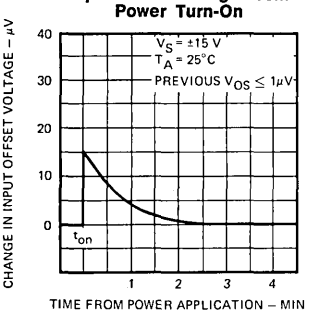
Transient Response



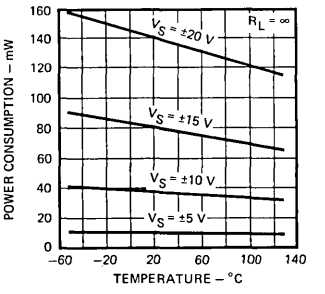
Absolute Maximum Power Dissipation As A Function Of Ambient Temperature



Stabilization Time Of Input Offset Voltage From Power Turn-On

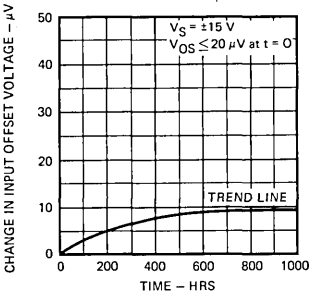


Power Consumption As A Function Of Temperature

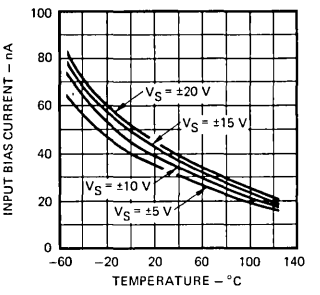


PERFORMANCE CURVES

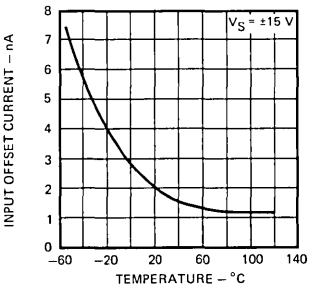
Input Offset Voltage Drift As A Function Of Time



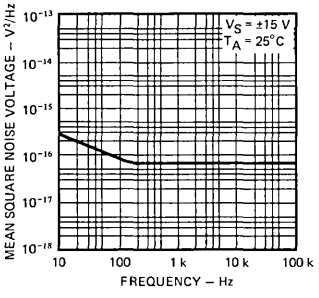
Input Bias Current As A Function Of Temperature



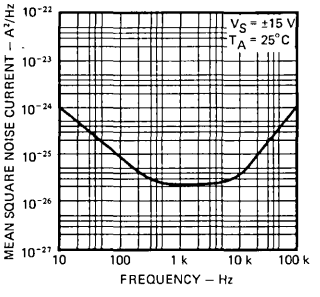
Input Offset Current As A Function Of Temperature



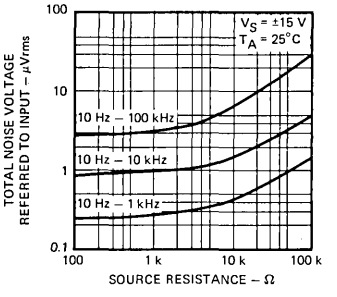
Input Noise Voltage As A Function Of Frequency



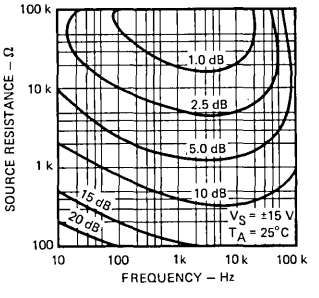
Input Noise Current As A Function Of Frequency



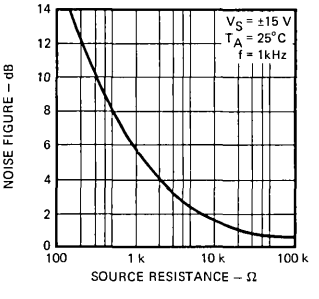
Broadband Noise For Various Bandwidths



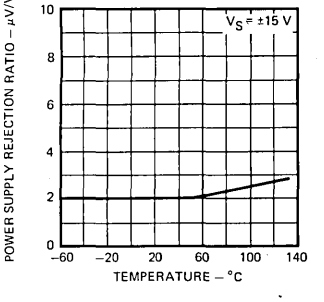
Narrow Band Spot Noise Figure Contours



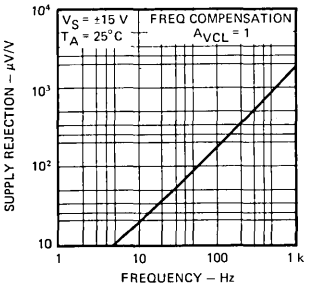
Noise Figure As A Function Of Source Resistance



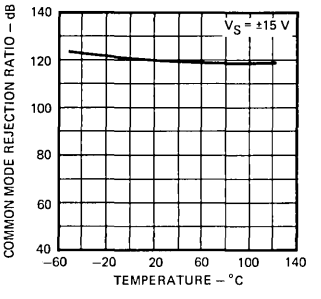
Supply Voltage Rejection Ratio As A Function Of Temperature



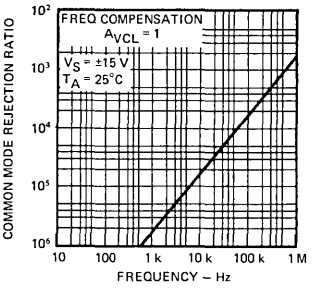
Supply Rejection As A Function Of Frequency



Common Mode Rejection Ratio As A Function Of Temperature

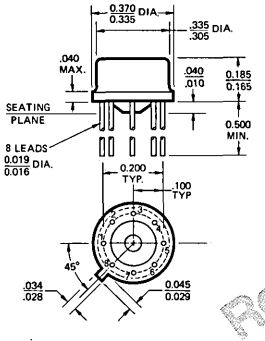


Common Mode Rejection Ratio As A Function Of Frequency

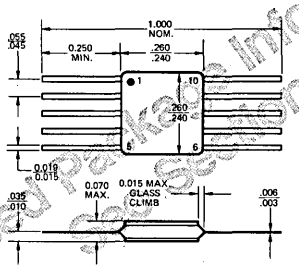


PHYSICAL DIMENSIONS

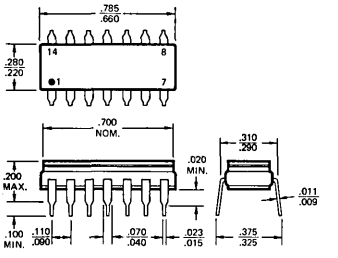
Metal Can



Flat Package

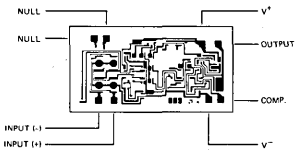


Dual-In-Line



Metallization and Pad Layout

50 x 95 Mils



ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am733/733C
Differential Video Amplifier

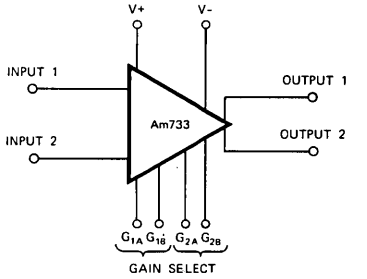
Distinctive Characteristics

- The Am733 and Am733C differential video amplifiers are functionally, electrically and pin-for-pin equivalent to the Fairchild μA733 and 733C.
- Bandwidths: 40 to 120 MHz
- Rise Times: 2.5 to 10 ns
- Propagation Delay: 3.6 to 10 ns
- 100% reliability assurance testing in compliance with MIL STD 883.
- Electrically tested and optically inspected dice for hybrid manufacturers.
- Mixing privilege for obtaining price discounts. Refer to price list.
- Available in metal can, hermetic dual-in-line or hermetic flat packages.

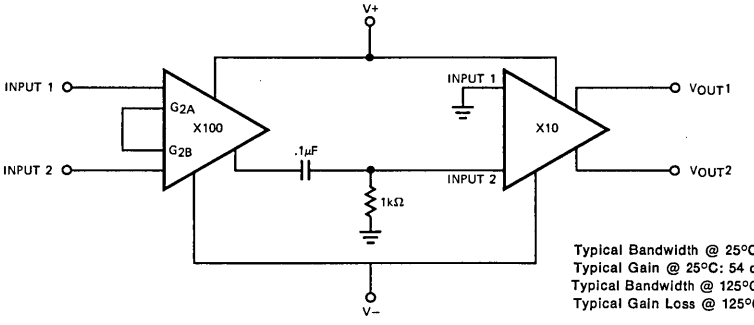
FUNCTIONAL DESCRIPTION

The Am733 is a monolithic two-stage differential input, emitter follower differential output video amplifier. Internal series-shunt feedback is used to obtain fixed gains of 10, 100 or 400, and adjustable gains from 10 to 400 by the use of an external resistor.

FUNCTIONAL DIAGRAM



TYPICAL APPLICATION
HIGH-GAIN WIDEBAND AMPLIFIER



Typical Bandwidth @ 25°C: 65 MHz
Typical Gain @ 25°C: 54 dB
Typical Bandwidth @ 125°C: 57 MHz
Typical Gain Loss @ 125°C: 1 dB

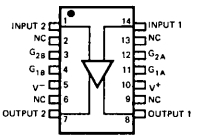
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am733C	Metal Can	0°C - +70°C	U5F7733393
	DIP	0°C - +70°C	U6A7733393
	Flat Pak	0°C - +70°C	U3F7733393
Am733	Metal Can	−55°C - +125°C	U5F7733312
	DIP	−55°C - +125°C	U6A7733312
	Flat Pak	−55°C - +125°C	U3F7733312
Am733	Dice	Note	UXX7733XXD

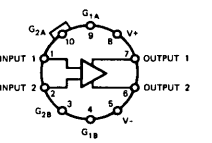
Note: The dice supplied will contain units which meet 0°C to 70°C, and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAMS
Top Views

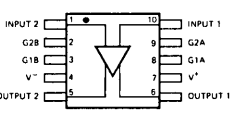
Dual-In-Line



Metal Can



Flat Package



NOTES:
(1) On Metal Can, pin 5 is connected to case.
(2) On DIP, pin 5 is connected to bottom of package.
(3) On Flat Package, pin 4 is connected to bottom of package.

MAXIMUM RATINGS

Supply Voltage	±8 V
Differential Input Voltage	±5 V
Common Mode Input Voltage	±6 V
Output Current	10 mA
Internal Power Dissipation (Note 1)	500 mW
Operating Temperature Range	
Am733C	0°C to +70°C
Am733	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_S = \pm 6.0$ V unless otherwise specified)

Parameter (see definitions)	Conditions	Am733C Min.	Am733C Typ.	Am733C Max.	Am733 Min.	Am733 Typ.	Am733 Max.	Units
Differential Voltage Gain								
Gain 1 (Note 2)		250	400	600	300	400	500	
Gain 2 (Note 3)		80	100	120	90	100	110	
Gain 3 (Note 4)		8.0	10	12	9.0	10	11	
Bandwidth	$R_S = 50\ \Omega$							
Gain 1			40			40		MHz
Gain 2			90			90		MHz
Gain 3			120			120		MHz
Risetime	$R_S = 50\ \Omega$, $V_{out} = 1$ Vpp							
Gain 1			10.5			10.5		ns
Gain 2			4.5	12		4.5	10	ns
Gain 3			2.5			2.5		ns
Propagation Delay	$R_S = 50\ \Omega$, $V_{out} = 1$ Vpp							
Gain 1			7.5			7.5		ns
Gain 2			6.0	10		6.0	10	ns
Gain 3			3.6			3.6		ns
Input Resistance								
Gain 1			4.0			4.0		kΩ
Gain 2		10	30		20	30		kΩ
Gain 3			250			250		kΩ
Input Capacitance	Gain 2		2.0			2.0		pF
Input Offset Current			0.4	5.0		0.4	3.0	μA
Input Bias Current			9.0	30		9.0	20	μA
Input Noise Voltage	$R_S = 50\ \Omega$, BW = 1 kHz to 10 MHz		12			12		μVrms
Input Voltage Range		±1.0			±1.0			V
Common Mode Rejection Ratio								
Gain 2	$V_{cm} = \pm 1$ V, f ≤ 100 kHz	60	86		60	86		dB
Gain 2	$V_{cm} = \pm 1$ V, f = 5 MHz		60			60		dB
Supply Voltage Rejection Ratio								
Gain 2	$\Delta V_S = \pm 0.5$ V	50	70		50	70		dB
Output Offset Voltage								
Gain 1			0.6	1.5		0.6	1.5	V
Gain 2 and Gain 3			0.35	1.5		0.35	1.0	V
Output Common Mode Voltage		2.4	2.9	3.4	2.4	2.9	3.4	V
Output Voltage Swing		3.0	4.0		3.0	4.0		Vpp
Output Sink Current		2.5	3.6		2.5	3.6		mA
Output Resistance			20			20		Ω
Power Supply Current			18	24		18	24	mA
The Following Specifications Apply Over The Operating Temperature Ranges								
Differential Voltage Gain								
Gain 1 (Note 2)		250	400	600	200	400	600	
Gain 2 (Note 3)		80	100	120	80	100	120	
Gain 3 (Note 4)		8.0	10	12	8.0	10	12	
Input Resistance								
Gain 1			4.0			4.0		kΩ
Gain 2		8.0	30		8.0	30		kΩ
Gain 3			250			250		kΩ
Input Offset Current			0.4	6.0		0.4	5.0	μA
Input Bias Current			9.0	40		9.0	40	μA
Input Voltage Range		±1.0			±1.0			V

Parameter (see definitions)	Conditions	Am733C Min.	Am733C Typ.	Am733C Max.	Am733 Min.	Am733 Typ.	Am733 Max.	Units
The Following Specifications Apply Over The Operating Temperature Ranges								
Common Mode Rejection Ratio Gain 2	$V_{cm} = \pm 1$ V, f ≤ 100 kHz	50	86		50	86		dB
Supply Voltage Rejection Ratio Gain 2	$\Delta V_S = \pm 0.5$ V	50	70		50	70		dB
Output Offset Voltage Gain 1			0.6	1.5		0.6	1.5	V
Gain 2 and Gain 3			0.35	1.5		0.35	1.2	V
Output Voltage Swing		2.8	4.0		2.5	4.0		Vpp
Output Sink Current		2.5	3.6		2.2	3.6		mA
Power Supply Current				27			27	mA

DEFINITION OF TERMS

BANDWIDTH The frequency at which the differential gain is 3 dB below its low frequency value.

COMMON MODE REJECTION RATIO The ratio of a change in input common mode voltage to the resulting change in output offset voltage referred to the input.

DIFFERENTIAL VOLTAGE GAIN The ratio of the change in the differential output voltage to the change in voltage between the input terminals producing it.

INPUT BIAS CURRENT The average of the two input currents.

INPUT OFFSET CURRENT The difference between the currents into the two input terminals.

INPUT RESISTANCE The resistance seen looking into either input terminal with the other grounded.

INPUT VOLTAGE RANGE The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

OUTPUT COMMON MODE VOLTAGE The average of the voltages at the two output terminals.

OUTPUT OFFSET VOLTAGE The difference between the voltages at the two output terminals with the inputs grounded.

OUTPUT RESISTANCE The resistance seen looking into either output terminal.

OUTPUT SINK CURRENT The peak negative current available at either output of the amplifier.

OUTPUT VOLTAGE SWING The peak-to-peak output swing that can be obtained without clipping. This includes the unbalance caused by output offset voltage.

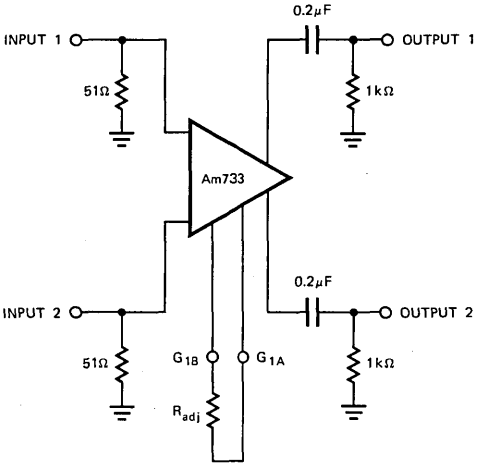
POWER SUPPLY CURRENT The current required from the power supplies to operate the device with no load.

PROPAGATION DELAY The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.

RISE TIME The time required for an output voltage step to change from 10% to 90% of its final value.

SUPPLY VOLTAGE REJECTION RATIO The ratio of a change in supply voltage to the resulting change in output offset voltage referred to the input.

Voltage Gain Adjust Circuit



Note 1: Derate metal can package at 6.8 mW/°C for operation at ambient temperatures above 85°C and Dual In-Line package at 9 mW/°C for operation at ambient temperatures above 100°C, and the Flat Packages at 5.4 mW/°C for operation at ambient temperatures above 65°C

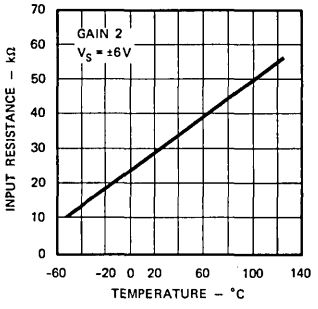
Note 2: Gain Select pins G_{1A} and G_{1B} connected together.

Note 3: Gain Select pins G_{2A} and G_{2B} connected together.

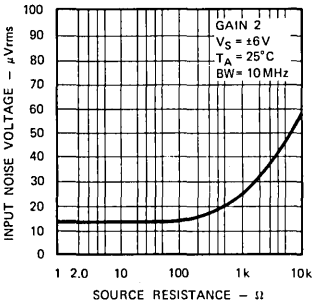
Note 4: All Gain Select pins open.

PERFORMANCE CURVES

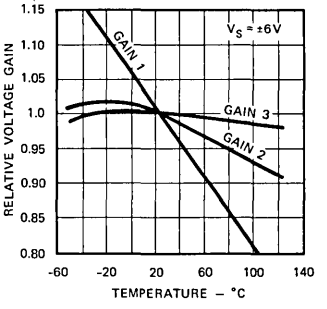
Input Resistance Vs. Temperature



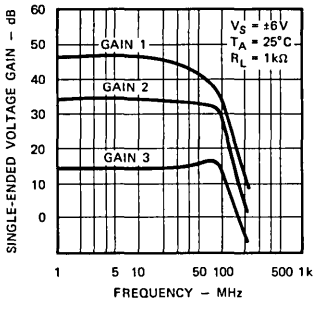
Input Noise Voltage



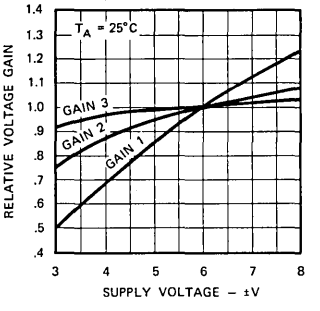
Gain Vs. Temperature



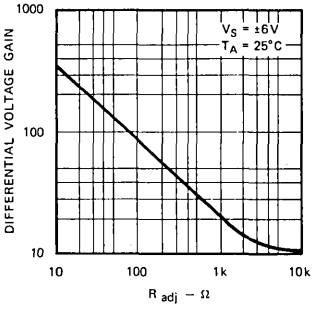
Gain Vs. Frequency



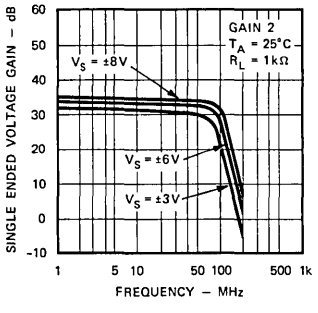
Gain Vs. Supply Voltage



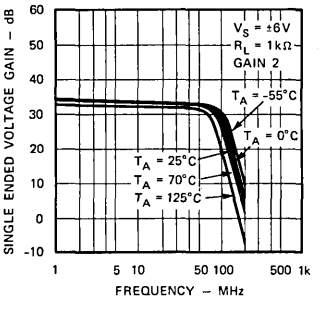
Gain Vs. R_{Adjust}



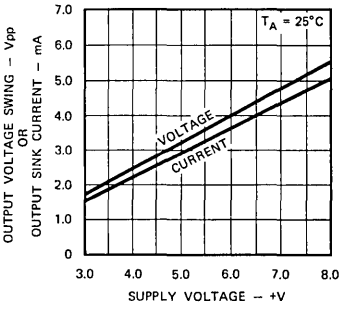
Gain Vs. Frequency and Supply Voltage



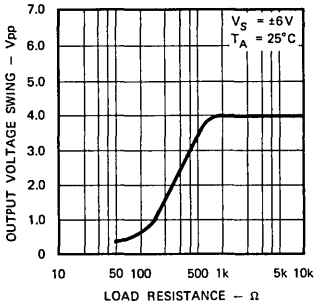
Gain Vs. Frequency and Temperature



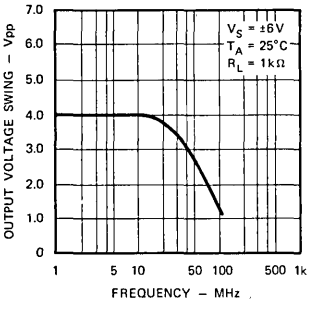
Output Voltage Swing And Sink Current Vs. Supply Voltage



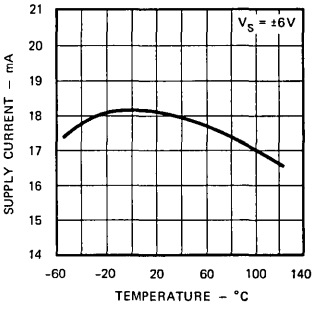
Output Voltage Swing Vs. Load Resistance



Output Voltage Swing Vs. Frequency

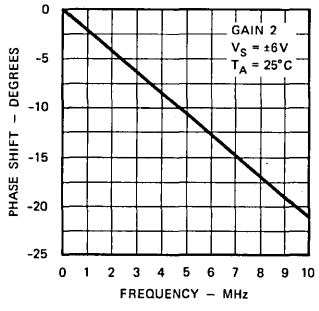


Supply Current Vs. Temperature

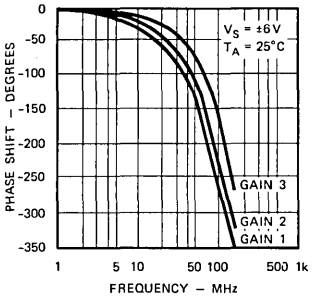


PERFORMANCE CURVES

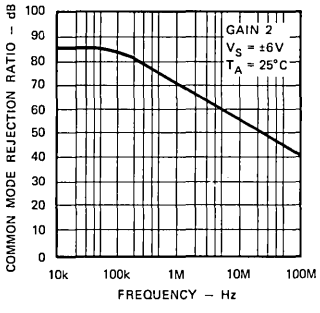
Phase Shift Vs. Frequency



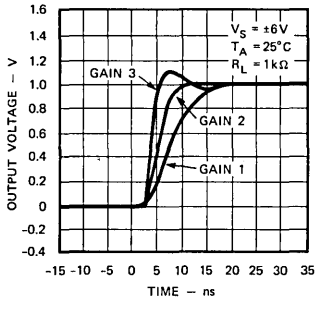
Phase Shift Vs. Frequency



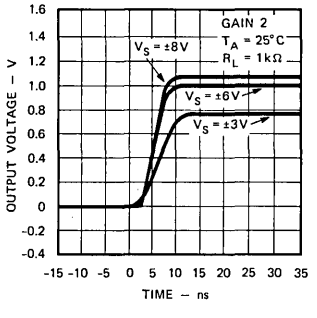
Common Mode Rejection Ratio



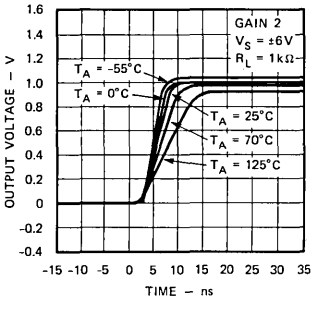
Pulse Response Vs. Gain



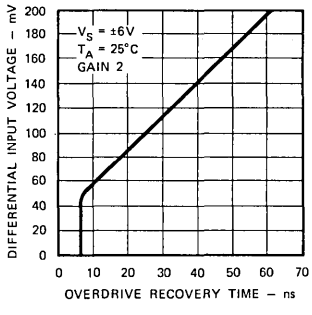
Pulse Response Vs. Supply Voltage



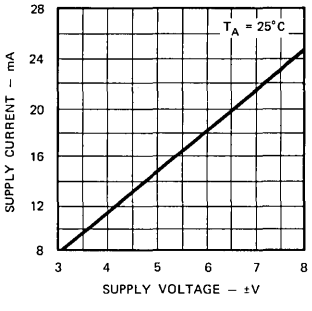
Pulse Response Vs. Temperature



Differential Overdrive Recovery Time

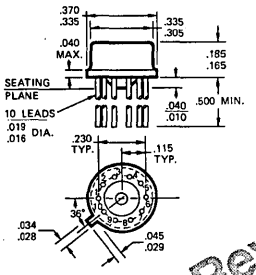


Supply Current Vs. Supply Voltage

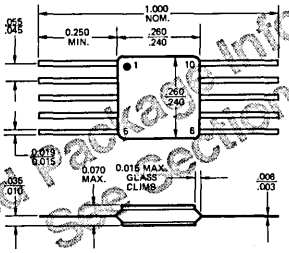


PHYSICAL DIMENSIONS

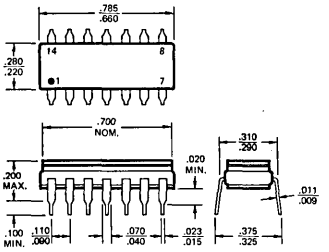
Metal Can



Flat Package

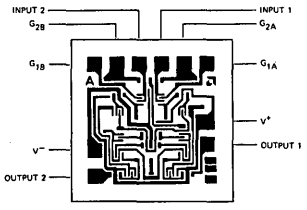


Dual-In-Line



Metallization and Pad Layout

41 x 41 Mils



ADVANCED
MICRO
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California 94086
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TELEX: 34-6306

Am741/741C

Frequency Compensated Operational Amplifier

Description: The Am741 and Am741C Frequency-Compensated Operational Amplifiers are functionally, electrically, and pin-for-pin equivalent to the Fairchild μA741 and μA741C. Both are available in the hermetic metal can, flat package, and dual-in-line packages.

Distinctive Characteristics: 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL STD 883.

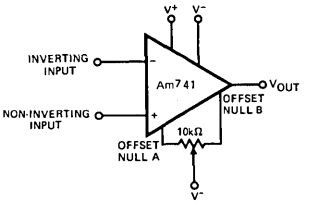
Mixing privileges for obtaining price discounts. Refer to price list.

Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

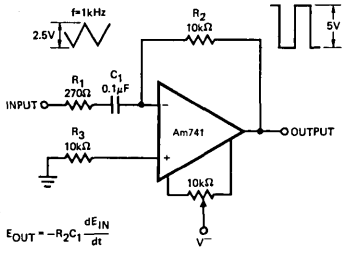
The Am741 and Am741C are differential input, class AB output amplifiers intended for general purpose applications. They are protected against faults at input and output, and require no external components for frequency compensation.

FUNCTIONAL DIAGRAM

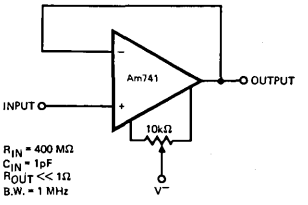


APPLICATIONS

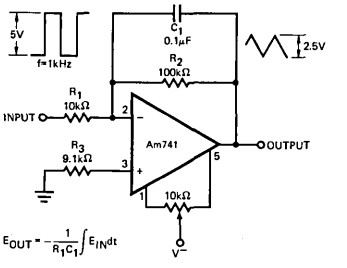
DIFFERENTIATOR



UNITY GAIN VOLTAGE FOLLOWER



INTEGRATOR



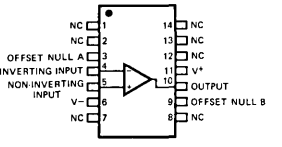
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am741C	Metal Can	0°C - 70°C	U5B7741393
	DIP	0°C - 70°C	U6A7741393
Am741	Metal Can	−55°C - +125°C	U5B7741312
	DIP	−55°C - +125°C	U6A7741312
	Flat Pak	−55°C - +125°C	U3177411312
Am741	Dice	Note	UXX7741XXD

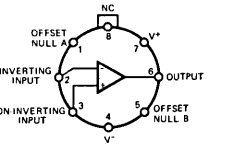
Note: The dice supplied will contain units which meet both 0°C to +70°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAMS
Top Views

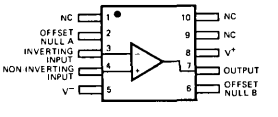
Dual-In-Line



Metal Can



Flat Package



NOTES:

(1) On Metal Can, pin 4 is connected to case.

(2) On DIP, pin 6 is connected to bottom of package.

(3) On Flat Package, pin 5 is connected to bottom of package.

MAXIMUM RATINGS

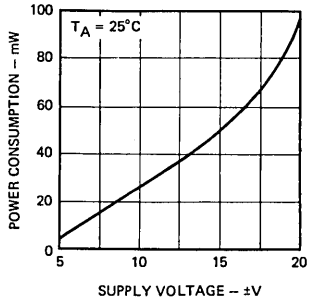
Supply Voltage	
Am741	±22 V
Am741C	±18 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30 V
Voltage between Offset Null and V^-	±0.5 V
Input Voltage (Note 2)	±15 V
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
Am741	−55°C to +125°C
Am741C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

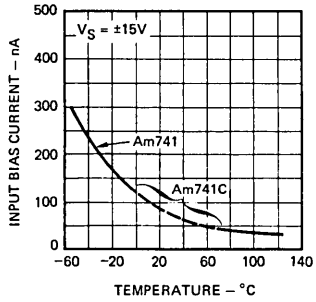
Parameter (see definitions)	Conditions	Am741C Min.	Am741C Typ.	Am741C Max.	Am741 Min.	Am741 Typ.	Am741 Max.	Units
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	6.0		1.0	5.0	mV
Input Offset Current			20	200		20	200	nA
Input Bias Current			80	500		80	500	nA
Input Resistance		0.3	2.0		0.3	2.0		MΩ
Input Capacitance			1.4			1.4		pF
Offset Voltage Adjustment Range			±15			±15		mV
Input Voltage Range		±12	±13		±12	±13		V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	20	200		50	200		V/mV
Output Resistance			75			75		Ω
Output Short-Circuit Current			25			25		mA
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150		30	150	μV/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Current			1.7	2.8		1.7	2.8	mA
Power Consumption			50	85		50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF							
Risetime			0.3			0.3		μs
Overshoot			5.0			5.0		%
Slew Rate	$R_L \geq 2$ kΩ	0.3	0.5		0.3	0.5		V/μs
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 10$ kΩ			7.5			6.0	mV
Input Offset Current	$T_{A(max)}$		9.0	300		7.0	200	nA
	$T_{A(min)}$		35	300		85	500	nA
Input Bias Current	$T_{A(max)}$		0.04	0.8		0.03	0.5	μA
	$T_{A(min)}$		0.13	0.8		0.3	1.5	μA
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	15			25			V/mV
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		±10	±13		V
Supply Current	$T_{A(max)}$		1.6	3.3		1.5	2.5	mA
	$T_{A(min)}$		1.8	3.3		2.0	3.3	mA
Power Consumption	$T_{A(max)}$		48	100		45	75	mW
	$T_{A(min)}$		54	100		60	100	mW

PERFORMANCE CURVES

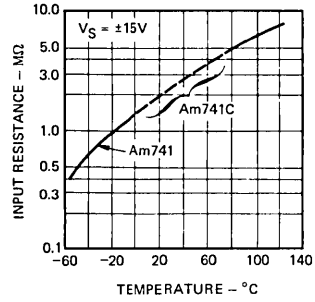
Power Consumption As A Function Of Supply Voltage



Input Bias Current As A Function Of Ambient Temperature



Input Resistance As A Function Of Ambient Temperature



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT The difference in the currents into the two input terminals with the output at zero volts.

INPUT BIAS CURRENT The average of the two input currents.

INPUT RESISTANCE The resistance looking into either input terminal with the other grounded.

INPUT CAPACITANCE The capacitance looking into either input terminal with the other grounded.

LARGE-SIGNAL VOLTAGE GAIN The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT RESISTANCE The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

OUTPUT SHORT-CIRCUIT CURRENT The maximum output current available from the amplifier with the output shorted to ground or to either supply.

SUPPLY CURRENT The DC current from the supplies required to operate the amplifier with the output at zero and with no load current.

POWER CONSUMPTION The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE The closed-loop step-function response of the amplifier under small-signal conditions.

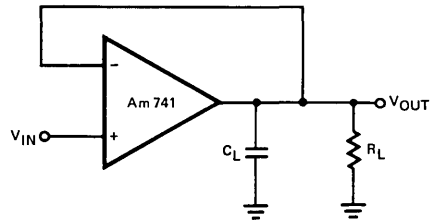
INPUT VOLTAGE RANGE The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

COMMON MODE REJECTION RATIO The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO The ratio of the change in input offset voltage to the change in supply voltage producing it.

OUTPUT VOLTAGE SWING The peak output swing, referred to zero, that can be obtained without clipping.

Slew Rate & Transient Response Test Circuit



$C_L \leq 100$ pF
$R_L = 2$ kΩ

SLEW RATE The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

NOTES

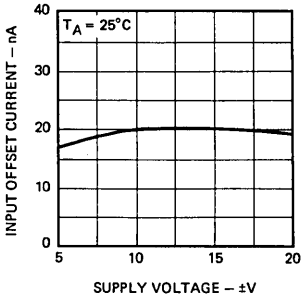
Note 1: Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C, the Dual In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C, and the Flat Package at 5.4 mW/°C for operation at ambient temperatures above 57°C.

Note 2: For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.

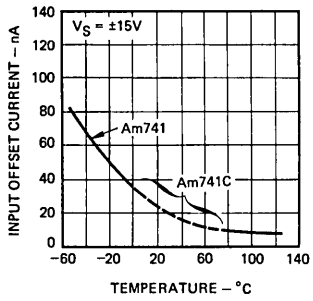
Note 3: Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

PERFORMANCE CURVES

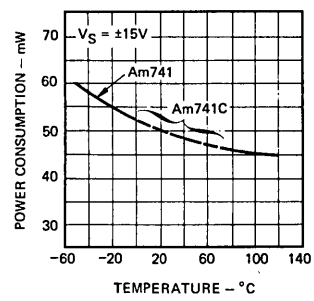
Input Offset Current As A Function Of Supply Voltage



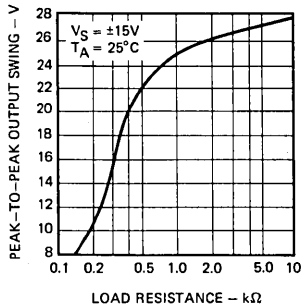
Input Offset Current As A Function Of Ambient Temperature



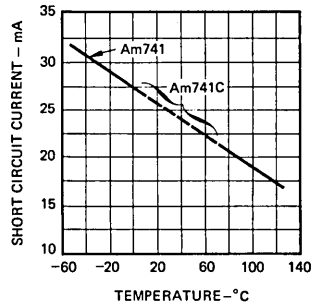
Power Consumption As A Function Of Ambient Temperature



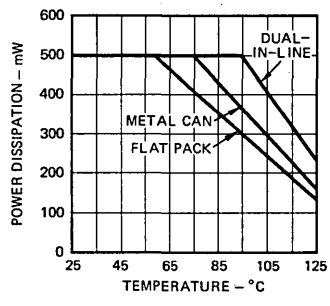
Output Voltage Swing As A Function Of Load Resistance



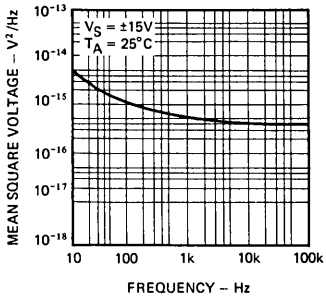
Output Short-Circuit Current As A Function Of Ambient Temperature



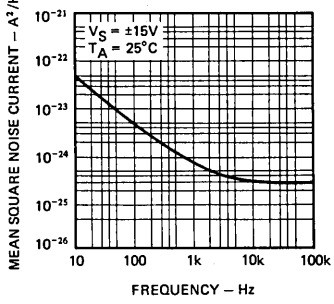
Absolute Maximum Power Dissipation As A Function Of Ambient Temperature



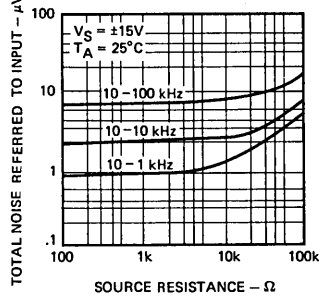
Input Noise Voltage As A Function Of Frequency



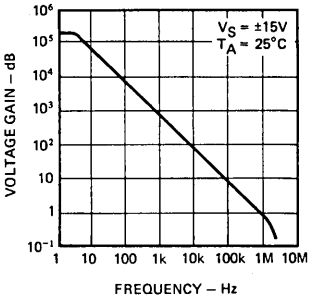
Input Noise Current As A Function Of Frequency



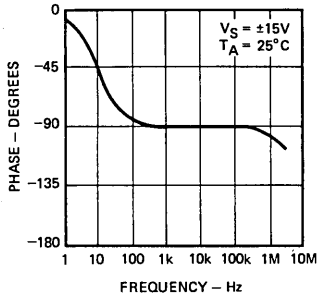
Broadband Noise For Various Bandwidths



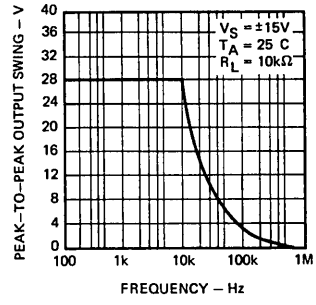
Open Loop Voltage Gain As A Function Of Frequency



Open Loop Phase Response As A Function Of Frequency

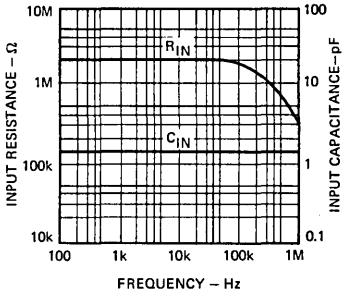


Output Voltage Swing As A Function Of Frequency

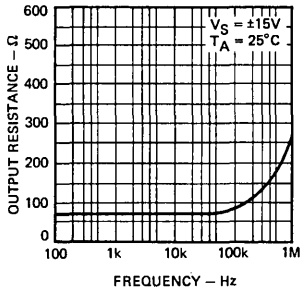


PERFORMANCE CURVES

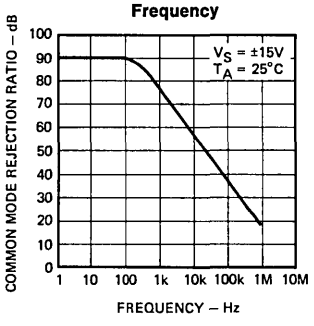
Input Resistance And Input Capacitance As A Function Of Frequency



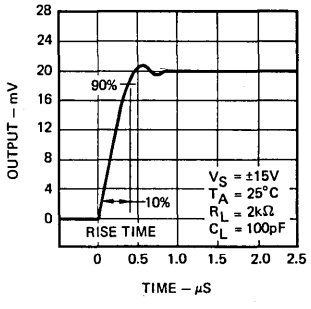
Output Resistance As A Function Of Frequency



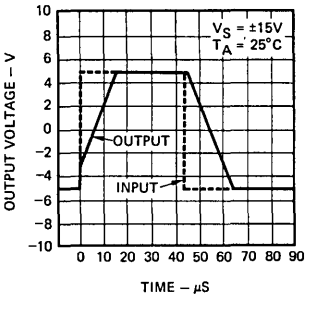
Common Mode Rejection Ratio As A Function Of Frequency



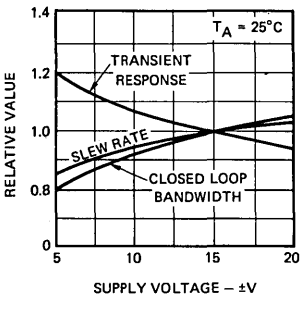
Transient Response



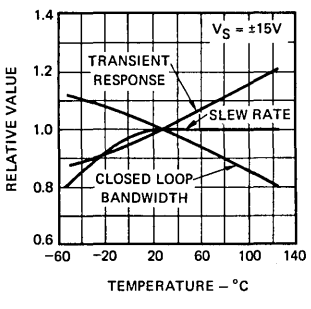
Voltage Follower Large-Signal Pulse Response



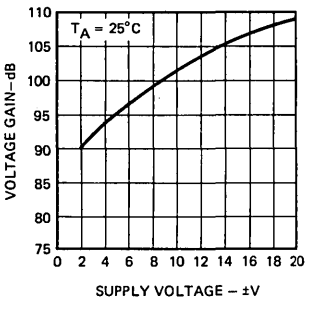
Frequency Characteristics As A Function Of Supply Voltage



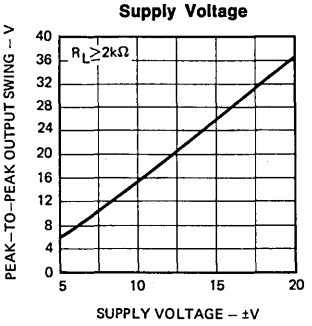
Frequency Characteristics As A Function Of Ambient Temperature



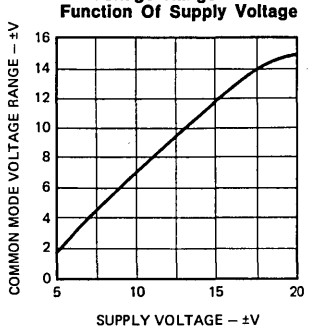
Open Loop Voltage Gain As A Function Of Supply Voltage



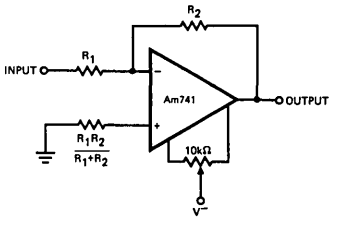
Output Voltage Swing As A Function Of Supply Voltage



Input Common Mode Voltage Range As A Function Of Supply Voltage

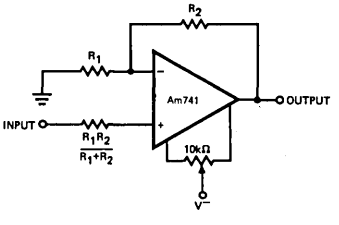


INVERTING AMPLIFIER



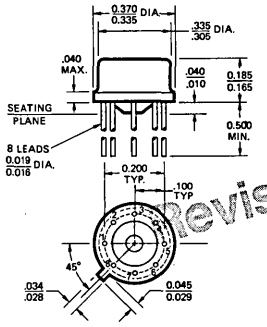
GAIN	R_1	R_2	B.W.	R_{IN}
1	10 kΩ	10 kΩ	1 MHz	10 kΩ
10	1 kΩ	10 kΩ	100 kHz	1 kΩ
100	1 kΩ	100 kΩ	10 kHz	1 kΩ
1000	100 Ω	100 kΩ	1 kHz	100 Ω

NON-INVERTING AMPLIFIER

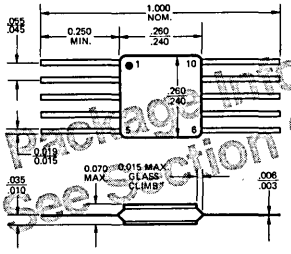


GAIN	R_1	R_2	B.W.	R_{IN}
10	1 kΩ	9 kΩ	100 kHz	400 MΩ
100	100 Ω	9.9 kΩ	10 kHz	280 MΩ
1000	100 Ω	99.9 kΩ	1 kHz	80 MΩ

Metal Can

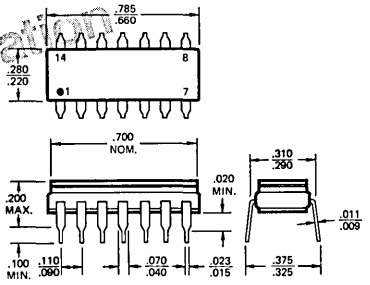


Flat Package



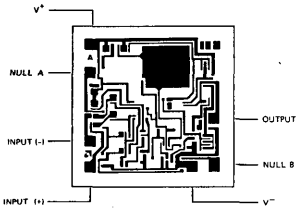
Note: All dimensions are in inches.
Leads are gold plated Kovar.

Dual-In-Line



Metallization and Pad Layout

56 x 56 Mils



ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am747/747C

Dual Frequency Compensated Operational Amplifier

Description: The Am747 and Am747C Dual Frequency-Compensated Operational Amplifiers are functionally, electrically, and pin-for-pin equivalent to the Fairchild μA747 and μA747C. Both are available in the hermetic metal can, dual-in-line and flat packages.

Distinctive Characteristics: 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL STD 883.

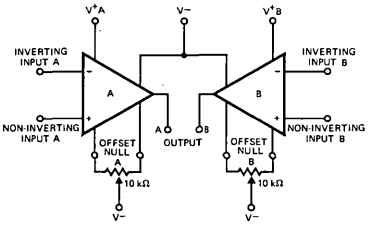
Mixing privileges for obtaining price discounts. Refer to price list.

Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION:

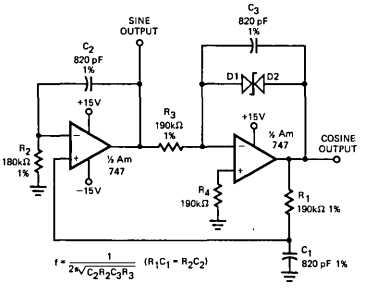
The Am747 is a dual Am741 internally compensated operational amplifier. The Am747 and Am747C are differential input, class AB output amplifiers intended for general purpose applications. They are protected against faults at input and output, and require no external components for frequency compensation.

FUNCTIONAL DIAGRAM



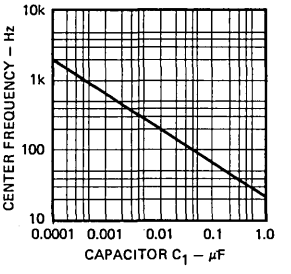
APPLICATIONS

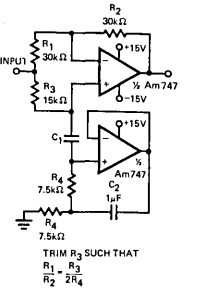
QUADRATURE OSCILLATOR



NOTCH FILTER USING THE Am747 AS A GYRATOR

Notch Frequency As A Function Of C_1





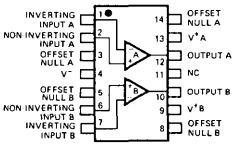
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am747C	DIP	0°C - 70°C	U6W7747393
	Metal Can	0°C - 70°C	U5F7747393
Am747	DIP	−55°C - +125°C	U6W7747312
	Metal Can	−55°C - +125°C	U5F7747312
	Flat Pak	−55°C - +125°C	U317747312
Am747	Dice	Note	UXX7747XXD

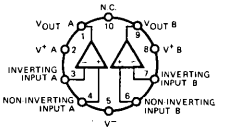
Note: The dice supplied will contain units which meet both 0°C to +70°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAMS
Top View

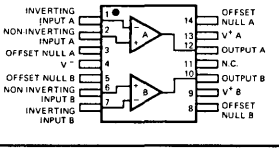
Dual-In-Line



Metal Can



Flat Package



NOTES:

(1) On Metal Can, pin 5 is connected to case.

(2) On DIP, pin 4 is connected to bottom of package.

(3) On Flat Package, pin 4 is connected to bottom of package.

MAXIMUM RATINGS

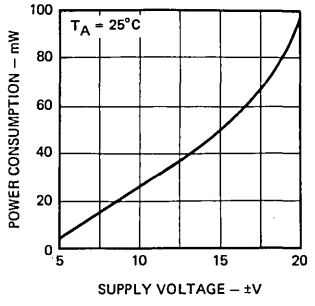
Supply Voltage	
Am747	±22 V
Am747C	±18 V
Internal Power Dissipation (Note 1)	
DIP, Metal Can	800 mW
Flat Package	500 mW
Differential Input Voltage	±30 V
Voltage between Offset Null and V^-	±0.5 V
Input Voltage (Note 2)	±15 V
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
Am747	−55°C to +125°C
Am747C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS—Each Amplifier ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

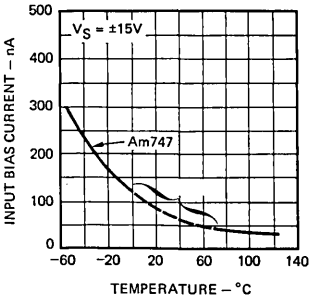
Parameter (see definitions)	Conditions	Am747C Min.	Am747C Typ.	Am747C Max.	Am747 Min.	Am747 Typ.	Am747 Max.	Units
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	6.0		1.0	5.0	mV
Input Offset Current			20	200		20	200	nA
Input Bias Current			80	500		80	500	nA
Input Resistance		0.3	2.0		0.3	2.0		MΩ
Input Capacitance			1.4			1.4		pF
Offset Voltage Adjustment Range			±15			±15		mV
Input Voltage Range		±12	±13		±12	±13		V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	50	200		50	200		V/mV
Output Resistance			75			75		Ω
Output Short-Circuit Current			25			25		mA
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150		30	150	μV/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Current			1.7	2.8		1.7	2.8	mA
Power Consumption			50	85		50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF							
Risetime			0.3			0.3		μs
Overshoot			5.0			5.0		%
Slew Rate	$R_L \geq 2$ kΩ	0.3	0.5		0.3	0.5		V/μs
Channel Separation	$R_S = 50$ Ω, $R_L \geq 10$ kΩ		120			120		dB
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 10$ kΩ			7.5			6.0	mV
Input Offset Current	$T_{A(max)}$		9.0	300		7.0	200	nA
	$T_{A(min)}$		35	300		85	500	nA
Input Bias Current	$T_{A(max)}$		0.04	0.8		0.03	0.5	μA
	$T_{A(min)}$		0.13	0.8		0.3	1.5	μA
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	25			25			V/mV
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		±10	±13		V
Supply Current	$T_{A(max)}$		1.6	3.3		1.5	2.5	mA
	$T_{A(min)}$		1.8	3.3		2.0	3.3	mA
Power Consumption	$T_{A(max)}$		48	100		45	75	mW
	$T_{A(min)}$		54	100		60	100	mW

PERFORMANCE CURVES
(Each Amplifier)

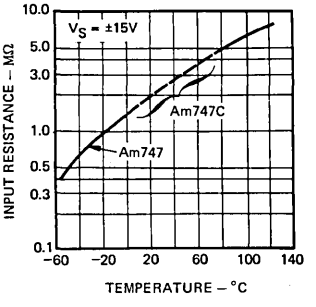
Power Consumption As A Function Of Supply Voltage



Input Bias Current As A Function Of Ambient Temperature



Input Resistance As A Function Of Ambient Temperature



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT The difference in the currents into the two input terminals with the output at zero volts.

INPUT BIAS CURRENT The average of the two input currents.

INPUT RESISTANCE The resistance looking into either input terminal with the other grounded.

INPUT CAPACITANCE The capacitance looking into either input terminal with the other grounded.

LARGE-SIGNAL VOLTAGE GAIN The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT RESISTANCE The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

OUTPUT SHORT-CIRCUIT CURRENT The maximum output current available from the amplifier with the output shorted to ground or to either supply.

SUPPLY CURRENT The DC current from the supplies required to operate the amplifier with the output at zero and with no load current.

POWER CONSUMPTION The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE The closed-loop step-function response of the amplifier under small-signal conditions.

INPUT VOLTAGE RANGE The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

COMMON MODE REJECTION RATIO The ratio of the input voltage range to the maximum change in input offset voltage over this range.

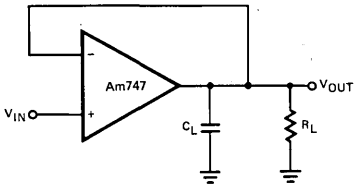
SLEW RATE The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

SUPPLY VOLTAGE REJECTION RATIO The ratio of the change in input offset voltage to the change in supply voltage producing it.

OUTPUT VOLTAGE SWING The peak output swing, referred to zero, that can be obtained without clipping.

CHANNEL SEPARATION The ratio of the output voltage of one amplifier to the input voltage produced in the other amplifier.

Transient Response Test Circuit



$C_L \leq 100$ pF
$R_L = 2$ kΩ

NOTES

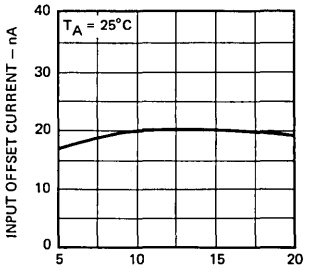
Note 1: Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 30°C, the Dual In-Line package at 9 mW/°C for operation at ambient temperatures above 60°C, and the Flat Package at 5.4 mW/°C for operation at ambient temperatures above 57°C.

Note 2: For supply voltages less than ± 15V, the absolute maximum input voltage is equal to the supply voltage.

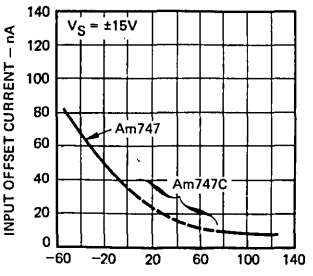
Note 3: Short circuit may be ground or either supply. Rating applies to 125°C case temperature or +60°C ambient temperature for each side.

PERFORMANCE CURVES
(Each Amplifier)

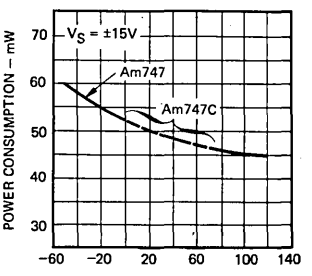
Input Offset Current As A Function Of Supply Voltage



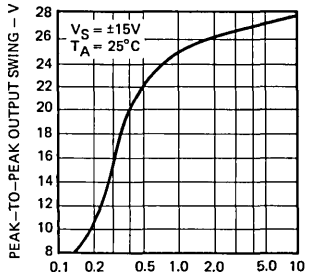
Input Offset Current As A Function Of Ambient Temperature



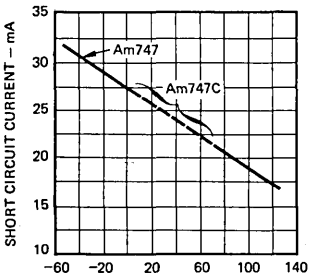
Power Consumption As A Function Of Ambient Temperature



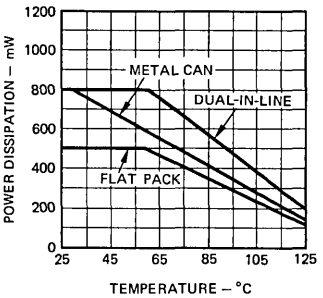
Output Voltage Swing As A Function Of Load Resistance



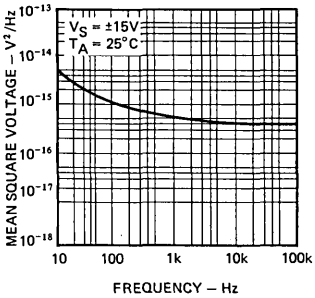
Output Short-Circuit Current As A Function Of Ambient Temperature



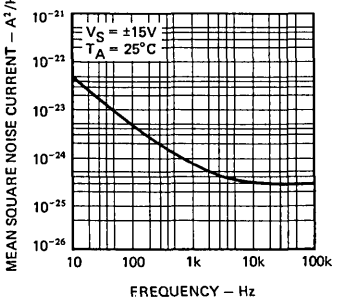
Absolute Maximum Power Dissipation As A Function Of Ambient Temperature



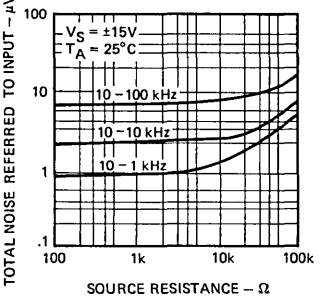
Input Noise Voltage As A Function Of Frequency



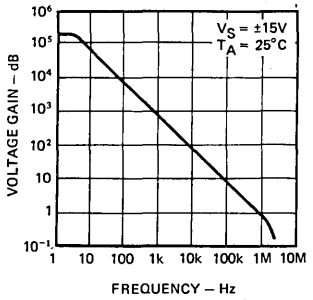
Input Noise Current As A Function Of Frequency



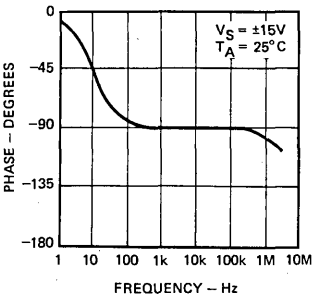
Broadband Noise For Various Bandwidths



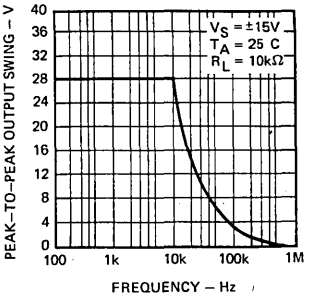
Open Loop Voltage Gain As A Function Of Frequency



Open Loop Phase Response As A Function Of Frequency



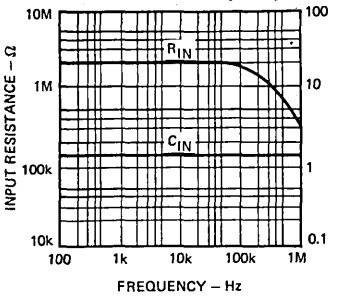
Output Voltage Swing As A Function Of Frequency



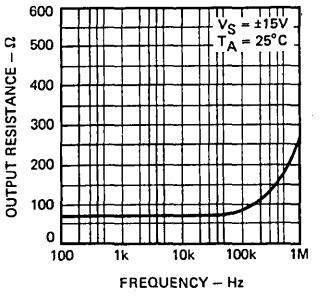
PERFORMANCE CURVES

(Each Amplifier)

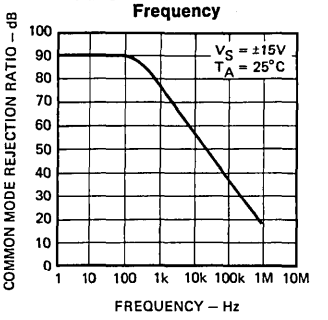
Input Resistance And Input Capacitance As A Function Of Frequency



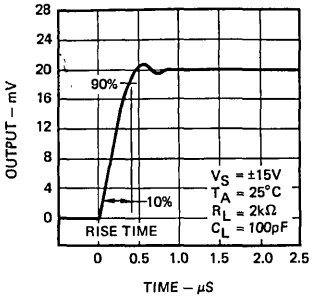
Output Resistance As A Function Of Frequency



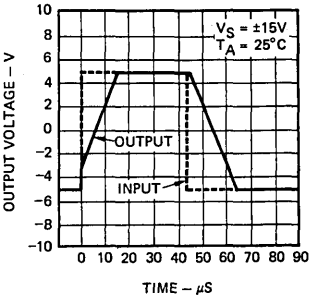
Common Mode Rejection Ratio As A Function Of Frequency



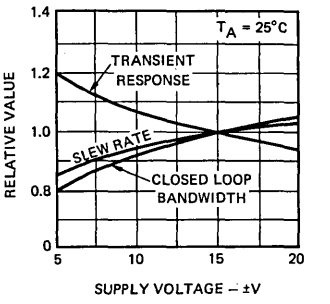
Transient Response



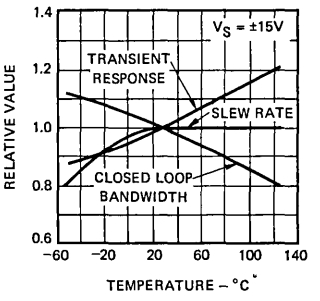
Voltage Follower Large-Signal Pulse Response



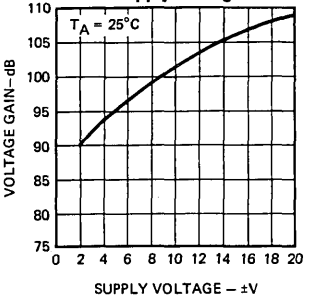
Frequency Characteristics As A Function Of Supply Voltage



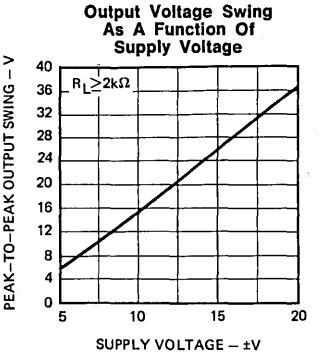
***Frequency Characteristics* As A Function Of Ambient Temperature**



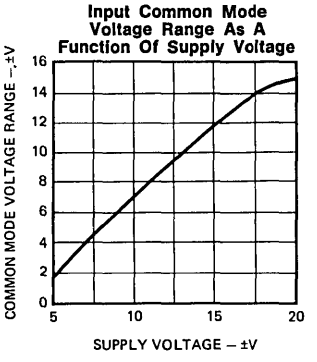
Open Loop Voltage Gain As A Function Of Supply Voltage



Output Voltage Swing As A Function Of Supply Voltage

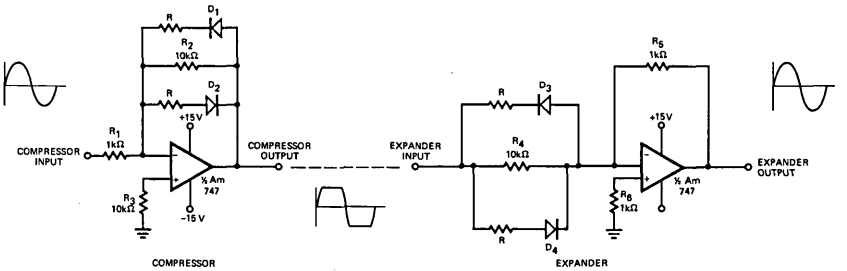


Input Common Mode Voltage Range As A Function Of Supply Voltage



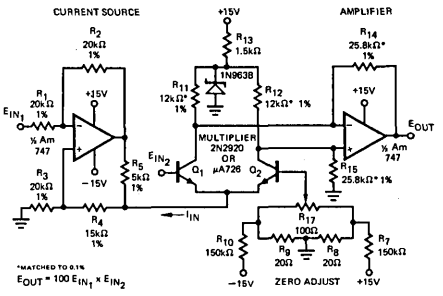
ADDITIONAL APPLICATIONS

COMPRESSOR/EXPANDER AMPLIFIERS

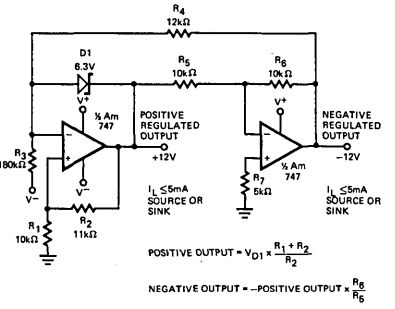


MAXIMUM COMPRESSION/EXPANSION RATIO = R_1/R (10 kΩ > R ≥ 0)
DIODES D_1 THROUGH D_4 ARE MATCHED FD6686 OR EQUIVALENT

ANALOG MULTIPLIER

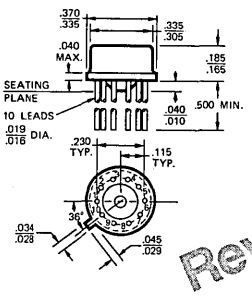


TRACKING POSITIVE AND NEGATIVE VOLTAGE REFERENCES

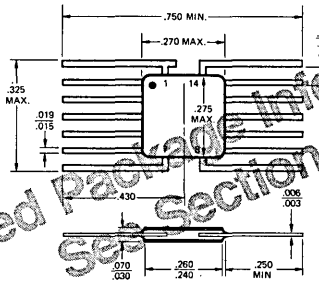


PHYSICAL DIMENSIONS

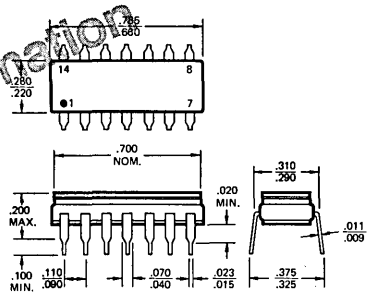
Metal Can



Flat Package



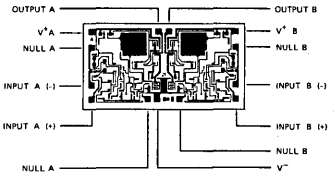
Dual-In-Line



Note: All dimensions are in inches.
Leads are gold plated Kovar.

Metallization and Pad Layout

56 x 106 Mils



ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am748/748C
Operational Amplifier

Description: The Am748/748C Monolithic Operational Amplifiers are functionally, electrically, and pin-for-pin equivalent to the Fairchild μA748 and μA748C. Both are available in the hermetic metal can, dual-in-line, and flat packages.

Distinctive Characteristics: 100% reliability assurance testing including high-temperature bake, temperature cycling, centrifuge and fine leak hermeticity testing in compliance with MIL STD 883 Class B.

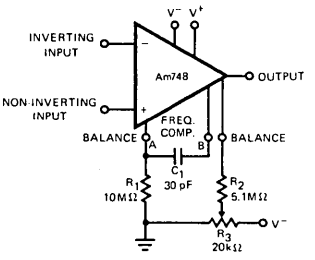
Mixing privileges for obtaining price discounts. Refer to price list.

Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION:

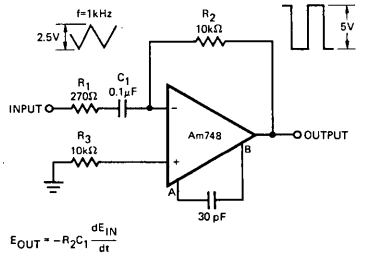
The Am748 and Am748C are differential input class AB output amplifiers intended for general-purpose application. They are protected against faults at input and output, and may be frequency compensated with an external 30 pF capacitor.

FUNCTIONAL DIAGRAM



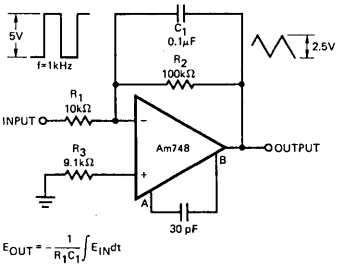
APPLICATIONS

DIFFERENTIATOR



$E_{OUT} = -R_2C_1\frac{dE_{IN}}{dt}$

INTEGRATOR



$E_{OUT} = -\frac{1}{R_1C_1}\int E_{IN}dt$

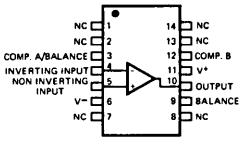
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am748C	DIP	0°C - 70°C	U5B7748393
	Metal Can	0°C - 70°C	U6A7748393
Am748	DIP	−55°C - +125°C	U5B7748312
	Metal Can	−55°C - +125°C	U6A7748312
	Flat Pak	−55°C - +125°C	U3F7748312
Am748	Dice	Note 4	UXX7748XXD

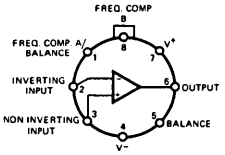
Note 4: The dice supplied will contain units which meet both 0°C to +70°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAMS
Top Views

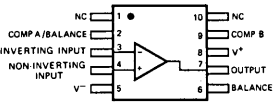
Dual-In-Line



Metal Can



Flat Package



NOTES:

(1) On Metal Can, pin 4 is connected to case.

(2) On DIP, pin 6 is connected to bottom of package.

(3) On Flat Package, pin 5 is connected to bottom of package.

MAXIMUM RATINGS

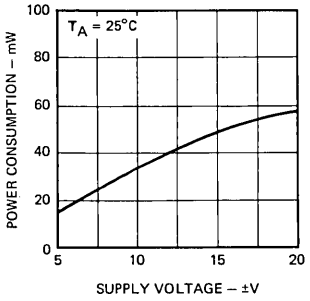
Supply Voltage	
Am748	±22 V
Am748C	±18 V
Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
Am748	−55°C to +125°C
Am748C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

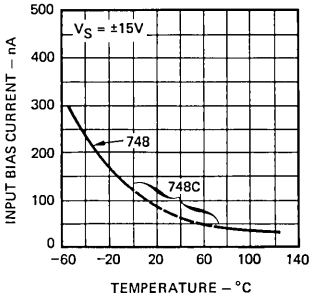
Parameter (see definitions)	Conditions	Am748C Min.	Am748C Typ.	Am748C Max.	Am748 Min.	Am748 Typ.	Am748 Max.	Units
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	6.0		1.0	5.0	mV
Input Offset Current			20	200		20	200	nA
Input Bias Current			80	500		80	500	nA
Input Resistance		0.3	2.0		0.3	2.0		MΩ
Input Capacitance			1.4			1.4		pF
Offset Voltage Adjustment Range			±15			±15		mV
Input Voltage Range		±12	±13		±12	±13		V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	50	200		50	200		V/mV
Output Resistance			75			75		Ω
Output Short-Circuit Current			25			25		mA
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150		30	150	μV/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Current			1.7	2.8		1.7	2.8	mA
Power Consumption			50	85		50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF							
Risetime			0.3			0.3		μs
Overshoot			5.0			5.0		%
Slew Rate	$R_L \geq 2$ kΩ	0.2	0.5		0.2	0.5		V/μs
The Following Specifications Apply Over The Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 10$ kΩ			7.5			6.0	mV
Input Offset Current	$T_{A(max)}$		9.0	300		7.0	200	nA
	$T_{A(min)}$		35	300		85	500	nA
Input Bias Current	$T_{A(max)}$		0.04	0.8		0.03	0.5	μA
	$T_{A(min)}$		0.13	0.8		0.3	1.5	μA
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	25			25			V/mV
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		±10	±13		V
Supply Current	$T_{A(max)}$		1.6	3.3		1.5	2.5	mA
	$T_{A(min)}$		1.8	3.3		2.0	3.3	mA
Power Consumption	$T_{A(max)}$		48	100		45	75	mW
	$T_{A(min)}$		54	100		60	100	mW

PERFORMANCE CURVES

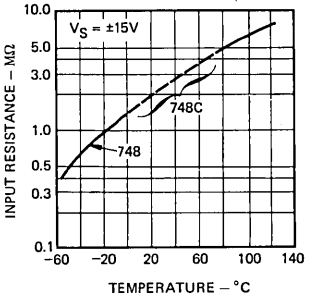
Power Consumption As A Function Of Supply Voltage



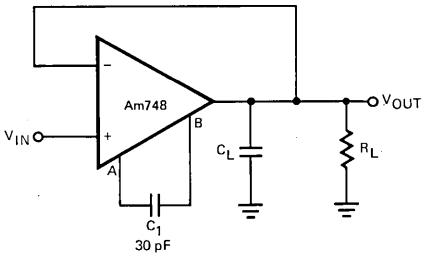
Input Bias Current As A Function Of Ambient Temperature



Input Resistance As A Function Of Ambient Temperature



TRANSIENT RESPONSE TEST CIRCUIT



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT The difference in the currents into the two input terminals with the output at zero volts.

INPUT BIAS CURRENT The average of the two input currents.

INPUT RESISTANCE The resistance looking into either input terminal with the other grounded.

INPUT CAPACITANCE The capacitance looking into either input terminal with the other grounded.

LARGE-SIGNAL VOLTAGE GAIN The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT RESISTANCE The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

OUTPUT SHORT-CIRCUIT CURRENT The maximum output current available from the amplifier with the output shorted to ground or to either supply.

SUPPLY CURRENT The DC current from the supplies required to operate the amplifier with the output at zero and with no load current.

POWER CONSUMPTION The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE The closed-loop step-function response of the amplifier under small-signal conditions.

INPUT VOLTAGE RANGE The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

COMMON MODE REJECTION RATIO The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO The ratio of the change in input offset voltage to the change in supply voltage producing it.

OUTPUT VOLTAGE SWING The peak output swing, referred to zero, that can be obtained without clipping.

NOTES

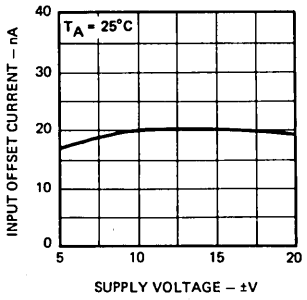
Note 1: Derate Metal Can package 6.8 mW/°C for operation at ambient temperatures above 75°C, the Dual In-Line at 9 mW/°C for operation at ambient temperatures above 95°C, and the Flat Packages at 5.4 mW/°C for operation at ambient temperatures above 57°C.

Note 2: For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.

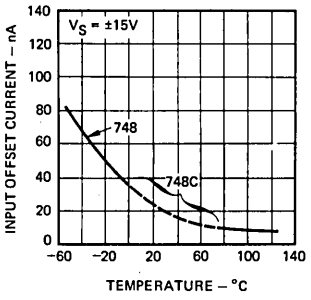
Note 3: Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

PERFORMANCE CURVES

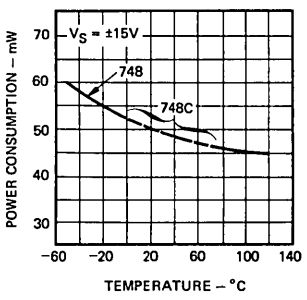
Input Offset Current As A Function Of Supply Voltage



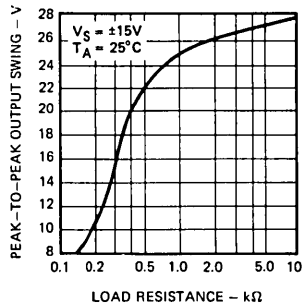
Input Offset Current As A Function Of Ambient Temperature



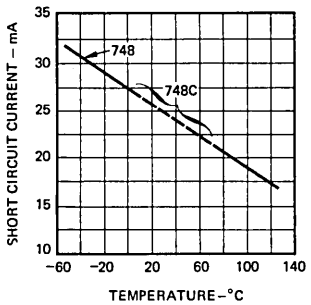
Power Consumption As A Function Of Ambient Temperature



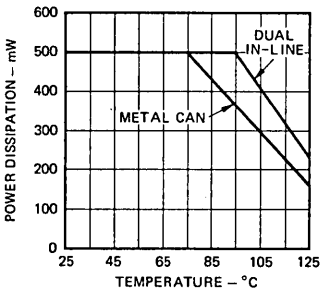
Output Voltage Swing As A Function Of Load Resistance



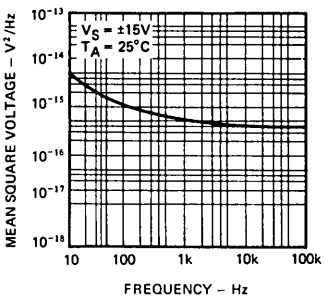
Output Short-Circuit Current As A Function Of Ambient Temperature



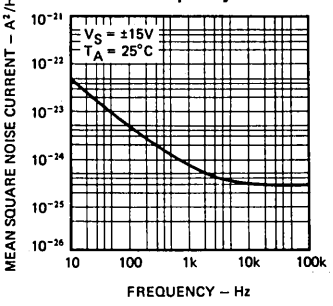
Absolute Maximum Power Dissipation As A Function Of Ambient Temperature



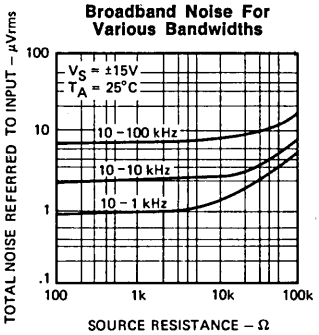
Input Noise Voltage As A Function Of Frequency



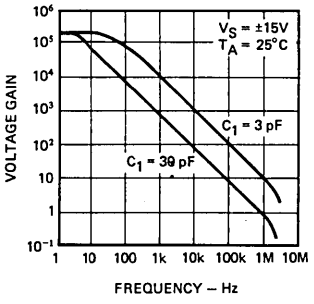
Input Noise Current As A Function Of Frequency



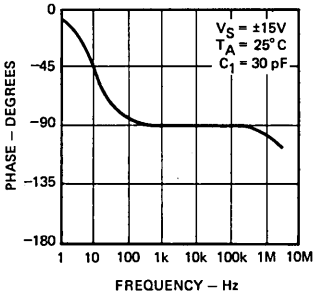
Broadband Noise For Various Bandwidths



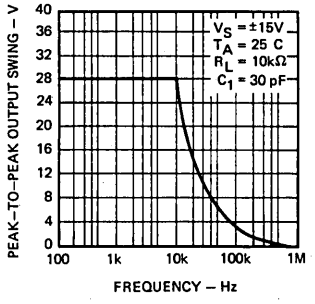
Open Loop Voltage Gain As A Function Of Frequency



Open Loop Phase Response As A Function Of Frequency

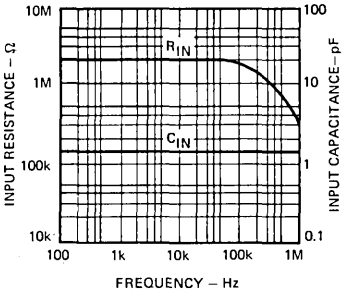


Output Voltage Swing As A Function Of Frequency

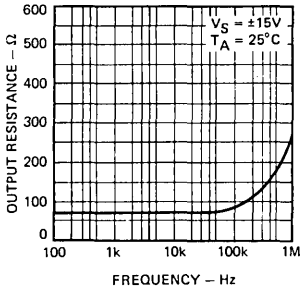


PERFORMANCE CURVES

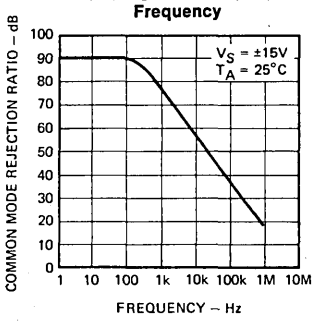
Input Resistance And Input Capacitance As A Function Of Frequency



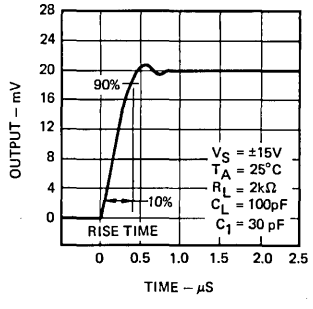
Output Resistance As A Function Of Frequency



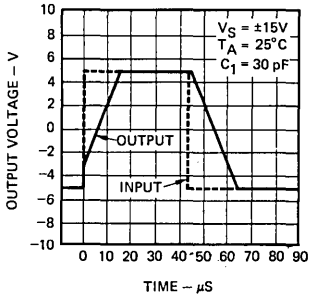
Common Mode Rejection Ratio As A Function Of Frequency



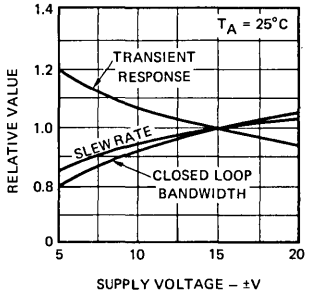
Transient Response



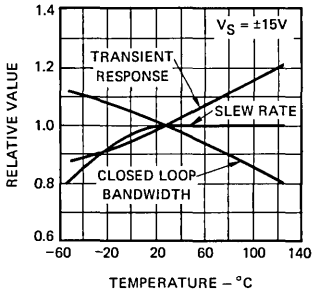
Voltage Follower Large-Signal Pulse Response



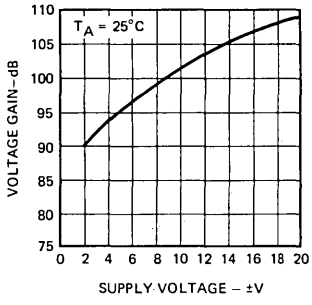
Frequency Characteristics As A Function Of Supply Voltage



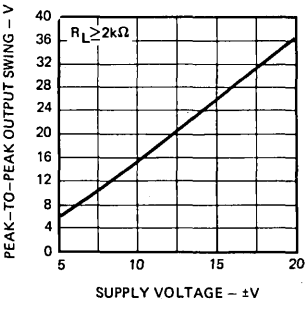
Frequency Characteristics As A Function Of Ambient Temperature



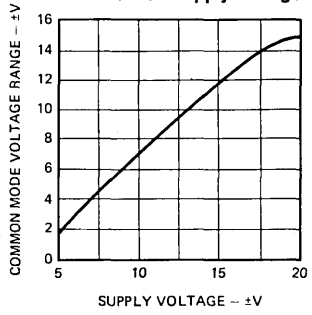
Open Loop Voltage Gain As A Function Of Supply Voltage



Output Voltage Swing As A Function Of Supply Voltage

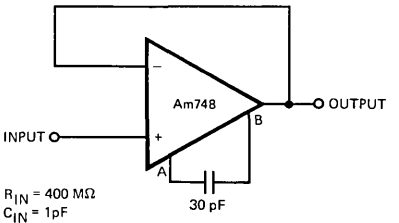


Input Common Mode Voltage Range As A Function Of Supply Voltage



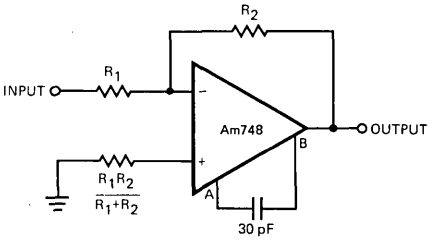
BASIC Am748 AMPLIFIER APPLICATIONS

UNITY GAIN VOLTAGE FOLLOWER



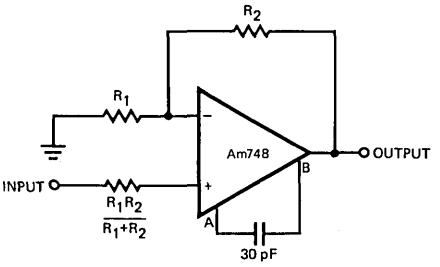
R_{IN} = 400 MΩ
C_{IN} = 1pF
$R_{OUT} << 1Ω$
B.W. = 1 MHz

INVERTING AMPLIFIER



GAIN	R_1	R_2	B.W.	R_{IN}
1	10 kΩ	10 kΩ	1 MHz	10 kΩ
10	1 kΩ	10 kΩ	100 kHz	1 kΩ
100	1 kΩ	100 kΩ	10 kHz	1 kΩ
1000	100 Ω	100 kΩ	1 kHz	100 Ω

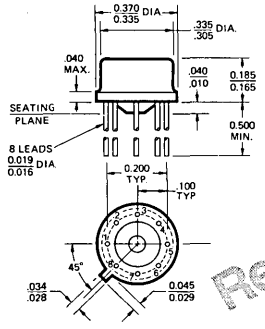
NON-INVERTING AMPLIFIER



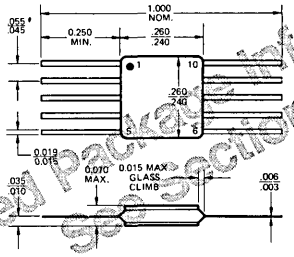
GAIN	R_1	R_2	B.W.	R_{IN}
10	1 kΩ	9 kΩ	100 kHz	400 MΩ
100	100 Ω	9.9 kΩ	10 kHz	280 MΩ
1000	100 Ω	99.9 kΩ	1 kHz	80 MΩ

PHYSICAL DIMENSIONS

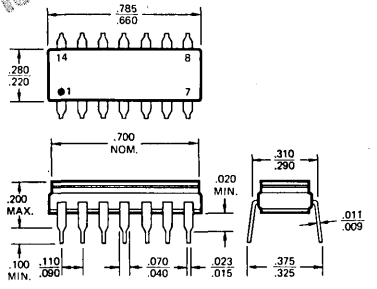
Metal Can



Flat Package



Dual-In-Line



Note: All dimensions are in inches.
Leads are gold plated Kovar.

ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am1500/111/211/311
Precision Voltage Comparator

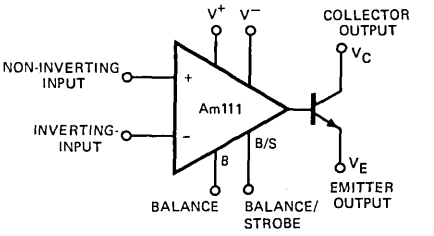
Distinctive Characteristics

- The Am111/211/311 are functionally, electrically, and pin-for-pin equivalent to the National LM 111/211/311.
- The Am1500 is a dual Am111, but requires 20% less power than two Am111 comparators.
- Output Drive — 50 V and 50 mA.
- Input Bias Current — 150 nA max.
- Input Offset Voltage — 4 mV max.
- Differential Input Voltage Range — ±30 V
- 100% reliability assurance testing in compliance with MIL STD 883.
- Electrically tested and optically inspected die for assemblers of hybrid products.
- Mixing privileges for obtaining price discounts. Refer to price list.
- Available in metal can, hermetic dual-in-line or hermetic flat packages.

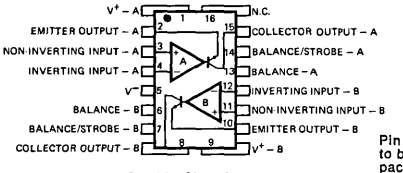
FUNCTIONAL DESCRIPTION

The Am1500/111/211/311 are voltage comparators featuring low input currents, high differential and common mode voltage ranges, wide supply voltage range, and outputs compatible with all bipolar and MOS circuitry. The inputs and outputs can be isolated from system ground, and the output can drive loads referred to ground or either supply. Strobing and offset balancing are available and the outputs can be wire ORed.

FUNCTIONAL DIAGRAM

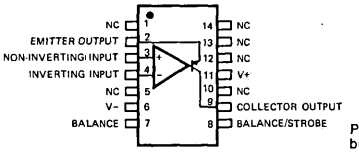


CONNECTION DIAGRAMS
Top Views
Dual-In-Line
Am1500



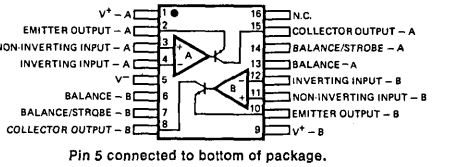
Pin 5 connected to bottom of package

Am111/211/311



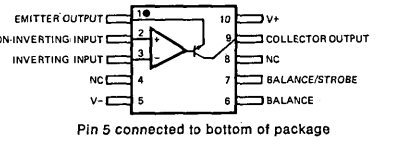
Pin 6 connected to bottom of package

CONNECTION DIAGRAM
Top View
Flat Package
Am1500



Pin 5 connected to bottom of package.

Am111/211/311



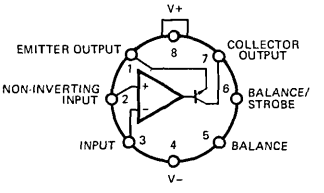
Pin 5 connected to bottom of package

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am311	Metal Can	0°C - 70°C	LM311H
	DIP	0°C - 70°C	LM311D
Am211	Metal Can	−25°C - +85°C	LM211H
	DIP	−25°C - +85°C	LM211D
Am111	Metal Can	−55°C - +125°C	LM111H
	DIP	−55°C - +125°C	LM111D
	Flat Pak	−55°C - +125°C	LM111F
Am1500	DIP	0°C - +70°C	AM150039E
	DIP	−25°C - +85°C	AM150032E
	Flat Pak	−25°C - +85°C	AM150032N
	DIP	−55°C - +125°C	AM150031E
	Flat Pak	−55°C - +125°C	AM150031N
Am111	Dice	Note	LMD11

Note The dice supplied will contain units which meet 0°C to +70°C, −25°C to +85°C and −55°C to +125°C temperature ranges.

CONNECTION DIAGRAM
Top View
Metal Can
Am111/211/311



MAXIMUM RATINGS

Voltage from V^+ to V^-		36 V
Voltage from Collector Output to V^-	Am150031/Am150032/111/211	50 V
	Am150039/311	40 V
Voltage from Emitter Output to V^-		30 V
Voltage between Inputs		±30 V
Voltage from Inputs to V^-		+30 V, −0 V
Voltage from Inputs to V^+		−30 V
Power Dissipation (Note 1)		500 mW
Output Short Circuit Duration		10 sec
Operating Temperature Range	Am150031/111	−55°C to +125°C
	Am150032/211	−25°C to +85°C
	Am150039/311	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (soldering, 10 sec)		300°C

ELECTRICAL CHARACTERISTICS

($T_A = 25°C$ unless otherwise specified) (Note 2)

Parameter (see definitions)	Conditions	Am150039 / Am311 Min	Am150039 / Am311 Typ	Am150039 / Am311 Max	Am111 / Am211 Min	Am111 / Am211 Typ	Am111 / Am211 Max	Am150031 / Am150032 Min	Am150031 / Am150032 Typ	Am150031 / Am150032 Max	Units
Input Offset Voltage (Note 3)			2	7.5		0.7	3.0		0.7	3.0	mV
Input Offset Current (Note 3)			6.0	50.0		4.0	10.0		4.0	10.0	nA
Input Bias Current (Note 3)			100	250		60	100		60	100	nA
Response Time (Note 4)	$R_L = 500\Omega$ to +5 V, $V_E = 0$		150	250		150	250		150	250	ns
Supply Current—Positive (Note 5)			3.9	7.5		3.9	6.0		3.5	4.8	mA
—Negative (Note 5)			2.6	5.0		2.6	4.5		2.4	3.8	mA
Voltage Gain			200			200			200		V/mV
Saturation Voltage	$V_{in} \leq -5$ mV, $I_C = 50$ mA					0.75	1.5		0.75	1.5	V
	$V_{in} \leq -10$ mV, $I_C = 50$ mA		0.75	1.5							V
Output Leakage Current	$V_{in} \geq +5$ mV, V_C to $V_E = 50$ V					0.2	10.0		0.2	10.0	nA
	$V_{in} \geq +10$ mV, V_C to $V_E = 40$ V		0.2	50.0							nA
The Following Specifications Apply Over The Operating Temperature Ranges											
Input Offset Voltage (Note 3)				10.0			4.0			4.0	mV
Input Offset Current (Note 3)				70.0			20.0			20.0	nA
Input Bias Current (Note 3)				300			150			150	nA
Saturation Voltage	$V_{in} \leq -6$ mV, $I_C = 8$ mA					0.23	0.40		0.23	0.40	V
	$V_{in} \leq -10$ mV, $I_C = 8$ mA		0.23	0.40							V
Output Leakage Current	$V_{in} \geq +6$ mV, V_C to $V_E = 50$ V					0.1	0.5		0.1	0.5	μA
Input Voltage Range		±13	±14		±13	±14		±13	±14		V
Supply Current—Positive (Note 5)	$T_A = 125°C$					2.7	4.5		2.4	3.2	mA
—Negative (Note 5)						1.8	3.5		1.6	2.2	mA

DEFINITION OF TERMS

INPUT BIAS CURRENT The average of the two input currents.

INPUT OFFSET CURRENT The difference between the two input currents for which the output will be driven higher than or lower than specified voltages.

INPUT OFFSET VOLTAGE The voltage between the input terminals required to make the output voltage greater or less than specified voltages.

INPUT VOLTAGE RANGE The range of voltages on the input terminals (common mode) for which all specifications apply.

OUTPUT LEAKAGE CURRENT The current into the collector output terminal with a specified output voltage relative to the emitter output terminal and the input drive equal to or greater than a given value.

RESPONSE TIME The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

SATURATION VOLTAGE The low output voltage level with the input drive equal to or greater than a specified value.

SUPPLY CURRENT The current required from the positive or negative supply to operate the comparator with no output load. The power will vary with input voltage, but is specified as a maximum for the entire range of input voltage conditions.

VOLTAGE GAIN The ratio of the change in output voltage to the change in voltage between the input terminals producing it.

NOTES

Note 1: For the Am111/211/311, derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C, the Dual In-Line at 9 mW/°C for operation at ambient temperatures above 95°C, and the Flat Packages at 5.4 mW/°C for operation at ambient temperatures above 57°C. For the Am1500, derate Flat Package at 6.5 mW/°C for operation at ambient temperatures above 83°C, and the Dual In-Line at 9 mW/°C for operation at ambient temperatures above 95°C.

Note 2: Unless otherwise specified, these specifications apply for $V^+ = +15$ V, $V^- = -15$ V, $V_E = -15$ V, and R_L at collector output = 7.5 kΩ to +15 V.

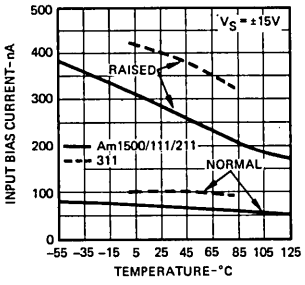
Note 3: The offset voltage, offset current and bias current given are the maximum values required to drive the collector output to within 1 V of the supplies with a 7.5 kΩ load. These parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 4: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

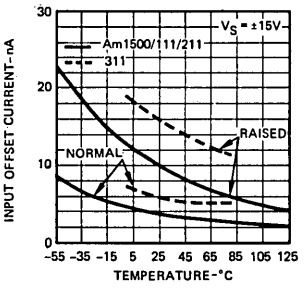
Note 5: The Am1500 supply current specified is the current required by each side.

PERFORMANCE CURVES

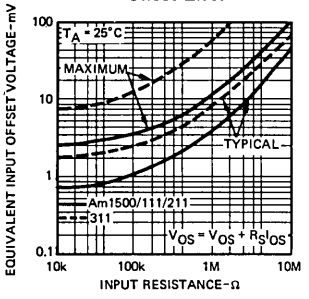
Input Bias Current



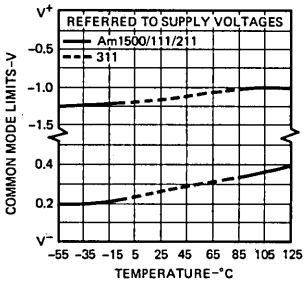
Input Offset Current



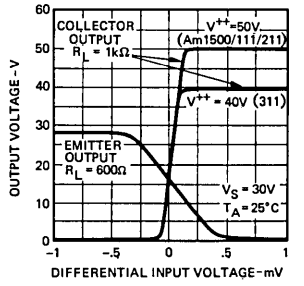
Offset Error



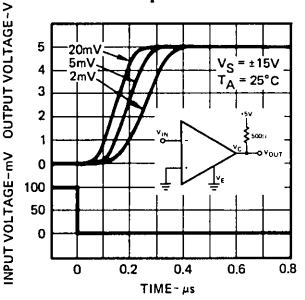
Common Mode Limits



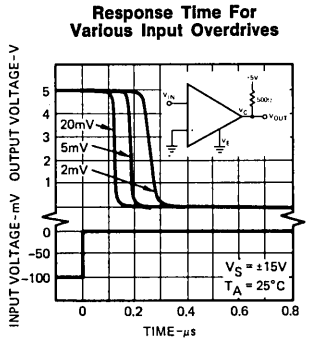
Transfer Function



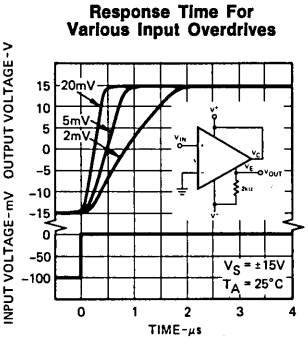
Response Time For Various Input Overdrives



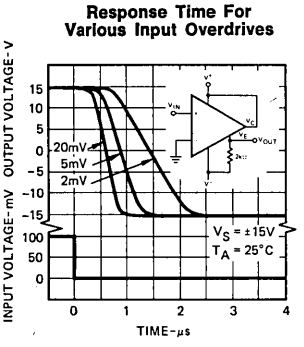
Response Time For Various Input Overdrives



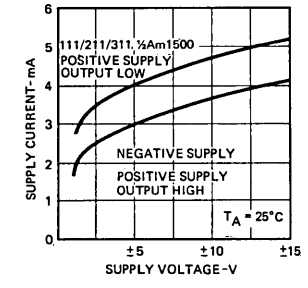
Response Time For Various Input Overdrives



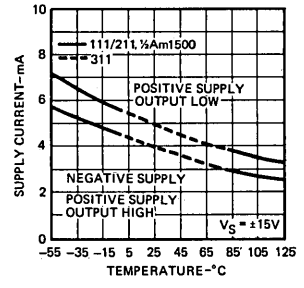
Response Time For Various Input Overdrives



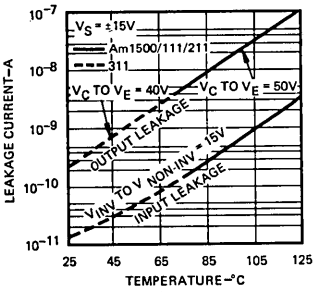
Supply Current



Supply Current

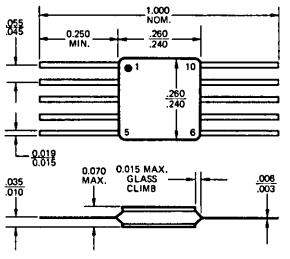


Leakage Current

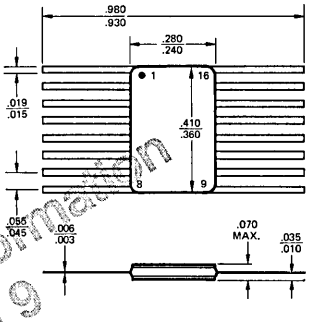


PHYSICAL DIMENSIONS

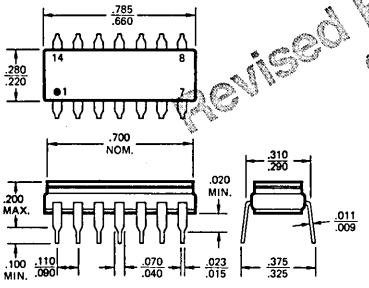
10-Pin Flat Package



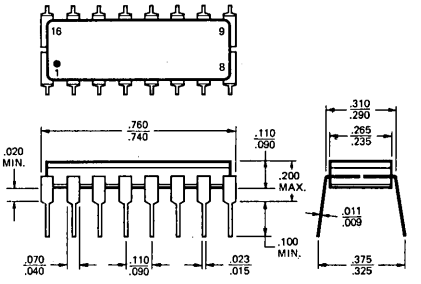
16-Pin Flat Package



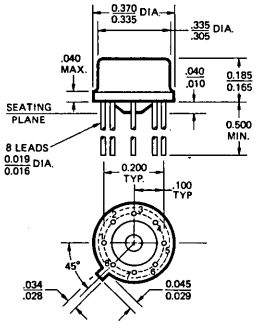
14-Pin Dual-In-Line



16-Pin Dual-In-Line

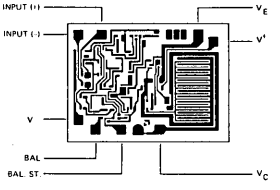


Metal Can



Metallization and Pad Layout

48 x 65 Mils



ADVANCED
MICRO
DEVICES INC.
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California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

Am1660
Operational Amplifier

Distinctive Characteristics

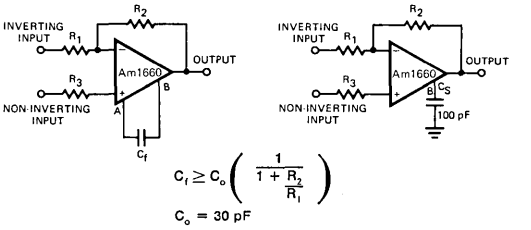
- An Am308 type monolithic operational amplifier electrically specified as a superior replacement for the LM301A, LM307, μA741C and μA748C.
- I_B = 25.0 nA max over temperature
- I_{OS} = 4.0 nA max over temperature
- $\frac{\Delta I_{OS}}{\Delta T}$ = 40 pA/°C max
- Power Dissipation = 30 mW max
- A low-cost functional and pin-for-pin replacement for Am308 and Am308A.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically tested and optically inspected die for the assemblers of hybrid products.
- Mixing privileges for obtaining price discounts. Refer to price list
- Available in metal can and hermetic dual in-line packages.

FUNCTIONAL DESCRIPTION

These differential input, precision amplifiers provide low input current and offset voltage competitive with FET and chopper stabilized amplifiers. They feature low-power consumption over a supply voltage range of ±2V to ±20V. The amplifiers may be frequency compensated with a single external capacitor and are pin-for-pin interchangeable with the Am308, Am301A, & Am 748C.

FUNCTIONAL DIAGRAM

Frequency Compensation Circuits

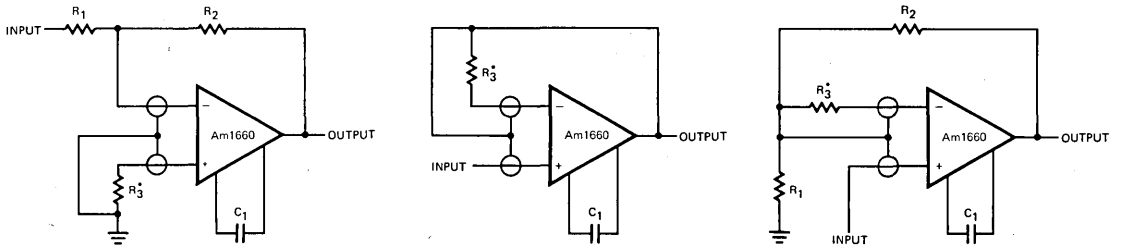


$$C_f \geq C_o\left(\frac{1}{1+\frac{R_2}{R_1}}\right)$$

C_o = 30 pF

APPLICATIONS

Connection of Input Guards



*Use to compensate for large source resistances.

NOTE: $\frac{R_1 R_2}{R_1 + R_2}$ Must be LOW impedance

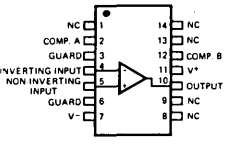
ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Order Number
Am1660	DIP	0°C to +70°C	AM166039F
Am1660	Metal Can	0°C to +70°C	AM166039T

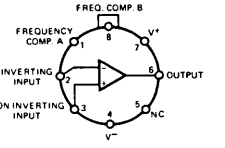
CONNECTION DIAGRAMS

Top Views

Dual-In-Line



Metal Can



NOTES:

(1) On DIP, pin 7 is connected to bottom of package.

(2) On Metal Can, pin 4 is connected to case.

MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15 V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_S = \pm 15$ V unless otherwise specified)

Parameter (see definitions)	**Conditions**	**Min.**	**Typ.**	**Max.**	**Units**
Input Offset Voltage			2.0	7.5	mV
Input Offset Current			0.8	2.0	nA
Input Bias Current			5.0	15	nA
Input Resistance		4.0	12		MΩ
Large-Signal Voltage Gain	$V_{out} = \pm 10$ V, $R_L = 10$ kΩ	25	150		V/mV
Supply Current			250	750	μA
Slew Rate	$A_V = 1$, $C_f = 30$ pF	0.1	0.2		V/μs
The following specifications apply for $0°C \leq T_A \leq 70°C$:					
Input Offset Voltage				10	mV
Average Temperature Coefficient of Input Offset Voltage			10	30	μV/°C
Input Offset Current				4.0	nA
Average Temperature Coefficient of Input Offset Current			10	40	pA/°C
Input Bias Current				25	nA
Input Voltage Range		±13.5			V
Common Mode Rejection Ratio		80	90		dB
Supply Voltage Rejection Ratio		80	90		dB
Output Voltage Swing	$R_L = 10$ kΩ	±13	±14		V
Large-Signal Voltage Gain	$V_{out} = \pm 10$ V, $R_L = 10$ kΩ	15			V/mV
Supply Current	$T_A = +70°C$ $T_A = 0°C$		200 300	750 1000	μA μA

DEFINITION OF TERMS

AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET CURRENT The ratio of the change in Input Offset Current over the operating temperature range to the temperature range.

AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET VOLTAGE The ratio of the change in Input Offset Voltage over the operating temperature range to the temperature range.

COMMON MODE REJECTION RATIO The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

INPUT BIAS CURRENT The average of the two input currents.

INPUT OFFSET CURRENT The difference in the currents into the two input terminals when the output is at zero.

INPUT OFFSET VOLTAGE That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

INPUT RESISTANCE The ratio of the change in input voltage to the change in input current on either input with the other grounded.

INPUT VOLTAGE RANGE The range of voltages on the input terminals for which the offset specifications apply.

LARGE-SIGNAL VOLTAGE GAIN The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT RESISTANCE The resistance seen looking into the output terminal with the output at null.

OUTPUT SHORT-CIRCUIT CURRENT The maximum output current available from the amplifier with the output shorted to ground or to either supply.

OUTPUT VOLTAGE SWING The peak output voltage swing, referred to zero, that can be obtained without clipping.

POWER SUPPLY REJECTION RATIO The ratio of the change in input offset voltage to the change in power supply voltages producing it.

SUPPLY CURRENT The current required from the power supply to operate the amplifier with no load and the output at zero.

SLEW RATE The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

NOTES

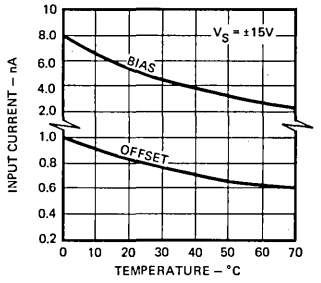
Note 1: Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C and the Dual In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C.

Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1 V is applied between the inputs unless some limiting resistance is used.

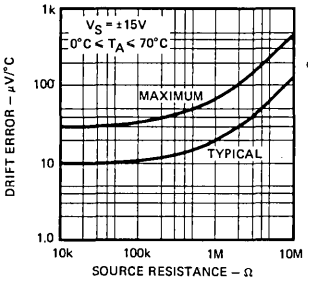
Note 3: For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.

TYPICAL PERFORMANCE CURVES

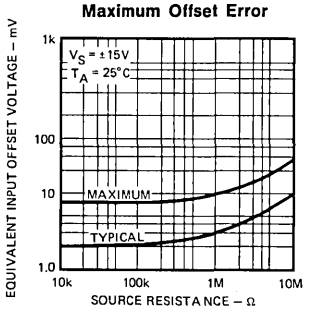
Input Currents



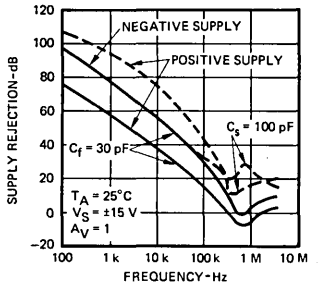
Maximum Drift Error



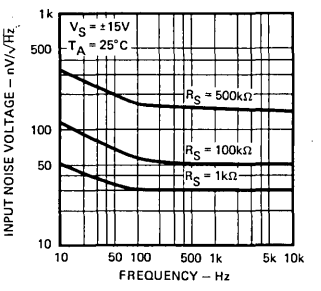
Maximum Offset Error



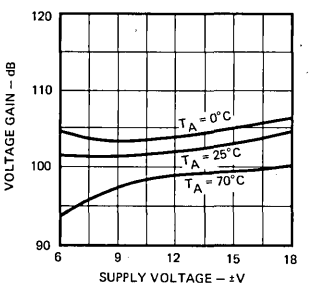
Power Supply Rejection



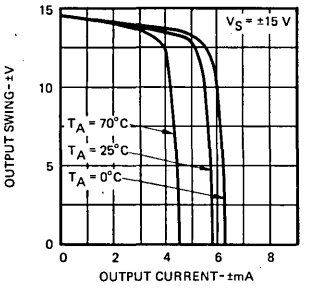
Input Noise Voltage



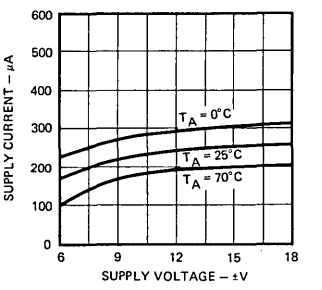
Voltage Gain



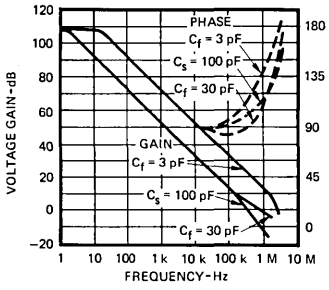
Output Swing



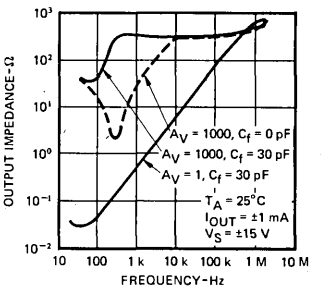
Supply Current



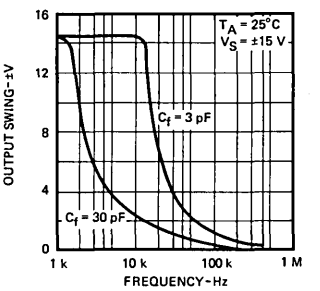
Open Loop Frequency Response



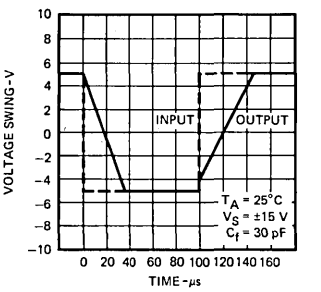
Closed Loop Output Impedance



Large Signal Frequency Response



Voltage Follower Pulse Response



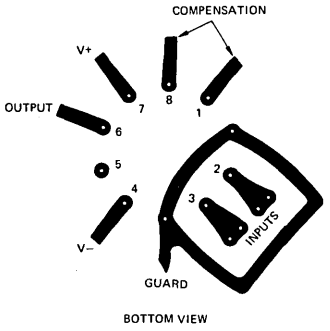
ADDITIONAL APPLICATIONS

GUARDING

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the Am1660 amplifier. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at 70°C, particularly since the inputs pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage at the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard Am748C and Am301A pin configuration.)

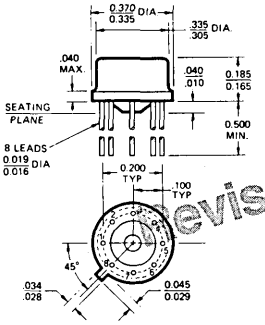


BOTTOM VIEW

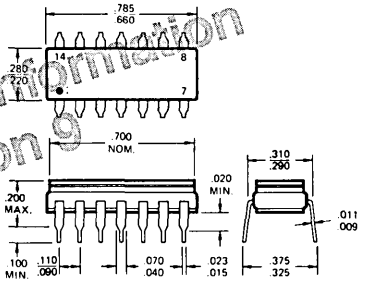
Board layout for Input Guarding with TO-99 package.

PHYSICAL DIMENSIONS

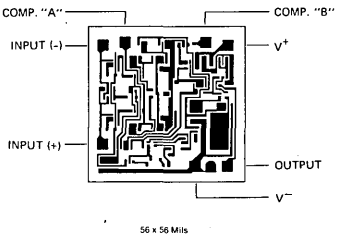
Metal Can



Dual-In-Line



Metallization and Pad Layout



56 x 56 Mils

ADVANCED MICRO DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

SSS725•SSS741•SSS747

High-Performance Operational Amplifiers

Functional Description

The SSS series are high-performance operational amplifiers designed for systems demanding extremely high accuracy. Superior DC and AC characteristics of low input offset voltage, low input offset current, low input bias current and high large signal voltage gain provide performance comparable to discrete or hybrid modules. The SSS series are functionally, electrically and pin-for-pin equivalent to the PMI SSS series.

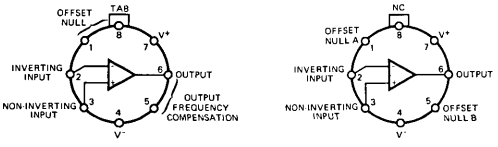
Distinctive Characteristics

- Superior DC and AC characteristics V_{OS}, I_{OS}, A_{VO}, I_B, CMRR, PSRR
- 100% reliability assurance testing in compliance with MIL-STD-883
- Mixing privileges for obtaining price discounts. Refer to price list.

CONNECTION DIAGRAMS

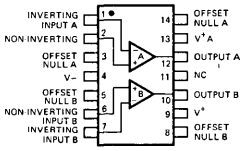
SSS725 **SSS741** **Top View** **SSS747**

Metal Cans

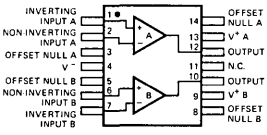


Notes:
(1) All leads through. No pins connected to case on SSS725.
(2) Pin 4 connected to case on SSS741.

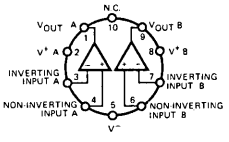
Dual-In-Line



Flat Package



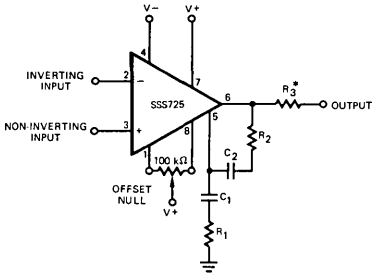
Metal Can



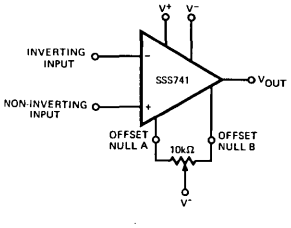
Notes:
(1) On Metal Can, pin 5 is connected to case.
(2) On DIP, pin 4 is connected to bottom of package.
(3) On Flat Package, pin 4 is connected to bottom of package.

FUNCTIONAL DIAGRAMS

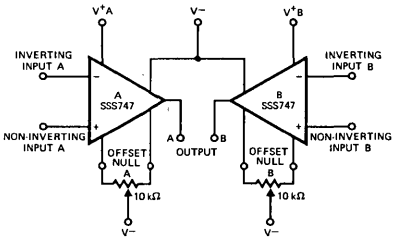
SSS725



SSS741



SSS747



ORDERING INFORMATION

Order Number	Package Type	Temperature Range
SSS725AJ	Metal Can	−55°C - +125°C
SSS725J	Metal Can	−55°C - +125°C
SSS725BJ	Metal Can	−25°C - +85°C
SSS725EJ	Metal Can	0°C - +70°C
SSS741J	Metal Can	−55°C - +125°C
SSS741CJ	Metal Can	0°C - +70°C
SSS747K	Metal Can	−55°C - +125°C
SSS747P	Hermetic DIP	−55°C - +125°C
SSS747M	Flat Pak	−55°C - +125°C
SSS747CK	Metal Can	0°C - +70°C
SSS747CP	Hermetic DIP	0°C - +70°C

SSS725 FREQUENCY

Compensation Component Values

A_{VCL}	R_1 (Ω)	C_1 (nF)	R_2 (Ω)	C_2 (nF)
1000	470	1.0	–	–
100	47	10	–	–
10	27	50	270	1.5
1	10	50	39	20

*Use R_3 = 51 Ω when the amplifier is operated with capacitive loads.

MAXIMUM RATINGS HIGH-PERFORMANCE INSTRUMENTATION OP AMP — SSS725

Supply Voltage	±22V
Internal Power Dissipation (Note 1) Metal Can (TO-99)	500mW
Differential Input Voltage	±5V
Input Voltage (Note 2)	±22V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
SSS725A, SSS725	−55°C to +125°C
SSS725B	−25°C to +85°C
SSS725E,	0°C to +70°C
Lead Temperature (Soldering, 60 sec.)	300°C
Output Short-Circuit Duration	Indefinite

ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_A = 25°C Unless Otherwise Specified)

Symbol	Parameter	Condition	SSS725A Min.	SSS725A Max.	SSS725/725E Min.	SSS725/725E Max.	SSS725B Min.	SSS725B Max.	Units
V_{os}	Input Offset Voltage (Without external trim)	$R_s \leq 20k\Omega$		0.1		0.5		0.75	mV
I_{os}	Input Offset Current			1.0		5.0		5.0	nA
I_B	Input Bias Current			70		80		80	nA
e_n	Input Noise Voltage (Note 3)	f_o = 10Hz f_o = 100Hz f_o = 1kHz		15.0 9.0 7.5		15.0 9.0 7.5		15.0 9.0 7.5	nV/√Hz nV/√Hz nV/√Hz
i_n	Input Noise Current (Note 3)	f_o = 10Hz f_o = 100Hz f_o = 1kHz		1.2 0.6 0.25		1.2 0.6 0.25		1.2 0.6 0.25	pA/√Hz pA/√Hz pA/√Hz
R_{in}	Input Resistance		0.8		0.7		0.7		MΩ
A_{vo}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$ V_o = ±10V	1,000,000		1,000,000		1,000,000		
V_{om}	Maximum Output Voltage Swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±11.0		±12.5 ±12.0 ±11.0		±12.5 ±12.0 ±11.0		V V V
CMVR	Input Voltage Range		±13.5		±13.5		±13.5		V
CMRR	Common Mode Rejection Ratio	$R_s \leq 20k\Omega$	120		120		110		dB
PSRR	Power Supply Rejection Ratio	$R_s \leq 20k\Omega$		2.0		5.0		5.0	μV/V
P_d	Power Consumption			120		120		120	mW
A_{vo}	Large Signal Voltage Gain	$R_L \geq 500\Omega$ V_o = ±0.5V V_s = ±3V	100,000		100,000		100,000		
P_d	Power Consumption	V_s = ±3V		6		6		6	mW

The Following Specifications Apply Over The Operating Temperature Ranges

Symbol	Parameter	Condition	SSS725A Min.	SSS725A Max.	SSS725 Min.	SSS725 Max.	SSS725E Min.	SSS725E Max.	SSS725B Min.	SSS725B Max.	Units
V_{os}	Input Offset Voltage (Without external trim)	$R_s \leq 20k\Omega$		0.18		0.7		0.6		1.0	mV
	Average Input Offset Voltage Drift (Without external trim) (Note 4)	$R_s = 50\Omega$		0.8		2.0		2.0 (Note 3)		2.8 (Note 3)	μV/°C
	Average Input Offset Voltage Drift (With external trim) (Note 4)	$R_s = 50\Omega$		0.6		1.0		0.6		1.0 (Note 3)	μV/°C
I_{os}	Input Offset Current	T_A MAX. T_A MIN.		1.0 4.0		4.0 18.0		5.0 7.0		5.0 14.0	nA nA
	Average Input Offset Current Drift			20		90		40 (Note 3)		90 (Note 3)	pA/°C
I_B	Input Bias Current	T_A MAX. T_A MIN.		60 120		70 180		80 100		80 150	nA nA
CMRR	Common Mode Rejection Ratio	$R_s \leq 20k\Omega$	114		110		115		106		dB
PSRR	Power Supply Rejection Ratio	$R_s \leq 20k\Omega$		5.0		8.0		7.0		8.0	μV/V
A_{vo}	Large Signal Voltage Gain	V_o = ±10V; T_A MAX. $R_L \geq 2k\Omega$; T_A MIN.	1,000,000 700,000		1,000,000 500,000		1,000,000 800,000		1,000,000 500,000		
V_{om}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	±12.0		±12.0		±12.0		±12.0		V

Notes 1. Derate at 6.8mW/°C for operation at ambient temperatures above 75°C.
2. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
3. Parameter is not 100% tested. 90% of all units meet these specifications.
4. Thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent the realization of the performance indicated if both sides of the contacts are not kept at approximately the same temperature. Therefore, the device ambient temperature should not be altered without simultaneously changing the contact temperature.

MAXIMUM RATINGS HIGH-PERFORMANCE FREQUENCY COMPENSATED OP AMP SSS741/741C

Supply Voltage	
SSS741	±22V
SSS741C	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Voltage between Offset Null and V^-	±0.5V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
SSS741	−55°C to +125°C
SSS741C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

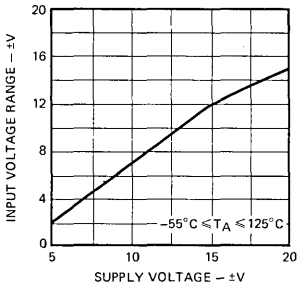
ELECTRICAL CHARACTERISTICS (T_A = 25°C) (Note 4)

Symbol	Parameter	Conditions	SSS741 Min.	SSS741 Max.	SSS741C Min.	SSS741C Max.	Units
V_{os}	Input Offset Voltage	$R_s \leq 50k\Omega$		2.0		5.0	mV
I_{os}	Input Offset Current			5.0		20	nA
I_B	Input Bias Current			50		100	nA
R_{in}	Input Resistance		2.0		1.0		MΩ
A_{vo}	Large-Signal Voltage Gain	$V_s = \pm15V$, $R_L \geq 2k\Omega$ $V_{out} = \pm10V$	100		50		V/mV
V_{om}	Output Voltage Swing	$V_s = \pm15V$, $R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12 ±10		±12 ±10		V V
CMVR	Input Voltage Range	$V_s = \pm15V$ $V_s = \pm20V$	±12 ±15		±12		V
CMRR	Common Mode Rejection Ratio	$R_s \leq 50k\Omega$	80		70		dB
PSRR	Power Supply Rejection Ratio	$R_s \leq 50k\Omega$		100		150	μV/V
P_d	Power Consumption	$V_s \leq \pm15V$		85		85	mW
The Following Specifications Apply Over the Operating Temperature Range							
V_{os}	Input Offset Voltage	$R_s \leq 50k\Omega$		3.0		6.0	mV
I_{os}	Input Offset Current			10		50	nA
I_B	Input Bias Current			100		200	nA
A_{vo}	Large-Signal Voltage Gain	$V_s = \pm15V$, $R_L \geq 2k\Omega$ $V_{out} = \pm10V$	25		25		V/mV
V_{om}	Output Voltage Swing	$V_s = \pm15V$, $R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12 ±10		±12 ±10		V V
CMVR	Input Voltage Range	$V_s = \pm20V$	±15				V
CMRR	Common Mode Rejection Ratio	$R_s \leq 50k\Omega$	80		70		dB
PSRR	Power Supply Rejection Ratio	$R_s \leq 50k\Omega$		100		150	μV/V

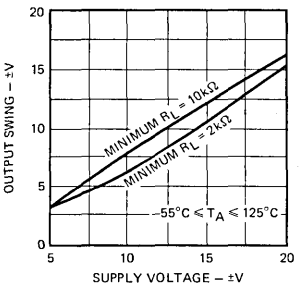
Notes 1. Derate metal can package at 6.8mW/°C for operation at ambient temperatures above 75°C.
2. For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
4. The SSS741 specifications apply for $\pm5V \leq V_s \leq \pm20V$. The SSS741C specifications apply for $V_s = \pm15V$.

GUARANTEED PERFORMANCE

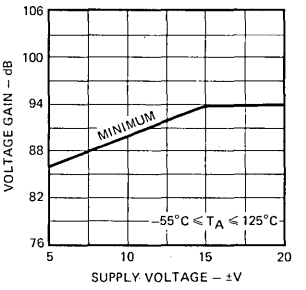
Input Voltage Range



Output Swing



Voltage Gain



MAXIMUM RATINGS HIGH-PERFORMANCE DUAL FREQUENCY COMPENSATED OP AMP SSS747/747C

Supply Voltage	
SSS747	±22V
SSS747C	±18V
Internal Power Dissipation (Note 1)	
DIP, Metal Can	800mW
Flat Package	500mW
Differential Input Voltage	±30V
Voltage between Offset Null and V^-	±0.5V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
SSS747	−55°C to +125°C
SSS747C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C) (Note 4)

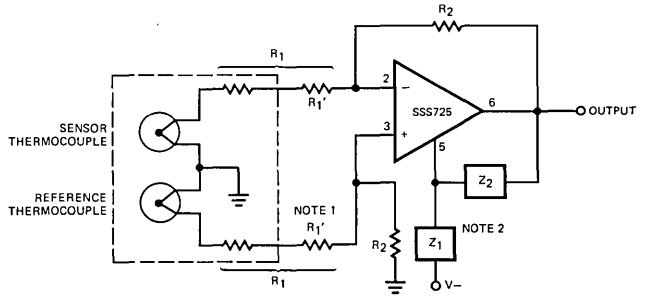
Symbol	Parameter	Conditions	SSS747 Min.	SSS747 Max.	SSS747C Min.	SSS747C Max.	Units
V_{os}	Input Offset Voltage	$R_S \leq 50k\Omega$		2.0		5.0	mV
I_{os}	Input Offset Current			5.0		20	nA
I_B	Input Bias Current			50		100	nA
R_{in}	Input Resistance		2.0		1.0		MΩ
A_{vo}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_s = \pm 15V$, $V_{out} = \pm 10V$	100		50		V/mV
V_{om}	Output Voltage Swing	$V_s = \pm 15V$, $R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12 ±10		±12 ±10		V V
CMVR	Input Voltage Range	$V_s = \pm 15V$ $V_s = \pm 20V$	 ±15		±12		V V
CMRR	Common Mode Rejection Ratio	$R_S \leq 50k\Omega$	80		70		dB
PSRR	Power Supply Rejection Ratio	$R_S \leq 50k\Omega$		100		150	μV/V
P_d	Power Dissipation	$V_s \leq \pm 15V$		85		85	mW
CS	Channel Separation		100				dB
The Following Specifications Apply Over The Operating Temperature Ranges							
V_{os}	Input Offset Voltage	$R_S \leq 50k\Omega$		3.0		6.0	mV
I_{os}	Input Offset Current			10		50	nA
I_B	Input Bias Current			100		150	nA
A_{vo}	Large Signal Voltage Gain	$V_s = \pm 15V$, $V_o = \pm 10V$, $R_L \geq 2k\Omega$	25		25		V/mV
V_{om}	Output Voltage Swing	$V_s = \pm 15V$, $R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	±12 ±10		±12 ±10		V V
CMVR	Input Voltage Range	$V_s = \pm 20V$	±15				V
CMRR	Common Mode Rejection Ratio	$R_S \leq 50k\Omega$	80		70		dB
PSRR	Power Supply Rejection Ratio	$R_S \leq 50k\Omega$		100		150	μV/V

Notes 1. *Derate metal can package at 6.8 mW/°C for operation at ambient temperatures above 30°C, the dual-in-line package at 9 mW/°C for operation at ambient temperatures above 60°C, and the Flat package at 5.4 mW/°C for operation at ambient temperatures above 57°C.*

2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be ground or either supply. Rating applies to 125°C case temperature or +60°C ambient temperature for each side.
4. The SSS747 specifications apply for $\pm 5V \leq V_s \leq \pm 20V$, unless otherwise noted. The SSS747C specifications apply for $\pm 5V \leq V_S \leq \pm 15V$, unless otherwise noted.

TYPICAL APPLICATIONS

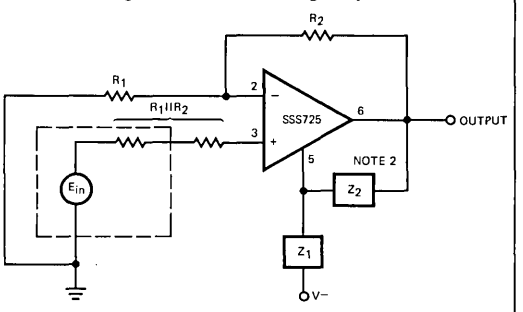
Thermocouple Amplifier — SSS725



$$A_V = \frac{-R_2}{R_1 + \frac{R_1}{A_{VO}} + \frac{R_2}{A_{VO}}}$$

Notes:
(1) R_1' is adjusted so that the sum of R_1' and the thermocouple circuit resistance equals the correct value for R_1.
(2) See Frequency Compensation Circuit.

High Gain Non-Inverting Amplifier

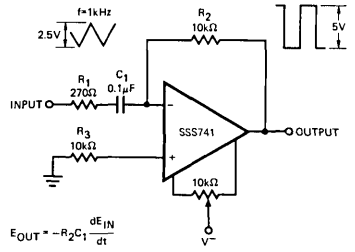


$$A_V = \frac{R_1 + R_2}{R_1 + \frac{R_1}{A_{VO}} + \frac{R_2}{A_{VO}}}$$

For ideal resistors and open loop gain greater than 10^6, in a +1000 gain configuration, the gain error will be less than 0.1% and input impedance will be greater than 700MΩ.

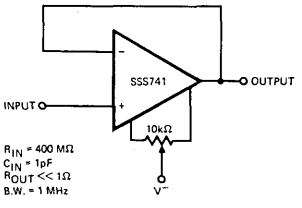
SSS741

Differentiator



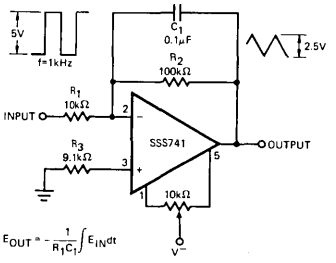
$$E_{OUT} = -R_2C_1\frac{dE_{IN}}{dt}$$

Unity Gain Voltage Follower



R_{IN} = 400 MΩ
C_{IN} = 1pF
R_{OUT} << 1Ω
B.W. = 1 MHz

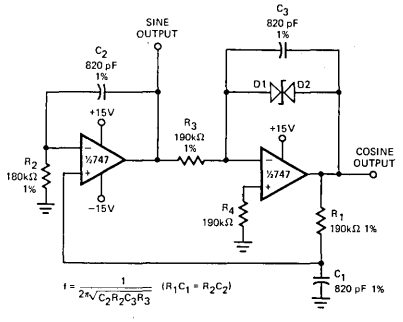
Integrator



$$E_{OUT} = -\frac{1}{R_1C_1}\int E_{IN}dt$$

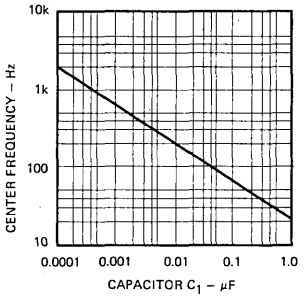
SSS747

Quadrature Oscillator

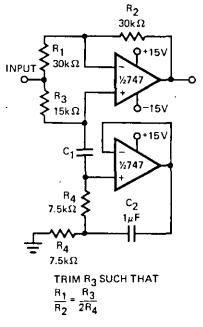


$$f = \frac{1}{2\pi\sqrt{C_2R_2C_3R_3}} \quad (R_1C_1 = R_2C_2)$$

Notch Frequency as a Function of C_1

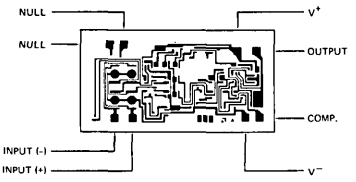


Notch Filter Using the 747 as a Gyrator

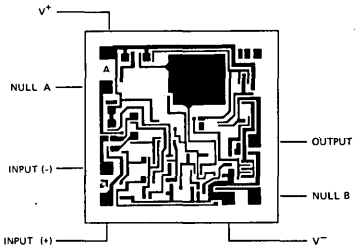


Metallization and Pad Layouts

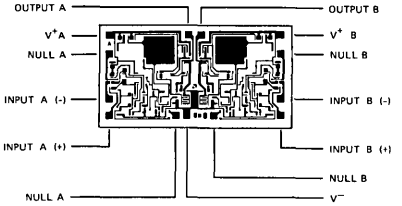
SSS725



SSS741

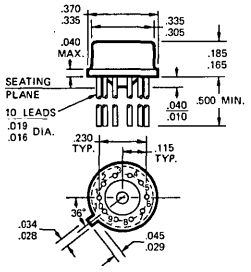


SSS747

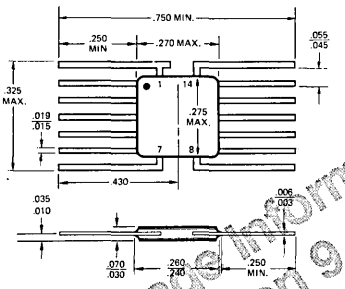


PHYSICAL DIMENSIONS SSS747

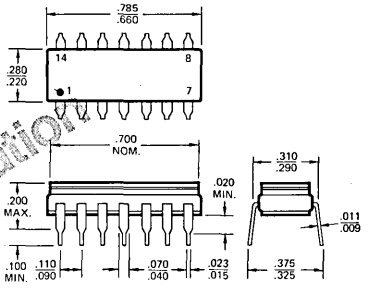
Metal Can



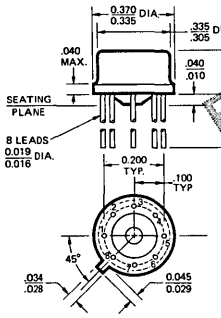
Flat Package



Dual-In-Line



Metal Can SSS725 SSS741



Notes:
(1) All dimensions in inches.
(2) Leads are gold-plated kovar.
(3) All leads through. No pins connected to case on SSS725.
(4) Pin 4 connected to case on SSS741.

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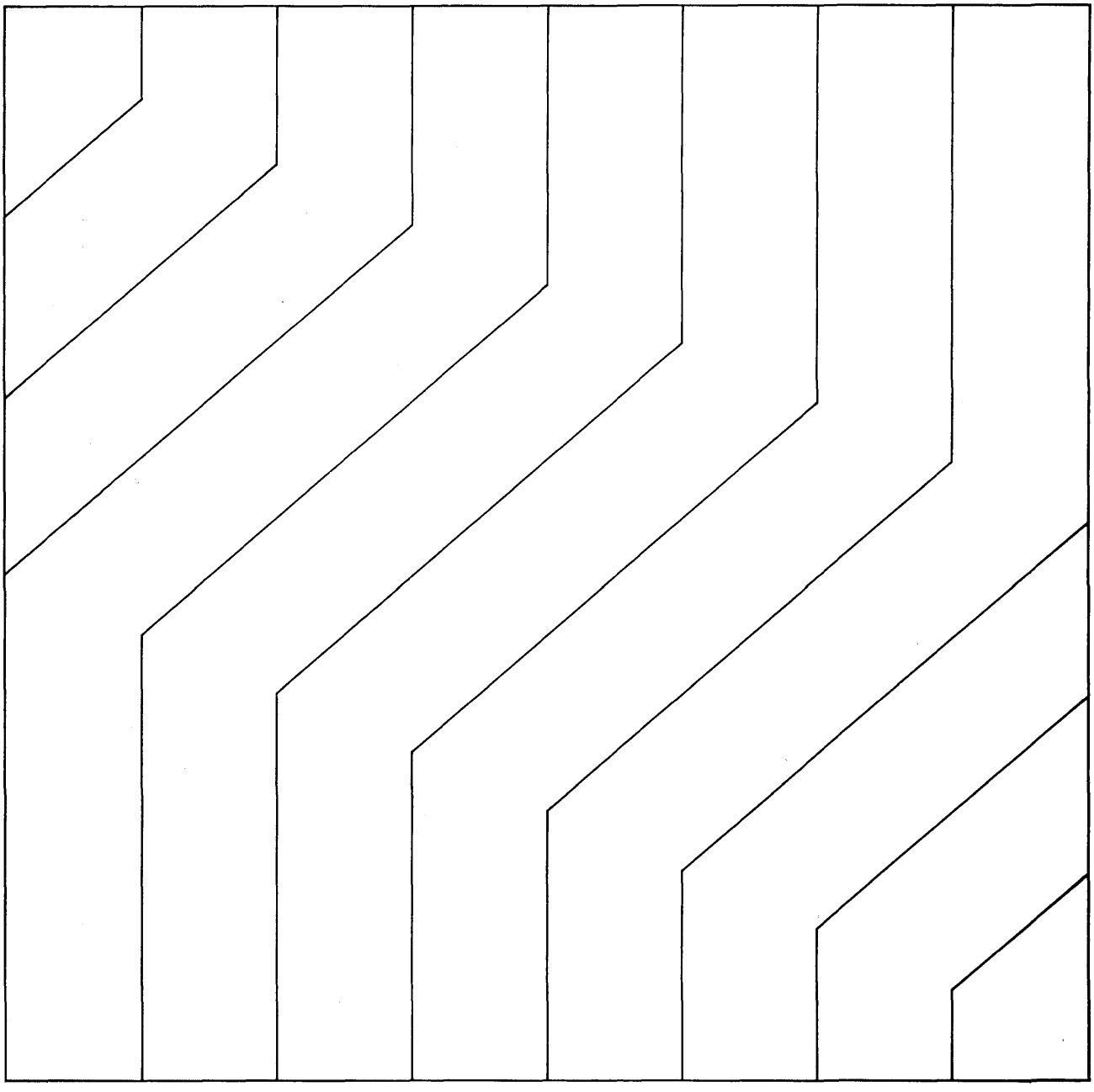


A DESIGNER'S GUIDE TO LOW POWER MSI

A DESIGNER'S GUIDE TO LOW-POWER MSI

A good system design meets three goals: minimum package count, maximum speed and minimum power dissipation. Advanced Micro Devices' family of low-power MSI circuits provides an important tool for achieving these goals and for optimizing total sytem performance.

Low-power MSI gives the logic designer the ability to trade off power and speed in his system to his best benefit. When only standard TTL/MSI is used, many devices operate at speeds much greater than that required by the system. This extra unused speed costs power. The Am93L family of low-power MSI has been designed to reduce power consumption and at the same time to maintain speed and drive capability at levels compatible with most system applications. As a general rule, low-power MSI devices consume one-fourth the power and operate at about one-half the speed of the equivalent standard MSI device.

The low-power MSI family includes all the functional building blocks of standard 9300 series MSI. The devices are pin-for-pin compatible and, in many cases, can simply be substituted for the standard part in existing systems. Low-power devices from Advanced Micro Devices are designated by an 'L' following the '93' prefix. For example, the low-power version of the 9316 counter is the Am93L16.

Because the 93L family has been designed with the total system in mind, the devices all have sufficient drive capability to interface with standard TTL circuits. Most outputs will drive three TTL loads, so there is generally no problem in mixing standard and low-power devices in the same system. By selecting low-power devices wherever speed is not critical and standard devices wherever speeds are crucial, the system designer can greatly reduce the power consumption of his system without sacrificing system speed.

TABLE 1

Device	Am93L Series speed	Am93L Series power	Standard 9300 Series speed	Standard 9300 Series power	% reduction in power using 93L
93L00 four bit shift reg.	10MHz	75mW	25MHz	300mW	75% lower
93L01 one of ten decoder	50ns	50mW	22ns	135mW	63% lower
93L08 dual four bit latch	30ns	100mW	16ns	325mW	69% lower
93L09 dual four input mux	30ns	37mW	10ns	150mW	75% lower
93L10 decade counter	13MHz	75mW	28MHz	300mW	75% lower
93L11 one of sixteen dec.	50ns	58mW	21ns	175mW	67% lower
93L12 eight input mux	30ns	45mW	10ns	135mW	67% lower
93L14 four bit latch	32ns	50mW	12ns	175mW	71% lower
93L16 hexadecimal counter	13MHz	75mW	28MHz	300mW	75% lower
93L18 priority encoder	29ns	75mW	16ns	275mW	73% lower
93L22 quad two input mux	31ns	45mW	10ns	150mW	70% lower
93L24 five bit comparator	68ns	52mW	31ns	195mW	74% lower
93L28 dual 8 bit shift reg.	16MHz	80mW	30MHz	300mW	73% lower
93L38 multiple port memory	170ns	99mW	48ns	320mW	69% lower
93L40 four bit ALU	56ns	110mW	20ns	425mW	74% lower
93L41 four bit ALU	48ns	125mW	19ns	470mW	73% lower
31L01 16w x 4b RAM	75ns	130mW	31ns	450mW	71% lower
96L02 dual one-shot	55ns	50mW	27ns	175mW	72% lower
26L02 dual one-shot	55ns	50mW	25ns	175mW	72% lower

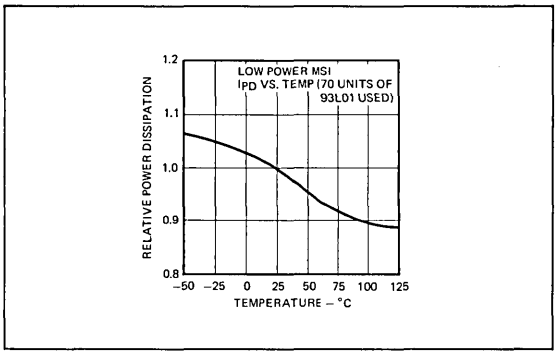


Fig. 1.

Because monolithic resistor values change with temperature, the power dissipation of the circuits is also a function of temperature. Figure 1 shows power consumption over full temperature ranges as a factor of the power dissipation at 25°C ambient. Guaranteed maximum power supply currents are given in the individual data sheets for each product for minimum, maximum and room temperature.

Input and Output Characteristics of Low-Power MSI

Low-power MSI uses the same basic circuits that are used in standard TTL. The lower power is achieved by changing resistor values and processing parameters. A typical LP/MSI input and output circuit is shown in Figure 2.

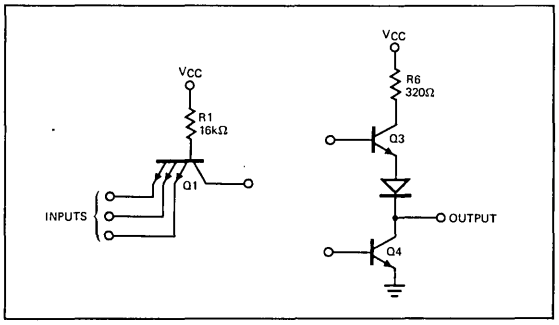


Fig. 2. Typical Low Power Output and Input

When an output is HIGH, Q3 is on and Q4 is off. The output voltage rises to about three volts, and current may be supplied via R6 and Q3. When an output is LOW, Q3 is off and Q4 is on. Current is sunk from the output to ground through Q4, with the output voltage lying at V (sat), or around 0.2 volt.

When an input is HIGH, then the emitter-base junction of Q1 is reverse biased, and only a small leakage current will flow into the input. A LOW input turns on Q1 and current flows from Vcc through R1 and Q1 and out the input.

Since the resistors R1 and R6 are four times as large as the corresponding resistors in standard TTL, currents in the input and output are only one-fourth as large. Voltage levels are about the same in both standard and low power devices.

The logic LOW and HIGH voltage levels are defined in Table II.

Table II
Logic Levels of Low-Power MSI

Parameter	Definition	Limit
V_{OL}	voltage on output when output is LOW	0.3 V max.
V_{IL}	highest voltage guaranteed to be interpreted as a LOW at an input	0.7 V max.
V_{OH}	voltage on output when output is HIGH	2.4 V min.
V_{IH}	lowest voltage guaranteed to be interpreted as a HIGH on an input	2.0 V min.

These voltages, of course, are specified at particular currents. The input currents are designated I_{IH} in the HIGH case and I_{IL} in the LOW case. Output levels are specified at I_{OH} and I_{OL} for a HIGH and LOW output, respectively. Table III gives low power Unit Load values for these currents.

Table III
Input and Output Currents

Parameter	Definition	Limit
I_{IH}	input reverse current at 2.4 V	20μA max
I_{IL}	input forward current at 0.3V	−0.4 mA max
I_{OH}	output HIGH current at 2.4 V	−0.4 mA min
I_{OL}	output LOW current at 0.3 V	4.0 mA min

Although the standard TTL load is defined at a different LOW voltage than the 93L unit load, the Am93L family is guaranteed to drive a mixture of standard and low-power inputs. For example, assume a low-power MSI device with loading rules as shown below:

LOADING RULES

In Unit Loads (Notes)

	TTL LOADS		93L LOADS	
Input Load Factor	**HIGH**	**LOW**	**HIGH**	**LOW**
A_0, A_1, A_2, A_3	0.5	0.25	1.0	1.0
Output Drive	**HIGH**	**LOW**	**HIGH**	**LOW**
All outputs	6	3	12	12

NOTES:
1) A TTL Unit Load is specified as 0.4 V at −1.6 mA LOW, 2.4 V at 40 μA HIGH.
2) A 93L Unit Load is specified as 0.3 V at−0.4mA LOW, 2.4 V at 20 μA HIGH.
3) Enough Output LOW current is available to mix TTL and 93L Loads and still meet the 93L requirement of a V_{OL} of 0.3 V.

The outputs can drive twelve 93L loads in either the HIGH or LOW state. This means that an output can be connected to twelve inputs of one load each. Alternatively, the output can drive three standard TTL inputs of one TTL load each. It is also possible to mix standard and low-power inputs. Enough current can be sunk in the LOW state to drive one or two standard TTL input loads while holding the output level below the 0.3 volt V_{OL} of the low power devices. Hence, the output described can drive any combination of loads shown in the table below:

TTL Loads Driven	Additional 93L loads which can be driven
0	12
1	8
2	4
3	0

If these loading rules are adhered to, then noise margins ($V_{OH} - V_{IH}$; $V_{IL} - V_{OL}$) will be at least 400 mV over the full temperature range for which the device is specified. For low-power outputs driving standard TTL inputs, the noise margin in the LOW state is increased to at least 500 mV.

Low-power MSI devices may be driven by standard TTL outputs. In this case the fan-out of the TTL device should be multiplied by four in the LOW state and two in the HIGH state to determine the number of 93L loads that may be driven. Most TTL outputs have a fan-out of twenty HIGH and ten LOW TTL loads. This is equivalent to forty 93L loads HIGH and LOW.

There is a reduction in guaranteed LOW level noise margin to 300 mV because the V_{OL} of standard TTL is 0.4 volt and the V_{IL} of LP/MSI is 0.7 V. In actual practice, the noise margin will be higher than 300 mV because the low-power V_{IL} drops to 0.7 V only at the temperature extremes, and even with full loading the standard TTL V_{OL} is rarely as high as 0.4V.

These noise margins are illustrated graphically in Figure 3. Because the low-power devices are slower than standard power

devices, the AC noise immunity is increased in a low-power system. The devices are less susceptible to false triggering and amplification of noise spikes than their standard power equivalents.

Switching Characteristics

The basic switching considerations in low-power MSI are identical to those in standard MSI; the times are just a little longer. Some of the terms used are defined and illustrated in the next few paragraphs.

1. $t_{pd}+$ and $t_{pd}-$

These are the standard designations for delays through combinational logic networks. The delay from an input change to an output going LOW is called "$t_{pd}-$"; the delay to an output going HIGH is "$t_{pd}+$". A typical waveform is shown in Figure 4.

In this waveform, the output will change at some time during the interval marked with diagonal lines. The output is guaranteed to be settled by $t_{pd}\pm$ max. Some devices also have a guaranteed t_{pd} min, which is the earliest that the output will change following an input transition.

2. ts : set up, hold and "release" times

For synchronous devices or devices with latches, some inputs must be stable for a certain time interval before the end of the clock or enable pulse. This interval is the region in time during which devices are "sampling" their inputs. As an example, consider a latch with a D input and an active LOW enable. The latch will store the information present on its input just before the enable goes HIGH. The question is, how long does the input level have to be present before the enable goes HIGH. A particular device will sample its input at some exact instant, but in a group of devices some are slower than others. The result is an interval at some time during which all devices, fast or slow, will sample their inputs.

Most inputs respond differently to HIGH and LOW data. There are, therefore, two set-up times for an input on a given device, the HIGH set-up time, t_{sH}, and the LOW set-up time, t_{sL}. Let's assume that for the latch, the following numbers are specified:

Parameter	Definition	min	typ	max	units
t_{sH}	HIGH data set-up time	−5	−1	5	ns
t_{sL}	LOW data set-up time	0	10	16	ns

These numbers mean that the slowest devices require 5ns. before the end of the enable to respond to a HIGH and 16 ns. to respond to a LOW. The fastest devices will store a LOW if it appears coincident with the end of the enable and a HIGH if it appears 5ns. after the enable.

To reliably store data, the following rules must be followed.

1. Storing a HIGH

The HIGH level must be applied by t_{sH} max. in order to guarantee the slowest devices responding. The HIGH must be maintained until after t_{sL} min. to guarantee that the fastest devices do not respond to a LOW.

2. Storing a LOW

The LOW must be applied by t_{sL} max. and must be maintained until after t_{sH} min.

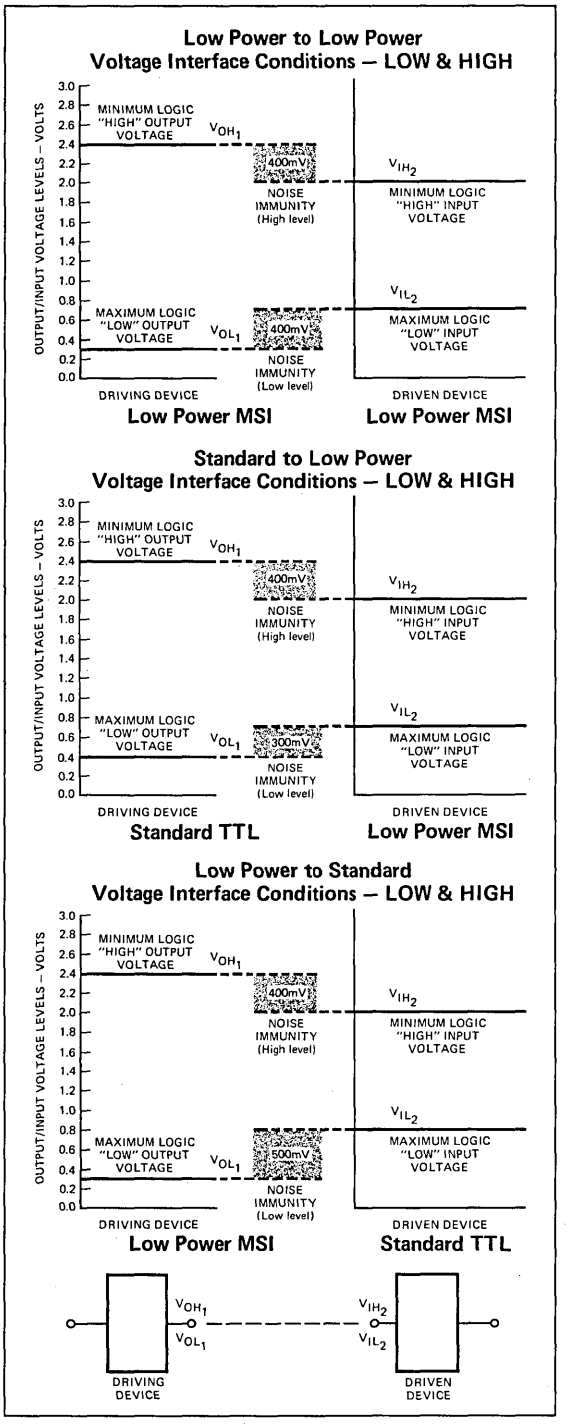


Fig. 3. Noise Margins in Low Power and Mixed Systems

A timing specification waveform is shown below. Figure 5 shows the input requirements for writing a HIGH and a LOW as two separate cases.

SWITCHING TIME WAVEFORMS

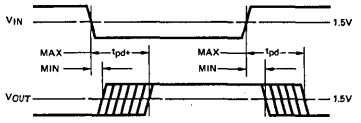


Fig. 4. Propagation Delay Specification

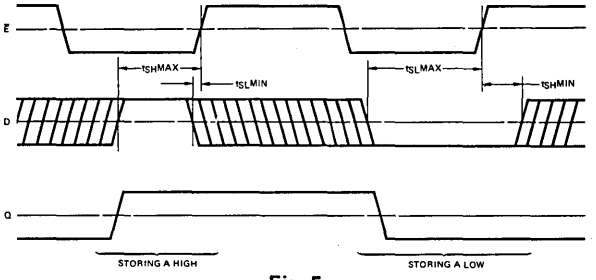


Fig. 5

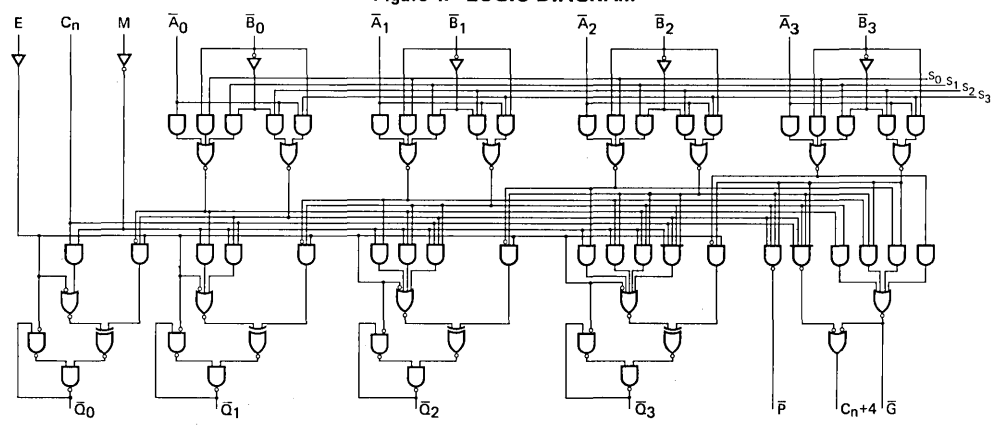
Key to Timing Diagrams

WAVEFORM				
INPUT FORCING FUNCTION	MUST BE STEADY	MAY CHANGE HIGH TO LOW	MAY CHANGE LOW TO HIGH	DON'T CARE
OUTPUT RESPONSE	WILL BE STEADY	WILL BE CHANGING HIGH TO LOW	WILL BE CHANGING LOW TO HIGH	CHANGING; STATE UNKNOWN

THE Am2506-- A LATCHING ALU

By John Springer, Digital Applications

Figure 1. LOGIC DIAGRAM



The Am2506 is a monolithic device that combines in a single package two functions commonly used together: a four-bit arithmetic logic unit (Am74181) and a four-bit latch.

Like the Am9341 or Am74181, the device performs addition, subtraction, or any logic function on two 4-bit words, A_{0-3} and B_{0-3}. The operation is determined by the mode control, M, and the four select lines S_{0-3}. The look-ahead carry functions, G and P, are produced as well as a carry-out signal, C_{n+4}. The function outputs of the device are Q_{0-3}. All these signals are located on the same pins as the corresponding signals on the Am9341 and Am74181.

The pin labeled "E" is an active HIGH latch enable. As long as this pin is HIGH, data from the ALU appears directly on the Q outputs, and the device operation is identical to the Am9341 in all respects including switching speeds. (The only difference is that the A=B output of the Am9341 has been replaced by the latch enable pin in the Am2506.) When the enable goes LOW, the data on the Q outputs latches and no further changes occur. This allows the inputs to the device to change without destroying the output data from the previous operation.

The Am2506 allows very high speed system operation in a "pipelined" mode, because the data can be synchronized at the Am2506 output. For example, the system shown in Figure 3 adds eight different numbers to produce a single sum. Using ordinary ALUs, signals must propagate through three levels of devices before the result is obtained. Using the Am2506, there are still three levels of devices, but the system can work on three problems at once. While the last Am2506 is adding the latched outputs of the second level, the second level is adding the latched outputs of the first level, and the first level is performing the initial addition of four new pairs of numbers. For a series of operations, the average delay is that of one level of ALUs rather than three levels.

Another application of the Am2506 involves using it in conjunction with a latch, as shown in Figure 4. Since the circuit has an active HIGH enable and the latch has an active LOW enable, the same signal can be applied to both pins, producing master-slave type operation. In Figure 4, the Am2506 outputs go to eight quad latches, and one of the latches is selected by the Am9301 decoder. Data is applied to the Am2506 input while the "clock" is LOW. When a HIGH level occurs on the clock line, the result is transferred, synchronously, into the selected latch. Any of the latch outputs can be fed back to the Am2506 inputs with no race conditions occurring.

Model of Am2506 Arithmetic Logic Unit

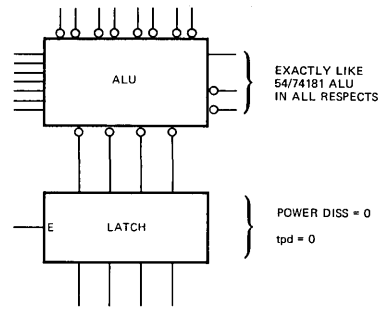


Figure 2

High Speed Multiple Word Adder Using Am2506s

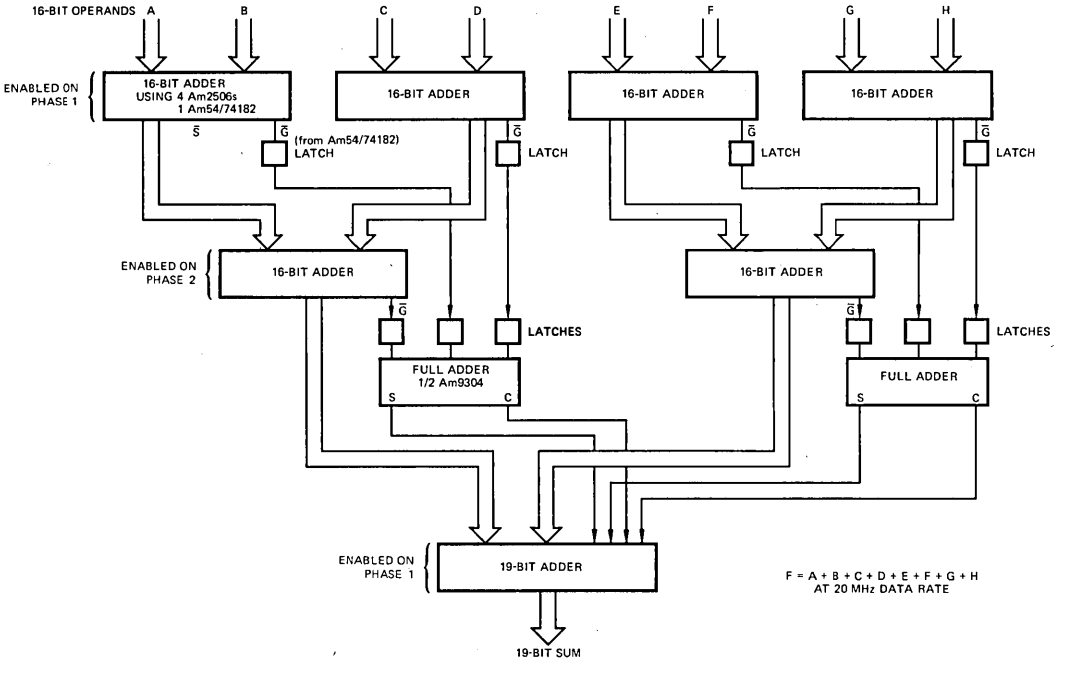


Figure 3.

Using quad latches with Am2506 to form multiple master-slave registers.

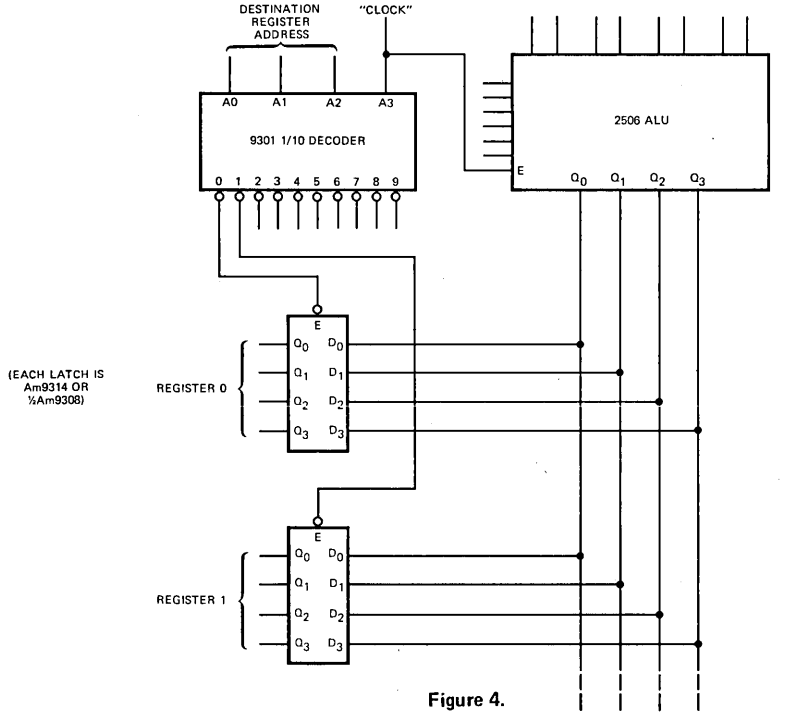
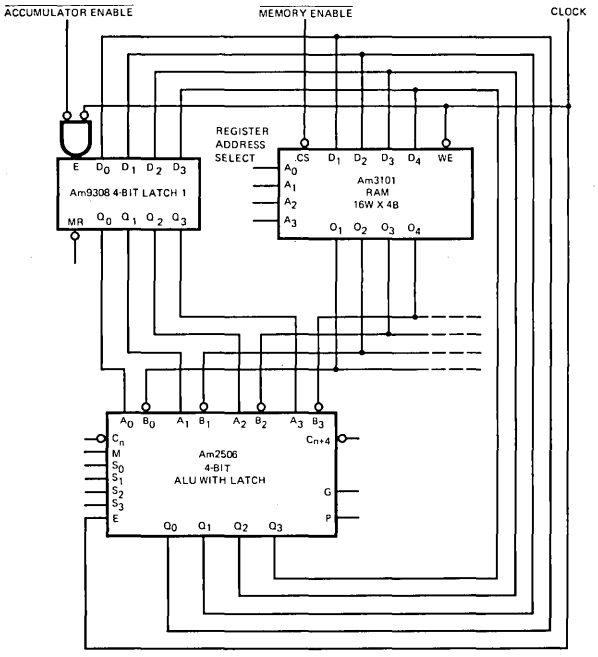


Figure 4.

16-Word Arithmetic Register 4-Bit Slice



FUNCTION TABLE

S_0	S_1	S_2	S_3	Arithmetic (M = L, $\overline{C}_n$ = H)	Logic (M = H)
L	L	L	L	A	$\overline{A}$
H	L	L	L	$A + \overline{B}$	$\overline{A}B$
L	H	L	L	A + B	$\overline{A}\overline{B}$
H	H	L	L	minus 1 (2's comp.)	Logic '0'
L	L	H	L	A plus AB	AB
H	L	H	L	AB plus $[A + \overline{B}]$	B
L	H	H	L	A plus B	$\overline{A \oplus B}$
H	H	H	L	AB minus 1	AB
L	L	L	H	A plus $A\overline{B}$	$\overline{A} + \overline{B}$
H	L	L	H	A minus B minus 1	$A \oplus B$
L	H	L	H	$A\overline{B}$ plus [A + B]	$\overline{B}$
H	H	L	H	$A\overline{B}$ minus 1	$A\overline{B}$
L	L	H	H	A plus A (2 x A)	Logic '1'
H	L	H	H	A plus $[A + \overline{B}]$	A + B
L	H	H	H	A plus [A + B]	$A + \overline{B}$
H	H	H	H	A minus 1	A

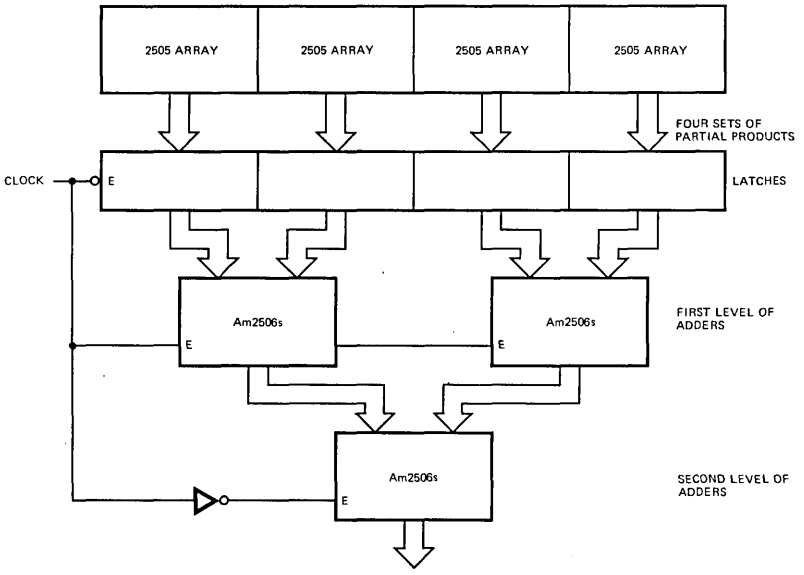
L = Low Voltage Level
H = High Voltage Level

Figure 5.

A variation of this system is shown in Figure 5, in which the Am2506 is used with the Am3101 16-word by 4-bit RAM. A four-bit latch, in this case half of an Am9308, is used as an accumulator, and the Am3101 is used as 16 data registers. The output of the Am2506 can be stored in either the accumulator latch or in the Am3101 memory. Data can enter the system on the open collector outputs of the memory and through the Am2506 using the "pass B" operation code. Note that since the memory inverts data passing through it, the B inputs to the Am2506 are interpreted as active LOW. To compensate for this, each of the functions in the function table has been modified by inverting the B variable.

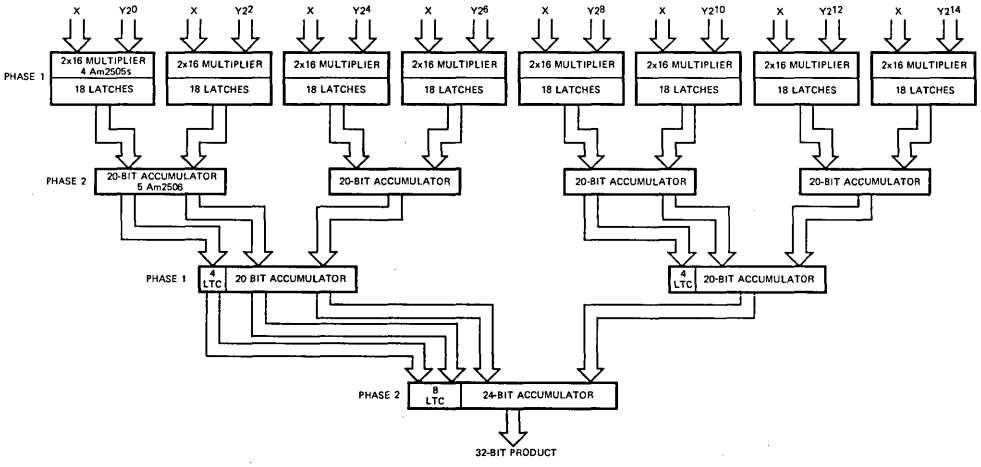
The Am2506 can be used in conjunction with the Am2505 digital multiplier to perform multiplication at a very high rate. Ordinarily multiplication is performed with the Am2505 by connecting the multipliers in an array. Each row of Am2505s generates a partial product dependent on the multiplicand and two bits of the multiplier. Each row of Am2505s then adds its partial product to that of the row above it, by means of an internal high-speed adder. When the addition has rippled through each row in the array, then all the partial products have been added together, and the outputs of the bottom row are the final product. Instead of using the internal adders in the Am2505s to sum the partial products, it is possible to allow each row to generate its partial product independently and then to add together the outputs of each row using separate high-speed look-ahead carry adders. When the Am2506 is used as the adder, then additional speed is gained because each level in the system can operate independently. This is outlined in Figure 6 for an eight by eight multiplication.

Four independent rows of Am2505 multipliers form four partial products in parallel. The partial products are latched and sent to two adders. As soon as the partial products are latched, a new multiplier and multiplicand can be applied to the Am2505s, so the next partial products are formed at the same time the first set is being added in the Am2506s. Another set of Am2506s forms a third level at which the final summation takes place. Assuming worst case propagation delays at 25°C, this system can accept new 8-bit operands every 100 ns. Typical delays allow operation at a 15 MHz rate. Figure 7 shows a 16 by 16 multiplier.



Very high-speed multiplication uses four arrays of Am2505 multipliers followed by two sets of adders for summing the partial products. The three levels of the system are operated in a "pipelined" fashion.

Figure 6.



10 MHz 16 by 16 Multiplier

Figure 7

TTL MSI ARITHMETIC LOGIC UNITS

By Clive Ghest, and John Springer, Digital Applications

INTRODUCTION

The arithmetic logic unit in a digital machine is usually the limiting element in the speed of a system. Now that MSI arithmetic logic units are available, much of the tedious design effort previously necessary has been reduced. These elements offer considerable cost and speed savings over an interconnected gate design, as well as reliability improvement. Complex MSIs give new emphasis to using hardware for solving problems previously performed in software, such as digital filter and Fast Fourier Transform calculations.

TECHNICAL BACKGROUND

An ALU is a digital subsystem that can perform various arithmetic and logic operations on two input variables. Speed is generally of the utmost importance, and, therefore, the majority of ALUs operate on parallel words. Maintaining high speed in a parallel operation presents a difficulty because the calculation starts at the least significant end of a word and proceeds to the most significant end. The result of an arithmetic operation at any bit position in the word depends not only on the two operand bits at that position, but also on all the less significant operand bits. The complete result is therefore not available until the carries have rippled through from the least to the most significant bit. The equations for the arithmetic operation "add" are:

$$S_i = A_i \oplus B_i \oplus C_i$$

$$C_{i+1} = A_iB_i + B_iC_i + A_iC_i$$

where A_i and B_i are the input operands at the i^{th} bit, C_i is the carry-in to the i^{th} bit and C_{i+1} is the carry-out of the i^{th} bit into the $(i+1)^{th}$ bit.

These iterative equations indicate that the delay for the addition of two n bit numbers is n−1 carry delays and one sum delay. A ripple carry adder for which this is indeed the case is shown in Figure 1. The adders are Am9304s.

In order to increase the speed of addition, extra logic must be used to anticipate what the carry will be at a given position without waiting for a ripple carry to propagate through the network. An adder constructed with carry anticipation circuitry is called a "look-ahead carry adder"

The carry-out of the i^{th} bit of an adder is:

$$C_{i+1} = A_i B_i + C_i (A_i + B_i)$$

Define two auxiliary equations:

$$\&_i = A_iB_i \qquad V_i = A_i + B_i$$

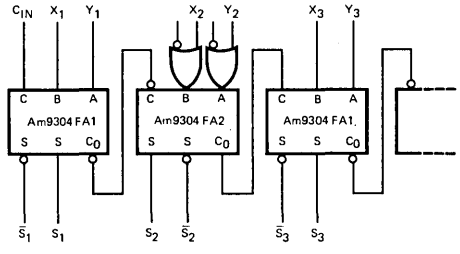
Then $C_{i+1} = \&_i + V_iC_i$

and by substituting for C_i, C_{i-1} etc.

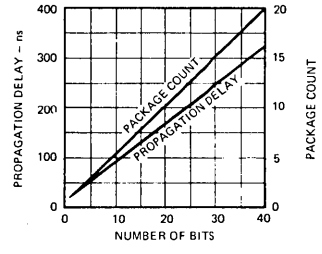
$$C_{i+1} = \&_i + V_i\&_{i-1} + V_iV_{i-1}\&_{i-2} + \ldots + (V_iV_{i-1}V_{i-2}\ldots V_O\, C_O)$$

An anticipated carry can be generated at any stage by implementing the above equation, using the auxiliary functions $\&_i$ and V_i. The sum equation can also be written in terms of these two auxiliary functions.

RIPPLE CARRY PARALLEL ADDITION



PROPAGATION DELAY AND PACKAGE COUNT AGAINST WORD LENGTH FOR RIPPLE CARRY ADDITION



Shown above is a high-speed ripple carry parallel addition scheme. Only one and-or-not gate delay is incurred at each stage allowing a typical addition speed of (N + 1) x 8 ns, where N is the number of bits in the word. The curve shows propagation delay of the ripple-Carry Adder drawn on the left. Plotted on the same diagram is a curve showing the low package count resulting from the Ripple Scheme.

Figure 1. Ripple Carry Adder

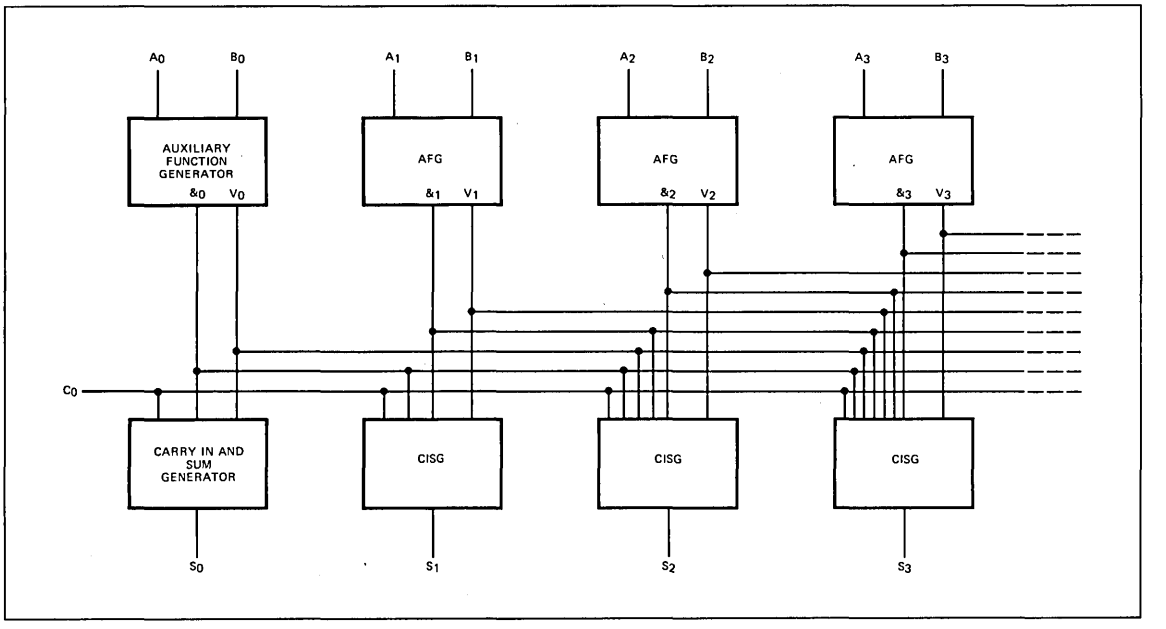


Figure 2. Single Level Look-Ahead Adder Using Auxiliary Functions

$$S_i = A_i \oplus B_i \oplus C_i$$

$$S_i = (A_i + B_i)\,(\overline{A_i B_i}) \oplus C_i$$

$$S_i = V_i \overline{\&_i} \oplus C_i$$

All the functions $\&_i$, V_i can be generated in one gate delay, and all the C_{i+1} signals in another gate delay. The sum terms S_i can therefore be obtained in approximately three unit delay times as against n+1 delay times for the ripple mode of operation. Figure 2 shows an adder using auxiliary equations.

The auxiliary function $\&_i$ is called "carry generate," because if it is true, then a carry is immediately produced into the next stage. The function V_i is called "carry propagate" because it implies that there will be a carry-in to the next stage if there is a carry-in to the i^{th} stage. That is, & causes a carry signal to be generated and V causes an existing carry to propagate from one stage to the next.

A serious drawback to the look-ahead carry adder is that as the word length is increased, the carry functions become more and more complex, eventually becoming impractical due to the large number of interconnections and heavy loading of the & and V functions. The auxiliary function concept can be extended, however, by dividing the word length into fairly small increments and defining auxiliary functions G and P (generate and propagate) for the entire block. For a given block, then, the function G is defined as a carry-out generated within the block; P is defined as a carry propagate over the block so that if the block receives a carry-in there should be a carry-out to the next block. If the block size is set at four bits, then the functions G and P can be defined in terms of the & and V functions for the four bits.

$$G = \&_3 + V_3\&_2 + V_3V_2\&_1 + V_3V_2V_1\&_0$$

$$P = V_3V_2V_1V_0$$

Note that neither of these terms involves a carry-in to the block, so no matter how many blocks are tied in an adder, all the blocks have stable G and P functions available in two gate delays (one to produce the & and V functions and another to produce G and P).

The G and P functions can be gated to produce a carry-in signal to each four-bit block, as a function of the less significant blocks. The carry-in to a block n is:

$$C_n = G_{n-1} + P_{n-1}G_{n-2} + P_{n-1}P_{n-2}G_{n-3} + \ldots$$

Finally, the carry-in to each of the bits in a four-bit block must include a term for a carry-in, so the carries-in to the four bits in the block are:

$$C_0 = C_n$$

$$C_1 = \&_0 + V_0\,C_n$$

$$C_2 = \&_1 + V_1\&_0 + V_1V_0C_n$$

$$C_3 = \&_2 + V_2\&_1 + V_2V_1\&_0 + V_2V_1V_0C_n$$

Figure 3 shows a look-ahead carry adder using a total of two levels of look-ahead (one internal to the four-bit blocks and one external). A total of four gate delays is required from application of operands to final sum.

The ripple-carry method can be used in conjunction with the look-ahead technique in several ways. (1) Look-ahead carry over sections of the adder and ripple carry between these sections. This method is often the most efficient in terms of hardware for a given speed requirement. (2) Look-ahead carry in parallel with a ripple carry. The logic required to perform this is less than for a true look-ahead though carries can be generated in the same delay as true look-ahead. However, the number of additions possible in a given time is reduced because when the inputs return to a quiescent state, a ripple situation occurs and n+1 delay times are required to remove the carries. This may not be a disadvantage since many systems require fast addition at a low frequency.

The majority of MSI arithmetic logic units have two levels of look-ahead as shown in Figure 3. The adder block consists of four stages and the second level auxiliary function generations

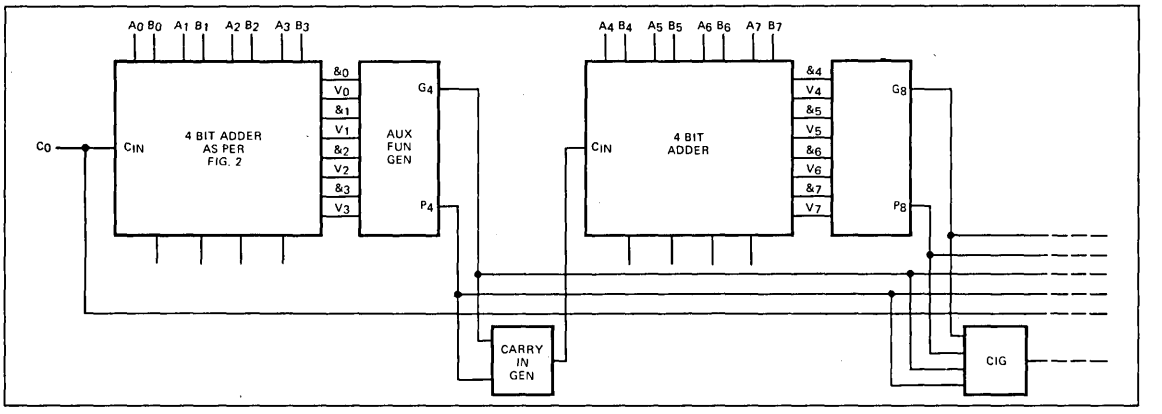


Figure 3. Two Level Look-Ahead Adder Using Two Sets of Auxiliary Functions

G and P are identical for each block. The design problem centers around the carry-in generation, which becomes more complex as the number of blocks of adders is increased, because the carry-in to a block is a function of all the previous Gs and Ps. There are two basic methods of solving this problem: (1) Incorporate the carry-in logic in the adder device itself. This has the advantage of a clean, straightforward design, but requires a considerable number of pins if the word length is long and the number of adder blocks is large. A compromise can be made by allowing ripple carry between groups of blocks of adders, and limiting the size of the carry input logic. This method is used in the Am9340 ALU. (2) Have the carry-input logic separate from the adder block. An MSI look-ahead carry circuit can then form the carry-input signals for several blocks. This method has the disadvantage that an extra circuit is required, few of which are needed in the system. The method does, however, free package pins for other important tasks, and is used on the Am54/74181 and Am2506 ALUs. The special look-ahead carry device is the Am54/74182.

FUNCTIONS

Many arithmetic and logic functions, other than addition, are required in digital systems. The most important of these is subtraction, since other arithmetic operations can be generated by a succession of additions and subtractions. The next most important function is shifting, which can be performed either before or after an arithmetic operation. Shifting operations can be built into ALUs, but require considerable pins if shifts of more than one place are allowed. Generally, shifting operations are performed external to the ALU with multiplexers; this allows the system designer more flexibility and frees pins for functions that can use the pins more efficiently. Although the number of possible logic functions of two variables is sixteen, the majority are seldom used. The most useful logic operations are AND and EXCLUSIVE OR. Other operations that can be used are OR and EQUIVALENCE, and the operation PASS, where one of the input operands passes through the ALU without change.

BINARY ARITHMETIC

There are several numbers representations commonly used in binary arithmetic. Positive numbers are the same in all representations, but notations for negative numbers differ.

1) Sign-Magnitude Notation
In this system the most significant bit of the number indicates the sign; 0 positive and 1 negative. The magnitude of the number is always positive.

Sign	MSB			LSB	
0,	1	1	0	1	+13
1,	1	1	0	1	-13

Sign magnitude is rarely used for addition or subtraction, though it may be convenient for multiplication and division.

2) 1s Complement
In 1s complement representation, negative numbers are the bit-wise inversion of their positive equivalents. Again, the most significant bit signifies sign. Arithmetically, $-X$ is represented as 2^N-X-1.

Sign	MSB			LSB	
0,	1	1	0	1	+13
1,	0	0	1	0	-13

Although 1s complement is extremely easy to form, it has a significant disadvantage of having two representations for zero, all 1s and all 0s.

3) 2s Complement
2s complement is the most common form of representation. It is more difficult to form than 1s complement, but it lends itself well to arithmetic computation and has no ambiguous states. It is formed by inverting the positive number and adding 1 to the LSB.

Sign	MSB			LSB	
0,	1	1	0	1	+13
1,	0	0	1	1	-13

For an N-bit word, the numerical values which can be represented range from $+(2^{N-1}-1)$ to $-(2^{N-1})$. Arithmetically $-X$ is represented as 2^N-X.

011	+3
010	+2
001	+1
000	0
111	-1
110	-2
101	-3
100	-4

ADDITION AND SUBTRACTION OF BINARY NUMBERS

For positive numbers in any representation, addition is straightforward, provided there is no carry-in to the sign bit.

For any N-bit X and Y

X plus Y = $A_i \oplus B_i \oplus Carry_i$ (i = 0 to N−1)

When one number is positive and one negative the operation depends on the representation of the negative number. If 2s complement is used, then ordinary addition gives the correct answer also in 2s complement.

	MSB				LSB	
+13	0	1	1	0	1	(The carry-out of the
− 6	1	1	0	1	0	most significant bit
+ 7	0	0	1	1	1	is disregarded)
−13	1	0	0	1	1	
+ 6	0	0	1	1	0	
− 7	1	1	0	0	1	

In 1s complement, a correction may be necessary in addition. If the result of the addition overflows (as in the first example above) an extra 1 must be added to the least significant bit.

	MSB				LSB	
+13	0	1	1	0	1	
− 6	1	1	0	0	1	
+ 7	1	0	0	1	1	0 overflow so add 1
						1 to LSB
	0	0	1	1	1	
−13	1	0	0	1	0	
+ 6	0	0	1	1	0	no overflow, so
− 7	1	1	0	0	0	answer is correct

The overflow in 1s complement is called an "end-around carry." The carry-out of the MSB is simply used as a carry-in to the LSB.

Subtraction is done in either representation by forming the 1 or 2s complement of the subtrahend and adding.

1s complement subtraction

+13	0	1	1	0	1	→	0	1	1	0	1
− + 6	0	0	1	1	0		1	1	0	0	1
+ 7							1	0	0	1	1	0
											→	1
							0	0	1	1	1	

2s complement subtraction

+ 8	0	1	0	0	0	→	0	1	0	0	0
− − 4	1	1	1	0	0		0	0	0	1	1
+12											1 ← (forced carry)
							0	1	1	0	0

Therefore, 2s complement subtraction is performed using IC ALUs by complementing (inverting) the subtrahend and forcing a carry-in to the LSB to add one. This effectively creates a 2s complement number. The carry-out of the adder becomes a "not borrow" out. Therefore, an adder with an active HIGH carry will have a LOW on the carry-out if a subtraction causes a borrow.

LOGIC POLARITIES

Arithmetic logic units have the property that the majority of arithmetic operations do not change when the logic polarity of signals is altered. The same device will perform arithmetic in either the active HIGH level (positive logic), or active LOW level (negative logic) representation. Logic operations usually change function when the polarity is reversed; this is often no disadvantage because the functions are a closed set, and when the polarity is altered, the resulting function is included in the same set.

The arithmetic functions add and subtract are independent of change of logic polarity. The sum and carry functions are:

$$S_i = A_i \oplus B_i \oplus C_i$$
$$C_{i+1} = A_i B_i + C_i A_i + C_i B_i$$

Inversion of the inputs results in inversion of the outputs:

$$\overline{A}_i \oplus \overline{B}_i \oplus \overline{C}_i = \overline{S}_i$$
$$\overline{A}_i \overline{B}_i + \overline{C}_i \overline{A}_i + \overline{C}_i \overline{B}_i = \overline{C}_{i+1}$$

These equations are the fundamental equations for an adder and the change of output polarity for several adder stages connected together must occur independent of what kind of carry structure is used. Auxiliary functions such as G and P do not remain invariant under change of input polarity, but the identical interconnection pattern must produce the correct carry-in function in either representation. All the above considerations are true for subtraction, since subtraction, if generated by using complements, only differs by having one variable in the adder equations inverted, and if it is true for one method, then it must be true for all other methods.

Logic functions change under a change of logic representation. For example, the logic function AND changes to the function OR, and the function EXCLUSIVE OR changes to EQUIVALENCE. If the logic functions form a set such that a change of polarity gives a change of function that is included in the set, then only the function code must be reinterpreted along with the operand logic polarity.

OVERFLOW

When numbers are added or subtracted the result must lie within the range of numbers that can be handled by the operand word length. Numbers are normally represented either as fractions with the binary point between the sign bit and the rest of the word, or as integers where the binary point is after the least significant bit.

For addition of numbers in fractional representation,

$$A = a2^{-(n-1)} - a_s \qquad -1 \leqslant A \leqslant 1-2^{n-1}$$
$$B = b2^{-(n-1)} - b_s \qquad -1 \leqslant B \leqslant 1-2^{n-1}$$
$$S = A + B = (a+b)2^{-(n-1)} - (a_s + b_s)$$

Overflow will occur if S lies outside this range. The logic function that indicates that the result of an operation is outside the range is:

OVR = $C_S \oplus C_{S+1}$ where C_S is the carry-in to the sign bit and C_{S+1} is the carry-out of the sign bit.

For a four-bit ALU with the sign bit in the most significant position, the carry-out of the sign bit is available, but the carry-in to the sign bit is not. Various methods are available to regenerate it. The simplest is to use the equation:

$$C_S = S_S \oplus A_S \oplus B_S$$

and

$$OVR = S_S \oplus A_S \oplus B_S \oplus C_{S+1}$$

This method produces the overflow signal after the sum bits. If subtraction as well as addition is used, the above equation must be changed to invert the B sign during subtraction.

$$C_S = S_S \oplus A_S \oplus B_S \oplus \overline{Add}/Subt$$

and

$$OVR = S_S \oplus A_S \oplus B_S \oplus \overline{Add}/Subt \oplus C_{S+1}$$

An improved method of generating the overflow signal requires only two gate delays after the carry-out is available. This allows the overflow to appear at about the same time as the sum. The sign bit is processed completely outside the ALU. The last bit of the ALU, where the sign bit would normally be, is set with $\overline{B}_3$ = LOW and $\overline{A}_3$ = Add/$\overline{Subt}$. This will force a permanent carry propagate condition on Bit F_3 so that the carry-out of the ALU will be the carry-out of the bit F_2 position. The carry-out of the ALU is then C_S, the carry-in to the sign bit. The equation for the overflow can be written as:

$$OVR = C_S \ [\overline{A}_S \oplus (B_S \oplus \overline{Add}/Subt)] \oplus A_S \ (B_S \oplus \overline{Add}/Subt)$$

Both the overflow and the final sum sign can be produced by an Am9309 dual four-input multiplexer used as a random function generator as shown in Figure 4. Since the C_S signal goes into the data input of the multiplexer, the overflow is generated only two gate delays later; the final sum digit is produced at approximately the same time as the other sum digits since the logic has to wait for the C_S signal before the sum bit can be generated.

ADVANCED MICRO DEVICES MSI ARITHMETIC LOGIC UNITS

The three most widely used and powerful MSI arithmetic logic units are the Am9340, the Am54/74181 (Am9341) and the Am2506. All of these devices are parallel four-bit units incorporating a look-ahead carry adder and are capable of performing addition, subtraction and various other arithmetic and logic operations at high speed. Each device has particular advantages, and the choice of which device is optimum depends upon the application and system speed requirement.

THE Am9340 ALU

The Am9340 MSI arithmetic logic unit is a high-speed combinatorial circuit capable of performing addition, subtraction, and several logic functions on two 4-bit binary words. Internally the device uses look-ahead carry logic for high speed. Provision is also made for look-ahead carry interconnections between several Am9340s with no additional logic required.

The ALU is extremely suitable for use in general and special purpose digital computers as the center of high-speed arithmetic units. The Am9340 can perform arithmetic on binary numbers in 1s complement or 2s complement. The input data can be either active HIGH or active LOW.

Am9340 FUNCTIONAL DESCRIPTION

The Am9340 logic diagram is shown in Figure 5. Functionally, the device can be divided into several parts. At the top is a set of gates that produce the AND and OR functions of the A and B inputs.

$$A_i B_i = \&_i$$

$$A_i + B_i = V_i$$

The gates that form the & and V functions are under the control of the S_0 and S_1 inputs so that several different AND and OR functions can be formed. For example, the functions, instead of being AB and A + B, may be $A\overline{B}$ and $A + \overline{B}$. This control is used to vary the function performed by the circuit. The two sets of functions cited above are used for addition and subtraction, respectively.

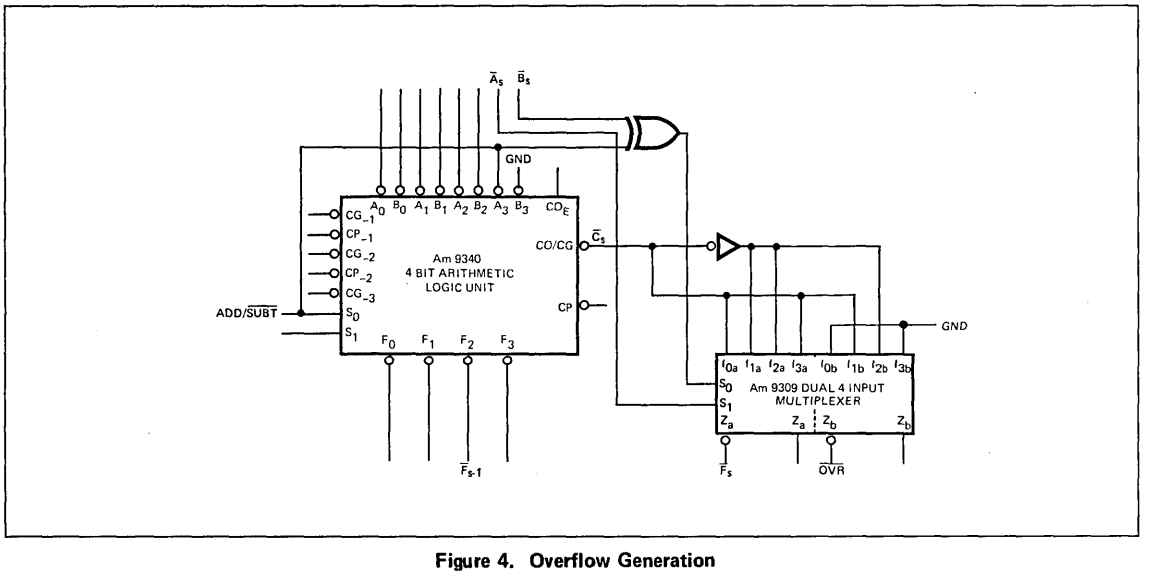


Figure 4. Overflow Generation

At the bottom of Figure 5 is a set of adders, which add (Ex OR) the & and V signals for a particular bit, and the carry-in to that bit.

At the left of the logic diagram is a set of gates that produce a carry-in function. These gates accept $\overline{CG}$ and $\overline{CP}$ outputs from other Am9340s to produce a carry-in.

$$\text{Carry-in} = \overline{CG}_{-1}\,\overline{CP}_{-1}\,\overline{CG}_{-2} + \overline{CP}_{-2}\,\overline{CG}_{-3}$$

The subscripts –1, –2, and –3 refer to the preceding devices. A carry-in to one Am9340 is produced by a carry generate from the immediately preceding device ($\overline{CG}_{-1}$) or by a propagate from the preceding device and a carry generate from an Am9340 two devices back ($\overline{CP}_{-1}\,\overline{CG}_{-2}$), etc.

One of the select lines, S_1, blocks the propagation of carries between bits. This control is used to select logic or arithmetic functions. For example, subtraction is basically A ⊕ $\overline{B}$ ⊕ Carry.

If S_1 is HIGH carries are forced at all bits, and the output becomes A ⊕ $\overline{B}$ ⊕ 1 = A ⊕ B.

At the right of Figure 5 is a series of gates that produce the look-ahead carry-out functions. One gate produces an active LOW carry propagate over the block of four bits. Logically, it is the AND of the four internal carry propagates. Functionally, it means that if there is a carry-in to this package, there should be a carry-out to the next package. It is activated by the presence of 1111 in the Am9340. CP = $V_3V_2V_1V_0$

	MSB			LSB	
Word A	1	0	1	0	
Word B	0	1	0	1	
Sum	1	1	1	1	"Carry Propagate"

The other gate forms an active LOW carry generate for the block of four bits. The CG is a carry-out from this particular device.

$$CG = \&_3 + V_3\&_2 + V_3V_2\&_1 + V_3V_2V_1\&_0$$

Note that neither the CG nor CP outputs are in any way affected by a carry-in signal; they are functions only of the A and B operand inputs.

The CG signal can be turned into a true carry-out if one additional term is added to include a carry-in condition. This term is controlled by the COE pin (carry-out enable). Since carry-out = CG + CP·C_{in}, for the Am9340 CG/CO = CG + CP C_{in} COE.

The internal carry signals for the Am9340 are defined by the following equations (C_0 C_1 C_2 refer to the internal carry signals to the four bits):

$$C_{in} = CG_{-1} + CP_{-1}\,CG_{-2} + CP_{-1}\,CP_{-2}\,CG_{-3}$$

$$C_0 = S_1 + C_{in}$$

$$C_1 = S_1 + (\&_0 + V_0C_{in})$$

$$C_2 = S_1 + (\&_1 + V_1\&_0 + V_1V_0C_{in})$$

$$C_3 = S_1 + (\&_2 + V_2\&_1 + V_2V_1V_0C_{in})$$

$$CP(\text{output}) = V_3V_2V_1V_0$$

$$CG(\text{output}) = (\&_3 + V_3\&_2 + V_3V_2\&_1 + V_3V_2V_1\&_0 + V_3V_2V_1V_0C_{in}COE)$$

FUNCTIONAL CONTROL OF THE Am9340

The S_0 and S_1 inputs control the function of the Am9340 in two ways. First, they determine the particular AND and OR functions produced by the input gating, and second, the S_1 input determines whether or not carries are propagated between the bits in the Am9340.

The functions of the Am9340 are outlined in the table below. Each F_i output is $\overline{\&_i}$ V_i ⊕ $Carry_i$. If S_1 is high, a carry is forced and the function becomes $\overline{\&_i}$ V_i ⊕ 1. The table is for active LOW A, B, and F.

S_0	S_1	&	V	$\overline{\&}$ V ⊕ Carry	Function
L	L	$A\overline{B}$	$A+\overline{B}$	A ⊕ $\overline{B}$ ⊕ Carry	A subtract B
H	L	AB	A+B	A ⊕ B ⊕ Carry	A add B
L	H	$A\overline{B}$	$A+\overline{B}$	A ⊕ $\overline{B}$ ⊕ 1	A ex-OR B
H	H	AB	1	$\overline{AB}$ ⊕ 1	A AND B

TABLE II – FUNCTIONS FOR ACTIVE LOW A, B, & F

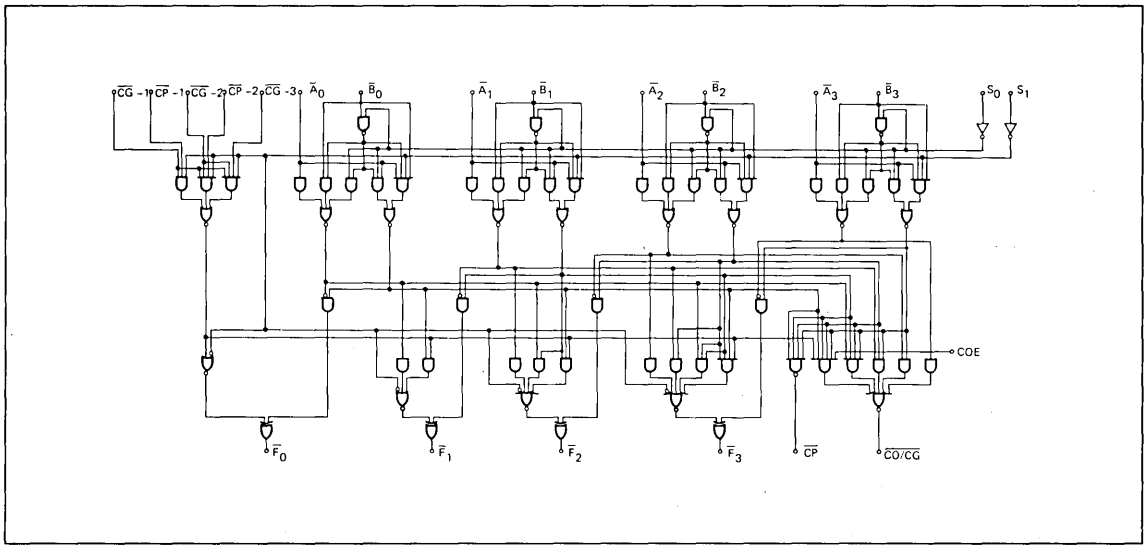


Figure 5. Logic Equivalents of Am9340 ALU

The corresponding function for inputs and outputs of various polarities may be determined by making the required inversion of the variables.

For example, if B is active HIGH and A and F are active LOW, the functions are found by replacing B with $\overline{B}$.

S_0	S_1	$\overline{\&}V \oplus$ Carry	Function
L	L	$A \oplus \overline{\overline{B}} \oplus$ Carry	A add B
H	L	$A \oplus \overline{B} \oplus$ Carry	A subtract B
L	H	$A \oplus \overline{\overline{B}} \oplus 1$	A compare B
H	H	$\overline{A}\,\overline{B} \oplus 1$	A AND $\overline{B}$

TABLE III – FUNCTIONS FOR ACTIVE HIGH B AND ACTIVE LOW A AND F

Similarly, the functions for active HIGH A and B and active HIGH F are found by replacing A and B and Carry in the first table with $\overline{A}$ and $\overline{B}$ and $\overline{\text{Carry}}$ and then inverting the entire function.

S_0	S_1	$\overline{\&}V \oplus$ Carry	Function
L	L	$\overline{A} \oplus \overline{\overline{B}} \oplus \overline{C}\text{arry} = A \oplus B \oplus$ Carry	A subtract B
H	L	$\overline{A} \oplus \overline{B} \oplus \overline{C}\text{arry} = A \oplus \overline{B} \oplus$ Carry	A add B
L	H	$\overline{A} \oplus \overline{\overline{B}} \oplus 1 = \overline{A \oplus \overline{B}} = A \oplus B$	A compare B
H	H	$\overline{A}\overline{B} \oplus 1 = \overline{A + B}$	A OR B

TABLE IV – FUNCTIONS FOR ACTIVE HIGH A, B, AND F

Functions for all useful representations of the Am9340 are shown in Figure 6.

The output signals labeled CG and CP are truly "carry generate" and "carry propagate" only in the active LOW representation. When the operands are active HIGH, the nature of the CG and CP signals changes. The CG output becomes similar to an active HIGH CP, and the CP output becomes similar to an active HIGH CG. It is important to recognize at this point, that an adder is always an adder. Once the carry signals are connected, the polarities of the inputs and outputs of an adder can be changed, but the device is still an adder.

This congruence implies that even though the carry signals from the Am9340 are no longer "carry propagate" and "carry generate", they can be connected to other devices exactly as if they were, and the adder will operate properly. To be accurate, the carry signals have been relabeled CX and CY in the active HIGH case.

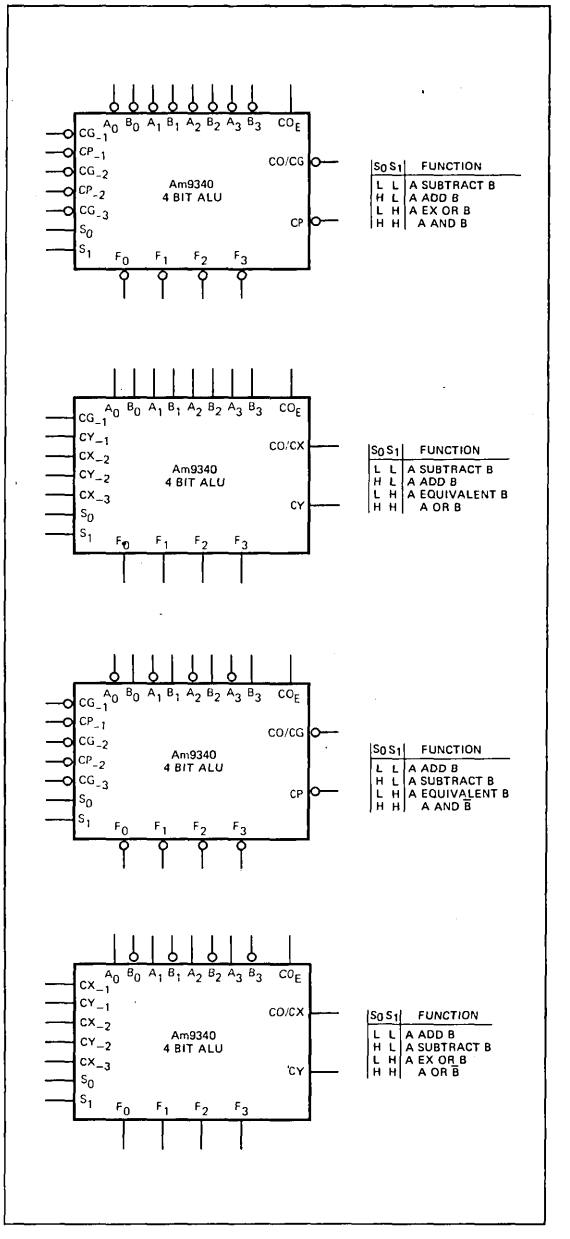


Figure 6. Logic Equivalents of Am9340 ALU

ARITHMETIC USING THE Am9340

The Am9340 can be used to perform arithmetic operations in all three binary signed number representations, including the most complex, sign magnitude. Sign magnitude is complex because when the signs are different and an addition takes place, or when the signs are the same and a subtraction takes place, the absolute magnitude of the difference between the numbers is required. There is also the problem that the sign bit must be handled separately from the rest of the word. Figure 7 shows a sign magnitude 5-bit arithmetic logic unit that uses two Am9340s, one for performing addition and subtraction on the two operands and the other to form the 2s complement of the result, if the result of the previous operation is negative. The scheme can be extended for larger word lengths; unused inputs at the most significant end of the first level of ALUs should have the $\overline{A}$ inputs at ground and the $\overline{B}$ inputs at a high logic level.

Because of these complications, sign magnitude arithmetic is rarely used except where a small amount of processing is involved and the operands are available in the sign magnitude representation. In most systems it is more efficient to work in complement arithmetic and convert to sign magnitude as required.

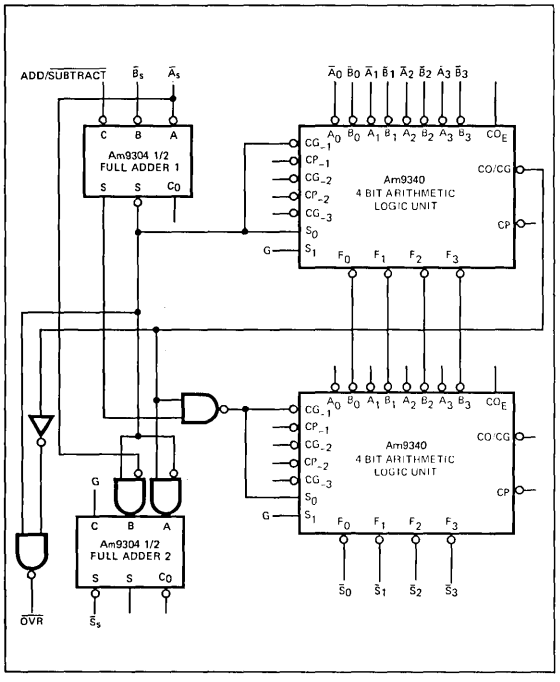


Figure 7. Sign Magnitude Addition and Subtraction

COMPLEMENT ARITHMETIC

Some machines use 1s complement arithmetic because of the apparent simplicity of performing subtraction in this representation. The main disadvantage is that the end-around carry causes extra delay, and only three ALUs can be cascaded in the first section of an ALU using Am9340s. The connections are shown in Figure 8.

The most popular method used in binary machines is 2s complement arithmetic. The sign bit is treated in an identical manner to the rest of the word, and, instead of an end-around carry, a carry-in is immediately forced when a subtraction takes place. This can conveniently be done in an ALU built using Am9340s by connecting the S_0 input to the $\overline{CG}_{-1}$ input of the first ALU in the chain. All applications performing arithmetic will assume that the 2s complement representation is used. The 16-bit arithmetic logic unit in Figure 9 is for numbers represented in the 2s complement notation using active LOW operands; for active HIGH operands the connection is the same except that an inverter must be inserted between the S_0 input and the CX_{-1} line, as shown in Figure 8. Figure 9 also shows how additional blocks of 12 ALU stages can be connected to form ripple-block addition and give very high speed arithmetic over large word lengths with no extra carry circuitry required. Since only two additional gate delays are incurred for each 12-bit increment, and when a separate look-ahead carry package is used, two delays are incurred for each level of look-ahead, the Am9340 is at least as fast as two-level look-ahead for up to 28-bit words.

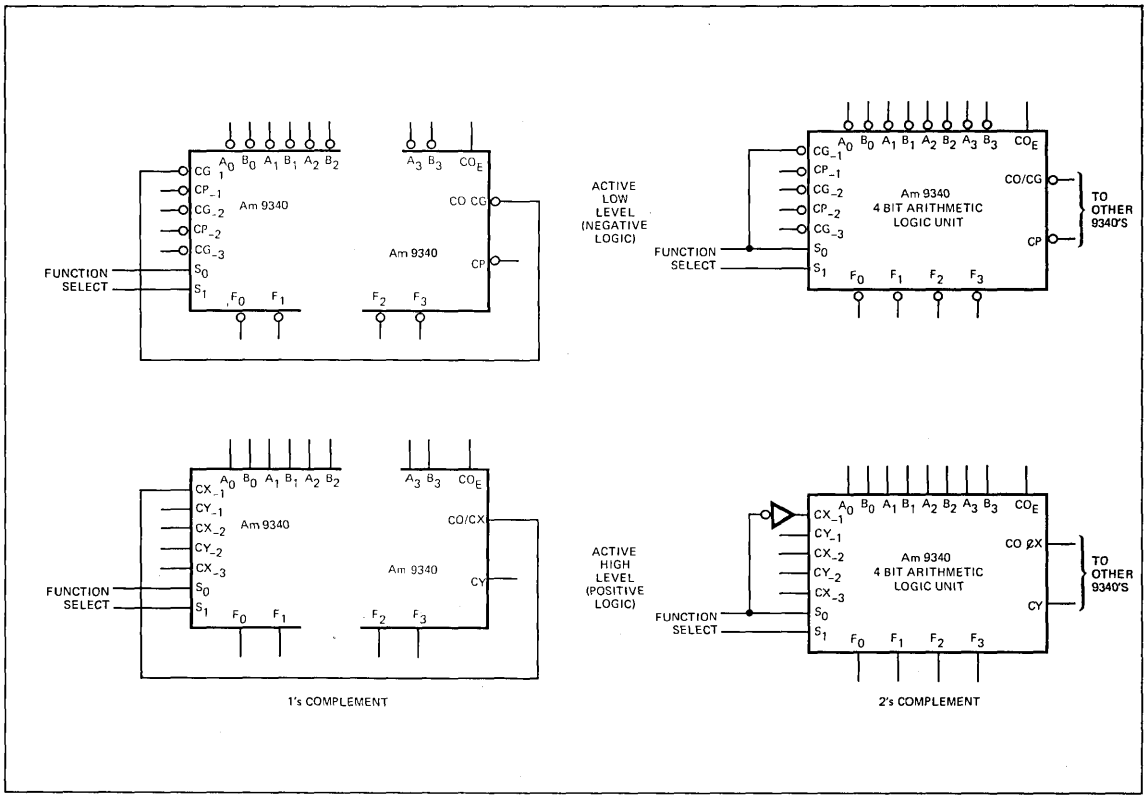
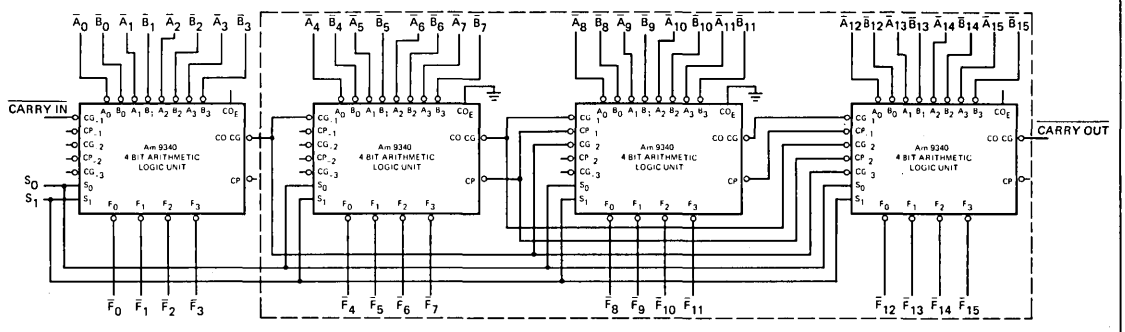


Figure 8. Am9340 Complement Arithmetic



16-Bit Full Look-ahead ALU

Four Am9340 ALU's can be connected together to form a 16-bit full look-ahead ALU. This ALU can work in 1's or 2's complement arithmetic representations and in the active LOW or active HIGH logic representations. If longer word lengths are required 12-bit ALU blocks connected as shown in the dashed portion of the diagram can be cascaded at the end of the 16-bit full look-ahead portion.

TYPICAL DELAY TABLE

WORD LENGTH (in bits)	ADD (in ns)	SUBTRACT (in ns)
1-4	20	25
5-16	34	39
17-28	47	52
29-40	60	65
41-52	73	78
53-64	86	91
65-76	99	104
77-88	114	127
89-100	127	140

Figure 9. 16-Bit Full Look-ahead ALU

SHIFTING OPERATIONS

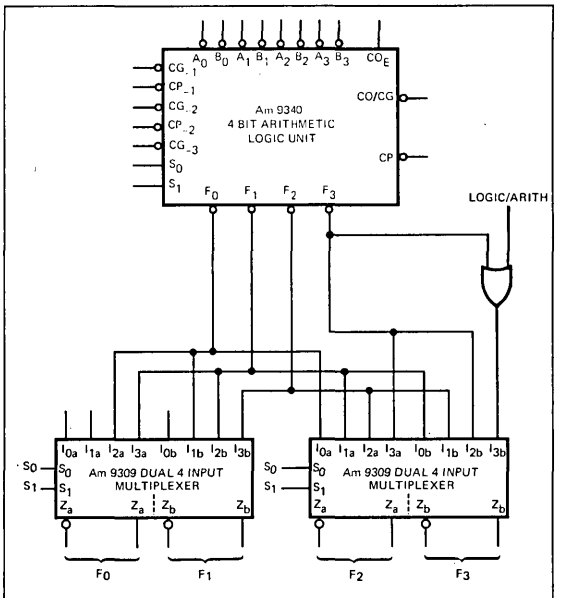
There is no shifting capability built in the Am9340, so if shifting operations are required, they must be provided outside the ALU, either at the input of the ALU, or more likely at the output, so that the result of an arithmetic operation can be shifted. Shifting operations can easily be performed with multiplexers, the select lines of the multiplexer acting as the shift-control lines. A four-input multiplexer has the capability of shifting one place up, pass with no shift, and shift one place down. The spare decode can be used for a variety of purposes, such as no operation or change the subtract operation from A–B to B–A, by inverting the sum outputs and not forcing a carry-in during subtraction to give –(A–B–1) –1 = B–A.

If arithmetic shifts are required, the sign bit must be repeated during a shift up. Logical shifts may pull in logic zeroes or allow recirculation of the data. These differences can be designed in by controlling the least and most significant shift inputs on the multiplexer words. Figure 10 shows a variety of shifting operations using two Am9309 multiplexers at the output of the Am9340.

COMPARISON FUNCTIONS

Magnitude comparison of the inputs to the Am9340 is performed by putting the device in the subtract mode and observing the carry-out signal.

In a 2s complement subtraction (with carry-in active) the function performed is A – B. If the carry-out signal from the sign is inactive, then A is greater than B. If the carry-input is removed, the function performed is A minus B minus 1. If the carry-output is active for this operation, then A is less than B. If neither of these cases is true, then obviously A=B.



SHIFT CODE		FUNCTION
S_0	S_1	
L	L	SHIFT F UP 2 PLACES
H	L	SHIFT F UP 1 PLACE
L	H	PASS (NO SHIFT)
H	H	SHIFT F DOWN 1 PLACE

Figure 10. Shifting Operations Using Multiplexer

It is possible to detect equivalence between A and B by using the carry generate and carry propagate outputs of the Am9340. If A and B are equal, then in the subtract mode or in the EX-OR mode, all the internal V signals will be active and none of the internal & signals will be active. This can be detected at the outputs by the condition

$$\text{Equivalence} = CP \cdot \overline{CG}$$

Equivalence over the entire word can be detected by forming the above function for each Am9340 and then ANDing all the signals.

THE Am54/74181 (Am9341) ARITHMETIC LOGIC UNIT

This ALU is a parallel four-bit MSI device that can perform 16 arithmetic and 16 logic operations on two 4-bit parallel words. The significant arithmetic operations are add, subtract, pass, increment, decrement, invert, and double. All 16 possible logic functions of two variables are available. The operation is selected by four select lines S_0 to S_3 and a mode control line M, which is HIGH for arithmetic operations and LOW for logic operations. The device has a carry-in, a carry-out for ripple-carry cascading of units, and two look-ahead auxiliary carry functions, carry generate and carry propagate for use with the look-ahead carry MSI device, the Am54/74182 (Am9342). An open collector "A=B" output is also provided that can be AND tied to the A=B outputs of other ALUs to detect an all HIGH output condition over several units.

Figure 11 shows the logic diagram of the arithmetic logic unit. Four identical AND, OR networks gate the A and B input operands with the four select lines S_0 to S_3 to produce the required first level auxiliary AND and OR functions, which are then used to generate the sum and carry functions. Internal look-ahead carry is used to give high speed. The A=B output is generated by sensing the all ones condition at the F outputs. When the control M is in the high state, carries are inhibited from propagating and logic functions are generated at the outputs.

The functions that are available with the device form a closed set such that inversion of the logic inputs produces a function which is still in the set. Therefore, the device performs the same logic and arithmetic functions in the active HIGH representation as it does in the active LOW representation, but with a different select code. If a mixed representation is employed, the majority of useful functions are still available. Figure 12 shows the four modes in which the ALU can be used and the operation table for each mode.

Am54/74181 (Am9341) CARRY METHODS

The Am54/74181 (Am9341) ALU can be used in a variety of carry modes. The simplest of these is in a ripple-carry mode where the carry-in C_n of an ALU is driven by the carry-out signal C_{n+4} from the previous ALU. This method of propagating the carry is slow for large word lengths but has the advantage that additional carry circuits are not required; if several levels of look-ahead are permitted and extra logic is used, the speed of the ALU can be improved. The Am54/74181 (Am9341) gives the auxiliary carry functions carry generate and carry propagate which can be used with the Am54/74182 (Am9342) to give complete look-ahead carry or ripple-block look-ahead. In this latter mode the ALU is split into 16-bit blocks, each with its own look-ahead, and carries are allowed to ripple between the blocks.

THE Am54/74182 (Am9342) LOOK-AHEAD CARRY CIRCUIT

The Am54/74181 (Am9341) ALU requires external logic for full look-ahead operation. The Am54/74182 (Am9342) has been specifically designed for this purpose. The device will accept up to four sets of carry generate and carry propagate functions and a carry-in and provide the three carry-outs required by the ALUs and also the next level auxiliary functions. These auxiliary functions generated by the look-ahead carry circuit allow further levels of look-ahead. Unfortunately, to satisfy signal polarities a penalty of two gate delays is incurred for each level of look-ahead, and the auxiliary functions are rarely used over more than two levels of look-ahead.

The logic symbols and logic diagram of the Am54/74182 (Am9342) look-ahead carry circuit are shown in Figures 13 and 14, respectively. The logic auxiliary functions in the active HIGH case are not carry generate and carry propagate, and have been labeled X and Y, respectively. Of course, they are

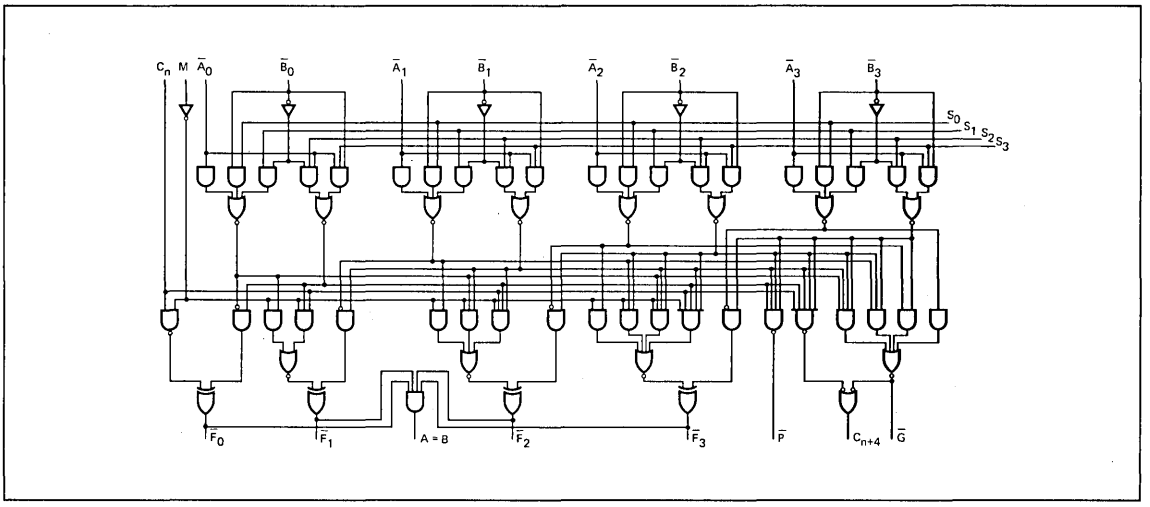
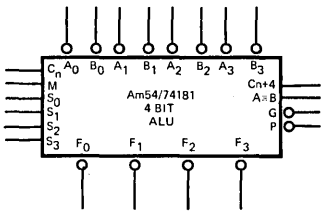
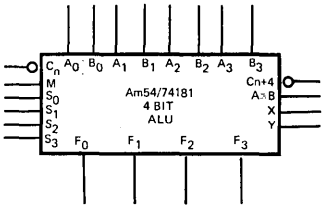


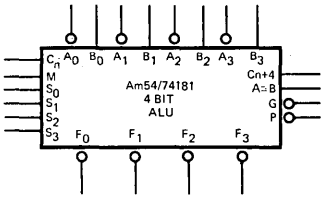
Figure 11. Am54/74181 (Am9341) Logic Diagram



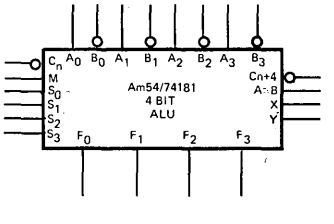
S_0	S_1	S_2	S_3	Arithmetic (M = L, C_n = L)	Logic (M = H)
L	L	L	L	A minus 1	$\overline{A}$
H	L	L	L	AB minus 1	$\overline{AB}$
L	H	L	L	$A\overline{B}$ minus 1	$\overline{A}+B$
H	H	L	L	minus 1 (2's comp.)	Logic '1'
L	L	H	L	A plus $[A+\overline{B}]$	$\overline{A+B}$
H	L	H	L	AB plus $[A+\overline{B}]$	$\overline{B}$
L	H	H	L	A minus B minus 1	$\overline{A \oplus B}$
H	H	H	L	$A+\overline{B}$	$A+\overline{B}$
L	L	L	H	A plus [A + B]	$\overline{AB}$
H	L	L	H	A plus B	$A \oplus B$
L	H	L	H	$A\overline{B}$ plus [A + B]	B
H	H	L	H	A + B	A + B
L	L	H	H	A plus A (2 x A)	Logic '0'
H	L	H	H	A plus AB	$A\overline{B}$
L	H	H	H	A plus $A\overline{B}$	AB
H	H	H	H	A	A



S_0	S_1	S_2	S_3	Arithmetic (M = L, $\overline{C_n}$ = H)	Logic (M = H)
L	L	L	L	A	$\overline{A}$
H	L	L	L	A + B	$\overline{A+B}$
L	H	L	L	$A+\overline{B}$	$\overline{AB}$
H	H	L	L	minus 1 (2's comp.)	Logic '0'
L	L	H	L	A plus $A\overline{B}$	$\overline{AB}$
H	L	H	L	$A\overline{B}$ plus $[A+\overline{B}]$	$\overline{B}$
L	H	H	L	A minus B minus 1	$A \oplus B$
H	H	H	L	$A\overline{B}$ minus 1	$A\overline{B}$
L	L	L	H	A plus $A\overline{B}$	$\overline{A}+B$
H	L	L	H	A plus B	$\overline{A \oplus B}$
L	H	L	H	AB plus $[A+\overline{B}]$	B
H	H	L	H	AB minus 1	AB
L	L	H	H	A plus A (2 x A)	Logic '1'
H	L	H	H	A plus $[A+\overline{B}]$	$A+\overline{B}$
L	H	H	H	A plus [A + B]	A + B
H	H	H	H	A minus 1	A



S_0	S_1	S_2	S_3	Arithmetic (M = L, C_n = L)	Logic (M = H)
L	L	L	L	A minus 1	$\overline{A}$
H	L	L	L	$A\overline{B}$ minus 1	$\overline{A}+B$
L	H	L	L	AB minus 1	$\overline{AB}$
H	H	L	L	minus 1 (2's comp.)	Logic '1'
L	L	H	L	A plus [A + B]	$\overline{AB}$
H	L	H	L	$A\overline{B}$ plus [A + B]	B
L	H	H	L	A plus B	$A \oplus B$
H	H	H	L	$A+\overline{B}$	A + B
L	L	L	H	A plus $[A+\overline{B}]$	$\overline{A+B}$
H	L	L	H	A minus B minus 1	$\overline{A \oplus B}$
L	H	L	H	$A\overline{B}$ plus $[A+\overline{B}]$	$\overline{B}$
H	H	L	H	$A+\overline{B}$	$A+\overline{B}$
L	L	H	H	A plus A (2 x A)	Logic '0'
H	L	H	H	A plus $A\overline{B}$	AB
L	H	H	H	A plus $A\overline{B}$	$A\overline{B}$
H	H	H	H	A	A



S_0	S_1	S_2	S_3	Arithmetic (M = L, $\overline{C_n}$ = H)	Logic (M = H)
L	L	L	L	A	$\overline{A}$
H	L	L	L	$A+\overline{B}$	$\overline{AB}$
L	H	L	L	A + B	$\overline{A+B}$
H	H	L	L	minus 1 (2's comp.)	Logic '0'
L	L	H	L	A plus AB	$\overline{A}+B$
H	L	H	L	AB plus $[A+\overline{B}]$	B
L	H	H	L	A plus B	$A \oplus B$
H	H	H	L	AB minus 1	AB
L	L	L	H	A plus $A\overline{B}$	$A+\overline{B}$
H	L	L	H	A minus B minus 1	$A \oplus B$
L	H	L	H	$A\overline{B}$ plus [A + B]	$\overline{B}$
H	H	L	H	$A\overline{B}$ minus 1	$A\overline{B}$
L	L	H	H	A plus A (2 x A)	Logic '1'
H	L	H	H	A plus $[A+\overline{B}]$	$A+B$
L	H	H	H	A plus [A + B]	$A+\overline{B}$
H	H	H	H	A minus 1	A

Figure 12. Logic Equivalents of Am54/74181 (Am9341) ALU

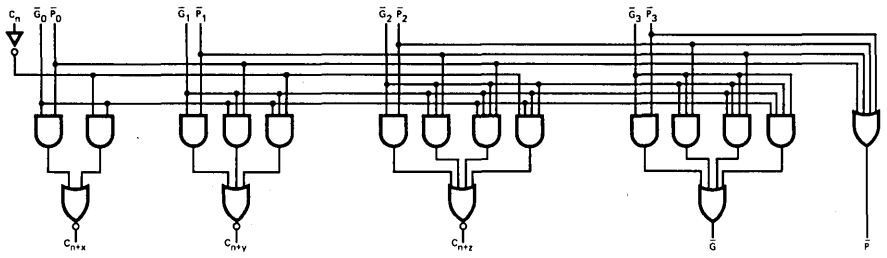


Figure 13. Am54/74182 (Am9342) Logic Diagram

Figure 14. Am54/74182 (Am9342) Logic Symbol

connected the same way as the active LOW case. The logic design is straightforward with the auxiliary functions being used to generate the three carry-out signals and the two auxiliary functions required for further levels of look-ahead.

Figure 15 shows how a single look-ahead carry circuit is used with four Am54/74181 (Am9341) ALUs to perform arithmetic operations with complete look-ahead carry over 16-bit words. If words of less than 32 bits are used, then the ripple-block mode of operation should be used since the delay is the same as for full two-level look-ahead. Figure 16 shows diagrammatically various methods of using the Am54/74182 (Am9342) with ALUs to perform arithmetic operations over large word lengths. Table I gives typical delays to be realized from the various connection methods. The table shows how the use of a small number of look-ahead carry packages considerably decreases the delay for the typical word lengths used in digital systems.

Typical addition times for various configurations are given in the table below. Subtraction times are approximately 5 ns longer.

TYPICAL ADDITION TIMES

No. of Bits	Total Addition Time (ns)	Add Time Per Bit (ns)	Package Count Am54/74181	Package Count Am54/74182
4	19	4.8	1	
8	32	3.9	2	
12	43	3.6	3	
12	32	2.6	3	1
16	55	3.5	4	
16	32	2.0	4	1
32	103	3.2	8	
32	79	2.5	8	1
32	56	1.8	8	2
48	151	3.2	12	
48	127	2.6	12	1
48	104	2.2	12	2
48	81	1.7	12	3
48	57	1.2	12	4
64	199	3.1	16	
64	152	2.4	16	2
64	129	2.0	16	3
64	106	1.7	16	4
64	57	0.9	16	5

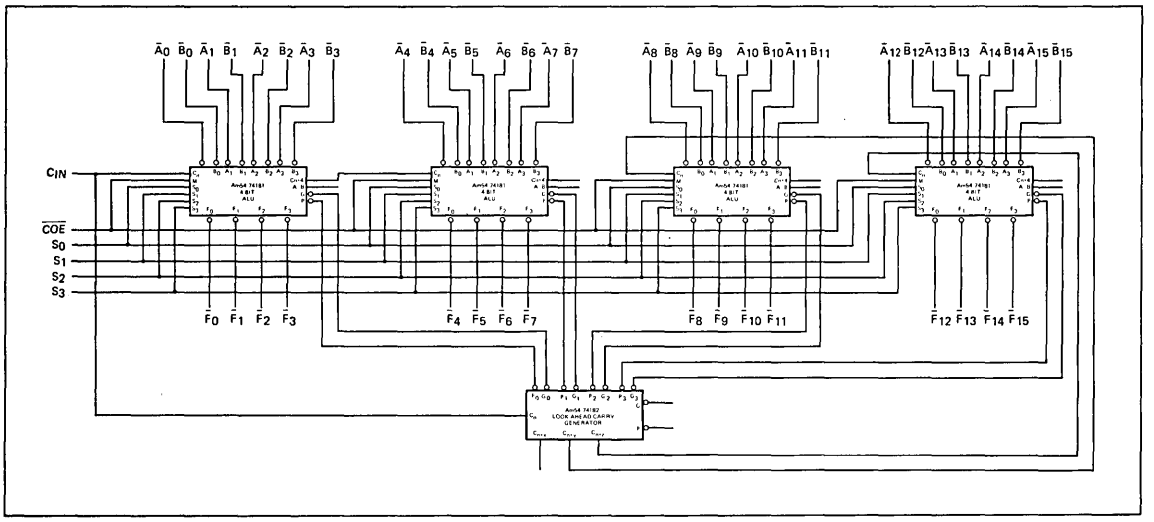
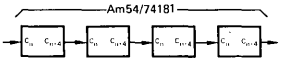
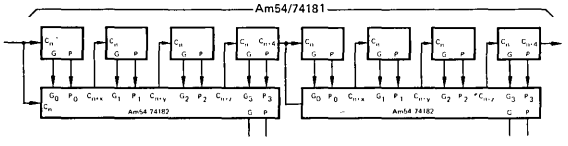


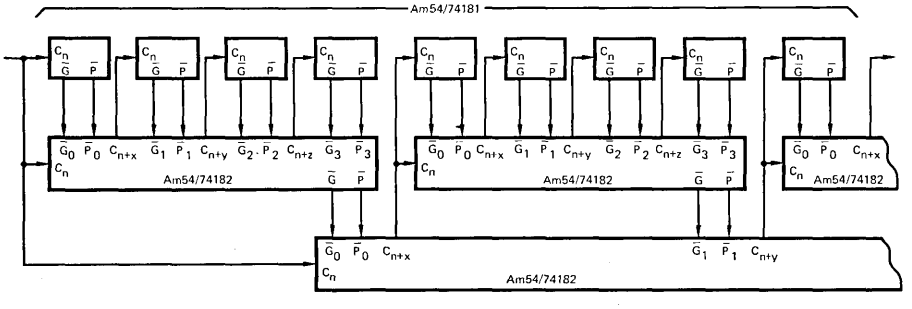
Figure 15. This Figure Illustrates Use of the Am54/74181 (Am9341) ALU and the Am54/74187 (Am9342) Look-Ahead Carry Generator



16-Bit ALU Ripple Carry



32-Bit ALU Two-Level Look-Ahead Over 16-Bit Groups



64-Bit ALU, Three Level Carry Look-Ahead

Figure 16. Am54/74181 (Am9341) Carry Methods

ARITHMETIC WITH THE Am54/74181 (Am9341)

The Am54/74181 (Am9341) can be used as an arithmetic element in all the common binary number representations. Reference is made to the section on the Am9340 for basic concepts. The most difficult number representation is sign magnitude. The Am54/74181 (Am9341) is more flexible than the Am9340 but additional peripheral logic must be used to decode the desired functions that are required by the select lines, and the carry-in at the first stage. The two most useful additional arithmetic operations that the Am54/74181 (Am9341) has as compared to the Am9340 are "double A" and "pass." Both of these operations are extremely useful in multiplication, division and square root routines. It is often possible to use the select code on the ALU to effectively perform additional decoding, for example if a control signal is to select between "add A and B" when S is HIGH and "pass A" when S is LOW, then (for the active HIGH case) S_0 is tied to S_3 to form S and S_1 and S_2 are tied LOW. This type of operation (Add or Pass) is useful in multiplication routines.

COMPARISON FUNCTIONS

Several comparison functions can be performed with the Am54/74181 (Am9341) by using the A=B and the C_{n+4} outputs. The A=B output is better described as "F=0," since this output goes HIGH anytime all the $\overline{F}$ outputs are HIGH. The outputs can therefore be used not only for comparing A=B during a subtract operation but can also be used to ascertain whether the function outputs are all HIGH after any arithmetic or logic operation. In the PASS operation, the output indicates that one of the operands is equal to zero. In the EX-OR operation, it indicates that the two operands are identical. In the EQUIVALENCE operation, it indicates that the two operands are complementary.

For signed arithmetic, with the signs of the operands at the most significant inputs to the ALU, the F output at the sign position can be used during subtraction to indicate the relative value of the two operands. For unsigned numbers, in which the most significant bit is positive, the carry-out of the ALU indicates relative magnitude. The table below lists the various comparison functions which can be performed in active HIGH and active LOW logic.

THE Am2506 ARITHMETIC LOGIC UNIT

After an ALU operation has been performed, the result is usually stored in a register or memory where it can be obtained at a later time for further computation. Arithmetic logic units are therefore frequently followed by latches to temporarily store the result. The Am2506 ALU incorporates these latches internally, thereby giving the user the advantages of higher system speed, lower power and fewer devices. The logic diagram and symbols are shown in Figures 17 and 18, respectively. The Am2506 is functionally identical to the Am54/74181 (Am9341) with the exception that the four F outputs can be stored and the A=B output is replaced by the common latch enable input. The result of an operation is stored in the latches when the common enable is at a LOW logic level. If the latch enable is HIGH or open, the device behaves exactly like an Am54/74181 (Am9341) in all respects, and may be plugged directly into a socket wired for the latter device if the A=B output is not used. The delay through the Am2506, including the latch, is the same as the delay through the Am54/74181 (Am9341) ALU, so that the entire delay of a latch is saved at the system level by the use of the Am2506. The Am2506 can be viewed as an Am54/74181 ALU followed by a four-bit latch which has zero delay and zero power consumption as shown in Figure 19. Because the enable is active HIGH, it can be connected to active LOW enables on external latches or to the active LOW write enable on a memory to obtain a master-slave flip flop operation. Figure 20 shows how the Am2506 can be used with an Am3101 memory to build a high-speed 4-bit arithmetic logic register slice which has sixteen general purpose registers.

Output	State	Operation	Active LOW Logic	Active HIGH Logic
A = B	H	A − B	A = B	A = B−1
	H	A ⊕ B	A = B	A = $\overline{B}$
	H	$\overline{A \oplus B}$	A = $\overline{B}$	A = B
Sign Bit (F_3, active HIGH)	H	A − B	A ≥ B	A < B
	L	A − B	A < B	A ≥ B
($\overline{F}_3$, active LOW)	H	A − B − 1	A > B	A ≤ B
	L	A − B − 1	A ≤ B	A > B
C_{n+4} (unsigned arithmetic only)				
($\overline{C_{n+4}}$, active HIGH)	H	A − B	A ≥ B	A < B
	L	A − B	A < B	A ≥ B
(C_{n+4}, active LOW)	H	A − B − 1	A > B	A ≤ B
	L	A − B − 1	A ≤ B	A > B

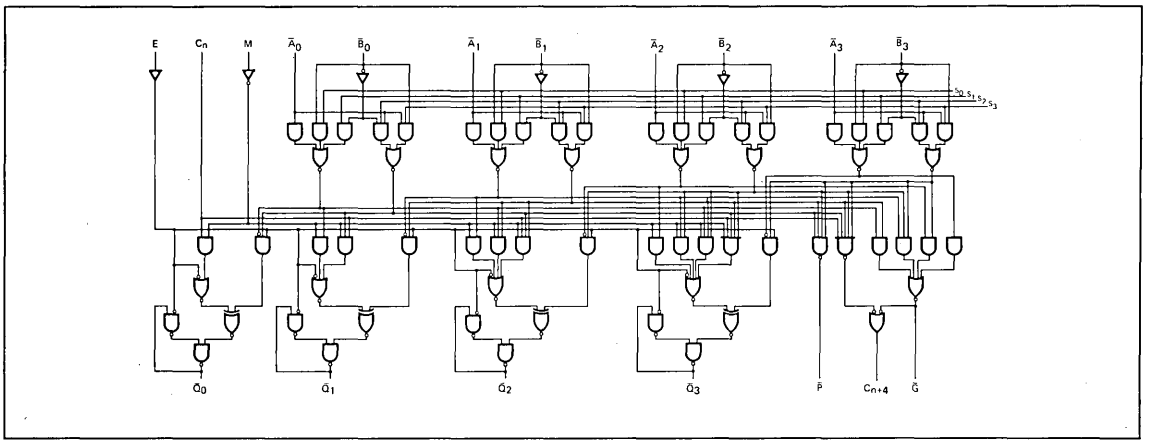


Figure 17. Am2506 ALU With Output Latch Logic Diagram

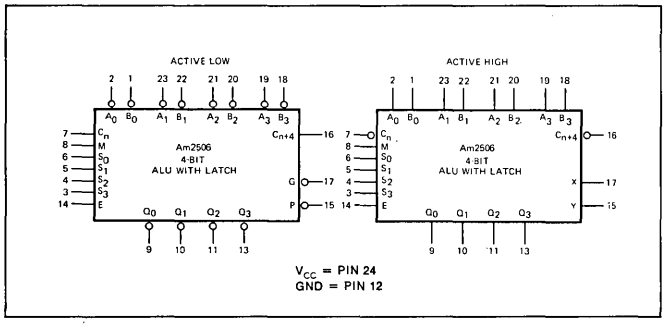


Figure 18. Am2506 Logic Symbols

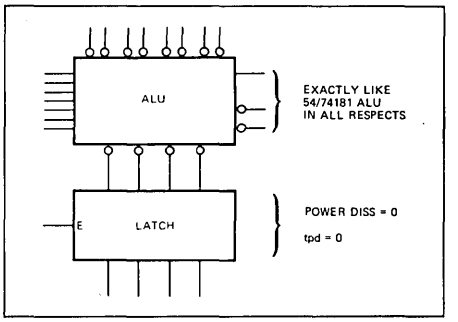
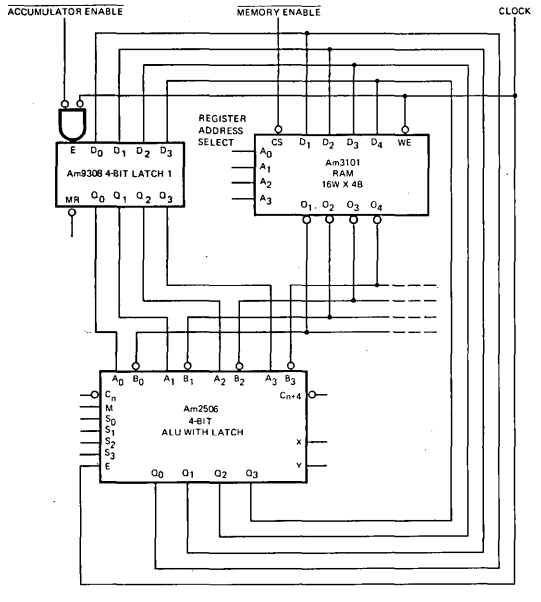


Figure 19. Am2506 Block Diagram



FUNCTION TABLE

S_0	S_1	S_2	S_3	Arithmetic (M = L, $\overline{C_n}$ = H)	Logic (M = H)
L	L	L	L	A	$\overline{A}$
H	L	L	L	$A + \overline{B}$	$\overline{A}B$
L	H	L	L	$A + B$	$\overline{A}\overline{B}$
H	H	L	L	minus 1 (2's comp.)	Logic '0'
L	L	H	L	A plus AB	AB
H	L	H	L	AB plus $[A + \overline{B}]$	B
L	H	H	L	A plus B	$A \oplus \overline{B}$
H	H	H	L	AB minus 1	AB
L	L	L	H	A plus $A\overline{B}$	$\overline{A} + \overline{B}$
H	L	L	H	A minus B minus 1	$A \oplus B$
L	H	L	H	$A\overline{B}$ plus $[A + B]$	$\overline{B}$
H	H	L	H	$A\overline{B}$ minus 1	$A\overline{B}$
L	L	H	H	A plus A (2 x A)	Logic '1'
H	L	H	H	A plus $[A + \overline{B}]$	$A + B$
L	H	H	H	A plus $[A + B]$	$A + \overline{B}$
H	H	H	H	A minus 1	A

L = Low Voltage Level
H = High Voltage Level

Figure 20. 16 Register 4-Bit Arithmetic Logic Register Slice

Another important application of the Am2506 is in very high-speed systems where arithmetic operations such as multiplication are performed in a sequential "pipelined" approach. The system in Figure 21 illustrates one such application, a multiple word adder. The system adds together eight parallel words simultaneously to produce a single sum.

Ordinarily, three levels of adders are required and the final sum appears after the delay of all three levels. Using the Am2506, however, allows synchronization of the data at each level, so that three different problems can be processed simultaneously. While the last 2506 is adding the latched outputs of the second level, the second level is adding the latched outputs of the first level, and the first level is performing the initial addition of four new parts of numbers. A short pulse on the enable pin causes each problem to drop into the next level of adders so that, for a series of additions, the average delay is

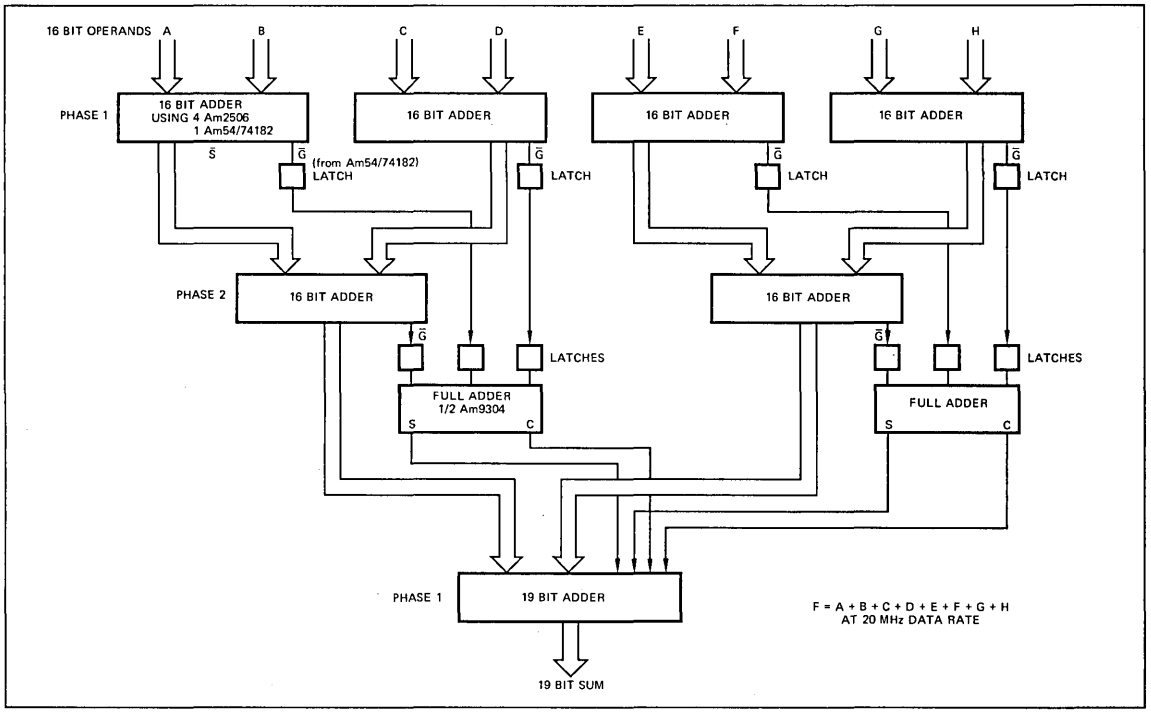


Figure 21. Multiple Word Adder Using Am2506s for Pipelining

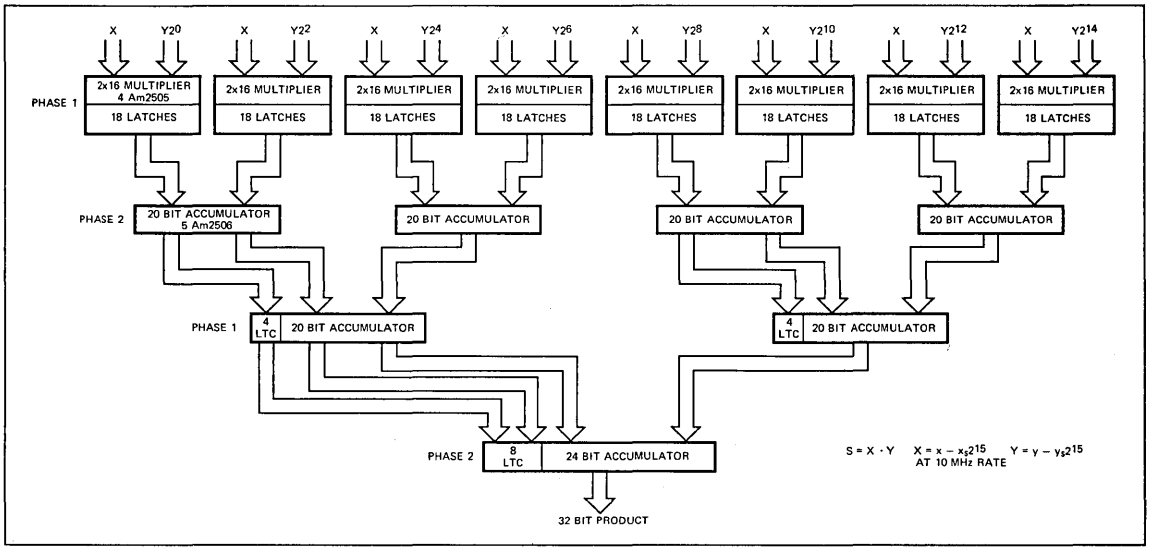


Figure 22. Very High Speed Multiplier Using Am2506s for Pipelining

that of one level of ALUs rather than three levels. Device propagation delays are used to separate the data in extreme cases; otherwise the latch enables at consecutive levels can be driven by complementary signals. Additional latches are used to store the output carries ($\overline{G}$) from the 16-bit adders. Two full adders at the second level and a final 19-bit adder at the third level are used to add in these carries to the final sum.

Figure 22 shows a scheme in which the Am2505 2s complement multiplier is used to perform high-speed multiplication and, to increase speed further, the multiplier array has been split into several smaller independent arrays. The results from the smaller arrays are partial products and are added together using Am2506s. The effective multiplication time is reduced from 275ns. to just 100ns. using this method.

COMPARISON OF ALUs

Selection of an ALU for a particular system depends on the specific requirements of the application. The features of the ALUs are contrasted below. If a simple adder/subtractor is required, then the Am9340 is the best product to use because it has built-in look-ahead for speed, and allows Add/Subtract control with a single line. For a high-speed minicomputer, the best product is the Am2506, since it can perform a large variety of functions and the output can be stored with no speed penalty, thereby allowing a higher system clock rate.

Figure 23 compares the add time of the ALUs using various methods of carry propagation in the case of the devices requiring external look-ahead packages for full look-ahead operation. Line A shows the Am54/74181 (Am9341) and Am2506 used

Device	Function		Speed	Storage	Key Points
Am9340	Add Subtract		34ns for 16-bit words	No	Built-in look-ahead carry to give complete two-level look-ahead over 16 bits
	EX OR AND		20ns		Fastest ALU for word lengths of 20 - 28 bits
Am54/74181 Am9341	Add Subtract Double Pass	Increment Decrement Do Nothing	32ns for 16-bit words with Am54/74182 (Am9342) look-ahead carry	No	Requires additional logic for full look-ahead Provides wide variety of arithmetic and logic functions
	All logic functions				
	Detection of all HIGH outputs		20ns		
Am2506	Add Subtract Double Pass	Increment Decrement Do Nothing	34ns for 16-bit words with Am54/74182 (Am9342) look-ahead carry	Yes	Plug-in replacement for Am54/74181 with output storage and no loss of speed
	All logic functions		20ns		

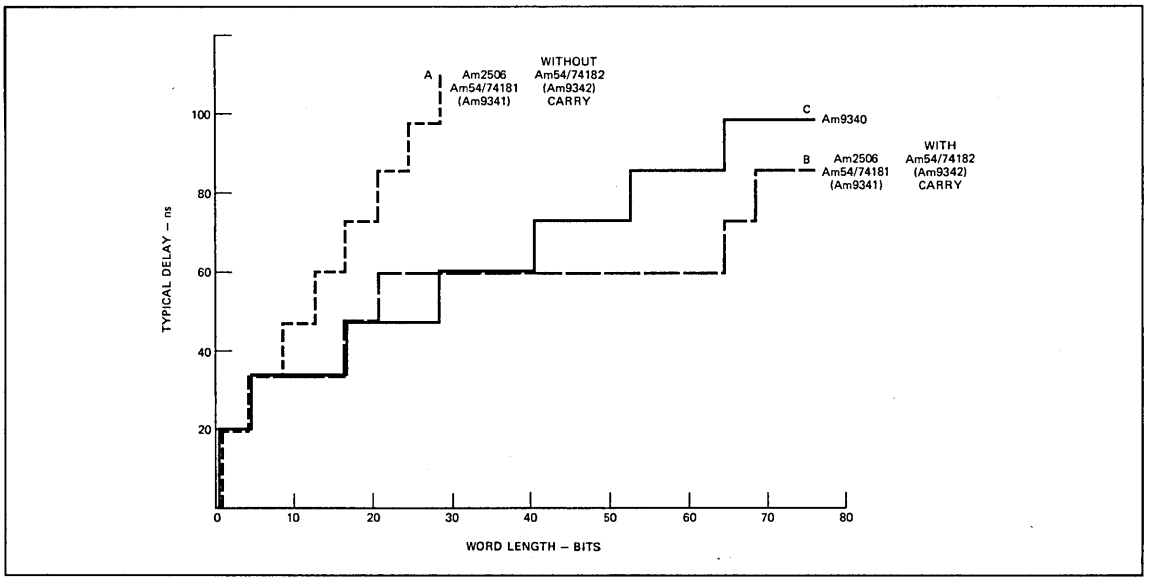


Figure 23. ALU Speed Comparison

in a ripple-carry mode; each increment of four bits essentially introduces a delay of 13ns. This is acceptable for short-word lengths but is excessive for long words. Line B shows the substantial speed improvement possible with full look-ahead.

At the first level of look-ahead (over 16 bits) the delay is 34ns., the next level of look-ahead covers 64 bits and an additional delay of 13ns. is incurred. The small discontinuities in the curve between 16 and 20 bits and between 64 and 68 bits appear because the last ALU is appended to the full look-ahead system, with its carry-in driven from the carry-output of the previous adder block, the carry is rippled into the last adder from the output of the full look-ahead scheme, and the delay is less than that for a complete additional level of look-ahead. Line C shows that speed of the Am9340 adder; the built-in look-ahead carry allows a look-ahead increment of 12 bits. Note that the Am9340 allows faster addition than the Am54/74181 (Am9341) for word lengths between 20 and 28 bits, and has the added advantage that carry packages are not required.

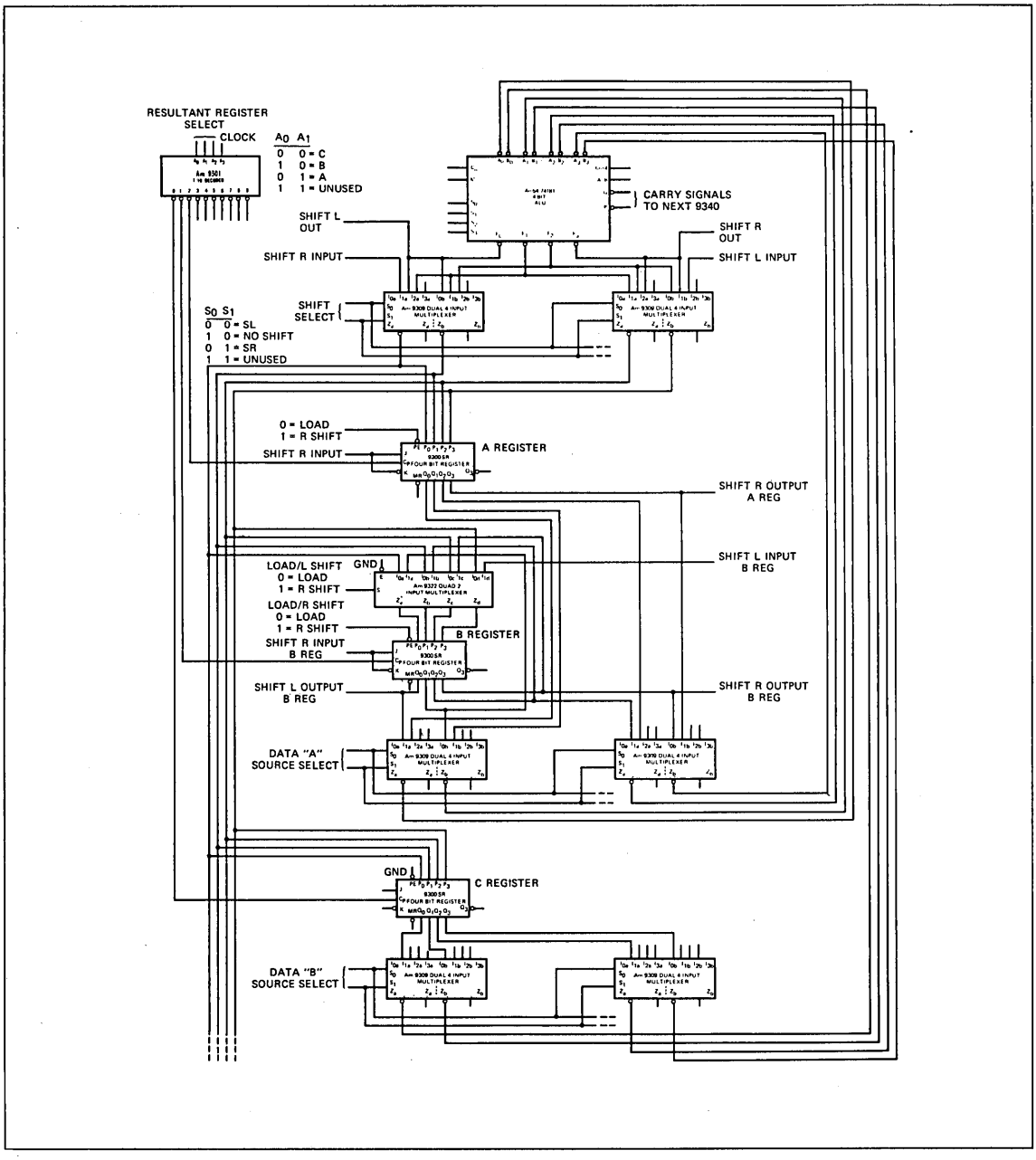


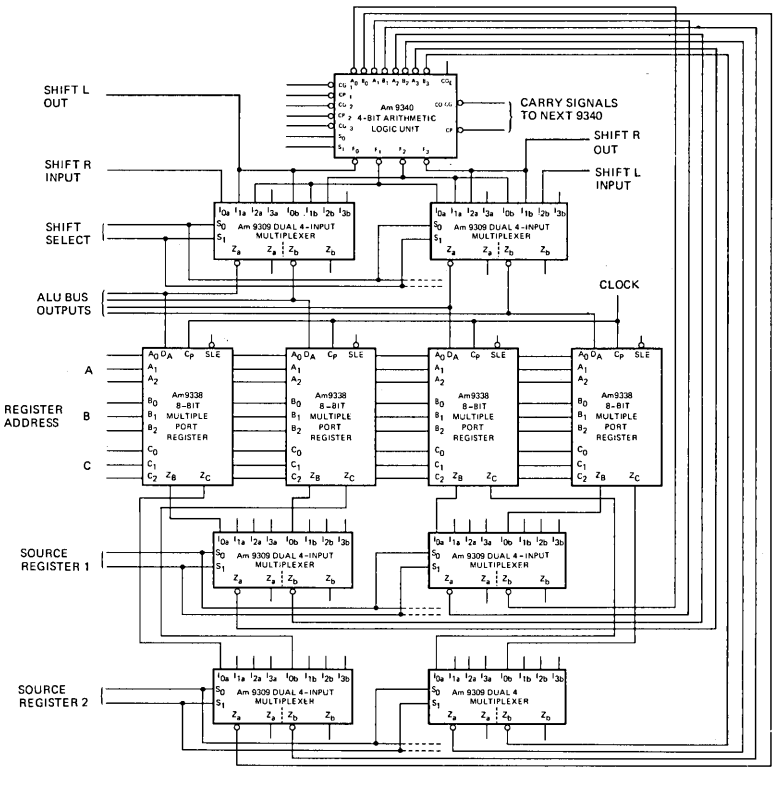
Figure 24. Single Address Arithmetic Register 4-Bit Slice

APPLICATIONS USING ALUs

The ALUs described previously can all be used as the arithmetic logic element in high-speed digital computers. For a simple machine with limited arithmetic and logic capabilities, the Am9340 is often used together with storage registers and multiplexers for shifting and bussing information to the ALU. Figure 24 shows a four-bit arithmetic logic slice of a single address computer with three working registers. Register A is the main working register that is used together with the main store, register B is a temporary register, which can be used in conjunction with register A to allow double-length operation. Register C is required for multiplication and division routines; this register would hold the divisor in division and the multiplicand in a multiply operation. If the Am2506 is used instead of the Am9340, not only is the function capability increased, but register A can be replaced with a high-speed semiconductor scratchpad memory, producing a very powerful two-address system.

If a three-address system is required for a very flexible high-speed machine, the three working registers can be replaced by the Am9338 multiple-port register as shown in Figure 25. This three-address system has distinct advantages over other methods since logic power and speed are increased even though the system uses fewer parts and is more modular than either the two or single-address systems. Three addresses are required, two for the source operands and one for the result.

The unit can perform arithmetic, shifting and logical operations in a 3-address format. Multiplication is performed by dividing the register system into odd and even addresses and placing the portion of the partial product which may have to be added to the multiplicand in the even part and the partial product half which does not need any further computation in the odd part. The double-length product will be contained in locations A and A+1 in the register system, where A is an even address. In division, the dividend must be in a double-length register, with the most significant half in odd register address. The remainder is left in the even address with the result



A typical three address arithmetic register system where two operands can be taken from any two registers, operated upon, and the result written in to any register in the system.

Figure 25. Three Address Arithmetic Register 4-Bit Slice

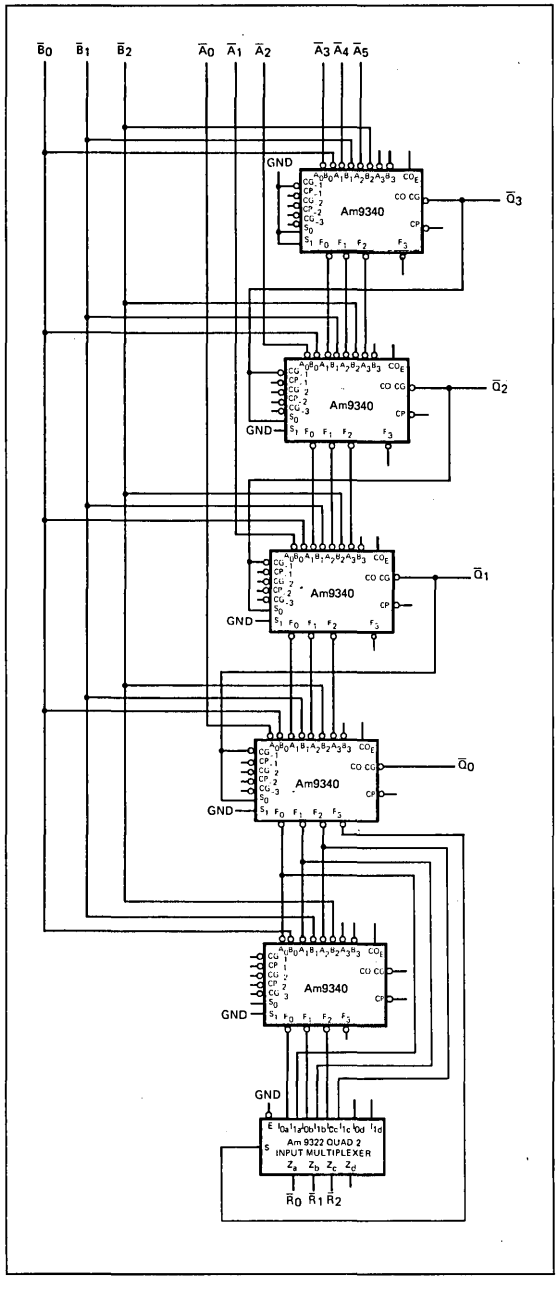


Figure 26 Iterative Unsigned Division

formed in the odd address. In this system fractional division is assumed but integer arithmetic could also be performed by changing interconnections. The Am9309 multiplexers in the design allow data from peripheral and storage devices to be sent to the ALU.

While arithmetic logic units are obviously important in the arithmetic and logic section of digital computers, the low cost of these devices makes them very attractive for use in special purpose digital processors such as FFT Processors and digital filters. Here the ALUs are hard wired to perform special purpose arithmetic such as iterative multiplication, division, square root and polynomial evaluation. There is a continual emphasis on speed as more and more systems are converted from analog to digital methods and process in real time. Therefore the conventional time sequenced approaches to complex arithmetic problems are too slow, and combinatorial hard-wired methods are used. These applications use large quantities of arithmetic elements, but allow straightforward high-speed designs to be implemented easily. A typical example is the non-restoring iterative division scheme shown in Figure 26.

Each level of ALUs subtracts or adds the divisor from the dividend and the carry from the operation gives the quotation digit. At the completion of the division, the remainder may have to be corrected by adding the divisor to the remainder so that the remainder stays positive. The diagram can be extended in the X and Y directions by using additional Am9340 devices.

THE Am9338 MULTIPLE PORT MEMORY

By R. C. Ghest, Digital Applications

The significant advantage of MSI circuits is that they are complete logic sub-systems produced in monolithic form at a fraction of the cost, with a substantial increase in reliability, and increased operational speed over the system produced with discrete integrated circuits. The Am9338 Multiple Port Memory is an excellent example, since, although it is packaged in a 16-pin package, it replaces five 16-pin simpler integrated circuits. Previous methods of building such logically powerful and complex sub-systems were so costly that until recently multiple port memories were considered for use only in the fastest military or special-purpose processors.

This type of memory allows several operations to occur concurrently with a corresponding increase in system speed. In its most flexible form the multiple port memory allows information to be read from two separate locations, with a simultaneous writing operation at a third location. This three-address memory system allows two pieces of data to be read from the memory, operated upon, and the result of the operation written back into the memory, all in one clock cycle. A beneficial side-effect of this type of memory organization is that it produces a neat, efficient design, where the indexing and temporary storage registers can be part of the high-speed working store, with a corresponding increase in flexibility, fewer interconnections and an increase in performance.

The Am9338 is an 8-word by 1-bit three-address memory where two of the addresses are read addresses and the third is

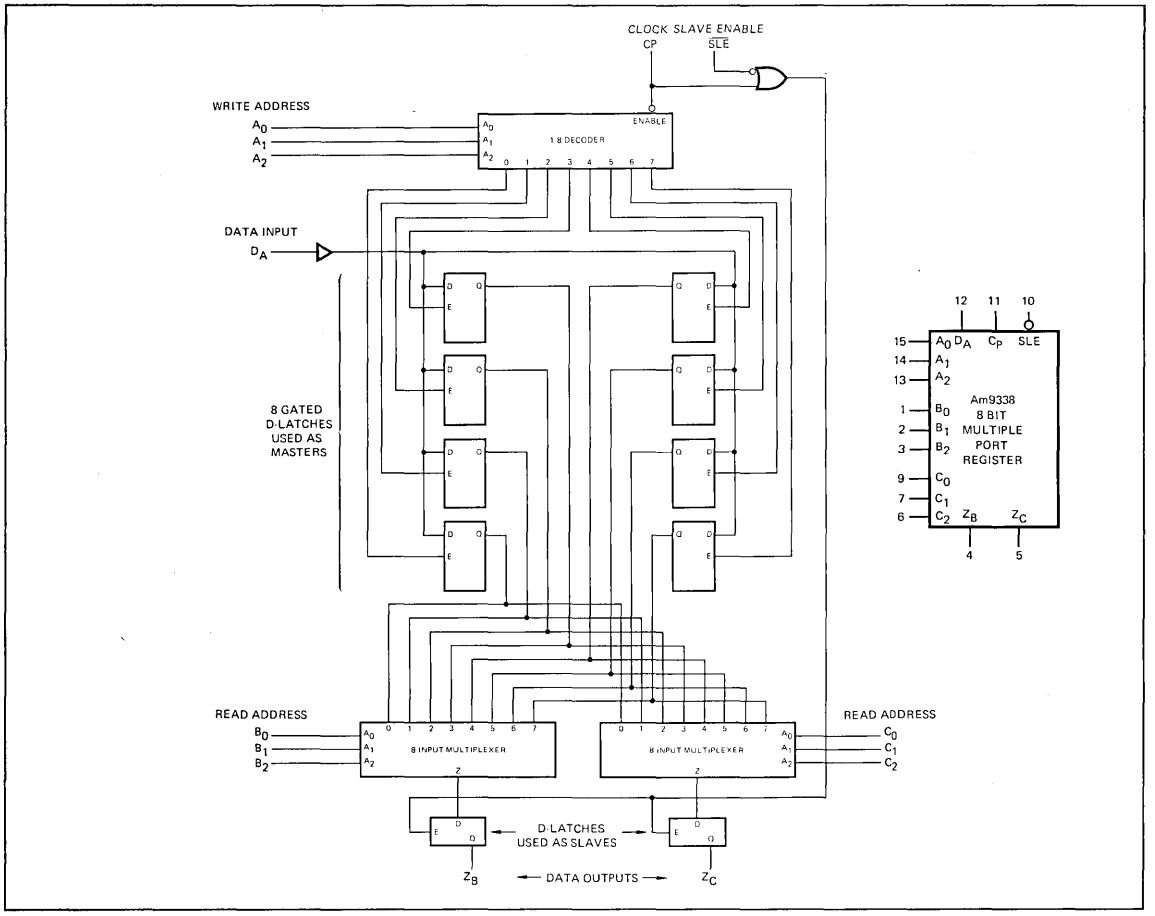


Figure 1. Logic Block Equivalent and Logic Symbol of the Am9338

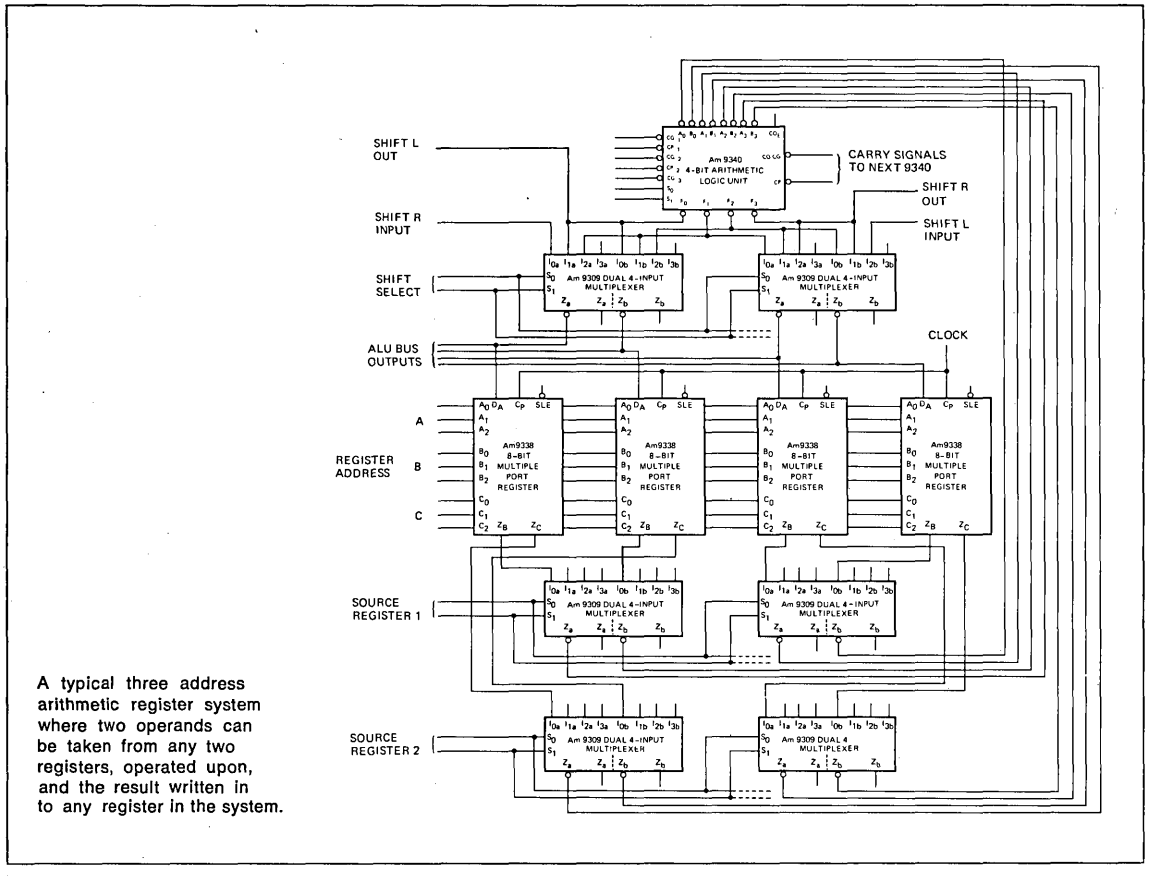
a write address. The write address is a 3-bit address field A, and the read addresses two 3-bit fields B and C. All three fields can be used simultaneously and each field can address any one of the eight memory words. A single data input line and two data output lines are provided; the remaining two logic pins are used for timing, and are the memory clock input, and a clock control called slave enable. A normal memory sequence for the Am9338 is as follows: with the clock HIGH, data from the two locations specified by the two read address fields is read out on the data outputs. This data can be operated upon by external logic, such as the Am54/74181 or Am9340 arithmetic logic units, and the result of the operation is presented back to the data input of the memory and written into the location specified by the A address field when the memory clock is low. Thus in one clock cycle two read operations and a write operation are performed. The memory appears to the user as eight D master-slave flip-flops with a common clock and common data input, and with two 8-input multiplexers on the output of the D flip-flops. The device actually consists of two banks of D latches; one bank is eight master latches that store the data on the data input in the master specified by the A address field when the clock goes low, and the other bank consists of two slave D latches that store the data from the two master latches designated by the B and C address fields when the clock goes high. Since D latches are used no 1s or 0s catching is possible and the only timing considerations of importance are the data in and address set-up times, and the minimum clock pulse width.

If the slave enable is held low the slave latches are continuously enabled and the contents of the eight master latches can be scanned by the B and C address fields. This feature is useful in certain applications, such as peripheral control. The Equivalent Logic Block diagram and Logic Symbol are shown in Figure 1.

The memory can be expanded in word length by commoning address fields and clock inputs of memories, and can be expanded in the number of words by using multiplexers at the data outputs, and a demultiplexer on the clock inputs.

APPLICATIONS

The most straightforward application is as the working store for high-speed 3-address computers. Use of the Am9338 in a computer enables the processing rate to be typically doubled as compared to a machine using a single-address scratchpad memory. A typical 3-address arithmetic register 4-bit slice of a computer using the Am9338 and Am9340 is shown in Figure 2.



A typical three address arithmetic register system where two operands can be taken from any two registers, operated upon, and the result written in to any register in the system.

Figure 2. Three Address 4-Bit Arithmetic Logic Register Slice

Data defined by the B and C address fields is switched through multiplexers onto two 4-bit parallel busses. The data is then operated upon in parallel by the Am9340 high-speed Arithmetic Logic Unit. The ALU has the function select lines set to the configuration required for the desired arithmetic or logic operation, and the result of this operation is presented to a multiplexer so that it can be shifted up one place (multiplied by two), shifted down one place (divided by two), or pass unmodified. The result, after passing through the multiplexer, is presented at the multi-port memory data inputs and written into the location specified by the A address field during the time the clock is LOW.

The operation this 4-bit arithmetic register slice performs is:

A′ = f(B, C) where A′ is the result address
B, and C the two operand addresses
and f is the function performed on
the operands.

The addresses A, B, and C can refer to any of the eight registers in the memory. A typical operation might be: Take the data in register 1, add it to the data in register 1, shift the result up 1 place and write the final result into register 1. The operation replaces the data in register 1 by itself multiplied by four. The complete operation takes only one clock time as compared to a single address system which would take 2 clock times.

The Am9338 in a First In First Out (FIFO) memory is shown in Figure 3. The FIFO memory is used in systems which require an asynchronous buffer; a memory in which information can be written in at one rate and read out completely independently at a different rate. A typical application would be in a high speed digital communication multiplexer where data from many different sources operating at different rates is sorted, tagged and stored ready for transmission over a high-speed communication link.

The write address field is driven from a write address counter and the B read address field from a read address counter. Information is written into the memory at the location specified by the write address counter on receipt of a write clock pulse, and the write address counter is incremented ready for the next data word. Information is therefore stored in ascending address sequence as it is received. Reading takes place completely independently of the write operation with the data word specified by the read address counter available at the Z_B outputs. On receipt of a read clock pulse the read address counter is incremented, ready for the next read operation. The Slave Enable ($\overline{SLE}$) of the memory is held LOW so that the reading operation is completely independent of the write operation, and the contents of the master latches are directly available at the data outputs.

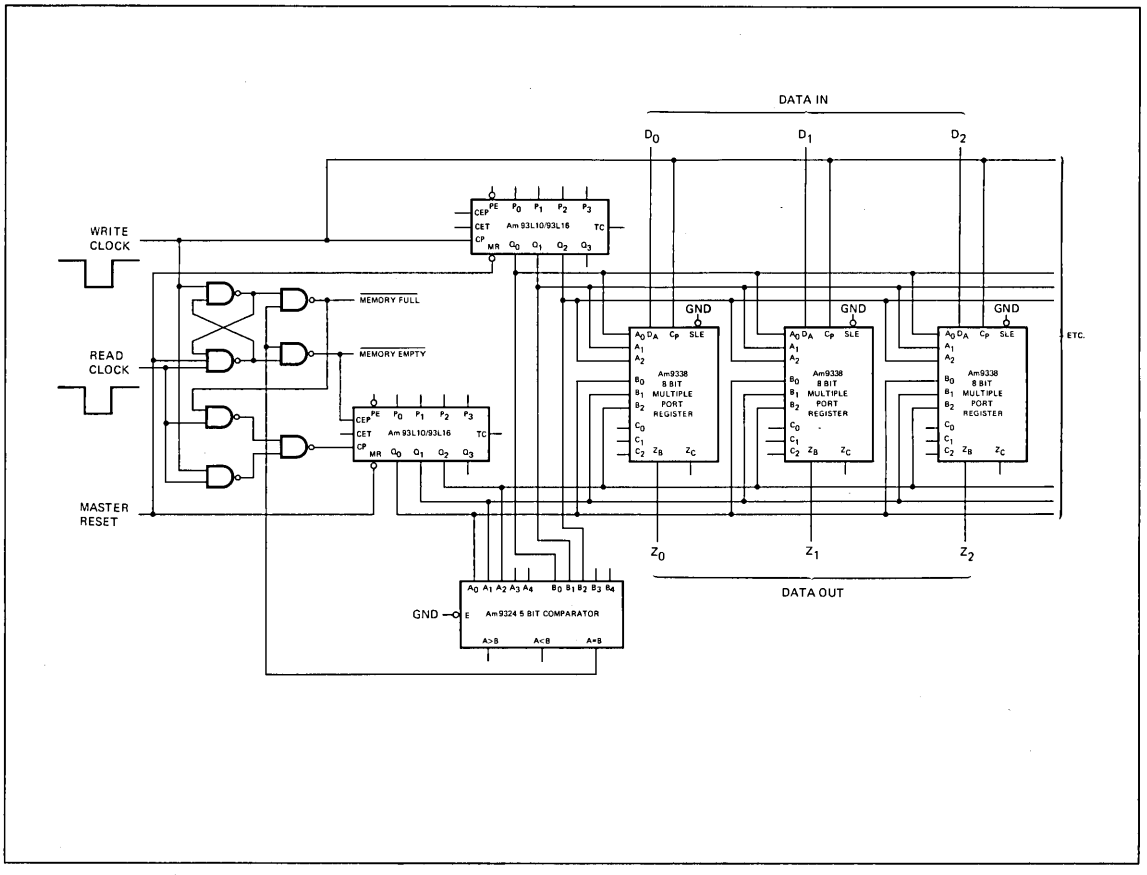


Figure 3. First In First Out Memory

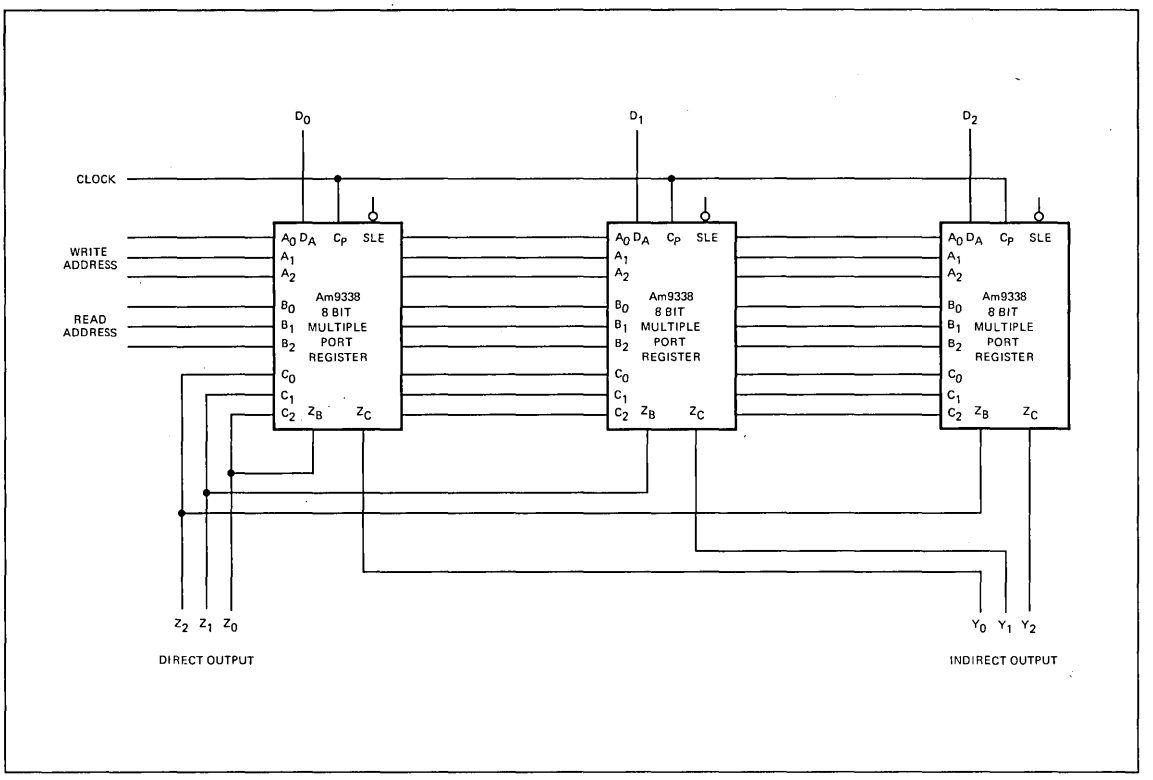


Figure 4. Direct Address/Indirect Address Memory System

Since there can be more read requests than there is data stored, and because the memory has a finite size, two problems occur. First, the memory can be empty, and read requests must be ignored until further information has been written into the memory; and second, the memory can be full and further write operations will overwrite unread data. This memory full condition must not only produce a write operation on receipt of new data, but also increment the read address counter so as to keep it in step. Both the memory empty and memory full conditions occur when the write address counter is identical to the read address counter. This condition is monitored by an Am9324 comparator, and if the read counter has caught up with the write counter further read requests do not increment the read address counter. If the write counter has caught up with the read counter then not only is the write request obeyed but the read address counter is also incremented.

An unusual application of the Am9338 is shown in Figure 4. Information held in this memory system can be addressed directly or indirectly. Directly addressed data is obtained by having the direct address at the B address field. The data then appears at the Z_B outputs. If the data is to be indirectly addressed, then the indirect address is applied to the B address field, the direct address appears at the Z_B outputs, and is fed back to the C address field, so that the required data appears at the Z_C outputs. Information, whether directly or indirectly addressed, can be obtained in one clock cycle. The scheme is shown for an 8-word 3-bits per word memory and can be extended by the use of additional Am9338's and multiplexers.

A SUCCESSIVE APPROXIMATION REGISTER

By R. C. Ghest, Digital Applications

INTRODUCTION

As more systems use digital methods of signal processing and display there is a growing requirement for high-speed, low-cost analog-to-digital converters to provide an interface with the analog world. The Am2502/3/4 TTL/MSI Successive Approximation Registers make the high-speed successive approximation method of conversion cost competitive with slower counting techniques.

The Am2502/3 are high-speed TTL special purpose registers that contain all the storage and digital control for an 8-bit successive approximation analog-to-digital converter. Packaged in 16-pin packages, they offer a considerable increase in reliability, and decrease in power and cost over the 10 or 12 packages now used to accomplish successive approximation conversion.

The Am2503 differs from the Am2502 in that an enable input for register expansion purposes is available in place of a serial data output.

The 12-bit version of the register, the Am2504, has both an enable input and a serial data output and is available in a 24-pin package. These three special-purpose registers can be used not only for analog-to-digital conversion, but also as serial-to-parallel converters, sequencers, ring counters and trial registers in recursive arithmetic routines.

The registers are also available in low-power versions: the Am25L02, Am25L03 and Am25L04. These low-power circuits consume only 1/3 the power of the standard circuits, but still perform at 40 per cent of the speed, and drive up to three standard TTL loads. In all other respects they are identical to the standard power devices.

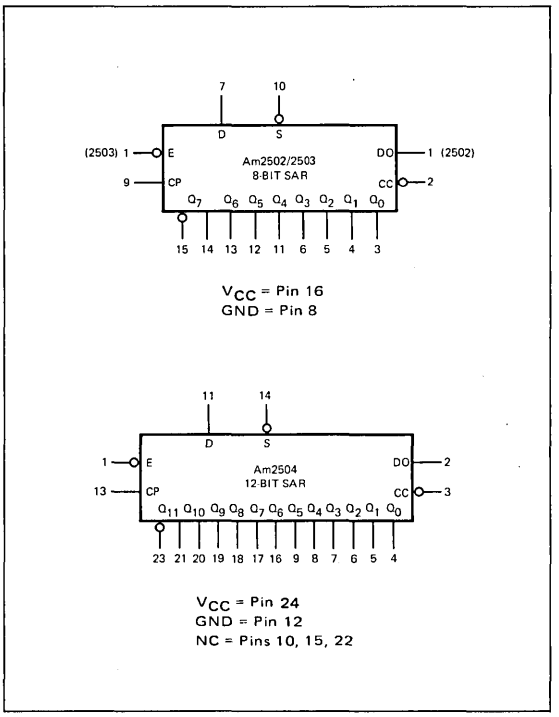


Figure 1. Successive Approximation Register Logic Symbols

FUNCTIONAL OPERATION

The logic symbols and pin numbers of the registers are shown in Figure 1. Each device is a special-purpose serial-to-parallel converter with a single line serial data input (D) and 8 (12 in the case of the Am2504) parallel data outputs. Both true and complement of the most significant bit are brought out to facilitate signed conversion. The register is driven by a single-phase TTL clock, and the register outputs change state synchronously on the LOW-to-HIGH transition of the clock.

Each device has a START input that, when LOW, causes the register to reset synchronously on the clock LOW-to-HIGH transition to a state with the most significant bit $Q_7(11)$ LOW and the remaining outputs HIGH. The conversion complete signal ($\overline{CC}$) will also go HIGH. The register remains in this reset state independent of clock transitions until the START input is moved HIGH. When the START signal goes HIGH, then on the next clock LOW-to-HIGH transition data on the serial data input enters $Q_7(11)$ and the next less significant register stage, $Q_6(10)$, is set to a LOW. The next LOW-to-HIGH transition on the clock puts the data on the data input into the $Q_6(10)$ register stage, and resets stage $Q_5(9)$ to a LOW, while the data in the $Q_7(11)$ stage remains unchanged. After each clock period the serial data moves into the next less significant stage and, at the same time, the stage below that goes LOW. This procedure is repeated for seven clock periods for the Am2502/3, and eleven for the Am2504. At the same time that the Q_0 register stage accepts data from the data input, the conversion complete flip-flop is set to a LOW.

The register is now in a completed state holding the serial train of input data, with the first bit of the serial train in the most significant register stage $Q_7(11)$ and the last data bit of the train in Q_0. Further clock transitions or data changes do not affect the state of the register. The register can now change state only by having a LOW on the $\overline{S}$ (START) input, which synchronously resets the register and reactivates the serial-to-parallel action. The truth table for the Am2502/3 is shown in Figure 2. The left side shows the input pattern at clock period n, and the right the resulting register state.

The registers can be made to operate in a START-CONVERSION-COMPLETE mode by having external circuitry produce a START signal to initiate conversion, and having the conversion complete flip-flop indicate to the system that the conversion has been performed and that the result of the operation is available in parallel from the register. The registers

Time	Inputs			Outputs									
t_n	P	$\overline{S}$	$\overline{E}$	D_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	$\overline{CC}$
0	X	L	L	X	X	X	X	X	X	X	X	X	X
1	D_7	H	L	X	L	H	H	H	H	H	H	H	H
2	D_6	H	L	D_7	D_7	L	H	H	H	H	H	H	H
3	D_5	H	L	D_6	D_7	D_6	L	H	H	H	H	H	H
4	D_4	H	L	D_5	D_7	D_6	D_5	L	H	H	H	H	H
5	D_3	H	L	D_4	D_7	D_6	D_5	D_4	L	H	H	H	H
6	D_2	H	L	D_3	D_7	D_6	D_5	D_4	D_3	L	H	H	H
7	D_1	H	L	D_2	D_7	D_6	D_5	D_4	D_3	D_2	L	H	H
8	D_0	H	L	D_1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	L	H
9	X	H	L	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
10	X	X	L	X	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
NC = No Change

Note: Truth Table for Am2504 is extended to include 12 outputs.

Figure 2. Am2502/3 Truth Table

will work in a continual conversion mode when the conversion complete output ($\overline{CC}$) is fed back to the START ($\overline{S}$) input. The register then automatically restarts ready for another conversion on the clock following conversion complete.

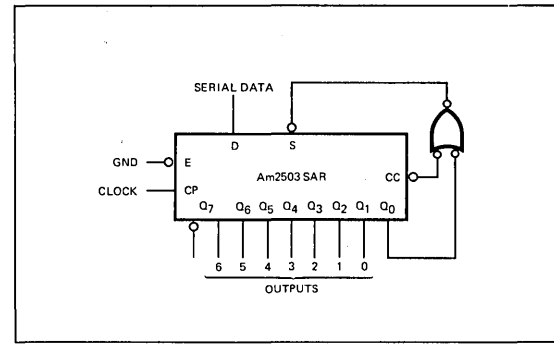


Figure 3. Truncation 7-Bit Continuous Conversion Register

A complete conversion takes nine clock pulses for the Am2502/3 and thirteen for the Am2504. One clock pulse is required for the initial reset condition, the remainder for the serial-to-parallel conversion. If a shorter register is required, one of the register outputs can be used to indicate the end of conversion, and can also be used as the feedback control signal to start the register for a continuous conversion. This register truncation is shown in Figure 3. The OR function is included to remove a possible lock-up condition.

Am2503 and Am2504 registers can be cascaded for expansion so that two Am2503 registers can form a 16-bit successive approximation register. The conversion complete of the more significant device is connected to the enable input of the next less significant device. The respective data, start and clock inputs are tied together. When the START signal goes LOW, then on the next clock all the registers are reset, but when the $\overline{CC}$ signal of the first register goes HIGH the most significant bit of the second register is forced HIGH via the enable connection. The second register will remain in the all HIGH state until its enable input goes LOW. When the enable goes LOW, the Q_7(11) output immediately goes LOW and conversion continues in the second device. The expansion of successive approximation registers is shown in Figure 4.

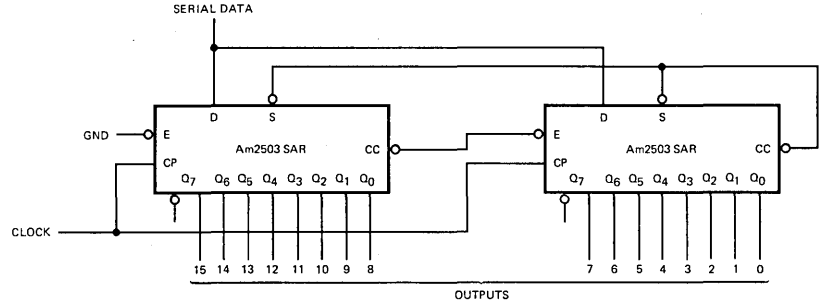
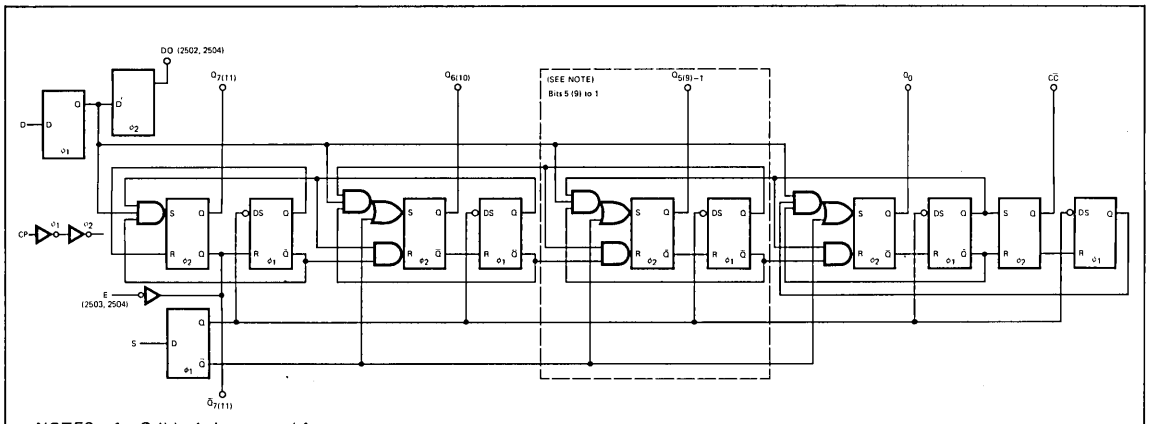


Figure 4. Expansion 16-Bit Continuous Conversion Register



NOTES: 1. Cell logic is repeated for register stages.
Q_5 to Q_1 Am2502/3
Q_9 to Q_1 Am2504
2. Numbers in parentheses are for Am2504

Figure 5. Successive Approximation Register Logic

REGISTER LOGIC

The logic diagram for the successive approximation registers is shown in Figure 5. The design differs from previous approaches in two ways. First, it has only one flip-flop per register stage; second, each stage is identical. These two factors allow an economical, efficient design particularly suitable for integrated circuit implementation. The design uses a minimum of components and power and operates at high speed.

The register flip-flops are split into two sets of latches. The master latches hold control information and change state when the clock input is LOW, and the slave latches hold the data and change state when the clock input is HIGH. The two latches used at each register stage are in a slave-master arrangement with gating between the slave and the master.

The peripheral logic necessary to take care of control inputs and outputs is fairly small. It consists of: (a) a master latch on the data input in which the serial data is temporarily stored prior to sending the data to the slave latch specified by the master control latches; (b) another master latch to hold the START information during the resetting of the register; (c) a conversion complete flip-flop; (d) for the Am2502 and Am2504 an extra slave latch, driven from the data master latch, which provides the serial data output; and (e) for the Am2503 and Am2504 registers enable logic, which is part of the most significant register bit slave latch and can override the resetting of this latch.

The enable input, $\overline{E}$, of the Am2503 and Am2504 allows registers to be cascaded for expansion and has the effect of controlling the state of the $Q_7(11)$ bit of the register so that when a START signal is applied the most significant bit stays HIGH instead of going LOW. The register remains at all HIGHs until the enable is released to a LOW. Immediately $Q_7(11)$ goes LOW, data is accepted at the data input, and conversion begins for this section of the register.

SUCCESSIVE APPROXIMATION CONVERSION

Successive approximation analog-to-digital converters operate by comparing an unknown analog input against a time-dependent feedback voltage derived from a digital-to-analog converter. Conversion proceeds one bit at a time with the most significant bit generated first. For the first iteration the most significant bit in the register is made LOW with all the remaining bits HIGH. The register then contains a "trial" binary number that lies in the center of the range of possible numbers. This number is fed to the D/A converter and a comparison is made between the resulting output of the digital-to-analog converter (1/2 full scale) and the incoming analog signal. If the incoming signal is larger than that from the digital-to-analog converter, a signal is fed back to the register to make the most significant bit active, and at the same time make the next less significant bit LOW ready for the next iteration. If, however, the analog input is less than the converter value, the most significant bit remains inactive, and only the next less significant bit changes for the next iteration.

Conversion of an analog input to an n-bit digital representation takes n+1 time slots. There are n time slots required for the data conversion and one time slot is required to initialize the register at the beginning of a conversion. The feedback voltage for the i th iteration of a conversion is

$$Vf_i = \frac{V_r}{2}\left[d_{n-1} + \frac{d_{n-2}}{2} + \frac{d_{n-3}}{4} \ldots + \frac{d_{n-i-1}}{2^i}\right]$$

Where: V_r is the total voltage range

$i = 0$ to $n-1$

$d_i = 0$ or 1, depending on the result of the i th comparison.

The number of bits in the register (n) is a measure of the digital resolution of the conversion.

Figure 6 shows an 8-bit straight binary analog-to-digital converter that is operating in a continual conversion mode. The Am2502 8-bit register provides the parallel input to an analog-to-digital converter. The output of this converter is then compared against the analog input and the result applied to the data input of the register. At each clock period an appropriate trial value is generated and a new data bit appears at the output of the comparator and is fed back to the register data input. When the conversion is complete, the $\overline{CC}$ output goes LOW and resets the register via the $\overline{S}$ input on the next clock.

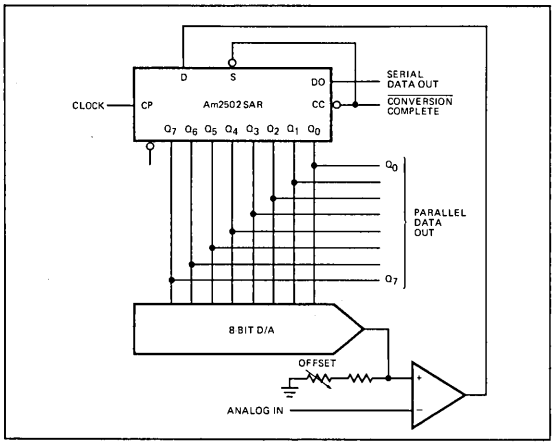


Figure 6. Successive Approximation 8-Bit Analog To Digital Converter

A timing diagram showing the states of all the inputs, outputs and internal signals is shown in Figure 7. The $\overline{CC}$ output can be used as a clock or enable to load the outputs of the successive approximation register into an 8-bit holding register or latch. A serial conversion train, most significant bit first, is available at the data output of the Am2502 if serial processing is required.

LOGIC POLARITIES

There are two notations used in the digital world to represent binary numbers. In active LOW level logic, the more negative voltage of the two voltage levels used to represent binary numbers is defined as logic "1"; logic "0" is the more positive voltage level. (This logic representation is often called negative logic). In active HIGH level logic, the more positive voltage level of the two is defined as logic "1", and the more negative is logic "0". (This logic representation is sometimes called positive logic). A logic network will not necessarily perform the same logic function in the two different representations. An example of a logic circuit that changes function on change of input operand polarity is the familiar NAND

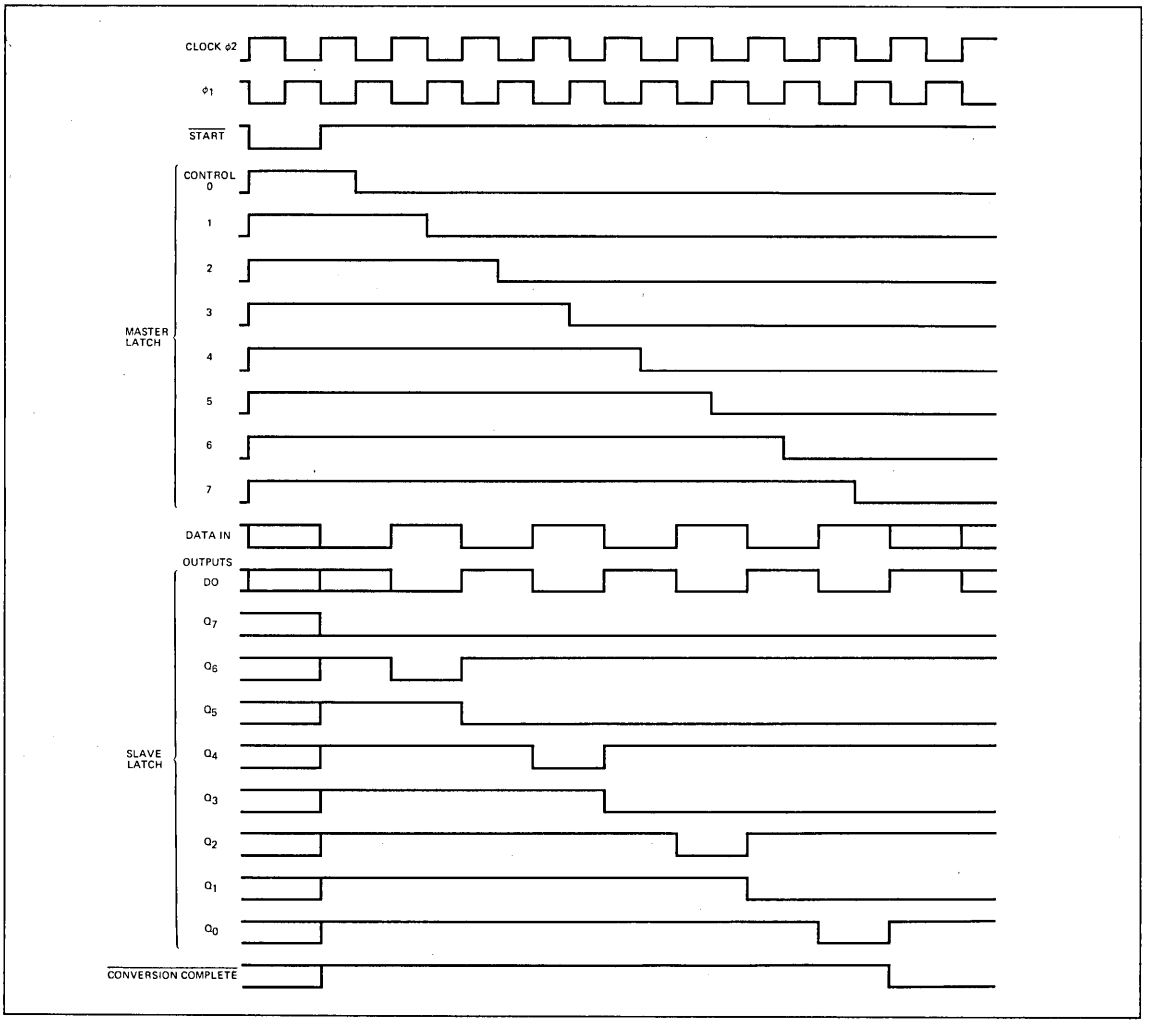


Figure 7. Am2503 8-Bit SAR Timing Diagram

Active High
Current Switches
Active High Digital Data
Bias Comparator $-\frac{1}{2}$ LSB
Effective Input $\frac{171}{256} > A > \frac{170}{256}$

TIME	Q_7	6	5	4	3	2	1	0	$\overline{CC}$	VALUE	D
0	L	H	H	H	H	H	H	H	H	127	H
1	H	L	H	H	H	H	H	H	H	191	L
2	H	L	L	H	H	H	H	H	H	159	H
3	H	L	H	L	H	H	H	H	H	175	L
4	H	L	H	L	L	H	H	H	H	167	H
5	H	L	H	L	H	L	H	H	H	171	L
6	H	L	H	L	H	L	L	H	H	169	H
7	H	L	H	L	H	L	H	L	H	170	H
8	H	L	H	L	H	L	H	H	L	171	
For	H	≡	"1"		L	≡	"0"				
	1	0	1	0	1	0	1	1		= 171	

Active Low
Current Switches
Active Low Digital Data
Bias Comparator $+\frac{1}{2}$ LSB
Effective Input $\frac{172}{256} > A > \frac{171}{256}$

TIME	Q_7	6	5	4	3	2	1	0	$\overline{CC}$	VALUE	D
0	L	H	H	H	H	H	H	H	H	128	L
1	L	L	H	H	H	H	H	H	H	192	H
2	L	H	L	H	H	H	H	H	H	160	L
3	L	H	L	L	H	H	H	H	H	176	H
4	L	H	L	H	L	H	H	H	H	168	L
5	L	H	L	H	L	L	H	H	H	172	H
6	L	H	L	H	L	H	L	H	H	170	L
7	L	H	L	H	L	H	L	L	H	171	L
8	L	H	L	H	L	H	L	L	L	171	
For	L	≡	"1"		H	≡	"0"				
	1	0	1	0	1	0	1	1		= 171	

Note: Analog input slightly greater than $\frac{171}{256}$ of full scale 8-bit conversion

Figure 8. Conversion With Active High And Active Low Current Switches

gate. With active HIGH inputs, it provides the AND function with an active LOW output. The identical logic gate provides the OR function with active LOW inputs and gives an active HIGH output.

There is no distinct advantage between the two representations. Some functions are simpler and take fewer components to perform with one representation than with the other. In practical systems logic polarities are usually mixed in order to take advantage of performing operations with a minimum of hardware and delay.

The successive approximation register can be used in either the active HIGH or active LOW logic representation simply by reinterpreting the input and output polarities. In practical systems this means that the register can be used for the digital storage and control with current switches which require a LOW voltage to turn on (active LOW current switches), or with current switches which turn on with a HIGH voltage level (active HIGH current switches). The circuitry is identical in both cases. The polarity of the current switch determines the logic polarity of the final digital converted value. The binary number will be active LOW for active LOW current switches and active HIGH for active HIGH current switches. The only other difference between the two representations is that the comparator must be offset +1/2 LSB for active LOW current switches and −1/2 LSB for active HIGH current switches to achieve a result with an accuracy of ±1/2 LSB. A numerical example of an 8-bit conversion using both types of current switch is shown in Figure 8.

CODING

An analog signal can be converted into a number of different digital codes. Figure 9 shows the output from a perfect 3-bit digital-to-analog converter and the various digital codes used versus the analog input signal. The connections between the successive approximation register and the analog-to-digital converter remain the same for all codes. The implementation of a particular code is made by offsetting the comparator, changing the weight of the most significant bit, and/or manipulating the result of the conversion.

STRAIGHT BINARY

The most straightforward code is straight binary or magnitude conversion. In this type of conversion the lowest analog input, usually zero volts, is assigned the digital value 000...0, and the highest analog input, the digital value 111...1. Analog inputs between the two extremes generate a binary number

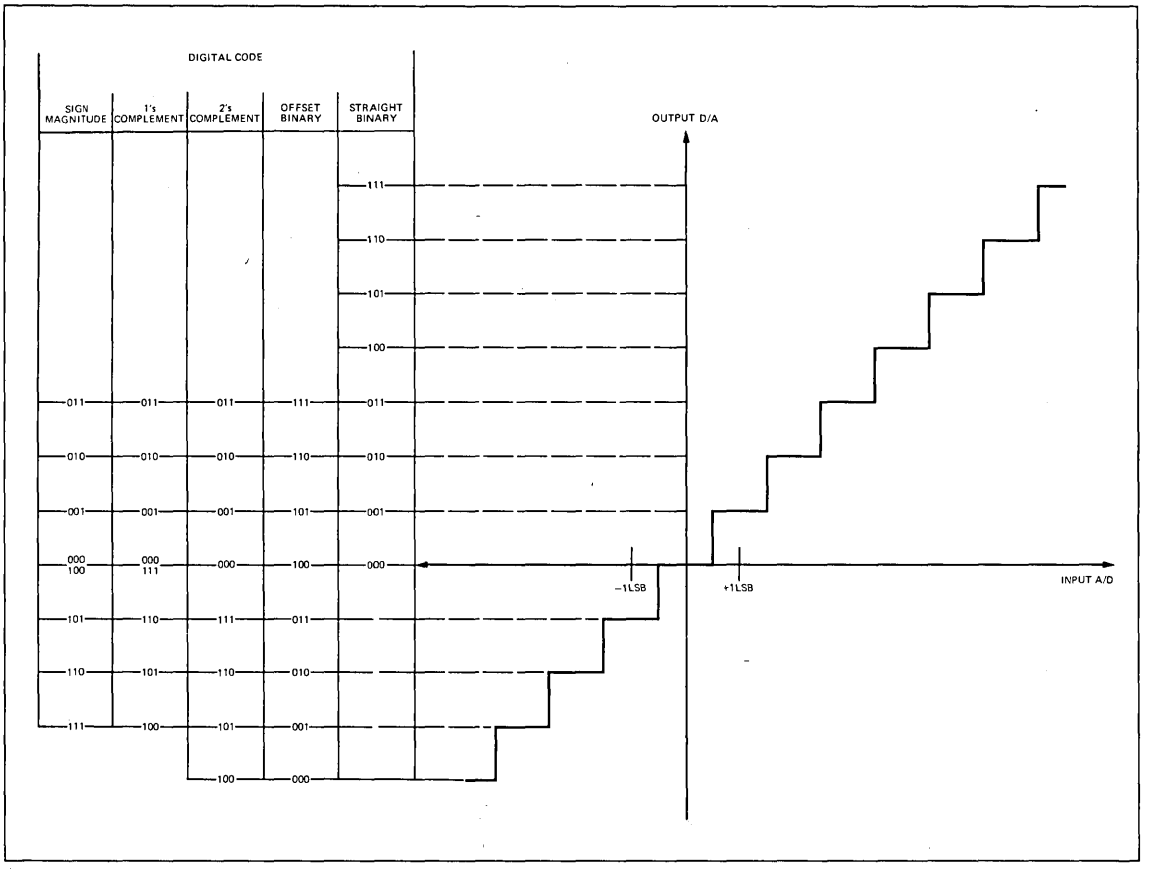


Figure 9. Analog Input vs Digital Output

that is the nearest integer to $\left(\frac{V_{in}}{V_r}\right)2^n$ where V_r is the total voltage range accepted by the converter and n is the number of bits in the conversion. Generally, the comparator is offset so that a transition between the codes 000...0000 and 000...001 is made when the analog input voltage is at $\frac{1}{2}\left(\frac{V_r}{2^n}\right)$. This offset causes rounding so that the digital value obtained is within 1/2 LSB of the true value.

OFFSET BINARY

This coding scheme is the same as the straight binary conversion except that it is used to convert bipolar analog signals—that is input signals which lie on either side of ground. The register is connected to the D/A converter exactly as in straight binary, and the comparator is offset by $-\frac{V_r}{2}+\frac{1}{2}\left(\frac{V_r}{2^n}\right)$ so that a transition from the digital value 1000..000 to 1000...001 is made when the analog input voltage is at $+\frac{1}{2}\left(\frac{V_r}{2^n}\right)$. Unfortunately, in the majority of digital systems the offset binary code is not directly usable by digital processors, and conversion to a different code has to be performed in the processor.

2's COMPLEMENT

Representation in the 2's complement mode is by far the most widely used bipolar representation for digital processors. The main reasons for this are that the coding scheme has only one code for zero and that arithmetic routines are straightforward. In this code the most significant bit represents the polarity of the input signal; the magnitude of a negative input voltage is represented as the 2's complement of the equivalent positive voltage. (The 2's complement of a number is obtained by inverting each bit and then adding a binary 1 at the least significant place of the number. For example, −1 in 2's complement is represented as 11111....111, which is the bitwise inversion of 0000....001 plus 1 at the least significant bit). For 2's complement representation the transition between the digital codes 0000...000 and 0000...001 occurs for an input voltage of $+\frac{1}{2}\left(\frac{V_r}{2^n}\right)$.

The 2's complement representation is identical to the offset binary representation except that the most significant bit is inverted. A 2's complement conversion then proceeds in identical manner to offset binary conversion, but the inverted output of the most significant bit of the register is used rather than the true output.

1's COMPLEMENT

The 1's complement notation represents negative values by the

bit-for-bit inverse of the equivalent positive number. This method of representing bipolar inputs has the severe disadvantage that there are two possible representations for zero: all zeroes 0000...000 and all ones 1111...111. Therefore, it is not often used and can cause some confusion in coding for the analog-to-digital converter at the zero input voltage level. To overcome this the most significant bit of the code is given an analog weight of $-(2^n-1)$, not -2^n. This has the effect of making the analog-to-digital converter give the same output (OV) for the codes 1000...000 and 0111...111. Apart from this change of weight, 1's complement conversion is identical to 2's complement conversion with the complement output of the most significant bit used rather than the true output.

SIGN MAGNITUDE

This coding scheme uses the most significant bit of the converted signal to indicate whether the analog input is positive or negative, with a digital "0" for positive and "1" for negative. The remaining bits in the word are used to indicate the magnitude of the analog input. Note that this coding scheme also suffers from the fact that there are two possible representations for zero: 0000..000 and 1000...000. Sign magnitude is, however, widely used in digital instrumentation since it is a familiar and effective way of representing bipolar analog quantities.

Sign magnitude conversion is very similar to 1's complement conversion. The digital-to-analog converter again has to produce a zero volt output for the codes 1000...000 and 0111... 111. Since in sign magnitude representation zero is represented by both 0000..000 and 1000...000, the result of the conversion uses the complement output from the most significant bit of the register as the sign bit and inverts the remainder of the result of the sign bit is a "1".

This inversion can be accomplished by a set of exclusive OR gates with each output of the register feeding one of the gate inputs, and the remaining gate inputs connected to the most significant register bit as a polarity control. An alternative method is to drive the serial train from the comparator through a single exclusive OR gate into a serial-to-parallel converter.

BCD CODES

The Successive Approximation Registers may also be used to convert an analog signal to a BCD Code by using a BCD Digital-to-Analog Converter in the conversion loop. During a BCD conversion the register must not be allowed to accept inputs which would make the converted value for each decade larger than "9", that is illegal codes must be suppressed.

For the normal 8421 BCD Code the two centre bits of each decade must not be allowed to turn on their respective current switches if the most significant bit of the decade under consideration has turned on its current switch. Using active LOW current switches this can be accomplished by forcing the data input HIGH during the comparisons taking place for generation of the two centre bits if the most significant bit of the register is LOW, and for the active HIGH case forcing the input LOW when the most significant bit of the decade is HIGH.

Logic which can take care of the illegal code situation for both active HIGH and active LOW current switches is shown in Figure 10.

OFFSETTING

Numerous methods for offsetting are available, and manufacturers of digital-to-analog converters indicate how the various offsetting schemes can be applied. Some digital-to-analog converters have an additional current switch and resistor leg that biases the converter output itself. Biasing can also be accomplished at one of the inputs to the analog comparator.

An important consideration is that the offsetting direction for an accuracy of $\pm\frac{1}{2}$LSB depends upon whether the current switches are turned on by a LOW or a HIGH, as shown in the section on logic polarity.

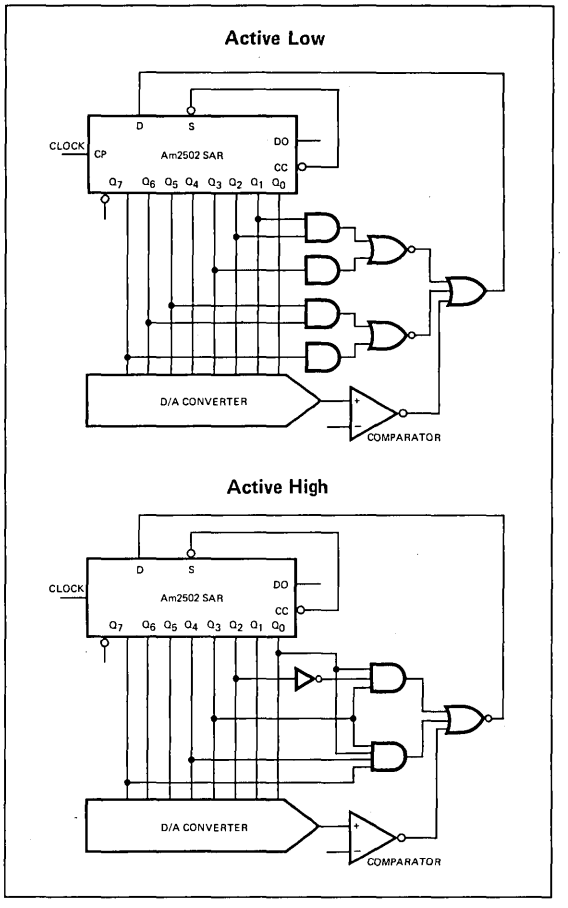


Figure 10. BCD Illegal Code Suppression

DIGITAL APPLICATIONS OF SUCCESSIVE APPROXIMATION REGISTERS

Recursive Arithmetic Routines

Successive approximation registers (SAR) can be used in pure digital systems. The most obvious application is in systems that perform recursive arithmetic operations similar to the analog-to-digital conversion sequence. An estimate is made of the operand and a calculation made with this trial value; the operand is then increased or decreased in value depending upon whether the result is less than or greater than a known value. This is a direct parallel with the analog-to-digital converter. A combinatorial switching network, where the output is some monotonic function of its input, takes the place of the D/A converter; and a digital comparator takes the place of the analog comparator. When the SAR is used as the trial register, an n-bit result is achieved in n+1 iterations (as against 2^n-1

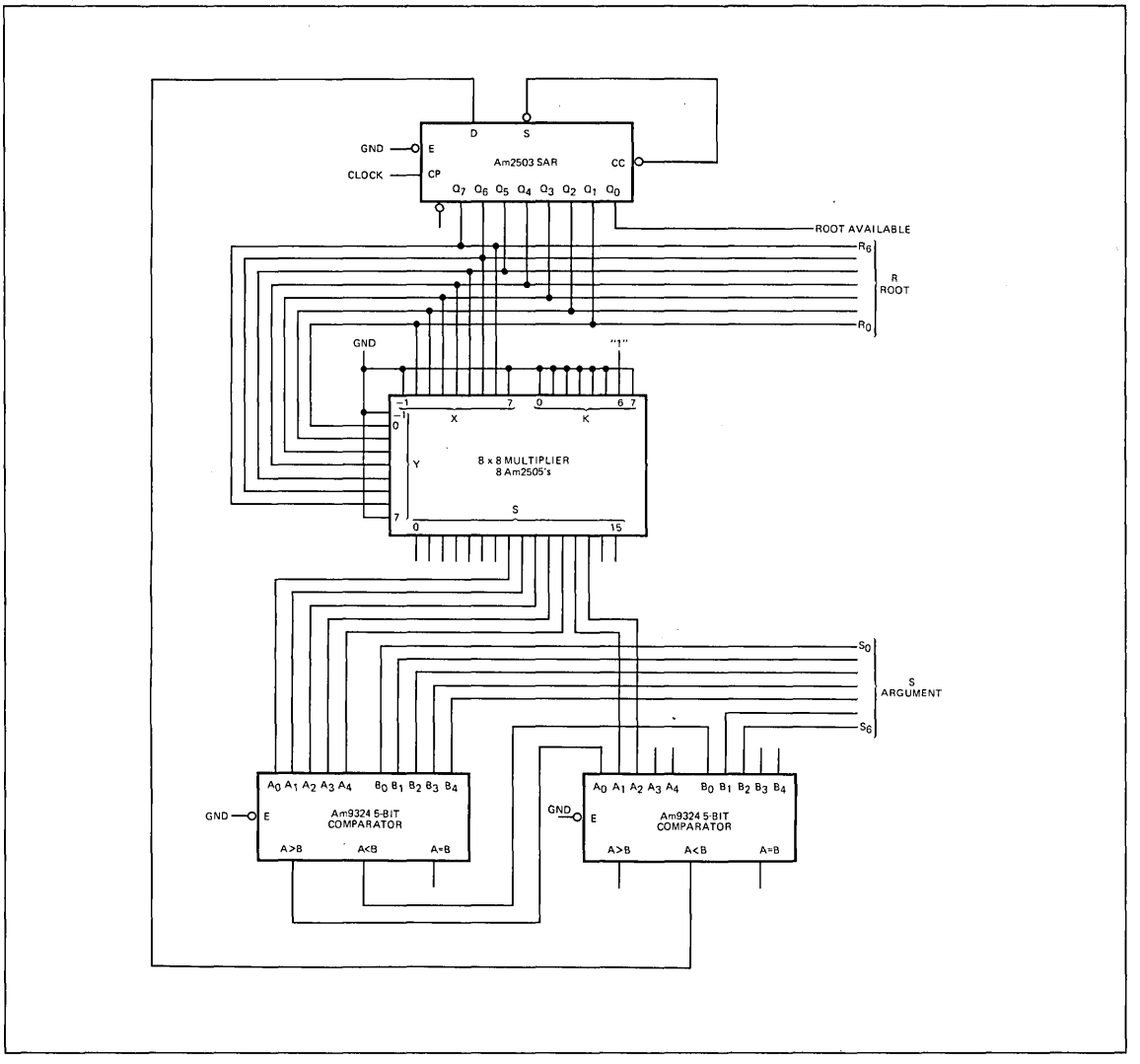


Figure 11. Square Root Evaluation By Recursion

iterations on the average if a counter is used as the trial register). Numerous mathematical equations can be solved by this method, including the derivation of the square root of a number and the quotient in a division operation. The only criteria necessary are that a real solution exists and that the solution is monotonic—that is, unique as far as magnitude is concerned.

Figure 11 shows how the square root of a number is formed using a multiplier array built with Am2505 digital multipliers as the function generator. The successive approximation registers provide the estimate that is then squared and compared with the number whose root is required. If the square of the trial value is less than the number whose root is desired, then a "1" is fed back to change the register bit under consideration. The time to achieve a square root is essentially n+1 multiply times, which, if the square root operation is not often employed, and a multiplier array is present may be very acceptable since it takes only an additional successive approximation register and a comparator. The network can easily be modified to perform operations of the type $r = (X^2 + Y^2 + Z^2)^{1/2}$. The multiplier array can be used to generate the various squares, add the products and then compare the result against a trial value derived from the same multiplier array. The time required would then be n+4 multiplication times.

Another application frequently used is the division operation. This can be performed by multiplying the trial value, n, by the divisor and comparing the result against the dividend. If the dividend is larger then the trial value has to be increased; if the dividend is smaller then the trial value has to be reduced. The operation is fairly straightforward for unsigned division; with signed division a few problems occur.

For 2's complement integer division the logic is shown in Figure 12.

The divisor, dividend and trial quotient are all treated as 2's complement numbers. The first trial value is all ones (–1).

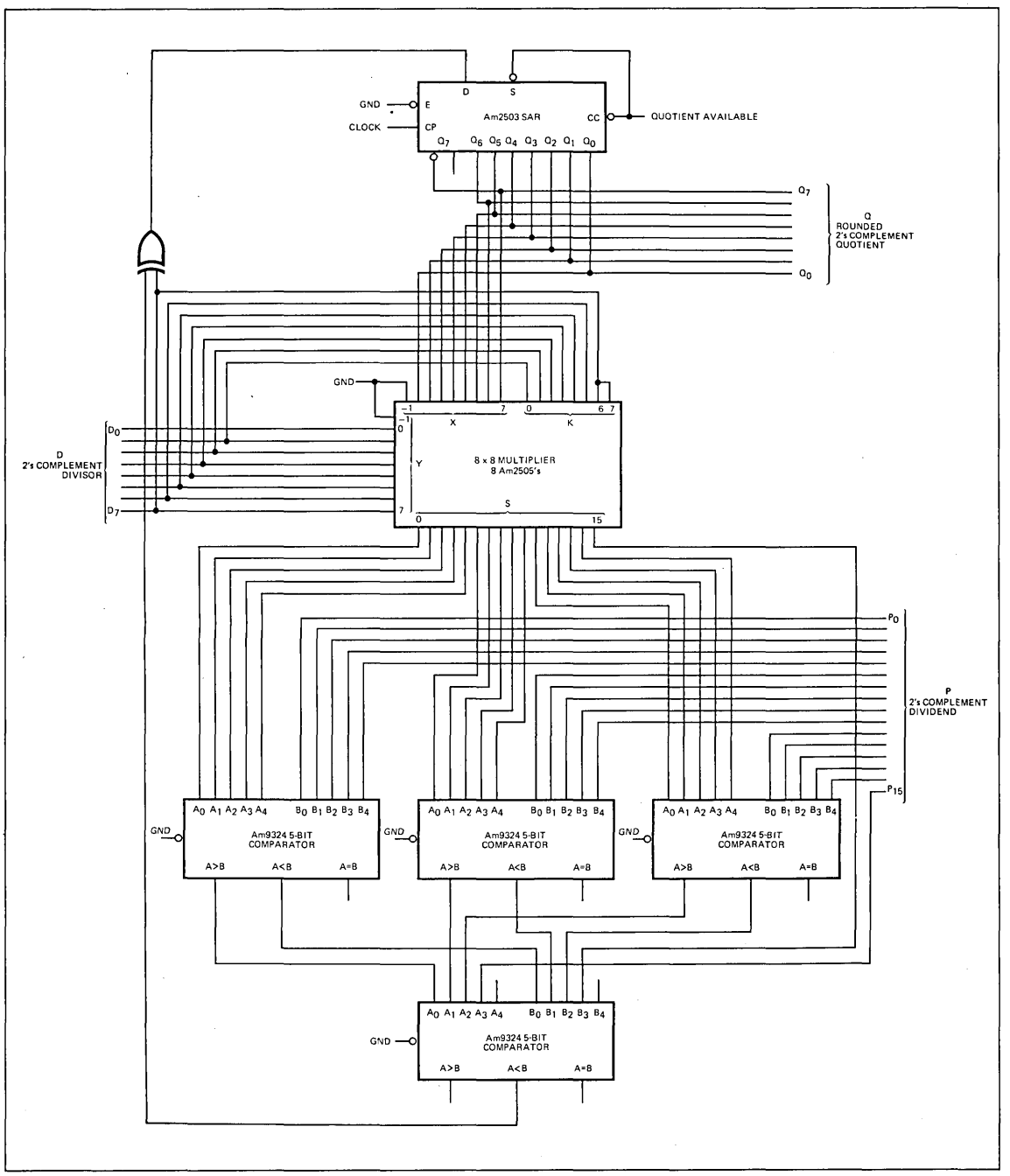


Figure 12. 2's Complement Rounded Division

The operations performed are:

For Q_S, the sign digit of the quotient:

If $D_7 = 0$ and $-\frac{D}{2} < P$ Set $Q_S = 0$ Otherwise $Q_S = 1$

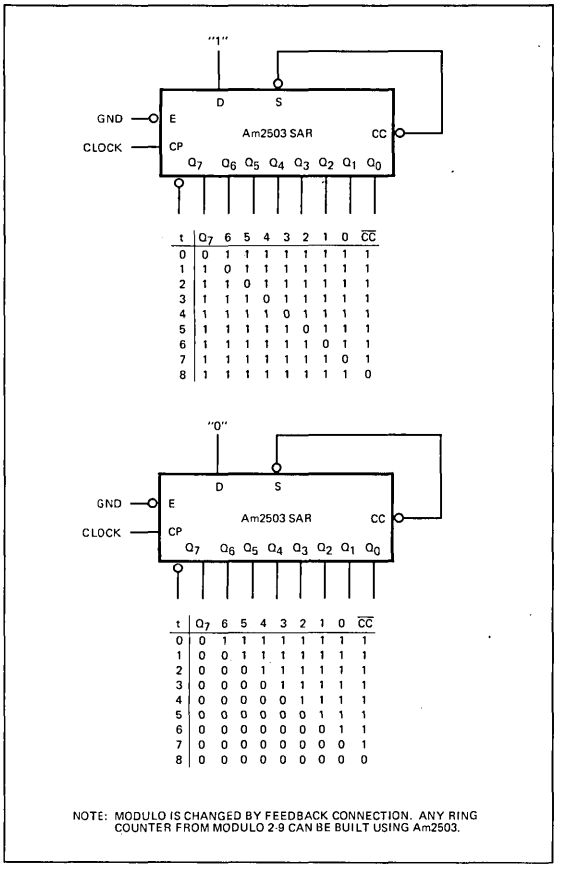
If $D_7 = 1$ and $-\frac{D}{2} < P$ Set $Q_S = 1$ Otherwise $Q_S = 0$

For the remaining quotient digits:

If $D_7 = 0$ and $T_{i-1}\, D + \frac{D}{2} < P$ Set $Q_i = 1$ Otherwise $Q_i = 0$

If $D_7 = 1$ and $T_{i-1}\, D + \frac{D}{2} < P$ Set $Q_i = 0$ Otherwise $Q_i = 1$

where T i is the i th trial value held in the SAR.



t	Q_7	6	5	4	3	2	1	0	$\overline{CC}$
0	0	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1
2	1	1	0	1	1	1	1	1	1
3	1	1	1	0	1	1	1	1	1
4	1	1	1	1	0	1	1	1	1
5	1	1	1	1	1	0	1	1	1
6	1	1	1	1	1	1	0	1	1
7	1	1	1	1	1	1	1	0	1
8	1	1	1	1	1	1	1	1	0

t	Q_7	6	5	4	3	2	1	0	$\overline{CC}$
0	0	1	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	1	1
2	0	0	0	1	1	1	1	1	1
3	0	0	0	0	1	1	1	1	1
4	0	0	0	0	0	1	1	1	1
5	0	0	0	0	0	0	1	1	1
6	0	0	0	0	0	0	0	1	1
7	0	0	0	0	0	0	0	0	1
8	0	0	0	0	0	0	0	0	0

NOTE: MODULO IS CHANGED BY FEEDBACK CONNECTION. ANY RING COUNTER FROM MODULO 2-9 CAN BE BUILT USING Am2503.

Figure 13. Ring Counters

Since the complement of the most significant bit of the register is used rather than the true output so that resetting the register presents −1 to the multiplier array, the change in algorithm between the sign bit and the rest of the bits is automatically taken care of.

The D/2 factor in the equations is used to round off the quotient. A double length dividend is assumed. The comparator is wired for a 2's complement comparison with the sign digit of the product and dividend crossed over, the dividend sign bit forming part of the multiplier word and the product sign bit forming part of the dividend word.

RING COUNTERS

Successive approximation registers can be used as ring counters by appropriate feedback. If the data input is held HIGH, as in Figure 13, then the register will fill up with logic 1s when clocked; and the trial bit, which is a logic "0", will shift along the register. The $\overline{CC}$ output can also be used as a counter stage so that the Am2502/3 can be made into a modulo 9 ring counter and the Am2504 into a modulo 13 counter. A counter with a smaller modulo can be generated by feeding back one of the register outputs to the START input. This type of ring counter is widely used for linear selection in memories, multiplexed display systems and for sequencing in control systems.

An alternative type of ring counter, essentially a moving edge, can be built by holding the data input LOW. The register on each clock pulse then fills with logic "0"s, and a logic edge moves across the register as it is clocked. Again, by suitable feedback connection, the counter modulo can be altered. The size of the ring counter can be increased by cascading several registers allowing ring counters of any length to be achieved.

SERIAL-TO-PARALLEL CONVERSION

The Am2502/3 and Am2504 are special purpose serial-to-parallel converters and can be used in digital systems for this purpose. In addition to performing the conversion function,

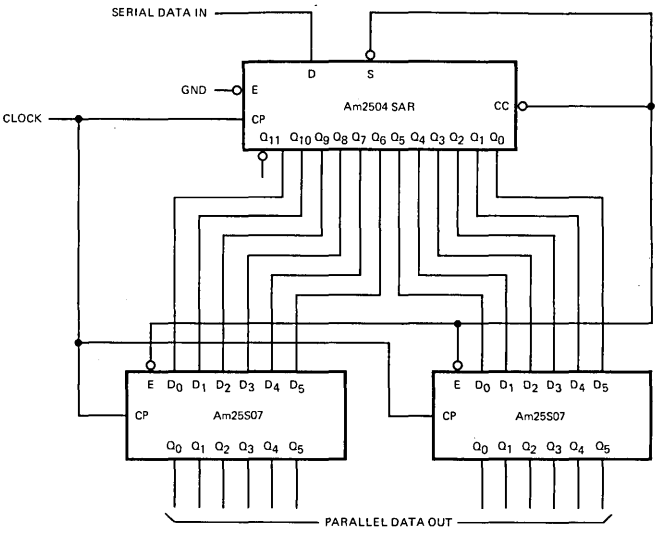


Figure 14. Controlled Serial-To-Parallel Conversion

the conversion complete and start logic can conveniently be used to have the register automatically load its contents into a holding register while another conversion is being performed. Figure 14 shows the Am2504 with two high-speed holding registers used to hold the result of the conversion while another conversion is being performed.

In many digital communications systems, data is sent serially with a synchronizing or frame marker inserted between blocks of data. A simple example of this is shown in Figure 15. The serial input consists of groups of nine bits: eight bits for data and a synchronizing bit at the end of each data block. Data enters the Am2503 serially until it is filled, whereupon the $\overline{CC}$ output goes LOW. The register cannot be reset unless the next incoming bit, hopefully the synchronizing bit, is a "1". The register can only continue on a "1" and assumes the next "1" in the serial stream is the synchronizing bit. The register is then reset when the "1" appears and conversion starts again. If the register was not synchronized, then the conversion will have begun in a different time frame and a check is again made the next time the $\overline{CC}$ output is LOW. Sooner or later the data stream becomes synchronized with the register and remains so until an error occurs, when it again slips bits until synchronization recurs.

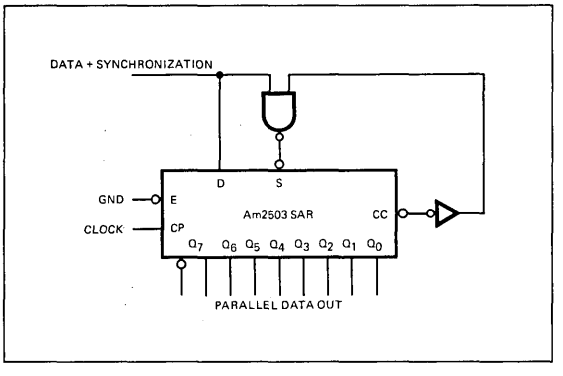


Figure 15. Synchronizing Serial-To-Parallel Converter

A more elaborate system is shown in Figure 16. This scheme is a multi-channel serial-to-parallel converter. Serial data enters each register in turn. When one register has its last stage LOW and the $\overline{CC}$ HIGH, it indicates that the data should be sent to the next register on the next one clock pulse. This method insures that the information is held in parallel in the registers for three-fourths of the total cycle. An extra input on the start control logic allows synchronization of the input pulse train to the converter.

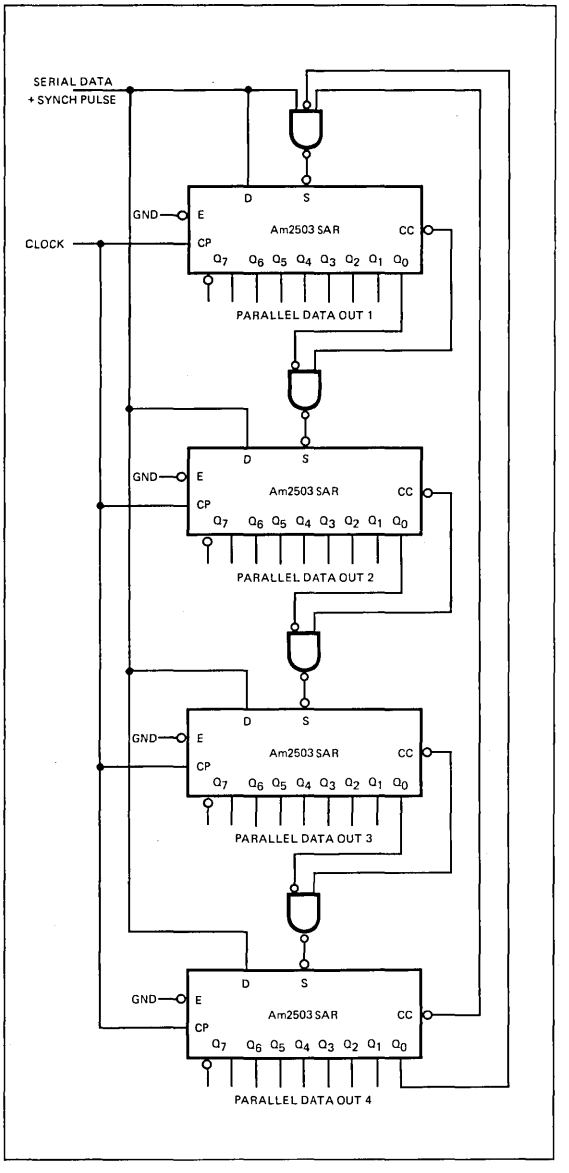


Figure 16. Synchronizing Multi-Channel Serial-To-Parallel Converter

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A NEW HIGH-SPEED COMPARATOR THE Am685

By Jim Giles and Alan Seales

INTRODUCTION

Modern electronic systems require more and more that operations be performed in a few nanoseconds so that the delay of the complete system, which may be very complex, be held to a minimum. There are abundant logic circuit elements available that meet this criterion: gold-doped TTL, Schottky TTL, and emitter-coupled logic (ECL), listed in descending order of propagation delay. Where it is necessary to interface from the analog world to the input of a logic system, or to detect very low-level logic signals in the presence of heavy noise, a high-speed precision comparator is needed. If such a comparator had a propagation delay less than 10ns, it could replace costly and complex circuitry that designers are now forced to use in very high-speed analog-to-digital converters, data acquisition systems, and optical isolators, as well as make possible many applications hitherto considered unfeasible. It could also be used as a sensitive line receiver or sense amplifier, in 100MHz sample and hold circuits, and in very high-frequency voltage-controlled oscillators.

The basic requirements for a high-speed precision comparator are few and well-defined: good resolution (high gain), high common-mode and differential voltage ranges, outputs compatible with standard logic levels, and, above all, very fast response to signal levels ranging from a few millivolts to several volts. The industry workhorse, the 710, has come close to meeting these requirements, and except for the most demanding applications, its 40ns propagation delay is adequate. A survey of presently available monolithic IC comparators (Table I) shows that there is really none that meets the requirements of very high-speed systems. The newer TTL-output circuits offer only marginal improvement over the 710 when measured under identical conditions of large input pulse and small overdrive, and the ECL-output comparator, although faster, has such poor resolution that it can be used only for large input signals. Advanced Micro Devices felt there was a need for a family of linear devices to fill the needs of very high-speed systems, with the first circuit being a precision comparator with less than 10ns delay.

Type No.	Logic Family	Propagation Delay	Resolution
Am111	TTL	200ns	0.012mV
μA710	TTL	40ns	1.4mV
Am106	TTL	40ns	0.06mV
μA760	TTL	25ns	0.5mV
NE527/529	TTL	25ns	0.5mV
MC1650	ECL	12ns	30mV

Table I: Propagation Delays of Available Monolithic IC Comparators (100mV Input Step, 5mV Overdrive)

DESIGN OBJECTIVES

In order to achieve the ultimate in speed, it is clear that the comparator outputs must be compatible with ECL, even though at present the majority of systems use TTL. Designers striving for the highest possible speed will already be using ECL in the critical circuit areas of their systems to squeeze the last possible nanosecond out of the overall delay. Further, an ECL circuit requires only one-third the gain of an equivalent TTL circuit for the same resolution owing to its smaller output logic swing. This means that lower impedances can be used and consequently larger bandwidth realized for the same power dissipation. Also, there is no problem interfacing the linear input stages with the digital output gate since an ECL gate is basically a non-saturating overdriven differential amplifier. Properly driving a TTL gate from a linear amplifier is more difficult, however, because it requires a large voltage swing suitably biased to track the input logic threshold with temperature, plus a large peak negative current capability to turn off the gate with minimum delay.

The usefulness and versatility of a comparator can be enhanced by adding a strobe or latch function to the circuit. A strobe simply forces the output of the comparator to one fixed state, independent of input signal conditions, whereas a latch locks the output in the logical state it was in at the instant the latch was enabled. The latch can thus perform a sample and hold function, allowing short input signals to be detected and held for further processing. If the latch is designed to operate directly upon the input stage—so the signal does not suffer any additional delays through the comparator—signals only a few nanoseconds wide can be acquired and held. A latch, therefore, provides a more useful function than a strobe for very high-speed processing.

The most difficult input signal for a comparator to respond to is a large amplitude pulse that just barely exceeds the input threshold. This forces the input stage of the comparator to swing from a full off (or on) state to a point somewhere near the center of its linear range. This exercises both the large-and small-signal responses of the stage. If the comparator has less than 10ns delay under these stringent conditions, then it should be as fast or faster for any other circumstances (see Figure 1). The industry standard measurement is with a

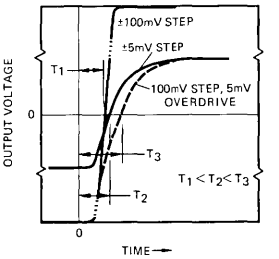


Figure 1. Response to step input signals at output of a differential amplifier

100mV input pulse and an overdrive 5mV above input threshold (this was used for the delays given in Table 1). Pulses larger than 100mV might be used, but this would multiply measurement difficulties, since only a few tenths of a percent aberration or ripple in the pulse generator waveform would be enough to seriously affect the accuracy of the small overdrive, and thus would give misleading results for the propagation delay.

To obtain satisfactory speed for all input signals and particularly for the worst case measurement conditions, the input stage of the comparator must have: 1) wide small-signal bandwidth, 2) high slew rate for large signals, 3) minimum voltage swings, and 4) high gain. The first requirement can be realized by using low-value load resistors, by making every effort in circuit design, device geometry and processing to minimize parasitic capacitances, and by using transistors with the highest f_T possible. The second item calls for high operating currents as well as minimum capacitance. The last two requirements are conflicting, since obtaining high gain normally requires a large voltage swing; therefore some means of clamping the swing must be used that does not degrade the propagation delay.

The overall gain of the complete comparator must also be high because, as illustrated in Figure 1, the propagation delay is less if each stage is well overdriven. To ensure that most of the input overdrive signal is actually used for overdriving, and not consumed in just moving the output from one state to the other, the gain error should be no more than about 10% of the input overdrive. Therefore, for a 5mV overdrive and an ECL output swing of 800mV, the minimum gain must be 1600. It is not practical to strive for much higher gain than this because the small-signal rise time begins to suffer as the stage gain increases. Addition of another stage is undesirable as this also adds delay and increases circuit complexity. It must be remembered that there is a maximum limit on power dissipation that a single integrated circuit package can handle adequately, and this consideration must influence the choice of operating currents and impedance levels throughout the design of the circuit.

With a figure for the total gain required, it is now possible to determine the number of stages and the gain per stage. Since the output stage must be ECL-compatible, its design is fixed, giving a differential-input to single-ended-output gain of about 6. This leaves a differential gain of 270 to be provided by the remainder of the comparator. This is most efficiently divided between two stages, each with a gain somewhat over 16. Both stages should be identical, since minimum overall delay time is obtained when identical stages are cascaded.

A factor not yet discussed that affects the accuracy of the comparator is its input offset voltage. Unless this is trimmed out initially, it must be added to the overdrive in determining the worse-case value of input signal for which the propagation delay specifications will be met. Even with trimming, the temperature drift of high-offset units is typically much greater than that of low-offset units. Therefore, it is desirable to have low initial offset so that trimming is not necessary, and so that the offset temperature coefficient will be good. Also affecting the offset voltage and its drift at higher source resistances are the input currents. To keep this contribution to the total offset low requires high current gains in the input transistors. Therefore, obtaining offsets in the 1–2mV range requires close attention to circuit design, mask layout, and very tight process control (equivalent to that needed for the high-performance, low-frequency operational amplifiers), but with the added kicker of f_Ts well above 1GHz.

As was mentioned, large common-mode and differential voltage ranges are desirable features of a comparator. The limits of the common-mode range in a well-designed circuit should be close to the supply voltages. Since a high-speed comparator will, of necessity, operate at fairly high current levels, the supply voltages must be low to stay within the package power dissipation limits. As a minimum, the common-mode range should be equal to or exceed the differential voltage range to take full advantage of the voltage breakdown characteristics of the input transistors. The basic differential amplifier input stage has a differential voltage breakdown in the range of 5 to 6 volts; the design goal for the common mode range should thus be at least ±3 volts.

In summary, the design objectives for a high-speed precision comparator are as follows:

1) propagation delay <10ns measured at 100mV input step, 5 mV overdrive
2) ECL-compatible outputs
3) latch capability
4) gain >1600
5) input offset voltage <±2mV
6) common -mode range >±3V

CIRCUIT DESIGN

The watchword in designing wideband circuits is simplicity – have the fewest possible active devices in the signal path, the lowest possible impedance levels, and the lowest possible capacitance. The simple, common-emitter differential amplifier can be designed to approach these ideals with one major exception: the deleterious shunting effect of the collector-to-base capacitance upon the driving source resistance is multiplied by the voltage gain of the stage (Miller effect). Even though the impedance levels will be only a few hundred ohms at most, this condition cannot be tolerated if maximum speed is to be achieved. The solution is to add an additional pair of common-base transistors to form a differential cascode amplifier (Figure 2). This circuit has all of the performance features of a common-emitter amplifier and no feedback capacitance.

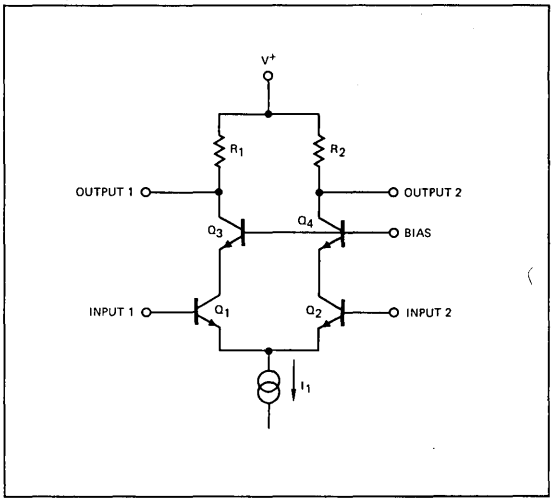


Figure 2. Differential cascode amplifier

Further advantages of the cascode will become apparent later when the latch design is discussed. The only drawback is that there are more devices in the signal path, the positive common-mode range is reduced, and circuitry has to be provided to bias the cascode transistors.

It is now necessary to provide a means of shifting the signal at the output of the cascode (which is very near the positive supply voltage) down to a lower voltage to drive the inputs of the second stage. The use of PNPs is definitely out because of their poor frequency response. This leaves three possibilities: a chain of forward-biased diodes, a programmed voltage drop across a resistor, or a zener diode. The diode chain is useful for level shifts of only a few volts at most, above that, the number of diodes gets too large, with a consequent increase in shunt capacitance and temperature coefficient. The use of a current-source/resistor combination is in the wrong direction for keeping impedance levels low. The resistors could be bypassed with capacitors, but this would offer only marginal improvement, since integrated capacitors have a large shunt component to the substrate. Besides, the addition of four capacitors (for both stages) would result in a large increase in chip area.

The zener diode is definitely superior for high-frequency applications because its shunt capacitance to ground is low, being equal to the collector-to-base capacitance of a transistor. It has no capacitance to the substrate, and its dynamic resistance is quite low. It does have the disadvantage that the level shift is limited to one voltage (6V), which restricts the range of power supply variation the circuit can tolerate. In addition it requires very tight control of the manufacturing process to maintain the matching required. For an input stage gain of 16 the zener voltages have to be matched to better than 0.25% to produce less than 1mV offset voltage at the input.

As shown in Figure 3, the zeners are buffered from the cascode collectors by emitter followers. The pulldown current through the zener-follower combination must be made large enough to discharge the node capacitance when the follower swings in the negative direction. The minimum value necessary is determined by the node capacitance, the signal swing, and the amount of delay that can be tolerated. The amount of signal swing can be reduced by adding clamping diodes across the collectors of the cascode. Regular diode-connected transistors could be used, but would add considerable collector-to-substrate capacitance across the load resistors as well as base-to-emitter capacitance between them. Schottky diodes, on the other hand, require little additional chip area, and are very fast. With clamping, some of the common-mode range lost when the cascode was added can be regained because the cascode transistors can be biased closer to the positive supply without fear of going into saturation at the extremes of the signal swing. The use of Schottky diodes, however, puts a few more gray hairs on the head of the process engineer since he has to control another set of characteristics without affecting the other parameters. The circuit values given in Figure 3 are designed for a minimum differential gain of 16, and a minimum negative-going slew rate at the output of the level-shifter of 1000V/μs.

As mentioned earlier the design of the output stage (Figure 4) can vary little from that of a standard ECL gate. The output emitter followers have to be large enough to handle loading by a 50Ω transmission line (25mA), yet small enough not to add a lot of capacitance that would slow down the response. Therefore, the transistor design must be as efficient as possible with regard to physical size and current-carrying

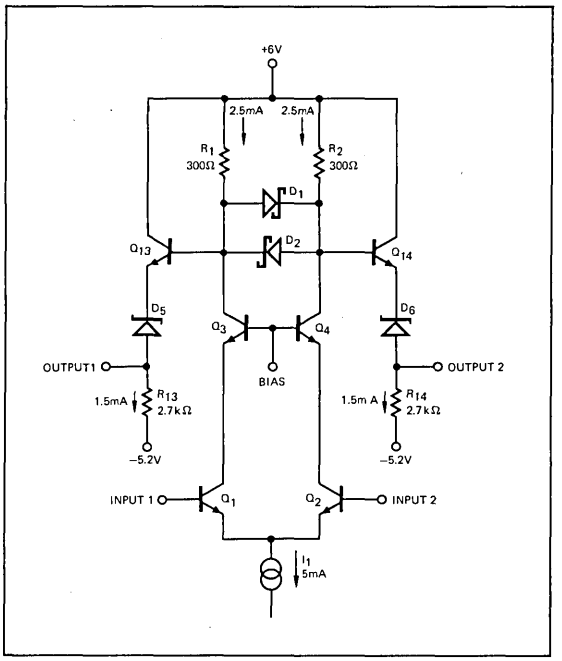


Figure 3. Basic cascode gain stage

capacity. Since the input common-mode level to the gate varies with changes in the power supplies and resistor tolerance, a current source is used to supply the emitters of the gate, rather than the usual resistor to the negative supply. The design of this current source must be such as to provide the correct logical "1" and "0" levels at the output and the proper variation with temperature and power supply changes. The propagation delays to either output of this gate will be equal, whereas they are slightly different in a standard ECL gate owing to the additional capacitive loading on the $\overline{Q}$ output caused by the multiple input transistors.

Implementation of the latch function must be accomplished without interfering with the normal comparator operation or degrading the speed in any way. It must be as close to the input as possible to permit short input signals to be acquired and held. One simple method of adding a latch to a differential

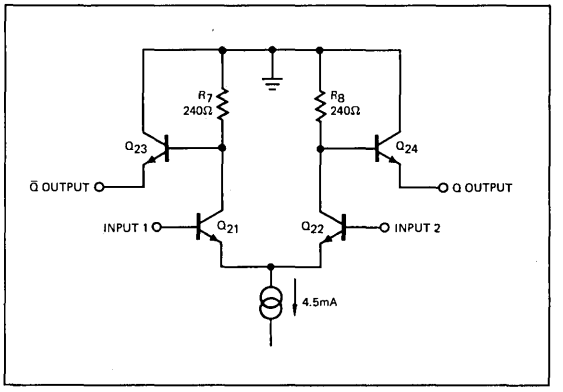


Figure 4. Output gate

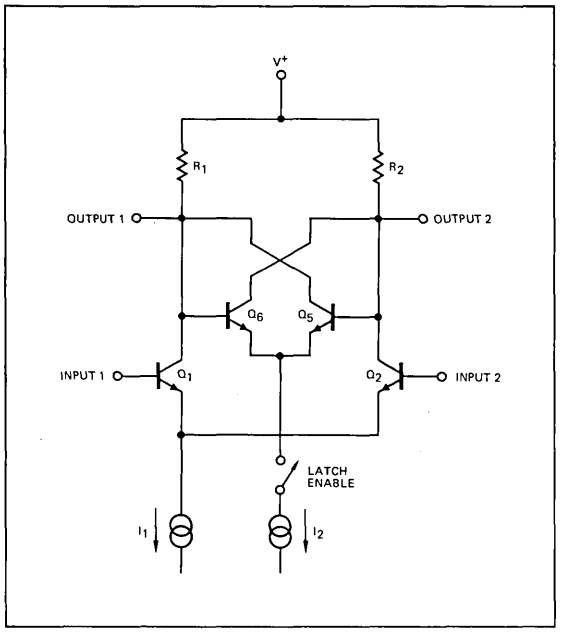


Figure 5. Simple latch circuit

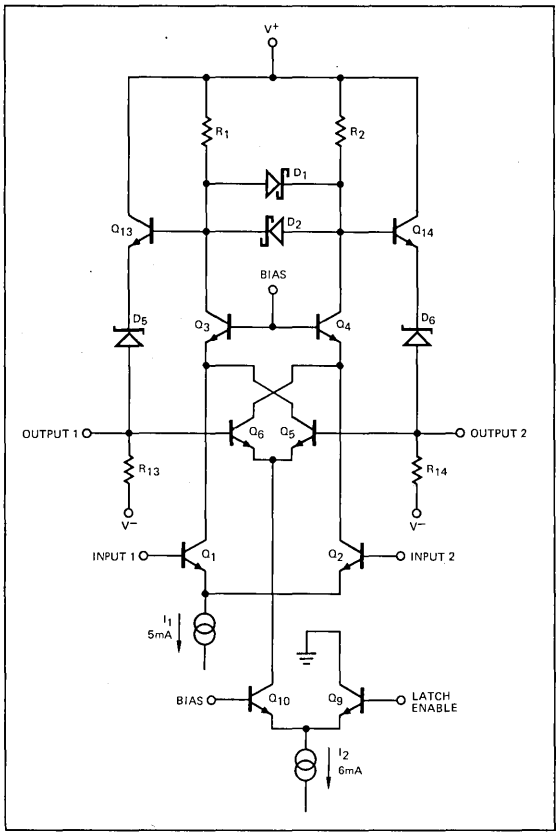


Figure 6. Cascode with latch

amplifier is shown in Figure 5. A pair of transistors, Q_5 and Q_6, are cross-coupled at the collectors of the input transistors, Q_1 and Q_2. The current source I_2 is switched on when it is desired to enable the latch. If I_2 is greater than I_1, the positive feedback via Q_5 and Q_6 will hold the circuit in whatever state it was in when the latch was turned on.

The simple circuit of Figure 5 is not the best for speed because of the added capacitance of Q_5 and Q_6 and the fact that they can saturate unless the signal swings are very small. However, it can be adapted to the cascode stage quite nicely as illustrated in Figure 6. Drive for the positive feedback transistors is taken from the level shifters, and the collectors go to the emitters of the cascode. With this arrangement there is no significant capacitive loading on the gain stage at all. The current source is switched by another differential amplifier, Q_9–Q_{10}, referenced to the ECL logic threshold voltage. This provides the correct input levels for the Latch Enable being driven from a standard ECL gate as well as being very fast, since only currents are being switched.

The latch current source (I_2) must be about 1mA greater than the input current source (I_1) to ensure positive latching for any condition of input signal. Thus, for 5mA in the input stage, at least 6mA must be used to power the latch. This amounts to a lot of power consumed for a function that some users may never even need. However, there is a way to cut the latch standby power down to zero; this is accomplished by the addition of Q_7 and Q_8, as shown in Figure 8.

To understand the function of these transistors, first refer to Figure 7. The differential voltage appearing across the emitters of the cascode transistors is equal to the input signal (for small input signals). This is because the currents through the lower pair of transistors in the cascode are equal to the corresponding currents through the upper pair, and the transistors are matched; therefore the differences in base-emitter voltages must be equal. Thus, Q_7 and Q_8 function as if they were

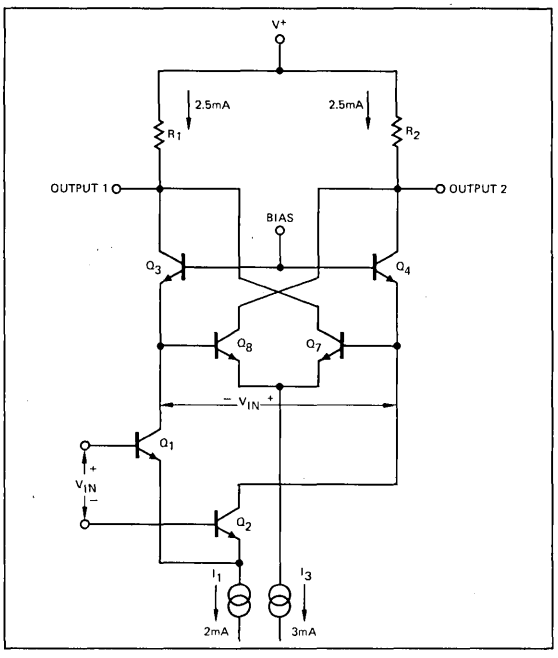


Figure 7. Cascode with "parallel" transistors

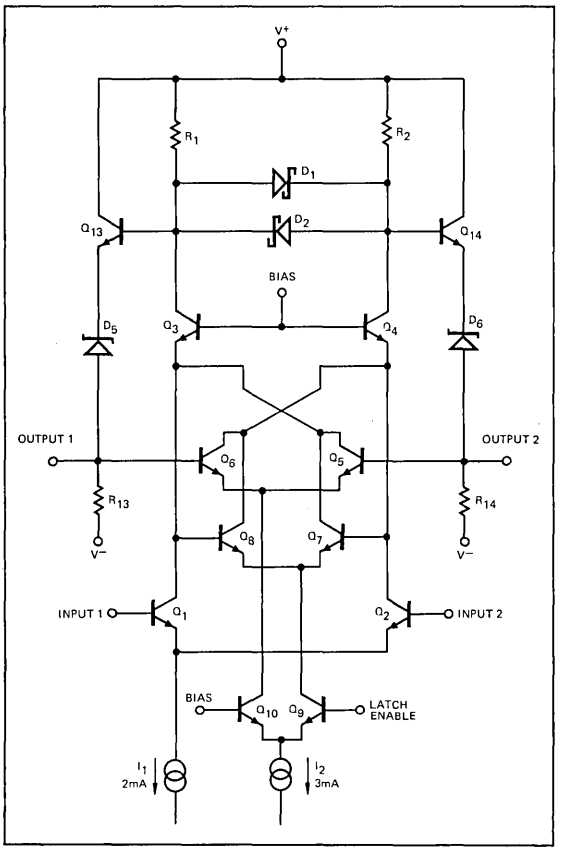


Figure 8. Complete input cascode stage with latch

simply connected in parallel with Q_1 and Q_2, as far as the net effect at the collector load resistors is concerned. To obtain the desired total stage gain, the current I_1 can be 2mA and I_3 can be 3mA.

Now refer to Figure 8. With the latch enable HIGH, Q_9 will be switched on and the 3mA current source will be supplied to the parallel transistors, Q_7–Q_8. The comparator functions normally, and no current is used up in the latch. When the latch enable goes LOW, I_2 will be switched through Q_{10} to the positive feedback transistors, robbing 3mA from the gain stage and giving it to the latch. The latch current is now 1mA greater than the input stage current, but the total current required is still only 5mA. As with the latch transistors, the collectors of the parallel transistors are connected to the emitters of the cascode, so no additional capacitance is added across the load resistors. This places the requirement on Q_7 and Q_8 that they maintain their high f_T at zero collector-to-base voltage.

The use of the parallel transistors has the added bonus that the input bias currents are decreased by more than a factor of two, thus reducing their influence on the offset voltage. The penalty paid is that all three pairs of junctions (Q_1–Q_2, Q_3–Q_4 and Q_7–Q_8) add equally to the input offset. Once again, the processing must be carefully controlled to keep the overall offset within the 2mV goal.

The complete circuit of the comparator is given in Figure 9. It includes some additional refinements as well as the DC biasing. The drive for the latching transistors is taken from the emitters of the second cascode rather than from the level-shifting zeners. This removes their input capacitance from the level shifter and also ensures that Q_{10} cannot saturate. A resistor (R_9) is included to center the common-mode voltage at the input to the gate within its dynamic range; this prevents saturation of the gate or its current source over the expected range of signal swing, temperature drift and supply voltage variations. A separate ground is used for the output emitter followers so that heavy loading at the output will not couple back into the remainder of the circuit. The DC bias chain for the current sources is referenced to ground and the negative supply, so the output logic levels will track those of other ECL circuits connected to the same negative supply. The current sources are designed to stay constant with temperature, which keeps the open-loop gain high at elevated temperatures (>1000 at +125°C), and thus helps to maintain good propagation delay.

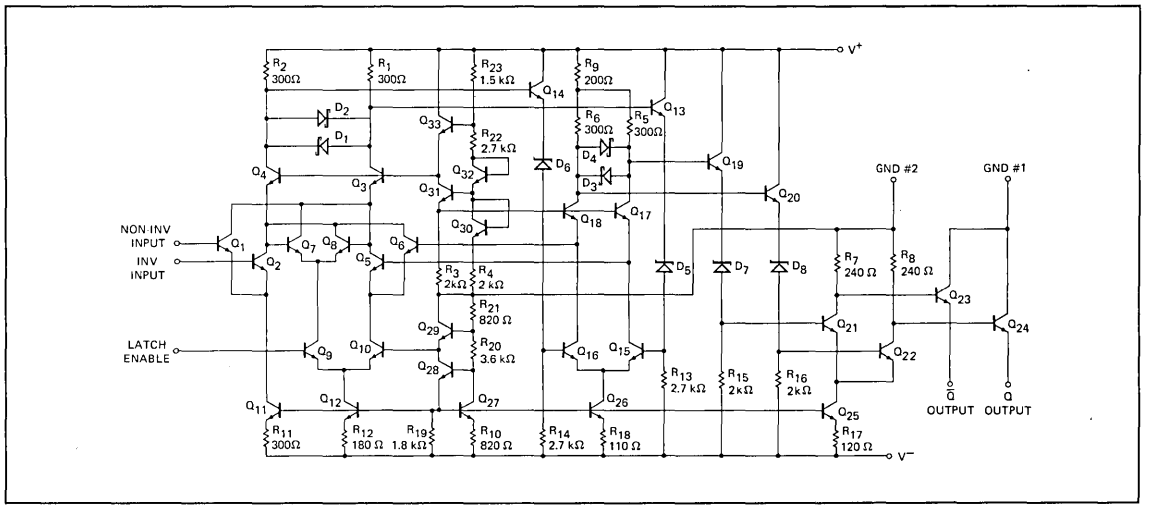


Figure 9. Complete schematic of the Am685 comparator

PROCESS TECHNOLOGY

Circuit design requirements for high speed and a latch function result in an input structure that has three pairs of transistors, the matching of which determines the offset voltage. This dictates that the matching of V_{BE} shall be extremely good between the transistors in each pair in order to meet the 2mV maximum offset voltage target. For the speeds necessary the transistor f_T has to be in the region above 1 GHz, so high-frequency performance can not be compromised. The slew rate of the input stage has to be very high for acceptable response with large input signals. This is achieved by high operating current and low stray capacitances. It is very desirable to keep both the input bias current and the input offset current very low so that the impedances in the source voltages do not introduce intolerable input voltage errors. It would be possible to use a Darlington-connected input stage to achieve these low currents, but the penalty exacted in offset voltage, offset voltage drift, and propagation delay is unacceptable, so high current-gain transistors that match extremely well are needed. The problems are thus centered on achieving very well-matched transistors with high beta and high f_T.

As previously mentioned, it is desirable in a comparator to have a wide common-mode voltage range and high power-supply rejection ratio. This is facilitated by using Schottky diodes to clamp the collector-to-collector swings in the first two stages. Schottky diodes can be fabricated simply by making a window in the oxide over the N-type epitaxial layer and using the same evaporated aluminum as is used for the interconnects (see Figure 10). The contact potential between silicon and aluminum causes a potential barrier to the flow of electrons. Making the metal positive lowers this barrier, allowing electrons to pass over it by virtue of their thermal energy. This process is essentially the same as thermionic emission. Since these electrons are majority carriers, Schottky diodes show extremely fast turn-off characteristics, desirable in this application. Why the Schottky diode is so attractive is that the forward voltage necessary to produce a given current may be several hundred millivolts less than that required to produce the same current in a p-n junction diode of about the same size. It can thus be used as a "clamp" to prevent a bipolar transistor from saturating, when connected from collector to base so as to prevent the forward voltage of the collector-base diode from rising to a level sufficient to cause appreciable current flow in the collector-base diode. This is the common application in Schottky TTL circuits.

In the ECL comparator the use is different. Here they are used back-to-back to limit the differential voltage swings between the collectors in both the first and the second stages. Connected in this way the reverse voltage seen by one Schottky diode is equal to the forward voltage drop of the other diode. Because this voltage is so small reverse leakage is not a great problem. In the simple Schottky diode structure, as described above, the reverse leakage is high. Most of this leakage current is generated at the perimeter of the metal, where there is an electric field concentration. In order to reduce this field the metal is extended all around the opening in the oxide, overlaying this oxide. Spacing the metal from the silicon in this way reduces the field and hence the leakage. In applications where low leakage is critical, the use of a P+ guard ring is called for, but this carries with it extra capacitance, so in view of the fact that the reverse voltage is so low the guard ring technique was discarded for this application. Even so, the diodes used in the comparator have low leakage characteristics with a breakdown at about 45V.

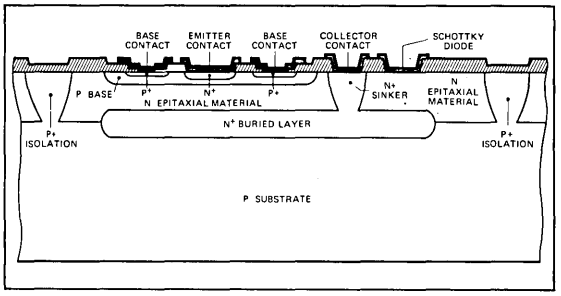


Figure 10. Cross section of transistor and Schottky diode showing sinker and P+ base contact enhancement

At the very high speeds being considered, much effort has to go into reducing capacitances and resistances. Thinning down the epitaxial layer to the minimum required to sustain the voltages encountered is of benefit in two ways: 1) the collector-isolation sidewall area is reduced, lowering the collector-to-substrate capacitance; 2) the collector-series resistance is reduced. The two major contributions to collector-series resistance are the resistance of the epitaxial material between the emitter and the buried N+ layer, and the resistance of the epitaxial layer between the collector contact and the buried layer. However, the first resistance is subject to reduction by conductivity modulation during operation of the device and thus is less important than the second term. The second term can be made very small by using a "sinker", which is a high concentration N-type diffusion from the surface, through the epitaxial layer, to the buried N+ layer. Contact to the collector is then made to the surface of the sinker. (see Figure 10)

Collector-to-base capacitance is held low by using very small dimensions and by using a relatively high epitaxial layer resistivity. The latter also serves to reduce the collector-to-substrate capacitance. A further reduction in collector-to-base capacitance results from using a shallow, high sheet-resistivity diffusion for the base. However, this raises the base resistance, both because the bulk resistance from the contact to the active base region is increased and because the specific contact resistance is increased. These resistances may be reduced by depositing P+ regions under the base contact areas after the main base diffusion.

A compromise has to be made in selecting emitter width. Large emitters are desirable for V_{BE} matching, but very small emitters are essential for high f_T. A stripe emitter, .25-mil wide and 1-mil long, was chosen as optimum. A difference in width, between two otherwise identical emitters, of .01-mil will be sufficient to cause an offset voltage of 1 mV. From this, it can be seen that the photolithography must be extremely carefully controlled, since the offset voltages of three pairs of transistors are summed to give the total offset of the comparator. Because the emitters are so narrow the normal procedure of making a contact cut inside of the emitter cannot be used. Instead, the emitter oxide is simply dissolved in hydrofluoric acid immediately before the aluminum evaporation in order to expose the emitter. As a consequence, the lateral distance between the metal and the emitter-base junction is very small, being equal to the lateral diffusion of the emitter. This means that the sintering process must be carried out at a temperature lower than is customary in linear circuit manufacture in order to avoid short-circuiting the

emitter-base junction by lateral migration of aluminum. An additional reason for lowering the sintering temperature is to avoid penetration of aluminum down through the emitter and base, causing emitter-to-collector shorts.

The requirement for high current gain, for low input bias currents, necessitates narrow base widths. Emitter-to-collector shorts can be a problem in these shallow, narrow-base structures. The probability of shorting can be minimized by careful cleaning procedures and by proper emitter doping levels. Keeping the emitter doping level low also reduces the magnitude of the "emitter dip" effect, whereby the diffusion coefficient of the boron in the region under the emitter is greatly increased by the lattice strain caused by the emitter, resulting in the running-on of the base under the emitter, making it very difficult to achieve a narrow base width.

An area that is neglected in digital circuit processing, because high beta is not necessary, but which is of major importance in linear processing, is the control of surface conditions. If high current gains are to be realized, both the surface area of the emitter-base-depletion region and the surface recombination velocity must be minimized. The former implies that ionic contamination, such as sodium ions, must be eliminated and that the surface state charge density, Qss, should be made as low as possible. The surface recombination velocity is proportional to the fast surface state density and so can be minimized by making this density very low. These three goals; low ionic contamination, low Qss and low fast surface state density are achieved by using the well known techniques of MOS and linear circuit processing, such as annealing in an inert atmosphere and proper choice of sintering cycle.

In the interests of minimum capacitance, the metal interconnects are designed to be narrower than is usual in linear circuits. Special etching techniques have to be employed in order to reproduce these narrow lines reliably. These lines can be seen in the photomicrograph of Figure 11.

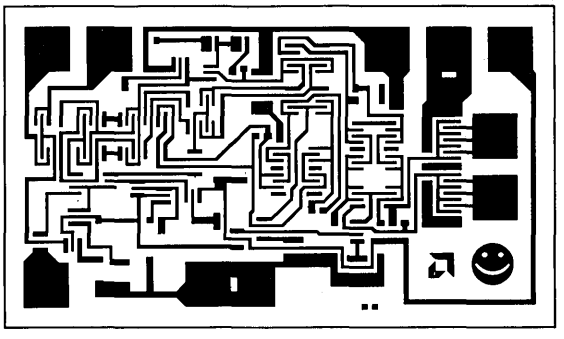


Figure 11. Photomicrograph of the Am685 comparator

PERFORMANCE

The primary design objective for the comparator was to obtain under 10ns propagation delay for large input signals with small overdrive. It should then be as fast or faster for any other input conditions. The performance of the Am685 comparator for a 100mV step input at various overdrives is shown in Figures 12 and 13. The propagation delay is measured from the time the input step crosses the input threshold voltage to the time the output crosses the logic threshold voltage. The input threshold voltage (i.e., the offset voltage) was adjusted for the figures so that the delay can be simply measured by

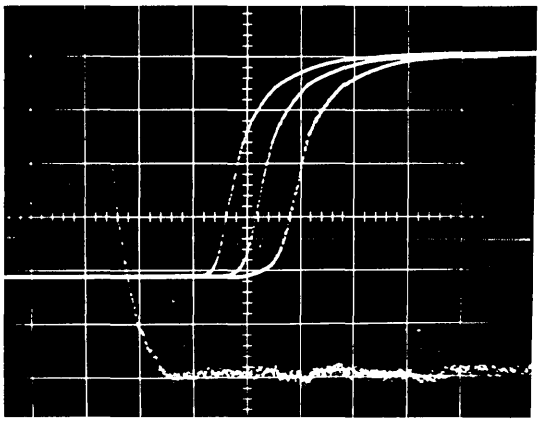


Figure 12. Tpd —"1" for 100mV step input and various overdrives (input = 5mV/cm, output = 200mV/cm)

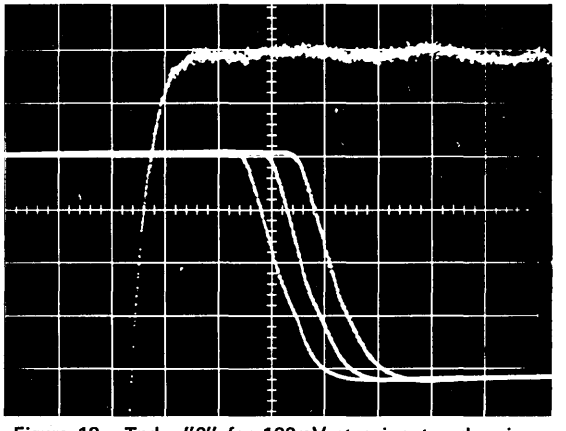


Figure 13. Tpd —"0" for 100mV step input and various overdrives (input = 5mV/cm, output = 200mV/cm)

counting up 5, 10, or 20mV from the bottom of the input pulse. The input pulse, therefore, is displayed on a magnified scale to facilitate this measurement and also to illustrate the purity of input signal required to make accurate measurements at millivolt overdrives.

For a 100mV input step and 5mV overdrive, the propagation delay for a logical "0" is 6.3ns and for a logical "1" is about 300ps less. A graph of delay as a function of overdrive is given in Figure 14. It was previously stated that any other condition

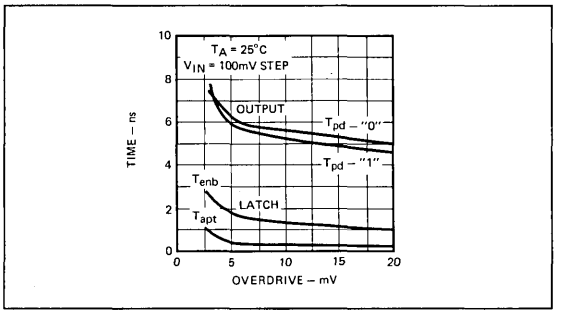


Figure 14. Delay times as a function of input overdrive

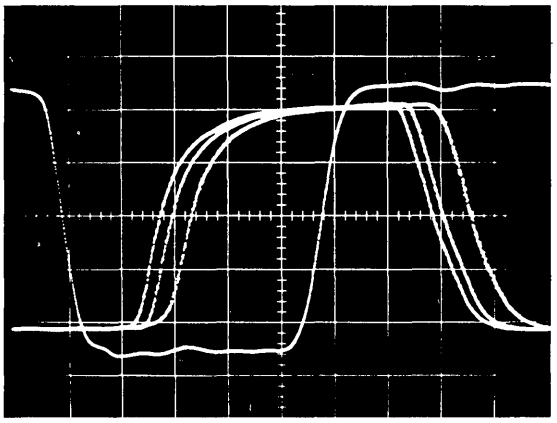


Figure 15. Response to symmetrical input signals

of input signal should give faster response (refer back to Figure 1). This is demonstrated by Figure 15, which illustrates the response of the comparator to symmetrical inputs ranging from ±5mV to ±500mV. The speeds are at least 1 to 2ns faster than for small overdrives.

Figure 16 shows how the delay time varies with temperature. The adverse effects of resistor and gain changes at elevated temperatures result in an increase in delay from 6.3ns at 25°C to 8.4 ns at 85°C and 10.4 ns at 125°C. All of the above data were taken with output loads of 50Ω connected to −2.0V. For lighter loading (such as 500Ω to −5.2V) the output rise and fall times and propagation delays are all slightly faster.

The usefulness of the latch is directly related to how quickly it can be enabled following a change in the input signal. The input signal must be present long enough to pass through the first stage of the comparator before the latching transistors can act upon it. The minimum time that the input must be present before the latch can be turned on is defined as the latch enable time. This is measured as the minimum time that must elapse

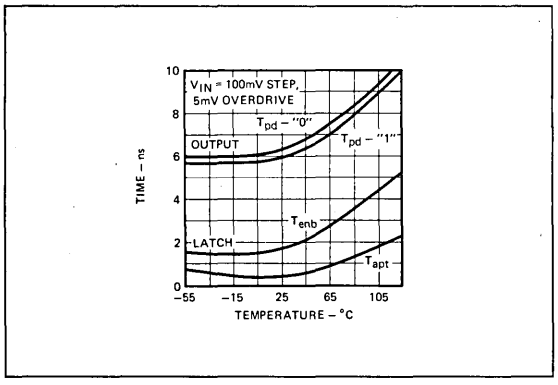


Figure 16. Delay times as a function of temperature

between the time the input step crosses the input threshold voltage and the time the latch enable input crosses the logic threshold voltage for which the comparator outputs will assume the correct states.

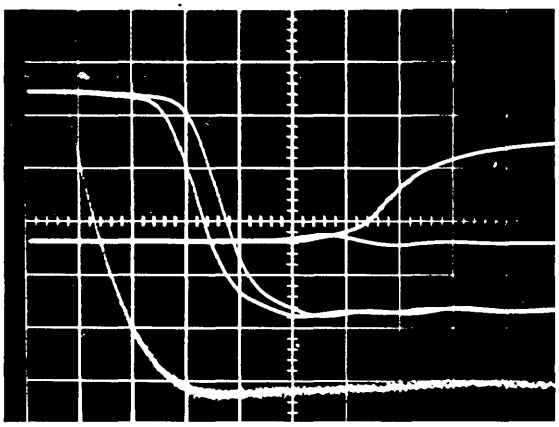


Figure 17. Latch enable time and latch aperature time for 100mV input step, 5mV overdrive (input = 5mV/cm, latch = 200mV/cm, output = 400mV/cm)

The performance of the latch function is illustrated by Figure 17. The input signal is the standard 100mV step with 5mV overdrive and is in the direction to cause the output to switch from a logical "0" to a logical "1". The delay of the latch signal relative to the input is adjusted until the output just switches to a "1"; this is the latch enable time and under these conditions is 1.8 ns. The difference between the latch timing for which the output just barely switches and when it does not switch is the latch aperture time; this is about 500ps for 5mV overdrive. The performance of the latch with input overdrive and temperature generally follows that of the propagation delays (Figure 14 and 16).

The overall performance of the Am685 is summarized in Table II. It is apparent from the table and the previous discussion that the device is ideally suited for applications where both precision and high speed are required, such as in analog-to-digital converters, data acquisition systems, and optical isolators. The device is the first in a family of new wideband linear integrated circuits designed to meet the requirements of very high-speed systems.

Propagation Delay (100mV step, 5mV overdrive)	7.5ns MAX
Input Offset Voltage	2.0mV MAX
Average Temperature Coefficient Of Input Offset Voltage	10μV/°C MAX
Input Offset Current	1.0μA MAX
Input Bias Current	10μA MAX
Common Mode Voltage Range	±3.3V MIN
Common Mode Rejection Ratio	80dB MIN
Supply Voltage Rejection Ratio	70dB MIN
Positive Supply Current	22mA MAX
Negative Supply Current	26mA MAX

Table II: Performance Characteristics of the Am685 Comparator (T_A = 25°C, V^+ = 6.0V, V^- = −5.2V, R_L = 50Ω to −2.0V)

LINE DRIVERS AND RECEIVERS

By R. C. Ghest, Digital Applications

INTRODUCTION

A familiar problem in digital systems is data communication between various peripheral units. Digital information must be reliably transmitted and received at high speed with a minimum of interconnections and components. Different pieces of equipment often have different ground systems, which are quite possibly at different potentials, and the interconnection is usually in a high-electrical-noise environment. Standard integrated circuit logic gates can be used for data transmission over short distances, but if the interconnection is fairly long they will severely limit the data rate and introduce errors. These errors are caused by the inability to match the circuit impedances correctly to the transmission line, and because standard logic gate circuits do not have sufficient immunity to the large amounts of noise present in practical systems. Even so-called "high-noise immunity" logic is not designed to transmit to and receive data from transmission lines and is susceptible to cross-talk and ground noise.

The criteria for a digital communication system are: Reliable operation in a high-electrical noise environment; ability to match into transmission lines to reduce line reflections; reasonable power consumption; high data rate and ease of use.

SINGLE ENDED

The simplest communication link consists of a driver with a single output driving a line and a receiver with a single input and a common ground path. This method of communication, called single-ended, has the disadvantage that the current supplied by the driver after traveling down the line returns through the common ground together with other system currents. These other currents couple noise into the transmission link and could cause errors at the receiver. The problem can be somewhat overcome by having a low-impedance ground or by using several ground returns.

Over short distances standard or high-noise immunity logic gates can be used for driving and receiving, but for longer distances circuits specifically designed for the task should be used. The advantages of single-ended operation over differential operation are simplicity and low cost. In many applications with a little care and attention a single-ended system forms an acceptable communication link. Figure 1 shows a typical single-ended system with the data strobed both at the receiver and the driver.

DIFFERENTIAL

Many of the requirements outlined for a reliable communication link indicate that a differential system should be used. A differential system can be designed to operate reliably over large distances in the presence of considerable electrical noise. Differential communication systems can be balanced or unbalanced.

BALANCED DIFFERENTIAL SYSTEM

A balanced differential communication system consists of a driver that accepts a logic input signal and provides complementary output signals that can drive a balanced two-wire transmission line; the transmission line and a differential receiver, which accepts the complementary signals from the line, ignores noise common to both lines and provides a replica of the original signal to following logic. This method of communication is shown in Figure 2a.

Provision is made at the receiver and/or driver to match the line impedance so that unwanted reflections do not generate noise, dissipate power or cause erroneous switching. Generally the differential receiver has a high-input impedance relative to the line impedance, and, therefore, appears to the line like an open circuit. External components can then be used to terminate the line from a variety of methods available.

The logic signals are often strobed at the driver and receiver, and the AC response of the receiver is often adjustable in order to suit the noise environment and provide a large AC noise immunity.

UNBALANCED DIFFERENTIAL SYSTEM

Often it is convenient to use a differential system that is unbalanced. The most common unbalanced system is single-ended. A single-ended system has signals traveling along one wire with a second wire used as a ground return. Complementary signals are not necessary, the driver is less complicated than for a balanced system, and several signal wires can share a common ground line. The number of wires in a multichannel, single-ended system is therefore one half the number necessary in a balanced system. Figure 2b shows an example of an unbalanced, single-ended differential communication system. A differential single-ended system gives protection from noise common to the signal and ground line, but is

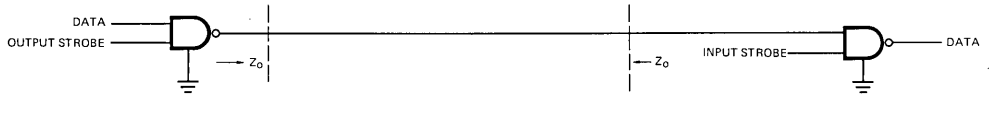


Figure 1. Single Wire With Common Ground

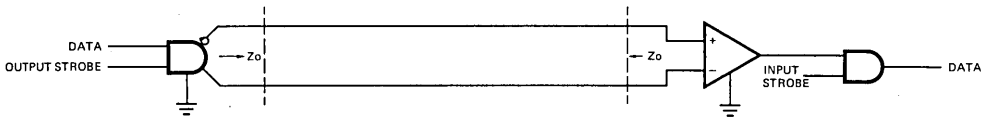


Figure 2a. Two Wire Balanced System

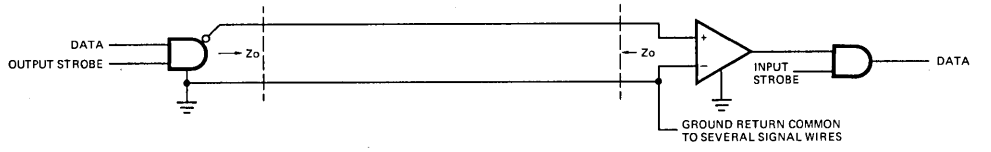


Figure 2b. Single Wire With Common Ground Unbalanced System

sensitive to noise injected unequally into the signal and ground wires. Another disadvantage is that inductive coupling between signal lines is increased by the presence of a common ground return. These disadvantages must be weighed against the considerable hardware and cost savings of an unbalanced system with common ground over a completely balanced system.

MATCHING

It is important in a digital communication system to have the minimum amount of noise generated by undesired reflections at the driver and receiver. There are numerous ways of matching to the line. The line can be matched at the driver, at the receiver or both, each method has advantages and disadvantages. Generally for any but the longest lines it is sufficient to match at one place, and only when there are discontinuities in the line, party line operation, or lack of a reasonable match at the opposite end of the line is the extra hardware of matching at both ends justified. The majority of transmission lines have fairly low characteristic impedances (in the range of 50 to 200 ohms) and the currents involved for a reasonable voltage swing are quite large. It is more difficult to couple noise into this low impedance, but it is also more difficult to drive, and line drivers must have the ability to supply large currents.

Various matching techniques that can be employed are shown in Figure 3. These impedance charts are useful in showing what happens to wave fronts traveling down a line, when the line delay is longer than the wave front transition. The DC input characteristic of the receiver, including any external components, is plotted on the V-I graph together with the output characteristic of the driver, including any external components used at the driving end. There are always quiescent points—points where the driver and receiver characteristics cross. These points represent the DC voltage/current conditions, which must eventually be satisfied. To determine the effect of switching from one quiescent point to the other, a line with a slope equal to the characteristic impedance of the transmission line is plotted, starting at the initial quiescent point and ending at the applicable output impedance characteristic. The point of intersection gives the voltage and current at the output of the driver (and the input of the transmission line immediately after the driver switches states). From this point a line having an equal but opposite slope is drawn to the input characteristic and, at the intersection shows the voltage/current conditions of the wave front at the input of the receiver. This procedure is repeated to the output characteristic and so on at each intersection of the characteristic, the voltage/current relationship for a particular reflection is given. The resulting time/voltage relationships for the traveling wavefront at the two ends of the transmission line are shown alongside.

From the graphs several important features can be seen. If the line is not matched at either end considerable transient voltage swings can occur. In fact if the input and output characteristics are at right angles to one another, the reflections continue for an infinite time if the line is assumed to have zero loss. Most lines have extremely low losses, and, therefore, a very undesirable situation exists if the line is not matched at either end.

If the line is matched at the receiver, a voltage wave of constant amplitude travels down the line and is absorbed at the termination. Note whether the line is terminated to ground or to the power supply the system consumes DC power, either in the HIGH logic level or in the LOW logic level. In order to reduce the power dissipation, a blocking capacitor can be used in series with the receiver termination. The capacitor can be chosen to look like a short circuit to the voltage wavefront but stop DC (current) flow. Since the capacitor must be charged and discharged through the line, the data rate is reduced, when this technique is employed.

If the line is matched with a series resistor at the driver, then the line input initially rises to one half the final voltage. This wave front travels down the line and is reflected at the receiver. When the reflection reaches the driver the voltage at the driver rises to its final amplitude. The receiver, however, sees one transition from the initial to the final amplitude. When the driver switches from HIGH to LOW a similar situation occurs, in which the input of the line sees at first a step to one half the final value and, two line delays later, the final LOW condition. This back matching mode of operation consumes no DC power if the input impedance of the receiver is infinite. The advantage of the method is that if the input impedance of the receiver is high, very little power is dissipated and current only flows during the transition time, which is twice the line delay time. If back matching is used in a balanced system the terminating series resistance must be divided into two equal resistances with resistors inserted in series with each wire in order to maintain a balanced system.

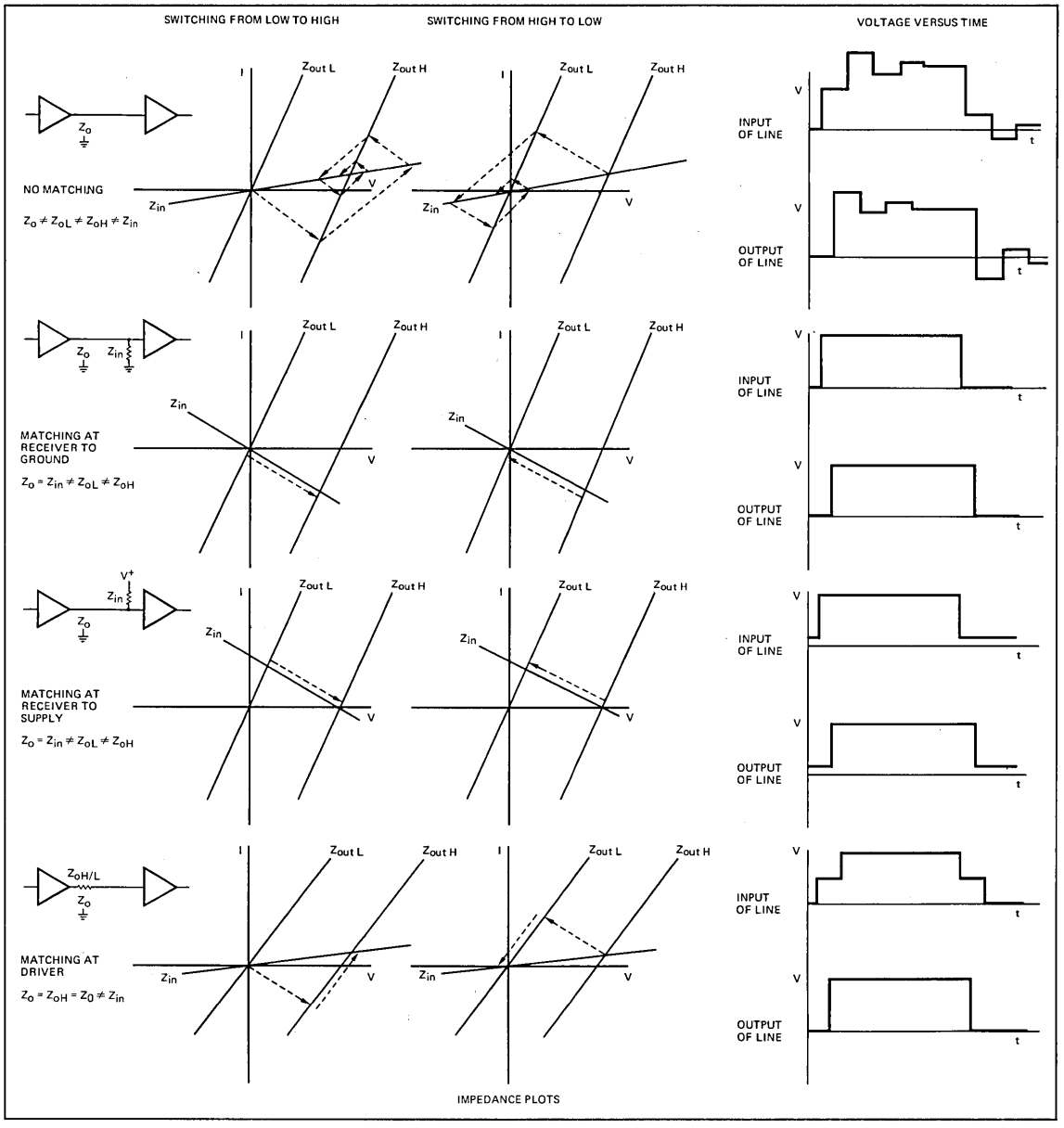


Figure 3. Line Matching Methods

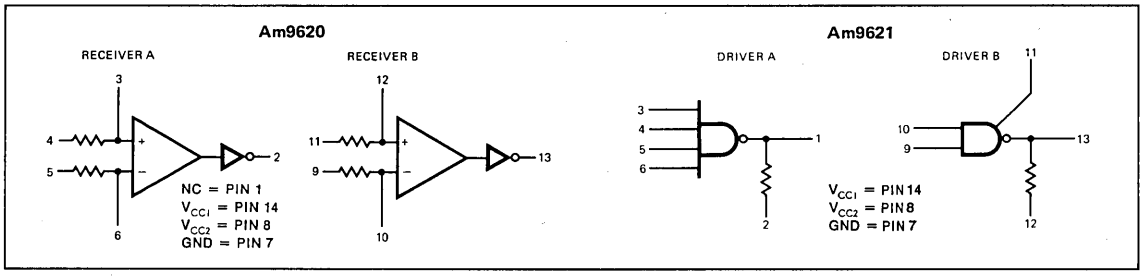


Figure 4. Logic Diagrams and Pin Numbers of the Am9620 and Am9621

THE Am9620 DUAL LINE RECEIVER AND Am9621 DUAL LINE DRIVER

The Am9620 and Am9621 are first generation devices specifically designed for differential digital transmission line systems. The devices can be used in either balanced or unbalanced systems. With these devices a transmission system can be designed that is immune to up to 15 volts of noise injected into the lines. This common-mode noise rejection makes the devices suitable for applications in which the noise level is high and the ground systems are at different potentials. Logic symbols and pin numbers are shown in Figure 4. In addition to the normal +5 volt supply an auxiliary +12 volt supply is required.

THE Am9620 RECEIVER CIRCUIT

The Am9620 dual differential line receiver is designed to receive differential data from transmission lines and deliver reshaped TTL logic signals at the output. The circuit diagram is shown in Figure 5. It consists of four parts: An attenuator, used to provide good common-mode noise rejection, a differential amplifier, a constant current source for the amplifier and an inverting output buffer.

The receiver accepts signals either through the input attenuator or directly at the inputs of the amplifier. A 500 mV differential between the attenuated inputs causes the output of the receiver to assume the corresponding TTL logic level. Up to ±15 volts of common-mode voltage is permitted on the two input signals. If the direct inputs are used only an 85 mV input difference is required, but the common-mode range is reduced. The output of the differential amplifier drives an inverting buffer to give a TTL level output, which can be AND tied for multiplexing purposes.

THE Am9621 DRIVER CIRCUIT

The Am9621 is a dual high fan-out inverting buffer that can be used to drive either balanced or unbalanced transmission lines. The circuit diagram is shown in Figure 6.

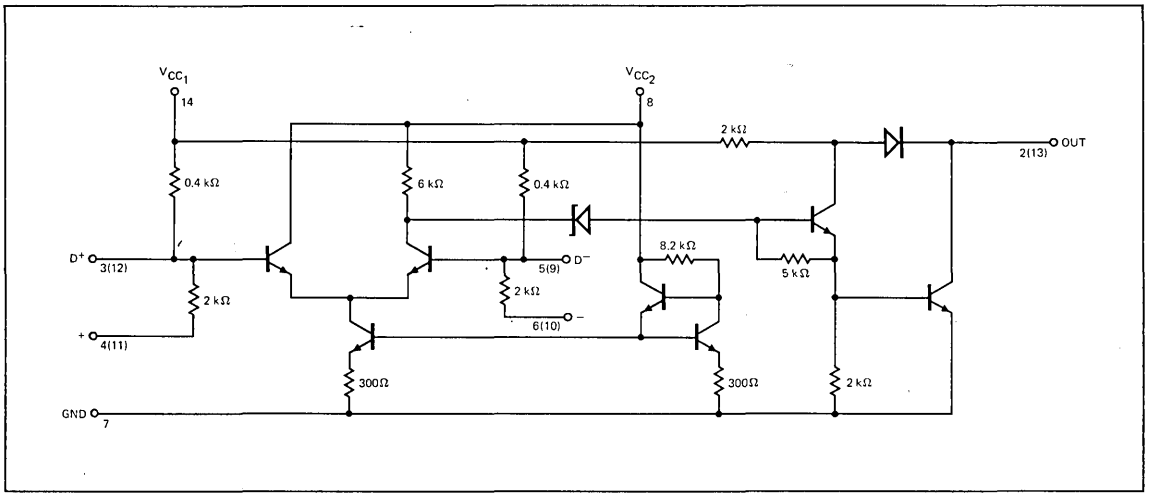


Figure 5. Am9620 Differential Receiver Circuit

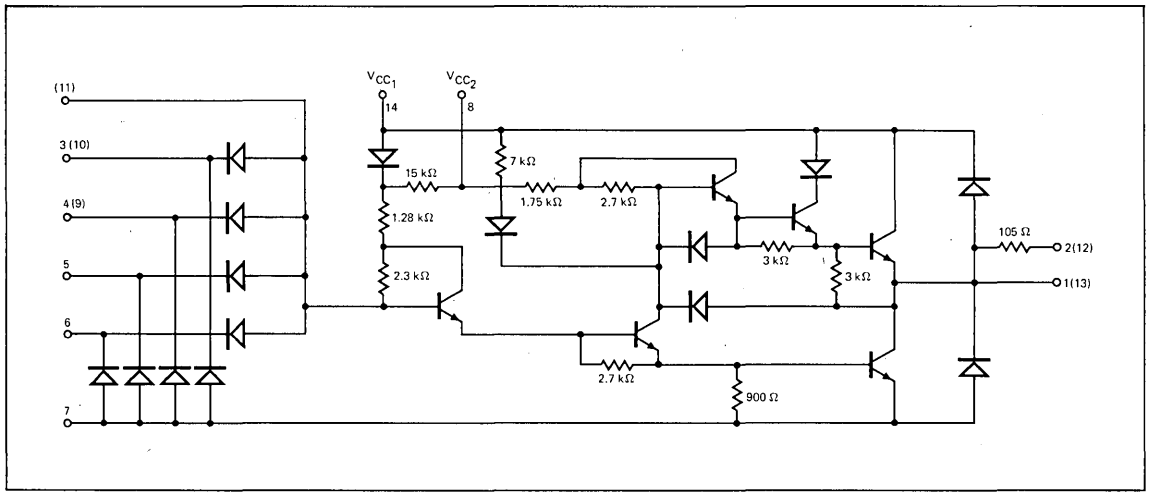


Figure 6. Am9621 Line Driver Circuit

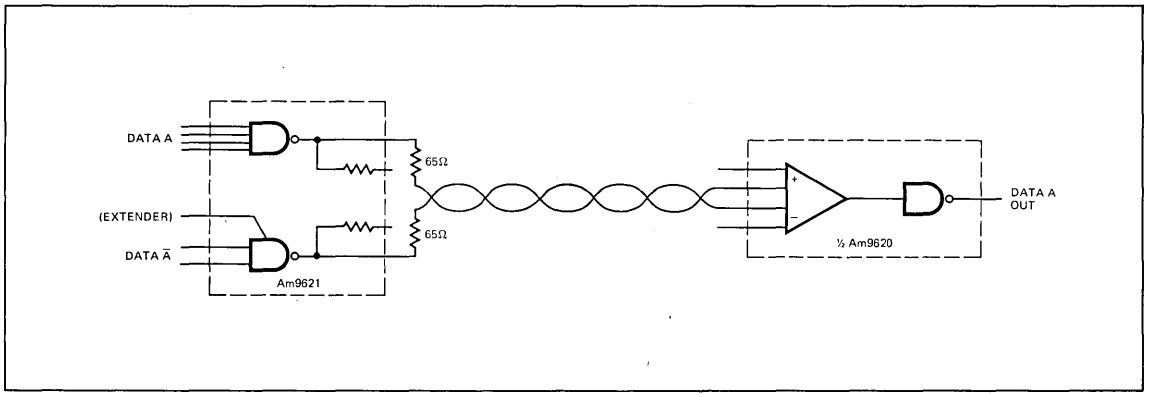


Figure 7. Am9620 and Am9621 Used in Balanced Differential Mode with Back-Matching

Z_o	R_M when used single ended	R_M when used differentially
50Ω	32Ω	16Ω
75Ω	62Ω	30Ω
92Ω	82Ω	41Ω
100Ω	90Ω	45Ω
130Ω	120Ω	60Ω
300Ω	290Ω	145Ω
600Ω	590Ω	295Ω

TABLE I BACK MATCHING FOR THE Am9621

One of the drivers has four logic inputs, and the other has two inputs plus an input extender pin. Both drivers have two outputs, a direct output and an output through a 130Ω (±25%) series resistor. This resistor output allows the driver to match into 130Ω twisted pair lines in the single ended mode.

The circuit consists of a conventional DTL gate that drives an active pull-up output. This output stage uses the +12 volt supply to give a large drive capability and noise margin in the HIGH logic level. The output is clamped by diodes to V_{CC} and ground in order to give a low impedance in all conditions of operation and limit line reflection transients.

COMMUNICATION SYSTEMS USING THE Am9620 AND Am9621

A balanced transmission line communication system is shown in Figure 7. In the balanced mode both drivers in the Am9621 must be used and are driven from complementary sources. One driver can be driven from the other, but this method has the disadvantage of introducing delay between the complementary signals, which can cause momentary erroneous switching at the receiver. (This noise can be screened by altering the input response of the receiver with external components.) The system incorporates back matching at the driver.

The signals from the driver travel down the line, are reflected at the effective high-impedance inputs of the receiver, and return to the driver where they are absorbed in the series impedance. This method of matching has the advantage of consuming only AC power as no DC component is present in the signals on the line.

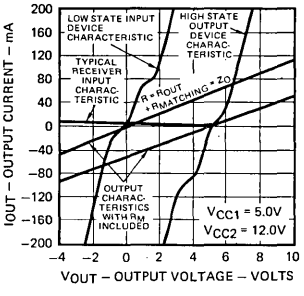


Figure 8. Am9620-Am9621 Impedance Chart

Figure 8 shows the input impedance of the Am9620 and the output impedances of the Am9621 in its two logic states with and without the internal resistor. This chart can be used to estimate the signal reflections occurring in a system by plotting the line impedance as illustrated in Figure 4.

When the Am9620 is used in an unbalanced system the input threshold of the differential amplifier is set at a level half-way between the two output levels of the driver in order to give a differential noise margin. This is done by biasing the negative input of the amplifier with a voltage source.

THE Am9614 DRIVER AND Am9615 RECEIVER

The Am9614 dual differential line driver and Am9615 dual differential line receiver (shown in Figure 9) are second generation elements designed to transmit and receive digital information over balanced transmission lines. The main difference between these and the Am9620 and Am9621 is that they use only a single +5 volt power supply and still provide common-mode rejection in a system of ±15 volts.

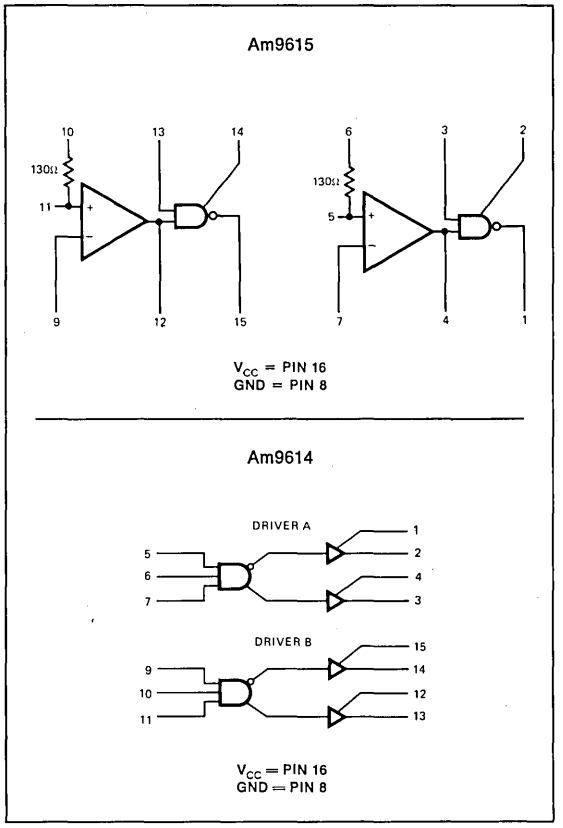


Figure 9. Logic Diagrams and Pin Numbers of the Am9614 and Am9615

The dual driver consists of two 3-input AND gates driving output buffers, which have complementary outputs. Each of these complementary outputs is split into an active pull-up output and an active pull-down output. The differential receiver has 5kΩ input impedance and provides ±15 volts of common-mode rejection. The receiver requires a 500 mV differential signal at the input in order to establish the correct logic level at the output over this common-mode range. Each receiver includes a 130Ω resistor, which can be used to terminate twisted pair lines. A response control input is available so that the AC response of the receiver can be adjusted to suit the particular system requirements. The output of the amplifier drives an inverting buffer, which has the active pull-up and pull-down circuits split and brought out on separate pins.

THE Am9614 DRIVER CIRCUIT

The Am9614 circuit is shown in Figure 10. Each driver consists of a 3-input TTL AND gate with input clamp diodes and complementary buffer outputs. Each buffer output is split into an active pull-up output capable of sourcing 10 mA at 2.4 volts, and an active pull-down output, which can sink 40 mA at 0.4 volts. The two outputs of each buffer can be connected to give a low-impedance output at both logic levels. The output impedance of the driver is low and approximately the same at both logic levels to allow good back matching characteristics.

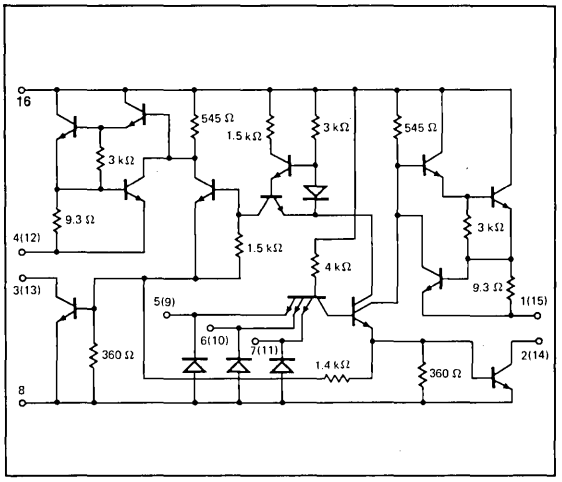


Figure 10. Am9614 Differential Line Driver Circuit Diagram

THE Am9615 RECEIVER CIRCUIT

The Am9615 circuit is shown in Figure 11. The receiver consists of: (1) an input attenuator used to improve noise rejection by decreasing the voltage seen at the inputs of the differential amplifier. The attenuator is designed to give a ±15 volt common-mode rejection with a single +5 volt supply and, to limit the voltage seen by the input transistors of the amplifier. A 130Ω terminating resistor is available at the input of the attenuator; (2) a two-stage differential amplifier that takes the attenuated signals and produces an amplified signal to drive the output buffer; (3) a temperature-compensated current source; (4) an output buffer which produces TTL logic levels. The active pull-up and active pull-down circuits are brought out to separate pins for multiplexed operation. A strobe input and frequency response control are also provided.

COMMUNICATION SYSTEMS USING THE Am9614 AND Am9615

The normal method of using the devices is in a two-wire balanced system. Various techniques are available for matching the circuits to the line. The most widely used, although not the most efficient in terms of power dissipation, is to match the line at the receiver with a terminating resistor equal to the characteristic impedance of the line. A blocking capacitor is sometimes used to stop DC current flow and to reduce power dissipation. A better method is to back match at the driver by placing a resistor in series with the line. Table II gives the value of series resistors required for optimum matching into lines of different characteristic impedance. These values take into account the output impedance of the driver. The impedance curves for the devices are shown in Figure 12.

In many systems several drivers are multiplexed onto a single transmission line to save cost. Drivers can be multiplexed, as shown in Figure 13, by having all the active pull-up outputs of the non-inverting buffer drive one line and all the active pull-down outputs of the complementary buffer drive the other line. Since this configuration provides a low-impedance drive to only one logic level, some method must be used to correctly define the other logic level. Pull-up and pull-down resistors can be used at the receiver, but this causes large

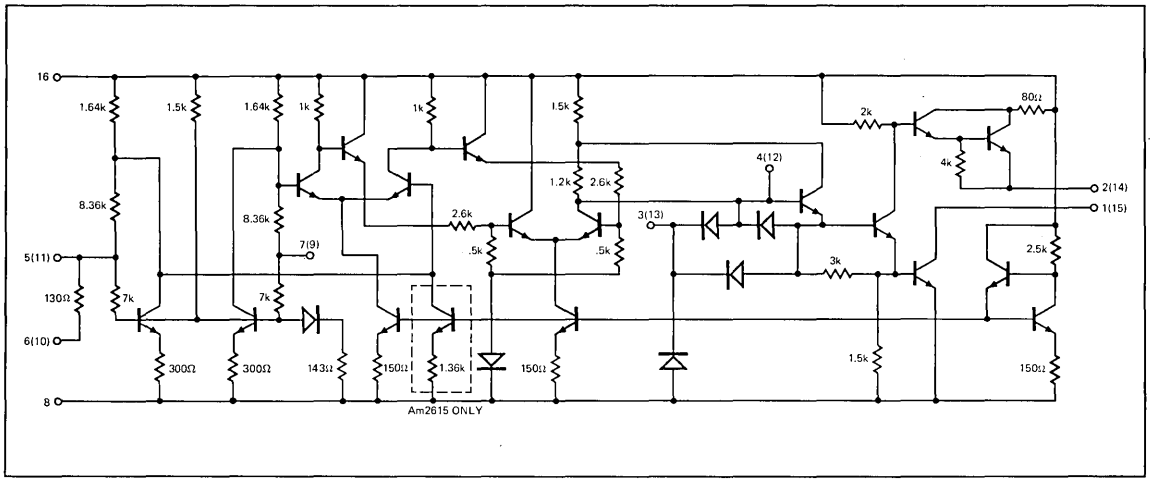


Figure 11. Am9615/Am2615 Differential Line Receiver Circuit Diagram

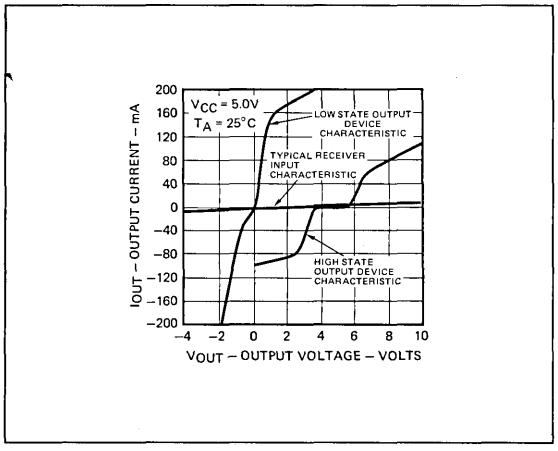


Figure 12. Am9614/Am9615 Impedance Chart

Z_o	R_M when used single ended	R_M when used differentially
50Ω	24Ω	12Ω
75Ω	51Ω	24Ω
92Ω	68Ω	33Ω
100Ω	75Ω	36Ω
130Ω	110Ω	54Ω
300Ω	280Ω	140Ω
600Ω	580Ω	290Ω

TABLE II BACK MATCHING FOR THE Am2614/Am9614

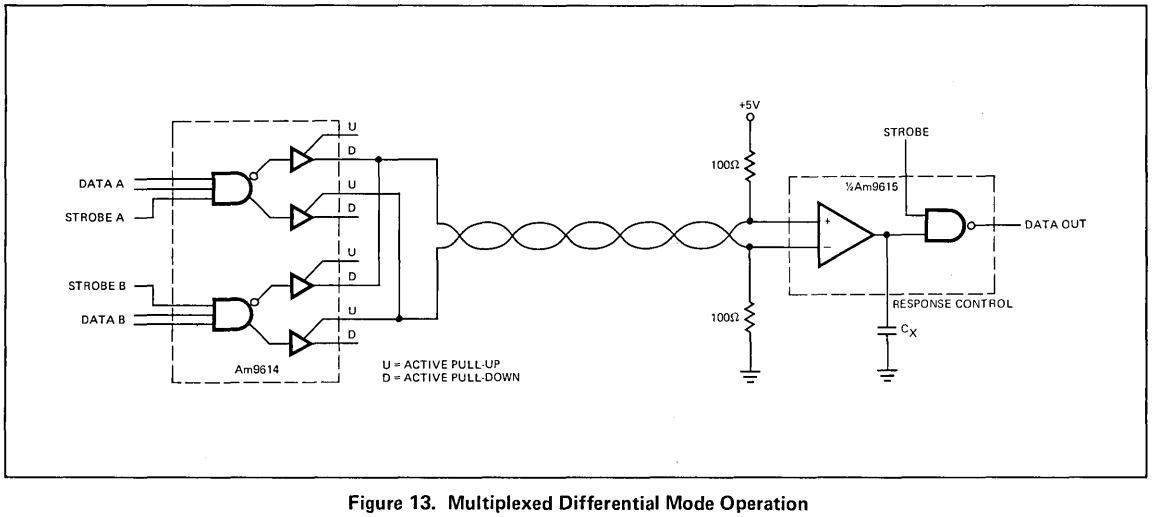


Figure 13. Multiplexed Differential Mode Operation

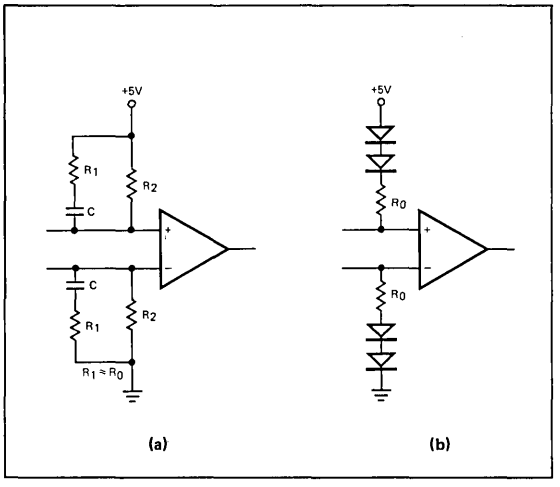


Figure 14. Am9615 Receiver Termination Methods When Multiplexing

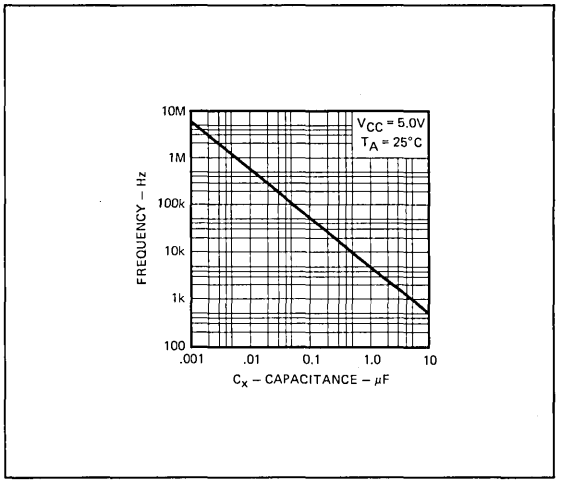


Figure 15. Am2615/Am9615 Receiver Cut-off Frequency External Capacitance

power dissipation, so some compromise is generally made between speed, power and DC noise margin. Figure 14 shows two alternate methods that can be used. In (a) the line is terminated in its characteristic impedance but with only a small DC current flow through R_2; (b) the voltage swing at the termination is reduced by the clamp diodes. The worse case DC noise margin of the balanced system is 1.5 volts at both logic levels. The AC noise margin can be adjusted at the response control input with an external capacitor to ground. Figure 15 shows the relationship between cut-off frequency and capacitor value. Input noise at frequencies above the cut-off frequency and pulses of duration less than $1/f_C$ will not cause changes in the receiver output.

THE Am2614 DRIVER AND Am2615 RECEIVER

The Am2614 and Am2615 are circuits designed for unbalanced differential communication systems. The driver is a quad high-speed, high fan-out buffer suitable for driving low-impedance transmission lines. The receiver is a dual differential device that has an input threshold mid-way between the standard TTL logic levels. Otherwise the receiver is identical to the Am9615 receiver.

The devices use a single +5 volt supply and give reliable communication with up to ±15 volts of common-mode noise.

THE Am2614 CIRCUIT

The Am2614 quad line driver consists of four high fan-out TTL NAND gates with active pull-up outputs. Each driver has provision for strobing the incoming data and can source 10 mA of current in the HIGH logic level, and sink 40 mA of current in the LOW logic level. The driver can be used as a high-speed buffer for logic applications as well as for line driving.

THE Am2615 CIRCUIT

The Am2615 is the only TTL compatible line receiver available that can accept single-ended data from a transmission line and give ±15 volts of common-mode noise rejection. The difference between this circuit and the Am9615 is that the differential threshold of the Am2615 is set at 1.5 volts, mid-way between the TTL logic levels, by biasing internally the differential amplifier.

UNBALANCED DIFFERENTIAL SYSTEMS USING THE Am2614 AND Am2615

The Am2614 and Am2615 circuits can be used in an unbalanced system with a separate ground wire for each channel or with a ground wire shared between a number of channels. In an unbalanced ground-return the only penalty paid is a reduction in differential noise margin to 800 mV. The advantage of half as many drivers as in a balanced system often justifies this reduction.

In an unbalanced system with a common ground, a four-channel system uses only three IC packages and five wires as against four ICs and eight wires for the balanced system. The common ground must be interlaced with the signal wires to ensure that any injected noise is common to all wires. Any unbalance will cause differential voltages.

The common ground is used at the negative input of each receiver, but the receiver ground is not connected to the common ground since it may be at a completely different potential. The main problem with an unbalanced system is that differences in potential are caused by: (1) DC currents that are summed in the common ground and cause a differential voltage drop at the input of the amplifiers. This difference voltage is usually small unless considerable DC currents are flowing down the lines; (2) AC currents that also add and cause voltage differences at the inputs of the amplifiers. These AC currents often can be quite large particularly if a low-impedance transmission line is driven. This current causes an induced voltage in all the signal wires, the amplitude of which is dependent upon the mutual inductance and capacitance between the lines, and the self inductance of the line. The effect is difficult to analyze for more than two signal wires, but as the number of signal wires which share a common ground is increased the induced voltages become larger, and can cause erroneous switching of the differential line receivers. The duration of the induced noise is a function of the transition times of the transmitted signals, and can be screened out by suitable choice of capacitor at the response control input of the receiver. In practice it is often convenient and satisfactory to split a multi-channel system into groups of eight channels with a separate ground wire for each group of eight channels, and either use a capacitor to remove any AC noise caused by

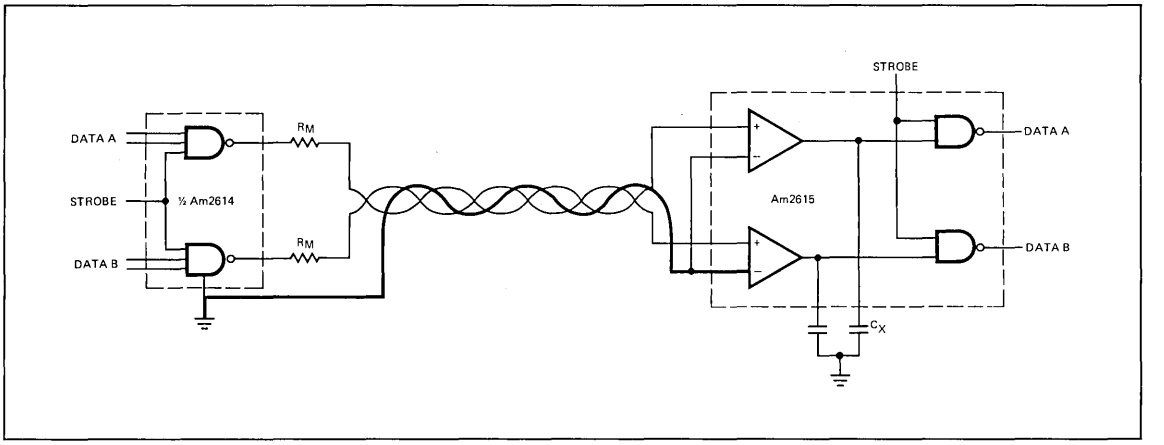


Figure 16. Single Ended Back-Matched Operation With Common Ground

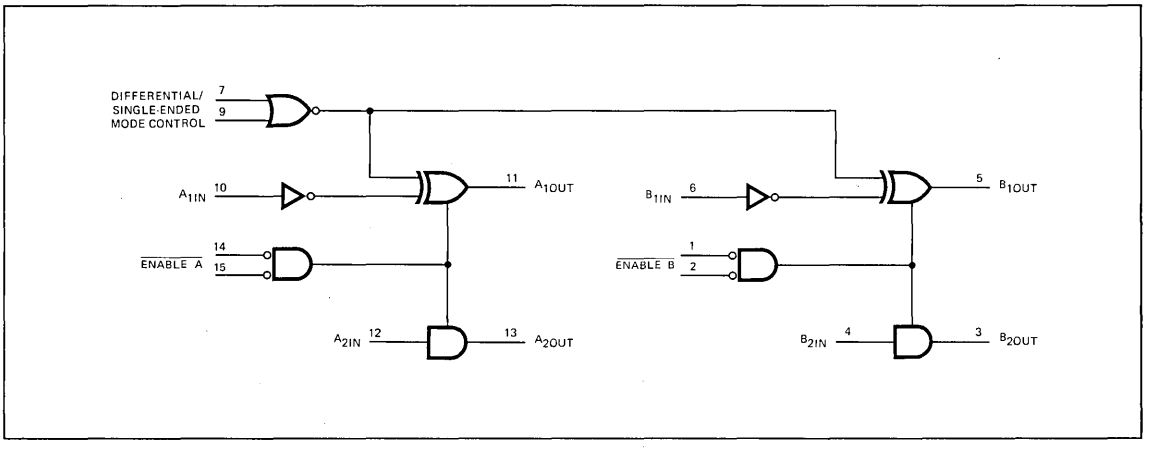


Figure 17. Am78/8831 Logic Diagram

sharing the common ground, or strobe the receivers at an appropriate time.

Figure 16 shows a typical unbalanced system with the signal wires sharing a common ground and the ground wire interlaced in with the signal wires.

THE Am78/8831 PARTY LINE DRIVER

The Am78/8831 is a party-line driver that can be used for either single-ended or differential operation. The device has a two-input NOR gate control that determines whether it is to be used as a quad single-ended driver or a dual differential driver. The four outputs of the device have a three-state capability so that outputs can be connected to a bus for multiplexed operation and yet still keep a low impedance drive at both logic levels. The output of a driver can act as a source and a sink of large currents for driving into fairly low impedance lines, and can also be disabled into a third HIGH impedance state with the output loading the line with just a small leakage current.

The logic diagram of the device is shown in Figure 17. A two-input NOR gate controls the mode of operation by switching exclusive OR gates on each pair of drivers. The four drivers are split into pairs of two, and each of these pairs can be operated independently by means of a two input active low AND Disable/Enable gate.

When used for single-ended operation the two differential/single-ended control inputs are held LOW. The device then operates as four independent non-inverting drivers. For differential working at least one differential/single-ended control input is held HIGH. The A-channel inputs are connected together and the B-channel inputs are connected together. Single inputs will then pass non-inverted to the A_2 and B_2 outputs and inverted on the A_1 and B_1 outputs.

For party-line operation outputs of different channels are tied together, and outputs of all channels except one are forced into the third high impedance state by having at least one of the channel disable inputs HIGH. The channel that is enabled has both channel disable inputs LOW, and the low-output impedance of this output at both logic levels controls the level of the bus, provides good capacitance drive and insures good waveform integrity.

The channel which is enabled can conveniently be selected by a decoding matrix using Am9301 1-of-10 or Am9311 1-of-16 active LOW output decoders. The high drive capability at

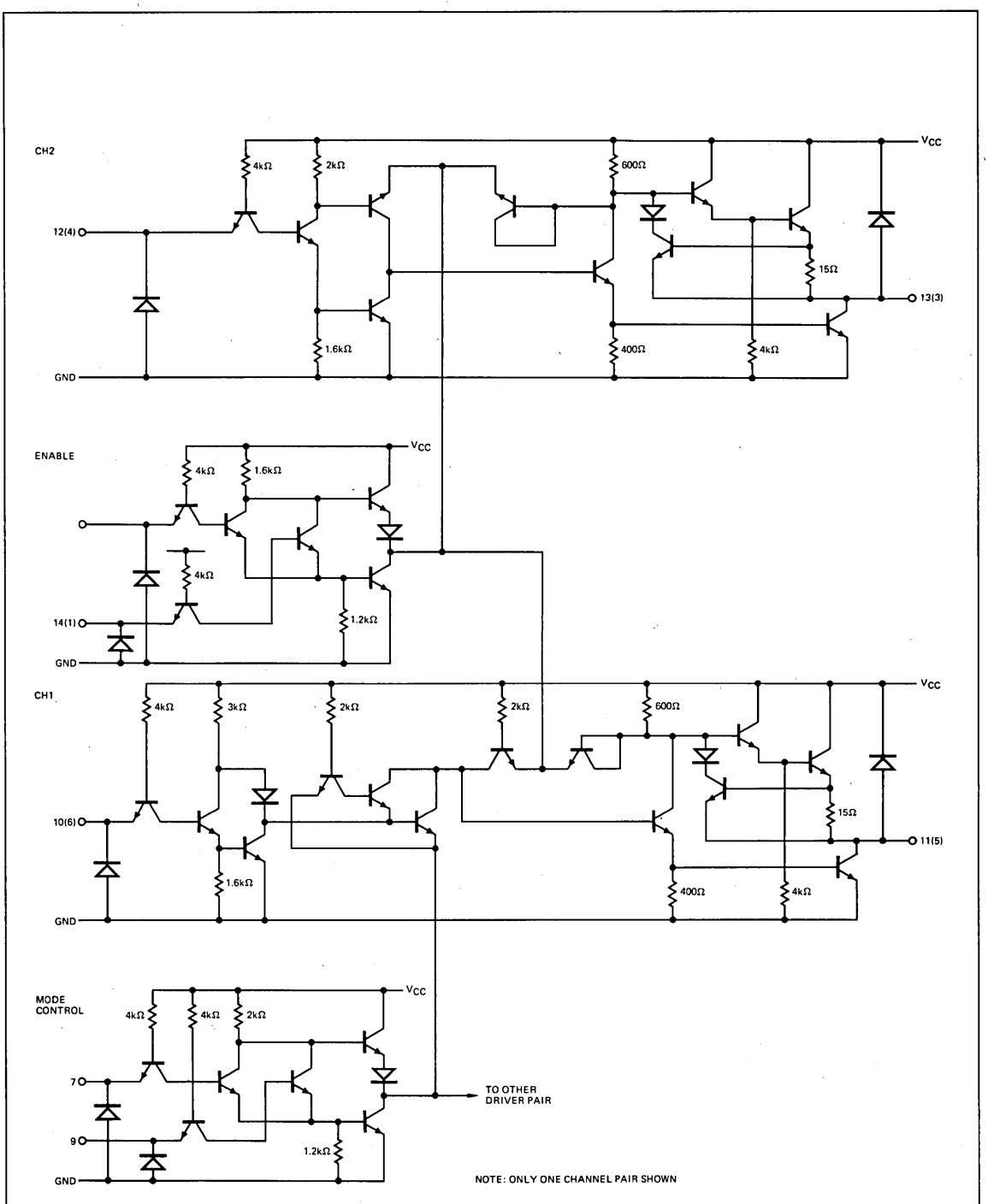


Figure 18. Am78/8831 Party Line Driver Circuit Diagram

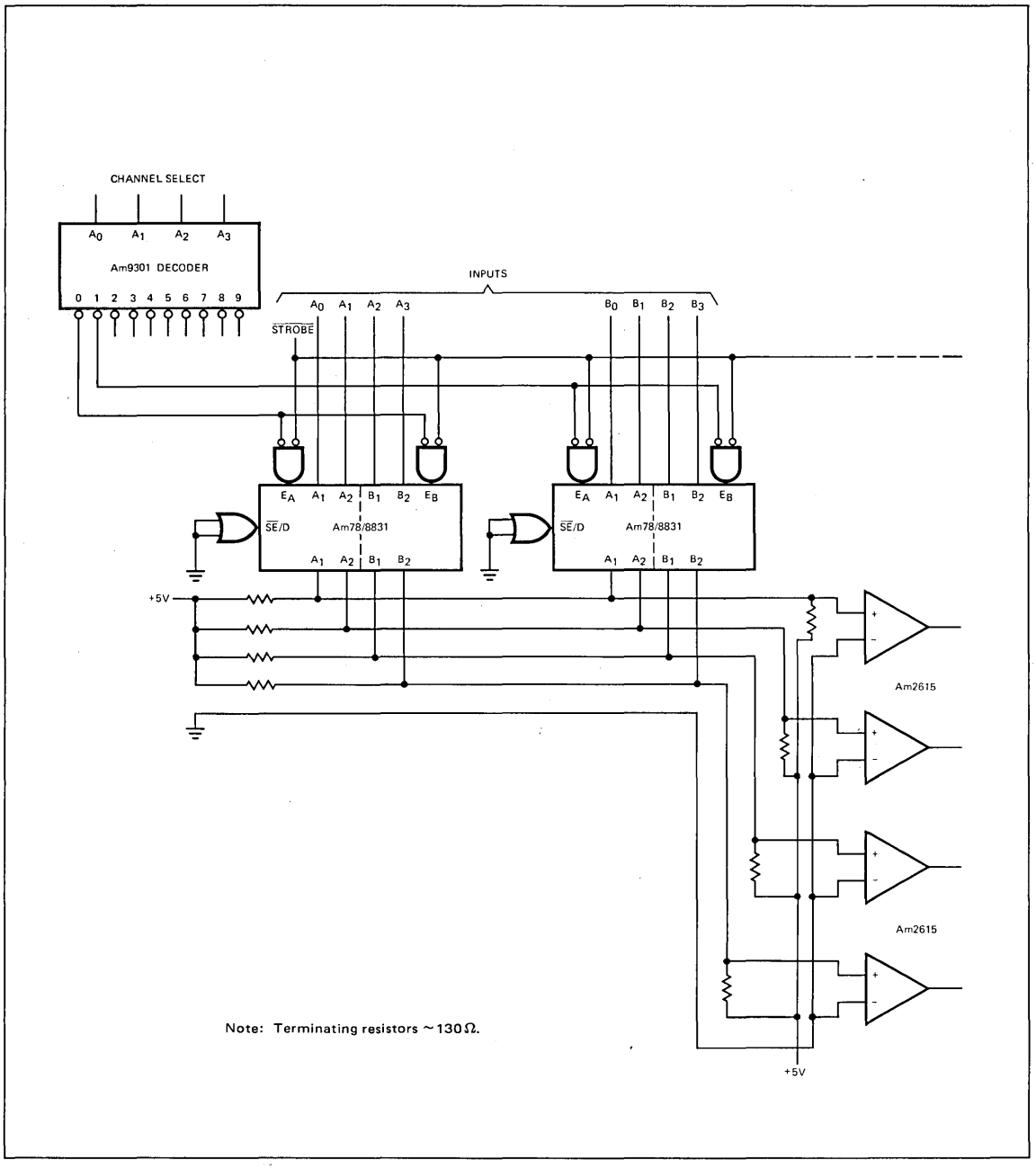


Figure 19. Quad Single-Ended Operation With the Am9615 Differential Receiver

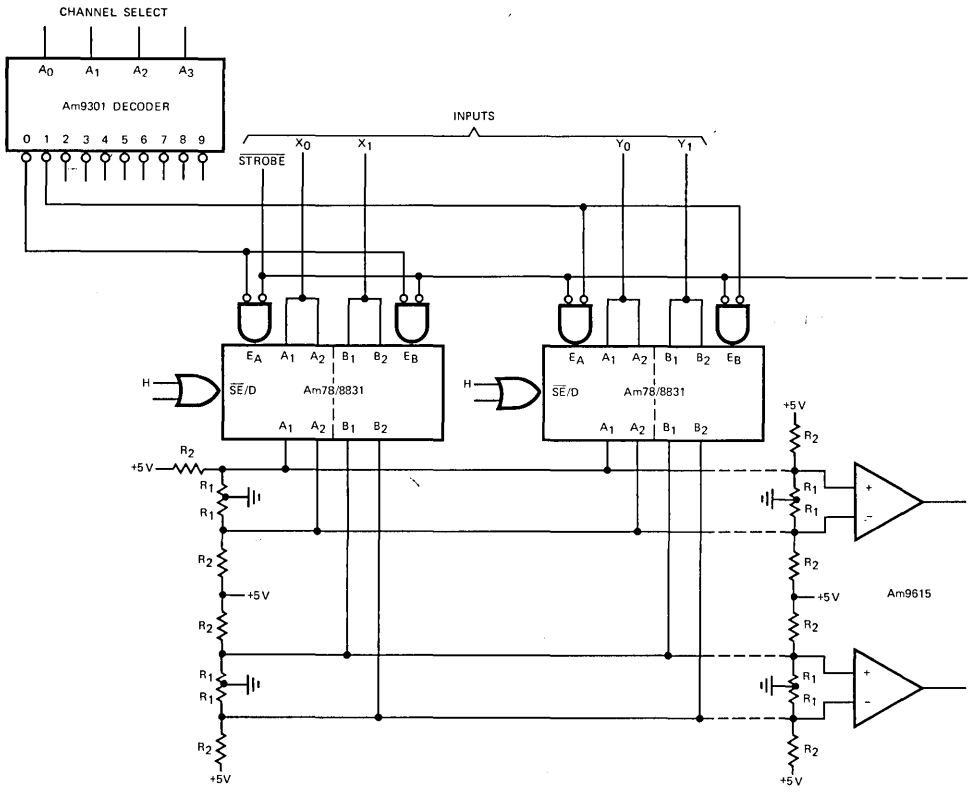
both logic levels enables drivers to drive a low impedance line and still supply the inverse leakage current of several disabled drivers.

The circuit diagram of the Am78/8831 is shown in Figure 18. The mode control gate is a conventional TTL NOR gate with diode pull-up. The output of this gate controls the polarity of the channels A_1 and B_1 through an exclusive OR circuit. The outputs of the drivers have emitter follower active pull-up's so as to present a low impedance in the HIGH logic level. The output has a short circuit current limiter and a clamp to the V_{CC} supply. The enable circuit consists of conventional TTL gate, which when enabled pulls down the collector of the phase splitter of the driver output and also cuts off the phase splitter so that both the active pull-up and pull-down circuitry are cut-off and only leakage current flows into the output. In this high impedance state the voltage level of the driver output is determined by external circuitry connected to the output.

APPLICATIONS OF THE Am78/8831

The Am78/8831 is very useful in party line systems. The driver outputs can be connected together onto a data bus and the driver outputs controlled by an active LOW decoder. Figure 19 shows the Am78/8831 in a single-ended party line system with four parallel data busses. The ideal receiver for such a system is the Am2615 since it gives common-mode noise rejection for a single-ended system. A single ground wire is used together with the four data lines and this ground wire used to establish the level at the negative input of the differential receivers. The party lines can be terminated at both ends so that undesirable reflections do not interfere with correct operation and a good differential noise margin is maintained. A driver that is some distance from both terminations sends out signals in both directions and the unwanted signal is absorbed in the termination.

The device can also be used in a differential mode as shown in Figure 20. The diagram shows a two channel differential party line system using the Am9615 dual differential receiver. The mode control of the Am78/8831 is held HIGH forcing the Channel 1 outputs of the devices to be the inverse of channel 2. The party line is terminated at both ends so that undesirable reflections are eliminated. This differential party line system will allow an extremely efficient system which is very insensitive to both differential and common mode noise.



Note: The R_{in} equivalent is 130Ω at 2.8 volts.

Figure 20. Dual Differential Operation Using Am9615 Differential Receiver

APPLICATION OF FIRST-IN FIRST-OUT MEMORIES

By John Springer, Digital Applications

The Am3341/2841, Am2812 and Am2813 are asynchronous first-in first-out memories using P-channel silicon gate MOS technology. All use the same fundamental storage mechanism, but are organized differently. The Am3341/2841 contains up to 64 four-bit words; the Am2812 holds up to 32 eight-bit words; the Am2813 holds up to 32 nine-bit words. All devices can easily be expanded to hold either more words or wider words. The Am2841 is functionally identical to the Am3341, but is faster. The logic symbols for these devices are shown in Figure 1.

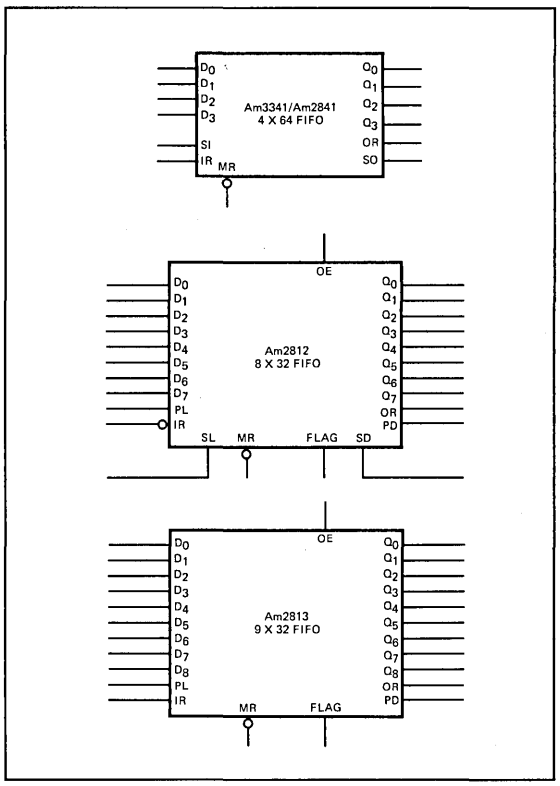


Figure 1. Logic Symbols

THE FUNCTION OF A FIRST-IN FIRST-OUT MEMORY

A first-in first-out memory (FIFO) is a read/write data storage unit that automatically keeps track of the order in which data was entered into the memory, and reads the data out in the same order. It behaves like a shift register whose length is always exactly equal to the number of words stored. The most common application of a FIFO is as a buffer memory between two pieces of digital equipment operating at different speeds. Such an application is illustrated in Figure 2, where machine 1 might be a relatively slow electromechanical input device and machine 2 might be a digital computer (or vice-versa). Data is frequently handled in a configuration like this by having machine 1 generate an interrupt requesting service from machine 2 every time a data word is available. If machine 1 transmits only a single word infrequently then the interrupt-oriented approach is reasonable, but if machine 1 is going to transmit 20 or 30 words, then the interrupt approach is inefficient. As each of the words becomes available, an interrupt must be generated, machine 2 must react, cleaning up its active processing, locate the interrupt, store the new data word, and return to its active processing only to receive another interrupt milliseconds later.

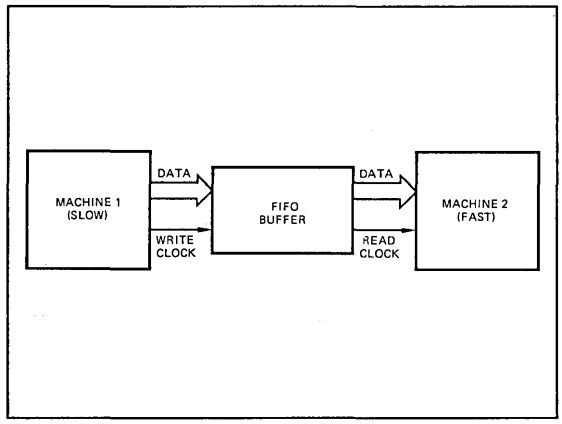


Figure 2. Asynchronous Interface between Two Digital Machines

An alternative processing method is cycle stealing on a direct memory access (DMA) channel. In this configuration the system is designed so that machine 1 has direct access to the memory of machine 2. As data becomes available from machine 1, it is inserted into machine two's memory during time periods when machine 2 is not using the memory. This method is fairly efficient, especially for transfer of large blocks of data from a disc or tape, but it also can result in interference with the active processing of machine 2 due to contention for the memory channel.

The most efficient way to handle the interface between these two machines is by using a special memory between the machines to temporarily store the data from machine 1 until machine 2 is ready to accept it. The memory must be large enough to store all the data that machine 1 might generate in-between services by machine 2, and should be able to write the data at the speed of, and under control of, machine 1,

while reading the data at the speed of machine 2. An extremely useful feature in such a memory is the ability to perform read and write operations at the two different rates simultaneously and completely independently. This allows machine 1 to write new data into the memory at the same time that machine 2 is reading data from the memory without requiring any kind of synchronization between the two.

METHODS OF CONSTRUCTING FIFO BUFFERS

There are a number of ways in which FIFO memories can be built. The design becomes trivial if there is no requirement for independent reading and writing. The data can be written into a shift register, for example, which is clocked by machine 1. When a block of data has been written, the register can be shifted until the first data word is available at the output, and then shift control can be handed to machine 2, which shifts the data out as required. This method requires that data transfer occur in blocks only, since once the data has been shifted to the output, a new word cannot be written until the last block has been completely read.

A somewhat more flexible FIFO can be built using a random access memory with counters used to generate the read and write addresses. A multiplexer is used to select the appropriate address counter for a read or write, and the counter is incremented at the end of the cycle, so that the next read or write will occur at the next counter address. Since the location of the next read and write are held in independent counters, reading and writing can be randomly intermixed. However, using an ordinary RAM, only one operation can be performed during a given cycle, since only one address can be selected at a time.

If the RAM is very fast relative to the machines using it, then the control logic can be designed to receive read and write requests independently and to execute them so quickly that the FIFO buffers appear to operate completely asynchronously. In the general case, this means the RAM cycle time must be less than half the cycle time of machines 1 or 2. This is necessary so that the buffer can perform alternate read and write operations at the maximum speed of both machines. The control logic to do this is fairly complex and requires an independent clock running at more than twice the frequency of machine 1 or 2.

The problem of handling read and write operations simultaneously is alleviated if a 2-port RAM is used. Such a device (e.g., the Am9338) has two independent sets of address inputs, one for reading and one for writing, so no synchronizing of read and write requests need occur. Unfortunately, two port RAMs are limited to small numbers of bits, and, therefore, are fairly expensive to use in a FIFO of reasonable size.

The Am3341/2841, Am2812 and Am2813 are totally integrated solutions to the problem of asynchronous FIFOs. A special unique control system is integrated into the device to make possible completely independent reading and writing. Because the control and data storage are intimately mixed on one LSI chip, a very efficient, cost-effective FIFO can be constructed. The three devices, all of which use the same basic control scheme, are organized into three different configurations to provide optimum flexibility for all applications.

STORAGE AND CONTROL IN THE Am3341/2841, Am2812 AND Am2813

The Am3341/2841, 64 x 4 FIFO will be used to explain the storage technique. A similar scheme is used in the Am2812 32 x 8 FIFO and Am2813 32 x 9 FIFO. A logic block diagram of the Am3341 is shown in Figure 3. Data words are stored in 64 four-bit registers, connected so the output of one feeds the input of the next. Note that if all 64 registers were clocked together, the device would look like a quad 64-bit shift register. FIFO operation is performed by clocking each register independently so that data can be selectively shifted through the registers. To shift or not to shift: that is the decision which must be made independently by each of the 64 registers. The decision is made by examining a control flip-flop associated with each register to determine if that register contains valid data or not.

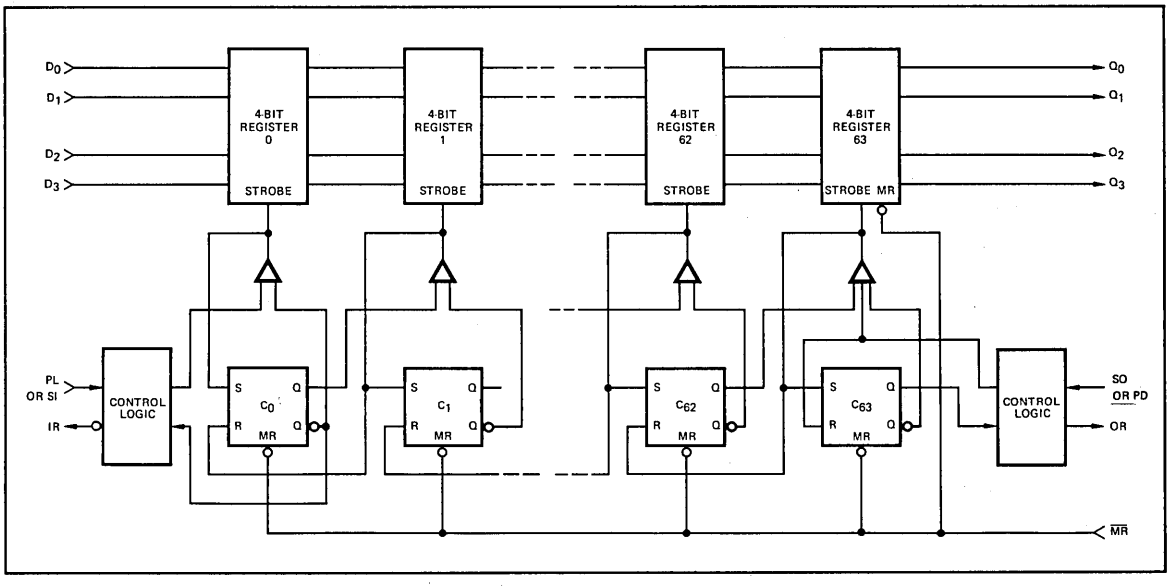


Figure 3

Initially, the FIFO is reset and there is no data anywhere in it. The control flip-flops are all reset to "0." A write command causes a 4-bit data word to be entered into the first register and sets the control flip-flop for that register, indicating valid data is present. The control flip-flop for the second register is a "0" and this causes it to continually examine the control flip-flop for the first register, looking for a "1." When the data is written into the first register, the second register sees the "1," and a clock is generated to it, copying the data from the first register into the second, setting the control flip-flop for the second register, and clearing the control flip-flop for the first register. In exactly the same fashion, the third register copies the data from the second, and the fourth from the third until finally the data ends up in the last location. At this point all 64 registers contain the same data, but only the last control flip-flop contains a "1," the others all having been reset as the data was copied into the next register.

As soon as the data moves from the first register to the second, the control flip-flop for the first register is cleared. A new data word can then be written into the first register. The first control bit is brought out as "input ready" (IR), and data can be entered anytime it is HIGH. When the data has been accepted, IR goes LOW (a "1" in the control bit) and when the data moves to the second register, IR goes HIGH again. The new data falls through the registers as long as there are "0s" in the corresponding control flip-flops. Eventually it reaches the register immediately behind a register already containing data. Since the control bit for that register is already a "1," the data is not moved any further and remains stacked up behind the existing data. A read command on the output causes the last control flip-flop to be cleared, creating a new empty location. The next to the last word is copied into the last word and the hole in the control register moves back toward the input as the data words move down one place. This process can continue until all data has been shifted out of the memory. When the last word has been read the external signal output ready (OR) remains LOW, indicating no more data is available.

This scheme allows the reading and writing of data to occur completely independently and even simultaneously. Data can be written into the device as rapidly as the device is capable of moving it away from the first register; it can be read at the same rate. The only constraint imposed by this scheme is that a certain amount of time is required for the first data word to propagate to the end of the register. This time is referred to as the "ripple-through" time and is the internal shift time multiplied by the number of bits from input to output.

CONTROL SIGNALS TO THE Am3341/2841 AND Am2813

There are four signals used with the Am3341/2841 and Am2813 to control the reading and writing of data. These are parallel load (PL, or SI on 3341), input ready (IR), parallel dump (PD or SO on 3341) and output ready (OR).

The two outputs, IR and OR, are derived from the state of the first and last control flip-flops, respectively, and are used to indicate the presence or absence of data at the input and output of the FIFO. When IR is LOW (that is, input not ready) then there is data residing in the first data register. New data may not be entered until this data has moved to the second register, indicated by IR going HIGH. The OR signal goes HIGH whenever valid data is present on the FIFO output. Whenever a shift-out command is received, OR goes LOW while the data is being changed. If there is no more data, OR stays LOW, indicating the memory is empty. Otherwise OR returns HIGH as soon as the new data is on the outputs. Data is entered into the FIFO by a LOW-to-HIGH transition on shift-in (PL), while IR is HIGH. The fact that both these signals are HIGH causes a strobe to the first data register to be generated, loading the data on the data inputs into register and setting the first control flip-flop. When the control flip-flop is set, IR goes LOW, indicating the data has been accepted. The input data can be changed after IR has gone LOW. When SI is then brought LOW, the data is transferred to the next register (unless there is already data there) and IR goes back HIGH, indicating that the input is ready to receive more data. If the memory is full, then the data in the first register will not move to the second, and IR will stay LOW. Once data moves into the second register, it falls spontaneously through the FIFO until it stacks up behind data already present.

Data in the last FIFO location is presented on the data outputs. While data is there, OR is HIGH. The next data word is obtained by applying a LOW-to-HIGH transition on shift-out (SO). This results in OR going LOW. The data does not actually change until SO is brought LOW again. The new data, if any, will be brought to the output and, after the data is stable, OR will go HIGH again. If the memory is empty, OR will remain LOW until a new word falls through from the input. Note that anytime OR is HIGH, there is good, stable data on the outputs.

MASTER-RESET

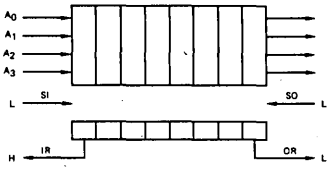
The master reset pin ($\overline{MR}$) is used to clear all data from the FIFO. When it goes LOW, all the control flip-flops are cleared and the output buffer is cleared. IR will be forced HIGH during this time. When the $\overline{MR}$ signal is removed the FIFO is ready to accept new data. Note that if SI is held HIGH as the master reset ends, then both SI and IR will be HIGH, resulting in immediate entry of the data on the data inputs into the FIFO. If this is not desired, then SI should be held LOW during the master reset and until new data is ready to be entered.

EXPANSION METHODS USING THE Am3341/2841

The four control signals on the Am3341 have been designed so that devices can be directly connected end-to-end, as in Fig. 6, and can thereby control each other. When data appears at the output of the first device OR goes HIGH. This causes an SI command to the second device which in turn causes IR to go LOW. Since IR is connected to SO, this causes a shift-out at the first device, driving OR LOW until new data is available, and the process repeats. Lengthening of the FIFO stack requires only this simple interconnection.

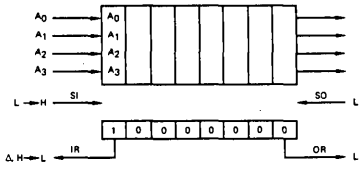
To make a wider FIFO devices are simply operated in parallel. Since each device is autonomous there need be no interconnection between paralleled devices, except that all the shift-ins at the front are connected together and all the shift outs at the end are connected together. Data then ripples independently through each row of FIFOs.

1



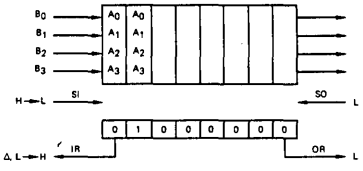
INITIAL CONDITION
FIFO empty, SI LOW IR HIGH, word "A" on inputs.

2



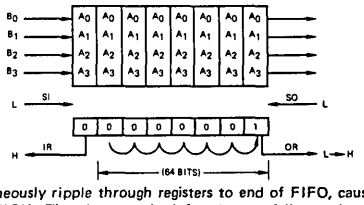
Write input into first stage by raising SI. (Δ = delay) IR goes LOW indicating data has been entered.

3



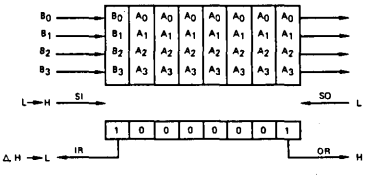
Release data into FIFO by lowering SI. After delay, data moves to second location, and IR goes HIGH indicating input available for new data word.

4



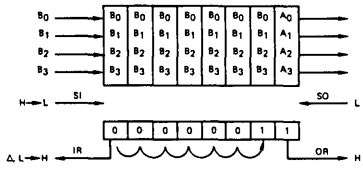
Data spontaneously ripple through registers to end of FIFO, causing OR to go HIGH. The time required for data to fall completely through the FIFO is the "Ripple-through Time".

5



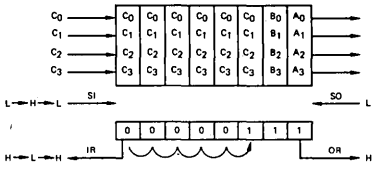
Word "B" written into FIFO

6



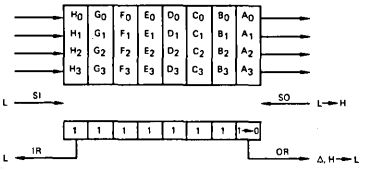
SI goes LOW allowing word "B" to fall through.

7



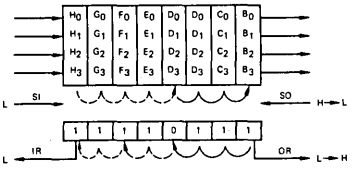
Word "C" written in same manner, and so on. When buffer is full, all control bits are 1's and IR stays LOW.

8



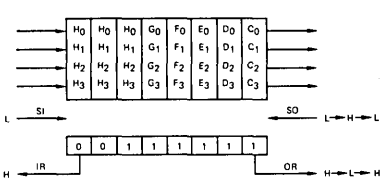
FIRST READ OPERATION
SO goes HIGH, indicating "Ready to Read". OR then goes LOW indicating "Data Read".

9



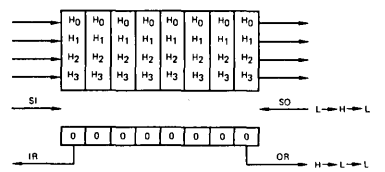
When SO goes LOW, the "0" in the last control bit bubbles toward the memory input. OR goes HIGH as the new word arrives at the output. IR goes HIGH when "0" reaches input.

10



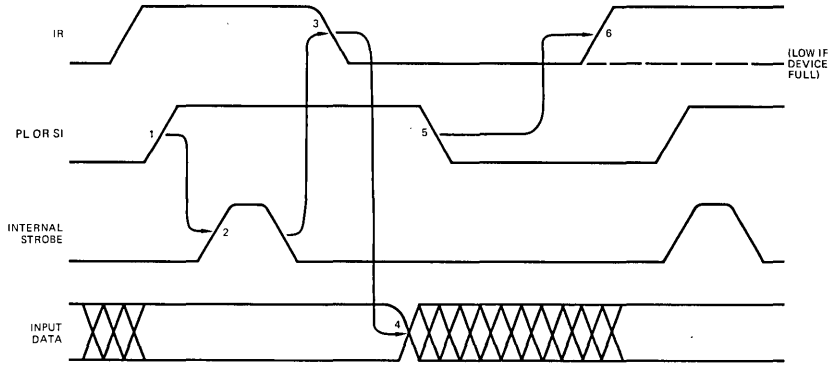
Read word "B" out, word "C" moves to output, and so on.

11



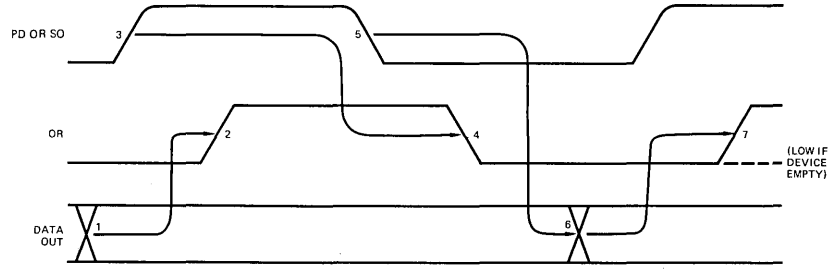
Read word "H". OR stays LOW because FIFO is empty. Word "H" remains in output until new word falls through.

Figure 4



INPUT TIMING SEQUENCE, Am3341/2841 AND Am2813

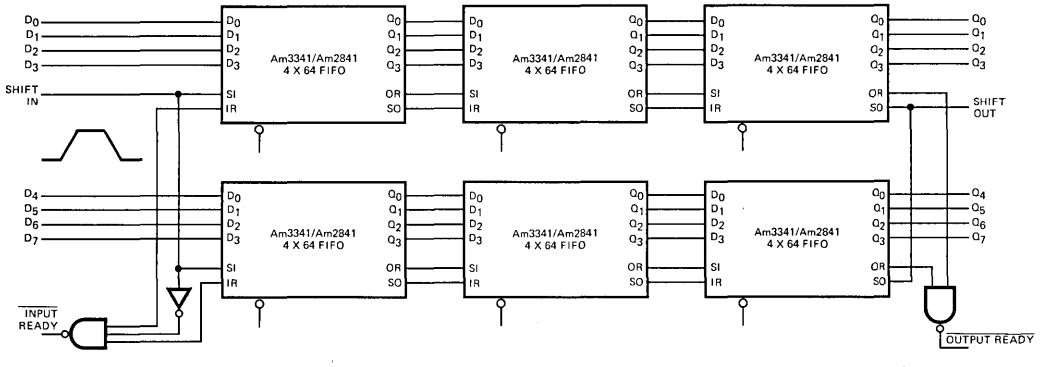
SI is brought HIGH (1) causing internal strobe (2) which loads data. When data has been loaded, IR goes LOW (3) indicating data can be changed (4). SI may then be brought LOW (5) causing IR to return HIGH (6).



OUTPUT TIMING SEQUENCE, Am3841/2841 AND Am2813

Data out changes (1); then OR goes HIGH (2). When SO goes HIGH (3), OR goes LOW (4) indicating data is about to change. After SO goes LOW (5) the data actually changes (6) and after it is stable, OR goes HIGH again (7).

Figure 5



The composite input ready indicates both devices are ready to receive data. The shift in pulse must be wide enough for all devices to load data under worst case conditions.

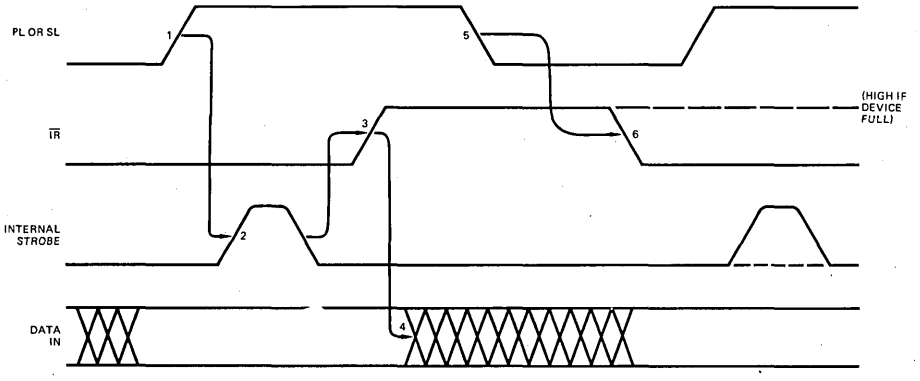
Figure 6. 8 x 192 FIFO Buffer Using Am3341/2841

CONTROL SIGNALS ON THE Am2812

The Am2812 is controlled exactly like the Am3341 and Am2813, except that the input ready signal is inverted. Internally operation is like the Am3341/2841. The control signals are slightly different, however, and there are some additional features. There is a parallel load (PL) input, used to

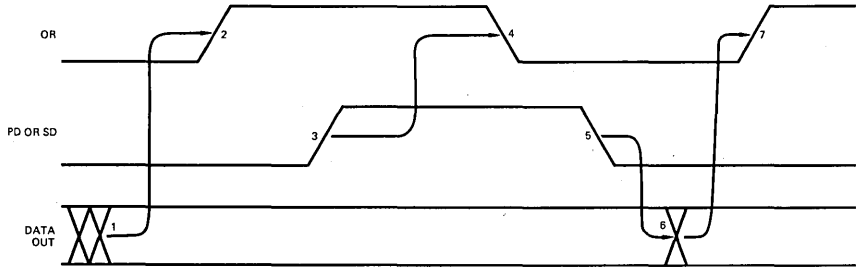
load an 8-bit word onto the first stage of the FIFO, and an input ready output ($\overline{IR}$) which indicates that the FIFO is ready to receive a new data word. At the output, there is a dump command (PD), used to bring the next data word to the outputs, and an output ready signal (OR) which indicates that good data is available on the data outputs.

Data is loaded into the first FIFO location by a LOW-to-HIGH word is present at the output, OR (output ready) will be HIGH. The next data word is shifted onto the outputs by a pulse on parallel dump (PD). When PD goes HIGH, the OR signal goes LOW, indicating that output data is about to be changed. When PD then goes LOW, the output data changes with the word behind the outputs moving onto the outputs. When the new output data has stabilized, OR will go HIGH indicating that good data is once again available on the FIFO outputs. If the PD pulse emptied the FIFO, then the OR signal will remain LOW and the last word read will remain on the outputs until a new data word falls through from the front of the FIFO.



Am2812 INPUT TIMING

When data is steady, PL or SL is brought HIGH (1) causing internal data strobe to be generated (2). When data has been loaded, $\overline{IR}$ goes HIGH (3) and data may be changed (4). $\overline{IR}$ remains HIGH until PL is brought LOW (5); then $\overline{IR}$ goes LOW (6) indicating new data may be entered.



Am2812 OUTPUT TIMING

When data out is steady (1), OR goes HIGH (2). When PD or SD goes HIGH (3), OR goes LOW (4). When PD or SD goes LOW again (5), the output data changes (6) and OR returns HIGH (7).

Figure 7.

transition on PL when $\overline{IR}$ is LOW. (It is the coincidence of PL HIGH and IR LOW which results in the internal load strobe.) When the data has been entered the first control flip-flop sets, causing $\overline{IR}$ to go HIGH. When PL goes LOW again, the data in the front of the FIFO begins falling through the stack toward the output, and $\overline{IR}$ goes LOW as soon as it has moved to the second register. If the FIFO was filled to capacity when the data was loaded, then $\overline{IR}$ will stay HIGH; new data cannot be entered, and any additional shift in command will be ignored until $\overline{IR}$ goes LOW after some data has been removed from the FIFO.

Data entered into the FIFO falls through the registers until it reaches either the output or another data word. When a data

MASTER RESET

A direct clear signal can be applied to the FIFO by a LOW logic level on the $\overline{MR}$ input. This will clear all the internal control register bits and will clear the data from the outputs. $\overline{IR}$ will go LOW indicating the FIFO is ready to receive new data. If the PL input is held HIGH when the $\overline{MR}$ returns to a HIGH state, then an internal input strobe will be generated, and whatever data is on the inputs will be loaded into the FIFO. If this is not desired then PL should be held LOW at the end of the master reset. The master reset will cause OR to go LOW and remain LOW until new data falls through from the input.

FLAG

A flag output is available on the Am2812 and Am2813 to indicate whether the FIFO is more or less than half full. The flag signal is generated by summing the "1s" in the control flip-flops, and therefore is not affected by the movement of data through the register. The flag signal goes HIGH when the 15th ±1 (i.e., the 14th, 15th, or 16th) word is loaded into the FIFO. It will remain HIGH until there are less than 15 ±1 words in the memory. It is always HIGH if there are more than 16 words in the FIFO.

OUTPUT ENABLE

The Am2812 and Am2813 data outputs are 3-state signals. When OE is HIGH, they will be in either a HIGH or LOW state; if OE is LOW, they will go to a high-impedance OFF state. Outputs of several FIFO buffers can then be tied together onto a bus, and one of the buffers can be selected to drive the bus. When OE is LOW, the dump function (both SD and PD) is disabled.

SERIAL INPUT AND OUTPUT (Am2812 ONLY)

The Am2812 also has the ability to read or write serial bit streams, rather than 8-bit words. The device then works like a 256 by 1-bit FIFO. A serial data stream can be loaded into the device by using the SL clock input and applying data to D_0 input. Inputs D_1 - D_7 must be grounded. The SL signal operates just like the PL input, causing $\overline{IR}$ to go HIGH and LOW as the bits are entered. The data is simply shifted across the 8-bit input register until 8 bits have been entered; the 8 bits then fall through the register as though they had been loaded in parallel.

A corresponding operation occurs on the output, with clock pulses on SD causing successive bits of data to appear on the O_7 output. OR moves HIGH and LOW with SD exactly as it does with PD. When 8 bits have been shifted out, the next word appears at the output. If a PD command is applied after the 8 bits on the outputs have been partially shifted out, the remainder of the word is dumped and a new 8-bit word is brought to the output.

When one of the serial clocks is used, the corresponding parallel signal (PL or PD) should be grounded.

EXPANSION OF THE Am2812 AND Am2813

The input and output shift and ready signals have been designed so FIFOs can be directly connected end-to-end to make a longer (i.e., more words) buffer memory, as shown in the applications in Figures 10 and 11. Wider words can be stored by using independent FIFO stacks, side by side, like the Am3341s in Figure 6. When FIFOs are connected end to end, the total number of words that can be stored is (31n+1) not 32n. This is due to the fact that when an SI command loads the 32nd word into a FIFO, the $\overline{IR}$ output stays HIGH, and no PD pulse is applied to the adjacent up-stream FIFO. As a result the word just written into the FIFO is duplicated at the output of the previous FIFO. When at least one word is removed from the downstream FIFO, the $\overline{IR}$ signal goes LOW, causing the duplicated word to be dumped from the up-stream device.

SYSTEM INTERFACING

Normally the input and output of a stack of FIFOs are interfaced with TTL logic. A special interface circuit is used internally on the inputs of the AMD family of FIFOs to provide complete electrical compatibility with TTL outputs; no external components need be used. The circuit works by using an MOS transistor inside the chip as a pull-up resistor in the HIGH state. When the voltage applied to the input is LOW, the internal resistor is disabled and presents no loading to the TTL output. THE V-I characteristic of the input is shown in Figure 8.

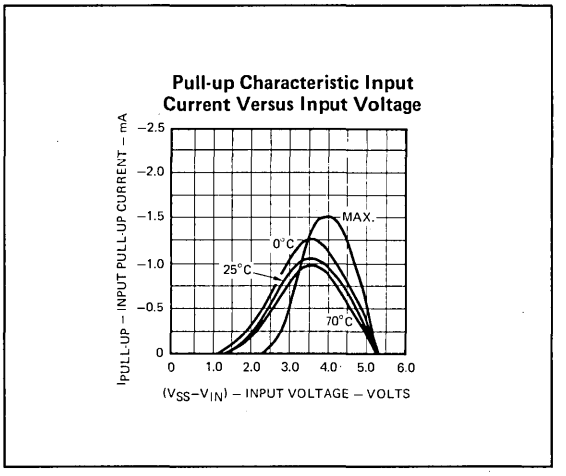


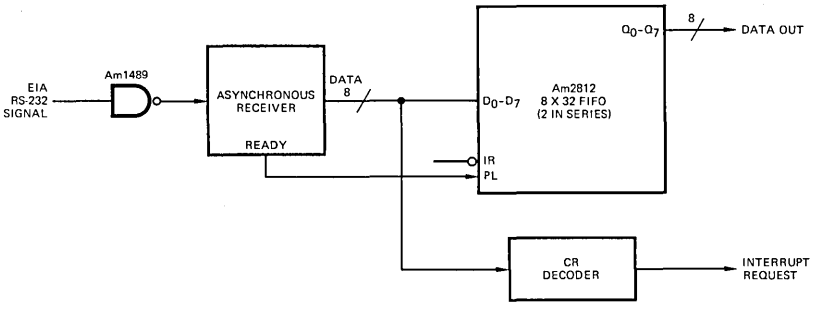
Figure 8. Input Voltage Current Characteristics

The logical interface between the FIFO inputs and the rest of the system must detect that all device inputs are ready, and then supply a shift in command when new data is available. Normally this is rather simple, since most data transfer interfaces contain a data strobe control and a not ready signal. Some caution must be exercised when a composite Input Ready signal for a parallel stack of FIFOs is formed. The inputs to the stack are ready to receive data only when PL is LOW and all input ready signals are HIGH (LOW on the Am2812. Data can be removed from the inputs to the stack only when all input ready signals have gone LOW (HIGH on the Am2812). The easiest way to handle this situation is to detect only that all inputs are ready to receive data, and then insure *that data remains as long as is required by the worst case specification*, rather than actually detecting that the data has been loaded into all devices.

The data on the data inputs must be held steady for about a 400ns period following the SI or PL LOW-to-HIGH transition. The internally generated data strobe will occur sometime during this period. The strobe will not occur, however, until at least 25ns after the SI transition. The rising SI signal may therefore also be a clock to a TTL register feeding the data inputs, as there is sufficient time available for the t_{pd} of the register. However, it is preferable to change the input data on the falling edge of SI for additional timing margin in the system.

At the output of the FIFO, the logic must detect that all outputs are ready, and then supply the dump command when the data has been received by the system. Again, these two kinds of signals are normally available in systems.

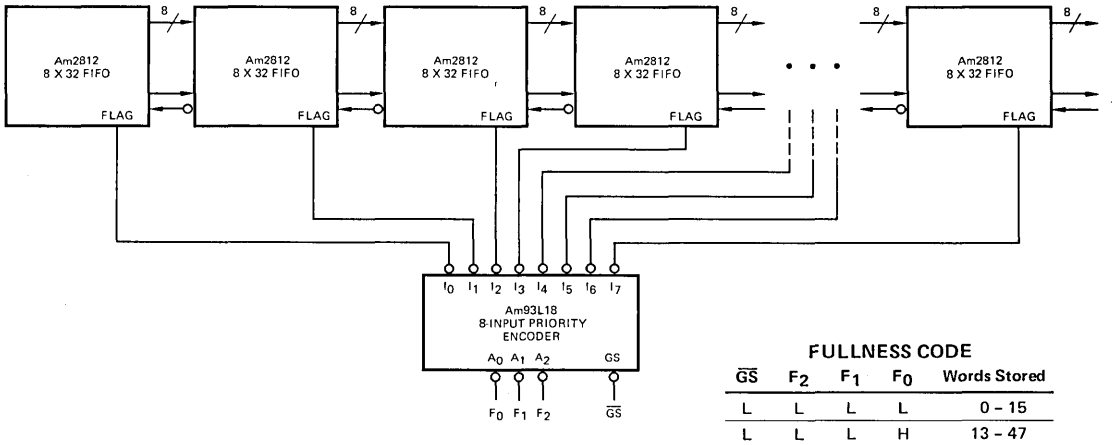
APPLICATIONS



CHARACTER BUFFER FOR TERMINAL

RS-232 data from the data set is converted to parallel 8-bit ASCII characters by an asynchronous receiver chip. When each character is received it is placed in the FIFO buffer. The characters (up to 64) are stored until a carriage return character is detected. An interrupt is then generated to the processor, informing it that a data line is ready.

Figure 9. Character Buffer for Terminal.



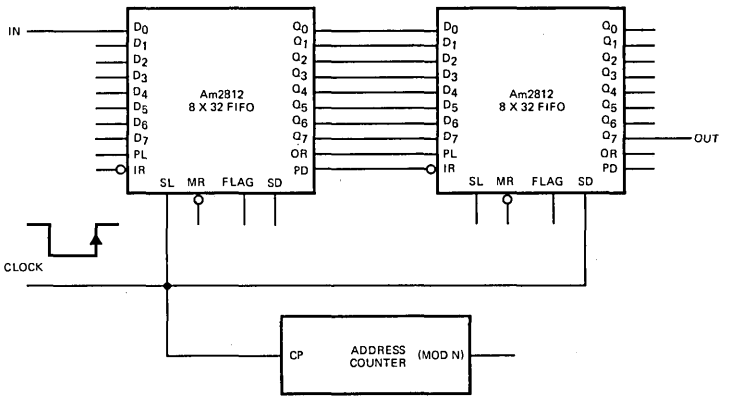
FULLNESS CODE

$\overline{GS}$	F_2	F_1	F_0	Words Stored
L	L	L	L	0 - 15
L	L	L	H	13 - 47
L	L	H	L	45 - 78
L	L	H	H	76 - 109
L	H	L	L	107 - 140
L	H	L	H	138 - 171
L	H	H	L	169 - 202
L	H	H	H	200 - 233
H	H	H	H	231 - 249

The Fullness Flags from Am2812 or Am2813 FIFOs can be encoded by an Am93L18 8-input priority encoder. The output code F_0-F_2 indicates the weight of the highest priority input which is LOW. GS is group signal; it is HIGH if all the inputs are HIGH.

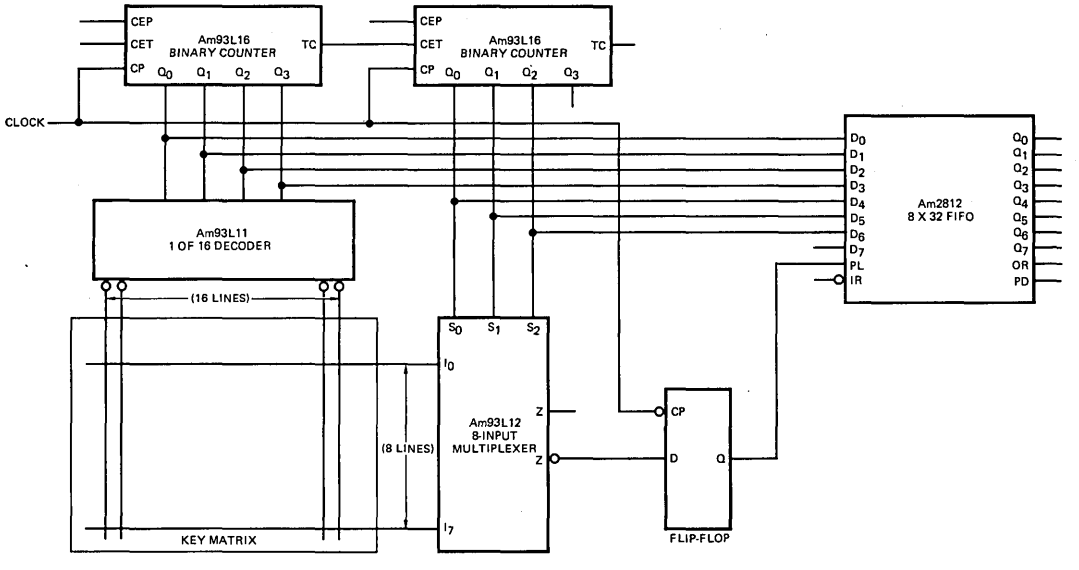
Figure 10

APPLICATIONS (Cont.)



The serial I/O of the Am2812 is used, with data clocked into the D_0 input by CP_{IN} and clocked out of the Q_7 output by CP_{OUT}. Since data stacks up at the output end, the shift register appears to have a length corresponding to the number of words stored. For a 327-bit shift register, for example, it should be initialized with 327 O's. Data may then be entered or recirculated and the MOD 327 counter can be used to indicate the "address" of the current bit. A parallel transfer between devices is used.

Figure 11. N-Bit Shift Register, N = 8 to 512.



The combination of the counters and multiplexers act as a key encoder on the key matrix. A closure will produce a HIGH on the multiplexer output $\overline{Z}$ when the appropriate switch is scanned. The HIGH is stored in a flip-flop to provide a shift-in command to the FIFO one clock period wide. The flip-flop is clocked on the falling clock edge to insure the count is stable during the shift-in pulse.

Figure 12. Storage of Switch or Key Closures.

APPLICATIONS OF DYNAMIC SHIFT REGISTERS

By John Springer, Digital Applications

INTRODUCTION

MOS technology has several characteristics that make it ideal for data storage. Because MOS structures are small, relative to bipolar devices, a large number of bits can be stored on a small chip. Additionally, MOS devices exhibit high impedances that make it possible to store data on small parasitic capacitors rather than in normal cross-coupled transistor pairs. Using capacitive storage techniques has the effect of further increasing the number of bits that can be stored in a given area, because the number of MOS devices needed per bit is reduced. Circuits that store data on capacitive nodes are called "dynamic" because they depend on continual refreshing of the stored charge to maintain its integrity. In random access memories this refreshing is usually accomplished by reading and re-writing the data back into the same storage nodes through some internal refresh circuitry. In dynamic shift registers refreshing is accomplished by simply shifting the register, so that the stored data is "read" from one bit and written into the next one. Dynamic storage introduces a new constraint on operation of a shift register in that there is not only a maximum operating frequency due to normal propagation delays, but also a minimum operating frequency defined by the maximum time that can elapse between refresh operations. This application note deals with the series of dynamic MOS shift registers in Table I.

Table 1

Device	Length	Maximum Data Rate
Am1402A	4 X 256	5 MHz
Am1403A	2 X 512	5 MHz
Am1404A	1024	5 MHz
Am1405A	512	3 MHz
Am2802	4 X 256	10 MHz
Am2803	2 X 512	10 MHz
Am2804	1024	10 MHz
Am2805	512	4 MHz
Am2806	1024	4 MHz
Am2807	512	4 MHz
Am2808	1024	4 MHz

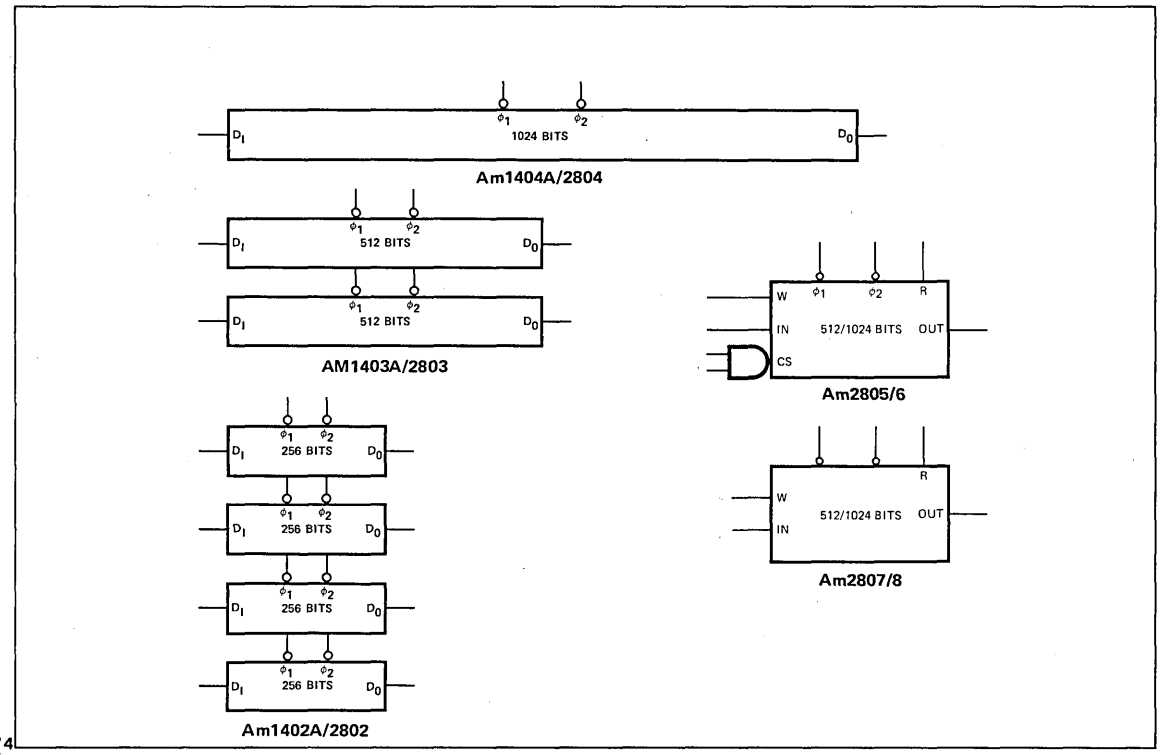


Figure 1. Advanced Micro Devices Dynamic Shift Registers

DYNAMIC SHIFT REGISTER CIRCUIT

In dynamic shift registers data storage occurs entirely on capacitive nodes. The circuit used for each bit of the registers is shown in Figure 2. Each cell consists of two storage nodes, which may be designated the master and the slave. There are two clock lines fed to each cell; one clock causes data on the input to be fed into the master storage node and the other causes data stored on the master node to be shifted into the slave. The output of the slave feeds the master input to the next cell. The two storage nodes, alternately activated, provide the escapement mechanism used in all types of dual rank flip-flops to prevent data from feeding straight through from the input to the output.

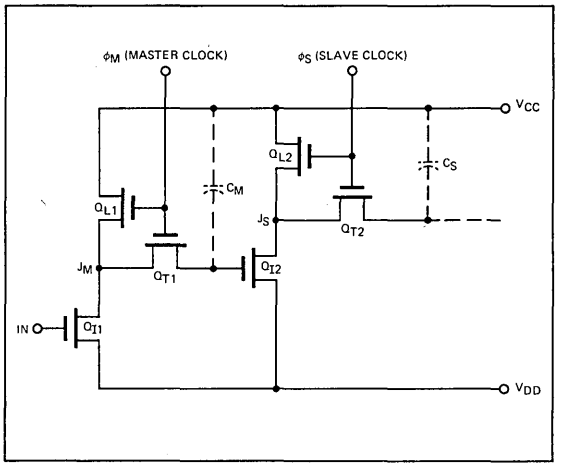


Figure 2. Dynamic Two-Phase Storage Cell

The master and the slave in the cell each consist of three transistors, which may be designated as the input transistor (Q_{I1}, Q_{I2}), the load transistor (QL_1, Q_{L2}) and the transfer gate (Q_{T1}, QT_2). Each of these transistors behaves like an open circuit when its gate is at a HIGH logic level and like a closed switch or resistor (the impedance depends on the geometry of the device) when its gate is at a LOW logic level. The gate input impedance is very high, on the order of 10^{18} ohms, so virtually no current flows into the gate.

The dynamic operation of the circuits is illustrated in Figure 3. When both clocks are HIGH the load and transfer gates are off, and no current flows in the circuit. The data on the input turns the input transistor on or off. When the master clock goes LOW, the load transistor turns on and serves as a load resistor of about 200k ohms for the input device, establishing a level near V_{CC} or near V_{DD} (depending on the state of the input transistor) at point JM. At the same time the transfer gate, Q_{T1}, turns on, allowing current to travel onto or off of the parasitic storage capacitor, so that the voltage on the capacitor is the same as the voltage at point JM. When the master clock goes HIGH, the transfer gate shuts off and the stored level is trapped on the capacitor. The load transistor also shuts off so that power is no longer dissipated through the input transistor. At some time later the slave clock goes LOW and the identical process occurs in the slave half of the cell. When the charge is stored at the output of the slave it is also at the input to the master of the next cell, so a shift of one bit in the register is accomplished by applying a master clock and then a slave clock. Note that power in the register is consumed only when one of the two clocks is LOW.

The mode of operation described above is typical for all dynamic two-phase shift registers. A disadvantage of the two-phase operation is that two clock pulses are needed for each shift of the register. The demanding requirements on the

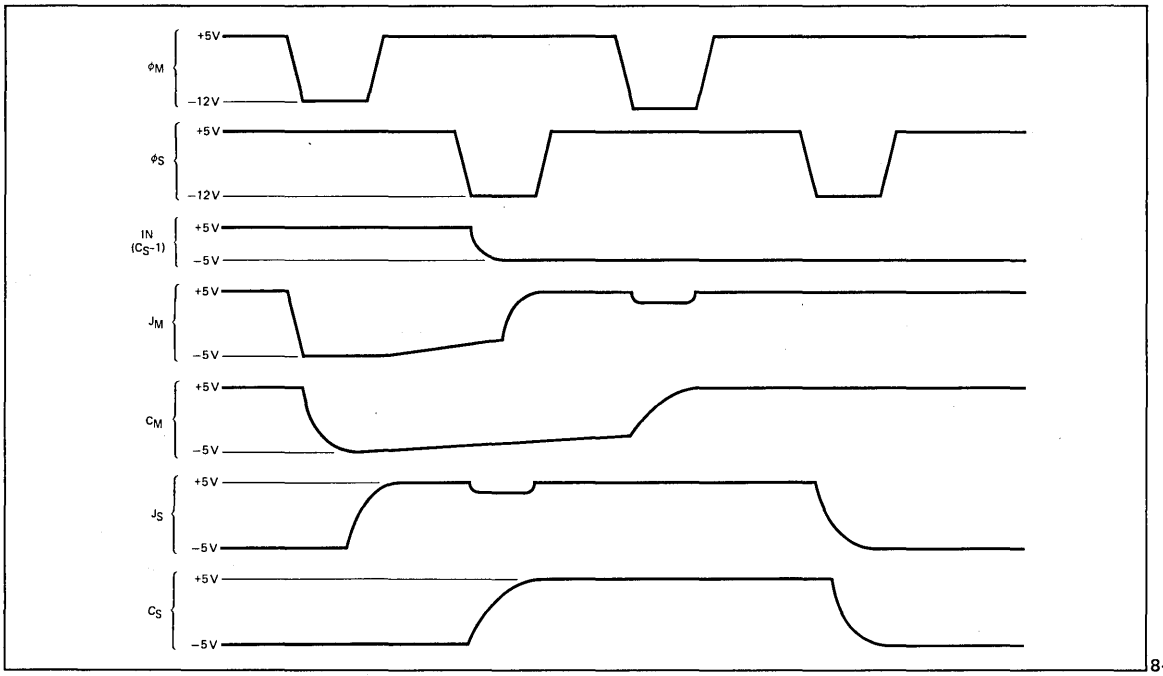


Figure 3. Voltages in Cell of Fig. 2 During Shift of a HIGH and a LOW

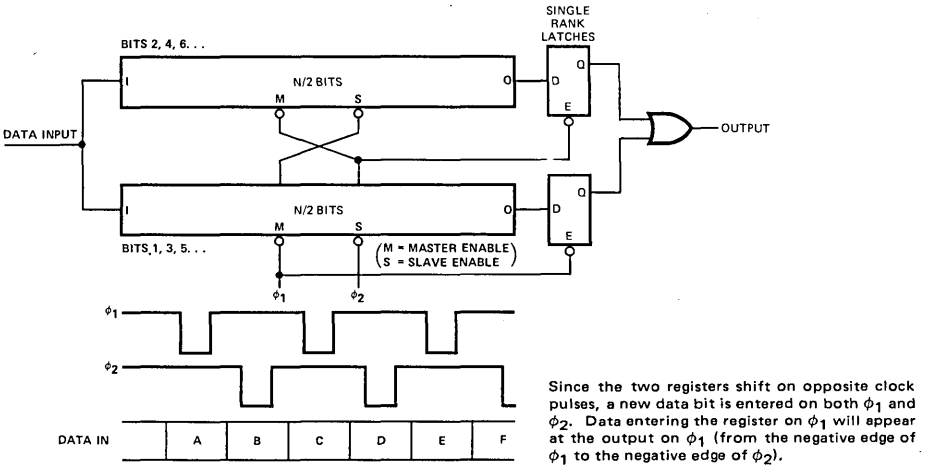


Figure 4. Functional Equivalent of Am1402/3/4A and Am2802/3/4

clock signals (pulse width, voltage levels and speed) limit the data rate through the register to about 2 to 3 MHz generally. It is possible, however, to alter the register configuration slightly to double the data rate through it.

In the Am1402/3/4A and Am2802/3/4 a data shift occurs on every clock pulse rather than on every pair of clock pulses. This is accomplished by multiplexing two registers onto the same input and output lines, as shown in Figure 4. The "odd" numbered bits are stored in one register and the "even" bits in the other. The master clock of one is tied to the slave clock of the other and vice-versa. Clock $\phi 1$ acts as a master clock to the odd register, shifting data on the data input into the master of flip-flop 1. The same clock acts as the slave to the even register, shifting data into the output of the last flip-flop. From the last flip-flop it is fed to a dynamic output multiplexer modeled in Fig. 4 as a pair of ORed latches so that it will appear on the output pin when $\phi 2$ occurs. The output multiplexer acts like an extra 1/2 bit of register, so that the data entering the odd register during $\phi 1$ will leave the multiplexer N pulses later, also during $\phi 1$. Similarly data entering the register during $\phi 2$ will appear on the output during $\phi 2$.

The data rate through the dynamic multiplexed register is twice the frequency of either of the clock inputs $\phi 1$ or $\phi 2$, so for a given clock frequency and using basically the same cell, the data rate is doubled over the normal two-phase register.

CLOCK TIMING IN THE REGISTERS

There are two constraints on clock timing imposed by the dynamic storage medium. First, the clock must be LOW long enough to fully charge or discharge the storage capacitor. The capacitor is approximately 0.1 pf and it is charged through the series resistance of the transfer gate (about 40 kΩ) and either the load transistor or the input transistor. Figure 5 shows the charge on the capacitor as a function of clock LOW time, assuming charging begins when the clock reaches about −10V. The LOW-to-HIGH charging occurs more rapidly because the impedance of the input gate is much less than the impedance of the load transistor. These are nominal curves and a guardband must be allowed for tolerances on the resistors and capacitor.

In between clocks the charge stored on the capacitor will slowly leak away due to PN junction leakage. If too much time elapses between clocks a stored negative level may decay so much that it cannot turn on the next input gate completely, so that during the next clock the stored level will appear to be a HIGH instead of a LOW, resulting in inversion of the data. The maximum time that the clocks can be stopped, or remain in the HIGH state, is a complex function of several parameters. It is principally affected by the temperature of the die inside the package, becoming shorter as the die gets hotter. The three curves in figures 6A, 6B and 6C can be used to determine the nominal maximum clock HIGH time. When the devices are operated in a "burst" mode, then the die temperature is governed by the greater of the two duty cycles. Again a guardband must be added as these curves assume typical device parameters. The calculations used for the curves are shown in the box.

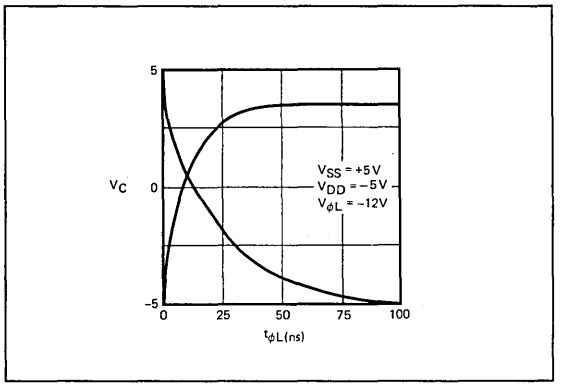


Figure 5. Charge on Storage Capacitor Versus Clock LOW Time ($V_{\phi L}$ = <−10V)

Maximum Clock HIGH Time Versus Ambient Temperature for Very Small Duty Cycles

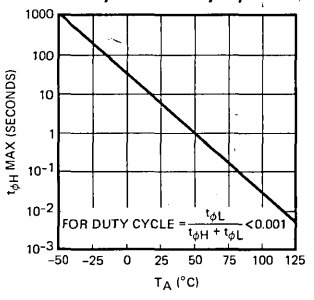


Figure 6A.

Maximum Clock HIGH Time Versus Clock Duty Cycle (Am1402A/2802)

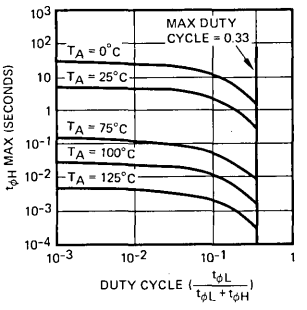


Figure 6B.

Maximum Clock HIGH Time Versus Clock Duty Cycle (Am1403A, 2803, 1404A, 2804, 2805, 2806)

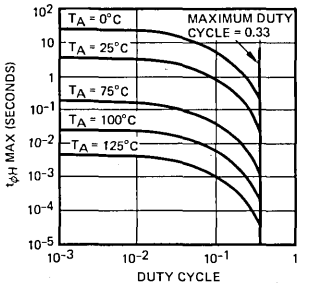


Figure 6C.

Note: These are theoretical typical curves and should not be used as guaranteed limits.

CALCULATION OF MAXIMUM CLOCK HIGH TIME

The maximum clock HIGH time is the time required for the charge on the capacitor to decay from its full value of −10V to a level at which it will be incorrectly read by the next stage input. This level is about 0V so a loss of 5V on the capacitor can be tolerated. The charge on the capacitor escapes through junction leakage, which, for these registers, is about 0.1 pA at 25°C. The leakage current doubles for every 10° rise in junction temperature. The capacitor is about 0.1 pF in value.

$\Delta V = 5V = \frac{it}{C}$, where i is leakage current and C is 0.1 pF

$t_{\phi H} = \frac{0.5}{i_{leak\ in\ pA}}$ where $t_{\phi H}$ = maximum clock HIGH time

$i_{leak} = 0.1 \times 2^k$

where $k = \frac{T_{junc} - 25°C}{10}$ because leakage doubles every 10°

$T_{junc} = T_a + \theta_{ja} \times$ power diss.,

where θ_{ja} is junction to ambient temperature

$\theta_{ja} = \begin{cases} 180°C/Watt\ for\ Metal\ can \\ 105°C/Watt\ for\ 16\ lead\ DIP\ (1402A/2802) \end{cases}$

power dissipation is directly porportional to clock duty cycle (clock LOW time divided by total clock period).

power = 1.2 x duty cycle (V_{DD} = −5V, V_{SS} = +5V)

$i_{leak} = 0.1 \times 2^k$ where $k = \frac{T_a + \theta_{ja}\ (1.2 \times DC) - 25}{10}$

$t_{\phi H}\ max = \frac{5}{2^k}$

For TO-5 can (Am1403A and 1404A):

$$\log (t_{\phi H}) = 1.45 - 0.03T_a - 6.45DC$$

For DIP package

$$\log (t_{\phi H}) = 1.45 - 0.03T_a - 3.78DC$$

Note that for small duty cycles the clock high time depends only on ambient temperature.

APPLICATIONS OF THE REGISTERS

1. Clock Driving

Numerous circuits are available for clock drivers for these registers. The clock HIGH level is 5 volts and the LOW level is −12 volts. The sophistication required in the clock driver depends on how rapidly the registers are to be driven. At low data rates the clock can be generated by simply driving a TTL clock signal into a PNP transistor with a pull down resistor (Figure 7). Of course this is not suitable for driving very large loads, or small loads at high speed, because of the slow fall time on the clock. Most often a monolithic driver such as the MH0026 is adequate. For very high speed operation, up to 10 MHz with the Am2802/3/4, a good hybrid driver or a discrete push-pull driver should be used. The rise and fall times of the clock signal can be controlled with a series resistor in the clock line.

A very important consideration in the clock driver is that the clock signal to the register MUST NEVER EXCEED V_{SS} + 0.3V! If the clock voltage rises higher than this, undesired PNP transistors are formed on the MOS chip, discharging the storage capacitors and possibly permanently damaging the register. To guard against overshoot on the clock lines, a germanium (not silicon) switching diode should be used to clamp the clocks to V_{SS}. For long clock traces on PC boards, it may be necessary to consider transmission line effects also, and backmatch the clock lines with a series resistor at the driver.

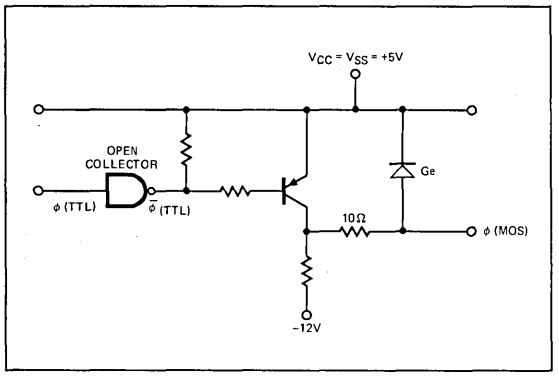


Figure 7. Simple Clock Driver

2. TTL Interfacing

The inputs and outputs of these registers are, except for the clock lines, compatible with TTL logic levels, although it is necessary to add some resistors. The input threshold is 2 volts below V_{CC}, higher than a normal TTL V_{OH}, so a pull-up resistor must be used on the TTL output to establish the higher logic level. DTL, which has an internal resistor pull-up, does not require the extra resistor.

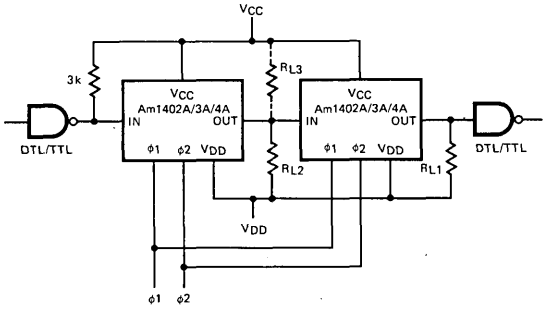
The output of the registers are open drain transistors whose sources are connected to V_{CC}. This output transistor has an impedance of about 1,000 ohms, and will establish the HIGH level on the output, but an external pull-down resistor must be connected between the output and V_{DD} to establish the LOW level. This is true whether the output is driving TTL or another MOS input. The pull-down resistor must be small enough to sink 1.6 mA (one TTL load) and maintain 0.4V at the TTL input and large enough that the MOS output can supply current to the resistor and still hold the output at 2.4V. A 3k ohm resistor to –5 volts will suit most applications as shown in Figure 8.

3. Register Output to Register Input Interfacing

A frequent application of the Am1402/3/4 and Am2802/3/4 is for serial storage of data which is updated from time to time. In this application several registers are connected end-to-end to provide the required storage capacity and the output of the last register is tied back to the input of the first register through a two-input multiplexer so that either the data output or some new data can be written into the first location. Such a system is illustrated in Figure 9.

When the registers are used in this fashion, some timing constraints must be observed. The output of the register switches state following the falling edge of the clock (either $\phi 1$ or $\phi 2$). The data remains stable until the falling edge of the next clock. The input accepts data just prior to the rising edge of the clock. When the output of one register is connected to the input of another register (or to its own input via a multiplexer) the data appearing on the output is written into the input during the same clock LOW time. This is different from TTL, in which the output of one register is written into the input of the next on the next clock edge. Because the data is transferred during the clock LOW time, the LOW time must be at least equal to the propagation delay (clock-to-output) plus the set-up time at the input. The sum of these times is substantially longer than the minimum clock pulse width so that when register output is tied to a register input the minimum clock pulse width must be lengthened.

If the registers must be operated at very high speed, then the clock LOW time must be as short as possible, and the requirement that data transfer occur during the LOW time may not be acceptable. In this case a TTL flip-flop can be used between registers to act as a single bit fast interface. The TTL flip-flop is clocked on the falling edge of both $\phi 1$ and $\phi 2$ so that in each case it stores the data brought to the MOS output on the previous clock. The same falling edge that clocks the TTL flip-flop is the start of the clock LOW period during which the data in the TTL flip-flop is written into the first bit of the next MOS register. While this scheme solves the speed problem, it introduces an extra bit of delay in the register string. See Figure 10.



R_L Load Resistor Values for Different V_{DD} Supplies

	$V_{CC} = 5$ V, $V_{DD} = -5$ V	$V_{CC} = 5$ V, $V_{DD} = -9$ V
R_{L1}	3.0 k	4.7 k
R_{L2}	4.7 k	6.2 k
R_{L3}	Not required	3.9 k

Figure 8. DTL/TTL to MOS to DTL/TTL Interface

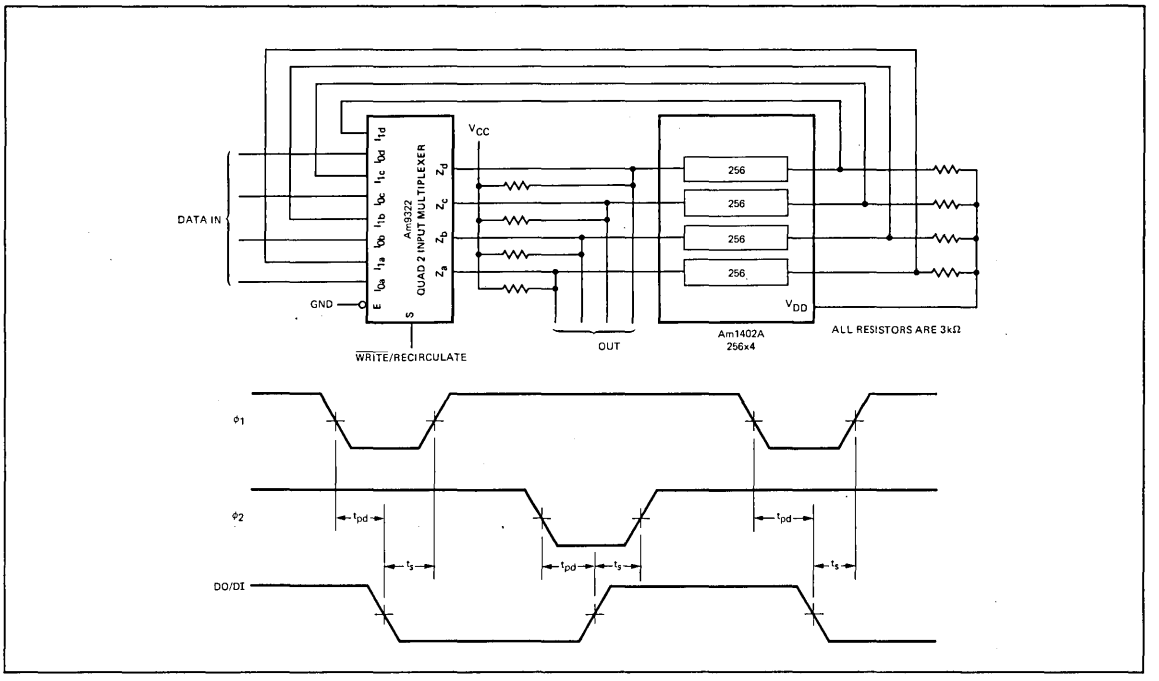


Figure 9. Recirculating Register. Data-out Changes Following Clock HIGH-to-LOW Transition and is Written Into Input During the Same Clock LOW Time.

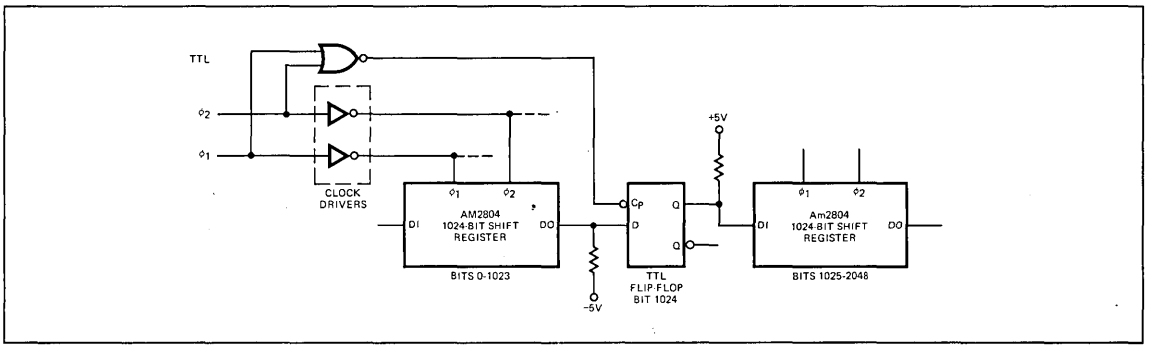


Figure 10. TTL Flip-Flop Acts as High Speed Interface Between Registers, Allowing Use of Short Clock Pulses, But Also Introduces an Extra Bit of Delay

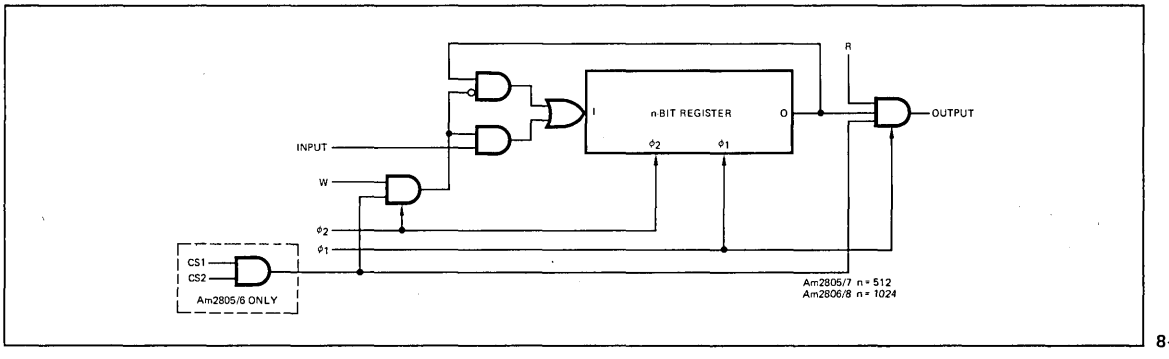


Figure 11. Functional Diagram of Am2805/6/7/8

4. Register Systems Using the Am2805/6/7/8

The Am2805/6/7/8 512 and 1024-bit registers are not internally multiplexed, but require a pair of clock pulses to product a shift of one bit. These registers also have recirculation logic built-in under control of a write input (W). When the write input is HIGH, data on the input enters the register during $\phi 2$, the master clock. When the write input is LOW, the data at the output of the last bit is written into the first bit instead. The functional diagram is shown in Figure 11. A read control, R, gates the output through an open drain AND gate, so that the outputs of several registers can be ORed together and one register selected. The Am2805 and Am2806 also have a two-input chip select gate; both inputs must be HIGH in order to write into or read from the register. If either chip select input is LOW, the register recirculates.

Note that the write and read gating is activated by the appropriate clock phase. This is done not for dynamic storage purposes but rather to conserve power; no power is dissipated in the input if $\phi 2$ is HIGH and no power is dissipated in the output if $\phi 1$ is HIGH. Dynamic storage does occur in the output gating, with the transfer gate activated when $\phi 1$ is LOW and the read control is HIGH. Data will appear on the output 100 ns after $\phi 1$ goes LOW and read goes HIGH. Data will be stored dynamically in the output stage until the next $\phi 1$ provided that read remains HIGH until the end of the clock LOW time. If read goes LOW before $\phi 1$ goes HIGH the output will turn off.

In large register systems, many Am2805/6/7/8 registers can be connected in parallel and the desired register addressed through the chip select and/or the read and write controls. When many register outputs are connected together the capacitance on the output is increased and care must be taken to insure that the 1,000 ohm output device can fully charge the line.

For higher speed operation, pairs of these registers can be connected in parallel in a multiplexed mode, like the internal configuration in the Am1402/3/4. The inputs and outputs are tied together and the clocks are reversed between the two devices. A flip-flop toggled on each clock pulse can be used to alternate control between the two MOS registers as shown in Figure 12.

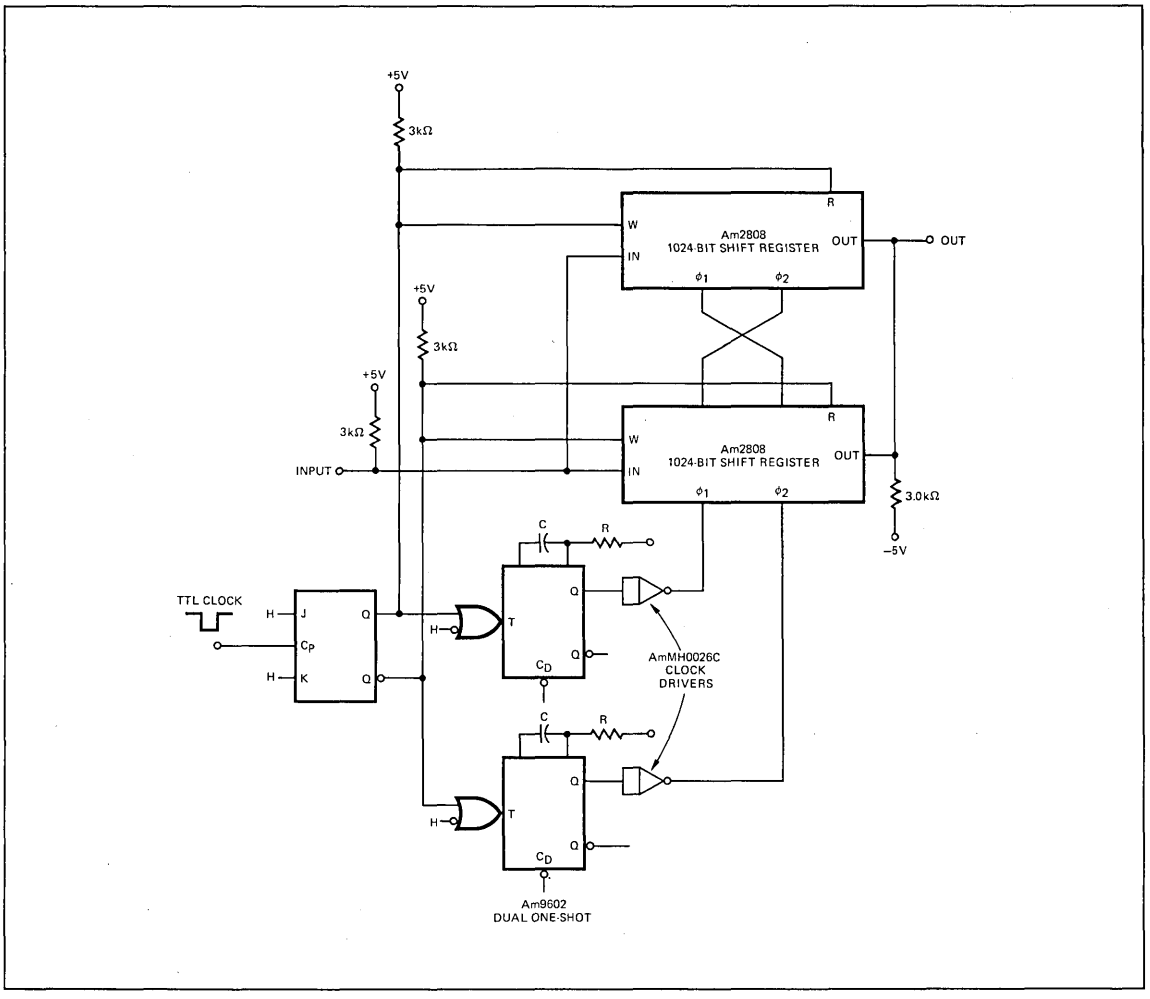


Figure 12. Multiplexed Am2048 Bit Recirculating Register f_{max} = 6 MHz

A RANDOM-PATTERN GENERATOR FOR TESTING DIGITAL DELAY ELEMENTS

By John Springer, Digital Applications

Shift registers can be tested simply with the use of a linear feedback shift register for pseudo-random bit pattern generation.

The most fundamental test that has to be applied to a digital delay element like a shift register, is to insure that it stores data correctly for the proper length of time. To perform this test, one should apply a sequence of bits to the input and, after a delay of n bits, that same sequence should appear at the output. **Fig. 1** illustrates a general scheme.

There are several possible ways to construct such a system. If the pattern is an infinite string of 1s or 0s, then the whole thing is trivial. Alternating 1s and 0s, or any other pattern for which the cycle length of the pattern divides the length of the register evenly, require no extra delay element since the output at any given time is the same as the input at the same time. For example, if the register is 256 bits long and the pattern is a 16-bit sequence, then the register will contain 16 full sequences and the bit on the output will be the same as the bit going into the input.

A good test pattern for a register is a pseudo-random sequence of bits formed by a Linear Feedback Shift Register (LFSR). The LFSR can be built easily from MSI devices, and will generate long sequences of apparently random 1s and 0s. An n-bit LFSR can always be designed to go through $2^n - 1$ states before repeating, and the

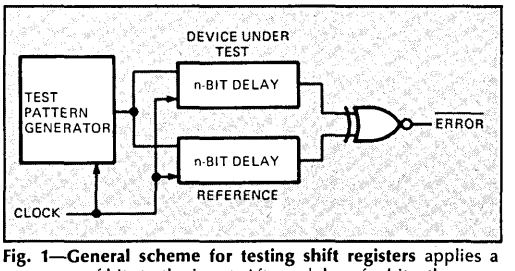


Fig. 1—General scheme for testing shift registers applies a sequence of bits to the input. After a delay of n bits, the same sequence should appear at the output.

serial output from the register will contain all possible sequences of n bits except one (usually all 0s). A significant advantage of the LFSR is that it is possible to generate combinationally the output sequence shifted in time by any number of bits, obviating the extra delay element in the tester.

Fig. 2 illustrates a 4-bit LFSR. An LFSR is formed by feeding the input to the register with the exclusive-OR of some of the register outputs. This particular register, whose input is the EX-OR of the first and last bits, will produce two loops or cycle sets. One is the persistent state of all 0s, and

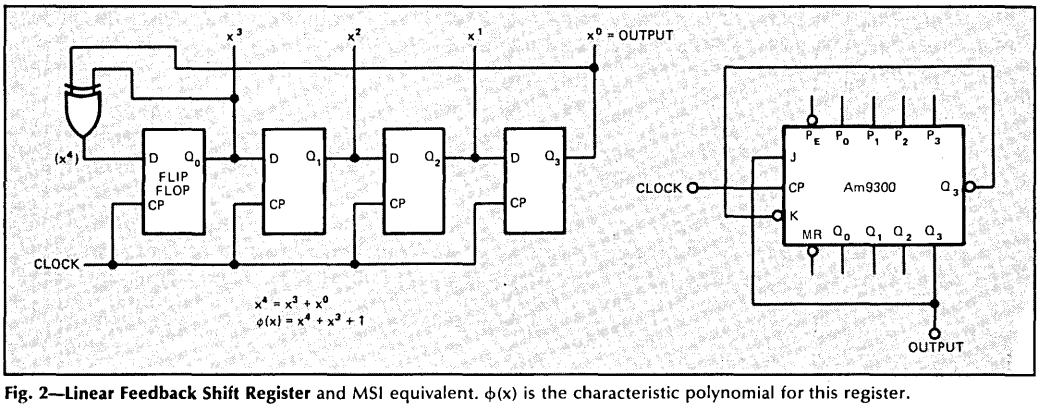


Fig. 2—Linear Feedback Shift Register and MSI equivalent. $\phi(x)$ is the characteristic polynomial for this register.

```
RUN SYNDIV

SYNDIV      12:58      07/05/73

WHAT IS THE LENGTH OF THE GENERATING REGISTER?20
WHERE ARE THE FEEDBACK TAPS (1 = FIRST STAGE, 20 = LAST. A TAP AT 20 IS ASSUMED.
TYPE 0 TO STOP
?1
?0
FOR WHAT DELAYS ARE YOU SOLVING (TYPE 0 TO STOP)
?128
?256
?512
?1025-4
?0
BITS:        5         10        15        20
TAPS FOR DELAY OF 128
   0   1   0   0   0   0   1   1   1   1   0   1   0   1   1   1   1   1   0   1

TAPS FOR DELAY OF 256
   1   0   0   0   1   1   1   0   1   0   1   0   1   1   0   0   1   0   0   0

TAPS FOR DELAY OF 512
   1   0   1   1   1   1   0   1   0   1   0   0   1   1   1   0   0   0   1   1   1

TAPS FOR DELAY OF 1024
   0   1   1   0   1   1   0   0   1   0   0   0   0   1   1   0   1   1   0   1

NOW AT 999
SRU'S:2.4
READY
```

```
 10   DIM F(40),R(40),T(10)
 11     WIDTH 132
 20   PRINT "WHAT IS THE LENGTH OF THE GENERATING REGISTER";
 30   INPUT N
 31   M = 2 ^ N
 32   K = J = 0
 33   P = N
 40   PRINT "WHERE ARE THE FEEDBACK TAPS (1 = FIRST STAGE, ";N;" = LAST.
      A TAP AT ";N;" IS ASSUMED."
 41   PRINT "TYPE 0 TO STOP"
 42   F(N) = 1
 50   INPUT Q
 51   IF Q < > 0 THEN 60
 55   PRINT "ERROR: THERE MUST BE AT LEAST ONE OTHER TAP."
 56   GO TO 40
 60   IF Q = 0 THEN 100
 61   F(Q) = 1
 62   INPUT Q
 65   GO TO 60
100   PRINT "FOR WHAT DELAYS ARE YOU SOLVING (TYPE 0 TO STOP)"
110   J = J + 1
120   INPUT T(J)
130   IF T(J) = 0 THEN 200
135   IF J = 1 THEN 150
140   IF T(J) < T(J - 1) THEN 150
145   PRINT "ERROR: SOLUTIONS MUST BE IN ASCENDING ORDER. BEGIN AGAIN."
146   J = 0
147   GO TO 100
150   IF T(J) < N THEN 160
151   PRINT "ERROR: THIS DELAY IS TRIVIAL. REENTER."
152   GO TO 120
160   IF T(J) > M THEN 110
165   PRINT "ERROR: DELAY IS GREATER THAN MAXIMUM CYCLE LENGTH."
166   GO TO 120
200   K = 1
210     J = J - 1
300   FOR I = 1 TO N
310   IF F(I) = R(I) THEN 350
320   I = N 'FOUND FIRST NON-EQUAL BITS
330   GO TO 360
350   F1 = I
360   NEXT I
400   IF F1 = N THEN 950 'REMAINDER IS ZERO
405   IF F1 = N - 1 THEN 900 'END OF CYCLE
410   FOR I = F1 + 2 TO N
420   IF F(I) = R(I) THEN 450
430   R(I - F1 - 1) = 1
440   GO TO 490
450   R(I - F1 - 1) = 0
490   NEXT I
500   FOR I = N - F1 TO N
510     IF P < T(K) THEN 520
515   GO SUB 800
520   R(I) = 0
525   P = P + 1
550   NEXT I
560   F1 = 0
590   GO TO 300
800     IF K < > 1 THEN 809
802     PRINT USING "BITS:      ";
803     FOR C1 = 1 TO N
804       IF C1/5 < > INT (C1/5) THEN 807
805       PRINT USING "# # #     ";C1;
807       NEXT C1
808       PRINT USING ""
809       PRINT "TAPS FOR DELAY OF " ;T(K)
810       IF F1 = 0 THEN 840 'NO LEADING 0S
820       FOR L = 1 TO N - I
825         PRINT " 0";
830       NEXT L
840         PRINT " 1";
850   IF F1 = N - 1 THEN 881 'NO REMAINDER AFTER 1
860   FOR L = 1 to I - 1
870   PRINT R(L);
880   NEXT L
881   PRINT
882   PRINT
885   IF K = J THEN 999
890     K = K + 1
895   RETURN
900   PRINT "END OF CYCLE ENCOUNTERED AFTER ";P;" STATES."
910   PRINT "CHECK REGISTER TAP CONNECTIONS; THIS IS NOT
      A MAXIMAL LENGTH REGISTER."
915   GO TO 999
950   PRINT "ERROR: REMAINDER IS ZERO. P = ";P
999     STOP
```

Fig. 3—BASIC program gives tap connections for up to 10 different delays for a register of up to 40 bits.

the other is a loop of $2^n - 1 = 15$ states.

Q0	Q1	Q2	Q3
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
0	1	1	1
1	0	1	1
0	1	0	1
1	0	1	0
1	1	0	1
0	1	1	0
0	0	1	1
1	0	0	1
0	1	0	0
0	0	1	0
0	0	0	1
0	0	0	0

The output of the register is Q3, a 15-bit cycle of 1s and 0s. An LFSR is described mathematically by a characteristic polynomial as shown in **Fig. 2.** The output of the register is labeled x^0. The next to the last bit is x^1 and so on. The exponent indicates the delay between a given register position and the LFSR output. Location x^3 is advanced by 3 time periods from the output x^0.

The characteristic polynomial is derived from the equation of the feedback, using modulo 2 addition. For the example in **Fig. 2,** the LFSR input, which is delayed four bits from the output, is labeled x^4.

$x^4 = x^3 + x^0$ (+ is modulo 2 addition, or EX- OR)

$x^4 = x^3 + 1$

$x^4 + x^3 + 1 = 0$

$\phi(x) = x^4 + x^3 + 1$ characteristic polynomial

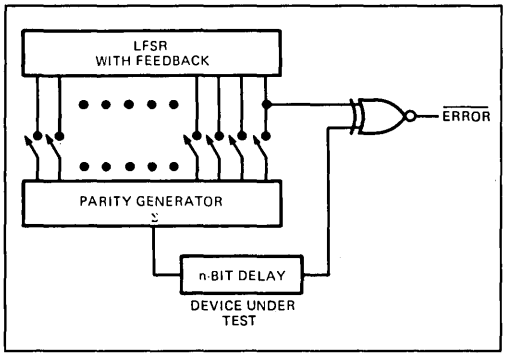


Fig. 4—General tester using LFSR for pattern generation and parity checker for producing advanced pattern.

A property of LFSRs is that exclusive-ORing any group of register outputs together will produce the same bit sequence as the output but shifted in time. The first four shifts of time are directly available at x^1, x^2, x^3 and x^4. Any other time shift can be obtained by EX-ORing the appropriate signals $x^0 - x^3$.

Determining which outputs to EX-OR requires a polynomial division. If n is the number of time periods to be shifted, then

$$\frac{x^n}{\phi(x)} = Q + \frac{R}{\phi(x)}$$

When the characteristic polynomial is divided into x^n the quotient Q is of no interest, but the remainder R indicates the register bits to be EX-ORed to obtain the time shift of n. The arithmetic can be performed by synthetic mod 2 division.

Suppose that for the 4-bit register used in the example, we want a signal that is the output stream advanced by nine time periods (same as delayed by six periods, since the cycle repeats every 15 states).

$\phi(x) = x^4 + x^3 + 1 = 11001$

$x^9 = 1000000000$

```
          111101
11001 ) 1000000000
        11001
         10010
         11001
          10110
          11001
           11110
           11001
             11100
             11001
               101
```

The remainder is $101 = x^2 + 1$. This indicates that the last bit and the second from the last bits should be EX-ORed. For a starting state of 1000:

x^0 = 000111101011001 000111101011001 . . .

delay of 9

$x^0 + x^2$ = 011001000111101 011001000111101 . . .

The synthetic division can be performed fairly easily on a computer. **Fig. 3** is a program written in Computer Science Corp.'s BASIC that gives tap connections for up to 10 different delays for a register of up to 40 bits (these limits are set only by the DIMENSION statement 10). The program generally costs less than 50¢ to run on-line. **Table 1** lists tap connections for some common long shift registers using a 20-bit LFSR with $\phi(x) = x^{20} + x + 1$ (input is EX-OR of the last two bits).

Table 1

ADVANCE SEQUENCE BY	EX-OR BITS
128	6, 8, 10, 12
256	4, 11, 12, 15, 16, 19, 20
512	2, 4, 7, 8, 10, 12, 18, 20
1024	3, 7, 8, 13, 14, 15, 19

The appropriate bits can be EX-ORed using an MSI parity generator/checker such as the 9348 (12 input) or the 74180 (8 input). The resulting scheme is shown in **Fig. 4.** □

The Am25S05, Am2505 and Am25L05 Schottky, Standard and Low Power TTL 2's Complement Digital Multipliers

By John R. Mick

INTRODUCTION

This application note is an updated and expanded version of the "A 2's complement Digital Multiplier – the Am2505" application note by R.C. Ghest, published in November, 1971. The device is now available in three technologies. The Am25S05 is a very high speed 2's complement multiplier built using advanced Schottky technology. The Am2505 is a standard power MSI element for medium speed applications. The Am25L05 is a low-power MSI circuit for slower speed applications.

The Am25S05, Am2505, and Am25L05 can be used in iterative arrays to perform multiplication of 2's complement numbers with a minimum of hardware. The new Am25S05 provides the capability to perform very high speed direct hardware multiplications and is especially suited for real-time digital processing applications. These devices will find applications in minicomputers, recursive or non-recursive digital filters, Fast Fourier Transform processors, adaptive digital integrators and many other digital implementations of special arithmetic algorithms.

At the present time, digital machines perform multiplication using either serial techniques, serial-parallel techniques, or all-parallel techniques. The multiplication speeds can be very slow to very fast depending on the exact hardware implementation used and the hardware constraints imposed. The Am25S05, Am2505, and Am25L05 are particularly suited for either all parallel multiplication or serial-parallel multiplication.

MULTIPLICATION DEFINITION

According to Webster's Dictionary, multiplication is "a mathematical operation that at its simplest is an abbreviated process of adding an integer to itself a specified number of times and that is extended to other numbers in accordance with laws that are valid for integers." This definition is particularly appropriate for binary numbers in that all hardware binary multiplication schemes make an "add" or "no-add" decision and maintain the "weighting" rules of binary numbers. The two numbers involved in the operation are usually called the multiplicand (the number to be multiplied) and the multiplier (the number that multiplies) with the result being called the product (later in this application note the partial products or partial sums will be important).

Binary multiplication is performed as in the following four digit example. The terms X and Y are:

$$X = x_0(2^0) + x_1(2^1) + x_2(2^2) + x_3(2^3)$$
$$X = x_0(1) + x_1(2) + x_2(4) + x_3(8)$$
$$Y = y_0(1) + y_1(2) + y_2(4) + y_3(8)$$

where x_i and y_i can assume a "0" or "1" value for i = 0, 1, 2 or 3.

If X is the multiplicand and Y is the multiplier, the product S of X·Y is

$$\begin{aligned} S = X \cdot Y = {} & y_0(1)\,[x_0(1) + x_1(2) + x_2(4) + x_3(8)] \\ & + y_1(2)\,[x_0(1) + x_1(2) + x_2(4) + x_3(8)] \\ & + y_2(4)\,[x_0(1) + x_1(2) + x_2(4) + x_3(8)] \\ & + y_3(8)\,[x_0(1) + x_1(2) + x_2(4) + x_3(8)] \end{aligned}$$

In the above example, it can be seen that three additions are required to generate the product S of X·Y; the first two of these are usually called partial products or partial sums. In order to examine the weighting of the binary numbers in the above example, the complete partial product solution is shown in Figure 1 and the weights of the x terms and y terms have been combined.

								Multiplicand	x_3 (8)	+	x_2 (4)	+	x_1 (2)	+	x_0 (1)	
								Multiplier	y_3 (8)	+	y_2 (4)	+	y_1 (2)	+	y_0 (1)	
									x_3y_0 (8)	+	x_2y_0 (4)	+	x_1y_0 (2)	+	x_0y_0 (1)	
								x_3y_1 (16)	+	x_2y_1 (8)	+	x_1y_1 (4)	+	x_0y_1 (2)		
						Carry (32)	+	Ps_4 (16)	+	Ps_3 (8)	+	Ps_2 (4)	+	Ps_1 (2)	+	Ps_0 (1)
						x_3y_2 (32)	+	x_2y_2 (16)	+	x_1y_2 (8)	+	x_0y_2 (4)				
				Carry (64)	+	Ps_5 (32)	+	Ps_4 (16)	+	Ps_3 (8)	+	Ps_2 (4)	+	Ps_1 (2)	+	Ps_0 (1)
				x_3y_3 (64)	+	x_2y_3 (32)	+	x_1y_3 (16)	+	x_0y_3 (8)						
s_7(128)	+	s_6(64)	+	s_5(32)	+	s_4(16)	+	s_3(8)	+	s_2(4)	+	s_1(2)	+	s_0(1)		

Figure 1. Multiplication of Two Unsigned 4-bit Numbers X and Y

The $s_7(128)$ term represents the carry out of the final summation. As is seen, the multiplication of two 4-bit unsigned words results in an 8-bit product. This can be extended to a general statement; that is, the multiplication of a m-bit unsigned number with a n-bit unsigned number gives a m + n bit resultant unsigned product. This number may be truncated of course and rules will be given later for determining the resulting accuracy when the hardware is being reduced.

It should be recognized that the product terms associated with y_0 and y_1 can be added in one adder and the product terms associated with y_2 and y_3 can be added in a second adder at the same time; thereby giving two partial products after one adder propagation delay time. These two partial sums can then be added in a third adder to give the resultant product of the multiplication.

One technique for reducing multiplication time that is presently being used in serial and serial-parallel multipliers is to ignore addition when the multiplier bit is a logic "0." When this is done the number of terms to be added is equal to the number of 1's in the multiplier word. This method can be extended in such a way that strings of 1's can also be ignored—this leads to an important new technique for performing high speed multiplication. This technique will be discussed in greater detail later.

Two's Complement				Decimal Number
Sign bit				
-2^3	2^2	2^1	2^0	
−8	4	2	1	
0	1	1	1	+7
0	1	1	0	+6
0	1	0	1	+5
0	1	0	0	+4
0	0	1	1	+3
0	0	1	0	+2
0	0	0	1	+1
0	0	0	0	0
1	1	1	1	−1
1	1	1	0	−2
1	1	0	1	−3
1	1	0	0	−4
1	0	1	1	−5
1	0	1	0	−6
1	0	0	1	−7
1	0	0	0	−8

Figure 2. Full Definition of a 4-bit Two's Complement Binary Number

TWO'S COMPLEMENT NOTATION

This section is presented as a quick review of the two's complement numbering system and is intended to give insight for the designer not familiar with two's complement notation. The two's complement numbering system is a technique for describing positive and negative numbers in a convenient notation. When contrasted with other numbering systems such as sign-magnitude and one's complement, it has the advantage of only having one representation for the number "zero." Also, two's complement numbers can be added or subtracted without concern for the sign of each number as the result will be correct in two's complement notation.

In 2's complement notation, the sign bit is a logical "0" for positive numbers and a logical "1" for negative numbers. Four bits may be used to represent the numbers +7 to −8 as shown in Figure 2. Notice that the sign bit does carry magnitude information that has a negative value.

From this example, it is readily apparent that the magnitude of the negative numbers is not represented by its associated magnitude bits if the sign bit is ignored as is the case for the positive numbers. One way to find the absolute magnitude of a negative 2's complement number is to invert all bits and add plus binary one as in the example below:

1011	Negative 2's complement number
0100	Inverted
+ 0001	One Added
0101	Result

From this example, it is seen that the magnitude of this negative numbers is five.

Likewise, to form a negative 2's complement number, the positive representation is taken, inverted, and plus binary one is added as shown.

Positive number +3	
Binary representation	0011
Inverted	1100
One added	+ 0001
Minus three in two's complement	1101

The advantage of two's complement in many computers and digital processors is that addition and subtraction can be performed without regard to whether the numbers being added or subtracted are positive or negative. Examples of addition are shown in Figure 3. Note that overflows are discarded.

0001	+1	0001	+1	1110	−2
0101	+5	1111	−1	0110	+6
0110	+6	(1) 0000	0	(1) 0100	+4
0110	+6	1010	−6	1110	−2
1110	−2	0011	+3	1101	−3
(1) 0100	+4	1101	−3	(1) 1011	−5

Figure 3. Examples of Two's Complement Addition

Subtraction is much like addition except that the number being subtracted (subtrahend) must be inverted and have one added to its value. It is then added to the minuend. This addition of +1 represents no problem in the hardware because the carry in (c_n) of the least significant adder can be used for this purpose — not an additional adder. Figure 4 shows examples of subtraction.

Minuend	0001 +1	1110 −2	1110 −2	1010 −6
Subtrahend	0101 +5	0110 +6	1101 −3	1101 −3
Minuend	0001	1110	1110	1010
Inverted Subtrahend	1010	1001	0010	0010
Add	1011	0111	0000	1100
Add One	0001	0001	0001	0001
Result (Binary)	1100	1000	0001	1101
Result (Decimal)	−4	−8	+1	−3

Figure 4. Examples of Two's Complement Subtraction.

From these examples, one might conclude that multiplication is simply the product of one 2's complement number with the other. Unfortunately, this is not correct for negative numbers. One obvious technique for multiplication in which negative numbers are represented by 2's complements is to determine the signs and magnitudes of the operands, multiply the magnitudes, and then if the result is negative, cast the result into 2's complement form. It seems preferable, however, to devise a scheme for multiplying such numbers more simply. Booth's method will be considered for this purpose.

BOOTH'S ALGORITHM

In the usual methods of digital multiplication, the multiplier digits are examined in turn and when the multiplier digit is a logical "1," the multiplicand is added to the running partial sum in the appropriate weight. For each multiplier digit, there is a relative one-digit shift between the multiplicand and partial sum whether there has been an addition or not. Booth's algorithm provides a tool whereby more than one shift at a time may be made, depending on the grouping of strings of logic 1's or logic 0's. This multiple shifting ability may be used to "speed up" the multiplication process.

The basic algorithm as developed by Booth is as follows: y_i is the i-th most significant bit of an n-bit multiplier representation. y_{-1} is zero. y_0 is the least significant bit. y_{n-1} is the sign bit. X is the multiplicand.

Starting with i = 0, y_i and y_{i-1} are compared:

1.) If $y_i = y_{i-1}$; add 0X.

2.) If $y_i = 1$ and $y_{i-1} = 0$; subtract 1X (the multiplicand) from the partial product. (Add the 2's complement).

3.) If $y_i = 0$ and $y_{i-1} = 1$; add 1X to the partial product.

Two examples of these rules are shown in Figure 5.

Example 1:

```
1  0 1 1 1      = −9
0  1 0 1 1 (0)  = +11
-------------------------------------------
0  0 0 0 0 1 0 0 1      y0 = 1    y−1 = 0
0  0 0 0 0 0 0 0 0      y1 = 1    y0  = 1
1  1 1 0 1 1 1 1        y2 = 0    y1  = 1
0  0 1 0 0 1            y3 = 1    y2  = 0
1  0 1 1 1              y4 = 0    y3  = 1
-------------------------------------------
(1) 1  1 0 0 1 1 1 0 1     = −99
```

Example 2:

```
1  1 0 1 1      = −5
1  1 0 0 1 (0)  = −7
-------------------------------------------
0  0 0 0 0 0 1 0 1      y0 = 1    y−1 = 0
1  1 1 1 1 0 1 1        y1 = 0    y0  = 1
0  0 0 0 0 0 0          y2 = 0    y1  = 0
0  0 0 1 0 1            y3 = 1    y2  = 0
0  0 0 0 0              y4 = 1    y3  = 1
-------------------------------------------
(1) 0  0 0 1 0 0 0 1 1     = +35
```

Figure 5. Examples of Booth's algorithm for two's complement multiplication

Based on these rules as developed by Booth, it is a straight forward process to make a table of desired action for each of the four possible two-bit combinations under inspection. This is shown below. K is the partial product before this level of the algorithm and is zero initially.

Table of Operation for Booth's Algorithm

y_{i-1}	y_i	Function	Partial Product
0	0	Do nothing	K + 0
1	0	Add X	K + X
0	1	Subtract X	K − X
1	1	Do nothing	K + 0 = K − 0

As stated earlier, one of the initial goals is to develop an algorithm that provides the ability to look ahead more than one bit at a time. Therefore, the above table for one multiplier bit y_i is expanded to Table I for two multiplier bits, y_i and y_{i+1}.

TABLE I – BOOTH'S ALGORITHM FOR TWO MULTIPLIER BITS TAKEN SIMULTANEOUSLY.

Input			For	For	Net Result
y_{i-1}	y_i	y_{i+1}	y_{i-1}, y_i	y_i, y_{i+1}	y_{i-1}, y_i, y_{i+1}
0	0	0	K+0	K+0	K+0
1	0	0	K+X	K+0	K+X
0	1	0	K–X	K+2X	K+X
1	1	0	K–0	K+2X	K+2X
0	0	1	K+0	K–2X	K–2X
1	0	1	K+X	K–2X	K–X
0	1	1	K–X	K–0	K–X
1	1	1	K–0	K–0	K–0

From Table I for two multiplier bits, the following conclusions can be drawn:

1.) The y_{i+1} bit can be used as an add/subtract control where logic "0" is add and logic "1" is subtract.

2.) The function $y_{i-1} \oplus y_i$ can be used as a X weight control indicating the addition or subtraction of X to the partial product K.

3.) The function $y_{i-1}\, y_i\, \overline{y}_{i+1} + \overline{y}_{i-1}\, \overline{y}_i\, y_{i+1}$ can be used as a 2X weight control indicating the addition or subtraction of 2X to the partial product K.

4.) When in the subtract mode, the 2's complement of X ($\overline{X}$ plus one) is added. Thus the x_i bits are exclusive OR'ed with the add/subtract control y_{i+1}. The plus one is generated in the partial product LSB by connecting the y_{i+1} to the first c_n of the adder used to add X and K.

5.) When 2X is being subtracted, the carry into the second LSB of the partial product is generated by connecting the first c_n to y_{i+1} and x_{-1} to logic 0.

Thus, all required functions of Table I can be implemented using combinatorial logic elements. The resultant output is a "partial product" of the total multiplication product. Remember that if y_{i+1} is 1, then y has been treated as a negative number up to that point so the partial product may not really be correct yet.

Both $y_{i-1} \oplus y_i$ and $y_{i-1}\, y_i\, \overline{y}_{i+1} + \overline{y}_{i-1}\, \overline{y}_i\, y_{i+1}$ are symmetric functions. This provides the ability to change from positive logic to negative logic ($X = \overline{X}$, $Y = \overline{Y}$) with the combinatorial functions remaining unchanged.

THE AM25S05

The Am25S05 is an advanced Schottky MSI circuit that implements the algorithm previously developed in this application note. It can be used to multiply signed or unsigned numbers in various number representations and performs multiplications in either positive or negative logic. This discussion applies to the Am2505 and Am25L05 as well; but the Am25S05 has been assumed to provide a single device for discussion purposes.

The logic diagram of the Am25S05 is shown in Figure 6. The logic symbols and connection diagram are shown in Figure 7. The Am25S05 consists of five parts: a multiplier decoder, a shifting array, a complementer, a high speed adder, and a overflow and sign control.

1.) Multiplier Decoder

The multiplier decoder generates the required control signals for the shifting array and complementer. First, it decodes whether 0X, 1X or 2X of the X multiplicand is to be added to the incoming partial product. Second, the multiplier decoder generates the add/subtract command. The decoder generates the functions.

$A = y_{i-1} \oplus y_i$ 1X used

$B = y_{i-1}\, y_i\, \overline{y}_{i+1} + \overline{y}_{i-1}\, \overline{y}_i\, y_{i+1}$ 2X used

$C = \overline{P}\, \overline{y}_{i+1} + P(y_{i+1}A + \overline{y}_{i-1}\, y_i)$ add/subtract

(P input LOW = positive logic; P input HIGH = negative logic; P defined true for negative logic).

The "zero" times the multiplicand is obtained by $\overline{A}\overline{B}$. The P input controls the add/subtract sequence so that the multiplier can work in either the positive or negative logic representation. The function includes terms to handle logic "0 X" independent of the positive or negative logic representation when the decoding functions A and B are both false.

2.) Shifting Array

The shifting array generates 0, 1 or 2 times the multiplicand and applies this to the complementer. X is inverted through the shifting array and "0" is implemented as all HIGH's out of the array. The x_{-1} input is used to shift up the next lower order bit for the 2X function.

3.) Complementer

The complementer consists of a set of exclusive-NOR circuits controlled by the add/subtract function. The add command applies a "0" to each exclusive-NOR while a subtract applies a "1" to each exclusive-NOR. The add command thereby causes each output of the shifting array to be inverted. Thus, the x_i inputs are applied non-inverted to the high speed adder in the add mode and applied inverted in the subtract mode.

4.) High-Speed Adder

The high-speed adder is a 4-bit high-speed parallel carry look-ahead adder that adds the selected function of the multiplicand, X, to the partial product presented at the K inputs. The adder also has a carry input, C_n; a carry output C_{n+4}; and four sum outputs, S_0 to S_3.

5.) Overflow and Sign Control

At the most significant end of the array, i.e. where the sign bits are processed, a problem arises when an overflow occurs as a result of (a) an addition or subtraction or (b) the need to use 2X in the adder. To overcome these overflow situations, the sign digits of the multiplicand and partial product must be repeated twice. Luckily some logic minimization is possible and the S_4 and S_5 outputs, which are the most significant bits of the 6-bit signed product, can be generated quite easily. These two outputs are required only at the most significant end of each iterative step of a multiplication. In order to re-

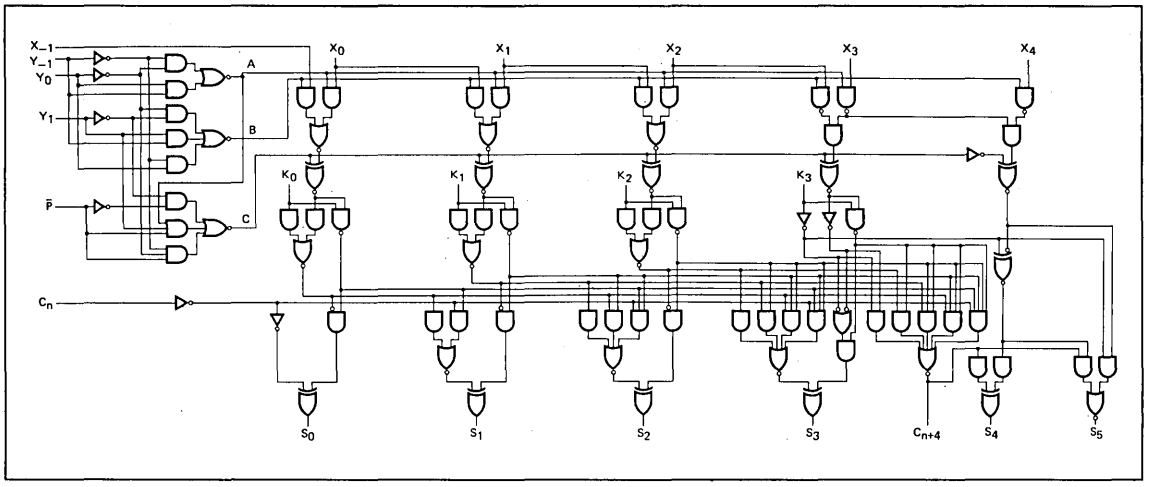


Figure 6. Logic Diagram for the Am25S05

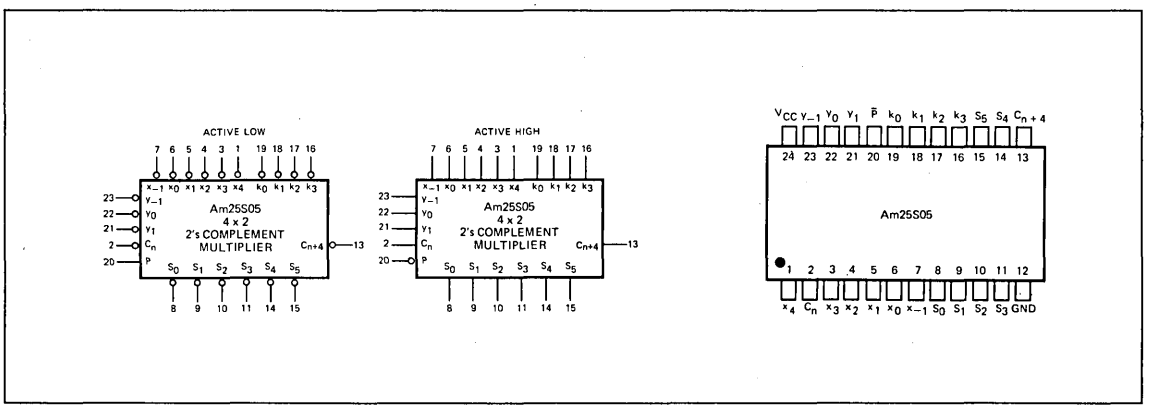


Figure 7. Logic Symbol and Connection Diagram for the Am25S05

duce input loading on x_3, an additional x_4 input is provided which is a part of this overflow circuitry. The x_4 input must be connected to x_3 at the most significant end of the array only and can be left unconnected elsewhere.

ITERATIVE ARRAYS USING THE Am25S05

Since the Am25S05 is a 2 x 4 multiplier and performs the arithmetic function S = XY + K, it can be used as an iterative cell in multiplication schemes. The number of multiplier devices required for the multiplication of a n-bit X by an m-bit Y is given by

$$\text{Number of devices} = \left(\frac{n}{4}\right)\left(\frac{m}{2}\right)$$

where X and Y are the multiplicand and multiplier, respectively. (Note – fractions must be rounded up).

When the array is extended, only the S_0 through S_3 outputs are used in the partial product until the most significant end of the array is reached. Then, the S_4 and S_5 outputs are used for the most significant bits. Thus, a 4 x 2 multiplication gives a 6-bit output; an 8 x 2 multiplication gives a 10-bit output; a 12 x 2 multiplication gives a 14-bit output and so forth. For the 12 x 2 multiplication case, S_0 through S_3 are the outputs of the two least significant multipliers and S_0 through S_5 are the outputs of the most significant multiplier to provide the 14-bit result. When the multiplier array is expanded in the Y direction, it is expanded on a row by row basis. The S outputs of one row are connected to the K inputs of the following row that are shifted up by two bits in the X direction (A weight of $2^2 = 4$). The two least significant output bits not connected (S_0 and S_1) provide two of the array outputs.

Figure 8 shows four Am25S05's connected to form a 4 x 8 array that produces a 2's complement product from a 4-bit 2's complement multiplier and an 8-bit 2's complement multiplicand. The scheme is shown for the positive logic representation; for the negative logic representation, P must be held high rather than LOW, and '1's and '0's must be reinterpreted. Since the first iteration is treated as if the previous operation were an addition, the x_{-1} and y_{-1} inputs are held at logic '0'. The S_4 and S_5 outputs are ignored except at the most significant edge of the array. The K inputs allow the accumulation

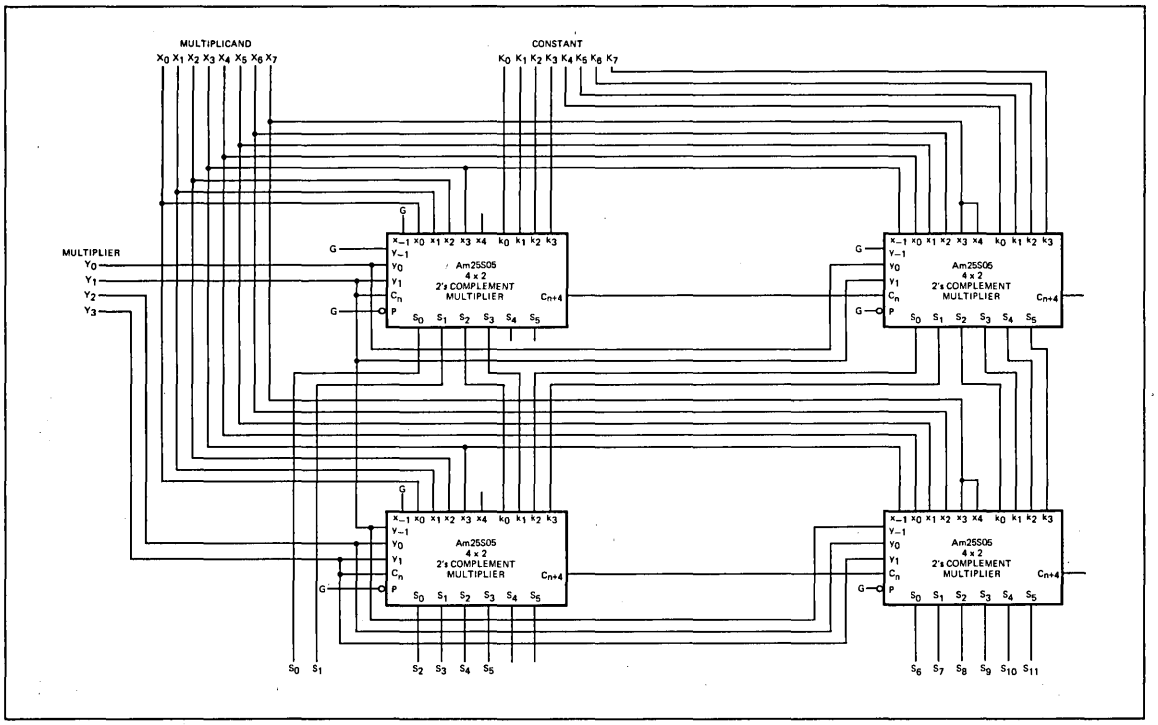


Figure 8. 2's Complement 8 x 4 Multiplication. Active High Levels

of partial products as information passes through the array.

Since at the first stage the partial product does not exist, the K inputs can be used to add in a number at the least significant end of the product. Otherwise the K inputs should be held at logic '0'. This feature is very useful as many arithmetic processes consist of a series of multiplication and additions, and these K inputs may save additional devices. For multiplication with longer word lengths, the array can be extended in both the X and Y directions.

Figure 10 shows the straightforward method of stacking multipliers so as to accumulate partial products and generate a resultant product.

Figure 9 diagrammatically shows the connection scheme for the 12 x 12 multiplier of Figure 10, the straightforward parallelogram structure. The longest propagation delay path is shown by the arrow. The typical propagation delay of this path is computed as shown in Table II. Note that this is not the maximum speed connection.

In the diagram of Figure 9, the shorthand notation inside the individual multiplier notation represents the "system" bit numbers connected to the y_0 and x_0 bits respectively. Thus, if the system words are A and B, 4·8 represent A_4 is connected to y_0 of that multiplier element and B_8 is connected to x_0 of that multiplier element. Remember, each individual Am25S05 is labeled y_{-1}, y_0, y_1, x_{-1}, x_0, x_1, x_2, x_3 and x_4. When connected in an iterative system, these inputs should be relabeled to y_{i-1}, y_i, y_{i+1}, x_{j-1}, x_j, x_{j+1}, x_{j+2}, x_{j+3} and x_{j+3} (not x_{j+4}). Then the ij nomenclature inside the element is for the subscript of the system bit numbers.

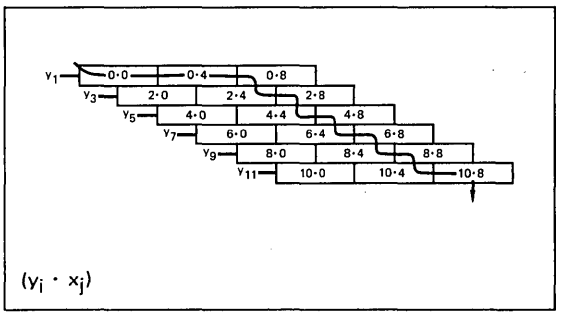


Figure 9. Diagrammatical Representation of Standard 12 x 12 Parallelogram Structure and Longest Propagation Path

TABLE II — CALCULATION OF TYPICAL PROPAGATION DELAY FOR PARALLELOGRAM 12 x 12 MULTIPLIER

	t_{PLH} Typical	t_{PHL} Typical	$\frac{t_{PLH} + t_{PHL}}{2}$
y_i to C_{n+4}	23 ns	20 ns	21.5 ns
C_n to C_{n+4}	8 ns	9 ns	8.5 ns
C_n to S_{03}	12 ns	10 ns	11.0 ns
k_i to C_{n+4}	6.5 ns	10 ns	8.25 ns
4 Additional C_n to S_{03} and k_i to C_{n+4} paths			77.0 ns
C_n to S_{45}	15 ns	13 ns	14.0 ns
		Total	140.25 ns

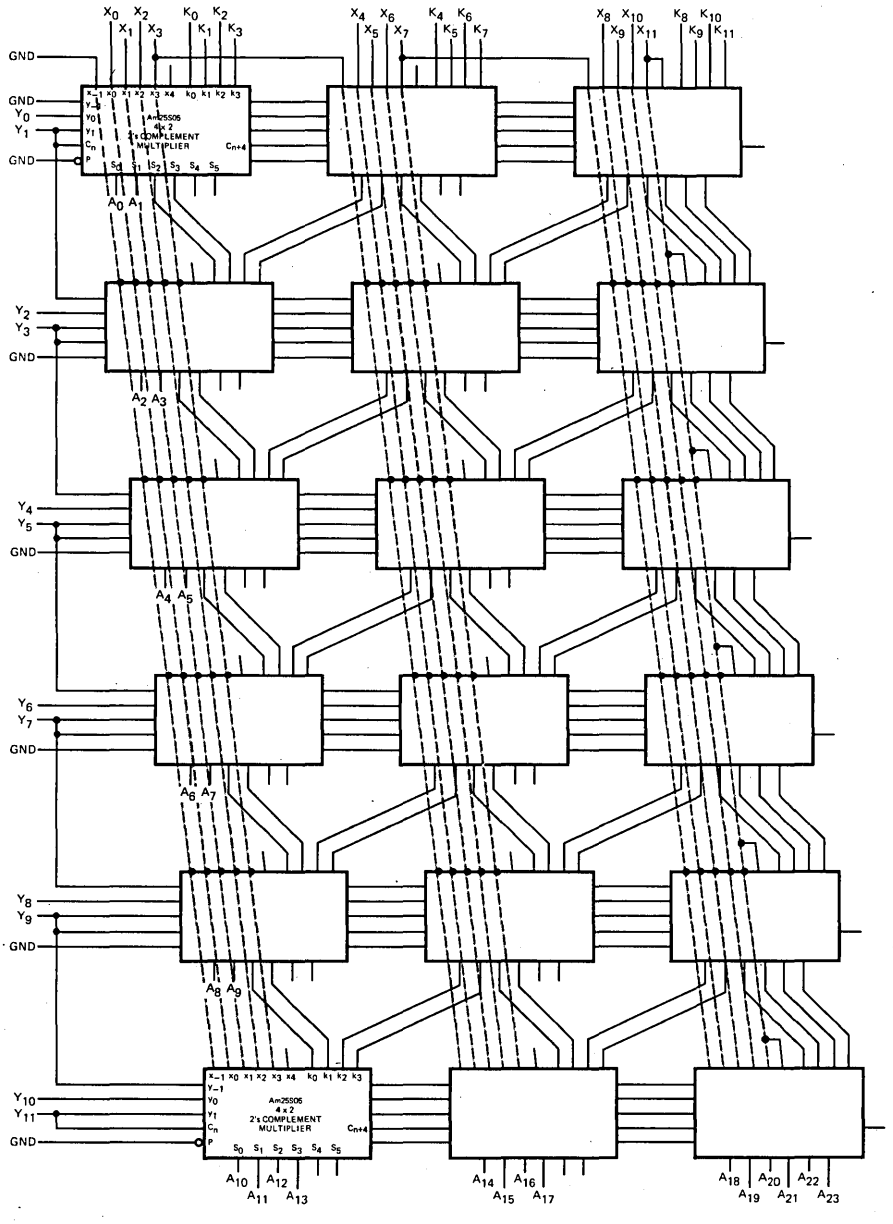


Figure 10. 12 x 12 Multiplier in Parallelogram Structure

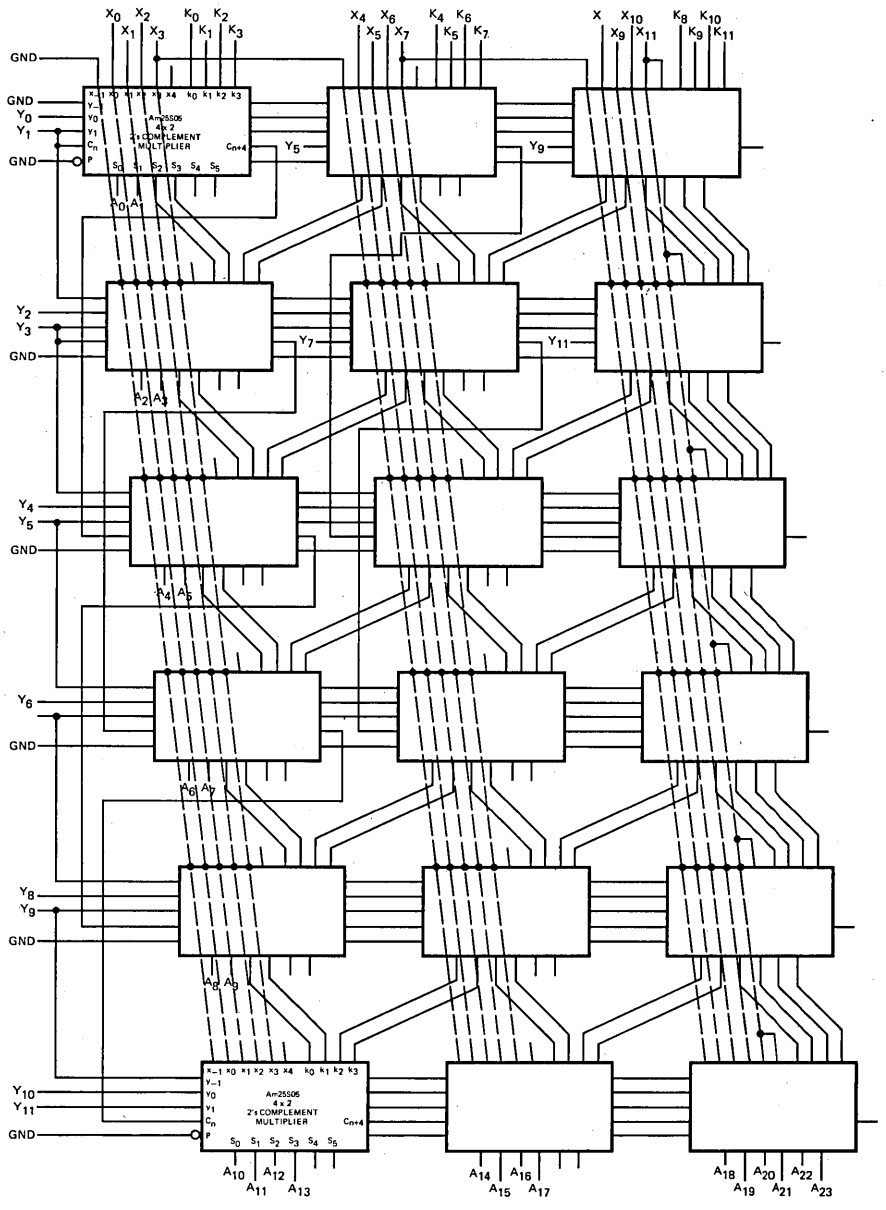


Figure 11. High Speed 12 x 12 2's Complement Multiplication

A second, faster configuration for the connection of a 12 x 12 multiplier in a parallelogram-type structure is shown in the connection diagram of Figure 11 and diagramatically in Figure 12. The significant difference between the connection in Figure 11 and the connection in Figure 10 involves the y inputs connected to the carry inputs. Notice in Figure 10 that there are y inputs going into carry inputs down the left edge of the array to add "1" at the LSB of the partial product during subtraction. Every odd y_{i+1} goes into a carry of weight i. However, within the array there are carry signals lying in the critical speed path with the same weight as these y inputs. By interchanging some of these y inputs with carries higher up in the array, it is possible to shorten the critical speed path. For example, the carry out of the first Am25S05 has a weight of 2^4 as does the y_5 input in the third row carry in. By interchanging these two signals as shown in Figure 11, the first Am25S05 is removed from the critical speed path. The carry between the first and second devices in the second row has a weight of 2^6 and may be interchanged with the y_7 signal. This interchanging may be continued across and down the array wherever applicable. The general philosophy of this method is to equalize the delays through the array from the top to all parts of the output rather than having some output bits available very rapidly and others more slowly. The result is that the longest propagation delay path will also be decreased. .Table III shows the computation for the typical propagation delay of the longest path for this connection.

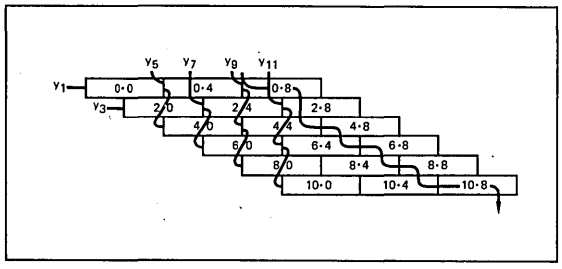


Figure 12. Diagrammatical Representation of High-Speed 12 x 12 Parallelogram Structure and Longest Propagation Path

TABLE III – CALCULATION OF TYPICAL PROPAGATION DELAY FOR 12x12 MULTIPLIER WITH CARRIES MOVED

	t_{PLH} Typical	t_{PHL} Typical	$\frac{t_{PLH} + t_{PHL}}{2}$
y_i to S_{03}	23 ns	23 ns	23 ns
k_i to S_{03}	13.5 ns	9.5 ns	11.5 ns
k_i to C_{n+4}	6.5 ns	10 ns	8.25 ns
C_n to S_{03}	12 ns	10 ns	11.0 ns
2 Additional k_i to C_{n+4} and C_n to S_{03} paths	2(8.25 +11.0)ns		38.5 ns
k_i to C_{n+4}	6.5 ns	10 ns	8.25 ns
C_n to S_{45}	15 ns	13 ns	14.0 ns
		Total	114.5 ns

A third configuration for a 12 x 12 multiplier is shown diagrammatically in Figure 13. In this structure, four of the Am25S05's have been moved vertically while maintaining the relative partial sum weights. This results in an increase in speed over the standard parallelogram structure by decreasing the maximum propagation path length. The speed of this triangular structure, Figures 13 and 15, is the same as that of the parallelogram structure with carries moved, Figures 11 and 12.

Figure 14 diagrammatically illustrates the connection scheme for 16 x 16 arrays connected in the three types of structures previously described. In each method the carry-in connection

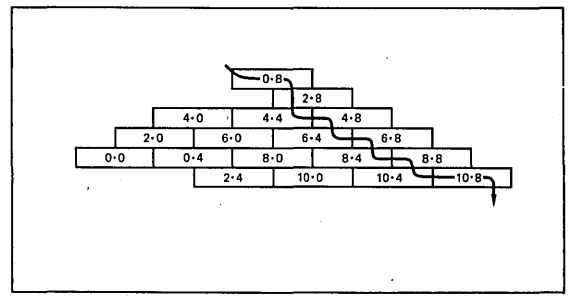


Figure 13. Diagrammatical Representation of 12 x 12 Multiplier in Triangular Array

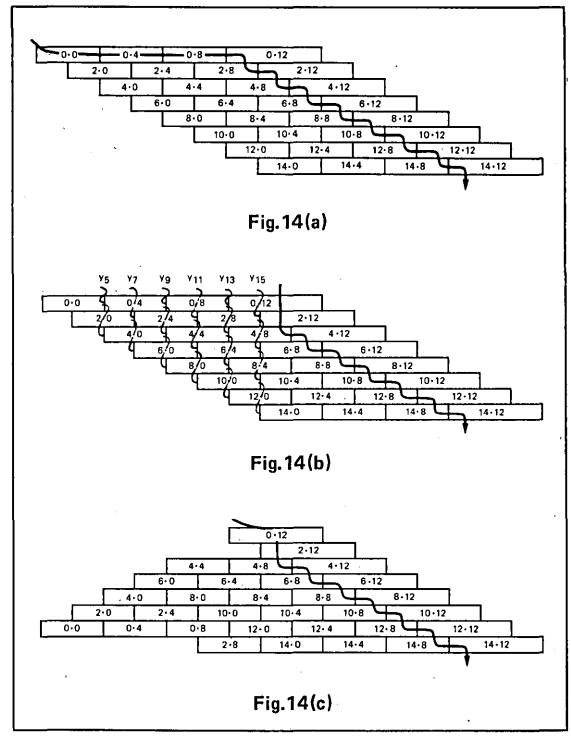


Figure 14. 16 x 16 Multiplier Connection Schemes

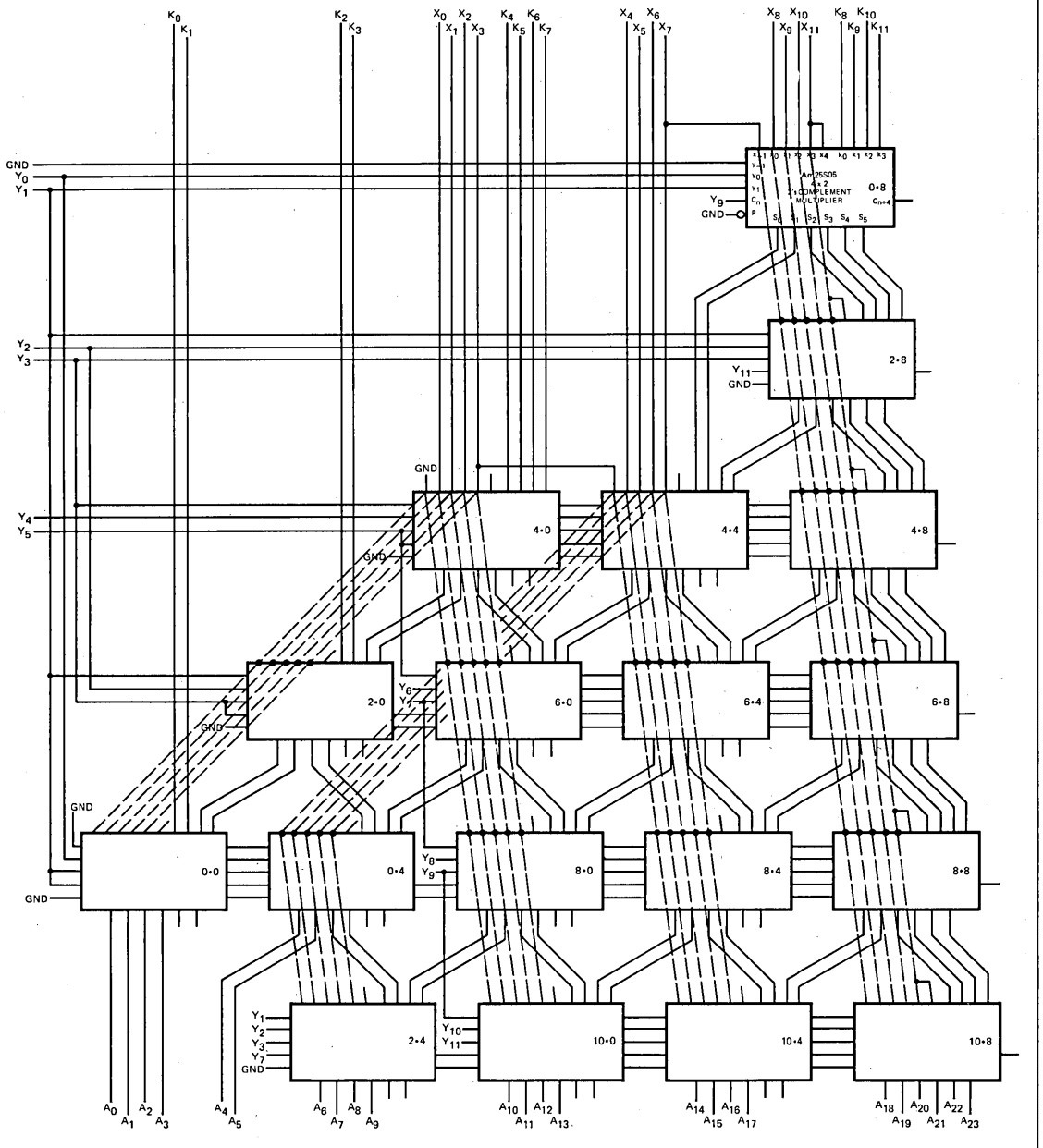


Figure 15. Connection for 12 x 12 Configuration in the Triangular Array.

TABLE IV – TYPICAL MULTIPLICATION TIME IN NANOSECONDS.

Array Size Y x X	Number of Am25S05's	Time (ns) Method 1	Time (ns) Method 2 Method 3
4 x 4	2	39	–
4 x 8	4	55	–
4 x 12	6	64	–
8 x 8	8	94	76
8 x 12	12	102	94
8 x 16	16	111	102
12 x 12	18	141	115
12 x 16	24	149	132
12 x 20	30	157	141
16 x 16	32	188	153
16 x 20	40	196	171
16 x 24	48	205	179
20 x 20	50	235	192
20 x 24	60	243	209
20 x 28	70	251	218
24 x 24	72	282	230
24 x 28	84	290	248
24 x 32	96	299	256
28 x 28	98	329	269
28 x 32	112	337	286
32 x 32	128	376	307

to the C_n level is shown. If no connection is shown, it is assumed that C_{n+4} is connected to the next C_n. Table IV shows the delays and package count for various size multiplier arrays using these three connection methods.

FASTER MULTIPLICATION USING ADDITIONAL ADDERS

If faster multipliers are required, the multiplication array can be split into several parts and the partial products from these parts added using high-speed carry look-ahead adders. This method results in a substantial increase in speed – especially for larger multipliers – with relatively few additional packages. One connection for a 16 x 16 multiplier using one level of additional partial product adders is shown diagrammatically in Figure 16.

This method involves breaking the array into two 8 x 16 indirectly structured arrays. The first contains all X connections and the Y connections to the 0, 1, 4, 5, 8, 9, 12 and 13 bits. The second array contains all X connections and the Y connections to the 2, 3, 6, 7, 10, 11, 14 and 15 bits. In all cases, the y_{i-1} bit is connected to the correct weight bit. For example, y_{i-1} is connected to bit 5 for $y_0 = 6$ and $y_1 = 7$. Notice that for both 8 x 16 structures, the y_{i-1} bits are cross coupled to the other array. The typical speed computation for this connection is shown in Table V.

Another connection scheme for a 16 x 16 multiplier using three additional partial product adders (two levels) is shown in Figure 17. Here, the multiplier is broken into four 4 x 16 arrays. Then the outputs of two of the arrays are combined in one high-speed adder and at the same time the outputs of the other two arrays are combined in another high speed adder.

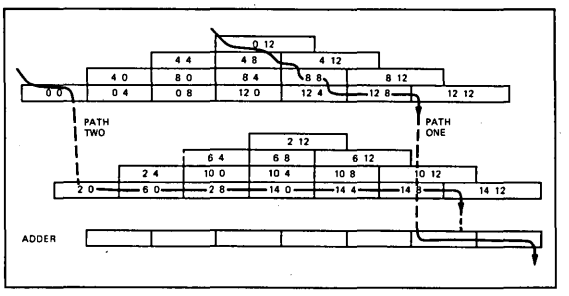


Figure 16. Multiplier Connection with One Level of Additional Adders

TABLE V – CRITICAL PROPAGATION DELAY PATH FOR 16 x 16 MILTIPLIER WITH ONE LEVEL OF ADDERS.

Path One	t_{PLH} Typical	t_{PHL} Typical	$\frac{t_{PLH} + t_{PHL}}{2}$
y_i to S_{03}	23.0 ns	23.0 ns	23.0 ns
k_i to C_{n+4}	6.5 ns	10.0 ns	8.25 ns
C_n to S_{03}	12.0 ns	10.0 ns	11.0 ns
k_i to S_{03}	13.5 ns	9.5 ns	11.5 ns
k_i to C_{n+4}	6.5 ns	10.0 ns	8.25 ns
C_n to C_{n+4}	8.0 ns	9.0 ns	8.5 ns
C_n to S_{03}	12.0 ns	10.0 ns	11.0 ns
A to C_{n+4}	Am54S/74S181	Assumed	12.5 ns
C_n to F	Am54S/74S181	Assumed	7.0 ns
			Total 101.0 ns
Path Two			
y_i to S_{03}	23.0 ns	23.0 ns	23.0 ns
k_i to C_{n+4}	6.5 ns	10.0 ns	8.25 ns
C_n to C_{n+4}	8.0 ns	9.0 ns	8.5 ns
4 Additional C_n to C_{n+4}	4(8.5 ns)		34.0 ns
C_n to S_{03}	12.0 ns	10.0 ns	11.0 ns
B to C_{n+4}	Am54S/74S181	Assumed	12.5 ns
C_n to F	Am54S/74S181	Assumed	7.0 ns
			Total 104.25 ns
			~105 ns

The resultant sums of the two high speed adders are combined in a third high speed adder which gives the total multiplication result. The typical speed computation for the longest path of this connection is shown in Table VI.

The advantage of the scheme shown in Figure 17 is that about one-half of the total delay is in the external adder. A further decrease in the average multiplication time can be achieved by storing the partial sums in registers or latches, then adding the stored parts in the high speed adders. This results in a two-step time sequenced mode of operation.

TIME-SEQUENCED MULTIPLIERS

The Am25S05 can be used as the main element in a time-sequenced multiplier. This is illustrated in Figure 18. The multiplier and partial product are shifted two places after each

iteration. Three single-length registers are required: one holds the multiplicand; the other two hold the double-length product. The least significant part of this double-length register originally holds the multiplier, which is sequentially shifted out during the computation. A shift of two places is obtained by splitting the multiplier and partial product into odd and even parts and placing the odd bits in one shift register and the even bits in the other. A shift of one place of both registers then effectively acts as a shift of two places.

The scheme can be extended to use any number of even multiplier bits. As the number of bits increases, the multiplication time increases, and the amount of ancillary hardware increases. When Am25S05's are used in a combinational array, the array does not require any additional devices. Time-sequenced multipliers are worthwhile mainly if the word lengths are long or if the auxiliary registers can be shared with other arithmetic operations. This is one example of a serial-parallel multiplier.

INTEGER MULTIPLICATION

The Am25S05 can multiply 2's complement numbers in either integer or fractional form. The primary difference is in the thought process of the designer. When the binary patterns are treated as integers, the 2's complement numbers can be represented as

$$X = x - x_s\,2^{n-1}$$
$$Y = y - y_s\,2^{m-1}$$
$$K = k - k_s\,2^{p-1}$$

where

x_s = sign bit of X (one or zero)
y_s = sign bit of Y (one or zero)
k_s = sign bit of K (one or zero)
x = magnitude bits of X (less sign)
y = magnitude bits of Y (less sign)
k = magnitude bits of K (less sign)
n = number of bits in X word
m = number of bits in Y word
p = number of bits in K word

For example, if six bits are assumed for X, n = 6 and the sign bit has a weight of $-2^{6-1} = -2^5 = -32$. The other magnitude bits have their normal weight and since there are five other magnitude bits, they are 2^0, 2^1, 2^2, 2^3, and 2^4. Thus, 2's complement integer numbers for n = 6 bits are as shown below:

Integer Decimal Number Equivalent	Magnitude bits					
	-2^5 Sign	2^4	2^3	2^2	2^1	2^0
	−32	16	8	4	2	1
14	0	0	1	1	1	0
31	0	1	1	1	1	1
0	0	0	0	0	0	0
−7	1	1	1	0	0	1
−25	1	0	0	1	1	1
−32	1	0	0	0	0	0

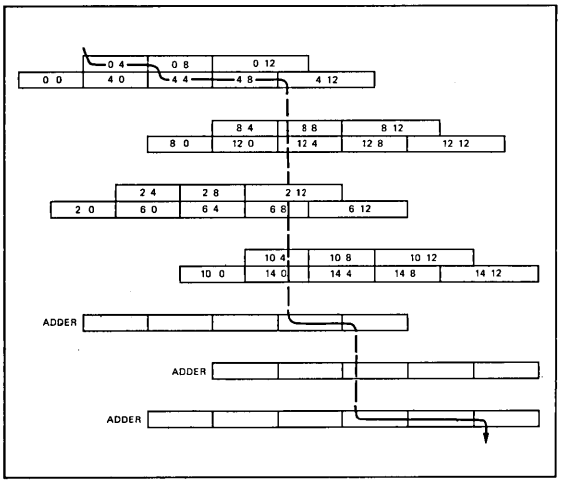


Figure 17. Multiplier Connection with Two Levels of Additional Adders

TABLE VI – CRITICAL PROPAGATION DELAY PATH FOR 16 x 16 MULTIPLIER WITH TWO LEVELS OF ADDERS

	t_{PLH} Typical	t_{PHL} Typical	$\frac{t_{PLH} + t_{PHL}}{2}$
y_i to C_{n+4}	23.0 ns	20.0 ns	21.5 ns
C_n to S_{03}	12.0 ns	10.0 ns	11.0 ns
k_i to C_{n+4}	6.5 ns	10.0 ns	8.25 ns
C_n to C_{n+4}	8.0 ns	9.0 ns	8.5 ns
C_n to S_{03}	12.0 ns	10.0 ns	11.0 ns
A to C_{n+4}	Am54S/74S181 Assumed		12.5 ns
C_n to F	Am54S/74S181 Assumed		7.0 ns
A to C_{n+4}	Am54S/74S181 Assumed		12.5 ns
C_n to C_{n+4}	Am54S/74S181 Assumed		7.0 ns
C_n to F	Am54S/74S181 Assumed		7.0 ns
		Total	106.75 ns

When the product of X and Y is considered, the following equation results:

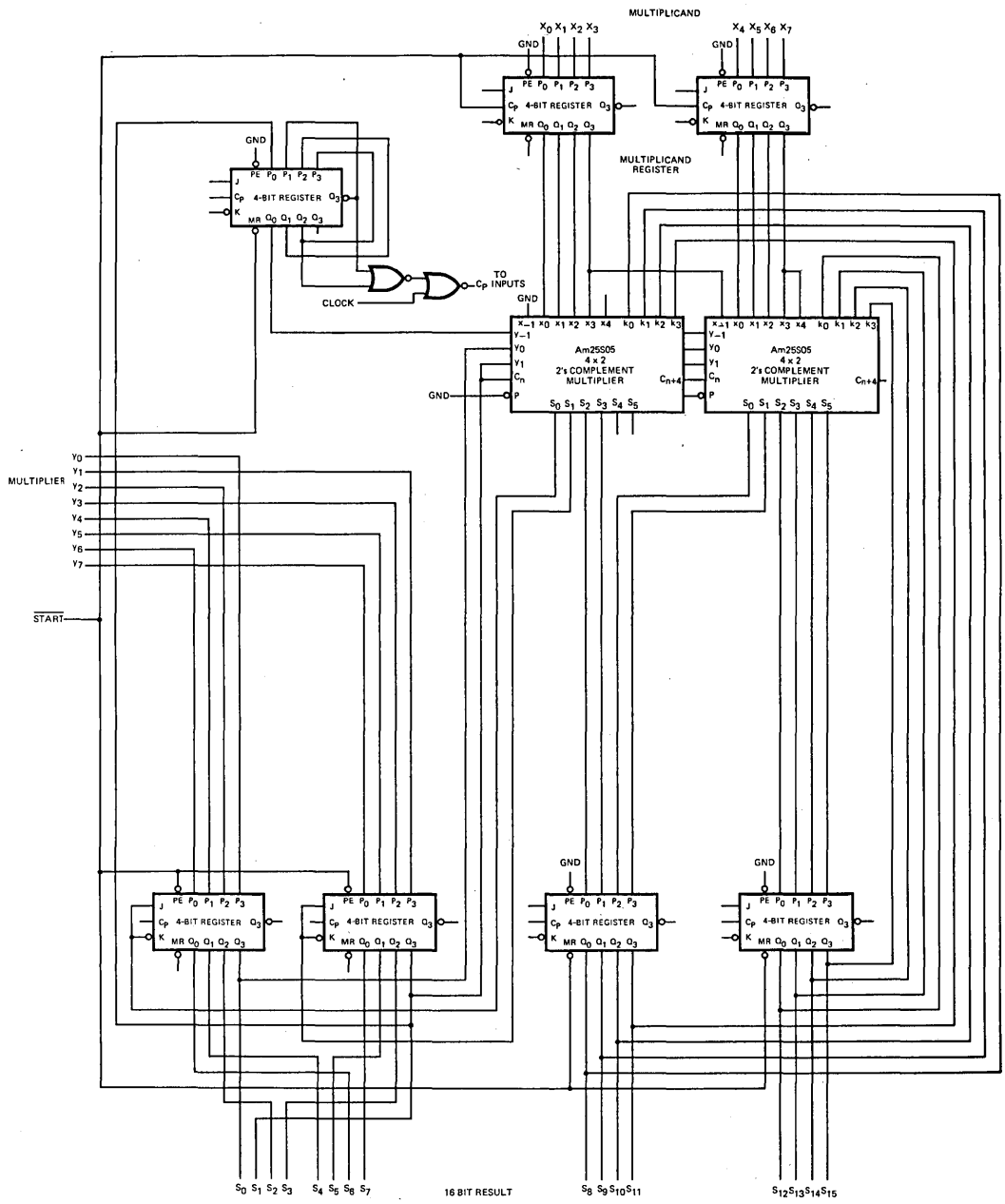
$$S = XY = x_s y_s\,2^{m+n-2} - xy_s\,2^{m-1} - yx_s\,2^{n-1} + xy$$

The 2's complement product requires m + n bits in order to represent all possibilities. Note that there is only one condition where the m + n bits are required; that condition being:

$$X = -2^{n-1} \text{ and } Y = -2^{m-1}$$

This condition gives $S = XY = 2^{m+n-2}$ which requires m + n digits in a 2's complement signed integer number.

Consider n = 6 and m = 4, then x_s has weight −32 and y_s has weight −8. For X = −32 and Y = −8, the product XY is +256. The 2's complement representation is 0100000000. Ten bits are required to properly represent the 2's complement number. All other combinations of values for X and Y require only m + n −1 bits to represent the 2's complement number. For n = 6 and m = 4 in this case, the ninth bit represents the product sign. Consider (+7) x (−31) is equal to −217 or



Note: 4-bit register is Am54S/74S195

Figure 18. 8 x 8 Time Sequenced Multiplier

100100111. Notice that 1100100111, the ten bit 2's complement representation is identical in value.

The *general* requirement for the product solution of XY is:

$$S = XY = s - s_s\, 2^{m+n-1}$$

and all binary operations must be carried through m + n bits in the product soltuion unless a simplification is assumed.

In the Am25S05 (as well as the Am2505 and Am25L05), the sum output, S, of the device is:

$$S = XY + K.$$

This can be seen in Figure 6.

The devices are designed such that in an iterative array, the K inputs to the adder are available only at the initial least significant partial product input. Thus in an iterative system, the sum is defined as:

$$S = x_s y_s\, 2^{m+n-2} - xy_s\, 2^{m-1} - (yx_s + k_s)\, 2^{n-1} + xy + k$$

The k_s term can contribute at weight 2^{n-1} and the k term at weight $2^0 = 1$. Thus, m + n bits are sufficient to contain all possible values of S = XY + K.

FRACTIONAL MULTIPLICATION

Fractional multiplication using the Am25S05 is identical with integer multiplication but the notation is changed. The fractional number range is usually limited to $-1 \leqslant X \leqslant 1-2^{-(n-1)}$.

The fractional 2's complement binary numbers can be represented as:

$$X = x\, 2^{-(n-1)} - x_s$$
$$Y = y\, 2^{-(m-1)} - y_s$$
$$K = k\, 2^{-(p-1)} - k_s$$

where the notation is as with integer arithmetic. The sign bit now has a weight of $-2^0 = -1$ and the other magnitude bits have their normal fractional weight.

Two's complement numbers for n = 6 are as shown below.

Fractional Equivalent	-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}
	−1	1/2	1/4	1/8	1/16	1/32
14/32 = 7/16	0	0	1	1	1	0
31/32	0	1	1	1	1	1
0	0	0	0	0	0	0
−7/32	1	1	1	0	0	1
−25/32	1	0	0	1	1	1
−32/32 = −1	1	0	0	0	0	0

The notation difference in the fractional representation is that all the integer representations have been divided by $2^{(n-1)}$.

The fractional product XY is

$$S = XY = x_s y_s - x_s y\, 2^{-(m-1)} - y_s\, x\, 2^{-(n-1)} + xy\, 2^{-(m+n-2)}$$

Again, m+n bits are required to cover all possible combinations. Note that X = −1 and Y = −1 results in XY = +1 which is beyond the normal range. In order to cover this possibility, the sign bit should be given a weight of −2 (instead of −1); the next most significant bit is weight +1, the next is +1/2, and so forth. If the −1 times −1 possibility is excluded only m+n−1 bits are required.

The Am25S05 used in an iterative structure produces a fractional sum S = XY + K, but the K inputs are now at the same weight as the least significant partial product inputs. Thus $K = k\, 2^{-(m+n-2)} - k_s\, 2^{-(m-1)}$. The sum is:

$$S = XY + K = x_s y_x - (x_s y + k_s)\, 2^{-(m-1)} - y_s\, x\, 2^{-(n-1)} + (xy + k)\, 2^{-(m+n-2)}$$

This general equation requires the sign bit to have a weight of −2 and all arithmetic to be carried to m+n bits to represent the two's complement solution.

In conventional minicomputer 2's complement multiplication of fractional numbers, the product, S, has only m+n−1 bits and is constrained in the range of $-1 \leqslant S \leqslant 1-2^{-(m+n-2)}$ with the most significant bit (sign bit) having a weight of −1. Outside of this range, an overflow indication is given. The Am25S05 produces a product of m+n digits so that all product results XY+K are correctly represented and the sign bit has weight −2. Notice that if K = 0 (the condition in conventional machine multiplication), m+n digits are required only for X = Y = −1. Thus if S is used with m+n−1 bits, the most significant bit of the Am25S05 array can be ignored, and an overflow indication can be generated by $S_{-2} \oplus S_{+1}$ ($S_5 \oplus S_4$ on the most significant Am25S05 output).

In fractional notation, the K inputs add to the least significant end of the adder. If K is negative, the k_s bit is in effect repeated completely across the most significant part of the product via the x_4 input and S_4 and S_5 outputs. If a double length K addition is required, an adder can be appended to the most significant part of the product with the carry-in terminal connected to k_s so that the "1"s across the most significant part of the product are removed and the desired most significant bits added. Figure 19 shows a 4 x 4 multiplication with double length addition while Figure 20 shows numeric examples of 4 x 4 multiplications.

In the connection scheme of Figure 19, an Am25S05 has been used as an adder to provide the desired overflow operation at the most significant end of the word. With the y input connection shown, the adder performs S = X plus K with the S_4 output correct for this 2's complement number range. The S_5 output is not used. If K is limited to the range of $-1\text{-}1/8 \leqslant K \leqslant \frac{63}{64}$, an adder such as the Am54S/74S181 or Am54S/74S283 can be used to perform the addition of the most significant K bits. In this case only 8 bits will be required to represent the product and it will be in the range of $-2 \leqslant S \leqslant 1\ \frac{63}{64}$.

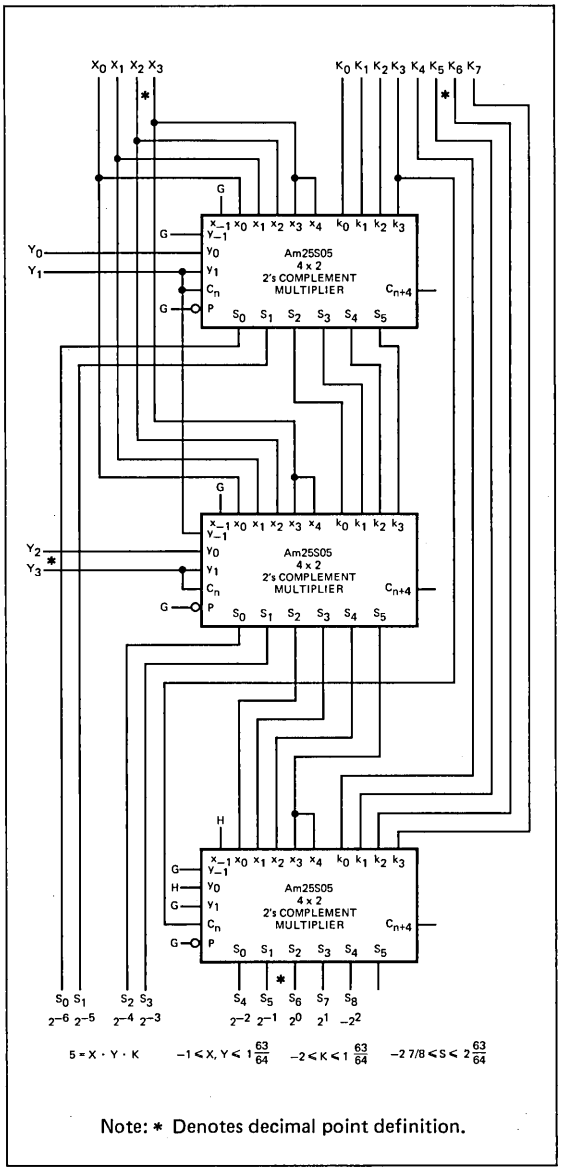


Figure 19. 4 x 4 Fractional Double Length Multiplication and Addition.

	OVER-FLOW	−1	1/2	1/4	1/8	1/16	1/32	1/64	Fractional value
Example #1									
X		0	1	0	1				5/8
Y		0	0	1	1				3/8
XY	0	0	0	0	1	1	1	1	15/64
+K	[0	0	0	0]	0	0	1	1	3/64
	Sign extended via k_s								
XY+K	0	0	0	1	0	0	1	0	18/64
Example #2									
X		1	0	0	0				-7/8
Y		0	1	0	0				1/2
XY	1	1	1	0	0	1	0	0	-28/64
+K	[1	1	1	1]	1	1	1	1	-1/64
	Sign extended via k_s								
XY+K	1	1	1	0	0	0	1	1	-29/64
Example #3									
X		1	1	0	1				-3/8
Y		1	0	0	1				-7/8
XY	0	0	0	1	0	1	0	1	
+K	[0	0	0	0]	0	0	0	0	0
	Sign extended via k_s								
XY+K	0	0	0	1	0	1	0	1	21/64

Figure 20. Three Examples of Two's Complement 4 x 4 Multiplications

ROUND-OFF

It is often convenient to use only the most significant half of a product. This product should be rounded off; that is, it should approximate the best n-bit answer possible. This can be done by examining the least significant half of the product, and if it is greater than or equal to a certain value, (normally 1/2 that of the least significant digit of the truncated product) adding a '1' to its most significant position.

Forming a rounded t-bit product from a conventional product constrained within the range $-1 \leqslant S \leqslant 1-2^{-(m+n-2)}$ can be accomplished by adding a '1' to the K input at weight 2^{-t}. For the case where t = m = n, this is one k position lower than the K sign digit. An example of rounding for t = m = n = 4 is shown below.

X	=	0.	0	1	1			= 3/8
Y	=	0.	1	0	1			= 5/8
XY	=	00.	0	0	1	1	1	1 = 15/64
+K	=	00.	0	0	0	1	0	0
S	=	00.	0	1	0	0	1	1

Rounded t-bit product from the 2t-bit product is

S	=	0.	0	1	0	= 1/4

For the case m = 4 and n = 8, the sum of n+m is 12. If a six bit rounded product is desired, a "1" is added at weight 2^{-6}. If an eight bit rounded product is desired, a one is added at weight 2^{-8}.

If the sum output is not constrained as before but covers the range $-2 \leqslant S \leqslant 2-2^{-(m+n-2)}$, care must be taken when rounding. For the case where m = n is rounded to m(or n) bits the "1" is to be added at the k_s (sign) weight. The multiplier would treat this as a negative k_s sign bit and it would be extended up through the array most significant bit. Therefore, this connection cannot be made. It is recommended that for this case, the k_s sign bit be connected to logic "0" and all lower order k bits be connected to logic "1". This comes very near the desired rounding criteria; otherwise an additional adder is required at the output to add a one at the k_s weight only.

TABLE VII — WORST CASE EFFECT OF TRUNCATION BY REMOVING MULTIPLIERS

12 bit LSB		Truncated Bits												
2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	Multiplier
14	13	12	11	10	9	8	7	6	5	4	3	2	1	removed
									(1)	1	1	1	1	0·0 removed
							(1)	1	1	1	1			2·0 removed
						1	0	0	1	1	0	1	1	effect
					1	1	1	1	⊗					0·4 removed
				1	0	0	1	1	1	1	0	1	1	effect
					1	1	1	1	1					4·0 removed
			1	0	0	0	1	1	0	1	0	1	1	effect
			1	1	1	1	⊗							2·4 removed
		1	0	1	1	1	1	1	0	1	0	1	1	effect
			1	1	1	1	1							6·0 removed
	1	0	0	1	1	1	0	1	0	1	0	1	1	effect

TRUNCATION

If the user is prepared to accept a truncated product where the product is incorrect by some fraction of a least significant digit, the number of IC's required for the multiplication can be reduced. The designer can determine the accuracy required for his application and remove packages as long as the error does not exceed the desired accuracy.

A simple procedure for examining the effects of removing each Am25S05 is as follows. Each 4 x 2 multiplier can effect 5 bits of the output partial product by its S_0, S_1, S_2, S_3, and C_{n+4} output. As each package is removed, the effect on each bit level can be evaluated by summing the total bits involved.

This is best shown by an example. Assume a 12 x 12 multiplier with a 24-bit result (Reference Figure 12). When the 0·0 multiplier (yx) is removed, the 5 LSB's are effected. If the 2·0 multiplier is removed, then the first eight LSB's are effected as shown in Table VII. If the 0·4 multiplier is also removed, then two multipliers have been removed from row one and one multiplier from row two. Only the first nine bits of row one can be effected by the removal of two multipliers. Since C_{n+4} of 0·0 was considered before, the S_0 bit of 0·4 cannot be added a second time. Therefore, when the 0·4 multiplier is removed, only the S_1, S_2, S_3 and C_{n+4} bits effect the result. This is shown in Table VII by cancelling the S_0 bit of "0·4 removed". When the 4·0 multiplier is removed from row 3 the S_0, S_1, S_2, S_3 and C_{n+4} bits effect the result. When the 2·4 multiplier is removed from row 2, the S_0 bit cannot be considered.

Thus, from Table VII it can be seen that when 0·0, 2·0, 0·4, 4·0 and 2·4 are removed, the first 12 LSB's are effected and the 12 bit sum output will be accurate to about 3/4 LSB at this point. Thus, 5 multiplier packages can be removed from a 12 x 12 multiplier and maintain a 3/4 LSB accuracy. Note that 18 devices are required for full accuracy. If the 6·0 multiplier is removed from row 4, the 12-bit result will be accurate to about 1 LSB, but only 12 devices are required rather than 18.

One further note on truncation; when a binary word is truncated, the accuracy is not ±1 LSB or ±1/2 LSB, etc. The truncated result can never increase the magnitude of the LSB because this would include rounding. Thus, a truncated result is always the sum, S, plus zero magnitude of the LSB and minus 1, 1/2 or 1/4 (or any other number) LSB. The magnitude always becomes more negative for either positive or negative numbers.

From this discussion, it should be apparent that the designer can remove packages and truncate the product to any desired bit length and accuracy. When the product is truncated, no speed increase usually occurs, since the removed multipliers are not in the longest critical speed path. This assumes that the highest speed connection is being used.

MULTIPLICATION IN OTHER NUMBER REPRESENTATIONS

Although 2's complement multiplication is the one most widely used, multiplication in other number representations often must be performed. The Am25S05 can be used to perform these multiplications if appropriate care is used and the proper connections are made.

UNSIGNED (Magnitude-only) MULTIPLICATION

The most straightforward technique to perform magnitude-only multiplication is to generate two "always positive" two's complement numbers. This is accomplished by adding a logic "0" as the most significant bit of each word, thereby generating a positive sign bit. This increases both the X and Y word lengths by one bit. The Am25S05 can be used "as is" to perform this multiplication and the two most significant multipliers

sum bits are ignored. Thus, if m = 4 and n = 6 in a magnitude-only representation, a 5 x 7 multiplier configuration is required. The two MSB's of the 12-bit sum are ignored which result in a 10-bit product solution in a magnitude-only representation. Note that the multiplier still performs XY + K and m + n bits are sufficient to contain all possibilities. (A 6 x 8 connection is actually used).

A second technique for unsigned multiplication also requires extending the word length one bit, but need not require a larger array. A logic "0" is appended to each word as a positive sign bit; then the LSB of each word is considered separately.

$$X_e = x_0 + 2x - x_s 2^n$$
$$Y_e = y_0 + 2y - y_s 2^m$$

Since $x_s = y_s = 0$, the extended product is

$$X_e Y_e = 4xy + 2xy_0 + 2yx_0 + x_0 y_0$$

A n-bit by m-bit multiplier array can be used to generate 4xy and a conditional adder can be used to generate $2xy_0 + 2yx_0$. The term from this adder can be added to the multiplier array at the K input. The 1, 2 and 4 show the proper weighting for each term. The term $x_0 y_0$ is just an AND function and cannot produce a carry output. The first stage of the conditional adder produces the first bit of the product. The remaining product digits are produced at the output of the multiplier array. The sign digits x_s, y_s and k_s are held at logic 0 and the two most significant multiplier sum bits are ignored. The advantage of this connection is that the conditional adder is connected to the K inputs and in some cases the total multiplication time may be faster than if the above method is used.

It should also be noted that depending on the word lengths being used, it may only be necessary to extend one of the input words (X or Y) beyond the iterative array convenient length. Then it may be possible to use the K inputs as most of the conditional adder.

SIGN-MAGNITUDE MULTIPLICATION

The most straightforward technique for performing sign magnitude multiplication is to split the sign from the magnitude and perform the magnitude multiplication as described in the magnitude-only section. The sum sign bit is $s_s = x_s\overline{y}_s + \overline{x}_s y_s = x_s \oplus y_s$, which can be performed in an external exclusive-OR circuit. Note that for a sign magnitude notation, m = 5 and n = 7 only m+n−1 = 11 bits are needed for the sign-magnitude XY product. **Caution** — care must be taken when using the K inputs because a negative product plus K may be positive and no provision is made for this in the sign bit representation.

The notation used for a sign-magnitude word is:

$$X_{sm} = x(1-2x_s)$$
$$Y_{sm} = y(1-2y_s)$$

The $X_{sm}Y_{sm}$ product is $S_{sm} = X_{sm}Y_{sm} = xy(1-2x_s)(1-2y_s) = xy(1-2x_s-2y_s+4x_s y_s)$

The Am25S05 2's complement multiplier produces the product: $S = XY = x_s y_s 2^{m+n-2} - xy_s 2^{m-1} - yx_s 2^{n-1} + xy$

The resulting solution for the sign magnitude multiplication if the signs are included in the Am25S05 connection is

$$S_{sm} = (XY - x_s y_s 2^{m+n-2} + xy_s 2^{m-1} + yx_s 2^{n-1})$$
$$(1-2x_s-2y_s + 4x_s y_s)$$

There are four conditions for $x_s y_s$ and the correction required in each case is as shown below:

$x_s y_s$	XY_{sm}	
00	XY	(no correction)
10	$-XY - y2^{n-1}$	
01	$-XY - x2^{m-1}$	
11	$XY - 2^{m+n-2} + x2^{m-1} + y2n-1$	

Since the terms to be added begin at weight 2^{m-1}, 2^{n-1} or 2^{m+n-2}, they must operate on the most significant part of the product. Therefore, additional adders are required at the output to make the proper connection. The technique of keeping the sign bits separate from the multiplier array and setting K = 0 is recommended.

ONE'S COMPLEMENT MULTIPLICATION

One's complement multiplication does not have a straightforward method as do unsigned or sign-magnitude multiplication schemes. The notation used to represent a 1's complement number is

$$X_1 = x - x_s(2^{n-1} - 1)$$
$$Y_1 = y - y_s(2^{m-1} - 1)$$
$$S_1 = X_1 Y_1 = xy + xy_s(1-2^{m-1}) + yx_s(1-2^{n-1}) + x_s y_s(1-2^{n-1} - 2^{m-1} + 2^{m+n-2})$$

If the X and Y word length are the same, then m = n and the product reduces to:

$$S_1 = X_1 Y_1 = xy + (xy_s + yx_s)(1-2^{n-1}) + x_s y_s(1-2^n + 2^{2n-2})$$

The Am25S05 product for m = n is

$$XY = x_s y_s 2^{2n-2} - (xy_s + yx_s) 2^{n-1} + xy$$

Remembering the definitions for X and Y in 2's complement, the solution for the one's complement multiplication sum for m = n is

$$S_1 = XY + xy_s + yx_s + x_s y_s (1-2\cdot 2^{n-1})$$
$$S_1 = XY + x_s Y + y_s X + x_s y_s$$

Note that the one's complement word relates to the two's complement word as

$$X_1 = X + x_s$$
$$Y_1 = Y + y_s$$

Therefore, the one's complement solution can also be given as

$$S_1 = XY + x_s Y_1 + y_s X_1 - x_s y_s$$

The four conditions for $x_s y_s$ with m = n are:

$x_s y_s$	X_1Y_1 Result Correction Requires 2's Complement Inputs and 2's Complement Addition	X_1Y_1 Result Correction Requires 1's Complement Inputs and 1's Complement Addition	X_1Y_1 Result Correction Requires 1's Complement Inputs and 2's Complement Addition
00	XY	XY	XY
10	XY + Y	XY + Y_1	XY + Y_1−1
01	XY + X	XY + X_1	XY + X_1−1
11	XY + X + Y + 1	XY + X_1 + Y_1−1	XY + X_1 + Y_1 + 1

Since the correction to be added is at weight $2^0 = 1$, the K inputs can conveniently be used for this purpose. Note that two designs have been described. The first requires having both one's complement numbers X_1 and Y_1 available converted to 2's complement numbers X and Y. The second requires only one's complement numbers but requires an addition of −1 (in one's complement notation). Thus, a conditional adder can be used to produce $x_sY_1 + y_sX_1 - x_sy_s$, and the sum can be added to the multiplier at the K inputs.

If m is not equal to n, then the product X_1Y_1, using the Am25S05 is $S_1 = X_1Y_1 = XY + xy_s + yx_s + x_sy_s (1 - 2^{n-1} - 2^{m-1})$. Note that the same type of solution is possible as with m = n. $S_1 = X_1Y_1 = XY + y_sX_1 + x_sY, - x_sy_s$.

Thus, a conditional adder can be used and the solution is identical with the four conditions shown for x_sy_s when m = n. The only difference is that the adder will use the m and n word lengths which must be extended sufficiently to cause repetition of the sign bit across the multipliers array.

THE y_{-1} BIT

It has been stated repeatedly that the multiplier array performs the function S = XY + K. This result assumes that the y_{-1} system bit is held at zero. If y_{-1} is held at logic "1", the array function becomes S = XY + K + X = X (Y+1) + K which may be expanded to include y_{-1} as S = XY + K + y_{-1} X = X (Y+y_{-1}) + K where y_{-1} is either logic 1 or 0. There are some applications of the multiplier array that can take advantage of this ability to add X to the product XY.

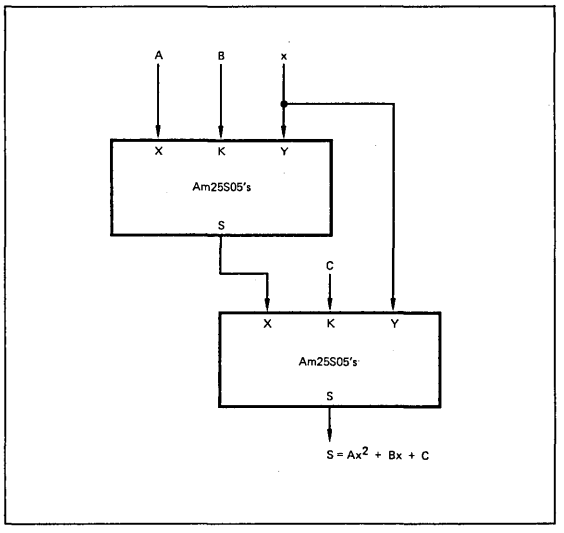


Figure 21. Polynomial Evaluation

APPLICATIONS

The multiplier is ideal for hardware multiplication in general and special purpose computers, digital filter circuits, Fast Fourier Transform (FFT) processors, and special purpose digital machines. In the applications described in the following figures, the multiplier array is shown as a box which performs the function S = XY + K. Care must be exercised in scaling the numbers appropriately. Likewise, various other registers and adders are assumed to have a word length sufficient to handle the accuracy and magnification required. Figure 21 shows two multiplier arrays connected to generate a quadratic in x. This can be extended to form polynomials with higher powers of x.

A multiplier array connected to perform higher order polynomial evaluation in a time sequenced mode is shown in Figure 22. Note that the output register is initialized to 0 and the constants sequentially applied to the K input.

Figure 23 shows a single-pole, low-pass, recursive digital filter. The z-plane pole location is at z = C where C is a constant. The register is used as the unit time delay operator z^{-1}. The K inputs can be used for the least significant bits of the data

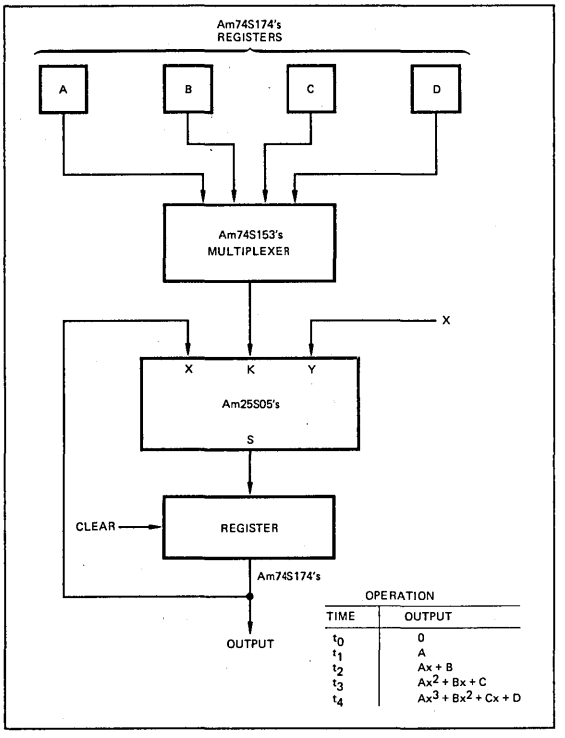


Figure 22. Time Sequenced Polynomial Evaluation

input E_i. In some designs, only the K input bits are required for the entire E_i input word. The DC gain at z = +1 is 1/(1-C).

A single pole, high-pass recursive digital filter is shown in Figure 24. The z-plane pole location is at z = C. Note the z-plane zero at z = 1 which results in a DC gain of 0, i.e., a high-pass filter.

A two-pole, low-pass recursive digital filter of canonical form is shown in Figure 25. This block produces a complex conjugate pair of poles in the z-plane when $|4D| > |C^2|$. The pole locations are $z_1, z_2 = \frac{C}{2} \pm j\frac{\sqrt{|C^2-4D|}}{2}$. This configuration can be used as a two-pole building block in more complex Butterworth or Chebychef filters. The DC gain is 1/(1−C+D). This value is usually very close to the peak internal build up which occurs at a frequency just below the filter break frequency. Also shown is the case in which the input word length has been extended to full length.

Figure 26 shows a general two-pole, two-zero recursive canonical structure. By appropriately selecting the A, B, C, and D constants in this configuration, the building block can be used as a high-pass, low-pass, or band-pass digital filter. The DC gain is (1+A+B)/(1−C+D). The pole locations are the same as for Figure 24. The zero pair will be complex if A is negative and $|4B| > |A^2|$. If A = −2 and B = 1, then the zeros are at $(z-1)^2$ and a two-pole, high-pass filter results.

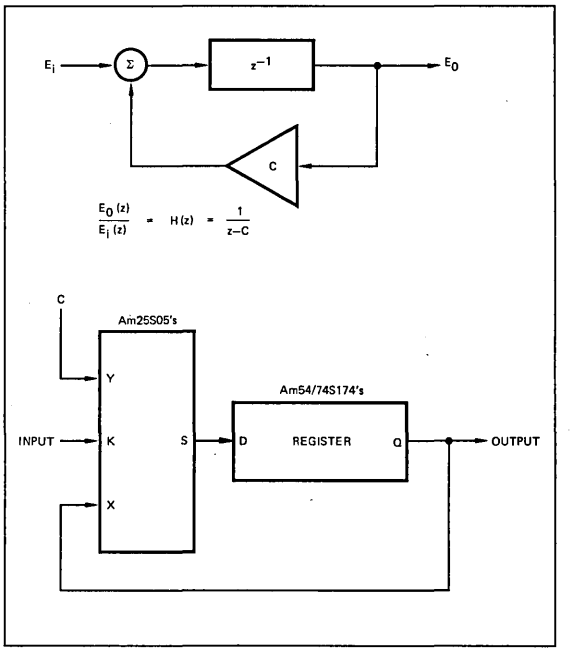


Figure 23. Single-Pole, Low Pass Recursive Digital Filter

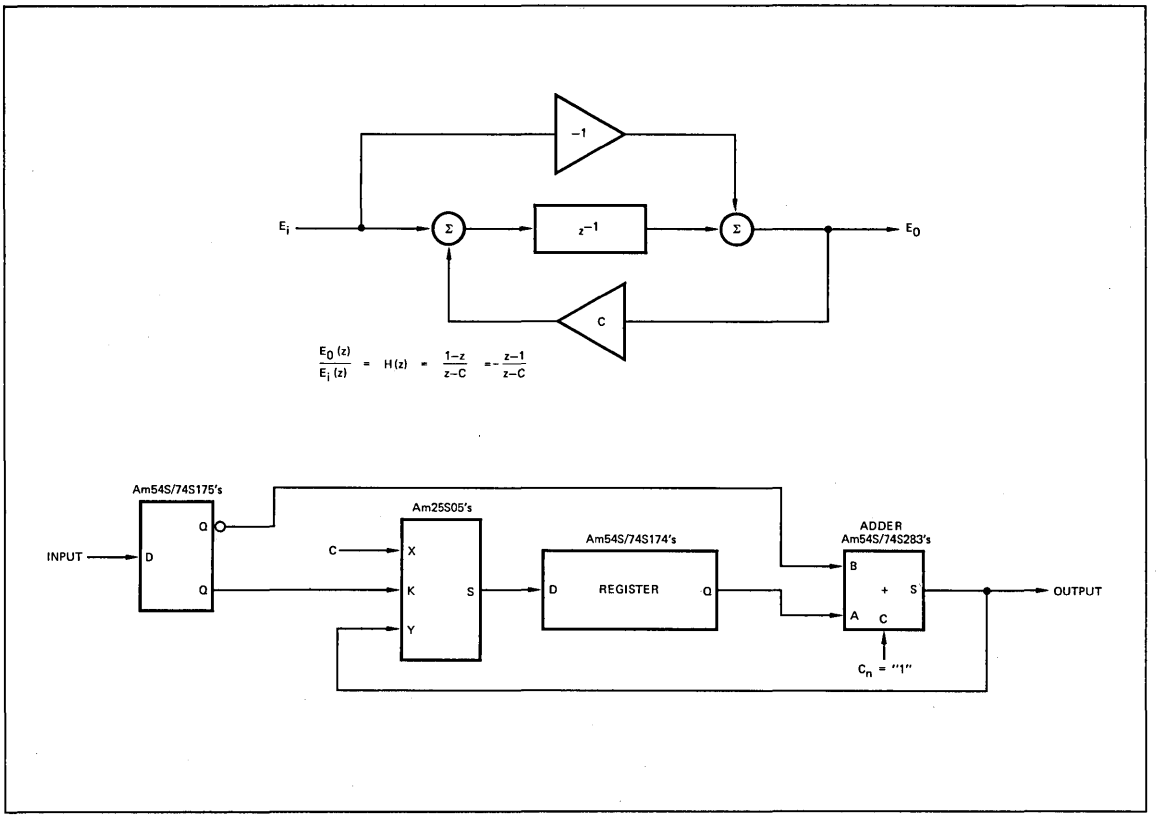


Figure 24. Single-pole, High-pass Recursive Digital Filter.

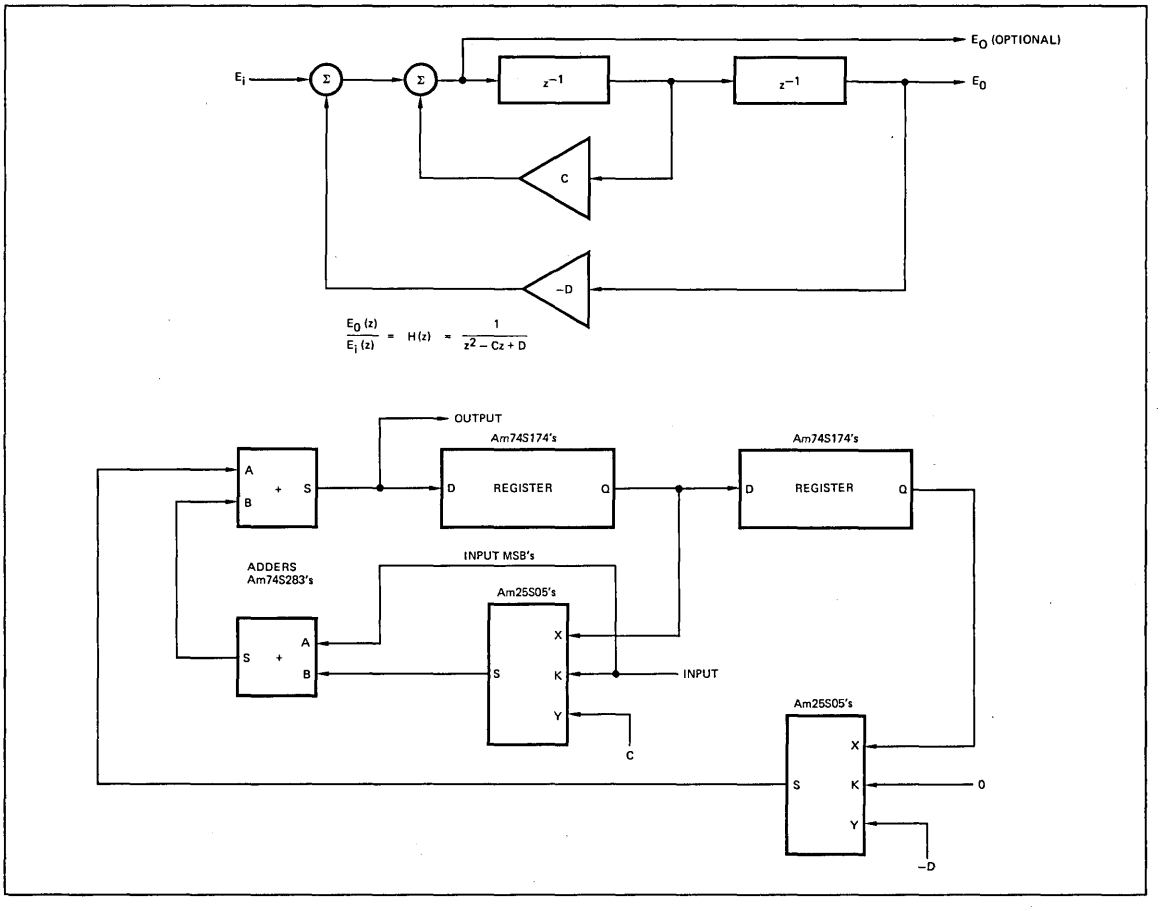


Figure 25. Two-pole, Low-pass Recursive Digital Filter

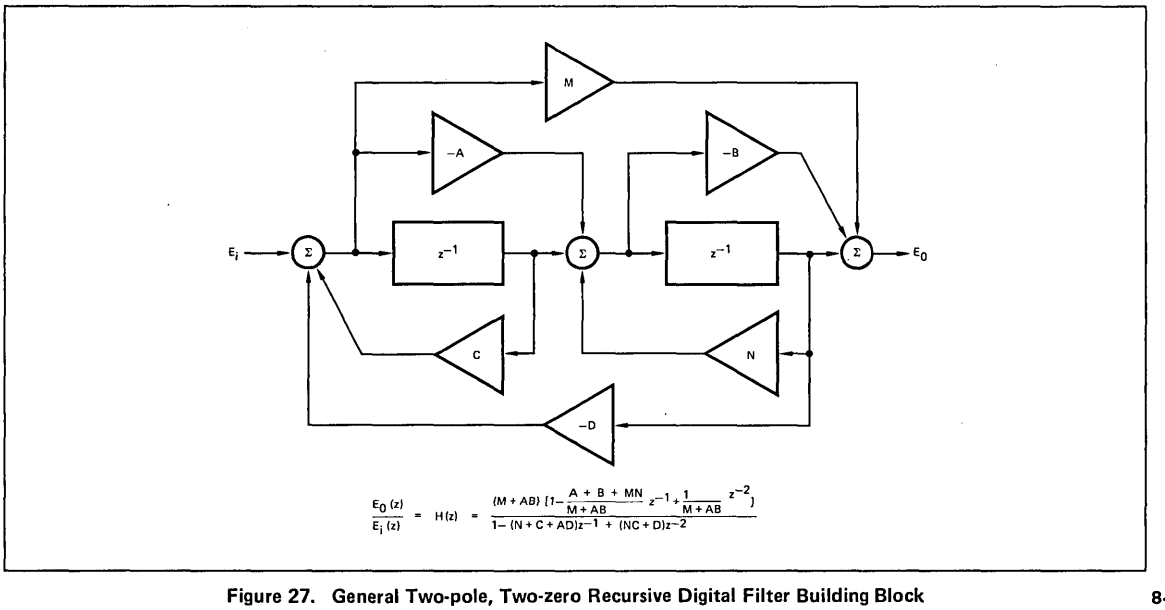
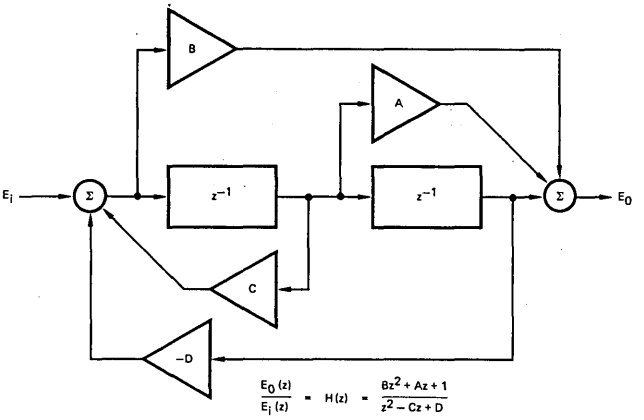


Figure 27. General Two-pole, Two-zero Recursive Digital Filter Building Block



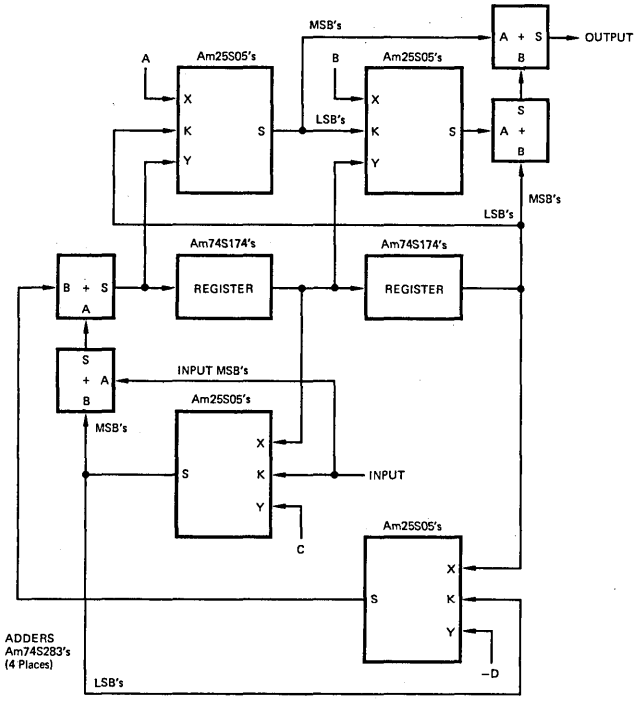


Figure 26. Canonical Two-pole, Two-zero Recursive Digital Filter.

A general two-pole building block is shown in Figure 27. There are several options for arranging the multipliers and adders depending on the application. The z-plane transfer function is also shown in Figure 27. The multiplier constants locate the poles and zeros of the filter. Also, the internal characteristics of the filter can be adjusted using the constants.

In all of the digital filter examples shown, the single unit delay register, z^{-1}, can be replaced with multi-word resisters. Thus, the arithmetic structure can be time shared by sequentially changing the multiplier constants. Also, such things as comb filters or range-gated filters can be designed using long word length registers. Remember, however, that each pole implemented requires one memory word and no sharing is possible.

A non-recursive digital filter is shown in Figure 28. These structures are useful as equalizers and for certain filter applications. These structures have a finite transient response whereas the recursive filter transient response tends to be infinite.

This same non-recursive structure can be implemented as shown in Figure 29. Here one multiplier and one register are used in a time-sequenced mode. Thus, with the non-recursive structure, both the multipliers and memory may be time shared. The coefficients A, B, C, etc., are evaluated by determining the transient response of the filter desired and implementing the z-transform constants as the multiplier constants. As shown, each constant is stored in a separate register and then multiplexed to the multiplier. This may be more convenient for adaptive filters. Otherwise, the constants can be stored in a shift register that is connected to the Y input of the multiplier.

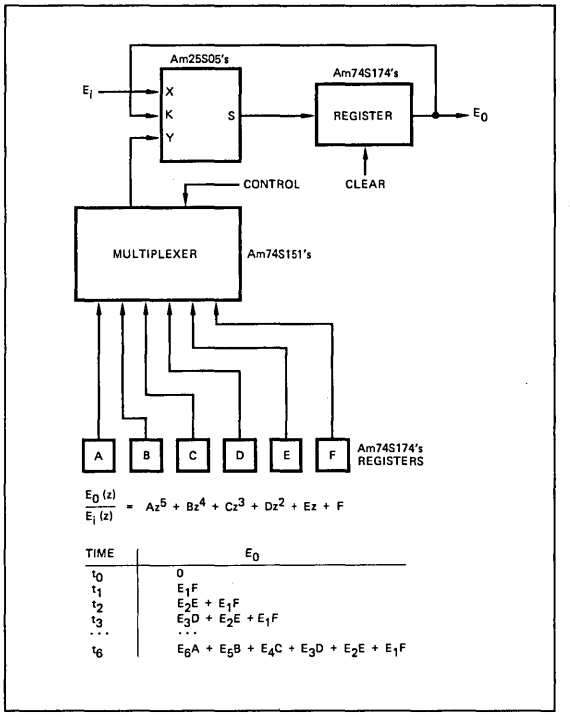


Figure 29. Time Sequenced Non-Recursive Digital Filter

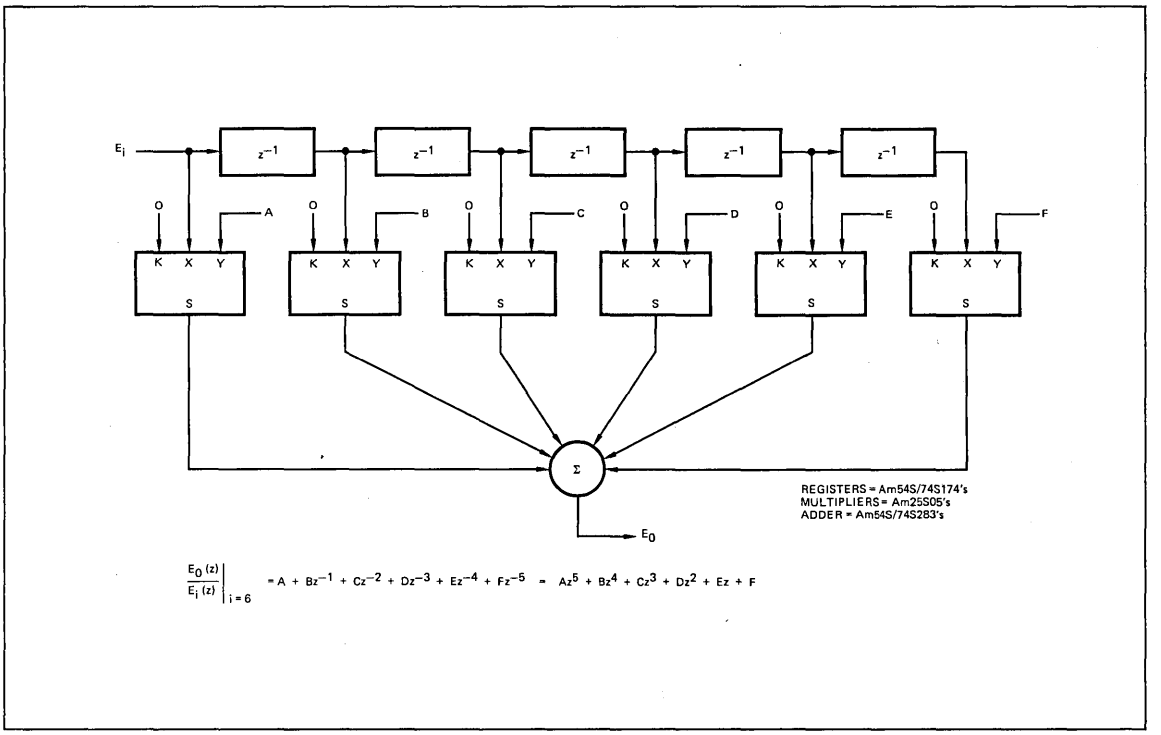


Figure 28. Non-recursive Digital Filter

Figure 30 shows how the square root of a number is formed using a multiplier array built with Am25S05 digital multipliers as the function generator. The successive approximation registers provide the estimate that is then squared and compared with the number whose root is required. If the square of the trial value is less than the number whose root is desired, then a "1" is fed back to change the register bit under consideration. The time to achieve a square root is essentially n+1 multiply times. The network can easily be modified to perform operations of the type $r = (X^2 + Y^2 + Z^2)^{1/2}$. The multiplier array can be used to generate the various squares, add the products and then compare the result against a trial value derived from the same multiplier array. The time required would then be n+4 multiplication times.

Another application frequently used is the division operation. This can be performed by multiplying the trial value, n, by the divisor and comparing the result against the dividend. If the dividend is larger then the trial value has to be increased; if the dividend is smaller then the trial value has to be reduced. The operation is fairly straightforward for unsigned division; with signed division a few problems occur.

For 2's complement integer division the logic is shown in Figure 31.

The divisor, dividend and trial quotient are all treated as 2's complement numbers. The first trial value is all ones (–1).

The operations performed are:

For Q_S, the sign digit of the quotient:

If $D_7 = 0$ and $-\frac{D}{2} < P$ Set $Q_S = 0$ Otherwise $Q_S = 1$

If $D_7 = 1$ and $-\frac{D}{2} < P$ Set $Q_S = 1$ Otherwise $Q_S = 0$

For the remaining quotient digits:

If $D_7 = 0$ and $T_{i-1}\, D + \frac{D}{2} < P$ Set $Q_i = 1$ Otherwise $Q_i = 0$

If $D_7 = 1$ and $T_{i-1}\, D + \frac{D}{2} < P$ Set $Q_i = 0$ Otherwise $Q_i = 1$

where T_i is the i th trial value held in the SAR.

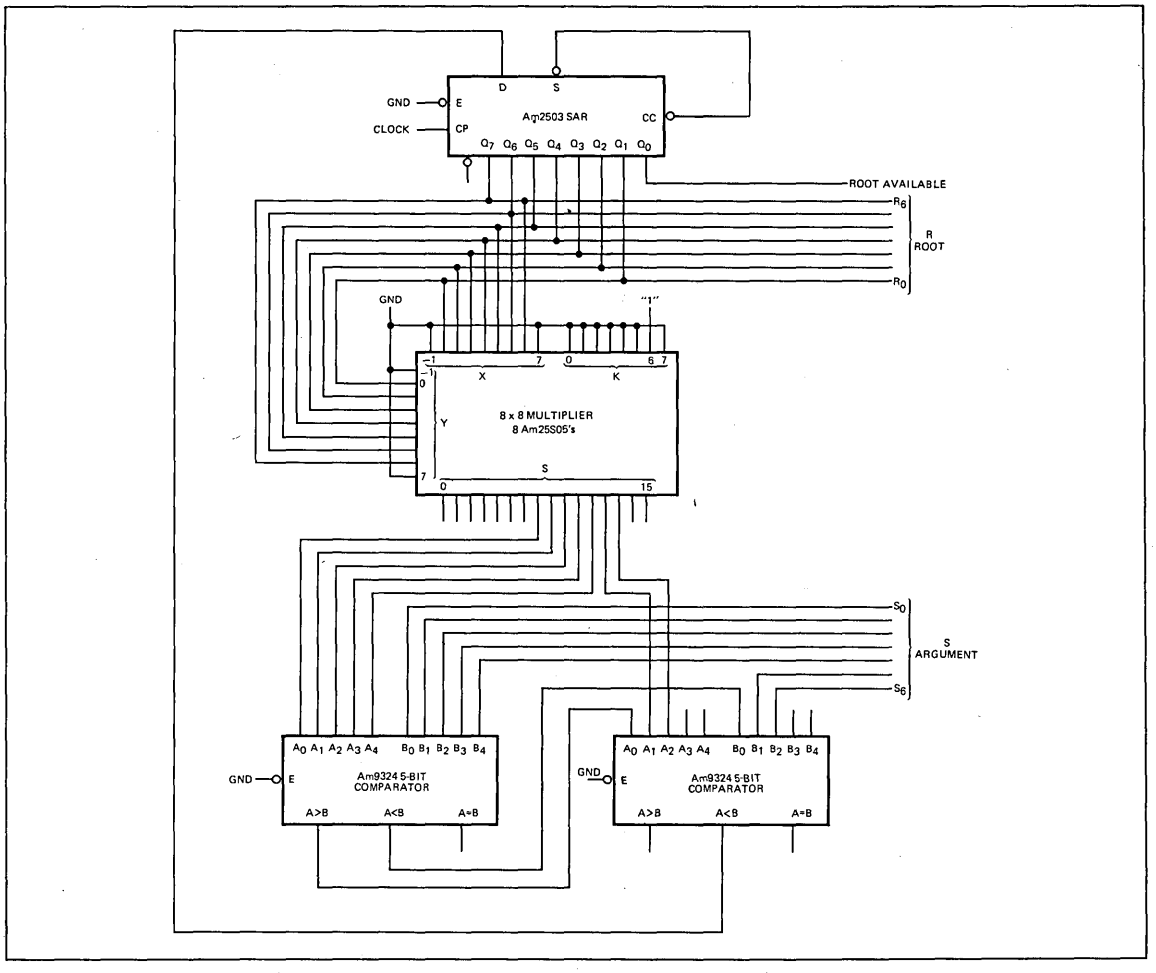


Figure 30. Square Root Evaluation by Recursion

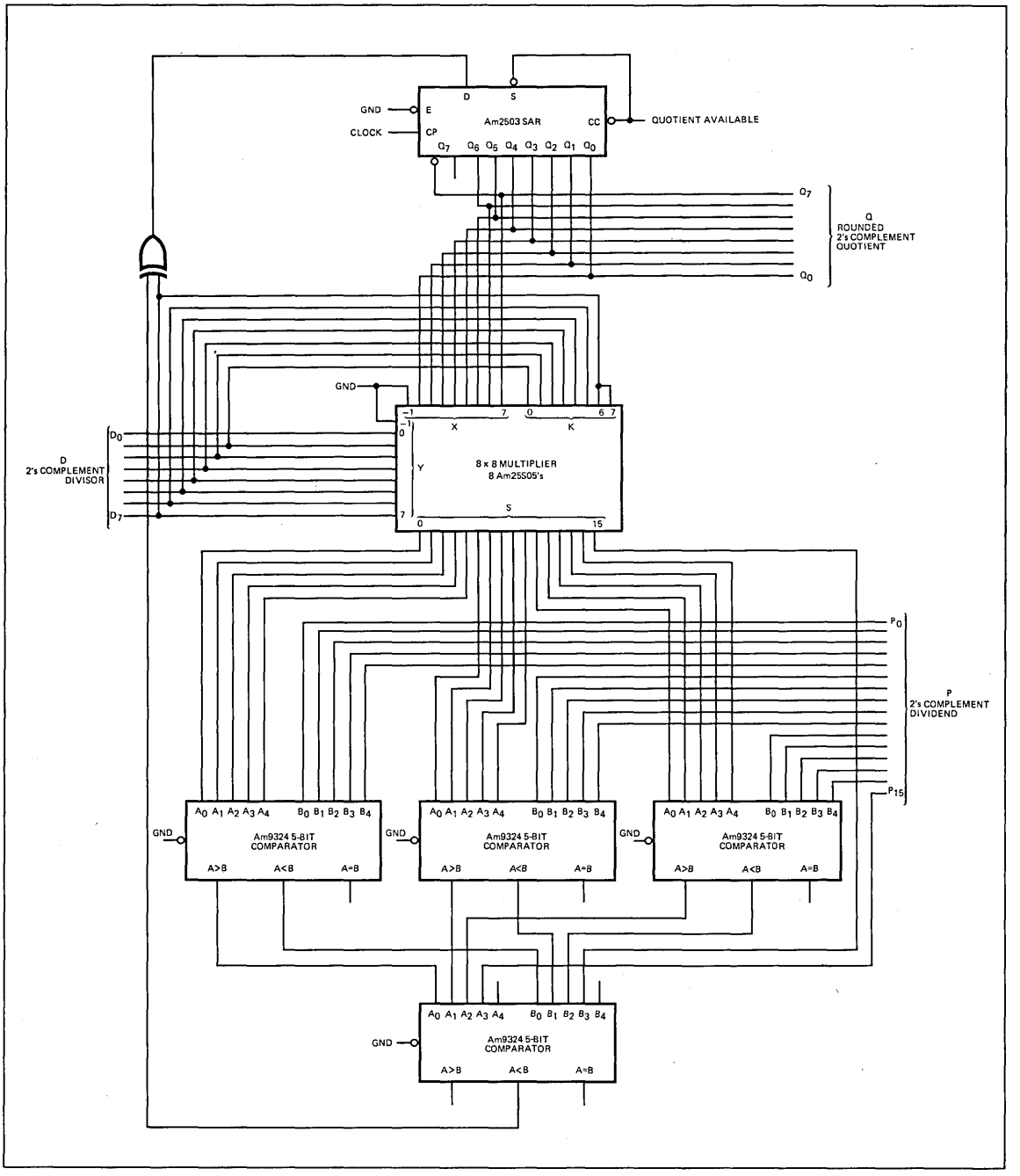


Figure 31. 2's Complement Rounded Division

Since the complement of the most significant bit of the register is used rather than the true output so that resetting the register presents −1 to the multiplier array, the change in algorithm between the sign bit and the rest of the bits is automatically taken care of.

The D/2 factor in the equations is used to round off the quotient. A double length dividend is assumed. The comparator is wired for a 2's complement comparison with the sign digit of the product and dividend crossed over, the dividend sign bit forming part of the multiplier word and the product sign bit forming part of the dividend word.

Am25S10 FOUR-BIT SHIFTER

By John R. Mick

INTRODUCTION

The Am25S10 is a high-speed MSI combinatorial logic block built using advanced Schottky technology. The device has the ability to shift four bits of data 0, 1, 2 or 3 places. The Am25S10 has two select lines that are decoded internally to determine the number of places the data is shifted. The device has seven data inputs I_{-3}, I_{-2}, I_{-1}, I_0, I_1, I_2, and I_3 and 4 three-state data outputs Y_0, Y_1, Y_2, and Y_3 as shown in the logic symbol diagram of Figure 1. The three-state outputs allow several devices to be bus organized for shifts of more than three places with a single level device propagation delay time. The three-state outputs are controlled by a single buffered active-LOW output control $\overline{OE}$. When the output control is LOW, the data outputs will follow the selected data inputs. When the output control is HIGH, the data outputs offer a high-impedance to the data bus.

FUNCTIONAL DESCRIPTION

The logic equations describing the output shifting capability of the Am25S10 when the output control is LOW are:

$$Y_0 = \overline{S}_0\ \overline{S}_1\ I_0 + S_0\ \overline{S}_1\ I_{-1} + \overline{S}_0\ S_1\ I_{-2} + S_0\ S_1\ I_{-3}$$

$$Y_1 = \overline{S}_0\ \overline{S}_1\ I_1 + S_0\ \overline{S}_1\ I_0 + \overline{S}_0\ S_1\ I_{-1} + S_0\ S_1\ I_{-2}$$

$$Y_2 = \overline{S}_0\ \overline{S}_1\ I_2 + S_0\ \overline{S}_1\ I_1 + \overline{S}_0\ S_1\ I_0 + S_0\ S_1\ I_{-1}$$

$$Y_3 = \overline{S}_0\ \overline{S}_1\ I_3 + S_0\ \overline{S}_1\ I_2 + \overline{S}_0\ S_1\ I_1 + S_0\ S_1\ I_0$$

From these equations it is seen that each output is operationally equivalent to a four-input multiplexer with the inputs connected such that the select code generates successive one-bit shifts of the input data word. The logic diagram of Figure 2 shows the internal connection of each multiplexer with respect to the seven data inputs. Because of this internal connection scheme, several devices can be connected to perform shifts of 0, 1, 2, or 3 places on words of any length.

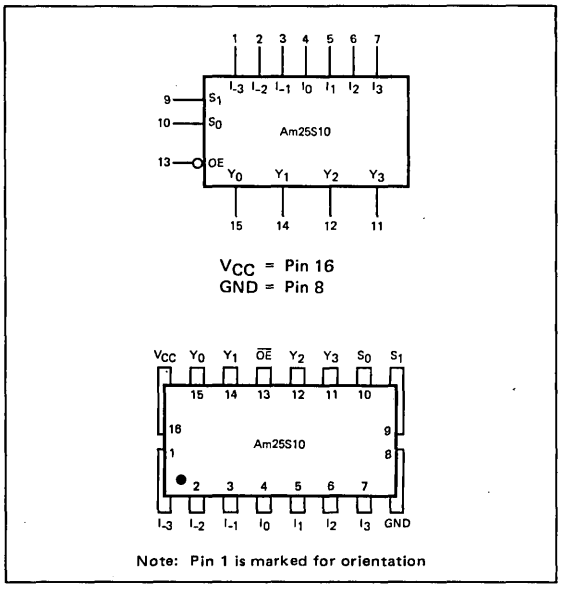


Figure 1. Logic Symbol and Connection Diagram.

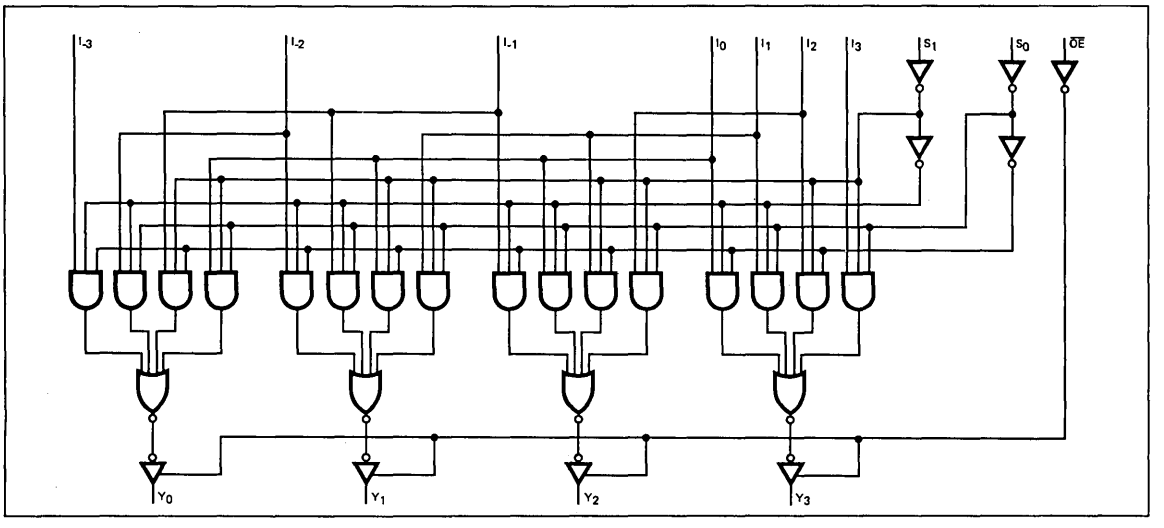


Figure 2. Logic Diagram of the Am25S10.

The operation of the Am25S10 is pictorially depicted in Figure 3. Here, the four shift positions of the data outputs with respect to the data inputs are shown via the dashed lines for the four possible select codes. Figure 4 shows a similiar operation only the notation now represents a seven-bit input word A_0 through A_6. The output code for each of the select field combinations applied to the S_0 and S_1 inputs is shown in the accompanying Function Table. In addition, the four outputs Y_0 through Y_3 can be forced to the high-impedance state by applying a HIGH to the "output control" input. This allows additional shifters to be cascaded on the same output lines, or the shifter array to be connected to a common data bus.

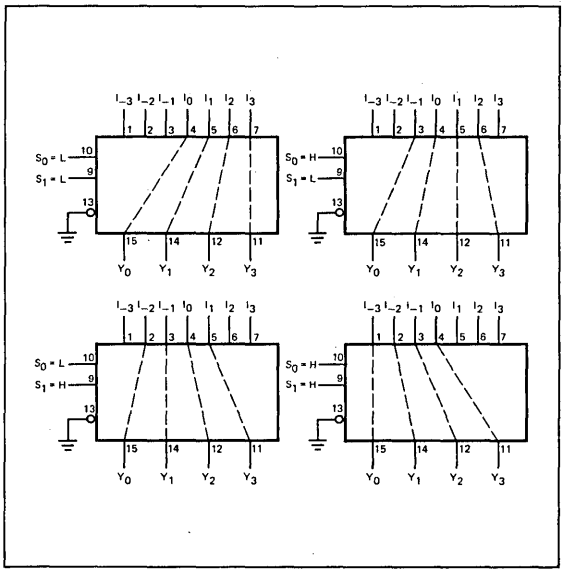
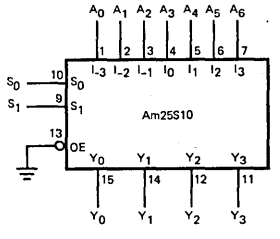


Figure 3. The Four Shift Positions of the Am25S10.



FUNCTION TABLE

S_1	S_0	Y_0	Y_1	Y_2	Y_3
0	0	A_3	A_4	A_5	A_6
0	1	A_2	A_3	A_4	A_5
1	0	A_1	A_2	A_3	A_4
1	1	A_0	A_1	A_2	A_3

Positive Logic

Figure 4. The Am25S10 4-Bit Shifter Operation.

INPUT LOADING

The logic diagram of Figure 2 shows the input connection scheme for the seven data inputs of the Am25S10. Table I shows the number of multiplexer inputs connected to each data input as well as the expected an actual Unit Load weighting on each input.

TABLE I .

Pin #	Data Input	Number of Multiplexer Inputs Connected	Expected Unit Loads	Actual Unit Loads
1	I_{-3}	1	1	1
2	I_{-2}	2	2	1.5
3	I_{-1}	3	3	1.5
4	I_0	4	4	1.5
5	I_1	3	3	1.5
6	I_2	2	2	1.5
7	I_3	1	1	1

Since the number of gate inputs for I_{-2}, I_{-1}, I_0, I_1 and I_2 data inputs is 2, 3, 4, 3, and 2 respectively, this could be expected to be the unit load fan-in for these data inputs. However, I_{IL} current sharing occurs internally with the select buffer outputs to reduce the external fan-in. Since a Schottky TTL unit load is defined as −2.0mA measured at 0.5V LOW, the maximum I_{IL} when measured at V_{IL} = 0.5V is −3mA or 1.5 STTL unit loads. As the measure voltage V_{IL} on these data inputs is decreased to 0V, the measured input current on I_{-2}, I_{-1}, I_0, I_1, and I_2 can increase to an I_{IL} maximum of −4, −6, −8, −6 and −4 mA respectively because of the decrease in current sharing with the internal select buffer outputs.

A plot of the typical input voltage versus input current for the data inputs is shown in Figure 5. This Figure shows the increased input current flow (negative current) as the input voltage is decreased. It also shows the effect of the input clamp diode as forward bias in applied.

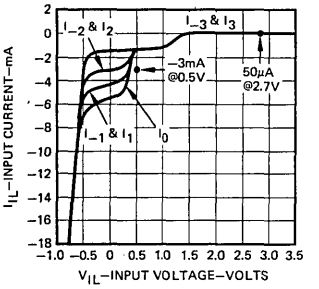
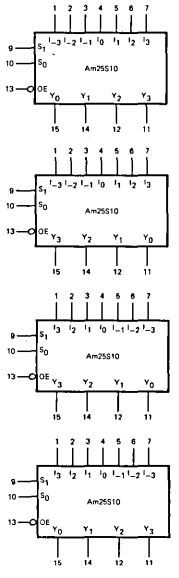


Figure 5. Typical Input Current Characteristics.

LOGIC EQUIVALENTS OF THE Am25S10

The Am25S10 exhibits several symmetrical properties that may be of advantage in some designs. These symmetrical properties involve the labeling of the inputs and outputs and the polarity of the select inputs. By relabeling the inputs in reverse order, labeling the outputs in reverse order, and considering the select inputs in positive logic (active-HIGH) or negative logic (active-LOW), eight logic equivalents for the device are possible. Figure 6 shows the operation of the device for the four combinations of input and output definitions for the positive logic notation while Figure 7 shows the operation of the device for the four combinations for the negative logic notation. The logic symbol for each set of definitions for the input pins and output pins is shown adjacent to the truth table.

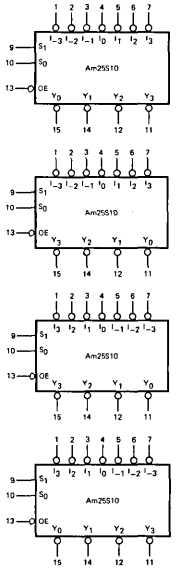
This relabeling of pins can provide the designer with some flexibility in printed circuit board layout. Likewise, the select code can be either positive logic or negative logic and the input data will be passed non-inverted. In some cases, the redefinition allows the designer to visualize shifting up versus shifting down for the same select code.



SELECT PINS		DATA INPUT PINS							DATA OUTPUT PINS			
9	10	1	2	3	4	5	6	7	11	12	14	15
S_1	S_0	I_{-3}	I_{-2}	I_{-1}	I_0	I_1	I_2	I_3	Y_3	Y_2	Y_1	Y_0
0	0	X	X	X	D_0	D_1	D_2	D_3	D_3	D_2	D_1	D_0
0	1	X	X	D_{-1}	D_0	D_1	D_2	X	D_2	D_1	D_0	D_{-1}
1	0	X	D_{-2}	D_{-1}	D_0	D_1	X	X	D_1	D_0	D_{-1}	D_{-2}
1	1	D_{-3}	D_{-2}	D_{-1}	D_0	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}
S_1	S_0	I_{-3}	I_{-2}	I_{-1}	I_0	I_1	I_2	I_3	Y_0	Y_1	Y_2	Y_3
0	0	X	X	X	D_0	D_1	D_2	D_3	D_3	D_2	D_1	D_0
0	1	X	X	D_{-1}	D_0	D_1	D_2	X	D_2	D_1	D_0	D_{-1}
1	0	X	D_{-2}	D_{-1}	D_0	D_1	X	X	D_1	D_0	D_{-1}	D_{-2}
1	1	D_{-3}	D_{-2}	D_{-1}	D_0	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}
S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_0	Y_1	Y_2	Y_3
0	0	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_{-3}	D_{-2}	D_{-1}	D_0
0	1	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_{-2}	D_{-1}	D_0	D_1
1	0	X	D_2	D_1	D_0	D_{-1}	X	X	D_{-1}	D_0	D_1	D_2
1	1	D_3	D_2	D_1	D_0	X	X	X	D_0	D_1	D_2	D_3
S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_3	Y_2	Y_1	Y_0
0	0	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_{-3}	D_{-2}	D_{-1}	D_0
0	1	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_{-2}	D_{-1}	D_0	D_1
1	0	X	D_2	D_1	D_0	D_{-1}	X	X	D_{-1}	D_0	D_1	D_2
1	1	D_3	D_2	D_1	D_0	X	X	X	D_0	D_1	D_2	D_3

Positive Logic (HIGH = 1, LOW = 0) for the select inputs.

Figure 6. Four Possible Input and Output Combinations for the Positive Logic Definition.



SELECT PINS		DATA INPUT PINS							DATA OUTPUT PINS			
9	10	1	2	3	4	5	6	7	11	12	14	15
S_1	S_0	I_{-3}	I_{-2}	I_{-1}	I_0	I_1	I_2	I_3	Y_3	Y_2	Y_1	Y_0
0	0	D_{-3}	D_{-2}	D_{-1}	D_0	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}
0	1	X	D_{-2}	D_{-1}	D_0	D_1	X	X	D_1	D_0	D_{-1}	D_{-2}
1	0	X	X	D_{-1}	D_0	D_1	D_2	X	D_2	D_1	D_0	D_{-1}
1	1	X	X	X	D_0	D_1	D_2	D_3	D_3	D_2	D_1	D_0
S_1	S_0	I_{-3}	I_{-2}	I_{-1}	I_0	I_1	I_2	I_3	Y_0	Y_1	Y_2	Y_3
0	0	D_{-3}	D_{-2}	D_{-1}	D_0	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}
0	1	X	D_{-2}	D_{-1}	D_0	D_1	X	X	D_1	D_0	D_{-1}	D_{-2}
1	0	X	X	D_{-1}	D_0	D_1	D_2	X	D_2	D_1	D_0	D_{-1}
1	1	X	X	X	D_0	D_1	D_2	D_3	D_3	D_2	D_1	D_0
S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_0	Y_1	Y_2	Y_3
0	0	D_3	D_2	D_1	D_0	X	X	X	D_0	D_1	D_2	D_3
0	1	X	D_2	D_1	D_0	D_{-1}	X	X	D_{-1}	D_0	D_1	D_2
1	0	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_{-2}	D_{-1}	D_0	D_1
1	1	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_{-3}	D_{-2}	D_{-1}	D_0
S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_3	Y_2	Y_1	Y_0
0	0	D_3	D_2	D_1	D_0	X	X	X	D_0	D_1	D_2	D_3
0	1	X	D_2	D_1	D_0	D_{-1}	X	X	D_{-1}	D_0	D_1	D_2
1	0	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_{-2}	D_{-1}	D_0	D_1
1	1	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_{-3}	D_{-2}	D_{-1}	D_0

Negative Logic (LOW = 1, HIGH = 0) for the select inputs.

Figure 7. Four Possible Input and Output Combinations for the Negative Logic Definition.

Am25S10 APPLICATIONS

The four-bit shifter is an ideal MSI element for high-speed shifting and scaling in digital systems. By suitable interconnection of the inputs and outputs, shifts of any number of places up or down can be made with a propagation delay of only one device. Shifting can be logical, with zeroes pulled in at either or both ends of the shifting field; arithmetic, where the sign bit is repeated during a shift down; or end around, where the data word forms a continuous loop. The three-state outputs can be used to increase the number of places shifted and also facilitate rapid data bus access in bus organized systems.

The Connection Diagram and Function Table of Figure 8 show a 16-bit word shifted up 0, 1, 2 or 3 places. In this example, the most significant bits (A_{13}, A_{14}, A_{15}) are discarded and logic zeroes are shifted in at the least significant end.

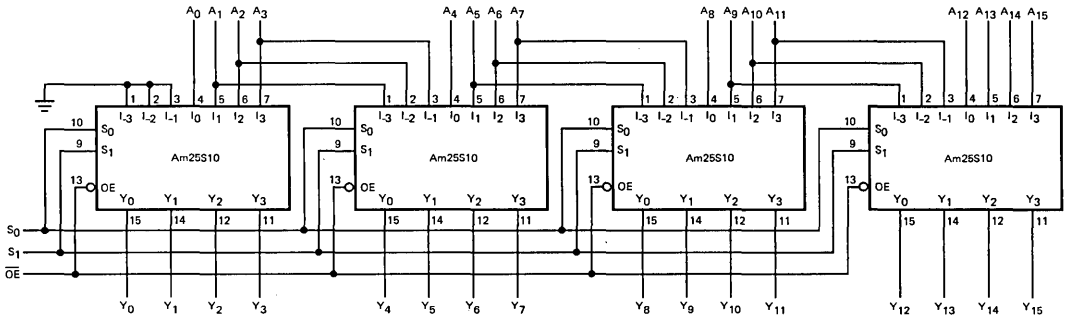
Figure 9 shows a Connection Diagram and Function Table for a 12-bit word shifted down 0, 1, 2 or 3 places. In this example, zeroes are shifted into the most significant bits and the least significant bits are discarded. Notice that one of the alternate definitions and pin assignments has been used to define the Am25S10.

A complete end-around barrel shift of 0, 1, 2, 3, 4, 5, 6 or 7 places is shown in Figure 10. In this configuration, the three-state capability of the outputs is used to connect one of two Am25S10's to the data output under the control of the S_2 and $\overline{S}_2$ select inputs. This technique can be expanded for longer word lengths by using one-of-four or one-of-eight decoders to control the active-LOW "output control" input.

A 13-bit two's complement scaler is shown in Figure 11. For this connection, the sign bit is pulled in at the most significant end and the least significant bits are truncated. Thus, the 13-bit two's complement binary output number is scaled to 1, 1/2, 1/4, or 1/8 of its input value.

A two-level 16-bit barrel shifter and its associated Function Table are shown in Figure 12. Only eight Am25S10's are required to perform this function. For clarity, the intermediate level of inputs and outputs have been labeled B_i. The sixteen-bit output word can be bus connected and controlled via the $\overline{OE}$ input.

Figure 13 demonstrates a unique way to convert a fixed point positive number to a floating-point mantissa and exponent. The priority encoder is used to determine the most significant bit position of the input word with a binary "1". The priority encoder output is a binary weighted code representing the number of places the input word is to be shifted up. This code controls the Am25S10 shifting array and shifts the input word such that the Y_7-bit of the mantissa is always a binary one (except for A = 0). The exponent is of the form 2^{-n} where n is the value of the binary weighted code from the priority encoder. Thus, the output of this functional block is of the form $Y2^{-n}$.

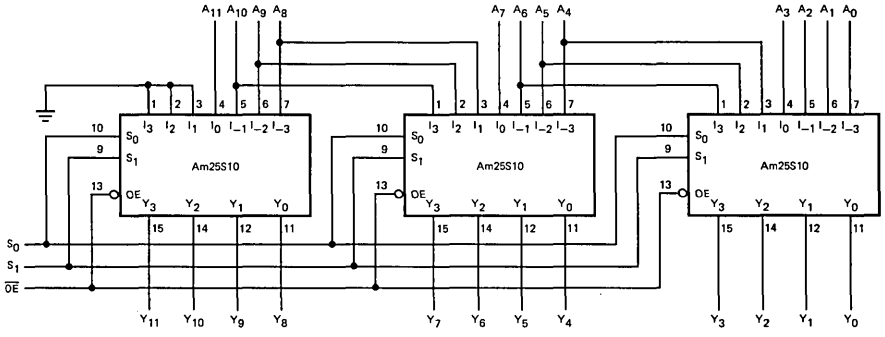


FUNCTION TABLE

S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9	Y_{10}	Y_{11}	Y_{12}	Y_{13}	Y_{14}	Y_{15}
0	0	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}
0	1	0	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}
1	0	0	0	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}
1	1	0	0	0	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}

Positive Logic

Figure 8. 16-Bit Shift-Up 0, 1, 2 or 3 Places.

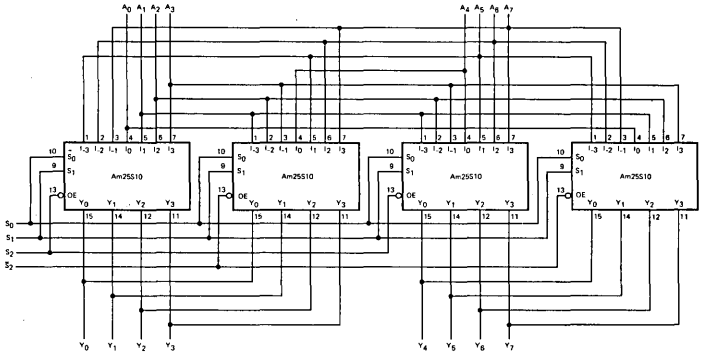


FUNCTION TABLE

S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9	Y_{10}	Y_{11}
0	0	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}
0	1	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	0
1	0	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	0	0
1	1	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	0	0	0

Positive Logic (Alternate Definitions)

Figure 9. 12-Bit Shift-Down 0, 1, 2 or 3 Places.

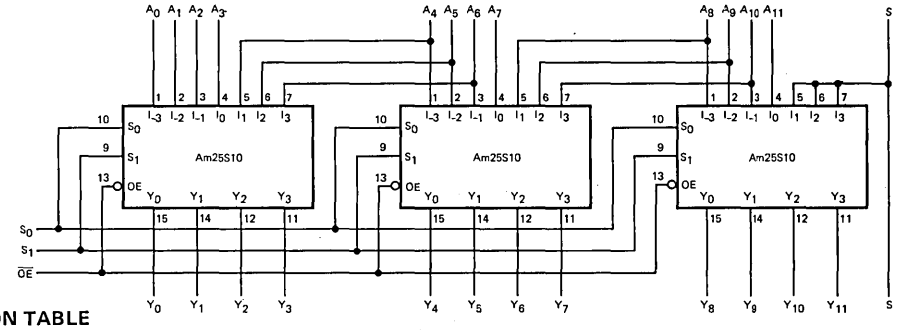


FUNCTION TABLE

S_2	S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
0	0	0	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7
0	0	1	A_7	A_0	A_1	A_2	A_3	A_4	A_5	A_6
0	1	0	A_6	A_7	A_0	A_1	A_2	A_3	A_4	A_5
0	1	1	A_5	A_6	A_7	A_0	A_1	A_2	A_3	A_4
1	0	0	A_4	A_5	A_6	A_7	A_0	A_1	A_2	A_3
1	0	1	A_3	A_4	A_5	A_6	A_7	A_0	A_1	A_2
1	1	0	A_2	A_3	A_4	A_5	A_6	A_7	A_0	A_1
1	1	1	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_0

Positive Logic

Figure 10. Eight-Bit End Around Shift 0, 1, 2, 3, 4, 5, 6 or 7 Places.

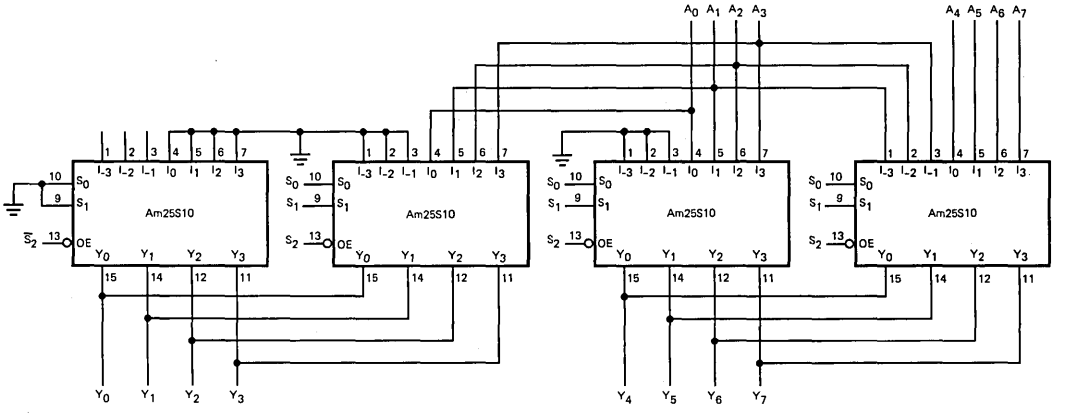


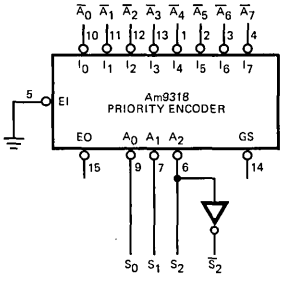
FUNCTION TABLE

SCALE	S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9	Y_{10}	Y_{11}	S
1/8	0	0	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	S	S	S	S
1/4	0	1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	S	S	S
1/2	1	0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	S	S
1	1	1	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	S

Positive Logic

Figure 11. 13-Bit 2's Complement Scaler.



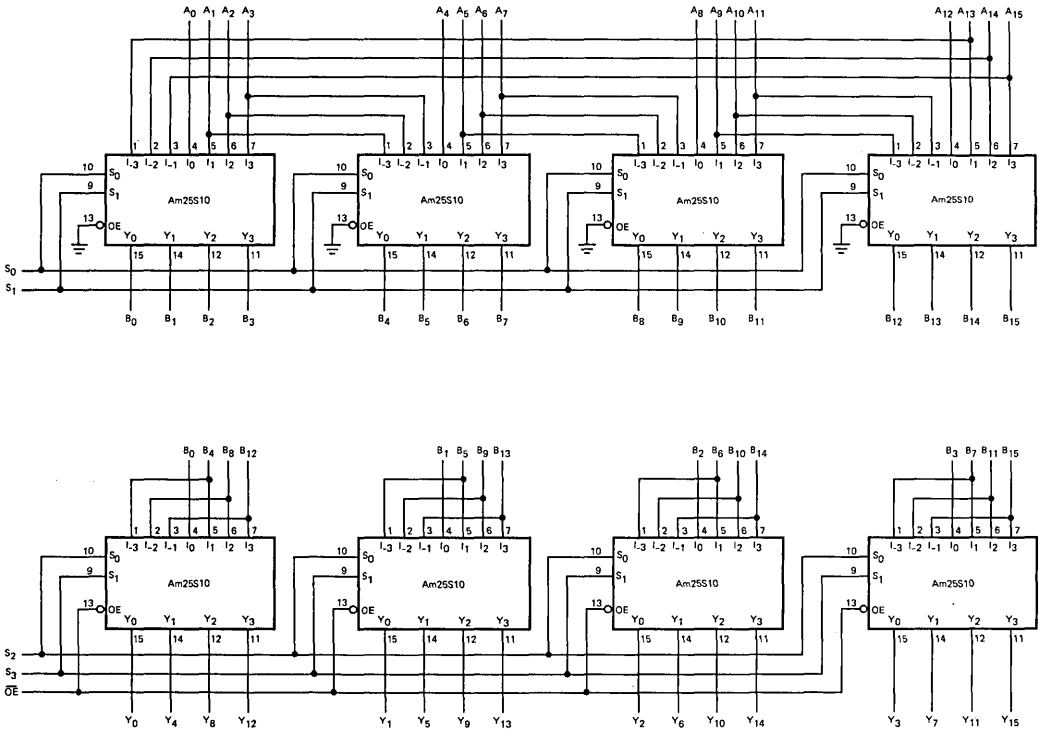


FUNCTION TABLE

EXPONENT			MANTISA							
S_2	S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
0	0	0	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7
0	0	1	0	A_0	A_1	A_2	A_3	A_4	A_5	A_6
0	1	0	0	0	A_0	A_1	A_2	A_3	A_4	A_5
0	1	1	0	0	0	A_0	A_1	A_2	A_3	A_4
1	0	0	0	0	0	0	A_0	A_1	A_2	A_3
1	0	1	0	0	0	0	0	A_0	A_1	A_2
1	1	0	0	0	0	0	0	0	A_0	A_1
1	1	1	0	0	0	0	0	0	0	A_0

Positive Logic

Figure 13. Binary Scaling to Give Mantisa and Exponent.



FUNCTION TABLE

S_3	S_2	S_1	S_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9	Y_{10}	Y_{11}	Y_{12}	Y_{13}	Y_{14}	Y_{15}
0	0	0	0	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}
0	0	0	1	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}
0	0	1	0	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}
0	0	1	1	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}
0	1	0	0	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}
0	1	0	1	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}
0	1	1	0	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9
0	1	1	1	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8
1	0	0	0	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7
1	0	0	1	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5	A_6
1	0	1	0	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4	A_5
1	0	1	1	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3	A_4
1	1	0	0	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2	A_3
1	1	0	1	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1	A_2
1	1	1	0	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0	A_1
1	1	1	1	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_0

Positive Logic

Figure 12. Full 16-Bit Barrel Shifter.

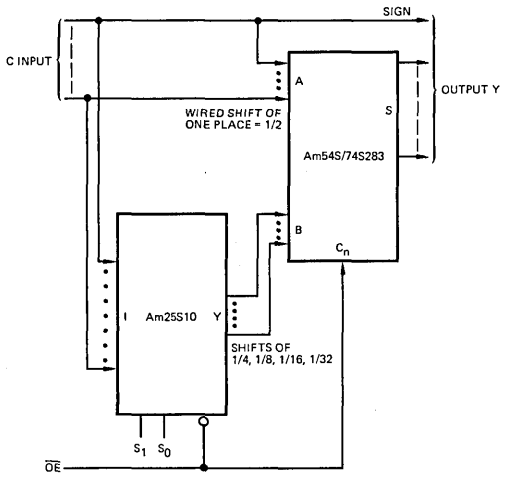
FIXED MULTIPLIERS

Digital systems requiring multiplication by a constant interger or constant fraction can make effective use of the Am25S10 if the constant must be varied over several values. By using four-bit shifters and high-speed adders, very high-speed "constant coefficient" or fixed multipliers can be built. The technique is shown diagrammatically in Figure 14. Here, the input word C is wired to the adder A inputs such that a shift of $\frac{1}{2}$ C is "built-in". The Am25S10 shifter is wired to the B inputs of the adder such that its four select states represent prescaling of $\frac{1}{4}$C, $\frac{1}{8}$C, $\frac{1}{16}$C, and $\frac{1}{32}$C of the C input word. If the $\overline{OE}$ input is used to disable the outputs (high impedance), the adder B inputs will assume the logical one state (HIGH). By adding a "one" at the adder carry input least significant end, the contribution of the B inputs to the sum output is zero and the adder A input will be passed to the output. Thus, the $\overline{OE}$ input can be used to generate a zero C value from the shifter.

Figure 15 shows the actual connection diagram for a 12-bit two's complement fixed multiplier using the scheme of Figure 14. The Y output weighting is the same as shown in the Function Table of Figure 14. The $\overline{OE}$ input is tied directly to the adder least significant C_n input to complete the shifter "zero" output function.

Figure 16 shows two shifter arrays used in conjunction with one adder. For the shifter A and shifter B select codes shown, twenty multiplication constants are realized with seventeen constants being unique. Other combinations could be used to realize different outputs. The combinations possible can be extended greatly by using multiple adders and multiple shifting arrays. For the example of Figure 16, the zero shifter output (high-impedance state) is used with only one shifter since only one C_n input is available.

This technique for fixed constant multipliers can be applied to two's complement, one's complement, sign-magnitude, or magnitude only arithmetic. In so doing, the sign must be handled appropriately and the adder output word size and number range must be considered. For the one's complement case, the all ones representation for zero must be handled separately.



FUNCTION TABLE

			4-BIT SHIFTER		A INPUT OF ADDER	OUTPUT Y
$\overline{OE}$	S_1	S_0	#SHIFTS	B INPUT OF ADDER		
0	0	0	Two	$\frac{1}{4}$C	$\frac{1}{2}$C	$\frac{3}{4}$C
0	0	1	Three	$\frac{1}{8}$C	$\frac{1}{2}$C	$\frac{5}{8}$C
0	1	0	Four	$\frac{1}{16}$C	$\frac{1}{2}$C	$\frac{9}{16}$C
0	1	1	Five	$\frac{1}{32}$C	$\frac{1}{2}$C	$\frac{17}{32}$C
1	X	X	Hi-Z	0C	$\frac{1}{2}$C	$\frac{1}{2}$C

Positive Logic

Figure 14. Parallel "Constant Coefficient" Multiplier Block Diagram and Function Table.

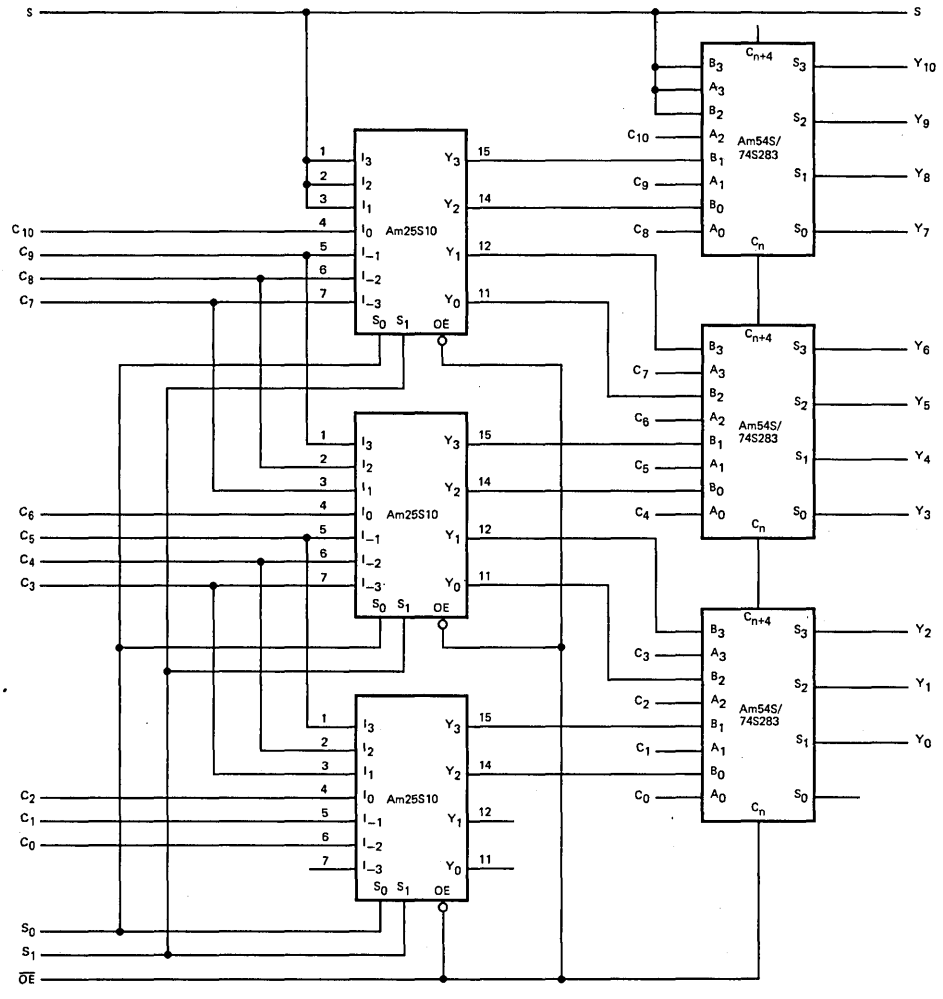
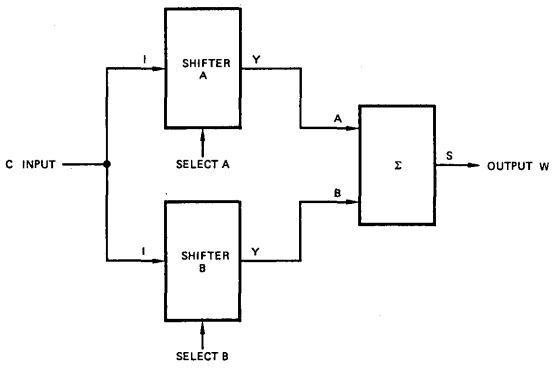


Figure 15. 12-Bit 2's Complement "Constant Coefficient" Multiplier.



SHIFTER A = $C, \frac{C}{2}, \frac{C}{4}, \frac{C}{8}$

SHIFTER B = $\frac{C}{4}, \frac{C}{8}, \frac{C}{16}, \frac{C}{32}, 0$

FIXED MULTIPLIER OUTPUT W

SHIFTER A \ SHIFTER B	$\frac{C}{4}$	$\frac{C}{8}$	$\frac{C}{16}$	$\frac{C}{32}$	0
C	$\frac{5}{4}C$	$\frac{9}{8}C$	$\frac{17}{16}C$	$\frac{33}{32}C$	C
$\frac{C}{2}$	$\frac{3}{4}C$	$\frac{5}{8}C$	$\frac{9}{16}C$	$\frac{17}{32}C$	$\frac{1}{2}C$
$\frac{C}{4}$	$\frac{1}{2}C$	$\frac{3}{8}C$	$\frac{5}{16}C$	$\frac{9}{32}C$	$\frac{1}{4}C$
$\frac{C}{8}$	$\frac{3}{8}C$	$\frac{1}{4}C$	$\frac{3}{16}C$	$\frac{5}{32}C$	$\frac{1}{8}C$

Figure 16. Two Shifter Arrays and One Adder Array in a Fixed Multiplier Connection.

CONCLUSION

The Am25S10 four-bit shifter is a new unique combinatorial logic element offering the system designer new shifting and scaling capability not previously available in a single package. The three-state output design of the Am25S10 provides increased flexibility in its use and the advanced Schottky construction offers minimum propagation delay. The device can be used to shift any number of bits any number of places; up, down or end-around.

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ORDERING AND PACKAGING INFORMATION

MSI CIRCUITS

Device Number	Order Number 0°C to +70°/75°C			Order Number −55°C to +125°C		
	Molded DIP	Hermetic DIP	Dice	Hermetic DIP	Flat Pack	Dice
Am25 Series						
Am2501	—	AM2501DC	AM2501XC	AM2501DM	—	AM2501XM
Am2502	AM2502PC	AM2502DC	AM2502XC	AM2502DM	AM2502FM	AM2502XM
Am2503	AM2503PC	AM2503DC	AM2503XC	AM2503DM	AM2503FM	AM2503XM
Am2504	AM2504PC	AM2504DC	AM2504XC	AM2504DM	AM2504FM	AM2504XM
Am2505	AM2505PC	AM2505DC	AM2505XC	AM2505DM	AM2505FM	AM2505XM
Am2506	AM2506PC	AM2506DC	AM2506XC	AM2506DM	AM2506FM	AM2506XM
Am25L Series						
Am25L02	AM25L02PC	AM25L02DC	AM25L02XC	AM25L02DM	AM25L02FM	AM25L02XM
Am25L03	AM25L03PC	AM25L03DC	AM25L03XC	AM25L03DM	AM25L03FM	AM25L03XM
Am25L04	AM25L04PC	AM25L04DC	AM25L04XC	AM25L04DM	AM25L04FM	AM25L04XM
Am25L05	AM25L05PC	AM25L05DC	AM25L05XC	AM25L05DM	AM25L05FM	AM25L05XM
Am25L06	AM25L06PC	AM25L06DC	AM25L06XC	AM25L06DM	AM25L06FM	AM25L06XM
Am54/74 Series						
Am54/74123	SN74123N	SN74123J	SN74123X	SN54123J	SN54123W	SN54123X
Am54/74153	SN74153N	SN74153J	SN74153X	SN54153J	SN54153W	SN54153X
Am54/74154	SN74154N	SN74154J	SN74154X	SN54154J	SN54154W	SN54154X
Am54/74157	SN74157N	SN74157J	SN74157X	SN54157J	SN54157W	SN54157X
Am54/74160	SN74160N	SN74160J	SN74160X	SN54160J	SN54160W	SN54160X
Am54/74161	SN74161N	SN74161J	SN74161X	SN54161J	SN54161W	SN54161X
Am54/74162	SN74162N	SN74162J	SN74162X	SN54162J	SN54162W	SN54162X
Am54/74163	SN74163N	SN74163J	SN74163X	SN54163J	SN54163W	SN54163X
Am54/74174	SN74174N	SN74174J	SN74174X	SN54174J	SN54174W	SN54174X
Am54/74175	SN74175N	SN74175J	SN74175X	SN54175J	SN54175W	SN54175X
Am54/74181	SN74181N	SN74181J	SN74181X	SN54181J	SN54181W	SN54181X
Am54/74182	SN74182N	SN74182J	SN74182X	SN54182J	SN54182W	SN54182X
Am54/74192	SN74192N	SN74192J	SN74192X	SN54192J	SN54192W	SN54192X
Am54/74193	SN74193N	SN74193J	SN74193X	SN54193J	SN54193W	SN54193X
Am54/74194	SN74194N	SN74194J	SN74194X	SN54194J	SN54194W	SN54194X
Am54/74195	SN74195N	SN74195J	SN74195X	SN54195J	SN54195W	SN54195X
Am54/74221	SN74221N	SN74221J	SN74221X	SN54221J	SN54221W	SN54221X
Am82 Series						
Am8284	N8284A	N8284F	N8284X	S8284F	—	S8284X
Am8285	N8285A	N8285F	N8285X	S8285F	—	S8285X
Am93 Series						
Am9300	9300PC	9300DC	9300XC	9300DM	9300FM	9300XM
Am9301	9301PC	9301DC	9301XC	9301DM	9301FM	9301XM
Am9304	9304PC	9304DC	9304XC	9304DM	9304FM	9304XM
Am9306	9306PC	9306DC	9306XC	9306DM	9306FM	9306XM
Am9308	9308PC	9308DC	9308XC	9308DM	9308FM	9308XM
Am9309	9309PC	9309DC	9309XC	9309DM	9309FM	9309XM
Am9310	9310PC	9310DC	9310XC	9310DM	9310FM	9310XM
Am9311	9311PC	9311DC	9311XC	9311DM	9311FM	9311XM
Am9312	9312PC	9312DC	9312XC	9312DM	9312FM	9312XM
Am9314	9314PC	9314DC	9314XC	9314DM	9314FM	9314XM
Am9316	9316PC	9316DC	9316XC	9316DM	9316FM	9316XM
Am9318	9318PC	9318DC	9318XC	9318DM	9318FM	9318XM
Am9321	9321PC	9321DC	9321XC	9321DM	9321FM	9321XM
Am9322	9322PC	9322DC	9322XC	9322DM	9322FM	9322XM
Am9324	9324PC	9324DC	9324XC	9324DM	9324FM	9324XM
Am9328	9328PC	9328DC	9328XC	9328DM	9328FM	9328XM
Am9334	9334PC	9334DC	9334XC	9334DM	9334FM	9334XM
Am9338	9338PC	9338DC	9338XC	9338DM	9338FM	9338XM
Am9340	9340PC	9340DC	9340XC	9340DM	9340FM	9340XM
Am9341	9341PC	9341DC	9341XC	9341DM	9341FM	9341XM
Am9342	9342PC	9342DC	9342XC	9342DM	9342FM	9342XM
Am9360	9360PC	9360DC	9360XC	9360DM	9360FM	9360XM
Am9366	9366PC	9366DC	9366XC	9366DM	9366FM	9366XM
Am93L Series						
Am93L00	93L00PC	93L00DC	93L00XC	93L00DM	93L00FM	93L00XM
Am93L01	93L01PC	93L01DC	93L01XC	93L01DM	93L01FM	93L01XM
Am93L08	93L08PC	93L08DC	93L08XC	93L08DM	93L08FM	93L08XM
Am93L09	93L09PC	93L09DC	93L09XC	93L09DM	93L09FM	93L09XM
Am93L10	93L10PC	93L10DC	93L10XC	93L10DM	93L10FM	93L10XM
Am93L11	93L11PC	93L11DC	93L11XC	93L11DM	93L11FM	93L11XM
Am93L12	93L12PC	93L12DC	93L12XC	93L12DM	93L12FM	93L12XM
Am93L14	93L14PC	93L14DC	93L14XC	93L14DM	93L14FM	93L14XM
Am93L16	93L16PC	93L16DC	93L16XC	93L16DM	93L16FM	93L16XM
Am93L18	93L18PC	93L18DC	93L18XC	93L18DM	93L18FM	93L18XM
Am93L21	93L21PC	93L21DC	93L21XC	93L21DM	93L21FM	93L21XM
Am93L22	93L22PC	93L22DC	93L22XC	93L22DM	93L22FM	93L22XM
Am93L24	93L24PC	93L24DC	93L24XC	93L24DM	93L24FM	93L24XM
Am93L28	93L28PC	93L28DC	93L28XC	93L28DM	93L28FM	93L28XM
Am93L34	93L34PC	93L34DC	93L34XC	93L34DM	93L34FM	93L34XM
Am93L38	93L38PC	93L38DC	93L38XC	93L38DM	93L38FM	93L38XM
Am93L40	93L40PC	93L40DC	93L40XC	93L40DM	93L40FM	93L40XM
Am93L41	93L41PC	93L41DC	93L41XC	93L41DM	93L41FM	93L41XM
Am93L60	93L60PC	93L60DC	93L60XC	93L60DM	93L60FM	93L60XM
Am93L66	93L66PC	93L66DC	93L66XC	93L66DM	93L66FM	93L66XM

SCHOTTKY MSI CIRCUITS

Device Number	Order Number 0°C to +70°/75°C			Order Number −55°C to +125°C		
	Molded DIP	Hermetic DIP	Dice	Hermetic DIP	Flat Pack	Dice
Am25S Series						
Am25S05	AM25S05PC	AM25S05DC	AM25S05XC	AM25S05DM	AM25S05FM	AM25S05XM
Am25S07	AM25S07PC	AM25S07DC	AM25S07XC	AM25S07DM	AM25S07FM	AM25S07XM
Am25S08	AM25S08PC	AM25S08DC	AM25S08XC	AM25S08DM	AM25S08FM	AM25S08XM
Am25S09	AM25S09PC	AM25S09DC	AM25S09XC	AM25S09DM	AM25S09FM	AM25S09XM
Am25S10	AM25S10PC	AM25S10DC	AM25S10XC	AM25S10DM	AM25S10FM	AM25S10XM
Am54S/74S Series						
Am54S/74S139	SN74S139N	SN74S139J	SN74S139X	SN54S139J	SN54S139W	SN54S139X
Am54S/74S151	SN74S151N	SN74S151J	SN74S151X	SN54S151J	SN54S151W	SN54S151X
Am54S/74S153	SN74S153N	SN74S153J	SN74S153X	SN54S153J	SN54S153W	SN54S153X
Am54S/74S157	SN74S157N	SN74S157J	SN74S157X	SN54S157J	SN54S157W	SN54S157X
Am54S/74S158	SN74S158N	SN74S158J	SN74S158X	SN54S158J	SN54S158W	SN54S158X
Am54S/74S174	SN74S174N	SN74S174J	SN74S174X	SN54S174J	SN54S174W	SN54S174X
Am54S/74S175	SN74S175N	SN74S175J	SN74S175X	SN54S175J	SN54S175W	SN54S175X
Am54S/74S181	SN74S181N	SN74S181J	SN74S181X	SN54S181J	SN54S181W	SN54S181X
Am54S/74S194	SN74S194N	SN74S194J	SN74S194X	SN54S194J	SN54S194W	SN54S194X
Am54S/74S195	SN74S195N	SN74S195J	SN74S195X	SN54S195J	SN54S195W	SN54S195X
Am54S/74S251	SN74S251N	SN74S251J	SN74S251X	SN54S251J	SN54S251W	SN54S251X
Am54S/74S253	SN74S253N	SN74S253J	SN74S253X	SN54S253J	SN54S253W	SN54S253X
Am54S/74S257	SN74S257N	SN74S257J	SN74S257X	SN54S257J	SN54S257W	SN54S257X
Am54S/74S258	SN74S258N	SN74S258J	SN74S258X	SN54S258J	SN54S258W	SN54S258X
Am82S/93S Series						
Am82S62	N82S62A	N82S62F	N82S62X	S82S62F	–	S82S62X
Am93S10	93S10PC	93S10DC	93S10XC	93S10DM	93S10FM	93S10XM
Am93S16	93S16PC	93S16DC	93S16XC	93S16DM	93S16FM	93S16XM
Am93S21	93S21PC	93S21DC	93S21XC	93S21DM	93S21FM	93S21XM
Am93S22	93S22PC	93S22DC	93S22XC	93S22DM	93S22FM	93S22XM
Am93S48	93S48PC	93S48DC	93S48XC	93S48DM	93S48FM	93S48XM

COMPUTER INTERFACE CIRCUITS

Device Number	Order Number 0°C to +70°/75°C			Order Number −55°C to +125°C		
	Molded DIP	Hermetic DIP	Dice	Hermetic DIP	Flat Pack	Dice
Am26 Series						
Am2600	AM2600PC	AM2600DC	AM2600XC	AM2600DM	AM2600FM	AM2600XM
Am2602	AM2602PC	AM2602DC	AM2602XC	AM2602DM	AM2602FM	AM2602XM
Am2614	AM2614PC	AM2614DC	AM2614XC	AM2614DM	AM2614FM	AM2614XM
Am2615	AM2615PC	AM2615DC	AM2615XC	AM2615DM	AM2615FM	AM2615XM
Am26123	AM26123PC	AM26123DC	AM26123XC	AM26123DM	AM26123FM	AM26123XM
Am26L02	AM26L02PC	AM26L02DC	AM26L02XC	AM26L02DM	AM26L02FM	AM26L02XM
Am26S02	AM26S02PC	AM26S02DC	AM26S02XC	AM26S02DM	AM26S02FM	AM26S02XM
Am26S12	AM26S12PC	AM26S12DC	AM26S12XC	AM26S12DM	AM26S12FM	AM26S12XM
Am26S12A	AM26S12APC	AM26S12ADC	AM26S12AXC	AM26S12ADM	AM26S12AFM	AM26S12AXM
Am78/88 Series						
Am78/8820	DM8820N	DM8820J	AM8820X	DM7820J	DM7820W	AM7820X
Am78/8820A	DM8820AN	DM8820AJ	AM8820AX	DM7820AJ	DM7820AW	AM7820AX
Am78/8830	DM8830N	DM8830J	AM8830X	DM7830J	DM7830W	AM7830X
Am78/8831	DM8831N	DM8831J	AM8831X	DM7831J	DM7831W	AM7831X
Am78/8832	DM8832N	DM8832J	AM8832X	DM7832J	DM7832W	AM7832X
Am55/75 Series						
Am55/75107B	SN75107BN	SN75107BJ	SN75107BX	SN55107BJ	SN55107BW	SN55107BX
Am55/75108B	SN75108BN	SN75108BJ	SN75108BX	SN55108BJ	SN55108BW	SN55108BX
Am55/75109	SN75109N	SN75109J	SN75109X	SN55109J	SN55109W	SN55109X
Am55/75110	SN75110N	SN75110J	SN75110X	SN55110J	SN55110W	SN55110X
Am75207	SN75207N	SN75207J	SN75207X	–	–	–
Am75208	SN75208N	SN75208J	SN75208X	–	–	–
Am96 Series						
Am9600	9600PC	9600DC	9600XC	9600DM	9600FM	9600XM
Am9601	9601PC	9601DC	9601XC	9601DM	9601FM	9601XM
Am9602	9602PC	9602DC	9602XC	9602DM	9602FM	9602XM
Am9614	9614PC	9614DC	9614XC	9614DM	9614FM	9614XM
Am9615	9615PC	9615DC	9615XC	9615DM	9615FM	9615XM
Am9616	–	9616DC	9616XC	–	–	–
Am9617	–	9617DC	9617XC	–	–	–
Am9620	9620PC	9620DC	9620XC	9620DM	9620FM	9620XM
Am9621	9621PC	9621DC	9621XC	9621DM	9621FM	9621XM
Am96L02	96L02PC	96L02DC	96L02XC	96L02DM	96L02FM	96L02XM
Other Devices						
Am1488	–	MC1488L	AM1488XC	–	–	–
Am1489	AM1489PC	MC1489L	AM1489XC	–	–	–
Am1489A	AM1489APC	MC1489AL	AM1489AXC	–	–	–
Am54/74123	SN74123N	SN74123J	SN74123X	SN54123J	SN54123W	SN54123X
Am54/74221	SN74221N	SN74221J	SN74221X	SN54221J	SN54221W	SN54221X
Am0026 (8 pin)	MH0026CN	MH0026CH*	AM0026CXC	MH0026H	–	AM0026XM
Am0026 (12 pin)	–	MH0026CG*	–	MH0026G	–	–
Am0026 (14 pin)	–	MMH0026CL	–	MMH0026L	–	–

*Metal Can

MOS CIRCUITS

Device Number	Order Number 0°C to +75°C				Order Number −55°C to +125°C	
	Molded Dip or Molded Mini-Dip	Hermetic Dip or Hermetic Mini-Dip	TO-5	Dice	Hermetic Dip or Hermetic Mini-Dip	TO-5
Am1002		MK1002P	MK1002L	AM1002XC		
Am1101A	P1101A	C1101A		AM1101XC	C1101ADM	
Am1101A1	P1101A1	C1101A1		AM1101A1XC	C1101A1DM	
Am1402A	AM1402APC	AM1402A		AM1402AXC	AM1402ADM	
Am1403A	AM1403APC		AM1403A	AM1403AXC		AM1403AHM
Am1404A	AM1404APC		AM1404A	AM1404AXC		AM1404AHM
Am1405A			AM1405A	AM1405AXC		AM1405AHM
Am1406				AM1406XC		AM1406HM
Am1407				AM1407XC		AM1407HM
Am1506			AM1506HC	AM1506XC		
Am1507			AM1507HC	AM1507XC		
Am2102	P2102	C2102		AM2102XC		
Am2102-1	P2102-1	C2102-1				
Am2102-2	P2102-2	C2102-2				
Am2505			AM2505K	AM2505XC		
Am2512			AM2512K	AM2512XC		
Am2521	AM2521V			AM2521XC		
Am2524	AM2524V			AM2524XC		
Am2525	AM2525V			AM2525XC		
Am2533	AM2533V			AM2533XC		
Am2802	AM2802PC	AM2802DC		AM2802XC	AM2802DM	
Am2803	AM2803PC		AM2803HC	AM2803XC		AM2803HM
Am2804	AM2804PC		AM2804HC	AM2804XC		AM2804HM
Am2805			AM2805HC	AM2805XC		AM2805HM
Am2806			AM2806HC	AM2806XC		AM2806HM
Am2807	AM2807PC			AM2807XC		
Am2808	AM2808PC			AM2808XC		
Am2809	AM2809PC		AM2809HC	AM2809XC		AM2809HM
Am2810		AM2810DC		AM2810XC	AM2810DM	
Am2812		AM2812DC		AM2812XC	AM2812DM	
Am2812A		AM2812ADC			AM2812ADM	
Am2813		AM2813DC		AM2813XC	AM2813DM	
Am2813A		AM2813ADC			AM2813ADM	
Am2814		AM2814DC		AM2814XC		
Am2833	AM2833PC	AM2833DC		AM2833XC	AM2833DM	
Am2841		AM2841DC		AM2841XC	AM2841DM	
Am3114	TMS3114NC	TMS3114JC		AM3114XC		
Am3341	AM3341PC	AM3341DC		AM3341XC	AM3341DM	
Am4055				AM4055XC	MM4055D	
Am4056				AM4056XC		MM4056H
Am4057				AM4057XC	MM4057D	
Am5055	MM5055N	MM5055D		AM5055XC		
Am5056			MM5056H	AM5056XC		
Am5057	MM5057N	MM5057D		AM5057XC		
Am9102	AM9102PC	AM9102DC			AM9102DM	
Am9102A	AM9102APC	AM9102ADC				
Am9102B	AM9102BPC	AM9102BDC				

BIPOLAR MEMORY CIRCUITS

Device Number	Order Number 0°C to +75°C			Order Number −55°C to +125°C		
	Molded Dip	Hermetic Dip	Dice	Hermetic Dip	Flat Pak	Dice
Am27LS00	AM27LS00PC	AM27LS00DC	AM27LS00XC	AM27LS00DM	AM27LS00FM	AM27LS00XM
Am27LS01	AM27LS01PC	AM27LS01DC	AM27LS01XC	AM27LS01DM	AM27LS01FM	AM27LS01XM
Am27S02	AM27S02PC	AM27S02DC	AM27S02XC	AM27S02DM	AM27S02FM	AM27S02XM
Am27S03	AM27S03PC	AM27S03DC	AM27S03XC	AM27S03DM	AM27S03FM	AM27S03XM
Am3101	P3101	C3101	AM3101XC	AM3101DM	AM3101FM	AM3101XM
Am31L01	AM31L01PC	AM31L01DC	AM31L01XC	AM31L01DM	AM31L01FM	AM31L01XM
Am3101A	P3101A	C3101A	AM3101AXC	AM3101ADM	AM3101AFM	AM3101AXM
Am5489				SN5489J	SN5489W	AM5489XM
Am7489	SN7489N	SN7489J	AM7489XC			
Am7599				DM7599J	DM7599W	AM7599XM
Am8599	DM8599N	DM8599J	AM8599XC			
Am93403	AM93403PC	AM93403DC	AM93403XC	AM93403DM	AM93403FM	AM93403XM

LINEAR CIRCUITS

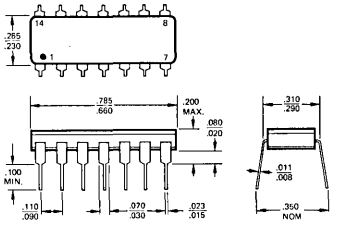
Device Number	Order Number 0°C to +70°C			Order Number −25°C to +85°C			Order Number −55°C to +125°C			
	TO-5	Hermetic DIP	Dice	TO-5	Hermetic DIP	Flat Pack	TO-5	Hermetic DIP	Flat Pack	Dice
Am685			AM685XL*	AM685HL	AM685DL		AM685HM	AM685DM		AM685XM
Am1500		AM1500DC			AM1500DL			AM1500DM	AM1500FM	
Am1501					AM1501DL			AM1501DM	AM1501FM	
Am1660	AM1660HC									
Am101	LM301		LMD01	LM201	LM201D	LM201F	LM101	LM101D	LM101F	LD101
Am101A	LM301A	LM301AD	LMD01A	LM201A	LM201AD	LM201AF	LM101A	LM101AD	LM101AF	LD101A
Am102	LM302		LMD02	LM202			LM102			LD102
Am105	LM305		LMD05	LM205		LM205F	LM105		LM105F	LD105
Am106	LM306		LMD06	LM206			LM106		LM106F	LD106
Am107	LM307	LM307D	LMD07	LM207	LM207D	LM207F	LM107	LM107D	LM107F	LD107
Am108	LM308	LM308D	LMD08	LM208	LM208D	LM208F	LM108	LM108D	LM108F	LD108
Am108A	LM308A	LM308AD	LMD08A	LM208A	LM208AD	LM208AF	LM108A	LM108AD	LM108AF	LD108A
Am110	LM310	LM310D	LMD10	LM210	LM210D		LM110	LM110D	LM110F	LD110
Am111	LM311	LM311D	LMD11	LM211	LM211D		LM111	LM111D	LM111F	LD111
Am112	LM312	LM312D	LMD12	LM212	LM212D		LM112	LM112D	LM112F	LD112
Am216	LM316	LM316D	LMD16	LM216	LM216D					LD216*
Am216A	LM316A	LM316AD	LMD16A	LM216A	LM216AD					LD216A*
Am118	LM318	LM318D	LMD18	LM218	LM218D		LM118	LM118D	LM118F	LD118
Am715	715HC	715DC	715XC				715HM	715DM		715XM
Am723	723HC	723DC	723XC				723HM	723DM		723XM
Am725	725HC	725DC	725XC	725HL			725HM	725DM		725XM
SSS725	SSS725EJ			SSS725BJ			SSS725AJ			
Am733	733HC	733DC	733XC				733HM	733DM	733FM	733XM
Am741	741HC	741DC	741XC				741HM	741DM	741FM	741XM
SSS741	SSS741CJ						SSS741J			
Am747	747HC	747DC	747XC				747HM	747DM	747FM	747XM
SSS747	SSS747CK	SSS747CP					SSS747K	SSS747P	SSS747M	
Am748	748DC	748HC	748XC				748DM	748HM	748FM	748XM

*Useage for −25° to +85°C

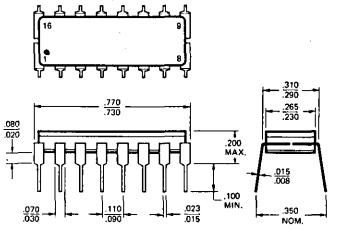
ADVANCED MICRO DEVICES, INC.
PACKAGE GUIDE

METAL HERMETIC

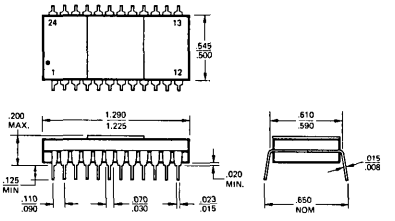
14-Lead Dual-In-Line



16-Lead Dual-In-Line

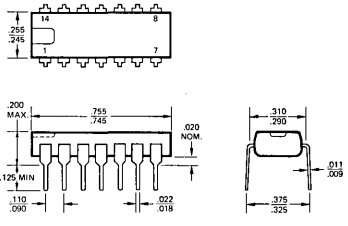


24-Lead Dual-In-Line

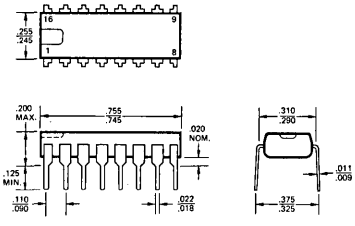


MOLDED

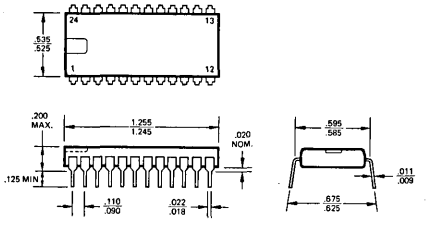
14-Lead Dual-In-Line



16-Lead Dual-In-Line



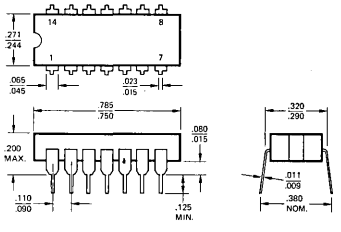
24-Lead Dual-In-Line



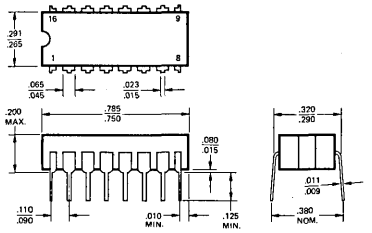
Note: All dimensions are in inches. Leads for 14 and 16-Pin Dual-In-Line packages are intended for insertion in hole rows on .300" centers and are misaligned to facilitate insertion. Leads for the 24-Pin Dual-In-Line packages are intended for insertion in hole rows on .600" centers and are misaligned to facilitate insertion.

CERAMIC HERMETIC

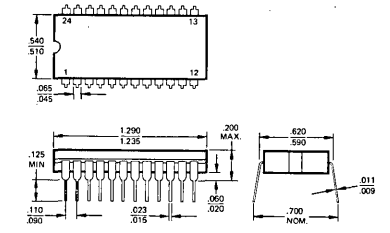
14-Lead Dual-In-Line



16-Lead Dual-In-Line



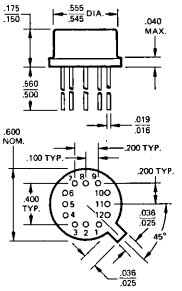
24-Lead Dual-In-Line

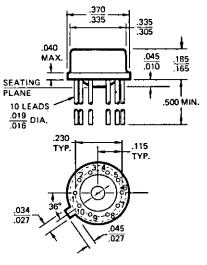


PACKAGE OUTLINES (CONT'D)

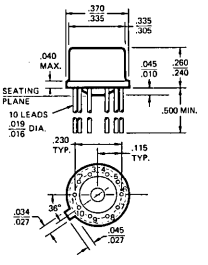
METAL CAN

TO-100

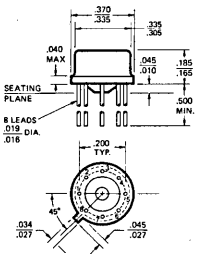




TO-100 HIGH

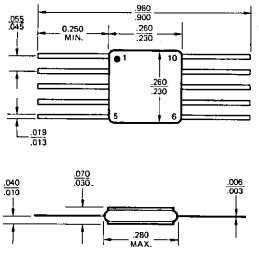


TO-99

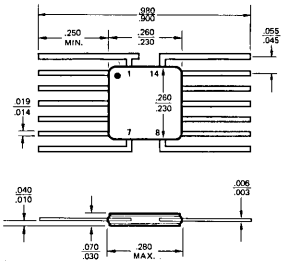


FLAT PACKAGE

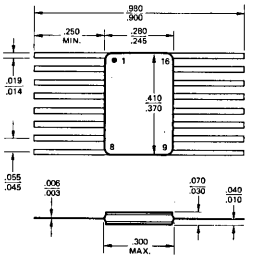
10-Lead Flat Package



14-Lead Flat Package



16-Lead Flat Package



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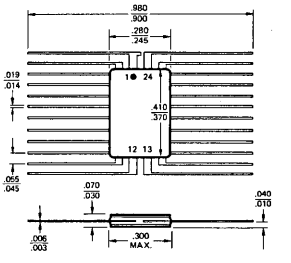

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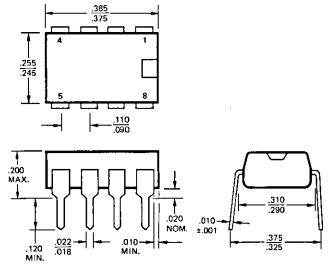

BRAZED

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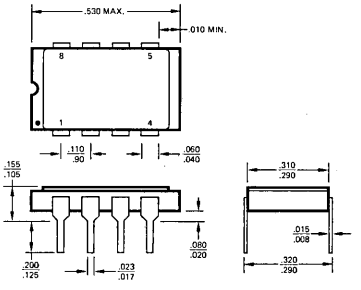

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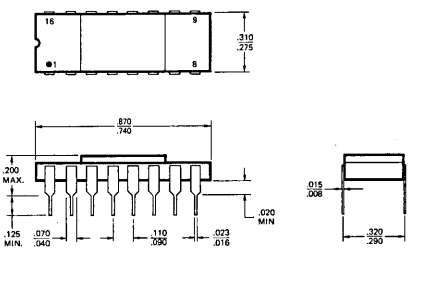

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- ☐ RF/IF & Video Amplifiers
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- ☐ Converters
- ☐ Other LIC
- ☐ Counters
- ☐ Registers
- ☐ Multiplexers & Demultiplexers
- ☐ Adders
- ☐ Interface
- ☐ Other DIC
- ☐ Memories
- ☐ MOS
- ☐ Other _____

Job Function
- ☐ General Engineering
- ☐ Design Engineer
- ☐ Component/Reliability/ Standards Engineering
- ☐ Purchasing & Material Mgt.
- ☐ General Management
- ☐ Marketing
- ☐ Magazine Editors
- ☐ Sales Reps
- ☐ Distributors
- ☐ Finance
- ☐ Other _____

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- ☐ Consumer
- ☐ Computer
- ☐ Computer Peripheral
- ☐ Instrumentation
- ☐ Aerospace and Defense
- ☐ Industrial
- ☐ Other _____

Product Interest
- ☐ Operational Amplifiers
- ☐ Sense Amplifiers & Comparators
- ☐ RF/IF & Video Amplifiers
- ☐ Voltage Regulators
- ☐ Converters
- ☐ Other LIC
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- ☐ Other _____

Schweber Electronics Distribution Locations

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Tel: (313) 583-9242

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Edina, Minnesota 55435
Tel: (612) 941-5280

NEW YORK
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Tel: (516) 334-7475

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Tel: (512) 837-2890

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The above locations of Schweber Electronics have been franchised for the distribution of the Advanced Micro Devices product line effective July 1, 1974.

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