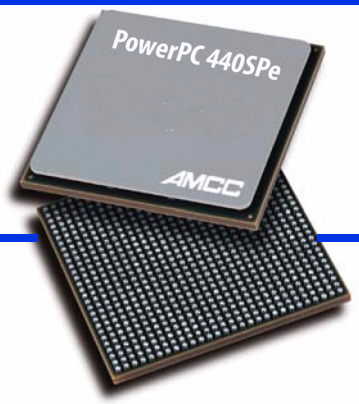


PowerPC 440SPe

Embedded Processor

With speeds of up to 667 MHz, the PowerPC 440SPe embedded processor offers a powerful mix of high bandwidth, design flexibility and robust features. With PCI Express and PCI-X interfaces, an on-chip DDR I/DDR II SDRAM controller, I2O messaging unit, RAID 5 and RAID 6 acceleration hardware, and a rich peripheral mix, the PowerPC 440SPe embedded processor is ideally suited for RAID controllers, storage area networking (SAN) equipment and other embedded storage and networking applications.

Benefits

- Delivers 533 MHz to 667 MHz performance for embedded I/O processor designs
- 32-Kbyte–I/32-Kbyte- D L1 caches
- 256-Kbyte L2 cache with parity protection, may also be used as on-chip SRAM
- High-speed processor local bus (PLB) with 2-way crossbar, supports 10.4-Gbytes/s peak bandwidth
- Three PCI Express interfaces
- PCI-X interface supports DDR operation
- Dual-ported 32/64-bit SDRAM memory controller, interfaced to both PLB slave segments, supporting 166/333 MHz DDR I and 333/667 MHz DDR II
- On-chip RAID 5 and RAID 6 acceleration hardware
- Integrated I2O messaging with two-channel DMA capability
- On-chip peripherals including 10/100/1000 Ethernet MAC, UARTs, IIC
- Offers low power dissipation and small form factor for high-density and power-conscious applications

The PowerPC 440 Core

To enhance overall throughput, the PowerPC 440 superscalar core incorporates a 7-stage pipeline and executes up to two instructions per cycle. Its large 32-Kbyte data cache and 32-Kbyte instruction cache are 64-way set-associative. For additional system performance, the PowerPC 440 core includes dynamic branch prediction and 24 digital signal processing (DSP) instructions, as well as non-blocking caches that can be managed in either write-through or write-back mode.

High-Bandwidth Bus Architecture

The PowerPC 440SPe CoreConnect 128-bit processor local bus (PLB) provides a two-way crossbar, with a separate 128-bit read and 128-bit write data bus for each way. The four 128-bit data buses may operate concurrently, providing up to 10.4 Gbytes/s of peak on-chip bandwidth at 166 MHz. The SDRAM is attached to two PLB slave ways to provide optimal access to memory from any other peripheral/core. Lower bandwidth I/O devices are supported by the on-chip peripheral bus (OPB).

High Performance Memory Support

The 440SPe incorporates a high-performance DDR memory controller supporting DDR I and DDR II memory devices. For DDR II operation, the memory interface can operate at an effective rate of DDR667, for a maximum bandwidth of 5.32 Gbytes/s. The interface can be configured for 64-bit or 32-bit memory implementations, with optional ECC. Industry standard DIMMS and discrete devices are supported for up to 16 Gbytes of memory. For greater efficiency, the memory controller provides parallel paths from each of the PLB slave segments and memory.

PCI Express and PCI-X Interfaces

The 440SPe offers three independent PCI Express interfaces compliant with PCI Express base specification 1.1. The primary interface has eight lanes and supports x8, x4, or x1 configurations. The two secondary interfaces have four lanes each and support x4 or x1 configurations. All three interfaces can be configured as root or end point ports.

In addition to the three PCI Express interfaces, the 440SPe includes one 64-bit PCI-X version 2.0 interface, which can operate at double data rate (DDR), latching data on both edges of the clock for an effective DDR266 throughput. The PCI-X interface offers a peak bandwidth of 2.13 Gbytes/s, is compatible with PCI-X v1.0a and PCI v2.3 specifications, and includes an internal arbiter. This interface may be configured in Host or Adapter mode.

The PCI Express and PCI-X interfaces can function as an opaque PCI bridge.

Ethernet Interface

A 10/100/1000-Mbytes/s Ethernet MAC (EMAC) provides a full-duplex GMII/MII interface with packet reject capability. In RAID controller applications this EMAC is intended to be used mainly as a management port.

RAID Hardware and I2O Accelerate Storage Applications

The 440SPe offers on-chip acceleration hardware for RAID 5 and RAID 6 parity generation and checking. This hardware, along with an internal high efficiency DMA engine, implements XOR and Galois Field P and Q operations at a high throughput rate.

I/O processing and other applications using multiple processors can benefit from the integrated messaging unit. Using I2O message frames, this messaging unit improves system performance by enabling the 440SPe to communicate with a host system on the host-side PCI Express bus. This enables the 440SPe to operate as an intelligent I/O adapter controller.

For increased performance, two DMA hardware controllers work with the RAID and I2O units to support memory-to-memory transfers.

Standard Peripherals

Two IIC controllers operate at 100/400 KHz. Both support master mode with multi-master and reset and target mode, and one supports serial boot ROM. The peripheral set also includes three UARTs, up to 32 general-purpose I/Os (GPIO) and general-purpose timers.

PowerPC 440SPe

PowerPC Partners Ecosystem

AMCC's embedded PowerPC processors are supported by an extensive ecosystem of products and services from a wide range of leading suppliers. AMCC's PowerPC Partners program includes industry-standard providers of:

- Embedded operating systems
- Hardware and software development tools
- Embedded software products and services
- Board-level products
- System design services
- Technical training

For full details of the products and services available through the PowerPC Partners program, or to browse support available for a specific processor, visit ***http://www.amcc.com/Embedded/Partners.***

AMCC also provides an evaluation kit for this PowerPC processor, including an optimized evaluation board as well as sample applications and other software.

Features

- Speed (frequency): 533 MHz to 667 MHz
- Performance: 2.0 DMIPS/MHz (1,334 DMIPS @ 667 MHz peak)
- 32-Kbyte–I/32-Kbyte D L1 caches, and 256-Kbyte L2/SRAM with parity protection
- 32/64-bit DDR I/DDR II SDRAM Controller, for DDR166/333 and DDR333/667 operation
- Three PCI Express interfaces, one with eight lanes configurable as x8, x4, x1 and two with four 4 lanes configurable as x4, x1; 2.5-Gbits/s full duplex per lane; compliant with PCI Express base specification 1.1; configurable as root or end point
- 64-bit PCI-X version 2.0 3.3v interface, up to 133 MHz / DDR266; 1.6-Gbytes/s sustained bandwidth, 2.13-Gbytes/s peak bandwidth; Support for PCI-X v1.0a up to 133 MHz and PCI v2.3, up to 66 MHz
- Opaque PCI Express to PCI Express, and PCI Express to PCI-X bridge functionality
- Ability to boot from the primary PCI-X bus memory
- RAID 5 and RAID 6 acceleration hardware for parity generation and check functions
- Intelligent messaging unit (I2O specification)
- Two-channel DMA included with I2O, one-channel DMA included with XOR
- External bus control (EBC) Interface (up to 83 MHz) supporting up to three ROM, RAM, or EPROM peripheral devices
- One 10/100/1000-Mbytes/s Ethernet MAC, full duplex GMII/MII interface with DMA capability by means of memory access layer (MAL)
- Three serial ports (16750-compliant UARTs) with 64-byte FIFOs
- Two IIC controllers
- Up to 32 general-purpose I/Os (GPIO)
- General-purpose timers
- Universal programmable interrupt controller supports 16 external interrupt sources and 101 internal sources
- Support for JTAG board testing, JTAG debuggers, and 4XX instruction trace interface

For more information, please visit ***http://www.amcc.com.***

Specifications

Technology

- 0.13-µm CMOS

Performance (estimated)

- 1,334 Dhrystone MIPS @ 667 MHz

Frequency

- CPU: 533 MHz to 667 MHz
- Memory:
  64-bit width: up to 5.3 Gbytes/s (DDR667)
  32-bit width: up to 1.3 Gbytes/s (DDR333)
- PCI Express:
  One 8-lane @ 2.5 Gbits/s per lane/direction
  Two 4-lane @ 2.5 Gbits/s per lane/direction
- PCI-X: 64-bit width @133 MHz, DDR266, 2.1-Gbytes/s peak throughput

Typical Power Dissipation

- < 10 W @ 533 MHz

Case Temperature Range

- 0° C to +95° C (case temperature)

Power Supply

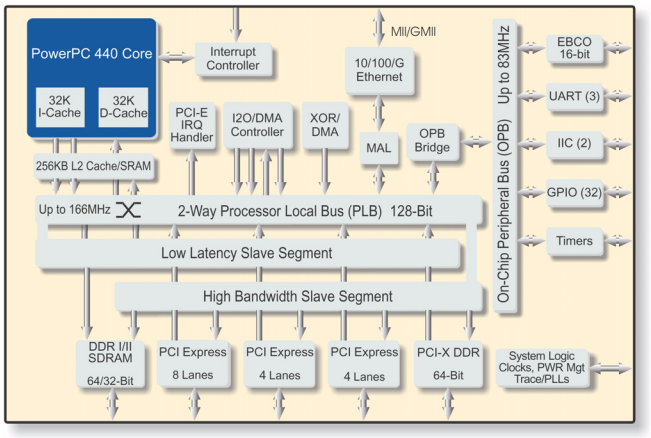
- 1.5 V (logic), 2.5 V/1.8 V (SDRAM), 3.3 V/1.5 V (PCI-X), 3.3 V (Ethernet, other I/O)

Signal I/Os

- 495

Packaging

- 675 FC-PBGA, 2 7mm x 27 mm with 1.0-mm pad pitch



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