405GP

Preliminary Application Note

Using a Spread Spectrum Clock Generator with the PowerPC® 405GP

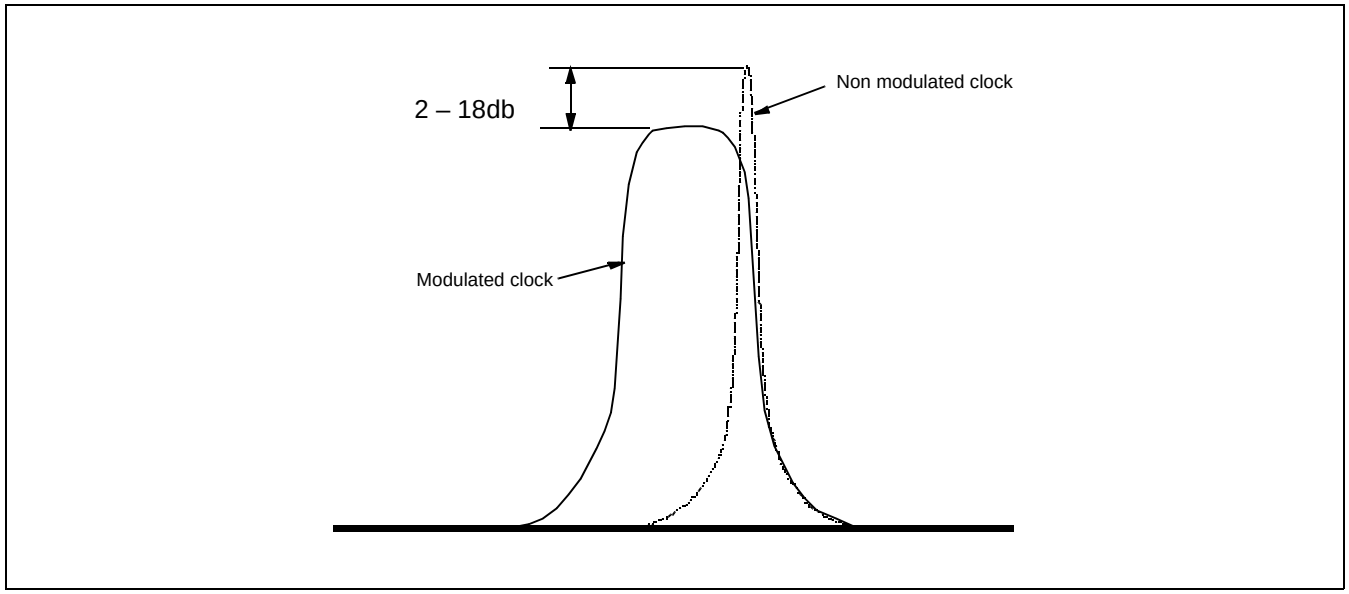
ABSTRACT

Products sold commercially must meet EMI radiated emissions limits regulated by the FCC in the US and similar agencies in Europe and the Far East. The clocks used in digital systems are one of the primary sources of unwanted electromagnetic interference. Energy spikes caused by clocks operating at a fixed frequency can be reduced by modulating the clock frequency. This technique is called spread spectrum clocking. This note describes the concept and the design considerations for the PowerPC 405GP processor and for the system.

OVERVIEW

The clocks used in digital systems are typically square waves with a 50% duty cycle, and as frequencies increase the edge rates are also getting faster and faster. Fourier analysis shows that a square wave is composed of the fundamental frequency and odd integer harmonics. The fundamental and the harmonics generate energy peaks that become the source of EMI. Typical clocks have a very high Q factor, which means that all of the energy at that frequency is concentrated in a very narrow bandwidth. Regulatory agencies test electronic equipment by measuring the amount of peak energy radiated from the equipment. In fact the peak level allowed decreases as the frequency increases. Standard methods of reducing EMI are to use shielding, filtering, multi-layer PCB's etc. Spread spectrum clocking reduces the peak energy by reducing the Q factor of the clock. This is done by slowly modulating the clock frequency. Figure 1 shows a conceptual view of the spectrum of the energy as viewed on a spectrum analyzer.

Figure 1. Clock energy spectrum



There are two types of SSCG (spread spectrum clock generators); center modulated and down modulated. Center modulated varies the frequency above and below a chosen center frequency and the down modulated only varies the frequency below the reference frequency. With center modulation, the average frequency is the same as the unmodulated frequency and there is no performance degradation. However, most processors are specified with a maximum frequency that cannot be exceeded so the modulation can only be used to decrease the clock frequency, down modulation. With down modulation, the average frequency is the unmodulated frequency minus 1/2 of the modulation range. For example, a 200 MHz processor with a 3% down spread would have an average frequency of 197MHz. For systems that operate with high cache hit ratios, performance may be reduced by the same –1.5%. An example of a specification requiring down spread only is the PCI specification. For 66 MHz operation the PCI specification specifies a down modulation only of -1% at 30-33KHz if a spread spectrum clock is used.

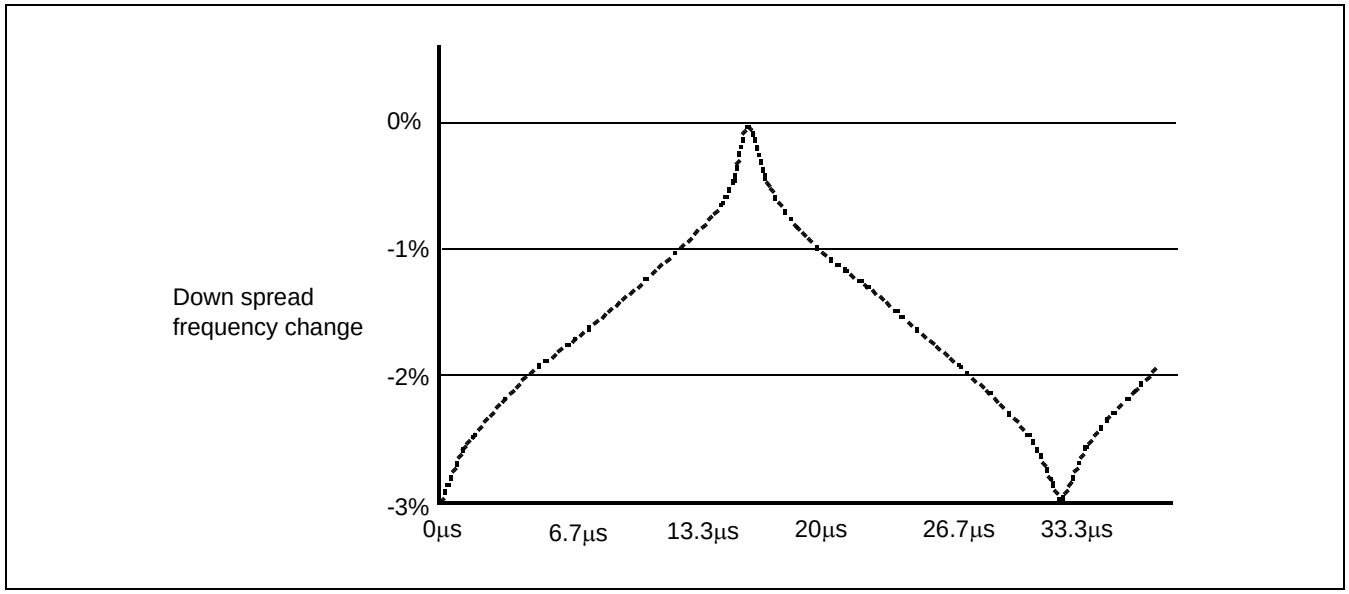
SYSTEM ISSUES

When designing with an SSCG, there are a number of design issues that must be taken into account. Many processors and systems are designed using PLLs. Care must be taken using SSCGs with microprocessors like the PPC405GP that use a PLL for clock generation inside the chip. When using a SSCG the strapping for the tune bits should be chosen as shown by the table below. Tune bit choices can also be set using CPC0_PLLMR[TUN]. The CPC0_PLLMR register is typically read only, however it can be enabled to allow writes. To allow writes to CPC0_PLLMR bit CPC0_CR0[0] must be set to a 1. It is important to avoid changing any other bits in the CPC0_PLLMR when updating the Tune bits. **Writing to the CPC0_PLLMR register causes an immediate chip reset to apply the changed values to the clocking logic. Obviously changing the CPC0_PLLMR register should be one of the first things done since any other peripheral initialization will be lost during the chip reset**. Now when the CPC0_PLLMR is read during initialization the tune bit value will be the one desired and the initialization code sequence can continue.

Function	Option	Ball Strapping		
PLL Tuning for Spread Spectrum for 6 ≤ M ≤ 7 use choice 2 for 7 < M ≤12 use choice 4 for 12 < M ≤ 32 use choice 7		AF3/U8	AF2/T8	AD16/AB15
	Choice 1; TUNE[5:0] = 010001	0	0	0
	Choice 2; TUNE[5:0] = 111011	0	0	1
	Choice 3; TUNE[5:0] = 010011	0	1	0
	Choice 4; TUNE[5:0] = 111101	0	1	1
	Choice 5; TUNE[5:0] = 010101	1	0	0
	Choice 6; TUNE[5:0] = 010110	1	0	1
	Choice 7; TUNE[5:0] = 111110	1	1	0
	Choice 8; TUNE[5:0] = 100100	1	1	1

The accuracy with which the PLL follows the SSCG is referred to as tracking skew. The PLL bandwidth and phase angle determine how much tracking skew there will be between the SSCG and the PLL for a given frequency deviation and modulation frequency. In addition, the optimum modulation profile is not linear. Work done by Lexmark[1] shows that a "Hershey Kiss™ "[2] profile yields the maximum reduction in peak energy. This modulation profile is shown in Figure 2.

Figure 2. Modulation profile



Analysis was done to show that, with a PLL bandwidth of 100x the modulation frequency and a phase angle << 0.1 degrees, tracking skew should be manageable. For the 405GP the tracking skew for up to a –3% variation in the SysClk frequency modulated at 30 kHz ranges from -77.5 to -185 ps depending on the VCO frequency. Tracking skew in pico seconds can be determined using the following formula.

skew = 37*sp*[1+((mod-30)/30)*.75]*[(m/(V))*42], where
skew = tracking skew in pico seconds Peak - Peak
sp = spread-spectrum frequency spread in %Peak - Peak (range = 1-5)
mod = spread-spectrum modulation frequency in KHz (range = 30-40)
m = total loop divider ratio (range = 6-32)
V=360, If VCO=400MHz,
V=319, If VCO=600MHz
V=303, If VCO=800MHz

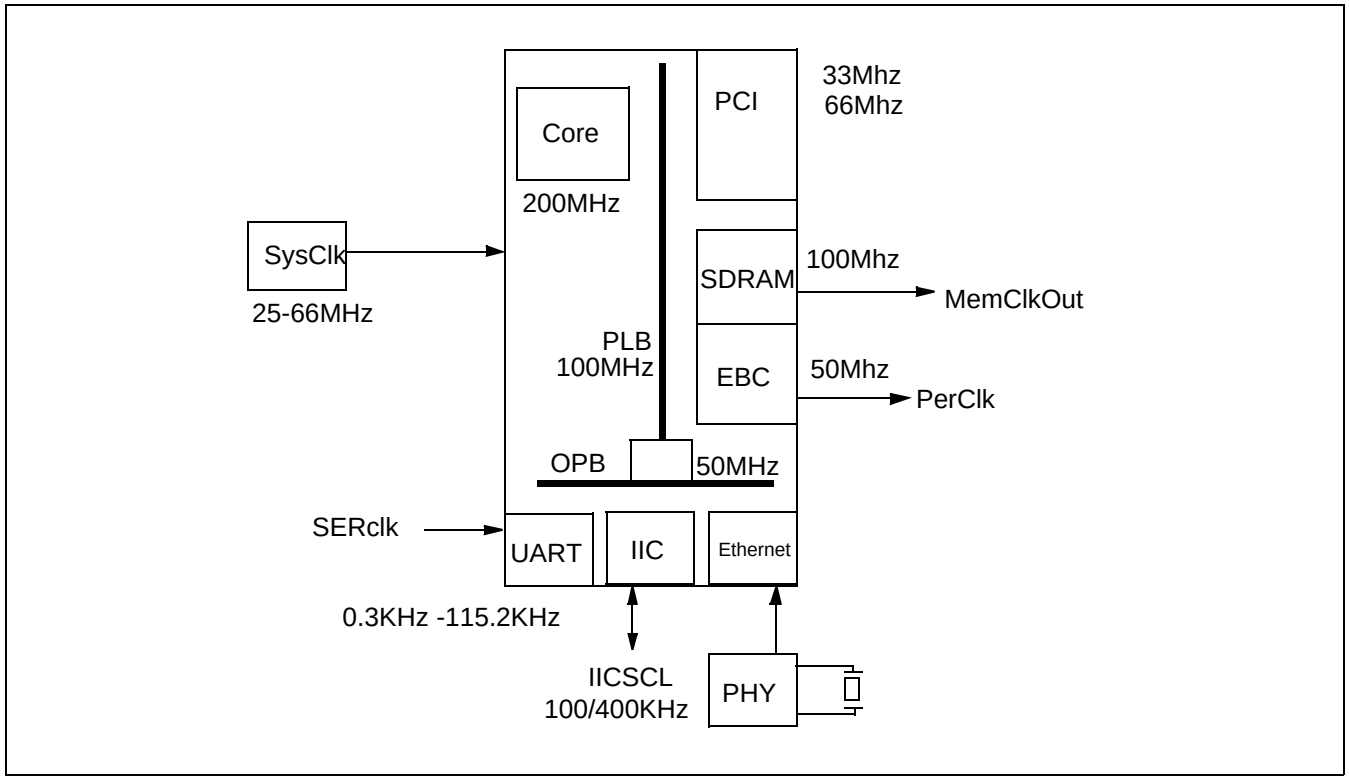
For example: for sp = 3, mod=30, m=24, V=303; then skew = 370ps Peak to Peak or ± 185ps. For a 3% down spread only the tracking skew would be –185ps.

Timing specifications for the processor and I/O interfaces has been specified with a jitter value specified in the data sheet. Tracking skew represents an additional amount of jitter that must be accounted for in the timing specs.

Once it has been determined that the processor is compatible with an SSCG, the system interfaces to the processor must be analyzed. For example, the 405GP is a highly integrated processor that has interfaces to PCI, Ethernet, SDRAM, UARTs, IIC, and a general purpose peripheral bus. Figure 3 shows a pictorial view of the different clock domains.

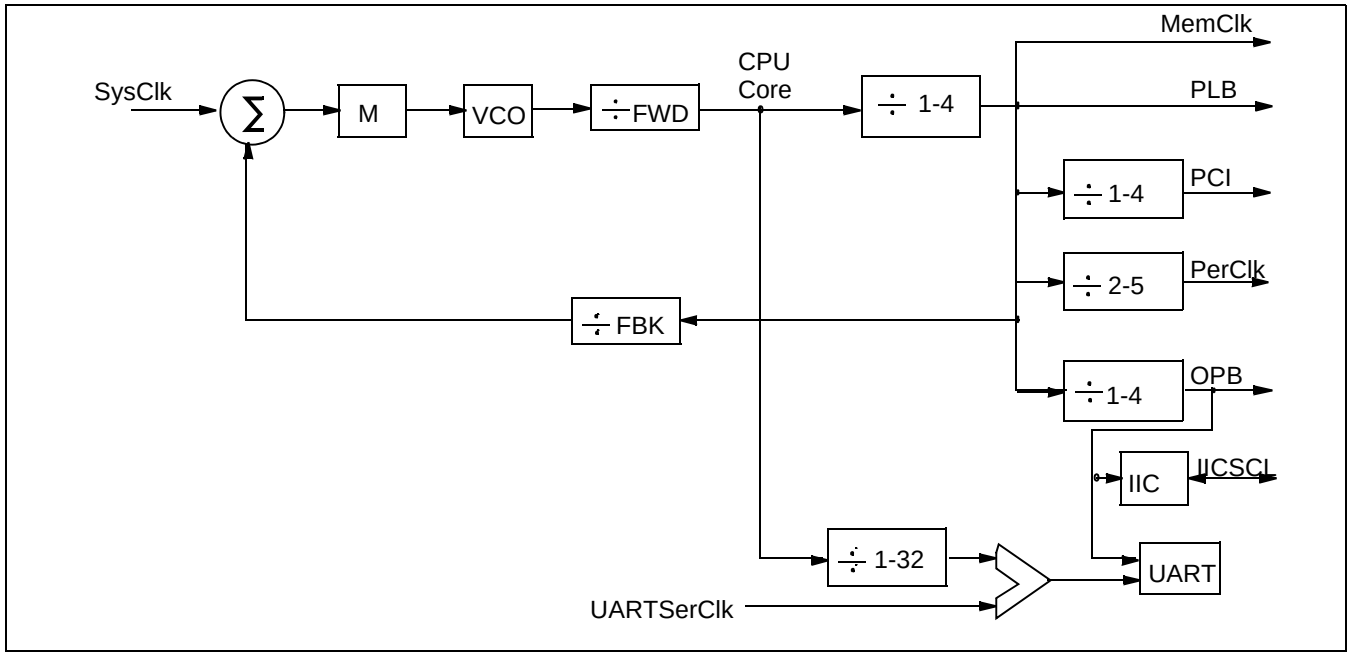
1.See US patent 5,631,920.
2.Hershey Kiss is a trademark of Hershey Foods Corp.

Figure 3. Clock domains



The clocking for the chip is derived from the input clock. Figure 4 is a simple representation of how the various clocks are derived from the system clock. The effect of using a SSCG must be examined for each interface.

Figure 4. Clock generation



PCI

The PCI Revision 2.2 specification addresses the use of Spread Spectrum Clocking. For synchronous 33 MHz systems the clock specifications of DC to 33.33MHz with dynamic variation of the clock allowed, would cover the use of SSCGs. For synchronous 66.66MHz systems the clocking specification limits the modulation to down spread only of –1% with a modulation frequency of 30-33KHz. The 405GP only supports synchronous mode only at 33MHz. If the 405GP is used in synchronous mode, either as a target or a master, the PCI clock from the host must be used as the input SysClk. In asynchronous PCI mode spread spectrum modulation has no effect.

PERIPHERAL BUS

The 405GP contains a general purpose bus interface that supports ROM/RAM/MMIO and an external bus master. System components that interface to this bus should use the PerClk output as the clock reference since it tracks the SSCG modulation. An alternative would be to use the same SSCG to drive SysClk and the logic attached to the peripheral bus, if they are the same frequency. If neither the SSCG or PerClk can be used, the timing analysis must be done over the range of spread chosen.

SDRAM BUS

The 405GP contains a PC100 compliant SDRAM controller. SDRAMs that interface to this bus should use the MemClkOutx outputs as the clock reference since it tracks the SSCG modulation. The SDRAM must be verified to work with a modulated clock.

ETHERNET

For the 405GP to attach to the ethernet link, an external PHY (physical link interface) is required. The clock that is used to drive the ethernet link is generated by the PHY. The connection of the 405GP to the PHY is fully asynchronous so the use of an SSCG has no impact.

UARTS

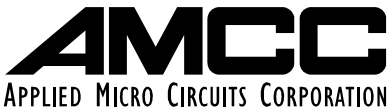
The serial port baud rates for the UARTs are generated from the core clock or from the UARTSerClk input. If the baud rate is generated using the internal clock and a SSCG is used for SysClk, the baud rate will be modulated. If UARTSerClk is used the baud rate will not be modulated. There is a requirement that UARTSerClk is less than 1/2 the OPB frequency as noted in the data sheet. This means that the calculation for UARTSerClk must account for the lowest frequency due to modulation. For systems using the internal clock to generate the baud rate the following caution applies. Most UARTs determine a bit value by multiple samples at some point near the mid baud time. If the stop bit is determined to be valid after 1/2 a baud time and the UART begins to look for a new start bit, the UART can tolerate a baud rate mismatch with a slightly faster baud rate. Since bit sampling is usually done at 1/2 the baud time a baud rate mismatch with a slightly slower baud rate is also tolerated. Baud rates that are generated from a clock that is an integer multiple of 1.3824MHz will yield baud rate errors that are essentially 0. However when typical system clocks are used some baud rate error is common. The serial port has a tolerance of approximately $\pm$ 1.5% on baud rate before framing errors begin to occur. Therefore, the SSCG could have a spread of –1.5% before framing errors would begin to occur. This spread range assumes that the connected device is running at a precise baud rate. The problems that may arise as a result of modulating the baud rate clock may be difficult to diagnose. Framing errors are cumulative in that the longer the bit stream (number of consecutive characters) the more likely a framing error will occur, due to a baud rate mismatch. Framing errors may appear intermittently due to variations in bit stream length and how the baud rate beats with the modulation frequency. Careful analysis and testing must be done.

IIC

The 405GP inter-integrated circuit bus supports master and slave operation. It also supports standard and fast clocking speeds of 100KHz and 400KHz. The clock for the IIC is derived from the OPB clock, which is modulated if a SSCG is used for SysClk. The IIC clocking specification states that the clock can vary between 0 and 100/400KHz. The specification, therefore, includes the spread range.

CONCLUSION

More information about Spread Spectrum Clock Generators can be found at the web sites of SSCG vendors such as Cypress Semiconductor Corporation. It is the responsibility of the system designer to ensure that the spread spectrum clock generator meets the above requirements and does not adversely affect other aspects of the system.



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