405GP

Preliminary Application Note

Migrating to the PowerPC® 405GPr from the PowerPC 405GP

SCOPE

The PowerPC 405GPr is a technology migration of the PowerPC 405GP offering a higher CPU clock rate, a larger data cache, and lower power dissipation in a footprint compatible package. This application note compares the 405GPr to the 405GP, and provides system designers with details for migrating 405GP-based applications to the 405GPr.

The 405GPr offers 405GP users the opportunity to realize increased system performance and lower power consumption with a minimum of circuit board modifications and minor software changes. To support usage with existing board layouts, the 405GPr is pin-compatible to the 405GP, with the exception of using a +1.8V supply for the internal logic instead of +2.5V. Although the 405GPr requires a reduced logic supply, all I/O voltage levels are identical to those supported by the 405GP. Furthermore, most of the 405GPr I/O timing specifications are equivalent to or better than those for the 405GP.

In terms of software, the only significant programming difference in porting an application from the 405GP to the 405GPr involves code that directly manipulates the data cache. Operating system routines and low-level applications that perform tasks such as cache flushing or invalidation need to account for the larger 16 KB data cache size. Other 405GPr differences that may affect existing software include new values for the Processor Version Register (PVR) and the JTAG ID Register (CPC0_JTAGID). While the 405GPr provides a minimal-change upgrade path for existing systems, new designs can benefit from its expanded capabilities. Not only does the 405GPr support non-integer ratios between the CPU and SDRAM clock frequencies, but it allows any six of the existing GPIOs to be used as additional external interrupt sources, and includes one more General Purpose I/O (GPIO). For complete and detailed information on the 405GPr, please refer to the *PowerPC 405GPr Embedded Processor User's Manual* and the *PowerPC 405GPr Embedded Processor Data Sheet.*

Introducing the 405GPr

The 405GPr is essentially a pin-compatible migration of the 405GP to 0.18µm technology. However, the 405GPr is more than simply a technology shrink. As shown in Table 2, the 405GPr extends CPU performance to 400 MHz, while non-integral CPU to SDRAM clock ratio support serves to maximize memory performance. CPU throughput was further enhanced by doubling the data cache size to 16 KB, while six additional external interrupts, each of which may be sourced from any of the 24 GPIOs, provide system architects with additional integration and design flexibility. Even with all of these improvements, at any given CPU frequency the 405GPr dissipates approximately half the power of a 405GP.

Table 1. Comparison of 405GP to 405GPr

Feature	405GP	405GPr
Technology	0.25µm (0.18µm Leff) CMOS SA-12E	0.18µm (0.11µm Leff) CMOS SA-27E
CPU Speed	200 & 266 MHz	266, 333, 400 MHz
SDRAM Clock Rate	100 & 133 MHz	Up to 133 MHz
CPU:SDRAM Ratios	1:1, 2:1, 3:1, 4:1	1:1, 2:1, 5:2, 3:1, 4:1
Dhrystones (DMIPS)	304@200 MHz, 404@266 MHz	404@266 MHz, 506@333 MHz, 607@400 MHz
I/O Voltage	+3.3V, +5V tolerant (except for SDRAM)	+3.3V, +5V tolerant (except for SDRAM & GPIO24)
Logic Voltage	+2.5V +/-0.20V	+1.8V +/-0.10V
Typical Power (W)	1.5W@200 MHz, 2.0W@266 MHz	Estimated: 1.1W@266 MHz, 1.3W@333 MHz
Caches	16 KB Instruction, 8 KB Data	16 KB Instruction, 16 KB Data

Table 1. Comparison of 405GP to 405GPr

Feature	405GP	405GPr
GPIOs	23	24
External Interrupts	7	7-13
Packaging	456 ball 35mm E-PBGA (1.27 mm ball pitch) 456 ball 27mm E-PBGA (1.0 mm ball pitch) 413 ball 25mm E-PBGA (1.0 mm ball pitch)	456 ball 35mm E-PBGA (1.27 mm ball pitch) 456 ball 27mm E-PBGA (1.0 mm ball pitch)

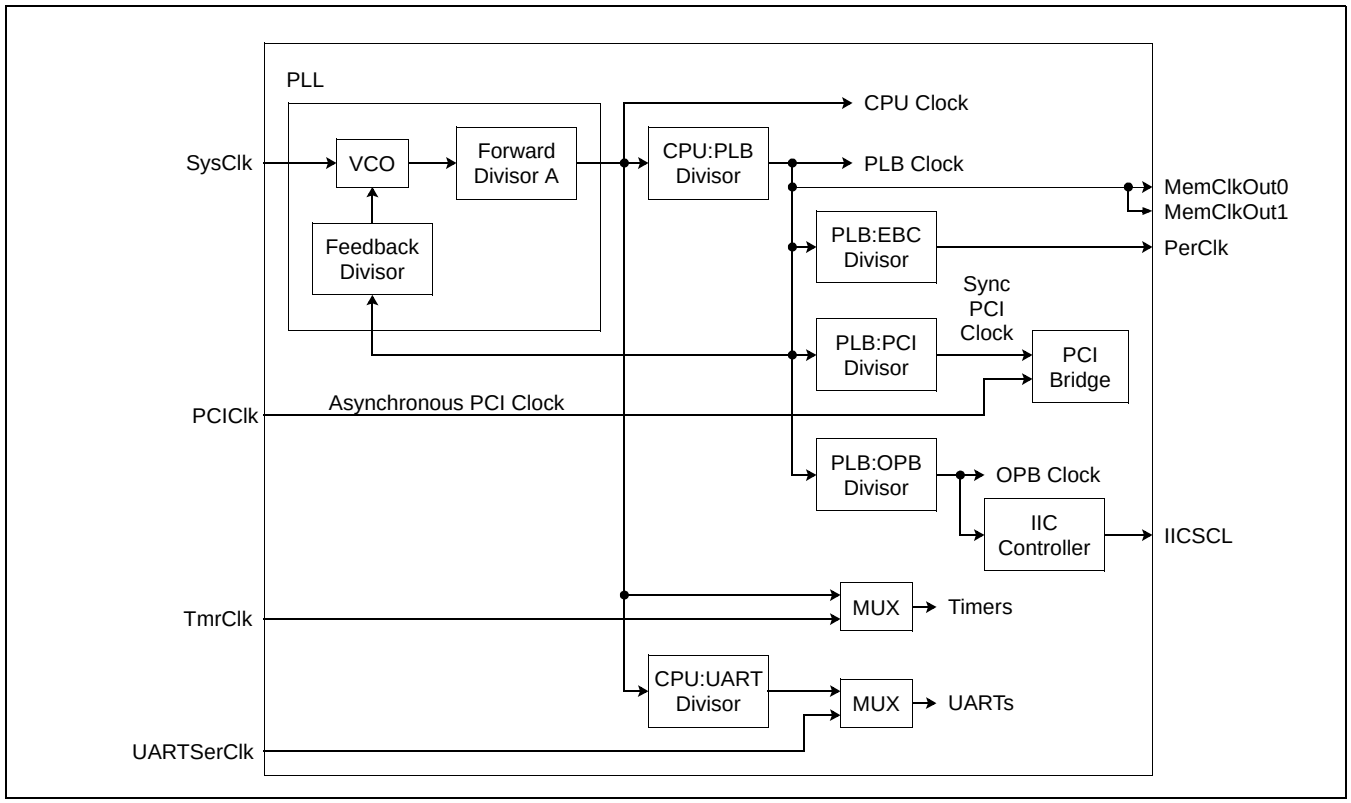
HARDWARE DIFFERENCES

Most of the hardware differences between the 405GPr and the 405GP are a direct result of mapping the 405GP design to the 0.18µm CMOS SA-27E process technology. While the most significant difference is the +1.8V logic supply voltage, the move to SA-27E brought along modifications required to support higher clock rates, along with minor changes and functional improvements to some of the IBM Blue Logic™ cores used to create the 405GPr.

Clocking Changes

Both the 405GP and 405GPr generate their internal clocks from SysClk through the use of an internal Phase Locked Loop (PLL). As shown in *Figure 1*, the 405GP SDRAM, CPU, Processor Local Bus (PLB), On-chip Peripheral Bus (OPB), synchronous PCI, and peripheral bus (PerClk) clocks are derived from a common PLL output clock.

Figure 1. PPC405GP Clocking Structure



Since each of the divisors must be an integer, all of these clocks are integer submultiples of the CPU clock rate. In addition, since the feedback clock to the PLL must be the same frequency as SysClk, it is required that the PLB clock, which is the same as the SDRAM clock, switch at an integer multiple of the SysClk input frequency. Summarizing, the 405GP clock rates are:

$$\begin{aligned} \text{CPU} &= \text{VCO} \div \text{Forward A Divisor} \\ \text{PLB} = \text{MemClkOut0:1} &= \text{CPU} \div \text{CPU:PLB Divisor} \\ \text{Synchronous PCI} &= \text{CPU} \div (\text{CPU:PLB Divisor} \bullet \text{PLB:PCI Divisor}) \\ \text{PerClk} &= \text{CPU} \div (\text{CPU:PLB Divisor} \bullet \text{PLB:EBC Divisor}) \\ \text{OPB} &= \text{CPU} \div (\text{CPU:PLB Divisor} \bullet \text{PLB:OPB Divisor}) \end{aligned}$$

where

$$\text{VCO} = \text{SysClk} \bullet (\text{Forward Divisor A} \bullet \text{CPU:PLB Divisor} \bullet \text{Feedback Divisor})$$

and each of the divisors are configurable with pull-up and pull-down resistors to values within the following ranges:

Table 2. 405GP Clock Divisors

Divisor	Range
Forward A	3, 4, 6
CPU:PLB	1-4
PLB:EBC	2-5
PLB:PCI	1-4
Feedback	1-4

Table 3 shows the most common clocking configurations used in 405GP-based designs.

Table 3. Typical 405GP Clocking Divisors and Resulting Clock Rates

	Divisor					Clock Rate (MHz)				
SysClk	Forward A	CPU:PLB	PLB:PCI	PLB:EBC	Feedback	VCO	CPU	PLB MemClkOut	PCI	PerClk
25 MHz	3	2	4	4	4	600	200	100	25	25
				2						50
	4		3	4		800			33.33	25
				2						50
33.33 MHz	3	2	4	4	4	800	266.66	133.33	33.33	33.33
				2						66.66

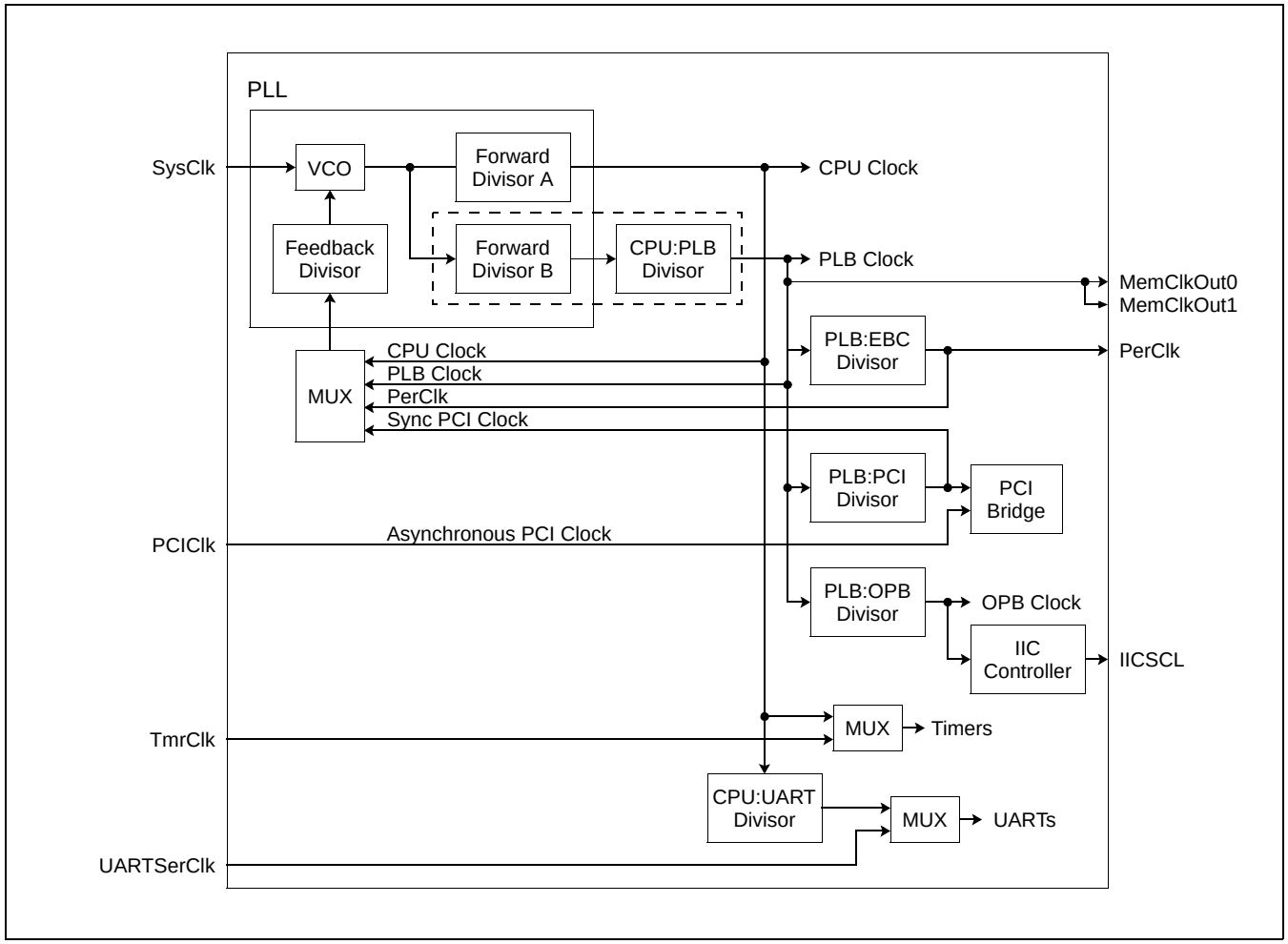
Table 3 illustrates that the SDRAM, synchronous PCI, and peripheral bus clock rates are all integer submultiples of the CPU clock rate. Given that the 405GP is offered at CPU frequencies of 200 MHz and 266.66 MHz, this is not a limitation as SDRAM memory is readily available at clock rates up to 133.33 MHz. However, since the 405GPr is offered at a CPU clock rate of 333.33 MHz, a non-integral CPU:SDRAM clock ratio of 5:2 is required for the CPU to run at 333.33 MHz while the SDRAM is clocked at the optimal rate of 133.33 MHz.

The 405GPr implements a new, yet 405GP-compatible clocking structure that supports both integral and non-integral ratios between the CPU and SDRAM clocks. As shown in *Figure 2* on page 6, the 405GPr uses independent PLL divisors to generate the CPU and PLB clocks from a common VCO output. It should be noted that the Forward A Divisor, Forward B Divisor, and CPU:PLB Divisor are not individually programmable. When the 405GPr is operating in Legacy Mode, both forward divisors are set to a common value as indicated by the PFWD strap inputs and the CPU:PLB divisor is set according to the PDC strap inputs. When using New Mode clocking, the forward divisors are set individually based on strapping inputs and the CPU:PLB Divisor is forced to a value of 2. Please see *Strapping Changes* on page 8 for details on how the 405GPr is configured for either Legacy or New Mode clocking.

The 405GPr clocks are derived from the VCO output as follows:

$$\begin{aligned}
\text{CPU} &= \text{VCO} \div \text{Forward A Divisor} \\
\text{PLB} = \text{MemClkOut0:1} &= \text{VCO} \div (\text{Forward B Divisor} \bullet \text{CPU:PLB Divisor}) \\
\text{Synchronous PCI} &= \text{VCO} \div ((\text{Forward B Divisor} \bullet \text{CPU:PLB Divisor}) \bullet \text{PLB:PCI Divisor}) \\
\text{PerClk} &= \text{VCO} \div ((\text{Forward B Divisor} \bullet \text{CPU:PLB Divisor}) \bullet \text{PLB:EBC Divisor}) \\
\text{OPB} &= \text{VCO} \div ((\text{Forward B Divisor} \bullet \text{CPU:PLB Divisor}) \bullet \text{PLB:OPB Divisor})
\end{aligned}$$

Figure 2. PPC405GPr Clocking Structure



where the VCO frequency is dependent on the source of the PLL feedback clock:

Table 4. 405GPr PLL VCO Frequency versus Feedback Clock

PLL Feedback Clock	VCO Frequency
CPU Clock	SysClk • Feedback Divisor • Forward A Divisor
PLB Clock	SysClk • Feedback Divisor • (Forward B Divisor • CPU:PLB Divisor)
PerClk	SysClk • Feedback Divisor • (Forward B Divisor • CPU:PLB Divisor) • PLB:EBC Divisor
Synchronous PCI Clock	SysClk • Feedback Divisor • (Forward B Divisor • CPU:PLB Divisor) • PLB:PCI Divisor

As shown in *Table 5*, the PLL feedback clock is selected automatically based on several bit fields within the Pin Strapping Register (CPC0_PSR).

Table 5. 405GPr PLL Feedback Mode

CPC0_PSR Bit Field				
PAME	**NEWE**	**EBDP=PFBD**	**ESME**	
PCI Asynchronous Mode Enable	**New Mode Enable**	**PLB:EBC Divisor equals Feedback Divider**	**External Bus Synchronous Mode Enable**	**PLL Feedback Clock**
0	—	—	—	Sync PCI Clock
1	0	False	—	PLB Clock
1	0	True	—	PerClk
1	1	—	0	CPU Clock
1	1	—	1	PerClk

Table 6 illustrates several of the clock ratios supported by the 405GPr clocking structure. For complete details on selecting and strapping a clocking configuration for the 405GPr, please refer to the *PowerPC 405GPr Embedded Processor User's Manual*. The *PowerPC 405GPr Embedded Processor Data Sheet* specifies the VCO, CPU, and other uppermost frequency limits for each of the various 405GPr speed grades.

Table 6. Sample 405GPr Clocking Divisors and Resulting Clock Rates

	Divisors		**Clock Rate (MHz)**		
SysClk	**Forward A**	**Forward B • CPU:PLB**	**VCO**	**CPU**	**PLB=MemClkOut**
33.33 MHz	4	8	800	200	100
	3	6	800	266.66	133.33
	2	6	600	300	100
	4	10	1333.33	333.33	133.33
	2	6	800	400	133.33

Internal Clocking Changes

Compared to the 405GP, the 405GPr includes several internal clocking changes designed to improve overall system performance. The Universal Interrupt Controller (UIC) now runs at the PLB clock rate instead of the OPB clock rate. By clocking the UIC at the higher PLB clock rate, Device Control Register (DCR) accesses targeting the UIC require less time. The ability to access the UIC in less time serves to reduce interrupt latency. The second clocking change is that the Media Access Layer (MAL) controller, which is used in conjunction with the internal ethernet controller, now runs at one half the PLB clock rate, whereas it previously ran at the OPB clock rate.

Strapping Changes

During a system reset, both the 405GP and 405GPr are configured through the use of strapping (pull-up or pull-down) resistors on various I/Os. To provide compatibility with existing designs, the 405GPr enters Legacy (405GP) Mode if a logic zero is detected on GPIO24 (ball D20). Since D20 is a reserved ball on the 405GP, and the 405GPr has an on-chip pull-down on this I/O, installing a 405GPr in a 405GP design automatically selects Legacy Mode. *Table 7* details the strapping differences between Legacy Mode and New Mode.

Table 7. Comparison of Legacy and New Mode Strapping

CPC0_PSR		I/O		Strap Function	
Bit	**Name**	**Name**	**Ball**	**Legacy Mode**	**New Mode**
0:1	PFWD	DMAAck0	D16	PLL Forward Dividers	Forward Divider A: Bit 0
		DMAAck1	B15		Forward Divider A: Bit 1
2:3	PFBD	DMAAck2	B14	PLL Feedback Divider	Feedback Divider: Bit 0
		DMAAck3	C12		Feedback Divider: Bit 1
4:6	PT	UART0_Tx	AF3	PLL Tuning Bits	
		UART0_DTR	AF2		
		UART0_RTS	AD16		
7:8	PDC	EMCTxD3	P25	CPU:PLB Divider	Forward B Divider: Bit 0
		EMCTxD2	L24		Forward B Divider: Bit 1
9:10	ODP	EMCTxD1	L25	PLB:OPB Divider	
		EMCTxD0	J26		
11	PDP	GPIO1[TS1E]	D18	PLB:PCI Divider	
12		GPIO2[TS2E]	C20		
13	EBDP	EMCTxErr	K25	PLB:EBC Divider	
14		EMCTxEn	K23		
15	RW	UART1_Tx	AC2	ROM Width	
16		$\overline{\text{UART1\_RTS}}$ [UART1_DTR]	AD2		
17	RL	HoldAck	U2	ROM Location	
18	Reserved				
19	PAME	ExtAck	Y3	PCI Asynchronous Mode Enable	
20	ESME	GPIO3[TS1O]	A22	—	Phase Align PerClk to SysClk
21	PAE	GPIO4[TS2O]	AF18	PCI Internal Arbiter Enable	
22	PFWDA	GPIO5[TS3]	AC09	—	Forward A Divider: Bit 2
23	PFWDB	GPIO6[TS4]	AE08	—	Forward B Divider: Bit 2

Table 7. Comparison of Legacy and New Mode Strapping (Continued)

CPC0_PSR		I/O		Strap Function	
Bit	**Name**	**Name**	**Ball**	**Legacy Mode**	**New Mode**
24:25	PFBD2	GPIO7[TS5]	AF05	—	Feedback Divider: Bit 2
		GPIO8[TS6]	AC07	—	Feedback Divider: Bit 3
26	NEWE	GPIO24	D20	New Mode Enable	
				0	1
27	FCD	GPIO9	AB3	Flip Circuit Disable	
				—	0
28:31	Reserved				

Whenever ball GPIO24 (ball D20) is strapped high to select New Mode clocking, it is required that GPIO9 (ball AB3) be strapped low. This enables logic within the 405GPr that ensures the CPU and PLB clocks are appropriately rising edge aligned when the CPU to PLB clock ratio is not an integer.

Reset Logic Changes

The new clocking structure included in the 405GPr results in a longer delay between the deassertion of $\overline{\text{SysReset}}$ and the start of code execution. When operating in Legacy Mode, there are approximately 8324 SysClk cycles from $\overline{\text{SysReset}}$ inactive until the start of code execution. This represents an increase over the 8192 SysClk cycles that occur with the 405GP. When New Mode clocking is active, the time until the first instruction fetch is approximately 16648 SysClk cycles.

I/O Differences

There are two categories of differences at the I/O level, those resulting from the use of 0.18µm CMOS SA-27E I/O cells, and those related to logical changes within the 405GPr. As a CoreConnect™ based product, the 405GPr was designed and fabricated using the IBM Blue Logic ASIC process flow. This methodology makes use of standard cell libraries, both for logic functions and I/Os. Since the I/Os are technology-specific, the 405GPr I/O drivers are somewhat different than those used for the 405GP. In all cases, the 405GPr drivers have the same output impedance as those on the 405GP. However, as shown in *Table 8*, there are some differences in both the logic low and logic high drive strengths and the slew rates. Since those I/Os with increased slew rates will exhibit faster signal transitions, a design migrated from the 405GP to the 405GPr may have a different radiated emissions profile. As a result, it is recommended that electromagnetic compatibility testing be performed to ensure that the migrated design conforms to all applicable standards.

Table 8. I/O Driver Comparison of 405GP to 405GPr

Driver Type	Drive Strength	Slew (mA/ns)		I_{high} (mA)		I_{low} (mA)	
		405GP	405GPr	405GP	405GPr	405GP	405GPr
PCI	A	Meets PCI Revision 2.2 Specifications for 3.3V Signalling					
3.3V 20Ω	B	105	135	40	28.7	25	19.3
3.3V 35Ω	A/B	75/110	90/125	19	15.3	12	10.2
3.3V 50Ω	B	100	130	12	10.3	8	7.1
3.3V 35Ω, 5V tolerant	A/B	110/115	90/125	17	15.3	11	10.2
3.3V 50Ω, 5V tolerant	A/B	95/95	80/130	12	10.3	8	7.1

Most of the 405GPr I/O timing specifications are bounded by those for the 405GP. *Table 9* lists all of the 405GPr I/Os with timing specifications that differ from the corresponding 266 MHz 405GP specifications. Instances where the 405GPr specifications exceed the 405GP are shaded in gray. While the 405GPr does not meet all of the 266 MHz 405GP specifications, it provides both increased output hold times (equivalent to the minimum output delay) and decreased input hold times on both the SDRAM and peripheral interfaces.

The SDRAM address and ethernet interfaces have timing differences which at first appear significant, yet should not affect most designs. To reduce simultaneous switching effects, the individual bits in the 405GPr SDRAM address bus transition in a staggered manner rather than all at once. While this change increased the SDRAM address output valid time to more than one MemClkOut0:1 cycle, the SDRAM address and control interface is multicycle. The address and control signals are configurable via SDRAM0_TR[LDF] such that they are driven 2 to 4 MemClkOut0:1 cycles prior to when they are used by the SDRAM. Even with the increased SDRAM address output delay, most designs should still have positive margin with the minimum possible leadoff setting of SDRAM0_TR[LDF]=2.

Table 9. I/O Timing Comparison (in ns) Between the 405GP and 405GPr

Interface	Signal	Input Setup (min)		Input Hold (min)		Output Delay (min)		Output Delay (max)	
		GP	GPr	GP	GPr	GP	GPr	GP	GPr
SDRAM	BA1:0	—	—	—	—	1.0	1.6	5.7	4.5
	BankSel3:0	—	—	—	—	1.0	1.5	4.8	4.5
	CAS	—	—	—	—	1.0	1.5	5.7	4.4
	ClkEn0:1	—	—	—	—	1.0	1.4	4.2	3.9
	DQM0:3	—	—	—	—	1.0	1.4	4.8	4.5
	DQMCB	—	—	—	—	1.0	1.4	4.8	4.3
	ECC0:7	1.5	1.4	1.0	0.0	1.0	1.5	4.8	4.5
	MemAddr12:0	—	—	—	—	1.0	1.5	5.7	11.0
	MemData0:31	1.5	1.4	1.0	0.0	1.0	1.4	4.9	4.6
	RAS	—	—	—	—	1.0	1.5	5.7	4.4
	WE	—	—	—	—	1.0	1.5	5.7	4.4

Table 9. I/O Timing Comparison (in ns) Between the 405GP and 405GPr (Continued)

Interface	Signal	Input Setup (min)		Input Hold (min)		Output Delay (min)		Output Delay (max)	
		GP	GPr	GP	GPr	GP	GPr	GP	GPr
Peripheral	BusReq	—	—	—	—	0.0	2.2	6.0	6.1
	DMAAck0:3	—	—	—	—	0.0	2.2	6.0	6.1
	DMAReq0:3	4.0	3.2	1.0	0.0	—	—	—	—
	EOT0:3[TC0:3]	—	—	—	—	0.0	2.0	6.0	6.4
	$\overline{\text{ExtAck}}$	—	—	—	—	0.0	2.1	6.0	5.9
	$\overline{\text{ExtReq}}$	4.0	4.1	1.0	0.0	—	—	—	—
	HoldAck	—	—	—	—	0.0	2.0	6.0	6.1
	HoldPri	3.0	2.1	1.0	0.0	—	—	—	—
	HoldReq	4.0	3.1	1.0	0.0	—	—	—	—
	PerAddr0:31	3.0	2.2	1.0	0.0	0.0	2.0	7.2	7.1
	$\overline{\text{PerBLast}}$	3.0	3.3	1.0	0.0	0.0	2.3	6.0	6.5
	$\overline{\text{PerCS0:7}}$	—	—	—	—	0.0	2.1	6.0	6.5
	PerData0:31	5.0	4.7	1.0	0.9	0.0	1.9	7.2	7.2
	PerErr	3.0	2.4	1.0	0.0	—	—	—	—
	$\overline{\text{PerOE}}$	—	—	—	—	0.0	2.1	6.0	6.5
	PerPar0:3	3.0	2.3	1.0	0.0	0.0	2.1	7.2	7.2
	PerR/$\overline{\text{W}}$	4.0	3.3	1.0	0.0	0.0	2.1	6.0	6.6
	PerReady	6.5	5.5	1.0	0.0	—	—	—	—
	$\overline{\text{PerWBE0:3}}$	3.0	2.3	1.0	0.0	0.0	2.2	6.0	6.1
Ethernet	EMCTxD3:0 EMCTxEn EMCTxErr	—	—	—	—	2	5	20	20
	EMCRxD3:0 EMCRxDV EMCRxErr	4	5	1	5	—	—	—	—

The ethernet interface timing differences resulted from the inclusion of edge conditioning circuitry designed to prevent noise external to the 405GPr die from producing extraneous edges and false clocking on the ethernet receive and transmit clocks. Please see “Edge Conditioning Circuitry” on page 15 for additional details. Although the 405GPr ethernet output delays and input setup times exceed the 405GP data sheet values, the 405GPr datasheet specifications meet the MII timing requirements dictated by the IEEE® Std 802.3 specification.

Given the I/O driver and timing differences between the 405GPr and 405GP, designers are strongly encouraged to revalidate existing designs using the 405GPr IBIS model in conjunction with the timing specifications presented in the *PowerPC 405GPr Embedded Processor Data Sheet*.

I/O Functionality Changes

As previously documented, one of the 405GP reserved balls was converted to GPIO24 and is used as a strapping input to determine whether the 405GPr operates in Legacy Mode or New Mode. In addition to this I/O change, the receiver and driver inhibit inputs, used only during production test, were removed, the PLL was provided with a dedicated ground ball, and a second GPIO is now utilized as a reset strapping input to enable logic that ensures the PLB and CPU clocks are rising edge aligned when the 405GPr operates in New Mode. These changes are documented in *Table 10*.

Table 10. I/O Functionality Changes

I/O Ball	405GP		405GPr	
	Name	Function	Name	Function
C25	RcvrInh	Receiver Inhibit	Reserved	No Internal Connection
E24	DrvrInh1	Driver Inhibit 1	Reserved	No Internal Connection
E23	DrvrInh2	Driver Inhibit 2	Reserved	No Internal Connection
E22	GND	Ground	AGND	PLL Analog Ground
D20	Reserved	—	GPIO24	GPIO
				Legacy Mode Select
AB3	GPIO9[TrcClk]	GPIO / Trace Clock	GPIO9[TrcClk]	GPIO / Trace Clock
				PLB/CPU Rising Edge Alignment (Flip) Circuit Enable

The 405GPr does not provide dedicated manufacturing test inputs for inhibiting the receivers and drivers. While some 405GP-based designs may have used these inputs to place the chip I/Os in the high-Z state for board-level testing, such usage was neither documented nor recommended. Instead, applications should use the JTAG boundary scan interface to place the 405GPr I/Os in the high-impedance state during board-level test.

RISCTrace Interface

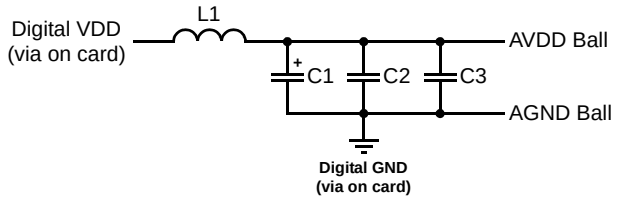
The 405GPr and 405GP RISCTrace™ interfaces are functionally identical and provide an instruction trace stream at one half the CPU clock rate. Since the 405GPr is offered at CPU speeds up to 400 MHz, the RISCTrace interface signals (TrcClk, TS1E, TS1O, TS2E, TS2O, TS3:6) can switch at up to a 200 MHz rate. Designs including RISCTrace functionality should use the combined RISCWatch™ / RISCTrace Mictor connector as it is electrically superior to pin headers. In addition, the RISCTrace signal nets should be matched in length and the 405GPr IBIS model used to ensure that all signals reach the Mictor connector at the same time and with minimal distortion.

PLL Analog Voltage Supply

In contrast to the 405GP, which did not provide a separate PLL analog ground, the 405GPr features dedicated voltage (AVDD) and ground (AGND) supply pins for the analog circuitry within the PLL. Noise on either of these signals can cause excessive phase jitter at the output of the PLL. To provide isolation from the noisy internal digital power and ground signals, AVDD and AGND are brought to dedicated package balls.

The filter circuit shown in *Figure 3* should be used to power the PLL. To provide the cleanest possible analog ground, AGND should be brought out from the package ball and connected to the digital ground plane at the capacitors. All wire lengths should be kept as short as possible, and appropriately shielded to minimize coupling from other signals.

Figure 3. Recommended Analog Voltage Filter Circuit Figure 4.



L1	2.2 μH SMT inductor (equivalent to MuRata LQH3C2R2M34) or SMT chip ferrite bead (equivalent to MuRata BLM31A700SN1)
C1	3.3 μF SMT tantalum
C2	0.1 μF SMT monolithic ceramic capacitor with X7R dielectric or equivalent
C3	0.01 μF SMT monolithic ceramic capacitor with X7R dielectric or equivalent

27mm Power Supply Pin Out Differences

Both the 405GP and 405GPr utilize PBGA packages where the silicon die is mechanically affixed to a miniature circuit board called a laminate. The powers, grounds, and signals on the die are wirebonded to pads on the top of the laminate and solder balls are attached to the bottom side. While each signal has a discrete trace from its wirebond pad to corresponding solder ball, powers and grounds are distributed through planes within the laminate.

As shown in Table 11, the 27mm 405GPr differs from the 27mm 405GP in that twelve previously reserved balls now serve as additional powers and grounds. For the 405GPr these ball locations tie directly to the internal OVdd (+3.3V) power and ground planes. In contrast, these balls are internal no-connects within the 27mm 405GP. While it is recommended that circuit boards designed to accept either the 27mm 405GP or 405GPr wire these balls as specified by the PPC405GPr Data Sheet, existing 27mm 405GP-based systems migrating to the 405GPr may leave the new powers and grounds unconnected.

Table 11. 27mm Power Supply Pin Out Differences

Package Ball	405GP	405GPr	Package Ball	405GP	405GPr
A19	Reserved	Ground	P03	Reserved	OVdd (+3.3V)
B17	Reserved	OVdd (+3.3V)	U25 Reserved	OVdd (+3.3V)	
C13	Reserved	OVdd (+3.3V)	W26	Reserved	Ground
H01	Reserved	Ground	AD14	Reserved	OVdd (+3.3V)
K02	Reserved	OVdd (+3.3V)	AE10	Reserved	OVdd (+3.3V)
N24	Reserved	OVdd (+3.3V)	AF08	Reserved	Ground

NEW FEATURES

In addition to the changes brought on by the migration to the 0.18μm CMOS SA-27E process technology, the 405GPr includes several hardware and software level enhancements. Receiver gating provides a means for effectively isolating unused inputs, thereby removing the need for pull-up or pull-down resistors. Edge conditioning circuitry on the ethernet clock and external interrupt inputs prevents off-die noise induced glitches from producing extraneous edge transitions. An additional GPIO, and the ability to use any six of the GPIOs as external interrupts help to minimize external logic, while the addition of several I/Os to the JTAG boundary scan chain raises board-level test coverage. Finally, the inclusion of a permanent, unique, 64-bit binary signature can serve as a means of identifying a particular system throughout its life cycle.

Receiver Gating

While neither the 405GP or 405GPr require that designers terminate most unused or undriven inputs and bididirectional I/Os, doing so is generally considered good design practice. By terminating unused I/Os, their input level is fixed to a defined logic state and, more importantly, the receiver section of the I/O is prevented from entering into and possibly staying in the logic zero to logic one transition region. The two key reasons for avoiding the transition region are that some types of receivers draw more current in the transition region and the possibility exists that the internal output of the receiver could oscillate. If this occurs, the result is both unnecessary power consumption and an increase in on-chip noise.

Through a software-controlled receiver gating feature, the 405GPr allows unused I/Os to be placed in a state that requires no external termination. When an I/O's receiver section is gated off, the voltage level present on the receiver input has no affect on either the receiver or any other logic within the 405GPr. As shown in *Table 12*, the 405GPr provides receiver gating for either an entire interface, or for a selectable portion of the interface. For example, since the peripheral bus interface width can be 8-, 16-, or 32-bits, the 405GPr allows gating only a portion of the peripheral data bus. In contrast, receiver gating for the PCI and SDRAM interfaces disables all receivers on the particular interface.

Table 12. 405GPr CPC0_CR1 Receiver Gating Bit Fields

Bits	Name	Reset Value	Usage
21:24	PARG	0b0000	Peripheral Address Bus 0b0000 No gating 0b0001 Gate PerAddr0:1 0b0010 Gate PerAddr0:2 0b0011 Gate PerAddr0:3 : : : : 0b1110 Gate PerAddr0:14 0b1111 Gate PerAddr0:15
25:26	PDRG	0b00	Peripheral Data Bus 0b00 No gating 0b01 Gate PerData8:31 0b10 Gate PerData16:31 0b11 Gate PerData24:31
27	PCIRG	0b0	PCI Interface 0b0 No gating 0b1 Gate PCIAD31:0. PCIC3:0[$\overline{\text{BE3:0}}$], PCIParity, $\overline{\text{PCIFrame}}$, $\overline{\text{PCIIRDY}}$, $\overline{\text{PCITRDY}}$, $\overline{\text{PCIStop}}$, $\overline{\text{PCIDevSel}}$, $\overline{\text{PCISErr}}$, $\overline{\text{PCIPErr}}$, PCIClk, $\overline{\text{PCIReq0}}$[$\overline{\text{Gnt}}$], and $\overline{\text{PCIReq1:5}}$
28	SDRG	0b0	SDRAM Interface 0b0 No gating 0b1 Gate MemData0:31 and ECC0:7
29	ENRG	0b0	Ethernet Interface 0b0 No gating 0b1 Gate EMCMDIO, PHYCol, PHYCrS, PHYRxD3:0, PHYRxClk, PHYRxDV, PHYRxErr, PHYRxErr, and PHYTxClk
30	U0RG	0b0	UART 0 0b0 No gating 0b1 Gate UART0_Rx, $\overline{\text{UART0\_DCD}}$, $\overline{\text{UART0\_CTS}}$, and $\overline{\text{UART0\_RI}}$
31	U1RG	0b0	UART 1 0b0 No gating 0b1 Gate UART1_Rx and $\overline{\text{UART1\_DSR}}$[$\overline{\text{UART1\_CTS}}$]

In addition to those I/Os which can have their receiver sections explicitly gated via CPC0_CR1, the external UART serial clock input, UARTSerClk, is automatically gated whenever CPC0_CR0[U0EC,U1EC]=0b00 as then both UARTs derive their clocks from the internal PLL rather than the external input. While the GPIOs do not implement receiver gating this is not an issue as software can simply program any unused GPIOs as outputs, and thus ensure that the receiver section of the corresponding GPIO observes a solid level.

Edge Conditioning Circuitry

The Ethernet receive clock (PHYRxClk), transmit clock (PHYTxClk), and external interrupts configured in edge-triggered mode are more sensitive to noise induced glitches than other signals because they drive clock inputs of registers. Whereas the noise sensitivity of data receiver inputs is proportional to the threshold voltage of the logic, noise sensitivity of clock receiver inputs is proportional to the hysteresis of the receiver, which is several times less than the logic threshold. Noise coupling between signal and clock traces external to the 405GPr chip die is aggravated by the faster 0.18µm technology. In order to allow the 405GPr to be used in all applications, including existing 405GP applications, without requiring board re-layout or further restrictions on driver slew rates, edge conditioning circuitry has been added to the Ethernet receiver and transmit clock inputs and edge-triggered external interrupt signals.

The edge conditioning circuitry prevents noise induced glitches from producing extraneous edges and false clocking. Although the edge conditioning circuitry skews the ethernet transmit data out of the 405GPr, the interface still easily conforms to the IEEE 802.3 media independent interface (MII) signal timing characteristics. The duration of glitches that can be conditioned during an edge is proportional to the setting of edge conditioning strength. Table 13 describes the Chip Edge Conditioning Register (CPC0_ECR) bit fields. During system intialization software must write CPC0_ECR with the recommended value of 0x60606000.

Table 13. 405GPr CPC0_ECR Chip Edge Conditioning Register Bit Fields

Bits	Name	Reset Value	Usage	Conditioning Strength
0:2	RX	0b000	Ethernet Receiver Clock (PHYRxClk) Edge Conditioning	0b000 = Bypass 0b001 = 1 0b010 = 2 0b011 = 3 0b100 = 4 0b101 = 6 0b110 = 8 0b111 = 10
8:10	TX	0b000	Ethernet Transmit Clock (PHYTxClk) Edge Conditioning	
16:18	UIC	0b000	UIC Edge-Triggered Interrupts Edge Conditioning	

New GPIO

In order to implement the automatic selection of Legacy Mode when a 405GPr is populated in a 405GP design, a reserved 405GP package ball was converted to a strapping pin shared with a new function: GPIO24. If during a chip reset GPIO24, which includes a weak internal pull-down, is observed at a logic zero, Legacy Mode clocking is selected. Otherwise, the 405GPr uses the more flexible New Mode clocking. After reset, GPIO24 may be used in a design the same as any of the other GPIOs that are shared with strapping functions, with the exception that GPIO24 is only +3.3V tolerant.

Additional External Interrupts

The 405GPr provides the ability to add six external interrupts to the seven already available on the 405GP. This is accomplished by logic that allows routing any of the 24 GPIOs to six previously unused Universal Interrupt Controller (UIC) inputs. For those GPIOs that are shared with other functions, the corresponding I/O must first be configured via CPC0_CR0 to be a GPIO. *Table 14* shows how the new GPIO to UIC External Interrupt Routing Register (CPC0_EIRR) logically routes GPIO inputs used as interrupts to the UIC..

Table 14. 405GPr GPIO to UIC External Interrupt Routing Register (CPC0_EIRR)

Bits	Name	Description
0:4	IRQ19	0b00000 Force input to UIC IRQn to logic zero 0b00001 Route GPIO1 to UIC IRQn 0b00010 Route GPIO2 to UIC IRQn 0b00011 Route GPIO3 to UIC IRQn : 0b11000 Route GPIO24 to UIC IRQn
5:9	IRQ20	
10:14	IRQ21	
15:19	IRQ22	
20:24	IRQ23	
25:29	IRQ24	

Electronic Chip ID

To facilitate production tracking within AMCC, each 405GPr is laser personalized with a 64-bit binary signature. Since no two 405GPr modules will ever have the same signature, 405GPr-based products can use the signature as a unique system level identifier. Software may read the signature via two 32-bit registers: ECID0 at DCR address 0xA8 and ECID1 at address 0xA9.

JTAG Boundary Scan Changes

The 405GPr enables a higher degree of board-level testing than the 405GP by including the SysClk and PCIClk inputs in the JTAG boundary scan chain. With the addition of these two signals, all I/Os are present in the scan chain except for the AMCC manufacturing only use TestEn input, and the JTAG signals: TRST, TCK, TMS, TDI, and TDO.

DIFFERENCES AFFECTING SOFTWARE

The most significant software-level difference between the 405GPr and 405GP is the larger data cache. The 16 KB 405GPr data cache has twice as many lines as were present in the 405GP data cache. As a result, all cache invalidation and flushing code requires modification to account for the additional lines.

Existing code bases may also be affected by the new Processor Version Register (PVR) and JTAG ID (CPC0_JTAGID) values assigned to the 405GPr. The remaining programming level differences involve new features and functions added to the 405GPr. *Table 15* is a complete list of all registers that are either new to the 405GPr, or include new bit fields. For more detailed information on these registers please see the *PowerPC 405GPr Embedded Processor User's Manual*.

Table 15. PPC405GPr Register Additions and Changes

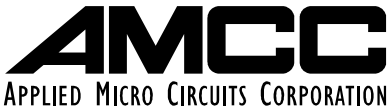
Register			Description	Change
Name	Type	Address		
CPC0_ECID0	DCR	0x0A8	Unique chip ID, upper 32 bits	New register
CPC0_ECID1	DCR	0x0A9	Unique chip ID, lower 32 bits	New register
CPC0_ECR	DCR	0x0AA	Chip Edge Conditioning Register	New register
CPC0_PLLMR	DCR	0x0B0	PLL Mode Register	Additional bit fields for new PLL control bits
CPC0_CR1	DCR	0x0B2	Chip Control Register 1	Additional bit fields for receiver gating
CPC0_PSR	DCR	0x0B4	Chip Pin Strapping Register	Additional bit fields for new PLL control bits

Table 15. PPC405GPr Register Additions and Changes (Continued)

Register			Description	Change
Name	**Type**	**Address**		
CPC0_JTAGID	DCR	0x0B5	JTAG ID Register	New value
CPC0_EIRR	DCR	0x0B6	External Interrupt Routing Register	New register
GPIO0_OR	Memory Mapped	0xEF600700	GPIO0 Output Register	Addtional bit field for GPIO24
GPIO0_TCR	Memory Mapped	0xEF600704	GPIO0 Three-State Control Register	
GPIO0_ODR	Memory Mapped	0xEF600718	GPIO0 Open Drain Register	
GPIO0_IR	Memory Mapped	0xEF60071C	GPIO0 Input Register	
UIC0_SR	DCR	0x0C0	UIC0 Status Register	Additional bits for new external interrupts
UIC0_ER	DCR	0x0C2	UIC0 Enable Register	
UIC0_CR	DCR	0x0C3	UIC0 Critical Register	
UIC0_PR	DCR	0x0C4	UIC0 Polarity Register	
UIC0_TR	DCR	0x0C5	UIC0 Triggering Register	
UIC0_MSR	DCR	0x0C6	UIC0 Masked Status Register	
PVR	SPR	0x1FF	Processor Version Register	New value
PCIC0_REVID	PCI Configuration Space		PCI Revision ID Register	New value
PCILO_PTM1MS	Memory Mapped	0xEF400030	PTM1 Memory Size/Attribute	Bit 0 (the lsb) is writeable to either 0 or 1.

CONCLUSION

Given the relatively minor hardware and software differences, the 405GPr provides an excellent opportunity for engineers with 405GP-based designs to realize increased system performance and at the same time reduce power dissipation. For compatibility with existing circuit board layouts, the 405GPr has the same physical I/O assignments as the 405GP. As a result, many applications can migrate their designs to the 405GPr by merely changing the logic supply voltage and confirming their system timing and signal integrity using the 405GPr IBIS model. New designs and redesigns of existing 405GP-based products can further utilize the increased integration of the 405GPr by taking advantage of an additional GPIO, an increased number of external interrupt inputs, and more flexible clocking options.



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