PM-DZ11
Asynchronous Multiplexer
Manual

Plessey
Peripheral
Systems

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General Information

1.1 INTRODUCTION

This manual provides the information needed to install and operate the PM-DZll multiplexed asynchronous serial line interface manufactured by Plessey Peripheral Systems, Irvine, California.

The material in this manual is arranged into four sections as follows:

Section 1 - GENERAL INFORMATION. This section contains a brief description of the PM-DZll, its configurations, and a list of specifications.

Section 2 - INSTALLATION AND OPERATION. This section explains the requirements and procedures for equipment installation. Interface information and switch settings are provided.

Section 3 - PROGRAMMING. A description of the PM-DZll control registers and programming features is presented to aid user programming.

Section 4 - FUNCTIONAL DESCRIPTION. This section provides a functional description of the PM-DZll and includes signal functions, block diagrams, and timing diagrams.

MAINTENANCE DRAWING PACKAGE. A separate drawing package, MD 701885, contains the parts lists, logic diagrams, and assembly drawings required for a complete understanding of the PM-DZll.

1.2 GENERAL DESCRIPTION

The PM-DZll is an asynchronous interface that connects a PDP-11 CPU to 8 or 16 asynchronous serial lines.* It is a low cost, multiplexed program controlled interface for connection of multiple local or remote terminals at moderate throughput. Local operation to terminals or computers is possible at speeds up to 9600 baud using EIA RS232C interfaces

*PDP-11 is a registered trademark of Digital Equipment Corporation.

or 20mA current loop. Remote operation using the public
switched telephone network is possible with EIA models. Data
set control is provided to permit auto answer (dial-up)
operation with modems capable of full-duplex operation (e.g.,
Bell Models 103 or 113). Remote operation over private lines
for full duplex point-to-point or full duplex multipoint (as
a master control station) is also possible. The PM-DZ11 does
not support half-duplex operations with secondary transmit
and receive operations. Half-duplex modems, such as the Bell
202, can be used on leased lines with the latter restrictions.
Figure 1-1 shows two possible applications for the PM-DZ11.
Further applications are inherent in these figures.
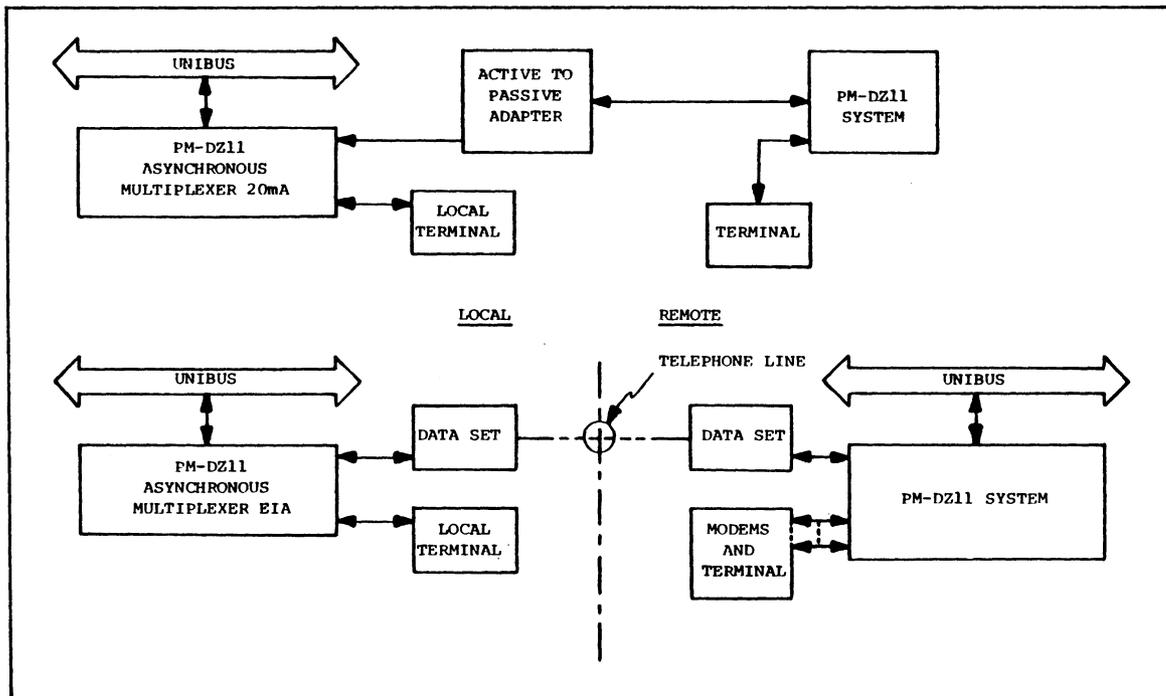
FIGURE 1-1: APPLICATIONS FOR THE PM-DZ11

1.3 FEATURES

Some of the features of the asynchronous interface are:

- Low cost 8 and 16-line multiplexed asynchronous interface
  for connecting Unibus PDP-11s to terminals or other
  computers.

- EIA and 20mA current loop models available.

- Local operation at speeds up to 9600 baud for maximum
  responsiveness of CRT terminals.

- Data set control on EIA models for full duplex dial-up remote operation.

- Programmable line speeds and character formats on a per line basis for flexibility and ease of configuration.

- FIFO buffered input transfers for reduced interrupt overhead and improved latency; program interrupt output transfers for low cost.

- Compact, single PC board, 8-line modularity.

- 16-line cable distribution panel conserves cabinet space.

1.4 PHYSICAL DESCRIPTION

The PM-DZll (8-line configuration) is comprised of a single hex small peripheral controller (SPC) module, a 5.25 inch unpowered distribution panel, and a 15-foot interconnecting cable. A 16-line configuration uses two modules and a single distribution panel which is connected by two ribbon cables. The basic PM-DZll module, cables, static filter panel, and distribution panel are shown in Figure 1-2.
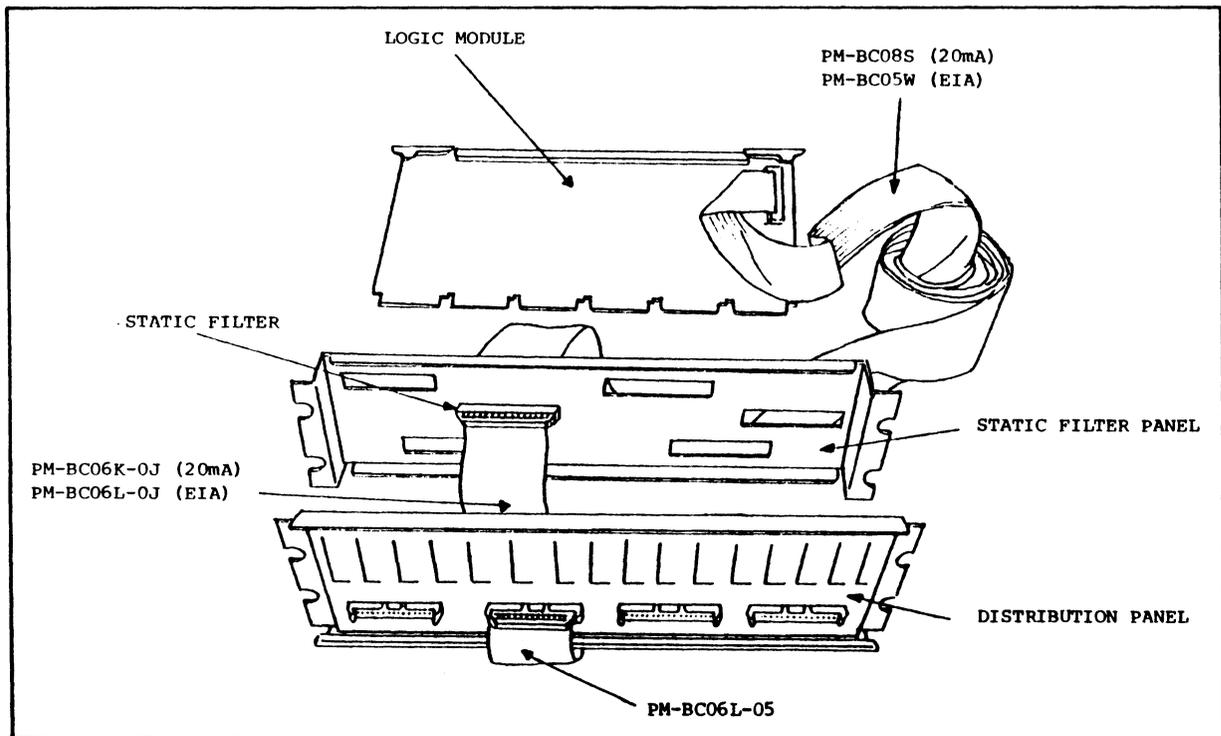
FIGURE 1-2: BASIC PM-DZll

1.5 CONFIGURATIONS

The PM-DZ11 is available in six different configurations. EIA models are PM-DZ11A, B, and E. Current loop models are PM-DZ11C, D, and F.

1.5.1 EIA Models

The PM-DZ11A is an 8-line configuration with EIA RS232C interface. It consists of a logic module, distribution panel, and interconnecting cables. The PM-DZ11B consists of an additional logic module, filter, and cables which expand the PM-DZ11A to a 16-line configuration. The PM-DZ11E is a 16-line configuration and is a combination of the PM-DZ11A and PM-DZ11B. Figure 1-3 shows the required hardware for various configurations.
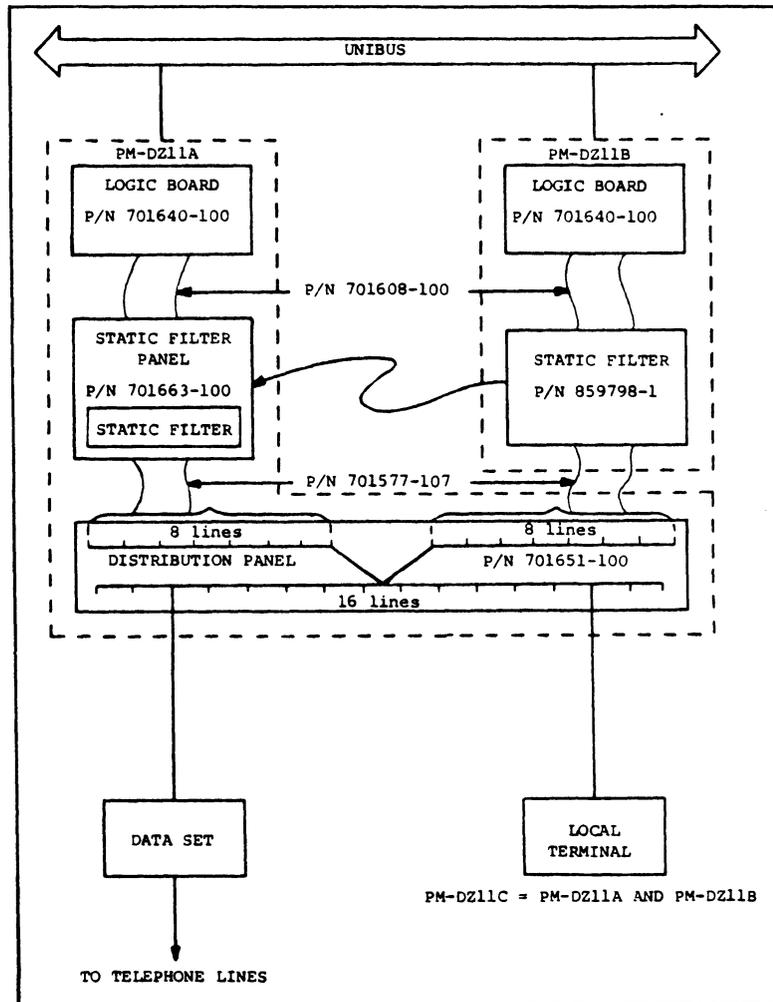
FIGURE 1-3: REQUIRED HARDWARE

1.5.2 Current Loop Models

The PM-DZ11C is an 8-line configuration with a 20mA current loop interface. It consists of a logic module, distribution panel, and interconnecting cables. The PM-DZ11D consists of additional logic module, filter, and cables which expand the PM-DZ11C to a 16-line configuration. The PM-DZ11F is a 16-line configuration and is a combination of the PM-DZ11C and PM-DZ11D. Figure 1-4 illustrates the required hardware for the 20mA model configurations.
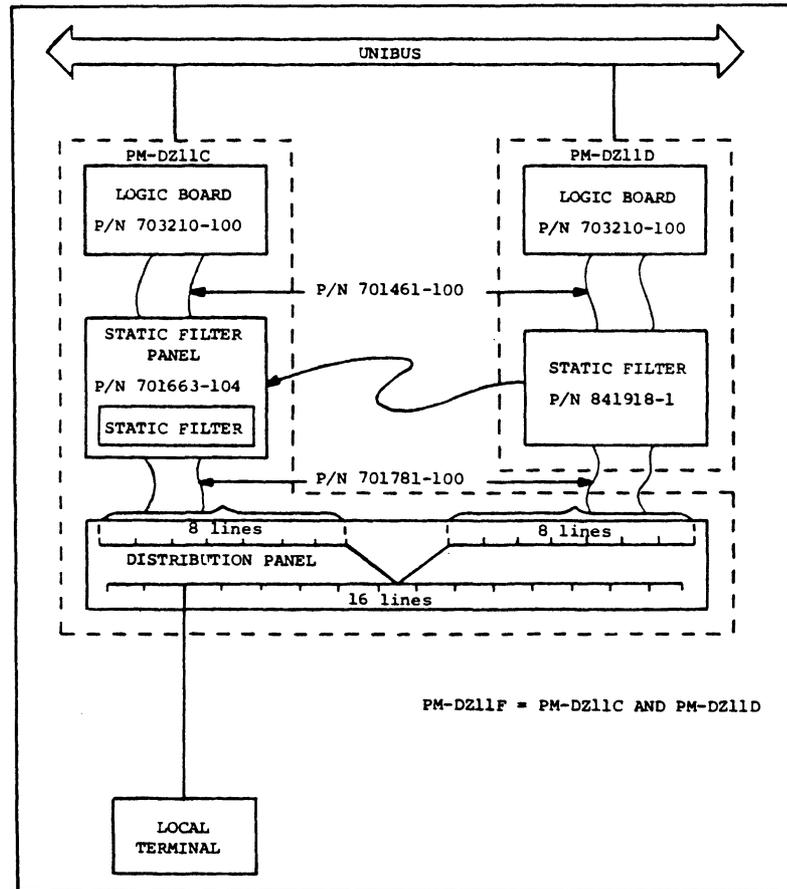
FIGURE 1-4: CURRENT LOOP MODEL HARDWARE

Maximum configuration allows 16 PM-DZ11E/F modules per Unibus for 128 lines of communication.*

*Unibus is a registered trademark of Digital Equipment Corporation.

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1.5.3 Hardware Descriptions

The distribution panel provides 16 communication lines using Cinch DB25P connectors, from two modules (8 lines per module), and is included with the PM-DZ11A/C and PM-DZ11E/F configurations. The PM-DZ11 logic module plugs into any hex SPC slot of the CPU or expansion chassis. The distribution panel requires no power and can be mounted in a standard 19-inch wide cabinet. The static filter panel is used to prevent problems caused by electrostatic discharge. A 50 conductor, flat, shielded cable, connects the logic module to the static filter. A second cable connects the static filter to the EIA distribution panel. The cables to modems and/or local devices are not provided with the basic PM-DZ11. See Table 2-5 for recommended cables for data set and/or local terminal interconnections.

1.5.4   Test Connectors

Two accessory test connectors are provided with each PM-DZ11A and PM-DZ11E. The PM-H325 test connector plugs into an EIA connector on the distribution panel or on the end of the modem cable to loop back data and modem signals on a single line. The PM-H3271 connected to the module with the interface cable staggers the data and modem lines as shown in Figure 1-5. The EIA test connectors are shown in Figures 1-6 and 1-7. Refer to Sections 2.3.4 and 2.3.5 for use of test connectors.

A priority level insert plugs into a socket on the logic module to establish interrupt levels on the Unibus.

FIGURE 1-5: TURNAROUND

*NOTE: PM-H325 test connector is testing line 5.
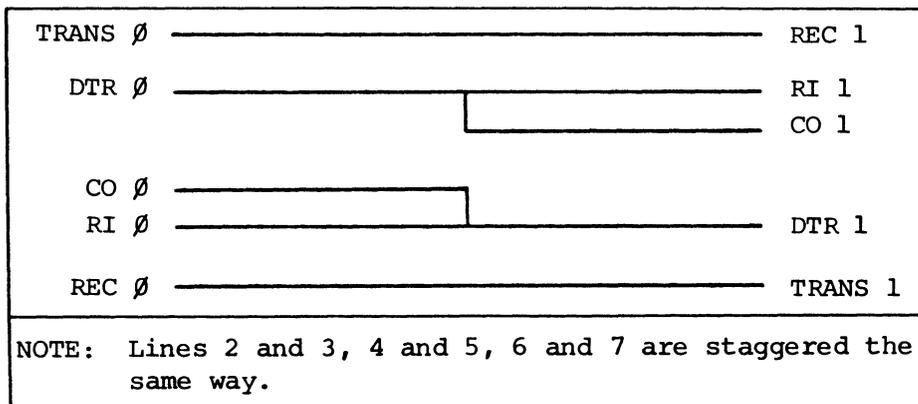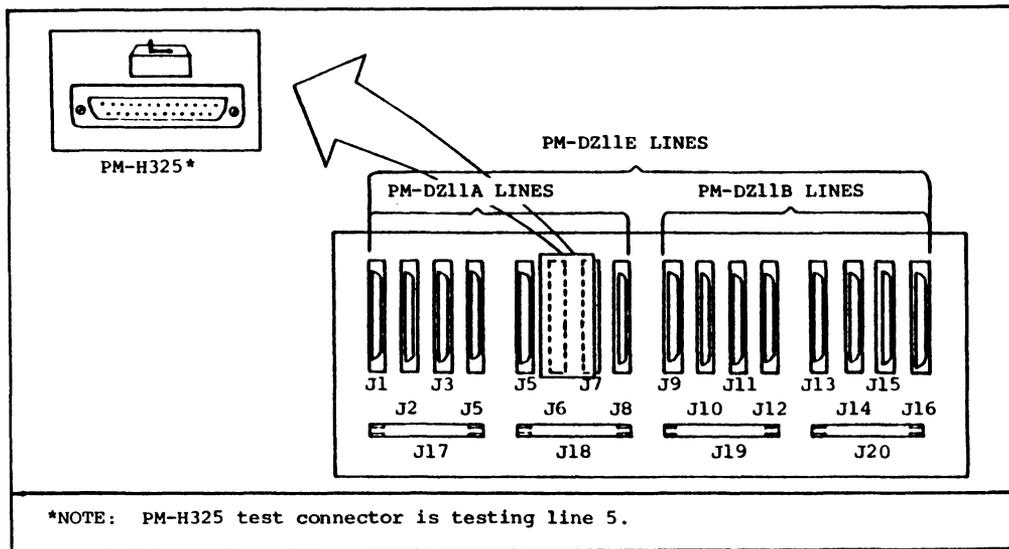
FIGURE 1-6:   PM-H325 TEST CONNECTOR (P/N 701587-100A)
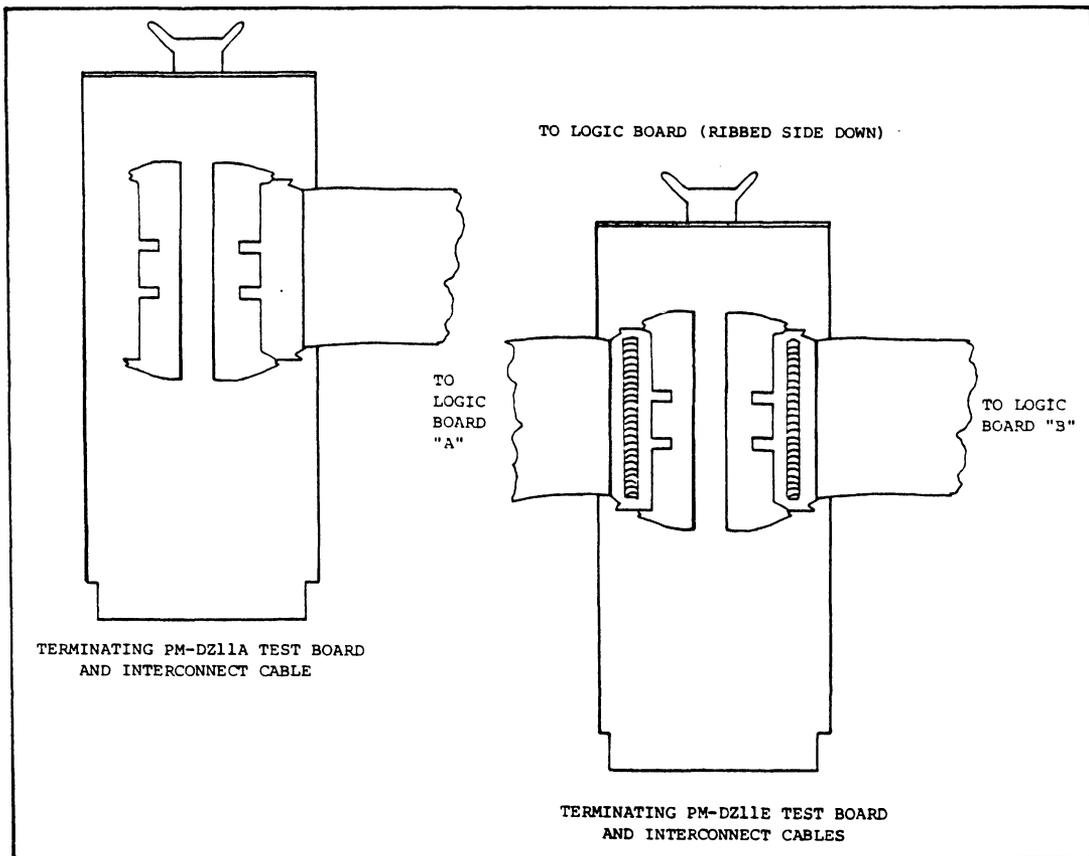
FIGURE 1-7:   PM-H3271 TEST CONNECTOR (P/N 701792-100X2)

The PM-DZ11C and PM-DZ11D also have a staggered turnaround
test connector (PM-3190) which is connected to the logic board
via the PM-BC08S cable. The PM-3190 staggers the data lines
as shown in Figure 1-5. Figure 1-8 illustrates the PM-3190
test connector. A priority level insert plugs into a socket
on the logic board to establish interrupt levels on the Unibus.

TERMINATING PM-DZ11C TEST BOARD
AND INTERCONNECT CABLE
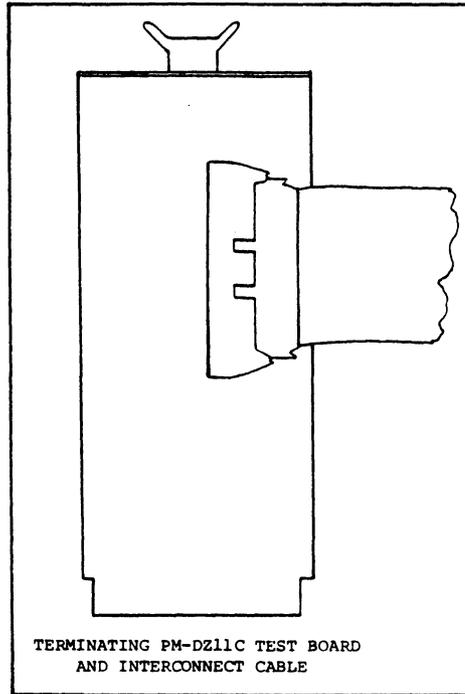
FIGURE 1-8: PM-3190 TEST CONNECTOR (P/N 703315)

1.6 FUNCTIONAL DESCRIPTION

The PM-DZ11 can be defined as three basic components: Unibus
interface, control logic, and line interface. These basic
structures are illustrated in a general block diagram shown
in Figure 1-9.

1.6.1 Unibus Interface

All transactions between the Unibus and the PM-DZ11 control
logic are related to the PDP-11 Unibus interface which performs
data handling, address recognition, and interrupt control. The
following explanations apply:

● Data Handling - The Unibus sends data to and from registers
                  in the control logic and provides the
                  voltage signals which determine transmission
                  or reception of data to and from the Unibus.

- Address Recognition - Preselected Unibus address recognition activates the proper load (write) and read signals which are used to route the in/out data to the desired locations.

- Interrupt Control - This function initiates and controls interrupt processing between the DZ11 and the CPU.
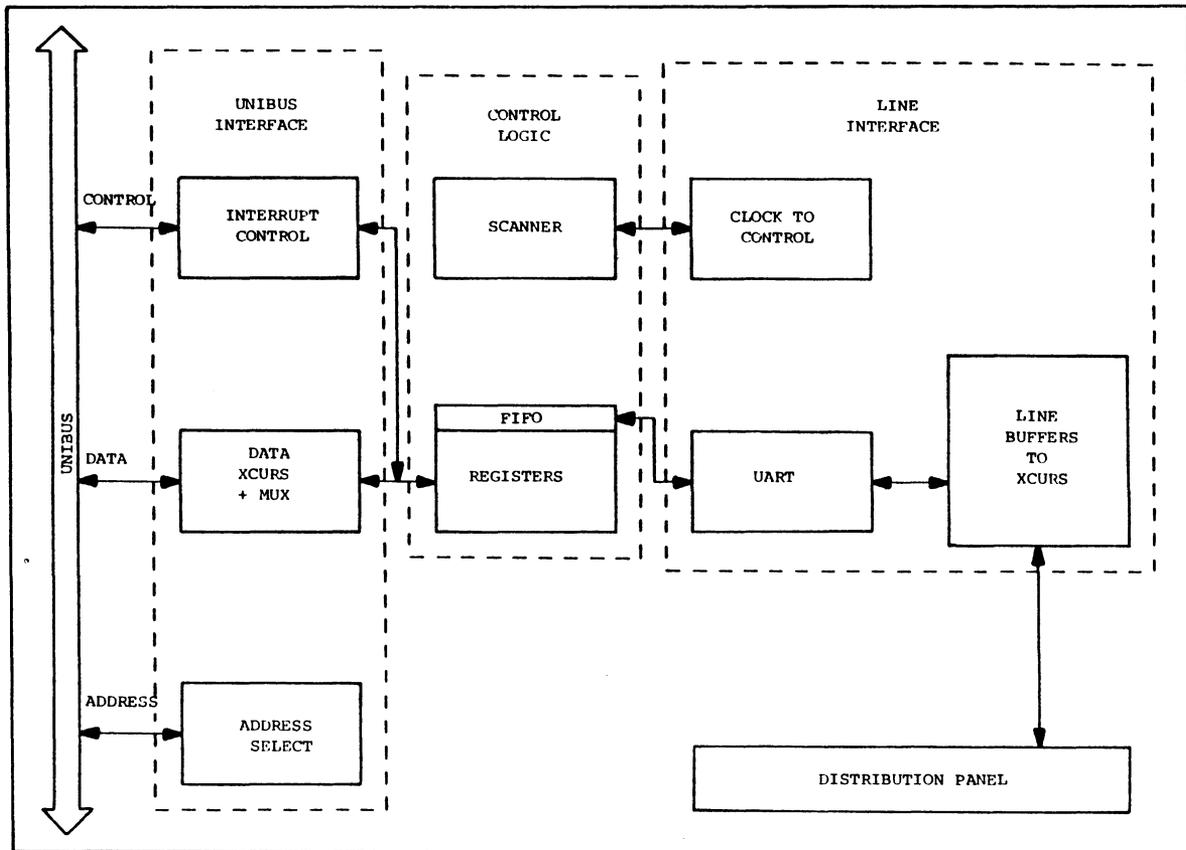
FIGURE 1-9: GENERAL FUNCTIONAL BLOCK DIAGRAM

1.6.2 Control Logic

Receiver and transmitter timing and control signals are generated by the control logic which consists of the scanner and the registers.

Information from the line interface and registers is continuously analyzed by the scanner which produces data flow to or from the appropriate line. The scanner consists of a clock and a four-phase clocking network.

Four device registers are utilized to provide six 16-bit
accessible registers. The device registers store input/output
data, monitor control signal conditions, and establish
operating status. The registers are accessible in bytes
and/or words and (depending on operation) can be read or
written, which extends the use of two of the device registers
to four independent registers.

1.6.3 Line Interface

The PM-DZ11 is located between the Unibus parallel data path
and serial data paths (terminals or telephone lines). The
line interface provides serial to parallel and parallel to
serial data format conversion. Conversions for each line in
the PM-DZ11 are performed by independent universal asynchronous
receiver/transmitter (UART) integrated circuits. The line
interface also allows the line receiver or driver to convert
TTL voltage levels in the PM-DZ11 to correspond to external
device input lines.

1.7 SPECIFICATIONS

1.7.1 Performance Parameters

Operating Mode:	Full-duplex
Data Format:	Asynchronous, serial by bit, 1 start and 1, 1 1/2 (5-level codes only) or 2 stop bits supplied by the hardware under program control
Character Size:	5, 6, 7 or 8 bits. Program selectable. (Does not include parity bit.)
Parity:	Even, odd or none. Program selectable.

Bit Polarities:	UNIBUS	INTERFACE	EIA OUT
Data Signal:	Low = 1	High = 1	Low = 1 = Mark
	High = $\emptyset$	Low = $\emptyset$	High = $\emptyset$ = Space
Control Signal:	Low = 1	High = 1	Low = OFF
	High = $\emptyset$	Low = $\emptyset$	High = ON

Order of Bit:	Transmission/reception low-order bit first
Baud Rates:	50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 4800, 7200, and 9600

Break: Can be generated and detected on each
                        line.

Throughput: 21,940 characters/second = (bits/second
                        x number of lines x direction)/
                        (bits/character)

                        Example: (9600 x 8 x 2)/7 = 21,940
                        characters/second

(NOTE)

        The theoretical maximum is 21,940.
        Actual throughput depends on other
        factors, such as type of CPU, system
        software, etc.

1.7.2 Outputs

● EIA   Each line provides voltage levels and
                        connector pins that conform to Electronic
                        Industries Association (EIA) standard
                        RS232C and CCITT recommendation V.24.
                        The leads supported by this option are:

Circuit AA (CCITT 101)   Pin 1   Protective Ground
Circuit AB (CCITT 102)   Pin 7   Signal Ground
Circuit BA (CCITT 103)   Pin 2   Transmitted Data
Circuit BB (CCITT 104)   Pin 3   Received Data
Circuit CD (CCITT 108.2)   Pin 20   Data Terminal Ready
Circuit CE (CCITT 125)   Pin 22   Ring Indicator
Circuit CF (CCITT 109)   Pin 8   Carrier

(NOTE)

        Signal ground and protective ground
        are connected.

        Circuit CA (CCITT 105 - Request to
        Send) is connected to circuit CD
        (DTR) through a jumper on the
        distribution panel. This allows
        control of the Request to Send line
        for full-duplex modem applications
        that use the RTS circuit.

● 20mA Current Loop

Each 20mA channel provides the current for the two pairs of signal lines (transmit and receive). The signals and associated pins are:

Receive +	Pin 1
Receive -	Pin 2
Transmit -	Pin 3
Transmit +	Pin 4

The 20mA line is connected to local terminals (no data set control). The line is active and drives only passive devices.

1.7.3 Inputs

The PDP-11 Unibus is the input for all PM-DZ11s. The PM-DZ11A or B and PM-DZ11C or D present one unit load to the Unibus. The PM-DZ11E and PM-DZ11F present two unit loads to the Unibus. Four AC loads per module are presented to the Unibus.

1.7.4 Power Requirements

The PM-DZ11A or B and PM-DZ11C or D require the following powers. The PM-DZ11E and PM-DZ11F require twice the following values.

	CURRENT	
VOLTAGE	TYPICAL	MAXIMUM
+ 5.0VDC	2.20 amps	2.50 amps
-15.0VDC	0.13 amps	0.15 amps
+15.0VDC	0.10 amps	0.13 amps

1.7.5 Environmental Requirements

Operating Temperature: 5° to 50°C (41° to 122°F). Reduce 1.8°C/1000 meters (1.0°F/1000 feet) for operation at altitudes above sea level.

Relative Humidity: 10% to 95% with maximum wet bulb of 32°C (90°F) and a minimum dewpoint of 2°C (36°F).

Cooling:

PM-DZ11A and B	Air flow 1.416 l/sec. (3 cu.ft./min.)
PM-DZ11E	Air flow 2.832 l/sec. (6 cu.ft./min.)

Heat Dissipation:

PM-DZ11A and B	3.99 g.cal./sec. (57 Btu/hr.)
PM-DZ11E	7.98 g.cal./sec. (114 Btu/hr.)

1.7.6 Distortion

"Space to Mark" and "Mark to Space" in a received character	Maximum 40%
Speed distortion in a received character for 2000 baud	Maximum 3.8%
All other baud rates	Maximum 4%
Speed distortion from the transmitter for 2000 baud	Maximum 2.2%
All other baud rates	Less than 2%

1.7.7 Interrupts

RDONE - Occurs each time a character appears at the FIFO output.

SA   - FIFO alarm. Occurs after 16 characters enter the FIFO. Rearmed by reading the FIFO. This interrupt disables the RDONE interrupt.

TRDY   - Occurs when the scanner finds a line ready to transmit on.

There are no modem interrupts. Normally, a level 5 priority plug is supplied. The interface level can be modified to level 4, 6 or 7 by using the proper priority plug.

1.7.8 Line Speed

The baud rate for a line (transmitter and receiver) is program selectable. Also, the receiver for each line can be individually turned on or off under program control. See Section 1.7.1 for available baud rates.

Section 2

Installation and Operation

2.1 GENERAL INFORMATION

This section provides information for the installation and operation of the PM-DZ11 multiplexed asynchronous serial line interface, with 701640 assembly revision D and above.

2.2 UNPACKING AND INSPECTION

The PM-DZ11 logic module(s), distribution panel, and cable(s) are shipped in a special packing carton designed to keep the equipment from vibrating and to give it maximum protection during shipment. The packing carton should be retained in the event the memory requires reshipment.

To unpack the PM-DZ11, remove any packing material and visually inspect for damage. Inventory of items that are supplied are noted in Table 2-1 for EIA models and Table 2-2 for 20mA current loop models.

PART NUMBER	DESCRIPTION	QUANTITY PM-DZ11 MODELS			FIGURE 2-1 AND 2-2 REFERENCE
		A	B	E	
701640-100	Logic Board Assembly	1	1	2	①
701651-100	Distribution Panel PM-H317E	1		1	②
701663-100	Static Filter Panel	1			③
701663-101	Static Filter Panel			1	④
859798-1	Static Filter		1		N/A
701608-100	Cable Assembly PM-BC05W	1	1	2	⑤
701694-100A	Cable Assembly PM-BC06L-0J	1	1	2	⑥
701588-100	Test Connector PM-H325	1		1	N/A
701792-100	Test Connector PM-H3271	1		1	N/A
701517-001	Bracket	2		2	N/A
701551-100	Hardware Pack	1		1	N/A
ZJ223-RB	Software Pack	1		1	N/A
MA701885	Manual PM-DZ11	1	1	1	N/A
MS51957-30	Mounting Hardware		2		N/A
MS35333-37	Mounting Hardware		2		N/A

TABLE 2-1: ITEMS SUPPLIED PER EIA CONFIGURATIONS

PART NUMBER	DESCRIPTION	QUANTITY PM-DZ11 MODELS			FIGURE 2-1 AND 2-2 REFERENCE
		C	D	E	
703210-100	Logic Board Assembly	1	1	2	①
702381-100	Distribution Panel PM-H317F	1		1	②
701663-104	Static Filter Panel	1			③
701663-105	Static Filter Panel			1	④
841918-1	Static Filter		1		N/A
701461-100	Cable Assembly 40-pin PM-BC08S	1	1	2	⑤
701781-100	Cable Assembly PM-BC06K-0J	1	1	2	⑥
703315-100	Test Connector PM-H3190	1			N/A
701517-001	Bracket	2		2	N/A
701551-100	Hardware Pack	1		1	N/A
ZJ223-RB	Software Pack	1		1	N/A
MA701885	PM-DZ11 Manual	1		1	N/A
MS51957-30	Mounting Hardware		2		N/A
MS35333-37	Mounting Hardware		2		N/A

TABLE 2-2: ITEMS SUPPLIED PER CURRENT
LOOP CONFIGURATIONS

2.3 INSTALLATION

The procedures described below should be followed for
equipment installation.

Ensure that the jumpers on the distribution panel are in
place. These jumpers anticipate future use of the PM-DZ11
with modems other than the 103 CCITT; however, two of the
jumpers are now functional. The jumper between pins H and J
connects DTR to pin 4 or Request to Send. This allows the
PM-DZ11 to assert both DTR and RTS when using a modem which
requires control of RTS. Pin K jumper is also connected to
the DTR lead for use in modems that implement the Force Busy
function. This jumper should normally be out, unless the
modem has the Force Busy feature, and the system software is
implemented to control it.

2.3.1 PM-DZ11A or PM-DZ11C Panel Installation

Refer to Figure 2-1.

● Insert the short mirror cable, PM-BC06L-0J (EIA) or
  PM-BC06K-0J (20mA), into the static filter.

● Using the supplied hardware, mount the filter panel and
  distribution panel in a standard 19-inch cabinet.

● Ensure that the filter is aligned with J18 (EIA) or
  J2 (20mA) on the distribution panel.

● Insert the remaining end of the mirror cable into J18 (EIA)
  or J1 (20mA) as shown in Figure 2-1.

SMOOTH SIDE UP: This end of cable should not be strain relieved.

RIBBED SIDE UP

*Arrows may not agree between connectors and jacks. Install cables with arrows in positions shown here.
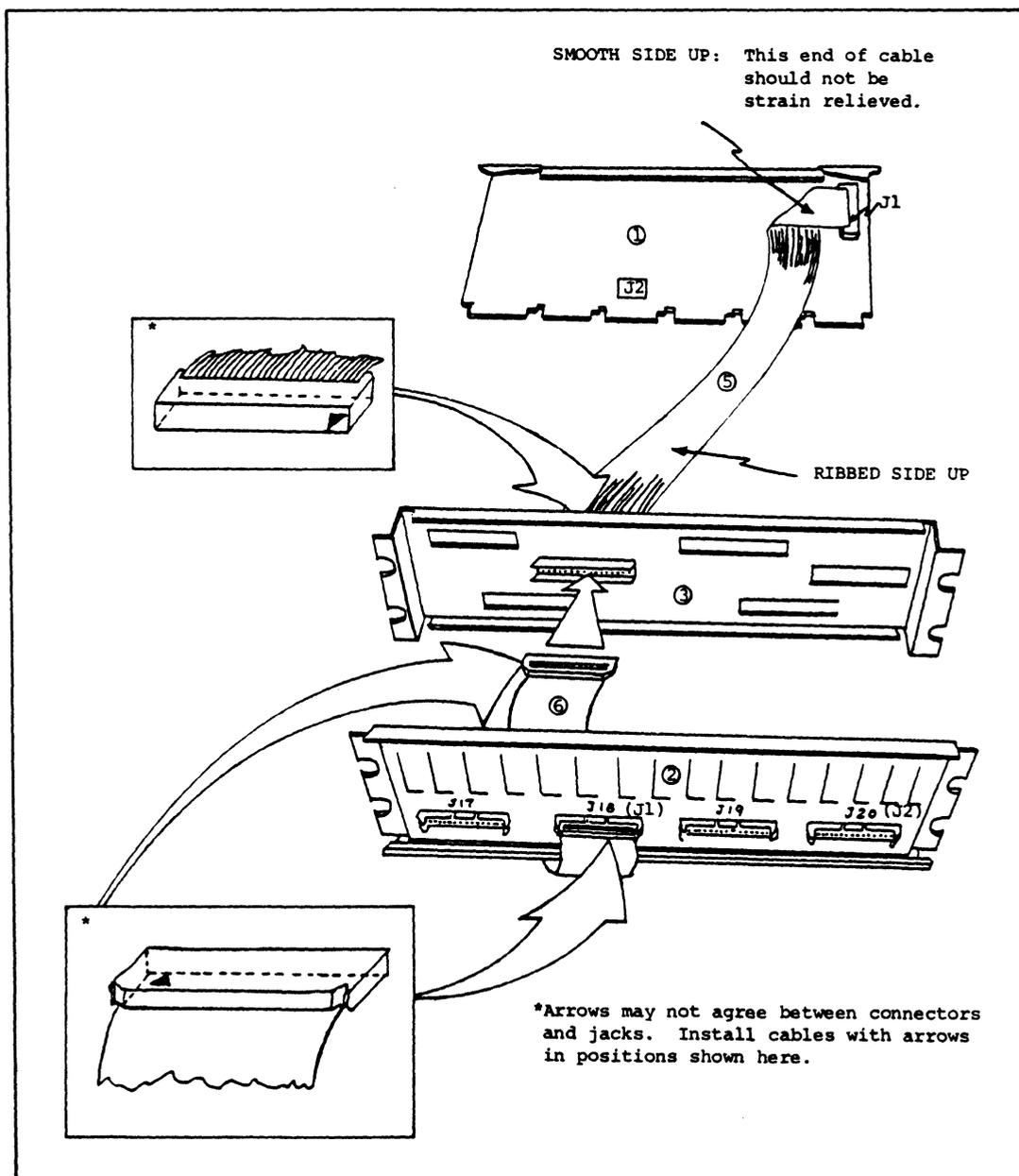
FIGURE 2-1: PM-DZ11A AND B OR PM-DZ11C AND D INSTALLATION

2.3.2   PM-DZ11E or PM-DZ11F Panel Installation

Refer to Figure 2-2.

● Insert two short mirror cables, PM-BC06L-0J (EIA) or PM-BC06K-0J (20mA), into the static filters.

● Using the supplied hardware, mount the filter panel and distribution panel in a standard 19-inch cabinet.

● Ensure that filter A and filter B are aligned with J18 (EIA) or J2 (20mA) and J20 (EIA) or J1 (20mA), respectively.

● Insert the remaining end of the mirror cables into J18 (J2) and J20 (J1) as shown in Figure 2-2.

```
( NOTE )
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Pin alignment arrows may not match on cable and board assignments. Note Figure 2-2.

2.3.3   PM-DZ11B or PM-DZ11D Filter Installation

Refer to Figure 2-2.

1. Ensure that the existing PM-DZ11A or PM-DZ11C is not in operation.

2. Disconnect the existing mirror cable from J18 (EIA) or J2 (20mA), or J20 (EIA) or J1 (20mA).

3. Unmount the distribution and static filter panels from the cabinet.

4. Install the additional static filter into the panel with the supplied hardware.

5. Connect the new mirror cable, PM-BC06L-0J (EIA) or PM-BC06K-0J (20mA), to the new filter (the existing filter should retain the existing mirror cable).

6. Remount the filter panel and distribution panel in the cabinet.

SMOOTH SIDE UP: This end of cable should not be strain relieved.

RIBBED SIDE UP

*( ) = 20mA

*Arrows may not agree between connectors and jacks. Install cables with arrows in positions shown here.
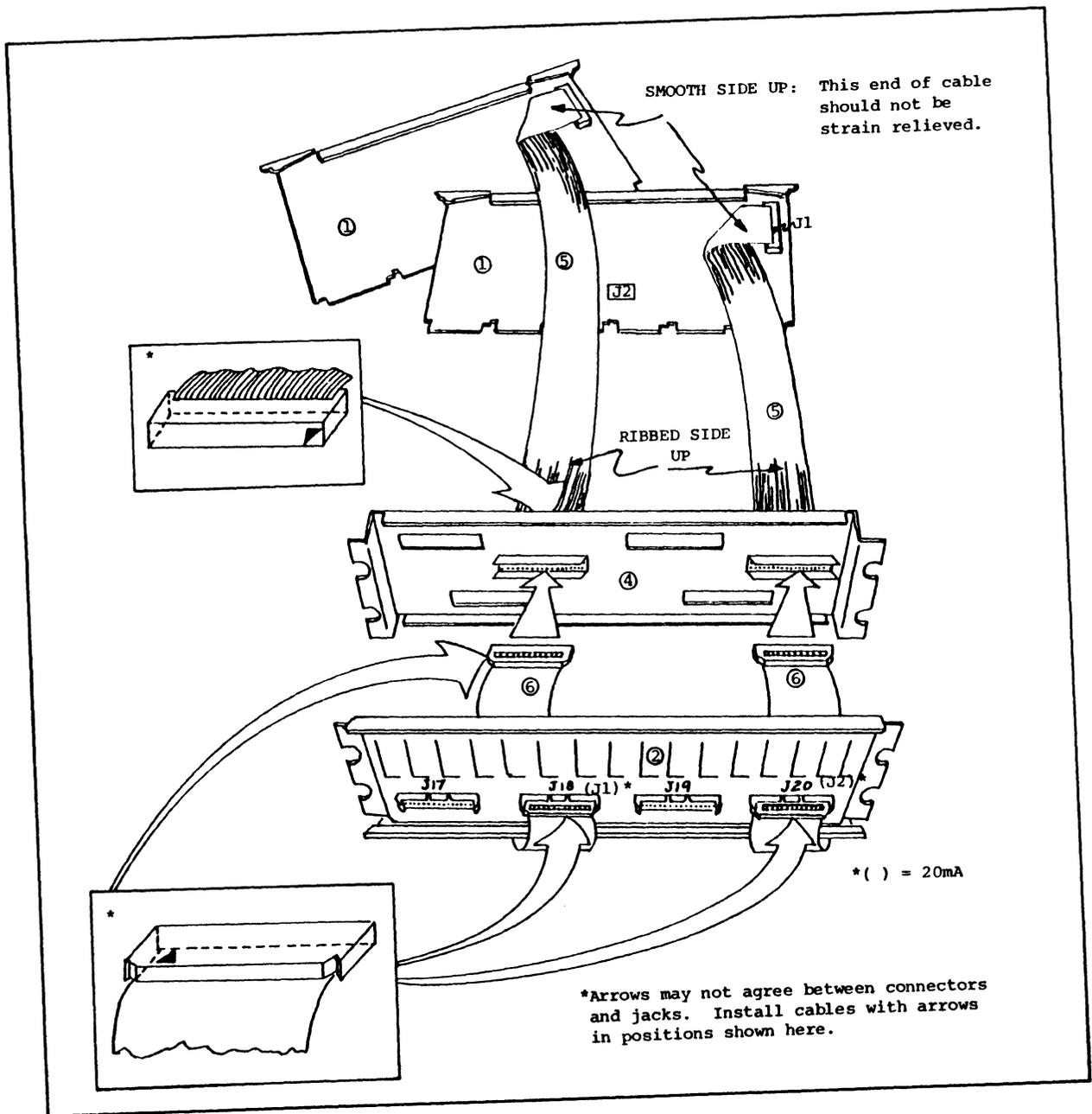
FIGURE 2-2: PM-DZ11E OR PM-DZ11F INSTALLATION

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7. Connect the two mirror cables to their respective jacks, J18 (EIA) or J2 (20mA) and J20 (EIA) or J1 (20mA), on the distribution panel.

(NOTE)

Pin alignment arrows may not match on cable and board assignments. Note Figure 2-2.

2.3.4 Logic Board Assembly Installation

The procedure described below should be followed for the logic board installation.

1. Ensure that the priority insert is properly seated in socket J2 on the module(s).

2. Select device address utilizing Table 2-3 and Section 3-2.

3. Select vector address utilizing Table 2-4 and Section 3-2.

4. Insert the module(s) into an SPC slot. Connect the flat shielded PM-BC05W-15 (EIA) or PM-BC08S (20mA) cable smooth side up to J1 on the module(s). Use the end of the cable that does not have the strain relief. If both ends have strain relief, remove it from one end. Utilizing the alignment arrows, connect the other end of the cable to the test connector as noted in Figure 1-7.

(CAUTION)

Install and remove modules carefully to avoid snagging components on the card guides and accidentally changing switch settings.

2.3.5 Diagnostic Testing

1. Run the PM-DZ11 diagnostic in staggered mode to verify module operation. Refer to MAINDEC-11 DZDZA. Run at least two passes without error.

2. Remove the cable(s) from the test connector and connect them to the static filter socket(s) on the back of the distribution panel ribbed side up.

	SW2 POSITIONS (20mA) - PM-DZ11C, D, F									
	10	9	8	7	6	5	4	3	2	1
	SW1 POSITIONS (EIA) - PM-DZ11A, B, E									
	1	3	2	10	9	8	6	4	7	5
	ADDRESS LINES									
	12	11	10	9	8	7	6	5	4	3
160000										
160010										0*
160020									0	
160030									0	0
160040								0		
160050								0		0
160060								0	0	
160070								0	0	0
160100							0			
160110							0			0
160560					0		0	0	0	
160570					0		0	0	0	0
160600					0	0				
160610					0	0				0
160620					0	0			0	
160630					0	0			0	0
160640					0	0		0		
160650					0	0		0		0
160660					0	0		0	0	
160670					0	0		0	0	0
161220				0		0			0	
161230				0		0			0	0
161240				0		0		0		
161250				0		0		0		0
161260				0		0		0	0	
161270				0		0		0	0	0
161300				0		0	0			
161310				0		0	0			0
161320				0		0	0		0	
161330				0		0	0		0	0
162100			0				0			
162110			0				0			0
162120			0				0		0	
162130			0				0		0	0
162140			0				0	0		
163730			0	0	0	0	0		0	0
163740			0	0	0	0	0	0		
163750			0	0	0	0	0	0		0
163760			0	0	0	0	0	0	0	
163770			0	0	0	0	0	0	0	0

*NOTE: 0 = Switch ON
        Blank = Switch OFF

TABLE 2-3: ADDRESS SELECTION CHART

PM-DZ11C, D, F 20mA (SW1)						
PM-DZ11A, B, E EIA (SW2)						
	1	2	3	4	5	6
	VECTOR LINES					
	8	7	6	5	4	3
300	O*			O	O	O
310	O			O	O	
320	O			O		O
330	O			O		
340	O				O	O
350	O				O	
360	O					O
370	O					
400		O	O	O	O	O
410		O	O	O	O	
570		O				
600			O	O	O	O
610			O	O	O	
620			O	O		O
630			O	O		
640			O		O	O
650			O		O	
660			O			O
670			O			
700				O	O	O
730				O		
740					O	O
750					O	
760						O
770						

*NOTE: O = Switch ON
Blank = Switch OFF

TABLE 2-4: VECTOR SELECTION CHART

3. EIA OPERATION ONLY. Omit this step for 20mA models.
Connect the PM-H325 test connector on the first line and
run the cable test diagnostics. The test connector may
be installed on the distribution panel or the end of an
EIA cable. Repeat this step for each line.

(NOTE)

Ensure that no devices are connected to
any of the remaining lines. Remove
PM-H325 when cable testing is completed.

4. Run DEC/X11 system exerciser to verify the absence of
Unibus interference with other system devices.

5. The PM-DZ11 is now ready for connection to external
equipment. If the connection is to a local terminal, a
null modem cable must be used. See Table 2-5 for

available cables. These cables are <u>not</u> components of the
standard PM-DZ11 and must be ordered separately. Further
description of these cables may be found in the Plessey
Product Summary, December 1979.

6. When possible, run the echo test diagnostic (subtest of main
   diagnostic) to verify the cable connections to terminal
   equipment.

DESCRIPTION	LENGTH	MODEL	PART NUMBER
Shielded Null Modem Cables*	2 ft 25 ft 50 ft	PM-BC03M-02 PM-BC03M-25 PM-BC03M-50	701606-100 701606-101 701606-102
Unshielded Null Modem Cables*	2 ft 25 ft 50 ft	PM-BC03P-02 PM-BC03P-25 PM-BC03P-50	701582-100 701582-101 701582-102
Shielded Null Modem Cables**	2 ft 25 ft 50 ft	PM-BC00B-02 PM-BC00B-25 PM-BC00B-50	701602-100 701602-101 701602-102
Modem Cables**	25 ft 50 ft	PM-BC05D-25 PM-BC05D-50	701603-100 701603-101
Current Loop Cables***	25 ft	PM-BC04R-100	701886-100

*These null modem cables have DB-25S sockets at both ends. They are
configured for use with DEC terminals having plug inputs.

**These null modem cables have a DB-25P plug on one end and a DB-25S
socket on the other end. They are configured for use with most
terminals other than DEC models.

***This cable has an 8-pin Mate 'N' Lock connector compatible with
those utilized on DEC terminals.

TABLE 2-5:   CABLES USED FOR CONNECTION
TO LOCAL TERMINALS

.

Section 3

Programming

3.1 INTRODUCTION

This section provides information to aid in programming the
PM-DZ11. A description of each register, including program
limits and bit assignments, is presented to facilitate
programming and maintenance.

3.2 ADDRESS AND VECTOR SPACE ASSIGNMENTS

PM-DZ11 device and vector addresses are selected from floating
device and vector address spaces. The device floating address
space is 160010_8 to 163776_8 and the vector space is 300_8 to
776_8.

Floating device and vector addresses enable the PM-DZ11 to be
assigned the lowest space in a defined sequence of addressable
options. The floating address space follows the sequence
DJ11, DH11, DQ11, DU11, DUP11, LK11 and DMC11. The floating
vector space follows the sequence DC11, KL11/DL11A, -B, DP11,
DM11-A, DN11, DM11-BB and other modem vectors, such as DR11-A,
DR11-C, PA611 reader or punch, DT11, DX11, DL11-C, -D, -E,
DJ11, DH11, GT40, LPS11, DQ11, KW11-W, DU11, DUP11, DV11,
LK11-A, DWUN and DMC11. The PM-DZ11 vector and device
addresses must be assigned to follow the vector and device
address space of the other options.

Device Address/Vector Assignment Examples. Given that the
floating address space is 160000_8 to 163776_8, vector space is
300_8 to 776_8, and device address/vector spaces are as defined
in Table 3-1. The following examples illustrate three
possibilities for the determination of the PM-DZ11's
vector/address assignment.

| ADDRESS/VECTOR | DEVICE SPACE SEQUENCE | |
STATUS	ADDRESS	VECTOR
Highest		DC11
		KL11/DL11-A, -B
		DP11
		DM11-A
		DN11
		DM11-BB
		DR11-A, -C
		PA611 Reader/Punch
		DT11
		DX11
		DL11-C, -D, -E
	DJ11	DJ11
	DH11	DH11
		GT40
		LPS11
	DQ11	DQ11
		KW11-W
	DU11	DU11
	DUP11	DUP11
		DV11
	LK11	LK11A
		DWUN
	DMC11	DMC11
Lowest	PM-DZ11	PM-DZ11

TABLE 3-1: DEVICE ADDRESS/VECTOR SEQUENCES

Example 1: One PM-DZ11 and no options

OPTION	DEVICE ADDRESS	NUMBER OF DEVICES	VECTOR ADDRESS	COMMENTS
DJ11	160010	None	N/A	
DH11	160020	None	N/A	
DQ11	160030	None	N/A	
DU11	160040	None	N/A	
DUP11	160050	None	N/A	
LK11	160060	None	N/A	
DMC11	160070	None	N/A	
PM-DZ11	160100	One	300	
PM-DZ11	160110	None		No more PM-DZ11s

Example 2: One DJll, one GT40, one KW11-W, and one PM-DZll

OPTION	DEVICE ADDRESS	NUMBER OF DEVICES	VECTOR ADDRESS	COMMENTS
DJll	160010	One	300	
DJll	160020	None	N/A	No more DJlls
DHll	160030	None	N/A	
GT40		One	310	GT40 address is not in the floating device address space
KW11-W		One	320	KW11-W device address is not in the floating address space
DQll	160040	None	N/A	
DUll	160050	None	N/A	
DUP11	160060	None	N/A	
LKll	160070	None	N/A	
DMCll	160100	None	N/A	
PM-DZll	160110	One	330	
PM-DZll	160120	None	N/A	No more PM-DZlls

Example 3: One DJll, one DHll, one KW11-W, one LKll, one DMCll, and two DZlls

| OPTION	DEVICE ADDRESS	NUMBER OF DEVICES	VECTOR ADDRESS	COMMENTS
DJll	160010	One	300	
DJll	160020	None	N/A	No more DJlls
DHll	160040	One	310	DHll must start on an address space that is a multiple of 20
DHll	160050	None	N/A	No more DHlls
DQll	160060	None	N/A	
KW11-W		One	320	KW11-W address is not in the floating device address space
DUll	160070	None	N/A	
DUP11	160100	None	N/A	
LKll-A	160110	One	330	
LKll-A	160120	None	N/A	No more LKlls
DMCll	160130	One	340	
DMCll	160140	None	N/A	No more DMClls
PM-DZll	160150	One	350	
PM-DZll	160160	One	360	
PM-DZll	160170	None	N/A	No more PM-DZlls

3.3 REGISTER BIT ASSIGNMENTS

The PM-DZ11 consists of four discrete device registers (R∅, R2, R4, and R6) which are expanded to provide six unique registers.

- R∅   Control Status   CSR   (Read/Write)

- R2   Receiver Buffer   RBUF   (Read Only)
         Line Parameter   LPR   (Write Only)

- R4   Transmit Control   TCR   (Read/Write)

- R6   Transmit Data   TDR   (Write Only)
         Modem Status   MSR   (Read Only)

The expansion to six registers is accomplished by assigning a read only or write only status to R2 and R6. As a result, PDP-11 processor instructions that perform a read-modify-write (DATIP) bus cycle, cannot be utilized with R2 and R6. Also, R2 allows only word instructions, but byte or word instructions may be used with R6. R∅ and R4 have no programming restraints. For all registers, read only bits are not affected by a write operation, and a read operation results in binary ∅ for write only or "not used" bits.

3.3.1 Control and Status Register (CSR) - R∅

The control and status register has no programming restraints. Write only and not used bits are read as zero by the Unibus. Read only bits are not affected by write attempts.


```
                      15  14  13  12  11  10  9   8   7   6   5   4   3   2   1   0
16XXX0               [  |   |   |   |///|   |   |   |   |   |   |   |///|///|///]

Transmitter Ready
Transmitter Interrupt
    Enable
FIFO Alarm
FIFO Alarm Enable
Transmitter Line Enable
Receiver Done
Receiver Interrupt Enable
Master Scan Enable
Clear
Maintenance
```

BIT	DESCRIPTION

15   <u>Transmitter Ready</u>. Set by PM-DZll when a line is found that has its transmit buffer empty and the LINE ENB bit corresponding to that line is set. Cleared by CLR, BUS INIT, and by loading the TBUF. Read only.

14   <u>Transmit Interrupt Enable</u>. If Transmitter Ready is set, this bit allows an interrupt when set. Read/Write.

13   <u>FIFO Alarm</u>. Set by PM-DZll after 16 characters enter FIFO. If bit Ø6 is set, it causes an interrupt. Cleared by CLR, BUS INIT, and reading RBUF. FIFO must be emptied when FIFO flag occurs as flag will not set again until another 16 characters enter FIFO. Read only.

12   <u>FIFO Alarm Enable</u>. If bit Ø6 is set, FAE allows bit 13 to cause interrupt after 16 characters enter the FIFO. If bit Ø6 is not set, FIFO alarm can be used as a flag. This bit can prevent Receiver Done from causing interrupts. Cleared by CLR and BUS INIT.

11   Not used.

Ø8-1Ø   <u>Transmit Line A through C</u>. These bits indicate the line that is ready to transmit a character when bit 15 is set. When the character is loaded into the transmit buffer, bit 15 clears. If another line is ready, bit 15 sets again. After a CLR or BUS INIT, these three bits return to line Ø. Only when bit 15 is true are these bits meaningful. Read only.

Ø7   <u>Receiver Done</u>. If bit Ø6 is set and bit 12 is clear, this bit generates RCV INT and clears when the receive buffer is read. Resets when another word reaches output of FIFO. Receiver Done can be used as a flag to indicate the FIFO contains a character if bit Ø6 is cleared.

Ø6   <u>Receiver Interrupt Enable</u>. Enables receiver interrupts. Cleared by CLR and BUS INIT. Read/Write.

Ø5   <u>Master Scan Enable</u>. Activates scanner to enable the receiver transmitter and FIFO. Cleared by CLR and BUS INIT. Read/Write.


BIT	DESCRIPTION

Ø4   **Clear.** Generates a reset which clears the receiver FIFO, all UARTs, and CSR. The CSR and line parameters must be reset after CLR is issued. Bits ØØ through 14 of RBUF and modem control registers are not affected. CLR = 1 indicates CLR in progress. Read/Write.

Ø3   **Maintenance.** Serial output data from transmitter is looped back as input data to the receiver when this bit is set. This permits running of the diagnostic without disturbing any connectors. Cleared by BUS INIT and CLR. Read/Write.

ØØ-Ø2   Not used.

3.3.2 Receive Buffer Register (RBUF) - R2

The Receive Buffer register is the read-only portion of register R2. Programming restraints are:

● Byte, TST, or BIT instructions cannot be used.

● CSR bit Ø5 (Master Scan Enable) must be set or else bits ØØ through 14 of the RBUF are invalid regardless of the status of Data Valid (bit 15) and the FIFO held empty. Each reading advances the FIFO and presents the next character to the program. Although they do not go to zero, bits ØØ through 14 become invalid and the FIFO is emptied after a CLR or BUS INIT. Data Valid (bit 15) goes to zero.

16XXX2 (Read Only)

Data Valid
Overrun
Framing Error
Parity Error
Line Number
Receiver Character
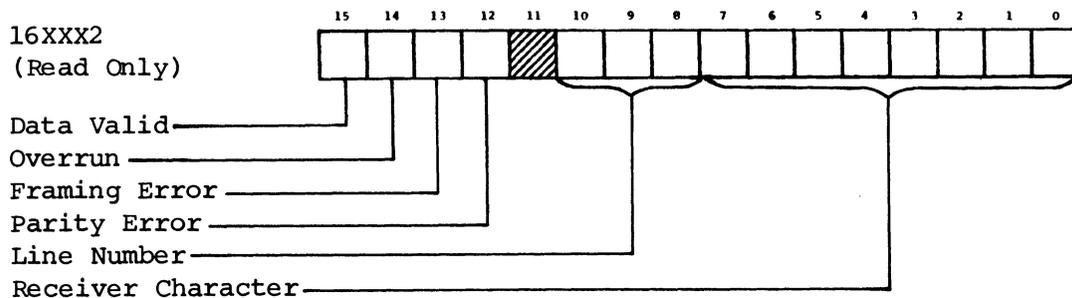
BIT	DESCRIPTION

15   <u>Data Valid</u>. Indicates character read from FIFO (RBUF) is valid. Until the data valid bit = ∅, indicating an invalid character and empty FIFO, the RBUF is read. Cleared by CLR and BUS INIT.

14   <u>Overrun</u>. Receiver buffer overflow indicated. When overflow occurs a received character is replaced by another received character before storage in the FIFO. One character is lost; the received character, put in the FIFO, is valid.

13   <u>Framing Error</u>. Indicates improper framing (stop bit not a mark) of received character; used for break detection also.

12   <u>Parity Error</u>. Does not appear in the RBUF word and is generated by the PM-DZll. Indicates the received bit had a parity error when set.

11   Not used.

∅8-1∅   <u>Line Number</u>. Present line number on which the character is received.

∅∅-∅7   <u>Received Character</u>. These bits contain the received character. High-order bits are forced to zero when selected code level is less than 8 bits wide.

3.3.3   Line Parameter Register (LPR) - R2

The line parameter register is the write only part of register R2. Line parameters for each line must be reloaded after a CLR (bit ∅4 of CSR) or BUS INIT operation. Programming constraints consist of non-allowable byte operations, BIS or BIC instructions and the write only status of the LPR.

16XXX2
(Write Only)

Receiver On
Speed Select
Odd Parity
Parity Enable
Stop Code
Character Length
Line Number
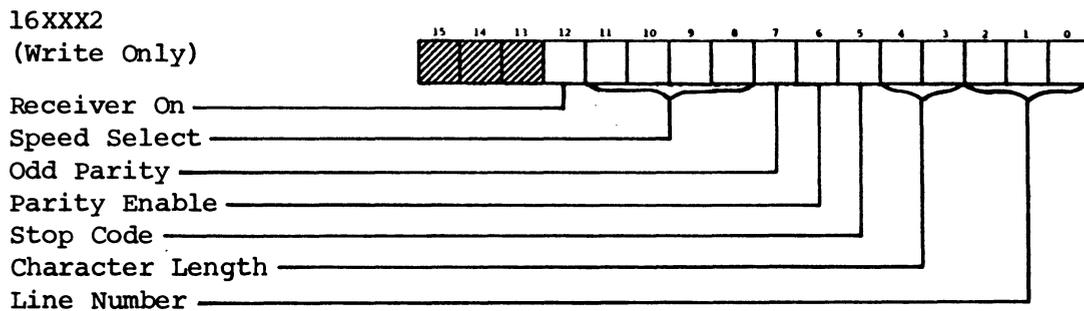
BIT	DESCRIPTION

15-13   Not used.

12   Receiver On. This bit activates the receiver clock and must be set when loading parameters. CLR or BUS INIT turns the receiver clock off.

Ø8-11   Speed Select. These bits select the baud rates as determined by the TRAN and RCV speed for the line selected by bits ØØ-Ø2. See Table 3-2 for applicable baud rates.

BITS				BAUD RATE
11	1Ø	Ø9	Ø8	
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	Not used

TABLE 3-2: BAUD RATE SELECTION CHART

Ø7   Parity. This bit determines whether it is even or odd parity (Ø = even, 1 = odd). Bit Ø6 must be set for this bit to be effective.

Ø6   Parity Enable. This bit enables parity option. If no parity is desired, this bit should not be set.

Ø5   Stop Code. Sets stop code length (Ø = 1 unit stop, 1 = 2 unit stop or 1.5 unit stop if a 5-level code is employed).

Ø3-Ø4   Character Length. These bits determine the character length for the selected line.

BIT Ø3	BIT Ø4	CHARACTER LENGTH
Ø	Ø	5 bits
Ø	1	6 bits
1	Ø	7 bits
1	1	8 bits

ØØ-Ø2   Line Number. These bits determine the line for parameter loading.

3.3.4 Transmit Control Register (TCR) - R4

The transmit control register is a read/write register. For
EIA operation, the high byte contains DTR for each line and
is cleared by BUS INIT only, not CLR. For current loop
operation, the high byte is unused and read as zero. The low
byte has a line enable bit for each line. A set bit allows
transmission on the corresponding line. The low byte is
cleared by CLR and BUS INIT.

16XXX4

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
┌──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┐
│  │  │  │  │  │  │  │  │  │  │  │  │  │  │  │  │
└──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┘
```

Unused - (20mA Version)
Data Terminal Ready - (EIA
    Version)
Transmit Enable
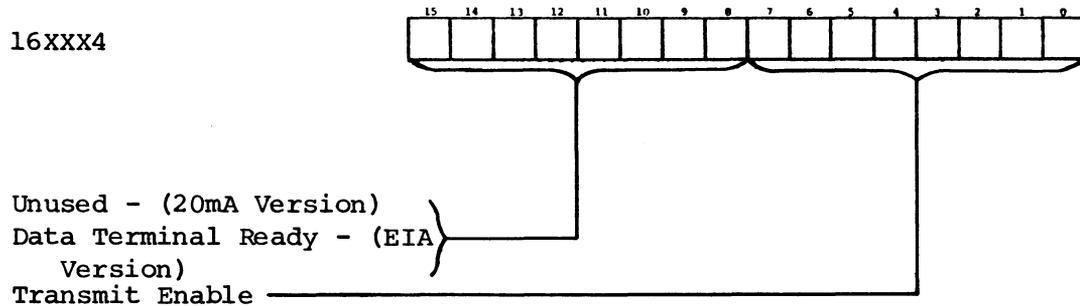
3.3.5 Modem Status Register (MSR) - R6

The modem status register is used for EIA operation only and
is the read only part of register R6. The low byte of the
modem status register monitors the state of each line's ring
indicator (RI) lead. The high byte monitors the state of
each line's carrier (CO) lead. Programming considerations
should include the format shown below, the read only status,
and the fact that CLR and BUS INIT have no effect on this
register.

16XXX6
(Read Only)

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
┌──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──┐
│  │  │  │  │  │  │  │  │  │  │  │  │  │  │  │  │
└──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┴──┘
```

Carrier

Ring
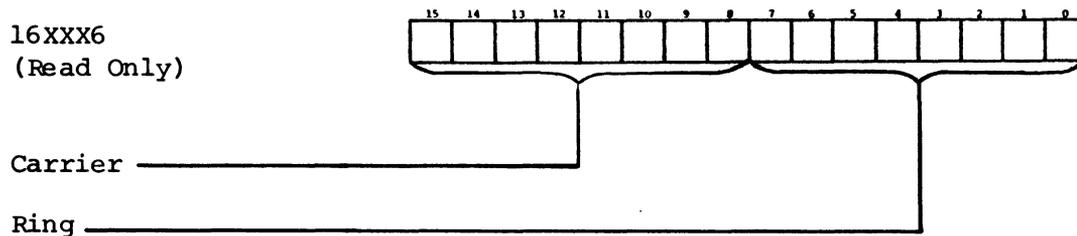
3.3.6 Transmit Data Register (TDR) - R6

The transmit data register is the write only part of register
R6. The low byte of TDR is the transmit buffer (TBUF) and
stores the character that is to be transmitted. The high byte
is the break register with each line controlled by an
individual bit ($07-00$). When a break is set, the associated
line sends zeros immediately and continuously. Programming
considerations should include the write only status of the

TDR and the following:

- BIS and BIC instructions cannot be used.

- For character lengths less than 8 bits, the character loaded into the TBUF must be right justified because the hardware induces the most significant bits to zero.

- This register is cleared by CLR and BUS INIT.

```
16XXX6                     15  14  13  12  11  10   9   8   7   6   5   4   3   2   1   0
(Write Only)              ┌───┬───┬───┬───┬───┬───┬───┬───┬───┬───┬───┬───┬───┬───┬───┬───┐
                          └───┴───┴───┴───┴───┴───┴───┴───┴───┴───┴───┴───┴───┴───┴───┴───┘

Break 7 ─────────────────────┘
Break 6 ─────────────────────────┘
Break 5 ─────────────────────────────┘
Break 4 ─────────────────────────────────┘
Break 3 ─────────────────────────────────────┘
Break 2 ─────────────────────────────────────────┘
Break 1 ─────────────────────────────────────────────┘
Break Ø ─────────────────────────────────────────────────┘
Transmit Character ──────────────────────────────────────────┘
```
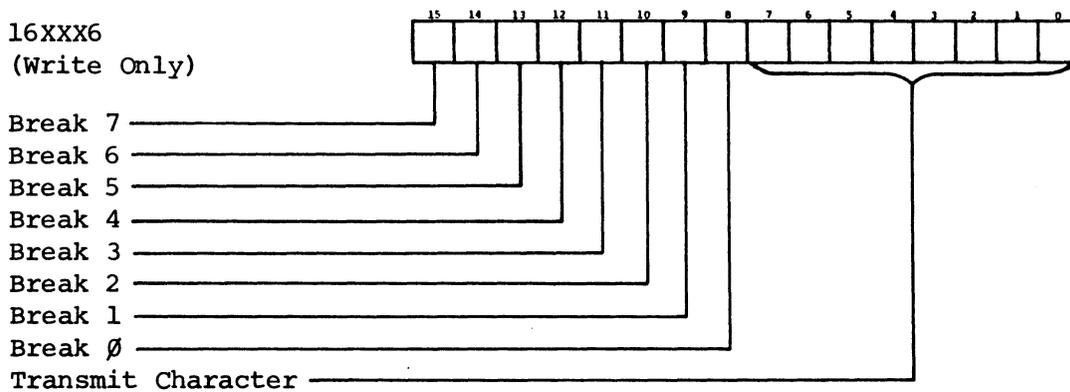
3.4 PROGRAMMING

The PM-DZ11 provides programming for baud rate, character length, stop bits, parity, and interrupts.

3.4.1 Baud Rate

Bits Ø8-11 of the Line Parameter Register (LPR) control the selection of transmission and reception speed. The speed for each line is the same for transmission and reception and is defined in Table 3-2. For the selected line, the receive clock is turned on and off by setting and clearing bit 12 of the LPR.

3.4.2 Character Length, Stop Bits, and Parity

See Section 3.3.3 for programming features derived by utilizing the Line Parameter Register (LPR).

3.4.3 Interrupts

The receiver interrupt enable (RIE) and FIFO alarm enable (FAE) bits in the CSR control the circumstances upon which the PM-DZ11 receiver interrupts the processor.

The PM-DZ11 never interrupts the PDP-11 processor if RIE and
FAE are both clear. The program must periodically check for
the availability of data in the FIFO, and empty the FIFO,
when data is present. The program should check for characters
in the FIFO at least as often as the FIFO fills, to allow a
safety factor to cover processor response delays and time to
empty the FIFO, if the program operates off a clock. When a
character is available in the FIFO, the RDONE bit in CSR will
set. With the TSTB or BIT instruction, the program can
periodically check this bit. The program should empty the
FIFO when RDONE is set.

3.4.4 Emptying the FIFO

By repeatedly performing MOV instructions from the RBUF to
temporary storage, the program can empty the FIFO. The bottom
character in the FIFO will be copied, and thus not lost, and
will clear out the bottom of the FIFO with each MOV
instruction. This allows the next character to move down for
access by a subsequent MOV instruction. By testing the data
valid bit in each word moved out of the RBUF, the program can
determine when the FIFO has been emptied, indicated by a zero
value. This test can be performed by branching on the condition
code following each MOV instruction. A TST or BIT instruction
must not access the RBUF. The TST or BIT instructions will
cause the next entry in the FIFO to move down without saving
the current bottom character, nor will the next character be
available for at least one microsecond. To prevent a false
indication of an empty FIFO on fast CPUs, the program must
use NOPs, or sufficient instructions, to ensure that
successive MOVs from the RBUF are separated by a minimum of
one microsecond.

3.4.5 Data Set Control (EIA Operation Only)

Data set control is a standard feature of the PM-DZ11A, B, or
E. The program may sense the state of the carrier and ring
indicator signals from each data set; the program may also
control the state of the data terminal ready signal to each
data set. Between the data set control logic and the receiver
and transmitter logic, there are no hardware interlocks. All
required coordination should be done under program control.

The program may access the DTR register with word or byte
instructions. Simultaneous DTR and line enable registers
are accessed if word instructions are used. Setting or
clearing a bit in this register will turn the appropriate
DTR signal ON or OFF, as this is a read/write register. The
DTR register is cleared by the INIT signal on the Unibus.
It is not cleared if the program clears the PM-DZ11 by
setting the CLR bit of the CSR.

The read-only registers are carrier (CAR) and ring (RING).
By examining the appropriate bit of the CAR register, the
program can determine the current state of the carrier signal
for a line. By examining the appropriate bit of the ring
register, the current state of the ring signal can be
determined. These registers can be examined separately. When
a carrier or ring signal changes state, the PDP-11 is not
interrupted by the PM-DZ11 data set control logic. Periodic
sampling of these registers should be accomplished to determine
the current status.

Section 4

Functional Description

4.1 INTRODUCTION

This section contains a brief functional description of the
PM-DZ11 circuitry. This section applies to all models of the
PM-DZ11 even though certain paragraphs contain information
related only to the EIA or current loop versions. These
paragraphs will specify to which model the information
pertains. For a complete understanding of the PM-DZ11
circuitry, this section must be used in conjunction with the
schematic diagrams contained in the separate maintenance
drawing package MD 701885, for EIA models, or MD 703001, for
current loop models.

4.2 PM-DZ11 LOGIC MODULE

The PM-DZ11 logic module contains all of the circuitry to
multiplex and connect the parallel data from the Unibus to
eight independent lines of serial data. Figure 4-1 is a
simplified block diagram of the logic module. Note that only
one universal asynchronous receiver/transmitter (UART) is
shown. The PM-DZ11 has eight UARTs on the logic module but
since each one (associated with one serial line of
communication) operates identically to the others, only one
will be discussed. The logic module performs three basic
functions: Unibus Interfacing, Data Control, and Serial Line
Interfacing. Also, note that the modem status register
applys only to the EIA module (701640).

The current loop module is Part Number 703210.

4.3 UNIBUS INTERFACE

All transactions between the CPU and the PM-DZ11 are related
to the Unibus interface. This interface performs address
recognition, interrupt control, and parallel data reception
and transmission (Refer to Figure 4-2.).

4.3.1 Address Selection

The PM-DZ11 address selection logic examines address lines
Ø3-17 and determines if the module has been addressed by the

UNIBUS

DATA
TRANS-
CEIVERS

BD(∅∅-15)

RBUF   FIFO   RX DATA

LPR

TDR   TX DATA
       BK(∅-7)
       CO(∅-7)
*MSR   R1(∅-7)
TCR   DTR(∅-7)
       LINE H
CSR

BAUD RATE
GEN.

TX & RX CLOCKS

UART
(TYPICAL
1 TO 8)

TSO
RS1

SERIAL
LINE
DRIVERS

SERIAL
LINE
RXURS

BA(∅∅-12)
BC(∅-1)
INIT

REGISTER
CONTROL
LOGIC

SCAN &
CONTROL
LOGIC

BA(∅3-17)
MSYN
SSYN

ADDRESS
SELECTION
LOGIC

INT REQ

INTERRUPT
LOGIC

VECTOR
CONTROL

SACK
INTR
BR(4-7)
BG(4-7)
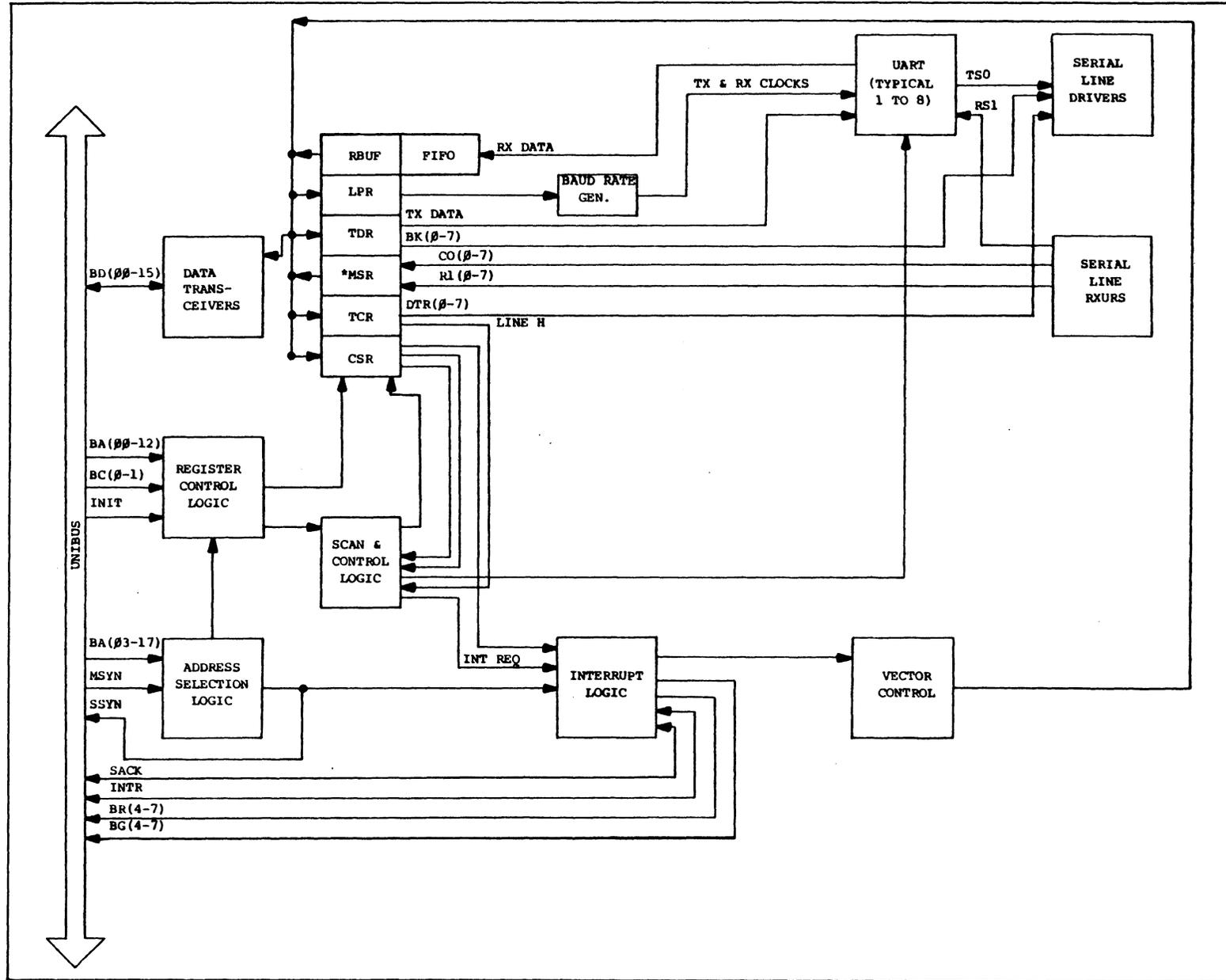
FIGURE 4-1:   FUNCTIONAL PM-DZ11 BLOCK DIAGRAM
(*EIA MODELS ONLY)
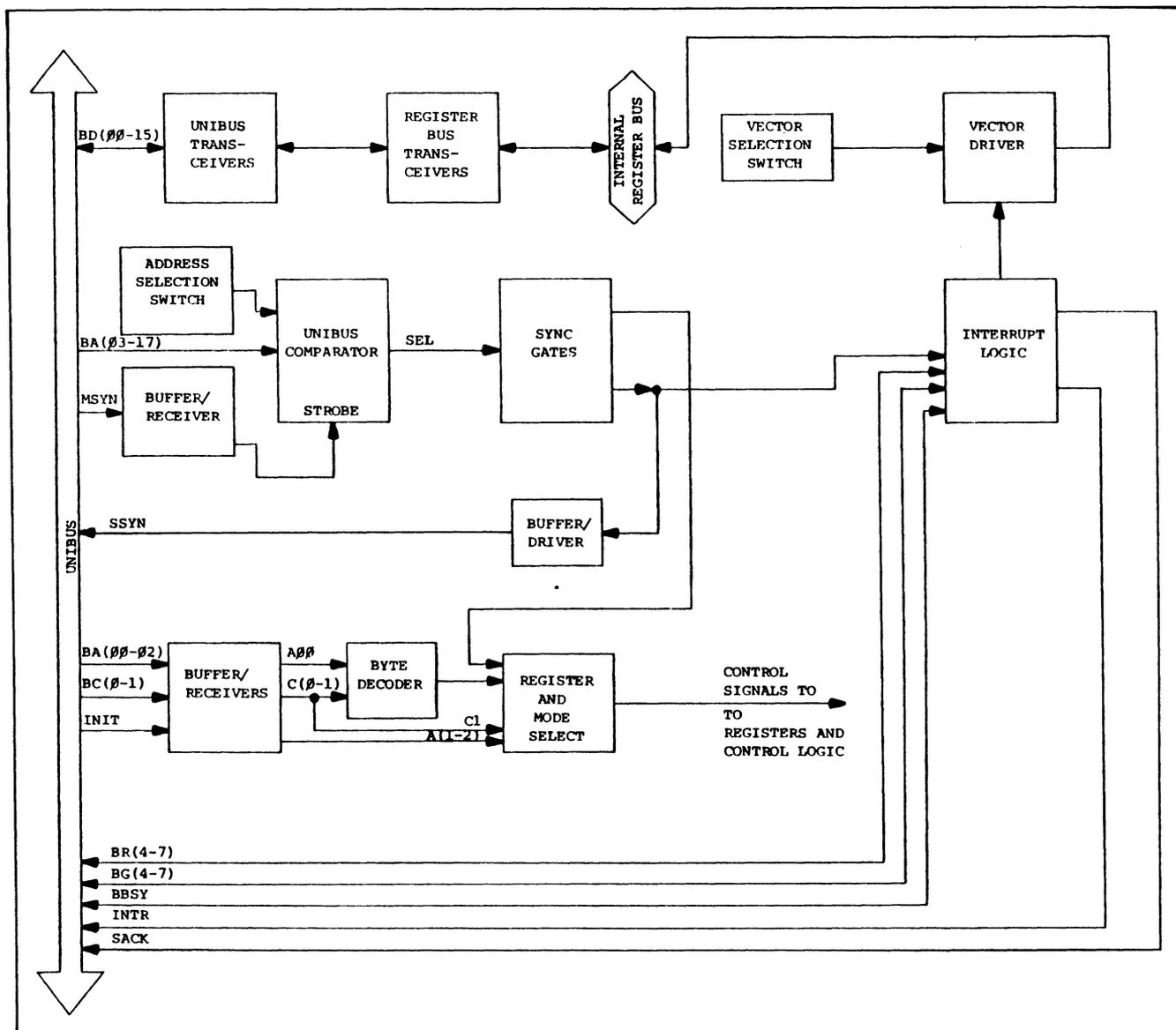
FIGURE 4-2: UNIBUS INTERFACE LOGIC BLOCK DIAGRAM

bus master. The Unibus comparators are utilized to receive
address data and examine the bits. Two of these comparators
compare address lines ∅3 through 14 with the address set by
the module's address selection switch. The third comparator
is hardware set to compare bits 15 through 17.

Master sync is received and then delayed by an R-C circuit
consisting of R18 and its associated capacitor and "AND" gate
prior to strobing the address comparators. This insures
sufficient set-up time. If all three comparators respond, a
signal, SEL H, is driven to the synchronization gates. Refer
to Sheet 2 of the schematics.

MA 701885   REV A

A series of gates sets up the proper time intervals necessary for synchronization of internal logic functions. These synchronization gates also generate slave sync (SSYN) which is then driven out the Unibus.

Slave sync is also applied to the interrupt logic for proper interrupt and request sequencing.

4.3.2 Register Selection

The remaining address lines (∅∅-∅2), the control lines, and INIT are received and buffered by Unibus compatible receivers. A random logic network determines which mode of operation is desired: Read, Write, Read Byte, or Write Byte. The address bits A(1-2) and control bit C1 are then applied to two ten-line decoders.

These decoders perform a BCD conversion to select the resultant output. The output lines are utilized as register enable signals. Only one of the two decoders is enabled at a time since one controls read register operations and the other controls write register functions.

4.3.3 Data Lines

Data is transferred to and from the Unibus by four transceivers. These transceivers match the bus impedance and connect the data lines D(∅∅-16)L to TTL compatible levels. The TTL levels are exchanged between a set of four tri-state bus transceivers. The data then travels a data bus internal to the PM-DZ11 logic module. This internal bus services all of the registers and the vector driver.

4.4 INTERRUPT CONTROL

The interrupt logic controls the generation of bus requests, slave acknowledge, and interrupts. Bus Busy is also monitored. Refer to Figure 4-3.

When the PM-DZ11 control logic requests an interrupt, a flip-flop circuit arbitrates to insure the receiver has priority over the transmitter. The request is placed on the Unibus through the priority plug inserted in J2.

Bus Grants also pass through the priority plug prior to being received and conditioned. If the module did not place a request at the level of the grant, the grant arbitration latches pass the grant to the Unibus through a driver.

If the logic module did make the request, then SACK is driven
on to the Unibus. Once the conditions have been met, INTR is
placed on the system bus.

4.4.1 Vector

The vector address is selected and set with an on-board switch.
When the interrupt logic wishes to retrieve the vector address,
it enables the tri-state vector driver. The driver then puts
the address onto the module's internal bus.

During a vector transfer only the two Unibus transceivers
passing the vector address are enabled.
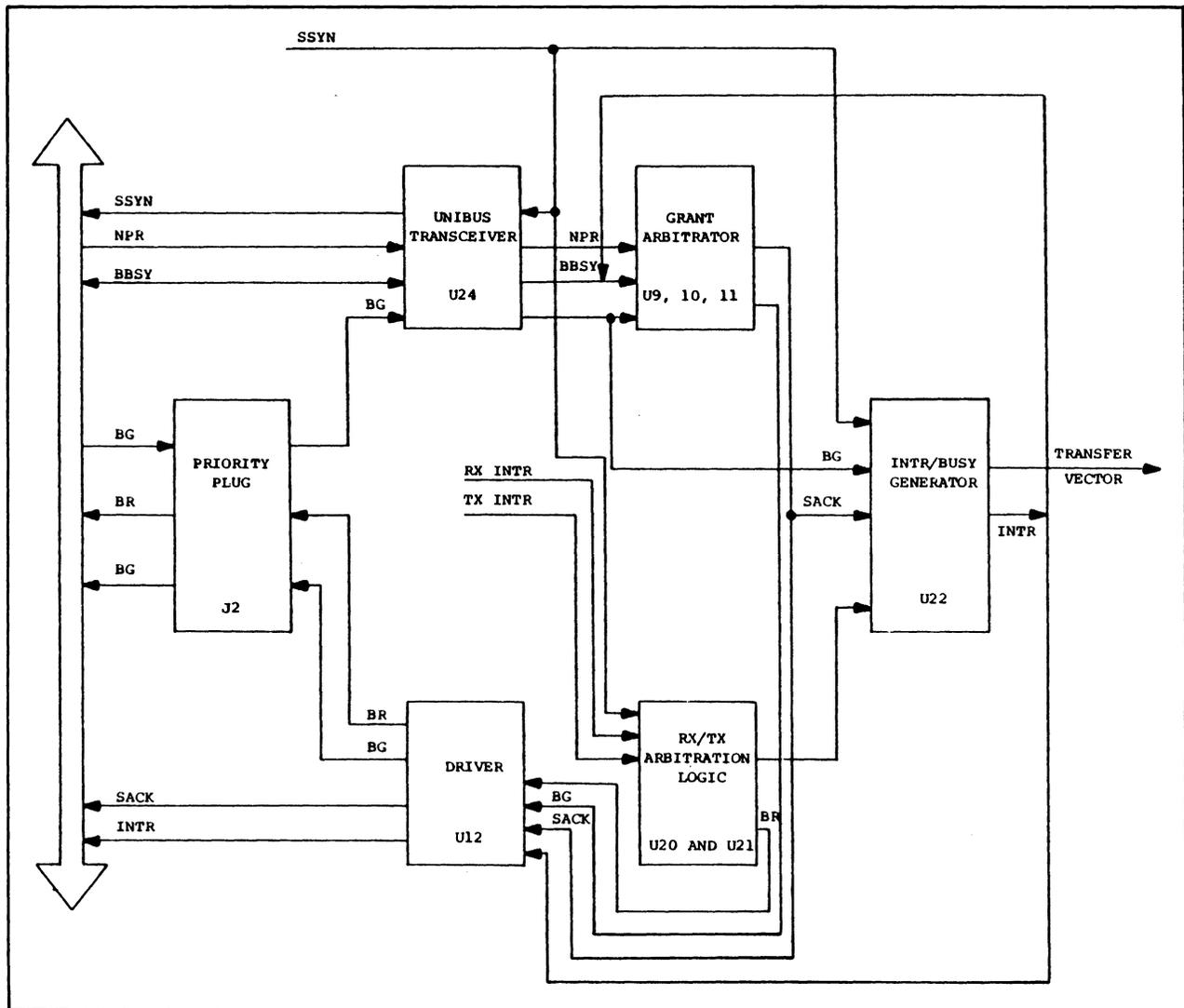
FIGURE 4-3: INTERRUPT LOGIC BLOCK DIAGRAM

4.5 DATA CONTROL

The PM-DZ11 contains six device registers. They are addressed
R∅, 2, 4, and 6. R2 and R4 are assigned Read only or Write
only status; hence six registers R∅ (R/W), R2 (R), R2 (W),
R4 (R/W), R6 (R), and R6 (W). Refer to Section 3 for a
complete description of the register bit assignments and
restrictions.

Note that the current loop models do not utilize R6 (W).

4.5.1 PM-DZ11A, B, and E Registers (EIA Versions Only)

The following subsections apply only to EIA versions of the
PM-DZ11. Schematic sheet numbers are in reference to
SD701640.

● Control Status Register

   The control status register is made up of 4 I.C.'s: U13,
   U32, U59, and U65. It receives most of its data from the
   module's control logic and the internal bus. Refer to
   Sheet 3 of schematics.

● Transmit Control Register

   The transmit control register consists of four tri-state
   bus registers: U90-93. Each bit in upper byte corresponds
   to data terminal ready (DTR) for each EIA line and is
   consequently connected to a buffer and EIA transmitters.
   The lower byte contains enable information for the module's
   control logic. Refer to Sheet 8 of schematics.

● Modem Status Register

   The modem status register is the read only section of R6.
   It is made up of 2 I.C.'s: U99 and U100. The inputs to
   this register come from EIA receivers, and the output is
   fed to the internal data bus. Refer to Sheet 9 of
   schematics.

● Transmit Data Register

   The transmit data register is the write only portion of R6.
   The upper byte receives its data from the internal data
   bus and controls Break for each EIA line. U84 and U85 are
   located on Sheet 9 of schematics. The lower byte buffers
   the serial data to be transmitted. U60 is shown on Sheet
   10 of schematics.

● Line Parameter Register

   The line parameter register is the write only portion of
   R2. The lower byte consists of U38, U40, and U60. Refer
   to Sheets 5 and 10 of the schematics. The upper byte of
   the LPR writes from the internal bus directly into the
   four baud rate generators U26-29. Refer to Sheet 6 of
   schematics.

● Receiver Buffer

   The receiver buffer is the read only portion of R2. It is
   contained in 2 I.C.s: U78 and U88. It receives its data
   from the FIFO and gives it to the internal data bus. Both
   the FIFO and receiver buffer are shown on Sheet 7 of the
   schematics.

4.5.2 PM-DZ11C, D, and F Registers (Current Loop Only)

The following sub-sections apply only to current loop versions
of the PM-DZ11. Schematic sheet numbers are in reference to
SD703210.

● Control Status Register

   The control and status register is made up of 3 I.C.s:
   U44, U53, and U77. It receives most of its inputs from
   the module's control logic and the internal tri-state bus.
   Refer to Sheet 3 of the schematics.

● Transmit Control Register

   The transmit control register consists of two tri-state bus
   registers: U27 and U3. The lower byte contains enabling
   bits for the module's control logic. The upper byte is
   unused; thus no logic is present. Refer to Sheet 5 of the
   schematics.

● Transmit Data Register

   The transmit data register is the write only portion of R6.
   The upper byte receives data from the internal bus and
   controls Break for each line. U40 and U39 make up the
   upper byte. The lower byte buffers the data to be
   transmitted. U74 performs this function. The TDR gates
   are shown on Sheet 5 of the schematics.

● Line Parameter Register

   The line parameter register is the write only portion of
   R2. The upper byte writes directly from the internal bus
   into the four baud rate generators U17-20. The lower byte

is comprised of U6 and U8. U6 and U8 are data selectors
for line enable. Most of the LPR logic is contained on
Sheet 4 of schematics.

● Receiver Buffer

The receiver buffer is the read only portion of R2. It is
contained in 2 I.C.'s: U75 and U76. It receives its data
from the FIFO and gives it to the internal data bus. Both
the FIFO array and the receiver buffer are shown on Sheet
5 of SD703210.

4.5.3   FIFO

The characters received from the line interface are stored in
a 64 by 16 bit First-In First-Out memory. This memory is
made up of four 64 by 4 bit memory I.C.'s. Parallel data
from the UART is loaded into the FIFO under control of the
scanner. Stored data is read out of the FIFO by a read
instruction to the RBUF.

4.5.4   Baud Rate Generation

The baud rate generators determine the speed of transmission
and reception of the UARTs. Each I.C. contains two separate
generators. The proper generator is enabled by the LPR lower
byte. Gates are utilized so the LPR may selectively disable
the individual receiver clocks to the UARTs.

4.6   DATA CONDITIONING

The data conditioning logic performs the task of converting
parallel data to serial data and vice versa, as well as
interfacing the TTL levels used on the logic module to levels
which meet the appropriate output standard.

4.6.1   Universal Asynchronous Receiver/Transmitter (UART)

The UART device simultaneously transmits and receives
asynchronous data in duplex or half-duplex operation. The
receiver converts serial asynchronous binary characters to a
parallel output. The separate transmitter/receiver clock
rates must be 16 times the desired baud rate (DC to 160KHz).

Control bits select 5, 6, 7, or 8 bit character lengths,
mode, odd, or even parity and 1.5 (5-level only), 1, or 2 stop
bits for 6, 7, or 8 bit characters. The 5-bit characters
require 1 or 1 1/2 start bits. Since the transmitter and

receiver have double character buffering, at least one complete
character is always available. Control information is stored
in a register. The format of a typical I/O serial word is
shown in Figure 4-4.
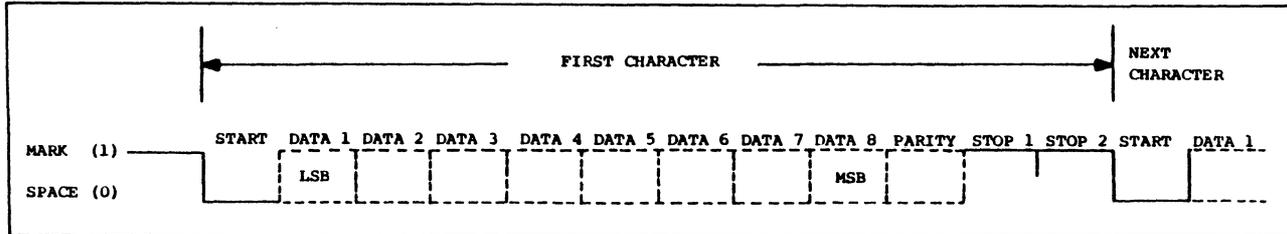
FIGURE 4-4: FORMAT OF TYPICAL INPUT/OUTPUT
           SERIAL CHARACTER

Figure 4-5 is a block diagram of the UART transmitter. The
data buffer can be loaded with a character when Transmitter
Buffer Empty (TBMT) line goes high. Loading is done by
generating a short negative pulse on the Data Strobe (DS)
line. The load operation is performed by the positive-going
trailing edge of the DS pulse. The character is transferred
to the UART Transmitter Shift Register as soon as the register
is empty. The start, stop, and parity bits are added to the
data initiating transmission. One sixteenth of a bit time
before a complete character (including stop bits) has been
transmitted, the End of Character (EOC) line goes high and
remains high until transmission of a new character begins.

A simplified block and timing diagram for the UART receiver is
shown in Figure 4-6. When serial asynchronous data is sent to
the Serial Input (SI) line, the UART searches for a high to
low (mark to space) transition on the SI line. If the high to
low transition is detected, the receiver searches for the
center of the start bit as the first sampling point. If the
point is low (space), the signal is considered a valid start
bit, and sampling continues at the center of the subsequent
data and stop bits.

The character is assembled bit by bit in the Shift Register
that utilizes control signals to determine the number of data
bits and stop bits, and the type of parity, if selected.
The Receiver Parity Error (PER) line goes high if parity is
selected and does not check. The Framing Error (FER) goes
high if the first stop bit is low. After the stop bit is
sampled, the receiver transfers the contents of Shift Register
into the Data Buffer in parallel. The receiver then sets the
Received Data Available (DA) line and transfers the state of
the framing and parity errors to the Status Buffer Register.
When the PM-DZ11 accepts the receiver outputs, it causes the
Reset Data Available (RDA) line low which, in turn, clears
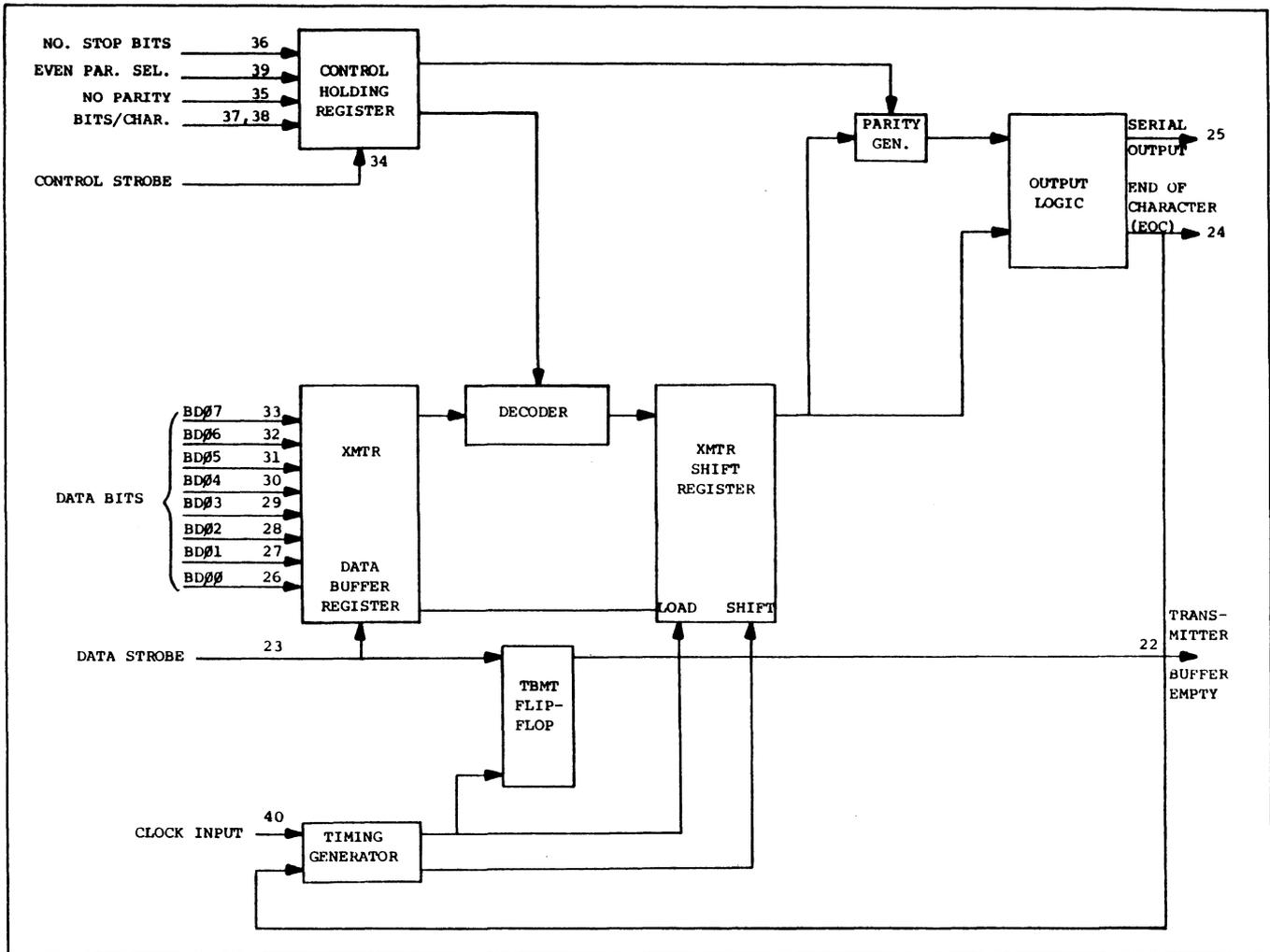
FIGURE 4-5:   UART TRANSMITTER, BLOCK DIAGRAM
AND SIMPLIFIED TIMING DIAGRAM
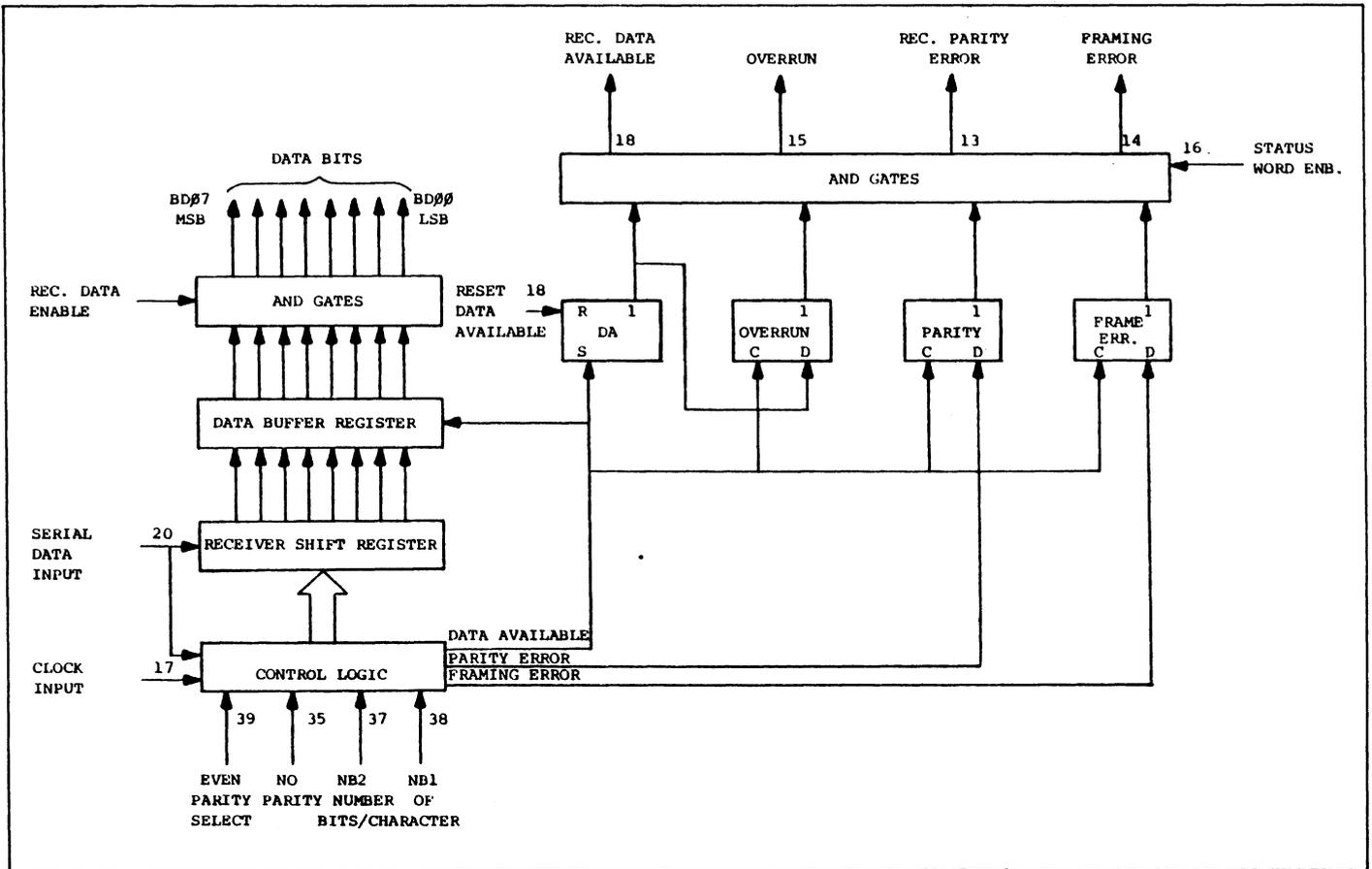
FIGURE 4-6:   UART RECEIVER, BLOCK DIAGRAM AND
              SIMPLIFIED TIMING DIAGRAM

the DA line. If the line is not reset before a new character
is transferred to the Data Buffer, the Overrun (OR) line goes
high. The OR line is held high until the next character is
loaded into the Data Buffer.

4.6.2 Data Level Conditioning

- EIA Versions

  Serial data is sent through EIA drivers and/or receivers.
  These drivers convert the TTL levels to those that conform
 with EIA standard RS232C.

- Current Loop Versions

  Serial data is passed through a transistor network. These
  transistors convert the TTL levels to 20mA current loop.
  The drivers are shown on Sheet 6; the receivers are shown
 on Sheet 8.

4.6.3 Distribution

All serial lines are cabled to the distribution panel. In
route all lines pass through a static filter to prevent
extraneous noise from entering the PM-DZll logic. The
distribution panel routes the serial data for each channel to
a separate connector for user supplied cabling to the modem
or terminal device.

Plessey Peripheral Systems • 17466 Daimler Ave., Irvine, CA. 92714 • Tel: (714) 540-9945