R. MOORHEAD

Digital Equipment Corporation
Maynard, Massachusetts

digital

PDP-9

SYSTEM ADJUSTMENT MANUAL

DEC-9A-H0AA-D

PDP-9
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ILLUSTRATIONS

1. INTRODUCTION

This document is prepared to assist field service personnel in performing a system adjustment of the PDP-9. Procedures are given for various adjustments of the Main Memory (MM), the Control Memory (CM), and some Input/Output (I/O) conditions.

The material is organized in a test procedure format and presumes a prior knowledge of the computer hardware and standard test equipment. It is further assumed that the user of this document is able to prepare and load certain diagnostic programs required in the performance of these procedures.

Where necessary, line tracings of oscilloscope waveforms are given to aid the technician in evaluating the system under test. These are not idealized waveforms but actual tracings made by the manufacturer under factory conditions. Any deviation in these patterns from those observed at the customer's site should be indicative only of differences in ambient conditions.

2. MAIN MEMORY (MM)

2.1 MC70B Voltage Checks and Adjustments

2.1.1 Main Voltage Check - The MM voltage is measured between J01M and H01M (negative probe of meter on H01M). Adjust the potentiometer on the G804 module, Location (LOC) HJ08 on the MC70B, for 23.5 Vdc. (See tech tip 108, PDP-9 tech tip 3 concerning G622s.)

2.1.2 Second Stage Clamp Voltage Check - The second stage clamp voltage is measured between E25B and E25N (negative probe of meter on E25B). Adjust the potentiometer on the G008 module, LOC E25 of the MC70B, for 6 Vdc. (This is the right-hand potentiometer on the G008 as you face the module handle.)

2.1.3 Slice Voltage Check - The slice voltage is measured between E25H and E25A (negative probe of meter on E25H). Adjust the potentiometer on the G008 module, LOC E25 of the MC70B for approximately 4.2 Vdc. (This is the left-hand potentiometer on the G008 as you face the module handle.)

NOTE

This is a ball park figure which will be refined, after the memory timing adjustments have been made, to balance the +10V margins on the sense amplifiers.

2.2 MC70B Timing Adjustments

2.2.1 Check - Check the MM timing adjustments by doing a JMP 0 in LOC 0, (LOC 00000 = 600000). If the computer will not run this instruction, turn the DATA switches to UP (all 1s) and the ADDRESS switches to DOWN (all 0s). With the REPT (REPEAT) switch turned UP, turn the MAINTENANCE switch to DEPOSIT. Use the highest REPT SPEED (position 5).

2.2.2 Set Up - Set the oscilloscope to ALT MODE and set the GAIN of both traces to 1 V/cm. With the input signals grounded, position the traces 1.5 cm above the center line of the grid. (The negative input signals should cross the center line of the Scope Grid (SG) when they are -1.5V.) All times are measured along the center line of the SG (see Figure 1).

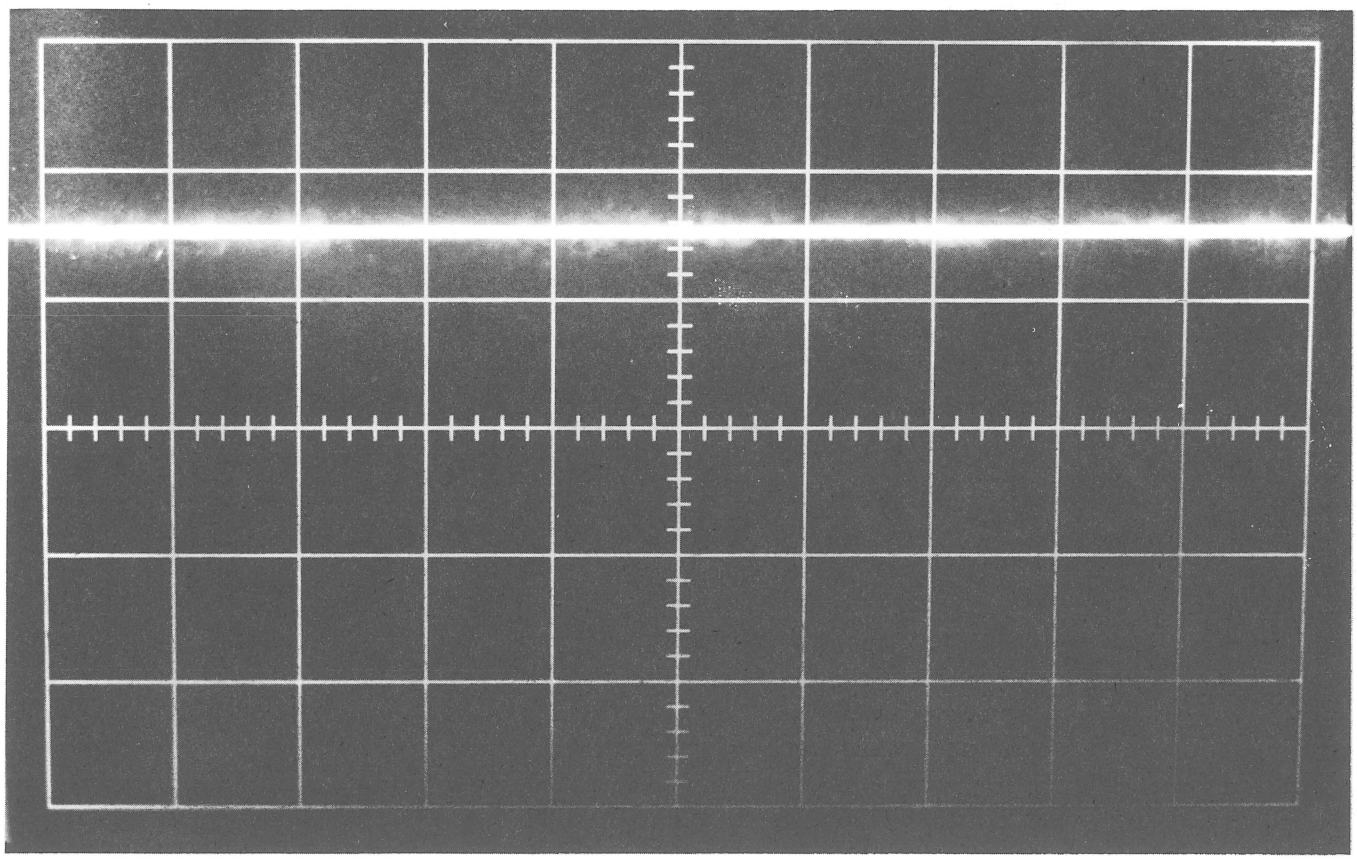

Figure 1 Ground Reference

2.2.3 Procedures - Unless otherwise noted, SYNC on probe 1 of the scope. If the scope is not equipped for this, use an external sync, and then SYNC on the same signal as is being observed on probe 1. Unless otherwise noted, all measurements are taken from the negative leading edge of the signal on channel 1 to the negative leading edge of the signal on channel 2. See specific figures for the time/cm settings. All locations, unless otherwise noted, refer to the MC70B section.

WARNING

Be sure to GROUND (GND) all probes.

2.2.3.1 MA Set Up

Probe 1: F36M = CLOCK (CLK)
Probe 2: C16D = DIGIT READ SYNC (RS)
Delay time: 180 ns
Adjust: D35
See Figure 2.

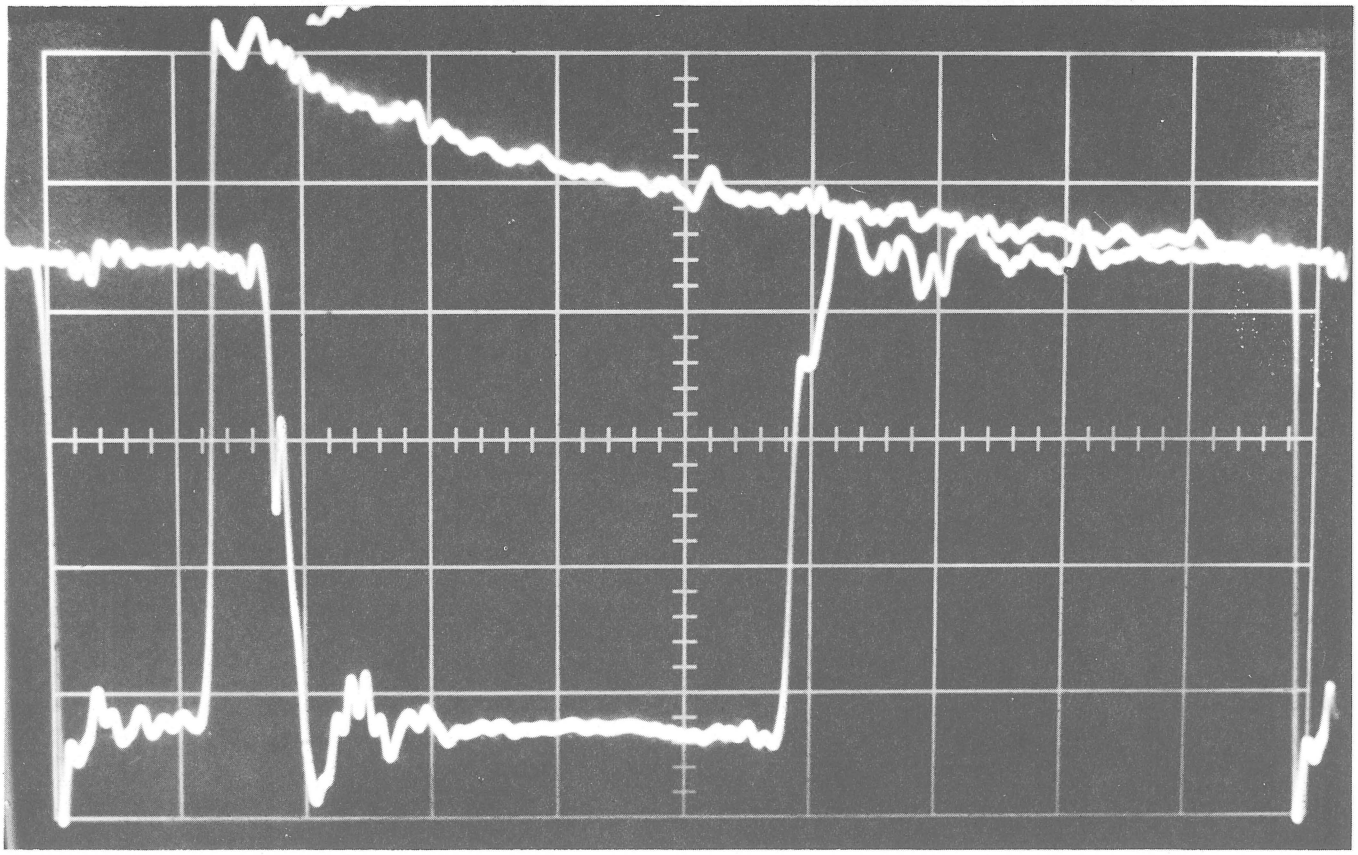

Figure 2 MA Set Up 100 ns/cm @ 1 V/cm

2.2.3.2 Stagger Delay

Probe 1: C16D = DIGIT RS

Probe 2: H33D = WORD READ (WR)

Delay time: Approximately 80 ns[1]

Adjust: D33

See Figure 3.

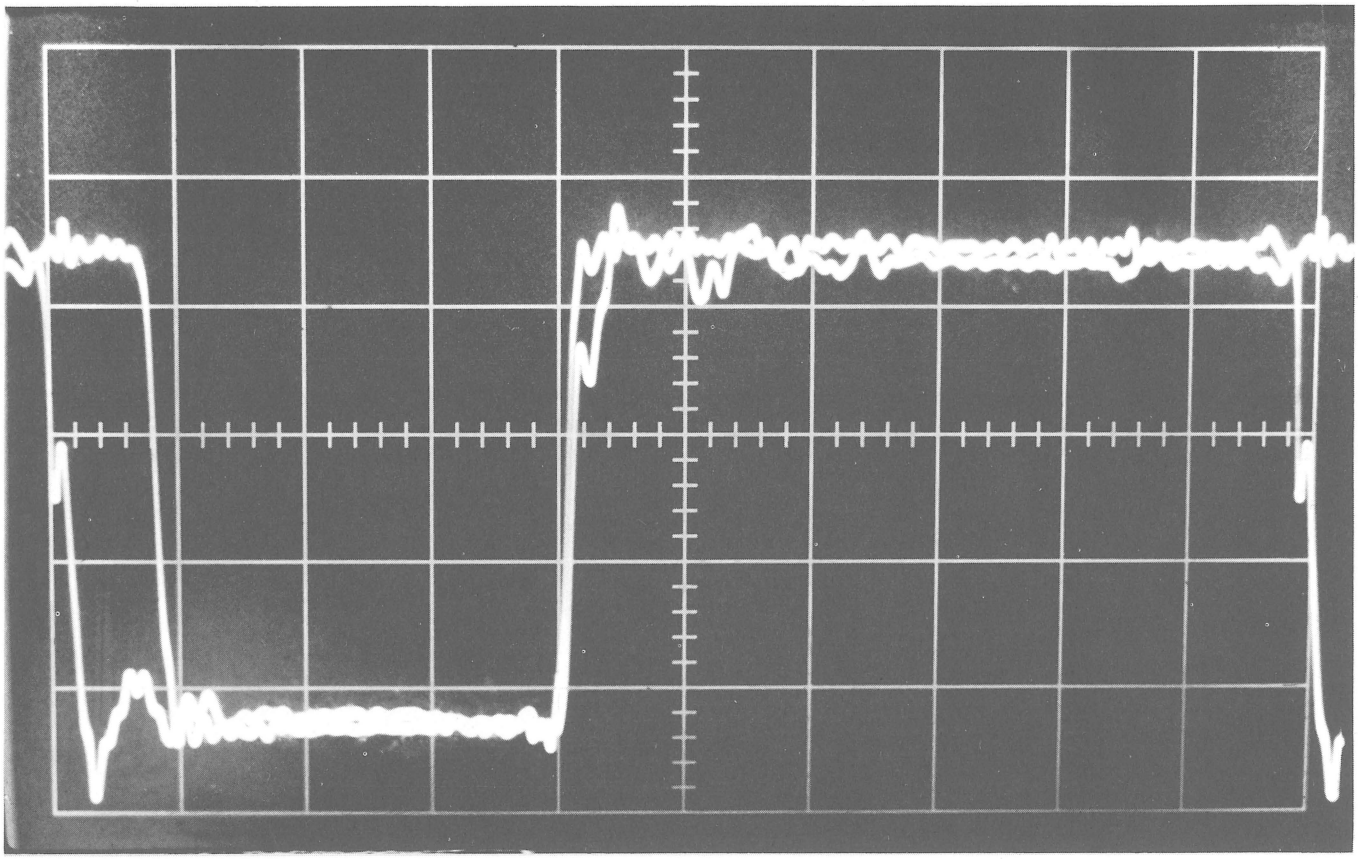

Figure 3 Stagger Time 100 ns/cm @ 1 V/cm

2.2.3.3 Strobe Delay[2]

Probe 1: C16D = DIGIT RS

Probe 2: E32L = MEM Strobe

Delay time: 320 ns

Adjust: E30

See Figure 4

[1]This is an approximate setting and may be refined later to optimize memory margins and operation.

[2]Any time that strobe (E30) is adjusted stagger (D33) must also be adjusted by the same amount to maintain the correct relationship between core memory output and strobe (see Figure 7).

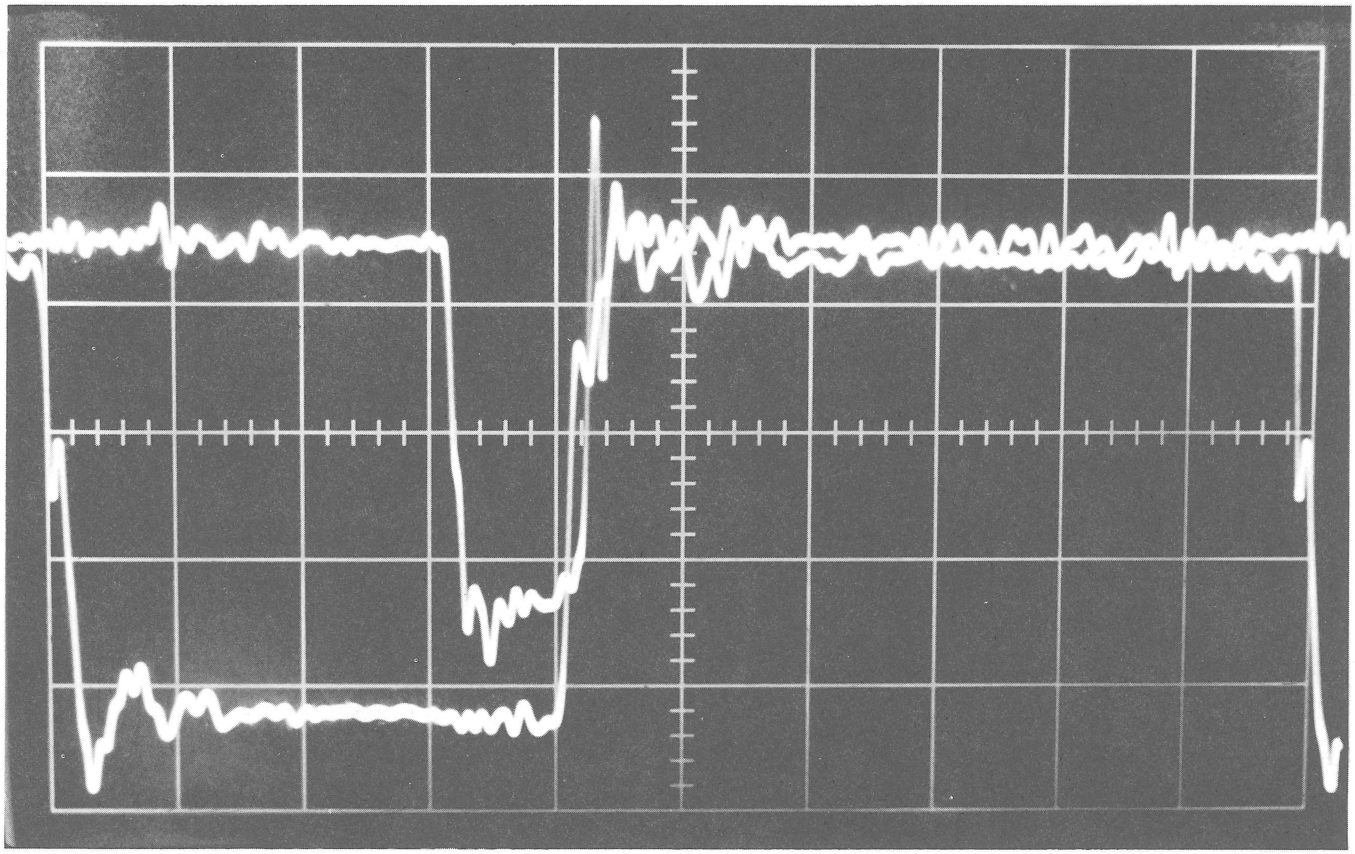

Figure 4 Strobe 100 ns/cm @ 1 V/cm

2.2.3.4 Pause Delay

Probe 1: E32L = MEM Strobe

Probe 2: H32N WORD WRITE (WW)

Delay time: 260 ns[1]

Adjust: F33

See Figure 5

2.2.3.5 Write Delay

Probe 1: F36M = CLK

Probe 2: H32N = WW

Delay time: Adjust for overlap of 20-30 ns

Adjust: F34

See Figure 6

[1] For a machine with parity option and a 1.2 μs cycle time, adjust pause (F33) for 400 ns instead of 260. All other memory timing adjustments will remain the same.

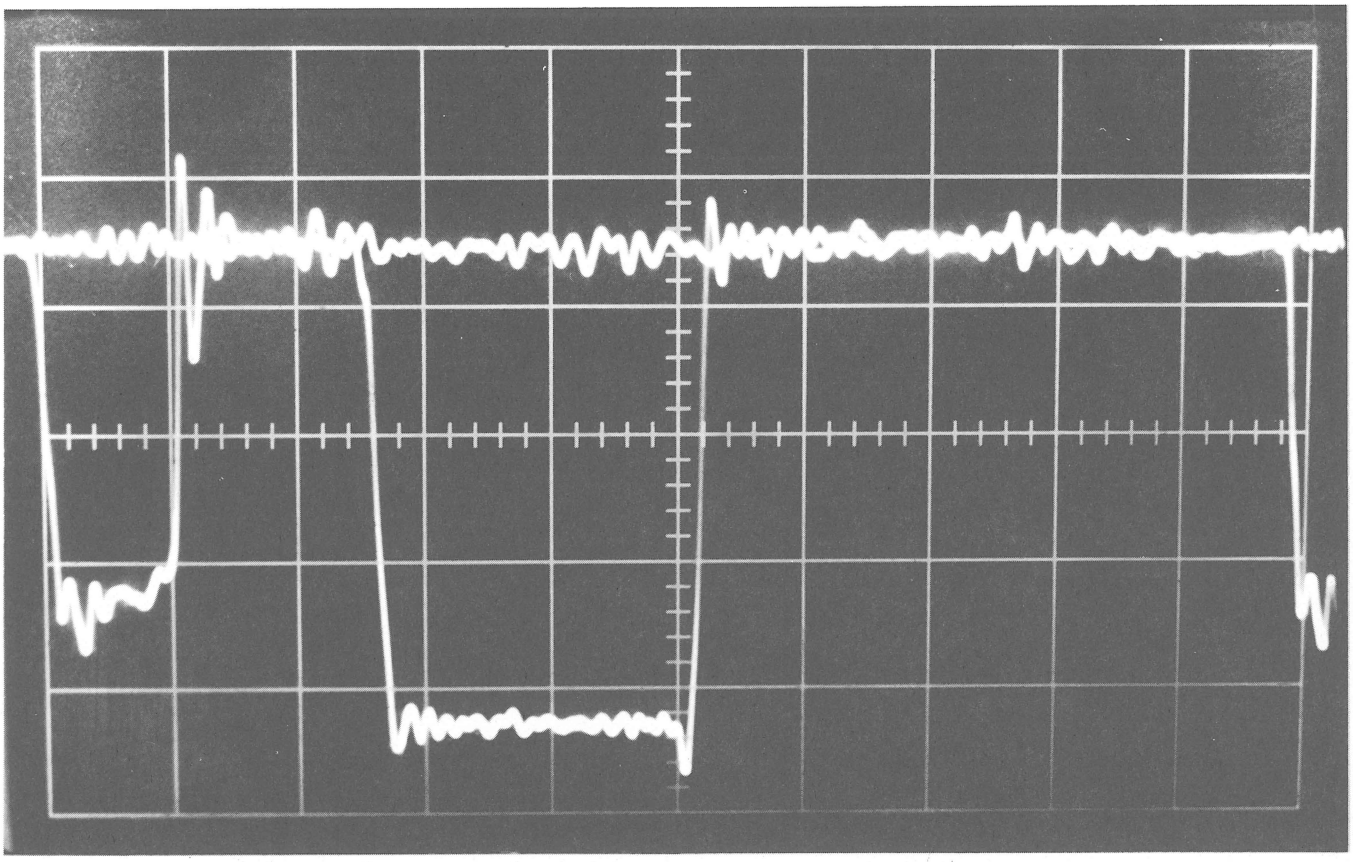

Figure 5 Pause Time 100 ns/cm @ 1 V/cm

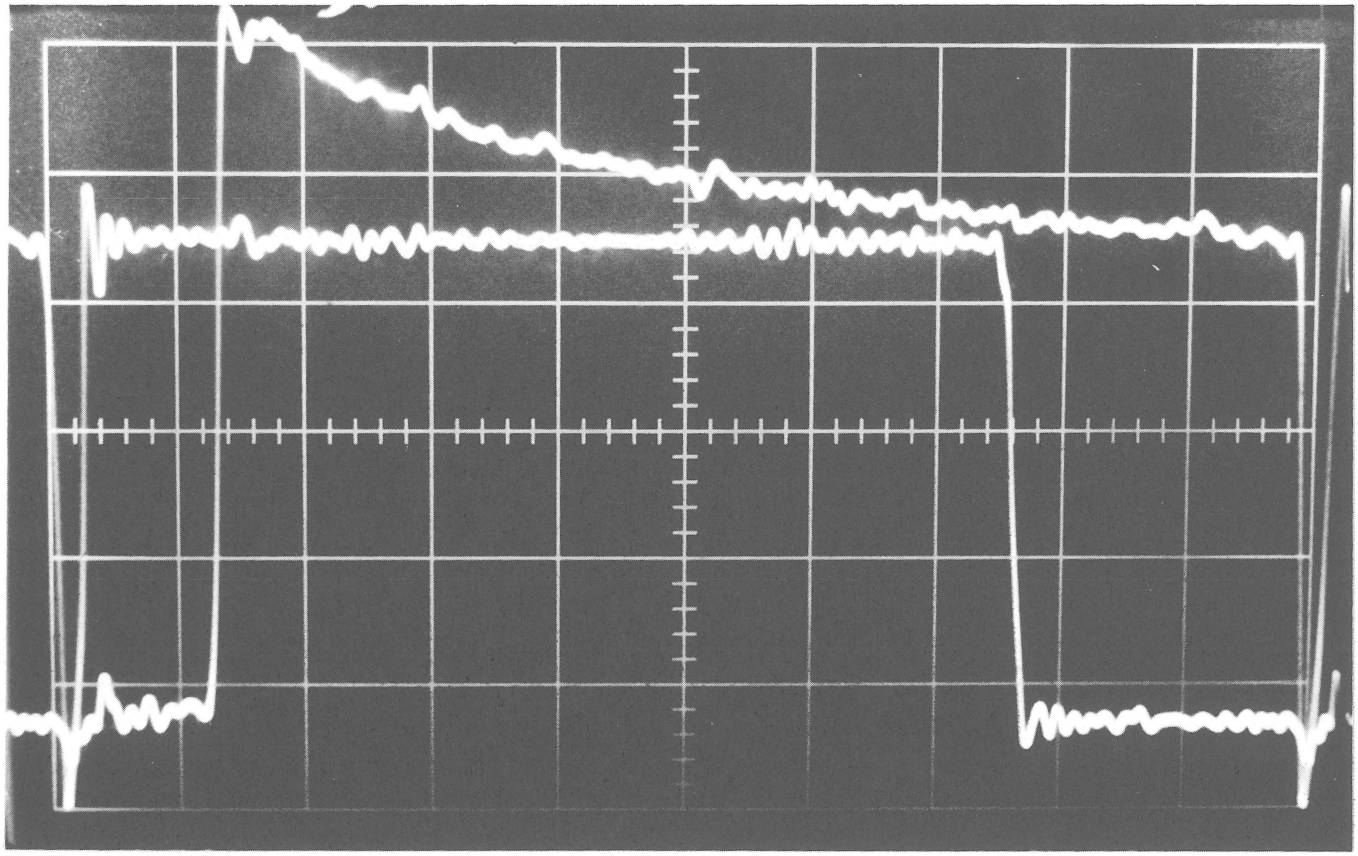

Figure 6 Write Time 100 ns/cm @ 1 V/cm

NOTE

If the computer will not run instuctions as yet, perform the CM adjustments in the KC09A central processor before proceeding.

2.2.3.6 Stagger Time Set Up - Load all 1s through memory, i.e., with all the DATA switches in the "1" position UP, ADDRESS switches DOWN (0s), and the REPT switch UP; press DEPOSIT (DEP) and then DEP NEXT. Hold the switch in the DEP NEXT position for a few seconds (until all locations are loaded); release, put the REPT switch DOWN, press I/O RESET and then START. The computer should loop through memory. Look at pin C23U - strobe SENSE AMPS RIGHT (SAR), with probe 1 and SYNC on this signal. Look at pins P or R of any sense amplifier, such as C23R, with probe 2. Adjust the scope so that the strobe pulse crosses the center line of the SG when it is -1.5V. Adjust stagger (D33) so that the peak output of the core signal (probe 2) intersects the negative leading edge of the strobe signal (probe 1) where it passes through the center line. See Figure 7. When making this adjustment be sure that the core output varies in time and not the strobe pulse.

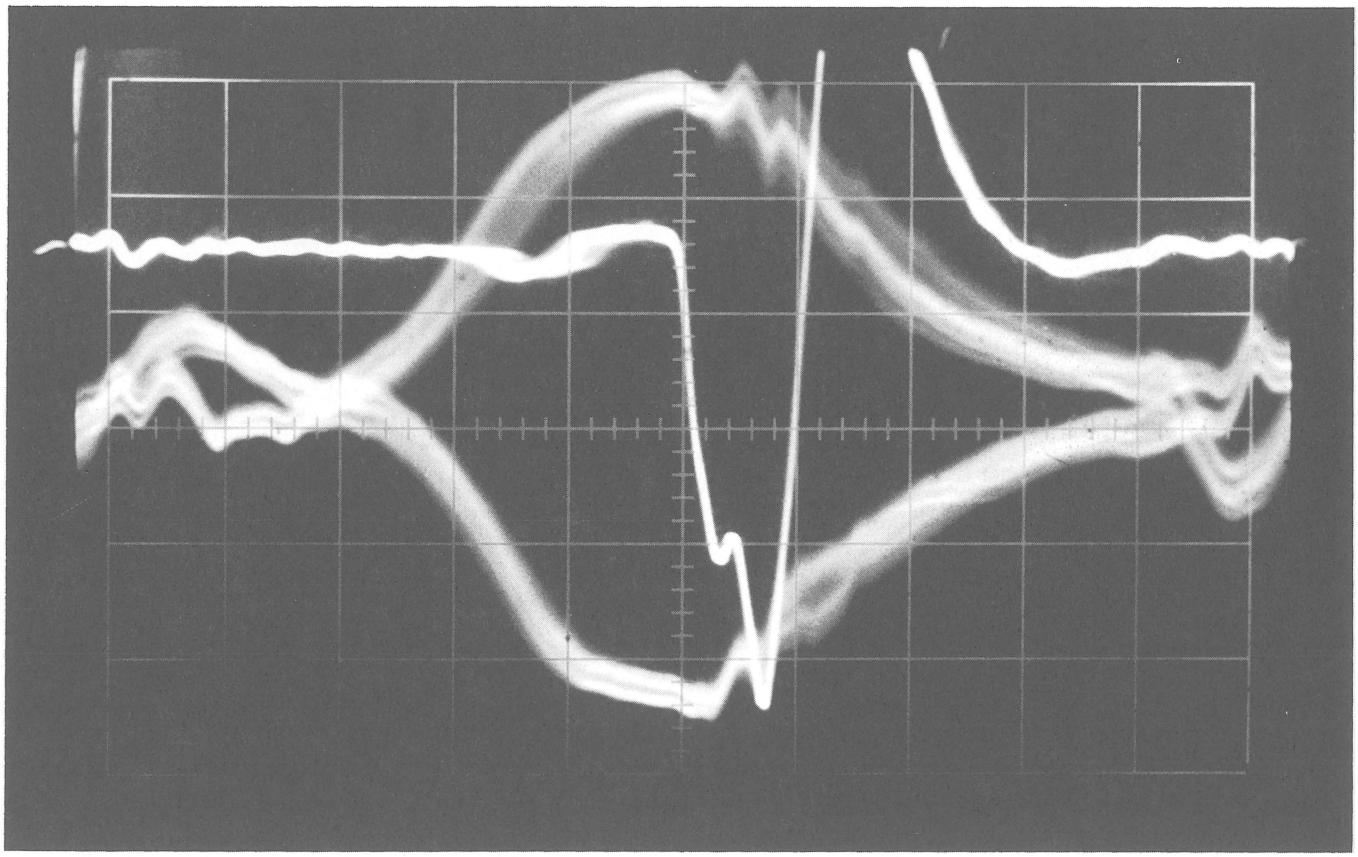

Figure 7 Core Output and SAR 50 ns/cm
(Sweep 0.5 μs/10) @ 1 V/cm

2.2.3.7 Slice Level Set Up - Using the same scope set up as in 2.2.3.6, look at channel 2 only. Set up scope timing as in Figure 8. With the all 1s program running through memory, adjust the potentiometer on the W016 module (LOC HJ21) until the deflection of the leading edge of the core signal is minimum. This adjustment balances the WS signals to each 4K portion of the 8K stack so that the sense amp outputs will occur at about the same time regardless of the bits address. The Null Point signals should be similar to those in Figure 9. After performing this adjustment recheck stagger time (Figure 7) and reset if necessary. Also see tech tip 18 for PDP-9s.

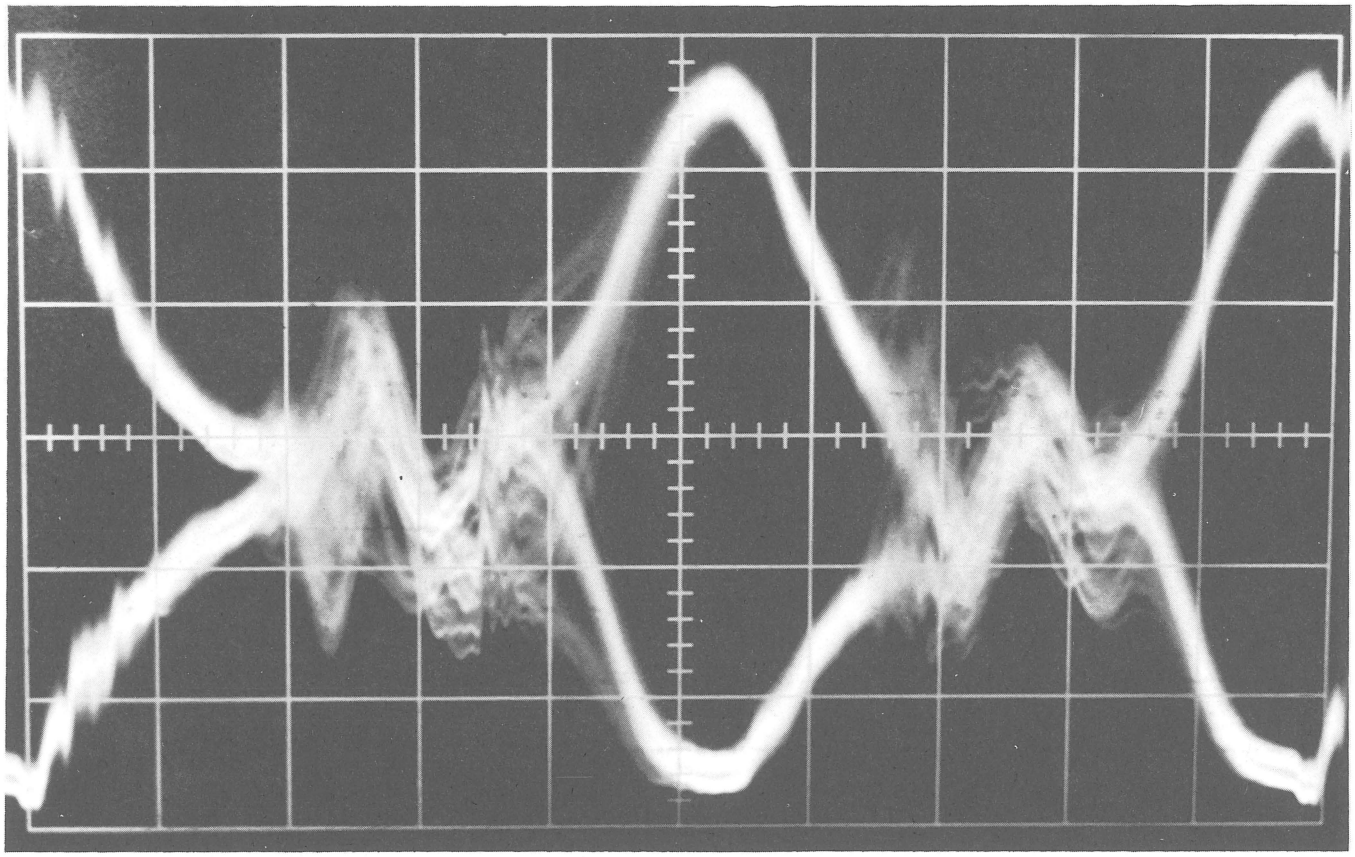

Figure 8 Core Output With Excessive Dispersion

To finalize the slice voltage setting, load the extended memory checkerboard program DEC-9A-D1BA-PH into memory as per those instructions. Stop program and turn off power. Turn on SENSE AMP MARGINS switch in MC70B (switch 7) and put the MARGINAL VOLTAGE switch to +10V. Turn on computer and run program. Vary margins in positive direction until a failure occurs. Record the setting on the meter. Do the same in the negative direction. Adjust the slice voltage level on the G008, as in Section 2.1.3, until equal positive and negative variations from 10V result. These

margins must be equal and should exceed the margin specifications for switch 7 @ ∓ 7.0V. This should require less than 1 complete turn in either direction to balance margins.

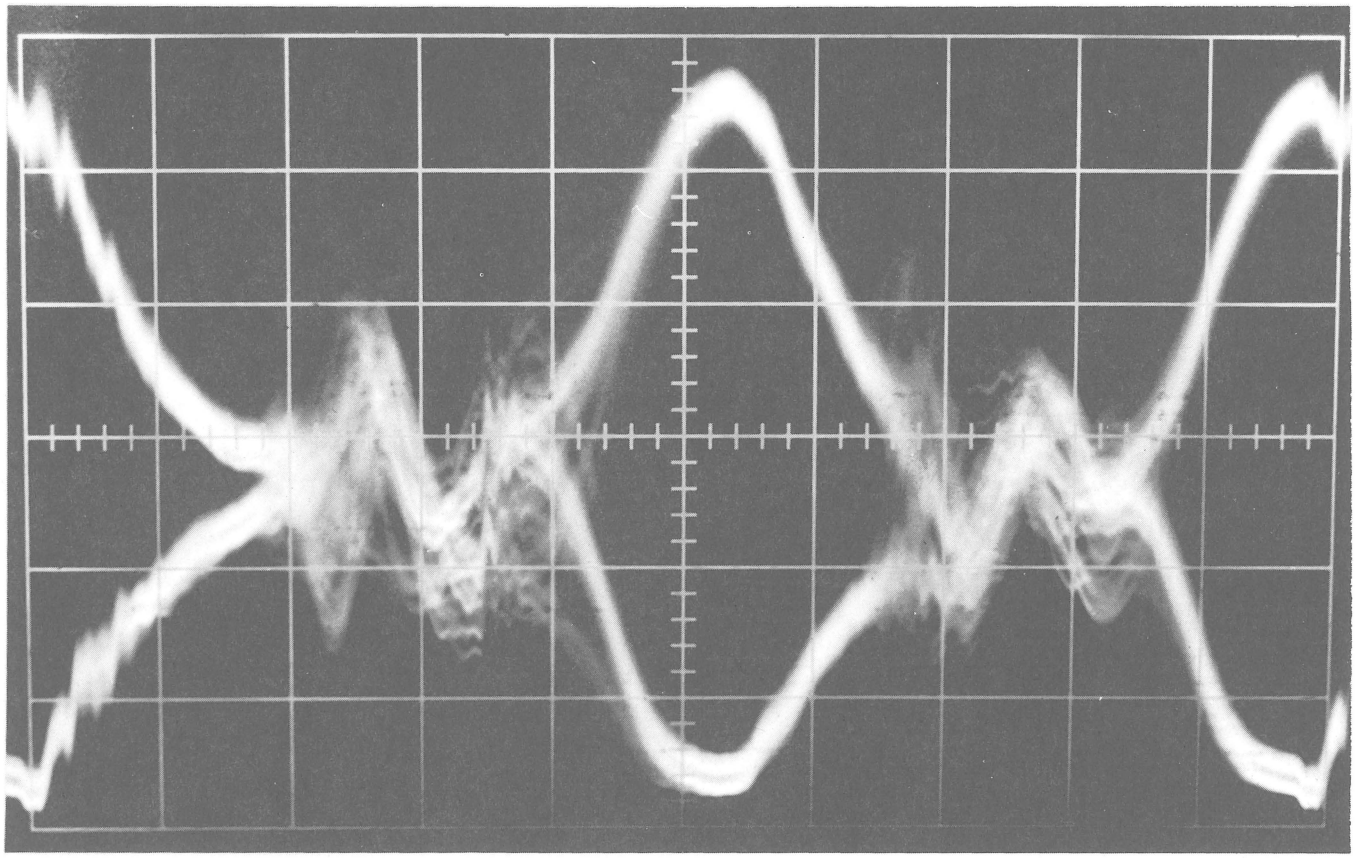

Figure 9 Core Output With Minimum Dispersion

3. CONTROL MEMORY (CM)

The CM delays are B310s whose delay times are adjusted by jumper wires on the wiring side of the PDP-9. These jumper wires are installed at the plant; however, if module replacement in the CM timing area is necessary and/or if margins fall below specifications, then adjustments must be made in the field. For adjustment procedures, refer to Figure 10. The B310 is adjustable in increments of 12.5 ns starting with a minimum delay through the circuit of about 27.5 ns when pins E and K or N and T are jumpered together. A maximum of 65 ns delay is available when E and F or N and P are jumpered together. When an adjustment is necessary "Adjust E33 E to K, J, H, F" might be called out. The user then need only remove the existing jumper wire, E to J and install a new wire, to make delay longer E to H.

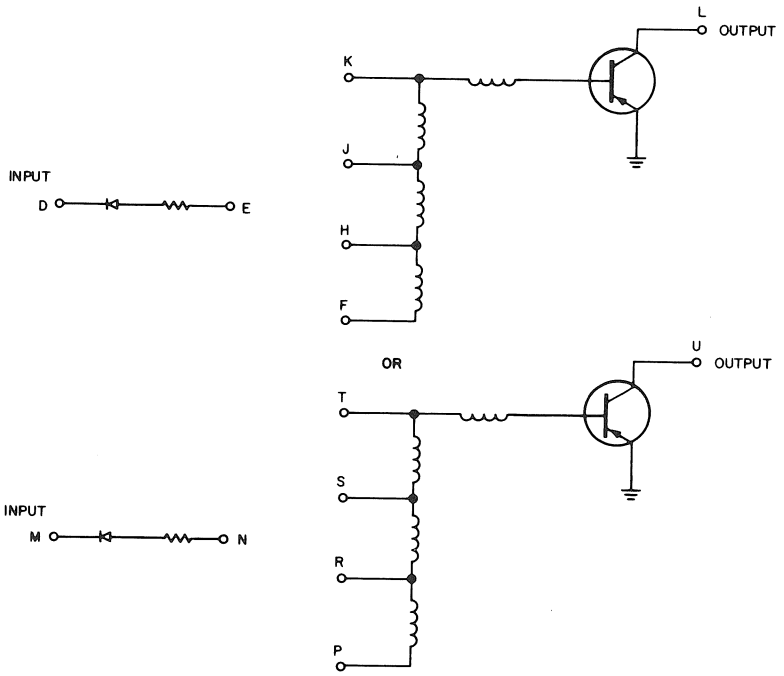

Figure 10 B310, Simplified Schematic

3.1 Check

To see if the delays are set properly, load the following program and look at B32D (MB 14 1) in the KC09.

```
LOC 00000 = 777777 Lam
    00001 = 700010 IOT CLA
    00002 = 600000 JMP 0
```

The correct signal is shown in Figure 11. If the signal appears as shown in Figure 12, the CLR pulse timing is off and the CM timing adjustments should be checked.

3.2 Set Up

All times are measured from the 50% point of the signal on probe 1 to the 50% point of the signal on probe 2 unless otherwise noted. Set up the oscilloscope in ALT MODE with gain on both

channels set to 1 V/cm and SYNC on probe 1. If the scope is not equipped for this SYNC externally with the same signal as on probe 1. See specific figures for the time/cm setting.

Program JMP0 LOC 00000 = 600000

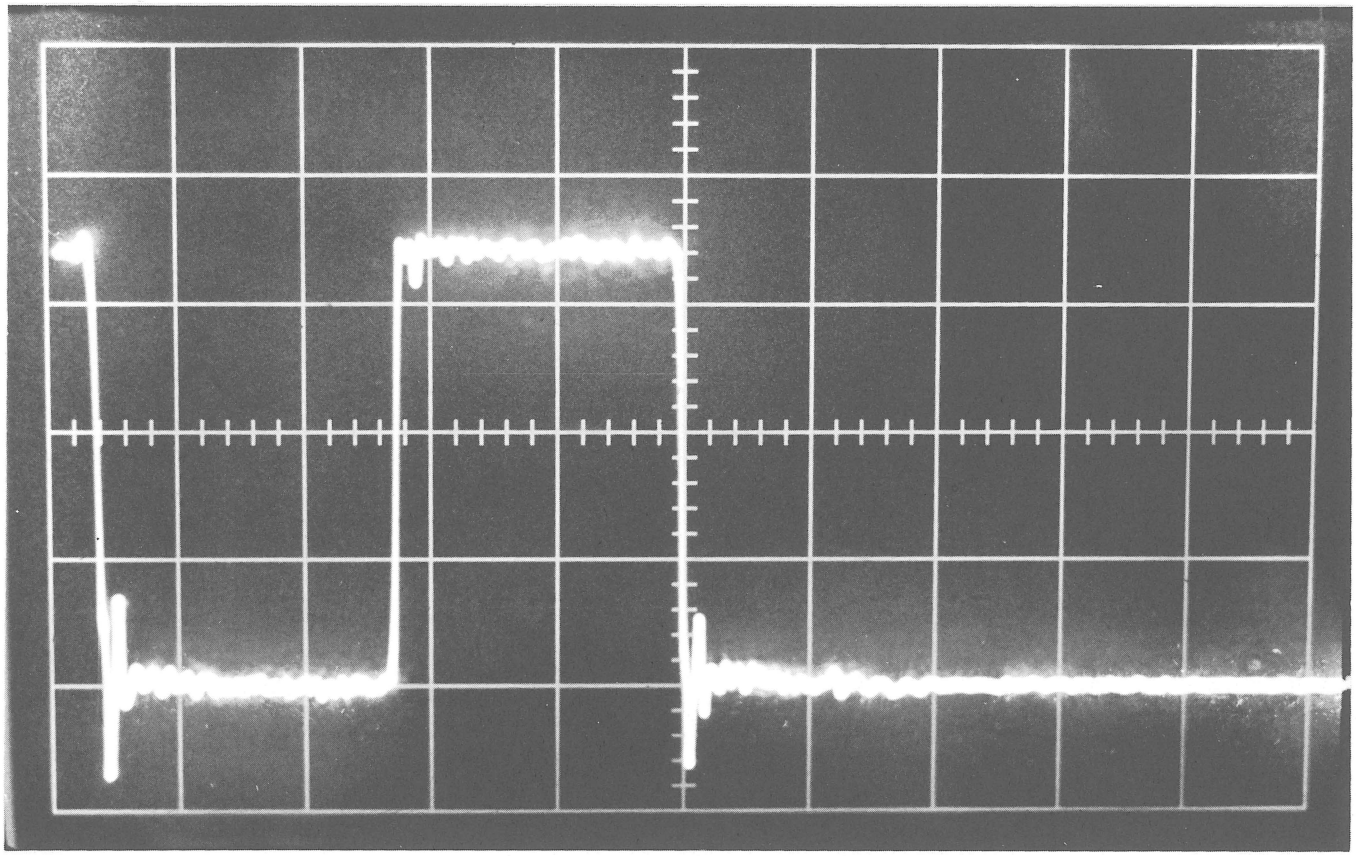

Figure 11 MB 14(1) With Correct Timing Adjustment

3.3 Procedures

3.3.1 Current Start Delay

Probe 1: C01H - CLK

Probe 2: F26U - CM current

Delay time: 26 ± 10 ns

Adjust: (see footnote 1)

See Figure 13

[1]This is only a check. There is no adjustment other then a module change and checking to see that all pertinent clamp loads are wired in and working.

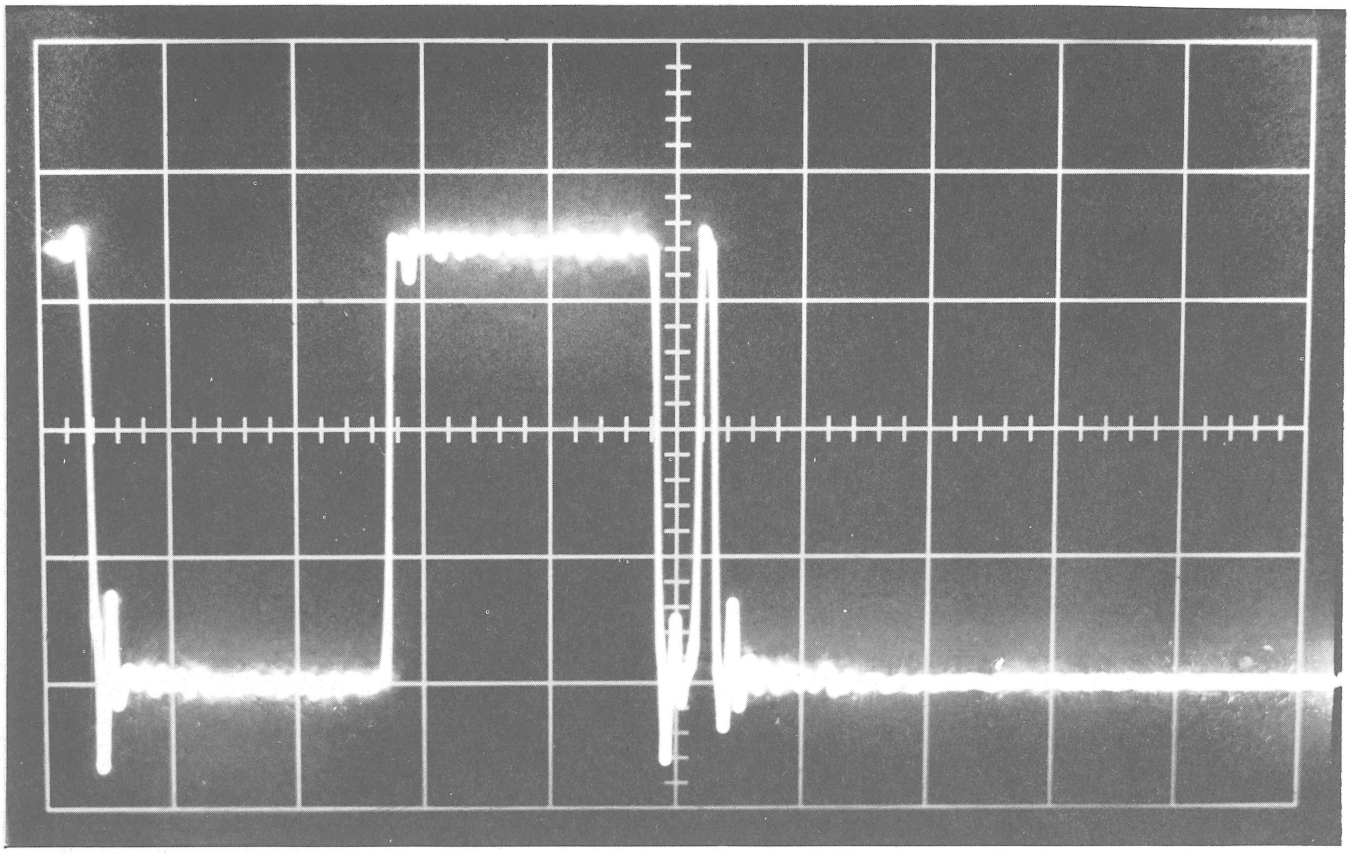

Figure 12 MB 14(1) With Incorrect Timing Adjustment

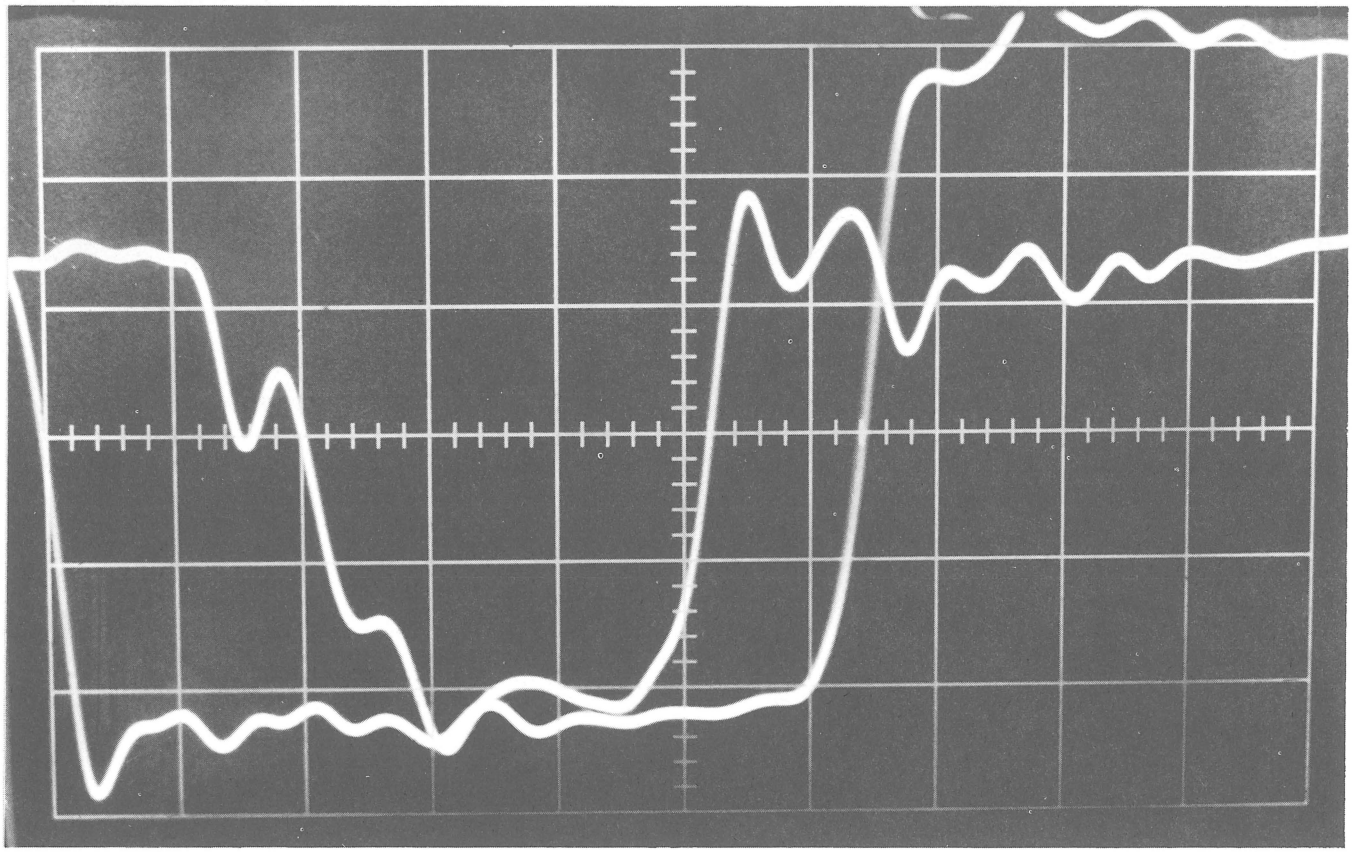

Figure 13 Current Start 20 ns/cm (0.2 μs X10) @ 1 V/cm

3.3.2 Start Delay

Probe 1: C01H - CLK

Probe 2: E27N - CM strobe D

Delay time: 100 ± 10 ns

Adjust: E29 E to F, H, J, K and N to P, R, S, T [1]

See Figure 14.

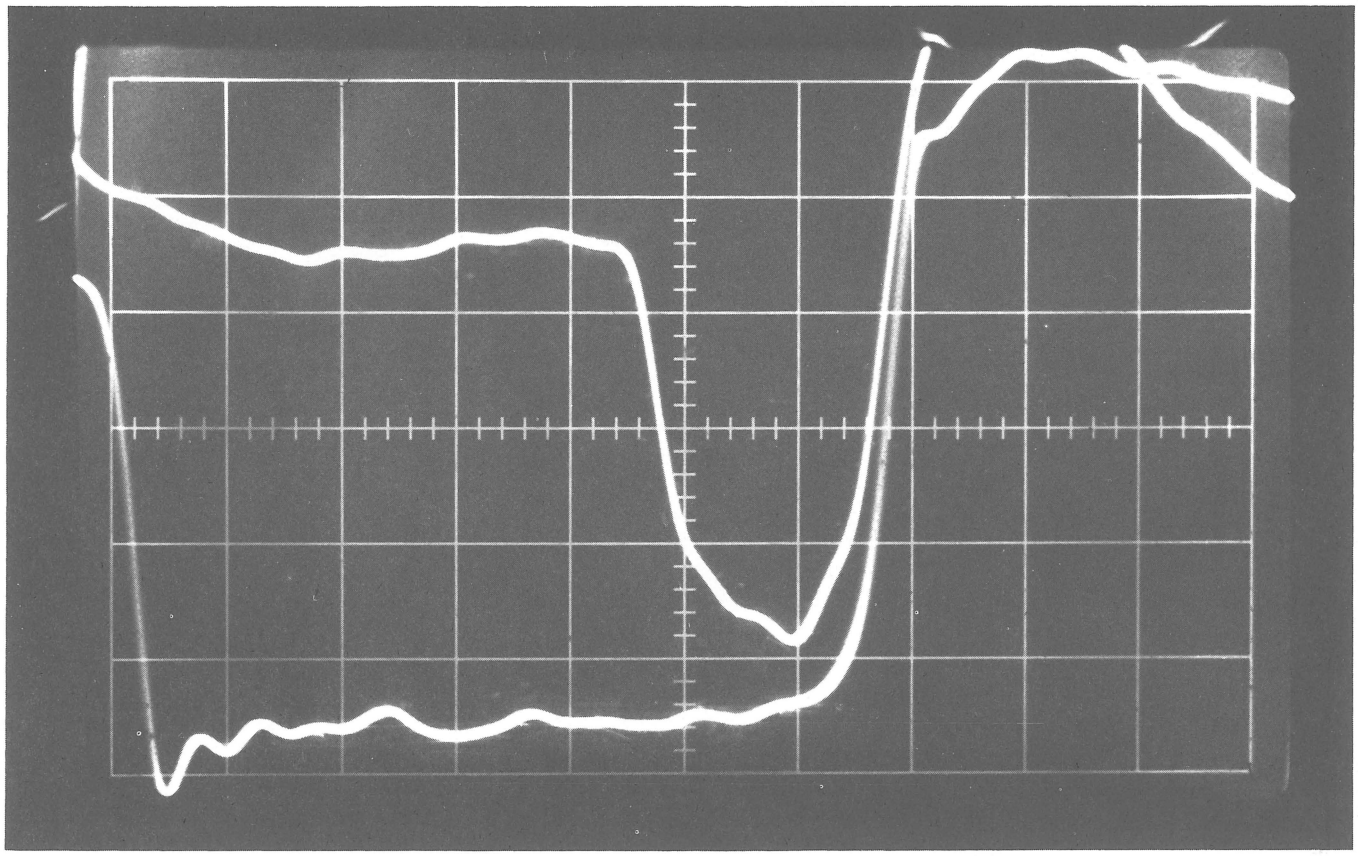

Figure 14 Start Delay 20 ns/cm @ 1 V/cm

3.3.3 Width Delay

Probe 1: C01H CLK

Probe 2: F26U CM current

Delay time: 80 + 25 - 0 ns

---

[1] Normally these delays are set to their maximum i.e., E to F and N to P. Module checking and clamp load testing may be necessary to get the specified time.

Adjust: (see footnote 1)

See Figure 15.

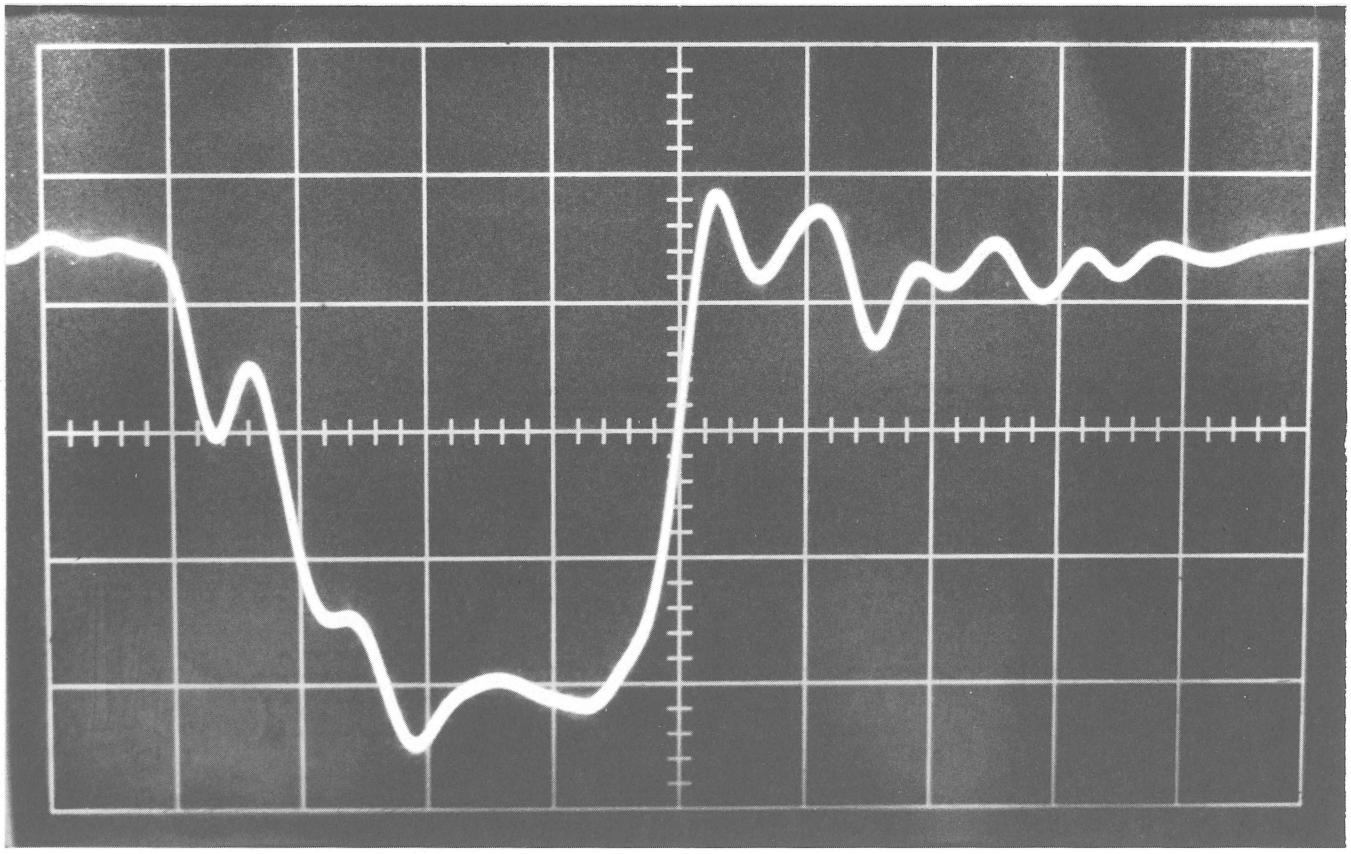

Figure 15 CM Current 20 ns/cm @ 1 V/cm

3.3.4 Loop Delay (see Section 3.3.8 for Final Check)

Probe 1: C01H CLK

Probe 2: E33M - CM strobe D.

Delay time: 212 + 0 -12 ns[2]

Adjust: E33 E to K, J, H, F

See Figure 16.

---

1 Again, this is a check only and the actual time is dependent upon circuit delays and proper module operation and clamp loads functioning. Look at probe 2 only.

2 This is the time from the first CM strobe D after CLK to the 2nd CM strobe D.

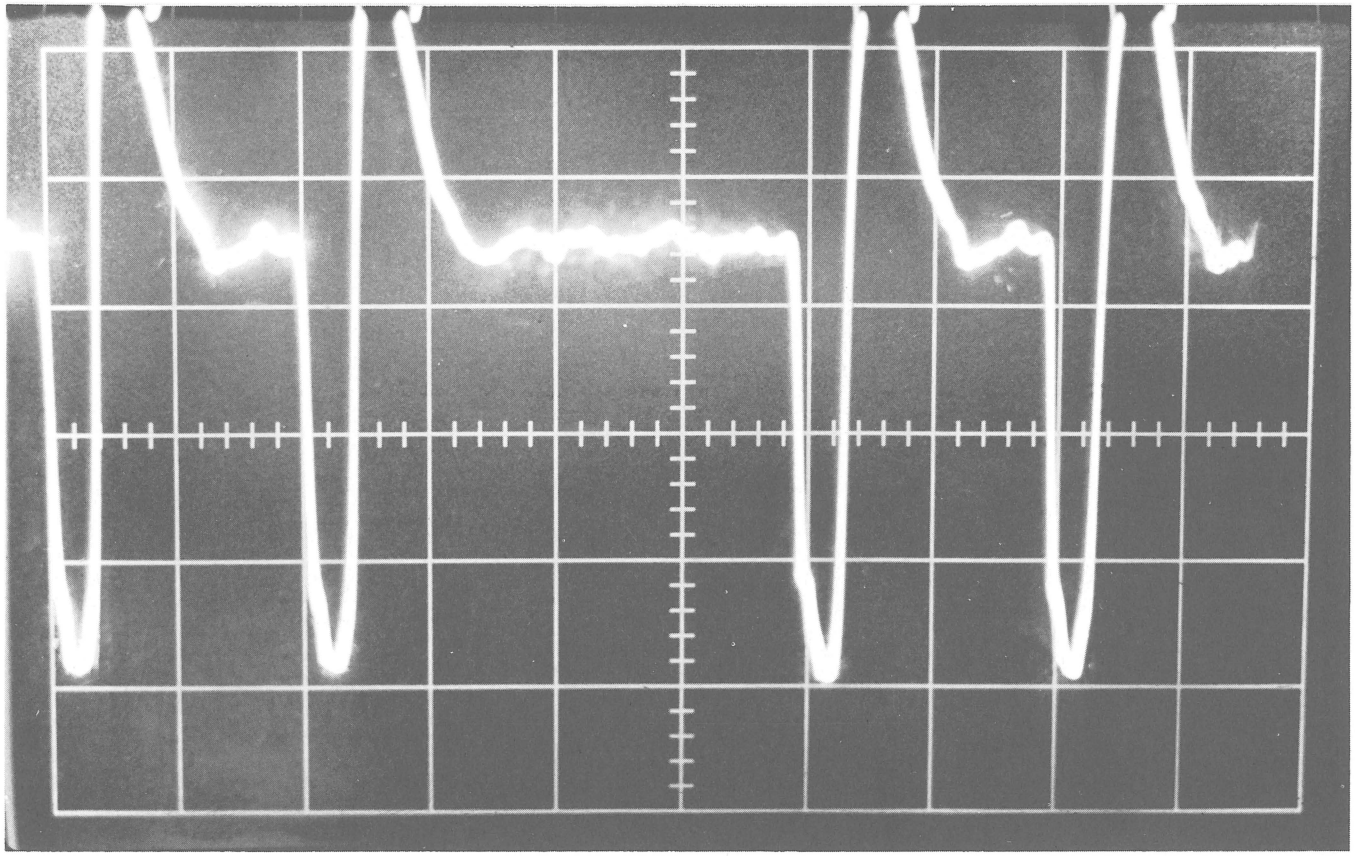

Figure 16 Loop Delay 100 ns/cm @ 1 V/cm

3.3.5 Strobe Start Delay

Probe 1: E31R - MEM strobe
Probe 2: E33M - CM strobe D
Delay time: 188 + 0 -12 ns
Adjust: F33 E to K, J, H, F
See Figure 17.

3.3.6 CLR Position Delay (see Section 3.3.8)

Probe 1: C01 H CLK
Probe 2: E20N CLR
Delay time: 488 + 0 - 12 ns
Adjust: F29N to T, S, R, P
See Figure 18.

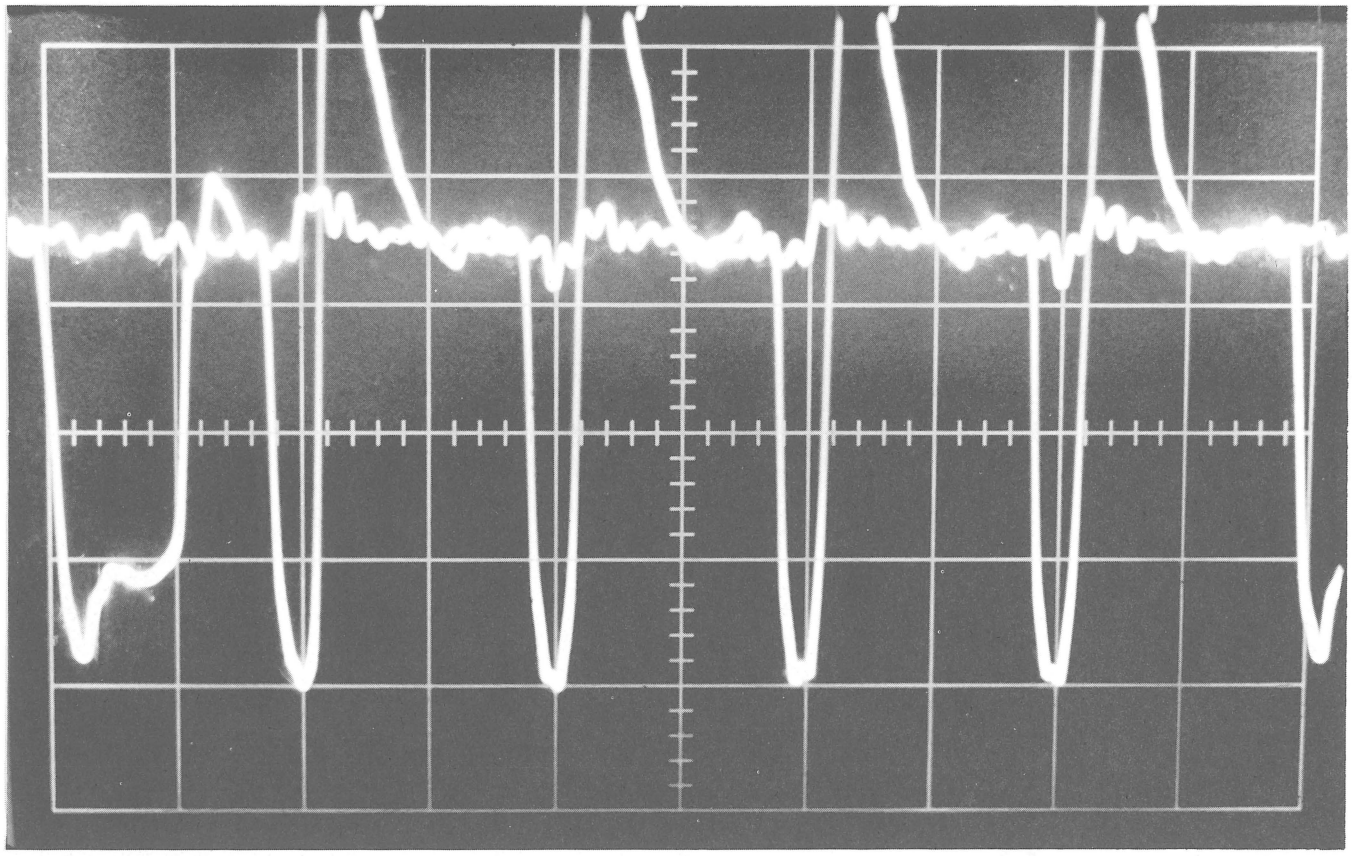

Figure 17 Strobe Start Delay 100 ns/cm @ 1 V/cm

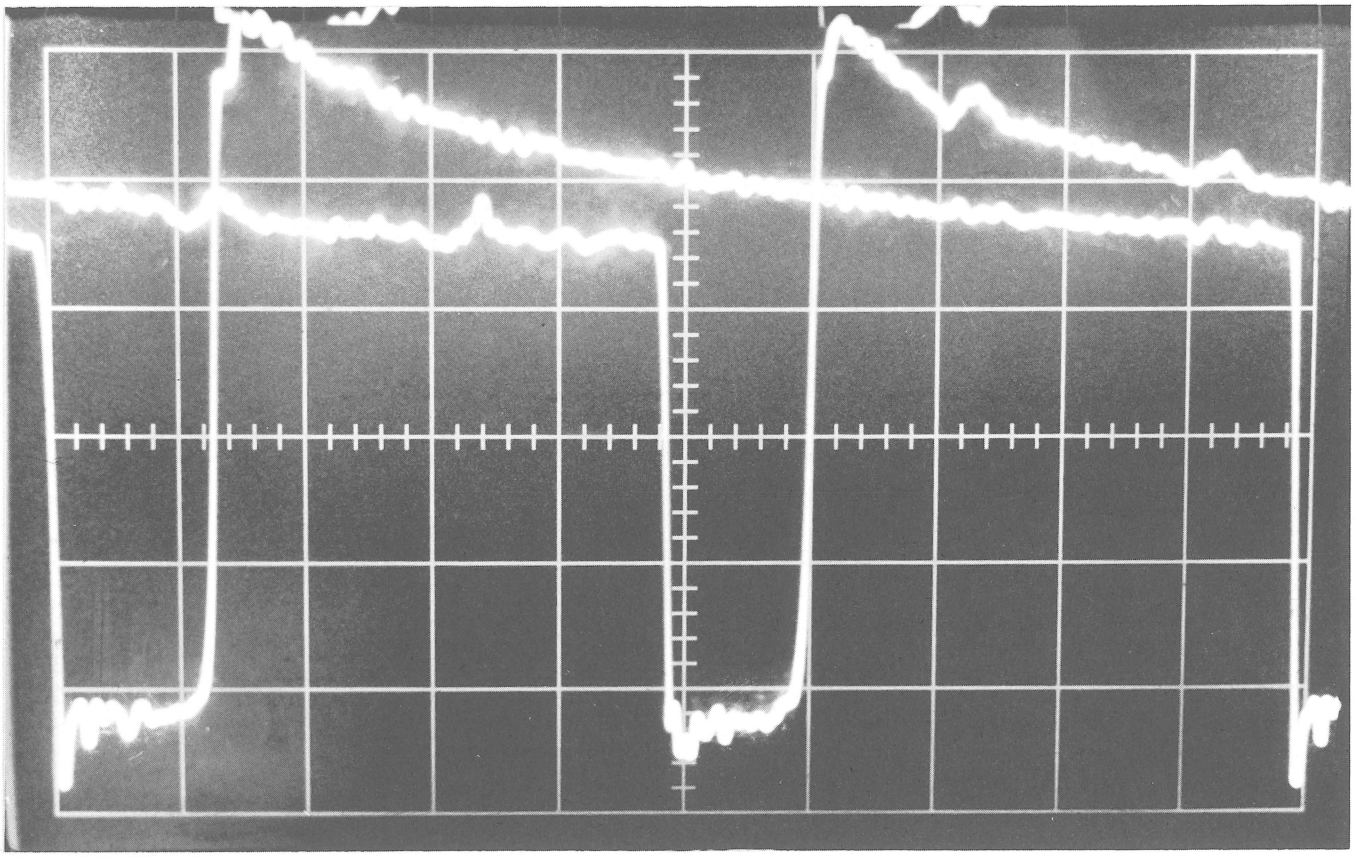

Figure 18 CLR Position 100 ns/cm @ 1 V/cm

3.3.7 Current Delay

Probe 1: C01 H - CLK

Probe 2: F26U

Delay time: Signal on probe 2 going positive at 115 ± 10 ns

Adjust: F29 E to K, J, H, F

See Figure 19

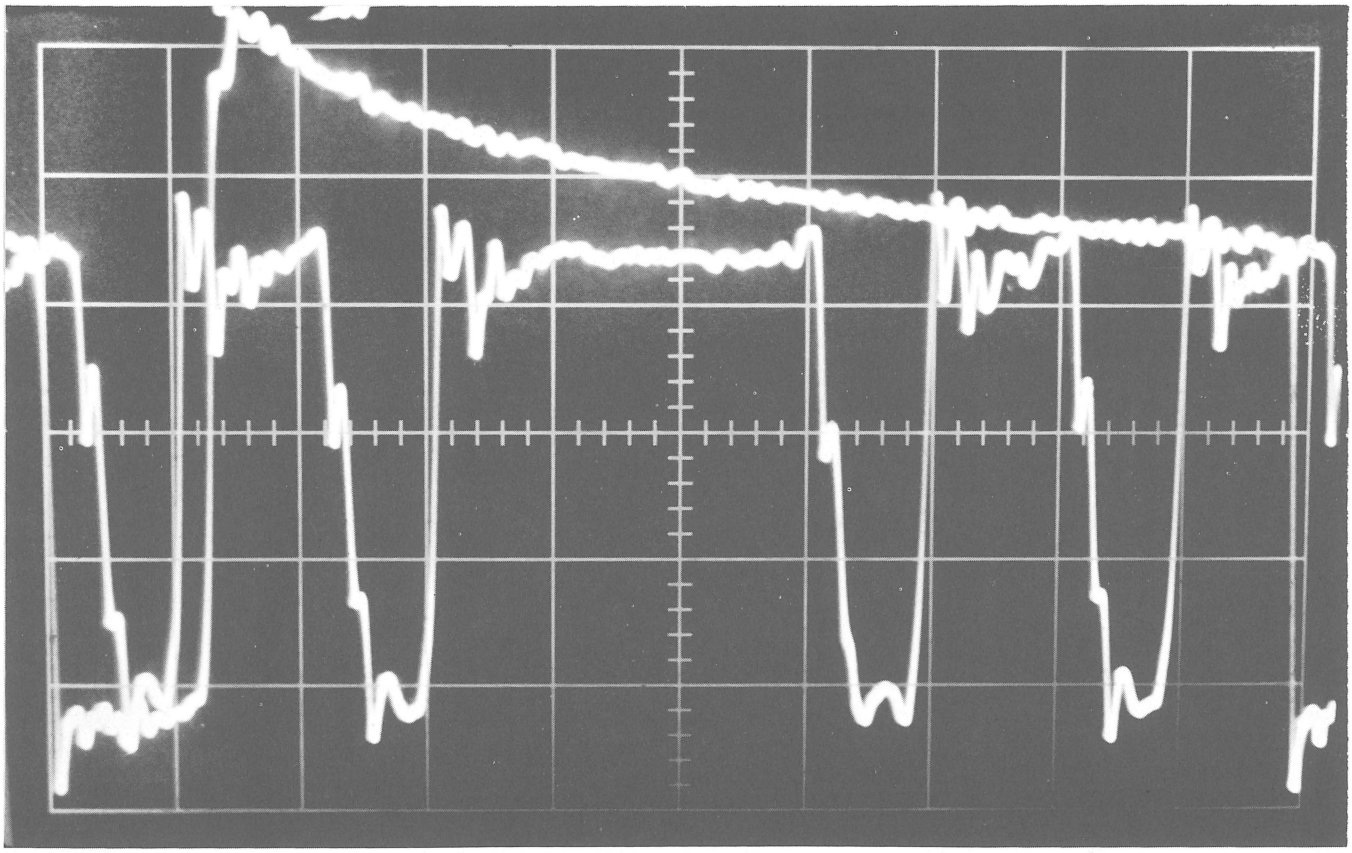

Figure 19 Current Delay 100 ns/cm @ 1 V/cm

3.3.8 System Timing - Since both CLR time and Loop time also depend upon the settings of E33 and F33 these two delays should be checked first to insure that they are set properly. E33 should be approximately 50 ns with pins E33N tied to E33P. This delay is to insure that CONT (1) will be negative at the base of F31 pin P before the pulse at pin N occurs. F33 should be about 37.5 ns with pins F33N tied to F33R. This is to insure that F31K is negative before the pulse occurs on F31J. Both these delays should be set as close as possible to their specifications to insure that Loop and CLR time can be properly set.

Check the CM strobes A, B, C, and D at the outputs of their respective P.A.s (E26D, E26N, E27D, and E27N) to make sure they are all about 40 ns wide. After changing any CM timing rerun the quick check in Section 3.1.

4. I/O ADJUSTMENTS

4.1 I/O Restart H22 KD09

4.1.1 Set Up - The setting for this delay is about 500 ns after CLK. To properly set up this delay, load the following:

LOC 0 = 700000 = IOT
LOC 1 = 600000 = JMP 0

SYNC ON and look at CLK, CP C01H, with channel 1 of the oscilloscope and at the RESTART node, CP F32D, with channel 2. Set the scope SWEEP speed for 100 ns/cm. The wave form should appear as shown in Figures 20 and 21.

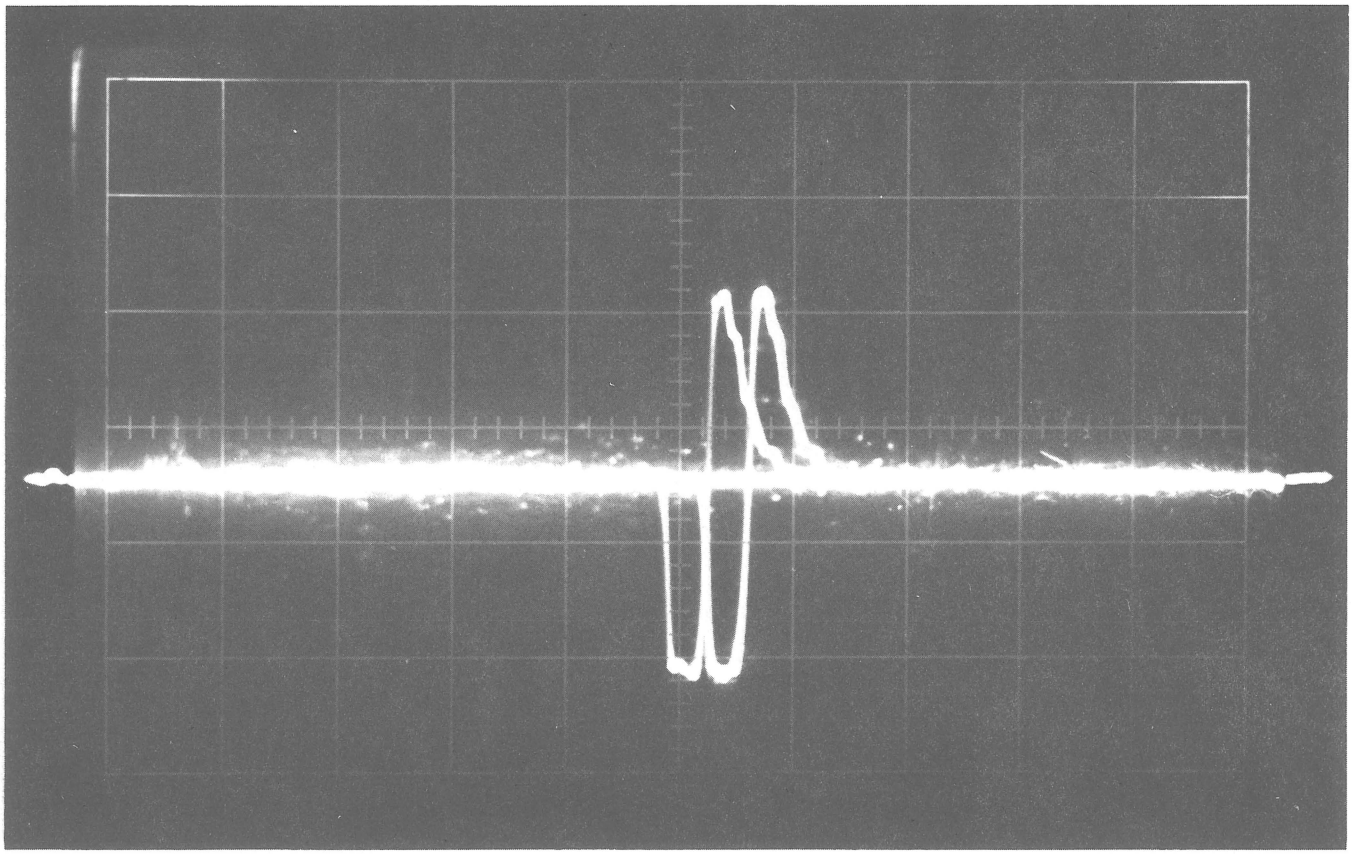

Figure 20 I/O Restart, Incorrect Set Up 100 ns/cm @ 1 V/cm

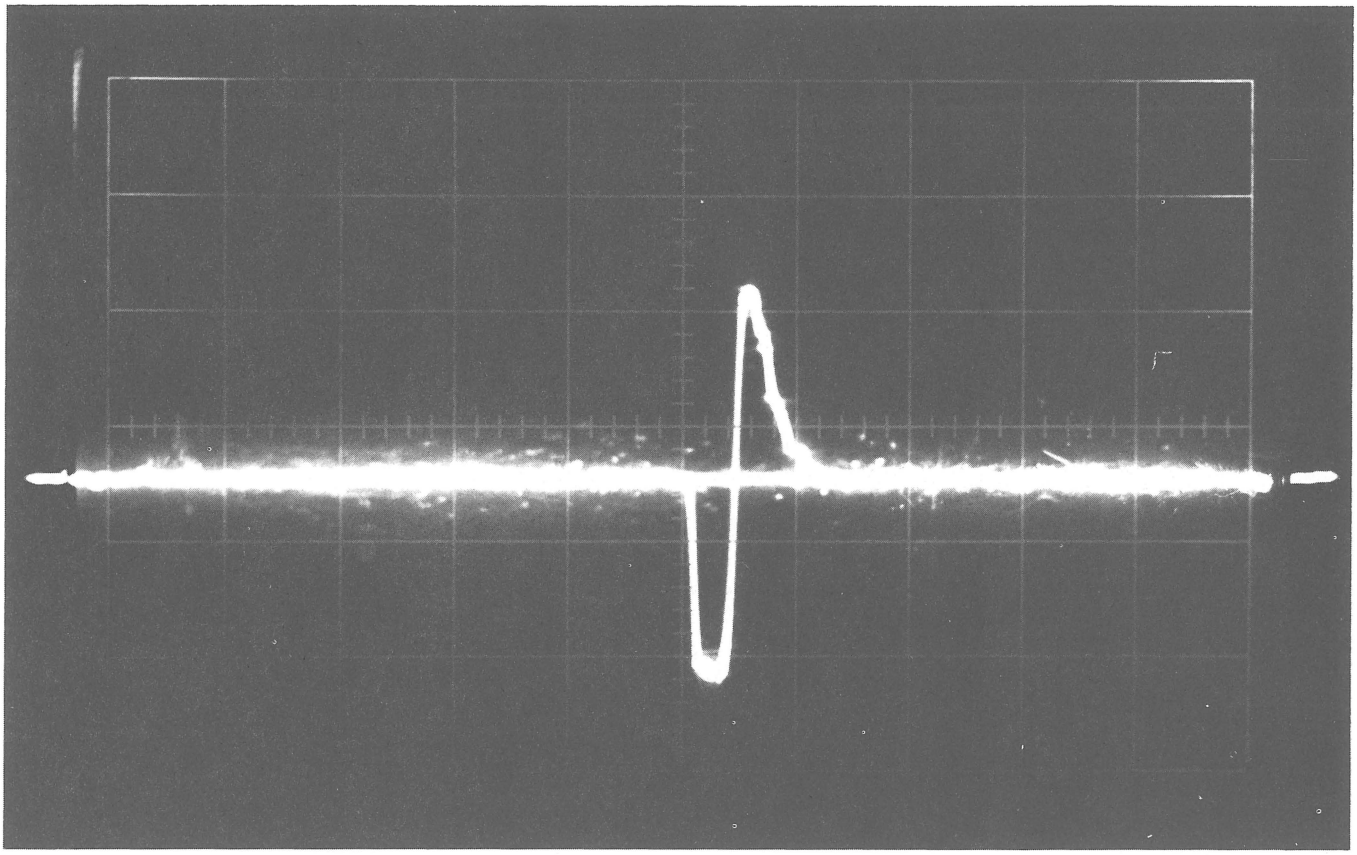

Figure 21 I/O Restart, Correct Set Up 100 ns/cm @ 1 V/cm

4.1.2 Procedure - Adjust H22, B201, in the I/O until the leading edge of the I/O RESTART pulse coincides with the leading edge of the MEM strobe pulse both of which will be visible at F32D. This now insures that CM strobes will occur at the proper times when restarting from an IOT instruction.

4.2 EAE Restart E40 KD07

4.2.1 Set Up - To set up the EAE RESTART delay, load the following:

LOC 0 = 640000 = EAE NOP
LOC 1 = 600000 = JMP 0

4.2.2 Procedure - SYNC ON and look at input I/O RESTART (H18T) in the I/O with channel 1 of the oscilloscope, and at CM strobe D (E33M) in the CP with channel 2. Set the SWEEP speed to 100 ns/cm. Position the SWEEP on the scope with the horizontal position knob until the CM strobe D pulse (which occurs immediately after the input I/O RESTART pulse) goes negative 110 ns before the center on the scope mask. Then, without disturbing the SWEEP horizontal position, remove probe 2 from

E33M and place it on CLK (C01H) in the CP. Adjust E40 in the I/O until the next CLK pulse after input I/O RESTART goes negative at the center line of the scope. This now insures that EAE RESTART is causing the next CM strobe D to occur 110 ns before the next CM CLK pulse, which will maintain the proper CM timing. See Figures 22 and 23. See PDP-9 tech tip 17.

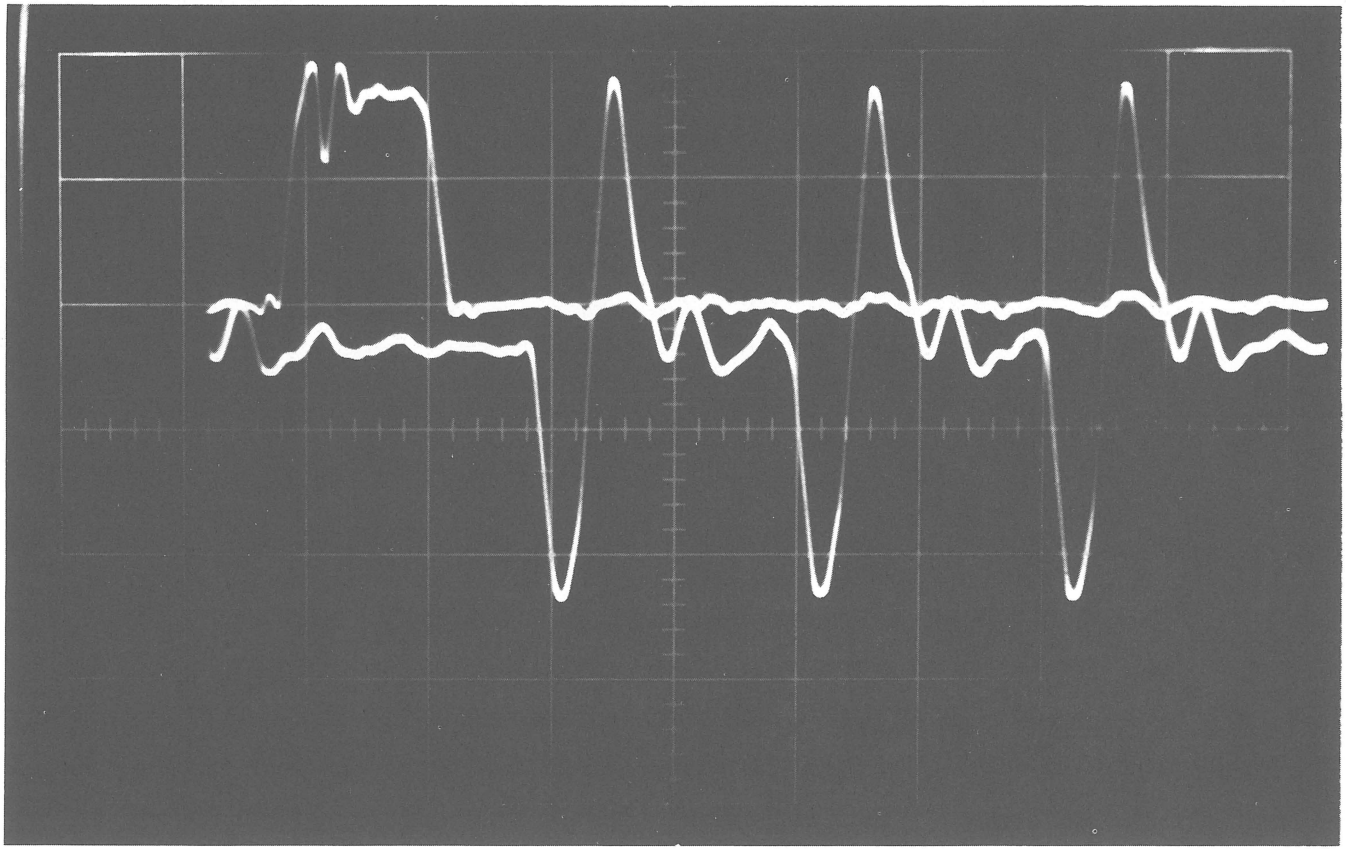

Figure 22 Set Up for EAE Restart 100 ns/cm @ 1 V/cm

4.3 Power Fail

If the machine is supplied with a power fail unit, option type KP09A, measure the -15V with a scope at pin J32B of the I/O for reference. Shut machine power OFF. Set the MARGINS switch on the console to -15V. Put I/O MARGIN switch 1 on. With probe 1 of the scope look at pin J32B in the I/O. This is just -15V dc. Adjust the MARGIN supply so that the measured voltage is down 1.5 to 1.75V from the nominal -15V that measured earlier. Put scope probe 1 on pin J32F in the I/O. Observe a -3V signal. Adjust the W505 until the level just switches to GND. Set the MARGIN supply to 0 (i.e. the nominal -15V) and check to see that the level returns to -3V. Shut off power and turn all MARGIN switches to OFF.

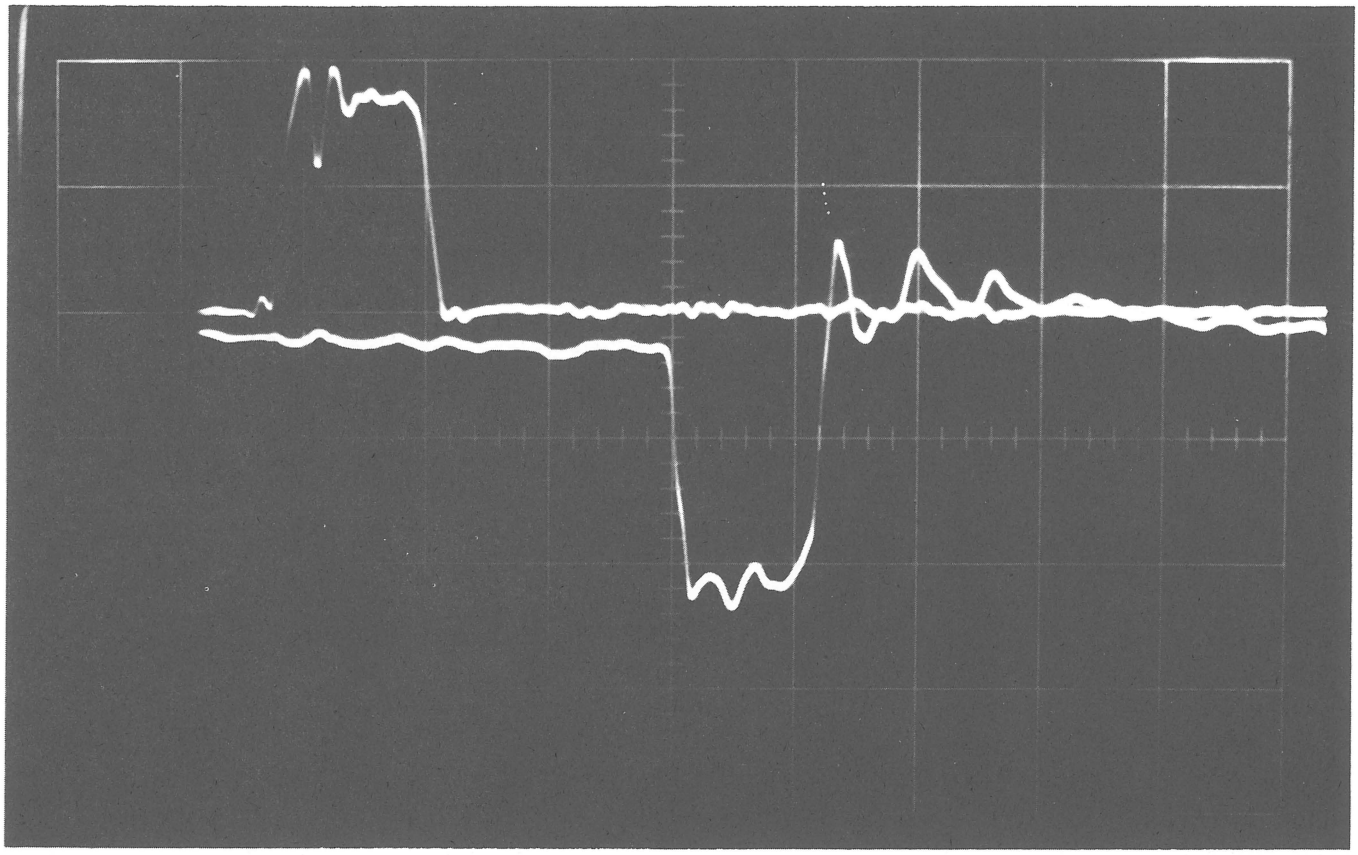

Figure 23 EAE Restart 100 ns/cm @ 1 V/cm

NOTE

Some early PDP-9s required a module modification before the power fail would operate correctly. See tech tip 11 for the modification and PDP-9 tech tip 25.

4.4 POWER OK DETECTOR

Turn machine power to OFF. Turn the MARGINAL CHECK switch on the front console to -15 V. Put CP MARGIN switch 2 ON. Turn power "on" and adjust the margin supply for -2.5V (i.e. 7.5V). SYNC and look at pin J23M in the CP with probe 1. Adjust the W505 until positive pulses just appear. Set the MARGIN VOLTAGE at 2.0V and check that the pulses disappear. Shut power off and turn all MARGIN switches to OFF.

4.5 PC09 Reader Timing

4.5.1 Set Up - Make a tape loop of alternate 1s and 0s (i.e. all 8 channels of 1s, then all 8 channels of 0s). Be sure tech tip 14 has been installed in the G904. Also install PDP-9 ECO's 212 and 237 if they have not already been installed. Put the following program in core:

```
LOC  100/  RSA     =  700104
           RSF     =  700101
           JMP -1  =  600101
           JMP -3  =  600100
```

Place the tape in the reader and press START. SYNC and look at the output of each channel at I/O pins A17D, E, F, H, J, K, L and M. Adjust the G904 module so that you have a 50% duty cycle. The best way to see the full duty cycle is to uncalibrate the SWEEP speed so that 1 full cycle is equal to 10 cm across the face of the scope. Now adjust the G904 so that you have a 50% duty cycle (i.e. ON for 5 cm then OFF for 5 cm). The allowable deviation is ±5% between channels.

4.5.2 Procedure - SYNC and look at the strobe clock pin E12J in the I/O with probe 1. Look at any one of the channel outputs with probe 2. Refer to Figures 24 and 25. Strobing occurs during the UP clock (positive transition) of the strobe pulse which should be positioned so that it occurs in the center of the data. To position strobe, loosen the 4 screws that hold the stepping motor. Rotate the motor to position strobe then tighten the 4 screws. If it is impossible to position strobe by rotating the the motor, loosen the sprocket wheel and rotate it slightly. Tighten the sprocket wheel and set the final position of strobe by rotating the motor.

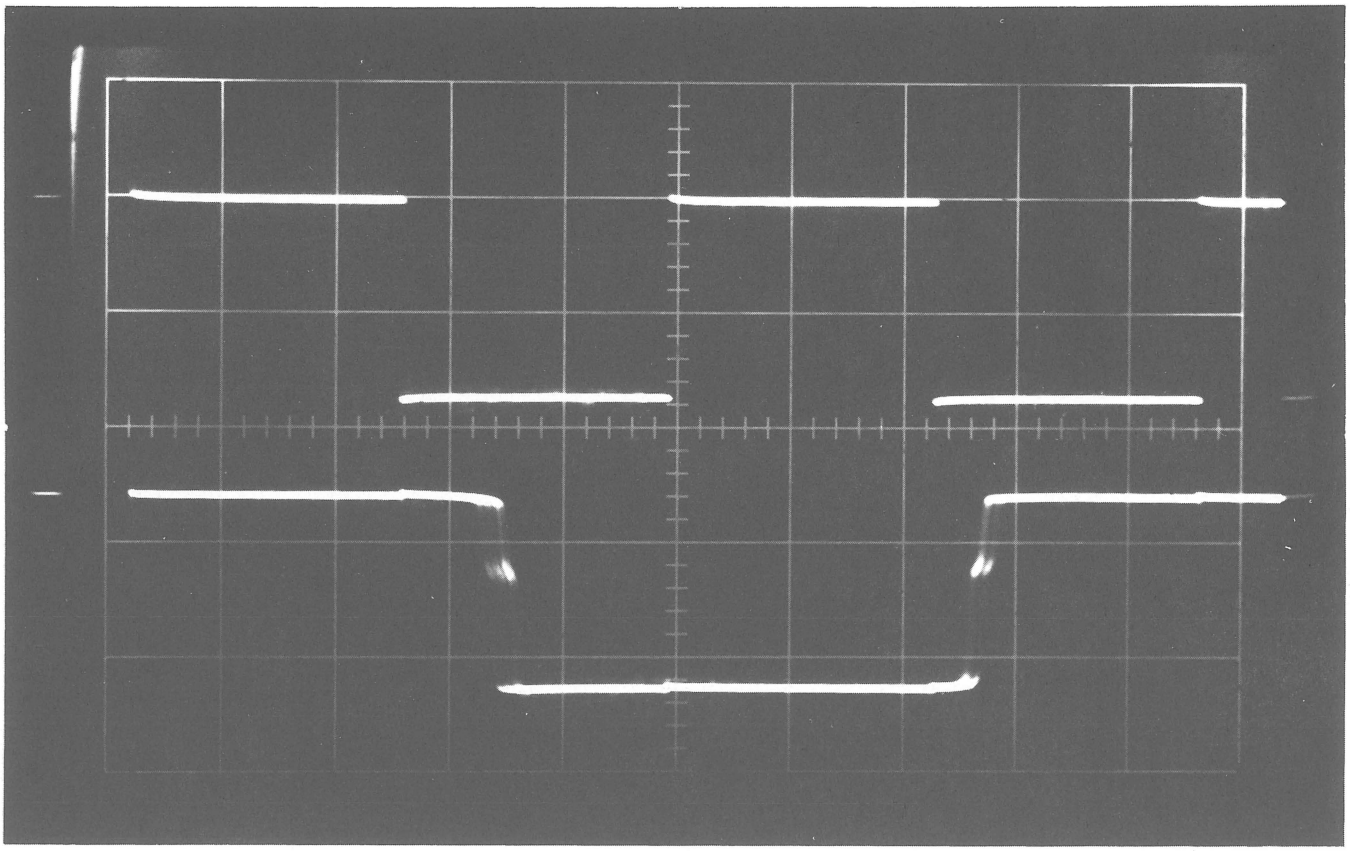

Figure 24 Reader Strobe Timing Adjustment

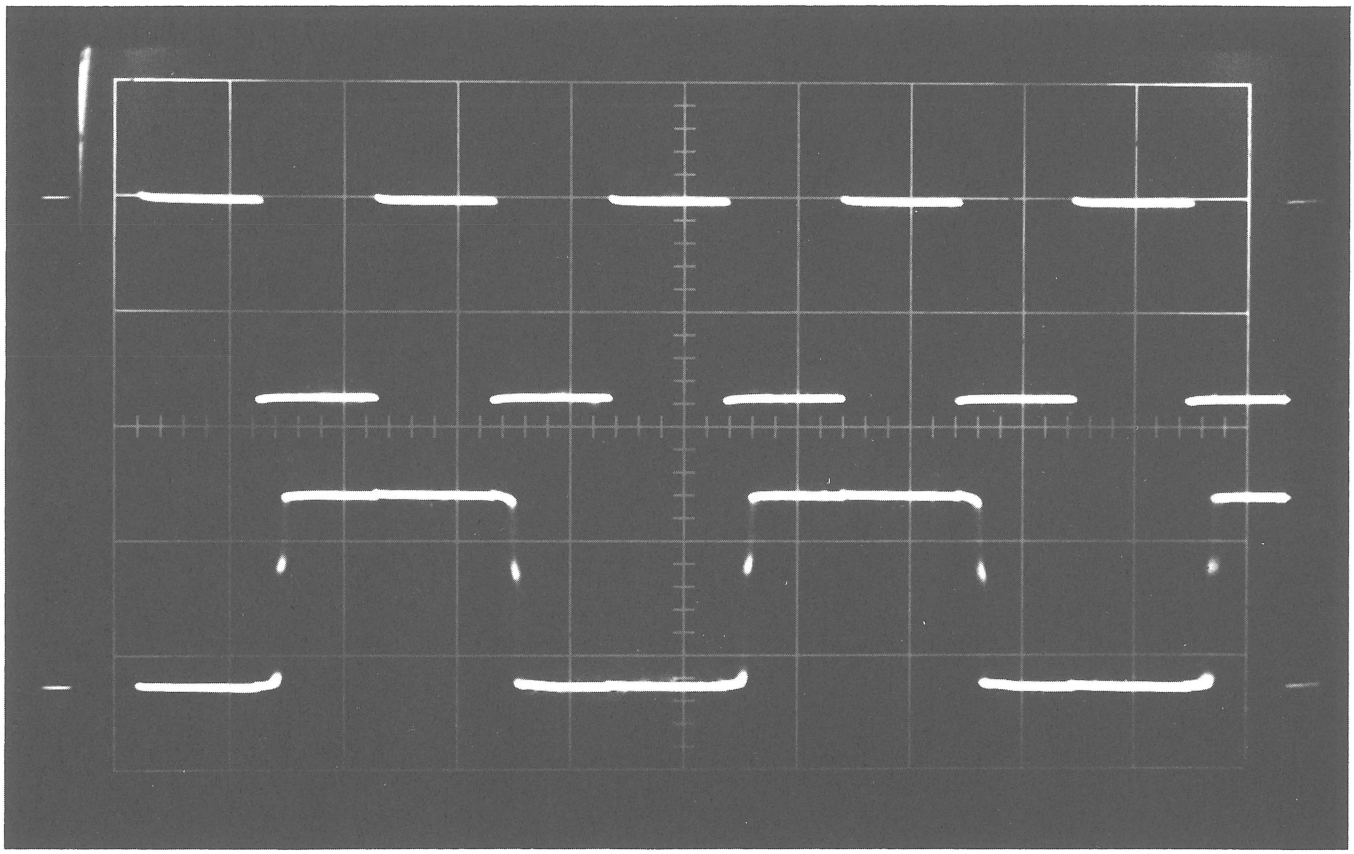

Figure 25 Reader Strobe Timing Adjustment, 50% Duty Cycle

Digital Equipment Corporation
Maynard, Massachusetts

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