THEORY OF OPERATION AND MAINTENANCE MANUAL 9003

MICROCOMPUTER TERMINAL SYSTEM

Zentec Corporation

ZENTEC Part No. 88-407-01 Rev. B

THEORY OF OPERATION
AND MAINTENANCE MANUAL
9003
MICROCOMPUTER TERMINAL SYSTEM

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TABLE OF CONTENTS PAGE

TABLE OF CONTENTS

WARRANTY

All ZENTEC products are warranted against defective materials and workmanship for 90 days from date of shipment. Any questions with respect to warranty should be referred to your ZENTEC Sales Representative.

All requests for repairs should be directed to the ZENTEC factory. This will assure the fastest possible service.

SECTION 1

GENERAL DESCRIPTION AND SPECIFICATIONS

FIGURE 1-1 THE 9003 MICROCOMPUTER TERMINAL SYSTEM

SPECIFICATIONS

CHARACTERISTIC	VALUE
SYSTEM	
DIMENSIONS	
CRT DIPLSAY CONSOLE	21 IN. W * 16 IN. H * 18 IN. D
KEYBOARD	20 IN. W * 3.5 IN. H * 13 IN. D
FINISH	TEXTURED VINYL, LIGHT BEIGE COLOR
POWER REQUIREMENTS	115V AC +/- 10%: 220V 50 HZ OPTIONAL 100V 60 HZ AND 100V 50 HZ OPTIONAL
MICROPROCESSOR	
TYPE	INTEL 8080 GENERAL PURPOSE PARALLEL PROCESSOR WITH INTERRUPT CAPABILITY; INPUTS AND OUTPUTS TTL COMPATIBLE.
WORD SIZE	8 BITS
INSTRUCTION SET	111
MEMORY ADDRESSING	CAN ADDRESS UP TO 64K BYTES DIRECTLY
MEMORY	NOTE: MAXIMUM COMBINED CAPACITY OF ROM, PROM AND RAM CANNOT EXCEED 65,536 BYTES
ROM/PROM	
CAPACITY	UP TO 10,250 BYTES
TYPE	ROM: 2048 X 8, AMI S9996 OR EQUIVALENT PROM: 256 X 8, INTEL 1702, 1702A, OR EQUIVALENT
RAM	
CAPACITY	UP TO 4096 BYTES CAN BE INSTALLED IN STANDARD SYSTEM, UP TO 60K BYTES WITH ADDITION OF OPTIONAL RAM BOARDS (2048 BYTES ARE USED FOR VIDEO DISPLAY IN A STANDARD SYSTEM)
TYPE	2048 X 1 DYNAMIC, NATIONAL MM5262, OR EQUIVALENT

SPECIFICATIONS

CHARACTERISTIC	VALUE
KEYBOARD	
OUTPUT CODE	128 ASCII AND 43 SPECIAL CODES
ALPHANUMERIC	96 ASCII CHARACTERS, UPPER AND LOWER CASE
CONTROL	32 ASCII BASIC, 32 SPECIAL, AS MODIFIED BY CTRL AND SHIFT KEYS
NUMERIC	10 SPECIAL CODED NUMBERS AND ONE SPECIAL CODE FOR DECIMAL POINT
CRT DISPLAY	
CRT	
SIZE	9 IN. X 11 IN., 15 IN. DIAGONAL
PHOSPHOR	P4 (WHITE)
SCAN METHOD	NONINTERLACED, RS-330, 525 LINE COMPATIBLE
SCAN RATE	60 FIELDS PER SECOND
CHARACTER FORMAT	
DISPLAY MATRIX	10 X 10 DOT MATRIX OF WHICH 7 X 9 MATRIX IS USED FOR CHARACTER FORMATION
SIZE	0.2 IN. HIGH BY 0.09 IN. WIDE
PAGE FORMAT	80 CHARACTERS ON EACH LINE, 25 LINES ON FULL SCREEN (DEFINED AS ONE PAGE). NOTE: OF THE 25 LINES, 24 ARE OPERATOR ACCESSIBLE, THE 25TH IS USED ONLY BY THE MICROPROCESSOR
TELECOMMUNICATIONS INTERFACE	
TYPE	RS-232C, ASYNCHRONOUS, FULL OR HALF DUPLEX
TRANSMISSION RATE	SELECTABLE AT 110, 300, 1200 OR 2400 BAUD; THE 2400 BAUD RATE CAN OPTIONALLY BE CHANGED TO 4800 OR 9600 BAUD
CHARACTER SIZE	8 DATA BITS, WITH ONE START AND ONE OR TWO STOP BITS
PARITY	ODD, EVEN OR NONE

1.0 GENERAL INFORMATION

The ZENTEC 9003 Microcomputer Terminal System is a new generation data handling and processing device that can function either as a complete standalone computer system or as an interactive intelligent data terminal. It is a general purpose system that can be used for text or forms generation and editing, or can be programmed for other data processing or communication tasks.

The 9003 system consists of a desktop CRT display console and separate keyboard from which data can be entered by the operator for display on the CRT screen. The system also can be interconnected via a telecommunications line to a host computer which can send data for processing and display on the CRT screen, or receive data from the 9003 system. A variety of peripheral devices can be connected to the system to expand its data handling capabilities or store programs and data for a particular processing application. Typical peripheral devices are a hard copy printer or auxiliary memory devices such as a disk, cassette, or reel-to-reel tape drive.

The basic 9003 system components are the keyboard, CRT display, and telecommunications interface electronics all functionally organized around a microcomputer that controls data communications into and out of the system and performs all internal data processing operations. The microcomputer and other components are described in more detail in paragraph 1.3.

1.1 APPLICATIOMS

The ZENTEC 9003 Microcomputer Terminal System can be used in two basic ways:

* as a standalone computer system (see Figure 1-2), or

* as a general purpose or dedicated data terminal (see Figure 1-3).

Every key on the keyboard is under software control except the RESET, SHIFT and ALL CAPS keys. The user (through programming) has complete control over the functions performed by the 9003 system. As a standalone computer, the 9003 system can be used as a small general purpose computer, or it can be programmed and dedicated to a specific task. It can be equipped with auxiliary memory and input/output devices (see Figure 1-4) as required to support its computing functions. As a terminal, the 9003 system can be used with a host computer for data entry or display purposes, interactive on-line communications with the computer, or be programmed to perform data preprocessing prior to its transmission to the host computer. It can be connected to the host computer via a modem and an RS-232C telecommunications line, or directly. When used as a terminal, it can manage an auxiliary buffer memory also (see Figure 1-4).

1.2 FUNCTIONAL DESCRIPTION OF THE SYSTEM

Functionally, the 9003 system consists of the microcomputer and associated input/output devices (see Figure 1-4). The microcomputer itself consists of an integrated circuit microprocessor, timing and control circuitry and ROM/PROM and RAM memory. These circuits, along with the microprocessor input/output interface circuits, are mounted on three circuit boards located inside the CRT display console.

All basic functions of the 9003 system are under the control of the microcomputer. This software-oriented organization of the system is the reason for its applications versatility. One or more operating programs available from ZENTEC can be stored in the microcomputer memory and programs can generally be changed. Additional user programs can be installed into the microcomputer by the interchange or addition of memory circuits.

1.3 THE MICROCOMPUTER

The microcomputer, Figure 1-4, is constructed around a general purpose microprocessor that can handle 8-bit words, has a repertoire of 111 instructions, and can address up to 64K bytes of memory. It connects to a direct memory access data input/output bus to which the keyboard, the CRT display, and the telecommunications interface electronics are connected. These circuits can perform their functions independently, while interfacing with the microprocessor or the memory on a priority basis. Optional interface circuits, peripheral devices available from ZENTEC, or devices added by the user can be connected to the I/O bus to operate in accordance with the priority discipline. Thus, the system can be expanded in a modular manner.

1.4 THE 9003 MICROCOMPUTER MEMORY

The basic microcomputer memory consists of read-only (ROM) and read/write semiconductor integrated circuits (RAM). The read-only segment of the memory (usually both ROM and PROM) contains the system operating program(s). The read/write segment (RAM) is used to store video display information that is repeatedly read out of the memory to refresh the CRT display screen, and can also be used to store microcomputer programs or other data, if the application requires it. Figure 1-5 shows a diagram of the standard 9003 microcomputer memory.

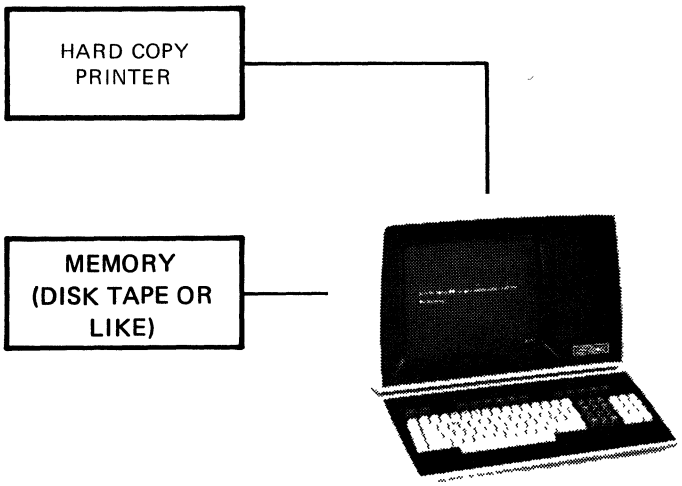


FIGURE 1-2 THE 9003 SYSTEM INSTALLATION FOR TYPICAL STANDALONE COMPUTING PURPOSES

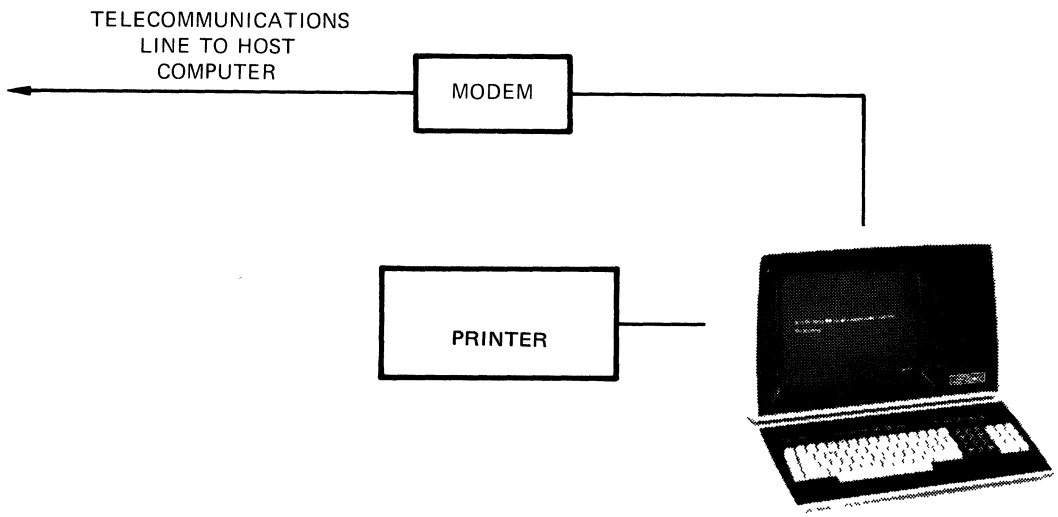


FIGURE 1-3 TYPICAL 9003 SYSTEM TELECOMMUNICATIONS INSTALLATION

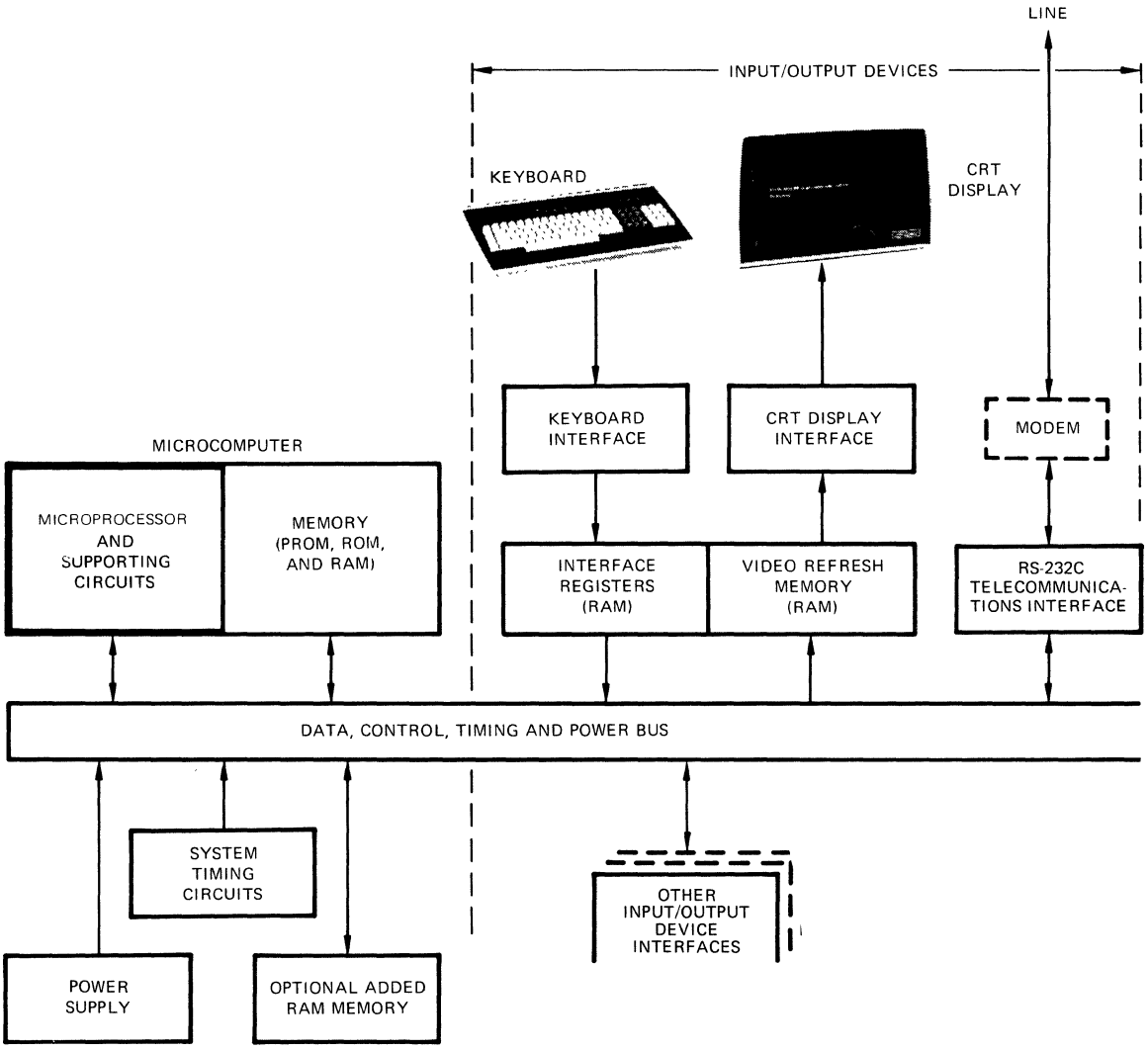


FIGURE 1-4

The exact size of the memory depends on the size of the microcomputer programs stored in the system, and the amount of video display memory used. In the standard system, space is provided for the installation of 10,250 8-bit bytes of ROM and/or PROM program memory and up to 4096 8-bit bytes of RAM memory (part of which is available for optional programs or expansion of video display information storage). With the addition of optional circuit boards, the total memory capacity can be expanded to 65,536 8-bit bytes. The additional memory is read/write RAM and can be used for additional program storage, video display information storage or telecommunications data storage.

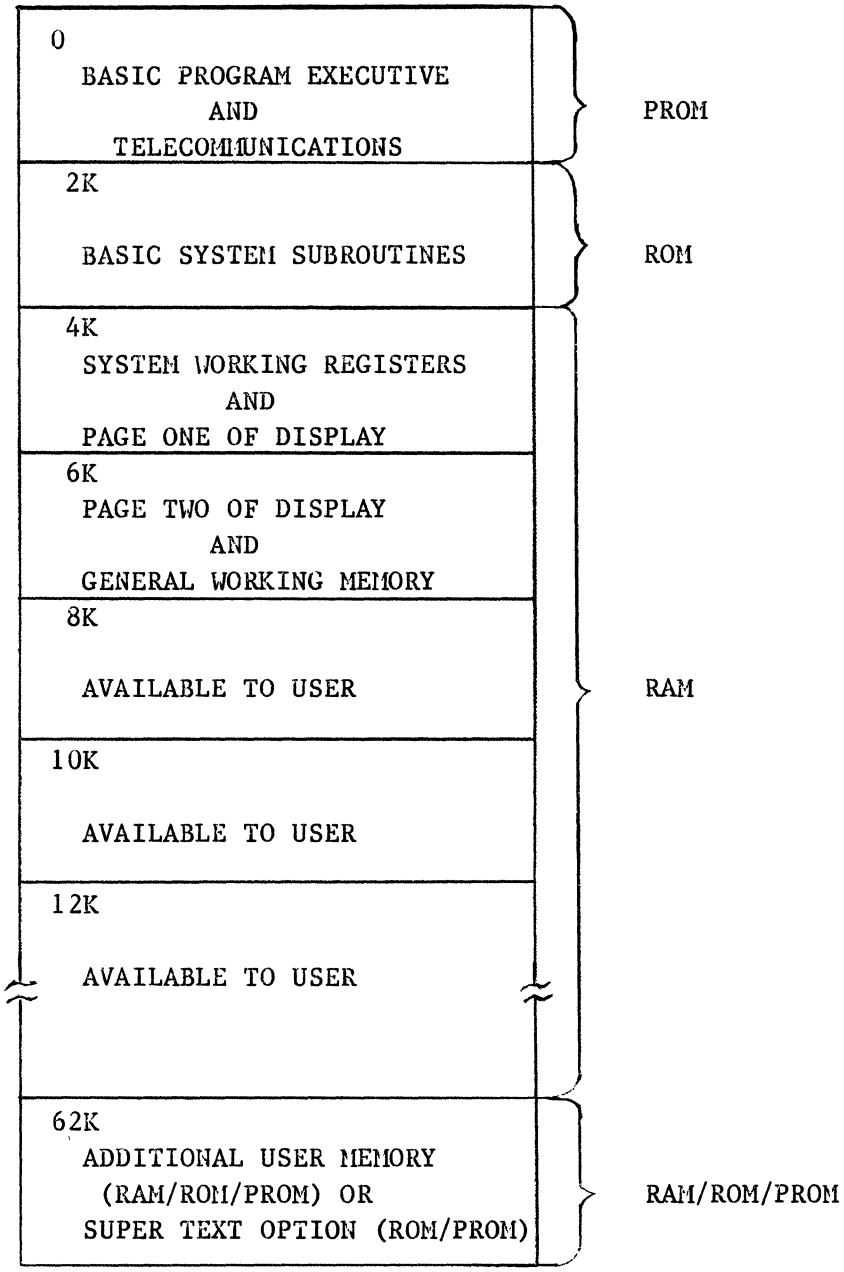


FIGURE 1-5 DIAGRAM OF STANDARD 9003 MICROCOMPUTER MEMORY

1.5 INPUT/OUTPUT INTERFACE CIRCUITS

Each of the 9003 system input/output devices is connected to the system bus through an interface circuit (and generally a RAM interface register). These circuits change the data signals from external devices to a common form compatible with the memory or microprocessor. The keyboard and CRT display access a location in the RAM segment of the memory, other optional peripheral devices can access the remaining parts of the RAM by addressing any of these locations. Some of the optional input/output interface circuits are designed to interface directly with the microprocessor.

1.6 PROGRAMS

The 9003 microcomputer terminal is controlled by programs which are executed by the microprocessor. The programs are stored as either firmware in ROM or PROM or as software in RAM. Because RAM is volatile, software programs must be loaded into the 9003 either via the RS-232C interface or from some auxilliary storage device such as a diskette or cassette. Both firmware and software programs can be either ZENTEC or user written.

The basic 9003 system includes a set of firmware routines which perform the basic control and processing function. Optionally, a comprehensive set of firmware and software programs are available to supplement the basic firmware.

The basic firmware consists of an executive, pointer address lists, and a set of closed subroutines. During normal operation, the executive uses the keyboard input to access the pointer address lists and transfer control to the appropriate subroutine which causes the terminal to perform the required function.

The following programs are currently available from ZENTEC:

1. Basic Firmware (included in basic system)
2. Second Page Option
3. Extended Text Editor
4. TCOM IV
5. ZIM
6. Disk Cataloger
7. Debug
8. ZAM

1.6.1 BASIC FIRMWARE

The Basic Program comprises the essential firmware used to operate the 9003 system. This program provides fundamental text and forms handling functions and serves as a base for extending system capabilities with supplemental programs - either those described below or application programs created by the user.

The Basic Program is for off-line operations involving only the keyboard and the screen. There are two types of operations that can be performed with the Basic Program: generating or editing of text, while viewing it on the screen; or filling in and correcting the contents of a form displayed on the screen. For each of the above operations there is a particular mode; thus there are two data modes: an edit mode and a forms mode. A third control mode includes the capability to generate the headings for new forms.

1.6.2 SECOND PAGE OPTION

This option includes a set of firmware routines which support a second 2KB of displayable memory, and allows PAGE UP, PAGE DOWN, SCROLL UP, SCROLL DOWN.

1.6.3 EXTENDED TEXT EDIT PROGRAM

The Extended Text Edit program enhances the edit mode capabilities of the Basic Program and can be installed in conjunction with the Basic or TCOM programs. Its purpose is to give added capabilities for the editing of text displayed on the screen. The Extended Text Editor enables the operator to insert or delete words or sentences and have the line(s) of text or entire paragraphs reformatted.

1.6.4 TCOM PROGRAMS

The TCOM programs include several different telecommunications support firmware programs. Generally, these programs extend the Basic Program in that they include the Basic Program subroutine set and add the capability for communications between the 9003 system and a host computer via the RS-232C interface circuit.

The TCOM IV program allows either single character or block transmission and reception. There are five basic operating modes of the terminal while it is under the control of the TCOM IV program: edit, form, control, TTY and transmit. A sixth mode, receive, is added when the batch option or the NCSS batch receive option is added to TCOM IV. TCOM IV also allows hard copy printing of display data and data received over the RS-232C line.

1.6.5 ZIM (ZENTEC Interrogation Module) PROGRAM

The ZIM firmware program provides a means for visual access to the contents of ROM, PROM, and RAM memories in the system. The contents of each location in the memory is displayed on the screen in hexadecimal coded form and various sections of the memory can be moved on or off the screen with the cursor controls. The contents of any memory location in the RAM segment can be altered from the keyboard when operating under the control of the ZIM program. ZIM is useful for programming, program debugging, and maintenance purposes.

Installation of the ZIM program requires that the page two video display option (paragraph 1-8) is present in the system.

1.6.6 DISK CATALOGER

Disk cataloger is a set of software routines which provide support for the dual flexible disk subsystem attached to a 9003 system. The capability is provided to allow the operator to store, retrieve and modify data files on disk.

1.6.7 DEBUG

Allows the users access to the program counter and registers to aide in the debugging of user written programs.

1.6.8 ZAM (ZENTEC ASSEMBLER METHOD)

ZAM is a set of software routines which allow symbolic programs to be written, tested, assembled and executed on a 9003 microcomputer terminal. ZAM requires the dual flexible disk subsystem and at least 6KB of added RAM.

1.7 OPTIONS

Because the 9003 system functions are programmable, the additon of any given optional function may require either a change in software (programs), addition of hardware (circuits), or both. Paragraphs 1-8 through 1-17 describe those options that require hardware changes. Note that even those options limited to software do require the change of ROM or PROMs and may or may not require the expansion of memory capacity (by installation of additional RAM).

1.8 PAGE TWO VIDEO DISPLAY OPTION

This option provides 2048 bytes of additional memory and supporting software for one full page (24 lines) of video display information. When the option is installed the operator can choose to display on the CRT display screen either of two full pages of video. With the paging and scrolling controls on the keyboard the operator can also choose to either scroll line by line through the two pages (always displaying 24 lines), or switch from one page to the

other. Scrolling is defined as moving the display material up the screen two lines at a time (with the scrolling controls); paging is defined as switching from one page to another (with the paging controls on the keyboard).

To implement this option. RAM and supporting circuits must be added on the character refresh board and program modifications must be made on the microprocessor board.

1.9 GENERAL PURPOSE 2K MEMORY OPTION

This option adds an identical amount of 2048 bytes of memory to the system, as the page two video display option does, except it does not include any video display supporting software. This option can be installed in lieu of the page two option (but not concurrently with it) and the 2048 bytes of memory can be used as general purpose memory for the microprocessor.

1.10 8K RAM BOARD

This option provides space for up to 8192 bytes of RAM memory, in addition to the ROM, PROM, and RAM memory provided in the standard system. It is located on one circuit board. which is installed in the display console card cage. The added memory space is under direct microprocessor control and can be used for additional program, video display, RS-232C interface, or keyboard data storage.

1.11 PRINTER SUBSYSTEM

The printer subsystem option enables the 9003 system to communicate with and print out data on a peripheral hard copy printer. The subsystem consists of a free-standing impact printer, a cable interconnecting the printer to the 9003 system display console, and a printer interface board inside the display console. The printer operates at up to 45 characters per second and can recieve data from the system, or operate off line. The printer is connected to the system bus via the printer interface board, similar to the manner shown in Figure 1-3.

1.12 DUAL RS-232 BOARD

This option provides two RS-232C asynchronous telecommunications interface circuits, in addition to the one provided in the standard 9003 system. The two added interfaces are located on a single circuit board that is installed in the display console card cage. The page two video option or the general purpose 2K memory option must be installed in the system to support this option.

If the dual RS-232C option is installed, there are three interfaces available for connecting to telecommunications lines or external equipment. The dual RS-232C circuits operate in such a manner that either can be receiving or transmitting data at any one time, but not both simultaneously. Switching between the two circuits must be done under software control. No supporting software is normally provided with this option.

1.13 DUAL DISK DRIVE SUBSYSTEM

This option is a disk memory peripheral device complete with interfacing hardware and supporting system software. The subsystem consists of a freestanding disk memory, a cable that connects the disk memory to the CRT display console and a disk memory interface board inside the display console.

The disk memory consists of two separate disk drives and a controller, all housed in a common enclosure. The disk memory uses removable flexible disks, and records in IBM compatible format. It connects to the system bus through the interface board and communicates both directly with the microprocessor and the system memory.

1.14 BAUD RATE OPTION

This option modifies the RS-232C telecommunication interface circuits so that the system can communicate data to and from the telecommunications line at 4800 or 9600 baud. The option involves a strapping change on the timing board and affects the operation of the BAUD RATE switch on the rear connector panel of the display console. If no baud rate option is installed in the system, placing the BAUD RATE switch in the SEL position enables the system to receive and transmit data at 2400 baud. If the option is installed, the corresponding rate is 4800 or 9600 baud.

1.15 16K RAM BOARD

This option allows for 16K bytes of RAM memory in addition to the 2K RAM provided in the basic 9003 Terminal.

1.16 MERCURY MOVE OPTION

The Mercury Move is an option board for the ZENTEC 9003 which will allow data to be moved from one part of memory to another without intervention from the CPU. The block to be moved can be any length specified by software up to 64K bytes. The transfer rate for a 2K byte block is less than 20 ms. Mercury Move is a direct memory access interface device.

1.17 SYNCHRONOUS INTERFACE BOARD

This option provides an interface between the ZENTEC 9003 and a synchronous modem for telecommunications. The interface allows operation to 19.2K Baud using the RS-232C interface.

1.18 POWER OPTION 50 Hz

This option changes the operating voltage requirement of the 9003 system to 100 volts, 50 Hz.

1.19 POWER OPTION 220V, 50 Hz

This option changes the operating power requirements of the 9003 system to 220 volts, 50 Hz.

SECTION 2

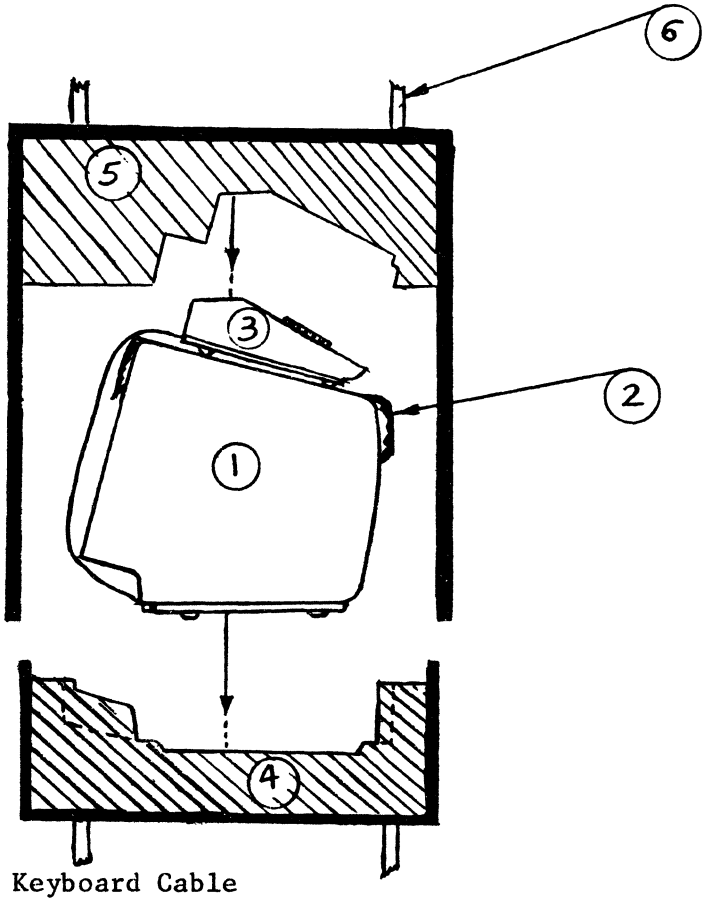
INSTALLATION

2.0 INSTALLATION

The 9003 system components are shipped in a special carton that protects against shipping damage. (See Figure 2-1.) The display console and the keyboard are shipped in the same enclosure with their interconnecting cable installed. Additional items such as option cables, small maintenance tools and instruction documents are packed in the same carton. Large options such as the hardcopy printer are shipped in their own separate containers.

To remove the terminal from its carton. first set the box on a table. Cut the packing straps. Then lift the upper box and remove it carefully, so that the keyboard does not fall. Remove the terminal from the lower box, by holding the terminal in the back and the front (a space is provided for your convenience). Have two people hold the terminal as it is withdrawn from the carton.

When unpacking the equipment, check each item in the packing case against the tabulation on the packing slip. If any breakage or physical damage is apparent, file a claim with the carrier immediately and notify ZENTEC. Use extreme care to prevent damage to the units during unpacking and removal from the shipping carton.



1. Terminal
2. Polyethylene
3. Keyboard with Keyboard Cable
4. Lower Box 27 x 24 x 8
5. Upper Box 27-5/8 x 24-5/8 x 24
6. Strap

FIGURE 2-1

The ZENTEC 9003 may be bench-mounted on a table, a desktop, or any other vibration-free horizontal surface reasonably free from lint and dust. Abnormally bright room light or direct sunlight from a window can interfere with viewing of the display. The display enclosure and keyboard together require a 27" x 16" space envelope. (See Figure 2-2.) The keyboard can be moved away from the CRT display console, within the radius permitted by the two-foot keyboard cable.

This equipment may be installed adjacent to most other types of electrical or electronic equipment without serious interference. Situate the terminal as far as possible from "noisy" electro-mechanical devices like card punches. Avoid locations that are characterized by strong magnetic fields, which can distort and interfere with the operation of the video display.

Environmental temperatures should never exceed 40 degrees Centigrade when the terminal system is in operation. No special cooling provisions are needed. Ensure a free flow of air at the fan exhaust on the rear of the display console. Do not set the terminal system on soft pads or other sound deadening devices which can impede the intake of cooling air at the bottom of the unit.

The display console is equipped with a detachable 6-foot 3-wire industrial power cord and requires 115 VAC/60 Hz power (4 Amperes maximum). Cabling for input/output devices is generally connected to the 9003 via the jacks on the rear panel of the display enclosure (refer to Figures 2-3 and 2-4). Disks and printers are shipped with their own interconnecting cables, which are 10 feet in length.

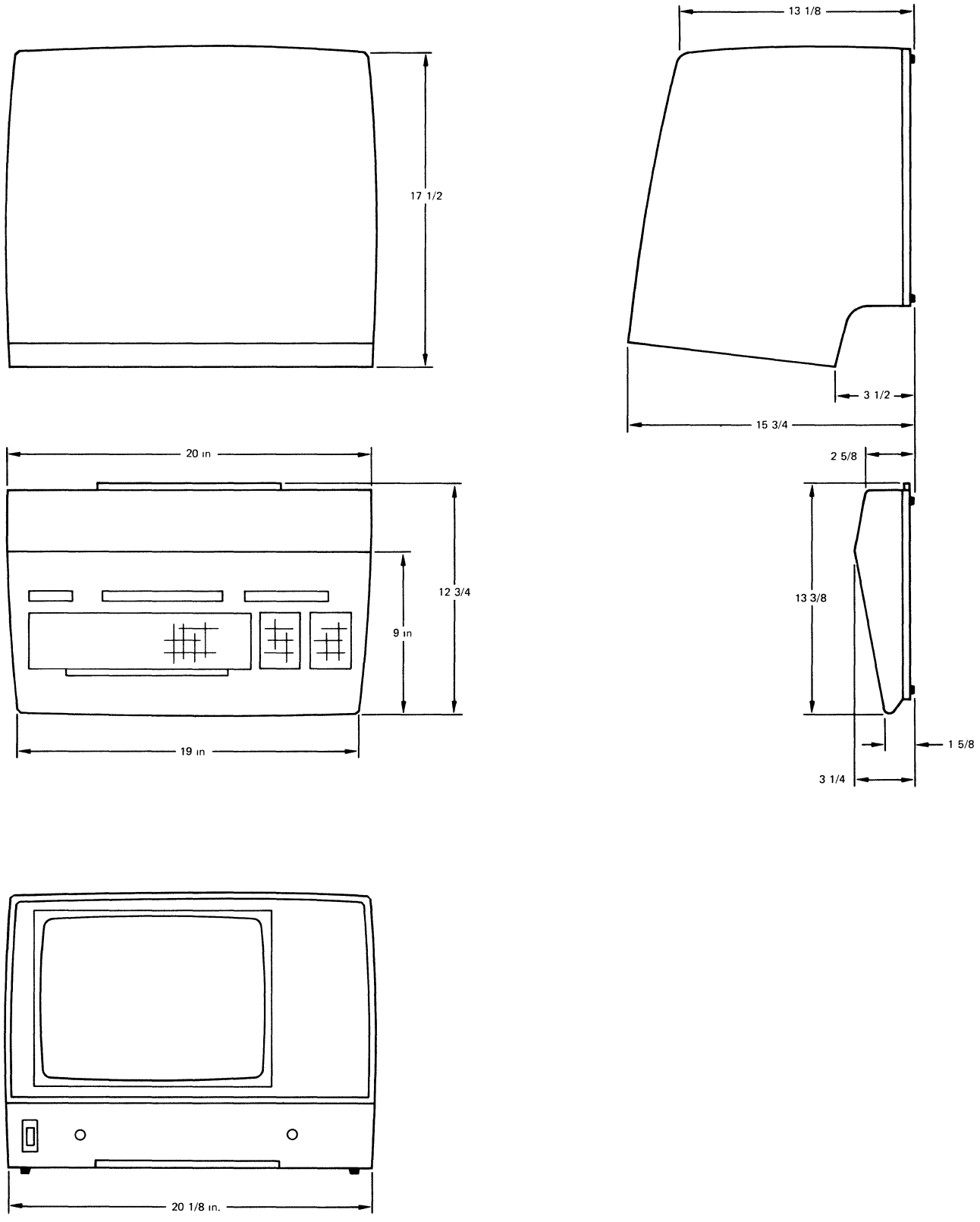


FIGURE 2-2 MOUNTING DIMENSIONS OF DISPLAY CONSOLE AND KEYBOARD

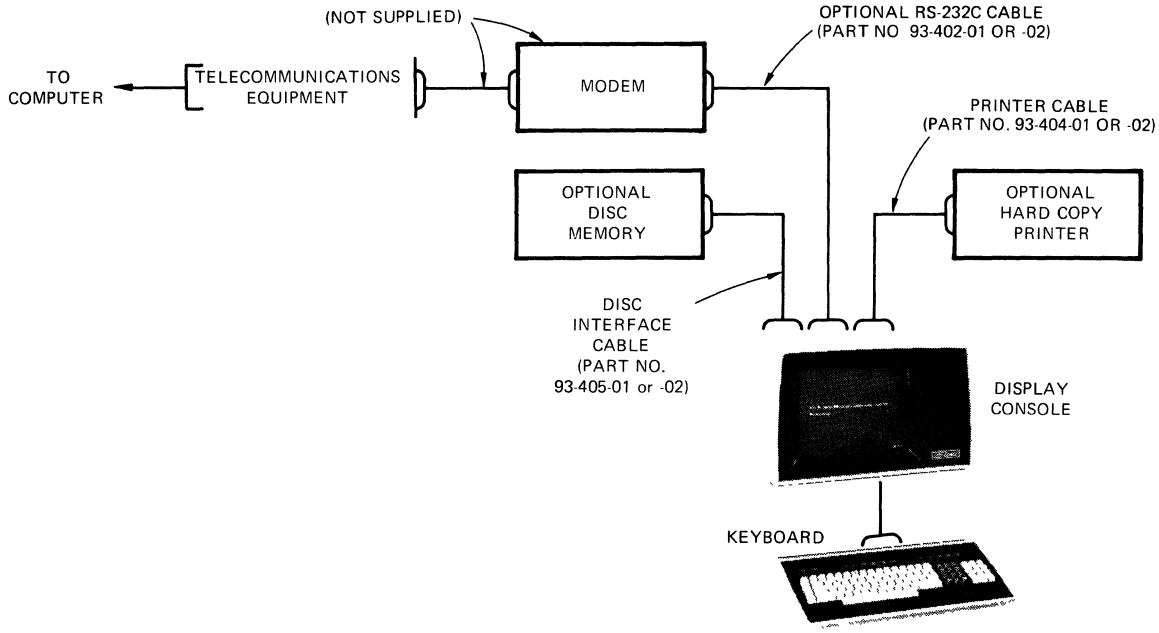


FIGURE 2-3 TYPICAL SYSTEM CABLING DIAGRAM SHOWING TELECOMMUNICATIONS INTERCONNECTION

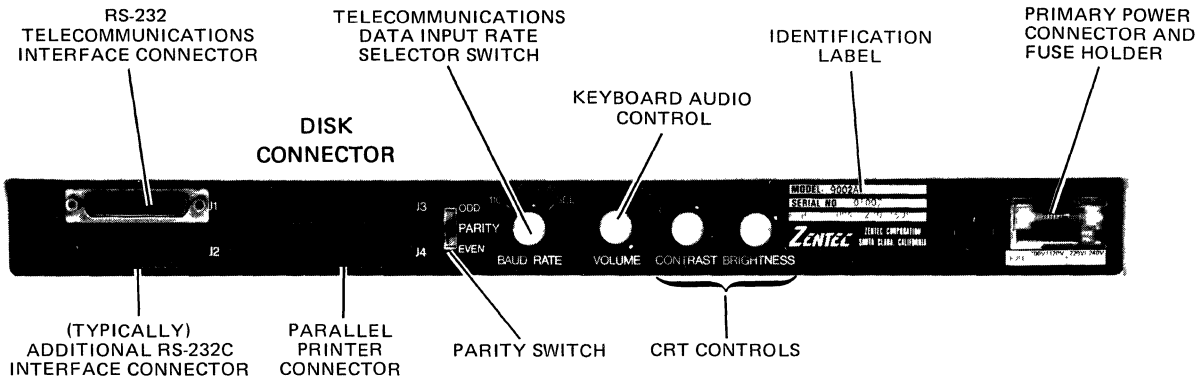


FIGURE 2-4

Data Rates of 110, 300, and 1200 baud may be selected directly, by positioning the rotary selector switch on the rear panel of the display console. The fourth position of the switch (SEL), selects a special internally programmed rate of 2400, 4800, or 9600 baud. Users can re-program this rate at the time of installation. See Section 7.

Parity can be selected by positioning the parity switch in the ODD, EVEN, or NONE position.

2.1 POWER "OFF" CHECKS

1. Insure that the A.C. Cord is attached.

2. Verify the interface connectors are firmly attached to the appropriate connector.

3. Insure the keyboard keys are all free (not stuck down).

2.2 POWER "ON" CHECKS

Turn the power switch on. Be sure that the BRIGHTNESS and CONTRAST controls have been turned up. (See Figure 2-4 for control location) You should hear a loud BEEP. After a warm-up of 15 to 30 seconds, the message REP FORM will appear in the lower right hand corner of the display.

If the message does not appear as expected, try pressing the RESET key on the keyboard. Should the terminal still fail to respond, check the BRIGHTNESS and CONTRAST controls. If the unit fails to display the proper message, consult the troubleshooting chart in Section 7.

When the message Rep Form appears, press the MODE key followed by the SCROLL UP key. The terminal will enter self test. The terminal will continue to test itself until a key is depressed (any key on the keyboard). If an error condition is detected, a message will appear on the 25th line, indicating the RAM location which is in error.

*Self Test will only test the system RAM. It is not a diagnostic but will give a good indication as to whether the terminal is operational.

For information on how to interpret the error message, see Section 6.

SECTION 3

GENERAL MAINTENANCE INFORMATION AND CONCEPTS

3.0 GENERAL MAINTENANCE INFORMATION

The ZENTEC 9003 System utilizes modular construction techniques. This allows the service technician to replace the failing module with a minimum amount of down time.

This section of the maintenance manual includes descriptions of each module, familiarization with major components and preventive maintenance information.

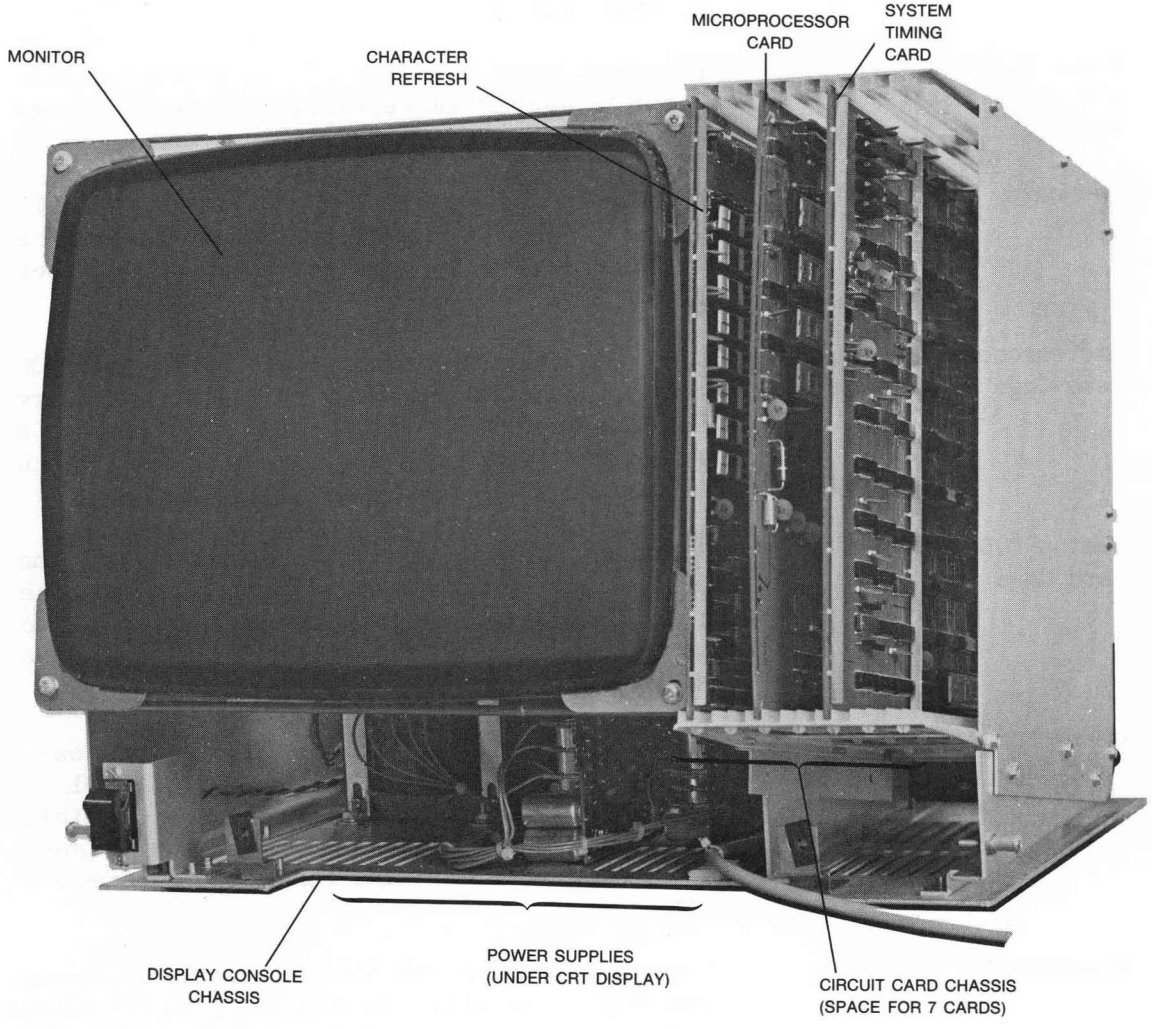


FIGURE 3-1 PCB PLACEMENT

There are seven major modules in the 9003 terminal. Other modules (options) may be added at the factory or by the user. Refer to paragraphs 1.8 through 1.17 for a description of these modules (options).

The seven major modules are listed below:

	MODULE NAME	FUNCTION
1.	Monitor	Contains CRT and drive electronics. Requires TTL inputs. Also has its own high voltage and filament supply.
2.	Power Supplies +5V,+12V,-15VDC +3.5V	Provides power for all of the logic modules. The 3.5V supply is referenced to +5V to form the +8.5V for the RAM memory.
3.	Keyboard	The keyboard provides 8 bit parallel ASCII data to the 9003 through a RAM interface register. It also provides a hardwire reset line.
4.	Microprocessor PCB Card Cage Slot J3	Contains the CPU and all resident ROM and PROM memory. Contains the clock generation circuitry for the 8080 CPU. Optionally available are a static RAM stack (256 x 8) and a timer(which allows the user to interrupt the CPU).
5.	Timing PCB Card Cage Slot J5	Contains the master crystal oscillator and the RS-232 interface. The board divides the chrystal frequency into the correct rate to provide horizontal and vertical drive to the monitor.
6.	Character Refresh PCB Card Cage Slot J1	Contains 2K of RAM for display and keyboard handling. Has provisions for an additional 2K of RAM which can be used as user accessible memory or to support a second page of video. The board also contains the keyboard interface circuitry.
7.	Motherboard	Distributes Data and Address information among the PCB's installed in the card cage. Also distributes D.C. power to all of the PCB's.

The three basic PCB's (Character Refresh, Microprocessor, Timing) are located in the system Card Cage Slots 1, 3, and 5.

Card Cage Slot 1 (J1) is located closest to the CRT and is reserved for the character refresh PCB.

Card Cage Slot 3 (J3) is reserved for the microprocessor PCB.

Card Cage Slot 5 (J5) is reserved for the system timing PCB.

These PCB's SHOULD NOT be relocated. Although no damage will result from misplacing the PCB's, the terminal will be rendered inoperative.

3.1 PRINTED CIRCUIT BOARD PRIORITY

The slots in the card cage are assigned a priority number. The assignment of PCB's to slots is based on this priority scheme and by hard wired harness assemblies.

The CPU has the highest priority on the System. Memory Refresh and Screen Refresh have the next highest prioroity ratings. These priorities are determined by the hardware and can not be changed by the user. DMA peripherals have a priority number that is determined by the card slot the peripheral printed circuit board is placed in.

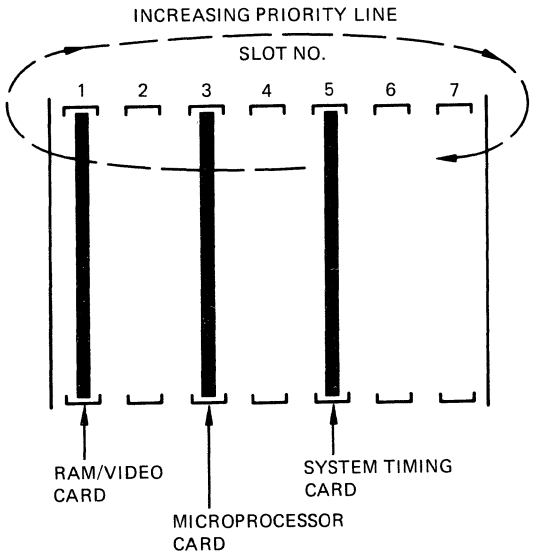


FIGURE 3-2 DIAGRAM OF SYSTEM BUS PRIORITY ASSIGNMENTS

FIGURE 3-3 SYSTEM TIMING PCB

The slots not occupied (2, 4, 6, and 7) must be filled in a given sequence. This sequence is slot 4, 2, 7, and 6.

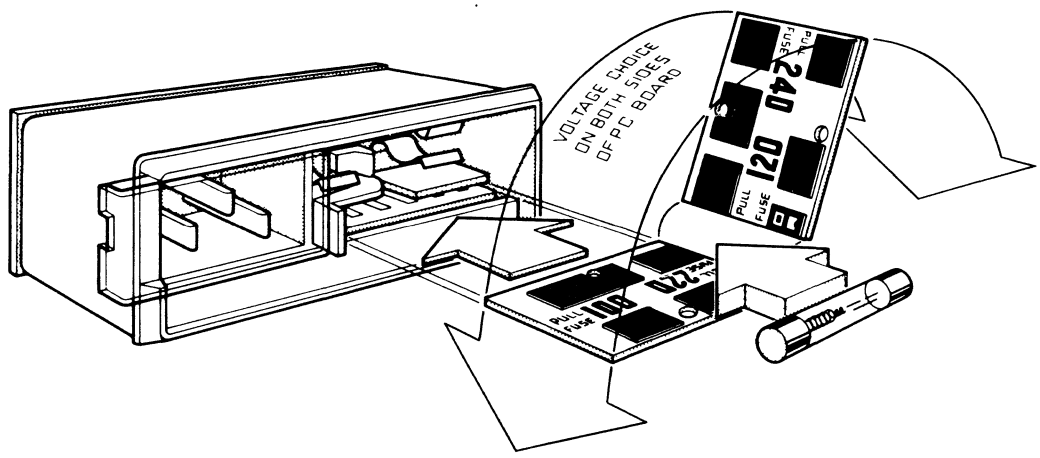
PCB's that do not create their own bus request signals (RAM PCB's) may be placed anywhere there is a vacant slot.

3.2 PRINTED CIRCUIT BOARD LAYOUT AND COMPONENT IDENTIFICATION

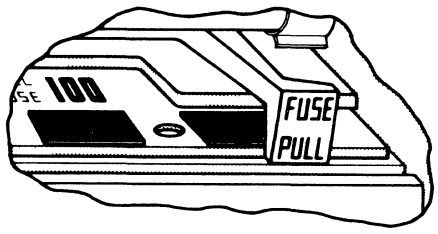
All ZENTEC's printed circuit boards are basically the same. The components are located by using an X-Y coordinate system. (See Figure 3-3.) This system is also used on the schematic diagrams. Each ZENTEC printed circuit board has 2 connectors (See Figure 3-3.) One for the system bus and one for an edge connector which allows connection to a peripheral device. Each ZENTEC printed circuit board carries an etched assembly number. This number can be used when ordering replacement printed circuit boards. A revision level number and letter are also marked on the printed circuit board.

3.3 AC INPUT STRAPPING

The ZENTEC 9003 can operate at four different AC input voltages. To strap the 9003 for operation at these different voltages, refer to Figure 3-4.



Operating voltage is shown in module window.



SELECTION OF OPERATING VOLTAGE

1. **Open cover door and rotate fuse-pull to left.**
2. **Select operating voltage by orienting PC board to position desired voltage on top-left side. Push board firmly into module slot.**
3. **Rotate fuse-pull back into normal position and re-insert fuse in holders, using caution to select correct fuse value.**

FIGURE 3-4

3.4 SWITCH SETTINGS

The ZENTEC 9003 provides the user with a number of switch selectable capabilities. There are switches located on the microprocessor printed circuit board and on the system timing board. There are 32 switches on the microprocessor printed circuit board. These switches are used to select each individual PROM, each row of PROMs, to define the starting address block for each row of PROMS, and to enable the executive ROM and internal stack (if installed).

A complete truth table of all switch settings can be found in Section 7.

3.5 POWER SUPPLIES

The ZENTEC 9003 uses four power supplies: +5V, -15V, +3.5V, and +12V. The power supplies are current limited and overvoltage protected. The supplies are located beneath the monitor assembly. The four supplies have voltage adjustment potentiometers which are accessible with the monitor in place (See Figure 3-6.)

In order to set the current and OVP potentiometers, it is necessary to remove the monitor. For complete adjustment procedures see Section 6.

3.6 PREVENTIVE MAINTENANCE

The ZENTEC 9003 requires very little preventive maintenance. The unit should be kept clean and in a reasonable operating environment.

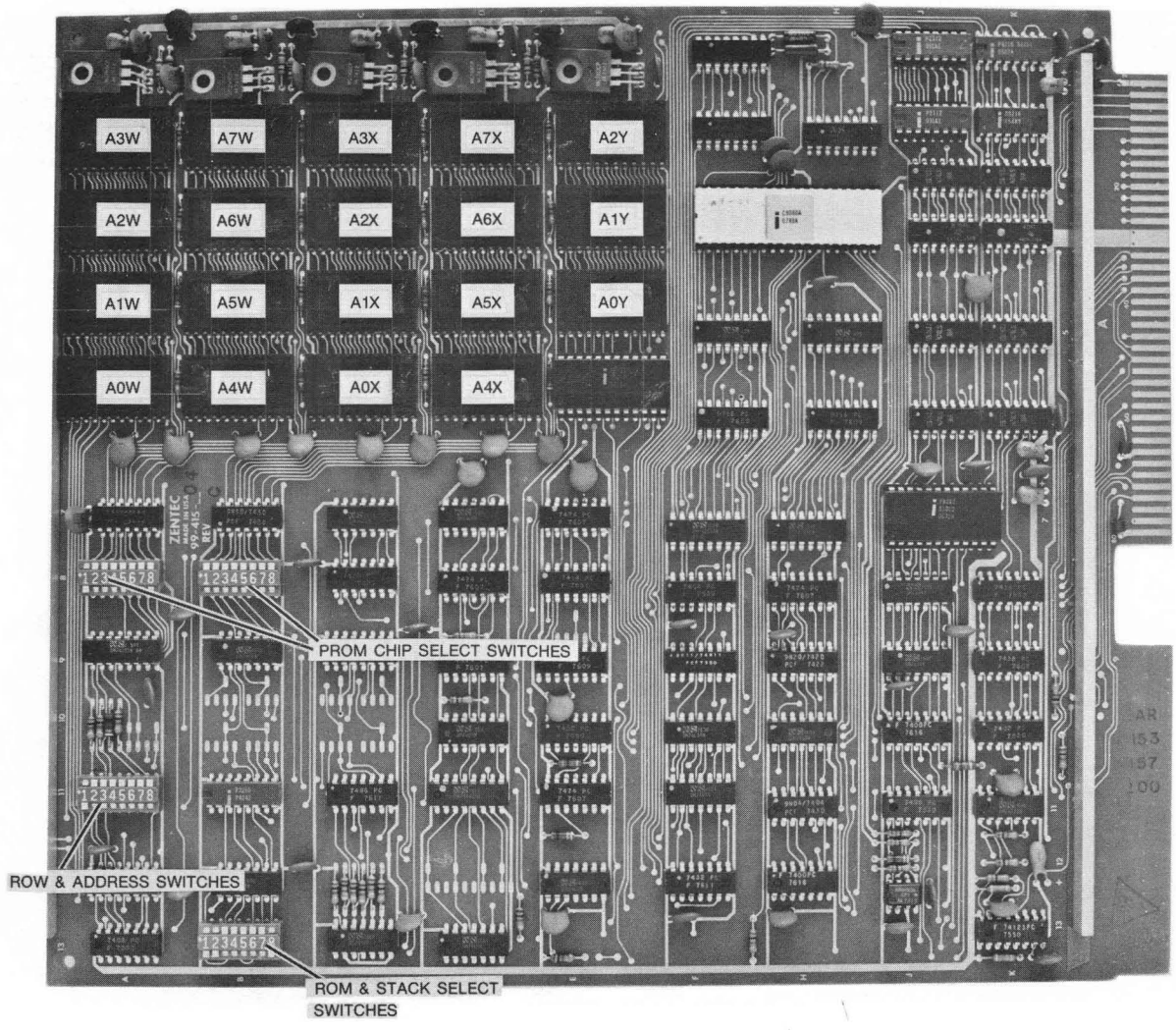


FIGURE 3-4 8080 MICROPROCESSOR PCB

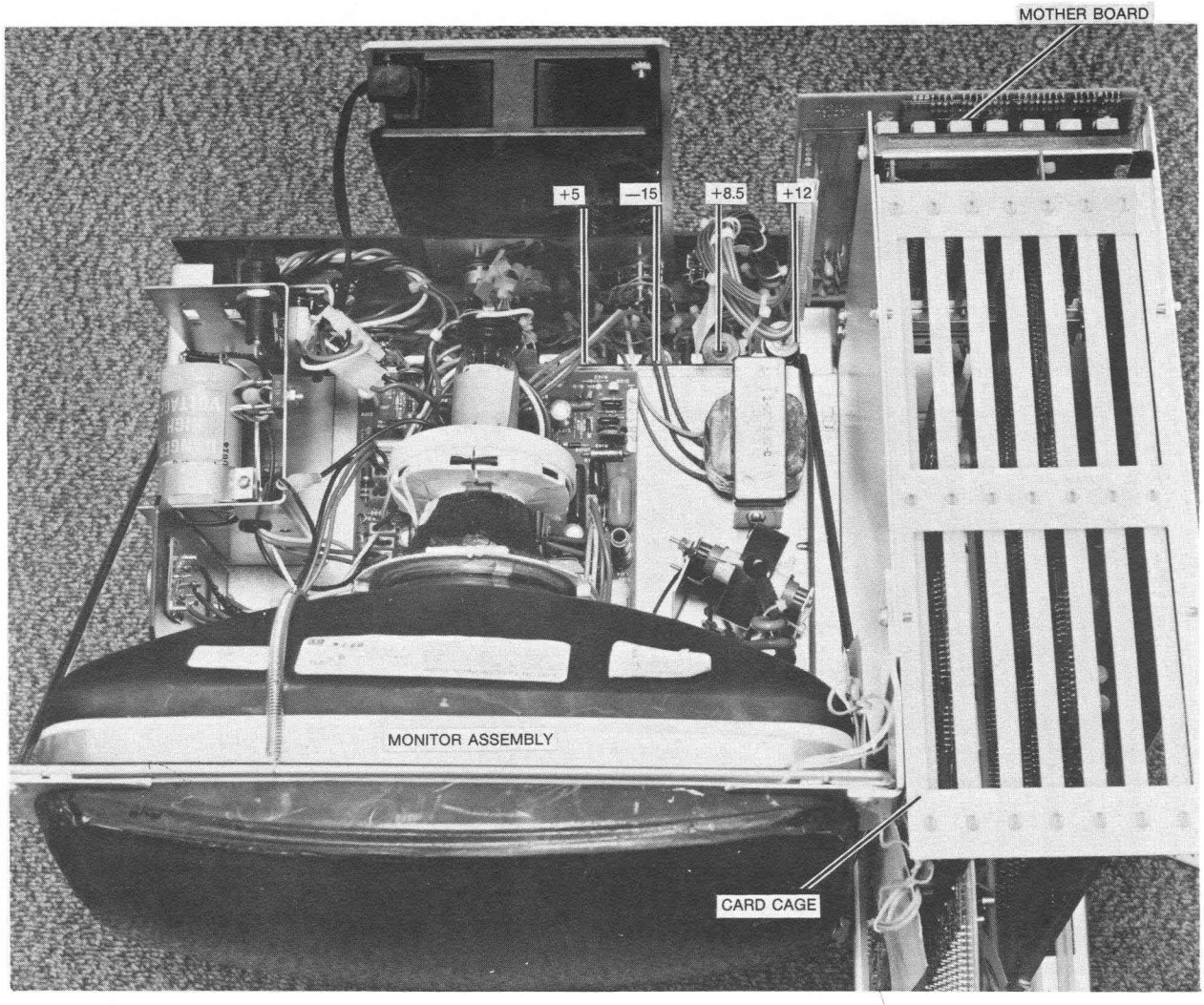


FIGURE 3-6 MONITOR ASSEMBLY SHOWING VOLTAGE ADJUST POWER SUPPLIES

SECTION 4

SYSTEM ARCHITECTURE

4.0 SYSTEM ARCHITECTURE

All input/output devices communicate with the microcomputer via a system bus. The system bus carries 8 parallel bits of data or instructions, up to 16 bits of memory address, internal commands and status signals, and allows any input/output device direct memory access. The bus also distributes power. Data is usually not communicated from an input/output device directly to the CPU, but rather through the RAM. RAM can be read and written into either by the CPU or any input/output device by requesting a memory cycle (memory cycle request.)

When the microcomputer completes a data processing sequence, it writes an ASCII coded alphanumeric character and control information back into the RAM for display. The video circuits read this information out of the RAM, convert the ASCII coded character into a video signal and use the control information to determine the location at which the character is to be displayed on the screen.

The RS-232C interface operates under the control of the TCOM firmware. It communicates data between an external telecommunications line and the CPU via input/output ports. The RS-232C interface can operate either in a single character or block transfer mode.

4.1 SYSTEM OPERATION

To access any memory location a 16-bit address must be used. In the standard 9003 user accessible memory is RAM (although disks or tape drives may be added.) The RAM functions as a physical interface between the hardware and software. The RAM consists of hardware and software registers and a video display section.

Data Input/Output and Processing Sequence

When a key is depressed on the keyboard, it causes the keyboard circuit to output an 8 bit ASCII code. This code is stored in the keyboard input register in RAM. The RAM location is monitored by the microprocessor.

If the entry is a data character, it is displayed on the screen. The ASCII code is loaded by the microprocessor into the video display section of the RAM at the current cursor position. The loading of the displayable character into the RAM is a software function. The subsequent functions associated with displaying it are performed by the system's hardware.

4.2 SYSTEM BUS USAGE

The CPU can obtain a memory cycle at any time. The refreshing of the dynamic RAM circuits and the CRT display both present real-time requirements, and must receive a number of memory cycles but cannot conflict with CPU cycle requirements. Additional memory cycles must be available to service all input/output devices connected to the system bus. To meet these requirements, several hardware considerations have been made. The RAM segment of the system memory is cycled at more than 3 times the effective rate of the CPU. This means that for every cycle the CPU is able to use, there are 2 other cycles available for other devices. Whenever the CPU reads out of the ROM/PROM system memory, (which is physically located on the same circuit board) it reads directly, without using the system bus. During these read operations the system bus can be used by another device to read or write into the RAM.

4.3 SOFTWARE/HARDWARE INTERFACE

The software/hardware section of RAM allows the microprocessor and the input/output hardware to perform their internal operations independently. It allows the microprocessor and hardware to operate at their own clock rates without direct timing synchronization between the two. The only communication between the software and hardware is through RAM. The RAM memory consists of 48 8-bit working registers and 2000 bytes of memory space for video display information.

4.4 WORKING REGISTERS

Working registers are 8-bits wide and are all located in the RAM. There are two types: software registers and hardware registers.

Software registers hold information used actively by the CPU during data processing. Their contents are not accessible by any other circuits. There are 23 software registers, 13 of which have assigned functions, the remaining 10 are unnamed temporary work spaces for the CPU. Software registers derive their name from the fact that they are written into and read out only by the CPU.

Hardware registers are written into and read out by the CPU, but their main usage is in communication with input/output hardware. The CPU stores in a hardware register the results of some data processing routine which is then read and interpreted by a hardware circuit as an instruction. A hardware circuit writes data into a register and the CPU fetches the data and processes it.

Software registers relate only to the microprocessor and its programs; while hardware registers relate to both the software as well as the hardware.

RAM locations and other numerical quantities are expressed in hexadecimal notation rather than decimal. Every hexadecimal number is preceded by the letter X and enclosed in apostrophes. Example: decimal 4096 = X'1000'

4.5 CURSOR ADDRESS REGISTERS

There are two cursor address registers. One register, at location X'1000' identifies the cursor row. The other, at location X'1001' identifies the cursor column. The cursor address registers are always loaded by the microprocessor and are read by the video circuits. The values can range from X'00' to X'19' for the row address register and X'00' to X'4F' for the column address. If the system contains the page 2 video display option, row addresses can extend to X'30'. Row address X'00' corresponds to the 25th line on the screen. Row address X'01' corresponds to row 1 of the first video display page and column address X'00' corresponds to the first column on the left of the screen. From these values on, all addresses are contiguous.

4.6 KEYBOARD INPUT CHARACTER REGISTER

The keyboard input register receives data from the keyboard via the keyboard interface circuit. The keyboard input register is located at address X'1002'. The keyboard register is loaded asynchronously by the keyboard interface circuit and is monitored by the microprocessor. The keyboard is allowed to write any code other than X'FF' into the register. After the microprocessor reads a character code out of the register it writes X'FF' into the register. When the microprocessor monitors the register it interprets X'FF'as the absence of a keyboard character. Any other bit combination is read and processed.

4.7 FUNCTION REGISTER

The function register is used to actuate the audible alert tone. Located at address X'1003', it is always loaded by the microprocessor and is read by the video circuits. A tone, approximately two seconds in duration, is produced whenever the eighth bit in the function register changes state. All other bits in the function register are reserved for program usage and do not affect the tone alarm circuit.

4.8 PAGE REGISTER

The page register stores the address of the video display section of the RAM which appears as the top line on the CRT screen. Located at X'1005', it is always loaded by the microprocessor and is read once every video scan field by the video circuitry. Its contents must be X'01'if there is only one page of video data in the RAM, but it can be any number between X'01' and X'19' if the page 2 option is installed in the system. The page register is also used for scrolling.

4.9 RS-232C COMMUNICATIONS

The RS-232C interface communicates with the CPU on an input/output port basis. Four input ports and two output ports are required.

4.10 DUAL RS-232C INTERFACE REGISTERS

There are six hardware registers in the RAM for the purpose of communicating data control and status information between the microprocessor and the Dual RS-232C interface circuit. These registers are written into and read by the microprocessor and the Dual RS-232C interface circuit.

4.11 VIDEO DISPLAY SECTION

The video display section of RAM stores one byte for every character position on the screen. Whenever a code is entered from the keyboard (or another source), the CPU processes that character and writes it in the video display RAM. It is read out periodically by the video circuitry, transformed into a video signal and displayed on the screen of the CRT display. The CPU writes into the video display section as needed to alter the display image, but the video circuitry continuously reads it out.

In the video display section there is space for a total of 1920 bytes of data representing the 80 characters on each of 24 display lines. An additional 80 bytes are reserved for the 25th line which identifies the current operating mode. One page of video display information occupies 2000 bytes of space in the RAM. The page 2 option requires only 1920 bytes because line 25 is common to both pages.

Any byte stored in the video section of RAM is interpreted by the video circuits either as a data character or as a control code. If a byte is interpreted as a data character, it is displayed on the screen at the cursor location, if it is a control code, it specifies the special display effect which applies to all following data. The control code can specify that all characters following are to be dimmed, or displayed on a reversed background, etc.

Whether a byte is a control code is determined by its three most significant bits. For a control code to be selected, Bit 7 must be active as well as either Bit 6 or 5. Otherwise the information is considered as data character. A control code specifies special display effects for all data characters from that location on until the end of the screen, or until another control character is encountered.

SECTION 5

THEORY OF OPERATION

5.1 SYSTEM TIMING

Timing generation circuits for the 9003 system are located on the timing board in card slot #5. A block diagram of the system's timing circuits is shown in Figure 5-1.

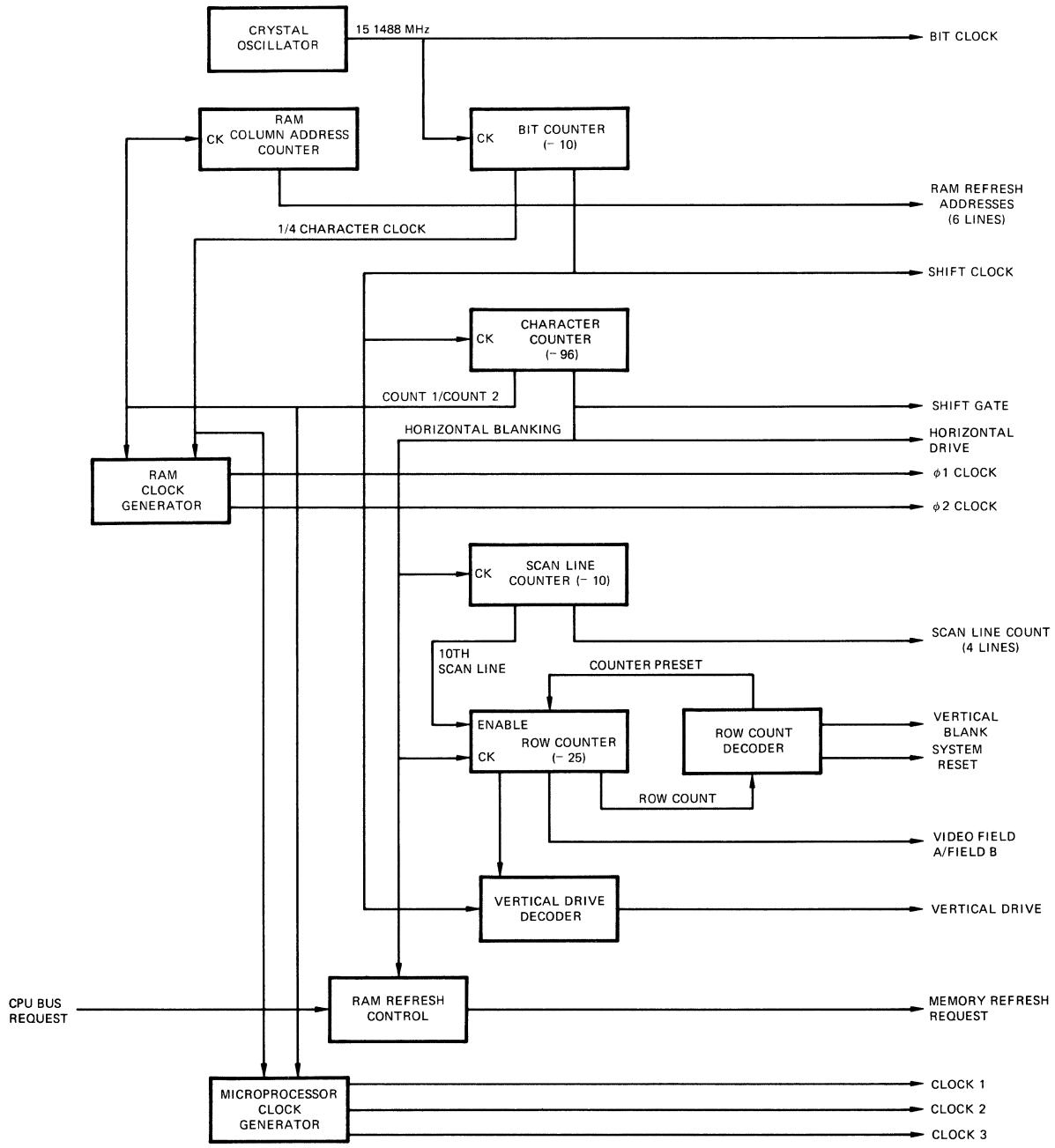


FIGURE 5-1
BLOCK DIAGRAM OF SYSTEM TIMING CIRCUITS

By convention, the standard video display consists of 60 complete images or frames every second. This rate is required in order to eliminate undesirable effects of flicker on the screen. The entire screen must be scanned at least once every 60th of a second. During the interval comprising one vertical frame, the entire area of the monitor screen must be scanned from left to right, beginning at the upper edge of the screen and proceeding downward. The screen is scanned horizontally 263 times during each vertical frame. The horizontal scanning circuitry has to be driven at approximately 15,780 Hz. (263 x 60). A picture includes intervals during which the screen is blank. These intervals include the time during which the beam is returned to the left side of the screen at the end of each horizontal line (horizontal retrace), as well as the interval during which the beam travels from the bottom of the screen back to the top (vertical retrace). To create the picture effect, the scanning beam is turned on and off during the horizontal scan. To maintain adequate resolution, a minimum video bandwidth of approximately 15 MHz is necessary. This guarantees the horizontal detail necessary to ensure a readable display.

A vertical frame consists of 263 individual scan lines. Thirteen lines can conveniently be assigned to vertical blanking. This leaves 250 lines to be divided among the 25 rows of the display. Each line of text on the screen will consist of 10 individual scan lines. To provide the detail necessary, each of the 80 character columns will consist of 10 individual bits. This assures horizontal resolution comparable to that obtained in the vertical dimension. There are 80 columns in the visible portion of each horizontal line. Characters within the line recur at a rate slightly in excess of 1.5 MHz. The 10 individual bits that go to make up each line within the character recur at 10 times that rate, or approximately 15.15 MHz. The divider chain used to derive the various frequencies is depicted in Figure 5-1.

Refer to Figure 5-1. Timing begins with a 15 MHz crystal oscillator. The output of this oscillator, BIT CLOCK, drives a divide-by-10 counter which determines the width of each character on the screen. The output of this counter is known as CHARACTER CLOCK, or as SHIFT CLOCK, depending on where it is used in the system. The SHIFT CLOCK drives a divide-by-96 counter which determines the length of the horizontal line. Part of this line must be devoted to horizontal blanking. Eighty counts of the CHARACTER CLOCK represent the visible line (80 columns). The remaining 16 counts constitute the horizontal blanking interval.

Ten horizontal lines make up each row of characters on the display. The video generator circuitry on the character refresh board requires signals which indicate the row in which a particular line falls, and also which line of that row is currently being scanned. The horizontal blanking signal from the character counter is divided by 10 in the scan line counter. The BCD output of the counter is used to drive the character generation circuitry on the RAM board. The overflow from the scan line counter drives the row counter (a divide by 25 arrangement which provides a continuous indication of the current display row.) Twenty-five rows constitute one visible frame. The overflow from the row counter can be used directly to derive vertical drive and blanking signals.

The frequencies needed to drive the display are considerable. It is convenient to use derivatives of these frequencies to provide timing functions for other system circuits. CHARACTER CLOCK drives logic which produces the CLOCK 1, CLOCK 2, and CLOCK 3 outputs shown at the bottom of Figure 5-1. These clocks drive the write and refresh circuitry of the dynamic RAM used both as video buffer and as general purpose working storage in the system. The CLOCK1, CLOCK 2, and CLOCK 3 signals become instrumental in synchronizing operations throughout the system. They control the timing of CPU bus requests, memory refresh requests, and video refresh requests.

The system timing board also contains a RAM column address counter shown immediately below the crystal oscillator in Figure 5-1. The column address counter controls the refresh cycling of the dynamic RAMs. Refresh is performed automatically during the first 4 microseconds of each horizontal blanking interval. The RAM refresh control logic relinquishes the current memory cycle anytime a CPU BUS REQUEST is pending. Under any other circumstances, RAM refresh has top priority within the system. Refresh control activates the MEMORY REFRESH REQUEST line, thus inhibiting memory requests originating in all lower priority components. Two memory cycles within each horizontal blanking interval are needed for memory refresh.

5.1.1 MASTER OSCILLATOR

System timing begins with the bit clock oscillator shown in Figure 96-414-03 Sheet 1. The oscillator consists of a 15.1488 MHz crystal and a capacitively coupled two-stage amplifier made up of two 74S04 sections (A1K)*. Resistors R53 and R54 damp the high gain of the two inverters. These cascaded stages act as a linear feedback amplifier to sustain oscillation in the crystal. The 15 MHz output known as the BIT CLOCK is buffered (AIF) and coupled out to the Character Refresh board.

5.1.2 COLUMN AND LINE CONTROL

Bit clock is also used to drive the divide-by-10 counter A2K2 (IC 2K Pin 2)

* Refers to the IC located at 1K on the PCB X-Y coordinate map.

The output of A2K-12 becomes CHARACTER CLOCK. CHARACTER CLOCK drive the input of the character counter A3K-2 and A4K-2 and the horizontal drive flip-flop A4J-3. A buffered form of the CHARACTER CLOCK (A1K-8) is known as the SHIFT CLOCK. SHIFT CLOCK is one of the principal driving inputs to the character refresh board. Load Gate is produced by gating selected phases of the CHARACTER CLOCK as shown (A2J8). The two-stage character counter establishes the horizontal line interval.

5.1.3 VERTICAL CONTROL

The two-stage row counter counts individual rows of the display so that vertical retrace can be triggered at the end of the 25th row. The clock inputs of the two-stage counter are enabled by the SCAN 9 signal (also used to preload the scan line counter). During the 10th scan in each display row, SCAN 9 is active (in order that the horizontal blanking signal at the end of that row can be registered by the row counter A3H-7 and A4H-10)

The preload input to A4H is 0. The 13th horizontal blanking pulse (the end of the vertical blanking interval) preloads this value into the row counter. The trailing edge at A4H-12 (the V.BLANK signal) marks the start of a new frame. The end of each horizontal row is marked by the SCAN 9 output. This enables the row counter to register the tenth horizontal blanking pulse. At the end of 24 rows, the counter will hold X'18' which is indicated by the SELECTED ROW signal (A2H-12 and 13). The absence of a vertical blanking signal (A2H-10) with the SCAN 9 output produces the BLANK START GATE signal. This with SELECTED ROWS enables the LOAD input of the row counter.

The vertical blanking pulse has not yet occurred so the preset input of the counter is X'4'. The final horizontal blanking pulse in the frame preloads this value into the row counter, initiating the beginning of vertical blanking. During vertical blanking, the row counter counts horizontal lines, not rows. Vertical blanking is applied to A6H-4 to hold the SCAN 9 output true continuously during the entire vertical blanking interval. This allows the row counter to be clocked at the end of every horizontal line. Twelve lines into the vertical blanking interval, A2H-3 will go true. This BLANKING LINE output concurs with the vertical blanking signal to enable the load input of the row counter. Since the vertical blanking signal is now active, the 13th horizontal blanking pulse bar again preloads the value X'00' into the row counter. Figure 5-2 shows timing during the vertical blanking interval.

5.1.4 SCREEN BLINK GATES

Two signals are derived from vertical blanking. The FIELD B output of the row counter (1/2 the frequency of the vertical blanking signal) is divided by 16 (A5J-11) and supplied to the video generator circuits as CURSOR BLINK GATE. CURSOR BLINK GATE is divided by 2 on the timing board to produce the character

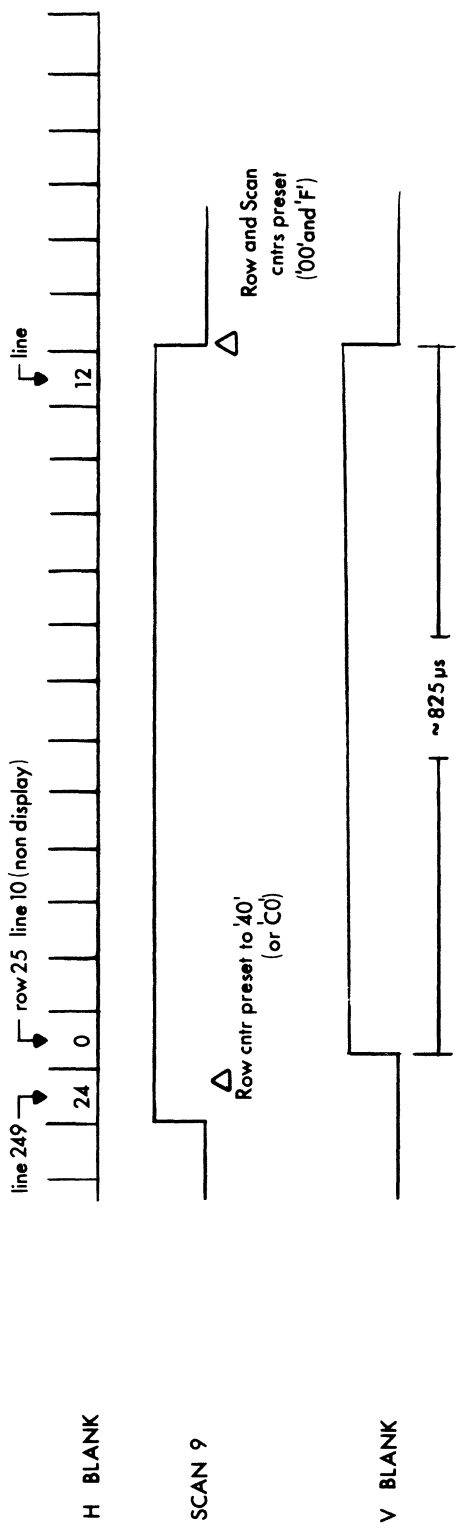


FIGURE 5-2 VERTICAL BLANKING

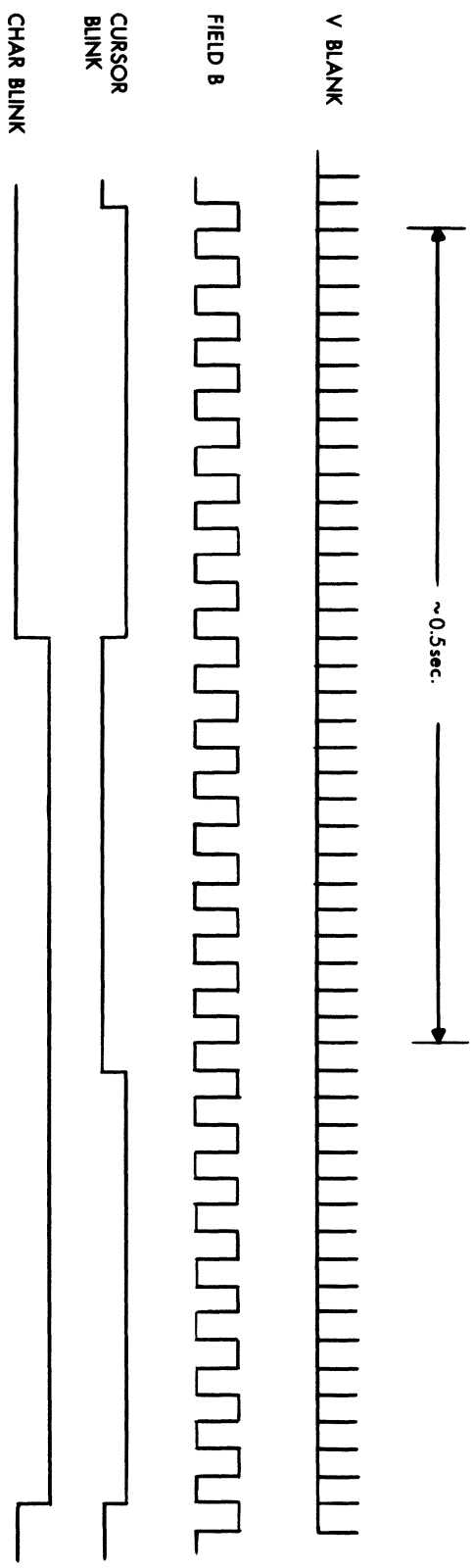


FIGURE 5-3 CURSOR AND FORMS BLINK CONTROL

character blink gate. This signal is used in the video generator circuitry to control the blinking of characters in the forms mode. Timing of these signals is shown in Figure 5-3.

5.1.5 RAM CLOCKS

Refer to Figure 96-414-03 Sheet 2. This shows the logic used to drive the RAM clocks and several timing signals. The VERTICAL DRIVE signal is delayed by one period of the CHARACTER CLOCK. This is to ensure that blanking occurs before retrace. Also shown are the 01 and 02 clock signals. These clocks are no longer used in the 9003. The RAM clocks are developed from CHARACTER CLOCK (A2A). Selected outputs of the BIT CLOCK counter are combined to divide CHARACTER CLOCK into discrete sub-intervals. The succeeding gates and flip-flops develop the four principal RAM clock signals. The relationship among these four signals is shown in Figure 5-4. The positive-going leading edge of the CLOCK 1 signal marks the beginning of each memory cycle in the system. CLOCK 1, CLOCK 3, and CLOCK 3 GATE control precharging and writing within the dynamic RAM, synchronization of the processor. and the video refresh logic which depends on RAM access.

5.1.6 RAM REFRESH CONTROL

The System Timing board contains the refresh control circuitry for the dynamic RAM (though the RAMs are physically situated on another assembly). This circuitry is shown in Figure 96-414-03 Sheet 3. Memory refresh occurs during the horizontal blanking interval and only two RAM rows are refreshed at the end of each horizontal scan. Refreshing at this rate ensures adequate recycling of the RAM. The horizontal blanking signal is combined with the CPU BUS REQUEST signal from the processor (A4F-8). REFRESH GATE (A4F-11) will be true during the horizontal blanking interval as long as a CPU BUS REQUEST is not pending. The trailing edge of CLOCK 3 GATE sets the refresh request flip-flop A4E3. As long as CPU BUS REQUEST remains false, MEMORY REFRESH REQUEST remains true. This inhibits any memory request originating in logic of lower priority. On the character refresh board, MEMORY REFRESH REQUEST gates CLOCK 1, CLOCK 2, and CLOCK 3 signals to the dynamic RAMs. MEMORY REFRESH REQUEST enables the address gates shown in Figure 96-414-03 Sheet 3, A5E and A6E. The contents of the address counter A5F and A6F are gated onto the address bus and directed to the RAM. One entire row in dynamic memory is refreshed during this cycle. MEMORY REFRESH REQUEST enables gate A6H-13. The CLOCK 2 signal which follows the refresh cycle will increment the row counter. MEMORY REFRESH REQUEST is also applied to the input (A4E-8d) of the reset flip-flop. The trailing edge of CLOCK 3 GATE at the end of the second refresh cycle clears the refresh request flip-flop. The process is repeated with each horizontal scan maintaining a constant recirculation of all data stored in dynamic RAM. Memory refresh timing is shown in Figure 5-5.

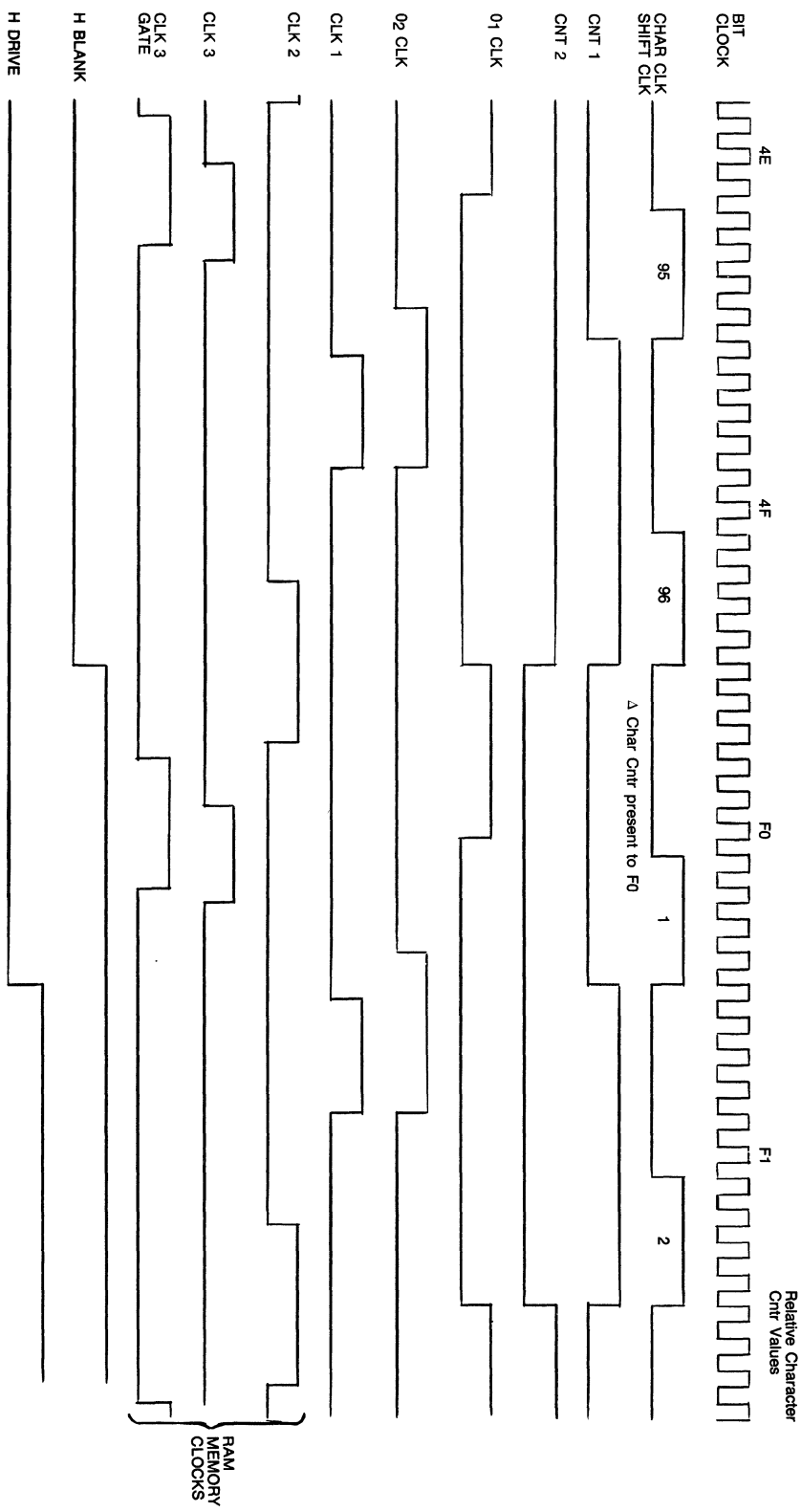


FIGURE 5-4 CLOCK GEN TIMING

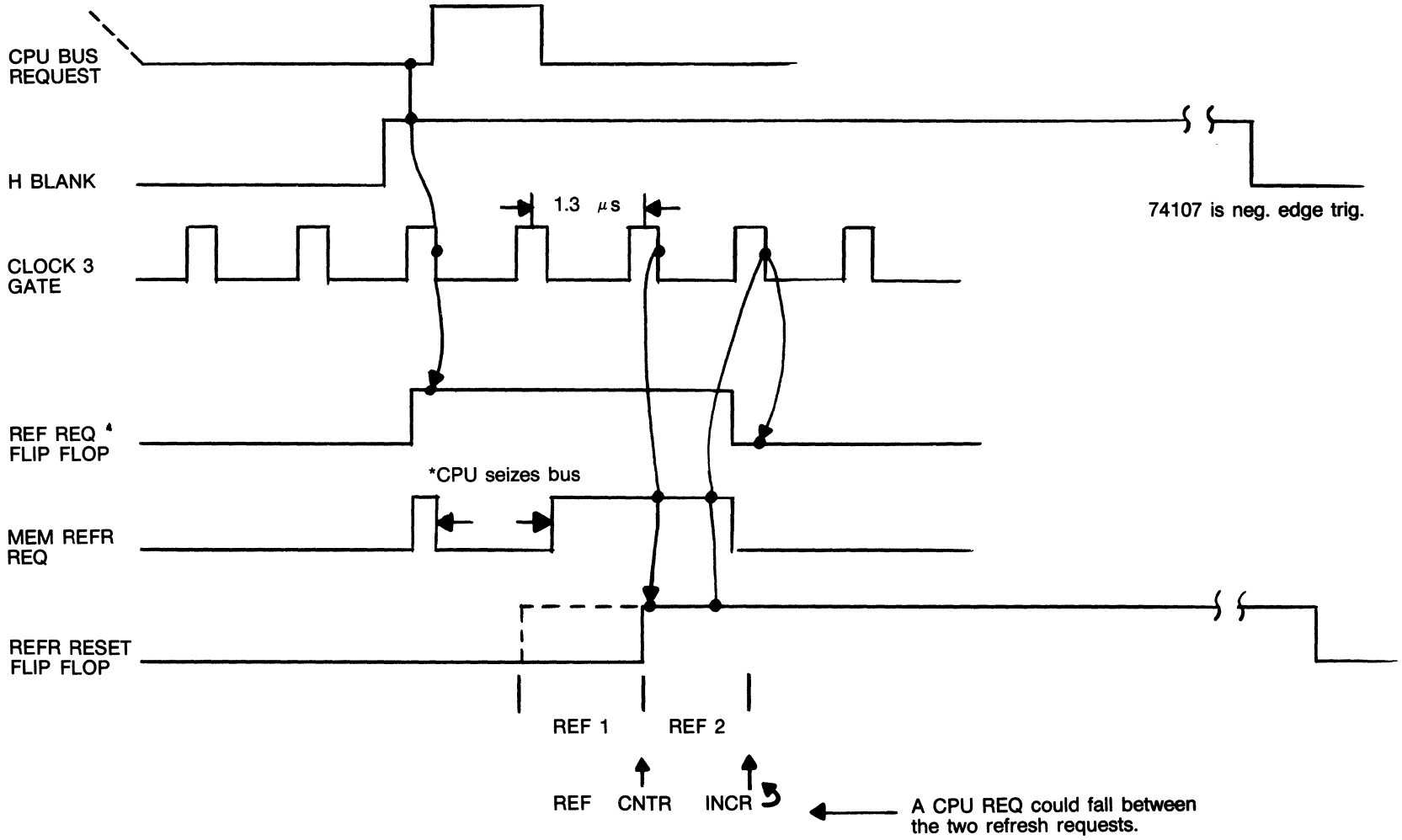


FIGURE 5-5 RAM REFRESH TIMING

5.1.7 ASYNCHRONOUS SERIAL INTERFACE (RS-232C)

In addition to the master oscillator and memory refresh circuitry the timing PCB contains a programmable serial interface circuit (RS-232C). The interface may be used in conjunction with the optional TCOM program or may be programmed by the user.

The heart of the serial communications interface is a universal asynchronous receiver transmitter (UART). This device contains two independent shift registers which share a single driving clock. Incoming serial data is collected by the receiving register and presented in parallel to the bus. The transmitter register accepts parallel data from the bus and converts to serial form for the communications line. The UART monitors the status of both transmit and receive functions, flagging errors such as parity and framing. Parity, start, and stop bits are automatically inserted by the transmitter section during transmission. They are stripped from the received data byte before it is sent to the bus.

Figure 5-6 shows the RS-232C interface in block diagram form. The receiving section of the interface is buffered, using a 64 x 8, first in-first out stack. This allows more effective use of the processor. Included are a built in built in current loop receiver and driver that allow the user to interface directly with units operating on loop currents of either 60 or 20 mils. The processor controls the interface by means of 4 input ports and 2 output ports. (Summarized in Figure 5-7.)

5.1.8 CLOCK GENERATOR

The serial interface derives its clocking signals from horizontal blanking and BIT CLOCK. Clock generation circuits are shown in Figure 96-414-03 Sheet 7. The horizontal blanking signal drives a divide-by-9 counter A5C-2. Output of the counter is a 1750 Hz clock which is divided by 16 within the UART. This produces the 110 baud communications rate. All other rate clocks are derived from BIT CLOCK which drives a cascaded divider chain consisting of devices A6C, A7C, A6D, and A4C. The outputs of the final divider (A4C) provide the basic 300, 1200, 2400, 4800 and 9600 baud clocks to the rate selection circuitry. These rates are selected by means of a switch on the back panel of the terminal. The fourth position of that switch selects a rate which is internally programmed by switches on the timing board. The user can select rates of 2400, 4800, or 9600 baud. These switches are shown at A4 on Figure 96-414-03 Sheet 7. The three standard rates, and the selected rate, are applied to A4D, where the BAUD RATE 1 and BAUD RATE 2 input panel selector switch are decoded and used to select a single clock. This is sent to the UART as the TELCOM CLOCK A7D-6. Both current loop and RS-232 level inputs are available to the serial interface. These are shown in Figure 96-414-03 Sheet 5. External jumpers connect either the current loop input of the RS-232C input to SEL Common. This is applied directly to the UART, A11C, Pin 20.

5.1.9 RECEIVE AND TRANSMIT DATA

Serial or parallel data conversion is performed automatically within the UART. Each time the UART receives a character, it raises DATA RECEIVED (pin 19). The eight bits of data are available at the D0 through D7 outputs of the UART. The character is applied directly to the inputs of the 64 byte FIFO A11F and A11E. If the input section of the FIFO is prepared to receive data, its INPUT READY (IR) outputs will be high. The IR true from each FIFO coupled with the DATA RECEIVED output of the UART places a one on the "J" input of the SHIFT IN flip-flop (A9D). The flip-flop is clocked by a derivative of the CLOCK 3 signal from the timing section. The flip-flop's output is used to clock the contents of the receive buffer into the FIFO. The output at pin 6 of the SHIFT IN flip-flop resets the UART logic (pin 18). This process is repeated with each incoming character until all 64 bytes of FIFO have been filled. The UART monitors each incoming character. An error either in framing (erronious START or STOP bits) or in parity is detected and forwarded to the error logic shown in Figure 96-414-03 Sheet 6 (A10B). An error in any of the 64 stack bytes will cause the appropriate error flag to be set. The framing and parity flags are made available to the multiplexing logic shown in Figure 96-414-03 Sheet 5, (9F and 10F) as status bits to the system bus.

Interface addressing logic is shown in Figure 96-414-03 Sheet 6. Any input addressed to port X'41', X'43', or X'0F' will enable the status multiplexer A7B. The enable MUX signal is applied in parallel to the 4 multiplexer sections shown in Figure 96-414-03 Sheet 5. The final selection of the port is determined by address bits 9 and 10. When the FIFO has at least one byte in it, the OR (Output Ready) of both FIFO sections goes true. These outputson pins 1 and 2 of A10D enable the received data available status bit. The processor (detecting this by reading status port X'41') will readout the FIFO. It does this by executing an input instruction directed to port X'0F'. This produces a shift-out output at pin 9 of flip-flop A8B. This is applied to the shift-out input of the FIFO. Each time the processor reads a byte from the FIFO, the FIFO is shifted automatically so that the next byte is available. By repeating this process, the processor can rapidly empty the 64 byte FIFO. Should the processor fail to remove data from the FIFO long enough for the FIFO to become full (64 characters), and another character is received by the receiver an overrun condition exists. The shift-in flip-flop cannot be toggled, and no clock will be applied to the FIFO input. The data received output from the UART and a not ready from the FIFO acts through A8F, A7K, and A7F to produce an overrun indication setting the overrun latch shown in Figure 96-414-03 Sheet 6. Overrun is also applied to the shift-out flip-flop generating an output which dumps the leading byte out of the FIFO. This causes the IR output of both FIFO sections to go high and enables the next CLOCK 3 pulse to shift the UART's output into the top of the FIFO. This way an overrun of the UART is prevented. The oldest byte in the FIFO is lost. Setting of the overrun flag alerts the processor accordingly.

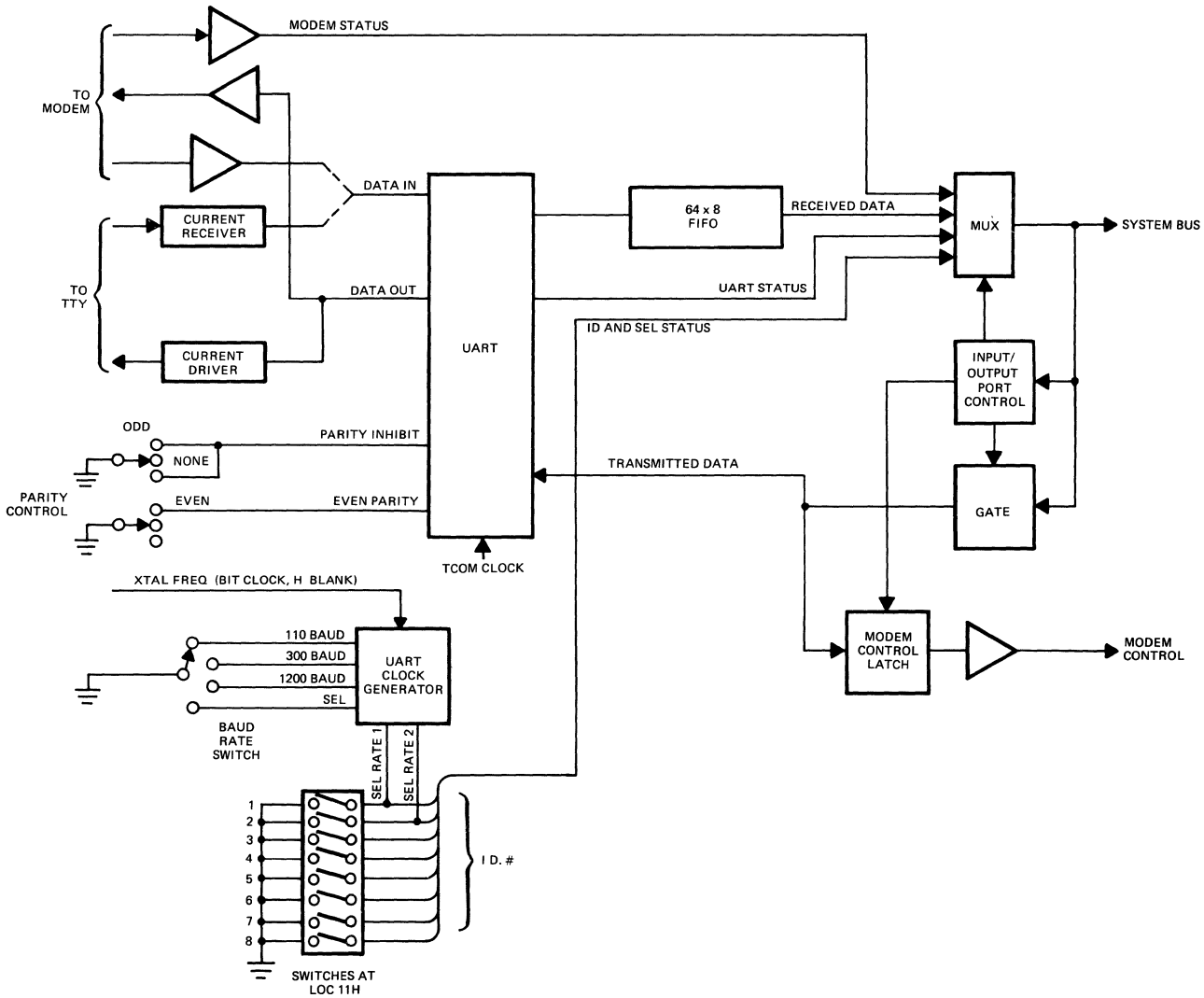


FIGURE 5-6 BLOCK DIAGRAM OF RS-232 INTERFACE

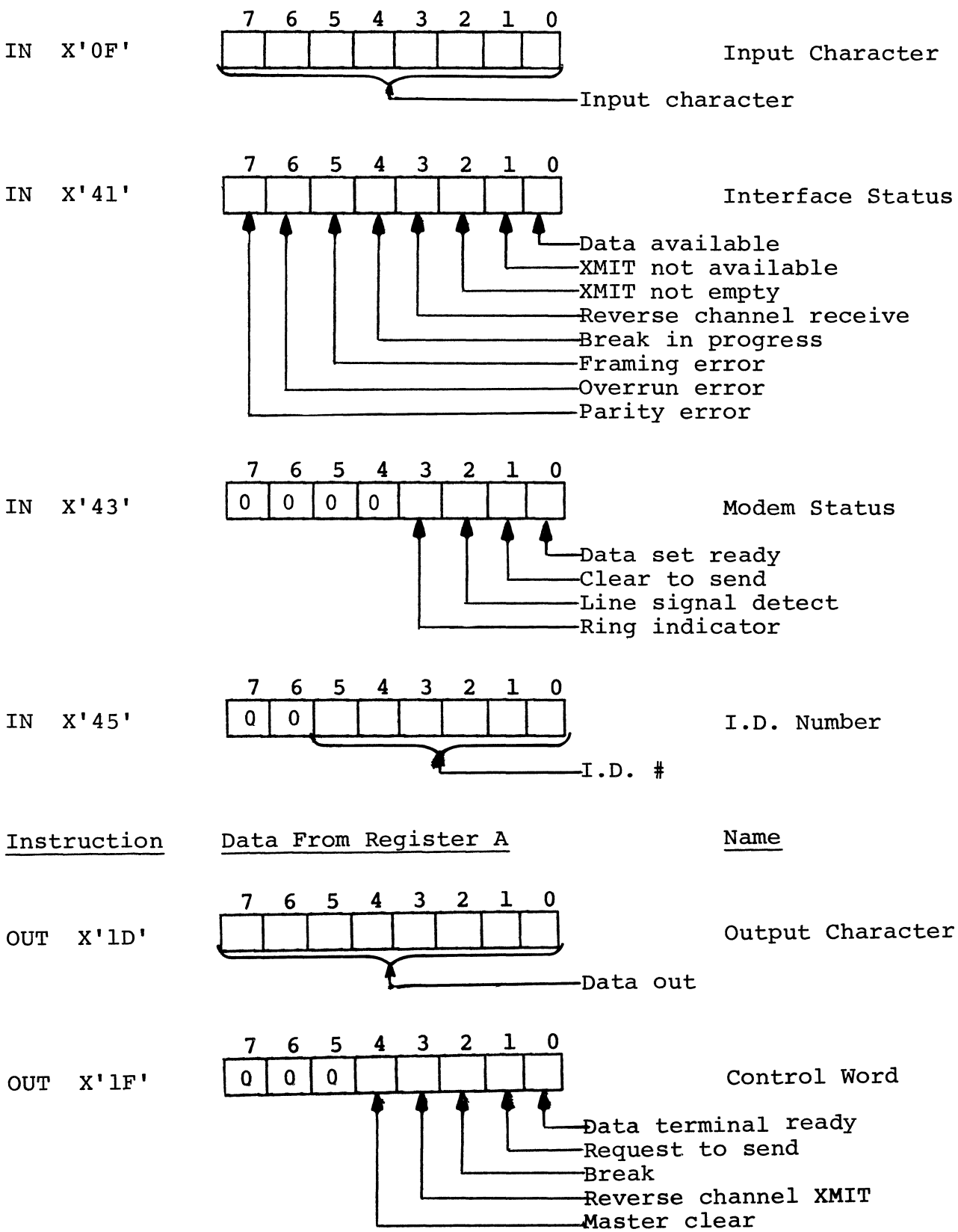


FIGURE 5-7 SERIAL INTERFACE STATUS AND CONTROL

The processor transmits by means of an output port (X'1D'). The TRANSMIT PORT output logic is shown in Figure 96-414-03 Sheet 6. The decoding logic combines with CLOCK 2 to produce a load transmitter output to the UART. Data on the UART's TR1 through TR8 inputs will be loaded and serialized. Refer to Figure 96-414-03 Sheet 5. Observe that these inputs communicate with the system address bus, bits 0 through 7. Serial output of the UART (Pin 25) is applied to the TTY output driver Q2 and to the RS-232 driver A10-A. Both outputs are made available at the interface connector. The shunt resister (R37) may be jumpered across R36 to permit operation in 60 milliamp teletype loops. R50 has a similar function. The serial interface includes the break and master reset functions. Break is initiated by writing out bit 2 of control port X'1F'. See Figure 96-414-03 Sheet 6. Execution of the command will cause the break one-shot A3B to fire. The duration of the break is approximately 250 milliseconds. A program reset may be initiated by the CPU to clear the interface prior to retransmission of data. Reset is triggered by an output instruction which sets bit 4 of the interface control port. Execution of this instruction will cause the reset flip-flop to be set. (Figure 96-414-03 Sheet 5.) Reset clears the UART, the FIFO and the error latches.

5.1.10 AUDIBLE RESPONSE CIRCUITS

The 9003 responds audibly to certain keyboard operations. A clicking sound is generated each time the operator depresses a key on the keyboard. Error conditions generate a beep to alert the operator. To produce these audible responses, an oscillator and amplifier on the Timing board are used to drive a speaker attached to the chassis. See Figure 96-414-03 Sheet 4. The signal which initiates keyboard feedback originates on the character refresh PCB. WRITE KEYBOARD gate and WRITE CHARACTER ENABLE produces a CLICK ENABLE signal. CLICK ENABLE enables a one-shot shown in Figure 96-420-01 Sheet 2. CLOCK 3 with CLICK ENABLE produces the CLICK command which is forwarded to the audio circuitry shown in Figure 96-414-03 Sheet 4. The CLICK is buffered twice and applied directly to the base of the audio driver transistor Q1. The output at Q1's collector drives the speaker through a 500 ohm volume control potentiometer mounted on the back panel of the terminal. BEEPER TRIGGER (the error beep) is derived on the timing board. Figure 96-420-01 Sheet 5 shows the function register. LOAD FUNCTION REGISTER gate (with the CLOCK 3) loads the contents of address X'1003' into the latch. The processor triggers the audible beep by reading and reversing the state of bit 7. Refer to Figure 96-414-03 Sheet 4. The circuit consisting of A8H, A8J, and A3F produces a negative-going trigger to the beeper one-shot A3B in response to any edge positive or negative on the BEEPER TRIGGER input. The output of the one-shot is a positive-going pulse 1/2 second in duration which enables A4B-5. The other input comes from the 555 timer (A4A-3). The output of the timer is a 500 Hz burst which drives the base of Q1, which drives the speaker.

5.2 CHARACTER REFRESH

RAM memory in the 9003 is in 2K blocks, using 2K x 1 dynamic RAMS. Eight of these devices are used to form each 2K x 8 segment as shown in Figure 96-420-01 Sheet 6. The eight RAMs shown at the top of the drawing comprise the working registers and video buffer. The 8 devices shown in row B constitute the RAMs of the page 2 option. All RAMs share an 11-bit address bus which is decoded internally. The bi-directional data input/outputs of corresponding devices are tied together to form the 8-bit output bus.

Since all devices are of the dynamic type, the array requires a 3-phase clock for each read or write cycle. CLOCK 1, CLOCK 2 and CLOCK 3 are generated on the timing board. Refer to the gate shown in Figure 96-420-01 Sheet 3 A8A. Memory clocks pass through this gate to the RAM during memory refresh request cycles or when CARD SELECT is active. CARD SELECT is a composite signal which enables the clock gate whenever the address decoding logic detects a bus address that specifies these RAMs. During character refresh cycles, CARD SELECT is activated by the address multiplexer. Clock gate will be enabled during memory refresh request, character refresh, or whenever the address on the system bus defines the video buffer. The output of A8A is applied to the circuitry shown in Figure 96-420-03 Sheet 7. This circuitry converts the clock signal levels to +5, -15 volts so that the RAMs can utilize them. The clocks are distributed in parallel to all devices in the memory array.

5.2.1 CPU READ

The CPU initiates a RAM whenever the program encounters an address outside the internal addressing range of the processor (the ROM/PROM segment of system memory). When this occurs, logic on the processor board generates a CPU BUS REQUEST. The CPU has the highest priority within the system. The processor places the desired address on the system's bus.

Refer to Figure 96-420-01 Sheet 1. This is the character refresh board's address decoder section. An address within the range of the video buffer, (defined by the upper five bits of the address bit) results in an ADDRESS DECODE 1 or an ADDRESS DECODE 2 output from the address decoder. Both outputs are applied to the address multiplexer A1J/ A1F/ A1H/ A1K. System priority logic inhibits character refresh during a CPU BUS REQUEST. The address multiplexer selects and forwards the 11 low order bits on the address bus to the RAM array shown in Figure 96-420-03 Sheet 6. The two outputs of the address decoder go to the RAM as CHIP SELECT 1 and CHIP SELECT 2. The page 1 or page 2 RAM bank will be enabled accordingly.

The ADDRESS DECODE 1 and ADDRESS DECODE 2 outputs are combined to generate the select data bus signal. This signal becomes CARD SELECT which is used (See Figure 96-420-01 Sheet 3) to enable the RAM clock gate. The eight sense amplifiers in Figure 96-420-01 Sheet 7 are coupled to the output gate shown in

Figure 96-420-01 Sheet 2 A2D and A2E. Refer to Figure 96-420-01 Sheet 1. The SELECT DATA BUS signal combines with the READ DATA output of the processor producing READ DATA GATE A2J-4. This signal enables the bus output gates A2D and A2E shown on Sheet 2 allowing the RAM data to pass back to the processor via the system data bus.

5.2.2 CPU WRITE

During the CPU write cycle, the processor initiates a CPU BUS REQUEST and places an address on the system bus. WRITE DATA will be active instead of READ DATA.

Refer to Figure 96-420-01 Sheet 1. Since CPU BUS REQUEST supersedes all other requests, the CHARACTER REFRESH will be momentarily inhibited. The CHIP SELECT signals are passed through the address multiplexer and are applied directly to the RAM array. The CARD SELECT output of the multiplexer will be active, enabling the RAM clock. The WRITE ENABLE output of the multiplexer will also be true because the WRITE DATA input from the system bus is true. READ DATA will be inactive, disabling the RAM data output gate shown in Figure 96-420-01 Sheet 7 A2D and A2E.

The RAM input multiplexer forwards the contents of the system data bus directly to the RAM inputs. A direct path is established between the CPU's data bus outputs and the data inputs of the RAM array. WRITE ENABLE permits the 3-phase clock signal to enter this data into the addressed RAM location.

5.2.3 REFRESH CYCLE

Refresh cycling is initiated at the beginning of each horizontal interval. The object is to refresh an entire row within the RAM chip. Only the low order 6-bits of the address are significant during refresh. The address multiplexer (shown in Figure 96-420-01 Sheet 2) establishes an address path between the refresh request logic on the timing board and the address inputs of the RAM array. MEMORY REFRESH supersedes CHARACTER REFRESH in the order of system priorities (Refer to Figure 96-420-01 Sheet 3). A CPU BUS REQUEST or a MEMORY REFRESH REQUEST can inhibit the CHARACTER REFRESH output of the A5K-6. CHARACTER REFRESH, which controls the address multiplexer. is false during any RAM refresh cycle. The address placed on the system's bus by the timing board's refresh logic will be forwarded through the multiplexer to the address inputs of the RAM matrix.

Refer to Figure 96-420-01 Sheet 3. Refresh of the dynamic RAM requires enabling the RAM clock gate, so that the internal pre-charge and re-write circuitry of the RAMs can be activated. MEMORY REFRESH REQUEST enables the RAM clock gate for one full memory cycle (A8A). The contents of the bus are immaterial during refresh, since logic within the RAM chips themselves

establishes an internal connection between the output of each column amplifier and the corresponding write input. Data currently in the device is simply restored.

Any access, read or write, refreshes every column within the selected address row. The critical requirement during refreshing is that each of the 64 rows within the RAM array be accessed frequently enough to ensure an adequate refresh rate. Two memory cycles always intervene between successive machine cycles of the processor. so that the two-phase refresh cycle is always completed within 3 memory cycles of horizontal retrace.

5.2.4 SCREEN REFRESH

The video circuits, (shown in the block diagram of Figure 5-8) read binary coded digital information out of the RAM, generate a video signal from this information and output the signal, together with horizontal and vertical blanking pulses to the CRT. The CRT, combines the video and blanking pulse with horizontal and vertical drive signals to drive the cathode ray beam.

There are two types of information read out of RAM. Every ten scan lines the video circuits read 80 characters out of the RAM. Prior to every video scan field they read the location of the cursor, special display effects information. and so forth. The binary coded character data is transformed into a signal that represents the character dot pattern on the CRT. This is combined with the cursor and special display effects information and output as a TTL level video signal.

The video circuits use a series of registers that store data output from the RAM. a character generator that generates the dot pattern for all characters and supporting logic that generates various RAM addressing, timing, and access control signals. (See Figure 5-8.)

During vertical retrace, a SYSTEM RESET signal from the display row counter (on the timing board) is supplied to the timing and control logic. This presets the RAM address counter to read RAM address X'1000'. At the same time, memory cycle request and read command are generated.

From this time on, six RAM registers are read out in sequence. The RAM address counter is advanced by one count every time a readout is completed. A new memory cycle is generated before each new readout.

The first two RAM registers read out contain the cursor row and column address (location X'1000' and X'1001'). This data determines the row and character column at which the cursor is to appear on the screen during the next field. Next, is location X'1002' (if a character input from the keyboard is available.)

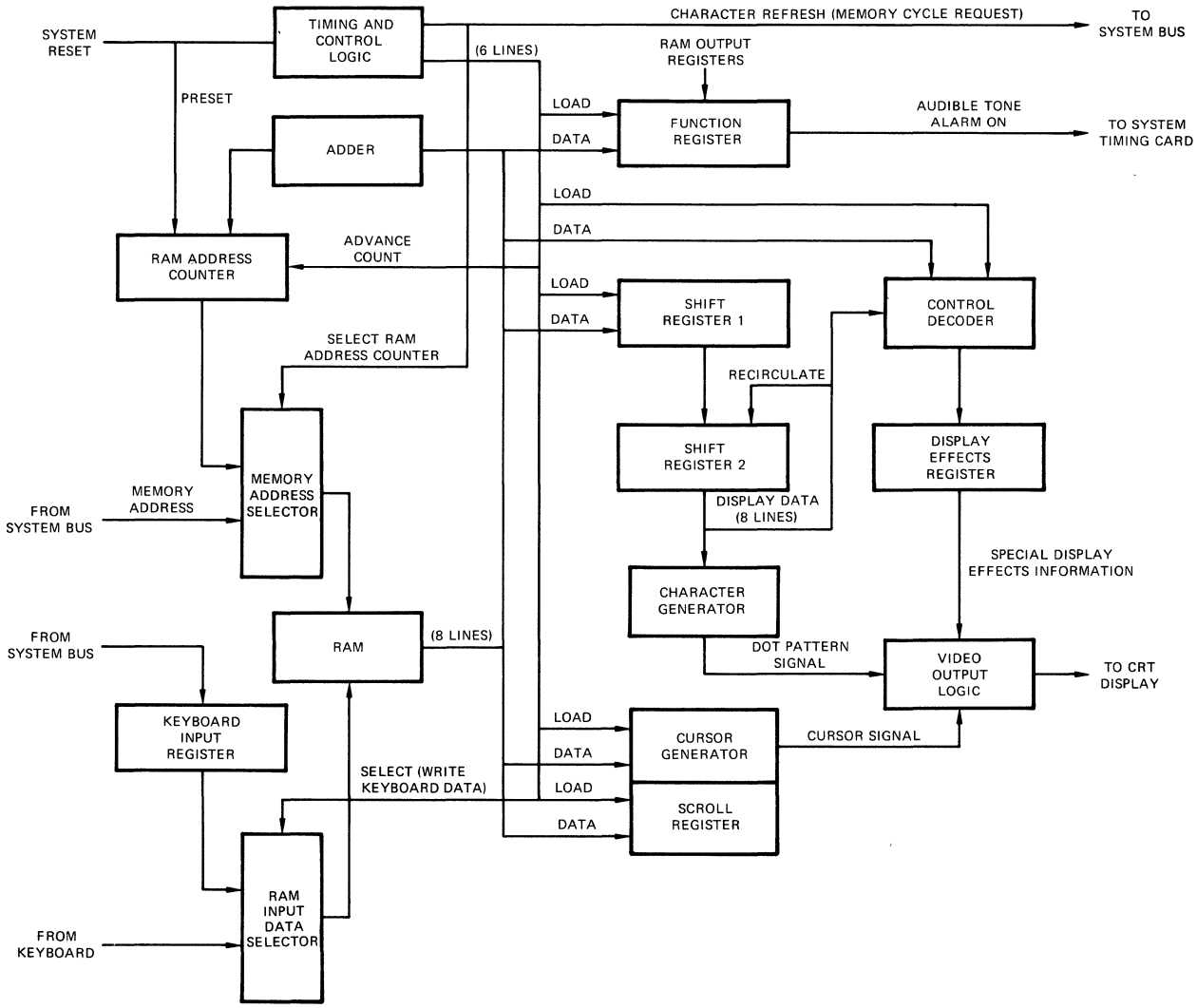


FIGURE 5-8 BLOCK DIAGRAM OF VIDEO CIRCUITS

The RAM register at X'1003' is read. The data is stored in the function register. It contains information that actuates the audible tone alarm. Next, location X'1004' is read. Its contents are decoded by the control decoder and stored in the display effects register. This data determines whether the display is started with any special display effects.

The page start row address is read out of location X'1005', entered into the page register, translated to a binary number, and entered into the RAM address counter. This completes the RAM reading sequence. With the next memory cycle, reading of display data begins.

Reading data out of the RAM is performed during 25 different intervals and during each interval 80 RAM locations are read. For one full video scan field, a total of 25 x 80 = 2000 locations are read. These represent the 80 character spaces on each of 25 display lines on the screen. The first 24 lines are read out of 1920 contiguous RAM locations, starting at the address entered into the RAM address counter. The 25th line, (which identifies the operating mode) is read starting at location X'1030' through location X'107F'.

The reading of the first 80 characters is performed with the first available memory cycle (after reading location X'1005'). The 80 characters are serially loaded into shift register 1 and from there into shift register 2. Each of the 80 characters is consecutively output from shift register 2 into the character generator, where it causes the generation of the first (topmost) scan line dot pattern signal. The characters are also supplied from shift register 2 to the control decoder. Bits 7, 6, and 5 are interpreted to check for a special display effects code.

The character generator does not respond to a display effects code. Instead the display effects register is loaded with the special display effects information.

The 80 characters are recirculated back to the input of the shift register 2. With the start of scan line 2, the sequence of outputs to the character generator, as well as the recirculation of shift register 2 is repeated. The character generator outputs the dot pattern of all 80 characters for scan line 2. This is repeated a total of ten times, causing the character generator to output the dot pattern for all 10 scan lines of each character.

While the dot patterns are generated and shift register 2 is being recirculated, shift register 1 is loaded with the next 80 characters. These characters are read out of the RAM.

During scan line 10 of row 1, the data in shift register 2 is not recirculated again, instead the data from shift register 1 is transfered into shift register 2. This sequence takes place during every video display row on the screen (a total of 25 times).

The output of the character generator is combined with the cursor signal, altered (if necessary to create any special display effects) and mixed with horizontal and vertical blanking information, then output as a TTL video signal.

5.2.5 VIDEO REFRESH INITIALIZATION CYCLE

Initialization of the video refresh circuitry takes place every vertical retrace interval. During initialization the contents of selected software registers are transferred to hardware registers in the video refresh control circuitry, establishing conditions for the next vertical frame. The initialization counter (shown on 96-420-01 Sheet 3), the video refresh address counter (shown on 96-420-01 Sheet 1). and the video refresh data register (shown on 96-420-01 Sheet 2) are described below.

Screen refresh begins with the SYSTEM RESET pulse from the timing board. (See Figure 5-9.) The leading edge of SYSTEM RESET occurs after the start of a vertical blanking interval. Refer to Figure 96-420-01 Sheet 1. SYSTEM RESET is applied to the "clear" input of the address counter A3J, A3H, A3F, preloading the counter value to X'000'. Only the 11 low order bits of the address counter are significant to the 2K RAM chips in the video buffer array. With CHIP SELECT active, the effective RAM address is X'1000'. Refer to Figure 96-420-01 Sheet 3. SYSTEM RESET is applied to the "load" input of the sequencing counter A6H-9. The trailing edge of *CLOCK 3 preloads this counter with X'B'. The output of the initialization counter is applied directly to a BCD to decimal decoder A7H.

Assume that no CPU BUS REQUEST of MEMORY REFRESH REQUEST occurs to interface with the CHARACTER REFRESH cycle. With CPU BUS REQUEST and MEMORY REFRESH both inactive, the enable input to the initialization counter will be continuously true. The trailing edge of each *CLOCK 3 pulse will increment the sequencing counter.

With the sequencing counter preset to X'B', the QA output at A6H, Pin 14 will be true, causing CHARACTER REFRESH to be active. CHARACTER REFRESH true causes the address multiplexer (Figure 96-420-01 Sheet 2 A3J, A3H, A3F) to select the output of the video refresh address counter and address the inputs of the RAM array. The CLOCK 3 input (A1K-13) is gated through the multiplexer and becomes DATA REGISTER CLOCK. The contents of RAM address X'1000' are clocked into the data register. (See Figure 99-420-01 Sheet 2 A3D and A3E.)

The same CLOCK 3 pulse increments the sequencing counter, which bumps the contents from X'B' to X'C'. This activates the CURSOR REGISTER GATE output of the BCD to decimal decoder. (Figure 96-420-01 Sheet 3 A7H, Pin 4) This allows the leading edge of the subsequent CLOCK 3 pulse to transfer the contents of the data register into the cursor row register A4E. The cursor row register now contains the data which was located at X'1000'.

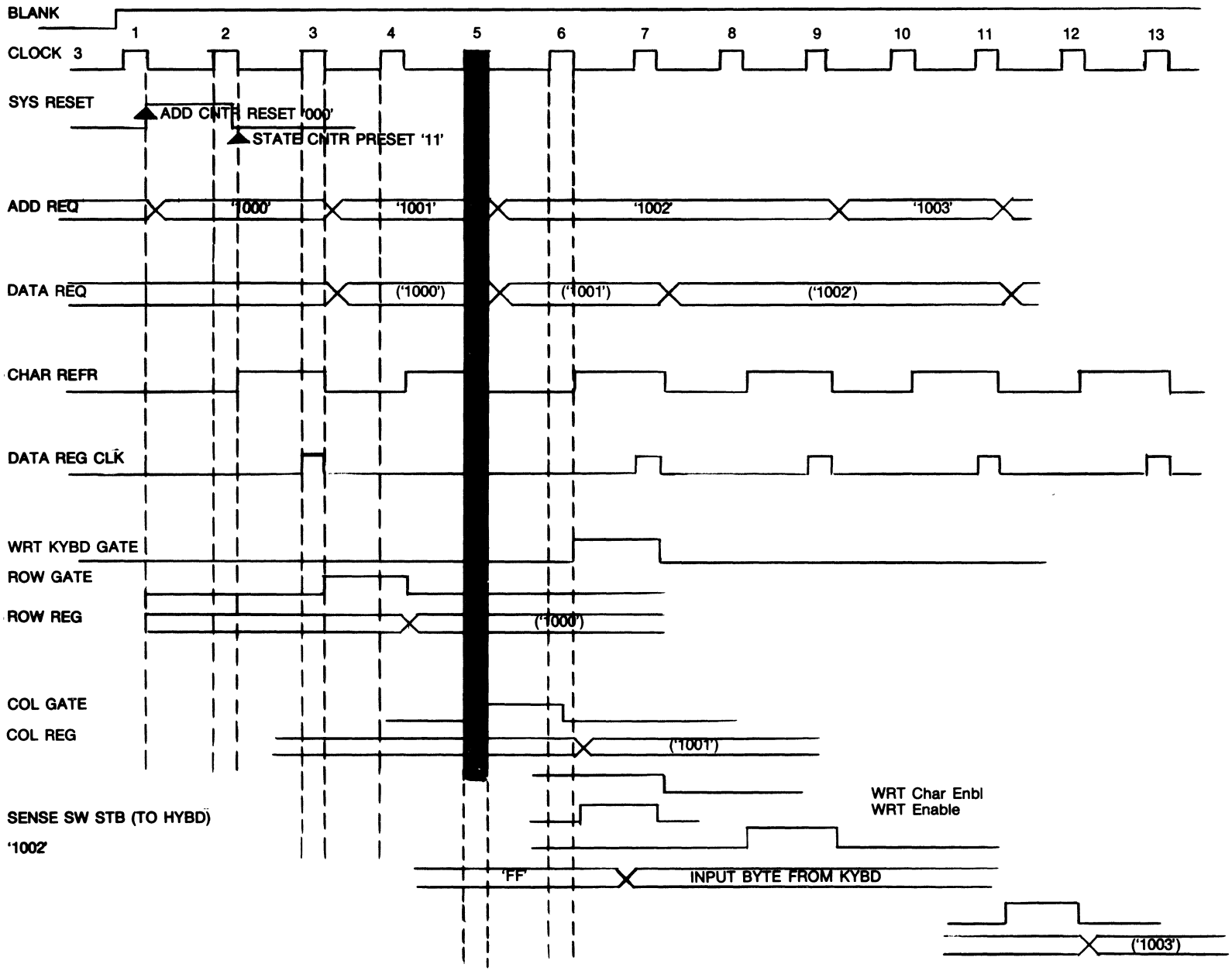


FIGURE 5-9 VIDEO REFRESH INITIALIZATION TIMING

Several things were going on simultaneously. Refer to Figure 96-420-01 Sheet 3. The output at A5J-3 enables the sequencing counter A6H. During CHARACTER REFRESH cycles, this counter is enabled by the CHARACTER REFRESH output at A5J-2. To enable the CHARACTER REFRESH line requires that A6H-14 be high. Character Refresh will be true on alternate cycles of *CLOCK 3. During those cycles in which CHARACTER REFRESH is inactive, the sequencing counter enables itself via A6H-14 and A5J-1. Therefore, the counter wil register each CLOCK 3 pulse, while the logic whose gating depends on an active CHARACTER REFRESH signal will be clocked only on every other impulse.

Refer to Figure 96-420-01 Sheet 1. The address counter is advanced by *CLOCK 3. However, its count input is enabled directly by the CHARACTER REFRESH output of the initialization counter. This counter reacts to every other CLOCK 3 impulse. The video refresh data register (Refer to Figure 96-420-01 Sheet 2) is clocked by a derivative of the CLOCK 3 timing signal. Refer to Figure 96-420-01 Sheet 1. CLOCK 3 passes through the address multiplexer becoming DATA REGOSTER clock. The multiplexer is operated by CHARACTER REFRESH. CLOCK 3 is divided by two before it drives the data register.

Refer to the timing diagram Figure 5-9. The address register is preset to X'1000' on the trailing edge of the first CLOCK 3 pulse. Clocking of the register is dependent on the CHARACTER REFRESH line. The counter will not be clocked again until two full periods of the CLOCK 3 signal have elapsed. When CHARACTER REFRESH goes true, on the trailing edge of the second CLOCK 3 pulse, the address currently stored in the address register (X'1000') will be applied directly to the address inputs of the RAM array. The third CLOCK 3 pulse not only advances the address register (to X'1001') but also clocks the contents of address X'1000' into the data register. The address register contains the address X'1000'. The fourth CLOCK 3 impulse in conjunction with ROW GATE clocks the contents of the data register into the row register.

The output of the sequencing counter (Figure 96-420-01 Sheet 3 A6H) is reversed. The 'QA' output of A6H goes to the 'D' inupt of A7H. The result is the counter maintains a linear counting sequence, but the output of the decoder is not sequential. While the counter proceeds through the states 11, 12, 13, and 14, the input to the decoder jumps from 13 to 3 to 11 to 7.

CHARACTER REFRESH goes true on every other memory cycle; enabling the RAM clock gate via the CARD SELECT output of the address multiplexer. This strobes the contents of the current address into the data register, and advances the address counter. Between CHARACTER REFRESH cycles, the contents of the refresh data register is moved into the appropriate hardware register by the load strobe output of the sequencing decoder.

The fifth CLOCK 3 impulse clocks the contents of address X'1001' into the data register and increments the address counter. At the same time, COLUMN GATE (Figure 96-420-01 Sheet 3) goes true, enabling the sixth CLOCK 3 impulse to transfer the contents of the data register to the cursor column register (A5D and A4D). The cursor column address which the software has stored in location X'1001' is transferred to the column register in the video refresh hardware.

On the third phase of the initialization cycle instead of reading data out of a software register, the logic transfers any pending character from the keyboard into RAM location X'1002'.

Following the trailing edge of the fifth CLOCK 3 pulse, (Figure 5-9) the address register counter will contain X'1002' (the destination of the keyboard input). The initialization counter contains X'E' (A6H). Refer to 96-420-01 Sheet 3. The trailing edge of the 6th CLOCK 3 pulse causes the CARRY output at A6H Pin 15 to go true. WRITE KEYBOARD GATE controls the transfer of information between the keyboard and RAM. (Figure 96-420-01 Sheet 1 A3J, A3H, and A3F) WRITE KEYBOARD GATE is combined with WRITE CHARACTER ENABLE of the keyboard interface circuit. These signals produce the CLICK ENABLE and WRITE ENABLE. CHARACTER REFRESH is true at this time. Both WRITE ENABLE and CARD SELECT are presented to the RAM array and to the RAM clock gate. Refer to Figure 96-420-01 Sheet 2. The RAM input multiplexer selects the input from the keyboard since SELECT DATA BUS is inactive during memory activity. The keyboard input character is written into RAM location X'1002'.

Four full cycles of CLOCK 3 elapse before the address counter is advanced to location X'1003'. The function register (Figure 96-420-01 Sheet 5 A8C) is loaded with the contents of X'1003'. The contents of the condition register are preloaded into the hardware condition register (A9C). The contents of the page register, which determines the first line of the video buffer displayed on the screen are loaded into the video refresh address register (Figure 96-420-01 Sheet 2).

Refer to Figure 96-420-01 Sheet 1. The address register contains a value between X'01' and X'19'. This value identifies the first row of the video buffer which will be displayed on the screen. The video buffer begins at X'1030'. There are 80 columns in each row of the display (X'50'). The first X'50' locations are dedicated to the 25th line of the display. The working buffer begins at address X'1080'.

5.2.6 BUFFER ACCESS AND RECIRCULATION CIRCUITRY

At the end of screen refresh initialization, the initialization counter (Figure 96-420-01 Sheet 3 A7H) contains X'A'. The "load" input of the sequencing counter will be enabled and the next *CLOCK 3 pulse will preload the counter with the value 9. The STATE 9 output of the decoder will be true.

The initialization logic now enters a different mode of operation in which it toggles back and forth between LOAD CHARACTER REGISTER and the STATE 9 phase. Each time LOAD CHARACTER REGISTER goes true, the contents of the memory location currently in the address register will be strobed into the data register. The address register is incremented, so that it always maintains the address of the next character in video buffer. This is used to load the first 80 columns of the video buffer into the low-speed shift register. (Refer to Figure 96-420-01 Sheet 4 A8H, A8F.)

The LOAD CHARACTER REGISTER output from the sequencing section is used to develop a clock for the low-speed shift register. The LOAD CHARACTER REGISTER signal is combined with NEW *CLOCK 3 to drive the low-speed register. The contents of the data register (the character which originated in the video buffer section of RAM) is transferred into the shift register.

Shift register capacity is 80 characters. Each cycle of the sequencing logic produces a new LOAD CHARACTER REGISTER pulse and hence a new character entry into the shift register.

When 79 characters of the first display row have been shifted into the low speed register, A8H-1 will go true. This output, in conjunction with the next LOAD CHARACTER REGISTER signal, will cause the CLOCK 3 impulse (which strobes the final character into the low-speed register) to reset the J-K flip-flop shown in Figure 96-420-01 sheet 4 (A8K). The SHIFT REGISTER FULL output returns to the sequencing logic in Sheet 3 (A7K-9). SHIFT REGISTER FULL inhibits the output of A5K-6, preventing further CHARACTER REFRESH REQUESTS and halting the sequencing logic.

The TRANSFER CHARACTER output from the timing board goes true during the last scan line of each display row. This disables the RECIRCULATE inputs of the high-speed register, forcing it to load the output of the low-speed register. During transfer, both registers must be clocked in synchronism. This is accomplished by the RECIRCULATE CLOCK which is formed by SHIFT GATE and the SHIFT CLOCK from the timing board. The result is fed directly to the "clock" inputs of the high-speed register. The low-speed register is also clocked by the RECIRCULATE CLOCK during the time that the TRANSFER CHARACTERS signal is active. Refer to Figure 96-420-01 Sheet 4. Recirculate Clock passes through A11E-11 and A8J-6 to the "clock" inputs of the low-speed register. At the start of the vertical frame, and at the end of each visible row, the contents of the low-speed register are dumped into the high-speed register for recirculation through the character generator.

At the end of the transfer, the TRANSFER CHARACTERS line goes false. The high-speed shift register lapses into the recirculate mode, and the low-speed register is empty except for the lone "1" in the least significant bit at the bottom of the stack. (This bit is loaded into the shift register by the coincidence of TRANSFER CHARACTERS and the Count 79 output from the system

timing board.) When TRANSFER CHARACTERS goes false, logic on the timing board raises the CLEAR SHIFT REGISTER FULL signal. (Figure 96-420-01 Sheet 4 A8K-1) This enables CLOCK 3 to reset the SHIFT REGISTER FULL output, and enables the CHARACTER REFRESH request logic on Sheet 3. The refresh logic begins loading the next display row into the low-speed shift register. This process is repeated with each row of the display, until 24 lines have been put on the screen. The character refresh logic then refreshes the 25th display row.

5.2.7 25TH LINE

When the 24th line of the screen has been transferred from the low-speed shift register to the high speed recirculator register, the timing board produces the LOAD MEMORY ADDRESS REGISTER output (LOAD MAR). This resets the video refresh address register in preparation for the loading of the 25th line.

Load MAR coincides with the CLEAR SHIFT REGISTER FULL output at the start of the 24th row. Refer to Sheet 1. LOAD MAR enables the "load" input of the address register. X'1030' is loaded directly into the address register by *CLOCK 3. Address X'1030' contains the control row information placed there by the firmware. The loading and recirculation of the 25th row is identical to that of the preceeding twenty-four.

5.2.8 CHARACTER GENERATION

The sequencing logic selects the proper video buffer addresses and loads the contents of these into the low-speed shift register. These characters are transferred into the high-speed shift register during the time that the TRANSFER CHARACTERS line is active. When TRANSFER CHARACTERS is inactive (at the beginning of a new row) the RECIRCULATE inputs of the high-speed shift register are pulled low. Data in the register continues to be re-cycled through the next 10 horizontal lines while this row is being refreshed.

Circulation is maintained by the RECIRCULATE CLOCK (which occurs 80 times during the visible portion of each horizontal scan line). The high-speed register has a capacity of 80 characters. Information stored in the register undergoes 10 revolutions during a row interval. Each character contained in the high-speed register is presented 10 times to the character generator ROM (once for each scan line).

Seven bits of each recirculating character represent an address input to the ROM. More information is needed to completely specify the charaacter generator's output, since the 10-bit sequence varies each scan line. The Scan 1 through Scan 8 outputs of the timing board provide the additional information needed. Each line of each character output from the recirculator register results in a unique output from the character generator ROM. This output is presented in parallel to the inputs of the video shift register A9J. (Sheet 4.)

The LOAD GATE output from the timing board with the trailing edge of BIT CLOCK, load the current output of the character generator into the video shift register. During the next eight periods of BIT CLOCK, the byte is serialized and presented to the video mixer as the RAW VIDEO signal. The serial input to the shift register at A9J Pin 1 is tied to the +5 Volt supply through pull-up resistor R59. As a result, the 9th and 10th impulses of the BIT CLOCK shift zeros onto the RAW VIDEO line. This dark interval corresponds to the standard spacing between adjacent columns of the display.

No character requires more than eight lines for its display. The centering of individual characters on the matrix can vary, so there are actually nine visible scan lines in a row, (even though only eight of them are used). This deals only with certain lower case characters such as "j" and "y" which occupy lower portions of the row not needed by any other characters. The gate network shown on Sheet 4 A8J, A10E, and A9D eliminate the need for a 2K ROM. The video shift register is selectively loaded when the output of the scan line counter is '8' (last visible line of the row) and when the output of the counter is '0' (the first visible line in each display row). Typically display characters are loaded into the shift register during scan '0' through scan '7'. Characters such as "j","p", and "y" which have descenders, will be loaded only during scan line 1 through scan line 8. This means the need for a 2K ROM has been eliminated by selective loading the character generator chip.

5.2.9 CURSOR GENERATOR

The cursor generator circuits are shown on Sheet 3 (lower half of the page). The cursor row register A4E is loaded with a hexadecimal value between X'00' and X'30' corresponding to the screen row in which the cursor appears. The column register (A4D and A5D) is loaded from the software column register at RAM address X'1001' which contains a value between X'00' and X'4F' corresponding to the cursor's column address.

The column register is loaded with the ones complement of the data in the data register. The register is incremented by the same RECIRCULATE CLOCK that drives the high-speed shift register. This clock is gated with TRANSFER CHARACTERS so that the column counter is active only during the last visible scan line of each display row. When the register overflows, it will be preloaded with the complement of X'50'. The counter will overflow repeatedly during the last visible scan line of every display row. The "carry" output of A4D marks the desired column and the desired scan line in each horizontal row. This output is applied directly to the "equals" input of the comparator 6E and 5E.

Inputs to the two-stage comparator come from the cursor row register and the page register. The page register is loaded during initialization, with a binary value that identifies the first visible row displayed on the screen. This register is incremented on the TRANSFER CHARACTERS gate at the end of

When the outputs from the cursor row register, the page register. and the overflow output from the cursor column register occur at the same time, the output of the comparator (A4E-6) will go true resulting in a Cursor output. The duration of which corresponds to the period of load gate. The cursor signal is applied to the video mixer logic shown on Sheet 5.

5.2.10 ATTRIBUTE DECODING AND CONTROL

Special display effects characters (attributes) are distinguished by the binary prefix 100 in the 3 most significant digits. Refer to Sheet 4. The output of the recirculator shift register is monitored by A11E and A11F. If the presence of an attribute character is immediately detected, CONTROL DECODE goes true and is sent to the attribute logic shown on Sheet 5.

In the attribute logic the control decoder's output is combined with the SHIFT CLOCK to enter the low order 5-bits of the recirculator register's output into the control register A9C (C2). These five bits go to the video mixing logic to produce the special display effects. The output from the control decoder activates the blank character generator. This output drives the inverted input of the character generator ROM to suppress any display when an attribute is present.

The condition register shown on Sheet 5 (A9C) is effectively a memory register. It is loaded from the software condition register during video initialization to establish the pre-existing screen condition at the start of every vertical field. The register can be loaded directly from the RECIRCU- LATOR SHIFT REGISTER. The condition register is designed to save the last attribute character in the preceding row of the display. This is necessary in order to re-establish the initial control conditions at the start of a row. ow. The output of the condition register is loaded automatically into the control register at the start of horizontal retrace, by inverted SHIFT GATE and the SHIFT CLOCK signal. Control information is not encoded. Each of the five significant bits in an attribute character controls one of the special effects individually. This permits the creation of special effects in any desired combination.

5.2.11 VIDEO MIXING AND OUTPUT

The mixer logic is shown on Sheet 5 on the lower half of the page. The horizontal and vertical blanking signals are combined to produce a composite blanking signal, and then mixed with the RAW VIDEO signal from the video serialization register to produce the composite video signal. The CURSOR output and outputs from the control character logic are combined with the basic video signal to produce the underscore, reversed polarity, half-intensity, and the blank character effects. The half-intensity effect is obtained by shortening the effective duty cycle of BIT CLOCK, rather than attempting to modulate the level of the video signal.

5.2.12 KEYBOARD AND KEYBOARD INTERFACE

ASCII encoded characters are stored in RAM location X'1002'. The processor scans this location periodically, discriminating between displayable and executive keystrokes.

Display characters undergo limited processing. Control characters never appear on the display. The processor interprets control characters as commands and transfers control to the appropriate subroutines. All codes between X'00' and X'1F' represent functions, X'20' to X'7F' represent displayable alphanumerics.

All control characters are charcterized by the numeric prefix '100' in the three most significant bit positions. The video refresh logic recognizes this prefix and suppresses the display when it occurs. The system discriminates aganst control characters during display, but not during keyboard entry.

Keyboard logic consists of the keyboard interface circuits located on the charcter refresh board, and the keyboard circuits within the keyboard enclosure. The keyboard circuits generate a unique 8-bit character code whenever a key on the keyboard is depressed. This code is accompanied by a synchronizing strobe. Both the strobe and the ASCII code are applied to the interface circuits on the Charcter Refresh board. The interface writes the character into the keyboard input register (X'1002') and generates acoustic feedback for the operator.

Certain keys are defined as repeatable. The keystroke is repeated automatically if the key is held down longer than 1/2 second. The STROBE output initiates each keystroke. but the KEYDOWN output maintains the auto-repeat.

Encoded data from the keyboard enters the interface circuits via the keyboard cable which attaches to connector B on the character refresh board. Refer to Sheet 2. Key depression is signalled by the CHARACTER STROBE line. The trailing edge of the subsequent CLOCK 3 pulse sets the flag flip-flop A6K. The incoming character is not written immediately into the keyboard register at location X'1002'. The actual entry of data always awaits the vertical blanking interval, during which the video refresh circuits get initialized. The Q output of the flag flip-flop concurs with the not-Q output of the reclock flip-flop (A6J) to produce write CHARACTER ENABLE.

Refer to Sheet 3. SYSTEM RESET occurs during the vertical blanking interval and always loads the initialization counter at the start of a frame and at the same time presets the refresh address counter to X'1000'. Two cycles later, the cursor row and column registers will have been loaded from locations X'1000'and X'1002' (the address of the keyboard input register). One more cycle, and WRITE KEYBOARD GATE signal goes true.

The reclock flip-flop is set, inhibiting WRITE CHARACTER ENABLE and activating the ACKNOWLEDGE output. The next two clock pulses clear the flag flip-flop and the reclock flip-flop, resetting both to their pre-input states and completing the keyboard entry cycle. The timing of events during this cycle is shown in Figure 5-10 and on Sheet 1.

WRITE KEYBOARD GATE combines with WRITE CHARACTER ENABLE to produce CLICK ENABLE. CLICK ENABLE will be forwarded to the RAM as WRITE ENABLE. The CARD SELECT output of the multiplexer will be true, so the RAM buffer receives three-phase clocks during this memory cycle. The data bus-multiplexer on Sheet 2 selects the keyboard input (since SELECT DATA BUS is false) and as a result, the ASCII input from the keyboard is written into RAM location X'1002'.

CHARACTER STROBE along with NEW *CLOCK 3 trigger the repeater one-shot when the character arrives from the keyboard. If the key is immediately released, KEY-DOWN will be false upon completion of the write cycle. The output at A5J-6 will be high and every successive CLOCK 3 pulse will retrigger the one-shot. If the key is held down this re-triggering will be prevented and the one-shot will time out after approximately 1/2 second. If Bit 10 is simultaneously true,(indicating a repeatable character) the output of A7K-11 will go high. CLOCK 3 will be repeated with every vertical frame and the key strokes are repeated automatically at a rate of approximately 60 Hz.

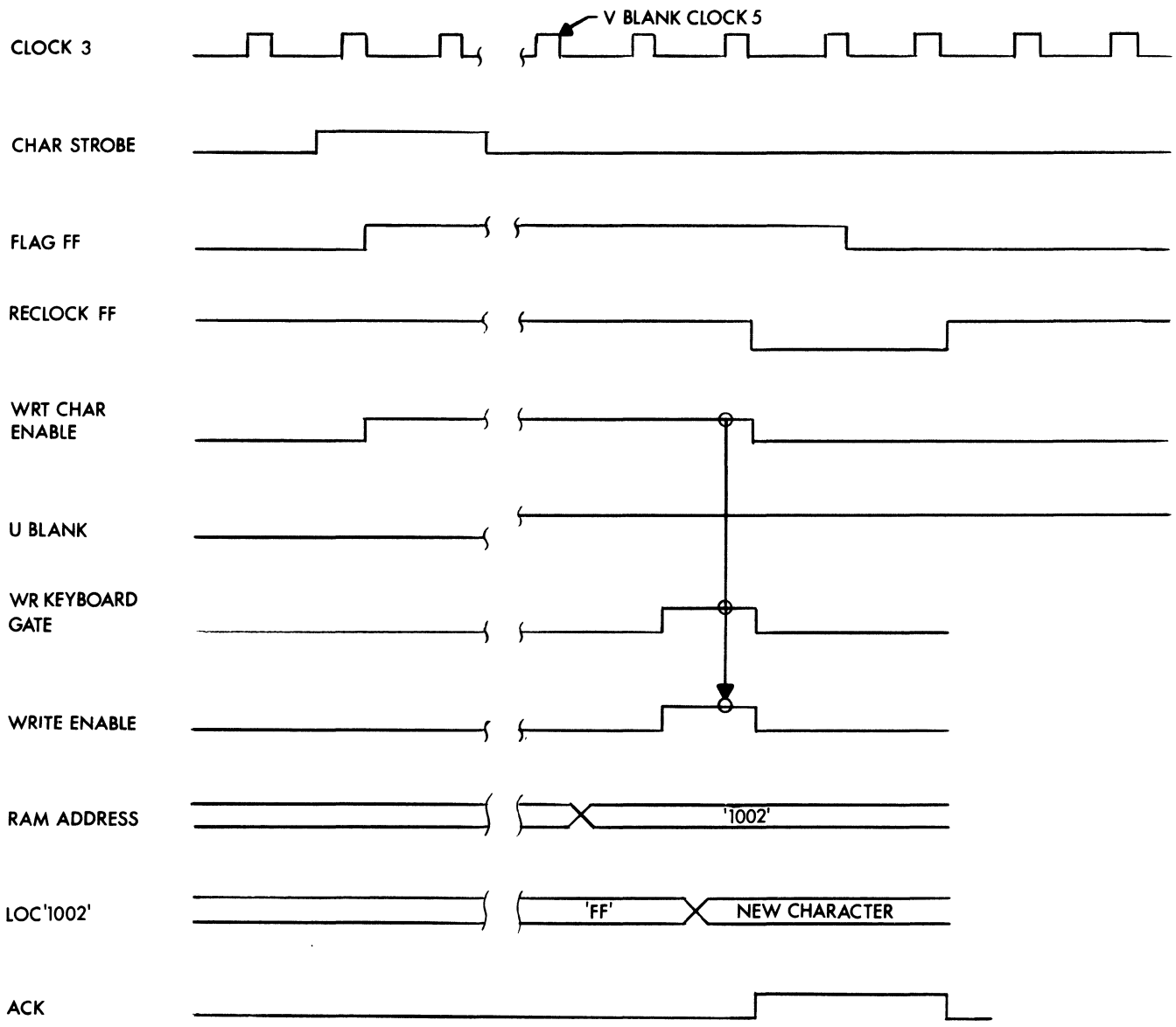


FIGURE 5-10 KEYBOARD RAM - WRITE

5.3 8080 MICROPROCESSOR

5.3.1 MICROPROCESSOR CIRCUITS

The microprocessor reads and writes into the RAM memory and communicates with peripheral devices (including the screen and the keyboard). It also establishes the screen conditions when power is first applied. Optionally, the processor board may include a 256 x 8 hardware stack and a programmable interval timer.

Figure 5-11 is a block diagram of the circuits on the processor board. The board contains an 8080 CPU, the CPU clock generator, both PROM and ROM, bus control logic and the gates and buffers needed to integrate these sections.

The clock generator provides the clocks that drive the CPU. The status latch contains the status byte transmitted during the first phase of each machine cycle. It presents this to the memory and bus control logic where the direction and synchronization of data transfers are developed.

The CPU is isolated from the system bus by the data output gate and the input latch. The processor is normally disconnected from the bus. Most of the time, the CPU will be executing programs directly from ROM and PROM. This means the CPU only infrequently references the RAM or I/O ports via the system bus. This frees the bus for RAM refresh, for video refresh, and for the DMA transfers executed by peripheral controllers.

In a typical instruction cycle from ROM or PROM, the CPU places an address on the processor board's internal address bus to access a desired item or instruction in ROM or PROM. Because no BUS REQUEST is issued, the main address gate remains disabled so the address never appears on the bus. The addressed ROM or PROM (which contains the data) places this data on the input bus (ROM 0 - ROM 7). The data will not appear on the system data bus. The data passes through the input gate to the stack bus and through the bi-directional buffer to the CPU data bus. No BUS REQUEST is issued for addresses that fall within the block controlled by the processor board.

In systems equipped with the optional 256 x 8 hardware stack, the CPU can place and retrieve data from the stack without ever issuing a CPU BUS REQUEST.

RESET gate (shown in the block diagram) is used to force a RESTART instruction into the CPU during the keyboard reset command. This is not the same as a true hardware reset of the CPU (which would destroy the data and address in the CPU.) Instead, control of the processor is transferred to location X'0008' in the firmware executive. This causes the terminal to enter the Rep Form mode without disturbing the data on the screen.

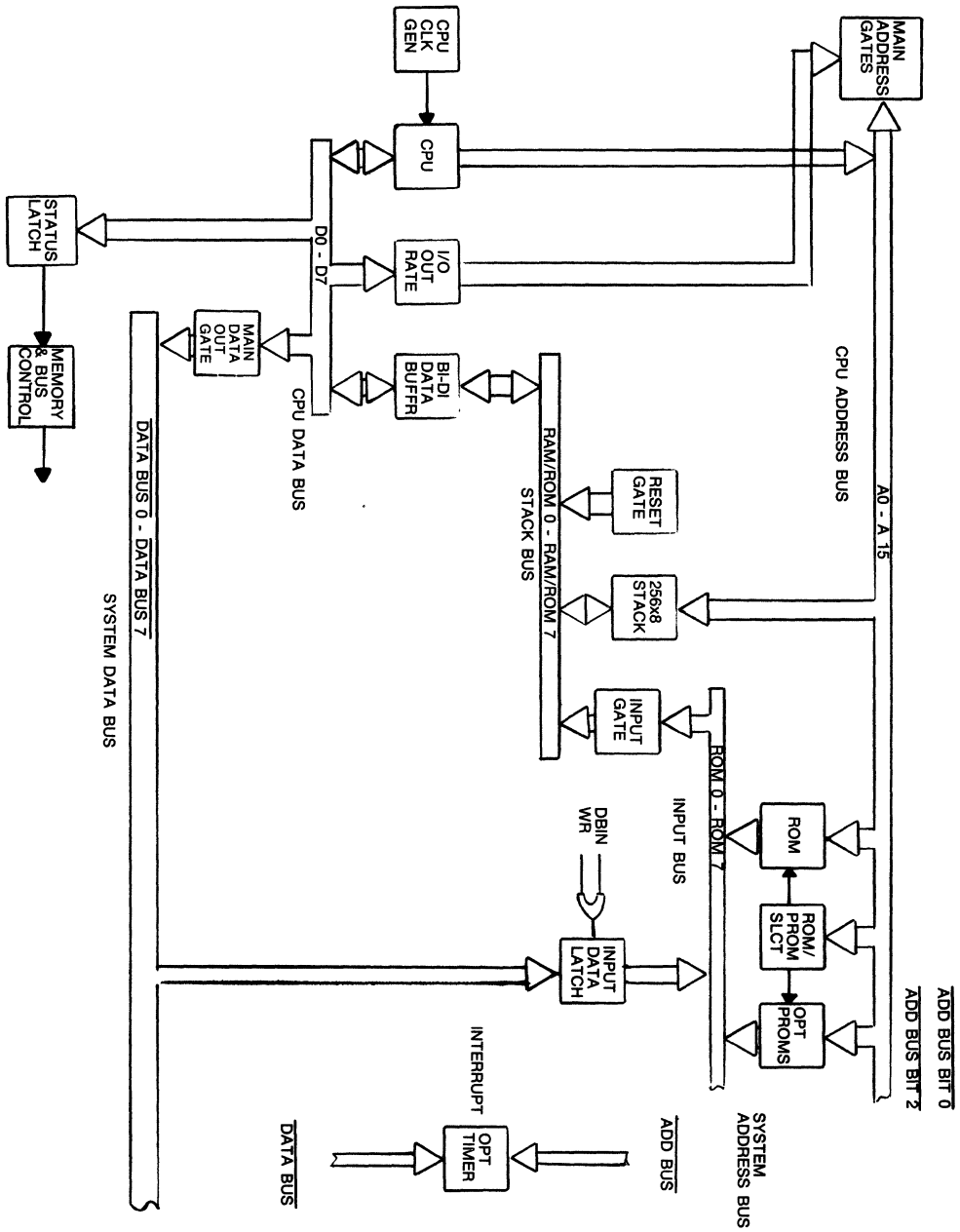


FIGURE 5-11 PROCESSOR BOARD

Addresses which are outside the range covered by the CRT's on board memory generate the memory and a CPU BUS REQUEST. This places the memory address on the system bus. The data from the addressed device returns via the system bus.

5.3.2 CLOCK GENERATOR

The clock generator is shown in Figure 96-415-03 Sheet 1. 02 is developed directly from SHIFT CLOCK. The 01 output is developed from SHIFT CLOCK and BIT CLOCK (run through a shift register delay (A11J). Both the 01 and 02 signals are conditioned MOS level signals suitable for the 8080 CPU. Timing relationships are shown in Figure 5-12.

The 8080 (Sheet 1) outputs a status byte on the data bus during the initial phase of every machine cycle. This byte provides status and directional information. The status latch is activated by the CPU's SYNC output and the leading edge of the 01 clock. (This identifies the T1 phase in each machine cycle.) Any data on the bus at this time is stored in the status latch shown on Sheet 2 A7J. The individual status bits are summarized in Figure 5-13. Status signals are available to the memory synchronization logic on Sheet 2 and the bus control and timing logic shown on Sheet 3.

5.3.3 MEMORY SYNCHRONIZATION SECTION

The memory synchronization logic consists of a programmable timer and a control flip-flop (Sheet 2).\ The concurrence of 01 and SYNC loads the status and produces an INTERRUPT output from the 8212 input/output port IC (A7J Pin 23). This is applied to the "set" input of the control flip-flop (A9D Pin 10) producing a READ output to the synchronization counter.

The READ output from the control flip-flop with the leading edge of SHIFT CLOCK 1 preloads the counter and resets the control flip-flop. The high performance 1702A PROMs used on the processor board have better access characteristics than do the ROMs. The value preloaded into the synchronization counter depends upon the type of memory being accessed. The ENABLE ROMs signal shown on Sheet 2 is developed in the chip select logic on Sheet 7 and distinguishes a ROM from a PROM. The ENABLE ROMs input with the MEMR status bit produces the READ FROM ROM signal, which selects a preload value of a decimal 13. TIMEOUT goes false when the counter is preloaded, inhibiting the READY input of the CPU as shown on Sheet 2.

The synchronization counter is incremented by the SHIFT CLOCK 1 input from the timing board. After two periods of SHIFT CLOCK, the counter's TIMEOUT output goes true, inhibiting the counter and restoring the READY input to the CPU. This process causes the insertion of two WAIT STATES between the T2 and T3 phases of the machine cycle. Timing relationships during ROM access are shown in Figure 5-14.

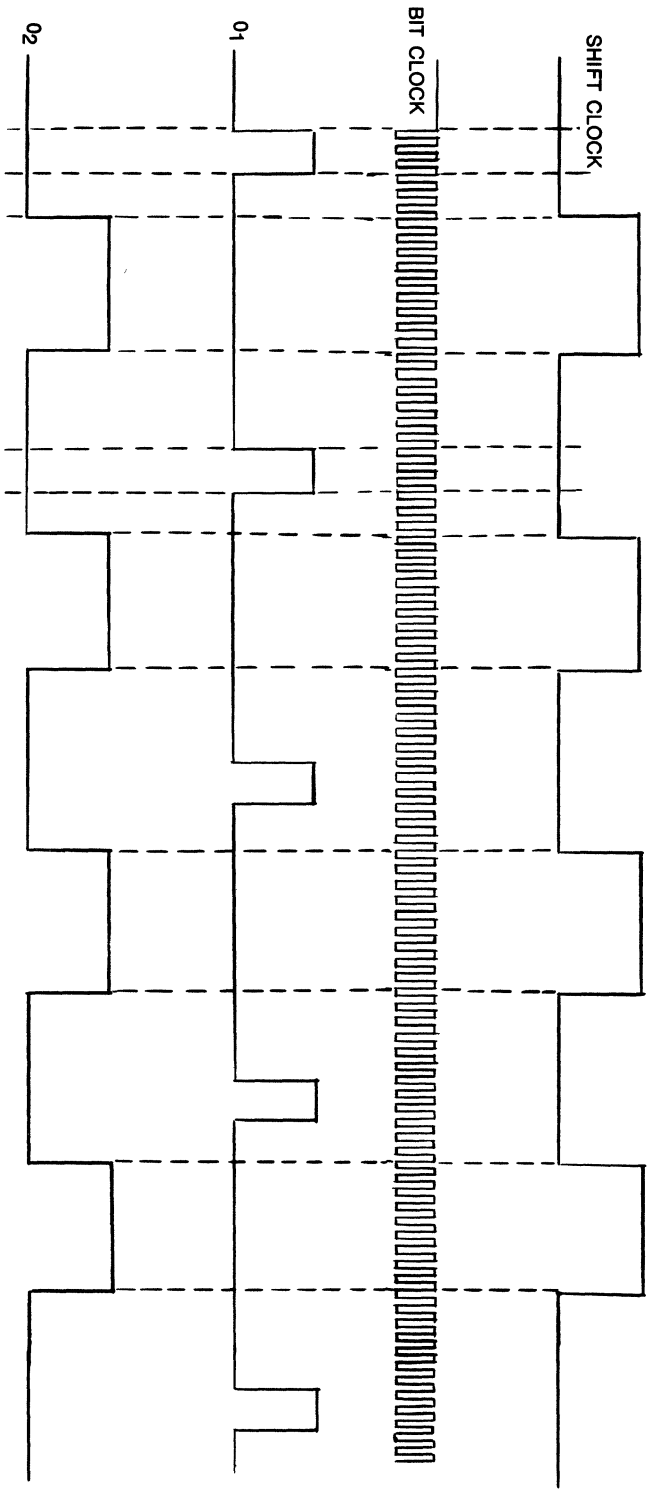


FIGURE 5-12 CPU CLOCKS

STATUS WORD CHART

TYPE OF MACHINE CYCLE

DATA BUS BIT	STATUS INFORMATION	① INSTRUCTION FETCH	② MEMORY READ	③ MEMORY WRITE	④ STACK READ	⑤ STACK WRITE	⑥ INPUT READ	⑦ OUTPUT WRITE	⑧ INTERRUPT ACKNOWLEDGE	⑨ HALT ACKNOWLEDGE	⑩ INTERRUPT ACKNOWLEDGE WHILE HALT
											← (N) STATUS WORD
D_0	INTA	0	0	0	0	0	0	0	1	0	1
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	0
D_2	STACK	0	0	0	1	1	0	0	0	0	0
D_3	HLTA	0	0	0	0	0	0	0	0	1	1
D_4	OUT	0	0	0	0	0	0	1	0	0	0
D_5	M_1	1	0	0	0	0	0	0	1	0	1
D_6	INP	0	0	0	0	0	1	0	0	0	0
D_7	MEMR	1	1	0	1	0	0	0	0	1	0

FIGURE 5-13 8080 CPU STATUS BYTE

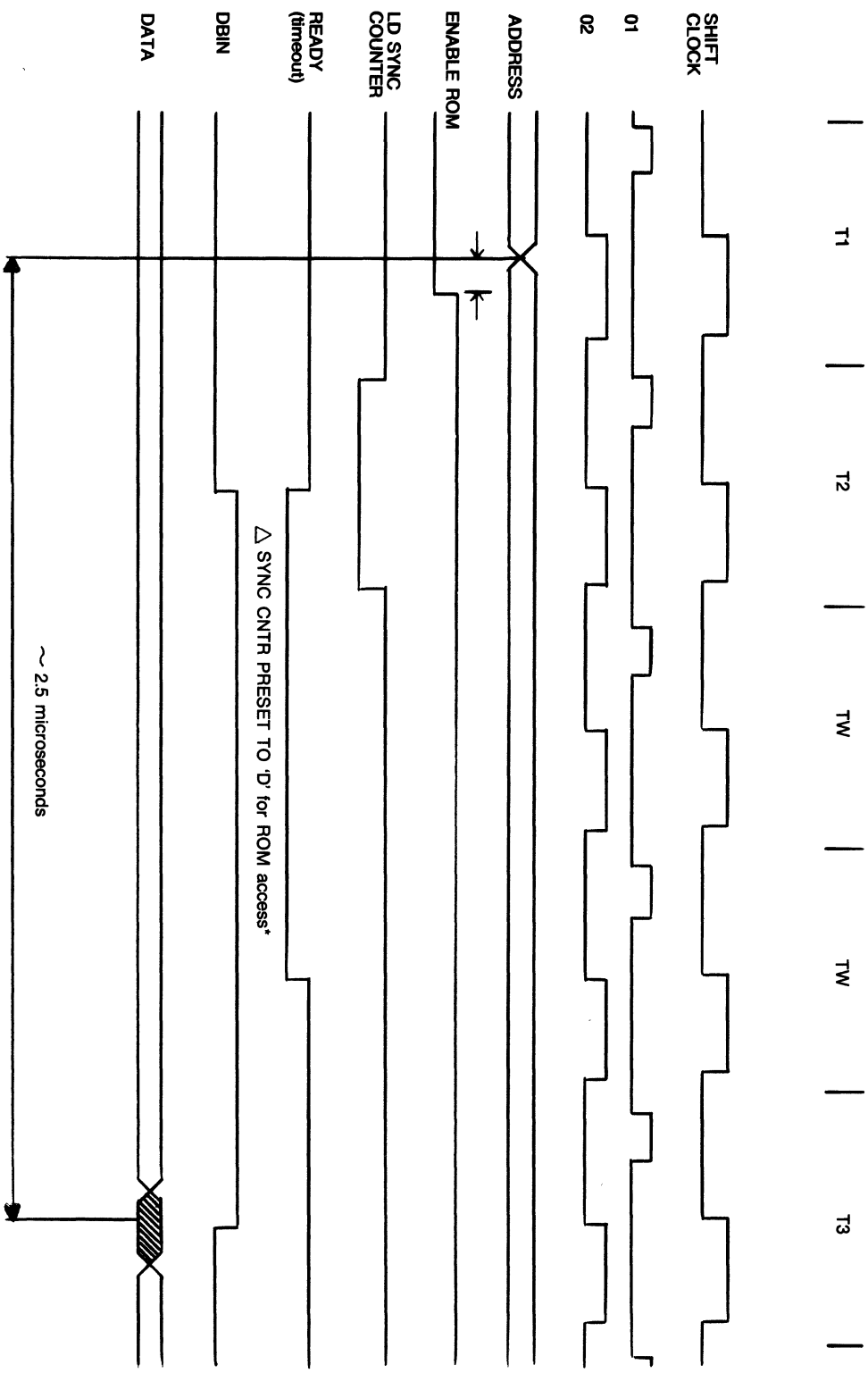


FIGURE 5-14 CPU MEMORY SYNC (ROM ACCESS)

If the processor had been accessing a PROM rather than a ROM, the ENABLE ROMs input to the synchronization logic would have been false. As a result, the preload value would be decimal 14 rather than decimal 13. The counter would timeout after only one period of the SHIFT CLOCK. allowing the CPU's machine cycle to proceed at the end of a single WAIT interval. This means the processor delays longer when reading from ROM than when reading from PROM.

Events during a RAM read are different. The dynamic RAMs used for storage in the 9003 have much better access times than either the ROMs or the PROMs. The high-speed of the dynamic RAMs is offset somewhat by the delays introduced by the system bus protocol.

Refer to Sheet 2. The synchronization counter is preloaded with a decimal 14 at the beginning of machine cycles in which RAM is referenced (just as it would if reference were to PROM). However, the synchronization counter initiates the holding state, by inhibiting the CPU's READY input for one period of the SHIFT CLOCK. The inhibition input is maintained by the SYSTEM BUS REQUEST, as shown on Sheet 2 (A10E Pin 3). SYSTEM BUS REQUEST remains true until the requested memory cycle is over. When READY goes true, the CPU proceeds to T3. The time needed for memory synchronization is 3 to 4 cycles of the 01 clock. See Figure 5-15.

5.3.4 ROM READ

The CPU reads from ROM during the fetch of an instruction. The first machine cycle of every instruction cycle begins with a fetch. A fetch is indicated by active M1 and MEMR bits in the CPU status byte. During the T1 phase, the status byte is latched in the processor's status latch as shown on Sheet 2 (A7J). The memory synchronization timer is preloaded and started during T2.

The address the CPU outputs at the start of T1 is applied to the ROM and PROM enable logic shown on Sheet 7 where it is used to distinguish ROM from PROM on the basis of address blocks. If the address falls within the ROM range, ENABLE ROM 1, ENABLE ROM 2, or ENABLE ROM 3 will be selected. The ENABLE ROMs output will be active. ROM enable is applied directly to the ROM as shown on Sheet 5. The low order (eleven bits) of the processor's address bus are decoded by the ROM to select the proper memory location. Output from the ROM goes to the ROM bus.

For the ROM output data to get to the CPU's data bus, it must pass through the gates shown on Sheet 4 (A1F and A2F). This gate is normally enabled. It is only inhibited during a reference to the on-board stack, or during a keyboard reset. The data passes through to the RAM/ROM bus where it is applied to the inputs of the bi-directional bus driver A1K/A2K. The data is forwarded to the CPU data bus where it is picked up by the processor.

5.3.4 PROM READ AND OVERLAYS

Refer to Sheet 7. A PROM read would be indistinguishable from a ROM read, except for the chip select logic. Any address that falls within the first or last 8K of the system's memory results in enabling the input to the LOW/HIGH address selector switches through A12A. Switches enable or disable outputs for each of the four 1K PROM sockets on the processor board. Each PROM bank is assigned individually to the high end or low end of system memory. Assignment is at the user's discretion. The first PROM bank is usually assigned to the lower 8K.

The upper and lower 8K address blocks are resolved into blocks of 1K by the second address decoder shown on Sheet 7 (A11B). The 1K chip selects are applied to decoders consisting of two 74155 de-multiplexers. Switches are used to enable particular multiplexer sections. The inputs of the two multiplexers are driven in parallel from the Address 8 and Address 9 inputs to further resolve the address reference into a single 256 byte quadrant within the 1K block. Each 256 byte sector is spanned by a single PROM. The outputs from the two multiplexers can be used to enable a particular PROM, as selected by the socket enabling switches shown on Sheet 7.

Whenever a CPU address falls within the range of the PROMs on the processor board, the Enable PROMs line will be active (A7C Pin 11). This inhibits the ROM Enable (A13A Pin 8) resolving any potential addressing conflicts in favor of the PROMs. This is known as overlay. Overlay lets sections of firmware in PROM supersede or supplant programs stored in ROM. Overlaying is useful for the addition of firmware options. It permits the user to patch or replace portions of the standard firmware to suit his application.

The PROM array is shown on Sheet 6. Output bytes from the PROM follow essentially the same path to the processor as do outputs from ROM.

5.3.6 SYSTEM BUS: RAM READ AND INPUT

The processor shares the bus with other devices, including the RAM refresh logic, the video refresh logic and with any peripherals that may be attached to the terminal. The processor board's support logic includes an 8-bit bus latch which serves as a holding register for all data entering the processor via the system bus. The latch is shown on Sheet 3 (A6E).

The CPU controls the direction of data transfers during input operations by its DBIN control line. Refer to Sheet 2 A11F Pin 2. DBIN is instrumental in producing the DATA LATCH ENABLE signal. This signal removes the "clear" input to the data latch on Sheet 3 (A6E Pin 14), preparing the latch to receive data.

A CPU bus request cycle begins by sending an address and a status byte in which the MEMR bit is set. Refer to Sheet 3. MEMR concurs with inactive

stack and ROM/PROM SELECT inputs to produce ENABLE READ DATA A8J Pin 6. Passing through A9J-8 ENABLE READ DATA with DBIN (in the form of DATA LATCH ENABLE) enables the DS2 input of the data latch ("device select"). The final input to the input latch comes from the latch itself (a false LATCH FULL output). This is applied to Pin 1 of the 8212 A6E (DEVICE SELECT 1).

DBIN through A10H-11 produces the ENABLE BUS REQUEST signal. This, combined with SELECT LATCH DATA produces the SYSTEM BUS REQUEST signal. At the same time, SELECT LATCH DATA removes the reset from the bus request flip-flop (A8H) permitting *CLOCK 3 to set it. This marks the beginning of a bus request cycle.

CPU WRITE DATA, READ THIS CYCLE, and WAIT signals shown on Sheet 3 are not used in the standard 9003 system. The output of the bus request flip-flop goes directly to and produces the ENABLE ADDRESS BUS signal. CPU BUS REQUEST is the signal which inhibits all other system activity during the CPU memory cycle. ENABLE ADDRESS BUS activates both halves of the address bus. Because ENABLE READ data is active, the READ DATA output at A8K-11 is true. These outputs provide the RAM array with the information necessary to complete its memory reference. The RAM responds by placing the requested data byte on the system bus.

The ENABLE ADDRESS BUS output is coupled to A9F-6. This inhibits the output that set the latch originally. The leading edge of CLOCK 3 through gate A10H-6 strobes the memory byte into the data latch. The trailing edge clears the bus request flip-flop and terminates the request cycle. At this time all CPU signals are cleared from the data bus and the request byte is stored in the data latch. The CPU will pick up the data from the data latch at the next T3 phase.

Refer to Sheet 2. The CPU's memory synchronization line (READY) is inhibited when SYSTEM BUS REQUEST is issued, and terminated upon completion of the request cycle. Three to four WAIT STATES will be inserted into the processor's machine cycle during a reference to RAM, due to inhibition of the READY LINE. The delay depends upon the phase relationship between the memory clock and the processor's clock at the time a bus request is issued. Figure 5-14 shows the timing of RAM access.

There are only minor differences between a RAM read and an input from a peripheral. Both operations initiate a CPU BUS REQUEST and both cause data to be deposited in the processor board's input latch. The method of synchronization is identical. Refer to Sheet 3.

The 8080 distinguishes between memory read and input by activating the INP status bit at the start of the input machine cycle. IN, rather than ENABLE READ DATA, acts through A9J-8 to activate the input latch. IN, operating through A10K-1, enables the Select Latch Data output to the bus request flip-flop. ENABLE COMMAND I/O will be active as a result of the IN status bit. This

activates the COMMAND I/O control line on the system bus. COMMAND I/O distinguishes an input operation from a memory read. There is no directional control information on the system bus during I/O operations. COMMAND I/O will be true during both input and output. It is the responsibility of the peripheral to distinguish between an input and an output operation on the basis of device address. During I/O references, the upper 8 bits of the CPU's address bus represent the object address. This same information is displayed on the lower half of the address bus but is not used.

5.3.7 SYSTEM BUS: RAM WRITE AND OUTPUT

The CPU begins every memory write cycle by sending the status byte X'0'. The negative true WO flag is the only active bit. The destination address is placed on the processor's data bus during Tl. At the end of T2 the WR output indicates the direction of transfer. Data from the accumulator is placed on the bus during the T2 phase and remains valid throughout the duration of the WR output. Synchronization between the CPU and RAM is achieved by inserting WAIT states (TW) between the T2 and the T3 phases of the machine cycle. WR remains true from the end of T2 to the end of T3, regardless of the number of intervening WAIT states necessary to ensure synchronization.

Refer to Sheet 3. The WO status bit (and the absence of the STACK and OUT flags) produces the the ENABLE WRITE DATA signal. After buffering ENABLE WRITE DATA goes to the bus gate logic. At the same time, ENABLE WRITE DATA is applied to A9H-8 where it activates the SELECT LATCH DATA output and removes the reset clamp on the bus request flip-flop. (A8H Pin 1.) SELECT LATCH DATA is also coupled to A9F-13 where WR (acting through DATA LATCH ENABLE) concurs to produce SYSTEM BUS REQUEST. CLOCK 3 sets the bus request flip-flop to initiate the CPU BUS REQUEST. Both halves of the system address bus are enabled. The bus control gate (A8K) is enabled permitting the WRITE DATA output to apear on the control bus. The coincidence of ENABLE ADDRESS BUS and WO produces the ENABLE DATA BUS output at AlOK-10.

5.3.8 HARDWARE STACK OPTION

A stack is a portion of read-write memory assigned specifically to the storage and recall of selected status items.

The 8080 CPU distinguishes between stack references and other memory references by means of the STACK STATUS flag. This bit is active only during CALLS and RETURNS from subroutines or during PUSH or POP instructions which are associated specifically with stack management.

The on-board stack is two 256 x 4 static RAMs. Refer to Sheet 4 AlJ and A2J. These are addressed directly from the processor board's internal address bus. Only the low-order eight bits of address are significant to the stack.

Refer to Sheet 2. The STACK bit in the processor's status latch is coupled to the support logic via the on-board selector switch A13-S8. Stack references are handled the same way as references to PROM. The READ FROM ROM signal produced by A13C-6 will be inhibited whenever the STACK flag is active. Refer to page 4. The STACK bit is combined with DBIN or WR to enable the two memory devices. Directional control is provided by the WRITE STACK DATA output (developed from the coincidence of the STACK status bit and WR.) Data passes between the CPU and the stack via the bi-directional driver (A1K, A2K)

5.3.9 PROGRAMMABLE TIMER OPTION

The programmable timer lets the programmer construct time delays that are independent of program execution. This improves processing efficiency by eliminating the need for programmed timing loops and continuous device polling. The programmed timer consists of a 4-stage binary counter and control logic, installed on the processor board.

The timer makes use of the CPU's input/output system to load the counter with a 16-bit binary value. The counter is driven by the eighth submultiple of the SHIFT GATE to produce incremental time delays in the range of .5 milliseconds to approximately 32.8 seconds. When the programmed interval times out, the processor is interrupted. Program control is vectored to location X'0010' (by forcing an RST 2 instruction onto the processor's ROM bus).

Sheet 8 shows the timer logic. Operation begins with the loading of two bytes into the presettable counter. The low-order byte is addressed to output port X'3C', the high-order byte is addressed to output port X'3E'. The two bytes may be loaded in any order. Both A7C-6 and A7C-8 are enabled whenever an output address of X'30' to X'3F' is selected. The outputs of these two gates are combined with the Clock 2 pulse from the timing board to produce load strobes and clocks for the two halves of the counter. Loading either the upper or lower byte of the timer resets the two control flip-flops shown on Sheet 8 A8D and clears the timer's clock counter A9E.

SHIFT GATE (used to drive the clock counter) is an inverted horizontal blanking signal, and its eighth sub-multiple is used to clock the delay counter. The first TIMEOUT CLOCK is applied to the counter approximtely 501 microseconds later. Succeeding clocks recur at 501 microsecond intervals which becomes the basic timer increment.

The counter is loaded with the ones complement of the value programmed. TIMEOUT DONE goes true as soon as the preset interval has elapsed. The next SHIFT CLOCK sets the TIMEOUT DONE flip-flop (A7E) and issues a TIMER INTERRUPT.

The CPU acknowledges an interrupt request by broadcasting the INTA status bit during the T1 phase. Refer to Sheet 8. TIMEOUT DONE and the TIMER INTERRUPT

output set the acknowledge flip-flop A80. The TIME OUT flag output goes true at this time.

Refer to Sheet 4. TIMEOUT flag produces an active RESTART (A12F Pin 8). RESTART is combined with M1 STATUS to produce the WAIT FOR RESTART signal. WAIT FOR RESTART inhibits ROM data gate and forces a hardwired RST 2 instruction onto the RAM/ROM bus. This instruction is picked up by the processor and used to vector the machine to address X'0010'.

The trailing edge of WAIT FOR RESTART is used to clock flip-flop A8D Pin 11 (Refer to Sheet 8) terminating the TIMER INTERRUPT and cancelling the TIMEOUT Flag. At the end of the timer cycle, the clock counter (A9E) is inhibited by the output of the TIMEOUT flip-flop A7E Pin 8. The counter remains in this state until restarted by the program. The timer is disabled by the occurrence of either power-up or keyboard reset.

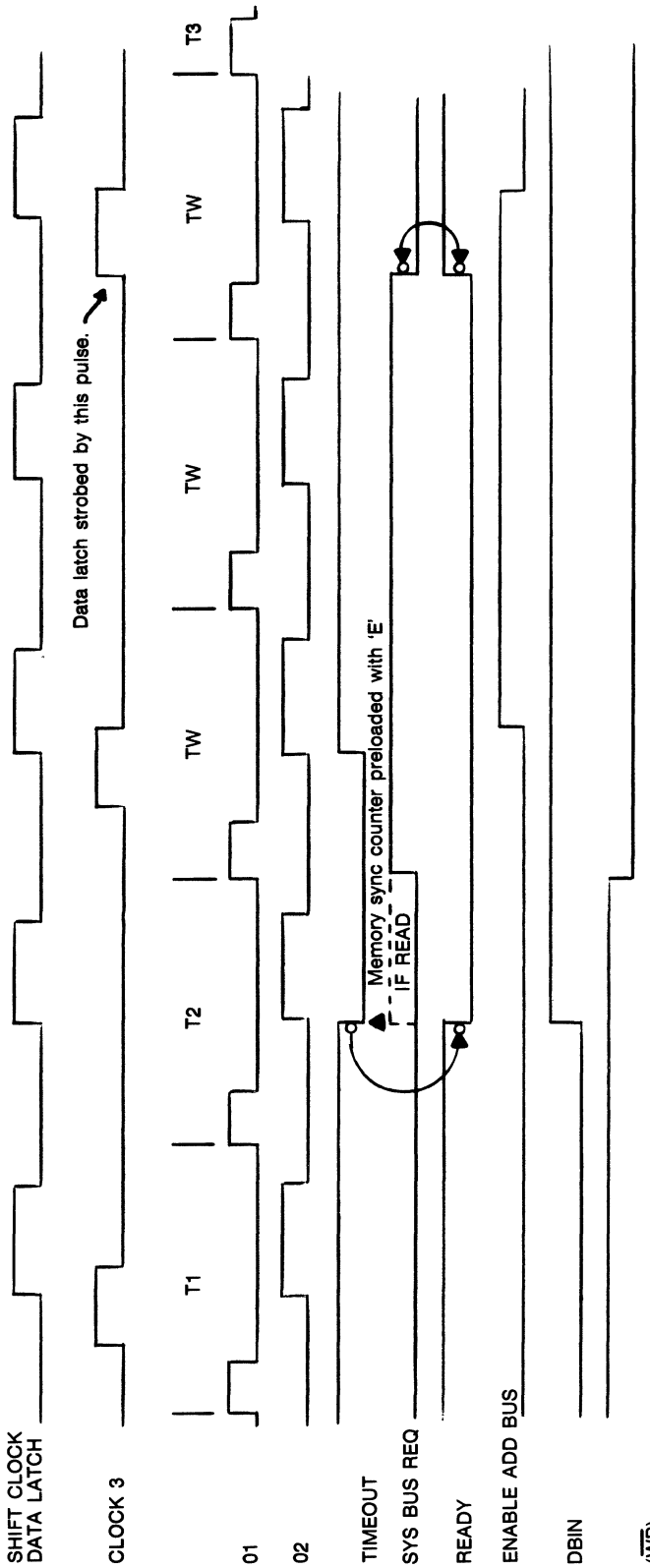


FIGURE 5-15 CPU BUS REQUEST AND MEMORY SYNC (RAM REFERENCE)

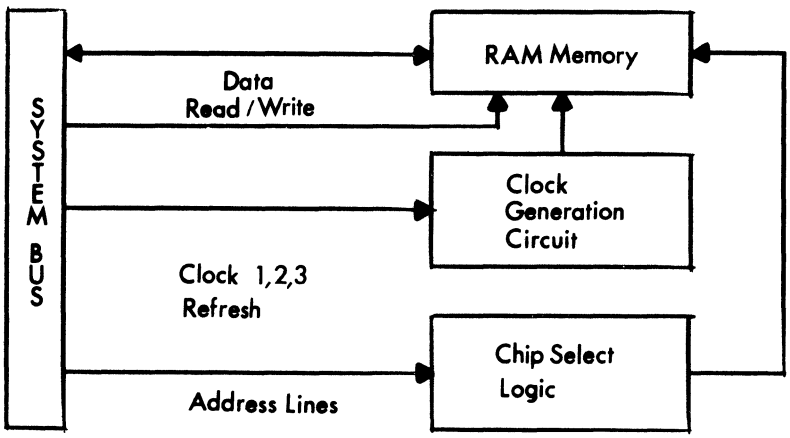
5.4 16K RAM

ZENTEC offers two extended memory printed circuit boards. These options are identified in Section 1 (Paragraphs 1.10 and 1-.15). Both PCB's utilize the same design concepts. In fact, the only difference between the two PCB's is the amount of address decoding logic necessary to define the amount of RAM memory accessed.

The 16K RAM PCB consists of eight 2K banks of random access memory IC's. Eight chip select lines are necessary to select the appropriate 2K bank of RAM to be utilized. (2K x 8 = 16K) Each RAM contains 2048 bit locations or addresses. Therefore, there are eleven address lines (2 to the eleventh power = 2048).

ZENTEC utilizes dynamic RAM memory. This means that the memory must be refreshed or the data contained within the RAMs will be lost. (The same principle is used on the character refresh PCB).

A block diagram of the extended memory PCB is shown below. Address information from the data bus is decoded to enable the desired segment of memory (RAM). If this is a write sequence, data from the data bus will be written into the RAM memory. For the actual writing of data to take place, WRITE ENABLE must be active. For a read sequence, the address information is decoded, READ DATA is enabled, and the data is placed on the data bus by the RAM. Because dynamic RAM's are used, the memory must be periodically refreshed. This is accomplished accomplished by clocking the RAMs with CLOCK 3 when the MEMORY REFRESH REQUEST line is active.



Refer to schematic drawing number 96-419-01 Rev B in Section 7.

Sheet 1 of the schematics shows the CHIP SELECT decoding, CLOCK input and the memory refresh request logic. Address bus bits 11 through 15 are decoded by IC's A3H and A2HB to produce the appropriate CHIP SELECT signal. The CHIP SELECT signal is then fed to the RAM array where it enables the designated 2K block of RAM.

MEMORY REFRESH REQUEST passes through IC A5H Pins 2 and 4 to enable IC's A5G and A4H. These IC's in turn enable A8H, A7G, A8G, and A6G. Memory refresh also goes to the aforementioned IC's via A9H Pin 11. This combination of gating allows clock 43, 33, 23, and 13 to be active whenever memory refresh is active. These clocks are all identical (they are all derived from Clock 3 through IC A6H).

Clocks 13 and 23 go to Sheet 7 where they are converted to voltage levels acceptable to the RAM's (+5V to -15V levels). The resultant output is known as M1 CLOCK 3 and M2 CLOCK 3. Clocks 33 and 43 go to Sheet 8 where the same voltage level translation takes place. The output of the voltage translator is known as M3 CLOCK 3 and M4 CLOCK 3.

These clocks refresh the RAM memory whenever memory refresh request is active. WRITE DATA signal is active (Sheet 1 IC A9H Pin 12) and the address decoding circuitry (A3H and A4G) is enabled.

Clocks 11, 21, 31, and 41 are derived from CLOCK 1. Clocks 12, 22, 32, and 42 are derived from CLOCK 2. These clocks go through the same level translation circuitry that Clocks 13, 23, 33, and 43 went through.

Sheet 2 of the schematics shows the address bus bits as they come off of the system bus. These bits are used to select the appropriate address within a 2K RAM block. It makes no difference if the operation to be performed is a read or a write. The address logic is always used in the same manner. The only difference being the READ DATA or WRITE ENABLE signals.

The dynamic RAMs require +8.5V, -15V, and +5VDC to operate. These voltages are filtered by the inductive capacitive filtering network shown on Sheet 2 to prevent voltage spikes from effecting the RAMs.

Sheet 2 also contains the data bus output driver IC's. Data from the RAMs is converted to TTL logic levels on Sheet 7 of the schematics and then sent through IC's A10H and A10G on Sheet 2 (if read data gate is active) to the data bus. Data from the data bus goes through IC's A9G, A11H, and A11G to the RAM array.

Sheets 3, 4, 5, and 6 contain the RAM arrays.

Sheet 7 contains the RAM output to TTL logic level conversion circuitry and the clock voltage level translation circuitry.

Sheet 8 contains the remaining clock voltage level translation circuitry as well as the filtering networks for the PCB's operating voltages.

SECTION 6

6.0 POWER SUPPLY ADJUSTMENT PROCEDURES
6.1 SELF TEST INTERPRETATION
6.2 PHOTOGRAPHS OF PRINTED CIRCUIT BOARDS

6.0 POWER SUPPLY ADJUSTMENT PROCEDURE

The ZENTEC 9003 uses four power supplies. These are a 12V, 5V, 3.5V, and a -15V supply. The 3.5 volt supply is referenced to the +5 Volt supply to form 8.5 volts. To access the potentiometers. first remove the cover. This is accomplished by removing the two screws on the rear of the terminal and sliding the cover off.

The +12V and the 3.5V supplys have only one potentiometer. This is the voltage adjust pot. The +5V and -15V power supplies have 3 potentiometers each. These are the voltage adjust, over voltage protection, and current limiting pots.

The voltage adjust pots are accessible without removing the monitor assembly (See Figure 6-1). The 5 volt supply should be adjusted first, and then the 3.5V supply. This insures the 8.5V output will be correct. The -15V and 12V supplies may be adjusted in any order.

WARNING!!

REMOVE ALL PCB'S PRIOR TO ADJUSTING POWER SUPPLIES.

The voltage test points are shown in Figure 6-2.

The voltages at the test points should be within + 2% of the specified value.

-15V + .3V
12V + .24V
5V + .10V
8.5V + .17V

After the voltages are set, re-install the PCBs and trim the power supplies to the desired voltage.

It is recommended that the OVP and current limit pots not be adjusted unless a new supply is being installed. These pots are preset at the factory. Should it become necessary to adjust these potentiometers, the following precedure should be used:

1. Remove the monitor assembly by taking out the five screws which hold it in place. (One at each corner and one on the 'L' bracket which fastens to the card cage.) Disconnect the AC power and logic interface plug and lift monitor clear.

2. Remove all PCB's from card cage.

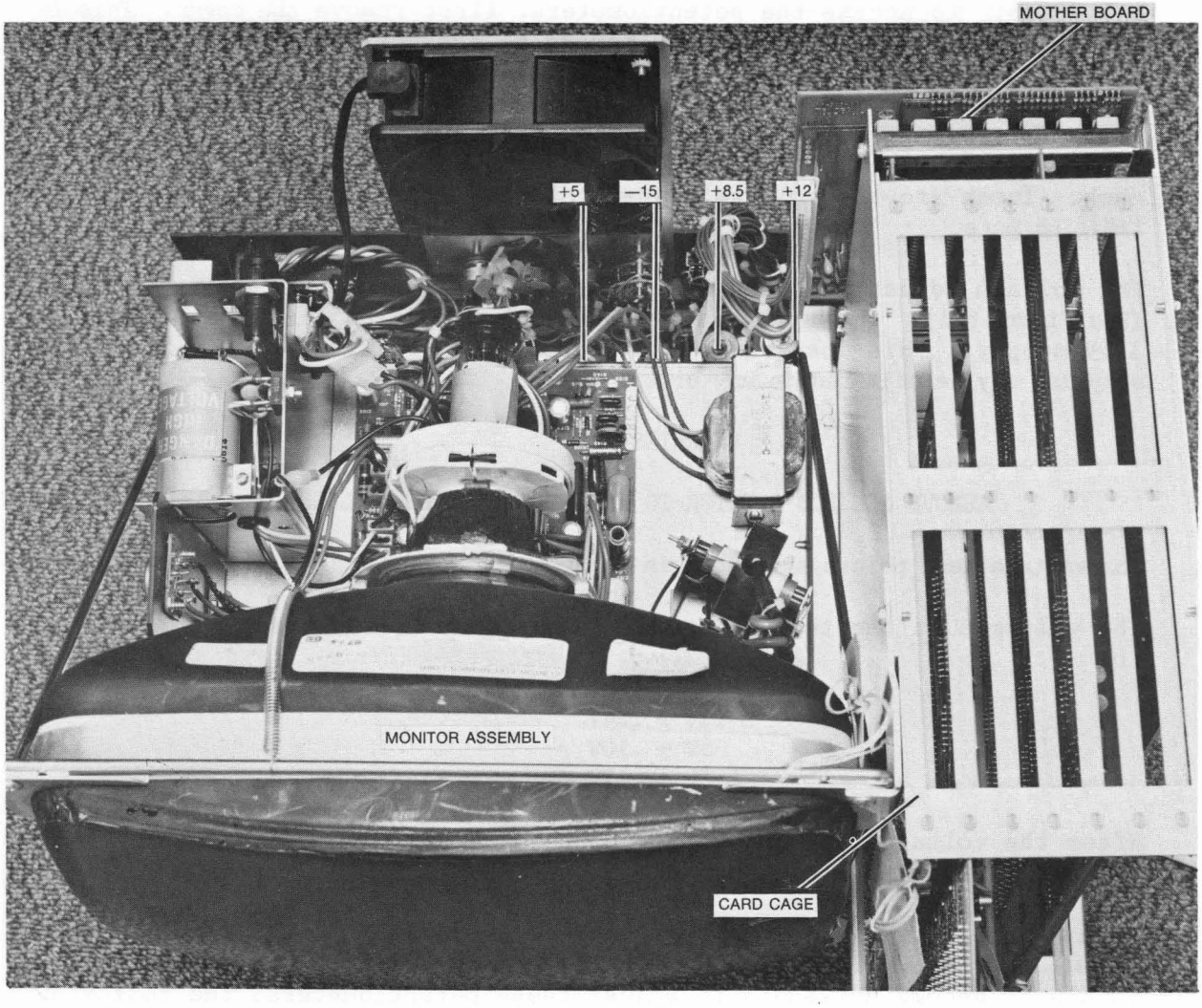


FIGURE 6-1 MONITOR ASSEMBLY SHOWING VOLTAGE ADJUST POWER SUPPLIES

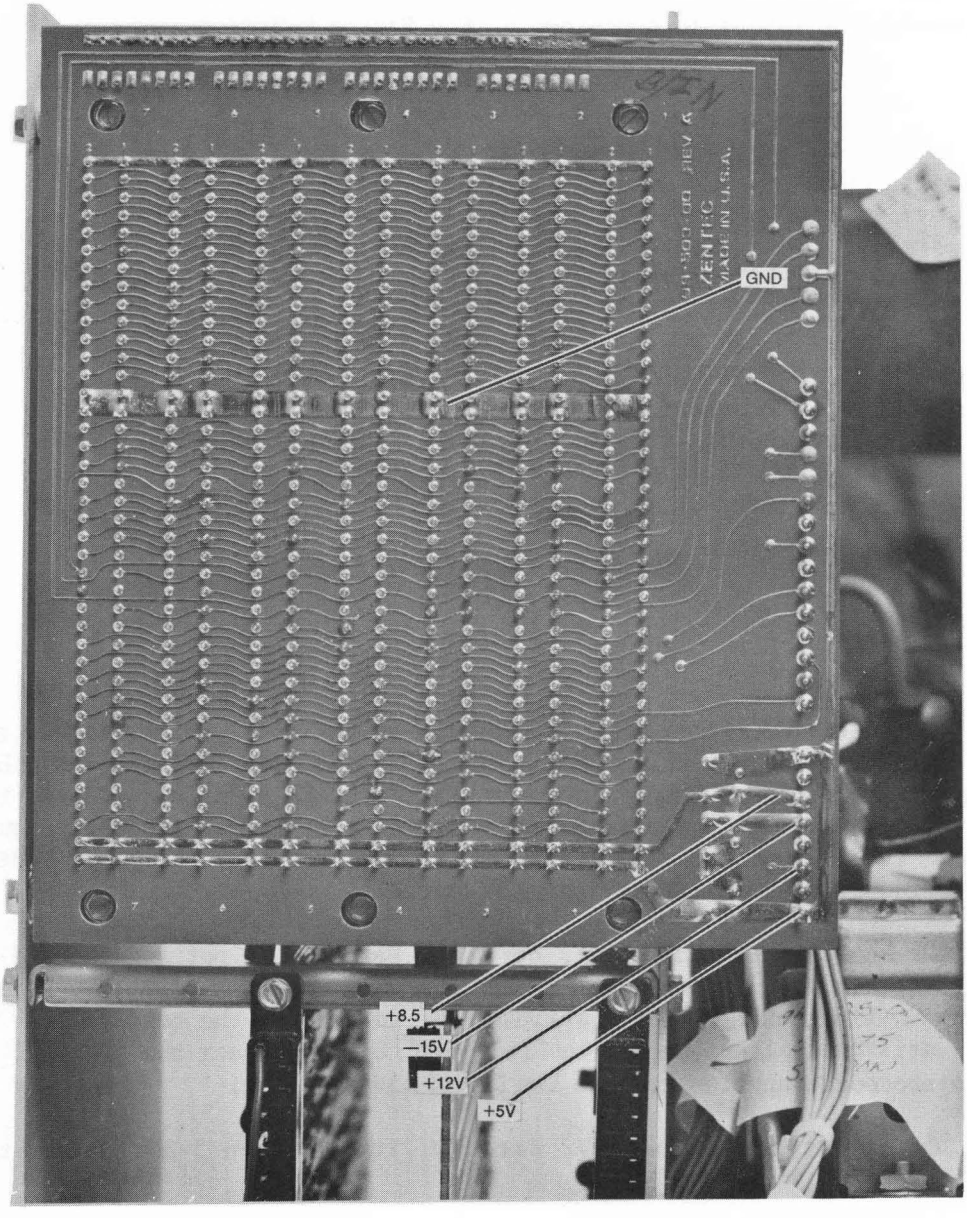


FIGURE 6-2 MOTHERBOARD PCB SHOWING VOLTAGE TEST POINTS

3. Use the test points shown in Figure 6-2.

4. Both the 15 volt and 5 volt supply are layed out the same (as far as the potentiometer layout is concerned.) See Figure 6-3.

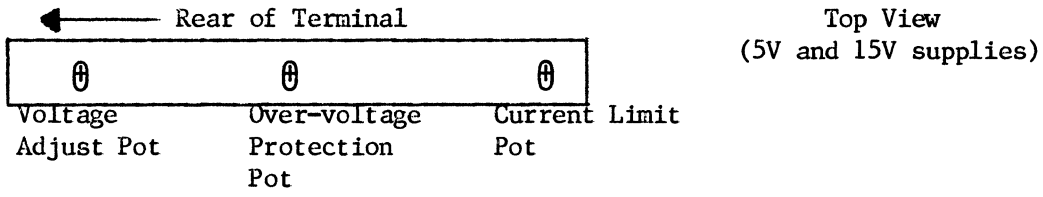


FIGURE 6-3

5. Set the voltage output for the 15V supply at 17 volts. Adjust the OVP pot until the voltage begins to "fall off". Turn the power off and set the voltage adjust pot for some value less than 17V. Turn the power on and trim the voltage adjust pot until 15 volts is measured at the test point. (The power supply will clamp if the voltage output exceeds the OVP setting. The power must be cycled (on-off-on) to re-initialize the OVP circuit.

6. To set current limiting, be sure that the OVP pot and voltage adjust pot are properly set. Install all of the PCB's turn the power on and adjust the current limit pot while observing the voltage at the test point. Rotate the pot until the voltage begins to "fall off" and then back the pot off 1/4 turn. This procedure applies to both the 5 and 15V supplies.

7. To adjust the 5 volt OVP circuit, follow step 5 except set the voltage output to 7V.

6.1 SELF TEST INTERPRETATION

Self Test is a specially designed diagnostic progrm which verifies correct operation of the microprocessor, all memory and the display. Keyboard operation involves: Depress MODE key to go into the CONTROL MODE, then depress SCROLL UP key. A special test will be executed. To exit this mode, and clear screen, depress the RETURN key. To erase the test results from the 25th line depress ERASE DISPLAY twice.

On detecting a failure in memory, Self Test indicates the address of the failure on the 25th line. The address is provided in the form of four hexadecimal digits that should be interpreted as follows:

first digit	second digit	third digit	fourth digit

The first and second digits indicate starting address of 2KB chip in which the error occurred. The third and fourth digits indicate the horizontal bit positions in which the error occurred. If converted to an 8-bit binary pattern then each "1" indicates a bit failure and each "0" indicates a bit O.K.

Example

Consider eight 2048 x 1 chips making 2KB memory with starting address of X'1800', bytes read from the chip have the pattern.

Bit Position= 7 6 5 4 3 2 1 0

During Self Test, errors are detected in bits 0 and 2. In binary, this pattern becomes:

Bits Failed= 0 0 0 0 0 1 0 1

Where 1= bit failed and 0= bit O.K.

This pattern translates to X'05' and since starting address of chip is X'1800', Self Test provides the failure address as 1805 which locates the failure to the chip level.

See Page 6-9 for memory address designations on 16K RAM PCB.

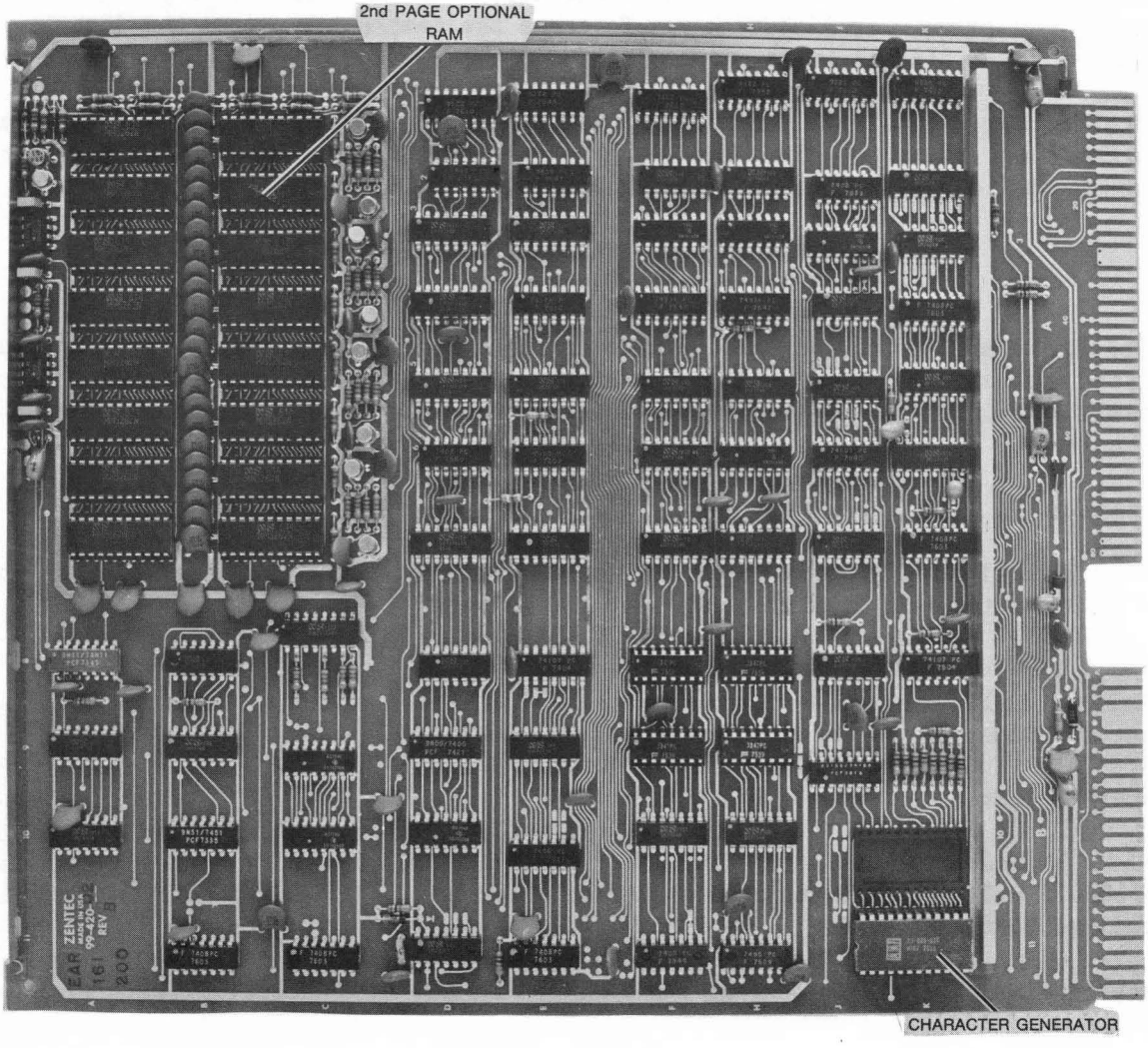


FIGURE 6-4 CHARACTER REFRESH BOARD SHOWING SECOND PAGE OPTIONAL RAM

FIGURE 6-5 SYSTEM TIMING PCB

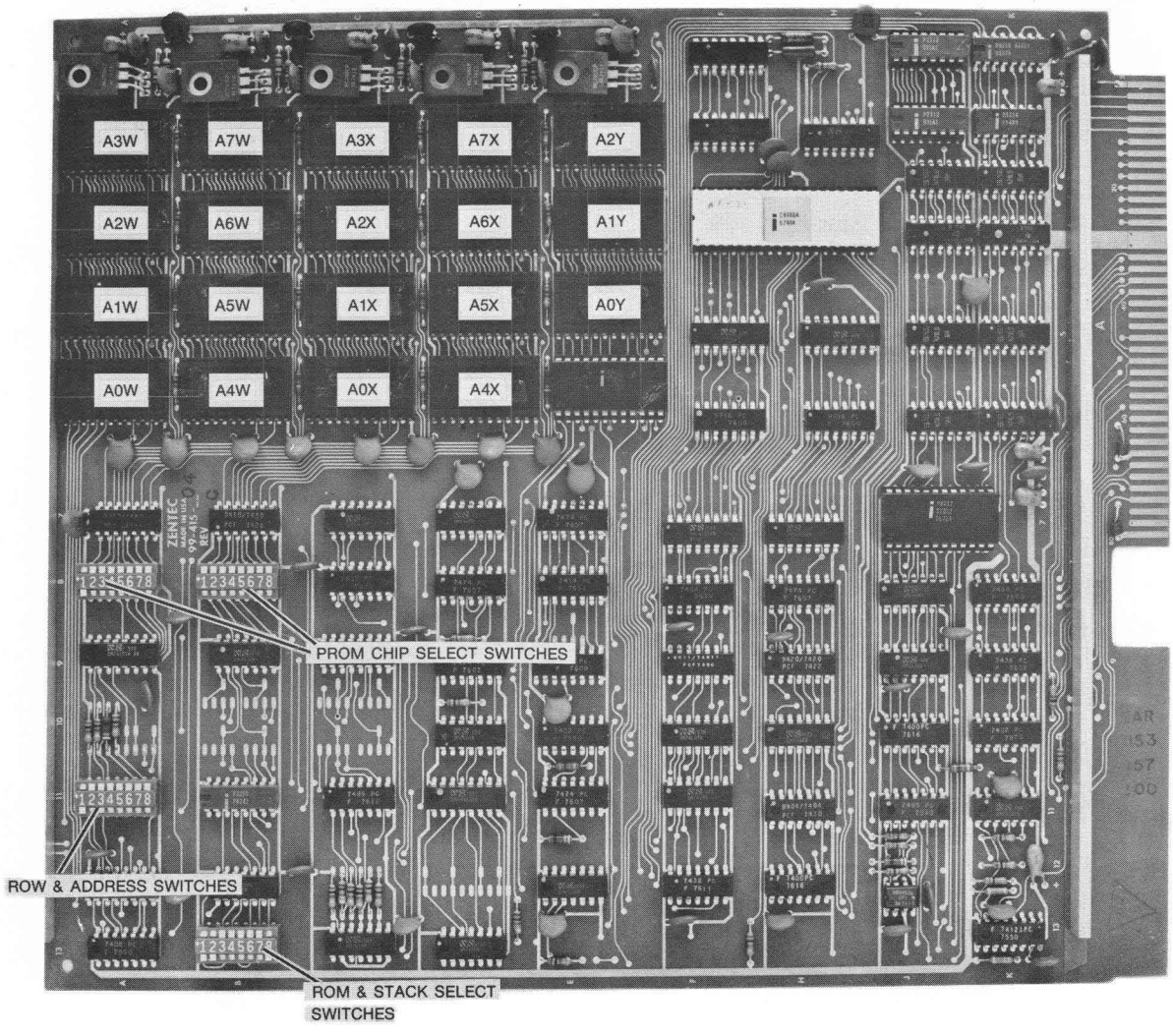


FIGURE 6-6 8080 MICROPROCESSOR PCB

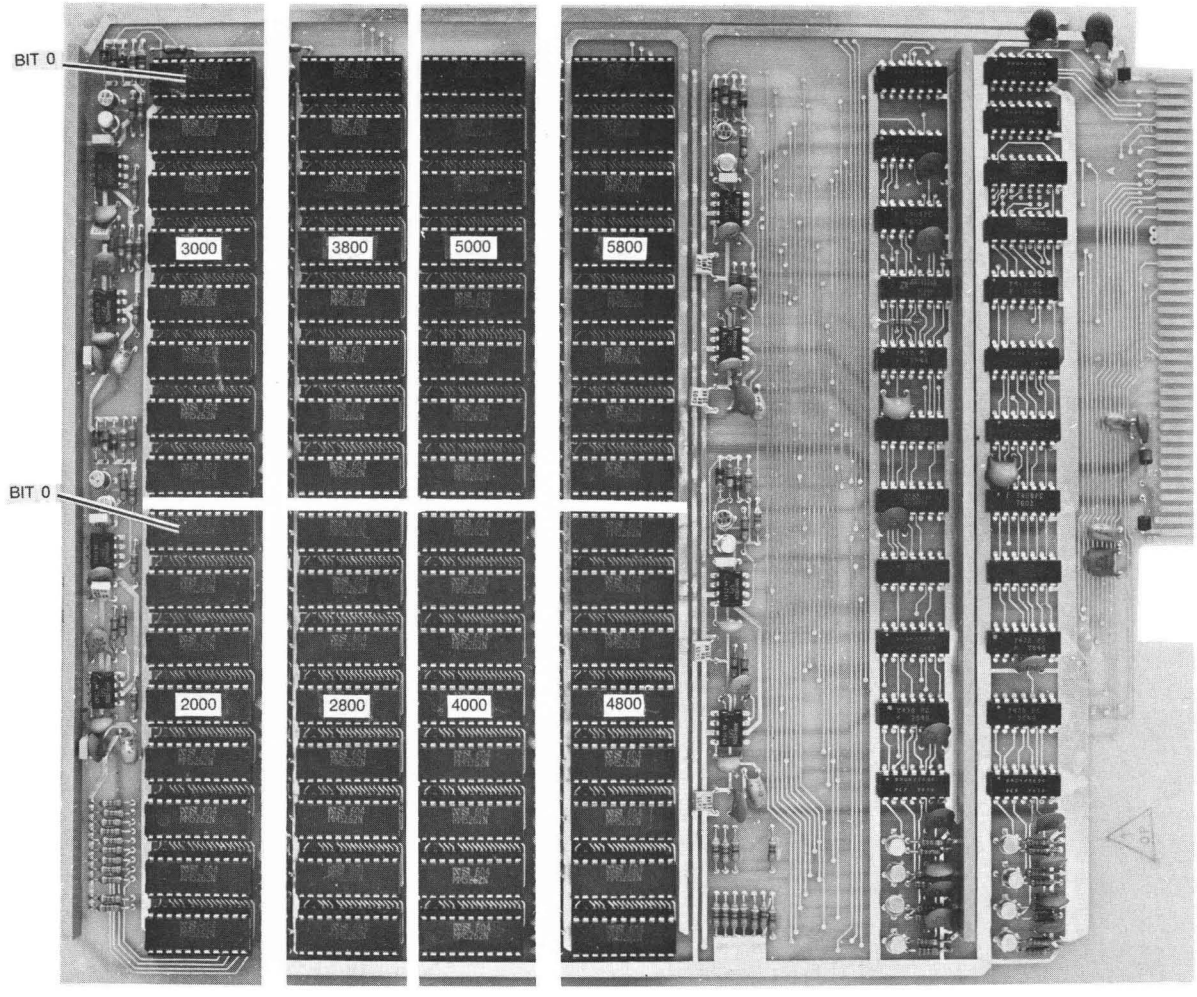
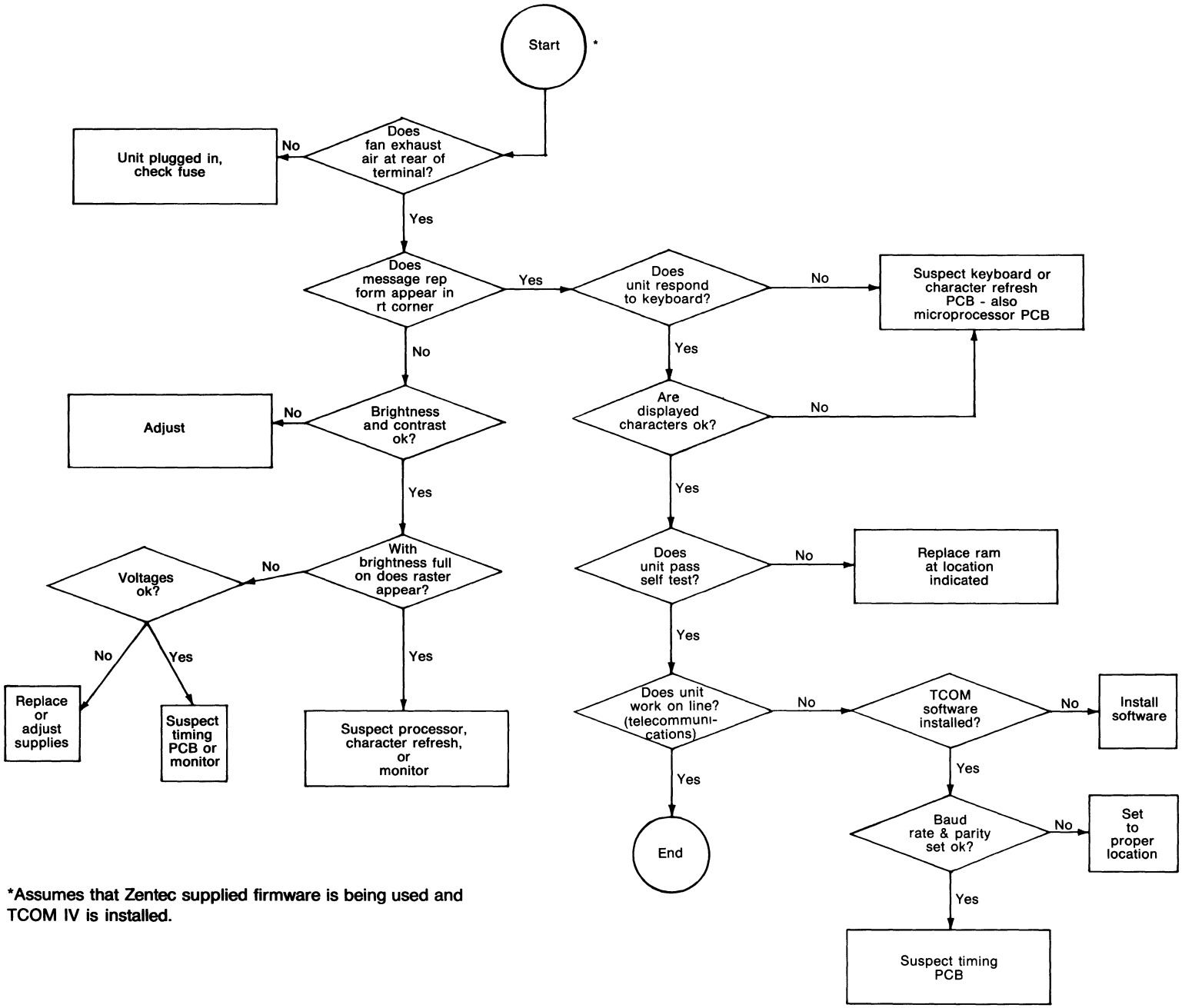


FIGURE 6-7 16K RAM PCB

SECTION 7

SCHEMATICS

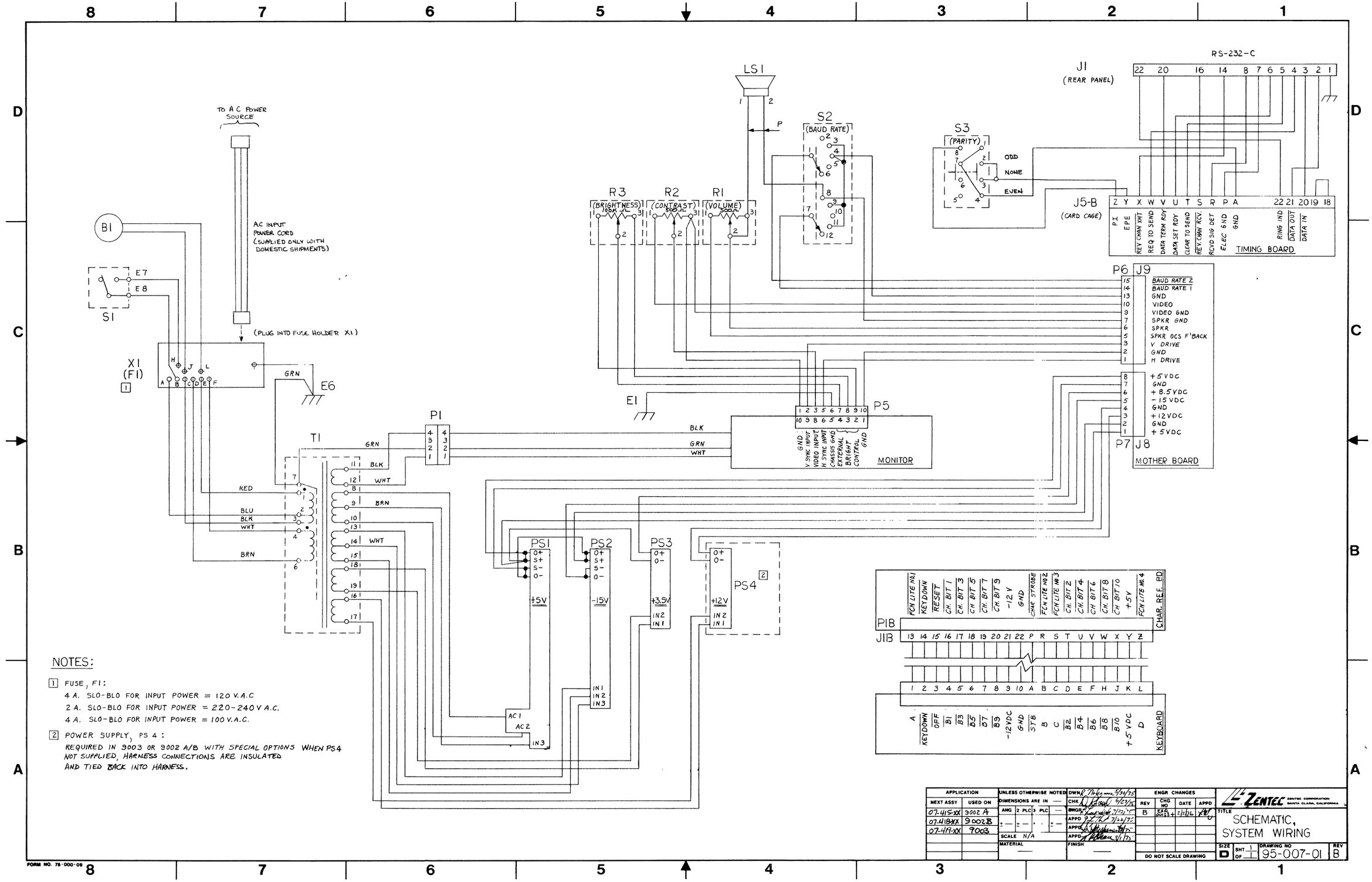


*Assumes that Zentec supplied firmware is being used and TCOM IV is installed.

SYSTEM TIMING PCB

ASYNCHRONOUS RS-232C INTERFACE CONNECTOR (J1)

PIN #	FUNCTION
1	SAFETY GROUND
2	DATA OUT
3	DATA IN
4	REQUEST TO SEND
5	CLEAR TO SEND
6	DATA SET READY
7	SIGNAL GROUND
8	NOT USED
9	NOT USED
10	NOT USED
11	NOT USED
12	NOT USED
13	NOT USED
14	REVERSE CHANNEL TRANSMIT
15	NOT USED
16	REVERSE CHANNEL RECEIVE
17	NOT USED
18	NOT USED
19	NOT USED
20	DATA TERMINAL READY
21	NOT USED
22	RING INDICATOR
23	NOT USED
24	NOT USED
25	NOT USED



NOTES:

1. FUSE, F1:
   - 4 A. SLO-BLO FOR INPUT POWER = 120 V.A.C
   - 2 A. SLO-BLO FOR INPUT POWER = 220-240 V A.C.
   - 4 A. SLO-BLO FOR INPUT POWER = 100 V.A.C.
2. POWER SUPPLY, PS 4:
   REQUIRED IN 9003 OR 9002 A/B WITH SPECIAL OPTIONS WHEN PS4 NOT SUPPLIED, HARNESS CONNECTIONS ARE INSULATED AND TIED BACK INTO HARNESS.

APPLICATION	
NEXT ASSY	USED ON
07-415-XX	9002 A
07-418-XX	9002 B
07-411-XX	9003

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN —
ANG ± — | 2 PLC ± — | 3 PLC ± —
SCALE N/A
MATERIAL —
FINISH —

DWN	R. McKenna	5/29/75
CHK	D. Brand	6/23/75
ENGR	D. Brand	7/22/75
APPD	[illegible]	7/22/75
APPD	[illegible]	7/22/75
APPD	[illegible]	8/1/75

ENGR CHANGES

REV	CHG NO	DATE	APPD
B	ECO 0023	2/24/76	

DO NOT SCALE DRAWING

ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA

TITLE: SCHEMATIC, SYSTEM WIRING

SIZE D | SHT 1 OF 1 | DRAWING NO 95-007-01 | REV B

FORM NO. 75-000-09

NOTES:
1. ALL RESISTOR VALUES ARE 1K OHMS
2. ALL CAPACITOR VALUES ARE IN MFD.

APPLICATION	
NEXT ASSY	USED ON
99-503-01	9002
99-503-01	9002 A/B
99-503-01	9003
99-503-01	KDS-7810R
99-503-01	TZ201
SEE STATUS CARD	

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN — ANG 2 PLC 3 PLC — ± -- ± -- ± --
SCALE NONE
MATERIAL
FINISH
DO NOT SCALE DRAWING

DWN ECT 8-11-75
CHK
ENGR
APPD
APPD
APPD

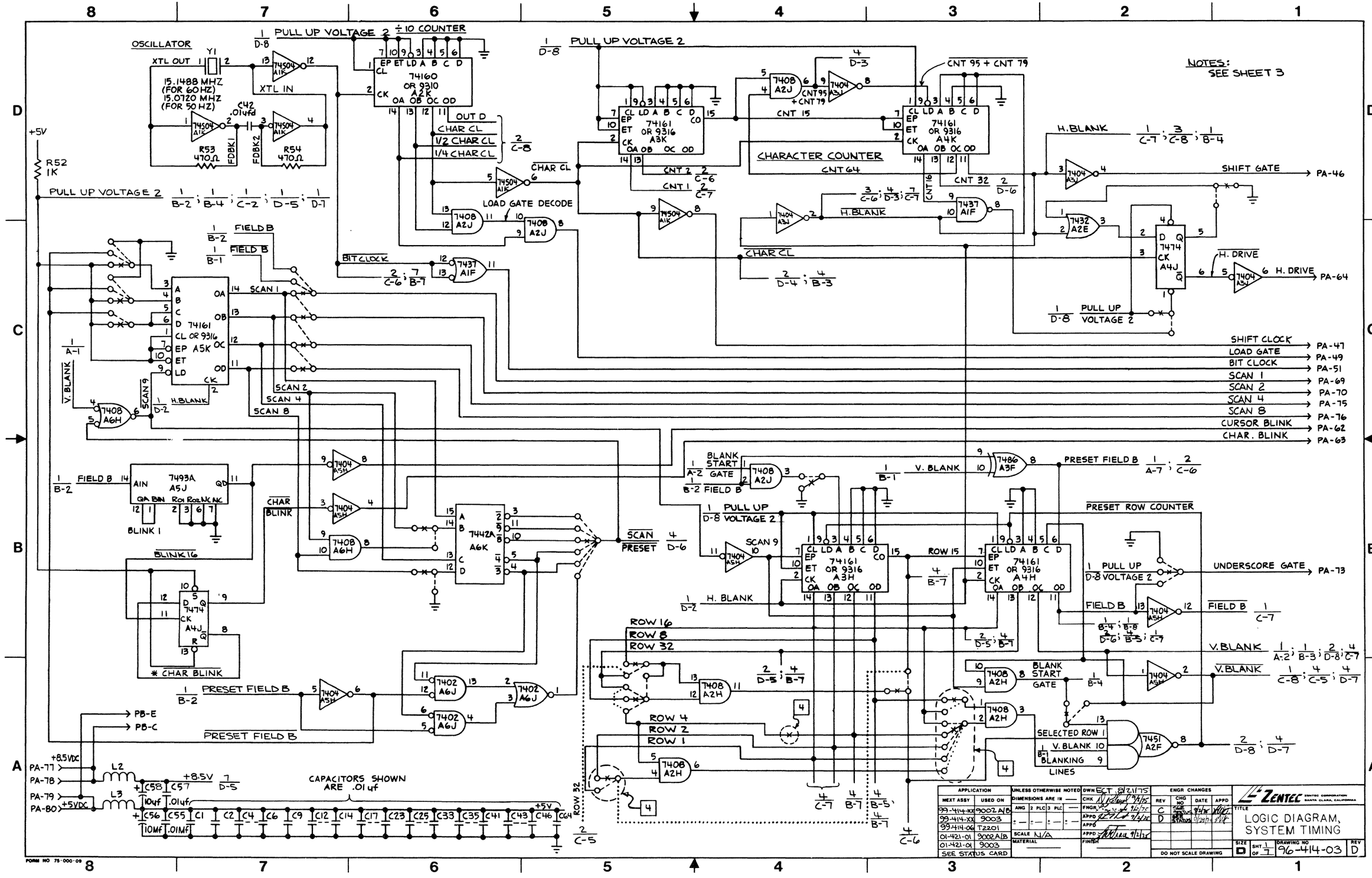
ENGR CHANGES			
REV	CHG NO	DATE	APPD
B	REDRAWN SCHEMATIC	9/12/75	
C	NOT RELEASED		
D	NEW NETWORK	12/4/75	

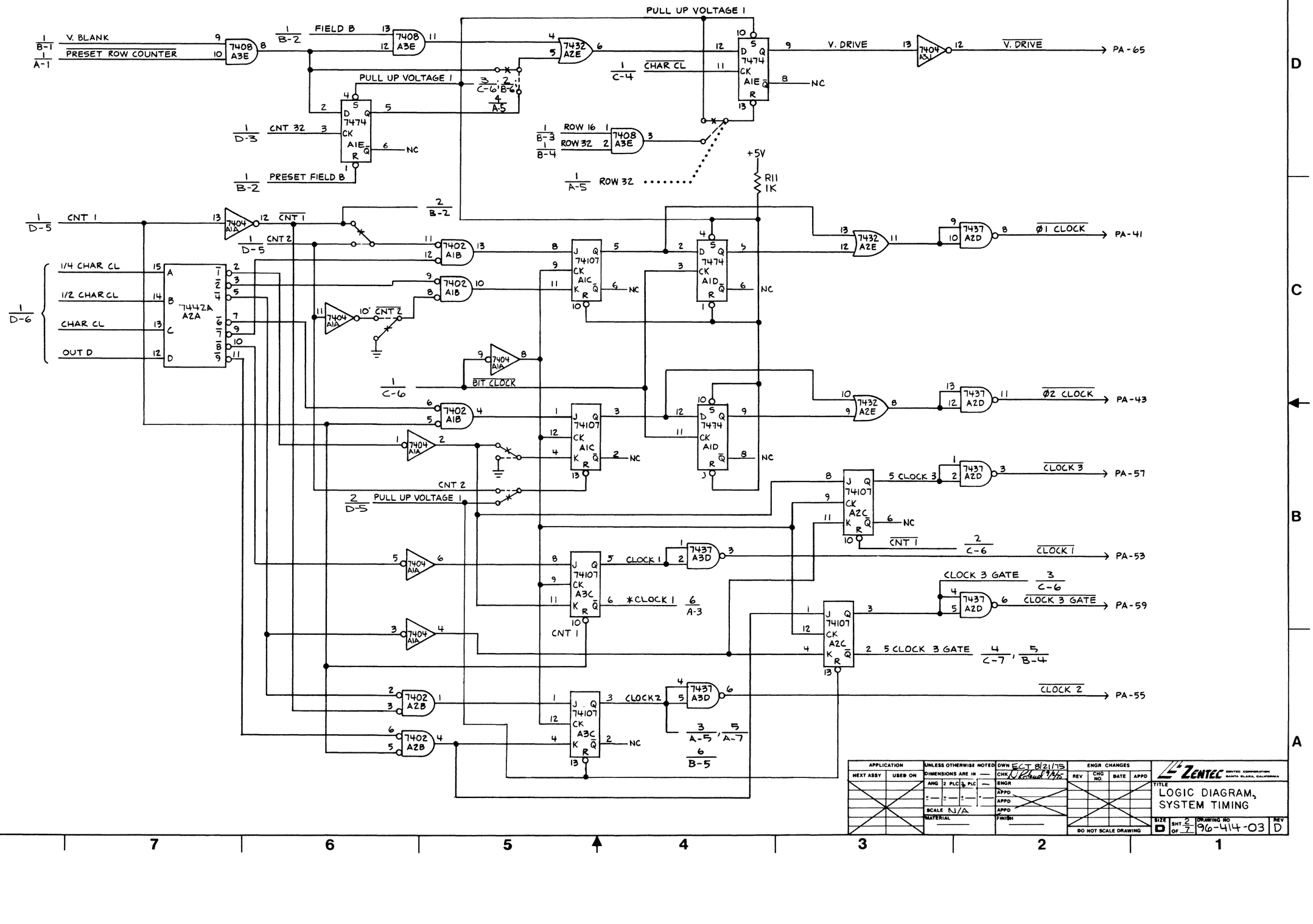
ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA

TITLE SCHEMATIC DIAGRAM, MOTHERBOARD

SIZE D SHT 1 OF 1 | DRAWING NO 96-503-01 | REV D

FORM NO 75-000-09


OSCILLATOR
Y1
XTL OUT
15.1488 MHZ (FOR 60 HZ)
15.0720 MHZ (FOR 50 HZ)
XTL IN
C42 .01uFd
R53 470Ω
R54 470Ω
FDBK1
FDBK2
+5V
R52 1K
PULL UP VOLTAGE 2
÷10 COUNTER
74160 OR 9310 A2K
OUT D
CHAR CL
1/2 CHAR CL
1/4 CHAR CL
LOAD GATE DECODE
BIT CLOCK
74161 OR 9316 A5K
FIELD B
SCAN 1
SCAN 2
SCAN 4
SCAN 8
SCAN 9
V. BLANK
H. BLANK
7493A A5J
BLINK 1
BLINK 16
7442A A6K
* CHAR BLINK
CHAR BLINK
PRESET FIELD B
SCAN PRESET
PB-E
PB-C
+8.5VDC
+5VDC
L2
L3
C58
C57
C56
C55
C1
C2
C4
C6
C9
C12
C14
C17
C23
C25
C33
C35
C41
C43
C46
C64
CAPACITORS SHOWN ARE .01uf
74161 OR 9316 A3K
74161 OR 9316 A4K
CNT 95 + CNT 79
CNT 15
CNT 2
CNT 1
CNT 32
CHARACTER COUNTER
CNT 64
CNT 16
SHIFT GATE
H. DRIVE
PULL UP VOLTAGE 2
SHIFT CLOCK
LOAD GATE
BIT CLOCK
SCAN 1
SCAN 2
SCAN 4
SCAN 8
CURSOR BLINK
CHAR. BLINK
BLANK START GATE
PRESET FIELD B
PRESET ROW COUNTER
ROW 15
ROW 16
ROW 8
ROW 32
ROW 4
ROW 2
ROW 1
ROW 32
UNDERSCORE GATE
SELECTED ROW 1
V. BLANK 10
BLANKING LINES
NOTES:
SEE SHEET 3
ZENTEC
LOGIC DIAGRAM, SYSTEM TIMING
DRAWING NO 96-414-03
REV D
SIZE D
SHT 1 OF 7



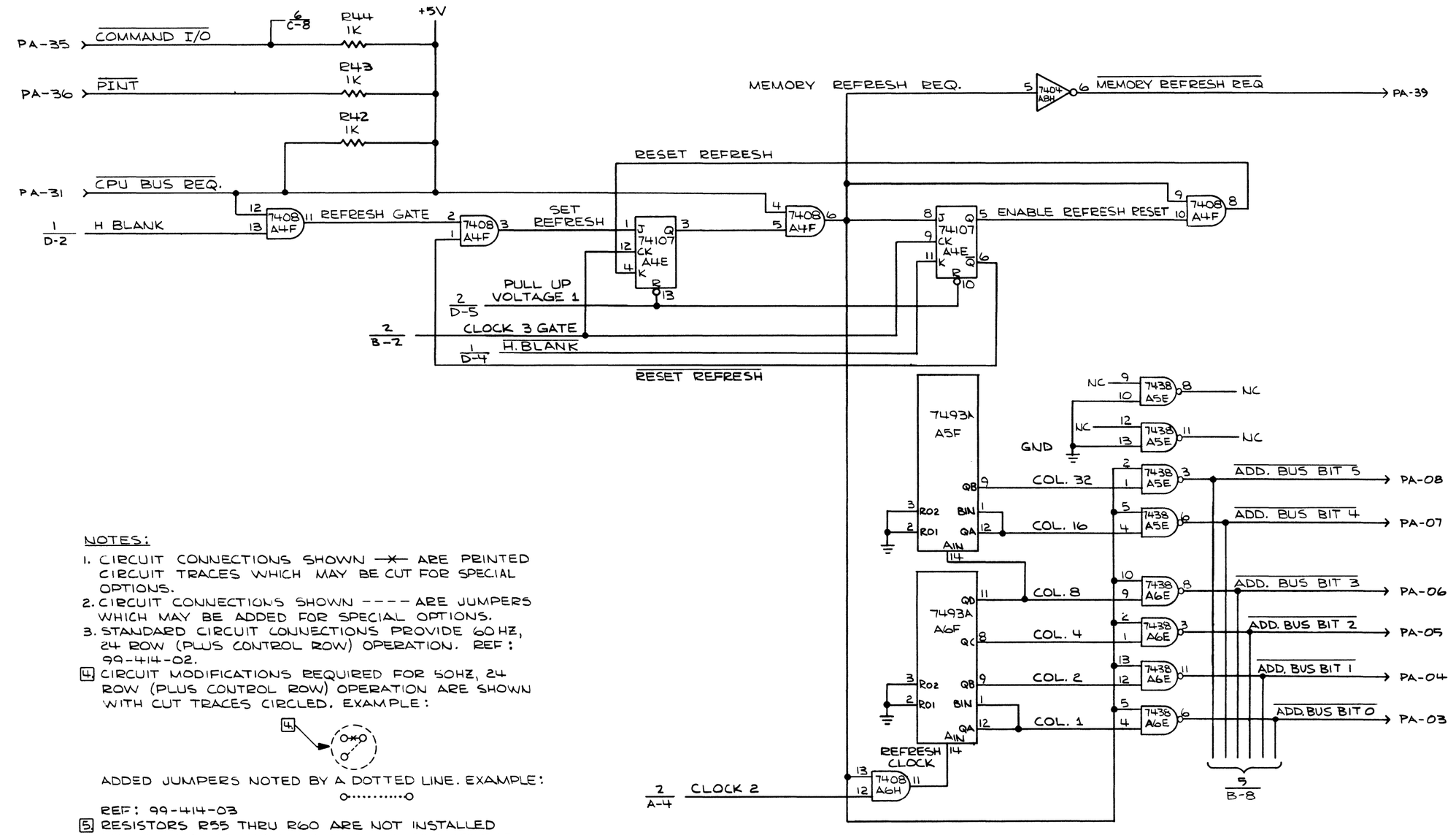
APPLICATION: NEXT ASSY / USED ON	UNLESS OTHERWISE NOTED DIMENSIONS ARE IN — ANG 2 PLC 3 PLC — ± — ± — ± — SCALE N/A MATERIAL	DWN ECT 8/21/75 CHK [illegible] 9/4/75 ENGR APPD APPD APPD FINISH	ENGR CHANGES: REV / CHG NO. / DATE / APPD — DO NOT SCALE DRAWING

ZENTEC — SANTA CLARA, CALIFORNIA

TITLE: LOGIC DIAGRAM, SYSTEM TIMING

SIZE D | SHT 2 OF 7 | DRAWING NO 96-414-03 | REV D

FORM NO 75-000-08



NOTES:

1. CIRCUIT CONNECTIONS SHOWN —×— ARE PRINTED CIRCUIT TRACES WHICH MAY BE CUT FOR SPECIAL OPTIONS.
2. CIRCUIT CONNECTIONS SHOWN - - - - ARE JUMPERS WHICH MAY BE ADDED FOR SPECIAL OPTIONS.
3. STANDARD CIRCUIT CONNECTIONS PROVIDE 60 HZ, 24 ROW (PLUS CONTROL ROW) OPERATION. REF: 99-414-02.
4. CIRCUIT MODIFICATIONS REQUIRED FOR 50HZ, 24 ROW (PLUS CONTROL ROW) OPERATION ARE SHOWN WITH CUT TRACES CIRCLED. EXAMPLE:

ADDED JUMPERS NOTED BY A DOTTED LINE. EXAMPLE:

o.....o

REF: 99-414-03

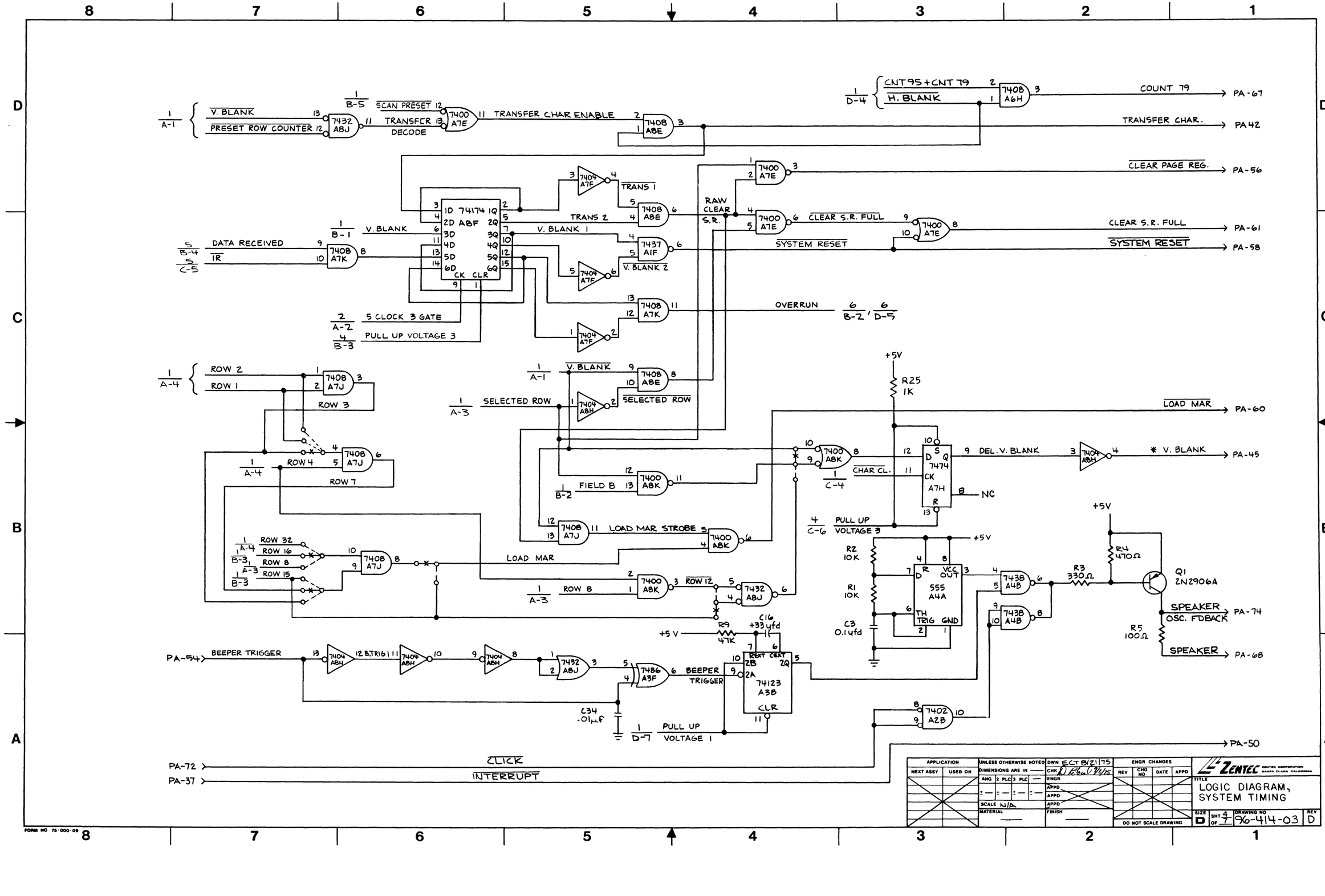
5. RESISTORS R55 THRU R60 ARE NOT INSTALLED FOR STANDARD ASSY; SPECIAL INSTRUCTIONS ARE REQUIRED.
6. THE LAST REFERENCE DESIGNATIONS USED ARE:

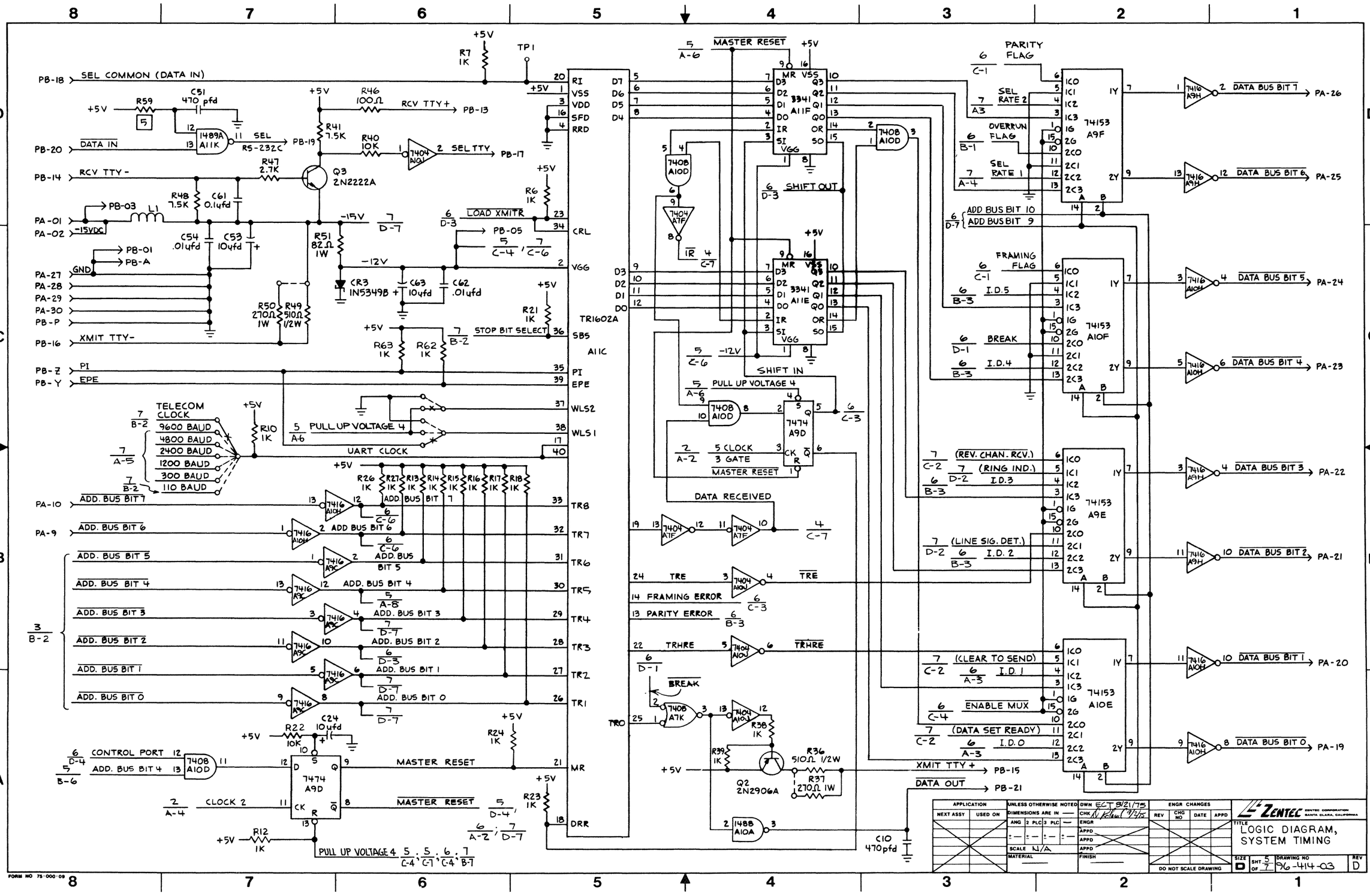
CAPACITORS	C64	CRYSTAL	Y1
DIODES	CR3	INDUCTORS	L3
RESISTORS	R64	TRANSISTORS	Q3

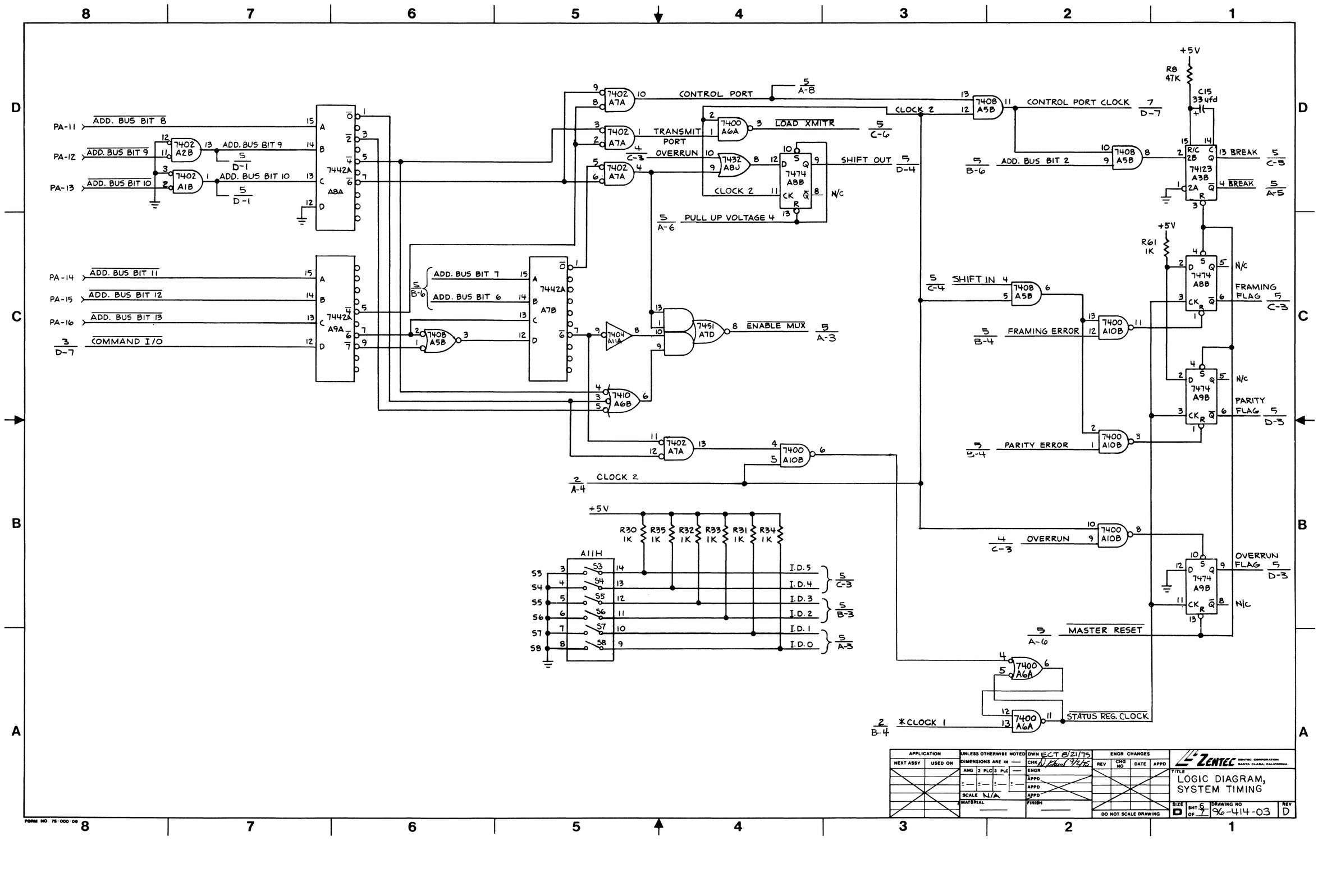
REFERENCE DESIGNATION CR1 IS NOT USED,

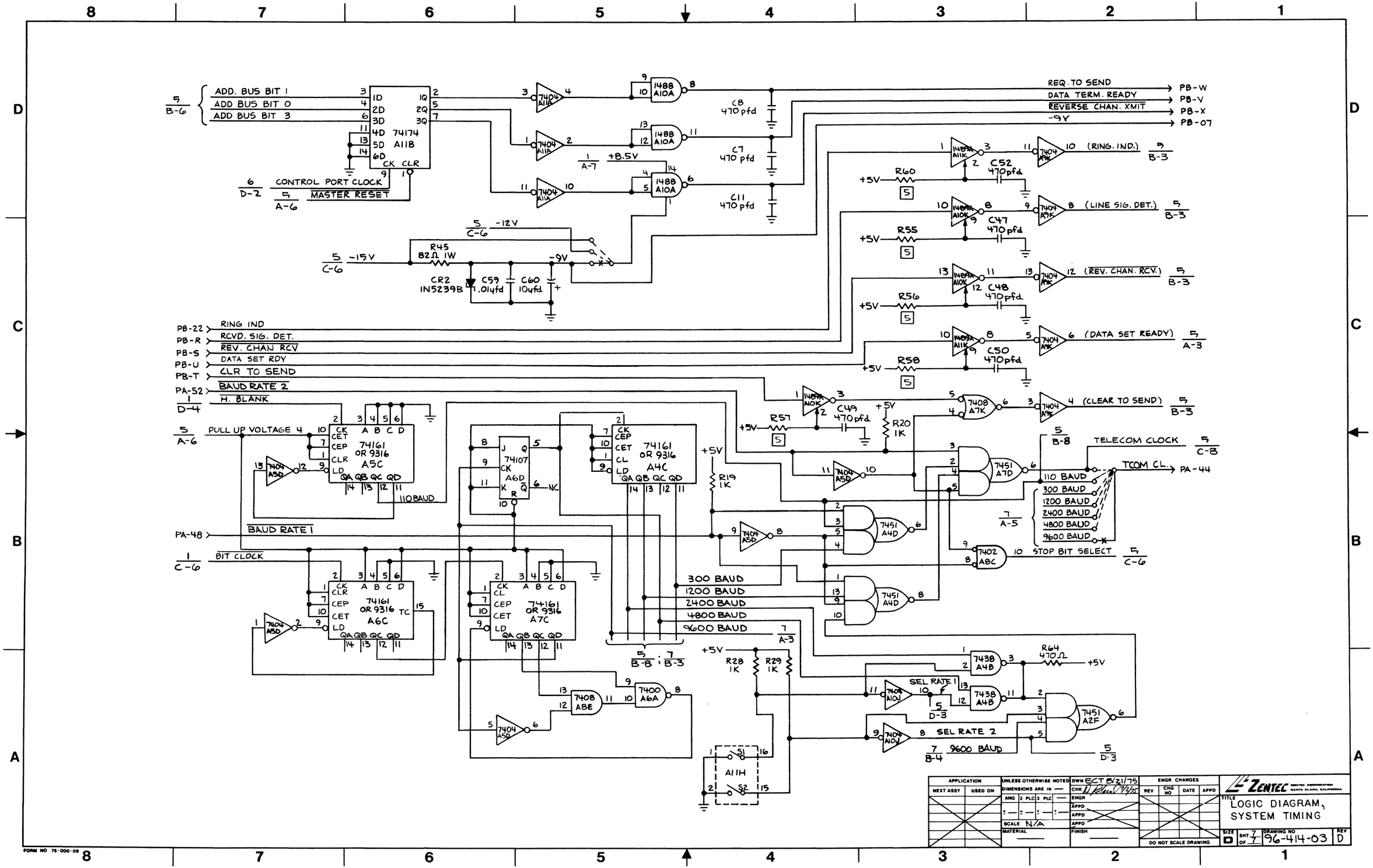
APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN —				DWN ECT 8/21/75	ENGR CHANGES				ZENTEC SYNTEC CORPORATION SANTA CLARA, CALIFORNIA
NEXT ASSY	USED ON	ANG	2 PLC	3 PLC		CHK [signature] 9/4/75	REV	CHG NO	DATE	APPD	TITLE
		± —	± —	± —	• —	ENGR					LOGIC DIAGRAM, SYSTEM TIMING
		SCALE N/A				APPD					
		MATERIAL —				APPD					SIZE D SHT 3 OF 7 DRAWING NO 96-414-03 REV D
						FINISH —	DO NOT SCALE DRAWING				

FORM NO 75-000-05


V. BLANK
PRESET ROW COUNTER 12
7432 A8J
SCAN PRESET 12
TRANSFER DECODE 13
7400 A7E
TRANSFER CHAR ENABLE
7408 A8E
CNT 95 + CNT 79
H. BLANK
7408 A6H
COUNT 79
PA-67
TRANSFER CHAR.
PA 42
CLEAR PAGE REG.
PA-56
7404 A7F
TRANS 1
TRANS 2
V. BLANK 1
7408 A8E
7437 A1F
V. BLANK 2
RAW CLEAR S.R.
7400 A7E
CLEAR S.R. FULL
SYSTEM RESET
PA-61
PA-58
DATA RECEIVED
IR
7408 A7K
74174 A8F
OVERRUN
5 CLOCK 3 GATE
PULL UP VOLTAGE 3
ROW 2
ROW 1
7408 A7J
ROW 3
ROW 4
ROW 7
SELECTED ROW
7404 A8H
LOAD MAR
PA-60
+5V
R25 1K
DEL. V. BLANK
* V. BLANK
PA-45
7474 A7H
CHAR CL.
NC
PULL UP VOLTAGE 3
ROW 32
ROW 16
ROW 8
ROW 15
LOAD MAR STROBE
FIELD B
ROW 12
R2 10K
R1 10K
C3 0.1 µfd
555 A4A
7438 A4B
R3 330Ω
R4 470Ω
Q1 2N2906A
SPEAKER OSC. FDBACK
SPEAKER
PA-74
PA-68
R5 100Ω
C16 +33 µfd
R9 47K
BEEPER TRIGGER
PA-54
7404 A8H
7432 A8J
7486 A3F
BEEPER TRIGGER
74123 A3B
C34 .01µf
PULL UP VOLTAGE 1
7402 A2B
PA-50
CLICK
INTERRUPT
PA-72
PA-37
APPLICATION
NEXT ASSY
USED ON
UNLESS OTHERWISE NOTED
DIMENSIONS ARE IN
SCALE N/A
MATERIAL
DWN ECT 8/21/75
CHK
ENGR
APPD
FINISH
ENGR CHANGES
REV
CHG NO
DATE
APPD
DO NOT SCALE DRAWING
ZENTEC
TITLE
LOGIC DIAGRAM, SYSTEM TIMING
SIZE D
SHT 4 OF 7
DRAWING NO 96-414-03
REV D
FORM NO 75-000-08


PB-18 SEL COMMON (DATA IN)
PB-20 DATA IN
PB-14 RCV TTY-
PA-01 -15VDC
PA-02
PB-03
L1
PB-01
PB-A
GND
PA-27
PA-28
PA-29
PA-30
PB-P
PB-16 XMIT TTY-
PB-Z PI
PB-Y EPE
+5V
R59 5
C51 470 pfd
1489A A11K
SEL RS-232C
PB-19
R46 100Ω
RCV TTY+ PB-13
R41 7.5K
R40 10K
7404 A01
SEL TTY PB-17
R47 2.7K
Q3 2N2222A
R48 7.5K
C61 0.1ufd
C54 .01ufd
C53 10ufd
R51 82Ω 1W
-15V
-12V
CR3 IN5349B
C63 10ufd
C62 .01ufd
R50 270Ω 1W
R49 510Ω 1/2W
R6 1K
R21 1K
LOAD XMITR
PB-05
STOP BIT SELECT
R63 1K
R62 1K
TP1
R7 1K
TRI602A A11C
RI VSS VDD RRD SFD CRL VGG SBS PI EPE WLS2 WLS1 TR8 TR7 TR6 TR5 TR4 TR3 TR2 TR1 DRR MR
D7 D6 D5 D4 D3 D2 D1 D0
TELECOM CLOCK
9600 BAUD
4800 BAUD
2400 BAUD
1200 BAUD
300 BAUD
110 BAUD
R10 1K
PULL UP VOLTAGE 4
UART CLOCK
R26 1K
R27 1K
R13 1K
R14 1K
R15 1K
R16 1K
R17 1K
R18 1K
ADD. BUS BIT 7
ADD. BUS BIT 6
ADD. BUS BIT 5
ADD. BUS BIT 4
ADD. BUS BIT 3
ADD. BUS BIT 2
ADD. BUS BIT 1
ADD. BUS BIT 0
7416 A10H
7416 A9C
R22 10K
C24 10ufd
CONTROL PORT
7408 A10D
7474 A9D
CLOCK 2
MASTER RESET
R12 1K
PULL UP VOLTAGE 4
R24 1K
R23 1K
MASTER RESET
3341 A11F
3341 A11E
7408 A10D
7404 A1F
SHIFT OUT
SHIFT IN
PULL UP VOLTAGE 4
7474 A9D
5 CLOCK
3 GATE
MASTER RESET
DATA RECEIVED
7404 A1F
TRE
FRAMING ERROR
PARITY ERROR
TRHRE
BREAK
7408 A7K
7404 A10J
R38 1K
R39 1K
Q2 2N2906A
R36 510Ω 1/2W
R37 270Ω 1W
1488 A10A
C10 470pfd
XMIT TTY + PB-15
DATA OUT PB-21
PARITY FLAG
SEL RATE 2
OVERRUN FLAG
SEL RATE 1
ADD BUS BIT 10
ADD BUS BIT 9
FRAMING FLAG
I.D.5
BREAK
I.D.4
(REV. CHAN. RCV.)
(RING IND.)
I.D.3
(LINE SIG. DET.)
I.D. 2
(CLEAR TO SEND)
I.D. 1
ENABLE MUX
(DATA SET READY)
I.D.0
74153 A9F
74153 A9E
74153 A10E
74153 A10F
7416 A9H
7416 A10H
DATA BUS BIT 7 PA-26
DATA BUS BIT 6 PA-25
DATA BUS BIT 5 PA-24
DATA BUS BIT 4 PA-23
DATA BUS BIT 3 PA-22
DATA BUS BIT 2 PA-21
DATA BUS BIT 1 PA-20
DATA BUS BIT 0 PA-19
APPLICATION
NEXT ASSY USED ON
UNLESS OTHERWISE NOTED
DIMENSIONS ARE IN —
ANG 2 PLC 3 PLC —
SCALE N/A
MATERIAL
FINISH
DWN ECT 8/21/75
CHK N. Pollard 9/4/75
ENGR
APPD
ENGR CHANGES
REV CHG NO DATE APPD
DO NOT SCALE DRAWING
ZENTEC ZENITH CORPORATION SANTA CLARA, CALIFORNIA
TITLE LOGIC DIAGRAM, SYSTEM TIMING
SIZE D SHT 5 OF 7 DRAWING NO 96-414-03 REV D
FORM NO 75-000-09


PA-11
ADD. BUS BIT 8
PA-12
ADD. BUS BIT 9
PA-13
ADD. BUS BIT 10
7402 A2B
7402 A1B
ADD. BUS BIT 9
ADD. BUS BIT 10
5 D-1
5 D-1
7442A A8A
PA-14
ADD. BUS BIT 11
PA-15
ADD. BUS BIT 12
PA-16
ADD. BUS BIT 13
3 D-7
COMMAND I/O
7442A A9A
ADD. BUS BIT 7
ADD. BUS BIT 6
5 B-6
7442A A7B
7408 A5B
7402 A7A
CONTROL PORT
5 A-8
7402 A7A
TRANSMIT PORT
7400 A6A
LOAD XMITR
5 C-6
4 C-3
OVERRUN
7432 A8U
7474 A8B
SHIFT OUT
5 D-4
CLOCK 2
N/C
5 A-6
PULL UP VOLTAGE 4
7402 A7A
7451 A7D
ENABLE MUX
5 A-3
7404 A11A
7410 A6B
7402 A7A
7400 A10B
2 A-4
CLOCK 2
+5V
R30 1K
R35 1K
R32 1K
R33 1K
R31 1K
R34 1K
A11H
S3
S4
S5
S6
S7
S8
I.D.5
I.D.4
I.D.3
I.D.2
I.D.1
I.D.0
5 C-3
5 B-3
5 A-3
7408 A5B
CLOCK 2
CONTROL PORT CLOCK
7 D-7
5 B-6
ADD. BUS BIT 2
7408 A5B
+5V
C15 33 4fd
74123 A3B
13 BREAK
5 C-3
4 BREAK
5 A-5
R61 1K
7474 A8B
N/C
5 C-4
SHIFT IN 4
7408 A5B
FRAMING FLAG
5 C-3
5 B-4
FRAMING ERROR
7400 A10B
7474 A9B
N/C
PARITY FLAG
5 D-3
5 D-4
PARITY ERROR
7400 A10B
4 C-3
OVERRUN
7400 A10B
7474 A9B
OVERRUN FLAG
5 D-3
N/C
5 A-6
MASTER RESET
7400 A6A
7400 A6A
2 B-4
*CLOCK 1
STATUS REG. CLOCK
APPLICATION
NEXT ASSY
USED ON
UNLESS OTHERWISE NOTED
DIMENSIONS ARE IN —
ANG 2 PLC 3 PLC
SCALE N/A
MATERIAL
DWN ECT 8/21/75
CHK
ENGR
APPD
APPD
APPD
FINISH
ENGR CHANGES
REV
CHG NO
DATE
APPD
DO NOT SCALE DRAWING
ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA
TITLE
LOGIC DIAGRAM, SYSTEM TIMING
SIZE D
SHT 6 OF 7
DRAWING NO 96-414-03
REV D
FORM NO 75-000-09



APPLICATION: NEXT ASSY / USED ON	UNLESS OTHERWISE NOTED DIMENSIONS ARE IN — ANG 2 PLC 3 PLC	DWN ECT 8/21/75 CHK	ENGR CHANGES: REV / CHG NO / DATE / APPD
	SCALE N/A	APPD / APPD / APPD	DO NOT SCALE DRAWING
	MATERIAL	FINISH	

ZENTEC CORPORATION, SANTA CLARA, CALIFORNIA

TITLE: LOGIC DIAGRAM, SYSTEM TIMING

SIZE D | SHT 7 OF 7 | DRAWING NO 96-414-03 | REV D

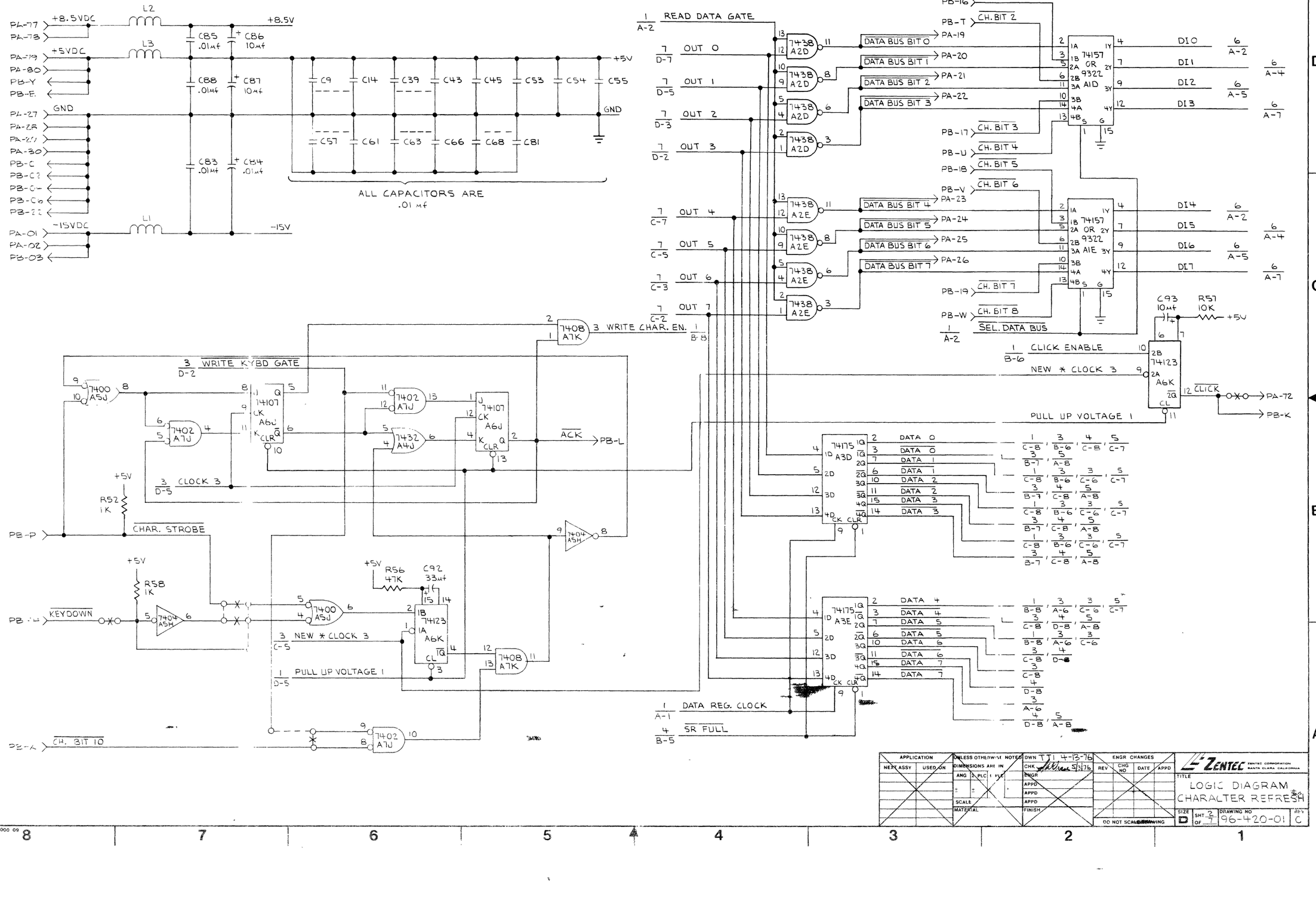
FORM NO 75-000-09

NOTES:
1. LAST REF. DESIG. USED: C93, CR4, L3, Q10, R70
2. CIRCUITS SHOWN —✱— ARE PRINTED CIRCUIT TRACES WHICH MAY BE CUT FOR SPECIFIC OPTIONS. CIRCUITS SHOWN — — — — — — ARE JUMPERS WHICH MAY BE ADDED FOR SPECIFIC OPTIONS.
3. REF. DESIG. C44 & C62 ARE NOT USED.

3 D-1 STATE 9
3 C-5 ✱CLOCK 3
+5V
R51 1K
PULL UP VOLTAGE 1
2 A-6, 3 C-8
3 D-2 WRITE KYBD GATE
3 C-1 CHARACTER REFRESH
DATA 0
DATA 1
2 B-2
7432 A4J
DATA 00
3 B-6
7483A A4H
74163 A3J
7400 A5J
7402 A2J
PA-03 ADD. BUS BIT 0
PA-04 ADD. BUS BIT 1
PA-05 ADD. BUS BIT 2
PA-06 ADD. BUS BIT 3
74157 OR9322 A1J
MEM. ADD. 0
MEM. ADD. 1
MEM. ADD. 2
MEM. ADD. 3
6 D-8
PA-07 ADD. BUS BIT 4
PA-08 ADD. BUS BIT 5
PA-09 ADD. BUS BIT 6
PA-10 ADD. BUS BIT 7
A3H
A1H
7404 A2H
MEM. ADD. 4
MEM. ADD. 5
MEM. ADD. 6
MEM. ADD. 7
6 C-8
PA-F,8 SYSTEM RESET
3 B-7
DATA 2
DATA 3
2 B-2
DATA 4
DATA 5
2 B-2
2 A-2
A4F
A3F
7404 A2F
PA-11 ADD. BUS BIT 8
PA-12 ADD. BUS BIT 9
PA-13 ADD. BUS BIT 10
A1F
MEM. ADD. 8
MEM. ADD. 9
MEM. ADD. 10
CHIP SELECT 2
6 B-8
PA-60 LOAD MAR
3 D-1 PAGE REG. GATE
4 B-5 CLEAR SR FULL
3 A-1 ROW 24
7408 A4K
7432 A4J
CHARACTER REFRESH
3 D-2 WRITE KYBD GATE
2 C-4 WRT. CHAR. EN.
CLICK ENABLE
2 C-2
A4K
CHIP SELECT 1
6 C-8
CARD SELECT
3 D-7
WRITE ENABLE
6 C-8
DATA REG. CLOCK
2 A-4
PA-14 ADD. BUS BIT 11
PA-15 ADD. BUS BIT 12
PA-16 ADD. BUS BIT 13
7442A A2K
ADD DECODE 1
ADD DECODE 2
R55 1K
R54 1K
+5V
A3K
A1K
3 D-5 CLOCK 3
SEL. DATA BUS
2 C-3
READ DATA GATE
2 D-4
PA-17 ADD BUS BIT 14
PA-18 ADD BUS BIT 15
7410 A5K
PB-B WRT. SENSE SW.
R53 1K
PA-33 WRITE DATA
PA-34 READ DATA
PA-39 MEMORY REFRESH REQ.
3 D-7

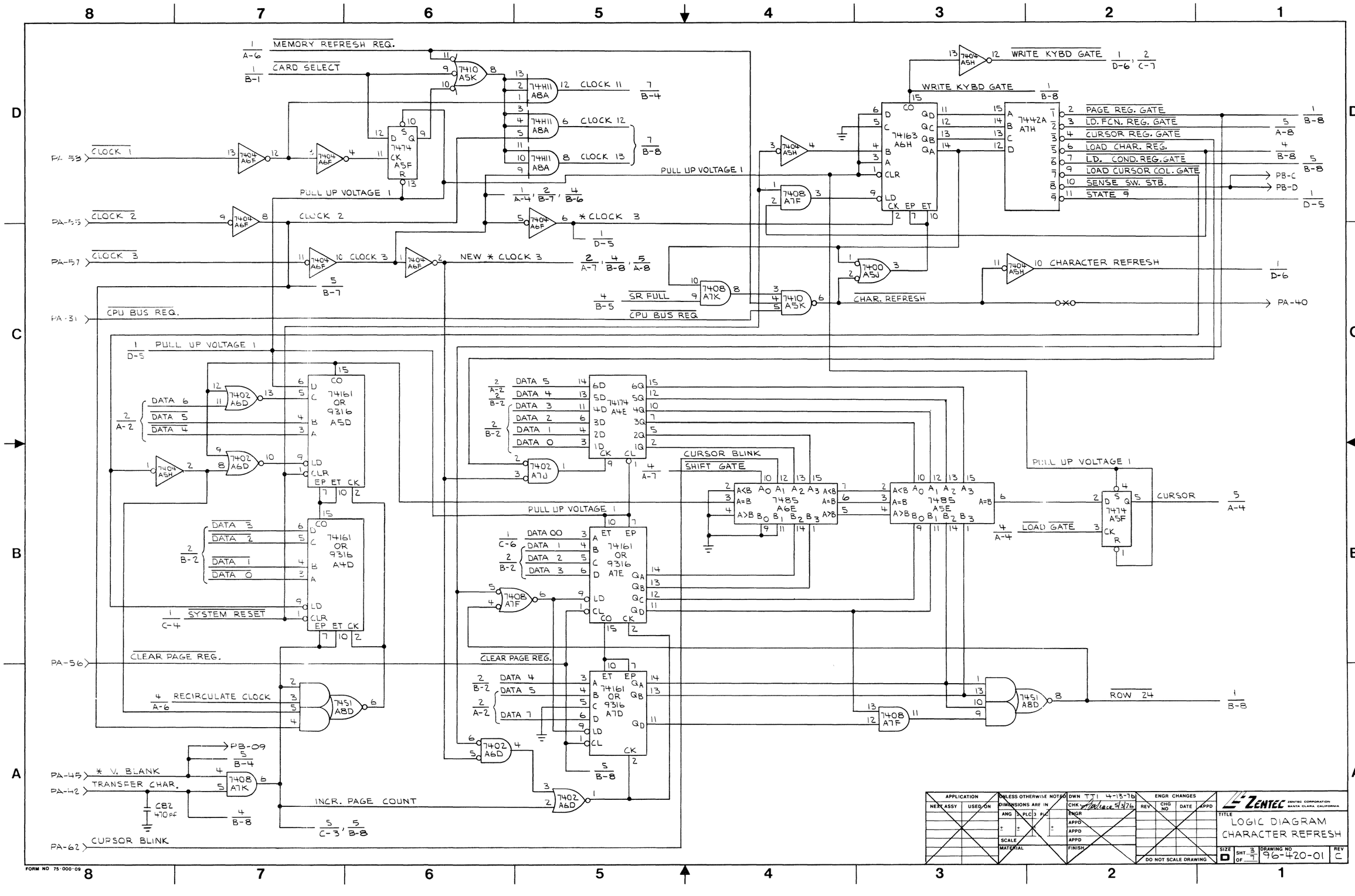
APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN				DWN TTI 4-13-76	ENGR CHANGES				ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA
NEXT ASSY	USED ON	ANG	2 PLC	3 PLC		CHK 5/3/76	REV	CHG NO	DATE	APPD	TITLE
99-420-XX	TZ201	±	±	±	±	ENGR 5/4/76	C	REDRAW EAR-5064	5/6/76	✱	LOGIC DIAGRAM CHARACTER REFRESH
↓	9002A/B	SCALE				APPR 5/4/76					
	9003	MATERIAL				APPD 5/4/76					
						APPR 5/6/76					
						FINISH	DO NOT SCALE DRAWING				SIZE D SHT 1 OF 7 DRAWING NO 96-420-01 REV C

FORM NO 75-000-09



APPLICATION		UNLESS OTHERWISE NOTED		DWN TTI 4-13-76	ENGR CHANGES			ZENTEC ZENTEC CORPORATION SANTA CLARA CALIFORNIA
NEXT ASSY	USED ON	DIMENSIONS ARE IN		CHK	REV	CHG NO	DATE	APPD
		ANG ±	2 PLC ±	ENGR				TITLE
		SCALE		APPD				LOGIC DIAGRAM CHARACTER REFRESH
		MATERIAL		APPD				
				FINISH	DO NOT SCALE DRAWING			SIZE D SHT 2 OF 7 DRAWING NO 96-420-01 REV C

FORM NO 75-000 09



APPLICATION	
NEXT ASSY	USED ON
UNLESS OTHERWISE NOTED DIMENSIONS ARE IN	
ANG ±	X PLC ± 3 PL ±
SCALE	
MATERIAL	
DWN TTI 4-13-76	
CHK Wallace 5/3/76	
ENGR	
APPD	
APPD	
APPD	
FINISH	
DO NOT SCALE DRAWING	
ENGR CHANGES: REV / CHG NO / DATE / APPD	
ZENTEC ZENTEC CORPORATION SANTA CLARA CALIFORNIA	
TITLE: LOGIC DIAGRAM CHARACTER REFRESH	
SIZE D	SHT 3 OF 7
DRAWING NO 96-420-01	REV C

FORM NO 75-000-09

CR4 IN5225B
-15V
-12V
R68 47K
C89 .01uf
C90 10 uf
PB-21
PB-05
5 C-3 BLANK CHARACTERS
5 B-7 FCN LITE 4
5 C-1 BLANK CHAR. GEN.
SR2 OUT 7
PULL UP VOLTAGE 3 4 A-5
SR.2 OUT 5
5 B-7
SR.2 OUT 4
5 D-8
SR.2 OUT 7 5 D-4
C67 .01uf
DATA 7
DATA 6
DATA 5
DATA 4
2 A-2
DATA 3
DATA 2
DATA 1
2 B-2
DATA 0
PA-67 COUNT 79
3 A-7
CLEAR SR FULL
PA-61
TRANSFER CHAR.
SR. 2 OUT 3
SR. 2 OUT 2
SR. 2 OUT 1
SR. 2 OUT 0
5 B-7
CONTROL DECODE 5 B-8
PA-75 SCAN 4
PA-70 SCAN 2
PA-69 SCAN 1
PULL UP VOLTAGE 2
1K (TYP 8 PLCS)
R62
R64
R66
R67
R65
R63
R61
R60
+5V
RAW VIDEO 5 A-6
Q11
74166 A9J
R59 1K
LD CK INH
CLEAR SR FULL 1 B-8
CLOCK 3 D-5
SR FULL 2 A-4, C-5
3 C-5 NEW * CLOCK 3
3 D-1 LOAD CHAR. REG.
SHIFT CL.
PB-H
RECIRCULATE CLOCK 3 A-8
5 B-6
LOAD GATE
PA-49 LOAD GATE
SHIFT GATE 3 B-5, 5 C-6
PA-46 SHIFT GATE
5 C-6
PA-47 SHIFT CL.
5 B-7
PA-51 BIT CLOCK
5 A-6
LOAD GATE 3 B-3, 5 C-3
BIT CLOCK
R69 330
R70 390
R14 1K
PULL UP VOLTAGE 3
4 D-3, 5 A-8
PA-76 SCAN 8
7404 A10F
7486 A10E
7408 A11E
7402 A11F
7408 A10E
7404 A10H
7485 A11H
7414 A4E
7408 A11E
7432 A8J
7407 A3K
74107 A8K
7402 A11F
74128 A10D
7414 A9F
7414 A9E
7408 A7F
74107 A8E
7432 A8J
7486 A10E
7400 A9D
A6280 A10K
A6280 A11K
3347 A8F
3347 A8H
3347 A9F
3347 A9H

APPLICATION		UNLESS OTHERWISE NOTED DIMENSIONS ARE IN		DWN TTI 4-13-76	ENGR CHANGES				ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA
NEXT ASSY	USED ON	ANG ±	X PLC 3 PL ±	CHK	REV	CHG NO	DATE	APPD	TITLE
		SCALE		ENGR					LOGIC DIAGRAM CHARACTER REFRESH
		MATERIAL		APPD					
				APPD					
				APPD					
				FINISH					
DO NOT SCALE DRAWING									SIZE D SHT 4 OF 7 DRAWING NO 96-420-01 REV C

FORM NO 75-000-09

PULL UP VOLTAGE 3

4 / C-5 SR. 2 OUT 4

7404 A10A

7451 A10B

7474 A9B

2 / B-2 DATA 4

4 / A-8 SHIFT GATE

4 / A-7 SHIFT GATE

7451 A8B

7474 A9B

CONTROL DECODE

4 / C-3 SR. 2 OUT 7

7402 A11F

7408 A11E

7474 A9A

7400 A9D

3 / A-7 INCR. PAGE COUNT

4 / A-4 LOAD GATE

BLANK CHARACTERS 4 / D-6, 5 / A-6

+5V

R9 1K

PA-73 UNDERSCORE GATE

2 / B-2 DATA 3, DATA 2, DATA 1, DATA 0

74298 A10C

74298 A9C

PA-63 CHAR. BLINK

7408 A11C

7432 A11D

BLANK CHAR. GEN. 4 / D-3

CONTROL DECODE

4 / B-4 SR. 2 OUT 3, SR. 2 OUT 2, SR. 2 OUT 1, SR. 2 OUT 0

4 / C-3 SR. 2 OUT 5

PA-65 V. DRIVE → PB-F

PA-64 H. DRIVE → PB-A

PB-15 RESET → PA-74

3 / D-1 LD. COND. REG. GATE

3 / A-5 CLEAR PAGE REG.

3 / C-7, 4 / A-6 CLOCK 2

SHIFT CL

4 / B-3, 3 / A-7 CONTROL DECODE

INCR. PAGE COUNT

7400 A9D

7451 A10B

7404 A10A

7451 A8B

7408 A11B

SHIFT CL

CONTROL DECODE

R45 180Ω PB-13 → PA-44

R46 180Ω PB-R → PA-48

R47 180Ω PB-S → PA-50

R48 180Ω PB-Z → PA-52

HALF BRIGHT

UNDERSCORE

UNDERSCORE

H. BLANK → PB-J

3 / A-7 *V. BLANK

7400 A9D

COMP. BL. → PB-08

PULL UP VOLTAGE 3

4 / D-6

74174 A8C

DATA 0, DATA 1, DATA 2, DATA 3, DATA 4, DATA 7

FCN LITE NO. 1

FCN LITE NO. 2

FCN LITE NO. 3

FCN LITE NO. 4

FORM ENABLE

BEEPER TRIGGER → PA-54, PB-07

4 / A-6 SHIFT CL

+5V

R50 1K

PA-66 FORMS

7432 A11D

7408 A11C

7408 A11C

7486 A10E

7486 A10E

74128 A10D

4 VIDEO → PA-71, PB-10

HALF BRIGHT

4 / A-4 BIT CLOCK

7408 A11C

C56 15pf

R49 1K

CR3 1N914B

7432 A11D

3 / B-1 CURSOR

4 / B-1 RAW VIDEO

5 / C-3 BLANK CHARACTERS

7432 A11D

3 / C-5, 3 / D-1 NEW * CLOCK 3

LD. FCN REG. GATE

74128 A10D

4 / A-5 PULL UP VOLTAGE 3

APPLICATION		DRWN T.T. 4-13-76
NEXT ASSY	USED ON	CHK Ted Lee 5/3/76
UNLESS OTHERWISE NOTED DIMENSIONS ARE IN		ENGR
ANG ±	2 PLC ± 3 PLC ±	APPD
SCALE		APPD
MATERIAL		APPD
		FINISH

ENGR CHANGES			
REV	CHG NO	DATE	APPD

DO NOT SCALE DRAWING

ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA

TITLE: LOGIC DIAGRAM CHARACTER REFRESH

SIZE D | SHT 5 OF 7 | DRAWING NO 96-420-01 | REV C

FORM NO 75-000-09

NOTE: ALL MEM CHIP VOLTAGES WILL TIE WITH CORRECT VOLTAGE ON PAGE 7 ZONE A-4 THRU A-7.
ALL MEMORY CHIPS ARE MM5262 OR 600314.

CHIP PIN DESIGNATIONS TYPICAL, 16 PLCS

+5V R2 470Ω

MEM.ADD.0
MEM.ADD.1
MEM.ADD.2
MEM.ADD.3
MEM.ADD.4
M CLOCK 2
M CLOCK 3
M CLOCK 1

CHIP SELECT 1
WRITE ENABLE

MEM.ADD.5
MEM.ADD.6
MEM.ADD.7
MEM.ADD.8
MEM.ADD.9
MEM.ADD.10

CHIP SELECT 2

A3W A2W A1W A0W
A7W A6W A5W A4W
A3X A2X A1X A0X
A7X A6X A5X A4X

+5V +8.5V -15V

R12 470Ω R15 470Ω R10 470Ω
R11 470Ω R8 470Ω R16 470Ω
R3 470Ω R17 470Ω R20 470Ω
R13 470Ω R18 470Ω
R19 470Ω R7 470Ω
R14 470Ω R21 470Ω

DOM 17 DOM 13
DOM 16 DOM 12
DOM 15 DOM 11
DOM 14 DOM 10
DIO DI4
DI3 DI7
DI2 DI6
DI1 DI5

R44 470Ω R39 470Ω
R38 470Ω R33 470Ω
R32 470Ω R27 470Ω

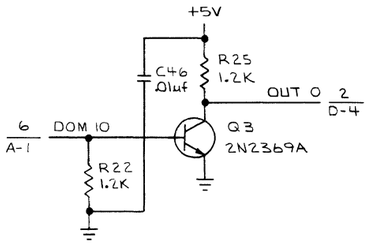
APPLICATION		DRWN TJ 4-13-76	ENGR CHANGES
NEXT ASSY	USED ON	CHK [illegible] 5/3/76	REV / CHG NO / DATE / APPD
UNLESS OTHERWISE NOTED DIMENSIONS ARE IN		ENGR	
ANG ±	X PLC ±	APPD	
SCALE		APPD	
MATERIAL		APPD	
		FINISH	
DO NOT SCALE DRAWING			

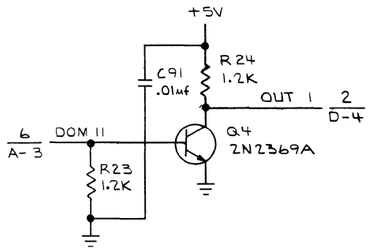
ZENITH RADIO CORPORATION SANTA CLARA, CALIFORNIA

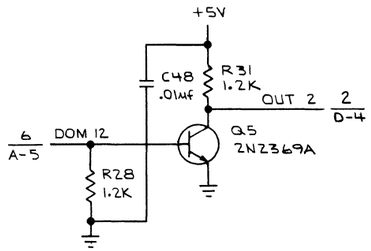
TITLE: LOGIC DIAGRAM CHARACTER REFRESH

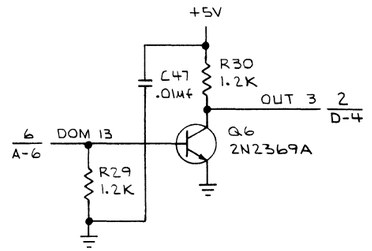
SIZE D | SHT 6 OF 7 | DRAWING NO 95-4C-01 | REV C

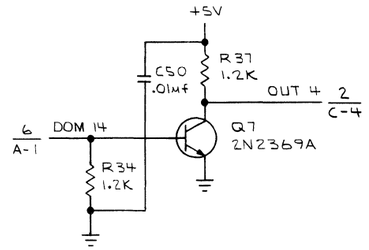
FORM NO 75 000-09

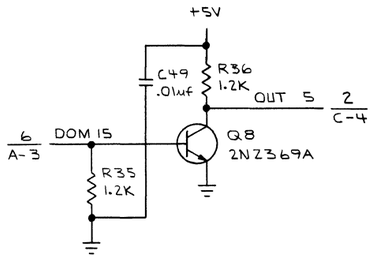


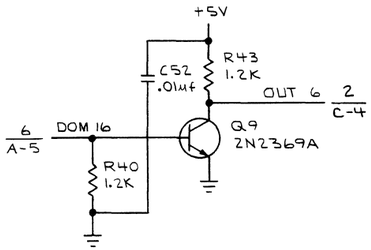


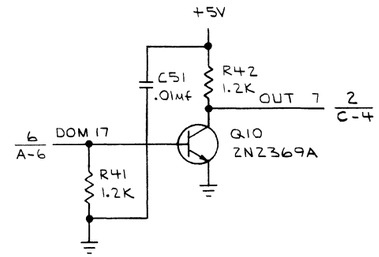


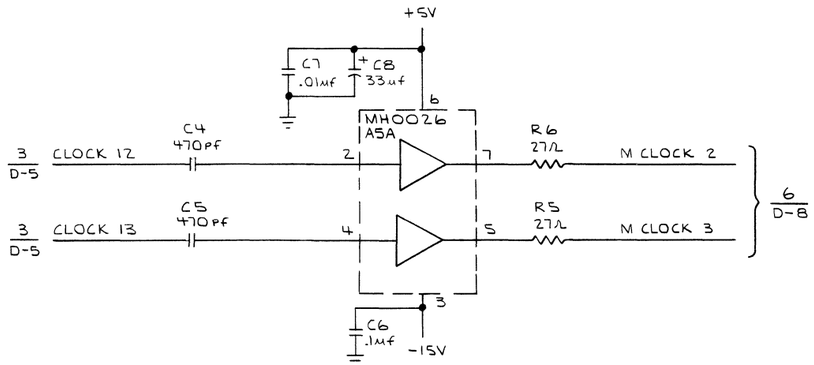


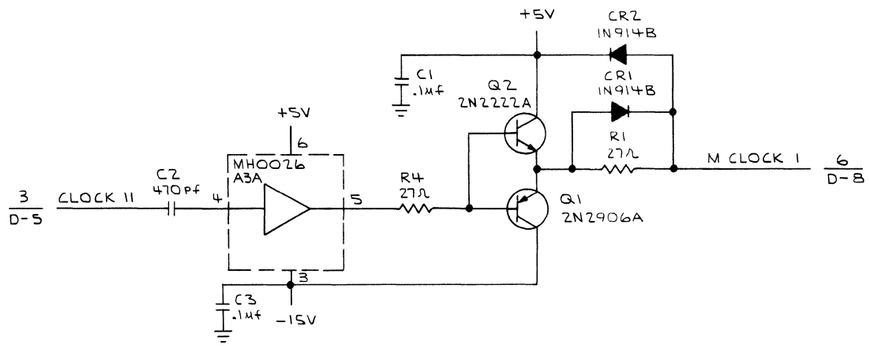


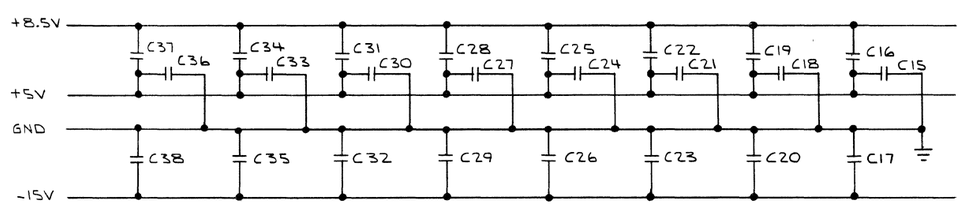










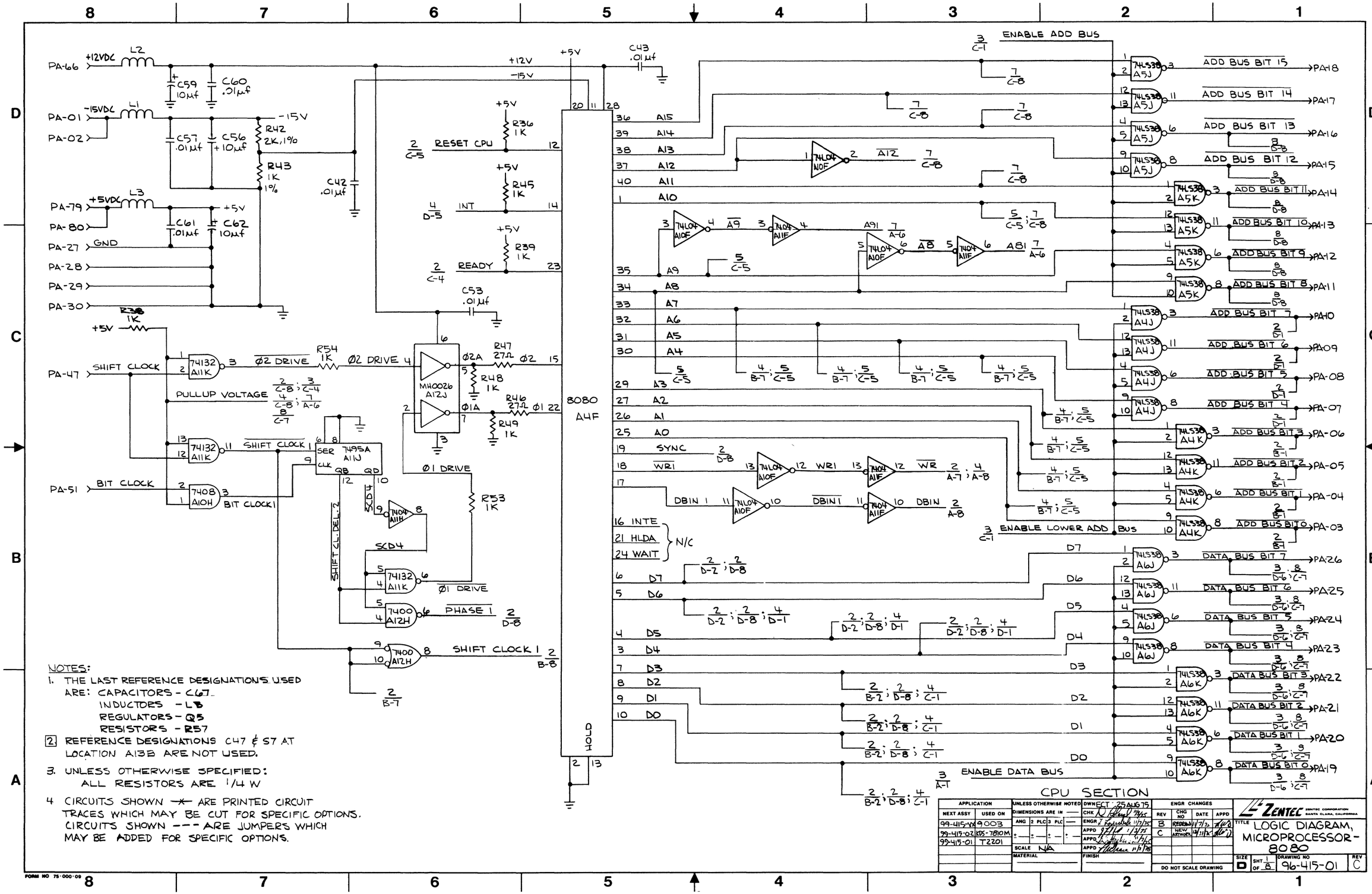


SEE NOTE 6 D-2

CAPACITORS C15 – C38 ARE .01mf

APPLICATION		UNLESS OTHERWISE NOTED		DWN TFI 4-13-76	ENGR CHANGES		ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA
NEXT ASSY	USED ON	DIMENSIONS ARE IN		CHK Williams 5/3/76	REV	CHG NO / DATE / APPD	TITLE
		ANG ±	2 PLC ±	ENGR			LOGIC DIAGRAM
		3 PLC ±		APPD			CHARACTOR REFRESH
		SCALE		APPD			
		MATERIAL		FINISH	DO NOT SCALE DRAWING		SIZE D / SHT 7 OF 7 / DRAWING NO 96-420-01 / REV C

FORM NO 75-000-09



NOTES:

1. THE LAST REFERENCE DESIGNATIONS USED ARE: CAPACITORS - C67
   INDUCTORS - L3
   REGULATORS - Q5
   RESISTORS - R57
2. REFERENCE DESIGNATIONS C47 & S7 AT LOCATION A13B ARE NOT USED.
3. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE 1/4 W
4. CIRCUITS SHOWN —×— ARE PRINTED CIRCUIT TRACES WHICH MAY BE CUT FOR SPECIFIC OPTIONS. CIRCUITS SHOWN - - - ARE JUMPERS WHICH MAY BE ADDED FOR SPECIFIC OPTIONS.

CPU SECTION

APPLICATION	
NEXT ASSY	USED ON
99-415-XX	9003
99-415-02	105-7810M
99-415-01	T2201

UNLESS OTHERWISE NOTED
DIMENSIONS ARE IN
ANG ± | 2 PLC ± | 3 PLC ±
SCALE N/A
MATERIAL

DWN ECT 25 AUG 75
CHK
ENGR
APPD
APPD
APPD
FINISH

ENGR CHANGES

REV	CHG NO	DATE	APPD
B	REDRAW	11/7/75	
C	NEW ARTWORK	12/31/75	

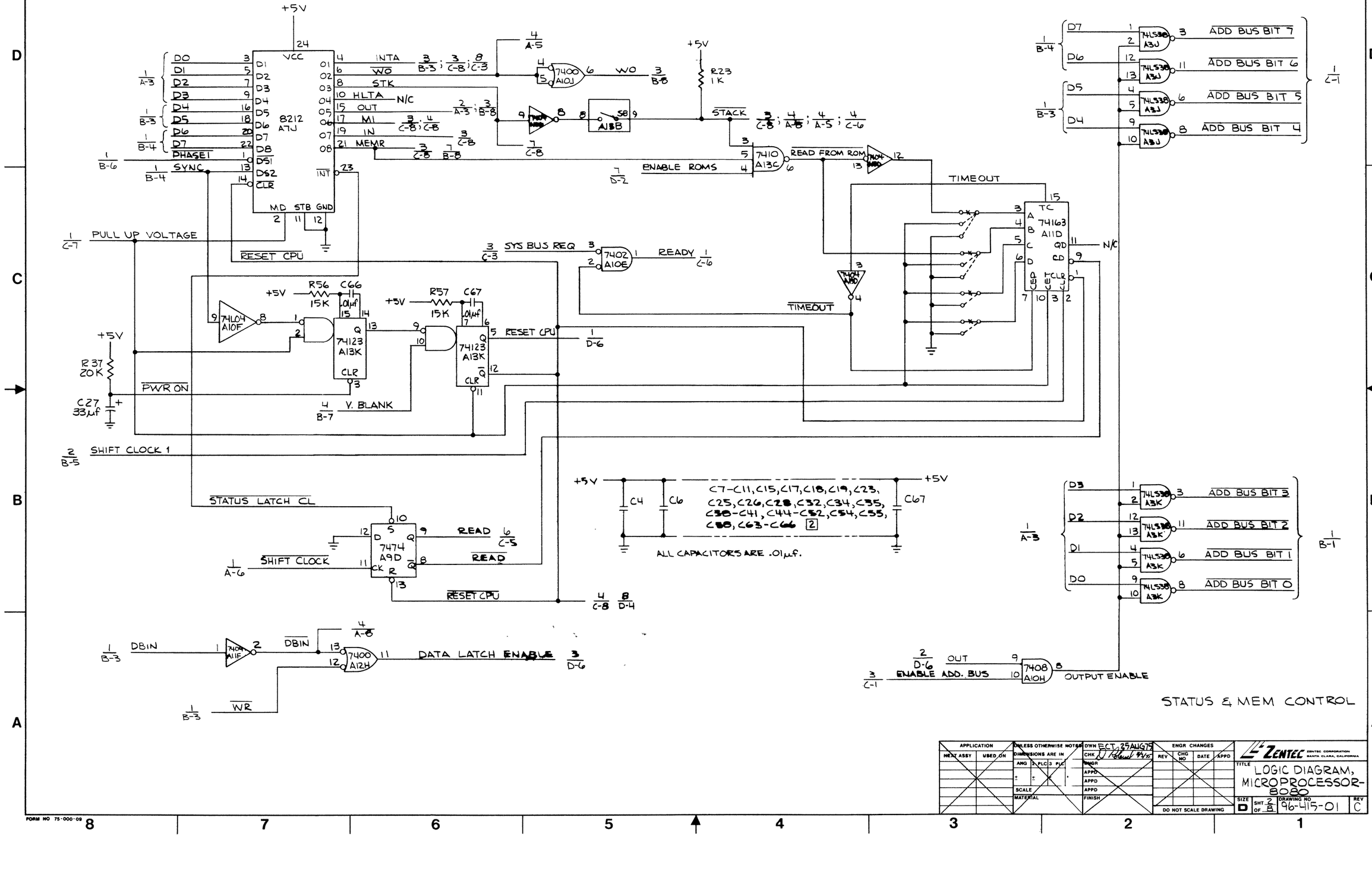
DO NOT SCALE DRAWING

ZENTEC CONTEC CORPORATION SANTA CLARA, CALIFORNIA

TITLE: LOGIC DIAGRAM, MICROPROCESSOR-8080

SIZE D | SHT 1 OF 8 | DRAWING NO 96-415-01 | REV C

FORM NO 75-000-09



STATUS & MEM CONTROL

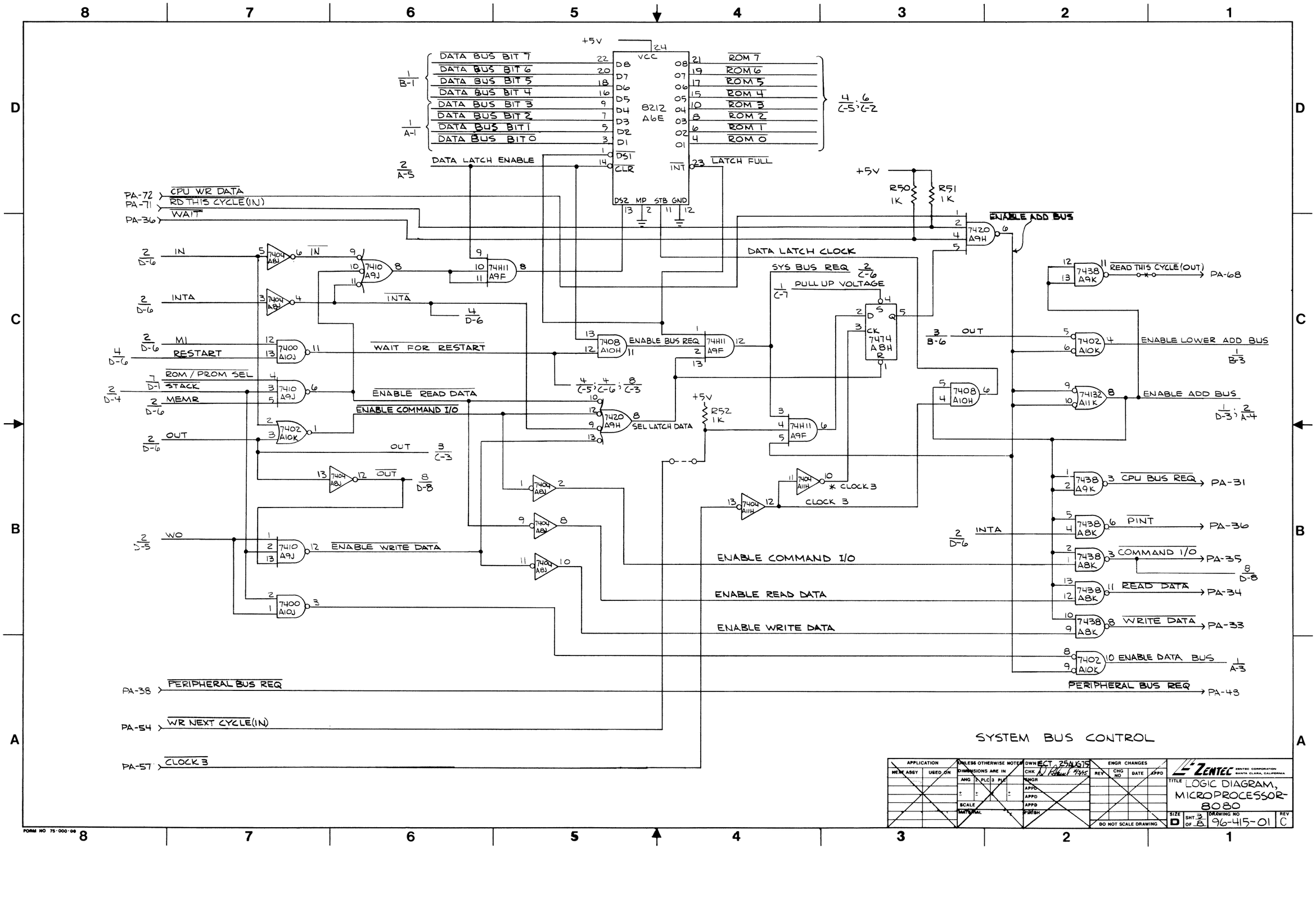
APPLICATION	UNLESS OTHERWISE NOTED	DWN ECT 25AUG75	ENGR CHANGES
NEXT ASSY / USED ON	DIMENSIONS ARE IN	CHK	REV / CHG NO / DATE / APPD
	ANG 3 PLC 3 PLC	ENGR	
	SCALE	APPD	
	MATERIAL	APPD	
		APPD	
		FINISH	
		DO NOT SCALE DRAWING	

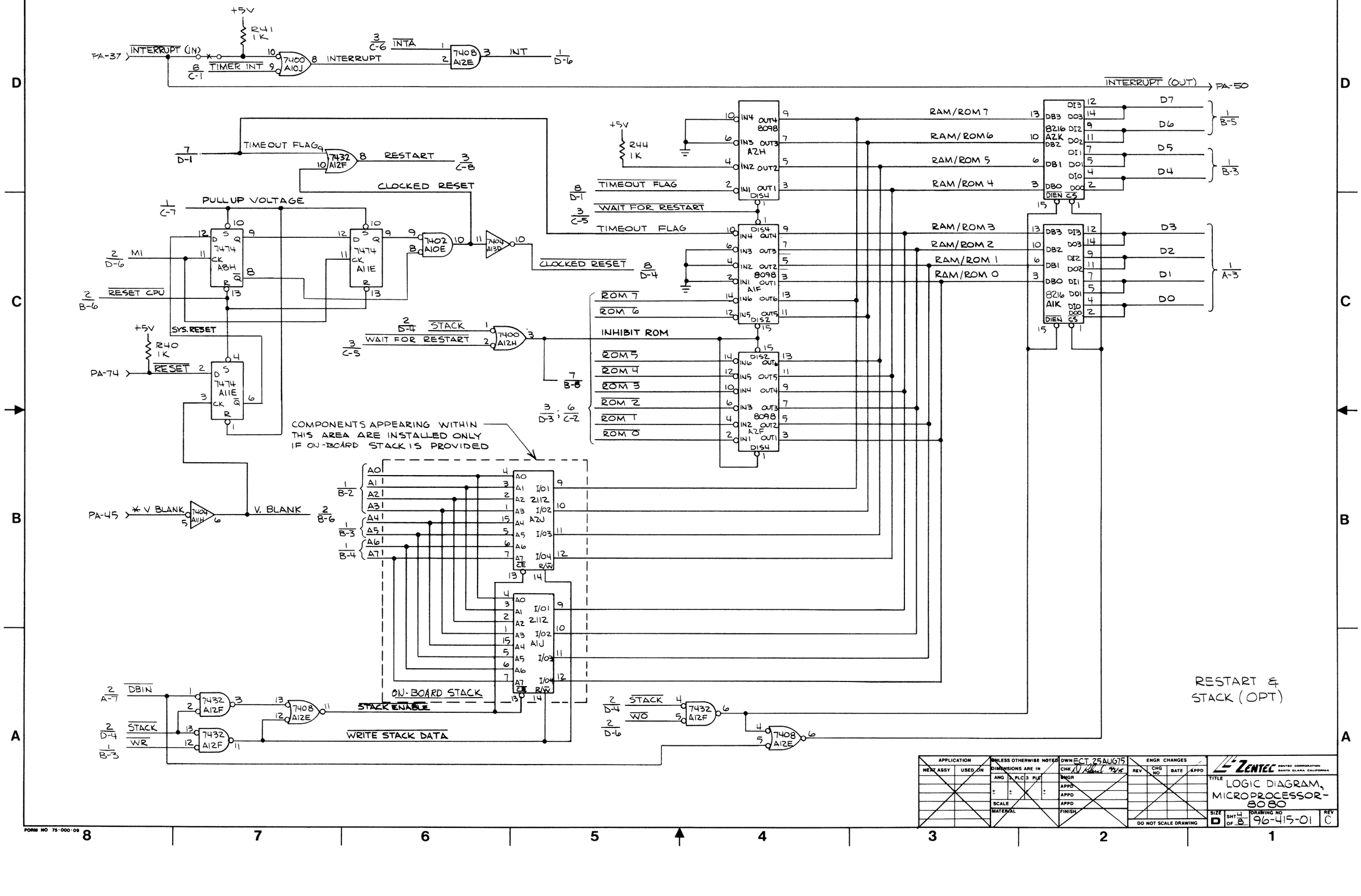
ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA

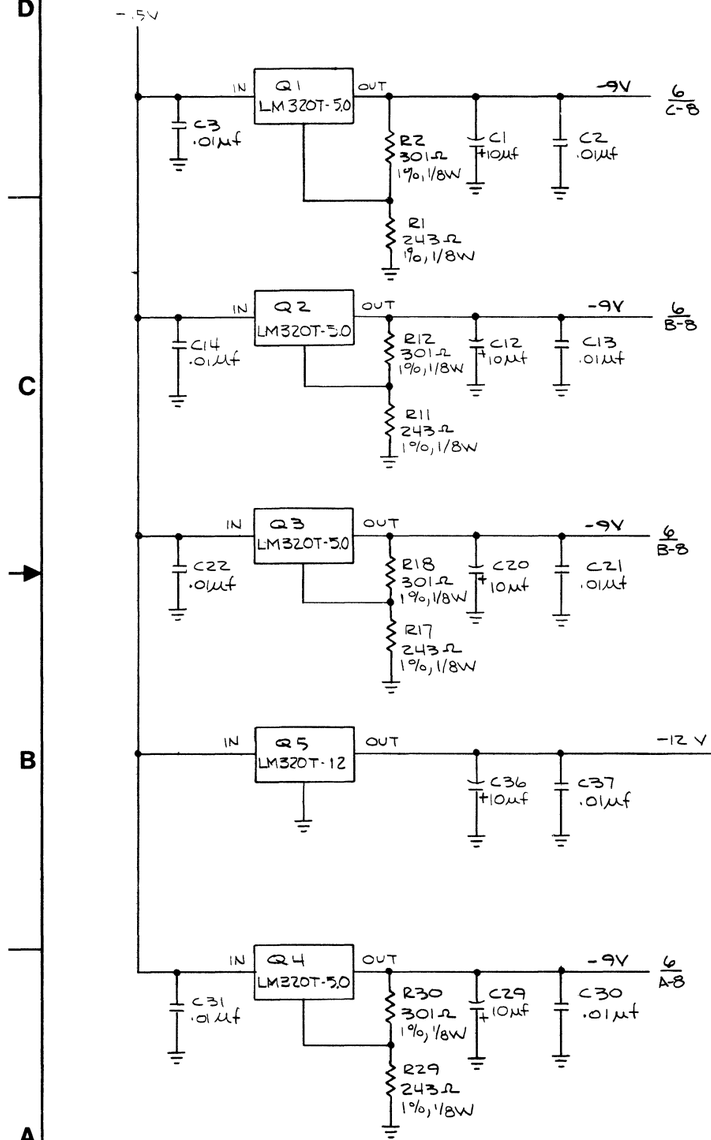
TITLE: LOGIC DIAGRAM, MICROPROCESSOR-8080

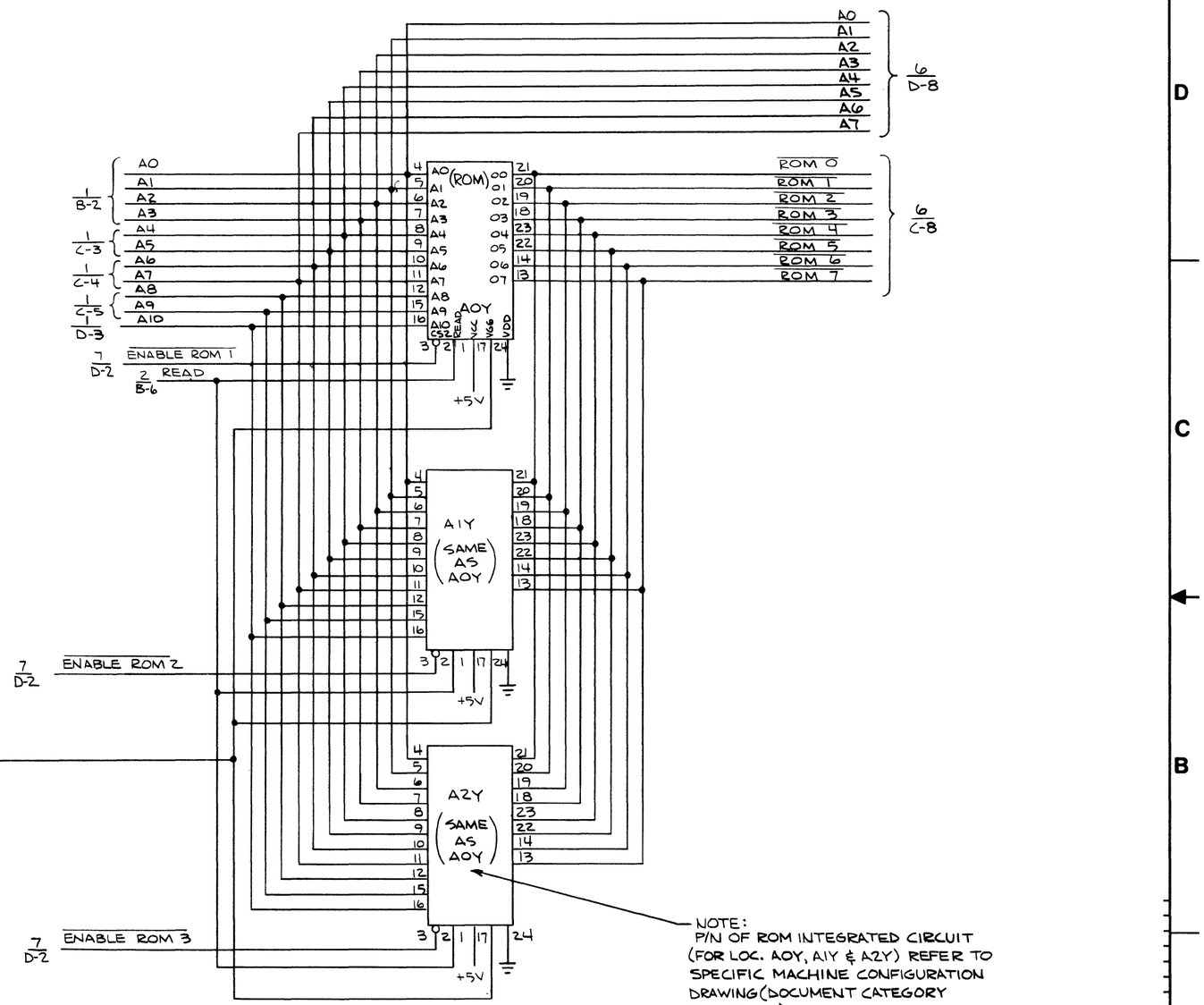
SIZE D | SHT 2 OF 8 | DRAWING NO. 96-415-01 | REV C

FORM NO 75-000-09


DATA BUS BIT 7
DATA BUS BIT 6
DATA BUS BIT 5
DATA BUS BIT 4
DATA BUS BIT 3
DATA BUS BIT 2
DATA BUS BIT 1
DATA BUS BIT 0
8212 A6E
DATA LATCH ENABLE
LATCH FULL
ROM 7
ROM 6
ROM 5
ROM 4
ROM 3
ROM 2
ROM 1
ROM 0
CPU WR DATA
RD THIS CYCLE(IN)
WAIT
IN
INTA
M1
RESTART
ROM / PROM SEL
STACK
MEMR
OUT
WO
ENABLE READ DATA
ENABLE COMMAND I/O
ENABLE WRITE DATA
WAIT FOR RESTART
ENABLE BUS REQ
SEL LATCH DATA
DATA LATCH CLOCK
SYS BUS REQ
PULL UP VOLTAGE
ENABLE ADD BUS
ENABLE LOWER ADD BUS
READ THIS CYCLE(OUT)
CPU BUS REQ
PINT
COMMAND I/O
READ DATA
WRITE DATA
ENABLE DATA BUS
PERIPHERAL BUS REQ
WR NEXT CYCLE(IN)
CLOCK 3
SYSTEM BUS CONTROL
ZENTEC
LOGIC DIAGRAM, MICROPROCESSOR-8080
96-415-01


+5V
R41 1K
PA-37
INTERRUPT (IN)
7400 A10J
TIMER INT
INTERRUPT
3 C-6 INTA
7408 A12E
INT
1 D-6
INTERRUPT (OUT)
PA-50
TIMEOUT FLAG
7432 A12F
RESTART
3 C-8
CLOCKED RESET
PULLUP VOLTAGE
1 C-7
7474 A8H
7474 A11E
7402 A10E
7404 A13D
CLOCKED RESET
8 D-4
2 D-6 M1
2 B-6 RESET CPU
SYS. RESET
+5V
R40 1K
PA-74
RESET
7474 A11E
2 D-4 STACK
WAIT FOR RESTART
3 C-5
7400 A12H
7 B-8
INHIBIT ROM
3 D-3; 6 C-2
ROM 7
ROM 6
ROM 5
ROM 4
ROM 3
ROM 2
ROM 1
ROM 0
+5V
R44 1K
8 D-1 TIMEOUT FLAG
WAIT FOR RESTART
3 C-5 TIMEOUT FLAG
8098 A1F
8098 A2F
8098 A2H
RAM/ROM 7
RAM/ROM 6
RAM/ROM 5
RAM/ROM 4
RAM/ROM 3
RAM/ROM 2
RAM/ROM 1
RAM/ROM 0
8216 A2K
8216 A1K
D7
D6
D5
D4
D3
D2
D1
D0
1 B-5
1 B-3
1 A-3
COMPONENTS APPEARING WITHIN THIS AREA ARE INSTALLED ONLY IF ON-BOARD STACK IS PROVIDED
A0
A1
A2
A3
A4
A5
A6
A7
1 B-2
1 B-3
1 B-4
2112 A2J
2112 A1J
ON-BOARD STACK
PA-45
* V BLANK
7404 A11H
V. BLANK
2 B-6
2 A-7 DBIN
2 D-4 STACK
WR
1 B-3
7432 A12F
7408 A12E
STACK ENABLE
WRITE STACK DATA
2 D-4 STACK
WO
2 D-6
RESTART & STACK (OPT)
APPLICATION
NEXT ASSY
USED ON
UNLESS OTHERWISE NOTED DIMENSIONS ARE IN
ANG
DWN ECT 25AUG75
CHK
ENGR
APPD
SCALE
MATERIAL
FINISH
DO NOT SCALE DRAWING
ENGR CHANGES
REV
CHG NO
DATE
APPD
ZENTEC ZENTEC CORPORATION SANTA CLARA CALIFORNIA
TITLE
LOGIC DIAGRAM, MICROPROCESSOR-8080
SIZE D
SHT 4 OF 8
DRAWING NO 96-415-01
REV C
FORM NO 75-000-09





ROM / PROM SECTION

APPLICATION: NEXT ASSY / USED ON	UNLESS OTHERWISE NOTED: DIMENSIONS ARE IN; ANG ± .X PLC ± .XX PLC ±	DWN ECT 25AUG75; CHK; ENGR; APPD; APPD; APPD; FINISH; SCALE:; MATERIAL	ENGR CHANGES: REV / CHG NO. / DATE / APPD; DO NOT SCALE DRAWING
ZENTEC ZENITH CORPORATION SANTA CLARA, CALIFORNIA	TITLE: LOGIC DIAGRAM, MICROPROCESSOR-8080	SIZE D; SHT 5 OF 8; DRAWING NO. 96-415-01; REV C	

FORM NO 75-000-09

NOTE:
P/N OF PROM INTEGRATED CIRCUIT (FOR LOC. A0W THRU A7W AND A0X THRU A7X), REFER TO SPECIFIC MACHINE CONFIGURATION DRAWING (DOCUMENT CATEGORY 10-XXX-XX).

ROM / PROM SECTION

APPLICATION		UNLESS OTHERWISE NOTED	DWN ECT 25AUG75	ENGR CHANGES				ZENTEC	
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK	REV	CHG NO.	DATE	APPD	TITLE	LOGIC DIAGRAM, MICROPROCESSOR-8080
		ANG ± PLC ± .3 PLC ±	ENGR						
			APPD						
		SCALE:	APPD						
		MATERIAL	FINISH					SIZE D	SHT 6 OF 8 DRAWING NO. 96-415-01 REV C
				DO NOT SCALE DRAWING					

FORM NO 75-000-09

ROM 1&2 ENABLE
1ST 2K
2ND 2K
3RD 2K
ENABLE ROM 1
ENABLE ROM 2
ENABLE ROM 3
ROM 3 ENABLE
ENABLE ROMS
ROM / PROM SEL
1ST 8K
LAST 8K
STK
INHIBIT ROM
MEMR
1ST 1K
2ND 1K
3RD 1K
4TH 1K
5TH 1K
6TH 1K
7TH 1K
8TH 1K
ENABLE PROMS
GP ONE SEL
GP TWO SEL
PULL UP VOLTAGE
ROM / PROM ENABLES

TITLE	LOGIC DIAGRAM, MICROPROCESSOR-8080
DRAWING NO	96-415-01
REV	C
SIZE	D
SHT	7 OF 8
ZENTEC	ZENTEC CORPORATION SANTA CLARA, CALIFORNIA

FORM NO 75-000-09

PA-55 > CLOCK 2

ADD BUS BIT 10
ADD BUS BIT 9
ADD BUS BIT 8
OUT
3 B-6
7442A ASF

ADD BUS BIT 11
ADD BUS BIT 12
ADD BUS BIT 13
COMMAND I/O
3 B-1
7442A ASH

LOAD UPPER
LOAD LOWER
LOAD LOWER CL
LOAD UPPER CL

2 B-6 RESET CPU
4 C-5 CLOCKED RESET
7408 A7D
CLEAR TIME OUT

+5V
R35 1K
7402 A8C
TIMEOUT FLAG 4 D-7
7414 A8E
TIMEOUT FLAG 4 C-5

7432 A7C

2 D-6 INTA
7474 A8D
WAIT FOR RESTART 3 C-5

+5V
R55 1K
TIMER INT 4 D-7

1 B-1 DATA BUS BIT 7
DATA BUS BIT 6
DATA BUS BIT 5
DATA BUS BIT 4
1 A-1 DATA BUS BIT 3
DATA BUS BIT 2
DATA BUS BIT 1
DATA BUS BIT 0

1 C-7 PULLUP VOLTAGE

74161 OR 9316 A7H
74161 OR 9316 A7F
74161 OR 9316 A6H
74161 OR 9316 A6F
74161 OR 9316 A9E
QA QB QC QD

TIMEOUT 15 DONE
7474 A7E
7402 A8F

TIMEOUT DONE
TIMEOUT CLOCK

THIS TRACE MAY BE CUT TO DISABLE TIMER CIRCUITRY

COMPONENTS APPEARING WITHIN THIS AREA ARE INSTALLED ONLY IF OPTIONAL TIMER IS PROVIDED

PA-46 > SHIFT GATE
7414 A8E
SHIFT GATE

TIMER (OPTIONAL)

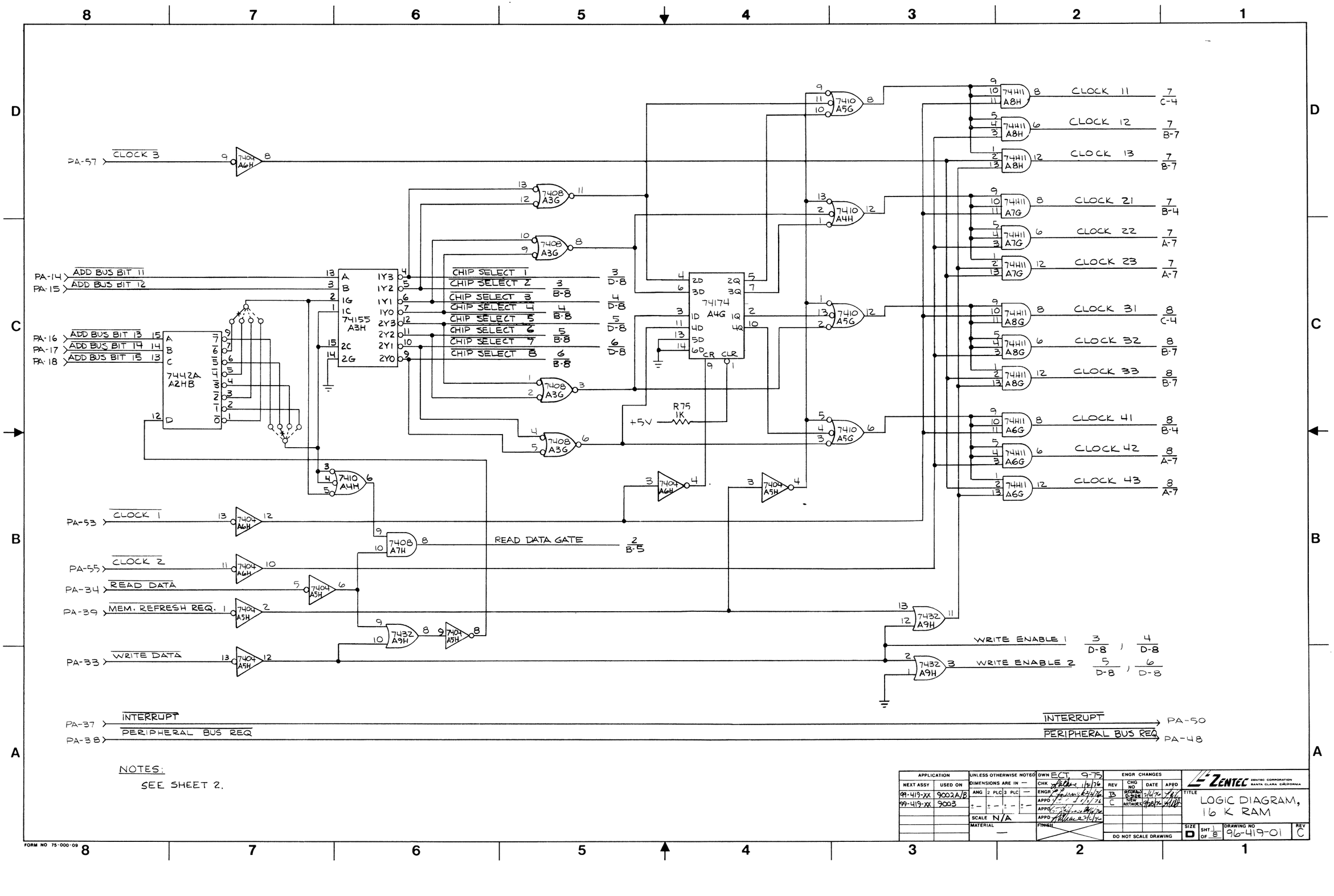
APPLICATION		UNLESS OTHERWISE NOTED		ENGR CHANGES			
NEXT ASSY	USED ON	DIMENSIONS ARE IN	DWN ECT 25AUG75	REV	CHG NO.	DATE	APPD
		ANG ±	3 PLC ±	2 PLC ±	CHK		
		SCALE:	MATERIAL		ENGR		
					APPD		
					APPD		
					APPD		
					FINISH		
		DO NOT SCALE DRAWING					

ZENTEC CORPORATION SANTA CLARA, CALIFORNIA

TITLE LOGIC DIAGRAM, MICROPROCESSOR-8080

SIZE D | SHT. 8 OF 8 | DRAWING NO. 96-415-01 | REV C

FORM NO 75-000-09

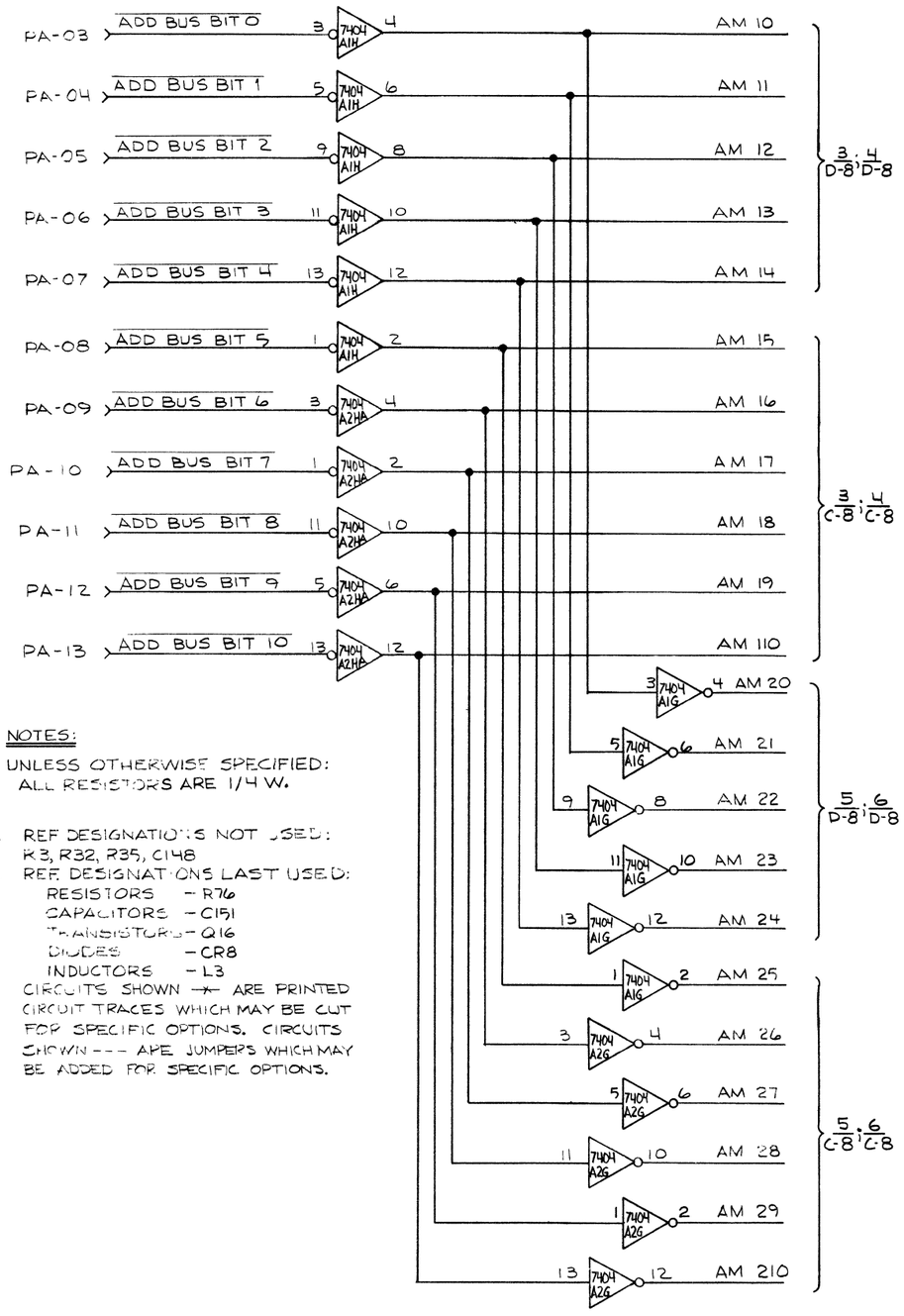


NOTES:

SEE SHEET 2.

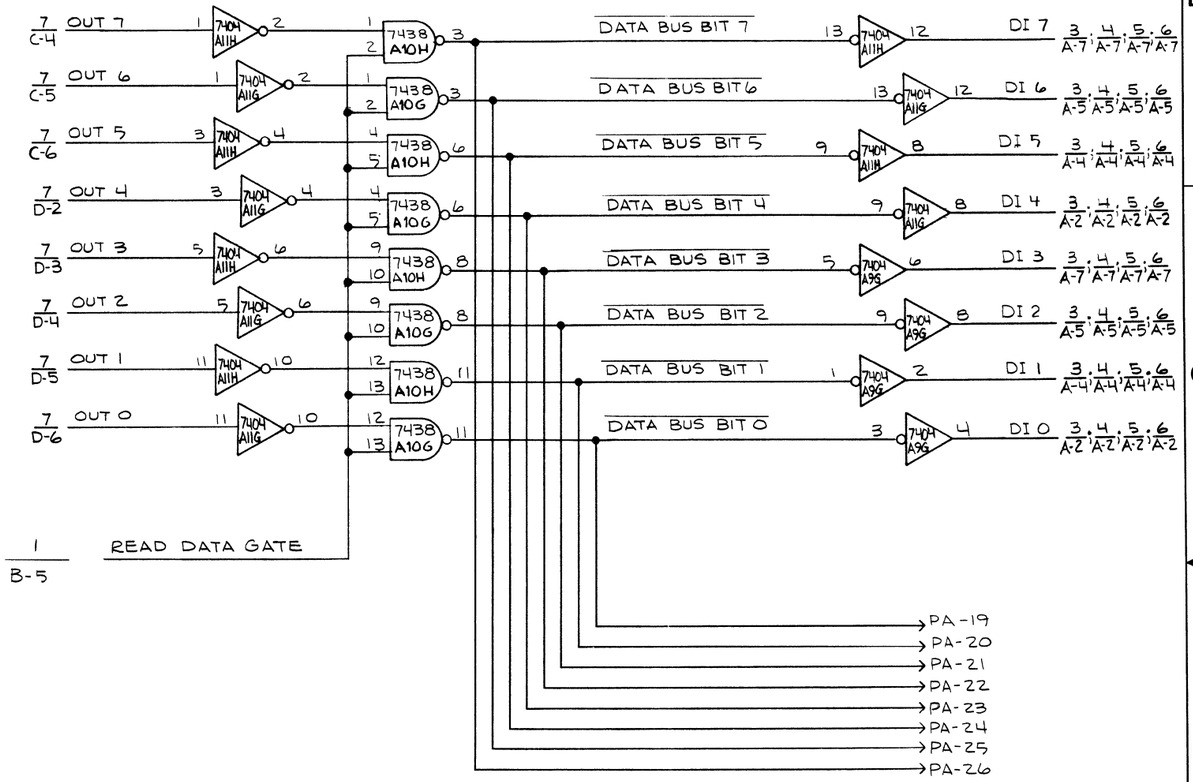
APPLICATION		UNLESS OTHERWISE NOTED	DWN ECT 9-75	ENGR CHANGES				ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA
NEXT ASSY	USED ON	DIMENSIONS ARE IN —	CHK 1/14/76	REV	CHG NO	DATE	APPD	TITLE
99-419-XX	9002A/B	ANG ± — 2 PLC ± — 3 PLC ± —	ENGR 1/14/76	B	RELEASED PER ECO	2/4/76		LOGIC DIAGRAM, 16 K RAM
99-419-XX	9003		APPD 1/14/76	C	NEW ARTWORK	4/20/76		
		SCALE N/A	APPD 2/4/76					
		MATERIAL —	FINISH	DO NOT SCALE DRAWING				SIZE D SHT 1 OF 8 DRAWING NO 96-419-01 REV C

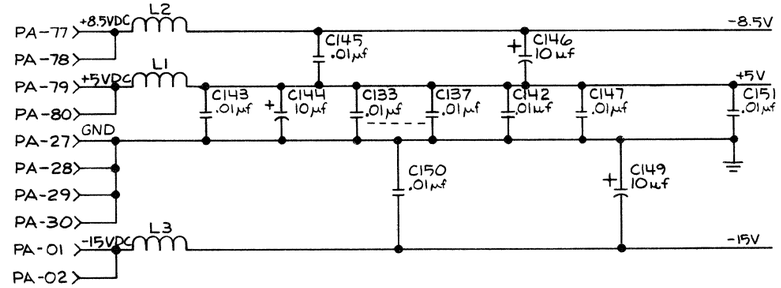
FORM NO 75-000-09



NOTES:

1. UNLESS OTHERWISE SPECIFIED: ALL RESISTORS ARE 1/4 W.
2. REF DESIGNATIONS NOT USED: R3, R32, R35, C148
3. REF. DESIGNATIONS LAST USED:
   RESISTORS - R76
   CAPACITORS - C151
   TRANSISTORS - Q16
   DIODES - CR8
   INDUCTORS - L3
4. CIRCUITS SHOWN —*— ARE PRINTED CIRCUIT TRACES WHICH MAY BE CUT FOR SPECIFIC OPTIONS. CIRCUITS SHOWN - - - ARE JUMPERS WHICH MAY BE ADDED FOR SPECIFIC OPTIONS.





APPLICATION		UNLESS OTHERWISE NOTED	DWN ECT 9-75	ENGR CHANGES				ZENTEC ZENTEC CORPORATION SANTA CLARA CALIFORNIA
NEXT ASSY	USED ON	DIMENSIONS ARE IN —	CHK [illegible] 11/3/76	REV	CHG NO	DATE	APPD	TITLE
		ANG 2 PLC 3 PLC —	ENGR					LOGIC DIAGRAM, 16K RAM
		± — ± — ± — ± —	APPD					
		SCALE N/A	APPD					
		MATERIAL —	APPD					
			FINISH	DO NOT SCALE DRAWING				SIZE D SHT 2 OF 2 DRAWING NO 96-419-01 REV C

FORM NO 75-000-09

NOTE: ALL MEM CHIP VOLTAGES WILL TIE WITH CORRECT VOLTAGE ON PAGE 8 ZONES D-3 THRU D-8. ALL MEMORY CHIPS ARE MM5262 OR 600314.

INSIDE CHIP DESIGNATION DATA TYPICAL-16 PLCS

+5V

R16 470Ω

2 D-5 { AM 10, AM 11, AM 12, AM 13, AM 14

7 B-5 { MI CLOCK 2, MI CLOCK 3

7 C-1 MI CLOCK 1

1 C-6 CHIP SELECT 1

1 C-6 WRITE ENABLE 1

A-2

2 C-5 { AM 15, AM 16, AM 17, AM 18, AM 19, AM 110

A3S A2S A1S A0S

A7S A6S A5S A4S

A3T A2T A1T A0T

A7T A6T A5T A4T

+5V +8.5V -15V

R12 470Ω R10 470Ω R8 470Ω

R11 470Ω R9 470Ω R15 470Ω

R29 470Ω R1 470Ω R6 470Ω

R7 470Ω R4 470Ω

R5 470Ω R2 470Ω

R33 470Ω R23 470Ω

1 C-6 CHIP SELECT 2

DOM 7 7 C-5

DOM 3 7 D-4

DOM 6 7 C-6

DOM 2 7 D-5

DOM 5 7 C-7

DOM 1 7 D-6

DOM 4 7 D-3

DOM 0 7 D-7

2 C-1 DI 3

2 D-1 DI 7

2 C-1 DI 2

2 D-1 DI 6

2 C-1 DI 1

2 D-1 DI 5

2 C-1 DI 0

2 C-1 DI 4

R22 470Ω R19 470Ω R26 470Ω R18 470Ω R27 470Ω R21 470Ω

APPLICATION		UNLESS OTHERWISE NOTED		DWN		ENGR CHANGES				ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA
NEXT ASSY	USED ON	DIMENSIONS ARE IN		CHK		REV	CHG NO	DATE	APPD	
		ANG 2 PLC 3 PLC		ENGR						TITLE LOGIC DIAGRAM, 16K RAM
		± — ± — ± —		APPD						
		SCALE N/A		APPD						
		MATERIAL		FINISH						
						DO NOT SCALE DRAWING				SIZE D SHT 3 OF 8 DRAWING NO 96-419-01 REV C

FORM NO 75-000-09

R30 470Ω +5V

R34 470Ω +5V

NOTE: ALL MEM CHIP VOLTAGES WILL TIE WITH CORRECT VOLTAGE ON PAGE 8 ZONES D5 THRU D-8 & C-5 THRU C-8. ALL MEMORY CHIPS ARE MM5262 OR 600314.

INSIDE CHIP DESIGNATION DATA TYPICAL-16 PLCS

2 D-5 AM 10, AM 11, AM 12, AM 13, AM 14

7 A-5 MZ CLOCK 2, MZ CLOCK 3

7 B-2 MZ CLOCK 1

1 C-6 CHIP SELECT 3

1 A-2 WRITE ENABLE 1

2 C-5 AM 15, AM 16, AM 17, AM 18, AM 19, AM 110

1 C-6 CHIP SELECT 4

A3U A2U A1U A0U

A7U A6U A5U A4U

A3V A2V A1V A0V

A7V A6V A5V A4V

DOM 7 7 C-5

DOM 6 7 C-6

DOM 5 7 C-7

DOM 4 7 D-3

DOM 3 7 D-4

DOM 2 7 D-5

DOM 1 7 D-6

DOM 0 7 D-7

2 C-1 DI 3

2 C-1 DI 2

2 C-1 DI 1

2 C-1 DI 0

2 D-1 DI 7

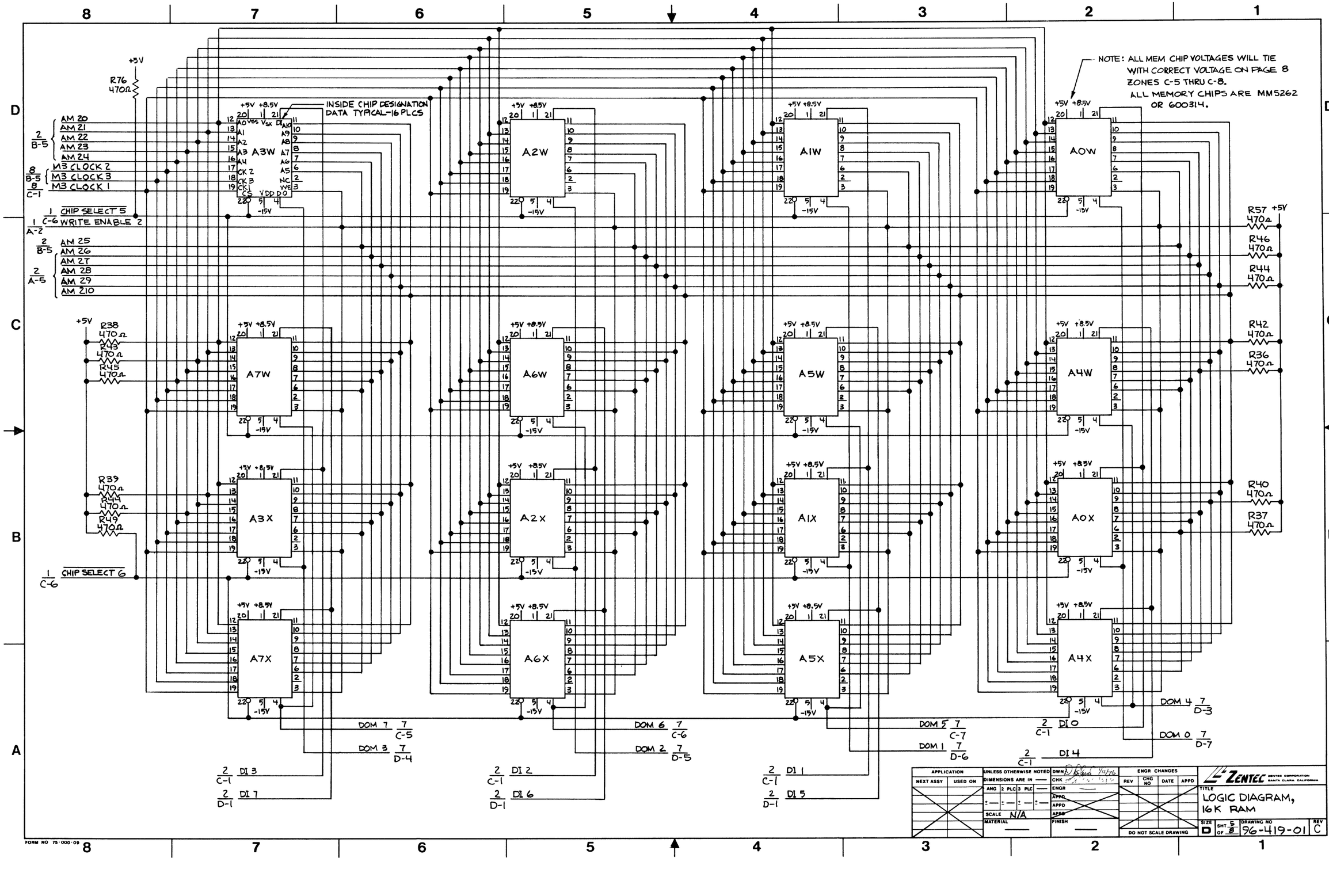
2 D-1 DI 6

2 D-1 DI 5

2 C-1 DI 4

APPLICATION		UNLESS OTHERWISE NOTED	DWN	ENGR CHANGES				ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA
NEXT ASSY	USED ON	DIMENSIONS ARE IN —	CHK	REV	CHG NO	DATE	APPD	TITLE
		ANG ± — 2 PLC ± — 3 PLC ± —	ENGR					LOGIC DIAGRAM, 16K RAM
		SCALE N/A	APPD					
		MATERIAL —	APPD					
			FINISH —	DO NOT SCALE DRAWING				SIZE D SHT 4 OF 8 DRAWING NO 96-419-01 REV C

FORM NO 75-000-09


NOTE: ALL MEM CHIP VOLTAGES WILL TIE WITH CORRECT VOLTAGE ON PAGE 8 ZONES C-5 THRU C-8. ALL MEMORY CHIPS ARE MM5262 OR 600314.
INSIDE CHIP DESIGNATION DATA TYPICAL-16 PLCS
+5V
R76 470Ω
AM 20
AM 21
AM 22
AM 23
AM 24
2 B-5
M3 CLOCK 2
M3 CLOCK 3
M3 CLOCK 1
8 B-5
8 C-1
CHIP SELECT 5
1 C-6
WRITE ENABLE 2
1 A-2
AM 25
AM 26
AM 27
AM 28
AM 29
AM 210
2 B-5
2 A-5
R38 470Ω
R43 470Ω
R45 470Ω
R39 470Ω
R44 470Ω
R49 470Ω
1 C-6 CHIP SELECT 6
A3W
A2W
A1W
A0W
A7W
A6W
A5W
A4W
A3X
A2X
A1X
A0X
A7X
A6X
A5X
A4X
+5V +8.5V
-15V
R57 470Ω
R46 470Ω
R44 470Ω
R42 470Ω
R36 470Ω
R40 470Ω
R37 470Ω
DOM 7 7 C-5
DOM 3 7 D-4
DOM 6 7 C-6
DOM 2 7 D-5
DOM 5 7 C-7
DOM 1 7 D-6
DOM 4 7 D-3
DOM 0 7 D-7
2 C-1 DI 3
2 D-1 DI 7
2 C-1 DI 2
2 D-1 DI 6
2 C-1 DI 1
2 D-1 DI 5
2 C-1 DI 0
2 C-1 DI 4
APPLICATION
NEXT ASSY
USED ON
UNLESS OTHERWISE NOTED DIMENSIONS ARE IN
ANG 2 PLC 3 PLC
SCALE N/A
MATERIAL
DWN
CHK
ENGR
APPD
APPD
APPD
FINISH
ENGR CHANGES
REV
CHG NO
DATE
APPD
DO NOT SCALE DRAWING
ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA
TITLE
LOGIC DIAGRAM, 16K RAM
SIZE D
SHT 5 OF 8
DRAWING NO 96-419-01
REV C
FORM NO 75-000-09

NOTE: ALL MEM CHIP VOLTAGES WILL TIE WITH CORRECT VOLTAGE ON PAGE 8 ZONES D-1 THRU D-4. ALL MEMORY CHIPS ARE MM5262 OR 600314.

INSIDE CHIP DESIGNATION DATA TYPICAL-16 PLCS

+5V

R51 470Ω

R53 470Ω

+5V +8.5V

-15V

A3Y A2Y A1Y A0Y

A7Y A6Y A5Y A4Y

A3Z A2Z A1Z A0Z

A7Z A6Z A5Z A4Z

2 B-5 AM 20
AM 21
AM 22
AM 23
AM 24

8 A-5 MU CLOCK 2
MU CLOCK 3

8 B-2 MU CLOCK 1

1 C-6 CHIP SELECT 7

1 A-2 WRITE ENABLE 2

2 B-5 AM 25

2 A-5 AM 26
AM 27
AM 28
AM 29
AM 210

1 C-6 CHIP SELECT 8

DOM 7 7 C-5

DOM 3 7 D-4

DOM 6 7 C-6

DOM 2 7 D-5

DOM 5 7 C-7

DOM 1 7 D-6

DOM 4 7 D-3

DOM 0 7 D-7

2 C-1 DI 3

2 D-1 DI 7

2 C-1 DI 2

2 D-1 DI 6

2 C-1 DI 1

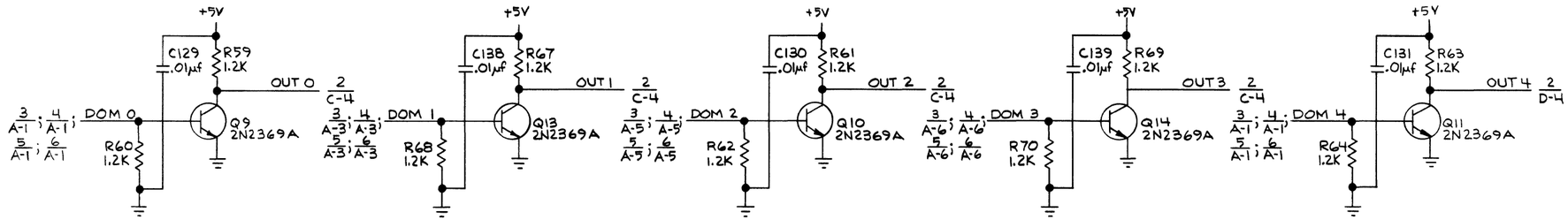
2 D-1 DI 5

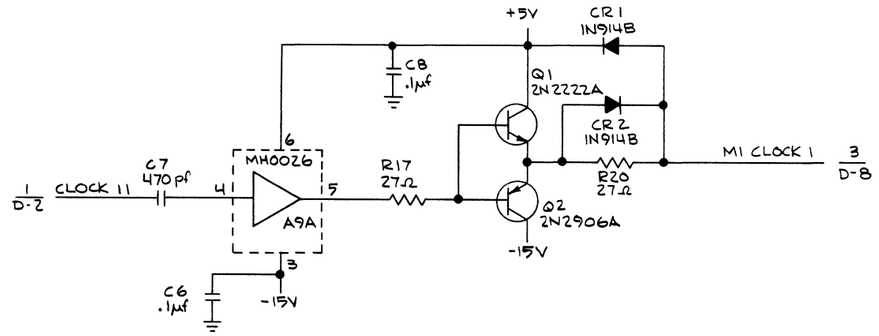
2 C-1 DI 0

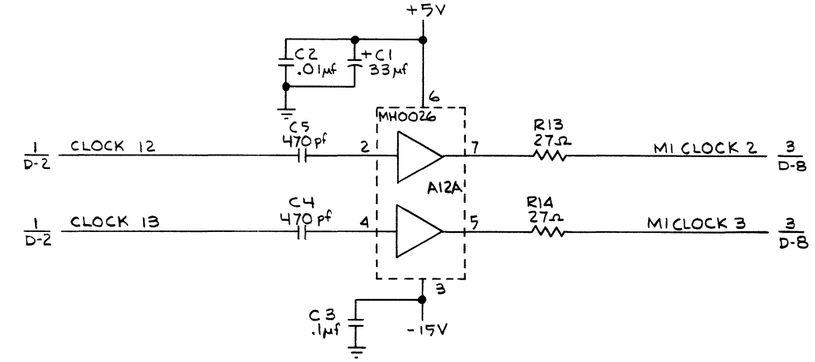
2 C-1 DI 4

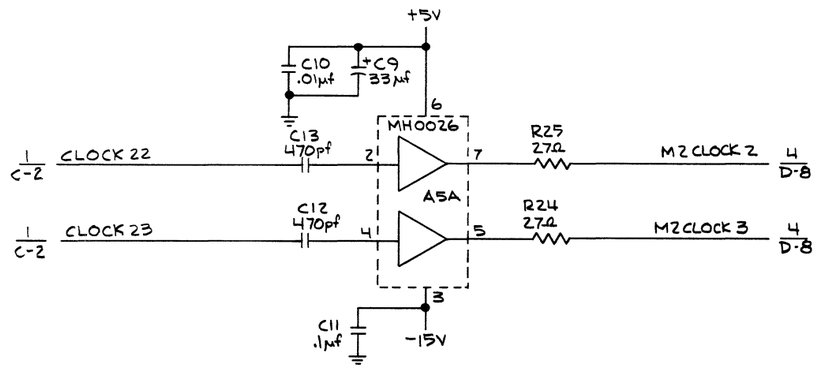
APPLICATION		UNLESS OTHERWISE NOTED	DWN	ENGR CHANGES				ZENTEC ZENTEC CORPORATION SANTA CLARA CALIFORNIA
NEXT ASSY	USED ON	DIMENSIONS ARE IN	CHK	REV	CHG NO	DATE	APPD	TITLE
		ANG 2 PLC 3 PLC	ENGR					LOGIC DIAGRAM, 16K RAM
			APPD					
		SCALE N/A	APPD					
		MATERIAL	FINISH	DO NOT SCALE DRAWING				SIZE D SHT 6 OF 8 DRAWING NO 96-419-01 REV C

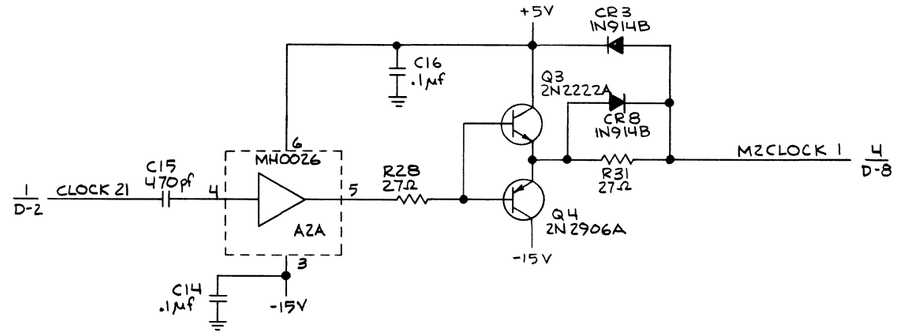
FORM NO 75 000-09











APPLICATION		UNLESS OTHERWISE NOTED	DWN D. Pollard 1/16/76	ENGR CHANGES				ZENTEC ZENTEC CORPORATION SANTA CLARA CALIFORNIA
NEXT ASSY	USED ON	DIMENSIONS ARE IN —	CHK [illegible] 1/17/76	REV	CHG NO	DATE	APPD	TITLE LOGIC DIAGRAM, 16K RAM
		ANG 2 PLC 3 PLC	ENGR					
		SCALE N/A	APPD					
		MATERIAL	APPD	DO NOT SCALE DRAWING				SIZE D SHT 7 OF 8 DRAWING NO 96-419-01 REV C
			FINISH					

FORM NO 75-000-09

ALL CAPACITORS ARE .01μf

+8.5V
+5V
GND
-15V

C18 C19 C21 C22 C24 C25 C27 C28 C30 C31 C33 C34 C36 C37 C39 C40
C17 C20 C23 C26 C29 C32 C35 C38

C42 C43 C45 C46 C48 C49 C51 C52 C54 C55 C57 C58 C60 C61 C63 C64
C41 C44 C47 C50 C53 C56 C59 C62

C66 C67 C69 C70 C72 C73 C75 C76 C78 C79 C81 C82 C84 C85 C87 C88
C65 C68 C71 C74 C77 C80 C83 C86

ALL CAPACITORS ARE .01μf

C90 C91 C93 C94 C96 C97 C99 C100 C102 C103 C105 C106 C108 C109 C111 C112
C89 C92 C95 C98 C101 C104 C107 C110

+5V
CR 4 IN914B
C120 .1μf
Q5 2N2222A
CR 5 IN914B
M3 CLOCK 1 5 D-8
1 C-2 CLOCK 31
C119 470pf
MH0026
A9F
R50 27Ω
R52 27Ω
Q6 2N2906A
-15V
C118 .1μf
-15V

+5V
C114 .01μf
C113 33μf
MH0026
1 C-2 CLOCK 32
C117 470pf
R47 27Ω
M3 CLOCK 2 5 D-8
A12F
1 C-2 CLOCK 33
C116 470pf
R48 27Ω
M3 CLOCK 3 5 D-8
C115 .1μf
-15V

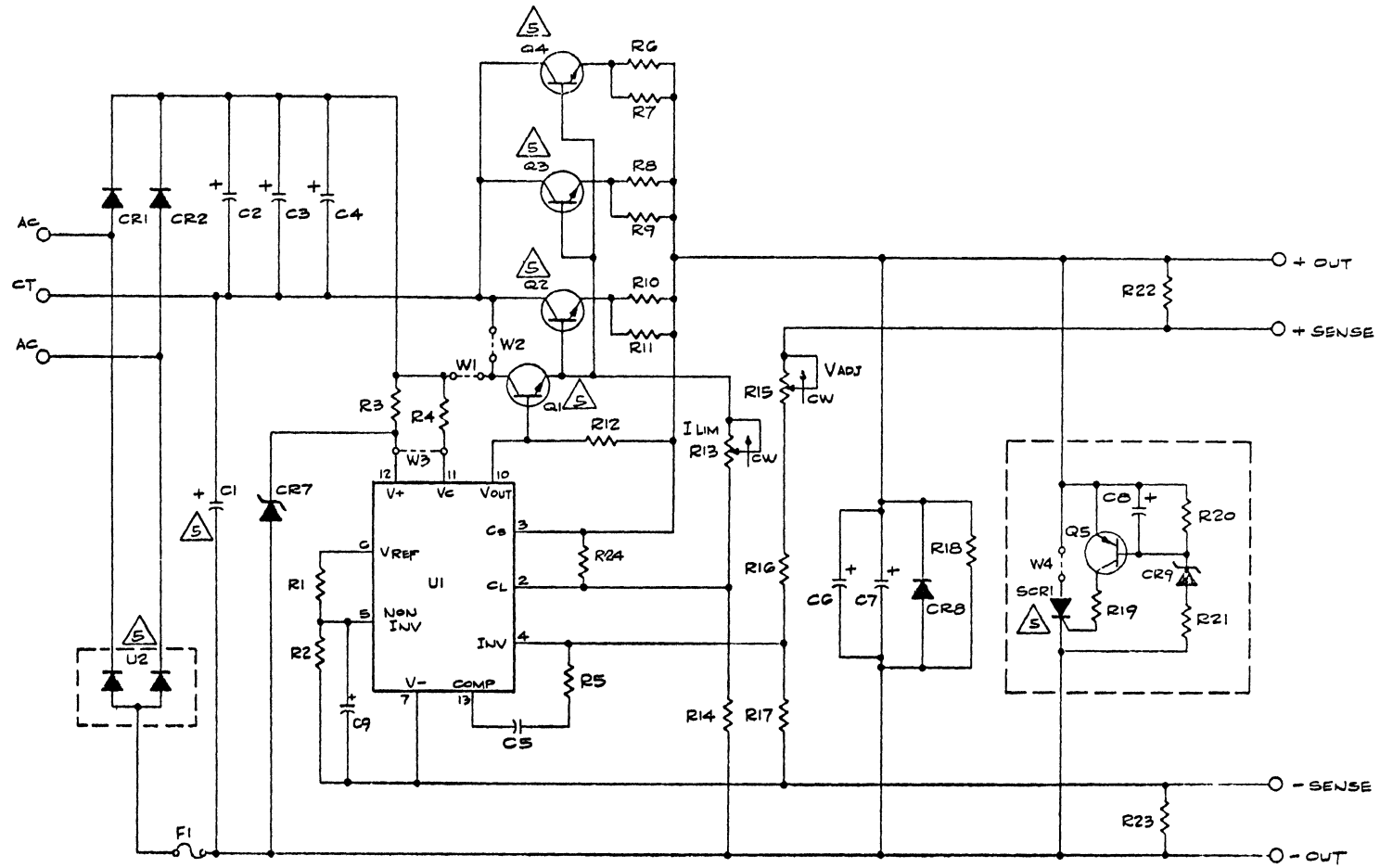
+5V
CR6 IN914B
C128 .1μf
Q7 2N2222A
CR7 IN914B
M4 CLOCK 1 6 D-8
1 C-2 CLOCK 41
C127 470pf
MH0026
A2F
R56 27Ω
R58 27Ω
Q8 2N2906A
-15V
C126 .1μf
-15V

+5V
C122 .01μf
C121 33μf
MH0026
1 B-2 CLOCK 42
C125 470pf
R54 27Ω
M4 CLOCK 2 6 D-8
A5F
1 B-2 CLOCK 43
C124 470pf
R55 27Ω
M4 CLOCK 3 6 D-8
C123 .1μf
-15V

APPLICATION		UNLESS OTHERWISE NOTED	DWN	ENGR CHANGES				ZENTEC ZENTEC CORPORATION SANTA CLARA CALIFORNIA
NEXT ASSY	USED ON	DIMENSIONS ARE IN —	CHK	REV	CHG NO	DATE	APPD	TITLE
		ANG 2 PLC 3 PLC —	ENGR					LOGIC DIAGRAM, 16K RAM
		± — ± — ± —	APPD					
		SCALE N/A	APPD					
		MATERIAL	FINISH	DO NOT SCALE DRAWING				SIZE D SHT 8 OF 8 DRAWING NO 96-419-01 REV C

FORM NO 75-000-09

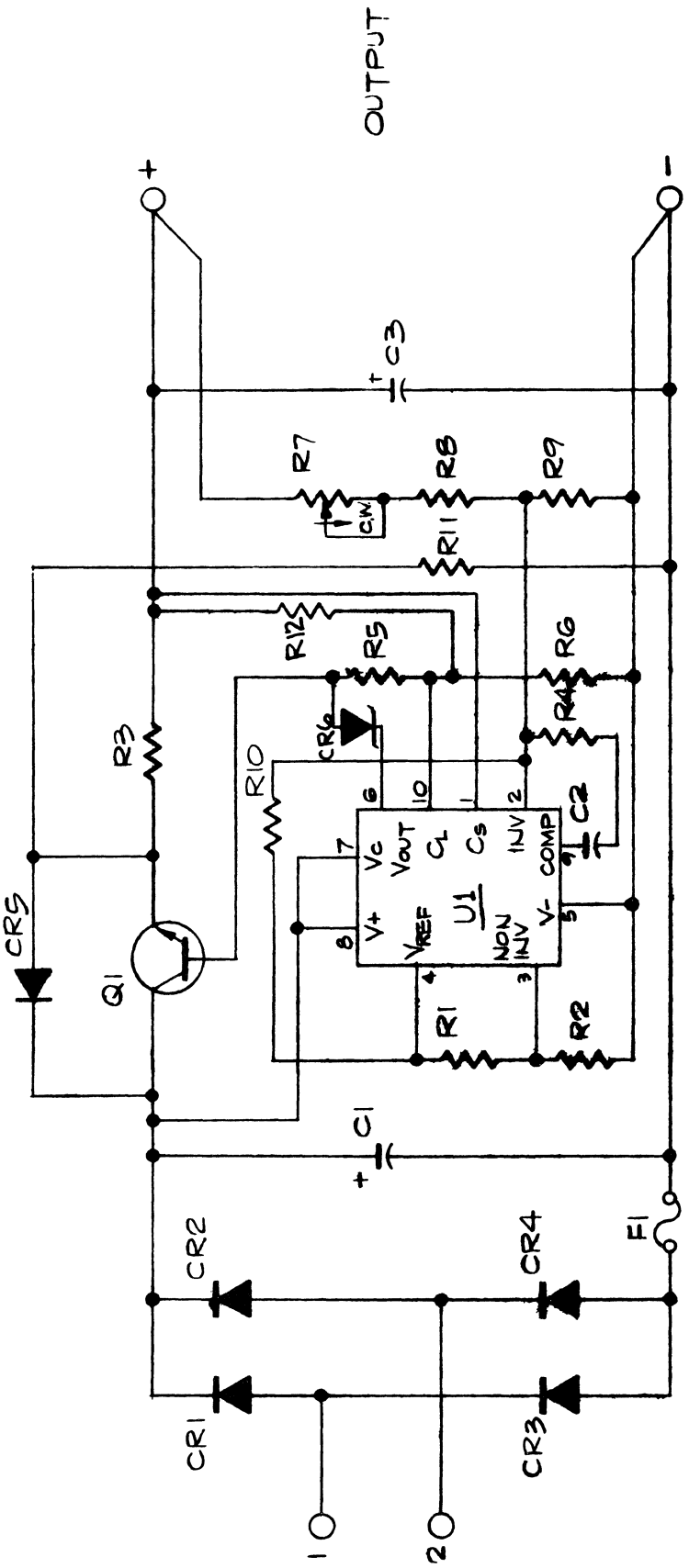
SCHEMATIC FOR 5 VOLT POWER SUPPLY.



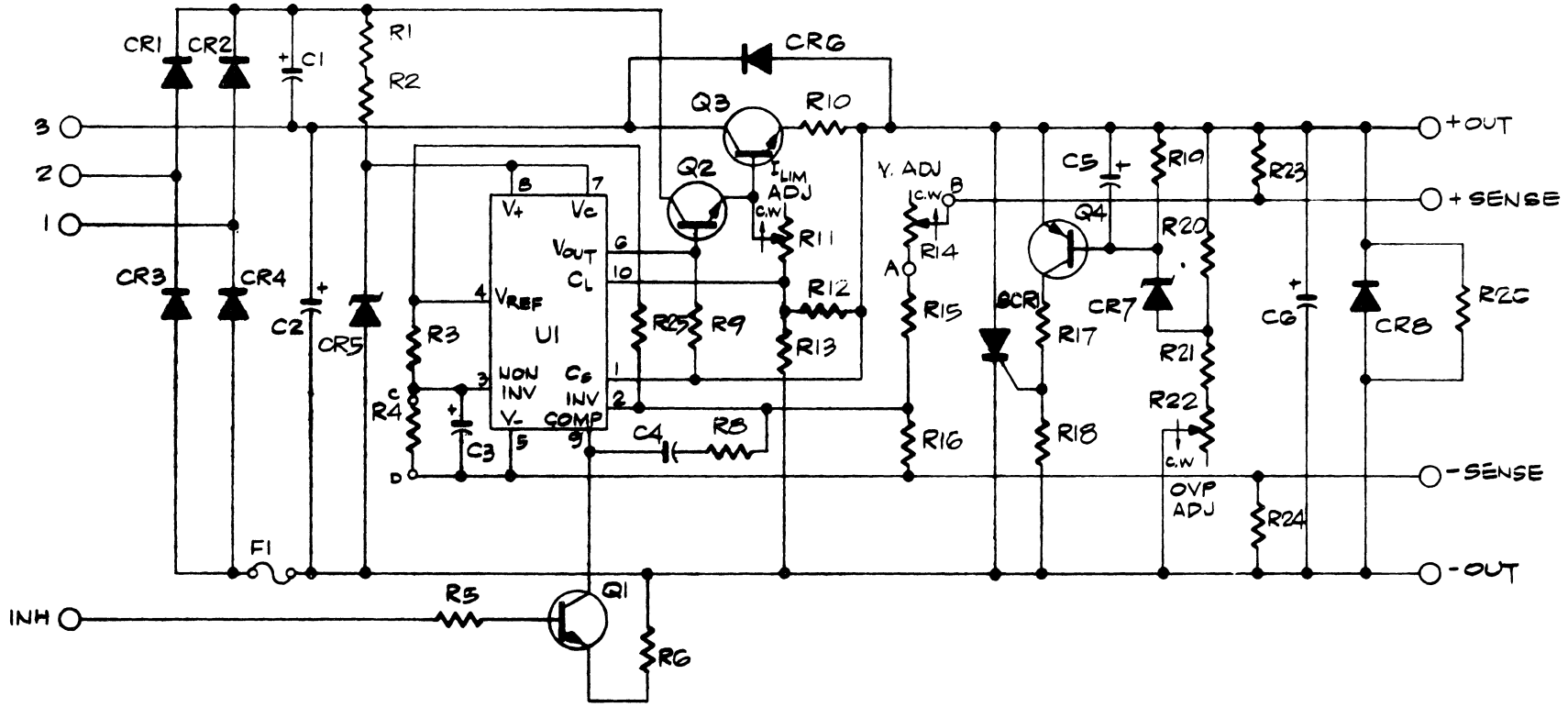
5 CHASSIS MOUNTED COMPONENT

4. 'W4' USED ON 'D' CASE ONLY.
3. RESISTANCE GIVEN IN OHMS, CAPACITANCE GIVEN IN MICROFARADS.
2. NOT USED — CR3,4,5,6
1. LAST USED — R24, C9, CR9, SCR1, Q5, U2, W4, F1

NOTE: UNLESS OTHERWISE SPECIFIED



SCHEMATIC FOR 3.5 AND 12 VOLT POWER SUPPLIES.



SCHEMATIC FOR 15 VOLT POWER SUPPLY.

TABLE 2
I.D. WORD [5]

	(MSB)							(LSB)
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
A11H SWITCH NO →	S2	S1	S3	S4	S5	S6	S7	S8
	'SEL' BAUD RATE SWITCH OFF = 0/SWITCH ON = 1 REF: TABLE 1		I.D. NUMBER SWITCH OFF = 1/SWITCH ON = 0					

CUT TRACES MARKED BY "X" AND ADD JUMPERS USING BUS WIRE (ITEM 85) AND INSUL. WIRE (ITEM 84) WHEN CROSSING TRACES. USED ON -05 VERSION ONLY.

(75) -04 & -06 VERSIONS ONLY
(76) -05 VERSION ONLY

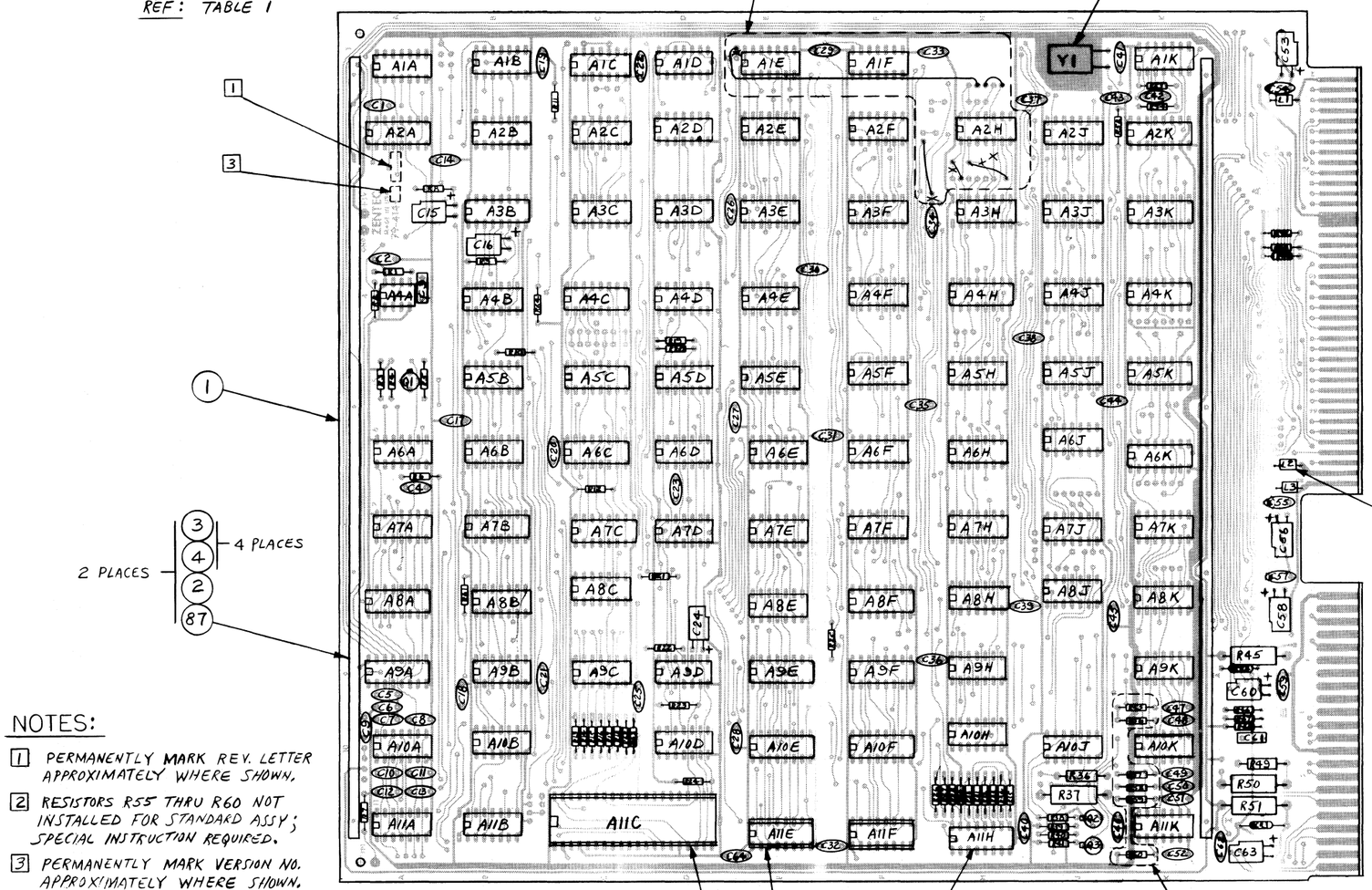
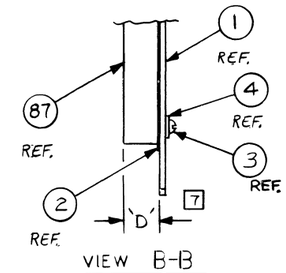


TABLE 1
SELECTABLE BAUD RATE SWITCH CONFIGURATION

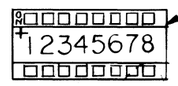
'SEL' BAUD RATE	SWITCH LOC. A11H S1	S2
2400	OFF	OFF
4800	ON	OFF
9600	OFF	ON

[4]



VIEW B-B
SCALE 1:1

A DEPRESSED BUTTON ON THIS SIDE OF DIP SWITCH INDICATES AN "ON" STATE



DETAIL A

SEE TABLE 1 FOR SPECIFIC SWITCH CONFIGURATION

NOTES:

1. PERMANENTLY MARK REV. LETTER APPROXIMATELY WHERE SHOWN.
2. RESISTORS R55 THRU R60 NOT INSTALLED FOR STANDARD ASSY; SPECIAL INSTRUCTION REQUIRED.
3. PERMANENTLY MARK VERSION NO. APPROXIMATELY WHERE SHOWN.
   -04 60 HZ, 24 ROWS (PLUS CONTROL ROW)
   -05 50 HZ, 24 ROWS (PLUS CONTROL ROW)
   -06 MODEL T2201 SPECIAL.
4. 9600 BAUD CAN ALSO BE SELECTED BY SETTING SWITCHES S1 "ON" & S2 "ON".
5. AN I.D. WORD, INDICATING THE 'SEL' BAUD RATE SETTING AND THE UNIT I.D. NUMBER (SET BY SWITCHES - A11H), IS PROVIDED TO THE CPU VIA INPUT PORT X'45' WITH AN 8008 CPU, THE ACCUMULATOR MUST BE SET TO X'40'.
6. LAST REFERENCE DESIGNATIONS USED ARE: C64, CR3, L3, Q3, R64 & Y1. REF. DESIG. CR1 IS NOT USED.
7. MAXIMUM HEIGHT 'D' OF ANY COMPONENT ABOVE SURFACE OF P.C. BOARD SHALL BE 0.400 INCHES.

APPLICATION	
NEXT ASSY	USED ON
01-417-XX	9002 A/B
01-417-XX	9003
07-422-XX	T2201
01-404-XX	9002
01-404-XX	9002A/B
SEE STATUS FILE	

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN IN

ANG	2 PLC	3 PLC	—
± —	± —	± —	± —

SCALE: 1:1
MATERIAL: SEE BILL OF MAT'L
FINISH: —

DWN R.P. Johnson 9-1-76
CHK [illegible] 9-9-76
ENGR [illegible] 9/9/76
APPD [illegible] 9/11/76
APPD [illegible] 9/17/76
APPD

ENGR CHANGES				
REV	CHG NO.	DATE	APPD	
D	SEE STATUS	9/30/76	[illegible]	

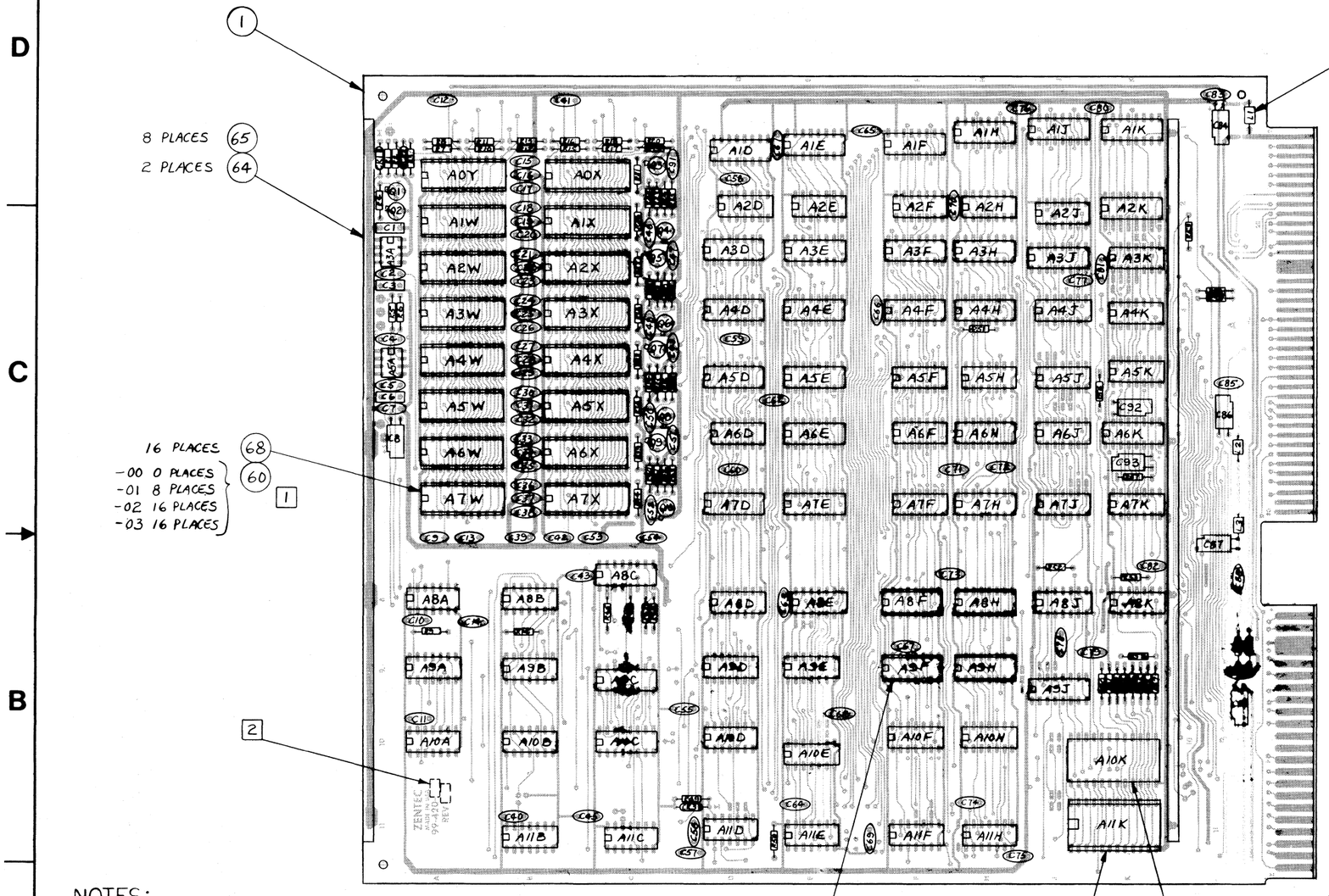
DO NOT SCALE DRAWING

ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA

TITLE: P.C. ASSEMBLY, SYSTEM TIMING

SIZE C | SHT 1 OF 1 | DRAWING NO. 99-414-XX | REV D

FORM NO. 75-000-08

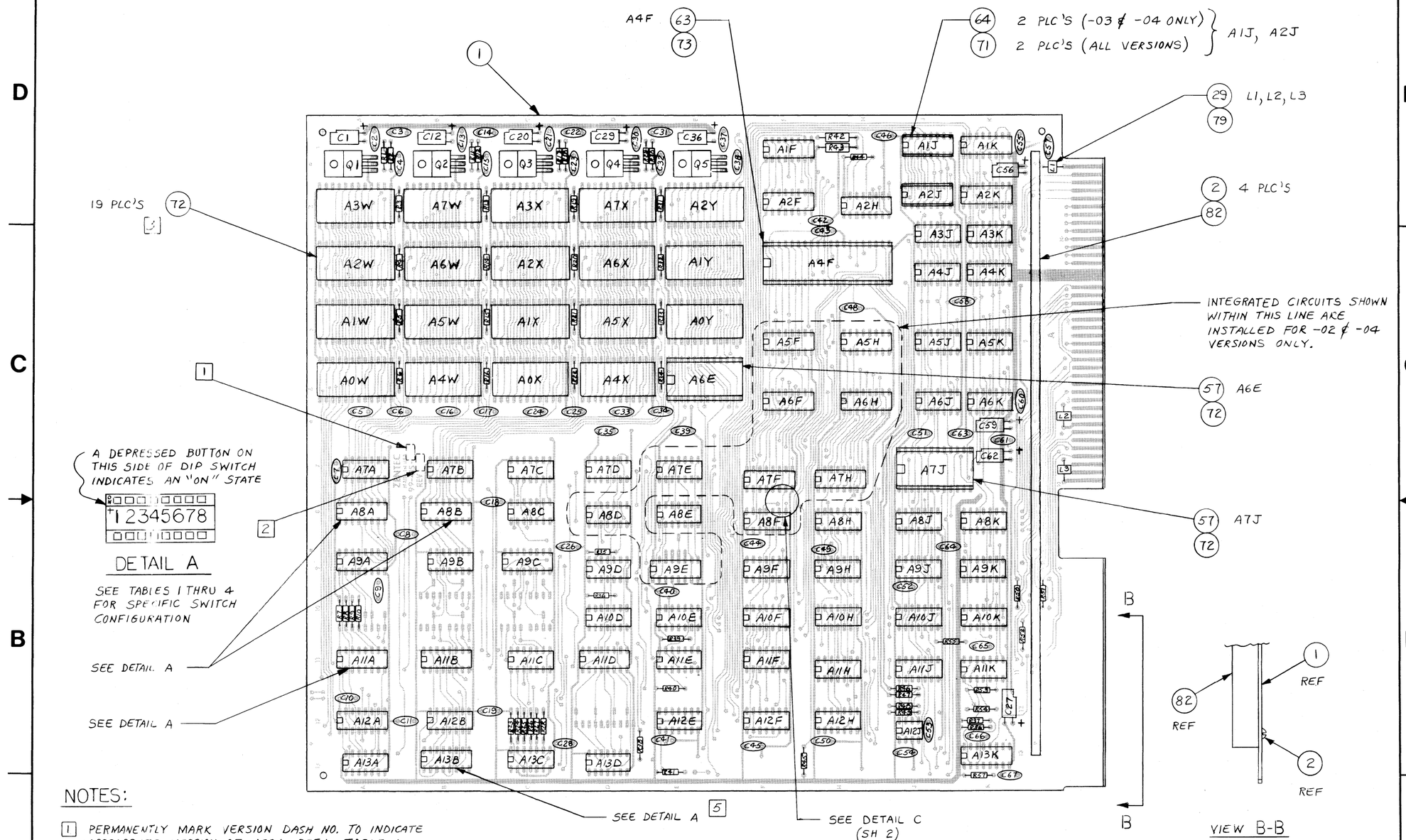


NOTES:

1. VERSION DEFINES QTY OF RAM
   - -00 = NO RAM, NO ITEM 60
   - -01 = 2K BYTES OF RAM, A0W THRU A7W
   - -02 = 4K BYTES OF RAM, A0W THRU A7W AND A0X THRU A7X
   - -03 = MODEL T2201 SPECIAL (4K BYTES OF RAM)
2. PERMANENTLY MARK VERSION NUMBER & REV. LETTER WHERE SHOWN.
3. LAST REF. DESIG. USED ARE: C93, CR4, L3, Q10, R68
   REF. DESIG. C44 NOT USED.

APPLICATION		UNLESS OTHERWISE NOTED				DWN R.T. Hyman 10-21-75	ENGR CHANGES				ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA
NEXT ASSY	USED ON	DIMENSIONS ARE IN IN.				CHK	REV	CHG NO.	DATE	APPD	TITLE P.C. ASSEMBLY, CHARACTER REFRESH
07-422-XX	T2201	ANG ± —	2 PLC ± —	3 PLC ± —	— ± —	ENGR	B	NEW ARTWORK	11/24/75		
		SCALE: 1:1				APPD					
		MATERIAL SEE BILL OF MAT'L				APPD					SIZE C SHT 1 OF 1 DRAWING NO. 99-420-XX REV B
						APPD					
						FINISH —					DO NOT SCALE DRAWING

FORM NO. 75-000-08



NOTES:

1. PERMANENTLY MARK VERSION DASH NO. TO INDICATE APPROPRIATE VERSION OF ASSY. REF: TABLE 1.
2. PERMANENTLY MARK REV. LETTER APPROXIMATELY WHERE SHOWN.
3. FOR QUANTITY AND LOCATION OF ROM AND PROM INTEGRATED CIRCUITS, REFER TO SPECIFIC FIRMWARE CONFIGURATION DRAWING. (DOCUMENT CATEGORY 10-XXX-XX.)

NOTES CONTINUED SHEET 2 —

APPLICATION	
NEXT ASSY	USED ON
07-419-XX	9003
27-010-01	KDS 7810 M
24-019-XX	9003
07-422-XX	T2201

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN IN
ANG ± — | 2 PLC ± — | 3 PLC ± — | — ± —
SCALE: 1:1
MATERIAL: SEE BILL OF MAT'L
FINISH: —

DWN R. Nelson 12-18-75
CHK D. Schmidt 12/19/75
ENGR [illegible] 12/19/75
APPD [illegible] 12/19/75
APPD [illegible] 12/19/75
APPD [illegible] 12/19/75

ENGR CHANGES			
REV	CHG NO.	DATE	APPD
C	NEW ARTWORK	12/19/75	[illegible]

DO NOT SCALE DRAWING

ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA

TITLE: P.C. ASSEMBLY, MICROPROCESSOR — 8080

SIZE C | SHT 1 OF 2 | DRAWING NO. 99-415-XX | REV C

FORM NO. 75-000-08

TABLE 1
VERSION TABLE

VERSION DASH NO.	DESCRIPTION	STACK ENABLE SWITCH LOCATION A13B SWITCH 8 [5]
-01	MICROPROCESSOR ONLY	SWITCH MUST BE IN "OFF" POSITION
-02	MICROPROCESSOR W/TIMER CIRCUIT ONLY	
-03	MICROPROCESSOR W/ON-BOARD STACK ONLY	SET SWITCH AS FOLLOWS: "ON" TO ENABLE STACK "OFF" TO DISABLE STACK
-04	MICROPROCESSOR W/BOTH TIMER & STACK	

TABLE 2
PROM ENABLE

PROM LOCATION	SWITCH LOCATION	SWITCH NUMBER	SWITCH POSITION ENABLE	SWITCH POSITION DISABLE
A0W	A8A	1	ON	OFF
A1W		2	↑	↑
A2W		3		
A3W		4		
A4W		5		
A5W		6		
A6W		7		
A7W		8		
A0X	A8B	1		
A1X		2		
A2X		3		
A3X		4		
A4X		5		
A5X		6		
A6X		7	↓	↓
A7X		8	ON	OFF

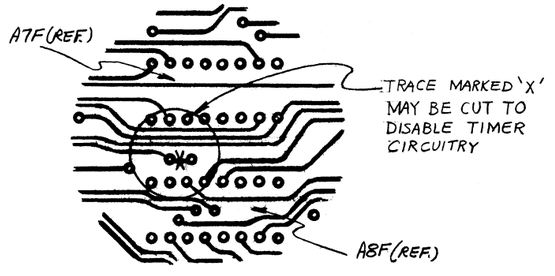
TABLE 3
PROM BLOCK ADDRESS ENABLE

PROM LOCATION	BLOCK ADDRESS (HEXADECIMAL)	SWITCH LOCATION A11A SWITCH NO. 1	SWITCH NO. 2
A0W - A3W	DISABLED	OFF	OFF
	'0000' - '03FF'	ON	OFF
	'F000' - 'F3FF'	OFF	ON
	SWITCH COMBINATION DISALLOWED	ON	ON
		SWITCH NO. 3	SWITCH NO. 4
A4W - A7W	DISABLED	OFF	OFF
	'0400' - '07FF'	ON	OFF
	'F400' - 'F7FF'	OFF	ON
	SWITCH COMBINATION DISALLOWED	ON	ON
		SWITCH NO. 5	SWITCH NO. 6
A0X - A3X	DISABLED	OFF	OFF
	'0800' - '0BFF'	ON	OFF
	'F800' - 'FBFF'	OFF	ON
	SWITCH COMBINATION DISALLOWED	ON	ON
		SWITCH NO. 7	SWITCH NO. 8
A4X - A7X	DISABLED	OFF	OFF
	'C000' - '0FFF'	ON	OFF
	'FC00' - 'FFFF'	OFF	ON
	SWITCH COMBINATION DISALLOWED	ON	ON

NOTES: (CON'T.)

4. THE LAST REF. DESIGNATIONS USED ARE AS FOLLOWS: CAPACITORS - C67, INDUCTORS - L3, TRANSISTORS - Q5, RESISTORS - R57. REF. DESIG. C47, NOT USED.

[5] SWITCH 7 AT LOCATION A13B IS NOT USED.



DETAIL C

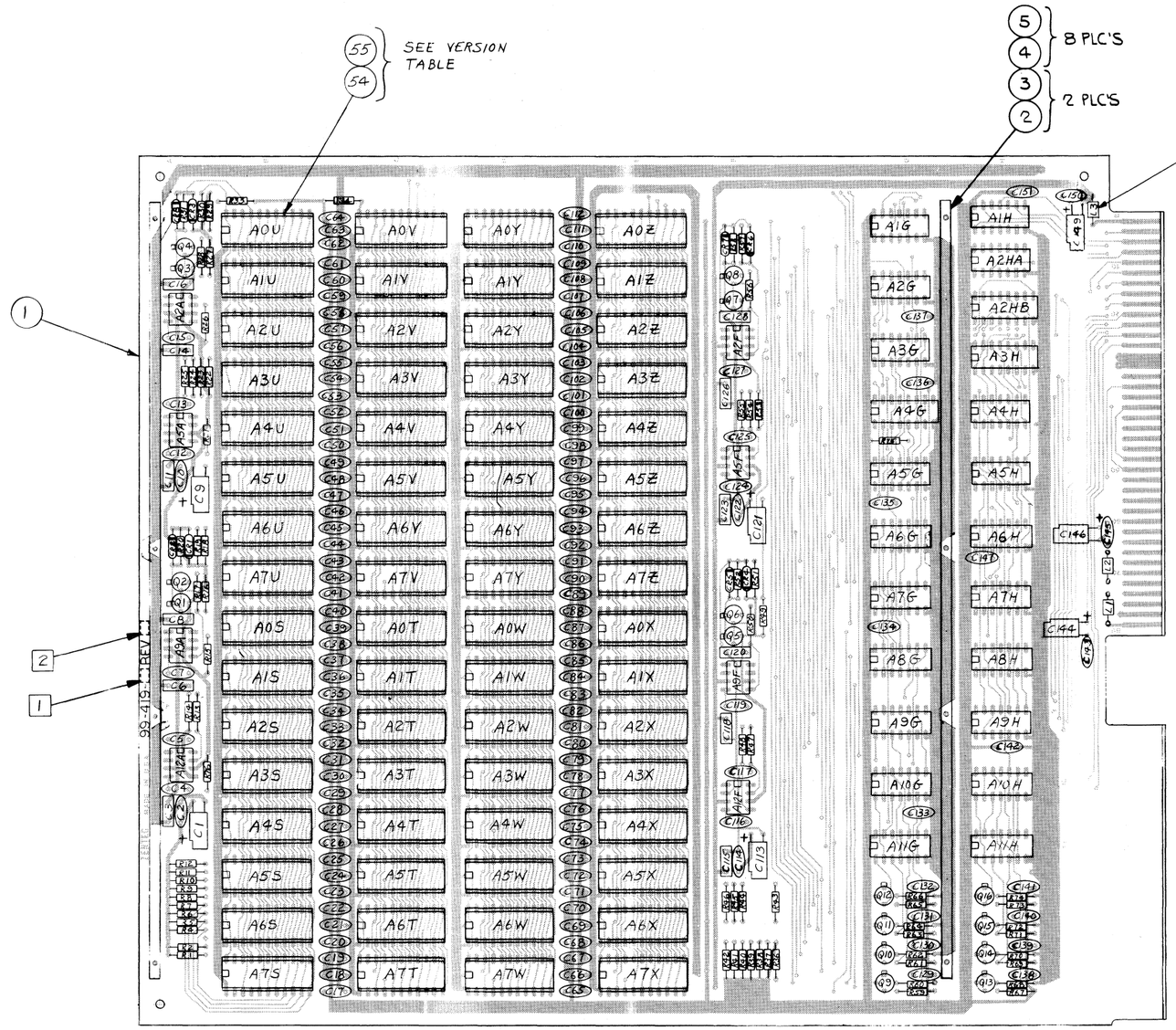
SOLDER SIDE
SCALE 2:1

TABLE 4
ROM BLOCK ADDRESS ENABLE

ROM LOCATION	BLOCK ADDRESS (HEXADECIMAL)	SWITCH LOCATION A13B [5] 1	2	3	4	5	6
A0Y	DISABLED	OFF	—	—	—	—	—
	'0000' - '07FF'	ON	—	—	—	—	—
A1Y	DISABLED	—	OFF	—	—	—	—
	'0800' - '0FFF'	—	ON	—	—	—	—
A2Y	DISABLED	—	—	OFF	OFF	OFF	OFF
	'E000' - 'E7FF'	—	—	ON	OFF	ON	OFF
	'E800' - 'EFFF'	—	—	OFF	ON	OFF	ON
	SWITCH COMBINATION DISALLOWED	—	—	ALL OTHER COMBINATIONS			

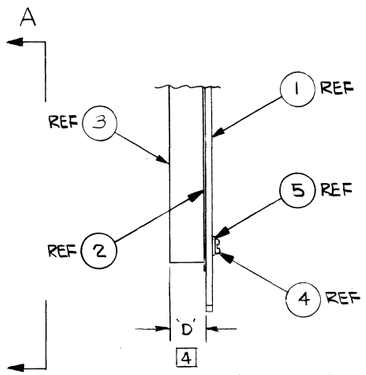
APPLICATION		UNLESS OTHERWISE NOTED		DWN	ENGR CHANGES				ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA
NEXT ASSY	USED ON	DIMENSIONS ARE IN —		CHK	REV	CHG NO.	DATE	APPD	TITLE P.C. ASSEMBLY, MICROPROCESSOR-8080
		ANG	2 PLC 3 PLC —	ENGR					
		± —	± — ± — ± —	APPD					
		SCALE: —		APPD					SIZE C SHT 2 OF 2 DRAWING NO. 99-415-XX REV C
		MATERIAL —		FINISH —	DO NOT SCALE DRAWING				

FORM NO. 75-000-08



VERSION TABLE

DASH NO.	QTY OF RAM	LOCATION
-00	64 SOCKETS ONLY/NO RAM	ALL RAM LOCATIONS
-01	16	A0S-A7S & A0T-A7T
-02	32	SAME AS -01 PLUS A0U-A7U & A0V-A7V
-03	48	SAME AS -02 PLUS A0W-A7W & A0X-A7X
-04	64	ALL RAM LOCATIONS



VIEW A-A
SCALE 1:1
(COMPONENTS NOT SHOWN FOR CLARITY)

NOTES:

1. PERMANENTLY MARK VERSION (DASH NO.) APPROXIMATELY WHERE SHOWN — SEE VERSION TABLE.
2. PERMANENTLY MARK REV. LETTER APPROXIMATELY WHERE SHOWN.
3. REFERENCE DESIGNATIONS R3, R32, R35 & C148 ARE NOT USED. LAST REF. DESIG. USED ARE C151, CR8, L3 Q16 & R76.
4. MAXIMUM HEIGHT ('D') OF ANY COMPONENT ABOVE COMPONENT-SIDE SURFACE OF P.C. BOARD SHALL BE 0.400 INCHES.
5. FOR INSTRUCTIONS TO MODIFY RAM BLOCK ADDRESSES, REFER TO 16K RAM ADDRESSING INSTRUCTION (ITEM 16).

APPLICATION	
NEXT ASSY	USED ON
02-405-XX	9003

UNLESS OTHERWISE NOTED DIMENSIONS ARE IN —
ANG ± — | 2 PLC ± — | 3 PLC ± —
SCALE: 1:1
MATERIAL: SEE BILL OF MAT'L

DWN R. Nakamura 1-29-76
CHK 3/5/76
ENGR 2/26/76
APPD 3/1/76
APPD 2/26/76
APPD 3/23/76
FINISH —

ENGR CHANGES			
REV	CHG NO.	DATE	APPD
B	NEW ARTWORK	3/23/76	
C	NEW ARTWORK	10/1/76	

DO NOT SCALE DRAWING

ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA

TITLE: P.C. ASSEMBLY, 16K RAM

SIZE C | SHT 1 OF 1 | DRAWING NO. 99-419-XX | REV C

FORM NO. 75-000-08

ITEM/ FIND NO.	QTY PER ASSY					UNIT OF MEAS	KEY(1)	KEY (2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REMARKS
			06	05	04						
1			1	1	1	01	D		98-414-03	P.C. BOARD, SYSTEM TIMING	
2			2	2	2	01	D		51-005-01	SPACER, INSULATING	
3			8	8	8	01	D		80-100-30	SCREW, SLOTTED, PAN HEAD, STAINLESS STEEL, 2-56 X 1/4	
4			8	8	8	01	D		80-154-10	WASHER, FLAT, NYLON, # 2	
5			2	2	2	01	D		80-202-39	RESISTOR, CARBON COMP., 100Ω, 5%, 1/4 W	R5, R46
6			1	1	1	↓	↓		80-202-51	330Ω	R3
7			4	4	4				80-202-55	470Ω	R4, R53, R54, R64
8			36	36	36				80-202-63	1KΩ	R6, R7, R10-R21, R23-R35, R38
9											R39, R42-R49, R52, R61, R62, R63
10			1	1	1				80-202-73	2.7KΩ	R47
11			2	2	2	↓	↓		80-202-84	7.5KΩ	R41, R48
12			4	4	4	01	D		80-202-87	RESISTOR, CARBON COMP., 10KΩ 5%, 1/4W	R1, R2, R22, R40
13											
14											
15			2	2	2	01	D		80-203-04	RESISTOR, CARBON COMP. 47KΩ, 5%, 1/4W	R8, R9
16											
17			2	2	2	01	D		80-204-56	RESISTOR, CARBON COMP., 510Ω 5%, 1/2W	R36, R49
18											
19											

NOTES:
1. VERSION - 04 60 Hz, 24 ROW (PLUS CONTROL ROW)
-05 50 Hz, 24 ROW (PLUS CONTROL ROW)
-06 MODEL T2201 SPECIAL.
2. RESISTORS R55-R60 ARE NOT INSTALLED FOR STANDARD ASSY; SPECIAL INSTRUCTION IS REQ'D.

APPLICATION	
NEXT ASSY	USED ON
01-417-XX	9002 A/B
01-417-XX	9003
07-422-XX	T2201
01-404-XX	9002
01-404-XX	9002 A/B
SEE STATUS CARD	

UNIT OF MEASURE:
01-EACH 04-BULK
02-INCH 05-AS REQ'D
03-FEET 09-OTHER (see notes)

KEY 1:
A-WITH B/M
D-WITHOUT B/M
R-REFERENCE
S-SPECIFICATION
O-OTHER (see notes)

DWN R. Nakamura 1/21/75
CHK [illegible] 1/22/75
ENGR L. Lowenbach 1/29/75
APPD [illegible] 2/18/76
APPD [illegible] 1/27/75
APPD [illegible] 2/4/75
KEY 2:

ENGR CHANGES			
REV	CHG NO.	DATE	APPD
B	SEE STATUS	6/4/75	[illegible]
C	SEE STATUS	11/26/75	[illegible]
D	SEE STATUS	9/30/76	[illegible]

ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA

TITLE P.C. ASSEMBLY, SYSTEM TIMING

SIZE	SHT	OF	BILL OF MAT'L NO.	REV
A	1	5	99-414-XX	D

FORM NO. 75-000-03

ITEM/ FIND NO.	QTY PER ASSY					UNIT OF MEAS	KEY(1)	KEY (2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REMARKS
			06	05	04						
20			2	2	2	01	D		80-206-37	RESISTOR, CARBON COMP., 82Ω, 5%, 1W	R45, R51
21			2	2	2	01	D		80-206-49	RESISTOR, CARBON COMP., 270Ω, 5%, 1W	R37, R50
22											
23			2	2	2	01	D		80-310-61	CAPACITOR, TANTALUM, 33μf, 20%, 10V.	C15, C16
24											
25			6	6	6	01	D		80-311-73	CAPACITOR, TANTALUM, 10μf, 20%, 25V.	C24, C53, C56, C58, C60, C63
26											
27			44	44	44	01	D		80-331-08	CAPACITOR, CERAMIC, .01μf, 20%, 50V.	C1, C2, C4-C6, C9, C12-C14
28											C17-C23, C25-C46, C54, C55
29											C57, C59, C62, C64
30			10	10	10	01	D		80-339-30	CAPACITOR, CERAMIC, 470 pf, 20%, 1KV	C7, C8, C10, C11, C47-C52
31											
32			2	2	2	01	D		80-345-49	CAPACITOR, CERAMIC, .1μf, 10%, 50V.	C3, C61
33											
34			3	3	3	01	D		80-430-01	SHIELDING BEAD	L1, L2, L3
35											
36											
37											
38			1	1	1	01	D		80-510-02	DIODE, ZENER, IN5239B	CR2

NOTES: 3. LAST REFERENCE DESIGNATIONS USED ARE: C64, CR3, L3, Q3, R64, & Y1. REF. DESIG. CR1 IS NOT USED.

APPLICATION	
NEXT ASSY	USED ON

UNIT OF MEASURE:
01-EACH 04-BULK
02-INCH 05-AS REQ'D
03-FEET 09-OTHER (see notes)

KEY 1:
A-WITH B/M
D-WITHOUT B/M
R-REFERENCE
S-SPECIFICATION
O-OTHER (see notes)

DWN R. Nakamura 1/21/75
CHK D. Reed 1/22/75
ENGR
APPD
APPD
APPD
KEY 2:

ENGR CHANGES			
REV	CHG NO.	DATE	APPD

ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA

TITLE
P. C. ASSEMBLY, SYSTEM TIMING

SIZE	SHT 2 OF 5	BILL OF MAT'L NO.	REV
A		99-414-XX	D

FORM NO. 75-000-03

ITEM/ FIND NO.	QTY PER ASSY		06	05	04	UNIT OF MEAS	KEY(1)	KEY (2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE / DESCRIPTION	REMARKS
39			1	1	1	01	D		80-510-03	DIODE, ZENER, IN5349B	CR3
40											
41			4	4	4	01	D		80-550-00	INTEGRATED CIRCUIT, 7400	A6A, A7E, A8K, A10B
42			5	5	5	↑	↑		80-550-02	↑ ↑ 7402	A1B, A2B, A6J, A7A, A8C
43			3	3	3				80-550-27	7438	A4B, A5E, A6E
44			9	9	9				80-550-04	7404	A1A, A3J, A5D, A5H, A7F, A8H,
45											A9K, A10J, A11A
46			3	3	3				80-550-14	7416	A9C, A9H, A10H
47			10	10	10				80-550-08	7408	A2H, A2J, A3E, A4F, A5B, A6H,
48											A7J, A7K, A8E, A10D
49			1	1	1				80-550-10	7410	A6B
50			2	2	2				80-550-24	7432	A2E, A8J
51			3	3	3				80-550-26	7437	A1F, A2D, A3D
52			5	5	5				80-550-29	7442A	A2A, A6K, A7B, A8A, A9A
53			3	3	3				80-550-38	7451	A2F, A4D, A7D
54			7	7	7				80-550-45	7474	A1D, A1E, A4J, A7H, A8B, A9B,
55											A9D
56			1	1	1	↓	↓		80-550-55	↓ ↓ 7486	A3F
57			3	3	3	01	D		80-550-61	INTEGRATED CIRCUIT, 7493A	A5F, A5J, A6F

NOTES:

APPLICATION	
NEXT ASSY	USED ON

UNIT OF MEASURE:
01-EACH 04-BULK
02-INCH 05-AS REQ'D
03-FEET 09-OTHER (see notes)

KEY 1:
A-WITH B/M
D-WITHOUT B/M
R-REFERENCE
S-SPECIFICATION
O-OTHER (see notes)

DWN R. Nakamura 1/21/75
CHK D. Roland 1/22/75
ENGR
APPD
APPD
APPD
KEY 2:

ENGR CHANGES			
REV	CHG NO.	DATE	APPD

ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA

TITLE
P.C. ASSEMBLY, SYSTEM TIMING

SIZE	SHT 3 OF 5	BILL OF MAT'L NO.	REV
A		99-414-XX	D

FORM NO. 75-000-03

ITEM/ FIND NO.	QTY PER ASSY					UNIT OF MEAS	KEY(1)	KEY (2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REMARKS
			06	05	04						
58			5	5	5	01	D		80-550-67	INTEGRATED CIRCUIT, 74107	A1C, A2C, A3C, A4E, A6D
59			1	1	1	↕	↕		80-550-75	↕ ↕ 74123	A3B
60			4	4	4				80-550-90	74153	A9E, A9F, A10E, A10F
61			1	1	1	↕	↕		80-550-96	↕ ↕ 74160 (ALT 9310)	A2K
62			9	9	9	01	D		80-550-97	INTEGRATED CIRCUIT, 74161 (ALT 9316)	A3H, A3K, A4C, A4H, A4K
63											A5C, A5K, A6C, A7C
64											
65			2	2	2	01	D		80-551-07	INTEGRATED CIRCUIT, 74174	A8F, A11B
66											
67			1	1	1	01	D		80-554-34	INTEGRATED CIRCUIT, 74S04	A1K
68											
69			1	1	1	01	D		80-560-10	INTEGRATED CIRCUIT, 1488	A10A
70			2	2	2	↕	↕		80-560-11	↕ ↕ 1489A	A10K, A11K
71			1	1	1				80-560-12	↕ ↕ TR1602A UART	A11C
72			2	2	2				80-560-13	INTEGRATED CIRCUIT, 3341	A11E, A11F
73											
74			1	1	1				80-580-02	INTEGRATED CIRCUIT, SE555V	A4A
75			1	–	1	↕	↕		80-590-09	CRYSTAL (OSCILLATOR) 15.1488 MHz	Y1 (60 Hz)
76			–	1	–	01	D		80-590-08	CRYSTAL (OSCILLATOR) 15.0720 MHz	Y1 (50 Hz)

NOTES:

APPLICATION	
NEXT ASSY	USED ON

UNIT OF MEASURE:
01-EACH 04-BULK
02-INCH 05-AS REQ'D
03-FEET 09-OTHER (see notes)

KEY 1:
A-WITH B/M
D-WITHOUT B/M
R-REFERENCE
S-SPECIFICATION
O-OTHER (see notes)

DWN	R. Nakamura 1/21/75
CHK	R. Rohm 1/22/75
ENGR	
APPD	
APPD	
APPD	
KEY 2:	

ENGR CHANGES			
REV	CHG NO.	DATE	APPD

ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA

TITLE
P.C. ASSEMBLY, SYSTEM TIMING

SIZE	SHT	OF	BILL OF MAT'L NO.	REV
A	4	5	99-414-XX	D

FORM NO. 75-000-03

ITEM/ FIND NO.	QTY PER ASSY					UNIT OF MEAS	KEY(1)	KEY (2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REMARKS
			06	05	04						
77			1	1	1	01	D		80-520-01	TRANSISTOR, NPN, 2N2222A	Q3
78											
79			2	2	2	01	D		80-530-01	TRANSISTOR, PNP, 2N2906A	Q1, Q2
80			1	1	1	01	D		80-680-04	SWITCH, DIP, 16 PIN	A11H
81			A/R	A/R	A/R	01	D		80-680-01	SWITCH, DIP, 16 PIN	A11H ALTERNATE
82			2	2	2	01	D		80-700-02	SOCKET, I.C., 16 PIN	REF: A11E, A11F
83			1	1	1	01	D		80-700-08	SOCKET, I.C. 40 PIN.	REF: A11C
84			–	6	–	02	D		80-810-01	WIRE, SOLID, INSULATED, 30AWG	
85			3	5	3	02	D		80-870-07	WIRE, BUSS, TINNED COPPER, 18 AWG	
86											
87			2	2	2	01	D		39-002-01	STIFFENER, P.C. BOARD, AL	
88											
89			1	1	1	05	R		96-414-03	LOGIC DIAGRAM, SYSTEM TIMING	
90											
91			1	–	–	01	A		27-017-01	MODEL T2201 DISPLAY FORMAT MODIFICATION	
92											
93											
94											
95											

NOTES:

APPLICATION	
NEXT ASSY	USED ON

UNIT OF MEASURE:

01-EACH	04-BULK
02-INCH	05-AS REQ'D
03-FEET	09-OTHER (see notes)

KEY 1:
A-WITH B/M
D-WITHOUT B/M
R-REFERENCE
S-SPECIFICATION
O-OTHER (see notes)

DWN	R. Nakamura 1/21/75
CHK	1/22/75
ENGR	
APPD	
APPD	
APPD	
KEY 2:	

ENGR CHANGES			
REV	CHG NO.	DATE	APPD

ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA

TITLE
P.C. ASSEMBLY, SYSTEM TIMING

SIZE	SHT	OF	BILL OF MAT'L NO.	REV
A	5	5	99-414-XX	D

FORM NO. 75-000-03

ITEM/ FIND NO.	QTY PER ASSY 03	02	01	00	UNIT OF MEAS	KEY(1)	KEY (2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REMARKS
1	1	1	1	1	01	D		98-420-01	P.C. BOARD, CHARACTER REFRESH	
2										
3	2	2	2	2	01	D		80-310-61	CAPACITOR, TANTALUM, 33µf, 20%, 10V.	C8, C92
4	5	5	5	5	01	D		80-311-73	CAPACITOR, TANTALUM, 10µf, 20%, 25V	C84, C86, C87, C90, C93
5	77	77	77	77	01	D		80-331-08	CAPACITOR, CERAMIC, .01µf, 20%, 50V.	C7, C9-C43, C45-C55,
6										C57-C81, C83, C85, C88
7										C89, C91
8	1	1	1	1	01	D		80-338-04	CAPACITOR, CERAMIC, 15pf, 10%, 1KV	C56
9	4	4	4	4	01	D		80-339-30	CAPACITOR, CERAMIC, 470pfd, 20% 1KV	C2, C4, C5, C82
10	3	3	3	3	01	D		80-345-49	CAPACITOR, CERAMIC, .1µf, 10%, 50V.	C1, C3, C6
11	3	3	3	3	01	D		80-430-01	SHIELDING BEAD	L1, L2, L3
12										
13	3	3	3	3	01	D		80-500-02	DIODE, IN914B	CR1, CR2, CR3
14	A/R	A/R	A/R	A/R	01	D		80-500-04	DIODE, IN4448	CR1-3 ALTERNATE
15	1	1	1	1	01	D		80-510-06	DIODE, ZENER, IN5225B	CR4
16										
17	1	1	1	1	01	D		80-520-01	TRANSISTOR, NPN, 2N2222A	Q2
18	8	8	8	8	01	D		80-520-02	TRANSISTOR, NPN, 2N2369A	Q3-Q10
19	1	1	1	1	01	D		80-530-01	TRANSISTOR, PNP, 2N2906A	Q1

NOTES: [1] VERSION DEFINES QTY OF RAM: -00 = NO RAM, NO ITEM 60; -01 = 2K BYTES OF RAM, A0W THRU A7W; -02 = 4K BYTES OF RAM A0W THRU A7W AND A0X THRU A7X; -03 = MODEL T2201 SPECIAL (4K BYTES OF RAM).

APPLICATION	
NEXT ASSY	USED ON
07-422-XX	T2201

UNIT OF MEASURE:
01-EACH 04-BULK
02-INCH 05-AS REQ'D
03-FEET 09-OTHER (see notes)

KEY 1:
A-WITH B/M
D-WITHOUT B/M
R-REFERENCE
S-SPECIFICATION
O-OTHER (see notes)

DWN C. Nathanson 8-26-75
CHK Bill Grace 9/16/75
ENGR T. Fourchalk 9/16/75
APPD R. Clough 9/16/75
APPD [illegible] 9/19/75
APPD Bill Grace 9/16/75

KEY 2:

ENGR CHANGES			
REV	CHG NO.	DATE	APPD
B	NEW ARTWORK	11/24/75	[illegible]

ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA

TITLE
P.C. ASSEMBLY CHARACTER REFRESH

SIZE	SHT	OF	BILL OF MAT'L NO.	REV
A	1	4	99-420-XX	B

FORM NO. 75-000-03

ITEM/ FIND NO.	QTY PER ASSY				UNIT OF MEAS	KEY(1)	KEY (2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE / DESCRIPTION	REMARKS
	03	02	01	00						
20	4	4	4	4	01	D		80-202-25	RESISTOR, CARBON COMP, 27 Ω, 5%, 1/4	R1, R4, R5, R6
21	4	4	4	4	01	D		80-202-45	RESISTOR, CARBON COMP, 180 Ω, 5%, 1/4W	R45-R48
22	22	22	22	22	01	D		80-202-55	RESISTOR, CARBON COMP, 470 Ω, 5%, 1/4W	R2, R3, R7, R8, R10, R11-R13,
23										R15-R21, R26, R27, R32, R33
24										R38, R39, R44
25	19	19	19	19	01	D		80-202-63	RESISTOR, CARBON COMP, 1K Ω, 5%, 1/4W	R9, R14, R49, R50, R51-R55
26										R58, R59, R60-R67
27	16	16	16	16	01	D		80-202-65	RESISTOR, CARBON COMP, 1.2K Ω, 5%, 1/4W	R22-R25, R28-R31,
28										R34-R37, R40-R43
29	1	1	1	1	01	D		80-202-87	RESISTOR, CARBON COMP, 10K Ω, 5%, 1/4W	R57
30	2	2	2	2	01	D		80-203-04	RESISTOR, CARBON COMP, 47K Ω, 5%, 1/4W	R56, R68
31										
32	1	1	1	1	01	D		80-550-13	INTEGRATED CIRCUIT, 7414	A9E
33	2	2	2	2	01	D		80-550-00	INTEGRATED CIRCUIT, 7400	A5J, A9D
34	4	4	4	4	01	D		80-550-02	7402	A2J, A6D, A7J, A11F
35	8	8	8	8	01	D		80-550-04	7404	A2F, A2H, A3K, A5H, A6F,
36										A10A, A10F, A10H
37	6	6	6	6	01	D		80-550-08	7408	A4K, A7F, A7K, A11B, A11C, A11E
38	1	1	1	1	01	D		80-550-10	INTEGRATED CIRCUIT, 7410	A5K

NOTES: 2 LAST REFERENCE DESIGNATIONS USED ARE: C93, CR4, L3, Q10, R68. REF. DESIG. C44 IS NOT USED

APPLICATION	
NEXT ASSY	USED ON

UNIT OF MEASURE:
01-EACH 04-BULK
02-INCH 05-AS REQ'D
03-FEET 09-OTHER (see notes)

KEY 1:
A-WITH B/M
D-WITHOUT B/M
R-REFERENCE
S-SPECIFICATION
O-OTHER (see notes)

DWN R. Nakamura 8-27-75
CHK [illegible] 9/16/75
ENGR
APPD
APPD
APPD
KEY 2:

ENGR CHANGES			
REV	CHG NO.	DATE	APPD

ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA

TITLE
P.C. ASSEMBLY
CHARACTER REFRESH

SIZE	SHT 2 OF 4	BILL OF MAT'L NO.	REV
A		99-420-XX	B

FORM NO. 75-000-03

ITEM/ FIND NO.	QTY PER ASSY 03	02	01	00	UNIT OF MEAS	KEY(1)	KEY(2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REMARKS
39	3	3	3	3	01	D		80-550-24	INTEGRATED CIRCUIT, 7432	A4J, A8J, A11D
40	2	2	2	2	01	D		80-550-27	7438	A2D, A2E
41	2	2	2	2	01	D		80-550-29	7442A	A2K, A7H
42	3	3	3	3	01	D		80-550-38	7451	A8B, A8D, A10B
43	3	3	3	3	01	D		80-550-45	7474	A5F, A9A, A9B
44	2	2	2	2	01	D		80-550-52	7483A	A4F, A4H
45	3	3	3	3	01	D		80-550-54	7485	A5E, A6E, A11H
46	1	1	1	1	01	D		80-550-55	7486	A10E
47	3	3	3	3	01	D		80-550-67	74107	A6J, A8E, A8K
48	1	1	1	1	01	D		80-550-75	74123	A6K
49	1	1	1	1	01	D		80-550-78	74128	A10D
50	6	6	6	6	01	D		80-550-94	74157 (ALT 9322)	A1D, A1E, A1F, A1H, A1J, A1K
51	4	4	4	4	01	D		80-550-97	74161 (ALT 9316)	A4D, A5D, A7D, A7E
52	4	4	4	4	01	D		80-550-99	74163	A3F, A3H, A3J, A6H
53	1	1	1	1	01	D		80-551-02	74166	A9J
54	2	2	2	2	01	D		80-551-07	74174	A4E, A8C
55	2	2	2	2	01	D		80-551-08	74175	A3D, A3E
56	2	2	2	2	01	D		80-551-40	74298	A9C, A10C
57	1	1	1	1	01	D		80-554-05	INTEGRATED CIRCUIT, 74H11	A8A

NOTES:

APPLICATION	
NEXT ASSY	USED ON

UNIT OF MEASURE:
01-EACH 04-BULK
02-INCH 05-AS REQ'D
03-FEET 09-OTHER (see notes)

KEY 1:
A-WITH B/M
D-WITHOUT B/M
R-REFERENCE
S-SPECIFICATION
O-OTHER (see notes)

DWN R. Nyhammer 8-27-75
CHK [illegible] 9/10/75
ENGR
APPD
APPD
APPD
KEY 2:

ENGR CHANGES			
REV	CHG NO.	DATE	APPD

ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA

TITLE
P. C. ASSEMBLY
CHARACTER REFRESH

SIZE	SHT	OF	BILL OF MAT'L NO.	REV
A	3	4	99-420-XX	B

FORM NO. 75-000-03

ITEM/ FIND NO.	QTY PER ASSY 03	02	01	00	UNIT OF MEAS	KEY(1)	KEY (2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REMARKS
58	2	2	2	2	01	D		80-560-01	INTEGRATED CIRCUIT, MH0026	A3A, A5A
59	4	4	4	4	01	D		80-560-02	INTEGRATED CIRCUIT, 3347	A8F, A8H, A9F, A9H
60	16	16	8	0	01	D		80-560-09	INTEGRATED CIRCUIT, RAM, MM5262	SEE NOTE [1]
61	A/R	A/R	A/R	0	01	D		80-560-06	INTEGRATED CIRCUIT, RAM, 600314	ALTERNATE ITEM 60
62	1	1	1	1	01	D		23-025-01	CHARACTER GENERATOR (ROM)	A11K
63										
64	2	2	2	2	01	D		40-002-01	STIFFENER, P.C. BOARD	
65	8	8	8	8	01	D		80-119-01	SCREW, SLOTTED, PAN HEAD, STEEL, 0-80 X 1/4	
66										
67	4	4	4	4	01	D		80-700-02	SOCKET, I.C. 16 PIN	
68	16	16	16	16	01	D		80-700-04	SOCKET, I.C. 22 PIN	
69	2	2	2	2	01	D		80-700-05	SOCKET, I.C. 24 PIN	
70										
71	3	3	3	3	2	D		80-870-07	WIRE, BUS, TINNED COPPER, 18 AWG	
72										
73	1	1	1	1	01	R		96-420-01	LOGIC DIAGRAM, CHARACTER REFRESH	
74										
75	1	–	–	–	01	A		27-017-02	MODEL T2201 DISPLAY FORMAT MODIFICATION	
76										

NOTES:

APPLICATION	
NEXT ASSY	USED ON

UNIT OF MEASURE:
01 – EACH 04 – BULK
02 – INCH 05 – AS REQ'D
03 – FEET 09 – OTHER (see notes)

KEY 1:
A – WITH B/M
D – WITHOUT B/M
R – REFERENCE
S – SPECIFICATION
O – OTHER (see notes)

DWN R. Nolasmun 8-27-75
CHK [illegible] 9/16/75
ENGR
APPD
APPD
APPD
KEY 2:

ENGR CHANGES			
REV	CHG NO.	DATE	APPD

ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA

TITLE
P. C. ASSEMBLY
CHARACTER REFRESH

SIZE	SHT 4 OF 4	BILL OF MAT'L NO.	REV
A		99-420-XX	B

FORM NO. 75-000-03

ITEM/ FIND NO.	QTY PER ASSY 04	03	02	01	UNIT OF MEAS	KEY(1)	KEY (2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE / DESCRIPTION	REMARKS
1	1	1	1	1	01	D		98-415-03	P.C. BOARD, MICROPROCESSOR-8080	
2	4	4	4	4	01	D		80-119-01	SCREW, SLOTTED, PAN HEAD, STEEL, 0-80 X 1/4	
3	2	2	2	2	01	D		80-202-25	RESISTOR, CARBON COMP, 27Ω, 5%, 1/4 W	R46, R47
4	42	42	42	42	01	D		80-202-63	RESISTOR, CARBON COMP, 1 KΩ, 5%, 1/4 W	R3-R10, R13-R16, R19-R28
5										R31-R36, R38-R41, R44,
6										R45, R48, R49, R50-R55
7	2	2	2	2	01	D		80-202-91	RESISTOR, CARBON COMP, 15 KΩ, 5%, 1/4 W	R56, R57
8	1	1	1	1	01	D		80-202-94	RESISTOR, CARBON COMP, 20 KΩ, 5%, 1/4 W	R37
9	4	4	4	4	01	D		80-260-01	RESISTOR, 243Ω, 1%, 1/8 W	R1, R11, R17, R29
10	4	4	4	4	01	D		80-260-02	RESISTOR, 301 Ω, 1%, 1/8 W	R2, R12, R18, R30
11										
12	1	1	1	1	01	D		80-261-01	RESISTOR, 1 KΩ, 1%, 1/4 W	R43
13	1	1	1	1	01	D		80-261-02	RESISTOR, 2 KΩ, 1%, 1/4 W	R42
14										
15										
16										
17	8	8	8	8	01	D		80-311-73	CAPACITOR, TANTALUM, 10 μfd, 20%, 25 V.	C1, C12, C20, C29
18										C36, C56, C59, C62
19	1	1	1	1	01	D		80-310-61	CAPACITOR, TANTALUM, 33 μfd, 20%, 10V.	C27

NOTES: 1. VERSION IDENTIFIES OPTIONAL FEATURES: -01 MICROPROCESSOR ONLY; -02 MICROPROC. W/TIMER; -03 MICROPROC. W/STACK; -04 MICROPROCESSOR W/TIMER AND STACK
2. LAST REF. DESIGNATIONS ARE: C67, L3, Q5, R57; REF. DESIG. C47, NOT USED.

APPLICATION	
NEXT ASSY	USED ON
07-419-XX	9003
27-010-01	KOS-78/10M
24-019-XX	9003
07-422-XX	T2201

UNIT OF MEASURE:
01-EACH 04-BULK
02-INCH 05-AS REQ'D
03-FEET 09-OTHER (see notes)

KEY 1:
A-WITH B/M
D-WITHOUT B/M
R-REFERENCE
S-SPECIFICATION
O-OTHER (see notes)

DWN R. Nahmmacher 5/20/75
CHK [illegible] 6/4/75
ENGR L. Fourchalet 6/23/75
APPD R. Chmara 6/4/75
APPD [illegible] 6/19/75
APPD [illegible] 7/2/75
KEY 2:

ENGR CHANGES REV	CHG NO.	DATE	APPD
B	SEE STATUS	10/10/75	
C	NEW ARTWORK	12/31/75	

ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA

TITLE P.C. ASSEMBLY MICROPROCESSOR-8080

SIZE	SHT	OF	BILL OF MAT'L NO.	REV
A	1	5	99-415-XX	C

FORM NO. 75-000-03

ITEM/ FIND NO.	QTY PER ASSY 04	03	02	01	UNIT OF MEAS	KEY(1)	KEY(2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REMARKS
20	57	57	57	57	01	D		80-331-08	CAPACITOR, CERAMIC, .01μf, 20%, 50V.	C2-C11, C13-C19, C21-C26
21										C28, C30-C35, C37-C46
22										C48-C55, C57, C58, C60,
23										C61, C63-C67
24										
25										
26										
27										
28										
29	3	3	3	3	01	D		80-430-01	SHIELDING BEAD	L1, L2, L3
30										
31										
32										
33	4	4	4	4	01	D		80-515-01	VOLTAGE REGULATOR, 5 VOLTS	Q1, Q2, Q3, Q4
34	1	1	1	1	01	D		80-515-02	VOLTAGE REGULATOR, 12 VOLTS	Q5
35	1	1	1	1	01	D		80-550-75	INTEGRATED CIRCUIT, 74123	A13K
36	3	3	3	3	01	D		80-550-00	INTEGRATED CIRCUIT, 7400	A10J, A12B, A12H
37	5	4	5	4	01	D		80-550-02	↕ 7402	A8C, A8F, A10E, A10K, A13A
38	2	2	2	2	01	D		80-550-27	INTEGRATED CIRCUIT, 7438	A8K, A9K

NOTES: 3. FOR QUANTITY AND P/N OF ROM & PROM INTEGRATED CIRCUITS REQUIRED, REFER TO SPECIFIC FIRMWARE CONFIGURATION DRAWING (DOCUMENT CATEGORY 10-XXX-XX)

APPLICATION

NEXT ASSY	USED ON

UNIT OF MEASURE:
01-EACH 04-BULK
02-INCH 05-AS REQ'D
03-FEET 09-OTHER (see notes)

KEY 1:
A-WITH B/M
D-WITHOUT B/M
R-REFERENCE
S-SPECIFICATION
O-OTHER (see notes)

DWN R. Nahamura 5/20/75
CHK [signature] 6/4/75
ENGR
APPD
APPD
APPD
KEY 2:

ENGR CHANGES

REV	CHG NO.	DATE	APPD

ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA

TITLE P.C. ASSEMBLY MICROPROCESSOR — 8080

SIZE A | SHT 2 OF 5 | BILL OF MAT'L NO. 99-415-XX | REV C

FORM NO. 75-000-03

ITEM/ FIND NO.	QTY PER ASSY 04	03	02	01	UNIT OF MEAS	KEY(1)	KEY(2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REMARKS
39	4	4	4	4	01	D		80-550-04	INTEGRATED CIRCUIT, 7404	A8J, A11F, A11H, A13D
40	1	1	1	1	01	D		80-550-13	7414	A8E
41	4	4	4	4	01	D		80-550-08	7408	A7D, A10D, A10H, A12E
42	2	2	2	2	01	D		80-550-10	7410	A9J, A13C
43	1	1	1	1	01	D		80-550-16	7420	A9H
44	2	2	2	2	01	D		80-550-23	7430	A7A, A7B
45	3	3	3	3	01	D		80-550-24	7432	A7C, A9B, A12F
46	1	1	1	1	01	D		80-550-79	74132	A11K
47	2	0	2	0	01	D		80-550-29	7442A	A5F, A5H
48	5	3	5	3	01	D		80-550-45	7474	A7E, A8D, A8H, A9D, A11E
49	1	1	1	1	01	D		80-550-55	7486	A11C
50	1	1	1	1	01	D		80-550-63	7495A	A11J
51	2	2	2	2	01	D		80-550-92	74155	A9A, A9C
52	5	0	5	0	01	D		80-550-97	INTEGRATED CIRCUIT, 74161 (ALT 9316)	A6F, A6H, A7F, A7H, A9E
53	1	1	1	1	01	D		80-550-99	INTEGRATED CIRCUIT, 74163	A11D
54	3	3	3	3	01	D		80-553-06	I.C. TRI-STATE HEX INVERTER, 8098	A1F, A2F, A2H
55	1	1	1	1	01	D		80-554-05	INTEGRATED CIRCUIT, 74H11	A9F
56	2	2	2	2	01	D		80-554-35	I.C. 1 OF 8 BINARY DECODER, 8205	A11B, A12A
57	2	2	2	2	01	D		80-554-36	I.C., MULTI-MODE LATCH BUFFER, 8212	A6E, A7J

NOTES:

APPLICATION

NEXT ASSY	USED ON

UNIT OF MEASURE:
01-EACH 04-BULK
02-INCH 05-AS REQ'D
03-FEET 09-OTHER (see notes)

KEY 1:
A-WITH B/M
D-WITHOUT B/M
R-REFERENCE
S-SPECIFICATION
O-OTHER (see notes)

DWN R. Nishimura 5/20/75
CHK [illegible] 6/4/75
ENGR
APPD
APPD
APPD
KEY 2:

ENGR CHANGES

REV	CHG NO.	DATE	APPD

ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA

TITLE P.C. ASSEMBLY MICROPROCESSOR - 8080

SIZE A | SHT 3 OF 5 | BILL OF MAT'L NO. 99-415-XX | REV C

FORM NO. 75-000-03

ITEM/ FIND NO.	QTY PER ASSY 04	03	02	01	UNIT OF MEAS	KEY(1)	KEY(2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REMARKS
58	2	2	2	2	01	D		80-554-37	I.C. PARALLEL, BI-DIREC, BUS DRVR. 8216	A1K, A2K
59	1	1	1	1	01	D		80-555-04	INTEGRATED CIRCUIT, 74L04	A10F
60	8	8	8	8	01	D		80-555-42	INTEGRATED CIRCUIT, 74LS38	A3J, A3K, A4J, A5J, A6J
61										A4K, A5K, A6K
62	1	1	1	1	01	D		80-560-01	I.C., MOS CLOCK DRIVER, MH0026N	A12J
63	1	1	1	1	01	D		80-560-15	I.C., MOS, CPU 8080	A4F
64	2	2	0	0	01	D		80-560-16	INTEGRATED CIRCUIT, 2112	A1J, A2J
65										
66										
67										
68	4	4	4	4	01	D		80-680-04	MINIATURE SWITCH, DIP. 8 SPST	A8A, A8B, A11A, A13B
69										
70										
71	2	2	2	2	01	D		80-700-02	SOCKET, I.C., 16 PIN	
72	21	21	21	21	01	D		80-700-05	SOCKET, I.C., 24 PIN	
73	1	1	1	1	01	D		80-700-08	SOCKET, I.C., 40 PIN	
74										
75										
76										

NOTES:

APPLICATION	
NEXT ASSY	USED ON

UNIT OF MEASURE:
01-EACH 04-BULK
02-INCH 05-AS REQ'D
03-FEET 09-OTHER (see notes)

KEY 1:
A-WITH B/M
D-WITHOUT B/M
R-REFERENCE
S-SPECIFICATION
O-OTHER (see notes)

DWN R. Nakamura 5/20/75
CHK [signature] 6/4/75
ENGR
APPD
APPD
APPD
KEY 2:

ENGR CHANGES			
REV	CHG NO.	DATE	APPD

ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA

TITLE P.C. ASSEMBLY MICROPROCESSOR - 8080

SIZE	SHT 4 OF 5	BILL OF MAT'L NO.	REV
A		99-415-XX	C

FORM NO. 75-000-03

ITEM/ FIND NO.	QTY PER ASSY 04	03	02	01	UNIT OF MEAS	KEY(1)	KEY (2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REMARKS
77										
78										
79	3	3	3	3	02	D		80-870-07	WIRE, BUSS, TINNED COPPER, 18AWG	
80										
81	1	1	1	1	05	R		10-XXX-XX	MACHINE CONFIGURATION	
82	1	1	1	1	01	D		40-002-01	STIFFENER, P.C. BOARD	
83	1	1	1	1	05	R		96-415-01	LOGIC DIAGRAM, MICROPROCESSOR-8080	

NOTES:

APPLICATION	
NEXT ASSY	USED ON

UNIT OF MEASURE:
01-EACH 04-BULK
02-INCH 05-AS REQ'D
03-FEET 09-OTHER (see notes)

KEY 1:
A-WITH B/M
D-WITHOUT B/M
R-REFERENCE
S-SPECIFICATION
O-OTHER (see notes)

DWN R. Nahumm 5/20/75
CHK [illegible] 6/4/75
ENGR
APPD
APPD
APPD
KEY 2:

ENGR CHANGES			
REV	CHG NO.	DATE	APPD

ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA

TITLE P.C. ASSEMBLY MICROPROCESSOR-8080

SIZE	SHT	OF	BILL OF MAT'L NO.	REV
A	5	5	99-415-XX	C

FORM NO. 75-000-03

ITEM/ FIND NO.	QTY PER ASSY 04	03	02	01	00	UNIT OF MEAS	KEY(1)	KEY(2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REMARKS
1	1	1	1	1	1	01	D		98-419-01	PC. BOARD, 16K RAM	
2	2	2	2	2	2	01	D		51-005-01	INSULATING SPACER	
3	2	2	2	2	2	01	D		39-002-01	STIFFENER, P.C. BOARD, AL	
4	8	8	8	8	8	01	D		80-100-30	SCREW, SLOTTED, PAN HD., SST, 2-56×1/4	
5	8	8	8	8	8	01	D		80-154-10	WASHER, NYLON, #2	
6											
7	16	16	16	16	16	01	D		80-202-25	RESISTOR, CARBON COMP, 27Ω, 5%, 1/4W	R13, R14, R17, R20, R24, R25, R28, R31, R47, R48, R50, R52, R54-R56, R58
8											
9											
10	40	40	40	40	40	01	D		80-202-55	RESISTOR, CARBON COMP, 470Ω, 5%, 1/4W	R1, R2, R4-R12, R15, R16, R18, R19, R21-R23, R26, R27, R29, R30, R33, R34, R36-R46, R49, R51, R53, R57, R76
11											
12											
13											
14	1	1	1	1	1	01	D		80-202-63	RESISTOR, CARBON COMP, 1KΩ, 5%, 1/4W	R75
15	16	16	16	16	16	01	D		80-202-65	RESISTOR, CARBON COMP, 1.2KΩ, 5%, 1/4W	R59-R74
16	1	1	1	1	1	05	R		10-029-XX	INSTRUCTION, 16K RAM ADDRESSING	
17											
18											
19											

NOTES: [1] VERSION DEFINES QTY OF RAM: -00 = NO RAM; -01 = 4K BYTES OF RAM, A0S-A7S & A0T-A7T; -02 = 8K BYTES OF RAM, A0S-A7S, A0T-A7T, A0U-A7U & A0V-A7V; -03 = 12K BYTES OF RAM, A0S-A7S, A0T-A7T, A0U-A7U, A0V-A7V, A0W-A7W & A0X-A7X; -04 = 16K BYTES OF RAM, ALL RAM LOCATIONS.

APPLICATION	
NEXT ASSY	USED ON
02-405-XX	9003

UNIT OF MEASURE:
01-EACH 04-BULK
02-INCH 05-AS REQ'D
03-FEET 09-OTHER (see notes)

KEY 1:
A-WITH B/M
D-WITHOUT B/M
R-REFERENCE
S-SPECIFICATION
O-OTHER (see notes)

DWN	11/18/75
CHK	1/10/76
ENGR	1/20/76
APPD	1/16/76
APPD	1/30/76
APPD	1/28/76

KEY 2:

ENGR CHANGES

REV	CHG NO.	DATE	APPD
B	NEW ARTWK	3/23/76	
C	NEW ARTWORK	10/1/76	

ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA

TITLE
P.C. ASSEMBLY, 16K RAM

SIZE	SHT	OF	BILL OF MAT'L NO.	REV
A	1	3	99-419-XX	C

FORM NO. 75-000-03

ITEM/ FIND NO.	QTY PER ASSY 04	03	02	01	00	UNIT OF MEAS	KEY(1)	KEY (2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE / DESCRIPTION	REMARKS
20	4	4	4	4	4	01	D		80-310-61	CAPACITOR, TANTALUM, 33μf, 20%, 10V	C1, C9, C113, C121
21	3	3	3	3	3	01	D		80-311-73	CAPACITOR, TANTALUM, 10μf, 20%, 25V	C144, C146, C149
22	119	119	119	119	119	01	D		80-331-08	CAPACITOR, CERAMIC, .01μf, 20%, 50V	C2, C10, C17-C112, C114,
23											C122, C129-C143, C145,
24											C147, C150, C151
25	12	12	12	12	12	01	D		80-339-30	CAPACITOR, CERAMIC, 470pf, 20%, 1KV	C4, C5, C7, C12, C13, C15,
26											C116, C117, C119, C124, C125,
27											C127,
28	12	12	12	12	12	01	D		80-345-49	CAPACITOR, CERAMIC, .1μf, 10%, 50V	C3, C6, C8, C11, C14, C16, C119
29											C118, C120, C123, C126, C128
30											
31	3	3	3	3	3	01	D		80-430-01	SHIELDING BEAD	L1, L2, L3
32	3	3	3	3	3	02	D		80-870-07	BUS WIRE, TINNED COPPER, 18 AWG	
33	8	8	8	8	8	01	D		80-500-02	DIODE, IN914B	CR1 - CR8
34	8	8	8	8	8	05	D		80-500-04	DIODE, IN4448	CR1 - CR8 ALTERNATE
35											
36											
37	4	4	4	4	4	01	D		80-520-01	TRANSISTOR, NPN, 2N2222A	Q1, Q3, Q5, Q7
38	8	8	8	8	8	01	D		80-520-02	TRANSISTOR, NPN, 2N2369A	Q9-Q16

NOTES: 2. REF. DESIGNATIONS R3, R32, R35 & C148 ARE NOT USED. LAST REF. DESIG. USED ARE C151, CR8, L3 Q16 & R76

APPLICATION	
NEXT ASSY	USED ON

UNIT OF MEASURE:
01-EACH 04-BULK
02-INCH 05-AS REQ'D
03-FEET 09-OTHER (see notes)

KEY 1:
A-WITH B/M
D-WITHOUT B/M
R-REFERENCE
S-SPECIFICATION
O-OTHER (see notes)

DWN	11/19/75
CHK	1/28/76
ENGR	
APPD	
APPD	
APPD	

KEY 2: —

ENGR CHANGES			
REV	CHG NO.	DATE	APPD

ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA

TITLE
P. C. ASSEMBLY, 16K RAM

SIZE	SHT	OF	BILL OF MAT'L NO.	REV
A	2	3	99-419-XX	C

FORM NO. 75-000-03

ITEM/ FIND NO.	QTY PER ASSY 04	03	02	01	00	UNIT OF MEAS	KEY(1)	KEY(2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REMARKS
39	4	4	4	4	4	01	D		80-530-01	TRANSISTOR, PNP, 2N2906A	Q2, Q4, Q6, Q8
40											
41											
42	9	9	9	9	9	01	D		80-550-04	INTEGRATED CIRCUIT, 7404	A1G, A2G, A9G, A11G,
43											A1H, A2HA, A5H, A6H, A11H
44	2	2	2	2	2	01	D		80-550-08	7408	A3G, A7H
45	2	2	2	2	2	01	D		80-550-10	7410	A5G, A4H
46	1	1	1	1	1	01	D		80-550-24	7432	A9H
47	2	2	2	2	2	01	D		80-550-27	7438	A10G, A10H
48	1	1	1	1	1	01	D		80-550-29	7442A	A2HB
49	1	1	1	1	1	01	D		80-551-07	74174	A4G
50	4	4	4	4	4	01	D		80-554-05	INTEGRATED CIRCUIT, 74H11	A6G, A7G, A8G, A8H
51	1	1	1	1	1	01	D		80-550-92	" " 74155	A3H
52	8	8	8	8	8	01	D		80-560-01	INTEGRATED CIRCUIT, MH0026	A2A, A5A, A9A, A12A,
53											A2F, A5F, A9F, A12F
54	64	48	32	16	0	01	D		80-560-09	INTEGRATED CIRCUIT, MM5262 RAM	[1]
55	64	64	32	16	64	01	D		80-700-04	SOCKET, I.C., 22 PIN	
56	64	48	32	16	0	05	D		80-560-06	INTEGRATED CIRCUIT, 600314 RAM	ALTERNATE ITEM 54
57	1	1	1	1	1	05	R		96-419-01	LOGIC DIAGRAM, 16K RAM	

NOTES:

APPLICATION	
NEXT ASSY	USED ON

UNIT OF MEASURE:
01-EACH 04-BULK
02-INCH 05-AS REQ'D
03-FEET 09-OTHER (see notes)

KEY 1:
A-WITH B/M
D-WITHOUT B/M
R-REFERENCE
S-SPECIFICATION
O-OTHER (see notes)

DWN O. Roland 11/9/75
CHK Lee Lane 11/10/76
ENGR
APPD
APPD
APPD

KEY 2: —

ENGR CHANGES			
REV	CHG NO.	DATE	APPD

ZENTEC ZENTEC CORPORATION SANTA CLARA, CALIFORNIA

TITLE
P. C. ASSEMBLY, 16K RAM

SIZE	SHT 3 OF 3	BILL OF MAT'L NO.	REV
A		99-419-XX	C

FORM NO. 75-000-03