THE SERIAL DATA INTERFACE MODULE PROVIDES THE CIRCUITRY, CABLES, AND CONNECTORS REQUIRED TO CONNECT AN ASYNCHRONOUS RS232 ORIENTED TERMINAL OR MODEM TO THE JUPITER II SYSTEM BUS.

THE SERIAL DATA INTERFACE MODULE CONVERTS THE PARALLEL DATA ON THE SYSTEM BUS TO SERIAL FORMAT ADDING STOP, START, AND PARITY BITS. THE MODULE ALSO HANDLES THE RECEIVING OF SERIAL DATA, STRIPPING OFF THE STOP, START, AND PARITY BITS, AND CONVERTING TO PARALLEL FORMAT.

THE MODULE IS DOUBLE BUFFERED ON BOTH INPUT AND OUTPUT WHICH ALLOWS ONE CHARACTER (SERIAL TRANSMISSION) TIME LEEWAY FOR INPUT OR OUTPUT OF DATA BETWEEN THE MODULE AND THE CPU. THE MODULE UTILIZES A SELECTABLE INTERRUPT TO NOTIFY THE CPU THAT IT IS READY TO RECEIVE (OR INPUT) ANOTHER DATA BYTE.

THEORY OF OPERATION

THE BLOCK DIAGRAM ILLUSTRATES THE MAJOR FUNCTIONAL COMPONENTS OF THE SERIAL DATA INTERFACE MODULE. THE MAJORITY OF THE MODULES CONTROL FUNCTIONS ARE IMPLEMENTED WITHIN IC1 WHICH IS A MOTOROLA MC6850 ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER.

ADDRESS SELECT LOGIC

THE UPPER 256 BYTES (FF00-FFFF) OF JUPITER II SYSTEM MEMORY ARE DESIGNATED FOR I/O ADDRESSING. WHEN MEMORY WITHIN THIS RANGE IS ADDRESSED, THE IO SIGNAL FROM THE CPU MODULE IS TRUE. THIS IO SIGNAL AND THE 8 LEAST SIGNIFICANT BITS OF THE MEMORY ADDRESS ON THE SYSTEM BUS ARE DECODED BY THE ADDRESS SELECT LOGIC. IF THE MEMORY ADDRESS ON THE SYSTEM BUS CORRESPONDS TO THE ADDRESS SELECTED FOR THIS MODULE, THE OUTPUT OF THE ADDRESS SELECT LOGIC GOES TRUE, TRIGGERING THE REPLY GENERATOR AND THE SELECTION AND CONTROL CIRCUITRY

REPLY GENERATOR

DATA IS TRANSFERRED BETWEEN THE CPU AND OTHER MODULES DURING THE CLOCK 2 TIMING PERIOD. TO INSURE THAT SUFFICIENT TIME IS ALLOWED FOR RELIABLE DATA TRANSFER, THE CLOCK 2 PERIOD IS VARIABLE. THE *RPLY SIGNAL IS USED TO NOTIFY THE CPU THAT THE ADDRESSED DEVICE HAS RECEIVED THE CLOCK 2 TIMING SIGNAL (THE CPU TERMINATES THE CLOCK 2 PERIOD 0.5 NANOSECONDS LATER). THE REPLY GENERATOR GATES THE DECODED ADDRESS SELECT SIGNAL WITH THE CLK2 FORMING *RPLY WHICH IS OUTPUT TO THE SYSTEM BUS.

THE SERIAL DATA INTERFACE MODULE PROVIDES THE CAPABILITY FOR THE CPU TO READ FROM OR WRITE INTO TWO SETS OF REGISTERS. ONE SET OF REGISTERS IS USED TO CONTROL MODULE OPERATION, AND TO ALLOW THE CPU TO DETERMINE MODULE STATUS (CONTROL/STATUS REGISTERS). THE OTHER SET OF REGISTERS IS USED TO TRANSFER DATA (DATA REGISTERS). THE SELECTION AND CONTROL LOGIC DETERMINES REGISTER SELECTION, AND PROVIDES THE VARIOUS CONTROL AND TIMING SIGNALS REQUIRED TO PERFORM THE MODULE FUNCTIONS.

WHEN THE ADDRESS SELECT LOGIC OUTPUT IS TRUE THE FOLLOWING MODULE INPUTS ARE UTILIZED BY THE SELECTION AND CONTROL LOGIC:

*WRITE - DETERMINES WHETHER OPERATION IS READ (INPUT TO CPU) OR WRITE (OUTPUT FROM CPU). WHEN *WRITE IS LOW THE CPU IS WRITING INTO THE MODULE CONTROL OR DATA REGISTERS. WHEN *WRITE IS HIGH, THE CPU IS READING FROM THE MODULE STATUS OR DATA REGISTERS.

A0 - THE LEAST SIGNIFICANT ADDRESS BIT IS USED TO SELECT THE DATA OR STATUS/CONTROL REGISTERS. WHEN A0 IS TRUE THE DATA REGISTERS ARE SELECTED.

CLK2 - THIS SIGNAL ENABLES THE DATA BUS BUFFERS AND CLOCKS DATA TO AND FROM THE MODULE.

DATA BUS BUFFERS

THE DATA BUS BUFFERS ARE TRI-STATE DEVICES MEANING THEY ARE ACTIVE BOTH THE HIGH AND LOW OUTPUT STATES, AND THEY HAVE A THIRD "OFF" STATE IN WHICH THEY PRESENT A HIGH IMPEDENCE TO THE DATA BUS. THESE BUFFERS ARE USED TO TRANSFER DATA TO OR FROM THE MODULE.

TRANSMITTER

DATA RECEIVED FROM THE CPU IS FED THROUGH THE DATA BUS BUFFERS TO THE TRANSMIT DATA REGISTER. THE DATA IS THEN TRANSFERRED TO A /SHIFT REGISTER WHERE IT IS SERIALIZED AND OUTPUT TO THE "TD" DRIVER. EACH DATA CHARACTER IS PRECEDED BY A START BIT AND FOLLOWED BY ONE OR TWO STOP BITS. OPTIONAL PARITY CAN BE OPTIONALLY ADDED TO THE CHARACTER BETWEEN THE LAST DATA BIT AND THE FIRST STOP BIT. WHEN THE CHARACTER HAS BEEN TRANSMITTED A STATUS BIT CALLED TRANSMITTER BUFFER EMPTY WILL GO TRUE INDICATING THAT ANOTHER CHARACTER MAY BE LOADED INTO THE DEVICE.

RECEIVER

SERIAL DATA IS BUFFERED AND TRANSMITTED TO THE RECIEVER /LOGIC WHERE IT IS SYNCHRONIZED WITH THE MODULE CLOCK AND INPUT TO A SHIFT REGISTER. WHEN A COMPLETE CHARACTER HAS BEEN RECEIVED, PARITY AND OTHER ERROR CONDITIONS ARE CHECKED AND THE CHARACTER IS TRANSFERRED TO THE RECEIVE DATA REGISTER. WHEN A CHARACTER IS TRANSFERRED TO THE RECEIVE DATA REGISTER, A RECEIVE DATA REGISTER FULL BIT IS SET IN THE STATUS REGISTER. AT THIS TIME DATA INDICATING ANY ERROR CONDITIONS DETECTED WOULD ALSO BE SET INTO THE STATUS REGISTER.

THE STATUS REGISTER CONTAINS INFORMATION PERTAINING TO THE STATUS OF THE DATA REGISTERS, THE MODEM OR TERMINAL, AND ANY DETECTED ERROR CONDITIONS RELATED TO THE CHARACTER CURRENTLY IN THE RECEIVE DATA REGISTER.

STATUS REGISTER BIT	CONTENTS	MEANING
0	RECEIVE DATA REGISTER FULL (RDRF)	RECEIVE DATA REGISTER CONTAINS A CHARACTER THAT HAS NOT BEEN INPUT TO THE CPU. IF RDRF IS FALSE, THE DATA IN THE RECEIVE DATA REGISTER IS NOT CURRENT.
1	TRANSMIT DATA REGISTER EMPTY (TDRE)	THE TRANSMIT DATA REGISTER IS READY TO RECEIVE ANOTHER CHARACTER FROM THE CPU. IF TDRE IS FALSE, THE CHARACTER PREVIOUSLY OUTPUT TO THE TRANSMIT DATA REGISTER HAS NOT BEEN TRANSFERRED TO THE SHIFT REGISTER.
2	RECEIVED LINE SIGNAL (RLS) DATA TERMINAL READY (DTR)	MODEM OR TERMINAL IS NOT IN READY STATE. IF A MODEM IS BEING UTILIZED IT IS NOT RECEIVING A VALID CARRIER SIGNAL. IF A TERMINAL IS CONNECTED, THE TERMINAL IS NOT READY TO TRANSMIT OR RECEIVE DATA.
3	CLEAR TO SEND (CTS) REQUEST TO SEND (RTS)	IF A MODEM IS CONNECTED, IT IS NOT READY TO TRANSMIT DATA. IF A TERMINAL IS CONNECTED, THE TERMINAL IS NOT READY TO RECEIVE DATA FROM THE CPU.
4	FRAMING ERROR	SYCHRONIZATION ERROR ON RECEIVED CHARACTER INDICATES TRANSMISSION PROBLEM. THE RECEIVED DATA WORD DID NOT HAVE A STOP BIT FOLLOWING IT. THIS CONDITION IS MOST OFTEN CAUSED BY THE 'BREAK' KEY BEING DEPRESSED ON A TERMINAL. THE DATA WORD IS USUALLY ZERO IN THIS CASE.
5	RECEIVER OVERRUN	ONE OR MORE RECEIVE CHARACTERS HAVE BEEN LOST BECAUSE DATA WAS NOT BEEN TRANSFERRED INTO CPU AT A RATE SUFFICIENT TO KEEP UP WITH LINE SPEED. THIS BIT IS NOT SET UNTIL THE VALID CHARACTER PRIOR TO OVERRUN HAS BEEN INPUT TO THE CPU.
6	PARITY ERROR	PARITY ERROR HAS BEEN DETECTED FOR CHARACTER CURRENTLY IN READ DATA REGISTER.
7	INTERRUPT REQUEST	MODULE IS REQUESTING AN INTERRUPT.

ALL RECEIVE ERROR BITS (4-6) WILL BE RESET WHEN CONTENTS OF READ DATA REGISTER ARE READ INTO THE CPU.

CONTROL REGISTER

THE CONTROL REGISTER IS LOADED FROM THE CPU THROUGH THE DATA BUS BUFFERS. THE CONTROL REGISTER CONTAINS INFORMATION NECESSARY TO OPERATE THE MODULE. THE CONTROL REGISTER IS ALSO USED AS A MASTER RESET FOR THE MODULE.

MASTER RESET - CONTROL REGISTER BITS 0 AND 1 MUST BE SET. FOR EXAMPLE, THE FOLLOWING DATA WORD TRANSMITTED TO THE CONTROL REGISTER WILL INITIATE A MASTER RESET: 03

COUNTER CONTROL - WHEN NOT INDICATING MASTER RESET, BITS 0 AND 1 CONTROL A CLOCK SYNCHRONIZATION COUNTER. AFTER MASTER RESET THESE BITS MUST ALWAYS BE SET AS FOLLOWS: BIT 1=0, BIT 0=1.

WORD SELECT - THE WORD SELECT BITS ARE USED TO SELECT WORD LENGTH, PARITY, AND THE NUMBER OF STOP BITS. THE ENCODING FORMAT IS AS FOLLOWS:

BIT 4	BIT 3	BIT 2	FUNCTION
0	0	0	7 BITS + EVEN PARITY + 2 STOP BITS
0	0	1	7 BITS + ODD PARITY + 2 STOP BITS
0	1	0	7 BITS + EVEN PARITY + 1 STOP BIT
0	1	1	7 BITS + ODD PARITY + 1 STOP BIT
1	0	0	8 BITS + 2 STOP BITS
1	0	1	8 BITS + 1 STOP BIT
1	1	0	8 BITS + EVEN PARITY + 1 STOP BIT
1	1	1	8 BITS + ODD PARITY + 1 STOP BIT

WORD LENGTH, PARITY SELECT, AND STOP BIT CHANGES ARE NOT BUFFERED AND THEREFORE BECOME EFFECTIVE IMMEDIATELY.

TRANSMITTER CONTROL BITS - BITS 5 AND 6 ARE USED TO CONTROL THE TRANSMITTING CONDITIONS. FOR NORMAL OPERATING CONDITIONS THESE BITS SHOULD BE SET AS FOLLOWS TO ENABLE TRANSMISSION: BIT 6=0, BIT 5=1. TO DISABLE TRANSMISSION: BIT 6=0, BIT 5=0. THE COMPLETE DEFINITIONS OF BITS 5 AND 6 ARE SHOWN IN THE FOLLOWING TABLE.

CR6	CR5	FUNCTION
0	0	RTS = LOW, TRANSMITTING INTERRUPT DISABLED.
0	1	RTS = LOW, TRANSMITTING INTERRUPT ENABLED.
1	0	RTS = HIGH, TRANSMITTING INTERRUPT DISABLED.
1	1	RTS = LOW, TRANSMITS A BREAK LEVEL ON THE TRANSMIT DATA OUTPUT. TRANSMITTING INTERRUPT DISABLED.

RECEIVE INTERRUPT ENABLE - RECEIVE DATA REGISTER FULL AND MODEM OR TERMINAL NOT READY (STATUS REGISTER BIT 2) INTERRUPTS ENABLED WHEN BIT 7 IS HIGH.

THE FOLLOWING TABLE ILLUSTRATES THE USE OF THE CONTROL REGISTER:

DATA WORD INTO CONTROL REGISTER	RESULT
03	MASTER RESET
	TRANSMISSION AND INTERRUPTS ENABLED. SET UP FOR MODULE TO GENERATE ODD PARITY AND SINGLE STOP BIT (7 BIT CHARACTER). MOST TERMINALS REQUIRE THIS FORMAT.
1D	TRANSMISSION AND INTERRUPTS ENABLED. SET UP FOR MODULE TO GENERATE ODD PARITY AND SINGLE STOP BIT (8-bit char)

THE CLOCK CIRCUIT USES A PROGRAMMABLE BIT GENERATOR TO GENERATE 14 COMMONLY USED BAUD RATES RANGING FROM 50 TO 9600 BAUD. REFER TO THE OPERATION SECTION FOR A COMPLETE LISTING OF AVAILABLE BAUD RATES. THE CLOCK CIRCUIT DRIVES THE TRANSMIT AND RECEIVE CLOCK INPUTS OF THE SELECTION AND CONTROL LOGIC.

DRIVERS/RECEIVERS

THE DRIVERS AND RECEIVERS ARE IMPLEMENTED USING CIRCUITS SPECIFICALLY DESIGNED TO MEET THE RS232-C SPECIFICATION. THESE CIRCUITS ARE UTILIZED TO INTERFACE THE MODULE TO THE CONTROLLED DEVICE. THESE CIRCUITS ARE CONNECTED TO THE CONTROLLED DEVICE THROUGH A SPECIAL CONNECTOR/CABLE ASSEMBLY. DEFFERENT ASSEMBLIES MUST BE SPECIFIED DEPENDING ON WHETHER THE CONTROLLED DEVICE IS A MODEM (DATA COMMUNICATION EQUIPMENT) OR A TERMINAL (DATA TERMINAL EQUIPMENT).

IF THE CONTROLLED DEVICE IS A MODEM, A DCE ASSEMBLY MUST BE SPECIFIED. IF THE DEVICE IS A TERMINAL, A DTE ASSEMBLY SHOULD BE USED.

PROGRAMMING CONSIDERATIONS

THE SERIAL DATA INTERFACE MODULE PROGRAMMING IS STRAIGHTFORWARD. ALL DATA TRANSFERS SHOULD BE CONTROLLED BY INTERRUPT. SINCE THE MODULE IS DOUBLE-BUFFERED ON BOTH INPUT AND OUTPUT, TIMING IS NOT CRITICAL. FOR EXAMPLE IF THE SERIAL I/O IS OPERATING AT THE RELATIVELY HIGH SPEED OF 1200 BAUD, THE CPU HAS A TOTAL OF 8.3 MILLISECONDS (1 CHARACTER TIME @ 10 BITS/CHARACTER) TO SERVICE AN INTERRUPT.

INITIAL SETUP (FIGURE)

THE INITIAL SETUP ROUTINE SHOULD BE FOLLOWED WHEN A SUBROUTINE FIRST BEGINS USING THE MODULE, WHEN CHANGING FROM TRANSMIT TO RECEIVE MODE, OR AFTER A POWER RESTORE INTERRUPT HAS OCCURRED. DURING THE POWER ON INITILIZATION ROUTINES, IT IS ADVISABLE TO MASK INTERRUPTS TO AVOID SERVICING INTERRUPTS CAUSED BY POWER TURN-ON GLITCHES.

OUTPUT THE MASTER RESET COMMAND (03) TO THE CONTROL REGISTER. THIS COMMAND MUST BE OUTPUT TO ENABLE THE INTERFACE AFTER A POWER-ON RESET HAS OCCURRED.

OUTPUT A CONTROL WORD TO THE CONTROL REGISTER. BIT 0 MUST EQUAL 1, BIT 1 MUST EQUAL 0 IN THIS WORD. BIT 7 MUST EQUAL 1 TO ENABLE THE RECEIVE INTERRUPT CIRCUITRY. BITS 2-4 MUST SET UP THE SERIAL CHARACTER FORMAT TO BE COMPATIBLE WITH THE INTERFACED DEVICE OR COMMUNICATION NETWORK.

OUTPUT RESET
TO
CONTROL REG.

SETUP C. R.
PARAMETERS

INITIALIZE
BUFFER POINTERS, ETC
CLEAR INTERRUPT MASK

INTERRUPT SERVICE

BEFORE TRANSFERRING DATA, THE CONTENTS OF THE STATUS REGISTER SHOULD BE INPUT TO THE CPU. THES STEP IS IMPORTANT SINCE THE STATUS REGISTER RECEIVE ERROR BITS ARE RESET WHEN DATA IS TRANSFERRED.

AT THIS TIME SR BIT 7 SHOULD BE CHECKED TO DETERMINE THAT THIS DEVICE GENERATED THE INTERRUPT REQUEST. IF SR BIT 7 IS NOT SET (ONE) AN ERROR CONDITION EXISTS (UNLESS OTHER DEVICES SHARE THE SAME INTERRUPT REQUEST LEVEL). THIS CONDITION COULD OCCUR BECAUSE OF A HARDWARE PROBLEM (NOISE GENERATED INTERRUPTS) OR BECAUSE A SUBROUTINE HAS ERRONOUSLY JUMPED TO THE INTERRUPT SERVICE ROUTINE.

STATUS REGISTER BITS 2 AND 3 INDICATE A PROBLEM RELATED TO THE MODEM OR TERMINAL (EG POWER OFF). A COMMON SOURCE OF THIS TYPE OF PROBLEM WOULD BE AN IMPROPERLY WIRED INTERFACE CONNECTOR. AN INTERFACE CONNECTOR IMPROPERLY SEATED COULD CAUSE THESE SR BITS TO BE SET.

STATUS REGISTER BITS 4 AND 6 INDICATE A TRANSMISSION PROBLEM. THESE PROBLEMS ARE NORMALLY ENCOUNTERED WITH TELEPHONE LINE CIRCUITS. WHEN THESE ERRORS OCCUR, THE ERROR RECOVERY SOFTWARE SHOULD REQUEST RETRANSMISSION OF THE MESSAGE FROM THE ORIGINATING SOURCE.

STATUS REGISTER BIT 5 WILL BE SET IF THE INTERRUPT IS NOT BEING SERVICED AT A FAST ENOUGH RATE. IF THESE ERRORS OCCUR, IT MAY BE NECESSARY TO CONNECT TO A HIGHER PRIORITY INTERRUPT REQUEST LINE.

READ STATUS
REGISTER

SR BIT 7 ? NO — CPU PROBLEM

YES

SR BIT
0 RECEIVE ? NO
1 TRANSMIT ?

SR BIT
2 OR 3 ? YES — TERMINAL OR MODEM PROBLEM

SR BIT
4 OR 6 YES — ERROR RECOVERY ROUTINE

YES — SR BIT 3 ? NO — INPUT (OR OUTPUT) DATA CHARACTER INCREMENT POINTER ETC

OPERATION

THIS SECTION PROVIDES INFORMATION REQUIRED TO SETUP ADDRESS, INTERRUPT, BAUD RATE, AND PERIPHERAL CONTROL SIGNAL SELECTION SWITCHES. DATA ON THE PERIPHERAL CONNECTORS IS ALSO INCLUDED IN THIS SECTION.

SWITCHING IS ACCOMPLISHED THROUGH THE USE OF JUMPER WIRES ON IC SOCKETS. REFER TO THE MODULE ASSEMBLY MANUAL FOR INFORMATION ON THE PREPARATION OF THESE JUMPERS.

ADDRESS SELECTION

CAPABILITY IS PROVIDED TO DESIGNATE PERMISSIBLE MEMORY LOCATION AS THE ADDRESS OF THIS MODULE.

THE PERMISSIBLE MEMORY LOCATIONS FOR IO DEVICES ARE FF00 THROUGH FFDF. CARE SHOULD BE TAKEN TO INSURE THAT TWO IO DEVICES DO NOT SHARE THE SAME MEMORY ADDRESSES.

THIS DEVICE UTILIZES TWO MEMORY LOCATIONS, ONE FOR LOADING THE CONTROL REGISTER OR READING THE STATUS REGISTER, AND THE OTHER FOR TRANSFER OF DATA. THIS SELECTION IS DETERMINED BY THE LOW ORDER ADDRESS BIT (A0). IF A0 IS TRUE THE DATA REGISTERS ARE SELECTED, IF A0 IA FALSE THE /CONTROL /STATUS REGISTERS ARE SELECTED. FOR EXAMPLE, IF THE MEMORY LOCATIONS SELECTED FOR THIS MODULE ARE FF08 AND FF09, FF08 WOULD ADDRESS THE CONTROL/STATUS REGISTERS, WHILE FF09 WOULD BE USED FOR DATA TRANSFER.

SWITCHES SW1 AND SW2 ARE USED FOR ADDRESS SELECTION. SW2 DETERMINES THE MOST SIGNIFICANT SELECTABLE HEX CHARACTER, WHILE SW1 SELECTS THE LEAST SIGNIFICANT CHARACTER E. G.

DEVICE MEMORY ADDRESSES: FFXY OR FFX(Y+1)
WHERE X = SW2
Y = SW1

THE ADDRESS CHARACTERS ARE SELECTED ACCORDING TO THE FOLLOWING TABLE:

SW2 ADDRESS BIT	SW1 ADDRESS BIT	CONNECT SWITCH PIN TO	SELECT TRUE	SELECT FALSE
A7	A3	14	15	13
A6	A2	17	18	16
A5	A1	5	4	6
A4		2	1	3

FOR EXAMPLE, TO SELECT DEVICE ADDRESS FF5A AND FF5B:

SW2 MUST BE WIRED TO SELECT THE CHARACTER 5, BINARY 0101;

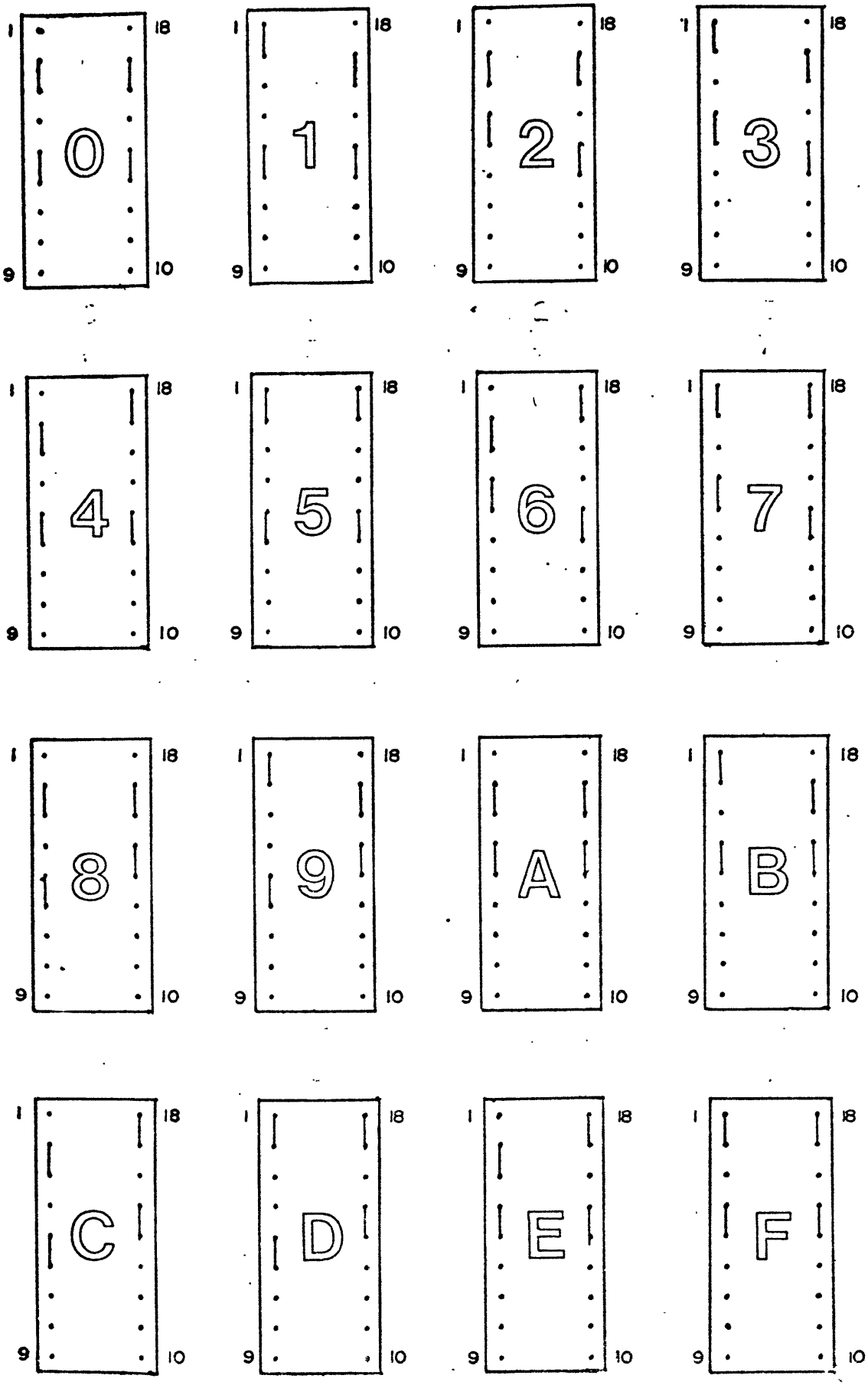
A7 = 0
A6 = 1
A5 = 0
A4 = 1

CONNECT A7 FALSE PIN 14 TO PIN 13
A6 TRUE PIN 17 TO PIN 18
A5 FALSE PIN 5 TO PIN 6
A4 TRUE PIN 2 TO PIN 1

SW1 MUST BE WIRED TO SELECT A OR B, BINARY 101X;
A3 = TRUE
A2 = FALSE
A1 = TRUE

CONNECT A3 TRUE PIN 14 TO PIN 15
A2 FALSE PIN 17 TO PIN 16
A1 TRUE PIN 5 TO PIN 4

THE FOLLOWING PICTURE ILLUSTRATES THE REQUIRED CONNECTIONS FOR EACH OF THE HEX CHARACTERS:

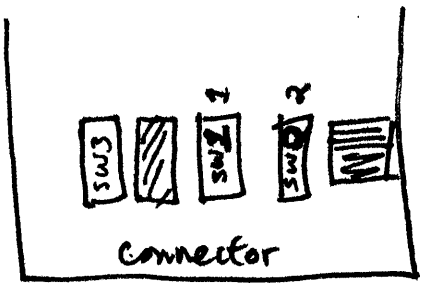


INTERRUPT SELECTION

ONE MASKABLE INTERRUPT LEVEL MAY BE SELECTED FROM THE FOLLOWING

AVAILABLE CHOICES:

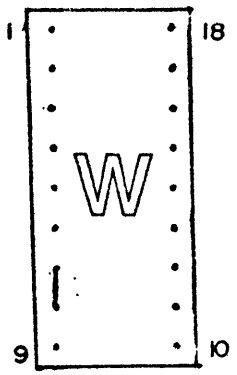
IRQ0
IRQ1
IRQ2
IRQ3
IRQ4
IRQ5
IRQ6
NONE

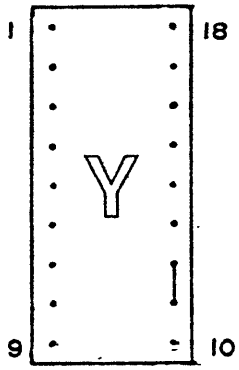


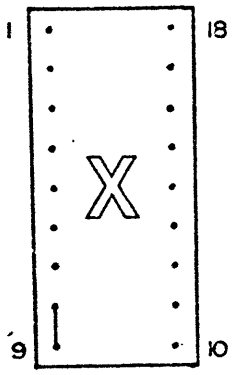
Top view of board

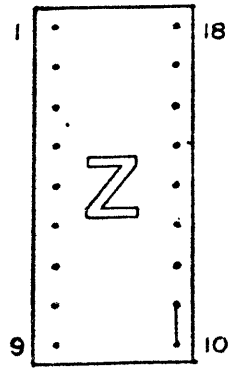
PORTIONS OF SW1 AND SW2 ARE UTILIZED TO MAKE THE INTERRUPT SELECTION:

	CONNECT SW1 PIN 8 TO:	CONNECT SW1 PIN 11 TO:		CONNECT SW2 PIN 8 TO:	CONNECT SW2 PIN 11 TO:
IRQ0 (W)	7	NC	IRQ4 (W)	7	NC
IRQ1 (X)	9	NC	IRQ5 (X)	9	NC
IRQ2 (Y)	NC	12	IRQ6 (Y)	NC	12
IRQ3 (Z)	NC	10			









SW3 IS UTILIZED TO SELECT BAUD RATE:
(USE HEX CHARACTERS FROM PREVIOUS PAGES)

BAUD	CHARACTER FROM TABLE
50	2
75	3
110	F
134.5	4
150	E
200	5
300	D
600	6
1200	B
1800	A
2400	7 OR C
4800	9
9600	8

PERIPHERAL CONTROL SIGNALS

CERTAIN SIGNALS THAT NORMALLY EMANATE FROM THE CONTROLLED DEVICE BE JUMPERED SUCH THAT THE SIGNAL IS ALWAYS TRUE. THIS JUMPERING IS IRED IF THE DEVICE DOES NOT PROVIDE THE SPECIFIED CONTROL SIGNAL. SW3 SED TO ACCOMPLISH THE JUMPERING. THE DEFINITION OF THE CONTROL SIGNAL DEPENDS ON WHETHER THE DEVICE IS A MODEM (DCE) OR A TERMINAL (DTE).

MODEM (DCE)

RECEIVED LINE SIGNAL (RLS) - THIS SIGNAL INDICATES THAT THE MODEM IS RECEIVING A VALID SIGNAL. IF THE MODEM TO BE UTILIZED DOES NOT PROVIDE THIS SIGNAL CONNECT SW3; PIN 7 TO PIN 8.

CLEAR TO SEND (CTS) - THIS SIGNAL INDICATES THAT THE MODEM IS READY TO TRANSMIT DATA TO THE TELETYPE LINE. IF THE MODEM DOES NOT PROVIDE THIS SIGNAL, CONNECT SW3; PIN 11 TO PIN 12.

TERMINAL (DTE)

DATA TERMINAL READY (DTR) - THIS SIGNAL INDICATES THAT THE TERMINAL IS READY TO TRANSMIT OR RECEIVE DATA. IF THE TERMINAL DOES NOT PROVIDE THIS SIGNAL, CONNECT SW3; PIN 7 TO PIN 8.

REQUEST TO SEND (RTS) - THIS SIGNAL INDICATES THAT THE TERMINAL IS READY TO RECEIVE DATA FROM THE CPU. IF THE TERMINAL DOES NOT PROVIDE THIS SIGNAL, CONNECT SW3; PIN 11 TO PIN 12

PERIPHERAL CONNECTOR

AT THE TIME OF ORDER, A DCE OR DTE CABLE AND CONNECTOR ASSEMBLY ARE SPECIFIED FOR INCLUSION WITH THIS MODULE. THESE ASSEMBLIES CONSIST OF A 10 -PIN CARD CONNECTOR, 15' CABLE, AND A 25 PIN RS232-C COMPATIBLE DEVICE CONNECTOR. A DCE (DATA COMMUNICATIONS EQUIPMENT) ASSEMBLY IS USED TO CONNECT TO A MODEM. A MALE DEVICE CONNECTOR IS SUPPLIED WITH THIS ASSEMBLY. A DTE (DATA TERMINAL EQUIPMENT) ASSEMBLY IS USED TO CONNECT TO A TERMINAL SUCH AS A CRT, TELETYPE, OR PRINTER. A FEMALE DEVICE CONNECTOR IS SUPPLIED WITH THIS ASSEMBLY.

THESE ASSEMBLIES ARE WIRED ACCORDING TO THE FOLLOWING TABLE:

CARD CONNECTOR PIN NO.	DCE RS232 MALE CONNECTOR	DTE RS232 FEMALE CONNECTOR
1	N/C	N/C
2	3-RD	2-TD
3	2-TD	3-RD
4	5-CTS	4-RTS
	4-RTS	5-CTS
	20-DTR	6-DSR
	7-SG	7-SG
8	8-RLS	20-DTR
9	N/C	8-RLS
10	N/C POLARIZED	N/C POLARIZED

THE ELECTRONIC INDUSTRIES ASSOCIATION HAS DEVISED A STANDARD INTERFACE SPECIFICATION PERTAINING TO DATA COMMUNICATION EQUIPMENT EMPLOYING A SERIAL INTERFACE. THE CURRENT VERSION OF THIS SPECIFICATION IS REFERRED TO AS "EIA STANDARD RS232-C". MOST DATA COMMUNICATION EQUIPMENT MANUFACTURED IN RECENT YEARS CONFORM TO THIS STANDARD. A NOTABLE EXCEPTION IS THE TELETYPE TERMINAL WHICH REQUIRES A SPECIAL ADAPTER TO BE RS232-C COMPATIBLE. THE RS232-C STANDARD DEFINES ALL INTERFACE SIGNAL ELECTRICAL AND FUNCTIONAL CHARACTERISTICS. THIS SECTION SUMMARIZES THE PORTIONS OF THE RS232-C STANDARD THAT ARE PERTINENT TO USE OF THIS MODULE. FOR A COMPLETE SPECIFICATION CONTACT:

EIA ENGINEERING DEPARTMENT
2001 EYE STREET, N.W.
WASHINGTON, D.C. 20006

THE STANDARD WAS ORIGINALLY DEFINED FOR CONNECTION OF REMOTE TERMINAL EQUIPMENT TO TELEPHONE LINES AND TREATS ALL DEVICES AS BEING EITHER DATA TERMINAL EQUIPMENT (DTE) OR DATA COMMUNICATION EQUIPMENT (DCE)

TERMINAL	MODEM	
DTE	DCE	COMMUNICATION CHANNEL

THEREFORE THE SERIAL DATA INTERFACE MODULE MAY BE TREATED AS EITHER DTE OR DCE DEPENDING ON THE CONFIGURATION:

	DCE	DTE
JUPITER II SYSTEM BUS	SERIAL DATA INTERFACE MODULE	TERMINAL

SERIAL DATA INTERFACE MODULE IS CONSIDERED DATA COMMUNICATION EQUIPMENT (DCE) WHEN INTERFACED TO A TERMINAL SUCH AS TELETYPE OR CRT.

	DTE	DCE	
JUPITER II SYSTEM BUS	SERIAL DATA INTERFACE MODULE	MODEM	COMMUNICATION CHANNEL

SERIAL DATA INTERFACE MODULE IS CONSIDERED DATA TERMINAL EQUIPMENT (DTE) WHEN INTERFACED TO A MODEM.

DIFFERENT SEX CONNECTORS AND DIFFERING PIN CONNECTIONS ARE SPECIFIED DEPENDING ON WHETHER A DEVICE IS SPECIFIED AS DTE OR DCE. DTE DEVICES UTILIZE MALE CONNECTORS WHILE DCE DEVICES USE FEMALE CONNECTORS.

PIN NUMBER	EIA CIRCUIT DESIGN	DESCRIPTION
1	AA	PROTECTIVE GROUND
2	BA	TRANSMITTED DATA
3	BB	RECEIVED DATA
4	CA	REQUEST TO SEND
5	CB	CLEAR TO SEND
6	CC	DATA SET READY
7	AB	SIGNAL GROUND (COMMON RETURN)
8	CF	RECEIVED LINE SIGNAL DETECTOR
9	-	(RESERVED FOR DATA SET TESTING)
10	-	(RESERVED FOR DATA SET TESTING)
11		UNASSIGNED (SEE SECTION 3.2.3)
12	SCF	SEC. REC'D. LINE SIG. DETECTOR

13	SCB	SEC. CLEAR TO SEND
14	SBA	SECONDARY TRANSMITTED DATA
15	DB	TRANSMISSION SIGNAL ELEMENT TIMING (DCE SOURCE)
16	SBB	SECONDARY RECEIVED DATA
17	DD	RECEIVER SIGNAL ELEMENT TIMING (DCE SOURCE)
18		UNASSIGNED
19	SCA	SECONDARY REQUEST TO SEND
20	CD	DATA TERMINAL READY
21	CG	SIGNAL QUALITY DETECTOR
22	CE	RING INDICATOR
23	CH/CI	DATA SIGNAL RATE SELECTOR (DTE/DCE SOURCE)
24	DA	TRANSMIT SIGNAL ELEMENT TIMING (DTE SOURCE)
25		UNASSIGNED

ELECTRICAL CHARACTERISTICS

THE VOLTAGES ON THE INTERFACE CIRCUITS MAY RANGE BETWEEN +25 VOLTS AND -25 VOLTS AND ARE DEFINED AS FOLLOWS:

DATA SIGNALS
TRUE (MARK) -3V TO -25V
FALSE (SPACE) +3V TO +25V

CONTROL SIGNALS
TRUE (ON) +3V TO +25V
FALSE (OFF) -3V TO -25V

THE REGION BETWEEN +3V AND -3V IS DEFINED AS THE TRANSITION REGION AND HAS NO LOGICAL DEFINITION. ALL SIGNALS ENTERING INTO THE TRANSITION REGION SHOULD PROCEED THROUGH THE TRANSISTION REGION TO THE OPPOSITE SIGNAL STATE AND SHOULD NOT REENTER THE TRANSITION REGION UNTIL THE NEXT SIGNIFICANT CHANGE OF SIGNAL CONDITION. THERE SHOULD BE NO REVERSAL OF THE DIRECTION OF VOLTAGE CHANGE WHILE THE SIGNAL IS IN THE TRANSITION REGION.

THE TIME REQUIRED FOR A CONTROL SIGNAL TO PASS THROUGH THE TRANSITION REGION SHOULD NOT EXCEED ONE MILLISECOND. THE TIME REQUIRED FOR A DATA SIGNAL TO PASS THROUGH THE TRANSITION REGION SHOULD NOT EXCEED ONE MILLISECOND OR 9 PERCENT OF THE BIT TIME, WHICHEVER IS GREATER.

DRIVER CIRCUITS

OUTPUT VOLTAGE
ABSOLUTE MAXIMUN: +=25 VOLTS
RANGE WHEN LOADED WITH 3K-7K OHMS: +=5V MINIMUM- +=15 V MAXIMUM

OUTPUT CURRENT
SHORT CIRCUIT MAXIMUM: 0.5 AMP

POWER OFF
OUTPUT IMPEDANCE MINIMUM: 300 OHMS

RECEIVER CIRCUITS

LOAD RESISTANCE: 3K OHM MINIMUM (@25V)- 7K OHM MAXIMUM (3-25V)

LOAD CAPACITANCE: 2500 PF MAXIMUN

LOAD INDUCTANCE: NONE ALLOWED

OPEN CONNECTION: INTERPRET AS OFF CONDITION

PROTECTIVE GROUND - CHASSIS GROUND

SIGNAL GROUND (SG) -

TRANSMITTED DATA (TD) - SERIAL DATA STREAM GENERATED BY DATA TERMINAL EQUIPMENT AND TRANSMITTED TO DATA COMMUNICATION EQUIPMENT. TD SHOULD NOT BE TRANSMITTED UNLESS THE FOLLOWING SIGNALS ARE ON (TRUE).

RTS	REQUEST TO SEND
CTS	CLEAR TO SEND
DSR	DATA SET READY
DTR	DATA TERMINAL READY

IT IS NOT NECESSARY FOR ALL FOUR OF THE ABOVE CONTROL SIGNALS TO BE IMPLEMENTED. THE TD LINE SHOULD BE IN THE TRUE (MARK) STATE WHEN NOT TRANSMITTING DATA.

RECEIVED DATA (RD) - SERIAL DATA STREAM RECEIVED FROM DATA COMMUNICATIONS EQUIPMENT OR TRANSMITTED TO DATA TERMINAL EQUIPMENT. RD SHOULD BE HELD IN THE TRUE (MARK) STATE WHEN THE RECEIVED LINE SIGNAL DETECTOR (RLS) SIGNAL IS OFF.

REQUEST TO SEND (RTS) - GENERATED BY TERMINAL TO NOTIFY COMMUNICATIONS EQUIPMENT THAT TERMINAL IS READY TO TRANSMIT DATA. THE DATA COMMUNICATIONS EQUIPMENT SHOULD RESPOND WITH CLEAR TO SEND (CTS) WHEN READY TO RECEIVE DATA FROM THE TERMINAL.

CLEAR TO SEND (CTS) - GENERATED BY DATA COMMUNICATION EQUIPMENT WHEN READY TO RECEIVE DATA FROM TERMINAL FOR TRANSMISSION.

DATA SET READY (DSR) - GENERATED BY DATA COMMUNICATION EQUIPMENT WHEN CONNECTED TO COMMUNICATION CHANNEL AND NOT IN TEST OR TALK MODE.

DATA TERMINAL READY (DTR) - GENERATED BY DATA TERMINAL EQUIPMENT TO INDICATE READY CONDITION.

RECEIVED LINE SIGNAL DETECTOR (RLS) - GENERATED BY DATA COMMUNICATION EQUIPMENT WHEN RECEIVING VALID SIGNAL FROM COMMUNICATION CHANNEL.

DETAILED THEORY OF OPERATION

ADDRESS SELECT LOGIC

THE ADDRESS SELECT LOGIC IS IMPLEMENTED USING IC5 AND PORTIONS OF SW1 AND SW2. THE INPUTS TO THE SWITCHES CONSIST OF THE ADDRESS LINES A1 - A7, AND THE ADDRESS DECODE LINES *A109 - *A715. SINCE THE MODULE TIMING IS CONTROLLED BY CLK2, ONLY THE LOW ORDER TERMS OF THE ADDRESS DECODE LINES (*A1 - *A7) ARE RELEVENT.

THE SWITCHES ARE USED TO SELECT THE TRUE (A1 - A7) OR COMPLEMENTED (*A1 - *A7) TERM OF EACH ADDRESS BIT FOR INPUT TO IC5.

IC5 FUNCTIONS AS AN 8 INPUT NAND GATE, GATING ADDRESS BITS A1 - A7 WITH IO. IO IS A SIGNAL GENERATED ON THE CPU CARD WHEN VMA (VALID MEMORY ADDRESS) AND THE HIGH ORDER 8 ADDRESS BIT ARE ALL TRUE. THIS CONDITION IS ONLY MET WHEN AN I/O DEVICE IS BEING ADDRESSED. THE OUTPUT OF THE ADDRESS SELECT LOGIC IC5-12 IS TRUE(0V) WHEN AN I/O ADDRESS CORRESPONDING TO THE SW1 AND SW2 JUMPERS APPEARS ON THE ADDRESS LINES.

REPLY GENERATOR

THE ADDRESS SELECTION LOGIC OUTPUT IC5-12 IS INVERTED (IC6-6) AND GATED WITH CLK2 TO FORM THE REPLY TERM (IC6-3) TRANSMITTED TO THE CPU MODULE. IC6 IS AN OPEN COLLECTOR DEVICE, MEANING THAT THE OUTPUTS REQUIRE EXTERNAL PULLUP RESISTORS FOR CORRECT OPERATION. THE PULLUP RESISTOR FOR *RPLY (IC6-3) IS LOCATED AT THE CIRCUIT TERMINATION ON THE CPU MODULE.

ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (ACIA)

THE ACIA IS A MOTROLA MC6850 LSI CHIP CONTAINING THE FOLLOWING FUNCTIONAL ELEMENTS:

SELECTION AND CONTROL

DATA BUS BUFFERS

TRANSMITTER

RECEIVER

STATUS REGISTER

CONTROL REGISTER

A TYPICAL TRANSMITTING SEQUENCE CONSISTS OF READING THE STATUS REGISTER EITHER AS A RESULT OF AN INTERRUPT OR A POLLING SEQUENCE. A CHARACTER MAY BE WRITTEN INTO THE /TRANSMIT /DATA /REGISTER IF THE STATUS READ OPERATION HAS INDICATED THAT THE /TRANSMIT /DATA /REGISTER IS EMPTY. THIS CHARACTER IS TRANSFERRED TO A /SHIFT /REGISTER WHERE IT IS SERIALIZED AND TRANSMITTED FROM THE TRANSMIT DATA OUTPUT PRECEDED BY A START BIT AND FOLLOWED BY ONE OR TWO STOP BITS. INTERNAL PARITY (ODD OR EVEN) CAN BE OPTIONALLY ADDED TO THE CHARACTER AND WILL OCCUR BETWEEN THE LAST DATA BIT AND THE FIRST STOP BIT. AFTER THE FIRST CHARACTER IS WRITTEN IN THE /DATA /REGISTER, THE STATUS REGISTER CAN BE READ AGAIN TO CHECK FOR A /TRANSMIT /DATA /REGISTER /EMPTY CONDITION AND CURRENT PERIPHERAL STATUS. IF THE REGISTER IS EMPTY, ANOTHER CHARACTER CAN BE LOADED FOR TRANSMISSION EVEN THOUGH THE FIRST CHARACTER IS IN THE PROCESS OF BEING TRANSMITTED (BECAUSE OF DOUBLE BUFFERING). THE SECOND CHARACTER WILL BE AUTOMATICALLY TRANSFERRED INTO THE SHIFT REGISTER WHEN THE FIRST CHARACTER TRANSMISSION IS COMPLETED. THIS SEQUENCE CONTINUES UNTIL ALL THE CHARACTERS HAVE BEEN TRANSMITTED.

DATA IS RECEIVED FROM A PERIPHERAL BY MEANS OF THE RECEIVE DATA INPUT. A DIVIDE BY 16 RATIO OF CLOCK INPUT TO BAUD RATE IS UTILIZED FOR BIT SYNCHRONIZATION. BIT SYNCHRONIZATION IS INITIATED BY THE DETECTION OF THE LEADING MARK-TO-SPACE TTRANSITION OF THE START BIT. FALSE START BIT DELETION CAPABILITY INSURES THAT A FULL HALF BIT OF A START BIT HAS BEEN RECEIVED BEFORE THE INTERNAL CLOCK IS SYNCHRONIZED TO THE BIT TIME. AS A CHARACTER IS BEING RECEIVED, PARITY (ODD OR EVEN) WILL BE CHECKED AND THE ERROR INDICATION WILL BE AVAILABLE IN THE STATUS REGISTER ALONG WITH FRAMING ERROR, OVERRUN ERROR, AND /RECEIVE /DATA /REGISTER FULL. IN A TYPICAL RECEIVING SEQUENCE, THE STATUS REGISTER IS READ TO DETERMINE IF A CHARACTER HAS BEEN RECEIVED FROM PERIPHERAL. IF THE RECEIVER DATA REGISTER IS FULL, THE CHARACTER IS PLACED ON THE 8-BIT DATA BUS WHEN A READ DATA COMMAMD IS RECEIVED FROM THE CPU. WHEN PARITY HAS BEEN SELECTED FOR AN 8-BIT WORD (7 BITS PLUS PARITY), THE RECEIVER STRIPS THE PARITY BIT (D7 = 0) SO THAT DATA ALONE IS TRANSFERRED TO THE CPU. THE STATUS REGISTER CAN CONTINUE TO BE READ AGAIN TO DETERMINE WHEN ANOTHER CHARACTER IS AVAILABLE IN THE /RECEIVE /DATA /REGISTER. THE RECEIVER IS ALSO DOUBLE BUFFERED SO THAT A CHARACTER CAN BE READ FROM THE DATA REGISTER AS ANOTHER CHARACTER IS BEING RECEIVED IN THE SHIFT REGISTER. THE ABOVE SEQUENCE CONTINUES UNTIL ALL CHARACTERS HAVE BEEN RECEIVED.

THE ACIA INTERFACES TO THE SYSTEM WITH AN 8-BIT BI-DIRECTOINAL DATA BUS, THREE CHIP SELECT LINES, A REGISTER SELECT LINE, AN INTERRUPT REQUEST LINE, READ/WRITE LINE, AND ENABLE LINE.

DATA (D0-D7) - THE BI-DIRECTIONAL DATA LINES (D0-D7) ALLOW FOR DATA TRANSFER BETWEEN THE ACIA AND THE CPU. THE DATA BUS OUTPUT DRIVERS ARE THREE-STATE DEVICES THAT REMAIN IN THE HIGH-IMPEDANCE (OFF STATE EXCEPT WHEN THE CPU PERFORMS AN ACIA READ OPERATION.

ENABLE (E) - ENABLES THE BUS INPUT/OUTPUT DATA BUFFERS AND CLOCKS DATA TO AND FROM THE ACIA.

READ/WRITE (R/W) - THE READ/WRITE LINE IS USED TO CONTROL THE DIRECTION OF DATA FLOW THROUGH THE ACIS'S INPUT/OUTPUT DATA BUS INTERFACE. WHEN READ/WRITE IS HIGH (CPU READ CYCLE), ACIA OUTPUT DRIVERS ARE TURNED ON AND A SELECTED REGISTER IS READ. WHEN IT IS LOW, THE ACIA OUTPUT DRIVERS ARE TURNED OFF AND THE CPU WRITES INTO A SELECTED REGISTER. THEREFORE, THE READ/WRITE SIGNAL IS USED TO SELECT READ-ONLY REGISTERS WITHIN THE ACIA.

CHIP SELECT (CS0, CS1, CS2) - THESE LINES ARE USED TO ADDRESS THE ACIA. IN THIS SYSTEM CS2 IS DRIVEN BY THE OUTPUT OF THE ADDRESS SELECT LOGIC (IC9-12) CS0 AND CS1 ARE TIED TO +5V (TRUE).

REGISTER SELECT (RS) - A HIGH LEVEL IS USED TO SELECT THE TRANSMIT/RECEIVE DATA REGISTERS AND A LOW LEVEL THE CONTROL/STATUS REGISTERS. THE READ/WRITE SIGNAL LINE IS USED IN CONJUNCTION WITH REGISTER SELECT TO SELECT THE READ-ONLY OR WRITE-ONLY REGISTER IN EACH REGISTER PAIR.

INTERRUPT REQUEST (IRQ) - THE INTERRUPT REQUEST IS SET WHEN THE ACIA IS READY TO RECEIVE ANOTHER CAHARACTER FOR TRANSMISSION, OR TO INPUT A RECEIVED CHARACTER TO THE CPU. THE INTERRUPT REQUEST REMAINS LOW AS LONG AS THE APPROPRIATE INTERRUPT ENABLE WITHIN THE ACIA IS SET.

TRANSMIT CLOCK (TX CLK) - THE TRANSMIT CLOCK INPUT IS USED FOR THE CLOCKING OF TRANSMITTED DATA. THE TRANSMITTER INITIATES DATA ON THE NEGATIVE TRANSITION OF THE CLOCK.

RECEIVE CLOCK (TX CLK) - THE RECEIVE CLOCK INPUT IS USED FOR SYNCHRONIZATION OF RECEIVED DATA. THE RECEIVER SAMPLES THE DATA ON THE POSITIVE TRANSITION OF THE CLOCK.

SERIAL INPUT/OUTPUT LINES

RECEIVE DATA (TX DATA) - THE RECEIVE DATA LINE IS THE INPUT THROUGH WHICH DATA IS RECEIVED IN A SERIAL FORMAT. SYNCHRONIZATION WITH A CLOCK FOR DETECTION OF DATA IS ACCOMPLISHED INTERNALLY.

TRANSMIT DATA (TX DATA) - THE TRANSMIT DATA OUTPUT LINE TRANSFERS SERIAL DATA TO A MODEM OR OTHER PERIPHERAL.

THE DRIVER CIRCUITS ARE DESIGNED TO CONVERT THE TTL LOGIC LEVELS USED WITHIN THE MODULE TO THE RS232-C SPECIFIED LEVELS. THE DRIVERS ACT AS INVERTERS GENERATING THE FOLLOWING OUTPUT LEVELS:

INPUT	OUTPUT
0V	+10V
+5V	-9V

THE DRIVER OUTPUT SLEW RATE (VOLTS/MICROSECONDS) IS A FUNCTION OF THE CAPACITANCE BETWEEN THE DRIVER OUTPUT AND SIGNAL GROUND. UNDER CERTAIN CONDITIONS IT MAY BE NECESSARY TO ADD AN EXTERNAL CAPACITOR TO MEET THE RS232-C MAXIMUM SPECIFIED 30 VOLT/MICROSECOND SLEW RATE.

CAPACITANCE TO GROUND PF	OUTPUT SLEW RATE VOLTS/MICROSECONDS
10	1000
100	100
30	30
1000	10

THE INPUTS TO TWO OF THE DRIVERS (IC3-4 AND IC3-2) ARE GROUNDED HOLDING THE CORRESPONDING OUTPUTS TRUE. THESE OUTPUTS ARE USED TO NOTIFY THE INTERFACED DEVICE THAT THE MODLUE IS IN A READY STATE.

THE RECEIVER CIRCUITS INVERT THE INPUT SIGNALS AND CONVERT THE RS232-C LOGIC LEVELS TO TTL COMPATIBLE SIGNALS:

RECEIVER INPUT	RECEIVER OUTPUT
-3V TO -25V	+5V
+3V TO +25V	0V

NOTE: 0V AND +5V ARE USED THROUGHOUT THIS MANUAL TO DESIGNATE LOW AND HIGH SIGNAL LEVELS. IN ACTUAL CIRCUIT OPERATION A LOW SIGNAL MAY RANGE BETWEEN 0V AND +0.8 WHILE A HIGH SIGNAL WILL RANGE BETWEEN +3V AND +5V.

EACH OF THE RECEIVER CIRCUITS UTILIZE A FEEDBACK CAPACITOR TO FILTER HIGH FREQUENCY NOISE PULSES.

RECEIVER OUTPUTS IC4-3 AND IC4-6 MAY BE JUMPERED THROUGH SW3 TO GROUND HOLDING THESE SIGNALS IN A TRUE STATE. REFER TO THE OPERATION SECTION FOR DETAILS ON USE OF THESE JUMPERS.

CLOCK

THE CLOCK CIRCUIT UTILIZES AN LSI CHIP (IC2) AND ON EXTERNAL TIMING CIRCUIT TO GENERATE THE RECEIVE AND TRANSMIT CLOCK SIGNALS REQUIRED BY IC1. IC2 IS A FAIRCHILD CMOS, 34702 PROGRAMMABLE BIT RATE GENERATOR. THE EXTERNAL CRYSTAL TIMING RESISTOR AND CAPACITORS ARE USED BY AN OSCILLATOR CIRCUIT WITHIN IC2 TO GENERATE A 2.4576 MHZ TIMING SIGNAL. THIS SIGNAL IS COUNTED DOWN BY A SERIES OF COUNTERS WITHIN IC2. INPUTS S0 -S3 DETERMINE WHICH POINT IN THE COUNTER CHAIN IS GATED TO THE OUTPUT (IC2-12). THIS OUTPUT WHICH DRIVES (IC1-3 AND IC1-4) IS 16 TIMES THE SELECTED BAUD RATE:

S3 IC2-13	S2 IC2-14	S1 IC2-15	S0 IC2-16	OUTPUT IC2-12	BAUD RATE
0	0	0	0	0	OFF
0	0	0	+5	0	OFF
0	0	+5	0	800	50
0	0	+5	+5	1200	75
0	+5	0	0	2152	134.5
0	+5	0	+5	3200	200
0	+5	+5	0	9600	600
0	+5	+5	+5	38400	2400
+5	0	0	0	153600	9600
+5	0	0	+5	76800	4800
+5	0	+5	0	28800	1800
+5	0	+5	+5	19200	1200
+5	+5	0	0	38400	2400
+5	+5	0	+5	4800	300
+5	+5	+5	0	2400	150
+5	+5	+5	+5	1760	110

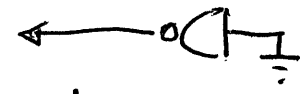
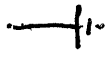
Dual Serial Interface

Console Device = .FFC0, .FFC1

Modem Device = .FFC4, .FFC5

11/25/82

Jupiter Serial port 10 pin connector

1	N.C.	
2	→	ACIA RXD
3	←	ACIA TXD
4	→	ACIA CTS'
5	←	ACIA RTS'
6	←	
7	—	
8	→	ACIA DCD
9	←	
10	N.C.	