CPU-125 CENTRAL PROCESSOR UNIT MODULE

THEORY AND OPERATION MANUAL

WAVE MATE COMPUTERS AND SYSTEMS
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SECTION 1 INTRODUCTION

THE CPU-125 CENTRAL PROCESSING UNIT MODULE CONTAINS THE MICROPROCESSOR INTEGRATED CIRCUIT AND VARIOUS OTHER TIMING AND CONTROL CIRCUITS REQUIRED TO IMPLEMENT THE WAVE MATE JUPITER II COMPUTER SYSTEM.

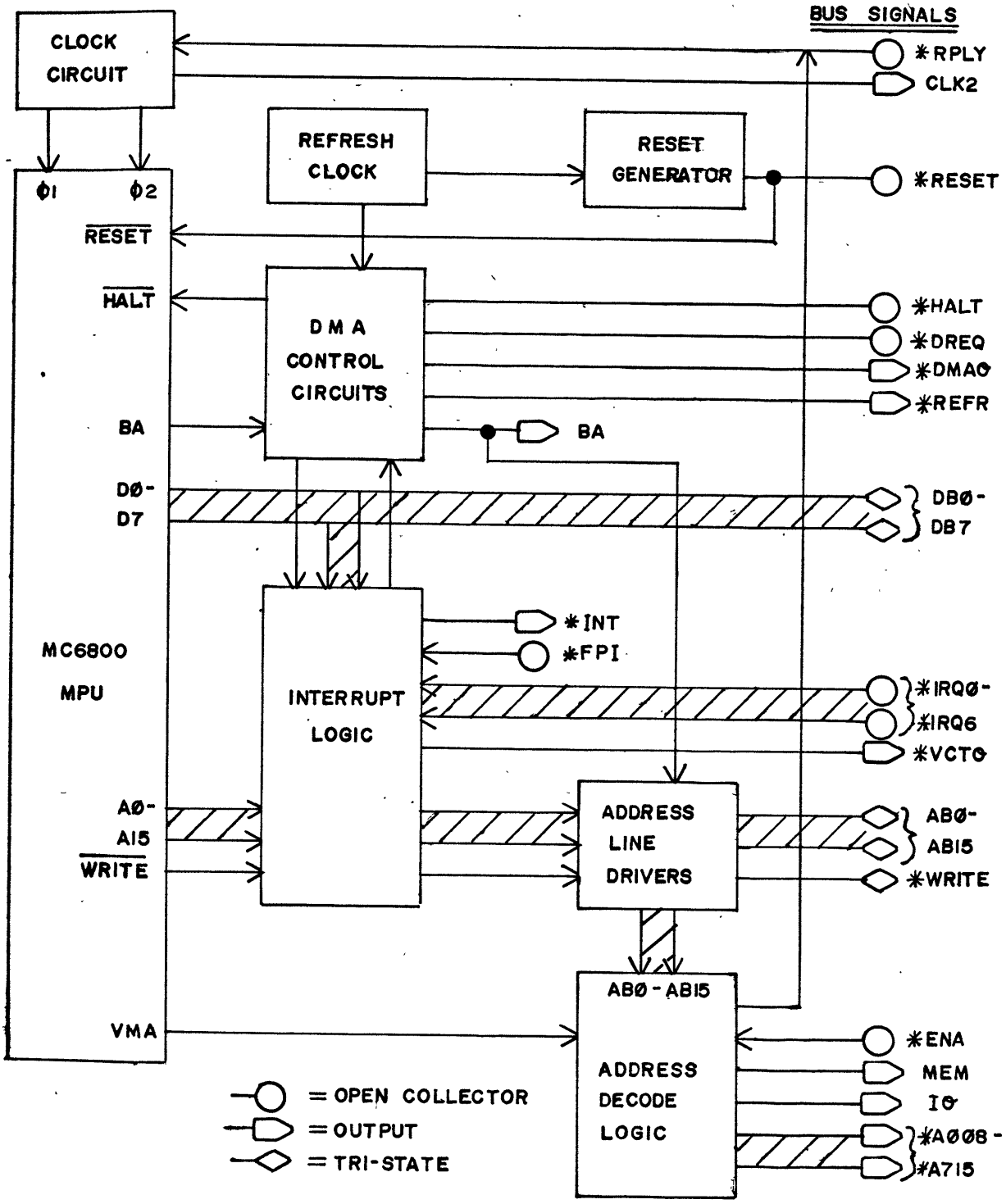
THE CENTRAL PROCESSING UNIT PROVIDES SEVERAL FEATURES THAT ENHANCE THE OPERATION OF THE MICROPROCESSOR:

THE ADDRESS DECODE LOGIC PROVIDES AN I/O ADDRESS NOTIFICATION SIGNAL AND COMPLEMENTED I/O ADDRESS LINES SIMPLIFYING PERIPHERAL DEVICE INTERFACING LOGIC.

THE DMA CONTROL LOGIC PROVIDES AN EXTERNAL DEVICE OPTION OF REQUESTING A BLOCK TRANSFER OR A SINGLE DMA CYCLE. THIS FEATURE PREVENTS DEVICES FROM MONOPOLIZING CPU TIME.

THE INTERRUPT LOGIC PROVIDES 8 LEVELS OF PRIORITY INTERRUPTS. ANY OR ALL OF THESE LEVELS (EXCEPT THE HIGHEST LEVEL) MAY BE MASKED UNDER SOFTWARE CONTROL.

THE BLOCK DIAGRAM ILLUSTRATES THE MAJOR FUNCTIONAL COMPONENTS OF THE CENTRAL PROCESSING UNIT MODULE.



CPU-125 CENTRAL PROCESSING UNIT MODULE BLOCK DIAGRAM

2.1 MC6800 MICROPROCESSOR

THE MICROPROCESSOR IS THE HEART OF THE JUPITER II COMPUTER SYSTEM. THE MICROPROCESSOR IS A MOTOROLA MC6800 UNIT CONTAINING THE FOLLOWING MAJOR COMPONENTS:

INSTRUCTION DECODE AND CONTROL

DATA BUFFERS - 8 LINES, BIDIRECTIONAL

ADDRESS OUTPUT BUFFERS - 16 LINES

INTERRUPT PROCESSING CONTROL - MASKABLE AND NON-MASKABLE

DIRECT MEMORY ACCESS CONTROL

PROGRAM COUNTER - 16 BITS

STACK POINTER - 16 BITS

INDEX REGISTER - 16 BITS

ACCUMULATORS - 2 @ 8 BITS

CONDITION CODE REGISTER

OPERATION OF THE MICROPROCESSOR IS DESCRIBED IN DETAIL IN CHAPTERS 1, 2, 4 AND APPENDIX A OF THE MOTOROLA M6800 MICROPROCESSOR APPLICATIONS MANUAL SUPPLIED WITH THIS MODULE.

2.2 CLOCK CIRCUIT

THE CLOCK CIRCUIT PROVIDES THE BASIC TIMING SIGNALS FOR THE JUPITER II SYSTEM. THE SYSTEM UTILIZES TWO BASIC CLOCK PERIODS. THE PHASE 1 CLOCK IS USED FOR MICROPROCESSOR OPERATION AND TO PUT ADDRESS AND CONTROL SIGNALS ON THE SYSTEM BUS. DATA IS TRANSFERRED DURING THE PHASE 2 CLOCK PERIOD. THE PHASE 1 CLOCK PERIOD IS SET AT 0.5 MICROSECONDS. THE PHASE 2 CLOCK PERIOD CAN AUTOMATICALLY VARY FROM 0.5 MICROSECONDS TO 3.5 MICROSECONDS.

NORMALLY, A SELECTED DEVICE OR MEMORY WILL COMPLEMENT THE PHASE 2 CLOCK SIGNAL AND SEND IT BACK TO THE CPU OVER THE REPLY LINE. THE DELAY TIME BETWEEN THE PHASE 2 CLOCK AND THE REPLY SIGNAL WILL BE ADDED TO THE NORMAL 0.5 MICROSECOND CLOCK TIME. IF THE DEVICE IS LOCATED THROUGH A BUS BUFFERING CIRCUIT, THE DELAY INCURRED BY THE ADDITIONAL DATA BUFFERING CIRCUITRY WILL AUTOMATICALLY BE COMPENSATED FOR. A DEVICE MAY PURPOSEFULLY IMPOSE A DELAY TO THE REPLY SIGNAL TO SLOW DOWN THE DATA TRANSFER IF IT IS UNABLE TO RESPOND AT A 0.5 MICROSECOND RATE. A DUMMY REPLY SIGNAL IS GENERATED TO CAUSE THIS TIMEOUT SPEEDUP IF THE INSTRUCTION BEING EXECUTED DOES NOT REFERENCE I/O DEVICES OR MEMORY.

2.3 REFRESH CLOCK

THE REFRESH CLOCK GENERATES A TIMING SIGNAL AT 32 MICROSECOND INTERVALS. THIS SIGNAL IS USED BY THE DMA CONTROL CIRCUITS TO GENERATE THE SIGNALS REQUIRED TO REFRESH THE SYSTEM'S DYNAMIC MEMORY MODULES.

2.4 DMA CONTROL CIRCUITS

THE DMA CONTROL CIRCUITS PROVIDE THE LOGIC AND SYNCHRONIZATION SIGNALS REQUIRED TO ENSURE RELIABLE DMA OPERATION. THE DMA CONTROL CIRCUITS EXPAND THE BASIC DMA CAPABILITY OF THE MPU CHIP BY ADDING A SINGLE CYCLE DMA OPERATION. THE DMA CONTROL CIRCUITS ALSO CONTROL MEMORY REFRESH OPERATION BY GENERATING A SINGLE DMA CYCLE WHEN REQUESTED BY THE REFRESH CLOCK.

2.5 INTERRUPT LOGIC

THE INTERRUPT LOGIC ENHANCES THE I/O PROCESSING CAPABILITY OF THE MICROPROCESSOR CHIP BY ADDING HARDWARE PRIORITIZING, VECTORING AND PROGRAMMABLE MASKING CAPABILITY.

A TOTAL OF 8 INTERRUPT LEVELS ARE PROVIDED. EACH OF THESE LEVELS IS ASSIGNED AN INDIVIDUAL PRIORITY AND WHEN RECOGNIZED, CAUSES THE GENERATION OF A UNIQUE VECTOR ADDRESS. THIS VECTOR ADDRESS CONTAINS THE LOCATION OF THE SERVICE ROUTINE FOR THE SPECIFIED INTERRUPT LEVEL. THE HIGHEST PRIORITY INTERRUPT LEVEL (*FPI) IS ASSIGNED TO THE FRONT PANEL "INT" SWITCH. THIS FEATURE ASSURES THAT AN INTERRUPT MAY ALWAYS BE TRIGGERED BY THE FRONT PANEL SWITCH, INDEPENDENT OF THE STATUS OF THE OPERATING SOFTWARE.

THE INTERRUPT REQUEST PRIORITIES ARE:

INTERRUPT LEVEL	PRIORITY
*FPI	1 (HIGHEST)
*IRQ6	2
*IRQ5	3
*IRQ4	4
*IRQ3	5
*IRQ2	6
*IRQ1	7
*IRQ0	8 (LOWEST)

ANY OF THE INTERRUPT LEVELS ASSIGNED TO I/O DEVICES (*IRQ0-*IRQ6) MAY BE MASKED UNDER SOFTWARE CONTROL. MASKING CAN BE ACCOMPLISHED BY OUTPUTTING A MASK WORD TO MEMORY ADDRESS FFFC. WHEN AN INTERRUPT IS SERVICED, THE MASK WORD REGISTER IS MODIFIED BY THE INTERRUPT LOGIC AND ALL 8 INTERRUPT LEVELS ARE TURNED OFF. THEREFORE EACH INTERRUPT SERVICE ROUTINE MUST OUTPUT AN APPROPRIATE MASK WORD BEFORE TERMINATION TO REENABLE ONE OR MORE INTERRUPT LEVELS. THE INTERRUPT MASK VALUES ARE:

INTERRUPT MASK VALUE	INTERRUPT LEVELS MASKED
0	*IRQ0-*IRQ6
1	*IRQ0-*IRQ5
2	*IRQ0-*IRQ4
3	*IRQ0-*IRQ3
4	*IRQ0-*IRQ2
5	*IRQ0-*IRQ1
6	*IRQ0
7	NONE

ALL HARDWARE INTERRUPTS ARE PROCESSED THROUGH THE MICROPROCESSOR'S NON-MASKABLE INTERRUPT LINE. THEREFORE THE INTERRUPT MASK IN THE CONDITION CODE REGISTER WILL NOT DISABLE HARDWARE INTERRUPTS. THESE INTERRUPTS CAN ONLY BE MASKED BY WRITING THE MASK VALUE TO MEMORY LOCATION FFFC. AFTER WRITING THE MASK VALUE, ONE ADDITIONAL INSTRUCTION WILL BE EXECUTED BEFORE THE NEW MASK VALUE WILL TAKE EFFECT. THE MICROPROCESSOR SOFTWARE INTERRUPT INSTRUCTION "SWI" IS UNAFFECTED BY THE INTERRUPT MASK VALUE.

THE VECTOR ADDRESS GENERATED BY EACH INTERRUPT LEVEL IS:

INTERRUPT LEVEL	VECTOR ADDRESS
0	FFEE-FFEF
1	FFEC-FFED
2	FFEA-FFEB
3	FFE8-FFE9
4	FFE6-FFE7
5	FFE4-FFE5
6	FFE2-FFE3
*FPI	FFE0-FFE1

IF A HARDWARE INTERRUPT REQUEST IS RECEIVED WHILE A SOFTWARE INTERRUPT IS BEING EXECUTED, THE MICROPROCESSOR WILL GENERATE AN IRQ ADDRESS VECTOR (FFF8 AND FFF9) RATHER THAN A SOFTWARE OR NON-MASKABLE INTERRUPT VECTOR.

IF AN INTERRUPT REQUEST IS RECEIVED DURING A HALT PERIOD, AFTER THE HALT IS REMOVED ONE INSTRUCTION WILL BE EXECUTED BEFORE THE INTERRUPT IS RECOGNIZED. AN INTERRUPT WILL ALWAYS BE RESPONDED TO WITHIN TWO INSTRUCTION TIMES NO MATTER WHAT THE CIRCUMSTANCES ARE.

2.6 ADDRESS LINE DRIVERS

THESE CIRCUITS ARE TRI-STATE DRIVERS PROVIDED TO ENHANCE THE DRIVE CAPABILITIES OF THE 16 ADDRESS LINES ON THE SYSTEM BUS. TRI-STATE DRIVERS ARE ACTIVE IN BOTH THE HIGH AND LOW OUTPUT STATES, AND HAVE A THIRD OFF STATE IN WHICH THEY PRESENT A HIGH IMPEDANCE TO THE OUTPUT LINE.

2.7 RESET GENERATOR

THIS CIRCUIT PROVIDES A RESET SIGNAL WHEN SYSTEM POWER IS FIRST APPLIED. THIS SIGNAL IS USED BY THE MICROPROCESSOR AND PERIPHERAL DEVICES TO INSURE AN ORDERLY STARTUP. IN ADDITION, THE RESET GENERATOR MONITORS THE REFRESH CLOCK TIMING SIGNAL. IF A REFRESH TIMING PULSE IS NOT ISSUED AT LEAST ONCE EVERY 100 MICROSECONDS, A RESET SIGNAL IS GENERATED RESTARTING THE ENTIRE SYSTEM.

2.8 ADDRESS DECODE LOGIC

THE ADDRESS DECODE LOGIC IS UTILIZED TO REDUCE THE NUMBER OF ADDRESS LINES THAT MUST BE BUFFERED AND DECODED BY A PERIPHERAL DEVICE CONTROLLER. EIGHT ADDRESS DECODE LINES ARE PROVIDED. WHEN AN I/O DEVICE IS BEING ADDRESSED, THE COMPLEMENT OF THE LOW ORDER ADDRESS SIGNALS AND AN IO CONTROL SIGNAL ARE GATED ONTO THE SYSTEM BUS. WHEN MEMORY IS BEING ADDRESSED, THE COMPLEMENT OF THE HIGH ORDER ADDRESS LINES AND A MEM CONTROL SIGNAL ARE GATED ONTO THE SYSTEM BUS.

2.9 FRONT PANEL CONNECTOR

PROVIDES SIGNALS AND CONTROL LINES REQUIRED FOR FRONT PANEL DISPLAYS AND SWITCHES. SIGNALS CARRIED TO THE FRONT PANEL INCLUDE:

ADDRESS LINES AB0-AB15
*FPI
*RESET
*INT
*HALT
BA
+5 VOLTS
CLK2
SIGNAL GROUND

3.1 MICROPROCESSOR

THE CPU CHIP (IC1) IS A MOTOROLA MC6800 MICROPROCESSER.

THE FOLLOWING PARAGRAPHS DESCRIBE THE FUNCTIONS OF THE MC6800 INPUT AND OUTPUT SIGNALS.

3.1.1 CLOCKS PHASE ONE AND PHASE TWO - TWO PINS ARE USED FOR A TWO-PHASE NON-OVERLAPPING CLOCK THAT RUNS AT THE VCC VOLTAGE LEVEL. THE PHASE ONE CLOCK IS USED INTERNALLY. THE PHASE TWO CLOCK TRANSFERS DATA BETWEEN MEMORY, PERIPHERALS AND THE MICROPROCESSOR.

3.1.2 RESET - THIS INPUT IS USED TO RESET AND START THE MICROPROCESSOR FROM A POWER DOWN CONDITION, RESULTING FROM A POWER FAILURE OR AN INITIAL START-UP OF THE PROCESSOR. IF A POSITIVE EDGE IS DETECTED ON THE INPUT THIS WILL SIGNAL THE MICROPROCESSOR TO BEGIN THE RESTART SEQUENCE.

3.2 CLOCK CIRCUIT (SHEET 1)

THE CLOCK CIRCUIT UTILIZES IC2 AS THE TIMING ELEMENT. IC2 IS A DUAL MONOSTABLE MULTIVIBRATOR (ONE-SHOT CIRCUITS). THE PULSE WIDTH OF EACH ONE-SHOT IS A FUNCTION OF THE CAPACITOR CONNECTED ACROSS PINS 1 AND 2 (OR 14 AND 15) AND THE RESISTANCE FROM PIN 2 (15) TO +5 VOLTS. THE PULSE WIDTH IS DEFINED AS:

$T = 0.31\ RC\ (1 + 1/R)$

WHERE R = KOHMS
C = PF (MUST BE LESS THAN 1000PF)
T = NSEC

EACH ONE-SHOT IS TRIGGERED BY A POSITIVE EDGE AT PIN 4 OR PIN 14. IC2-7 IS THE LOW TRUE (0V) OUTPUT OF THE PHASE 1 CLOCK. IC2-11 IS THE LOW TRUE (0V) OUTPUT OF THE PHASE 2 (CLK2) CLOCK.

THE PULSE WIDTH OF THE PHASE 1 CLOCK IS 0.5 MICROSECOND.

THE TIME CONSTANT OF THE PHASE 2 CLOCK IS DETERMINED BY THE STATUS OF *RPLY. IF *RPLY IS FALSE (+5V), IC14-2 IS LOW (0V) AND THE PULSE WIDTH IS DETERMINED BY R2 (3.5 MICROSECONDS). WHEN THE *RPLY SIGNAL GOES TRUE (0V), IC14-2 GOES HIGH AND THE PULSE WIDTH IS DETERMINED BY R3 (IN PARALLEL WITH R2). THE BACK-TO-BACK DIODE COMBINATION D1, D2 KEEPS THE OUTPUT IC14-2 FROM INTERFERING WITH THE R/C TIME CONSTANT OF R2, R3, AND C2.

THE INVERTED PHASE 1 (IC2-7) AND PHASE 2 (IC2-11) SIGNALS DRIVE THE CLOCK INPUT OF THE MICROPROCESSOR (IC1 PINS 3 AND 37) THROUGH THE INVERTING POWER DRIVER CIRCUITS IC21 (PINS 3 AND 15).

3.3 REFRESH CLOCK (SHEET 1)

THE REFRESH CLOCK CIRCUITRY UTILIZES IC22, THE LEFT HALF OF IC10, AND A PORTION OF IC23 TO GENERATE THE REFRESH REQUEST SIGNAL.

THE BASIC REFRESH CLOCK TIMING IS PERFORMED BY IC22. IC22 IS A TIMING CIRCUIT CONNECTED IN AN OSCILLATOR. THE FREQUENCY OF OSCILLATION AND DUTY CYCLE ARE DETERMINED BY C3, R4, AND R5. THE OSCILLATOR IS SET UP TO OUTPUT A 23 MICROSECOND PULSE AT A 31 MICROSECOND RATE.

THE OSCILLATOR OUTPUT (IC22-3) DRIVES IC10-4. IC10 IS A MONOSTABLE MULTIVIBRATOR (ONE-SHOT). SINCE TIMING ELEMENTS ARE NOT CONNECTED TO IC10 (PINS 1 AND 2), THIS CIRCUIT ACTS AS AN EDGE-TRIGGERED SET/RESET FLIP-FLOP. IC10 IS SET BY THE LEADING EDGE OF THE REFRESH CLOCK SIGNAL (IC22-3). THE OUTPUT OF IC10 (IC10-6) IS INPUT TO THE DMA CONTROL CIRCUIT IC3 (PINS 1 AND 4). IC10-6 ALSO IS INVERTED (IC23 PINS 4, 5, AND 6) AND INPUT TO THE DMA CONTROL CIRCUIT (IC11-13) WHERE IT IS CONNECTED IN A WIRED "OR" CONFIGURATION TO *DREQ. THE DMA CONTROL CIRCUIT HALTS THE MICROPROCESSOR AND GENERATES THE REFRESH SIGNAL (*REFR). WHEN GENERATED, *REFR (IC20-11) RESETS IC10-3 (LEFT SIDE).

3.4 DMA CONTROL CIRCUITS (SHEET 1)

THE DMA CONTROL CIRCUITS GENERATE ALL SIGNALS REQUIRED TO CONTROL DIRECT MEMORY ACCESS OPERATION. A DMA OPERATION CAN BE GENERATED BY ONE OF 3 EVENTS:

*DREQ - THIS SIGNAL FROM AN EXTERNAL DEVICE REQUESTS A SINGLE CPU CYCLE.

*HALT - THIS SIGNAL FROM AN EXTERNAL DEVICE REQUESTS AN UNDEFINED NUMBER OF CPU CYCLES. WHEN GRANTED THE CPU WILL REMAIN IN THE DMA (HALT) MODE UNTIL THE *HALT LINE IS RELEASED (GOES HIGH) BY THE DEVICE.

REFRESH CLOCK - THE SIGNAL FROM THE REFRESH CLOCK REQUESTS A SINGLE CPU CYCLE.

THE DMA CONTROL CIRCUITS GENERATE THE FOLLOWING CONTROL SIGNALS:

*HALT - THIS SIGNAL TO THE MPU CHIP HALTS ALL MPU ACTIVITY TO ALLOW DMA OPERATION.

*DMAO - THIS SIGNAL IS PRIORITY CHAINED TO ALL DEVICES CAPABLE OF GENERATING DMA TRANSFERS. THIS SIGNAL NOTIFIES THE DEVICE THAT A DMA REQUEST HAS BEEN GRANTED. IF THE FIRST DEVICE IS NOT REQUESTING DMA OPERATION THE SIGNAL IS PASSED TO THE NEXT DEVICE IN THE CHAIN.

*REFR - THIS SIGNAL TRIGGERS A REFRESH OPERATION IN ALL DYNAMIC MEMORY MODULES.

IC3 CONTAINS FOUR 2-INPUT MULTIPLEXERS WITH STORAGE. THE SELECT INPUT (IC3-12) DETERMINES WHETHER THE "1" OR "2" INPUT OF EACH CIRCUIT IS TO BE SELECTED. A NEGATIVE GOING EDGE AT THE CLOCK PULSE INPUT (IC3-13) STROBES THE SELECTED INPUT TO THE STORAGE FLIP-FLOP. THE OUTPUT (Q) REPRESENTS THE STORAGE FLIP-FLOP.

IN THIS CIRCUIT THE CLOCKING IS PERFORMED BY THE LEADING EDGE OF THE PHASE 1 CLOCK. THE "1" INPUT TO THE "C" MULTIPLEXER (IC3-11) IS THE HALT "OR" DREQ SIGNAL. IF NEITHER OF THESE TERMS ARE TRUE AT THE BEGINNING OF THE PHASE 1 CLOCK, THE OUTPUT OF THE "C" MULTIPLEXER (IC3-15) WILL BE LOW. WHEN EITHER OF THESE TERMS BECOME TRUE, IC3-15 WILL GO TRUE (+5V) AFTER THE NEXT LEADING EDGE OF THE PHASE 1 CLOCK. IC3-15 IS USED TO DRIVE THE SELECT INPUT (IC3-12). WHEN IC3-15 GOES TRUE, THE NEXT LEADING EDGE OF THE PHASE 1 CLOCK WILL CAUSE THE "2" INPUT OF EACH OF THE FOUR MULTIPLEXER CIRCUITS TO BE SELECTED.

THE "2" INPUTS WILL REMAIN SELECTED UNTIL IC11-6 GOES LOW. IC11-6 WILL GO LOW WHEN *HALT IS FALSE (IC11-5 HIGH) "AND" BA "OR" RESET ARE INPUTS TO BE SELECTED ON THE LEADING EDGE OF THE PHASE 1 CLOCK.

IN SUMMARY, ALL THE "1" INPUTS TO THE MULTIPLEXERS ARE SELECTED WHEN A "DMA" CYCLE IS BEING REQUESTED. THE "2" INPUTS WILL BECOME SELECTED AGAIN ONLY AFTER THE "DMA" CYCLE HAS BEEN GRANTED (BA) AND NO HALT REQUEST IS PRESENT.

THE BA SIGNAL (BUS AVAILABLE) IS SYNCHRONIZED WITH THE PHASE ONE CLOCK (IC36, 14) AND IS USED TO GATE BOTH THE *DMAO AND *REFR OUTPUTS (IC13-3, IC20-14).

THE REFRESH REQUEST SIGNAL (IC10-6) IS SYNCHRONIZED WITH THE PHASE ONE CLOCK (IC3-1, 4, 16) AND GATES THE *DMAO "OFF" (IC13-4) AND *REFR "ON" (IC20-13). THE *REFR SIGNAL IS "ON" FOR ONE COMPLETE PHASE ONE CLOCK CYCLE.

THE *DMAO SIGNAL IS GATED WITH *CLK2 (IC13-5) SO THE *DMAO SIGNAL IS ONLY TRUE DURING THE FIRST HALF OF PHASE ONE.

3.5 INTERRUPT LOGIC (SHEET 2)

THE INTERRUPT LOGIC CONSISTS OF IC'S 4, 17, 19, 24, AND PORTIONS OF IC'S 3, 12, AND 20.

IC4 IS AN 8-LINE TO 3-LINE PRIORITY ENCODER. THE OUTPUT OF IC4 (PINS 6, 7, AND 11) IS A BINARY REPRESENTATION (LOW TRUE) OF THE HIGHEST PRIORITY INPUT. OUTPUT GS (IC4-16) IS TRUE (LOW) WHEN ANY OF THE INPUT LINES ARE TRUE (LOW). THE INPUTS TO IC4 CONSIST OF 7 INTERRUPT REQUEST LINES, *IRQ0-6, AND *FPI. LINE *FPI IS THE HIGHEST PRIORITY AND IS RESERVED FOR THE FRONT PANEL INTERRUPT. *IRQ0- *IRQ6 ARE AVAILABLE FOR SYSTEM USAGE. THE FOLLOWING TABLE LISTS THE OUTPUT OF IC4 FOR EACH INPUT CONDITION:

INPUTS								OUTPUTS			
*FPI	*IRQ6	*IRQ5	*IRQ4	*IRQ3	*IRQ2	*IRQ1	*IRQ0	A2	A1	A0	GS
H	H	H	H	H	H	H	H	H	H	H	H
L	X	X	X	X	X	X	X	L	L	L	L
H	L	X	X	X	X	X	X	L	L	H	L
H	H	L	X	X	X	X	X	L	H	L	L
H	H	H	L	X	X	X	X	L	H	H	L
H	H	H	H	L	X	X	X	H	L	L	L
H	H	H	H	H	L	X	X	H	L	H	L
H	H	H	H	H	H	L	X	H	H	L	L
H	H	H	H	H	H	H	L	H	H	H	L

H = FALSE (+5 VOLTS)
L = TRUE (0 VOLTS)
X = H OR L (DON'T CARE)

THE GS OUTPUT (IC4-16) GENERATES *INT WHICH IS USED TO TRIGGER THE FRONT PANEL INT REQ DISPLAY. THE BINARY OUTPUTS OF IC4 (IC4 PINS 6, 7, AND 11) DRIVE IC17 AND IC24. IC17 IS USED TO STORE THE INTERRUPT MASK OR THE LEVEL OF INTERRUPT CURRENTLY BEING SERVICED. IC24 COMPARES THE LEVEL OF AN INTERRUPT REQUEST TO THE INTERRUPT MASK.

IC17 CONTAINS FOUR 2-INPUT MULTIPLEXERS WITH STORAGE REGISTERS FOR EACH OUTPUT LINE. IC17 IS CONTROLLED BY CP (IC17-13) AND S (IC17-12). WHEN S IS LOW, THE TRAILING EDGE OF THE POSITIVE CP PULSE STROBES THE "1" INPUTS (A1, B1, C1, D1) INTO THE OUTPUT STORAGE REGISTERS (IC17 PINS 14, 15, 16, AND 17). WHEN S IS HIGH, THE "2" INPUTS ARE STROBED INTO THE REGISTERS BY THE CP STROBE.

IC24 IS A 5-BIT COMPARATOR. WHEN THE BINARY VALUE OF THE "A" INPUTS EXCEEDS THE VALUE OF THE "B" INPUTS, THE OUTPUT (IC24-17) IS LOW. THE A AND B INPUTS ARE NUMBERED 0 THROUGH 4 WITH 4 HAVING THE HIGHEST VALUE.

WHEN THE INTERRUPT LOGIC IS IN AN INACTIVE CONDITION, IC17 CONTAINS AN INTERRUPT MASK VALUE PREVIOUSLY INPUT THROUGH DB0-DB2 (IC17 PINS 2, 1, AND 5) CORRESPONDING TO THE INTERRUPT LEVEL THAT MUST BE EXCEEDED FOR AN INTERRUPT TO BE RECOGNIZED. THIS VALUE IS INPUT TO IC17 THROUGH SOFTWARE BY WRITING INTO ONE OF THE INTERRUPT VECTOR MEMORY ADDRESS LOCATIONS (FFF8- FFFF). SINCE THE INTERRUPT VECTOR MEMORY LOCATIONS ARE IMPLEMENTED USING READ ONLY MEMORY (ROM), THE DATA WILL NOT ACTUALLY BE WRITTEN INTO THESE LOCATIONS. HOWEVER WHEN ADDRESSES WITHIN THE RANGE FFF8-FFFF ARE ADDRESSED, IC14-14 GOES HIGH

CAUSING THE "2" INPUTS (DB0, DB1, DB2, AND +5V) TO BE SELECTED ON IC17. THE SELECT SIGNAL IS INVERTED (IC19-3, 4) AND GATED WITH *WRITE (IC19-15) AND *CLK2 (IC19-1) TO GIVE A POSITIVE PULSE OF PHASE TWO DURATION TO THE CP INPUT (IC17-13) OF THE MASK REGISTER.

IN SUMMARY, INTERRUPT MASK DATA IS WRITTEN INTO IC17 THROUGH THE "2" INPUTS WHEN *WRITE IS TRUE (LOW) AND MEMORY WITHIN THE RANGE FFF8-FFFF IS BEING ADDRESSED.

IF AN INTERRUPT IS NOT BEING PROCESSED, THE A, B, AND C OUTPUTS OF IC17 (PINS 15, 16, AND 17) CONTAIN THE INTERRUPT MASK LEVEL. THE D OUTPUT (IC17-14) CONTAINS A LOGIC 1 (+5 VOLTS). IF AN INTERRUPT IS NOT BEING REQUESTED THE A INPUTS TO IC24 (PINS 11, 12, 13, 14, AND 15) ARE ALL LOGIC 1 (IC4 OPERATES ON LOW TRUE LOGIC, IC24 ON HIGH TRUE LOGIC). THEREFORE IF AN INTERRUPT IS NOT BEING REQUESTED, THE A INPUTS TO IC24 HAVE A VALUE GREATER THAN THE B INPUTS (SINCE B3, IC24-6 IS TIED TO GROUND) AND SINCE A>B, IC24-17 IS HIGH.

WHEN AN INTERRUPT REQUEST IS RECEIVED, *INT (IC4-16) GOES LOW AND THE BINARY VALUE OF THE INTERRUPT IS OUTPUT TO THE "A" INPUTS OF IC24 (PINS 13, 14 AND 15). SINCE IC4 OPERATES USING LOW TRUE LOGIC AND IC24 USES HIGH TRUE LOGIC, THE INTERRUPT LEVEL PRESENTED TO THE A INPUTS OF IC24 CAN BE CONSIDERED TO BE THE ONE'S COMPLEMENT OF THE ACTUAL VALUE. THEREFORE WHEN COMPARING THE A AND B INPUTS, IC24 WILL LOGICALLY BE COMPARING THE COMPLEMENT OF THE REQUEST LEVEL AND THE MASK VALUE. THE FOLLOWING TABLE LISTS THE MASKED AND UNMASKED INTERRUPT LEVELS CORRESPONDING TO EACH MASK VALUE.

INTERRUPT MASK VALUE	INTERRUPT LEVELS MASKED	INTERRUPT LEVELS ACTIVE
0	0-6	7
1	0-5	6-7
2	0-4	5-7
3	0-3	4-7
4	0-2	3-7
5	0-1	2-7
6	0	1-7
7	NONE	0-7

IF THE INTERRUPT REQUEST LEVEL IS NOT MASKED, THE OUTPUT OF IC24 (PIN 17) GOES LOW RESETTING IC20. IC20 (PINS 5, 6, AND 7) IS A SET/RESET FLIP-FLOP. THE OUTPUT OF IC20 (PIN 7) GOES LOW.

IC3 IS A PORTION OF THE 2-INPUT MULTIPLEXER USED IN THE DMA CONTROL CIRCUITS. IF A DMA OPERATION IS IN PROCESS, THE A2 INPUT IS SELECTED, OTHERWISE THE A1 INPUT IS SELECTED. IF A DMA OPERATION IS NOT IN PROCESS IC19-7 (INVERTED OUTPUT OF IC20) DRIVES IC3-17 HIGH AFTER THE NEXT PHASE ONE CLOCK EDGE. IC12-16 GOES LOW TRIGGERING A NON-MASKABLE INTERRUPT (NMI) WITHIN THE MICROPROCESSOR. AN INTERRUPT IS IN PROGRESS (*NMI TRUE) AND A DMA CYCLE IS REQUESTED (A2 INPUTS SELECTED). *NMI WILL REMAIN TRUE UNTIL IC20 IS SET (IC20-6 LOW). *INT DISABLES THE HALT SIGNAL TO THE MPU UNIT (IC23-16 SHEET 1) UNTIL IC20 IS SET. IF A DMA OPERATION IS IN PROGRESS WHEN THE INTERRUPT REQUEST IS RECEIVED, IC19-11 REMAINS LOW BECAUSE IC12-17 IS STILL LOW KEEPING IC19-13 HIGH. WHEN THE DMA OPERATION IS COMPLETED, THE A1 INPUT IS SELECTED AND IC3-17 GOES HIGH TRIGGERING A NMI REQUEST.

IN SUMMARY THE INTERRUPT REQUESTS AND DMA REQUESTS ARE HANDLED ON A FIRST COME, FIRST SERVED BASIS. A DMA REQUEST WILL LOCK OUT THE INTERRUPT CIRCUITRY UNTIL DONE. IF AN INTERRUPT IS REQUESTED DURING A DMA CYCLE IT WILL BE PROCESSED AFTER THE DMA REQUEST IS DONE AND ONE ADDITIONAL INSTRUCTION IS EXECUTED. IF A DMA CYCLE IS REQUESTED AFTER AN INTERRUPT REQUEST, THE CURRENT INSTRUCTION WILL BE COMPLETED. THEN ALL OF THE STATUS WILL BE PUSHED ONTO THE STACK AND THE PROGRAM COUNTER WILL BE SET TO THE VECTOR ADDRESS BEFORE A DMA CYCLE WILL BE GRANTED.

WHEN IC3-17 GOES HIGH, IC19-4 GOES LOW ENABLING THE CLOCK CONTROL GATE (IC19 PINS 1, 14, 15, 16, AND 17). WHEN THE MICROPROCESSOR RECOGNIZES AN INTERRUPT, IT STORES THE CONTENTS OF ITS PROGRAMMABLE REGISTERS IN MEMORY LOCATIONS SPECIFIED BY THE STACK POINTER. THIS STACKING OPERATION INVOLVES 7 MEMORY WRITE COMMANDS. EACH TIME A WRITE COMMAND IS EXECUTED, THE CLOCK CONTROL GATE IS ENABLED, STROBING THE INTERRUPT REQUEST LEVEL INTO THE IC17 OUTPUT REGISTERS (IC17-12 IS LOW BECAUSE ADDRESSES ARE NOT SELECTED IN THE RANGE FFF8-FFFF). THEREFORE IF A LOW PRIORITY LEVEL INTERRUPT TRIGGERS AN INTERRUPT REQUEST AND A HIGHER PRIORITY INTERRUPT REQUEST BECOMES ACTIVE BEFORE THE STACKING PROCESS IS COMPLETED, THE HIGHER PRIORITY INTERRUPT WILL BE PROCESSED. AT THE COMPLETION OF THE STACKING OPERATION THE COMPLEMENT OF THE HIGHEST PRIORITY INTERRUPT REQUEST RECEIVED WILL BE CONTAINED WITHIN THE IC17 OUTPUT REGISTERS.

THE FIRST WRITE CYCLE AFTER AN INTERRUPT IS REQUESTED WILL CAUSE A ZERO TO BE STROBED INTO IC17-14. THIS OUTPUT WILL THEN DISABLE THE OUTPUT OF THE COMPARATOR (IC24-17) BECAUSE WITH B4 = L AND A4 = H, B WILL ALWAYS BE LESS THAN A. IC24-17 WILL GO HIGH REMOVING THE RESET FROM IC20-5.

AFTER THE PROGRAMMABLE REGISTERS ARE STACKED, THE MICROPROCESSOR ACCESSES AN INTERRUPT VECTOR LOCATION TO FIND THE ADDRESS OF THE INTERRUPT SERVICE ROUTINE. THE MICROPROCESSOR ALWAYS VECTORS TO MEMORY LOCATIONS FFFC AND FFFD WHEN PROCESSING A NON-MASKABLE INTERRUPT. IC13-16 GOES LOW WHEN THESE ADDRESSES APPEAR ON THE MICROPROCESSOR ADDRESS OUTPUT LINES (IC1 PINS 9-25).

IC5 IS A 2-INPUT, 4-BIT MULTIPLEXER. IC5 IS USED TO SUBSTITUTE A VECTOR ADDRESS CORRESPONDING TO THE LEVEL OF INTERRUPT BEING SERVICED FOR THE NMI VECTOR OUTPUT BY THE MICROPROCESSOR. WHEN IC5-11 IS HIGH, THE MICROPROCESSOR ADDRESS LINES A1-A4 ARE OUTPUT TO ADDRESS DRIVERS (IC6). WHEN IC5-11 GOES LOW, IC5 SUBSTITUTES THE OUTPUTS OF IC17 (PINS 14-17) FOR MICROPROCESSOR ADDRESS LINES A1-4. THE FOLLOWING TABLE LISTS THE VECTOR ADDRESS SUBSTITUTED FOR THE NMI VECTOR FOR EACH INTERRUPT LEVEL.

INTERRUPT LEVEL	VECTOR ADDRESS
0	FFEE-FFEF
1	FFEC-FFED
2	FFEA-FFEB
3	FFE8-FFE9
4	FFE6-FFE7
5	FFE4-FFE5
6	FFE2-FFE3
*FPI	FFE0-FFE1

ALL MICROPROCESSOR INTERRUPT VECTOR ADDRESSES ARE WITHIN THE RANGE FFF8-FFFF. WHEN THE MICROPROCESSOR READS AN INTERRUPT VECTOR, LOCATION IC13-12 GOES LOW GENERATING *VCTO. THIS SIGNAL IS USED BY A MEMORY MODULE TO ACTIVATE THE MEMORY CONTAINING THE INTERRUPT SERVICE ROUTINE JUMP ADDRESSES. *VCTO ALSO DRIVES IC20-6 SETTING THE FLIP-FLOP OUTPUT (IC20-7) HIGH CAUSING IC3-17 TO GO LOW REMOVING THE NMI REQUEST (IC1-6) AND REMOVING THE ENABLE TERM FROM IC14-2.

SINCE STROBING THE INTERRUPT LEVEL INTO THE IC-17 OUTPUT REGISTERS ERASED THE MASK LEVEL, THE INTERRUPT SERVICE ROUTINE MUST RESTORE THE MASK (OR WRITE A NEW MASK) BY WRITING THE MASK LEVEL INTO AN ADDRESS WITHIN THE RANGE FFF8-FFFF.

3.6 ADDRESS LINE DRIVERS (SHEET 2)

THE ADDRESS LINE DRIVERS USE IC6, IC7, AND IC8 TO BUFFER THE MPU ADDRESS LINES AND DRIVE THE SYSTEM ADDRESS BUS (AB0-AB15) AND THE READ/WRITE LINE. THESE BUFFERS ARE THREE STATE DEVICES AND ARE GATED INTO THE THIRD HIGH IMPEDANCE STATE DURING DMA CYCLES OR WHEN THE MPU EXECUTES A "WAI" INSTRUCTION.

3.7 RESET GENERATOR (SHEET 1)

THE RESET GENERATOR USES PORTIONS OF IC'S 10, 14, 20, AND 23 TO GENERATE A SYSTEM RESET COMMAND. IC10 (RIGHT-SIDE) IS A MONOSTABLE-MULTIVIBRATOR (ONE-SHOT) UTILIZED AS A WATCHDOG TIMER. A 100 MICROSECOND TIMING PULSE IS TRIGGERED BY A POSITIVE TRANSITION ON IC10-14 OR A NEGATIVE TRANSITION ON IC10-13.

WHEN SYSTEM POWER IS FIRST TURNED ON, IC14-3 IS HELD LOW BY C4 AND R6, HOLDING IC14-4 HIGH. THE HIGH SIGNAL AT IC14-4 HOLDS THE TIMER TRIGGER CIRCUIT TRUE, PREVENTING A LOW GOING TRANSITION AT IC10-13 (*REFR) FROM TRIGGERING THE ONE-SHOT. IC10-12 REMAINS LOW HOLDING IC20 (IC20 IS A SET/RESET FLIP-FLOP) IN A SET CONDITION. THE OUTPUT OF IC20 (IC20-15) IS HELD HIGH ALLOWING THE REFRESH TIMING SIGNALS (IC22-3) THROUGH IC23 (PINS 2 AND 3) GENERATING RESET PULSES.

WHEN CAPACITOR C4 HAS CHARGED TO THE UPPER THRESHOLD OF IC14-3 (IC14 IS A SCHMITT TRIGGER INVERTER), IC14-4 WILL GO LOW, ALLOWING *REFR SIGNALS TO TRIGGER THE WATCHDOG TIMER. IC10-12 WILL GO TO A HIGH CONDITION AND REMAIN AS LONG AS *REFR SIGNALS ARRIVE AT A RATE FASTER THAN 100 MICROSECONDS.

AFTER IC10-12 GOES HIGH, THE NEXT *VCTO SIGNAL GENERATED (BY THE MICROPROCESSOR POWER ON INTERRUPT ROUTINE) WILL RESET IC20 (RIGHT-SIDE), SETTING IC23-1 LOW INHIBITING THE GENERATION OF *RESET SIGNALS.

IF AT ANY POINT IN TIME *REFR IS NOT GENERATED AT LEAST ONCE EVERY 100 MICROSECONDS, IC10-12 WILL GO LOW, SETTING IC20-15 HIGH, ALLOWING THE GENERATION OF *RESET.

3.8 ADDRESS DECODE LOGIC (SHEET 3)

THE ADDRESS DECODE CIRCUITRY CONSISTS OF IC'S 15, 16, AND 18 AND OTHER GATES AND INVERTERS. IC18 IS A 13-INPUT NAND GATE. THE INPUTS TO THIS GATE INCLUDE THE HIGH ORDER ADDRESS LINES (AB8-AB15) AND THE FUNCTION VMA "OR" *ENA (IC11-16). WHEN ALL OF THE HIGH ORDER ADDRESS LINES AND IC11-15 ARE TRUE (HIGH), THE OUTPUT OF IC18 (IC18-11) IS TRUE (LOW). IC18-11 IS INVERTED (IC12-14) AND BECOMES "IO" ON THE SYSTEM BUS.

IC18-11 IS ALSO USED AS THE SELECT SIGNAL FOR THE ADDRESS DECODE MULTIPLEXERS (IC15 AND IC16). EACH OF THESE IC'S CONTAIN FOUR TWO-INPUT INVERTING MULTIPLEXERS. WHEN IC18-11 IS TRUE (LOW), THE LOW ORDER ADDRESS SIGNALS ARE GATED ONTO THE ADDRESS DECODE LINES. WHEN IC18-11 IS HIGH, THE HIGH ORDER ADDRESS SIGNALS ARE GATED ONTO THE ADDRESS DECODE LINES.

IC11-15 (VMA OR *ENA) IS ALSO USED TO GENERATE THE "MEM" SIGNAL ON THE SYSTEM BUS. IF IC18-11 IS FALSE ("NOT" IO) AND IC11-15 IS TRUE (VALID ADDRESS), IC20-4 IS TRUE (0V) DRIVING IC12-12 HIGH ("MEM").

IC23-12 IS USED TO GENERATE A "DUMMY REPLY" SIGNAL. IF IO (IC18-11) IS FALSE (+5V) AND MEM (IC20-9) IS FALSE (+5V), IC23-12 PULLS THE *RPLY LINE TRUE (0V) GENERATING A REPLY CONDITION.

SUMMARIZING, IF A VALID MEMORY ADDRESS EXISTS (INDICATED BY THE EXISTANCE OF VMA FOR CPU OR *ENA FOR DMA), AND ALL OF THE HIGH ORDER ADDRESS BITS ARE TRUE, (FF00 TO FFFF) "IO" IS GENERATED AND THE COMPLEMENT OF THE LOW ORDER ADDRESS SIGNALS ARE GATED ONTO THE ADDRESS DECODE LINES. THIS CONDITION IS REQUIRED TO CAUSE AN I/O OPERATION.

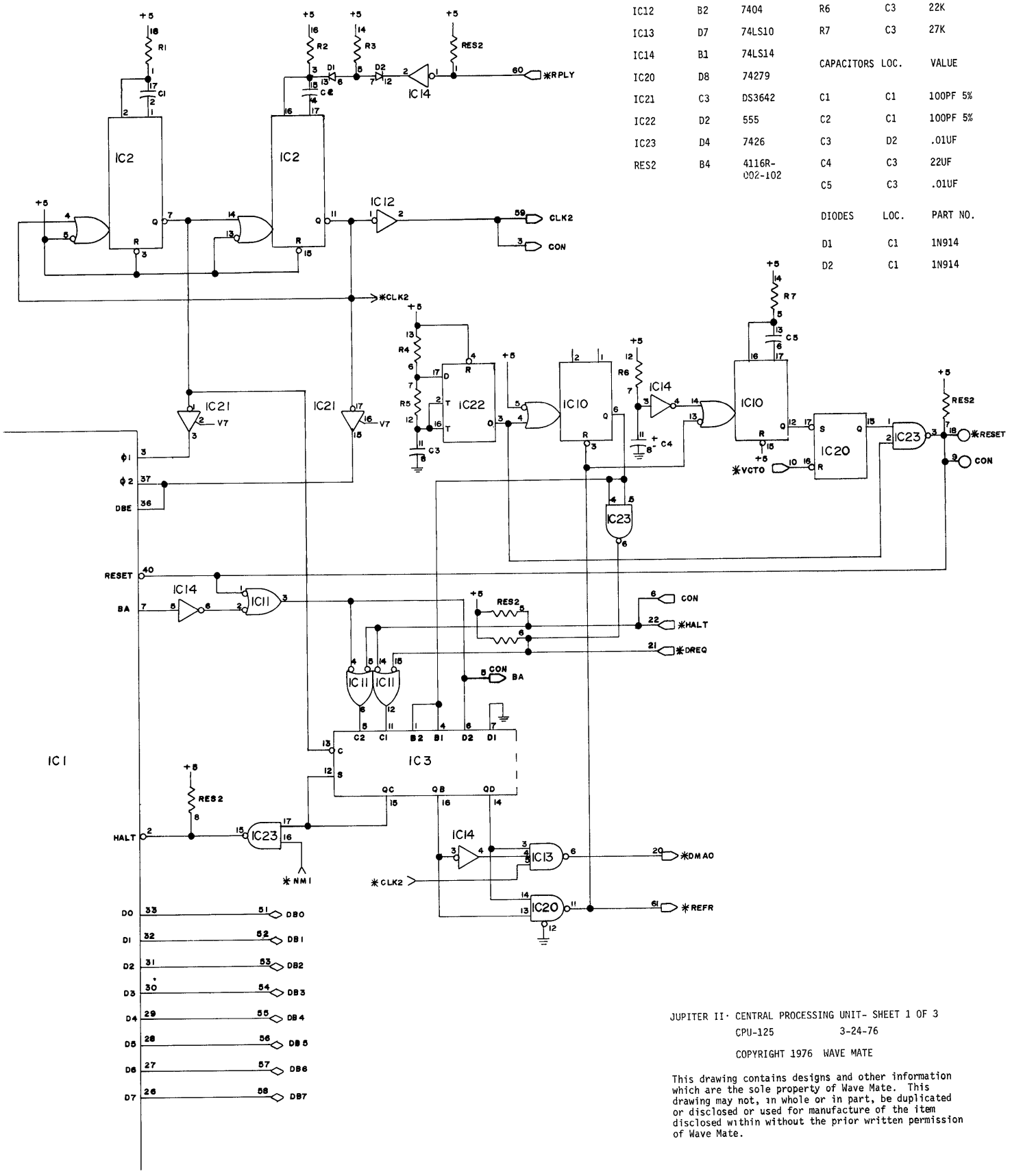
ON THE OTHER HAND IF A VALID MEMORY ADDRESS EXISTS AND ALL OF THE HIGH ORDER ADDRESS BITS ARE NOT TRUE, "MEM" IS GENERATED AND THE COMPLEMENT OF THE HIGH ORDER ADDRESS SIGNALS ARE GATED ONTO THE ADDRESS DECODE LINES. THIS CONDITION IS REQUIRED TO CAUSE A MEMORY TRANSFER OPERATION.

IC NO.	LOCATION	PART NO.
IC1	C4	MC6800
IC2	C2	9602
IC3	D6	74LS298
IC10	D3	9602
IC11	B3	74LS00
IC12	B2	7404
IC13	D7	74LS10
IC14	B1	74LS14
IC20	D8	74279
IC21	C3	DS3642
IC22	D2	555
IC23	D4	7426
RES2	B4	4116R-002-102

RESISTORS	LOC.	VALUE
R1	C1	11K 2%
R2	C1	51K
R3	C1	15K 2%
R4	D2	2.2K
R5	D2	1K
R6	C3	22K
R7	C3	27K

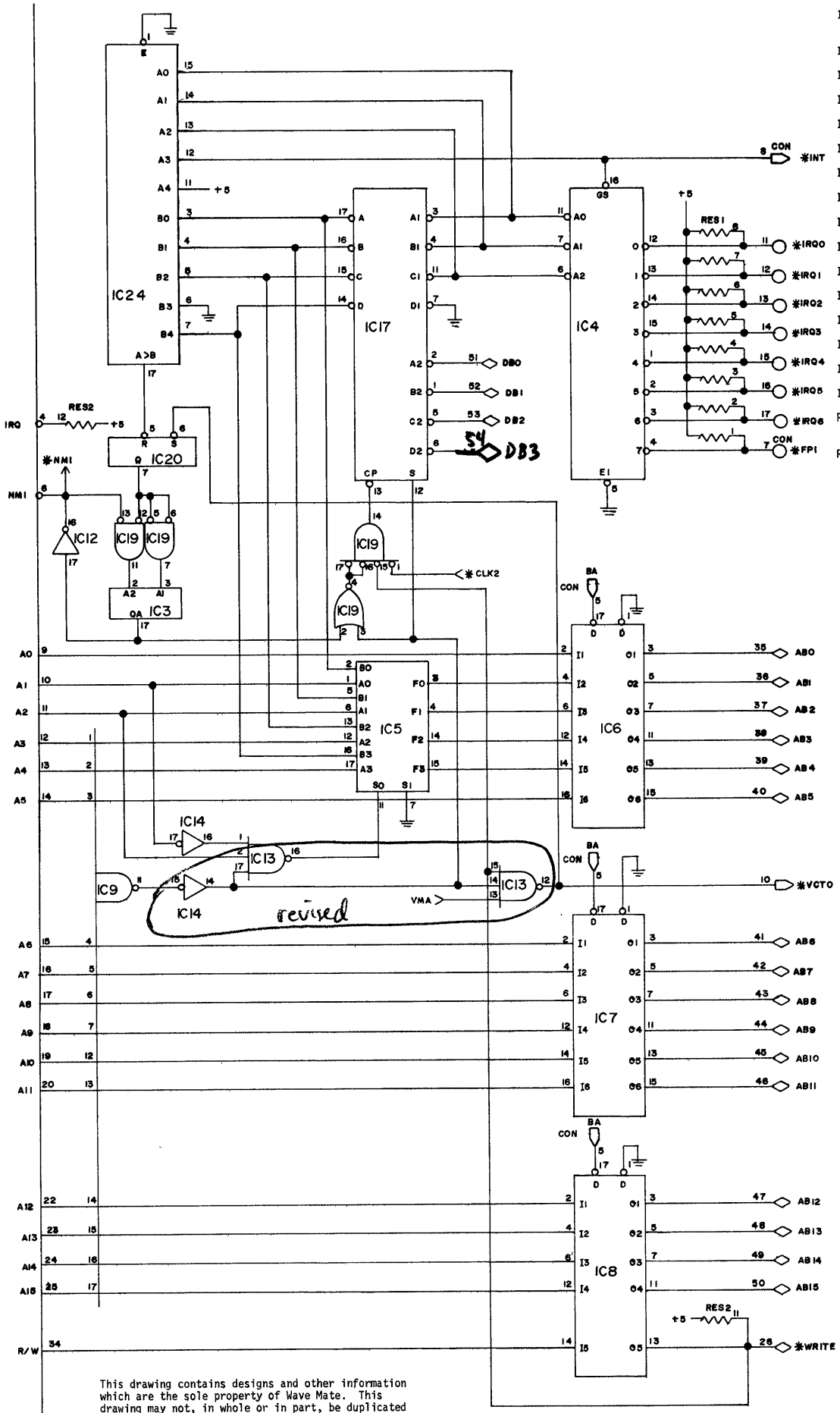
CAPACITORS	LOC.	VALUE
C1	C1	100PF 5%
C2	C1	100PF 5%
C3	D2	.01UF
C4	C3	22UF
C5	C3	.01UF

DIODES	LOC.	PART NO.
D1	C1	1N914
D2	C1	1N914



JUPITER II· CENTRAL PROCESSING UNIT- SHEET 1 OF 3

CPU-125 3-24-76



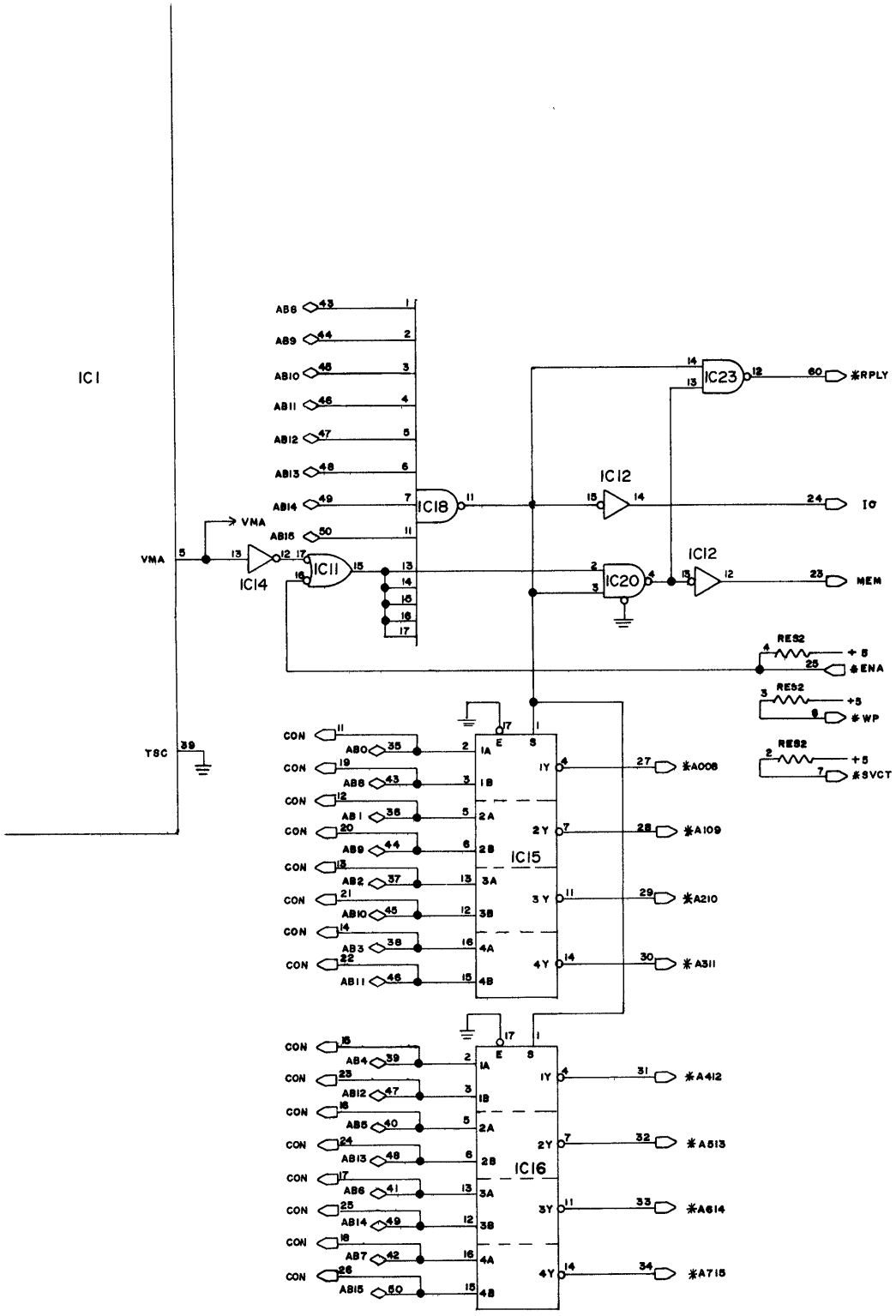
IC NO.	LOC.	PART NO.
IC1	C4	MC6800
IC3	D6	74LS298
IC4	A2	93L18
IC5	B7	82S33
IC6	A6	8T95
IC7	A7	8T95
IC8	A8	8T95
IC9	B8	74LS133
IC12	B2	7404
IC13	D7	74LS10
IC14	B1	74LS14
IC17	B5	74LS298
IC19	D5	9015
IC20	D8	74279
IC24	B6	93L24
RES1	A1	4116R-001-562
RES2	B4	4116R-002-102

IC 1

JUPITER II: CENTRAL PROCESSING UNIT- SHEET 2 OF 3

CPU-125 3-24-76

IC NO.	LOCATION	PART NO.
IC1	C4	MC6800
IC11	B3	74LS00
IC12	B2	7404
IC14	B1	74LS14
IC15	A3	74158
IC16	A4	74158
IC18	A5	74LS133
IC20	D8	74279
IC23	D4	7426
RES2	B4	4116R-002-102



JUPITER II: CENTRAL PROCESSING UNIT- SHEET 3 OF 3

CPU-125 3-24-76

Wave Mate
Computers & Systems
1015 W. 190th STREET • GARDENA, CALIFORNIA 90248

11-18-1976

Changes- CPU-125

DELETE	ADD	WIRE
B2-2 (2) BUS-59	CON-3 (1) D8-1	Blue
CON-3 (1) B2-2	B2-2 (1) BUS-59	Brown
	D8-1 (2) B2-2	White
C4-5 (2) D7-13		
B1-13 (1) C4-5	C4-5 (1) B1-13	Yellow
B4-4 (2) BUS-25	B1-12 (1) D5-6	Blue
B3-16 (1) B4-4	D5-6 (2) D8-2	Red
D4-14 (2) B2-15	D8-3 (1) C1-11	White
D4-14 (1) D8-3	B4-4 (1) BUS-25	White
	C1-11 (2) B4-4	Red
D5-15 (2) D7-15		
B4-11 (2) A8-13	B3-16 (1) D4-14	Green
B4-11 (1) D5-15	B3-16 (2) B2-15	Black
D4-13 (2) D8-4	B4-11 (1) D7-15	White
B2-13 (1) D4-13	A8-13 (2) B4-11	Yellow
B3-17 (1) B1-12	A8-15 (1) D5-15	Orange
	D5-15 (2) D2-14	Red
B8-11 (1) B1-15		
	D4-13 (1) B3-15	Blue
C1-6 (2) C1-7	B3-15 (2) B2-13	Black
C4-34 (1) A8-14	B8-11 (1) D5-5	White
D6-3 (1) D5-7	C1-7 (1) C1-8	Black
	C1-6 (2) C1-7	Black
D8-12 (2) D8-1		
	C4-34 (1) A8-16	Blue
D5-6 (2) D5-12	A8-16 (2) A8-14	Black
D5-12 (1) D8-7		
D5-5 (1) D5-6	D2-8 (1) D2-5	Black
B5-12 (2) B1-14	D6-3 (1) B1-14	White
D7-14 (2) D5-3		
B5-12 (1) D5-3	B1-15 (1) D5-12	Blue
	D5-12 (2) D8-7	Red
A5-17 (2) B3-15		
B3-15 (1) D8-2	D7-13 (1) D5-7	Red
	D5-3 (1) B5-12	Blue
D5-1 (2) C3-17	D7-14 (2) D7-13	Black
	D5-7 (2) D5-3	Black
C2-11 (2) C2-4		

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Computers & Systems
1015 W. 190th STREET • GARDENA, CALIFORNIA 90248

11-18-1976

Changes- CPU-125

DELETE	ADD	WIRE
B2-2 (2) BUS-59	CON-3 (1) D8-1	Blue
CON-3 (1) B2-2	B2-2 (1) BUS-59	Brown
	D8-1 (2) B2-2	White
C4-5 (2) D7-13		
B1-13 (1) C4-5	C4-5 (1) B1-13	Yellow
B4-4 (2) BUS-25	B1-12 (1) D5-6	Blue
B3-16 (1) B4-4	D5-6 (2) D8-2	Red
D4-14 (2) B2-15	D8-3 (1) C1-11	White
D4-14 (1) D8-3	B4-4 (1) BUS-25	White
	C1-11 (2) B4-4	Red
D5-15 (2) D7-15		
B4-11 (2) A8-13	B3-16 (1) D4-14	Green
B4-11 (1) D5-15	B3-16 (2) B2-15	Black
D4-13 (2) D8-4	B4-11 (1) D7-15	White
B2-13 (1) D4-13	A8-13 (2) B4-11	Yellow
B3-17 (1) B1-12	A8-15 (1) D5-15	Orange
	D5-15 (2) D2-14	Red
B8-11 (1) B1-15		
	D4-13 (1) B3-15	Blue
C1-6 (2) C1-7	B3-15 (2) B2-13	Black
C4-34 (1) A8-14	B8-11 (1) D5-5	White
D6-3 (1) D5-7	C1-7 (1) C1-8	Black
	C1-6 (2) C1-7	Black
D8-12 (2) D8-1		
	C4-34 (1) A8-16	Blue
D5-6 (2) D5-12	A8-16 (2) A8-14	Black
D5-12 (1) D8-7		
D5-5 (1) D5-6	D2-8 (1) D2-5	Black
B5-12 (2) B1-14	D6-3 (1) B1-14	White
D7-14 (2) D5-3		
B5-12 (1) D5-3	B1-15 (1) D5-12	Blue
	D5-12 (2) D8-7	Red
A5-17 (2) B3-15		
B3-15 (1) D8-2	D7-13 (1) D5-7	Red
	D5-3 (1) B5-12	Blue
D5-1 (2) C3-17	D7-14 (2) D7-13	Black
	D5-7 (2) D5-3	Black
C2-11 (2) C2-4		

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Changes- CPU-125 Cont.

DELETE	ADD	WIRE
D7-5 (1) D5-1	D8-4 (1) B3-17	White
	B3-17 (2) A5-17	Red
C3-17 (1) C2-11		
	C2-6 (1) D7-5	Blue
C2-4 (1) B2-1	D5-1 (1) C3-17	Yellow
	C2-11 (1) C2-4	Black
C2-14 (2) C3-1	C3-17 (2) C2-11	Black
C3-1 (1) D6-13	C2-4 (2) B2-1	Red
	C2-14 (2) C3-1	Black
	C2-12 (1) D6-13	Green

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Changes- CPU-125 Cont.

DELETE	ADD	WIRE
D7-5 (1) D5-1	D8-4 (1) B3-17	White
	B3-17 (2) A5-17	Red
C3-17 (1) C2-11	C2-6 (1) D7-5	Blue
C2-4 (1) B2-1	D5-1 (1) C3-17	Yellow
	C2-11 (1) C2-4	Black
C2-14 (2) C3-1	C3-17 (2) C2-11	Black
C3-1 (1) D6-13	C2-4 (2) B2-1	Red
	C2-14 (2) C3-1	Black
	C2-12 (1) D6-13	Green

ENGINEERING CHANGE SHEET

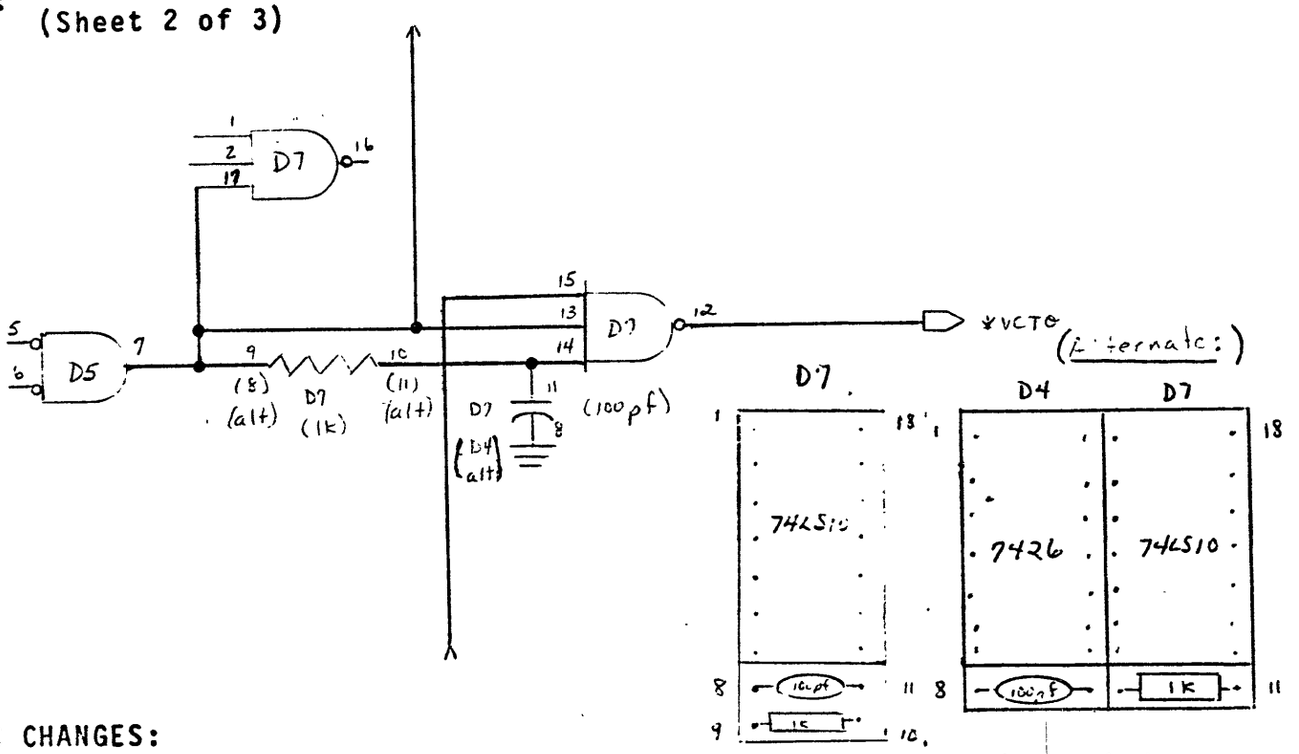
DATE: 4/25/78 (6/11/78) BY: D. Brown (J. Young)

MODULE: CPU-125 (6800) REVISION NO.: 5

ISSUE TO SERIAL NOS.: All

REASON FOR CHANGE: Eliminate timing differential between VMA and address actually valid, causing 50ns spikes, which reset interrupts prematurely.

SCHEMATIC: (Sheet 2 of 3)



WIRING/IC CHANGES:

REMOVE:	D7-14 (2) D7-13	Black	Alternate for 16-pin sockets-	
	D7-17 (1) D7-14	Black	→ SAME	
ADD:	D7-17 (1) D7-9	Black	D7-17 (1) D7-8	Black
	D7-17 (2) D7-13	Black	D7-17 (2) D7-13	Black
	D7-14 (1) D7-11	Black	D7-14 (1) D7-11	Black
	D7-11 (2) D7-10	Black	D4-11 (2) D7-11	Red
	D7-8 (1) D7-7	Black	D4-8 (1) D4-7	Black

ADD: 1K Resistor (Brown-Black-Red) = D7-9 to D7-10 (Alt. D7-8 to D7-11)

100 pf cap ("101") = D7-8 to D7-11 (Alt. D4-8 to D4-11)

ENGINEERING CHANGE SHEET

DATE: 8/18/78 (12/11/79) BY: D. Brown (J. Young)

MODULE: CPU-125 (6800) REVISION NO.: 6

ISSUE TO SERIAL NOS.: all using SDOS or MTS software

REASON FOR CHANGE: more control for Interrupt system

SCHEMATIC:

Rev. 7 - change R4 (loc. D2, pins 6-13)
from 2.2k (RRR) to 1.8K (Br, Gray, Red)

79.12.11
J. Young

WIRING/IC CHANGES:

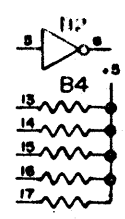
Remove: B5-6 (2) B5-18 Black

Add: B5-6 (2) C4-30 Yellow

~~BUS-8 (3) A8-17 White~~

BUS-8 (2) A8-17 Orange

UNUSED ELEMENTS



6800 CPU MODULE
CPU-125 3-24-76

SHEET 1 OF 3
DRAWN BY: A. [illegible]
REVISION 5

C4

Non-vectored interrupt. mods 5/23/81

1.2MHz
C1-5 to C1-12 7.5K
C1-1 to C1-16 4.7K
use 68B09

1 MHz CPU
C1-5 to C1-12: 7.5K
C1-1 to C1-16: 11K
(original design)

1.4MHz CPU
C1-5 to C1-12 4.3K
C1-1 to C1-16 4.7K
Use 68B00!
disk+ mods 11/15/83

NVI Non Vectored Interrupt Mods

6800 CPU MODULE
CPU-125 3-24-76
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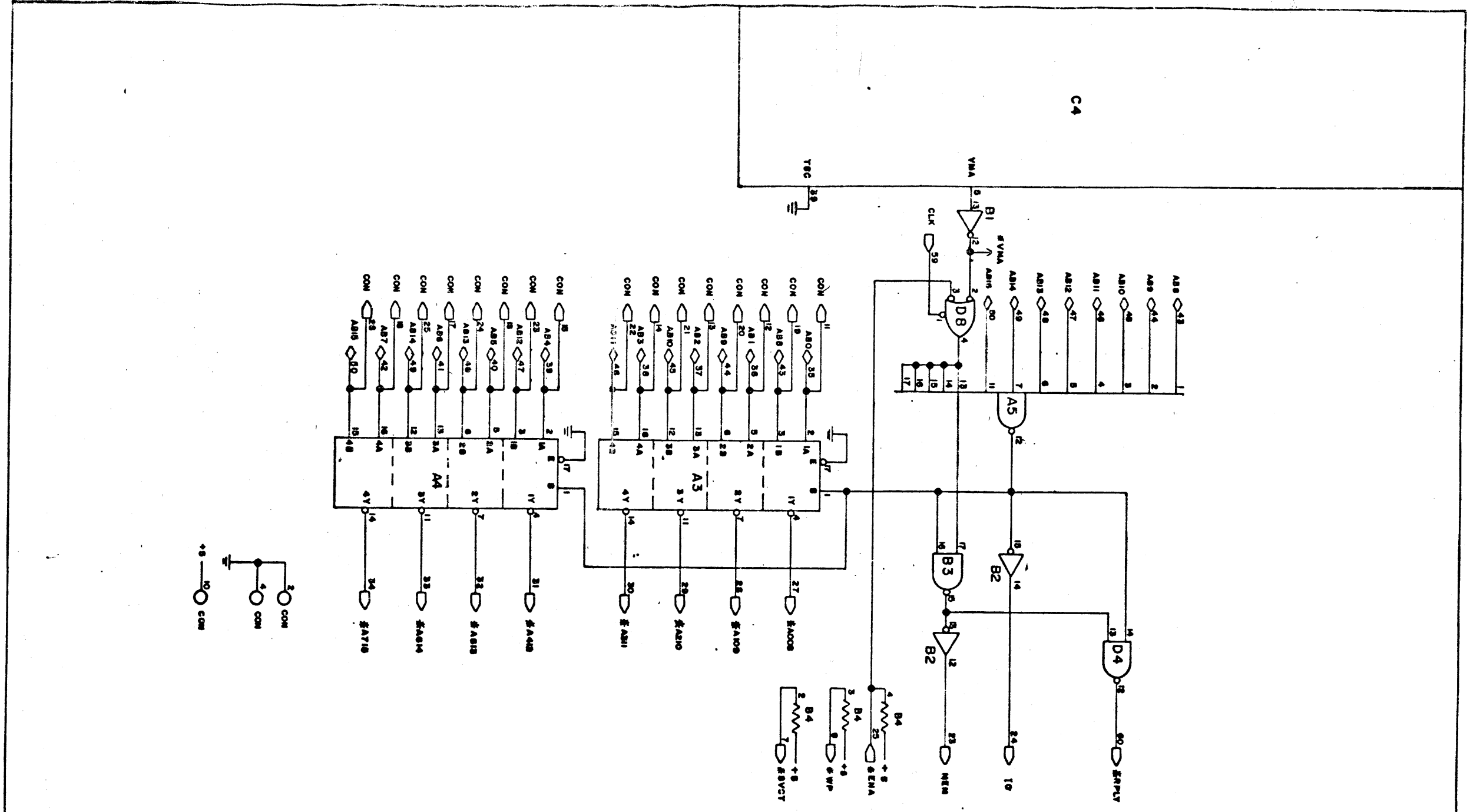
SHEET 2 OF 3
DRAWN BY: A. Yuen
REVISION: 5

C4



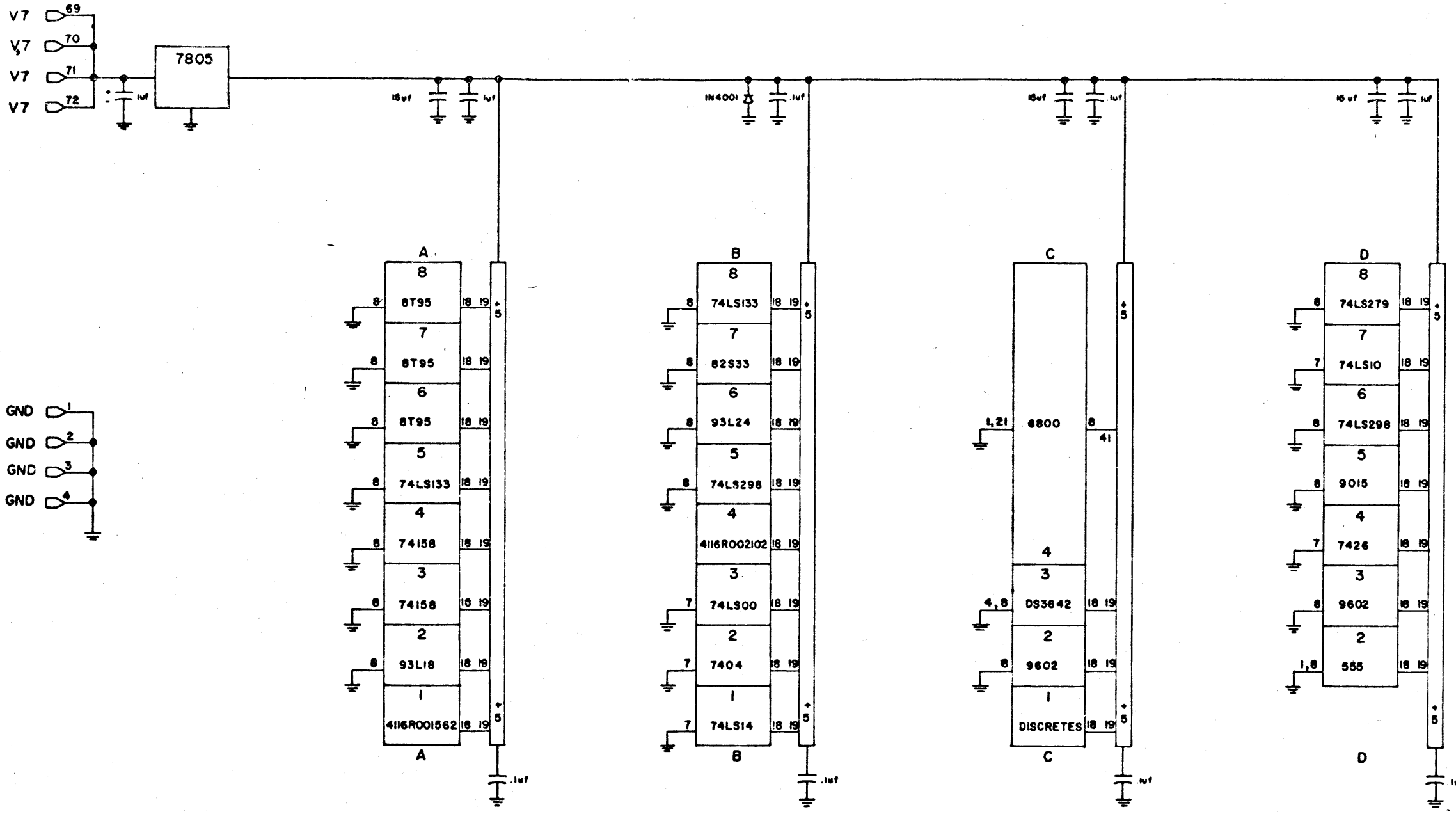
6800 CPU MODULE

CPU-125 3-24-76

SHEET 3 OF 3

DRAWN BY: A. Martin

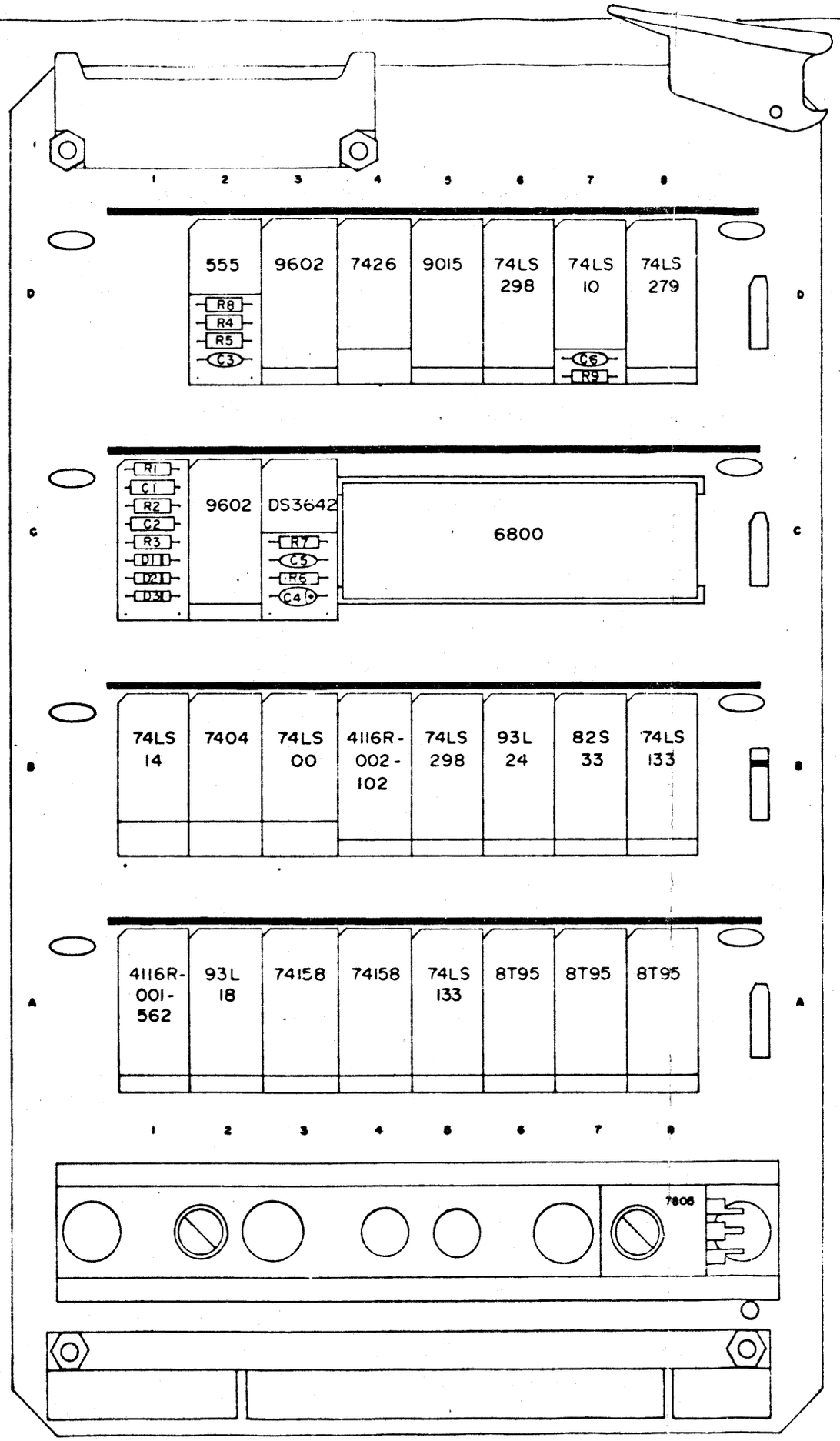
REVISION: 5



POWER DISTRIBUTION
6800 CPU MODULE
CPU-125

DRAWN BY a Hanke

REVISION 5



NAME	PART NUMBER
A1	4116R-001-562 (5.6KΩ)
A2	93L18
A3	74158
A4	74158
A5	74LS133
A6	8T95
A7	8T95
A8	8T95
B1	74LS74
B2	7404
B3	74LS00
B4	4116R-002-102 (1KΩ)
B5	74LS298
B6	93L24
B7	82S33
B8	74LS 33
C1	DISCRETES
C2	9602
C3	DS3642
C4	6800
D2	555
D3	9602
D4	7426
D5	9015
D6	74LS298
D7	74LS10
D8	74LS279

LOCATION & NAME	PART NUMBER
C1 - R1	11K RESISTOR 2%
- C1	100pf CAPACITOR
- R2	51K RESISTOR 2%
- C2	200pf CAPACITOR
- R3	7.5K RESISTOR 2%
- D1	IN914 DIODE
- D2	IN914 "
- D3	IN914 "
C3 - R7	27K RESISTOR 5%
- C5	.01uf CAPACITOR
- R6	22K RESISTOR 5%
- C4	22uf CAPACITOR
D2 - R8	1K RESISTOR 5%
- R4	22K " "
- R5	1K " "
- C8	4.7Kpf CAPACITOR
D7 - C6	100 pf "
- R9	1K RESISTOR 5%

6800 CPU MODULE

CPU-125 3-24-76

DRAWN BY: a Martin

REVISION 5