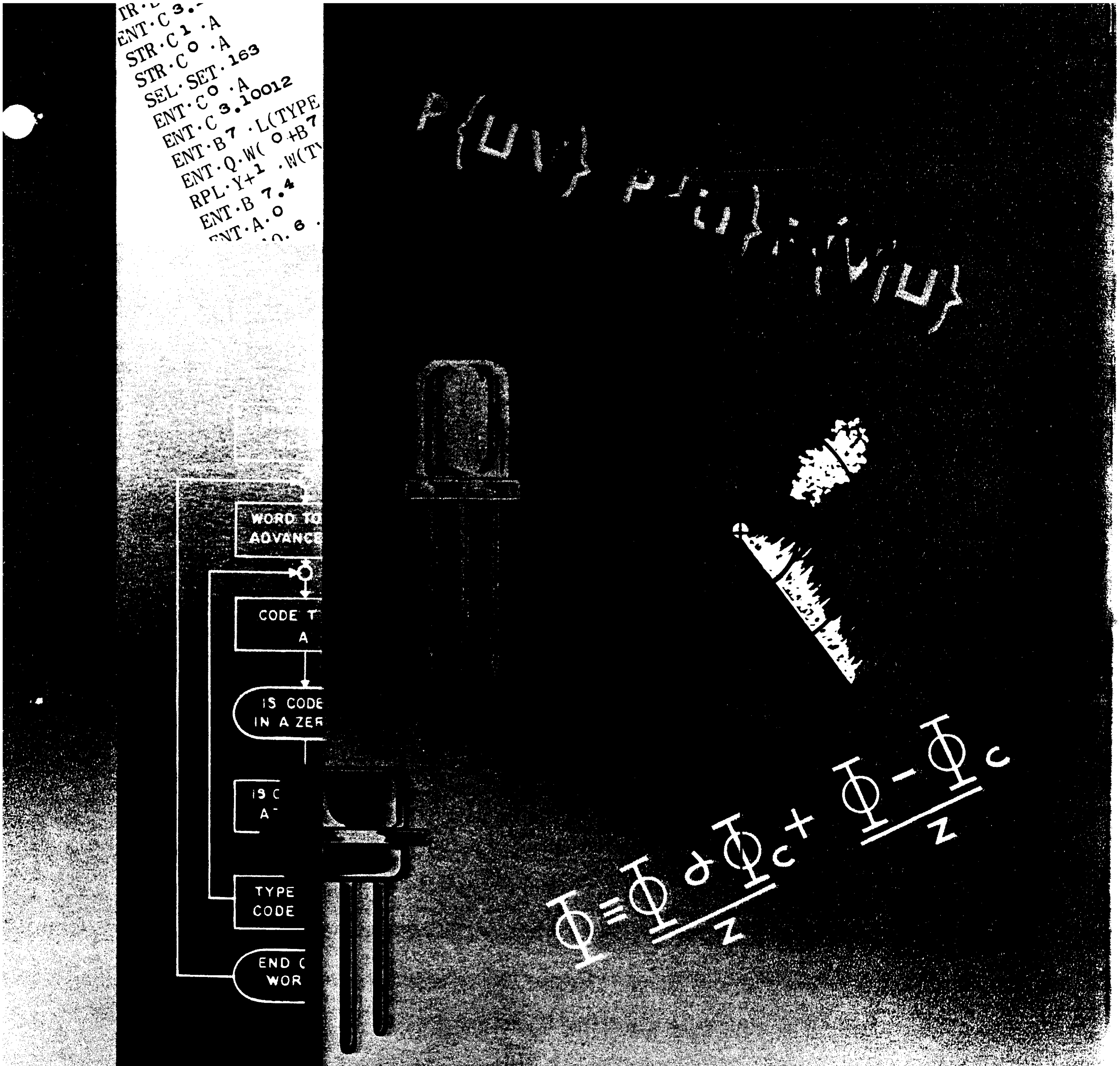

NAVAL TACTICAL DATA SYSTEM (NTDS)

technical note no. 221

INPUT/OUTPUT SPECIFICATION - AN/USQ-20 COMPUTER SET

Remington Rand Univac
DIVISION OF SPERRY RAND CORPORATION
UNIVAC PARK, ST. PAUL 16, MINNESOTA

NAVAL TACTICAL DATA SYSTEM
TECHNICAL NOTE
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INPUT/OUTPUT SPECIFICATION
for the
AN/USQ-20 COMPUTER SET
and
ASSOCIATED EQUIPMENT

PX 1343-11

Remington Rand Univac®
DIVISION OF SPERRY RAND CORPORATION
UNIVAC PARK, ST. PAUL 16, MINNESOTA

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INPUT/OUTPUT SPECIFICATION FOR THE AN/USQ-20 COMPUTER SET AND ASSOCIATED EQUIPMENT

1. INTRODUCTION

1.1 GENERAL

Communication with the NTDS Unit Computer is carried on in a 30-bit parallel mode. The Unit Computer is provided with ~~one~~ input register, which is divided into ~~eight~~ *normal* input channels and ~~three~~ *special* input channels, and two output registers, which are divided into respectively ~~eight~~ *normal* and ~~three~~ *special* output channels. External Function Codes (formerly known as C^3 codes) are carried over the same 30 lines as are used for data, but the control signals used with External Function Codes are carried on different lines to indicate the nature of the signals on the 30 lines.

Note that all references, in this section of the Technical Note, to input or output are made from the standpoint of the computer; that is, *input* is input *to* the computer and *output* is output *from* the computer.

1.2 CONTROL COMMUNICATION

The NTDS Unit Computer is designed to use a d-c level input/output system. Signals are d-c levels which may be changed upon interchange of control information. Signals may exist for microseconds or days, depending on the nature of the particular task. Signals cannot be pulses of arbitrary duration, picked to satisfy the requirements of a particular piece of NTDS equipment. Although a given external equipment may be used successfully by doing this, the result is to restrict the inherent flexibility of the NTDS.

It should be noted that the input/output circuits for the control lines are no different from those of the data lines. Hence, delay times, rise and fall times, and storage times are similar.

1.3 DATA AND CONTROL SIGNALS

Each input and each output channel has its own cable associated with it (~~22~~ 28 cables in all). Each cable has 30 data lines plus three of a possible four control lines, as listed in Table 1.

TABLE 1. Control Signals in Input and Output Cables

NORMAL INPUT CABLE	*SPECIAL* INPUT CABLE	*NORMAL* OUTPUT CABLE	*SPECIAL* OUTPUT CABLE
Input Data Request	Input Data Request	Output Data Request	Ready
Input Acknowledge	Input Acknowledge	Output Acknowledge	Resume
Interrupt	Interrupt (not used in inter-computer communication)	External Function	(Not Used)
(Not Used)	Input Buffer Active (used only in inter-computer communication)	(Not Used)	Input Buffer Active

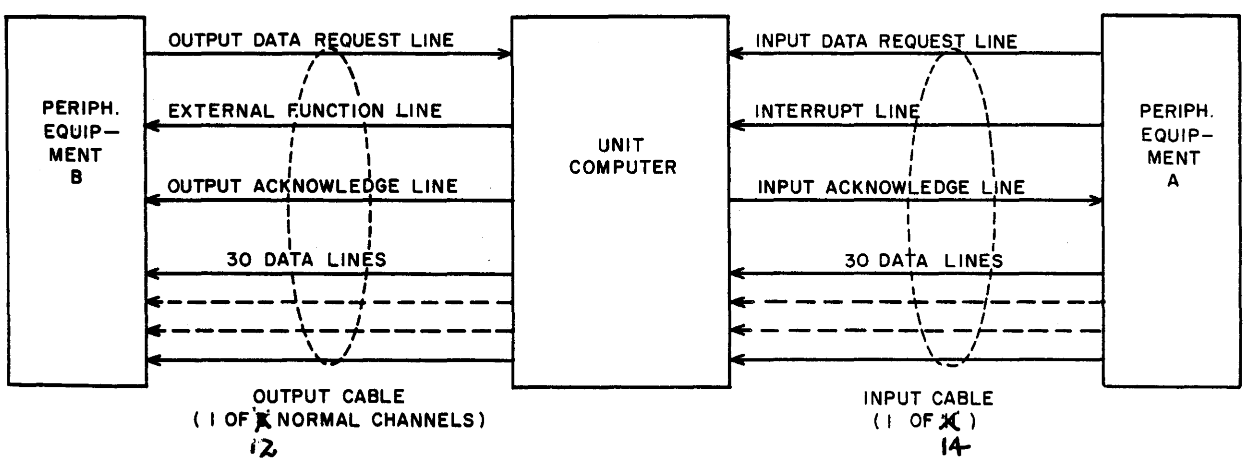

Figure 1. Cable Connections

Figure 1 shows the Unit Computer receiving input from equipment A and sending output to equipment B. Of course in most cases, both input and output cables will be used on the same peripheral equipment. Only normal output channels are used for output to peripheral equipment. Any input channel may be used for input from peripheral equipment. Note the direction of information flow. The Data Request signals are always sent from the peripheral equipment to the computer. The Acknowledge signals are always sent from the computer to the peripheral equipment. The third set of control signals, called Interrupt in the input cable and External Function in the output cables, are always sent in the same direction as the data flow.

1.4 SEQUENCE OF EVENTS

The Sequence of events for each of the four cases of communication between the Unit Computer and the peripheral equipment follows:

1.4.1 Normal input sequence for data transfer from equipment A to computer (Buffer Mode):

1. Peripheral equipment places data word on 30 data lines.
2. Peripheral equipment sets the Input Data Request line to indicate that it has data ready for transmission.
3. Computer detects the Input Data Request.
4. Computer samples the 30 data lines at its own convenience.
5. Computer sets the Input Acknowledge line, indicating that it has sampled the data.
6. Peripheral equipment senses the Input Acknowledge line.
7. Peripheral equipment drops the data lines and the Input Data Request line.

This sequence is repeated for every data word.

1.4.2 Sequence for peripheral equipment A transmitting an Interrupt code to computer:

1. Peripheral equipment places the Interrupt code on the 30 data lines.
2. Peripheral equipment sets the Interrupt line.
3. Computer detects the Interrupt.
4. Computer samples the 30 data lines.

5. Computer sets the Input Acknowledge line, indicating that it has sampled the data.

6. Peripheral equipment senses the Input Acknowledge line.

7. Peripheral equipment drops the Interrupt code from the data lines and the Interrupt line.

1.4.3 Normal output sequence for data transfer from Unit Computer to equipment B (Buffer Mode):

1. Peripheral equipment sets the Output Data Request line indicating that it is in a condition to accept data.

2. Computer detects Output Data Request at its convenience.

3. Computer places information on the 30 data lines.

4. Computer sets the Output Acknowledge line, indicating that data are ready for sampling.

5. Peripheral equipment detects the Output Acknowledge.

6. Peripheral equipment samples the 30 data lines.

7. Computer drops Output Acknowledge and data lines.

8. Peripheral equipment drops Output Data Request.

This sequence is repeated for every data word.

1.4.4 Sequence for Unit Computer transmitting an External Function Code to equipment B:

1. Computer places the external function code on the 30 data lines.

2. Computer sets the External Function line.

3. Peripheral equipment detects the External Function line.

4. Peripheral equipment samples the 30 data lines.

5. Computer drops External Function code on the 30 data lines and the External Function line.

1.5 USE OF SPECIAL OUTPUT CHANNELS

Communications between two computers take place using the three special output channels reserved for this purpose. They are connected into a special input channel on the receiving computer. Note that while either a normal or a special input channel may be used for input from peripheral equipment, a special input channel is required for inter-computer communication to connect to a special output channel.

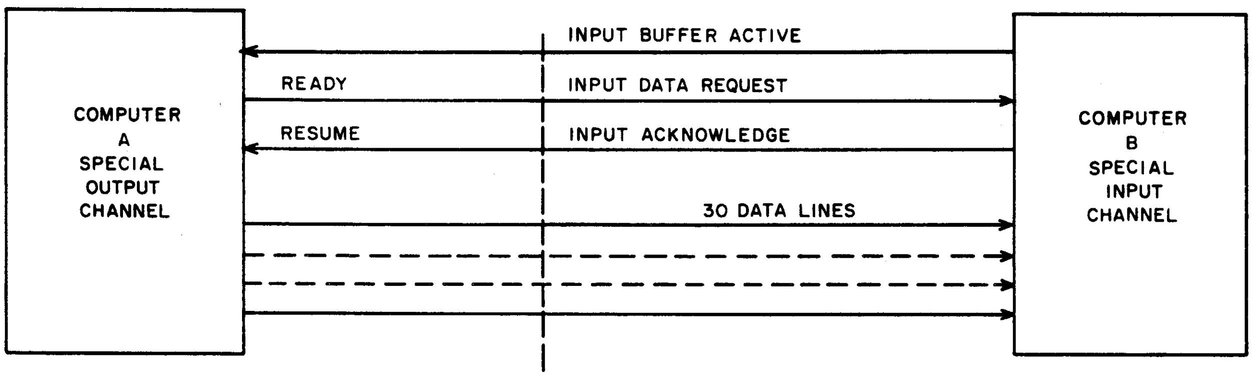

Figure 2. Connections from Computer A to Computer B

Figure 2 illustrates the connections for Computer A to transmit data to Computer B. Another cable using a special output channel of Computer B and a special input channel of Computer A would be necessary if Computer B were going to transmit data to Computer A.

Sequence of events for normal transfer of data from Computer A to Computer B (Buffer Mode):

1. Computer B sets Input Buffer Active signal.
2. Computer A detects Input Buffer Active signal.
3. Computer A places data on 30 data lines.
4. Computer A sets *Ready* which becomes Input Data Request in Computer B.
5. Computer B detects Input Data Request.
6. Computer B samples 30 data lines.
7. Computer B sets Input Acknowledge line which is returned to Computer A as *Resume*.

8. Computer A senses *Resume* line.

9. Computer A drops data lines and *Ready* line.

Steps 3 through 9 of this sequence are repeated for every data word. Input Buffer Active remains energized during entire transfer of block of words.

1.6 TIMING

When transmitting data from the Unit Computer to an external equipment, the data lines must be stable before being sampled. For this reason, a fixed time delay of 4.5 microseconds exists between the instant the Unit Computer loads an output register and the instant the Acknowledge signal is energized.

Figure 3 illustrates how tolerances might build up adversely to cause the Acknowledge signal to be recognized less than a microsecond after the data have reached the recognition state.

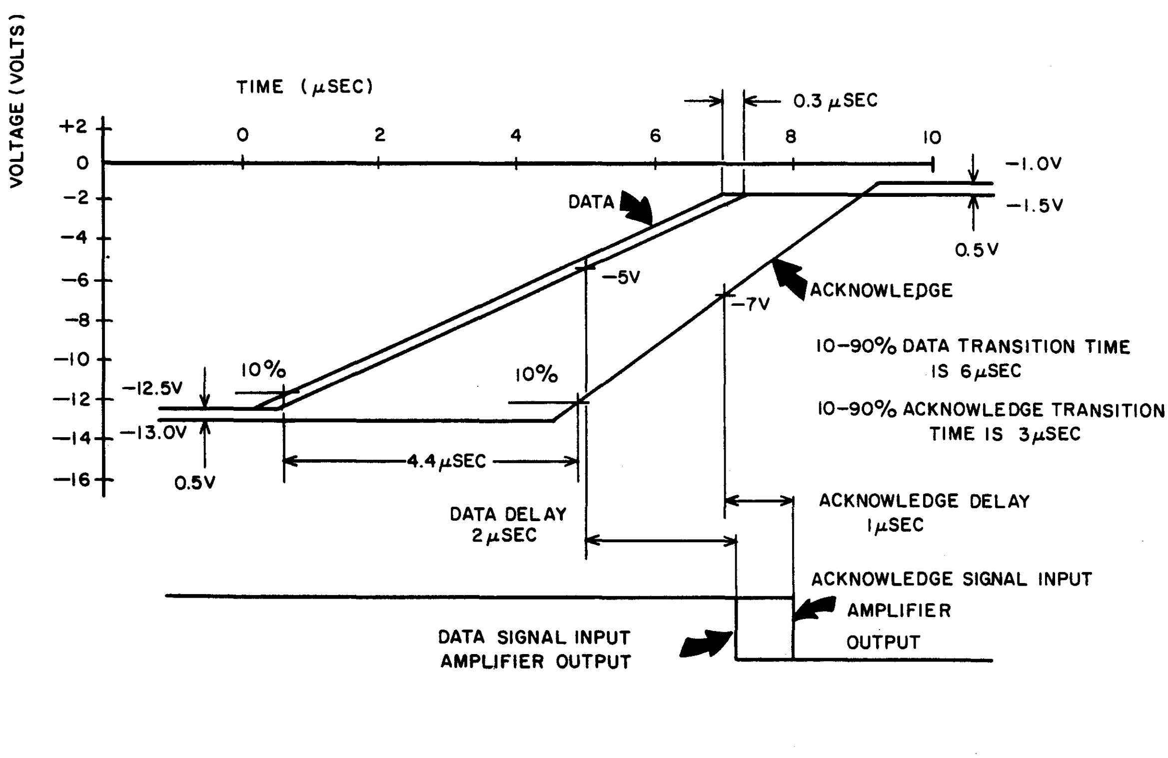

Figure 3. Effect of Tolerances on Timing

An analogous situation exists for computer input. For this reason, in each equipment sending data to the Unit Computer, it is necessary to incorporate a delay of at least 4.5 microseconds between the time the data are placed on the lines and the time the Input Data Request signal is initiated.

1.6.1 Input Timing Considerations

The Input Data Request (or Interrupt) must be maintained on the lines until an Input Acknowledge is received. Note that there is no maximum limit on the time the Input Data Request may stay up until being acknowledged. The data lines must remain stable as long as the Input Data Request is up.

The Input Acknowledge signal will be set for a fixed time only, nominally 15 microseconds. The peripheral equipment must be capable of detecting as an Input Acknowledge a signal which may exist in a stable "one" state for as little as 9 microseconds, allowing for the maximum permissible rise time of 6 microseconds. On sensing the Input Acknowledge, the Input Data Request (or Interrupt) may be dropped to the "zero" state anytime, but it must remain in the "zero" state at least 10 microseconds before another Input Data Request can be initiated. These relations are illustrated in Figure 4.

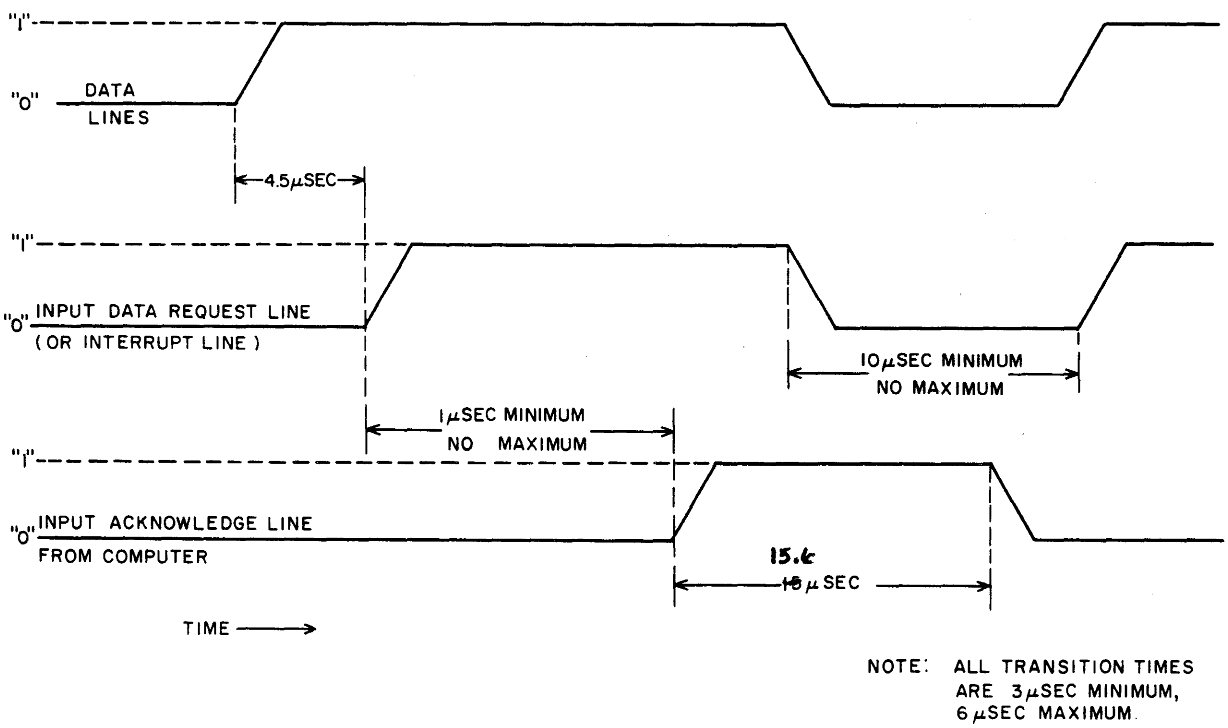

Figure 4. Timing of Input

1.6.2 Output Timing Considerations for Normal Output

The peripheral equipment must set the Output Data Request line indicating it is in a condition to accept data from the Unit Computer. This is necessary because the data will be available to the peripheral equipment for a fixed time only, nominally 24 microseconds. There is no requirement that the data lines be returned to the "zero" state before being reset to the "one" state. The time which may elapse between the request and the data being placed on the line is not fixed, but may vary from 1 microsecond upward, depending upon the computer program, the priority of the particular channel, and the data rates of the other peripheral equipment.

The Computer will put the Output Acknowledge on the line a nominal 4.5 microseconds after placing the data on the line.

The peripheral equipment must sample the data lines within 15 microseconds after the Output Acknowledge has been sent. The peripheral equipment must be capable of recognizing as an Output Acknowledge a signal which may exist in the stable "one" state for as little as 9 microseconds, allowing for a maximum permissible rise time of 6 microseconds. In view of the future desirability of speeding up the output cycle, it is recommended that new equipments be designed to operate with an "Output Acknowledge" of 12 microseconds duration which would exist in a stable "one" state for a minimum of 6 microseconds.

The Unit Computer will not recognize another Output Data Request unless the line is dropped to the "zero" state for at least 10 microseconds. These relationships are illustrated in Figure 5.

1.6.3 Output Timing Considerations for External Function Output

The External Function output is peculiar in that no response is sent from the peripheral equipment. The Unit Computer places the external function code on the 30 data lines

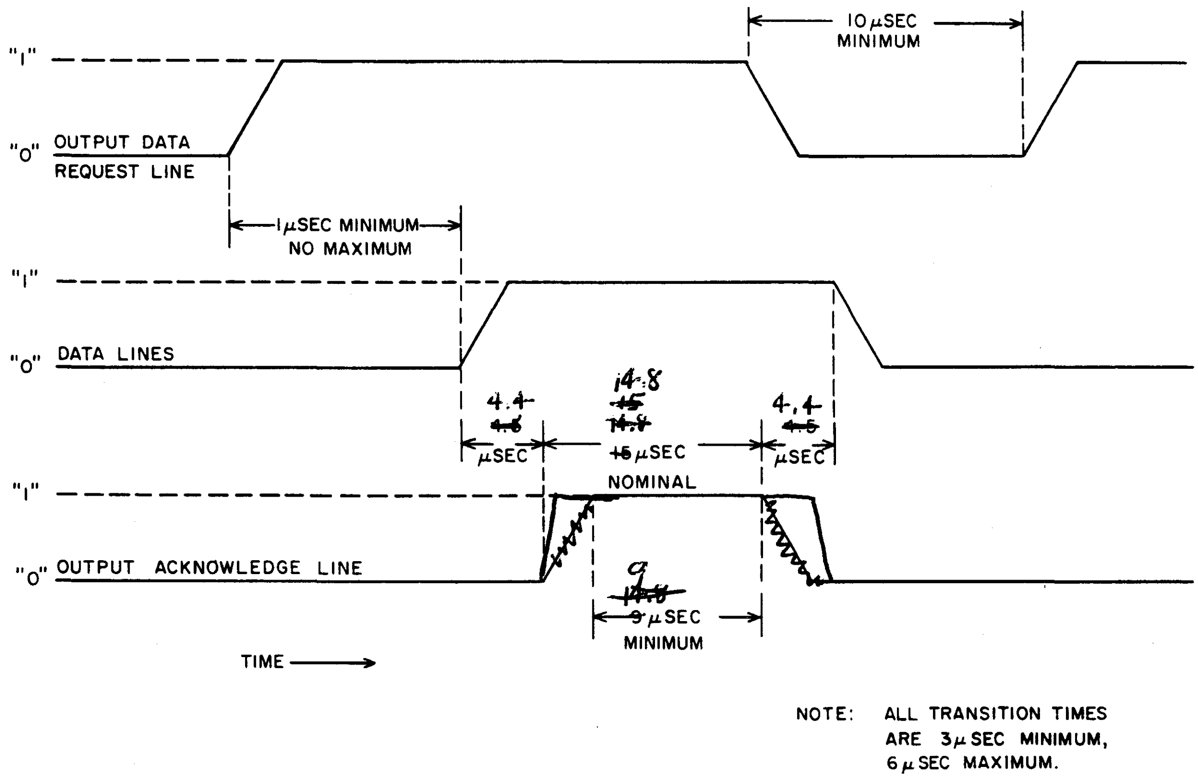

Figure 5. Timing for Normal Output

and follows 4.5 microseconds later with the External Function signal. The External Function remains for a minimum of 13 microseconds, then is dropped, followed 4.5 microseconds later by the dropping of the data lines. The External Function line will be dropped to the "zero" state for at least 10 microseconds before being reset. See Figure 6 for these relationships.

The duration of the External Function signal and the External Function code on the data lines is affected by the instruction sequence. The minimum times given above are for the worst practical case, that of an External Function instruction (13 instruction) followed by another External Function instruction. If the program restriction is made that an External Function instruction may not be followed by another External Function instruction, the times are both increased by 3 microseconds. All equipment designers should plan to operate with the shorter times.

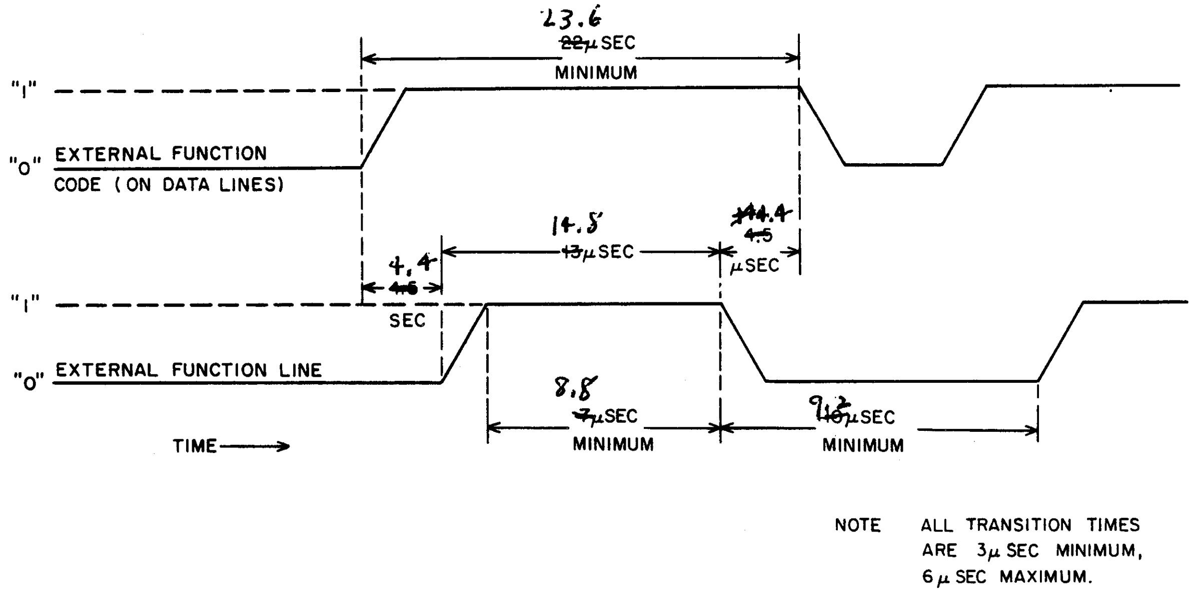

Figure 6. Timing for External Function Output

2. INPUT/OUTPUT CIRCUITRY SPECIFICATION

2.1 GENERAL

2.1.1 This portion of the specification applies to all devices which connect with the NTDS Unit Computer.

2.1.2 This specification is written to allow minimum data transfer time consistent with good engineering practice and moderate hardware requirements.

2.1.3 The binary zero and one voltage levels shall be measured at the output terminals of the computer and the output terminals of peripheral equipment with currents specified below.

2.1.4 Rise and fall (transition) times are measured from 10 per cent to 90 per cent amplitude.

2.1.5 The d-c resistance of the ground return for a cable shall not exceed 0.5 ohm.

2.1.6 For the purpose of this specification, an output circuit shall be any circuit in the Unit Computer or in the peripheral equipment that applies data or control information to an intercommunication cable in the NTDS.

An input circuit shall be any circuit in the Unit Computer or in the peripheral equipment that receives data or control information from an intercommunication cable in the NTDS.

An output circuit located in the NTDS Unit Computer will be connected to an input circuit located in the peripheral equipment. An input circuit located in the NTDS Unit Computer will be connected to an output circuit located in the peripheral equipment.

2.2 OUTPUT CIRCUITS

2.2.1 The binary one state of an output amplifier shall be 0 volt ± 1.5 volts at the terminals of the equipment under all conditions.

2.2.2 The binary zero state of an output amplifier shall be -12.5 volts ± 2.5 volts at the terminals of the equipment under all conditions.

2.2.3 In the binary one or zero state, an output circuit (located in the Unit Computer or peripheral equipment) need supply no more than a nominal 1 milliampere to any one input circuit in another equipment. Any exception to this requirement will be made only by written consent of the Bureau of Ships.

2.2.4 The waveform that any output circuit applies to any line shall have the following characteristics:

2.2.4.1 No transition whose slope is greater than 5 volts per microsecond shall be generated.

2.2.4.2 The minimum transition time shall be 3 microseconds.

2.2.4.3 The maximum transition time shall be 6 microseconds.

2.2.5 The total wiring capacity an output circuit must drive may vary from 0 to 18000 micromicrofarads if maximum cable length of 300 feet is to be used. If shorter maximum cable is permissible, capacity driving requirements may be reduced proportionally.

~~2.3 Output circuits~~ 2.3 Output circuits used for control signals must present a high impedance (100 K or greater) to the line when the power is turned off to avoid false triggering of control signals.

2.3 CHARACTERISTICS OF OUTPUT CIRCUITS

2.3.1 Data signals within the same cable:

2.3.1.1 Shall be in phase within 0.3 microsecond at all times when they change in the same direction.

2.3.1.2 Shall reach 10 per cent amplitude within 0.5 microsecond of each other when they change in opposite directions.

2.3.1.3 Shall have the same zero and one levels within ± 0.5 volt.

2.3.2 When data are to be transmitted to the computer, the Input Data Request signal will be delayed such that the 10 per cent amplitude of the Input Data Request signal occurs 4.5 microseconds ± 0.1 microsecond after the 10 per cent amplitude of the earliest data signal.

2.3.3 When an interrupt code is to be transmitted to the computer, the Interrupt signal will be delayed such that the 10 per cent amplitude of the Interrupt signal occurs 4.5 microseconds ± 0.1 microsecond after the 10 per cent amplitude of the earliest signal on the data lines.

2.3.4 When data are to be transmitted from the computer to the peripheral equipment, the Output Data Request signal must first be set in the peripheral equipment. There is a minimum delay of 1 microsecond between the computer sensing of the Output Data Request line and the computer placing data on the lines. There is no maximum limit on this delay.

2.3.4.1 After placing data on the output lines, the computer will delay the Output Acknowledge signal, such that the 10 per cent amplitude of the Output Acknowledge will occur ~~4.5~~ 4.4 microseconds ± 0.1 microsecond after the 10 percent amplitude of the earliest data signal.

2.3.4.2 The Output Acknowledge signal will be present for a minimum period of ~~15~~ 14.8 microseconds. Allowing for the maximum permissible rise time of 6 microseconds, this leaves 9 microseconds during which the data may be sampled.

2.3.4.3 The data will remain on the output lines after the signal on the Output Acknowledge line has dropped, such that 10 per cent amplitude of the Output Acknowledge line will occur ~~4.5~~ 4.4 microseconds ± 0.1 microsecond before 10 per cent amplitude of the earliest data signal.

2.3.5 When the computer transmits an external function code to the peripheral equipment, the external function code will be placed on the data lines before the External Function line is set, such that 10 per cent amplitude of the External Function signal occurs ~~4.5~~ 4.4 microseconds ± 0.1 microsecond after 10 per cent amplitude of the earliest data signal.

2.3.5.1 The External Function signal will be present for a minimum period of ~~18~~ 14.5 microseconds. Allowing for the maximum permissible rise time of 6 microseconds, this leaves ~~8~~ 3.8 microseconds during which the external function code on the data lines may be sampled.

2.3.5.2 The External Function code on the data lines will be maintained after the External Function signal has dropped, such that the 10 per cent amplitude of the External Function signal will occur ~~4.5~~ 4.4 microseconds ± 0.1 microsecond before the 10 per cent amplitude of the earliest data signal.

2.4 INPUT CIRCUITS

2.4.1 The maximum steady-state current drawn from a line by an input circuit shall not exceed 1 milliampere.

2.4.2 The input circuit shall be such that if the input wire is disconnected, the effect will be as though a zero were present at the input.

2.4.3 The threshold level distinguishing the one state from the zero state shall be -6 volts ± 1 volt at the input terminals.

2.4.4 The input circuit shall provide an integration delay of 1.5 microseconds ± 0.5 microsecond to a step function of 15 volts applied to the input.

2.4.5 The current drawn from a line by an input circuit shall have a waveshape whose slope does not exceed 0.5 milliampere per microsecond.

2.4.6 Phase relations between data signals, and between data and computer Output Acknowledge and Input Data Request signals, shall be preserved through input circuits connected to the same cable - except as they are affected by the tolerance allowed for integration delay.

2.4.7 All external equipment must adequately resynchronize all control signals, i.e., signals other than data. Resynchronization will be accomplished by sensing the transition from the "zero" to the "one" state and gating the generated signal against a steady "one" state of the control signal to guard false triggering on noise pulses.

2.5 SYSTEM REQUIREMENTS

2.5.1 The sum of the lengths of all cables connected to an output circuit shall not exceed 300 feet.

2.5.2 Voltages on the data lines must be stable before an Input Data Request signal or an Interrupt signal is sent to the computer.

2.5.3 It is recognized that cables longer than 300 feet will be necessary in certain special cases:

2.5.3.1 If a longer cable is necessary and maximum data transfer rate must be maintained, the output circuit of the peripheral equipment must be designed to meet the foregoing conditions. All parts of this specification will apply.

2.5.3.2 If a longer cable is necessary and maximum data transfer rate is unnecessary, the following parts of this specification may be modified by consent of the Bureau of Ships: 2.1.2, 2.3.1, 2.3.2, 2.3.3, and 2.4.4. In any event, 2.5.2 must be met.

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