INSTRUCTION BOOK
for

BOGART COMPUTING SYSTEM NAVY MODEL CXPK

TEST EQUIPMENT

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SECTION 1

GENERAL DESCRIPTION

1-1. GENERAL

The test equipment (see Figure 1-1) included with the Navy Model CXPK (Bogart) computer consists of a card tester unit and a Type 531 oscilloscope manufactured by Tektronix Inc., Portland, Oregon. (For information concerning the type 531 oscilloscope, refer to the instruction book accompanying this device).

The card tester unit is designed to test the printed circuit cards and certain chassis used in the Navy Model CXPK computer and associated equipment. The chassis, circuits, switches, etc. making up the tester unit are housed in a separate cabinet from the Bogart computer.

The card tester unit consists of a Test Control panel which contains the necessary indicators and selector switches to test a particular printed circuit card or chassis and a test chassis which contains the jacks in which the printed circuit cards are inserted for testing. Figure 1-2 shows the test chassis. The logic chassis and power supplies are contained within the card tester cabinet and are cooled by a 1/8 hp centrifugal blower. Figures 1-3 and 1-4 illustrate the chassis and power supplies contained in the card tester cabinet.

The logical circuits used in the card tester unit are composed of the same types of magnetic switch cards as were used in the Bogart computer. This method simplifies the overall design and reduces the number of spare cards necessary for the overall system. The card tester operates on 115 vac, 60 cps, one-phase power and 200 vac, 400 cps, three-phase power which is taken from the same motor-generator as the one supplying the Bogart computer.

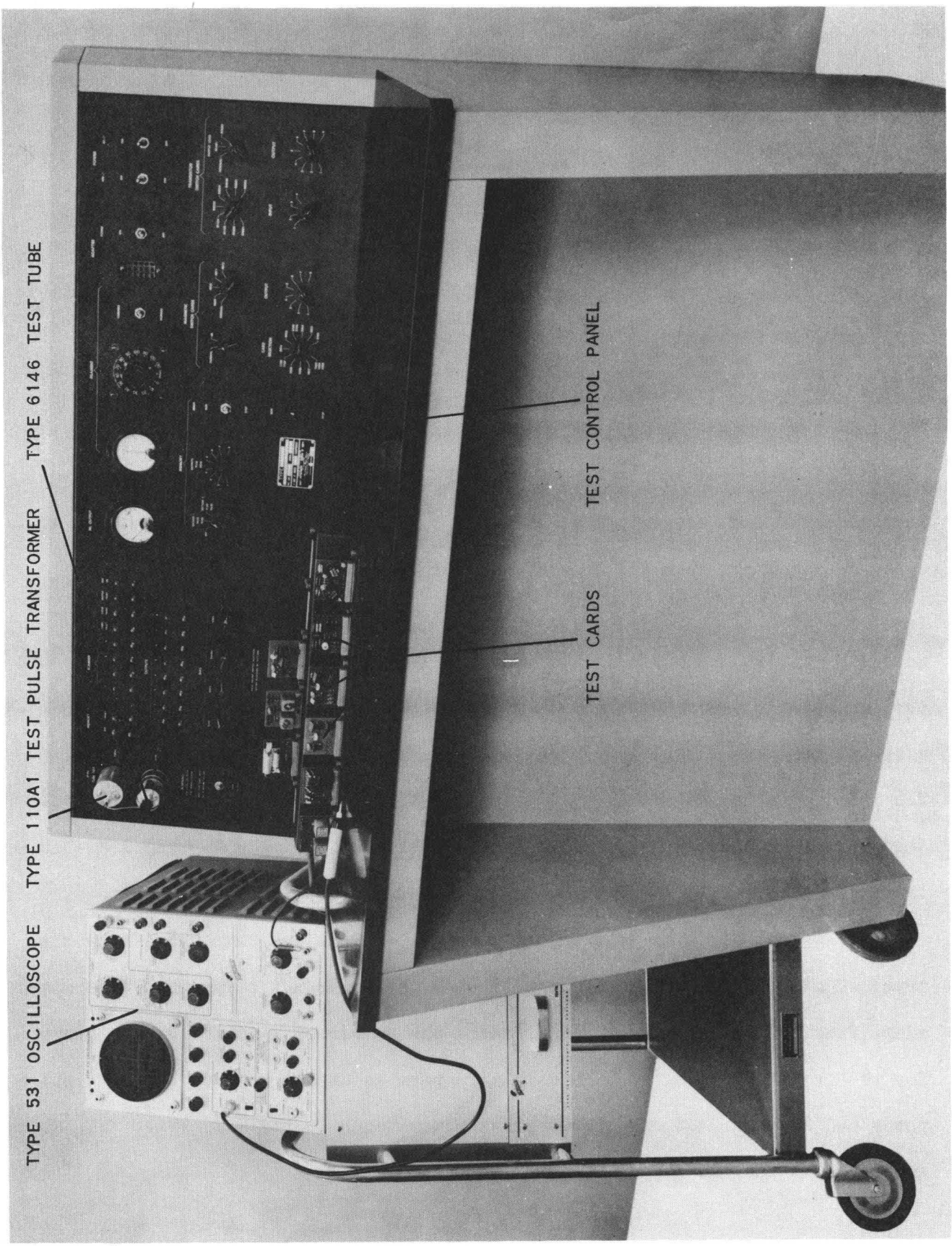

Figure 1-1. Test Equipment

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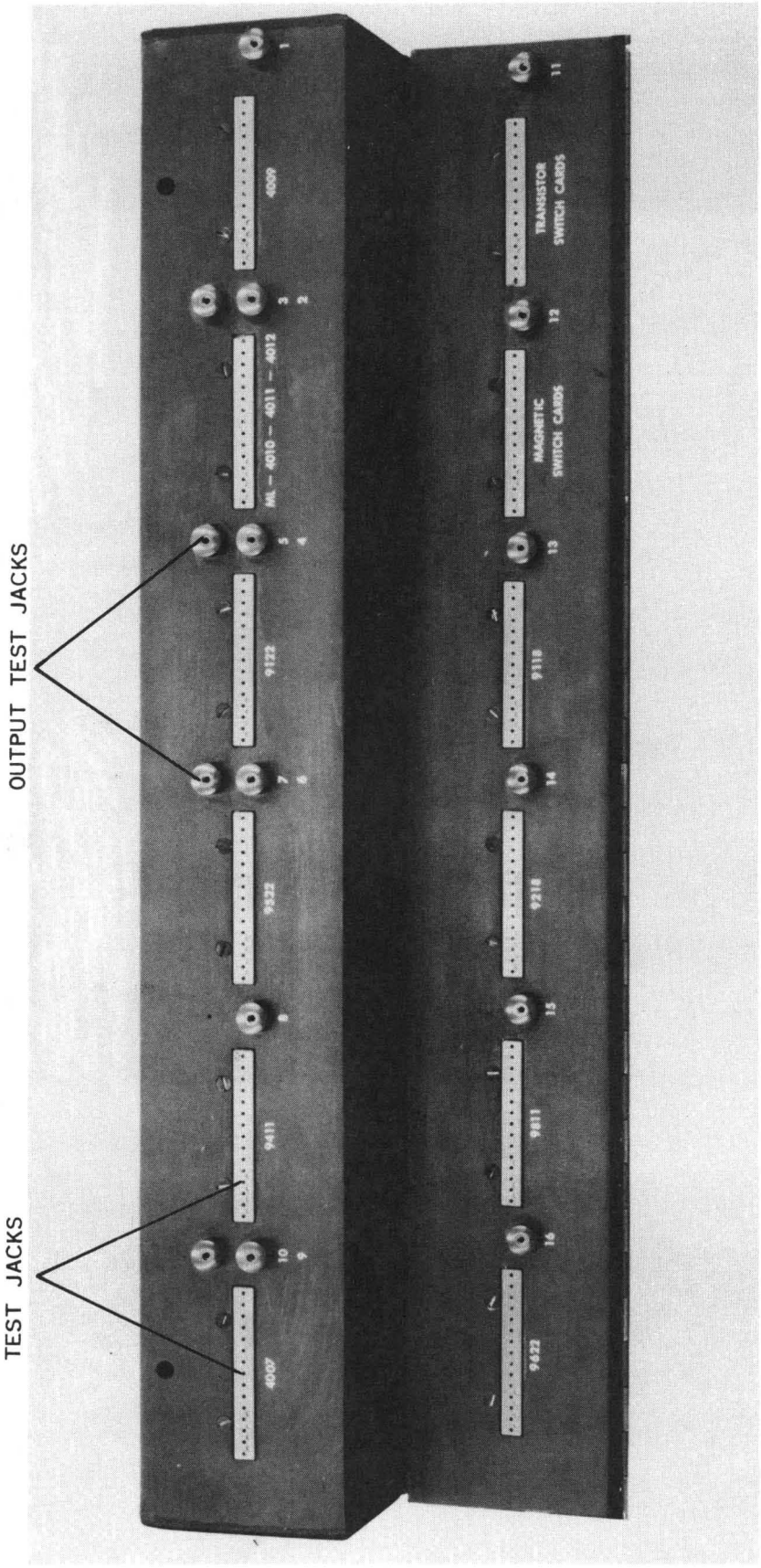

Figure 1-2. Test Card Chassis

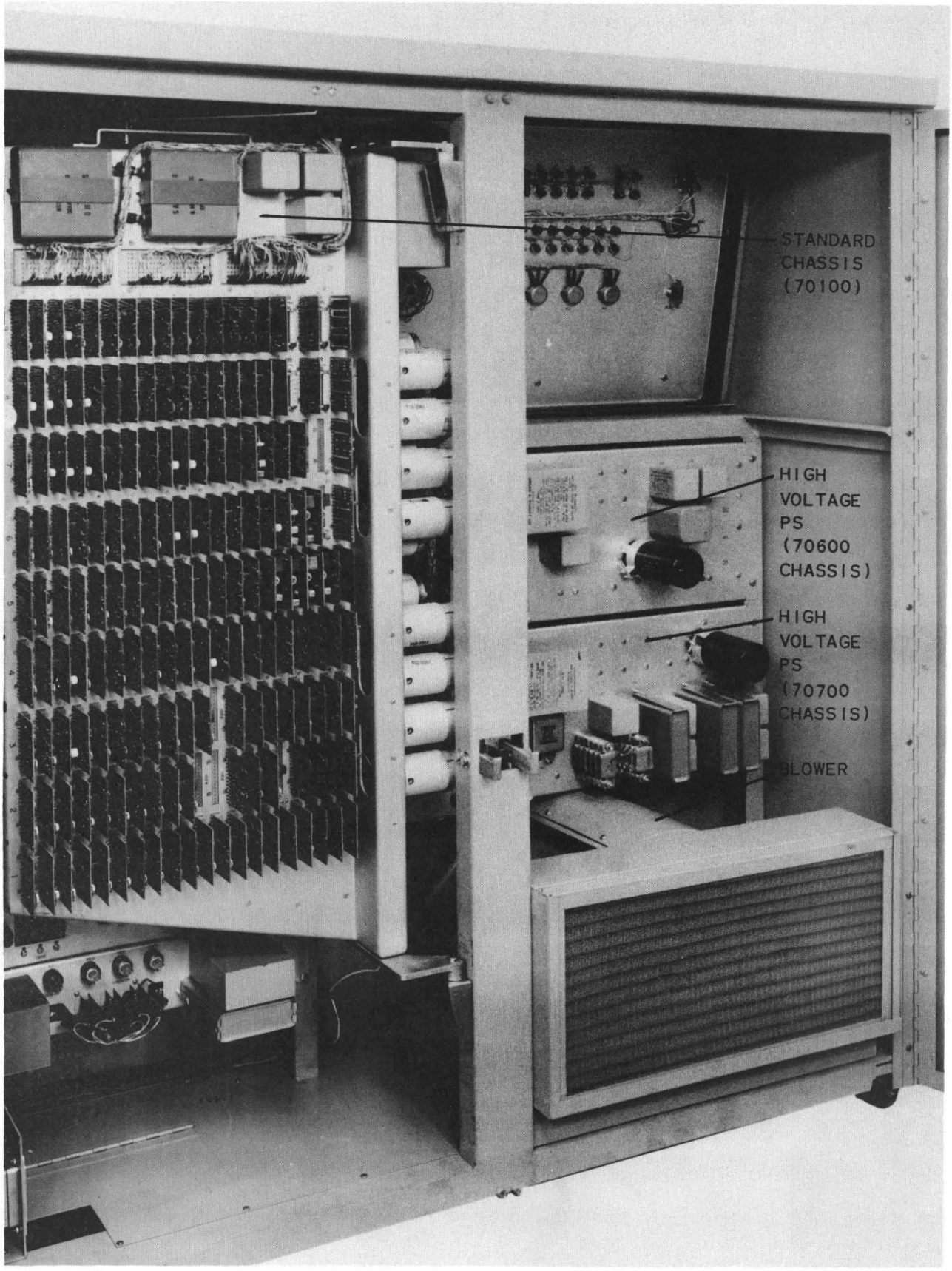

Figure 1-3. Rear of Card Tester Cabinet
(Doors Removed)

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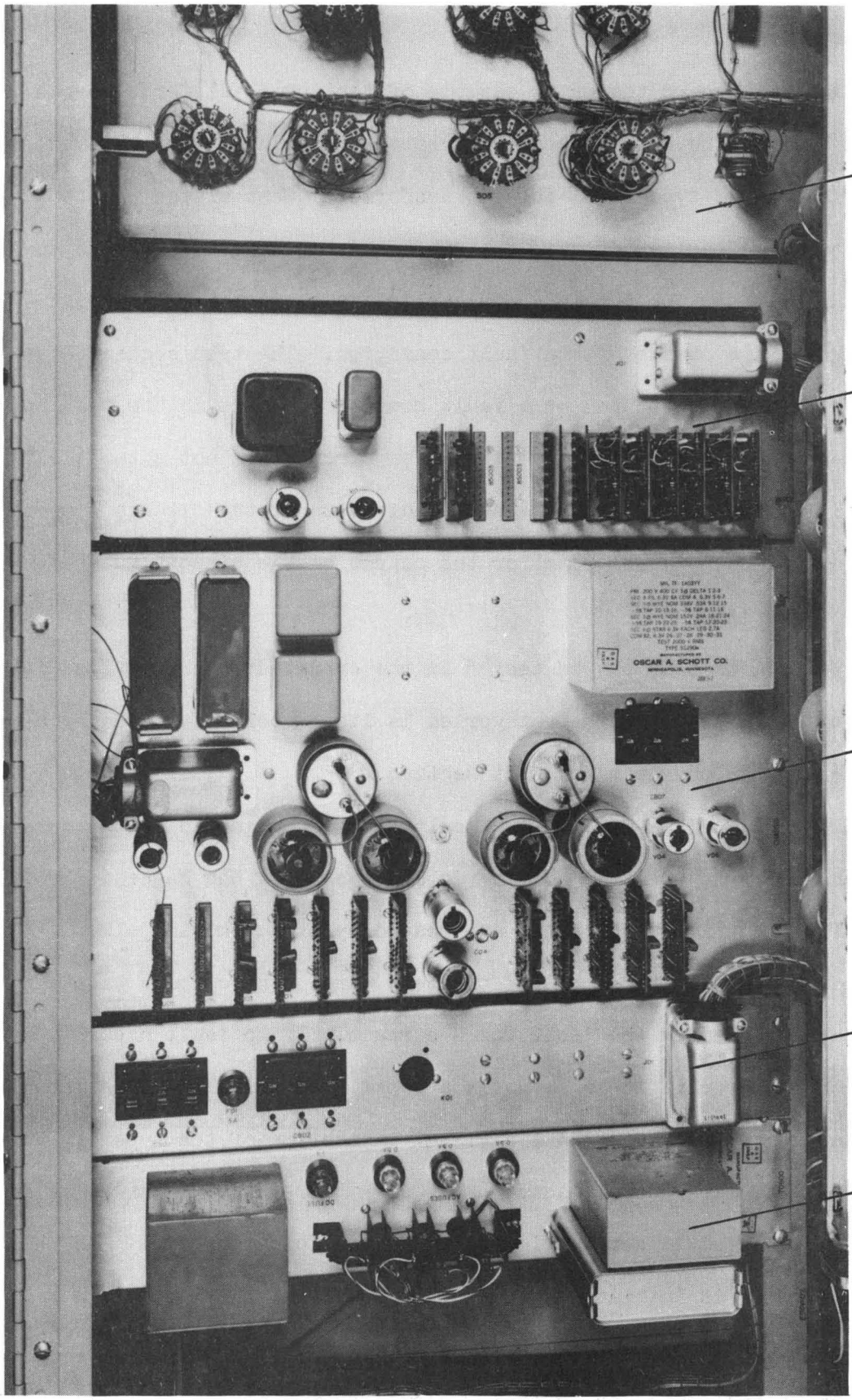

Figure 1-4. Rear of Card Tester Cabinet
(Behind the Standard Chassis)

1-2. BASIC PRINCIPLES

a. GENERAL. - The card tester is capable of testing 37 different types of printed circuit boards, the converter driver chassis, and the 6146 tube type, along with its associated type 110A1 pulse transformer. Most of the printed circuit cards tested in the card tester are subjected to an automatic test sequence in which the proper input pulses are applied to the input of the test card and the outputs are checked for a fault condition. The test sequence continues until it is manually stopped or a fault condition occurs in the test card. In some instances, the outputs of the test card or circuit are not automatically checked for a fault. In these cases a visual indication of the circuit s operation is given on the Test Control panel or the output of the circuit is monitored with an oscilloscope.

The types of circuits that can be tested in the card tester are divided into six basic catagories. Each of these catagories is listed below followed by a brief description of the operation of that section.

b. MAGNETIC SWITCH TEST SECTION. - The 15 types of magnetic switch cards, the M-L cards and the type 4011 and 4012 cards are tested in the Magnetic Switch Test section. The magnetic switch cards are tested by an automatic pulse sequence which is applied to the input of the test card. The outputs of the test card are then checked by the Fault Check circuit. If no fault occurs, the test sequence continues until it is manually stopped. If a fault occurs, however, the test sequence terminates, and a visual indication of the type of fault is given on the Test Control panel.

The M-L card is tested in conjunction with a magnetic switch card. In this test, the test sequence is initiated through the manual set portion of the M-L card, and the output of the card is checked by observation of the M-L Output meter on the Test Control panel or by oscilloscope monitoring.

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The transistor input (4011) card is checked by the application of a standard transistor switch card input to the inputs of the test card. The outputs of the 4011 test card are applied to the input of a magnetic switch card. The output of the magnetic switch card is then monitored by an oscilloscope.

The line driver (4012) card is also checked in conjunction with a magnetic switch card. The output of the magnetic switch card is applied to the input of the line driver with the output of the line driver being monitored with an oscilloscope.

c. TRANSISTOR SWITCH CARD TEST SECTION. - Nine types of transistor switch cards (types 85001 and 85002 cards are included in this section) are checked in this section. In general, a particular transistor switch card is checked by applying the output of a standard transistor switch to the inputs of the transistor switch test card, and then observing the output wave-form of the test card with an oscilloscope.

d. MEMORY CARD TEST SECTION. - This section checks the printed circuit cards used in the Magnetic Core Storage (Memory) section of the Bogart computer. A particular memory card is tested by inserting it in the proper test jack; the remaining memory section test jacks being filled with their corresponding pre-tested memory cards. It is important to note at this point that all of the memory test jacks must be filled with their corresponding cards before this section can function.

The memory card test section functions in conjunction with two memory cores which are suspended on their respective control wires and are mounted on the 70300 chassis. The test consists mainly in the selection of one of these cores. This core remains selected for a 128 microsecond period during which the four following phases of the test take place:

1) A "1" is written in the memory core.

2) The memory card test section is checked for a "1" output of the memory core.

3) A "0" is written in the memory core.

4) The memory card test section is checked for a "0" output of the memory core.

After the completion of the four phases listed above, the other memory core is selected and the same four phases are repeated for that core.

The failure of either the "1" or "0" fault check causes an indication of the type of fault to appear on the Test Control panel and the Scanner circuit to stop (if the Memory Error switch is in the STOP position). Since each doubtful memory card is tested in conjunction with six other memory cards known to be functioning properly, it is evident that a failure of the memory test section indicates that the doubtful test card is not functioning properly.

e. RESYNC DELAY TEST. - The two resync delay cards (4009 and 4010) are tested as one part of a resync delay circuit with the other part being composed of a standard 4009 and 4010 card. The output of this resync delay circuit is then compared with a standard resync delay circuit to determine whether the test 4009 or 4010 card is functioning properly.

f. 6146 TUBE, 110A1 TRANSFORMER, AND 4007 CARD TEST. - In general, these three units are tested conjunctively by the application of rp0 and rp1 (from the Clock circuit) to the AND input in the 4007 card. The output of the 4007 test card is then applied to the control grid of the 6146 tube which subsequently produces the transfer pulse through the 110A1 pulse transformer. The output of the pulse transformer and the grid of the 6146 tube may be monitored with an oscilloscope to determine whether the unit being tested is functioning properly.

g. CONVERTER DRIVER CHASSIS TEST. - The four converter driver chassis may be tested by the card tester unit through the use of the driver chassis adapter.

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Figures 1-6 and 1-5 respectively, show views of the driver chassis adapter with and without an attached converter driver chassis.

A converter driver chassis is tested by attaching it to the adapter and by plugging the adapter plug in the proper jack on the card tester. The card tester applies the pulse input to a particular driver stage depending upon the position of the Driver Stage selector. The output of the converter test chassis is tested by monitoring the selected output with an oscilloscope.

1-3. MAINTENANCE OF THE CARD TESTER

The general trouble shooting and maintenance of the card tester unit is accomplished in a manner similar to that used in the Bogart computer. The major difference is that there are no maintenance tests for the card tester since the card tester does not function in conjunction with the computer. The maintenance procedures given in Bolume 4 of the "Instruction Book for the Bogart Computer, Navy Model CXPK" is used for the maintenance of the card tester with the exception of the maintenance test programs. A valuable aid in the trouble shooting of the card tester is the logic and circuit diagrams which are found in Volume 11 of the Bogart instruction book.

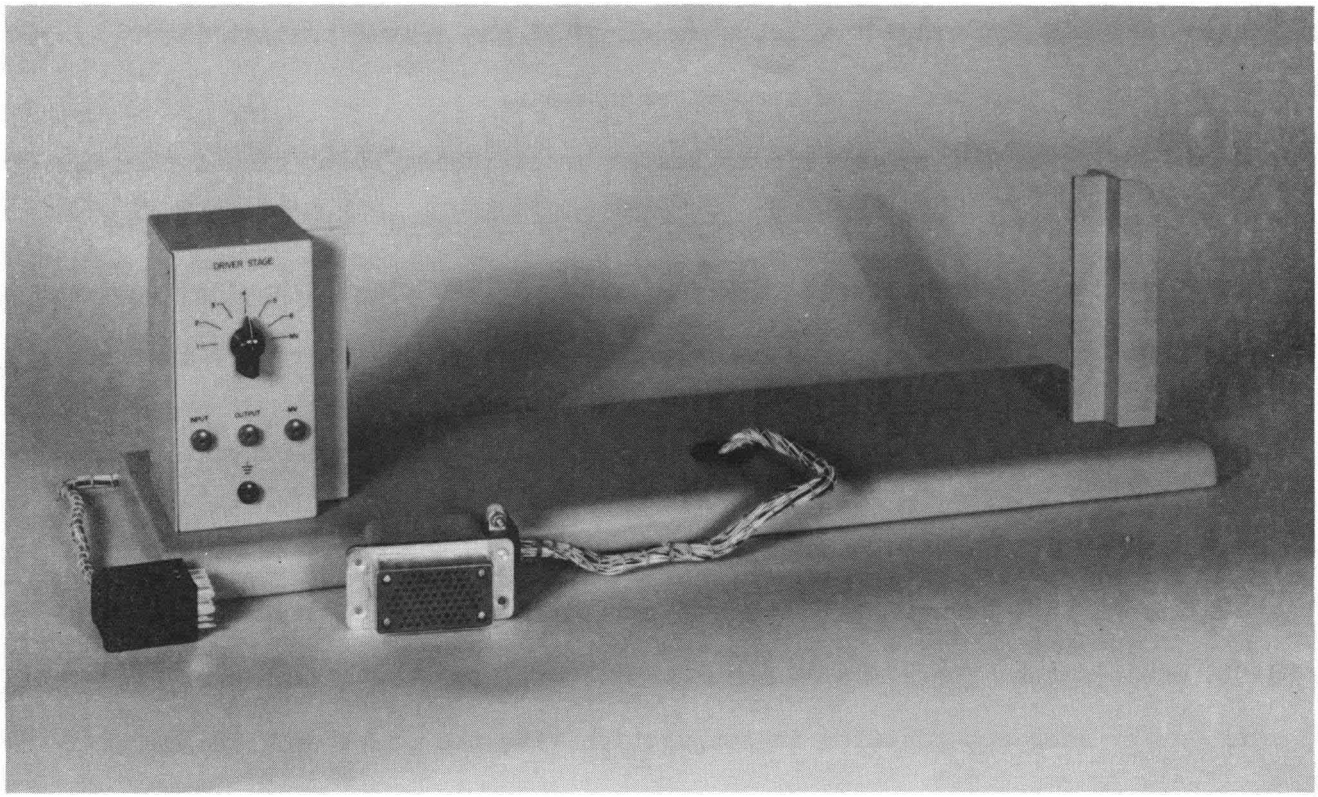

Figure 1-5. Converter Driver Chassis Adapter

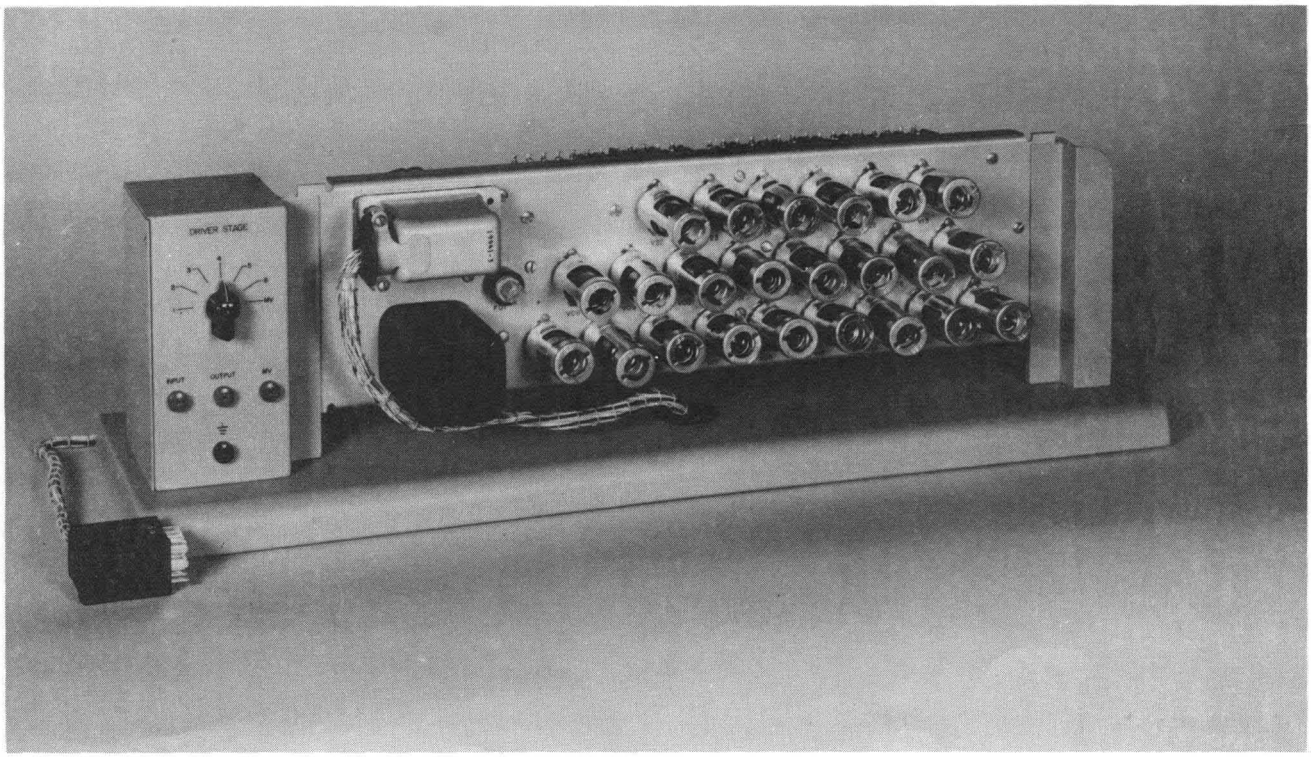

Figure 1-6. Converter Driver Chassis Adapter
(With Attached Driver Chassis)

SECTION 2

OPERATION

2-1. GENERAL

The operational section is devoted to the listing of procedures involved in placing the card tester in operation and in operating the tester when it has been properly prepared.

This section concerns the geneal operation of the card tester unit. Detailed procedures involved in the testing of each individual printed circuit card or other unit are given in Test Procedures which are contained in an accompanying volume.

2-2. TURNING ON THE EQUIPMENT

There are two power switches that must be activated in order to apply power to the card tester unit. These are the 60-Cycle and 400-Cycle Power switches which are both contained on the Test Control panel (see Figure 2-1). Placing both of these switches in the ON position applies power to the tester.

CAUTION

THE 60-CYCLE POWER SWITCH MUST BE TURNED ON WHENEVER
400-CYCLE POWER IS APPLIED TO THE CARD TESTER IN ORDER
TO PREVENT OVERHEATING OF THE CABINET.

2-3. TEST CONTROL PANEL

The Test Control panel provides a means of controlling the operation of the card tester unit and of visually observing the results of some tests.

a. INDICATOR SECTION. - The indicator lights for the card tester circulation bits are contained in the upper left hand corner of the Test Control panel (see Figure 2-1). Each pair of indicator lights (upper and lower light) corresponds to a circulation bit. The indicator lights are connected so that when

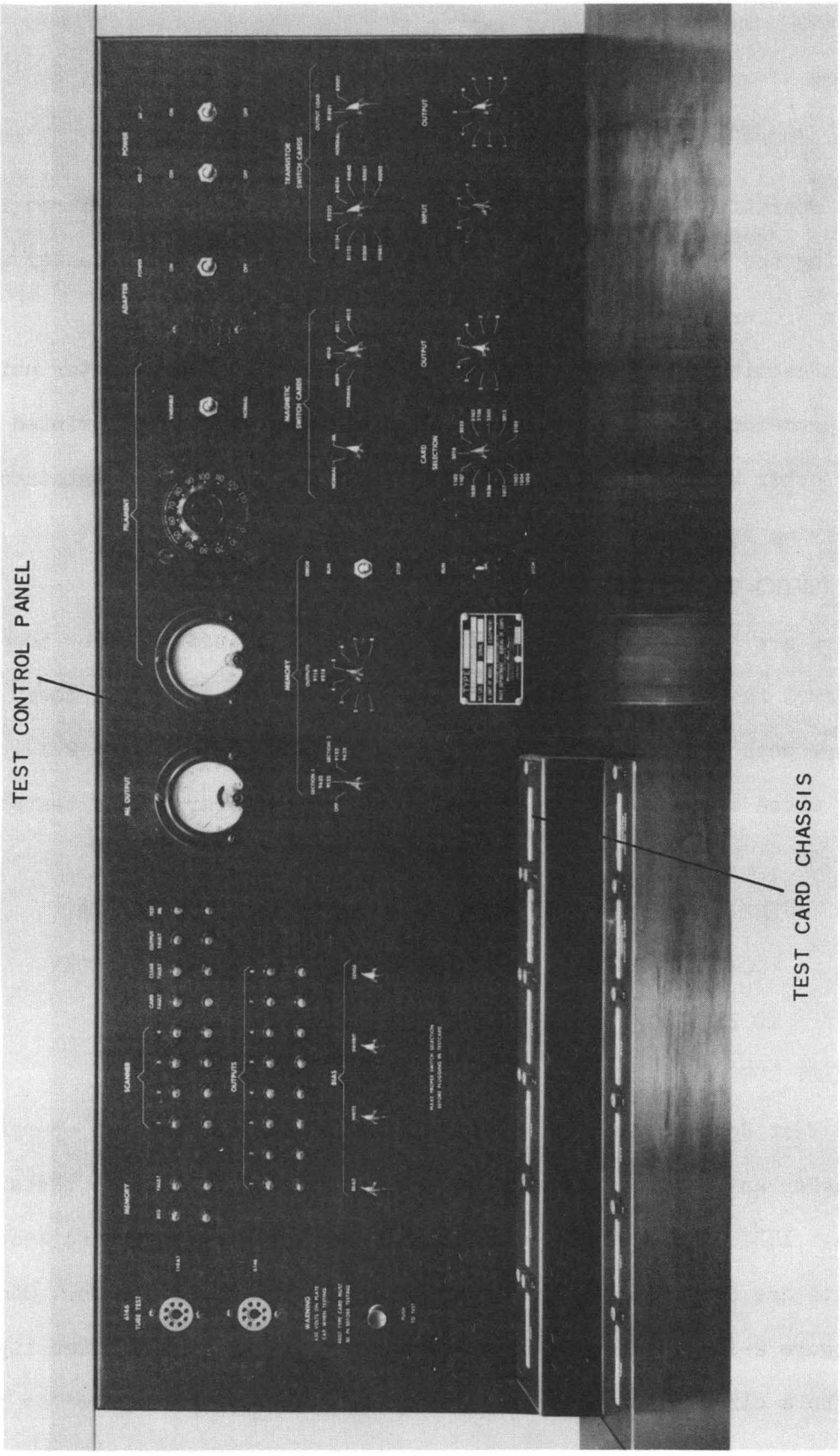

Figure 2-1. Test Control Panel and Test Card Chassis

the corresponding circulation bit is set (in the "1" state) the upper light is lit, and when the bit is cleared (in the "0" state) the lower light is illuminated. The indicator lights are divided into four groups, each of which is discussed below. In the discussion that follows, an indicator is said to be illuminated when the corresponding circulation bit is in the "1" state. (Upper light is lit.)

(1) MEMORY INDICATORS. - There are two indicator lights associated with the Memory Test section. These are the Memory circulation bit and Memory Fault indicators. The Memory circulation bit indicator is illuminated whenever the Memory circulation bit is set, i.e. whenever a "1" is read from the selected memory core. The Memory Fault is illuminated whenever a fault is detected by the Memory Card Test section.

(2) SCANNER INDICATORS. - There is an indicator in this group for each of the four Scanner stages. When a Fault stop occurs during a test procedure, the phase of the test during which the fault occurred can be determined by observing which Scanner indicator is presently illuminated.

(3) FAULT INDICATORS. - Each indicator in this group provides an indicaton of what fault occurred (if any) during a test sequence.

(a) CARD FAULT. - This indicator is illuminated whenever the magnetic switch test card fails to set during the normal test sequence.

(b) CLEAR FAULT. - This indicator is illuminated whenever the magnetic switch test card fails to clear during a normal test sequence.

(c) OUTPUT FAULT. - The illumination of a particular Output Fault indicator denotes that the corresponding output diode in the magnetic switch test card is open.

(4) OUTPUT INDICATORS. - Each of the eight indicators in this group coincides with the corresponding Output circulation bit in the Magnetic Switch Test section. These indicators provide a means of determining which of the

output diodes on the magnetic switch card are open when an Output Fault occurs.

b. M-L OUTPUT METER. - The M-L Output Meter (top cener of Test Control panel, Figure 2-1) provides a relative output voltage reading for the M-L test card during "1" and "0" outputs. The M-L test procedure contained in the "Test Procedures" volume, gives the proper readings of this meter for "1" and "0" outputs of the M-L test card.

c. FILAMENT CONTROL. - The filament control consists of a variac and a voltmeter mounted on the Test Control panel. The variac controls the amount of filament voltage applied to the 6146 test tube or to the tube on the 9411 test card. The variac is effective only when the Filament switch is in the VARIABLE position.

d. ADAPTER CONTROL. - The converter driver chassis adapter control consists of the adapter input plug and the adapter power switch. The 15-pin input plug to the adapter is plugged into the polarized 15-pin jack on the Test Control panel. The power switch applies power to the converter test chassis through the adapter.

e. MEMORY TEST SECTION CONTROL. - The Memory Test Section control consists of two selector switches and the Memory Error switch.

(1) OFF-SECTION 1-SECTION 2. - This three-position selector determines which of two sections on the 9622 and 9122 cards is to be tested. It should be noted that if the position of this selector is altered during the course of the Memory test a Memory Fault will occur.

(2) 9118 AND 9218 OUTPUT SELECTOR. - This eight-position selector determines which of the eight outputs of the 9118 and 9218 card is to be tested. Changing the position of this indicator during the memory test will cause a Memory Fault to occur.

(3) MEMORY ERROR SWITCH. - In order to stop the memory test sequence

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when a fault occurs, the Memory Error switch must be placed in the STOP position. Conversely, if this switch is placed in the RUN position, the test sequence will not stop when a fault is detected although a visual indication of the fault will be given on the Test Control panel.

f. MAGNETIC SWITCH CARD TEST CONTROL. - The magnetic switch card test control consists of the following four selector switches:

(1) NORMAL-ML SELECTOR. - For the testing of a standard magnetic switch card this selector is placed in the NORMAL position. Conversely, this switch is placed in the ML position for the testing of the M-L card.

(2) NORMAL-4009-4010-4011-4012. - For the testing of all standard magnetic switch cards and M-L cards, this switch is placed in the NORMAL position. For the testing of a resync delay card (4009 or 4010), this switch may be in either the 4009 or 4010 position. During the test of the 4011 and 4012 cards, the switch is placed in the appropriate position.

(3) CARD SELECTION SWITCH. - This switch is placed in the position corresponding to the type number of the magnetic switch card being tested.

(4) OUTPUT SELECTOR. - During the testing of a magnetic switch card, this switch is placed in the position corresponding to the number of outputs on the magnetic switch card being tested.

g. TRANSISTOR SWITCH CARD TEST CONTROL. - The transistor switch card test control consists of the following four selector switches:

(1) TRANSISTOR SWITCH TYPE SELECTOR. - This switch is placed on the number corresponding to the transistor switch type being tested.

(2) OUTPUT LOAD SELECTOR. - This switch determines the proper output load for the transistor switch card type being selected. In the case of all transistor switch types other than the 81001 and 85002 types, the switch is placed in the NORMAL position. When testing the 81001 or 85002 types the switch

switch is placed in the corresponding position.

(3) INPUT SELECTOR. - The Input selector is placed in the position corresponding to the number of inputs of the card type being tested.

(4) OUTPUT SELECTOR. - This switch is placed in the position corresponding to the number of outputs on the transistor switch being selected.

2-4. TEST CARD CHASSIS

The Test Card chassis is located at the lower left portion of the Test Control panel and is partially recessed in the table portion of the card tester cabinet (see Figure 2-1). The Test Card chassis is hinged at its lower end to allow easy access to the wiring side. Figure 2-2 shows a detailed view of the Test Card chassis.

The Test Card chassis contains the 15-pin connector jacks (test jacks) for receiving the test cards. The Test Card chassis also contains the output test jacks for oscilloscope monitoring of the test card. Some of the test jacks are used in the testing of an entire group of test cards, e.g. the magnetic switch card test jack, while the others are used in the testing of one type of card only.

2-5. TURNING OFF THE EQUIPMENT

The 400- and 60-cycle power is removed from the card tester by placing the 400-Cycle and 60-Cycle Power switches in the OFF position. However, it is advisable to leave the 60-Cycle Power switch on for approximately five minutes after removing the 400-cycle power source. This allows the blower to cool the unit more rapidly.

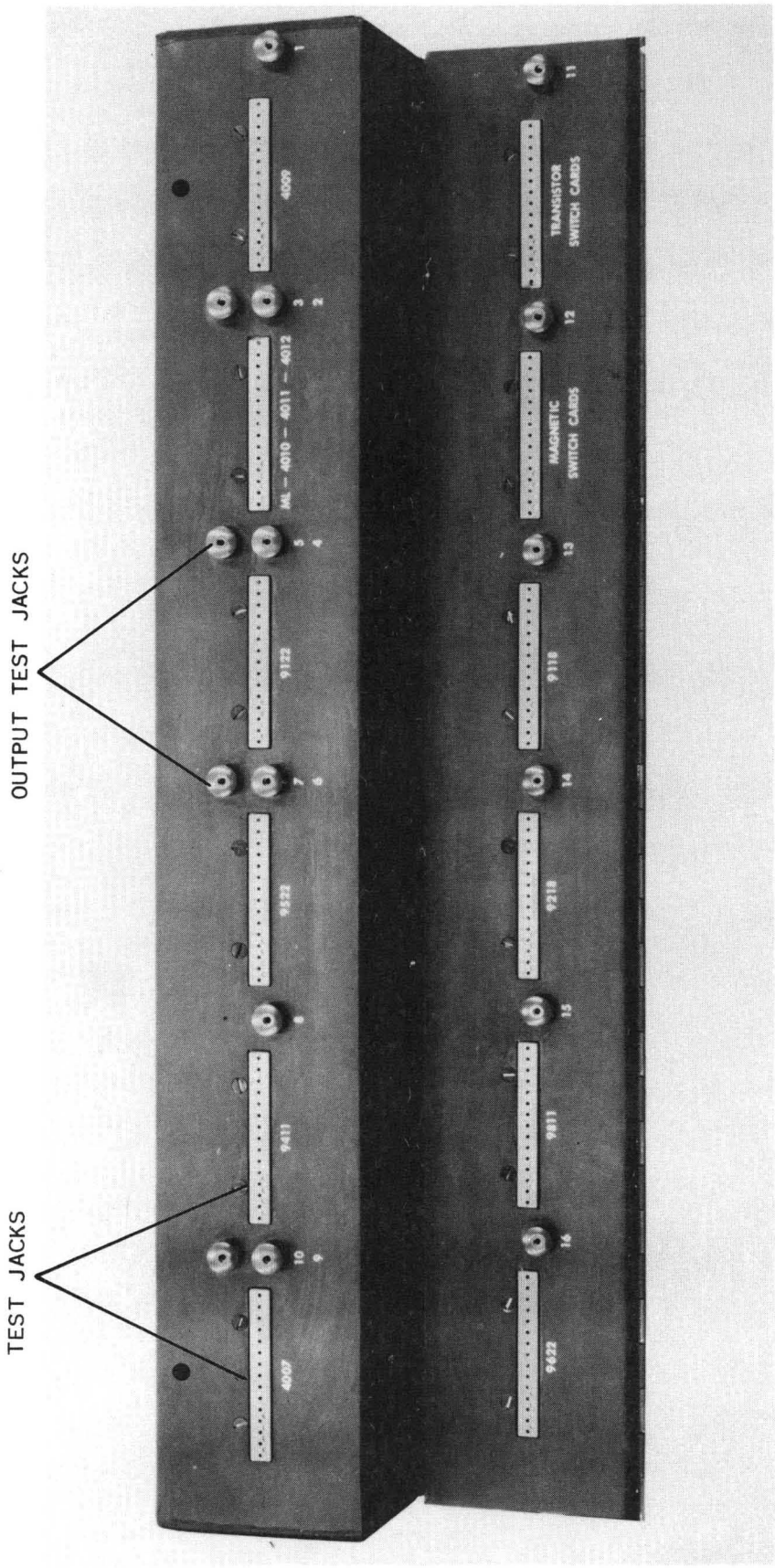

Figure 2-2. Test Card Chassis

THEORY OF OPERATION
SECTION 3

3-1. GENERAL

The card tester unit contains the circuits necessary to test the electrical operation of most printed circuit cards used in the Navy Model CXPK computer and its associated external equipment. In addition the card tester can be used to check the Converter Driver chassis through the use of an adapter. Tube type 6146 and the type 110A1 pulse transformer can also be tested by the card tester.

A particular printed circuit card is tested by inserting it in the proper test jack and making the proper adjustments and selections on the Test Control panel (see Figure 2-1). After the Run switch is placed in the RUN position, the tester automatically supplies the correct pulses or voltage levels to the input(s) of the card under test and in most cases checks the card for the proper pulse or voltage level outputs. In some instances, viz. the transistor switch cards, an oscilloscope must be used to check the output voltage levels. In cases of an automatic test sequence, the sequence is repeated until the Run/Stop switch is placed in the STOP position or until the card fails to function properly. It is sometimes useful to use the oscilloscope with the card tester unit. Although the outputs of the test card are checked automatically, test jacks are available on the card chassis for scope monitoring, but test points on the card are a greater aid in some cases.

The types of printed circuit cards that can be tested by the card tester are divided into three major catagories as follows: Memory (Magnetic Core Storage), Transistor Switch, and Magnetic Switch cards. In addition, certain other card types can be tested. These are the Converter Driver chassis, Resync Delay circuit (4009 and 4010), Transistor Input (4011), M-L cards, and Line Driver (4012) cards.

The following sub-paragraphs discuss the operation of the card tester for each of the card types mentioned above, in addition to a discussion of the Clock circuit, power supplies, and cooling system which affect the entire card tester unit.

3-2. CLOCK CIRCUIT

The Clock circuit used in the card tester unit is electrically identical to the Bogart Clock. As a result, the card tester Clock circuit produces a four-phase pulse sequence in an identical manner to the Clock in the Bogart system. The logical circuits in the card tester are composed of magnetic switch circuits which also are identical to those used in the Bogart computer. This method reduces the number of printed circuit types in the overall system and also simplifies maintenance of the equipment.

The Clock circuit is contained on the Clock chassis (70400) which is also identical (physically and electrically) to the corresponding chassis in the Bogart converter (see Diagram 87647, Volume 12, page 35) except that +450 and +200 vdc is brought out of the card tester Clock power supply to a set of relay contacts in the Relay chassis (70500). Because of the identity of the Bogart system and card tester Clock circuits, the Clock circuit theory of operation is not contained in this volume; reference is made to the Instruction Book for Bogart Computing System, Navy Model CXPK , Volume 2, Section 4.

3-3. MAGNETIC SWITCH TEST SECTION.

a. GENERAL. - The Magnetic Switch Test section of the card tester automatically tests the operation of the magnetic switch cards. In addition this section functions in conjunction with other circuits to test the M-L, Transistor Input (4011), and Line Driver (4012) cards. The major portion of the Magnetic Switch Test section is devoted to the testing of the magnetic switch cards since the remainder of the cards tested by this section operate in conjunction with a

magnetic switch. For this reason, the operation of the Magnetic Switch Test section is first discussed for the testing of the standard magnetic switch cards.

b. MAGNETIC SWITCH CARD TESTING. - The testing of the magnetic switch cards is largely controlled by the selections made on the Test Control panel. In order to test a particular type of magnetic switch card, the two upper switches in the Magnetic Switch card section of the Test Control panel must be in the NORMAL position (see Figure 2-1). In addition, the Card Selection switch must be set to the type number of the card to be tested and the Output switch must be set to the number of outputs on the test card. These selections enable the automatic testing of the desired magnetic switch card when the Run/Stop switch is placed in the RUN position. The test card is then automatically subjected to a test sequence which includes the checking of each output diode for an opening, the setting and reading of the core on the test card to determine if it is setting properly, and if the particular test card contains a Clear input, whether the core is clearing after it has been set. If one or more of these tests fail, the appropriate circulation bit in the fault circuit is set and the corresponding indicator on the Test Control panel is illuminated. The occurrence of most faults stops the test sequence in the phase of the test where the error occurred. The detected types of magnetic switch card faults are the Zero Fault (open output diode), Card Fault (magnetic switch core fails to set), and the Clear Fault (test core fails to clear on the negation portion of the test sequence). The timing of the test sequence is basically controlled by the Time Delay circuit which delays a pulse for 32 microseconds. The delayed timing pulse then sets the Scanner circuit in operation. The Scanner circuit controls the sequence of pulses transmitted to the test card in order to set the test core through each input and, if the test card has a clear input, to clear the test core at the proper time. The Scanner circuit is made up of four stages which determine the

input to which the pulse is applied. A different Scanner stage is set every 32 microseonds. For example, if Stage one was the last stage set, Stage two will be set 32 microseconds later. After Stage four has been set, Stage one is again set 32 microseconds later by the following timing pulse. This cycle is continuously repeated until the Run/Stop switch is placed in the STOP position or until a fault is detected.

The actual checking portion of the magnetic switch test is performed by the Fault Check circuit. Depending upon the output selection, up to eight outputs of the test card are checked for a Zero fault. Output 1 is sensed by the Fault Check circuit to determine whether a Clear or a Card Fault condition exists in the test card.

(1) TIME DELAY CIRCUIT. - The Time Delay circuit (see Diagram 186820, Volume 11, page 20) produces a timing pulse every 32 microseconds in order to set the proper stage of the Scanner circuit and to control the general timing sequence of the Magnetic Switch Test circuit.

The first stage of the Time Delay circuit is composed of C^{00}_{06} and C^{20}_{06}. Core C^{00}_{06} is unconditionally set at time 2 . At time 0, C^{00}_{06} is read out, and C^{20}_{06} is set. At time 2, B^{30}_{01} is set by the output of C^{20}_{06}. Thus, four microseconds after C^{00}_{06} is first set, the second stage is set. The second stage of the Time Delay circuit is composed of C^{30}_{01}, B^{30}_{01}, and C^{10}_{01}. On the tenth microsecond after B^{30}_{01} is first set, B^{00}_{02} is set. The third stage, composed of C^{00}_{02}, B^{00}_{02}, and C^{20}_{02}, functions identically to the second stage. On the 18th microsecond after B^{00}_{02} is first set, B^{10}_{03} is set. On the following time 1, B^{10}_{03} is read out and the timing pulse is produced. After 32 microseconds, B^{10}_{03} produces another pulse. This

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All drawing references refer to Volume 11, General Circuit Diagrams of the CXPK computer (Bogart) instruction book.

All time periods refer to the clock pulses produced by the Clock circuit (see Paragraph 2 of this section).

sequence is continued until the clock source is removed.

(2) RUN/STOP CONTROL. - The Run/Stop control circuit (see Diagram 186820) is composed of the Run (G^{00}_{02}- G^{20}_{02}), Normal (G^{20}_{01}- G^{00}_{01}), and Stop (G^{20}_{00}- G^{00}_{00}) circulation bits. Each of these circulation bits is controlled by its respective switch on the Test Control panel and the 32 microsecond timing pulse.

The first timing pulse produced by B^{10}_{03} sets B^{20}_{03}. The pulse output of B^{10}_{03} also negates B^{21}_{03}. At time 2, the output of B^{20}_{03} probes the AND inputs to each of the three circulation bits mentioned above.

(a) RUN/NORMAL. - If one of the standard magnetic switches is to be tested, the Run/Stop switch is placed in the RUN position and the Normal/M-L switch is placed in the Normal position. As a result, when B^{20}_{03} produces an output pulse, the Run (G^{00}_{02}- G^{20}_{02}) and Normal (G^{00}_{01}- G^{20}_{01}) circulation bits are set. The setting of these two bits begins the magnetic switch test sequence.

It can be noted by referring to Diagram 186820, that at the time B^{20}_{03} is set by the first timing pulse, B^{21}_{03} is negated. This does not prevent the setting of the Run circulation bit if the Run/Stop switch is in the RUN position. However, on each succeeding timing pulse, the normal circulation path of G^{00}_{02}- G^{20}_{02} is disabled by the negation of B^{21}_{03}. Thus, the Run circulation bit remains set only as long as the Run/Stop switch is held in the RUN position. When this switch is released (the switch returns to the neutral position), the next timing pulse causes the negation of B^{21}_{03} and as a result, the Run circulation bit is cleared until the Run/Stop switch is again placed in the RUN position.

It can also be noted that the first timing pulse (i.e., the first output of B^{20}_{03}) does not actually initiate the operation of the Scanner circuit. This is due to the fact that G^{20}_{02}, which is in the Run circulation bit, is not set until two time periods after B^{20}_{03} is read out. As a result, B^{30}_{04} is not set until the

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next timing pulse is produced.

(b) STOP. - The Stop circulation bit (G^{00}_{00}- G^{20}_{00}) is set on a timing pulse if the Run/Stop switch is in the STOP position. The normal circulation of the Stop circulation bit is disabled on the timing pulse following the time it was first set. Thus, the Run/Stop switch must remain in the STOP position in order for the stop circulation bit to remain set. When the Run/Stop switch is allowed to return to the neutral position, the following timing pulse will negate B^{21}_{03} which results in the disabling of the Stop circulation bit. Regardless of the speed with which the Run/Stop switch is removed from the STOP position, the output of G^{20}_{00} will have ample time to perform its designated function.

The setting of the Stop circulation bit causes B^{30}_{03} to be set on the following timing pulse (if the Normal circulation bit is set). When B^{30}_{03} reads out, it negates each stage of the Scanner circuit, the Normal circulation bit, and both the Card and Clear Fault circulation bits (see Diagram 186820, Volume 11, page 21). In addition, the output of B^{30}_{03} sets B^{10}_{04}, which negates W^{20}_{00}. This prevents Stage one of the Scanner from remaining set even though W^{00}_{00} is negated at time 3 by the output of B^{30}_{03}. If B^{10}_{04} were not in the circuit, Stage one could remain set after a Stop through the setting of W^{20}_{00} by the ANDed outputs of B^{00}_{05} and B^{00}_{04}. As a result, the test sequence would continue even though the Run/Stop switch were placed in the STOP position.

(3) SCANNER CIRCUIT. - The Scanner circuit is composed of four stages which produce the initial input pulses to the magnetic switch card under test. In general, the Scanner circuit controls the basic timing sequence of the input pulses for the Magnetic Switch test section. The operation of the Scanner circuit is initiated on a timing pulse when B^{00}_{04} and B^{00}_{05} are set. The setting of these two cores causes the first stage of the Scanner (W^{00}_{00}- W^{20}_{00}) to be set. In

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addition, the output of B^{30}_{04} initiates the control core chain (N cores) by setting N^{10}_{01}. The output of B^{30}_{04} also negates the Normal circulation bit (G^{00}_{01}- G^{20}_{01}).

(a) STAGE ONE. - After being set by the outputs of B^{00}_{04} and B^{00}_{05}, the Stage one circulation bit (W^{00}_{00}- W^{20}_{00}) continues to circulate until the following timing pulse occurs. At that time, Stage two is set, and Stage one is cleared.

The output of Stage one core W^{20}_{00} sets C^{31}_{00} which subsequently clears Stage four by negating W^{00}_{03}. The output of W^{00}_{00}, on the other hand, initiates the actual test sequence by setting N^{11}_{00} which subsequently sets cores N^{20}_{00}, N^{20}_{01}, N^{20}_{03}, and N^{31}_{01}. The output of W^{00}_{00} is also utilized in the Memory Card test section as will be explained in a subsequent paragraph.

(b) STAGES TWO, THREE, AND FOUR. - Stages two, three, and four of the Scanner function in an identical manner to the stage previously explained. In general, each Scanner stage is set on the timing pulse immediately following the setting of the previous stage. Each stage is sequentially set and cleared in this manner until the Run/Stop switch is placed in the STOP position or until a fault occurs. In the case of a Stop, each stage is cleared by the negation of its respective W^{00}_{0x} core. Te occurrence of a fault causes B^{00}_{04} to be negated which prevents the next Scanner stage from being set on the following timing pulse. As a result, the Scanner stage that was in operation at the time the fault occurred continues to circulate.

(c) SCANNER OUTPUT CORES. - By referring to Diagram 186820 it can be seen that the output of each Scanner stage (W^{00}_{0x}) sets a corresponding N^{11}_{0x} core. This group of cores composed of N^{11}_{00}, N^{11}_{01}, N^{11}_{02}, N^{11}_{03}, serves as inter-

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An x-designation in the super or sub script of an equation term denotes a number that varies from a group of cores only by the number omited.

mediate cores between the Scanner stages and the test card input cores. In this capacity, these cores serve as additional outputs for the Scanner stages. This is necessary due to the limitation of the number of outputs of a magnetic switch card.

(d) TEST CARD INPUT CORES. - Generally, the Test Card Input cores, consisting of the N^{20}_{0x} and N^{30}_{0x} cores, produce the Set or Clear pulses for the magnetic switch card under test via the Magnetic Switch Card selector (S-7). Thus, the selection of a particular card type on S-7 causes the Test Card Input cores to distribute the Set and Clear pulses to the proper inputs of the test card.

By referring to Diagram 186820 it can be seen that the Test Card Input cores are set by the outputs of the corresponding Scanner Output cores. Thus, the setting of a particular Scanner stage subsequently causes the setting of a certain set of Test Card Input cores. The outputs of a set of these cores are then distributed to the proper position of S-7 where depending upon the card type selected and the Scanner stage currently functioning one of the output pulses is used to set or clear the test card. For example, the setting of Scanner stage one subsequently causes the setting of N^{20}_{00}, N^{20}_{01}, and N^{20}_{03}. The output of N^{20}_{00} is distributed to positions 1, 2, 3, 4 in sections AA, BA, CA, and DA respectively of S-7, while the output of N^{20}_{01} is distributed to positions 5, 6, and 7 in BA, CA, and DA respectively. The output of N^{20}_{03} is distributed in a similar manner.

The Test Card Input cores are divided into two distinct groups according to the times at which they produce their respective output pulses. These groups are the N^{20}_{0x} and N^{30}_{0x} cores. By noting the time digits of the two terms it is obvious that these two groups are read out on two successive time periods. The outputs of the N^{20}_{0x} cores are used exclusively for Set inputs to the test card (at time n-2) while the outputs of the N^{30}_{0x} cores are used for Set inputs at

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time n-1 or for Negation inputs at time n-1, depending upon card type selection. The N^{30}_{0x} group of cores can be further divided into two additional groups. The first group consisting of cores N^{30}_{00}, N^{30}_{01}, and N^{30}_{02} produces only Set inputs at time n-1 while the second group (N^{30}_{03}, N^{30}_{04}, and N^{30}_{05}) produces only Clear inputs at time n-1. By referring to the previously mentioned diagram, it can be seen that the inputs to cores N^{30}_{03}, N^{30}_{04}, and N^{30}_{05} are grounded on certain positions of Section EA of S-7. This is done in order to prevent the setting of these cores during the testing of certain card types. For example, the selection of card types 1017, 1026, 2016, 2025, or 3015 grounds the input to N^{30}_{03}. The reason for this is apparent since these cards have just one or two Clear inputs, thus eliminating the necessity for a third Clear input. Table 3-1 lists each of the Test Card Input cores and their output distribution.

The outputs of the N^{20}_{0x} and N^{30}_{0x} cores are conditioned by the outputs of N^{21}_{00} and N^{31}_{00}, respectively. These two cores are set as part of the normal timing chain following a timing pulse. During the period between successive timing pulses, these cores are also set by outputs of the Fault Check circuit. At the time the output of the test card is checked for a fault condition, N^{21}_{00} and N^{31}_{00} are re-set by N^{10}_{03} or by the ANDing of 0^{10}_{00} and N^{10}_{04} in order to produce successive input pulses to the test card between timing pulses. As a result, each test card receives eight Set or Set and Clear pulses for each 32 microsecond period that the Scanner is in operation.

(4) OUTPUT FAULT CIRCUIT. - The Output Fault circuit (see Diagram 186820, Volume 11, page 21) checks the output of the test card for the three basic types of magnetic switch card faults which are as follows:

1) Zero Fault - open output diode or possibly an open clamp diode

2) Card Fault - failure of a card to set

3) Clear Fault - failure of a card to clear or negate

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Table 3-1. Test Card Input Distribution

CORE	SET BY	SET INPUT TO	CLEAR INPUT TO
N^{20}_{00}	Stages 1, 2, 3, and 4	1002, 1004, and 1008 (pin 9) 1017 (pin 8) 1026 (pin 7) 1035 (pin 6)	None None
N^{20}_{01}	Stages 1 and 3	1102 and 1107 (pin 8) 2016 (pin 7) 2025 (pin 6)	None None
N^{20}_{02}	Stages 2 and 4	2016 (pin 8) 2103 (pin 8) 2106 (pin 8) 2025 (pin 7)	None None
N^{20}_{03}	Stage 1	2103 (pin 7) 2106 (pin 7) 2205 (pin 6) 3015 (pin 6) 3105 (pin 6)	None None
N^{20}_{04}	Stage 2	2205 (pin 7) 3015 (pin 7) 3105 (pin 7)	None None
N^{20}_{05}	Stage 3	3015 (pin 8) 3105 (pin 8)	None None
N^{30}_{00}	Stage 2 and 4	1102 (pin 9) 1107 (pin 9) (Time n-1)	None None
N^{30}_{01}	Stage 3	2103 (pin 9) 2106 (pin 9) 2205 (pin 8) (Time n-1)	None None
N^{30}_{02}	Stage 4	2205 (pin 9) 3105 (pin 9) (Time n-1)	None None
N^{30}_{03}	Stage 2	None	1035 (pin 7) (Time n-1)
N^{30}_{04}	Stage 3	None	1026 (pin 8) 1035 (pin 8) 2025 (pin 8) (time n-1)

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Table 3-1. Test Card Input Distribution (con t)

N^{30}_{05}	Stage 4	None	1017 (pin 9) 1026 (pin 9) 1035 (pin 9) 2016 (pin 9) 2025 (pin 9) 3015 (pin 9)
		None	(time n-1)

If, in the process of testing a magnetic switch card, one or more of the above mentioned faults occurs, an indication of the type of fault is given on the Test Control panel, and in the case of either a Card or Clear fault, the test sequence is stopped.

(a) ZERO FAULT. - A Zero fault occurs when one of the Output circulation bits is set at a time when a "1" should not be read from the test card. This may be caused by an open output diode or possibly by a bad clamping diode. By referring to the above mentioned diagram, it can be seen that each of the outputs of the test card (via the test jack) passes through a section of the Output Selector switch (S-5). This feature grounds the outputs of the test card which are not used, thus preventing the corresponding Output circulation bits from being set. For example, if a 1017 card is to be tested the Output Selector switch is set on 7 (the number of outputs of the card). As a result, only the input to the Output 8 circulation bit is grounded through Section H of S-5, thus preventing that circulation bit from being set at any time.

If one or more of the output diodes in the test card are open, the corresponding Output circulation bit or bits will be set. As a result, either N^{15}_{01} or N^{15}_{02} will be set, which will result in the subsequent setting of the Zero Fault core, N^{35}_{00}. The setting of this core causes the Zero Fault indicator on the Test Control panel to be illuminated. This indicator continues to be illuminated until the faulty card is removed from the test jack or a Run condition is initiated. However, the setting of the Zero Fault bit does not stop the operation of the Scanner but merely indicates that a fault has occurred.

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In the reading out of a "1" from the test core, the O^{10}_{OX} cores in the Output circulation bits are normally set. In these instances, however, the Output circulation bits should not be set, for if they were, a Zero fault would result each time the test card was read out. For this reason, normal circulation control core N^{05}_{OO} is negated by the output of N^{31}_{O1} one time period before the test core is read out. Thus, core N^{15}_{OO} is not set and as a result, the AND inputs to each of the O^{30}_{OX} cores in the Output circulation bits are disabled momentarily, thereby preventing the Output circulation bits from being set. When a "1" is not to be read from the test core, N^{05}_{OO} is unconditionaly set at time 2 and is not negated by N^{31}_{O1}.

(b) CARD FAULT. - A Card Fault occurs when the test card is set by the output of the Scanner circuit, but a "1" is not subsequently read from the card. If this condition occurs, O^{10}_{OO} is not set when the test card is read out, and subsequently N^{32}_{OO} is not negated. The output of N^{32}_{OO} then sets the Card Fault circulation bit (W^{12}_{OO}- W^{32}_{OO}). An indication of a Card fault is given on the Test Control panel and B^{30}_{O5} is set which results in the negating of B^{00}_{O4}, thus preventing the setting of the next Scanner stage. (see Diagram 186820, Volume 11, page 20). The Scanner stage which was set at the time the fault occurred continues to circulate and produce output pulses to the test card until the tester is stopped. This allows the operator to determine in what part of the test sequence the fault occurred.

(c) CLEAR FAULT. - A Clear fault is caused by the failure of a test card to negate on the proper cycle of the Scanner. This fault is detected when a "1" is read from a test card which was supposed to have been negated. As a result, the output of O^{10}_{OO} ANDs with the output of N^{10}_{O3} to set N^{32}_{O1} in the Fault Check circuit. The output of N^{32}_{O1} sets the Clear Fault circulation bit (W^{12}_{O1}- W^{32}_{O1}) which illuminates the Clear Fault indicator and sets B^{30}_{O5}.

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c. M-L TEST. - Since, in actual use, the M-L card functions in conjunction

with a magnetic switch card, the M-L test card also receives its input from a magnetic switch card which is plugged into the magnetic switch jack (TJ-A2).

In order to test an M-L card, the test card must first be plugged into TJ-B2 (see Diagram 186824) and a magnetic switch card into TJ-A2. Any type of magnetic switch card that has a continuous "1" output (no Clear input) may be used.

Since both the magnetic switch card and the M-L card will be tested simultaneously, there is no need to employ a pre-tested magnetic switch card.

Both functions of the M-L card are tested in the M-L test section, i.e. the manual set and indicator input functions. As a result, the M-L test sequence is divided into these two basic catagories.

(1) MANUAL INPUT TEST. - The manual input portion of the M-L test card is checked by the routing of the Run switch output through this portion of the M-L test card. This is accomplished by placing the Normal/M L switch (S-8) in the M L position and the Normal-4009-4010-4011-4012 (S-9) switch in the NORMAL position. Thus, when the Run/Stop switch is placed in the RUN position, the +8 vdc output of S-9 is applied to pin 2 of the M-L test card. The Manual set output (pin 8) of the test card is routed through Section BA of S-6 to the Run circulation bit (G^{00}_{02}- G^{20}_{02}) via the M L position of S-8. This is a conclusive test of the manual set portion of the M-L test card since the Run circulation bit must be setin order to initiate the M-L test sequence If the Run circulation bit fails to set, diode CR07 of the M-L test card is open (see Diagram 86870, Volume 10, page 16).

(2) INDICATOR INPUT TEST. - Following the setting of the Run circulation bit by the manual set portion of the M-L test card, the magnetic switch test section functions in an identical manner to its operation during the testing of a magnetic switch card. However, an additional output is taken from the

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magnetic switch card (through 0^{10}_{00}) and applied to the Set input of the M-L test card (pin 9) via Section BB of S-6. The resulting output of the M-L test card (pin 1) is routed through Section AA of S-6 to the control grid of the M-L cathode follower on the 70300 chassis (see Diagram 186826). The output of the M-L cathode follower is applied to the M-L Test Card Output meter (see Diagram 186824) through the M L position of S-8. Although it is an ammeter, the M-L Test Card Output meter does not measure the output current of the M-L test card. It merely reflects the voltage output of the M-L card. The face of the meter contains green shaded areas denoting readings at which the M-L card is functioning properly. However, a more conclusive test is gained if the test point on the card is monitored with a vacuum tube voltmeter or an oscilloscope. In monitoring the output of the M-L card, care should be taken to prevent loading of the card output. It is best to use a vacuum tube voltmeter for minimum loading although an oscilloscope will give relative voltage readings.

As previously mentioned, a GREEN reading on the meter indicates an optimum voltage output of the M-L card. For a "0" output of the card (magnetic test section in the STOP condition), the voltage output should be in the range between +30 and +47 volts. For a "1" output of the card (magnetic test section in the RUN condition), the voltage output should be in the range between +80 and +110 volts.

d. TRANSISTOR INPUT (4011) TEST. - As in the M-L test the Transistor Input (4011) card is also tested in conjunction with a magnetic switch card. The 4011 test card is plugged into TJ- B2 where it receives its input on pin 8 from the type 81154 transistor switch (on the 70300 chassis) via the Transistor Switch Input selector (see Diagram 186823) and Section BAof S-6 (see Diagram 186824). The input to the 4011 card consists of a series of 9kc pulses which vary between ground and -3 vdc. As a result, the outputs of the 4011 card alternate from high impedance to ground, respectively.

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The outputs of the 4011 test card (pins 1 and 2 of TJ-B2) are applied to positions 1 and 2 of the Magnetic Switch Output selector (S-5) via Sections AA and AB of S-6. Depending upon the position of S-5 (1 or 2), each output is separately applied to the input of the magnetic switch card in TJ-A2 via Section DA of S-6. As a result, the outputs of the 4011 test card serve as Set inputs to the magnetic switch by alternately grounding its input and placing its input at a high impedance. The operation of the 4011 test card is checked by monitoring the output of the magnetic switch with an oscilloscope.

e. LINE DRIVER (4012) TEST. - The line driver (4012) test card receives its input from magnetic switch N_{oo}^{11} (see Diagram 186820, page 20) via Section BB of S-6 (see Diagram 186824). Thus, the input (pin 9) of the 4012 card receives a series of eight pulses from N_{oo}^{11} whenever Stage one of the Scanner circuit is set. The operation of the line driver is checked by the monitoring of its output (pin 1) with an oscilloscope. The function of the 4012 card is such that when it receives a series of input pulses from N_{oo}^{11} its output should be at a ground level and when the pulses are removed the output should be at -14 vdc.

3-4. RESYNC DELAY (4009 and 4010) TEST SECTION. - The 4009 and 4010 test cards are tested conjunctively as one portion of a standard resync delay circuit. A logic diagram of the 4009 and 4010 test section is shown on the upper left hand corner of Diagram 186824.

In order to test the 4009 and 4010 cards, S-6 is set to position 4009 or 4010, and the two cards are plugged into their respective test jacks. The setting of S-6 to either of these positions interconnects the two test cards in the proper manner. The cards which comprise the other section of the standard high-speed resync delay circuit are located on chassis 70300.

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For a detailed discussion of the 4011 or 4012 circuit refer to "Instruction Book for CXPK Computer" , Volume 4, Section 6.

In general, the 4009 and 4010 cards are tested by comparing the outputs of the resync delay test circuit with those of a standard re-sync delay circuit which is also contained on the 70300 chassis. The test of the 4009 and 4010 cards is divided into two basic divisions as follows: the single pulse test and the multiple pulse test.

a. SINGLE PULSE TEST. - The general function of the Resync Delay circuit is to produce a single Set pulse to a magnetic switch from an external input pulse. As a result, a certain portion of the Resync Delay Test section is devoted to checking the output of the resync delay test circuit to determine if it is producing a single output pulse for each input pulse variation from a transistor switch card. The input to the transistor switch card is furnished by a free-running multivibrator circuit (9 kc). Thus, the input to the standard resync delay circuit is in phase with the input to the test resync delay circuit. However, the outputs of these two circuits are wired so as to be 180° out of phase with each other.

A positive output of Y^{80}_{03} in the standard resync delay circuit will set circulation bit D^{00}_{01}- D^{20}_{01}. However, the output of Y^{80}_{02} is negative at this time which fails to meet the AND input to E^{10}_{00} until the following cycle when the outputs of Y^{80}_{02} and Y^{80}_{03} reverse polarity. At this time E^{10}_{00} is set and D^{20}_{01} is negated. The output of E^{10}_{00} sets circulation bit D^{10}_{01}- D^{30}_{01}. Simultaneously, the output of Y^{80}_{01} in the test resync delay circuit sets D^{10}_{00}. Cores D^{10}_{00} and D^{30}_{00} function as a circulation bit.

On the following cycle, E^{00}_{00} is set by AND inputs Y^{80}_{00} and D^{30}_{00} (the outputs of Y^{80}_{00} and Y^{80}_{01} reverse). At the same time circulation bit D^{00}_{01}- D^{20}_{01} is

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For a complete description of the resync delay circuit, refer to the "Instruction Book for the CXPK Computer", Volume 4, Section 6.

again set. The output of E^{00}_{00} negates circulation bit D^{10}_{01}- D^{30}_{01} which prevents a resync delay fault from occurring on the following cycle. Thus, if the test resync delay circuit had failed to produce an output pulse for each input cycle D^{10}_{01}- D^{30}_{01} would not have been negated, and as a result E^{20}_{00} would have been set, which would have set the Card Fault circulation bit (see Diagram 186820, page 21).

b. MULTIPLE PULSE TEST. - The multiple pulse phase of the test is a check to determine whether the test resync delay circuit produces more than one output pulse for each input cycle.

The output of E^{00}_{00} sets circulation bit D^{00}_{00}- D^{20}_{00}. Thus, if the test resync delay circuit produces another output pulse before the standard resync delay circuit, D^{00}_{00}- D^{20}_{00} is not negated by the output of E^{10}_{00} and as a result, E^{20}_{00} is set by AND inputs $E^{00}_{00}D^{00}_{00}$. As a result, a Card Fault will occur.

3-5. MEMORY CARD TEST SECTION

a. GENERAL. - All of the memory test cards, including types 9118, 9122, 9218, 9411, 9522, 9622, and 9811, are tested conjunctively in the Memory Card Test section. In order to test a particular memory card type, the test card is inserted in the proper test jack and the remainder of the memory card test jacks are filled with pre-tested cards of the proper type. In addition, a magnetic switch card must be inserted in the magnetic switch test jack, and the magnetic switch test selection switches must be set for the type of magnetic switch card inserted. Because of the conjunctive manner in which the memory cards are tested, the operation of the Memory Card Test section is discussed on the basis of its overall operation rather than for each individual card test.

The magnetic core memory used in conjunction with the Memory Card Test section employs two magnetic cores which are suspended on their proper control

wires and mounted on a terminal board contained on the 70300 chassis (see Diagram 186826). These two cores compose a one-bit, two word memory system which is used exclusively with the Memory Card Test section.

In general, the memory card test is divided into four phases. In the first phase, one of the memory cores is selected by the Word Selection circuit and a "1"is written in the core. No fault check is made after the completion of this phase. During the second phase, the "1" is read from the core, and a "1" Fault Check is made. The third phase consists of writing a "0" in the same core while in the fourth phase of the test, the "0" is read out of the core and a "0" fault test is made. After the completion of the four phases above, the second memory core is selected and the same four phases are repeated for that core.

If a Memory Fault occurs while the Memory Error switch is in the STOP position, the Scanner circuit is stopped on the Scanner stage where the fault occurred. However, if the Memory Error switch is in the RUN position, the Scanner continues to operate although a visual indication of the Memory Fault is given on the Test Control panel.

The basic timing sequence of the Memory Card Test section is controlled by the timing pulse and the Scanner circuit. As a result, one phase of the Memory Card Test sequence is completed during the operation of a particular Scanner stage with a complete cycle of four phases being completed in 128 microseconds.

b. SELECTIONS. - In order to test a particular memory card, the test card is inserted in its proper test jack. The remainder of the memory test jacks are then filled with the proper cards which have been previously tested to insure that they are functioning properly. In addition, one type of magnetic switch card is inserted in its test jack, and the proper switch settings are made for this type. It is then decided whether the Scanner is to stop when a

Memory Fault occurs. The Memory Error switch is then placed in the corresponding position.

The setting of S-12 (Off-Section one-Section two switch) is optional, depending on which section of the 9622 or 9122 card is to be tested but in either case this switch must not be in the OFF position, or the Memory Test Section will not function. The position of the Memory Card Output selector is also optional depending upon which of the eight outputs of the 9118 and 9218 test cards is to be tested.

NOTE

IF THE MEMORY CARD OUTPUT OR 9622-9122 TEST SELECTORS
ARE ACTUATED WHILE THE TEST IS IN PROGRESS,
A FAULT WILL OCCUR.

c. WORD SELECTION CIRCUIT. - The Word Selection circuit (see Diagram 186822) controls the selection of the two memory cores. After the selection of one of these cores has been made, the selection is maintained for a period of 128 microseconds (one complete test sequence). The Word Selection circuit then enables the other core for the same period. Thus, the Word Selection circuit alternately selects the two memory cores for periods of 128 microseconds.

The test is initiated when the timing pulse is produced (B^{00}_{04} set), Stage 1 of the Scanner is set (B^{00}_{05} set), and the Word Selection circulation bit (S^{00}_{01}- S^{20}_{01}) is set. As a result, S^{00}_{02} (unconditionally set at time 2) is negated at time 3 of each clock cycle for a period of 128 microseconds.
The output of S^{00}_{01} partially enables the AND input to the pulse stretcher Y^{20}_{01} for a 128 microsecond period. (The other AND input is enabled as part of the test timing sequence.) When its AND input is completed, the output of Y^{20}_{01} partially enables Read/Write generators Y^{50}_{01} and Y^{50}_{11} respectively. The outputs of this pair of Read/Write generators drive the first memory core which may be considered to be at address 00.

At the end of the first 128 microsecond period, S^{10}_{00} is set by AND input

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B^{00}_{04} B^{00}_{05} S^{00}_{01}. As a result, the Word Selection circulation bit is negated, and S^{00}_{02} is set at time 2 of each clock cycle. Depending upon the position of S-11, one section of the 9122 test card (Y^{20}_{00}) receives its input from S^{00}_{02} during the next 128 microseconds which causes Read/Write generator combination $Y^{50}_{00}$and Y^{50}_{10} to be selected during this period. This Read/Write generator combination then drives the second memory core which may be considered to be at a hypothetical address of 01. It should be noted here that the 9122 card test takes place during the time that this core is selected.

d. TIMING SEQUENCE. - The timing sequence of all phases of the Memory Card Test is controlled by timing chain cores (R cores). By referring to Diagram 186822, it can be seen that the R cores are distributed on the diagram according to the times at which they are affected.

The timing sequence of a particular phase begins on a timing pulse (once every 32 microseconds). At this time, B^{20}_{05} is set by the output of B^{00}_{04} (see Diagram 186820, page 20). The output of B^{20}_{05} ANDs with the output of one of the Scanner stages (W^{20}_{00}, W^{20}_{01}, W^{20}_{02}, or W^{20}_{03}) to set B^{01}_{06} which initiates the memory cycle by setting R^{20}_{00}, and clears the Memory circulation bit (Z^{10}_{00}- Z^{30}_{00}). As a result of setting R^{20}_{00}, the Translator Control circulation bit (R^{21}_{00}- R^{01}_{00}) and the Start Read core (R^{00}_{02}) are set. The output of the Translator Control circulation bit completes the AND input to the selected pulse stretcher (Y^{20}_{01} or Y^{20}_{00}), which enables the Read/Write current generators for the memory core.

(1) READ SEQUENCE. - The Read Sequence is initiated at the time R^{00}_{02} is set. The output of R^{00}_{02} enables Read generator Y^{50}_{01} or Y^{50}_{00} to read out the selected memory core through current diverter Y^{55}_{00}. It is noted that one section of the 9522 test card is tested at this point, along with one of the outputs of the 9118 test card.

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The output of R^{00}_{02} also sets the Read Strobe core R^{20}_{04}, which in turn sets R^{30}_{05} and R^{00}_{06}. As a result, N^{14}_{00} is set, but on phases one and three of the test it is immediately negated by the output of the first or third stage of the Scanner (W^{00}_{00} or W^{00}_{02}). The negation of this core on phases one and three of the test disables the output of the selected memory core. This is done because it is not necessary to check the contents of the memory core during these phases of the test. On phases two and four, however, N^{14}_{00} is not negated. As a result, its output ANDs with the output of the sense amplifier (Y^{52}_{00}) test card to set the Memory bit or leave it in the "0" state, depending upon whether a "1" or "0" is read from the selected memory core.

The Read Sequence terminates when the Stop Read core (R^{30}_{09}) discharges pulse stretcher Y^{21}_{02}.

(2) INHIBIT SEQUENCE. - An Inhibit pulse is not produced during phases one and two of the test since a "1" is to be written or restored in the selected memory core during these phases.

During phase one of the test, the output of the Start Inhibit core (R^{20}_{08}) ANDs with N^{24}_{01} (set when stage one of the Scanner is set) to set the Memory circulation bit (Z^{10}_{00}- Z^{30}_{00}). The setting of this bit causes a "1" to be stored in this bit regardless of what was read from the memory core. The output of the Memory circulation bit negates R^{00}_{10} which prevents the Inhibit pulse from being produced. During phase two of the test, the Inhibit sequence is nearly identical to phase one except that the Memory bit is not set by the AND input N^{24}_{01} R^{20}_{08} but is set by the output of the selected memory core. The output of Z^{30}_{00} subsequently negates R^{00}_{10} as it did during phase one.

During phases three and four of the test, R^{00}_{10} is not negated, since the Memory bit contains a "0". As a result, Inhibit generator Y^{51}_{00} produces the Inhibit pulse through the selected section of the 9622 inhibit transformer test

card. The Inhibit pulse terminates when R^{20}_{20} discharges Y^{30}_{00} through the 9218 pulse discharger test card Y^{22}_{00}.

(3) WRITE SEQUENCE. - The Write Sequence is initiated when the Start Write core (R^{10}_{11}) is set. The output of R^{10}_{11} enables Write generator Y^{50}_{11} or Y^{50}_{10} to write a "1" or "0" in the selected memory core. The output of R^{10}_{11} also sets the Stop Translator control core, R^{10}_{15}, via intermediate timing core R^{30}_{13}. The Stop Translator Control core subsequently negates the Translator Control circulation bit which disables the inputs to Y^{21}_{00}, Y^{20}_{01} and Y^{20}_{00}. The Stop Write core, R^{30}_{17}, is also set at this time. The output of R^{30}_{17} terminates the Write operation by discharging pulse stretcher Y^{11}_{00} through pulse discharger Y^{32}_{01}.

(4) DISTURB. - The Disturb pulse is produced by the output of R^{00}_{18} through pulse stretcher Y^{02}_{00}, thus causing Inhibit/Disturb generator Y^{51}_{00} to transmit the Disturb pulse through the Inhibit transformer (9622) test card. The section of the 9622 test card through which the Disturb pulse is transmitted depends upon the position of the 9622-9122 Test selector (S-11). It is to be noted here that the 9411 and 9622 cards are not tested exclusively during this phase of the test sequence, but are tested on each phase.

The output of R^{00}_{18} causes pulse stretchers Y^{21}_{00}, Y^{20}_{01}, and Y^{20}_{00} to be discharged through pulse discharger Y^{02}_{00}. The output of R^{20}_{20} causes pulse stretcher Y^{30}_{00} to be discharged through the 9218 pulse discharger test card, thus ending the Disturb pulse.

e. FAULT CHECK CIRCUIT. - The Fault Check circuit samples the output of the Memory circulation bit to determine whether a "0" or a "1" was read from the selected memory core. Depending upon the phase of the test, the Memory Fault circulation bit (W^{03}_{00}- W^{23}_{00}) is set if the correct bit was not read from the memory core. The Fault Check circuit is divided into two types of checks which are the "1" and "0" checks. The "1" check occurs on phase two while the "0"

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check is made on phase four. No fault check is made on phases one or three.

(1) "1" CHECK. - As previously mentioned, the "1" check is made on phase two of the memory card test. The check is initiated by the setting of the Memory Fault circulation bit by the output of R^{00}_{18} and W^{00}_{01} (Scanner stage two). On the following time 2, the "1" Check bit, N^{34}_{01}, is set by the outputs of R^{20}_{20} and W^{20}_{01}. At time 3, the output of N^{34}_{01} ANDs with the output of the Memory circulation bit (Z^{30}_{00}) to negate the Memory Fault bit if a "1" was read from the memory core, which is the normal or no-fault condition. However, if a "1" was not read from the memory core the AND input to W^{03}_{00} is not completed, and the Memory Fault circulation bit is not negated. As a result, the Memory Fault circulation bit continues to circulate, and depending upon the position of the Memory Error switch (S-09), B^{30}_{05} either is set by the output of W^{23}_{00} or has its input grounded. If S-09 is in the STOP position, B^{30}_{05} will be set, which will cause the Scanner to stop on the stage where the error occurred (Stage 2 or 4). By observing which Scanner stage is set, the operator can determine whether a "1" or"0" fault occurred. If, however, S-09 is in the RUN position, the Scanner will not stop when an error occurs, but a visual indication of the fault will be given on the Test Control panel.

It is interesting to note at this point that the setting of W^{23}_{00} by the output of R^{00}_{18} at the beginning of the test causes B^{30}_{05} to be set (if S-09) is in the STOP position) although the output of the Memory bit has not been sampled. However, this occurs approximately eight microseconds before B^{00}_{04} is set by the timing pulse, and does not affect the operation of the Scanner unless the Memory Fault bit is not negated on the following clock cycle.

(2) "0" CHECK. - The "0" check occurs on phase four of the memory test and functions in much the same manner as the "1" check. The check is initiated

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when the Memory Fault circulation bit is set by the outputs of R^{00}_{18} and W^{00}_{03} (Stage four). On time 2 the output of R^{20}_{20} ANDs with the output of W^{20}_{03} (Stage four) to set the "0" check bit, N^{04}_{00}. If a "0" is present in the Memory circulation bit, N^{04}_{00} is not negated, and as a result, the Memory Fault bit is negated by the output of N^{14}_{01}. If a "1" was read from the memory core (fault condition), the output of Z^{30}_{00} negates N^{04}_{00}; thus the Memory Fault bit is not negated. The function of the Memory Fault bit during a"0"fault condition is identical to its function for a "1" fault condition.

3-6. TRANSISTOR SWITCH TEST SECTION

a. GENERAL. - This section consists mainly of a switch for transferring a standard transistor switch output into the proper inputs of the transistor switch test card. The input to the test cards is supplied by a free-running multivibrator (9kc) through type 81154 and 81001 transistor switches contained on the 70300 chassis. The outputs of the test card are subsequently checked by oscilloscope monitoring.

b. SWITCH SELECTIONS. - Prior to the testing of the transistor switch card, the Transistor Switch Test selection switches (see Diagram 186823, Volume 11, page 23) must be set to the proper position. (See "Test Procedures" for detailed switch settings for each card type. These switch selections are as follows:

1) Set the Transistor Switch Input selector (S-3) to the number of inputs on the test card.

2) Set the Transistor Switch Card selector (S-4) to the type of card to be tested.

3) Set the Transistor Switch Output selector (S-1) to the number of outputs on the test card.

4) Set the Transistor Switch Output Load selector (S-2) to NORMAL unless a type 81001 or 85002 card is to be tested.

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After the above selections have been made the test card may be inserted in the Transistor Switch Test jack (TJ-A1).

CAUTION

DO NOT INSERT THE TEST CARD INTO THE TEST JACK UNTIL THE PROPER SWITCH SELECTIONS HAVE BEEN MADE. DAMAGE TO THE TEST CARD MAY RESULT IF THE CARD IS TESTED WITH IMPROPER SWITCH SELECTIONS.

c. OUTPUT MONITORING. - By referring to Diagram 186823, it can be seen that the outputs of the transistor switch test card are not checked automatically by the test section. The output of the card can be checked only by monitoring the test jack or the test point on the card with an oscilloscope. For the proper output waveforms, refer to "Test Procedures".

3-7. TYPE 6146 TUBE, 110A1 TRANSFORMER, AND 4007 CARD TEST SECTION

a. GENERAL. - The basic function of this section is to test the operation of the type 6146 driver tube, which is used in the Bogart computer to produce the transfer pulses. However, this section also checks the operation of the type 110A1 pulse transformer and the 4007 Transfer card.

b. TEST OPERATION. - In order to test one of the three units above, all three of these units must be inserted in the proper test jack or socket. For example, if the type 6146 tube is to be tested, the 6146 tube and the type 110A1 transformer are both inserted in their proper receptacles on the Test Control panel. In addition, the type 4007 card must be plugged in TJ-B6. The subsequent depression of the 6146 Test switch (S-09) energizes K02 on chassis 70500 (see Diagram 186830, Volume 11, page 30) which applies +200 vdc to pin 15 of the 4007 test card and +450 vdc to pin 7 of the 110A1 transformer.

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WARNING

DURING THE TIME THAT THE 6146 TEST SWITCH IS DEPRESSED, +450 VDC IS PRESENT ON THE TOP CAP OF THE 110A1 TRANSFORMER.

The ANDing of rp0 and rp1 (from the Clock chassis) in the 4007 test card causes the grid of the 6146 tube to be at ground or slightly positive . As a result, the 6146 tube conducts, thus producing the Transfer pulse at the secondary of the 110A1 transformer and also at test jack (TJ10) where it can be monitored with an oscilloscope. (For waveforms of the Standard Transfer pulses, refer to "The Bogart Instruction Book, Navy Model CXPK," Volume 4, Section 6.)

From the above discussion it is evident that the 6146 test section functions in an identical manner to the equivalent circuit in the Bogart computer. For a detailed discussion of this circuit, refer to "Instruction Book for Bogart Computer, Navy Model CXPK" , Volume 2, Section 4.

3-8. POWER AND COOLING

a. GENERAL. - The card tester unit operates on 115 vac, 60 cps, one-phase power and 200 vac, 400 cps, three-phase power. The 115 vac power is used directly to operate devices such as relays, the blower motor, etc. The 200 vac is supplied by the regulated output of the motor-generator combination furnished with the Bogart computer. This power is distributed to the various transformers and power supplies in the card tester unit.

b. POWER SUPPLY AND DISTRIBUTION. - The main 200 vac input is controlled by relay K02 on relay chassis 70500 (see Diagram 186828, Volume 11, page 28). When the 400-cycle On switch (S-15) is placed in the ON position, K02 is energized, thus applying 400 cps power to chassis 70800 and 70400. Phase one of the power is also applied to the transformer chassis (70300) through the Filament switch (S-17). The 400 cycle input to the standard chassis (70100) is controlled by CB-01 while the 400 cps input to the 70600 and 70700 chassis is controlled by CB-02.

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The grid input to the 6146 tube in the tester is lower than in the Bogart computer due to additional line capacitance.

When the 60 Cycle switch (S-14) is turned on, the blower motor is started.

(1) STANDARD CHASSIS POWER SUPPLY. - The regulated 200 vac input to the standard chassis (see Drawing 87742, Volume 11, page 6) is converted into +450v, +200v, +8v, and 6.3 vac power supplies, as shown in Drawing 87203, Volume 11, page 1. The +450v supply is produced from the 200 vac supply through a step-up, delta-wye transformer and a full-wave rectifier circuit. The +200v supply is produced from the 200 vac supply through a delta-wye transformer and a full-wave rectifier circuit. The +450v and +200v power supplies are used in producing the Read and Transfer Pulse circuits.

The +8v supply is produced from the 200 vac supply through a step-down, delta-star transformer and a full-wave rectifier circuit. This supply is furnished to bus bars which distribute the +8v to the circuit cards. The +8v from Chassis 70100 is also used for the manual switches on the Test Control panel as shown in Drawing 121279, Volume 11, page 12. The 6.3 vac four-ampere supply is produced from the 200 vac source through a step-down, delta-wye filament transformer and is distributed to each of the eight vacuum tubes.

(2) CLOCK CHASSIS POWER SUPPLY. - The clock chassis (70400) uses the same power supplies as the standard chassis described in the preceding section. However, it also uses a 6.3 vac, 10-ampere power supply which is produced from the regulated 200 vac supply through a step-down, delta-delta filament transformer and furnished to bus bars located on the chassis. This circuit is shown in Drawing 87740, Volume 11, page 2.

In addition to the normal outputs of the Clock chassis, +200 and +450 vdc outputs are brought out to the NO contacts of K02 on the 70500 chassis (see Diagram 186828). These outputs are used in the 6146 tube test and associated circuits.

(3) LOW AND HIGH VOLTAGE POWER SUPPLIES. - The regulated 200 vac

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power supply is converted into +150v, +60v, +9v, -14v, -25v, -100v, -125v -165v, 6.3 vac, and various bias voltages as shown in Drawing 121290, Volume 11, pages 3 and 4. These voltages are distributed to each chassis that is associated with memory. The +150v, +60v, -100v, -125v, and -165v supplies are produced from the 200 vac supply through step-down, delta-wye transformers and full-wave rectifier circuits. The Read, Write, and Inhibit bias voltages are taken from the -125v source and controlled by potentiometers R01, R02, and R03 (see Drawing 87742), mounted on the Test Control panel.

The +8v, -14v and -25v supplies are produced from the 200 vac supply through step-down, delta-star transformers and full-wave rectifier circuits. The Sense Amplifier bias voltage is taken from the +8v supply and is controlled by potentiometer R04 mounted on the Test Control panel.

The 6.3 vac supply is produced from the regulated 200 vac supply through a step-down, delta-wye filament transformer. This supply is distributed to bus bars.

In addition to the normal outputs of chassis 70700, +150 vdc is brought out through the NO contacts of K01 on chassis 70500 (see Diagram 186828). This output is used in the test of the converter driver chassis.

(4) CARD VOLTAGE SUPPLIES. - Some electronic circuits in the card tester require voltages other than those produced by transformer-rectifier circuits. These circuits have low power and stability requirements, so that voltages obtained from resistors used as voltage dividers are sufficient.

Stability to high-frequency load variation is provided by a small condenser in parallel with the load. All voltage divider type supplies are located on the printed-circuit cards which they serve.

Each standard magnetic switch card has a voltage divider which produces +2 volts from the +8 volt supply. The +2 volt power is also produced on the

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Manual Set and Indicator Light (M-L) cards.

All transistor switch cards, and resynchronization delay cards 4009 and 4010 hold dividers which produce -3 volts from the -15 volt supply.

Type 4012 line drivers, and 9118 and 9122 pulse stretchers contain divider-type supplies which produce +5 volts from the +8 volt supply.

(5) -80 VDC POWER SUPPLY. - The -80 vdc power supply (70800) supplies power to the converter driver test chassis through the NO contacts of K01 on chassis 70500 (see Diagram 186828. Volume 11, page 28).

The -80 vdc power supply consists of a delta-star transformer with a full-wave rectifier output (see Diagram 186819, Volume 11, page 27). The -80 vdc output is protected by a two-ampere indicating fuse (F04).

c. COOLING. - The card tester is cooled by a 1/8 hp centrifugal blower. The blower is mounted in the rear of the cabinet, thus blowing the cool air over the major portion of the chassis.

SECTION 4

CARD TESTER EQUATIONS

4-1. TERMS USED IN THE CARD TESTER EQUATIONS

As in the Bogart instruction book, alpha-numeric terms are used in the card tester diagrams, text, and logical equations to identify the magnetic switches. Each magnetic switch symbol is identified by a unique term with all of the terms concerning a certain circuit or general section having the same alphabetical designation. The first digit of the numerical superscript denotes the time at which that particular core is read out while the remainder of the digits make each core unique. For a complete discussion of the logical equations (Boolean Algebra), see "The Instruction Book for the Bogart Computer, Navy Model CXPK", Volume 2, Section 4.

Each of the alphabetical term designations is listed below with the corresponding circuit or general section.

B	Main timing control cores
C	Intermediate timing control cores
D	Circulation bit cores in the resync delay test section
E	Control cores in the resync delay test section
G	Run/Normal/Stop circulation bit cores
I	Indicator designations (M-L cards)
N	Miscellaneous control cores
O	Output circulation bit cores
R	Memory Test section timing cores
S	Memory word selection cores
W	Fault circulation and control cores

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Y	Non-magnetic switch cards*
Z	Memory circulation bit cores

4-2. LOGIC AND CARD PLACEMENT

The two charts that follow respectively show the logic and card placement for chassis 70100. The logic placement chart shows the co-ordinate locations of the cards on chassis 70100 according to their term disignations. Conversely, the card placement chart shows the co-ordinate location of the cards according to their card type designations.

*The Y terms do not conform to the normal equation terms in that they do not designate a particular read out time. They merely provide a means of including the non-standard circuits as inputs to the normal equation terms.

Table 4-1. Logic Placement (Chassis 70100)

	9	8	7	6	5	4	3	2	1
A									
B					R^{00}_{18}	R^{30}_{13}	R^{20}_{08}	R^{00}_{06}	C^{00}_{00}
C	Y^{50}_{01}	Y^{50}_{11}			Y^{02}_{00}	R^{10}_{15}	R^{00}_{10}	R^{20}_{04}	C^{20}_{00}
D			E^{20}_{00}	Y^{21}_{02}	Y^{32}_{00}	R^{30}_{17}	R^{30}_{09}	R^{00}_{02}	B^{30}_{01}
E	Y^{50}_{00}	Y^{50}_{10}	D^{20}_{00}	Y^{20}_{01}	Y^{1}_{00}	B^{10}_{04}	R^{10}_{11}		C^{10}_{01}
F	D^{10}_{01}	D^{30}_{01}	D^{00}_{00}	L^{-1}_{11}	Y^{32}_{01}	R^{01}_{00}	R^{21}_{00}	R^{30}_{05}	C^{30}_{01}
G	E^{10}_{00}	D^{00}_{01}	Y^{30}_{00}	S^{00}_{01}	R^{20}_{20}	W^{03}_{00}	R^{20}_{00}	N^{14}_{00}	B^{00}_{02}
H	E^{00}_{00}	D^{30}_{00}	D^{20}_{01}	S^{20}_{01}	N^{34}_{01}	W^{23}_{00}	B^{01}_{08}	B^{20}_{05}	C^{20}_{02}
I	N^{05}_{00}	N^{15}_{00}	D^{10}_{00}	S^{10}_{00}	N^{04}_{00}	B^{30}_{05}			C^{00}_{02}
J	Z^{10}_{00}	Z^{30}_{00}	S^{30}_{00}	S^{00}_{02}	N^{14}_{01}	L^{-1}_{12}	N^{24}_{01}		B^{10}_{03}
K	N^{11}_{01}	N^{11}_{00}	L^{-2}_{01}	L^{-2}_{00}	B^{30}_{03}	G^{00}_{02}	G^{00}_{01}	G^{00}_{00}	B^{21}_{03}
L	N^{11}_{03}	N^{11}_{02}	L^{-2}_{03}	L^{-2}_{02}	B^{30}_{04}	G^{20}_{02}	G^{20}_{01}	G^{20}_{00}	B^{20}_{03}
M	N^{31}_{01}	N^{31}_{00}	N^{21}_{00}	B^{00}_{08}	B^{00}_{04}	W^{00}_{03}	W^{00}_{02}	W^{00}_{01}	W^{00}_{00}
N	N^{20}_{03}	N^{20}_{02}	N^{20}_{01}	N^{20}_{00}	N^{10}_{01}	W^{20}_{03}	W^{20}_{02}	W^{20}_{01}	W^{20}_{00}
O	N^{30}_{01}	N^{30}_{00}	N^{20}_{05}	N^{20}_{04}	N^{30}_{06}	C^{31}_{03}	C^{31}_{02}	C^{31}_{01}	C^{31}_{00}
P	N^{30}_{05}	N^{30}_{04}	N^{30}_{03}	N^{30}_{02}	N^{10}_{02}	W^{12}_{00}	W^{12}_{01}	B^{00}_{05}	N^{15}_{02}
Q	O^{10}_{00}	L^{-1}_{00}	L^{-1}_{01}	N^{10}_{03}	N^{22}_{00}	W^{32}_{00}	W^{32}_{01}	O^{30}_{04}	O^{30}_{05}
R	L^{-1}_{04}	L^{-1}_{03}	L^{-1}_{02}	N^{10}_{04}	N^{32}_{00}	L^{-1}_{10}	L^{-1}_{09}	O^{10}_{04}	O^{10}_{05}
S	L^{-1}_{07}	L^{-1}_{06}	L^{-1}_{05}	O^{30}_{01}	N^{32}_{01}	O^{30}_{02}	O^{30}_{03}	O^{30}_{06}	O^{30}_{07}
T	O^{30}_{00}	L^{-2}_{04}	N^{35}_{00}	O^{10}_{01}	N^{15}_{01}	O^{10}_{02}	M^{10}_{03}	O^{10}_{08}	O^{10}_{07}

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Table 4-2. Card Placement (Chassis 70100)

	9	8	7	6	5	4	3	2	1
A	4014	4007	4008	4007	85003	4007	4008	4007	4014
B	-	-	-	-	1008	1002	1004	1002	1017
C	9411	9411	-	9218	9218	1002	1017	1002	1002
D	-	-	1102	9118	9218	1004	1002	1002	1004
E	9411	9411	2016	9122	9118	1002	1002	-	2016
F	1017	1102	1002	ML	9218	1107	1017	1002	1002
G	1004	1002	9122	1004	1004	1026	1002	1026	1004
H	1004	1002	2016	2016	1002	3015	3105	1004	2016
I	1017	1008	2016	1002	1017	2103	-	-	1002
J	1026	2106	1002	1017	1002	ML	1002	-	1004
K	1008	1008	ML	ML	1008	1102	2025	1102	1017
L	1008	1008	ML	ML	1004	1002	1004	1002	1008
M	3105	2106	2106	1002	1017	1026	1026	1026	1026
N	1002	1102	1102	3105	1002	1107	1107	1107	2016
O	1002	1102	1002	1002	1002	1002	1002	1002	1002
P	1002	1002	1002	1002	1002	2016	2016	1107	3105
Q	1107	ML	ML	2106	1102	1102	1002	1002	1002
R	ML	ML	ML	1004	1017	ML	ML	1102	1102
S	ML	ML	ML	1002	1002	1002	1002	1002	1002
T	1002	ML	1102	1102	3105	1102	1102	1102	1102

EQUATIONS FOR CARD TESTER

$B^{30}_{01} = C^{20}_{00}$

J01D1 1004 C^{00}_{00} C^{10}_{01} B^{00}_{02}

$B^{00}_{02} = C^{30}_{01} B^{30}_{01}$

J01G1 1004 C^{20}_{02} B^{10}_{03} C^{10}_{01}

$B^{10}_{03} = B^{00}_{02} C^{00}_{02}$

J01J1 1004 C^{20}_{02} B^{20}_{03} B^{21}_{03}

$B^{20}_{03} = B^{10}_{03}$

J01L1 1008 G^{00}_{00} G^{00}_{01} G^{00}_{02} B^{30}_{03} B^{30}_{04} B^{00}_{04}

$B^{30}_{03} = B^{20}_{03} G^{20}_{00} G^{20}_{01}$

J01K5 1008 G^{00}_{01} B^{00}_{08} W^{00}_{00} W^{00}_{01} W^{00}_{02} W^{00}_{03} W^{03}_{00} B^{10}_{04}

$B^{00}_{04} = (B^{20}_{03}) (B^{30}_{05})^{-1}$

J01M5 1017 W^{20}_{00} W^{20}_{01} W^{20}_{02} W^{20}_{03} B^{20}_{05} S^{20}_{01} S^{10}_{00}

$B^{10}_{04} = B^{30}_{03}$

J01E4 1002 W^{20}_{00}

$B^{30}_{04} = B^{20}_{03} G^{20}_{01} G^{20}_{02}$

J01L5 1004 G^{00}_{01} B^{00}_{05} N^{10}_{01}

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$B^{00}_{05} = B^{30}_{04} + C^{31}_{03}$

J01P2 1107 W^{20}_{00} S^{10}_{00} S^{20}_{01}

$B^{20}_{05} = B^{00}_{04}$

J01H2 1004 B^{01}_{06} B^{01}_{06} B^{01}_{06} B^{01}_{06}

$B^{30}_{05} = W^{12}_{00} + W^{12}_{01} + W^{23}_{00}$

J01I4 2103 B^{00}_{04}

$B^{00}_{06} = B^{30}_{03}$

J01M6 1002 W^{12}_{00} W^{12}_{01} Z^{10}_{00}

$B^{21}_{03} = (\ )\ (B^{10})^{-1}$

J01K1 1017 G^{00}_{00} G^{00}_{02}

$B^{01}_{08} = B^{20}_{05} W^{20}_{00} + B^{20}_{05} W^{20}_{01} + B^{20}_{05} W^{20}_{02} + B^{20}_{05} W^{20}_{03}$

J01H3 3105 R^{20}_{00} Z^{10}_{00}

$C^{00}_{00} = (\ )\ (B^{30}_{01})^{-1}$

J01B1 1017 C^{20}_{00}

$C^{20}_{00} = C^{00}_{00}$

J01C1 1002 B^{30}_{01}

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$C^{10}_{01} = (B^{30}_{01} + C^{30}_{01})\,(B^{00}_{02})^{-1}$

J01E1	2016	C^{30}_{01}	

$C^{30}_{01} = C^{10}_{01}$

J01F1	1002	C^{10}_{01}	B^{00}_{02}

$C^{00}_{02} = C^{20}_{02}$

J01I1	1002	C^{20}_{02}	B^{10}_{03}

$C^{20}_{02} = (B^{00}_{02} + C^{00}_{02})\,(B^{10}_{03})^{-1}$

J01H1	2016	C^{00}_{02}	

$C^{31}_{00} = W^{20}_{00}$

J0101	1002	W^{00}_{03}	

$C^{31}_{01} = W^{20}_{01}$

J0102	1002	W^{00}_{00}	

$C^{31}_{02} = W^{20}_{02}$

J0103	1002	W^{00}_{01}	

$C^{31}_{03} = W^{20}_{03}$

J0104	1002	W^{00}_{02}	B^{00}_{05}

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$$D^{00}_{00} = D^{20}_{00}$$

J01F7 1002 D^{20}_{00} E^{20}_{00}

$$D^{10}_{00} = (Y^{80}_{01} + D^{30}_{00})(E^{00}_{00})^{-1}$$

J01I7 2016 D^{30}_{00} D^{30}_{01}

$$D^{20}_{00} = (D^{00}_{00} + E^{00}_{00})(E^{10}_{00})^{-1}$$

J01E7 2016 D^{00}_{00}

$$D^{30}_{00} = D^{10}_{00}$$

J01H8 1002 D^{10}_{00} E^{00}_{00}

$$D^{00}_{01} = D^{20}_{01}$$

J01G8 1002 D^{20}_{01} E^{10}_{00}

$$D^{10}_{01} = (D^{30}_{01})(E^{00}_{00})^{-1}$$

J01F9 1017 D^{30}_{01} E^{20}_{00}

$$D^{20}_{01} = (Y^{80}_{02})(D^{00}_{01})(E^{10}_{00})^{-1}$$

J01H7 2016 D^{00}_{01}

$$D^{30}_{01} = D^{10}_{01} + E^{10}_{00}$$

J01F8 1102 D^{10}_{01}

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$$E^{00}_{00} = D^{30}_{00}\, Y^{80}_{00}$$

J01H9 1004 D^{10}_{00} D^{20}_{00} D^{10}_{01} E^{20}_{00}

$$E^{10}_{00} = D^{00}_{01}\, Y^{80}_{03}$$

J01G9 1004 D^{20}_{00} D^{20}_{01} D^{30}_{01} E^{20}_{00}

$$E^{20}_{00} = E^{00}_{00}\, D^{00}_{00} + E^{10}_{00}\, D^{10}_{01}$$

J01D7 1102 W^{32}_{00}

$$G^{00}_{00} = B^{20}_{03}\, M^{-2}_{00} + G^{20}_{00}\, B^{21}_{03}$$

J01K2 1102 G^{20}_{00}

$$G^{20}_{00} = G^{00}_{00}$$

J01L2 1002 G^{00}_{00} B^{30}_{03}

$$G^{00}_{01} = (B^{20}_{03}\, M^{-2}_{01} + G^{20}_{01})\,(B^{30}_{03} + B^{30}_{04})^{-1}$$

J01K3 2025 G^{20}_{01}

$$G^{20}_{01} = G^{00}_{01}$$

J01L3 1004 G^{00}_{01} B^{30}_{03} B^{30}_{04}

$$G^{00}_{02} = B^{20}_{03}\, M^{-2}_{02} + G^{20}_{02}\, B^{21}_{03}$$

J01K4 1102 G^{20}_{02}

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$G^{20}_{02} = G^{00}_{02}$

J01L4 1002 G^{00}_{02} B^{30}_{04}

$L^{-1}_{00} = 0^{10}_{00}$

J01Q8 ML

$L^{-1}_{01} = 0^{10}_{01}$

J01Q7 ML

$L^{-1}_{02} = 0^{10}_{02}$

J01R7 ML

$L^{-1}_{03} = 0^{10}_{03}$

J01R8 ML

$L^{-1}_{04} = 0^{10}_{04}$

J01R9 ML

$L^{-1}_{05} = 0^{10}_{05}$

J01S7 ML

$L^{-1}_{06} = 0^{10}_{06}$

J01S8 ML

$L^{-1}_{07} = 0^{10}_{07}$

J01S9 ML

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$L^{-1}_{09} = W^{12}_{01}$

J01R3 ML

$L^{-1}_{10} = W^{12}_{00}$

J01R4 ML

$L^{-1}_{11} = Z^{30}_{00}$

J01F6 ML

$L^{-1}_{12} = W^{23}_{00}$

J01J4 ML

$L^{-2}_{00} = W^{20}_{00}$

J01K6 ML

$L^{-2}_{01} = W^{20}_{01}$

J01K7 ML

$L^{-2}_{02} = W^{20}_{02}$

J01L6 ML

$L^{-2}_{03} = W^{20}_{03}$

J01L7 ML

$L^{-2}_{04} = N^{35}_{00}$

J01T8 ML

PX 624

$N^{20}_{00} = N^{11}_{00} + N^{11}_{01} + N^{11}_{02} + N^{11}_{03}$

J01N6 3105 T^{00}_{00}

$N^{30}_{00} = N^{11}_{01} + N^{11}_{03}$

J0108 1102 T^{00}_{00}

$N^{10}_{01} = B^{30}_{04}$

J01N5 1002 N^{30}_{06}

$N^{20}_{01} = N^{11}_{00} + N^{11}_{02}$

J01N7 1102

$N^{30}_{01} = N^{11}_{02}$

J0109 1002 T^{00}_{00}

$N^{10}_{02} = N^{30}_{06}$

J01P5 1002 N^{21}_{00} N^{31}_{00}

$N^{20}_{02} = N^{11}_{01} + N^{11}_{03}$

J01N8 1102 T^{00}_{00}

$N^{30}_{02} = N^{11}_{03}$

J01P6 1002 T^{00}_{00}

PX 824

$N^{10}_{03} = N^{30}_{03} + N^{30}_{04} + N^{30}_{05}$

J01Q6 2106 N^{21}_{00} N^{31}_{00} N^{22}_{00} N^{32}_{01}

$N^{20}_{03} = N^{11}_{00}$

J01N9 1002 T^{00}_{00}

$N^{30}_{03} = N^{11}_{01}$

J01P7 1002 N^{10}_{03} T^{00}_{00}

$N^{10}_{04} = N^{31}_{01}$

J01R6 1004 N^{21}_{00} N^{31}_{00} N^{32}_{00}

$N^{20}_{04} = N^{11}_{01}$

J0106 1002 T^{00}_{00}

$N^{30}_{04} = N^{11}_{02}$

J01P8 1002 N^{10}_{03} T^{00}_{00}

$N^{20}_{05} = N^{11}_{02}$

J0107 1002 T^{00}_{00}

PX 824

$N^{30}_{05} = N^{11}_{03}$

J01P9 1002 N^{10}_{03} T^{00}_{00}

$N^{30}_{06} = N^{10}_{01}$

J0105 1002 N^{10}_{02}

$N^{11}_{00} = W^{00}_{00}$

J01K8 1008 N^{31}_{01} N^{20}_{00} N^{20}_{01} N^{20}_{03}

$N^{21}_{00} = N^{10}_{02} + N^{10}_{03} + 0^{10}_{00} N^{10}_{04}$

J01M7 2106

$N^{31}_{00} = N^{10}_{02} + N^{10}_{03} + 0^{10}_{00} N^{10}_{04}$

J01M8 2106

$N^{11}_{01} = W^{00}_{01}$

J01K9 1008 N^{31}_{01} N^{20}_{00} N^{30}_{00} N^{20}_{02} N^{30}_{03} N^{20}_{04} test 4012

$N^{31}_{01} = N^{11}_{00} + N^{11}_{01} + N^{11}_{02} + N^{11}_{03}$

J01M9 3105 N^{10}_{04} N^{05}_{00}

$N^{11}_{02} = W^{00}_{02}$

J01L8 1008 N^{31}_{01} N^{20}_{00} N^{20}_{01} N^{30}_{01} N^{30}_{04} N^{20}_{05}

PX 824

$N^{11}_{03} = W^{00}_{03}$

J01L9 1008 N^{31}_{01} N^{20}_{00} N^{30}_{00} N^{20}_{02} N^{30}_{02} N^{30}_{05}

$N^{22}_{00} = O^{10}_{00} + N^{10}_{03}$

J01Q5 1102 N^{32}_{00}

$N^{32}_{00} = (N^{10}_{04})\ (N^{22}_{00})^{-1}$

J01R5 1017 W^{12}_{00}

$N^{32}_{01} = O^{10}_{00}\ N^{10}_{03}$

J01S5 1002 W^{12}_{01}

$N^{04}_{00} = (R^{20}_{20}\ W^{20}_{03})\ (Z^{30}_{00})^{-1}$

J01I5 1017 N^{14}_{01}

$N^{14}_{00} = (R^{30}_{05})\ (W^{00}_{00}\ W^{00}_{02})^{-1}$

J01G2 1026 Z^{30}_{00}

PX 824

$N^{14}_{01} = N^{04}_{00}$

J01J5 1002 W^{23}_{00}

$N^{24}_{01} = W^{00}_{00}$

J01J3 1002 Z^{30}_{00}

$N^{34}_{01} = R^{20}_{20} W^{20}_{01}$

J01H5 1002 W^{03}_{00}

$N^{05}_{00} = (\ ) (N^{31}_{01})^{-1}$

J01I9 1017 N^{15}_{00}

$N^{15}_{00} = N^{05}_{00}$

J01I8 1008 0^{30}_{00} 0^{30}_{01} 0^{30}_{02} 0^{30}_{03} 0^{30}_{04} 0^{30}_{05} 0^{30}_{06} 0^{30}_{07}

$N^{15}_{01} = 0^{30}_{00} + 0^{30}_{01} + 0^{30}_{02} + 0^{30}_{03}$

J01T5 3105 N^{35}_{00}

$N^{15}_{02} = 0^{30}_{04} + 0^{30}_{05} + 0^{30}_{06} + 0^{30}_{07}$

J01P1 3105 N^{35}_{00}

$N^{35}_{00} = N^{15}_{01} + N^{15}_{02}$

J01T7 1102 L^{-2}_{04}

PX 824

$O^{10}_{00} = T^{00}_{00} + O^{30}_{00}$

J01Q9 1107 O^{30}_{00} N^{21}_{00} N^{31}_{00} N^{22}_{00} N^{32}_{01} L^{-1}_{00} test ML

$O^{30}_{00} = O^{10}_{00} N^{15}_{00}$

J01T9 1002 O^{10}_{00} N^{15}_{01}

$O^{10}_{01} = T^{00}_{00} + O^{30}_{01}$

J01T6 1102 O^{30}_{01} L^{-1}_{01}

$O^{30}_{01} = O^{10}_{01} N^{15}_{00}$

J01S6 1002 O^{10}_{01} N^{15}_{01}

$O^{10}_{02} = T^{00}_{00} + O^{30}_{02}$

J01T4 1102 O^{30}_{02} L^{-1}_{02}

$O^{30}_{02} = O^{10}_{02} N^{15}_{00}$

J01S4 1002 O^{10}_{02} N^{15}_{01}

$O^{10}_{03} = T^{00}_{00} + O^{30}_{03}$

J01T3 1102 O^{30}_{03} L^{-1}_{03}

$O^{30}_{03} = O^{10}_{03} N^{15}_{00}$

J01S3 1002 O^{10}_{03} N^{15}_{01}

PX 824

$O^{10}_{04} = T^{00}_{00} + O^{30}_{04}$

J01R2 1102 O^{30}_{04} L^{-1}_{04}

$O^{30}_{04} = O^{10}_{04} N^{15}_{00}$

J01Q2 1002 O^{10}_{04} N^{15}_{02}

$O^{10}_{05} = T^{00}_{00} + O^{30}_{05}$

J01R1 1102 O^{30}_{05} L^{-1}_{05}

$O^{30}_{05} = O^{10}_{05} N^{15}_{00}$

J01Q1 1002 O^{10}_{05} N^{15}_{02}

$O^{10}_{06} = T^{00}_{00} + O^{30}_{06}$

J01T2 1102 O^{30}_{06} L^{-1}_{06}

$O^{30}_{06} = O^{10}_{06} N^{15}_{00}$

J01S2 1002 O^{10}_{06} N^{15}_{02}

$O^{10}_{07} = T^{00}_{00} + O^{30}_{07}$

J01T1 1102 O^{30}_{07} L^{-1}_{07}

$O^{30}_{07} = O^{10}_{07} N^{15}_{00}$

J01S1 1002 O^{10}_{07} N^{15}_{02}

PX 824

$R^{20}_{00} = B^{01}_{06}$

J01G3 1002 R^{01}_{00} R^{00}_{02}

$R^{00}_{02} = R^{20}_{00}$

J01D2 1002 R^{20}_{04} Y^{21}_{02}

$R^{20}_{04} = R^{00}_{02}$

J01C2 1002 R^{00}_{06} R^{30}_{05}

$R^{30}_{05} = R^{20}_{04}$

J01F2 1002 N^{14}_{00}

$R^{00}_{06} = R^{20}_{04}$

J01B2 1002 R^{20}_{08}

$R^{20}_{08} = R^{00}_{06}$

J01B3 1004 R^{30}_{09} R^{00}_{10} Z^{30}_{00}

$R^{30}_{09} = R^{20}_{08}$

J01D3 1002 R^{10}_{11} Y^{32}_{00}

$R^{00}_{10} = (R^{20}_{08})\ (Z^{30}_{00})^{-1}$

J01C3 1017 Y^{30}_{00}

PX 824

$R^{10}_{11} = R^{30}_{09}$

J01E3 1002 R^{30}_{13} Y^{11}_{00}

$R^{30}_{13} = R^{10}_{11}$

J01B4 1002 R^{10}_{15}

$R^{10}_{15} = R^{30}_{13}$

J01C4 1002 R^{30}_{17} R^{21}_{00}

$R^{30}_{17} = R^{10}_{15}$

J01D4 1004 R^{00}_{18} Y^{32}_{01}

$R^{00}_{18} = R^{30}_{17}$

J01B5 1008 R^{20}_{20} W^{23}_{00} W^{23}_{00} Y^{02}_{00} Y^{30}_{00}

$R^{20}_{20} = R^{00}_{18}$

J01G5 1004 Y^{22}_{00} N^{34}_{01} N^{04}_{00}

$R^{01}_{00} = R^{20}_{00} + R^{21}_{00}$

J01F4 1107 R^{21}_{00} Y^{20}_{00} Y^{20}_{01} Y^{21}_{00}

$R^{21}_{00} = (R^{01}_{00})\ (R^{10}_{15})^{-1}$

J01F3 1017 R^{01}_{00}

PX 824

$S^{10}_{00} = B^{00}_{04}\ S^{00}_{01}\ B^{00}_{05}$

J01I6 1002 S^{20}_{01}

$S^{30}_{00} = S^{20}_{01}$

J01J7 1002 S^{00}_{02}

$S^{00}_{01} = S^{20}_{01}$

J01G6 1004 $S^{20}_{01}\ S^{10}_{00}\ Y^{20}_{01}$

$S^{20}_{01} = (B^{00}_{04}\ B^{00}_{05}\ S^{00}_{02} + S^{00}_{01})(S^{10}_{00})^{-1}$

J01H6 2016 $S^{00}_{01}\ S^{30}_{00}$

$S^{00}_{02} = (\ )\ (S^{30}_{00})^{-1}$

J01J6 1017 $S^{20}_{01}\ Y^{20}_{00}$

$W^{00}_{00} = (W^{20}_{00})\ (C^{31}_{01} + B^{30}_{03})^{-1}$

J01M1 1026 $W^{20}_{00}\ W^{20}_{01}\ N^{11}_{00}\ N^{24}_{01}\ T^{00}_{02}$

$W^{20}_{00} = (W^{00}_{00} + B^{00}_{05}\ B^{00}_{04})\ (B^{10}_{04})^{-1}$

J01N1 2016 $W^{00}_{00}\ C^{31}_{00}\ L^{-2}_{00}\ B^{00}_{06}$

$W^{00}_{01} = (W^{20}_{01})\ (C^{31}_{02} + B^{30}_{03})^{-1}$

J01M2 1026 $W^{20}_{01}\ W^{20}_{02}\ N^{11}_{01}\ W^{23}_{00}$

PX 824

$$W^{20}_{01} = W^{00}_{01} + W^{00}_{00} B^{00}_{04}$$

J01N2 1107 $W^{00}_{01}\ C^{31}_{01}\ L^{-2}_{01}\ N^{34}_{01}\ B^{00}_{06}$

$$W^{00}_{02} = (W^{20}_{02})\ (C^{31}_{03} + B^{30}_{03})^{-1}$$

J01M3 1026 $W^{20}_{02}\ W^{20}_{03}\ N^{11}_{02}\ N^{24}_{00}\ N^{14}_{02}$

$$W^{20}_{02} = W^{00}_{02} + W^{00}_{01} B^{00}_{04}$$

J01N3 1107 $W^{00}_{02}\ C^{31}_{02}\ L^{-2}_{02}\ B^{00}_{06}$

$$W^{00}_{03} = (W^{20}_{03})\ (C^{31}_{00} + B^{30}_{03})^{-1}$$

J01M4 1026 $W^{20}_{03}\ N^{11}_{03}\ W^{23}_{00}$

$$W^{20}_{03} = W^{00}_{03} + W^{00}_{02} B^{00}_{04}$$

J01N4 1107 $W^{00}_{03}\ C^{31}_{03}\ L^{-2}_{03}\ N^{04}_{00}\ B^{00}_{06}$

$$W^{12}_{00} = (N^{32}_{00} + W^{32}_{00})\ (B^{00}_{06})^{-1}$$

J01P4 2016 $W^{32}_{00}\ L^{-1}_{10}\ B^{30}_{05}$

$$W^{32}_{00} = W^{12}_{00} + E^{20}_{00}$$

J01Q4 1102 W^{12}_{00}

PX 824

$$W^{12}_{01} = (N^{32}_{01} + W^{32}_{01})\,(B^{00}_{08})^{-1}$$

J01P3 2016 $W^{32}_{01}\,L^{-1}_{09}\,B^{30}_{05}$

$$W^{32}_{01} = W^{12}_{01}$$

J01Q3 1002 W^{12}_{01}

$$W^{03}_{00} = (W^{23}_{00})\,(N^{34}_{01}\,Z^{30}_{00} + B^{30}_{03})^{-1}$$

J01G4 1026 W^{23}_{00}

$$W^{23}_{00} = (R^{00}_{18}\,W^{00}_{01} + R^{00}_{18}\,W^{00}_{03} + W^{03}_{00})(N^{14}_{01})^{-1}$$

J01H4 3015

$$Y^{20}_{00} = (S^{00}_{02}\ R^{01}_{00})\ (Y^{02}_{00})^{-1}$$

T J - B3 9122 Y^{50}_{10} Y^{50}_{00}

$$Y^{30}_{00} = (R^{00}_{10} + R^{00}_{18})\ (Y^{22}_{00})^{-1}$$

J01G7 9122 Y^{51}_{00}

$$Y^{20}_{01} = (S^{00}_{01}\ R^{01}_{00})\ (Y^{02}_{00})^{-1}$$

J01E6 9122 Y^{50}_{11} Y^{50}_{01}

$$Y^{11}_{00} = (R^{10}_{11})\ (Y^{32}_{01})^{-1}$$

J01E5 9118 Y^{50}_{01} Y^{50}_{11}

$$Y^{21}_{00} = (R^{01}_{00})\ (Y^{02}_{00})^{-1}$$

T J - A3 9118 Y^{55}_{00}

$$Y^{21}_{02} = (R^{00}_{02})\ (Y^{32}_{00})^{-1}$$

J01D6 9118 Y^{50}_{00} Y^{50}_{01}

$$Y^{02}_{00} = R^{00}_{18}$$

J01C5 9218 Y^{20}_{00} Y^{20}_{01} Y^{21}_{00}

$$Y^{22}_{00} = R^{20}_{20}$$

T J - A4 9218 Y^{30}_{00}

$Y^{32}_{00} = R^{30}_{09}$

J01D5 9218 Y^{21}_{02}

$Y^{32}_{01} = R^{30}_{17}$

J01F5 9218 Y^{11}_{00}

$Y^{50}_{00} = Y^{20}_{00}\ Y^{21}_{02}$

J01E9 9411 Y^{55}_{00}

$Y^{50}_{01} = Y^{20}_{01}\ Y^{21}_{02}$

J01C9 9411 Y^{55}_{00}

$Y^{50}_{10} = Y^{20}_{00}\ Y^{11}_{00}$

J01E8 9411 Y^{55}_{00}

$Y^{50}_{11} = Y^{20}_{01}\ Y^{11}_{00}$

J01C8 9411 Y^{55}_{00}

$Y^{51}_{00} = Y^{30}_{00}$

T J - B5 9411 Y^{53}_{00}

Y^{52}_{00} = Memory Core

T J - A5 9811 Z^{30}_{00}

pr 824

$$Y^{53}_{00} = Y^{51}_{00}$$

T J - A6 9622 Memory Core

$$Y^{55}_{00} = Y^{50}_{00} - Y^{50}_{01} - Y^{50}_{10} - Y^{50}_{11} - Y^{21}_{00}$$

T J - B4 9522 Memory Cores 1 and 2

$$Z^{10}_{00} = (Z^{30}_{00})\,(B^{01}_{08} + B^{30}_{03})^{-1}$$

J01J9 1026 Z^{30}_{00}

$$Z^{30}_{00} = Z^{10}_{00} + R^{20}_{08}\,N^{24}_{01} + N^{14}_{00}\,Y^{52}_{00}$$

J01J8 2106 $Z^{10}_{00}\,R^{00}_{10}\,N^{04}_{00}\,W^{03}_{00}\,L^{-1}_{11}$