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REVISION TO MANUAL

MH-1049

VOLUME I

MAGNETIC TAPE UNIT

TYPE 1540

(UNIVAC)

APRIL 26, 1976

THIS REVISION UPDATES THE MANUAL TO REFLECT THE CHANGE DATA INDICATED ON THE RECORD-OF-CHANGES PAGE, WHICH IS INCLUDED AS PART OF THIS REVISION.

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MARCH 25, 1975

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Volume I
Sections 1-7

TECHNICAL MANUAL

MAGNETIC TAPE UNIT

TYPE 1540

(UNIVAC)

November 1967
(Revised April 26, 1976)

PX 3334-1-4

Prepared for
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
Contract NAS5-23000

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Reissued November 1967	Univac NAS5-9816	EI's: 1895 1896 2360 2361 2362 2507 2555 2593 2594 2608 2640 2657 2705 2721 2722 2913 2914 2915 3251 3251, Ch. 1	August 7, 1972	Bendix NAS5-23000 DWR-0536	EI's: 4264 4264, Ch. 1 4264, Ch. 2 4540 4600 4600, Ch. 1 EC's: 0123-216E 0178-216E 0178-216E, Ch. 1 0178-216E, Ch. 2 CRS, GSFC July 29, 1971 CRS, CYI Aug. 25, 1971
			March 25, 1975	Bendix NAS5-23000 DWR-3345	EC's: 0888 0983 0983, Ch. 1 0983, Ch. 2 0983, Ch. 3 1257 1257, Ch. 1
November 5, 1969	Bendix NAS5-10750 TD-626 OMPUB-507	EI's: 3520 3521, Ch. 2 CRS, CYI Feb. 12. 1968 CRS, GWM July 17, 1968 CRS, MFED Nov. 18, 1968 MPL-397	April 26, 1976	Bendix NAS5-23000 DWR-4661	EI's: 1895, Ch. 1 2360, Ch. 1 2360, Ch. 2 2361, Ch. 1 2361, Ch. 2 2361, Ch. 3 2361, Ch. 4 2507, Ch. 1 2555, Ch. 1 2593, Ch. 1

RECORD-OF-CHANGES

DATE OF REVISION	CONTRACTOR & AUTHORITY	DESCRIPTION OF CHANGE	DATE OF REVISION	CONTRACTOR & AUTHORITY	DESCRIPTION OF CHANGE
April 26, 1976 (Cont.)		EI's: 2608, Ch. 1 2705, Ch. 1 2705, Ch. 2 2722, Ch. 1 2913, Ch. 1 2913, Ch. 2 2915, Ch. 1 2915, Ch. 2 2915, Ch. 3 2915, Ch. 4 4127A 4127A, Ch. 1 4127A, Ch. 2 4127A, Ch. 3 4127A, Ch. 4 4127A, Ch. 5 4127A, Ch. 6 4127A, Ch. 7 4127A, Ch. 8 4127A, Ch. 9 4127A, Ch. 10 EC's: 2057 2058			

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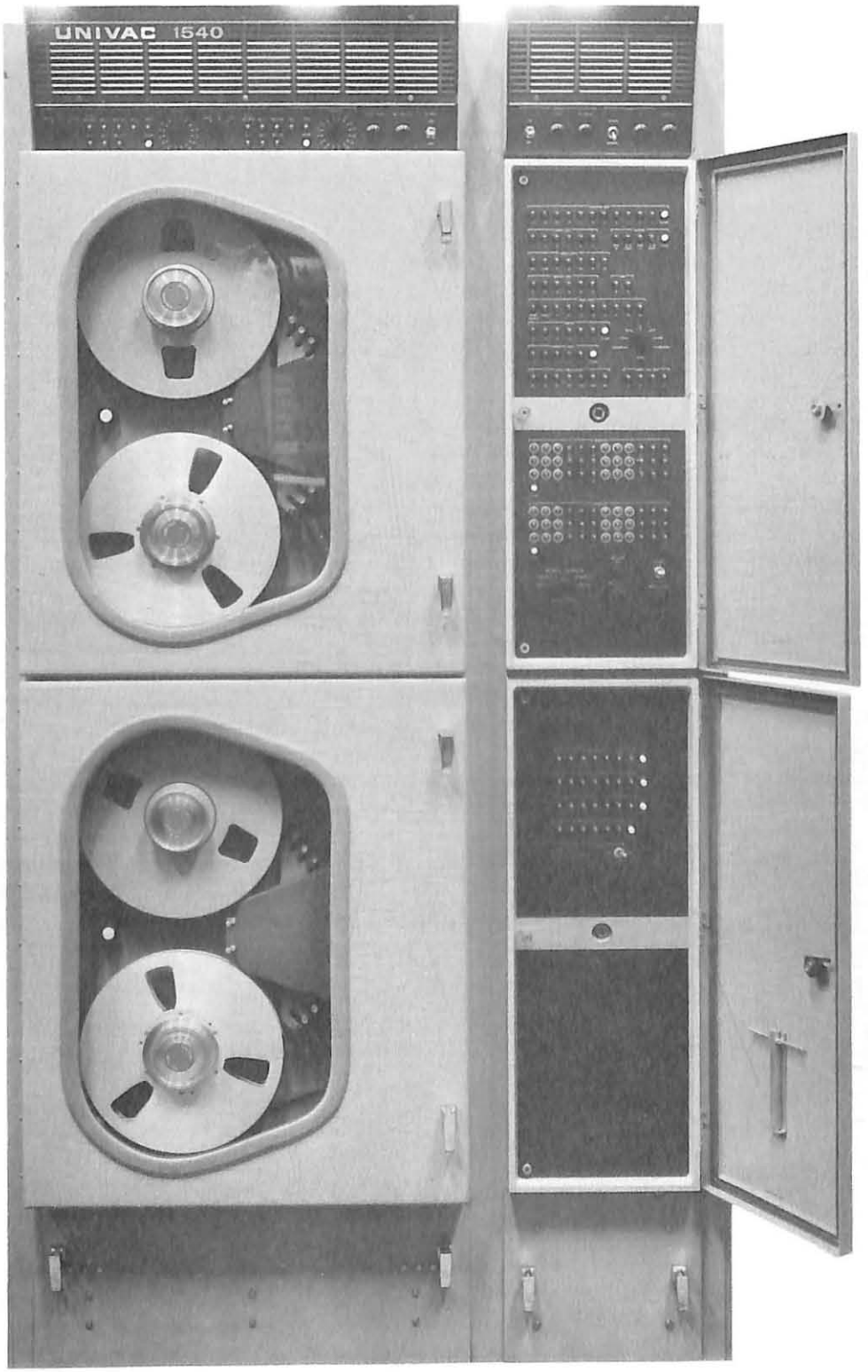

Figure 1-1. Magnetic Tape Unit (Basic Unit)

SECTION 1

GENERAL INFORMATION

1-1. SCOPE.

The information contained in this technical manual will enable a data processing technician to install, operate, and maintain the UNIVAC® Type 1540 Magnetic Tape Unit.

Section 1 contains a general description of the Magnetic Tape Unit and is intended for personnel requiring a general knowledge of the equipment. Detailed installation, operation, and maintenance information is contained in the subsequent sections of the manual.

1-2. EQUIPMENT ILLUSTRATION.

The Type 1540 Magnetic Tape Unit, commonly referred to as the MTU, is a large-capacity, medium-speed, magnetic tape storage system. Figures 1-1 and 1-2 illustrate the basic and add-on MTU configurations.

1-3. GENERAL DESCRIPTION.

a. FUNCTIONAL DESCRIPTION. - The MTU is capable of either receiving data from a computer and recording it on magnetic tape or retrieving information previously recorded on tape and transferring it to a computer. The MTU is compatible in all respects with the Univac computers listed in table 1-1. The MTU also may be used in an off-line mode of operation with the UNIVAC ® Type 1469 High-Speed Printer. When used with the printer, information recorded on magnetic tape is retrieved and transferred to the printer for recording in printed form.

The basic MTU consists of a tape transport (or handler) containing two tape transports and a tape transport control section, and a magnetic tape control section. However, there may be as many as eight units connected together to form a magnetic tape storage system (see figure 1-3). When units are connected to form a configuration other than the basic unit, the magnetic tape control section of the basic unit controls the other units; the other units only contain two tape transports and a tape transport control section.

The magnetic tape control section of the basic MTU selects and directs the proper tape transport in a magnetic tape configuration. The MTU's tape transport control section selects and directs the proper tape transport in its associated unit. The tape transports perform the movement and the recording, or reading, of the magnetic tape.

The MTU uses one-half inch, Mylar backed magnetic tape in an "A" wind configuration. The upper reel is the supply or payout reel, and the bottom or left reel is the takeup reel. The oxide coating of the tape is in or toward the center of the reel. The MTU records information received from the computer on the tape with one of the three densities. The density of recording depends on the computer program.

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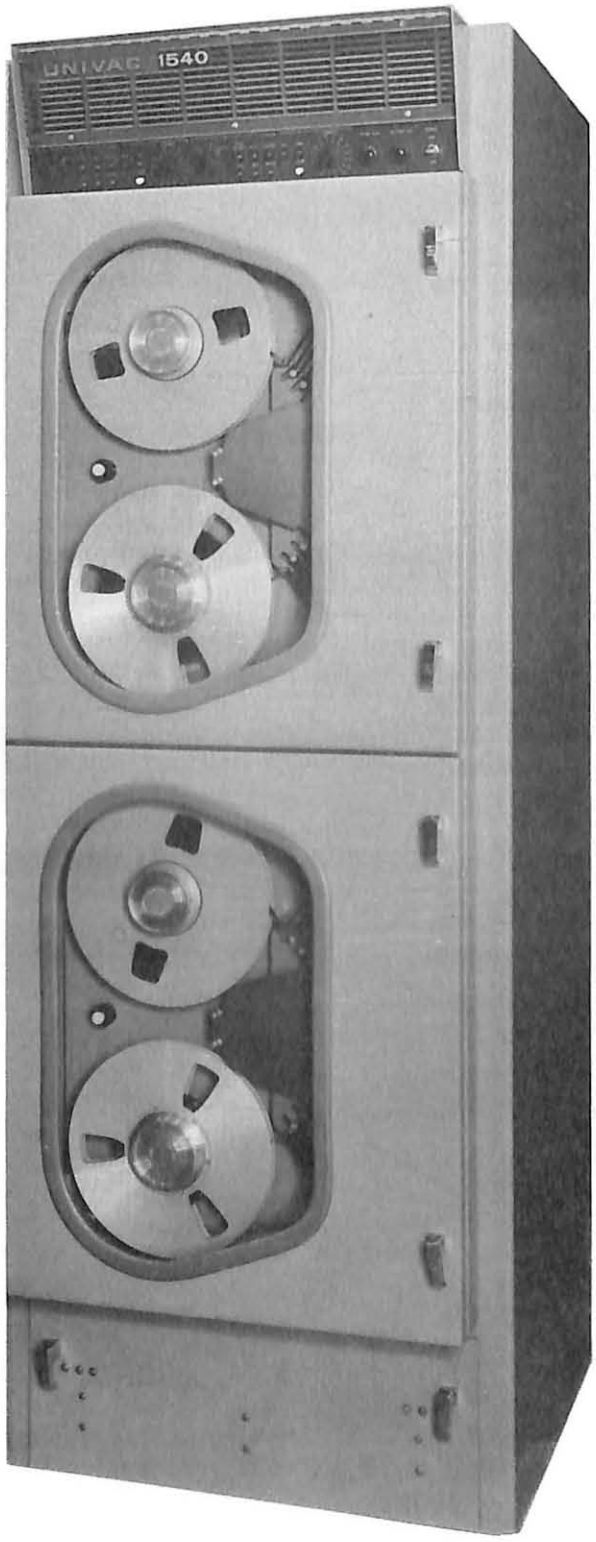

Figure 1-2. Magnetic Tape Unit (Add-on Unit)

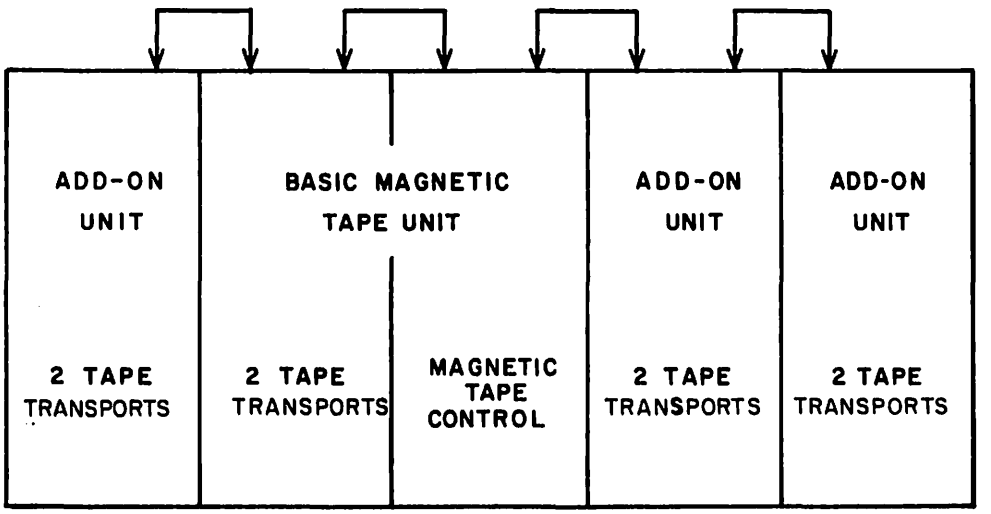

Figure 1-3. Magnetic Tape Storage System (Maximum Configuration)

A flexible format allows the recording and reading of magnetic tapes compatible in all respects with the IBM ®727, 729II, 729IV, and 729VI magnetic tape systems and with the UNIVAC ® Type 1240 Magnetic Tape Unit.

TABLE 1-1. MAGNETIC TAPE UNIT-COMPUTER COMPATIBILITY

COMPUTER NOMENCLATURE		INTERFACE*	
UNIVAC	MILITARY	WORD LENGTH (BITS)	VOLTAGE LEVEL (VDC)
490	None	30	-3
CP-667	CP-667/USQ-20(V)	18 or 36	-15 or -3
1107	None	36	-3
1206	CP-642/USQ-20(V)	30	-15
1206	CP-642A/USQ-20(V)	30	-15
1212	CP-642B/USQ-20(V)	30	-15 or -3
1218	None	18 or 36	-15 or -3
1219	None	18 or 36	-15 or -3
1230	Modified CP-642B/ USQ-20(V)	30	-15 or -3
CP-808	CP-808/TYK	30	-15 or -3

* In systems using less than 36 data lines, the unused lines are always interpreted as 0's.

b. OPTIONAL CONFIGURATIONS. - The MTU is available in several optional configurations; all configurations have identical functional characteristics but have an optional number of tape transports, optional cooling, optional computer interfaces, and optional computer duplexing.

(1) TAPE TRANSPORTS. - The MTU is available with two, four, six, or eight tape transports.

(2) COOLING. - There are two methods of cooling the MTU, water cooling or air cooling.

In a water-cooled unit, the blowers recirculate air over water-cooled coils. The blowers mount in the lower-rear of the unit, and the cooling coil mounts on the rear of the unit. Each tape transport section utilizes two blowers; the magnetic tape control section utilizes one blower.

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In an air-cooled unit, the blowers pull in room air through the air intake located at the top-front of the cabinet, circulate it through the unit, and exhaust it through the exhaust located at the bottom-rear of the cabinet. Each tape transport section utilizes four blowers; the magnetic tape control section utilizes two blowers.

(3) INTERFACE. - The optional interfaces between the MTU and a computer are as follows.

1) 18-bit parallel data transmission, nominal 15-volt logic level.

2) 24-bit parallel data transmission, nominal 15-volt logic level.

3) 30-bit parallel data transmission, nominal 15-volt logic level.

4) 36-bit parallel data transmission, nominal 15-volt logic level.

5) 18-bit parallel data transmission, nominal 3-volt logic level.

6) 24-bit parallel data transmission, nominal 3-volt logic level.

7) 30-bit parallel data transmission, nominal 3-volt logic level.

8) 36-bit parallel data transmission, nominal 3-volt logic level.

(4) DUPLEXING. - Computer duplexing is an optional feature of the MTU.

c. MODULARITY. - The MTU system can contain from one to four individual units with each containing two tape transport (see figure 1-3). The basic computer consists of interface and control circuitry, two tape transports, and associated read/write electronics. Each MTU add-on unit consists of two tape transports and associated read/write electronics.

d. REFERENCES. - Refer to the Potter tape handler manual furnished with the equipment for information pertaining to the tape transport.

The maintenance test manuals for computer testing of the Magnetic Tape Unit is supplied with the equipment.

1-4. QUICK REFERENCE DATA.

Table 1-2 lists quick reference data.

1-5. EQUIPMENT LISTS.

a. EQUIPMENT AND PUBLICATIONS SUPPLIED. - Table 1-3 lists the equipment and publications supplied with each MTU.

b. EQUIPMENT REQUIRED BUT NOT SUPPLIED. - Table 1-4 lists the equipment that is required but is not supplied with the MTU.

c. SHIPPING DATA. - Each equipment is shipped as one complete unit either crated or uncrated, depending on the mode of transportation (refer to table 1-5).

d. MODULE COMPLEMENT. - Table 7-2 lists the printed circuit module complement of the MTU.

1-6. GLOSSARY OF SYMBOLS AND ABBREVIATIONS.

Table 1-6 lists the symbols and abbreviations, and their associated definitions, used in set 1 and 2 of this manual.

TABLE 1-2. QUICK REFERENCE DATA

INPUT POWER		
Logic	115 vac ±10%, 400 cycles ±5%, 3-phase, regulated	
Blowers (water-cooled unit)	115 vac ±10%, 400 cycles, 3-phase, regulated	
Tape Transports Blowers (air-cooled unit)	115 vac, 60 cycles, unregulated 115 vac ±5%, 400 cycles, 3-phase, regulated	
	INPUT	OUTPUT
POWER SUPPLY CHARACTERISTICS	115 vac ±5%, 400 cycles ±5%, 3-phase	+15 vdc -15 vdc -4.5 vdc -26.5 vdc +26.5 vdc
SIGNAL LEVELS	ON EXTERNAL LINES	INTERNAL
LOGIC 1	0±1.5 vdc	-4.5 vdc
LOGIC 0	-13.5+3.5, -4 vdc	0 vdc
LOGIC 1	0+0.5 vdc	-4.5 vdc
LOGIC 0	-3,-0.75 vdc	0 vdc
	INPUT	OUTPUT
DATE TRANSMISSION	18-, 24-, 30-, or 36-bit parallel	18-, 24-, 30- or 36-bit parallel
COOLING CHARACTERISTICS	Cabinet air recirculated over water-cooled coils or room air circulated through the cabinet and exhausted.	Overtemperature warning 46°C (115°F) Overtemperature shutdown 60°C (140°F)
RECORD LENGTH	Any length up to capacity of tape.	

	INPUT	OUTPUT
DATE TRANSMISSION	18-, 24-, 30-, or 36-bit parallel	18-, 24-, 30- or 36-bit parallel
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4) 36-bit parallel data transmission, nominal 15-volt logic level.

5) 18-bit parallel data transmission, nominal 3-volt logic level.

6) 24-bit parallel data transmission, nominal 3-volt logic level.

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Tape Transports and blowers (air-cooled unit)	115 vac, 60 cycles, unregulated	
	INPUT	OUTPUT
POWER SUPPLY CHARACTERISTICS	115 vac ±5%, 400 cycles ±5%, 3-phase	+15 vdc -15 vdc -4.5 vdc -26.5 vdc +26.5 vdc
SIGNAL LEVELS	ON EXTERNAL LINES	INTERNAL
LOGIC 1	0±1.5 vdc	-4.5 vdc
LOGIC 0	-13.5+3.5, -4 vdc	0 vdc
LOGIC 1	0+0.5 vdc	-4.5 vdc
LOGIC 0	-3,-0.75 vdc	0 vdc
	INPUT	OUTPUT
DATE TRANSMISSION	18-, 24-, 30-, or 36-bit parallel	18-, 24-, 30- or 36-bit parallel
COOLING CHARACTERISTICS	Cabinet air recirculated over water-cooled coils or room air circulated through the cabinet and exhausted.	Overtemperature warning 46°C (115°F) Overtemperature shutdown 60°C (140°F)
RECORD LENGTH	Any length up to capacity of tape.	

TABLE 1-2. QUICK REFERENCE DATA (CONT.)

RECORDING LEVEL	Nonreturn to zero.	
RECORDING DENSITY	Programmable 200, 556, or 800 frames-per-inch.	
TAPE COMPATIBILITY	Recorded tapes are interchangeable with the IBM tape systems and with the UNIVAC Type 1240 MTU.	
TAPE TYPE	Instrumentation grade Mylar.	
TAPE WIDTH	1/2-inch	
TAPE THICKNESS	1 or 1-1/2 mils	
REELS	Potter Precision NARTB, IBM 10 1/2-inch, or Ampex 1/2-inch	
SUPPLY HUB	Instant release using a push-pull mechanism.	
TAKEUP HUB	Fixed semi-permanent mount for takeup reel.	
TAPE WIND	"A" wind. Oxide coating inside. Payout reel on top.	
TAPE SPEED	ALL OPERATIONS EXCEPT REWIND	REWIND
1540 MTU	120 inches-per-second	240 inches-per-second until approximately 100 feet from beginning of tape, then the speed reduces to 120 inches-per-second.
1541 MTU	150 inches-per-second	225 inches-per-second until approximately 100 feet from beginning of tape, then the speed reduces to 150 inches-per-second.
VARIATIONS	±2%	
HEAD CHARACTERISTICS		
TRACKS	7 tracks, IBM format.	
WRITE HEAD	Track width: 0.048±0.0005 inch	
	Gap length: 0.0005-inch nominal	
	Resistance: 7.5 ohms (center tap to end)	
	Record current: 60 milliamperes nominal	
READ HEAD	Track width: 0.030±0.0005 inch	
	Gap length: 0.00025-inch nominal	
	Resistance: 10 ohms	

TABLE 1-2. QUICK REFERENCE DATA (CONT.)

READ HEAD (CONT.)	Readback voltage: 20 millivolts peak-to-peak minimum on all channels
CROSSTALK	1540 MTU: write to read 5% maximum 1541 MTU: write to read 8% maximum Interchannel: 5% maximum
AMPLITUDE VARIATION	Not more than 25% from 200 bits-per-inch to 800 bits-per-inch.
DYNAMIC SKEW	Less than 2 microseconds between any two channels.
STATIC SKEW	Less than 3 microseconds between the center channel and any other channel.
ACCURACY	Not more than one error in recording or reading 10^7 bits.
READ-WRITE GAP SEPARATION	0.200±0.002 inch
ERASE HEAD	Width: Full tape width Gap: 0.018-inch nominal Resistance: 70 ohms nominal Erase current: 60 milliamperes ±10% Erasure of data: 99% minimum
ERASE-WRITE GAP SEPARATION	0.687-inch nominal

TABLE 1-3. MAGNETIC TAPE UNIT, EQUIPMENT AND PUBLICATIONS SUPPLIED

QUANTITY PER UNIT			
MTU		NOMENCLATURE	
BASIC UNIT	ADD-ON UNIT	NAME	DESIGNATION
2	0	Technical Manual for Type 1540 Magnetic Tape Unit, Volumes I and II	PX 3334-1-2 PX 3334-2-2
2	0	Handbook for MTS-120-X41427 Magnetic Tape System or Handbook for MTS-120 Magnetic Tape System	Potter Instrument Company, S365-84 or S365-55
0	0	Handbook of Operation and Maintenance for MT-150A Magnetic Tape Transport System	Potter Instrument Company
0	0	Technical Manual for TM-12(R) Tape Transport	Computer Products Division, Ampex Corporation
2*	0	1540-1218/1219 Maintenance Test	PX 3644-0-1
2*	0	1540-642B/1230 Maintenance Test	PX 3645-0-1
2	2	Tape Reel	S2356975 (IBM) 421602-8 (Potter), or 3101267-10 (Ampex)
1	1	Cable Assembly, Power, Electrical	7025995-00
1**	0	Connector, Plug, Electrical (Dummy)	7025991-00
1	0	Cleaning Kit	425484 (Potter)
1	0	Circuit Board Extender	EC-120 (Potter)
0	0	Circuit Board Extender	EC-150 (Potter)
0	0	Extender Card, Test Points	3112490 (Ampex)
2***	2***	Coupling, Water Supply (Hansen)	91066-05
1	0	Wrench, Chassis Engaging	7008938-00

* The maintenance test manual provided is dependent on the type of computer system for which the MTU is destined (the title designates which computer system requires which test).

** Used on the last add-on unit located on the right of the basic unit (see figure 2-5).

*** For water-cooled units only.

TABLE 1-4. MAGNETIC TAPE UNIT, EQUIPMENT REQUIRED BUT NOT SUPPLIED

QTY. PER EQUIP.	NOMENCLATURE		REQUIRED USE	REQUIRED CHARACTERISTICS
	NAME	DESIGNATION		
1	Oscilloscope	H02-170A or 545A (Tektronix)	Troubleshooting and maintenance procedures.	Max horizontal sweep: 220 msec Max amplitude: 220 volts, peak-to-peak Response: 500 kc
1	Plug-in Dual Trace Amplifier	H02-162A or CA (Tektronix)	Troubleshooting and maintenance procedures.	
1	Plug-in High Gain Amplifier	H02-162D or D (Tektronix)	Troubleshooting and maintenance procedures.	
1	Multimeter	AN/PSM-4C	Troubleshooting and maintenance procedures.	Voltages: 12 to 115 vac 0 to 26.5 vdc Frequency: 60 to 400 cps
1	Spring Scale, 0 - 2 lb	219-2 (CHATILLON)	Tension arm adjustment	Tension arm force: 24 ozs
1	Spring Scale, 0 - 20 lb	719-20 (CHATILLON)	Pinch-roller solenoid adjustment.	Breakaway force: Static - 16 lb (min) Dynamic - 8 lb
1	Retaining Applicator	CR-12 and CR-18 (Heyer)	Maintenance: apply retaining rings.	
1	Retaining Ring Plier	No's. 1, 2, and 3 (Heyer)	Maintenance: remove retaining rings.	
1	Wire-Wrap Gun	14-R2 (Gardner-Denver)	Maintenance: wire-wrap terminal connections.	
1	Wire-Wrap Bit, 24 gauge	26263 (Gardner-Denver)	Maintenance: used with gun to wrap 24 gauge wire around terminals.	

TABLE 1-4. MAGNETIC TAPE UNIT, EQUIPMENT REQUIRED BUT NOT SUPPLIED (CONT.)

QTY. PER EQUIP.	NOMENCLATURE		REQUIRED USE	REQUIRED CHARACTERISTICS
	NAME	DESIGNATION		
1	Wire-Wrap Sleeve, 24 gauge	18840 (Gardner-Denver)		
1	Wire-Unwrap Tool, 24 gauge	500130 (Gardner-Denver)	Maintenance: unwrap wire terminal connections.	
1	Insertion Tool	380306-2 and 380306-3 (AMP)	Maintenance: insert taper pins.	
1	Crimping Tool	47043 and 48698 (AMP)	Maintenance: crimp wire in taper pins.	
1	Nutdriver	No. 20 (Gulmite)	Maintenance: loosen and secure knurled nut holding indicators.	
	Wrench Set, Hux	AW-1011K (Snap-on)	Tape handler maintenance.	
1	Tool Set	AN/USM-3	General maintenance.	
1	Hand Stripper	45-171 (Ideal)	Maintenance: removal of wire insulation.	
1	Tape Analysis Solution	Visi-Mag Type F	Maintenance: make magnetic field on tape visible.	
1	Magnetic Tape	1/2 498-25GR (3M)	Troubleshooting and maintenance procedures.	
1	Master Alignment Tape	IBM432640 (600 Ft.) IBM432641 (1200 Ft.)	Maintenance procedures.	
1	Card Extender Cable Assembly	7009452 (UNIVAC)	Troubleshooting procedures.	
1	Trouble Light		Troubleshooting procedures.	
1	Wire-Wrap Bit, 30 gauge	504221 (Gardner-Denver)	Maintenance: used with gun to wrap 30-gauge wire around terminals.	

TABLE 1.-4. MAGNETIC TAPE UNIT, EQUIPMENT REQUIRED BUT NOT SUPPLIED (CONT.)

QTY. PER EQUIP.	NOMENCLATURE		REQUIRED USE	REQUIRED CHARACTERISTICS
	NAME	DESIGNATION		
1	Wire-Wrap Sleeve, 30 gauge	500350 and 17611-2 (Gardner-Denver)		
1	Wire-Unwrap Tool, 30 gauge	505244 (Gardner-Denver)	Maintenance: unwrap wire terminal connections.	
1	Wire-Wrap Sleeve, 20 gauge	18633 (Gardner-Denver)	Maintenance: wrap resistor-wire terminal connections.	
1	Wire-Wrap Bit, 20 gauge	26245 (Gardner-Denver)	Maintenance: wrap resistor-wire terminal connections.	

TABLE 1-5. MAGNETIC TAPE UNIT, SHIPPING DATA

NOMENCLATURE		OVERALL DIMENSIONS (IN.)*			WEIGHT (LBS)*	VOLUME (CU.IN.)
TYPE	OPTIONS	HEIGHT	WIDTH	DEPTH		
Basic Unit	Air Cooled	72	38	29	1,388	91,175
	Water Cooled	72	38	35.46	1,538	99,300
Add-on Unit	Air Cooled	72	25.88	29	948	54,037
	Water Cooled	72	25.88	35.46	1,098	66,074

*Equipment not crated. If shipped crated, add approximately 6 inches to each dimension and 150 pounds to each weight.

TABLE 1-6. GLOSSARY OF SYMBOLS AND ABBREVIATIONS

SYMBOL OR ABBREVIATION	DEFINITION
Symbols	
$\Longrightarrow$	Signifies "if", "when", or "means".
$\longrightarrow$	Transfer to specified direction.
$\longleftrightarrow$	Transfer in either direction.

TABLE 1-6. GLOSSARY OF SYMBOLS AND ABBREVIATIONS (CONT.)

SYMBOL OR ABBREVIATION	DEFINITION
Symbols (Cont.)	
•	Boolean algebraic symbol for "and".
+	Boolean algebraic symbol for "or".
Abbreviations	
ACK	Acknowledge
ADDR	Address
AMPS	Amplifiers
BOT	Beginning of tape (designates load point)
BPI	Bits-per-inch
CLD	Control line driver
CLR	Clear
COND	Conditional
CT	Count
CTR	Counter
DESIG	Designator or Designation
EF	External Function
EN	Enable
EOR	End of record
EOT	End of tape
EOW	End of write
ERR	Error
FTG	Frame time generator
FUNCT	Function
FWD	Forward
H	High in reference signals, represents 0.0 volt.

TABLE 1-6. GLOSSARY OF SYMBOLS AND ABBREVIATIONS (CONT.)

SYMBOL OR ABBREVIATION	DEFINITION
Abbreviations (Cont.)	
IA	Input amplifier
IDR	Input data request
IMP COND	Improper condition
INTER	Interrupt
I/O	Input/output
IPS	Inches-per-second
IRG	Interrecord gap
ITE	Input timing error
K_C	Character counter
L	Low, in reference to logic singnals, represents -4.5 volts and in reference to non-logic signals represents -15 volts.
LONG	Longitudinal
LTHC	Local tape handler control
MCLR	Master clear
MOD	Modulus, moduli, or modified
MTC	Magnetic tape control
MTU	Magnetic Tape Unit
ODR	Output data request
OP	Operation
OTE	Output timing error
RCD	Read compensation delay
RDNT	Redundant (octal)
REG	Register
REQ	Request or require

TABLE 1-6. GLOSSARY OF SYMBOLS AND ABBREVIATIONS (CONT.)

SYMBOL OR ABBREVIATION	DEFINITION
Abbreviations (Cont.)	
R_L	Read register lower
R^*_L	R* register lower
R_U	Read register upper
R^*_U	R* register upper
RWD	Rewind
SECT	Section
SELECT	Select or selective
SEQ	Sequence
TM	Tape Mark
WCD	Write compensation delay
XIRG	Extended interrecord gap
XLATION	Translation

SECTION 2

INSTALLATION

2-1. UNPACKING AND HANDLING.

The basic MTU is housed in a single cabinet and consists of two magnetic tape transports and their associated power and control circuits.

Installation personnel must be familiar with the contents of sections 1 through 6 of this manual and the tape handler manual before attempting the installation and checkout procedures.

To remove the equipment from a shipping crate, proceed as follows.

STEP 1. Place shipping crate in upright position and cut steel strapping along side of crate.

STEP 2. Remove lid and two adjacent sides from crate and open waterproof barrier.

STEP 3. Remove inner carton from crate.

STEP 4. Open carton and remove Magnetic Tape Unit.

STEP 5. Check assembly for chips, dents, scratches, broken indicators, and missing parts.

STEP 6. Ensure that all items listed in table 1-3 are included in shipment.

STEP 7. Ensure that all printed circuit cards are in correct jack locations and are secured properly. See chassis maps, figures 8-118 through 8-123 in volume II of this manual, for card locations.

2-2. SITE SELECTION.

Select a level site area that has provisions for securing the unit to the floor or deck. The area of the floor or deck on which the unit is to be mounted must be flat to within 0.03 inch. Adequate space (see figures 2-1 through 2-4) and proper ac power must be available. The water requirement for water-cooled units is four gallons per minute. Normal office or laboratory lighting is adequate.

2-3. POWER REQUIREMENTS AND DISTRIBUTION.

Table 2-1 lists the power requirements for the MTU. See figures 8-94 through 8-117 in Volume 2 for power control and distribution diagrams.

2-4. INSTALLATION LAYOUT.

Position the MTU to allow minimum cable lengths to the computer. The maximum cable length is 300 feet. A minimum of 40 inches front clearance is required for maintenance. Air-cooled units must be far enough from obstruction to allow air circulation of 600 cubic feet per minute for basic units and 400 cubic feet per minute for add-on units. Light switches should be located near the unit so that the illumination can be reduced when checking oscilloscope traces during maintenance.

TABLE 2-1. POWER REQUIREMENTS

DESCRIPTION	FREQUENCY (CPS)	VOLTAGE (VAC)	PHASES	POWER (WATTS) AT START UP	POWER (WATTS) OPERATIONAL
MTU (Basic Unit)					
Tape Transports (2)	60	115	Single	2800	2400
Vacuum Motor (2)	400	115	Three	*	*
Blowers:					
Air Cooled	60	115	Single	190	180
Water Cooled	400	115	Three	675	440
Logic	400	115	Three	800	600
MTU (Add-on Unit)					
Tape Transports (2)	60	115	Single	2800	2400
Vacuum Motor (2)	400	115	Three	*	*
Blowers:					
Air Cooled	60	115	Single	125	120
Water Cooled	400	115	Three	350	295
Logic	400	115	Three	15	10

*Data not available

2-5. INSTALLATION REQUIREMENTS.

a. INSTALLATION POINTERS. - In general, the installation requirements of the MTU are dependent upon the site selected. Refer to the general installation plan for the site before installing this equipment. The MTU has four screw holes (3/8-16 UNC) which are located at the top corner of each unit and are accessible only when the top is removed. These screw holes are used for eyebolt insertion, during installation, to facilitate lifting.

b. OUTLINE DRAWINGS. - Figures 2-1 through 2-4 show the MTU outline dimensions. Review these drawings carefully before attempting any final installation of the equipment. Make sure the installation area allows sufficient room for maintenance and operation.

c. INTERCONNECTION DIAGRAM. - Figure 2-5 shows the functional relationship between the MTU and the computer, the intercabinet connections, and the primary power connections. Since cables associated with a computer are referenced to the computer, the input cable provides inputs to the computer and the output cable provides outputs from the computer.

d. CABLE ASSEMBLY. - The MTU is supplied with the necessary intercabinet cables. When the necessary computer cable assemblies are fabricated at the installation, they must be checked thoroughly to ensure they are correct. Figures 2-1 through 2-4 show the connector locations on the Magnetic Tape Unit; table 2-2 lists the functions of the cables associated with each major chassis connector.

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STEP 5. Check assembly for chips, dents, scratches, broken indicators, and missing parts.

STEP 6. Ensure that all items listed in table 1-3 are included in shipment.

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Blowers:					
Air Cooled	60	115	Single	190	180
Water Cooled	400	115	Three	675	440
Logic	400	115	Three	800	600
MTU (Add-on Unit)					
Tape Transports (2)	60	115	Single	2800	2400
Blowers:					
Air Cooled	60	115	Single	125	120
Water Cooled	400	115	Three	350	295
Logic	400	115	Three	15	10

2-5. INSTALLATION REQUIREMENTS.

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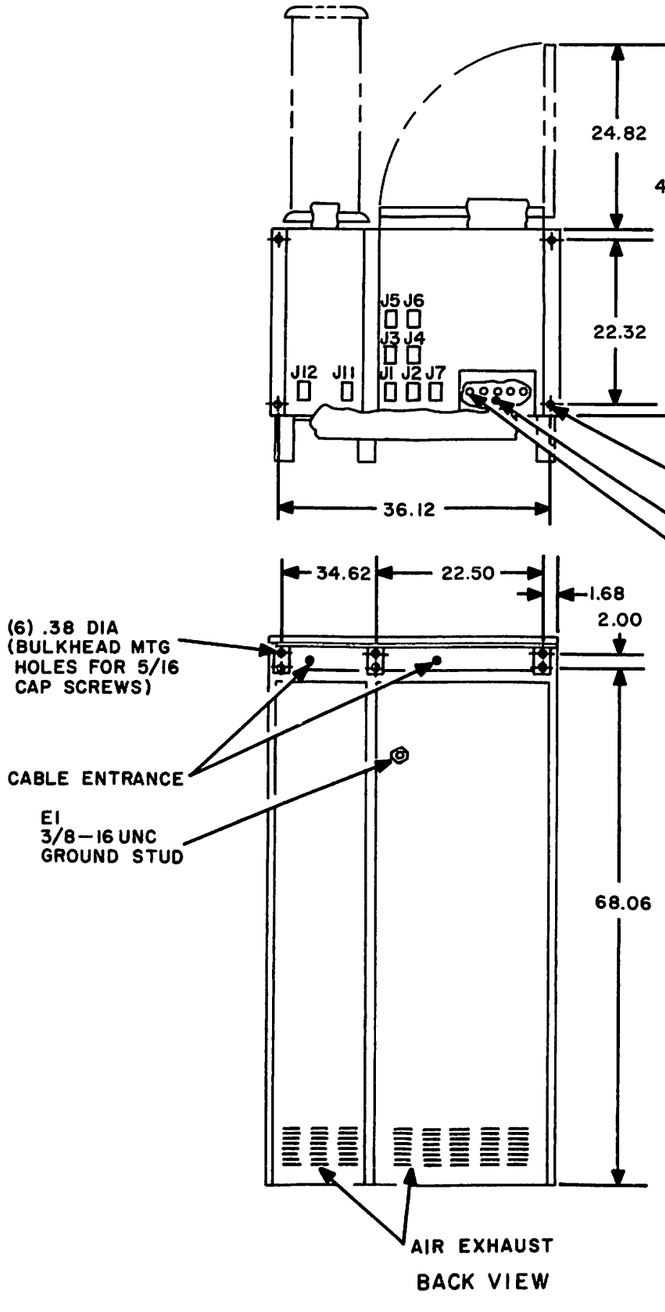
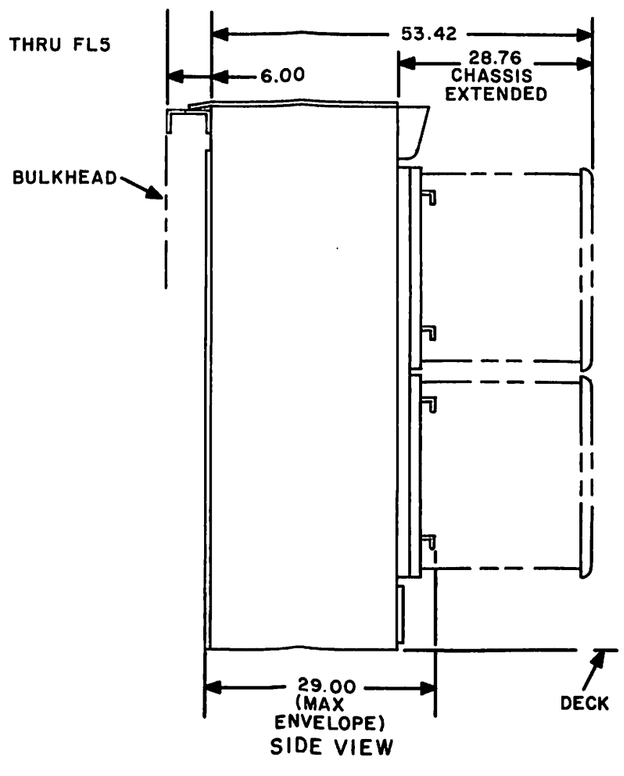
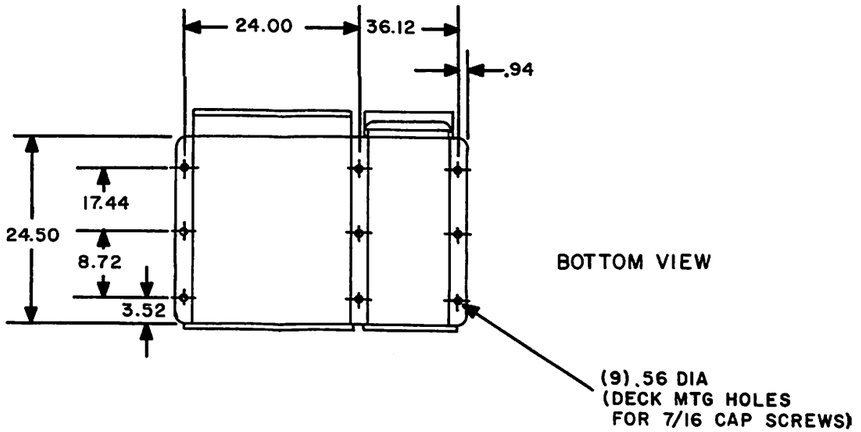






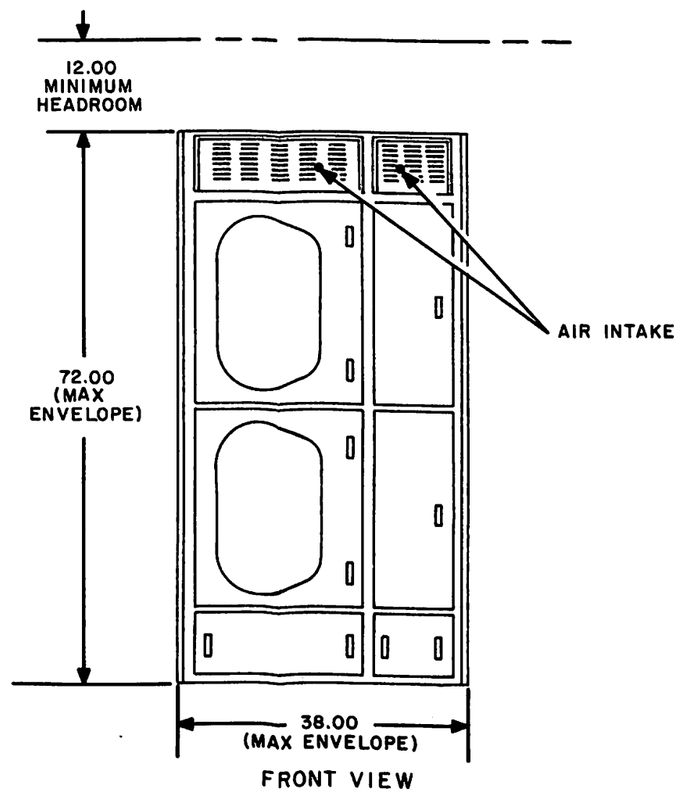


Figure 2-1. Dimensional Data for Basic Magnetic Tape Unit (Air-Cooled)

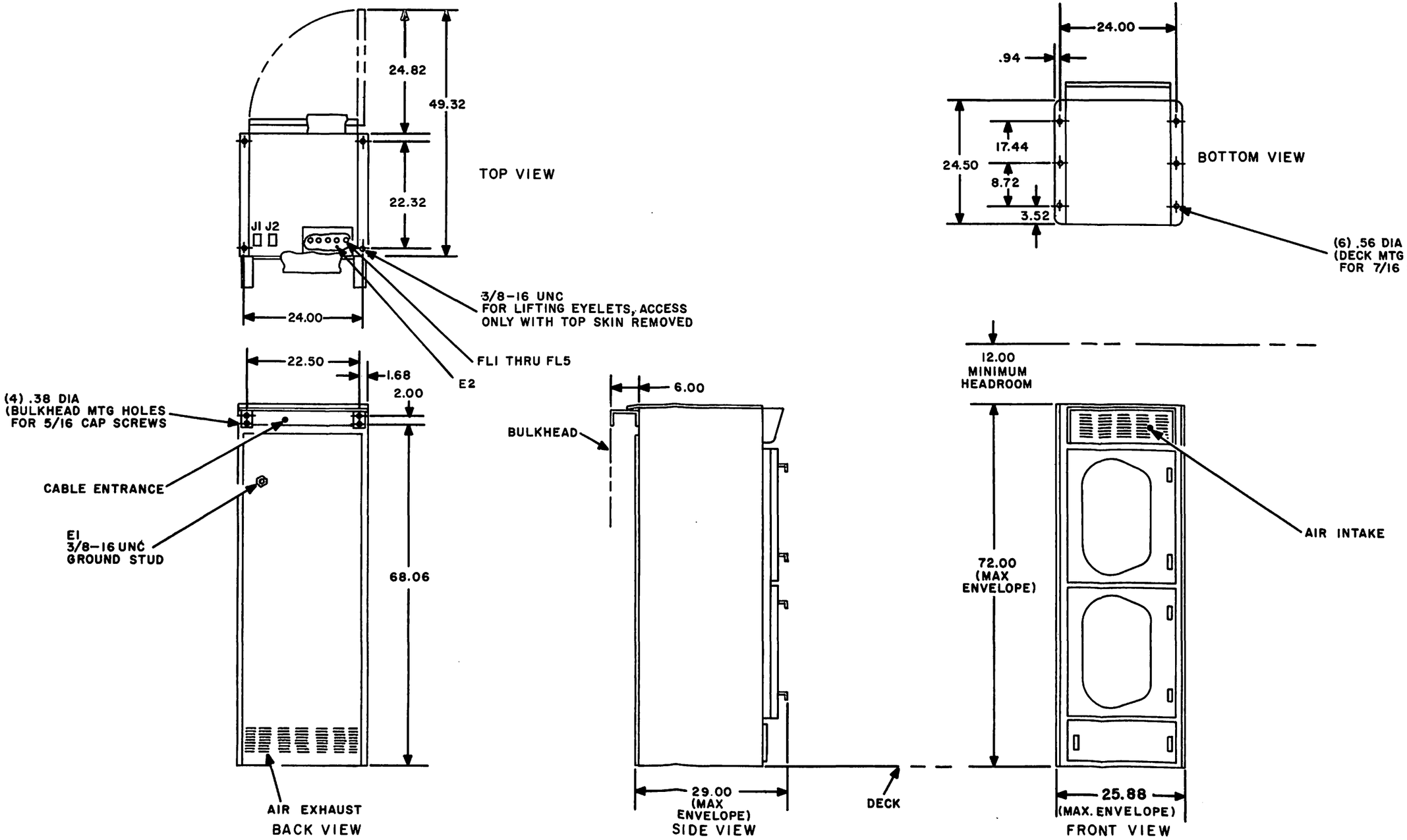


Figure 2-2. Dimensional Data for Add-on Magnetic Tape Unit (Air-Cooled)

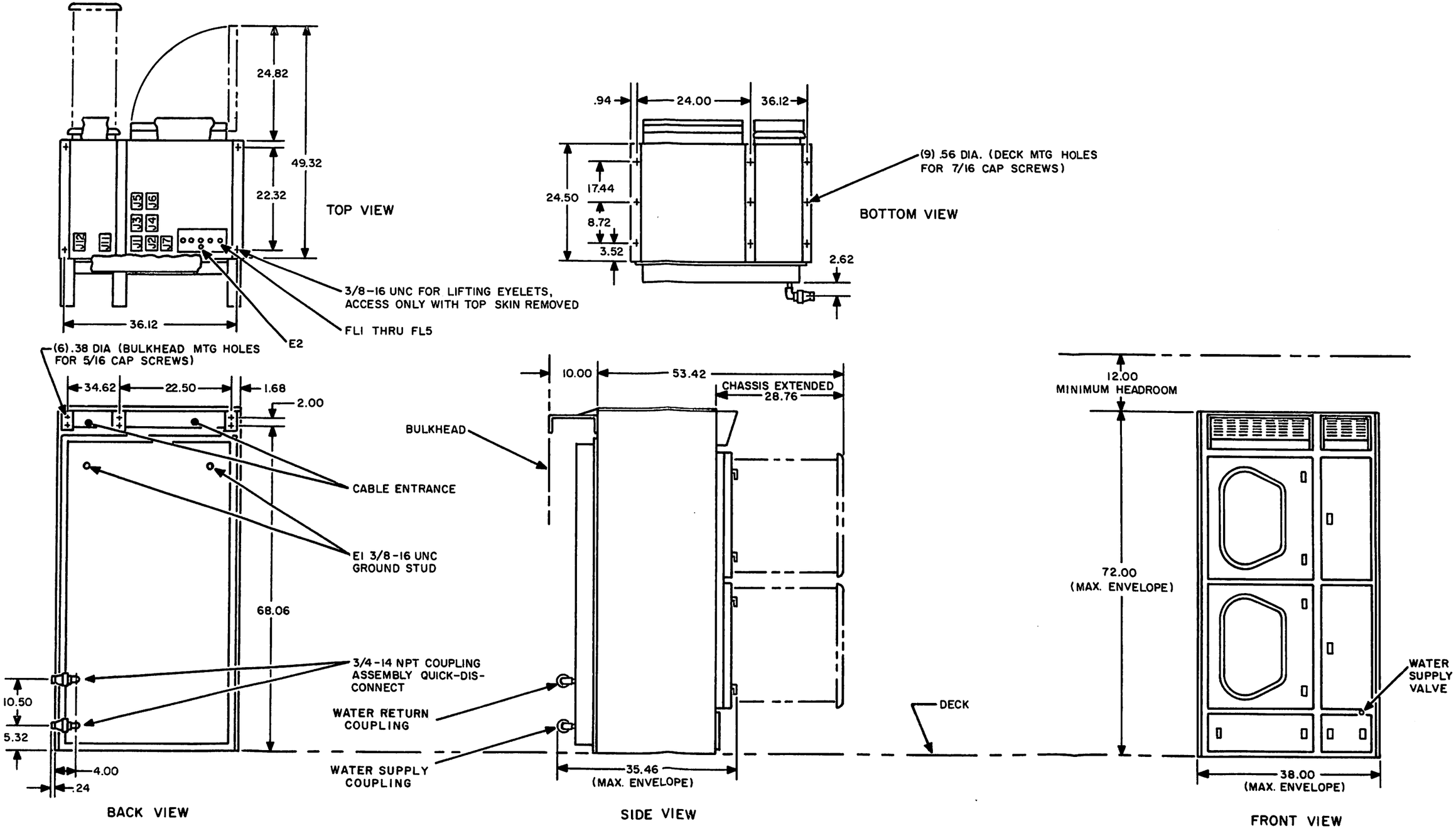


Figure 2-3. Dimensional Data for Basic Magnetic Tape Unit (Water-Cooled)

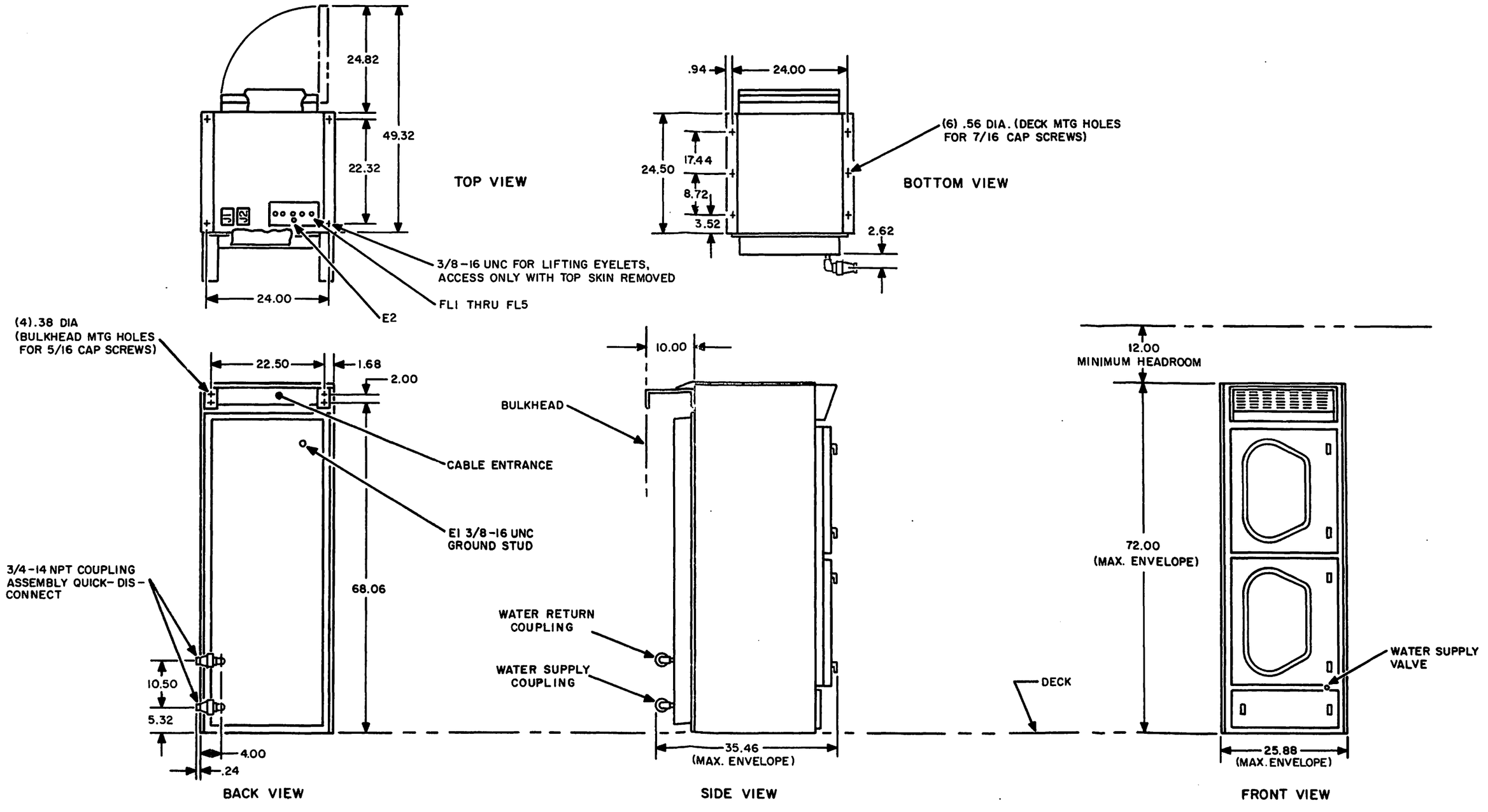
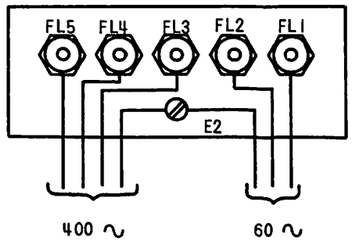


Figure 2-4. Dimensional Data for Add-On Magnetic Tape Unit (Water-Cooled)



TYPICAL POWER HOOK-UP
FOR MAGNETIC TAPE UNIT

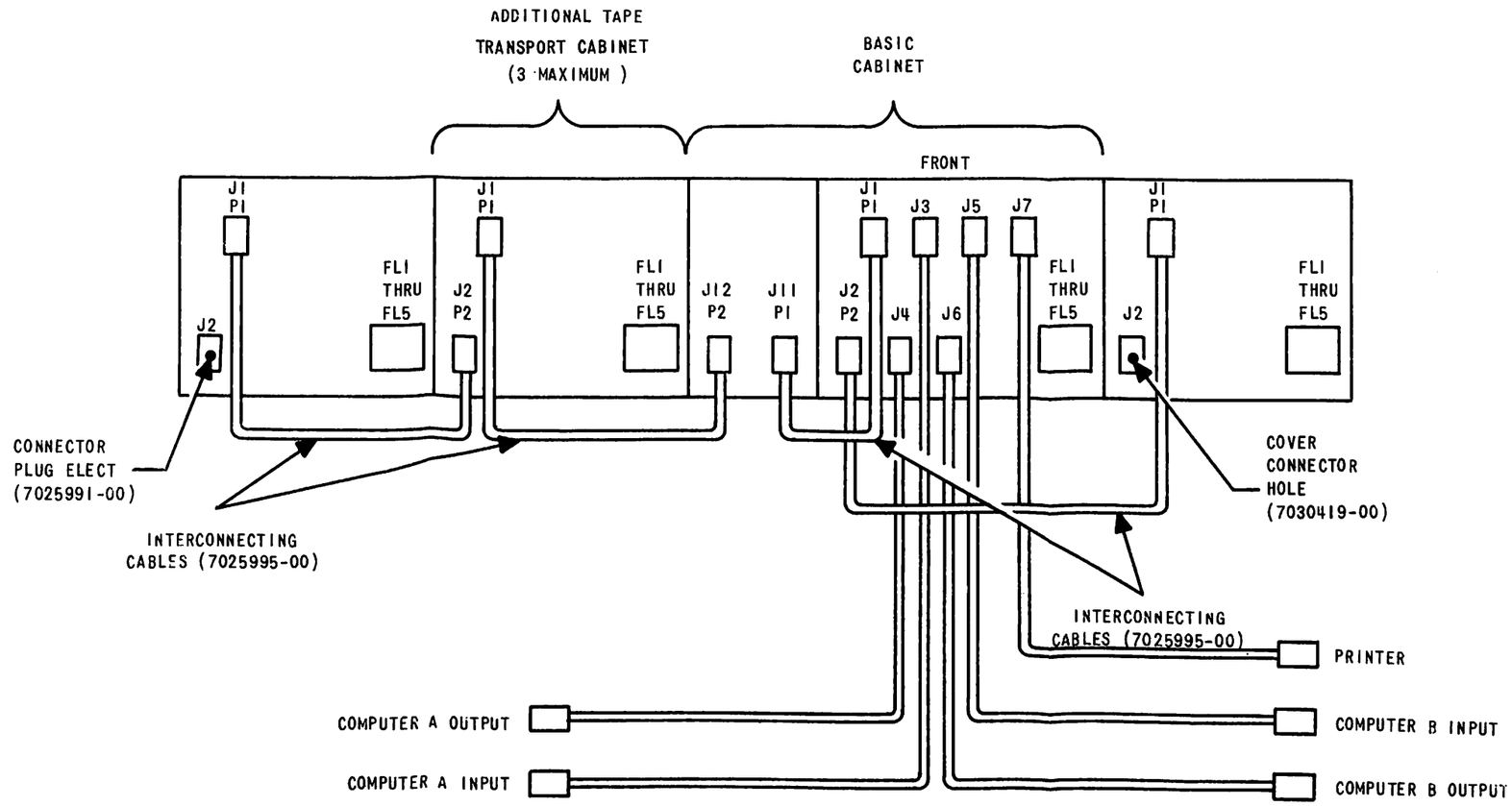


Figure 2-5. Interconnection Diagram

TABLE 2-2. CABLE FUNCTIONS

UNIT	ORIGIN	FUNCTION	DESTINATION
BASIC	J1	Intercabinet - Power, data, and control	J11
	J2	Intercabinet - Power, data, and control	J1 of left add-on unit
	J3	Signal Input	Computer A
	J4	Signal Output	Computer A
	J5	Signal Input	Computer B
	J6	Signal Output	Computer B
	J7	Signal	Printer
	J12	Intercabinet - Power, data,and control	J1 of right add-on unit
ADD-ON	J1	Intercabinet - Power, data, and control	J11 or J12 of basic unit or J2 of another add-on unit
	J2*	Intercabinet - Power, data, and control	J1 of another add-on unit

* A dummy connector must be installed in J2 of the extreme right-hand add-on unit (see figure 2-5.)

Table 2-3 lists the pin designations for computer connections. The data in the table will be an aid during checkout, since it specifies the signal associated with each pin. Continuity within each cable can be checked with a multimeter or, if available, a cable checker.

2-6. EQUIPMENT INSPECTION AND ADJUSTMENTS.

a. WATER COOLING SYSTEM. - When the Magnetic Tape Unit has been installed in the selected area, connect the cooling system to the installation water source using the quick-disconnect couplings. Both parts of the couplings are supplied with the equipment.

After the water connections have been made, turn on the necessary valves to allow the water to circulate through the cooling system. Thoroughly inspect the cooling system to ensure that there are no leaks or bad connections and that water can flow freely through the cooling system. The control handles for the cabinet cooling system are accessible on the lower front of the unit.

b. AC VOLTAGE CHECKS. - To check the MTU ac voltages, proceed as follows.

WARNING

Turn off the local power source before making any power connections.

STEP 1. Make power and ground connections listed in table 2-4. (Filters are located at top rear of tape transport section; see figures 2-1 through 2-4.)

STEP 2. Set all switches listed in table 2-5 to OFF.

TABLE 2-3. COMPUTER CABLE CONNECTOR PIN DESIGNATIONS*

PIN NUMBER	INPUT PIN**	OUTPUT PIN**
1	Input Data Request	Output Acknowledge
2	Input Acknowledge	Output Data Request
3	Interrupt	External Function
4	Spare	Spare
5	Data Bit 2^{32}	Data Bit 2^{32}
6	Data Bit 2^{33}	Data Bit 2^{33}
7	Data Bit 2^{34}	Data Bit 2^{34}
8	Data Bit 2^{35}	Data Bit 2^{35}
9	Data Bit 2^{0}	Data Bit 2^{0}
10	Data Bit 2^{1}	Data Bit 2^{1}
11	Input Data Request (r)	Output Acknowledge (r)
12	Input Acknowledge (r)	Output Data Request (r)
13	Interrupt (r)	External Function (r)
14	Spare	Spare
15	Data Bit 2^{32} (r)	Data Bit 2^{32} (r)
16	Data Bit 2^{33} (r)	Data Bit 2^{33} (r)
17	Data Bit 2^{34} (r)	Data Bit 2^{34} (r)
18	Data Bit 2^{35} (r)	Data Bit 2^{35} (r)
19	Data Bit 2^{0} (r)	Data Bit 2^{0} (r)
20	Data Bit 2^{1} (r)	Data Bit 2^{1} (r)
21	Not Used	Not Used
22	Data Bit 2^{2}	Data Bit 2^{2}
23	Data Bit 2^{3}	Data Bit 2^{3}
24	Data Bit 2^{4}	Data Bit 2^{4}
25	Data Bit 2^{5}	Data Bit 2^{5}
26	Data Bit 2^{6}	Data Bit 2^{6}
27	Data Bit 2^{7}	Data Bit 2^{7}
28	Data Bit 2^{8}	Data Bit 2^{8}
29	Data Bit 2^{9}	Data Bit 2^{9}
30	Data Bit 2^{10}	Data Bit 2^{10}
31	Data Bit 2^{11}	Data Bit 2^{11}
32	Data Bit 2^{12}	Data Bit 2^{12}
33	Data Bit 2^{2} (r)	Data Bit 2^{2} (r)
34	Data Bit 2^{3} (r)	Data Bit 2^{3} (r)
35	Data Bit 2^{4} (r)	Data Bit 2^{4} (r)
36	Data Bit 2^{5} (r)	Data Bit 2^{5} (r)
37	Data Bit 2^{6} (r)	Data Bit 2^{6} (r)
38	Data Bit 2^{7} (r)	Data Bit 2^{7} (r)
39	Data Bit 2^{8} (r)	Data Bit 2^{8} (r)
40	Data Bit 2^{9} (r)	Data Bit 2^{9} (r)
41	Data Bit 2^{10} (r)	Data Bit 2^{10} (r)
42	Data Bit 2^{11} (r)	Data Bit 2^{11} (r)
43	Data Bit 2^{12} (r)	Data Bit 2^{12} (r)
44	Not Used	Not Used
45	Ground (Shield)	Ground (Shield)
46	Not Used	Not Used
47	Data Bit 2^{13}	Data Bit 2^{13}
48	Data Bit 2^{14}	Data Bit 2^{14}
49	Data Bit 2^{15}	Data Bit 2^{15}

* This is the standard computer cable and is utilized for all computer applications regardless of the number of data lines required.

**Note (r) denotes ground return of the twisted pair.

TABLE 2-3. COMPUTER CABLE CONNECTOR PIN DESIGNATIONS* (CONT.)

PIN NUMBER	INPUT PIN**	OUTPUT PIN**
50	Data Bit 2^{16}	Data Bit 2^{16}
51	Data Bit 2^{17}	Data Bit 2^{17}
52	Data Bit 2^{18}	Data Bit 2^{18}
53	Data Bit 2^{19}	Data Bit 2^{19}
54	Data Bit 2^{20}	Data Bit 2^{20}
55	Data Bit 2^{21}	Data Bit 2^{21}
56	Data Bit 2^{22}	Data Bit 2^{22}
57	Data Bit 2^{23}	Data Bit 2^{23}
58	Data Bit 2^{13} (r)	Data Bit 2^{13} (r)
59	Data Bit 2^{14} (r)	Data Bit 2^{14} (r)
60	Data Bit 2^{15} (r)	Data Bit 2^{15} (r)
61	Data Bit 2^{16} (r)	Data Bit 2^{16} (r)
62	Data Bit 2^{17} (r)	Data Bit 2^{17} (r)
63	Data Bit 2^{18} (r)	Data Bit 2^{18} (r)
64	Data Bit 2^{19} (r)	Data Bit 2^{19} (r)
65	Data Bit 2^{20} (r)	Data Bit 2^{20} (r)
66	Data Bit 2^{21} (r)	Data Bit 2^{21} (r)
67	Data Bit 2^{22} (r)	Data Bit 2^{22} (r)
68	Data Bit 2^{23} (r)	Data Bit 2^{23} (r)
69	Ground (Shield)	Ground (Shield)
70	Data Bit 2^{24}	Data Bit 2^{24}
71	Data Bit 2^{25}	Data Bit 2^{25}
72	Data Bit 2^{26}	Data Bit 2^{26}
73	Data Bit 2^{27}	Data Bit 2^{27}
74	Data Bit 2^{28}	Data Bit 2^{28}
75	Data Bit 2^{29}	Data Bit 2^{29}
76	Data Bit 2^{30}	Data Bit 2^{30}
77	Data Bit 2^{31}	Data Bit 2^{31}
78	Not Used	Not Used
79	Not Used	Not Used
80	Data Bit 2^{24} (r)	Data Bit 2^{24} (r)
81	Data Bit 2^{25} (r)	Data Bit 2^{25} (r)
82	Data Bit 2^{26} (r)	Data Bit 2^{26} (r)
83	Data Bit 2^{27} (r)	Data Bit 2^{27} (r)
84	Data Bit 2^{28} (r)	Data Bit 2^{28} (r)
85	Data Bit 2^{29} (r)	Data Bit 2^{29} (r)
86	Data Bit 2^{30} (r)	Data Bit 2^{30} (r)
87	Data Bit 2^{31} (r)	Data Bit 2^{31} (r)
88	Not Used	Not Used
89	Not Used	Not Used
90	Not Used	Not Used

* This is the standard computer cable and is utilized for all computer applications regardless of the number of data lines required.

** Note (r) denotes ground return of the twisted pair.

STEP 3. Turn on local power source.

STEP 4. Verify line-to-line and line-to-ground voltages listed in table 2-4 using a multimeter. (See the appropriate filter orientation diagram in figure 2-5.)

STEP 5. Verify proper phase relationship at FL3, FL4, and FL5 using the oscilloscope.

STEP 6. Set primary power control panel POWER switch (see figure 3-1) to ON. Blowers should start and the LOGIC and BLOWER indicators should light.

STEP 7. Set tape handler control panel POWER switch (see figures 3-2 and 3-3) to ON. BLOWER ON indicator should light.

STEP 8. Check fuses listed in table 2-4. Fuses are located on interior of tape transport section above tape transport 1; see power control unit A2, figure 5-18. Replace all glowing fuses. Note that although number of fuses may vary, the location of fuses in add-on units is same as in basic units.

STEP 9. Check blower fuses listed in tables 2-6 and 2-7 (for location see A2 on figure 5-18). Replace all glowing fuses.

CAUTION

Do not turn MAN-OFF-AUTO switches on tape handler 1 and 2 to MAN/AUTO positions simultaneously. The current surge of both vacuum motors will cause circuit breaker (A3A3/CB1) to trip. Allow handler motor 1 to come to full speed (approximately 5 seconds) prior to turning handler 2 switch to MAN/AUTO.

STEP 10. Set each MAN-OFF-AUTO switch, located on tape transport control panels (figure 3-2), to MAN. RUNNING TIME meter(s) should be energized.

STEP 11. Check transport fuses listed in tables 2-6 and 2-7. Replace all glowing fuses.

c. DC VOLTAGE CHECKS. - To check the MTU dc voltages proceed as follows.

STEP 1. Using accurate (±0.1%) voltohmmeter, check test points listed in table 2-8.

STEP 2. If deviations from tolerances in table 2-8 are uniform, readjust regulated 400-cycle voltage.

STEP 3. Check ripple at test points listed in table 2-8 using oscilloscope.

d. CONTROL CIRCUIT CHECKS AND ADJUSTMENTS. - Perform the control circuit checks when the preceding installation procedures have been completed. Refer to the troubleshooting procedure in paragraph 5-3 for the control circuit checkout procedures.

TABLE 2-3. COMPUTER CABLE CONNECTOR PIN DESIGNATIONS* (CONT.)

PIN NUMBER	INPUT PIN**	OUTPUT PIN**
50	Data Bit 2^{16}	Data Bit 2^{16}
51	Data Bit 2^{17}	Data Bit 2^{17}
52	Data Bit 2^{18}	Data Bit 2^{18}
53	Data Bit 2^{19}	Data Bit 2^{19}
54	Data Bit 2^{20}	Data Bit 2^{20}
55	Data Bit 2^{21}	Data Bit 2^{21}
56	Data Bit 2^{22}	Data Bit 2^{22}
57	Data Bit 2^{23}	Data Bit 2^{23}
58	Data Bit 2^{13} (r)	Data Bit 2^{13} (r)
59	Data Bit 2^{14} (r)	Data Bit 2^{14} (r)
60	Data Bit 2^{15} (r)	Data Bit 2^{15} (r)
61	Data Bit 2^{16} (r)	Data Bit 2^{16} (r)
62	Data Bit 2^{17} (r)	Data Bit 2^{17} (r)
63	Data Bit 2^{18} (r)	Data Bit 2^{18} (r)
64	Data Bit 2^{19} (r)	Data Bit 2^{19} (r)
65	Data Bit 2^{20} (r)	Data Bit 2^{20} (r)
66	Data Bit 2^{21} (r)	Data Bit 2^{21} (r)
67	Data Bit 2^{22} (r)	Data Bit 2^{22} (r)
68	Data Bit 2^{23} (r)	Data Bit 2^{23} (r)
69	Ground (Shield)	Ground (Shield)
70	Data Bit 2^{24}	Data Bit 2^{24}
71	Data Bit 2^{25}	Data Bit 2^{25}
72	Data Bit 2^{26}	Data Bit 2^{26}
73	Data Bit 2^{27}	Data Bit 2^{27}
74	Data Bit 2^{28}	Data Bit 2^{28}
75	Data Bit 2^{29}	Data Bit 2^{29}
76	Data Bit 2^{30}	Data Bit 2^{30}
77	Data Bit 2^{31}	Data Bit 2^{31}
78	Not Used	Not Used
79	Not Used	Not Used
80	Data Bit 2^{24} (r)	Data Bit 2^{24} (r)
81	Data Bit 2^{25} (r)	Data Bit 2^{25} (r)
82	Data Bit 2^{26} (r)	Data Bit 2^{26} (r)
83	Data Bit 2^{27} (r)	Data Bit 2^{27} (r)
84	Data Bit 2^{28} (r)	Data Bit 2^{28} (r)
85	Data Bit 2^{29} (r)	Data Bit 2^{29} (r)
86	Data Bit 2^{30} (r)	Data Bit 2^{30} (r)
87	Data Bit 2^{31} (r)	Data Bit 2^{31} (r)
88	Not Used	Not Used
89	Not Used	Not Used
90	Not Used	Not Used

* This is the standard computer cable and is utilized for all computer applications regardless of the number of data lines required.

** Note (r) denotes ground return of the twisted pair.

STEP 3. Turn on local power source.

STEP 4. Verify line-to-line and line-to-ground voltages listed in table 2-4 using a multimeter. (See the appropriate filter orientation diagram in figure 2-5.)

STEP 5. Verify proper phase relationship at FL3, FL4, and FL5 using the oscilloscope.

STEP 6. Set primary power control panel POWER switch (see figure 3-1) to ON. Blowers should start and the LOGIC and BLOWER indicators should light.

STEP 7. Set tape handler control panel POWER switch (see figures 3-2 and 3-3) to ON. BLOWER ON indicator should light.

STEP 8. Check fuses listed in table 2-4. Fuses are located on interior of tape transport section above tape transport 1; see power control unit A2, figure 5-18. Replace all glowing fuses. Note that although number of fuses may vary, the location of fuses in add-on units is same as in basic units.

STEP 9. Check blower fuses listed in tables 2-6 and 2-7 (for location see A2 on figure 5-18). Replace all glowing fuses.

STEP 10. Set each MAN-OFF-AUTO switch, located on tape transport control panels (figure 3-2), to MAN. RUNNING TIME meter(s) should be energized.

STEP 11. Check transport fuses listed in tables 2-6 and 2-7. Replace all glowing fuses.

c. DC VOLTAGE CHECKS. - To check the MTU dc voltages proceed as follows.

STEP 1. Using accurate (±0.1%) voltohmmeter, check test points listed in table 2-8.

STEP 2. If deviations from tolerances in table 2-8 are uniform, readjust regulated 400-cycle voltage.

STEP 3. Check ripple at test points listed in table 2-8 using oscilloscope.

d. CONTROL CIRCUIT CHECKS AND ADJUSTMENTS. - Perform the control circuit checks when the preceding installation procedures have been completed. Refer to the troubleshooting procedure in paragraph 5-3 for the control circuit checkout procedures.

The adjustments are divided into two groups: mechanical adjustments for the tape transports and electrical adjustments for the control circuits. The Potter tape handler manual describes the adjustments pertaining to the tape transports. Paragraph 5-2d of this manual describes the control circuit adjustments. Check the following control circuit adjustments to ensure proper operation of the MTU.

1) Voltage regulator adjustments

2) Time delay adjustments

3) Read amplifier adjustments

The adjustments are divided into two groups: mechanical adjustments for the tape transports and electrical adjustments for the control circuits. The Potter tape handler manual describes the adjustments pertaining to the tape transports. Paragraph 5-2d of this manual describes the control circuit adjustments. Check the following control circuit adjustments to ensure proper operation of the MTU.

1) Voltage regulator adjustments

2) Time delay adjustments

3) Read amplifier adjustments

TABLE 2-4. AC POWER DATA

TERMINAL CONNECTIONS	CHARACTERISTICS	LINE-TO-LINE POTENTIAL	LINE-TO-GROUND POTENTIAL	FUSING 1540 FUSE	BASIC UNIT	ADD-ON UNIT
A4FL1	60-cycle, unregulated	115 volts ±10%				
A4FL2	60-cycle, unregulated	115 volts ±10%				
A4FL3	400-cycle, phase 1, regulated	115 volts ±5%	65 volts	A2F11	10	1
A4FL4	400-cycle, phase 2, regulated	115 volts ±5%	65 volts	A2F12	10	1
A4FL5	400-cycle, phase 3, regulated	115 volts ±5%	65 volts	A2F13	10	1
A4E2	Power ground	-	-	-	-	
E1	System ground	-	-	-	-	

TABLE 2-5. POWER CONTROL SWITCHES

DESIGNATION	NOMENCLATURE	LOCATION
A11S1	POWER ON-OFF	Primary power control section (left) (A11)
A1S1	POWER ON-OFF	Tape handler control panel (right) (A1)
A1S2	HANDLER MAN-OFF-AUTO	Tape handler control panel (center) (A1)
A1S3	HANDLER MAN-OFF-AUTO	Tape handler control panel (left) (A1)

TABLE 2-6. BLOWER AND TAPE TRANSPORT FUSING FOR BASIC UNIT

FUSE	VALUE (AMPS)	PHASE	CIRCUIT FOR WATER-COOLED UNIT	CIRCUIT FOR AIR-COOLED UNIT
A2F1	15	Single	Tape Transport 1	Tape Transport 1
A2F2	15	Single	Tape Transport 1	Tape Transport 1
A2F3	15	Single	Tape Transport 2	Tape Transport 2
A2F4	15	Single	Tape Transport 2	Tape Transport 2
A2F5	1 2	Single Phase 3	Blower B3	Blowers A1B3 and A1B4
A2F6	1 2	Single Phase 3	Blower B3	Blowers A1B3 and A1B4
A2F7	1 2	Single Phase 3	Blower B1	Blowers A1B1 and A1B2
A2F8	1 2	Single Phase 2	Blower B1	Blowers A1B1 and A1B2
A2F9	1 2	Single Phase 3	Blower B5	Blowers A15B5 and A15B6
A2F10	1 2	Single Phase 2	Blower B5	Blowers A15B5 and A15B6

TABLE 2-7. BLOWER AND TAPE TRANSPORT FUSING FOR ADD-ON UNIT

FUSE	VALUE (AMPS)	PHASE	CIRCUIT FOR WATER-COOLED UNIT	CIRCUIT FOR AIR-COOLED UNIT
A2F1	15	Single	Tape Transport 1	Tape Transport 1
A2F2	15	Single	Tape Transport 1	Tape Transport 1
A2F3	15	Single	Tape Transport 2	Tape Transport 2
A2F4	15	Single	Tape Transport 2	Tape Transport 2
A2F5	1 2	Single Phase 3	Blower B3	Blowers A1B3 and A1B4
A2F6	1 2	Single Phase 2	Blower B3	Blowers A1B3 and A1B4
A2F7	1 2	Single Phase 3	Blower B1	Blowers A1B1 and A1B2
A2F8	1 2	Single Phase 2	Blower B1	Blowers A1B1 and A1B2

TABLE 2-8. DC POWER DATA

TEST POINT CHASSIS A13A1	LINE-TO-GROUND POTENTIAL	MAXIMUM RIPPLE (VOLTS)	FUSE	PHASE	VALUE (AMPS)
TB1-B33	-26.5 vdc ±2.7v	3.0	A13A1F1*	-	6
TB1-C31	±26.5 vdc ±2.7v	3.0	A13A1F2*	-	6
TB1-D33	+15 vdc ±0.8v	0.2	PS1F7**	1	2
			PS1F8**	2	2
			PS1F9**	3	2
TB1-E33	-15 vdc ±0.8v	0.2	PS1F4**	1	3
			PS1F5**	2	3
			PS1F6**	3	3
TB1-F33	-4.5 vdc ±0.1v	0.5	PS1F1**	1	1.5
			PS1F2**	2	1.5
			PS1F3**	3	1.5
TB1-G33	Ground	-	-	-	-

* 26.5-volt fuses are located on chassis A13A1 (see figure 5-6).
** DC power supply PS1 is fused on the 3-phase primary inputs to each dc supply transformer with non-indicating type fuses. Fuses are physically located in the dc power supply drawer located in the bottom of the magnetic tape control section (see figure 5-13).

4) Read detector adjustments

5) Read deskewing adjustments

6) Write deskewing adjustments

7) Read reverse deskewing adjustments

8) Handler start-stop checks

2-7. GROUNDING. - A dc level system is utilized for connecting the MTU to the computer. Any difference in ground potential between these equipments has a direct effect on the discrimination between a logical one and a logical zero on the transmission and control lines. High impedance of the primary power ground lines causes an increase in the rise, fall, and delay times of the data control pulses to a degree sufficient to cause loss of information.

The computer is the central point or hub of the data processing system, with peripheral devices communicating directly with the computer. To provide the shortest possible interconnecting ground scheme, keep the system configuration within the smallest allowable floor space. A quasi-ground plane should be used with the computer as shown in Figure 2-6. The common tie point or central system ground is E1 located on the back of the computer. Individual ground straps from each peripheral equipment are terminated at this point.

Complete the following steps to properly install the quasi-ground plane.

STEP 1. Install and secure all equipment of system in such a manner as to afford minimum of one megohm of dc resistance between any cabinet and primary power ground prior to installation of ground straps, power lines, or conduits, or input-output cabling.

STEP 2. Connect each unit individually to central system ground (E1) using interconnecting ground straps that provide maximum surface area per cross sectional area, i.e., for given cross sectional area, flat strip is preferable to round wire. Interconnected system must have minimum dc resistance of one megohm from central system ground (E1) to primary power ground.

STEP 3. Connect 400 cycle neutral (E2) to single central ground (E1).

STEP 4. Connect 60 cycle ground (E3) to single central ground (E1).

STEP 5. Connect motor generator case to 60 cycle ground (E3).

STEP 6. Be sure that shields on I/O cables are adequately grounded to equipment cabinets at both ends.

2-8. PREPARATION FOR RESHIPMENT.

No unusual precautions are required in preparing this equipment for reshipment beyond the careful handling appropriate for complicated equipment.

The unit should be shipped completely assembled. Ensure that the equipment listed in table 1-3 is included in the shipment (equipment is determined by the type of tape unit being reshipped).

Advise the packaging and packing facility of the type of equipment being shipped and whether to prepare it for domestic shipment and immediate use, domestic shipment and storage, or overseas shipment. Mark the box containing the technical manuals, "TECHNICAL MANUALS INSIDE."

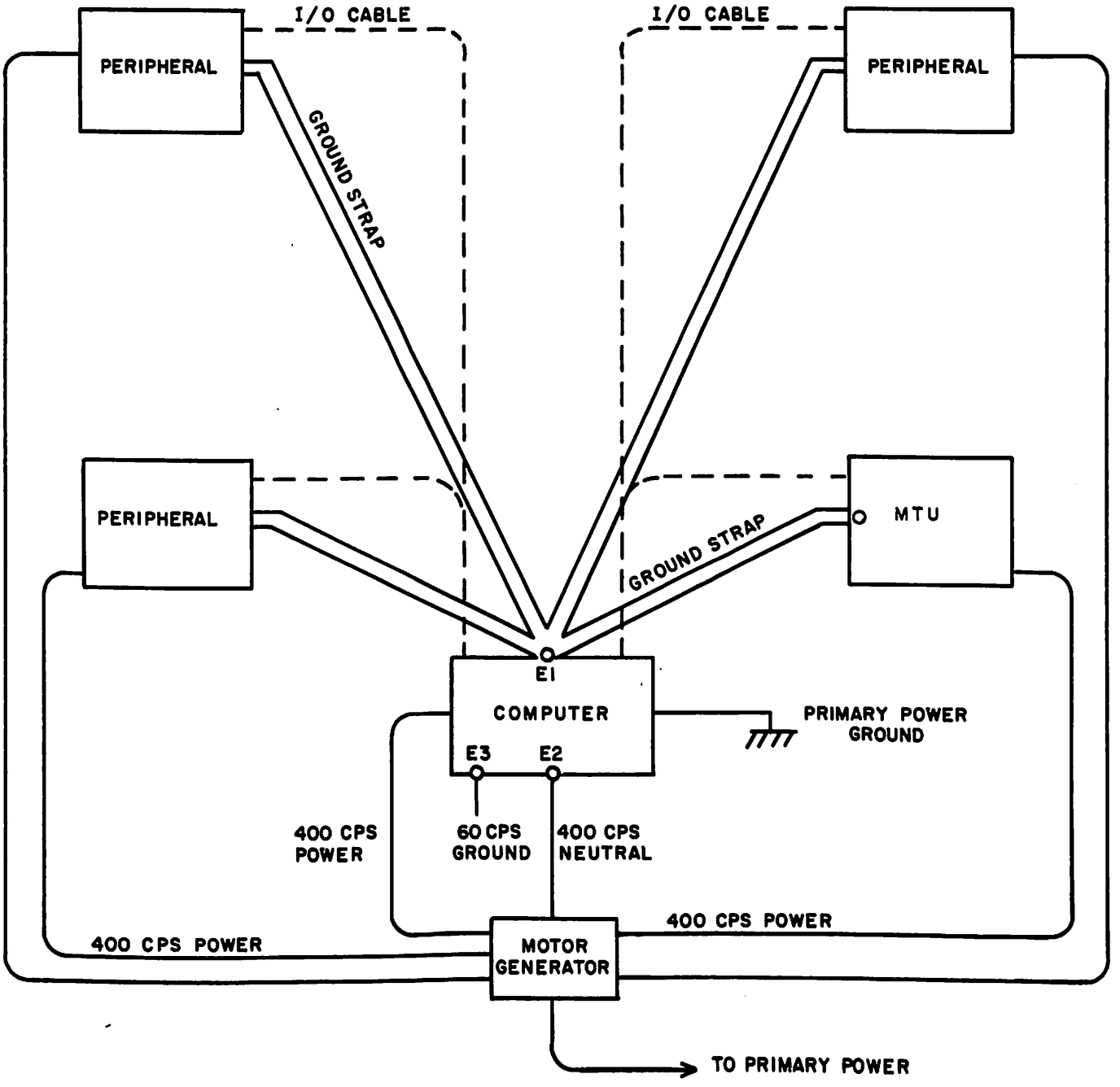


Figure 2-6. Quasi-ground Plane System

SECTION 3

OPERATION

3-1. FUNCTIONAL OPERATION.

The function of the MTU is to provide auxiliary data storage for a computer. Under computer control, the MTU receives computer-sized (36-, 30-, 24-, or 18-bit binary data words, disassembles them into 6-bit subwords, generates a parity bit for each subword, and records the subwords in 7-bit frames on one-half inch tape. When requested by the computer, the MTU retrieves data from tape, checks and deletes parity, reassembles the data into computer-sized data words, and transmits it to the computer.

The computer controls the MTU operations through an external function word. The operation code portion of the external function word commands the MTU to perform one of 28 operations which consist, basically, of read, write, search, space file, and rewind with certain operations supplemented by format (modulus, character, and parity) and density selections. The densities available are 200, 556, and 800 bits-per-inch.

For read operations, a selected tape transport moves the tape at the normal speed of 120 inches-per-second. The MTU reads and assembles the requested data, places the data on the computer input lines, and sets an input data request (IDR) line. The computer senses the IDR, samples the data, and returns an input acknowledge signal to the MTU.

When a write operation is sensed, the MTU sends an output data request (ODR) indicating it is ready to receive and record data. The computer places the data on its output lines and sets an output acknowledge line. The MTU senses the output acknowledge, samples the data, and removes the ODR. The MTU then disassembles the data, generates parity, and records the data on tape.

When a search operation is sensed, the MTU sends an ODR to the computer. Sensing the ODR, the computer places the search key on its output lines and sets an output acknowledge line. The MTU senses the output acknowledge, accepts the search key, and assembles the first word of each record. If a find occurs, the MTU performs a normal read of the find record and transfers it to the computer. If no find occurs, the status word notifies the computer when the search is ended.

In a space file operation the MTU moves the tape until it detects a tape mark and then stops it in the interrecord gap following the tape mark.

A rewind operation results in tape movement in a reverse direction at high speed (240 inches-per-second) until approximately 100 feet from load point. The tape speed then reduces to normal speed (120 inches-per-second) and stops at the load point.

For maintenance and/or testing purposes the MTU can be operated off-line. External function commands are simulated manually at the magnetic tape control section maintenance and control panels. Direct communication with a high-speed printer is also available in off-line operation.

Section 4 contains detailed descriptions of the MTU operations.

3-2. OPERATING PROCEDURES.

a. DESCRIPTION OF CONTROLS AND INDICATORS. - Each basic MTU contains a primary power control panel, a tape handler control panel, an upper maintenance and control panel, and a lower maintenance and control panel. The add-on units contain only a tape handler control panel.

The primary power control panel (see figure 3-1) is located at the top of the magnetic tape control section; the indicators and controls are described in table 3-1. The tape handler control panel (see figure 3-2) is located at the top of the tape transport section; the indicators and controls are described in table 3-2. The upper and lower portions of the upper maintenance and control panel (see figures 3-3 and 3-4, respectively) are located in the magnetic tape control section directly beneath the primary power control panel; the indicators and controls are described in table 3-3. The lower maintenance and control panel (see figure 3-5) is located directly beneath the upper maintenance and control panel; the indicators and controls are described in table 3-4.

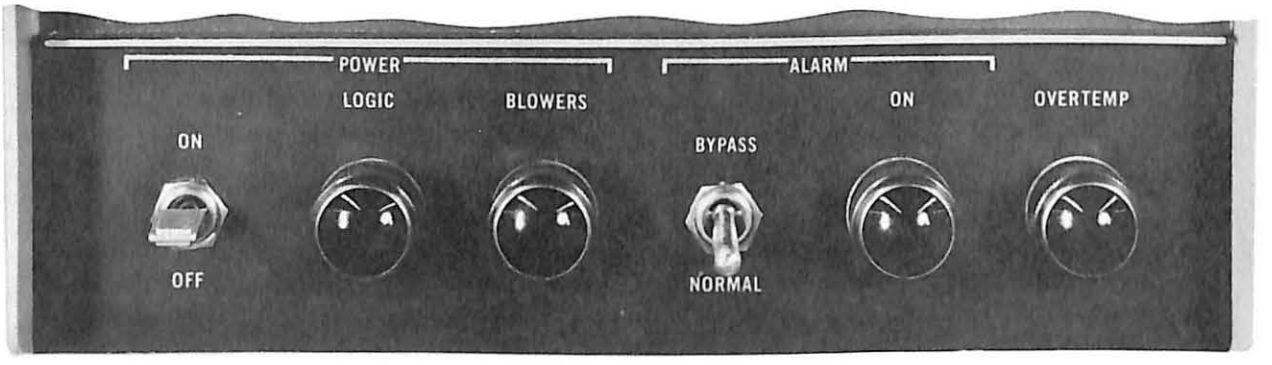


Figure 3-1. Primary Power Control Panel

TABLE 3-1. PRIMARY POWER CONTROL PANEL INDICATORS AND CONTROLS

NOMENCLATURE	SWITCH OR INDICATOR	FUNCTION
POWER ON-OFF	Three-position, momentary contact, toggle switch	ON: Sets relays which apply primary power to power supplies, blowers, and handler POWER switch (located on tape handler control panel). These relays also furnish enabling power to relays which supply 60-cycle power to the transports. OFF: Removes all power from MTU.
LOGIC	Indicator (green)	Lights when primary power is applied to logic power supply.

TABLE 3-1. PRIMARY POWER CONTROL PANEL INDICATORS AND CONTROLS (CONT.)

NOMENCLATURE	SWITCH OR INDICATOR	FUNCTION
BLOWERS	Indicator (green)	Lights when primary power is applied to blower circuits in magnetic tape control section.
ALARM BYPASS-NORMAL	Two-position toggle switch	BYPASS: Disables the alarm horn if overtemp alarm sounds. NORMAL: Enables overtemp alarm horn. Should be in NORMAL position when no overtemp condition exists.
ON	Indicator (red)	Lights when BYPASS-NORMAL switch is in BYPASS position.
OVERTEMP	Indicator (red)	Lights when cabinet temperatures exceeds 46°C (115°F).

TABLE 3-2. TAPE HANDLER CONTROL PANEL INDICATORS AND CONTROLS

NOMENCLATURE	SWITCH OR INDICATOR	FUNCTION
POWER ON-OFF	Three-position, nomentary contact, toggle switch	ON: Applies primary power to MAN-OFF-AUTO switches, energizes a relay that enables transport selection relays, and applies power to blowers. OFF: Removes all transport enabling power from relays, the MAN-OFF-AUTO switches, and the blowers.
BLOWER ON	Indicator (green)	Lights when primary power is applied to blower circuits in tape transport section. Indicator remains lighted, regardless of overtemp condition, until primary power is removed.
OVER TEMP	Indicator (red)	Lights when tape transport section temperature exceeds 46°C (115°F).

TABLE 3-2. TAPE HANDLER CONTROL PANEL INDICATORS AND CONTROLS (CONT.)

NOMENCLATURE	SWITCH OR INDICATOR	FUNCTION
HANDLER 1 ADDRESS 1 - 16	Sixteen-position rotary switch	Selects address to which associated transport will respond when it receives a select command. When more than one handler ADDRESS switch in a system is set to the same address, the one having its MAN-OFF-AUTO rotary switch in the AUTO position will be selected, otherwise the one on the leftmost unit has priority. Within the transports in one unit, transport 1 has priority.
FWD	Pushbutton indicator-switch	Lights when tape moves forward. In MAN operation, causes tape to move forward at 120 inches-per-second when depressed.
REV	Pushbutton indicator-switch	Lights when tape moves backward. In MAN operation, causes tape to move backward at 120 inches-per-second when depressed.
REWIND	Pushbutton indicator-switch	Lights when tape is rewinding. In MAN operation, causes tape to move backward at 240 inches-per-second when depressed. Tape slows to 120 inches-per-second during last 100 feet of rewind and stops at load point.
SELECT	Pushbutton indicator-switch	Lights when associated transport is selected. Operative in AUTO only.
WRITE ENABLE	Pushbutton indicator-switch	Permits writing on tape when operated manually. Lights when necessary conditions are satisfied and write functions are performed on associated tape. Inoperative in MAN.
EOT	Pushbutton indicator-switch	Lights when end-of-tape is reached. Tape stops in 1/2 second. If depressed while tape is running forward in MAN operation, simulates end-of-tape.

TABLE 3-2. TAPE HANDLER CONTROL PANEL INDICATORS AND CONTROLS (CONT.)

NOMENCLATURE	SWITCH OR INDICATOR	FUNCTION
HANDLER 1		
BOT	Pushbutton indicator-switch	Lights when tape is at load point. If depressed while tape is running backward in manual operation, tape stops but indicator is extinguished. REWIND and REV still operative.
READY	Pushbutton indicator-switch*	Lights when HANDLER switch is set to MAN or AUTO except when tape is positioned at load point. Conditioned on POWER ON and transport interlocks.
STOP	Pushbutton switch	Stops tape motion when depressed. Operative in MAN only.
MAN-OFF-AUTO	Three-position rotary switch	MAN: Applies power to transport 1 and permits manual operation. OFF: Removes power from transport 1. NOTE Transport power is conditioned on primary power control panel POWER ON switch (A11S1), tape handler control panel POWER ON switch (A1S1), and transport interlocks. AUTO: Applies power to transport and permits automatic operation.
HANDLER 2	Same as handler 1	Switches and indicators exercise same controls over transport 2 as those described for transport 1.

* No switch functions

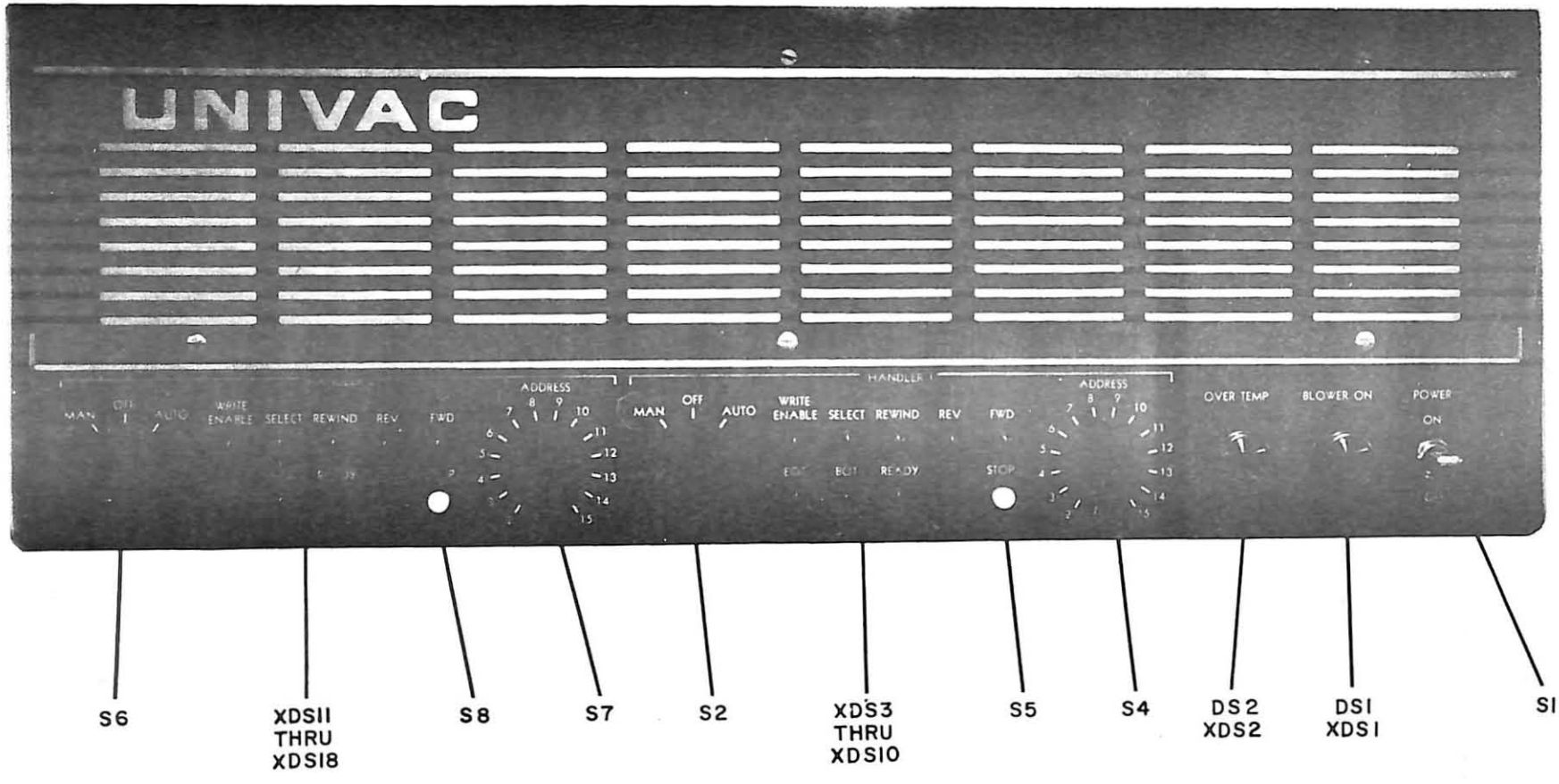


Figure 3-2. Tape Handler Control Panel, (A1)

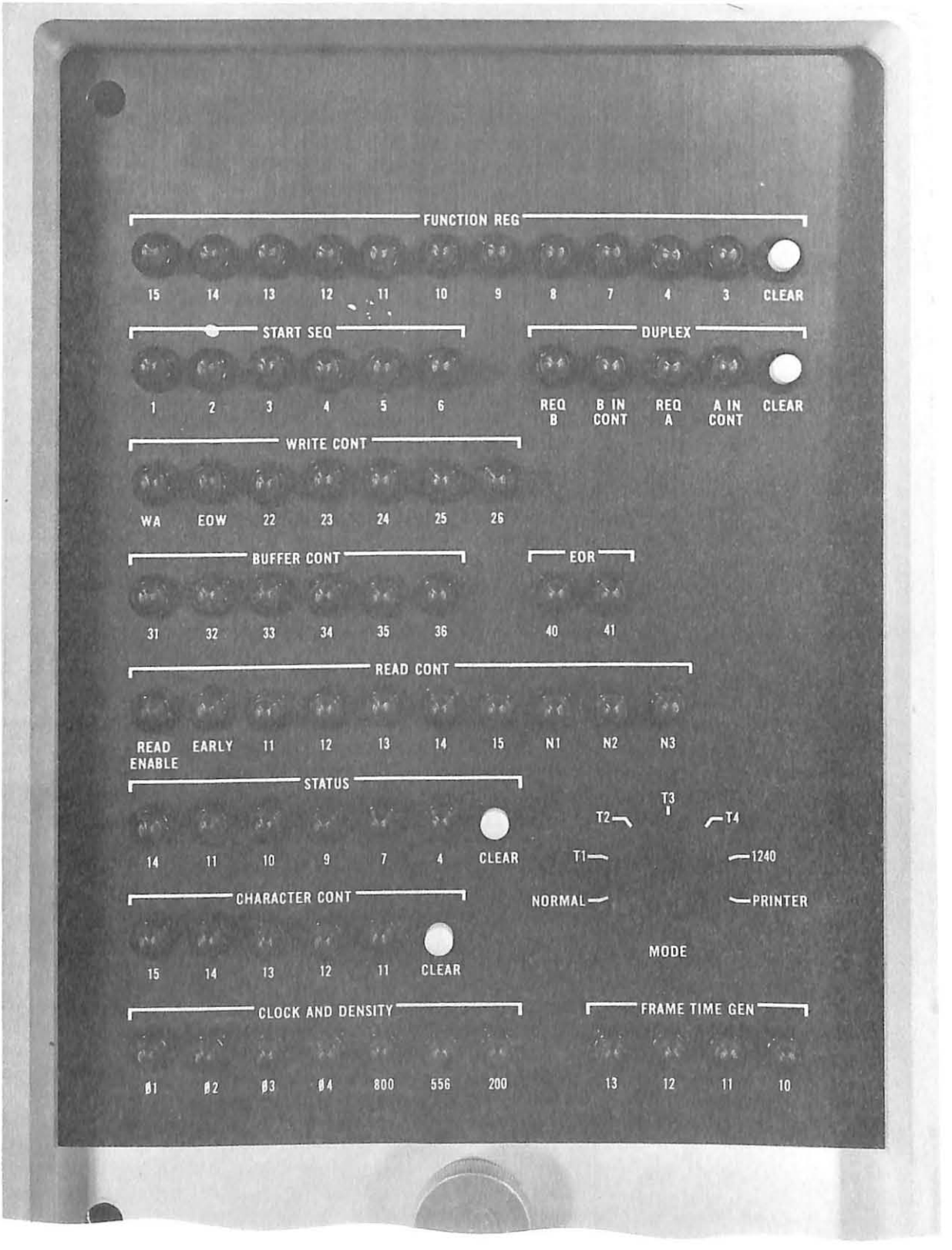


Figure 3-3. Upper Maintenance and Control Panel (Upper Portion)

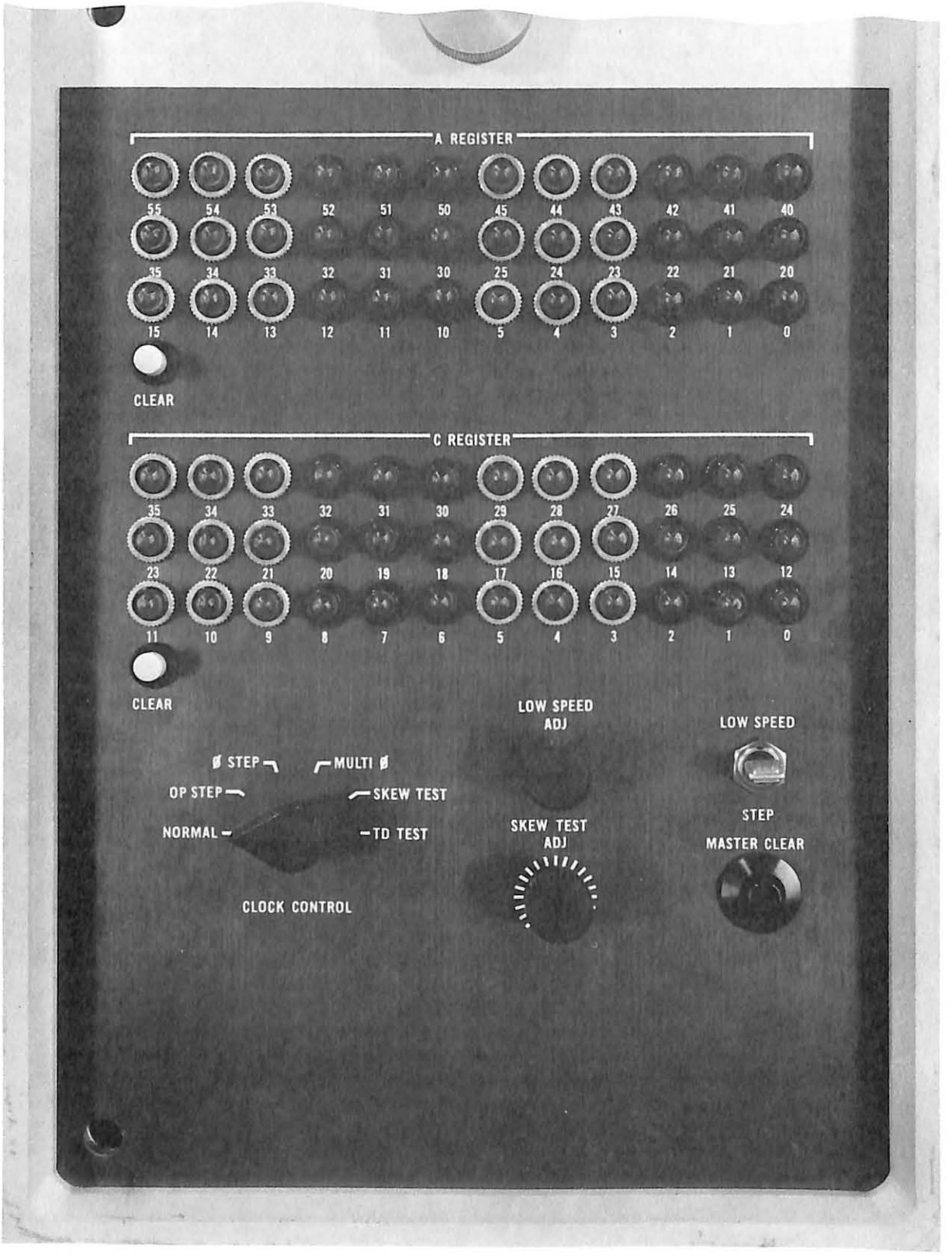


Figure 3-4. Upper Maintenance and Control Panel (Lower Portion)

TABLE 3-2. TAPE HANDLER CONTROL PANEL INDICATORS AND CONTROLS (CONT.)

NOMENCLATURE	SWITCH OR INDICATOR	FUNCTION
HANDLER 1		
BOT	Pushbutton indicator-switch	Lights when tape is at load point. If depressed while tape is running backward in manual operation, tape stops but indicator is extinguished. REWIND and REV still operative.
READY	Pushbutton indicator-switch*	Lights when HANDLER switch is set to MAN or AUTO except when tape is positioned at load point. Conditioned on POWER ON and transport interlocks.
STOP	Pushbutton switch	Stops tape motion when depressed. Operative in MAN only.
MAN-OFF-AUTO	Three-position rotary switch	MAN: Applies power to transport 1 and permits manual operation. OFF: Removes power from transport 1 (Note CAUTION on page 3-13.). NOTE Transport power is conditioned on primary power control panel POWER ON switch (A11S1), tape handler control panel POWER ON switch (A1S1), and transport interlocks. AUTO: Applies power to transport and permits automatic operation (Note CAUTION on page 3-13.)
HANDLER 2	Same as handler 1	Switches and indicators exercise same controls over transport 2 as those described for transport 1.

* No switch functions

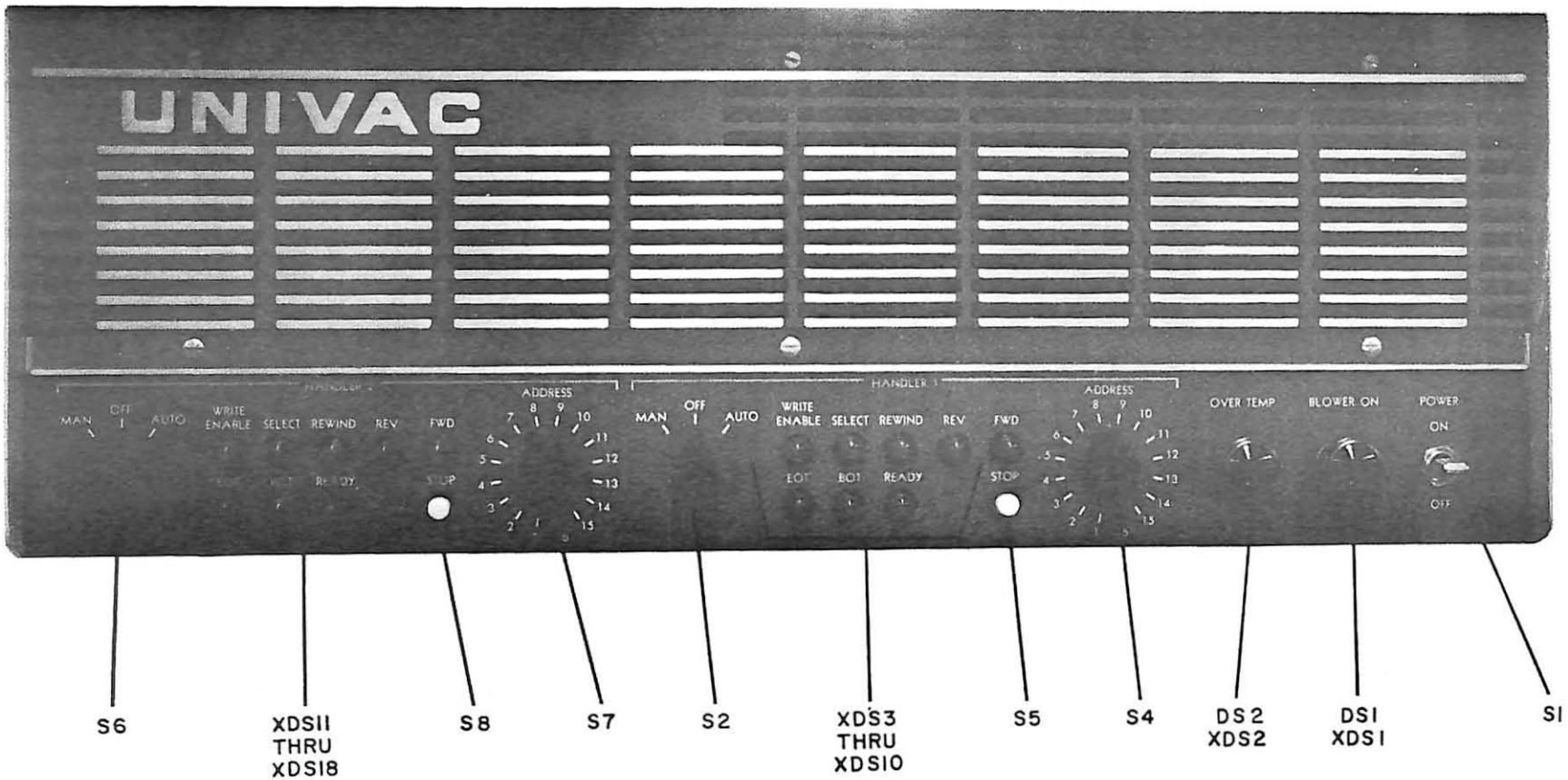


Figure 3-2. Tape Handler Control Panel, (A1)

TABLE 3-4. LOWER MAINTENANCE AND CONTROL PANEL CONTROLS AND INDICATORS

NOMENCLATURE	SWITCH OR INDICATOR	FUNCTION
LONG COUNT READ WRITE R* REG	Pushbutton indicator-switches	Indicators: Always active. Show state of associated register bits. Switches: Inactive in NORMAL and 1240 modes. When active, depressing indicator-switches sets associated register bits and depressing CLEAR switches, clears associated registers.
HANDLER TEST ADJUST SPEED	Control	Varies frequency of pulses provided by RANGE FAST-SLOW.
RANGE FAST-SLOW	Two-position toggle switch	FAST: Provides oscillator pulses that may be varied, by SPEED control, from approximately 2.5 cycles per second to 40 cycles per second for checking handler start-stop times. SLOW: Provides oscillator pulses that may be varied, by SPEED control, from approximately 0.33 cycle per second to 3.0 cycles per second for checking transport start-stop times.

b. TURN-ON PROCEDURE. - The turn-on procedure must be accomplished prior to loading the tape. To turn on the MTU, proceed as follows.

STEP 1. Ensure that circuit breaker on handler electronic drive unit is on.

STEP 2. Set HANDLER MAN-OFF-AUTO switch(es) to OFF.

STEP 3. Momentarily set primary power control panel POWER switch to ON. Green LOGIC and BLOWERS indicator light.

STEP 4. Momentarily set tape handler control panel POWER switch to ON. Green BLOWER ON indicator lights.

CAUTION

Do not turn MAN-OFF-AUTO switches on tape handlers 1 and 2 to MAN/AUTO positions simultaneously. The current surge of both vacuum motors will cause circuit breaker (A3A3/CB1) to trip. Allow handler motor 1 to come to full speed (approximately 5 seconds) prior to turning handler 2 switch to MAN/AUTO.

STEP 5. Set appropriate HANDLER MAN-OFF-AUTO switch(es) to MAN.

NOTE

For emergency turnoff, set primary power control panel POWER switch to OFF.

c. TAPE LOAD PROCEDURE. - Loading the tape on the tape transports requires mounting a reel of tape on the upper or right tape transport hub, attaching the tape to a takeup reel on the lower or left hub, performing the appropriate tape threading, and positioning the tape at the beginning of tape reference mark (load point).

To load a tape on the MTU, proceed as follows.

STEP 1. Perform turn-on procedure (refer to paragraph 3-2b).

STEP 2. Mount reel of tape on upper hub (see figure 3-6).

NOTE

If a write operation is to be executed during the program, ensure that the write enable ring is positioned in the reel. If a master tape is used, ensure that the write enable ring has been removed from the reel to prevent accidental writing on the master tape.

STEP 3. Mount empty reel on lower hub if required.

STEP 4. Depress retraction switch (see figure 3-6) on tape transport. Tension arms position to tape load (center) position.

STEP 5. Unwind several feet of tape from upper reel.

STEP 6. Hold free end of tape to core of takeup reel with finger and wind about three turns of tape on takeup reel in clockwise direction (tape path is as shown in figure 3-6).

CAUTION

Do not slip the free end of the tape into the reel core slot, and do not secure the free end to the reel in any manner.

STEP 7. Open vacuum buffer cover and head cover.

STEP 8. Thread tape through drive assembly (see figure 3-6).

STEP 9. Remove slack in tape by rotating lower reel in clockwise direction.

STEP 10. Press retraction switch and wait for tension arms to stop.

STEP 11. Manually rotate reels until tension arms are at their normal run position (mid range).

STEP 12. Inspect to ensure tape is properly positioned within guide rollers and guide trough.

TABLE 3-3. UPPER MAINTENANCE AND CONTROL PANEL INDICATORS AND CONTROLS

NOMENCLATURE	SWITCH OR INDICATOR	FUNCTION
FUNCTION REG	Pushbutton indicator-switches	Indicators: Always active. Show state of associated register bits. Switches: Inactive in NORMAL and 1240 modes. When active, depressing indicator-switches sets associated register bits and depressing CLEAR switch clears the register.
START SEQ DUPLEX WRITE CONT BUFFER CONT EOR READ CONT	Pushbutton indicator-switches	Indicators: Always active. Show state of associated flip-flop. Switches: Inactive in NORMAL and 1240 modes. When active, depressing indicator-switches sets associated flip-flop and depressing CLEAR switch clears duplexer. In simplexed units, A IN CONT indicator immediately relights.
STATUS	Pushbutton indicator-switches	Indicators: Always active. Show state of associated register bits. Switches: Inactive in NORMAL and 1240 modes. When active, depressing indicator-switches sets associated register bits and depressing CLEAR switch clears the register.
CHARACTER CONT	Pushbutton indicator-switches	Indicators: Always active. Show state of associated character counter stage. Switches: Inactive in NORMAL and 1240 modes. When active, depressing indicator-switches sets associated character counter stage and depressing CLEAR switch clears character counter.
MODE NORMAL-T1-T2-T3-T4-1240-PRINTER	Seven-position rotary switch	NORMAL: Places MTU under computer control. All indicators are active and all switches, except WRITE ENABLE, are inactive provided the HANDLER MAN-OFF-AUTO switch is set to AUTO. (WRITE ENABLE and HANDLER MAN-OFF-AUTO switches are located on tape handler control panel.) T1: Enables operation of all switches on upper and lower maintenance and control panels. MTU may be under computer or manual control. T2: Places MTU under manual control. All upper and lower maintenance and control panel switches and indicator-switches are active.

TABLE 3-3. UPPER MAINTENANCE AND CONTROL PANEL INDICATORS AND CONTROLS (CONT.)

NOMENCLATURE	SWITCH OR INDICATOR	FUNCTION
MODE (Cont.)		T3: Enables MTU to perform operation contained in function register. Defined by CLOCK CONTROL switch each time LOW SPEED-STEP switch is depressed. When switch is set to LOW SPEED, function repeats at a rate determined by LOW SPEED ADJ. T4: Enables 1240 mode. MTU may be under computer or manual control. All switches are operative. 1240: Enables MTU to operate with the computer using programs developed for 1240 MTU. MTU is under computer control. All indicator-switches, except WRITE ENABLE (on tape handler control panel), are inoperative. PRINTER: Enables MTU to send data read to a high-speed printer.
FRAME TIME GEN	Indicator-switches	Indicators always active. Show state of associated FTG stage. Switches are inactive in NORMAL and 1240 modes.
CLOCK AND DENSITY	Indicators	Ø1, Ø2, Ø3, Ø4: Light for respective clock phases being issued. 800, 556, 200: Indicate selected density.
A REGISTER C REGISTER	Pushbutton indicator-switches	Indicators: Always active. Show state of associated register bits. Switches: Inactive in NORMAL and 1240 modes. When active, depressing indicator-switches sets associated register bits and depressing CLEAR switches clears associated register.
CLOCK CONTROL NORMAL-OP STEP-Ø STEP-MULTI Ø-SKEW TEST-TD TEST	Six-position rotary switch	Provides selection of rates at which MTU produces clock phases or cycling of time delays so that output can be observed. NORMAL: Enables clock to issue four phase signals each clock cycle. Cycle and phase durations are dependent upon computer density selection. OP STEP: Allows checking of start sequence. Normal sequence occurs up to the point of handler selection. When LOW SPEED-STEP switch is set to STEP, designated transport is selected but starting of tape movement is disabled.

TABLE 3-3. UPPER MAINTENANCE AND CONTROL PANEL INDICATORS AND CONTROLS (CONT.)

NOMENCLATURE	SWITCH OR INDICATOR	FUNCTION
CLOCK CONTROL (Cont.)		When LOW SPEED-STEP switch is released, tape movement is started and MTU continues to operate in high speed. Ø STEP: Enables clock to advance to next phase each time LOW SPEED-STEP switch is set to STEP. With switch set to LOW SPEED, clock advances at rate determined by LOW SPEED ADJ. MULTI Ø: Enables clock to continuously issue selected clock phase each time LOW SPEED-STEP switch is depressed to STEP in LOW SPEED, at rate determined by LOW SPEED ADJ. SKEW TEST: Enables read circuits to provide for a rapid overall check of deskewing delays. TD TEST: Allows setting of time delay circuits under control of LOW SPEED-STEP switch for maintenance purposes.
LOW SPEED ADJ	Control	Varies frequency of low-speed oscillator between 2 and 140 pulses-per-second. Used in conjunction with LOW SPEED-STEP switch.
LOW SPEED-STEP	Three-position toggle switch; spring loaded in STEP position	In conjunction with CLOCK CONTROL switch, controls issuance of clock phases. In conjunction with CLOCK CONTROL and MODE switches, controls manual initiation of MTU operations. Operation is performed each time switch is set momentarily to STEP. In LOW SPEED position, operations are performed at a rate determined by LOW SPEED ADJ.
MASTER CLEAR	Pushbutton switch	Clears control sequences and MTU registers when operating in any mode except NORMAL and 1240.
SKEW TEST ADJ	Control	Varies time allowed for gating data read from tape through read register into R* register.

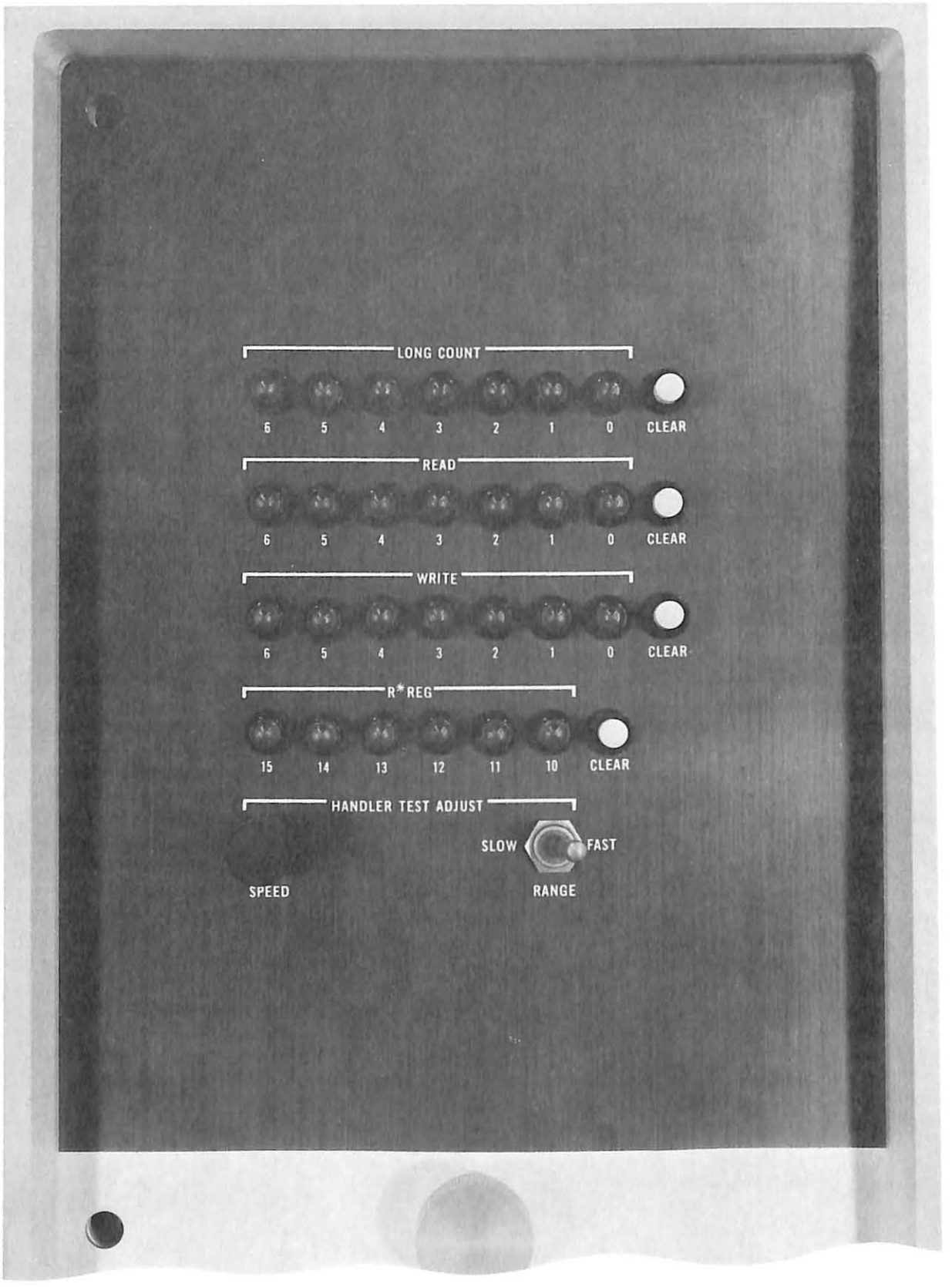


Figure 3-5. Lower Maintenance and Control Panel

TABLE 3-4. LOWER MAINTENANCE AND CONTROL PANEL CONTROLS AND INDICATORS

NOMENCLATURE	SWITCH OR INDICATOR	FUNCTION
LONG COUNT READ WRITE R* REG	Pushbutton indicator-switches	Indicators: Always active. Show state of associated register bits. Switches: Inactive in NORMAL and 1240 modes. When active, depressing indicator-switches sets associated register bits and depressing CLEAR switches, clears associated registers.
HANDLER TEST ADJUST SPEED	Control	Varies frequency of pulses provided by RANGE FAST-SLOW.
RANGE FAST-SLOW	Two-position toggle switch	FAST: Provides oscillator pulses that may be varied, by SPEED control, from approximately 2.5 cycles per second to 40 cycles per second for checking handler start-stop times. SLOW: Provides oscillator pulses that may be varied, by SPEED control, from approximately 0.33 cycle per second to 3.0 cycles per second for checking transport start-stop times.

b. TURN-ON PROCEDURE. - The turn-on procedure must be accomplished prior to loading the tape. To turn on the MTU, proceed as follows.

STEP 1. Ensure that circuit breaker on handler electronic drive unit is on.

STEP 2. Set HANDLER MAN-OFF-AUTO switch(es) to OFF.

STEP 3. Momentarily set primary power control panel POWER switch to ON. Green LOGIC and BLOWERS indicator light.

STEP 4. Momentarily set tape handler control panel POWER switch to ON. Green BLOWER ON indicator lights.

STEP 5. Set appropriate HANDLER MAN-OFF-AUTO switch(es) to MAN.

NOTE

For emergency turnoff, set primary power control panel POWER switch to OFF.

c. TAPE LOAD PROCEDURE. - Loading the tape on the tape transports requires mounting a reel of tape on the upper or right tape transport hub, attaching the tape to a takeup reel on the lower or left hub, performing the appropriate tape threading, and positioning the tape at the beginning of tape reference mark (load point).

To load a tape on the MTU, proceed as follows.

STEP 1. Perform turn-on procedure (refer to paragraph 3-2b).

STEP 2. Mount reel of tape on upper hub (see figure 3-6).

NOTE

If a write operation is to be executed during the program, ensure that the write enable ring is positioned in the reel. If a master tape is used, ensure that the write enable ring has been removed from the reel to prevent accidental writing on the master tape.

STEP 3. Mount empty reel on lower hub if required.

STEP 4. Depress retraction switch (see figure 3-6) on tape transport. Tension arms position to tape load (center) position.

STEP 5. Unwind several feet of tape from upper reel.

STEP 6. Hold free end of tape to core of takeup reel with finger and wind about three turns of tape on takeup reel in clockwise direction (tape path is as shown in figure 3-6).

CAUTION

Do not slip the free end of the tape into the reel core slot, and do not secure the free end to the reel in any manner.

STEP 7. Open vacuum buffer cover and head cover.

STEP 8. Thread tape through drive assembly (see figure 3-6).

STEP 9. Remove slack in tape by rotating lower reel in clockwise direction.

STEP 10. Press retraction switch and wait for tension arms to stop.

STEP 11. Manually rotate reels until tension arms are at their normal run position (mid range).

STEP 12. Inspect to ensure tape is properly positioned within guide rollers and guide trough.

STEP 13. Close head and buffer covers.

STEP 14. Depress appropriate HANDLER FWD switch and let tape run forward for about 5 seconds. Depress HANDLER STOP switch.

STEP 15. Press HANDLER REWIND switch. Tape will run in reverse to load point and stop.

STEP 13. Close head and buffer covers.

STEP 14. Depress appropriate HANDLER FWD switch and let tape run forward for about 5 seconds. Depress HANDLER STOP switch.

STEP 15. Press HANDLER REWIND switch. Tape will run in reverse to load point and stop.

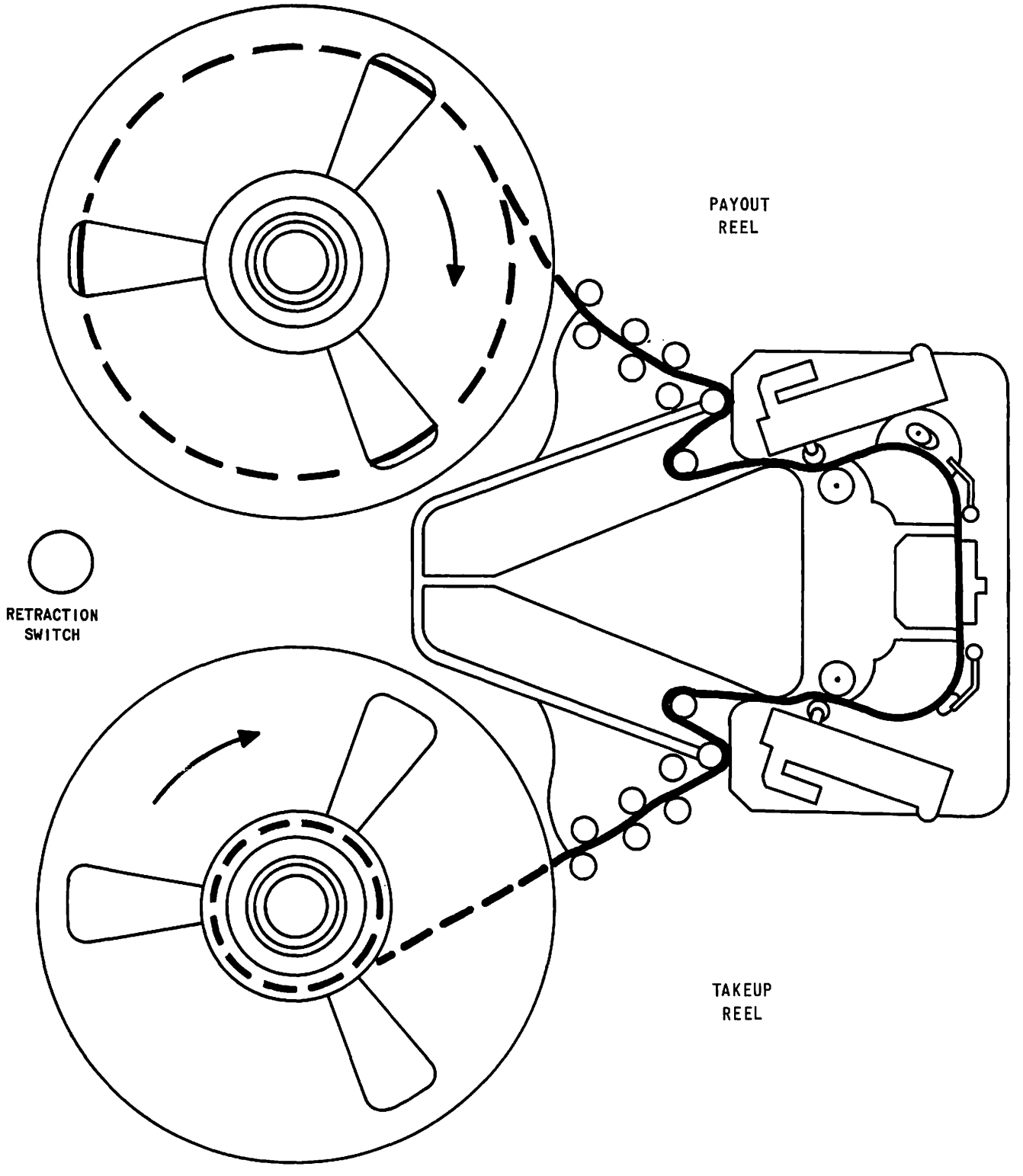


Figure 3-6. Tape Threading

d. TRANSPORT CHECKOUT. - The procedures in this paragraph enable the operator to check the transport's responses to the commands which affect the tape movement. It is assumed that the turnon and tape load procedures have been completed.

STEP 1. Depress HANDLER FORWARD (FED) switch. Tape runs forward and FORWARD (FWD) indicator lights. Allow tape to run forward for about one minute.

STEP 2. Depress HANDLER STOP switch. Tape stops and FORWARD (FWD) indicator extinguishes.

STEP 3. Depress HANDLER FORWARD (FWD) switch. Tape runs forward and FORWARD (FWD) indicator lights.

STEP 4. Depress HANDLER STOP switch. Tape stops and FORWARD (FWD) indicator extinguishes.

STEP 5. Depress HANDLER REVERSE (REV) switch. Tape runs backward. REVERSE (REV) indicator lights.

STEP 6. Depress HANDLER STOP switch. Tape stops. REVERSE (REV) indicator extinguishes.

STEP 7. Depress and hold HANDLER FORWARD (FWD) and REWIND switches. Tape moves forward at high speed. Release REWIND switch. Tape slows to normal speed.

STEP 8. Depress HANDLER EOT switch. Tape stops in 1/2-second and FORWARD (FWD) indicator extinguishes.

STEP 9. Depress HANDLER REWIND switch. REWIND indicator lights. Tape runs backward at high speed.

STEP 10. Depress HANDLER BOT switch. Tape stops and REWIND indicator extinguishes.

STEP 11. Depress HANDLER REWIND switch. REWIND indicator lights. Tape runs backward at high speed until low tape is sensed, then slows down to normal speed. When load point is reached, tape stops, REWIND indicator extinguishes, and BOT indicator lights.

NOTE

The tape is now properly positioned for automatic operation. The HANDLER REVERSE (REV) and REWIND switches are ineffective.

e. AUTOMATIC OPERATION WITH COMPUTER. - After the turnon and tape loading procedures of paragraphs 3-2b and 3-2c or the transport checkout of paragraph 3-2d has been completed, prepare the MTU for automatic operation with the computer by proceeding as follows.

STEP 1. Set all HANDLER MAN-OFF-AUTO switches to OFF. All HANDLER READY indicators extinguish.

STEP 2. Set each HANDLER ADDRESS switch to transport address desired.

STEP 3. Set MODE switch to NORMAL.

CAUTION

Do not turn MAN-OFF-AUTO switches on tape handlers 1 and 2 to MAN/AUTO positions simultaneously. The current surge of both vacuum motors will cause circuit breaker (A3A3/CB1) to trip. Allow handler motor 1 to come to full speed (approximately 5 seconds) prior to turning handler 2 switch to MAN/AUTO.

STEP 4. Set HANDLER MAN-OFF-AUTO switch to AUTO on each transport to be used. HANDLER READY and BOT indicators will light for each handler so energized.

STEP 5. Depress HANDLER WRITE ENABLE switch if tape is to be written on.

STEP 6. Depress MASTER CLEAR switch. The MTU is now prepared for computer control.

f. AUTOMATIC OPERATION WITH HIGH-SPEED PRINTER. - When the MTU output (printer-input) cable is connected to the high-speed printer, perform the following steps to prepare it for automatic operation.

STEP 1. Make sure HANDLER 1 ADDRESS switch is set to 1.

STEP 2. Set HANDLER 1 MAN-OFF-AUTO switch to AUTO.

STEP 3. Manually select transport 1 as follows.

a. Set MODE switch to T4.

b. Set CLOCK CONTROL switch to OP STEP.

c. Depress MASTER CLEAR switch.

d. Depress C REGISTER indicator-switches 0, 3, and 17.

e. Depress START SEQ indicator-switch 1.

STEP 4. Set CLOCK CONTROL switch to NORMAL.

STEP 5. Depress MASTER CLEAR switch.

STEP 6. Set MODE switch to PRINTER. Note that F REGISTER bit 10 is set (Mod 5).

STEP 7. Manually set character, parity, and density bits in F REGISTER to conform with those in which tape was recorded.

STEP 8. Place high-speed printer on-line.

g. TAPE UNLOAD PROCEDURES.

To unload a tape from the MTU, proceed as follows.

STEP 1. Make sure primary power control panel POWER and tape handler control panel POWER switches are set to ON.

STEP 2. Set HANDLER MAN-OFF-AUTO switch to MAN.

STEP 3. Depress retraction switch on tape transport. Tension arms position to tape load (center) position.

STEP 4. Rotate tape payout reel counterclockwise to remove slack from tape.

STEP 5. Rotate both reels counterclockwise until all tape is on payout reel.

STEP 6. Remove payout reel.

h. TURNOFF PROCEDURE. To turn off the MTU, proceed as follows.

STEP 1. Set HANDLER MAN-OFF-AUTO switch(es) to OFF.

STEP 2. Momentarily set primary power control panel POWER switch to OFF.

STEP 4. Set HANDLER MAN-OFF-AUTO switch to AUTO on each transport to be used. HANDLER READY and BOT indicators will light for each handler so energized.

STEP 5. Depress HANDLER WRITE ENABLE switch if tape is to be written on.

STEP 6. Depress MASTER CLEAR switch. The MTU is now prepared for computer control.

f. AUTOMATIC OPERATION WITH HIGH-SPEED PRINTER. - When the MTU output (printer-input) cable is connected to the high-speed printer, perform the following steps to prepare it for automatic operation.

STEP 1. Make sure HANDLER 1 ADDRESS switch is set to 1.

STEP 2. Set HANDLER 1 MAN-OFF-AUTO switch to AUTO.

STEP 3. Manually select transport 1 as follows.

a. Set MODE switch to T4.

b. Set CLOCK CONTROL switch to OP STEP.

c. Depress MASTER CLEAR switch.

d. Depress C REGISTER indicator-switches 0,3, and 17.

e. Depress START SEQ indicator-switch 1.

STEP 4. Set CLOCK CONTROL switch to NORMAL.

STEP 5. Depress MASTER CLEAR switch.

STEP 6. Set MODE switch to PRINTER. Note that F REGISTER bit 10 is set (Mod 5).

STEP 7. Manually set character, parity, and density bits in F REGISTER to conform with those in which tape was recorded.

STEP 8. Place high-speed printer on-line.

g. TAPE UNLOAD PROCEDURES.

To unload a tape from the MTU, proceed as follows.

STEP 1. Make sure primary power control panel POWER and tape handler control panel POWER switches are set to ON.

STEP 2. Set HANDLER MAN-OFF-AUTO switch to MAN.

STEP 3. Depress retraction switch on tape transport. Tension arms position to tape load (center) position.

STEP 4. Rotate tape payout reel counterclockwise to remove slack from tape.

STEP 5. Rotate both reels counterclockwise until all tape is on payout reel.

STEP 6. Remove payout reel.

h. TURNOFF PROCEDURE. To turn off the MTU, proceed as follows.

STEP 1. Set HANDLER MAN-OFF-AUTO switch(es) to OFF.

STEP 2. Momentarily set primary power control panel POWER switch to OFF.

SECTION 4

PRINCIPLES OF OPERATION

4-1. OVERALL FUNCTIONAL DESCRIPTION.

This section describes the operations of the functional sections and the subsections, MTU-computer interfaces, instruction and status words, high-speed printer-MTU interfaces, recording methods, and the programmer considerations during operation.

a. BLOCK DIAGRAM DESCRIPTIONS OF FUNCTIONAL SECTIONS. - Figure 4-1 illustrates the basic relationships existing between all of the functional sections and subsections of the MTU. The three basic functional sections are: magnetic tape control, tape transport control, and the tape transports. The magnetic tape control section is further subdivided into the input/output, data format, and primary subsections. The description of each of these sections is supported by an applicable block diagram.

(1) MAGNETIC TAPE CONTROL SECTION. - The magnetic tape control section which is comprised of the input/output (I/O), data format, and primary control subsections, consists of registers, counters, and timing circuits. The circuits function together to communicate with the computer(s), set up timing sequences, and perform the other control operations which are necessary to successfully execute assigned functions.

(a) INPUT/OUTPUT SUBSECTION. - See figure 4-2. The I/O subsection provides the means for maintaining communications with the computer. The I/O subsection consists of the (C) register communications, I/O control, and duplex control.

1. C REGISTER. - The C register is a 36 stage, input/output buffer register through which all data, either to or from the computer, passes. During the initiating phases of a function, the C register stores the function word while the operations are begun. While performing a search or selective read operation, the C register stores the search key or selective read identifier.

2. I/O CONTROL. - I/O control receives the control signals originated by the computer(s) and initiates the responsive actions required for each signal. For a duplex external function, I/O control enables duplex control to sample the computer output lines in order to establish the designated duplex operation. For a non-duplex operation, I/O control clears the C register, gates the external function (EF) word from the computer output lines into the C register, and initiates the start sequence via duplex control. When I/O control receives an output acknowledge from the computer, it clears the C register, gates the data on the computer output lines into the C register, and removes the ODR in write control. When I/O control receives an input acknowledge from the computer, it removes the IDR in buffer control. Interrupts are sent to the computer by way of duplex control. When the input acknowledge is received, I/O control clears the interrupt circuits.

3. DUPLEX CONTROL. - Duplex control enables the MTU to be controlled by either of two computers on a one-at-a-time basis. It provides for requesting control, demanding control, releasing control, and master clearing of the MTU by a computer when in control.

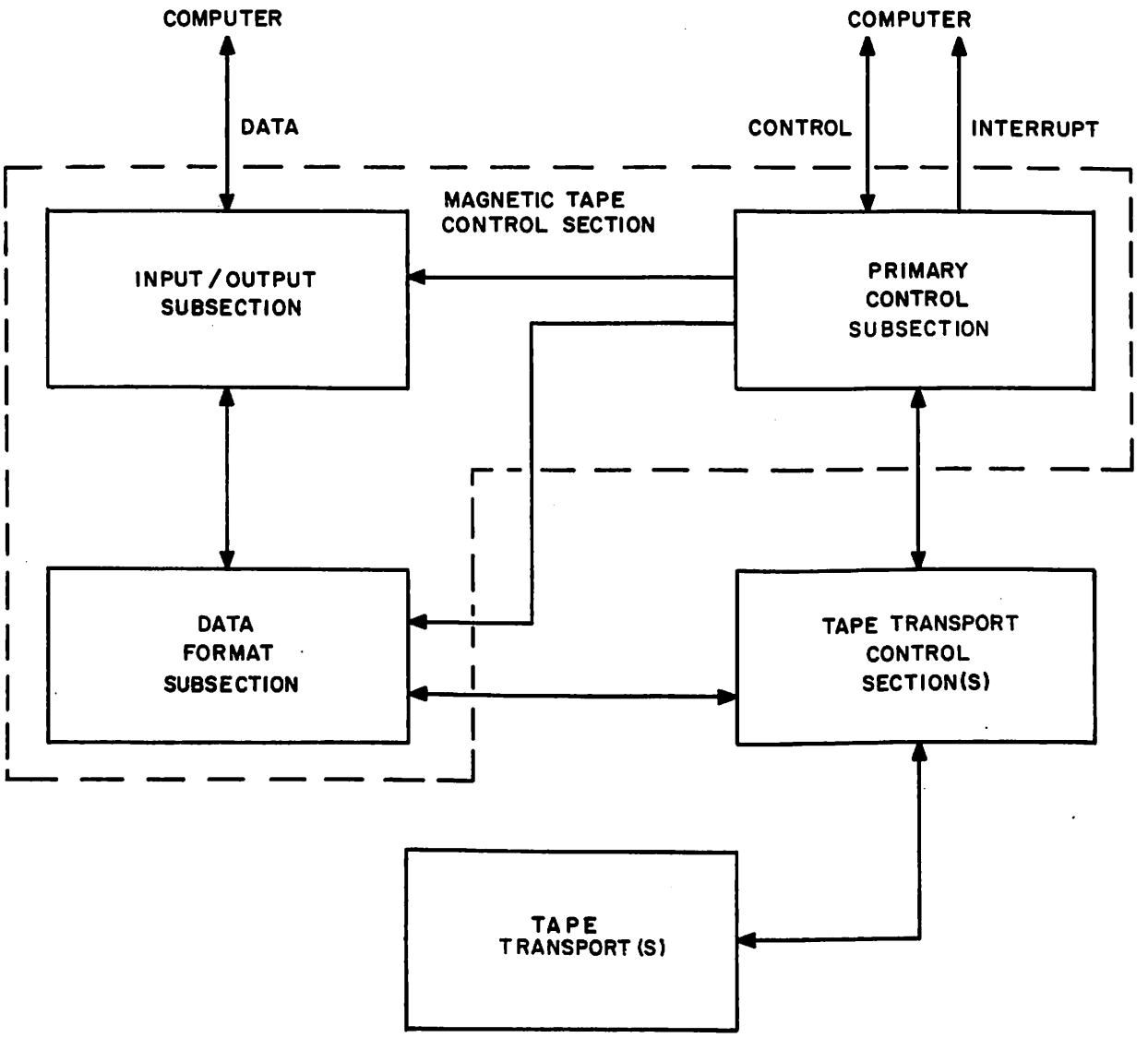


Figure 4-1. Magnetic Tape Unit, Simplified Block Diagram

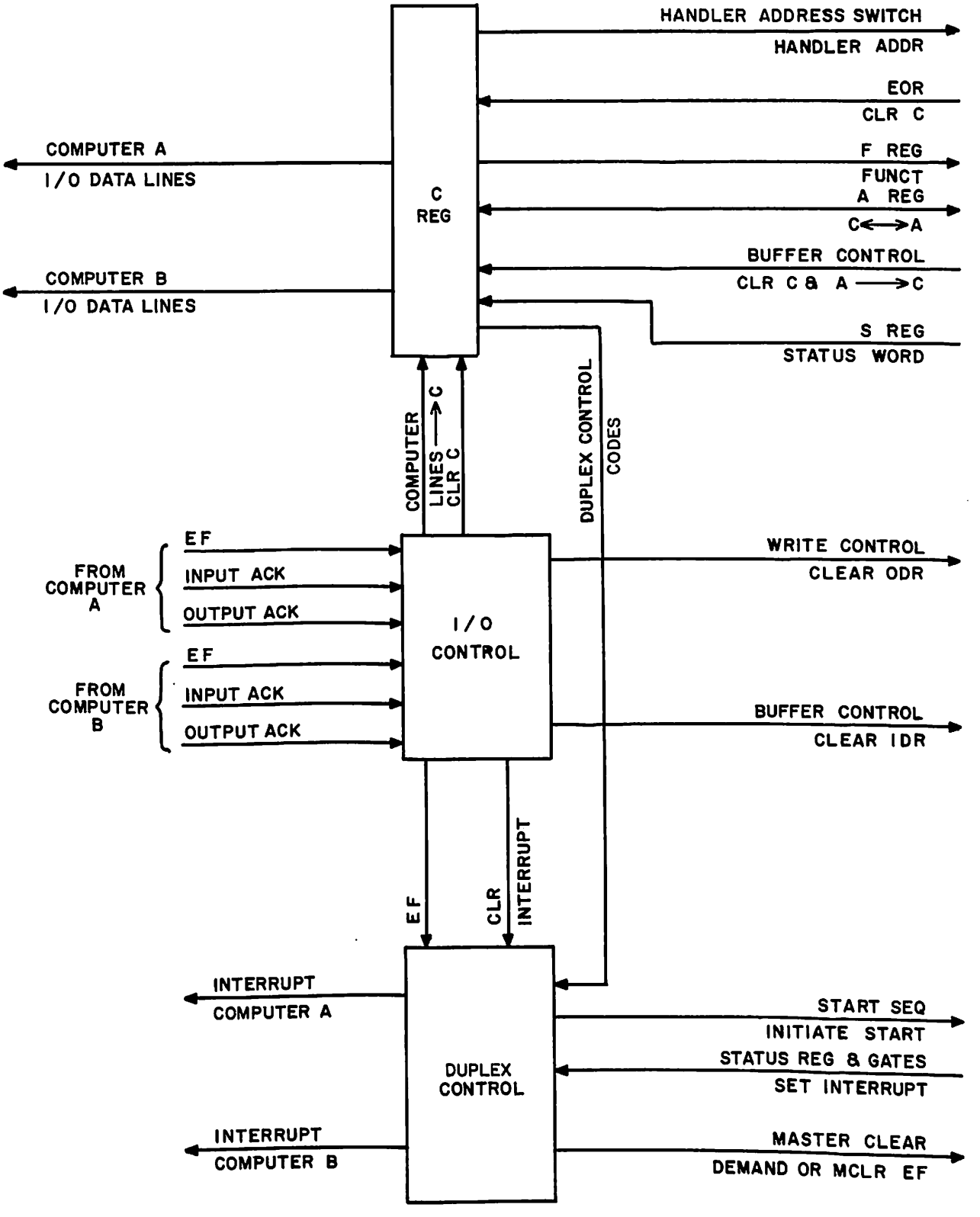


Figure 4-2. Input/Output Subsection, Block Diagram

(b) DATA FORMAT SUBSECTION. - See figure 4-3. The data format subsection is utilized by the magnetic tape control section, in a write mode, to disassemble computer words, develop parity, and control the character (octal or bioctal) in which the data is recorded on tape. In a read mode, the data format section receives data from the tape transport, checks and deletes the parity bit, assembles the data into computer words, and makes the data available for transmission to the computer. To accomplish word assembly or disassembly the data format subsection utilizes the character counter (K_C), the assembly-disassembly (A) register, the R* register, the write (W) register, the read (R) register, the write encoder, the R accumulator, and the read and write compensation delays (RCD's and WCD's).

1. R REGISTER. - The R register is a seven-stage buffer register which receives each frame of information read from the tape after it has been amplified, detected, and deskewed. The R register stages provide outputs to the R accumulator for making a lateral parity check of each frame, and to the longitudinal count (L) register for maintaining a check on longitudinal parity. The R register stages also provide outputs to the R* register.

2. R* REGISTER. - The R* register is a six-stage register which provides a means for assembling two frames which have been recorded octally (redundant format) into the six bits of data from which the two frames were originally derived. In bioctal format, the six data bits in the R register are gated, in parallel, into the R* register. The parity bit is not gated into the R* register and is thus deleted. When reading redundant format in a forward direction, read control, in conjunction with the K_C, gates the upper and lower three data bits of the first frame from the R register into the upper three stages of the R* register. The second frame is then gated in a similar manner into the lower three stages of the R* register. When reading the tape in a reverse direction, the lower three stages of the R* register receive the first frame read and the upper three stages receive the second frame. R* register outputs are provided to each of the A subregisters.

3. A REGISTER. - The A register is a 36-stage register which, when utilized in conjunction with the K_C, disassembles computer words into 6-bit subwords for recording on tape (during write operations) or assembles the 6-bit data frames read from tape into computer words (during read-type operations). To facilitate the assembling and disassembling of computer words, the A register is divided into 6-bit subregisters, A0 through A5. During read operations, each frame of data read into the R* register is gated into its appropriate A subregister under control of the K_C. When a complete computer word has been assembled, it may be transmitted in parallel to the C register for transmission to the computer. In a write operation, the A register receives a computer word, in parallel, from the C register and transmits each subregister (as specified by the K_C and character designators), in turn, to the write encoder for subsequent recording on tape. The A register also contains circuits which compare the contents of the C register to the contents of the A register for search and read selective operations.

4. W REGISTER. - The W register is a seven-stage register which makes the 7-bit frames (six data bits and one parity bit) of information available to drive the write heads. The information is gated from the write encoder to the WCD's for each channel. The outputs of the WCD's, in turn, feed the flip-flop toggle circuits that either clear or set the W register stages for each logic 1 to be recorded (depending on the prior condition of each stage).

5. RCD'S. - The RCD's consist of a time delay in each read channel. Each time delay is adjusted automatically, by preset deskewing adjustments, to compensate for the read head skew of each tape transport.

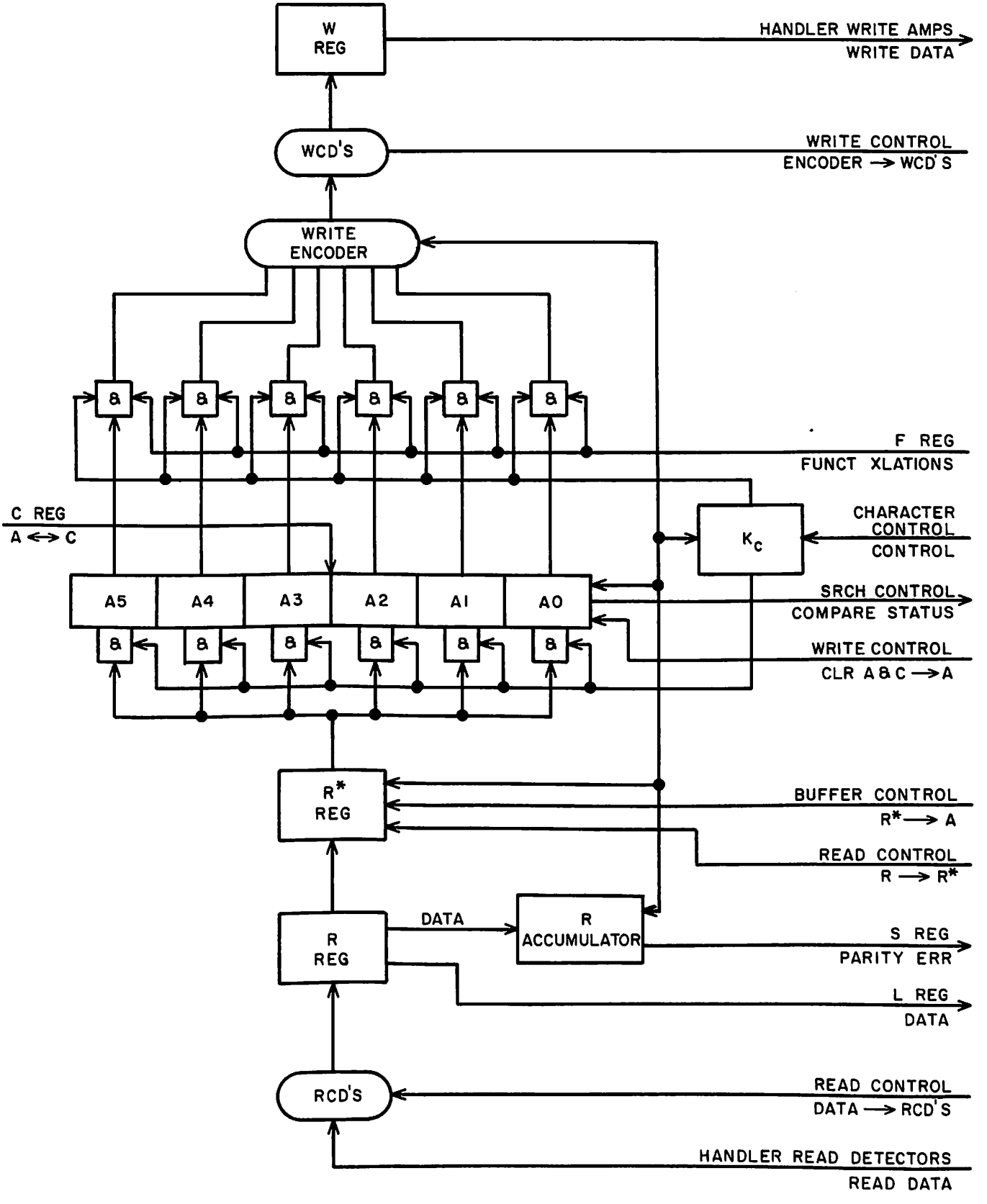


Figure 4-3. Data Format Subsection, Block Diagram

6. WCD'S. - The WCD's consist of a time delay in each write channel. Each time delay is adjusted automatically, by preset deskewing adjustments, to compensate for the write head skew of each tape transport.

7. R ACCUMULATOR. - The R accumulator receives inputs from the R register stages for each frame read from one tape and determines if the parity, as recorded, is correct. If the parity is determined to be incorrect, the R accumulator provides an output for setting a data error indicator in the status (S) register.

8. WRITE ENCODER. - In octal character, the write encoder develops a 6 bit data frame and a parity bit from each group of three bits, in an A subregister, being gated to it by the K_C. Thus, each 6 bit character of the computer word is recorded on two frames on tape. In bioctal character, the K_C gates all six bits of data in an A subregister through the write encoder in parallel. The write encoder generates the parity bit. Write control gates the outputs of the write encoder to the WCD's. When the delay of the WCD's expires, the stages of the W register which receive a logic 1 are toggled and the data is recorded on tape by way of the write amplifiers and the write head.

9. CHARACTER COUNTER (K_C). - The K_C is a five-stage counter which, during a write, controls the flow of data from the A subregisters to the write encoder for subsequent recording on tape. During a read the K_C controls the flow of data from the R* register into the appropriate A subregisters for assembling into computer words. The K_C operation is regulated by character control, in conjunction with the format designators, in the function register.

(c) PRIMARY CONTROL SUBSECTION. - See figure 4-4. The primary control subsection consists of the circuits that exercise basic control over the other sections and/or subsections. The primary control section consists of the following registers, counters, and control circuits:

1) Clock logic
2) Master clear
3) Function (F) register and translator
4) Status (S) register and status gates
5) Longitudinal count (L) register
6) Frame time generator (FTG)
7) EOR counter
8) Start sequence
9) Character control
10) Write control
11) Read control
12) Buffer control

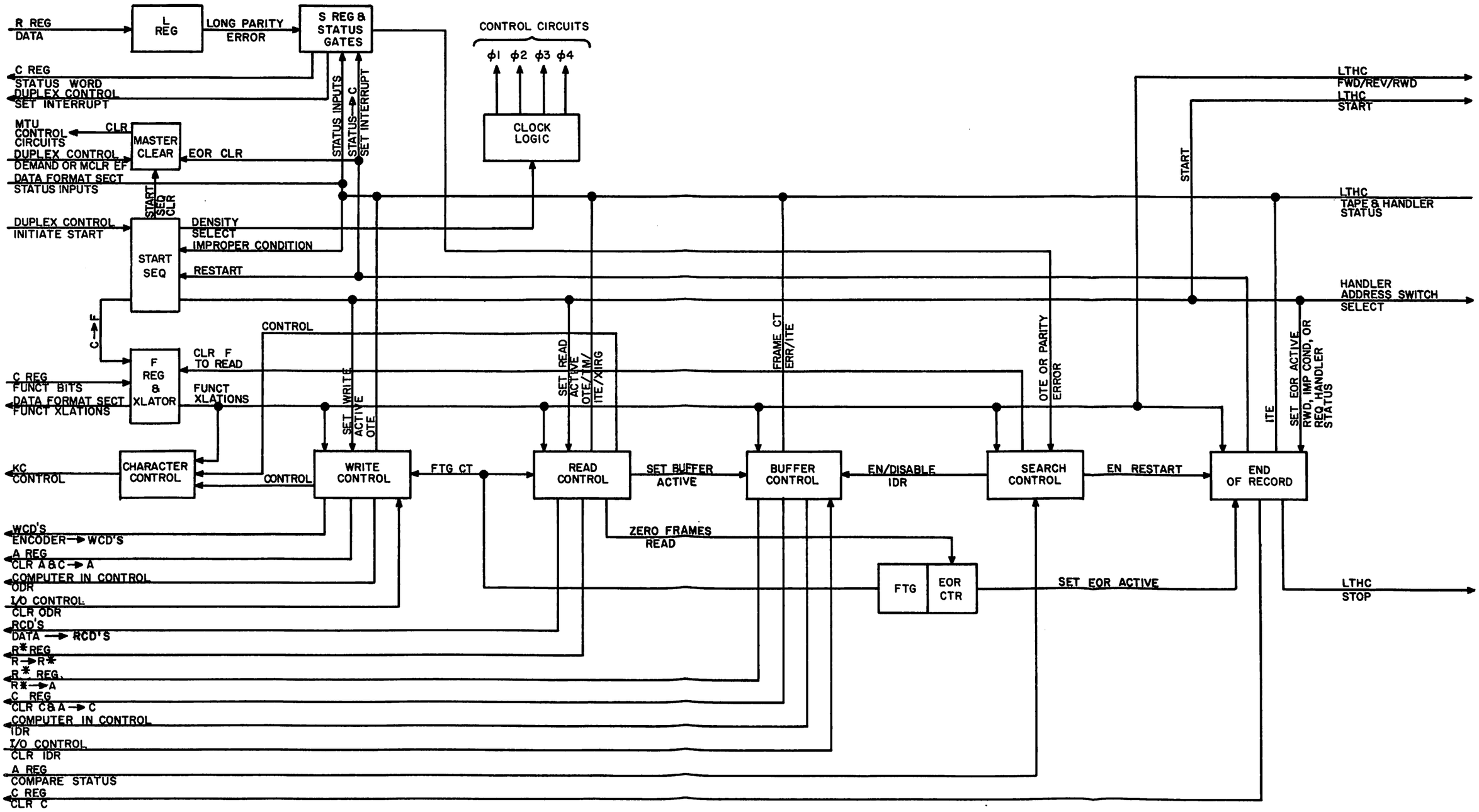


Figure 4-4. Primary Control Subsection, Block Diagram

13) End of record

14) Search control

1. CLOCK LOGIC. - The clock logic provides the basic timing pulses which are used throughout the magnetic tape control section to sequence the operational functions. The clock is basically a crystal-controlled, four-stage timing chain with the cycle time and phase duration dependent upon the density selection. Phase 1, phase 2, phase 3, and phase 4 are produced each clock cycle.

2. MASTER CLEAR. - The master clear circuits, when activated, prepare the MTU to start a new operation by clearing the various registers, counters, and control circuits. The master clear circuits are activated by power on, a demand control EF, or by a MASTER CLEAR switch on the upper maintenance and control panel. The start sequence and end of record utilize separate circuit groups within the master clear to clear specified circuit groups.

3. F REGISTER AND TRANSLATOR. - The F register is an 11-stage register which stores the parts of the external function command (from the computer) that will be required while performing a specified operation. The upper five stages of the F register store the operation code. The lower two stages of the F register store the bias designator bits. The remaining stages store the format designators which are the modulus, redundant, and parity designators. The F translator consists of a group of circuits that provides translations of the F register contents to the various control circuits that require them.

4. S REGISTER AND STATUS GATES. - The S register is a six-stage register which stores certain status information for use by the control circuits and/or later transmission, by way of the status gates and the C register, to the computer.

5. LONGITUDINAL COUNT (L) REGISTER. - The L register is a seven-stage register. Flip-flop toggle circuits control the input to each stage. It is used to maintain a record of the 1's (longitudinal parity) that are recorded in each of the seven recorded channels.

6. FRAME TIME GENERATOR (FTG). - The FTG is a four-stage binary counter which is controlled by the clock. It regulates the operation of write control and thus controls the frequency with which the frames of data are recorded on tape. The FTG is also used within read control for gating the data, read from tape, from the R register into the R* register. When reading zero frames in an interrecord gap, the FTG advances the EOR counter once for each frame period.

7. EOR COUNTER. - The EOR counter is a four-stage counter. Each of its stages is set, in turn, by the FTG each time a zero frame is read from the tape. When the EOR counter's lower three stages are set, it enables initiation of the end-of-record sequence for terminating the operation. The fourth stage provides an output that is used within the end-of-record sequence.

8. START SEQUENCE. - The start sequence initiates the required tape motion at the desired tape transport and the secondary control sequences needed to carry out the assigned function. The start sequence is initiated by I/O control, by way of duplex control, when a non-duplex EF is received from the computer. It gates the required portions of the function word from the C register into the F register by way of the handler select switch(es), selects the tape

transport specified by the function word, enables the specified density to control the clock logics, and starts the selected transport driving the tape in the direction specified by the operation code in the F register. After a delay for the tape to start moving, it initiates the required secondary control section(s).

9. CHARACTER CONTROL. - Character control directs the clearing, setting, and incrementing, or decrementing, of the K_C under the direction of the read or write control section in conjunction with the format designators.

10. WRITE CONTROL. - Write control provides the necessary timing and command control for processing data from the computer and transferring it to the W register for recording on tape. At the proper time, write control, by way of character control, reduces the value in the K_C and gates the output of the write encoder to the write register by way of the WCD's. As the last six bits in the A register are gated from the write encoder to the WCD's, write control effects the clearing of the A register, gates the contents of the C register (new data word from the computer) into the A register, and sends an ODR to the computer to obtain the next data word to be recorded.

11. READ CONTROL. - Read control provides the command control and timing required to process the data read from tape. It enables the data gates of the RCD's. When data is detected in the R register, read control enables buffer control, initiates character control for toggling the K_C, and gates the contents of the R register into the R* register. Buffer control, in turn, gates the R* register into the appropriate A subregister with the aid of the K_C.

12. BUFFER CONTROL. - Buffer control, initiated read control, gates the R* register into the A subregister designated by the K_C for each frame of data read from the tape. As the last frame of a computer word is assembled in the A register, buffer control clears the C register, gates the A register in parallel into the C register, and sends an IDR to the computer.

13. END OF RECORD (EOR). - The EOR is used primarily to terminate a tape operation, gate the status word into the C register, and initiate an interrupt to the computer. EOR is normally initiated by the EOR counter when the blank frames of an interrecord gap (IRG) are read. It may also be initiated at the end of the start sequence by a rewind, request transport status, or an improper condition. EOR initiates an EOR clear, clears the C register, gates status into the C register, initiates the interrupt, and sends a stop command to the local tape handler control for terminating the tape motion. EOR also provides circuits for restarting the start sequence for search file, space file, and rewind read operations. When EOR performs a restart, the normal EOR actions described above are inhibited.

14. SEARCH CONTROL. - Search control is used to control the sequence of events when a search find or a search or selective read fail occurs. For a search or selective read, a fail condition is detected when a complete word assembled in the A register does not compare with the search key or the selective read identifier; when an output timing error (OTE) occurs (the computer fails to supply the search key or selective read identifier in time); or when a lateral parity error is detected. For a fail condition, search control enables the EOR to restart the start sequence and disables the setting of the IDR. For a search find condition, search control enables the clearing of the operation code in the F register in order to permit a reading of the find record. When a 1240 mode back search find occurs, search control, by way of EOR, enables a forward restart to read the find record.

(2) TAPE TRANSPORT CONTROL SECTION(S). - See figure 4-5. Each tape transport control section performs a direct command control over its associated tape transport and provides other necessary functions as discussed in the following paragraphs. Each tape transport control section consists of a local tape transport control section, a tape handler address switch, read amplifiers, detectors, write amplifiers, and elapse time indicators.

(a) HANDLER ADDRESS SWITCH. - The HANDLER ADDRESS switch is used to select a tape transport by selecting its associated local tape transport control. When the HANDLER ADDRESS switch receives a select command from the start sequence, the switch setting is compared to the address bits in the C register and, if they are identical, the associate local tape transport control is selected.

(b) LOCAL TAPE TRANSPORT CONTROL (LTTC). - The LTTC exercises direct control over one tape transport. The handler address switch selects the LTTC as described above. When the LTTC receives a start command from the start sequence, it analyzes the tape motion requirements of the function translation received from the F register and sends the appropriate "go" command(s) to the tape transport. When a rewind is specified and the tape transport indicates a low tape condition, LTTC commands a fast rewind. Tape status and transport status information is received from the tape transport and relayed, by way of the LTTC, to the S register or status gates. When a read type or write operation is specified, the LTTC enables the read detectors. The write amplifiers are also enabled for a write operation. A stop signal from EOR causes the LTTC to remove the "go" signal from the tape transport and the tape motion ceases.

(c) READ AMPLIFIERS AND DETECTORS. - The read amplifiers receive the small signals generated by the channel read heads, amplify them, and send them to the detectors. The detectors (enabled by their associated LTTC) further amplify the signals, shape them, and send them to the associated R register stages in magnetic tape control by way of the RCD's. The read heads are enabled by the read amplifiers whenever the power is turned on, but the read information is not available until the detectors are enabled by LTTC.

(d) WRITE AMPLIFIERS. - The write amplifiers, when enabled by LTTC, enable the write heads. The data received from the W register is amplified for driving the write head.

(e) ELAPSE TIME INDICATORS. - The elapse time indicators (M1/M2) provide a means of measuring the actual time of tape movement across the read/write heads (see figures 4-5, 8-73, and 8-76).

(3) TAPE TRANSPORT(S) - See figure 4-5. The tape transports perform the physical function of moving the tape in the direction, and at the speed, dictated by the LTHC. The transport heads perform the function of writing magnetically on the tape or of reading previously recorded data from the tape.

b. MTU COMPUTER INTERFACE. - See figure 4-6. The MTU communicates with the computer through two channels (cables): a normal computer output channel and a normal computer input channel.

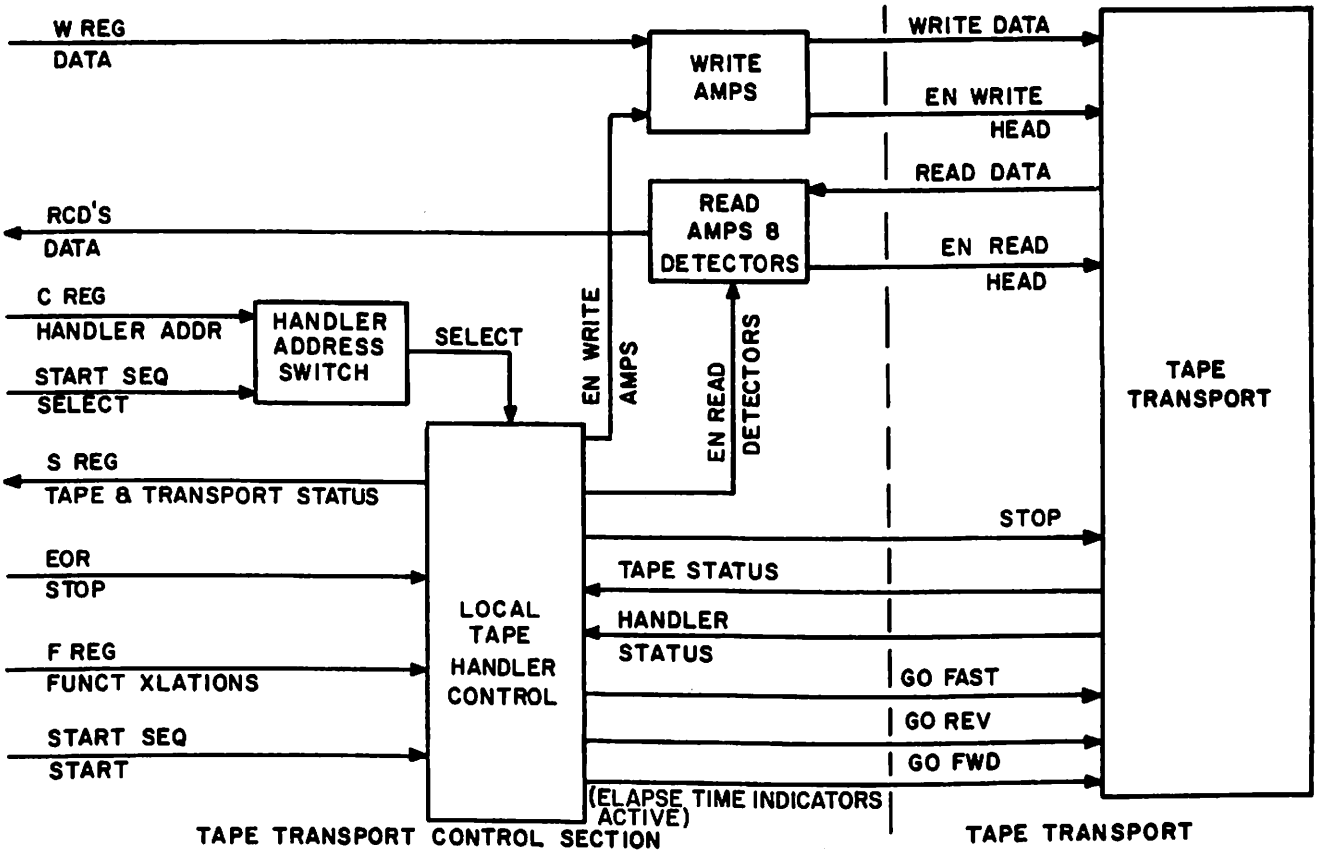


Figure 4-5. Tape Transport Control Section and Tape Transport, Block Diagram

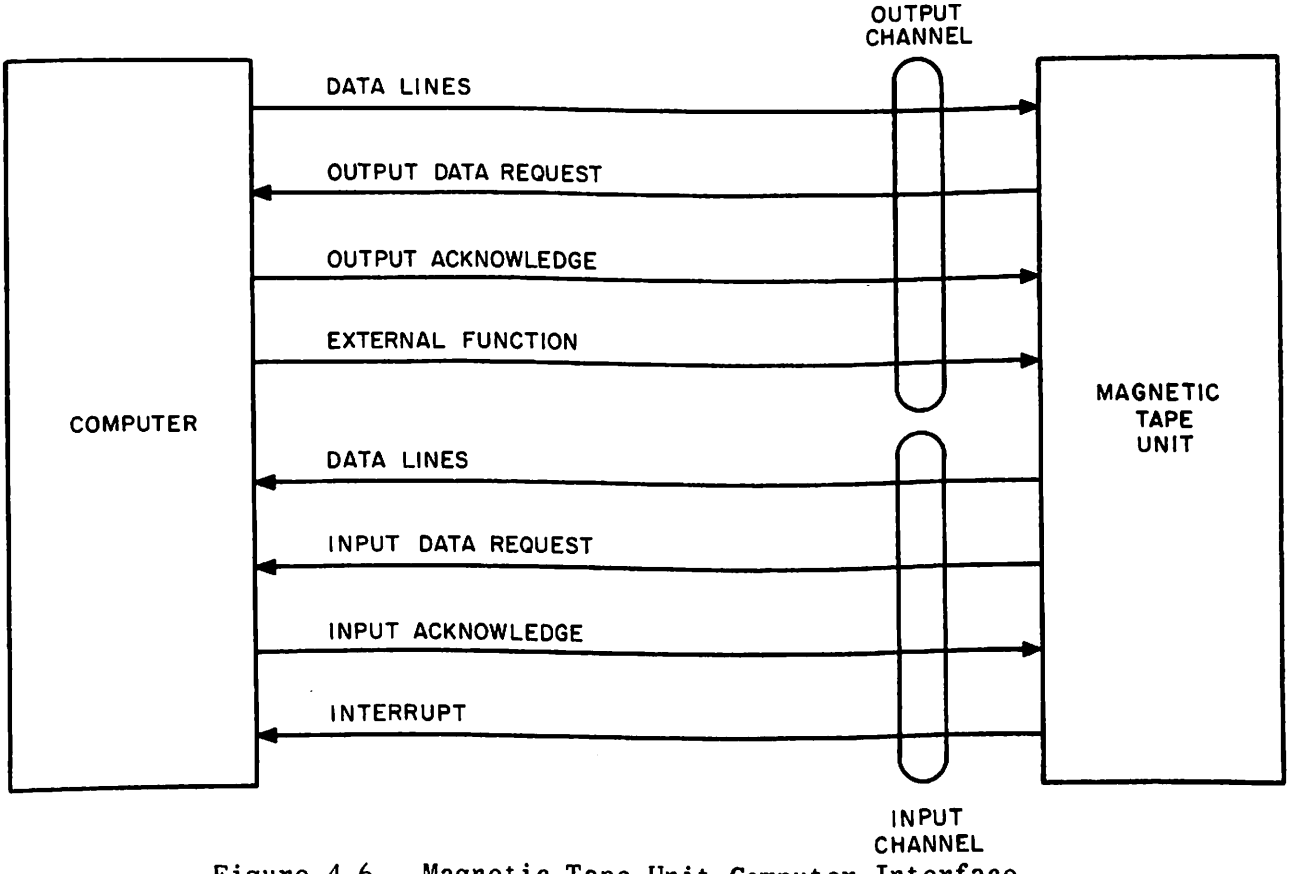


Figure 4-6. Magnetic Tape Unit-Computer Interface

(2) TAPE TRANSPORT CONTROL SECTION(S). - See figure 4-5. Each tape transport control section performs a direct command control over its associated tape transport and provides other necessary functions as discussed in the following paragraphs. Each tape transport control section consists of a local tape transport control section, a tape handler address switch, read amplifiers and detectors, and write amplifiers.

(a) HANDLER ADDRESS SWITCH. - The HANDLER ADDRESS switch is used to select a tape transport by selecting its associated local tape transport control. When the HANDLER ADDRESS switch receives a select command from the start sequence, the switch setting is compared to the address bits in the C register and, if they are identical, the associate local tape transport control is selected.

(b) LOCAL TAPE TRANSPORT CONTROL (LTTC). - The LTTC exercises direct control over one tape transport. The handler address switch selects the LTTC as described above. When the LTTC receives a start command from the start sequence, it analyzes the tape motion requirements of the function translation received from the F register and sends the appropriate "go" command(s) to the tape transport. When a rewind is specified and the tape transport indicates a low tape condition, LTTC commands a fast rewind. Tape status and transport status information is received from the tape transport and relayed, by way of the LTTC, to the S register or status gates. When a read type or write operation is specified, the LTTC enables the read detectors. The write amplifiers are also enabled for a write operation. A stop signal from EOR causes the LTTC to remove the "go" signal from the tape transport and the tape motion ceases.

(c) READ AMPLIFIERS AND DETECTORS. - The read amplifiers receive the small signals generated by the channel read heads, amplify them, and send them to the detectors. The detectors (enabled by their associated LTTC) further amplify the signals, shape them, and send them to the associated R register stages in magnetic tape control by way of the RCD's. The read heads are enabled by the read amplifiers whenever the power is turned on, but the read information is not available until the detectors are enabled by LTTC.

(d) WRITE AMPLIFIERS. - The write amplifiers, when enabled by LTTC, enable the write heads. The data received from the W register is amplified for driving the write head.

(3) TAPE TRANSPORT(S) - See figure 4-5. The tape transports perform the physical function of moving the tape in the direction, and at the speed, dictated by the LTHC. The transport heads perform the function of writing magnetically on the tape or of reading previously recorded data from the tape.

b. MTU COMPUTER INTERFACE. - See figure 4-6. The MTU communicates with the computer through two channels (cables): a normal computer output channel and a normal computer input channel.

(1) COMPUTER OUTPUT CHANNEL. - The computer output channel carries function commands and parallel output data from the computer to the MTU. The channel consists of data lines, an output data request line, an output acknowledge line, and an external function line.

(2) COMPUTER INPUT CHANNEL. - The computer input channel carries equipment status information and parallel input data from the MTU to the computer. The channel consists of data lines, an input data request line, an input acknowledge line, and an interrupt line.

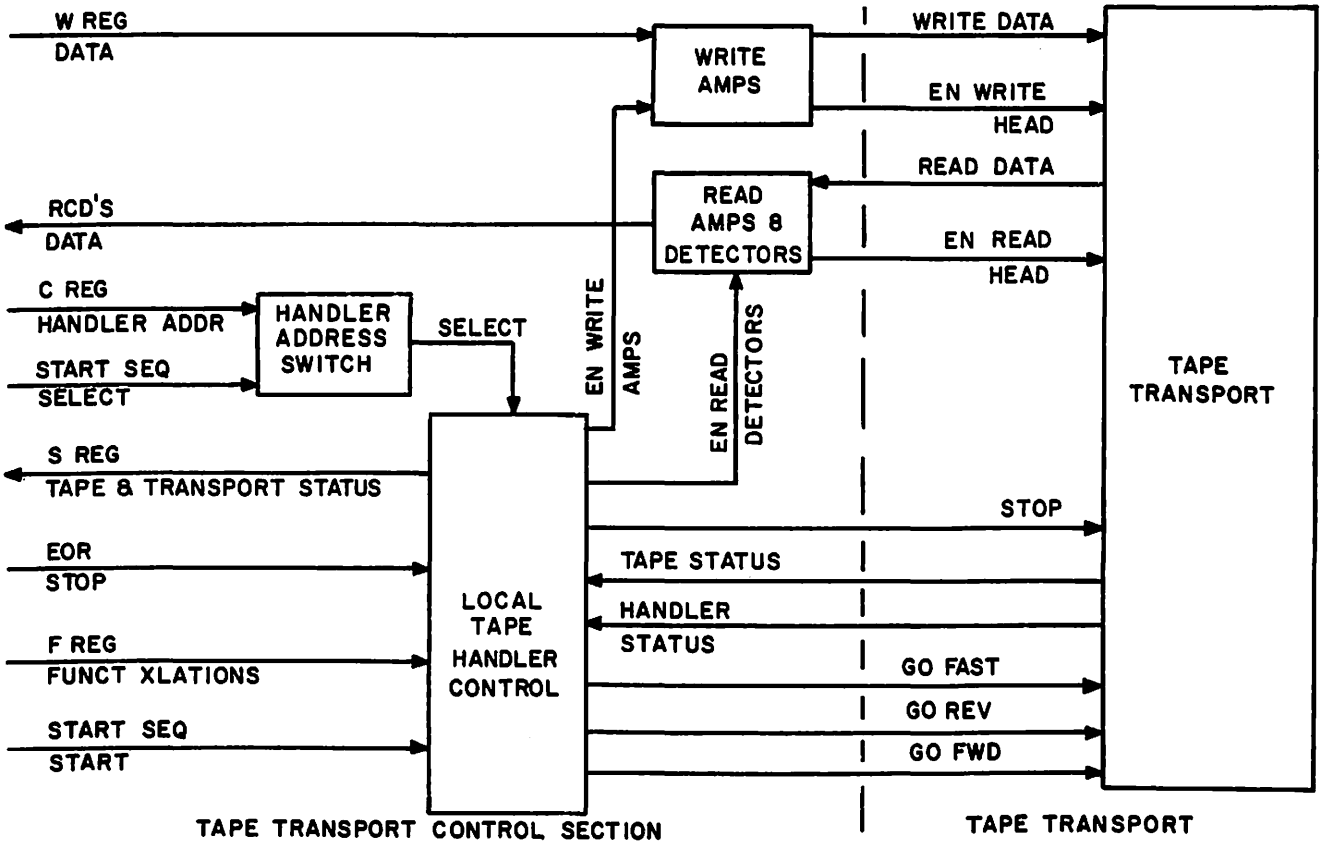


Figure 4-5. Tape Transport Control Section and Tape Transport, Block Diagram

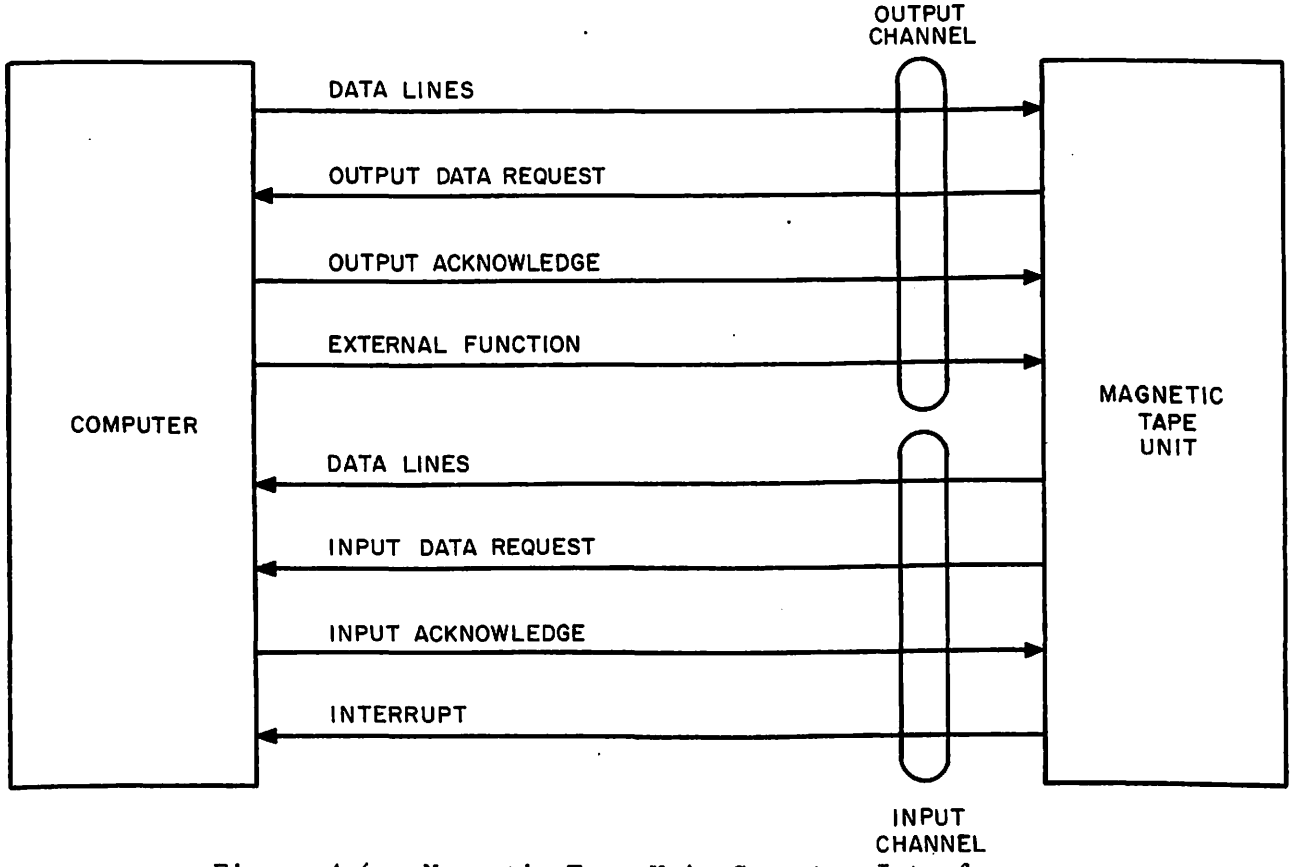


Figure 4-6. Magnetic Tape Unit-Computer Interface

(1) COMPUTER OUTPUT CHANNEL. - The computer output channel carries function commands and parallel output data from the computer to the MTU. The channel consists of data lines, an output data request line, an output acknowledge line, and an external function line.

(2) COMPUTER INPUT CHANNEL. - The computer input channel carries equipment status information and parallel input data from the MTU to the computer. The channel consists of data lines, an input data request line, an input acknowledge line, and an interrupt line.

The timing, voltage levels, current, and transition time requirements for the MTU-computer interface are contained in the technical manual for the particular type of computer being used with the MTU. Refer to table 1-1.

c. WORD FORMATS. - The MTU communicates with the computer in the request acknowledge mode. The computer issues commands to the MTU by means of the external function signal and an instruction (function) word. The magnetic tape control (MTU) section inspects the instruction word and performs the specified operation(s).

The operations stated in the instruction word are of six basic types: duplex selection, read, search, write, space file, and rewind. The basic operations are supplemented by transport selection, bias selection, format designators, and density designators, as applicable.

The MTU is capable of communicating with only one tape transport at a particular moment. Starting from a master cleared state, the general sequence of events is as follows.

1) The computer issues an instruction word by way of the external function command.

2) The MTU samples the instruction word and selects the addressed tape transport.

3) The operations stated in the instruction word are initiated and carried to completion.

4) The MTU interrupts the computer with a status word.

5) The MTU issues a stop command to the tape transport.

6) The computer samples the status word and acknowledges the interrupt.*

(1) EXTERNAL FUNCTION WORD CODES. - The EF word contains, in coded form, the instructions to be carried out by the MTU. The elements of the EF word are the duplex control code, operation code, tape transport address code, format designator codes (modulus, character, and parity), density code, bias designator codes, and the computer-originated master clear codes. Figure 4-7 shows the EF function word format and the following paragraphs discuss each of the instruction codes.

(a) EF MASTER CLEAR (Bits 16 and 17). - A master clear of the MTU is performed when the computer in control issues a function word with bits 16 and 17 containing logic 1's. The master clear differs from the other operations in two respects: it has priority over all of the other operations in the function word, and it does not result in a status interrupt to the issuing computer. The master clear will send a loss of control interrupt to another computer if this other computer has control at the time.

Master clear stops all tape motion (except a rewinding tape) and leaves the MTU in an idle state. Since master clear is not considered a normal operation, its use should be restricted to the times when the MTU is believed to be in an illogical state or when the state of the MTU cannot be determined.

(b) DUPLEX CONTROL (Bits 16 and 17). - The duplex control codes provide for non-duplex operation, release duplex control, request duplex control, and demand

* (Items 5 and 6 may be interchanged, or take place simultaneously.)

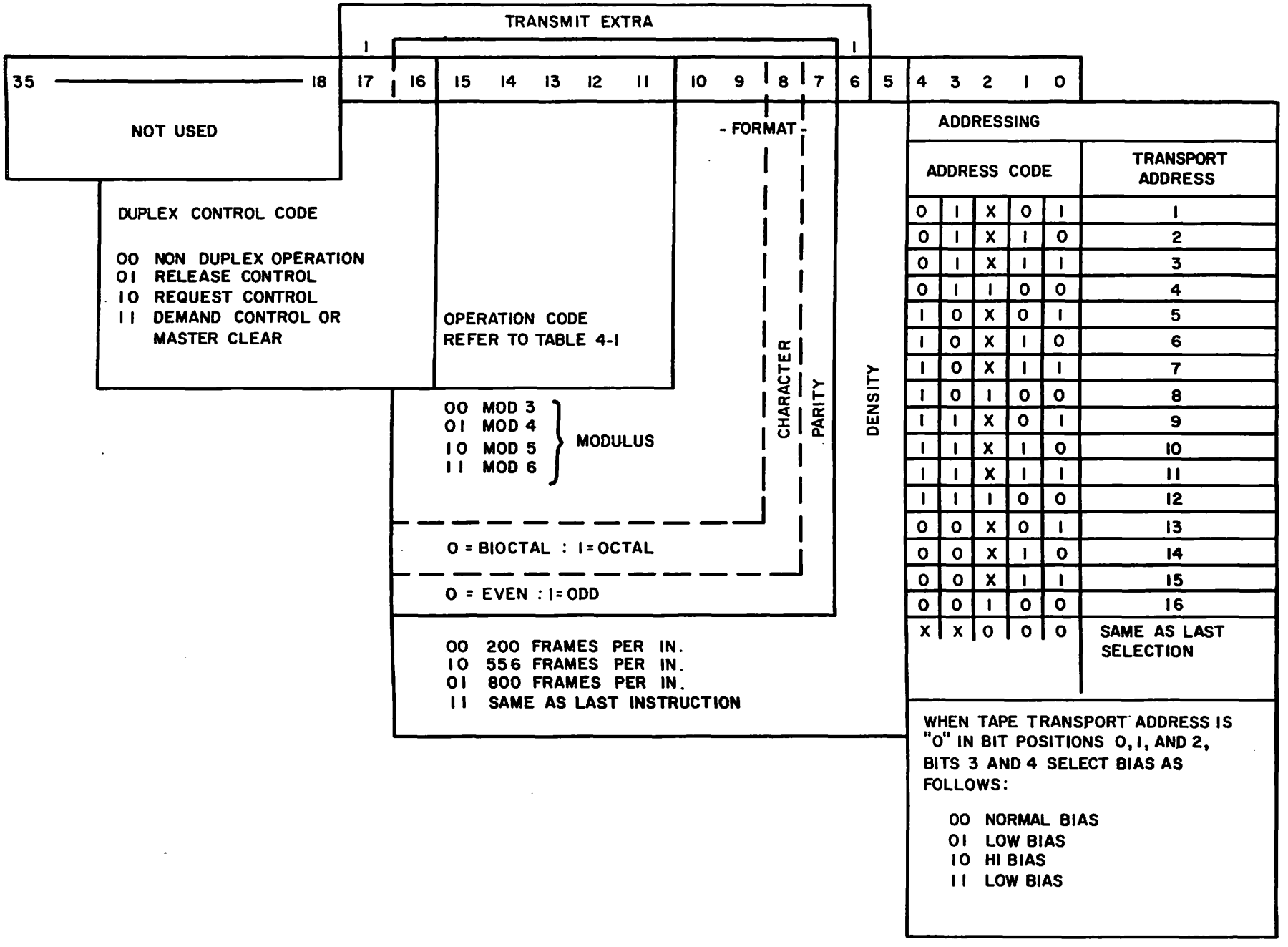


Figure 4-7. External Function Word Format

duplex control. The duplexer is optional equipment in the MTU. No special programming considerations are required if the duplexer is not installed.

1. NON-DUPLEX OPERATION. - Non-duplex operation is specified when bits 16 and 17 of the EF word are both 0's. This is the only duplex control code that permits a tape operation to be initiated. If the MTU is not equipped with a duplexer or if the computer initiating the non-duplex operation has previously established duplex control, the MTU accepts the EF word and carries the operations specified to completion. If the computer initiating the non-duplex operation is not in duplex control (possible in duplexer operation only), the MTU interrupts that computer with a not-in-control status indication.

2. RELEASE CONTROL. - If the computer that is in duplex control sends an EF word to the MTU with a 1 in bit 16 and a 0 in bit 17, the MTU places the duplexer, for that computer, in a neutral or not-in-control status. A release control EF from a computer that is not in control has no effect on the MTU.

3. REQUEST CONTROL. - If neither computer is in duplex control, an EF word with a 0 in bit 16 and a 1 in bit 17 causes the MTU to place the computer issuing the EF in control of the MTU. The MTU then issues a status interrupt to the originating computer to notify it that it has established control. If the computer initiating the request control EF is already in control, the MTU issues a status interrupt to that computer notifying it that it is in control. If computer A requests control and computer B is in control, the MTU stores the request for control until computer B releases control. The MTU then places computer A in control and notifies computer A by way of status interrupt that it is in control.

4. DEMAND CONTROL. - The EF demand control consists of 1's in bit positions 16 and 17 of the EF word. If computer B is in control and computer A sends an EF demand control, the MTU stops any current operation by master clearing. Computer A is placed in control and computer B is notified of the loss of control by way of the status interrupt. No interrupt is sent to computer A. If neither computer is in control when a demand is received, the MTU places the demanding computer in control. No interrupt is issued to either computer. Issuance of a demand control code by a computer that is in control is an EF master clear. Refer to paragraph 4-1c(1)(a).

(c) OPERATION CODE (Bits 11 through 15). - The magnetic tape operations to be performed by the MTU are defined by the operation code. The basic operations defined in the operation code are read, search, space file, write, rewind, and request transport status. Table 4-1 provides a translation of the operation codes for 1540 and 1240 modes. The following paragraphs explain the functions commanded by the operation codes.

1. READ. - The read function is supplemented by the proper selection of format and density. Two types of read operations are performed: normal read and selective read.

The selected tape transport moves the tape at normal speed in the forward direction and transfers 7-bit frames (read from tape) to the MTC. Depending on the format, the frames are checked for proper parity and assembled into computer words. (The size of the assembled words depends on the moduli selection.) The assembled computer word is placed on the data lines of the input cable, and an IDR signal is sent. The computer senses the IDR, samples the data lines at its convenience, and returns an input acknowledge to the MTU. Because the tape continues to move and a new word is being assembled (until end of record is reached), the computer should

acknowledge the IDR within a specified time to prevent the loss of one or more words in the record. The time is dependent on the format and density (refer to table 4-2). If the computer fails to acknowledge the IDR within the allotted time, an input timing error (ITE) occurs. The computer is informed of an input timing error by the status interrupt word at the end of the read function. The error indication is received by the computer when the status interrupt is sent.

For a selective read operation, an ODR is sent to the computer during the start operations to obtain the selective read identifier. In response to the ODR, the computer returns the selective read identifier which is stored in bit positions 0 through 5 of the C register until the operation is terminated by an end of record.

TABLE 4-1. OPERATION CODES, 1540 AND 1240 MODES

FUNCTION BITS					FUNCTION CODES	
15	14	13	12	11	1540	1240
0	0	0	0	0	READ	READ
0	0	0	0	1	READ, SELECTIVE	READ, SELECTIVE
0	0	0	1	0	READ, MODIFIED STOP	READ, IGNORE ERROR HALT
0	0	0	1	1	SPACE FILE	SPACE FILE
0	0	1	0	0	SEARCH, TYPE I	SEARCH, TYPE I
0	0	1	0	1	SEARCH, TYPE II	SEARCH, TYPE II
0	0	1	1	0	SEARCH FILE, TYPE I	SEARCH FILE, TYPE I
0	0	1	1	1	SEARCH FILE, TYPE II	SEARCH FILE, TYPE II
0	1	0	0	0	WRITE	WRITE
0	1	0	0	1	WRITE, XIRG	WRITE, XIRG
0	1	0	1	0	WRITE, IGNORE ERROR HALT	WRITE, IGNORE ERROR HALT
0	1	0	1	1	WRITE, XIRG-IGNORE ERROR HALT	WRITE, XIRG-IGNORE ERROR HALT
0	1	1	0	0	WRITE, MODIFIED STOP	WRITE, TAPE MARK
0	1	1	0	1	WRITE, EDIT	WRITE, TAPE MARK, XIRG
0	1	1	1	0	WRITE, TAPE MARK	WRITE, TAPE MARK
0	1	1	1	1	WRITE, TAPE MARK, XIRG	WRITE, TAPE MARK, XIRG
1	0	0	0	0	BACK READ	BACK SPACE
1	0	0	0	1	BACK READ, SELECTIVE	BACK SPACE
1	0	0	1	0	BACK READ, MODIFIED STOP	BACK SPACE-READ
1	0	0	1	1	BACK SPACE, FILE	BACK SPACE, FILE
1	0	1	0	0	BACK SEARCH, TYPE I	BACK SEARCH, TYPE I
1	0	1	0	1	BACK SEARCH, TYPE II	BACK SEARCH, TYPE II
1	0	1	1	0	BACK SEARCH FILE, TYPE I	BACK SEARCH FILE, TYPE I
1	0	1	1	1	BACK SEARCH FILE, TYPE II	BACK SEARCH FILE, TYPE II

TABLE 4-1. OPERATION CODES, 1540 AND 1240 MODES (Cont.

FUNCTION BITS					FUNCTION CODES	
15	14	13	12	11	1540	1240
1	1	0	0	0	REWIND	REWIND
1	1	0	0	1	REWIND, CLEAR WRITE ENABLE	REWIND, CLEAR WRITE ENABLE
1	1	0	1	0	REWIND	REWIND
1	1	0	1	1	REWIND, CLEAR WRITE ENABLE	REWIND, CLEAR WRITE ENABLE
1	1	1	0	0	REWIND-READ	REWIND-READ
1	1	1	0	1	REWIND-READ, CLEAR WRITE ENABLE	REWIND-READ, CLEAR WRITE ENABLE
1	1	1	1	0	REWIND-READ	REWIND-READ
1	1	1	1	1	REQUEST HANDLER STATUS	REWIND-READ-CLEAR WRITE ENABLE

TABLE 4-2. WORD ASSEMBLY TIMES

FORMAT		WORD ASSEMBLY TIME		
MODULUS	CHARACTER	AT 200 BPI (usec)	AT 556 BPI (usec)	AT 800 BPI (usec)
3	Bioctal	125	45	31.2
4	Bioctal	167	60	41.6
5	Bioctal	208	75	52.0
6	Bioctal	250	90	62.4
3	Octal	250	90	62.4
4	Octal	334	120	83.2
5	Octal	416	150	104.0
6	Octal	500	180	124.8

During the selective read process, the MTC compares the lower six bits of each assembled word with the selective read identifier in the C register. If the comparison is not satisfied, the assembled word is discarded. If the lower six bits of the assembled word are identical to the identifier, the comparison is satisfied and the assembled word is sent to the computer. An output timing error (OTE) is recognized if the selective read identifier is not provided by

the computer before the second frame of data is read from tape. Both the OTE and parity error inhibit the transmissions to the computer. An ITE allows data transfers to be performed and the computer is notified by a status interrupt.

The read modified stop, used in a forward direction, delays the stopping of the tape transfer for an additional 0.3 inch of tape travel. The modified stop gives the computer time to initiate a new forward function without a stop signal actually being applied to the tape transport. If a new forward function is not received immediately, the tape stops after moving an additional 0.3 inch into the IRG.

The backread and backread selective operations function in the same manner as the read and read selective operations except that the tape movement is in a reverse direction and the computer receives the words of the record in reverse order.

A modified stop for a backread results in the tape's stopping at a point where the head is positioned 0.072 inch less than normal into the IRG. This can be useful for obtaining access to an abnormally short IRG for reading an associated record.

2. SEARCH. - The search function combines the features of a normal read with the MTC's ability to compare the first word of each record read (in either the forward or reverse direction) with an identifier word. When a find is made, that record is transferred to the computer. The search comparison is performed on the first word of a record with a search key word. The search key is obtained from the computer in the same manner as the read selective identifier. The search key, however, is a full-sized computer word. The two types of search comparisons are Type I, ones compare, and Type II, identical compare.

If a parity error occurs before a find is made, the tape unit aborts the search and stops in the next IRG. The computer is notified by an interrupt status.

The ones compare (Type I) is defined as a bit-per-bit, greater-than-or-equal-to compare. The following example demonstrates this definition. For explanatory purposes only, the example uses 6-bit words.

EXAMPLE

Search Key:	001101	
Find	: 011101	Bits 0, 2, and 3 compare
Find	: 001101	Bits 0, 2, and 3 compare
Find	: 001111	Bits 0, 2, and 3 compare
No Find	: 010101	Bit 3 does not compare
No Find	: 001100	Bit 0 does not compare

An identical compare (Type II) is defined as a search comparison in which the search key and the first word of the record read are exactly identical. An output

timing error occurs if the MTU does not receive the search key before reading the second frame of the record. The MTU terminates the search operation when it detects an error. The computer is informed of the error by a status interrupt when the end of record is reached. The tape is then positioned in the IRG before or after the record in which the error occurred, depending on the direction of the search.

An input buffer is also required to read the find record. The total search capability of the MTU is the sum of the capabilities outlined as follows.

a) SEARCH FORWARD/BACKWARD. - The search forward/backward operation may be within a Type I or Type II comparison depending on which operation code is used in the instruction word. The instruction word is sent to the MTU, by means of the EF command, and is executed in the normal manner. It is followed by a one-word output buffer with the search key from the computer. The search key is then stored in the MTC where the search comparison takes place. The MTU reads continuously, transferring the first word of each record to the MTU until a search comparison is satisfied. A normal read is then performed for the balance of the find record. If the back search operation is specified in the instruction word, the tape movement is backward. When a search comparison is made, a normal backread operation transfers the record to the computer.

b) SEARCH FILE FORWARD/BACKWARD. - The search file instruction performs the same function as the search forward/backward except that the search operation is limited to a file (see figure 4-8). A file is defined as one or more records separated from the succeeding file by a tape mark. The difference between search and search file is that a search file instruction is terminated if a tape mark is detected before a search comparison is satisfied. The computer is informed, by means of a status interrupt indicating tape mark, that the comparison was not satisfied.

The tape mark is a one-frame record which is used to separate files of information. It appears on the tape as binary 0 001 111 following an interrecord gap. Longitudinal parity follows three frames later.

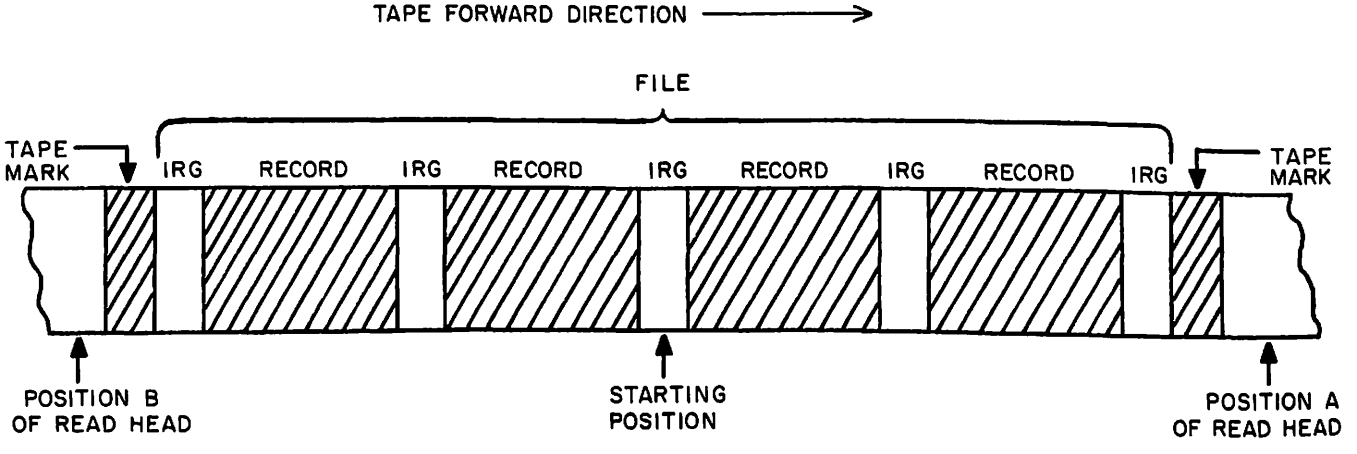


Figure 4-8. Search/Space File

3. SPACE FILE FORWARD/BACKWARD. - When instructed to space file, the MTU causes the addressed tape transport to move the tape in the specified direction and to stop with the tape positioned beyond the first tape mark encountered (see figure 4-8). The MTU stops and notifies the computer, by way of a status interrupt, of a tape mark indication.

From the starting position, when instructed to space file forward, the tape stops when it is positioned at B. When instructed to back space file the tape stops when it is positioned at A (see figure 4-8).

4. WRITE. - The write function is supplemented by format and density. The selected tape transport moves the tape forward at normal speed. The MTU takes words from the output data lines, disassembles them into 6-bit characters according to the modulus selection, generates frame parity, and transfers each seven bits to the tape transport for recording in a frame on tape. The read head then reads back each frame, in turn, and performs a parity check. If a parity error is detected, the MTU halts the write operation and informs the computer, by way of a status interrupt, that an error in recording has been detected, unless a write, ignore error halt function is used.

When the MTC recognizes a write function, an output data request is sent to the computer. The computer, at its convenience, places data on the output lines and responds with an output acknowledge. The MTU recognizes the output acknowledge, samples the data lines, and removes the ODR. MTC disassembles the word and starts the writing process. When the word is transferred to the disassembly register, another ODR is issued. This process continues until the computer no longer acknowledges the ODR within time sufficient to allow another word to be written. The time allotted is dependent on the format and density (refer to table 4-2). This situation is recognized as an end of write (EOW) and the recording is terminated. If the computer acknowledges an ODR after the allotted time, the MTC senses an output timing error and notifies the computer by way of a status interrupt. When the MTC detects EOW, it stops the tape motion allowing for an interrecord space of approximately 3/4-inch. The MTU then removes the ODR, places a status word on the input lines, and sets the interrupt line. The computer samples the status word and acknowledges the interrupt, whereupon the MTU becomes idle. Variations to the write operation such as ignore-error-halt, tape mark, edit, modified stop, and extended interrecord gap functions are possible. When instructed to write-ignore-error-halt, the MTU will not stop the write operation if a lateral parity error is detected.

The extended interrecord gap feature causes a 3-1/2 inch IRG to be written in place of the normal 3/4-inch IRG. This extended gap precedes the record specified by the instruction word.

When instructed to write-tape-mark, the parity and character is ignored, and a file marker (tape mark) is recorded on tape. The tape mark is modulus sensitive.

The write edit operation is used to write over an existing record. The performance is the same as a normal write except that the erase head is not energized and certain programming restrictions are placed on the operation. Refer to paragraph 4-1f(8).

The modified stop feature is identical to that described for a forward read.

5. REWIND. - The rewind function causes the transport to move the tape in a reverse direction to the load point.

If more than 100 feet of tape are to be rewound, the tape rewinds at a speed of 240 inches-per-second. When there are approximately 100 feet of tape left to be rewound, the tape speed reduces to the normal operational speed of 120 ips until the tape stops at the load point. If the tape is at load point when a rewind function is received, there is no tape motion and no improper status is indicated.

A rewind clear write enable causes the addressed transport to rewind in the normal manner, but does not permit a write function on that transport without manual intervention.

The rewind read instruction causes the tape on the addressed tape transport to be rewound and then causes the first record to be read and sent to the computer. The rewind read is supplemented by format and density.

6. REQUEST TRANSPORT STATUS. - The request transport status instruction causes the MTU to send a status interrupt to the computer that reflects the status of the selected tape transport.

(d) FORMAT (Bits 7 through 10). - The format portion of the instruction word consists of the modulus, character, and parity instructions. A complete format selection must be included in all of the instruction words that require a recording or reading operation. The three elements of format are discussed in the following paragraphs.

1. PARITY (Bit 7). - Two types of parity can be designated, odd and even. A 1 in bit 7 indicates odd parity and a 0 in bit 7 indicates even parity.

The parity designator causes a bit to be recorded for each frame of tape in order to make the total number of 1 bits in a frame either even or odd as designated.

2. CHARACTER (Bit 8). - Two types of character recording can be designated, octal and bioctal. A 1 in bit 8 causes each octal number in the computer word to be recorded twice in each frame for added reliability. For instance, if the computer word contained octal 01234 56701, it would appear on tape as shown in figure 4-9. Note that when recording octally a 0 is recorded as 0 111 000. When recording octally, the parity designator is ignored and odd parity is always generated. When read, the two halves of each frame are combined in an OR type function so that if a 1 bit has been dropped on the one half of the tape, it may be recovered from the other half. See figure 4-10 for an example.

A 0 in bit 8 causes two octal numbers (six bits) of the computer word to be recorded in each frame. The parity designated may be either odd or even.

3. MODULUS (Bits 9 and 10). - The MTU is capable of recording and reading in four different moduli. These moduli and their appropriate designator bits (10-9) are:

00 = Mod 3, 18-bit words

01 = Mod 4, 24-bit words

10 = Mod 5, 30-bit words

11 = Mod 6, 36-bit words

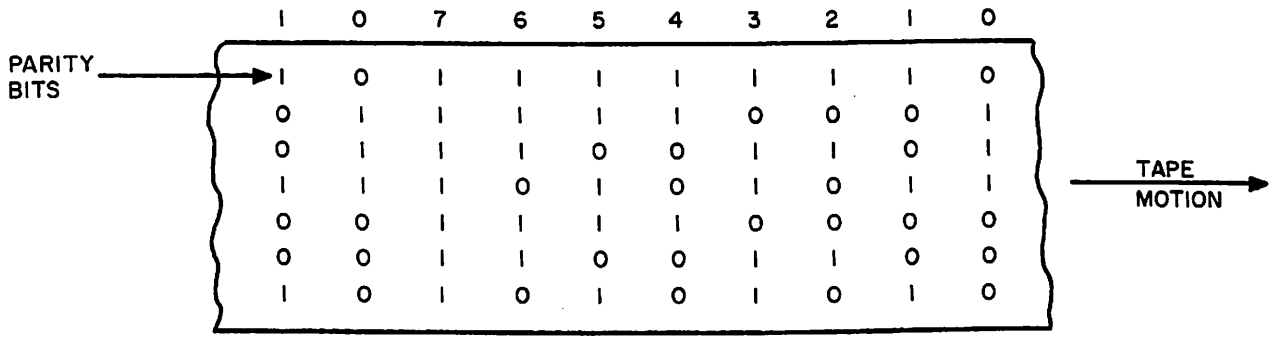


Figure 4-9. Octal Recording

ORIGINAL NUMBER = 101
READ FROM 1st HALF = 101
READ FROM 2nd HALF = 001

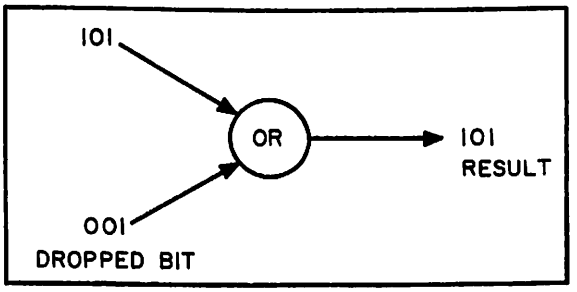


Figure 4-10. Octal Recording OR Condition

The word assembly time for each modulus is listed in table 4-2. The bit arrangement on the tape for a bioctal recording is shown in figure 4-11. The bit arrangement for an octal recording is shown in figure 4-12.

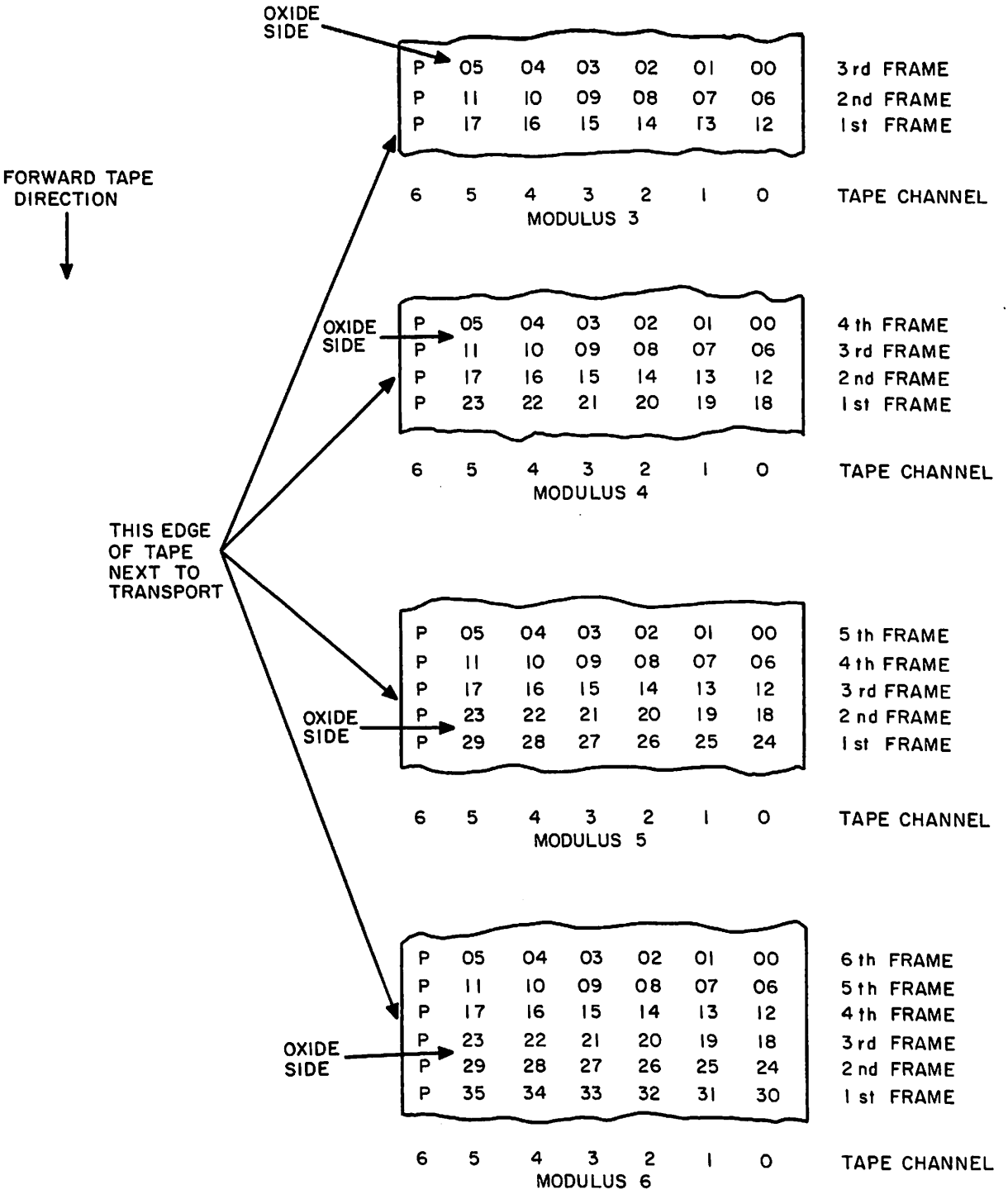


Figure 4-11. Bioctal Tape Formats

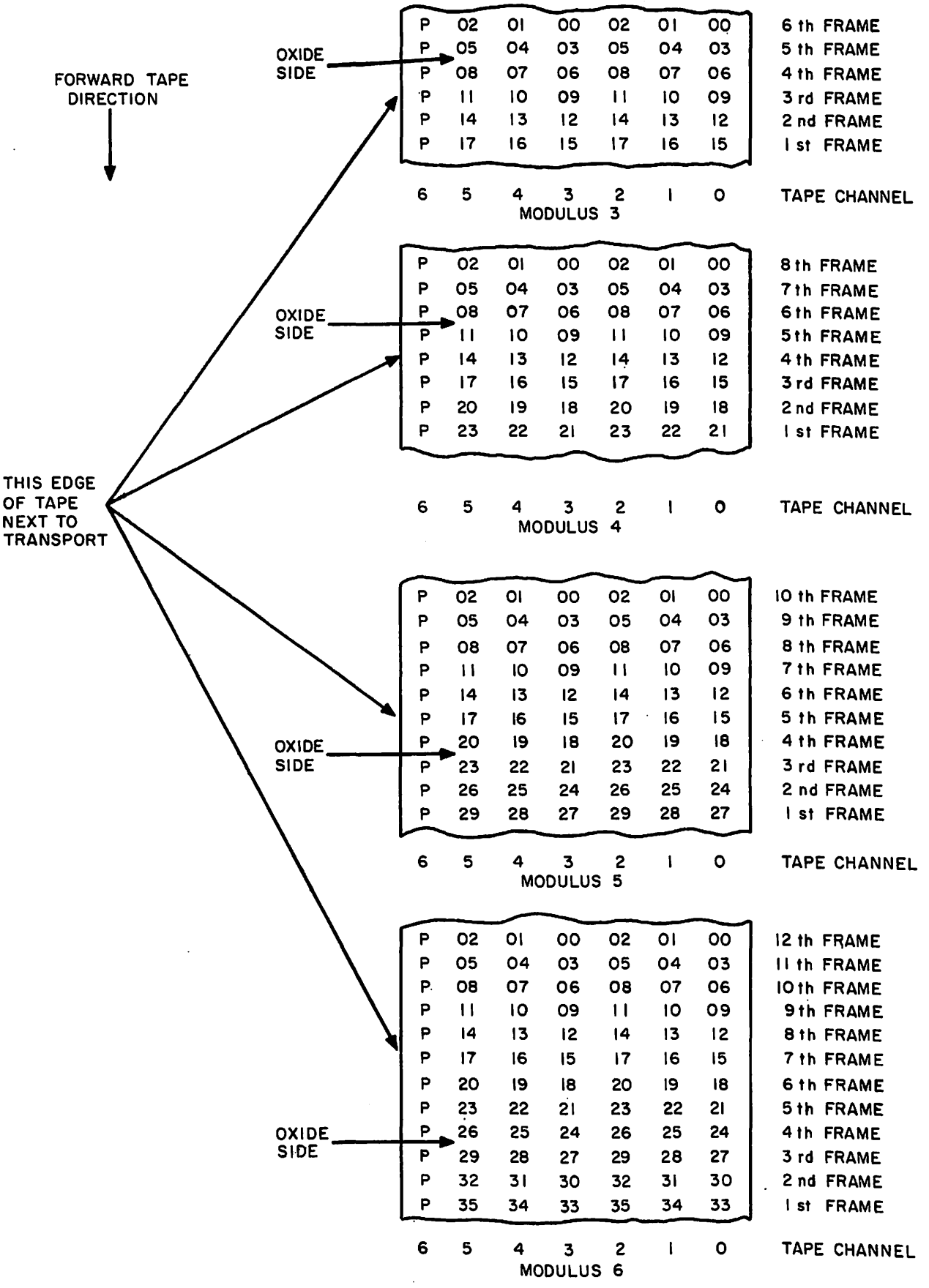


Figure 4-12. Octal Tape Formats

a) MOD 3. - Mod 3 is obtained by reducing 18 bits of a computer word to three (bioctal characters) frames of data. In reading Mod 3 bioctal a word is sent to the computer for every three characters assembled. The characters are assembled in the lower 18 bits (17-0) of the data word. The upper bits (if any) of the data word contain 0's. When reading octal, six tape frames are read to complete the computer word.

When recording Mod 3 bioctal, the 18 bits of a computer word are recorded in three 7-bit frames with each frame consisting of a 6-bit character plus parity. For octal recording, the number of tape frames is doubled.

b) MOD 4. - Mod 4 is obtained by reducing 24 bits of a computer word to four (bioctal characters) frames of data. In reading Mod 4 bioctal a word is sent to the computer for every four characters assembled. The characters are assembled in the lower 24 bits (23-0) of the data word. The upper bits (if any) of the data word contain 0's. When reading octal, eight tape frames are read to complete the computer word.

When recording Mod 4 bioctal, the 24 bits of a computer word are recorded in four 7-bit frames with each frame consisting of a 6-bit character plus parity. For octal recording, the number of tape frames is doubled.

c) MOD 5. - Mod 5 is obtained by reducing 30 bits of a computer word to five (bioctal characters) frames of data. In reading Mod 5 bioctal, a word is sent to the computer for every five characters assembled. The characters are assembled in the lower 30 bits (29-0) of the data word. The upper bits (if any) of the data word contain 0's. When reading octal, ten frames are read to complete the computer word.

When recording Mod 5 bioctal, the 30 bits of a computer word are recorded in five 7-bit frames with each frame consisting of a 6-bit character plus parity. For octal recording, the number of tape frames is doubled.

d) MOD 6. - Mod 6 is obtained by reducing 36 bits of a computer word to six (bioctal characters) frames of data. In reading Mod 6 bioctal, a word is sent to the computer for every six characters assembled. The characters are assembled in the 36 bits (35-0) of the data word. When reading octal, twelve frames are read to complete the computer word.

When recording Mod 6 bioctal, the 36 bits of a computer word are recorded in six 7-bit frames with each frame consisting of a 6-bit character plus parity. For octal recording, the number of frames is doubled.

(e) DENSITY (Bits 5 and 6). - The MTU is capable of recording data on tape in three programmable densities. These densities and their appropriate designator bits (6-5) are the following.

00 = 200 frames-per-inch

10 = 556 frames-per-inch

01 = 800 frames-per-inch

11 = Same as last instruction

(f) TRANSPORT SELECTION (Bits 0 through 4). - The transport selection code is used to select the transport whose ADDRESS switch is set on any number from one to sixteen inclusive. The maximum number of transports which can be incorporated in a Type 1540 MTU system is eight, but as many as sixteen can be incorporated in a Type 1240 MTU system. Thus, in order to establish Type 1240 program compatibility, the transport switches may be set to a number as high as sixteen. The address code for each transport address is shown in figure 4-7.

(g) BIAS SELECTION. - When bits 0 through 2 of the address code are zeros (indicating the same transport selection as the last instruction), bits 3 and 4 of the instruction word determine the biasing level for the read detectors. Four bias modes are available. These modes and their appropriate designator bits (4-3) are as follows.

00 = Normal

01 = Low

10 = Hi

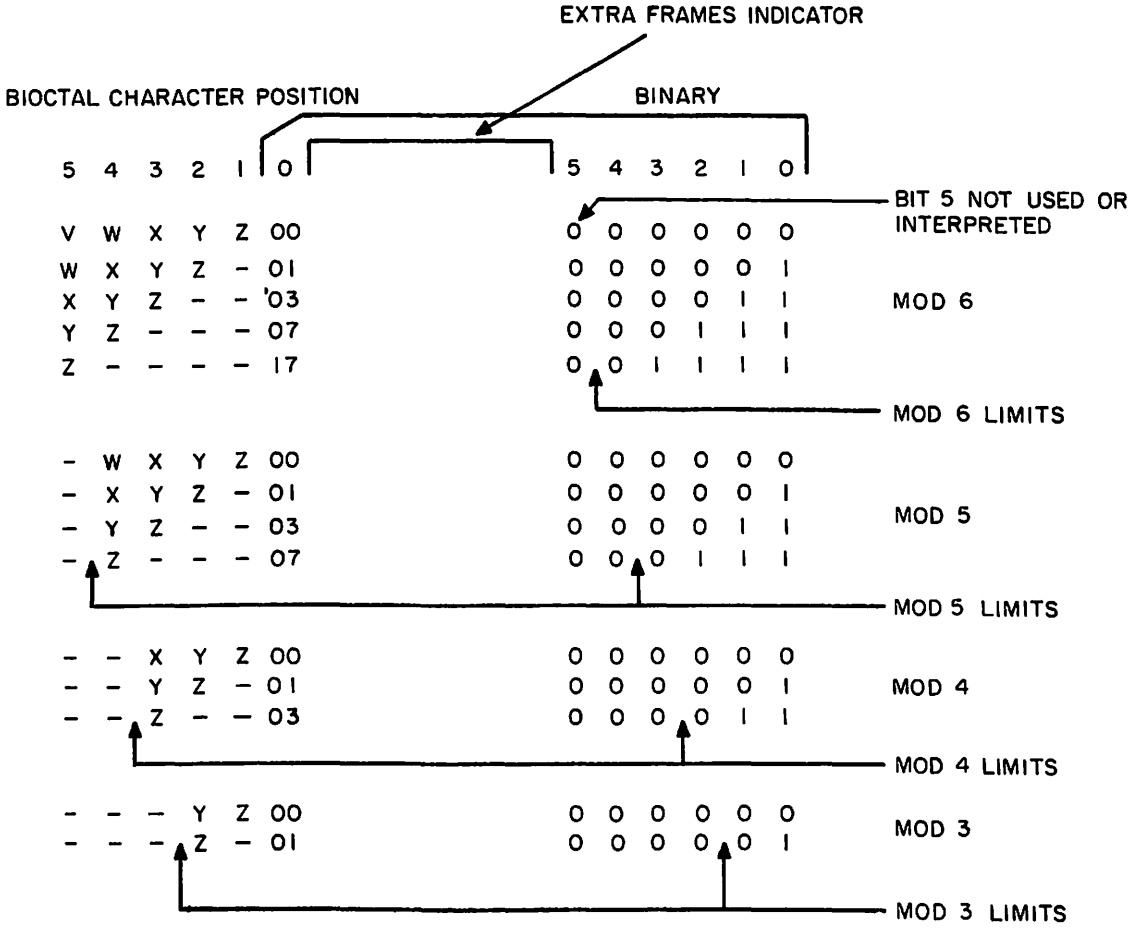
11 = Low

(h) TRANSMIT EXTRA. - The transmit extra function can only be performed after using a forward read. When reading the tape in a modulus other than the one in which it was recorded, the number of frames read may not form an integral number of computer words. When this occurs the extra frames of data have remained stored in the MTU; the status interrupt informs the computer of the error by means of a frame count error indication with correct longitudinal parity. The transmit extra code is contained in bit positions 6 and 17 of the EF word. A 1 in these bit positions is used by the computer to obtain the extra frames of data.

When the MTU senses a transmit extra command, it clears the C register, gates the extra frames from the A0 through A5 subregisters into the corresponding bit positions of the C register, (A0 is always zero since if any frames are missing, A0 will be cleared) gates the translation of the character counter into the (extra frames indicator) lower six bit positions of the C register (data lines), and sends an IDR to the computer. The computer samples the data and sends an input acknowledge that causes the MTU to clear the IDR. The computer may analyze the extra frames indicator of the data word to determine the number of extra frames it received (see figure 4-13). The extra characters in the data word are designated by a logic 0 in the bit position (within modulus limits) of the extra frames indicator that corresponds to each character position within the data portion of the computer word. For a transmit extra function, the transports are not used or interrogated and the function is not terminated by a status interrupt.

(2) STATUS WORDS. - A status word is sent to the computer following the completion of most functions specified by an operation code. It is placed on the data lines of the input cable. The bit structure of the status word enables the computer to determine whether or not the previous function has been successfully completed.

The computer program must recognize that after an EF instruction has been issued to the MTU, no subsequent command specified by an operation code will be recognized untiluntil the acknowledge to the status interrupt is received (signifies the end of the first instruction).



NOTES: Z DENOTES LAST FRAME, Y DENOTES SECOND LAST FRAME, ETC. A 0 IN THE EXTRA FRAMES INDICATOR WITHIN THE MOD LIMITS INDICATES AN EXTRA FRAME OF DATA IN THE CORRESPONDING POSITION OF THE COMPUTER WORD (WITHIN THE MOD LIMITS).

Figure 4-13. Transmit Extra Computer Word Format

Figure 4-14 illustrates the bit assignments in the status word. The upper bits are interpreted as 0's. The status word includes the conditions described in the following paragraphs.

(a) IMPROPER CONDITION (Bit 14). - A 1 in bit position 14 may imply that operator intervention is necessary to overcome the difficulty. An improper condition will occur under the following circumstances:

1) The referenced tape transport is not in an automatic condition.

2) No tape transport is selected when one is required.

3) A forward command is sent to a tape transport whose tape is positioned at end of tape.

4) A reverse command is sent to a tape transport whose tape is positioned at load point (rewind excepted).

5) A write instruction is issued to a tape transport that has no write enable.

When the computer has been notified of an improper condition, the computer program may either refrain from issuing further external function commands to the tape system to allow visual inspection of the trouble, or it may issue another external function command. An external function command to the tape unit extinguishes the improper condition indication.

If a tape transport is not in the automatic condition, one of the following situations is implied:

1) Tape transport was manually removed from automatic.

2) Tape transport is not in the ready condition for one of the following reasons:

No power, broken tape, burned-out lamp, or improperly loaded tape.

(b) DUPLEX CONTROL (Bit 13). - When bit 13 of the status word is a logic 0, it indicates to the computer receiving it that it is in control of the MTU. If an interrupt is initiated by duplex control (not a normal status interrupt), the computer should read only bit 13 of the status word; the remainder of the status word is invalid. A 1 in bit 13 of the status word indicates to the computer receiving it that it is not in control of the MTU.

(c) TRANSPORT READY (Bit 12). - A 1 in bit position 12 of the status word indicates that the selected tape transport is properly loaded with tape, powered up, and ready to operate.

(d) XIRG DETECTED (Bit 11). - A 1 in bit position 11 of the status word indicates that an XIRG was detected at the beginning of the operation for which the status interrupt was initiated (tape traveled at least an inch before detecting the data).

(e) OUTPUT TIMING ERROR (Bit 10). - A 1 in bit position 10 indicates that either the computer did not acknowledge the first ODR or the computer acknowledged an ODR too late for the data word to be written in its proper place. The acknowledge time is related to the format and density. The times shown in table 4-2 apply.

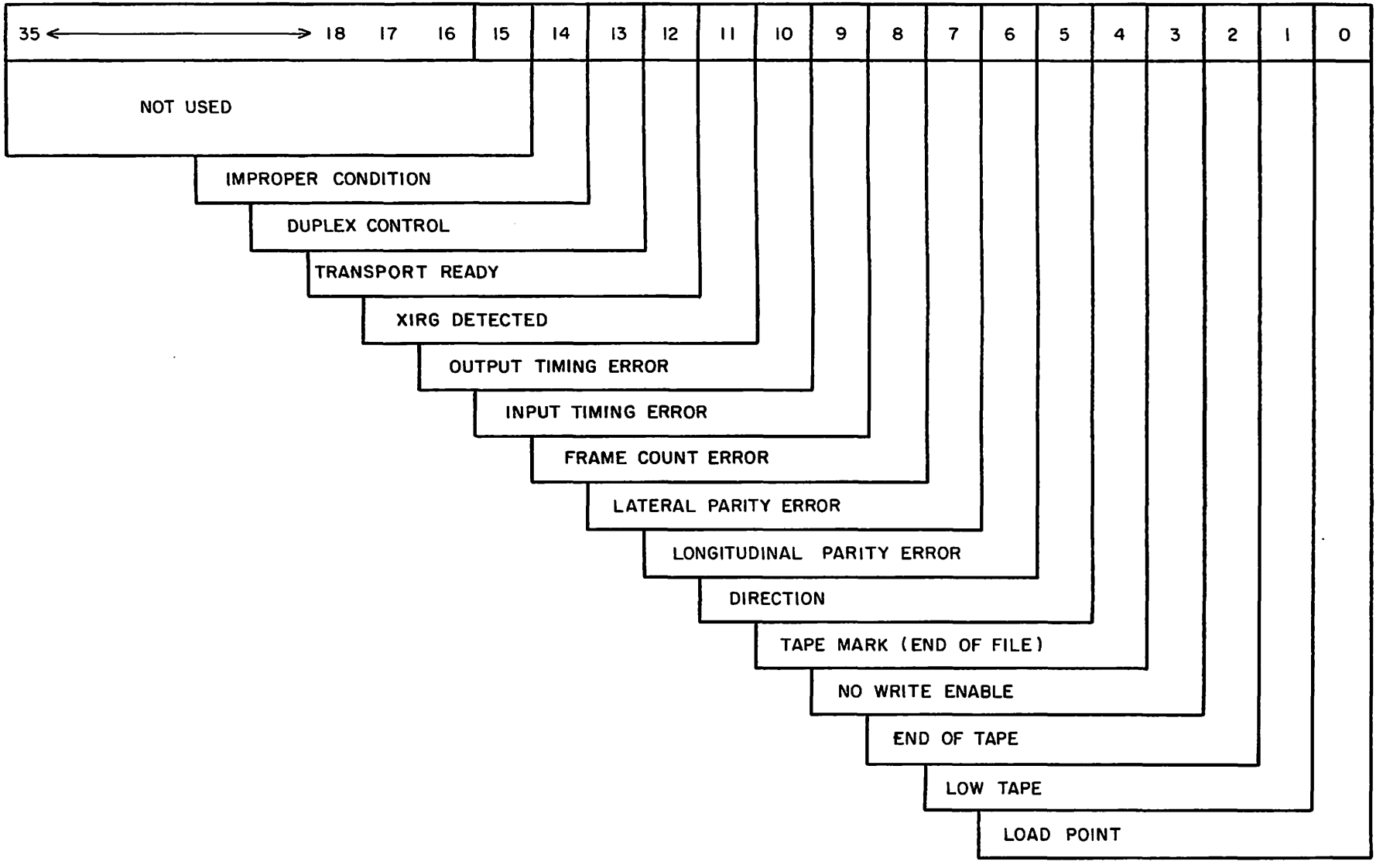


Figure 4-14. Status Word Format

An output timing error can also occur during a search or selective read operation if the MTU does not receive the search key or selective read identifier before reading the record.

(f) INPUT TIMING ERROR (Bit 9). - A 1 in bit position 9 indicates that the MTU information on the input lines was not accepted by the computer before the subsequent word was to be placed on the input lines. This condition indicates that the computer lost one or more words of the last record.

(g) FRAME COUNT ERROR (Bit 8). - A 1 in bit position 8 indicates that some frames were lost or an improper modulus was specified, that is, there were not enough frames detected in the record to complete an integral number of computer words. This situation may result from one or more of the following conditions.

1) One or more characters were not properly read or recorded.

2) Bad spots on the tape caused characters to be lost.

3) A record with the wrong format was read (for example, reading Mod 4 with a tape recorded at Mod 5). In this instance, extra frames of data are stored in the MTU and may be transferred to the computer by use of a transmit extra EF.

A longitudinal parity error will usually occur in conjunction with a frame count error if a frame(s) was lost.

(h) LATERAL PARITY ERROR (Bit 7). - A 1 in bit position 7 informs the computer that the lateral parity of one or more of the frames read did not agree with that specified in the format. A lateral parity error can also indicate to the computer that it did not receive the complete record in which the error occurred because a lateral parity error halted the transfer of data to the computer.

(i) LONGITUDINAL PARITY ERROR (Bit 6). - When recording, longitudinal parity is generated by the MTC for each channel and is recorded after the last data frame of the record. When performing read-type functions or a post-write check, the longitudinal parity of a record is checked by the MTC and, if it is in error, noted by a 1 in bit position 6 of the status word.

(j) TAPE DIRECTION (Bit 5). - Bit 5 of the status word indicates the direction the tape was moving in when an interrupt condition occurred. Bit 5 is 0 when the tape movement was forward and is a 1 when the tape was moving in a reverse direction.

(k) TAPE MARK (Bit 4). - A 1 in bit position 4 indicates that the MTC has sensed a tape mark during the function.

(l) NO WRITE ENABLE (Bit 3). - A 1 in bit position 3 informs the computer that the referenced tape transport has the write enable cleared. If a write operation is directed for a transport having no write enable, the status word also reflects an improper condition.

(m) END OF TAPE (Bit 2). - A 1 in bit position 2 indicates that the EOT marker has been detected with the tape moving in a forward direction. The computer must recognize that it cannot perform another forward operation on the selected transport until a reverse operation has moved the tape in a reverse direction past the EOT marker.

(n) LOW TAPE (Bit 1). - A 1 in bit position 1 informs the computer that the tape is positioned less than 100 feet from the EOT marker.

(o) LOAD POINT (Bit 0). - Whenever an operation is terminated with the tape positioned at the load point marker, bit 0 is set to 1. The computer must recognize that a reverse type operation cannot be performed on a transport when the tape is positioned at load point.

d. HIGH-SPEED PRINTER - MTU INTERFACES. - The MTU is capable of communicating directly with the UNIVAC Type 1469 High-Speed Printer for an off-line operation. The MTU-printer interface is shown in figure 4-15.

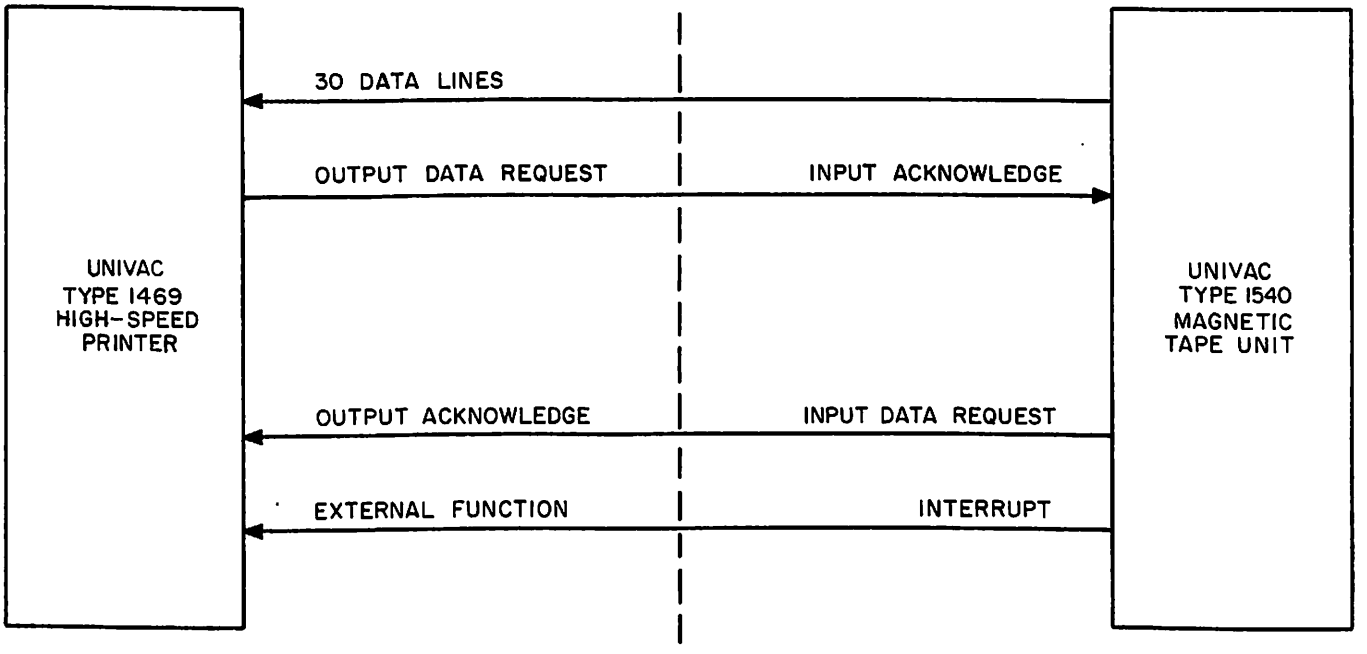


Figure 4-15. MTU High-Speed Printer Interface

In order for data to be accepted and printed by the high-speed printer, it must be recorded on tape in files, separated by tape marks, of 120 characters each.

To accomplish a data transfer, the MTU is placed in the printer mode and master cleared and tape handler 1 is manually selected. Character, density, and parity are then manually inserted into the F register. These should be the same as the ones used when the tape was recorded. Mod 5 is automatically selected in the printer mode. The high-speed printer is placed off line and master cleared. To start the operations, the printer is placed on line precipitating an ODR. The ODR is received on the MTU input acknowledge line. The first signal received on the input acknowledge line is interpreted as an external function. The signal initiates a read function with the format and density specified by the contents of the F register. When the MTU has read and assembled a 30-bit word from tape, it places the data on the printer input lines and sends an IDR. The printer recognizes the IDR as an output acknowledge, clears the ODR, and samples the data lines. The

printer then sends another ODR which is interpreted as an input acknowledge by the MTU. The MTU drops the IDR until another 30 bits of data are ready to be transmitted to the printer.

When a tape mark is read the MTU operation is terminated, a status word is assembled in the C register with the tape mark bit (bit 4) set, and an interrupt is sent. The interrupt is recognized by the printer as an EF. The printer then examines bit 4 and, finding that it is set, prints the data that is stored in its memory, and positions the paper in the printer to the top of the next page.

The operation is terminated any time the MTU sends less than 120 characters to the printer. Characters of the terminal words (record) should consist of octal 05 which is a space code and is not printed.

e. RECORDING. - Recording is accomplished by using the nonreturn to zero-change on one technique (see figure 4-16). In this method of recording, the tape is magnetized in one direction (in a given channel) until a 1 is recorded. When a 1 is recorded the direction of magnetization is reversed and remains constant in the new direction (through any number of frames) until the next 1 is recorded, at which time the direction of magnetization again reverses.

(1) RECORDING DENSITIES. - Data can be recorded and read at densities of 200, 556, or 800 frames per inch. The tape must be read at the same density as that used when the tape was recorded.

(2) TAPE FORMAT. - (See figure 4-17). The end-of-tape marker is a pressure-sensitive, adhesive-coated, aluminum reflector strip. It is 1 inch long by 3/16-inch wide and is located on the nonoxide side of the tape, 1/32 of an inch from the tape transport edge of the tape (rear edge). The end-of-tape marker is located a minimum of 14 feet from the physical end of the tape.

The load-point marker is similar to the end-of-tape marker except that it is located a minimum of 10 feet from the physical leading end of the tape and 1/32 of an inch from the front edge of the tape. The markers are detected by reflective photosensing means.

When recording on tape, the first record is recorded 3-1/2 inches from the starting position of the write head. The first record is customarily a tape mark although this is a programmer's option. A 3/4-inch interval in which no information is recorded is normally maintained between the records. This interval is called the interrecord gap (IRG). A record may be preceded by an extended IRG of 3-1/2 inches. Suitable programming will enable an IRG of any length to be written before a record; thus, records may subsequently be lengthened provided suitable IRG's were originally used. This feature may also be utilized to bypass bad spots on the tape.

The data frames of each record are followed by three blank frames, a longitudinal parity frame, an IRG, and the next record in that order.

Files of information are separated by tape marks. A tape mark is a separate record and consists of the binary number 001 111, recorded with even parity, followed by three blank frames and a longitudinal parity frame.

f. PROGRAMMING CONSIDERATIONS. - The following paragraphs include considerations which stress the programming responsibilities rather than the system capabilities.

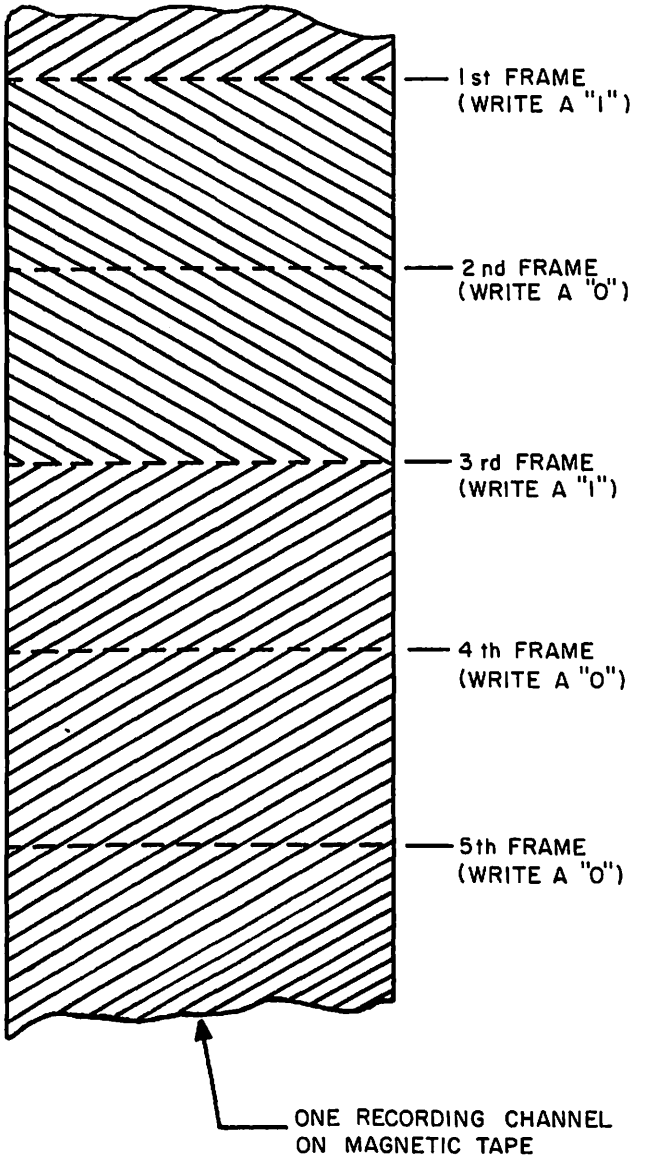


Figure 4-16. Nonreturn to Zero-Change on One Recording

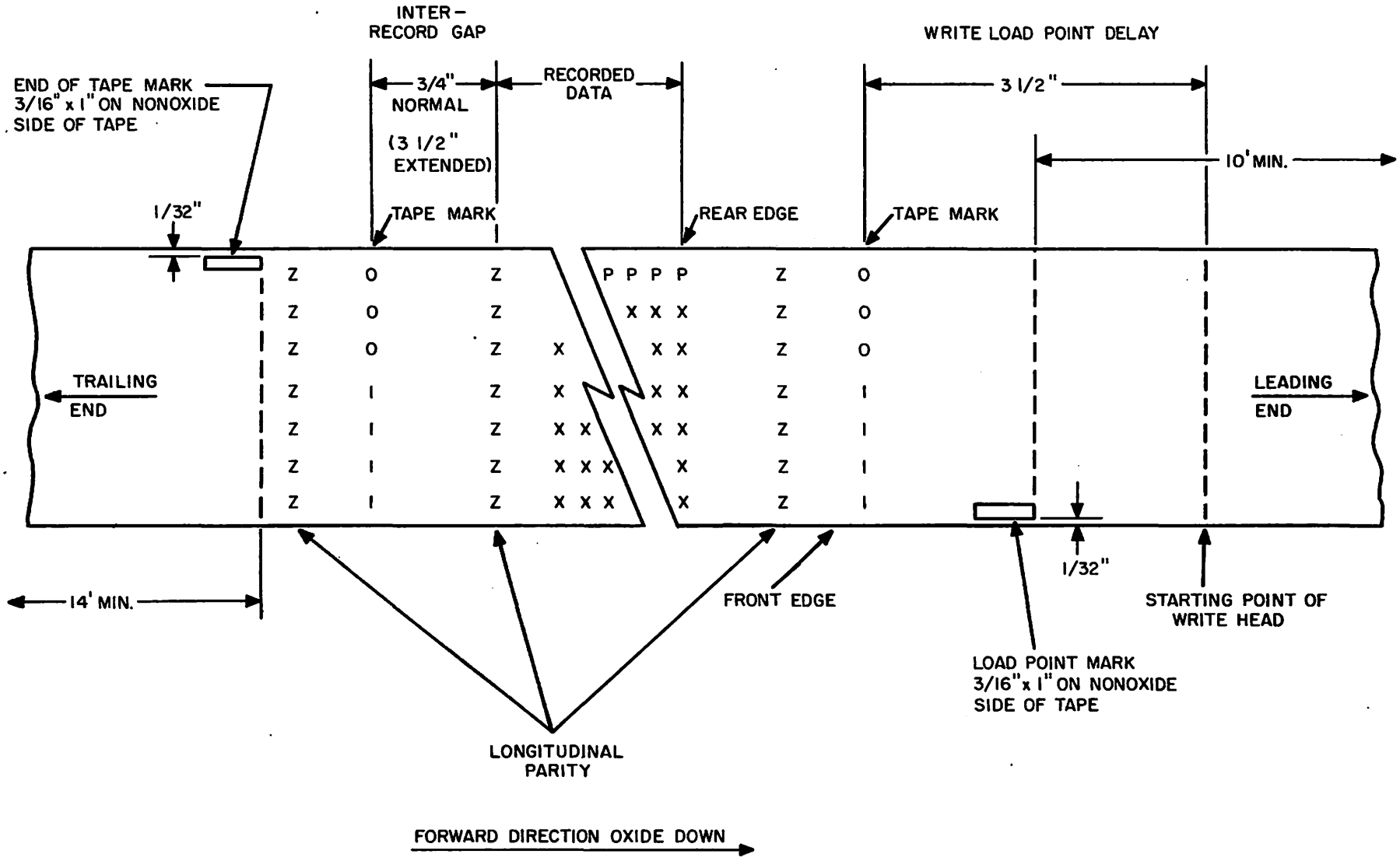


Figure 4-17. Tape Format

(1) TAPE UNIT AVAILABILITY. - It is illegal for the computer to issue a non-duplex external function before the status interrupt is received for the last specified operation. The new function would be locked out by the MTU.

(2) RECORD LENGTH. - There are no limits on record length which can be used within the capacity of the tape. When reading tapes of unknown record lengths, the programmer must either make the input buffers large enough to ensure reading the complete record or initiate an input buffer with monitor and make provisions for the initiation of additional buffers to read the complete record.

(3) WRITING CONSIDERATIONS. - In order to record on a tape, the write enable ring must be positioned in the tape supply reel to depress the write lockout switch on the tape transport and thus provide a ground to the WRITE ENABLE indicator-switch. The WRITE ENABLE indicator-switch of the desired tape transport (on the tape transport control panel) must also be depressed. An improper condition is noted in the status word if an attempt is made to write without the write enable ring in place or with the WRITE ENABLE switch off.

(4) PARITY. - When reading or recording in redundant (octal) format, the MTU automatically selects odd parity and the parity bit of the instruction word is not interpreted. For this reason it is optional if the parity bit of the instruction word is a 0 or a 1 when the redundant format is specified.

When recording in bioctal format with even parity, exercise care to ensure that no more than two zero frames are recorded sequentially. When tapes are read completely, zero frames are interpreted by the MTU as frame count errors or as an end-of-record indication. When zero data frames are liable to be recorded, odd parity must be used to ensure against a false EOR detection or frame count errors.

(5) BAD TAPE. - If a bad spot is encountered on a tape when writing a record, the computer may backread, with no buffer enabled, to the beginning of the record and rewrite it with an extended interrecord gap. The extended interrecord gap may be sufficient to allow the bad spot to move past the write head before the recording begins. Successive extended interrecord gaps may be used if the bad spot still appears. It is advisable to write a tape mark before and after the bad spot to avoid difficulties in the future. However, use of a tape with a bad spot is not recommended, especially if the tape must be used on different tape systems.

(6) WORD ASSEMBLY TIME. - Word assembly time is the time needed to read a word from tape and assemble it into a computer word. At the completion of assembly, the word is transferred to the C register. At this time an input data request is sent to the computer and the next word is read off the tape and assembled in the A register. Therefore, the computer must accept the word in the C register before the next word is assembled and is ready to be transferred to the C register. The assembly times in table 4-3 are actually the lengths of time the computer has to accept words in the different modes or moduli, as well as the length of time necessary to assemble a word.

(7) DUPLEX STATUS. - For an interrupt response to a duplex function only bit 13 of the status word should be examined. The remainder of the status word is invalid.

(8) WRITE EDIT. - For a write edit operation, the erase head is not enabled and the writing is imposed over the previous record. This entails certain considerations not present for a normal write.

1) The record to be recorded must be exactly the same length as the record to be written over if another record follows it.

2) A backread should not precede a write edit as tape creep may cause the spacing to be incorrect and leave part of the old record in the IRG.

3) Care must be exercised with any records that were written using XIRG because part of the old record may be left in the succeeding IRG.

(9) ADDRESSING TAPE TRANSPORT. - Whenever the tape handler address bits (other than 0's) are included in the lower three bit positions of the function word, a 20-millisecond delay is incorporated between the stop command for the last function and the start of the new function. If the tape transport to be used is the same as that used for the last function, inclusion of 0's in the lower three bit positions of the function code will bypass the 20-millisecond delay provided the direction of tape movement is the same as for the last operation. Any time the tape direction is reversed, the 20-millisecond delay between the operations is required. These factors must be taken into consideration for any "real time" program uses of the MTU.

(10) SHORT IRG. - If an abnormally short IRG is encountered when reading a tape recorded by another type of MTU, a backread modified stop operation should allow the read head to be positioned so that the record following the short IRG may be read successfully.

4-2. BLOCK FUNCTIONAL DESCRIPTION.

a. GENERAL. - The following description is applicable only to an automatic operation of the MTU when the computer is in the NORMAL or 1240 mode. The numbers or letters appearing in parentheses throughout this discussion refer to the corresponding circled line numbers or letters appearing in figure 4-18 (Parts 1 and 2).

The sequence of operations described in the following paragraphs includes the duplex control selection; the start operation; the read, write EOR and EOR restart operations; and the transmit extra.

b. DUPLEX CONTROL. - (Figure 4-19) If the MTU is duplexed with two computers, one of the computers must establish control before operational functions can be performed by the MTU. If only one computer is used, it can be connected to either computer A or B input and output lines. No duplexing functions are required when using the 1240 mode. The computer must be connected to channel A.

Initially, the I/O section receives an EF signal from a computer and sends it to duplex control (1). The EF enables duplex control to examine the duplex control code which it receives from the ungated input amplifiers of the C register (2).

(1) REQUEST CONTROL. - When the duplex control code is a request control and the duplex control section is in a neutral status, the requesting computer is placed in control of the MTU. The requesting computer is notified that it is in control by way of an interrupt with a 0 in bit 13 of the C register (3). If the other computer is in control, the request is stored; the requesting computer receives a duplex status interrupt and assumes control only when the other computer releases control. If the computer requesting control is already in control, the only action taken is the duplex status interrupt. When the computer acknowledges the interrupt, the I/O control sends the input acknowledge to duplex control to clear the interrupt (4).

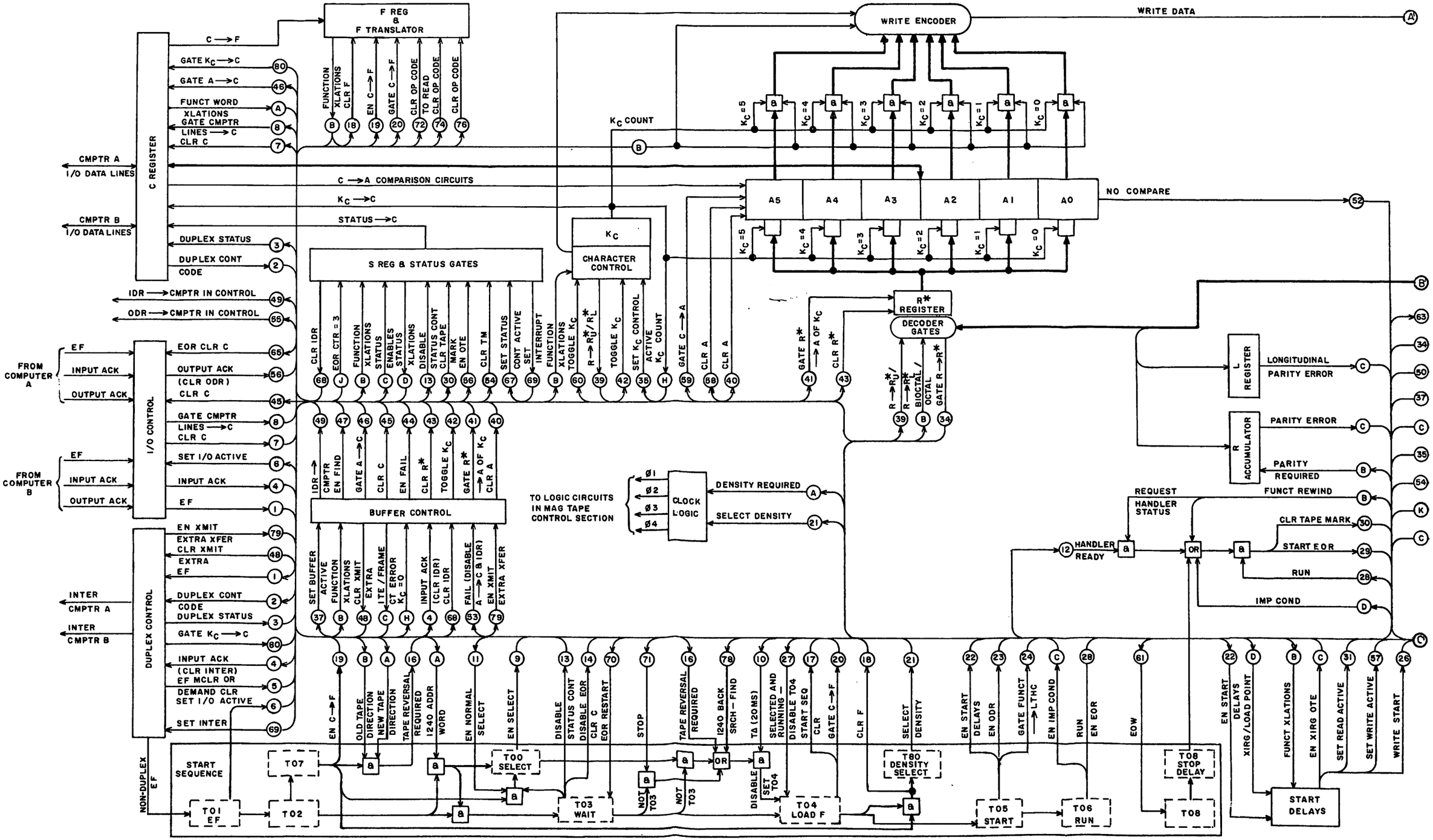


Figure 4-18. Overall Block Diagram of MTU (Part 1)

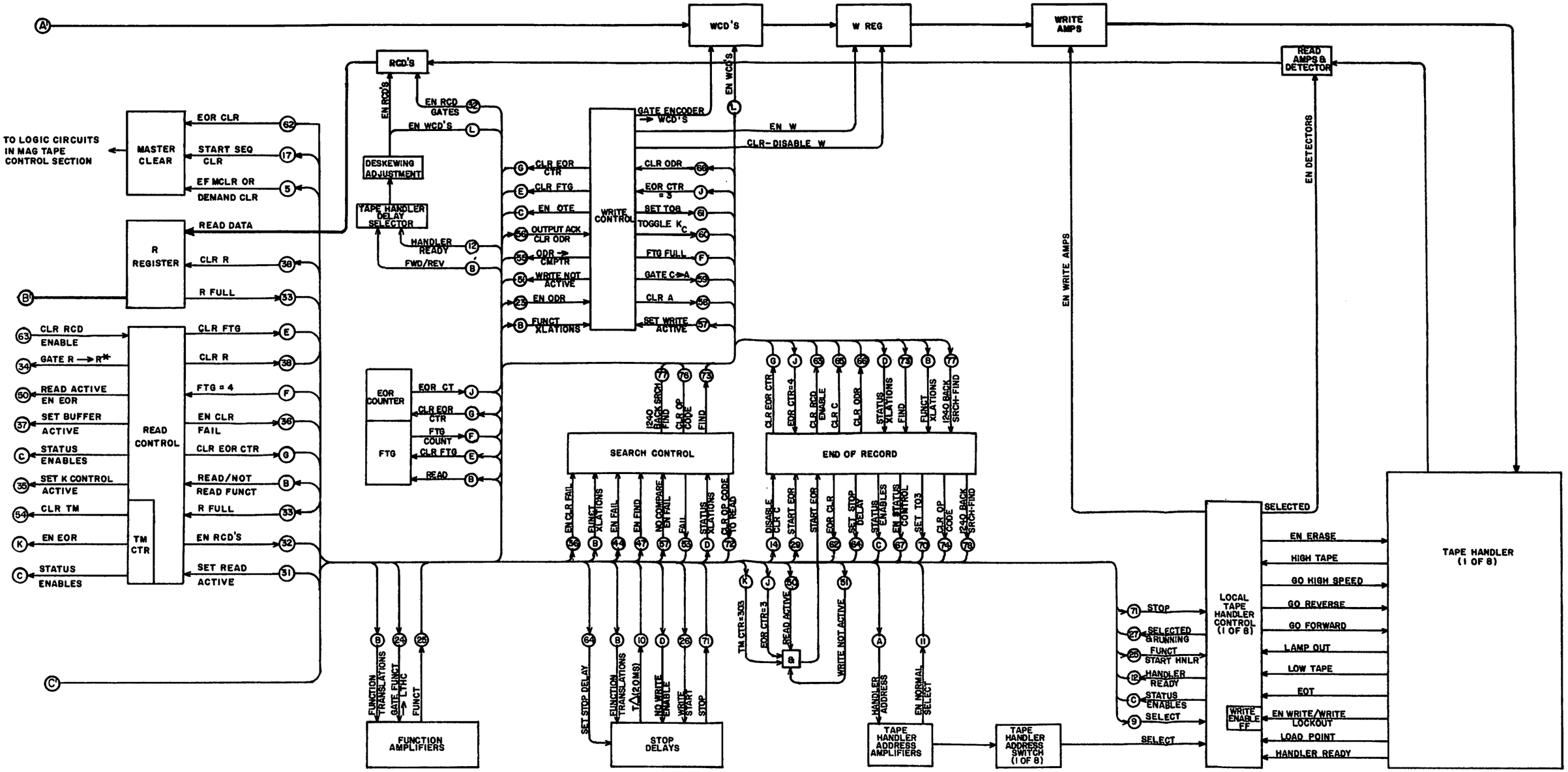


Figure 4-18. Overall Block Diagram of MTU (Part 2)

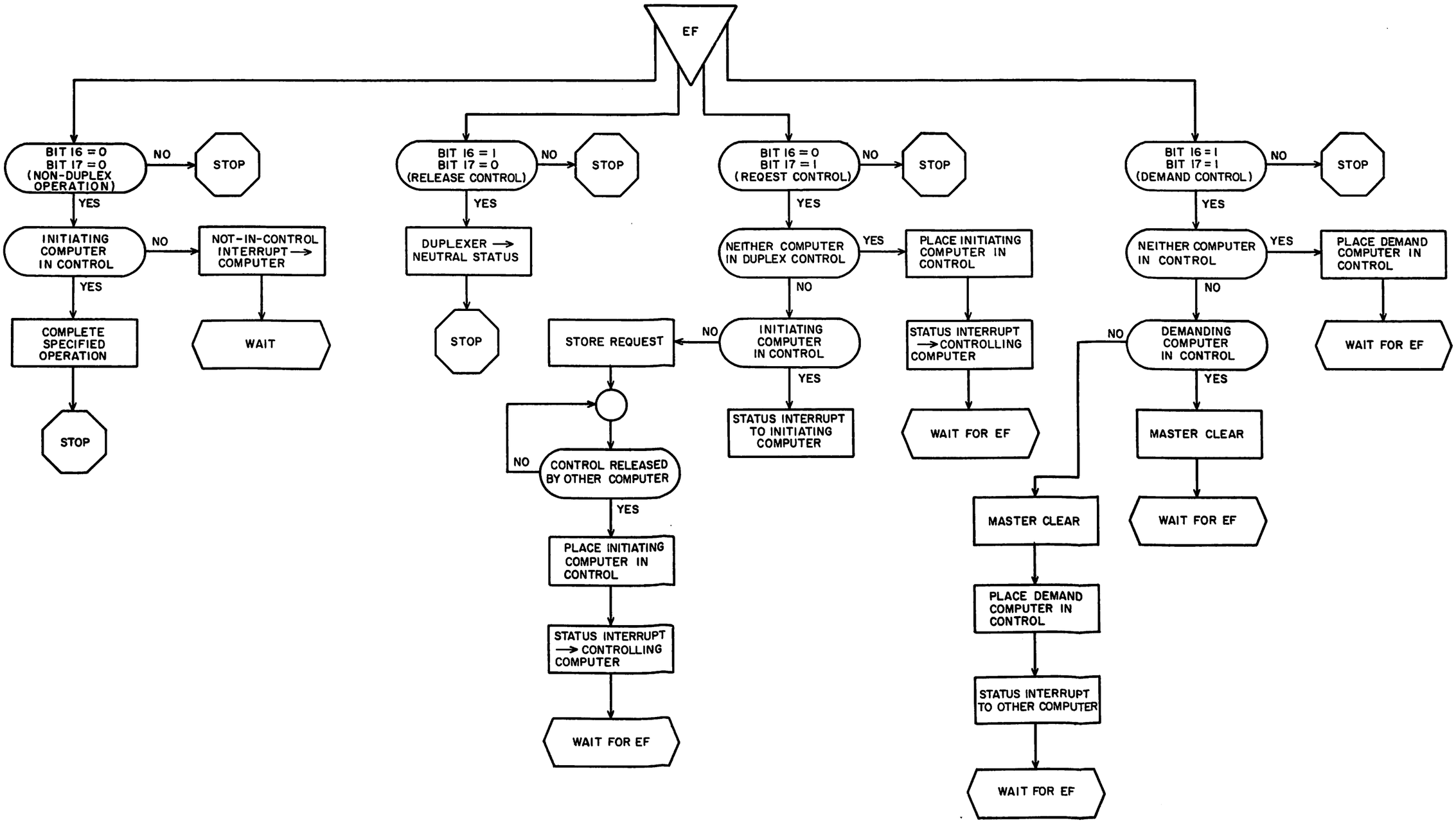


Figure 4-19. Flow Chart, Duplex Control

(2) RELEASE CONTROL. - When the duplex control code reflects a release control duplex function, the requesting computer is released from control. No interrupt is sent to the releasing computer. However, if another computer has asked for control, it will now receive an interrupt informing it that it now is in control (bit 13 is zero). If the computer originating the function is not in control, no actions are performed.

(3) DEMAND CONTROL. - When computer B is in control and computer A issues a demand control EF, duplex control commands a master clear (5), removes computer B from control, sends an interrupt to computer B with a 1 in bit 13 of the C REGISTER MTU. If computer B is not in control, the duplex control functions are the same as those described in paragraph 4-2b(1).

(4) EF MASTER CLEAR. - If the computer in control desires a master clear of the MTU while operating in the NORMAL mode, it issues a demand control duplex code. The only action taken by duplex control is to initiate the master clear circuits (5).

In the 1240 mode, an EF master clear is the same as the duplex control code request control, however, due to the mode difference, it functions to initiate the master clear circuits (5).

(5) NON-DUPLEX EF. - When a non-duplex EF is initiated by the computer in control, duplex control sets EF flip-flop T01 in the start sequence, and T01, in turn, sets I/O control active (6). I/O control clears the C REGISTER (7) and then gates the function word into the C REGISTER (8). When the I/O control is set active, the EF flip-flop is disabled after a 2 microsecond delay. Thus no other EF will be accepted in the start sequence, unless there is a demand clear or demand control, until the current operation has been completed.

When a computer not in control issues a non-duplex EF, a duplex status interrupt is sent to that computer signifying that it is not in control.

c. STARTING AN OPERATION. - (See figure 4-20) The start sequence is a timing chain which initiates a particular operation on the magnetic tape. The purpose of the various flip-flops are as follows.

(T00) SELECT - enables selection of the appropriate tape transport, and is either set by an output from T02 or a combination of outputs from T03 and T07, depending on the mode of operation.

(T01) EF - enables 1240 EF master clear, and informs MTU that a new function is being initiated.

(T03) WAIT - stops the timing chain until all tape movement conditions are satisfied. It disables control circuits of the status gates (13), disables the EOR clear circuits (14), and enables the setting of T04.

(T04) LOAD C F - initiates start sequence clear (17) and enables transfer of C F (20). It also sets density flip-flop T80, and starts flip-flop T05.

(T05) START - effects transmission of direction, control, and function signals to the selected local tape transport. It sets proper start delays (22), sets the ODR (22), and gates the function (24) from the function amplifiers to LTHC (25).

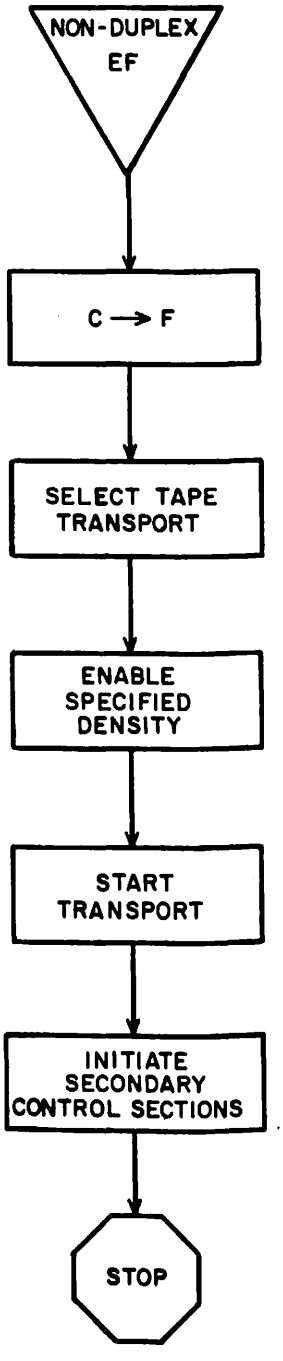


Figure 4-20. Flow Chart, Start Sequence

(T06) RUN - keeps tape moving and in conjunction with start and initiates proper read, write, and buffer control subsequence. It enables the start of the EOR control sequence (29) if there is an improper condition (D).

d. READ OPERATION. - (See figure 4-21) The read start delay is set (by the start sequence) for all operations. However, if the EOR is initiated from T06 for an improper condition, rewind, or request transport status operation, the delay is reset by an EOR clear and read control is set active. Under normal conditions, the read control is set active by the read start delay (31) when it expires. When read control is set active, it enables the read compensation delay (RCD) gates (32).

Read control is a timing chain which supplies the necessary enables for reading frames off tape. Data recognized in the read register enables the timing chain. The timing chain continues to run each and every time data is detected in the read register. The detection of three successive blank frames after at least two data frames have been read is interpreted as an end of record and therefore read control is disabled.

During the performance of all operational functions except rewind, data detected on tape is transferred into the read register. One-shot circuits are located at the input of the register. Once the read register receives a data bit from the read head, these one-shots disable any more data from entering the read register until it is cleared. The read register is cleared by a pulse from Strobe flip-flop in the read control circuit.

The R* Register is a 6-bit register that is used in the read and search operations. It receives its data from the R register. A series of AND/OR gates controls the flow of data between the two registers. In a normal read in bioctal form (B) these gates allow direct flow of the data from the R register to the R* register. When doing a back read or forward read in redundant form, these gates control the flow of data between the two registers such that the data appears in the R* register in the correct form.

e. WRITE OPERATION. - (See figure 4-22.) When a write operation is specified, T05 of the start sequence sets the write start delay (22) and initiates an ODR (23) by way of write control (55). When the computer senses the ODR, it places a data word on line to the MTU and sends an output acknowledge. The output acknowledge causes I/O control to clear the C register (7), gate the computer word into the C register (8), and send a signal to write control to remove the ODR (56). As the write start delay expires, it sets write control active (57) and enables an OTE designator in the S register (C).

Write control is a timing chain which supplies the necessary enables for writing information on tape. The timing continues to function until the output request control line is found to be up. When this occurs, three blank frames are written on tape; then a longitudinal parity frame is written and write control is inactivated and thereby interpreted as end of write. If the first output request has not been acknowledged by the time the C register is to be gated to the A register, an output timing error (C) occurs and end of record sequence (29) is initiated.

The write register contains seven flip-flops that control the writing of data on the tape. Before any data can be written on tape, the register must receive an enable from the write active flip-flop. The write register receives its data from the write encoder circuit. Data is stored on tape in a form known as change on one. Each of the seven flip-flops in the write register has two flip-flops tied

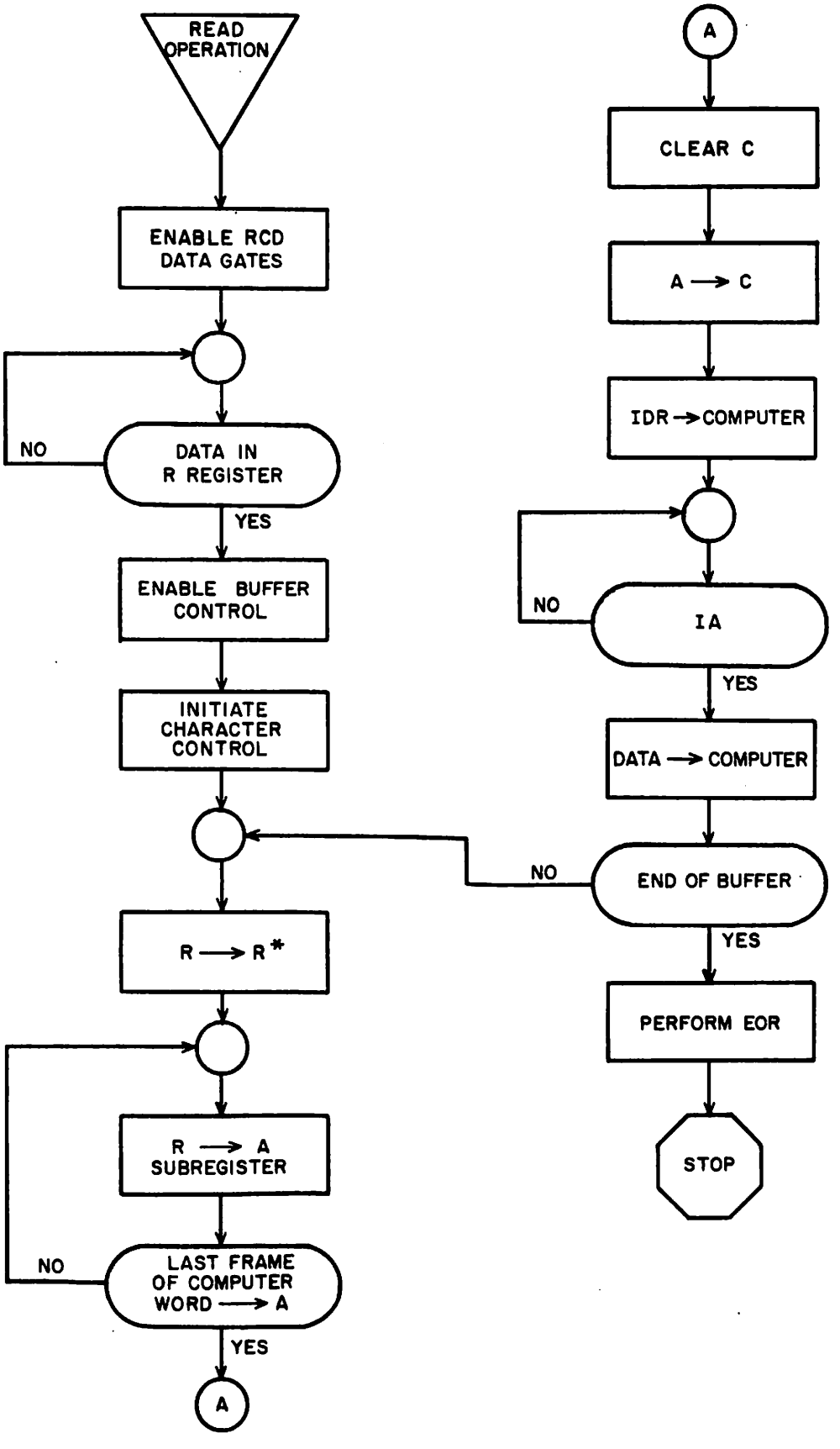


Figure 4-21. Flow Chart, Read Operation

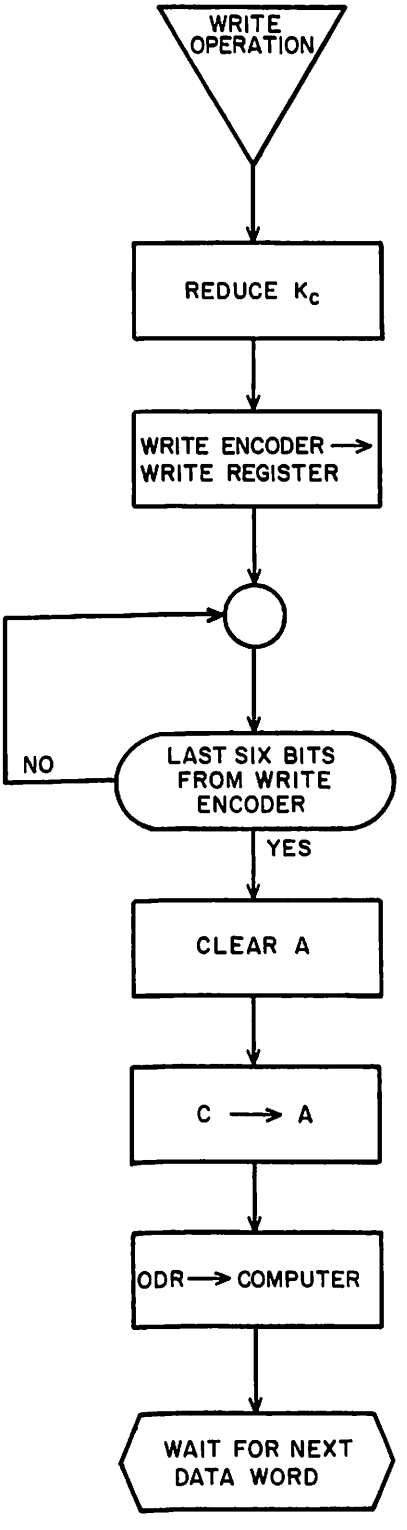


Figure 4-22. Flow Chart, Write Control

together in their input circuits. It is these flip-flops that allows the data to be written in a change on one form.

f. NORMAL END OF RECORD. - The purpose of the end of record sequence is to terminate the operation and stop the tape transport. There are 5 methods of initiating end of record.

1) Improper condition

2) Rewind

3) Request handler status

4) Emergency stop (data not read during a write function after 3 ms).

5) Read three successive blank frames after at least 2 data frames have been read.

The end of record sequence gates a status word to the C register and enables the external interrupt. It also initiates a restart condition for the multifunction operations.

g. EOR RESTART OPERATION. - There are several operations that may require tape movement through more than one record, or which require tape movement to stop and be initiated in the opposite direction. These operations are:

1) Search

2) Space file

3) Rewind-read

4) 1240 backspace-read

The EOR sequence incorporates provisions for performing the restart operations required.

(1) SPACE FILE OPERATION. - (See figure 4-23) A space file or a backspace file starts as a normal read function with read control initiated from the start delays (31). Read control together with the buffer control read and assemble data words in the A register. Every time a full computer word is assembled, an enable fail signal (44) is sent to search control. This is ANDed with the space file function and a fail signal (53) is sent back to buffer control to disable setting the IDR (49). Therefore, no data is transferred to the computer. When an IRG is detected, the EOR sequence initiates a restart signal (70) which enables the start sequence.

A space file operation functions in the same manner as previously described through any number of records, until a tape mark (file marker) is read. Read control reads the tape mark frame and advances the TM counter to one. Three blank frames are then read advancing the EOR counter to three. The TM count (C) and EOR count (J) enable the setting of a TM designator in the S register. The TM translation is sent to EOR (D) and prevents another restart. EOR performs normally to end the operation with a status interrupt to the computer.

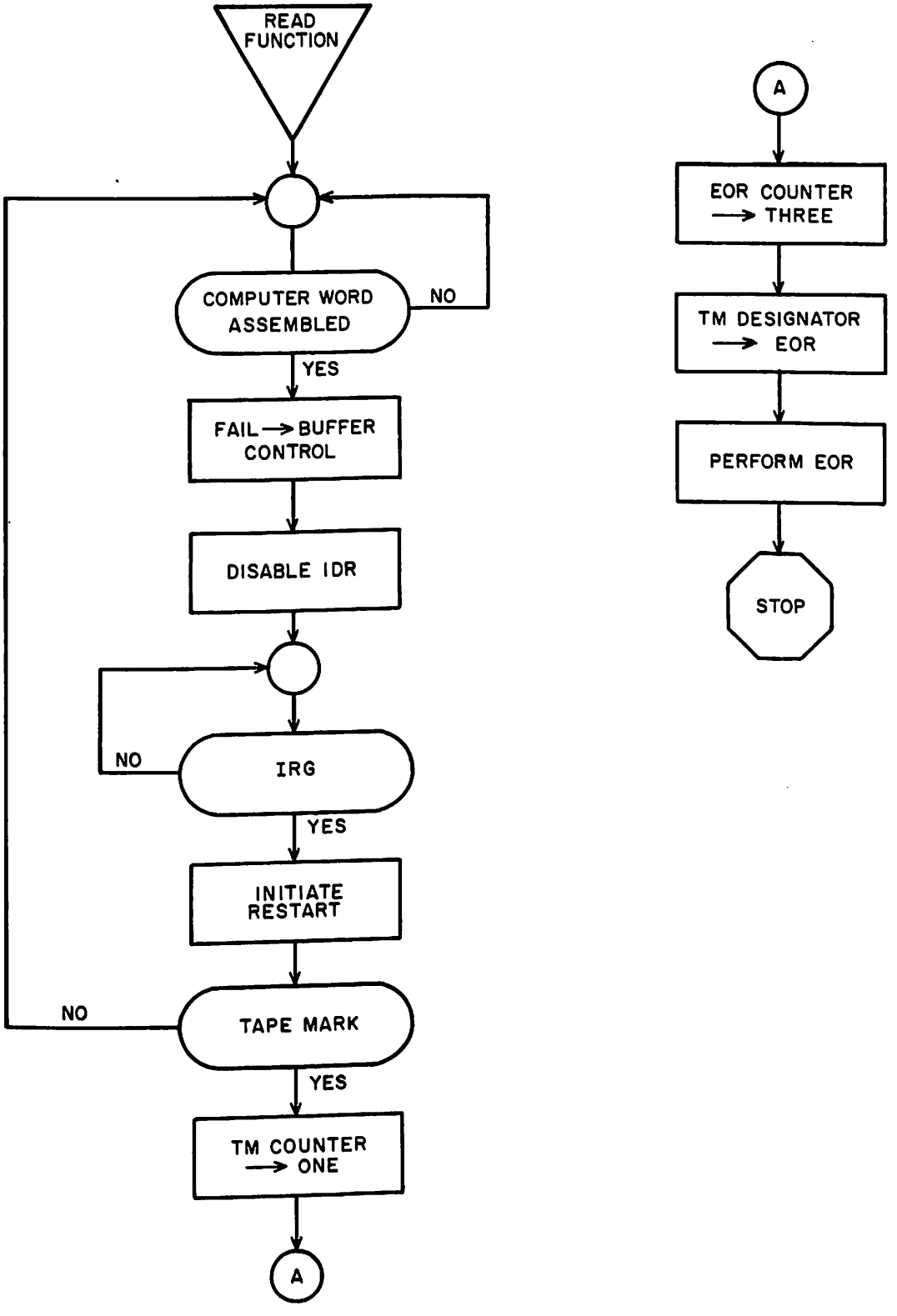


Figure 4-23. Flow Chart, Space File Operation

(2) SEARCH OPERATION. - (See figure 4-24) A Search operation is started in the normal manner by sending an ODR to obtain the search key initiated by T05 of the start sequence (23). The search key is held in the C register. Read control and buffer control assemble the first data word of the record in the A register and a search comparison takes place between the A register and the C register. If the comparison is not satisfied, the A register provides a no compare signal (52) to search control that sets a fail designator. The remainder of the record is passed over and the restart operation, during the EOR sequence, functions in the same manner as previously described for space file. If a compare is made, the find designator is set, the record is transferred to the computer, and a normal EOR stop sequence is performed when the next IRG is detected.

(3) REWIND-READ. - The selected transport rewinds the tape to the load point at 240 inches per second and then performs a normal read of the first record according to the format and density stated in the instruction word. A status word containing MTS status and any of all errors is sent to the computer with an interrupt after detecting the EOR.

(4) 1240 BACKSEARCH. - The 1240 backsearch is initiated and performed in the same manner as that previously described for a search operation except that a 1240 backsearch does not use the search control fail and find circuits which were discussed.

(5) 1240 BACKSPACE READ. - In a backspace read operation, the tape moves in the reverse direction through one record. When the EOR restart sequence sets T03 (70) it also clears the operation code in the F register (74). The start sequence then initiates a forward read operation which is terminated by a normal EOR sequence.

h. TRANSMIT EXTRA. - (See figure 4-25) When a frame(s) of data is lost (not read), a transposition of frames between computer words occurs. When the last word is read it is one or more frames short of a complete word. When this occurs K_C is not equal to zero and the clearing of the C register, gating of C to A, and setting of the IDR cannot occur. Buffer control sets a frame count error designator in the S register and the status interrupt to the computer at EOR informs the computer of a frame count error and a longitudinal parity error. A similar situation may also arise if a record is read in a modulus other than that in which it was recorded. However, in this case, longitudinal parity is indicated as correct. The extra frames of data remain in the A register at EOR. The computer may obtain these extra frames of data by use of a transmit extra EF. When duplex control senses the transmit extra control code, it sets a transmit extra designator. The transmit extra designator enables buffer control to perform a transmit extra transfer (79). These enables allow the clearing of the C register, gating of all of the A register, to the C register, and setting of the IDR. At the same time duplex control enables the gating of the translation of K_C to the lower five bit positions of C (80). The transmit extra designator is cleared by the IDR when set (48). A0 is always zero before the K_C translation is gated in, because if any frames are missing, A0 is not filled.

4-3. FUNCTIONAL ANALYSIS.

This section contains functional analysis and detailed description of the MTU.

a. MAGNETIC TAPE CONTROL SECTION.

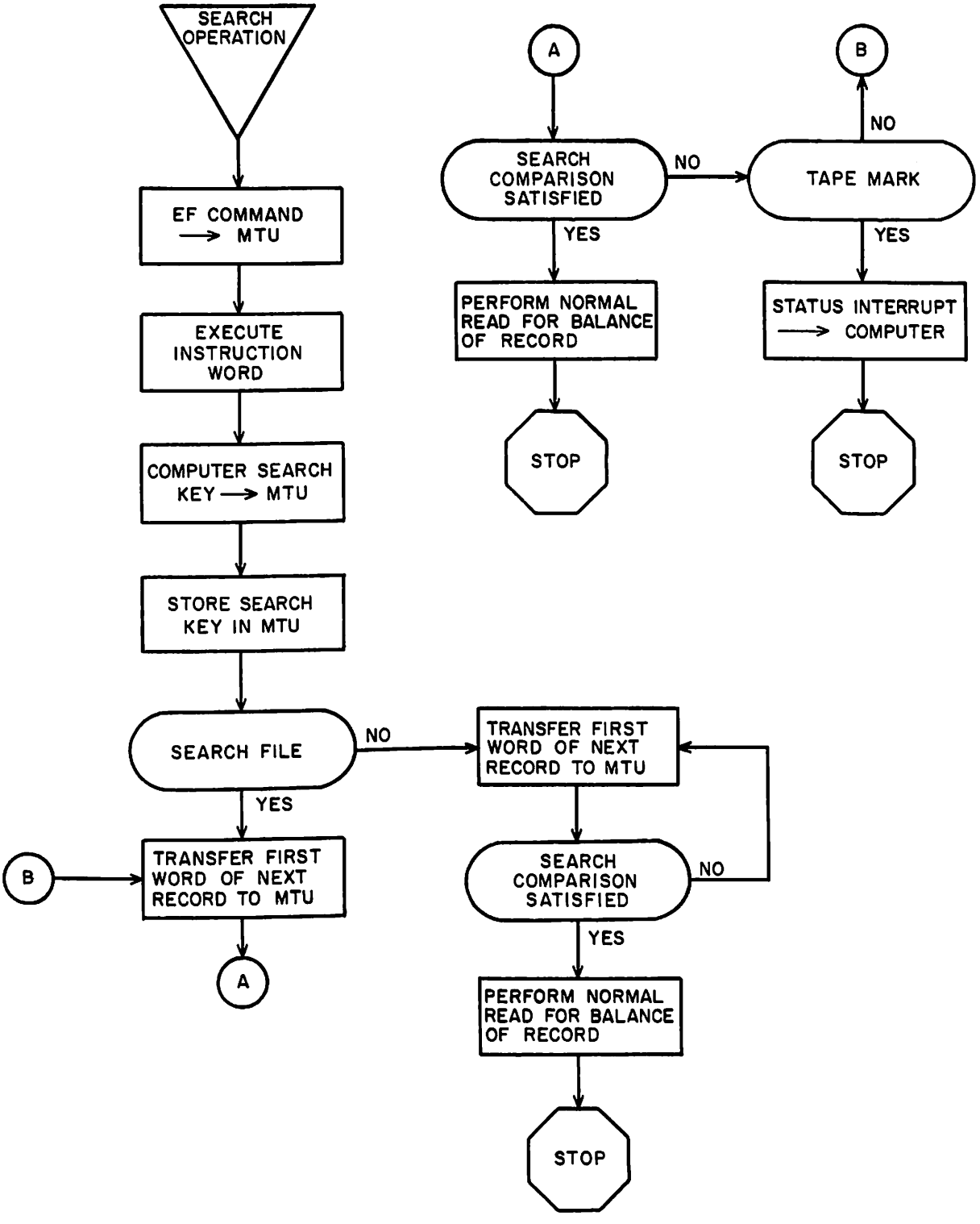


Figure 4-24. Flow Chart, Search Operation

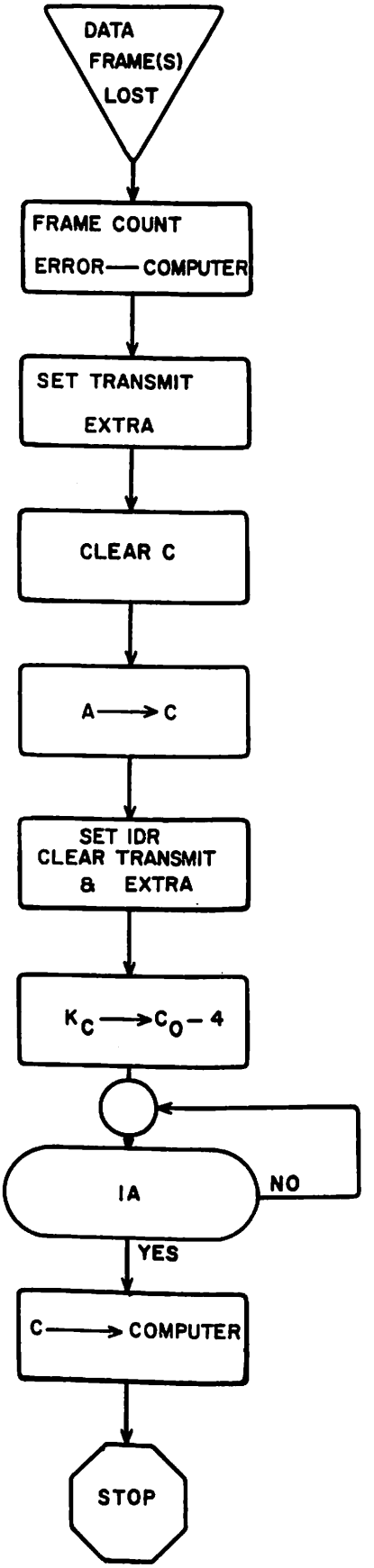


Figure 4-25. Flow Chart, Transmit Extra Operation

(1) INPUT/OUTPUT SUBSECTION.

(a) COMMUNICATIONS REGISTER. - See figures 8-55 through 8-63. The communications (C) register is a 36-stage input/output buffer register through which all data from or to the computer or to a printer is transferred.

While beginning a function, the C register stores the EF word as the initiating actions are performed. During a search operation, the C register stores the search key while the search comparisons are made. The C register is also used to store the selective-read identifier during a selective read operation.

The inputs to the C register are from the computer output lines, the corresponding stages of the A register, the status gates, the character counter, and duplex control. The computer output lines are sent to the register by way of gates enabled from I/O control (see figure 8-3).

All C register stages provide direct outputs to the corresponding A register stages, to the comparison circuits in the A register, and to the input lines of the printer, computer A, and computer B. Certain stages provide the special outputs that are required to initiate functions such as those sent to the F register and the tape transport address amplifiers. When the transmission of data to computer B, computer A, or the printer is required, the right AND input of the appropriate OR inverter is enabled. During duplexing functions, the left AND of the appropriate OR inverter may be enabled by an interrupt to inform a computer that it is not in control.

The contents of the C register are visually displayed on the upper maintenance and control panel to facilitate the maintenance and troubleshooting procedures. In all positions of the MODE switch, except NORMAL and 1240, a ground is supplied to all indicator-switches to allow for manually setting the individual bit registers.

(b) I/O CONTROL. - See figures 4-26, 8-2, and 8-3. The I/O control section provides the means for receiving and processing all of the control signals from the computer(s).

The control signals from only one computer, designated computer A, are described in the following paragraphs. A second computer (duplex operation), if used, is designated computer B and functions in basically the same manner as computer A.

1. EXTERNAL FUNCTION. - The external function (EF) signal from computer A is sensed from the computer output lines as high input. When the EF signal is removed, the duplexing requirements of the function are determined.

If a non-duplex EF is detected, the start sequence sets the I/O control active, the C register is cleared, and the EF word is gated from the computer into the C register. Once the word is in the C register, no EF except a demand clear or demand control is accepted in the start sequence, until the current operation is completed.

2. INPUT ACKNOWLEDGE. - When the MTU sends an interrupt or an input data request (IDR) to the computer, the computer senses the input data lines and sends an input acknowledge to the MTU. The input acknowledge from computer A or a printer is sensed as a high. It sets input acknowledge A flip-flop, thus clearing interrupt A flip-flop in the duplex control if it is set. If computer A is in control the IDR flip-flop in this buffer control is also cleared.

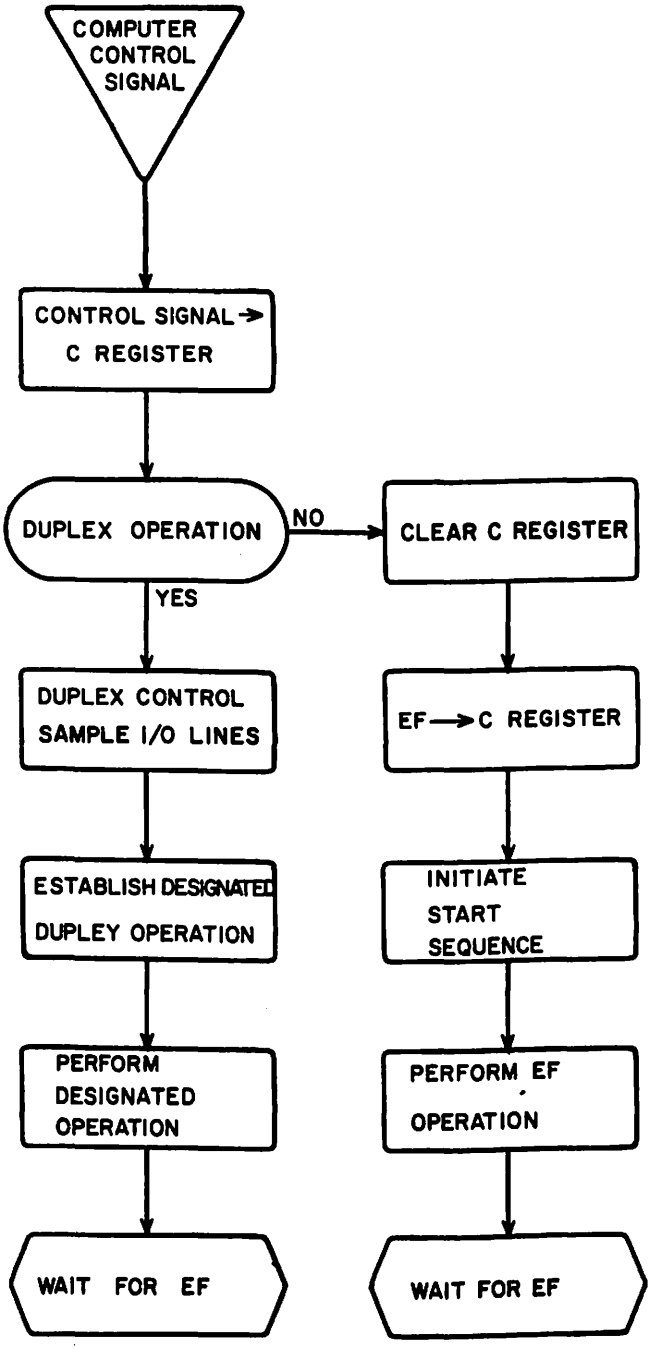


Figure 4-26. Flow Chart, I/O Control

3. OUTPUT ACKNOWLEDGE. - When the MTU sends an output data request (ODR) to the computer, the computer places data on its output lines and sends an output acknowledge to the MTU. An output acknowledge from computer A clears the C register and gates the data into the C register.

4. CLEAR CIRCUITS. - The active I/O flip-flop is cleared after it is satisfied by an interrupt, an EOR is placed in the printer mode, a tape mark status is placed in the printer mode, or a select is placed in the 1240 mode. The C register can be cleared by a master clear by setting the IDR flip-flop in buffer control, and when it is enabled by an EOR at the completion of the backspace portion of a 1240 mode backspace read in the function translator.

(c) DUPLEX CONTROL. - See figures 4-19, 8-2, 8-4, 8-5, and 8-6. Duplex control receives EF signals from I/O control, determines the duplex requirements of the EF, and performs the specified duplexing operations.

The following paragraphs describe the duplexing operations for computer A only. The duplexing operations for computer B function in basically the same manner.

1. EF REQUEST CONTROL. - When computer A sends an EF request control and a duplex control code to the MTU, a request A is recorded. This in turn sets the assign flip-flop which enables the setting of the A-in-control flip-flop. The A-in-control flip-flop performs several functions (see figure 8-5).

After computer A has assumed control and has been so notified by the interrupt, it can issue non-duplex EF's for performing tape operations.

2. EF NONDUPLEX. - With computer A in control, the EF nonduplex signal is received by I/O control; I/O control sets EF flip-flop to initiate the start sequence. If computer A is not in control, the interrupt flip-flop is not set, and computer A is notified that it is not in control.

3. EF RELEASE CONTROL. - When computer A sends an EF release control, the A-in-control flip-flop is cleared.

4. EF DEMAND CONTROL. - If it is assumed that computer B is in control when computer A initiates an EF demand control, the I/O control section performs a master clear of the MTU. After the master clear, the demand A flip-flop and request A flip-flop are set.

5. EF TRANSMIT EXTRA. - When the EF signal is received in I/O control the transmit extra flip-flop is set. With the transmit extra recorded the C register is cleared, the A1 through A5 registers are gated to the C register, and the ODR is set. Simultaneously, the transmission of the A0 register to the C register is disabled, the contents of the character counter are gated into the lower five bit positions of the C register, the fail flip-flop is cleared, and EF flip-flop T01 and the I/O active flip-flop are cleared and disabled, the data error flip-flop is cleared. Transmit extra can only be performed after using a forward read.

6. EF MASTER CLEAR. - When computer A, while in control, desires a master clear of the MTU, it initiates an EF with the same bits in the function word as for demand control. Since the master clear circuits are initiated for demand control and the demand A flip-flop cannot be set, only the request A is set. However, it is cleared on the first Ø4, and the only actions completed are those performed by the master clear circuits.

(2) DATA FORMAT SUBSECTION.

(a) READ (R) REGISTER. - The read (R) register receives each frame of data read from the tape and stores it while the processing of the frame is begun. It receives its inputs from the RCD's and provides outputs to the R accumulator for checking parity, to the L register for maintaining a record of longitudinal parity, and to the decoder gates of the R* register.

The R register is composed of standard flip-flop stages. See figures 8-36 and 8-37. Each stage has an associated indicator-switch on the upper maintenance and control panel that shows the set or cleared state of the flip-flops. In all positions of the MODE switch except NORMAL and 1240, the switch portions of the indicator-switches are active and may be used to set the associated flip-flop by either normal or manual operation. If one or more stages are set, an R full condition results.

The clearing of the R register is accomplished by manually by the R register CLEAR switch, S2, (if the MODE switch is not set to NORMAL or 1240). Internally, the R register is cleared for a start-sequence clear or master clear by flip-flop R07 during the read control sequence.

The input gates to the R register are one-shot type circuits.

(b) R* REGISTER. - See figure 8-41. The R* register is a six-stage register which is used for storing the data bits of a frame read from tape until it is gated into the A register. The R* register circuits consist of three elements.

1) Register stages R10 through R15.

2) Gates used for making the contents of the register stages available to each subregister of the A register.

3) Decoder gates which are required for assembling the data bits from two tape frames into one 6-bit data character when reading in octal format.

The output gates of the R* register, are enabled before buffer control. The outputs of the R* register gates, in turn, feed the corresponding stage in each A subregister.

The contents of the R* register are displayed on the upper maintenance and control panel and in all positions of the MODE switch except NORMAL or 1240, the Individual bit registers may be set by depressing the associated indicator-switch.

Clearing actions for the R* register are provided by the R*-register-full flip-flop, T31, in buffer control. The R* register is held clear during all periods except when T31 is set.

(c) ASSEMBLY-DISASSEMBLY (A) REGISTER. - The assembly-disassembly (A) register is a 36-bit register used in the read mode to assemble computer words from the data frames read from tape or in the write mode to disassemble a computer word into 6-bit data characters for recording in frames on tape. To facilitate assembly and disassembly of computer words, the A register is sectionalized into character length (6-bit) subregisters (see figures 8-42 through 8-47). These subregisters are called A0, A1, A2, A3, A4, and A5, respectively.

The A register has provisions for sending 36-bits in parallel to the C register or receiving 36-bits in parallel from the C register. The gates for transmitting the contents of the C register into the A bit registers are controlled by write control (see figure 8-12). The gates for gating the contents of the R* register into the A subregisters are controlled by the character counter (K_C) as follows.

1) A0 when K_C equals zero.

2) A1 when K_C equals one.

3) A2 when K_C equals two.

4) A3 when K_C equals three.

5) A4 when K_C equals four.

6) A5 when K_C equals five.

Each A subregister provides outputs to the write encoder for use during write operations.

The A register contains a group of circuits used for search and selective read comparisons. These circuits consist basically of OR inverters using multiple AND inputs. Due to the limited number of inputs available on printed circuit modules, the compare circuits are arranged in a cascade configuration. For further explanation see figure 4-27.

For a read selective operation, only the lower six bits are compared with the selective read identifier in the C register. For a selective read, the result of the comparisons of A1 through A5 with the corresponding stages of the C register is disabled (see figure 8-42).

The A register can be cleared when satisfied as follows.

1) By the A register CLEAR switch, in all positions of the MODE switch except NORMAL or 1240.

2) By master clear or start sequence clear.

3) From write control, prior to a C → A transfer.

4) From buffer control.

5) From the S register, when a tape mark is written.

The contents of the A register are displayed on the upper maintenance and control panel and in all positions of the MODE switch except NORMAL or 1240, the individual stages may be set by depressing the associated indicator-switch.

(d) WRITE REGISTER. - The write (W) register is a seven-stage register that controls, by way of amplifiers, the individual write head in each channel. See figures 8-51 and 8-52. The inputs to the W register are from the write compensation delays. These inputs control their individual stages by way of flip-flop toggle circuits. The actions of these toggle circuits are the same as the actions explained

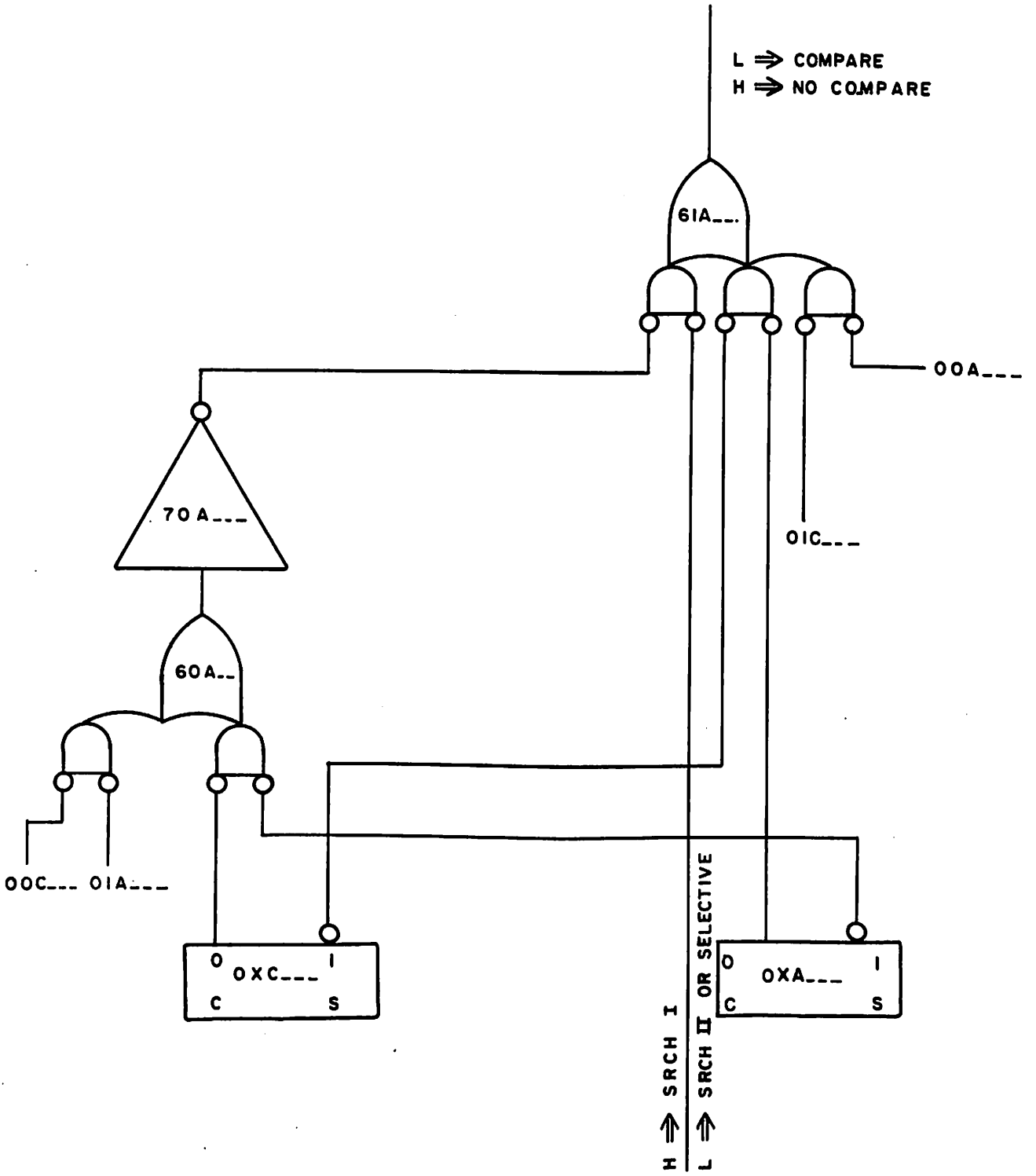


Figure 4-27. A Register Compare Circuits

for the L register. The outputs are taken from the one side of each stage and routed, to jack J11 and, by way of an interconnecting cable, to the write amplifiers in the tape handlers located to the left of the magnetic tape control section. In a similar manner, by way of jack J12, the signals may be routed to the write amplifiers of the tape handlers located to the right of magnetic tape control.

The contents of the W register are displayed on the lower maintenance and control panel. The individual stages may be set by depressing the associated indicator-switch, in all positions of the MODE switch except NORMAL or 1240.

The W register is cleared during the following:

1) A start sequence clear or master clear.

2) At an end of write longitudinal parity.

3) Whenever write is not active.

4) When MODE switch is not in the NORMAL or 1240 mode positions, and the W register CLEAR switch, S3, is pressed.

The 1540 write amplifiers are on figures 8-85 through 8-88. These circuits, under control of the write register stages, control the direction of current flow through the channel write heads.

(e) READ COMPENSATION DELAYS. - Due to variations inherent in read/write head manufacturing, data frames are read from skewed tape (see A, figure 4-28).

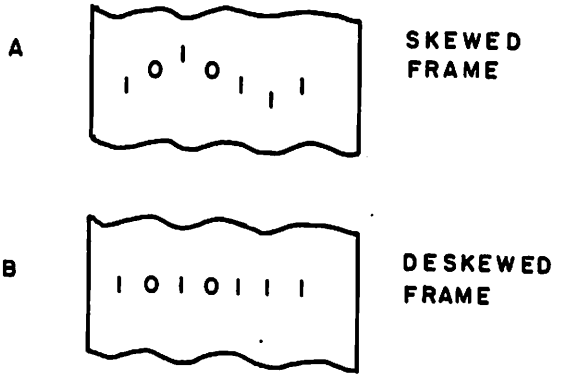


Figure 4-28. Skew

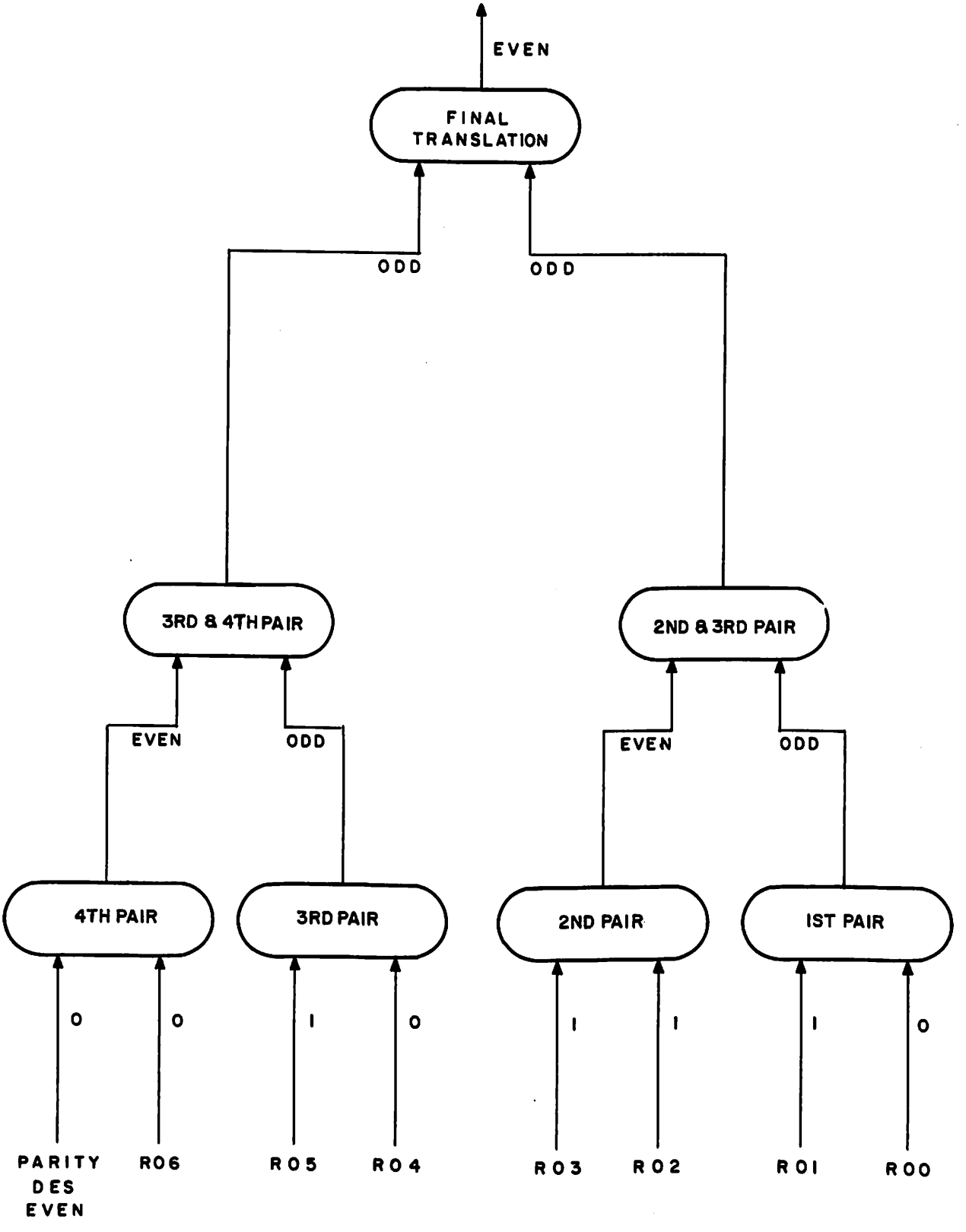


Figure 4-29. R Accumulator (Simplified)

To correct for this skew, the data is gated into the R register by way of delay circuits. (See figures 8-34 and 8-35.) The delay of each circuit is adjusted automatically from the read deskewing adjustments for the particular handler involved and the direction of the tape movement specified so that all bits of the frame are gated into the R register at the same time (see B, figure 4-28).

(f) WRITE COMPENSATION DELAYS. - See figure 8-50. Due to variations inherent in write head manufacturing, the information frames to be recorded on tape would be skewed (see A, figure 4-28). To correct this, the data to be recorded is gated into the W register write compensation delays. The delay of each WCD is automatically controlled for each channel, to compensate for each channel's individual head variation, so that the data will be recorded on the tape with little or no skew (see B, figure 4-28). The period of the WCD for each channel of each tape handler write head is controlled by the deskewing adjustment for each channel of each write head.

(g) R ACCUMULATOR. - (See figure 4-26.) The R accumulator (figure 8-58) is used to determine the parity of each 7-bit frame read from tape. If the format requires even parity (as indicated by parity designator) and odd parity is determined, the R accumulator produces a low output that will result in setting the Data Error flip-flop of the S register at read control strobe. The same actions occur if odd parity is required and the 7-bit frame contains an even number of 1 bits.

The final translation is obtained by progressive comparisons (first in pairs, then in combinations of new pairs) of the bits read from tape, combined with the output of the parity designator, which repeats until a single result is obtained (see figure 4-28). Consider, for example, the character 0 101 110 with even parity required. A comparison of successive pairs shows the following conditions (O = odd, E = even, P = parity designated).

Read from tape	(P)0101110	(P)0-10-11-10
First translation	EOEO	E O - E O
Second translation	OO	O - O
Final result	E	E

Inputs to the R accumulator are from parity designator and the R register.

(h) WRITE ENCODER. - See figures 8-48 and 8-49. The write encoder channels the contents of the A subregisters into the W register in conformance with the character designated (octal or bioctal) during write operations. It also has a parity translator which, in conjunction with the parity designator, determines whether a 0 or a 1 parity bit should be recorded with the data character.

The write encoder gates receive their enables from the character counter. For instance, a character counter equal to zero translation gates subregister A0 into the write encoder, a character counter equal to one gates subregister A1 into the write encoder, and so forth.

The write encoder is used for determining which data bits from the designated A subregister are to be gated into their corresponding stages of the W register.

When write bioctal character is designated, the six bits of data in the designated A subregister are sent to the write register in parallel, by way of the WCD's, to be recorded in one frame on tape.

When writing an octal character, the contents of each A subregister are written in two frames on tape. The encoding of the first or odd numbered frame is dependent on the upper three bits of the designated A subregister. These bits are duplicated both in the upper three and the lower three bit positions except if the original three bits are all 0's.

The lower three bits of the A subregister are recorded in both the upper and lower halves of the data character recorded in the second or even-numbered frame. Note that during either frame if the three bits of the A subregister being considered are all 0's, 1's will be recorded in the upper three bit positions of the data character and 0's in the lower three bit positions.

The parity translator portion of the write encoder is used to ensure that parity is recorded on tape to meet the requirements of the parity designator. Parity may be designated by the function word as either even or odd. The parity translation is obtained by a progressive comparison (first in pairs, then in combinations of new pairs) of the bits in a number (even or odd), which repeats until a single result is obtained. Consider, for example, the character 001101 with even parity required. A comparison of successive pairs shows the following conditions (E = even, O = odd) (see figure 4-30).

First translation	EEO
The parity designation is now paired off with the highest-order translation to reflect	(E)EE)
Repeating the process now leaves	EO
Final result	O

A 1 parity bit is written in this case to make the frame parity even.

(i) CHARACTER CONTROL AND CHARACTER COUNTER. - See figure 8-25 and 8-26. Character control is used by the read and write control for manipulating the K_C. The K_C stores the count translations used for assembling the 6-bit data characters that are read from the tape into computer words (read operation) or, in a word disassembly, for gating six bits of a computer word at a time to the write encoder for subsequent recording on tape (write operation).

A detailed description of these circuits will be found under Character Control of the Primary Control subsection.

(3) PRIMARY CONTROL SUBSECTION.

(a) CLOCK LOGIC. - See figures 8-89, 8-90, and 8-91. The clock logic furnishes the basic timing control to the logic circuits of the magnetic tape control section of the MTU. In normal operation, the clock logic generates four phase signals (Ø1, Ø2, Ø3, and Ø4) every clock cycle. The times established for clock phases and clock cycles are listed in table 4-3.

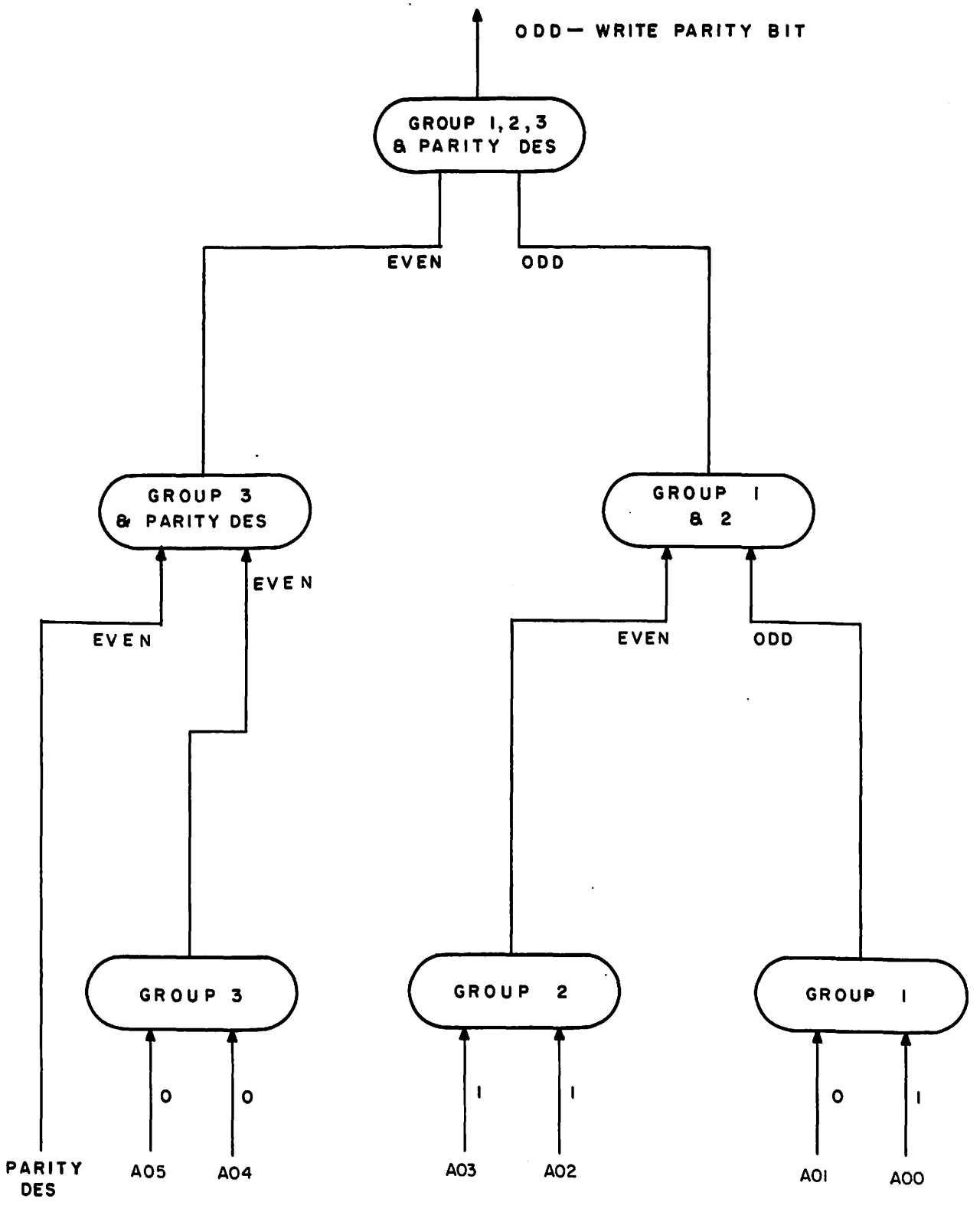


Figure 4-30. Write Encoder Parity Translator (Simplified)

TABLE 4-3. CLOCK PHASE AND CYCLE TIMES

MTU TYPE	DENSITY SELECTED (BPI)	CRYSTAL FREQ (MC)	CYCLE TIME (usec)	PHASE DURATION (usec)
1540	200	2.31	3.464	0.8660
1540	556	1.60	1.256	0.3125
1540	800	2.31	0.866	0.2165

The clock logic consists basically of two crystal oscillators, a frequency divider network (see figures 8-89 and 8-90), and a phase enable timing chain (see figure 8-91). Part 2 (see figure 8-90) of the clock logic provides the circuits for the manual control of the phase production for maintenance and test purposes. Manual control is exercised by the CLOCK CONTROL switch, S8 (see figure 8-31) and LOW SPEED-STEP switch, S9. In the manual control positions of the CLOCK CONTROL switch and the LOW SPEED position of S9, the production of clock phases is controlled by a variable low speed oscillator. The frequency of the low speed oscillator may be varied from 2 to 200 cycles-per-second by means of potentiometer R1 (LOW SPEED ADJ).

1. NORMAL CLOCK OPERATION. - At time T04 of the start sequence, the density select flip-flop is set (see figures 8-8, 8-89, and 8-92). It sets the density flip-flop desingated by the density code in the C register and clears the non-selected density flip-flops. To further ensure that the other density flip-flops are cleared, the selected density flip-flop, by way of a single-shot circuit, grounds the one side of the other two density flip-flops. When an 800 bit-per-inch density is selected, the 800 density flip-flop is set, disabling the frequency-divider circuits. Thus the fastest rate of the 200-800 bpi oscillator is used to generate the clock phases. See figure 4-31.

For densities of 556 bits-per-inch, the 556 density flip-flop is set, enabling the 556 BPI oscillator.

For densities of 200 bits-per-inch, the 200 density flip-flop is set enabling the frequency divider network. Thus the slowest rate of the 200-800 BPI oscillator is used to generate the four clock phases.

During all normal clock operation, the actions of the phase enable flip-flops for phase production are identical. The only differences are the rate at which the phases are produced and the corresponding time durations of the phases and clock cycles.

2. MANUAL CLOCK OPERATION - Manual control of the clock phase production is available in the Ø STEP and MULTI Ø positions of the CLOCK CONTROL switch.

In the MULTI Ø position of the CLOCK CONTROL switch, the phase enable timing chain is advanced in the same manner as for Ø STEP.

3. LOW-SPEED CLOCK OPERATION. - In the LOW SPEED position of S9, the low speed oscillator automatically performs the operations described above for the STEP position of S9. See figure 4-32.

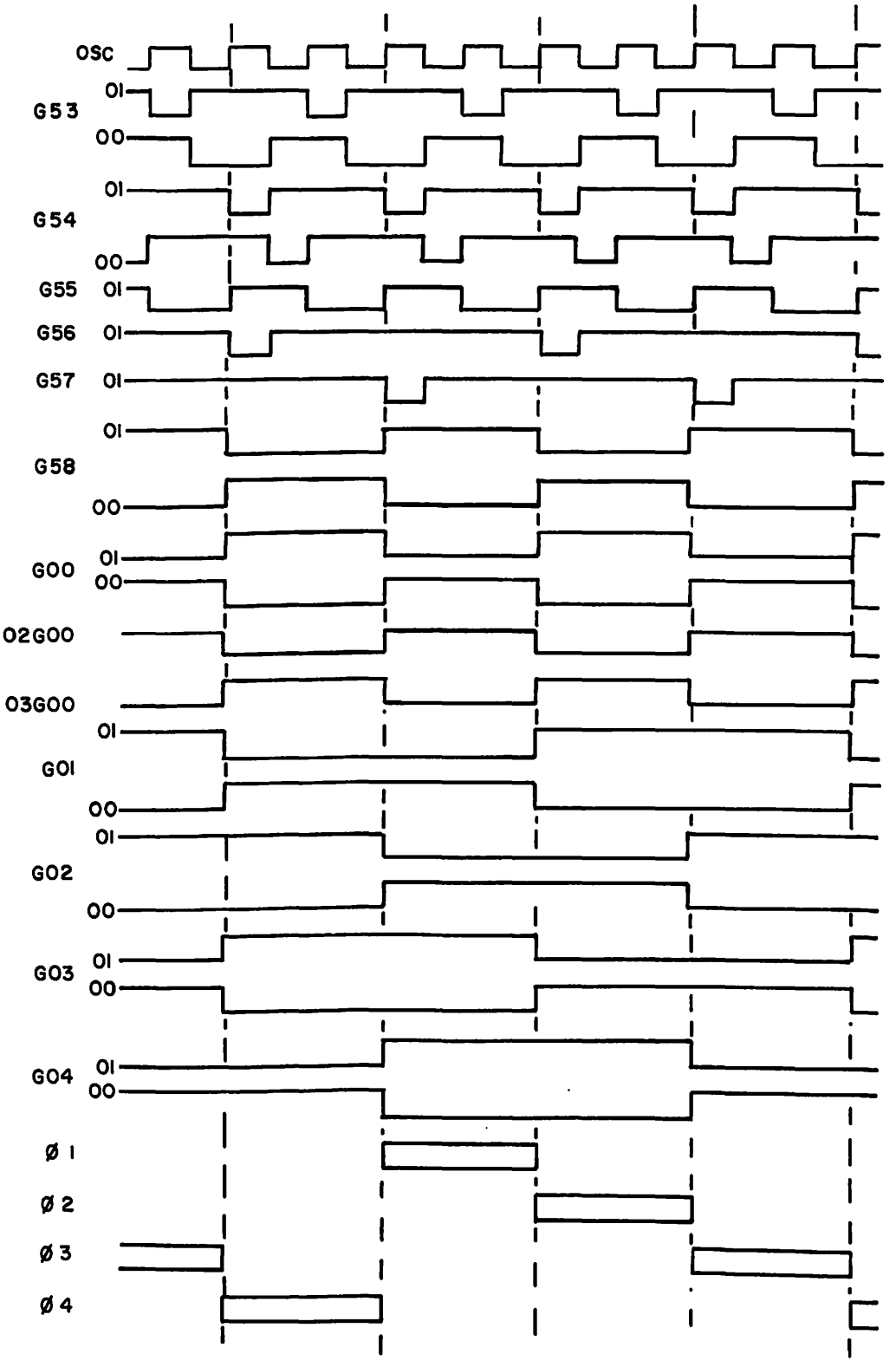


Figure 4-31. Clock Logic Waveforms for Density Selection of 200 Bits-Per-Inch

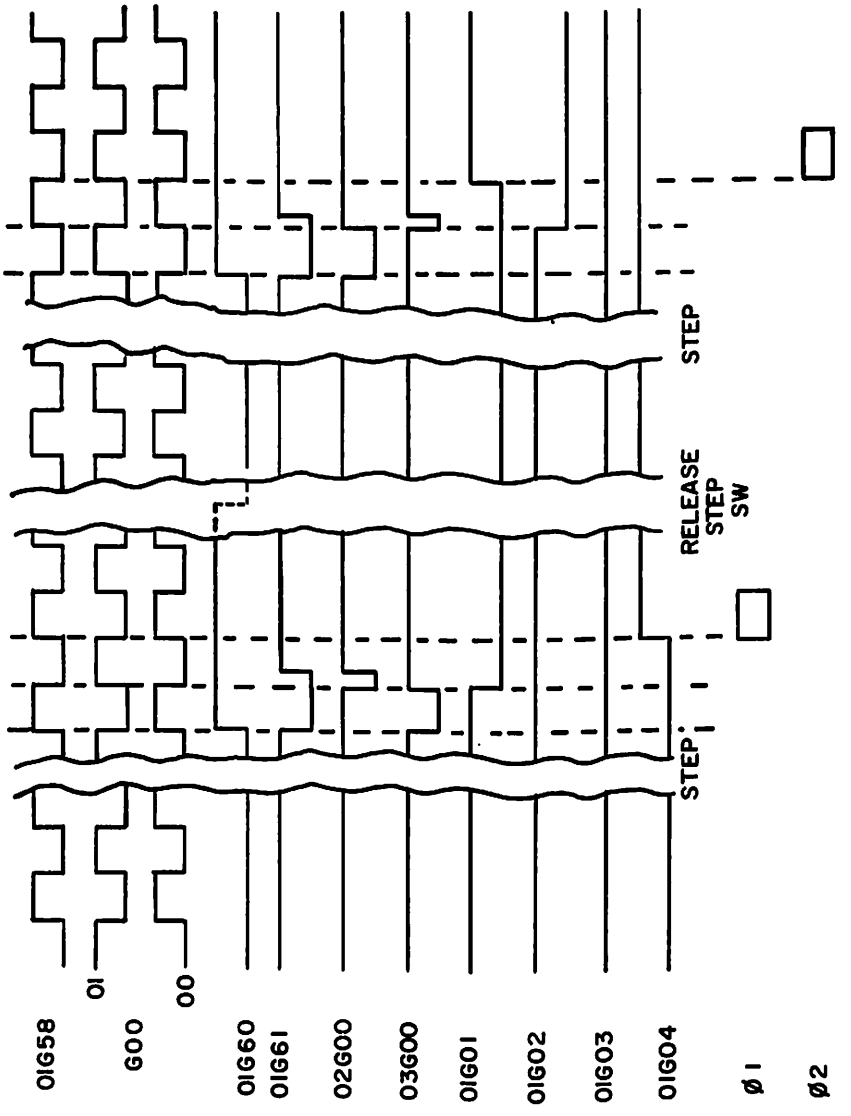


Figure 4-32. Clock Logic Waveforms for Phase Step Operation

(b) MASTER CLEAR. - See figures 8-28 and 8-29. The master clear circuit provides the means by which the MTU may be brought to a ready condition regardless of the current status. Most of the registers and circuits are cleared and are ready for a new instruction. The master clear may be initiated in four ways:

1) Power turnon

2) Receipt of a demand control or master clear EF

3) Receipt of a 1240 EF master clear (bit 16 set in the function word)

4) Depress MASTER CLEAR switch S10

The two parts of the master clear circuit shown in figure 8-29 are also used as a start sequence clear and an end-of-record clear, respectively. They perform the selective clearing actions required at the time by the subsections that initiate them.

(c) FUNCTION REGISTER. - See figures 8-18, 8-19, and 8-20. The function (F) register is an 11-stage register used to store the operation code, format, and biasing bits of the EF word for use during execution of a function. The bits that are stored in the F register are as follows:

1) F03 and F04 - The bias designators when the EF word does not specify a handler selection

2) F07 - Parity designator

3) F08 - Character designator

4) F09 and F10 - Modulus designators

5) F11 ; through F15 - The operation code which is defined as follows.

a) F14 and F15 - The basic function:

00 = read
01 = write
10 = reverse read type operations
11 = rewind or request handler status

b) F11 through F13 - The bits that modify the basic functions.

The F register provides maintenance panel indicators of its contents, and the indicator-switches may be used to set individual stages when the MODE switch is set to any position except NORMAL or 1240. The F register CLEAR switch is also effective in any mode switch position except NORMAL or 1240.

(d) FUNCTION TRANSLATOR. - See figures 8-21 and 8-22. The function translator circuits are used to distribute translations of the F register contents to the various logic circuits that require them during a functional operation.

(e) STATUS REGISTER AND STATUS GATES. - See figures 8-23 and 8-24. The status register is a six-stage register which is used to store certain status information so that it can be used by the control sequences or retained until required for the status word.

The status information that is stored in the bits of the S register is as follows:

1) S04 - Tape mark
2) S07 - Lateral parity error
3) S09 - Input timing error
4) S10 - Output timing error
5) S11 - Extended interrecord gap
6) S14 - Improper condition

The gates for transmitting the status information into the C register, during the EOR sequence, are also included on the S register schematics.

The contents of the S register are displayed on the upper maintenance and control panel. The individual bit registers may be set in all positions of the MODE switch except NORMAL or 1240 by pressing the associated indicator-switch.

The clearing of the S register is accomplished by a master clear or a start sequence clear and can also be cleared by the S register CLEAR switch, S3, in any position of the MODE switch except NORMAL or 1240.

(f) LONGITUDINAL COUNT REGISTER. - The longitudinal count (L) register is used to keep a running record of the parity in each tape channel along the longitudinal axis of the tape. At the end of each record the longitudinal parity for each channel should be even, that is, an even number of 1's recorded in each channel. When data is written on tape, each record is terminated by recording a longitudinal parity frame. This frame should containa a I whenever necessary to make longitudinal parity, for each channel, even.

The register is composed of standard flip-flop stages with an indicator-switch, on the upper maintenance and control panel, for each stage. See figures 8-39 and 8-40. The individual stages may be set by pressing the associated indicator-switch when the MODE switch is set to any position except NORMAL or 1240. Two flip-flop circuits per stage are used to provide toggle inputs to the register stages. The inputs to the L register are provided from the zero side of the corresponding stages of the R register.

Whenever one or more of the L register flip-flop stages is set at an end of record, a longitudinal parity error is detected. The error output is used to include the parity error in the status word. It will also prevent a rewind-read, search, or search file restart operation when a longitudinal parity error is present.

(g) FRAME TIME GENERATOR. - See figure 8-27 (schematic diagram). The frame time generator (FTG) is a binary counter which is used to regulate the period of time that a frame of data is exposed to the magnetic tape by the write heads. It is also used to advance the EOR counter for timing the EOR sequence.

At this time the write control sequence, and an end of write (EOW) are enabled. The FTG will start advancing again on the next Ø2. The FTG is cleared during a read type operation from read control on a Ø3. The FTG is also cleared on Ø3 as write control is set active for a write operation. See table 4-4.

TABLE 4-4. FTG COUNT TABLE

COUNT	TIME Ø	G 13	12	11	10	G 82	81	80	ACTION
12	4	0	0	0	0	0	0	0	CLEAR GZO
1	2	0	0	0	1	0	0	0	
	4	0	0	0	0	0	0	1	
2	2	0	0	1	1	0	0	0	
	3	0	0	1	0	0	0	0	
	4	0	0	1	0	0	0	0	
3	2	0	0	1	1	0	0	0	
	4	0	0	0	0	0	1	1	
4	2	0	1	1	1	0	0	0	
	3	0	1	0	0	0	0	0	
	4	0	0	0	0	0	0	0	
5	2	0	1	0	1	0	0	0	
	4	0	0	0	0	1	0	1	
6	2	0	1	1	1	0	0	0	
	3	0	1	1	0	0	0	0	
	4	0	0	0	0	0	0	0	
7	2	0	1	1	1	0	0	0	
	4	0	0	0	0	1	1	1	
8	2	1	1	1	1	0	0	0	
	3	1	0	0	0	0	0	0	
	4	0	0	0	0	0	0	0	
9	2	1	0	0	1	0	0	0	
	4	0	0	0	0	0	0	1	
10	2	1	0	1	1	0	0	0	
	3	1	0	1	0	0	0	0	
	4	0	0	0	0	0	0	0	
11	2	1	0	1	1	0	0	0	
	4	0	0	0	0	0	1	1	SET G20
12	2	1	1	1	1	0	0	0	
	3	0	0	0	0	0	0	0	SET T22

(h) EOR COUNTER. - The EOR counter is a 4-stage ones counter that is advanced each frame period by the FTG when it is enabled by read control or write control.

The EOR counter is enabled during read type functions, but is cleared each time strobe flip-flop T15 sets in read control. Thus during read type operations or after write active is cleared during a write operation, the only time the EOR counter can advance is when blank frames are read from tape (the read control is enabled but cannot run). The outputs of the EOR counter are not used during a write operation until an EOW is detected. When EOW is detected, the EOR counter is cleared. When the EOR counter has again advanced to 3 the W register and the Write Active flip-flop are cleared. When the write active flip-flop is cleared, control of the counter is turned over to read control for completing the readback portion of the write operation. When the EOR counter has advanced to 3, the EOR control sequence is enabled. The first stage of EOR, clears the EOR counter. The EOR counter must now count full (four frame periods) to allow the second stage of EOR control to set.

The EOR counter is cleared for a master clear or start sequence clear.

When read control detects a tape mark, the EOR counter advances to 3 and sets the tape mark flip-flop in the status register.

(i) START SEQUENCE. - See figure 8-7 and 8-8. The start sequence is a timing chain that provides the command enables required for selecting the tape handler; storing the operation code, format, and address portions of the function word; enabling the proper density; starting tape motion at the selected tape handler; and enabling the secondary control sections, such as read and write control.

The start sequence is initiated by a duplex control output which is provided only when a non-duplex EF is initiated by the computer in control. When the start sequence is initiated, the wait flip-flop is set.

When operating in the 1240 mode with an address word in the C register, the select flip-flop is set and the local tape handler control (LTHC) section is enabled. In the LTHC, the enable signal is combined with a ready signal from the tape handler and with the select signal from the tape handler ADDRESS switch to select the desired LTHC. The tape handler ADDRESS switches translate the address received from the C register and select the handler that has its switch positioned to that address. If the T Δ 20-millisecond delay is still set from a previous stop command, it inhibits setting the Load F flip-flop until the 20-millisecond delay expires.

When operating in the NORMAL mode with an address in the function word, the tape handler selection is performed in the same manner as described above for a 1240 mode select.

The LTHC, when selected, enables gating the tape and handler status to the status register, enables the read detector circuits, and gates the handler ready signal to the tape handler delay selector.

The control circuits of the status gates and the EOR clear C circuits are disabled by the wait flip-flop.

Next, the appropriate start delays are set, the ODR in write control is set for a write, read selective, or search operation, and the function is gated to the LTHC. The LTHC in turn causes the tape handler to start moving the tape in the specified direction.

For all operations except write and rewind, the tape direction specified may be either forward or reverse. When a write operation is specified (and write is enabled), the tape is started in a forward direction and the write amplifiers and erase head are enabled. If a write enable ring has not been inserted into the tape supply reel, a write lockout signal is sent to the LTHC by the tape handler and the write cannot be enabled. When the write enable has been returned to the LTHC, the write enable flip-flop may be set by a pushbutton. If a write enable ring is not positioned in the tape supply reel or the write enable flip-flop has not been manually set, a no write enable signal is sent to the S register. The no write enable status is sent from the S register to the stop delay circuits where it is combined with a write start condition from the start delay circuits to initiate a stop command to LTHC.

When a write edit function is sent to the LTHC, the same actions as described in the previous paragraph are taken except that the LTHC does not enable the erase head.

The writing of an extended interrecord gap (XIRG) is a function of longer than normal start delays.

For a rewind operation when the handler is reflecting low tape, LTHC enables the tape handler to start moving the tape in a reverse direction at a high speed. When the handler indicates high tape, the LTHC removes the high-speed enable and the tape rewinds to load point at a normal speed.

After the start command to the tape handlers is issued, the run flip-flop is set. The run flip-flop remains set until an operation has been completed and then enables the start of the EOR control sequence. The run flip-flop enables an improper condition status in the S register. If, for some reason, the tape handler did not start running, an improper condition designation is set in the S register.

Any of several conditions at this time, when combined with the output of the run flip-flop will initiate the EOR sequence and clear the tape mark designation in the S register. These conditions are: a rewind function; an improper condition; or a request handler status function with a handler ready.

(j) START DELAYS. - See figure 8-9. The start delay circuits are used to initiate the write and/or read control sections at the proper time in relation to a load point condition, the function requested, or the length of the IRG from which the tape motion is being started.

1. READ START DELAYS. - The read start time delays are both set from the start sequence for all operations except request handler status and rewind. In these two instances a reset signal from the function translator disables them. When read start delays are set, their normally low output goes high and two single-shot circuits are permitted to reset. When the read start time delay expires, its output sets the read enable flip-flop in read control (see figure 8-10). If the tape is being started from load point, a status gate (see figure 8-23) disables the load point detectors until the tape has moved the load point past the detector.

The load point flip-flop is cleared by the start sequence, an EOR clear, or a master clear.

2. WRITE START DELAYS. - The write start delays are time delay circuits. For a normal start (not load point or XIRG), a short delay is provided before setting write active. For a load point condition or XIRG, a 24-millisecond delay is provided before setting write active.

The start time delay circuits are reset when satisfied for a request handler status function, for a rewind function, or for an EOR clear or master clear.

3. TD TEST. - The input from the clock logic swings alternately high and low at a rate determined by the low speed oscillator when the CLOCK CONTROL switch is set to the TD TEST position. This input is used for pulsing the time delay circuits for making time delay checks and adjustments.

(k) CHARACTER CONTROL. - See figures 8-25 and 8-26. Character control is used by the read and write control for manipulating the K_C. The K_C stores the count translations used for assembling the 6-bit data characters that are read from the tape into computer words (read type operation) or, in word disassembly, for gating six bits of a computer word at a time to the write encoder for subsequent recording on tape (write operation).

(l) WRITE CONTROL. - See figures 8-11 and 8-12 (functional schematics) and figure 4-33 (timing chart). Write control furnishes the command control and timing required for writing the data, received from the computer, on magnetic tape.

When a write operation is specified, the start sequence sets the write start delay and initiates an ODR by way of write control. When the computer senses the ODR, it places a data word on line to the MTU and sends an output acknowledge. The output acknowledge causes I/O control to clear the C register, gate the computer word into the C register and send a signal to write control to remove the ODR.

As the write start delay expires, it sets write control active and enables an OTE designator in the S register. The ODR from write control also enables the OTE designator in S. If the ODR is still set when the write start delay expires (computer has failed to supply the data for writing), the OTE designator in the S register sets. As write control sets active, it synchronizes the FTG by clearing it, removes a clear disable from the W register, clears the A register, gates the C register into the A register, and sends an ODR to the computer to obtain the second computer word. When the FTG has counted full, write control sends a toggle command to K_C and gates the contents of the write encoder to the WCD's. (The WCD's were enabled from the deskewing adjustments when write start was initiated. The first toggle for each computer word sets the K_C to the value specified by the modulus designator. Each succeeding toggle reduces the K_C by one. At this time the decoder gates between one A subregister and the write encoders are enabled by the function translations and the current value of K_C. For instance, when modulus 5 is designated, K_C equals 4 and the bioctal character is designated; the entire contents of A4 are gated into the write encoder in parallel, however, if octal character is designated, only the upper three bits of A4 are gated into the encoder. In this case enables/disables from character control and the F register are used to duplicate the three bits in both the upper and lower half of the write encoder. The encoder also develops the correct parity as specified by the function register. In the case of octal write, write control functions as described above, however, the toggle for reducing K_C by one is effective only every other frame. During the second frame period of write control the lower half of A4 is encoded into both the upper and lower halves of the write encoder.

The WCD's are adjusted so that data will be properly skewed, feeding their corresponding stages of the W register. Data within the W register is sent to the write heads by way of the write amplifiers.

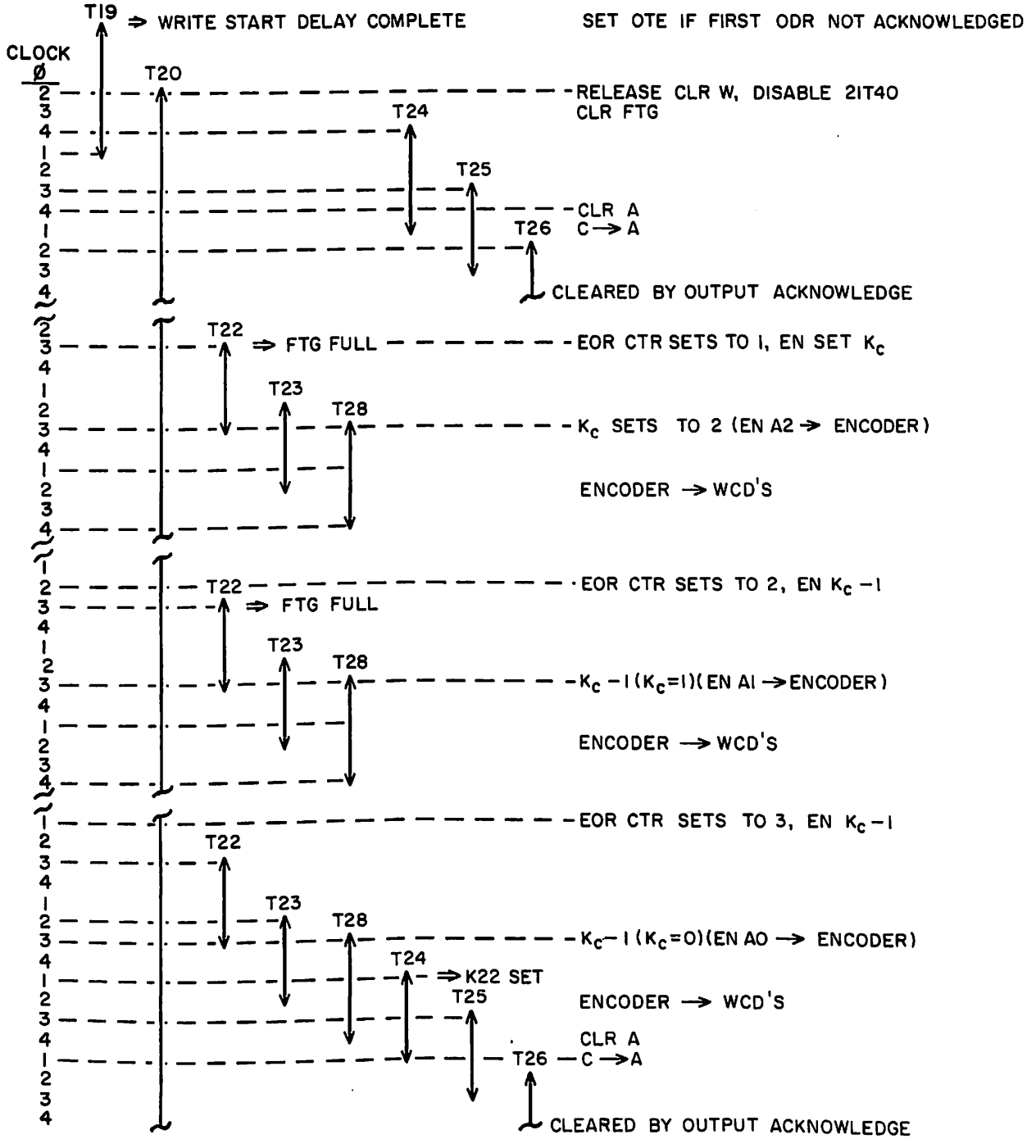


Figure 4-33. Write Timing (Mod 3)

Write control functions repetitively, as described above, until K_C equals zero (the entire computer word has been processed). When K_C is equal to zero, write control clears the A register, gates the second computer word from the C register into the A register, and sends an ODR to the computer to obtain the next data word.

When K_C is equal to zero and the ODR is still set, write control waits until the FTG again counts full and then it enables an OTE status designator, and clears the EOR counter. When the EOR counter has counted to 3, write control places a clear-disable on the W register (causing a longitudinal parity frame to be recorded), again clears the EOR counter, and clears write control active thus turning control of the EOR counter over to read control. Read control then initiates the EOR sequence after it has performed a readback of the last data recorded. If an output acknowledge occurs after the OTE is enabled (as described above), it will cause the OTE designator in the S register to set (the data was received too late to be recorded in its proper place on tape).

(m) READ CONTROL. - See figure 8-10 (functional schematic) and figures 4-34 and 4-35 (timing charts). The read control section provides the command control and timing necessary to process the data frames read from tape by the read head. The read control section is enabled and utilized for all operations except request handler status and rewind.

The read start delay is set (by the start sequence) for all operations; however, if the EOR is initiated for an improper condition, rewind, or request handler status operation, the delay will be reset by an EOR clear and read control will not be set active. Under normal conditions, the read control is set active by the read start delay when it expires. The start delay enables the extended interrecord gap (XIRG) designator in the S register and if a load point condition is present or no data is read from tape for an abnormally long period, the tape mark (TM) counter in read control enables the setting of the XIRG designator in the S register. When read control is set active, it, in turn, enables the read compensation delay (RCD) gates. The RCD's are also enabled by the ready signal from the LTHC by way of the tape handler delay selector and the deskewing adjustments. (The read amplifiers and detectors were enabled when the LTHC was selected.) The data detected on the tape by the tape handler is sent to the R register by way of the read amplifiers and detectors and to the read compensation delays. When the R register senses the data, it returns an R full signal to read control. Read control synchronizes the frame time generator (FTG) by clearing it and advances the TM counter. When read control performs a readback operation during a write, the FTG is under direction of write control and is not cleared at this time. During this period, the contents of the R register are fed, ungated, into the longitudinal count (L) register and the R accumulator. The L register keeps track of the longitudinal parity and the R accumulator determines if the parity of the data frame in the R register is correct.

During a readback operation, a strobe will occur at this time. During read type operations, however, a wait is necessary until the FTG has advanced to 4. The strobe performs the following actions:

1) Gates the contents of the R register into the R* register by way of the decoder gates.

2) Clears the EOR counter if a read type operation is in progress. If write control is active, control of the EOR counter is maintained by write control.

3) Character control is set active. Again this is a function of read control that is effective only for a read type operation.

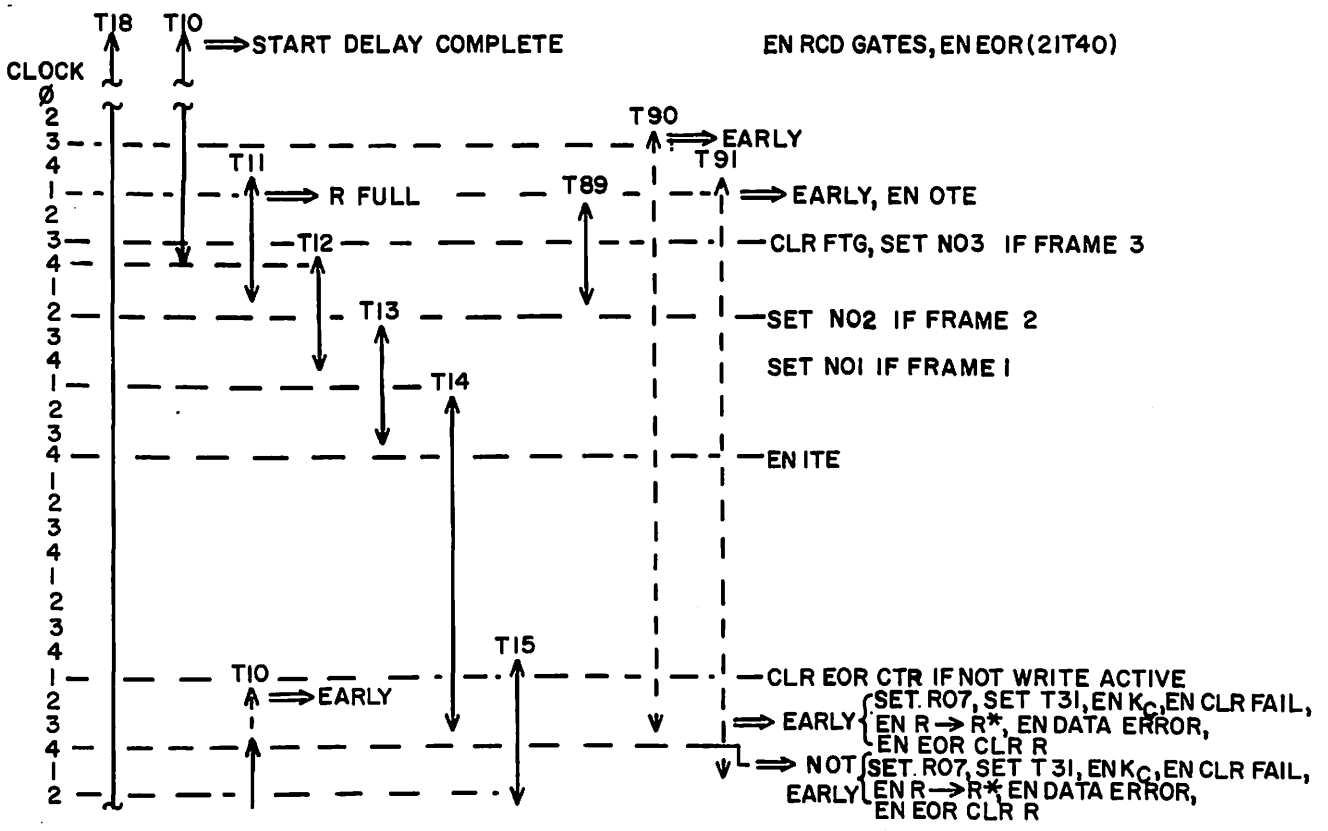


Figure 4-34. Read Timing for a Read Type Function

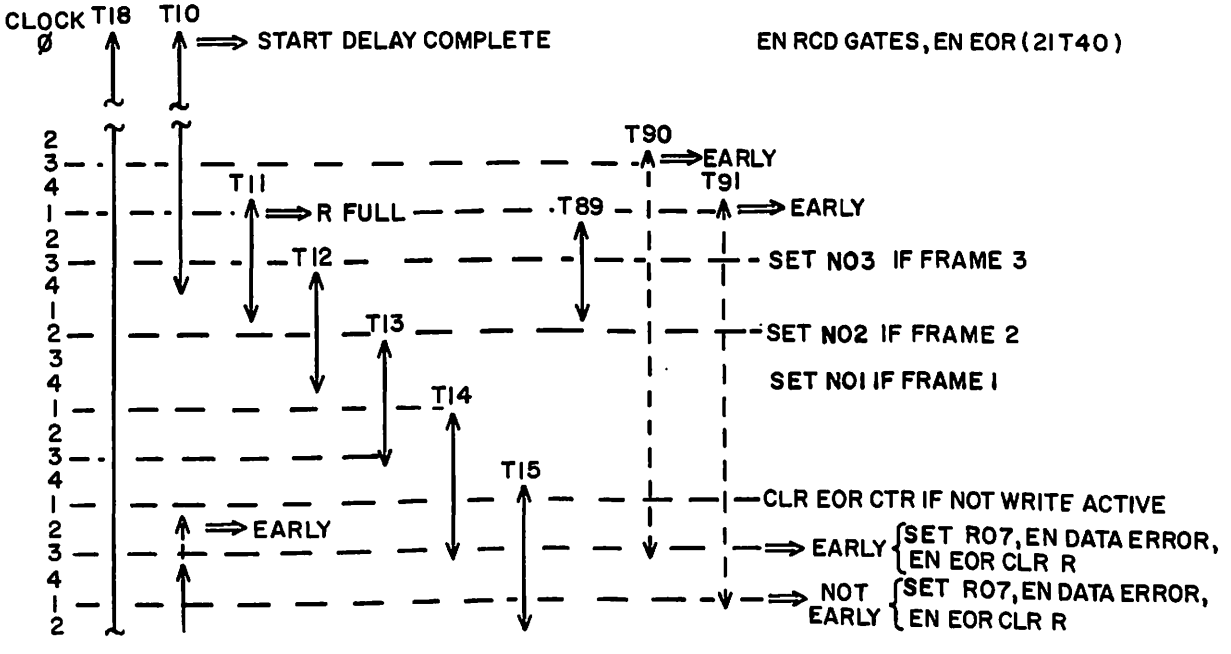


Figure 4-35. Read Timing for a Write Function

4) Enables the clearing of the fail designator in search control.

5) Enables the setting of the data error designator in the S register when the R accumulator has detected a parity error.

6) Sets buffer control active.

7) Clears the R register.

When the character designated is bioctal, the entire contents of the R register are gated in parallel into the R* register. If the character designated is octal, the R* register decoder gates, using the function translations and the enables from character control, gate both the upper half and the lower half of the R register into one half of the R* register. Buffer control, although set active, is not allowed to run. When the second or even-numbered frame of data is gated from the R register into the R* register, both halves are gated into the other half of the R* register thereby filling it up.

After the R* register is full (one frame bioctal or two frames octal), buffer control clears the A register (the first frame of each computer word only), gates the R* register to the A subregister designated by K_C, issues a toggle K_C command to character control, and clears the R* register. The toggle command, if it is the first one for a computer word when the tape is moving in a forward direction, causes K_C to be set to the value specified by the modulus designators. If it is not the first toggle for the assembly of a computer word, K_C is decreased by one for a forward operation or is advanced by one for a reverse operation.

The above operation of read control and buffer control continues until a complete computer word is assembled in the A register, at which time K_C is equal to zero. When K_C equals zero, buffer control enables the setting of a fail designation in search control, commands the clearing of the C register by way of the I/O control, gates the contents of the A register into the C register enables the setting of a find designation in search control, clears the transmit extra designator in duplex control, and places an IDR on a control line to the computer in control. The computer senses the IDR and sends an input acknowledge to I/O control. I/O control, in turn, clears the IDR.

Each time read control runs, it enables an input timing error (ITE) input to the status register. As buffer control is enabled, it also enables the ITE. When it is time for buffer control to gate a frame of data from the R* register into the A subregister designated by K_C with this condition prevailing, the last word has not been accepted by the computer and the ITE designator in the S register sets.

As read control senses the second frame of data in the R register, the tape mark counter and read control enable an output timing error (OTE) designator in the S register. If the operation is a search or selective read and the computer does not supply a search key or selective read identifier (ODR is still set), the OTE designator in the S register sets.

After read control has read the last frame of data in a record, no other full signals are received from the R register and the actions of read control stop. Thus with no strobes present, the EOR counter is not cleared and will advance each time the FTG counts a frame period.

The EOR sequence is then initiated, by way of an AND function, when: read is active but not running, the EOR counter has advanced to 3, the TM counter equals 2 or 3, and write control is not active.

A selective read is performed in the same manner as a normal read except that after each complete computer word has been assembled, a comparison of the selective read identifier, in the C register, is made with the contents of the A register. If the comparison is not satisfied, the fail designator in search control sets when it is enabled from buffer control. The fail translation from search control is sent to buffer control and prevents the transfer of A to C and the setting of the IDR. Thus, the only words that are sent to the computer are those that compare with the selective read identifier. At each strobe for a selective read, read control clears the fail designator.

The tape mark counter functions as a part of the read control sequence. Its basic function is to determine when a tape mark record has been read. Each time read control processes a frame of data, it advances the TM counter by one. Thus when TM equals one and the EOR counter is equal to three, the TM designator in the S register sets. When read control reads the longitudinal parity frame, the TM counter sets to 2 and the EOR counter is cleared. When the EOR counter has again advanced to 3, EOR is initiated in the normal manner by way of the AND function. If additional frames are read after setting the TM designator in the S register, the TM counter will set to 3 and clear the TM designator. The TM counter values are also used to enable the XIRG and OTE status designators.

(n) BUFFER CONTROL. - See figures 8-14 and 8-15 (schematic diagrams) and figure 4-36 (timing chart). Buffer control is used by read control, during read type functions, for assembling computer words from the frames of data read from tape, transferring the assembled words into the C register if applicable, and sending an IDR to the computer if the word is to be transferred.

The R* register full flip-flop is set from read control, on Ø2 when data is early or on Ø4 when not early. The contents of the R* register stages are then transferred to the corresponding stages of the A subregister currently enabled by the character counter. If the character counter is not equal to 0, the computer word is not completely assembled, a frame has been lost, or the reading is being performed in a modulus other than that in which the tape was recorded. If the computer word is not completely assembled, the buffer control process is repeated until the complete computer word is assembled. When the computer word is completely assembled, the character counter is equal to 0 and the register full flip-flop is set.

During a read type operation, if a frame of data is not read (due to a bad spot on the tape for instance), read control does not run, buffer control is not initiated, and the value in the character counter does not change. Thus, to complete assembly of the current computer word, it is necessary to read an additional frame. The additional frame should be the first frame read for the next computer word. This transposing of a frame of data occurs in each computer word until an EOR. At EOR the last computer word (short one frame) remains in the A register with the character counter not equal to 0. As a result, the IDR cannot be sent to the computer. At EOR, when the status is gated into the C register, bit 8 of the C register is set (status word), thus notifying the computer of a lost frame.

When reading the tape in a modulus other than that in which it was recorded, frames will be transposed between assembled words in the same manner as when frames are lost. The result may be the same as for a lost frame. With a lost frame, the

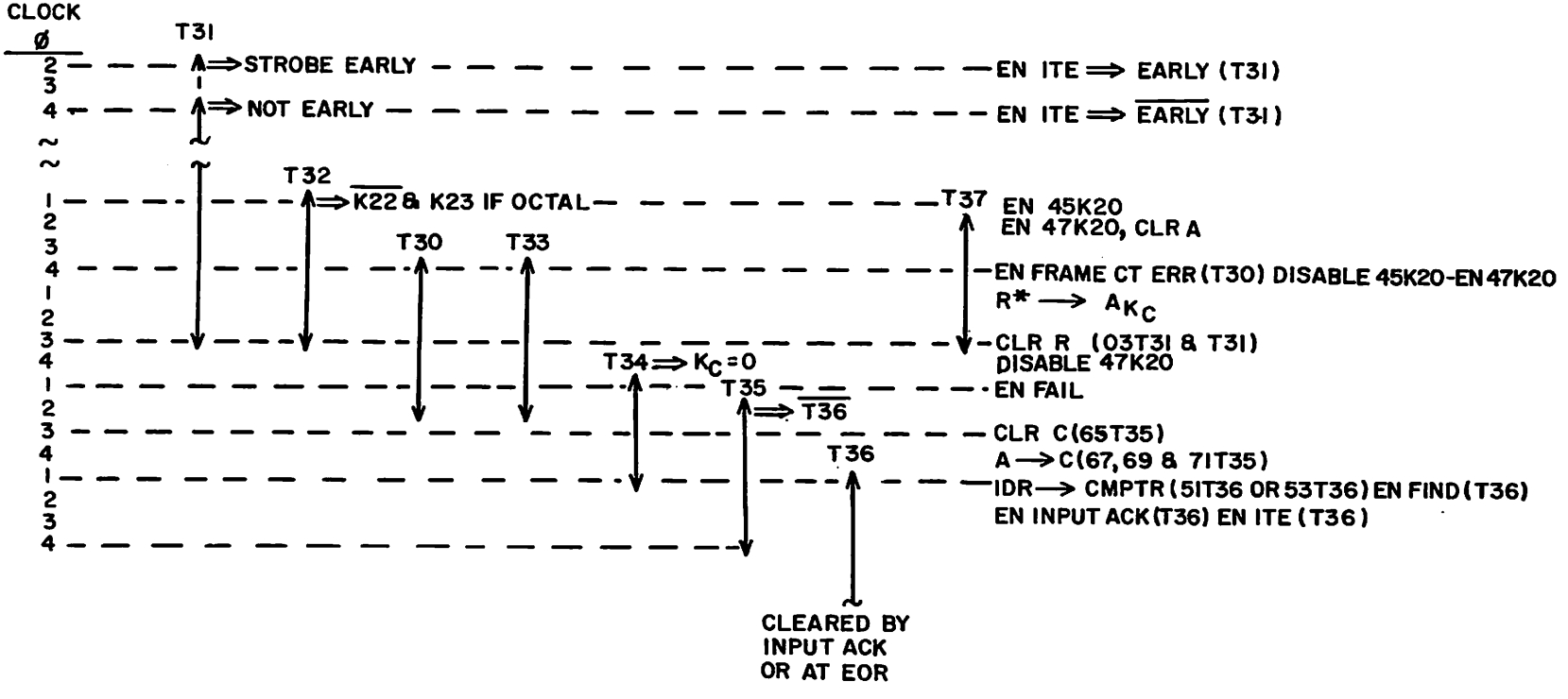


Figure 4-36. Buffer Control Timing

frame count error is noted in the status word along with a longitudinal parity error. However, when data is read in the wrong modulus, the frame count error is noted, but longitudinal parity will be indicated as correct. In either case, the extra frames of data that remain in the A register at EOR may be transferred to the computer by use of a transmit extra EF.

(o) END OF RECORD. - The EOR control sequence provides the necessary timing and command control for properly ending each function. When an operation is complete, the EOR stops the tape motion, enables the assembly of a status word in the C register, and enables an interrupt to be sent to the computer. The computer analyzes the status word to determine the degree of success achieved by the operation and to determine tape and handler status.

Operations are usually terminated each time read control detects the end of the record being processed (and interrecord gap (IRG)). However, some operations encompass more than one record and in others, the tape motion must be stopped and reinitiated in the opposite direction. The EOR control sequence has special restart circuits to continue or restart these types of operation.

For the following explanations see the end of record functional schematic diagram, figure 8-16.

The EOR may also be initiated from 50T06, in the start sequence (see figure 8-8).

1. NORMAL END OF RECORD. - The normal starting of the EOR is through an AND function that is satisfied when the tape mark counter is equal to 2 or 3 (at least two frames of data were read from tape), write control is inactive, the EOR counter equals 3, and read control is active.

When started, EOR clears the EOR counter and initiates an EOR clear (by way of master clear). When the EOR counter has counted to 4, EOR clears the RCD enables in the read register, sets the appropriate stop delay, clears the C register by way of I/O control, clears the ODR, and enables an ITE. If the computer has not accepted the last data word, the IDR in buffer control also enables the ITE designator and it sets. EOR enables the control circuits in the S register that clear the IDR, gates the contents of the S register into the C register, and sets an interrupt (of computer in control) in duplex control.

2. EOR RESTART OPERATION. - When an operation requires the tape movement to continue in the original direction through one or more IRG's, an EOR is initiated as each IRG is detected, but a restart is enabled in the start sequence. When the stop signal has cleared the motion flip-flop in the local tape handler control section, the start sequence is allowed to perform its functions. Before the relatively slow mechanical action required to stop the tape can take effect, the start sequence has reset the motion flip-flop and tape motion continues uninterrupted.

The operations that require the tape to be stopped and reinitiated in the opposite direction are also enabled from an EOR. However in these instances, a 20-millisecond time delay, initiated by the stop command, causes the tape movement to stop completely. The restart sequence is then allowed to run, initiating the tape movement in the new direction.

3. STOP DELAYS. - See figure 8-17 (schematic diagram) and figures 4-37 and 4-38 (timing charts). The stop delays are used to provide stop commands to the tape handlers at the proper time, by way of the local tape handler control, consistent with the function specified.

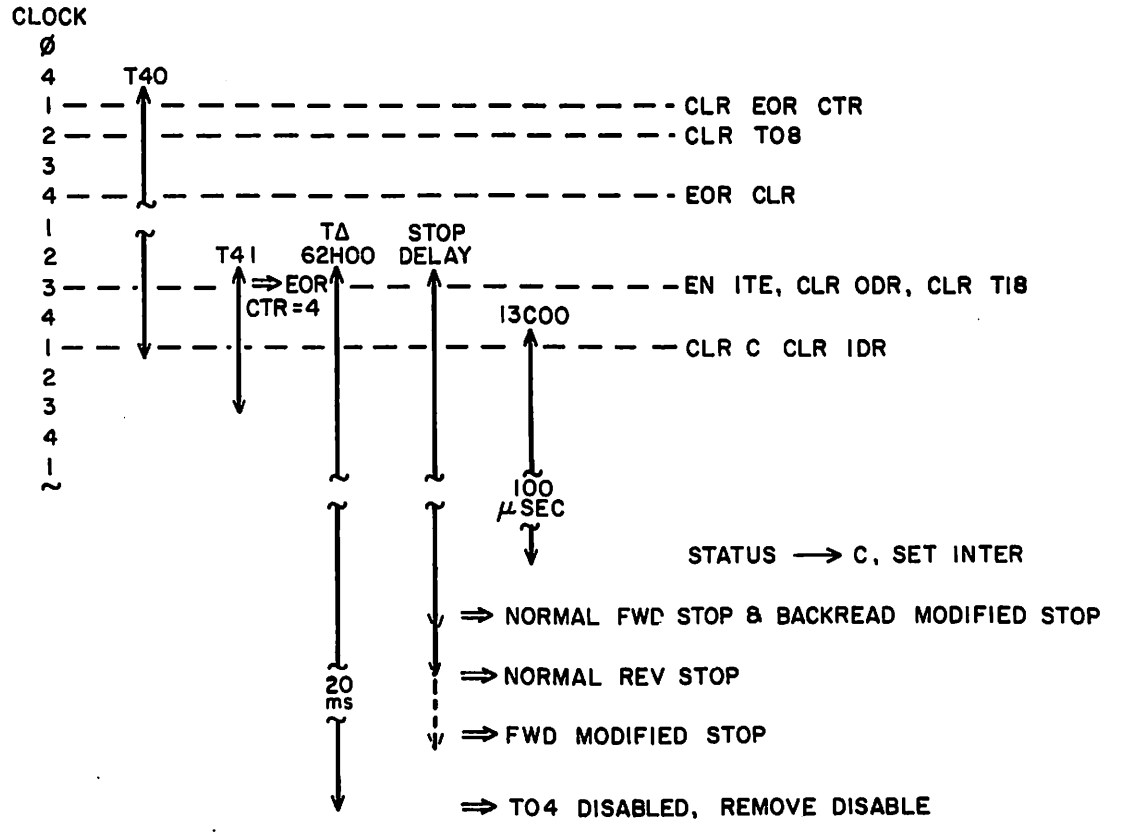


Figure 4-37. Normal EOR Timing

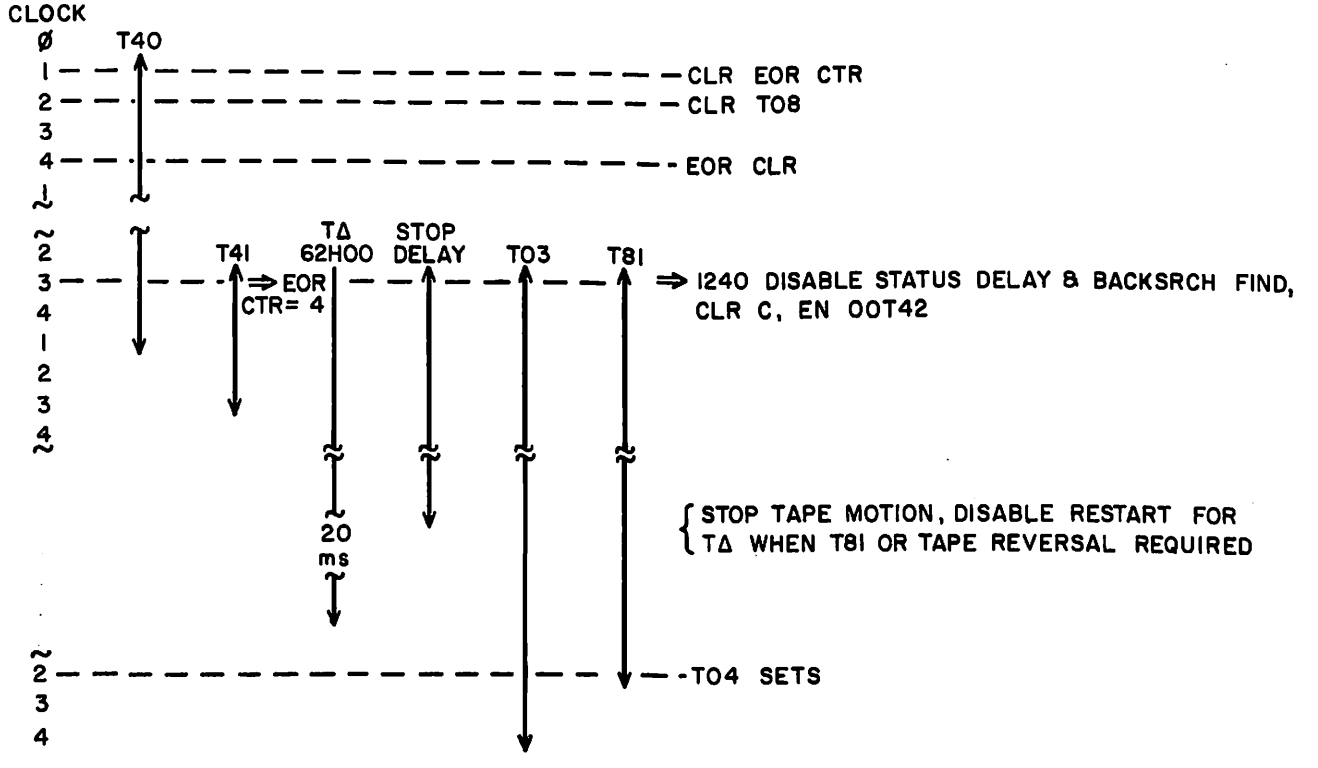


Figure 4-38. EOR Restart Timing

(p) SEARCH CONTROL. - See figure 8-13 Search control is used mainly by the EOR sequence for determining if a restart operation should be initiated for the space file, search, and 1240 backspace-read operations. It is also used to enable the setting of the IDR when a selective read comparison is satisfied.

1. SEARCH OPERATION. - For a search operation, read and buffer control assemble the data in the A register in the same manner as for a normal read. When the first word of each record has been completely assembled, a search comparison is made (the contents of the A register are compared to the search key in the C register). If the comparison is not satisfied, the same actions occur as those described for selective read; however during a search, the fail designator cannot be cleared until the start sequence clear, so the comparison is effective only for the first word of each record. At EOR, the operation is restarted and the first word of the next record is examined. This process is repetitive. When the first word of a record compares with the search key, the fail designator cannot set, the contents of the A register are transferred to the C register, and the IDR is set. The remainder of the find record is then read and sent to the computer in the same manner as for a normal read.

If an OTE (search key not returned by computer) or a parity error is detected, the fail designator, in search control, is set regardless of whether or not a compare has occurred in the A register. Under these circumstances, the error translations to the EOR sequence preclude a restart operation and a normal EOR ensues at the end of the record in which the error was detected. The computer is notified in the status interrupt that the search was not completed because of the OTE or parity error.

When the first word of a record compares with the search key and a parity error is not detected, the fail designator in search control cannot be set by buffer control. Buffer control will then function normally to clear the C register, gate the contents of the A register into the C register, and place an IDR on the control line to the computer. At the same time a find enable is sent to search control that sets a find designator. The find designator sends a command to the F register to clear the lower portion of the operation code so that it will reflect a read operation and to the EOR to prevent another restart. The remainder of the record is then read and transferred to the computer in the normal manner and a normal EOR completes the operation with a status interrupt. A search is limited only by a find, an error, an EOT or load point (depending on the direction of the tape movement).

The search file operations are performed in the same manner as described above for a search operation except that when a file marker (tape mark) is read before a find occurs, the normal EOR sequence is initiated in the same manner as described above for a space file.

2. 1240 BACKSEARCH. - The 1240 backsearch is initiated and performed in the same manner as that described above for a search operation except that a 1240 backsearch does not use the search control fail and find circuits that were discussed above. When in the 1240 mode, a reverse function translation to buffer control prevents the clearing of the C register, the gating of A to C, and the sending of an IDR to the computer. As each IRG is detected, and an EOR initiated, the last word read (first word of the record, as recorded) is still in the A register. A comparison takes place and if a no compare situation exists, the next record is read. When a comparison is satisfied at EOR, a 1240 backsearch find designator is set in search control. This designator clears the operation code in the F register and thus causes it to reflect a forward read. The EOR sequence runs in the restart mode

and after the start sequence initiates a normal forward read for the find record and performs a normal EOR sequence at the end of record.

3. 1240 BACK SPACE READ. - In a back space read operation, the tape moves in the reverse direction through one record. The EOR restart sequence clears the operation code in the F register. The start sequence then initiates a forward read operation that is terminated by a normal EOR sequence.

4. SPACE FILE OPERATION. - A space file or a back space file is started in the normal fashion with read control initiated from the start delays. Read control, in conjunction with buffer control, reads and assembles the data words in the A register. As the assembly of the first word of a record is completed, an enable fail signal from buffer control unconditionally effects the setting of the fail designator in search control. The fail signal is sent back to buffer control and prevents the setting of the IDR and the transfer of the A register to the C register. As the next frame of data is processed, the last word is cleared out of the A register by buffer control and the assembly of the next data word proceeds. This process repeats until the IRG is detected. Read control then initiates EOR in the normal manner. EOR then clears the EOR counter, initiates an EOR clear, disables the RCD's, sets the stop delay and sends a signal to EOR that prevents the clearing of the C register and to the S register control circuits that prevents the S to C transfer and the setting of the interrupt. When the stop delay expires, a stop command is sent to the LTHC, which, in turn, removes the "go" signal from the tape handler and removes the selected and running signal. The rest of the start sequence performs normally. The start commands are effective before the relatively slow mechanical actions of the tape handler have begun stopping the tape motion so the tape motion does not stop.

A space file operation will function in the same manner as described above, through any number of records, until a tape mark (file marker) is read.

(g) TAPE TRANSPORT CONTROL (SECTION(S) - See figure 4-5. Each tape transport control section performs a direct command control over its associated tape handler and provides other necessary functions as discussed in the following paragraphs. Each type transport control section consists of a local tape transport control section, a tape handler address switch, read amplifiers and detectors, and write amplifiers.

1. HANDLER ADDRESS SWITCH. - The HANDLER ADDRESS switch is used to select a tape handler by selecting its associated local tape transport control. When the HANDLER ADDRESS switch receives a select command from the start sequence, the switch setting is compared to the address bits in the C register and, if they are identical, the associate local tape transport control is selected.

See figure 8-68. The tape handler address amplifiers receive the address bits from the C register and amplify them for transmission to the LTTC, by way of the tape handler address switch(es).

2. LOCAL TAPE TRANSPORT CONTROL (LTTC). - The LTTC exercises direct control over one tape handler. The handler address switch selects the LTTC as described above. When the LTTC receives a start command from the start sequence, it analyzes the tape motion requirements of the function translation received from the F register and sends the appropriate "go" command(s) to the tape transport. When a rewind is specified and the tape handler indicates a low tape condition, LTTC commands a fast rewind. Tape status and handler status information is received from the tape handler and relayed, by way of the LTTC, to the S register or status gates. When

a read type or write operation is specified, the LTTC enables the read detectors. The write amplifiers are also enabled for a write operation. A stop signal from EOR causes the LTTC to remove the "go" signal from the tape handler and the tape motion ceases.

3. READ AMPLIFIERS AND DETECTORS. - The read amplifiers receive the small signals generated by the channel read heads, amplify them, and send them to the detectors. The detectors (enabled by their associated LTHC) further amplify the signals, shape them, and send them to the associated R register stages in magnetic tape control by way of the RCD's. The read heads are enabled by the read amplifiers whenever the power is turned on, but the read information is not available until the detectors are enabled by LTHC.

See figures 4-39, 8-32, 8-33, and 8-81 through 8-84. The read amplifiers receive the small signals generated by the read head (see A, figure 4-39), amplify them (see B, figure 4-39), and send them to the detectors. The detectors rectify the signal, at the level specified by the biasing designators in the function word, differentiate the rectified signal (see C, figure 4-39), and amplify and shape it into a logic signal (see D, figure 4-39).

4. WRITE AMPLIFIERS. - The write amplifiers, when enabled by LTHC, enable the write heads. The data received from the W register is amplified for driving the write head.

1540 write amplifiers are on figures 8-85 through 8-88. The write amplifiers, under control of the write register stages, control the direction of current flow through the channel write heads.

An enabling signal is provided to the write amplifiers from the selected local tape handler control section when write is specified by the function word, the select flip-flop is set, the write enable flip-flop is set, and the forward flip-flop is set for controlling the tape motion.

5. ELAPSE TIME INDICATORS. - The elapse time indicators (M1/M2) provide a means of measuring the actual time of tape movement across the read/write heads. The indicators receive a -4.5 vdc input directly from the forward flip-flops (see figures 4-5, 8-73, and 8-76). The indicators have been calibrated to give a full scale reading of 500 hours; this corresponds to a meter current of 20.8 microamperes. Since the indicators respond only to forward tape motion, the actual total tape motion time may be read directly from the indicators.

b. TAPE TRANSPORT(S). - The tape handlers perform the physical function of moving the tape in the direction, and at the speed, dictated by the LTHC. The handler heads perform the function of writing magnetically on the tape or of reading previously recorded data from the tape.

(1) FORWARD OPERATION. - When a forward operation code is gated into the F register, the enabled tape handler delay selectors are completely enabled and, in turn, enable the deskewing adjustments for the selected tape handler.

(2) REVERSE OPERATIONS (NOT REWIND). - For a reverse read type operation, the reverse flip-flop is set from the function amplifiers (see figure 8-72), and the tape handler starts moving the tape in a reverse direction.

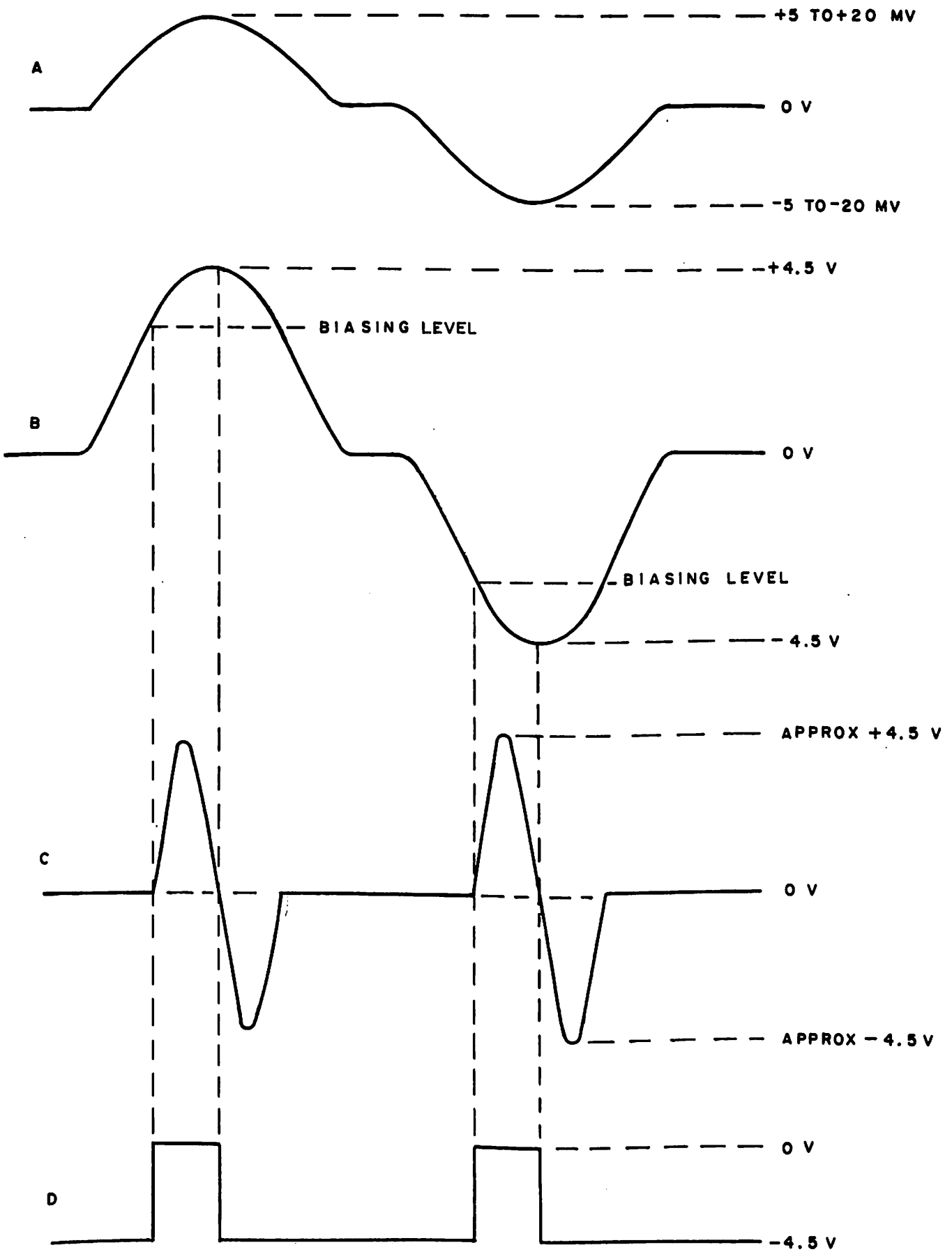


Figure 4-39. Read Amplifier and Detector Waveforms

a read type or write operation is specified, the LTTC enables the read detectors. The write amplifiers are also enabled for a write operation. A stop signal from EOR causes the LTTC to remove the "go" signal from the tape handler and the tape motion ceases.

3. READ AMPLIFIERS AND DETECTORS. - The read amplifiers receive the small signals generated by the channel read heads, amplify them, and send them to the detectors. The detectors (enabled by their associated LTHC) further amplify the signals, shape them, and send them to the associated R register stages in magnetic tape control by way of the RCD's. The read heads are enabled by the read amplifiers whenever the power is turned on, but the read information is not available until the detectors are enabled by LTHC.

See figures 4-39, 8-32, 8-33, and 8-81 through 8-84. The read amplifiers receive the small signals generated by the read head (see A, figure 4-39), amplify them (see B, figure 4-39), and send them to the detectors. The detectors rectify the signal, at the level specified by the biasing designators in the function word, differentiate the rectified signal (see C, figure 4-39), and amplify and shape it into a logic signal (see D, figure 4-39).

4. WRITE AMPLIFIERS. - The write amplifers, when enabled by LTHC, enable the write heads. The data received from the W register is amplified for driving the write head.

1540 write amplifers are on figures 8-85 through 8-88. The write amplifiers, under control of the write register stages, control the direction of current flow through the channel write heads.

An enabling signal is provided to the write amplifiers from the selected local tape handler control section when write is specified by the function word, the select flip-flop is set, the write enable flip-flop is set, and the forward flip-flop is set for controlling the tape motion.

b. TAPE TRANSPORT(S). - The tape handlers perform the physical function of moving the tape in the direction, and at the speed, dictated by the LTHC. The handler heads perform the function of writing magnetically on the tape or of reading previously recorded data from the tape.

(1) FORWARD OPERATION. - When a forward operation code is gated into the F register, the enabled tape handler delay selectors are completely enabled and, in turn, enable the deskewing adjustments for the selected tape handler.

(2) REVERSE OPERATIONS (NOT REWIND). - For a reverse read type operation, the reverse flip-flop is set from the function amplifiers (see figure 8-72), and the tape handler starts moving the tape in a reverse direction.

(3) REWIND OPERATION. - For a rewind function, the reverse flip-flop and the rewind flip-flop are set from the function amplifiers at time T05 of the start sequence. At time T06 of the start sequence, the EOR control sequence is initiated. At the conclusion of EOR, magnetic tape control is prepared to receive and process functions on another tape handler. The tape handler rewinds at high speed provided a low tape condition exists. When approximately 100 feet of tape remain to be rewound, the tape handler detects a high tape condition, thus removing the high-speed enable from the tape handler. The remaining tape will be rewound at normal speed. When load point is detected the reverse and rewind flip-flops are cleared from the tape handler.

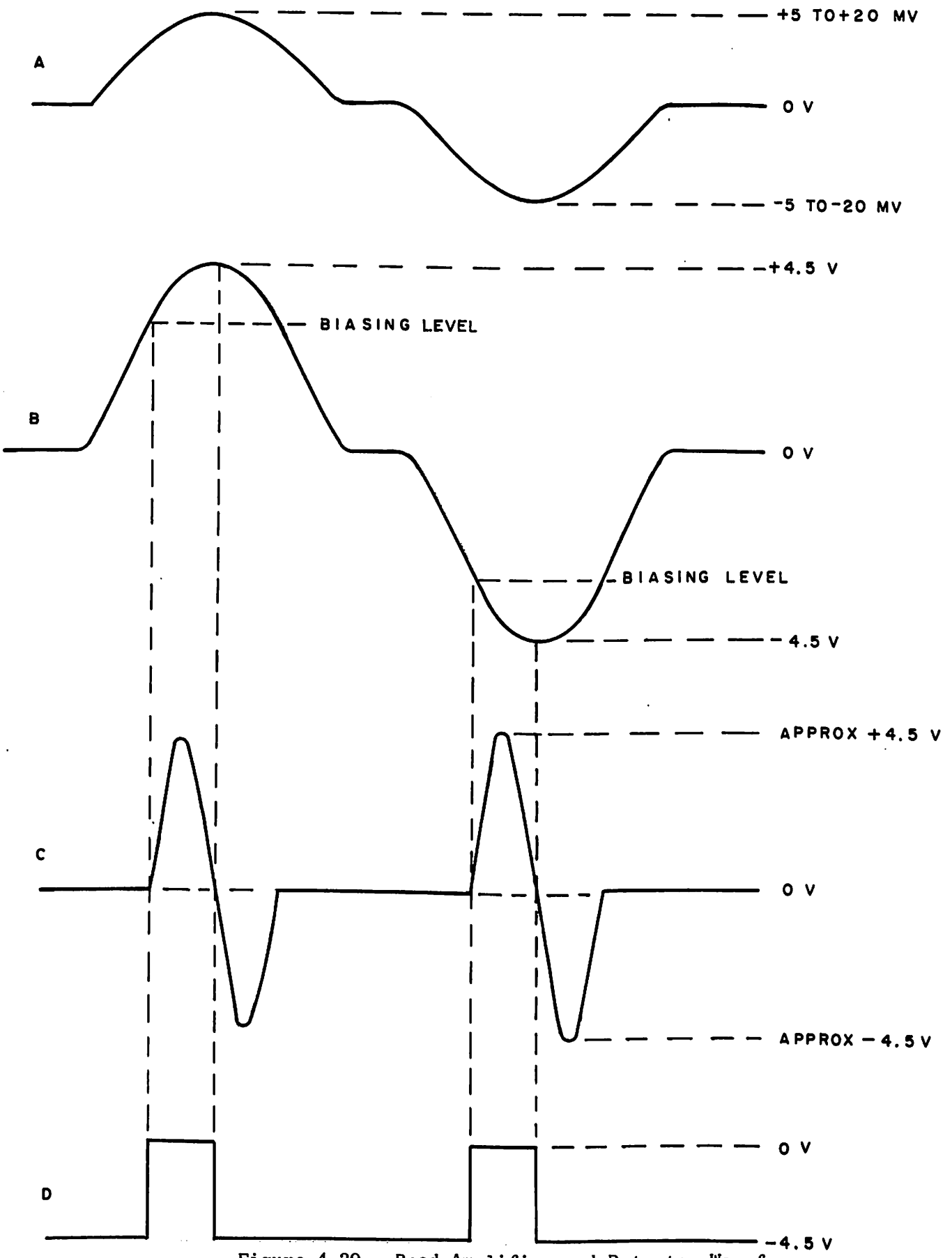


Figure 4-39. Read Amplifier and Detector Waveforms

When one or more of the sensor lamps is out, a clear disable is placed on the forward and reverse flip-flops. A function initiated under these conditions would result in an improved condition.

(4) MANUAL OPERATION. - When the HANDLER MAN-OFF-AUTO switch is set to the MAN position, a clear-disable is held. The motion flip-flops may be set by depressing the associated indicator-switches. End of tape and load point may be simulated by depressing the EOT or BOT indicator-switches. Depressing the STOP indicator-switch will clear any active motion flip-flop. The switch sections of these indicator-switches are active only in the MAN position of the HANDLER MAN-OFF-AUTO switch.

4-4. MANUAL CONTROL CIRCUITS.

A number of controls and circuits have been designed into the magnetic tape control section fo facilitate manual operation for maintenance, troubleshooting, and adjustment procedures. The MODE switch, CLOCK CONTROL switch, LOW SPEED-STEP switch, low speed oscillator, and handler test oscillator are discussed in the following paragraphs.

a MODE SWITCH, S7. - See figure 8-30. The MODE switch is a seven-position rotary switch which provides for normal operation with a computer in the NORMAL position, operation with a computer using 1240 Magnetic Tape Unit programs in the 1240 position, choice of four modes of test operation in the T1, T2, T3, and T4 positions, and operation with a UNIVAC Type 1469 High-Speed Printer in the PRINTER position. The explanation of each MODE switch position is given below.

(1) NORMAL. - The NORMAL position is used for automatic operation with a computer. The pushbutton switch section of all indicator-switches is disabled. All CLEAR switches, including MASTER CLEAR, are disabled and the clock is held in high-speed operation regardless of the CLOCK CONTROL switch setting.

(2) T1. - The T1 position of the MODE switch allows control of the MTU by a computer, by the maintenance and control panel, or by a combination of both. The switch portions of the indicator-switches and the CLEAR switches are enabled. Control of the clock is exercised by the CLOCK CONTROL switch (see figure 8-31).

(3) T2. - The T2 position of the MODE switch disables the I/O circuits, enables the switch sections of the indicator-switches, and enables the CLEAR switches. Clock control is maintained by the CLOCK CONTROL switch setting. Control of the MTU is exercised from the maintenance and control panels.

(4) T3. - In the T3 position of the MODE switch, the switch section of the indicator-switches is active, the CLEAR switches are active, and the clock is controlled by the position of the CLOCK CONTROL switch. An instruction manually inserted in the F register will be repeated each time the LOW SPEED-STEP switch is depressed or, in the LOW SPEED position, each time the low-speed oscillator provides a low output.

(5) T4. - The T4 position of the MODE switch allows control of the MTU, with 1240 MTU programming, to be exercised by a computer, by the maintenance and control panel, or by a combination of both. The switch section of the indicator-switches and the CLEAR switches are enabled. Control of the clock is exercised by the CLOCK CONTROL switch.

(6) 1240. - The 1240 position of the MODE switch enables a computer to control the MTU using 1240 MTU programs. The switch section of the indicator-switches is disabled. The CLEAR switches are also disabled and the clock is held in high-speed operation without regard to the position of the CLOCK CONTROL switch.

(7) PRINTER. - The PRINTER position of the MODE switch sets up circuits in the MTU so that data may be read from the tape and transferred to a UNIVAC Type 1469 High-Speed Printer. The CLEAR switches and the switch sections of the indicator-switches are active. Clock control is exercised by the CLOCK CONTROL switch.

b. CLOCK CONTROL SWITCH, S8. - See figure 8-31. CLOCK CONTROL switch S8 is a six-position rotary switch that is used to control the production of clock phases in the NORMAL, Ø STEP, and MULTI Ø positions. It is also used for Op step, skew test, and TD test operations.

(1) NORMAL. - With switch S8 in the NORMAL position, the clock phases will be produced at high speed as dictated by the density designators.

(2) OP STEP. - The OP STEP position of the CLOCK CONTROL switch causes the clock to run at normal high speed, but incorporates provisions for stopping the start sequence to visually inspect start sequence performance at the maintenance and control panel. OP STEP may be used with manual operation or with the computer.

(3) Ø STEP. - The Ø STEP position of the CLOCK CONTROL switch provides for producing clock phases one at a time.

(4) MULTI Ø. - The MULTI Ø position of the CLOCK CONTROL switch provides for producing a single clock phase repetitiously.

(5) SKEW TEST. - The SKEW TEST position provides for enabling/disabling read circuits and is used for a rapid overall check of the deskewing adjustments.

(6) TD TEST. - The TD TEST switch setting provides for triggering time delay circuits, at a rate determined by the low-speed oscillator, so that they may be observed on an oscilloscope and checked and adjusted.

c. LOW SPEED-STEP SWITCH. - See figure 8-90. The LOW SPEED STEP switch is a three-position toggle switch which is used in conjunction with the CLOCK CONTROL switch, MODE switch, low speed oscillator, and other circuits to manually control the clock and other operations of the MTU.

d. LOW-SPEED OSCILLATOR. - See figure 8-90. The low-speed oscillator produces pulses at a rate that is variable from approximately 2 to 200 cycles-per-second. In the LOW SPEED position of the LOW SPEED-STEP switch, the stepping operations are performed automatically at a rate determined by the low-speed oscillator.

e. TRANSPORT TEST OSCILLATOR. - See figure 8-31. The handler test oscillator produces pulses at a rate variable from approximately 0.3 to 40 cycles-per-second for use in performing the tape handler start-stop checks.

4-5. POWER CONTROL AND DISTRIBUTION.

a. INTRODUCTION. - The power and power control circuits include three basic elements; the primary power control unit (A2), the power supplies and the wiring harness, switches, blowers, and various other components which are either attached to or are integral parts of the cabinet assemblies.

(3) REWIND OPERATION. - For a rewind function, the reverse flip-flop and the rewind flip-flop are set from the function amplifiers at time T05 of the start sequence. At time T06 of the start sequence, the EOR control sequence is initiated. At the conclusion of EOR, magnetic tape control is prepared to receive and process functions on another tape handler. The tape handler rewinds at high speed provided a low tape condition exists. When approximately 100 feet of tape remain to be rewound, the tape handler detects a high tape condition, thus removing the high-speed enable from the tape handler. The remaining tape will be rewound at normal speed. When load point is detected the reverse and rewind flip-flops are cleared from the tape handler.

The operation of these circuits can best be explained by first describing a normal power sequence and then tracing the sequence of events in abnormal situations. For the following descriptions refer to the 1540 power circuits shown on figures 8-94 through 8-97.

Primary power is brought into the MTU by way of filter assemblies A4FL-1 through A4FL-5 and routed to primary power control unit A2.

The power fuses for the Type 1540 MTU are mounted on the front panel of primary power control unit A2.

b. NORMAL OPERATION. - The primary power control POWER ON-OFF switch, A11S1, is located on the top front of the magnetic tape control section. It is a three-position, momentary-contact, toggle switch, spring loaded to the center position. When A11S1 is set to the ON position, it actuates the relays which, in turn, apply power to the blowers, the handler POWER switch, and the logic power supply. The relays also partially establish the circuits which supply the power to the individual tape handlers.

When the primary power control POWER switch A11S1 (see figure 8-96) is set to the ON (up) position, relay K6 is energized. The 115-vac circuit is completed from Ø3 at K6-C2 (see figure 8-94 or 8-95) to Ø2 by way of J2 and A4P16-m, TB4-1, across contacts 4 and 5 of A11S1, TB4-2, A4P16, and J2-j, the normally closed contacts of K5, the coil of K6, J2 and A4P16-S, TB8-8, interlock S1, TB8-9, TB6-6, thermoswitch S5, TB6-5, A4P16, and J2-T. It may appear at first glance that relays K6 and K5 should energize at the same time, however, resistor R2, in series with the coil of K5, does not pass enough current to allow it to energize. When K6 has been energized, K5 is energized by way of the normally open contacts C2 and C1 of K6. When POWER switch S1 is released, the holding power for relay K6 will be maintained by way of the normally open contacts D1 and D2 of K5 and resistor R3.

When K6 is energized, three sets of contacts close to supply regulated, three-phase, 115-vac, 400-cylic power to logic power supply PS-1 and to the -26.5 volt power supply (see figure 8-101). When the dc power is up, +15 volts is supplied by way of W4, J1 and A10P1-R, W5, W1, J11-60, an interconnecting cable (not shown), J1-60 (see figure 8-96), TB7-5, and TB3-7, to light the LOGIC indicator A11DS-1. W1 supplies +15 volts (see figure 8-109), by way of J11-61, an interconnecting cable (not shown), J1-61 (see figure 8-96), TB7-6, A4P16, and J2-U, to energize relay K1. Relay K1 connects the -15 volts present at A4P16 and J2-d to the write enable amplifiers (60M20 and 50M70) of each tape handler, by way of J2 and A4P16-C, and A4P14 and J2-48. As the -26.5 volt supply rises to full value, the OVERTEMP warning sensors (thermoswitches S2 and S4) are enabled by way of P1 and A4A2J1-A10 (see figure 8-101), J11-63 (see figure 8-113), an interconnecting cable (not shown), J1-63 (see figure 8-96), TB7-7, TB4-7, and TB6-3. Switch S4 is enabled from TB6-3, by way of TB6-7.

When relay K5 is energized, power is supplied to the magnetic tape control section blower(s) (B6 and/or B5), by way of J2 and A4P16-L, and M. The power supplied to the blowers also lights the BLOWERS indicator A11DS-2.

The handler POWER ON-OFF switch, A1S1, is the same type as the control POWER switch described above. When set to the ON position, it activates a relay that enables power to be supplied to the tape handler(s) and energizes the blowers in the tape handler section.

When the handler POWER ON-OFF switch, A1S1, is set to the ON (up) position, Ø2 power is routed to Ø3 through the normally open contacts of relay K1, the coil of relay K2, J2 and A4P16-4, TB3-2, contacts 4 and 5 of the switch, TB3-1, TB4-1, and A4P16 and J2-m, energizing relay K2. The power is then routed, by way of the normally open contacts of K2 and pins H and F of J3 and A4P16, to energize blowers B2 and B4 and/or B1 and B3. Another set of normally open contacts of K2 provide a path for Ø3 to Ø2, by way of the coils of relays K3 and K4, J1 and A4P15-H, TB3-5, TB6-1, thermoswitch S3, TB6-5, and A4P16 and J2-T, for energizing relays K3 and K4. The normally open contacts of K3 and K4 then route 60-cycle power to the tape handlers. When switch A11S1 is released, the holding power for relay K2 is maintained by way of R1, J2 and A4P16-e, TB3-3, pins 1 and 3 of A11S1, TB3-6, A4P16 and J2-g, and the normally open contacts of K2.

When the HANDLER 1 MAN-OFF-AUTO switch, A1S2, is set to the MAN or AUTO position, the circuits for energizing relay K9 are completed. The TB7-7 routes -26.5 volts for AUTO (see figure 8-96), by way of TB4-7, A4P16 and J2-V, the coil of K9, J2 and A4P16-k, TB3-4, and to ground by way of S2A pin 1 and C, for MAN, or pin 3 and C. The normally open contacts of K9 now complete the handler 60-cycle power circuits (within the tape handler), by way of J2 and A4P16 pins s and p and the handler interlocks. For the Type 1540 MTU, relay K7, in conjunction with the HANDLER 2 MAN-OFF-AUTO switch S6, performs in a similar manner for handler 2. When a handler is energized, its associated RUNNING TIME meter, M1 or M2, is activated.

To remove all power from the system, it is only necessary to set primary power control POWER ON-OFF switch A11S1 to the OFF (down) position. This action opens contacts 1 and 3 of A11S1 thereby deenergizing relay K6 and, in turn, K5 thus opening the primary power lines. Since the power to the tape handlers is conditioned on relay K1, which is also dependent on the primary power, the tape handler power will be interrupted. However, during normal turnoff, the more prudent sequence would to be (1) remove the power from the individual tape handlers by setting the MAN-OFF-AUTO switches to OFF, (2) remove the power from the handler section by setting POWER switch A1S1 to OFF, and (3) setting control POWER switch A11S1 to OFF.

c. HIGH-TEMPERATURE PROTECTION. - The power circuits are protected from high-temperature operation by two thermoswitches in each cabinet section; one opens at 60°C (140°F) and the other one closes at 46°C (115°F). The 46°C (115°F) switches, when activated, cause an audible alarm to sound which is a warning that the cabinet temperature has risen to an abnormal value. If the temperature continues to rise and reaches 60°C (140°F), the power is automatically shut down. These processes are described in the following paragraphs.

(1) OVER TEMPERATURE WARNING. - When the temperature in one of the cabinet sections rises to 46°C (115°F), the appropriate thermoswitch (S2 or S4) closes and applies -26.5 volts to the associated OVER TEMP indicator. When an over temp condition occurs in the logic section, thermoswitch S4 closes (see figure 8-97). OVER TEMP indicator DS-4 is lighted by -26.5 volts from TB7-7 by way of TB4-7, TB6-3, TB6-7, thermoswitch S4, TB6-8, and TB4-8 through DS-4 to ground. Relay K8 is energized by -26.5 volts from TB4-8 by way of A4P16 and J2-W, diode CR3, J2 and A4P16-n, TB4-5, pins 5 and 4 of BYPASS-NORMAL switch S2, TB4-6, A4P16 and J2-h, and the coil of relay K8 to ground. The normally open contacts of K8 provide a path for +15 volts to horn LS-1, causing an audible alarm to sound. The horn is mounted on power control unit A2 in the handler section.

Placing the ALARM BYPASS-NORMAL switch in the BYPASS position opens the energizing path for the horn and supplies -26.5 volts to the ALARM ON indicator, A11DS3.

The other circuits are not affected. Over temp warning circuits for the handler section function in a similar manner.

NOTE

Limited operation under these conditions will not cause damage to the unit, but the unit's reliability may decrease considerably.

(2) OVER TEMPERATURE SHUTDOWN. - When the temperature in one of the cabinet sections rises to 60°C (140°F), the associated thermoswitch (S3 or S5) will open and thereby remove the power from the coil of relay K6. When the contacts of K6 are open, the dc (logic) power is interrupted which results in deenergizing relay K1. This, in turn, causes the removal of power from the handler section and all of the power, except the blower power, from magnetic tape control section. When the temperature in the overheated cabinet section drops below 60°C (140°F), the thermoswitch closes and all power is restored. If an over temperature shutdown occurs, set the HANDLER POWER switches to the OFF position to prevent any personal injuries which might occur if the power is restored while someone is handling the tape reels.

SECTION 5

MAINTENANCE

5-1. GENERAL.

The information presented in this section is intended to acquaint maintenance personnel with the preventive maintenance, troubleshooting, and corrective maintenance procedures that may be used with the system. Many of the troubles encountered in a system can be eliminated by strict adherence to the preventive maintenance schedules. However, when a fault occurs, it can be isolated to a specific section of a subassembly through visual, electrical, and dynamic testing. Careful analysis of the fault indications and a thorough knowledge of the system are the most useful tools for troubleshooting. Under these conditions, unnecessary time is eliminated.

5-2. PREVENTIVE MAINTENANCE.

The following preventive maintenance procedures are separated into daily, weekly, bi-weekly, and monthly categories and are to be performed as indicated. Use the Preventive Maintenance Chart, table 5-1, as a check-list and a record keeping device.

a. DAILY MAINTENANCE.

(1) CLEANING PROCEDURES. - Clean the entire front panel, record/playback head surface, and all other surfaces contacted by the tape such as bridge rollers, pinch rollers, trough guides, capstans, tension arm rollers, end-of-tape sensors, and inside surface and cover of the vacuum buffer with compressed air. Then use Vithene D, a commercial solvent available with the Potter Cleaning Kit, Part No. #425484, or from Tect Inc., Northvale, N.J., or Dupont Freon TF. (Use solvent sparingly.)

Carefully clean drag pads with brush or compressed air. The drag pads can be loosened from their bond if care is not used.

Clear the bleed holes in the vacuum buffer with compressed air and a toothpick or similar instrument.

Each time a new roll of magnetic tape is placed on the transport, see that the tape is free in the guidance system, and that all rollers are properly rotating before applying power to the system.

(2) MAINTENANCE TESTS. - The maintenance tests are controlled tests which provide for computer checkout of the MTU to determine its functional capabilities. The maintenance tests and test procedures are contained in the following UNIVAC publications.

a) PX3644-0-1 - Maintenance tests for Type 1540 Magnetic Tape Unit used with UNIVAC Type 1218 and 1219 Computers.

b) PX3645-0-1 - Maintenance tests for Type 1540 Magnetic Tape Unit used with UNIVAC Type 1206, 1212, 1230 and CP-667 Computers and CP-642/USQ-20 (V) CP-642A/USQ-20 (V) CP-642B/USQ-20 (V), MCP-667 Military Computers.

TABLE 5-1. PREVENTIVE MAINTENANCE CHART

SCHEDULE	PROCEDURES		DATE	EXTRA WEEKS
Daily	Cleaning Maintenance Checks	Monday		
		Tuesday		
		Wednesday		
		Thursday		
		Friday		
Weekly	Select Transport			
	Write All Ones - Check Start Stop			
Biweekly	Vacuum - Clean Filters			
	Power Check			
Monthly	Time Delay Checks			
	Voltage Regulator/Bias			
	Read Amplifier Checks			
	Read Detector Checks			
	Read Deskewing Checks			
	Write Deskewing Checks			
	Read Reverse Deskewing Checks			
	Erase Head Polarity Checks			
	Overtemp Sensor Check			

Record date and check-off P.M. procedures as you perform them. Take corrective action on abnormalities immediately.

b. WEEKLY MAINTENANCE.

(1) AIR FILTER CLEANING PROCEDURE. - The air filters for air-cooled tape units are located behind the grill(s) above the primary power control panel(s) at the top front of the MTU. To accomplish filter cleaning, proceed as follows.

STEP 1. Turn quarter-turn fasteners on grill 90 degrees counterclockwise.

STEP 2. Swing grill upward and lift out filter.

STEP 3. Vacuum clean filter.

STEP 4. Replace filter, ensuring that spring clips are against grill and not cabinet.

STEP 5. To secure grill, depress and turn quarter-turn fasteners 90 degrees clockwise.

(2) POWER CHECK. - Complete the following steps.

STEP 1. Open upper servo transport door(s) on basic unit and each add-on unit.

STEP 2. Turn power on at junction box on main control panel.

STEP 3. See figure 5-1 for location of terminal connections.

STEP 4. See table 5-2 for values of input power and test point locations.

STEP 5. If all voltages check out properly proceed to step 6. If not, recheck source; then with power off check cable connections.

STEP 6. Set primary power control panel POWER switch to ON. Set tape handler control panel POWER switch to ON. All blowers should be running and all power indicators should be lit. Also check that all blowers are turning in proper direction, pulling air thru air filters, and exhausting air out exhaust grill.

STEP 7. Check dc voltage levels on chassis A13A1, A13A2, A12A1, A12A2, and A17 (see table 5-3).

STEP 8. If deviations from tolerances are uniform, readjust regulated 400-cycle voltage or troubleshoot power supplies.

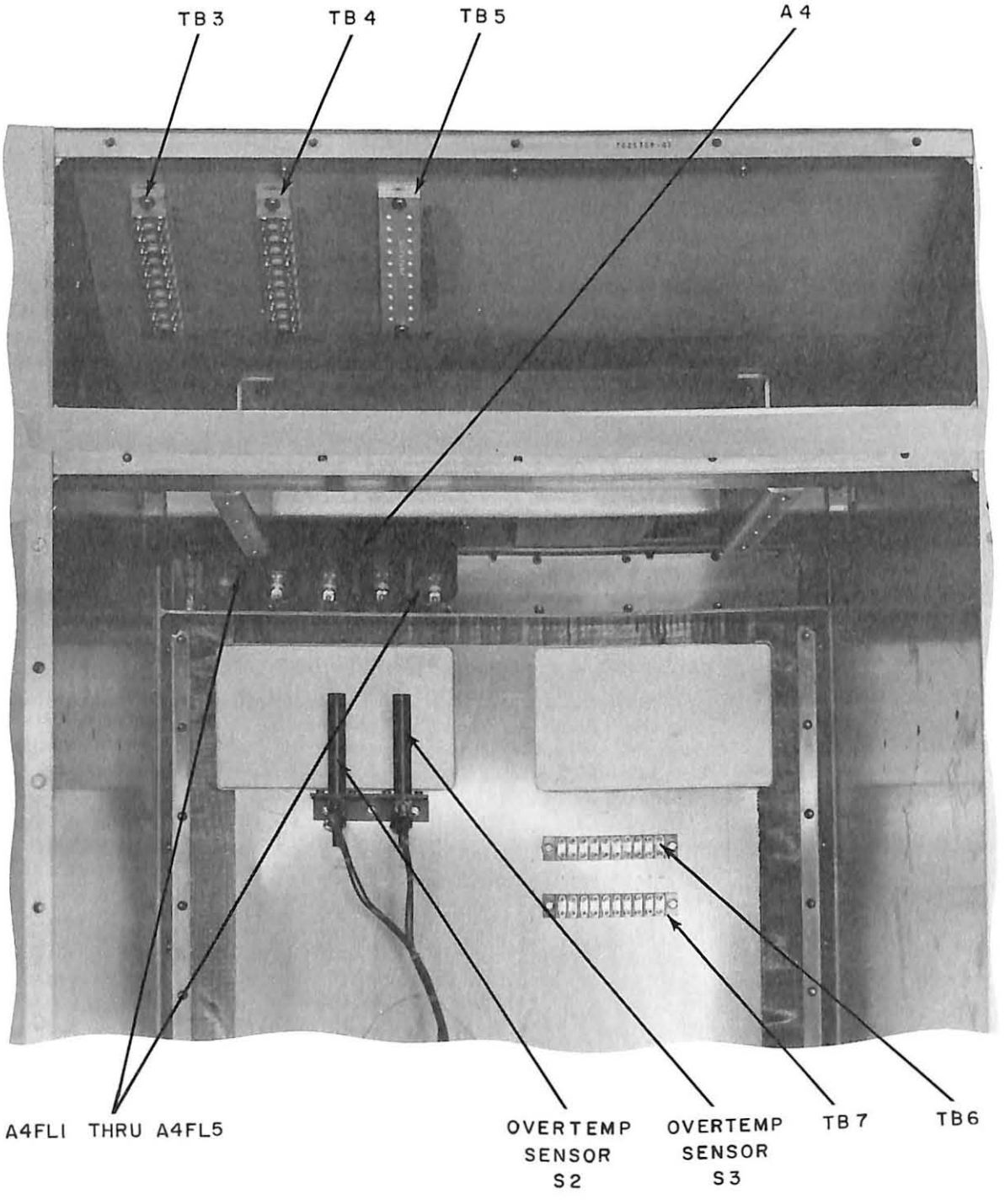


Figure 5-1. Tape Transport Cabinet, Partially Assembled View of Upper Half, Air Cooled

TABLE 5-2. AC POWER DATA

TERMINAL CONNECTIONS	CHARACTERISTICS	LINE-TO-LINE POTENTIAL	LINE-TO-GROUND POTENTIAL	FUSING		VALUE BASIC UNIT	(AMPS) ADD-ON UNIT
				1541 FUSE	1540 FUSE		
A4FL1	60-cycle, unregulated	115 volts ±10%	--				
A4FL2	60-cycle, unregulated	115 volts ±10%	-- --				
A4FL3	400-cycle, phase 1, regulated	115 volts ±5%	65 volts	A1F1	A2F11	10	1
A4FL4	400-cycle, phase 2, regulated	115 volts ±5%	65 volts	A1F2	A2F12	10	1
A4FL5	400-cycle, phase 3, regulated	115 volts ±5%	65 volts	A1F3	A2F13	10	1
A4E2	Power ground	--	--	--	--	--	
E1	System ground	--	--	--	--	--	

TABLE 5-3. DC POWER DATA

TEST POINT CHASSIS A13A1-A2 A13A2-A2	LINE-TO-GROUND POTENTIAL	MAXIMUM RIPPLE (VOLTS)	FUSE	PHASE	VALUE (AMPS)
TB1-B33	-26.5 vdc ±2.7v	3.0	A13A1F1*	-	6
TB1-C31	+26.5 vdc ±2.7v	3.0	A13A1F2*	-	6
TB1-D33	+15 vdc ±0.8v	0.2	PS1F7**	1	2
			PS1F8**	2	2
			PS1F9**	3	2
TB1-E33	-15 vdc ±0.8v	0.2	PS1F4**	1	3
			PS1F5**	2	3
			PS1F6**	3	3

TABLE 5-3. DC POWER DATA (CONT)

TEST POINT CHASSIS A13A1-A2 A12A2-A2	LINE-TO-GROUND POTENTIAL	MAXIMUM RIPPLE (VOLTS)	FUSE	PHASE	VALUE (AMPS)
TB1-F33	-4.5 vdc ±0.1v	0.5	PS1F1**	1	1.5
			PS1F2**	2	1.5
			PS1F3**	3	1.5
TB1-G33 A-17	Ground	-	-	-	-
TB2-A2	+15 vdc ±0.8v	0.2	SAME	SAME	SAME
TB2-A3	-15 vdc ±0.8	0.2	AS	AS	AS
TB2-A4	-4.5 vdc ±0.1v	0.5	ABOVE	ABOVE	ABOVE
TB2-A1	Ground	-	-	-	-

* 26.5-volt fuses are located on chassis A13A1.
** DC power supply PS1 is fused on the 3-phase primary inputs to each dc supply transformer with non-indicating type fuses. Fuses are physically located in the dc power supply drawer located in the bottom of the magnetic tape control section.

c. BIWEEKLY MAINTENANCE.

(1) TRANSPORT START-STOP CHECKS. - Complete the following steps.

STEP 1. Set HANDLER ADDRESS switch to desired address on transport to be checked. Set all other HANDLER ADDRESS switches to any other position.

STEP 2. Load blank tape with write ring installed.

STEP 3. Set MAN/OFF/AUTO switch to AUTO.

STEP 4. Set bits 14 and 15 in C REGISTER.

STEP 5. Set bits in C REGISTER to the previously selected address. (See table 5-4.)

TABLE 5-4. TRANSPORT ADDRESS CODES

ADDRESS	C REGISTER 4 3 2 1 0	ADDRESS	C REGISTER 4 3 2 1 0
1	0 1 0 0 1	9	1 1 0 0 1
2	0 1 0 1 0	10	1 1 0 1 0
3	0 1 0 1 1	11	1 1 0 1 1
4	0 1 1 0 0	12	1 1 1 0 0
5	1 0 0 0 1	13	0 0 0 0 1
6	1 0 0 1 0	14	0 0 0 1 0
7	1 0 0 1 1	15	0 0 0 1 1
8	1 0 1 0 0	16	0 0 1 0 0

STEP 6. Set MODE switch to T2.

STEP 7. Set CLOCK CONTROL switch to OP STEP.

STEP 8. Set indicator 1 in START SEQ. Indicator 3 lights.

STEP 9. PRESS LOW SPEED/STEP switch. SELECT INDICATOR on transport should stay on; transport should attempt a rewind.

STEP 10. Master Clear.

(2) WRITE ALL ONES AND START-STOP CHECK.

STEP 1. Set bits 14 and 7 in FUNCTION REG.

STEP 2. Set 800 B.P.I. density indicator in clock.

STEP 3. Set indicator 3 in start sequence.

STEP 4. Set lower 18 bits of C REGISTER. Allow tape to write to E.O.T. marker and press LOW SPEED/STEP switch.

STEP 5. After transport has stopped at E.O.T. set MAN/OFF/AUTO switch to manual.

STEP 6. Set REVERSE indicator for transport. Press STOP switch when transport is approximately in center of reel of tape.

CAUTION

The oscillator output card is easily damaged. Do not ground it.

STEP 7. Jumper test oscillator to following test point for handler being checked. This causes transport to move in the direction specified.

TT#1
A13A1 TB2-G10 ---------- TB1-C2 A17 reverse
A13A1 TB2-G10 ---------- TB1-B8 A17 forward
TT#2
A13A1 TB2-G10 ---------- TB2-C2 A17 reverse
A13A1 TB2-G10 ---------- TB2-B8 A17 forward

STEP 8. Sync external on oscillator output A13A1-G10.

STEP 9. Connect oscilloscope lead to TP1 on any read amplifier module on chassis A17 of transport under test (see figure 5-2).

STEP 10. **Sync positive and look at read amp for transport being checked. Check start time in each direction. Vary speed of oscillator by speed adjust control. Try oscillator in both fast and slow range. Start time remains constant as shown in figure 5-3.

STEP 11. **Sync negative and look at read amp for transport being checked. Check stop time. Vary speed of oscillator as in step 10. Stop time remains constant as shown in figure 5-3. Check it in both directions.

STEP 12. **Repeat steps 6 through 12 for each transport.

** See the Potter manual for adjustment procedure.

NOTE

The preceding procedure is also used for Type 1540 add-on units. Failure of the start/stop checks may be caused by the following conditions: 1) pinch rollers out of adjustment, 2) pressure pads out of adjustment, 3) improper vacuum.

For readjustment procedures, refer to section 6 of Potter tape handler manual. The transport test oscillator is used as the square wave generator called out in the handler manual.

d. MONTHLY MAINTENANCE.

(1) TIME DELAY CHECKS/ADJUSTMENTS - For the following checks/adjustment, it is assumed that power turn on has been accomplished and voltage checks have been completed. To check all delays except 49T06 (see table 5-5), complete the following steps. Another method of setting the delays is to run maintenance routines and use the normal operating pulse.

STEP 1. Set MODE switch to T1.

STEP 2. Set CLOCK CONTROL switch to TD TEST.

STEP 3. Using external sync, connect oscilloscope leads, in turn, to test points indicated in table 5-5. It is advisable to display sync while setting delays so that no sync mistake is made. 2 ms error can be realized due to width of test signal.

STEP 4. For delays that do not correspond to values listed in table 5-5, adjust resistor to delay module. Module locations are listed in table 5-5.

NOTE

The time delay test signal is about 2 ms in duration. If the delay under test is less than 2 ms, the delay output terminates at the proper time but immediately resets due to the long test pulse. The first voltage spike occurs when the delay is set.

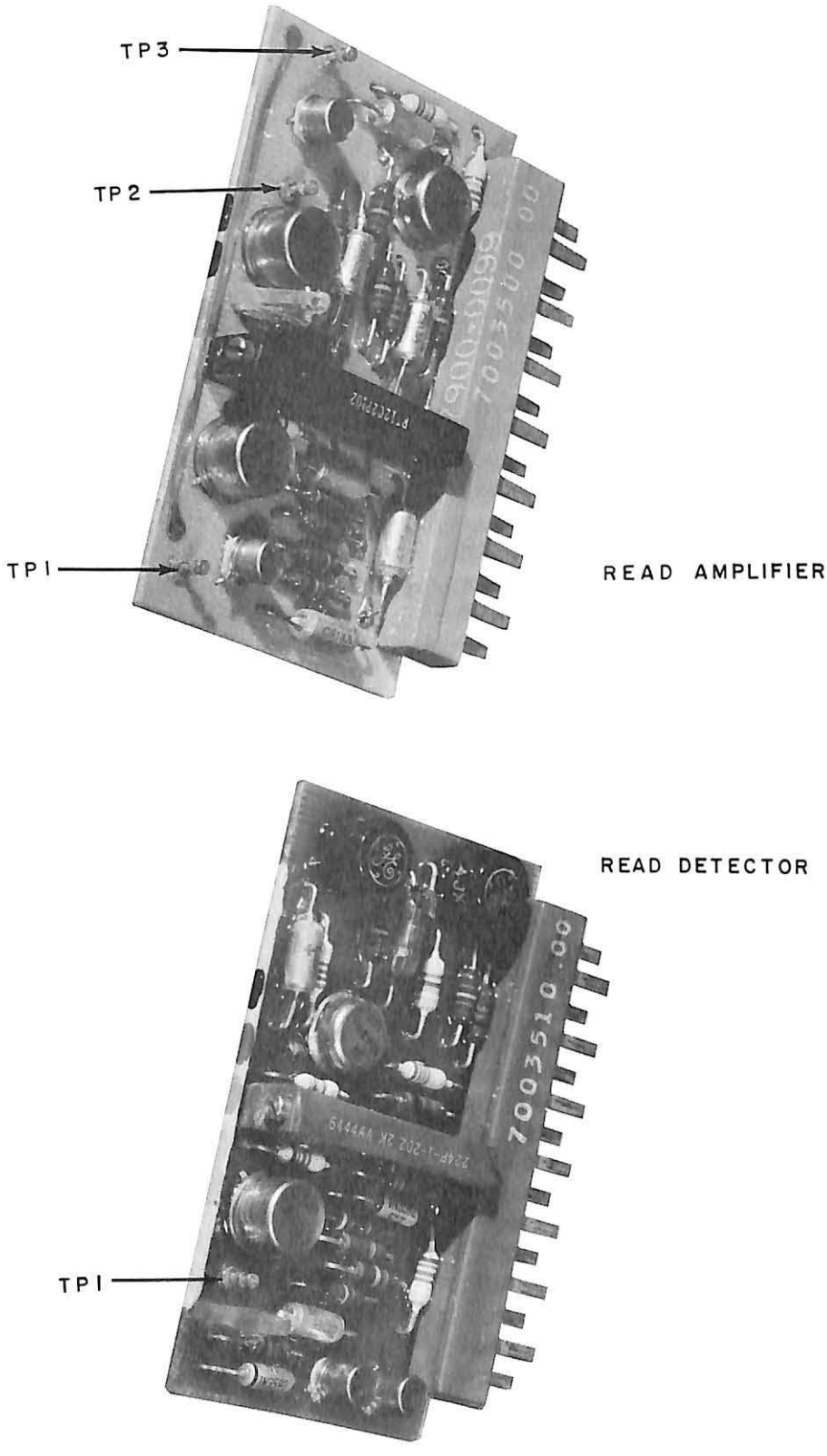


Figure 5-2. Read Detector and Amplifier Test Points

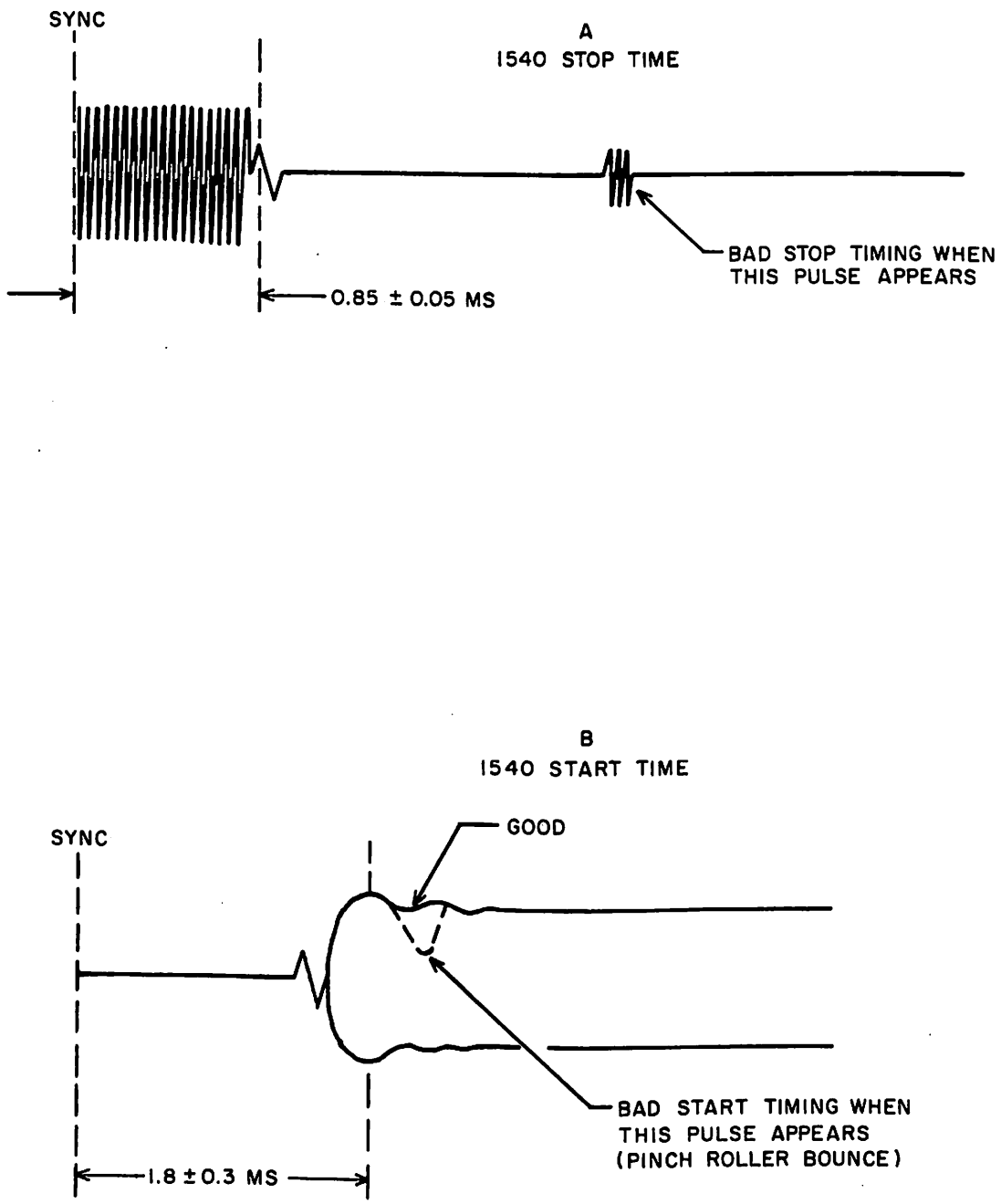


Figure 5-3. Transport Start-Stop Check Waveforms

TABLE 5-5. TIME DELAY CHECKS/ADJUSTMENTS

FIGURE NUMBER	TERM	CHASSIS	SYNC AT TEST POINT	READ AT TEST POINT	MODULE LOCATION	DELAY TIME	PULSE POLARITY	NAME
8-17	64H00	A13A1	TB2C1	TB2B4	J33D	1.08 ms	POS	Reverse position
8-17	58H00	A13A1	TB2F4	TB2D4	J33E	2.0 ms	POS	Normal stop
8-9	48H01	A13A1	TB2G3	TB2E3	J35F	2.0 ms	POS	Read
8-17	56H00	A13A1	TB2G1	TB2E4	J34E	4.1 ms	POS	Modified Stop
8-9	58H01	A13A1	TB2E1	TB2C1	J33F	4.5 ms	POS	Write
8-17	62H00	A13A1	TB2C4	TB2A4	J34D	20.0 ms	POS	Reverse Direction and select.
8-9	19H02	A13A1	TB2G3	TB2F3	J35E	20.0 ms	POS	Load Point Read
8-9	56H01	A13A1	TB2F1	TB2D1	J34F	21.0 ms	POS	XIRG
8-23	13C00	A12A1	TB2E20	TB2G20	J34E	100.0 used	NEG	Status to C
8-12	49T26	A12A2	TB2A25	TB1G11	J24F	*7.0 used **1.2 used	POS	Interface
8-15	49T36	A12A2	TB2B25	TB2C25	J23F	*7.0 used **1.2 used	POS	Interface
8-8	49T06	A12A1	TB1E32	TB2F26	J34G	3.0 ms	POS	Write Emergency Stop

To check the delay of 49T06, proceed as follows.

STEP 1. Select desired transport; see paragraph 5-3 f1.

STEP 2. Set MODE switch to T3.

STEP 3. Ground TB1D14 12A2. (20T10 inhibits read control.)

STEP 4. Master clear; ensure C REGISTER is cleared.

STEP 5. Insert write tapemark instruction (01110) in F REGISTER.

STEP 6. Depress START SEQUENCE indicator - indicator 3.

STEP 7. Set LOW SPEED - STEP switch to LOW SPEED.

(2) VOLTAGE REGULATOR/BIAS ADJUSTMENTS

(a) VOLTAGE REGULATOR ADJUSTMENTS - The voltage regulator adjustments listed below should be completed before any other adjustments are attempted. Perform the voltage regulator adjustments by carefully completing the following steps. The multimeter used must reflect a minimum of 2,000 ohms - per volt on the scales used.

CAUTION

Insulate the ends of the probes so that they cannot short out to chassis. A short will result in damage to the modules.

STEP 1. Set MODE switch to T-2.

STEP 2. Set LOW SPEED/STEP switch to NORMAL.

STEP 3. Set CLOCK CONTROL switch to OP STEP Master Clear.

STEP 4. Set -15V.R.A13A1-C33 Test point A13A1 TB1-A33. (DESKEWING)

STEP 5. Set +15V.R.A17 32B Test Point TB2-M4 Top pot.

STEP 6. Set -15V.R.A17 15C Test point TB2-M7.

STEP 7. Repeat steps 5 and 6 for each add on cabinet.

(b) TRANSPORT 1 BIAS SUPPLY ADJUSTMENT.

STEP 1. +15 V.R. and -15V.R. must be adjusted before adjusting bias.

STEP 2. Place negative meter lead in TB2-M4.

STEP 3. Place positive meter lead in TB-1-15.

STEP 4. Set bit 3 in FUNCTION REG.

STEP 5. Adjust resistor farthest from chassis front on A17-C32. Set for +.3 vdc.

STEP 6. Clear F REGISTER.

STEP 7. Adjust Center resistor on A17-C32. Set for +.9 vdc.

STEP 8. Set bit 4 in FUNCTION REG.

STEP 9. Adjust resistor closest to chassis front A17-C32. Set for +1.2 vdc.

STEP 10. Repeat steps 1 through 9 for each add on unit.

NOTE

Bias settings are good "ball park" values. The settings can be varied depending on whether the transport is dropping or picking up bits. The normal value has a range of .6 to 1.3 volts. The high bias should always be .3 to .4 higher than normal. The low bias adjustment can be used to "gang" adjust all biases.

(c) TRANSPORT 2 BIAS SUPPLY ADJUSTMENT.

STEP 1. Place negative meter lead in TB2-M4.

STEP 2. Place positive meter lead in TB2-I5.

STEP 3. Set bit 3 in FUNCTION REG.

STEP 4. Adjust resistor farthest from chassis front on A17-C17. Set for +.3 vdc.

STEP 5. Clear FUNCTION REG.

STEP 6. Adjust center resistor A17-C17. Set for +.9 vdc.

STEP 7. Set bit 1 in FUNCTION REG.

STEP 8. Adjust bottom resistor on A 7-C17. Set for +1.2 vdc.

STEP 9. Repeat steps 1 through 8 for each add on unit.

(3) READ AMPLIFIER CHECKS/ADJUSTMENTS. - Select desired transport (see paragraph 5-2c(1), steps 1 thru 10). Steps 1 thru 8 set up a write 1's pattern, low density and odd parity.

STEP 1. Set MODE switch to T2.

STEP 2. Master clear.

STEP 3. Depress HANDLER/WRITE ENABLE indicator - switch.

STEP 4. Insert write instruction (01000), odd parity, low density in F REGISTER.

STEP 5. Insert 1's pattern in C REGISTER in conformance with module specified in F REGISTER.

STEP 6. Depress START SEQ indicator - switch 3.

STEP 7. Depress and release LOW SPEED/STEP switch.

STEP 8. Check waveform at test point 1 of each read amplifier module (see figure 5-3) of selected tape transport. Observed signal should be 9 volts peak-to-peak. Read amplifier module locations are listed in table 5-6.

NOTE:

Experience in the field indicates that settings as low as 6.5 volts give fewer parity errors. 800 BPI will be about 1.5 volts lower than what is set at 200 BPI. Also check TP2 for proper output (this amplifier is push-pull). TP3 is ground.

STEP 9. If observed signal is not 9 volts peak-to-peak, adjust register on module until 9 volt peak-to-peak signal is observed.

STEP 10. Repeat steps 1 thru 9 for each additional tape transport.

(4) READ DETECTOR CHECKS/ADJUSTMENTS. - Perform read amplifier checks/ adjustments first. Select a transport and write all ones. See paragraph 5-2c(1) and (2). Perform the following steps while the unit is writing or reading this tape.

TABLE 5-6. DATA FOR READ AMPLIFIER AND READ DETECTOR CHECKS/ADJUSTMENTS

TRANSPORT NUMBER	READ AMPS		READ DETECTORS			
	TERM	LOCATION	TERM	LOCATION	TEST POINT	BIT
MTU CHASSIS A17						
1, 3, 5, or 7	60M10	J25D	61M10	J25C	TB1A8	0
	60M11	J26D	61M11	J26C	TB1B1	1
	60M12	J27D	61M12	J27C	TB1B2	2
	60M13	J28D	61M13	J28C	TB1B3	3
	60M14	J29D	61M14	J29C	TB1B4	4
	60M15	J30D	61M15	J30C	TB1B5	5
	60M16	J31D	61M16	J31C	TB1B6	6
2, 4, 6, or 8	60M60	J18D	61M60	J18C	TB2A8	0
	60M61	J19D	61M61	J19C	TB2B1	1
	60M62	J20D	61M62	J20C	TB2B2	2
	60M63	J21D	61M63	J21C	TB2B3	3
	60M64	J22D	61M64	J22C	TB2B4	4
	60M65	J23D	61M65	J23C	TB2B5	5
	60M66	J24D	61M66	J24C	TB2B6	6

NOTE

The final detector setting is just a few turns from the most counterclockwise stop. If in doubt, turn all pots counterclockwise before adjusting.

STEP 1. Using AC EXTERNAL, sync oscilloscope on read detector (A17-TBI or TB2) test point. See figure 5-3 for module test point location and refer to table 5-7 for read detector module location.

STEP 2. Read signal at read detector module test point 1.

STEP 3. Break in waveform (caused by sync) should coincide with zero crossover point of waveform.

STEP 4. If necessary, adjust resistor on detector module until it does coincide with zero crossover point of waveform.

TABLE 5-7. READ DETECTOR MODULE LOCATIONS

TT#1	BIT	TT#2
Look sync		Look sync
J25C--TB1-A8	0	J18C-TB2-A8
J26C--TB1-B1	1	J19C--TB2-B1
J27C--TB1-B2	2	J20C--TB2-B2
J28C--TB1-B3	3	J21C--TB2-B3
J29C-TB1-B4	4	J22C-TB2-B4
J30C-TB1-B5	5	J23C-TB2-B5
J31C-TB1-B6	6	J24C--TB2-B6

STEP 5. Perform steps 1 thru 3 above and if necessary, step 4, for each read detector module of selected transport.

STEP 6. Repeat for additional transport(s).

(5) READ DESKEWING CHECKS/ADJUSTMENTS. - Before performing the following steps, load a master alignment tape. IBM Part #432-641 (1200 ft.) or #432640 (600 ft.). Both are 800BPI.

CAUTION

Ensure that a write-enable ring is not positioned in the master tape reel.

STEP 1. Perform steps 1 thru 10 of paragraph 5-2c(1).

STEP 2. Insert read instruction (00000), odd parity and high density (800 bits-per-inch).

STEP 3. Sync oscilloscope on AC EXT at TB1B18 figure 8-34, Input to Bit 2^3 Read Compensation Delay on chassis A13A2.

STEP 4. Set sequence indicator 3, OP STEP.

STEP 5. Read signal in order listed on chassis A13A2 at test points shown in table 5-8 (sync remains at TB1B18). Viewed pulse should be delayed 4.5 microseconds from sync pulse.

STEP 6. If necessary, adjust resistor for channel under test (see figure 5-4) on module indicated in table 5-9 column 3, for transport under test.

STEP 7. Repeat read deskewing checks/adjustments for each tape transport.

(6) WRITE DESKEWING CHECKS/ADJUSTMENTS.

STEP 1. Load scratch tape; select transport.

STEP 2. Initiate single instruction, write all 1's operation with odd parity at 800 BPI.

STEP 3. Sync oscilloscope on AC EXT at test point 2G11 (figure 8-50, Encoder to write compensation delay) on chassis A13A2.

STEP 4. Read channel 3 signal at test point 1G12 (figure 8-50, output of 2^3 write compensation delay) on chassis A13A2. Observed waveform should be 4.5 microseconds from sync.

STEP 5. If necessary, adjust channel 3 resistor (see figure 5-4 on module listed in column 4 of table 5-9 for transport being tested.

STEP 6. Sync oscilloscope on AC EXT at test point 1B18 (figure 8-34, input to Bit 2^3 read compensation delay) A13A2.

STEP 7. Using oscilloscope on channel A, observe waveform at channel 3 test point (refer to table 5-8).

NOTE

The observed signal may appear earlier than the 4.5 microseconds for which it was set, but do not readjust for channel 3.

STEP 8. Using dual trace (channel B) observe waveforms for other channels using test points in table 5-8. Channel B waveform should coincide with channel A waveform.

STEP 9. If necessary, adjust resistor for channel concerned (see figure 5-4 on write deskewing module for transport concerned (refer to table 5-9 column 4) until channel B waveform coincides with channel A waveform.

STEP 10. Repeat procedure for each transport.

TABLE 5-8. TEST POINTS FOR DESKEWING CHECKS/ADJUSTMENTS

CHANNEL	CHASSIS 13A2	FIG.#	READ SIGNAL AT
3		8-34	TB1E3
0		8-34	TB1A4
1		8-34	TB1G3
2		8-34	TB1F3
4		8-35	TB1D3
5		8-35	TB1C3
6		8-35	TB1B3

(7) READ REVERSE DESKEWING CHECKS/ADJUSTMENTS.

STEP 1. Write all 1's tape with parity at 800BPI.

STEP 2. Initiate backread with odd parity at 800BPI.

STEP 3. Sync oscilloscope on AC EXT at TB1B18 (figure 8-34, input to bit 2^3 read compensation delay) on chassis A13A2.

STEP 4. Read signal, in turn, at test points (on chassis A13A2) listed in table 5-8. Delay should be 4.5 microseconds from sync pulse.

STEP 5. If necessary, adjust resistor for channel under test (see figure 5-4) on module indicated in table 5-9, column 5 for transport under test.

STEP 6. Repeat read reverse deskewing checks/adjustments for other tape transports.

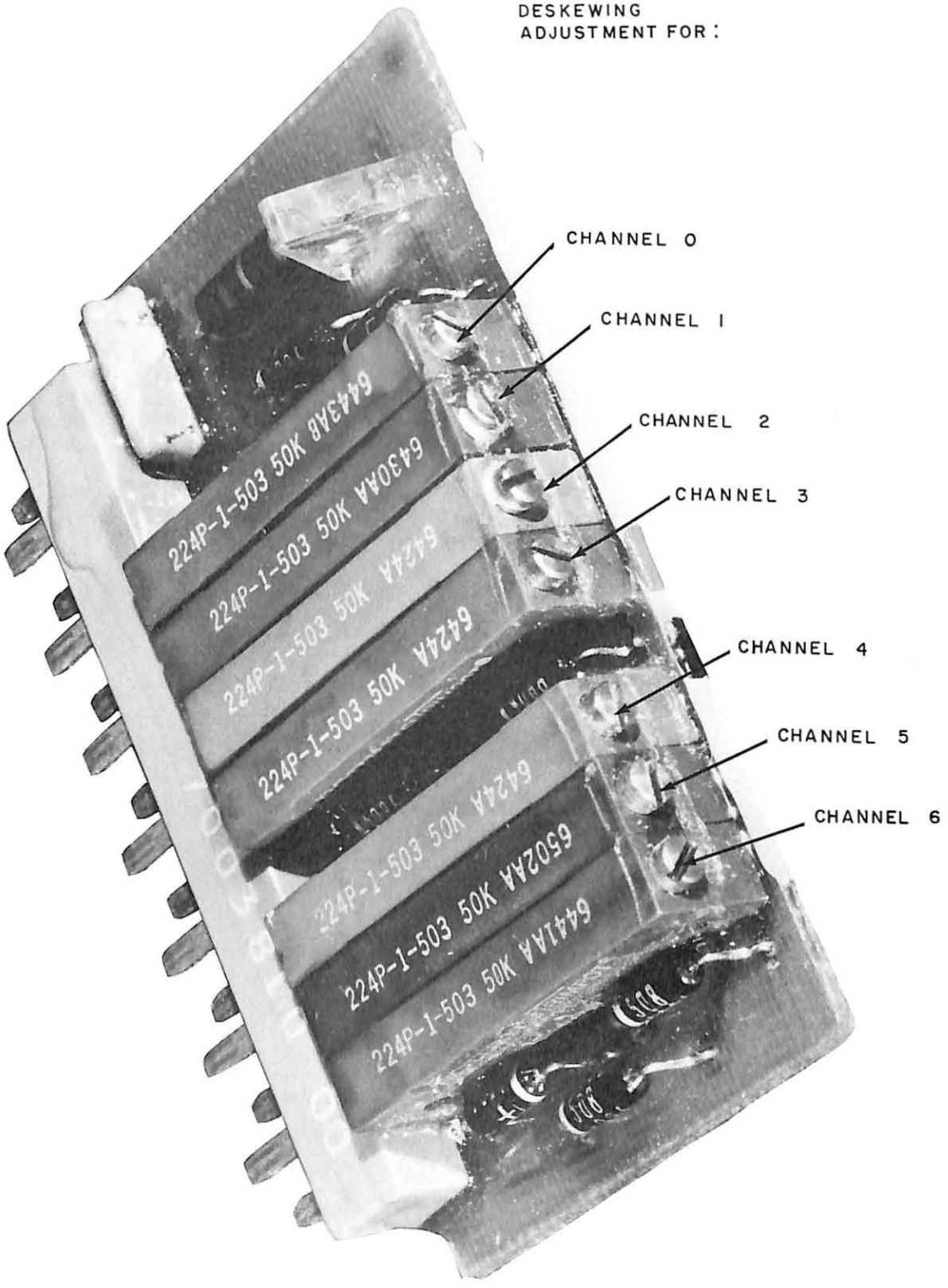


Figure 5-4. Channel Designations for Deskewing Adjustments

TABLE 5-9. LOCATION OF DESKEWING ADJUSTMENTS

HANDLER NUMBER	CHASSIS	READ ADJUST MODULE	WRITE ADJUST MODULE	READ REV. ADJUST MODULE
MTU FIGURES 8-65 THROUGH 8-67				
1	A13A2	J35A	J34A	J33A
2		J35C	J34C	J33C
3		J35B	J34B	J33B
4		J35D	J34D	J33D
5		J35E	J34E	J33E
6		J35G	J34G	J33G
7		J35F	J34F	J33F
8	A13A1	J35G	J34G	J33G

(8) ERASE HEAD POLARITY CHECK. - The erase head polarity check should be made immediately following an erase head replacement operation. Begin the erase head polarity check with the tape positioned at the load point.

STEP 1. Select transport. See paragraph 5-3g(1).

STEP 2. Select 800 BPI.

STEP 3. Set FUNCTION REG. to write 1 MOD. 3, odd parity. (01000000100).

STEP 4. Set all bits of C REGISTER.

STEP 5. Write continuous 1's for about 30 seconds. See paragraph 5-3g(2). To terminate write operation set bit 26 in WRITE CONT.

STEP 6. Rewind tape.

STEP 7. Select 800 BPI.

STEP 8. Set FUNCTION REG to write all 0's (01000000000).

STEP 9. Clear C REGISTER.

STEP 10. Perform repeat/write operation according to paragraph 5-3g(2).

STEP 11. Repeat the following.

1) Write blocks of 0's for about 30 seconds with the LOW SPEED ADJ at about mid range.

2) Press LOW SPEED/STEP switch. If write function does not terminate, set bit 26 in WRITE CONT.

STEP 12. Master Clear.

STEP 13. Set bit 15 in FUNCTION REG.

STEP 14. Press LOW SPEED/STEP switch. This should initiate read reverse function and tape should move back to load point without reading data. Observe by noting that LONG COUNT register and N1, N2, and N3 are clear. If data is read this indicates that either the erase head is bad, the erase head polarity is reversed, or LOGIC enabling the erase head is defective.

(9) OVERTEMP SENSOR CHECKS. - To check the overtemp sensors in a cabinet, remove the blower fuses for that cabinet and hold an ordinary 100-watt light bulb against the sensors. When the sensors have warmed to 46°C (115°F) the overtemp warning should be heard. Some time later when the sensors have warmed to 60°C (140°F) all power should shut down except the blower power in the adjacent cabinet(s).

(10) ELAPSE TIME INDICATOR CHECKS/ADJUSTMENTS. - The elapse time indicators (M1/M2) are located in logic chassis A17 and may be checked and adjusted in the following manner:

STEP 1. Using procedure in paragraph 5-4c(2), extend A17 chassis. Keep accurate records of readings of elapse time indicators.

NOTE

It is not necessary to remove PC card containing meters M1/M2 from chassis to obtain elapse time readings.

STEP 2. To remove meters M1/M2 for resetting, use procedures outlined in paragraph 5-4c(15).

CAUTION

The elapse time indicators are susceptible to handling shocks, such as dropping on a desk or workbench. These shocks can easily exceed 200-300g, and a careful visual check of gap appearance should be made after accidental dropping.

STEP 3. To calibrate indicators, use a +4.5 vdc source, adjust the current for each indicator to 20.8 millamperes via the respective trimpots (R3/R4) (see figure 8-94A).

STEP 4. The elapse time indicators are considered throw-away items. When the indicator reaches maximum time, remove and replace with a spare unit.

5-3. TROUBLESHOOTING.

Troubleshooting the system is primarily a logical analysis of symptoms peculiar to the malfunction. The printed-circuit module concept simplifies the task of troubleshooting because module replacement eliminates the need for component malfunction

isolation. No circuit module repair procedures are included in this manual; defective modules are replaced. If, when troubleshooting, a malfunction of the Potter tape transport is discovered, consult the Potter tape handler manual.

a. TEST EQUIPMENT AND SPECIAL TOOLS. - Tables 1-3, 1-4, and 5-10 list the test equipment and special tools required for troubleshooting the MTU. In addition, a small screwdriver with a 4-inch shank and 1/8-inch blade is useful.

b. INITIAL INSPECTION. - Following the detection of a malfunction, make a visual inspection of the panel indicators, switches, and fuses. If this inspection reveals a trouble area, a logical process of elimination will, in many instances, reveal the source of the trouble. Since this logical approach varies with the individual maintenance technician, no definite rules are included in this text.

c. TEST POINTS. - All test points are shown on the functional schematic diagrams in section 8 of this manual. The test block and the test point coordinates within the test block are also shown.

d. TYPICAL TROUBLES CHART. - Table 5-11 lists the typical troubles which may be encountered and includes the symptom, probable cause, and remedial action for each.

e. COMPONENT LOCATIONS. - Figures 5-5 through 5-19 show the location of the MTU's major components, assemblies, and subassemblies; and their reference designation prefixes.

f. MALFUNCTION ISOLATION. - After a malfunction has been localized to a specific section or assembly, through a logical analysis in conjunction with the panel indications, the problem may be isolated to a particular circuit by checking the suspected circuits at the test points. Troubleshooting the logic circuits merely by voltage and resistance measurements is impractical. When a circuit failure is indicated, the printed circuit card containing the circuit should be replaced.
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Point-to-point wiring may be checked by use of the information presented in the functional schematics in section 8. The distribution of dc operating voltages is primarily by way of bus bars. These are shown on the chassis power distribution diagrams, figures 8-110 through 8-117.

TABLE 5-10. TROUBLESHOOTING TEST EQUIPMENT AND SPECIAL TOOLS

ITEM	NAME	VENDOR AND PART NO.	UNIVAC EQUIVALENT
1	Oscilloscope	Tektronix 545B	
2	Dual Trace Pre-Amplifier	Tektronix CA	
3	Voltohmmeter	Triplett 630A	
4	Crimping Tool - Single 24-26 ga	Berg HT-14	
5	Crimping Tool - Single 22 ga double 24 ga	AMP No. 47042	

2) Press LOW SPEED/STEP switch. If write function does not terminate, set bit 26 in WRITE CONT.

STEP 12. Master Clear.

STEP 13. Set bit 15 in FUNCTION REG.

STEP 14. Press LOW SPEED/STEP switch. This should initiate read reverse function and tape should move back to load point without reading data. Observe by noting that LONG COUNT register and N1, N2, and N3 are clear. If data is read this indicates that either the erase head is bad, the erase head polarity is reversed, or LOGIC enabling the erase head is defective.

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3	Voltohmmeter	Triplett 630A	
4	Crimping Tool - Single 24-26 ga	Berg HT-14	
5	Crimping Tool - Single 22 ga double 24 ga	AMP No. 47042	
6	Crimping Tool - Single 18-22 ga double 20-22 ga	AMP No. 47043	8839-109
7	Crimping Tool - Single 16 ga double 18 ga	AMP No. 47044	
8	Insertion Tool	AMP No. 380306-2	8839-213
9	Insertion Tool	AMP No. 380310-3	8839-212
10	Insertion Tip	AMP No. 395042	
11	Insertion Tip	Berg No. 34965	
	The following bits and sleeves are used with item 11.		
	22 ga. Bit (Std) Sleeve	Gardner-Denver Co., No. 26699 18640	8130-145 8130-146
	24 ga. Bit (Std) 24/30 ga. Sleeve	26589 17611-2	8130-120 8130-129
	24 ga. Bit (**) Sleeve	26263 18840	8130-121 8130-128
	24 ga. Bit (Std) Sleeve	A17612-2 17611-2	8130-123 8130-129

TABLE 5-10. TROUBLESHOOTING TEST EQUIPMENT AND SPECIAL TOOLS (CONTINUED)

ITEM	NAME	VENDOR AND PART NO.	UNIVAC EQUIPMENT
6	Crimping Tool - Single 18-22 ga double 20-22 ga	AMP No. 47043	8839-109
7	Crimping Tool - Single 16 ga double 18 ga	AMP No. 47044	
8	Insertion Tool	AMP No. 380306-2	8839-213
9	Insertion Tool	AMP No. 380310-3	8839-212
10	Insertion Tip	AMP No. 395042	
11	Insertion Tip	Berg No. 34965	
	The following bits and sleeves are used with item 11.		
		Gardner-Denver Co.,	
	22 ga. Bit (Std)	26699 No.	8130-145
	Sleeve	18640	8130-146
	24 ga. Bit (Std)	26589	8130-120
	24/30 ga. Sleeve	17611-2	8130-129
	24 ga. Bit (**)	26263	8130-121
	Sleeve	18840	8130-128
	24 ga. Bit (Std)	A17612-2	8130-123
	Sleeve	17611-2	8130-129
	28 ga. Bit	507387	8130-154
	Sleeve	502129	8130-156
	28 ga. Bit (**)	501389	8130-155
	Sleeve	502129	8130-156
	30 ga. Bit (Std)	504221	8130-141
	Sleeve	500350	8130-142
	30 ga. Bit (**)	501381	8130-143
	Sleeve	17611-2	8130-129

TABLE 5-10. TROUBLESHOOTING TEST EQUIPMENT AND SPECIAL TOOLS (CONTINUED)

ITEM	NAME	VENDOR AND PART NO.	UNIVAC EQUIPMENT
	20 ga. -26 ga. (Inclusive)	500130	8130-138
	30 ga.	505244	8130-137
12	Wire Wrap Gun	Gardner-Denver No. 14R2	8130-132
13	Unwrap Tool, 30 ga	No. 505244	8130-137
14	Unwrap Tool, 20 ga. - 26 ga. (Inclusive)	No. 500130	8130-138

** Modified (will wrap 1-1/4 more times than standard).

g. MANUAL OPERATION/TEST PROCEDURES. - There are many manual procedures which may be developed through usage and experience with the MTU. The following paragraphs give step-by-step procedures for using the basic manual operations. These basic operations may be modified by varying the CLOCK CONTROL switch settings and using the LOW SPEED/STEP switch. For the following procedures, it is assumed that the tape is properly loaded and power turn-on has been accomplished.

(1) TRANSPORT SELECTION. - To select the desired tape transport, refer to paragraph 5-2c(1).

(2) SINGLE INSTRUCTION OPERATION. - To perform a single instruction operation, proceed as follows (ensure that the desired handler is selected, refer to paragraph 5-4a).

CAUTION

Do not turn MAN-OFF-AUTO switches on tape handlers 1 and 2 to MAN/AUTO positions simultaneously. The current surge of both vacuum motors will cause circuit breaker (A3A3/CB1) to trip. Allow handler motor 1 to come to full speed (approximately 5 seconds) prior to turning handler 2 switch to MAN/AUTO.

STEP 1. Set HANDLER MAN/OFF/AUTO switch of selected handler to AUTO.

STEP 2. Set MODE switch to T2.

STEP 3. Set CLOCK CONTROL switch to OP STEP.

TABLE 5-10. TROUBLESHOOTING TEST EQUIPMENT AND SPECIAL TOOLS (CONTINUED)

	28 ga. Bit Sleeve	507387 502129	8130-154 8130-156
	28 ga. Bit (**) Sleeve	501389 502129	8130-155 8130-156
	30 ga. Bit (Std) Sleeve	504221 500350	8130-141 8130-142
	30 ga. Bit (**) Sleeve	501381 17611-2	8130-143 8130-129
	20 ga.-26 ga. (Inclusive)	500130	8130-138
	30 ga.	505244	8130-137
12	Wire Wrap Gun	Gardner-Denver No. 14R2	8130-132
13	Unwrap Tool, 30 ga	No. 505244	8130-137
14	Unwrap Tool, 20 ga. - 26 ga. (Inclusive)	No. 500130	8130-138

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(1) TRANSPORT SELECTION. - To select the desired tape transport, refer to paragraph 5-2c(1).

(2) SINGLE INSTRUCTION OPERATION. - To perform a single instruction operation, proceed as follows (ensure that the desired handler is selected, refer to paragraph 5-4a).

STEP 1. Set HANDLER MAN/OFF/AUTO switch of selected handler to AUTO.

STEP 2. Set MODE switch to T2.

STEP 3. Set CLOCK CONTROL switch to OP STEP.

TABLE 5-11. TYPICAL TROUBLES CHART (CONT.)

SYMPTOM	PROBABLE CAUSE	REMEDIAL ACTION
Improper frame count.	Improper start-stop time adjustment.	Perform handler start-stop check adjustments (refer to paragraphs 5-2c(1).
Reads incorrectly at high density, but reads properly at low density.	Improper deskewing adjustments. See paragraphs 5-2d (5), 5-2d(7).	Perform deskewing checks/ adjustments.
Dropping and/or picking up bits in the C register.	Defective input amplifiers.	Check input amplifiers.
	Defective C register circuits.	Check C register circuits.
	Defective A register circuits.	Check A register circuits.
Master clock does not run.	One phase is missing or grounded.	Check for defective phase driver module. Check for missing phase grounded in another module.
	Phase enable missing or grounded.	Check for defective phase enable module. Check for missing phase enable grounded in another module.
Incorrect results for a search function.	Defective A register compare circuits.	Check compare circuits.
HANDLER READY indicator does not light (tape properly loaded and equipment power OK).	Defective EOT or load point sensor lamp.	Replace defective sensor lamp.
Write enable will not set.	Defective HANDLER WRITE ENABLE switch.	Check HANDLER WRITE ENABLE switch.
	Write enable ring missing from tape reel.	Insert write enable ring in reel.
Fails to detect load point and/or EOT.	EOT and/or load point markers on tape are worn and dull or missing.	Replace markers on tape.
Tape will not move from load point. HANDLER EOT indicator lighted.	Handler power off and logic power on.	Shut logic power off momentarily.

TABLE 5-11. TYPICAL TROUBLES CHART (CONT.)

SYMPTOM	PROBABLE CAUSE	REMEDIAL ACTION
	EOT does not clear.	Check adjustment of EOT amplifier.
Does not rewind at high speed.	Defective speed change relay in the tape handler.	Refer to table 6-1 in Potter tape handler manual.
Does not reduce speed during rewind	Defective low tape sensor or microswitch.	Replace sensor or adjust microswitch.
Excessive tension arm swing and reel has more than 90^{0} of play when stopped.	Servo amplifier gain too low.	Adjust servo amplifier gain control on module.
Tension arms are normal as tape runs in one direction, but swing far from normal when tape runs in opposite direction.	Defective servo amplifier.	Check servo amplifier.
	Servo amplifier gain too low.	Adjust amplifier gain.
	Power supply voltages too low.	Check power supply voltages (refer to table in Potter tape handler manual.
Tension arm swings so far that it stops tape movement when speed changes from high to low during rewind.	Servo amplifier gain low.	Adjust servo amplifier gain.
Reels jitter when stopped.		Check servo loop by turning reel manually with handler on. If opposite torque is:
	Defective tension arm potentiometer.	jerky and grabby, check tension arm potentiometer.
	Defective servo amplifier.	steady, check servo amplifier.
	Improperly adjusted or defective servo amplifier.	weak, check servo amplifier.
	Also refer to handler manual.	refer to handler manual.

STEP 4. Master clear.

STEP 5. Depress HANDLER WRITE ENABLE indicator-switch if write instruction is to be performed.

STEP 6. Manually insert instruction in F REGISTER.

STEP 7. If instruction to be used is write, manually insert data pattern to be recorded in C REGISTER in conformance with moduli specified in F REGISTER.

STEP 8. Depress START SEQ indicator-switch 3.

STEP 9. Depress and release LOW/SPEED switch.

STEP 10. If instruction is write, terminate record when desired by depressing WRITE CONT indicator-switch 26 (ODR). Other instructions are self-terminating.

(3) REPEAT. - In the repeat operation, a manually set-up function may be performed repetitiously. The following procedure describes a repeat-write operation. Ensure that the desired tape handler is selected. See paragraph 5-2c(1).

STEP 1. Set HANDLER MAN/OFF/AUTO switch to AUTO.

STEP 2. Set MODE switch to T3.

STEP 3. Set CLOCK CONTROL switch to OP STEP.

STEP 4. Master clear.

STEP 5. Manually insert instruction in F REGISTER.

STEP 6. Manually insert pattern to be recorded in C REGISTER.

STEP 7. Depress START SEQ indicator-switch 3.

NOTE

The LOW SPEED/STEP switch may be placed in the LOW SPEED position and the MTU automatically writes consecutive records until the switch is returned to the center position.

STEP 8. Depress LOW SPEED/STEP switch.

STEP 9. Release LOW SPEED/STEP switch. Tape transport should start, record one record, and stop with START SEQ indicator-switch 3 lighted. Length of record is dependent on setting of LOW SPEED ADJ potentiometer and may be varied from record to record.

STEP 10. To write more records, repeat steps 8 and 9.

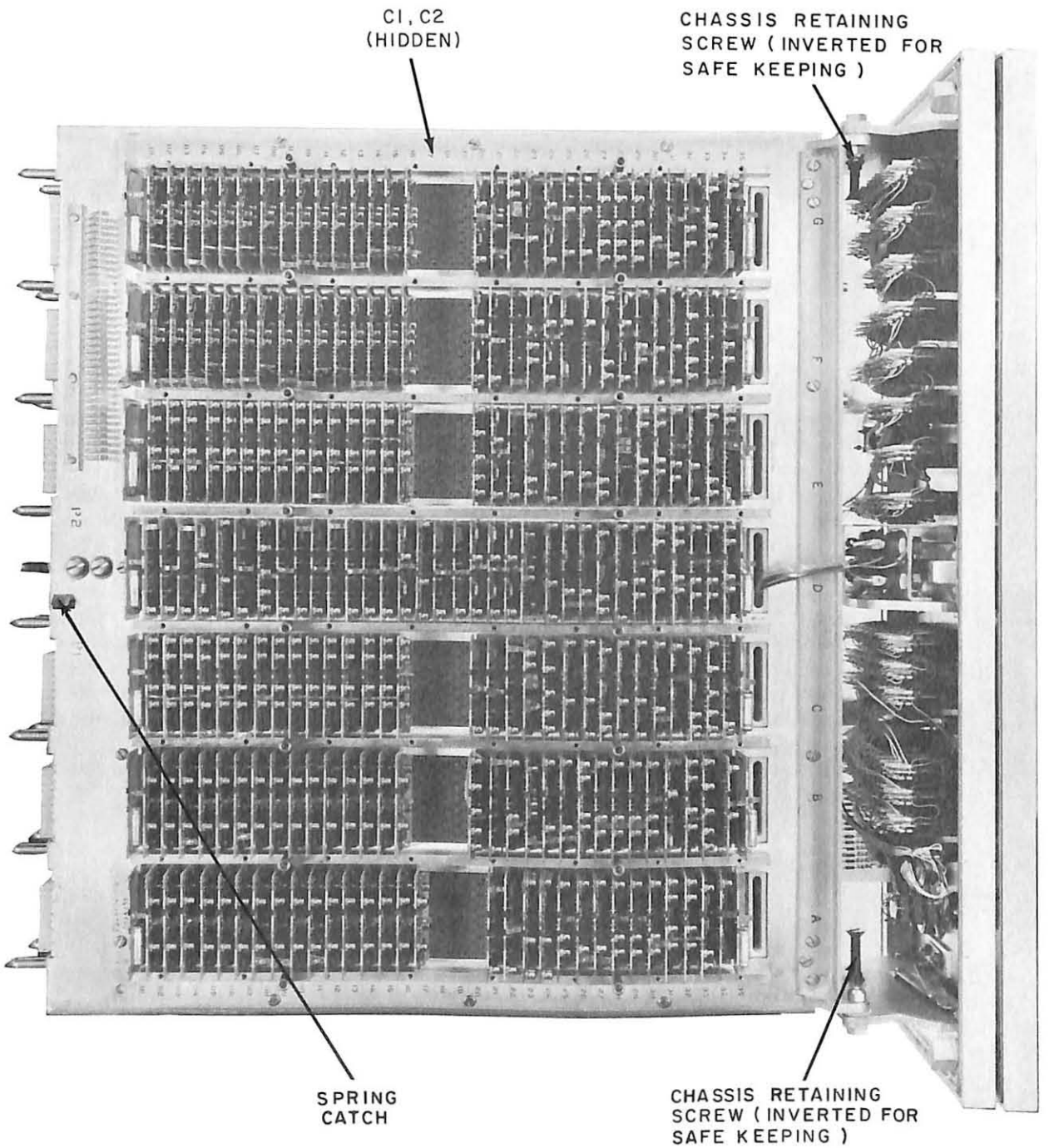


Figure 5-5. Logic Chassis A12A1

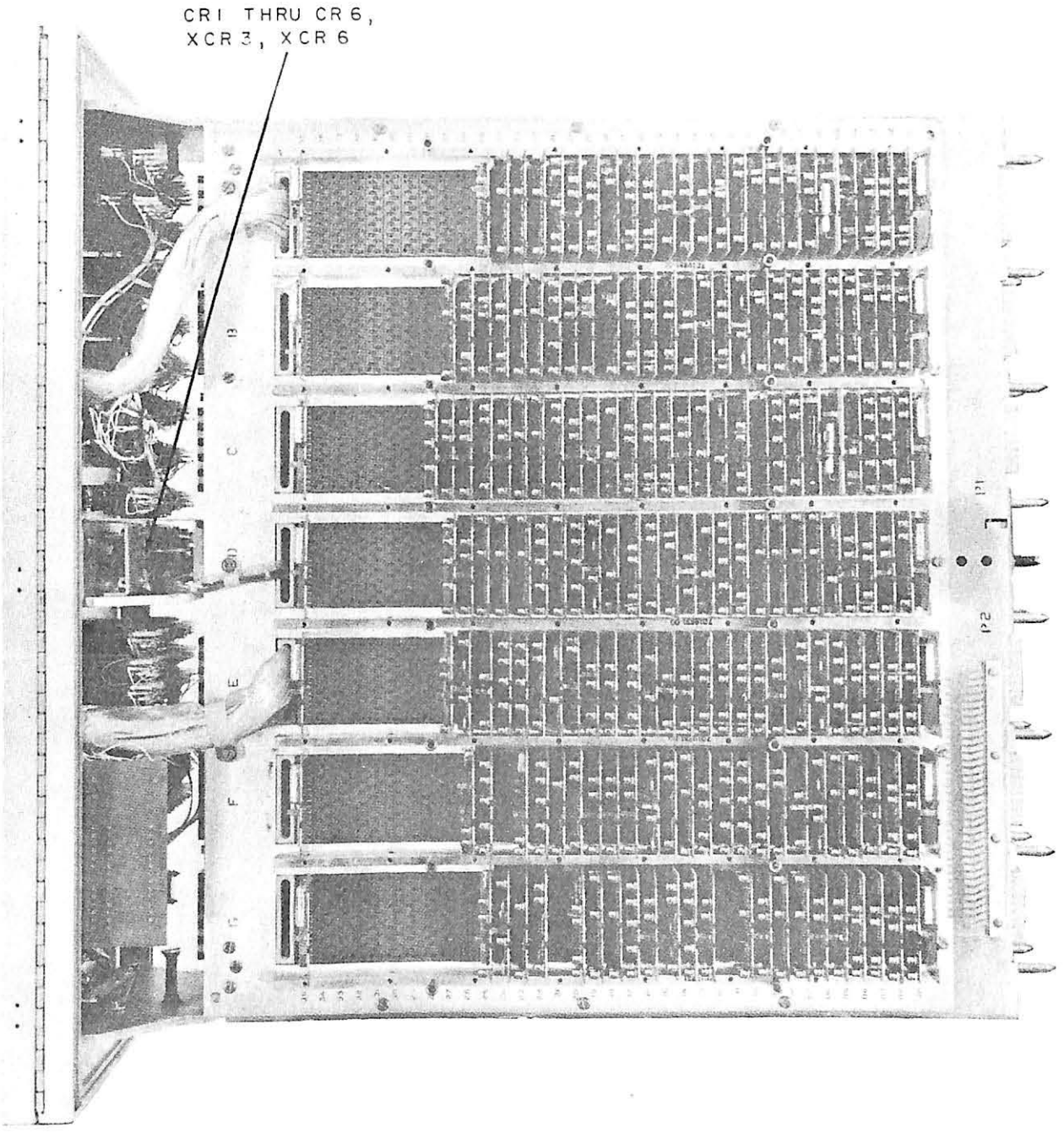


Figure 5-6. Logic Chassis A12A2

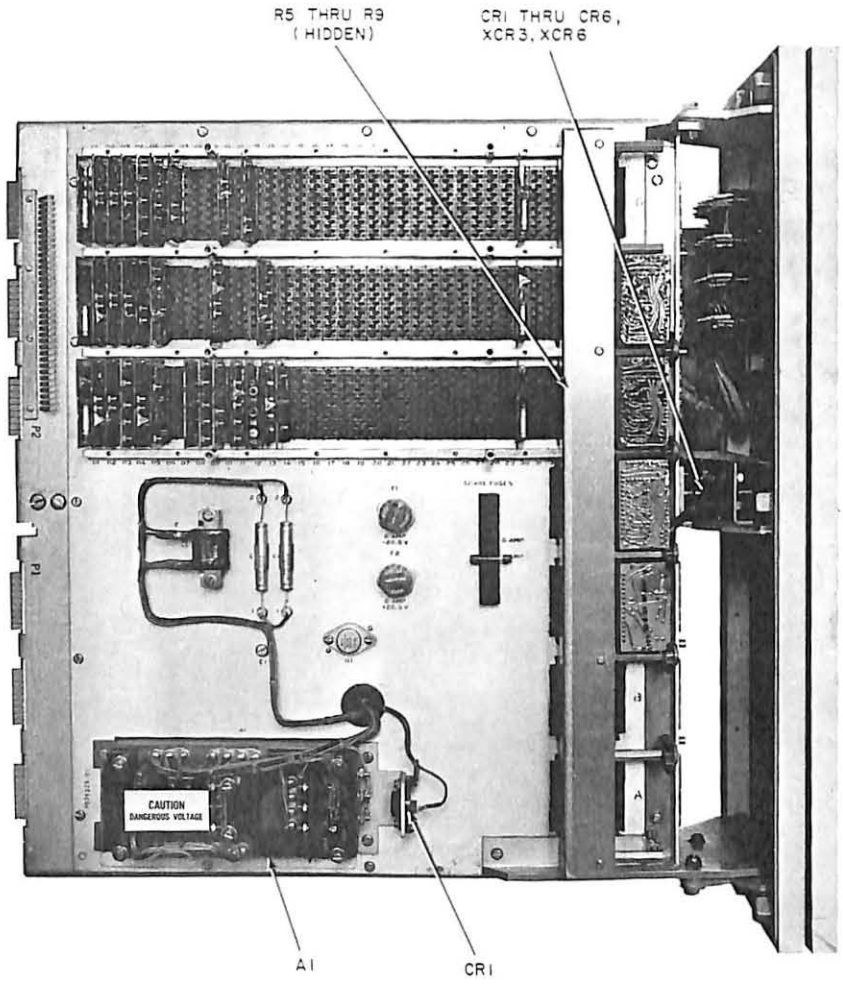


Figure 5-7. Logic Chassis A13A1

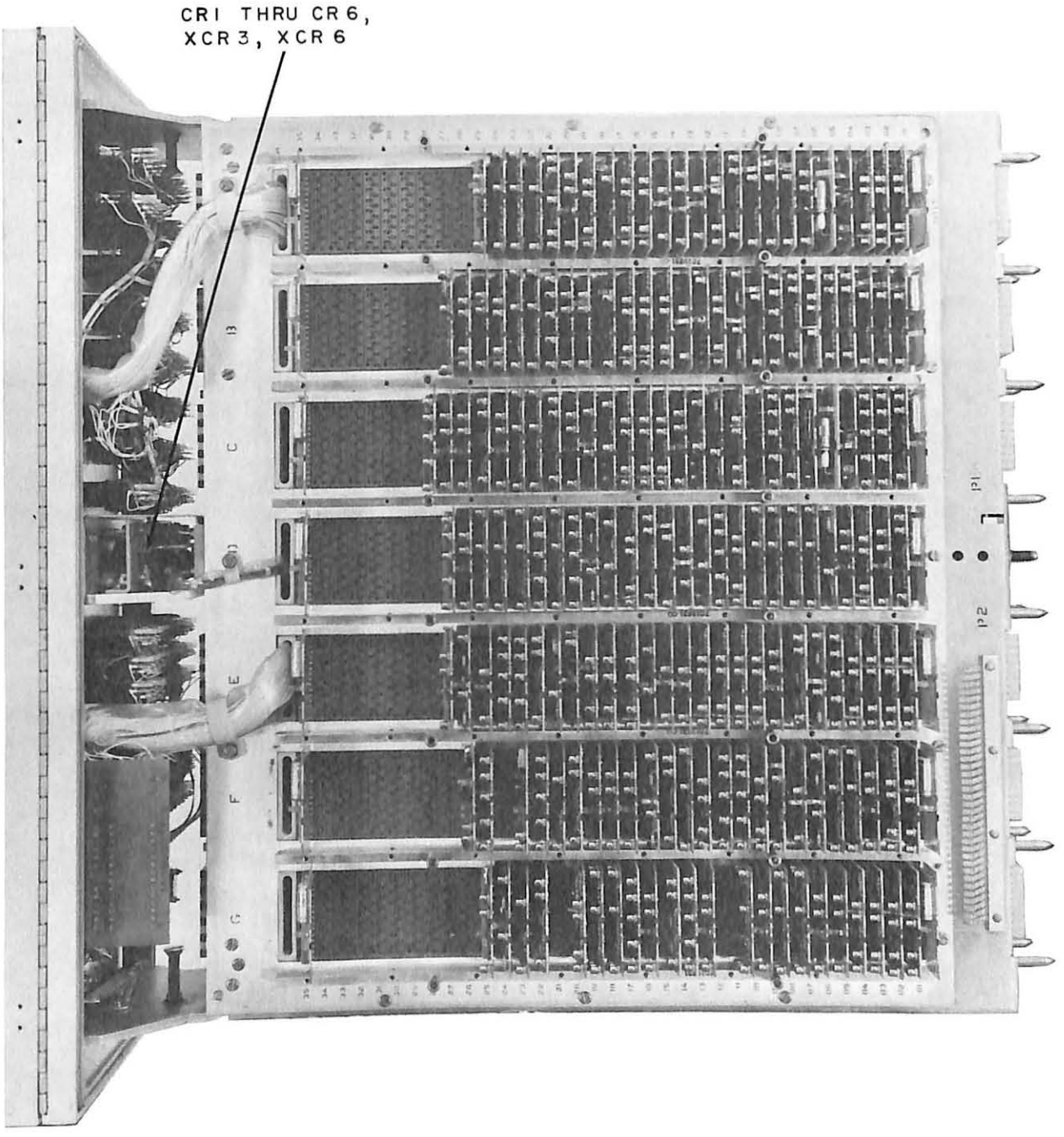


Figure 5-6. Logic Chassis A12A2

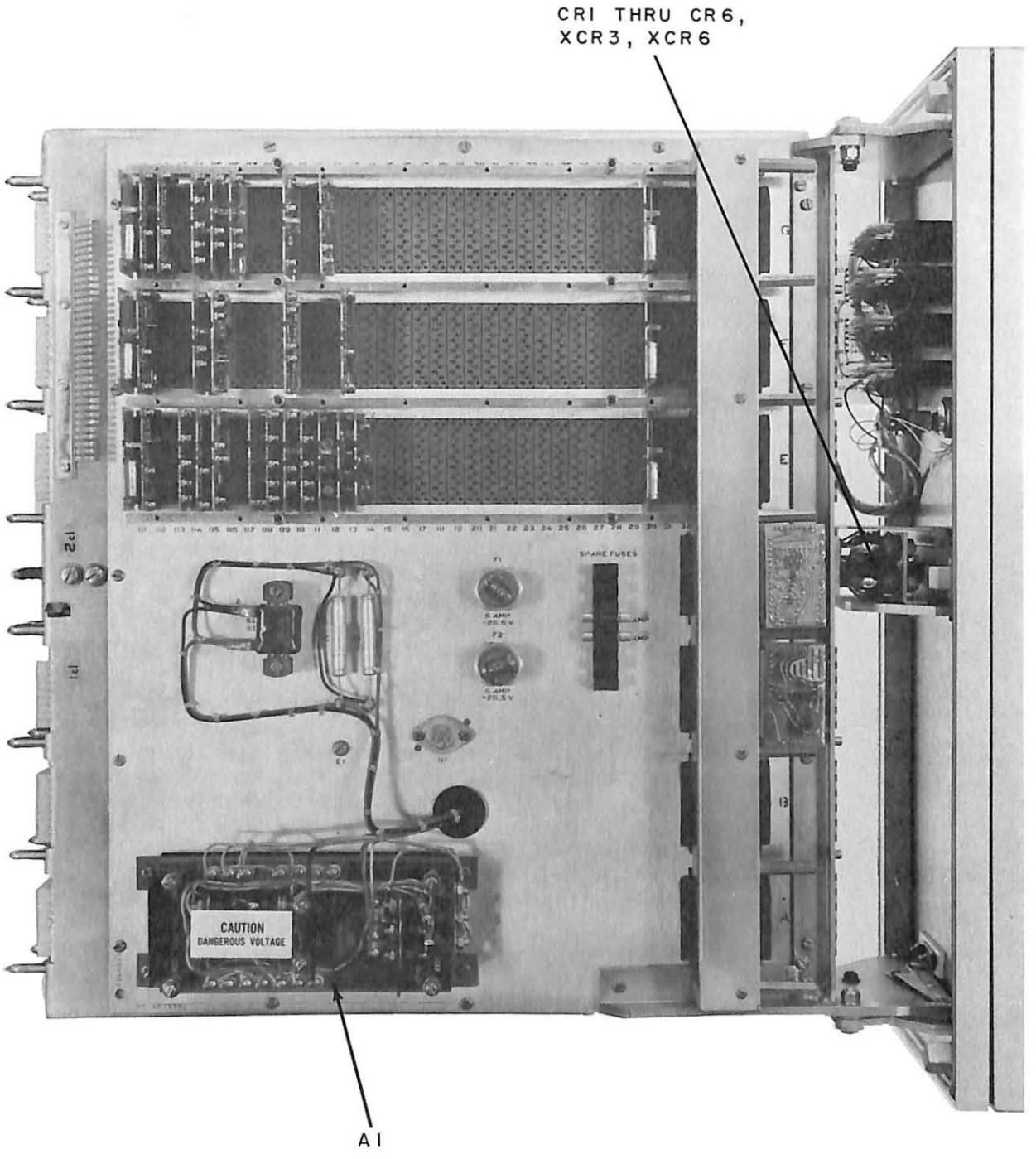


Figure 5-7. Logic Chassis A13A1

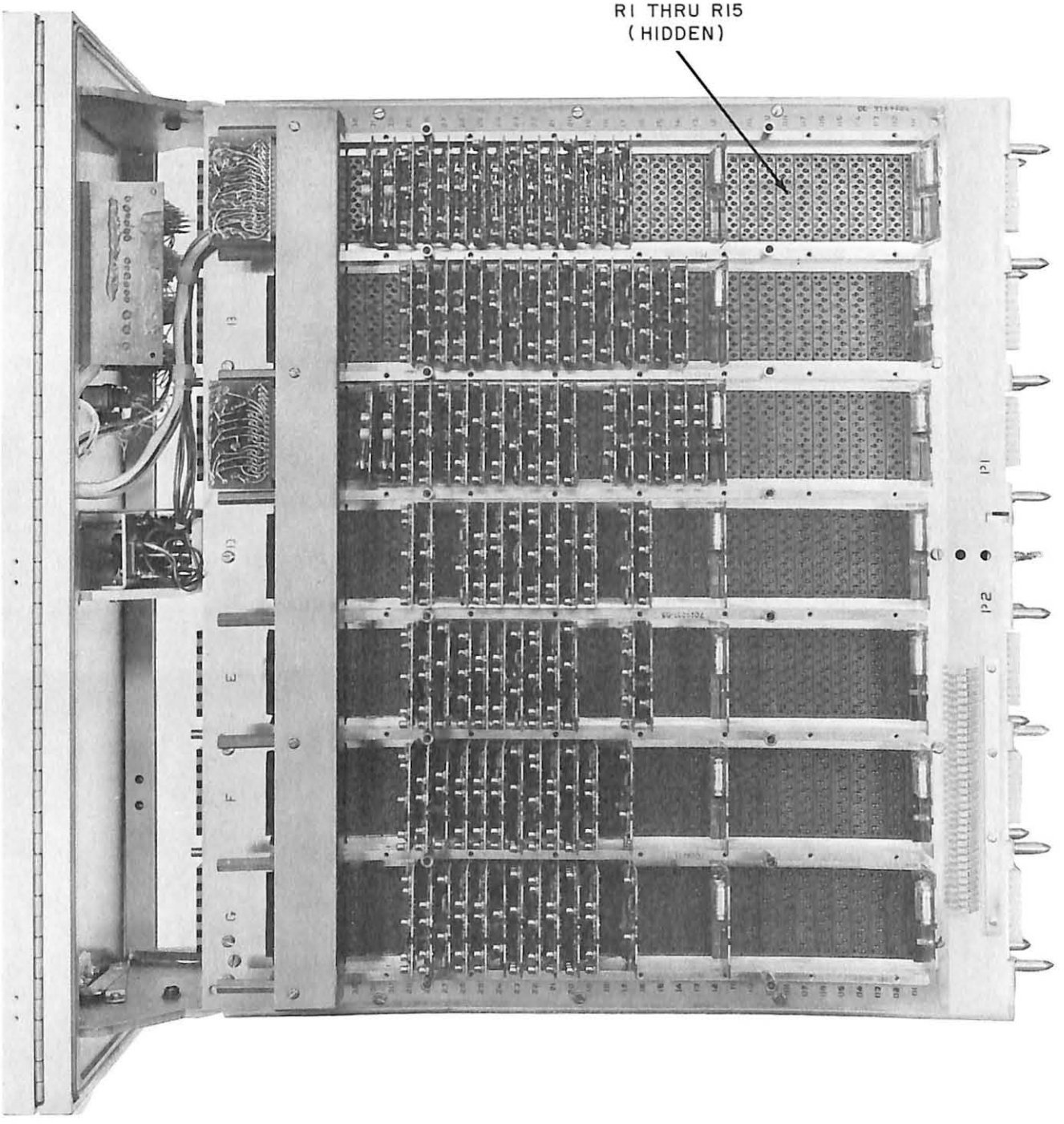


Figure 5-8. Chassis A13A2

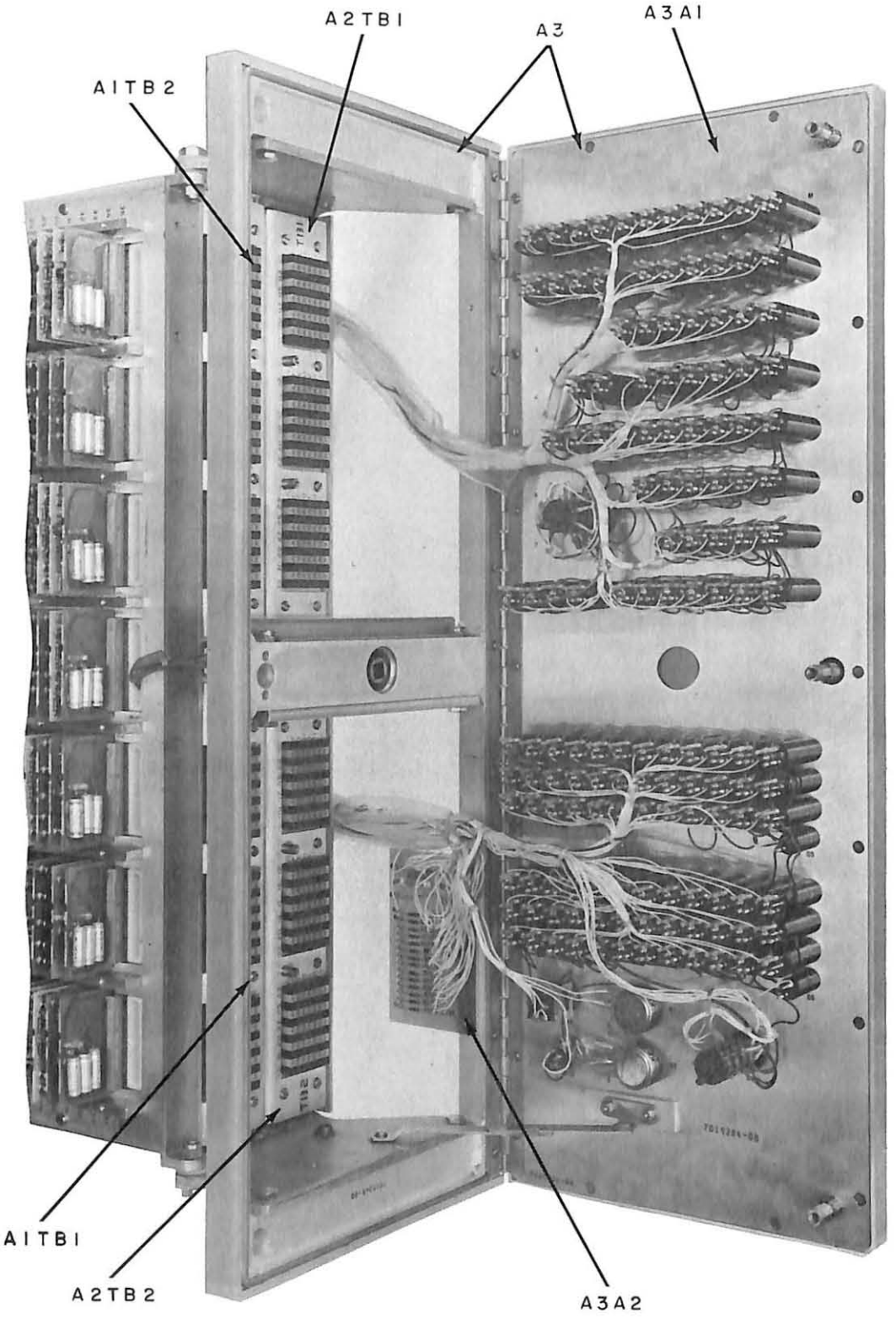


Figure 5-9. Drawer Assembly A12, Front End, Panel Open

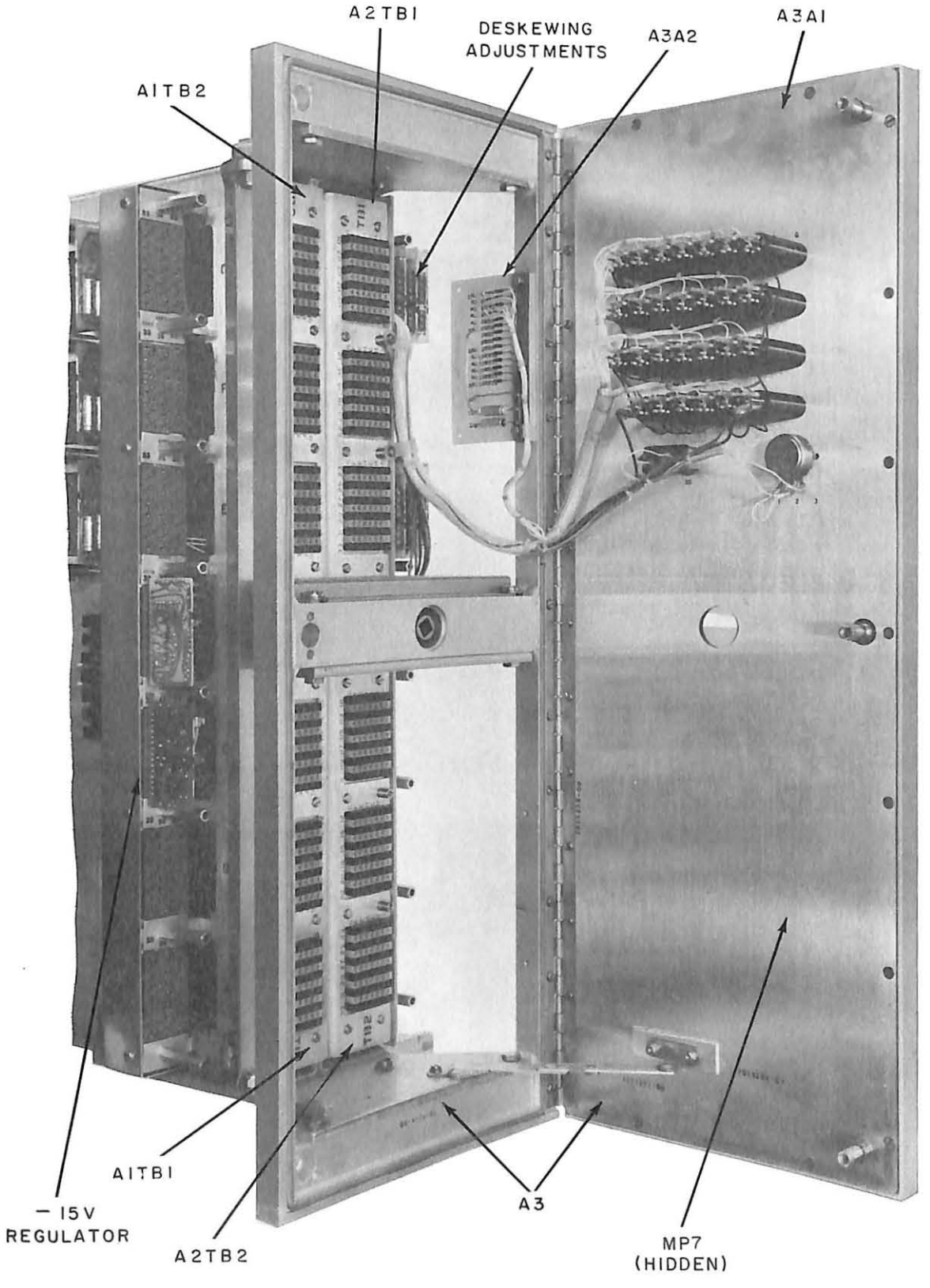


Figure 5-10. Drawer Assembly A13, Front End, Panel Open

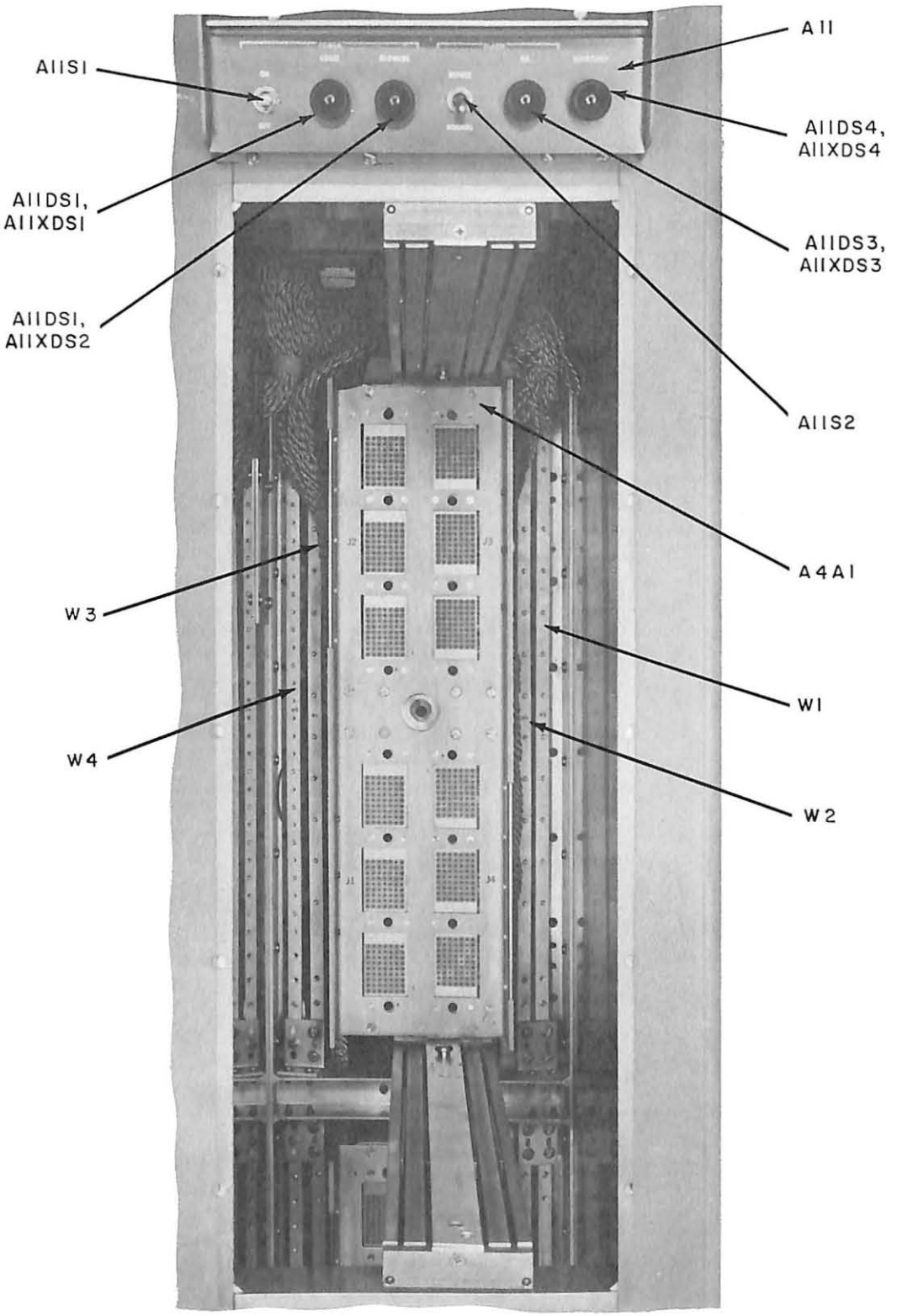


Figure 5-11. Magnetic Tape Control Cabinet, Interior View, Upper Half

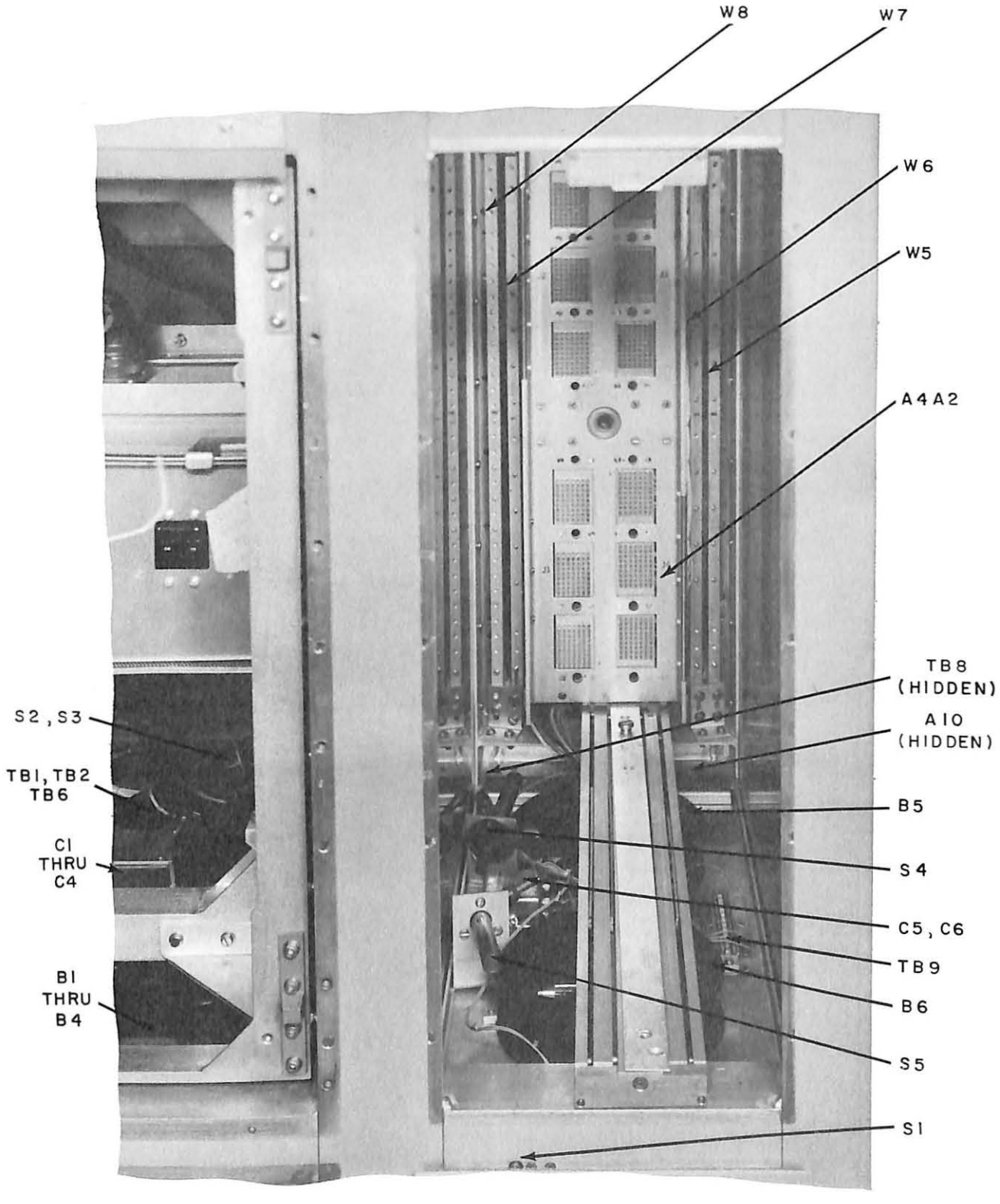


Figure 5-12. Magnetic Tape Control Cabinet, Interior View, Lower Half, Air Cooled

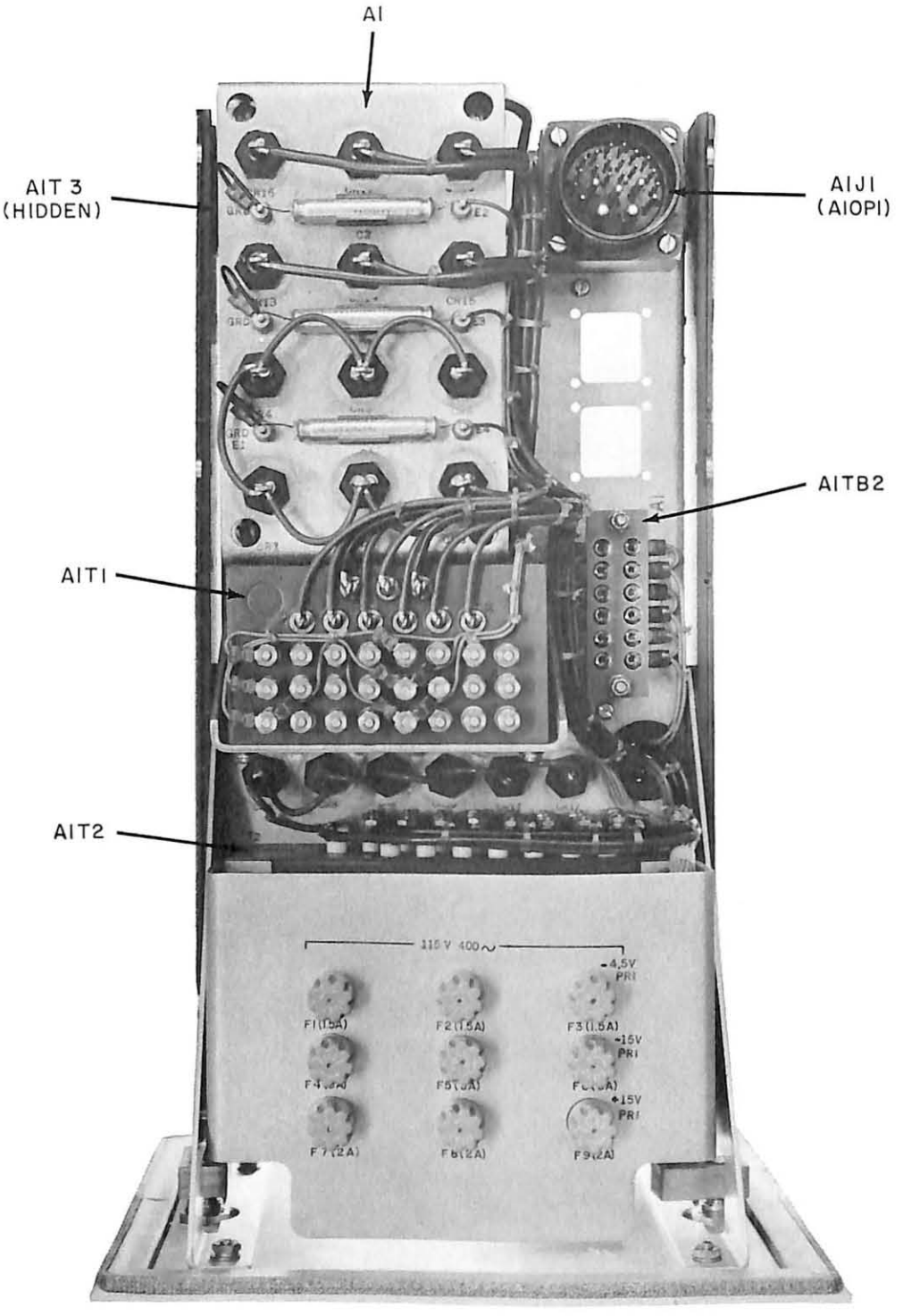


Figure 5-13. Logic Power Supply Drawer Assembly PS1, Top View

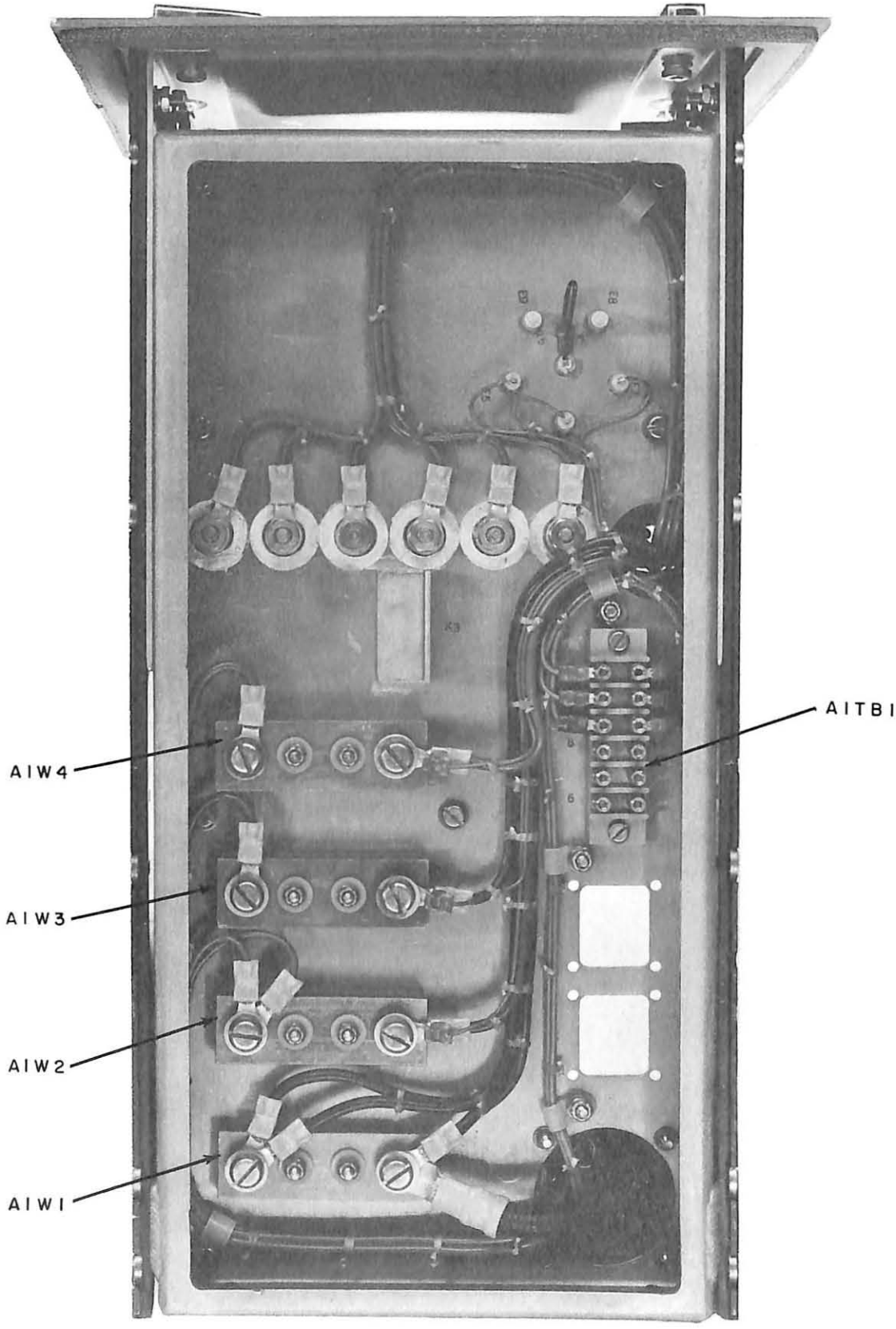


Figure 5-14. Logic Power Supply Drawer Assembly PS1, Bottom View

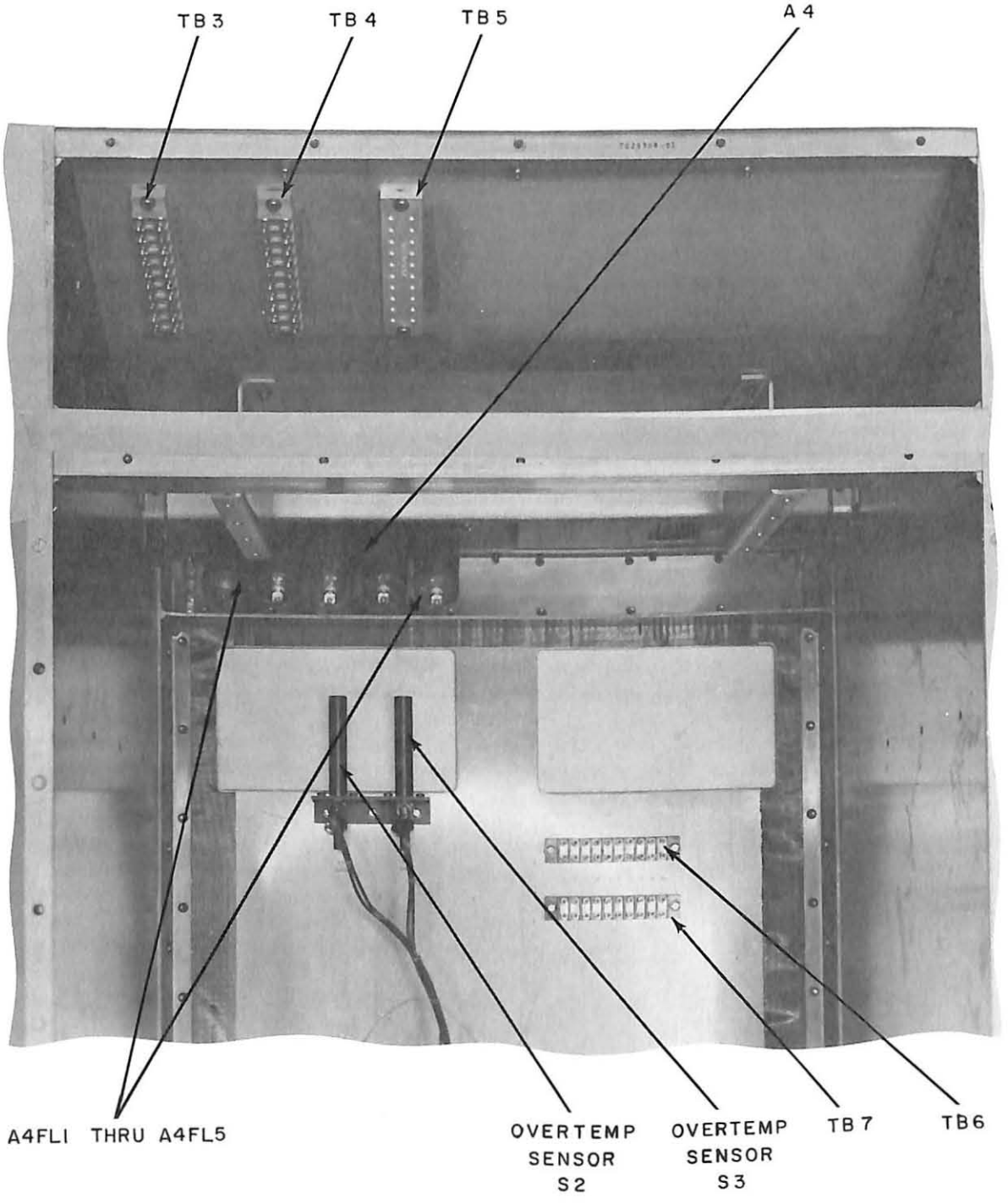


Figure 5-15. Tape Transport Cabinet, Partially Assembled
View of Upper Half, Water Cooled

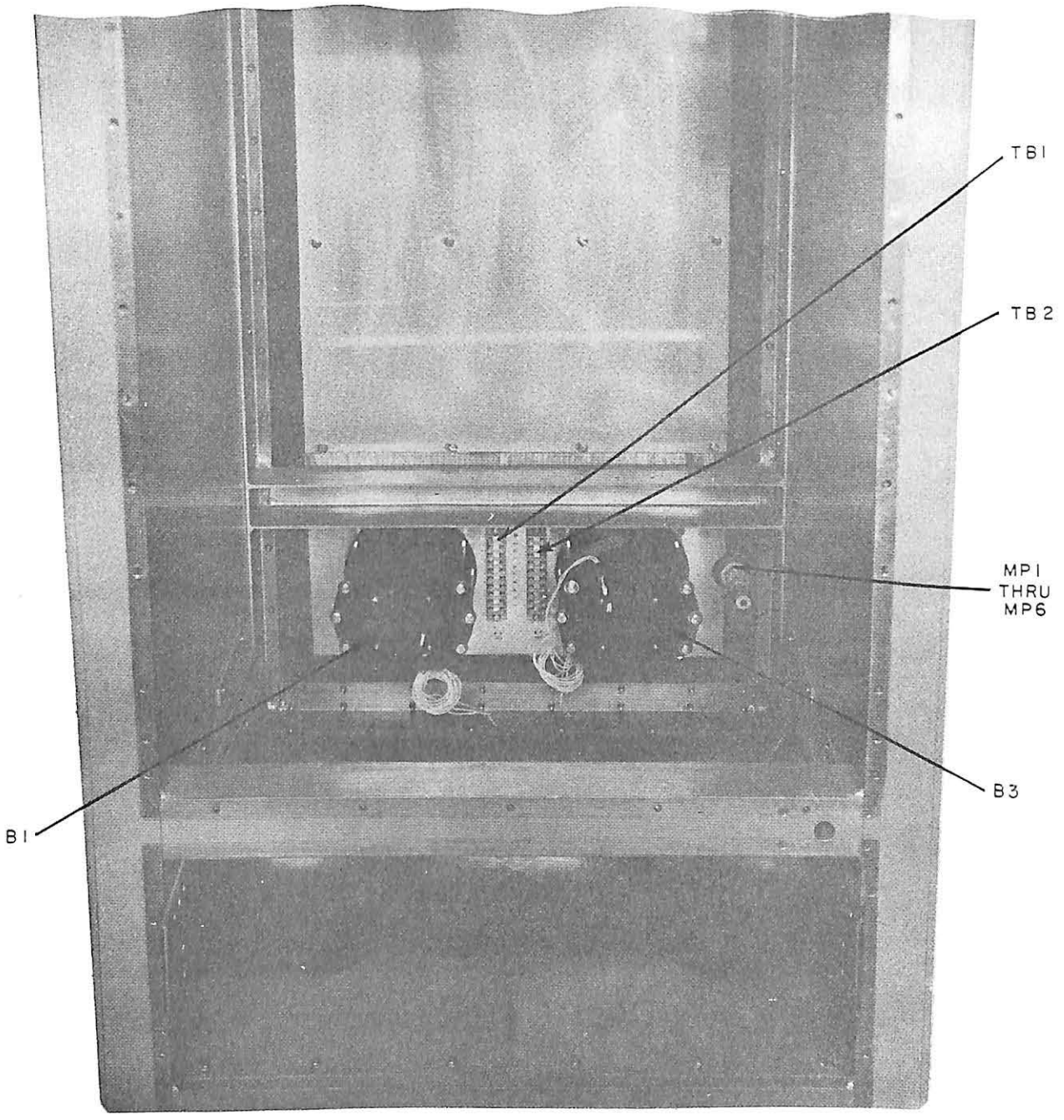


Figure 5-16. Tape Transport Cabinet, Partially Assembled View of Lower Half, Water Cooled

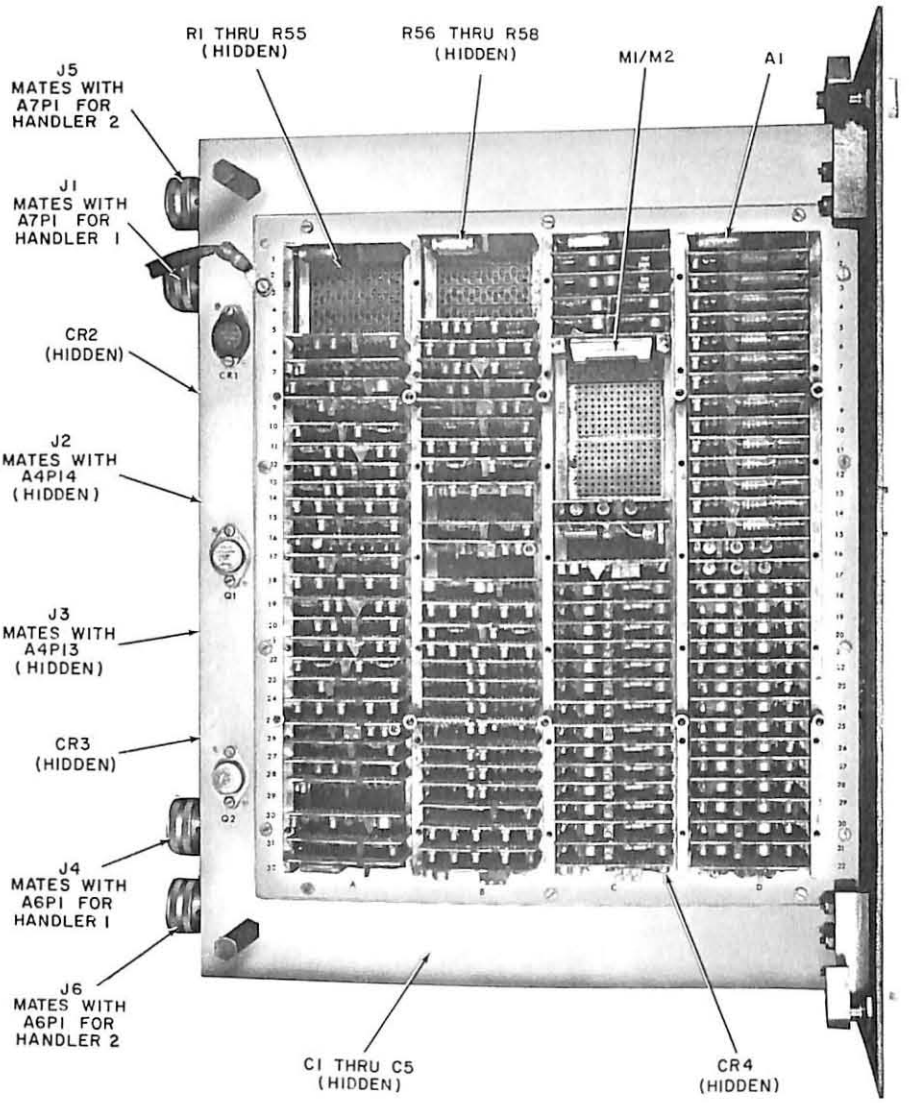


Figure 5-17. Tape Transport Logic Chassis Drawer Assembly A17

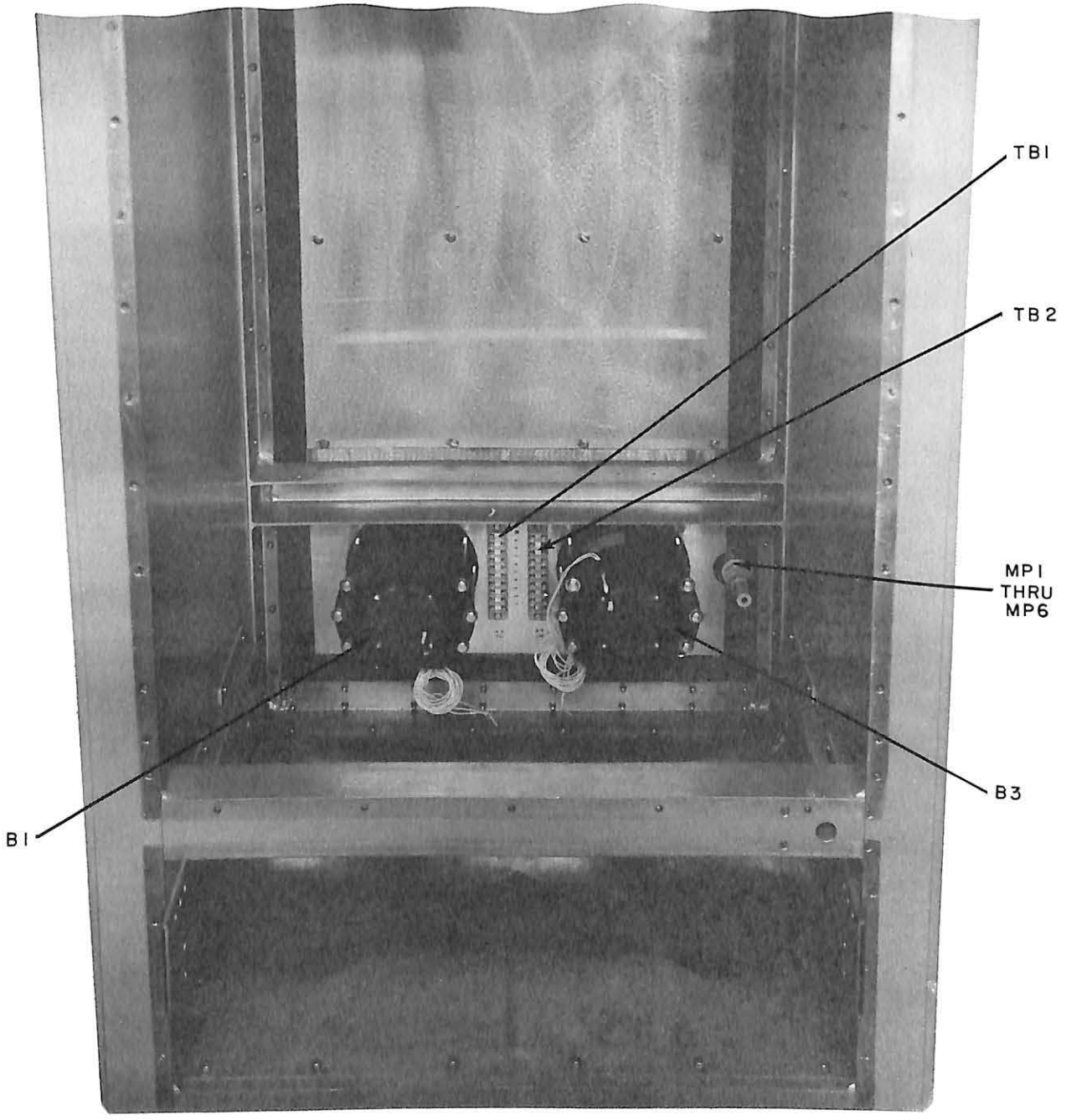


Figure 5-16. Tape Transport Cabinet, Partially Assembled View of Lower Half, Water Cooled

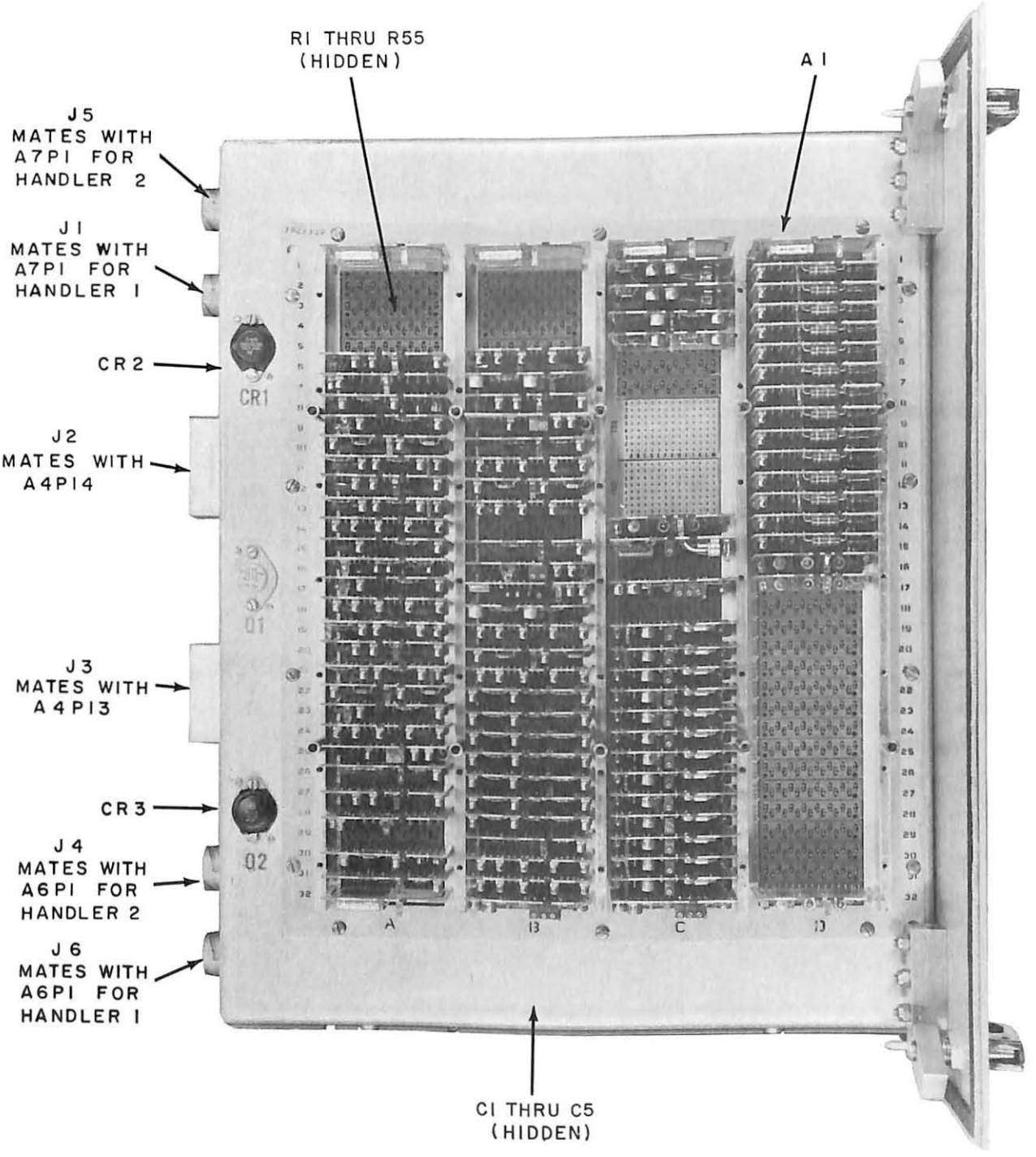


Figure 5-17. Tape Transport Control Logic Chassis Drawer Assembly A17

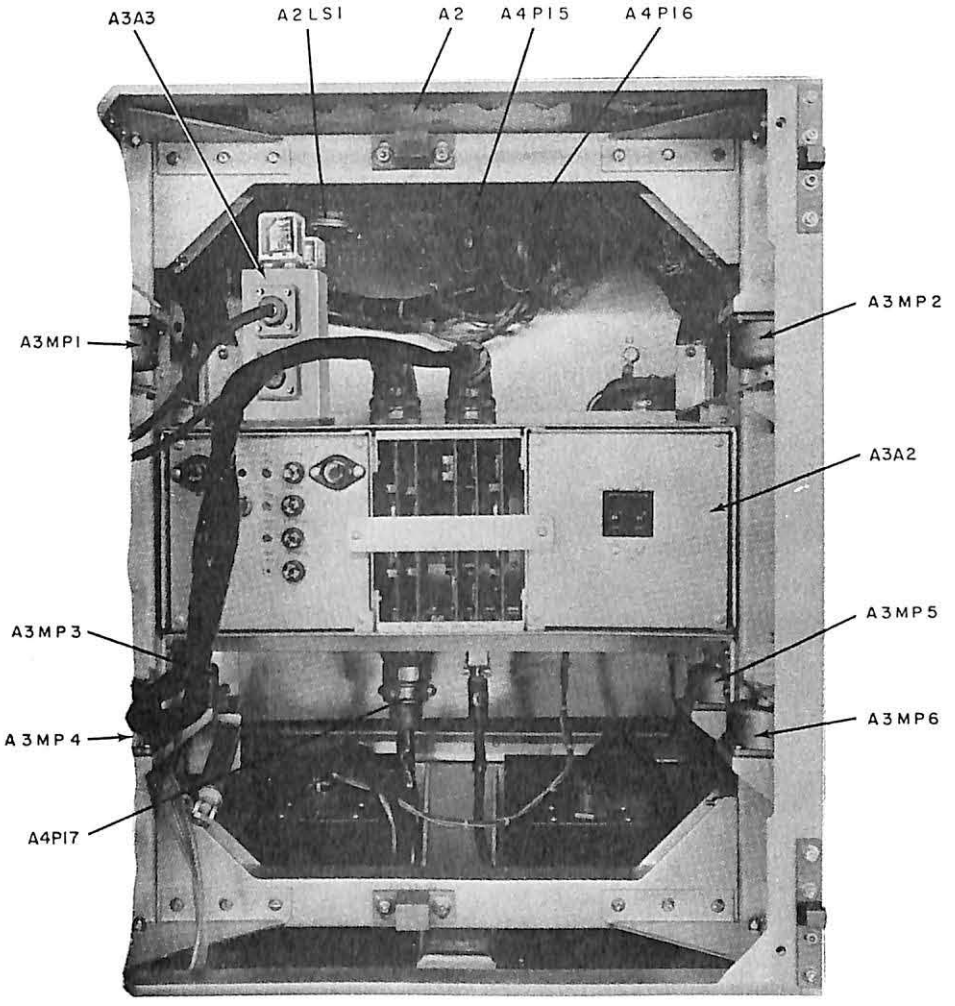


Figure 5-18. Tape Transport Cabinet, Interior View, Upper Half

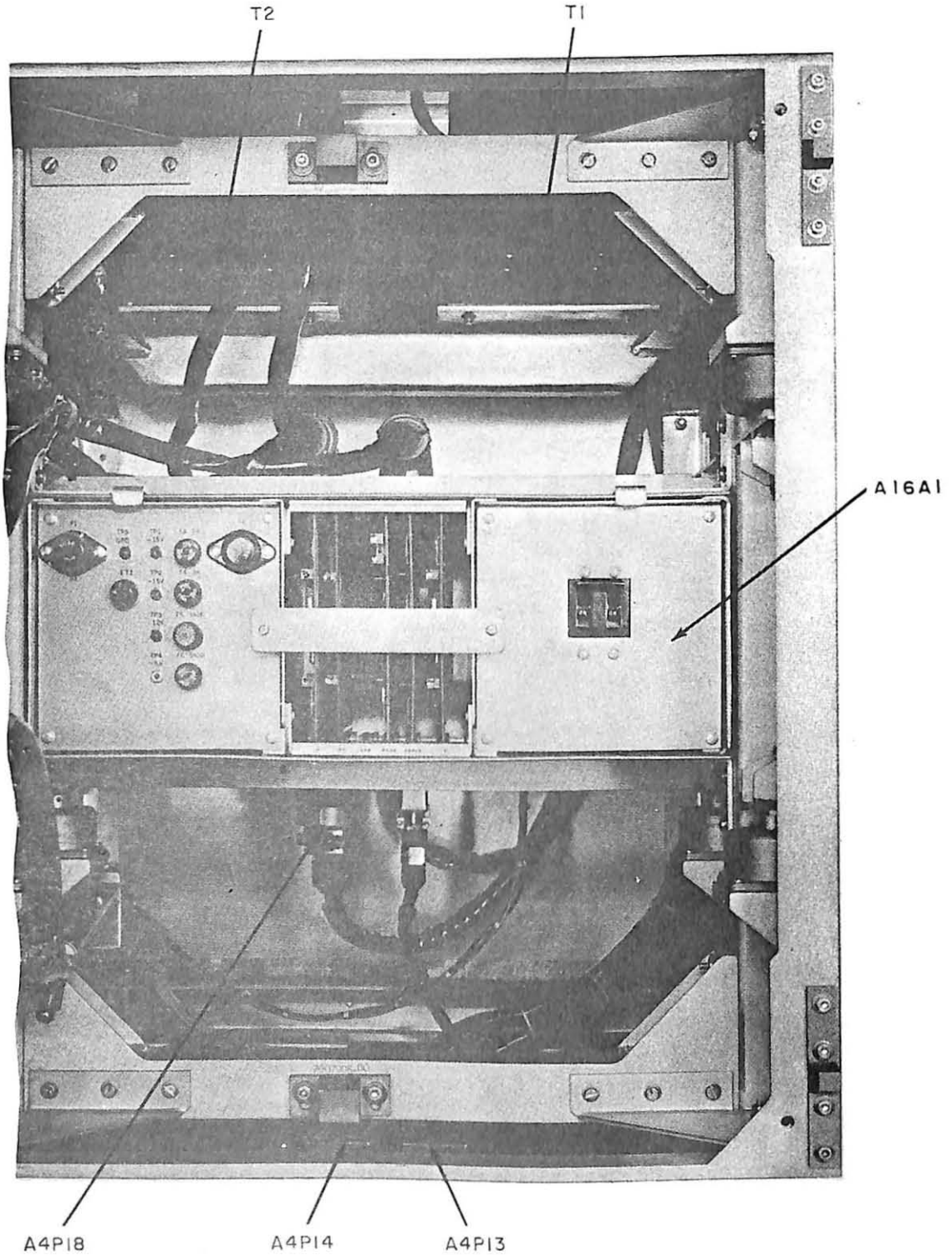


Figure 5-19. Tape Transport Cabinet, Interior View, Lower Half

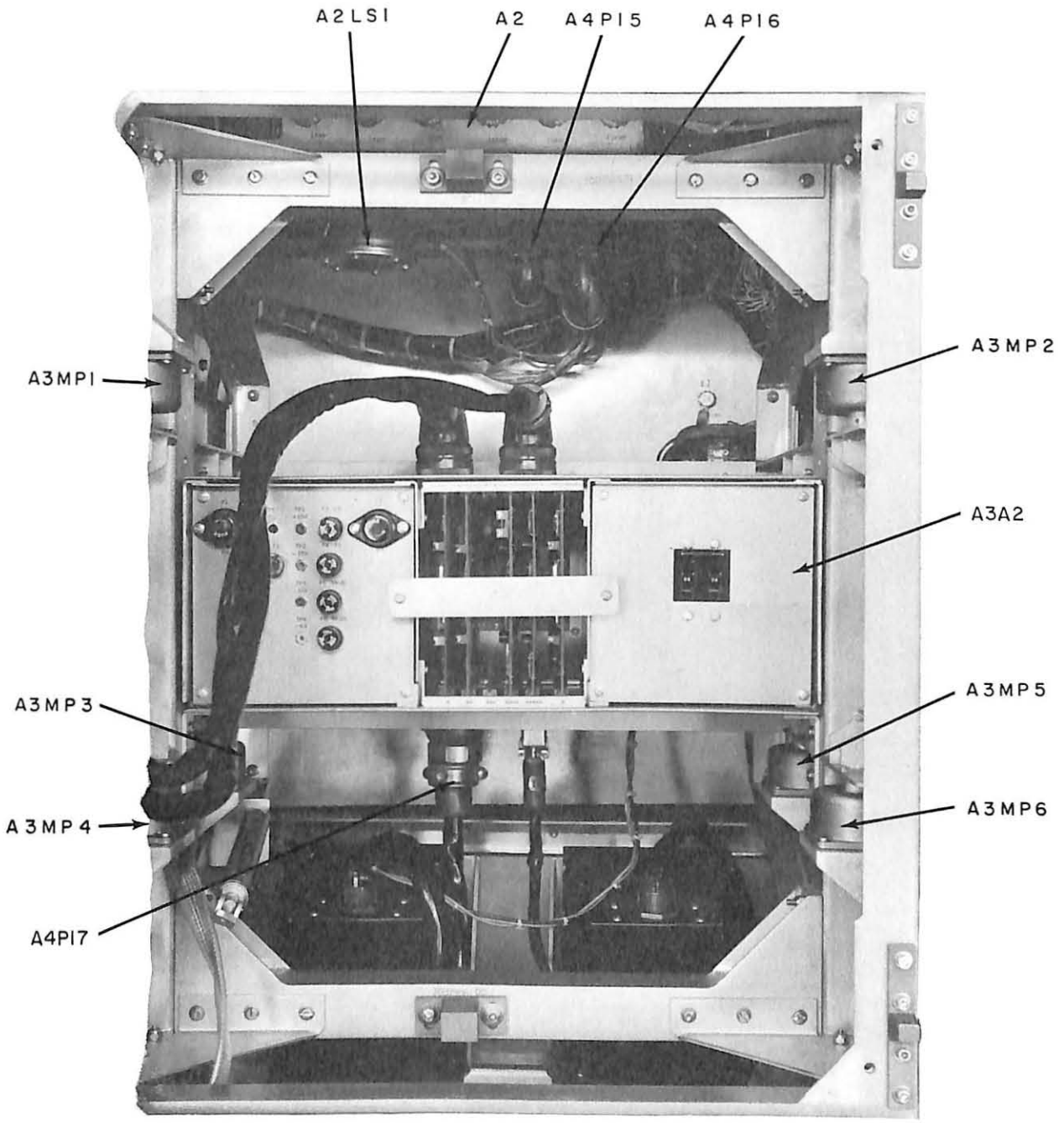


Figure 5-18. Tape Transport Cabinet, Interior View, Upper Half

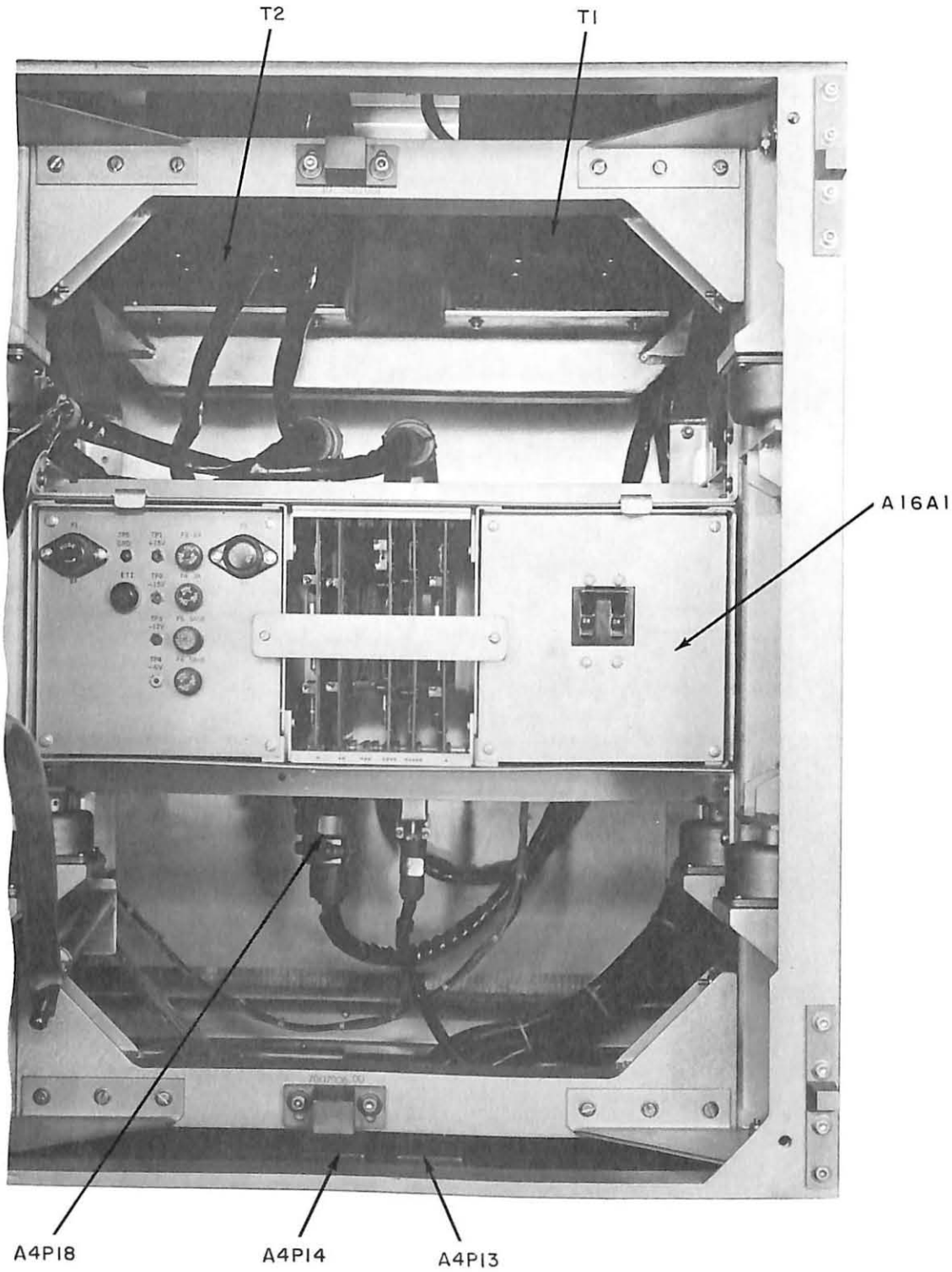


Figure 5-19. Tape Transport Cabinet, Interior View, Lower Half

5-4. CORRECTIVE MAINTENANCE.

Paragraph 5-4 provides the information required to correct any malfunction except tape transport failures. For tape transport failures, consult the Potter tape handler manual.

a. FAILURE REPORT. - Report each failure of the equipment, whether caused by a defective part, wear, improper operation, or an external cause. The importance of providing complete information cannot be over emphasized. Be sure that you include the model designation and serial number of the equipment (from the equipment identification plate), the type number and serial number of the major unit (from the major unit identification plate), and the type number and reference designation of the particular defective part (from the technical manual or the Potter tape handler manual). Describe the cause of failure completely. Do not substitute brevity for clarity.

b. CHECKS AND ADJUSTMENTS. - The checks and adjustments for the MTU are used to achieve optimum performance from the system. The checks and adjustments associated with the magnetic tape unit are divided into two groups: those for the tape handlers and those for the magnetic tape control and power supply circuits.

Checks and adjustments pertaining to the tape transports are described in paragraph 5-2 of the Potter tape handler manual.

c. COMPONENT REMOVAL AND REPLACEMENT.

(1) TEST BLOCK LOCATION. - To expose the test blocks for any chassis, proceed as follows.

STEP 1. Lift latch fastener of lower drawer assembly, turn 90 degrees, and open door.

STEP 2. Remove chassis engaging wrench from spring clips.

STEP 3. If test blocks are to be exposed for upper drawer, repeat step 1 for upper drawer.

STEP 4. Remove knurled protective knob from front center of appropriate drawer.

STEP 5. Use combination tool and turn three retaining screws on left front of drawer panel.

STEP 6. Swing front panel out to expose test blocks and connections to switches and indicators on front panel (see figure 5-9 or 5-10).

(2) EXTENDING A DRAWER. - To extend a drawer from the MTU, proceed as follows.

CAUTION

Remove the power from the MTU circuitry before extending a drawer to prevent possible damage to the logic modules.

STEP 1. Ensure that three retaining screws on front panel are secured.

STEP 2. Remove knurled protective knob from front of drawer.

STEP 3. Use combination tool and turn exposed drawer locking screw counterclockwise until plugs on rear of drawer are disengaged from jacks on rear panel.

CAUTION

When a drawer is to be removed or extensive work performed with a drawer extended, remove the chassis door by opening and then lifting it vertically off the hinge pins. Place in a safe place until the work is completed.

STEP 4. Slowly pull drawer forward to fully-extended position. Slide catch will engage when drawer is fully extended. It may be necessary to lift front of drawer slightly to engage slide catch.

STEP 5. To return drawer to cabinet, release slide catch, push drawer into cabinet, and, using combination tool, turn socket clockwise until drawer is fully seated in cabinet. Replace knurled protective knob.

(3) OPENING A CHASSIS. - To open the chassis and expose the chassis wiring, proceed as follows.

STEP 1. Extend drawer as directed in steps 1 through 4, paragraph 5-4c(2).

STEP 2. Press spring catch on rear edge of left chassis (see figure 5-5.

STEP 3. Slowly swing chassis on hinges to expose wiring.

STEP 4. To secure chassis to drawer, slowly swing chassis closed until spring catch snaps into latched position.

(4) DRAWER REMOVAL. - To remove a drawer from the cabinet, proceed as follows.

STEP 1. Prepare work area on which to place drawer assembly.

STEP 2. Extend drawer as directed in steps 1 through 4, paragraph 5-4c(2).

WARNING

Do not attempt to remove a chassis alone. Get assistance. Personnel disregarding this warning could very easily receive a serious injury. Do not leave the chassis unattended when the chassis retaining screws have been removed. Carry the chassis to the work area immediately after the chassis retaining screws have been removed.

STEP 3. Remove two flat-head, slotted, chassis-retaining screws from top and bottom of front of drawer slide (see figure 5-5.)

NOTE

The chassis retaining screws may be placed into the chassis nut a half turn or so, as shown in figure 5-5, for safekeeping and to avoid damaging the threads.

STEP 4. Slowly pull drawer forward from cabinet.

(5) DRAWER REPLACEMENT. - The replacement procedure for the drawer assembly is the reverse of the drawer removal procedure.

NOTE

Care must be exercised, when the chassis is positioned into the slide assemblies, to ensure that the slots in the rear of the right-hand chassis (A2) engage with the securing studs on the rear of the slide assemblies.

(6) EXTENDING POWER SUPPLY PS1. - To extend the logic power supply, proceed as follows.

STEP 1. Lift latch fasterners and turn 90 degrees.

STEP 2. Slowly slide power supply from cabinet until slide stops engage (click).

(7) RETURNING POWER SUPPLY PS1. - To return the logic power supply to the cabinet, proceed as follows.

STEP 1. Depress forward slide stops located on each slide assembly and slowly push power supply into cabinet.

STEP 2. Rotate latch fasteners 90 degrees to lock power supply in place and depress latch fasteners.

(8) REMOVING POWER SUPPLY PS1. - To remove the logic power supply, proceed as follows.

STEP 1. Perform steps 1 and 2 of paragraph 5-4c(5).

STEP 2. Remove cable plug assembly A1OP1 from top rear of power supply (see figure 5-13).

STEP 3. Depress rear slide stops located on each slide assembly and pull power supply forward from slide assemblies.

(9) REPLACING POWER SUPPLY PS1. - To replace the logic power supply, proceed as follows.

STEP 1. Slide power supply into slide assemblies until slide stops engage (click).

STEP 2. Connect cable plug assembly A1OP1 to jack J1.

STEP 3. Perform steps 1 and 2 of paragraph 5-4c(5).

(10) EXTENDING TAPE TRANSPORT CONTROL CHASSIS A17. - The procedure for extending chassis A17 is the same as the procedure in paragraph 5-4c(5).

(11) RETURNING TAPE TRANSPORT CONTROL CHASSIS A17. - The procedure for returning chassis A17 is the same as the procedure in paragraph 5-4c(6).

(12) REMOVING TAPE TRANSPORT CONTROL CHASSIS A17. - The procedure for removing chassis A17 is the same as the procedure in paragraph 5-4c(7) except that in step 2, six cable plug assemblies must be disconnected from the rear end of the chassis.

(13) REPLACING TAPE TRANSPORT CONTROL CHASSIS A17. - The procedure for replacing chassis A17 is the same as the procedure in paragraph 5-4c(8), except that in step 2, six cable plug assemblies must be connected to the jacks on the rear end of the chassis.

CAUTION

Ensure that both A7P1's and both A6P1's are mated correctly for their respective transports. See figure 5-17.

(14) FILTER MAINTENANCE. - The air filters for air-cooled tape units are located behind the grill(s) above the primary power control panel(s) at the top front of the MTU. These filters must be cleaned once a week. To accomplish filter cleaning, proceed as follows.

STEP 1. Turn quarter-turn fasteners on grill 90 degrees counterclockwise.

STEP 2. Swing grill upward and lift out filter.

STEP 3. Clean filter in hot soapy water and dry with forced air.

STEP 4. Apply thin coat of SAE #5 oil. Wipe off excess oil with clean cloth.

STEP 5. Replace filter, ensuring that spring clips are against grill and not cabinet.

STEP 6. To secure grill, depress and turn quarter-turn fasteners 90 degrees clockwise.

(15) CIRCUIT MODULE REPLACEMENT. - When a malfunction is isolated to a particular circuit module, replace module. This module replacement concept of troubleshooting simplifies repair procedures since it is the lowest level of repair to be performed. To replace a module, proceed as follows.

STEP 1. Extend appropriate drawer following steps 1 through 4 as listed in paragraph 5-4c(2).

STEP 2. Obtain physical position of module on chassis from appropriate functional schematic diagram or chassis map.

STEP 3. Remove necessary hold-down strap or straps and slowly but firmly remove module from chassis jack.

STEP 4. Replace module, fasten hold-down straps, and perform step 5 of paragraph 5-4c(2).

d. WIRE-WRAP PROCEDURES.

(1) GENERAL. - Most of the electrical connections in the MTU are mechanical and solderless. These connections are formed by wrapping a component lead or wire around a terminal post. Each terminal post has a rectangular cross section. A wrapped connection forms a coil around the terminal post, with points of contact at each of the four terminal post corners. The four points of contact are made for each turn of the connecting wire that encircles the post.

Before a broken wire can be replaced, the terminal post lead must be removed. An unwrap tool is used for removing the lead. If it is impractical to remove the wire, trim both ends of the wire and leave it in place. A replacement wire lead is routed exactly as the original lead except that it is placed on top of the other lead.

Wire-wrap connections are made with a wire-wrap gun. This gun has a stationary sleeve and three bits, 20 gauge, 24 gauge, and 30 gauge. The stationary sleeve has a slotted end which prevents the wire lead from rotating during the wrapping operation and holds the bit in place. The sleeve is held in the wire-wrap gun by a chuck. Each of the bits has a longitudinal groove that accommodates the end of the wire to be wrapped. A hole in the end of each bit allows the bit to be slipped over the terminal post where the wire-wrap connection is to be made.

When the wire-wrap gun is used, the end of the wire is inserted between the longitudinal groove in the bit and the stationary sleeve. The wire is bent so the wire lead is perpendicular to the longitudinal axis of the bit before the wire-wrap gun and wire are positioned over the terminal. Positioning the gun over the terminal and pressing the trigger allows the wrap to be made. The wire-wrap gun supplies all the power.

(2) PREPARATION FOR WIRE WRAPPING. - To prepare for a wire-wrapping operation, proceed as follows.

STEP 1. Strip wire with automatic stripping machine whenever possible; however, hand stripping machine with die type blades can be used.

NOTE

Do not use wire strippers with "V" type blades.

STEP 2. When forming wire patterns, use routing bullets or spacers over via terminals to eliminate shorting and tight wires.

STEP 3. When installing wires in previously-wrapped area, use nonmetallic pointed rod to move adjacent wires from terminal to be wrapped.

(3) WIRE-WRAPPING PROCEDURE. - The wire-wrapping tools and the necessary wire-wrapping information are listed in tables 5-12 and 5-13 respectively. To wire-wrap, proceed as follows.

NOTE

Ensure the gun battery is fully charged before attempting the 20-guage wrap.

STEP 1. Select proper gun, bit, sleeve, and level-stop collar.

STEP 2. Insert stripped end of wire in wire slot provided in wrapping bit. Bend wire into insulation relief which is located on side of sleeve.

STEP 3. Squarely place wrapping gun over terminal and squeeze trigger.

NOTE

A momentary squeeze on the trigger is sufficient to complete the connection. To produce an acceptable connection, the backforce (pressure exerted by the operator in oppostion to the wire wrapping around the terminal) should be approximately 1 to 1-1/2 pounds; however, this is acquired with experience only. Figure 5-20 shows acceptable and unacceptable connections.

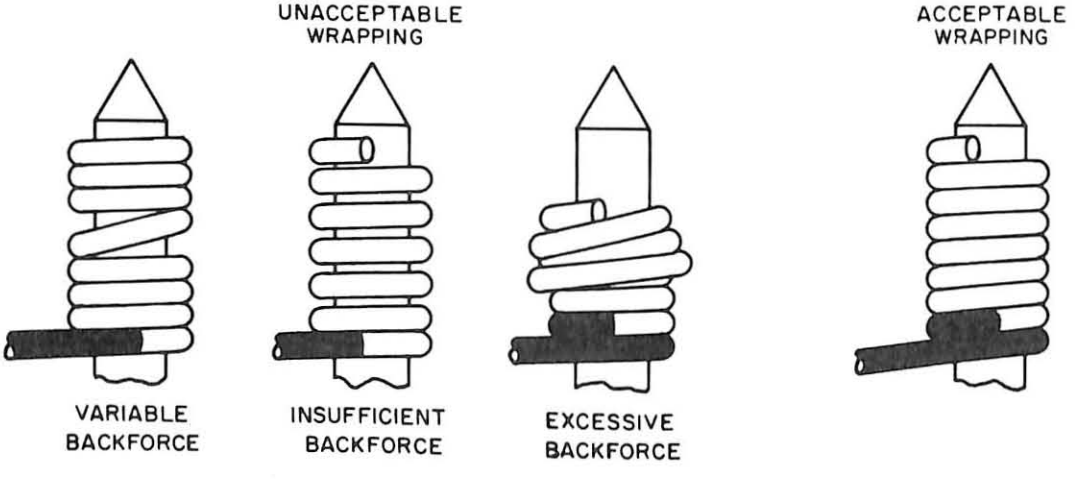


Figure 5-20. Wire Wrapping

TABLE 5-12. WIRE-WRAPPING TOOLS REQUIRED

ITEM	MODEL OR TYPE
Wrapping Tool	
Battery Gun 22 to 32 ga.	14R2 (8130-132)
Unwrapping Tool	
Dual 20 to 26 ga.	500130 (8130-138)
Bits and Sleeves	
24 ga. standard wrap on 0.035 x 0.050 pin bit	26589 (8130-123)
sleeve	17611-2 (8130-129)
Level-Stop Collars	
Level One	Brown
Level Two	Red
Level Three	Orange

TABLE 5-13. WIRE-WRAPPING INFORMATION

WIRE GAUGE	PIN DIMENSION	STRIP LENGTH (INCHES)	TURNS OF BARE WIRE	TURNS OF INSULATION ON MODIFIED WRAPS
20	0.035 x 0.050	1-1/2 ± 1/16	4 to 5	1/2 to 2
24	0.035 x 0.050	1-1/2 ± 1/16	5 to 6	1/2 to 2
30	0.035 x 0.050 0.025 x 0.025	1-1/2 ± 1/16	7 to 10	1/2 to 2

SECTION 6

PRINTED CIRCUIT CARDS

6-1. GENERAL

This section describes each printed circuit card used in the MTU. The descriptions are functional in that they describe each circuit in terms of its inputs and outputs rather than its internal electronic operation.

Functionally, the inputs and outputs of the circuit modules are defined as highs and lows. For the normal logic type circuit, a low implies -4.5 volts and a high implies 0.0 volt. On I/O, and other special circuits, a low may imply -3 or -15 volts.

When a printed circuit module is inserted into a jack, the external edge of the module displays five color-coded bands. These colored bands are read in the same manner as the color code for resistors. The color code is applicable to the last five digits of the type number. A module with black, red, black, brown, and red bands would read 02012. Thus, because the 700 series type modules are used in the MTU, this would indicate the module is a type 7002012.

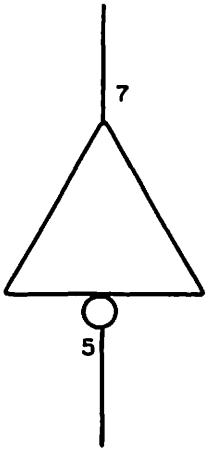
The least significant digit in the card type number gives the revision of the basic card. That is, if card type 7002010 has been revised 3 times it is listed as card type 7002013. Any card type of a new revision can replace an old revision card, however, an older revision card cannot be substituted for a new revision card. The card type numbers and the functional schematics of Section 8 and card descriptions that follow will not be updated if a new revision of a card is released, since the new revision replaces the old card.

6.2. FUNCTIONAL DESCRIPTION OF PRINTED CIRCUIT CARDS.

Figures 6-1 through 6-49 contain the following information.

Card name and type number.
Symbol used to represent the card on the functional schematics.
A logic description and a design description.
Input and output pin numbers for each circuit on the card.
Power requirements.

Pin numbers are shown on logic symbols for each module. Where more than one set of pin numbers can be applied to the same module because of circuit duplicity, the numbers are listed in rows. On these figures the upper ((or outer) input pin numbers are associated with the upper (or outer) output pin numbers.



LOGIC SYMBOL

LOGIC DESCRIPTION

When the input is high the output will be a low. When the input is low, the output will be a high.

ELECTRICAL DESCRIPTION

This circuit operates with inputs of -4.5 volts and 0.0 volts. The excursions of the output are equal to and opposite of those at the inputs.

With 0.0 volts applied, the output is clamped at -4.5 volts. With -4.5 volts applied the circuit allows a path to ground placing the output at 0.0 volts.

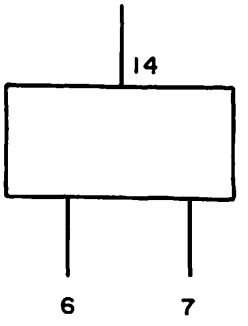
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volts	HIGH	0.0 Volts
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Grd	+15.0	-15.0	-4.5

Figure 6-1. Inverter, Module 7000070



LOGIC SYMBOL

LOGIC DESCRIPTION

This circuit produces a 2-millisecond pulse output on pin 14, alternating between 0 and -15 volts. A potentiometer connects between input pins 6 and 7 and controls the frequency from 2 to 200 cps.

ELECTRICAL DESCRIPTION

The output is normally connected to the input of 7002090 card with the ground return connected to pin 1.

Used to supply substitute timing signals for maintenance and test purposes.

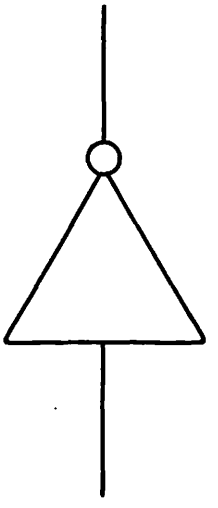
LOGIC

INPUT		OUTPUT	
HIGH		HIGH	0.0 Volt
LOW		LOW	-15 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Grd	-	-15	-

Figure 6-2. Low-Speed Variable Pulse-Delay Oscillator, Module 7000210



LOGIC SYMBOL

LOGIC DESCRIPTION

With a high at the input, the output will be a low. With a low at the input, the output will be a high.

ELECTRICAL DESCRIPTION

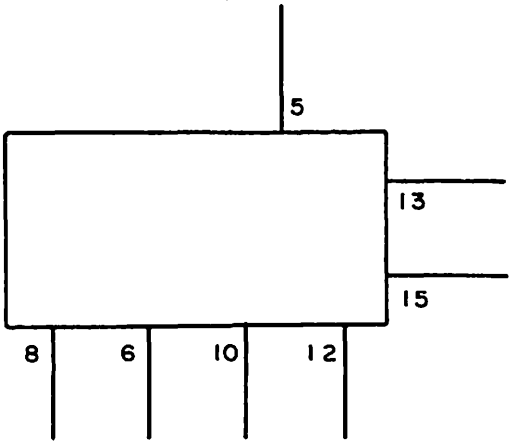
The four inverters contained in this circuit (three with two inputs, one with one input) operate with logic level inputs and furnish outputs of -15 volts.

With the input at -4.5 volts, the output is ground. With the input at ground, the output will be -15 volts.

LOGIC			
INPUT		OUTPUT	
HIGH	0.0 Volt	HIGH	0.0 Volt
LOW	-4.5 Volts	LOW	-15 Volts

POWER REQUIREMENTS				
PIN	1	2	3	
VOLTAGE	Grd	+15	-15	

Figure 6-3. Inverter-Heavy Duty, Module 7000780



ELECTRICAL CONNECTIONS

LOGIC DESCRIPTION

(NOT APPLICABLE)

ELECTRICAL DESCRIPTION

This circuit, combined with external capacitors (pins 6 and 13, 8 and 15) and resistors (pins 10 and 12), generates rectangular pulses from one cps to several hundred cps. The output at pin 5 is a square wave moving between 0 volt and -4.5 volts.

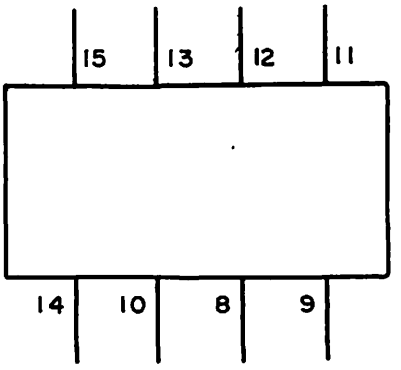
LOGIC

INPUT		OUTPUT	
HIGH		HIGH	0.0 Volt
LOW		LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Grd	+15	-15	-4.5

Figure 6-4. Oscillator, Square Wave - Variable, Module 7000850



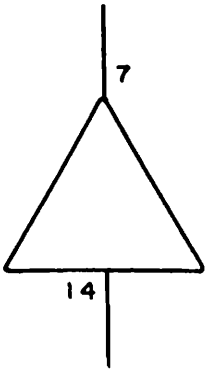
ELECTRICAL CONNECTIONS

LOGIC DESCRIPTION	ELECTRICAL DESCRIPTION
(NOT APPLICABLE)	This module consists of an assortment of capacitors for use, as required, with other circuits.

LOGIC			
INPUT		OUTPUT	

POWER REQUIREMENTS				
PIN	1	2	3	4
VOLTAGE	Grd	+15	-15	-4.5

Figure 6-5. Capacitor Assembly, Module 7001000



LOGIC SYMBOL

LOGIC DESCRIPTION

A high at input pin 14 produces a high at output pin 7.

A low at input pin 14 produces a low at output pin 7.

ELECTRICAL DESCRIPTION

This circuit operates with inputs of -4.5 volts and 0.0 volt. When 0.0 volt is applied at pin 14, the circuit is enabled, completing a path to -15 volts (connected to pin 7 through the tape-head coil) allowing approximately 100 ma to flow. When -4.5 volts is applied, the circuit is disabled and no current flows through the head.

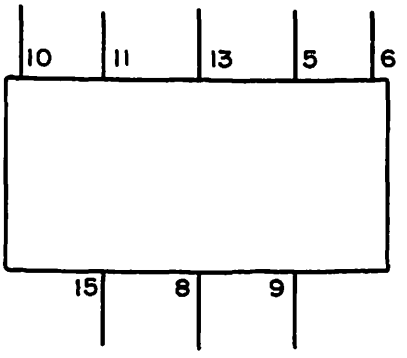
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volt	HIGH	0.0 Volt
LOW	-4.5 Volts	LOW	-15 Volts

POWER REQUIREMENTS

PIN	1	2	3 & 10	4
VOLTAGE	Grd	+15	-15	-4.5

Figure 6-6. Amplifier, Electronic Control-Write, Module 7001070



ELECTRICAL CONNECTIONS

LOGIC DESCRIPTION

(NOT APPLICABLE)

ELECTRICAL DESCRIPTION

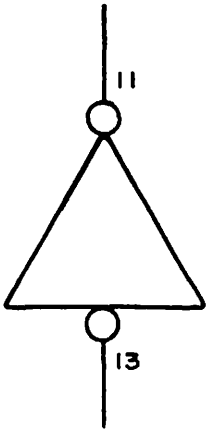
The circuit operates from -26.5 volts applied to pin 15 and delivers -15 volts regulated at pins 5 and 6.

An internally-mounted transistor senses changes in voltage and effects a change in the resistance of an external transistor causing it to conduct more or less depending on the fluctuations.

Output level may be varied by adjustment of a resistor connected to the base of the internal transistor.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	8	9	15	
		HIGH	0.0 Volt	VOLTAGE	Grd	Grd	-26.5	
		LOW	-15 Volts					

Figure 6-7. Voltage Regulator (15V), Module 7001090



LOGIC SYMBOL

LOGIC DESCRIPTION

A low at input pin 13 results in -15 volts at output pin 11. A logical high at input pin 13 results in an open circuit to pin 11.

ELECTRICAL DESCRIPTION

This circuit, when enabled by -4.5 volts at pin 13, furnishes -15 volts at pin 11 for driving up to seven write heads. When 0.0 volt are applied at pin 13 the output (pin 11) reflects an infinite resistance interrupting current to the write heads.

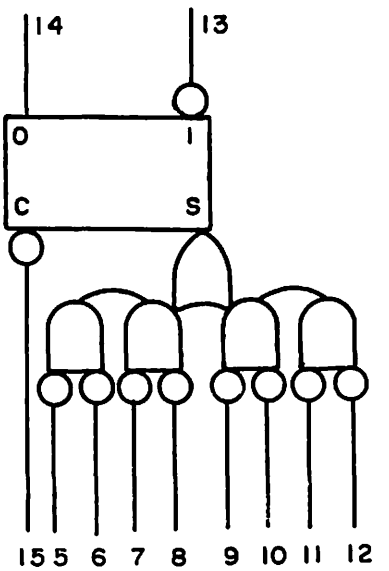
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volt	HIGH	Open
LOW	-4.5 Volts	LOW	-15 Volts

POWER REQUIREMENTS

PIN	1	2	3	9
VOLTAGE	Grd	+15	-15	-26.5

Figure 6-8. Amplifier, Write Enable, Module 7001170



LOGIC SYMBOL

LOGIC DESCRIPTION

The right side of the flip-flop symbol is referred to as the set side, and the left as the clear side.

A low input on the left side will cause a low output on the left side, and a high output on the right side. When one of the AND's on the right side has two low inputs, the output on the right side is a low and the output on the left side is a high.

NOTE

The input configuration can be reversed so that the multiple-input inverter functions as the clear-side inverter.

ELECTRICAL DESCRIPTION

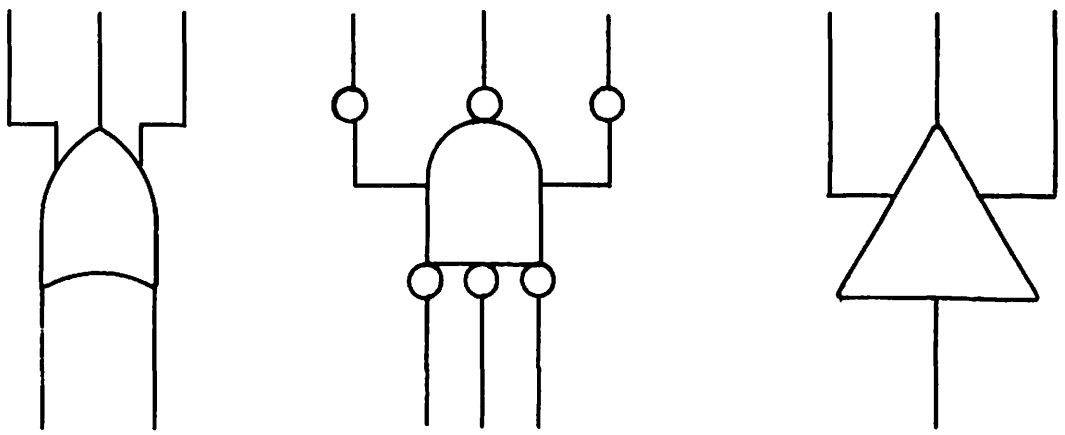
This circuit operates with input pulses that have positive excursions between 0.0 vdc to -0.5 vdc, and negative excursions between -3.6 vdc to -5.4 vdc. The excursions of the output voltage pulses are the same as those given for the input pulses.

The maximum input current required is 7.1 ma. The circuit can drive four AND's plus one indicator driver or 4 AND-OR's plus one indicator driver.

This circuit's maximum speed is such that the second of two series-connected circuits produces a usable output before the clock phase input to the first has expired. A normal clock phase is 166 nanoseconds long.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volt	HIGH	0.0 Volt	VOLTAGE	Grd	+15	-15	-4.5
LOW	-4.5 Volts	LOW	-4.5 Volts					

Figure 6-9. Flip-Flop, Module 7002000



LOGIC SYMBOLS

LOGIC DESCRIPTION

When any of the input pins has a high input, the output of that circuit is a high. When all of the input pins have a low input, the output of that circuit is a low.

This card contains two circuits, one having three inputs and one having two inputs.

ELECTRICAL DESCRIPTION

The circuit operates with input pulses that have excursions between 0.0 to -0.5 vdc and -3.6 to -5.4 vdc. The output voltage excursion is the same as those given for the input voltage pulse.

The maximum input current required is 5.8 ma. The circuit can drive six AND-OR's or six AND's from each output pin, for a total of 18 circuits.

This circuit's maximum speed is such that the second of two series-connected circuits produces a usable output before the clock phase input to the first has expired.

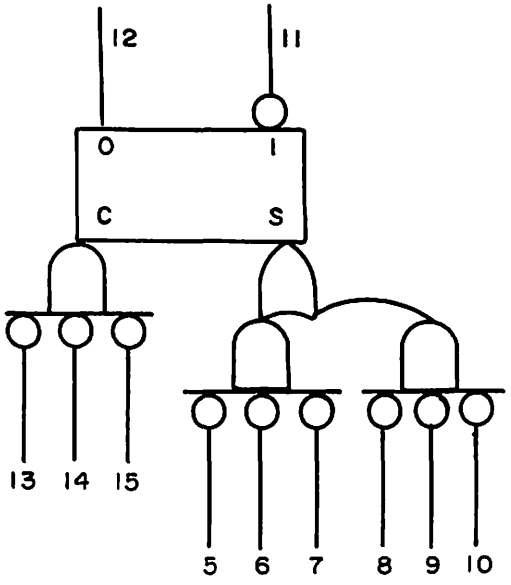
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volt	HIGH	0.0 Volt
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Grd	+15	-15	-4.5

Figure 6-10. Amplifier Driver, Module 7002012, 7002013



LOGIC SYMBOL

LOGIC DESCRIPTION

The right side of the flip-flop symbol is the set side, and the left the clear side.

When an AND gate on the right side has all low inputs, the output on the right side is a low and the output on the left side is a high. When the AND on the left side has all low inputs, the output on the left side is a low and on the right side the output is a high.

NOTE

The input configuration can be reversed so that the multiple-AND's function as the clear side.

ELECTRICAL DESCRIPTION

This circuit operates with input pulses that have positive excursions between 0.0 vdc to -0.5 vdc, and negative excursions between -3.6 vdc to -5.4 vdc. The excursions of the output voltage pulses are the same as those given for the input pulses.

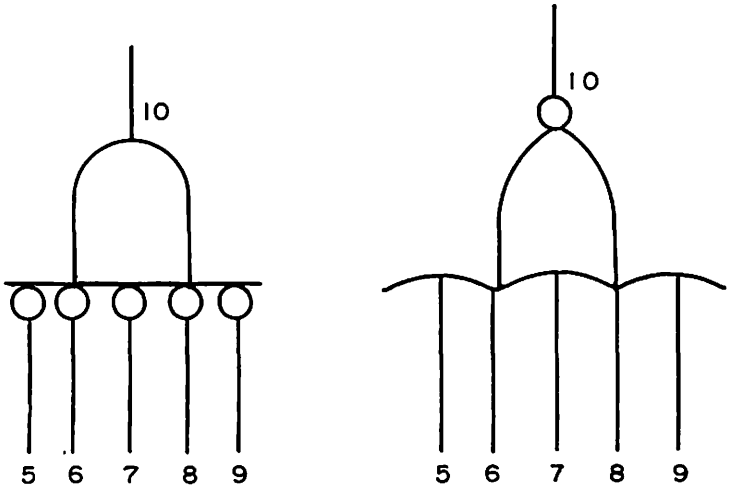
The maximum input current required is 7.1 ma. The circuit can drive four AND's plus one indicator driver.

This circuit's maximum speed is such that the second of two series-connected circuits produces a usable output before the clock phase input to the first has expired. A normal clock phase is 166 nanoseconds long.

LOGIC			
INPUT		OUTPUT	
HIGH	0.0 Volt	HIGH	0.0 Volt
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS				
PIN	1	2	3	4
VOLTAGE	Grd	+15	-15	-4.5

Figure 6-11. Flip-Flop, Module 7002020

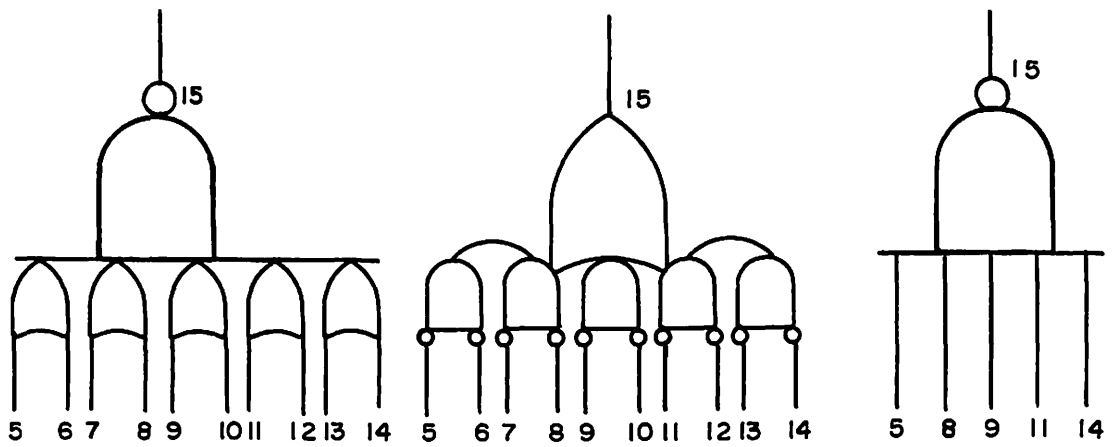


LOGIC SYMBOLS

LOGIC DESCRIPTION	ELECTRICAL DESCRIPTION
When any one or more inputs are high, the output is a low. When all used inputs have a low, the output is a high.	The circuit operates with input pulses that have positive excursions between 0.0 vdc to -0.5 vdc, and negative excursions between -3.6 vdc to -5.4 vdc. The excursions of the output voltage pulses are the same as those given for the input. The maximum input current required is 5.8 ma. The circuit can drive five AND-OR's or six AND's. This circuit's maximum speed is such that the second of two series-connected circuits produces a usable output before the clock phase input to the first has expired. A normal clock phase is 166 nanoseconds long.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volt	HIGH	0.0 Volt	VOLTAGE	Grd	+15	-15	-4.5
LOW	-4.5 Volts	LOW	-4.5 Volts					

Figure 6-12. Inverter, Module 7002030



LOGIC SYMBOLS

LOGIC DESCRIPTION

When both inputs to any one of the AND circuits are low, the output of the circuit is high. Conversely, the circuit produces a low output when a high input is present on at least one input to all AND circuits.

ELECTRICAL DESCRIPTION

This circuit operates with input pulses that have positive excursions to a level between 0.0 vdc and -0.5 vdc, and negative excursions to a level between -3.0 vdc and -5.0 vdc. The excursions of the output voltage pulses are the same as those given for the input pulses.

The maximum input current required is 7.1 ma. The circuit can drive five AND-OR's or six AND's.

This circuit's maximum speed is such that the second of two series-connected inverters produces a usable output before the clock phase input to the first has expired. A normal clock phase is 166 nanoseconds long.

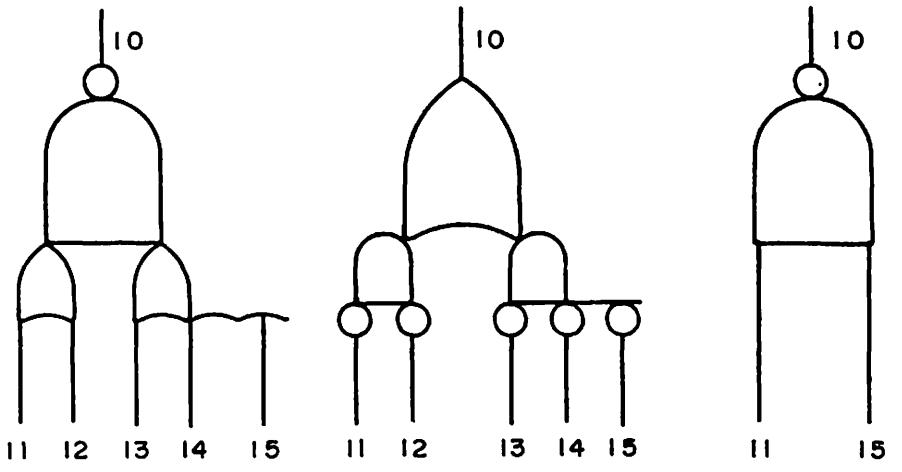
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volt	HIGH	0.0 Volt
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Grd	+15	-15	-4.5

Figure 6-13. Inverter, Module 7002040



LOGIC SYMBOLS

LOGIC DESCRIPTION

When all of the inputs to either AND are low, the output of the circuit is a high. When at least one input to each of the AND's is a high, the output is a low. Unused AND's must have a high input.

ELECTRICAL DESCRIPTION

This circuit operates with input pulses that have positive excursions between 0.0 vdc and -0.5 vdc, and negative excursions between -3.6 vdc and -5.4 vdc. The excursions of the output voltage pulses are the same as those given for the input pulses.

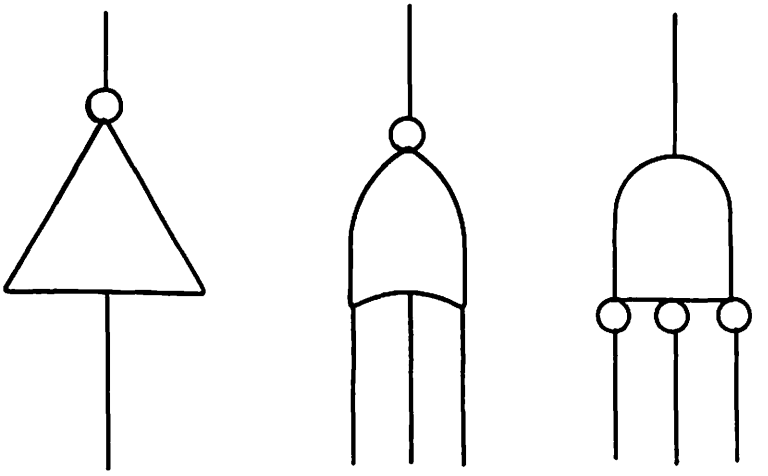
The maximum input current required is 6.85 ma. The circuit can drive six AND's or five AND-OR's.

This circuit's maximum speed is such that the second of two series-connected circuits produces a usable output before the clock phase input to the first has expired. A normal clock phase is 166 nanoseconds long.

LOGIC			
INPUT		OUTPUT	
HIGH	0.0 Volt	HIGH	0.0 Volt
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS				
PIN	1	2	3	4
VOLTAGE	Grd	+15	-15	-4.5

Figure 6-14. Inverter, Module 7002050



LOGIC SYMBOLS

LOGIC DESCRIPTION

When all inputs are low, the output is a high. When at least one input is a high, the output is a low.

This card contains three circuits, each containing three, three, and two inputs, respectively.

ELECTRICAL DESCRIPTION

This circuit operates with input pulses that have positive excursions between 0.0 vdc and -0.5 vdc, and negative excursions between -3.6 vdc and -5.4 vdc. The excursions of the output voltage pulses, are the same as those given for the input pulses.

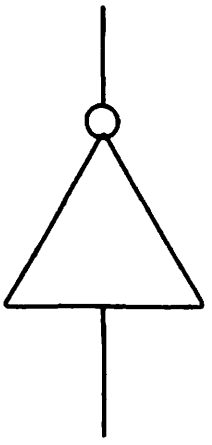
The maximum input current required is 5.8 ma. The circuit can drive five AND-OR's or six AND's.

This circuit's maximum speed is such that the second of two series-connected circuits produces a usable output before the clock phase input to the first has expired. A normal clock phase is 166 nanoseconds long.

LOGIC			
INPUT		OUTPUT	
HIGH	0.0 Volt	HIGH	0.0 Volt
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER				
PIN	1	2	3	4
VOLTAGE	Grd	+15	-15	-4.5

Figure 6-15. Inverter, Module 7002060



LOGIC SYMBOL

LOGIC DESCRIPTION

A low input produces a high output. A high input produces a low output.

The module contains a total of five independent inverter circuits.

ELECTRICAL DESCRIPTION

This circuit operates with input pulses that have positive excursions between 0.0 vdc and -0.5 vdc, and negative excursions between -3.6 vdc and -5.4 vdc. The excursions of the output voltage pulses are equal and opposite to those given for the input pulses.

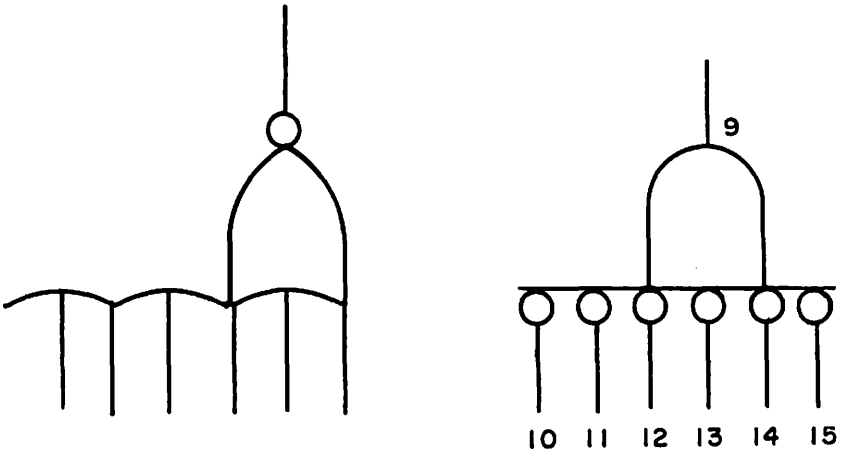
The maximum input current required is 5.8 ma. The circuit can drive five AND-OR's or six AND's.

This circuit's maximum speed is such that the second of two series-connected circuits produces a usable output before the clock phase input to the first has expired. A normal clock phase is 166 nanoseconds long.

LOGIC			
INPUT		OUTPUT	
HIGH	0.0 Volt	HIGH	0.0 Volt
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER				
PIN	1	2	3	4
VOLTAGE	Grd	+15	-15	-4.5

Figure 6-16. Inverter, Module 7002070



LOGIC SYMBOLS

LOGIC DESCRIPTION

When all used inputs are low, the output is a high. When at least one input is high, the output is low.

ELECTRICAL DESCRIPTION

This circuit operates with input pulses that have positive excursions to a level between 0.0 vdc and -0.5 vdc, and negative excursions to a level between -3.0 vdc and -5.0 vdc. The excursions of the output voltage pulses are the same as those given for the input pulses.

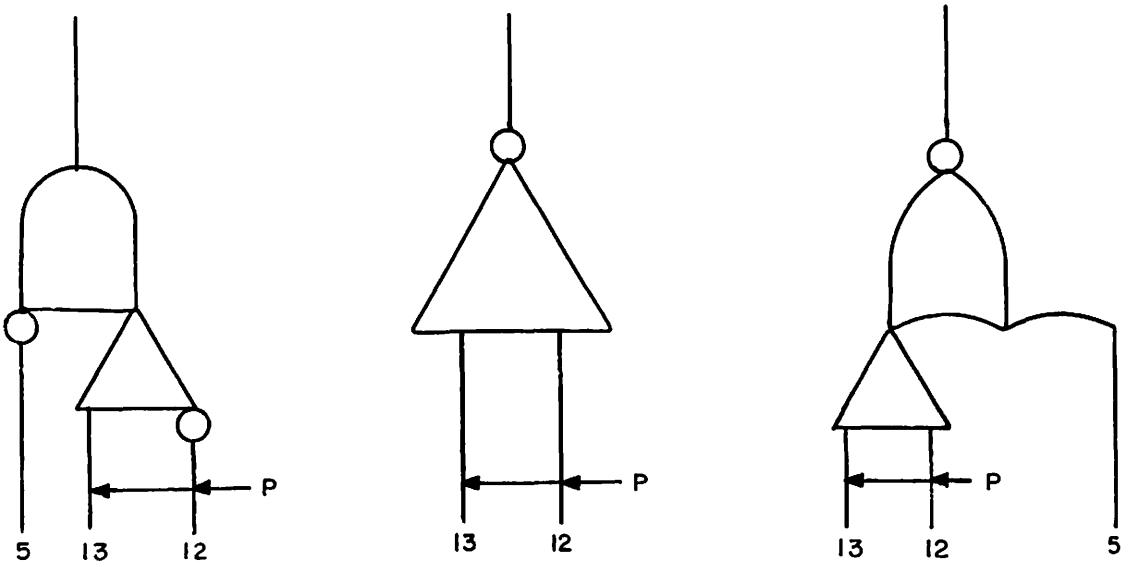
The maximum input current required is 5.8 ma. The circuit can drive five AND-OR's or six AND's.

This circuit's maximum speed is such that the second of two series-connected circuits produces a usable output before the clock phase input to the first has expired. A normal clock phase is 166 nanoseconds long.

LOGIC			
INPUT		OUTPUT	
HIGH	0.0 Volt	HIGH	0.0 Volt
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS				
PIN	1	2	3	4
VOLTAGE	Grd	+15	-15	-4.5

Figure 6-17. Inverter, Module 7002080



LOGIC SYMBOLS

LOGIC DESCRIPTION

When the input to pin 12 is -15 v, and the input to pin 5 is a low, the output is a high. When the input to pin 12 is 0 v and the input to pin 5 is a low, the output is a low. When the input to pin 5 is a high, the output is a low, regardless of the other input. Pin 13 is the grounded return of the twisted pair.

ELECTRICAL DESCRIPTION

This circuit operates with input pulses that have positive excursions between 0.0 vdc and -0.5 vdc, and negative excursions between -13.5 vdc and -16.5 vdc. The gating input-pulses (pin 5) have positive excursions between 0.0 vdc and -0.5 vdc, and negative excursions between -3.6 vdc and -5.4 vdc. The excursions of the output voltage pulses are the same as those given for the gating input-pulses.

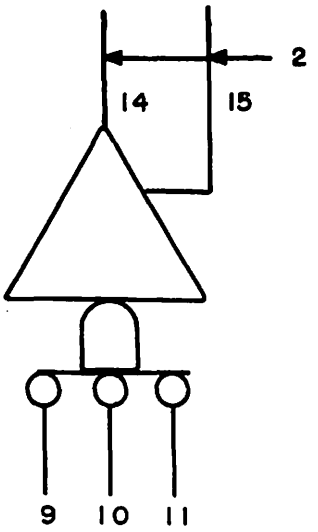
The maximum input current required is 3.7 ma. The circuit can drive two AND-OR's or two AND's.

This circuit is primarily used for interface between equipment.

The circuit delay is 1 to 2.2 microseconds.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	-15 Volts	HIGH	0.0 Volt	VOLTAGE	Grd	+15	-15	-4.5
LOW	0.0 Volt	LOW	-4.5 Volts					

Figure 6-18. Inverter Amplifier, Module 7002090



LOGIC SYMBOL

LOGIC DESCRIPTION

With at least one high input on an input line, the output on pin 14 is -13.5 v. When all the input lines have a low input present, the output on pin 14 is 0 v. Pin 15 is the grounded return of the twisted pair.

ELECTRICAL DESCRIPTION

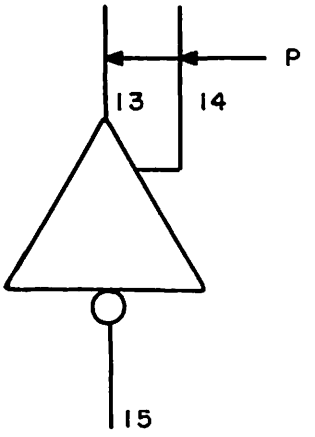
This circuit operates with input pulses that have positive excursions between 0.0 vdc and -0.5 vdc, and negative excursions between -3.6 vdc and -5.4 vdc. The output pulses have positive excursions between 0.0 vdc and -0.7 vdc, and negative excursions between -11.0 vdc and -15.0 vdc.

The maximum input current required is 2.0 ma.

Both the rise and fall times are controlled so that the greatest change is 5 v/microsecond.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volt	HIGH	0.00 Volt	VOLTAGE	Grd	+15	-15	-4.5
LOW	-4.5 Volts	LOW	-13.5 Volts					

Figure 6-19. Slow-Interface Amplifier-Driver, Module 7002130



LOGIC SYMBOL

LOGIC DESCRIPTION

When the input is a low, the output at pin 13 is 0 v. When the input is a high, the output at pin 13 is -13.5 v. Pin 14 is the grounded return of the twisted pair.

ELECTRICAL DESCRIPTION

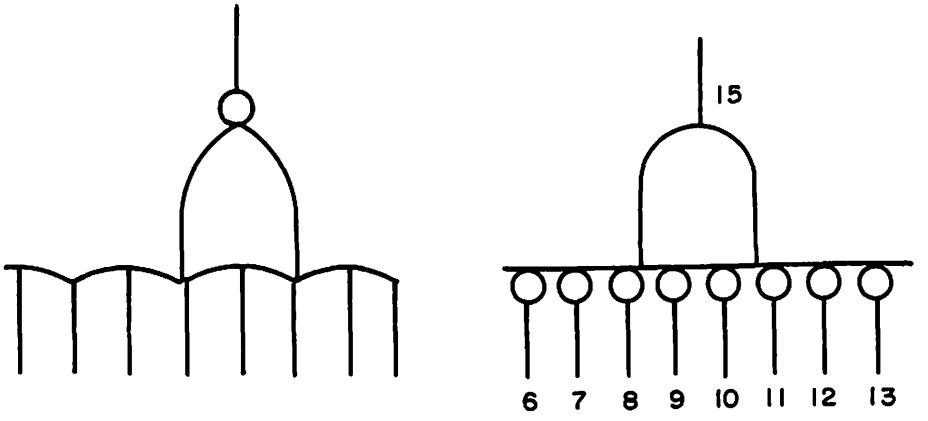
This circuit operates with input pulses that have positive excursions between 0.0 vdc and -1.5 vdc, and negative excursions between -3.6 vdc and -5.4 vdc. The output pulses have positive excursions between 0.0 vdc and -0.5 vdc, and negative excursions between -10.0 vdc and -17.0 vdc.

The maximum input current required is 2.25 ma.

The rise and fall times are controlled to be less than 5 v/microsecond. The circuit can drive four twisted-pair cables up to 300 feet in length.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volt	HIGH	0.0 Volt	VOLTAGE	Grd	+15	-15	-4.5
LOW	-4.5 Volts	LOW	-13.5 Volts					

Figure 6-20. Slow-Interface Amplifier-Driver, Module 7002140, 7002141



LOGIC SYMBOLS

LOGIC DESCRIPTION

When all used inputs are low, the output is high. When one (or more) input is high, the output is low.

ELECTRICAL DESCRIPTION

This circuit operates with input pulses that have positive excursions to a level between 0.0 vdc and -0.5 vdc, and negative excursions to a level between -3.8 vdc and -5.0 vdc. The excursions of the output voltage pulses are the same as those given for the input pulses.

The maximum input current required is 5.8 ma.

This circuit's maximum speed is such that the second of two series-connected circuits produces a usable output before the clock phase input to the first has expired. A normal clock phase is 166 nanoseconds long.

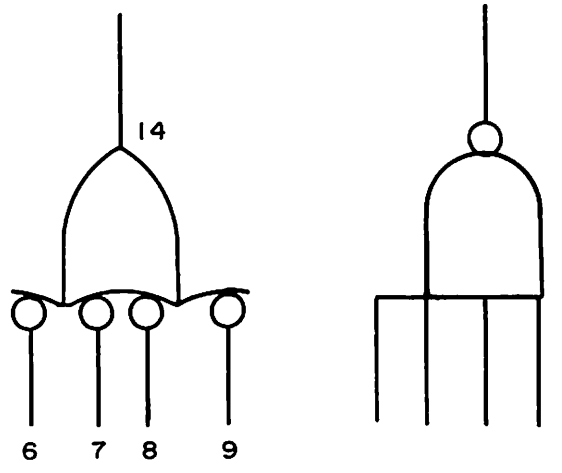
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volt	HIGH	0.0 Volt
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Grd	+15	-15	-4.5

Figure 6-21. Inverter, Module 7002160



LOGIC SYMBOLS

LOGIC DESCRIPTION

When any input is a low, the output is a high. When all inputs are high, the output is low.

ELECTRICAL DESCRIPTION

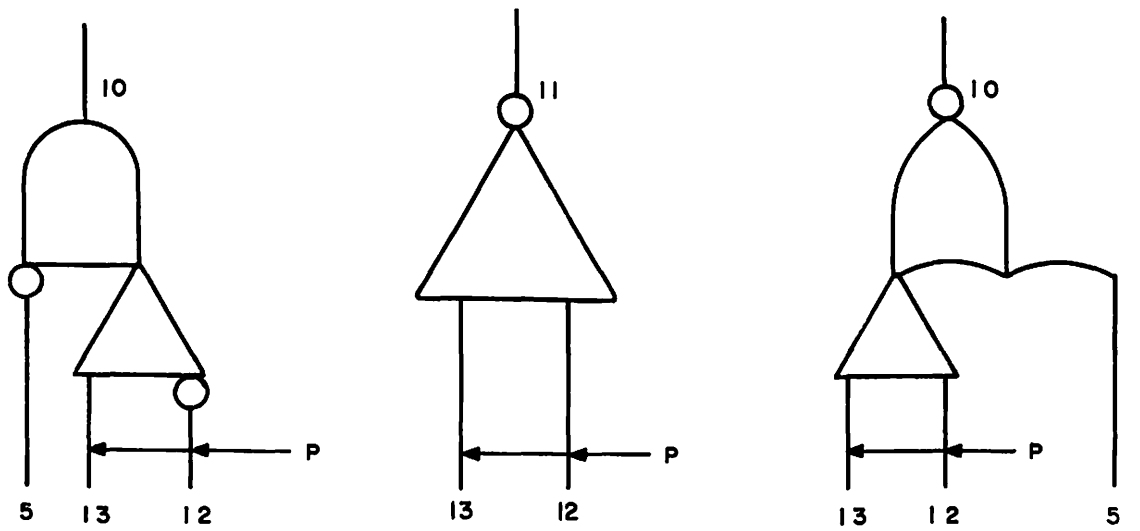
This circuit operates with input pulses that have positive excursions between 0.0 vdc and -0.5 vdc, and negative excursions between -3.6 vdc and -5.4 vdc. The excursions of the output voltage pulses are the same as those given for the input pulses.

The maximum input current required is 7.0 ma. The circuit can drive six AND's or five AND-OR's.

This circuit's maximum speed is such that the second of two series-connected circuits produces a usable output before the clock phase input to the first has expired. A normal clock phase is 166 nanoseconds long.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volt	HIGH	0.0 Volt	VOLTAGE	Grd	+15	-15	-4.5
LOW	-4.5 Volts	LOW	-4.5 Volts					

Figure 6-22. Inverter, Module 7002220



LOGIC SYMBOLS

LOGIC DESCRIPTION

When the input to pin 12 is a low and the input to pin 5 is a low, the output is a high. When the input to pin 12 is a high and the input to pin 5 is a low, the output is a low.

When the input to pin 5 is a high (disable), the output is a low, regardless of the other input. Pin 13 is the return of the twisted pair.

ELECTRICAL DESCRIPTION

The circuit operates with input signals that have positive excursions between 0.0 vdc to -0.5 vdc and negative excursions between -3.0 vdc and -4.5 vdc.

The output signal has a positive excursion between 0.0 vdc and -0.4 vdc and negative excursion between -3.8 vdc and -5.2 vdc. The required gate signal is the same as the output signal. A gate signal between 0.0 vdc and -0.4 vdc holds the output negative. The circuit may be used with the gate open if desired.

The maximum circuit delay and storage is 200 nanoseconds. The maximum input current required is 1.1 ma.

The circuit has high common-mode noise-rejection when used with a twisted pair cable. The input impedance is balanced so noise coupled in one conductor will also be coupled into the other conductor.

The threshold level, voltage difference between input conductors, is between -1.1 vdc and -1.9 vdc.

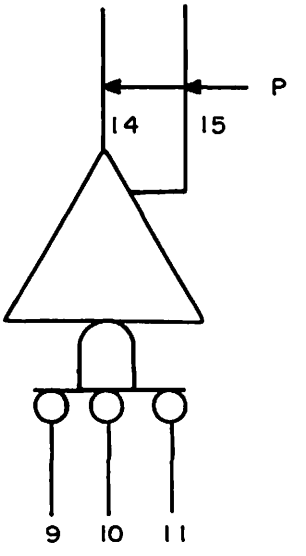
LOGIC

INPUT		OUTPUT	
HIGH	-0.0 Volt	HIGH	0.0 Volt
LOW	-3.0 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Grd	+15	-15	-4.5

Figure 6-23. Fast-Interface Inverter-Amplifier, Module 7002320, 7002321



LOGIC SYMBOL

LOGIC DESCRIPTION

When all the input lines have a low input present, the output on pin 14 will be high. With at least one high input on an input line, the output on pin 14 will be low. Pin 15 is the grounded return of the twisted pair.

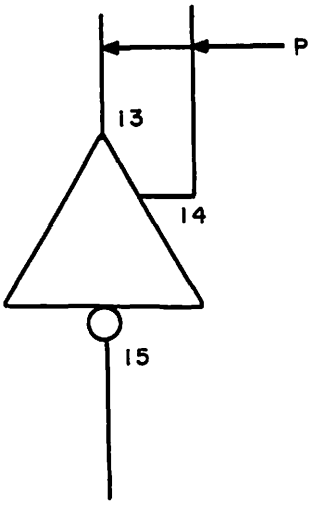
ELECTRICAL DESCRIPTION

This circuit contains high impedance features with power off and a negative voltage applied from a remote source through the cable into pin 14. The circuit will have an impedance not less than 100,000 ohms.

LOGIC			
INPUT		OUTPUT	
HIGH	0.0 Volt	HIGH	0.0 Volt
LOW	-4.5 Volts	LOW	-3.0 Volts

POWER REQUIREMENTS				
PIN	1	2	3	4
VOLTAGE	Grd	+15	-15	-4.5

Figure 6-24. Fast-Interface Amplifier-Driver, Module 7002330, 7002332



LOGIC SYMBOL

LOGIC DESCRIPTION

When input pin 15 is low, output pin 13 is high. When the input pin 15 is high, the output is low.

ELECTRICAL DESCRIPTION

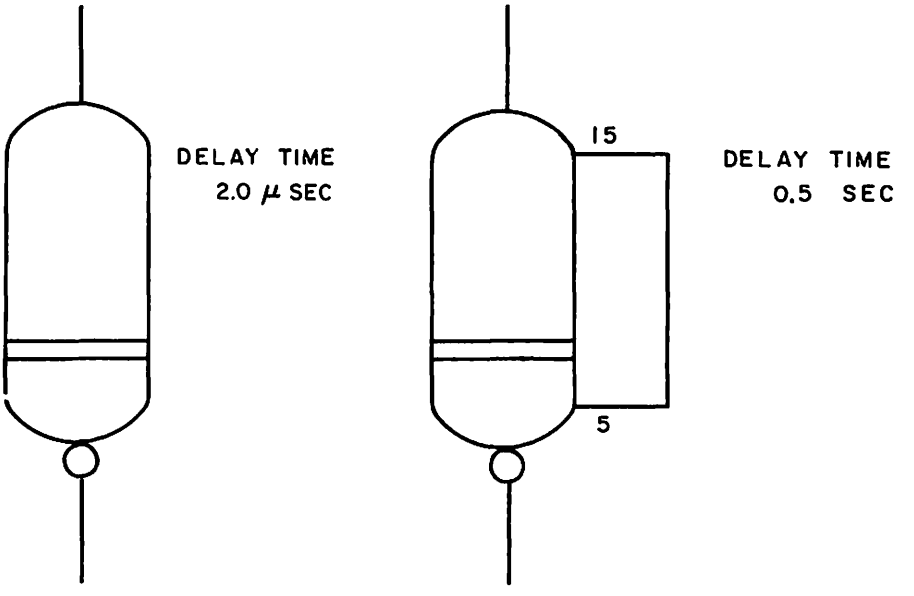
This circuit operates with inputs of -0.3 vdc and -4.5 vdc. The outputs are nominally 0.0 vdc and -4.5 vdc. The maximum input current required is 4.6 ma at 0.0 vdc input.

This circuit has a maximum turn on/ turn off time of 200 nanoseconds and can drive four input amplifier circuits through 150 feet of cable each.

LOGIC			
INPUT		OUTPUT	
HIGH	0.0 Volt	HIGH	0.0 Volt
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS				
PIN	1	2	3	4
VOLTAGE	Grd	+15	-15	-4.5

Figure 6-25. Fast-Interface Amplifier-Driver, Module 7002340, 7002342



LOGIC SYMBOLS

LOGIC DESCRIPTION

When the circuit is quiescent, the input pin is a high, and the output pin is a low. When a low is applied to the input pin, the time constant of the input circuit allows the output pin to remain low for the charging duration. When the charging operation is completed the output pin goes high and remains high until the input pin returns to a high. The output pin then returns to a low.

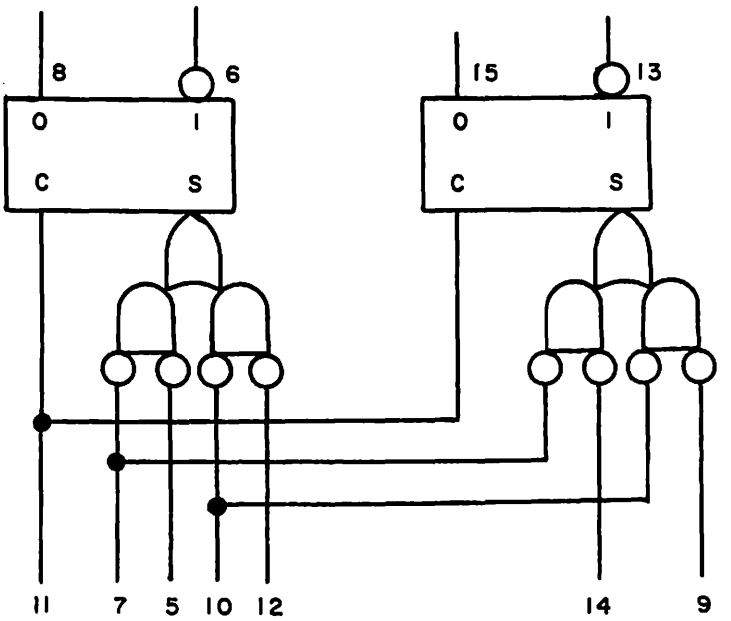
ELECTRICAL DESCRIPTION

This circuit operates with input pulses that have positive excursions between 0.0 vdc and -0.4 vdc, and negative excursions between -3.8 vdc and -5.2 vdc. The excursions of the output voltage pulses are the same as those given for the input pulses.

The maximum input current required is 7.0 ma. The circuit can drive one AND or one AND-OR.

LOGIC				ELECTRICAL DESCRIPTION				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volt	HIGH	0.0 Volt	VOLTAGE	Grd	+15	-15	-4.5
LOW	-4.5 Volts	LOW	-4.5 Volts					

Figure 6-26. Time Delay, Module 7002830



LOGIC SYMBOL

LOGIC DESCRIPTION

When both inputs to either set gate are low, the flip-flop sets. The output on the set side (pins 6 and 13) goes to a low and the output on the clear side (pins 8 and 15) goes to a high. The normal input on pin 11 is a low. When the input on pin 11 goes to a high, the flip-flop clears, if set. The output on the set side goes to a high and on the clear side, to a low.

ELECTRICAL DESCRIPTION

This assembly consists of two flip-flop circuits each having two 2 input AND-OR gates and one OR gate shared with an input pin and the other side of the flip-flop. The nominal positive excursion of the input pulse is 0 vdc. The nominal negative excursion of the input pulse is -4.5 vdc. The positive and negative excursions of the output signal are the same as those for the input pulse.

The maximum current required at input pins 5, 9, 12, and 14 is 6.85 ma and at input pins 7, 10, and 11 is 13.7 ma with the input at 0 v. Each output pin is capable of driving five AND or four AND-OR logic circuits.

The maximum turnon and turnoff time for each logic circuit is 50 and 60 nanoseconds respectively.

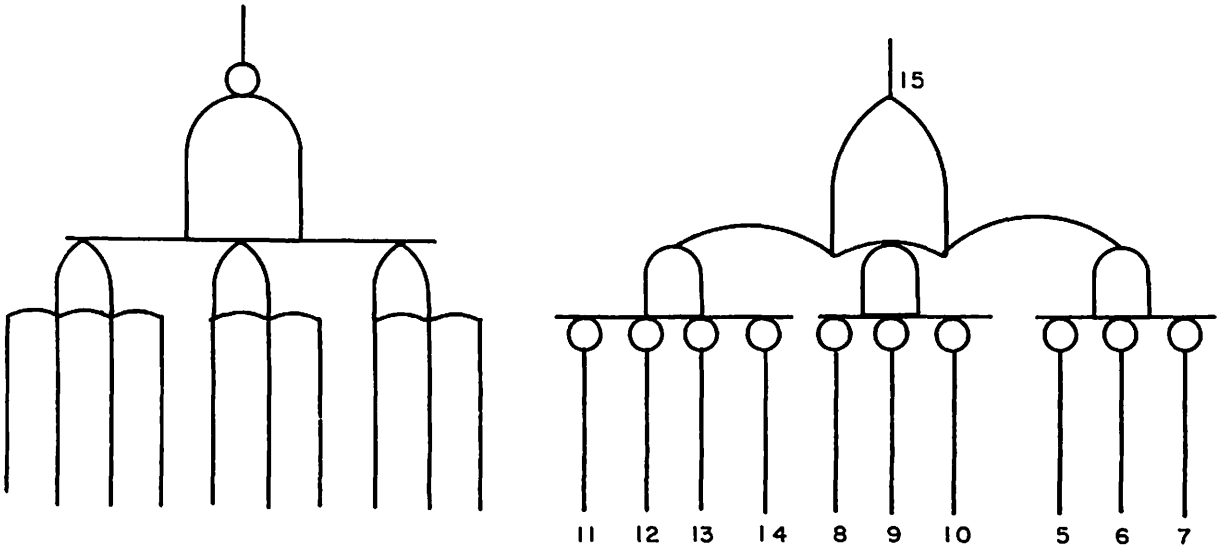
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volt	HIGH	0.0 Volt
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Grd	+15	-15	-4.5

Figure 6-27. Flip-Flop, Module 7002900



LOGIC SYMBOLS

LOGIC DESCRIPTION

When all inputs to any one of the AND circuits are low, the output of the circuit is a high. Conversely, the circuit produces a low when a high input is present on at least one input to all AND circuits.

ELECTRICAL DESCRIPTION

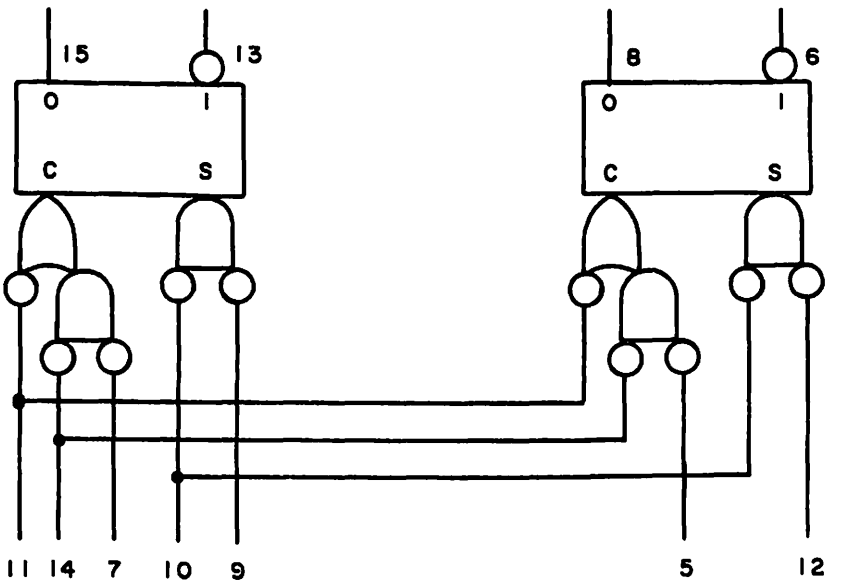
This assembly consists of a logic inverter having three input OR gates. Two of the three OR gates have 3 AND inputs and the other has a 4 AND input. This circuit operates with input pulses that have nominal positive excursions of -0.3 vdc and nominal negative excursions of -4.5 vdc. The excursions of the output signal are the same as those given for the input pulses.

The maximum input current required is 7.1 ma at 0 vdc input. The circuit can drive five AND/OR's or six AND's.

The maximum turn-on and turn-off time is 50 and 60 nanoseconds respectively.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volt	HIGH	0.0 Volt	VOLTAGE	Grd	+15	-15	-4.5
LOW	-4.5 Volts	LOW	-4.5 Volts					

Figure 6-28. Inverter, Module 7002920



LOGIC SYMBOL

LOGIC DESCRIPTION

In the set condition, the output at pins 13 and 6 is low; the output at pins 15 and 8 is high. In order to set the flip-flop, pins 9 and 10 or 9 and 12 must have a low input. In the clear condition, the output at pins 15 and 8 is low. In order to clear the flip-flop, pins 14 and 7 or 14 and 5 must have a low input. A low input to pin 11 will also clear both flip-flops.

ELECTRICAL DESCRIPTION

This assembly consists of two logic flip-flop circuits. One side of each flip-flop is a two-input AND gate; the other side is an OR gate having a two-input AND gate and a single-input AND gate. One input pin of each AND gate is common input to both flip-flop circuits. The circuit operates with a nominal positive excursion of 0 vdc and a nominal negative excursion of -4.5 vdc. The excursions of the output signals are the same as the input signals.

The maximum current required for a single input pin is 7.1 ma or 14.2 ma for a common input pin at 0 vdc input. Each output is capable of driving four AND logic circuits plus an indicator driver, or four AND-OR logic circuits plus an indicator driver.

The maximum turn-on and turn-off times per logic circuit are 50 and 60 nanoseconds respectively.

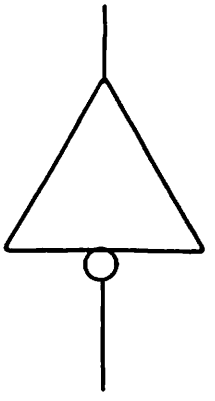
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volt	HIGH	0.0 Volt
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Grd	+15	-15	-4.5

Figure 6-29. Flip-Flop, Module 7002930



LOGIC SYMBOL

LOGIC DESCRIPTION

When the input is a low, the output is a high (Ground). When the input is a high, the output is a low.

ELECTRICAL DESCRIPTION

The circuit operates with input pulses that have positive excursions between 0.0 vdc and -0.5 vdc, and negative excursions between -3.6 vdc and -5.4 vdc. The circuit requires an input current of one milliampere. The current handling capability of the output stage is 180 milliamperes at -24 vdc.

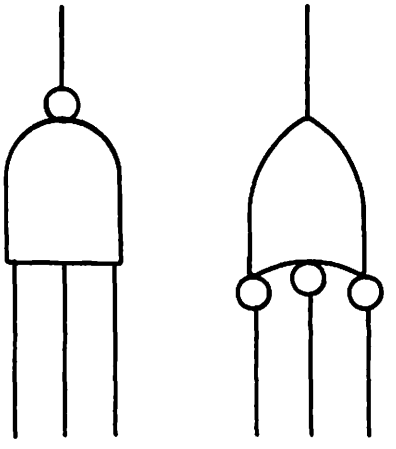
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volt	HIGH	Ground
LOW	-4.5 Volts	LOW	Open

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Grd	+15	-15	-4.5

Figure 6-30. Relay Puller, Module 7002940



LOGIC SYMBOLS

LOGIC DESCRIPTION

When all inputs are high, the output is a low. When any one input is a low, the output is a high.

This card contains three circuits each containing three, three, and two inputs, respectively.

ELECTRICAL DESCRIPTION

The circuit consists of two 3-input and one 2-input OR inverter circuits. Each inverter has one output pin.

The circuit operates with input pulses that have nominal positive excursions of -0.3 vdc and nominal negative excursions of -4.5 vdc.

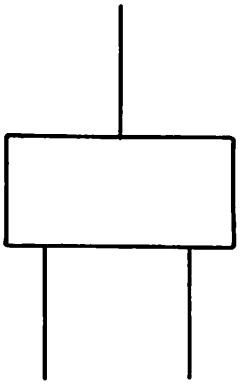
The maximum input current required is 6.85 ma at 0 vdc input.

The maximum turn-on and turn-off time is 50 and 60 nanoseconds respectively.

LOGIC			
INPUT		OUTPUT	
HIGH	0.0 Volt	HIGH	0.0 Volt
LOW	-4.5 Volts	LOW	-4.5 Volts

ELECTRICAL DESCRIPTION				
PIN	1	2	3	4
VOLTAGE	Grd	+15	-15	-4.5

Figure 6-31. Inverter, Module 7002990



ELECTRICAL CONNECTIONS

LOGIC DESCRIPTION

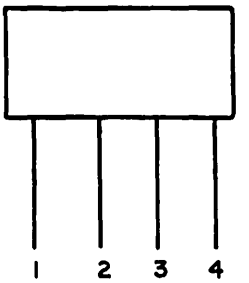
An externally-mounted crystal connects to input pins 9 and 15. The output at pin 5 is a square wave that switches between 0 volt and -4.5 volts.

ELECTRICAL DESCRIPTION

The operating range of this oscillator is determined by the externally-mounted crystal. An emitter-follower isolates the oscillator circuit for the output stage. The square-wave output is clamped at -4.5 volts.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH		HIGH	0.0 Volt	VOLTAGE	Grd	+15	-15	-4.5
LOW		LOW	-4.5 Volts					

Figure 6-32. Amplifier, Crystal Oscillator, Module 7003060



ELECTRICAL CONNECTIONS

LOGIC DESCRIPTION

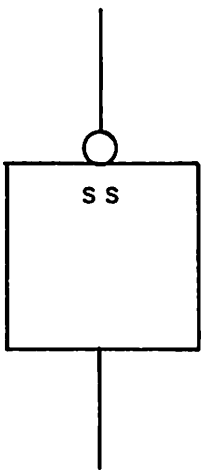
The capacitors on this circuit card connect to the dc voltage buses. The chassis maps show where these circuits are located.

ELECTRICAL DESCRIPTION

(NOT APPLICABLE)

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH		HIGH		VOLTAGE	Grd	+15	-15	-4.5
LOW		LOW						

Figure 6-33. Capacitor Assembly, Module 7003180



LOGIC SYMBOL

LOGIC DESCRIPTION

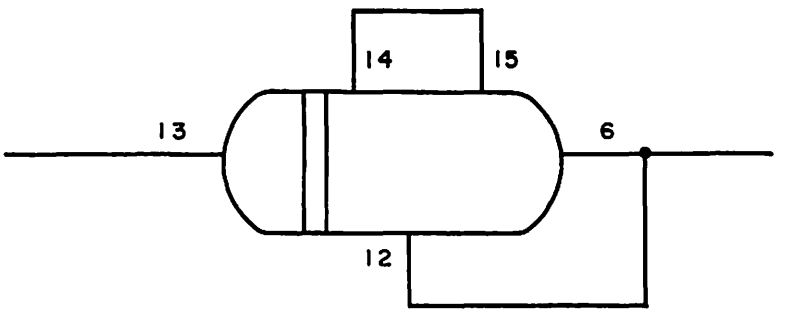
A high at the input pins produces a low pulse at the output pin. The module contains four independent but identical circuits.

ELECTRICAL DESCRIPTION

A 4.5 v positive transition at the input produces a 4.5 v, 300-nanosecond pulse at the output.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volt	HIGH	0.0 Volt	VOLTAGE	Grd	+15	-15	-4.5
LOW	-4.5 Volts	LOW	-4.5 Volts					

Figure 6-34. Amplifier, Driver-Inverter, Module 7003290



LOGIC SYMBOL

LOGIC DESCRIPTION

A high input at pin 13 will produce a high output at pin 6. After the delay time the output at pin 6 will become low again.

ELECTRICAL DESCRIPTION

This time delay operates with input and output pulses that have nominal positive excursions of 0 vdc and nominal negative excursions of -4.5 vdc.

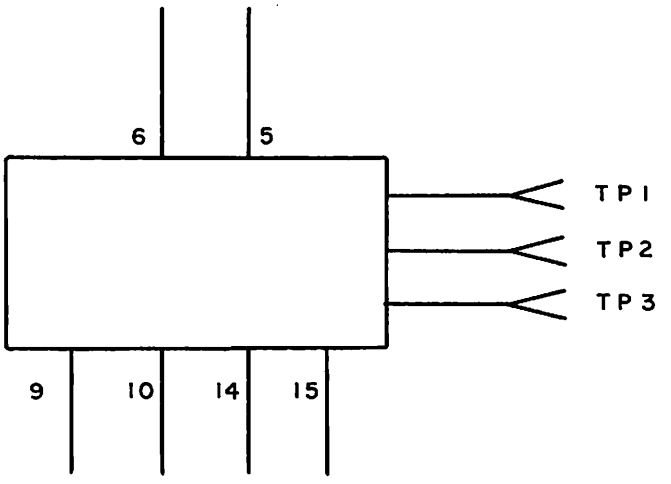
The maximum input current is 5.8 ma at 0 vdc. The output can drive three AND-OR's or three AND circuits.

The delay time may be varied by R7 from 16.5 μsec to 1.2 μsec.

LOGIC			
INPUT		OUTPUT	
HIGH	0.0 Volt	HIGH	0.0 Volt
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS				
PIN	1	2	3	4
VOLTAGE	Grd	+15	-15	-4.5

Figure 6-35. Time Delay, 1.2 to 16.5 MS, Module 7003480



ELECTRICAL CONNECTIONS

LOGIC DESCRIPTION

When input pin 14 is low, input pin 15 will be high. The outputs at this time will be a low at pin 6 and a high at pin 5.

Each succeeding 1 read from tape will reverse the polarity at the inputs and outputs.

ELECTRICAL DESCRIPTION

This amplifier is a balanced, differential input amplifier used to amplify signals received from the read head.

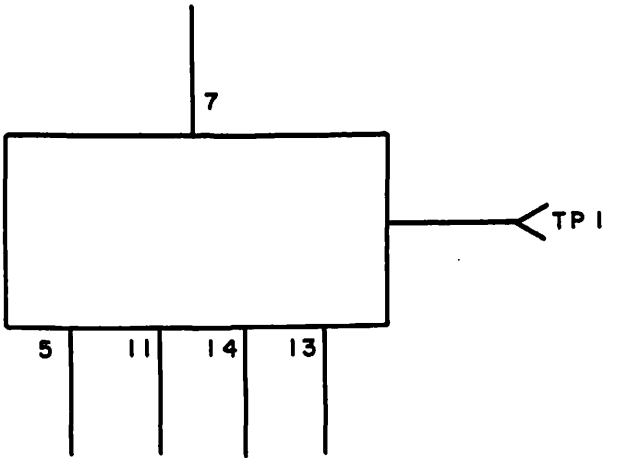
Pins 9 and 10 are regulated power to the circuit.

Pins 14 and 15 sense 25 ±5 mv peak-to-peak received from the read head. This signal is then amplified to approximately 8 volts peak-to-peak. The output will reflect the same polarity as its respective input.

LOGIC			
INPUT		OUTPUT	
25 ±5 MV Peak-To Peak	0	8 Volt Peak-To Peak	0

POWER REQUIREMENTS				
PIN	1	2	3	4
VOLTAGE	Grd	+15	-15	-4.5

Figure 6-36. Amplifier, Differential-Read #2, Module 7003500



ELECTRICAL CONNECTIONS

LOGIC DESCRIPTION

When the input to pins 13 and 14 sense a significant negative voltage and pin 5 is low, the output at pin 7 is a high.

When the input to pin 5 is high, the output will be a constant low regardless of what is at the other inputs.

Pin 11 is the bias input.

ELECTRICAL DESCRIPTION

This circuit operates with input signals that are 8 volts peak-to-peak and the proper bias selected. The bias level (pin 11) is set at either a high, normal, or low level, based on input signal levels.

The required gate signal must be approximately -4.5 volts for this circuit to function.

The output at TP1 will be a differentiated spike whose pulse width depends on signal level and bias level.

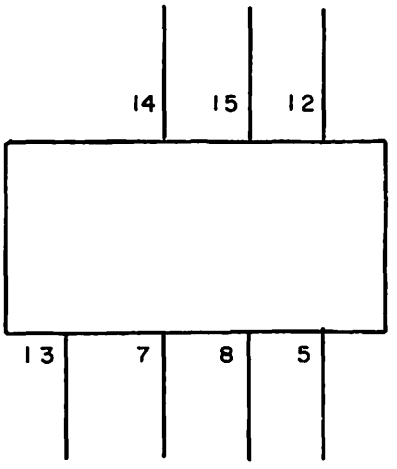
LOGIC

INPUT		OUTPUT	
HIGH	+8 Volts	HIGH	0.0 Volt
LOW	-8 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	9	10
VOLTAGE	Grd	+15	-15	-15R	+15R

Figure 6-37. Amplifier, Detector-Read, Module 7003510



ELECTRICAL CONNECTIONS

LOGIC DESCRIPTION

Pin 13 is internally connected to pin 15.

With a low at input pins 7, 8, and 5, pin 14 is a high impedance and pin 12 is ground.

A high at pins 7, 8, and 5 causes a high impedance at pin 12 and a ground at pin 14.

ELECTRICAL DESCRIPTION

This circuit controls the current applied on the write head. Whenever this current is reversed, it indicates a logic 1 has been written. Conversely, no change in current indicates a logical "0".

The write head is connected to pins 12 and 14, and is center-tapped at pin 15.

This circuit is enabled with -15 volts on input pin 13.

With a low at pins 7, 8, and 5 current flow is between pins 15 and 12 through half of the write head. With a high at pins 7, 8, and 5 current flow is through the other half of the write head between pins 15 and 14.

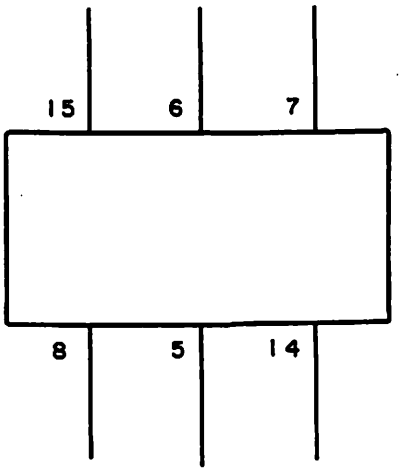
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volt	HIGH	GRD
LOW	-4.5 Volts	LOW	HIGH IMPEDANCE

POWER REQUIREMENTS

PIN	1	2	3	4	9
VOLTAGE	Grd	+15	-15	-4.5	-26.5

Figure 6-38. Amplifier, Driver-Write #2, Module 7003520



LOGIC SYMBOL

LOGIC DESCRIPTION

With +26.5 volts at pin 14 and with various combinations of highs and lows at pins 8 and 5, output pins 15, 6, and 7 will be one of three possible voltage levels.

For analysis see electrical description.

ELECTRICAL DESCRIPTION

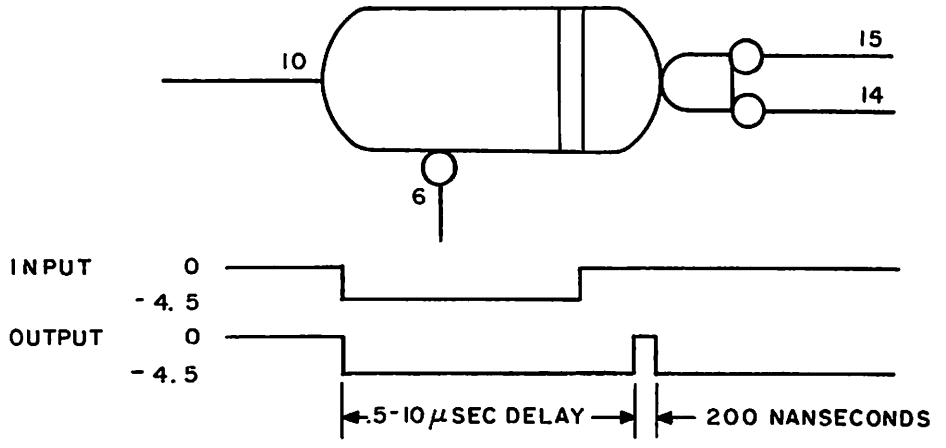
This circuit operates from +26.5 volts and delivers approximately +15.2, +15.8 or +16.0 volts, regulated. With +26.5 volts at pin 14 and -4.5 volts at pins 8 and 5, the output of this circuit is +15.2 volts. With ground at either pin 8 or 5, the output of this circuit will increase to 15.8 or 16.0 volts.

Since pins 8 and 5 are connected to identical circuits the adjustment of potentiometers in either circuit will determine which pin will affect a 15.8-volt output and which pin will affect a 16.0-volt output when -4.5 volts is applied.

With an externally-mounted transistor this circuit may be adapted so as to supply +15 volts regulated.

LOGIC			POWER REQUIREMENTS				
INPUT		OUTPUT	PIN	1	2	3	4
+26.5	-4.5	+15.2 +15.8 +16.0	VOLTAGE	Grd	+15	-15	-4.5

Figure 6-39. Regulator, Voltage-Bias Supply #2, Module 7003530



LOGIC SYMBOL

LOGIC DESCRIPTION

When input pins 14 and 15 are low and pin 6 is low, output pin 10, after a predetermined time, will momentarily go high and then return to a low output.

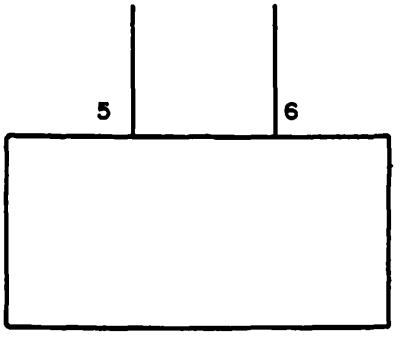
ELECTRICAL DESCRIPTION

This circuit operates with input signals of 0.0 vdc and -4.5 vdc. Pin 6 which is connected to a variable resistance controls the length of the delay and must be low for this circuit to operate properly.

With -4.5 volts at the inputs, and after a delay of approximately 0.5 to 10 msec (adjustable), the output will go to 0.0 volt for 200 nanoseconds and return to -4.5 volts. This -4.5 volt input must be removed during the delay time or the output will remain a constant -4.5 volts.

LOGIC				POWER REQUIREMENTS					
INPUT		OUTPUT		PIN	1	2	3	4	9
HIGH	0.0 Volt	HIGH	0.0 Volt	VOLTAGE	Grd	+15	-15	-4.5	-15 Reg
LOW	-4.5 Volts	LOW	-4.5 Volts						

Figure 6-40. Time Delay - #11, Module 7003540

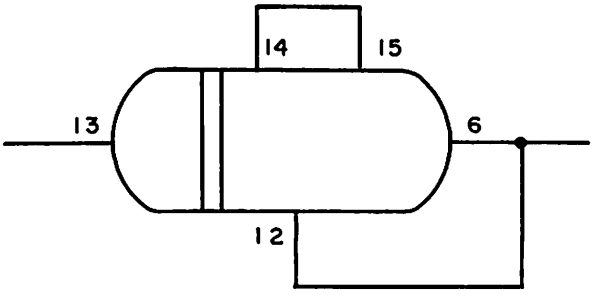


ELECTRICAL CONNECTIONS

LOGIC DESCRIPTION	ELECTRICAL DESCRIPTION
(NOT APPLICABLE)	This module is a 2mc, hermetically-sealed, quartz crystal with a frequency stability of ±.005% at 25°C (77°F).

LOGIC	POWER REQUIREMENTS
(NOT APPLICABLE)	(NOT APPLICABLE)

Figure 6-41. Crystal - 2 MC, Module 7003550



LOGIC SYMBOL

LOGIC DESCRIPTION

A high input at pin 13 will produce a high output at pin 6. After the delay time has elapsed the output at pin 6 will become low again.

ELECTRICAL DESCRIPTION

This delay operates with input and output pulses between 0.0 volt and -4.5 volts.

The maximum input current is 5.8 ma at 0 vdc. The output can drive three AND-OR's or three AND circuits.

The delay time may be varied by R7 from 15 usec to 150 usec.

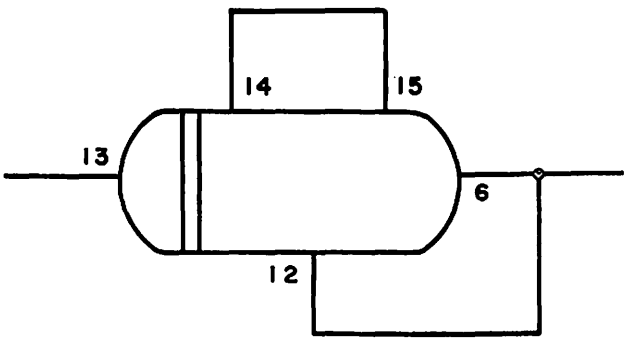
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volt	HIGH	0.0 Volt
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4	9
VOLTAGE	Grd	+15	-15	-4.5	-15 Reg.

Figure 6-42. Time Delay, Module 7003560



LOGIC SYMBOL

LOGIC DESCRIPTION

A high at input pin 13 will result in an immediate high at output pin 6 which will remain for the duration of the time delay and then return to a low.

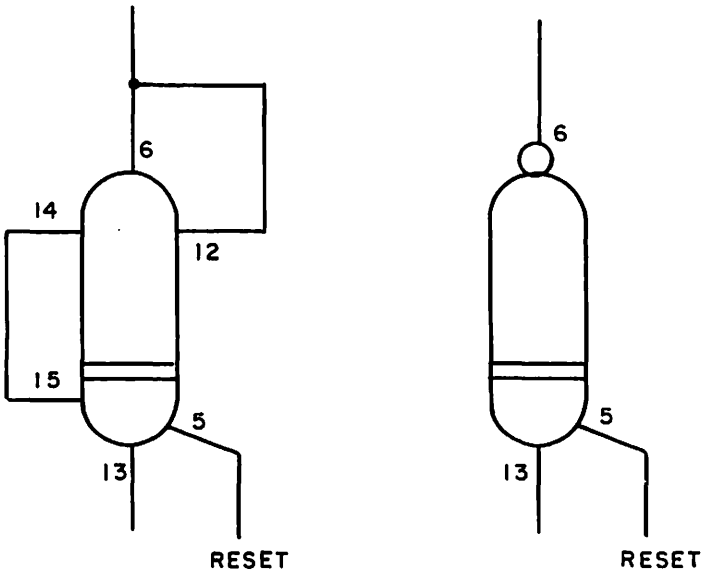
ELECTRICAL DESCRIPTION

This circuit operates with input and output pulses of nominally 0.0 volt and -4.5 volts. Input pulse duration must be greater than 110 nanoseconds, but less than the delay time. The delay time is adjustable from 125 to 1200 usec by R7.

The maximum input current is 5.8 ma at 0.0 vdc. The output can drive three AND-OR's or three AND circuits.

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
HIGH	0.0 Volt	HIGH	0.0 Volt	VOLTAGE	Grd	+15	-15	-4.5
LOW	-4.5 Volts	LOW	-4.5 Volts					

Figure 6-43. Time Delay - 125 to 1200 Microseconds, Module 7003570



LOGIC SYMBOLS

LOGIC DESCRIPTION

A high at the input produces a high at the output at the end of the delay. A high at pin 5 (reset) overrides the delayed output to immediately produce a low at pin 6.

With pins 14 and 15, and pins 6 and 12 connected, a high at the input produces an immediate high at the output. At the end of the delay the output goes low.

ELECTRICAL DESCRIPTION

When the input at pin 13 goes positive, the output at pin 6 remains at -4.5 vdc until after the delay. It then goes positive and remains positive until the input signal drops. 0 vdc at input pin 5 drives the output at pin 6 to -4.5 vdc. Voltage excursion is 0.0 vdc positive and 5.0 vdc negative.

With pins 6 and 12, and 14 and 15 connected, when the input at pin 13 goes positive the output also goes positive. When the delay is complete, the output goes to -4.5 volts. The delay time is variable from 1.5 to 15 usec.

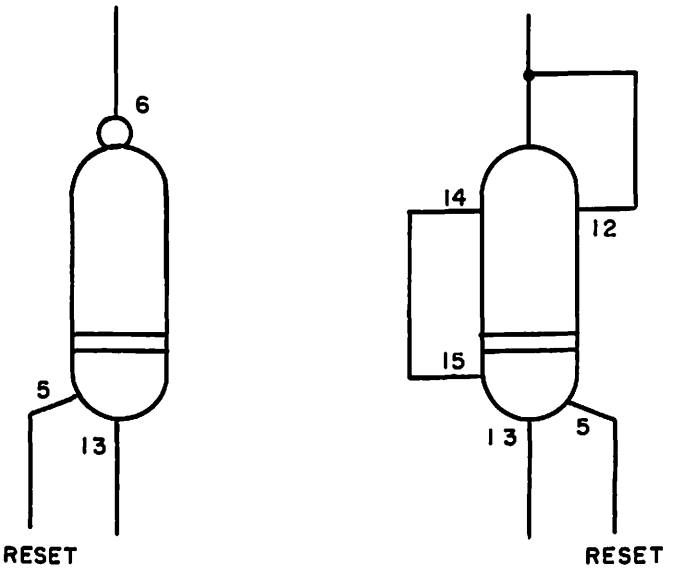
LOGIC

INPUT		OUTPUT	
HIGH	0.0 Volt	HIGH	0.0 Volt
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS

PIN	1	2	3	4
VOLTAGE	Grd	+15	-15	-4.5

Figure 6-44. Time Delay, Module 7003580



LOGIC SYMBOLS

LOGIC DESCRIPTION

A high at the input produces a high at the output at the end of the delay. A high at pin 5 (reset) overrides the delayed output to immediately produce a low at pin 6.

With pins 14 and 15, and pins 6 and 12 connected, a high at the input produces an immediate high at the output. At the end of the delay the output goes low.

ELECTRICAL DESCRIPTION

This circuit operates with input and output pulses that have nominal positive excursions of -0.3 vdc and nominal negative excursions of -4.5 vdc.

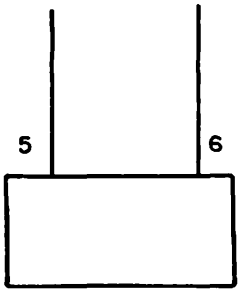
The maximum input current required is 5.8 ma at 0 vdc input. The output from pin 6 can drive three AND or three AND-OR circuits. The output from pin 14 can drive one logic circuit.

The delay time is variable from 13 to 160 usec.

LOGIC			
INPUT		OUTPUT	
HIGH	0.0 Volt	HIGH	0.0 Volt
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS				
PIN	1	2	3	4
VOLTAGE	Grd	+15	-15	-4.5

Figure 6-45. Time Delay, Module 7003590

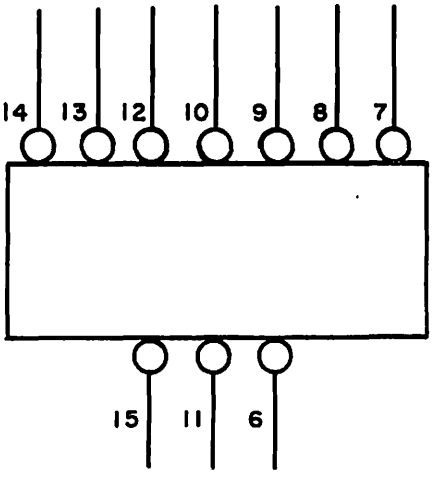


ELECTRICAL CONNECTIONS

LOGIC DESCRIPTION	ELECTRICAL DESCRIPTION
(NOT APPLICABLE)	A 2.88 mc, hermetically-sealed, quartz crystal with a frequency stability of ±.005% at 25°C (77°F).

LOGIC				POWER REQUIREMENTS				
INPUT		OUTPUT		PIN	1	2	3	4
			(NOT APPLICABLE)					

Figure 6-46. Crystal - 2.88 MC, Module 7003790



LOGIC SYMBOL

LOGIC DESCRIPTION

A low at the inputs will result in a low at the outputs (adjustable).

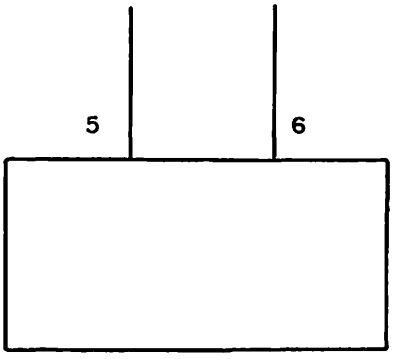
ELECTRICAL DESCRIPTION

This circuit consists of seven individual networks each consisting of a variable resistor in series with a diode.

LOGIC			
INPUT		OUTPUT	
HIGH		HIGH	
LOW	-4.5 Volts	LOW	-4.5 Volts

POWER REQUIREMENTS				
PIN	1	2	3	4
VOLTAGE	Grd	+15	-15	-4.5

Figure 6-47. Resistor and Diode Assembly - #3, Module 7003810

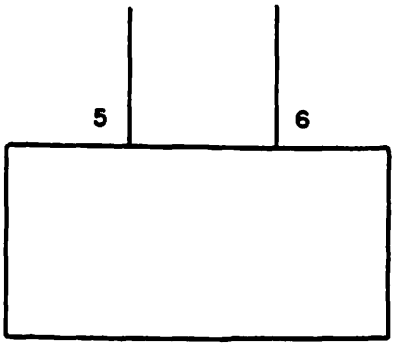


ELECTRICAL CONNECTIONS

LOGIC DESCRIPTION	ELECTRICAL DESCRIPTION
(NOT APPLICABLE)	A 1.6 mc, hermetically-sealed, quartz crystal with a frequency stability of ±.005% at 25°C (77°F).

LOGIC				POWER REQUIREMENTS				
(NOT APPLICABLE)				PIN	1	2	3	4
				VOLTAGE	Grd	+15	-15	-4.5

Figure 6-48. Crystal - 1.6 MC, Module 7104160



ELECTRICAL CONNECTIONS

LOGIC DESCRIPTION	ELECTRICAL DESCRIPTION
(NOT APPLICABLE)	A 2.31 mc, hermetically-sealed, quartz crystal with a frequency stability of ±.005% at 25°C (77°F).

LOGIC			
(NOT APPLICABLE)			

POWER REQUIREMENTS				
PIN	1	2	3	4
VOLTAGE	Grd	+15	-15	-4.5

Figure 6-49. Crystal - 2.31 MC, Module 7104170

SECTION 7

PARTS LIST

7-1. INTRODUCTION.

This Parts List identifies the assemblies and detail parts of the Magnetic Tape Unit. For component parts of the tape transport (22A1A3A1) and the drive electronics (22A1A3A2) in the MTU, refer to the vendor manual "Potter Instrument Handbook S365-84 for MTS-120-X41427 Magnetic Tape System." Reference designations 22A1, 22A2, 22A3, and 22A4 do not appear on the equipment, drawings, or diagrams but they have been added to the Parts List as cabinet area references to clarify the location of assemblies. All other reference designations appearing in the Parts List coincide with the designations marked on the equipment, drawings, and diagrams. Figures 7-1 through 7-8 show various detail parts.

7-2. VARIABLE APPLICATIONS.

Table 7-1 lists the variable applications of the MTU.

7-3. PRINTED CIRCUIT MODULE COMPLEMENT.

Table 7-2 lists all of the printed circuit modules used in the MTU. These modules are nonrepairable items. The last four digits of the Univac part numbers are used on the logic diagrams and the chassis maps as module locating symbols. Column 1 of each table lists, in numerical order, the Univac part numbers assigned to each module. Column 2 gives a short description of each module. Column 3 lists the quantity of modules used in each chassis.

7-4. MAINTENANCE PARTS LIST.

Table 7-3 lists, by assemblies, all of the electrical parts of the MTU. Column 1 of each table lists, in alphanumeric order, the reference designations of the various components followed by a breakdown of the "A" assemblies in alphanumeric order. Column 2 pertains to the vendors' part numbers and codes. Column 3 contains Univac part numbers for each item. Column 4 gives the item names and descriptions. Column 5 keys the component parts and assemblies to the illustrations or photographs in the manual showing their locations.

7-5. LIST OF MANUFACTURERS.

Table 7-4 lists the manufacturers of the parts used. Column 1 gives the vendors' codes as listed in column 2 of table 7-3. Column 2 lists the vendors' names. Column 3 provides the vendors' addresses.

7-6. UNIT VARIABLES.

Variables in the QUANTITY PER CHASSIS column of the Printed Circuit Module Complement List (table 7-2) and PART NUMBER and MANUFACTURER column of the Maintenance Parts List (table 7-3) indicate the variations of assemblies and components in variable units. The absence of a variable code signifies a commom application of parts and assemblies.

TABLE 7-1. MAGNETIC TAPE UNIT, VARIABLE APPLICATIONS

VARIABLE	NO. OF HANDLERS	COOLING	MOUNT	CHARACTERISTIC	INTERFACE	WORD LENGTH (BITS)
1	4 (MT-120)	Water	Shock	Simplex	Slow	30
2	2 (MT-120)	Air	Shock	Duplex	Fast	30
3	2 (MT-120)	Air	Shock	Duplex	Fast	36
4	2 (MT-120)	Air	Shock	Simplex	Fast	36
5	4 (MT-120)	Air	Shock	Simplex	Fast	36
6	4 (MT-120)	Water	Shock	Simplex	Fast	30

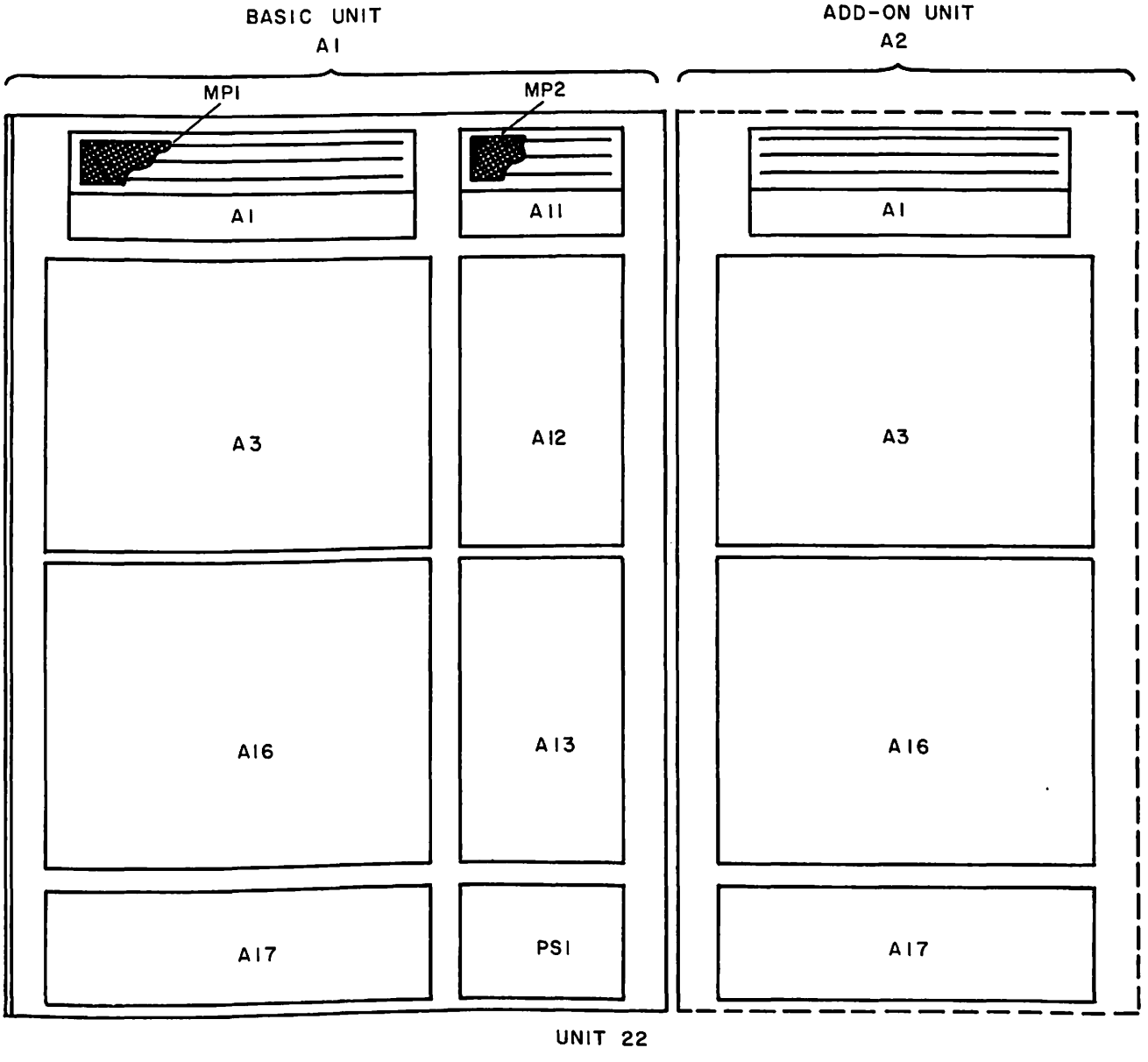


Figure 7-1. Basic and Add-on Magnetic Tape Units, Assembly Location

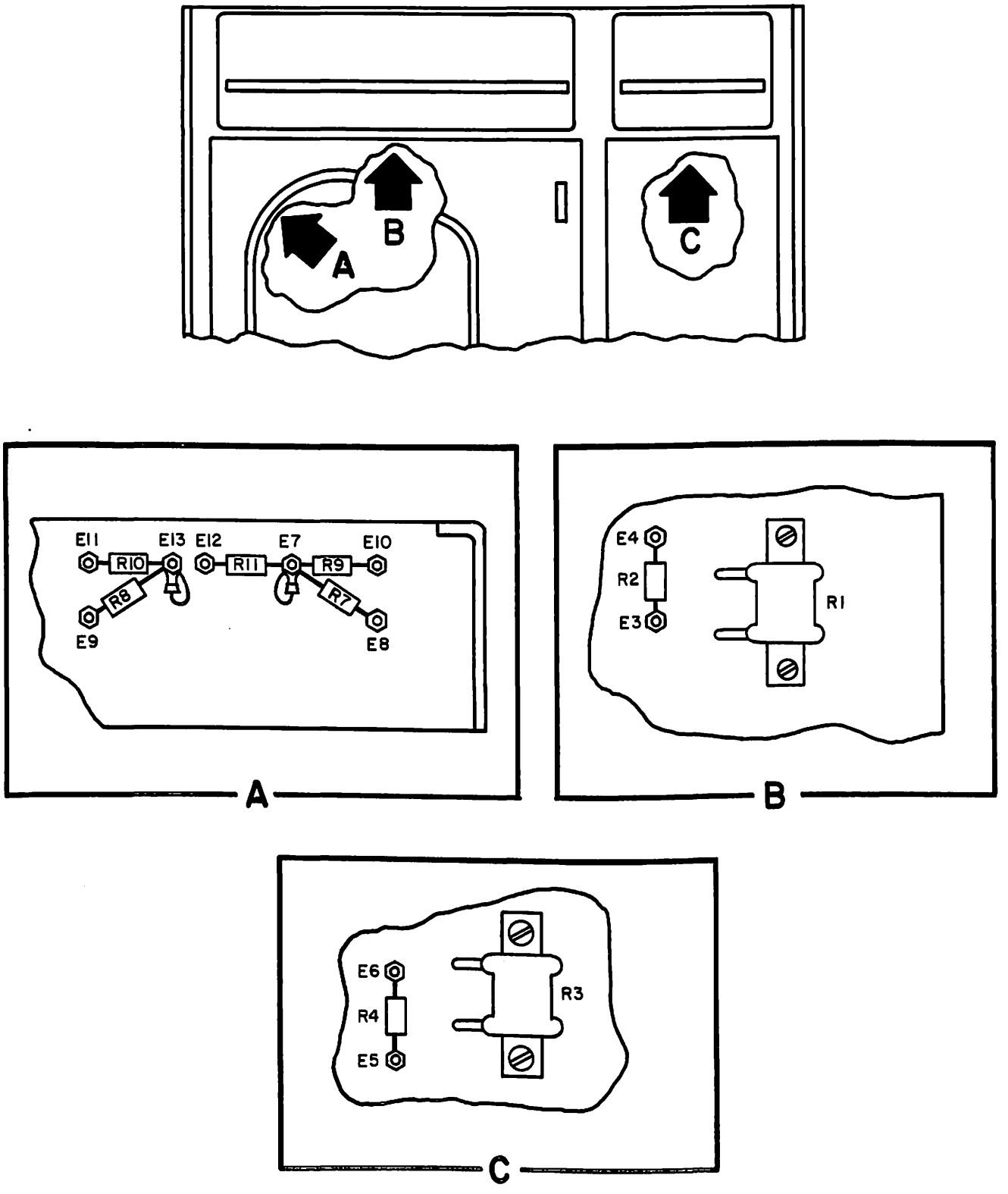


Figure 7-2. Magnetic Tape Unit, Upper Half

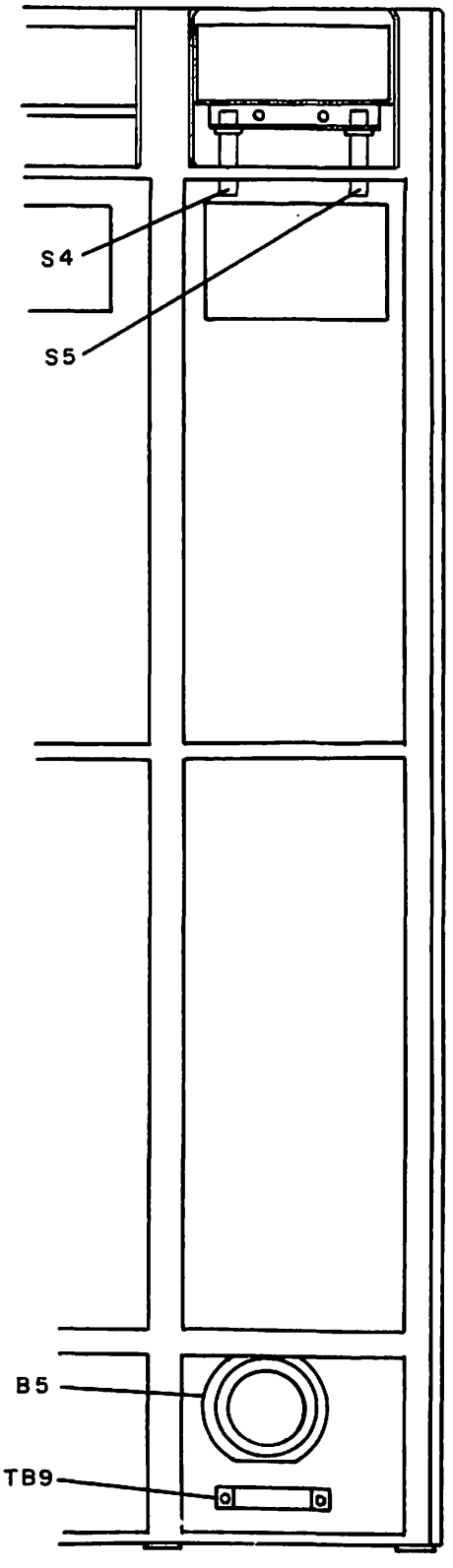


Figure 7-3. Magnetic Tape Control Section, Water Cooled, Interior View

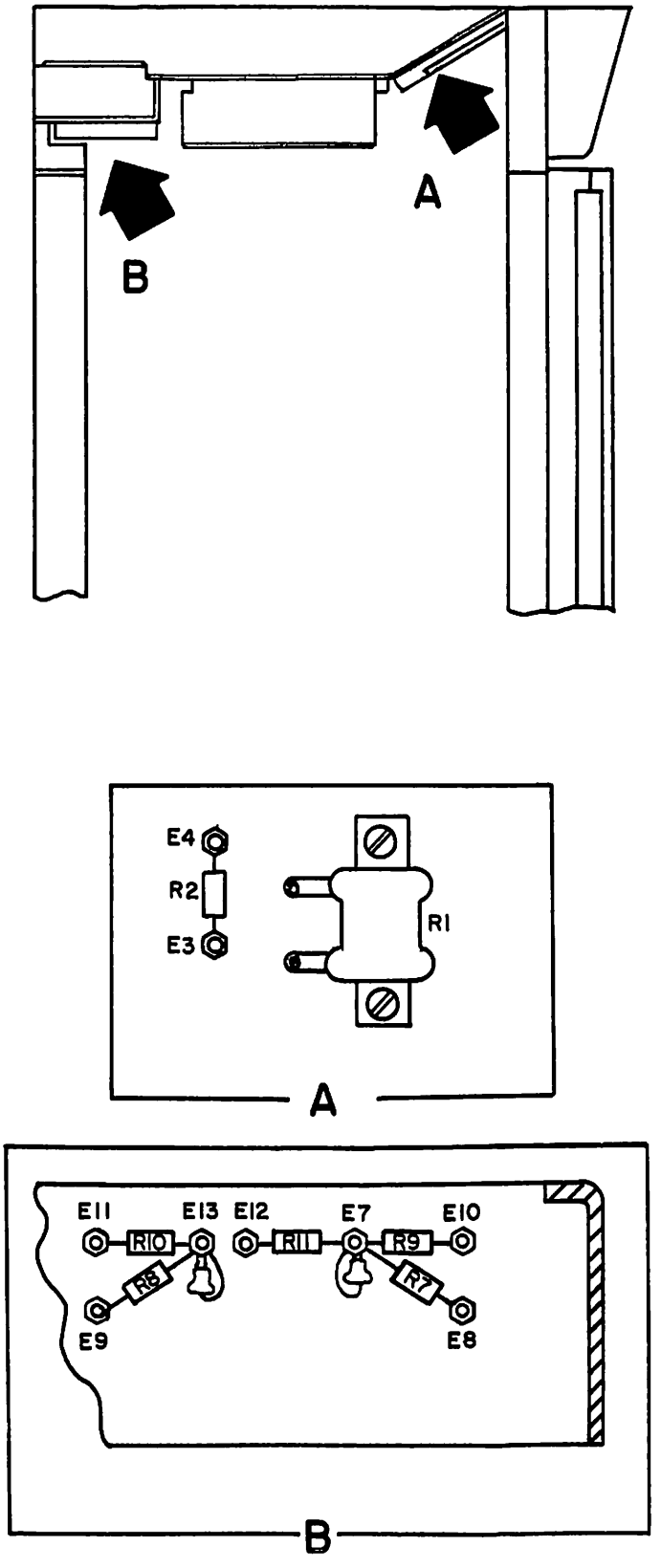


Figure 7-4. Magnetic Tape Unit, Handler Section, Interior Side View

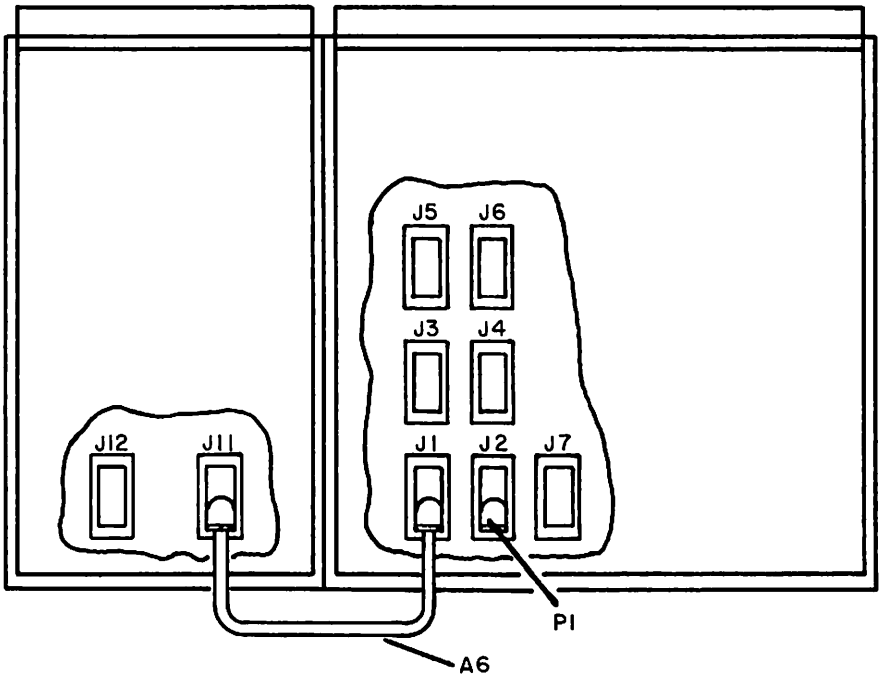


Figure 7-5. Magnetic Tape Unit (A4), Top View

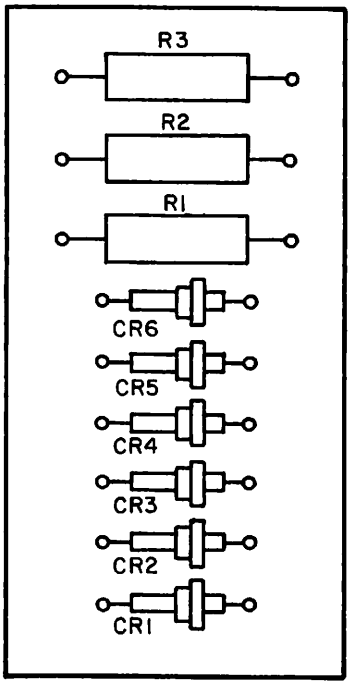
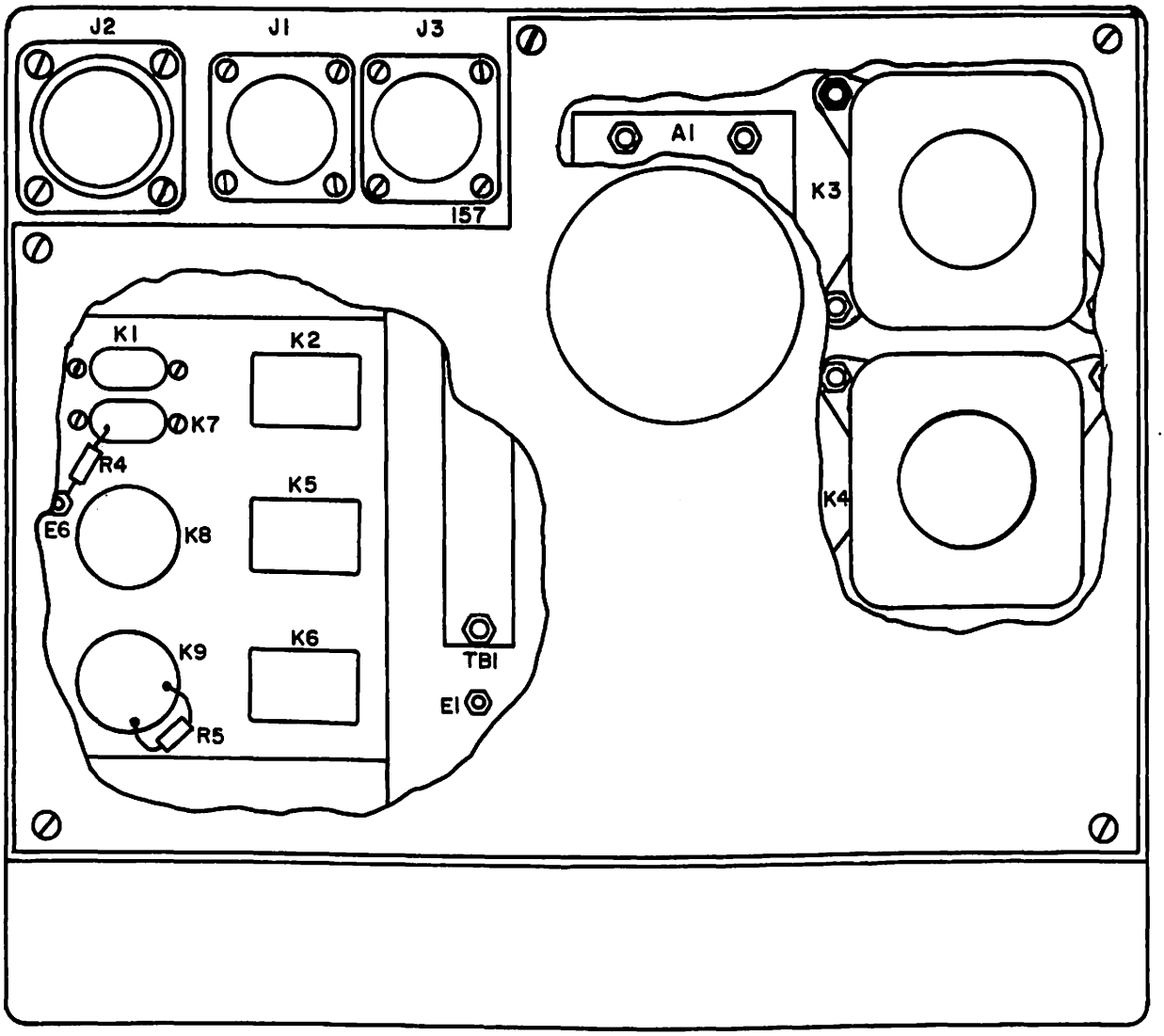
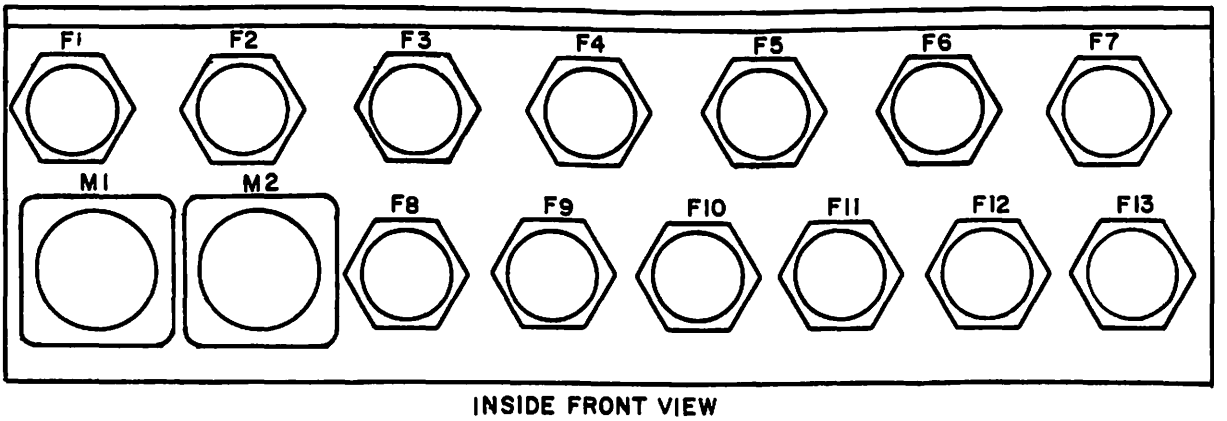


Figure 7-6. Magnetic Tape Unit, Resistor and Diode Assembly



TOP VIEW



INSIDE FRONT VIEW

Figure 7-7. Magnetic Tape Unit Handler, Power Supply Control (A2)

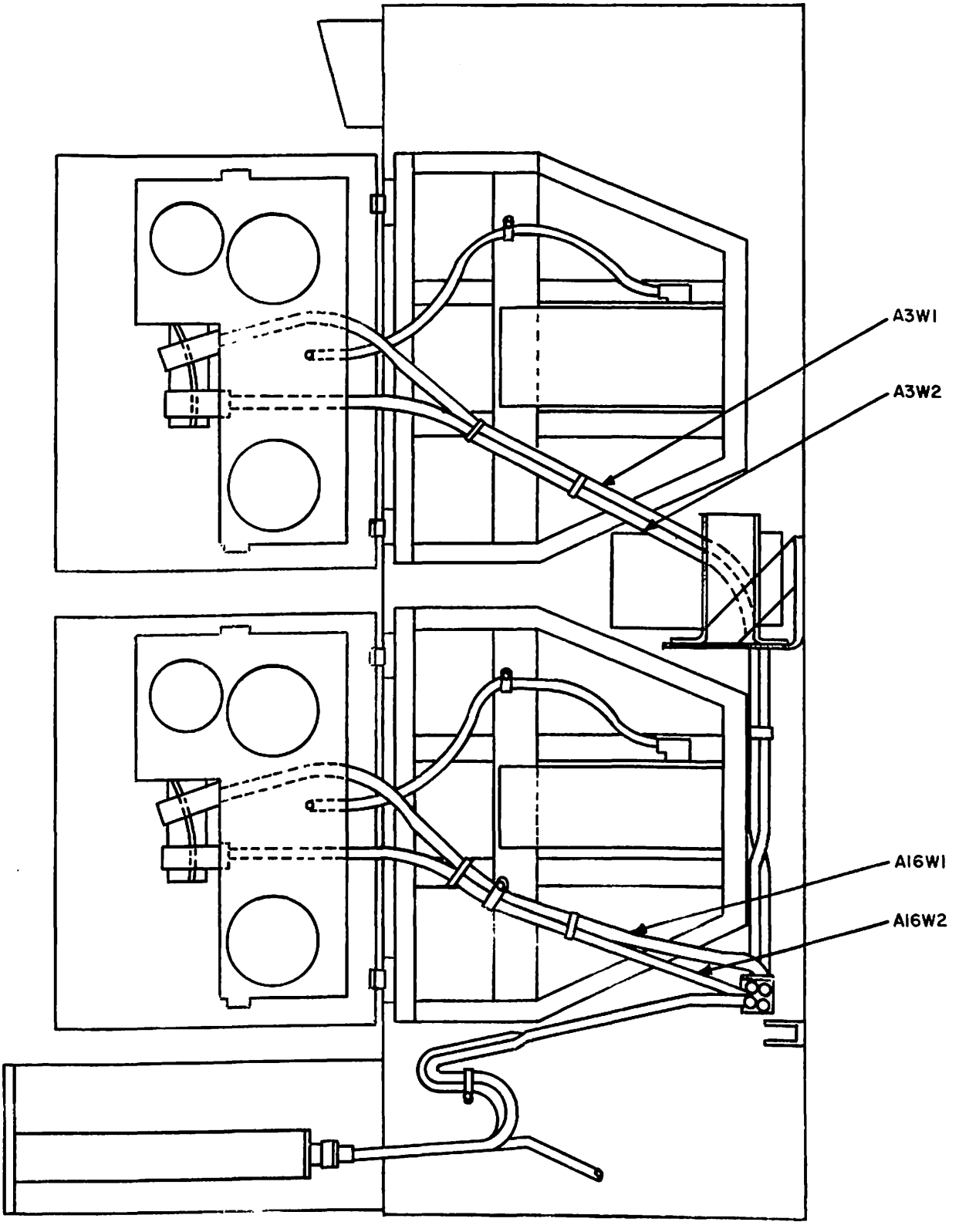


Figure 7-8. Magnetic Tape Unit, Handler Power Supply Cables

TABLE 7-2. MAGNETIC TAPE UNIT, PRINTED CIRCUIT MODULE COMPLEMENT

PART NUMBER	DESCRIPTION	QUANTITY PER CHASSIS										
		A12					A13			A17		
		VAR. 1	VAR. 2	VAR. 3	VAR. 4,5	VAR. 6	VAR. 1,5,6	VAR. 2,3	VAR. 4	VAR. 1-6	VAR. 2,3,4,5	
7000070-00	Inverter						1	1	1			
7000210-00	Oscillator, Pulse Delay	1	1	1	1	1						
7000780-00	Inverter									1	1	
7000850-00	Oscillator, Square Wave						1	1	1			
7001000-00	Capacitor Assembly						1	1	1	4	4	
7001070-00	Amplifier, Control-Write									2	2	
7001090-00	Regulator, Voltage						1	1	1	1	1	
7001170-00	Amplifier, Write Enable						8	4	4	2	2	
7002000-00	Flip-Flop	4	5	5	4	4						
7002013-00	Amplifier, Driver	36	38	38	36	36	23	23	23	7	7	
7002020-00	Flip-Flop	18	24	24	18	18				4	4	
7002030-00	Inverter	8	8	8	8	8						
7002040-00	Inverter	19	19	21	21	19						
7002050-00	Inverter	18	18	18	18	18	13	13	13	4	4	
7002060-00	Inverter	44	45	45	44	44	9	9	9	5	5	
7002070-00	Inverter	30	30	30	30	30	11	11	11	10	10	
7002080-00	Inverter	2	2	2	2	2						

TABLE 7-2. MAGNETIC TAPE UNIT, PRINTED CIRCUIT MODULE COMPLEMENT (CONT.)

PART NUMBER	DESCRIPTION	QUANTITY PER CHASSIS									
		A12					A13			A17	
		VAR. 1	VAR. 2	VAR. 3	VAR. 4,5	VAR. 6	VAR. 1,5,6	VAR. 2,3	VAR. 4	VAR. 1-6	VAR. 2,3,4,5
7002090-00	Inverter	18	1	1	1	1				2	2
7002130-00	Amplifier, Driver	3									
7002141-00	Amplifier, Driver	30									
7002160-00	Inverter	1	1	1	1	1	2	2	2		
7002220-00	Inverter	4	4	4	4	4	1	1	1	2	2
7002320-00	Amplifier, Differential								4		
7002321-00	Amplifier, Differential		33	39	20	17	4	4		1	1
7002332-00	Amplifier, Control Line		6	6	3	3				2	2
7002342-00	Amplifier, Data Line		31	37	36	30					
7002830-00	Inverter	4	4	4	4	4	1	1	1	3	3
7002900-00	Flip-Flop	42	42	48	48	42	11	11	11		
7002920-00	Inverter	2	2	2	2	2				5	5
7002930-00	Flip-Flop	38	38	38	38	38	23	23	23	4	4
7002990-00	Inverter	24	24	24	24	24	7	6	6		
7003060-00	Amplifier-Oscillator	2	2	2	2	2					
7003180-00	Capacitor Assembly	28	28	28	28	28	13	13	13	5	5

TABLE 7-2. MAGNETIC TAPE UNIT, PRINTED CIRCUIT MODULE COMPLEMENT (CONT.)

PART NUMBER	DESCRIPTION	QUANTITY PER CHASSIS									
		A12					A13			A17	
		VAR. 1	VAR. 2	VAR. 3	VAR. 4,5	VAR. 6	VAR. 1,5,6	VAR. 2,3	VAR. 4	VAR. 1-6	VAR. 2,3,4,5
7003290-00	Amplifier, Driver	3	3	3	3	3	3	3	3		
7003480-00	Time Delay	2	2	2	2	2					
7003500-00	Amplifier, Differential									14	14
7003510-00	Amplifier, Detector Read									14	14
7003520-00	Amplifier, Driver									14	14
7003530-00	Regulator, Voltage									3	3
7003540-00	Time Delay	1	1	1	1	1	14	14	14		
7003560-00	Time Delay	1	1	1	1	1					
7003570-00	Time Delay						1	1	1		
7003580-00	Time Delay	1	1	1	1	1	4	4	4	1	1
7003590-00	Time Delay						3	3	3		
7003810-00	Resistor-Diode Assembly						12	6	6		
7104160-00	Crystal Unit, Quartz	1	1	1	1	1					
7104170-00	Crystal Unit, Quartz	1	1	1	1	1					

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22	(VARIABLE 1) (VARIABLE 2) (VARIABLE 3) (VARIABLE 4) (VARIABLE 5) (VARIABLE 6)	7025294-00 7025278-00 7025275-00 7025300-00 7025301-00 7025350-00	RECORDER-REPRODUCER SET, SIGNAL DATA (MAGNETIC TAPE UNIT): UNIVAC 1540; recorder-reproducer is a large capacity, medium speed, magnetic tape storage system. It is capable of receiving data from a computer and recording it on magnetic tape or retrieving information previously recorded on tape and transferring it to a computer. Operating power requirements 115v, 400 cps, three phase	7-1
22A1			CABINET ELECTRICAL EQUIPMENT, BASIC UNIT (For reference only)	7-1
22A1B1	(VARIABLE 1,6) BT2914V-1 92702	909869-00	FAN, VANEAXIAL: 115 vac, 400 cps, 3 phase, 175 cfm; 1 stage, 4.6 in. od, 8 blades, cw rotation; permanent bearings	5-16
22A1B1	(VARIABLE 2,3,4,5) 340ZS-Saucer 82877	906905-00	FAN, TUBEAXIAL: 115 vac, 50/60 cps, single phase 270 cfm rated at free delivery	5-12
22A1B2	(VARIABLE 2,3,4,5)		FAN: Same as 22A1B1 Variable 2,3,4,5	5-12
22A1B3	(VARIABLE 1,6)		FAN: Same as 22A1B1 Variable 1,6	5-16
22A1B3	(VARIABLE 2,3,4,5)		FAN: Same as 22A1B1 Variable 2,3,4,5	5-12
22A1B4	(VARIABLE 2,3,4,5)		FAN: Same as 22A1B1 Variable 2,3,4,5	5-12
22A1B5	(VARIABLE 1,6)		FAN: Same as 22A1B1 Variable 1,6	7-3
22A1B5	(VARIABLE 2,3,4,5)		FAN: Same as 22A1B1 Variable 2,3,4,5	5-12
22A1B6	(VARIABLE 2,3,4,5)		FAN: Same as 22A1B1 Variable 2,3,4,5	5-12

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1C1	(VARIABLE 2,3,4,5) CH53BIMF205K MIL-C-18312	7900081-04	CAPACITOR, FIXED, PAPER DIELECTRIC: 2 uf, ±10 pct, 600 vdc; metal case, hermetically sealed	5-12
22A1C2 thru 22A1C6	(VARIABLE 2,3,4,5)		CAPACITOR: Same as 22A1C1 Variable 2,3,4,5	5-12
22A1E3	3650-2-05 71279	910185-02	TERMINAL, STUD: Insulated, standoff; solder-plated brass term	7-2
22A1E4 thru 22A1E6			TERMINAL: Same as 22A1E3	7-2
22A1E7	3650-1-05 71279	910185-01	TERMINAL, STUD: Insulated, standoff: solder-plated brass term	7-2
22A1E8 thru 22A1E13			TERMINAL: Same as 22A1E7	7-2
22A1MP1	(VARIABLE 1,6) B6-HK&SOC-1-HK 73992	910663-05	COUPLING ASSEMBLY, Quick disconnect: With dust cap	5-16
22A1MP1	(VARIABLE 2,3,4,5)	7006631-01	FILTER, AIR CONDITIONING: A1, RF shielded, oil type	7-1
22A1MP2	(VARIABLE 1,6)		COUPLING ASSEMBLY, Quick Disconnect: Same as 22A1MP1 Variable 1,6	5-16
22A1MP2	(VARIABLE 2,3,4,5)	7006630-01	FILTER, AIR CONDITIONING: A1, RF shielded, oil type	7-1
22A1MP3	(VARIABLE 1,6) COMMERCIAL	910848-04	ELBOW PIPE: Brass; 90 deg street, 3/4-14 NPT thread	5-16

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1MP4	(VARIABLE 1,6)		ELBOW PIPE: Same as 22A1MP3	5-16
22A1MP5	(VARIABLE 1,6)	7008933-00	UNIVERSAL JOINT: Cres	5-16
22A1MP6	(VARIABLE 1,6)	7025369-00	ADAPTER, UNIVERSAL JOINT TO SOCKET	5-16
22A1MP7		7008938-00	WRENCH, CHASSIS ENGAGING	5-10
22A1P1		7025991-00	CONNECTOR, PLUG, ELECTRICAL: Female, 90 contact, rectangular	7-5
22A1PS1	(VARIABLE 1,6) (VARIABLE 2,3,4,5)	7024617-02 7024617-01	POWER SUPPLY: Contains 1 power supply subassembly (-01 to -02 mechanical change only)	7-1
22A1PS1A1		7024620-03	POWER SUPPLY SUBASSEMBLY: Contains 3 capacitors, 18 diodes, 6 terminal studs, 9 fuses, 1 connector, 3 transformers, 2 terminal boards, 4 bus bars, and 9 fuseholders	5-13
22A1PS1A1C1	CL25BH221TP3 MIL-C-3965	4912776-03	CAPACITOR, FIXED, ELECTROLYTIC: 50 vdc, 220 uf, -15 pct, +75 pct; -55 deg C(-67 deg F) to 85 deg C(185 deg F) operating temp range; insulated, hermetically sealed, metal case	5-13
22A1PS1A1C2			CAPACITOR: Same as 22A1PS1A1C1	5-13
22A1PS1A1C3			CAPACITOR: Same as 22A1PS1A1C1	5-13
22A1PS1A1CR1	1N1186 MIL-S-19500	7900134-00	SEMICONDUCTOR DEVICE, DIODE: Silicon, power; 35 amp.	5-13
22A1PS1A1CR2 thru 22A1PS1A1CR18			DIODE: Same as 11A1PS1A1CR1	5-13

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1PS1A1E1	3648-1 71279	903412-01	TERMINAL, STUD: Insulated, 2 turret	5-13
22A1PS1A1E2 thru 22A1PS1A1E4			TERMINAL: Same as 22A1PS1A1E1	5-13
22A1PS1A1E11			TERMINAL: Same as 22A1PS1A1E1	5-13
22A1PS1A1E12			TERMINAL: Same as 22A1PS1A1E1	5-13
22A1PS1A1F1	MDL-1 1/2 71400	900541-02	FUSE, CARTRIDGE: 1.5 amp, 125v; slow blow	5-13
22A1PS1A1F2			FUSE: Same as 22A1PS1A1F1	5-13
22A1PS1A1F3			FUSE: Same as 22A1PS1A1F1	
22A1PS1A1F4	F03B125V3AS MIL-F-15160	909993-01	FUSE, CARTRIDGE: 3 amp, 125v; Slow blow	5-13
22A1PS1A1F5			FUSE: Same as 22A1PS1A1F4	5-13
22A1PS1A1F6			FUSE: Same as 22A1PS1A1F4	5-13
22A1PS1A1F7	MDL-2 71400	900541-04	FUSE, CARTRIDGE: 2 amp, 125v; slow blow	5-13
22A1PS1A1F8			FUSE: Same as 22A1PS1A1F7	5-13
22A1PS1A1F9			FUSE: Same as 22A1PS1A1F7	5-13
22A1PS1A1J1	MS3102A32-6P MIL-C-5015 MS3102 AND10434	905522-01	CONNECTOR, RECEPTACLE, ELECTRICAL: Male, 23 contact, arc resistant plastic dielectric	5-13

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1PS1A1T1	S3860 80023	4911962-00	REACTOR-TRANSFORMER: Contains 1 fixed inductor and 1 transformer; inductor 0.18 mh, 0.011 ohm max; transformer input 115 vac, 400 cps each leg of 3-phase delta; output 4.25 vrms each leg of 6-phase star	5-13
22A1PS1A1T2	S3861 80023	4911960-00	REACTOR-TRANSFORMER: Contains 1 fixed inductor and 1 transformer; inductor 0.4 mh at 20 amp dc, 0.0155 ohm max; transformer input 115 vac, 400 cps each leg of 3-phase delta; output 12 vrms each leg of 6-phase star	5-13
22A1PS1A1T3			TRANSFORMER: Same as 22A1PS1A1T2	5-13
22A1PS1A1TB1	8TB6 MIL-T-16784 MIL-STD-242	910161-02	TERMINAL BOARD: Barrier type; 12 thd stud type terminals	5-14
22A1PS1A1TB2			TERMINAL BOARD: Same as 22A1PS1A1TB1	5-13
22A1PS1A1W1		7005432-00	BUS BAR: Brass; 3 in. lg	5-14
22A1PS1A1W2 thru 22A1PS1A1W4			BUS BAR: Same as 22A1PS1A1W1	5-14
22A1PS1A1XF1	FHN26G MIL-F-1920	911884-00	FUSEHOLDER: Extractor post, 250v, 30 amp	5-13
22A1PS1A1XF2 thru 22A1PS1A1XF9			FUSEHOLDER: Same as 22A1PS1A1XF1	5-13
22A1R1	RW20V202 MIL-R-26 MS90178	910177-09	RESISTOR, FIXED, WIRE WOUND: 2,000 ohm, ±5 pct, 21w at 25 deg C(77 deg F)	7-2

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1R2	RC32GF472J MIL-R-11	4911676-72	RESISTOR, FIXED, COMPOSITION: 4,700 ohm, ±5 pct, 1w at 70 deg C9158 deg F)	7-2
22A1R3			RESISTOR: Same as 22A1R1	7-2
22A1R4			RESISTOR: Same as 22A1R2	7-2
22A1R7	RC07GF104J MIL-R-11	4911672-81	RESISTOR, FIXED, COMPOSITION: 100,000 ohm, ±5 pct, 0.25 w at 70 deg C(158 deg F)	7-2
22A1R8 thru 22A1R11			RESISTOR: Same as 22A1R7	7-2
22A1S1	2AC6 91929	900139-00	SWITCH, PUSH: Spdt contact; interlock; 115/250 vac at 10 amp	5-12
22A1S2	47300-400 with mod no. 1,2,3,10B,13 and 34, set at 60 deg C(140 deg F) 73168	908944-01	SWITCH, THERMOSTATIC: Contacts open on temp increase; 0 deg C(32 deg F) to 93 deg C(140 deg F) adjustable temp range; factory set at 60 deg C (140 deg F); bimetal temp element	5-12 5-15
22A1S3	47301-400 with mod no. 1,2,3,10B,13 and 34, set at 46 deg C(115 deg F) 73168	908944-02	SWITCH, THERMOSTATIC: Contacts close on temp increase; 0 deg C(32 deg F) to 93 deg C(200 deg F) adjustable temp range; factory set at 46 deg C (115 deg F); bimetal temp element	5-12 5-15
22A1S4			SWITCH: Same as 22A1S2	5-12 7-3
22A1S5			SWITCH: Same as 22A1S3	5-12 7-3

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1T1	TR120-11 48294	7900917-03	TRANSFORMER: Power	5-19
22A1T2			TRANSFORMER: Same as 22A1T1	5-19
22A1TB1	8TB10 MIL-T-16784 MIL-STD-242	910161-04	TERMINAL BOARD: Barrier type; 20 thd stud type terminals	5-12 5-16
22A1TB2 thru 22A1TB4			TERMINAL BOARD: Same as 22A1TB1	5-12 5-15 5-16
22A1TB5		7026017-00	BUS BAR: Ground	5-15
22A1TB6 thru 22A1TB8			TERMINAL BOARD: Same as 22A1TB1	5-12 5-15
22A1TB9	(VARIABLE 1,6)		TERMINAL BOARD: Same as 22A1TB1	7-3
22A1TB9	(VARIABLE 2,3,4,5) 26TB12 MIL-T-16784 MIL-STD-242	911813-04	TERMINAL BOARD: Barrier type; 24 thd stud type terminals	5-12
22A1W1		7025652-02	BUS BAR: Power	5-11
22A1W2			BUS BAR: Same as 22A1W1	5-11
22A2W3			BUS BAR: Same as 22A1W1	5-11
22A1W4		7025651-00	BUS BAR: Ground	5-11
22A1W5 thru 22A1W7			BUS BAR: Same as 22A1W1	5-12

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1W8			BUS BAR: Same as 22A1W4	5-12
22A1A1		7025311-00	HOOD ASSEMBLY: Contains 2 lamps, 7 switches, and 18 indicators	7-1
22A1A1DS1	1819 08806	909809-00	LAMP, INCANDESCENT: Miniature; type T3-1/4; 0.04 amp, 28v	3-2
22A1A1DS2	1820 08806	910860-00	LAMP, INCANDESCENT: 0.1 amp at 28v	3-2
22A1A1S1	13AT401T4 91929	7900635-02	SWITCH, TOGGLE: 2 spdt contacts; 3 position, 2 momentary; 5 amp at 250 vac contact rating	3-2
22A1A1S2	MS16109-36-3-3N MILS-3786 MS16109	7900003-19	SWITCH, ROTARY: 3 deck, 3 position, 2 amp at 115 vac or 1 amp at 28 vdc	3-2
22A1A1S4	3-1900-4B16C 91812	7900362-59	SWITCH, ROTARY: 2 deck, 16 position	3-2
22A1A1S5	MBS-S-1838A-9 07137	7900987-00	SWITCH, PUSH: Spst contact; 1 momentary; white pushbutton; 100 ma at 110 vac contact rating	3-2
22A1A1S6			SWITCH: Same as 22A1A1S2	3-2
22A1A1S7			SWITCH: Same as 22A1A1S4	3-2
22A1A1S8			SWITCH: Same as 22A1A1S5	3-2
22A1A1XDS1	85410W-112 72619	7900678-01	LIGHT, INDICATOR: Thd mtd lensholder, phenolic barrel; 0.891 in. dia, glass green lens	3-2
22A1A1XDS2	85410W-111 72619	7900678-00	LIGHT, INDICATOR: Thd mtd lensholder, phenolic barrel; dia, glass red lens	3-2

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A1XDS3	H26-1166-1633 72619	7900496-23	SWITCH, PUSH: Spst contact, normally open, momentary; with 1 replaceable lamp, GE type 344; amber (transparent) lens	3-2
22A1A1XDS4 thru 22A1A1XDS18			INDICATOR: Same as 22A1A1XDS3	3-2
22A1A2	(VARIABLE 1,6) (VARIABLE 2,3,4,5)	7025316-02 7025316-00	CONTROL, POWER SUPPLY: Contains 3 capacitors, 2 resistors, 13 fuses, 3 connectors, 9 relays, 1 horn, 2 meters, 1 terminal board, 13 fuseholders, and 1 resistor-diode assembly	7-7
22A1A2C1	(VARIABLE 1,6) CPC09A1KE104KM 93790	907661-20	CAPACITOR, FIXED, PAPER DIELECTRIC: 0.1uf, ±10 pct, 400 vdc; metal case, hermetically sealed	7-7
22A1A2C2			CAPACITOR: Same as 22A1A2C1	7-7
22A1A2F1	F03A250V15AS MIL-F-15160	907783-19	FUSE, CARTRIDGE: 15 amp, 250v, normal instantaneous	7-7
22A1A2F2 thru 22A1A2F4			FUSE: Same as 22A1A2F1	7-7
22A1A2F5	(VARIABLE 1,6) F02A250V2AS MIL-F-15160	907783-11	FUSE, CARTRIDGE: 2 amp, 250v, normal instantaneous	7-7
22A1A2F5	(VARIABLE 2,3,4,5) F02A250V1AS MIL-F-15160	907783-09	FUSE, CARTRIDGE: 1 amp, 250v, normal instantaneous	7-7
22A1A2F6	(VARIABLE 1,6)		FUSE: Same as 22A1A2F5 Variable 1,6	7-7
22A1A2F6	(VARIABLE 2,3,4,5		FUSE: Same as 22A1A2F5 Variable 2,3,4,5	7-7

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A2F7	(VARIABLE 1,6)		FUSE: Same as 22A1A2F5 Variable 1,6	7-7
22A1A2F7	(VARIABLE 2,3,4,5)		FUSE: Same as 22A1A2F5 Variable 2,3,4,5	7-7
22A1A2F8	(VARIABLE 1,6)		FUSE: Same as 22A1A2F5 Variable 1,6	7-7
22A1A2F8	(VARIABLE 2,3,4,5)		FUSE: Same as 22A1A2F5 Variable 2,3,4,5	7-7
22A1A2F9	(VARIABLE 1,6)		FUSE: Same as 22A1A2F5 Variable 1,6	7-7
22A1A2F9	(VARIABLE 2,3,4,5)		FUSE: Same as 22A1A2F5 Variable 2,3,4,5	7-7
22A1A2F10	(VARIABLE 1,6)		FUSE: Same as 22A1A2F5 Variable 1,6	7-7
22A1A2F10	(VARIABLE 2,3,4,5)		FUSE: Same as 22A1A2F5 Variable 2,3,4,5	7-7
22A1A2F11	F03A250V10AS MIL-F-15160	907783-17	FUSE, CARTRIDGE: 10 amp, 250v, normal instantaneous	7-7
22A1A2F12			FUSE: Same as 22A1A2F11	7-7
22A1A2F13			FUSE: Same as 22A1A2F11	7-7
22A1A2J1	MS3102A18-1P MIL-C-5015 MS3102 MS33684	901773-01	CONNECTOR, RECEPTACLE, ELECTRICAL: Male, 10 contact, arc resistant plastic dielectric	7-7
22A1A2J2	MS3102A28-21S MIL-C-5015 MS3102 AND10434	902136-01	CONNECTOR, RECEPTACLE, ELECTRICAL: Female, 37 contact, arc resistant plastic dielectric	7-7
22A1A2J3	MS3102A20-22P MS3102 AND10430 MIL-C-5015	904142-01	CONNECTOR, RECEPTACLE, ELECTRICAL: Male, 6 contact, arc resistant plastic dielectric	7-7

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A2K1	R805-4-A-2.5K(3)	908162-00	RELAY, ARMATURE: 2 spdt contacts; 2500 ohm, 2 amp at 28 vdc or at 115 vac, 60 cps or 2 amp at 28 vdc contact rating	7-7
22A1A2K2	MS25271-A1 MIL-R-6106	908951-00	RELAY, ARMATURE: 4 spdt contacts; 10 amp at 115 vac or 28 vdc contact rating	7-7
22A1A2K3	6042 H47 15605	911909-00	RELAY, ARMATURE: 3pst contacts; 25 amp at 28 vdc or 115/200 vac, 400 cps contact rating	7-7
22A1A2K4			RELAY: Same as 22A1A2K3	7-7
22A1A2K5			RELAY: Same as 22A1A2K2	7-7
22A1A2K6			RELAY: Same as 22A1A2K2	7-7
22A1A2K7			RELAY: Same as 22A1A2K1	7-7
22A1A2K8	1000-156 98089	908161-00	RELAY, SOLENOID: 6 spdt contacts; 2 amp at 26.5 vdc contact rating	7-7
22A1A2K9			RELAY: Same as 22A1A2K8	7-7
22A1A2LS1	433M1-120V,400 Cycle 80252	909862-01	HORN, ELECTRICAL: 100 db minimum sound intensity rating at 3 ft; 120v, 220 ma, 400 cps	5-18 7-7
22A1A2M1	7010-010 27780	7900983-00	METER, TIME TOTALIZING: 115v, 60 cps, non-resettable elapsed time indicator 9999.9 hours; hermetically sealed	7-7
22A1A2M2			METER: Same as 22A1A2M1	7-7
22A1A2R4	C20GF471J MIL-R-11	4911674-41	RESISTOR, FIXED, COMPOSITION: 470 ohm, ±5 pct, 5 w at 70 deg C(158 deg F)	7-7
22A1A2R5			RESISTOR: Same as 22A1A2R4	7-7

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A2TB1	17TB10 MIL-P-15037 MIL-B-895	910893-00	TERMINAL BOARD: Barrier type; 20 thd stud type terminals	7-7
22A1A2XF1	IND300-9(IND300-9 cap only) 84613	908672-09	FUSEHOLDER: Extractor post; 125v, 30 amp	7-7
22A1A2XF2 thru 22A1A2XF13			FUSEHOLDER: Same as 22A1S3XF1	7-7
22A1A2A1		7025934-00	RESISTOR-DIODE ASSEMBLY: Contains 6 diodes and 3 resistors	7-7
22A1A2A1CR1	1N538M	907186-00	SEMICONDUCTOR DEVICE, DIODE: Silicon, power	7-6
22A1A2A1CR2 thru 22A1A2A1CR6			DIODE: Same as 22A1A2A1CR1	7-6
22A1A2A1R1	RW55G302 MIL-R-26 MS90178	900507-15	RESISTOR, FIXED, WIRE WOUND: 3,000 ohm, ±5 pct, 5w at 25 deg C(77 deg F)	7-6
22A1A2A1R2			RESISTOR: Same as 22A1A2A1R1	7-6
22A1A2A1R3			RESISTOR: Same as 22A1A2A1R1	7-6
22A1A3		7007900-02	TRANSPORT AND FRAME ASSEMBLY: Contains 6 mounts, 1 tape transport assembly, 1 drive electronics assembly, and 2 cable assemblies	7-1
22A1A3MP1	HT2-100 76005	7900282-00	MOUNT, RESILIENT: Rubber, medium load	5-18

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A3MP2 thru 22A1A3MP6			MOUNT: Same as 22A1A3MP1	5-18
22A1A3W1		7039461-01	CABLE ASSEMBLY, SPECIAL PURPOSE, ELECTRICAL: Write; contains 2 connectors	7-8
22A1A3W1P1	67-06C18-24S(113) 02660	7900875-03	CONNECTOR, PLUG, ELECTRICAL: Female; 24 contact, 1 connector mating end	7-8
22A1A3W1P2			CONNECTOR: Same as 22A1A3W1P1	7-8
22A1A3W2		7039460-01	CABLE ASSEMBLY, SPECIAL PURPOSE, ELECTRICAL: Read; contains 2 connectors	7-8
22A1A3W2P1	67-06C18-24P(113) 02660	7900878-03	CONNECTOR, PLUG, ELECTRICAL: Male; 24 contact, 1 connector mating end	7-8
22A1A3W2P2			CONNECTOR: Same as 22A1A3W2P1	7-8
22A1A3A1	MT120X41427 48294	7900917-01	TAPE TRANSPORT: Magnetic; 120 ips (refer to vendor manual, Potter Instrument Handbook S365-84 for MTS-120-X41427)	
22A1A3A2	MC120X41427 48294	7900917-02	DRIVE ELECTRONICS: (refer to vendor manual, Potter Instrument Handbook S365-84 for MTS-120-X41427)	
22A1A3A3A3			CHASSIS ASSEMBLY	5-18
22A1A3A3A3CB1	HE3C3-6-1 74193		CIRCUIT BREAKER	5-18
22A1A3A3A3J1	MS3102R14S-5S 81349		CONNECTOR, BULKHEAD	5-18
22A1A3A3A3J2			CONNECTOR: Same as 22A1A3A3A3J1	5-18
22A1A3A3A3J3	MS3102A14S-5SX 81349		CONNECTOR, BULKHEAD	5-18

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A3A3A3K1	KHU17A11-120 77342		RELAY	5-18
22A1A3A3A3K2			RELAY: Same as 22A1A3A3A3K1	5-18
22A1A3A3A3XK1	27E006 77342		SOCKET, RELAY	5-18
22A1A3A3A3XK2			SOCKET: Same as 22A1A3A3A3XK1	5-18
22A1A4	(VARIABLE 1,6)	7025315-00	CONNECTOR-FILTER ASSEMBLY: Contains 5 filters, 15 connectors, and 2 connector assemblies	5-15
22A1A4	(VARIABLE 2,3,4,5)	7026046-00	CONNECTOR-FILTER ASSEMBLY: Contains 5 filters 19 connectors, and 2 connector assemblies	5-15
22A1A4FL1	20JX31 56289	7900608-00	FILTER, RADIO FREQUENCY: 400 vdc or 125 vac at 20 amp	5-15
22A1A4FL2 thru 22A1A4FL5			FILTER: Same as 22A1A4FL1	5-15
22A1A4J1	DPD4500-1388 71468	906489-00	CONNECTOR, RECEPTACLE, ELECTRICAL: Male, 90 contact, arc resistant plastic dielectric	7-5
22A1A4J2 thru 22A1A4J7			CONNECTOR: Same as 22A1A4J1	7-5
22A1A4J11			CONNECTOR: Same as 22A1A4J1	7-5
22A1A4J12			CONNECTOR: Same as 22A1A4J1	7-5
22A1A4P13	DPD4500-5092 71468	908220-01	CONNECTOR, RECEPTACLE, ELECTRICAL: Female, 90 contact, arc resistant plastic dielectric	5-19

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A3MP2 thru 22A1A3MP6			MOUNT: Same as 22A1A3MP1	5-18
22A1A3W1		7039461-01	CABLE ASSEMBLY, SPECIAL PURPOSE, ELECTRICAL: Write; contains 2 connectors	7-8
22A1A3W1P1	67-06C18-24S(113) 02660	7900875-03	CONNECTOR, PLUG, ELECTRICAL: Female; 24 contact, 1 connector mating end	7-8
22A1A3W1P2			CONNECTOR: Same as 22A1A3W1P1	7-8
22A1A3W2		7039460-01	CABLE ASSEMBLY, SPECIAL PURPOSE, ELECTRICAL: Read; contains 2 connectors	7-8
22A1A3W2P1	67-06C18-24P(113) 02660	7900878-03	CONNECTOR, PLUG, ELECTRICAL: Male; 24 contact, 1 connector mating end	7-8
22A1A3W2P2			CONNECTOR: Same as 22A1A3W2P1	7-8
22A1A3A1	MT120X41427 48294	7900917-01	TAPE TRANSPORT: Magnetic; 120 ips (refer to vendor manual, Potter Instrument Handbook S365-84 for MTS-120-X41427)	
22A1A3A2	MC120X41427 48294	7900917-02	DRIVE ELECTRONICS: (refer to vendor manual, Potter Instrument Handbook S365-84 for MTS-120-X41427	
22A1A4	(VARIABLE 1,6)	7025315-00	CONNECTOR-FILTER ASSEMBLY: Contains 5 filters, 15 connectors, and 2 connector assemblies	5-15
22A1A4	(VARIABLE 2,3,4,5)	7026046-00	CONNECTOR-FILTER ASSEMBLY: Contains 5 filters 16 connectors, and 2 connector assemblies	5-15
22A1A4FL1	20JX31 56289	7900608-00	FILTER, RADIO FREQUENCY: 400 vdc or 125 vac at 20 amp	5-15

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A4FL2 thru 22A1A4FL5			FILTER: Same as 22A1A4FL1	5-15
22A1A4J1	DPD4500-1388 71468	906489-00	CONNECTOR, RECEPTACLE, ELECTRICAL: Male, 90 contact, arc resistant plastic dielectric	7-5
22A1A4J2 thru 22A1A4J7			CONNECTOR: Same as 22A1A4J1	7-5
22A1A4J11			CONNECTOR: Same as 22A1A4J1	7-5
22A1A4J12			CONNECTOR: Same as 22A1A4J1	7-5
22A1A4P13	DPD4500-5092 71468	908220-01	CONNECTOR, RECEPTACLE, ELECTRICAL: Female, 90 contact, arc resistant plastic dielectric	5-19
22A1A4P14	DPD4500-5104 71468	908221-00	CONNECTOR, RECEPTACLE, ELECTRICAL: Male, 90 contact, arc resistant plastic dielectric	5-19
22A1A4P15	MS3108B18-1S MIL-C-5015 MS3108 MS33684	911822-00	CONNECTOR, PLUG, ELECTRICAL: 10 contact, 1 connector mating end	5-18
22A1A4P16	MS3108B28-21P MIL-C-5015 MS3108 AND10433	903889-01	CONNECTOR, PLUG, ELECTRICAL: Male, 37 contact, 1 connector mating end	5-18
22A1A4P17	MRAC50-S-JTC6-H8 81312	7901119-00	CONNECTOR, PLUG, ELECTRICAL: Female, 50 contact, arc resistant plastic dielectric	5-18
22A1A4P18			CONNECTOR: Same as 22A1A4P17	5-19

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A4P14	DPD4500-5104 71468	908221-00	CONNECTOR, RECEPTACLE, ELECTRICAL: Male, 90 contact, arc resistant plastic dielectric	5-19
22A1A4P15	MS3108B18-1S MIL-C-5015 MS3108 MS33684	911822-00	CONNECTOR, PLUG, ELECTRICAL: 10 contact, 1 connector mating end	5-18
22A1A4P16	MS3108B28-21P MIL-C-5015 MS3108 AND10433	903889-01	CONNECTOR, PLUG, ELECTRICAL: Male, 37 contact, 1 connector mating end	5-18
22A1A4P17	MRAC50-S-JTC6-H8 81312	7901119-00	CONNECTOR, PLUG, ELECTRICAL: Female, 50 contact, arc resistant plastic dielectric	5-18
22A1A4P18			CONNECTOR: Same as 22A1A4P17	5-19
22A1A4P21	MS3106A20-22S MIL-C-5015 MS3106 AND10430	905720-01	CONNECTOR, PLUG, ELECTRICAL: Female, 6 contact, arc resistant plastic dielectric	
22A1A4P22	MS3106A14S-5PX 81349		CONNECTOR, PLUG	5-18
22A1A4P23	MS3106A14S-5P 81349		CONNECTOR, PLUG	5-18
22A1A4P24			CONNECTOR: Same as 22A1A4P23	5-18
22A1A4XP22	MS3057-6A 81349		ADAPTER, BACK-SHELL	5-18
22A1A4XP23			ADAPTER: Same as 22A1A4XP22	5-18

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A4XP24			ADAPTER: Same as 22A1A4XP22	5-18
22A1A4A1		7019245-00	CONNECTOR ASSEMBLY: Contains 4 connectors	5-11
22A1A4A1J1	3614875 91886	7900842-00	CONNECTOR, RECEPTACLE, ELECTRICAL: Male, 189 contacts, wire-wrap type to accommodate 2 wraps of 24 awg wire	5-11
22A1A4A1J2 thru 22A1A4A1J4			CONNECTOR: Same as 22A1A4A1J1	5-11
22A1A4A2			CONNECTOR ASSEMBLY: Same as 22A1A4A1	5-12
22A1A10		7025981-00	WIRING HARNESS: Contains 1 connector	5-12
22A1A10P1	MS3108B16-6S MIL-C-5015 MS3108 AND10428	905071-01	CONNECTOR, PLUG, ELECTRICAL: Female, 23 contact; 1 connector mating end	5-13
22A1A11		7025960-00	HOOD ASSEMBLY: Contains 4 lamps, 2 switches, and 4 indicators	7-1
22A1A11DS1	1826 71744	7900677-00	LAMP, INCANDESCENT: 0.15 amp, 18 vdc; single contact, miniature bayonet	5-11
22A1A11DS2			LAMP: Same as 22A1A1DS1	5-11
22A1A11DS3			LAMP: Same as 22A1A1DS2	5-11
22A1A11DS4			LAMP: Same as 22A1A1DS2	5-11
22A1A11S1			SWITCH: Same as 22A1A1S1	5-11

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A4P21	MS3106A20-22S MIL-C-5015 MS3106 AND10430	905720-01	CONNECTOR, PLUG, ELECTRICAL: Female, 6 contact, arc resistant plastic dielectric	
22A1A4A1		7019245-00	CONNECTOR ASSEMBLY: Contains 4 connectors	5-11
22A1A4A1J1	3614875 91886	7900842-00	CONNECTOR, RECEPTACLE, ELECTRICAL: Male, 189 contacts, wire-wrap type to accomodate 2 wraps of 24 awg wire	5-11
22A1A4A1J2 thru 22A1A4A1J4			CONNECTOR: Same as 22A1A4A1J1	5-11
22A1A4A2			CONNECTOR ASSEMBLY: Same as 22A1A4A1	5-12
22A1A10		7025981-00	WIRING HARNESS: Contains 1 connector	5-12
22A1A10P1	MS3108B16-6S MIL-C-5015 MS3108 AND10428	905071-01	CONNECTOR, PLUG, ELECTRICAL: Female, 23 contact; 1 connector mating end	5-13
22A1A11		7025960-00	HOOD ASSEMBLY: Contains 4 lamps, 2 switches, and 4 indicators	7-1
22A1A11DS1	1826 71744	7900677-00	LAMP, INCANDESCENT: 0.15 amp, 18 vdc; single contact, miniature bayonet	5-11
22A1A11DS2			LAMP: Same as 22A1A1DS1	5-11
22A1A11DS3			LAMP: Same as 22A1A1DS2	5-11
22A1A11DS4			LAMP: Same as 22A1A1DS2	5-11

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A11S1			SWITCH: Same as 22A1A1S1	5-11
22A1A11S2	23AT1 91929	908484-00	SWITCH, TOGGLE: Dpdt contact; 5 amp at 115/200 vac, 400 cps contact rating	5-11
22A1A11XDS1			INDICATOR: Same as 22A1A1XDS1	5-11
22A1A11XDS2			INDICATOR: Same as 22A1A1XDS1	5-11
22A1A11XDS3			INDICATOR: Same as 22A1A1XDS2	5-11
22A1A11XDS4			INDICATOR: Same as 22A1A1XDS2	5-11
22A1A12		7019247-06	CONVERTER, DIGITAL-TO-DIGITAL: Contains 6 diodes, 2 sockets, 2 logic chassis assemblies, and 1 door and panel assembly	7-1
22A1A12CR1			DIODE: Same as 22A1PS1A1CR1	5-6
22A1A12CR2			DIODE: Same as 22A1PS1A1CR1	5-6
22A1A12CR3	IN2804RB MIL-S-19500	908578-01	SEMICONDUCTOR DEVICE, DIODE: Silicon, voltage regulator, 50 watts, reverse	5-6
22A1A12CR4			DIODE: Same as 22A1PS1A1CR1	5-6
22A1A12CR5			DIODE: Same as 22A1PS1A1CR1	5-6
22A1A12CR6			DIODE: Same as 22A1A12CR3	5-6
22A1A12XCR3	8038-1G3 91506	7900149-00	SOCKET, SEMICONDUCTOR DEVICE: TO-3	5-6
22A1A12XCR6			SOCKET: Same as 22A1A12XCR3	5-6

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A11S2	23AT1 91929	908484-00	SWITCH, TOGGLE: Dpdt contact; 5 amp at 115/200 vac, 400 cps contact rating	5-11
22A1A11XDS1			INDICATOR: Same as 22A1A1XDS1	5-11
22A1A11XDS2			INDICATOR: Same as 22A1A1XDS1	5-11
22A1A11XDS3			INDICATOR: Same as 22A1A1XDS2	5-11
22A1A11XDS4			INDICATOR: Same as 22A1A1XDS2	5-11
22A1A12		7019247-06	CONVERTER, DIGITAL-TO-DIGITAL: Contains 6 diodes, 2 sockets, 2 logic chassis assemblies, and 1 door and panel assembly	7-1
22A1A12CR1			DIODE: Same as 22A1PS1A1CR1	5-6
22A1A12CR2			DIODE: Same as 22A1PS1A1CR1	5-6
22A1A12CR3	IN2804RB MIL-S-19500	908578-01	SEMICONDUCTOR DEVICE, DIODE: Silicon, voltage regulator, 50 watts, reverse	5-6
22A1A12CR4			DIODE: Same as 22A1PS1A1CR1	5-6
22A1A12CR5			DIODE: Same as 22A1PS1A1CR1	5-6
22A1A12CR6			DIODE: Same as 22A1A12CR3	5-6
22A1A12XCR3	8038-1G3 91506	7900149-00	SOCKET, SEMICONDUCTOR DEVICE: TO-3	5-6
22A1A12XCR6			SOCKET: Same as 22A1A12XCR3	5-6

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A12A1		7019234-10	LOGIC CHASSIS ASSEMBLY: Contains 2 capacitors, 247 connectors, 2 resistors, and 2 test point assemblies	5-5
22A1A12A1C1	3C3 56289	7900288-00	CAPACITOR, FIXED, CERAMIC DIELECTRIC: 25 vdc, 0.01 uf, ±20 pct; 0 deg C(32 deg F) to 85 deg C (185 deg F) operating temp range; insulated; 0.125 in. deep, 0.202 in. high, 0.39 in. wide	5-5
22A1A12A1C2			CAPACITOR: Same as 22A1A12A1C1	5-5
22A1A12A1J1A	A2345-10 16512	7900251-01	CONNECTOR, RECEPTACLE, ELECTRICAL: Female; wire-wrap, 15 solder contacts, with ground clip, black body Note: All 245 card jacks this assembly are the same as 22A1A12A1J1A	
22A1A12A1P1	3614676 91886	7900843-00	CONNECTOR, RECEPTACLE, ELECTRICAL: Female, 189 contacts, wire-wrap type to accommodate 2 wraps of 24 awg wire	5-5
22A1A12A1P2			CONNECTOR: Same as 22A1A12A1P1	5-5
22A1A12A1R1	RC07GF181J MIL-R-11	4911672-15	RESISTOR, FIXED, COMPOSITION: 180 ohm, ±5 pct, 0.25 w at 70 deg C(158 deg F)	
22A1A12A1R2			RESISTOR: Same as 22A1A12A1R1	
22A1A12A1TB1	3614873 91886	7900841-00	TEST POINT ASSEMBLY: 231 contacts, wire wrap type to accommodate 1 wrap of 24 awg wire	5-9
22A1A12A1TB2			TEST POINT ASSEMBLY: Same as 22A1A12A1TB1	5-9
22A1A12A2		7019234-11	LOGIC CHASSIS ASSEMBLY: Contains 1 capacitor, 247 connectors, 10 resistors, and 2 test point assemblies	5-6

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A12A2C1	CK12AX102M 00656	7900959-08	CAPACITOR, FIXED, CERAMIC DIELECTRIC: 100 vdc, 1,000 uuf, ±20 pct; insulated body; 0.07 in. dia, 0.29 in. lg	
22A1A12A2J1A	A2345-10 16512	7900251-01	CONNECTOR, RECEPTACLE, ELECTRICAL: Female; wire wrap, 15 solder contacts, with ground clip, black body Note: All 245 card jacks this assembly are the same as 22A1A12A2J1A	5-6
22A1A12A2P1			CONNECTOR: Same as 22A1A12A1P1	5-6
22A1A12A2P2			CONNECTOR: Same as 22A1A12A1P1	5-6
22A1A12A2R1 thru 22A1A12A2R8			RESISTOR: Same as 22A1A12A1R1	
22A1A12A2R9	RC07GF102J MIL-R-11	4911672-33	RESISTOR, FIXED, COMPOSITION: 1,000 ohm, ±5 pct, 0.25w at 70 deg C(158 deg F)	
22A1A12A2R10			RESISTOR: Same as 22A1A12A2R9	
22A1A12A2TB1			TEST POINT ASSEMBLY: Same as 22A1A12A1TB1	5-9
22A1A12A2TB2			TEST POINT ASSEMBLY: Same as 22A1A12A1TB1	5-9
22A1A12A3		7019284-08	DOOR AND PANEL ASSEMBLY: Contains 1 control-indicator and 1 capacitor-resistor assembly	5-9
22A1A12A3A1		7025255-00	CONTROL-INDICATOR: Contains 2 resistors, 10 switches, and 140 indicators	5-9

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A12A3A1R1	JA1N056S105UA 01121	910389-14	RESISTOR, VARIABLE: Composition; 1 megohm ±10 pct, 2w at 70 deg C(158 deg F); linear taper, slotted, self-locking	5-9
22A1A12A3A1R2	JA1N056S503UA 01121	910389-10	RESISTOR, VARIABLE: Composition; 50,000 ohm, ±10 pct, 2w at 70 deg C(158 deg F); linear taper, slotted, self-locking shaft	5-9
22A1A12A3A1S1 thru 22A1A12A3A1S6			SWITCH: Same as 22A1A1S5	5-9
22A1A12A3A1S7	MS16109-36-4-7N MIL-S-3786 MS16109	7900003-32	SWITCH, ROTARY: Sectional type; 1 pole, 4 deck, 7 position	5-9
22A1A12A3A1S8	MS16109-36-4-6N MIL-S-3786 MS16109	7900003-31	SWITCH, ROTARY: Sectional type; 1 pole, 4 deck, 6 position	5-9
22A1A12A3A1S9	13AT403T2 91929	908832-00	SWITCH, TOGGLE: 2 pdt contacts; 3 position, 1 momentary, 5 amp at 250 vac or 30 vdc contact rating	5-9
22A1A12A3A1S10	MS25089-3C MIL-S-6743 MS25089	908035-02	SWITCH, PUSH: Dpst contact; black button; 28v, 10 amp	5-9
22A1A12A3A1XDS8A thru 22A1A12A3A1XDS14A			INDICATOR: Same as 22A1A1XDS3	
22A1A12A3A1XDS1B			INDICATOR: Same as 22A1A1XDS3	5-9
22A1A12A3A1XDS2B			INDICATOR: Same as 22A1A1XDS3	5-9

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A12A3A1XDS8B thru 22A1A12A3A1XDS14B			INDICATOR: Same as 22A1A1XDS3	5-9
22A1A12A3A1XDS1C			INDICATOR: Same as 22A1A1XDS3	5-9
22A1A12A3A1XDS2C			INDICATOR: Same as 22A1A1XDS3	5-9
22A1A12A3A1XDS5C			INDICATOR: Same as 22A1A1XDS3	5-9
22A1A12A3A1XDS8C thru 22A1A12A3A1XDS14C			INDICATOR: Same as 22A1A1XDS3	5-9
22A1A12A3A1XDS1D			INDICATOR: Same as 22A1A1XDS3	5-9
22A1A12A3A1XDS2D			INDICATOR: Same as 22A1A1XDS3	5-9
22A1A12A3A1XDS4D			INDICATOR: Same as 22A1A1XDS3	5-9
22A1A12A3A1XDS5D			INDICATOR: Same as 22A1A1XDS3	5-9
22A1A12A3A1XDS8D thru 22A1A12A3A1XDS14D			INDICATOR: Same as 22A1A1XDS3	5-9
22A1A12A3A1XDS1E			INDICATOR: Same as 22A1A1XDS3	5-9
22A1A12A3A1XDS2E			INDICATOR: Same as 22A1A1XDS3	5-9
22A1A12A3A1XDS4E			INDICATOR: Same as 22A1A1XDS3	5-9
22A1A12A3A1XDS5E			INDICATOR: Same as 22A1A1XDS3	5-9

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A12A3A1XDS9E thru 22A1A12A3A1XDS14E			INDICATOR: Same as 22A1A1XDS3	5-9
22A1A12A3A1XDS1F			INDICATOR: Same as 22A1A1XDS3	5-9
22A1A12A3A1XDS3F			INDICATOR: Same as 22A1A1XDS3	5-9
22A1A12A3A1XDS5F			INDICATOR: Same as 22A1A1XDS3	5-9
22A1A12A3A1XDS8F thru 22A1A12A3A1XDS14F			INDICATOR: Same as 22A1A1XDS3	5-9
22A1A12A3A1XDS1G thru 22A1A12A3A1XDS6G			INDICATOR: Same as 22A1A1XDS3	5-9
22A1A12A3A1XDS8G thru 22A1A12A3A1XDS14G			INDICATOR: Same as 22A1A1XDS3	5-9
22A1A12A3A1XDS1H thru 22A1A12A3A1XDS14H			INDICATOR: Same as 22A1A1XDS3	5-9
22A1A12A3A1XDS1J thru 22A1A12A3A1XDS14J			INDICATOR: Same as 22A1A1XDS3	5-9
22A1A12A3A1XDS1K thru 22A1A12A3A1XDS14K			INDICATOR: Same as 22A1A1XDS3	5-9

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A12A3A1XDS1L thru 22A1A12A3A1XDS14L			INDICATOR: Same as 22A1A1XDS3	5-9
22A1A12A3A1XDS1M thru 22A1A12A3A1XDS14M			INDICATOR: Same as 22A1A1XDS3	5-9
22A1A12A3A2		7005360-01	CAPACITOR-RESISTOR ASSEMBLY: Contains 2 capacitors and 14 resistors	5-9
22A1A12A3A2C2	CL25BG400UP3 MIL-C-3965	4912778-01	CAPACITOR, FIXED, ELECTROLYTIC: 25 vdc, 40 uf, -15 pct, +75 pct; -55 deg C(-67 deg F) to 85 deg C(185 deg F) operating temp range; metal case, insulated, hermetically sealed	5-9
22A1A12A3A2C3	150D157X0006R2 56289	908404-16	CAPACITOR, FIXED, ELECTROLYTIC: 6 vdc, 150 uf, ±20 pct, -80 deg C(-112 deg F) to 85 deg C(185 deg F) operating temp range; metal case, insulated, hermetically sealed	5-9
22A1A12A3A2R1	RC07GF471J MIL-R-11	4911672-25	RESISTOR, FIXED, COMPOSITION: 470 ohm, ±5 pct, 0.25w at 70 deg C(158 deg F)	5-9
22A1A12A3A2R2 thru 22A1A12A3A2R14			RESISTOR: Same as 22A1A12A3A2R1	5-9
22A1A13		7019247-07	CONVERTER, DIGITAL TO DIGITAL: Contains 6 diodes, 2 sockets, 1 power supply, 1 converter subassembly, and 1 door and panel assembly	7-1
22A1A13CR1			DIODE: Same as 22A1PS1A1CR1	5-7
22A1A13CR2			DIODE: Same as 22A1PS1A1CR1	5-7

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A17C33 thru 22A1A17C44			Not used	
22A1A17C45			CAPACITOR: Same as 22A1A17C12	5-17

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A17CR1			DIODE: Same as 22A1A12CR3	5-17
22A1A17CR2			DIODE: Same as 22A1A13A1A1CR1	5-17
22A1A17CR3			DIODE: Same as 22A1A13A1A1CR1	5-17
22A1A17CR4			DIODE: Same as 22A1A13A1CR1	5-17
22A1A17XCR4			SOCKET: Same as 22A1A12XCR3	5-17
22A1A17J1	67-00C18-24P(113) 02660	7900876-03	CONNECTOR, RECEPTACLE, ELECTRICAL: Male, 24 contact, arc resistant plastic dielectric	
22A1A17J2			CONNECTOR: Same as 22A1A4P13	5-17
22A1A17J3			CONNECTOR: Same as 22A1A4P14	5-17
22A1A17J4	67-00C18-24S(113) 02660	7900877-03	CONNECTOR, RECEPTACLE, ELECTRICAL: Female, 24 contact, arc resistant plastic dielectric	5-17
22A1A17J5			CONNECTOR: Same as 22A1A17J1	5-17
22A1A17J6			CONNECTOR: Same as 22A1A17J4	5-17
22A1A17M1	150SP-2 18583		INDICATOR, ELAPSED TIME	5-17
22A1A17M2			INDICATOR: Same as 22A1A17M1	5-17
22A1A17Q1			TRANSISTOR: Same as 22A1A13A1Q1	5-17
22A1A17Q2	2N1490 02735	4913289-00	TRANSISTOR: NPN, silicon, power	5-17
22A1A17R1 thru 22A1A17R6			RESISTOR: Same as 22A1A13A2R1	5-17

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A17R8			RESISTOR: Same as 22A1A13A2R1	5-17
22A1A17R9			RESISTOR: Same as 22A1A13A2R1	5-17
22A1A17R10 thru 22A1A17R17			RESISTOR: Same as 22A1A12A1R1	5-17
22A1A17R18	RC07GF511J MIL-R-11	4911672-26	RESISTOR, FIXED, COMPOSITION: 510 ohm, ±5 pct, 0.25w at 70 deg C(158 deg F)	5-17
22A1A17R19			RESISTOR: Same as 22A1A17R18	5-17
22A1A17R20			RESISTOR: Same as 22A1A12A1R1	5-17
22A1A17R21 thru 22A1A17R28			RESISTOR: Same as 22A1A13A2R1	5-17
22A1A17R29 thru 22A1A17R38			RESISTOR: Same as 22A1A12A1R1	5-17
22A1A17R40			RESISTOR: Same as 22A1A17R18	5-17
22A1A17R42			RESISTOR: Same as 22A1A17R18	5-17
22A1A17R43	RC07GF271J MIL-R-11	4911672-19	RESISTOR, FIXED, COMPOSITION: 270 ohm, ±5 pct, 0.25w at 70 deg C(158 deg F)	5-17
22A1A17R44			RESISTOR: Same as 22A1A17R43	5-17
22A1A17R45	RC07GF222J MIL-R-11	4911672-41	RESISTOR, FIXED, COMPOSITION: 2,200 ohm, ±5 pct, 0.25w at 70 deg C(158 deg F)	5-17
22A1A17R46			RESISTOR: Same as 22A1A17R43	5-17

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A17CR1			DIODE: Same as 22A1A12CR3	5-17
22A1A17CR2			DIODE: Same as 22A1A13A1A1CR1	5-17
22A1A17CR3			DIODE: Same as 22A1A13A1A1CR1	5-17
22A1A17J1	67-00C18-24P(113) 02660	7900876-03	CONNECTOR, RECEPTACLE, ELECTRICAL: Male, 24 contact, arc resistant plastic dielectric	
22A1A17J2			CONNECTOR: Same as 22A1A4P13	5-17
22A1A17J3			CONNECTOR: Same as 22A1A4P14	5-17
22A1A17J4	67-00C18-24S(113) 02660	7900877-03	CONNECTOR, RECEPTACLE, ELECTRICAL: Female, 24 contact, arc resistant plastic dielectric	5-17
22A1A17J5			CONNECTOR: Same as 22A1A17J1	5-17
22A1A17J6			CONNECTOR: Same as 22A1A17J4	5-17
22A1A17Q1			TRANSISTOR: Same as 22A1A13A1Q1	5-17
22A1A17Q2	2N1490 02735	4913289-00	TRANSISTOR: NPN, silicon, power	5-17
22A1A17R1 thru 22A1A17R6			RESISTOR: Same as 22A1A13A2R1	5-17
22A1A17R8			RESISTOR: Same as 22A1A13A2R1	5-17
22A1A17R9			RESISTOR: Same as 22A1A13A2R1	5-17
22A1A17R10 thru 22A1A17R17			RESISTOR: Same as 22A1A12A1R1	5-17

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A17R18	RC07GF511J MIL-R-11	4911672-26	RESISTOR, FIXED, COMPOSITION: 510 ohm, ±5 pct, 0.25w at 70 deg C(158 deg F)	5-17
22A1A17R19			RESISTOR: Same as 22A1A17R18	5-17
22A1A17R20			RESISTOR: Same as 22A1A12A1R1	5-17
22A1A17R21 thru 22A1A17R28			RESISTOR: Same as 22A1A13A2R1	5-17
22A1A17R29 thru 22A1A17R38			RESISTOR: Same as 22A1A12A1R1	5-17
22A1A17R40			RESISTOR: Same as 22A1A17R18	5-17
22A1A17R42			RESISTOR: Same as 22A1A17R18	5-17
22A1A17R43	RC07GF271J MIL-R-11	4911672-19	RESISTOR, FIXED, COMPOSITION: 270 ohm, ±5 pct, 0.25w at 70 deg C(158 deg F)	5-17
22A1A17R44			RESISTOR: Same as 22A1A17R43	5-17
22A1A17R45	RC07GF222J MIL-R-11	4911672-41	RESISTOR, FIXED, COMPOSITION: 2,200 ohm, ±5 pct, 0.25w at 70 deg C(158 deg F)	5-17
22A1A17R46			RESISTOR: Same as 22A1A17R43	5-17
22A1A17R47			RESISTOR: Same as 22A1A17R43	5-17
22A1A17R49	RC07GF470J MIL-R-11	4911672-01	RESISTOR; FIXED, COMPOSITION: 47 ohm, ±5 pct, 0.25w at 70 deg C(158 deg F)	5-17
22A1A17R50 thru 22A1A17R52			RESISTOR: Same as 22A1A17R49	5-17

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A17R47			RESISTOR: Same as 22A1A17R43	5-17
22A1A17R49	RC07GF470J MIL-R-11	4911672-01	RESISTOR; FIXED, COMPOSITION: 47 ohm, ±5 pct, 0.25w at 70 deg C(158 deg F)	5-17
22A1A17R50 thru 22A1A17R52			RESISTOR: Same as 22A1A17R49	5-17
22A1A17R54	RC20GF101J MIL-R-11	4911674-25	RESISTOR, FIXED, COMPOSITION: 100 ohm, ±5 pct, 0.5w at 70 deg C(158 deg F)	5-17
22A1A17R55			RESISTOR: Same as 22A1A17R54	5-17
22A1A17R56 thru 22A1A17R58	RC07GF302J 81349		RESISTOR: Same as 22A1A13A1R5	5-17
22A1A17R59	RC07GF204J 81349		RESISTOR, FIXED, COMPOSITION, 200.000 ohm, ±5 pct, 0.25w at 70 deg C(158 deg F)	5-17
22A1A17R60			RESISTOR: Same as 22A1A17R59	5-17
22A1A17R61	6010P-1-503 80294		RESISTOR, VARIABLE: 50.000 ohm	5-17
22A1A17R62			RESISTOR: Same as 22A1A17R61	5-17
22A1A17XCR1			SOCKET: Same as 22A1A12XCR3	5-17
22A1A17XM1	A501 18583		SOCKET, INDICATOR MOUNTING	5-17
22A1A17XM2			SOCKET, Same as 22A1A17XM1	5-17
22A1A17XQ1			SOCKET: Same as 22A1A12XCR3	5-17

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A17XQ2			SOCKET: Same as 22A1A12XCR3	5-17
22A1A17A1		7025332-00	CONNECTOR ASSEMBLY: Contains 122 connectors and 2 test blocks	5-17
22A1A17A1J1A	A2345-10 16512	7900251-01	CONNECTOR, RECEPTACLE, ELECTRICAL: Female, wire-wrap, 15 solder contacts, with ground clip, black body Note: All 122 card jacks this assembly are the same as 22A1A17A1J1A	5-17
22A1A17A1TB1		7007928-00	TEST BLOCK	5-17
22A1A17A1TB2			TEST BLOCK: Same as 22A1A17A1TB1	5-17
22A2			CABINET ELECTRICAL EQUIPMENT, ADD-ON UNIT (For reference only)	7-1
22A2B1	(VARIABLE 1,6)		FAN: Same as 22A1B1 Variable 1,6	5-16
22A2B1	(VARIABLE 5)		FAN: Same as 22A1B1 Variable 2,3,4,5	5-12
22A2B2	(VARIABLE 5)		FAN: Same as 22A1B1 Variable 2,3,4,5	5-12
22A2B3	(VARIABLE 1,6)		FAN: Same as 22A1B1 Variable 1,6	5-16
22A2B3	(VARIABLE 5)		FAN: Same as 22A1B1 Variable 2,3,4,5	5-12
22A2B4	(VARIABLE 5)		FAN: Same as 22A1B1 Variable 2,3,4,5	5-12
22A2C1 thru 22A2C4	(VARIABLE 5)		CAPACITOR: Same as 22A1C1 Variable 2,3,4,5	5-12
22A2E3	(VARIABLE 1,5,6)		TERMINAL: Same as 22A1E3	7-4

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A17R54	RC20GF101J MIL-R-11	4911674-25	RESISTOR, FIXED, COMPOSITION: 100 ohm, ±5 pct, 0.5w at 70 deg C(158 deg F)	5-17
22A1A17R55			RESISTOR: Same as 22A1A17R54	5-17
22A1A17XCR1			SOCKET: Same as 22A1A12XCR3	5-17
22A1A17XQ1			SOCKET: Same as 22A1A12XCR3	5-17
22A1A17XQ2			SOCKET: Same as 22A1A12XCR3	5-17
22A1A17A1		7025332-00	CONNECTOR ASSEMBLY: Contains 122 connectors and 2 test blocks	5-17
22A1A17A1J1A	A2345-10 16512	7900251-01	CONNECTOR, RECEPTACLE, ELECTRICAL: Female, wire-wrap, 15 solder contacts, with ground clip, black body Note: All 122 card jacks this assembly are the same as 22A1A17A1J1A	5-17
22A1A17A1TB1		7007928-00	TEST BLOCK	5-17
22A1A17A1TB2			TEST BLOCK: Same as 22A1A17A1TB1	5-17
22A2			CABINET ELECTRICAL EQUIPMENT, ADD-ON UNIT (For reference only)	7-1
22A2B1	(VARIABLE 1,6)		FAN: Same as 22A1B1 Variable 1,6	5-16
22A2B1	(VARIABLE 5)		FAN: Same as 22A1B1 Variable 2,3,4,5	5-12
22A2B2	(VARIABLE 5)		FAN: Same as 22A1B1 Variable 2,3,4,5	5-12
22A2B3	(VARIABLE 1,6)		FAN: Same as 22A1B1 Variable 1,6	5-16

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A2B3	(VARIABLE 5)		FAN: Same as 22A1B1 Variable 2,3,4,5	5-12
22A2B4	(VARIABLE 5)		FAN: Same as 22A1B1 Variable 2,3,4.5	5-12
22A2C1 thru 22A2C4	(VARIABLE 5)		CAPACITOR: Same as 22A1C1 Variable 2,3,4,5	5-12
22A2E3	(VARIABLE 1,5,6)		TERMINAL: Same as 22A1E3	7-4
22A2E4	(VARIABLE 1,5,6)		TERMINAL: Same as 22A1E3	7-4
22A2E7 thru 22A2E13	(VARIABLE 1,5,6)		TERMINAL: Same as 22A1E7	7-4
22A2MP1			COUPLING ASSEMBLY-DUST CAP: Same as 22A1MP1 Variable 1,6	5-16
22A2MP1			FILTER, AIR CONDITIONING: Same as 22A1MP1	5-16
22A2MP2			COUPLING ASSEMBLY-DUST CAP: Same as 22A1MP1 Variable 1,6	
22A2MP3	(VARIABLE 1,6)		ELBOW PIPE: Same as 22A1MP3	5-16
22A2MP4	(VARIABLE 1,6)		ELBOW PIPE: Same as 22A1MP3	5-16
22A2MP5	(VARIABLE 1,6)		UNIVERSAL JOINT: Same as 22A1MP5	5-16
22A2MP6	(VARIABLE 1,6)		ADAPTER: Same as 22A1MP6	5-16
22A2R1	(VARIABLE 1,5,6)		RESISTOR: Same as 22A1R1	7-4
22A2R2	(VARIABLE 1,5,6)		RESISTOR: Same as 22A1R2	7-4

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A2E4	(VARIABLE 1,5,6)		TERMINAL: Same as 22A1E3	7-4
22A2E7 thru 22A2E13	(VARIABLE 1,5,6)		TERMINAL: Same as 22A1E7	7-4
22A2MP1			COUPLING ASSEMBLY-DUST CAP: Same as 22A1MP1 Variable 1,6	5-16
22A2MP1			FILTER, AIR CONDITIONING: Same as 22A1MP1	5-16
22A2MP2			COUPLING ASSEMBLY-DUST CAP: Same as 22A1MP1 Variable 1,6	
22A2MP3	(VARIABLE 1,6)		ELBOW PIPE: Same as 22A1MP3	5-16
22A2MP4	(VARIABLE 1,6)		ELBOW PIPE: Same as 22A1MP3	5-16
22A2MP5	(VARIABLE 1,6)		UNIVERSAL JOINT: Same as 22A1MP5	5-16
22A2MP6	(VARIABLE 1,6)		ADAPTER: Same as 22A1MP6	5-16
22A2R1	(VARIABLE 1,5,6)		RESISTOR: Same as 22A1R1	7-4
22A2R2	(VARIABLE 1,5,6)		RESISTOR: Same as 22A1R2	7-4

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A2R7 thru 22A2R11	(VARIABLE 1,5,6)		RESISTOR: Same as 22A1R7	7-4
22A2S2	(VARIABLE 1,5,6)		SWITCH: Same as 22A1S2	5-12 5-15
22A2S3	(VARIABLE 1,5,6)		SWITCH: Same as 22A1S3	5-12 5-15
22A2T1	(VARIABLE 1,5,6)		TRANSFORMER: Same as 22A1T1	5-19
22A2T2	(VARIABLE 1,5,6)		TRANSFORMER: Same as 22A1T1	5-19
22A2TB1 thru 22A2TB2	(VARIABLE 1,5,6)		TERMINAL BOARD: Same as 22A1TB1	5-12 5-15 5-16
22A2TB5	(VARIABLE 1,5,6)		BUS BAR: Same as 22A1TB5	5-12 5-15 5-16
22A2TB6	(VARIABLE 1,5,6)		TERMINAL BOARD: Same as 22A1TB1	5-12 5-15 5-16
22A2A1	(VARIABLE 1,5,6)		HOOD ASSEMBLY: Same as 22A1A1	7-1
22A2A2	(VARIABLE 1,6) (VARIABLE 5)	7025316-03 7025316-01	POWER SUPPLY CONTROL: Contains 2 capacitors, 13 fuses, 3 connectors, 6 relays, 2 meters, 1 terminal board, 13 fuseholders, and 1 resistor-diode assembly	5-18
22A2A2C1	(VARIABLE 1,5,6)		CAPACITOR: Same as 22A1A2C1	7-7
22A1A2C2	(VARIABLE 1,5,6)		CAPACITOR: Same as 22A1A2C1	7-7

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A2A2F1 thru 22A2A2F4	(VARIABLE 1,5,6)		FUSE: Same as 22A1A2F1	7-7
22A2A2F5	(VARIABLE 1,6)		FUSE: Same as 22A1A2F5 Variable 1,6	7-7
22A2A2F5	(VARIABLE 5)		FUSE: Same as 22A1A2F5 Variable 2,3,4,5	7-7
22A2A2F6	(VARIABLE 1,6)		FUSE: Same as 22A1A2F5 Variable 1,6	7-7
22A2A2F6	(VARIABLE 5)		FUSE: Same as 22A1A2F5 Variable 2,3,4,5	7-7
22A2A2F7	(VARIABLE 1,6)		FUSE: Same as 22A1A2F5 Variable 1,6	7-7
22A2A2F7	(VARIABLE 5)		FUSE: Same as 22A1A2F5 Variable 2,3,4,5	7-7
22A2A2F8	(VARIABLE 1,6)		FUSE: Same as 22A1A2F5 Variable 1,6	7-7
22A2A2F8	(VARIABLE 5)		FUSE: Same as 22A1A2F5 Variable 2,3,4,5	7-7
22A2A2F9	(VARIABLE 1,6)		FUSE: Same as 22A1A2F5 Variable 1,6	7-7
22A2A2F9	(VARIABLE 5)		FUSE: Same as 22A1A2F5 Variable 2,3,4,5	7-7
22A2A2F10	(VARIABLE 1,6)		FUSE: Same as 22A1A2F5 Variable 1,6	7-7
22A2A2F10	(VARIABLE 5)		FUSE: Same as 22A1A2F5 Variable 2,3,4,5	7-7
22A2A2F11 thru 22A2A2F13	(VARIABLE 1,5,6)		FUSE: Same as 22A1A2F5 Variable 2,3,4,5	7-7
22A2A2J1	(VARIABLE 1,5,6)		CONNECTOR: Same as 22A1A2J1	7-7
22A2A2J2	(VARIABLE 1,5,6)		CONNECTOR: Same as 22A1A2J2	7-7

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A2A2J3	(VARIABLE 1,5,6)		CONNECTOR: Same as 22A1A2J3	7-7
22A2A2K1	(VARIABLE 1,5,6)		RELAY: Same as 22A1A2K1	7-7
22A2A2K2	(VARIABLE 1,5,6)		RELAY: Same as 22A1A2K2	7-7
22A2A2K3	(VARIABLE 1,5,6)		RELAY: Same as 22A1A2K3	7-7
22A2A2K4	(VARIABLE 1,5,6)		RELAY: Same as 22A1A2K3	7-7
22A2A2K7	(VARIABLE 1,5,6)		RELAY: Same as 22A1A2K1	7-7
22A2A2K9	(VARIABLE 1,5,6)		RELAY: Same as 22A1A2K8	7-7
22A2A2M1	(VARIABLE 1,5,6)		METER: Same as 22A1A2M1	7-7
22A2A2M2	(VARIABLE 1,5,6)		METER: Same as 22A1A2M1	7-7
22A2A2R4	(VARIABLE 1,5,6)		RESISTOR: Same as 22A1A2R4	7-7
22A2A2R5	(VARIABLE 1,5,6)		RESISTOR: Same as 22A1A2R4	7-7
22A2A2TB1	(VARIABLE 1,5,6)		TERMINAL BOARD: Same as 22A1A2TB1	7-7
22A2A2XF1 thru 22A2A2XF13	(VARIABLE 1,5,6)		FUSEHOLDER: Same as 22A1A2XF1	7-7
22A2A2A1	(VARIABLE 1,5,6)	7025934-01	RESISTOR-DIODE ASSEMBLY: Contains 4 diodes and 1 resistor	7-7
22A2A2A1CR1	(VARIABLE 1,5,6)		DIODE: Same as 22A1A2A1CR1	7-6
22A2A2A1CR2	(VARIABLE 1,5,6)		DIODE: Same as 22A1A2A1CR1	7-6
22A2A2A1CR4	(VARIABLE 1,5,6)		DIODE: Same as 22A1A2A1CR1	7-6

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A2A2A1CR6	(VARIABLE 1,5,6)		DIODE: Same as 22A1A2A1CR1	7-6
22A2A2A1R1	(VARIABLE 1,5,6)		RESISTOR: Same as 22A1A2A1R1	7-6
22A2A3			TRANSPORT AND FRAME ASSEMBLY: Same as 22A1A3	7-1
22A2A4	(VARIABLE 1,6)	7025317-00	CONNECTOR-FILTER ASSEMBLY: Contains 5 filters and 8 connectors	5-15
22A2A4	(VARIABLE 5)	7026047-00	CONNECTOR-FILTER ASSEMBLY: Contains 5 filters and 9 connectors	5-15
22A2A4FL1 thru 22A2A4FL5			FILTER: Same as 22A1A4FL1	5-15
22A2A4J1	(VARIABLE 1,5,6)		CONNECTOR: Same as 22A1A4J1	7-5
22A2A4J2	(VARIABLE 1,5,6)		CONNECTOR: Same as 22A1A4J1	7-5
22A2A4P13	(VARIABLE 1,5,6)		CONNECTOR: Same as 22A1A4P13	5-19
22A2A4P14	(VARIABLE 1,5,6)		CONNECTOR: Same as 22A1A4P14	5-19
22A2A4P15	(VARIABLE 1,6)		CONNECTOR: Same as 22A1A4P15 Variable 1,6	5-18
22A2A4P15	(VARIABLE 5)		CONNECTOR: Same as 22A1A4P15 Variable, 2,3,4,5	5-18
22A2A4P16	(VARIABLE 1,5,6)		CONNECTOR: Same as 22A1A4P16	5-18
22A2A4P17	(VARIABLE 1,5,6)		CONNECTOR: Same as 22A1A4P17	5-18
22A2A4P18	(VARIABLE 1,5,6)		CONNECTOR: Same as 22A1A4P17	5-19
22A2A4P21			CONNECTOR: Same as 22A1A4P21	5-19

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A2A6	(VARIABLE 1,5,6)	7025995-00	CABLE ASSEMBLY: Contains 2 connectors	7-5
22A2A6P1	(VARIABLE 1,5,6) DPD4500-5002 71468	908220-00	CONNECTOR, RECEPTACLE, ELECTRICAL: Female, 90 contact, arc resistant plastic dielectric	7-5
22A2A6P2	(VARIABLE 1,5,6)		CONNECTOR: Same as 22A2A6P1	7-5
22A2A16	(VARIABLE 1,3,6)		TRANSPORT AND FRAME ASSEMBLY: Same as 22A1A3	7-1
22A2A17	(VARIABLE 1,5,6)		CONVERTER: Same as 22A1A17 Variable 2,3,4,5	7-1

TABLE 7-4. MANUFACTURERS' CODES

CODE	NAME	ADDRESS
00656	Aerovox Corp.	740 Belleville Ave. New Bedford, MA 02741
01121	Allen-Bradley Co.	1201 2nd St. Milwaukee, WI 53212
02660	Amphenol-Borg Electronics Corp.	2801 S. 25th Ave. Broadview, IL 60153
02735	RCA Corp. Solid State Division	Rt. 202 Somerville, NJ 08876
07137	TEC Inc.	6700 Washington Ave South Eden Prairie, MN 55343
08806	General Electric Co. Miniature Lamp Department	Nela Park Cleveland, OH 44112
15605	Cutler-Hammer, Inc.	4201 N. 27th St. Milwaukee, WI 53216
16512	Fabri-Tex, Inc. National Connector Div.	9210 Science Center Dr. New Hope, MN
18583	Curtis Instrument, Inc.	200 Kisco Ave. Mount Kisco, NY 10549
27780	General Time Corp. Industrial Controls Div.	Rt. 8 Torrington, CT 06791
37942	Mallory, P. R. and Co., Inc.	3029 East Washington St. Indianapolis, IN 46206
48294	Potter Instrument Co.	151 Sunnyside Blvd. Plainview, NY 11803
56289	Sprague Electric Co.	North Adams, MA 01247
71279	Cambridge Thermionic Corp.	445 Concord Ave. Cambridge, MA 02138
71400	Bussmann Mfg., Division of McGraw-Edison Co.	2536 W. University St. St. Louis, MO 63017
71468	ITT, Cannon Electric	666 E. Dyer Rd. Santa Ana, CA 92702

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A2A6	(VARIABLE 1,5,6)	7025995-00	CABLE ASSEMBLY: Contains 2 connectors	7-5
22A2A6P1	(VARIABLE 1,5,6) DPD4500-5002 71468	908220-00	CONNECTOR, RECEPTACLE, ELECTRICAL: Female, 90 contact, arc resistant plastic dielectric	7-5
22A2A6P2	(VARIABLE 1,5,6)		CONNECTOR: Same as 22A2A6P1	7-5
22A2A16	(VARIABLE 1,5,6)		TRANSPORT AND FRAME ASSEMBLY: Same as 22A1A3	7-1
22A2A17	(VARIABLE 1,5,6)		CONVERTER: Same as 22A1A17 Variable 2,3,4,5	7-1

TABLE 7-4. MAGNETIC TAPE UNIT, LIST OF MANUFACTURERS

VENDOR CODE	NAME	ADDRESS
00656	Aerovox Corp.	New Bedford, Mass.
01121	Allen-Bradley Co.	Milwaukee, Wis.
02660	Amphenol-Borg Electronics Corp.	Broadview (Chicago), Ill.
02735	Radio Corp. of America, Commercial Receiving Tube and Semiconductor Division	Somerville, N.J.
07137	Transistor Electronics Corp.	Minneapolis, Minn.
08806	General Electric Co., Miniature Lamp Department	Cleveland, Ohio
15605	Cutler-Hammer, Inc.	Milwaukee, Wis.
16512	Nation Connector Corp.	Minneapolis, Minn.
27780	Haydon Division of General Time Corp.	Torrington, Conn.
37942	Mallory, P. R. and Co., Inc.	Indianapolis, Ind.
48294	Potter Instrument Co., Inc.	Plainview, N.Y.
56289	Sprague Electric Co.	North Adams, Mass.
71279	Cambridge Thermionic Corp.	Cambridge, Mass.
71400	Bussmann Mfg., Division of McGraw-Edison Co.	St. Louis, Mo.
71468	ITT, Cannon Electric, Inc.	Los Angeles, Calif.
71744	Chicago Miniature Lamp Works	Chicago, Ill.
72619	Dialight Corp.	Brooklyn, N.Y.
73168	Fenwal, Inc.	Ashland, Mass.
73992	Hansen Mfg. Co.	Cleveland, Ohio
76005	Lord Mfg. Co.	Erie, Pa.
80023	Schott, Oscar A. Co., Inc.	Minneapolis, Minn.
80183	Sprague Products Co.	North Adams, Mass.

TABLE 7-4. MANUFACTURERS' CODES (CONT.)

CODE	NAME	ADDRESS
71744	Chicago Miniature Lamp Works	4433 Ravenwood Ave. Chicago, IL 60640
72619	Dialight Corp. Sub. of Digitronics Corp.	60 Stewart Ave. Brooklyn, NY 11237
73168	Fenwal, Inc.	400 Main St. Ashland, MA 01721
74193	Heinemann Electric Co.	2600 Brunswick Pike P.O. Box 299 Trenton, NJ 08602
73992	Hansen Mfg. Co.	4031 W. 150th St. Cleveland, OH 44135
76005	Lord Mfg. Co. Division of Lord Corp.	1635 West 12th Street Erie, PA 16512
77342	AMF, Inc. Potter and Brumfield Div.	1200 E. Broadway P.O. Box 522 Princeton, IN 47570
80023	Schoot, Oscar A. Co., Inc.	500 11th Ave. S Minneapolis, MN 55415
80183	Superseded by 56289	
80252	Faraday, Incorporated	805 S. Maumee St. Tecumseh, MI 49286
80294	Bourns, Inc., Instrument Div.	6135 Magnolia Ave. Riverside, CA 92506
81312	Winchester Electronics Div. of Litton Industries, Inc.	Main St. and Hillside Ave. Oakville, CT 06779
81349	Military Specifications Promulgated by Military Departments/Agencies under Authority of Defense Standardization Manual 4120-3M	
82877	Rotron Inc.	7-9 Hasbrouck Lane Woodstock, NY 12498

TABLE 7-4. MANUFACTURERS' CODES (CONT.)

CODE	NAME	ADDRESS
84613	Fuse Indicator Corp.	5900 Fishers Lane Rockville, MD 20850
91506	Augat, Inc.	33 Perry Ave. Attleboro, MA 02703
91812	Janco Corp.	3111 Wivona Ave. Box 3038 Burbank, CA 91504
91886	Malco Mfg. Co., Inc.	5150 West Roosevelt Rd. Chicago, IL 60650
91929	Honeywell, Inc. Micro-Switch Division	Chicago and Spring Streets Freeport, IL 61032
92702	IMC Magnetic Corp. Eastern Division	570 Main St. Westbury (Long Island), NY 11591
92739	Ampex Corp.	401 Broadway Redwood City, CA 94063
93790	Cornell-Dubilier Electric Division, Federal Pacific Electric Co.	1605 Rodney French Blvd. New Bedford, MA 02744
96906	Military Standards Promulgated by Standardization Div. Directorate of Logistics Services DSA	
98089	Electro-Tec Corp.	Hwy 460 West P.O. Box 129 Blacksbury, VA 24060
98927	Electronic Specialty Co. Portland Electronics Division	18900 N.E. Sandy Rd. P.O. Box 20055 Portland, OR 97220

TABLE 7-4. MAGNETIC TAPE UNIT, LIST OF MANUFACTURERS (CONT.)

VENDOR CODE	NAME	ADDRESS
80252	Sperti Faraday, Inc.	Adrian, Mich.
81312	Winchester Electronics, Division Litton Industries, Inc.	Oakville, Conn.
82877	Rotron Mfg. Co., Inc.	Woodstock, N.Y.
84613	Fuse Indicator Corp.	Rockville, Md.
91506	Augat, Inc.	Attleboro, Mass.
91812	Janco Corp.	Burbank, Calif.
91886	Malco Mfg. Co.	Chicago, Ill.
91929	Honeywell, Inc., Micro-Switch Division	Freeport, Ill.
92702	IMC Magnetic Corp, Eastern Division	Westbury (Long Island), N.Y.
92739	Ampex Corp.	Redwood City, Calif.
93790	Cornell-Dubilier Electric Division, Federal Pacific Electric Corp.	New Bedford, Mass.
98089	Electro Tec Corp.	Blacksbury, Va.
98927	Electronic Specialty Co., Electronics Division	Portland, Ore.

TYPEFACE SPECIMEN SHEET

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TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A13CR3			DIODE: Same as 22A1A12CR3	5-7
22A1A13CR4			DIODE: Same as 22A1PS1A1CR1	5-7
22A1A13CR5			DIODE: Same as 22A1PS1A1CR1	5-7
22A1A13CR6			DIODE: Same as 22A1A12CR3	5-7
22A1A13XCR3			SOCKET: Same as 22A1A12XCR3	5-7
22A1A13XCR6			SOCKET: Same as 22A1A12XCR3	5-7
22A1A13A1		7025229-00	POWER SUPPLY: Contains 2 capacitors, 1 diode, 2 fuses, 119 connectors, 1 transistor, 9 resistors, 2 fuseholders, 2 sockets, 1 power supply subassembly, 2 test point	5-7
22A1A13A1C1			CAPACITOR: Same as 22A1PS1A1C1	5-7
22A1A13A1C2			CAPACITOR: Same as 22A1PS1A1C1	5-7
22A1A13A1CR1	1N2825B	7902219-32	SEMICONDUCTOR DEVICE, DIODE	5-7
22A1A13A1F1	F02A250V6AS MIL-F-15160	907783-15	FUSE, CARTRIDGE: 6 amp, 250v, normal instantaneous	5-7
22A1A13A1F2			FUSE: Same as 22A1A13A1F1	5-7
22A1A13A1J33A	A2345-10 16512	7900251-01	CONNECTOR, RECEPTACLE, ELECTRICAL: Female; wire wrap, 15 solder contacts, with ground clip, black body Note: All 117 card jacks this assembly are the same as 22A1A13A1J33A	5-7
22A1A13A1P1			CONNECTOR: Same as 22A1A12A1P1	5-7

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A13A1P2			CONNECTOR: Same as 22A1A12A1P1	5-7
22A1A13A1Q1	2N297A MIL-S-19500	7900895-00	TRANSISTOR: PNP, germanium, power	5-7
22A1A13A1R1	RW20V101 MIL-R-26 MS90178	910177-51	RESISTOR, FIXED, WIRE WOUND: 100 ohm, ±5 pct, 21w at 25 deg C(77 deg F)	5-7
22A1A13A1R2			RESISTOR: Same as 22A1A13A1R1	5-7
22A1A13A1R3	RC07GF562J MIL-R-11	4911672-51	RESISTOR, FIXED, COMPOSITION: 5,600 ohm, ±5 pct, 0.25w at 70 deg C(158 deg F)	5-7
22A1A13A1R4			RESISTOR: Same as 22A1A13A1R3	
22A1A13A1R5 thru 22A1A13A1R9	RC07GF302J 81349		RESISTOR, FIXED, COMPOSITION: 3000 ohm, ±5 pct, 0.25w at 70 deg C(158 deg F)	5-7
22A1A13A1TB1			TEST POINT ASSEMBLY: Same as 22A1A12A1TB1	5-10
22A1A13A1TB2			TEST POINT ASSEMBLY: Same as 22A1A12A1TB1	5-10
22A1A13A1XCR1			SOCKET: Same as 22A1A12XCR3	5-7
22A1A13A1XF1	IND300-5(IND300-5 cap only) 84613	908672-05	FUSEHOLDER: Extractor post; 26.5v, 30 amp	5-7
22A1A13A1XF2			FUSEHOLDER: Same as 22A1A13A1XF1	5-7
22A1A13A1XQ1			SOCKET: Same as 22A1A12XCR3	5-7
22A1A13A1A1		7007753-00	POWER SUPPLY SUBASSEMBLY: Contains 12 diodes and 1 transformer	5-7

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONTD.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A13CR3			DIODE: Same as 22A1A12CR3	5-7
22A1A13CR4			DIODE: Same as 22A1PS1A1CR1	5-7
22A1A13CR5			DIODE: Same as 22A1PS1A1CR1	5-7
22A1A13CR6			DIODE: Same as 22A1A12CR3	5-7
22A1A13XCR3			SOCKET: Same as 22A1A12XCR3	5-7
22A1A13XCR6			SOCKET: Same as 22A1A12XCR3	5-7
22A1A13A1		7025229-00	POWER SUPPLY: Contains 2 capacitors, 2 fuses, 119 connectors, 1 transistor, 4 resistors, 2 fuseholders, 1 socket, 1 power supply subassembly, 2 test point	5-7
22A1A13A1C1			CAPACITOR: Same as 22A1PS1A1C1	5-7
22A1A13A1C2			CAPACITOR: Same as 22A1PS1A1C1	5-7
22A1A13A1F1	F02A250V6AS MIL-F-15160	907783-15	FUSE, CARTRIDGE: 6 amp, 250v, normal instantaneous	5-7
22A1A13A1F2			FUSE: Same as 22A1A13A1F1	5-7
22A1A13A1J33A	A2345-10 16512	7900251-01	CONNECTOR, RECEPTACLE, ELECTRICAL: Female; wire wrap, 15 solder contacts, with ground clip, black body Note: All 117 card jacks this assembly are the same as 22A1A13A1J33A	5-7
22A1A13A1P1			CONNECTOR: Same as 22A1A12A1P1	5-7

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A13A1P2			CONNECTOR: Same as 22A1A12A1P1	5-7
22A1A13A1Q1	2N297A MIL-S-19500	7900895-00	TRANSISTOR: PNP, germanium, power	5-7
22A1A13A1R1	RW20V101 MIL-R-26 MS90178	910177-51	RESISTOR, FIXED, WIRE WOUND: 100 ohm, ±5 pct, 21w at 25 deg C(77 deg F)	5-7
22A1A13A1R2			RESISTOR: Same as 22A1A13A1R1	5-7
22A1A13A1R3	RC07GF562J MIL-R-11	4911672-51	RESISTOR, FIXED, COMPOSITION: 5,600 ohm, ±5 pct, 0.25w at 70 deg C(158 deg F)	5-7
22A1A13A1R4			RESISTOR: Same as 22A1A13A1R3	
22A1A13A1TB1			TEST POINT ASSEMBLY: Same as 22A1A12A1TB1	5-10
22A1A13A1TB2			TEST POINT ASSEMBLY: Same as 22A1A12A1TB1	5-10
22A1A13A1XF1	IND300-5(IND300-5 cap only) 84613	908672-05	FUSEHOLDER: Extractor post; 26.5v, 30 amp	5-7
22A1A13A1XF2			FUSEHOLDER: Same as 22A1A13A1XF1	5-7
22A1A13A1XQ1			SOCKET: Same as 22A1A12XCR3	5-7
22A1A13A1A1		7007753-00	POWER SUPPLY SUBASSEMBLY: Contains 12 diodes and 1 transformer	5-7
22A1A13A1A1CR1	1N1202 MIL-S-19500	908293-00	SEMICONDUCTOR DEVICE, DIODE: Silicon, power; 200v	5-7

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A13A1A1CR1	1N1202 MIL-S-19500	908293-00	SEMICONDUCTOR DEVICE, DIODE: Silicon, power; 200v	5-7

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A13A1A1CR2 thru 22A1A13A1A1CR12			DIODE: Same as 22A1A13A1A1CR1	5-7
22A1A13A1A1T1	S4293 80023	7900299-00	REACTOR-TRANSFORMER: Contains 1 transformer and 2 inductors; each inductor 500 uh min. at 70 amp dc, 1.33 vrms, 2400 cps; input 115 vac, 400 cps, 3-phase; output 28.8 vrms each leg at no load, 7 amp dc, 6-phase star, 12.8 vrms at no load, 2 amp vrms; single phase	5-7
22A1A13A2		7025916-00	CONVERTER SUBASSEMBLY: Contains 247 connectors, 15 resistor, and 2 test point assemblies	5-8
22A1A13A2J1A	A2345-10 16512	7900251-01	CONNECTOR, RECEPTACLE, ELECTRICAL: Female; wire wrap, 15 solder contacts, with ground clip, black body Note: All 245 card jacks this assembly are the same as 22A1A13A2J1A	5-8
22A1A13A2P1			CONNECTOR: Same as 22A1A12A1P1	5-8
22A1A13A2P2			CONNECTOR: Same as 22A1A12A1P1	5-8
22A1A13A2R1	RC20GF820J MIL-R-11	4911674-23	RESISTOR, FIXED, COMPOSITION: 82 ohm, ±5 pct, 0.5 w at 70 deg C(158 deg F)	5-8
22A1A13A2R2 thru 22A1A13A2R14			RESISTOR: Same as 22A1A13A2R1	5-8
22A1A13A2R15	RC07GF201J MIL-R-11	4911672-16	RESISTOR, FIXED, COMPOSITION: 200 ohm, ±5 pct, 0.25w at 70 deg C(158 deg F)	
22A1A13A2TB1			TEST POINT ASSEMBLY: Same as 22A1A12A1TB1	5-10
22A1A13A2TB2			TEST POINT ASSEMBLY: Same as 22A1A12A1TB1	5-10
22A1A13A3		7019284-09	DOOR AND PANEL ASSEMBLY: Contains 1 control-indicator and 1 capacitor-resistor assembly	5-10

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A13A3A1		7025257-00	CONTROL-INDICATOR: Contains 1 resistor, 5 switches, and 27 indicators	5-10
22A1A13A3A1R1			RESISTOR: Same as 22A1A12A3A1R1	5-10
22A1A13A3A1S1 thru 22A1A13A3A1S4			SWITCH: Same as 22A1A1S5	5-10
22A1A13A3A1S5	MS25306-231 MIL-S-8836	910658-00	SWITCH, TOGGLE: Spdt contact; 20 amp at 115 vac, 60 cps	5-10
22A1A13A3A1XDS1A thru 22A1A13A3A1XDS3A			INDICATOR: Same as 22A1A1XDS3	5-10
22A1A13A3A1XDS1B thru 22A1A13A3A1XDS4B			INDICATOR: Same as 22A1A1XDS3	5-10
22A1A13A3A1XDS1C thru 22A1A13A3A1XDS4C			INDICATOR: Same as 22A1A1XDS3	5-10
22A1A13A3A1XDS1D thru 22A1A13A3A1XDS4D			INDICATOR: Same as 22A1A1XDS3	5-10
22A1A13A3A1XDS1E thru 22A1A13A3A1XDS4E			INDICATOR: Same as 22A1A1XDS3	5-10
22A1A13A3A1XDS1F thru 22A1A13A3A1XDS4F			INDICATOR: Same as 22A1A1XDS3	5-10

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A13A3A1XDS1G thru 22A1A13A3A1XDS4G			INDICATOR: Same as 22A1A1XDS3	5-10
22A1A13A3A2		7005360-00	CAPACITOR-RESISTOR ASSEMBLY: Contains 2 capacitors and 14 resistors	5-10
22A1A13A3A2C2			CAPACITOR: Same as 22A1A12A3A2C2	5-10
22A1A13A3A2C3			CAPACITOR: Same as 22A1A12A3A2C3	5-10
22A1A13A3A2R1 thru 22A1A13A3A2R13			RESISTOR: Same as 22A1A12A3A2R1	5-10
22A1A13A3A2R14	RC07GF330J MIL-R-11	4911673-51	RESISTOR, FIXED, COMPOSITION: 33 ohm, ±5 pct, 0.25 w at 70 deg C(158 deg F)	5-10
22A1A16			TRANSPORT AND FRAME ASSEMBLY: Same as 22A1A3	7-1
22A1A17	(VARIABLE 1,6) (VARIABLE 2,3,4,5)	7025309-01 7025309-00	CONVERTER, DIGITAL-TO-DIGITAL: Contains 32 capacitors, 4 diodes, 6 connectors, 2 transistors, 62 resistors, 4 sockets, 2 meters, and 1 connector assembly	7-1
22A1A17C1	CL25BH301TP3 MIL-C-3965	4912776-04	CAPACITOR, FIXED, ELECTROLYTIC: 50 vdc, 300 uf, -15 pct, +75 pct; -55 deg C(-67 deg F) to 85 deg C(185 deg F) operating temp range; insulated, hermetically sealed, metal case	5-17
22A1A17C2 thru 22A1A17C5			CAPACITOR: Same as 22A1A17C1	5-17

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A17C7	4C023474X0250A3 80183	7900288-10	CAPACITOR, FIXED, CERAMIC DIELECTRIC: 25 vdc 0.47 uf, +20 pct; -55 deg C(-67 deg F) to 85 deg C (185 deg F) operating temp range; insulated	5-17
22A1A17C8 thru 22A1A17C11			CAPACITOR: Same as 22A1A17C7	5-17
22A1A17C12	CS13BF156K MIL-C-26655	7900164-20	CAPACITOR, FIXED, ELECTROLYTIC: 35 vdc, 15 uf, ±10 pct; -55 deg C(-67 deg F) to 85 deg C(185 deg F) operating temp range; insulated, hermetically sealed, metal case	5-17
22A1A17C13			CAPACITOR: Same as 22A1A17C12	5-17
22A1A17C14			CAPACITOR: Same as 22A1A17C7	5-17
22A1A17C15			CAPACITOR: Same as 22A1A17C7	
22A1A17C17			CAPACITOR: Same as 22A1A17C12	5-17
22A1A17C20 thru 22A1A17C25			CAPACITOR: Same as 22A1A17C12	5-17
22A1A17C27			CAPACITOR: Same as 22A1A17C12	5-17
22A1A17C28			CAPACITOR: Same as 22A1A17C12	5-17
22A1A17C29	CK12AX222M MIL-C-11015	7900959-09	CAPACITOR, FIXED, CERAMIC DIELECTRIC: 100 vdc, 2,200 uuf, ±20 pct; insulated body; 0.090 in. dia; 0.470 in. lg	5-17
22A1A17C30 thru 22A1A17C32			CAPACITOR: Same as 22A1A17C7	5-17

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A13A3A1XDS1G thru 22A1A13A3A1XDS4G			INDICATOR: Same as 22A1A1XDS3	5-10
22A1A13A3A2		7005360-00	CAPACITOR-RESISTOR ASSEMBLY: Contains 2 capacitors and 14 resistors	5-10
22A1A13A3A2C2			CAPACITOR: Same as 22A1A12A3A2C2	5-10
22A1A13A3A2C3			CAPACITOR: Same as 22A1A12A3A2C3	5-10
22A1A13A3A2R1 thru 22A1A13A3A2R13			RESISTOR: Same as 22A1A12A3A2R1	5-10
22A1A13A3A2R14	RC07GF330J MIL-R-11	4911673-51	RESISTOR, FIXED, COMPOSITION: 33 ohm, ±5 pct, 0.25 w at 70 deg C(158 deg F)	5-10
22A1A16			TRANSPORT AND FRAME ASSEMBLY: Same as 22A1A3	7-1
22A1A17	(VARIABLE 1,6) (VARIABLE 2,3,4,5)	7025309-01 7025309-00	CONVERTER, DIGITAL-TO-DIGITAL: Contains 32 capacitors, 3 diodes, 6 connectors, 2 transistors, 55 resistors, 3 sockets, and 1 connector assembly	7-1
22A1A17C1	CL25BH301TP3 MIL-C-3965	4912776-04	CAPACITOR, FIXED, ELECTROLYTIC: 50 vdc, 300 uf, -15 pct, +75 pct; -55 deg C(-67 deg F) to 85 deg C(185 deg F) operating temp range; insulated, hermetically sealed, metal case	5-17
22A1A17C2 thru 22A1A17C5			CAPACITOR: Same as 22A1A17C1	5-17

TABLE 7-3. MAGNETIC TAPE UNIT, MAINTENANCE PARTS LIST (CONT.)

REFERENCE DESIGNATION	PART NUMBER AND MANUFACTURER	UNIVAC PART NUMBER	NAME AND DESCRIPTION	FIGURE NUMBER
22A1A17C7	4C023474X0250A3 80183	7900288-10	CAPACITOR, FIXED, CERAMIC DIELECTRIC: 25 vdc 0.47 uf, +20 pct; -55 deg C(-67 deg F) to 85 deg C (185 deg F) operating temp range; insulated	5-17
22A1A17C8 thru 22A1A17C11			CAPACITOR: Same as 22A1A17C7	5-17
22A1A17C12	CS13BF156K MIL-C-26655	7900164-20	CAPACITOR, FIXED, ELECTROLYTIC: 35 vdc, 15 uf, ±10 pct; -55 deg C(-67 deg F) to 85 deg C(185 deg F) operating temp range; insulated, hermetically sealed, metal case	5-17
22A1A17C13			CAPACITOR: Same as 22A1A17C12	5-17
22A1A17C14			CAPACITOR: Same as 22A1A17C7	5-17
22A1A17C15			CAPACITOR: Same as 22A1A17C7	
22A1A17C17			CAPACITOR: Same as 22A1A17C12	5-17
22A1A17C20 thru 22A1A17C25			CAPACITOR: Same as 22A1A17C12	5-17
22A1A17C27			CAPACITOR: Same as 22A1A17C12	5-17
22A1A17C28			CAPACITOR: Same as 22A1A17C12	5-17
22A1A17C29	CK12AX222M MIL-C-11015	7900959-09	CAPACITOR, FIXED, CERAMIC DIELECTRIC: 100 vdc, 2,200 uuf, ±20 pct; insulated body; 0.090 in. dia; 0.470 in. lg	5-17
22A1A17C30 thru 22A1A17C32			CAPACITOR: Same as 22A1A17C7	5-17