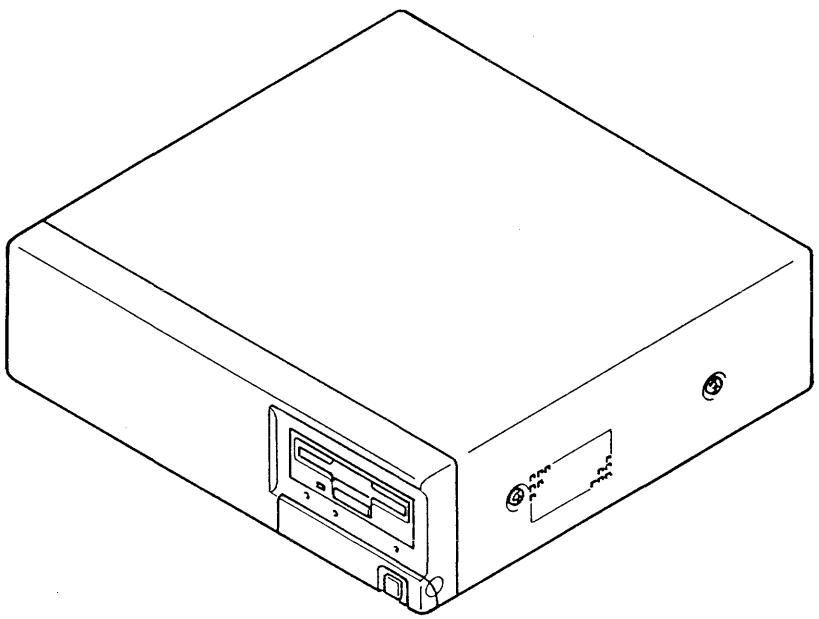
NWS-1510/1530/1580

SERVICE MANUAL

EK Model



NEWS

NET WORK STATION

SONY®

CONTENTS

CHAPTER 1
OPERATION

System Overview

Superb architecture with high-performance 32-bit processor

The NEWS 1500 Series NET WORK STATION boasts a superb architecture employing a high-performance 25MHz MC68030 32-bit microprocessor.

UNIX[1] workstation features

The NET WORK STATION NWS-1510/1530/1580 consists of a 32-bit MC68030, a 25MHz MC68882 floating point co-processor, a 4M byte main memory (expandable up to 16M bytes). It also incorporates a large capacity hard disk drive, and a 3.5-inch floppydisk drive. In keeping with the NEWS 1700 Series design concept, it is also equipped with an Ethernet[2] controller, two RS-232C serial ports, a parallel port for printer connection, a keyboard/mouse interface, SCSI bus for external storage devices, and bitmap interface supporting 1024 x 768 bits display with 256 different colors selected from approximately 16.7 million colors at a time (NWS-1530, NWS-1580).
When connected to one of the optional bitmap displays and an Ethernet transceiver, it allows you to configure a high-performance UNIX workstation.

The NEWS 1500 Series comes in three models whose specifications differ as follows.

Model name	Hard disk	Bitmap Interface	Main memory
NWS-1510	40M bytes*	Not equipped	4M bytes
NWS-1530	40M bytes*	Color bitmap	4M bytes
NWS-1580	170M bytes*	Color bitmap	4M bytes

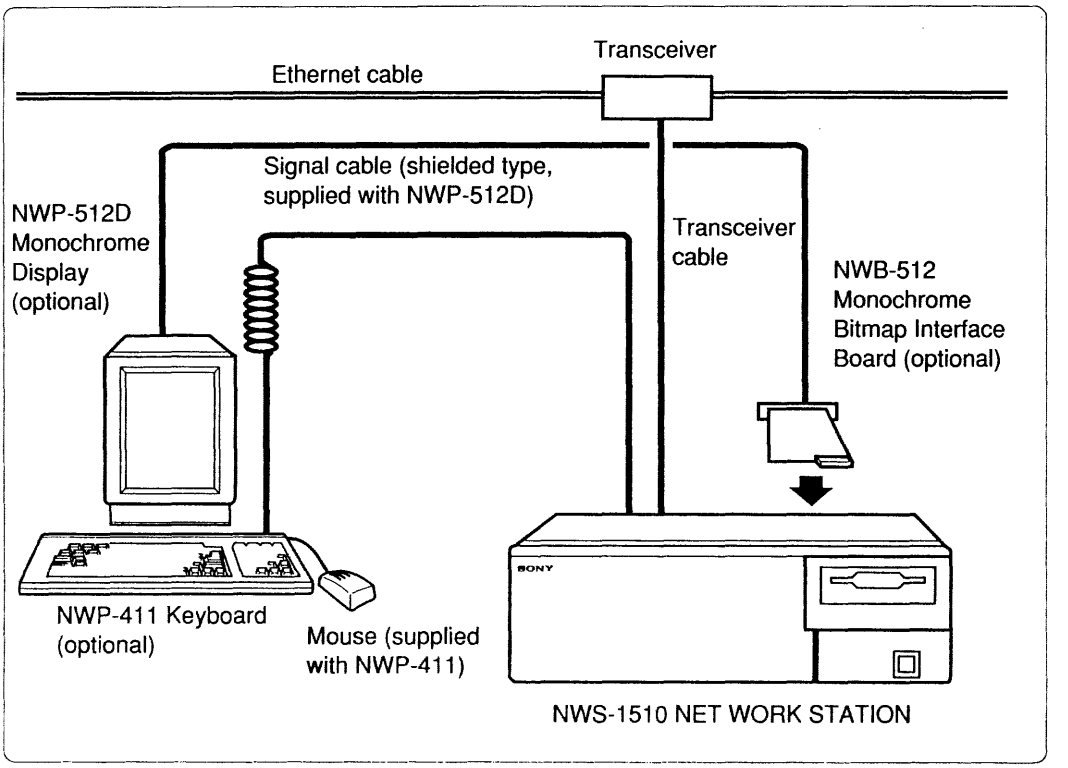
* (when formatted)

1) UNIX is a registered trademark of AT&T in the U.S.A. and other countries.
2) Ethernet is a trademark of Xerox Corporation.

Setting up the NEWS System

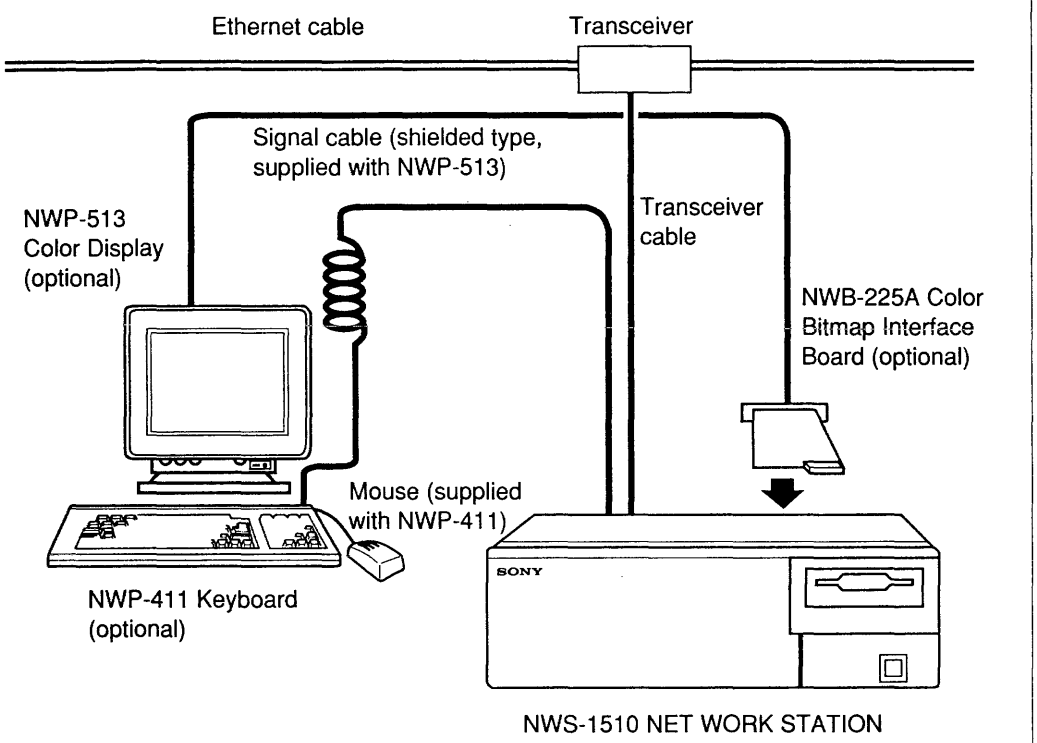
The NEWS system can be used for a variety of applications when combined selectively with one or more of the peripheral devices available. The following are examples of system configuration.

Monochrome Display System (NWS-1510 only)

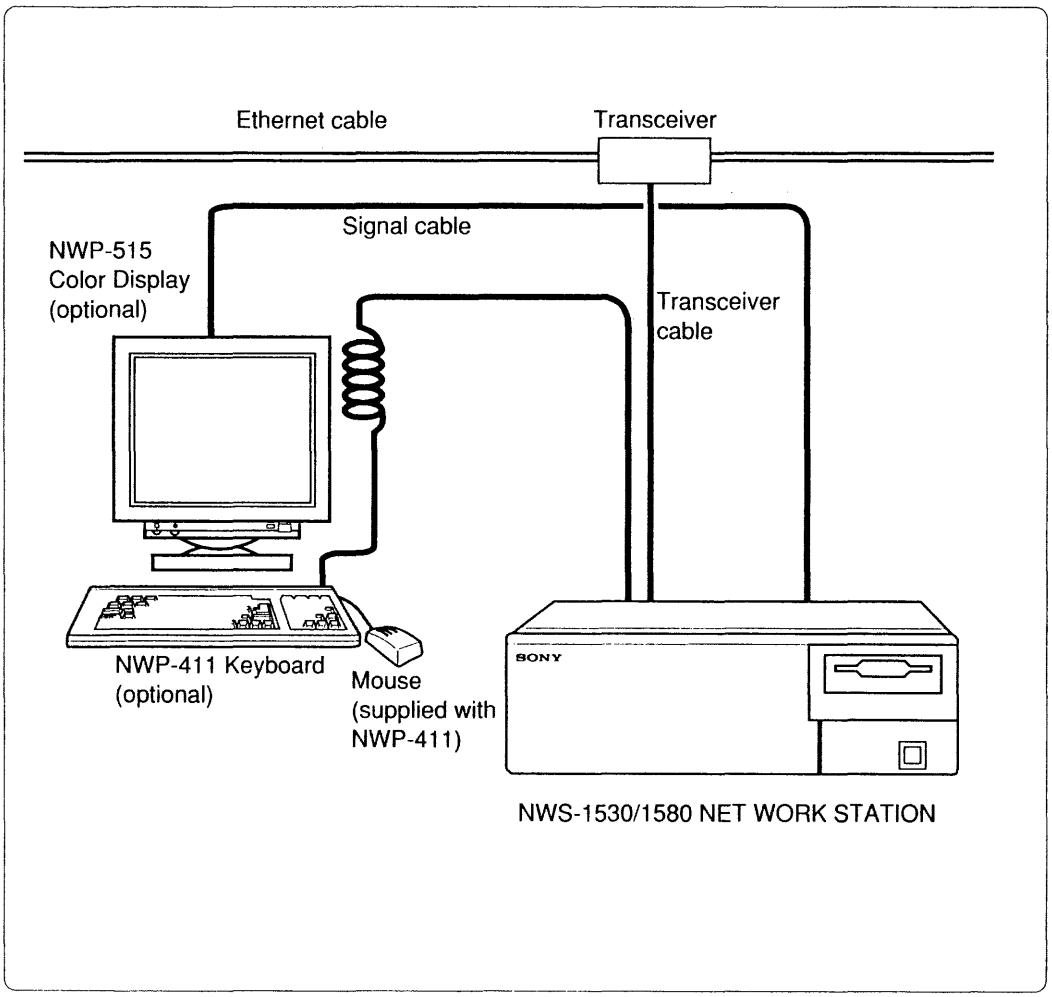


When using the workstation as a standalone system, no Ethernet transceiver is required.

Color Display System (NWS-1510 only)



Color Display System (NWS-1530/1580)



Peripheral Devices

The following optional board cannot be installed in the NWS-1510/1530/1580 because of the incompatible board height.

- NWB-232A GP-IB Interface Board

For more details, contact your authorized Sony representative for assistance.

Precautions

Safety

- The unit operates on 220-240V AC, 50 Hz.
- Should any solid object or liquid fall into the cabinet, keyboard or mouse, unplug the unit and have it checked by qualified personnel before operating any further.
- Unplug the unit from the wall outlet if it is not to be used for an extended period of time.
- To disconnect the cord, pull it out by the plug. Never pull the cord itself.
- Do not share the AC outlet with any other power-consuming equipment such as copying machines or shredders.
- Connect all power cables of the unit and its peripheral equipment to the same AC supply line. AC derived from different supply lines may result in voltage differences which can cause unwanted weak currents at the time of connection or unstable operation.

Installation

- The NET WORK STATION, keyboard and mouse consist of high-precision electronic parts. Do not drop or bump them against other objects. Do not place them in locations subject to vibration or on an unstable base.
- Do not install the unit near heat sources such as radiators or air ducts, or in a place subject to direct sunlight, excessive dust and/or moisture.
- Do not place electronic equipment near the computer. The computer's electromagnetic field may cause them to malfunction.
- The computer uses high frequency radio signals and may cause interference to radio or TV reception. Should this occur, relocate the computer a suitable distance away from the set.
- Provide adequate air circulation to prevent internal heat build-up. Do not place the unit on loose surfaces (rugs, blankets) or near materials (curtains, draperies) that may block its ventilation slots.
- Use only specified peripheral equipment or interface cables; otherwise, problems may result.
- When moving the unit, insert the supplied yellow protection sheet to the floppydisk drive.
- Do not place anything on the opened front cover. The front cover cannot sustain extra loads.

Cleaning

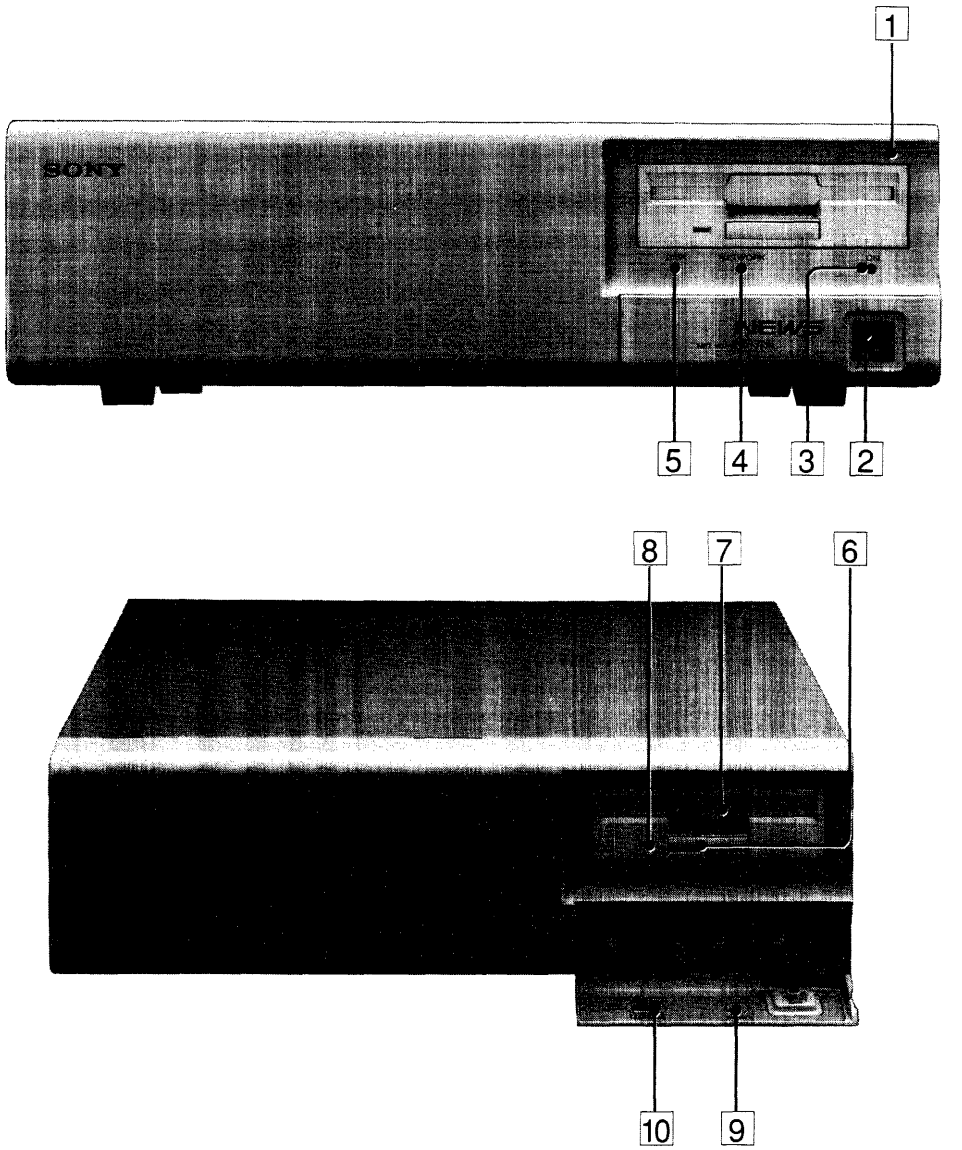
- Clean the cabinet with a soft, dry cloth, or a soft cloth lightly moistened with a mild detergent solution. Do not use any type of solvent, such as alcohol or benzine, as this may damage the finish.

Notes on Moisture Condensation

If the unit is brought directly from a cold to a warm location, moisture may condense inside the unit. In this case, allow more than one hour before turning on the unit.
Remove the floppydisk immediately when there is any sign of moisture condensation.

Location and Function of Parts and Controls

Front



[1] **Front cover**
Open this front cover when operating the POWER OFF/RESET switch [9] or the DIP switches [10] during initial setting, or using the floppydisk drive.

[2] **POWER switch**
Push to turn on the unit. Keep it depressed for more than two seconds until the POWER indicator lights up.
You cannot turn the power off with this switch. To turn the power off, use the appropriate ROM monitor system or operating system command.

[3] **POWER indicator**
Lights up green when power to the unit is on.

[4] **NETWORK indicator**
Lights up orange when the Ethernet controller receives or transmits a packet.

[5] **DISK indicator**
Lights up red when the processor is accessing the built-in hard disk or the external storage device connected to the SCSI bus.

[6] **Floppydisk eject button**
Push to eject a floppydisk from the floppydisk drive. For inserting and ejecting floppydisks, follow the instructions of the software in use. For details, refer to your software manual.

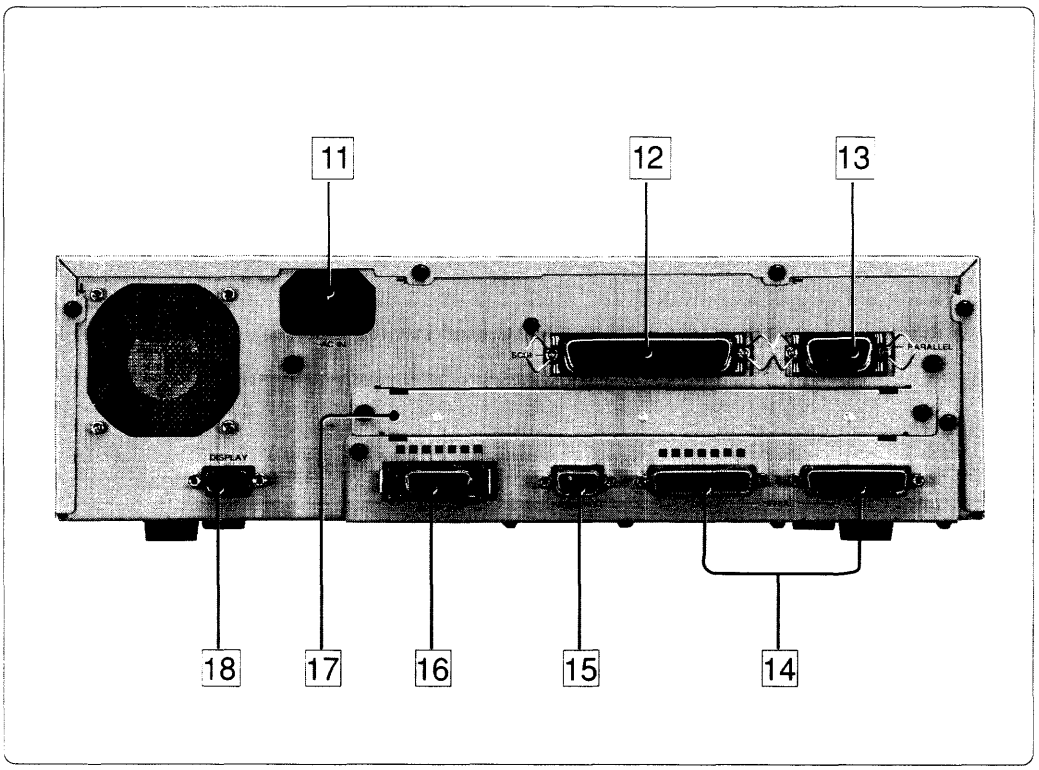
[7] **3.5-inch floppydisk drive**
Floppydisks are inserted into this slot.

[8] **Floppydisk IN-USE indicator**
Lights when data on the inserted floppydisk is accessed. **Do not eject the floppydisk while this indicator is lit. Data stored on the floppydisk may be destroyed.**

[9] **POWER OFF/RESET switch**
Used to forcibly turn off power to the unit. In normal use software commands should be used to turn off power to the unit.
To reset the CPU, push this switch while holding down the POWER switch [2]. After releasing this switch, keep the POWER switch depressed (for about two seconds) until the POWER indicator lights up again.

[10] **DIP switches**
Set these switches to designate the type of the connected display, the OS booting device, and the starting program at power on. Refer
to page 1-9 and 1-10 for setting instructions.

Rear



11 **AC inlet**
Connect to an AC outlet (AC 220–240V) with the supplied power cord.

12 **SCSI bus connector**
Connect an external storage device for expansion.

13 **PARALLEL port connector**
Connect a printer equipped with a Centronics interface.

14 **SERIAL port connector**
Connect a computer terminal, a modem or a printer equipped with an RS-232C interface. There are two channels: CH0 and CH1.

15 **KEYBOARD connector**
Connect an optional keyboard. Signals from the mouse are also input to this connector through the keyboard.

16 **NETWORK connector**
Connect an Ethernet transceiver.

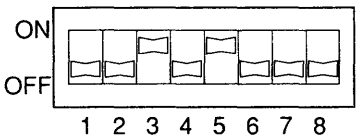
17 **Expansion I/O slot**
Insert optional boards, such as a bitmap interface board, into this slot.

18 **DISPLAY connector** (NWS-1530/1580 only)
Connect the signal cable from NWP-515.

DIP Switch Setting

This section explains the setting of the DIP switches located in the front cover. Be sure to set them properly before operating the unit.

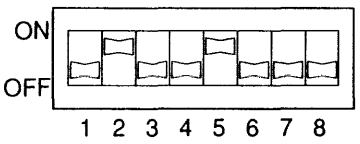
DIP switches (Open the front cover to access.)



NWS-1510 only

<table>
<tr><td>Switch 1–3</td><td>Console setting bits
<table>
<tr><td colspan="3">Switch</td><td rowspan="2">Function</td></tr>
<tr><td>1</td><td>2</td><td>3</td></tr>
<tr><td>OFF</td><td>OFF</td><td>OFF</td><td>Console is an ANSI standard terminal (9600 bps, 8 bits, no parity, 1 stop bit) connected to the serial port CH0.</td></tr>
<tr><td>OFF</td><td>OFF</td><td>ON</td><td>Console is a monochrome bitmap display (Using NWB-512 and NWP-512D)</td></tr>
<tr><td>ON</td><td>OFF</td><td>OFF</td><td>Console is a color bitmap display (Using NWB-225A and NWP-513)</td></tr>
<tr><td>ON</td><td>ON</td><td>ON</td><td>Provided for future system expansion</td></tr>
</table></td></tr>
<tr><td>Switch 4</td><td>Selects the OS booting device during autoboot.
ON: Floppydisk
OFF: Hard disk</td></tr>
<tr><td>Switch 5</td><td>Sets the starting program at power on.
ON: Autoboot
OFF: Monitor</td></tr>
<tr><td>Switch 6</td><td>Must be set to OFF.
(The unit does not operate when this switch is set to ON.)</td></tr>
<tr><td>Switches 7 and 8</td><td>Reserved</td></tr>
</table>

DIP switches (Open the front cover to access.)



Both NWS-1530 and NWS-1580

<table>
<tr><td>Switch 1–3</td><td>Console setting bits</td></tr>
<tr><td colspan="2"><table>
<tr><td colspan="3">Switch</td><td rowspan="2">Function</td></tr>
<tr><td>1</td><td>2</td><td>3</td></tr>
<tr><td>OFF</td><td>ON</td><td>OFF</td><td>Cannot be altered. The system does not function when these switches are set otherwise.</td></tr>
</table></td></tr>
<tr><td>Switch 4</td><td>Selects the OS booting device during autoboot.
ON: Floppydisk
OFF: Hard disk</td></tr>
<tr><td>Switch 5</td><td>Sets the starting program at power on.
ON: Autoboot
OFF: Monitor</td></tr>
<tr><td>Switch 6</td><td>Must be set to OFF.
(The unit does not operate when this switch is set to ON.)</td></tr>
<tr><td>Switches 7 and 8</td><td>Reserved</td></tr>
</table>

SCSI Bus Connection

Address Setting

The NEWS system employs the SCSI (Small Computer System Interface) bus for connection between the workstation and its peripheral devices such as NWP-532. The SCSI bus is an 8-bit parallel interface bus specified by ANSI standard X3.131-1986, allowing connection of up to eight SCSI controllers per system. In the NEWS system, each peripheral device has one SCSI controller. In addition to the workstation itself, the built-in hard disk drive has one controller.

Each controller has a unique SCSI bus address so as to prevent errors in daisy chain connections. When using more than one peripheral device, follow instructions so as to avoid address duplication.

SCSI address	NWS-1510/1530/1580
0	Reserved (built-in hard disk)
1	
2	
3	
4	
5	
6	
7	Reserved (workstation)

- As indicated in the table above, the addresses for the unit and built-in drive are already set as follows.

  Address of workstation 7
  Address of built-in hard disk 0

  Do not allocate these addresses to external units.

- For details on address setting procedures, refer to the operating manual of each unit to be connected.

Memory Expansion

The main memory of this unit can be expanded in 4M-byte units up to 16M bytes using the optional NWA-028 4MB Expansion RAM Kit. For installation of the expansion RAM board and RAM Kit, contact your authorized Sony representative for assistance. (There is a charge for this service.)

Note

NWA-029 4MB Expansion RAM Kit cannot be used for this unit.

Specifications

Processor

Main processor	MC68030RC25
Clock frequency	25MHz
Wait for fetch	Two waits for main memory
On-chip MMU	
Floating point co-processor	MC68882RC25
Clock frequency	25MHz

Memory

Main memory	4M bytes (standard) Expandable up to 16M bytes
Buffer memory for Ethernet	16K bytes
Battery backed- up memory	2040 bytes
Display memory	1M bytes (NWS-1530/1580 only)

External Storage Device

Floppydisk drive	
Disk used:	3.5-inch micro floppydisk 2M-byte or 1M-byte type (unformatted)
Hard disk drive	40M bytes (formatted, NWS-1510/1530) 170M bytes (formatted, NWS-1580)

I/O Interface

SCSI bus	50-pin connector ANSI SCSI standard X3.191-1986
PARALLEL port	14-pin connector Centronics 8-bit parallel interface
SERIAL ports (2 ports)	25-pin connector EIA RS-232C interface Maximum baud rate: 9600 bps (when internal clock is used) Asynchronous and synchronous transmission External clock is usable
NETWORK port	15-pin connector 10M bps Ethernet transceiver interface
Keyboard/mouse interface	9-pin connector TTL level serial transfer
Expansion slot	Expansion I/O board connector
DISPLAY port (NWS-1530/1580 only)	15-pin connector

DISPLAY (NWS-1530/1580 only)

Displayed area	1024 (horizontal) x 768 (vertical) pixels
CLUT function (Color Look Up Table)	Displays 256 colors selectd from approx. 16.7 million colors
Output (Adjusted to NWP-515 Color Display)	
RGB video signal (75 ohms) with the separated sync signal	
R/G/B signal	0.714 Vp-p positive
H/V signal	TTL level
Scanning frequency	Horizontal: 48.78 KHz Vertical: 60.0 Hz

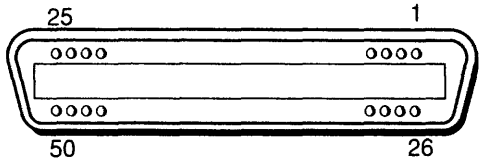
General

Power requirement	220 – 240V AC ±10%, 50 Hz
Current drain	1A
Operating conditions	
Temperature:	10°C to 35°C (50°F to 95°F)
Humidity:	30% to 70% (no condensation)
Storage conditions	
Unpacked	
Temperature:	5°C to 50°C (41°F to 122°F)
Humidity:	20% to 90% (no condensation)
Packed	
Temperature:	–20°C to 60°C (–4°F to 140°F)
Humidity:	20% to 90% (no condensation)
Dimensions	355 x 100 x 341 mm (w/h/d) (14 x 4 x 13 5/12 inches) excluding projecting parts and rubber legs
Weight	Approx. 10.0 kg (22 lb)

Note
This appliance conforms with EEC Directives 76/889 and 82/499 regarding interference suppression.

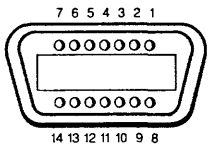
Pin Assignment

SCSI bus connector
(ANSI SCSI standard X3.131-1986)



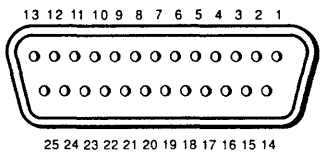
Pin No.	Signal	Pin No.	Signal
1	GND	26	DB0
2	GND	27	DB1
3	GND	28	DB2
4	GND	29	DB3
5	GND	30	DB4
6	GND	31	DB5
7	GND	32	DB6
8	GND	33	DB7
9	GND	34	DBP
10	GND	35	GND
11	GND	36	GND
12	GND	37	GND
13		38	+ 5V
14	GND	39	GND
15	GND	40	GND
16	GND	41	ATN
17	GND	42	GND
18	GND	43	BSY
19	GND	44	ACK
20	GND	45	RST
21	GND	46	MSG
22	GND	47	SEL
23	GND	48	C/D
24	GND	49	REQ
25	GND	50	I/O

PARALLEL port connector
(Centronics 8-bit parallel interface)



Pin No.	Signal	Pin No.	Signal
1	STRB	8	D6
2	D0	9	D7
3	D1	10	
4	D2	11	BUSY
5	D3	12	
6	D4	13	FAULT
7	D5	14	GND

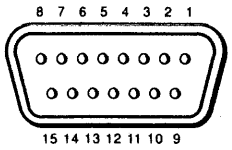
SERIAL port connector
(EIA RS-232C interface)



Pin No.	Signal	Pin No.	Signal
1	Frame GND	14	
2	TXD	15	TXclock (~~input~~)
3	RXD	16	
4	RTS	17	RXclock (input)
5	CTS	18	
6	DSR	19	
7	Signal GND	20	DTR
8	DCD	21	
9		22	RI
10		23	
11		24	
12		25	
13			

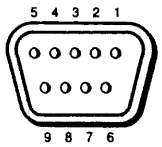
The pin assignment is common to channels 0 and 1.

NETWORK connector
(Ethernet interface)



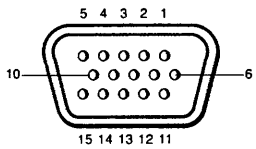
Pin No.	Signal	Pin No.	Signal
1	Shield	9	Collision –
2	Collision +	10	Transmit –
3	Transmit +	11	
4		12	Receive –
5	Receive +	13	Power
6	Return	14	
7		15	
8			

KEYBOARD connector
(TTL level serial interface)



Pin No.	Signal	Pin No.	Signal
1	+ 5V	6	Reserved
2	Buzzer	7	Mouse data
3	Key data	8	Power on
4	Reserved	9	
5	GND		

DISPLAY connector (NWS-1530/1580)
(Color bitmap interface)



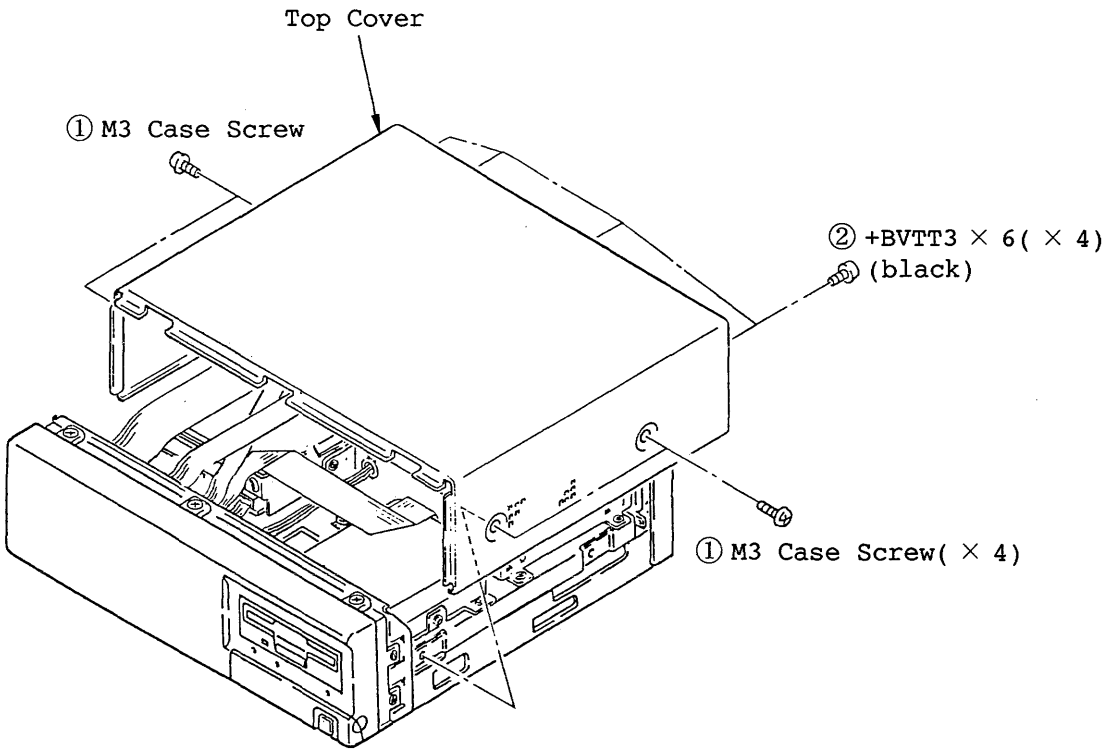
Pin No.	Signal	Pin No.	Signal
1	Red	9	
2	Green	10	Ground
3	Blue	11	
4		12	
5		13	Horizontal Sync
6	Red Return	14	Vertical Sync
7	Green Return	15	
8	Blue Return		

CHAPTER 2
REMOVAL

Perform the following removal in numerical order given.

2-1.

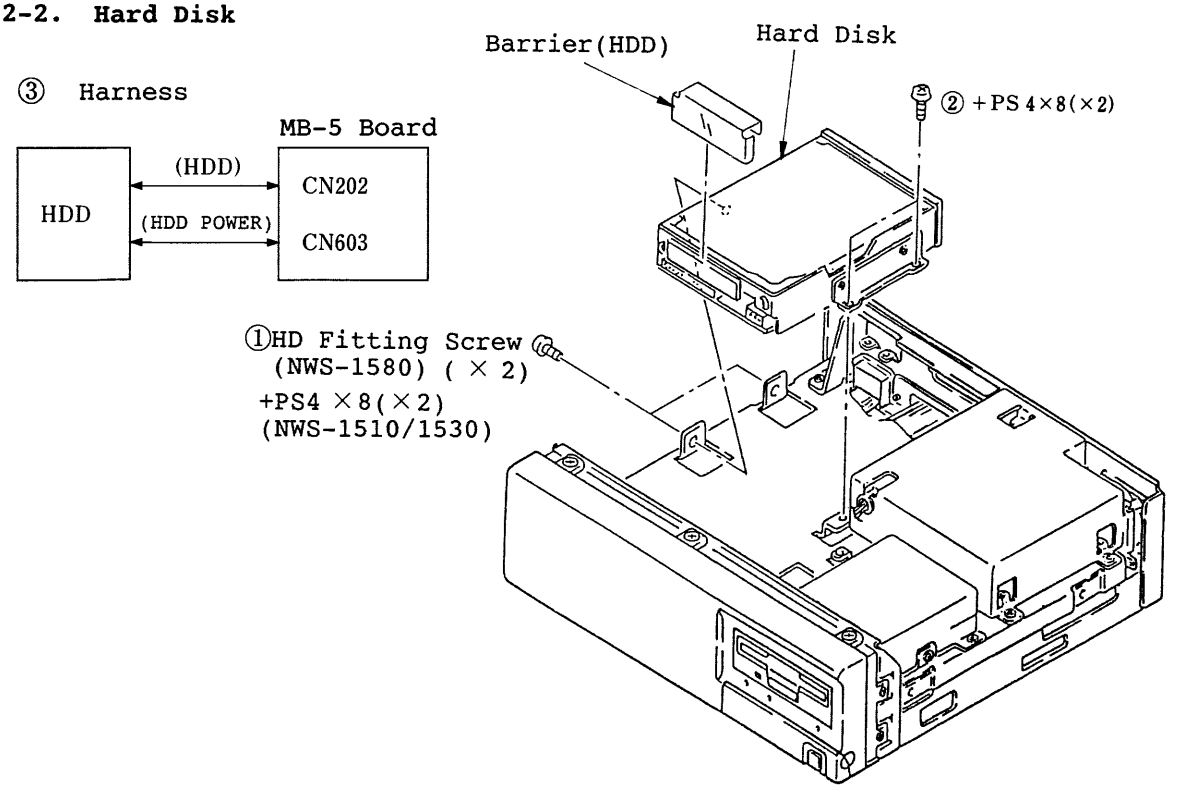
Top Cover



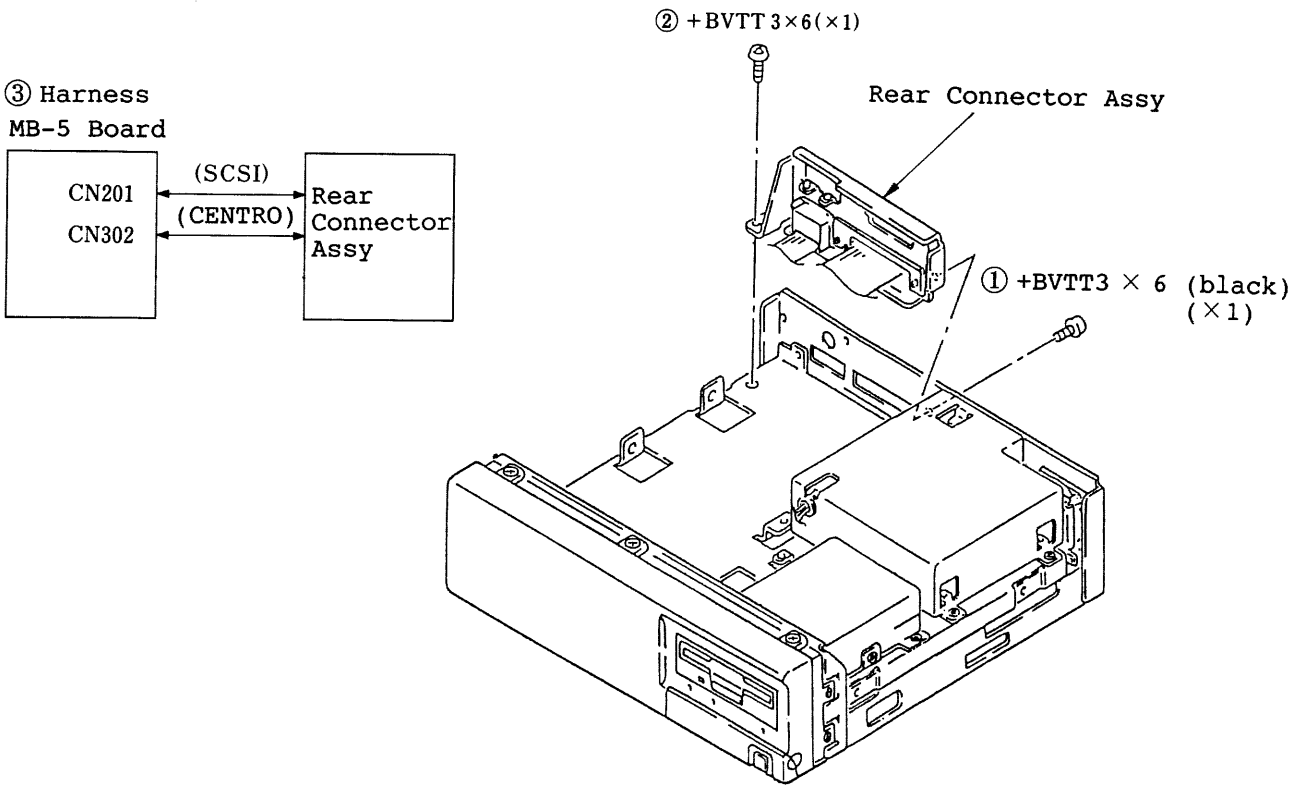
Cautions

- Before removal, be sure to unplug the unit.
- Do not drop HDD(Hard Disk Drive unit) or bump it against other objects.

2-2. Hard Disk

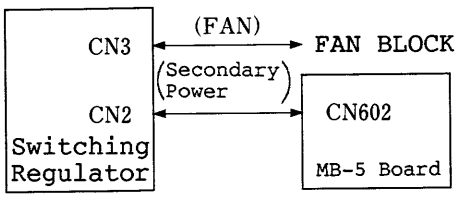


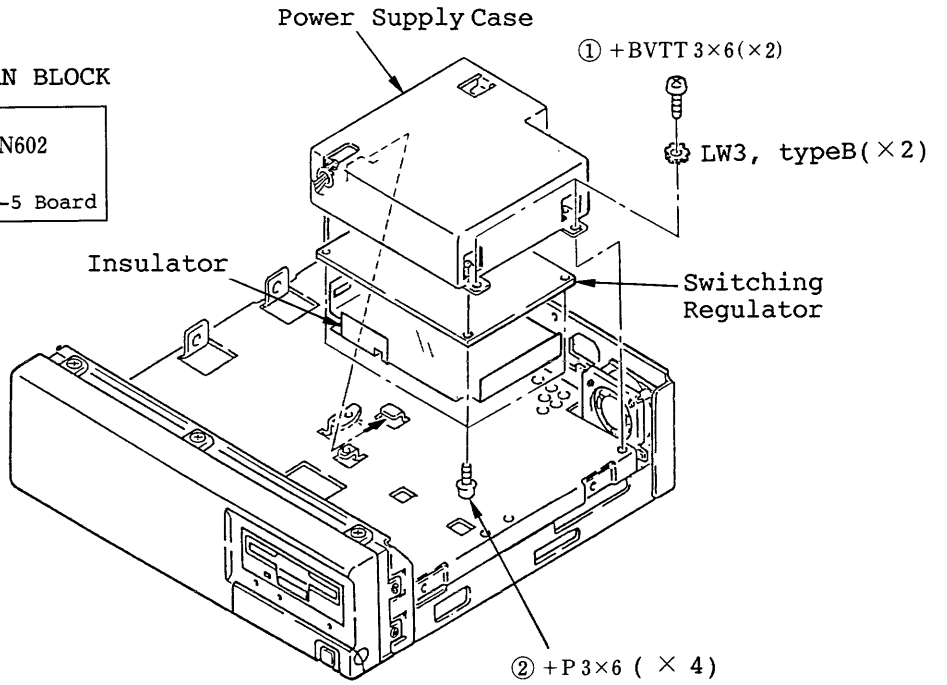
2-3. Rear Connector Assy



2-4. Switching Regulator

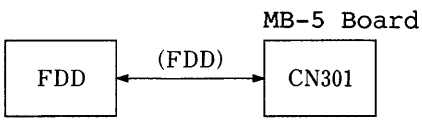
③ Harness

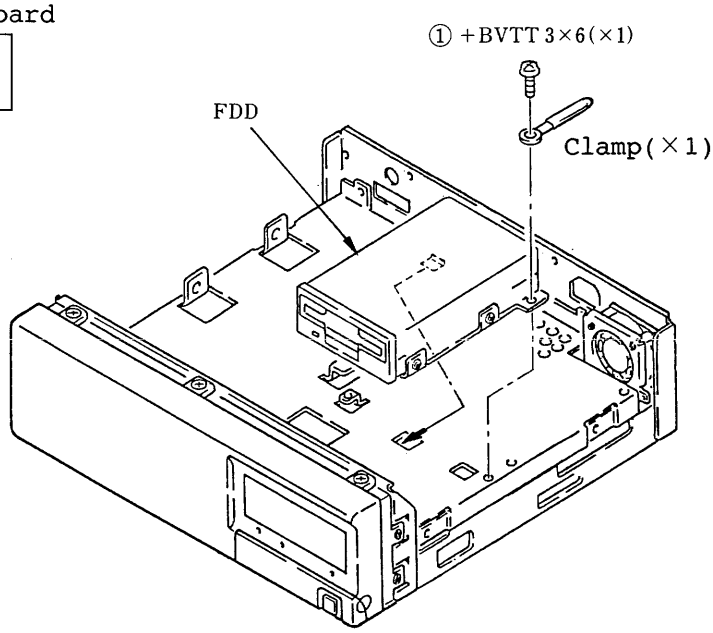




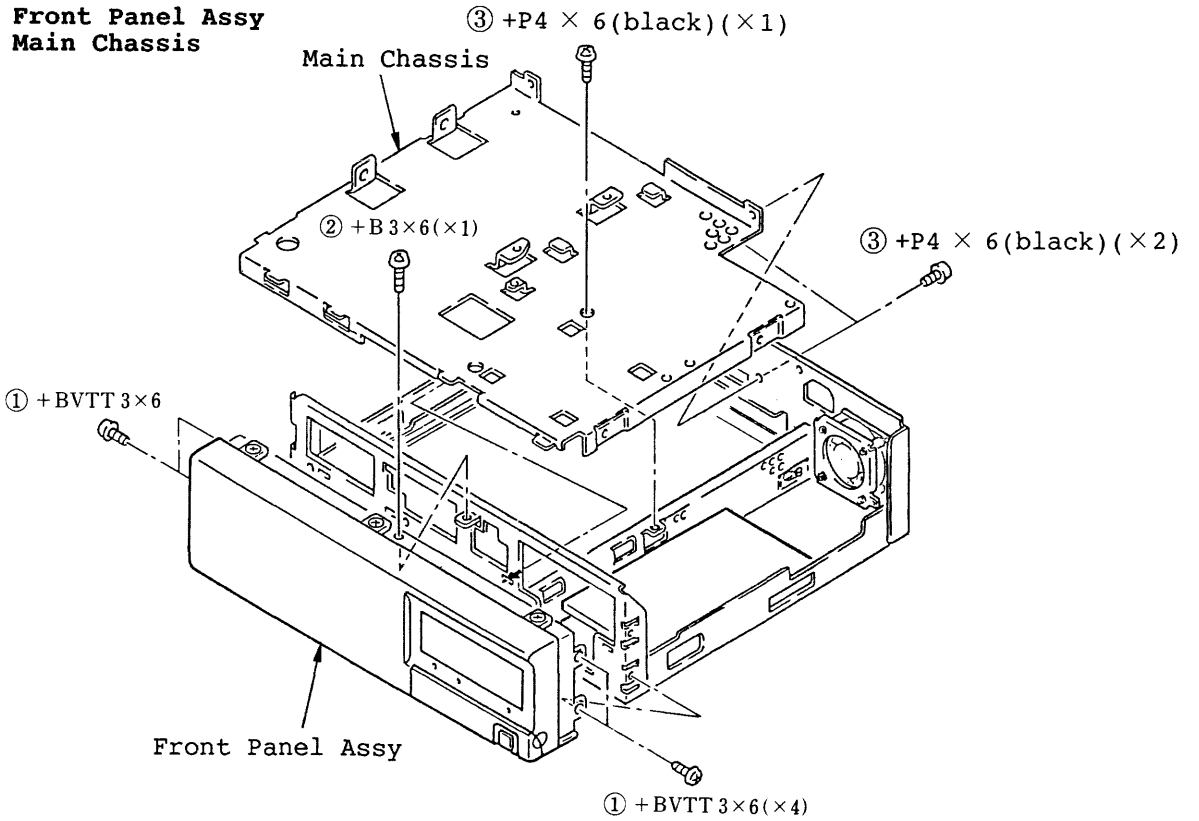
2-5.FDD

② Harness



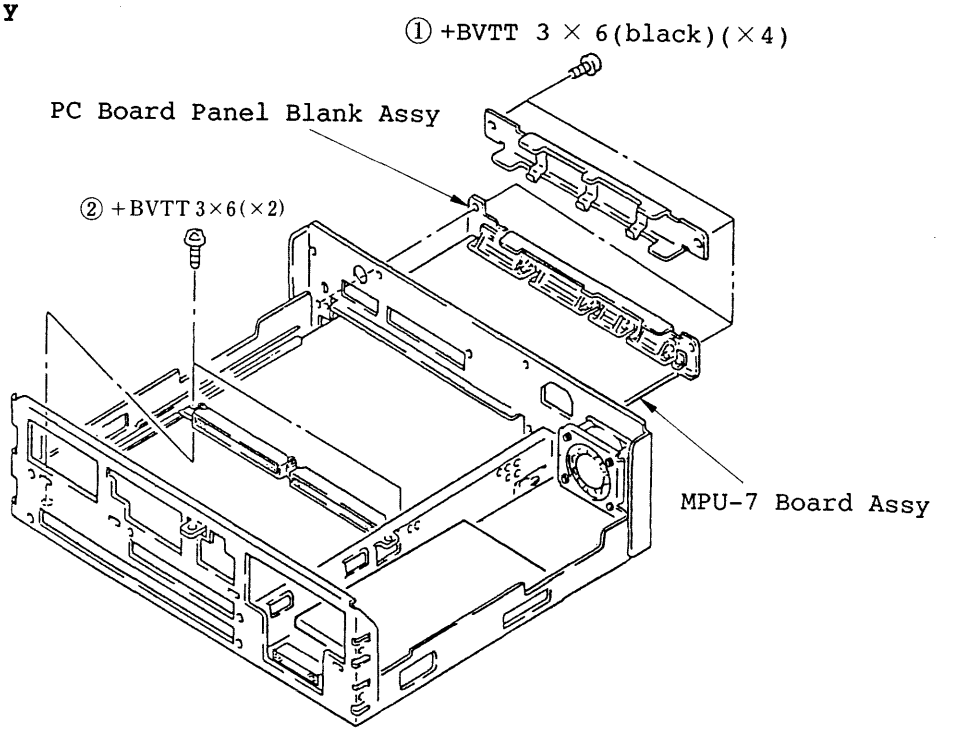


2-6. Front Panel Assy Main Chassis

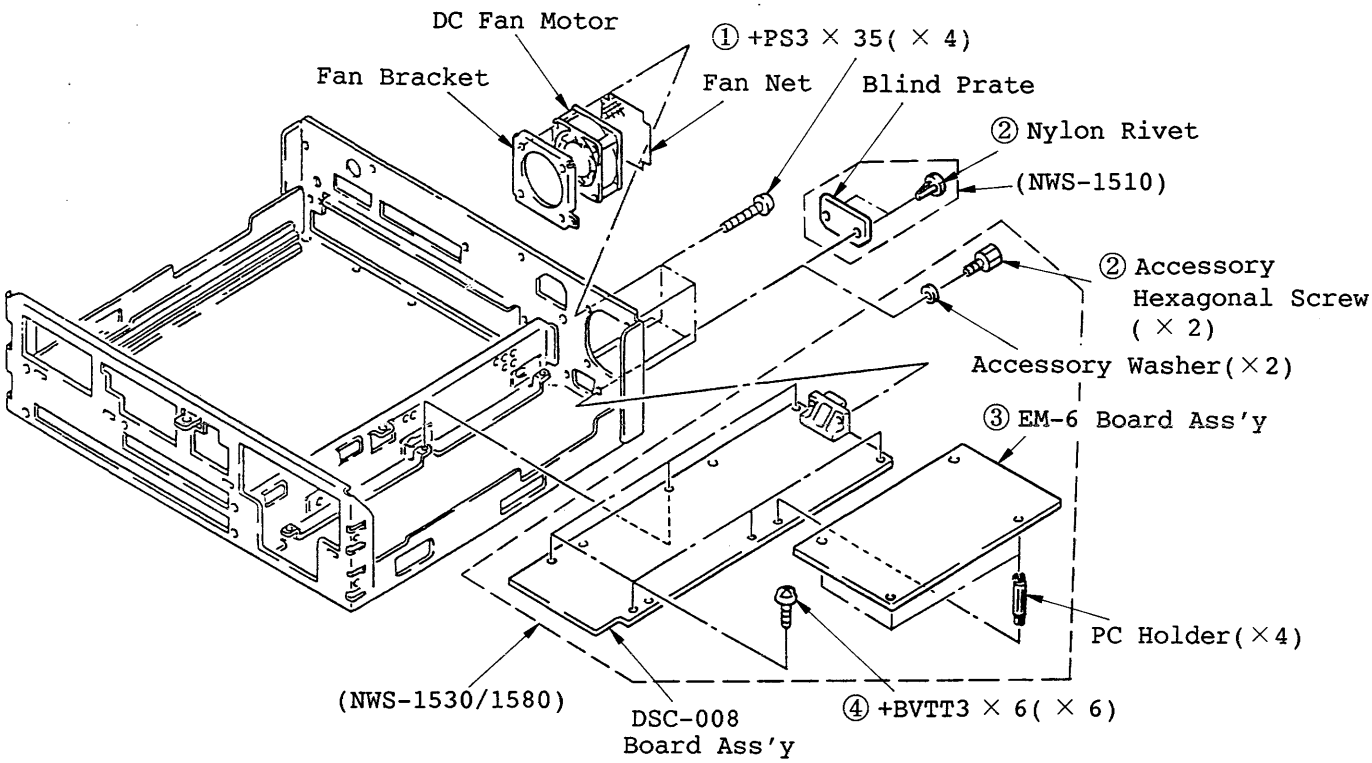


2-7. MPU-7 Board Ass'y

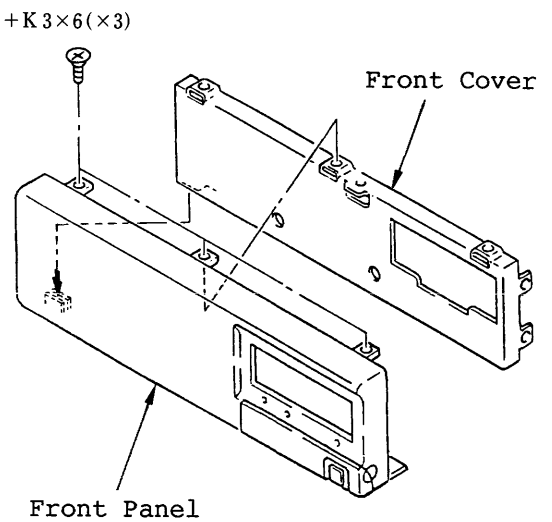
③ Harness
(See page 5-54)



2-8. DC Fan Motor
DSC-008Board Ass'y

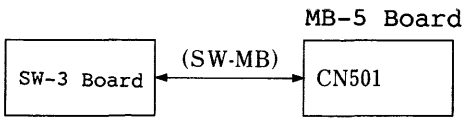


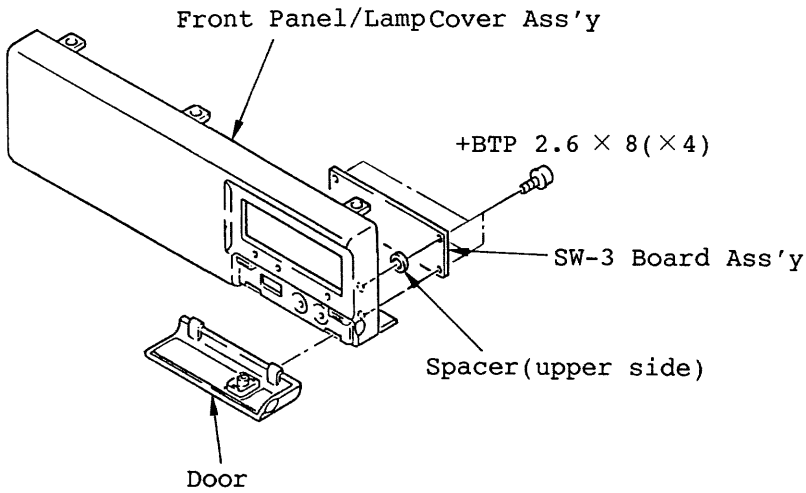
2-9. Front Cover



2-10. SW-3 Board Ass'y

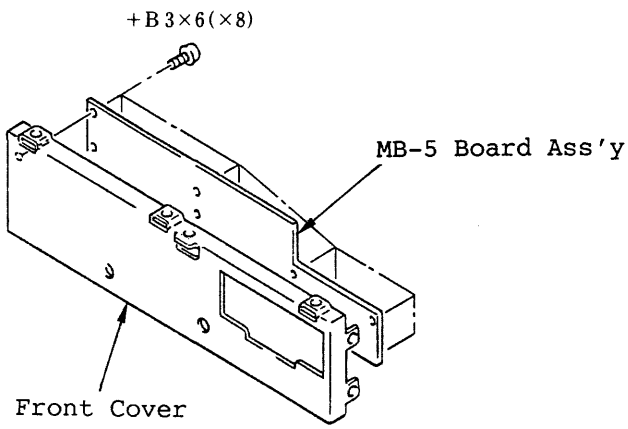
② Harness





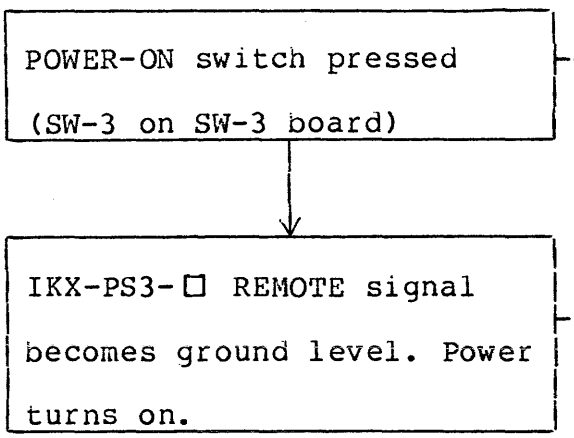
2-11. MB-5 Board Ass'y

②Harness
(See page 5-24)



CHAPTER 3
CIRCUIT DESCRIPTION

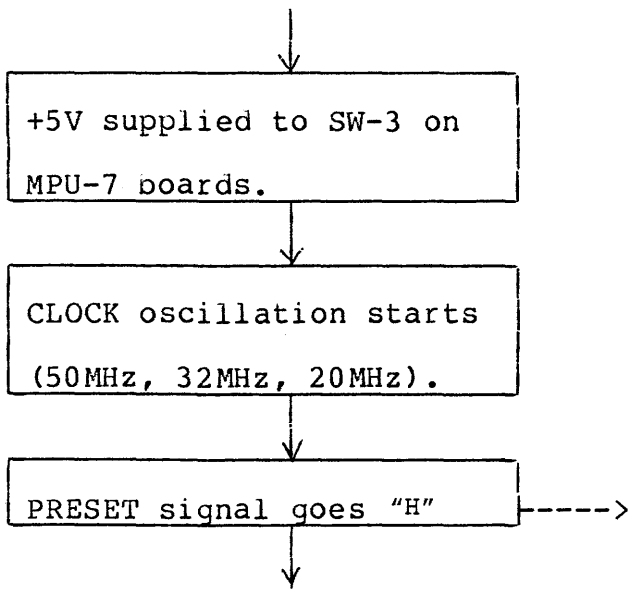
3-1. POWER ON SEQUENCE



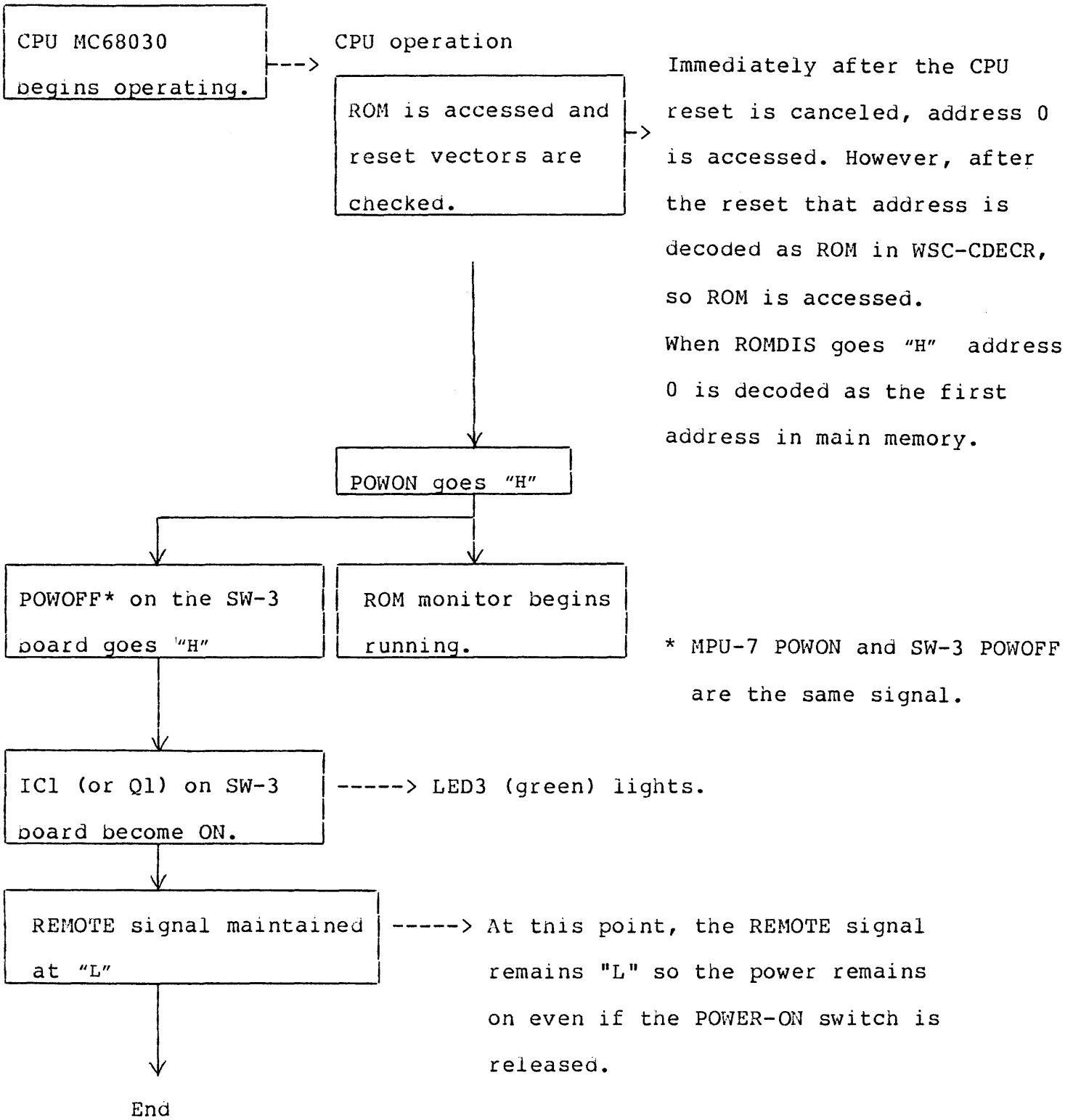
Must be pressed until [end] (approximately 2 seconds)

At this point, IC1 (or Q1) on the SW-3 board is off, so power is cut off if the POWER-ON switch is released.

* Power is supplied when the IKX-PS-□ REMOTE signal is at ground or TTL "L" level and cut off when it is OPEN or at TTL "H" level.

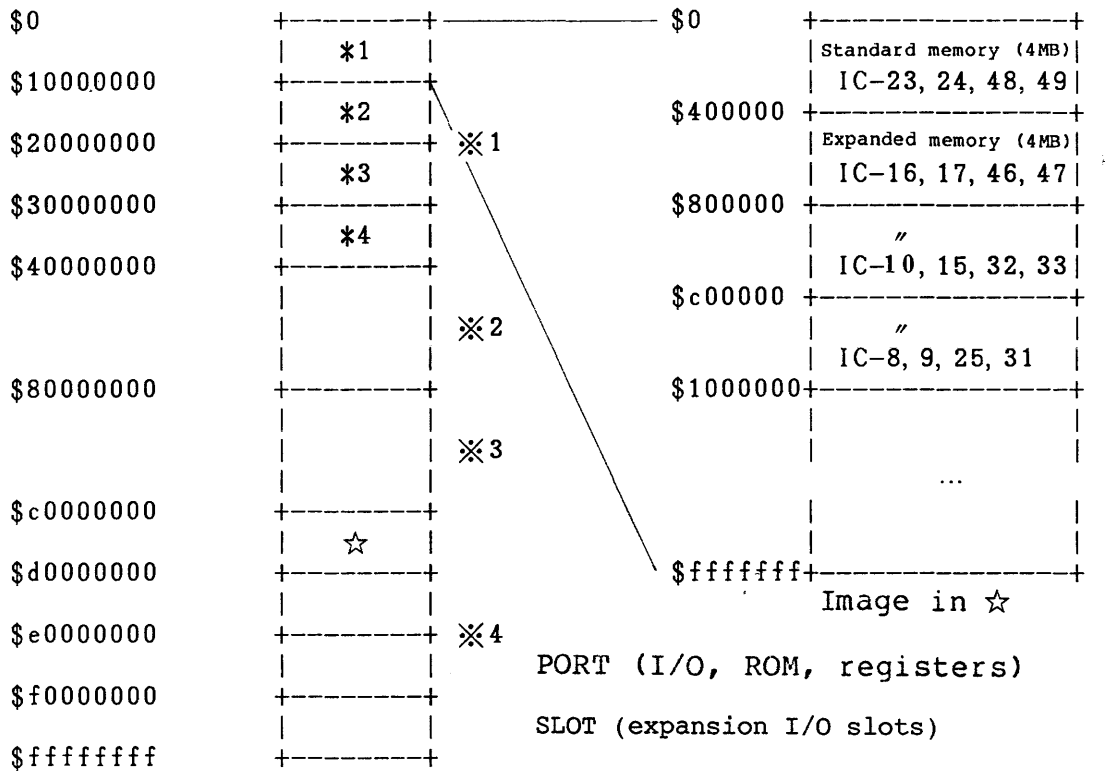


Output goes "H" approximately 1 second after +5V is supplied to IC77 (TL7705) on the MPU-7 board.


CPU MC68030 begins operating.
CPU operation
ROM is accessed and reset vectors are checked.
Immediately after the CPU reset is canceled, address 0 is accessed. However, after the reset that address is decoded as ROM in WSC-CDECR, so ROM is accessed.
When ROMDIS goes "H" address 0 is decoded as the first address in main memory.
POWON goes "H"
POWOFF* on the SW-3 board goes "H"
ROM monitor begins running.
* MPU-7 POWON and SW-3 POWOFF are the same signal.
IC1 (or Q1) on SW-3 board become ON.
-----> LED3 (green) lights.
REMOTE signal maintained at "L"
-----> At this point, the REMOTE signal remains "L" so the power remains on even if the POWER-ON switch is released.
End

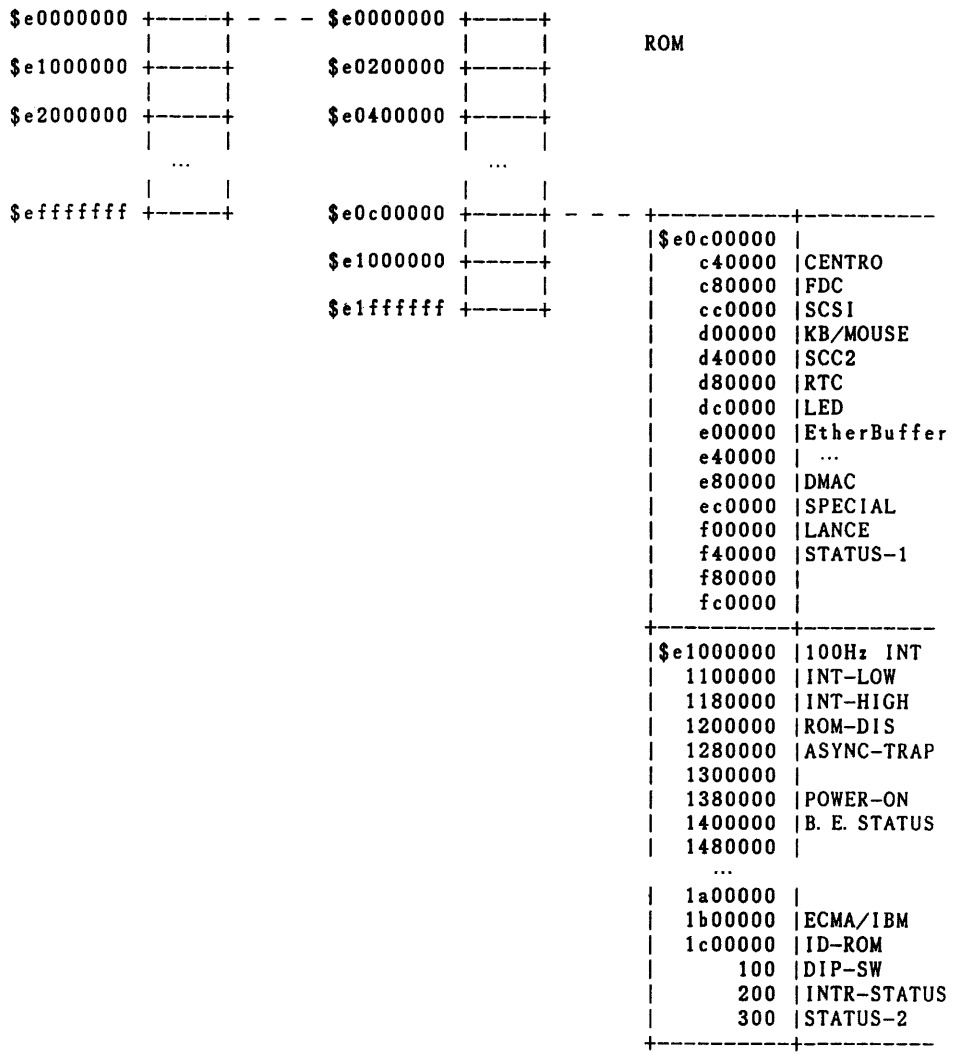
3-2. ADDRESS MAP

Addresses are as follows from the point of view of the CPU:



Addresses A31 and A30 are not used, the images from *1 - *4 appear as *2 - *4. The address space from $20000000 - $e0000000 is not used and addresses from $c0000000 and below are configured in software so that the MMU is not used, making direct access possible.

The PORT address map is given below:



3-3. CPU OPERATION

3-3-1. ROM Access

The ROM space is accessed in either of two cases. The first occurs after a CPU reset is canceled when the reset vectors are fetched. The second is when ROM monitor is being executed.

The first is a function identical to that used in 68000 type CPUs. It is a cycle to fetch the interrupt stack addresses for all addresses for the first command executed after the CPU reset is canceled. Bytes 0 to 4 of each address are the stack address and the next four bytes are the command address.

The second is a cycle carried out when commands written in ROM are read. The first ROM address is $e00000000.

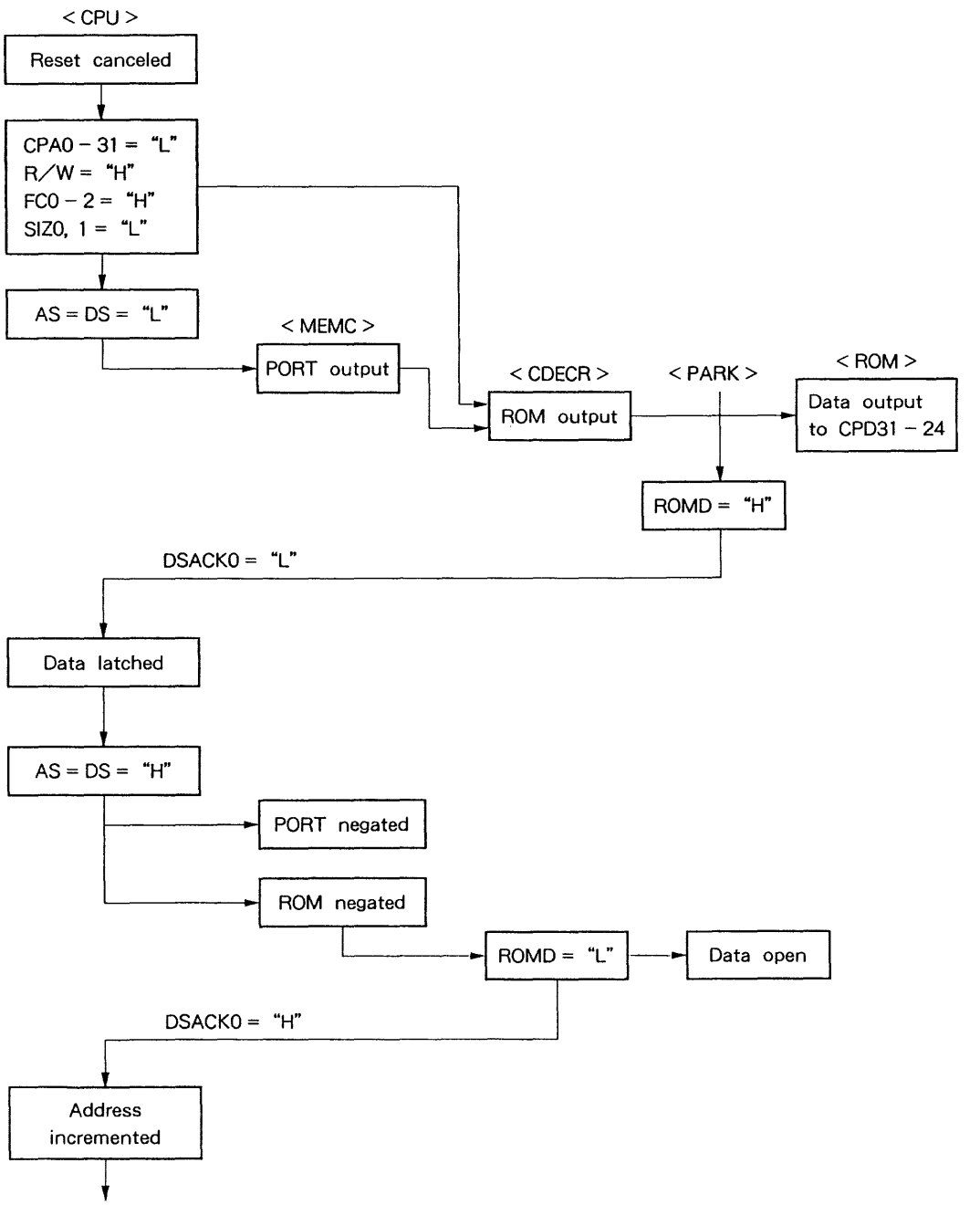
For either cycle, the ROM data width is only 8 bytes. Therefore, to access long words (32-bit) four readout cycles are required and for words (16-bit) two cycles. A flowchart of the various cycles is given below.

WSC-CDECR outputs the ROM access signal (ROM) when PORT output from WSC-MEMC is "L" and addresses A22, A23 and A24 are all "L" MEMC outputs PORT in either of two cases: 1) ROMDIS is "H" and AS is "L" 2) ROMDIS is "L" A29 is "H" and A28 is "L" 1) is for a reset vector fetch and 2) for normal ROM access.

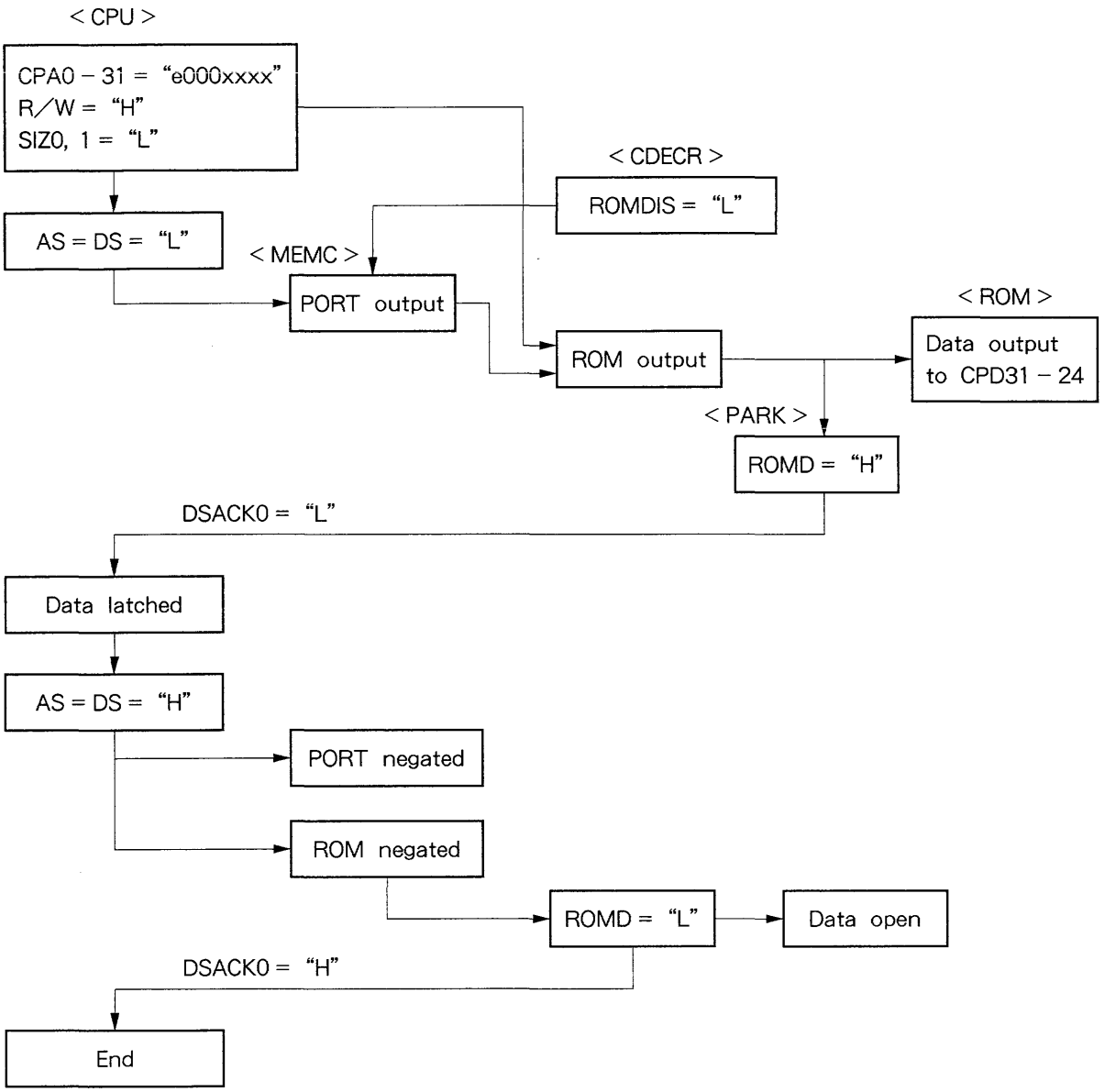
WSC-CDECR is output from ROMDIS. It can be either "H" because of a reset signal, or "L" when "1" is written to the CDECR

internal control register bit. Therefore, since the rest vector fetch is the first cycle after the reset is canceled, ROMDIS is always "H" and cycle 1) is executed.
When ROM monitor is executed, first POWON is set. Next, ROMDIS is cleared. Therefore, if address $e00000000 is subsequently accessed, ROM is output. When ROMD IS is "H" "L" access to A22, A23 or A24 is considered ROM access.

a) Reset vector fetch



b) ROM data readout



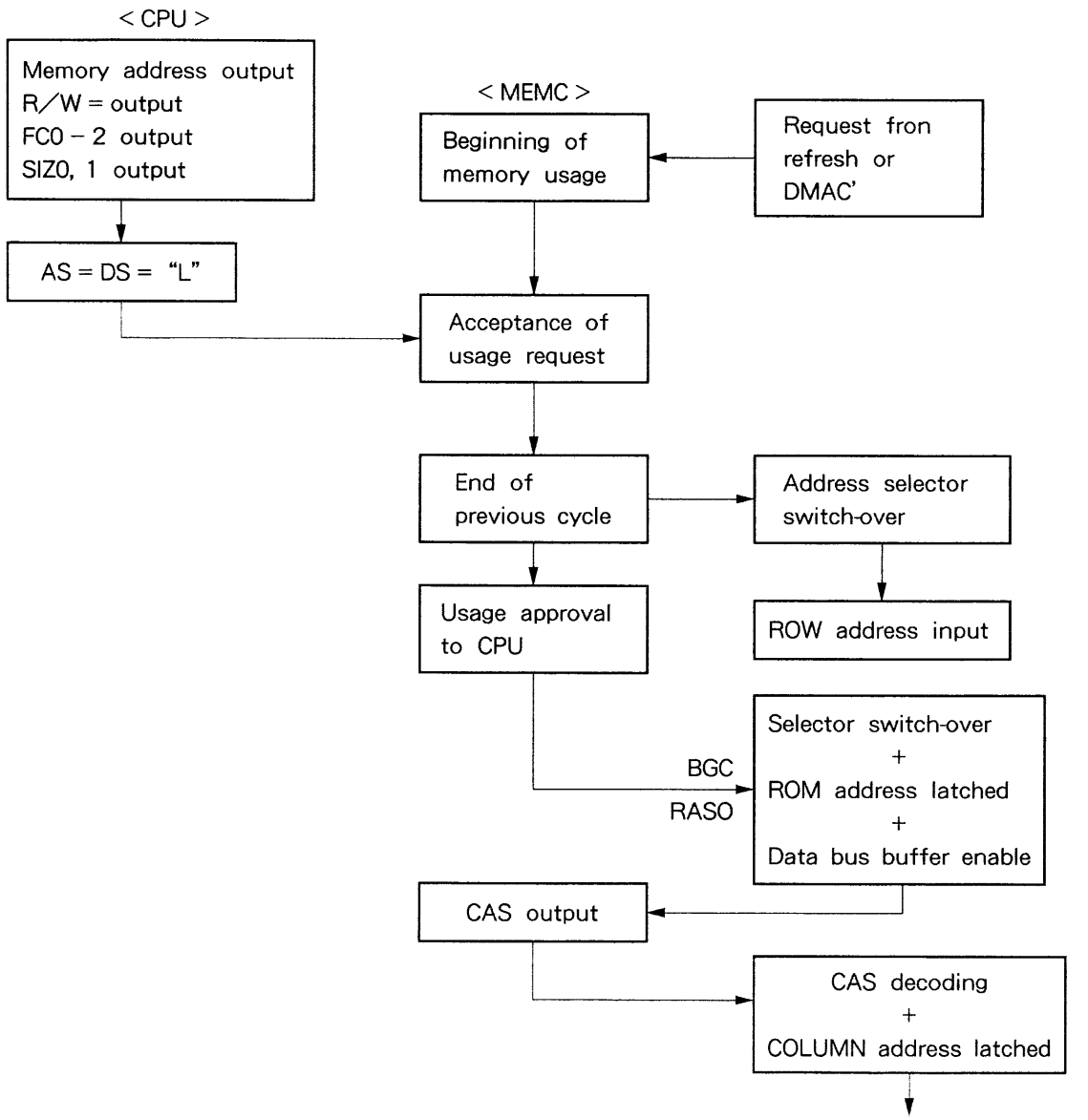
3-3-2. Main Memory Access

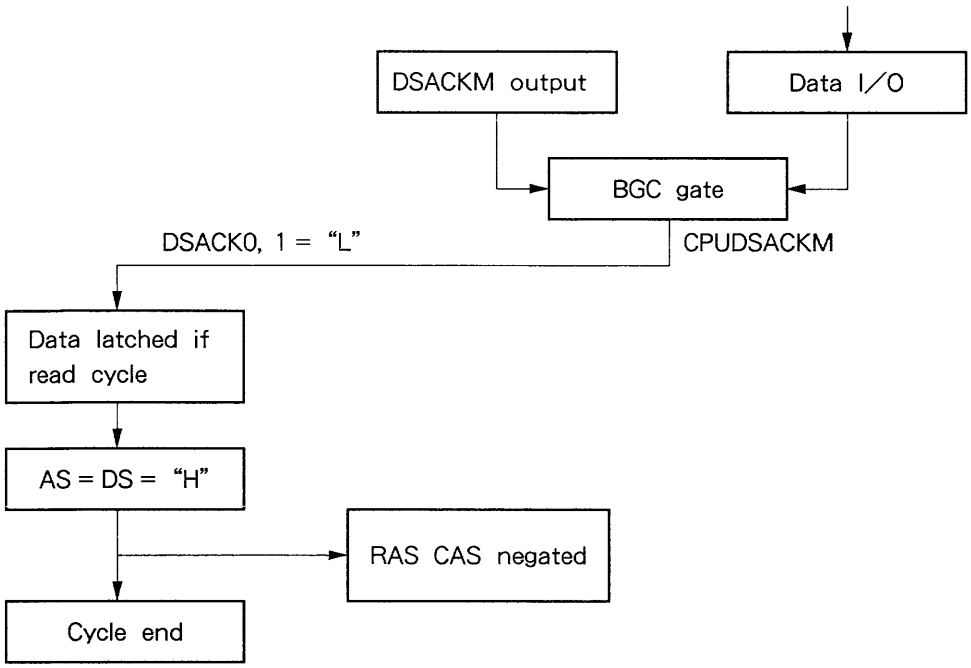
WSC-MEMC controls main memory access. Main memory is accessed by the CPU and DMAC (WSC-ICKDMAC), and WSC-MEMC controls these two and refreshes as well as the generation of arbitration signals RAS and CAS for DMAC register access by the CPU and the generation of the DSACK signal (to the CPU and DMAC). Here discuss memory access by the CPU.

Let us assume ROMDIS, output by WSC-CDECR, is reset to "L" If this signal is "H" an image of ROM appears in the first 4MB of main memory ($0 - $400000).

When the CPU accesses the main memory area, memory arbitration takes place within MEMC. If at this point DMAC or a refresh is using main memory, the COU must wait until that cycle has finished. When the cycle of the previous memory user has finished, RASO, 1 BRASO - 3 goes "H". If the previous memory user was DMAC, DMAG is "L" if it was a refresh, REFAL is "H". After this, the CPU cycle begins.

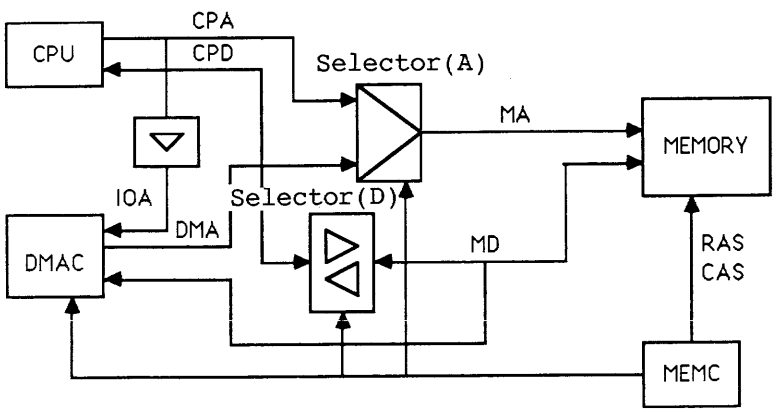
A flowchart of this process is given below.



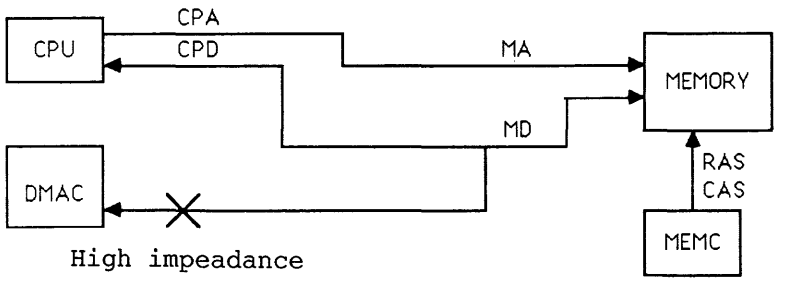


3-3-3. DMAC Access

The CPU accesses DMAC when the DMAC internal registers are read or written to. Data I/O is accomplished via DMAC D31 - D0 (the 32-bit bus connected to the memory. The diagram below shows the connection between the CPU, DMAC and memory.



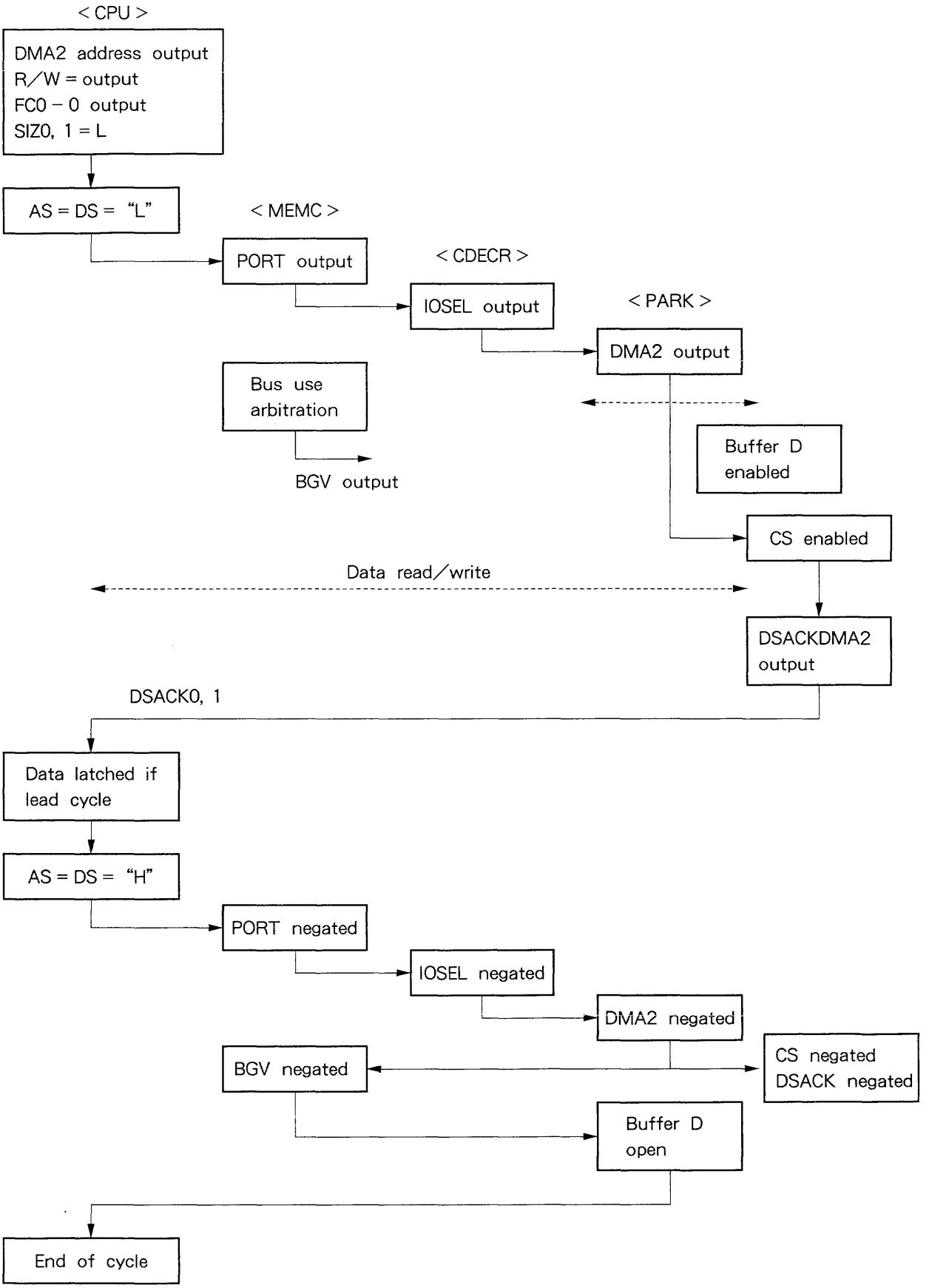
When the CPU accesses main memory, selector A switches from CPU to MA and the DMAC data line is opened.



The same type of bus can be used when the CPU accesses DMAC. However, when RAS/CAS are not output from MEMC, CPD switches to MD(DMA) when writing data to DMAC, and from to MD(DMA) to CPD when reading data. IOA is for specification of DMAC register addresses, RWO is for read/writes and DSACKDMA2 is for DSACK from DMAC.

The bus used by the CPU to access DMAC is the same type as that it uses to access main memory. Therefore, arbitration of bus usage is necessary between the CPU and DMAC memory. For this purpose, a MDA2 access decode signal is input to DMA, and BGV is output when main memory arbitration has been obtained. The logical product of DMA2 and BVG is input to the DMAC CS. BVG is also input to buffer D to initially enable it.

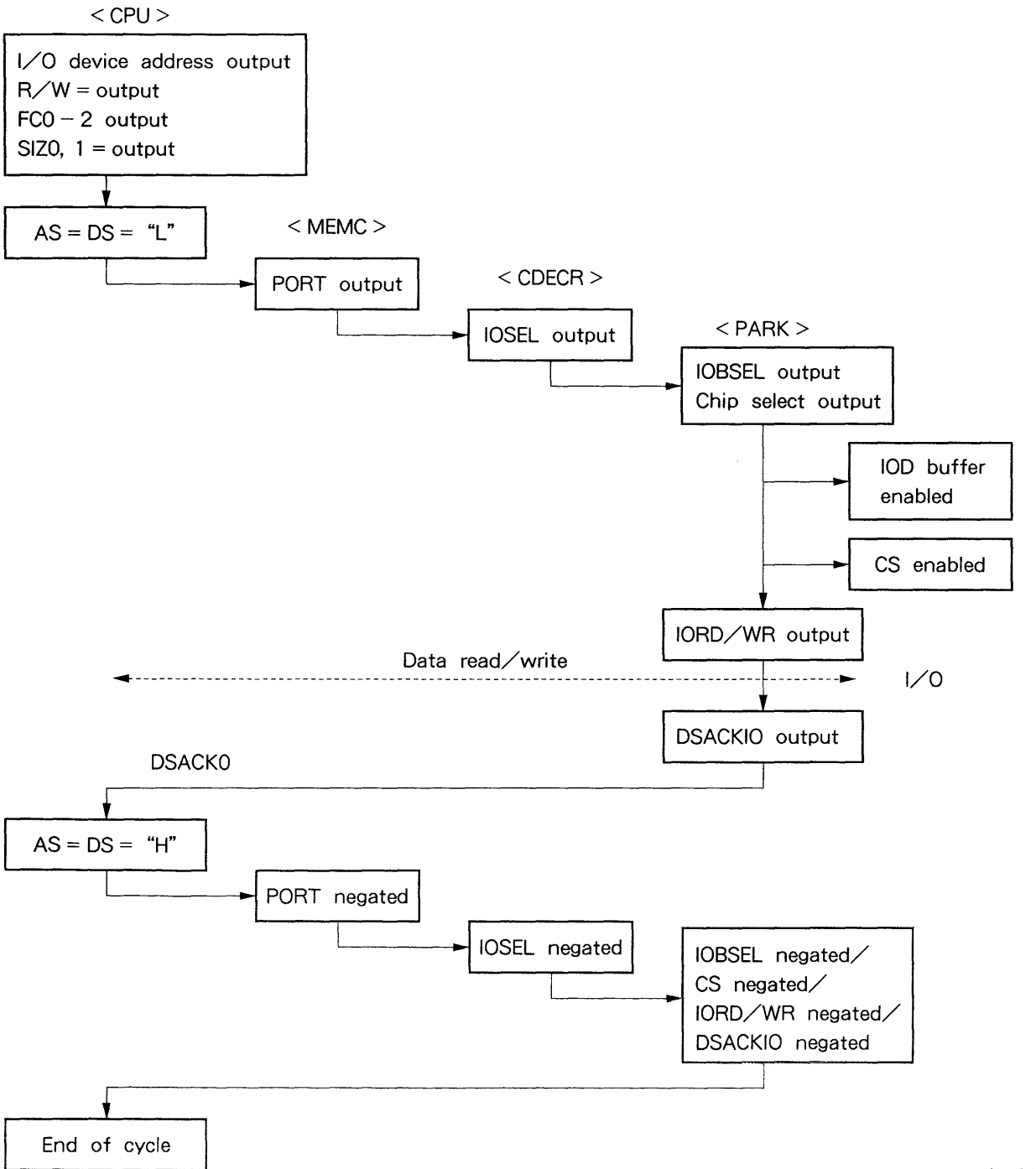
A flowchart of this process is given below.


< CPU >
DMA2 address output
R/W = output
FC0 – 0 output
SIZ0, 1 = L
AS = DS = "L"
< MEMC >
PORT output
< CDECR >
IOSEL output
< PARK >
DMA2 output
Bus use arbitration
BGV output
Buffer D enabled
CS enabled
Data read/write
DSACKDMA2 output
DSACK0, 1
Data latched if lead cycle
AS = DS = "H"
PORT negated
IOSEL negated
DMA2 negated
BGV negated
CS negated
DSACK negated
Buffer D open
End of cycle

3-3-4. GENERAL I/O Access

The general I/O access referred to here covers I/O devices connected to data bus IOD0 to IOD7 and accessed using the chip select signal output by WSC-PARK. The chip select signals and the devices they refer to are listed below.

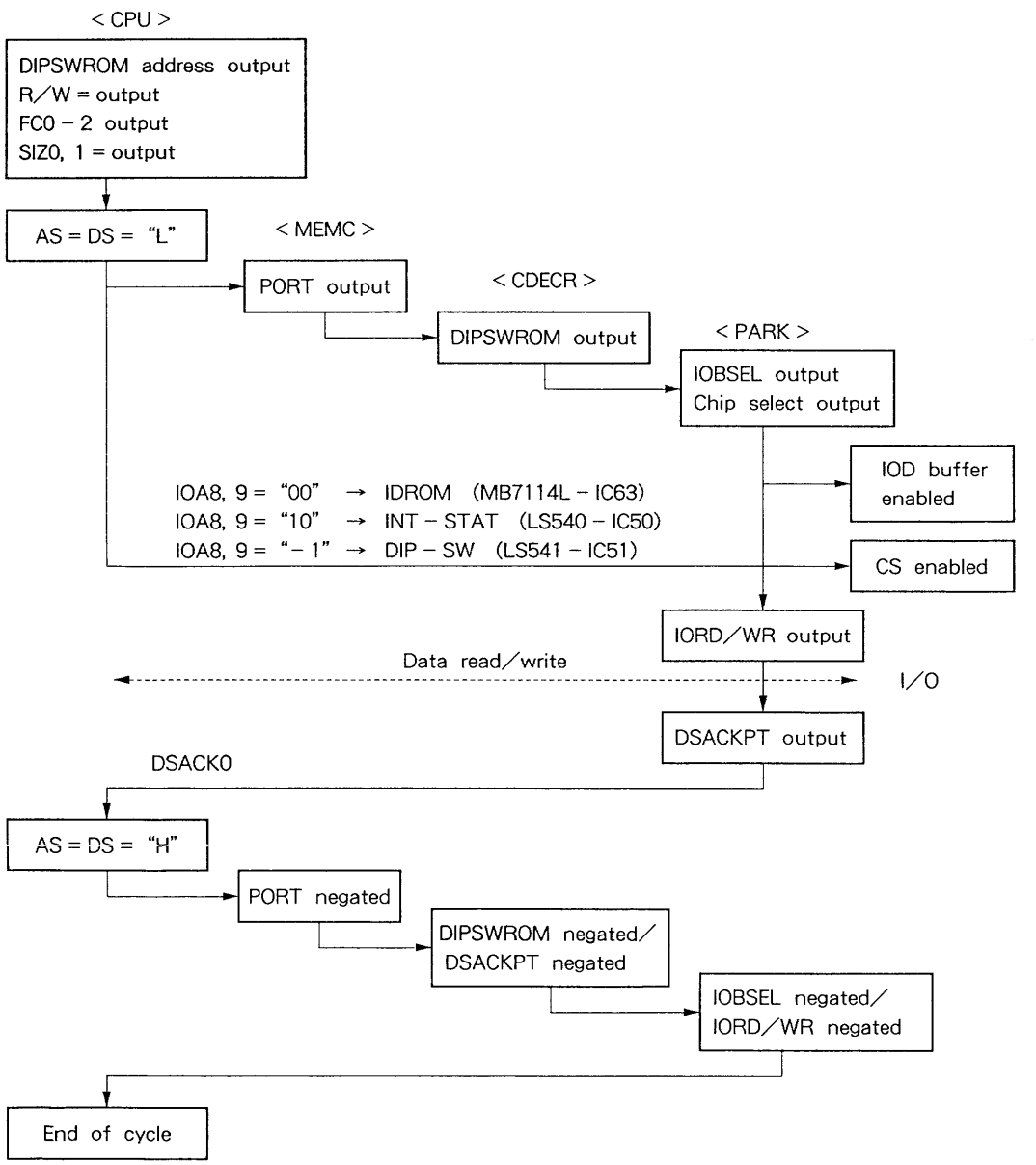
Device	IC	Chip select signal
Real Time Clock	MK48T02(B)	RTC
Serial Communication	LH8530A	SCC2
FloppyDisk Controller	uPD72067G	FDC



3-3-5. DIP Switch, ID-ROM and INT-STAT Access

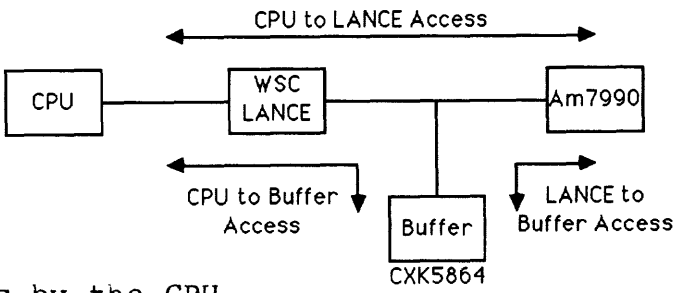
These devices are connected to the I/O bus (IOD7 - IOD10), but the chip select signal is output by WSC-CDECR. DSACK signals output to the CPU are also issued by CDECR. The chip select signal is DIPSWROM, but address bits 7 and 8 are re-decoded and allocated to the various ICs.

A flowchart of this process is given below.

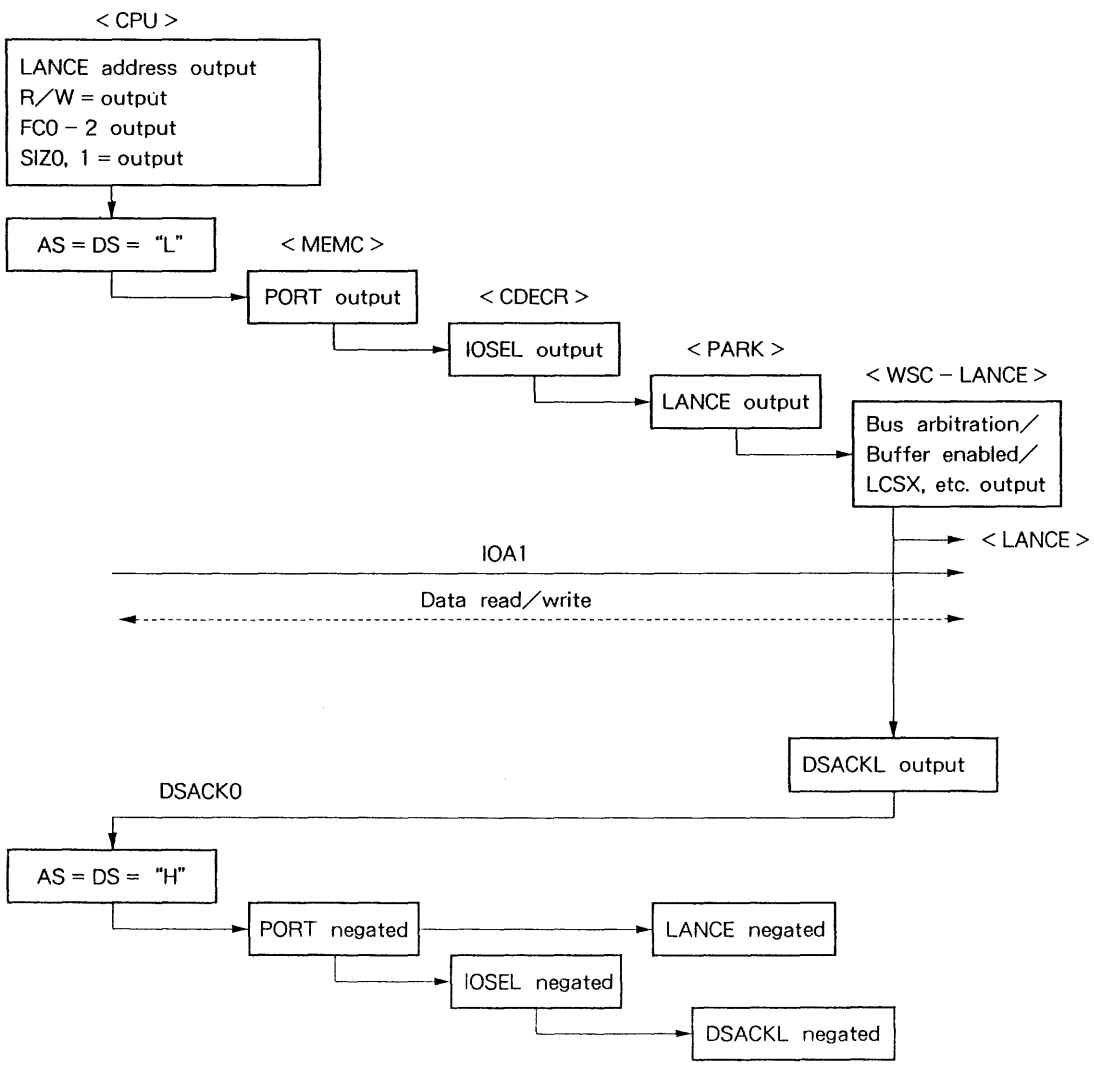


3-3-6. LANCE, LANCE-Buffer Access

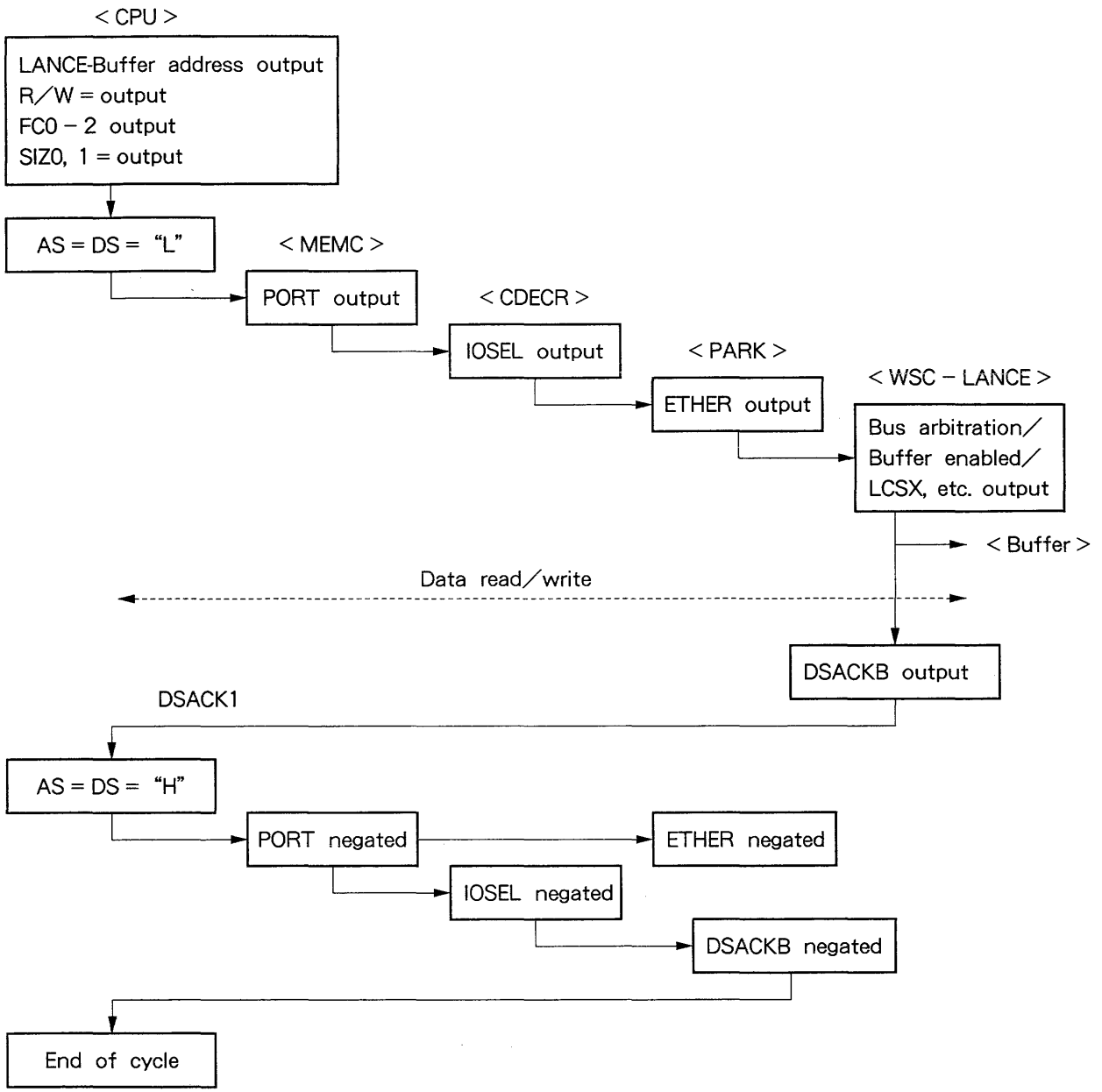
LANCE and the LANCE-buffer are accessed using a chip select signal output by PARK. DSACK, however, is output directly from a LANCE-use gate array (WSC-LANCE). WSC-LANCE controls the buffers by performing arbitration when the CPU and LANCE access buffers. It performs switching between when the CPU accesses LANCE and when it accesses a buffer.



a) LANCE access by the CPU

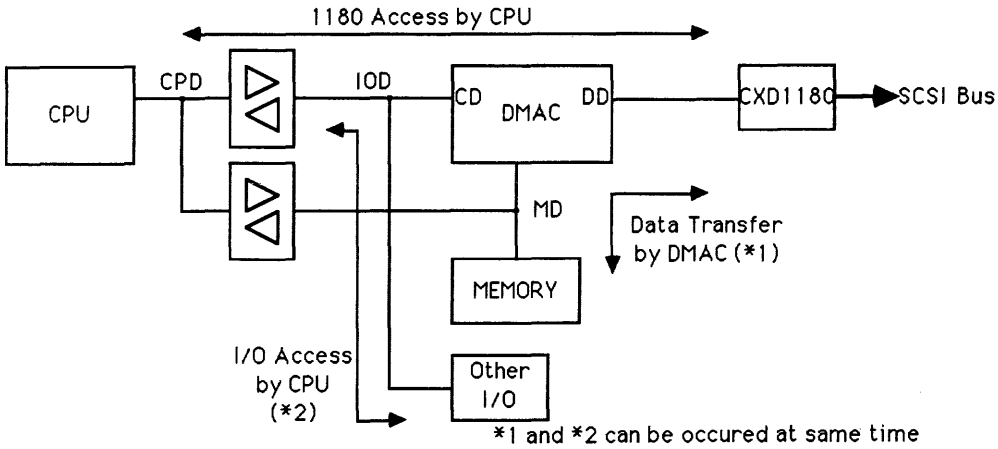


b) LANCE-Buffer access by the CPU

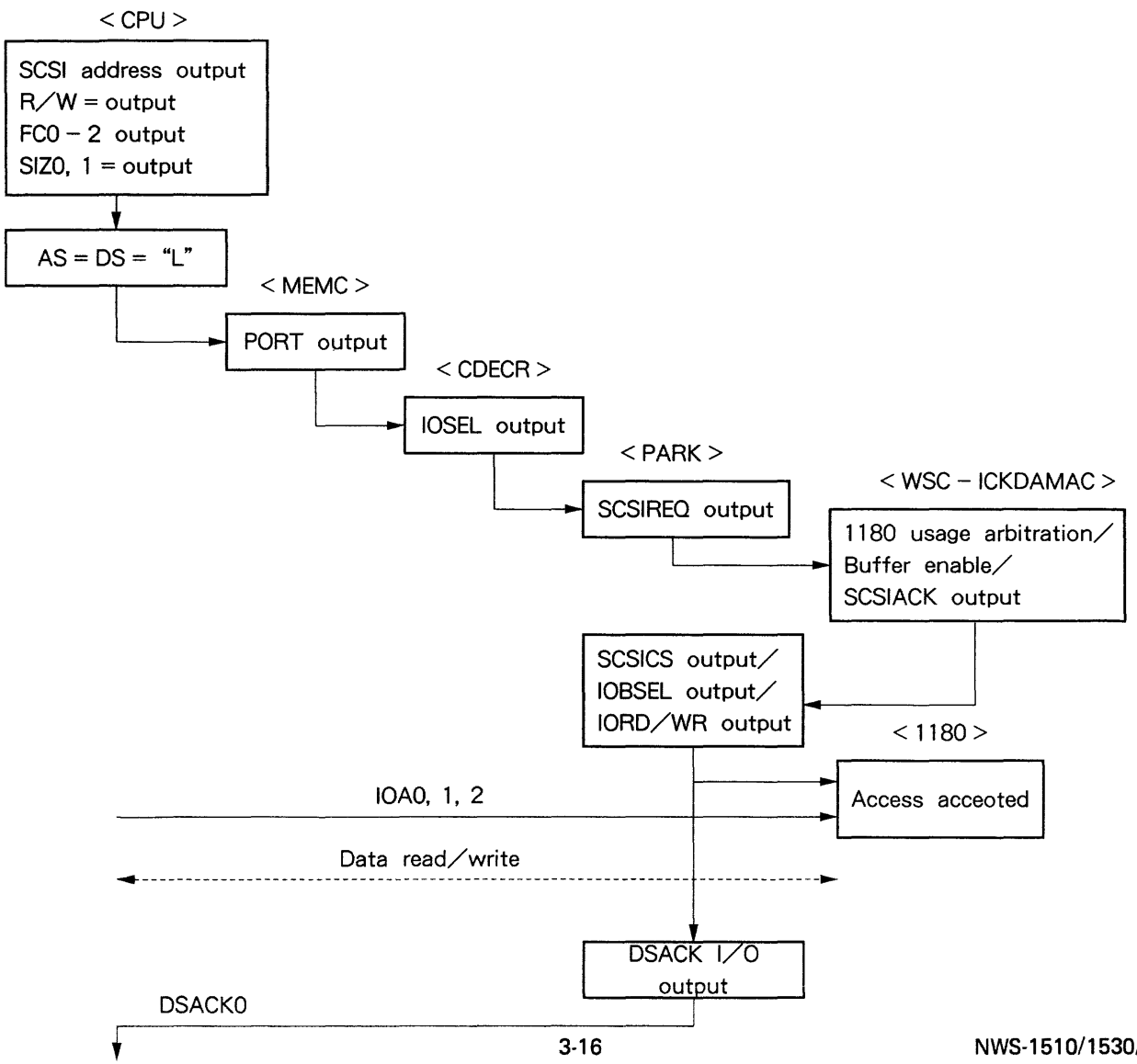


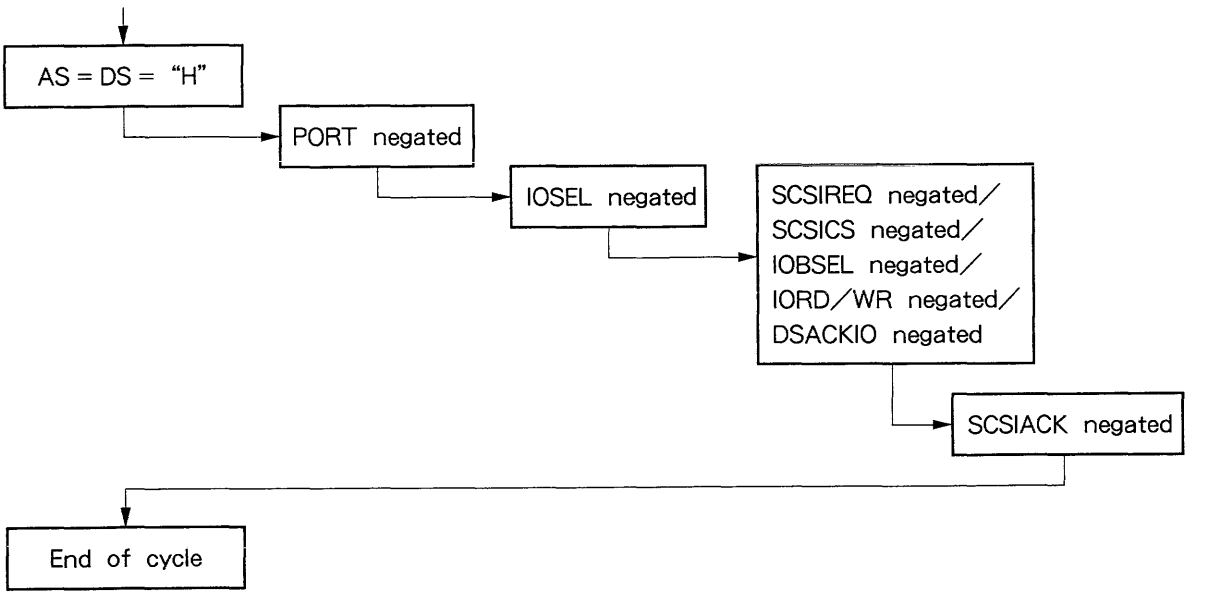
3-3-7. SCSI Access

It is possible for the CPU to access the SCSI controller chip (CXD1180) using the I/O bus while DMAC is executing data transfers between SCSI and memory as shown below.



Therefore, when the CPU needs to access CXD1180, usage arbitration circuit built into DMAC must give it authorization first. A flowchart of this process is given below.





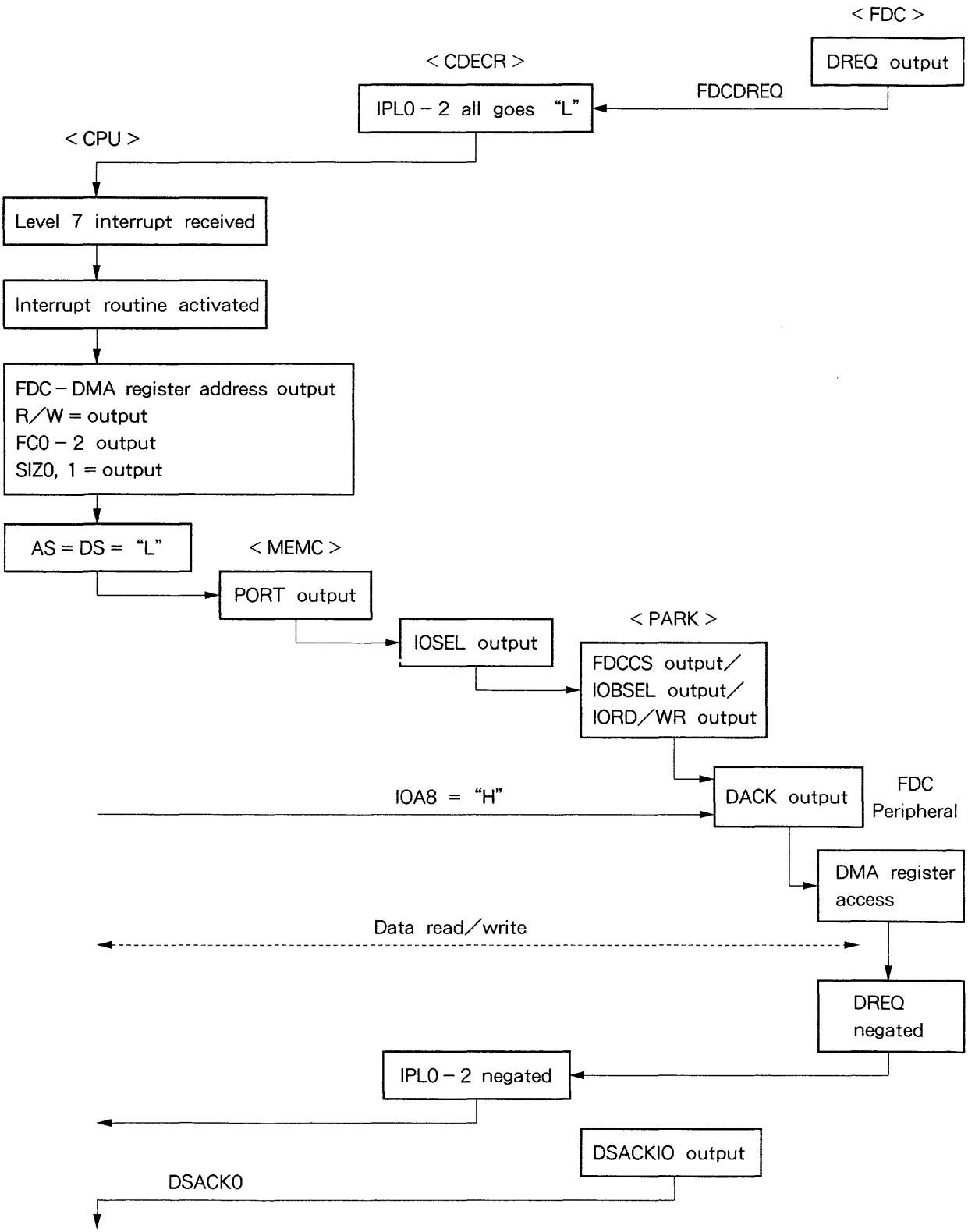
3-3-8. FDC Pseudo DMA Access

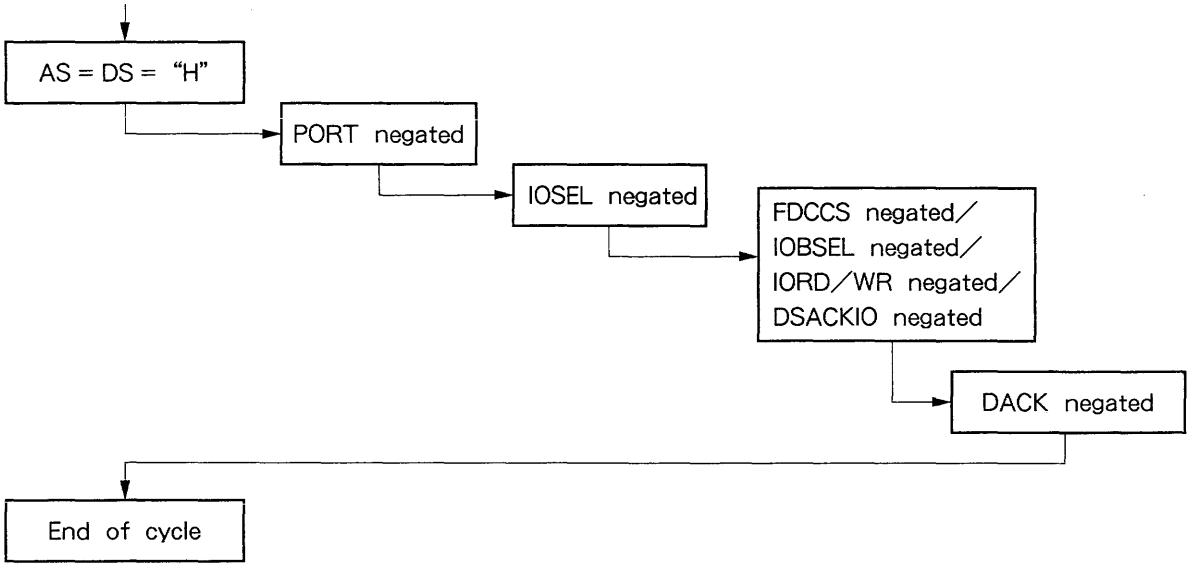
Accessing the FDC chip (uPD72067G) was covered in 3.4. Here we provide an description of assessing of the FDC DMA registers which takes place in the pseudo DMA mode.

Data transfer between FDD and FDC is accomplished using the FDC DMA transfer function. One byte of data is transferred in 16usec and, due to the processing required for software polling, the CPU is not free to do any other work during this period.

If the FDC must transfer data from (or to) the FDD, it outputs a DMA request: DREQ. This signal is connected to the CPU level 7 (top priority) interrupt. The CPU immediately reads data from (or writes to) the FDC. To do so, the CPU must access the FDC DMA registers (A8 is "H" during access to FDC). Then, external circuit converts FDCCS to DACK and access to the FDC DMA registers is accomplished. When the CPU succeeds in accessing the DMSA registers, DREQ is automatically negated, canceling the interrupt request.

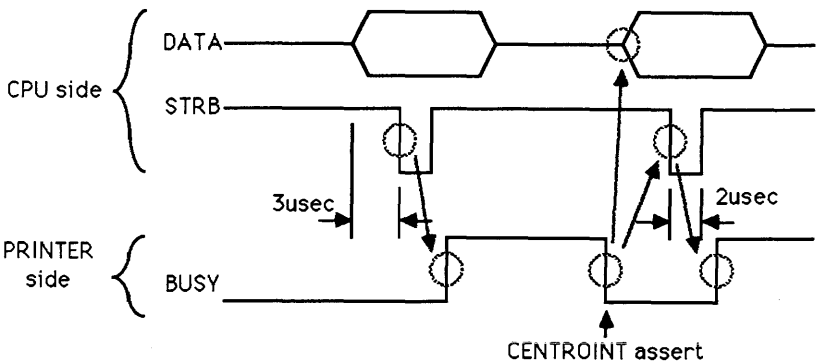
A flowcnart of this process is given below.


< FDC >
DREQ output
< CDECR >
FDCDREQ
IPL0 – 2 all goes "L"
< CPU >
Level 7 interrupt received
Interrupt routine activated
FDC – DMA register address output
R/W = output
FC0 – 2 output
SIZ0, 1 = output
AS = DS = "L"
< MEMC >
PORT output
IOSEL output
< PARK >
FDCCS output/
IOBSEL output/
IORD/WR output
IOA8 = "H"
DACK output
FDC
Peripheral
DMA register
access
Data read/write
DREQ
negated
IPL0 – 2 negated
DSACKIO output
DSACK0

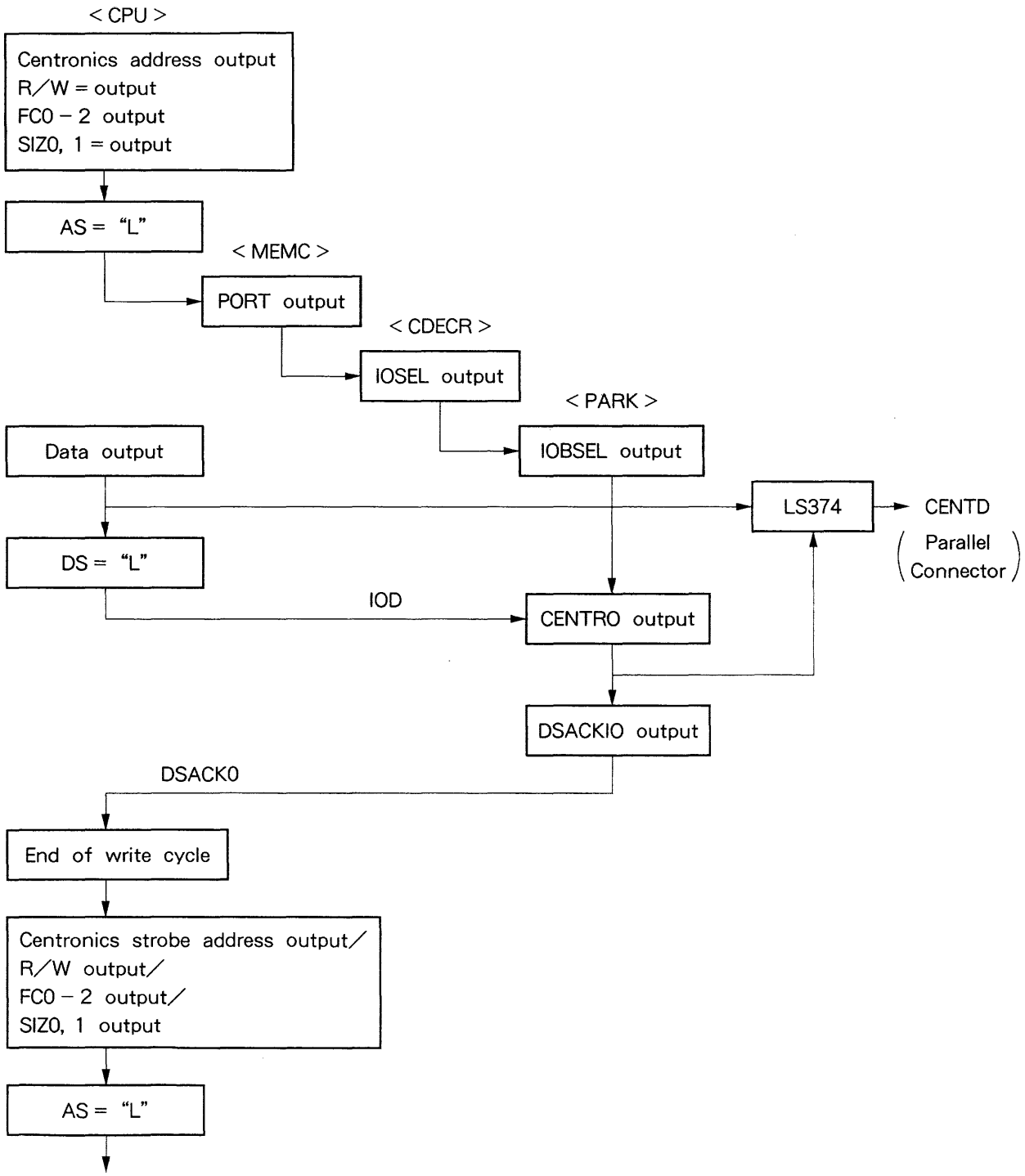


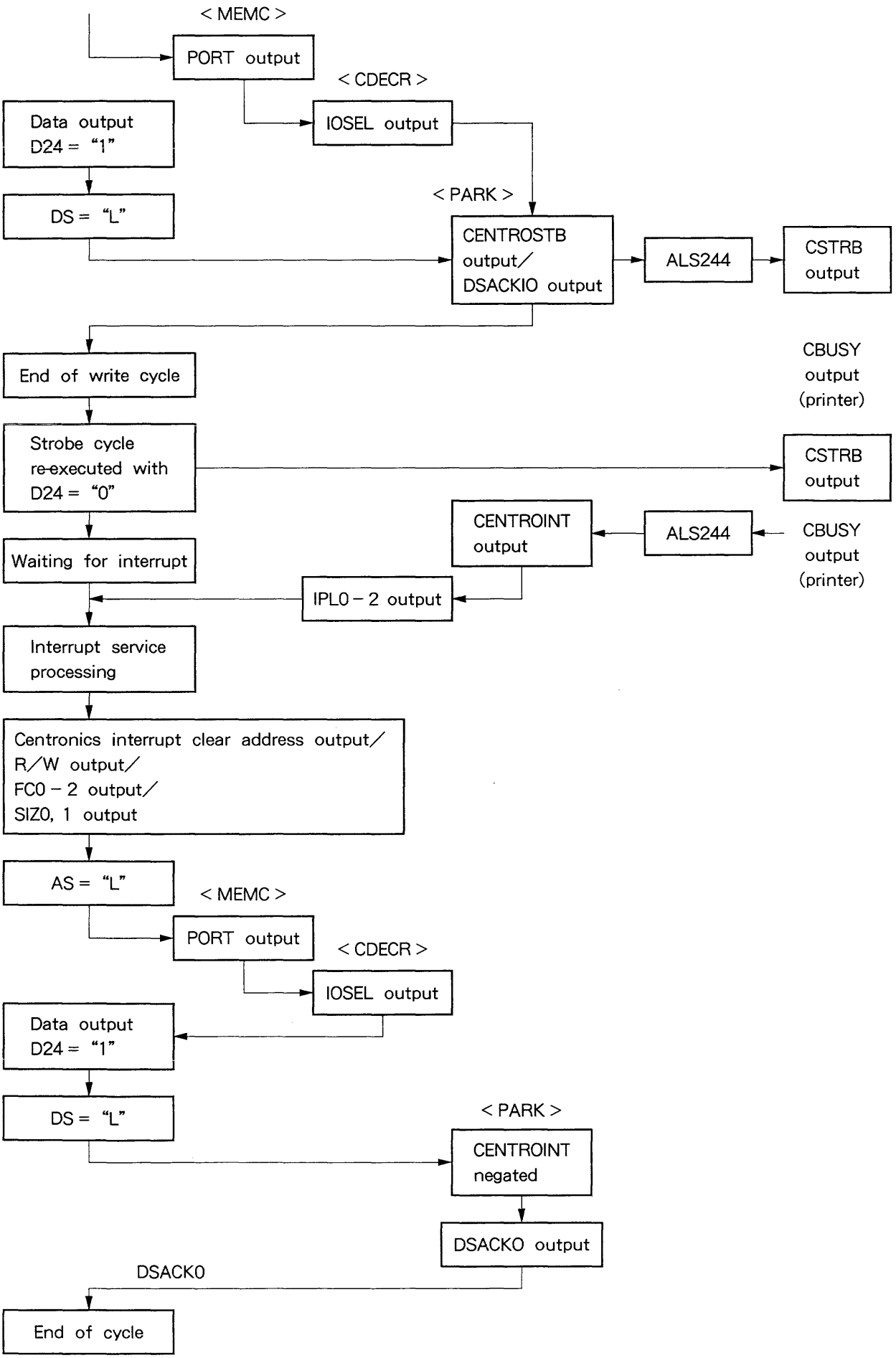
3-3-9. Centronics (Parallel Port) Access

The parallel (Centronics) port is an output-only 8-bit parallel interface. It is principally used to connect a printer and conforms to the specification developed by the Centronics company. The signal transition is shown below. Timing is fixed by **NWS-1500.**



A flowchart showing the output of 1 byte from the parallel port is given below.




< MEMC >
PORT output
< CDECR >
IOSEL output
Data output
D24 = "1"
DS = "L"
< PARK >
CENTROSTB
output/
DSACKIO output
ALS244
CSTRB
output
End of write cycle
CBUSY
output
(printer)
Strobe cycle
re-executed with
D24 = "0"
CSTRB
output
CENTROINT
output
ALS244
CBUSY
output
(printer)
Waiting for interrupt
IPL0 – 2 output
Interrupt service
processing
Centronics interrupt clear address output/
R/W output/
FC0 – 2 output/
SIZ0, 1 output
AS = "L"
< MEMC >
PORT output
< CDECR >
IOSEL output
Data output
D24 = "1"
DS = "L"
< PARK >
CENTROINT
negated
DSACK0 output
DSACK0
End of cycle

3-3-10. External Slot Access

The CPU accesses devices external to the MPU-7 board in the following four cases:

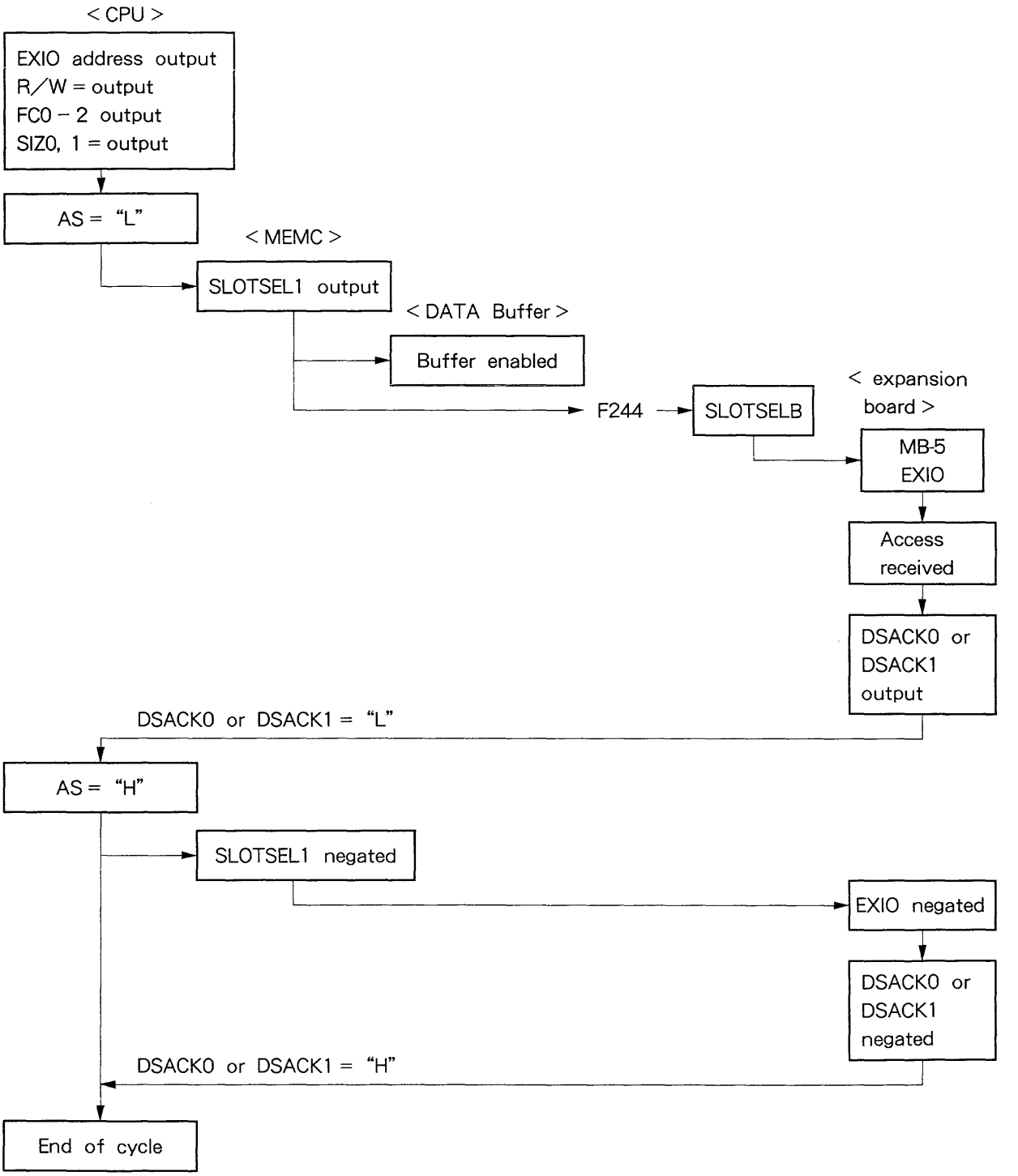
1) When it accesses boards installed in the expansion I/O slots
2) When it accesses the display controller circuit board (DSC-008) -> EXIO access
3) When it accesses an optional sound board
   -> special access
4) When it fetches an interrupt vector in response to a request issued by LH8530A on the NWB-231A board installed in an expansion I/O slot
   -> VECT access.

The above can be classified into three type sequences, 1 and 2 being basically identical.

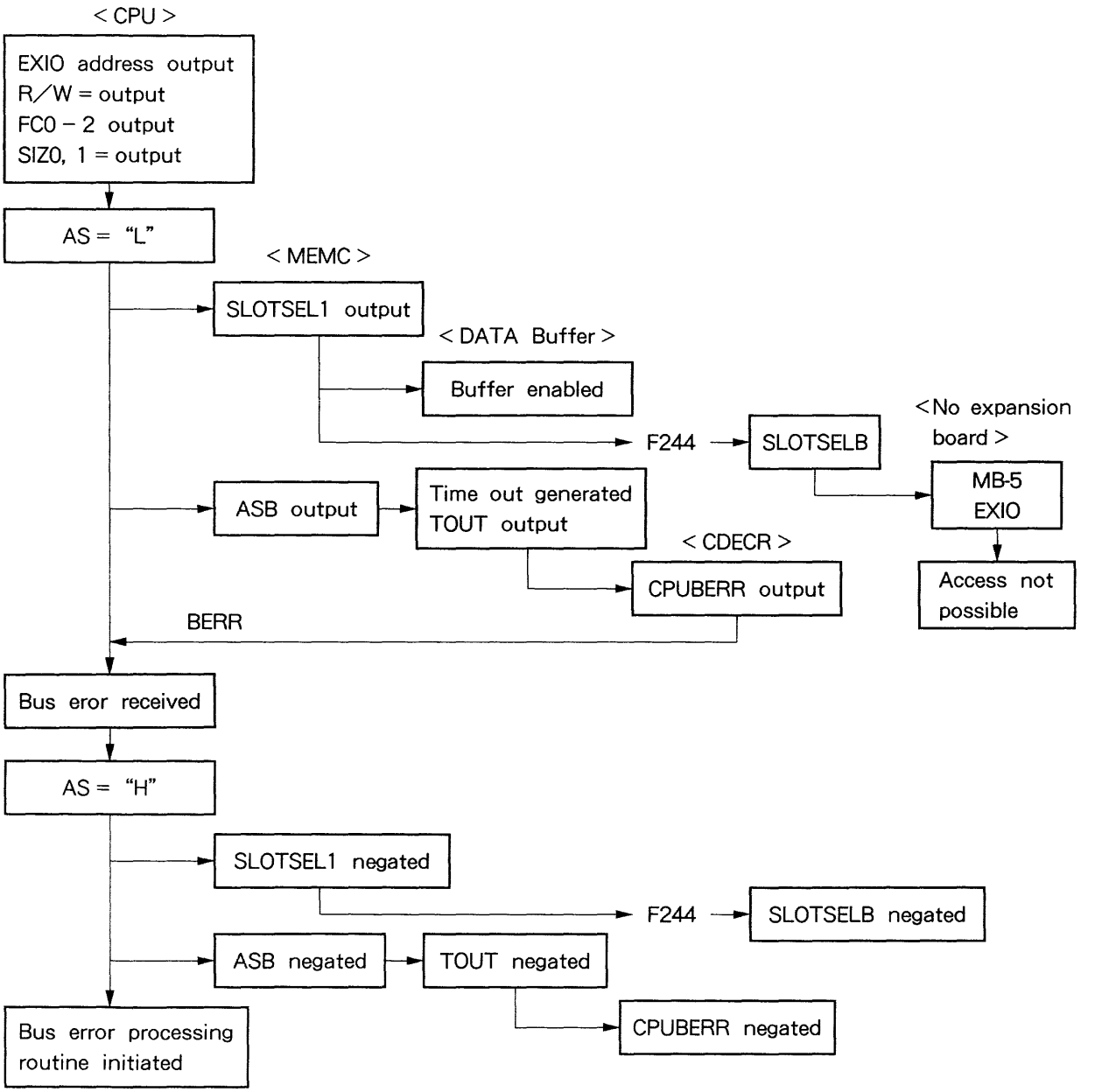
3-3-10-1. EXIO access

EXIO access is used by the CPU to access a board installed in one of the expansion I/O slots or the DSC-007 dedicated black-and-white display controller. The DSACK signal cannot be generated automatically by MPU-7 internally. It is input via an external connector. A bus error is generated if an attempt is made to access a non-existent address. A flowchart of this process is given below.

a) Normal operation

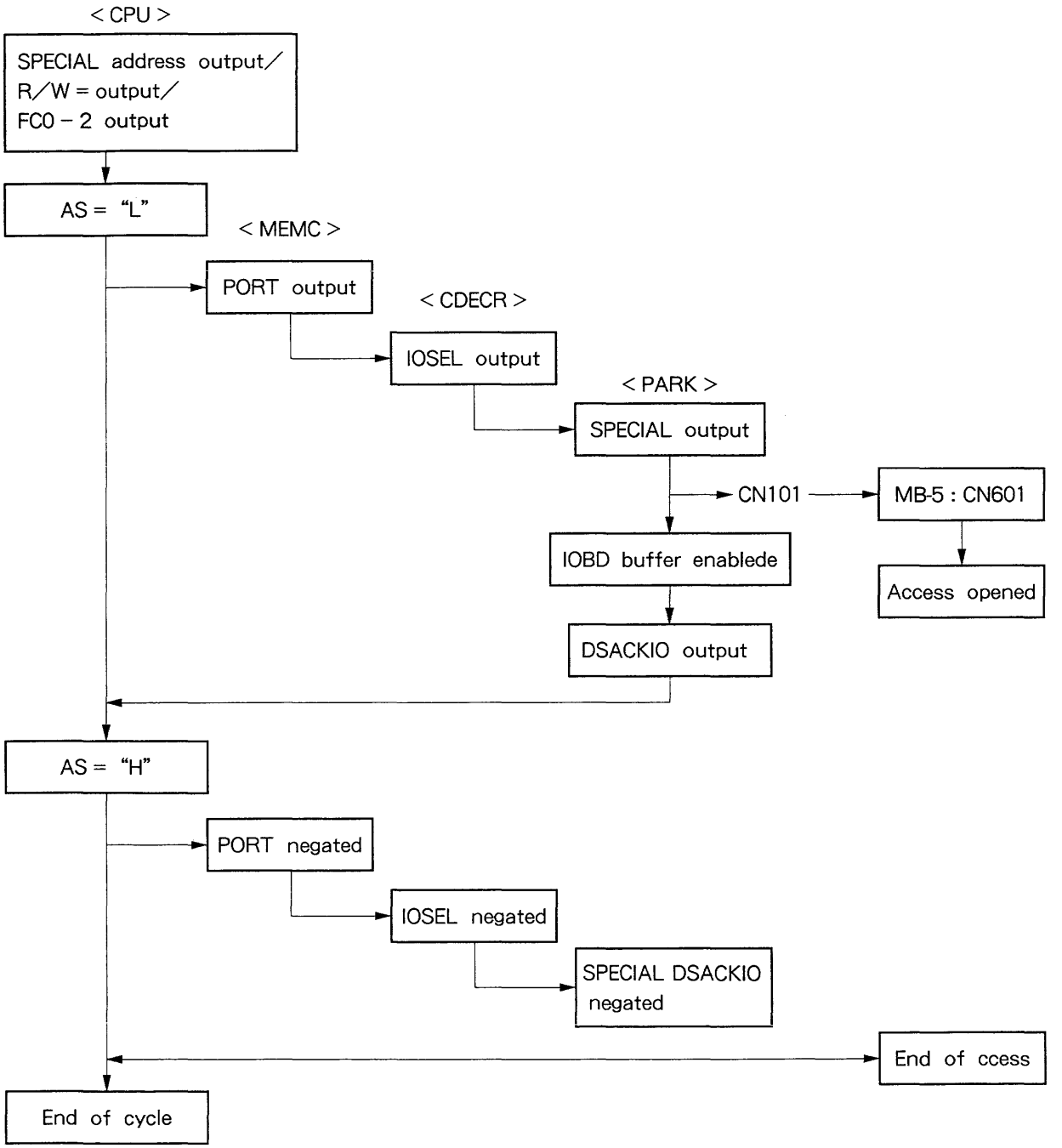

< CPU >
EXIO address output
R/W = output
FC0 – 2 output
SIZ0, 1 = output
AS = "L"
< MEMC >
SLOTSEL1 output
< DATA Buffer >
Buffer enabled
F244
SLOTSELB
< expansion board >
MB-5 EXIO
Access received
DSACK0 or DSACK1 output
DSACK0 or DSACK1 = "L"
AS = "H"
SLOTSEL1 negated
EXIO negated
DSACK0 or DSACK1 negated
DSACK0 or DSACK1 = "H"
End of cycle

b) Bus error generated



3-3-10-2. SPECIAL access

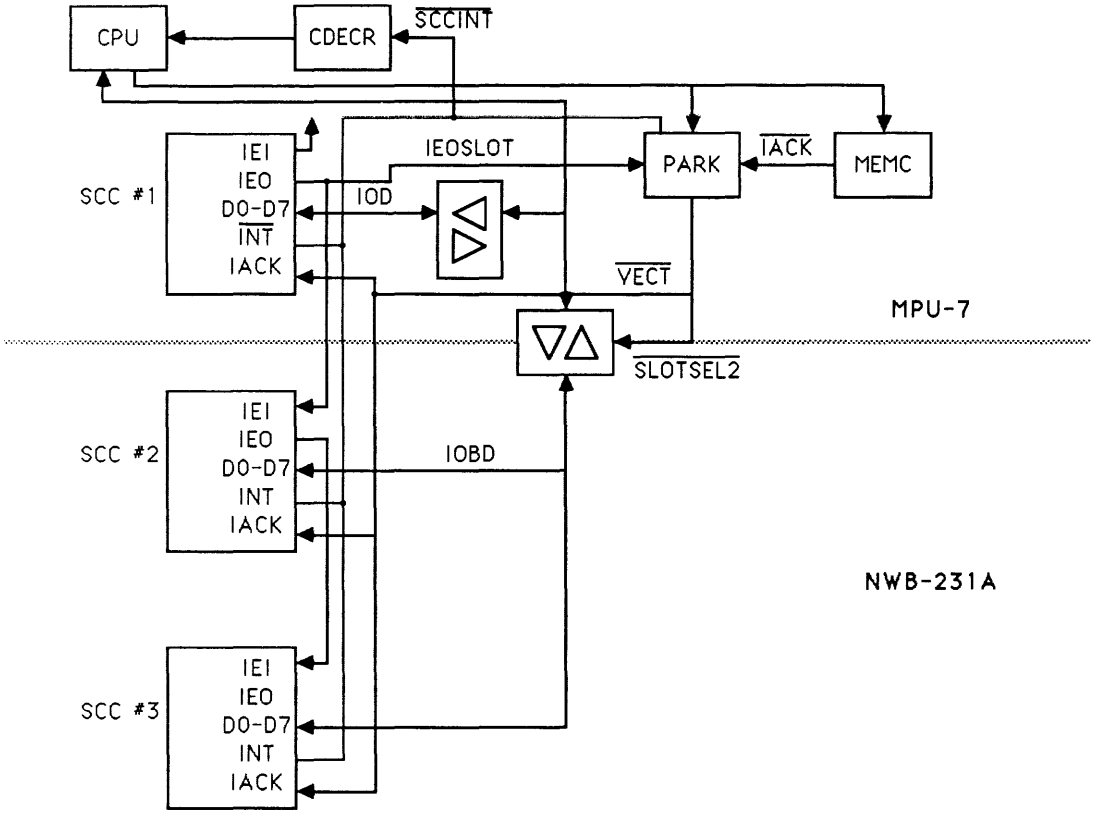
SPECIAL access is used by the CPU to access an optional sound board installed in CN601 on the MB-5 board. The DSACK signal is generated automatically by WSC-PARK.



3-3-10-3. VECT access

VECT access is used by the CPU fetch an interrupt vector in response to an interrupt issued by SCC (LH8530A) on the NWB-231A board installed in an expansion I/O slot. The

internal SCC and expansion SCC interrupt systems are shown below.

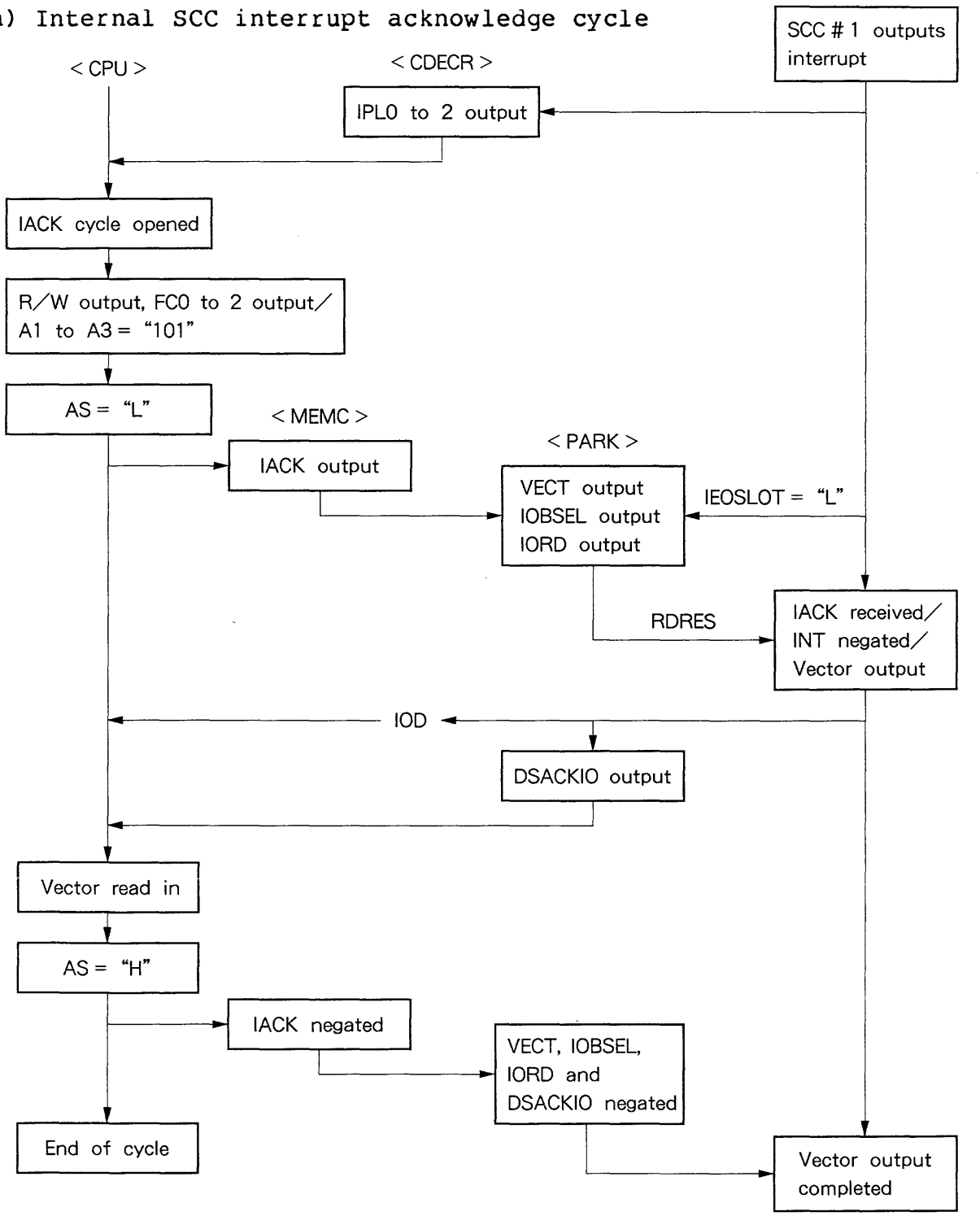


If an internal or external SCC generates a signal send/receive interrupt, CDECR is input to the priority encoder, creating IPL0 - 2 which are input to the CPU. The CPU enters an interrupt acknowledge cycle and AS is output with FD* all "H" and addresses 16 - 19 all "H." Under these conditions, MEMC outputs IACK. PARK is output when addresses 1 - 3 are "101" VECT is output if IACK = "L" and SCCINT = "L" SCC #1 - #3 are in the process generating interrupts themselves, so they respond to VECT only when IEI = "H" by outputting the interrupt vector. For #1, if an INT is output, its outputting IEO (IEI of #2) goes "L" and the vector is output. At this point, IEOSLOT = "L" so IOBD is in buffer disabled status (PARK function). For #2, if an INT is output, IEO = "H" while the #1 VECT = "L" Therefore, IEOSLOT = "H" and PARK outputs SLOTSEL2, enabling the IOBD buffer. The #2

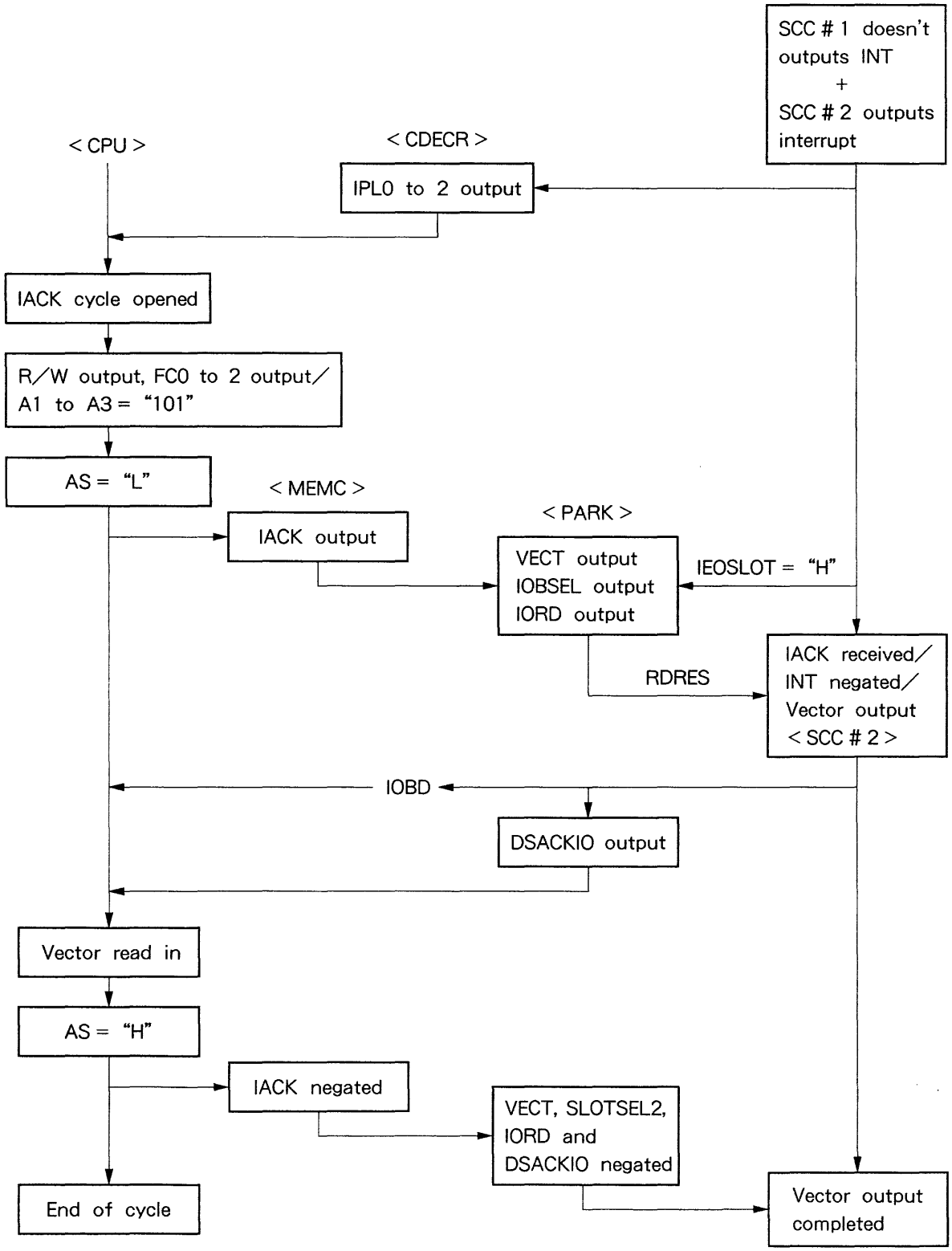
SCC IEI = "H" and VECT (IACK) = "L" so the vector is output.
At t his point the #2 IEO is "L"

Flowcharts showing the process when INT is output by #1-SCC and when it is output by #2-SCC are given below.

a) Internal SCC interrupt acknowledge cycle



b) External SCC interrupt acknowledge cycle



3-4. INTERRUPTS

MPU-7 interrupts use levels 1 to 7. The correspondence between devices and interrupt levels is given below.

Level 7 FDC (DREQ in DMA mode)

Level 6 Timer interrupt (100Hz interrupt)

Level 5 SCC (internal and external) *
Keyboard/mouse data receive interrupts

Level 4 LANCE (Am7990 INT)
SCSI (CXD1180 IRQ)
SLOTINT3 (expansion slot IPIRQ3)

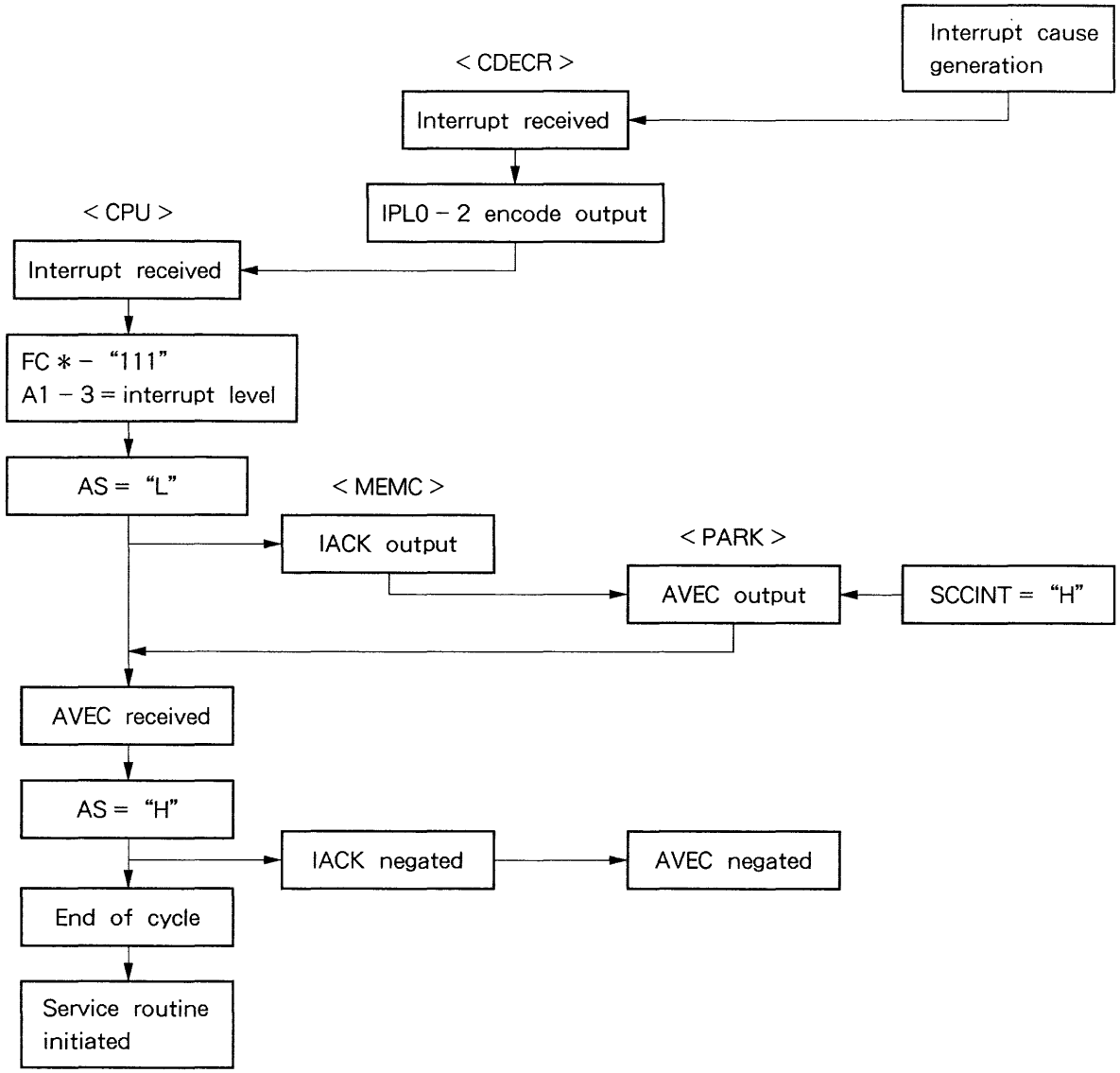
Level 3 FDC (uPD72067G INT)
SLOTINT1 (expansion slot IPIRQ1)

Level 2 INTH (based on CDECR internal control register)

Level 1 Async trap (based on CDECR external control register)

* The external SCSI interrupt is connected to IPIRQ5 on the MB-5 board.

Only interrupts from external and internal SCC are vector interrupts (VECT is output). All the others are auto vector interrupts (AVEC is output). If two interrupts at the same level are received simultaneously, the causes of the interrupts are determined using an INT0STAT register readout and the appropriate service routines are called.
A flowchart for auto vector interrupts is given below.



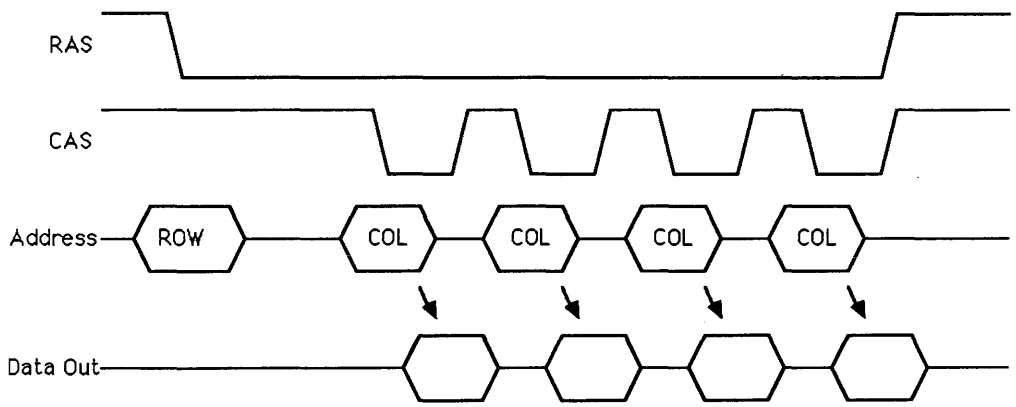
3-5. CACHE BURST TRANSFER FUNCTION

The a command/data cache is built into the MC68030, the CPU used by the PWS-1500 Series. Its performance level is high, but in order to speed up operation further using the cache, a burst transfer function is provided for loading commands and data. Details are provided in the "MC68030 User's Manual" provided by Motorola. Here we provide only a brief description of the operation of the hardware used for implementing this function.

When the CPU is operating with the cache and it determines that the commands or data to be executed next is not present in the cache, it loads the necessary commands or data into the cache from external memory. The special type of cycle

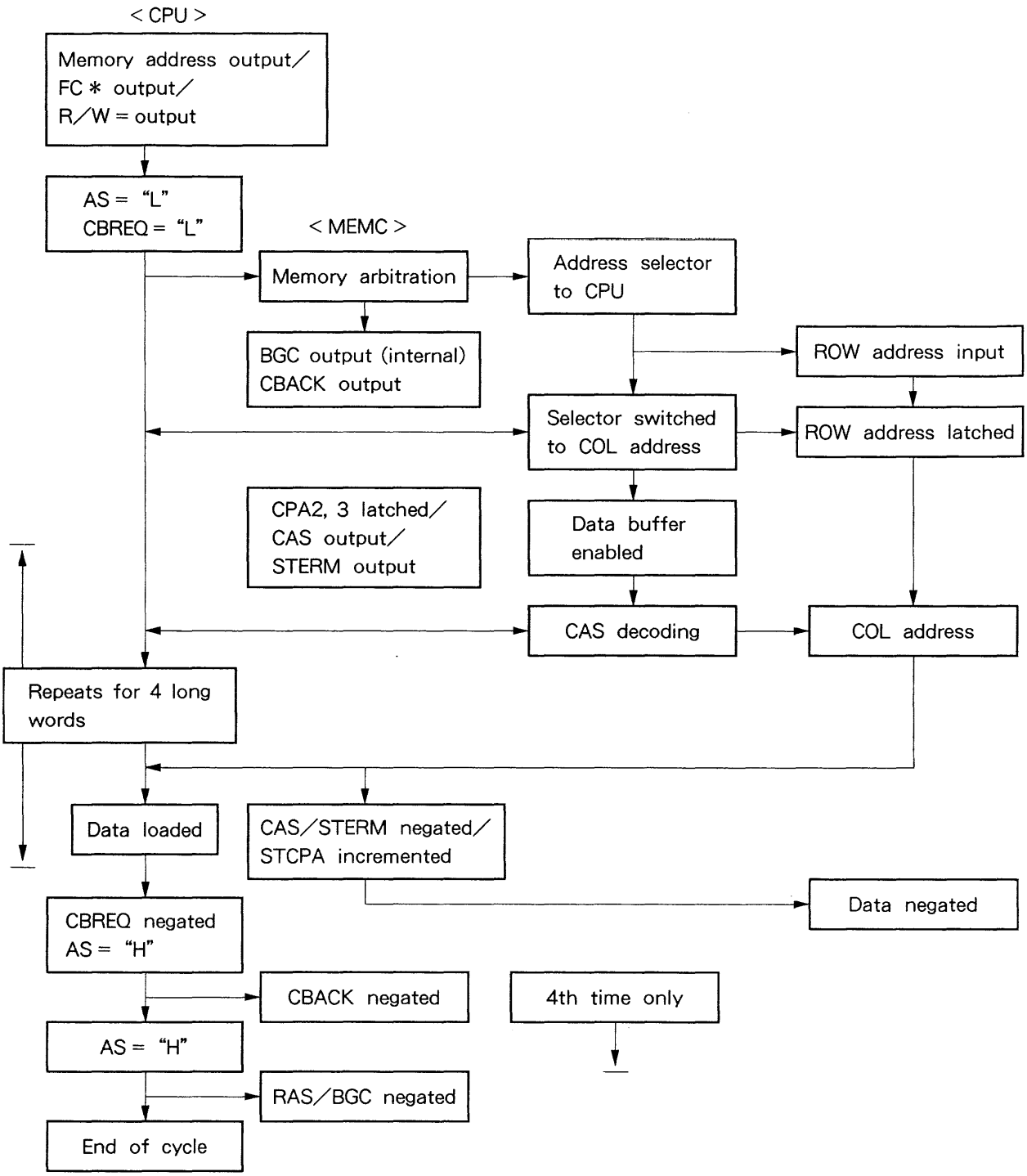
used for this operation is called burst transfer. A normal memory access requires a minimum of 3 clocks (5 in the case of the 1500 because it operates with two wait states). A burst transfer to the cache, however, operates as follows. If no wait state intervenes, four long words can be accessed within 5 clocks. In the case of the 1500, the first long word needs two wait states and the subsequent three words one each for a total of 10 clocks.

In the PWS-1500, this function is implemented using circuit built into WSC-MEMC on the MPU-7 board and the main memory's high-speed page mode read cycle. The high-speed page mode read cycle is a DRAM special function as shown below.



In other words, RAS is maintained "L" in the same lower address, and each time the column address is switched CAS is input, causing data from continuous addresses to be read.

A flowchart of the process when the CPU issues a burst transfer request (CBREQ) is given below.



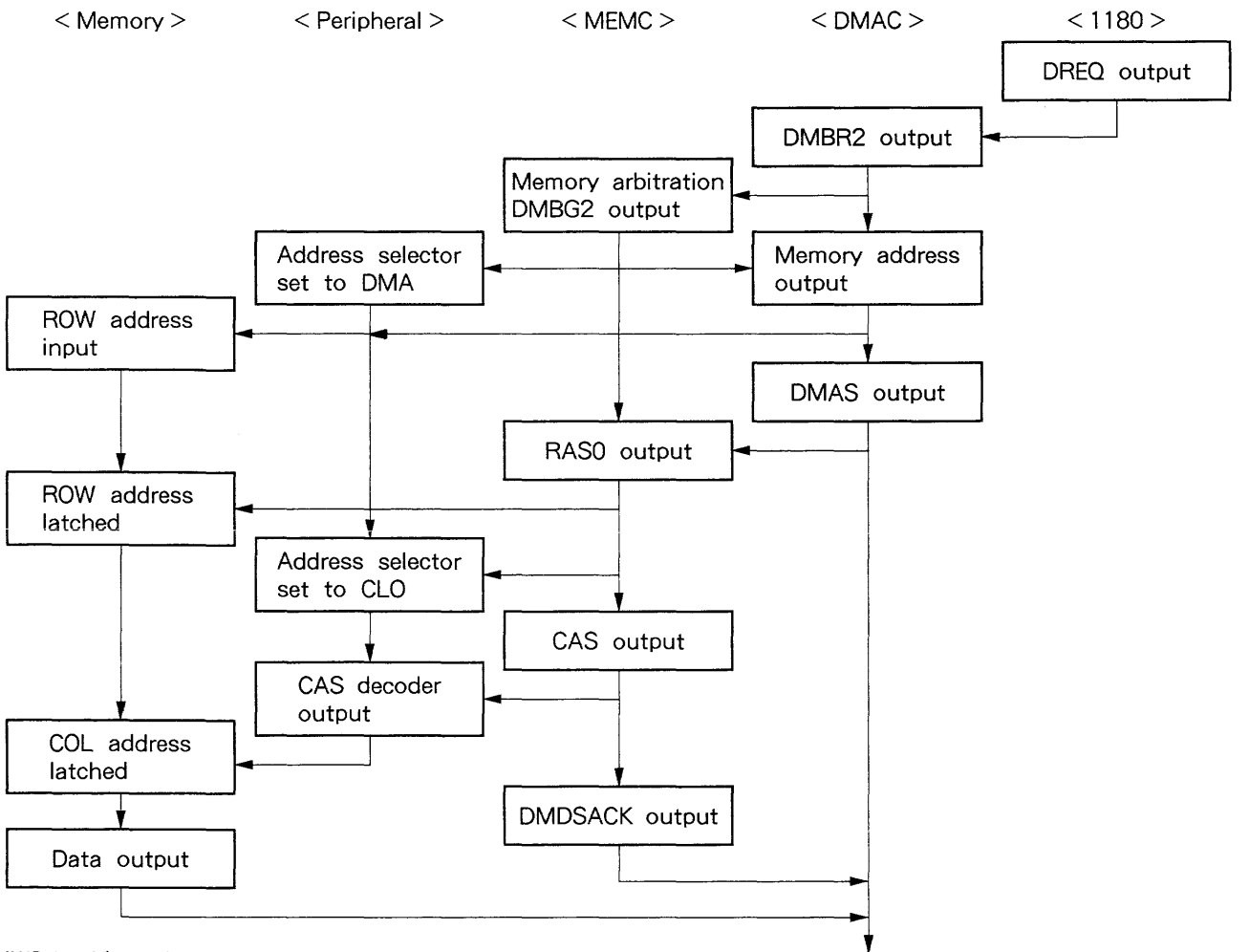
3-6. DMAC OPERATION

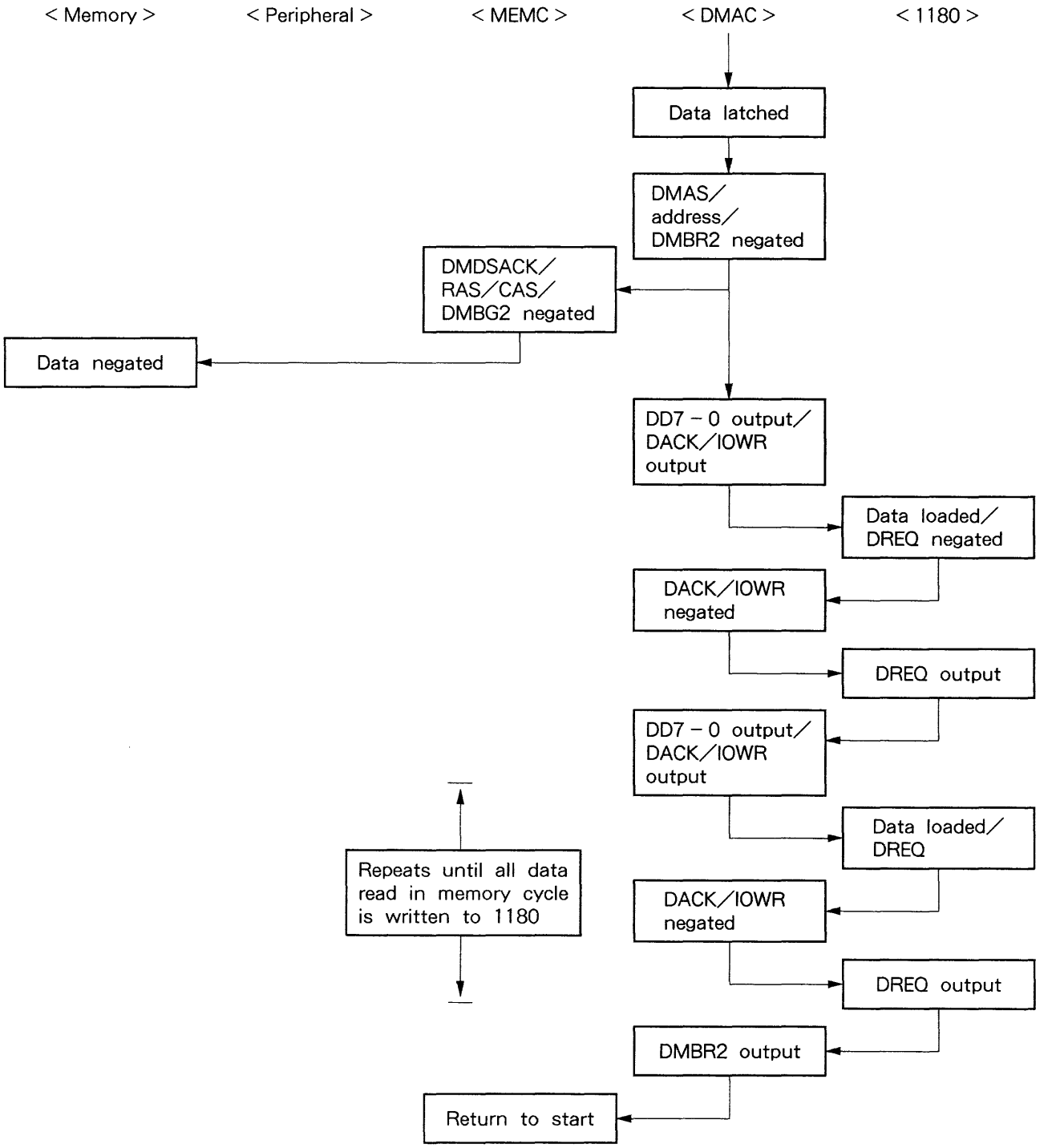
The relationship between the DMAC, CPU and SCSI controller (CXD1180) was described in section 3-7. Here we present an overview of DMAC and a description of data transfer between SCSI and memory carried out using DMAC. WSC-ICKDMAC is a 32-bit DMAC developed specifically for data transfer between the CXD1180 and memory. When data is transferred from memory

to SCSI, 4 bytes (on long word) of data is loaded from memory at a time. It is then divided up byte by byte and written to CXD1180. When data is transferred from SCSI to memory, the data read from the 1180 is packed into one long word and written to memory. A built-in address conversion table is used when memory is accessed. This allows even data scattered at nonconsecutive memory areas to be accessed as if it were all in one contiguous area. Using the table, it is possible to transfer a maximum of 516K bytes of data at one time. MEMC performs memory usage arbitration.

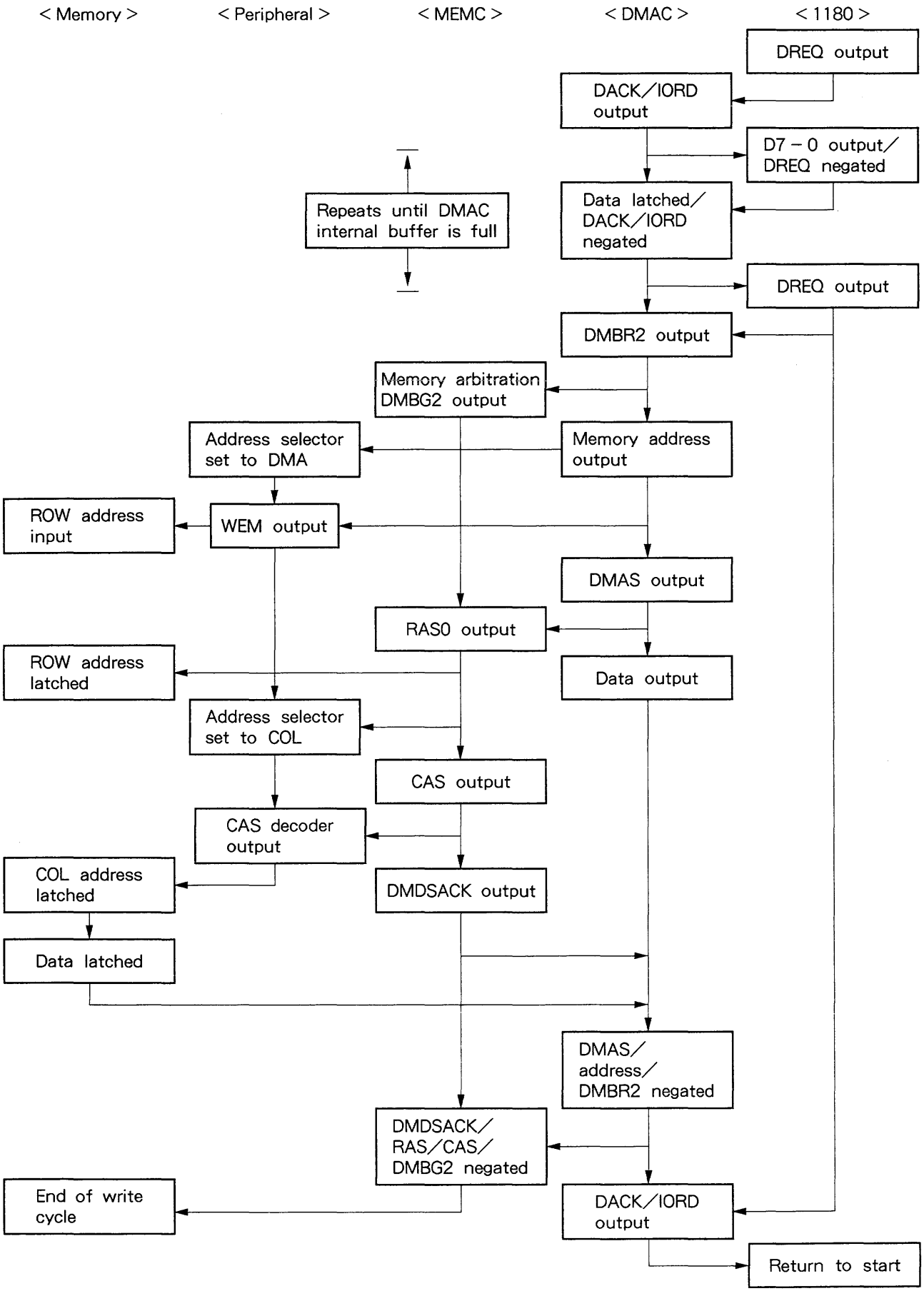
Flowcharts for data transfers from memory to SCSI and from SCSI to memory are given below.

a) Memory to SCSI transfer




< Memory >
< Peripheral >
< MEMC >
< DMAC >
< 1180 >
Data latched
DMAS/
address/
DMBR2 negated
DMDSACK/
RAS/CAS/
DMBG2 negated
Data negated
DD7 – 0 output/
DACK/IOWR
output
Data loaded/
DREQ negated
DACK/IOWR
negated
DREQ output
DD7 – 0 output/
DACK/IOWR
output
Data loaded/
DREQ
DACK/IOWR
negated
DREQ output
Repeats until all data
read in memory cycle
is written to 1180
DMBR2 output
Return to start

b) SCSI to memory transfer

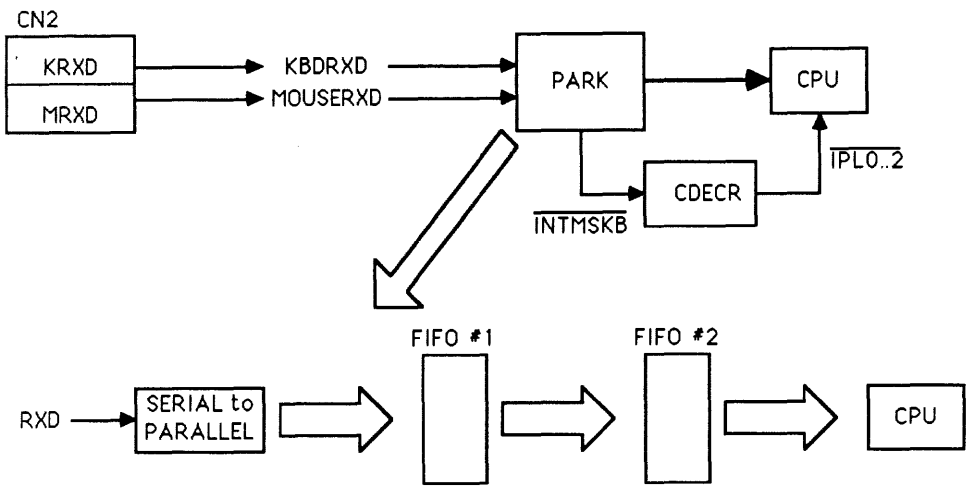


3-7. KEYBOARD/MOUSE

3-7-1. Data Reception

The keyboard/mouse data receiving port is implemented using circuit built into WSC-PARK. Data is received as serial input at 9600 bps from the keyboard and 1200 bps from the mouse. It is then converted into parallel form and interrupts are issued to the CPU to indicate that data has been received. A 2-byte FIFO is built into PARK allowing 2 bytes of data to be stored.

An interrupt is generated when one byte has been received. The interrupt is normally cleared after the CPU reads the data, but if the second data byte has already been received, the interrupt is not cleared. The system is illustrated below.

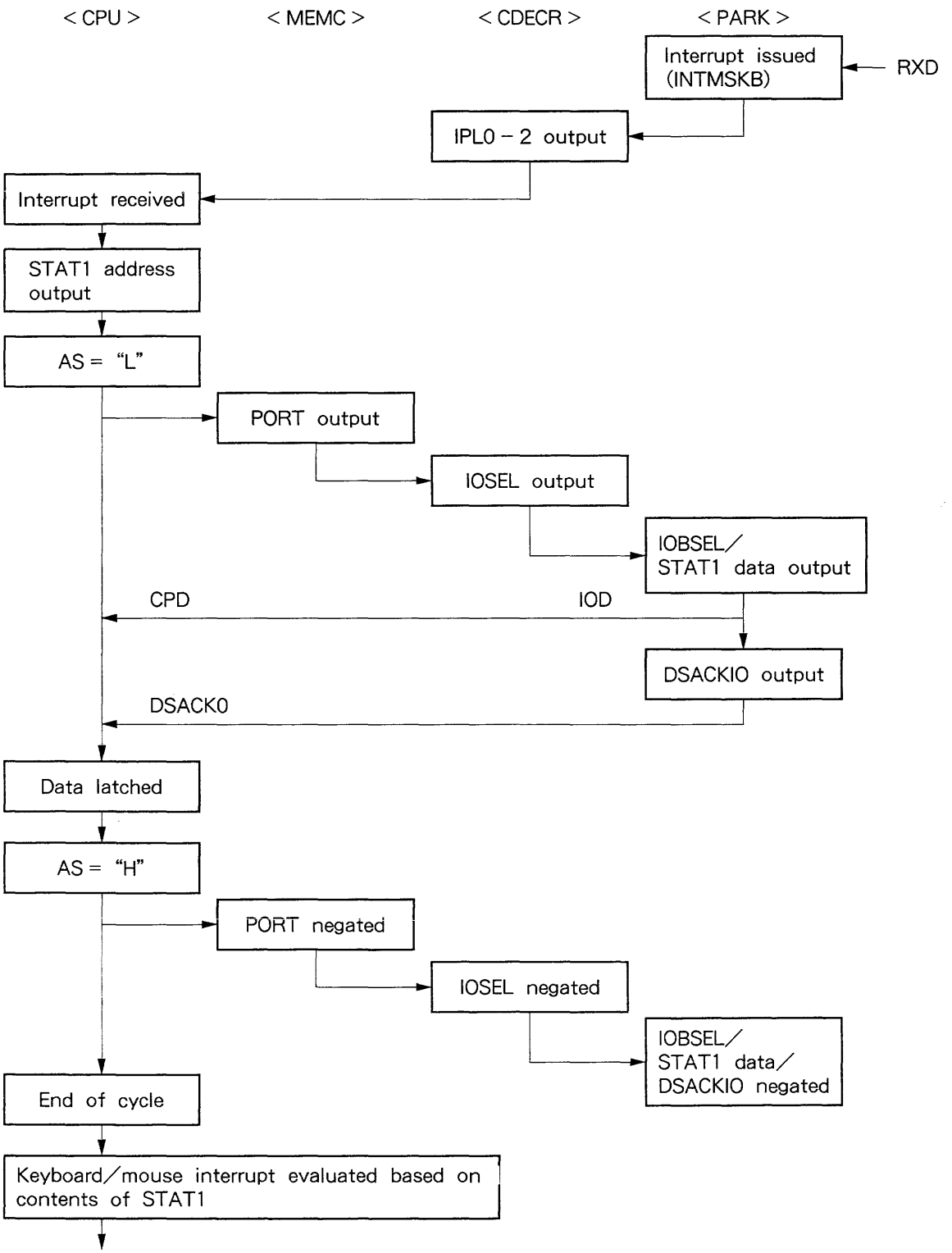


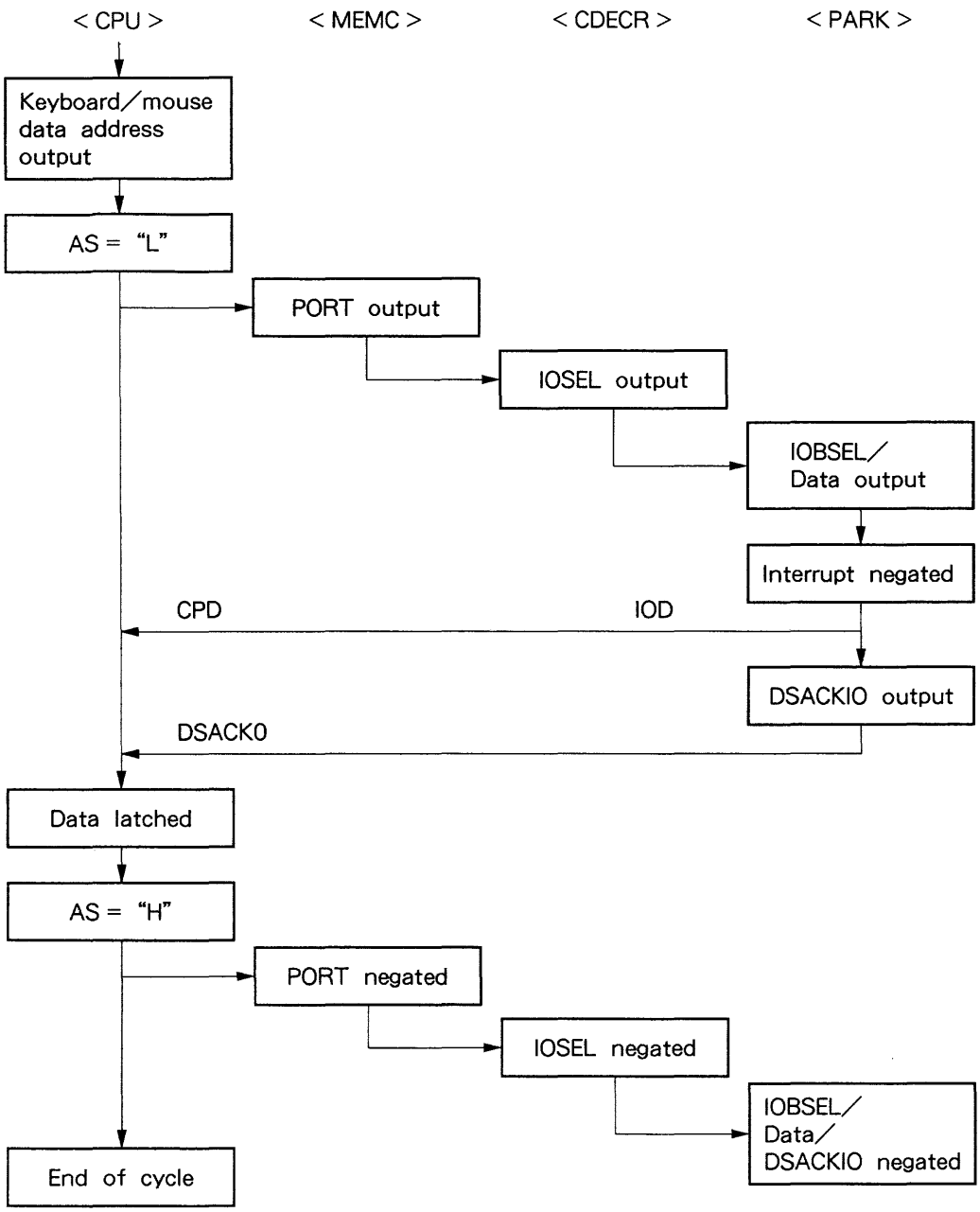
The first byte of data immediately passes FIFO#1 and is latched to FIFO#2. At this point an interrupt is generated. The interrupt is cleared if the CPU immediately reads the contents of FIFO#2.

If, before the CPU reads FIFO#2, the next data byte has entered FIFO#1, the interrupt is not cleared even when the CPU reads FIFO#2. It is cleared only after the CPU reads the

data moved from FIFO#1 to FIFO#2 (the second byte). Any additional data received when FIFO#1 and FIFO#2 already both have data is lost.

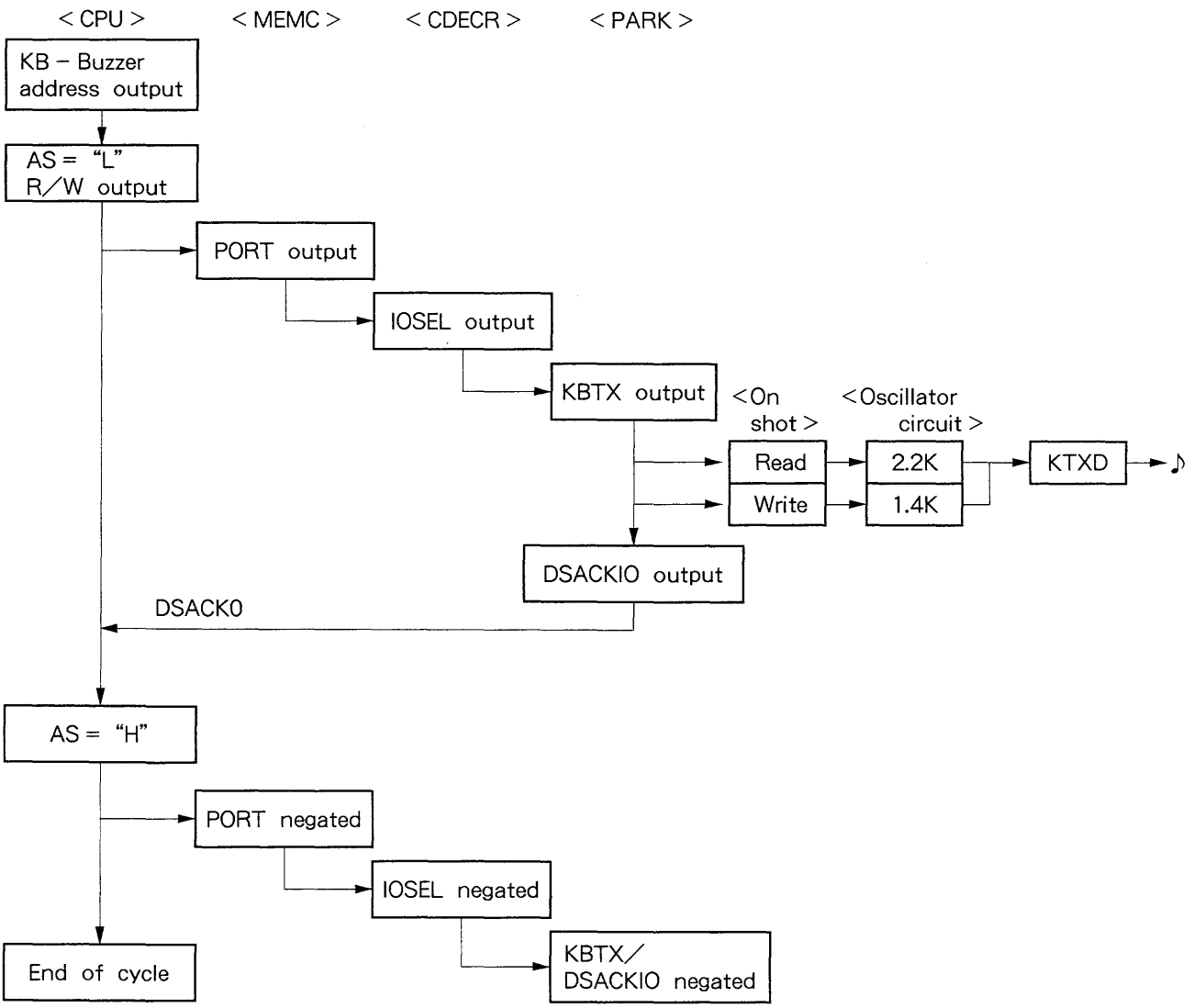
The following flowchart shows the process with which the CPU reads keyboard/mouse data after the interrupt from PARK is received.




< CPU >
< MEMC >
< CDECR >
< PARK >
Keyboard/mouse data address output
AS = "L"
PORT output
IOSEL output
IOBSEL/ Data output
Interrupt negated
CPD
IOD
DSACKIO output
DSACK0
Data latched
AS = "H"
PORT negated
IOSEL negated
IOBSEL/ Data/ DSACKIO negated
End of cycle

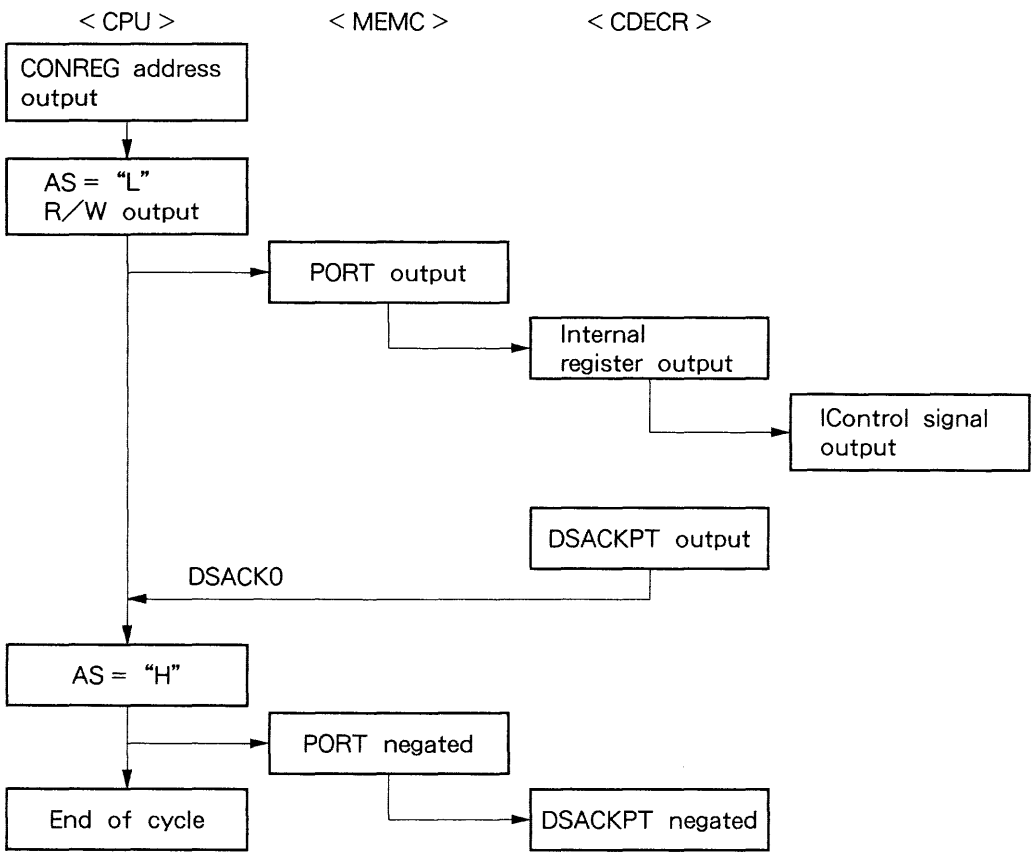
3-7-2. keyboard Buzzer

The NEWS series keyboard features a built-in buzzer which can be buzzed by a signal from the system unit. In the NWS-1500, the external oscillator circuit is activated when the keyboard buzzer port is accessed, producing the sound of a buzzer. The buzzer frequency is different depending on whether the port is read or write accessed. With READ, the tone produced is approximately 2.2kHz, with WRITE, approximately 1.4kHz. A flowchart of this process is given below.



3-8. CONTROL REGISTERS

WSC-CDECR has control registers built-in to accommodate various types of control signals. Readers are referred to a separate section for the contents of the respective registers. A flowchart of register access is given below.



3-9. DSC－008 board circuit description(NWS-1530/1580 Only)

3-9-1. Points of difference with present bitmap display controller

* First stage FIFO (cycle time: 6 clock, 240 nsec － 300 nsec).
* Second operand and mask raster operation support.
* The kanji ROM has been allocated to a portion of the FB.
* It is now possible to copy from any plane to all planes within the FB.

3-9-2. Special color bitmap board addresses

Two DIP switches on the board allow changing of addresses.

(1) Raster operation command registers

SW1	SW0	Address
0	0	Oxf0f20000~Oxf0f3ffff
0	1	Oxf0f60000~Oxf0f7ffff
1	0	Oxf0fa0000~Oxf0fbffff
1	1	Oxf0fe0000~Oxf0ffffff

(2) CRTC, status, color palette

SW1	SW0	Status	CRTC	Color palette
0	0	Oxf0f00000	Oxf0f02000	Oxf0f04000
0	1	Oxf0f40000	Oxf0f42000	Oxf0f44000
1	0	Oxf0f80000	Oxf0f82000	Oxf0f84000
1	1	Oxf0fc0000	Oxf0fc2000	Oxf0fc4000

Normally, SW1 and SW0 are both set to 1.

3-9-3. CRTC, color palette

(1) Monitor timing (NWP－515)

Drive system Non－interlaced

Pixels clock	64MHz
Number of horizontal display pixels	1024dot
Number of horizontal blanking pixels	288dot(4.5usec)
Total number of horizontal pixels	1312dot
Horizontal cycle	20.5usec
Horizontal frequency	48.78kHZ
Horizontal front porch	64dot(1usec)
Horizontal sync cycle	96dot(1.5usec)
Horizontal back porch	128dot(1.5usec)
Number of vertical display lines	768line
Number of vertical blanking lines	45line(922.5usec)
Total number of vertical lines	813line
Vertical cycle	16.660msec
Vertical frequency	60.0Hz
Vertical front porcn	31line
Vertical sync cycle	31line(61.5uaec)
Vertical back porch	39line(799.5usec)

(2) HD6445 CRTC register settings

HD644CRTC generates horizontal and vertical sync signals for the NWP－515 as well as display blanking timing. HD6445 operates on a frequency equal to the pixel clock divided by 16 because of constraints imposed by its maximum operating frequency. It is therefore possible to set display timing in units of 16 horizon－tal pixels. For this reason, HD6445 sets the following values:

Register	Register name	Setting unit	Setting value
RO	Total number of horizontal character	chr16 pixel	unitOx51
R1	Number of horizontal characters displayed	chr	Ox40
R2	Horizontal sync position	chr	Ox48
R3	Sync pulse width	chr	Ox33
R4	Total number of vertical characters	line	Ox64
R5	Total raster adjust	raster	Ox5
R6	Number of vertical characters displayed	line	Ox60
R7	Vertical sync position	line	Ox60
R8	Interlace and skew		Ox10
R9	Maximum	raster	address
Ra	Cursor 1 start raster		
Rc	Starting address 1 (high)	mem adrs	0
Rd	Starting address 1 (low)	mem adrs	0
R1b	Vertical sync position fine adjustment	raster Ox3	
R1e	Control		1Ox8

See the HD6445 user's manual for the meanings of parameters, bit positions, etc.

(3) Setting data sent to the HD6445

First the raster number for the desired address register setting is read in. Next, the setting for the data register is read in.
This ensures that data is read into the designated register. Data may be read out of readable registers in the same way.
Example: Setting register R6 to 128
1 Write 6 to the address register.
2 Write 182 to the data register.
3 Completed.
The default setting for the address register is 0xf0fc2000 and that for the data register is 0xf0fc2001.

(4) Color palette

Am81C458 (Bt548) is a video D/A converter incorporating 256 x 24 bits of color palette RAM. The DSC − 008 has a 8 − frame frame buff − er, allowing simultaneous display of 256 colors from a palette of 16.7 million. Like the CRTC, the color palette has data and control registers which allow programming as described in (3) above. The normal setting for the address register is 0xf0fc4000 and for the data register is 0xf0fc4004.
See the data sheet for a detailed description.

3-9-4. Status registers

The status registers are at the address shown in 12.2 (2). See Fig. 1.
(page 3-44, 3-45)

Status registers
(Read)

Bit 0: If the req signal status is 1, a read/write is being executed in the frame buffer (FB).
Bit 1: If the exec signal status is 1, a command is being execut − ed in the frame buffer (FB). The relation of this signal to the req signal is as follows:
req exec
0 0 : Idle
0 1 : Waiting for command to execute.
1 0 : Waiting for read/write (read/write command to FB, mask command).

1 1 : FB read/write in progress.
Bit 2: Indicates V − sync.
Bit 3: Indicates the presence of a V − sync interrupt if status is 1.
Bit 4: Indicates the presence of a command completion interrupt if status is 1.
Bit 5: Version number; 0 at present.
Bit 6: 0: B/W; 1: Color
(Write)
Bit 0: Resets the raster operation controller.
0: Reset.
1: Execute possible.
Bit 1: Inhibits the kanji ROM.
0: Reset. (In this status, the source/destination address regis − ter must be set to 0. This is to prevent ROM data from bein g output to the HD bus.)
1: Enable.
Bit 3: V − sync interrupt enable/clear.
0: Clear/disable.
1: Enable.
Bit 4: Command completion interrupt enable/clear.
0: Clear/disable.
1: Enable.

(A reset signal from the host sets all bits to 0.)

3-9-5. Raster operation command registers

The DSC − 008 is basically identical to the NWB − 225A in that frame buffer operations are possible by means of raster operation (rop) commands. The raster operation commands perform the following functions:
1) Copying from a source rectangle to a destination rectangle within one plane in the FB.
2) Copying from a source rectangle on one FB plane to destination rectangles in all planes.
3) Reads and writes from the host to the FB destination rectan − gle.
4) 1 − pixel writes in the FB.
Rop commands are conveyed using an address (A16 − A1) and data (D11 − 0) from the host.
Conveyed as address:
The register setting which is specified as a value (A16 − A15 and A6 − A1).
Setting specifying whether or not to execute the rop (A14).
Setting specifying whether or not to set the shift count (A13).
Y address (A12 − A1) (A0 is always 0 for word access.)
Conveyed as data:
Rop operating mode (D7 − D0)
Rop function (D3 − D0)
Rop mask data (D15 − D0)
Write data (D15 − D0)
Write plane setting (D7 − D)
X address (D11 − D0)

See Fig. 2.(page 3-57, 3-58)

The following registers must be set to execute a rop:

Func. register (4 bits):
Sets the 16 types of logical operations between source and desti − nation.
Specifies the plane using the four low order bits (A3 − A1) of the address. (Each plane is set.)
Mask register (16 bits):
In case of a rop, sets a mask pattern (pixels not to be changed) for the destination. (Corresponds to one word (16 aligned pixels) at the destination.)
0: Change
1: No change

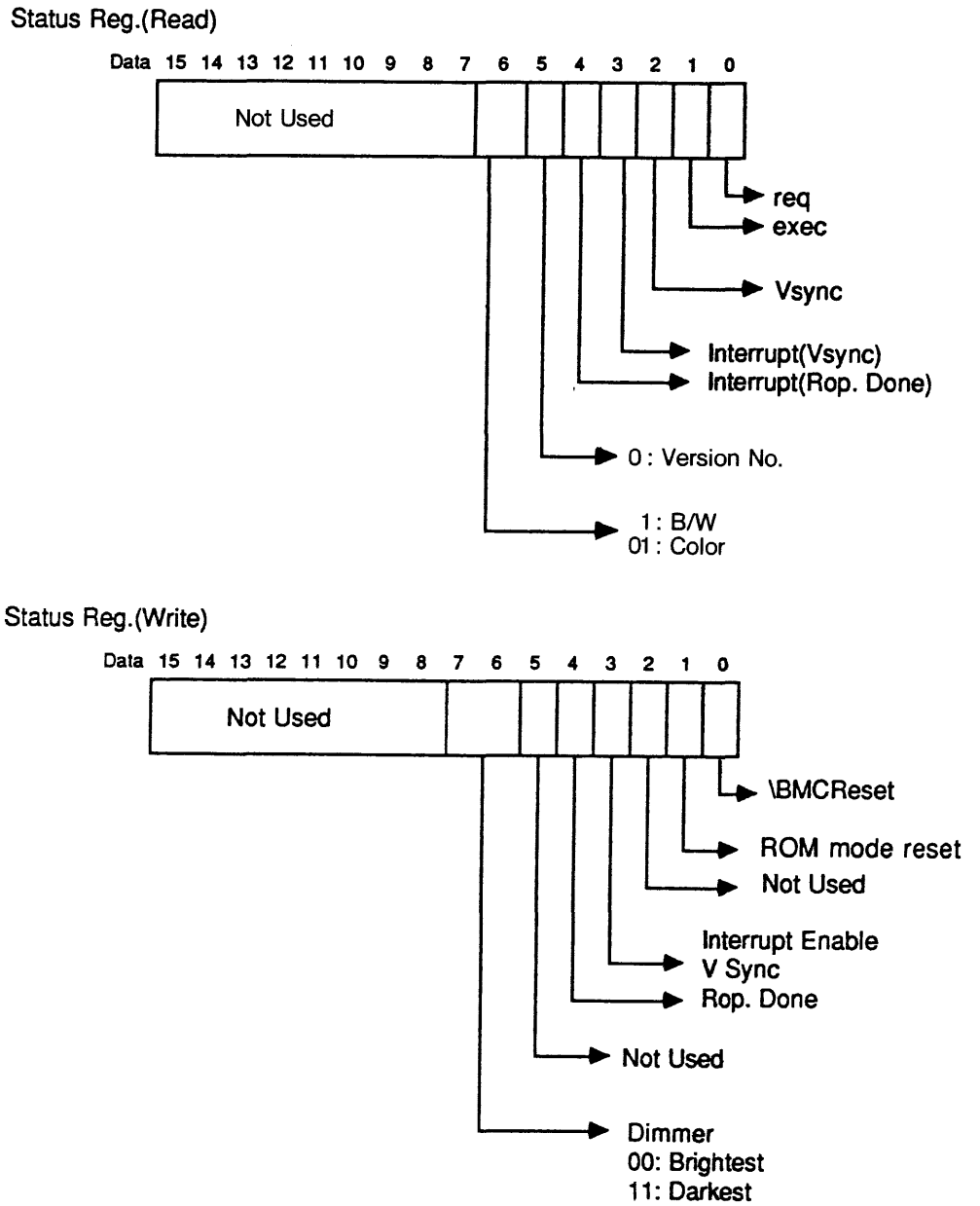
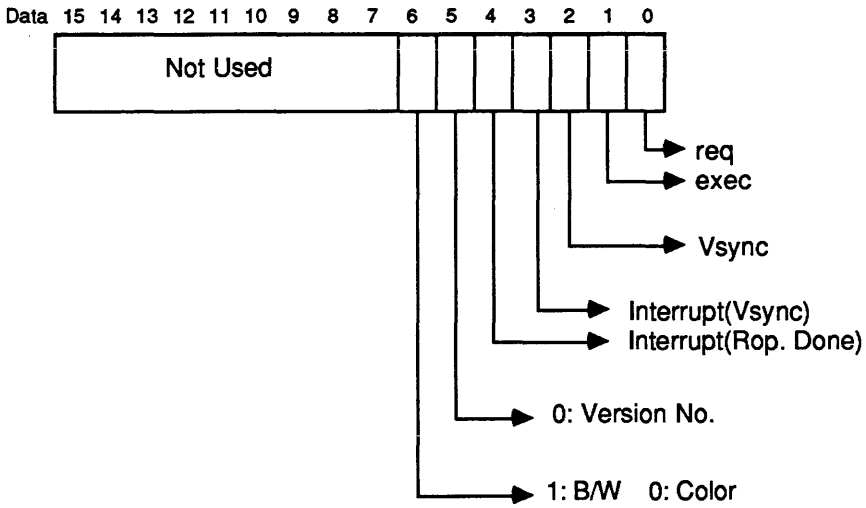
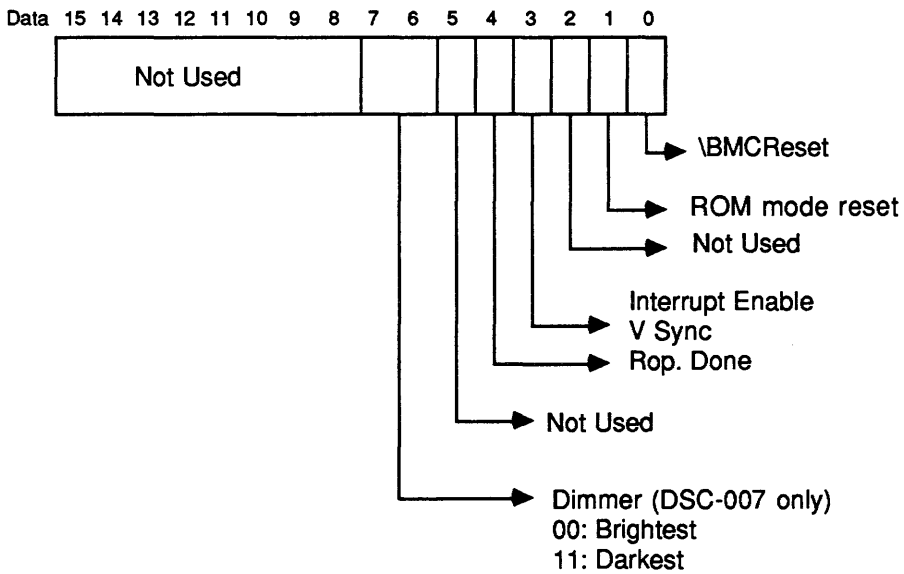


Fig. 1 Status Register

Status Reg.(Read)



Status Reg.(Write)



Data register (16 bits)
(Write): Writes data from the host to the FB.
(Read): Reads data from the FB to the host.

Shift register (4 bits):
Sets the shift number by which source data is shifted. Data is shifted either to the left or to the right depending on the direction of the X address increment set in rop mode (same direc − tion as X address).

Rop mode register (8 bits)
Sets rop execution mode.
Bit 87654321 Command
00xxxx11 Copy mode within FB (within same plane). −− Copy
01xxxx11 Copy mode within FB (from one plane to all planes). −−
PCopy

1 0 x x 1 1 0 1 Write mode from host to FB. -- HWrite
- - - - 1 - - - Increment X address to the right (valid in Copy and PCopy modes).
- - - - 0 - - - Increment X address to the left (valid in Copy and PCopy modes).
- - - - - 1 - - Increment Y address to the right (valid in Copy and PCopy modes).
- - - - - 0 - - Increment Y address to the left (valid in Copy and PCopy modes).
- - 1 - - - - - Send one to one from source to destination (valid in Copy, PCopy and HWrite modes).
- - 0 - - - - - Put 16 pixels from the source in one line at the destination (valid in Copy, PCopy and HWrite modes).
- - - 1 - - - - Do not change during rop mask execution (valid in Copy, PCopy and HWrite modes).
- - - 0 - - - - Change the rop mask in the destination word by word (valid in Copy, PCopy and HWrite modes).
1 1 0 0 1 1 1 1 FB to host read mode. -- HRead
1 0 0 0 1 1 0 0 Pixel mode. -- DirRd/DirWt/DWrite

Destination address register (X: D10 - D0, Y: A12 - A1)
Sets the rop destination X, Y address. The destination address is one of the four corners of the destination rectangle depending on the direction in which the X, Y address set in rop mode reg. is incremented.

Source address register (X: D10 - D0, Y: A12 - A1)
Sets the source destination X, Y address. The source address is one of the four corners of the destination rectangle depending on the direction in which the X, Y address set in rop mode reg. is incremented.

Limit address register (X: D10 - D0, Y count: A12 - A1)
Sets the X address (opposite the destination X address in the case of a read) of the right (left in the case of a read) edge of the destination (source in the case of a read) rectangle and number of rop execution lines minus 1 (rectangle height minus 1 in the case of a read).

Exec. flag (A14)
Requests FB read/write execution based on the set register value.

The following registers are transparent to the user, but exist in the hardware. These mask registers are used to set the unchanging portion between two words beginning or ending at any pixel on either side when writing those words. This is due to the fact that the FB uses 16 - bit words. They are set simultaneously when the destination X address is set as a rop command or when the limit X address is set.

Left mask register:
Mask for the one word at the left edge of the rectangle.
It is set to 0xc000 if the rectangle begins from the third pixel of the word.

Right mask register:
Mask for the one word at the right edge of the rectangle.
It is set to 0x1fff if the rectangle begins from the third pixel of the word.

Dot mask register:
Mask used when writing single pixels.
It is set to 0xdfff to write to the third pixel of the word.

3-9-6. DSC – 008 circuit board block diagram

FIFO:
A one – stage FIFO is provided for raster operation commands and data. It allows asynchronous operation in order to cut the host's waiting time to a minimum.

Raster operation cycle controller
This controller overseas FB read/write operations based on com – mands and CRTC from the host. The three main controller states are idle, display and command execution. The display status consists of FB refresh and send display ad – dress cycles. The controller is synchronized with H – sync during display operation and interrupts are given higher priority than
during command execution status. In command execution status there is a wait of two memory cycles.

Command execution status is the condition under which commands from the host are executed. Available operations are copy within plane (Copy), copy between planes (PCopy), write to plane (HWRite) and read from plane (HRead).
The controller is in idle status when not in one of the states described above.

Address controller (uPD6501G – 160):
Addresses needed to execute commands are maintained in gate array uPD6501G – 160. The addresses needed to define the source and destination rectangles are as follows: source rectangle X address (SRXA), source X address (SXA), source Y address (SYA), destina – tion rectangle X address (DRXA), destination X address (DXA), destination Y address (DYA). The difference between the rectangle X address and X address is that, while the rectangle X address is the X address of the rectangle, the X address is the FB address actually used for read/write operations.
These addresses are set, incremented or reduced, and altered (SRXA (DRXA) is loaded into SXA (DXA)) in command status.

Raster operation chip (WSC – SBLT):
An up – graded version of the CXD1029 used in the NWB – 225A, this chip shifts data read from the FB and performs Boolean logic operations. The CXD1029 was capable of handling a single plane, but the WSC – SBLT can handle two planes at once.

RAMDAC (Am81C458 – 80JC):
This device converts video data read from 8 – frame memory into 24 – bit form using its built – in color palette and drives the display monitor.

Fig. 3 is a block diagram of the DSC – 008 circuit board.(page 3-59, 3-60)

3-9-7. Host interface/FIFO

Two PAL's are used to decode addresses and for ACK and FIFO
control. The decode signal meanings are as follows:
/ROPAS: Raster command (decodes AS only)
/ROPDS: Raster command (AS and DS)
/CTRL: Control port, CRTC, and color palette (AS and DS)
/ROPR: Raster command access (AS only)

There are four types of timing with which the /ACK signal is returned to the host.
1) Control port: When the wait signal is high (320 nsec)
2) Raster command (write): When /FIFL is high
3) Raster command (read): When /FIFL and /ROP are both high (This controller assumes that the address data is fixed from the point at which /ACK
goes low to when /FIFL goes low.)
/Freq goes low if /FIFL id high (FIFO is empty) and /ROPDS is low (access from the host). It remains low while /FIFL is low.
/FIFL is the signal that indicates that data is in FIFO. It goes low at the next clock (F) after Freq becomes 0. After the regis − ter is set (QE is high), it goes high. This indicates that FIFO is empty.

One raster command can be loaded into FIFO. A raster command consists of data (D0 − D15) and an address (A1 − A16).
Fig. 4 is a timing chart.(page 3-61)

3-9-8. Rop registers
Execution of the command in FIFO begins when /Bust goes high.
Command execution is in two stages: register setting and FB
read/write. FB read/writes only takes place if A14 of the command address portion is 1. Register setting is based on the preceding QA. Registers set using commands are as follows:

QA	Register
L->H:	Rop Mode Register(/SCOMR)
	Source Rectangle X, Y Address(SSOUR, /SSOUR)
	Destination Rectangle X, Y Address(SDEST, /SDEST)
	Limit X Address(SLIMIT)
	Rop Mask(/SROPM)
	Data Register(/SDREG)
H:	Source X, Y Address(/SSOUR)
	Limit Y-Counter(/SLIMIT)
	Destination X, Y Address(/SDEST)
H->L:	Rop Function(SROPF01-67)
	Right/Left Mask Register(SDEST, SLIMIT)
	Shift Counter(XSSC)
	Dot Mask Register(XSDWR)
	Read Plane Register

The req flag is set when QB is high and CA14 is 1. It directs the rop mode controller to perform a memory read/write.
HDREAD is the signal for outputting to the DH bus (HD0 − 15),not data from the host but rather data from the raster chip's ROM. It is active during read requests from the host and when copies between planes are being executed.
The /ps01 signal is for reading to the raster chip. It permits reading of the data corresponding to the read plane reg. setting.
It is active when HDREAD is active and the source is not ROM.

3-9-9. Raster operation cycle controller (ROCC)
This controls rop execution (raster chip, address register, and memory) based on commands from the host (when CA14 is high).

(1) Mode registers

COM01:

00 Copy (FB −> FB, copy within same plane)

01 PCopy (copy from one plane in FB −> other planes in FB)

****

10 HWrite (Host −> FB), Dot Write

11 HRead (FB −> Host)

These are further modified by COM2 and COM3.

COM2: Puts pattern from source, a 16 − pixel wide rectangle, in a one − line destination.

COM3: Sets the mask pattern from the host once each write for a masked rop.

Also, during Copy or PCopy execution within FB, it is necessary to return the copy direction based on the source rectangle and destination rectangle positions.

Source X address < destination X address

−> Direction in which the X address is reduced (to the left),

XINC is 0. Otherwise, direction in which the X address is in − creased (to the right), XINC is 1.

Source Y address < destination Y address

−> Direction in which the Y address is reduced (to the left),

YINC is 0. Otherwise, direction in which the Y address is in − creased (to the right), YINC is 1.

XINC: Signal which controls the address chip (uPD65013G)

0: Direction in which the X address is reduced (both source and destination)

1: Direction in which the X address is increased (both source and destination)

YINC: Signal which controls the address chip (uPD65013G)

0: Direction in which the Y address is reduced (both source and destination)

1: Direction in which the Y address is increased (both source and destination)

XEDR: Signal which controls the raster chip (raster chip XEDR)

Switches internal shift register input.

0: Switches shift register input to data register.

1: Switches shift register input to data from FB.

DOTM: Signal which controls the raster chip and exec flag

0: Read/write in word (16 − pixel) units.

1: Read/write in pixel units.

(2) Req and exec flags

ROCC start, stop and wait are controlled by the req and exec flags.

rec	exec	description
0	0	Stop/idle (completion of command)
1	0	Start (request to begin command execution)
0	1	Wait (wait to read the write or mask data from the host)
1	1	Executing (FB read/write being executed)

The timing for setting the rec flag is set by QB if the rop command exec flag (A14) is 1.

The exec flag is set by /NCK except in the pixel mode.

The timing for clearing the req flag is quite complicated.

Either /clreq0 or /clreq1 is used as the req flag clear signal.

This is determined using a logical OR operation based on the rop mode.

```
/clreq0:
        Copy/PCopy Mode                                  (f)lwt & !/ylast
        Copy/PCopy (Continue) with Mask                  (f)(l)wt
        Copy/PCopy Continue                              (f)lwt & !/ylast

             Write (Continue)  with Mask Mode                 (f)(l)(n)(p)wt
                                        [/NWR /LMK /PRED] = [x,  x,  x]

             Read Mode                                        (f)(l)rd
                                        [/NWR /LMK /PRED] = [x,  x,  1]
                     Not cleared in (f)(l)p(n).
                                        [/NWR /LMK /PRED] = [x,  x,  0]

             Reset

      /clreq1:
             Write                                            (f)(l)(p)wt
                                        [/NWR /LMK /PRED] = [1,  x,  x]
                                                              (f)(p)wt
                                        [/NWR /LMK /PRED] = [0,  1,  x]
                                                              (f)lpnwt
                                        [/NWR /LMK /PRED] = [0,  0,  0]
                     Not cleared in (f)lnwt.
                                        [/NWR /LMK /PRED] = [0,  0,  1]

             Write Continue Mode                              fpwt
                                        [/NWR /LMK /PRED] = [x,  1,  0]
                                                              (f)l(p)wt
                                        [/NWR /LMK /PRED] = [1,  0,  x]
                                                              (f)lnwt
                                        [/NWR /LMK /PRED] = [0,  0,  1]
                     Not cleared in flpnwt or (f)wt.
                                        [/NWR /LMK /PRED] = [0,  0,  0]
                                        [/NWR /LMK /PRED] = [x,  1,  1]

             Reset

      The exec flag is cleared when the rop command is completed.
      /clexec:
             Copy and PCopy Mode                  (f)lwt & !ylast
             Read and Write Mode                  (f)lwt/rd & !ylast
             Reset
```

The commencement of rop command execution is controlled by the /busy signal. /Busy is high during two types of timing based on command CA14. /Busy is high in the following circumstances:

a. It is maintained at high when QA is high, even if req or exec change.
b. During read/writes from the host.
c. When rop mask data is written from the host.
d. Circumstances other than those noted above.

(3) State

ROCC status is determined by the rop mode as well as the posi − tions of the source and destination rectangles. The status dif − fers depending on the size of the rectangles. The following describes /NWR and /PRD which determine the ROCC status when not in the rop mode.

/NWR: Indicates that the number of words in the source rectangle (size when aligned with a scale of 16 − pixel units) is fewer than the number of words in the destination rectangle.

/NWR is 0 when XINC = 1 and DRXA[0 − 3] − SRAX[0 − 3] < LXA[0 − 3]
/NWR is 0 when XINC = 0 and DRXA[0 − 3] − SRAX[0 − 3] > LXA[0 − 3]
/NWR is 1 in cases other than the above.
/PRD: Indicates that the number of words in the source rectangle (size when aligned with a scale of 16 − pixel units) is greater than the number of words in the destination rectangle.
/PRD is 0 when XINC = 1 and DRXA[0 − 3] < SRAX[0 − 3]
/PRD is 0 when XINC = 0 and DRXA[0 − 3] > SRAX[0 − 3]
/PRD is 1 in cases other than the above.
(The number of words are equal if /NWR and /PRD are both 0.)

ROCC status is shown by /ROP, CP, WRITE, /FMK, /LMK and /PRED.
/ROP: Requests an FB read/write.
CP: 1: Copy and PCopy mode; 0: HWrite and HRead
WRITE: 1: Write to FB; 0: Read from FB
/FMK: Indicates the first word in one line of a rectangle. (indicates that a left (right) mask is necessary to write to the FB, a right mask if XINC is 1 and a left mask if XINC is 0.)
/LMK: Indicates the last word in one line of a rectangle. (indi − cates that a left (right) mask is necessary to write to the FB, a right mask if XINC is 1 and a left mask if XINC is 0.)
/PRED: Indicates that the source rectangle X address pixel posi − tion is greater (less) than the destination rectangle X address pixel position and that two initial reads are necessary (when /PRD is 0).
ROCC states are described as follows:

```
/ROP:    0: -    1: W
/FMK:    0: f    1: -
/LMK:    0: l    1: -
/PRED:   0: p    1: -
CP:      0: -    1: c
WRITE:   0: rd   1: wt
```

(Note: Not indicated as a state when writing the last line when
/NWR is 0.)
For example, /ROP, CP, WRITE, /FMK, /LMK, and /PRED behave as follows:

```
(0, 1, 1, 1, 1, 1) -> cwt, (0, 0, 0, 0, 0, 0) -> flprd
(1, 0, 1, 0, 1, 0) -> Wfpwt
(1, 0, 1, 1, 1, 1) -> Wrd, (1, 1, 1, 1, 1, 1) -> Wwt
```

ROCC status changes for one line only are shown below. States are shown as follows:

a) FB->FB(COM01:00)

Normal(COM0123: 0000)

```
(xpn)    (x: /XLAST, p: /PRD, n: /NWR)

(01x)    flcrd. flcwt
(00x)    flpcrd. flcrd. flcwt

(111)    fcrd. fcwt. lcrd. lcwt
(101)    fpcrd. fcrd. fcwt. lcrd. lcwt
(110)    fcrd. fcwt. lncwt
(100)    fpcrd. fcrd. fcwt. lncwt
```

```
      (111)    fcrd. fcwt. crd. cwt... lcrd. lcwt
      (101)    fpcrd. fcrd. fcwt. crd. cwt... lcrd. lcwt
      (110)    fcrd. fcwt. crd. cwt.... lncwt
      (100)    fpcrd. fcrd. fcwt. crd. cwt.... lncwt

MASK(0001)

      (01x)    flcrd. (Wflcwt). flcwt
      (00x)    flpcrd. flcrd. (Wflcwt). flcwt

      (111)    fcrd. (Wfcwt). fcwt. lcrd. (Wlcwt). lcwt
      (101)    fpcrd. fcrd. (Wfcwt). fcwt. lcrd. (Wlcwt). lcwt
      (110)    fcrd. (Wfcwt). fcwt. (Wlcwt). lncwt
      (100)    fpcrd. fcrd. (Wfcwt). fcwt. (Wlncwt). lncwt

      (111)    fcrd. (Wfcwt). fcwt. crd. (Wcwt). cwt... lcrd. (Wlcwt). lcwt
      (101)    fpcrd. fcrd. (Wfcwt). fcwt. crd. (Wcwt). cwt... lcrd. (Wlcwt). lcwt
      (110)    fcrd. (Wfcwt). fcwt. crd. (Wcwt). cwt.... (Wlcwt). lncwt

      (100)    fpcrd. fcrd. (Wfcwt). fcwt. crd. (Wcwt). cwt.... (Wlcwt). lncwt

CONTM(0010)

      (01x)    flcrd. flcwt
      (00x)    flpcrd. flcrd. flcwt

      (111)    fcrd. fcwt. lcwt
      (101)    fpcrd. fcrd. fcwt. lcwt
      (110)    fcrd. fcwt. cwt.... lncwt
      (100)    fpcrd. fcrd. fcwt. cwt.... lncwt

CONTM Mask(0011)

      (01x)    flcrd. (Wflcwt). flcwt
      (00x)    flpcrd. flcrd. (Wflcwt). flcwt

      (111)    fcrd. (Wfcwt). fcwt. (Wlcwt). lcwt
      (101)    fpcrd. fcrd. (Wfcwt). fcwt. (Wlcwt). lcwt
      (110)    fcrd. (Wfcwt). fcwt. (Wcwt). cwt.... (Wlcwt). lncwt
      (100)    fpcrd. fcrd. (Wfcwt). fcwt. (Wcwt). cwt.... (Wlcwt). lncwt
```

b)MEM->FB(10)

```
Normal(1000)

      (xpn)
      (01x)    (Wflwt). flwt
      (001)    (Wflpwt). flpwt. (Wflwt). flwt
      (000)    (Wflpwt). flpnwt. flwt

      (111)    (Wfwt). fwt. (Wlwt). lwt
      (101)    (Wfpwt). fpwt. (Wfwt). fwt. (Wlwt). lwt
      (110)    (Wfwt). fwt. lnwt
      (100)    (Wfpwt). fpwt. (Wfwt). fwt. lnwt

      (111)    (Wfwt). fwt. (Wwt). wt... (Wlwt). lwt
      (101)    (Wfpwt). fpwt. (Wfwt). fwt. (Wwt). wt... (Wlwt). lwt
      (110)    (Wfwt). fwt. (Wwt). wt.... lnwt
      (100)    (Wfpwt). fpwt. (Wfwt). fwt. (Wwt). wt.... lnwt
```

MASK(1001)

```
(01x)   (Wflwt). flwt
(001)   (Wflpwt). flpwt. (Wflwt). flwt
(000)   (Wflpwt). flpnwt. flnwt

(111)   (Wfwt). fwt. (Wlwt). lwt
(101)   (Wfpwt). fpwt. (Wfwt). fwt. (Wlwt). lwt
(110)   (Wfwt). fwt. (Wlwt). lnwt
(100)   (Wfpwt). fpwt. (Wfwt). fwt. (Wlwt). lnwt

(111)   (Wfwt). fwt. (Wwt). wt... (Wlwt). lwt
(101)   (Wfpwt). fpwt. (Wfwt). fwt. (Wwt). wt... (Wlwt). lwt
(110)   (Wfwt). fwt. (Wwt). wt.... (Wlwt). lnwt
(100)   (Wfpwt). fpwt. (Wfwt). fwt. (Wwt). wt.... (Wlwt). lnwt
```

CONTM(1010)

```
(01x)   (Wflwt). flwt
(001)   (Wflpwt). flpwt. (Wflwt). flwt
(000)   (Wflpwt). flpwt. flnwt

(111)   (Wfwt). fwt. lwt
(101)   (Wfpwt). fpwt. (Wfwt). fwt. lwt
(110)   (Wfwt). fwt. wt.... lnwt
(100)   (Wfpwt). fpwt. (Wfwt). fwt. wt.... lnwt
```

c)FB->MEM(11)

Normal(1100)

```
(xpn)
(01x)   flrd. (Wflrd)
(00x)   flprd. flrd. (Wflprd)

(11x)   frd. (Wlrd). lrd. (Wfrd)
(10x)   fprd. frd. (Wlrd). lrd. (Wfprd)

(11x)   frd. (Wrd). rd... (Wlrd). lrd. (Wfrd)
(10x)   fprd. frd. (Wrd). rd... (Wlrd). lrd. (Wfprd)
```

Fig. 5 gives the memory timing for one cycle in each mode.(page 3-62, 3~63)

3-9-10. Address registers

(1) uPD65013G

FB addresses which affect rop are in uPD65013G.

```
A12 - 1:        Y address setting data (input)
D11 - 0:        X address setting data (input)
RA18 - 1:       FB address (source/destination X[9 - 0] Y[11 - 0])(output)
HD12 - 15:      Rop chip data (output)
BD3 - 0:        DH12 - 15 data (input)

SRCXPR:         Signal to load the D11 - 0 value in SRXA (input)
/SRCXLD1 - 4:   SXA load signal, 0: Load SRXA value in SXA; 1: Hold (input)
/SRCXUP:        16 added to SXA by the clock (SRCXCX) when 0, but sub - tracted when 1
SRCXCX:         SXA clock (input)
```

SRCXEN: SXA clock enable signal (input)

DESTXPR: Signal to load the D11 − 0 value in DRXA (input)
/DESTXLD: DXA load signal, 0: Load DRXA value in DXA; 1: Hold (input)
/DESTXUP: 16 added to DXA by the clock (SRCXCX) when 0, but subtracted when 1
DESTXCX: DXA clock (input)
DESTXEN: DXA clock enable signal (input)

/SRCYLD: Signal to load the A12 − 0 value in SYA (input)
/SRCYUP: 1 added to SYA by the clock (SRCYCK) when 0, but sub − tracted when 1
SRCYCK: SYA clock (input)
SRCYEN: SYA clock enable signal (input)

/DESTYLD: Signal to load the A12 − 0 value in SYA (input)
/DESTYUP: 1 added to DYA by the clock (SRCYCK) when 0, but sub − tracted when 1
DESTYCK: DYA clock (input)
DESTYEN: DYA clock enable signal (input)

SETWX: Signal to load the D11 − 0 value in LXA (input)
/SETWY: Signal to load the A12 − 0 value in YC (input)
YCLK: Clock for reducing YC (input)

XSLM: Signal for setting the left mask of the raster op. chip. SLIMIT is unchanged if the XINC signal is 1 and SDEST is 0. The mask is set at the trailing edge of this signal. (output)

XSRM: Signal for setting the right mask of the raster op. chip. SDEST is unchanged if the XINC signal is 1 and SLIMIT is 0. The mask is set at the trailing edge of this signal. (output)

XELM: Signal for enabling the left mask of the raster op. chip. Becomes 0 (enable) when XINC is 1, /PRERM is 0 and /CLRERM is 1 or if XINC is 0 and XLASTIN is 1. Mask is enabled when set to 0. (output)

XERM: Signal for enabling the right mask of the raster op. chip. Becomes 0 (enable) when XINC is 1 and XLASTIN is 1 or if XINC is 0, /PRERM is 0 and /CLRERM is 1. Mask is enabled when set to 0. (output)

/XLAST: Becomes 0 when DXA and LXA are the same value. Used by ROCC. (Since DXA is used, DXA and SXA must be set to the same value when reading from the FB.) (output)

/YLAST: Becomes 0 when the value of YC is 0. Used by ROCC. (output)

/GENSCC: Switches data output to HD12 − 15. When 0, data required to set the rop chip shift count is output. (DRXA[0 − 3] − SRXA[0 − 3]) When 1, the value of BD0 − BD3 is output unchanged. (input)

/GENEN: Signal for enabling HD12 − 15. (input)
/RAEN: Signal for enabling RA0 − 18. (input)
/SELOR1, 2
/SELG: Switches data output on top of RA0 − 18. 0: Destination address; 1: Source address (input)

XINC: X address increase/decrease direction (input)
XLASTIN: XELM, XELR control signal. (input)
/PRERM, /CLRERM

/NWR: Control signal input to ROCC
0 when XINC=1 and DRXA[0 − 3] − SRAX[0 − 3] < LXA[0 − 3]; 0 when XINC=0 and DRXA[0 − 3] − SRAX[0 − 3] > LXA[0 − 3]; 1 otherwise. (output)

/PRD: Control signal input to ROCC
0 when XINC=1 and DRXA[0 − 3] − SRAX[0 − 3] < LXA[0 − 3]; 0 when XINC=0 and DRXA[0 − 3] − SRAX[0 − 3] > LXA[0 − 3]; 0 when XINC=1 and DRXA[0 − 3] < SRAX[0 − 3]; 0 when XINC=0 and DRXA[0 − 3] > SRAX[0 − 3]; 1 otherwise. (output)

/CLRDEST: Signal to clear destination X address[0 − 3].
/SFH: Signal to clear source X address[0 − 3].

(2) Control timing

CA12 − 1 and HD15 − 4 are used to set the address registers. There − fore they are valid after commands written from the host are input to FIFO until the next input is received. (They must be maintained at least when QA goes from low to high and while QA is high and when QA goes from high to low.) SSOUR, SDEST and SLIMIT are generated by QA.

RA18 − 1 is maintained from when /SELOR1, 2 and /SELG change to when the address increases or decreases (ADCK), or until a new value is set by the host (SSOUR, SDEST). In order to make the timing of ADCK, SSOUR and SDEST easier, LS373 is latched when fc is high. Therefore ADCK, SSOUR and SDEST can occur anytime when fc is low.

The latched output becomes MA15 − 0 and a FB address. (If only DRAM were used, it could be maintained by the /ras and /cas trailing edges only, but since ROM is used too, it is latched.

WPB3 − 0 (HD15 − 12 of uPD65013G) is a data signal from the rop chip's mask, shift and rop func register. It must be maintained by the trailing edge of QA (SROPF, XSLM, XSRM, XSSC). (When WPB3 − 0 sets the raster chip shift count, the value set at the leading edge of QA (DRXA[0 − 3] − SRXA[0 − 3]) is used. Therefore, QA must last a minimum of 60 nsec) This data is used by /SROPF, XSLM, XERM, XSSC and XSDWR.

XELM and XERM must be maintained when a mask is set in the FB (write per bit is used, so maintenance is necessary for 35 nsec after the /ras trailing edge).

/NWR and /PRD are used by ROCC, so they must be maintained while /NCK is low.

However, they change when an address is set by the host or due to XINC in the rop mode, so it is sufficient if there is a period of 70 nsec between the SSOUR, SDEST, and SLIMIT leading edges and the /NCK leading edge.

/XLAST is used to determine the next status using ROCC. There – fore, it must be maintained by /NCK. /XLAST changes due to ADCK, so the period between the ADCK leading edge and /NCK leading edge must be a minimum of 75 nsec
/YLAST is the concluding condition for ROCC, so it must be main – tained by /rclr.
/GENSCC must be maintained during shift setting (while QA is high).
/SELOR1, 2 and /SELG, in order to switch addresses, must last a minimum of 40 nsec to the trailing edges of /res and /cas for the FB and for a minimum of 300 nsec until the leading edge of fc for the kanji ROM.
XINC is used by XSLM, XSRM, XERM, XELM, /PRD and /NWR, so it must be maintained for 35 nsec from the /ras trailing edge for regis – ter setting and at the leading edge of /NCK.
XLATIN, /PRERM and /CLRERM are used by XERM and XELM, so they must be maintained for 35 nsec from the /ras trailing edge.
The address registers are set by the host (SDEST, SSOUR, and SLIMIT), but can be changed by ADCK. For this reason, /XINC, /YINC, /LMK, WRITE, COMO and 1 must be maintained from the lead – ing to the trailing edge of ADCK.

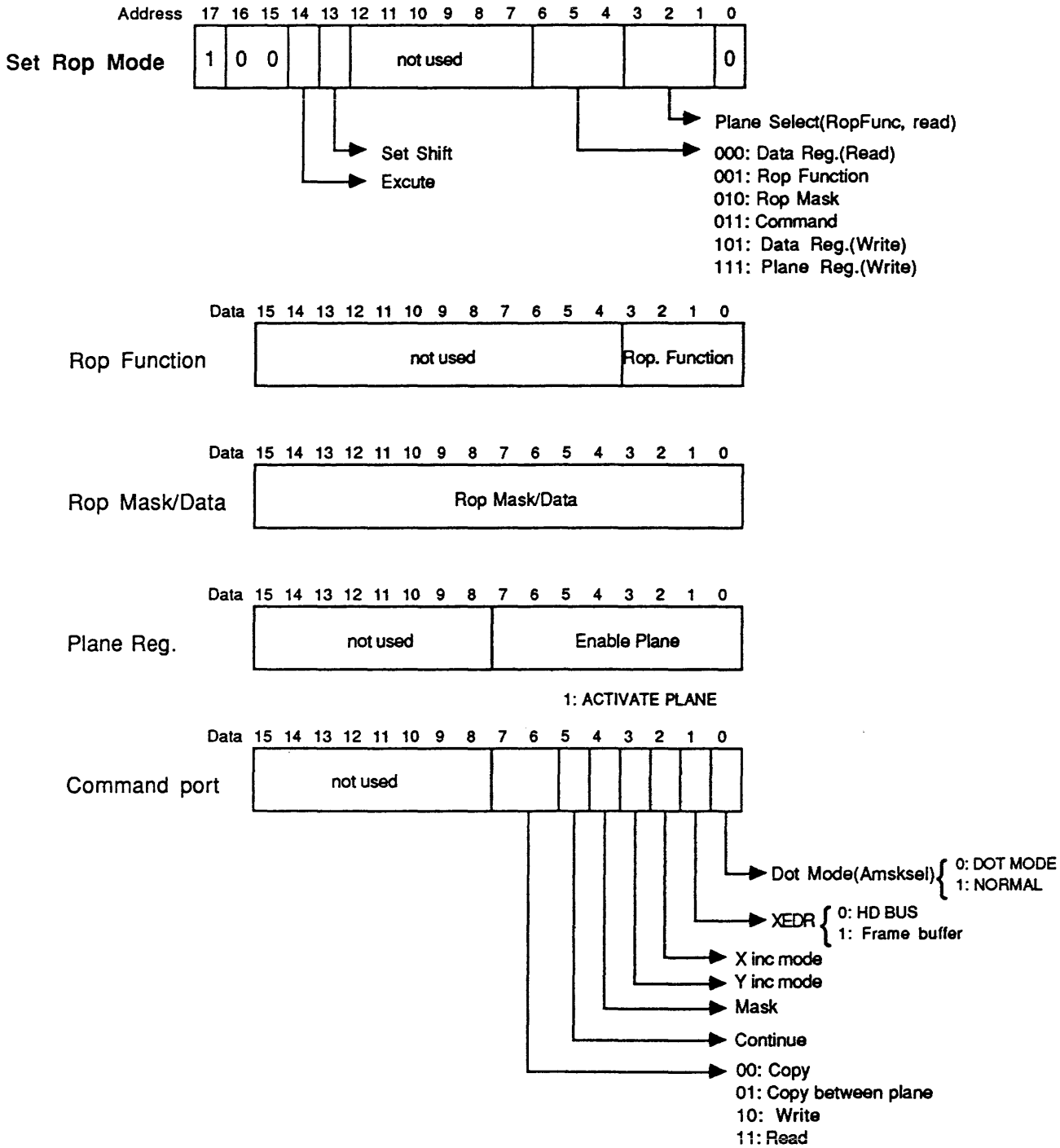
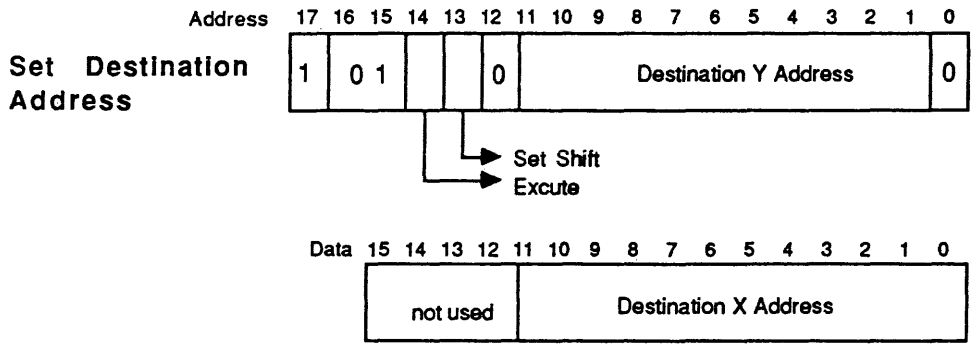
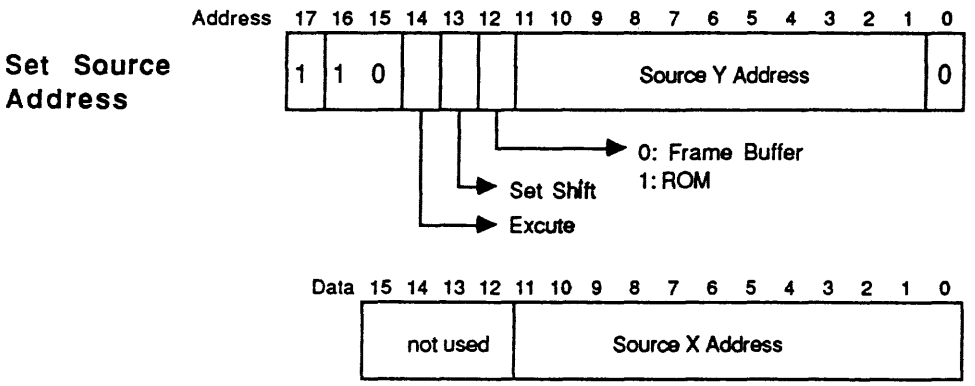


Fig. 2 Raster operation commands (1/2)





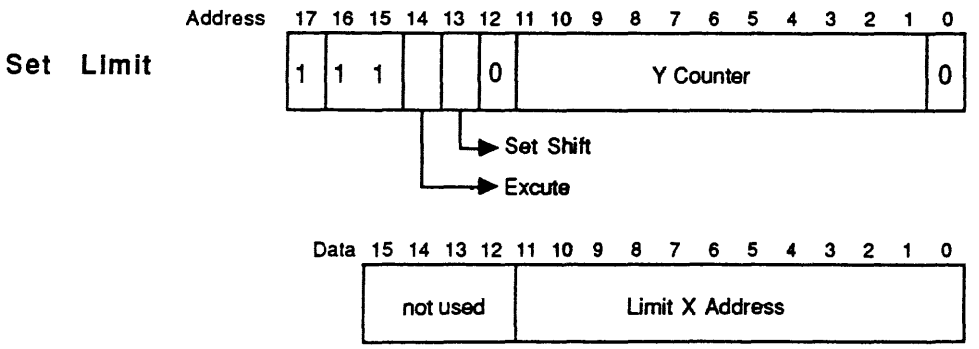


Fig. 2 Raster Operation Commands (2/2)

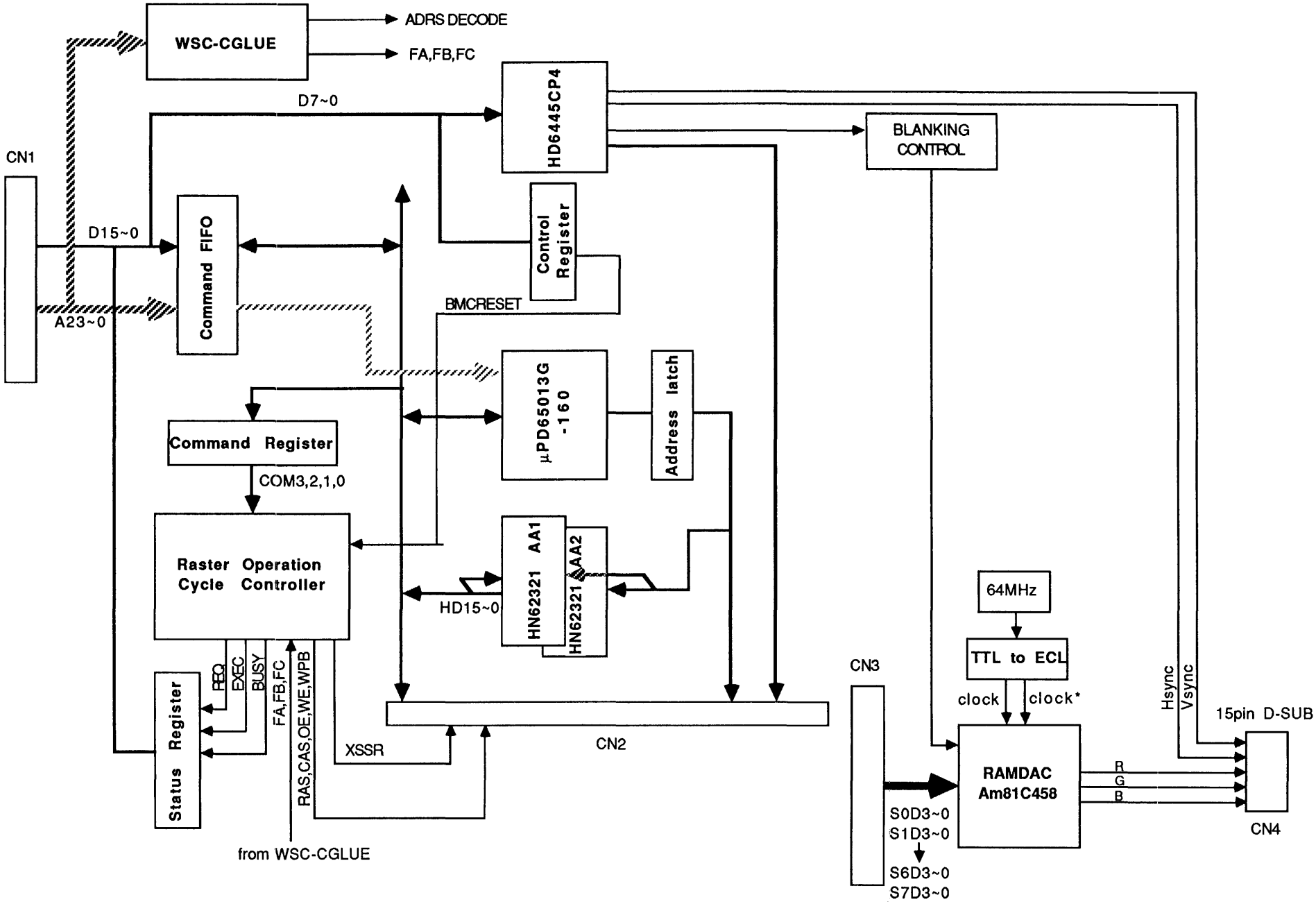


Fig. 3 DSC－008 block diagram (1/2)

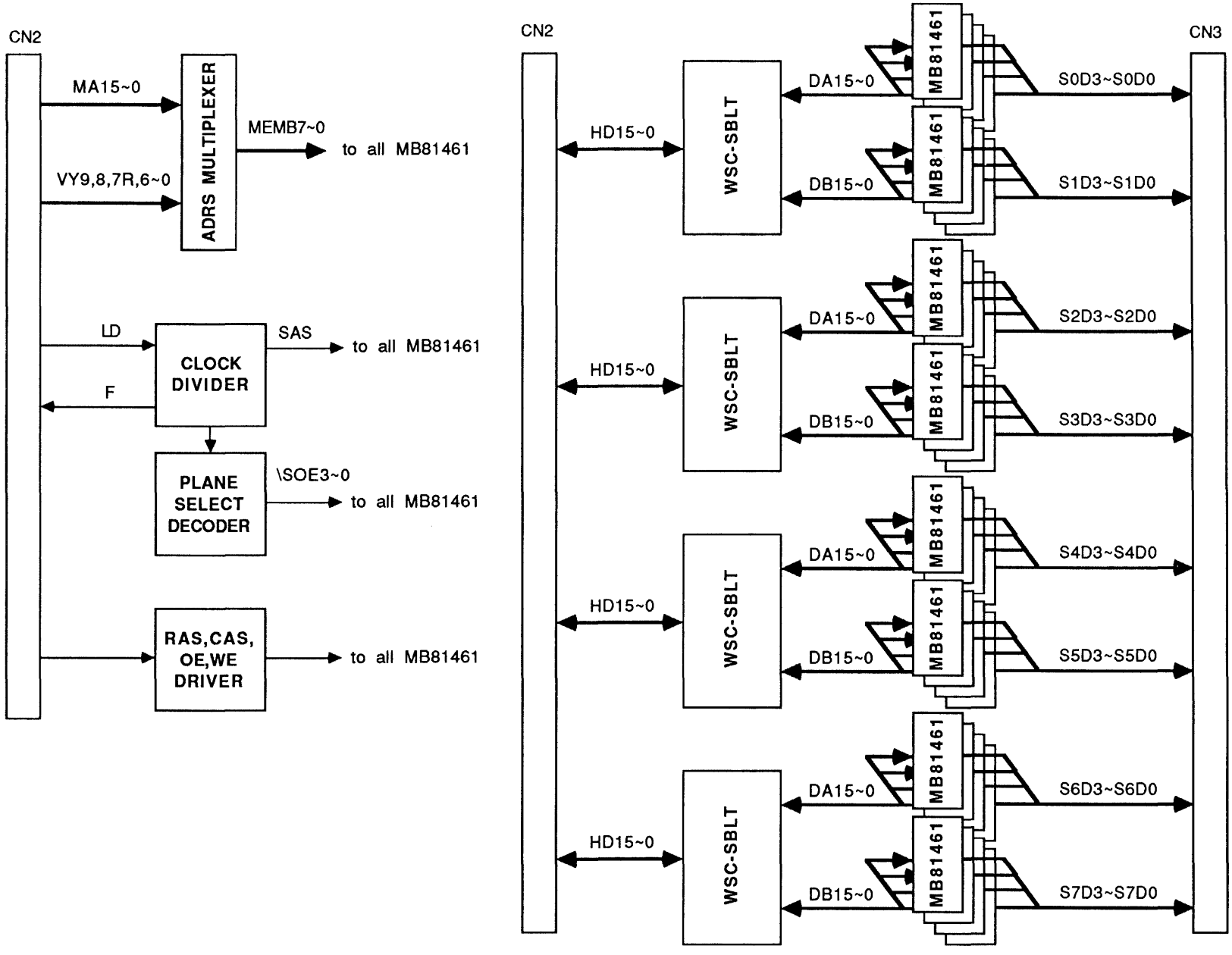


Fig. 3 DSC－008 block diagram (EM－6 daughterboard) (2/2)

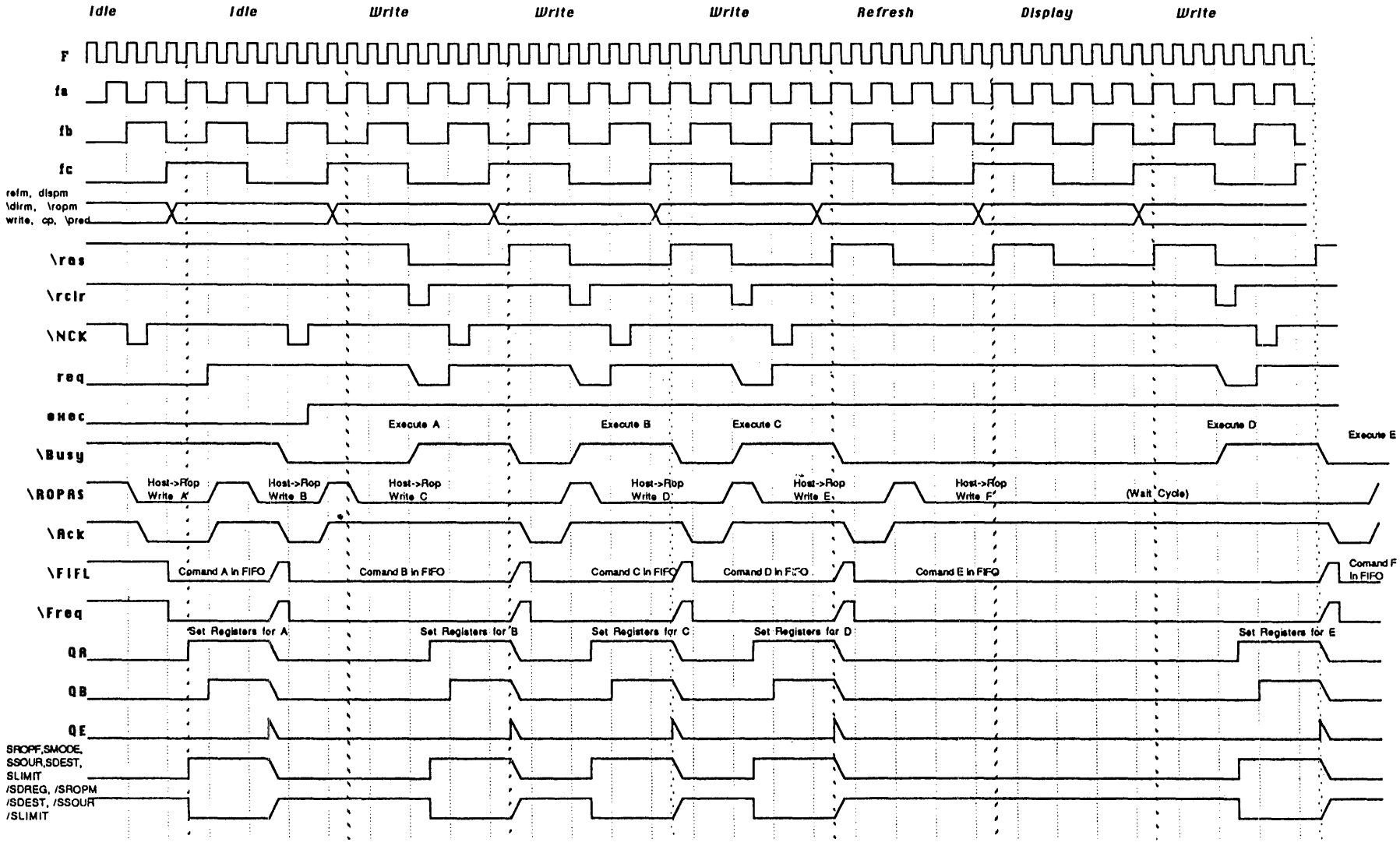


Fig. 4 Host interface timing chart

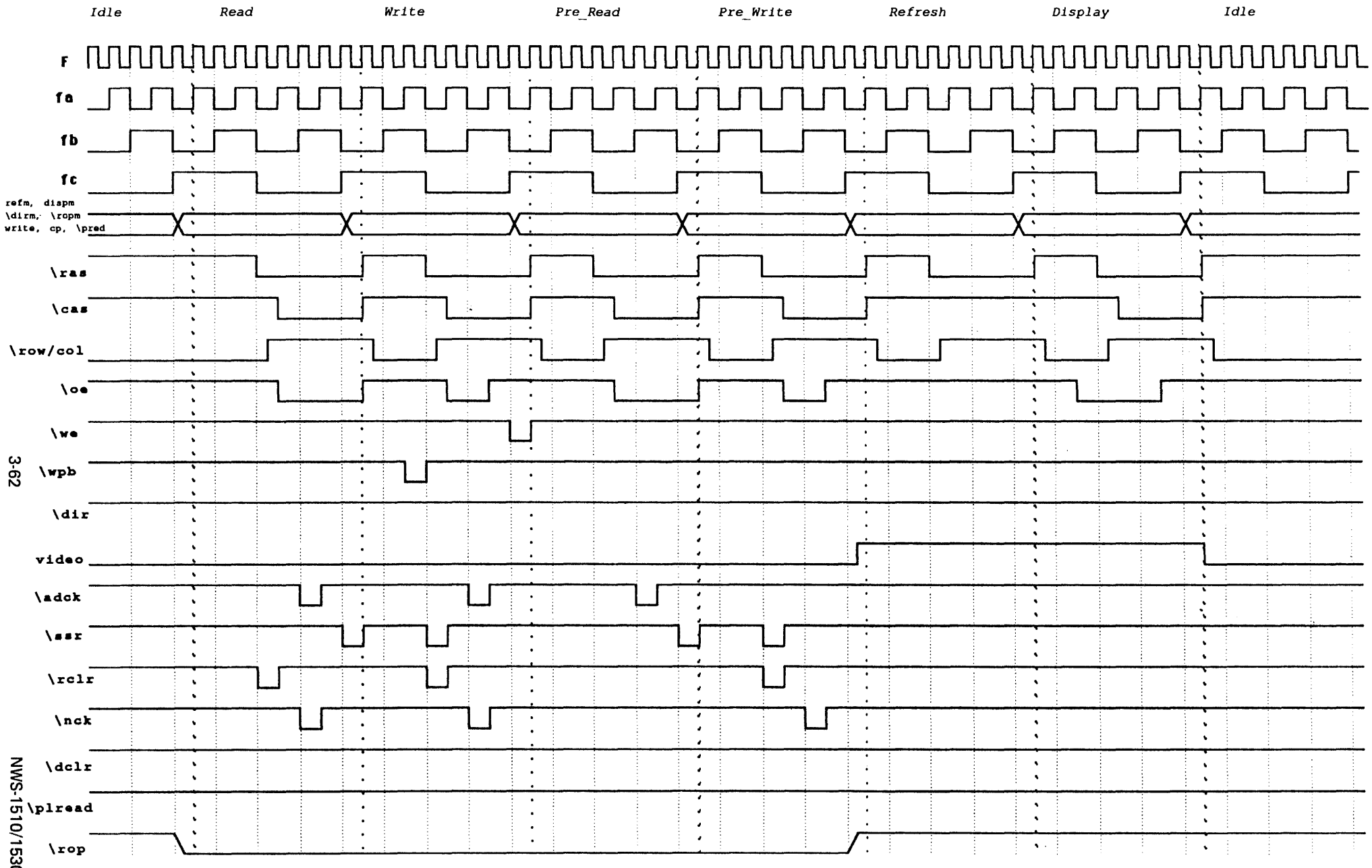


Fig. 5 Memory timing chart (1/2)

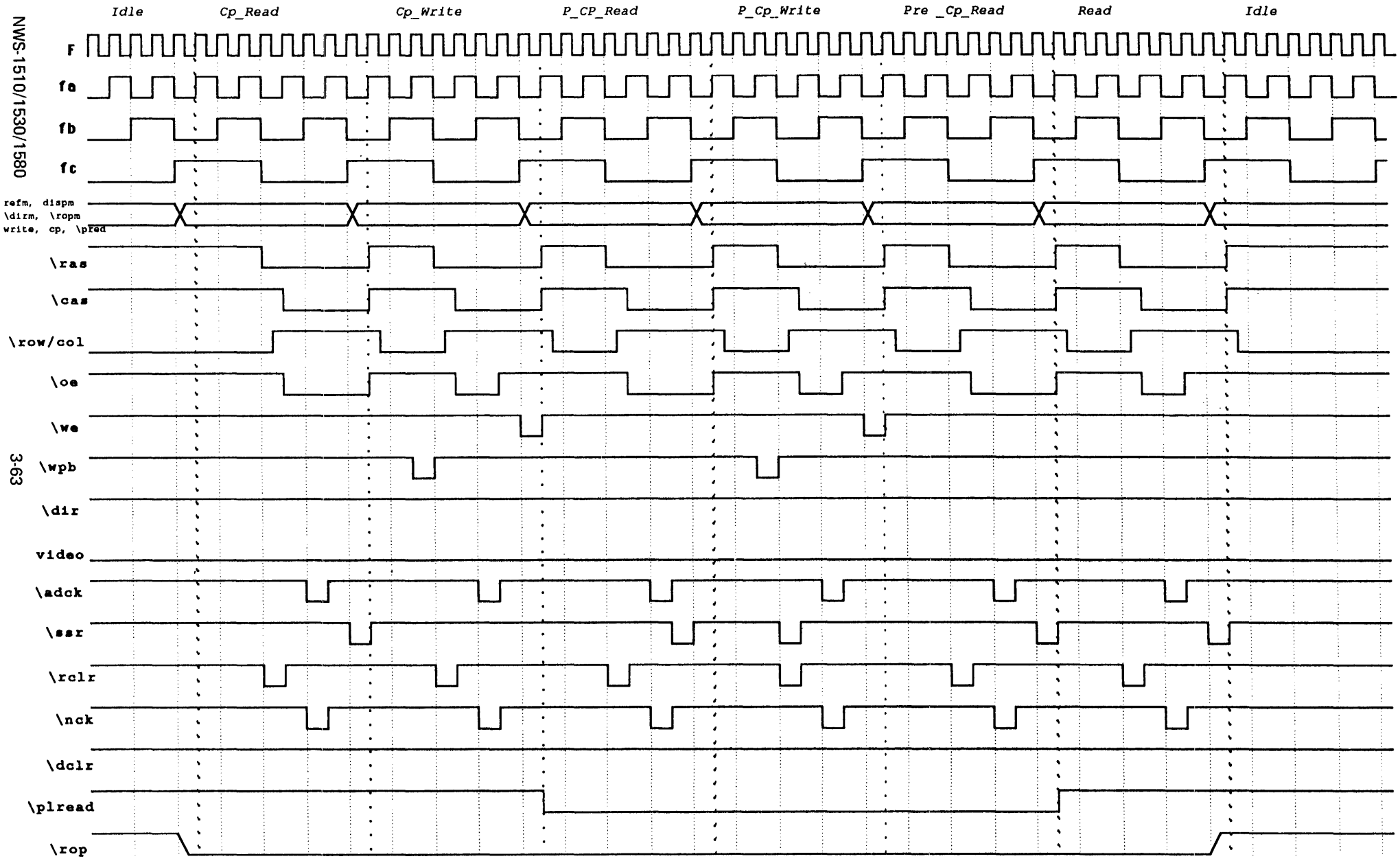


Fig.5 Memory timing chart (2/2)

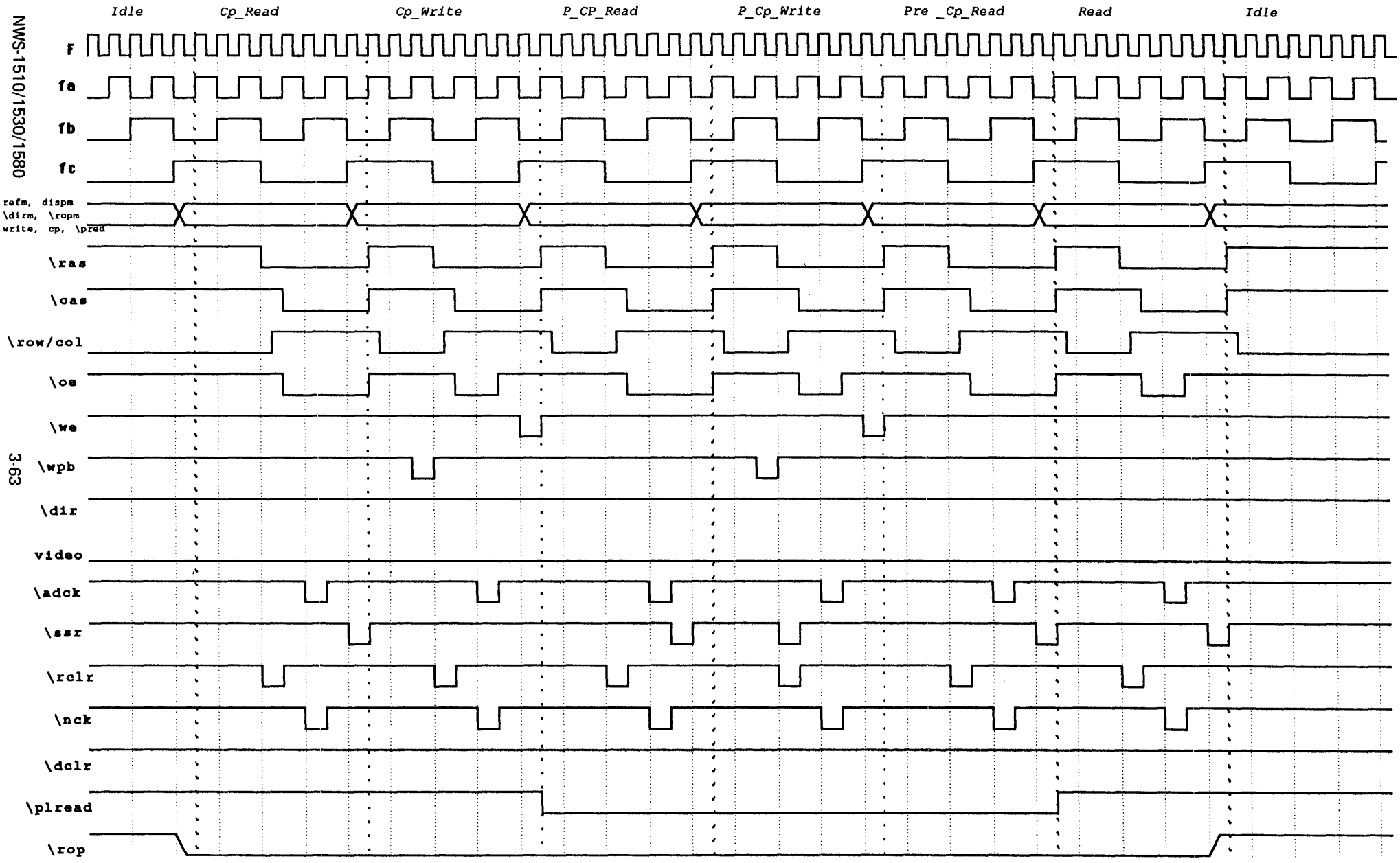
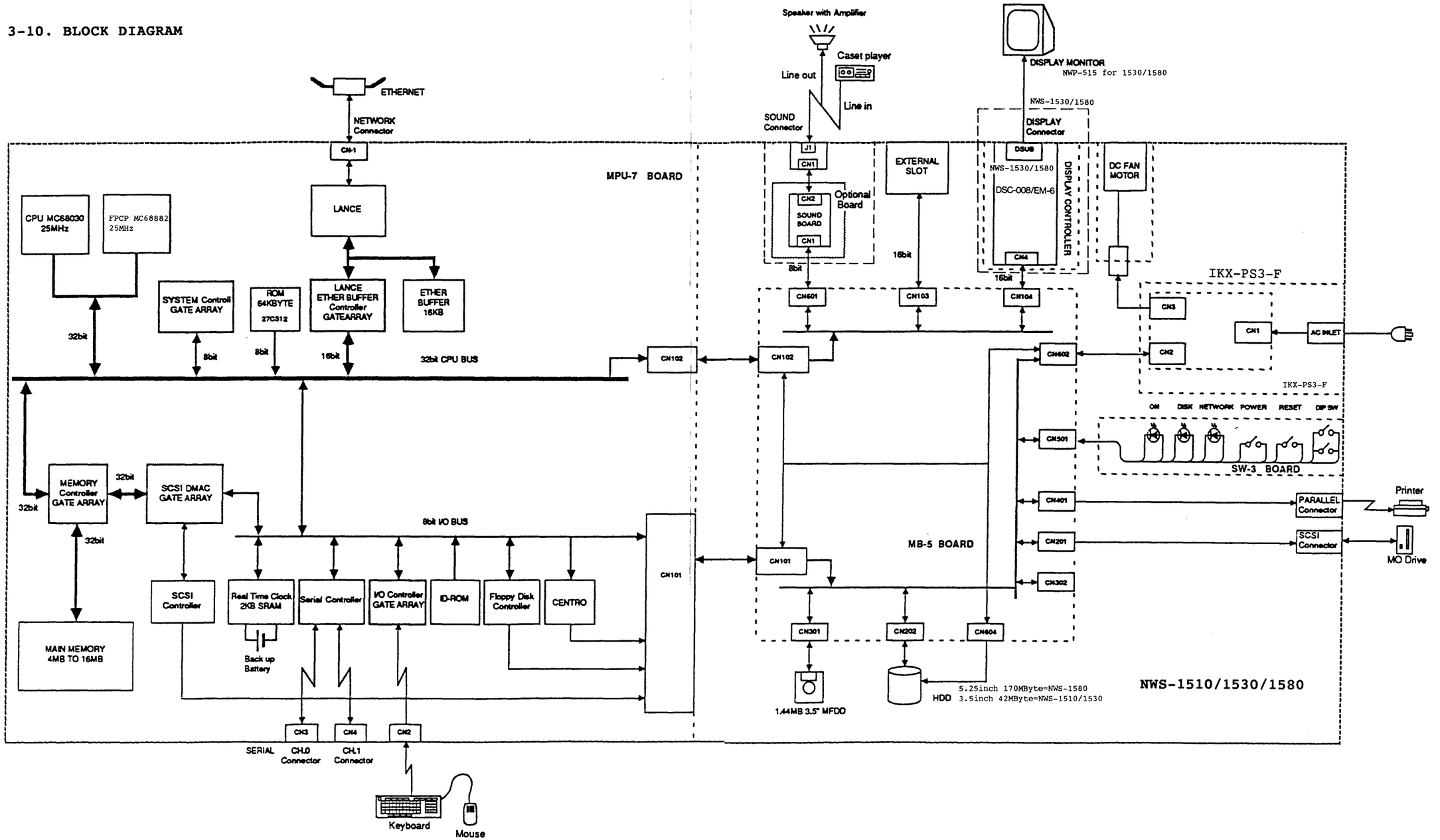


Fig.5 Memory timing chart (2／2)

3-10. BLOCK DIAGRAM



CHAPTER 4
SELF-DIAGNOSTICS

OVERVIEW

This document describes the procedure for entering the self diagnostic mode and the commands which are available in that mode. Examples displays are also presented.

4 – 1. Entering Self-diagnostics Mode

The system must be set as described in the steps to follow when performing self-diagnostics on the NWS-1510/1530/1580.

1) Use one of the two possible input/output device configurations given below when checking the NWS-1510/1530/1580.

a) Connect a terminal (NWP-511 or character terminal) to the serial port (CH.0).

b) Connect a color bitmap display (NWP-515) and a keyboard (NWP-410 or NWP-411) to the internal color bitmap board built into the NWS-1510/1530/1580.

2) Depending on the tests to be performed, one or more testers may need to be connected to the NETWORK, SERIAL, or PARALLEL ports. It may also be necessary to connect a color bitmap display (NWP-515) and a keyboard (NWP-410 or NWP-411) as described in 1-b above, as they are required for some of the self-diagnostics checks.

3) Open the front cover and set the dip switch corresponding to bit 6 to "on". The settings for the dip switches corresponding to the other bits depend on the input/output device configuration being used and are given below.

a) If a terminal has been connected to the serial port (CH.0), set all of the other dip switches to "off".

b) If connections have been made to the internal color bitmap board, set the dip switch corresponding to bit 2 to "on".

4) Insert the NWS-1510/1530/1580 self-diagnostics floppy disk into the self-diagnostics disk and executed when the NWS-1510/1530/1580 is turned on.

5) Turn on the NWS-1510/1530/1580.

The self -diagnostics program will be loaded from the self-diagnostics disk and executed when the NWS-1510/1530/1580 is turned on.

The following display will then appear on the display screen.

```
**** Diagnostic mode ****

loading fh(0,0)main
4620+3528+4
loading fh(0,0)kern
10360+3536+27840 start c0010000
start: main
```

*The display may differ slightly depending upon the model or version being used.

**Since none of the bitmap checks are performed automatically, be sure to watch the display and check that the images produced on it are correct.

When the main program starts, a menu (diagnostic check items) such as that shown below appear. The "diag>" prompt appears to indicate that the system is waiting for a command.

```
menu:
   0.  all       [-v][-c][-#][-Nx[,y,...] | x+X | Y+y]          : Check All
   1.  memory    [-v][-c][-#]                                   : Main Memory
   2.  eprom     [-v][-c][-#]                                   : EP-ROM
   3.  idrom     [-v][-c][-#]                                   : ID-ROM
   4.  timer     [-v][-c][-#]                                   : Timer intr
   5.  intr      [-v][-c][-#]                                   : Self interrupts
   6.  fpcp      [-v][-c][-#]                                   : FPCP
   7.  network   [-v][-c][-#][-ne]                              : Network
   8.  rtc       [-v][-c][-#][-fn]                              : RTC
   9.  scsi      [-v][-c][-#][-d#][-p][-nd]                     : SCSI/Hard Disk
  10.  bitmap    [-v][-c][-#][-s]                               : Bitmap board
  11.  parallel  [-v][-c][-#]                                   : Parallel port
  12.  serial    [-v][-c][-#][-ch#]                             : Serial ports
  13.  keyboard  [-v][-c][-#][-o][-us]                          : Keyboard
  14.  mouse     [-v][-c][-#]                                   : Mouse
  15.  led       [-v][-c][-#]                                   : LED lamps
  16.  dipsw     [-v][-c][-#]                                   : DIP Switch
  17.  floppy    [-v][-c][-#][-a][-dd][-hd][-f][-t#][-d#][-nws] : Floppy Disk
  18.  mon                                                      : ROM monitor
  19.  off                                                      : Power off
  20.  menu                                                     : Display menu
diag>
```

Detailed descriptions of the available commands are given in Section 3 (Page 4 – 6)

4 - 2. SELF DIAGNOSTIC PROCEDURE

4 - 2 - 1. Method of Inputting Commands and Additional General Items

To input commands, type either the number of the command as listed on the menu (first menu item) or the name of the command (second menu item) and press the return key.

For example, to perform a check of main memory (the items at the far right of the menu are the titles of the tests), you would input either "memory" or "1".

The items shown to the right of the command names are options. Added functions can be selected for commands by appending options. To add options to commands, simply type the appropriate option after the command as shown below.

"command -option"

The following options are common to all commands:

-v option

Specifying "-v" turns the verbose mode on. In this mode, a detailed description is displayed while each test is being run.

-c option

Specifying "-c" turns the continue mode on. In this mode, diagnostics continue even if an error is encountered along the way. When not in the continue mode, diagnostic execution is terminated if an error is encountered.

-# option

The -# option is set with a decimal number. It specifies how many times the command it is appended to should be repeated. If the -# option is not used, the command is executed only once.

If the command and option to be entered are identical to the one which was entered immediately before, "!!" can be entered instead. To append additional options to the previous command and options, the syntax "!! -option" may be used.

If the previous command was entered incorrectly, a modify function is available which enables you to change only the option portion. To use the modify function, enter the characters you wish to change preceded by a " ". Follow this with another " " and the correct character string.

For example, if the preceding command string was "abc -def" and you wish to change it to "zyz -def", you would enter " abc zyz". To modify the original string to "abc -dkf", you would enter " e k".

To halt execution of a command in mid course, either enter " C" (hold down the Ctrl key and press C) or the Del key (for the NWP-410 or NWP-411).

4 – 3. SELF DIAGNOSTICS

The following describes the displays produced for each item in the verbose mode and the content of each self diagnostic test. Where appropriate, the displays produced when the special options available for each item are appended are shown.

4 – 3 – 1. Main Memory Command

In the memory size test, the installed memory capacity is determined and displayed. All memory must be installed with successive addresses. Therefore, if there is a discrepancy between the memory size displayed and the amount of memory actually installed, there may be a problem with the order in which the memory was inserted.

In the data lines test, the data signal lines are checked. Data in which one bit is "1" and the remaining 31 bits "0" is written. It is then read back and checked against the original.

In the byte access test, first a 55(16) pattern is written in byte access, and a check is performed to determine if it can be read correctly. Next, an AA(16) pattern is written and read back as above as an additional check.

In the word access test, first a 5555(16) pattern is written in word access, and a check is performed to determine if it can be read correctly. Next, an AAAA(16) pattern is written and read back as above as an additional check.

In the long access test, first a 55555555(16) pattern is written in long access, and a check is performed to determine if it can be read correctly. Next, an AAAAAAAA(16) pattern is written and read back as above as an additional check.

In the addr lines test, first a FFFFFFFF(16) pattern is written to the entire memory area to be checked. It is then read back one byte at a time beginning from the lower addresses and checked to see if FF(16) was read correctly. If correct, 00(16) is written to that address. This allows any bad address lines to be found.

The dynamic bus sizing test checks whether the dynamic bus sizing function operates properly. It confirms whether the DSACK0, DSACK1, SIZ0, and SIZ1 signals work properly.

The burst mode operation test check to see whether the CPU can read data correctly from the internal cache in the burst mode.

```
diag> memory -v
MAIN MEMORY CHECK:
        Memory  size ..............................  4-MByte
        Data  lines  ..............................  OK
        Byte  access ..............................  OK
        Word  access ..............................  OK
        Long  access ..............................  OK
        Addr  lines  ..............................  OK
        Dynamic bus sizing ........................  OK
        Burst mode operation ......................  OK
diag>
```

4 – 3 – 2. EP-ROM Command

This test calculates the checksum for the EP-ROM and checks whether it is correct. This determines whether the contents of the EP-ROM are intact or not and confirms that there are no problems with the control signals or with the data and address buses from the CPU to the EP-ROM.

```
diag> eprom -v
EP-ROM CHECK ..................................... OK
diag>
```

4 – 3 – 3. ID-ROM Command

This test calculates the checksum for the P-ROM on the motherboard and checks whether it is correct. Then displays the data that is stored in P-RAM. It is then necessary to check whether this data is correct. ("Checksum" is the only error checking performed.)

```
diag> idrom -v
ID-ROM CHECK:
        Checksum ..................................... OK
        Model name          : NWS-1580
        Serial no           : 010001
        Lot                 : 1989-07
        Ethernet address : 08 00 46 00 01 15
diag>
```

4 – 3 – 4. Timer Intr Command

This test enables the 100Hz timer interrupt and uses an interrupt processing routine to count the number of interrupts generated in one second. The number of interrupts should be approximately 100. (A program loop is set up for one second.) If the number of interrupts generated per second is not approximately 100, possible causes include a problem with the interrupt circuit or the CPU clock may have erroneously set the program loop duration to a value other than one second.

```
diag> timer -v
TIMER CHECK:
        Timer interrupt check ..................... OK
                Interrupt count = 100 / 100
diag>
```

4 – 3 – 5. Self Interrupts Command

At level 2, the CPU issues an auto vector level 2 interrupt to itself.

AST refers to an interrupt auto vector level 1 which is issued when a special authorization command is executed with the CPU in user status. The AST interrupt is issued when a special authorization command is executed from a user program.

For both types of interrupt, a "TIME OUT" error is generated if no interrupt is generated within a fixed period of time.

```
diag> intr -v
SELF INTERRUPTS CHECK:
        Level 2 ..................................... OK
        AST ......................................... OK
diag>
```

4 – 3 – 6. FPCP Command

The FPCP (floating-point coprocessor) test performs floating-point calculations of the four basic arithmetic functions and checks whether the results are correct. Lastly, it determines and displays the coprocessor type (MC68882)

```
diag> fpcp -v
FLOATING-POINT COPROCESSOR CHECK:
        Calculation ................................. OK
        Coprocessor type ............................ MC68882
diag>
```

4 – 3 – 7. Network Command

To perform the network check, it is necessary to connect a test jig (ethernet transceiver) to the NETWORK port on the rear panel.

The buffer memory check determines whether read/write operations with the buffer memory used for sending and receiving network signals can be performed correctly.

The methods used by the data line, byte access, word access, long access and address line checks are identical to those described in the "Main Memory command" section.

The LANCE (Am7990) initialize check initializes the LANCE (Am7990) and confirms that an initialization complete interrupt is generated.

The internal loopback check sends data over the network via the ethernet transceiver and determines tests whether the same data can then be received correctly.

In the CRC logic check, data to which a CRC calculated in software has been appended is sent and, after it is received again, a CRC is again calculated in software. The two CRCs should agree. Next, data to which a CRC calculated in hardware has been appended is sent. The CRC is then calculated in software after the data has been received again and the two CRCs compared to see if they agree.

The collision and retry logic check sets the flag which indicates a LANCE collision and determines whether a reset is properly triggered.

Description of options:

-ne: no external option

This option is used to disable all checks performed via the ethernet transceiver.

If this option is specified, the "external loopback" and "collision and reentry logic" checks are not performed. It sound be used in cases where the Network command is used with no ethernet transceiver connected.

```
diag> network -v
NETWORK CHECK:
        Buffer memory check:
                Data line ..... OK
                Byte access ..... OK
                Word access ..... OK
                Long access ..... OK
                Address line ..... OK
        LANCE(Am7990) initialize ..... OK
        Internal loopback ..... OK
        External loopback ..... OK
        CRC logic ..... OK
        Collision and retry logic ..... OK
diag> !! -ne
network -v -ne
NETWORK CHECK:
        Buffer memory check:
                Data line ..... OK
                Byte access ..... OK
                Word access ..... OK
                Long access ..... OK
                Address line ..... OK
        LANCE(Am7990) initialize ..... OK
        Internal loopback ..... OK
        CRC logic ..... OK
diag>
```

4 – 3 – 8 RTC Command

This is a check of the RTC (Real Time Clock).

The RTC battery test checks the condition of the battery used to back up the RTC.

The static RAM test checks whether the static memory built into the RTC can be written to and read from properly.

In the starting the oscillator test, the oscillator built into the RTC is started from a stopped state. (This test is performed only once even if the -# option has been specified.)

The leap year check tests whether the calendar advances properly from February 28 to 29 on leap years.

The new month check confirms that the calendar advances properly to the next month after the end of the previous one has been reached normally.

The new year check confirms that the calendar advances properly to the next year on January 1st.

In the stopping the oscillator test, the oscillator built into the RTC is halted from an oscillating state. This prevents unnecessary drain on the battery. (This test is performed only once even if the -# option has been specified.)

Description of options:

-fn: function option

This is a service which allows specific RTC settings to be made individually. When the RTC command is executed with this option appended, the "RTC function>" prompt is displayed and the system waits for a command. The following commands and functions are available:

"1" or "start": start the built-in oscillator.

"2" or "stop": stop the built-in oscillator.

"3" or "set": set the calendar (year, month, day).

"4" or "read": read the current calendar setting.

"0" or "exit": terminate the RTC command.

```
diag> rtc -v
REAL TIME CLOCK CHECK:
        RTC Battery ..............................  OK
        Static RAM ...............................  OK
        Starting the Oscillator ..................  done
                set time->              1992/02/28 FRI 23:59:59
                Read after 1sec->       1992/02/29 SAT 00:00:00
        Leap Year Check ..........................  OK
                set time->              1989/02/28 TUE 23:59:59
                Read after 1sec->       1989/03/01 WED 00:00:00
        New Month Check ..........................  OK
                set time->              1988/12/31 SAT 23:59:59
                Read after 1sec->       1989/01/01 SUN 00:00:00
        New Year Check ...........................  OK
        Stopping the Oscillator ..................  done
diag> ^-v^-fn
rtc -fn
REAL TIME CLOCK function service
        1.  start    the Oscillator
        2.  stop     the Oscillator
        3.  set      the Clock
        4.  read     the Clock
        0.  exit     this function
RTC function> read
Read the Clock ..................  1989/01/01/SUN 00:00:01
RTC function> 0
diag>
```

4 – 3 – 9. SCSI/Hard Disk Command

This command checks the SCSI bus and the hard disk.

The open channel test checks whether the hard disk drive controller is operating properly and displays the drive's vendor ID, model number and revision level. (The test cannot detect errors in the vendor ID, model number or revision level reported.)

The buffer size inquiry check determines and displays the size of the hard disk drive controller's buffer memory.

The data write test checks whether the hard disk drive controller's buffer memory can be written to correctly.

The data write test checks whether the hard disk drive controller's buffer memory can be read from correctly.

The data verify test checks write data to the hard disk drive controller's buffer memory, then reads it back and tests for accuracy.

The DISK read first 1 block test checks whether the data recorded on the hard disk can be read correctly.

Description of options:

-d#: drive number option (#= 0, 1, 2, 3, 4, 5, 6, 7)

By specifying this option, the desired SCSI channel (drive number) can be checked.

Use this command to specify the appropriate drive number in order to check an external hard disk drive. If the -d# option is not used, the default drive number is "0" (the internal drive).

Example: -d1 (drive number "1")

– p: programmed I/O option

When this option is selected, all data I/O takes place in the programmed I/O mode. If the option is not used, all SCSI bus data I/O is carried out in the DMAC mode. Therefore, if the SCSI/Hard Disk command can be run successfully with the -p option but generates an error without it, tne DMAC should be suspected.

-nd: no disk option

This option allows checking of the system unit SCSI controller only. It is used if no hard disk drive is present or if the open channel test was terminated with an error. If there are no errors when this option is specified, but errors are generated when no options or the -p option is used, either the SCSI controller or the hard disk drive may be bad.

```
diag> scsi -v
SCSI/HARD DISK CHECK:
        Open Channel ..............................  OK
                Vender  ID  : CDC              (*)
                Model name  : WREN5-Half Heifht (*)
                Rev. level  : 5457             (*)
        Buffer size inquiry .......................  OK
                Buffer size : 32768 bytes       (*)
        Data write ................................  OK
        Data read .................................  OK
        Data verify ...............................  OK
        DISK read first 1 block ...................  OK
diag> !! -nd
scsi -v -nd
SCSI CHECK:
        Initialize CXD-1180 .......................  OK
        Bus control for Initiator .................  OK
        Bus control for Target ....................  OK
        Interrupt .................................  OK
diag>
```

* Differs depending on model and version number.

4 – 3 – 10. Bitmap board command

Used to check the internal color bitmap board.(**)
Used to test the memory read/write functions of the board.
Used during raster operation to determine if the effects of raster operation are correct.
Used during vector operation to determine if the effects of vector operation are correct.
During vector operation, the following patterns should appear on the color display in the following order.

a) Vertical stripes (Fig.1)

Vertical stripes are displayed using every other pixel in the horzontal rows.

b) Vertical stripes (Fig.2)

The previous display is completely overwritten with a white screen, then vertical stripes are again displayed using every other pixel in the horizontal rows.

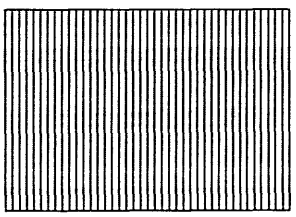


Fig.1

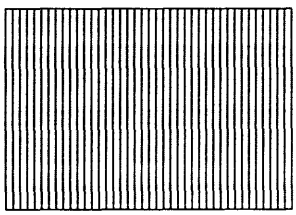


Fig.2

c) Write pattern(Fig.3)

A □□□□□□□□ pattern is repeated in the horizontal direction.

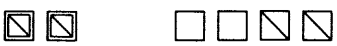


Fig.3

d) Bitbit test (Fig.4)

Kanji patterns are written over pattern c), and the mixed result is displayed.

e) Bitbit test (Fig.5)

Geometrical patterns are written over pattern d), and the mixed result is displayed.

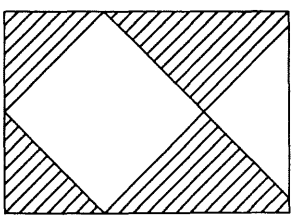


Fig.4

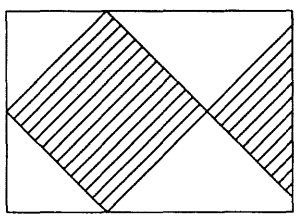


Fig.5

▨ indicates the newly written portion.

** The bitmap checks are all automatic. The user is only required to confirm whether the patterns are correctly displayed or not.

f) Flash pattern (Fig.6)

A pattern of lines radiating out from a point is displayed in the left portion of the screen.

g) Crosshatch 8 × 6 (Fig.7)

A crosshatch pattern of white lines dividing the screen into 8 sections horizontally and 6 sections vertically is displayed.

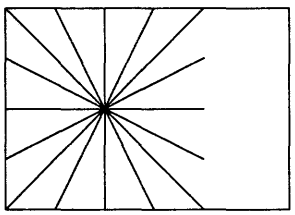


Fig.6

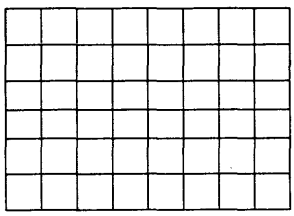


Fig.7

h) Crosshatch 8 × 6

The reverse of pattern g) is displayed.

i) Color bars (Fig.9)

The screen is divided into 8 sections horizontally and 2 sections vertically. Bars appear in the top half in the following colors, from left to right: white, yellow, cyan, green, purple, red, magenta, black. A black bar appears in the far bottom left, followed by successively lighter shades of gray and a white bar on the far right.

j) Color-bar gradations (Fig.10)

The following colors gradations appear in the following colors, from left to right: red, green, yellow, blue, purple, cyan. The black bar appears in the far bottom left, followed by 64 shades of gray and one white bar in the far right.

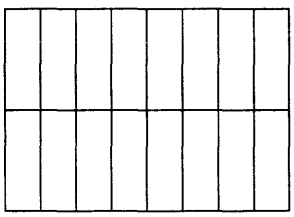


Fig.9

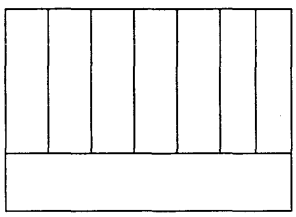


Fig.10

k) Red gradations (Fig.11)

Red gradations are displayed beginning with black followed by successively lighter shades of red to the right.

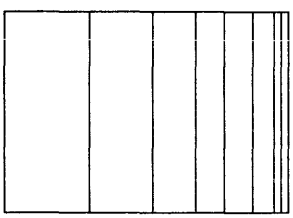


Fig.11

l)Green gradations
Analogous to red gradations.
m)Yelloww gradations
Analogous to red gradations.
n)Blue gradations
Analogous to red gradations.
o)Purple gradations
Analogous to red gradations.
p)Cyan gradations
Analogous to red gradations.
q)White gradations
Analogous to red gradations.

Raster operation interrupt is used to make sure an interrupt is generated properly after raster operation is completed.
The raster operation interrupt count is used to keep track of the number of interrupts generated during two raster operations.
V-sync interrupt is used to make sure a vertical synchronization interrupt is generated properly.
The V-sync interrupt count is used to keep track of the number of V-sync interrupts generated during one second (created using a program loop). It checks whether the number of interrupts is 60 (approximately) as it should be.

Discription of options
-s: step option
Whenever the image on the screen changes, the program waits for key input while preserving the current status. Press any key to continue (except for "^C" or the "Del" key, either of which will abort the check).

```
diag> bitmap -v
BITMAP BOARD CHECK:
        Memory ..................................... OK
        Rster operation ............................ OK
        Vector operation ........................... OK
        Raster operation interrupt ................. OK
        Raster operation interrupt count ........... OK
                Interrupt count = 2 / 2
        V-sync interrupt ........................... OK
        V-sync interrupt count ..................... OK
                Interrupt count = 60 / 60
diag>
```

Note) All messages are displayed together after the bitmap board display check is completed.

4 – 3 – 11, Parallel Port Command

To use this command, a printer with a standard Centronics interface must be connected to the PARALLEL port on the rear panel. A Centronics test jig may also be used in place of a printer (see appendix).

Once a printer has been connected, first polling is used to detect the BUSY signal, and all available characters are then printed. Next, the BUSY signal is detected using an interrupt and, again, a full set of characters is printed.

If a Centronics test jig is connected, one of the data signal lines is set to "ON", the signal content is looped back to the BUSY signal and a read check is performed. The STB signal is used to choose which of the eight data lines should be set to "ON". This means all data lines can be tested. Finally, the test determines if an interrupt was properly generated.

```
diag> parallel -v
Set PRINTER or TEST PROBE to the PARALLEL PORT and hit <RETURN> key
PARALLEL PORT CHECK:
        Write data by Polling ..... OK
        Write data by Interrupt ..... OK
diag>
```

Printer connected

```
diag> parallel -v
Set PRINTER or TEST PROBE to the PARALLEL PORT and hit <RETURN> key
PARALLEL PORT CHECK:
        Data lines all Low ..... OK
        Data lines ..... OK
        Interrupt ..... OK
diag>
```

Centronics test jig connected

4 – 3 – 12. Serial Ports Command

In order to test the serial ports, a test jig must be connected to the port(s) to be tested (see appendix).

Increment data patterns from 0 to 255 are sent from TxD to serial ports CH.1 and CH.0. They pass through the jig and are received at Rxd. The sent and received data are then compared for accuracy. An ON/OFF signal is sent from DTR. It passes through the jig and is received at DCD/DSR. Then the sent and received data are compared for accuracy. The RTS-CTS/RI interface is tested in like manner.

All tests are performed at 9600 baud. The baud rate of ports other than those connected to the terminal cannot be cnecked using this command.

Description of options:

-ch#: cnannel number option

Tnis option is used to test a 4-channel serial interface board (NWB-231A) which is being utilized as a serial port. The # is replaced by the NWB-231A port number. To test a second NWB-231A, 4 should be added to the port number indicated by #.

Example: -ch0 (CH.0 of NWB-231A number 1), -ch7 (CH.3 of NWB-231A number 1)

```
diag> serial -v
SERIAL PORTS CHECK:
        Set TEST PROBE to the SERIAL PORT CH.1 and hit <RETURN> key
        SERIAL PORT CH.1:
                Controller open ..................... OK
                Characters loopback ................. OK
                DTR->DCD/DSR loopback 0 ............. OK
                DTR->DCD/DSR loopback 1 ............. OK
                RTS->CTS/RI  loopback 0 ............. OK
                RTS->CTS/RI  loopback 1 ............. OK
        Exchange TERMINAL from CH.0 to CH.1 and hit <RETURN> key (*)
        Set TEST PROBE to the SERIAL PORT CH.0 and hit <RETURN> key
        SERIAL PORT CH.0:
                Controller open ..................... OK
                Characters loopback ................. OK
                DTR->DCD/DSR loopback 0 ............. OK
                DTR->DCD/DSR loopback 1 ............. OK
                RTS->CTS/RI  loopback 0 ............. OK
                RTS->CTS/RI  loopback 1 ............. OK
diag> !! -ch0
serial -v -ch0
SERIAL PORTS CHECK:
        Set TEST PROBE to the OPTIONAL SERIAL PORT CH.0 and hit <RETURN> key
        OPTINAL SERIAL PORT CH.0:
                Controller open ..................... OK
                Characters loopback ................. OK
                DTR->DCD/DSR loopback 0 ............. OK
                DTR->DCD/DSR loopback 1 ............. OK
                RTS->CTS/RI  loopback 0 ............. OK
                RTS->CTS/RI  loopback 1 ............. OK
diag>
```

---

* Note: I/O cannot be performed with I/O devices if a serial port other than CH.0 is used.

4 – 3 – 13. Keyboard Command

This command cnecks tne operation of all the keys on the NWP-411 or NWP-410 keyboard, the beep function and interrupts. A keyboard must be connected to the KEYBOARD PORT in order to run this test.

In the keyboard check, a diagram showing the layout of the keyboard is displayed on the screen and the system waits for the user to press a key. When a key is pressed and released, tne corresponding place on the screen diagram changes to reverse. The proper operation of all the keys is confirmed when all are displayed in reverse on the screen. In order to test the keyboard port, press the <RETURN> key two times in succession after hitting a few keys at random to continue with tne next step.

In tne beep function check, tne user presses any key and confirms that a beep issued from tne keyboard. (Each time a key is pressed, a beep is generated by switching between write access and read access.) To continue with tne next step, press <RETURN>.

If a malfunction is detected, tne keyboard itself and tne keyboard serial port can be suspected.

Description of options:

-o: oyayubi option

This option is used when an index finger (Japanese: oyayubi) shift keyboard (NWP-410) is connected. This check does not test for simultaneous keystrokes.

-us: us option

This option is used when a U.S. keyboard (NWP-411) is connected.

When neither of the above options is used, the default is a standard keyboard (NWP-411).

```
diag> keyboard -v
(The screen is cleared.)
KEYBOARD CHECK:

        Push all keys   (for Exit, hit <RETURN> key 2 times)


        @@@@ @@@@ @@@@ @@@@ @@@@   @@@@ @@@@ @@@@ @@@@ @@@@
@@@@[1] [2] [3] [4] [5] [6] [7] [8] [9] [0] [-] [=] [\] @@@@  [7] [8] [9] [-]
@@@@ [Q] [W] [E] [R] [T] [Y] [U] [I] [O] [P] [[] []] @@@ @@@  [4] [5] [6] [+]
@@@@@ [A] [S] [D] [F] [G] [H] [J] [K] [L] [;] ['] ['] @@@@@@  [1] [2] [3] [,]
@@@@@@@ [Z] [X] [C] [V] [B] [N] [M] [,] [.] [/] [ ] @@@@@@@@  [0] @@@ [.] @@@
@@@@@ @@@ @@@@@ @@@@@@@@@@@@@@@@@@@@@@@@ @@@@@ @@@ @@@ @@@@@@  @@@ @@@ @@@ @@@


        Push any key to beep  (at End, hit <RETURN> key)


        Push any key to interrupt

                Interrupt check ..... OK

diag>
```

Note: The layout displayed when the -o option is selected differs from that shown above.

4 – 3 – 14. Mouse Command

This command checks the operation of the mouse supplied with the keyboard.

In the mouse button check, a picture of the mouse appears on the screen. When the three mouse buttons are pressed in sequence, the corresponding places on the screen switch to reverse display. The mouse buttons are operating properly if all three buttons on the screen switch to reverse.

In the mouse move check, X and Y axes as well as a mouse cursor are displayed on the screen. If the mouse cursor

moves about the screen in correspondence with the movements of the mouse when the user moves it up and down and to the left and right, the X and Y position data is correct.

Finally, the test checks for the interrupt from the mouse. An interrupt should be generated when one of the mouse buttons is pressed or the mouse is moved.

If the mouse does not perform correctly in this test, either the mouse itself, the keyboard mouse circuit or the mouse serial port is probably bad.

```
diag> mouse -v
(The screen is cleared.)
MOUSE CHECK:

       Push all mouse buttons  (for Exit, hit <Del> key)

                                    |
                              ------|------
                              |           |
                              |  0  0  0  |
                              |  0  0  0  |
                              |           |
                              |           |
                              |           |
                              -------------
```

When the mouse button test is completed, the screen is redrawn for the mouse cursor test.

```
(The screen is redrawn.)
MOUSE CHECK:

        Move mouse cursor  (for Exit, Push any mouse button)

                                        |
                                        |
                                        |
                                        |
                                        |
                                        |
                                        |
                                        |
                                        |
    ------------------------------------+------------------------------------
                                        |
                                        |
                                        |
                                        |
                                        |
                                        |
                                        |
                                        |
                                        |
                                        |

        Move mouse or push any mouse button to interrupt

                Interrupt check ..................... OK

diag>
```

4 − 3 − 15. Led Lamps Command

This command test lights the two LEDs on the main board. The operator must confirm visually whether they light properly.

First the green LED is tested. It lights when the <RETURN> key is pressed. Next, the yellow LED is tested in the same way.

```
diag> led -v
LED LAMPS CHECK:
        GREEN LED LAMP ON :hit <RETURN> key
        YELLOW LED LAMP ON :hit <RETURN> key
        Hit <RETURN> key to NEXT
diag>
```

4 – 3 – 16. Dip Switch Command

This command tests whether the DIP switch settings can be read properly by asking the operator to set them in specified ways.

If the -# option is used with a value of 2 or above, the DIP switch status is displayed each time a switch is turned ON or OFF.

```
diag> dipsw -v
DIP-SWITCH CHECK [ 1 = ON / 0 = OFF / X = DON'T CARE ]:
        Set  DIP-SWITCH = 111111XX      and hit <RETURN> key ... OK
        Set  DIP-SWITCH = 011111XX      and hit <RETURN> key ... OK
        Set  DIP-SWITCH = 001111XX      and hit <RETURN> key ... OK
        Set  DIP-SWITCH = 000111XX      and hit <RETURN> key ... OK
        Set  DIP-SWITCH = 000011XX      and hit <RETURN> key ... OK
        Set  DIP-SWITCH = 000001XX      and hit <RETURN> key ... OK
        Set  DIP-SWITCH = 000000XX      and hit <RETURN> key ... OK
Set DIP SWITCH as before [ 000001XX ] and hit <RETURN> key (*)
diag> !! -3
dipsw -v -3
DIP-SWITCH CHECK [ 1 = ON / 0 = OFF / X = DON'T CARE ]:
        Read DIP-SWITCH = 100001XX (**)
        Read DIP-SWITCH = 101001XX (**)
        Read DIP-SWITCH = 101011XX (**)
Set DIP SWITCH as before [ 000001XX ] and hit <RETURN> key (*)
diag>
```

Notes:

* Set DIP switches as they were before the check.

** A DIP switch was turned ON or OFF. (The display differs depending on the current status.)

4 – 3 – 17. Floppy Disk Command

This command is used to test the floppy disk drive. Two formatted diskettes, one 2DD and one 2HD are required. Neither disk should be write-protected. To format the floppy disks, either use the method described among the options below or use the OS format command.

The write protect test enables the operator to test whether the self-diagnostic floppy diskette is properly write-protected or not.

Next, the drive's ability to write to the (formatted) 2DD diskette is tested. (100 random sectors are written to.)

Finally, the drive's ability to write to the (formatted) 2HD diskette is tested. (100 random sectors are written to.)

Insert and change floppies as instructed by the messages.

Description of options:

-a: all sector option

Instead of writing or reading 100 random sectors, all sectors on the disk are written or read.

-dd: 2dd option

Perform 2DD floppy disk check only.

-hd: 2hd option

Perform 2HD floppy disk check only.

-f: format option

Specify to format a floppy disk. This option is ignored if it is not accompanied by the -dd or -hd option.

Example: -f -dd (formats a 2DD floppy disk)

Example: -f -hd (formats a 2HD floppy disk)

-t#: retry count option

Specifies the number to retries to be attempted in case of an error. The default is 10 times.

Example: -t3 (retry three times)

-d#: drive number option (# = 1, 2, 3, 4)

The default if this option is not specified is drive number "1" (the internal 3.5" drive). To test an exter-

nal floppy disk drive, use this option to specify the appropriate drive number (2, 3 or 4). Drive numbers 2, 3, and 4 are treated as 5.25" MS-DOS format drives.

Example: -d3 (drive number "3")

-nws: news format option

Drive numbers 2, 3, and 4 are normally treated as 5.25" MS-DOS format drives, but this option can be added to the drive option to specify the drive as 3.5" NEWS format.

Example: -d2 -nws (drive number "2" is a 3.5" NEWS format drive)

```
diag> floppy -v
FLOPPY DISK CHECK:
        Write protect ..... OK
        Set 2DD Floppydisk and hit <RETURN> key
                Write some data ..... OK
                Verify the data ..... OK
        Set 2HD Floppydisk and hit <RETURN> key
                Write some data ..... OK
                Verify the data ..... OK
        Set DIAG Floppydisk and hit <RETURN> key
diag> !! -f -hd
floppy -v -f -hd
FLOPPY DISK CHECK:
        Set 2HD Floppydisk for format and hit <RETURN> key
                Format the disk ..... OK
                Verify the disk ..... OK
diag>
```

4 – 3 – 18. ROM Moniter Command

Switches to from the self-diagnostic mode to the ROM monitor mode.

```
diag> mon
EXIT Diagnostic mode
```

4 – 3 – 19. Power Off Command

Powers down the system unit. You are asked for confirmation "(y/n)?". Type "y" to switch off power to the system.

```
diag> off
Power off OK (y/n) ? y
```

4 – 3 – 20. Display Menu Command

Displays a menu of the commands available in the self-diagnostic program. The menu is identical to that which appears when the program first starts.

4 – 3 – 21. Check All Command

Executes all commands from 3-1 to 3-17 in that order.

All options other than -# are automatically passed to the appropriate commands. Only applicable options take effect.

Description of options:

-#: times option

When this option (# is a value of 2 or above) is appended to the Check All command, all commands from 3-1 to 3-17 are executed the specified number of times. If the -# option is not used, each command is executed once.

-N: execute number option

If the option "-N" is issued followed by a list of command numbers (as listed on the command menu), only the

listed commands (separated by commas) are executed in the order specified, from left to right. If the comma delimiter is replaced by a "+", the intervening command number are executed.

Example: -N2,3,5,7,9 (Commands 2, 3, 5, 7, and 9 are executed)

Example: -N2+4,7+9,17 (Commands 2, 3, 4, 7, 8, 9, and 17 are executed)

Note: Command numbers 0, 18, 19, and 20 cannot be executed using the -N option.

Appendix A: Serial Port Test Jig

This appendix describes the test jig which must be connected to the serial port (CH.0/CH.1) of the network station NEWS for performing self diagnostics on the serial circuit and the testi jig which is connected to the 4-channel interface board (optional serial port) for a similar purpose.

1) Serial board pin assignments

System unit serial port (CH.0/CH.1)

Pin No.	Signal	I/O direction	Pin No.	Signal	I/O direction
1	-		14	-	
2	TxD	-->	15	TRxC	
3	RxD	<--	16	-	
4	RTS	-->	17	RTxC	
5	CTS	<--	18	-	
6	DSR	-->	19	-	
7	GND		20	DTR	<--
8	DCD	<--	21	-	
9	-		22	RI	-->
10	-		23	-	
11	-		24	-	
12	-		25	-	
13	-				

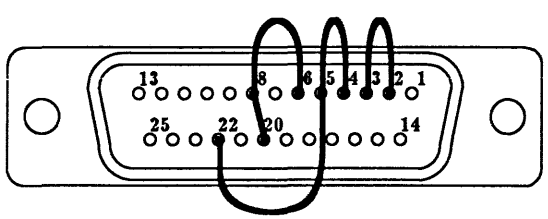
Optional serial port (CH.0-CH.3)

Pin No.	Signal	I/O direction	Pin No.	Signal	I/O direction
1	DCD	<--	6	DSR	-->
2	RxD	<--	7	RTS	-->
3	TxD	-->	8	CTS	<--
4	DTR	<--	9	RI	<--
5	GND				

-->: Output signal

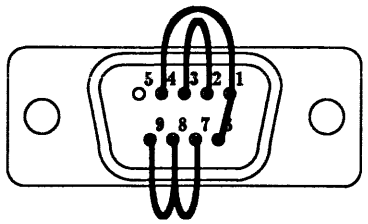
<--: Input signal

2) Serial port test jig wiring



System unit serial port

(CH.0/CH.1)



Optional serial port

(CH.0-CH.3)

A (male) D-SUB socket is used for the jig connector.

Appendix B: Parallel Port Test Jig

This appendix describes the test jig which must be connected to the parallel port for performing self diagnostics on the serial circuit.

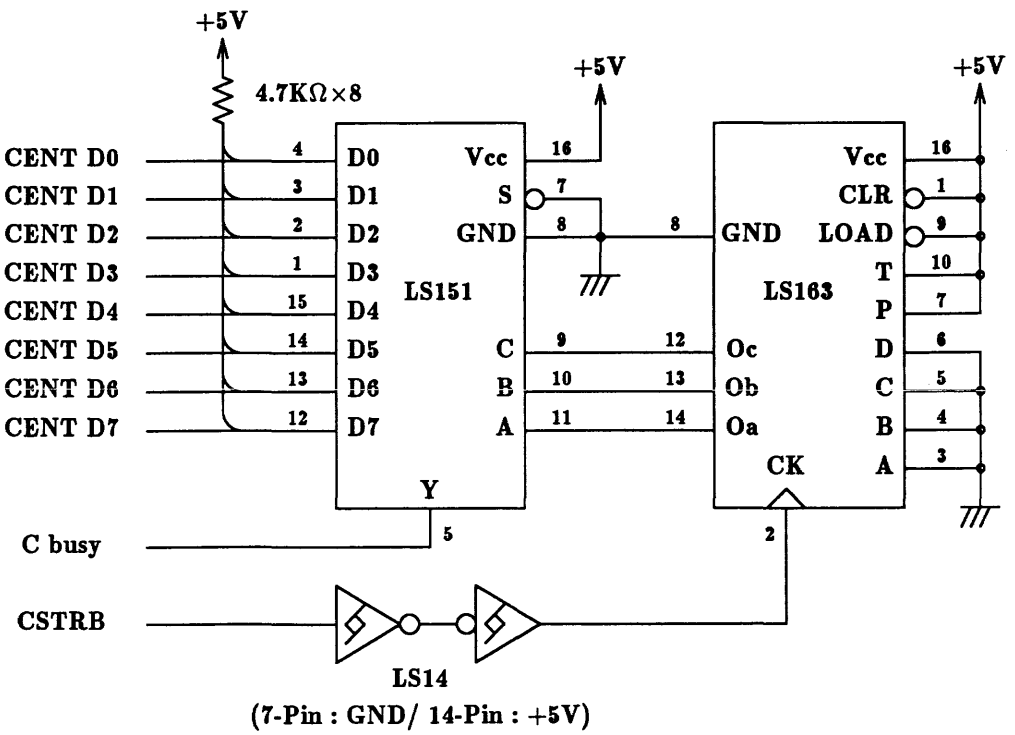
1) Parallel board pin assignments

Pin No.	Signal	I/O direction	Pin No.	Signal	I/O direction
1	CSTRB	-->	8	CENT D6	-->
2	CENT D0	-->	9	CENT D7	-->
3	CENT D1	-->	10	-	
4	CENT D2	-->	11	C busy	<--
5	CENT D3	-->	12	-	
6	CENT D4	-->	13	C fault	<--
7	CENT D5	-->	14	GND	

-->: Output signal

<--: Input signal

2) Parallel port test jig wiring

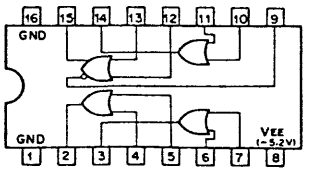


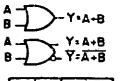
CHAPTER 5
DIAGRAMS

5-1. Semiconductor Index

NWS-1510/1530/1580 EK

MC10H103L (MOTOROLA)
ECL 2-INPUT OR GATE
— TOP VIEW —

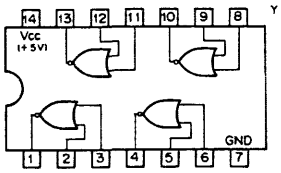


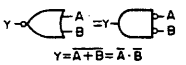


A	B	Y	$\overline{Y}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

0;LOW LEVEL
1;HIGH LEVEL

74F02PC(FSC)
MC74F02N (MOTOROLA)
TTL 2-INPUT POSITIVE-NOR GATE
— TOP VIEW —

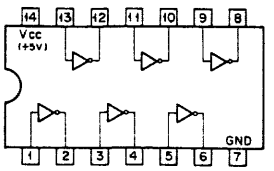


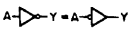


A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

0;LOW LEVEL
1;HIGH LEVEL

MC74F04N (MOTOROLA)
TTL INVERTER
— TOP VIEW —

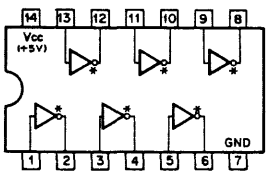




A	Y
0	1
1	0

0;LOW LEVEL
1;HIGH LEVEL

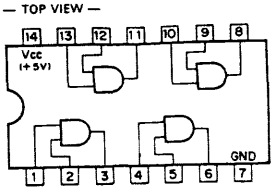
SN74S05N (TI)
TTL INVERTER WITH OPEN-COLLECTOR
— TOP VIEW —

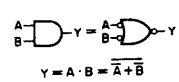


A	Y
0	1
1	0

0;LOW LEVEL
1;HIGH LEVEL
*;OPEN COLLECTOR

SN74LS08N (TI)
MC74F08N (MOTOROLA)
TTL 2-INPUT POSITIVE-AND GATE
— TOP VIEW —

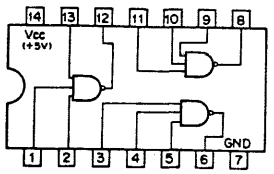


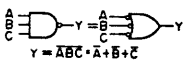


A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

0;LOW LEVEL
1;HIGH LEVEL

MC74F10N (MOTOROLA)
TTL 3-INPUT POSITIVE NAND GATE
— TOP VIEW —

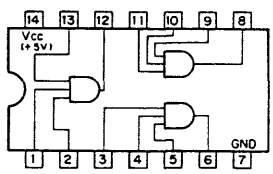


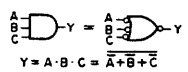


A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

0 : LOW LEVEL
1 : HIGH LEVEL

MC74F11N (MOTOROLA)
TTL 3-INPUT POSITIVE-AND GATE
— TOP VIEW —

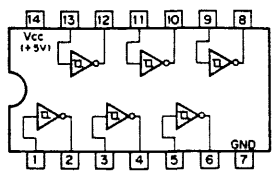


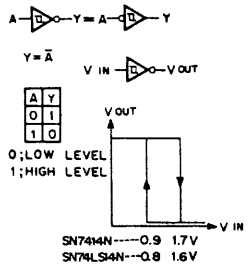


A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

0;LOW LEVEL
1;HIGH LEVEL

SN74LS14N (TI)
TTL SCHMITT TRIGGER INVERTER
— TOP VIEW —

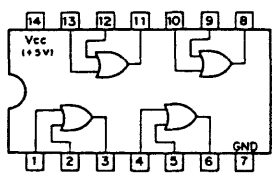


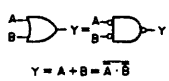


A	Y
0	1
1	0

0;LOW LEVEL
1;HIGH LEVEL

MC74F32N (MOTOROLA)
TTL 2-INPUT POSITIVE-OR GATE
— TOP VIEW —

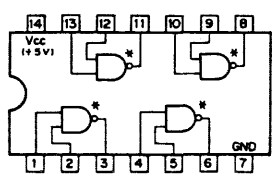


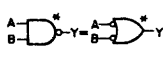


A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

0;LOW LEVEL
1;HIGH LEVEL

SN74S38N (TI)
TTL 2-INPUT POSITIVE-NAND GATE BUFFER
WITH OPEN-COLLECTOR
— TOP VIEW —





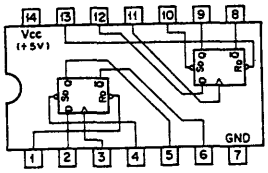
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

0 ; LOW LEVEL
1 ; HIGH LEVEL
*; OPEN COLLECTOR

MC74F74N (MOTOROLA)

TTL D-TYPE FLIP FLOP WITH DIRECT SET/RESET

— TOP VIEW —



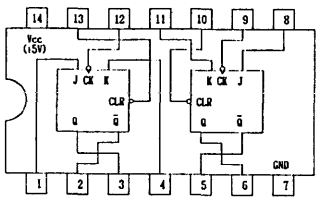
INPUTS				OUTPUTS	
$\overline{S_D}$	$\overline{R_D}$	CK	D	Qn+1	$\overline{Q_{n+1}}$
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	1*	1*
1	1	↑	1	1	0
1	1	↑	0	0	1
1	1	0	X	Qn	$\overline{Q_n}$

0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE
1* ; NONSTABLE

SN74LS107AN (TI)

DUAL J-K FLIP-FLOPS WITH CLEAR

— TOP VIEW —



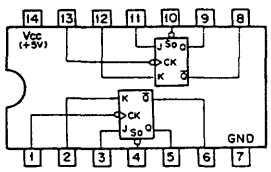
INPUT				OUTPUT	
CLR	CK	J	K	Q	$\overline{Q}$
0	×	×	×	0	1
1	↓	0	0	Q_0	$\overline{Q_0}$
1	↓	1	0	1	0
1	↓	0	1	0	1
1	↓	1	1	TOGGLE	
1	1	×	×	Q_0	$\overline{Q_0}$

0 ; LOW LEVEL
1 ; HIGH LEVEL
× ; DON'T CARE

74F113PC (FSC)

TTL J-K FLIP FLOP WITH DIRECT SET

— TOP VIEW —



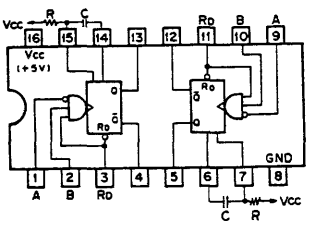
INPUTS				OUTPUTS	
$\overline{S_D}$	CK	J	K	Qn+1	$\overline{Q_{n+1}}$
0	X	X	X	1	0
1	↓	0	0	Qn	$\overline{Q_n}$
1	↓	0	1	0	1
1	↓	1	0	1	0
1	↓	1	1	$\overline{Q_n}$	Qn
1	1	X	X	Qn	$\overline{Q_n}$

0 ; LOW LEVEL X ; DON'T CARE
1 ; HIGH LEVEL

SN74LS123N (TI)

TTL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH DIRECT RESET

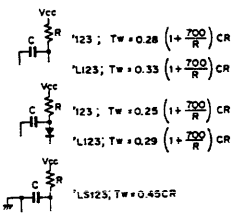
— TOP VIEW —



INPUTS			OUTPUTS	
$\overline{R_D}$	A	B	Q	$\overline{Q}$
0	X	X	0	1
X	1	X	0	1
X	X	0	0	1
1	0	↑	⊓	⊓
1	↓	↑	⊓	⊓
↑	0	↑	⊓	⊓

0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE

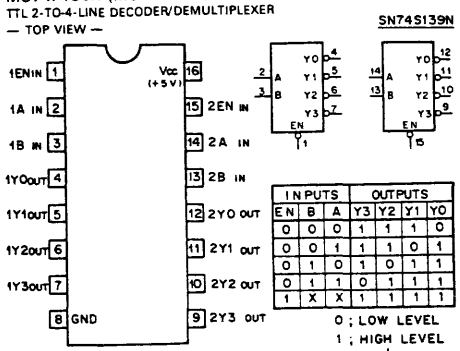
OUTPUT PULSE WIDTH



MC74F139N (MOTOROLA)

TTL 2-TO-4-LINE DECODER/DEMULTIPLEXER

— TOP VIEW —



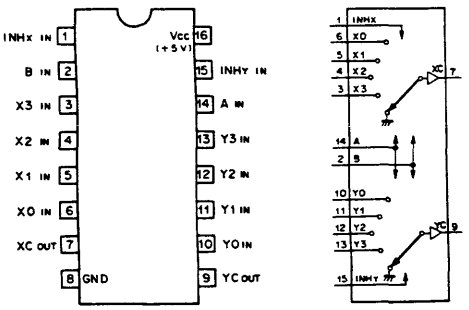
INPUTS			OUTPUTS			
EN	B	A	Y3	Y2	Y1	Y0
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1
1	X	X	1	1	1	1

0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE

MC74F153N (TI)

TTL 4-LINE-TO-1-LINE DATA SELECTOR/MULTIPLEXER

— TOP VIEW —



CONTROL IN			ON CHANNEL
INH	B	A	
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	X	X	GND

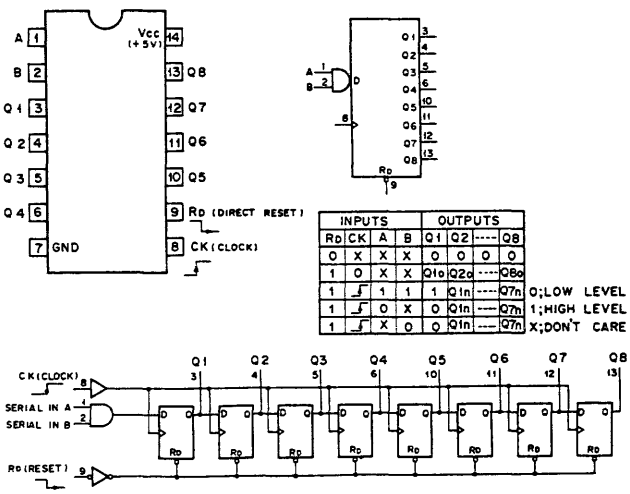
0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE

74F164PC(FSC)

74F164PC (FSC)

TTL 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER

— TOP VIEW —

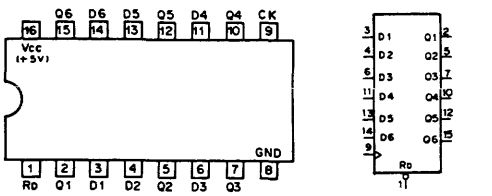


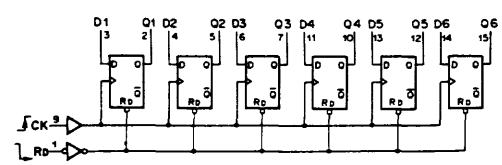
INPUTS				OUTPUTS				
$\overline{R_D}$	CK	A	B	Q1	Q2	----	Q8	
0	X	X	X	0	0	0	0	
1	0	X	X	Q_{1_0}	Q_{2_0}	----	Q_{8_0}	
1	↑	1	1	1	Q_{1n}	----	Q_{7n}	0 ; LOW LEVEL
1	↑	0	X	0	Q_{1n}	----	Q_{7n}	1 ; HIGH LEVEL
1	↑	X	0	0	Q_{1n}	----	Q_{7n}	X ; DON'T CARE

SN74LS174N (TI)

TTL D-TYPE FLIP-FLOP WITH DIRECT RESET

— TOP VIEW —



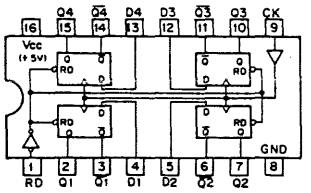


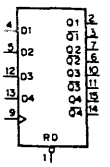
EACH FLIP-FLOP

INPUTS			OUT
$\overline{R_D}$	CK	D	Q
0	X	X	0
1	↑	0	0
1	↑	1	1
1	0	X	Q_0

0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE

MC74F175N (MOTOROLA)
SN74LS175N(TI)
TTL D-TYPE FLIP-FLOP WITH CLEAR
— TOP VIEW —

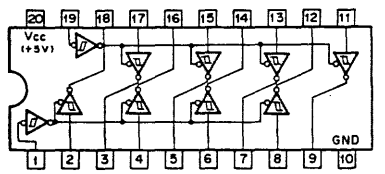




RD	CK	D	Q	$\overline{Q}$
0	X	X	0	1
1	↓	1	1	0
1	↓	0	0	1
1	0	X	Q_0	$\overline{Q}_0$

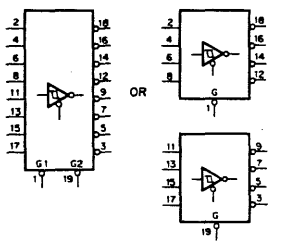
0;LOW LEVEL
1;HIGH LEVEL
X;DON'T CARE

SN74LS240N (TI)
SN74S240N (TI)
SN74ALS244BN(TI)
TTL 3-STATE SCHMITT TRIGGER INVERTER/LINE DRIVER
— TOP VIEW —

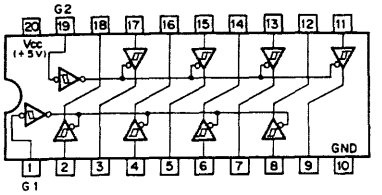


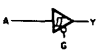
G	A	Y
0	0	1
0	1	0
1	X	HI-Z

0;LOW LEVEL
1;HIGH LEVEL
X;DON'T CARE
HI-Z;HIGH IMPEDANCE



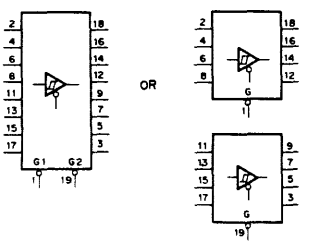
74F244PC(FSC)
MC74F244N (MOTOROLA)
TTL 3-STATE SCHMITT TRIGGER BUFFER/DRIVER
— TOP VIEW —



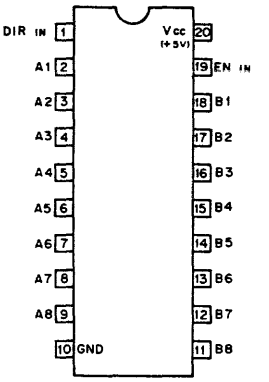


G	A	Y
0	0	0
0	1	1
1	X	HI-Z

0;LOW LEVEL
1;HIGH LEVEL
X;DON'T CARE
HI-Z;HIGH IMPEDANCE

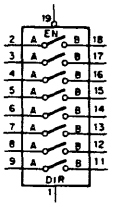


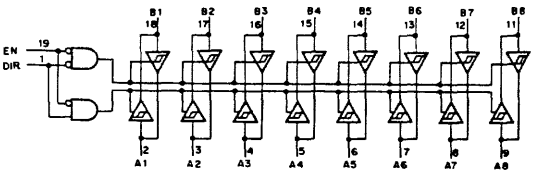
MC74F245N (MOTOROLA)
SN74LS245N (TI)
TTL BILATERAL SCHMITT TRIGGER BUS TRANSCEIVERS WITH 3-STATE OUTPUT
— TOP VIEW —



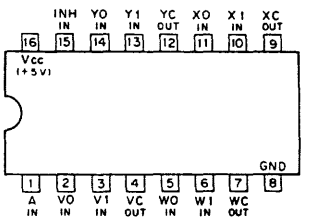
EN	DIR	OPERATION
0	0	B to A
0	1	A to B
1	X	HI-Z

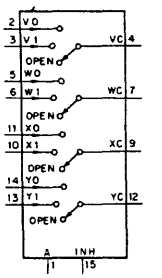
0;LOW LEVEL
1;HIGH LEVEL
X;DON'T CARE.
HI-Z;HIGH IMPEDANCE





SN74LS257BN (TI)
SN74S257N (TI)
TTL 2-LINE-TO-1-LINE DATA SELECTOR/MULTIPLEXER
— TOP VIEW —

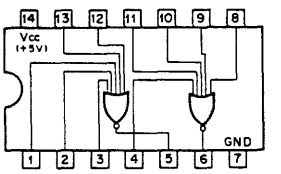


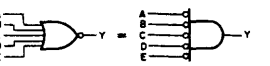


CONT. IN		ON
INH	A	CHANNEL
0	0	0
0	1	1
1	X	OPEN

0;LOW LEVEL
1;HIGH LEVEL
X;DON'T CARE

SN74S260N (TI)
TTL 5-INPUT POSITIVE-NOR GATE
— TOP VIEW —



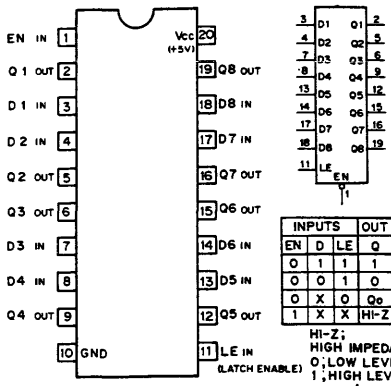


$Y = \overline{A+B+C+D+E} = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} \cdot \overline{E}$

A	B	C	D	E	Y
0	0	0	0	0	1
X	X	X	X	1	0
X	X	X	1	X	0
X	X	1	X	X	0
X	1	X	X	X	0
1	X	X	X	X	0

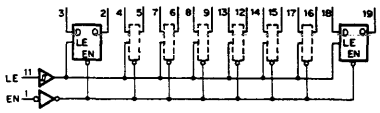
0;LOW LEVEL
1;HIGH LEVEL
X;DON'T CARE

SN74LS373N (TI)
TTL 3-STATE OUTPUTS OCTAL LATCHES
— TOP VIEW —

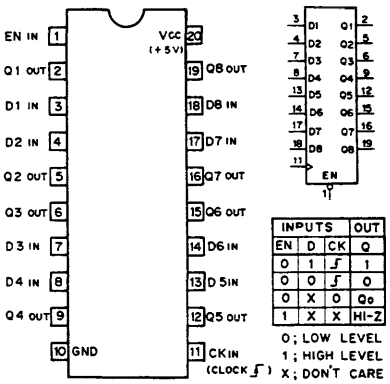


INPUTS			OUT
EN	D	LE	Q
0	1	1	1
0	0	1	0
0	X	0	Q0
1	X	X	HI-Z

HI-Z; HIGH IMPEDANCE
0; LOW LEVEL
1; HIGH LEVEL
X; DON'T CARE

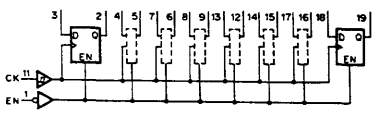


MC74F374N (MOTOROLA)
SN74LS374N (TI)
TTL 3-STATE OUTPUTS OCTAL D-TYPE FLIP-FLOP
— TOP VIEW —

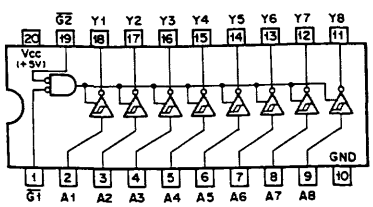


INPUTS			OUT
EN	D	CK	Q
0	1	↓	1
0	0	↓	0
0	X	0	Q0
1	X	X	HI-Z

0; LOW LEVEL
1; HIGH LEVEL
X; DON'T CARE
HI-Z; HIGH IMPEDANCE

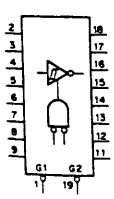


SN74LS540N (TI)
TTL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS
— TOP VIEW —

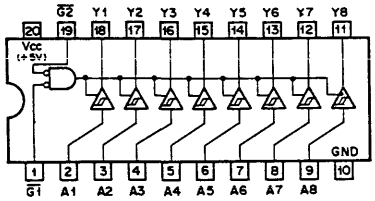


G1	G2	A	Y
0	0	0	1
0	0	1	0
1	X	X	HI-Z
X	1	X	HI-Z

0; LOW LEVEL
1; HIGH LEVEL
X; DON'T CARE
HI-Z; HIGH IMPEDANCE

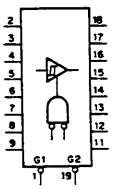


SN74LS541N (TI)
TTL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS
— TOP VIEW —

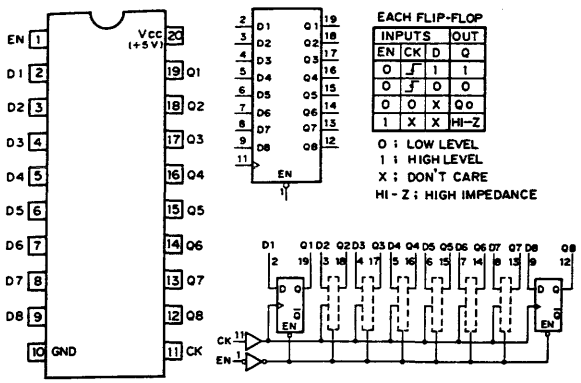


G1	G2	A	Y
0	0	0	0
0	0	1	1
1	X	X	HI-Z
X	1	X	HI-Z

0; LOW LEVEL
1; HIGH LEVEL
X; DON'T CARE
HI-Z; HIGH IMPEDANCE



SN74ALS574AN (TI)
TTL 3-STATE D-TYPE EDGE-TRIGGERED FLIP-FLOP
— TOP VIEW —

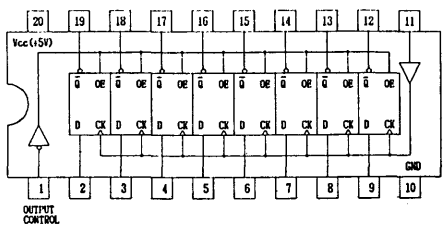


EACH FLIP-FLOP

INPUTS			OUT
EN	CK	D	Q
0	↑	1	1
0	↑	0	0
0	0	X	Q0
1	X	X	HI-Z

0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE
HI-Z ; HIGH IMPEDANCE

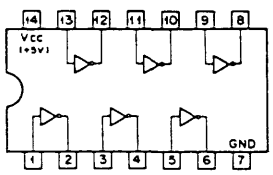
SN74ALS576AN (TI)
D-TYPE EDGE-TRIGGERED FLIP-FLOPS
WITH INVERTED OUTPUTS
— TOP VIEW —

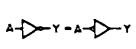


INPUT		OUTPUT
OUTPUT CONTROL	CK	
X	↑	DATA LOAD
1	X	HI-Z

↑ ; HIGH LEVEL
X ; DON'T CARE

SN74AS1004AN (TI)
TTL INVERTER
— TOP VIEW —



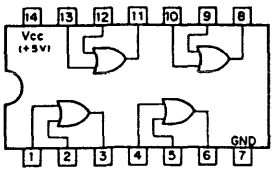


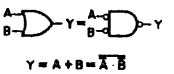
Y = $\overline{A}$

A	Y
0	1
1	0

0: LOW LEVEL
1: HIGH LEVEL

SN74AS1032AN (TI)
MC74F32N (MOTOROLA)
TTL 2-INPUT POSITIVE-OR GATE
— TOP VIEW —

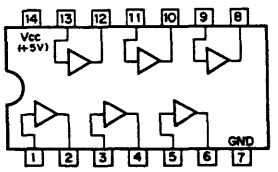




A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

0:LOW LEVEL
1:HIGH LEVEL

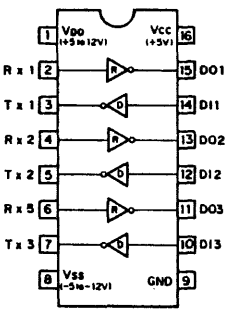
SN74AS1034AN (TI)
TTL BUFFER/DRIVER
— TOP VIEW —

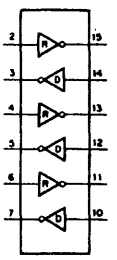


A	Y
0	0
1	1

0; LOW LEVEL
1; HIGH LEVEL

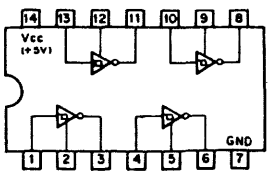
MC145406P (MOTOROLA)
RS-232-C/V.28 DRIVER/RECEIVER
— TOP VIEW —



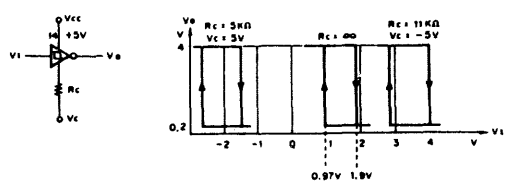


D; DRIVER
R; RECEIVER

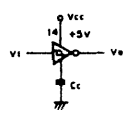
MC1489AP (MOTOROLA)
QUADRUPLE LINE RECEIVER
— TOP VIEW —



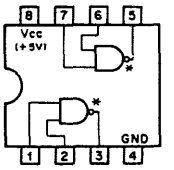
INPUT THRESHOLD SHIFTING

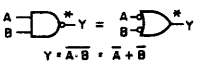


INPUT NOISE FILTERING



SN75452BP (TI)
TTL PERIPHERAL POSITIVE-NAND DRIVER
WITH OPEN-COLLECTOR
— TOP VIEW —

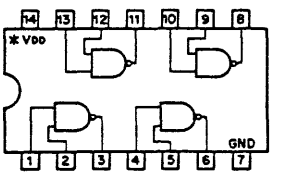


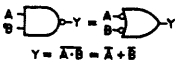


A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

0 ; LOW LEVEL
1 ; HIGH LEVEL

SN74HC00N (TI)
TC74HC00P
C-MOS 2-INPUT NAND GATE
— TOP VIEW —



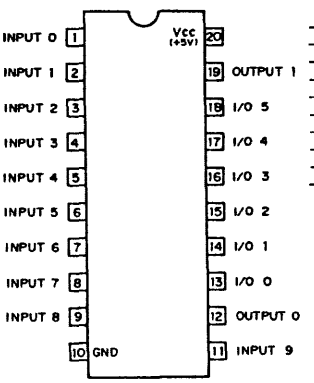


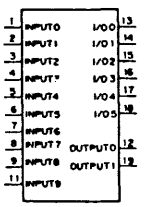
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

0; LOW LEVEL
1; HIGH LEVEL

*Vdd HC; +2 to +6V
HCT; +5V

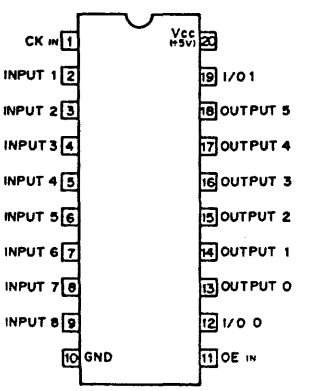
AMPAL16L8APC (AMD)
AMPAL16L8B-PC (AMD) (MEMORIES)
PAL16L8B-CN (MONOLITHIC MEMORIES)
PROGRAMMABLE ARRAY LOGIC
— TOP VIEW —

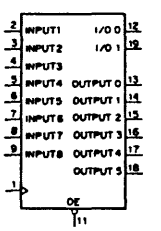




* ABOVE DIAGRAM SHOWS CONDITIONS BEFORE WRITING OF DATA.

PCAMPAL16R6B-PC (AMD)
PAL16R8B-CN (MONOLITHIC MEMORIES)
PROGRAMMABLE ARRAY LOGIC
— TOP VIEW —



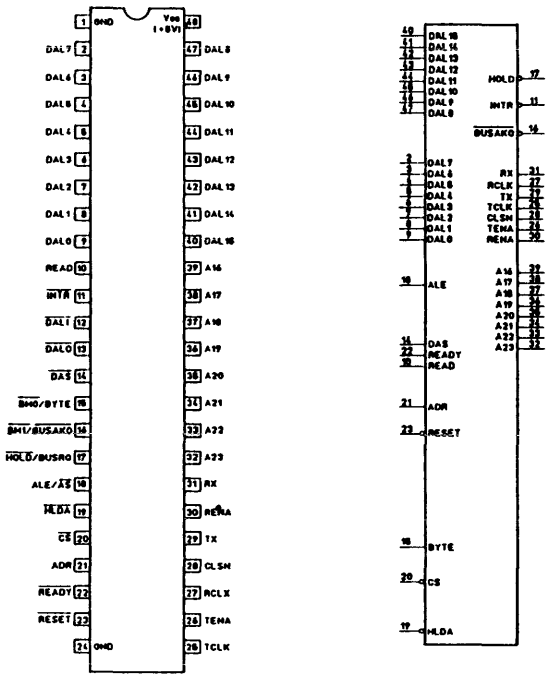


* ABOVE DIAGRAM SHOWS CONDITIONS BEFORE WRITING OF DATA.

AM7990PC-80 (AMC)

LOCAL AREA NETWORK CONTROLLER FOR ETHERNET

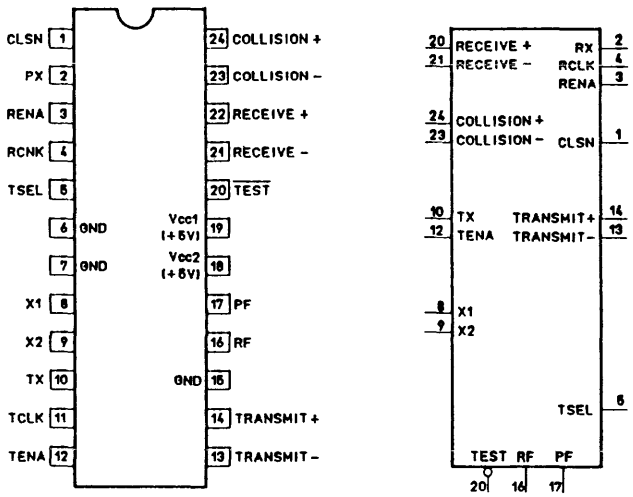
– TOP VIEW –



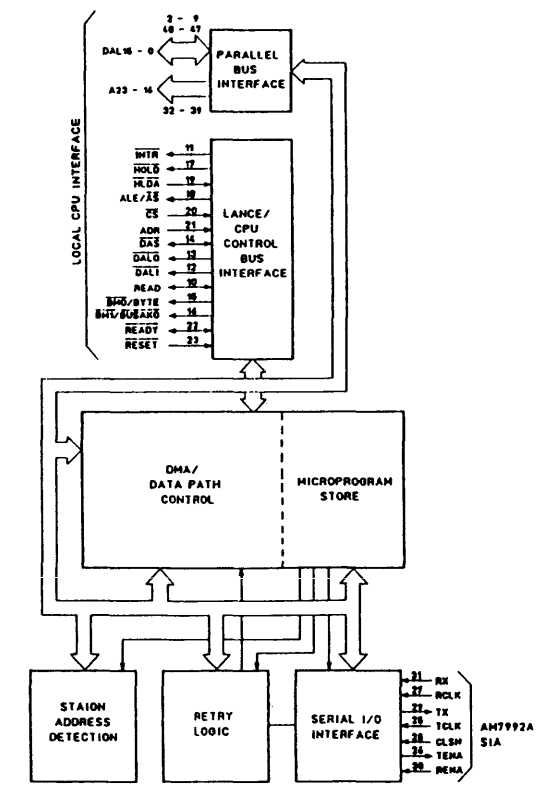
AM7992BDC (AMD)

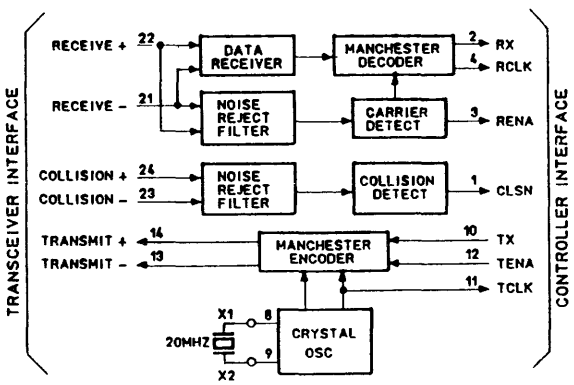
SERIAL INTERFACE ADAPTER

– TOP VIEW –

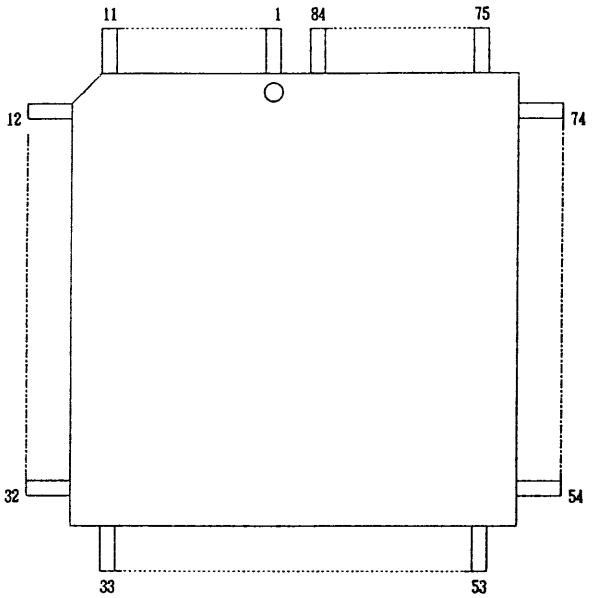



```
CLSN  ;COLLISION
PF    ;RECEIVE PATH PLL FILTER
RCLK  ;RECEIVE CLOCK
RENA  ;CARRIER PRESENT
RF    ;FREQUENCY SETTING VCO LOOP FILTER
RX    ;RECEIVE DATA
TCLK  ;TRANSMIT CLOCK
TENA  ;TRANSMIT ENABLE
TEST  ;TEST CONTROL
TSEL  ;TRANSMIT MODE SELECT
TX    ;TRANSMIT DATA
X1,X2 ;CRYSTAL
```

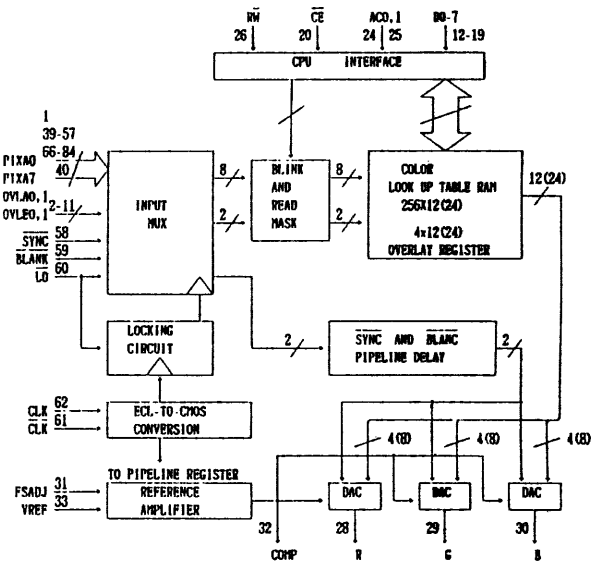




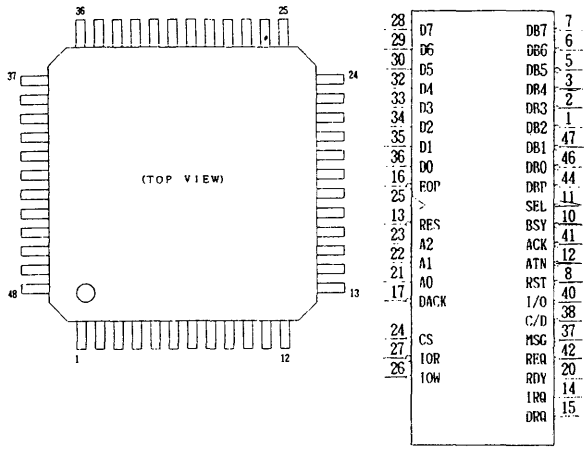
AM81C458JC-80 (AMD)
CMOS COLOR PALETTE
—TOP VIEW—



PIN No.	SIGNAL NAME	PIN No.	SIGNAL NAME	PIN No.	SIGNAL NAME	PIN No.	SIGNAL NAME
1	PIXA0	22	GND(D)	43	PIXE6	64	VCC(D)
2	OVLE1	23	VCC(D)	44	PIXD6	65	GND(D)
3	OVLD1	24	AC0	45	PIXC6	66	PIXE3
4	OVLC1	25	AC1	46	PIXB6	67	PIXD3
5	OVLB1	26	R/W	47	PIXA6	68	PIXC3
6	OVLA1	27	VCC(A)	48	PIXE5	69	PIXB3
7	OVLE0	28	R	49	PIXD5	70	PIXA3
8	OVLD0	29	G	50	PIXC5	71	PIXE2
9	OVLC0	30	B	51	PIXB5	72	PIXD2
10	OVLB0	31	FSADJ	52	PIXA5	73	PIXC2
11	OVLA0	32	COMP	53	PIXE4	74	PIXB2
12	D0	33	VREF	54	PIXD4	75	PIXA2
13	D1	34	GND(A)	55	PIXC4	76	PIXE1
14	D2	35	VCC(A)	56	PIXB4	77	PIXD1
15	D3	36	GND(A)	57	PIXA4	78	PIXC1
16	D4	37	VCC(A)	58	SYNC	79	PIXB1
17	D5	38	PIXE7	59	BLANK	80	PIXA1
18	D6	39	PIXD7	60	LD	81	PIXE0
19	D7	40	PIXC7	61	CLK	82	PIXD0
20	CE	41	PIXB7	62	CLK	83	PIXC0
21	GND(D)	42	PIXA7	63	VCC(D)	84	PIXB0

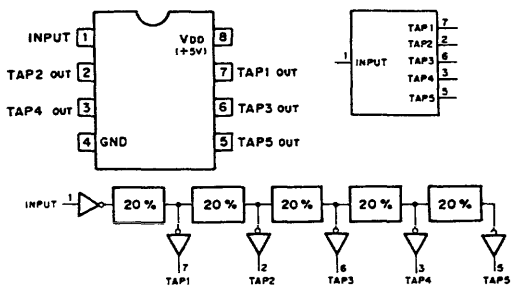


CXD1180Q-Z (SONY)
SCSI INTERFACE



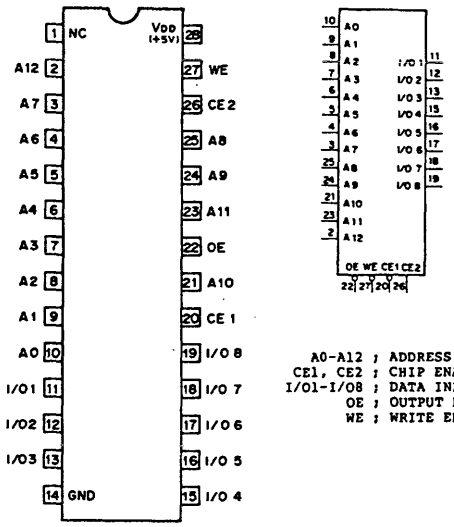
PIN No.	SIGNAL	I/O	PIN No.	SIGNAL	I/O	PIN No.	SIGNAL	I/O	PIN No.	SIGNAL	I/O
1	$\overline{DB2}$	I/O	13	$\overline{RES}$	I	25	CLK	I	37	$\overline{MSG}$	I/O
2	$\overline{DB3}$	I/O	14	IRQ	O	26	$\overline{IOW}$	I	38	$\overline{C/D}$	I/O
3	$\overline{DB4}$	I/O	15	DRQ	O	27	$\overline{IOR}$	I	39	Vss	
4	Vss	I/O	16	$\overline{EOP}$	I	28	D7	I/O	40	$\overline{I/O}$	I/O
5	$\overline{DB5}$	I/O	17	$\overline{DACK}$	I	29	D6	I/O	41	$\overline{ACK}$	I/O
6	$\overline{DB6}$	I/O	18	Vss	O	30	D5	I/O	42	$\overline{REQ}$	I/O
7	$\overline{DB7}$	I/O	19	V_{DD}	O	31	V_{DD}		43	V_{DD}	
8	$\overline{RST}$	I/O	20	RDY	O	32	D4	I/O	44	$\overline{DBP}$	I/O
9	Vss	I/O	21	A0	I	33	D3	I/O	45	Vss	
10	$\overline{BSY}$	I/O	22	A1	I	34	D2	I/O	46	$\overline{DB0}$	I/O
11	$\overline{SEL}$	I/O	23	A2	I	35	D1	I/O	47	$\overline{DB1}$	I/O
12	$\overline{ATN}$	I/O	24	$\overline{CS}$	I	36	D0	I/O	48	Vss	

DS1000M-50 (DALLAS SEMICONDUCTOR) (DELAY TIME = 50nS)
C-MOS DELAY LINE
— TOP VIEW —



TYPE. NO.	DELAY TIME (ns)				
	TAP1	TAP2	TAP3	TAP4	TAP5
DS1000M-50	10	20	30	40	50
DS1000M-60	12	24	36	48	60
DS1000M-75	15	30	45	60	75
DS1000M-100	20	40	60	80	100
DS1000M-125	25	50	75	100	125
DS1000M-150	30	60	90	120	150
DS1000M-175	35	70	105	140	175
DS1000M-200	40	80	120	160	200
DS1000M-250	50	100	150	200	250
DS1000M-500	100	200	300	400	500

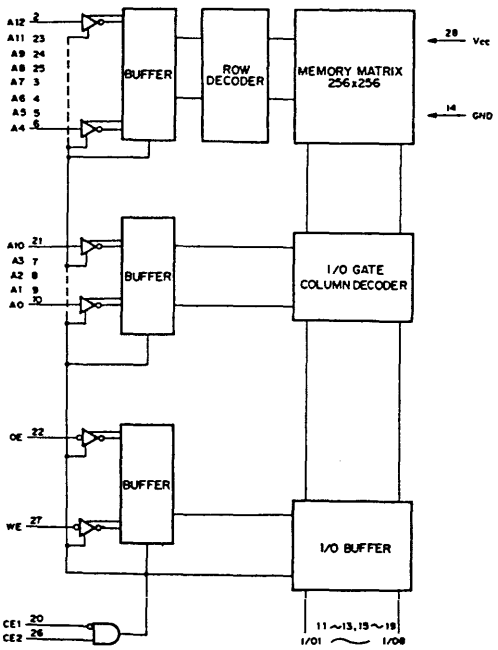
CXK5864BSP-10L
CMOS 8192 WORDx8 BIT STATIC RAM
— TOP VIEW —



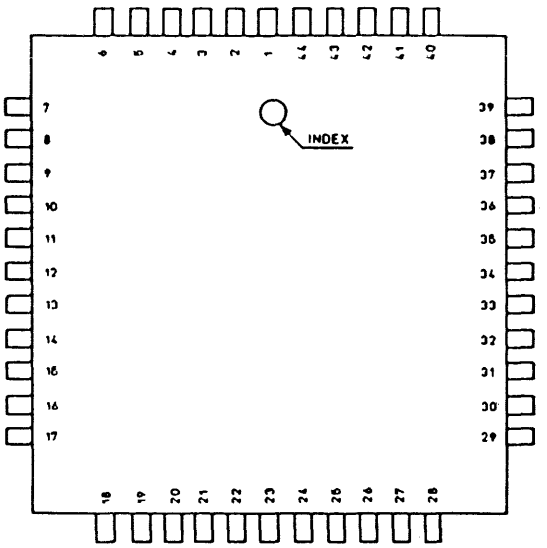
A0-A12 ; ADDRESS INPUT
CE1, CE2 ; CHIP ENABLE INPUT
I/O1-I/O8 ; DATA INPUT/OUTPUT
OE ; OUTPUT ENABLE INPUT
WE ; WRITE ENABLE INPUT

CE1	CE2	OE	WE	MODE	I/O TERMINAL
1	X	X	X	NOT SELECT	HIGH IMPEDANCE
X	0	X	X	NOT SELECT	HIGH IMPEDANCE
0	1	1	1	OUTPUT DISABLE	HIGH IMPEDANCE
0	1	0	1	READ	OUTPUT DATA
0	1	X	0	WRITE	INPUT DATA

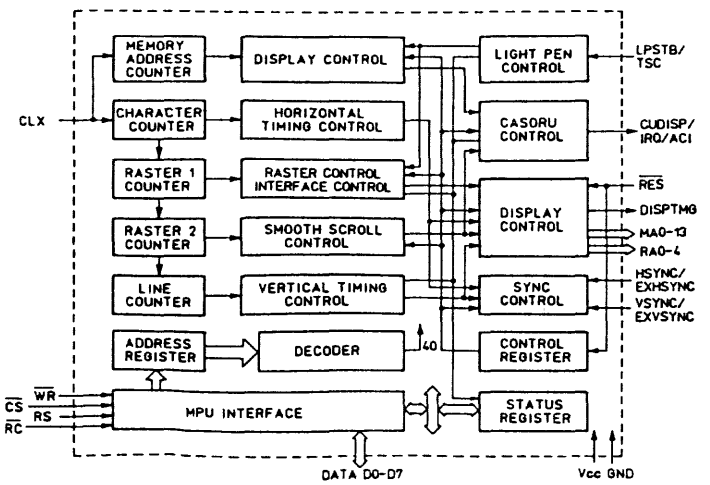
0;LOW LEVEL
1;HIGH LEVEL
X;DON'T CARE



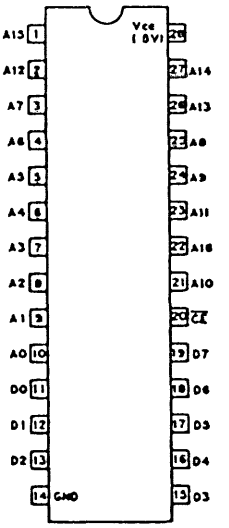
HD6445CP4 (HITACHI)
CRT CONTROLLER
– TOP VIEW –

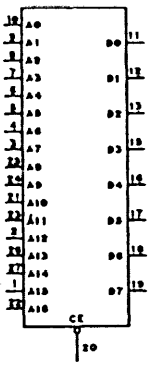


PIN No	SIGNAL NAME	PIN No	SIGNAL NAME	PIN No	SIGNAL NAME	PIN No	SIGNAL NAME
1	GND 1	12	NC	23	VCC2	34	NC
2	GND 2	13	MA7	24	CLK	35	D2
3	$\overline{RES}$	14	MA8	25	$\overline{WR}$	36	D1
4	LPSTB/TSC	15	MA9	26	$\overline{RD}$	37	D0
5	MA0	16	MA10	27	RS	38	RA4
6	MA1	17	MA11	28	$\overline{CS}$	39	RA3
7	MA2	18	MA12	29	D7	40	RA2
8	MA3	19	MA13	30	D6	41	RA1
9	MA4	20	DISPTMG	31	D5	42	RA0
10	MA5	21	CUDISP/ACI	32	D4	43	HSYNC/EXHSYNC
11	MA6	22	VCC1	33	D3	44	VSYNC/EXVSYNC

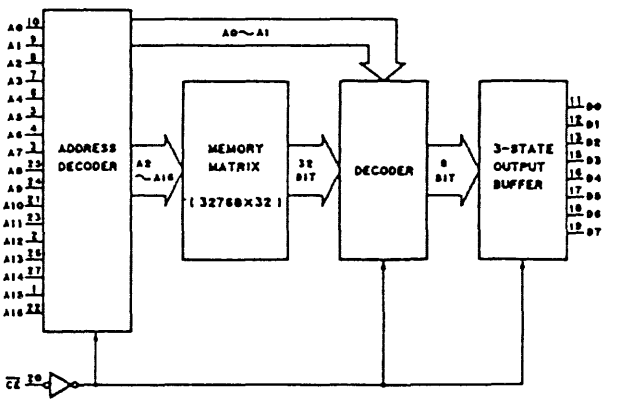


HN62321BPAA1
C-MOS 131,072WORDx8-BIT MASK PROGRAMMABLE ROM
– TOP VIEW –



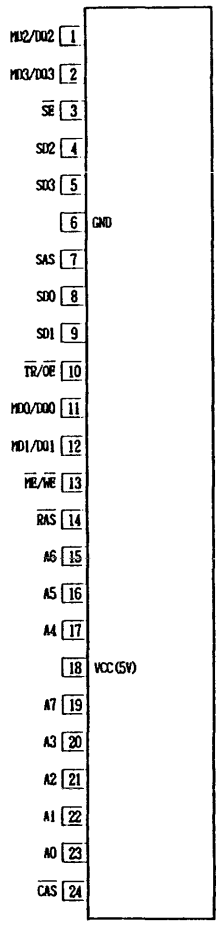


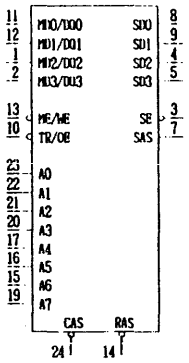
A0~A12 ; ADDRESS INPUTS
CE ; CHIP ENABLE
D0~D7 ; DATA OUTPUT



MB81461-12PSZ (FUJITSU)

N-MOS 256K BIT DUAL PORT DYNAMIC RAM
— SIDE VIEW —





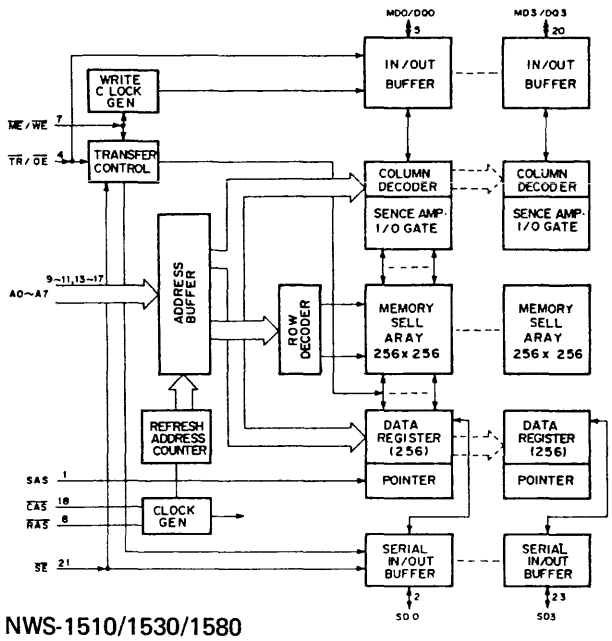
A0-A7 ; ADDRESS
CAS ; COLUMN ADDRESS STROBE
MDO/DQO-MD3/DQ3 ; MASK DATA/DATA IN/OUT
ME/WE ; MASK MODE ENABLE/WRITE ENABLE
SAS ; SERIAL ACCESS MEMORY STROBE
SDO-SD3 ; SERIAL DATA IN/OUT
SE ; SERIAL PORT ENABLE
TR/OE ; TRNSFER ENABLE/OUTPUT ENABLE

RAS SIGNAL			RAM	SAM
TR/OE	WE	SE		
1	1	X	READ/WRITE	NON
	0	X	BIT MASK WRITE	NON
0	1	X	READ TRANSFER RAM→SAM	OUTPUT MODE SET
	0	0	WRITE TRANSFER SAM→RAM	INPUT MODE SET
		1	READ REFRESH	INPUT MODE SET

0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE
HI-Z ; HIGH IMPEDANCE

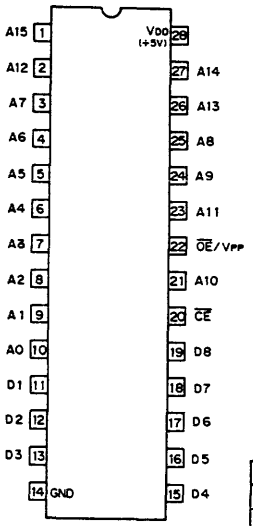
NORMALY READ/WRITE

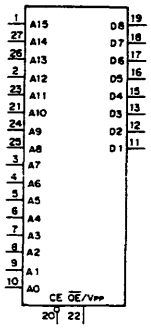
RAS	CAS	ME/WE	TR/OE	ADDRES	DQO ~ DQ3	
1	1	X	X	X	X	STANDBY
0	0	1	↓	FIXED	DATA OUTPUT FIXED	READ
0	0	0	1→X	FIXED	DATA INPUT FIXED	EARLY WRITE
0	0	↓	1→X	FIXED	DATA INPUT FIXED	DELAYED WRITE
0	0	↓	↓↑	FIXED	DATA OUTPUT FIXED → DATA INPUT FIXED	READ MODIFY WRITE
0	1	X	1→X	ROW	HI-Z	RAS ONLY REFRESH
↓	0	X	1→X	X	HI-Z	CAS BEFORE RAS REFRESH



MBM27C512-25 (FUJISTU) (ACCESS TIME 250nS)

C-MOS 512K(524,288)-BIT ERASABLE PROM
— TOP VIEW —

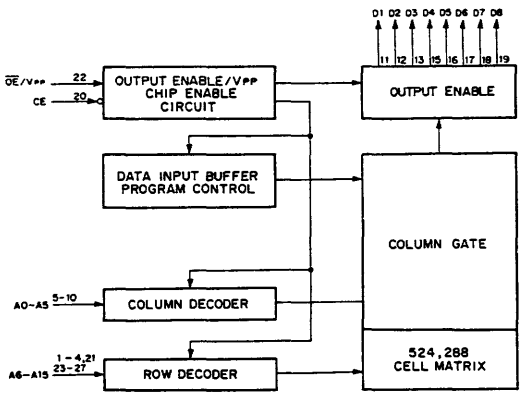




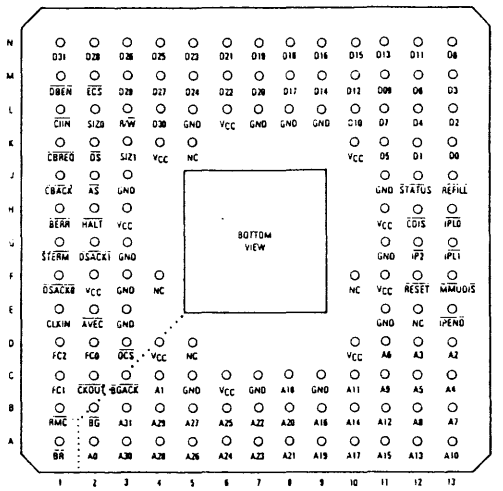
A0-A15; ADDRESS BUS
CE; CHIP ENABLE
D1-D8; DATA OUT
OE; OUTPUT ENABLE
VPP; PROGRAM POWER SUPPLY

An	CE	OE/Vpp	Vcc	Dn	FUNCTION
AIN	0	0	+5V	DOUT	READ
AIN	0	1	+5V	HI-Z	OUTPUT DISABLE
X	1	X	+5V	HI-Z	STANDBY
AIN	0	+12.5V	+6V	DIN	PGM
AIN	0	0	+6V	DOUT	PGM VERIFY
X	1	+12.5V	+6V	HI-Z	PGM INH

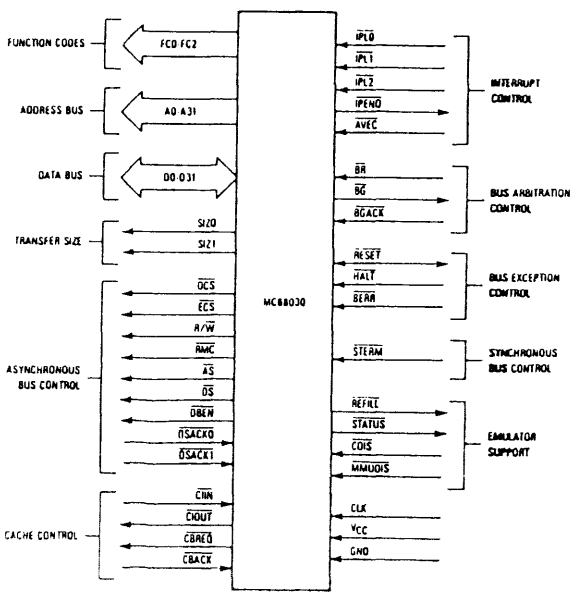
0; LOW LEVEL
1; HIGH LEVEL
HI-Z; HIGH IMPEDANCE
X; DON'T CARE



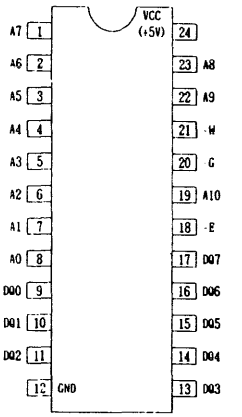
MC68030RC25 (MOTOROLA)
HC-MOS 32 BIT MICROPROCESSOR
— BOTTOM VIEW —

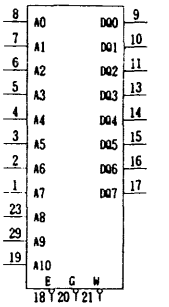


A0-31	; ADDRESS BUS
AS	; ADDRESS STROBE
AVEC	; AUTO VECTOR
BERR	; BUS ERROR
BG	; BUS GRANT
BGACK	; BUS GRANT ACKNOWLEDGE
BR	; BUS REQUEST
CBACK	; CACHE BURST ACKNOWLEDGE
CBREQ	; CACHE BURST REQUEST
CDIS	; CACHE DISABLE
CIIN	; CACHE INHIBIT IN
CIOUT	; CACHE INHIBIT OUT
CLK	; CLOCK
D0-31	; DATA BUS
DBEN	; DATA BUFFER ENABLE
DS	; DATA STROBE
DSACK0,1	; DATA TRANSFER AND SIZE ACKNOWLEDGE
ECS	; EXTERNAL CYCLE START
FC0-3	; FUNCTION CODE SIGNAL
HALT	; HALT
IPEND	; INTERRUPT PENDING
IPL0-2	; INTERRUPT PRIORITY LEVEL
MMUDIS	; MMU DISABLE
OCS	; OPERAND CYCLE START
REFILL	; PIPELINE REFILL
RESET	; RESET
RMC	; READ MODIFY/WRITE CYCLE
R/W	; READ/WRITE
SIZ0,1	; TRANSFER SIZE
STATUS	; MICROSEQUENCER STATUS
STERM	; SYNCHRONOUS TERMINATION

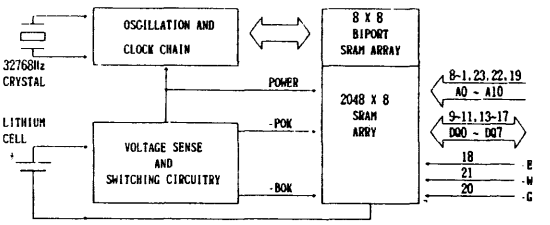


MK48T02(B)-25(TOMEN)
REAL TIME CLOCK
— TOP VIEW —

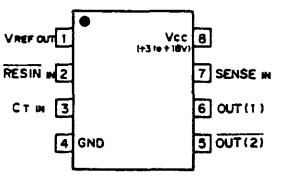




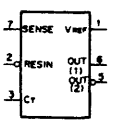
A0 ~ A10:ADDRESS INPUT
DQ0~ DQ7:DATA IN/DATA OUT
-E:CHIP ENABLE
-W:WRITE ENABLE
-G:OUTPUT ENABLE

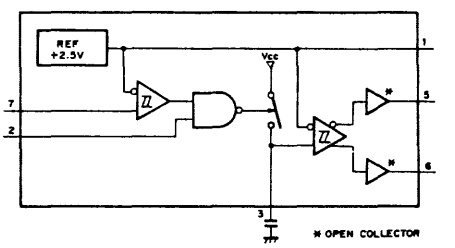


TL7705CPS-B (TI)
— TOP VIEW —

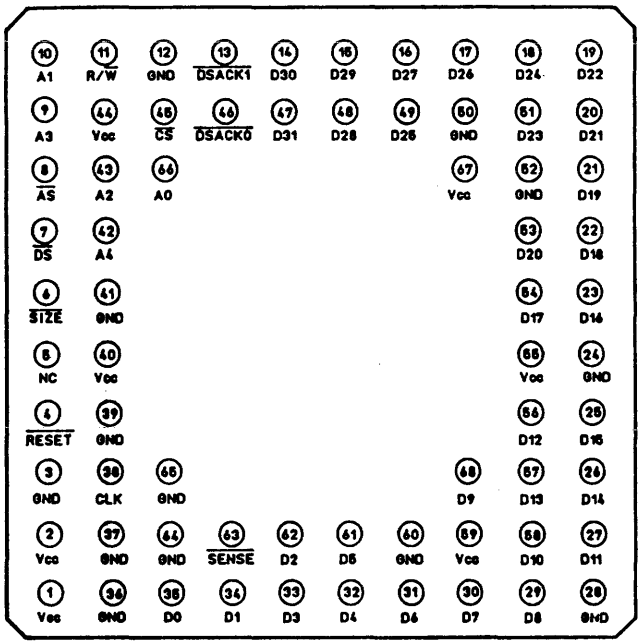


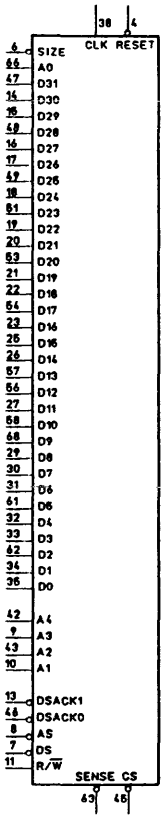
TL7705CP



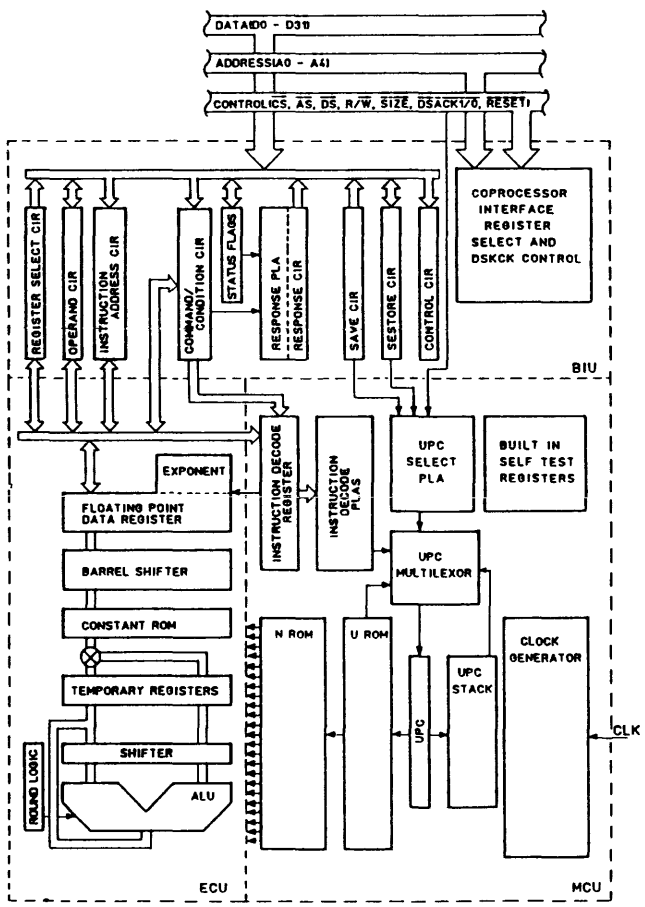


MC68881RC-25
HC MDS
– BOTTOM VIEW –





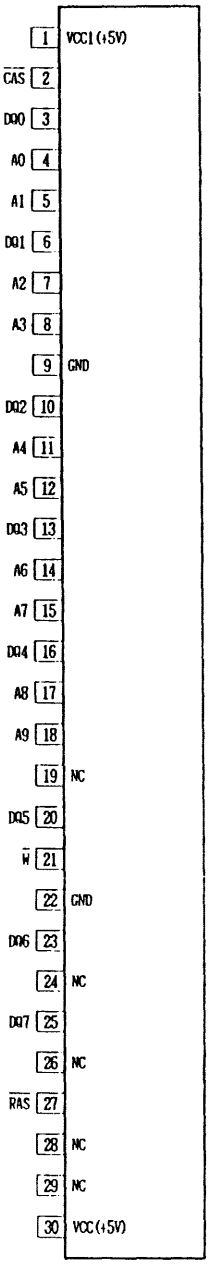
AO-A4 ;HIGH ADDRESS BUS INPUT
AS ;LOW ADDRESS STROBE INPUT
CS ;LOW CHIP SELECT INPUT
CLK ;CLOCK INPUT
DO-D13 ;HIGH DATA BUS INPUT/OUTPUT
DS ;LOW DATA STROBE INPUT
DSACKO,1;LOW DATA TRANSFER AND SIZE ACKNOWLEDGE OUTPUT
R/-W ;HIGH/LOW READ/WRITE INPUT
RESET ;LOW RESET INPUT

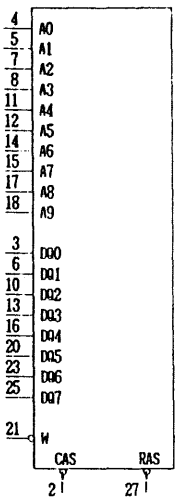


THM81000L-80

1,048,576-WORD x 8-BIT DYNAMIC RAM MODULE

— MOUNTED SIDE VIEW —



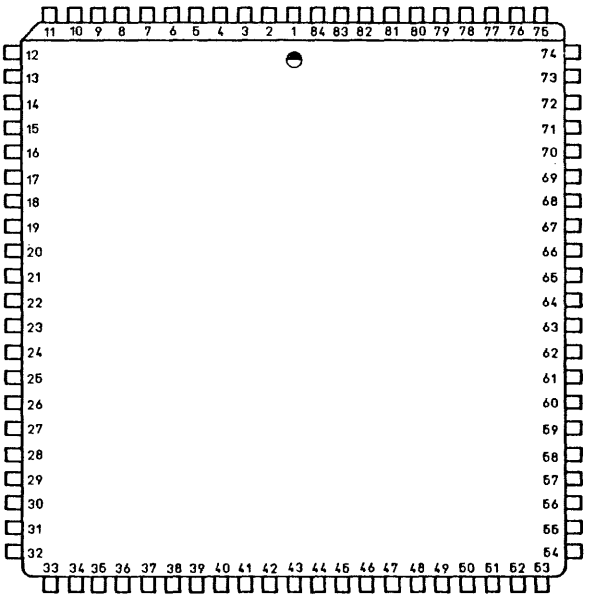


A0-A9: ADDRESS INPUT
CAS: COLUMN ADDRESS STROBE
DQ0-DQ7: DATA INPUT/OUTPUT
RAS: ROW ADDRESS STROBE
W: READ/WRITE INPUT

WSC-SBLT (FUJITSU)

RASTER OPERATION CONTROLLER

-TOP VIEW-

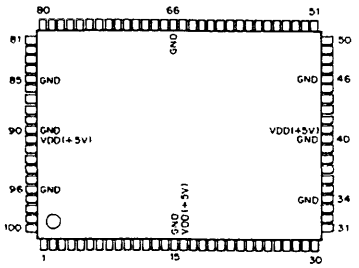


PIN No.	I/O	PIN NAME	PIN No.	I/O	PIN NAME	PIN No.	I/O	PIN NAME	PIN No.	I/O	PIN NAME
1	—	VSS	22	—	VSS	43	—	VSS	64	—	VSS
2	I/O	DA0	23	I	XSWPE	44	I/O	DB0	65	I/O	HD0
3	I/O	DA1	24	I	LATCHDT	45	I/O	DB1	66	I/O	HD1
4	I/O	DA2	25	I	XOE	46	I/O	DB2	67	I/O	HD2
5	I/O	DA3	26	I	XAMSKRST	47	I/O	DB3	68	I/O	HD3
6	I/O	DA4	27	I	XRD	48	I/O	DB4	69	I/O	HD4
7	I/O	DA5	28	I	XEA	49	I/O	DB5	70	I/O	HD5
8	I/O	DA6	29	I	XSSC	50	I/O	DB6	71	I/O	HD6
9	I/O	DA7	30	I	XEDR	51	I/O	DB7	72	I/O	HD7
10	O	SRDA	31	I	INCX	52	I	AMSKSEL	73	I	WPB3
11	O	SRDB	32	I	DRCT	53	I	WDBALL	74	I	WPB2
12	—	N.C.	33	I	MSKSL0	54	I	WDAALL	75	I	WPB1
13	I/O	DA8	34	I	MSKSL1	55	I/O	DB8	76	I	WPB0
14	I/O	DA9	35	I	XSRP	56	I/O	DB9	77	I/O	HD8
15	I/O	DA10	36	I	XSLM	57	I/O	DB10	78	I/O	HD9
16	I/O	DA11	37	I	XSRM	58	I/O	DB11	79	I/O	HD10
17	I/O	DA12	38	I	XELM	59	I/O	DB12	80	I/O	HD11
18	I/O	DA13	39	I	XERM	60	I/O	DB13	81	I/O	HD12
19	I/O	DA14	40	I	XSDR	61	I/O	DB14	82	I/O	HD13
20	I/O	DA15	41	I	XSSR	62	I/O	DB15	83	I/O	HD14
21	—	VDD	42	I	XSDWR	63	—	VDD	84	I/O	HD15

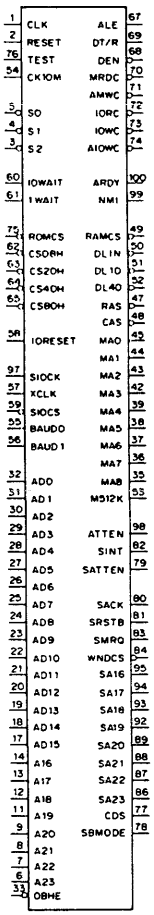
uPD65013G-160 (SONY)

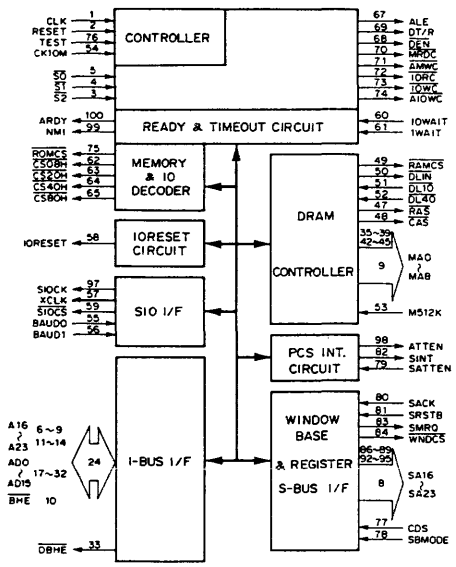
C-MOS PERIPHERAL CONTROLLER

— TOP VIEW —



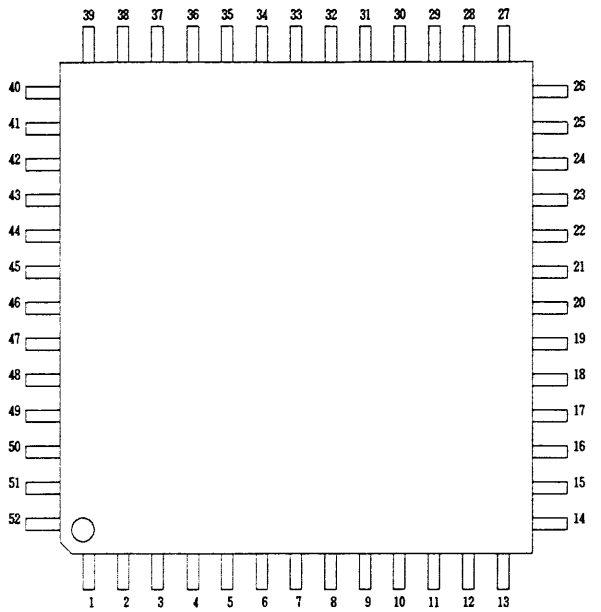
PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME
1	CLK	26	AD6	51	DL10	76	TEST
2	RESET	27	AD5	52	DL40	77	CDS
3	S2	28	AD4	53	M512K	78	SBMODE
4	S1	29	AD3	54	CK10M	79	SATTEN
5	S0	30	AD2	55	BAUD0	80	SACK
6	A23	31	AD1	56	BAUD1	81	SRSTB
7	A22	32	AD0	57	XCLK	82	SINT
8	A21	33	OBHE	58	IORESET	83	SMRQ
9	A20	34	GND	59	SIOCS	84	WNDCS
10	BHE	35	MA8	60	IOWAIT	85	GND
11	A19	36	MA7	61	1WAIT	86	SA23
12	A18	37	MA6	62	CS08H	87	SA22
13	A17	38	MA5	63	CS20H	88	SA21
14	A16	39	MA4	64	CS40H	89	SA20
15	GND	40	GND	65	CS80H	90	GND
16	VDD(+5V)	41	VDD(+5V)	66	GND	91	VDD(+5V)
17	AD15	42	MA3	67	ALE	92	SA19
18	AD14	43	MA2	68	DEN	93	SA18
19	AD13	44	MA1	69	DT/R	94	SA17
20	AD12	45	MA0	70	MRDC	95	SA16
21	AD11	46	GND	71	AMWC	96	GND
22	AD10	47	RAS	72	IORC	97	SIOCK
23	AD9	48	CAS	73	IOWC	98	ATTEN
24	AD8	49	RAMCS	74	AIOWC	99	NMI
25	AD7	50	DLIN	75	ROMCS	100	ARDY



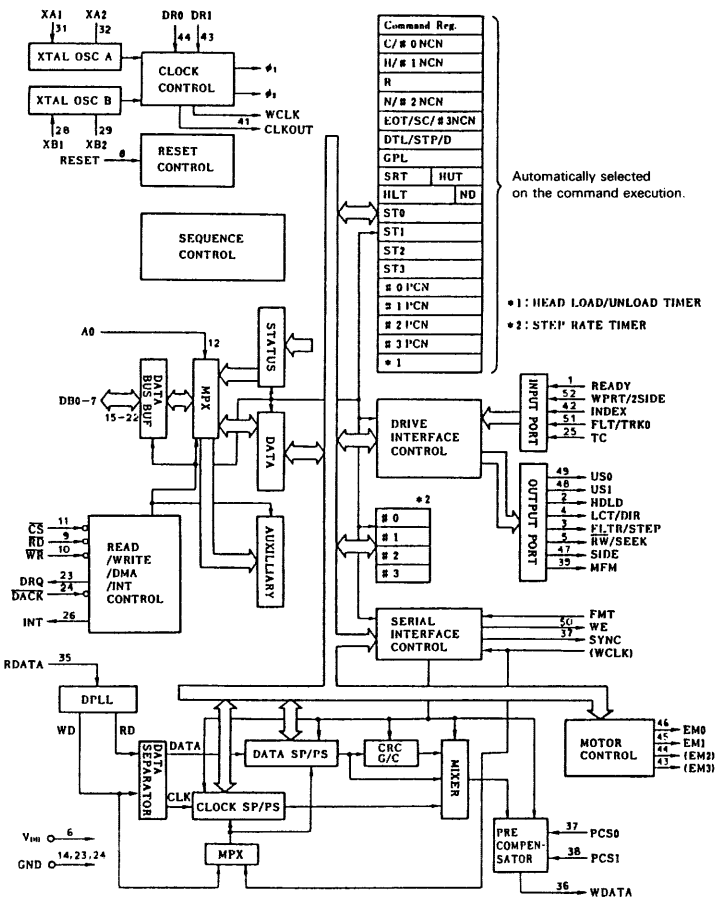



```
1WAIT     ;1 WAIT
A16-A20   ;ADDRESS/STATUS BUS
A20-A23   ;ADDRESS BUS
AD0-AD15  ;ADDRESS/DATA BUS
AIOWC     ;ADVANCED I/O WRITE COMMAND
ALE       ;ADDRESS LATCH ENABLE
AMWC      ;ADVANCED MEMORY WRITE COMMAND
ARDY      ;ASYNCRONOUS READY
ATTEN     ;ATTENTION TO CPU
BAUD0,1   ;BAUD-RATE 0,1
BHE       ;BYTE HIGH ENABLE
CAS       ;COLUMN ADDRESS STROBE
CDS       ;COMP/DECOMPRESSION SUBSYSTEM MODE
CK10M     ;CLOCK 10MHZ
CLK       ;CLOCK
CS08H     ;I/O ADDRESS 08H CHIP SELECT
CS20H     ;I/O ADDRESS 20H CHIP SELECT
CS40H     ;I/O ADDRESS 40H CHIP SELECT
CS80H     ;I/O ADDRESS 80H CHIP SELECT
DEN       ;DATA ENABLE
DL10      ;DELAY LINE 10NS
DL40      ;DELAY LINE 40NS
DLIN      ;DELAY LINE INPUT
DT/R      ;DATA TRANSMIT/RECEIVE
IORC      ;I/O READ COMMAND
IORESET   ;I/O RESET
IOWAIT    ;I/O WAIT
IOWC      ;I/O WRITE COMMAND
M512K     ;MEMORY 512KB ENABLE
MA0-MA8   ;MEMORY ADDRESS BUS
MRDC      ;MEMORY READ COMMAND
NMI       ;NON MASKABLE INTERRUPT
OBHE      ;OUTPUT OF BYTE HIGH ENABLE
RAMCS     ;RAM CHIP SELECT
RAS       ;ROW ADDRESS STROBE
RESET     ;RESET
ROMCS     ;ROM CHIP SELECT
S0-S2     ;STATUS
SA16-SA23;SYSTEM ADDRESS BUS
SACK      ;SYSTEM ACKNOWLEDGE
SATTEN    ;SYSTEM ATTENTION FROM PCS
SBMODE    ;SYSTEM BUS MODE
SINT      ;SYSTEM INTERRUPT
SIOCK     ;SIO CLOCK
SIOCS     ;SIO CHIP SELECT
SMRQ      ;SYSTEM MEMORY REQUEST
SRSTB     ;SYSTEM READ STROBE
TEST      ;TEST MODE
WNDCS     ;WINDOW CHIP SELECT
XCLK      ;TX/RX CLOCK
```

UPD72067GC-3B6 (NEC)
C-MOS PROGRAMMABLE FLOPPY DISK CONTROLLER
–TOP VIEW–

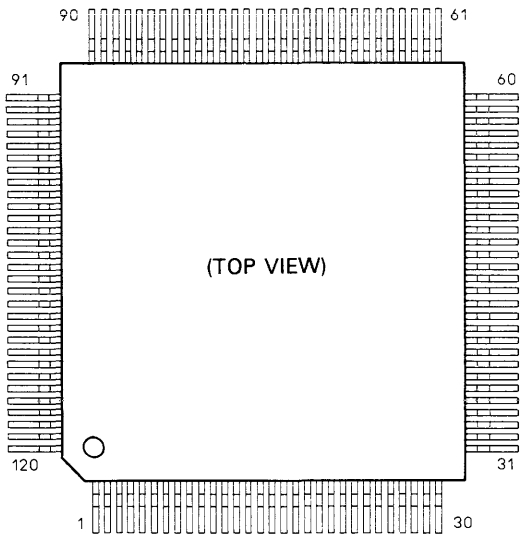


PIN No.	SIMBOL	PIN No.	SIMBOL
1	READY	27	NC
2	HOLD	28	XB1
3	FLTR/STEP	29	XB2
4	LCT/DIR	30	EXT
5	RW/SEEK	31	XA1
6	VDD	32	XA2
7	NC	33	GND
8	RESET	34	GND
9	RD	35	RDATA
10	WR	36	WDATA
11	CS	37	PCS0 (SYNC)
12	A0	38	PCS1 (WINDOW)
13	NC	39	FMT (MFM)
14	GND	40	NC
15	DB0	41	CLKOUT
16	DB1	42	INDEX
17	DB2	43	DR1 (EM3)
18	DB3	44	DR0 (EM2)
19	DB4	45	EM1
20	DB5	46	EM0
21	DB6	47	SIDE
22	DB7	48	US1
23	DRQ	49	US0
24	DACK	50	WE
25	TC	51	FLT/TRK0
26	INT	52	WPRT/2SIDE

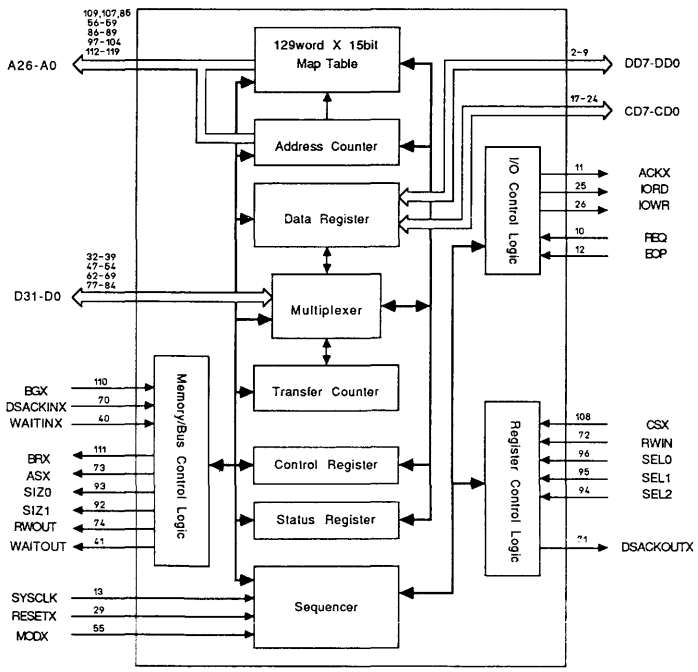


( ): Using the external VFO.
(when the internal mode is EXT=1 or the external mode.)

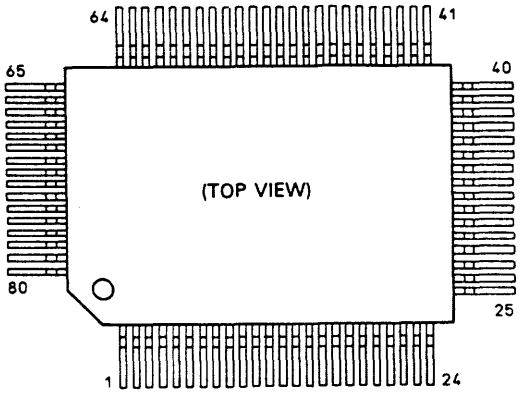
WSC-ICKDMAC (LSI LOGIC)
DMA CONTROLLER



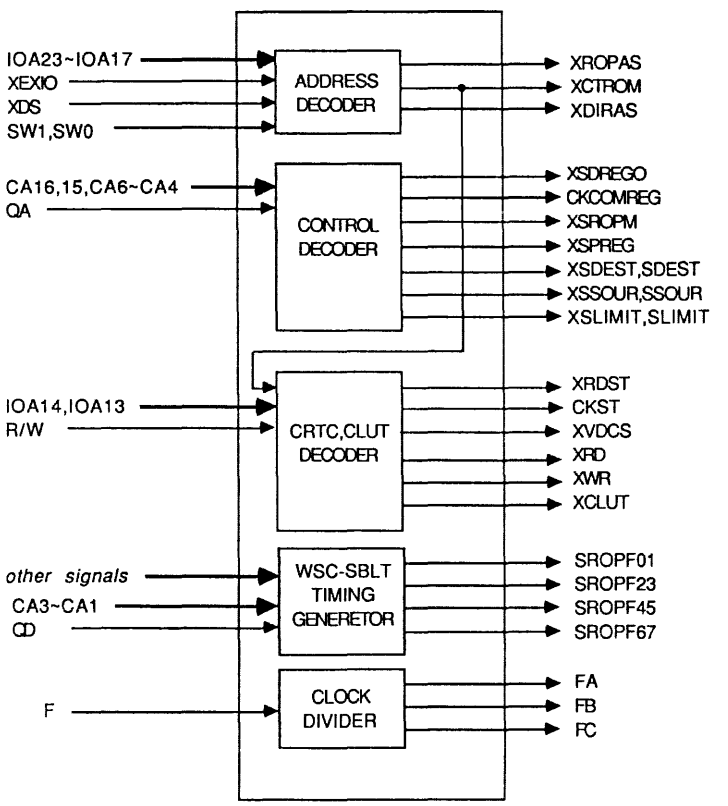
PIN	I/O	PIN NAME	PIN	I/O	PIN NAME	PIN	I/O	PIN NAME
1	-	GND	41	O	WAITOUT	81	I/O	D3
2	I/O	DD7	42	-	N.C.	82	I/O	D2
3	I/O	DD6	43	-	N.C.	83	I/O	D1
4	I/O	DD5	44	-	N.C.	84	I/O	D0
5	I/O	DD4	45	-	GND	85	O	A24
6	I/O	DD3	46	-	VDD	86	O	A19
7	I/O	DD2	47	I/O	D23	87	O	A18
8	I/O	DD1	48	I/O	D22	88	O	A17
9	I/O	DD0	49	I/O	D21	89	O	A16
10	I	REQ	50	I/O	D20	90	-	GND
11	O	ACKX	51	I/O	D19	91	-	VDD
12	I	ECP	52	I/O	D18	92	O	SIZ1
13	I	SYSCLK	53	I/O	D17	93	O	SIZ0
14	-	N.C.	54	I/O	D16	94	I	SEL2
15	-	VDD	55	I	MODX	95	I	SEL1
16	-	GND	56	O	A23	96	I	SEL0
17	I/O	CD7	57	O	A22	97	O	A15
18	I/O	CD6	58	O	A21	98	O	A14
19	I/O	CD5	59	O	A20	99	O	A13
20	I/O	CD4	60	-	GND	100	O	A12
21	I/O	CD3	61	-	VDD	101	O	A11
22	I/O	CD2	62	I/O	D15	102	O	A10
23	I/O	CD1	63	I/O	D14	103	O	A9
24	I/O	CD0	64	I/O	D13	104	O	A8
25	O	IORD	65	I/O	D12	105	-	VDD
26	O	IOWR	66	I/O	D11	106	-	GND
27	-	N.C.	67	I/O	D10	107	O	A25
28	-	N.C.	68	I/O	D9	108	I	CSX
29	I	RESETX	69	I/O	D8	109	O	A26
30	-	VDD	70	I	DSACKINX	110	I	BGX
31	-	GND	71	O	DSACKOUTX	111	O	BRX
32	I/O	D31	72	I	RWIN	112	O	A7
33	I/O	D30	73	I	ASX	113	O	A6
34	I/O	D29	74	O	RWOUT	114	O	A5
35	I/O	D28	75	-	GND	115	O	A4
36	I/O	D27	76	-	VDD	116	O	A3
37	I/O	D26	77	I/O	D7	117	O	A2
38	I/O	D25	78	I/O	D6	118	O	A1
39	I/O	D24	79	I/O	D5	119	O	A0
40	I	WAITINX	80	I/O	D4	120	-	VDD



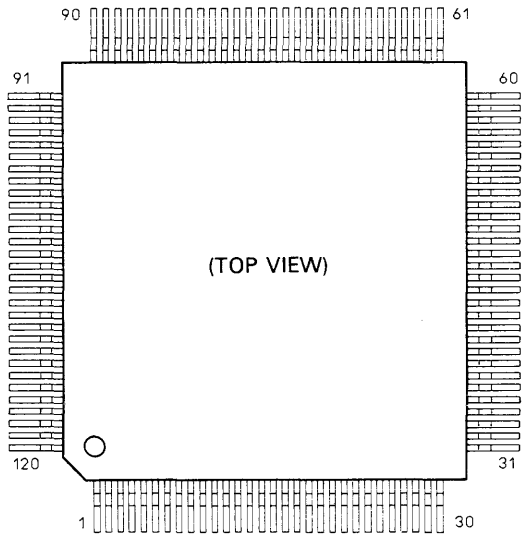
WSC-CGLUE (NEC)
MEMORY CONTROLLER



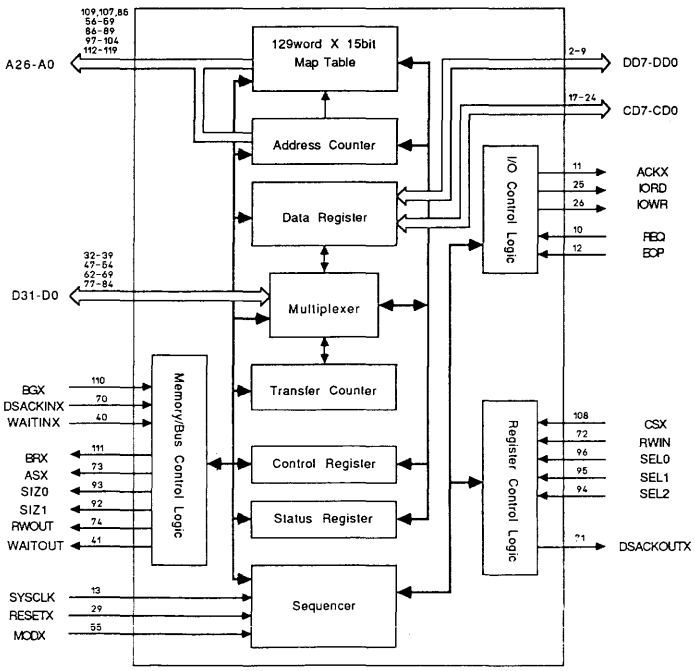
Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name
1	O	XDIRF	21	I	IOA21	41	I	QA	61	O	XSLIMIT
2	–	VSS	22	I	IOA20	42	–	VSS	62	O	SLIMIT
3	O	XVDCS	23	–	VSS	43	O	XROPAS	63	–	VSS
4	O	XCLUT	24	I	IOA19	44	O	XCTROM	64	O	FA
5	O	XRDST	25	I	IOA18	45	O	XDIRAS	65	O	FB
6	I	SW1	26	I	IOA17	46	O	XPS	66	O	FC
7	I	SW0	27	I	IOA14	47	O	XSDR	67	I	F
8	O	DKST	28	I	IOA13	48	O	HDREAD	68	I	XREF
9	O	XEDB	29	I	CA16	49	O	XEA	69	I	XPLREAD
10	O	XRD	30	I	CA15	50	O	SROPF01	70	I	XSPLSD
11	O	XWR	31	I	CA6	51	O	SROPF23	71	I	VY7
12	–	VSS	32	I	CA5	52	–	VSS	72	I	XROM
13	O	XSDEST	33	–	VDD	53	O	SROPF45	73	–	VDD
14	O	SDEST	34	I	CA4	54	O	SROPF67	74	I	XRCLR
15	O	XSSOUR	35	I	CA3	55	O	CKCOMREG	75	I	FBCK
16	O	SSOUR	36	I	CA2	56	O	XSROPM	76	I	XSDREGI
17	O	WAIT	37	I	CA1	57	I	XBUSY	77	O	XSDREGO
18	I	XROPR	38	I	XEXIO	58	I	XRESET	78	O	XSPREG
19	I	IOA23	39	I	RW	59	I	QD	79	O	PS1Q
20	I	IOA22	40	I	XDS	60	O	VY7R	80	O	PS2Q



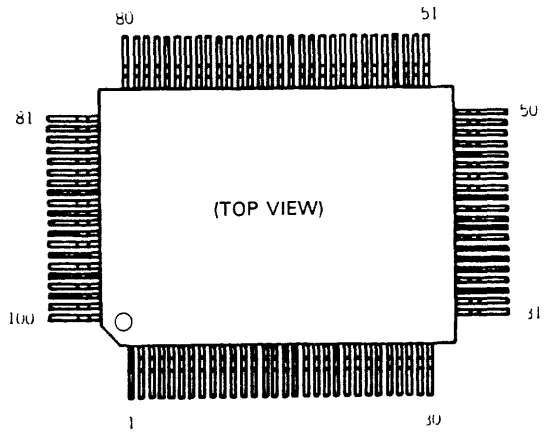
WSC-ICKDMAC (LSI LOGIC)
DMA CONTROLLER



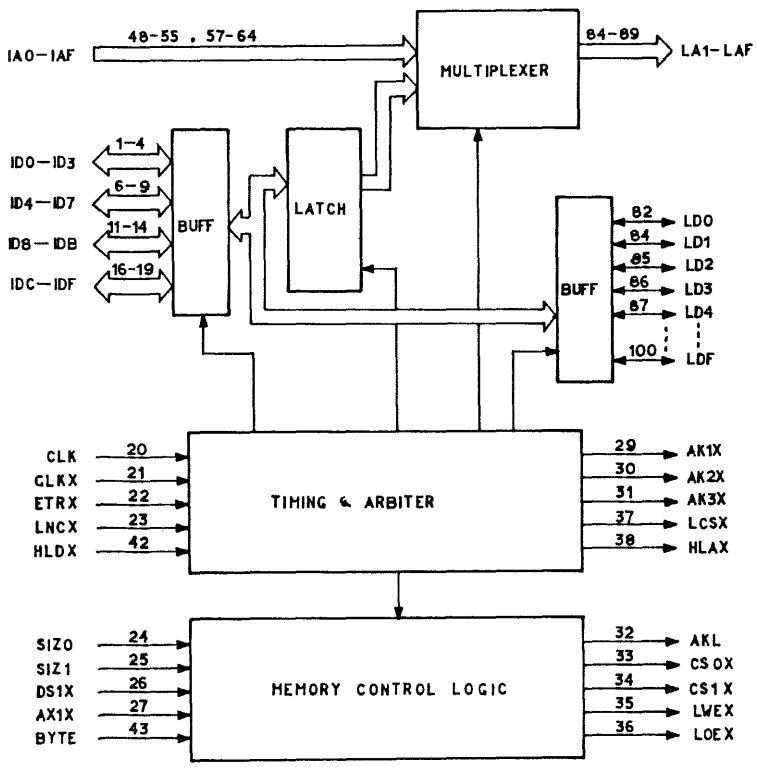
PIN	I/O	PIN NAME	PIN	I/O	PIN NAME	PIN	I/O	PIN NAME
1	-	GND	41	O	WAITOUT	81	I/O	D3
2	I/O	DD7	42	-	N.C.	82	I/O	D2
3	I/O	DD6	43	-	N.C.	83	I/O	D1
4	I/O	DD5	44	-	N.C.	84	I/O	D0
5	I/O	DD4	45	-	GND	85	O	A24
6	I/O	DD3	46	-	VDD	86	O	A19
7	I/O	DD2	47	I/O	D23	87	O	A18
8	I/O	DD1	48	I/O	D22	88	O	A17
9	I/O	DD0	49	I/O	D21	89	O	A16
10	I	REQ	50	I/O	D20	90	-	GND
11	O	ACKX	51	I/O	D19	91	-	VDD
12	I	ECP	52	I/O	D18	92	O	SIZ1
13	I	SYSCLK	53	I/O	D17	93	O	SIZ0
14	-	N.C.	54	I/O	D16	94	I	SEL2
15	-	VDD	55	I	MODX	95	I	SEL1
16	-	GND	56	O	A23	96	I	SEL0
17	I/O	CD7	57	O	A22	97	O	A15
18	I/O	CD6	58	O	A21	98	O	A14
19	I/O	CD5	59	O	A20	99	O	A13
20	I/O	CD4	60	-	GND	100	O	A12
21	I/O	CD3	61	-	VDD	101	O	A11
22	I/O	CD2	62	I/O	D15	102	O	A10
23	I/O	CD1	63	I/O	D14	103	O	A9
24	I/O	CD0	64	I/O	D13	104	O	A8
25	O	IORD	65	I/O	D12	105	-	VDD
26	O	IOWR	66	I/O	D11	106	-	GND
27	-	N.C.	67	I/O	D10	107	O	A25
28	-	N.C.	68	I/O	D9	108	I	CSX
29	I	RESETX	69	I/O	D8	109	O	A26
30	-	VDD	70	I	DSACKINX	110	I	BGX
31	-	GND	71	O	DSACKOUTX	111	O	BRX
32	I/O	D31	72	I	RWIN	112	O	A7
33	I/O	D30	73	I	ASX	113	O	A6
34	I/O	D29	74	O	RWOUT	114	O	A5
35	I/O	D28	75	-	GND	115	O	A4
36	I/O	D27	76	-	VDD	116	O	A3
37	I/O	D26	77	I/O	D7	117	O	A2
38	I/O	D25	78	I/O	D6	118	O	A1
39	I/O	D24	79	I/O	D5	119	O	A0
40	I	WAITINX	80	I/O	D4	120		VDD



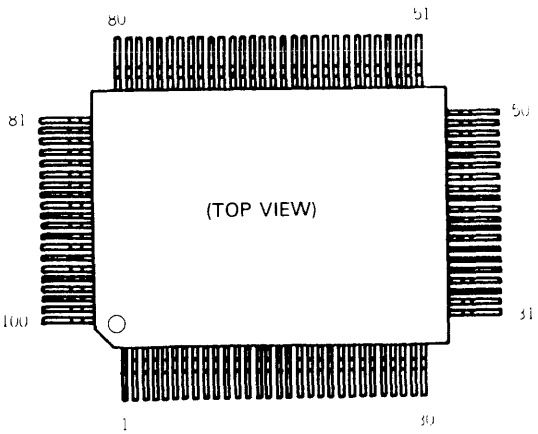
WC-LANCE
MULTIPLEXER, I?O CONTROLLER



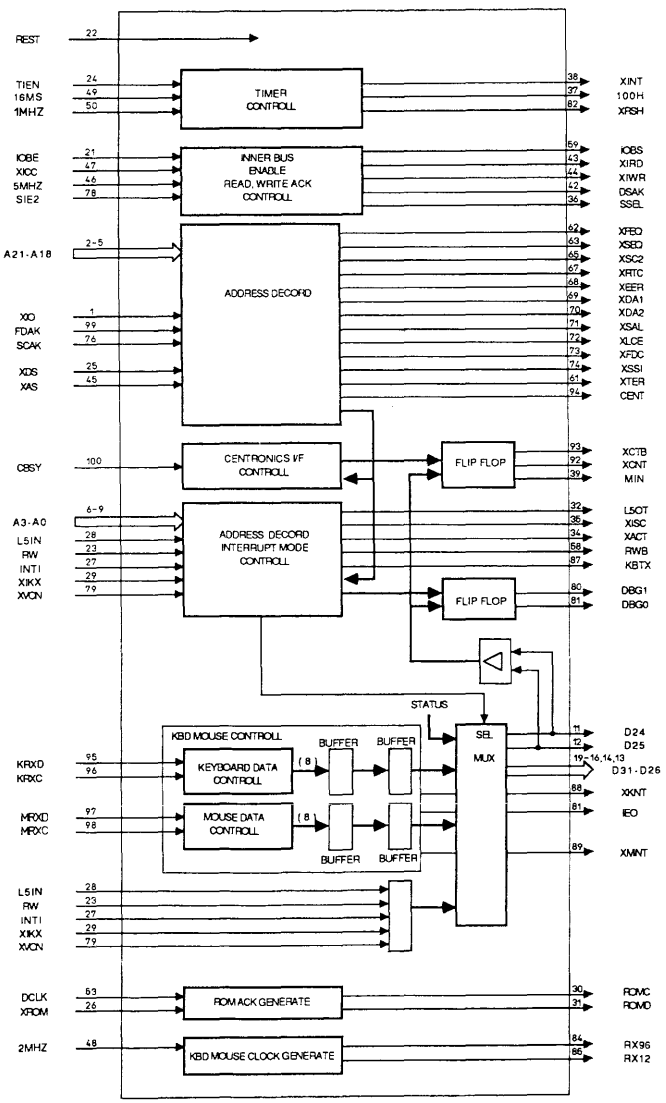
PIN	I/O	PIN NAME	PIN	I/O	PIN NAME	PIN	I/O	PIN NAME
1	I/Ō	ID0	35	Ō	LWEX	69	Ō	LA4
2	I/Ō	ID1	36	Ō	LOEX	70	Ō	LA5
3	I/Ō	ID2	37	Ō	LCSX	71	Ō	LA6
4	I/Ō	ID3	38	Ō	HLAX	72	—	GND
5	—	GND	39	I	ALE	73	Ō	LA7
6	I/Ō	ID4	40	—	GND	74	Ō	LA8
7	I/Ō	ID5	41	—	VDD	75	Ō	LA9
8	I/Ō	ID6	42	I	HLDX	76	Ō	LAA
9	I/Ō	ID7	43	I	BYTE	77	Ō	LAB
10	—	GND	44	I/Ō	DAS	78	Ō	LAC
11	I/Ō	ID8	45	I/Ō	RDY	79	Ō	LAD
12	I/Ō	ID9	46	I/Ō	RDD	80	Ō	LAE
13	I/Ō	IDA	47	I	TEST	81	Ō	LAF
14	I/Ō	IDB	48	I	IA0	82	I/Ō	LD0
15	—	GND	49	I	IA1	83		GND
16	I/Ō	IDC	50	I	IA2	84	I/Ō	LD1
17	I/Ō	IDD	51	I	IA3	85	I/Ō	LD2
18	I/Ō	IDE	52	I	IA4	86	I/Ō	LD3
19	I/Ō	IDF	53	I	IA5	87	I/Ō	LD4
20	I	CLK	54	I	IA6	88	I/Ō	LD5
21	I	CLKX	55	I	IA7	89	I/Ō	LD6
22	I	ETRX	56		VDD	90	—	GND
23	I	LNCX	57	I	IA8	91	—	VDD
24	I	SIZ0	58	I	IA9	92	I/Ō	LD7
25	I	SIZ1	59	I	IAA	93	I/Ō	LD8
26	I	DS1X	60	I	IAB	94	I/Ō	LD9
27	I	AS1X	61	I	IAC	95	I/Ō	LDA
28	I	RWIB	62	I	IAD	96	I/Ō	LDB
29	Ō	AK1X	63	I	IAE	97	I/Ō	LDC
30	Ō	AK2X	64	I	IAF	98	I/Ō	LDD
31	Ō	AK3X	65	Ō	LA1	99	I/Ō	LDE
32	Ō	AKL	66	—	GND	100	I/Ō	LDF
33	Ō	CSOX	67	Ō	LA2			
34	Ō	CS1X	68	Ō	LA3			



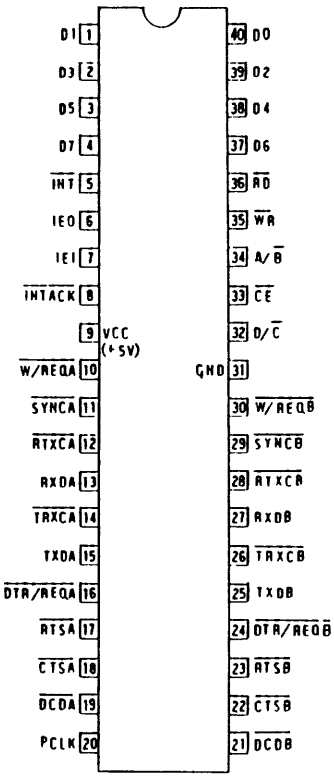
WSC-PARK(NEC)
I/O CONTROLLER

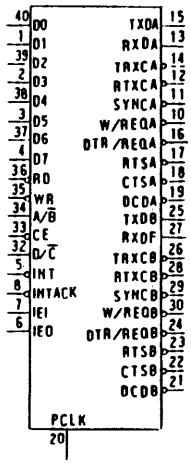


PIN	I/O	PIN NAME	PIN	I/O	PIN NAME	PIN	I/O	PIN NAME
1	I	XO	41	-	VDD	81	O	DBG0
2	I	A21	42	O	DSAK	82	O	XRSH
3	I	A20	43	O	XIRD	83	-	GND
4	I	A19	44	O	XIWR	84	O	RX96
5	I	A18	45	I	XAS	85	O	RX12
6	I	A3	46	I	5MHZ	86	O	IEO
7	I	A2	47	I	XICC	87	O	KBTX
8	I	A1	48	I	2MHZ	88	O	XKNT
9	I	A0	49	I	16MS	89	O	XMNT
10	-	GND	50	I	1MHZ	90	-	GND
11	I/O	D24	51	I	FERQ	91	-	VDD
12	I/O	D25	52	I	DHG	92	O	XCNT
13	O	D26	53	I	DCLK	93	O	XCTB
14	O	D27	54	I	YCBI	94	O	CENT
15	-	GND	55	I	INTH	95	I	KRXD
16	O	D28	56	I	INTL	96	I	KRXC
17	O	D29	57	I	AST	97	I	MRXD
18	O	D30	58	O	RWB	98	I	MRXC
19	O	D31	59	O	IOBS	99	I	FDAK
20	-	VDD	60	-	GND	100	I	CBSY
21	I	IOBE	61	O	XTER			
22	I	REST	62	O	XFED			
23	I	RW	63	O	XSED			
24	I	TIEN	64	O	XSC1			
25	I	XDS	65	O	XSC2			
26	I	XROM	66	-	GND			
27	I	INT1	67	O	XRTC			
28	I	L5IN	68	O	XEER			
29	I	XIKX	69	O	XDA1			
30	O	ROMC	70	O	XDA2			
31	O	ROMD	71	O	XSAL			
32	O	L5OT	72	O	XLCE			
33	-	GND	73	O	XFDC			
34	O	XACT	74	O	XSSI			
35	O	XISC	75	-	GND			
36	O	SSEL	76	I	SCAK			
37	O	100H	77	I	XSBN			
38	O	XINT	78	I	SIE2			
39	I	MIN	79	I	XVCN			
40	-	GND	80	O	DBG1			

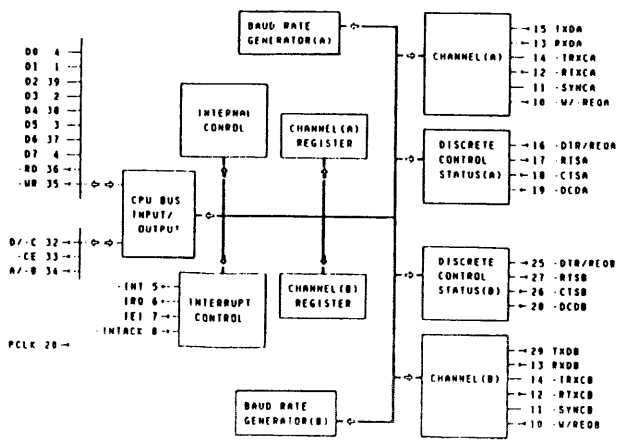


Z0853008PSC
NMOS SIRIAL CONTROLLER
— TOP VIEW —

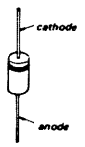




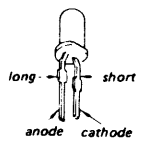
A/-B	;A/B SELECT
CE	;CHIP ENABLE
CTSA,CTSB	;TRANSMIT ENABLE
D/-C	;DATA/CONTROL
D0-D7	;DATA BUS
DCDA,DCDB	;DATA CARRIER DETECT
DTR/REQA,DTR/RECB	;DATA TERMINAL READY/REQUEST
IEI	;INTERRUPT ENABLE INPUT
IEO	;INTERRUPT ENABLE OUTPUT
INT	;INTERRUPT REQUEST
INTACK	;INTERRUPT ACKNOWLEDGE
PCLK	;MASTER CLOCK
RD	;READ
RTSA,RTSB	;TRANSMIT REQUEST
RTXCA,RTXCB	;RECEIVE/TRANSMIT CLOCK
RXDA,RXDB	;RECEIVE DATA
SYNCA,SYNCB	;SYNCHRONOUS
TRXCA,TRXCB	;CHANNEL CLOCK
TXDA,TXDB	;TRANSMIT DATA
W/REQA,W/RECB	;WAIT/REQUEST
WR	;WRITE



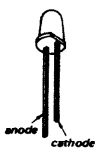
1S2348
1SR139-400



TLR124
TLY124
TLG124A

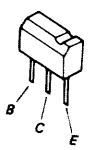


SLR34MC3

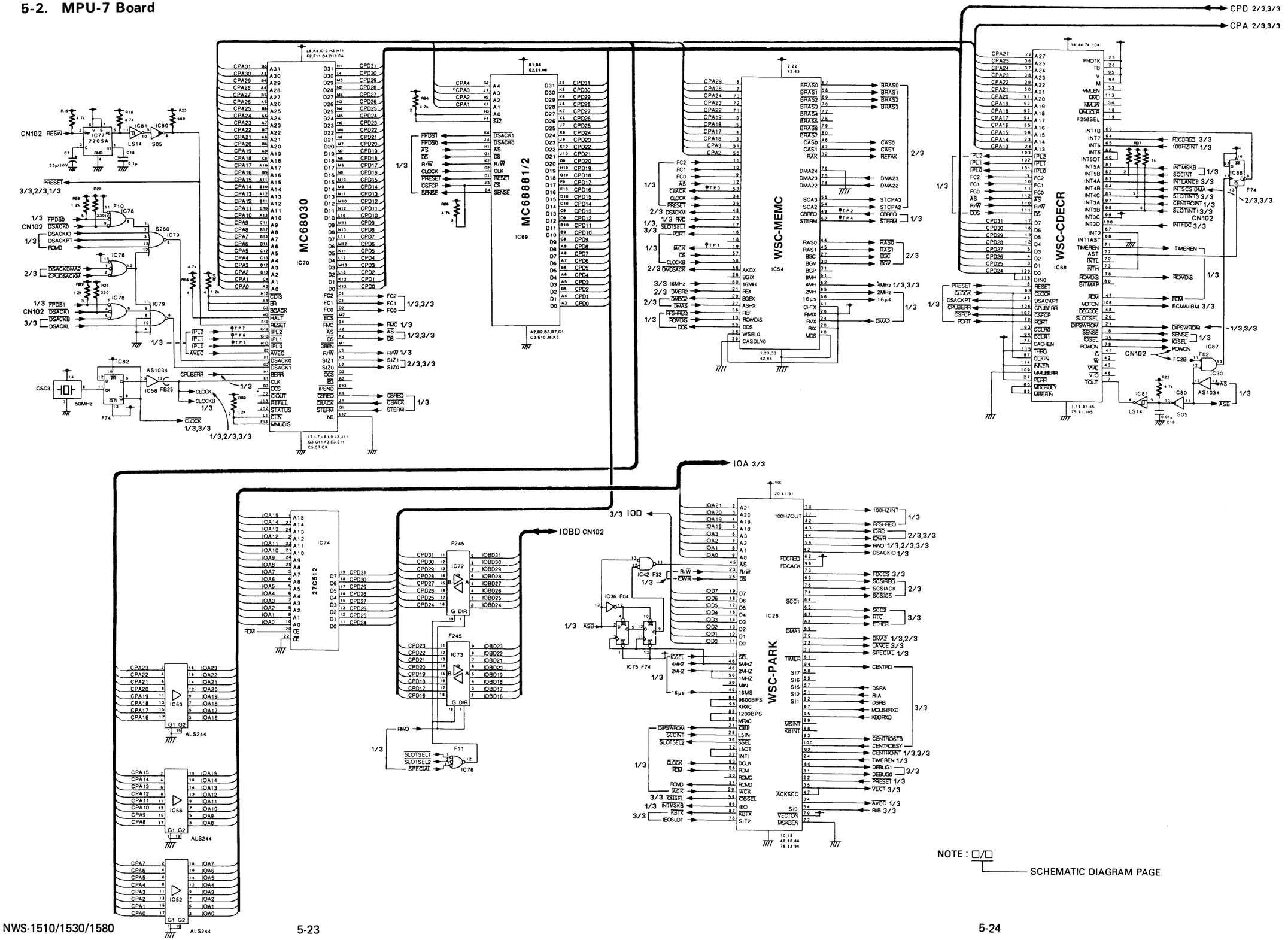


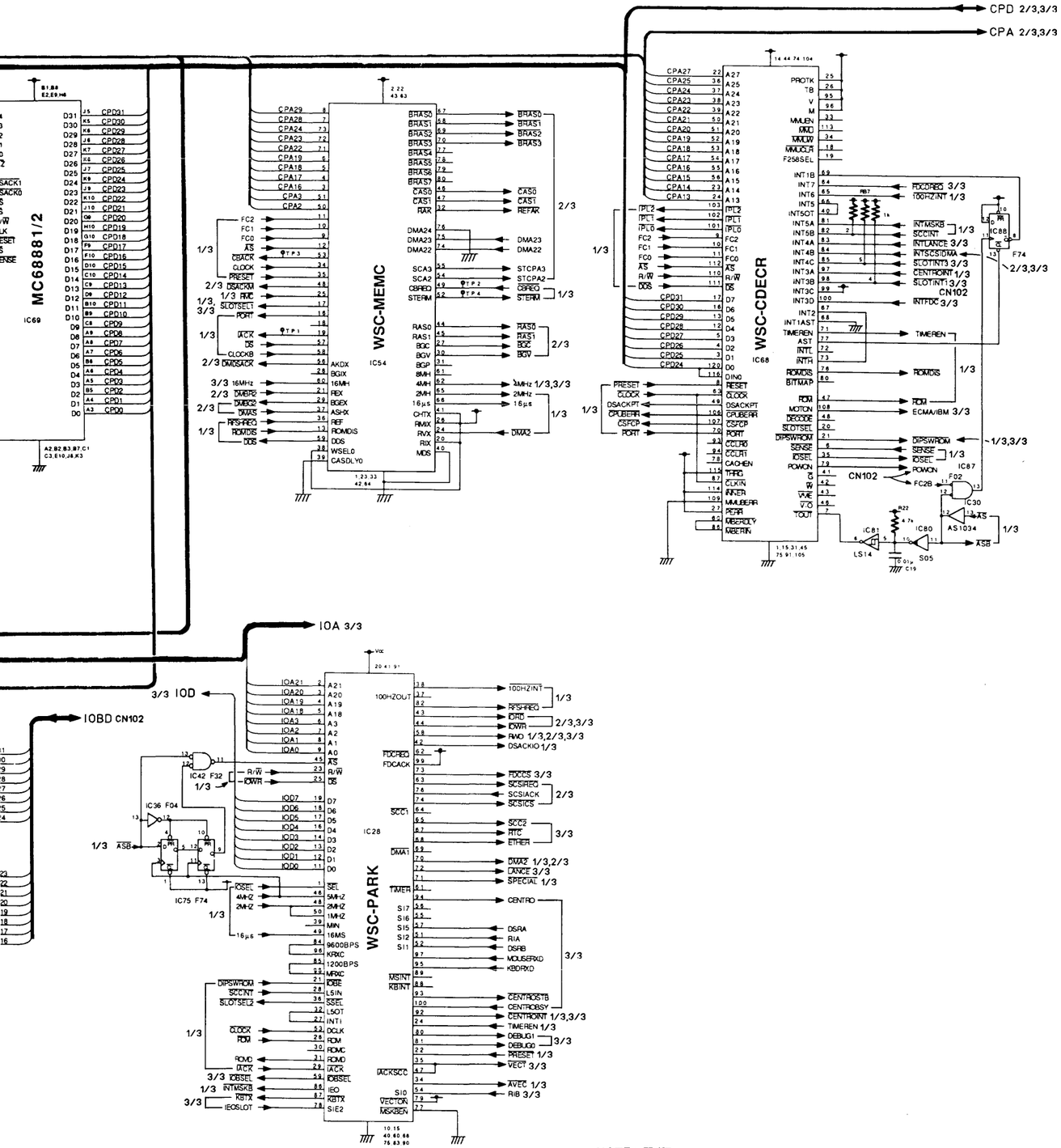
SLR34YC3

DTC114EF



5-2. MPU-7 Board





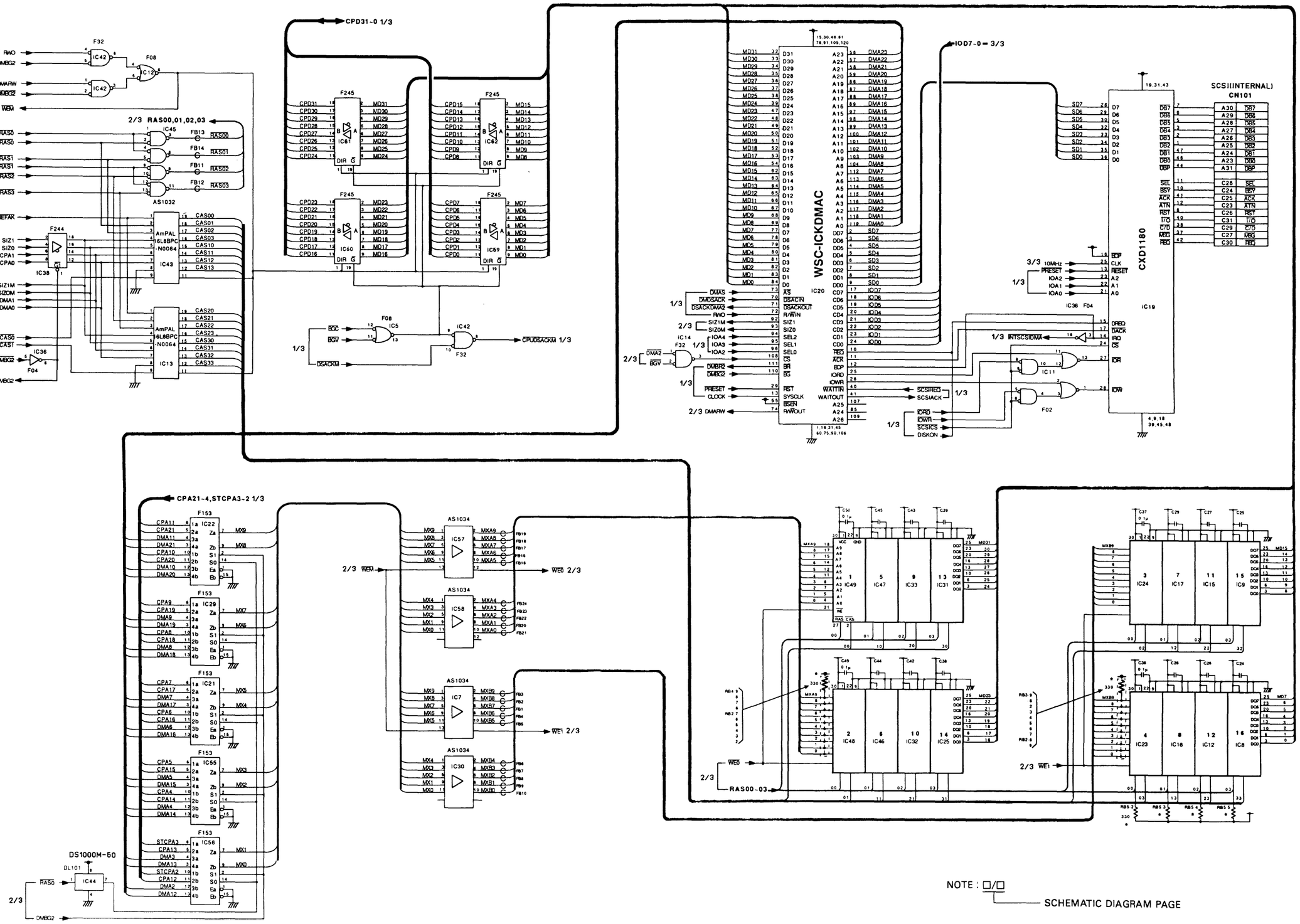
NOTE : □/□
SCHEMATIC DIAGRAM PAGE

REF.NO.	TYPE	PIN NO.	
		+5V	GND
IC30	SN74AS1034AN	14	7
IC36	MC74F04N	14	7
IC42	MC74F32N	14	7
IC52,IC53	SN74ALS244AN	20	10
IC58	SN74AS1034AN	14	7
IC66	SN74ALS244AN	20	10
IC72,IC73	MC74F245N	20	10
IC74	MBM27C512-25	28	14
IC75	MC74F74N	14	7
IC76	MC74F11N	14	7
IC77	TL7705CP-B	8	4
IC78	MC74F10N	14	7
IC79	SN74S260N	14	7
IC80	SN74S05N	14	7
IC81	SN74LS14N	14	7
IC82	MC74F74N	14	7
IC87	MC74F02N	14	7
IC88	MC74F74N	14	7

REF.NO.	TYPE	PIN NO.	
		+5V	GND
IC30	SN74AS1034AN	14	7
IC36	MC74F04N	14	7
IC42	MC74F32N	14	7
IC52,IC53	SN74ALS244AN	20	10
IC58	SN74AS1034AN	14	7
IC66	SN74ALS244AN	20	10
IC72,IC73	MC74F245N	20	10
IC74	MBM27C512-25	28	14
IC75	MC74F74N	14	7
IC76	MC74F11N	14	7
IC77	TL7705CP-B	8	4
IC78	MC74F10N	14	7
IC79	SN74S260N	14	7
IC80	SN74S05N	14	7
IC81	SN74LS14N	14	7
IC82	MC74F74N	14	7
IC87	MC74F02N	14	7
IC88	MC74F74N	14	7

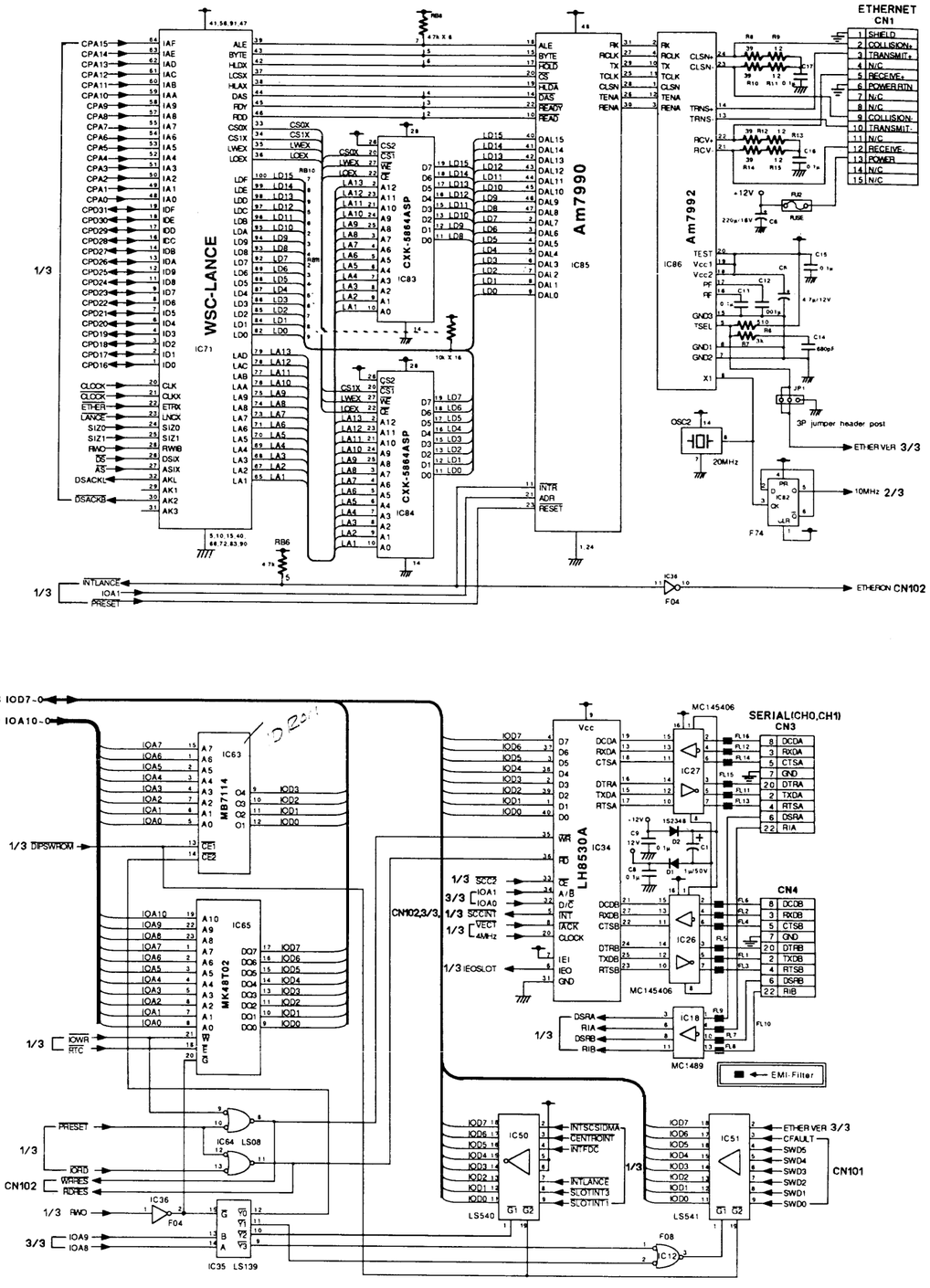
REF.NO.	TYPE	PIN NO.	
		+5V	GND
IC5	MC74F08N	14	7
IC7	SN74AS1034AN	14	7
IC11	MC74F02N	14	7
IC12	MC74F08N	14	7
IC13,IC43	AMPAL-16L8BPC -N0064	20	10
IC14	MC74F32N	14	7
IC21,IC22	MC74F153N	16	8
IC23,IC24	THM81000L-80	1,30	9,22
IC29	MC74F153N	16	8
IC30	SN74AS1034AN	14	7
IC36	MC74F04N	14	7
IC38	MC74F244N	20	10
IC42	MC74F32N	14	7
IC45	SN74AS1032AN	14	7
IC48,IC49	THM81000L-80	1,30	9,22
IC55,IC56	MC74F153N	16	8
IC57,IC58	SN74AS1034AN	14	7
IC59-IC62	MC74245N	20	10

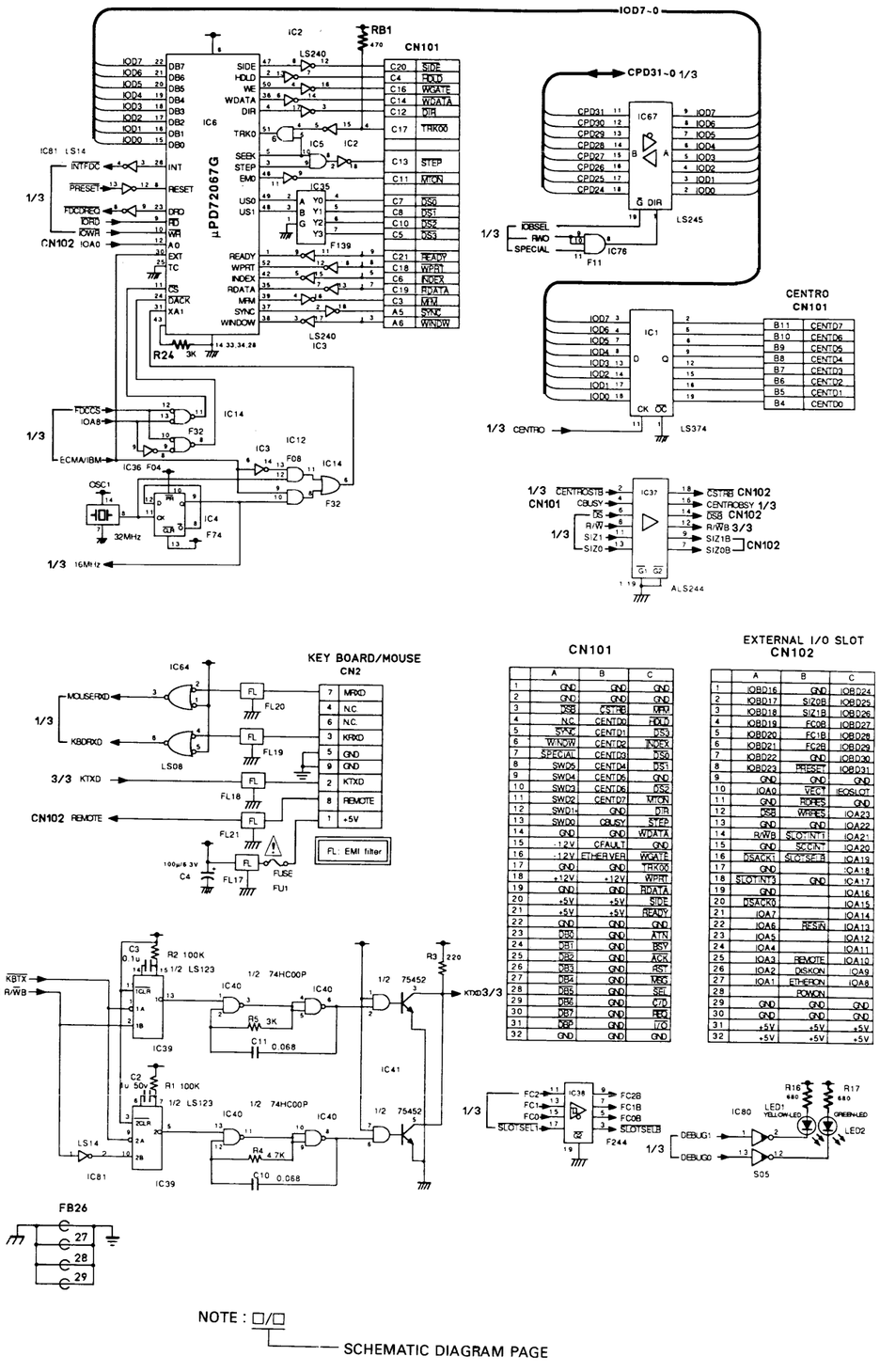
MPU-7(2/3) MPU-7(2/3)



REF.NO.	
IC5	MC7
IC7	SN7
IC11	MC7
IC12	MC7
IC13.IC43	AMP
IC14	MC7
IC21,IC22	MC7
IC23,IC24	THM
IC29	MC7
IC30	SN7
IC36	MC7
IC38	MC7
IC42	MC7
IC45	SN7
IC48,IC49	THM
IC55,IC56	MC7
IC57,IC58	SN7
IC59-IC62	MC7

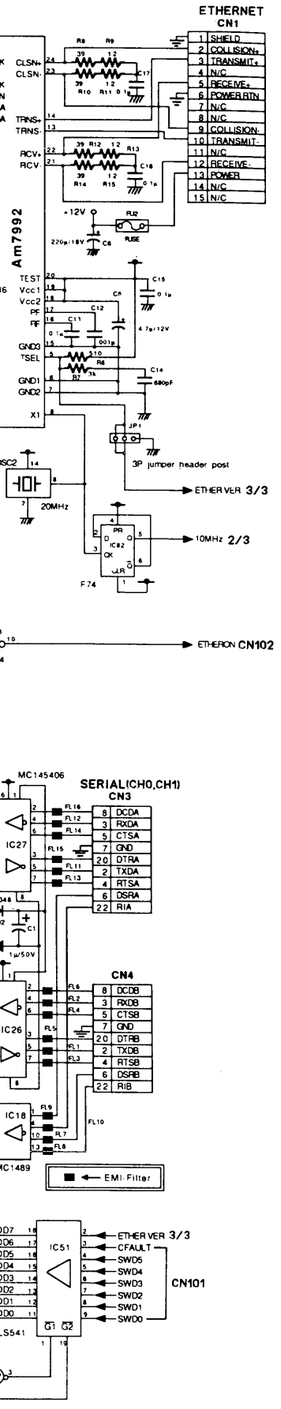
NOTE : □/□
└── SCHEMATIC DIAGRAM PAGE

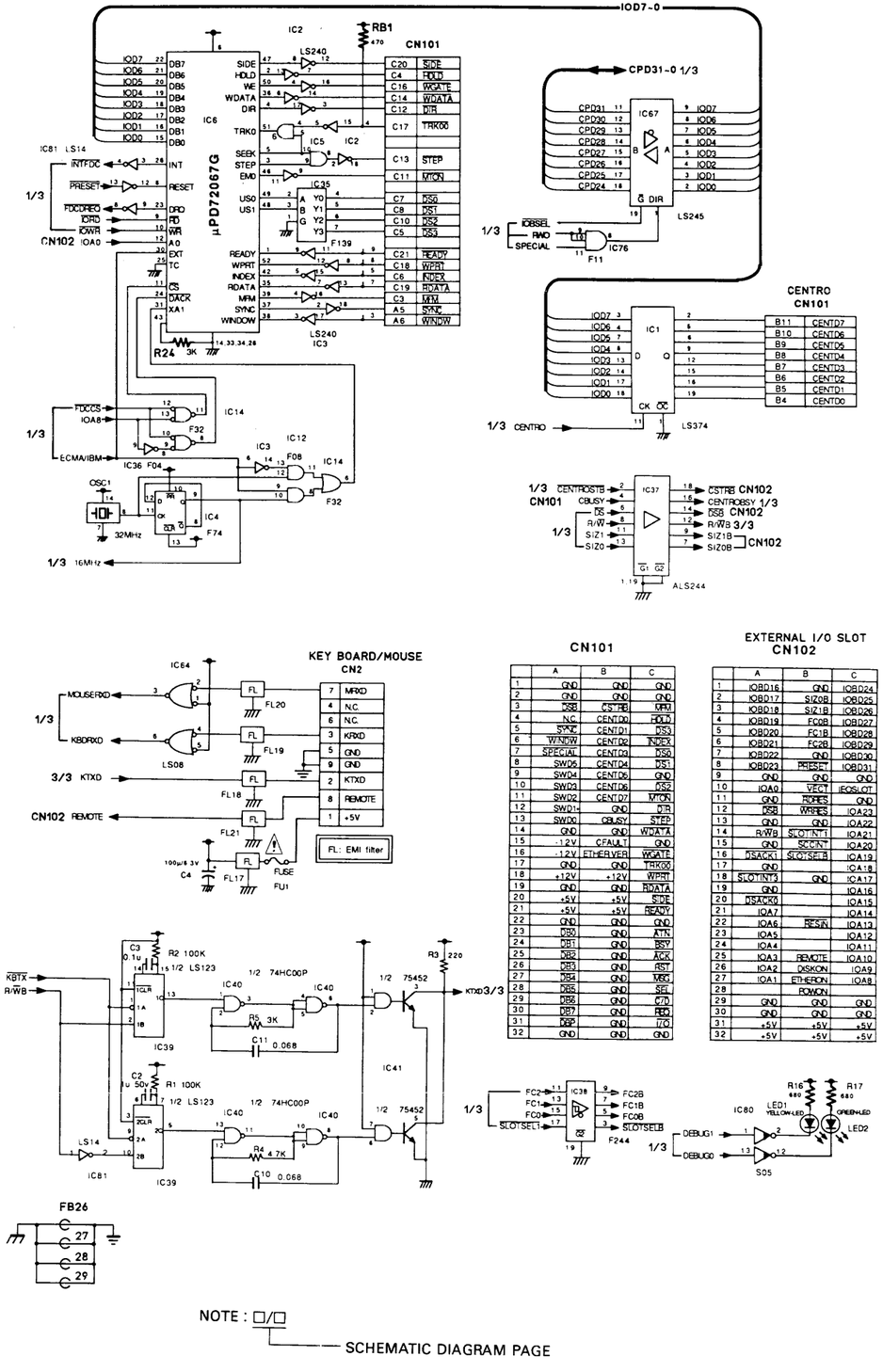




NOTE : □/□ — SCHEMATIC DIAGRAM PAGE

MPU-7(3/3)





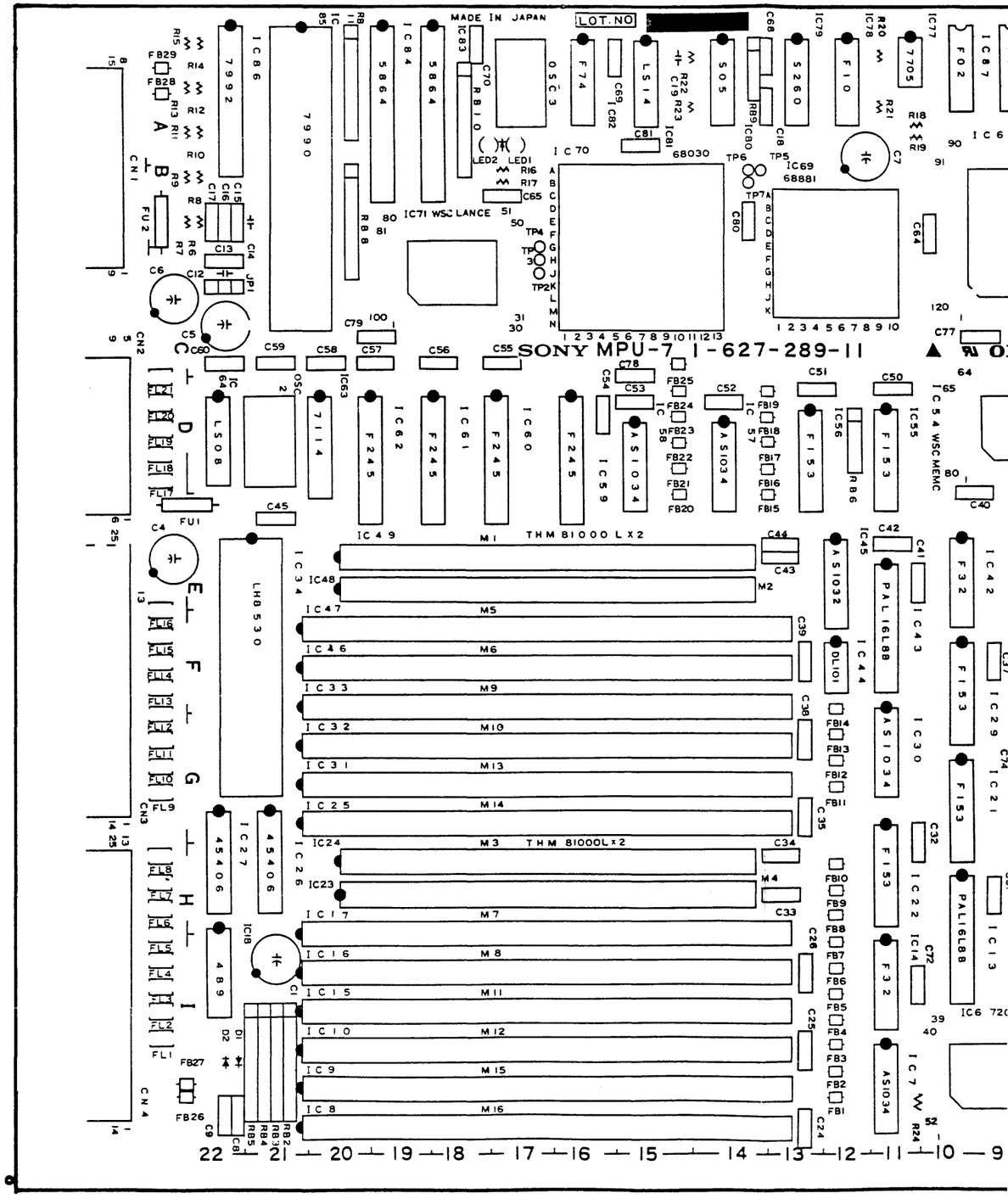
NOTE : □/□

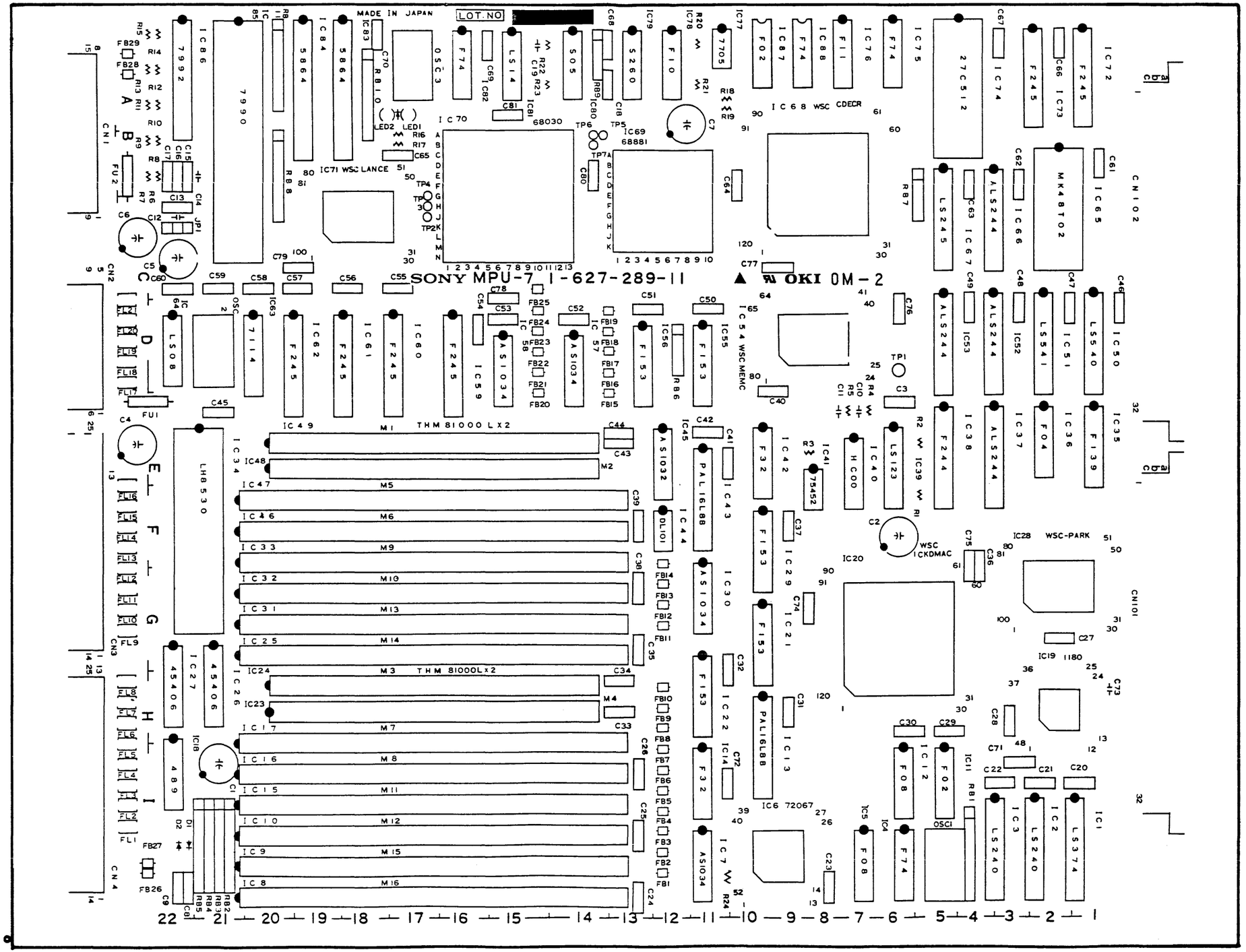
└── SCHEMATIC DIAGRAM PAGE

REF.NO.	TYPE	PIN NO.	
		+5V	GND
IC1	SN74LS374N	20	10
IC2,IC3	SN74LS240N	20	10
IC4	MC74F74N	14	7
IC5,IC12	MC74F08N	14	7
IC14	MC74F32N	14	7
IC18	MC1489AP	14	7
IC26,IC27	MC145406P	16	8
IC35	MC74F139N	16	8
IC36	MC74F04N	14	7
IC37	SN74ALS244AN	20	10
IC38	MC74F244N	20	10
IC39	SN74LS123N	16	8
IC40	SN74HC00N	14	7
IC41	SN75452BP	8	4
IC50	SN74LS540N	20	10
IC51	SN74LS541N	20	10
IC63	MB7114L	16	8
IC64	SN74LS08N	14	7
IC65	MK480T02(B)-25	24	12
IC67	SN74LS245N	20	10
IC80	SN74S05N	14	7
IC81	SN74LS14N	14	7
IC82	MC74F74N	14	7
IC86	AM7992BDC	19,18	6,7,15

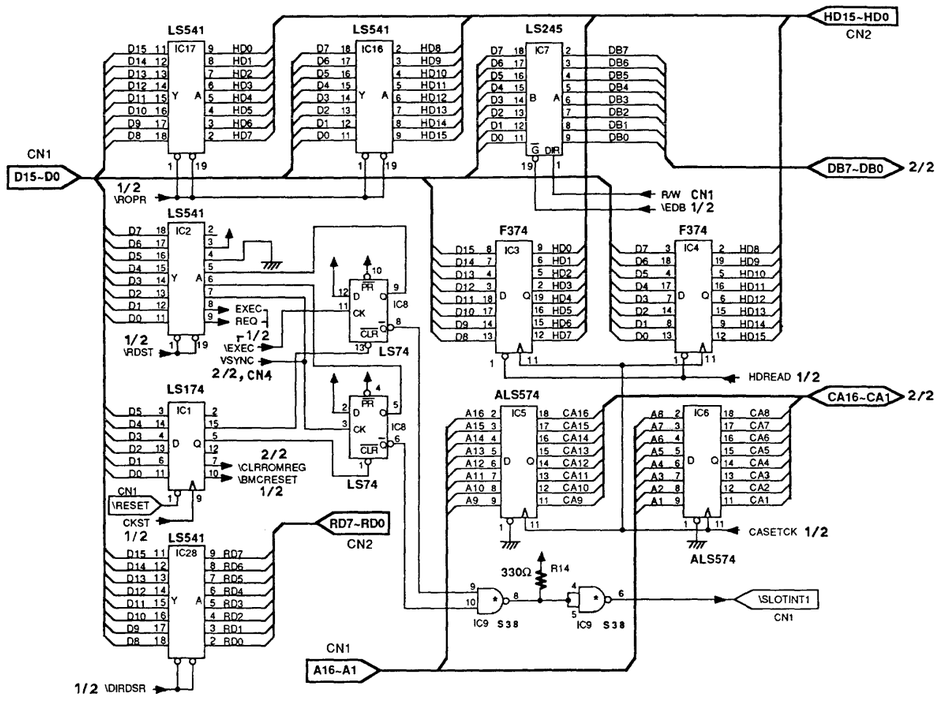
Locations

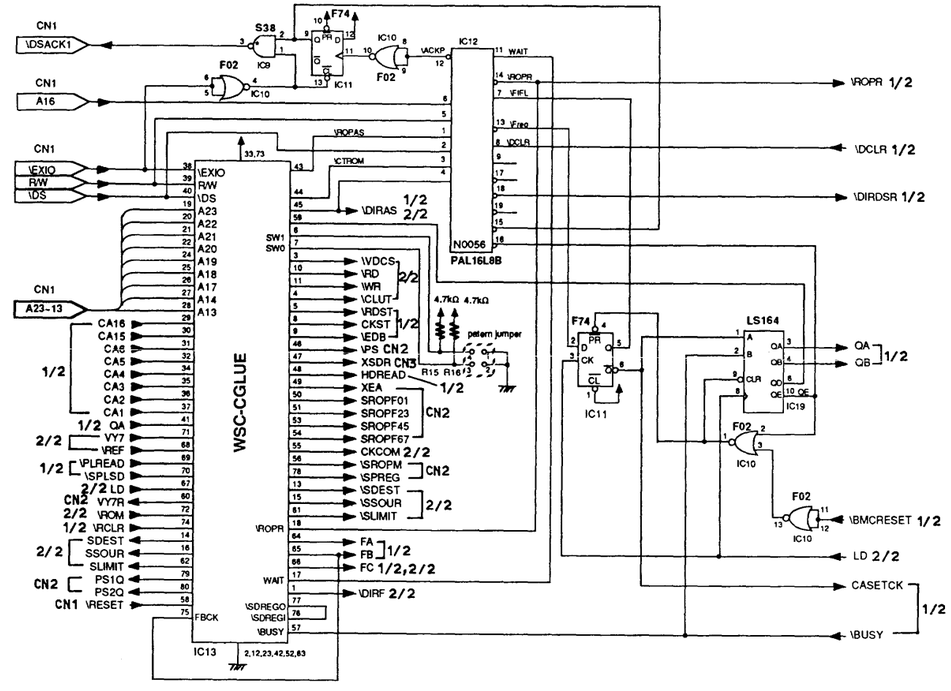
IC1	I-1	IC28	G-2	IC53	D-5	IC73	A-2
IC2	I-2	IC29	F-10	IC54	D-9	IC74	A-4
IC3	I-3	IC30	G-11	IC55	D-11	IC75	A-6
IC4	I-6	IC34	F-21	IC56	D-13	IC76	A-7
IC5	I-7	IC35	E-1	IC57	D-14	IC77	A-11
IC6	I-9	IC36	E-2	IC58	D-15	IC78	A-12
IC7	I-11	IC37	E-3	IC59	D-16	IC79	A-13
IC11	I-5	IC38	E-5	IC60	D-17	IC80	A-14
IC12	I-6	IC39	E-6	IC61	D-19	IC81	A-15
IC13	I-10	IC40	E-7	IC62	D-19	IC82	A-16
IC14	I-11	IC41	E-8	IC63	D-20	IC83	A-18
IC18	I-22	IC42	E-10	IC64	D-22	IC84	A-19
IC19	H-2	IC43	F-11	IC65	C-2	IC85	A-21
IC20	G-6	IC44	F-12	IC66	C-3	IC86	A-22
IC21	G-10	IC45	E-12	IC67	C-5	IC87	A-10
IC22	H-11	IC48	E-17	IC68	B-8	IC88	A-9
IC23	H-17	IC49	E-17	IC69	B-12		
IC24	H-17	IC50	D-1	IC70	B-15		
IC26	H-21	IC51	D-2	IC71	C-18		
IC27	H-22	IC52	D-3	IC72	A-1		

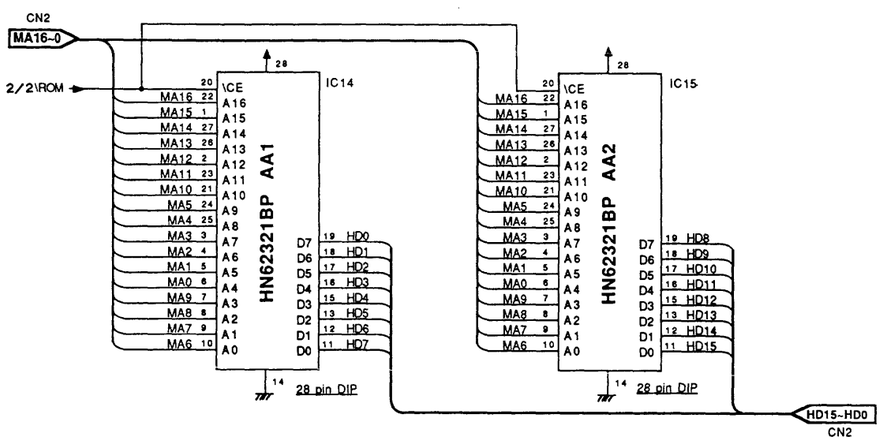



MADE IN JAPAN
LOT.NO
SONY MPU-7 1-627-289-11
OKI OM-2
IC70
68030
IC69
68881
IC71 WSC LANCE
IC68 WSC CDECR
IC54 WSC MEMC
IC20
IC6 72067
IC28 WSC-PARK
WSC ICKDMAC
IC49
THM 81000 LX2
IC24
THM 81000LX2
CN1
CN2
CN3
CN4
CN101
CN102

5 – 3. DSC-008 BOARD(NWS-1530/1580)





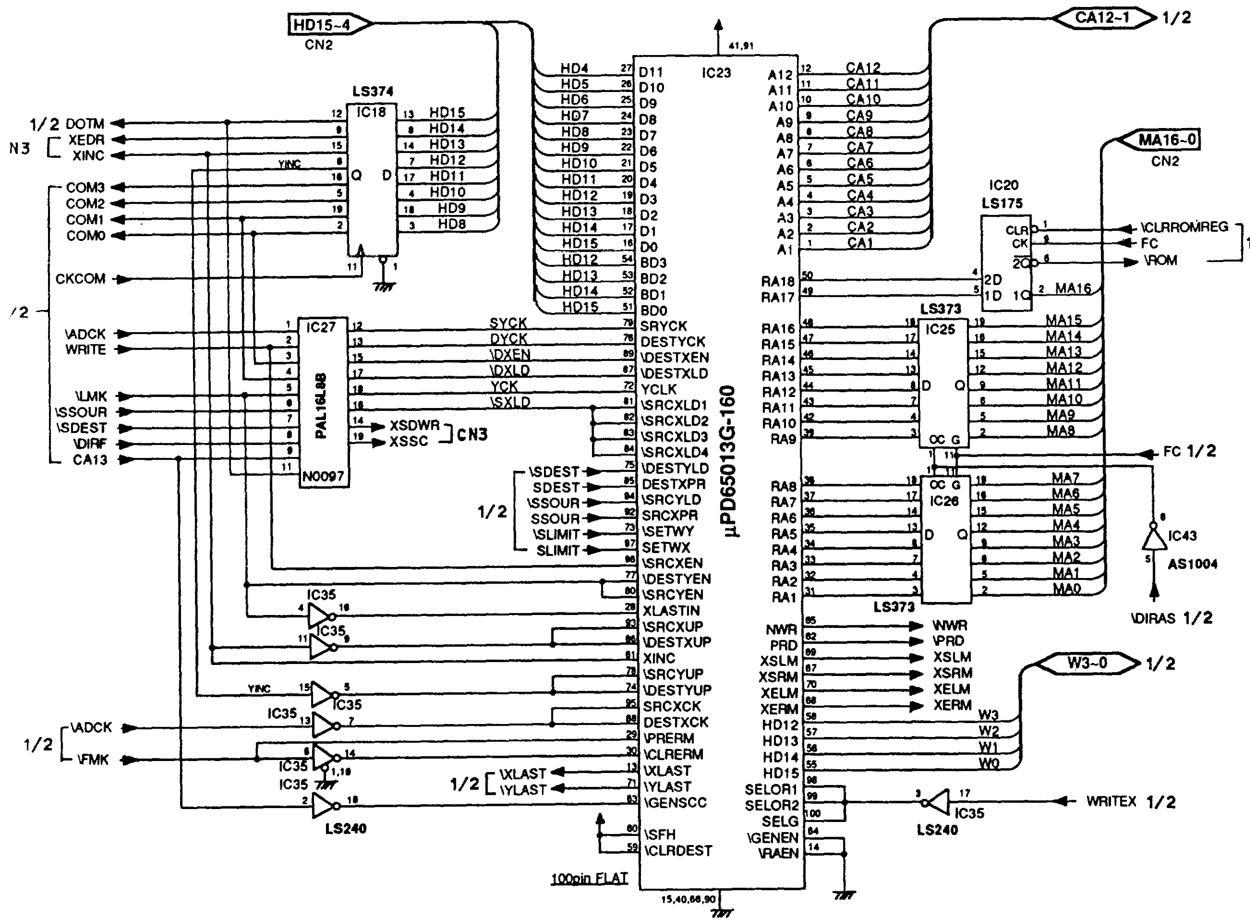


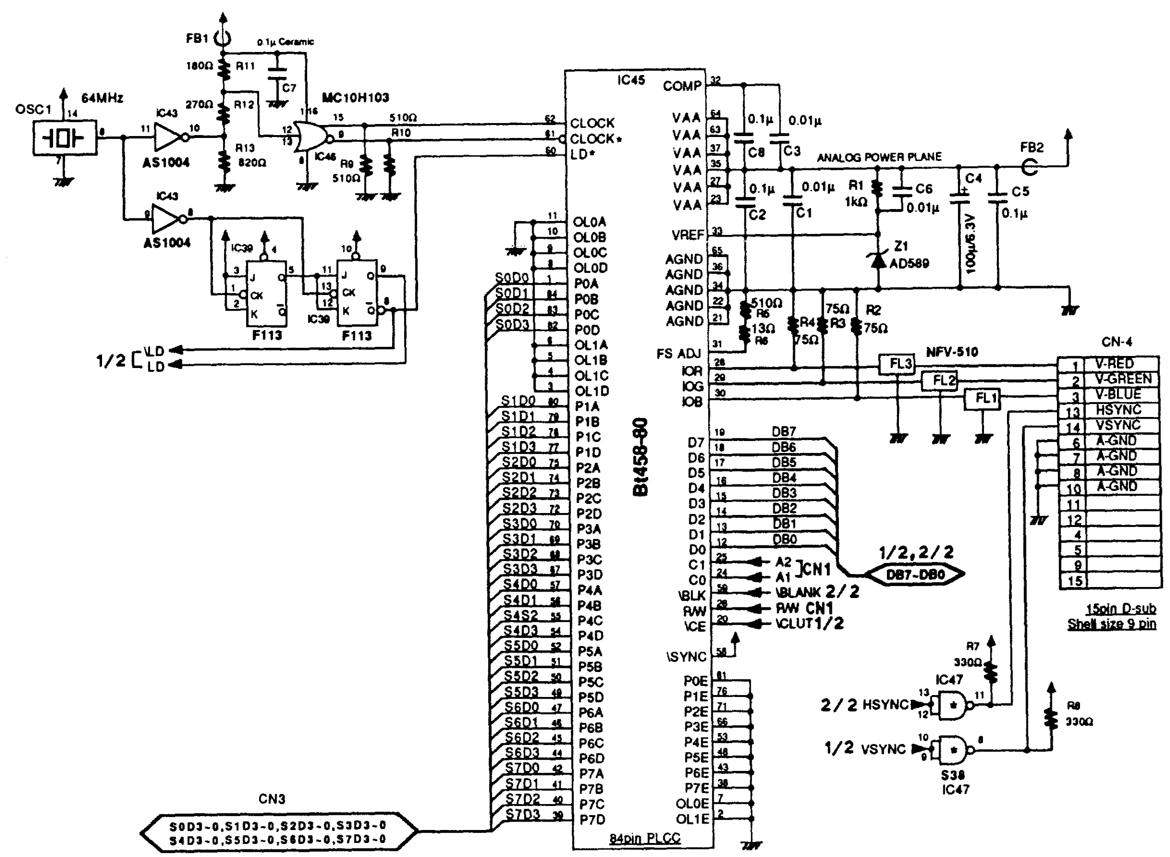
REF.NO.	TYPE	PIN NO.	
		+5V	GND
IC1	SN74LS174N	16	8
IC2	SN74LS541N	20	10
IC3.IC4	MC74F374N	20	10
IC5.IC6	SN74ALS574AN	20	10
IC7	SN74LS245N	20	10
IC8	SN74LS74AN	14	7
IC9	SN74S38N	14	7
IC10	MC74F02N	14	7

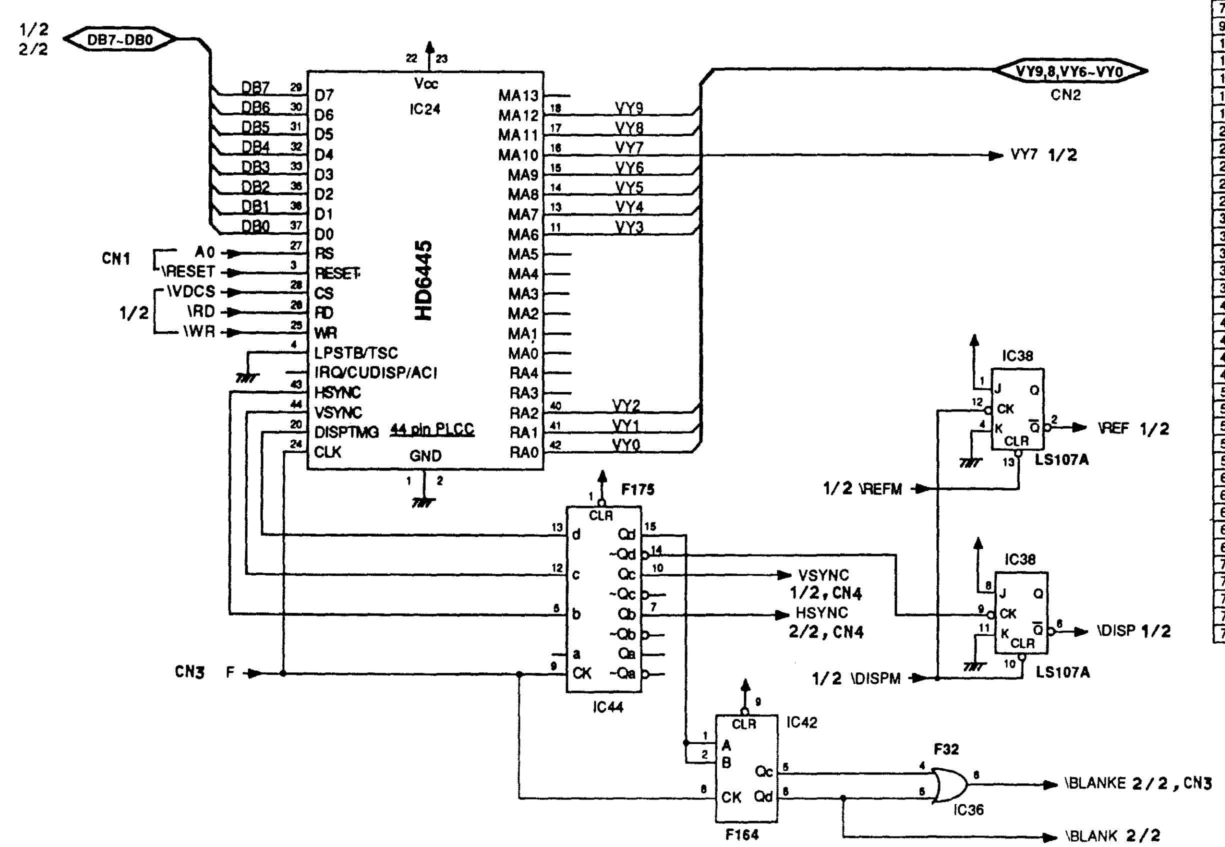
REF.NO.	TYPE	PIN NO.	
		+5V	GND
IC11	MC74F74N	14	7
IC12	AMPAL16L8B	20	10
IC16.IC17	SN74LS541N	20	10
IC19	SN74LS164N	14	7
IC21.IC22	SN74LS541N	20	10
IC28	SN74LS541N	20	10
IC29	SN74LS257BN	16	8
IC30	PAL16R6B	20	10

REF.NO.	TYPE	PIN NO.	
		+5V	GND
IC31	MC74F374N	20	10
IC32	PAL16R6B	20	10
IC33	PAL16L8B	20	10
IC34	PAL16R6B	20	10
IC36	MC74F32N	14	7
IC37	MC74F08N	14	7
IC40.IC41	MC74F74N	14	7
IC43	SN74AS104AN	14	7

NOTE : □／□ SCHEMATIC DIAGRAM PAGE







CN1

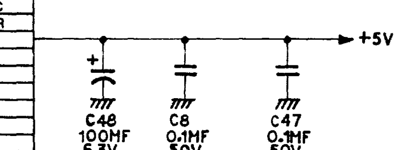
1	GND	2	GND
3	D0	4	D8
5	D1	6	D9
7	D2	8	D10
9	D3	10	D11
11	D4	12	D12
13	D5	14	D13
15	D6	16	D14
17	D7	18	D15
19	GND	20	GND
21	A0	22	A12
23	A1	24	A13
25	A2	26	A14
27	A3	28	A15
29	A4	30	A16
31	A5	32	A17
33	A6	34	A18
35	A7	36	A19
37	A8	38	A20
39	A9	40	A21
41	A10	42	A22
43	A11	44	A23
45	GND	46	GND
47	+5V.	48	+5V
49	\DSACK1	50	\RESET
51	\SLOTINT1	52	\EXIO
53	R/W	54	\DS
55	GND	56	GND
57	+5V	58	+5V
59	+5V	60	+5V
61	+5V	62	+5V
63	+5V	64	+5V
65	+5V	66	+5V
67	GND	68	GND
69	GND	70	GND
71	GND	72	GND
73	GND	74	GND
75	+12V	76	+12V
77	+12V	78	+12V
79	+5V	80	+5V

CN2

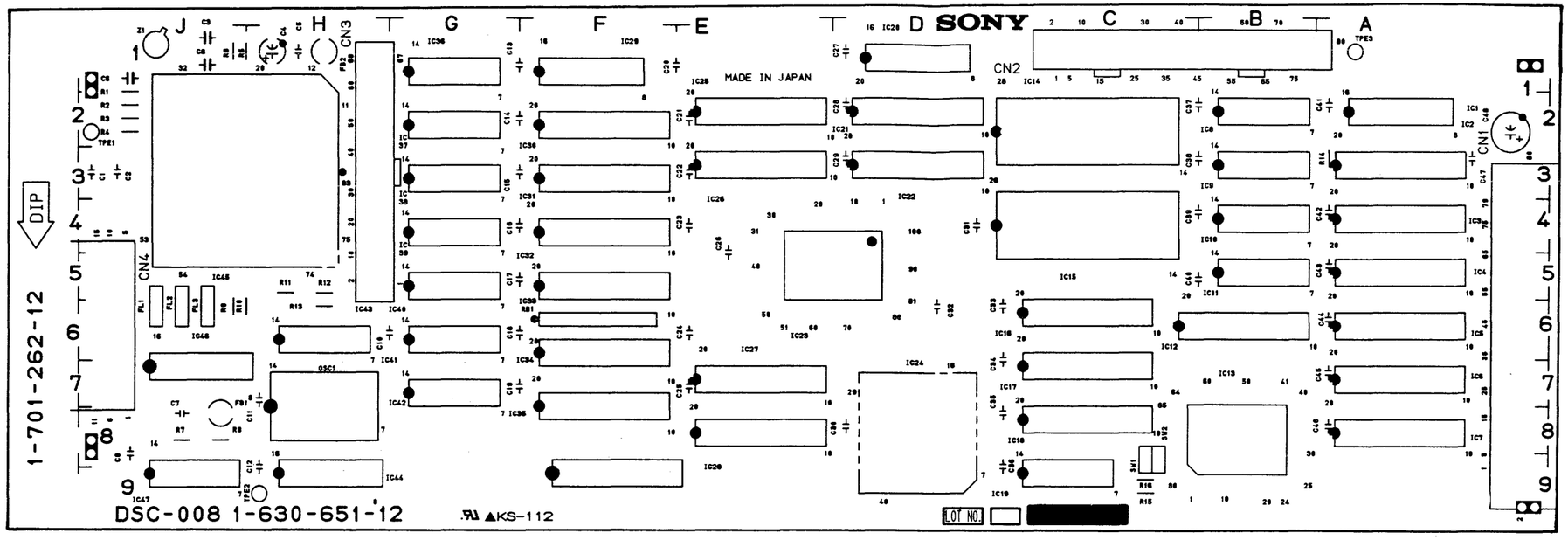
1	MA15	32	HD15
3	MA14	30	HD14
5	MA13	28	HD13
7	MA12	26	HD12
9	MA11	24	HD11
11	MA10	22	HD10
13	MA9	20	HD9
15	MA8	18	HD8
17	MA7	16	HD7
19	MA6	14	HD6
21	MA5	12	HD5
23	MA4	10	HD4
25	MA3	8	HD3
27	MA2	6	HD2
29	MA1	4	HD1
31	MA0	2	HD0
50	VY9	55	\SPREG
52	VY8	41	\DCLR
54	VY7R	57	\SROPM
56	VY6	37	XERM
58	VY5	35	XELM
60	VY4	39	XSRM
62	VY3	33	XSLM
64	VY2	67	XEA
66	VY1	65	SROPF01
68	VY0	63	SROPF23
48	RD7	61	SROPF45
46	RD6	59	SROPF67
44	RD5	53	PS1Q
42	RD4	51	PS2Q
40	RD3	47	\PS
38	RD2		
36	RD1		
34	RD0		
69	VCC	75	GND
70	VCC	76	GND
71	VCC	77	GND
72	VCC	78	GND
73	VCC	79	GND
74	VCC	80	GND

CN3

1	S0D3	25	LD
2	S0D2	43	F
3	S0D1	11	
4	S0D0	35	\BLANKE
6	S1D3	53	WPB3
7	S1D2	51	WPB2
8	S1D1	57	WPB1
9	S1D0	55	WPB0
10	S2D3	33	\ROW/COL
12	S2D2	45	VIDEO
14	S2D1	39	\WEPB
16	S2D0	27	\RAS
18	S3D3	29	\CAS
20	S3D2	41	\OE
22	S3D1	31	CE
24	S3D0	23	XSSR
26	S4D3	49	XSSC
28	S4D2	47	XSDWR
30	S4S1	15	\PLREAD
32	S4D0	13	XSDR
34	S5D3	17	DOTM
36	S5D2	21	XINC
38	S5D1	19	XEDR
40	S5D0	58	VCC
42	S6D3	59	VCC
44	S6D2	60	VCC
46	S6D1	61	VCC
48	S6D0	62	VCC
50	S7D3	63	VCC
52	S7D2	64	GND
54	S7D1	65	GND
56	S7D0	66	GND
		67	GND
		68	GND



REF.NO.	TYPE	PIN NO.	
		+5V	GND
IC18	SN74LS374N	20	10
IC20	SN74LS175N	16	8
IC25	SN74LS373N	20	10
IC26	SN74LS373N	20	10
IC27	PAL16L8B	20	10
IC35	SN74LS240N	20	10
IC36	MC74F32N	14	7
IC38	SN74LS107AN	14	7
IC39	74F113PC	14	7
IC42	74F164PC	14	7
IC43	SN74AS1004AN	14	7
IC44	MC74F175N	16	8
IC46	MC10H103L	16	8
IC47	SN74S38N	14	7



Locations

C1	J-3	C31	D-4	IC1	A-2	IC31	F-3	R11	H-5
C2	J-3	C32	D-6	IC2	A-3	IC32	F-4	R12	H-5
C3	J-1	C33	D-6	IC3	A-4	IC33	F-5	R13	H-6
C4	H-1	C34	D-7	IC4	A-5	IC34	F-6	R14	A-3
C5	H-1	C35	D-8	IC5	A-6	IC35	F-7	R15	C-9
C6	J-1	C36	D-9	IC6	A-7	IC36	G-1	R16	C-9
C7	J-8	C37	C-2	IC7	A-8	IC37	G-2		
C8	J-1	C38	C-3	IC8	B-2	IC38	G-3	RB1	F-6
C9	J-9	C39	C-4	IC9	B-3	IC39	G-4		
C10	H-6	C40	C-5	IC10	B-4	IC40	G-5	Z1	J-1
C11	H-7	C41	A-2	IC11	B-5	IC41	G-6		
C12	H-9	C42	A-4	IC12	B-6	IC42	G-7		
C13	G-1	C43	A-5	IC13	B-8	IC43	H-6		
C14	G-2	C44	A-6	IC14	C-2	IC44	H-9		
C15	G-3	C45	A-7	IC15	C-4	IC45	H-3		
C16	G-4	C46	A-8	IC16	C-6	IC46	J-7		
C17	G-5	C47	A-3	IC17	C-7	IC47	J-9		
C18	G-6	C48	A-2	IC18	C-8				
C19	G-7			IC19	C-9	OSC	H-7		
C20	F-1			IC20	D-1				
C21	E-2	CN1	A-6	IC21	D-2	R1	J-2		
C22	E-3	CN2	C-1	IC22	D-3	R2	J-2		
C23	E-4	CN3	H-3	IC23	D-5	R3	J-2		
C24	E-6	CN4	J-6	IC24	D-7	R4	J-2		
C25	E-7			IC25	E-2	R5	J-1		
C26	E-4	FB1	J-8	IC26	E-3	R6	J-1		
C27	D-1	FB2	H-1	IC27	E-7	R7	J-8		
C28	D-2	FL1	J-6	IC28	E-8	R8	J-8		
C29	D-3	FL2	J-6	IC29	F-1	R9	J-6		
C30	D-8	FL3	J-6	IC30	F-2	R10	J-6		

5-4. MB-5 Board

CN101

	A	B	C
1	GND	GND	GND
2	GND	GND	GND
3	CLOCK1	$\overline{CSTRB}$	$\overline{MFM}$
4	N.C	CENTD0	$\overline{HOLD}$
5	$\overline{SYNC}$	CENTD1	$\overline{DS4}$
6	$\overline{WINDW}$	CENTD2	$\overline{INDEX}$
7	$\overline{SPECIAL}$	CENTD3	$\overline{DS1}$
8	SWD5	CENTD4	$\overline{DS2}$
9	SWD4	CENTD5	GND
10	SWD3	CENTD6	$\overline{DS3}$
11	SWD2	CENTD7	$\overline{MTON}$
12	SWD1	GND	$\overline{DIR}$
13	SWD0	CBUSY	$\overline{STEP}$
14	GND	GND	$\overline{WDATA}$
15	-12V	CFAULT	GND
16	-12V	CLOCK2	$\overline{WGATE}$
17	GND	GND	$\overline{TRK00}$
18	+12V	+12V	$\overline{WPRT}$
19	GND	GND	$\overline{RDATA}$
20	-5V	+5V	$\overline{SIDE}$
21	-5V	+5V	$\overline{READY}$
22	GND	GND	GND
23	$\overline{DB0}$	GND	$\overline{ATN}$
24	$\overline{DB1}$	GND	$\overline{BSY}$
25	$\overline{DB2}$	GND	$\overline{ACK}$
26	$\overline{DB3}$	GND	$\overline{RST}$
27	$\overline{DB4}$	GND	$\overline{MSG}$
28	$\overline{DB5}$	GND	$\overline{SEL}$
29	$\overline{DB6}$	GND	$\overline{C/D}$
30	$\overline{DB7}$	GND	$\overline{REQ}$
31	$\overline{DBP}$	GND	$\overline{I/O}$
32	GND	GND	GND

CN102

	A	B	C
1	10BD16	GND	10BD24
2	10BD17	SIZ0	10BD25
3	10BD18	SIZ1	10BD26
4	10BD19	FC0	10BD27
5	10BD20	FC1	10BD28
6	10BD21	FC2	10BD29
7	10BD22	GND	10BD30
8	10BD23	$\overline{RESET}$	10BD31
9	GND	GND	GND
10	10A0	$\overline{TRCKST0}$	IE0
11	GND	$\overline{RDRES}$	GND
12	$\overline{DS1B}$	$\overline{WARES}$	10A23
13	GND	GND	10A22
14	$\overline{AWIB}$	$\overline{IPIRQ1}$	10A21
15	GND	$\overline{IPIRQ5}$	10A20
16	$\overline{DSACK1}$	$\overline{EXIO}$	10A19
17	GND	N.C.	10A18
18	$\overline{IPIRQ3}$	GND	10A17
19	GND	N.C.	10A16
20	$\overline{DSACK0}$	CLOCK	10A15
21	10A7	N.C.	10A14
22	10A6	$\overline{RESIN}$	10A13
23	10A5	N.C.	10A12
24	10A4	N.C.	10A11
25	10A3	REMOTE	10A10
26	10A2	DISKON	10A9
27	10A1	ETHERON	10A8
28	N.C.	POWOFF	N.C.
29	GND	GND	GND
30	GND	GND	GND
31	+5V	-5V	-5V
32	+5V	-5V	-5V

CN103

	A	B	C
1	10BD16	GND	10BD24
2	10BD17	SIZ0	10BD25
3	10BD18	SIZ1	10BD26
4	10BD19	FC0	10BD27
5	10BD20	FC1	10BD28
6	10BD21	FC2	10BD29
7	10BD22	GND	10BD30
8	10BD23	$\overline{RESET}$	10BD31
9	GND	GND	GND
10	10A0	$\overline{TRCKST0}$	IE0
11	GND	$\overline{RDRES}$	GND
12	$\overline{DS1B}$	$\overline{WARES}$	10A23
13	GND	GND	10A22
14	$\overline{AWIB}$	$\overline{IPIRQ1}$	10A21
15	GND	$\overline{IPIRQ5}$	10A20
16	$\overline{DSACK1}$	$\overline{EXIO}$	10A19
17	GND	N.C.	10A18
18	$\overline{IPIRQ3}$	GND	10A17
19	GND	N.C.	10A16
20	$\overline{DSACK0}$	N.C.	10A15
21	10A7	N.C.	10A14
22	10A6	N.C.	10A13
23	10A5	N.C.	10A12
24	10A4	N.C.	10A11
25	10A3	N.C.	10A10
26	10A2	N.C.	10A9
27	10A1	N.C.	10A8
28	-12V	N.C.	-12V
29	GND	GND	GND
30	GND	GND	GND
31	+5V	+5V	+5V
32	+5V	+5V	+5V

CN104

1	GND	2	GND
3	10BD16	4	10BD24
5	10BD17	6	10BD25
7	10BD18	8	10BD26
9	10BD19	10	10BD27
11	10BD20	12	10BD28
13	10BD21	14	10BD29
15	10BD22	16	10BD30
17	10BD23	18	10BD31
19	GND	20	GND
21	10A0	22	10A12
23	10A1	24	10A13
25	10A2	26	10A14
27	10A3	28	10A15
29	10A4	30	10A16
31	10A5	32	10A17
33	10A6	34	10A18
35	10A7	36	10A19
37	10A8	38	10A20
39	10A9	40	10A21
41	10A10	42	10A22
43	10A11	44	10A23
45	GND	46	GND
47	+5V	48	+5V
49	$\overline{DSACK1}$	50	$\overline{RESET}$
51	$\overline{IPIRQ1}$	52	$\overline{EXIO}$
53	$\overline{AWIB}$	54	$\overline{DS1B}$
55	GND	56	GND
57	+5V	58	+5V
59	+5V	60	+5V
61	+5V	62	+5V
63	+5V	64	+5V
65	+5V	66	+5V
67	GND	68	GND
69	GND	70	GND
71	GND	72	GND
73	GND	74	GND
75	+12V	76	+12V
77	+12V	78	+12V
79	+5V	80	+5V

CN201

1	GND	2	$\overline{DB0}$
3	GND	4	$\overline{DB1}$
5	GND	6	$\overline{DB2}$
7	GND	8	$\overline{DB3}$
9	GND	10	$\overline{DB4}$
11	GND	12	$\overline{DB5}$
13	GND	14	$\overline{DB6}$
15	GND	16	$\overline{DB7}$
17	GND	18	$\overline{DBP}$
19	GND	20	GND
21	GND	22	GND
23	GND	24	GND
25	N.C.	26	+5UF
27	GND	28	GND
29	GND	30	GND
31	GND	32	$\overline{ATN}$
33	GND	34	GND
35	GND	36	$\overline{BSY}$
37	GND	38	$\overline{ACK}$
39	GND	40	$\overline{RST}$
41	GND	42	$\overline{MSG}$
43	GND	44	$\overline{SEL}$
45	GND	46	$\overline{C/D}$
47	GND	48	$\overline{REQ}$
49	GND	50	$\overline{I/O}$

CN202

1	GND	2	$\overline{DB0}$
3	GND	4	$\overline{DB1}$
5	GND	6	$\overline{DB2}$
7	GND	8	$\overline{DB3}$
9	GND	10	$\overline{DB4}$
11	GND	12	$\overline{DB5}$
13	GND	14	$\overline{DB6}$
15	GND	16	$\overline{DB7}$
17	GND	18	$\overline{DBP}$
19	GND	20	GND
21	GND	22	GND
23	GND	24	GND
25	N.C.	26	+5UF
27	GND	28	GND
29	GND	30	GND
31	GND	32	$\overline{ATN}$
33	GND	34	GND
35	GND	36	$\overline{BSY}$
37	GND	38	$\overline{ACK}$
39	GND	40	$\overline{RST}$
41	GND	42	$\overline{MSG}$
43	GND	44	$\overline{SEL}$
45	GND	46	$\overline{C/D}$
47	GND	48	$\overline{REQ}$
49	GND	50	$\overline{I/O}$

FUSE 125V2A 1SR139-400

CN301

1	N.C.	2	
3	EMS	4	$\overline{HOLD}$
5	EMS	6	$\overline{DS4}$
7	EMS	8	$\overline{INDEX}$
9	EMS	10	$\overline{DS1}$
11	EMS	12	$\overline{DS2}$
13	GND	14	$\overline{DS3}$
15	GND	16	$\overline{MTON}$
17	GND	18	$\overline{DIR}$
19	GND	20	$\overline{STEP}$
21	GND	22	$\overline{WDATA}$
23	GND	24	$\overline{WGATE}$
25	GND	26	$\overline{TRK00}$
27	GND	28	$\overline{WPRT}$
29	EM12	30	$\overline{RDATA}$
31	EM12	32	$\overline{SIDE}$
33	EM12	34	$\overline{READY}$

J1 +5V +12V 47uF/16V 47uF/16V GND

CN302

1	$\overline{WINDW}$	2	GND
3	$\overline{MFM}$	4	GND
5	$\overline{FDATA}$	6	GND
7	$\overline{SPRT}$	8	GND
9	$\overline{TRK00}$	10	GND
11	$\overline{WDATE}$	12	GND
13	$\overline{WDATA}$	14	GND
15	$\overline{STEP}$	16	GND
17	$\overline{DIR}$	18	GND
19	$\overline{DS4}$	20	GND
21	$\overline{DS3}$	22	GND
23	$\overline{DS2}$	24	GND
25	$\overline{DS1}$	26	GND
27	$\overline{SYNC}$	28	GND
29	$\overline{READY}$	30	GND
31	$\overline{INDEX}$	32	GND
33	$\overline{HOLD}$	34	GND
35	N.C.	36	GND
37	$\overline{SIDE}$	38	GND
39	N.C.	40	GND
41	N.C.	42	GND
43	$\overline{MTON}$	44	GND
45	N.C.	46	GND
47	N.C.	48	GND
49	N.C.	50	GND

CN401

1	$\overline{CSTRB}$	2	CENTD6
3	CENTD0	4	CENTD7
5	CENTD1	6	N.C.
7	CENTD2	8	CBUSY
9	CENTD3	10	N.C.
11	CENTD4	12	CFAULT
13	CENTD5	14	GND

CN501

1	N.C	2	N.C.
3	SWD5	4	ETHERON
5	DISKON	6	POWOFF
7	RESIN	8	+5U
9	GND	10	REMOTE
11	SWD4	12	SWD3
13	SWD2	14	SWD1
15	SWD0	16	GND
17	CENTD0	18	CENTD4
19	CENTD1	20	CENTD5
21	CENTD2	22	CENTD6
23	CENTD3	24	CENTD7
25		26	

CN601

1	GND	2	GND
3	10BD24	4	CLOCK1
5	10BD25	6	CLOCK2
7	10BD26	8	N.C.
9	10BD27	10	N.C.
11	10BD28	12	N.C.
13	10BD29	14	N.C.
15	10BD30	16	N.C.
17	10BD31	18	GND
19	GND	20	+5U
21	10A0	22	+5U
23	10A1	24	+5U
25	10A2	26	+5U
27	GND	28	GND
29	$\overline{IPIRQ1}$	30	+12U
31	$\overline{DSACK0}$	32	+12U
33	$\overline{RESET}$	34	-12U
35	$\overline{SPECIAL}$	36	GND
37	N.C.	38	$\overline{AWIB}$
39	GND	40	GND

CN602

1	+5U
2	+5U
3	+5U
4	GND
5	GND
6	GND
7	+12U
8	+12U
9	-12U
10	REMOTE

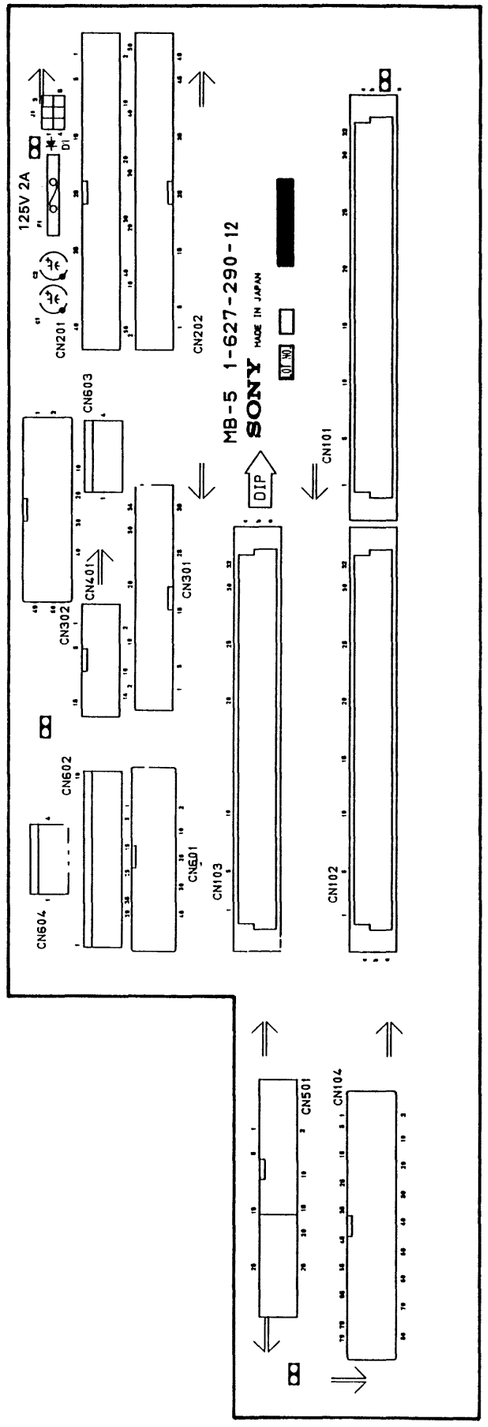
CN603

1	+12U
2	GND
3	GND
4	+5U

CN604

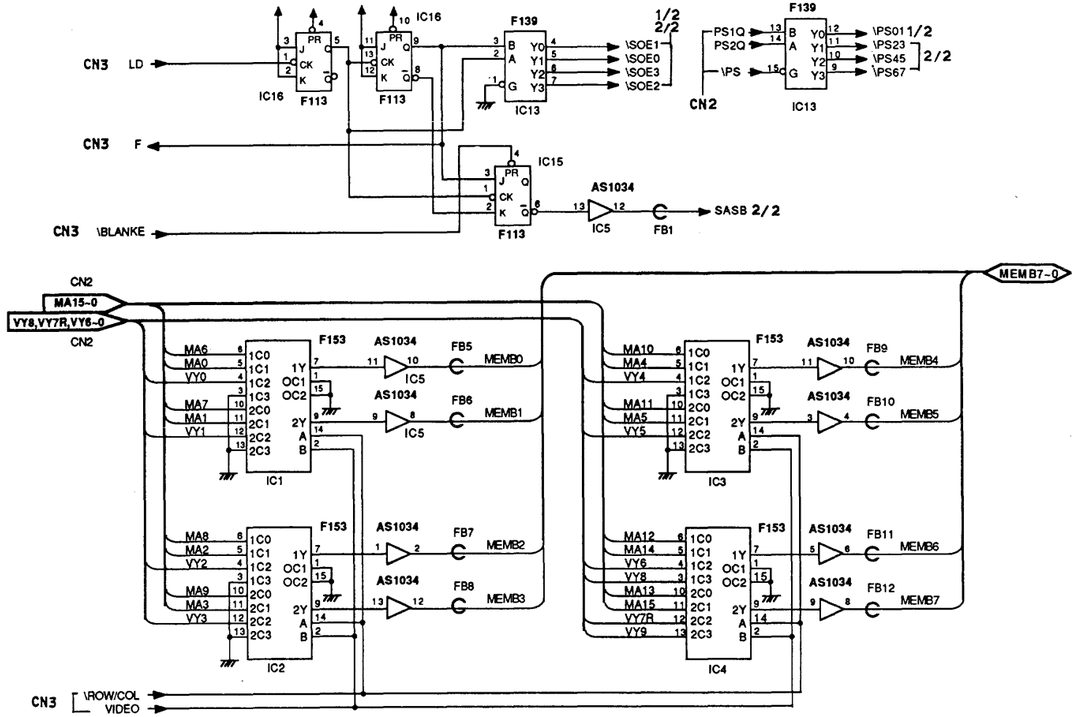
1	+12U
2	GND
3	GND
4	+5U

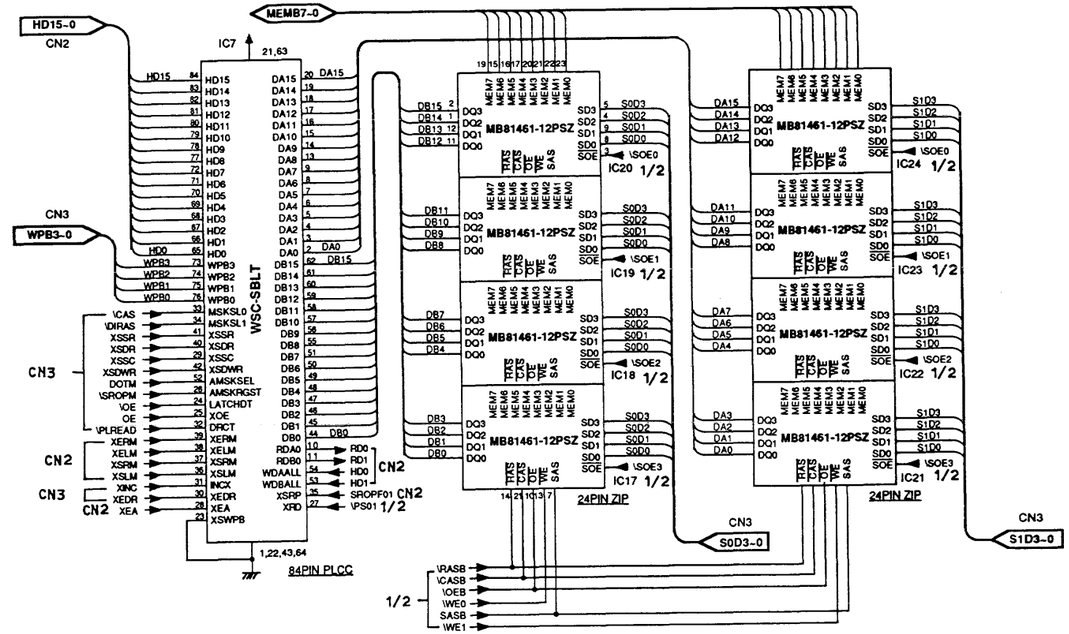
Note: The components identified by mark ⚠ or dotted line with mark ⚠ are critical for safety. Replace only with part number specified.

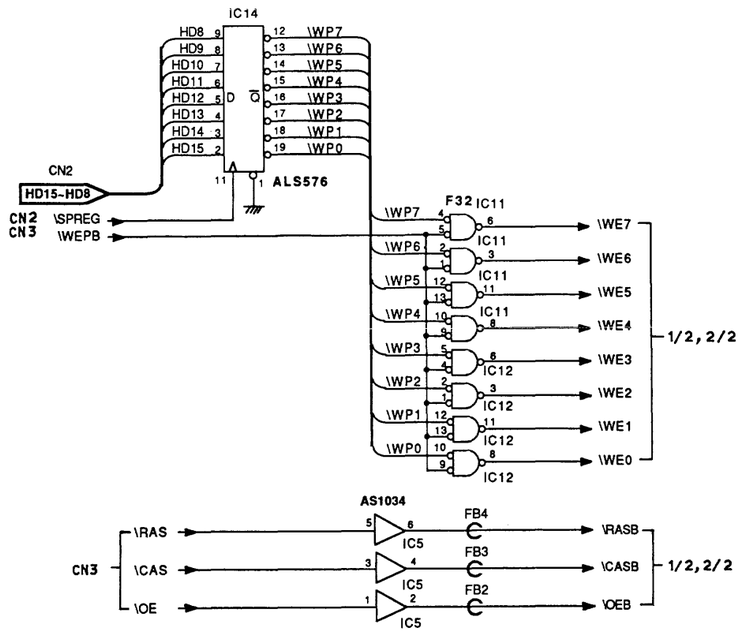


NOTE : □/□ — SCHEMATIC DIAGRAM PAGE

5 – 5. EM-6 BOARD(NWS-1530/1580)



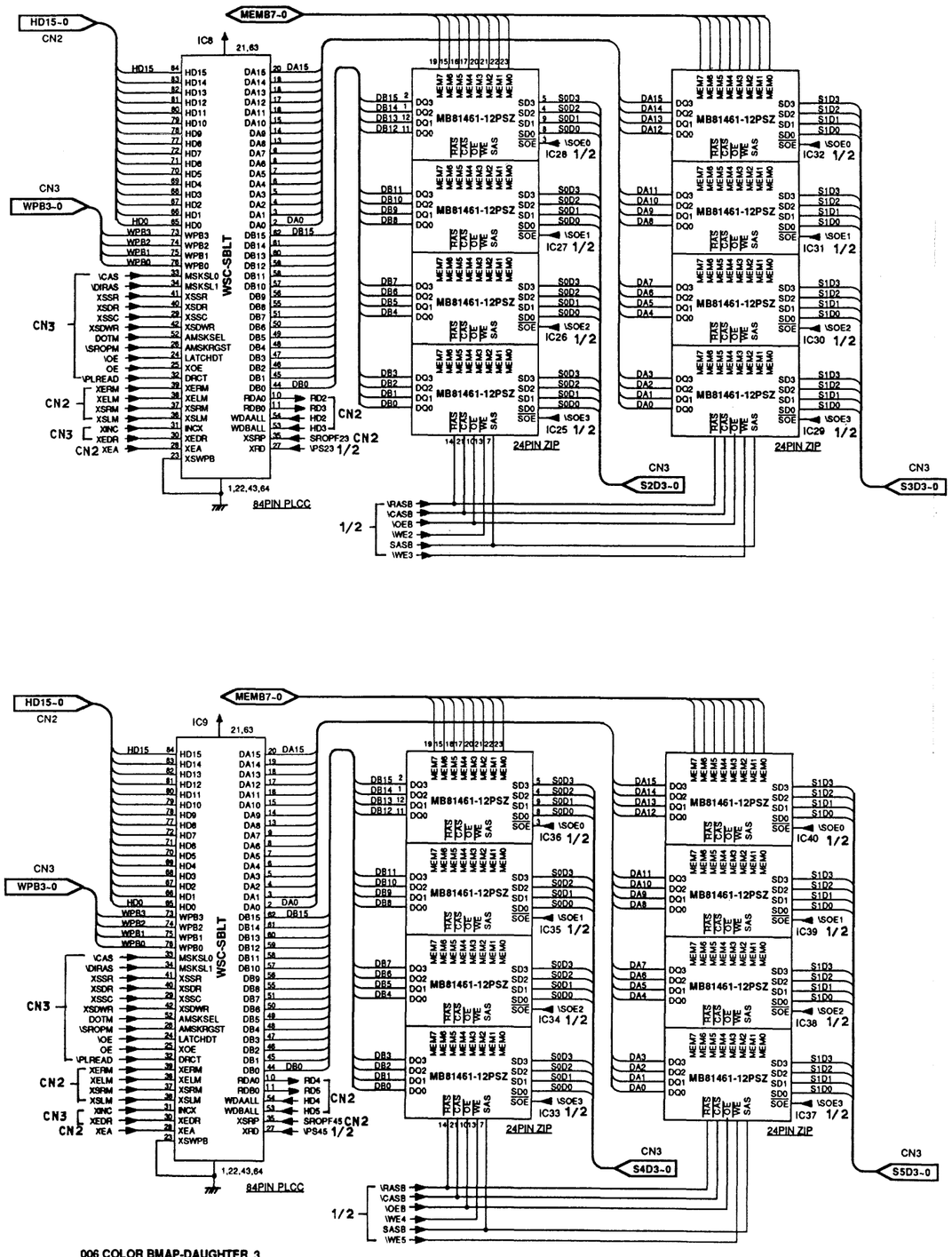


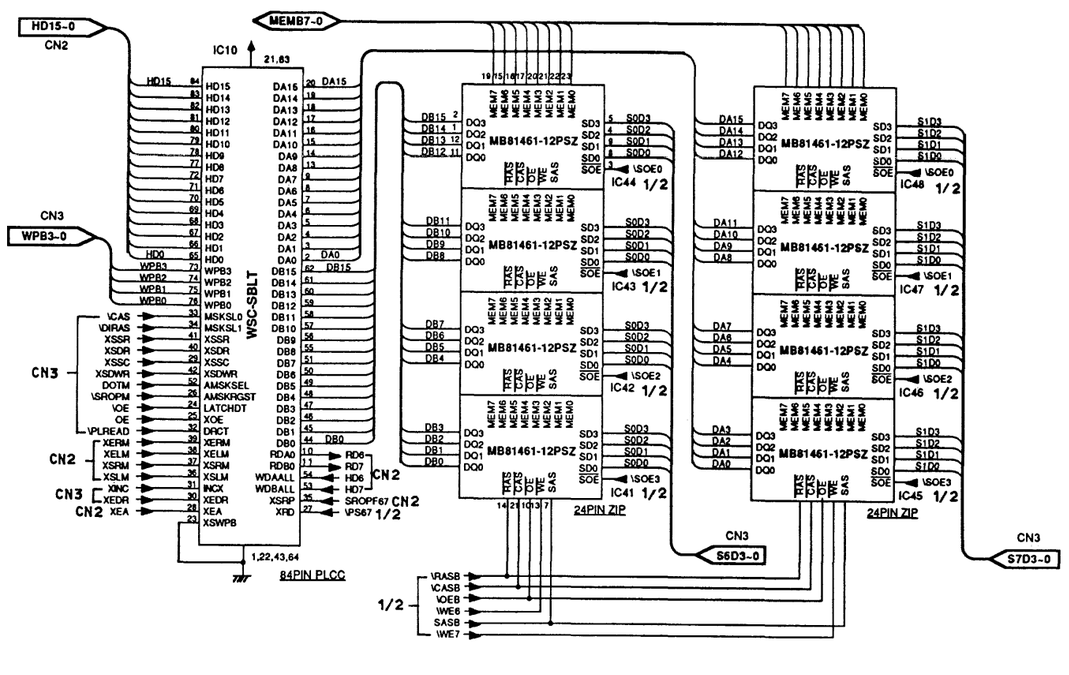


REF.NO.	TYPE	PIN NO.	
		+5V	GND
IC1-IC4	MC74F153N	16	8
IC5	SN74AS1034AN	14	7
IC6	SN74AS1034AN	14	7
IC11	MC74F32N	14	7
IC12	MC74F32N	14	7
IC13	MC74F139N	16	8
IC14	SN74ALS576AN	20	10
IC15	74F113PC	14	7
IC16	74F113PC	14	7
IC17-IC24	MB81461-12PSZ	18	6

NOTE : □ / □

SCHEMATIC DIAGRAM PAGE





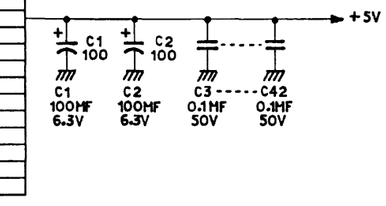
006 COLOR BMAP-DAUGHTER_3
FRMAE MEMORY-4/5

CN2

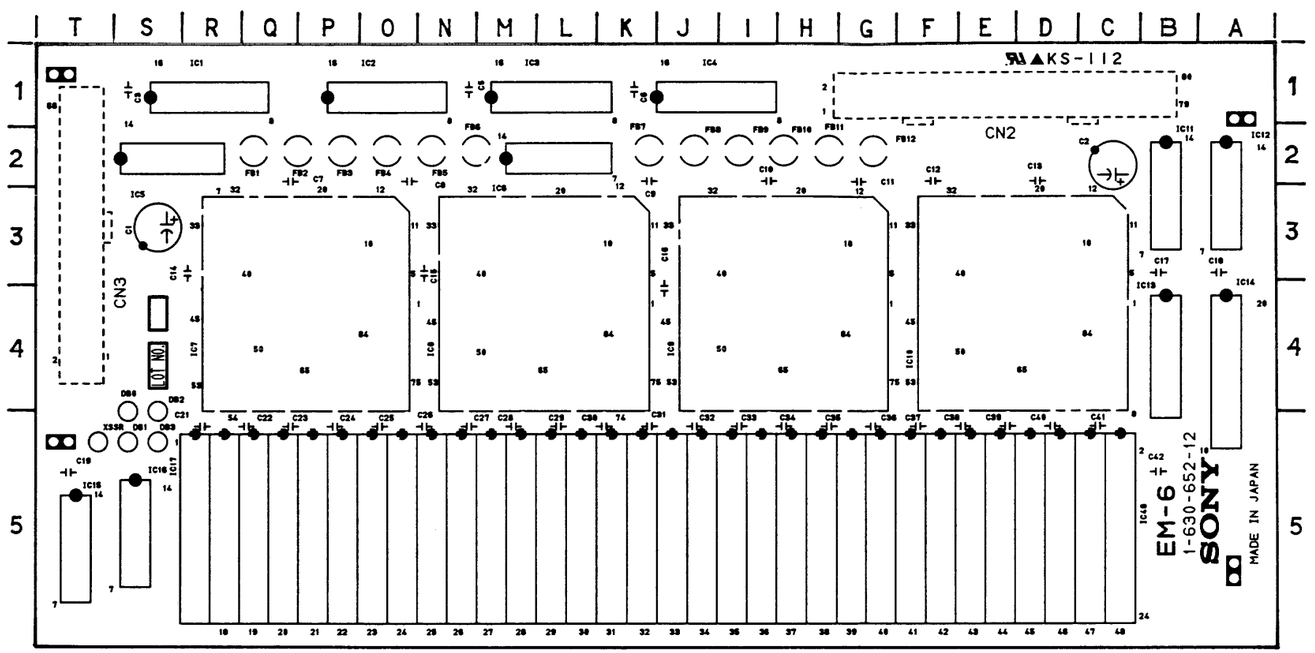
1	MA15	32	HD15
3	MA14	30	HD14
5	MA13	28	HD13
7	MA12	26	HD12
9	MA11	24	HD11
11	MA10	22	HD10
13	MA9	20	HD9
15	MA8	18	HD8
17	MA7	16	HD7
19	MA6	14	HD6
21	MA5	12	HD5
23	MA4	10	HD4
25	MA3	8	HD3
27	MA2	6	HD2
29	MA1	4	HD1
31	MA0	2	HD0
50	VY9	55	\SPBEG
52	VY8	41	\DCLR
54	VY7R	57	\SROPM
56	VY6	37	XERM
58	VY5	35	XELM
60	VY4	39	XSRM
62	VY3	33	XSLM
64	VY2	67	XEA
66	VY1	65	SROPF01
68	VY0	63	SROPF23
48	RD7	61	SROPF45
46	RD6	59	SROPF67
44	RD5	53	PS1Q
42	RD4	51	PS2Q
40	RD3	47	\PS
38	RD2		
36	RD1		
34	RD0		
69	VCC	75	GND
70	VCC	76	GND
71	VCC	77	GND
72	VCC	78	GND
73	VCC	79	GND
74	VCC	80	GND

CN3

1	S0D3	25	LD
2	S0D2	43	F
3	S0D1	11	
4	S0D0	35	\BLANKE
6	S1D3	53	WPB3
7	S1D2	51	WPB2
8	S1D1	57	WPB1
9	S1D0	55	WPB0
10	S2D3	33	\ROW/COL
12	S2D2	45	VIDEO
14	S2D1	39	\WEPB
16	S2D0	27	\RAS
18	S3D3	29	\CAS
20	S3D2	41	\OE
22	S3D1	31	OE
24	S3D0	23	XSSR
26	S4D3	49	XSSC
28	S4D2	47	XSDWR
30	S4S1	15	\PLREAD
32	S4D0	13	XSDR
34	S5D3	17	DOTM
36	S5D2	21	XINC
38	S5D1	19	XEDR
40	S5D0	58	VCC
42	S6D3	59	VCC
44	S6D2	60	VCC
46	S6D1	61	VCC
48	S6D0	62	VCC
50	S7D3	63	VCC
52	S7D2	64	GND
54	S7D1	65	GND
56	S7D0	66	GND
		67	GND
		68	GND



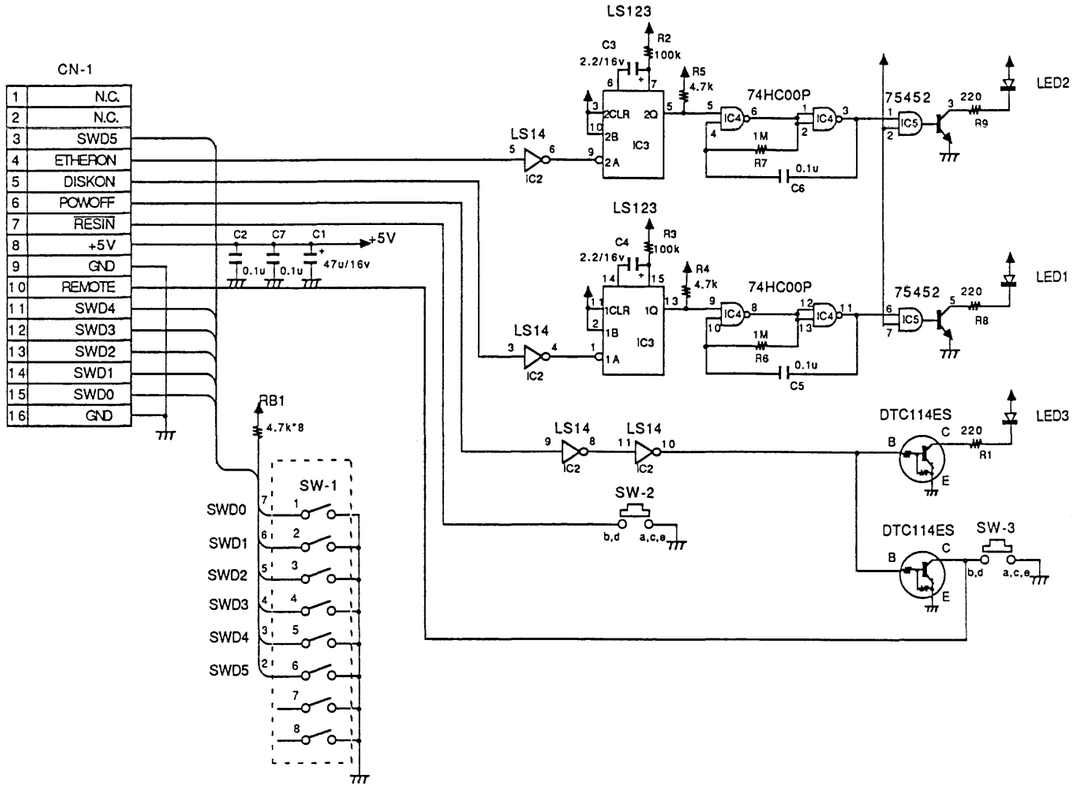
REF.NO.	TYPE	PIN NO.	
		+5V	GND
IC25-IC48	MB81461-12PSZ	18	6



Locations

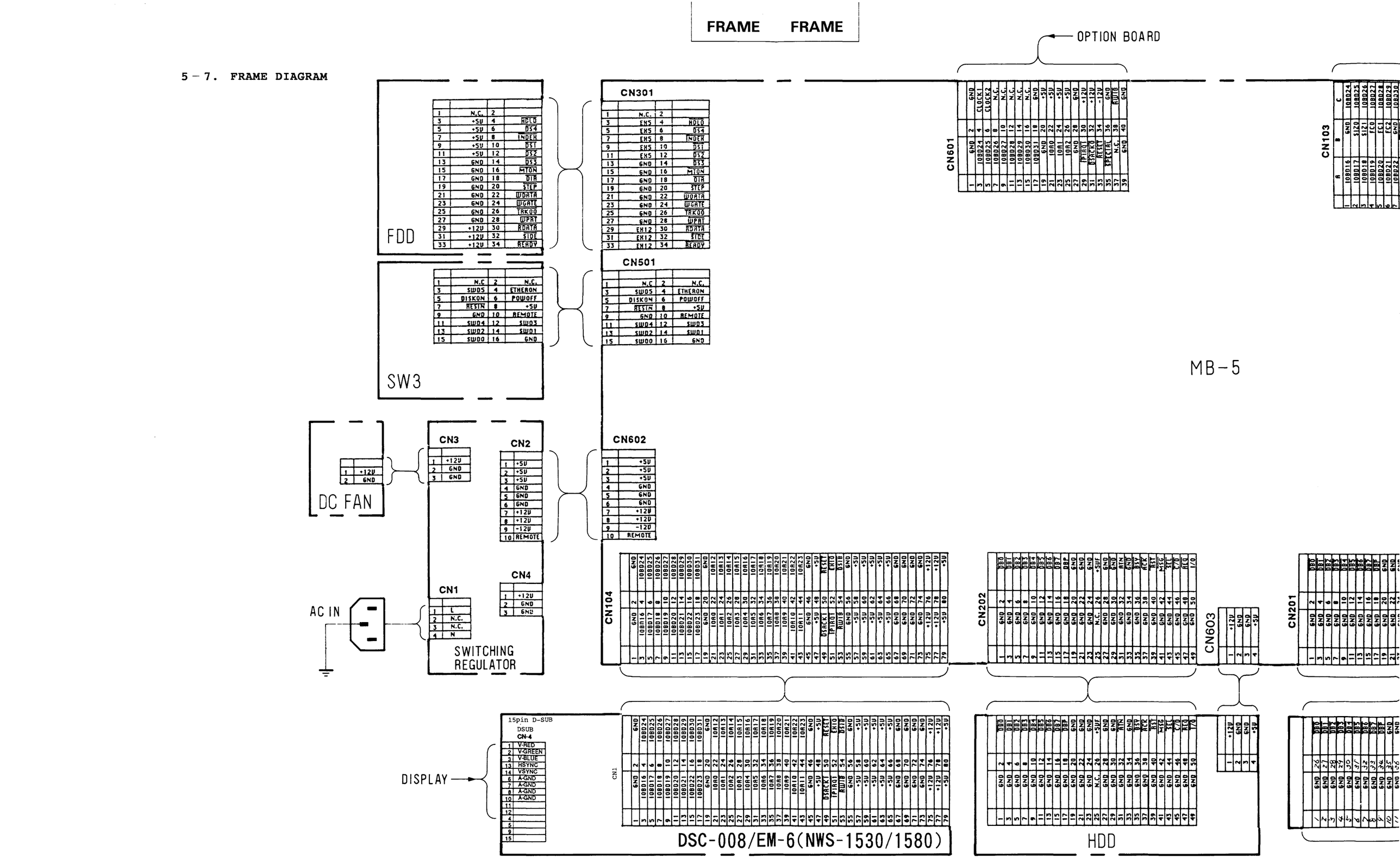
C3	S-1	C35	H-5	IC8	L-4	IC38	H-5
C5	N-1	C36	G-5	IC9	H-4	IC39	G-5
C6	K-1	C37	F-5	IC10	D-4	IC40	G-5
C7	Q-2	C38	E-5	IC11	B-2	IC41	F-5
C8	O-2	C39	E-5	IC12	A-2	IC42	F-5
C9	K-2	C40	D-5	IC13	B-4	IC43	E-5
C10	I-2	C41	C-5	IC14	A-4	IC44	E-5
C11	G-2	C42	B-5	IC15	T-5	IC45	D-5
C12	F-5	CN2	E-1	IC16	S-5	IC46	D-5
C13	D-2	CN3	T-3	IC17	R-5	IC47	C-5
C14	R-3	FB1	Q-2	IC18	R-5	IC48	C-5
C15	N-3	FB2	P-2	IC19	Q-5		
C16	K-4	FB3	P-2	IC20	Q-5		
C17	B-3	FB4	O-2	IC21	P-5		
C18	A-3	FB5	N-2	IC22	P-5		
C19	T-5	FB6	N-2	IC23	O-5		
C21	R-5	FB7	K-2	IC24	O-5		
C22	Q-5	FB8	J-2	IC25	N-5		
C23	Q-5	FB9	I-2	IC26	N-5		
C24	P-5	FB10	H-2	IC27	M-5		
C25	O-5	FB11	H-2	IC28	M-5		
C26	N-5	FB12	G-2	IC29	L-5		
C27	N-5			IC30	L-5		
C28	M-5	IC1	R-1	IC31	K-5		
C29	L-5	IC2	O-1	IC32	K-5		
C30	K-5	IC3	L-1	IC33	J-5		
C31	K-5	IC4	I-1	IC34	J-5		
C32	J-5	IC5	S-2	IC35	I-5		
C33	I-5	IC6	L-2	IC36	I-5		
C34	H-5	IC7	P-4	IC37	H-5		

5 − 6. SW-3 BOARD



REF.NO.	TYPE	PIN NO.	
		+5V	GND
IC1	SN75452BP	8	4
IC2	SN74LS14N	14	7
IC3	SN74LS123N	16	8
IC4	SN74HC00N	14	7
IC5	SN75452BP	8	4

5 – 7. FRAME DIAGRAM



FRAME FRAME

OPTION BOARD

EXPANSION BOARD

FRAME

CN601

1	GND	2
3	CLOCK1	4
5	CLOCK2	6
7	N.C.	8
9	N.C.	10
11	N.C.	12
13	N.C.	14
15	N.C.	16
17	GND	18
19	+5U	20
21	+5U	22
23	+5U	24
25	+5U	26
27	GND	28
29	+12U	30
31	+12U	32
33	-12U	34
35	GND	36
37	RDTB	38
39	GND	40

CN103

	C		B		A
1	IOBD24	2	GND	1	IOBD16
3	IOBD25	4	SI20	2	IOBD17
5	IOBD26	6	SI21	3	IOBD18
7	IOBD27	8	FC0	4	IOBD19
9	IOBD28	10	FC1	5	IOBD20
11	IOBD29	12	FC2	6	IOBD21
13	IOBD30	14	GND	7	IOBD22
15	IOBD31	16	RESET	8	IOBD23
17	GND	18	GND	9	GND
19	IIO	20	IACKSTO	10	IOA0
21	GND	22	IRDRES	11	GND
23	IOA23	24	IWRRES	12	DSTB
25	IOA22	26	GND	13	GND
27	IOA21	28	IPTROI	14	RWTB
29	IOA20	30	IPTROS	15	GND
31	IOA19	32	EXTO	16	DSACK1
33	IOA18	34	N.C.	17	GND
35	IOA17	36	GND	18	IPTRO3
37	IOA16	38	N.C.	19	GND
39	IOA15	40	N.C.	20	DSACK0
41	IOA14	42	N.C.	21	IOA7
43	IOA13	44	N.C.	22	IOA6
45	IOA12	46	N.C.	23	IOA5
47	IOA11	48	N.C.	24	IOA4
49	IOA10	50	N.C.	25	IOA3
51	IOA9	52	N.C.	26	IOA2
53	IOA8	54	-12U	27	IOA1
55	-12U	56	+12U	28	IOA0
57	GND	58	GND	29	GND
59	GND	60	GND	30	GND
61	+5U	62	+5U	31	+5U
63	+5U	64	+5U	32	+5U
65	+5U	66	+5U		
67	GND	68	GND		
69	GND	70	GND		
71	GND	72	GND		
73	+12U	74	+12U		
75	+12U	76	+12U		
77	+12U	78	+12U		
79	+5U	80	+5U		

CN604

1	+12U
2	GND
3	GND
4	+5U

CN101

	A	B	C
1	GND	GND	GND
2	GND	GND	GND
3	CLOCK1	CSTAB	MFM
4	N.C	CENTD0	HOLD
5	SYNC	CENTD1	DS4
6	WINDW	CENTD2	INDEX
7	SPECIAL	CENTD3	DS1
8	SWD5	CENTD4	DS2
9	SWD4	CENTD5	GND
10	SWD3	CENTD6	DS3
11	SWD2	CENTD7	MTON
12	SWD1	GND	DIR
13	SWD0	CBUSY	STEP
14	GND	GND	WDATA
15	-12U	CFAULT	GND
16	-12U	CLOCK2	WGATE
17	GND	GND	TRK00
18	+12U	+12U	WPRT
19	GND	GND	RDATA
20	+5U	+5U	SIDE
21	+5U	+5U	READY
22	GND	GND	GND
23	DB0	GND	MIN
24	DB1	GND	BSY
25	DB2	GND	ACK
26	DB3	GND	AST
27	DB4	GND	MSG
28	DB5	GND	SEL
29	DB6	GND	C/D
30	DB7	GND	REQ
31	DBP	GND	I/O
32	GND	GND	GND

CN102

	A	B	C
1	IOBD16	GND	IOBD24
2	IOBD17	SI20	IOBD25
3	IOBD18	SI21	IOBD26
4	IOBD19	FC0	IOBD27
5	IOBD20	FC1	IOBD28
6	IOBD21	FC2	IOBD29
7	IOBD22	GND	IOBD30
8	IOBD23	RESET	IOBD31
9	GND	GND	GND
10	IOA0	IACKSTO	IIO
11	GND	IORES	GND
12	DSTB	IWRES	IOA23
13	GND	GND	IOA22
14	RWTB	IPTRO1	IOA21
15	GND	IPTRO5	IOA20
16	DSACK1	EXTO	IOA19
17	GND	N.C.	IOA18
18	IPTRO3	GND	IOA17
19	GND	N.C.	IOA16
20	DSACK0	CLOCK	IOA15
21	IOA7	N.C.	IOA14
22	IOA6	RESIN	IOA13
23	IOA5	N.C.	IOA12
24	IOA4	N.C.	IOA11
25	IOA3	REMOTE	IOA10
26	IOA2	DISKON	IOA9
27	IOA1	ETHERON	IOA8
28	N.C.	POWOFF	N.C.
29	GND	GND	GND
30	GND	GND	GND
31	+5U	+5U	+5U
32	+5U	+5U	+5U

CN602

1	+5U
2	+5U
3	+5U
4	GND
5	GND
6	GND
7	+12U
8	+12U
9	-12U
10	REMOTE

CN301

N.C.	2	
EM5	4	HOLD
EM5	6	DS4
EM5	8	INDEX
EM5	10	DS1
EM5	12	DS2
GND	14	DS3
GND	16	MTON
GND	18	DIR
GND	20	STEP
GND	22	WDATA
GND	24	WGATE
GND	26	TRK00
GND	28	WPRT
EM12	30	RDATA
EM12	32	SIDE
EM12	34	READY

CN501

N.C	2	N.C.
SWD5	4	ETHERON
DISKON	6	POWOFF
RESIN	8	+5U
GND	10	REMOTE
SWD4	12	SWD3
SWD2	14	SWD1
SWD0	16	GND

CN202

1	GND	2
3	GND	4
5	GND	6
7	GND	8
9	GND	10
11	GND	12
13	GND	14
15	GND	16
17	GND	18
19	GND	20
21	GND	22
23	GND	24
25	N.C.	26
27	GND	28
29	GND	30
31	GND	32
33	GND	34
35	GND	36
37	GND	38
39	GND	40
41	GND	42
43	GND	44
45	GND	46
47	GND	48
49	GND	50

CN603

1	+12U
2	GND
3	GND
4	+5U

CN201

1	GND	2	DB0
3	GND	4	DB1
5	GND	6	DB2
7	GND	8	DB3
9	GND	10	DB4
11	GND	12	DB5
13	GND	14	DB6
15	GND	16	DB7
17	GND	18	DBP
19	GND	20	GND
21	GND	22	GND
23	GND	24	GND
25	N.C.	26	+5UF
27	GND	28	GND
29	GND	30	GND
31	GND	32	MIN
33	GND	34	BSY
35	GND	36	ACK
37	GND	38	RST
39	GND	40	MSG
41	GND	42	SEL
43	GND	44	C/D
45	GND	46	REQ
47	GND	48	I/O
49	GND	50	TPO

CN302

1	WINDW	2	GND
3	MFM	4	GND
5	RDATA	6	GND
7	WPRT	8	GND
9	TRK00	10	GND
11	WGATE	12	GND
13	WDATA	14	GND
15	STEP	16	GND
17	DIR	18	GND
19	DS4	20	GND
21	DS3	22	GND
23	DS2	24	GND
25	DS1	26	GND
27	SYNC	28	GND
29	RDATA	30	GND
31	HOLD	32	GND
33	N.C.	34	GND
35	SIDE	36	GND
37	N.C.	38	GND
39	N.C.	40	GND
41	MTON	44	GND
43	N.C.	46	GND
45	N.C.	48	GND
47	N.C.	50	GND

CN401

1	CSTAB	2	CENTD6
3	CENTD0	4	CENTD7
5	CENTD1	6	N.C.
7	CENTD2	8	CBUSY
9	CENTD3	10	N.C.
11	CENTD4	12	CFAULT
13	CENTD5	14	GND

MB-5

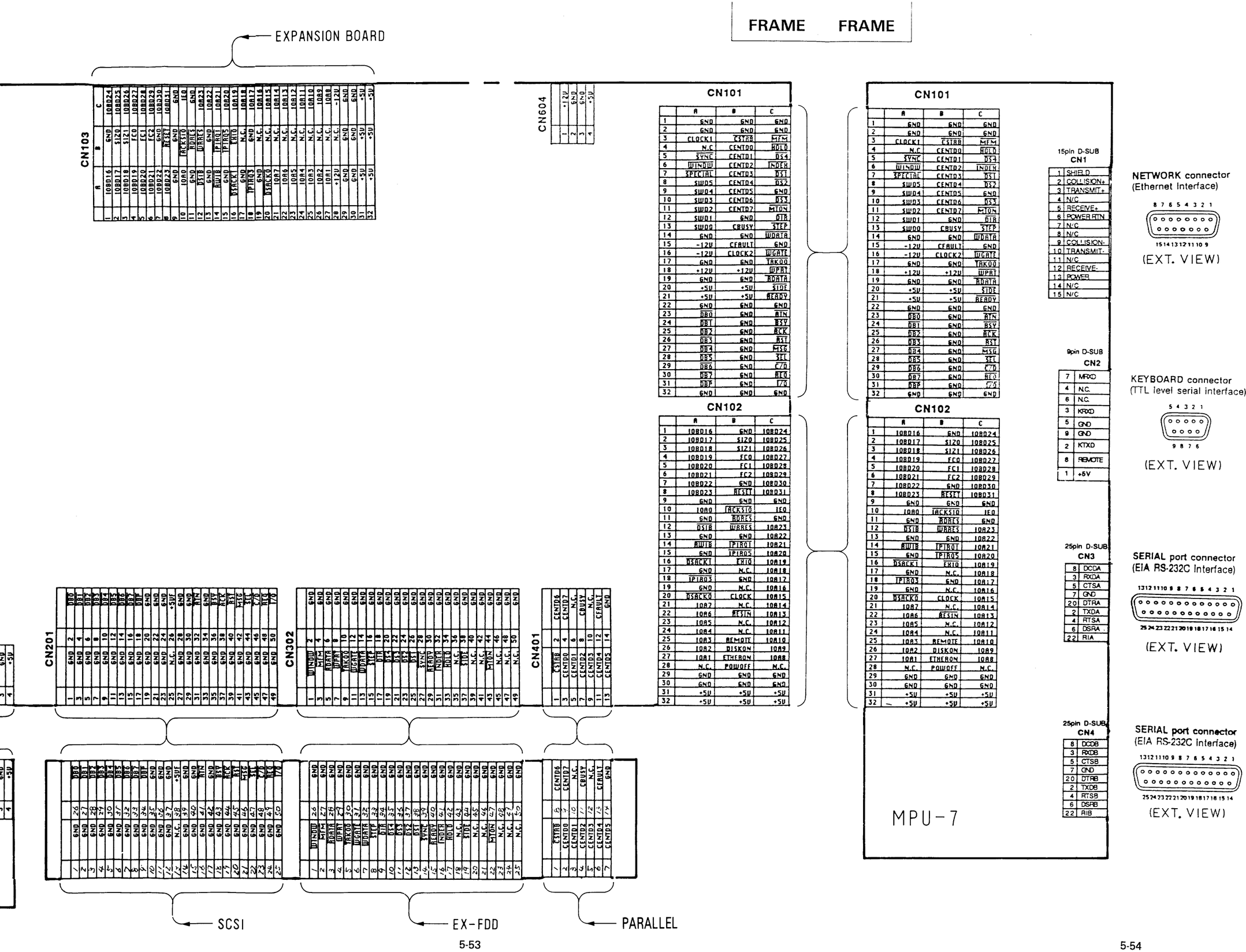
DSC-008/EM-6(NWS-1530/1580)

HDD

SCSI

EX-FDD

PARALLEL


FRAME
FRAME
EXPANSION BOARD
CN103
CN604
CN101
CN102
CN201
CN302
CN401
SCSI
EX-FDD
PARALLEL
MPU-7
15pin D-SUB
CN1
NETWORK connector
(Ethernet Interface)
(EXT. VIEW)
9pin D-SUB
CN2
KEYBOARD connector
(TTL level serial interface)
(EXT. VIEW)
25pin D-SUB
CN3
SERIAL port connector
(EIA RS-232C Interface)
(EXT. VIEW)
25pin D-SUB
CN4
SERIAL port connector
(EIA RS-232C Interface)
(EXT. VIEW)

CHAPTER 6
EXPLODED VIEW AND PARTS LIST

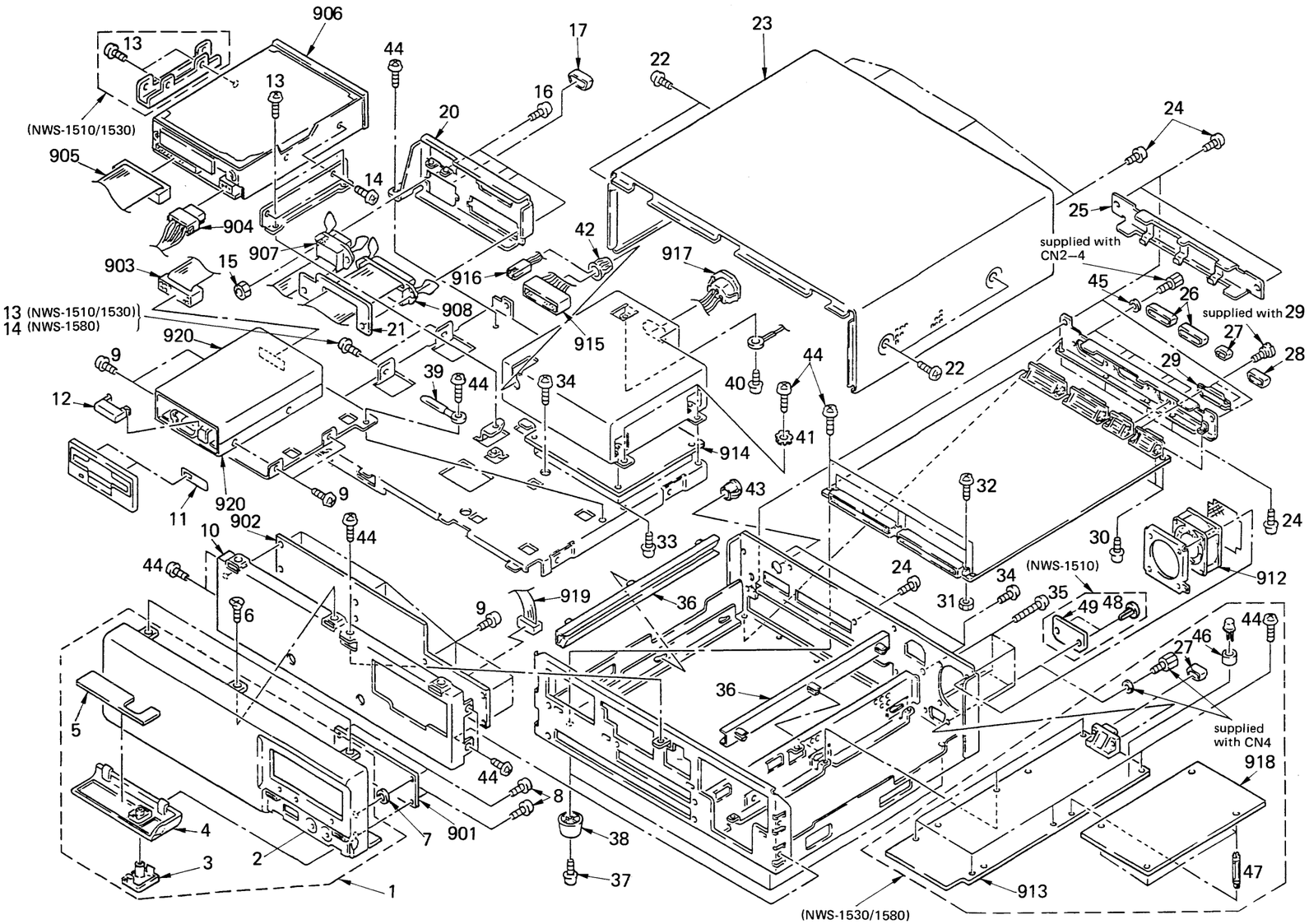
6-1. EXPLODED VIEW

NOTE:

- The mechanical parts with no reference number in the exploded views are not supplied.
- The construction parts of an assembled part are indicated with a collation number in the remark column.
- Items marked "★" are not stocked since they are seldom required for routine service. Some delay should be anticipated when ordering these items.
- Due to standardization, parts with part number suffix -XX and -X may be different from the parts specified in the components used on the set.
- Color Indication of Appearance Parts
  Example:
  (RED) . . . KNOB, BALANCE (WHITE)
  ↑ Cabinet's Color ↑ Parts Color

The components identified by mark ⚠ or dotted line with mark ⚠ are critical for safety.
Replace only with part number specified.

Note: The components identified by mark ⚠ or dotted line with mark ⚠ are critical for safety.
Replace only with part number specified.



Ref.No.	Part No.	Description
1	*A-8041-285-A	(NWS-1580)...PANEL ASSY, FRONT
	*A-8041-298-A	(NWS-1510)...PANEL ASSY, FRONT
	*A-8041-256-A	(NWS-1530)...PANEL ASSY, FRONT
2	*X-4615-401-1	FRONT PANEL/LAMP COVER ASSY
3	4-615-410-02	BUTTON
4	4-615-412-41	(NWS-1580)...DOOR
	4-615-412-51	(NWS-1510)...DOOR
	4-615-412-31	(NWS-1530)...DOOR
5	4-615-411-02	PANEL, ORNAMENTAL
6	7-682-247-04	SCREW +K 3X6
7	*3-555-872-21	SPACER
8	7-685-534-14	SCREW +BTP 2.6X8 TYPE2 N-S
9	7-682-547-04	SCREW +B 3X6
10	*4-615-415-02	COVER, FRONT
11	4-609-222-01	SPRING
12	*4-609-223-11	BUTTON, EJECT
13	7-682-661-09	SCREW +PS 4X8
14	4-612-633-01	SCREW, HD FITTING
15	7-684-023-04	N 3, TYPE 2
16	7-682-149-15	SCREW +P 3X10
17	*2-990-028-11	CAP, DUST
20	*4-615-403-01	BRACKET, CONNECTOR
21	*4-615-404-01	PLATE, CONNECTOR
22	4-886-821-11	SCREW, M3 CASE
23	*4-615-416-01	COVER, TOP
24	7-682-871-09	SCREW +BVTT 3X6 (S)
25	*X-4611-813-1	PANEL (BLANK) ASSY, PC BOARD
26	3-676-269-00	CAP (25P SOCKET SIDE), DUST
27	*4-611-831-01	CAP (C), DUST
28	*4-611-832-01	CAP (D), DUST
29	*4-606-306-11	RETAINER (CN1)
30	3-701-809-21	SCREW, TERMINAL (M3X6)
31	7-622-207-05	N 2.6, TYPE 2
32	7-628-254-40	SCREW +PS 2.6X12
33	7-682-147-01	SCREW +P 3X6
34	7-682-160-09	SCREW +P 4X6
35	7-682-656-09	SCREW +PS 3X35
36	*3-673-676-31	RAIL, PC BOARD GUIDE
37	7-685-872-09	SCREW +BVTT 3X8 (S)
38	X-3556-910-0	FOOT ASSY, MF
39	3-703-150-11	CLAMP
40	7-682-160-01	SCREW +P 4X6
41	7-623-422-07	LW 3, TYPE B
42	*3-162-704-01	BUSHING
43	4-615-429-01	PLUG, HOLE
44	7-685-871-01	SCREW +BVTT 3X6 (S)
45	7-623-207-22	SW 2.6, TYPE 2
46	4-886-543-00	(NWS-1530/1580)...TUBE, CUSHION
47	*3-682-419-01	(NWS-1510/1580)...HOLDER, P.C.B
48	3-531-576-01	(NWS-1510)...RIVET, NYLON
49	4-616-379-01	(NWS-1510)...PLATE, BLIND
901	*A-8080-385-A	MOUNTED PCB, SW-3
902	*A-8080-384-A	MOUNTED PCB, MB-5
903	1-942-879-11	HARNESS (FDD)
904	*1-942-880-11	(NWS-1580)...HARNESS (HDD POWER)
	*1-942-880-21	(NWS-1510/1530)...HARNESS (HDD POWER)
905	1-942-878-11	(NWS-1580)...HARNESS (HDD)
	1-943-570-11	(NWS-1510/1530)...HARNESS (HDD)
906	1-550-516-11	(NWS-1580)...DISC DRIVE, HARD (170MB)
	A-8000-796-A	(NWS-1510/1530)...DISC DRIVE, HARD
907	1-942-886-11	HARNESS (CENTRONICS)
908	1-942-884-11	HARNESS (SCSI)
911	*A-8041-207-A	PC BOARD ASSY (S), MPU-7
912	1-541-642-11	MOTOR, DC FAN
913	*A-8051-518-A	(NWS-1530/1580)...COMPLETE PCB, DSC-008
914	⚠1-413-452-11	REGULATOR,SWITCHING(IKX-PS3-F)
915	*1-942-882-11	HARNESS (SECONDARY POWER)
916	*1-942-883-11	HARNESS (FAN)
917	1-944-007-11	HARNESS (PRIMARY POWER)
918	*A-8051-519-A	(NWS-1530/1580)...COMPLETE PCB, EM-6
919	*1-942-887-11	HARNESS (SW-MB)
920	A-8040-838-A	FDD ASSY

6-2. ELECTRICAL PARTS LIST

NOTE:

- Due to standardization, replacements in the parts list may be different from the parts specified in the diagrams or the components used on the set.
- Items marked "*" are not stocked since they are seldom required for routine service. Some delay should be anticipated when ordering these items.
- If there are two or more same circuits in a set such as a stereophonic machine, only typical circuit parts may be indicated and capacitors and resistors in other same circuits may be omitted.

CAPACITORS:
MF: μF, PF: μμF.

RESISTORS
- All resistors are in ohms.
- F: nonflammable

COILS
- MMH: mH, UH: μH

SEMICONDUCTORS
In each case, U: μ, for example:
UA...: μA..., UPA...: μPA..., UPC...: μPC, UPD...: μPD...

The components identified by mark ⚠ or dotted line with mark ⚠ are critical for safety.
Replace only with part number specified.

Ref.No	Part No.	Description			
		SW-3 BOARD			
		**********			
919	*1-942-887-11	HARNESS (SW-MB)			
C1	1-124-589-11	ELECT	47MF	20%	10V
C2	1-161-485-00	CERAMIC	0.1MF		50V
C3	1-131-361-00	TANTALUM	2.2MF	10%	20V
C4	1-131-361-00	TANTALUM	2.2MF	10%	20V
C5	1-161-485-00	CERAMIC	0.1MF		50V
C6	1-161-485-00	CERAMIC	0.1MF		50V
C7	1-161-485-00	CERAMIC	0.1MF		50V
IC2	8-759-900-14	IC SN74LS14N			
IC3	8-759-901-23	IC SN74LS123N			
IC4	8-759-202-11	IC SN74HC00N			
LED1	8-719-812-41	DIODE TLR124			
LED2	8-719-938-68	DIODE TLY124			
LED3	8-719-812-43	DIODE TLG124A			
Q1	8-729-900-45	TRANSISTOR DTC114EF			
Q2	8-729-900-45	TRANSISTOR DTC114EF			
Q3	8-729-900-45	TRANSISTOR DTC114EF			
Q4	8-729-900-45	TRANSISTOR DTC114EF			
R1	1-249-409-11	CARBON	220	5%	1/4W
R2	1-249-441-11	CARBON	100K	5%	1/4W
R3	1-249-441-11	CARBON	100K	5%	1/4W
R4	1-249-425-11	CARBON	4.7K	5%	1/4W
R5	1-249-425-11	CARBON	4.7K	5%	1/4W
R6	1-247-903-00	CARBON	1M	5%	1/4W
R7	1-247-903-00	CARBON	1M	5%	1/4W
R8	1-249-409-11	CARBON	220	5%	1/4W
R9	1-249-409-11	CARBON	220	5%	1/4W
RB1	1-235-720-11	RES, ENCAPSULATED CERMET			
SW1	*1-526-654-00	SOCKET, IC (DP) 16P			
SW1	*1-570-922-11	SWITCH, DIP			
SW2	1-570-282-21	SWITCH, KEY BOARD			
SW3	1-570-282-21	SWITCH, KEY BOARD			

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Ref.No	Part No.	Description			
		MPU-7 MOARD			
		**********			
C1	1-123-380-00	ELECT	1MF	20%	50V
C2	1-123-380-00	ELECT	1MF	20%	50V
C3	1-164-159-11	CERAMIC	0.1MF		50V
C4	1-124-443-00	ELECT	100MF	20%	6.3V
C5	1-123-369-00	ELECT	4.7MF	20%	25V
C6	1-124-120-11	ELECT	220MF	20%	16V
C7	1-124-963-11	ELECT	33MF	20%	10V
C8	1-164-159-11	CERAMIC	0.1MF		50V
C9	1-164-159-11	CERAMIC	0.1MF		50V
C10	1-162-804-11	CERAMIC	0.068MF	10%	50V
C11	1-162-804-11	CERAMIC	0.068MF	10%	50V
C12	1-106-343-00	MYLAR	0.001MF	10%	100V
C13	1-164-159-11	CERAMIC	0.1MF		50V
C14	1-102-116-00	CERAMIC	680PF	10%	50V
C15	1-164-159-11	CERAMIC	0.1MF		50V
C16	1-164-159-11	CERAMIC	0.1MF		50V
C17	1-164-159-11	CERAMIC	0.1MF		50V
C18	1-164-159-11	CERAMIC	0.1MF		50V
C19	1-130-483-00	MYLAR	0.01MF	5%	50V
C20-C81	1-164-159-11	CERAMIC	0.1MF		50V
CN1	*1-564-958-11	CONNECTOR (D SUB) 15P			
	*4-606-306-11	RETAINER (CN1)			
CN2	1-563-323-11	CONNECTOR, D-SUB(MOUNT TYPE)9P			
	4-604-882-01	PIN, DUMMY (CN2)			
CN3	1-563-322-11	CONNECTOR,D-SUB(MOUNT TYPE)25P			
CN4	1-563-322-11	CONNECTOR,D-SUB(MOUNT TYPE)25P			
CN101	*1-506-748-31	PIN, DIN CONNECTOR (DIP) 96P			
CN102	*1-506-748-31	PIN, DIN CONNECTOR (DIP) 96P			
D1	8-719-923-48	DIODE 1S2348H			
D2	8-719-923-48	DIODE 1S2348H			
FB1-FB29	1-410-396-41	FERRITE BEAD INDUCTOR			
FL1-FL21	1-424-007-21	FILTER, NOISE (SIGNAL LINE)			
FU1	⚠1-532-779-11	FUSE, MICRO (SECONDARY)			
FU2	⚠1-532-779-11	FUSE, MICRO (SECONDARY)			
IC1	8-759-903-74	IC SN74LS374N			
	*1-526-656-00	SOCKET, IC 20P (IC1)			
IC2	8-759-902-40	IC SN74LS240N			
	*1-526-656-00	SOCKET, IC 20P (IC2)			
IC3	8-759-902-40	IC SN74LS240N			
	*1-526-656-00	SOCKET, IC 20P (IC3)			
IC4	8-759-001-90	IC MC74F74N			
IC5	8-759-904-81	IC 74F08PC			
IC6	8-759-143-35	IC UPD72067GC-3B6			
IC7	8-759-936-16	IC SN74AS1034AN			
IC8	1-540-018-11	SOCKET, IC (SIP MODULE) 30P			
IC9	1-540-018-11	SOCKET, IC (SIP MODULE) 30P			
IC10	1-540-018-11	SOCKET, IC (SIP MODULE) 30P			
IC11	8-759-915-41	IC 74F02PC			
IC12	8-759-904-81	IC 74F08PC			
IC13	8-759-797-25	IC PAL16L8BCN-N0064			
IC14	8-759-904-83	IC 74F32PC			
IC15	1-540-018-11	SOCKET, IC (SIP MODULE) 30P			
IC16	1-540-018-11	SOCKET, IC (SIP MODULE) 30P			
IC17	1-540-018-11	SOCKET, IC (SIP MODULE) 30P			
IC18	8-759-012-77	IC MC1489AP			
	*1-526-715-11	SOCKET, IC 14P (IC18)			
IC19	8-752-326-14	IC CXD1180AQ			
IC20	8-759-980-21	IC WSC-ICKDMAC			

Ref.No	Part No.	Description
IC21	8-759-002-00	IC MC74F153N
IC22	8-759-002-00	IC MC74F153N
IC23	8-749-920-39	IC THM81000L-80
IC24	8-749-920-39	IC THM81000L-80
IC25	1-540-018-11	SOCKET, IC (SIP MODULE) 30P
IC26	8-759-011-83	IC MC145406P
	*1-526-654-00	SOCKET, IC 16P (IC26)
IC27	8-759-011-83	IC MC145406P
	*1-526-654-00	SOCKET, IC 16P (IC27)
IC28	8-759-143-65	IC WSC-PARK
IC29	8-759-002-00	IC MC74F153N
IC30	8-759-936-16	IC SN74AS1034AN
IC31	1-540-018-11	SOCKET, IC (SIP MODULE) 30P
IC32	1-540-018-11	SOCKET, IC (SIP MODULE) 30P
IC33	1-540-018-11	SOCKET, IC (SIP MODULE) 30P
IC34	8-759-987-88	IC Z0853008PSC
IC35	8-759-001-97	IC MC74F139N
	*1-526-654-00	SOCKET, IC 16P (IC35)
IC36	8-759-904-80	IC 74F04PC
IC37	8-759-989-55	IC SN74ALS244BN
IC38	8-759-917-72	IC 74F244PC
IC39	8-759-901-23	IC SN74LS123N
IC40	8-759-202-11	IC TC74HC00P
IC41	8-759-354-52	IC HD75452P
IC42	8-759-904-83	IC 74F32PC
IC43	8-759-797-25	IC PAL16L8BCN-N0064
IC44	8-759-948-40	IC DS1000M-50
IC45	8-759-973-51	IC SN74AS1032AN
IC46	1-540-018-11	SOCKET, IC (SIP MODULE) 30P
IC47	1-540-018-11	SOCKET, IC (SIP MODULE) 30P
IC48	8-749-920-39	IC THM81000L-80
IC49	8-749-920-39	IC THM81000L-80
IC50	8-759-902-91	IC SN74LS540N
IC51	8-759-902-92	IC SN74LS541N
IC52	8-759-989-55	IC SN74ALS244BN
IC53	8-759-989-55	IC SN74ALS244BN
IC54	8-759-143-34	IC WSC-MEMC
IC55	8-759-002-00	IC MC74F153N
IC56	8-759-002-00	IC MC74F153N
IC57	8-759-936-16	IC SN74AS1034AN
IC58	8-759-936-16	IC SN74AS1034AN
IC59	8-759-002-25	IC MC74F245N
IC60	8-759-002-25	IC MC74F245N
IC61	8-759-002-25	IC MC74F245N
IC62	8-759-002-25	IC MC74F245N
IC63	8-759-747-06	IC MB7114L
	*1-526-654-00	SOCKET, IC 16P (IC63)
IC64	8-759-900-08	IC SN74LS08N
IC65	8-759-973-80	IC MK48T02(B)-25
	1-526-658-21	SOCKET, IC 24P (IC65)
IC66	8-759-989-55	IC SN74ALS244BN
IC67	8-759-902-45	IC SN74LS245N
IC68	8-759-980-22	IC WSC-CDECR
IC69	8-759-030-45	IC MC68882RC25
	*1-540-077-11	SOCKET, PGA 68P (IC69)

Ref.No	Part No.	Description
IC70	8-759-030-44	IC MC68030RC25
	*1-540-076-11	SOCKET, PGA 124P (IC70)
IC71	8-759-142-26	IC WSC-LANCE
IC72	8-759-002-25	IC MC74F245N
	*1-526-656-00	SOCKET, IC 20P (IC72)
IC73	8-759-002-25	IC MC74F245N
	*1-526-656-00	SOCKET, IC 20P (IC73)
IC74	8-759-746-99	IC MBM27C512-25
	1-526-659-00	SOCKET, IC 28P (IC74)
IC75	8-759-001-90	IC MC74F74N
IC76	8-759-917-46	IC 74F11PC
IC77	8-759-908-35	IC TL7705CP-B
IC78	8-759-904-82	IC 74F10PC
IC79	8-759-912-60	IC SN74S260N
IC80	8-759-910-05	IC SN74S05N
IC81	8-759-900-14	IC SN74LS14N
IC82	8-759-001-90	IC MC74F74N
IC83	8-752-328-02	IC CXK5864BSP-10L
IC84	8-752-328-02	IC CXK5864BSP-10L
IC85	8-759-939-32	IC AM7990PC-80
IC86	8-759-938-40	IC AM7992BDC
	*1-526-941-11	SOCKET, IC 24P (IC86)
IC87	8-759-915-41	IC 74F02PC
IC88	8-759-001-90	IC MC74F74N
LED1	8-719-812-32	DIODE TLY123
LED2	8-719-940-82	DIODE SLR-34MC3
OSC1	1-577-258-11	OSCILLATOR, CRYSTAL
OSC2	1-577-172-11	OSCILLATOR, CRYSTAL
OSC3	1-577-170-11	OSCILLATOR, CRYSTAL
R1	1-249-441-11	CARBON 100K 5% 1/4W
R2	1-249-441-11	CARBON 100K 5% 1/4W
R3	1-249-409-11	CARBON 220 5% 1/4W
R4	1-249-425-11	CARBON 4.7K 5% 1/4W
R5	1-247-842-11	CARBON 3K 5% 1/4W
R6	1-249-442-11	CARBON 510 5% 1/4W
R7	1-247-842-11	CARBON 3K 5% 1/4W
R8	1-214-695-00	METAL 39 1% 1/4W
R9	1-214-659-11	METAL 1.2 1% 1/4W
R10	1-214-695-00	METAL 39 1% 1/4W
R11	1-214-659-11	METAL 1.2 1% 1/4W
R12	1-214-695-00	METAL 39 1% 1/4W
R13	1-214-659-11	METAL 1.2 1% 1/4W
R14	1-214-695-00	METAL 39 1% 1/4W
R15	1-214-659-11	METAL 1.2 1% 1/4W
R16	1-249-415-11	CARBON 680 5% 1/4W
R17	1-249-415-11	CARBON 680 5% 1/4W
R18	1-249-425-11	CARBON 4.7K 5% 1/4W
R19	1-249-425-11	CARBON 4.7K 5% 1/4W
R20	1-249-411-11	CARBON 330 5% 1/4W
R21	1-249-411-11	CARBON 330 5% 1/4W
R22	1-249-425-11	CARBON 4.7K 5% 1/4W
R23	1-249-415-11	CARBON 680 5% 1/4W
R24	1-247-842-11	CARBON 3K 5% 1/4W

Ref.No	Part No.	Description
IC21	8-759-002-00	IC MC74F153N
IC22	8-759-002-00	IC MC74F153N
IC23	8-749-920-39	IC THM81000L-80
IC24	8-749-920-39	IC THM81000L-80
IC25	1-540-018-11	SOCKET, IC (SIP MODULE) 30P
IC26	8-759-011-83	IC MC145406P
	*1-526-654-00	SOCKET, IC 16P (IC26)
IC27	8-759-011-83	IC MC145406P
	*1-526-654-00	SOCKET, IC 16P (IC27)
IC28	8-759-143-65	IC WSC-PARK
IC29	8-759-002-00	IC MC74F153N
IC30	8-759-936-16	IC SN74AS1034AN
IC31	1-540-018-11	SOCKET, IC (SIP MODULE) 30P
IC32	1-540-018-11	SOCKET, IC (SIP MODULE) 30P
IC33	1-540-018-11	SOCKET, IC (SIP MODULE) 30P
IC34	8-759-987-88	IC Z0853008PSC
IC35	8-759-001-97	IC MC74F139N
	*1-526-654-00	SOCKET, IC 16P (IC35)
IC36	8-759-904-80	IC 74F04PC
IC37	8-759-989-55	IC SN74ALS244BN
IC38	8-759-917-72	IC 74F244PC
IC39	8-759-901-23	IC SN74LS123N
IC40	8-759-202-11	IC TC74HC00P
IC41	8-759-354-52	IC HD75452P
IC42	8-759-904-83	IC 74F32PC
IC43	8-759-797-25	IC PAL16L8BCN-N0064
IC44	8-759-948-40	IC DS1000M-50
IC45	8-759-973-51	IC SN74AS1032AN
IC46	1-540-018-11	SOCKET, IC (SIP MODULE) 30P
IC47	1-540-018-11	SOCKET, IC (SIP MODULE) 30P
IC48	8-749-920-39	IC THM81000L-80
IC49	8-749-920-39	IC THM81000L-80
IC50	8-759-902-91	IC SN74LS540N
IC51	8-759-902-92	IC SN74LS541N
IC52	8-759-989-55	IC SN74ALS244BN
IC53	8-759-989-55	IC SN74ALS244BN
IC54	8-759-143-34	IC WSC-MEMC
IC55	8-759-002-00	IC MC74F153N
IC56	8-759-002-00	IC MC74F153N
IC57	8-759-936-16	IC SN74AS1034AN
IC58	8-759-936-16	IC SN74AS1034AN
IC59	8-759-002-25	IC MC74F245N
IC60	8-759-002-25	IC MC74F245N
IC61	8-759-002-25	IC MC74F245N
IC62	8-759-002-25	IC MC74F245N
IC63	8-759-747-06	IC MB7114L
	*1-526-654-00	SOCKET, IC 16P (IC63)
IC64	8-759-900-08	IC SN74LS08N
IC65	8-759-973-80	IC MK48T02(B)-25
	1-526-658-21	SOCKET, IC 24P (IC65)
IC66	8-759-989-55	IC SN74ALS244BN
IC67	8-759-902-45	IC SN74LS245N
IC68	8-759-980-22	IC WSC-CDECR
IC69	8-759-030-45	IC MC68882RC25
	*1-540-077-11	SOCKET, PGA 68P (IC69)

Ref.No	Part No.	Description
IC70	8-759-030-44	IC MC68030RC25
	*1-540-076-11	SOCKET, PGA 124P (IC70)
IC71	8-759-142-26	IC WSC-LANCE
IC72	8-759-002-25	IC MC74F245N
	*1-526-656-00	SOCKET, IC 20P (IC72)
IC73	8-759-002-25	IC MC74F245N
	*1-526-656-00	SOCKET, IC 20P (IC73)
IC74	8-759-746-99	IC MBM27C512-25
	1-526-659-00	SOCKET, IC 28P (IC74)
IC75	8-759-001-90	IC MC74F74N
IC76	8-759-917-46	IC 74F11PC
IC77	8-759-908-35	IC TL7705CP-B
IC78	8-759-904-82	IC 74F10PC
IC79	8-759-912-60	IC SN74S260N
IC80	8-759-910-05	IC SN74S05N
IC81	8-759-900-14	IC SN74LS14N
IC82	8-759-001-90	IC MC74F74N
IC83	8-752-328-02	IC CXK5864BSP-10L
IC84	8-752-328-02	IC CXK5864BSP-10L
IC85	8-759-939-32	IC AM7990PC-80
IC86	8-759-938-40	IC AM7992BDC
	*1-526-941-11	SOCKET, IC 24P (IC86)
IC87	8-759-915-41	IC 74F02PC
IC88	8-759-001-90	IC MC74F74N
LED1	8-719-812-32	DIODE TLY123
LED2	8-719-940-82	DIODE SLR-34MC3
OSC1	1-577-258-11	OSCILLATOR, CRYSTAL
OSC2	1-577-172-11	OSCILLATOR, CRYSTAL
OSC3	1-577-170-11	OSCILLATOR, CRYSTAL

R1	1-249-441-11	CARBON	100K	5%	1/4W
R2	1-249-441-11	CARBON	100K	5%	1/4W
R3	1-249-409-11	CARBON	220	5%	1/4W
R4	1-249-425-11	CARBON	4.7K	5%	1/4W
R5	1-247-842-11	CARBON	3K	5%	1/4W
R6	1-249-442-11	CARBON	510	5%	1/4W
R7	1-247-842-11	CARBON	3K	5%	1/4W
R8	1-214-695-00	METAL	39	1%	1/4W
R9	1-214-659-11	METAL	1.2	1%	1/4W
R10	1-214-695-00	METAL	39	1%	1/4W
R11	1-214-659-11	METAL	1.2	1%	1/4W
R12	1-214-695-00	METAL	39	1%	1/4W
R13	1-214-659-11	METAL	1.2	1%	1/4W
R14	1-214-695-00	METAL	39	1%	1/4W
R15	1-214-659-11	METAL	1.2	1%	1/4W
R16	1-249-415-11	CARBON	680	5%	1/4W
R17	1-249-415-11	CARBON	680	5%	1/4W
R18	1-249-425-11	CARBON	4.7K	5%	1/4W
R19	1-249-425-11	CARBON	4.7K	5%	1/4W
R20	1-249-411-11	CARBON	330	5%	1/4W
R21	1-249-411-11	CARBON	330	5%	1/4W
R22	1-249-425-11	CARBON	4.7K	5%	1/4W
R23	1-249-415-11	CARBON	680	5%	1/4W
R24	1-247-842-11	CARBON	3K	5%	1/4W

Ref.No	Part No.	Description			
RB1	1-235-708-11	RES, ENCAPSULATED CERMET			
RB2	1-235-706-11	RES, BLOCK			
RB3	1-235-706-11	RES, BLOCK			
RB4	1-235-706-11	RES, BLOCK			
RB5	1-235-706-11	RES, BLOCK			
RB6	1-235-352-11	RES, BLOCK			
RB7	1-235-656-11	RES, ENCAPSULATED CERMET			
RB8	1-235-720-11	RES, ENCAPSULATED CERMET			
RB9	1-235-656-11	RES, ENCAPSULATED CERMET			
RB10	1-235-720-11	RES, ENCAPSULATED CERMET			
RB11	1-235-720-11	RES, ENCAPSULATED CERMET			

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DSC-008 BOARD (NWS-1530/1580)
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913	*A-8051-518-A	(NWS-1530/1580)...COMPLETE PCB, DSC-008			
C1	1-161-473-00	CERAMIC	0.01MF	10%	50V
C2	1-164-159-11	CERAMIC	0.1MF		50V
C3	1-161-473-00	CERAMIC	0.01MF	10%	50V
C4	1-126-101-11	ELECT	100MF	20%	6.3V
C5	1-164-159-11	CERAMIC	0.1MF		50V
C6	1-161-473-00	CERAMIC	0.01MF	10%	50V
C7-C47	1-164-159-11	CERAMIC	0.1MF		50V
C48	1-126-101-11	ELECT	100MF	20%	6.3V
CN1	*1-568-058-11	CONNECTOR,TX(P.L)(PC BOARD)80P			
CN2	*1-568-062-11	CONNECTOR,TX(S.S)(PC BOARD)80P			
CN3	*1-568-574-11	CONNECTOR,TX(S.S)(PC BOARD)68P			
CN4	1-568-463-11	CONNECTOR, D-SUB (SOCKET) 15P			
FB1	1-410-396-41	FERRITE BEAD INDUCTOR			
FB2	1-410-396-41	FERRITE BEAD INDUCTOR			
FL1	1-424-103-11	FILTER, SIGNAL LINE NOISE			
FL2	1-424-103-11	FILTER, SIGNAL LINE NOISE			
FL3	1-424-103-11	FILTER, SIGNAL LINE NOISE			
IC1	8-759-901-74	IC SN74LS174N			
IC2	8-759-902-92	IC SN74LS541N			
IC3	8-759-904-87	IC 74F374PC			
IC4	8-759-904-87	IC 74F374PC			
IC5	8-759-946-38	IC SN74ALS574AN			
IC6	8-759-946-38	IC SN74ALS574AN			
IC7	8-759-902-45	IC SN74LS245N			
IC8	8-759-900-74	IC SN74LS74AN			
IC9	8-759-910-38	IC SN74S38N			
IC10	8-759-915-41	IC 74F02PC			
IC11	8-759-001-90	IC MC74F74N			
IC12	8-759-795-31	IC AMPAL16L8BPC-N0056			
IC13	8-759-987-94	IC WSC-CGLUE			
IC14	8-759-320-79	IC HN62321BPAA1			
	1-526-659-00	SOCKET, IC 28P (IC14)			

Ref.No	Part No.	Description			
IC15	8-759-320-80	IC HN62321BPAA2			
	1-526-659-00	SOCKET, IC 28P (IC15)			
IC16	8-759-902-92	IC SN74LS541N			
IC17	8-759-902-92	IC SN74LS541N			
IC18	8-759-903-74	IC SN74LS374N			
IC19	8-759-901-64	IC SN74LS164N			
IC20	8-759-901-75	IC SN74LS175N			
IC21	8-759-902-92	IC SN74LS541N			
IC22	8-759-902-92	IC SN74LS541N			
IC23	8-759-113-38	IC UPD65013G-160			
IC24	8-759-321-22	IC HD6445CP4			
	*1-540-055-11	SOCKET, IC (PCC PACKAGE) 44P (IC24)			
IC25	8-759-903-73	IC SN74LS373N			
IC26	8-759-903-73	IC SN74LS373N			
IC27	8-759-796-52	IC PAL16L8BCN-N0097			
	*1-526-656-00	SOCKET, IC 20P (IC27)			
IC28	8-759-902-92	IC SN74LS541N			
IC29	8-759-989-73	IC SN74LS257BN			
IC30	8-759-796-54	IC PAL16R6BPC-N0099			
IC31	8-759-904-87	IC 74F374PC			
IC32	8-759-795-36	IC AMPAL16R6BPC-N0061			
IC33	8-759-795-35	IC AMPAL16L8BPC-N0060			
IC34	8-759-796-53	IC PAL16R6BPC-N0098			
IC35	8-759-902-40	IC SN74LS240N			
IC36	8-759-904-83	IC 74F32PC			
IC37	8-759-904-81	IC 74F08PC			
IC38	8-759-901-07	IC SN74LS107AN			
IC39	8-759-917-50	IC 74F113PC			
IC40	8-759-001-90	IC MC74F74N			
IC41	8-759-001-90	IC MC74F74N			
IC42	8-759-917-58	IC 74F164PC			
IC43	8-759-947-42	IC SN74AS1004AN			
IC44	8-759-906-71	IC 74F175PC			
IC45	8-759-987-93	IC AM81C458JC-80			
IC46	8-759-002-64	IC MC10H103L			
IC47	8-759-910-38	IC SN74S38N			
OSC1	1-577-550-11	OSCILLATOR, CRYSTAL			
R1	1-214-729-00	METAL	1K	1%	1/4W
R2	1-214-702-00	METAL	75	1%	1/4W
R3	1-214-702-00	METAL	75	1%	1/4W
R4	1-214-702-00	METAL	75	1%	1/4W
R5	1-214-722-00	METAL	510	1%	1/4W
R6	1-214-684-11	METAL	13	1%	1/4W
R7	1-249-411-11	CARBON	330	5%	1/4W
R8	1-249-411-11	CARBON	330	5%	1/4W
R9	1-249-442-11	CARBON	510	5%	1/4W
R10	1-249-442-11	CARBON	510	5%	1/4W
R11	1-249-408-11	CARBON	180	5%	1/4W
R12	1-249-410-11	CARBON	270	5%	1/4W
R13	1-249-416-11	CARBON	820	5%	1/4W
R14	1-249-411-11	CARBON	330	5%	1/4W
R15	1-249-425-11	CARBON	4.7K	5%	1/4W
R16	1-249-425-11	CARBON	4.7K	5%	1/4W

Ref.No	Part No.	Description			
RB1	1-235-713-11	RES, ENCAPSULATED CERMET			
Z1	8-759-941-83	IC AD589JH			

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EM-6 BOARD (NWS-1530/1580)
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918	*A-8051-519-A	(NWS-1530/1580)...COMPLETEDPCB,,EM-6			
C1	1-126-101-11	ELECT	100MF	20%	6.3V
C2	1-126-101-11	ELECT	100MF	20%	6.3V
C3	1-164-159-11	CERAMIC	0.1MF		50V
C5-C19	1-164-159-11	CERAMIC	0.1MF		50V
C21-C42	1-164-159-11	CERAMIC	0.1MF		50V
CN2	*1-568-575-11	HEADER, CONNECTOR PIN 80P			
CN3	*1-568-576-11	HEADER, CONNECTOR PIN 68P			
FB1-FB12	1-410-396-41	FERRITE BEAD INDUCTOR			
IC1	8-759-002-00	IC MC74F153N			
IC2	8-759-002-00	IC MC74F153N			
IC3	8-759-002-00	IC MC74F153N			
IC4	8-759-002-00	IC MC74F153N			
IC5	8-759-936-16	IC SN74AS1034AN			
IC6	8-759-936-16	IC SN74AS1034AN			
IC7	8-759-980-30	IC WSC-SBLT			
IC8	8-759-980-30	IC WSC-SBLT			
IC9	8-759-980-30	IC WSC-SBLT			
IC10	8-759-980-30	IC WSC-SBLT			
IC11	8-759-904-83	IC 74F32PC			
IC12	8-759-904-83	IC 74F32PC			
IC13	8-759-001-97	IC MC74F139N			
IC14	8-759-989-63	IC SN74ALS576AN			
IC15	8-759-917-50	IC 74F113PC			
IC16	8-759-917-50	IC 74F113PC			
IC17-IC48	8-759-941-94	IC MB81461-12PSZ			

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MB-5 BOARD
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902	*A-8080-384-A	MONTED PCB, MB-5			
C1	1-123-332-00	ELECT	47MF	20%	16V
C2	1-123-332-00	ELECT	47MF	20%	16V
CN101	1-563-736-11	SOCKET, PC BOARD MOUNT DIN 96P			
CN102	1-563-736-11	SOCKET, PC BOARD MOUNT DIN 96P			
CN103	1-563-736-11	SOCKET, PC BOARD MOUNT DIN 96P			
CN104	*1-568-062-11	CONNECTOR,TX(S.S)(PC BOARD)80P			
CN201	1-566-312-11	HEADER, CONNECTOR 50P			
CN202	1-566-312-11	HEADER, CONNECTOR 50P			
CN301	*1-565-429-11	HEADER, CONNECTOR 34P			
CN302	*1-568-109-11	HEADER, CONNECTOR 50P			
CN401	*1-565-198-11	HEADER, CONNECTOR 14P			
CN501	*1-568-063-11	HEADER, CONNECTOR 16P			
CN601	*1-565-089-11	CONNECTOR,TX(S.S)(PC BOARD)40P			
CN602	*1-506-599-11	PIN, CONNECTOR 10P			
CN603	*1-564-241-00	PIN, CONNECTOR 4P			
CN604	*1-564-241-00	PIN, CONNECTOR 4P			
D1	8-719-970-02	DIODE 1SR139-400			
F1	⚠1-532-779-11	FUSE, MICRO (SECONDARY)			

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ACCESSORY & PACKING MATARIAL
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3-750-688-12	MANUAL, INSTRUCTION
3-786-490-11	MANUAL, INSTRUCTION (ROM MONITOR)
⚠1-551-631-00	CORD, POWER
*3-704-350-01	SHEET (STANDARD), PROTECTION

Note: The components identified by mark ⚠ or dotted line with mark ⚠ are critical for safety. Replace only with part number specified.

9-974-300-11

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