FWT0100/FWT1100
Winchester/Floppy Disk Storage System
OEM Manual

Scientific Micro Systems, Inc.

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WINCHESTER/FLOPPY DISK STORAGE SYSTEM

OEM MANUAL

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APPLICABLE PRODUCT NUMBERS		
Board	PWB. Assy.	Prog. Assy.
FWD0101 Formatter	0003904 Rev. K and up	1001943 Rev. K and up
LSI-11 I/F	0003770 Rev. E and up	1001939 Rev. M and up
PDP-11 I/F	0003799 Rev. F and up	1001956 Rev. C and up
TS0100	0004356 Rev. D and up	1002049 Rev. B and up

Warning: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. As temporarily permitted by regulation it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

See section II-K for additional information.

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I. INTRODUCTION

A. PRODUCT LINE OVERVIEW

The FWT system provides power and enclosure for a complete disk system with up to 71.2 Mbytes of formatted 8" Winchester disk storage plus the convenience of floppy disk or 1/4 inch cartridge tape removable media for any of the DEC* PDP-11 or LSI-11 computers. The disk controller can be operated as an RX02 compatible controller or in an extended mode for many feature and performance advantages over RX02. All of this capacity and performance comes in a standard rack mounting or desk top unit which is 5.25 inches high.

The disk system is supplied with a complete disk controller installed along with 2 floppy disks or 1 fixed disk with either 1 floppy disk or 1 cartridge tape. Table top, rack mount and a variety of voltage and frequency options are supported.

The SMS floppy/Winchester disk controller consists of two printed circuit boards. One, called the interface board, plugs into the host CPU (LSI-11 or PDP-11) backplane. The other, called the formatter board, is mounted above the disk drives. Cartridge tape systems have two interface boards, one for the Winchester disk, and one for the cartridge tape drive.

The following FWT models are currently available:

Model Number	Configuration
FWT0122S	LSI-11 disk system with (2) Shugart SA800 single head floppies and FWD0101 formatter
FWT0127S	LSI-11 disk system with (2) Shugart SA850 dual head floppies and FWD0101 formatter
FWT01172	LSI-11 disk system with (1) Shugart SA850 dual head floppy plus (1) Shugart SA1004 8" 8.9Mbyte (formatted) Winchester.
FWT01174	LSI-11 disk system with (1) Shugart SA850 dual head floppy plus (1) Quantum Q2020 8" 17.8MByte (formatted) Winchester.
FWT01177	LSI-11 disk system with (1) Shugart SA850 dual head floppy plus (1) Quantum Q2040 8" 35.6MByte (formatted) Winchester.
FWT01178	LSI-11 disk system with (1) Shugart SA850 dual head floppy plus (1) Quantum Q2080 8" 71.2Mb (formatted) Winchester.
FWT01184	LSI-11 disk system with (1) Quantum Q2020 8" 17.8 MByte (formatted) Winchester and (1) Kennedy 6455 cartridge tape system.

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* DEC, PDP, UNIBUS, LSI-11, and RSX are registered trademarks of Digital Equipment Corporation.

FWT01187	LSI-11 disk system with (1) Quantum Q2040 8" 35.6 MByte (formatted) Winchester and (1) Kennedy 6455 cartridge tape system.
FWT01188	LSI-11 disk system with (1) Quantum Q2080 8" 71.2 MByte (formatted) Winchester and (1) Kennedy 6455 cartridge tape system.
FWT01180	One add-on cartridge tape system complete with cabinet, power suppply, and Q-BUS interface board.
FWT00002	One add-on 8.9 MByte (formatted) Winchester complete with cabinet, power supply, and cable for connection to an existing FWD controller.
FWT00004	One add-on 17.8 MByte (formatted) Winchester complete with cabinet, power supply, and cable for connection to an existing FWD controller.
FWT00006	One add-on 35.6 MByte (formatted) Winchester complete with cabinet, power supply, and cable for connection to an existing FWD controller.
FWT00008	One add-on 71.2 MByte (formatted) Winchester complete with cabinet, power supply, and cable for connection to an existing FWD controller.

Model Number	Configuration
FWT1122S	PDP-11 disk system with (2) Shugart SA800 single head floppies and FWD0101 formatter
FWT1127S	PDP-11 disk system with (2) Shugart SA850 dual head floppies and FWD0101 formatter
FWT11172	PDP-11 disk system with (1) Shugart SA850 dual head floppy plus (1) Shugart SA1004 8" 8.9Mbyte (formatted) Winchester.
FWT11174	PDP-11 disk system with (1) Shugart SA850 dual head floppy plus (1) Quantum Q2020 8" 17.8MByte (formatted) Winchester.
FWT11177	PDP-11 disk system with (1) Shugart SA850 dual head floppy plus (1) Quantum Q2040 8" 35.6MByte (formatted) Winchester.
FWT11178	PDP-11 disk system with (1) Shugart SA850 dual head floppy plus (1) Quantum Q2080 8" 71.2Mb (formatted) Winchester.
FWT11184	PDP-11 disk system with (1) Quantum Q2020 8" 17.8 MByte (formatted) Winchester and (1) Kennedy 6455 cartridge tape system.

FWT11187	PDP-11 disk system with (1) Quantum Q2040 8" 35.6 MByte (formatted) Winchester and (1) Kennedy 6455 cartridge tape system.
FWT11188	PDP-11 disk system with (1) Quantum Q2080 8" 71.2 MByte (formatted) Winchester and (1) Kennedy 6455 cartridge tape system.
FWT11180	One add-on cartridge tape system complete with cabinet, power suppply, and UNIBUS interface board.

All systems above configured for 115VAC/60Hz operation.

Options (append after model number):

-E	Option for 230VAC, 50Hz.
-R	Includes rack mounting slides and hardware.
-ER	230VAC, 50Hz and rack mount.
-D	Option for 115VAC, 50Hz.
-DR	115VAC, 50Hz and rack mount.
-U	230VAC, 60Hz Option
-UR	230VAC, 60Hz and rack mount.

B. FEATURES

- RX02 interface and command compatible with optional performance improvements
- Complete, high performance Winchester/floppy combination DMA controller
- Enclosure occupies only 5.25" of standard RETMA rack space
- RX01, RX02, IBM 1, 2/2D floppy format compatibility plus additional formats
- Program selectable formats: 128, 256, 512, 1024 bytes/sector for the floppy disks and 256, 512 bytes/sector for the fixed disk
- Patented data recovery circuit that requires no adjustments for maximum reliability
- Complete error retry
- Error correction
- Flaw management for fixed disks
- Dual height LSI-11 interface board, quad height PDP-11 interface board
- Programmable sector interleave and track and head switch offsets on both the floppy and fixed disk drives for maximum performance
- Block reads/writes across cylinder boundaries up to 64K words
- Optimized DMA transfers for minimum bus loading
- Direct transfers to/from memory through 64 word First In, First Out buffer
- TS-11/TSV05 compatible cartridge tape
- Comprehensive self-diagnostics and test commands
- Supports both physical and logical disk addresses
- Full 22-bit Q-BUS addressing for disk and cartridge tape
- Selectable device register and interrupt vector address
- Bootstrap from floppy, fixed disk, or cartridge tape
- Complete RT-11 and RSX-11M software support for the extended function and performance mode
- Comprehensive stand-alone software utility package for disk formatting, back-up, copying and system testing.
- Table top or rack mounting options available
- European and other voltage options available

C. DISK FUNCTIONAL SPECIFICATIONS

Floppy drives supported:	Shugart SA800 (single sided), Shugart SA850 (double sided) or compatible
Diskette formats:	IBM Diskette 1, 2/2D. DEC RX01, RX02 double density plus program selected bytes/sector of 128, 256, 512 or 1024 on both single and double density.
Fixed drives supported:	Shugart SA1000 8" Winchester drive series. Quantum Q2000 8" Winchester drive series.
Fixed drive format:	MFM encoding with selectable formats of 256 or 512 bytes/sector
Number of bus registers:	2 (4 addresses)
Register addresses:	Jumper selectable (177170_8, 177172_8 is configured at factory)
Interrupt address:	Jumper selectable (264_8 is configured at factory)
Controller Bus Loading:	All bus connections present 1 DC load and 2.5 AC loads to the bus.
LSI-11 DMA cycle time:	On a read, if reply is asserted within 150 ns of the assertion of DIN, the DMA cycle will complete in 1.0us. On a write, if reply is asserted within 150ns of the assertion of DOUT, the DMA cycle will complete within 1.15us. On Winchester transfers, multiple word bursts (up to 4 max.) are performed, minimizing arbitration overhead.
PDP-11 DMA cycle time:	If the memory access is less than 300 ns, then the DMA cycle will complete within 850 ns. On Winchester transfers, multiple word bursts (2 or 4 words, strap selectable) are performed, minimizing arbitration overhead.

D. CARTRIDGE TAPE FUNCTIONAL SPECIFICATIONS

Tape drives supported:	1/4" Kennedy 6455 cartridge (4 track)
Media:	3M type DC300A, DC300XL, DC300XL+, and DC600A isoelastic 1/4" data cartridge
Number of bus registers:	2 (4 addresses)
Register addresses:	jumper selectable (7725208 - 7725238 is configured at factory)
Interrupt address:	jumper selectable (2248 is configured at factory)
Boot PROM address:	jumper selectable (7730008 is configured at factory)
Controller bus loading:	all bus connections present 1 DC load and 2.5 AC loads to the bus
LSI-11 DMA cycle time:	BSACKL is asserted for 2us per word

E. PHYSICAL SPECIFICATIONS

Environmental:

Relative humidity: 20 - 80% (required by floppy drives)

Operating temperature: 4 to 40 degrees C
Storage temperature: -20 to 50 degrees C

Wet bulb and dew point temperatures (i.e. humidity temperature combinations) which cause internal or external condensation are not allowed.

NOTE: 1) Environmental requirements for floppy disk media may vary. Diskettes should be allowed to reach ambient temperature before formatting, reading or writing.

2) Interface board requires an operating temperature of 0-50 degrees C and a relative humidity of 10-90%.

Electrical:

Input: 90 - 127VAC or 180 - 253VAC
Frequency: 50 or 60Hz + .5Hz

(See section II-H for fuse requirements.)

Steady state max current (both drives stepping):
115VAC installations - 4.6A
230VAC installations - 2.3A

Starting current (3 sec. Winchester sys. only):
115VAC installations - ~7.6A*
230VAC installations - ~4.8A*

*Starting current may exceed these values for less than 100 msec when power is first applied.

Interface board DC current requirement (5V):

LSI-11	2.9A max.
PDP-11	3.1A max.

FCC and VDE restrictions for conducted and radiated RFI are met in a properly grounded installation.

Mechanical:

Size: 17.5" wide, 5.25" high, 22.2" deep (rack)
17.9" wide, 5.25" high, 22.2" deep (table)

Weight: 65 pounds (2 floppies)
69 pounds (winchester/floppy)
67 pounds (winchester/tape)

(See Figure 1 or 2 for detailed mechanical information.)

Table top or rack mounting options (Add four pounds for rack mount.)

F. DISK DRIVE DATA

Drive Model	[1] Capacity (MB)	No. Cylinders	No. Heads	Rot. Latency	Avg. Access Time	[2] Data XFR Rate Max.	Avg.
SA1004	10.67	256	4	9.60	70	543	453
Q2020	21.33	512	4	10.00	55	543	453
Q2040	42.67	512	8	10.00	65	543	453
Q2080	85.00	1172	7	10.00	40	543	453
SA800	.80	77	1	83.30	205	31.25 S	20[3]
						62.50 D	49[3]
SA850	1.60	77	2	83.30	77	31.25 S	20[3]
						62.50 D	49[3]

Notes

[1] Unformatted capacity. See Table 8 for formatted capacities.

[2] Data transfer in KBytes/second. AVG. = Average across track.

[3] Assumes no interleave. A 2:1 interleave (e.g. RX02) would cut average transfer rate by two.

[4] S = single density; D = double density.

G. CARTRIDGE TAPE DATA

Type	Recording Density	Number of Tracks	Tape Speed	Fast Speed	Data Transfer Rate Bits/Sec	Capacity
K6455	6400BPI	4	30IPS	90IPS	192,000	21.6Mbytes (max)

MEDIA TYPE: 3M DC300, DC300XL, OR DC600A

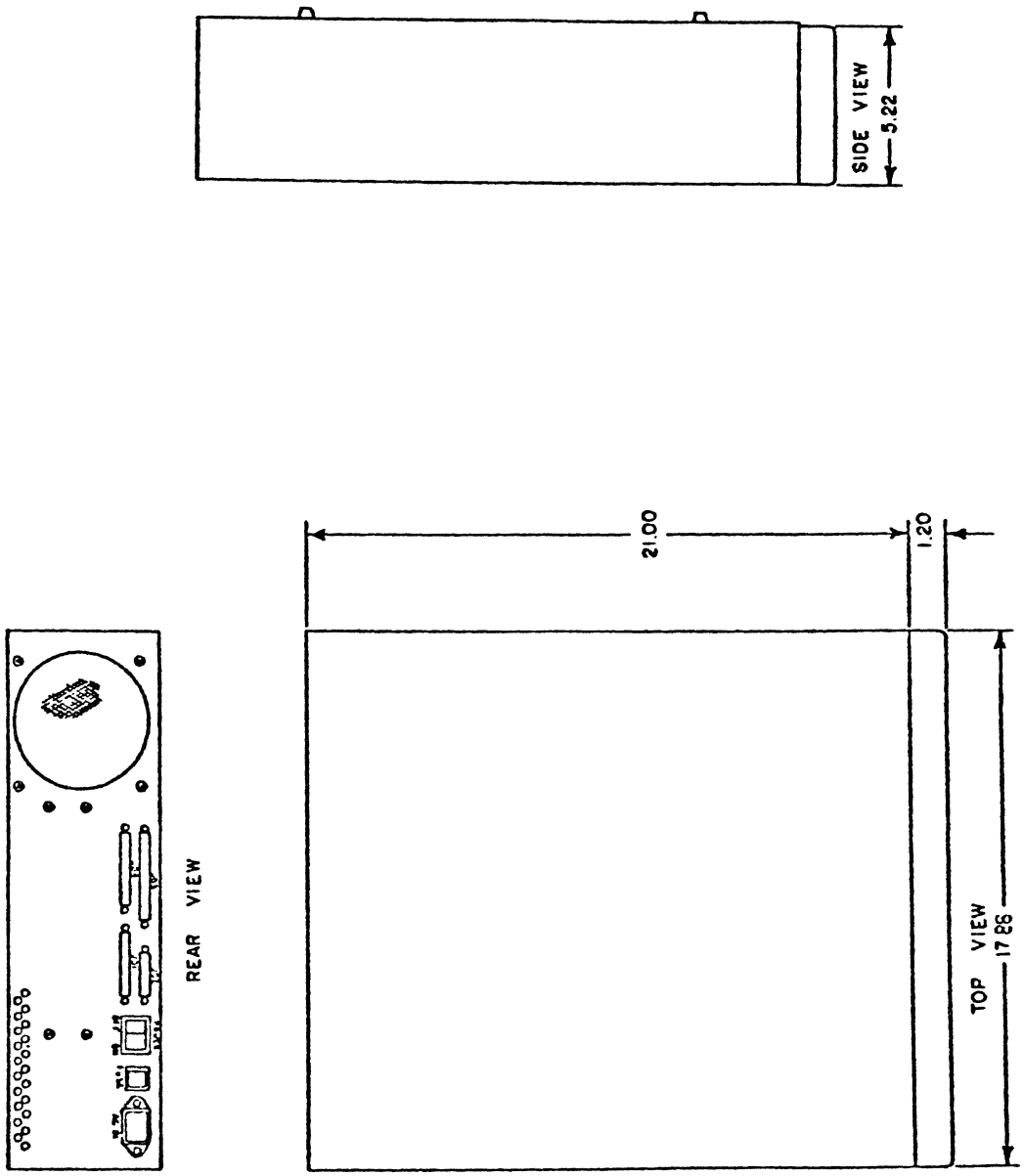


Figure 1. Enclosure Assembly, FWT System, Desk Top.

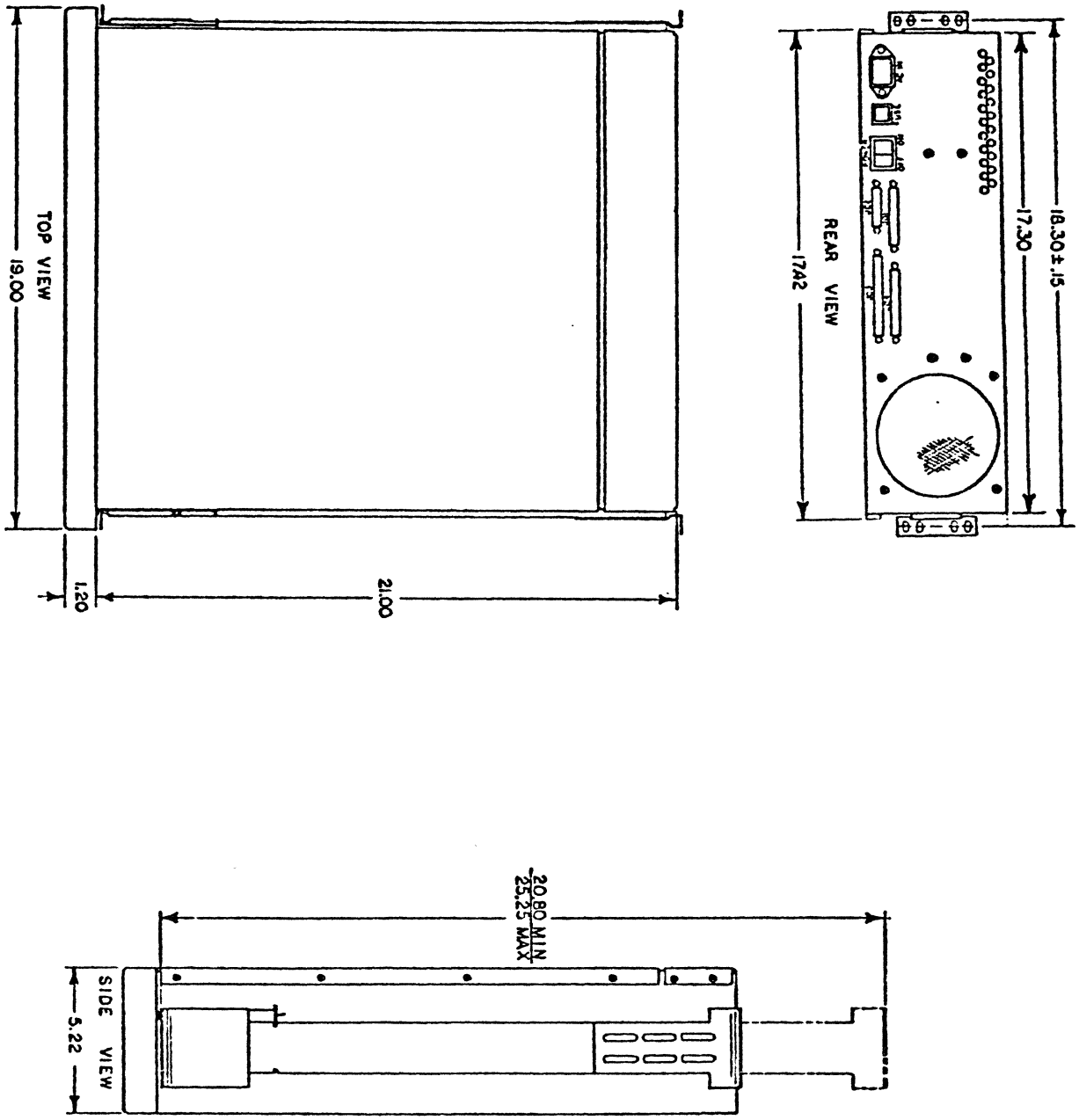


Figure 2. Enclosure Assembly, FWT System, Rack Mount.

II. SYSTEM INSTALLATION AND OPERATION

This section of the manual describes how to install, configure, and operate the disk system. It also describes what options are available in the system and how to select these options.

A. UNPACKING

Examine all shipping containers for evidence of damage prior to unpacking the equipment. If any damage is found, notify an authorized representative of the shipping concern before unpacking the equipment.

No special unpacking instructions are provided since the shipping containers are of a standard type and easily disassembled. All sub-assemblies are adequately protected from normal shocks incurred during shipping.

Visually inspect each assembly in the shipment for damage. Check each item against the packing list to ascertain that all items have been received.

B. SITE SELECTION

The site selected for the disk system must provide ample space around the unit to allow adequate circulation of cool air and easy maintenance accessibility. Under no circumstances should any cables, walls, or mounting hardware be allowed to restrict air flow to the fan on the rear panel. Proper ac voltage must be provided for the unit as described in the specification section. The normal office environment is adequate for satisfactory operation of the unit.

C. SYSTEM GROUNDING

As shown in the wiring diagram, Figure 3, signal ground is connected to the chassis at the terminal pc board, located on a side wall. The chassis is then connected to the ground wire of the ac input. It is imperative for safety reasons that ground continuity be provided at the customer's installation. This may be accomplished with a three wire installation.

D. WINCHESTER LOCKING MECHANISM

If your system has a Winchester disk drive in it, the spindle locking mechanism must be removed before power is applied. See documentation attached to your unit for instructions on how to remove the locking mechanism.

E. PLACEMENT OR MOUNTING

After unpacking the system enclosure, it should be positioned on a table or desk top within reasonable proximity to the host system and the required power source, or it may be rack mounted.

To accommodate rack mounting of the FWT system into a standard RETMA rack (per EIA RS-310 specifications), the system enclosure is equipped with slides mounted to the side of the unit. The slide brackets will adjust to a rack depth of 21 to 22 inches. They will also adjust at .50 inch increments up to a rack depth of 24.50 inches.

F. INTERFACE BOARD INSTALLATION

1) Insure the appropriate interface board straps are installed. See Table 1 (PDP-11) or Table 2 (LSI-11).

2) Install the interface board into the backplane. The placement selection depends on various system parameters, however, for Unibus installations, the Non-Processor Grant (NPG) and Bus Grant (BG4-BG7) signals must be daisy chained to the interface board from the CPU in order for the interface board to correctly arbitrate the bus. Therefore, all SPC slots between the PDP-11 processor and the interface board must be populated with either SPC's or Flip Chips. Since Flip Chips only complete the BG daisychain, those slots populated with Flip Chips must have NPGIN jumpered to NPGOUT (pin CA1 wired to CB1) on the Unibus backplane. The NPGIN to NPGOUT jumper at the interface board's SPC must be removed. If these requirements are not met, then the bus will hang whenever the interface board attempts a DMA or interrupt operation.

   For LSI-11 installation, there must not be any vacant slots between the interface board and the CPU board. If the LSI-11 computer occupies slot 1-A/B, then slot 1-C/D is the dual wide slot adjacent to slot 1-A/B. For cabling convenience, the disk controller interface board is typically installed in slot 1-C/D. Slots 2-C/D through 8-C/D may be used for any Q-BUS compatible boards. Because of cabling requirements, the cartridge tape interface board is typically installed in slot 2-A/B or slot 3-A/B. All boards must be inserted with the component side facing the disk drives.

3) Install the cable between the interface board connector (J06) and the chassis connector J04 on the rear panel.

G. CONTROLLER AND DRIVE OPTIONS

Certain strap options are provided on both the controller interface board, located in the backplane, and the controller formatter board, located under the hinged cover. These options are factory set to provide the most widely used system; however, the information is presented here to allow for special customer requirements and maintenance.

The interface board strap options are listed in Tables 1 and 2. Notice that all jumpers, if required, must be wirewrapped because of height restrictions.

The formatter board options are listed in Tables 3 and 4. The factory defaults are indicated with a double asterisk. In case of a drive failure, the floppy mapping switch may be used to logically reverse drive addresses 0 and 1.

H. AC POWER SWITCH AND FUSE

The only external switch on the FWT system is the AC power switch, which is located on the rear panel. Before turning AC power on, insure any Winchester locking mechanisms have been removed.

The AC power fuse is also located on the rear panel. The following are recommended fuse sizes for the various configurations.

115 VAC, 2 floppies	5.00A
230 VAC, 2 floppies	3.00A
115 VAC, 1 floppy, 1 Winchester	6.25A SLO BLO
230 VAC, 1 floppy, 1 Winchester	3.20A SLO BLO

TABLE 1. PDP-11 FW INTERFACE STRAPS.

INTERRUPT PRIORITY SELECTION (STRAP PACKS U76, U77)

PRIORITY	U76								U77							
LEVEL	S1	S2	S3	S4	S5	S6	S7	S8	S1	S2	S3	S4	S5	S6	S7	S8
**BR4	I	R	R	I	R	I	R	I	I	I	R	R	R	R	R	R
BR5	R	I	I	R	R	I	R	I	R	R	I	I	R	R	R	R
BR6	R	I	R	I	I	R	R	I	R	R	R	R	I	I	R	R
BR7	R	I	R	I	R	I	I	R	R	R	R	R	R	R	I	I

BOOT PROMS STARTING ADDRESS (STRAP PACK U40)

S2	S3	S4	
I	I	I	1600008
I	I	R	171000**
I	R	I	162000
I	R	R	173000
R	I	I	164000
R	I	R	175000
R	R	I	166000
R	R	R	177000

CSR ADDRESS (STRAP PACK U40)

S5	S6	S7	S8	
I	I	I	I	1770408
I	I	I	R	177060
I	I	R	I	177050
I	I	R	R	177070
I	R	I	I	177140
I	R	I	R	177160
I	R	R	I	177150
I	R	R	R	177170**
R	I	I	I	177240
R	I	I	R	177260
R	I	R	I	177250
R	I	R	R	177270
R	R	I	I	177340
R	R	I	R	177360
R	R	R	I	177350
R	R	R	R	177370

INTERRUPT VECTOR (STRAP PACK U40)

S1 REMOVED - 2708
INSTALLED - 264_8**

W1 BOOT PROM DISABLE*

REMOVED - BOOT PROM'S ARE ENABLED **
INSTALLED - BOOT PROM'S ARE DISABLED

NOTE: I = INSTALLED = 0 = CLOSED
R = REMOVED = 1 = OPEN

* Wirewrap must be used here or height restrictions will be violated.
** Double asterisk indicates factory option.

TABLE 2. LSI-11 FW INTERFACE STRAPS

STRAP NUMBER	MEANING
W1	*BOOT PROM'S DISABLE
	** REMOVED - BOOT PROM'S ARE ENABLED
	INSTALLED - BOOT PROM'S ARE DISABLED, (CONTROLLER WILL NOT RESPOND TO BOOT PROM ADDRESS)
W2, W3	*PARITY CONTROL
	W2 INSTALLED - PARITY ENABLED
	** W3 INSTALLED - PARITY DISABLED
W4 - W9	INTERRUPT PRIORITY

	W4	W5	W6	W7	W8	W9
BR4	R	R	R	R	I	I
BR5	I	R	I	R	R	I
BR6	I	I	R	I	R	R

NOTE: THE LSI-11 I/F BOARD CANNOT BE CONFIGURED AS A BR7 DEVICE, HOWEVER IT DOES RECOGNIZE OTHER BR7 DEVICES AS SUCH, AND CORRECTLY ARBITRATES INTERRUPTS WHEN BR7 DEVICES ARE PRESENT.

S1 (U42) INTERRUPT VECTOR SELECTION

REMOVED - 270_8

** INSTALLED - 264_8

S2-S4 (U42) BOOT PROM'S STARTING ADDRESS

	S2	S3	S4			S2	S3	S4	
	I	I	I	160000_8		R	I	I	164000_8
	I	I	R	171000		R	I	R	175000
	I	R	I	162000		R	R	I	166000
**	I	R	R	173000 (DEFAULT)		R	R	R	177000

S5-S8 (U42) CONTROLLER COMMAND AND STATUS REGISTER ADDRESS

	S5	S6	S7	S8		S5	S6	S7	S8	
	I	I	I	I	177040_8	R	I	I	I	177240_8
	I	I	I	R	177060	R	I	I	R	177260
	I	I	R	I	177050	R	I	R	I	177250
	I	I	R	R	177070	R	I	R	R	177270
	I	R	I	I	177140	R	R	I	I	177340
	I	R	I	R	177160	R	R	I	R	177360
	I	R	R	I	177150	R	R	R	I	177350
**	I	R	R	R	177170 (DEFAULT)	R	R	R	R	177370

* Wirewrap must be used here or height restrictions will be violated.
** Double asterisk indicates factory option.

TABLE 3. FW FORMATTER SWITCHES

SWITCH	MEANING		VALUES	
1-2	SELF TEST SEE SECTION V-B FOR SELF AND DRIVE TEST DESCRIPTION		1 2	
			C C	NO SELF TEST IS RUN
		**	C O	SELF TEST RUN ONCE AT POWER ON OR INITIALIZATION
			O C	SELF TEST RUN CONTINUOUSLY
			O O	DRIVE TEST
3	FLOPPY TYPE		C = SHUGART 850 OR EQUIVALENT	
			O = SHUGART 800 OR EQUIVALENT	
4	FLOPPY MAPPING	**	C = NO MAPPING	
			O = DRIVES LOGICALLY REVERSED	
5	FLAW MAP (SEE SECTION VI)		C = FLAW MAPPING NOT TO BE DONE BY THE CONTROLLER	
		**	O = THE CONTROLLER WILL MAP FLAWS	
6-8	WINCHESTER DRIVE TYPE		6 7 8	
			C C C	SHUGART SA1002
			C C O	SHUGART SA1004
			C O C	QUANTUM Q2010
			C O O	QUANTUM Q2020
			O C C	QUANTUM Q2080*
			O C O	QUANTUM Q2040
			O O C	NOT USED
			O O O	NOT USED

* Earlier versions of the disk controller used this setting for Q2030 Winchester disks.
** Factory Option

TABLE 4. FW FORMATTER STRAPS

FWD0101 FORMATTER

STRAP NUMBER	MEANING
W1	NUMBER OF WORDS TO TRANSFER PER DMA BURST ** REMOVED - 4 WORD BURST INSTALLED - 2 WORD BURST NOTE: NORMALLY A 4 WORD BURST IS USED FOR LSI-11 AND A 2 WORD BURST IS USED FOR THE PDP-11. THIS STRAP MUST BE INSTALLED WHEN THE HOST COMPUTER IS THE VAX.
W2	RESERVED - MUST BE INSTALLED NOTE: FORMATTER BOARDS WITH PROGRAM ASSEMBLY 1001943 REV. OR LATER PERFORM SINGLE SIDED PRECOMPENSATION REGARDLASS OF THE STRAP SETTING. SMS STILL RESERVES THE STRAP FOR FUTURE USE.
W3	DOUBLE SIDED FLOPPY WRITE PRECOMPENSATION FOR DOUBLE DENSITY DISKETTES REMOVED - NO PRECOMPENSATION ** INSTALLED - PRECOMPENSATION DONE
W4	WINCHESTER WRITE PRECOMPENSATION REMOVED - NO PRECOMPENSATION ** INSTALLED - PRECOMPENSATION DONE
W5	TEST AID - MUST BE REMOVED
W6,11	TEST AID - MUST BE INSTALLED
W7-W9,W12	TEST AID - MUST BE REMOVED
W10	POWER UP AND INITIALIZE MODE REMOVED - COMPATIBLE MODE SET ON POWER UP AND BUS INIT. ** INSTALLED - MODE IS NOT SET ON POWER UP OR CHANGED ON A BUS INIT. NOTE: AFTER POWER ON OR BUS INIT, THE MODE CAN BE PROGRAMMATICALLY CHANGED. ONLY THOSE SYSTEMS WHICH ARE FLOPPY ONLY AND DO NOT USE THE SMS BOOTSTRAP WILL NEED THIS STRAP REMOVED.

** Factory Option

TABLE 5. DRIVE OPTIONS AND SPECIFICATIONS

SHUGART SA800

DRIVE	JUMPER
**DRIVE 0	DS3,X,Y,A,T1,T2,800*,HL,J1 PIN 6 TO C POST
**DRIVE 1	DS4,X,Y,A,T1,T2,800*,HL,D POST (J1 PIN 16) TO C POST.

If the L jumper is present (latest SA800 revisions do not require a negative voltage), it should be installed. No other jumpers are to be implemented.

SHUGART SA850

DRIVE	JUMPER
**DRIVE 0	A,X,Y,R,I,C POST TO J1/6 AND TO H POST***,S2,2S,DS3,850,HL,IT,RM, IWI (NOT TO GND),M
**DRIVE 1	A,X,Y,R,I,D POST (J1 PIN 16) TO C POST AND TO H POST***,S2,2S,DS4, 850,HL,IT,RM,IWI (NOT TO GROUND),M.

DD, RR, and RI are etched on the pc board and are assumed to be connected. Z and B are connected via straps at location 4F on the drive and should be cut. No other jumpers are to be implemented.

SHUGART SA1000

Install the folowlowing jumpers:

DS1,Voltage selection (-5), terminator pack at location 8C.

QUANTUM Q2000

Install the folowing jumpers:

DS1,Voltage selection (-5), terminator pack at location 6J.

*The 800 strap is only applicable to level 4 boards.
**For the FWD0101 formatter, floppy drives 0, 1 are physically optioned as drives 2,3 (DS3, DS4) since the Winchester is on the same control cable.
***The H post is connected to the IT jumper on the pc board and the C post is connected to the X strap on the pc board.

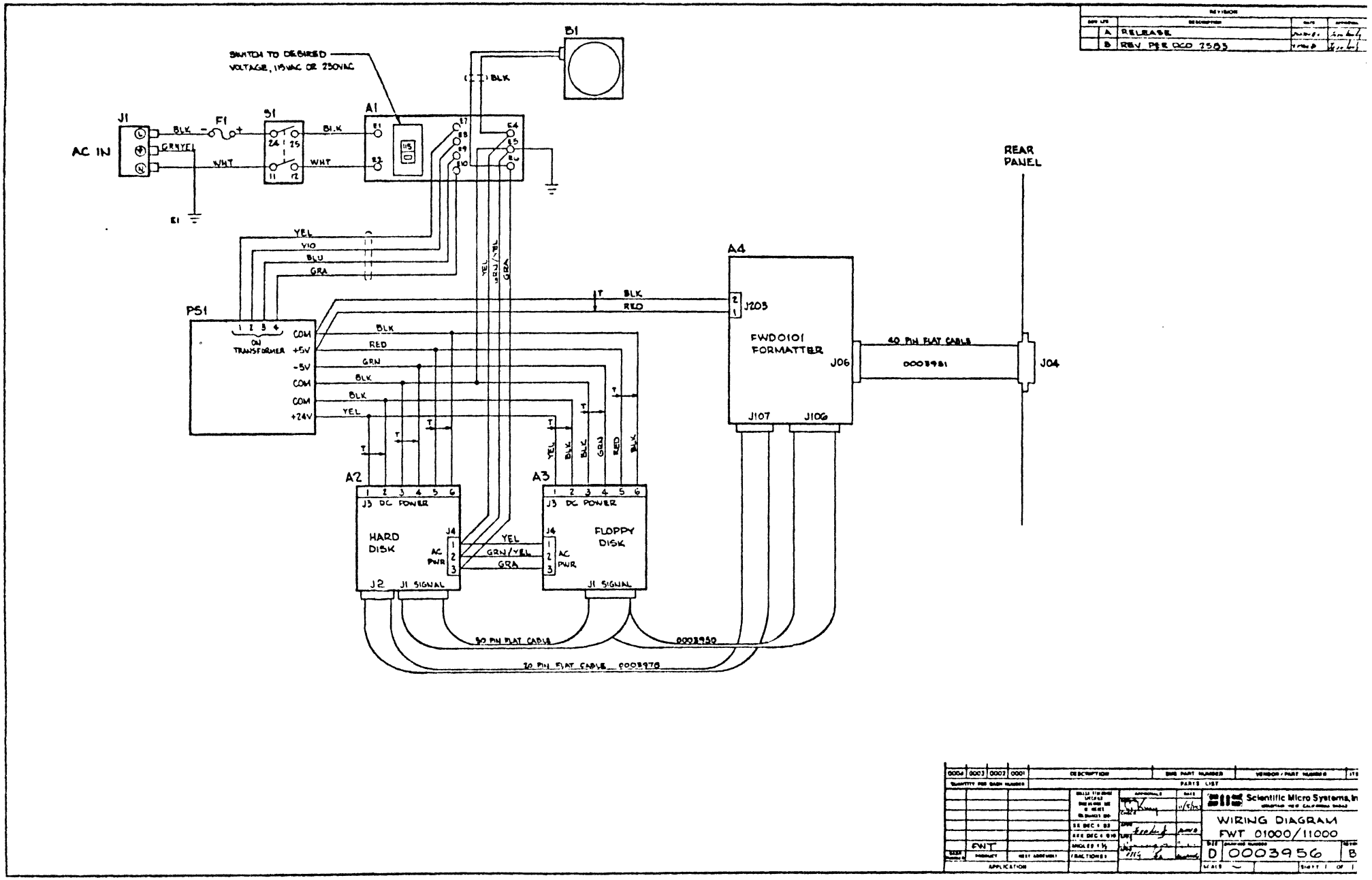


Figure 3. FWT System Wiring Diagram

I. BOOTSTRAPPING (PROGRAM LOADING FROM DISK)

In order to load a software program from the floppy or Winchester disk, the FW controller provides a bootstrap program. This bootstrap program, plus limited CPU and memory diagnostics, resides in PROMs on the interface board and normally occupies the address range from 773000_8 to 773777_8 for the LSI-11, and 171000_8 to 171777_8 for the PDP-11.

The basic operation of the boot program is to read 512 words from the first block of the specified drive into host memory, starting at address 0, and then cause the host CPU to start execution at address 0. The program read into memory from the first block of the drive then reads the remainder of the program being booted, and thus is often called the boot block.

The simplest and most convenient way to start the FW boot program when the LSI-11 CPU is in power-up mode 2 (see the DEC Microcomputer Processor Handbook) is to cause a bus reset (cycle DC power). This causes the CPU to start execution at a specified address, typically 773000_8. Another way is to use the console ODT 'G' command. The console emulator provides a convenient way to boot the system when the PDP-11 is the host computer.

For example, the FW Installation and Test program can be booted as follows (See Section IV for booting from tape):

LSI-11 Power-Up Mode 2

1) place diskette in drive 0 (or drive 1)
2) push Reset
3) wait for the DRV (F0, W0 OR T)? prompt
4) type F0 (or F1 in upper case)

LSI-11 Using Console ODT (@ sign is prompt)

1) place diskette in drive 0
2) push the break key on the terminal keyboard
   (the @ prompt should be printed)
3) type 773000G
4) wait for the DRV (F0, W0 OR T)? prompt
5) type F0 (in upper case)

PDP-11 Using Console Emulator ($ is console emulator prompt)

1) place the diskette in drive 0
2) type L771000
3) type S
4) wait for the DRV (F0, W0 OR T)? prompt
5) type F0 (in upper case)

The program will then be read from the disk and its execution started.

In order to allow for different system configurations, there are two entry points for this program -- the base address or the base address plus 20_8. The base address is normally 773000_8 or 771000_8, but may be changed or disabled. When the program is started at the base address, the following functions are executed by it:

1) Exercise host CPU

2) System memory sizing and testing

3) Boot device I/O address is tested

4) A set extended mode command is issued to the controller (if it is not already in extended mode)

5) Bootstrap prompt DRV (F0, W0 OR T)? is written to the console device

6) The user then responds with one of the following (upper case alphanumerics must be used):

F0	floppy drive 0	W0	Winchester drive 0
F1	floppy drive 1	W1	Winchester drive 1

Note that these are logical addresses. The physical address of the drives may be different as shown in Tables 5 and 6.

If the operator responds with one of the above prompts before the timeout expires, the controller will attempt to read 512 words from the device starting at host address 0 and disk address sector 1, track 1, head 0 for the floppy, and sector 1, track 0, head 0 for the Winchester. If the read is unsuccessful, or if host address 0 does not contain a NOP after the read, the boot program will halt.

If a successful read was from F0 or F1 and if the format of the diskette is RX01 or RX02, then the controller is issued a set compatible mode command. Host program execution is then started at address 0. It is assumed that the bootstrap block contains a valid program and that it will change the controller's mode if required.

When the bootstrap program, loaded from the first block of the disk, is started, R0 contains the unit number that the bootstrap block was read from:

R0 = 0	floppy drive 0	R0 = 2	Winchester drive 0
R0 = 1	floppy drive 1	R0 = 3	Winchester drive 1

If, after about 5-10 seconds, no response has been entered to the DRV (W0,F0,T)? prompt, the controller will search all drives for a valid bootstrap block. The search order is W0, W1, F0, F1*. If, after several minutes* of trying, no valid bootstrap block is found, the program will halt to prevent excessive media wear

*Earlier versions of the bootstrap program selected the floppy disks and then the Winchesters when performing an automatic bootstrap. Auto boot from cartridge tape is not supported because most systems include a disk. You can force a boot from tape by responding T to the prompt.

in unattended operations. If a valid bootstrap block is found, it is read into host memory and program execution started just as above.

Note: Typically the controller should be strapped for not setting the mode at power up. This allows extended mode operation — including bootstrap from the Winchester — as well as bootstrap of standard DEC software from the floppy.

The bootstrap and diagnostic program is started at the second entry point when the default I/O addresses are to be overridden. The second entry assumes:

Memory Address	Contents
0	FW controller base address (default 177170_8)
2	Console terminal base address (default 1775608)
4	0 for normal drive searching as above. No drive searching is done if this word is non-zero. This word contains the unit designator word described in section IV-F. This allows bootstrapping from any unit in any format.

Error Reporting

The bootstrap program reports all errors, either by halting or by waiting indefinitely for an event to occur. The program counter (PC) value thus indicates what the error is. Table 6-A details the various error stops.

J. OPERATION WITH THE WINCHESTER DRIVE

The Winchester drive is a simple and very reliable device. It does not require any normal preventive maintenance, however a few precautions must be taken when power is first applied.

1) Most Winchester drives have a spindle locking device (e.g. Shugart SA1000), and some have both a spindle locking mechanism and a carriage locking mechanism (e.g. Quantum Q2000). Be sure to unlock these mechanisms before turning power on.

2) All Winchester drives require a period of time to reach operational speed. When the drive is at speed, it outputs a signal called Ready and will allow disk accesses to take place. The Shugart SA1000 takes less than 10 seconds to become ready.

3) When first applying power, the drive may be cold. As the drive warms up, some thermal expansion will take place. As a result, it is recommended that the drive not be formatted or written to until after AC power has been applied for two minutes.

K. FCC RULES AND REGULATIONS INFORMATION

SMS has conducted preliminary testing on this chassis to determine if it complies with FCC Rules and Regulations. The chassis by itself does meet all requirements for a Class A computing device. However the flat ribbon cable which attaches the chassis to the host computer causes the unit as a whole to not comply with the Class A radiation limit. The cable causes the unit to exceed the radiation limit at one frequency by about 10%. The unit does meet all conduction requirements. If a fully shielded cable is used or if the unit is housed in a metal enclosure (e.g. rack mount) the unit will comply with the Class A radiation limits. Please contact SMS for test results or further information.

TABLE 6-A. BOOTSTRAP PROGRAM HALT LOCATIONS

Note: All of the following addresses are relative to the base address of the bootstrap program. Normally the base address of the bootstrap program is 173000_8 or 171000$_8$.

Relative Address	Error
0-150	Host CPU Failure
140,142 or 650,660	Enter Compatible Mode Failed*
164 or 166	Fill Buffer Command failed
216 or 220	Empty Buffer Command failed
214,242 or 246	Memory Test failed on write of all 1's. R2 points to failed location.
224,252 or 256	Memory test failed on write of all 0's. R2 points to to failed location.
250,252 or 324,353,356	Enter Extended Mode failed
274,322 or 326	Memory Access error at controller CSR address (i.e., could not read CSR)
426 or 452	No valid bootstrap block could be found

* Possible CPU failure, however more probable that a controller error occurred.

TABLE 6-B. BOOTSTRAP PROGRAM HANG LOCATIONS

If the boot program does not start after waiting about 30 seconds, push the break key to determine the 'hang' location. Typically these errors indicate faulty system configurations and/or controller problems.

Relative Address	Error
24-34	Waiting for TR, Done or Error to be set on CSR
54-60	Waiting for Done or Error to be set in CSR
264,312-320	Waiting for Done to be set after a RESET
650-716	Waiting for TR, Done or Error to be set in CSR

III. DISK SURFACE MANAGEMENT AND FORMATS

A. DISK SURFACE LAYOUT

The surface of a disk (both floppy and fixed) is divided into a series of concentric circles. Each one of these circles is called a track. As the disk rotates, a track passes under a read/write head which is used to transfer information from/to the disk. Many disk drives support multiple read/write heads, all of which are mounted on a single carriage. The carriage moves or positions the heads over the disk surface. On drives which support multiple heads, all tracks which can be accessed from one position of the carriage are called a cylinder. Thus a cylinder consists of 1 to N tracks where N is the number of read/write heads mounted on the carriage. The concept of cylinders is important because switching from one head to another is very fast when compared to physically moving the carriage.

Each track is divided into several records called sectors. The sectors are numbered from 1 to X where X is the number of sectors per track. The number of sectors per cylinder is thus X times the number of heads. All sectors on one cylinder are of the same size.

B. DISK SURFACE ADDRESSING

The surface of either the floppy or fixed disk can be accessed using a physical address or a logical address.

A physical address is one which specifies a sector position by naming the head, cylinder and sector number. Note that the head number specifies a track within the cylinder. Note also that cylinder and head numbering starts at zero while sector numbering starts at one.

A logical address is one which specifies a sector position by using a logical sector number only. When logical addressing is used, the storage area can be viewed as sequential series of sectors on the entire disk. The advantage of using logical addressing is that it is independent of disk flaws and interleave factors. For example, if logical sector K is read, then the next logical record is K+1 even though physically it may not be on the same cylinder as sector K. If the fixed disk has a fixed head option installed, physical addressing must be used to access the fixed head area. Logical addressing is for the moving heads only.

Logical addressing starts with logical record one for both the floppy and Winchester drives. However logical record one is equivalent to cylinder 1, head 0, sector 1 for the floppy (i.e. logical addresses start at cylinder 1, not cylinder 0 for the floppies), and equivalent to cylinder 0, head 0, sector 1 on the Winchester assuming there are no flaws.

If the Winchester has flaws then logical record 1 will be the first non-flawed sector on the disk.

Cylinder 0 on the floppies can be accessed using physical addressing only.

C. SECTOR INTERLEAVING

When sector interleaving is used, consecutive sectors on a disk are never read or written. Interleaving typically does not affect disk storage capacity, but does affect system throughput and performance.

Interleaving is used to simplify controller design and/or reduce the effective data transfer rate. Interleaving can be accomplished logically by host or controller software, or physically when the disk is formatted.

The DEC RX02 system uses a logical 2:1 interleave. The interleave is accomplished by the device handler (i.e. DY.MAC in RT-11 V3B). The interleave is required because the DEC RX02 controller cannot read/write more than one sector at a time. The time gained by skipping a sector is used to process the status from the previous command and issue the next command. Conversely, some IBM systems use physical interleaving.

The controller does not require any interleave when accessing a floppy drive and most Winchester drives. Recommended interleaves for the various drives are given in section IV-G, Format commands. In order to be compatible with other systems and allow reduced data rates, a physical interleave can be specified when either the fixed or floppy disk is formatted.

When interleaving is used, any physical offset (see next section) and interleave are not additive. The number of sectors skipped is the greater of the offset and interleave factor.

D. CYLINDER OFFSET

Cylinder offsetting is a technique used to improve system performance on transfers crossing cylinder boundaries.

To understand how cylinder offsetting works it is necessary to look at the timing constraints of a disk drive. A disk drive can take from 10 to 20 msec to move a read/write head from one cylinder to the next. If a transfer is taking place such that the last sector on track X has just been read and the next sector to be read is the first sector on track X+1, it is desirable to be able to read this sector as soon as the head has been positioned over track X+1. Typically this is not possible because step time is greater than the delay provided by the disk rotation. Thus the controller must wait an entire rotation (167 msec for floppies) before the desired sector can be read.

This product provides offsets on both the fixed and floppy disks to improve system performance. The offset for the floppy can be either a physical offset done at format time, or a logical offset selected programmatically when the data is read or written. When using logical offset and/or interleave, the data must be read and written using the same offset/interleave.

E. FLOPPY DISK TRACK FORMATS

This controller supports the DEC RX01/RX02 (single/double density) formats, and the IBM single/double density formats. All of these formats are 'soft-sectored' formats. This means that the position of each sector on a track is marked by the controller writing a special pattern, called an address mark (AM), on the diskette. The address mark, along with other identification data (track, head, sector and format), is written only when the diskette is formatted. In normal reads/writes only the data, data address mark and data CRC bytes are written.

It is important to distinguish between what 'formatting' a diskette means versus how the data is arranged on the diskette. Format implies what the encoding type is, what address marks are used and how many bytes per sector there are. On the other hand, data can be arranged on the diskette using various interleave and offset factors.

Diskette formats can be divided into three basic categories:

1) IBM Single Density

2) IBM Double Density

3) DEC Double Density

IBM single density is equivalent to DEC RX01 single density in regards to the format. However DEC RX01 also implies a 2:1 interleave and 6 sector offset. The IBM single density format implies frequency modulation (FM) encoding and single byte address marks.

The IBM double density format implies Modified Frequency Modulation (MFM) and four byte address marks.

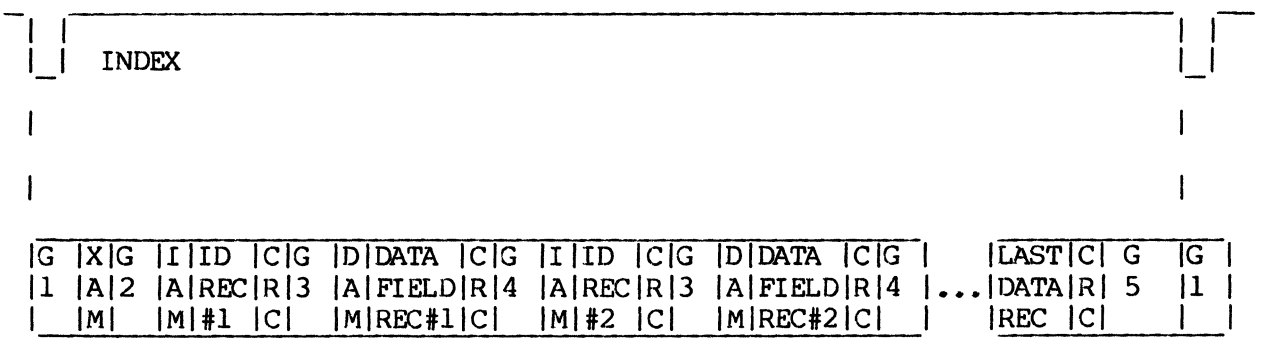
The DEC RX02 double density format uses FM encoding for the identification field (i.e. the ID's written at format time are identical to IBM single density, 128 bytes/sector) and a slightly modified MFM for the data fields. DEC RX02 also implies a 2:1 interleave and 6 sector offset.

The IBM formats have one other important feature — the format of the first track is constant regardless of the format of the remainder of the diskette. The format for cylinder 0, head 0 is IBM single density, 128 bytes/sector. If the diskette is double sided cylinder 0, head 1 can be one of two formats only. These are single density, 128 bytes/sector if the remainder of the diskette is single density or double density, 256 bytes/sector if the remainder of the diskette is double density.

The following table summarizes the aspects of the various formats:

Density	Encoding	Bytes/ Sect.	Sect./ Track	Gap 4	Gap 5	Implied Data Arrangement
IBM SD	FM	128	26	33	274	None
		256	15	48	212	
		512	8	72	313	
		1024	4	86	667	
DEC SD	FM	128	26	33	274	2:1 sector interleave, 6 sector offset
IBM DD	MFM	128	44	50	277	None
		256	26	66	653	
		512	16	61	352	
		1024	8	128	771	
DEC DD	FM, Modified MFM	256	26	33	274	2:1 sector interleave, 6 sector offset

The arrangement of sectors, ID, etc. on each floppy track is shown below:



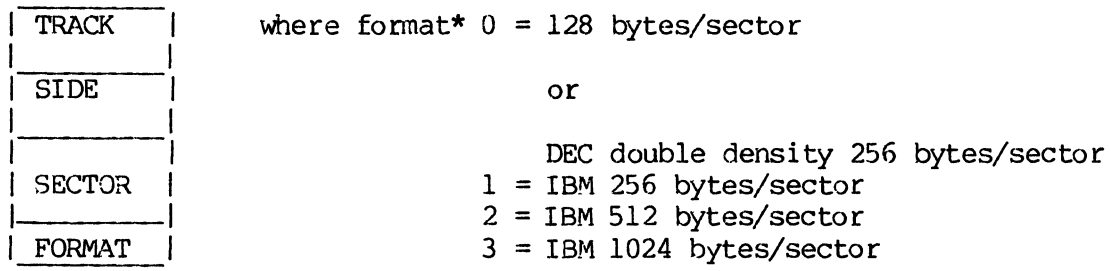
where G1 to G5 is GAP1 to GAP5
XAM is Index Address Mark (1 byte in single density,4 in double density)
IAM is ID Address Mark (1 byte in single density, 4 in double density)
ID REC is ID Record (4 bytes)
DAM is Data address mark (1 byte in single density, 4 in double density)
CRC is Cyclic Redundancy Check (2 bytes)
Gaps 1,2 and 3 are fixed and have the following values:

	Gap 1	Gap 2	Gap 3
IBM Single Density/RX02 Double Density	46	32	17
IBM Double Density	92	62	34

Gaps 4 and 5 vary depending on the diskette format and drive tolerance.

The nominal values for these gaps are shown above.

Each ID record consists of 4 bytes in the following format:

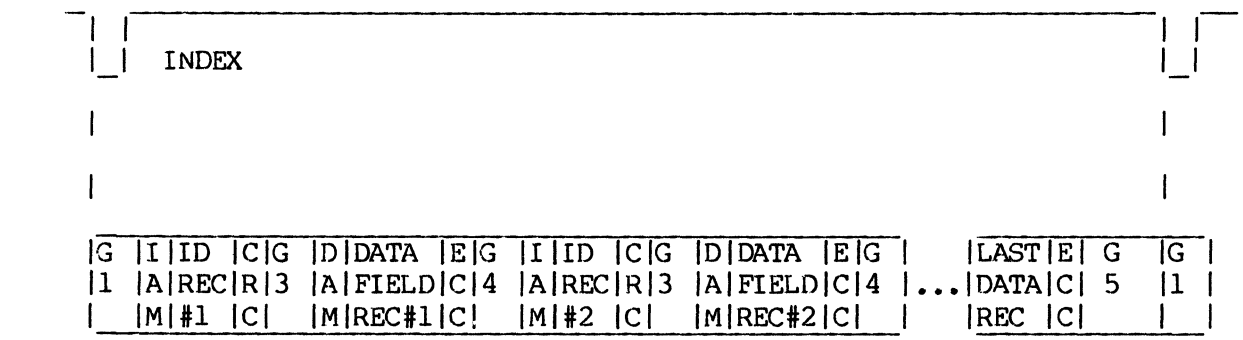


*Note: Different data address marks are used to distinguish between DEC single and double density.

F. FIXED DISK TRACK FORMAT

Shugart SA1000/Quantum 2000

The SA1000 and Q2000 drives are soft sectored Winchesters and their track formats are similar to the floppy disk except that there is no index address mark (XAM) or gap 2 (G2). This means that gap 1 immediately precedes the ID address mark for sector 1. It should also be noted that the 2 byte data CRC which is used on the floppy disk is replaced with a 3 byte data ECC capable of detecting all 10 bit (or fewer) burst errors, and correcting up to a 6 bit burst error. The arrangement of sectors, ID, etc., on each track is shown below:



where G1 to G5 is GAP1 to GAP5
IAM is ID Address Mark (3 bytes)
ID REC is ID Record (3 bytes)
DAM is Data address mark (4 bits)
CRC is Cyclic Redundancy Check (2 bytes)
ECC is Error Correction Code (3 bytes)
Gap 1 is fixed at 18 bytes (includes sync bytes which precede AM)
Gap 3 is fixed at 14 bytes (includes sync bytes which precede AM)
Gap 4 and Gap 5 depend on format (see Table 7).

Each ID record consists of 3 bytes in the following format:

FORMAT	HEAD
CYL	SECTOR
CYLINDER	

where format 01 = 32 256 byte sectors/track
05 = 31 256 byte sectors/track
02 = 17 512 byte sectors/track
06 = 16 512 byte sectors/track

Due to the fact that there is no clock track on the SA1000/Q2000, rotational velocity variation, caused by drive tolerances and AC power fluctuation, will result in changes in the gap size after the data has been overwritten. The users choice of format must then reflect the particular line frequency variation in his area of use. SMS feels that any of the formats shown in Table 7 may be used without sector interleave with U.S. domestic AC power.

TABLE 7. SA1000, Q2000 FORMAT SELECTION

BYTES/ SEC.	SEC./ TRACK	SPEED TOL. W	SPEED TOL. W/O	GAP 4 '00'	GAP 5 '4E'	WR	SL
256	32	1.59%	2.83%	34	323	0	01
256	31	3.30%	3.50%	44	339	1	01
512	17	2.90%	3.50%	57	343	1	10
512	16	3.50%	3.50%	93	398	1	10

Key: W Rotation to rotation tolerance with write to read recovery time provided, (i.e. used for consecutive sectors).

W/O Rotation to rotation tolerance without write to read recovery time provided, (i.e. used for interleaved sectors).

WR,SL The write to read (WR) recovery time and sector length (SL) are specified in the disk format descriptor parameter when the disk is formatted. See section IV-F, Disk Format Designator for Winchester drives.

TABLE 8. WINCHESTER FORMATTED CAPACITIES (RECOMMENDED FORMAT)

SA1000, Q2000

Bytes/ Sector	Sectors/ Track	Track Capacity	Formatted Disk Capacity (MBytes) SA1004/ SA1002	Q2010	Q2020	Q2040	Q2080
512	17	8704	4.5	8.9	17.8	35.6	71.2

G. ERROR DETECTION AND CORRECTION

Both error detection and correction are widely used in computer memory systems to increase the reliability of the computer systems. Error detection and correction both involve recording redundant information. In the case of error detection, the redundant information is used to detect errors. With error correction the information is used to detect and, if possible, correct errors.

Error detection and correction codes are not infallible. All error detection codes have a small, finite probability of not detecting an error. All error correction codes have a small, finite probability of not detecting an error and, if an error is detected, of miscorrecting (i.e. a correction is done incorrectly and no error is reported).

For floppy disks the most widely used code is the code introduced by IBM on its floppy disk. This code, commonly referred to as Cyclic Redundancy Check (CCITT CRC), has excellent detection properties and some correction capabilities. It is sixteen bits in length and is recorded at the end of each sector.

In the FWD0101 formatter both error detection and error correction are supported. The code used for the Winchester drives is a 24 bit code which can correct any error burst up to six bits in length and detect any error burst up to ten bits in length. In order to minimize the miscorrection probability, error correction is not attempted until the ECC residue is identical for two successive reads. (See section IV-A, Error Correction Policy, for details.)

The floppy code, of course, continues to be the CCITT CRC. However, this code is capable of correcting all single bit errors and thus error correction is supported on the floppy also. SMS, however, does not recommend its use in normal operation. This is due to the fact that the probability of a miscorrection is significant when multiple bit errors occur. Error correction on the floppy is intended to be used as the last part of an error recovery procedure. If a diskette is unreadable, SMS recommends that an attempt be made to copy the bad file (or sector) with floppy correction enabled. (SMS' Installation and Test Program supports this feature.)

Error correction when compared to error detection, given the same code length, increases the probability of correctly recovering data on the disk.

The use of error correction on the Winchester disk is recommended by SMS. The error correction code has been carefully designed to allow both correction and detection in normal use. However, the use of error correction does not eliminate the need for flaw mapping sectors with known flaws. This is so because if a second hard error were to develop on a sector with a flaw, then the probability of detecting and correcting this second error is significantly lower than detecting and correcting it on a sector with no flaws. Systems which use both flaw mapping and error correction will show increased reliability over those which do not use these features.

IV. CARTRIDGE TAPE

A. INTRODUCTION

The FWT Storage Systems can be configured with a 1/4 inch start/stop cartridge tape drive that provides low-cost bulk storage. The tape drive is a Kennedy Model 6455 connected to the LSI-11 Q-BUS by the TS0100 interface board, or the PDP-11 UNIBUS by the TS1100 interface board. These boards emulate the DEC TSV05 or TS05 tape controllers, respectively. These interface boards support existing applications without modification.

Each interface board is a single, dual height board that plugs directly into a bus slot, and includes a self contained bootstrap program. The TS0100 board fully supports 22-bit Q-BUS systems and the LSI-11/23 multipriority interrupt structure.

B. MEDIA AND CAPACITY

SMS recommends the use of standard 3M DC600A (600'), DC300XL (450'), and DC300A (300') tape cartridges. Cartridge tapes do not have to be formatted.

The capacity of a cartridge tape depends on the length of the tape and the size of the blocks. Block size affects the tape capacity because stopping and starting the tape between write operations leaves gaps of unused tape. The effect of block size is shown below:

BLOCK SIZE	CAPACITY 450 FT. TAPE	CAPACITY 600 FT. TAPE
.5KB	5.90MB	7.80MB
1KB	8.80MB	11.70MB
2KB	11.67MB	15.50MB
4KB	13.90MB	18.50MB
8KB	15.40MB	20.50MB
16KB	16.20MB	21.60MB

Different software programs and utilities use different block lengths, which affects the capacity of the tape:

SOFTWARE PROGRAM	BLOCK SIZE
FW INSTALLATION & TEST	16KB
BRU (RSX-11M)	4KB
COPY (RT-11)	.5KB
COPY/DEV (RT-11)	1KB
PIP (RSX-11M)	.5KB

C. FRONT PANEL OPERATION

The front panel has three switches and three LED indicators:

SWITCH	FUNCTION
ON LINE	This momentary contact switch places the tape drive on or off line. If the drive is on line (ON LINE LED is lit), the drive is available to the system. Pressing this switch takes the drive off line and winds the tape to the end of the tape. If the drive is off line (ON LINE LED is dark), pressing this switch brings the drive on line and rewinds the tape to its beginning.
300/450 or 600	This two-position switch identifies the media type being used so that the drive can compensate for the different magnetic properties of 600' tapes. Be sure to set this switch to correspond with the length of the tape being used.
OPER/TEST	This switch is normally left in the OPER (operate) position. Use the TEST position only for off-line testing. Test procedures are described in Section F.

LED	MEANING WHEN LIT
ON LINE	The tape drive is on-line and available for access.
IN USE	The tape is moving to perform a read, write, wind, or rewind operation.
ERROR	An error has occurred. Error conditions and test procedures are described in Section F.

The LED indicators are also used to display error codes during test procedures. See section F.

D. USING THE TAPE DRIVE

Use the following procedures for normal tape operation:

1) Be sure that the OPER/TEST front panel switch is in the OPER (operate) position.

2) Check the length of the tape to be used and set the 300/450 or 600 front panel switch to the corresponding position.

3) Check the position of the write-protect plug on the tape cartridge. When the plug is in the SAFE position, the system can read the tape but cannot write to it.

4) Insert the cartridge into the open slot of the tape drive.

5) Press the ON LINE switch. The tape drive immediately rewinds a newly inserted cartridge to the beginning of the tape. The rewind operation takes from five seconds to four minutes, depending on the tape length and the position of the tape within the cartridge. The IN USE LED remains lit while the tape rewinds.

6) When the rewind completes, only the ON LINE LED remains lit to indicate that the drive is available to the system.

7) Do not press the ON LINE switch while the tape is in use. Pressing the switch takes the tape drive off line and winds the tape to the end.

9) Most users prefer to store tapes either fully rewound or wound to the end. To rewind the tape to the beginning, do the following:

- o Remove the cartridge.
- o Insert the cartridge back into the drive.
- o Press the ON LINE switch.
- o Wait for the IN USE indicator to go dark.
- o Remove the cartridge and store it safely.

10) To store the tape wound to the end, do the following:

- o Press the ON LINE switch.
- o Wait for the IN USE indicator to go dark.
- o Remove the cartridge and store it safely.

E. BOOTSTRAPPING (PROGRAM LOADING FROM CARTRIDGE TAPE)

You can load a bootstrap program from a Winchester or floppy disk or from a cartridge tape. Use the following procedures to load a bootstrap from cartridge tape:

1) Insert the cartridge and press the ON LINE switch.

2) Press the system RESET switch.

3) Wait for the console terminal to issue the prompt DRV (W0,F0,T)?

4) Type the letter T (uppercase is required).

5) The IN USE indicator on the tape drive should blink, and the tape should move.

F. DIAGNOSTICS AND TESTING

If a tape drive error occurs, one or more of the following problems may exist:

1) The tape drive read/write heads need cleaning.

2) The tape is defective.

3) A program is trying to write on a tape when the write-protect plug is set in the SAFE position.

4) The OPER/TEST switch on the tape drive's front panel is set on TEST rather than OPER.

5) The tape length does not correspond with the setting of the 300/450 or 600 switch.

6) The cable that connects the interface board to the tape drive is not secure.

7) The interface board is not securely seated in the bus backplane.

8) The system software has been generated incorrectly.

DIAGNOSTICS

The FWT cartridge tape systems have extensive self test and diagnostic capabilities. There are three types of diagnostic tools: on line system testing, off line testing, and tape drive self testing.

On Line System Testing

The FW Installation and Test software tests the tape system on line. Use the following procedure to perform on line testing:

1) Boot load the FW Installation and Test software from disc or tape.

2) Insert a write-enabled scratch tape.

3) Enter SELECT COMMAND: T (for test)

4) Enter SELECT SUB-COMMAND: T (for tape)

Off Line Diagnostic Test

The following procedure tests the tape drive off line:

1) Before starting the test, the OPER/TEST switch should be in the OPER position.

2) Turn on the power if the system is not already powered up. The LED indicators on the tape drive's front panel should all be off. Press the ON LINE switch if necessary to take the drive off line. If any indicators are remain lit, the controller is inoperative. See step 5, below.

3) Insert a scratch cartridge into the drive (it will not be written on) and set the 300/450 or 600 switch to correspond to the length of the scratch tape.

4) Start the self test by moving the OPER/TEST switch to the TEST position. Let the test run for a minute or two. The LED indicators should remain off

except when an error is detected. If an error occurs, the LED indicators display one of the following error codes:

TABLE 9. LED MEANING DURING TAPE SELF TEST

ON LINE	IN USE	ERROR	PROBLEM
OFF	OFF	OFF	no error
OFF	OFF	ON	PICO bus disconnected
OFF	ON	OFF	no cartridge or drive fault
OFF	ON	ON	parity error on PICO bus
ON	OFF	OFF	drive not ready after a load
ON	OFF	ON	Kennedy self test fails
ON	ON	OFF	PICO bus timeout
ON	ON	ON	LED test OK

5) The tape controller halts when an error occurs. An LSI-11 bus init (BINITL) command is required to restart the controller.

6) After the test runs for a minute or two without displaying an error code, you may want to make sure that the LED indicators are all working. Press and hold down the ON LINE switch. All three LED indicators should remain lit while you hold down the switch.

7) Stop the test by moving the OPER/TEST switch to the OPER position. Although the test will run as long as you let it, a minute or two is adequate for testing. Running the test for a long time (more than half an hour), causes excessive wear on the section of tape used for the test.

Drive Self Test

The Kennedy 6455 tape system includes self test diagnostics. The system must be reconfigured when these tests are used. For more information about these tests, see the TS0100 OEM manual or the Kennedy Operation and Maintenance manual. SMS will provide these manuals on request.

TABLE 10. TS0100 STRAPPING OPTIONS

W1	INSTALLED *	Enable Q-Bus parity error detection
	REMOVED	Disable Q-Bus parity error detection
W2	INSTALLED	Enable on-board LED's (no front panel)
	REMOVED *	Disable on-board LED's
W3	INSTALLED	8X305 emulator connected (factory testing)
	REMOVED *	8X305 on board (normal mode)

W5	W4	Interrupt vector select (octal)
I	I *	224
I	R	214
R	I	260
R	R	300

W8	W7	W6	Base register TSDB select (octal)
I	I	I *	772520
I	I	R	772524
I	R	I	772530
I	R	R	772534
R	I	I	Reserved
R	I	R	Reserved
R	R	I	Reserved
R	R	R	Reserved

W10	W9	Bootstrap address select (octal)
I	I *	disabled
I	R	775000
R	I	766000
R	R	773000

W11	W12	W13	W14	W15	W16	W17	W18	Interrupt Priority
R	R	R	I	R	I	R	R	4
I	R	I	R	R	I	R	R*	5
R	I	R	R	I	R	I	R	6
R	I	I	R	R	R	I	I	7

W19	R *	For SMS use only (factory testing)
W20	I *	
W21	R *	
W22	I *	
W23	I *	Systems using Q-Bus pins BC1, BD1, BE1, or BF1
W24	I *	for signals other than BDAL18L-21L should cut
W25	I *	these jumpers
W26	I *	
W27	I *	Enable oscillator (factory testing)

*SMS Default strapping (See figure on next page). R = Removed I = Installed

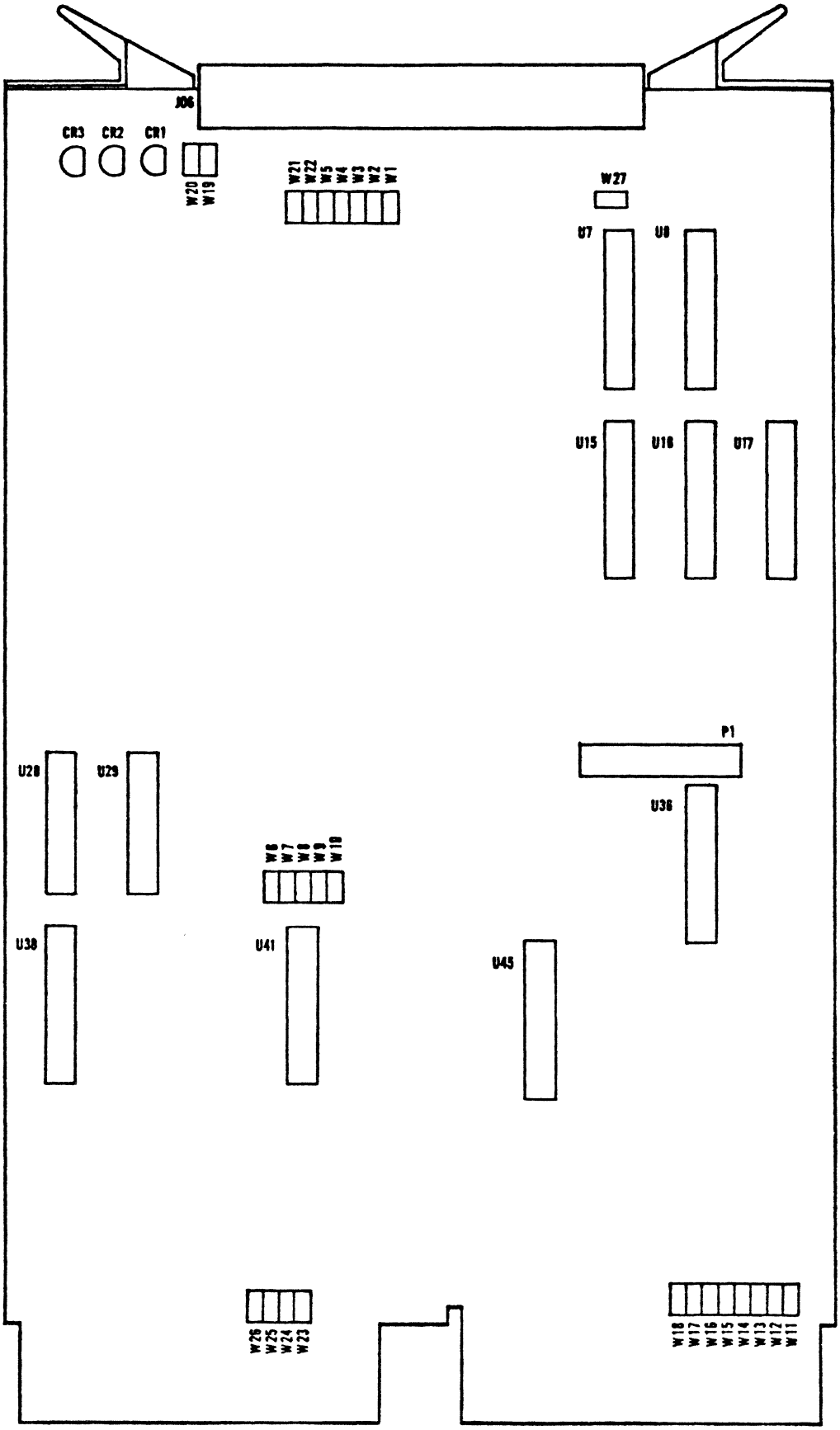


Figure 4. TS0100 Printed Circuit Board Options (Rev. B and up)

H. ADDITIONAL INFORMATION

For information concerning programming the tape system, see the TS0100 OEM Manual, SMS part number 3000879, or DEC's TS-11/TSV05 Manual.

For information concerning the differences between the TS0100 and the DEC TS-11/TSV05, see the TS0100 OEM manual.

For information concerning the maintenance of the tape drive, see the Kennedy Operation and Maintenance Manual for the model 6455 tape drive.

V. DISK CONTROLLER PROGRAMMER'S GUIDE

A. MODES OF OPERATION

In order to be either compatible with DEC software or alternately to offer enhanced performance and capacity, the controller may be operated in one of two modes. These modes are the RX02 compatible mode and the extended mode.

RX02 Compatible Mode

In this mode the controller is completely compatible with the DEC RX02 floppy family, including single and double density format compatibility. When the controller is operated in the compatible mode, the following features are offered over the DEC RX02 system.

- o on board bootstrap and diagnostics
- o write protection on selected diskettes
- o choice of Shugart or compatible disk drives
- o drive activity light and faster seek of SA-850
- o a faster buffer/memory DMA rate
- o immediate drive status versus waiting .25 seconds for status

Extended Mode

The extended mode of the controller is its most powerful and useful mode. This mode offers significant functional and performance advantages over the DEC RX02 floppy disk system plus access to a fixed Winchester disk drive using a common software handler. The same device registers are used to access both the floppy and fixed drives.

Extended mode offers the following advantages over the compatible mode.

- o IBM 2/2D formats (all sector sizes)
- o access to Winchester fixed disks and floppy disks
- o direct transfers from/to host memory to/from the floppy and fixed disks
- o block reads/writes of multiple sectors across cylinder boundaries
- o programmable sector interleave plus cylinder offset for maximum performance on both floppy and fixed disks
- o overlapped seeking
- o error retry is accomplished by the controller, not the host
- o diagnostic commands
- o full 22-bit addressing

In this mode the command set of the controller is expanded to add eight commands and thus allow significant functional and performance increases. For example, in the extended mode direct transfers from memory to the disk (or from the disk to memory) are possible. These transfers are done through a 64 word first-in, first-out (FIFO) buffer and occur at the transfer rate of the disk (up to 1.0 Mbytes/second). The eight commands are added by including the Unit Select bit in the Command and Status register in the function field. The unit number is

passed as a parameter via the data buffer register just as other parameters are passed. The additional functions are listed in section V-G.

The host firmware can cause the controller to enter the extended mode by issuing a Set Media Density command with a parameter of ASCII "SE" (octal pattern of 51505) instead of an ASCII "I". The host can return to the compatible mode by using the command with the parameter "EC" (octal pattern of 42503) or by setting the initialize bit in the Command and Status Register.

At power on the controller can be placed in either the compatible mode or extended mode as determined by the extended/compatible mode strap (see Table 4).

Error Retry Policy

During the execution of a command in the extended mode, if an error is encountered, the controller will retry the command if the error falls into the optionally retriable class and the host has enabled retries by clearing the retry bit in the unit designator word (see section V-F). The retry policy is the same for both the floppy and Winchester drives.

The optionally retriable errors are divided into two classes -- class 1 and class 2.

The class 1 errors are retried only twice and the retry policy is:

1) seek to cylinder 0
2) seek to the desired cylinder
3) re-execute the command.

Class 1 errors:

1) head positioning
2) no address marks found on track
3) sector ID not found
4) media not readable before sector ID found.

The class 2 errors are retried eight times. The retry policy is to simply retry the operation on the sector that caused the error. Class 2 errors are:

1) data CRC check failed
2) missing data address mark
3) data late
4) media not readable after sector ID has been found.

Whenever retries are attempted during the execution of a command, the retry bit is set in the Error and Status Word (see section V-F) regardless of the success or failure of the retry. This alerts the host to potential media or hardware problems.

Error Correction Policy

If Error Correction is enabled then error correction on data field read errors will be attempted. However, error correction is not attempted until the ECC residue is identical for two successive reads. This insures error correction is not attempted on soft errors and thus decreases the probability of miscorrection.

If, when error correction is attempted, the error is not correctable, up to eight retries and correction attempts are made before an error is reported.

B. HOST/CONTROLLER PROTOCOL

Because of the nature of the system design, certain protocols must be followed in order to insure error free exchange of information between the host (LSI-11) and the controller. In this system there are two protocols. One is the standard protocol used by RX02 compatible systems and one is the protocol used when overlapped seeking is being done. In the compatible mode only the RX02 protocol can be used. In the extended mode the RX02 protocol can be used as long as the seek command is not used; otherwise the overlapped seek protocol must be used.

RX02 Protocol

1. Issue and initiate a function by writing the function (plus extended address, density, unit select and interrupt enable if required) into the CSR register with the GO bit set. Setting the GO bit results in the Done and the Error bits being cleared. The CSR can be written only when the Done bit is set (i.e. controller not busy).

   NOTE: Because the CSR contains some write only bits the bit set and bit clear instruction should not be used when accessing this register (e.g. a bit set of the function field followed by a bit set of the GO bit will not work correctly).

2. Wait for either the command to complete (Done set) or the TR bit in CSR to be set.

3. If TR is set, then write the required parameter to DBR and go to step 2. Note that writing a parameter into DBR clears TR.

4. When the command completes (Done Set) read status from DBR.

WARNING: When the RX02 protocol is used in the extended mode, the SR bit (density in compatible mode) in the command and status register must always be written as a 0. The AV bit has no meaning in this case and should be ignored.

Overlapped Seek Protocol (Extended Mode only)

In those systems which use overlapped seeks, a somewhat more complex protocol is required. This is caused by two possible events:

1. The host CPU begins to issue a new command at the same time as a previously issued command is completed. Because the setting of the GO bit clears any pending interrupt and because the passing of parameters through DBR overwrites any status information held there, it is possible for the host to thus lose all indication that the previous action has finished.

2. Two overlapped operations complete either nearly simultaneously or during a period where the host CPU has interrupts disabled and is not polling the CSR. Status information in DBR from the second operation would overwrite similar information from the first operation without detection by the host CPU.

In order to address these potential errors, a protocol involving three CSR bits is used. These bits are:

SR - Status Read — CSR R/W bit 8. (Density bit in compatible mode.) Pulsed high by the host to acknowledge the raising of DN and to indicate that status information has been read from DBR.

DN - Done — CSR R/O bit 5. (Done bit also in compatible mode.) Set high by the controller to generate an interrupt and to indicate to the host CPU that an operation has completed and that status information for that operation may be read from DBR. Cleared by the setting of the GO bit by the host CPU or by the controller to indicate an overlapped command is being processed.

AV - Available — CSR R/O bit 11. (RX02 bit in compatible mode.) Set high by the controller during any time period where the controller is able to accept another command from the host CPU.

The overlapped seek protocol to be followed is as shown below:

Issuing Commands

1. Wait for Available to be set (AV=1). If Done (DN) is set and Available (AV) is not set, status is pending.

2. Disable interrupts.

3. Issue and initiate function by writing the function plus the extended address bit and interrupt enable into the CSR with the GO bit set and the SR bit cleared.

   Because the CSR contains some write only bits the bit set and bit clear instruction should not be used when accessing this register (e.g. a bit set of the function field followed by a bit set of the GO bit will not work correctly).

4. Wait for the TR or the DN bit to be set.

5. IF DN is set before TR THEN

   BEGIN
   a) Read status from DBR
   b) Set SR
   c) Wait for AV to be set
   d) Clear SR
   e) Process status
   f) Go to step 3 (re-issue command)
   END

6. IF TR is set before DN THEN

   BEGIN
   a) Issue next parameter by writing it to DBR
      (NOTE: writing to DBR clears TR)
   b) If all parameters have been issued then go to step 7.
   c) Wait for TR to be set.
   d) Go to 6a.
   END

7. Enable interrupts and exit.

NOTE: Interrupts are enabled and disabled (steps 2 and 7) to insure that if in step 5 DN is seen before TR, the host re-issues the command. The host must re-issue the command whenever DN is set before TR, since status is pending. The controller cannot continue until the pending status is accepted by the host, thus it ignores the command issued in step 3.

Step 5 will be executed infrequently since DN is set before TR only when the controller is attempting to report status at the same time the host is issuing a new seek command.

Interrupt Processing (or poll for Done)

1. When interrupt occurs (Done set) then read status from DBR.

2. Set the SR bit (SR=1).

3. Wait for Available to be set (AV=1).

4. When AV=1 then clear SR (SR=0).

5. Process status and exit.

Note: When handshaking status using the SR bit, controller interrupts should remain enabled if they were enabled when the command was issued (i.e. set SR with MOV #500,@#177170 and clear SR with MOV #100,@#177170).

C. CONTROLLER REGISTERS

The controller is programmed by using two device registers:

1) Command and Status Registers (CSR)
2) Multipurpose Data Register (DBR)

The CSR register is normally assigned a bus address of 177170_8 while the DBR register address is 177172_8. However these addresses are jumper selectable and can be changed.

The interrupt vector address is normally 264_8. This address may also be changed using jumpers.

In the compatible mode, the CSR and DBR registers are identical to the RX02 registers RX2CS and RX2DB.

The multipurpose data register is used to pass additional command information, such as track number, from the host computer to the controller. This register can be thought of as either one physical register which is used to emulate several logical registers inside the controller, or as a data buffer used to pass parameters (track, sector, etc.) to the controller. In this document the latter concept is used.

D. REGISTER DESCRIPTION FOR COMPATIBLE MODE

Command and Status Register (CSR)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ER	IN	EA	EA	RX	R	SS	DS	TR	IE	DN	US	FN	FN	FN	GO

Field Mnemonic (bit)	Description
ER (15)	Error Indicator. This bit is set when an error has been detected during the execution of a command. It is cleared by issuing a new command or by setting the initialize (IN) bit. This is a read only bit.
IN (14)	Initialize. This is a write only bit which can be set under software control to initialize the controller without affecting any other device on the bus. The following functions are performed when this bit is set: 1) Done is cleared when IN is set; done is set when all initialize functions have been completed. 2) All heads are marked as unregistered. Registration will occur on the first access. 3) Self test is executed according to switch setting (see Table 2). 4) Track 1, sector 1 on drive 0 is read into the buffer. 5) The CSR and DBR are updated.

EA (12,13) Extended Address. These write only bits indicate an extended bus address. Bit 13 is the most significant bit.

RX (11) RX02 Identification bit. In compatible mode, this read only bit is always set to indicate the controller is emulating an RX02. The controller does not emulate an RX01.

R (10) Reserved (must be written as a zero).

SS (9) Side Select. This bit is set by the host in order to read or write on the second side of a double sided diskette (only valid for dual sided floppy disk drives).

DS (8) Data Density. This read/write bit is readable only when Done is set at which time it indicates the density of the data of the previous command. When it is written it specifies the data density of the command to be executed. When the bit is set RX02 double density is selected. When it is clear single density is selected.

TR (7) Transfer Request. This read only bit indicates the host may write the data buffer register (DBR) when it is set.

IE (6) Interrupt Enable. This bit enables interrupts. This read/write bit is cleared when an initialize is done (bit 14=1) or by software.

NOTE: When Done is set and this bit changes from a 0 to a 1, the controller generates a host interrupt. If interrupts are enabled and the Go bit is set at the same time, an interrupt will be generated only when the command completes.

DN (5) Done. When Done is set (DN=1), this read only bit indicates the completion of a function. If Interrupt Enable is set, Done will generate an interrupt when asserted.

US (4) Unit Select. This field selects the desired disk. This read/write bit is readable when DN=1.

FN (1-3) Function Field. These bits determine the function to be executed. The Codes/Functions for these write only fields are listed below:

Code	Function
000	Fill Buffer
001	Empty Buffer
010	Write Sector
011	Read Sector
100	Set Media Density
101	Maintenance Read Status
110	Write Deleted Data Sector
111	Read Error Code

GO (0) Go. When GO=1, this write only bit will start the command.

Multipurpose Data Register (DBR)

Parameter: Track Address

Format:

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
<-- N O T   U S E D -->  0  <--- T R A C K --->
```

Description: This parameter specifies which tracks (0-76) will be addressed by a given function. Bits 8-15 are unused.

Parameter: Sector Address

Format:

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
<-- N O T   U S E D -->  0  0  0  <--SECTOR-->
```

Description: This parameter specifies which sector (1-26) will be addressed by a given function. Bits 8-15 are not used.

Parameter: Word Count

Format:

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
<-- N O T   U S E D -->  <-W O R D  C O U N T->
```

Description: This parameter specifies the number of words (0-128 for double density max, 0-64 for single density max) to transfer. If the word count exceeds the maximum number allowed, Word Count Overflow is set in the Error and Status Register.

Parameter: Bus Address

Format:

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
<---------- B U S   A D D R E S S ---------->
```

Description: This parameter specifies the bus address of the first data word to be transferred.

Parameter: Mode/Set Media Density Word

Format:

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
<---------- MODE/SET DENSITY WORD ---------->
```

Description: This parameter is used to set the controller mode or to specify the RX02 set media density command. There are two allowable values. They are:

OCTAL VALUE	ASCII CODE	MEANING
000111_8	I	RX02 Set Media Density
51505$_8$	*SE	Set extended mode

*Note: This becomes a .WORD "ES in Macro-11.

Parameter: Error and Status Word in Compatible Mode

Format:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<NOT	USED>			NM	WO	R	US	DR	DD	DK	DE	PF	ID	DS	CE

Field Mnemonic (Bit)	Description
NM (11)	Nonexistent Memory or Parity Error. When set, this bit indicates an invalid memory address for a DMA transfer.
WO (10)	Word Count Overflow. This bit indicates that a fill or empty buffer function would exceed the sector size.
R (9)	Reserved (when read these bits will be 0)
US (8)	Unit Select. This bit indicates the current drive selected.
DR (7)	Drive Ready. If DR=1 the drive is ready. This bit is valid only after a Read Status function or an initialize.
DD (6)	When DD=1, indicates Deleted Data AM read on last operation.
DK (5)	Drive Density. This field specifies the diskette data density in the last selected drive on the last access to that drive.
DE (4)	Density Error. This field indicates that the function and diskette densities differ. When this error is detected the command is terminated by setting Error and Done.
PF (3)	Indicates power failure when PF=1.
ID (2)	Initialize Done. When ID=1 the initialization sequence is complete. Initialization sequence is entered on: 1) power on; 2) bus initialize; 3) IN=1 in the command and status register.
DS (1)	When DS=1 a double sided diskette is installed.
CE (0)	CRC Error. If CE=1 the data transferred is invalid because a CRC has been detected. When this error is detected the command is terminated by setting Error and Done.

E. COMPATIBLE MODE FUNCTIONS

In the compatible mode a total of eight functions (or commands) are available. These functions operate on the floppy disk only and are identical to the DEC RX02 functions. These functions are summarized below and described in detail in the following sections. In these sections the parameters are listed in the order in which they are written to the data register (DBR). All parameters must be sent to the controller using the protocol described in section V-B. Commands are always initiated by writing the function to the Command and Status register with the GO bit set. This is allowed only when the Done bit is set. If a command is written to the Command and Status register when the Done bit is not set, the command is ignored. Whenever a command is initiated properly, the Done bit is cleared.

If an error is detected the command is terminated by setting Done and Error in the Command and Status Register.

The cause for the error is reported with the Error and Status word which is written to register DBR.

CODE	FUNCTION
000	Fill Buffer
001	Empty Buffer
010	Write Sector from buffer
011	Read sector to buffer
100	Set Media Density/Set Mode
101	Read Status
110	Write Deleted Data Sector from buffer
111	Read Error Code

Command: Fill Buffer (000)

Parameters: Word 1 - Word Count
Word 2 - Buffer Address (host memory)

Function: Transfer from 1 to 128 words of data from host memory to the controller data buffer.

Operation: If the word count is zero the command is terminated (Done is set). Error is not set when the word count is zero. If the word count is greater than 128 words with the double density bit set (or 64 words with the double density bit clear) the command is terminated by setting Done and Error.

If the word count is less than or equal to 128 (64 for single density), the requested number of words are transferred from memory to the controller's buffer. If the transfer is less than 128 words the controller fills the remaining words with zero's.

Upon completion of the command, Done is set, and the Error and Status word can be read from the data register (DBR).

Command: Empty Buffer (001)

Parameters: Word 1 - Word Count
Word 2 - Buffer Address (host memory)

Function: Transfer from 1 to 128 words of data from the controller buffer to host memory.

Operation: If the word count is zero the command is terminated (Done is set). Error is not set when the word count is zero. If the word count is greater than 128 words with the double density bit set (or 64 words with the double density bit clear) the command is terminated by setting Done and Error.

If the word count is less than or equal to 128 (64 for single density), the requested number of words are transferred from the controller buffer to host memory.

Upon completion of the command, Done is set, and the Error and Status word can be read from the data register (DBR).

Command: Write Sector from Buffer (010)

Parameters: Word 1 - Sector Number
Word 2 - Track Number

Function: Write one sector from the controller's buffer to a floppy drive.

Operation: After the command and parameters have been received the track number is checked to insure it is within 0 to 76. If not the command is terminated and an error reported. The sector number is not limit checked, but only the least significant byte is used.

If the parameters are valid the controller seeks to the requested track, validates the track number and locates the requested sector. The diskette density and the requested density are then compared. If they are the same the entire sector is then written; otherwise the command is terminated and an error reported.

Upon completion of the command, Done is set and the Error and Status word is available in the data register DBR.

Command: Read Sector to Buffer (011)

Parameters: Word 1 - Sector Number
Word 2 - Track Number

Function: Read one sector from a floppy drive to the controller's buffer.

Operation: After the command and parameters have been received the track number is checked to insure it is within 0 to 76. If not the command is terminated and an error reported. The sector number is not limit checked, but only the least significant byte is used.

If the parameters are valid the controller seeks to the requested track, validates the track number and locates the requested sector. The diskette density and the requested density are then compared. If they are the same the entire sector is then read; otherwise the command is terminated and an error reported.

Upon completion of the command, Done is set and the Error and Status word is available in the data register DBR. If a deleted data address mark was read the deleted data bit in the Error and Status word is set.

Command: Set Mode/Media Density (100)

Parameters: Mode/Set Media Density Word

Function: Set the controller mode or set the media density

Operation: The Mode/Set Density word is compared to one of two values. If the parameter is an ASCII 'I' and the format selected (via a switch) is RX02 double density, then starting at sector 1, track 0, the diskette's data fields are initialized to the density selected by the density bit in the command and status register. The diskette header (ID) information is not modified.

The Set Media Density operation must not be interrupted. If it is, the operation must be repeated.

Initializing (formatting) diskettes can be accomplished by using the format command in the extended mode.

If the parameter is an ASCII 'SE' (a .WORD "ES in Macro-11) then the controller enters the extended mode. See section V-F,G for a description of the extended mode.

Upon completion of the command, Done is set and the Error and Status word is available in register DBR.

Command: Maintenance Read Status (101)

Parameters: None

Function: Read the Error and Status word

Operation: The drive ready status is updated by checking the drive ready signal from the floppy, thus this command takes about the same time as a read sector command does (less than 60 msec) when no stepping is done.

If the drive is ready the density status is updated by loading the head of selected drive and reading the first data address mark.

If the drive is not ready, the density status of the last successful read is reported.

After the above has been accomplished the Error and Status word is available in DBR.

Errors are reported if the density bit in CSR does not agree with the density of the diskette or if a data address mark cannot be found. No error is reported if the drive is not ready.

Command: Write Deleted Data Sector from Buffer (110)

Parameters: Word 1 - Sector Number
Word 2 - Track Number

Function: Write one sector using deleted data (control) address marks from the controller buffer to a floppy drive.

Operation: The operation is the same as Write Sector function except that a deleted data address mark is written in place of the standard address mark.

Command: Read Error Code (111)

Parameters: Word 1 - Buffer Address

Function: Read extended status into memory

Operation: Upon receipt of the command and parameter, the controller DMA's four words of status to the buffer address (specified by the parameter and bits 12,13 in CSR). The format of these status words is:

Word 1<7:0>	Definitive Error Code***
Word 1<15:8>	Word Count Register
Word 2<7:0>	Current Track Address of Drive 0
Word 2<15:8>	Current Track Address of Drive 1
Word 3<7:0>	Target Track of Current Disk Access
Word 3<15:8>	Target Sector of Current Disk Access
Word 4<7>	Unit Select Bit*
Word 4<5>	Head Load Bit*
Word 4<6><4>	Drive Density Bit of Both Drives*
Word 4<0>	Density of Read Error Code Command*
Word 4<15:8>	Track Address of Selected Drive**

* Five status bits are included in an 8-bit word. Unit Select = bit 7, Density of Drive 1 = bit 6, Head Load = bit 5, Density of Drive 0 = bit 4, Density of Read Error Code Command = bit 0.

**The Track Address of the Selected Drive/error is only meaningful on a code 150 error. The register contains the address of the cylinder that the head reached on a seek.

***The definitive error code is updated only when an error occurs. Thus, when a command is issued, the definitive error code will remain unchanged if no error occurs. Read Error Code cannot be used to determine if an error occurred on the last command.

The definitive error codes are (codes in octal):

Code	Error Code Meaning
0040	Tried to access a track greater than 76.
0070	Desired sector could not be found after looking at 52 headers (two revolutions).
0120	A preamble could not be found.
0130	No ID mark found within allotted time span.
0150	The header track address of a good header does not compare with the desired track.
0170	Data AM not found in allotted time.
0200	CRC error on reading the sector from the disk. No code appears in the ERREG.
0220	R/W electronics failed maintenance mode test.
0230	Word count overflow.
0240	Density Error.
0250	Wrong key word for set media density command.

F. REGISTER DESCRIPTION IN THE EXTENDED MODE

Command and Status Register (CSR)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ER	IN	EA	EA	AV	R	XA	SR	TR	IE	DN	FN	FN	FN	FN	GO

Field Mnemonic (bit)	Description
ER (15)	Error Indicator. This bit is set when an error has been detected during the execution of a command. It is cleared by issuing a new command or by setting the initialize (IN) bit. This is a read only bit.
IN (14)	Initialize. This is a write only bit which can be set under software control to initialize the controller without affecting any other device on the bus. The following functions are performed when this bit is set: 1) Done is cleared in the CSR. 2) All heads are marked as unregistered. Registration will occur on the first access. 3) Controller power diagnostics are executed. 4) If available, any flaw maps are read from the Winchester. 5) The command and status register (CSR) is set to 40408, and the data bus register (DBR) is set to zero.
EA (12-13)	Extended 18-Bit Address. These bits are the most significant bits of the bus address (bit 13 is the MSB) and are write only bits. Note: These bits are not used if XA bit=1.
AV (11)	Available. Set high during any time period in which the controller is able to accept another command from the host CPU. This is a read only bit. If the RX02 protocol is used, this bit will remain low when the controller is placed in extended mode until a power on or initialize is issued. Thus this bit can be used to indicate if the controller is in extended or compatible mode.
R (10)	Reserved. Must be set to 0 when writing CSR.
XA (9)	If this bit=0 when the CSR is written then 18-bit addressing is done with bits 12,13 (EA) being used. If this bit=1 when the CSR is written then 22-bit addressing is done. CSR bits 12 and 13 (EA) are not used. The extra address bits are transferred by passing an additional buffer address word.

SR (8) Status Read. This bit must be used when overlapped seeking is being done and provides a means for the host to notify the controller it has read the Error and Status word from DBR. See the Seek command description and section V-B for details on using this bit. This is a read/write bit. This bit is always set to 0 when issuing a new command regardless of protocol being used.

TR (7) This read only bit indicates the host may write the data buffer register (DBR) when it is set.

IE (6) Interrupt Enable. This bit enables interrupts. This is a read/write bit. It is cleared when an initialize is done (bit 14=1) or by software.

NOTE: Whenever Done is set and this bit is changed from a 0 to a 1, the controller will generate a host interrupt. If interrupts are enabled and the Go bit is set at the same time, an interrupt will be generated only when the command completes.

DN (5) RX02 Protocol

Done. This read only bit indicates the completion of a function and that status can be read from the DBR. When this bit is set another command may be issued. When this bit is clear a command is in the process of being executed. Any commands issued when Done is clear are ignored.

Overlapped Seek Protocol

Done. This read only bit indicates the completion of a function and that status can be read from the DBR. Unlike the RX02 protocol however, the controller will accept another command, as long as the Available bit (AV) is set, when Done is clear (DN=0). When this bit is clear a command is in the process of being executed.

When Done is set, status should be handshaked as described in section V-B, interrupt processing.

FN (1-4) Function Field. These bits determine the function to be executed. See section V-G for a description of the codes and functions. The function field is a write only field.

Note: Bit 4 of the CSR is not a write only bit and thus, unlike bits 1-3, it may be a 0 or 1 when read.

GO (0) Go. This bit, when set to a 1, will start the command. GO is a write only bit.

Multipurpose Data Register (DBR)

This register is used to pass parameters from the host CPU to the controller and for the host to receive status from the controller. The formats and meaning of the parameters passed to the controller and the status received by the host are detailed below. The host must observe the protocol described in section V-B when writing the DBR register.

Parameter Name: Unit Designator

Format:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PA	EC	R	R	DS	DS	SL	SL	IL	IL	DL	NR	NC	R	DT	UN

Field Mnemonic (bit)	Description
PA (15)	Determines whether the disk address is interpreted as a physical (PA=1) or logical (PA=0) address. See section III-B for a discussion of physical versus logical addressing. Note: When using physical addressing, if a flawed sector is accessed, an error will be reported.
EC (14)	This bit, when set, enables floppy error correction. See section III-G for a detailed discussion of floppy error correction. Under normal conditions this bit would not be set (i.e. no floppy error correction would be done.)
R (2,12-13)	Reserved (must be written as a 0)
DS (10-11)	This field specifies the floppy disk encoding as shown below. This field is not used when the device is a fixed disk (DT=1). 00 single density (IBM 3740, DEC RX01) 01 RX02 double density (always 256 bytes/sector) 10 IBM double density 11 IBM double density (same as 10)
SL (8-9)	This field specifies the floppy sector length as shown below. This field is not used when the device is a fixed disk (DT=1) or when the diskette density selected is RX02 double density. 00 128 bytes/sector (IBM 3740, DEC RX01) 01 256 bytes/sector (IBM 2D) 10 512 bytes/sector 11 1024 bytes/sector (IBM 2D)
IL (6-7)	This field applies to floppies only and specifies whether any logical offsetting and/or interleaving is to be done by the controller. 00 no logical offset or interleave 01 1/4 track logical offset compatible with the SMS HIP.

The algorithm used to determine the actual sector read or written on the floppy is as follows:

NOTES: 1) all division is integer division (remainder discarded);
2) logical addresses are converted to a physical address before adding the logical offset.

For track 0

No offset

For tracks 1-76

$$ASN = (\text{Remainder of } (\underline{T-1})) * (\underline{NS}) + PSN$$
$$\qquad\qquad\qquad\qquad\quad 4 \qquad 4$$

IF ASN > NS THEN ASN = ASN-NS

where ASN = Actual Sector Number read or written
T = Track Number
NS = Number of Sectors per track
PSN = Physical Sector Number issued by host (this may have been converted from a logical address).

Note: When double sided drives are being used the offset is the same for both sides, however, head switching occurs only at the index hole (i.e. after the last physical sector).

Thus for a double sided diskette, 512 bytes/sector, 16 sectors/track, the sector sequence for a large block transfer starting at cylinder 3 would be:

CYL 3 Side 0, sectors 9-16
CYL 3 Side 1, sectors 1-16
CYL 3 Side 0, sectors 1-8
CYL 4 Side 0, sectors 13-16
CYL 4 Side 1, sectors 1-16
etc.

The above sequencing eliminates the need for any head switch offset for floppies.

10 six sector offset and 2:1 interleave compatible with the DEC RX02 offset and interleave done by the DEC RT-11 Handler (e.g. the controller replaces the need to do this in the handler and thus allows one command to transfer multiple blocks).

This offset/interleave is valid only for formats which result in having 26 sectors/track (e.g. RX02 single or double density, IBM single density 128 bytes/sector, IBM double density 256 bytes/sector).

Given a logical track, sector, the algorithm used to determine the physical sector actually written is as follows:

```
T = track number-1
S = logical sector number-1
IF    double sided
THEN  T = (T*2) + head number
IF    S < 13
THEN  S = (T*6) + (S*2)
ELSE  S = (T*6) + (S*2) + 1
WHILE S ≥ DO  S = S-26

S = S+27 = physical sector to be accessed
```

This results in the following sequence:

Track	Logical Sector Number Passed to Controller
	1 2 3...11 12 13 14 15 16...26
1	1 3 5...21 23 25 2 4 6...26
2	7 9 11....1 3 5 8 10 12....6
3	13 15 17....7 9 11 14 16 18...12
.	.
.	.
.	.

Note that all of the odd numbered sectors are accessed first, followed by all even numbered sectors, and that two sectors, instead of one, are skipped on the odd to even transitions.

11 Same as 10.

DL (5) Deleted Data (control data) Flag. On a read if DL=1 then any sector which has a deleted data address mark is skipped. If DL=0 and a deleted data address mark is encountered, the sector is read and the operation is terminated. Deleted Data Addresses are used on the floppy disk only.

NR (4) Retry Flag. If NR=0, retries are always attempted according to the retry policy (see section V-A) when an error is encountered. If NR=1, no retries are done when an error is encountered, except for the data late (DMA latency) error.

NC (3) This bit, when set, disables Winchester error correction. Under normal conditions this bit would be 0 which would enable Winchester error correction. See section III-G for a detailed discussion of Winchester error correction.

DT (1) Device Type. If DT=0 the device type is a floppy. If DT=1 the device type is a fixed Winchester drive.

UN (0) Unit Number. This field selects the desired unit (0-1).

Parameter Name: Disk Address

Format: Physical Disk Address

```
          15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
WORD 1    <NOT  USED> <-  HEAD ->  <---  S E C T O R --->
WORD 2    <--- NOT  USED --->  <------ C Y L I N D E R ------>
```

Format: Logical Disk Address

```
          15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
WORD 1    <---------- N O T   U S E D ---------->  <-- LR -->
WORD 2    <---------- LOGICAL RECORD NUMBER (LR)---------->
```

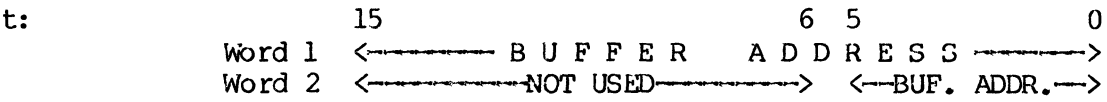
Description: The disk address can be specified as either a physical or logical address as determined by bit PA in the unit designator word. The disk address always consists of two words as shown above. The logical record number is a 20 bit field with the most significant bit in word 1, bit 3 and the least significant bit in word 2, bit 0. The logical record number starts at 1, not 0.

When physical addressing is used head addresses always start at 0 and go to the maximum number of heads minus one.

Cylinder addressing also starts at 0 and goes to the maximum number of cylinders minus one, while sector addressing starts at 1 and goes to the maximum number of sectors per track.

Parameter: Buffer Address

Format:

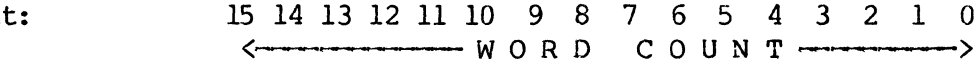


Description: If the XA bit in the CSR is written as a 0 then only word 1 of the buffer address is requested by the controller. It specifies the 16 least significant bits of the buffer address while the EA bits in the CSR specify the two most significant bits of the buffer address. If the XA bit in the CSR is written as a 1 then both words of the buffer address are requested by the controller. The EA bits in the CSR are not used. The first word contains the 16 least significant bits while the second word contains the six most significant bits of the buffer address.

Note: Bit 0 of word 0 (LSB) must always be=0, that is transfers always start at a word boundary.

Parameter: Word Count

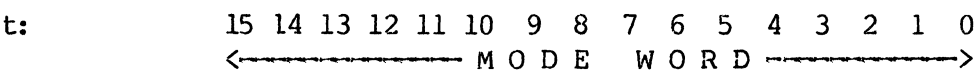
Format:



Description: This parameter specifies the number of words to transfer. From 0 to 65535 words can be transferred. The actual word count is loaded with 0 to 65535 words (not two's complement).

Parameter: Mode Word

Format:



Description: This parameter is used to set the controller to the compatible mode. The only allowable value is:

OCTAL CODE	ASCII VALUE	MEANING
42503	*EC	Enter compatible mode

*Note: This becomes a .WORD "CE in Macro-11.

Parameter: Disk Format Designator for Winchester Drives

Format:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	WR	SL	SL	SI	SI	SI	SI	0	0	0	UN

Field Mnemonic (bit)	Description
WR (10)	This bit is used only when the device type is a Winchester and specifies whether the gap at the end of each sector should include or not include the drive write to read recovery time. For the Shugart SA1000 or Quantum Q2000 drives, setting this bit will increase the speed tolerance as shown in Table 7.
SL (8-9)	This field specifies the sector length as follows: 00 not used 01 256 bytes/sector 10 512 bytes/sector 11 not used
UN (0)	This field selects unit 0 or unit 1.
SI (4-7)	Sector Interleave Increment. This value specifies the increment between sectors read or written. The number of sectors skipped is the interleave increment - 1. Thus, an increment of 1 results in consecutive sectors being read or written. An increment of 2 results in one sector being skipped and so on.

Parameter: Disk Format Designator for Floppy Drives

Format:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	DS	DS	SL	SL	SI	SI	SI	SI	0	0	0	UN

Field Mnemonic (bit)	Description
DS (10-11), SL (8-9), UN (0)	Same as unit designator parameter.
SI (4-7)	Sector Interleave Increment. Same as for Winchester drives.

Parameter: Starting Cylinder

Format:

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
 0 <----------> 0  <----- C Y L I N D E R ----->
```

Description: This parameter specifies the cylinder at which the formatting will start.

Parameter: Number of Cylinders to Format

Format:

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
 0 <----------> 0  <--- NUMBER OF CYLINDERS--->
```

Description: This parameter specifies the number of cylinders to format. If this parameter is zero all cylinders will be formatted.

Parameter: Head Step and Switch Offsets

Format:

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
<--- Switch Offset ---->  <--- Step  Offset --->
```

Description: Head Switch Offset: This field specifies the number of sectors to offset when switching from one track to another track within a cylinder (i.e. Head select time).

Head Step Offset: This field specifies the number of sectors to offset when moving the head to the next cylinder.

An offset of 0 or 1 results in no offset (e.g. a head switch will go from the last sector of the current track to the first sector of the next track).

An offset of 2 will cause one sector to be skipped, an offset of 3 will cause two sectors to be skipped, and so on.

Offsets are not applied to fixed heads or to floppy cylinder 0.

Parameter: Subtest/Unit Number

Format:

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
<------ Subtest ------>  0  0  0  0  0  0  0 UN
```

Description: UN (0) is the same as unit designator. The Subtest field is used to specify the activity of the maintenance command.

Upon completion of all commands the multipurpose data register (DBR) contains status and error information. This status information can be read only when the Done bit in the Command and Status register is set.

The meaning and format of the status and error information for the extended mode of operation is as follows.

Parameter: Error and Status Word (in extended mode)

Format:

```
15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
SC TO EC<---------->EC TS WP RF DR DD ND DT UN
```

Field Mnemonic	Description
SC (15)	When this bit is set a seek caused by the seek command has completed on the unit indicated by the UN field.
TO (14)	Head positioned at track 0
EC (8-13)	Error Codes. This field shows what caused the error as follows (number in parentheses is in octal):

0 No error

1 (1) Illegal head address error.
The host passed the controller a head address outside the range of the drive being accessed. Head numbers start at 1.

2 (2) Illegal sector address error.
The host passed the controller a sector number outside the range of allowable values. Sector addressing starts at sector 1 with the largest sector number depending on drive type and format.

3 (3) Illegal cylinder address error.
The host passed the controller a cylinder number outside the range of allowable values of the drive being accessed. Cylinder numbers start at 0.

4 (4) Illegal logical address error.
Logical addresses range from 1 to the number of unflawed sectors on the disk. This error occurs when the host passes the controller an address outside of this range.

5 (5) Registration timeout error.
This error will occur when a Winchester does not report seek complete or the track 0 indication is not seen by the controller.

6 (6) Reserved for internal controller uses.
(Illegal word count in compatible mode).

7 (7) Illegal drive type error.
If an attempt is made to access a Winchester and the formatter board drive type switches are set to a NOT USED position, this error will occur.

8 (10) Format error (sector length wrong).
This error will occur when sector length of the diskette does not agree with that passed to the controller by the host.

9 (11) Head select error.
If after one revolution the controller cannot find the desired sector, it will read an ID to determine if the head is correct. If it is not this error will be reported.

10 (12) Write protected error.
Host attempted to write or format a write protected diskette.

11 (13) Deleted data error.
Deleted data (control) AM read and the DL in the unit designator word was 0. If the DL bit is 1 the sector is skipped if it has a deleted data AM and no error is reported. This error applies to floppies only.

12 (14) Key word error.
Wrong key word passed by host on the Set Mode command.

13 (15) DMA error.
The controller detected a non-existent memory or parity error when attempting to access host memory.

14 (16) Disk overrun error.
The host attempted to read beyond the end of the disk.

15 (17) Head positioning or seek error.
After positioning the carriage over the desired cylinder if an error occurs, the controller reads an ID to determine if the cylinder is correct. If it is not, this error is reported.

NOTE: If retries are not enabled, then, following a seek error, the host should issue an initialization to re-register the heads.

16 (20) No address marks on track error (floppy only).
The controller could not find any valid address marks on the track. An unformatted diskette will typically cause this error.

17 (21) Sector ID not found error.
The controller could not find the sector the host has requested. This would indicate media or drive problem.

18 (22) Data CRC or non-correctable ECC error.
After reading a sector, the CRC computed did not agree with that previously written. CRC errors often indicate media problems.

19 (23) Missing data address mark error.
The controller has found the desired sector but the data address mark is invalid or missing. This error will occur on any disk reads to a Winchester after a Write ID command since the write ID command will not write a valid data AM. This error may indicate drive or media problems.

20 (24) Data late or DMA latency error.
Host memory transfers were not occurring quickly enough to keep up with the required transfer rate of the disk. Another DMA device would typically have to be "hogging" the bus for this error to occur.

21 (25) Data transfer timeout error.
The controller will timeout any host memory access request after 20 msec.

22 (26) Diskette densities don't match error.
The density of the diskette being accessed does not agree with the value given to the controller by the host.

23 (27) Media not readable error (floppy only).
The controller is unable to maintain phase lock with the diskette data. This error implies media or drive problems.

24 (30) Drive not ready error.
The drive being accessed is not ready. If a diskette is not inserted or inserted backwards, the drive will not be ready.

25 (31) Drive in use error.
If a drive is busy seeking (as a result of a seek command) and another command is issued to that drive this error will be reported.

26 (32) Illegal format for RX02 error.
There must be 26 sectors/track when the IL bits of the unit designator are set to RX02 offset and interleave.

27 (33) Flaw map not valid error.
If flaw mapping is selected and a valid flaw map has not been placed on the drive, this error will be reported on any read/write access.

If an error is detected, such as CRC, when the controller attempts to read the flaw map, the CRC error will be reported. Access errors will always override CRC or ECC errors.

28 (34) Illegal command error.
The host has passed the controller an illegal command.

29 (35) Interface board does not support 22-bit addressing.
This error will be generated if an attempt is made to use 22-bit addressing with a formatter board that supports 22-bit addressing but an interface board that does not.

30 (36) Winchester ID CRC error.
A CRC error was detected when reading the ID field.

31 (37) Winchester write fault error.
Write Fault from the Winchester drive cannot be cleared. This usually indicates a drive or cabling problem.

32 (40) Spare.

33 (41) Flawed sector access error.
Attempt to access a flawed sector. This error will be reported when a flawed sector is accessed using physical addressing. Flawed sectors are skipped if logical addressing is used.

34 (42) Missing Winchester data synchronization mark or DMA access fails.
This error would typically indicate a drive is faulty. However, this error could occur if a DMA access was initiated by the controller and the DMA access was not allowed to complete.

35-47 (43-57) Spare

NOTE: Errors 48-63 are controller hardware and/or firmware failures. The error message will have little meaning to the general user but may be useful when controller repair is attempted.

48 (60) BP fails to respond to reset

49 (61) BP done timeout in WFBPD

50 (62) DMA channel fails to go ready

51 (63) BP start timeout in WFNST

52 (64) BP start timeout - floppy read ID

53 (65) Unknown BP state when decoding error - PBPER

54 (66) BP start timeout - write sect buffered

55 (67) BP start timeout in REBPSD or WFNSTM

56 (70) BP start timeout in FRWD

57 (71) BP start timeout in FORMAT

58 (72) BP error in write sector pulse

59 (73) BP timeout in FWDRW

60-63 (74-77) Spare

TS (7) Two sided diskette flag. This bit is valid only when the drive type is a floppy (DT=0). It is set when a double sided diskette is loaded into the drive.

WP (6) Write protect flag. When set the unit indicated by UN is write protected.

RF (5) Retry flag. Retries or error correction occurred on the last operation if this bit is set. If the error bit in the Command and Status register is not set, then the retries or error correction were successful.

DR (4) Drive ready flag. If DR=1 the drive, indicated by UN, is ready.

DD (3) Deleted data AM flag. Deleted data AM read on last operation when DD=1.

ND (2) New diskette flag. When ND=1 a diskette change has been detected (i.e. the drive has gone from ready to not-ready to ready or from not-ready to ready since the last access).

DT, UN Same as in unit designator.

G. EXTENDED MODE FUNCTIONS

In the extended mode a total of sixteen function codes are available. These functions and their codes are summarized in the table below.

The extended mode functions add additional capability and increase performance over the DEC RX02 floppy disk system plus provide complete support for the Winchester disk drives.

Each of these functions is described in detail in the following sections. In these sections the parameters are listed in the order in which they are written to the data register (DBR). All parameters must be sent to the controller using a protocol described in section V-B. Commands are always initiated by writing the function to the Command and Status Register with the GO bit set. Whenever a command is initiated properly, the Done bit is cleared.

If an error is detected during command execution and if it is a retriable error then it is retried according to the retry policy (see section V-A). If retries fail or it was a non-retriable error, the command is terminated by setting Done and Error in the Command and Status Register.

EXTENDED MODE FUNCTIONS

CODE	FUNCTION
0000	Seek
0001	Format Floppy
0010	Write Direct
0011	Read Direct
0100	Set Mode
0101	Read Drive Status
0110	Write Deleted Data Direct (floppy only)
0111	Read Extended Status
1000	Read ID
1001	Write Winchester ID
1010	Write Flaw Map
1011	Read Flaw Map
1100	Maintenance
1101	Identify
1110	Not Used
1111	Not Used

The cause for the error is reported with the Error and Status word which is written to register DBR. In all cases when the error bit in the Command and Status Register is set, the error field of the Error and Status word will be non-zero.

If the command terminates successfully, the ERROR bit is cleared and the Done bit is set. The error field of the Error and Status word will be non-zero only if retries were done, in which case it contains the cause of the last retry.

Unless otherwise noted, the extended mode commands operate identically with either floppy or fixed drives.

Command: Seek (0000)

Parameters: Word 1 - Unit Designator
Word 2,3 - Disk Address

Function: Position disk head over specified cylinders

Operation: Since all disk read/write commands have implied seeks, the Seek command is typically used only when overlapped seeks are done.

When the Seek command is issued all parameters are checked. If no errors were detected and the drive is capable of seeking then Available (AV) is set and All Seek Commands Finished is cleared. An interrupt is not generated at this point. An interrupt is generated only when the seek completes and Done is set. However because AV is set any new command, except Set Mode, may be issued. Both the seeking and the new command will proceed concurrently. If a new command is issued before Done is set, then the overlapped seek protocol must be used.

If a Seek command and any other command are in progress at the same time, the Seek command will always complete last.

Whenever the Seek command is used the host handler software will typically be interrupt driven. If interrupts are not used the host must poll the controller to determine when a seek completes.

If a Seek command is issued to a drive already busy seeking, an error will be reported.

Command: Format Floppy (0001)

Parameters:
Word 1 - Disk Format Designator For Floppy Drives
Word 2 - Starting Cylinder
Word 3 - Number of Cylinders
Word 4 - Offsets

Function: Format (initialize) a diskette in one of several formats. Formatting a diskette includes the writing of header information (sector number, track number, etc.) and initializing the data field. The allowable formats are described in detail in section III.

Using this command, from one to all cylinders on a diskette can be formatted. Typically the entire surface is formatted, however, if desired, cylinders may be formatted individually.

Operation: After the command and parameter has been passed the controller validates all fields and insures the selected values apply to the drive specified.

The controller next seeks to track 0 and then steps the heads to the specified starting cylinder. When index is detected the cylinder is formatted according to the format selected. After the cylinder is formatted a step to the next cylinder is done and it is formatted. This is repeated until the number of cylinders specified have been formatted.

Upon completion of the command, the Done is set and the Error and Status word can be read at DBR.

Note: If no logical offsetting is being done then, for better performance, SMS recommends the use of a 1/4 track physical offset as shown below:

Bytes/ Sector	Density	Head Step Offset	Head Switch Offset
128	Single	7	1
256	Single	5	1
512	Single	3	1
1024	Single	1	1
128	Double	12	1
256	Double	7	1
512	Double	5	1
1024	Double	3	1

Command: Write Direct (0010)

Parameters:
Word 1 - Unit Designator
Word 2,3 - Disk Address
Word 4 - Word Count
Word 5 - Buffer Address
Word 6 - Buffer address (requested only if XA in the CSR is written as a 1)

Function: Write the specified number of words directly from host memory to the disk.

Operation: After the commands and parameters have been passed and validated, the controller seeks to the cylinder specified by the Disk Address parameter. The disk address may be specified either as a physical (PA=1) or logical address (PA=0). The cylinder number is verified and the desired sector is located. Once the starting sector is located, the number of words specified by word count are transferred from host memory to the disk. Any cylinder boundaries are automatically crossed during the transfer. If the transfer completes with a partially filled sector the controller will zero fill this sector. The data is taken from the memory address specified by the parameter buffer address.

If a read or write direct is issued to a drive busy seeking as a result of a Seek command, an error will be reported (i.e. if Seek commands are being used the host must wait for the seek to complete before issuing the write or read).

The command completes when either an error is detected or all requested words have been transferred. Upon completion of the command Done is set, and, if necessary, the error bit is set. When Done is set the Error and Status word is available in DBR.

Command: Read Direct (0011)

Parameters:
Word 1 - Unit Designator
Word 2,3 - Disk Address
Word 4 - Word Count
Word 5 - Buffer Address
Word 6 - Buffer address (requested only if XA in the CSR is written as a 1)

Function: Read the specified number of words directly from the disk to host memory.

Operation: After the commands and parameters have been passed and validated the controller seeks to the cylinder specified by the Disk Address parameters. The disk address may be specified either as a physical (PA=1) or logical address (PA=0). The cylinder number is verified and the desired sector is located. Once the starting sector is located the number of words specified by Word Count are transferred directly from the disk to host memory specified by the Buffer Address. Any cylinder boundaries are automatically crossed during the transfer.

If a read or write direct is issued to a drive busy seeking as a result of a Seek command, an error will be reported (i.e. if Seek commands are being used the host must wait for the seek to complete before issuing the write or read).

The command completes when all requested words have been transferred or an error is detected. Upon completion of the commmand Done is set, and the ERROR bit is set if necessary. The Error and Status word is available in DBR when the command completes.

Command: Set Mode (0100)

Parameters: Mode Word

Function: Establish the controller mode

Operation: The mode word must be the value described in section V-F. If it is not, the command is terminated with the appropriate error and the controller mode remains unchanged.

If the mode word is correct the controller enters the compatible mode and terminates the command.

The controller mode cannot be changed while a seek is in progress, thus both the Done bit and the All Seek Commands Finished bit must be set before this command can be legally issued.

Done is set, and the Error and Status word is available in DBR when the command completes.

NOTE: To set media density use the format command or enter the compatible mode and use the Set Media density command.

Command: Read Status (0101)

Parameters: Unit Designator

Function: Read Error and Status Word

Operation: This is the extended mode equivalent for the compatible mode read status.

After the command has been received all bits in the error and status are updated and the error status word is written to the DBR. Done is then set to indicate the host may read the DBR. This command will never cause the Error bit to be set.

Command: Write Deleted Data Direct To Floppy (0110)

Parameters:
Word 1 - Unit Designator
Word 2,3 - Disk Address
Word 4 - Word Count
Word 5 - Buffer Address
Word 6 - Buffer address (requested only if XA in the CSR is written as a 1)

Function: Write the specified number of words directly from host memory to a floppy disk using a deleted data address mark. Deleted data address marks are not used on the fixed disks.

Operation: After the commands and parameters have been passed and validated, the controller seeks to the cylinder specified by the Disk Address parameter. The disk address may be specified either as a physical (PA=1) or logical address (PA=0). The cylinder number is verified and the desired sector is located. Once the starting sector is located, the number of words specified by word count are transferred from host memory to the disk using a deleted data address mark. Any cylinder boundaries are automatically crossed during the transfer. If the transfer completes with a partially filled sector the controller will zero fill this sector. The data is taken from the memory address specified by the parameter buffer address.

If a read or write direct is issued to a drive busy seeking as a result of a Seek command, an error will be reported (i.e. if Seek commands are being used the host must wait for the seek to complete before issuing the write or read).

The command completes when either an error is detected or all requested words have been transferred. Upon completion of the command Done is set, and, if necessary, the ERROR bit is set. When Done is set the Error and Status word is available in DBR.

Command: Read Extended Status (0111)

Parameters:
Word 1 - Unit Designator
Word 2 - Buffer Address (least significant)
Word 3 - Buffer address (requested only if XA in the CSR is written as a 1)

Function: Report extended status on a drive by drive basis

Operation: After the command and parameters have been passed and validated the controller transfers several words of status information for the drive selected to host memory. When the transfer is complete, Done is set and the Error and Status word is available in DBR.

The format of the status transferred to memory is as follows:

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word 1	0	0	0	0	0	0	C	<-	-	-	-	-	-	-	->	C
Word 2	<-	-	-	-	-	-	-	-	O	P	T	I	O	N	S	->
Word 3	<-	-	-	-	-	-	-	-	O	P	T	I	O	N	S	->
Word 4	0	0	0	0	0	0	0	0	0	0	0	0	N	<-MSB->		N
Word 5	N	<-MIDDLE	-	-	-	-	-	-	-	-	-	-	-	-	LSB->	N
Word 6	0	0	0	0	H	<-	->	H	S	<-	-	-	-	-	->	S
Word 7	0	0	0	0	0	0	C	<-	-	-	-	-	-	-	->	C

Word 1: Current cylinder of selected unit.
Word 2-3: Option straps (see below)
Word 4-5: Number of logical records (sectors); Winchester flaws are deducted.
Word 6-7: Physical disk address of the last R/W direct disk access. If a disk error occurs on a read/write direct this will be the address of the error. This value is valid only for R/W direct commands. H=Head, S=Sector, C=Cylinder. Thus, for example, if a CRC error occurs this command can be issued to determine the disk address of the error.

OPTION STRAPS

Word 2

BITS 2	1	0	FORMATTER TYPE
0	0	0	FWD0101 REV. E AND BELOW
0	0	1	RESERVED
0	1	0	FWD0101 REV. F AND ABOVE
0	1	1	RESERVED
'	'	'	'
1	1	1	RESERVED

BIT 3	DRIVE MAPPING ENABLE
0	NO MAPPING
1	FLOPPY DRIVES REVERSED

BITS 7	6	5	4	FLOPPY TYPE
0	0	0	0	SA850
0	0	0	1	SA800
0	0	1	0	RESERVED
'	'	'	'	'
1	1	1	1	RESERVED

BITS 9	8	SELF TEST
0	0	NONE
0	1	ONCE AT INIT
1	0	RESERVED
1	1	RESERVED

BIT 10	FLAW MAPPING
1	ENABLED
0	DISABLED

BIT 11	INTERRUPT VECTOR
0	2648
1	2708

BIT 12	POWER UP MODE
0	NO CHANGE
1	RX02 EMULATOR

BITS 15	14	13	PRECOMP ENABLE
		1	DISABLED SINGLE SIDED FLOPPY
		0	ENABLED SINGLE SIDED FLOPPY
	1		DISABLED DOUBLE SIDED FLOPPY
	0		ENABLED DOUBLE SIDED FLOPPY
1			DISABLED WINCHESTER
0			ENABLED WINCHESTER

WORD 3

BITS 4	3	2	1	0	WINCHESTER DRIVE 0 TYPE
0	0	0	0	0	RESERVED
'	'	'	'	'	'
0	0	1	1	1	RESERVED
0	1	0	0	0	SA1002
0	1	0	0	1	SA1004
0	1	0	1	0	Q2010
0	1	0	1	1	Q2020
0	1	1	0	0	Q2080
0	1	1	0	1	Q2040
0	1	1	1	0	RESERVED
'	'	'	'	'	'
1	1	1	1	1	RESERVED

BITS 12	11	10	9	8	WINCHESTER DRIVE 1 TYPE

SAME AS WINCHESTER DRIVE 0

BITS	
15-13	RESERVED
7-5	RESERVED

Command: Read ID (1000)

Parameters:
Word 1 - Unit Designator
Word 2 - Buffer Address
Word 3 - Buffer address (requested only if XA in the CSR is written as a 1)

Function: Read the next available ID header information and transfer it to host memory specified by the Buffer Address.

Operation: The command and parameters are verified and the next available ID information is read and transferred to memory.

ID information transferred is as follows:

Word 1: Cylinder
Word 2: Head
Word 3: Sector
Word 4: Bytes/sector
- 0 = 128 bytes/sector
- 1 = 256 bytes/sector
- 2 = 512 bytes/sector
- 3 =1024 bytes/sector
- 4 = not used
- 5 = 256 bytes/sector with recovery (Winch. only)
- 6 = 512 bytes/sector with recovery (Winch. only)
- 7 = not used

Word 5: Density
- 0 = SD
- 1 = RX02 DD
- 2 = IBM DD
- 3 = Winchester (MFM)

On command completion Done is set,
and the Error and Status word is available in DBR.

Command: Write Winchester ID's (1001)

Parameters:
Word 1 - Disk Format Designator for Winchester Drive
Word 2 - Starting Cylinder
Word 3 - Number of Cylinders
Word 4 - Offsets

Function: Write the ID headers on the specified cylinder.

Operation: Beginning at the starting cylinder the controller writes the header portion of the sector to all sectors on all cylinders specified.
The data fields are set to zero.

WARNING: This command must be followed by a write flaw map command if there are flaws on the drive.

For optimal performance, SMS recommends the following:

SA1000 Series

Bytes/ Sector	Sectors/ Track	(1) Interleave	Head Switch Offset	Head Step Offset
256	32	1	2	7
256	31	1	2	8
512 (2)	17	1	2	4
512	16	1	2	4

Q2000 Series

Bytes/ Sector	Sectors/ Track	(1) Interleave	Head Switch Offset	Head Step Offset
256	32	1	2	1
256	31	1	2	1
512 (2)	17	1	2	1
512	16	1	2	1

Notes: 1) See Table 7 for drive rotational speed tolerance requirements.
2) Standard values used by SMS for maximum capacity.

Command: Write Flaw Map (1010)

Parameters:
Word 1 - Unit Designator
Word 2,3 - Disk Address
Word 4 - Buffer Address
Word 5 - Buffer Address (requested only if XA in the CSR is written as a 1)

Function: This command allows the host to write the flaw map to the disk 128 bytes at a time. The flaw map is written starting at cylinder 0, head 0, sector 1 and duplicated at cylinder 0, head 1, sector 1.

Operation: The flaw map is a set of linked sectors of which only the first 128 bytes are used. The host must generate the flaw map as described in section VI and write the flaw map one sector at a time, using physical addressing, to those sectors indicated by the link.

CAUTION: The write flaw map command bypasses the check for flawed sectors. The host must insure the sectors being written are not flawed. The controller assumes the first sector of the flaw map is not flawed.

Command: Read Flaw Map (1011)

Parameters:
Word 1 - Unit Designator
Word 2,3 - Disk Address
Word 4 - Buffer Address
Word 5 - Buffer Address (requested only if XA in the CSR is written as a 1)

Function: This command allows the host to read the flaw map 128 bytes at a time. The flaw map is a set of linked sectors starting at cylinder 0, head 0, sector 1 and is duplicated at cylinder 0, head 1 sector 1.

Operation: When this command is received 128 bytes of the sector specified will be stored at "buffer address". Physical addressing must be used and not logical addressing.

The format of the flaw map is shown in section VI.

CAUTION: The read flaw map command bypasses the check for flaws, thus allowing flawed sectors to be read. It is assumed that the first sector of the flaw map is not flawed.

Command: Maintenance (1100)

Parameters: Word 1 - Subtest Number/Unit
Word 2 - Subtest Dependent Parameter

Function: This command provides a drive test and several floppy maintenance functions. The drive test can be run either by issuing this command or from switches on the formatter PC boards.

Subtests 1 to 4 apply to the floppy only.

Operation: This command is unique in that the command will execute (except for subtest 4) until an error occurs or until the controller is issued an initialize.

When an error is detected the controller will set Done and Error, and generate an interrupt request as with all other commands.

If no error is detected, the command will continue indefinitely and Done will not be set.

NOTE: The second parameter (word 2) must always be written even if the sub-test does not require a parameter.

Subtest 0

Function: This subtest will perform the drive test on all ready disk drives. The test will not write to any drives and thus will not destroy any existing data on the diskettes or Winchester.

While this test is executing, the LED's on the formatter board will flash on and off. If an error is detected, it will be reported to the host in the normal manner. The LED's will be off at test completion.

Parameter: N/A

Subtest 1

Function: This subtest will select the specified floppy drive, seek it to the specified track and load the head. Various maintenance and alignment functions can then be performed.

Parameter: Track number.

Subtest 2

Function: This subtest will select the specified drive, seek it to the specified track and then load and unload the floppy head about five times per second.

Parameter: Track number.

Subtest 3

Function: This subtest will select the specified drive, load the head and seek it to the specified track. It will then step the drive between the specified track and the specified track plus one about ten times per second.

Parameter: Track number.

Subtest 4

Function: This subtest selects the specified drive, loads the head, seeks to the specified track, and writes the entire track, including headers, with all 1's in single density (FM).

This test will set Done and/or Error after the track has been written.

CAUTION: The diskette must be reformatted after this subtest is issued if the diskette is to be used in normal operations again.

Command: Identify (1101)

Parameters: None

Function: This command allows the host to determine if the controller supports 22-bit addressing. If the command executes without error then the controller supports 22-bit addressing.

If the controller does not support 22-bit addressing then either error 28 (illegal command) or error 29 is reported. Error 29 indicates that the interface board does not support 22-bit addressing (or is faulty) and error 28 indicates that the formatter does not support 22-bit addressing.

H. PROGRAMMING EXAMPLES

The following examples present in a straight forward manner how the controller interface is used. These examples are not intended to be used as application programs, but are for instructive purposes only. For more detailed examples refer to the FW Installation and Test source code. (See section V-C.)

Example #1

```
;
;   COMPATIBLE MODE READ FLOPPY SECTOR INTO HOST MEMORY
;
;   FIRST READ THE SECTOR INTO THE CONTROLLER'S BUFFER
;
        MOV     #407,@#177170       ;ISSUE READ SECTOR COMMAND
                                    ;TO UNIT 0, DOUBLE DENSITY
        JSR     PC,TR               ;WAIT FOR TR TO BE SET
        MOV     #2,@#177172         ;READ SECTOR 2 (THIS CLEARS TR)
        JSR     PC,TR               ;WAIT FOR TR
        MOV     #4,@#177172         ;READ TRACK 4
        JSR     PC,DONE             ;WAIT FOR COMMAND COMPLETION
        BNE     ERROR               ;BRANCH IF ERROR
;
;   NOW EMPTY THE BUFFER INTO HOST MEMORY
;
        MOV     #403,@#177170       ;ISSUE EMPTY BUFFER
        JSR     PC,TR               ;WAIT FOR TR
        MOV     #128.,@#177172      ;EMPTY ENTIRE BUFFER
        JSR     PC,TR
        MOV     #1000,@#177172      ;PLACE DATA AT LOCATION 1000
        JSR     PC,DONE             ;WAIT FOR COMMAND COMPLETION
        BEQ     EXIT
;
;   ERROR HAS OCCURRED
;
ERROR:  MOV     @#177172,R0         ;GET STATUS
        JSR     PC,RERR             ;PROCESS ERROR (APPLICATION DEPENDENT)
;
EXIT:   RTS     PC
;
;   WAIT FOR TR
;
TR:     BIT     #200,@#177170       ;TEST TR
        BEQ     TR                  ;LOOP UNTIL TR=1
        RTS     PC
;
;   WAIT FOR DONE
;
DONE:   BIT     #40,@#177170        ;TEST FOR DONE
        BEQ     DONE                ;WAIT UNTIL IT'S SET
```

```
;
;    DONE IS SET -- TEST FOR ERROR
;
         BIT       #100000,@#177170    ;ESTABLISH CONDITION CODES
         RTS       PC
```

NOTE: In normal use it is good practice to timeout waiting for TR.

Example #2

```
;
;    EXTENDED MODE WINCHESTER READ BLOCK, RX02 PROTOCOL
;
         MOV       #7,@#177170         ;ISSUE READ COMMAND
         MOV       #PARAM,R2           ;GET ADDRESS OF PARAMETERS
         MOV       #5,R0               ;GET PARAMETER COUNT
;
;    ISSUE PARAMETERS
;
10$:     JSR       PC,TR               ;WAIT FOR TR
         MOV       (R2)+,@#177172      ;WRITE PARAMETER (THIS CLEARS TR)
         DEC       R0
         BNE       10$                 ;LOOP UNTIL ALL PARAM. ISSUED
;
         JSR       PC,DONE
         BEQ       EXIT
;
;    ERROR OCCURRED
;
         MOV       @#177172,R0         ;GET STATUS
         JSR       PC,REXST            ;PROCESS ERROR (APPLICATION DEPENENT)
;
EXIT:    RTS       PC
;
;    READ SECTOR PARAMETERS
;
PARAM:   .WORD     100002              ;UNIT DESIGNATOR: WINCHESTER UNIT 0,
;                                      ;PHYSICAL ADDRESS, ENABLE RETRIES
         .WORD       2                 ;DISK ADDRESS, HEAD 0, SECTOR 2
         .WORD       4                 ;CYLINDER 4
         .WORD    1000                 ;WORD COUNT
         .WORD    1000                 ;BUFFER ADDRESS
```

Example #3

```
;   EXTENDED MODE, ISSUE COMMAND OVERLAPPED SEEK PROTOCOL
;
;   ASSUME R0 = PARAMETER COUNT, R2 = POINTS TO COMMAND FOLLOWED BY PARAMETERS
;          R3 = 177170 (CSR), R4 = 177172 (DBR)
;
;   WAIT FOR AVAILABLE
;
10$:    BIT     #4000,(R3)
        BEQ     10$
        MTPS    #340            ;DISABLE INTERRUPTS
15$:    MOV     (R2)+,(R3)      ;ISSUE COMMAND, ENABLE DEVICE INTERRUPT
;
;   WAIT FOR TR OR DONE
;
20$:    BIT     #200,(R3)       ;TEST TR
        BNE     40$             ;BRANCH IF TR IS SET
        BIT     #40,(R3)        ;TEST DONE
        BEQ     20$
;
;   DONE IS SET -- GET STATUS USING OVERLAPPED SEEK HANDSHAKE
;
        MOV     (R4),R1         ;READ STATUS FROM DBR
        MOV     #500,(R3)       ;SET SR, KEEP INTERRUPTS ON
30$:    BIT     #4000,(R3)      ;WAIT FOR AVAILABLE
        BEQ     30$
        MOV     #100,(R3)       ;CLEAR SR, KEEP INTERRUPTS ON
        JSR     PC,PSTAT        ;PROCESS STATUS (APPLICATION DEPENDENT)
        ADD     #-2,R2
        BR      15$             ;GO RE-ISSUE COMMAND
;
;   TR IS SET FOR FIRST TIME -- ISSUE PARAMETERS
;
40$:    MOV     (R2)+,(R4)
        JSR     PC,TR           ;WAIT FOR TR
        DEC     R0
        BNE     40$
        MTPS    #0              ;ENABLE INTERRUPTS
        RTS     PC              ;GO WAIT FOR INTERRUPT (DONE)
;
; OVERLAPPED SEEK INTERRUPT HANDLER
;
        0                       ;SAVE REGISTER, ETC.
        0
        0
        MOV     @#177172,R1     ;GET STATUS
        MOV     #177170,R3      ;NOW DO HANDSHAKE
        MOV     #500,(R3)       ;SET SR, LEAVE INTERRUPTS ON
10$:    BIT     #4000,(R3)      ;WAIT FOR AVAILABLE
        BEQ     10$
        MOV     #100,(R3)       ;CLEAR SR, LEAVE INTERRUPTS ON
        JSR     PC,PSTAT        ;PROCESS STATUS
        RTI
```

VI. SYSTEM TESTING AND TROUBLE ISOLATION

A hierarchy of system testing is provided with all SMS FW controllers and systems. This hierarchy of testing is used to insure the system is operating correctly and, if a failure occurs, to isolate the failure to a major sub-component.

The following paragraphs detail the test programs available.

A. BOOT PROGRAM DIAGNOSTICS

Whenever the boot program (contained in PROM on the interface board) is executed, a simple host (e.g. LSI-11) CPU and memory test (up to 32 KW) is executed. Errors are reported on the console terminal (see section II-I for details).

If the CPU and memory test passes, some basic commands are issued to the controller to insure it is operational. If these tests pass, the boot program prints the DRV (F0, W0 or T)? message and allows the boot operation to continue. If the tests fail, the boot program will either halt or hang (see section II-I).

B. CONTROLLER SELF TESTS AND DRIVE TEST

At power on or after an initialization, the controller can be configured, via switches on the formatter board (see Table 3), to run a self test or a drive test. The self test can be run continuously or bypassed.

To run the self test or drive test, set the switches to the desired position (see Table 3) and then initialize the controller. The controller can be initialized by cycling DC power, AC power, or, if the interface board is installed, by entering a 40000_8 into the Command and Status Register (CSR) which is normally at address 777170_8.

> NOTE: Cycling AC power to start the drive test in systems with Winchester drives may not work since the Winchester drive has a fixed spin up time which may exceed the power on reset time. If this occurs, either cycle DC power or allow the Winchester to reach speed and then quickly cycle AC power.

Controller Self Test

The self test is a thorough functional test of the controller. As with all self tests, it cannot detect 100% of all possible errors, but, if the self test passes, there is a very high probability that the controller is operating correctly.

When the self test is run, if any errors are detected, the error will be reported via the light-emitting diodes (LED's) on the formatter board. If any error is detected, the controller will not set Done and will not accept any commands. The meaning of the LED's patterns during self test is shown in Table 11.

Drive Test

The drive test can be run either via the switches on the formatter board (with or without an interface board present), or via a command issued by the host to the controller. The drive test exercises the controller and all ready drives. The test does not write to any drives, thus it will not overwrite any user data on the drives. The drive test will run continuously until an error is detected. When an error is detected the drive number of the suspect drive is displayed in the LED's (see Table 12) if it was run via the switches. If the drive test is run from the host, the error is reported in the normal manner in the CSR and the DBR.

When a drive test error occurs, insure that the diskettes are formatted and readable (if floppy error is indicated) and that all required cables and straps are installed. Also check drive power.

C. INSTALLATION AND TEST PROGRAM

The SMS Installation and Test program is contained on diskette number 1001941 and described in document number 3000500. The program serves two purposes: 1) it provides a variety of utility functions which allow the user to format his disks, install a flaw map on the Winchester, backup a Winchester to a floppy disk (at less than 1 minute per Mbyte), copy diskettes, etc.; 2) it provides system level diagnostic capability which can be run interactively from the system console.

The Installation and Test Program can be bootstrapped from the floppy as a standalone software system. This is its most typical mode of operation. The program can also be loaded and run as an RT-11 file. See document number 3000500 for details.

NOTE: The Installation and Test Program requires a minimum of 28K words of memory and assumes a standard configuration for the operator's console (vector at 60,64 and CSR at 177560).

TABLE 11. LED MEANING DURING SELF TEST

CR1	CR2	CR3	Meaning
OFF	OFF	OFF	Passes all self tests
OFF	OFF	ON	Byte Processor Failure. Indicates that the formatter board is inoperative.
OFF	ON	OFF	8085 to Interface Board Failure. Indicates that the 8085 processor cannot communicate with the interface board. The interface board, formatter board or the cable between them could be bad.
OFF	ON	ON	8085 System Failure. Indicates an 8085 system component, such as an 8255 I/O port, has failed. Since the EPROM checksum and RAM test have passed, the 8085 itself is probably good. When this failure occurs, the formatter board is inoperative.
ON	OFF	OFF	RAM Failure. Indicates the RAM on the formatter board is faulty. The formatter board may be inoperative.
ON	OFF	ON	8085 EPROM Checksum Failure. Indicates either the 8085 or its program storage is faulty. When this failure occurs, the formatter board is inoperative.
ON	ON	OFF	Byte Processor to Interface Board Failure. Indicates that the byte processor cannot communicate with the interface board. The interface board, formatter board or cable between them could be bad.
ON	ON	ON	Formatter Inoperative. Indicates that the formatter board is inoperative. Check to insure DC power is correct and all socketted parts are seated firmly.

TABLE 12. LED MEANING DURING DRIVE TEST

CR1	CR2	CR3	Meaning
ON	ON	ON	Floppy 0 suspect
ON	ON	OFF	Floppy 1 suspect
OFF	ON	ON	Winchester 0 suspect
OFF	ON	OFF	Winchester 1 suspect
ON	OFF	ON	No drives are ready.
OFF	OFF	OFF	Suspect Winchester 0 or 1. No seek complete indication or -5V power. All drive activity will cease.

D. TROUBLE ISOLATION GUIDE

This section of the manual outlines some steps to follow when the system is not operating as expected. A basic understanding of computer systems and console ODT (or the Console Emulator) is assumed.

It is not possible to isolate all failures in the field. However, many problems can be isolated and corrected by following the steps outlined below. These steps point out some of the most common problems. If trouble persists, contact SMS.

Step 1: The first step is to establish communication between the computer and the system terminal.

If console ODT (LSI-11) or console emulator (PDP-11) is working go to step 2.

If the terminal does not respond at all when the break key is pushed (LSI-11), or if the Console Emulator (PDP-11) does not respond, check the following:

1) Insure there are no overlapped I/O addresses (i.e. if another I/O device were responding to the same CSR address as the terminal, neither would work).

2) For console ODT to work, the CPU, memory and serial I/O boards must all be installed in the backplane and working. Insure there are no vacant slots between these boards.

Step 2: Once console communication has been established, the next step is to execute the SMS boot and diagnostic program. See section II-I. If the boot program does <u>not</u> print DRV (F0, W0 OR T)?, then check the following:

1) For the LSI-11, the Line Time Clock (LTC) is off. Note: If the LSI-11 CPU is in power up mode 2, the LTC can be on since mode 2 will disable CPU interrupts.

2) If the boot diagnostics indicate CPU or memory problems, then corect the problems and attempt to boot again. Note: Insure the memory board is strapped to the correct starting address.

3) If the CSR address for the controller (normally 777170_8) could not be accessed, check the strapping on the interface board.

4) If no valid bootstrap block could be found then either a read error occurred or no program was on the disk(ette). Check for a read error by examining CSR address (normally 777170_8). If the most significant bit is set, an error occurred, and the error is in the DBR (normally 777172_8), bits 8-13. Note: Improper drive optioning can cause read errors. Any external drives must be optioned as shown in section II-G.

5) Any other halt or hang location indicates possible controller and/or CPU failures. However, these failures can also be caused by improper

system configuration such as overlapped I/O or memory addresses. If the controller is suspected of being faulty, go to step 4.

Step 3: Booting the SMS Installation and Test Program

At this point the DRV (F0, W0 OR T)? prompt has been printed on the console. A typical operator response will be to type F0 (in upper case). If no valid bootstrap block could be found go to step 2 part 4. If the program appears to load (floppy LED comes on and head steps), but stops before printing the entire menu, then it is likely that interrupts are not being received. Insure all boards are inserted in the correct sequence with no vacant slots and that the interface board strapping is correct.

Note: The Installation and Test program requires a minimum of 28KW of memory and assumes the default I/O addresses and interrupt vectors for the controller and system console.

Step 4: Isolating Controller Failures

If the controller is suspected of being faulty, then:

1) Check the formatter board LED's. All LED's should be off. If they are on and blinking, check the self test configuration. If they are on and not blinking, then the controller may be inoperative.

   Note: The interface board must be properly connected to the formatter board and must be installed in the CPU backplane with power applied to the backplane for the self test to pass (all LED's off).

2) If the LED's are off and power is applied, then examine the CSR register. After power on, it should be 4040_8 or 4440_8 (assuming a diskette is not installed in drive 0). If the CSR register cannot be accessed, insure the CSR address is strapped correctly. If the value in the CSR is not 4040_8 or 4440_8, insure the cables between the formatter and interface board are properly installed.

3) Execute the drive test from the formatter switches by placing switches 1 and 2 in the open position and issuing a CPU reset (cycle DC power). If the drive test fails the formatter or drives are faulty. The drive test does not require the interface board to be connected. If the drive test passes the interface board or interconnecting cable may be faulty.

   NOTE: Cycling AC power on the FWT chassis may cause the drive test to fail since the Winchester may not be up to speed.

VII. WINCHESTER FLAW MANAGEMENT

A. OVERVIEW

Fixed Winchester disks are often shipped with known defects on the disk surface. These defects can vary from a bad bit to an entire bad track and thus can be a considerable management problem.

The defect information is provided to the user (disk purchaser) in the form of a defect map which normally lists the defect by cylinder, head, byte from index, and length of defect. The FW series disk controller provides complete bad sector/track management on the fixed disk by providing logical addressing capabilities and the capability to read/write a flaw map on the disk surface.

When the flaw management capabilities of the FW controller are used, any flaws will be automatically skipped when they are encountered. The host, if logical addressing is used, can thus view the disk as a series of consecutive records from 1 to N where N is the maximum number of records on the disk minus the number of flawed sectors (including the flaw map itself). The number N can be determined with the Read Extended status command.

The following paragraphs describe the details of flaw management done by the FW controller. In many applications the user may wish to use the SMS Installation Test Program to implement flaw management instead of writing additional programs. All flaw management will be disabled if the formatter is strapped to do so.

At power on, (or after an initialize) if flaw management is enabled, the controller will attempt to read the flaw map from the disk into its internal memory. If a valid map is present it will then use the map to skip any flaws when logical addressing is used for disk accesses. If physical addressing is used an error is returned when a flawed sector is encountered.

If a valid flaw map is not present any read/write access will result in an error being reported. To prevent the controller from overwriting the flaw map, the sectors containing the flaw map are placed in the flaw map.

NOTE: Please refer to the FW Installation and Test Manual for additional flaw map information and for details on how to install the flaw map using the Installation and Test program.

B. FLAW MAP INITIALIZATION PROCEDURE

The following steps must be executed to initialize and write the flaw to a blank Winchester.

1) Write the Winchester ID's.
2) Write the flaw map to the disk using the write flaw command. Only one sector per command can be written.
3) Initialize the controller to cause the flaw map to be read by the controller.
4) Scan the disk to insure all writes were successful.

C. FLAW MAP FORMAT

The first sector of the flaw map is called the pointer sector since it contains links to the remainder of the flaw map. The controller assumes the pointer sector is at cylinder 0, head 0, sector 1, or cylinder 0, head 1, sector 1. One or both can contain the pointer sector. See Figure 5.

The pointer sectors contain links (in the form of physical disk addresses) to two files. One is called the processed flaw data file and the other is called the raw flaw data file. The processed flaw data file contains a list of all flaws on the disk in physical disk address format (i.e. cylinder, head, sector). The raw flaw data file contains the flaw data as received from the Winchester manufacturer (e.g. track, byte from index, length of flaw). The controller does not read or make use of the raw flaw data file. It is used by the Installation and Test Program. By placing the raw flaw data on the disk it does not have to be re-entered each time the disk is formatted.

At power on the controller will read the pointer sector and then it will read into controller memory the processed flaw data. It is the user's responsibility to insure the pointer sector and the processed flaw data is in the correct format and that the flaw map itself is placed in the flaw map.

When the controller reads the processed flaw data, if the primary sector cannot be read it will try the alternate for that sector. The alternate and primary sector can be the same sector if desired. If neither the primary nor the alternate can be read, the appropriate error is reported.

The processed flaw data is arranged to allow simple and fast searching by the controller and must be in the format shown in Figures 4-7.

The processed flaw data can be a maximum of 256 bytes in size if there are two Winchesters in the system or 512 bytes if there is only one Winchester in the system. These maximum sizes are due to limits on controller memory size.

The alternate sectors must be placed in the map, however the alternate sectors can be the same as the primary sectors if desired.

All fill bytes must be as shown since the controller checks these to insure the pointer sector is valid.

In addition all track numbers and sector numbers must be in ascending order to allow binary searching.

BYTE	CONTENT	DESCRIPTION
0	0AA16	Start marker
1	Drive Type	4=SA1000, 5=Q2000, 6=SA1100
2	0	Fill Byte
3	0	Fill Byte
4	Sector*	Pointer to first primary sector of pro-
5	Head	cessed flaw data
6	Cylinder - LSB	
7	Cylinder - MSB	
8	Sector*	Pointer to alternate first sector for
9	Head	processed flaw data
10	Cylinder - LSB	
11	Cylinder - MSB	
12	Sector*	Pointer to second primary sector of pro-
13	Head	cessed flaw data
14	Cylinder - LSB	
15	Cylinder - MSB	
16	Sector*	Pointer to alternate second sector of pro-
17	Head	cessed flaw data
18	Cylinder - LSB	
19	Cylinder - MSB	
20		Pointers to raw flaw data
.		(Same format as above)
.		
.		
36		
37	0	Not used
.	.	
.	.	
.	.	
100	$0FF_{16}$	Fill
101	0	
102	FF_{16}	
103	0	
104	FF_{16}	
.	.	
.	.	Alternating 0, FF's
.	.	
127		Fill

*A zero in the first byte of the disk address terminates the string.

Figure 5. Flaw Map Pointer Sector Format.

BYTE	MNEMONIC	DESCRIPTION
0	NT	Number of flawed tracks on the disk.
1,2	T1	Bad track number* (LSB first)
3,4	O1	Offset to sector table in bytes (LSB first)
5,6	T2	Bad track number
7,8	O2	Offset to sector table in bytes
		. (repeated NT times)
01	NS1	Number of bad sectors on first bad track (0 => entire track is bad)
01+1	S1	List of bad sectors on first bad track
01+2	S2	
.	S3	
.	S4	
02	NS2	Number of bad sectors on second bad track
02+1	S1	List of bad sectors on second bad track
.	S2	
.	S3	
.	S4	

*Track Number = (Cylinder address * number of moving heads) + head address

Figure 6. Processed Flaw Map Data Sector Format

BYTE	CONTENT (HEX)	DESCRIPTION
0	AA	Marker
1	4	SA1000 drive
2	0	
3	0	
4	2	Sector 2
5	0	Head 0
6	0	Cylinder 0
7	0	
8	3	Alternate for processed flaw data
9	0	
10	0	
11	0	
12	0	Terminator (only 1 sector of data)
.		used by controller
.		
.		
100	FF	
.	0	
.	FF	
.	0	
.	.	
.	.	
.	.	
127	0	

Figure 7. Flaw Map Pointer Sector Example

BYTE	CONTENT	DESCRIPTION
0	5	Number of flawed tracks
1,2	0,0	Track 0 flawed (flaw map itself)
3,4	17,0	Offset to sector table (LSB first)
5,6	5,0	Track 5 flawed
7,8	21,0	Offset
9,10	111,0	Track 111 flawed
11,12	23,0	Offset
13,14	171,0	Track 171 flawed
15,16	24,0	Offset
17	3	Number of flawed sectors on track 0
18	1	Sectors 1,2,3 are the flaw map itself
19	2	
20	3	
21	1	Number of flawed sectors on track 5
22	31	Sector 31 is flawed
23	0	All sectors on track 111 are bad
24	6	Number of flawed sectors on track 171
25	2	Sectors 2,8,10,30,31,32 are flawed on
26	8	track 171
27	10	
28	30	
29	31	
30	32	
31	—	Not used by the controller
•		
•		
•		
127		

Figure 8. Processed Flaw Map Data Example

D. PROCESSING THE RAW FLAW DATA

The method of reporting Winchester flaws is determined by the drive manufacturers. Some manuacturers report flaws by giving the track, head, byte from index and number of bits in the flaw. Others report a sector, head and track and assume a known format (e.g. 256 bytes/sector with so many bytes of overhead, etc.). Flaws are typically found by the drive manufacturer's analog techniques which require special equipment. A flaw does not necessarily mean a sector cannot be read/written, but simply that the flaw will result in higher soft error rates. Thus, simply scanning a disk may not be sufficient to find all flaws on a disk (i.e. the manufacturer's raw flaw data must be used).

The determination of the sector in which a flaw will appear depends on many factors. The disk format, head step/switch offsets and interleave must all be taken into account. For soft sectored drives the rotational tolerance of the drive also plays a key role in determining which sectors to flaw.

Accordingly, SMS has developed a set of rules for processing the manufacturer's flaw data. These rules have been implemented in the FW Installation and Test Program (see section V-C) and are described in the FW Installation and Test manual.

VIII. SYSTEM MAINTENANCE

A. PREVENTIVE MAINTENANCE

Air Filter Cleaning

The air filter on the rear of the FWT chssis should be cleaned periodically. To remove the filter simply turn AC power off and pull the filter out. It can be cleaned in soap and water if desired.

Floppy Disk Maintenance

A head cleaning kit (available from Shugart, SAlll P/N 54612) can be used to clean the floppy read/write heads. The normal preventative maintenance, recommended by Shugart, is to clean the heads once a month at 25% duty cycles or 40 hours of usage, whichever occurs first. An alternative is to clean the heads when a read error occurs (CRC error) especially when excessive diskette wear has been noticed.

Cartridge Tape Maintenance

A reasonable maintenance schedule assures trouble-free operation of the cartridge tape drive. Check the heads frequently for any sign of dirt or oxide accumulation. At the first sign of any dirt, clean the entire tape path thoroughly, but gently. Be especially careful with the delicate heads.

A cotton swab makes a convenient cleaning tool, but make sure the wodden portion never touches the heads. Useful solvents include 1.1.1 trichloroethane and isopropyl alcohol. Do not use any of the following:

- o acetone or lacquer thinner
- o aerosol sprays
- o rubbing alcohol

Do not use too much of any solvent. Never allow the solvent to penetrate the bearing of the capstan motor; the solvent can destroy the bearing lubrication.

B. ENCLOSURE DISASSEMBLY

The FWT chassis is a modular assembly and each major component can be easily removed for testing or replacement.

Drives

Each drive is held in place by four screws on the bottom of the chassis. To remove a drive, simply remove these four screws, disconnect the AC, DC and control cables, and pull the drive out.

NOTE: The DC cable to the Shugart SA1000 Winchester drive is difficult to remove because of poor placement of the connector on the drive. One side of the clamp has been cut to facilitate removal.

Formatter

The formatter pc board can be removed by disconnecting the drive cables, the DC cable and the seven plastic nuts. All cables are keyed to facilitate reinstallation.

Power Supply

The power supply is held in place by four screws in the back panel of the chassis. The power supply and power distribution board located next to the power supply must be removed as one assembly. The power distribution board is mounted by six screws to a side panel.

To remove, disconnect DC cable harness from the power supply (six lugs), the drive AC power cable from the power distribution board (3 lugs), the fan AC power cable from the distribution board (2 lugs), and the AC input cable from the distribution board (3 lugs). Then remove the screws holding the power supply and distribution board in place and remove the assembly.

TABLE 13. FWT MAJOR REPLACEABLE ASSEMBLIES

ITEM NO.	SMS PART NUMBER	DESCRIPTION	FIGURE NO.
1	0003941-0001	Panel, Rear	9
2	0003944-0001	Hinge, Modified	9
3	0003970-0001	Power Supply Assy.	9
4	9000923-0001	Power Supply	Ref.
5	9000932-0001	Fan, 115 volt	9
6	9000932-0002	Fan, 230 volt	9
7	0003963-0001	AC Input Harness	9
8	0003964-0001	Fan Cord Assy.	9
9	9000928-0001	Switch, Rocker	9
10	9000281-0001	Fuse Holder	9
11	0003976-0001	Filter, Air	9
12	0003947-0001	Barrier, Filter	9
13	0003943-0001	Frame, Air Filter	9
14	0003937-0001	Top Cover, Hinged	8
15	0003938-0001	Chassis	8
16	0003978-0001	Cable Assy., Drive Data	8
17	0003951-0001	Cable Assy., Interface I/O	8
18	0003950-0001	Cable Assy., Drive Signal (HD and FD)	8
19	0003966-0001	DC Wire Harness (Formatter)	8
20	0003967-0001	DC Wire Harness (FD0500)	8
21	0003962-0001	AC Wire Harness (SA800 Comp.)	8
22	0003962-0002	AC Wire Harness (SA850 Comp.)	8
23	0003987-0001	Insulator, AC Dist. PWB	8
24	0003957-0001	PWB Assy., AC Distribution	8
25	0003956-0001	Wiring Diagram (Chassis)	Ref.
26	0003955-0001	Lock-Block, Motor	8
27	0003935-0001 (0004006-0001)	Bezel, Finished Rack Mtg.	8
28	0003945-0001	Bezel, Finished Desk Top	8
29	0003954-0001	Spacer, Bezel, Desk Top	8
30	0003869-0001	Label, Overlay, FWT Series	8
31	0003421-0001	Insulator, Cover	8
32	0003936-0001	Cover, Desk Top	8
33	9000344-0001	Foot, Plastic	8
34	1001943-0001	Top PWB Assy., FWD0101 Formatter	8
36	---	Floppy Drive: All floppy drives have an SMS label which specifies the SMS assembly number to order. By ordering this assembly number, the correct options will be installed. An example of an assembly number (ASSY NO) is 0003692-0001.	8
37	---	Winchester Drive: All Winchester drives have an SMS label attached which specifies the SMS assembly number to order. By ordering this assembly, the correct options will be installed. An example of an assembly number (ASSY NO) is 0003917-0005.	8

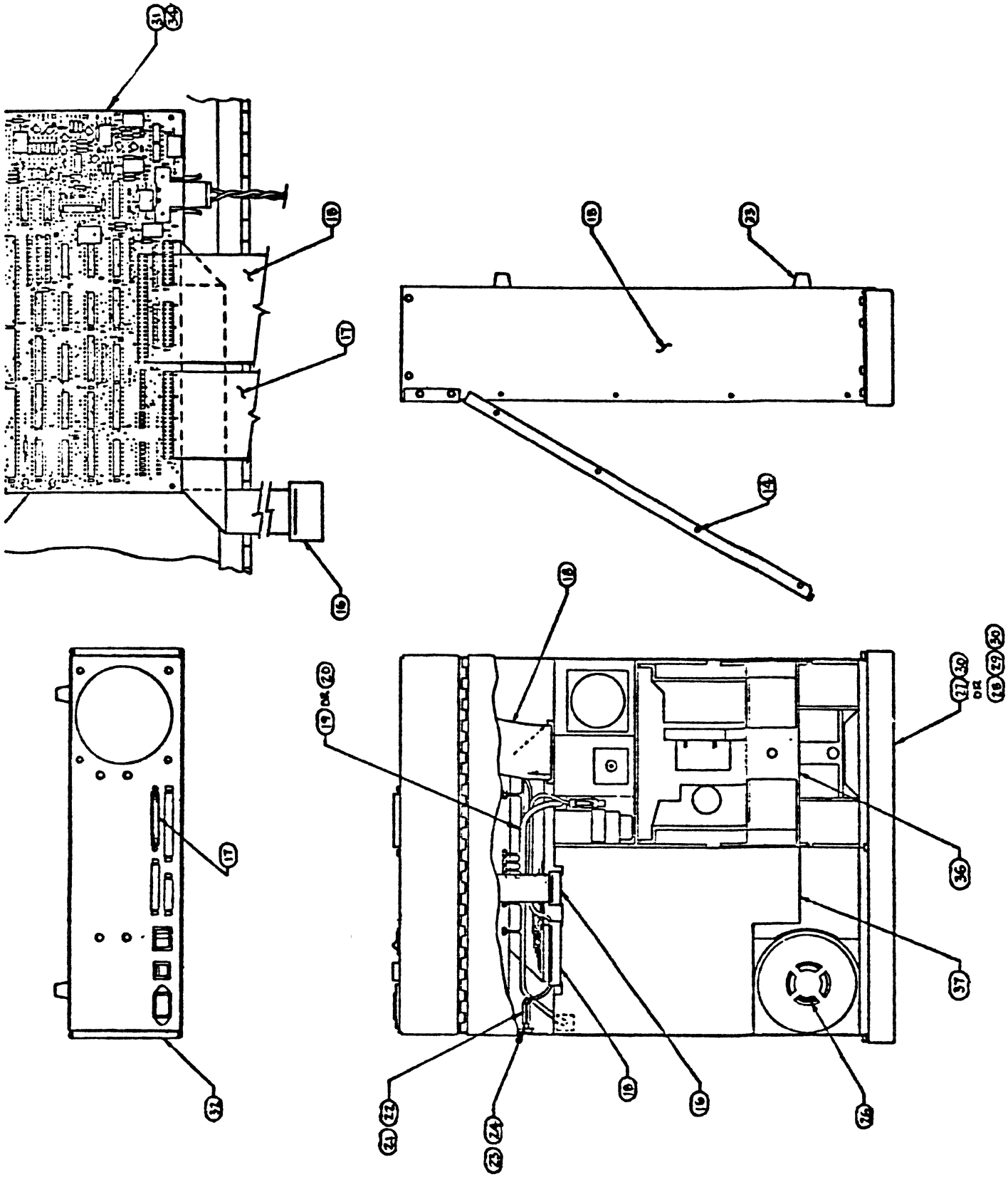


Figure 9. Chassis Assembly, FWT System

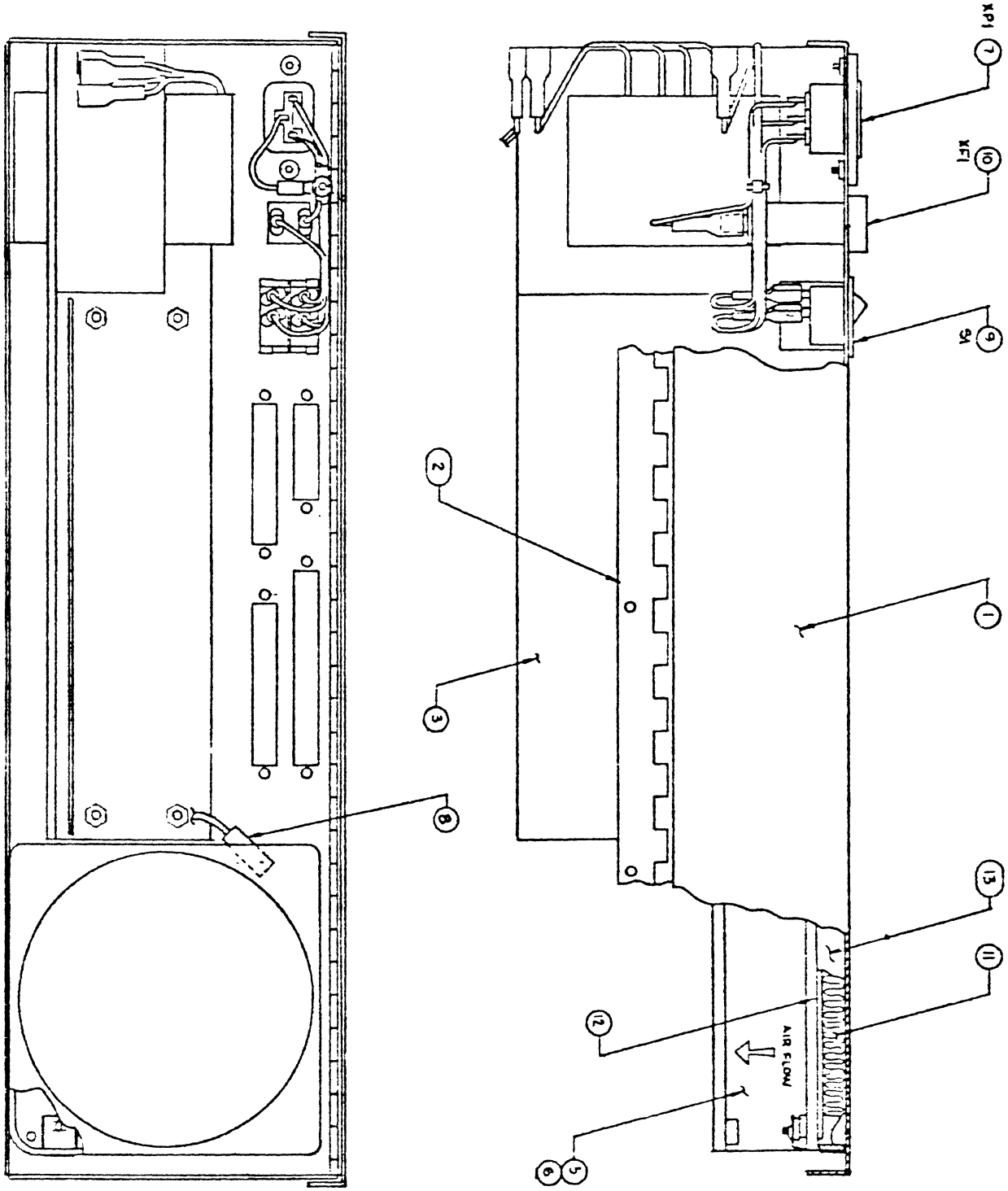


Figure 10. Rear Panel Assembly, FWT System