Friden

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SERVICE MANUAL

Model 21 Processor

Friden, Inc.
SAN LEANDRO, CALIF

SERVICE MANUAL

MODEL 20/21 PROCESSOR

SYSTEM TEN

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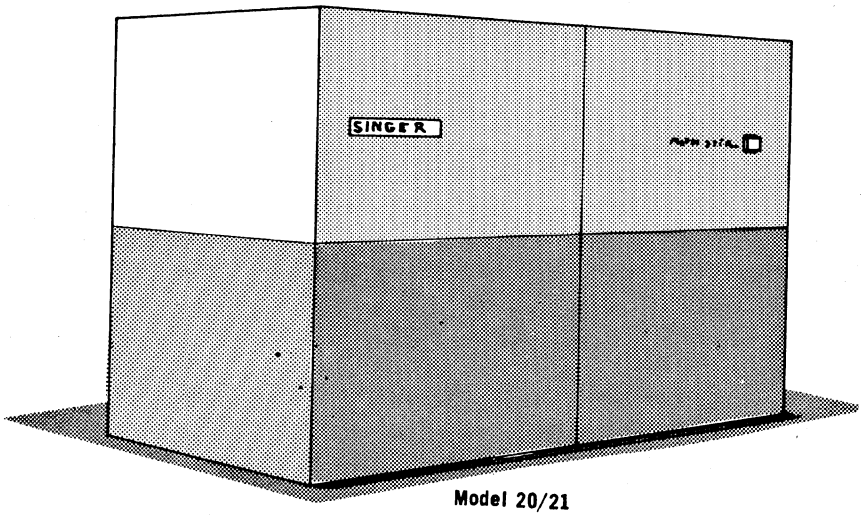
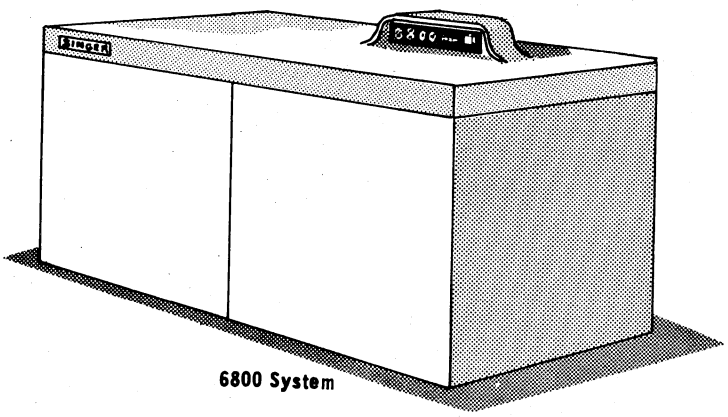
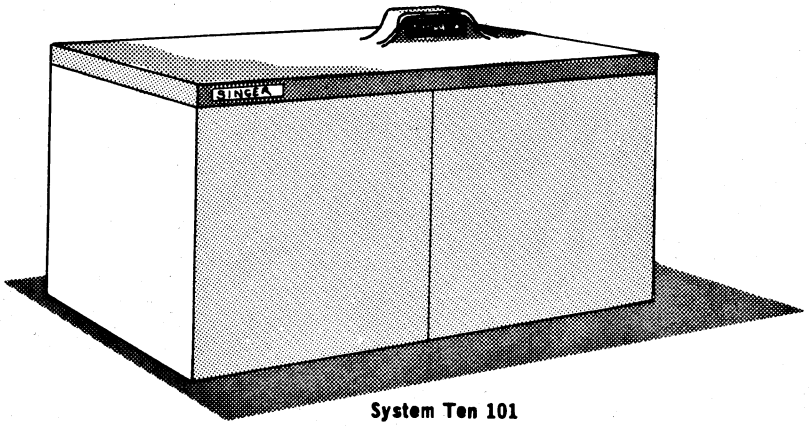


Model 20/21



6800 System



System Ten 101

1-0.0 GENERAL INTRODUCTION

This manual describes the organization and hardware operation of the Model 20, Model 21, 6800, and 101 processors. This section of the manual provides a general description of the equipment, its purpose, and relationship to other equipment. Later sections describe the principals of operation, installation, and maintenance information. Generally throughout this manual, the hardware portion of the Model 20, Model 21, 6800, and 101 is called the processor. Individual differences of the various models are described only where the differences affect the service of the equipment.

1-1.0 EQUIPMENT DESCRIPTION

The basic cabinet configurations of the Model 20/21, 6800, and 101 processors are shown in the artist's concept on the opposing page. The processors are business-oriented, stored program digital computers that combine small size, and medium performance, with the ability to service several independent users simultaneously.

The 6800 system and System Ten 101 are special versions of the basic Model 21 processor, and for service considerations, they can be treated as a Model 21 with limited memory and IOCs.

The processor hardware can be thought of as four seperate, but interworking units,
Main Memory
Arithmetic and Control Unit (ACU)
File Access Channel (FAC) and
Input/Output Controllers (IOC).

1-1.1 MAIN MEMORY

The main memory provides random access core storage for a minimum of 10,000 to a maximum of 110,000 6-bit characters (the 6800 system and 101 processor are limited to a maximum of 30,000 characters of storage in main memory). Memory modules can be added to a minimum system in increments of 10,000 characters each until the maximum capacity of the system is reached. Additional and/or redundant character storage is available through the file access channel to magnetic disc or tape units. All transfers into or out of the main memory are performed by the arithmetic and control unit.

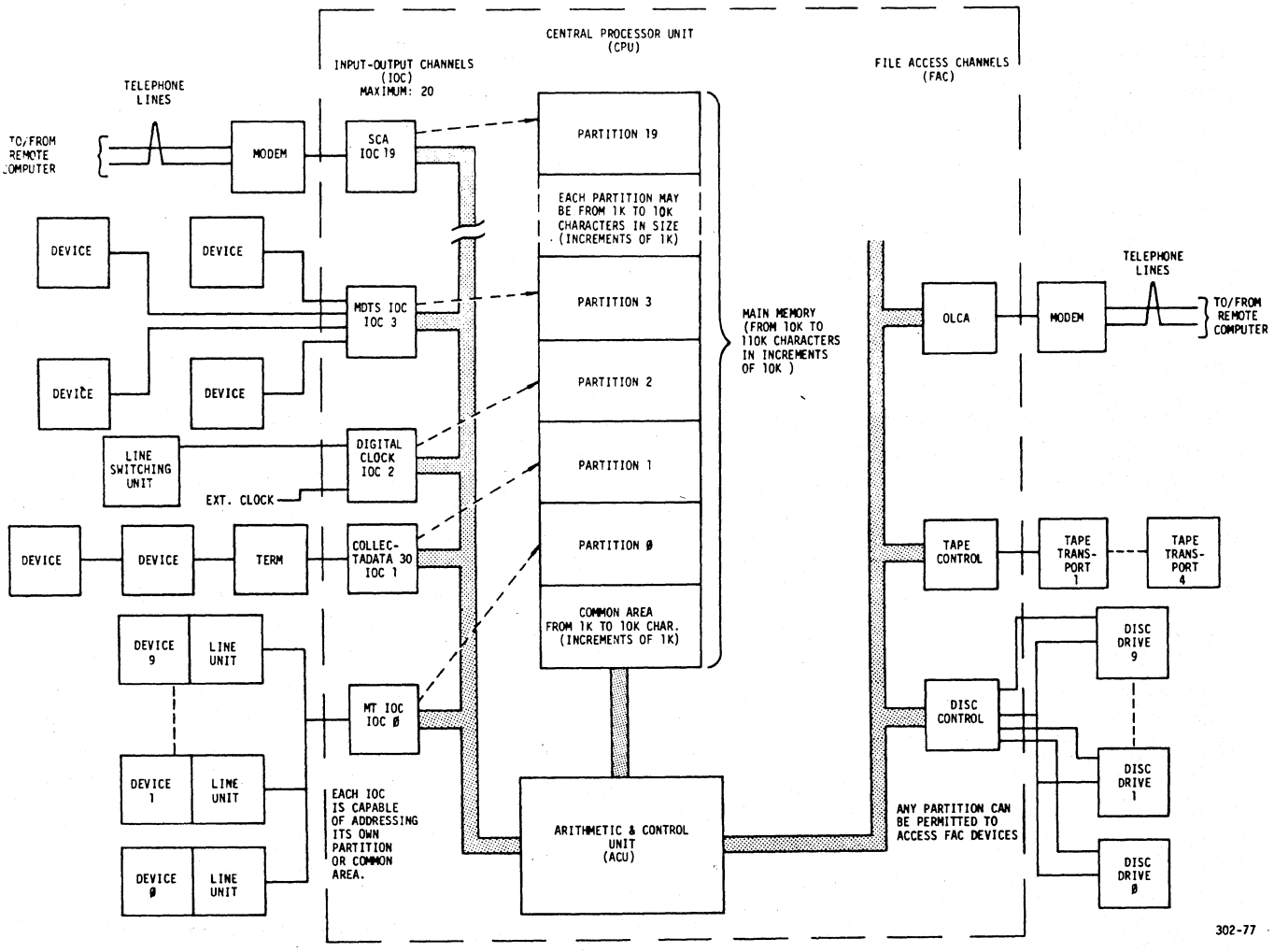
The main memory is electrically divided into user areas (called partitions) that correspond to one IOC for each partition. The size of each partition is determined by hardware jumpers on its IOC card, and can be from 1000 characters to 10,000 characters each. However, the total of all memory allotments cannot exceed the amount of memory that is contained in the system.

In addition to user partitions, the main memory has a common portion that is available for use by any of the partitions (IOCs). The size of common memory is governed by jumpers on the RBA/RBX card within the ACU, and is adjustable from 1,000 characters to 10,000 characters for the Model 20, 29,000 characters for the 6800 and 101 systems, and 65,000 characters for the Model 21. The Model 21 can be patched for a greater number, but is limited by software standards to 65K. All partitions are serviced in sequence, and only one character at a time can enter or exit main memory.

1-1.2 ARITHMETIC AND CONTROL UNIT

The Arithmetic and Control Unit (ACU) fetches instruction and data from memory, operates on the data, and stores the results in main memory. The ACU also transfers data between main memory and the IOCs or FAC. All interface to main memory is through the ACU. Each user (IOC) is selected by the ACU in numerical sequence, and monopolizes the unit for a short time. The ACU limits this monoply to 37.5 ms, after which time, the first successful branch in the software program will cause a switch to the next partition. During power up and power down, the ACU stores the necessary information to allow normal processing to continue without re-loading program after each power interruption.

The block diagram below shows the relationship of the ACU to main memory, the IOCs, and the FAC. Each system will vary greatly in requirements, and only the general elements are shown in the illustration.



EXAMPLE OF A SYSTEM CONFIGURATION

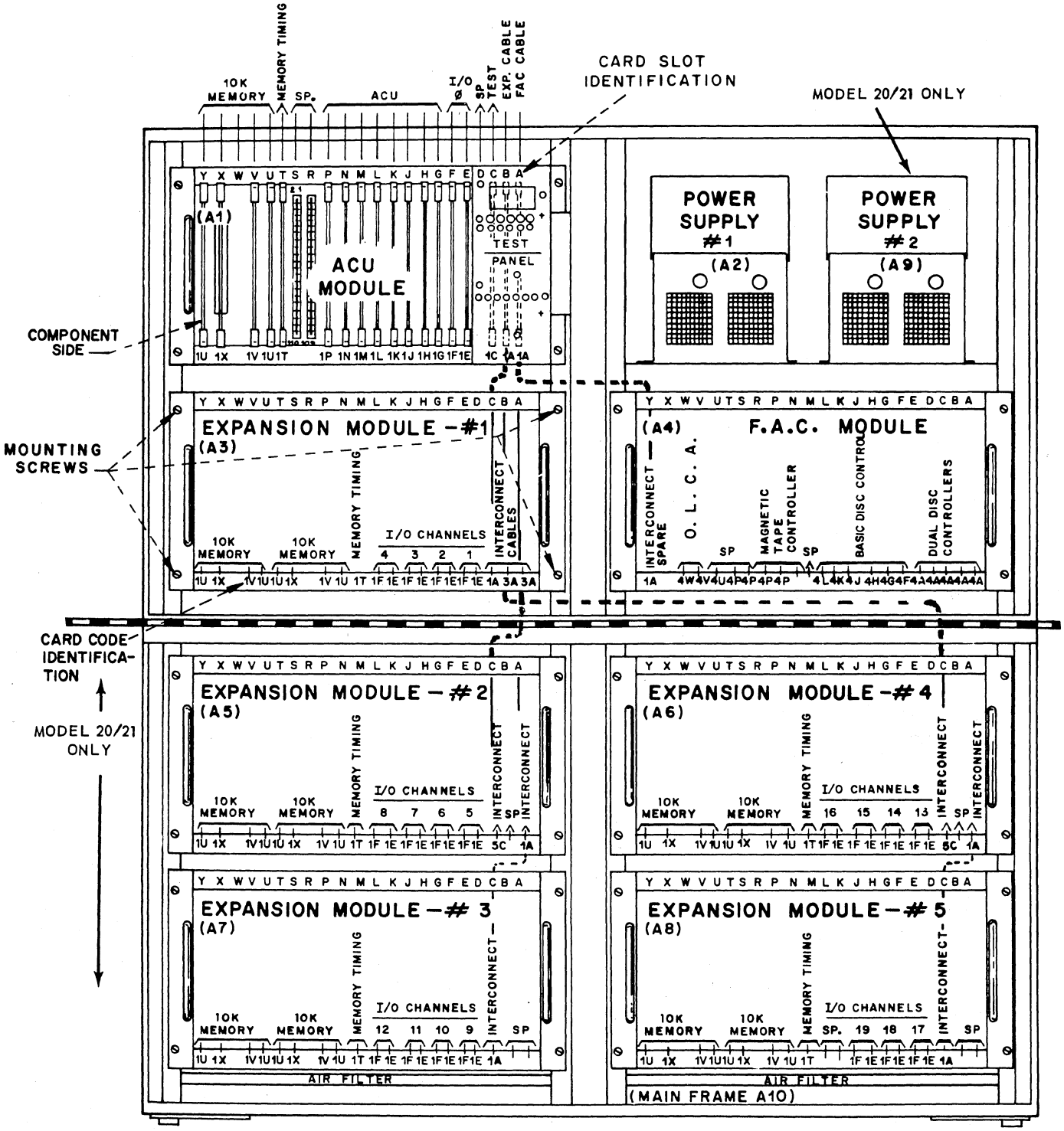
1-1.3 INPUT/OUTPUT CONTROLLERS

The input/output controllers (IOCs) provide communication between the ACU and the various peripheral devices, or through communication lines to remote computers. The type of IOC that is used for a partition depends upon the user device that is needed. A general list of the currently available IOCs is given below; a detailed description of each IOC is given in a later section of this manual.

IOC Type	Circuit Card Identification	User Device(s)
Multi-terminal IOC (MTIOC)	CH1, CH2	Workstation (typebar printer or CRT), Card Reader, Paper Tape Reader, Line Printer, Card Punch, Paper Tape Punch.
MDTS IOC	CX3, CX4 (CH3, CH4)	Retail Terminal, Manufacturing Information System.
Synchronous Communication Adapter (SCA)	CH5, CH6, CH8 (CH7 if auto dial)	Remote computer or other synchronous device. Must use modem if long distance is involved.
Asynchronous Communication Adapter (ACA)	AC1, AC2, AC4 (CH7 if auto dial)	Remote asynchronous devices, including computers. Must use modem if long distance is involved.
Asynchronous Terminal Adapter (ATA)	TA1, TA2 (CH7 if auto dial)	Model 7102 or similar OEM devices. mod 30, TTY 33
Digital Clock	CL3, CL4	External Clock Interface and/or Terminal switching Unit.
Collectadata 30 IOC	IO1, IO2	Collectadata 30 Terminals.

Each IOC is capable of addressing any character within its memory partition, or the common area of memory. IOC partition size is determined by hardware jumpers that are located on one of the IOC cards (see the individual IOC description for patching procedures). Partition size is always 1,000 to 10,000 characters, in 1K increments. Common area in the Model 20 is limited to 10,000 characters, but the 6800, and 101 systems can have all memory as common, except for the minimum 1K for each IOC that is installed. The Model 21 hardware follows the same rules, but because of software limitations, should not be patched for a common size that is greater than 65K.

The Model 20 has a Priveledged area of common memory that, if patched by jumpers on the RBA card, allows only those IOCs that are patched for Priveledged access into that portion of memory. This feature applies only to the Model 21, 6800, or 101 systems.



PROCESSOR MODULE ARRANGEMENT

1-1.4 FILE ACCESS CHANNEL

The File Access Channel (FAC) provides interface to magnetic disc storage and magnetic tape storage. The FAC contains the controllers that direct and control the magnetic storage devices under direction of program and the ACU. Data is transferred to disc units in groups of 100 characters each, preceded by a leader and track ID, and followed by a trailer. Magnetic tape transfers are not limited to a specific number of characters, and may vary considerably in data field length, with controlling or identifying characters preceding and following the data.

In some processors the FAC may also include an on-line communication adapter (OLCA) that is used for synchronous communication to another computer. This device may be cabled to the other computer if local, or it may have a modem that interfaces to either a leased line or the dial telephone system.

1-2.0 EQUIPMENT CONSTRUCTION

The Model 20/21 processor is physically a main frame that houses up to seven modules and two power supplies. The 6800 and 101 systems have only three modules and one power supply. The figure on the opposing page shows the module arrangement for the processor main frame. The 6800 and 101 processor modules are confined to the area above the large dotted line. And because of the limited need, the 6800 and 101 have only one power supply. The general construction of the modules provides for up to 22 circuit cards to be installed into rear connectors that directly interface to the motherboard. The modules are interconnected by cables that connect to designated card slots (shown by dotted lines on the illustration). The four basic modules are:

ACU module
Expansion module
FAC module
Power supply

1-2.1 ACU MODULE

The ACU module contains nine circuit cards that comprise the ACU (including the Test Panel), five cards that make up the minimum memory (10K storage and the associated circuits), two expansion cable slots, and one IOC position (two slots). The IOC within the ACU module is partition zero, the only partition that is capable of performing the SET MODE instruction.

1-2.2 EXPANSION MODULES

Expansion modules are used to increase the total capacity of the processor. Each expansion module can add 20K more memory, and four IOCs. The memory capability can be added in 10K units, but should be placed in the lower addresses first (M,P, S,T and U). In the full size processor (model 20/21) the memory should be added to the lower numbered expansion modules first.

The IOCs have no direct effect on the memory expansion, and can be installed at random. However, the partition number that is assigned to an IOC is determined by the physical position within the processor. If an IOC position is left open, and filled at a later time, all higher partitions are moved up in memory, making it necessary to re-load the programs in those higher partitions.

MEMORY USE, INSTRUCTION AND DATA FORMATS

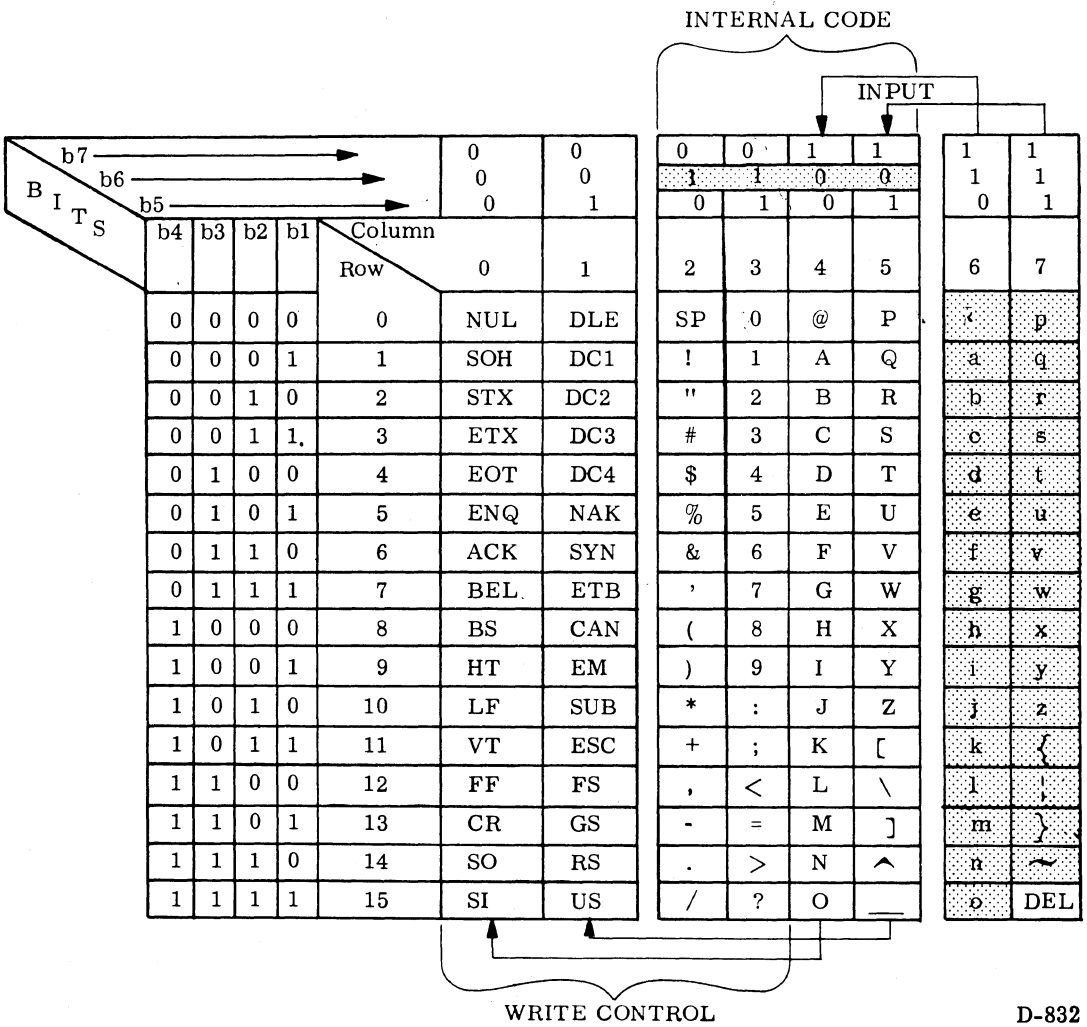
SECTION 2

CONTENTS

Bit 7	1	ZONE BITS	Determine columns on ASCII chart
Bit 5	1		
Bit 4	0	VALUE BITS	Provide BCD value of numeric characters; Determine rows on ASCII chart
Bit 3	1		
Bit 2	0		
Bit 1	1		

(This figure shows the letter U.)

CHARACTER STRUCTURE



b4	b3	b2	b1	Row	Col 0 (000)	Col 1 (001)	Col 2 (010)	Col 3 (011)	Col 4 (100)	Col 5 (101)	Col 6 (110)	Col 7 (111)
0	0	0	0	0	NUL	DLE	SP	0	@	P	`	p
0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
0	0	1	0	2	STX	DC2	"	2	B	R	b	r
0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
0	1	1	1	7	BEL	ETB	'	7	G	W	g	w
1	0	0	0	8	BS	CAN	(	8	H	X	h	x
1	0	0	1	9	HT	EM	)	9	I	Y	i	y
1	0	1	0	10	LF	SUB	*	:	J	Z	j	z
1	0	1	1	11	VT	ESC	+	;	K	[	k	{
1	1	0	0	12	FF	FS	,	<	L	\	l	|
1	1	0	1	13	CR	GS	-	=	M	]	m	}
1	1	1	0	14	SO	RS	.	>	N	^	n	~
1	1	1	1	15	SI	US	/	?	O	_	o	DEL

ASCII CODE CHART

2-1.0 MEMORY USE, INSTRUCTION AND DATA FORMATS

The Arithmetic and Control Unit (ACU) performs arithmetic operations, manipulates data, and provides access to main memory by the IOCs and FAC. These operations are directed by instructions that are stored in memory and retrieved by the ACU. The instructions are executed in sequence except for branch instructions that may cause the ACU to begin operation at a different memory address. Under the control of a stored program and/or hardware, the ACU can commence or stop executing any program in storage, it may alter an instruction or replace the entire program, it may request additional inputs or perform subroutines called for by condition codes, or may provide abnormal condition indication (status). During the instruction fetching portion of the ACU operation, the ACU examines the contents of memory in groups of ten characters (actually two groups of five each). It is because of this that all instructions (words of ten characters each) must begin at an address that is evenly divisable by ten. Other than this restriction, program and/or data can reside anywhere in the IOC partition of memory, or anywhere in common memory, except the protected area.

2-1.1 CHARACTER USE AND STRUCTURE

The ACU uses and stores in memory a six-bit character. Since the ASCII code is a seven bit code (plus parity), the IOC device must convert the incomming characters to the internal ASCII sub-set, and the outgoing characters back to the full ASCII equivalent. The ASCII chart on the opposing page has been modified to show the conversions that are made for the ACU hardware.

Normally, the 6- and 7- bits of the processor internal code are opposite for the alphabetic characters. Therefore, when characters are entered into main memory, the 6-bit is dropped. The result is the loss of distinction between upper and lower case letters, and the loss of the control characters in columns 0 and 1.

Characters that are transfered from memory to an IOC device are reconstructed by inverting the 7-bit from storage, and placing that bit in the 6-bit position. The 7-bit remains unchanged, and the character is recognized as the upper case letter of the ASCII code that was stored. When an instruction calls for a (WRITE) control code, the 6-bit is created as for a normal character, but then the 7-bit is forced to zero. This causes characters that were stored in memory as those in columns 4 and 5 to be recognized as the control codes from columns 0 and 1. (Example: a WRITE Control C transmits an ETX)

The lower four bits of a character provide a numeric value from 0 to 15, corresponding to the sixteen rows of the ASCII chart. The 5- and 7- bits determine the column within the chart, and are called zone bits.

The use of a character determines its structure and categorizes it into one of two types: data or instruction. A data character is the basic unit of a word or field that is meaningful to the operator; an instruction character is the basic unit of a ten-character word and/or a many word program that is meaningful to the ACU hardware. Data words may be entered at any selected location within the partition or common area of memory, and may vary greatly in length. Instruction words are always stored at an address that is evenly divisible by ten, and they are always ten characters long. All memory addressing is by character position. The six individual bits of the character are addressed simultaneously, and are considered as one memory location.

2-1.2 DATA WORD AND FIELD

A data word or field consists of one or more contiguous (continuously-adjacent) characters that are treated by an instruction as a single unit. A data field or word can be located anywhere in the memory that is available to the I/O device, and has no hardware restrictions that require an even or divisable-by-ten address. It is addressed by the leading character position which resides at the lowest numbered character position in memory. As the field is read (or written into) the ACU increments the internal addresing structure one count for each character. In an arithmetic instruction, the data word is a decimal number, with the leading character as the most significant digit. In that case, the ACU adjusts the addressing before the number is read so that the least significant digit is acted upon first. In an arithmetic instruction, the internal memory addressing is counted down as the word is read.

2-1.3 INSTRUCTION WORD

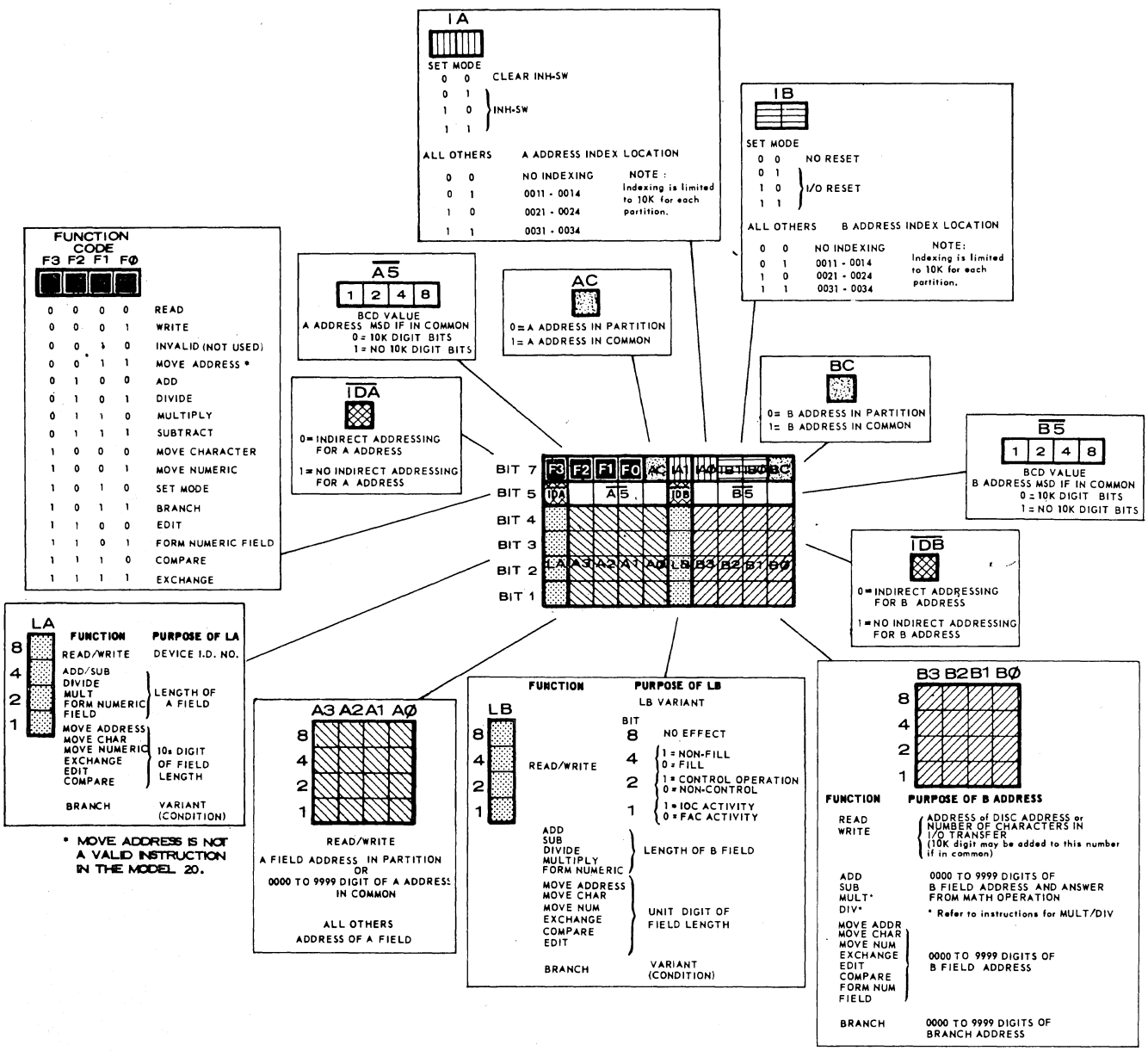
Instruction words are the basic units that comprise the computer program. The address of each instruction word must be evenly divisable by ten (this is unlike the data word which can have its leading character at any location). One other condition is imposed upon all instruction words: The lower four bits of any character within an instruction word must not represent a BCD value that is greater than a decimal nine. Specific details of the instruction word operation and conditions are given in section 3 of this manual.

An instruction word is always ten characters long, and causes the processor to perform the specified operation. To perform this operation, the ACU will step through hardware routines that resemble response to software instructions. However, these routines are internal, and are performed without the aid of external program. Each instruction word consists of modular groups of bits which identify data fields, define what is to be done with the fields, set up the conditions under which the operation will be performed, and specify the location into which the answer or result will be placed.

The figure at the right shows a composite block of the instruction word bits. The basic units of the instruction word are expanded upon in the surrounding blocks.

The basic portion of the instruction word is the Function Code (also called the Operation, or "Op" Code) that sets up the initial conditions for the operation that is to be performed. During the operation, the hardware sequencing will change the internal function code many times. Each ACU function, such as READ, WRITE, BRANCH, etc., is performed under hardware direction that is implimented by changing the internal function code. These internal changes are completely automatic, and depend upon the original function code, and the conditions that are encountered during the performance of the instruction.

Data that is involved in the performance of an instruction is usually identified by the A and B addresses. The exception to this is the disc instruction, where the B address tells the location of the disc address in memory. The AC and BC bits indicate whether the A or B address is in partition memory or in common memory. In all of the processors except the model 20, there is the possibility of an A5 and B5 character. These are the MSD or 10K digit of the address, if the address is in the



common area of memory. Notice that unlike the main portion of the address, the A5 and B5 characters are structured laterally within the instruction word.

The Model 20 processor is limited to 10K addressing, even in common, because of a requirement that the 5 bits of all characters in an instruction must be 1s. The Model 20 hardware will set a data check condition if this requirement is not met. A data check will be set in all models if the lower four bits of any instruction character exceed a binary 9.

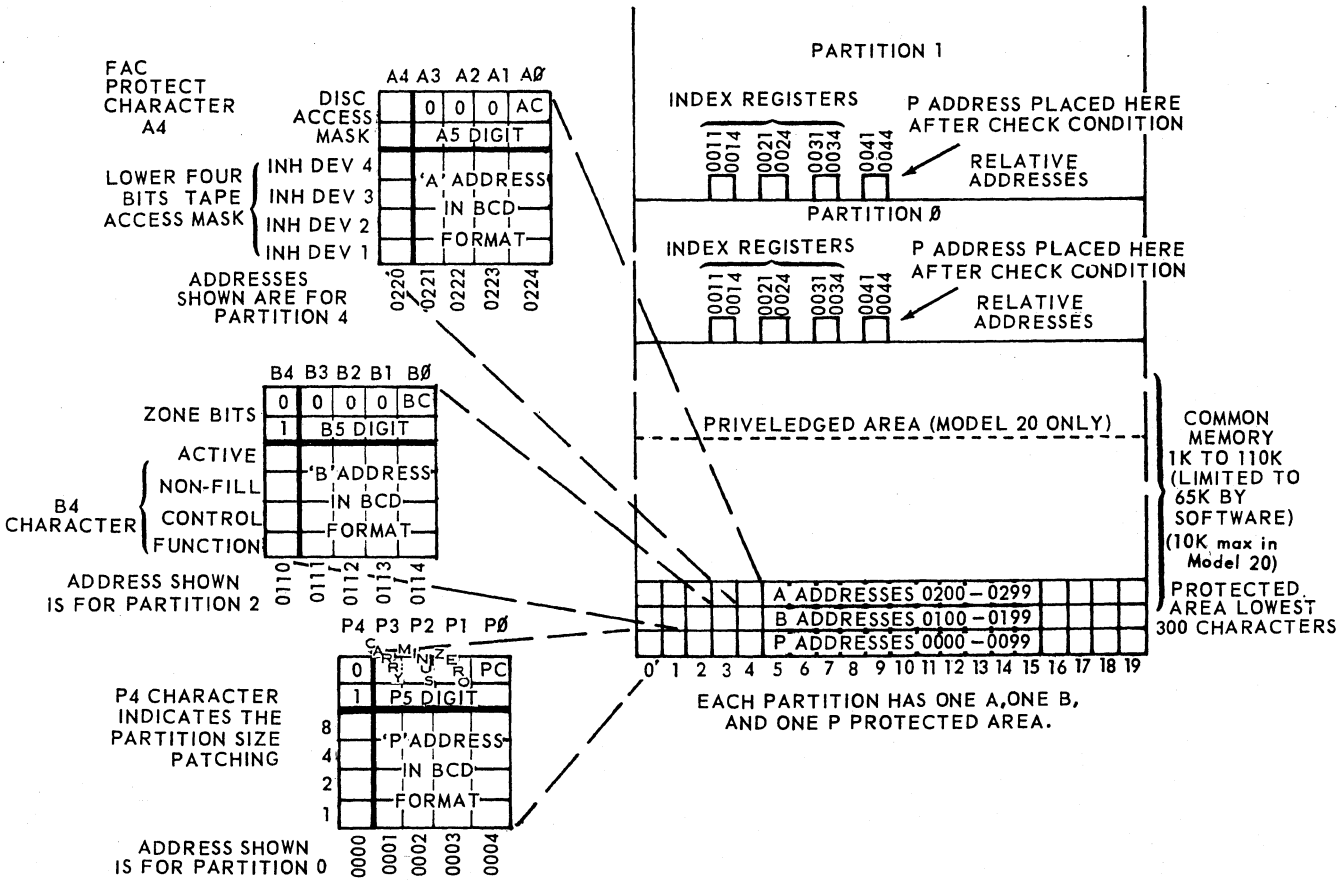
The LA and LB characters identify the device number when performing a READ or WRITE operation, specify BRANCH conditions, or the length of field for other instructions.

2-1.3 INSTRUCTION WORD (Continued)

The index codes, IA and IB, direct the hardware to one of three automatically located addresses in memory. The numeric portion(lower four bits) of the four characters at the specified location are then added to the A and/or B address (as specified by IA and IB) before the A and B addresses are used. The four-character areas of memory that are located automatically by the IA and IB bits are considered to be registers, even though the area is not restricted by hardware to that use. The index register areas of memory can be used for data or instructions, without restrictions (other than the normal restrictions that apply to all memory).

2-2.0 MEMORY ORGANIZATION

The figure below is a graphic representation of a portion of the processor memory. The large divisions represent the partitioning into common and individual user areas of memory. The small blocks within the individual partitions represent the index register areas of that partition. The address of these registers is hardware assigned relative to the zero address of the partition. For example, the first index register within a partition begins at the eleventh character position, and includes the characters to the fourteenth character position. If the size of a lower numbered partition is changed, or if the size of common is changed, the physical location of the index register is changed, but the relationship to the zero address of the partition remains the same.



2-2.1 PROTECTED AREA

The first three hundred character positions in memory are called the protected area. This area is contained within the Common area of memory, and is used by the ACU as a temporary storage area for pertinent information about the instruction that is in progress in each partition, or the instruction address that will be used when the partition is next serviced by the ACU.

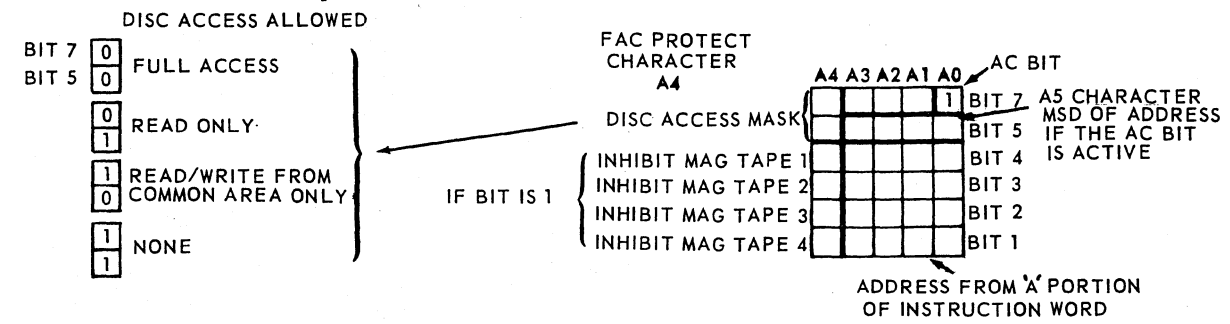
The protected area can be examined by any partition, but can only be altered by entry from the Test Panel, or by partition zero under the SET MODE instruction. Normally the protected area is used only by the ACU as a placemarker for partitions that are not being serviced. If the processor power is failing, the information from the active partition is placed into protected memory. Because the program addresses for all the other, inactive, partitions are already stored, processing begins again after a power failure without a loss of data.

The A and B addresses are stored in the protected area during Read and Write operations. The stored A and B addresses are used by the ACU during Interrupt cycles of the Read or Write operation. Each time an A or B address is used in this way, it is advanced by one number, placing the next character address in position to be used for the next interrupt cycle. This procedure is explained in greater detail under Read and Write, in section 3 of this manual.

Each I/O channel is assigned a partition in memory (by the physical position of the I/O cards), and is also associated with one A address, one B address, and one P address in protected memory. The explanations that follow for the A, B, and P addresses describe the uses within one partition. The uses and restrictions apply equally to all partitions.

A ADDRESS

The A address area (0200 to 0299) contains a series of five-character A addresses, one for each I/O. The A address, as mentioned above, is from the A portion of a READ or WRITE instruction word. However, the first character (A4) of the protected A address is the FAC Protect Character. This character (A4) is not altered by the ACU (except by special operator or program intervention) and controls which of the FAC magnetic tape or magnetic disc devices can be used by the associated partition. The A4 character can be examined by addressing a one character WRITE from: the partition number times five, plus 200 (with the AC bit active). The A4 character is entered into protected memory, either from the Test Panel, or from partition zero under a SET MODE instruction. If the A4 character is any other than a space code (all zero bits) one or more of the FAC devices is restricted from use by the partition. The example below shows the meaning and restrictions that are contained in the five-character A protected area.



2-2.1 PROTECTED AREA

A ADDRESS (Continued)

Most of the characters in the A protected area are from the instruction word, and follow the rule that the lower four bits cannot exceed a binary nine. The A4 character is an exception to this rule, and can be any value, and is not checked by the ACU for a data fault. A-protected is not used by an FAC instruction.

The A address example that is shown below illustrates the bits that might be used in a customer situation. From the location of the characters in the protected area, it is determined that the user, in this case, is partition 2. The device or devices on this partition are allowed full access to the disc storage within the system. However, only magnetic tape drive number 2 is available to this partition. The type of instruction cannot be determined from the A protected area, but the active data in the instruction is located at 3941 in the Common area of memory. Notice that the 5 bits in the A0, A1, A2, and A3 characters are all 1s. In the 6800, 101, and model 21, one or more of these bits may be zero. In that case, the zeros represent the binary value of the 10K digit of the A address (providing the AC bit is a 1 as it is in the example).

0210	0211	0212	0213	0214	BIT
0	0	0	0	1	7
0	1	1	1	1	5
1	0	1	0	0	4
1	0	0	1	0	3
0	1	0	0	0	2
1	1	1	0	1	1

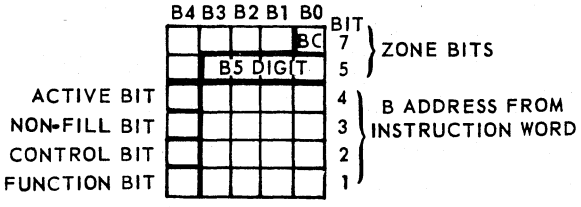
B ADDRESS

The B address area (0100 to 0199) contains a series of five-character B addresses, one for each I/O. The B area of protected memory will accomodate 20 such addresses, but abbreviated systems such as the 6800 and 101 can only use a portion of these.

The B-protected area is used during an IOC READ or WRITE to store the remaining number of characters (less one) that are yet to be transfered. This number is decremented with each character transfer until a borrow condition is created, and the LAST flip-flop is set, terminating the operation. The conditions under which the characters are transfered are controlled by the B4 character of the B-protect area of memory.

The B4 character contains the I/O channel control bits. These bits are loaded from several sources, and are not the same as the B4, or LB, portion of the instruction word. Bit 1 comes from FØ (showing a READ or WRITE condition), bits 2 and 3 come from LB bits 2 and 3, and bit 4 is placed by the ACU as a status retrieval flag. Bit 4 causes status to be read by the ACU after an I/O instruction has been completed.

The B address area in protected memory is also used at the termination of an FAC Read or WRITE instruction to store any residual count (less one). A disc instruction that ends in normal status leaves a count of 9999 (one less than zero). A disc instruction that ends in FAULT leaves a residual count of 0099 (one less than 100).



B ADDRESS BIT STRUCTURE

COMMON AREA ADDRESS

	0145	0146	0147	0148	0149	
	B4	B3	B2	B1	B0	
	0	0	0	0	0	7
	1	1	1	1	1	5
ACTIVE BIT	1	0	1	0	0	4
NON-FILL BIT	0	0	0	0	0	3
CONTROL BIT	0	1	0	0	0	2
FUNCTION BIT	0	0	0	1	0	1

EXAMPLE OF B ADDRESS

2-2.1 PROTECTED AREA

B ADDRESS (Continued)

The B-protected number that is recorded after a Mag Tape WRITE instruction (from memory to tape) is always 9999. A Mag Tape READ instruction that is filled or exceeded will also record 9999 in the B-protected area. A Mag Tape instruction that is terminated before the field is filled (the usual programming procedure) will leave a residual count in B-protected that is one count less than the number of characters that would be required to fill the remainder of the field.

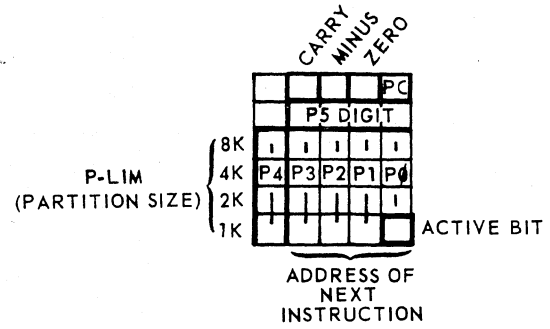
The example shows that partition 9 is busy with a normal (not CONTROL) read instruction that needs 2811 additional characters to complete the specified field. If the operation is terminated before that number of characters is received, the rest of the field will be filled with blanks (SPace codes).

P ADDRESS

The P area of protected memory contains a series of five-character addresses that are mostly used to direct the ACU to the proper program location when the partition is serviced. The lower four bits of the P4 character are a read-out of the P-LIM jumper settings on the I/O card. The read-out is only an indication to the system operator, and is not used by the ACU in any other way.

The 7-bit in the PØ character is the PC bit, indicating that the P address is in the common area of memory if it is a 1. The lowest order bit of the PØ character is set to a Ø each time the ACU begins to service the partition, and restored to a 1 when the ACU leaves the partition (except when the ACU leaves to service an INTerrupt on a cycle stealing basis). The 7-bits of the P1, P2, and P3 characters indicate the status of the condition flip-flops when the ACU switched partitions. These bits are used to re-establish the states of the condition flip-flops when the partition is serviced again. The condition flip-flops are used to direct a conditional BRANCH, if that is the next instruction that is pulled.

The P address bit structure is shown in the illustration below, along with an example of a P address that could be found in memory. The example shows the address for partition 5, which has the P-LIM jumpers set to a partition size of 7K, or 7000 characters. The last instruction in that partition ended normally, and the next instruction to be used is at location 24060 in the common area of memory. The new instruction address does not include the active bit of the PØ character. This example would be impossible in a Model 20 processor, because the zero (the 10K digit) in the 5-bit area would have caused a data check, causing a program restart.



P ADDRESS BIT STRUCTURE

COMMON AREA ADDRESS

0025	0026	0027	0028	0029	BIT
0	0	0	1	1	7
1	1	0	1	1	5
0	0	0	0	0	4
1	1	0	1	0	3
1	0	0	1	0	2
1	0	0	0	1	1

EXAMPLE OF P ADDRESS

2-2.2 INDEX REGISTERS

There are three locations of four characters each within each partition that can be automatically accessed as index registers. These index registers are not devices, but are character addresses at fixed positions within the relative partition location. Indexing bits within the instruction word cause the characters that are stored at the specified index register location(s) to be retrieved and temporarily added to the A and/or B address portion of the instruction. The index registers are relative to the partition, and are at the same relative positions within each partition. Indexing allows up to 9999 to be added to the instruction address, and can cause address errors if the modified address is greater than the partition size.

There is no restriction that reserves the index register area exclusively for indexing. Data and/or program instructions can be written into any or all of the index register areas in memory.

LOCATION 40

Location 40 within each partition is essentially an error register for storing the P count when an error is detected. The P (program) count is the memory location of the next instruction, or the next character in a READ or WRITE transfer. When the ACU hardware detects an error, the CHECK flip-flop is set, causing the contents of the (hardware) P register to be stored along with the P-LIM value into locations 0040 through 0044 in partition memory, rather than into the P protected area of memory. The P-LIM value is a single digit from 1 to : (:=10K) representing the 1K increments of the partition size patching. If an error is made during the character transfer portion of an I/O (input/output) instruction, the P count will be one count greater than the address where the error occurred. Any other error will cause the P count to be eleven (one instruction word + 1) greater than the error causing instruction. In the case of a branch instruction to a location that is greater than the partition (or common) limit, the branch will be completed before the error is discovered, and the stored P count will only reveal the branch destination, and not the source of the error.

Normal data or program can be placed into the location 40 area with no restrictions other than the regular conditions of data and program entry. However it is not advisable to place data at this location, because it will be destroyed and replaced if an error is made. Detectable errors that will cause the P address to be stored at location 40 are of three basic types that are listed below.

Address Error

- An address that is greater than the partition size.
- An address that is greater than the alloted common size.
- In the Model 20 only, an attempt to address the priveledged area of memory from a partition that is not patched for priveledged entry.
- An attempt to change data in protected memory (except through SET MODE).

Invalid Function Code

- Binary 3 (0011) used in an instruction word.
- Binary 2 (0010) used in a Model 20 instruction word.
- Binary 10 (1010) used when the SET MODE enable jumper is not installed (on the LIF card).

Data Fault

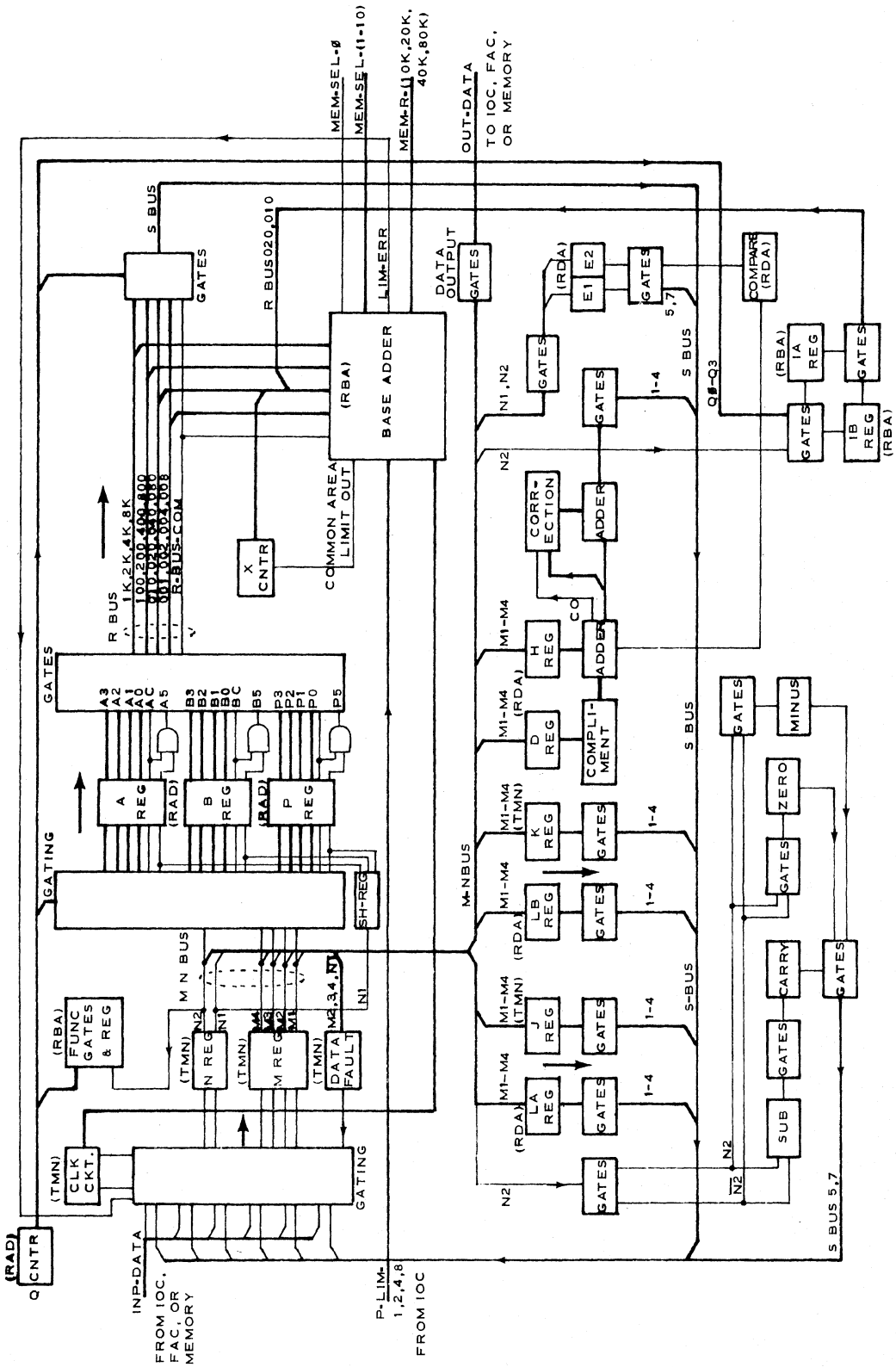
- Lack of a 1 in the 5-bit position of any character in a Model 20 instruction.
- Lack of a 1 in the 5-bit position of a disc address (the six-character data field at the B address).
- A binary value greater than 9 in the lower four bits of an instruction character, character used for indexing, or a disc address character (except for the disc unit number in all models other than Model 20).

SECTION 3

CONTENTS

MODEL 20/21 PROCESSOR

ARITHMETIC & CONTROL UNIT



ARITHMETIC & CONTROL UNIT
SIMPLIFIED BLOCK DIAGRAM

3-0.0 ARITHMETIC & CONTROL UNIT

The Arithmetic and Control Unit (ACU) is the central logic and time sequencing for the entire processor. All program instructions and data manipulations (to and from memory) are processed by the ACU. Automatic operations that are caused by certain instructions and conditions are controlled by the ACU. User (partition) sequencing and time sharing is also controlled by the ACU.

The ACU services information from only one user at a time, even though service appears to be simultaneous by quickly switching from one operation to the next. The ACU hardware is exclusively available to the partition that is being serviced, but may be released for short periods between instructions to allow INTerrupt memory cycles. Most I/O controllers process data transfers to and from peripheral devices (or communication lines) independantely from the ACU, requesting memory cycles on an INTerrupt basis. Before fetching a new instruction in the active partition, the ACU may momentarily leave the working partition to service these INTerrupt requests. Each operation, including the INTerrupt memory cycles, is performed in sequence, one at a time.

The ACU simplified block diagram on the opposing page shows the general organization and signal flow within the ACU. Data or instruction characters that come from either an I/O device, an FAC device, or from memory, enter the ACU on the INP-DATA lines. Timing signals from the ACU clock circuits gate the information from the INP-DATA lines into the M and N registers, one character at a time.

The M and N bus, a series of six data lines, routes each character to the inputs of the various registers within the ACU. As each character is entered into the M and N registers, ACU timing and enabling conditions cause the bits to enter the appropriate hardware registers (most of the timing and qualifying inputs for the registers are omitted from the block diagram). The general data flow of data within the ACU is summarized below.

- Characters are gated into the M and N registers, and thus onto the M and N bus.
- Each bit is gated into an appropriate register, where it will be acted upon or stored until required.
- The processed data is gated from the outputs of the registers, one character at a time, onto the S bus.
- Input gating clocks the characters from the S bus into the M and N registers, and onto the M and N bus.
- The data output gates are enabled, sending characters onto the OUT-DATA lines, and to an IOC device, an FAC device, or to memory.

3-1.0 DATA AND INSTRUCTION REGISTERS AND COUNTERS

The ACU contains many registers, flip-flops, and counters that temporarily store instruction and data bits, and provide sequencing for many of the ACU operations. Some of these registers and counters are named for the portions of the instruction word that they store or control. For example, the LA portion of the instruction word is stored in the LA register. Other registers are for data manipulation, and the names do not relate to their operation.

3-1.0 DATA AND INSTRUCTION REGISTERS AND COUNTERS (Continued)

The instruction word is literally taken apart as it is received from memory, and placed into hardware registers. The overall and specific content of the hardware registers determines the character, or operation, of the ACU for the duration of the instruction. The ACU will pass through many internal functions during the completion of an instruction, but is always guided and directed by the bit content of the instruction word, and the conditions that are encountered during the progress of the instruction.

When service begins in a partition, the ACU is working under the internal function BEGIN. The P count is recalled from protected memory, and that position in memory is addressed. The first five characters are "pulled" from memory, one at a time. A series of checks for data fault, branch, etc. are made, and if none of these conditions are present, the second five characters of the instruction word are pulled. The Q counter is used as the clocking source for the instruction pulling routine. The Q counter is a five-count device (Q for quinary) and is described later in this section.

As the instruction word characters are pulled from memory, the bits are placed into registers that assemble the various portions of the instruction. Each portion is completed as a seperate item, and in some cases, can cause major actions before the entire instruction word is drawn from memory. For example, a five-character BRANCH will cause a change of address without pulling or examining the second half of the instruction. A five-character branch is explained in a later portion of this section. Some of the bits from the incomming instruction word are placed into more than one register. This duplication may be for overlaping duties of the bits, or it may be a temporary storage in the event of a special condition such as an FAC cycle or a five-character branch. The listing below shows where the instruction word bits are placed as they are pulled from memory. The listing on the following page is a general summary of all of the hardware registers, their use, and location.

REGISTER DESTINATION OF INSTRUCTION BITS

CHARACTER	STATE (Q COUNT)	LOWER FOUR BITS	5 BIT	7 BIT
1st	BG3 (Q=Ø)	LA, J, LB	IDA	F3
2nd	BG3 (Q=1)	A3, B3	A5(BIT 1)*	F2
3rd	BG3 (Q=2)	A2, B2	A5(BIT 2)*	F1
4th	BG3 (Q=3)	A1, B1	A5(BIT 3)*	FØ
5th	BG3 (Q=4)	AØ, BØ	A5(BIT4)*	AC, BC
6th	BG4 (Q=Ø)	LB, K	IDB	IA1
7th	BG4 (Q=1)	B3	B5(BIT 1)*	IAØ
8th	BG4 (Q=2)	B2	B5(BIT2)*	IB1
9th	BG4 (Q=3)	B1	B5(BIT3)*	IBØ
10th	BG4 (Q=4)	BØ	B5(BIT4)*	BC

* The A and B 5-bits are deserialized in a shift register and strobed to the proper register as a complete character.

3-1.0 DATA AND INSTRUCTION REGISTERS AND COUNTERS (Continued)

HARDWARE REGISTER DESCRIPTION

REGISTER	LOCATION (P.C. CARD)	DESCRIPTION	FUNCTIONS
A	RAD	Five decimal counters	Hardware storage for the A address from the instruction word.
AC	RAX	D flip-flop	Hardware storage for AC bit.
B	RAD	Five decimal counters	Hardware storage for B address from instruction word.
BC	RAX	D flip-flop	Hardware storage for BC bit.
D	RDA	One decimal counter.	Hardware storage for the A input to the adder in A± B operations.
E	RDA	One D flip-flop and one cross-coupled latch	Hardware storage for zone bits.
F	RBA	Four cross-coupled latches.	Stores function code from instruction word.
H	RDA	One decimal counter.	Stores the B input to adder in A ± B operations.
IA	RBA	Two cross-coupled latches.	Stores IAØ and IA1 from the instruction word.
IB	RBA	Two cross coupled latches.	Stores IBØ and IB1 from the instruction word.
ID	LIX	D flip-flop	Stores the IDA bit in BG4, and the IDB bit in BG5.
J	TMN	One decimal counter.	Stores lower 4 bits of B4 (from protected) or alternate storage for LA.
K	TMN	One decimal counter.	Alternate storage for LB; data buffer; quotient accumulator; multiplier storage.
LA	RDA	One decimal counter.	Stores LA from instruction word.
LB	RDA	One decimal counter.	Stores LB from instruction word.
M	TMN	Four cross-coupled latches.	Stores the M bits, which are the lower four bits of character.
N	TMN	Two cross coupled latches.	Stores the N bits, which are the zone bits of a character.
P	RAD	Five decimal counters	Stores the P (next instruction) address from protected memory.
PC	RAX	D flip-flop	Stores the PC bit from the P protected address.
Q	RAD	One quinary (5-state) counter.	Clocks five-part operations; provides part of addressing for protected memory.
X	RBA	One decimal counter and one D flip-flop.	Addresses IOCs (SEL DIGIT and SEL GROUP); part of protected memory address.
Y	RBA	One binary counter (four bits) and two decimal counters.	Stores base address of the working partition.
Z	RBA	Three decimal counters.	Stores base address of partition using the FAC.

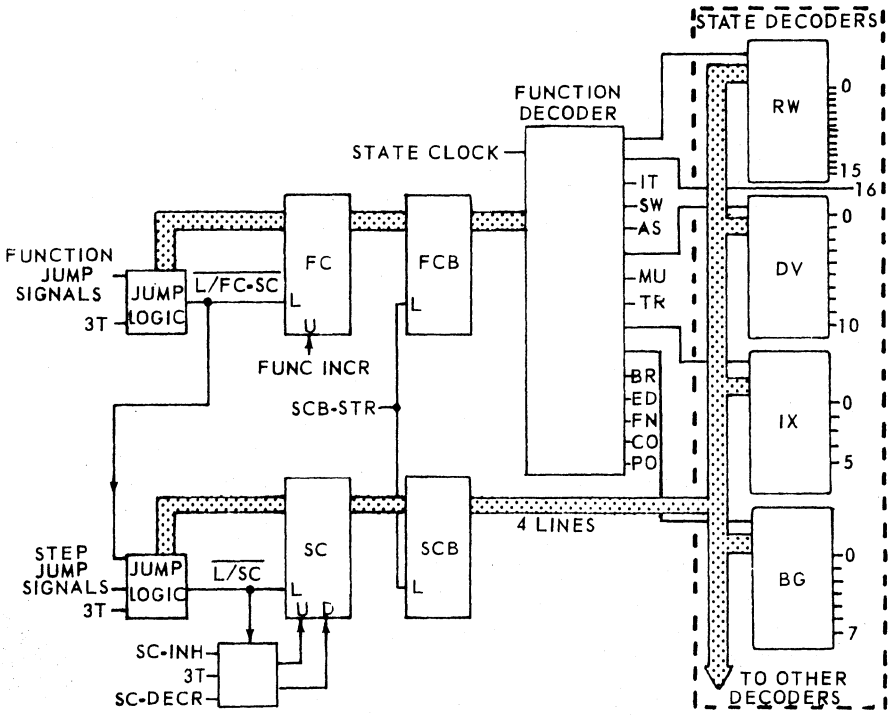
3-1.1 TIMING AND SEQUENCING

Basic timing for the ACU is derived from a 9mHz oscillator that is located on the TMN card. From this, and other qualifying logic, comes the State Clocks, Function Clocks, and a series of sub-divided timing signals that sequence the various logic operations.

The figure below shows some of the more significant timing signals in the ACU. One of the major timing sources is the State Clock, refered to as State. A State only exists during the time that the State Clock signal is active. Between states, there is a "dead" time when no state exists. A normal state time is 777 ns, but the time is extended to 3.33 us for either a core cycle (in or out of memory) or for an FAC cycle.

The Functions and Steps are the main timing and qualification for the various operations that are required to complete an instruction. The Function and Step Code register contents can be changed during an active State Time, but the change will not be decoded and become effective until the next dead time between states.

The complete ACU requires and generates approximately 150 logic control signals. These signals are listed, along with a short definition, in the Reference section of this manual. Normal processing is directed by the State Decoders, that are fed by the Function and Step counters (and buffers). However, the Jump logic can cause direct entry into a specific function and step, and takes presedence over all other signals.

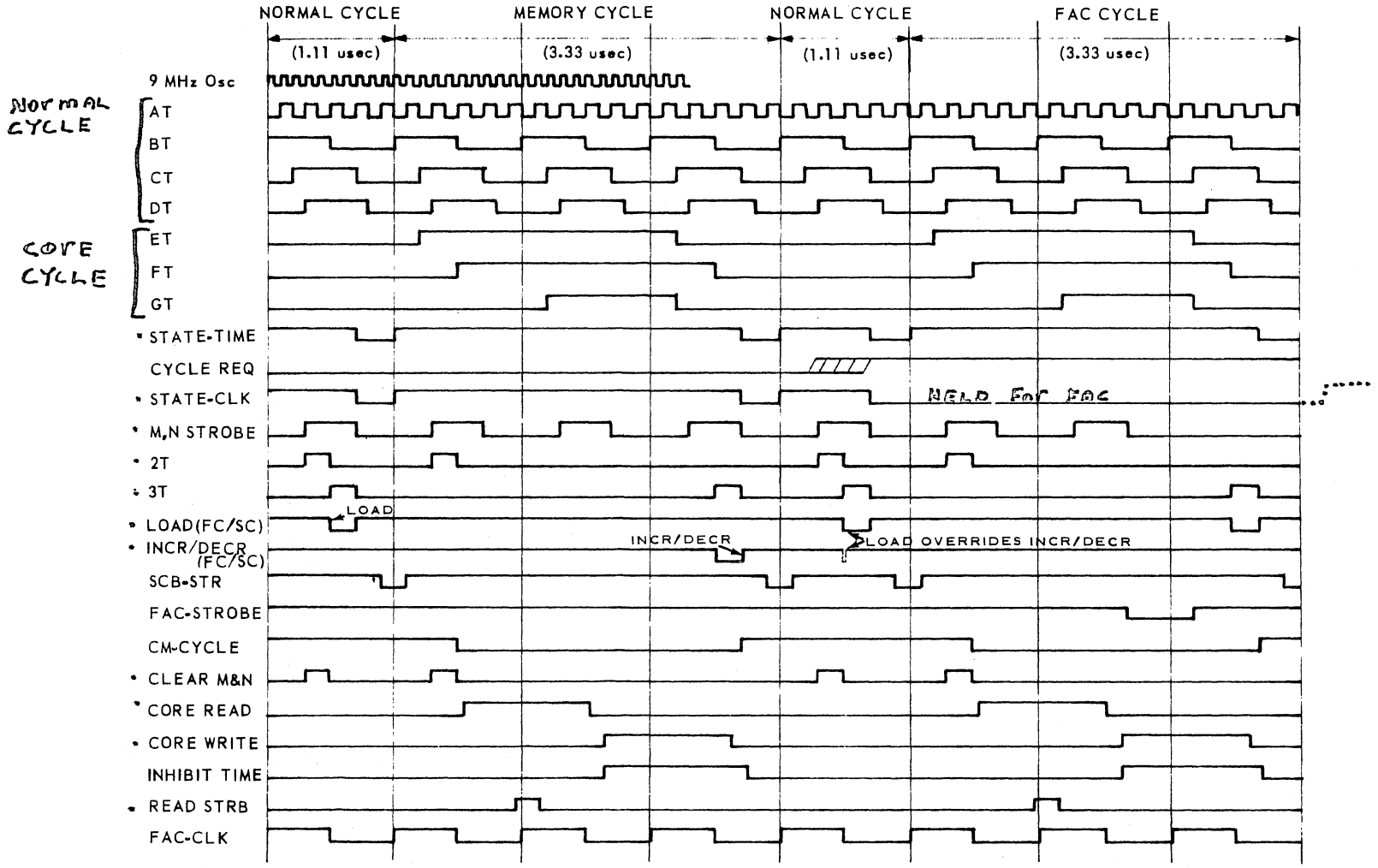


SIMPLIFIED BLOCK DIAGRAM OF BASIC CONTROL LOGIC

3-1.1 TIMING AND SEQUENCING (Continued)

As was mentioned before, the basic 9mHz oscillator frequency is modified by counters, flip-flops, and gates to arrive at the needed control timing. The figure below is a timing chart of some of the major timing signals within the ACU. The chart shows examples of a normal ACU cycle, a memory cycle, and an FAC cycle. The signal levels that are shown on the timing chart are given in a relative state, and do not necessarily show the +5v or 0v state of the signal.

Notice that the CYCLE-REQuest signal stops STATE CLOCK, suspending all "normal" ACU operation. It is during the "dead" time that is created by the STATE CLOCK



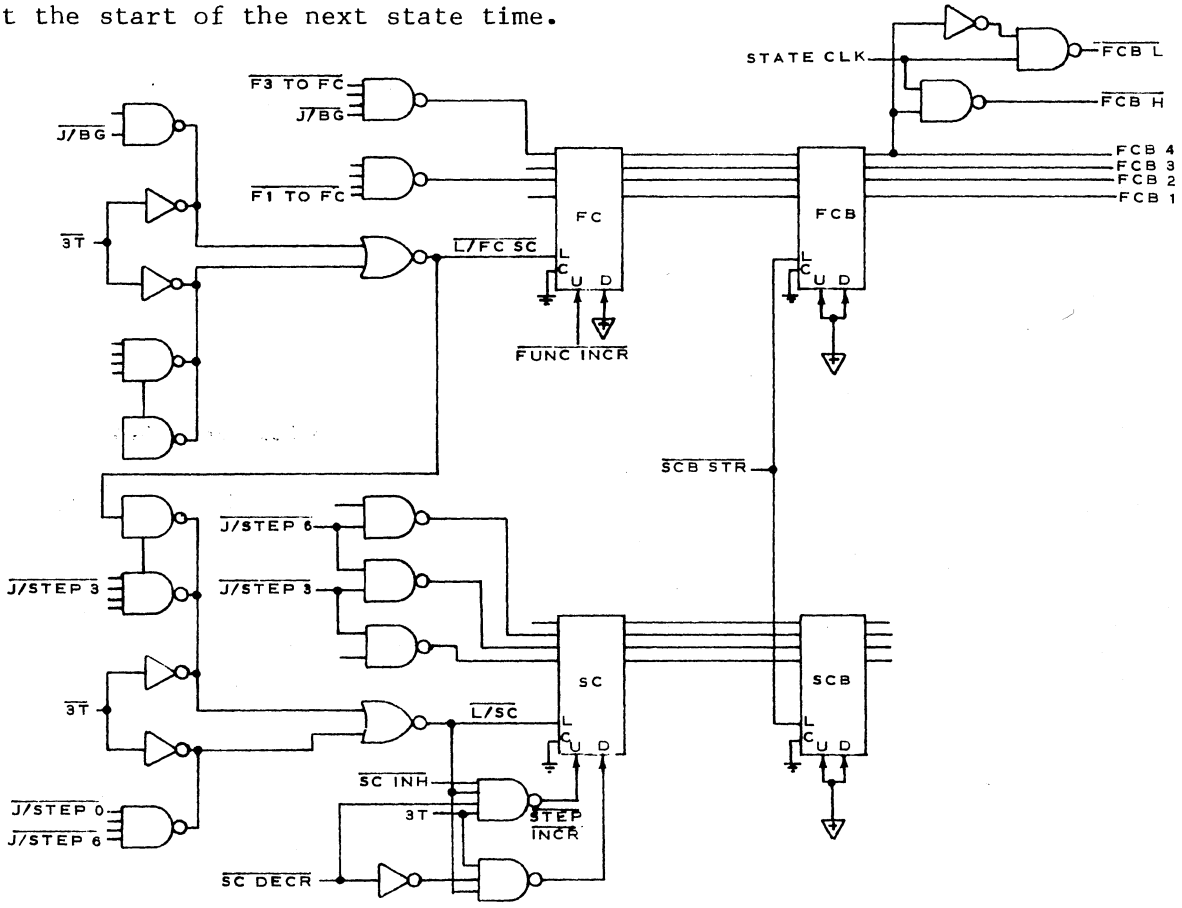
ACU BASIC TIMING SIGNALS

suspension that the FAC memory cycle is performed. The FAC memory cycle can occur between any of the steps of the INTERRUPT function, and involves a large number of logic decisions and steps. These steps and decisions are explained further in the later paragraphs covering INTERRUPT and READ/WRITE, FAC.

3-1.1 TIMING AND SEQUENCING (Continued)

FUNCTION AND STEP COUNTERS

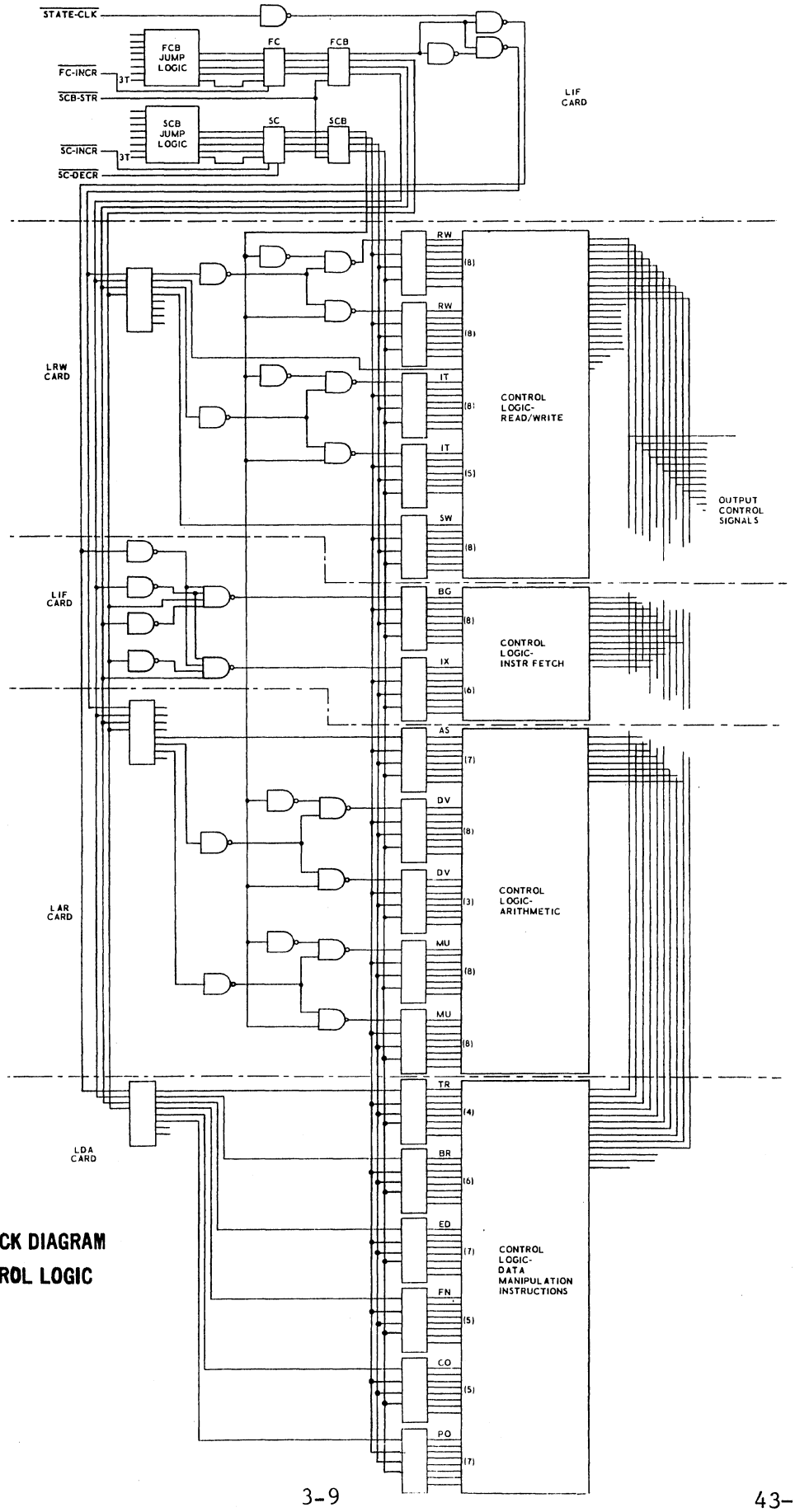
The Function Counter and Function Count Buffer, in conjunction with the State Decoders, provide the states, or steps, within each function. The number of decoded steps within each function is unique to that function, but may coincidentally contain the same number of steps as some other function. Each function has a seperate State Decoder, and because of the great number of steps that are required in READ/WRITE, INTERRUPT, MULTIPLY, and DIVIDE, two decoders are provided for each of these functions. The figure below shows the major portions of the function and step logic. A change in function or step can be developed during an active state time, but the change will not be loaded into the buffers until the SCB-STR signal is given at the start of the next state time.



SIMPLIFIED LOGIC DIAGRAM OF CONTROL LOGIC

When no increment, decrement, or jump signals are developed, the step counter will increment at the end of each state, unless an INHIBIT-SC signal is present to block the increment. An SC-DECR signal overides both the increment and the inhibit signals, and a jump (L/SC) takes presedence over all other signals.

The figure on the opposing page is a simplified block diagram of the ACU control logic. Notice that the functions that are to take place on a particular card are decoded on that card.



SIMPLIFIED BLOCK DIAGRAM OF ACU CONTROL LOGIC

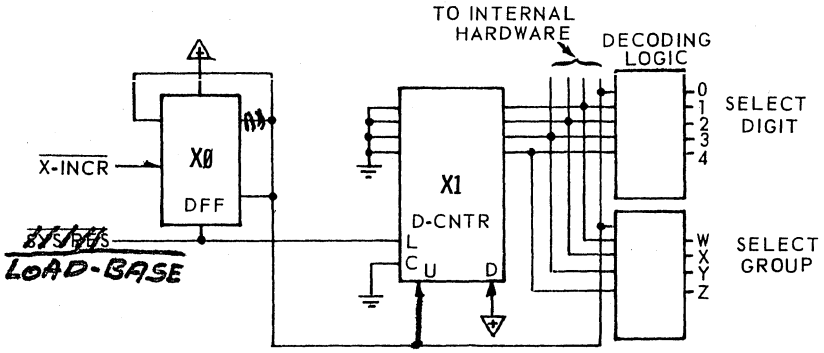
3-1.1 TIMING AND SEQUENCING (Continued)

X COUNTER

The X COUNTER is a twenty state binary counter that is located on the RBA card. It always counts in an ascending progression, starting again at zero when a count of 19 is reached. The decoded number that is in the x counter represents the partition that is being addressed by the ACU.

The binary output of the x counter is decoded into select digit (SEL-DIGIT) and select group (SEL-GROUP) signals that are used to address a particular IOC (partition). The figure on the opposing page shows the addressing scheme that is used to select only one IOC at a time. The illustration is for a Model 21 with the full 20 partitions, but the scheme applies to the 6800 and the 101 models as well.

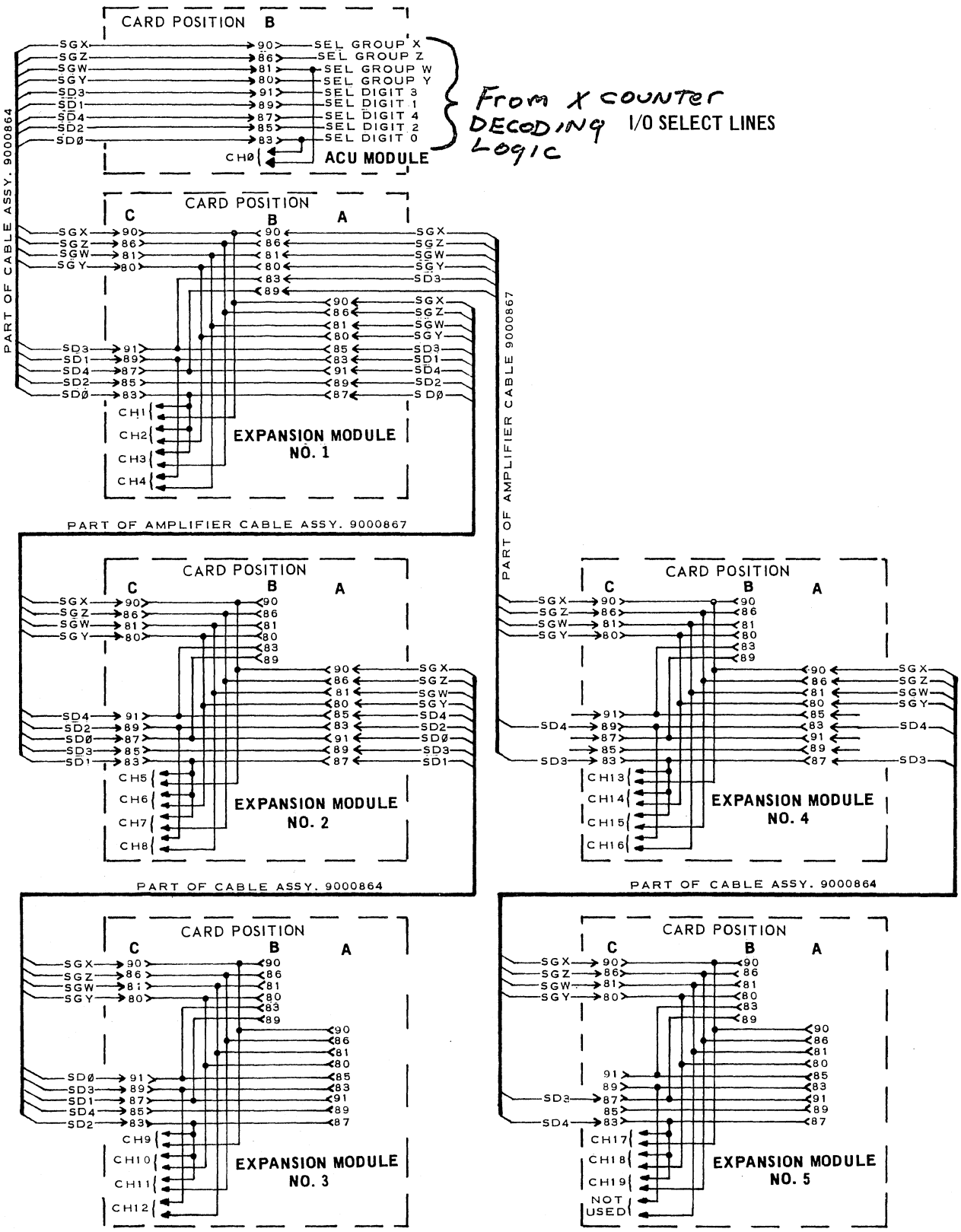
The x counter is also used by the ACU to address the common area of memory. The X1 output directly addresses the 10s digit of the protected address, and the XØ output qualifies with the Q counter to address the unit digit of the address. The figure and table below show the X Counter (simplified) and the counts that are used for partition selection and protected memory addressing.



IOC ADDRESSING			X COUNTER				
			X1				XØ
PARTITION	SEL-DIGIT	SEL-GROUP	8	4	2	1	
0	0	W	0	0	0	0	0
1	0	X	0	0	0	0	1
2	0	Y	0	0	0	1	0
3	0	Z	0	0	0	1	1
4	1	W	0	0	1	0	0
5	1	X	0	0	1	0	1
6	1	Y	0	0	1	1	0
7	1	Z	0	0	1	1	1
8	2	W	0	1	0	0	0
9	2	X	0	1	0	0	1
10	2	Y	0	1	0	1	0
11	2	Z	0	1	0	1	1
12	3	W	0	1	1	0	0
13	3	X	0	1	1	0	1
14	3	Y	0	1	1	1	0
15	3	Z	0	1	1	1	1
16	4	W	1	0	0	0	0
17	4	X	1	0	0	0	1
18	4	Y	1	0	0	1	0
19	4	Z	1	0	0	1	1

PROTECTED MEMORY ADDRESS					
10s Digit	Units Digit				
0	0	1	2	3	4
0	5	6	7	8	9
1	0	1	2	3	4
1	5	6	7	8	9
2	0	1	2	3	4
2	5	6	7	8	9
3	0	1	2	3	4
3	5	6	7	8	9
4	0	1	2	3	4
4	5	6	7	8	9
5	0	1	2	3	4
5	5	6	7	8	9
6	0	1	2	3	4
6	5	6	7	8	9
7	0	1	2	3	4
7	5	6	7	8	9
8	0	1	2	3	4
8	5	6	7	8	9
9	0	1	2	3	4
9	5	6	7	8	9
	0	1	2	3	4
	Q COUNT				

X COUNTER


CARD POSITION B
SGX 90 SEL GROUP X
SGZ 86 SEL GROUP Z
SGW 81 SEL GROUP W
SGY 80 SEL GROUP Y
SD3 91 SEL DIGIT 3
SD1 89 SEL DIGIT 1
SD4 87 SEL DIGIT 4
SD2 85 SEL DIGIT 2
SDØ 83 SEL DIGIT 0
CHØ
ACU MODULE
From X counter DECODING Logic
I/O SELECT LINES
PART OF CABLE ASSY. 9000864
CARD POSITION C B A
EXPANSION MODULE NO. 1
CH1
CH2
CH3
CH4
PART OF AMPLIFIER CABLE ASSY. 9000867
PART OF AMPLIFIER CABLE 9000867
EXPANSION MODULE NO. 2
CH5
CH6
CH7
CH8
EXPANSION MODULE NO. 4
CH13
CH14
CH15
CH16
PART OF CABLE ASSY. 9000864
EXPANSION MODULE NO. 3
CH9
CH10
CH11
CH12
EXPANSION MODULE NO. 5
CH17
CH18
CH19
NOT USED

3-1.1 TIMING AND SEQUENCING

X COUNTER (Continued)

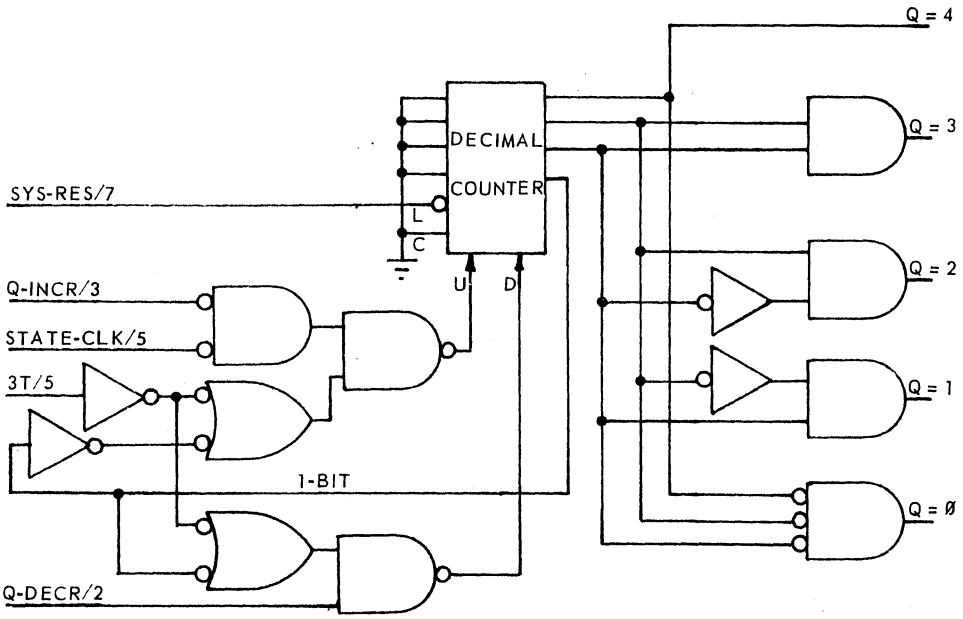
The x counter must be at zero for the SET MODE instruction to be performed. This limits the SET MODE instruction to partition zero (in the ACU module).

In BEGIN Ø, the ACU tests for INTerrupts. If the INTerrupt flip-flop is set, the ACU must leave for a short time to service the request, or requests. As the ACU leaves BEGIN, the D and H counters are cleared, and incremented along with the x counter. When the interrupts are serviced, the D and H counters are at an unknown value. To find the partition that was active before the interrupt, H (and X) is incremented until the value of 20 is reached (D2). The x counter is now setting at the partition that was left for the INTerrupt.

Q COUNTER

The Q counter is a five-state (quinary) counter on the RAD card. It is a special arrangement of a D-counter and decoding gates. The Q counter is used to address the unit digits of the index register locations in partition memory (also the location 40 register), and to address protected memory (qualified with the x counter). The Q counter is also used for stepping through 4 or 5 part operations of hardware sequences.

The Q counter (simplified) is shown below. The Q counter is loaded with zero value by the SYS-RES/7 signal at the start of processor operation or whenever the



Up = Q-INCR • STATE-CLK • ($\overline{3T}$ + 1-BIT)
Down = (3T+ $\overline{1\text{-BIT}}$) • Q-DECR

Both up and down inputs are normally a logic 1. When the conditions are met, the U or D input changes momentarily to a logic 9. The counter is incremented or decremented by the trailing edge of the U or D pulse.

3-1.1 TIMING AND SEQUENCING

Q COUNTER (Continued)

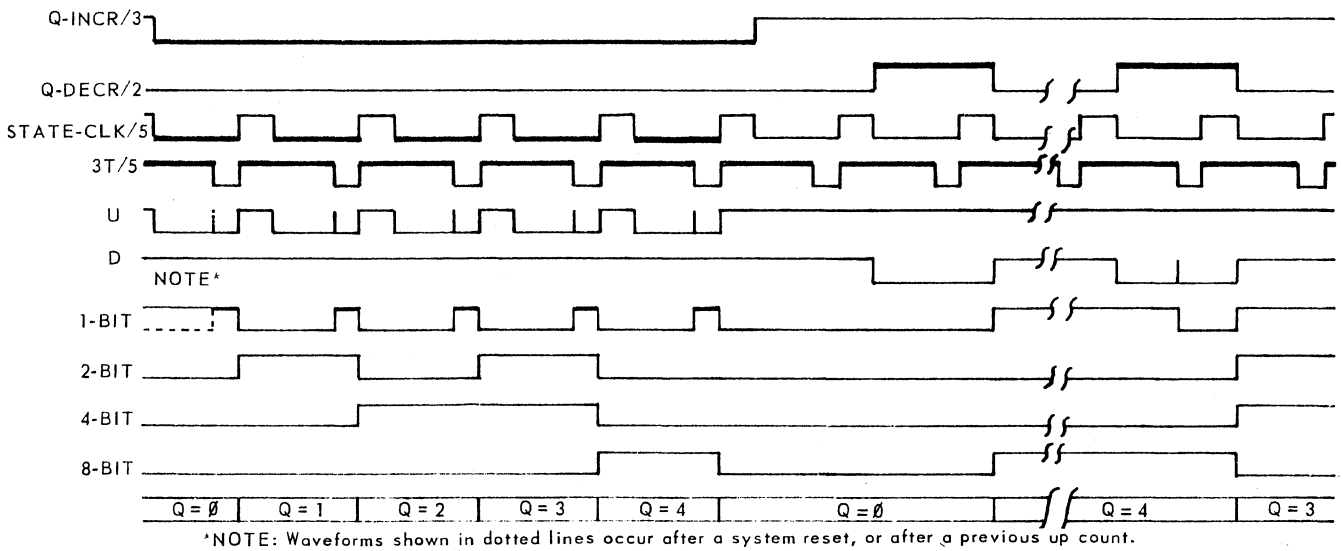
logic is reset by that signal. All other Q counter activity comes from the inputs to the Up and Down count logic. The U and D inputs to the D-counter are normally at a logic 1 (+ v). In order to increment or decrement the counter, the input must be qualified to a logic 0, then allowed to return to logic 1. The actual count is made when the input returns to the logic 1 state. Because of the feedback and decoding configuration, it takes two counts into the D-counter to move the Q count up or down one number when the counting direction is reversed. The inset shows counts that can be contained in the D-counter for the various Q counts. The Q counter is made to count up (Q-INCR) in BEGIN (BG), BRANCH (BR), INTERRUPT (IT), POSITIONING (PO), READ/WRITE (RW), and SWITCH (SW), but is only made to count down (Q-DECR) in INDEX (IX).

Q COUNTER TRUTH TABLE

DCTR BINARY VALUE								Q COUNT
INCREMENT				DECREMENT				
8	4	2	1	8	4	2	1	
0	0	0	0					Ø
				0	0	0	1	
1	0	0	0					4
				1	0	0	1	
0	1	1	0					3
				0	1	1	1	
0	1	0	0					2
				0	1	0	1	
0	0	1	0					1
				0	0	1	1	
BCD COUNT			IGNORED	BCD COUNT			IGNORED	

Timing for the Q counter is shown in the illustration below. Notice that the Q-INCR/3 input can remain at logic 0 while the counter is incremented through all five counts. However, the Q-DECR/2 input must switch to a logic 1 for each down count. Then, when the Q-DECR/2 signal goes low again, the D input to the decimal counter is returned to logic 1 for the increment.

When Q-INCR/3 and STATE-CLK/5 are both active (both low), either the presence of a 1-bit from the D-counter, or the absence of the 3T/5 signal will cause a logic 0 at the U input to the counter. If the last input to the counter was a down count, the 1-bit will have an output, and the 3T/5 signal must be removed twice to increment the Q count; if the last input to the counter was an up count, the first time that the 3T/5 signal is removed, the Q count will increment.



*NOTE: Waveforms shown in dotted lines occur after a system reset, or after a previous up count.

Q COUNTER TIMING DIAGRAM

3-2.0 MEMORY ADDRESSING

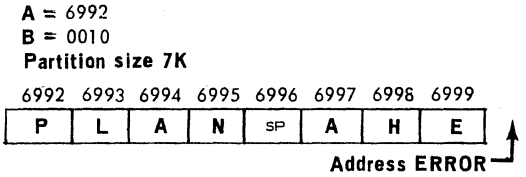
Addressing within each partition is relative to the beginning of that partition. The A and B addresses that are used by the programmer are placed into the A, B, and P registers and provide the majority of relative addressing. The Q counter and the IA and IB registers provide the relative addresses for the active index registers. The location 40 register (essentially an error register) is derived from a combination of the Q counter and the x counter. The 1, 10, and 100 digits of a relative address is given to the memory matrix in a twelve-wire BCD form. The 1000 digit is added to the base address by the Base Adder (as an internal operation of the ACU) to arrive at the actual location in memory, called the absolute address.

In the extended Common area addressing of the models 21, 6800, and 101, the 10K digit is decoded from the base adder by logic on the RDX card, and passed directly to the memory select system (R-BUS-K).

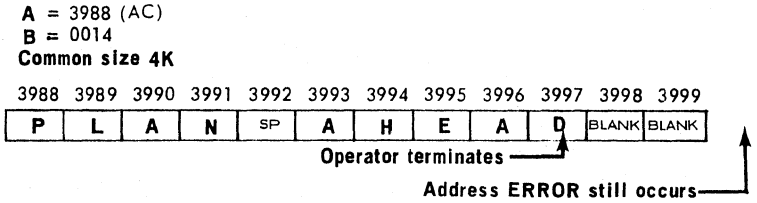
3-2.1 ADDRESS ERROR

An address error occurs because the instruction expects the ACU to address a position in memory that is greater than the allotted partition (or common) size. In the case of a 10K (exactly) partition, an overrun at address 9999 causes the next character to be entered at address 0000. This makes it impossible for a 10K partition to have an address error within the partition. However, when a 10K partition is working in the common area of memory, an address error can be made in the same way as any other partition.

A simplified example of an address error is shown below. The instruction is asking to read (enter into memory) ten characters, starting at a relative partition address of 6992. However, the partition is only patched for 7K, allowing only eight characters to be entered. When an attempt to enter the ninth character is made, an address error occurs.



In the next example, ample space was allowed for the intended message, but too much spillover room was specified. The intended message was entered into memory, but an address error occured because the instruction must complete the specified number of characters.



An address error can be made with no characters entering memory if an address is specified that is greater than the partition or common size. The relative address is checked against partition (or common) size and the base address before each memory cycle, and if the address is too large, the cycle does not take place. The limit circuitry is located on the RBA/RBX card.

3-2.2 RELATIVE ADDRESSING

All addresses within a partition are relative to the beginning point for that partition. The base adder converts the relative address to a true, or absolute, address by adding the size (total) of common memory, and the patched sizes of all lower numbered partitions to the relative address. For example, if a relative (instruction) address of 2304 is given in partition 4, and the lower partitions are patched for 2K, 5K, and 3K, with a common of 2K, the absolute address is 14,304. The absolute address is the position that the ACU must find for the memory transaction.

Knowledge of the true address can be an aid in troubleshooting and isolating a memory problem.

3-2.3 COMMON ADDRESSING

Common area addressing does not use the Base Adder, and the R-BUS-COM/3 signal that is generated by a common area address forces a logic zero into the Base Adder. With the base adder inhibited, the thousands digit of the specified address becomes the thousands digit that is applied to the memory select circuits. This digit is also compared to the common area limit (which has been gated onto the R-BUS for the comparason), and if the thousands digit is greater than the common area limit, an error condition is set.

If the common area address is less than 300 (indicating that it is within the protected area) the function code is checked. Any READ instruction with an address less than 300 must also be accompanied by the inhibit switch condition (either from the test panel, or through the SET MODE instruction) or an address error will be set by gates on the TMN card. These checks make it impossible to enter characters into protected memory except through inhibit switch.

Any address error condition causes the ACU to preset CHECK, and decrement P1 (marking the partition inactive), and the character transfer that is in progress is terminated.

3-2.4 BASE ADDER

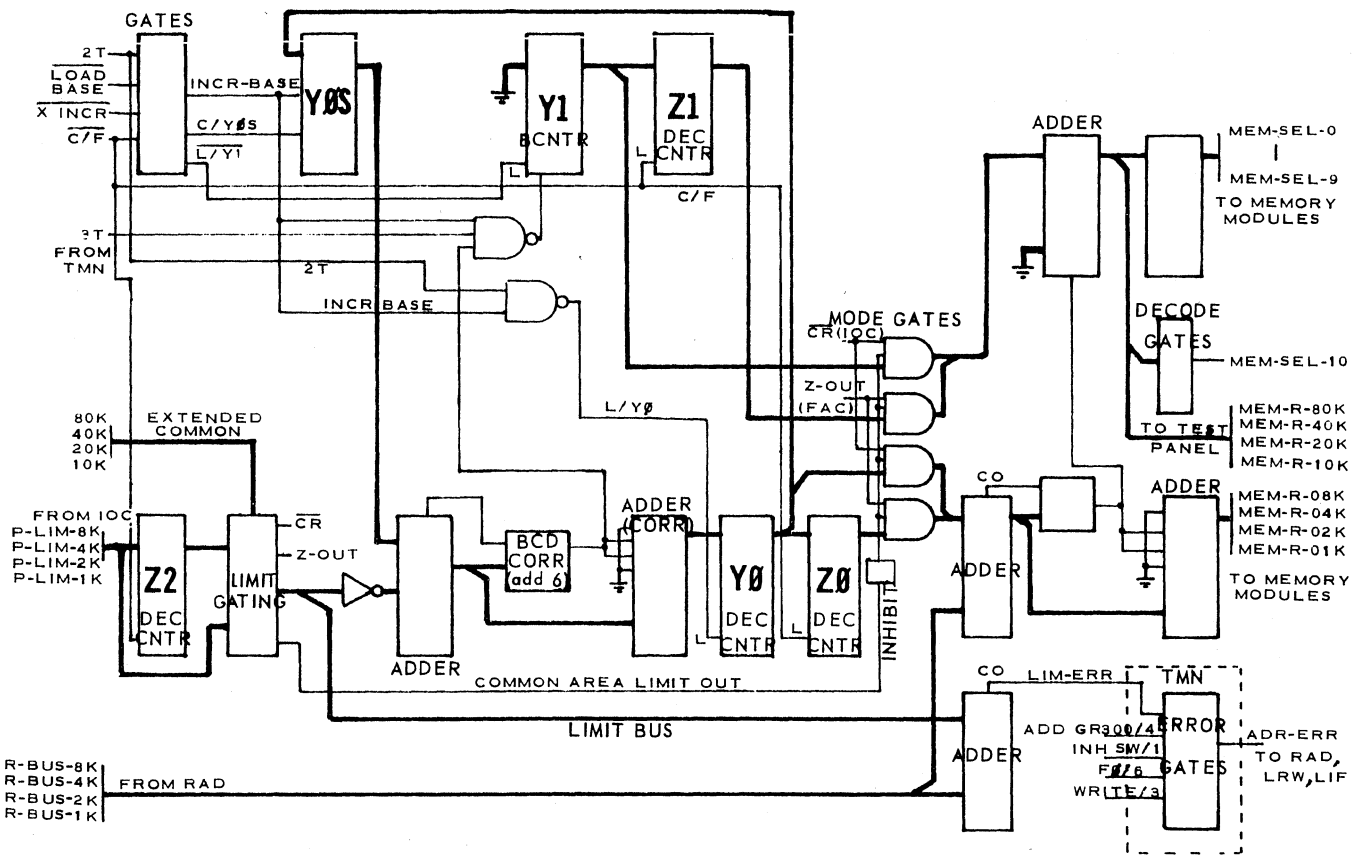
The base adder adds the patched size of the common area, and the size of all lower numbered partitions to arrive at the base address of the working partition. The base address of the partition is added to the relative (instruction) address when a character is to be located in memory. The upper limit of the common area, and consequently the base address of partition zero, is determined by the patches on the RBA card. The base address of succeeding partitions is determined by the patches on the IOC cards of all lower numbered partitions.

As the ACU steps from one partition to the next, the base adder establishes the new partition's base address (the 0000 relative address location). Normally when the ACU is working in a partition the base address is stored in the Y and Z registers. During an FAC cycle, the ACU will answer INTerrupt requests by other partitions until the FAC device is actually ready to transfer characters. The

3-2.4 BASE ADDER (Continued)

working partition address (the one in which the FAC cycle is to take place) is retained in the Z register while the Y register is incremented to find INTerrups. When the FAC device is ready for a character transfer, the CYCLE-REQuest signal is raised, causing the ACU to suspend all other operations (at the end of the active step) and perform the FAC cycle during the "dead" time between states. This process is nearly instantaneous, requiring an immediate base address for the (FAC) working partition, which is available from the Z register. When the FAC cycle is complete (in a disc operation, CYCLE-REQuest is held until all 100 characters are transfered) the CYCLE-REQ signal is dropped, allowing STATE CLOCK to become active, and the ACU proceeds to the next step of INTerrupt as if the cycle request had never existed (useing the Y register for the base address of the interrupting partition).

The choice of which register the base address should come from is determined by the mode gates (see the illustration below) that are triggered by either an IOC or an FAC operation.



BLOCK DIAGRAM BASE ADDER

3-3.0 LOGIC OPERATION

The ACU performs all major functions by entering hardware routines that are controlled by function codes. These function codes are placed into the F register, and at the proper time, strobed into the function code buffer. The hardware generates some functions as a normal part of power up, power down (or power fail), and partition switching (time sharing). As an example, the power up point is in the SWitch function, and under normal conditions, the ACU jumps to BEGIN to pull the software instruction from memory. Once the instruction is pulled, and placed into the proper registers, the future course of action is determined by the function code that is part of the instruction.

Even though the general course of action is set by the instruction word function code, the ACU must step through many states and jump functions many times to perform the various checks and duties that are necessary to complete an instruction. The sequence of steps and functions is different for each software instruction, and is modified or cancelled if certain conditions, such as a data error, an inactive peripheral, or a busy disc drive are found.

The table shown below is a listing of both the hardware generated (internal) functions and the software (instruction) functions.

INSTRUCTION	FUNCTION	F REGISTER				MNEMONIC
		F3	F2	F1	F0	
		FCB				
		8	4	2	1	
READ	READ/WRITE	0	0	0	0	RW
WRITE	READ/WRITE	0	0	0	1	RW
(not used)	INTERRUPT	0	0	1	0	IT
MOVE ADDRESS	SWITCH	0	0	1	1	SW
ADD	ADD/SUB	0	1	0	0	AS
DIVIDE	DIVIDE	0	1	0	1	DV
MULTIPLY	MULTIPLY	0	1	1	0	MU
SUBTRACT	(not used)	0	1	1	1	
MOVE CHARACTER	TRANSFER	1	0	0	0	TR
MOVE NUMERIC	INDEX	1	0	0	1	IX
SET MODE	BEGIN	1	0	1	0	BG
BRANCH	BRANCH	1	0	1	1	BR
EDIT	EDIT	1	1	0	0	ED
FORM NUM FIELD	FORM NUM FLD	1	1	0	1	FN
COMPARE	COMPARE	1	1	1	0	CO
EXCHANGE	POSITION	1	1	1	1	PO

During an input/output operation (READ/WRITE) the ACU sets up the necessary conditions within the IOC by presenting it with a Select Character that contains most or all of the information that is needed by the IOC. A similar FAC character is given to the controllers within the FAC module if the READ/WRITE is to or from an FAC device. In the case of the IOC, the partition is switched, and the relatively slower IOC is allowed to make the preparations for character transfers. When the IOC is ready to transfer a character, it raises an INTerrupt signal to the ACU. An IOC that is in the process of completing an operation is marked IO BUSY, by a flip-flop that was set by the ACU when the Select Character was presented. When the ACU first switches to service a new partition, and again before each new instruction is pulled, the ACU will answer any requests for a character transfer by detecting the INTERRUPT signal, and switching partitions until the INT-REQ signal is found. When the interrupt requests are satisfied, The ACU then checks for failing power and if the IOC is busy, and will not pull an instruction in the partition if either of

3-3.0 LOGIC OPERATION (Continued)

these conditions are present. If the IOC is busy, the ACU switches to the next partition and begins by checking for INTerrups again; if the power is failing the function code is also changed to SWITCH, but a routine is initiated to store the the P count, etc. from the active partition into the protected area of memory.

A summary flow chart of the ACU actions is located as the last page (foldout) of this section. Portions of that chart are shown with individual function explanations.

3-3.1 READ CONTROL (LOAD REQUEST)

Load request is a READ instruction that has certain CONTROLs and conditions for placing the ten character software instruction "bootstrap" into the memory core. The load condition can be called for by an IOC (although some IOCs cannot load program), or it can, and will, be forced by the ACU if a CHECK condition (instruction error) is detected. The only difference between the two situations (as far as ACU operation is concerned) is that when the CHECK condition is present, the ACU performs some extra steps before the LOAD-REQuest operation. These steps, and the LOAD-REQeust operation are described in the following text, along with the various states that are excerpted from the Algorithms to show the logic action. The complete state is sometimes not shown, only the action that is refered to in the text.

In BEGIN 3 and 4, the ACU pulls the ten character instruction from the address that is specified by the P count. If the lower four bits of any of the characters is greater than a binary nine, the ACU sets CHECK. The Model 20 (only) makes an additional check for a 5-bit (N1); the combination of these two checks in the Model 20 is called a DATA FAULT.

BEGIN		3	Fetch Characters Ø-4 of Instruction	P-OUT
				READ
				L/F (3T)
				L/A
				L/B (3T)
				Q-INCR
				P-INCR
				
				If $\overline{(Q=4)}$: SC-INH
				If M > 9·3T: P/$\overline{CHECK}$
				If (Q=4)·$\overline{M > 9}$·$\overline{CHECK}$·
				E1·(BR-OK):J/BRANCH
				If (Q=4):INST-STOP(3T)
				
				If Q=Ø: L/E1
				If Q=4·$\overline{E1}$·$\overline{CHECK}$: C/ID
				J/TRANSFER
				J/STEP 5
					Q=Ø : L/E1
					
					(Q=Ø).Load F:
					Load LA,J,LB,F3
					
					Q=1: Load A3,B3,F2
					
					Q=2: Load A2,B2,F1
					
					Q=3: Load A1,B1,FØ
					
					Q=4: Load AØ,BØ
					AC,BC
					A5 B5
					$\overline{E1}$=Indirect Addressing
						TR 5
						BR Ø

	TR 7	4	Fetch Characters 5-9 of Instruction	P-OUT
				READ
				L/I
				L/B (3T)
				Q-INCR
				P-INCR
				
				If $\overline{(Q=4)}$: SC-INH
				If M > 9·3T: P/$\overline{CHECK}$
				If (Q=4)·$\overline{M > 9}$·$\overline{CHECK}$·
				E1·(BR-OK):J/BRANCH
				If (Q=4): INST-STOP(3T)
					(Q=Ø).Load I:
					Load LB,K,IA1
					
					Q=1: Load B3,IAØ
					
					Q=2: Load B2,IB1
					
					Q=3: Load B1,IBØ
					
					Q=4: Load BØ,BC,B5	

3-3.1 READ CONTROL (LOAD REQUEST)

A test of the instruction that was just pulled is made for INDEXing. If the instruction contains indexing bits, the indexing operation will be performed, even though the CHECK may be set. In any case, the ACU steps to, or returns to BEGIN 6, where a check is made for invalid instructions. Either condition causes a jump to

BEGIN	IX 3	6	Jumps for Arith. Op. or Invalid Opcodes or Exchange or Indirect Address	C/CONDS C/DH If $(F2.\overline{F1}.\overline{F\emptyset}+\overline{F3}.F2).CHECK$: J/Positioning INST-STOP (3T) If $(\overline{F2}.F1.\overline{F\emptyset}+CHECK)$: J/BEGIN P/CHECK If $(F3.F1.F\emptyset+\overline{F2}.F1.F\emptyset)$: J/Transfer	C/CONDS: Clear MINUS Clear SUBTRACT Preset ZERO C/DH: Clear H Clear D NOTE: CARRY follows SUBTRACT Arith. Op: 4,5,6,7 or 13(FN) Invalid Op: 2, (10) Address Transfer : 3 Exchange: 15	PO Ø BG Ø TR Ø

BEGIN Ø where INTerrupts will be detected and answered, then on to BEGIN 1 for power failure and IO BUSY checks. Assuming that the power is not failing, the logic steps to BG 2. A load request is not detected in BEGIN 2, because the LOAD-REQ flip-flop is not yet set. However, the CHECK condition is discovered by the ACU, causing a jump to SWITCH Ø.

BEGIN		2	Test for Load Request	ØØØ1-TO-M If ACU-LD-REQ: C/P P/F3 J/Read, Write If CHECK.$\overline{\text{ACU-LD-REQ}}$: J/SWITCH	C/P: Clear P Clear A Clear J Clear LA Clear B3,B2,BØ Clear Conditions Load B1 L/K L/LB	RW Ø SW Ø

The ACU begins to "close out" the operation within the active partition by placing the program (P) count on the S bus (where it would normally be sent to protected memory), and marking the partition inactive.

· ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
SWITCH BG 1 BG 2 BR 5 RW 9 RW 1Ø RW 11 RW 12 RW 16 Step 1	Ø	Transfer P to M,N	CONDS-TO-S R-TO-S If (Q=Ø): P-LIM-TO-S P-INCR 01-TO-N	CONDS-TO-S: P-OUT $(R\text{-}TO\text{-}S)(\overline{Q=\emptyset})$: L/N Q=Ø: P-LIM Q=1: P3, Carry Q=2: P2, Minus Q=3: P1, ZERO Q=4: PØ, PC (PØ=1) = Partition Inactive	

3-3.1 READ CONTROL (Continued)

In SWITCH 1, the X counter is normally used to address the protected area of core to store the P count. But when CHECK is set, the 40 address is brought out, and will be used when the P count (the address where the error was made) and the status conditions will be loaded. Meanwhile, the CHECK condition has kept the partition from being incremented (in SW 4). When the loading is complete (SW 6) the ACU steps to SW 7, presets LD-REQ (in the IOC), and jumps to BEGIN. When the P/LD-REQ signal is given to the IOC, the CHECK condition is cleared in the IOC. The CHECK and LD-REQ flip-flops reside in the IOC, but can be considered as a part of the ACU operation, that is unique to the partition.

SWITCH →		1	Store P in Core	WRITE Q-INCR If $\overline{\text{CHECK}}$: X-OUT If CHECK: 40-OUT If $(\overline{Q=4})$: SC-DECR	X-OUT or 40-OUT gives Q-OUT (P5 in zone bits)	Step 0
	START	2	Detect Power Failure	If PWR-FAIL: SC-INH	Upon detection of power failure, the ACU is held in this state.	
SWITCH →	Step 5	4	Increment Partition Number	C/TIMEOUT C/Disc Access-FF If $\overline{\text{INH-SW}}.\overline{\text{CHECK}}$: X-INCR	C/TIMEOUT: Clear F, Clear IA,IB, Load Z	
SWITCH →	IT 8	6	Load P & Conditions	X-OUT READ L/P L/CONDS Q-INCR C/FAC-DONE If (Q=4): C/M If $(\overline{Q=4})$: SC-INH	Q=0: -- Q=1: P3, Carry Q=2: P2, Minus Q=3: P1, Zero Q=4: P0,PC,P5 (P0=0) = Partition Active	
		7	Exit for normal Switching	J/BEGIN If CHECK: P/LD-REQ	P/LD-REQ resets CHECK in the IOC	

3-3.1 READ CONTROL (Continued)

From this point forward, the logic action is the same whether the LOAD request was brought on by a CHECK condition, or by operator control through an IOC peripheral. As the ACU passes through BEGIN Ø, any interrupt requests from other partitions will be serviced. The power fail check is made in BG 1, and providing the power is not failing, the ACU steps to BG 2 where the test is made for load request. The load

BEGIN		2	Test for Load Request	ØØØ1-TO-M If ACU-LD-REQ: C/P P/F3 J/Read, Write If CHECK.$\overline{\text{ACU-LD-REQ}}$: J/SWITCH	C/P: Clear P Clear A Clear J Clear LA Clear B3,B2,BØ Clear Conditions Load B1 L/K L/LB	 RW Ø SW Ø

request that was just set is detected. This causes the ACU registers to set up for a READ instruction of ten characters from IOC device zero. Preparation is made for this in BG 2 by clearing P so that the next instruction will be pulled from location ØØØØ (in partition memory). The M register is always loaded with ØØØ1 in BG 2, but is only used when there is a load request, as in this case, to load the necessary other registers for the READ CONTROL action. The K and LB registers are loaded with a 1, and the F register is loaded with 1ØØØ developing the I/O Select character that will be used later. The F register is used in this case to show that a LOAD is in progress. When all of this is done, the ACU jumps to R/W Ø, and on to R/W 1.

READ/WRITE		1	Recall (B4) Check for Active Bits	X-OUT 1ØØ-OUT READ B-DECR If ($\overline{\text{M4}}$.$\overline{\text{M2}}$) + (F3.M4): J/STEP 4	F3 = Load in Progress M2.$\overline{\text{M4}}$ = Load Active M4 = I/O Active	 Step 4

In R/W 1, the B4 character indicates that the partition is not active with an I/O operation, causing a jump into step 4 (still in READ/WRITE). In R/W 4 the IOC Sel-

	ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
READ/WRITE	Step 1	4	Send Device Number & Command to IOC	J-TO-S IOF-TO-S LOAD-IOS (3T) Q-INCR	J-TO-S Device # IOF-TO-S: If $\overline{\text{F3 + LB2}}$: 1 to N2 If FØ : 1 to N1	

ect character is developed, and sent to the IOC. The contents of the J register (that in this case was cleared in BG 2) is brought to the S bus and sent as the device number portion of the select character. The F3 bit indicates that a load is in progress, causing the 7-bit of the select character to be a 1 (IOF-TO-S).

If the partition is an MTIOC (the most common IOC that would be loading program) the Select Character is sent on to the Line Unit, causing some appropriate action in the peripheral device.

3-3.1 READ CONTROL (Continued)

Once the Select character has been given to the IOC, the ACU stores the contents of the A register (A was cleared in BG 2) into protected memory (in R/W 5 and 6). In R/W 7 and 8, the contents of the B register are stored in protected memory, with the $\overline{M4}$•M2 bits indicating that an IOC LOAD is in progress. The ACU then sets the

READ/WRITE	Step 8	7	Transfer B to M,N	B-OUT R-TO-S If (Q=Ø): ACTVE-TO-S	R-TO-S.$\overline{Q=Ø}$: L/N ACTIVE-TO-S: If F3: 1 to M4 If LB3: 1 to M3 If F3 + LB2: 1 to M2 If FØ: 1 to M1	
		8	Store B	X-OUT 1ØØ-OUT WRITE Q-INCR If ($\overline{Q=4}$): SC-DECR If Q=Ø: 01-TO-N	Q=Ø: B4(Active Bits) Q=1: B3 Q=2: B2 Q=3: B1 Q=4: BØ,BC (B5 in zone bits)	Step 7

IO BUSY flip-flop in the IOC, and jumps to SWITCH, and prepares to go to another partition. The actual entry of the ten character instruction is then handled by the IOC through the interrupt process while the ACU is servicing other partitions.

READ/WRITE	9	IOC Exit	J/SWITCH If F3 + $\overline{\text{ACU-LD-REQ}}$: P/IO-BUSY If $\overline{\text{ADR-ERR}}$.$\overline{\text{CHECK}}$.3T: P1-DECR		SW Ø

In preparing to switch to another partition, the ACU stores the P count in the protected area of memory. The P count (because of the decrement) is 999Ø at this time. However, when it is stored in protected, the normal status bits are added to make the stored characters 99Y1. The P storage process is done in SW Ø and SW 1. When it is stored, the ACU switches to the next partition in the normal processing routine.

When the operator enters a character (from a peripheral device), the character is sent to the IOC and held ready for the ACU. In the IOC the INTerrupt flip-flop is set to inform the ACU that the character is ready. The INTerrupt is detected in BEGIN Ø, and the transfer is serviced by jumping to IT temporarily. In the MTIOC the transfer may not be an actual character if the operator has entered a unit seperator (US) code as the first character of the bootstrap. The US code is an operator option in the MTIOC that causes the INT flip-flop to be held, and zeros supplied to the ACU. With INT held, the ten-zero instruction will be entered into memory by ten successive interrupt cycles. At the end of each interrupt cycle, however, the ACU returns to BG before jumping back to IT (because the INT signal is still active). This procedure forces a complete circle through all partitions in the IT function.

The all zero instruction causes a READ from the disc (the next time the partition is serviced) at drive Ø, surface Ø, and sector ØØ. Normal software procedure will have a basic program at that address.

3-3.1 READ CONTROL (Continued)

When the ten character entry is complete, the IO BUSY flip-flop is reset. This is done in INTERRUPT as the ACU transfers the last character from the IOC. The ACU then continues to service all partitions in its normal sequence.

When the partition that just completed the ten character load is reached (in SW 6), the P hardware register is loaded from the number that is in the P protected area of memory. This number was 99Y1, but as it is pulled, the partition is marked active, making the number 99YØ. The ACU then jumps to BEGIN (from SW 7).

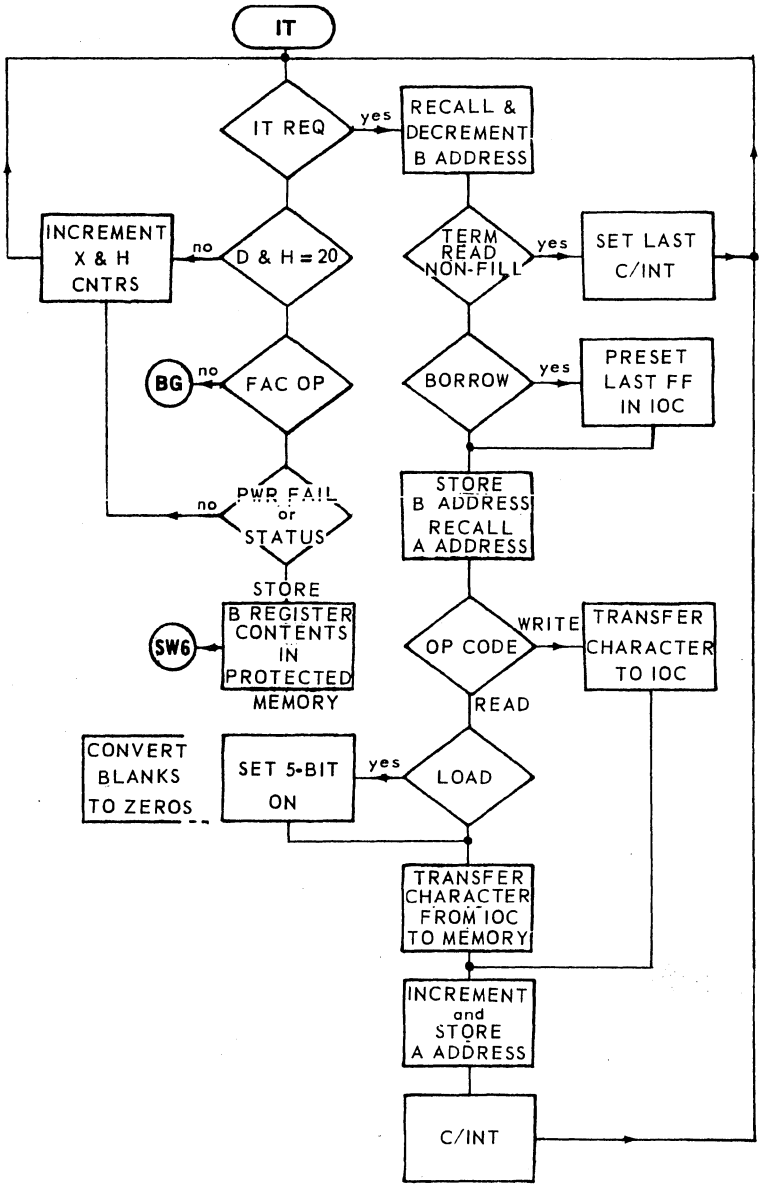
	ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
	Step 5	4	Increment Partition Number	C/TIMEOUT C/Disc Access-FF If $\overline{\text{INH-SW}}.\overline{\text{CHECK}}$: X-INCR	C/TIMEOUT: Clear F Clear IA,IB Load Z X-INCR: X-Incr H-Incr	
SWITCH		5		If $\overline{\text{IO-SEL}}$: SC-DECR		Step 4
	IT 8	6	Load P & Conditions	X-OUT READ L/P L/CONDS Q-INCR C/FAC-DONE If (Q=4): C/M If $\overline{(Q=4)}$: SC-INH	Q=Ø: -- Q=1: P3, Carry Q=2: P2, Minus Q=3: P1, Zero Q=4: PØ,PC,P5 (PØ=Ø) = Partition Active	
		7	Exit for normal Switching	J/BEGIN		

After making routine tests for INTerrupt (and servicing them if there are), power fail, and IO BUSY, the ACU discovers in BG 2 that the load request condition still exists. P is cleared again, F3 is set (the load in progress indication), and the ACU jumps to READ/WRITE.

		2	Test for Load Request	ØØØ1-TO-M If ACU-LD-REQ: C/P P/F3 J/Read, Write If CHECK.$\overline{\text{ACU-LD-REQ}}$: J/SWITCH	C/P: Clear P Clear A Clear J Clear LA Clear B3,B2,BØ Clear Conditions Load B1 L/K L/LB	 RW Ø SW Ø
BEGIN						

The B4 character is recalled in RW 1, and the ACU finds that the load has been completed, and status must be pulled (from the IOC). Status is pulled in RW 2, setting the proper condition flip-flops for the status that was reported.

If status is ERROR or FAULT, the operation must be repeated. If normal or FLAG status is reported, the ACU clears the I/O and LOAD active bits, and jumps to BEGIN. In BEGIN, the instruction that was just loaded is pulled and implimented.



LOGIC FLOW CHART

ACU INTERRUPT

3-4.0 HARDWARE FUNCTIONS

Hardware functions are the internal conditions that are set up by the ACU to perform a specific portion of an overall instruction. The basic sequences of SWITCH, BEGIN, and INTERRUPT are common to all instruction pulling and general "housekeeping". Within these functions, such items as failing power, ACU check condition, etc. are tested and acted upon if necessary. The Interrupt function is designed specifically to allow R/W instructions to be completed by I/O devices on a cycle stealing basis.

The following series of discussions present the hardware functions as seperate subjects. In ACU operation, the hardware functions are interdependant, and are only parts of the overall scheme. Many functions may be entered, and re-entered in the course of one instruction.

3-4.1 INTERRUPT

Interrupt is a function that is a specialized portion of the character transfer process. It is the only function in which characters can be given to or taken from external (IOC or FAC) devices. While there are modified uses of interrupt to get dialing digits or control characters from memory, the main and most common use of interrupt is transferring characters during a READ or WRITE operation. As is explained earlier, the READ/WRITE condition is established in the IOC, and the ACU does not pull instructions in that partition (because of IO BUSY) until the number of characters that was specified in the R/W instruction has been transfered. The character transfers are made one at a time, through the interrupt process.

The interrupt portion of the READ/WRITE process is entered only if the IOC indicates that a character is ready for transfer, or that the IOC is ready to receive a character from the ACU. The IOC or FAC cannot access memory directly, this is a function of the ACU. Portions of the FAC cycle confine the ACU to interrupt, even if there are no requests for character transfer.

During normal processing (in any partition) the ACU steps through BG Ø and discovers the INTerrupt signal if some IOC is requesting a character transfer. This is done just before an instruction is pulled from memory, whether it is the first instruction for the partition, or one of many in a sequence. The ACU will enter the interrupt function (shown on the opposing page) if the signal is detected.

Once in interrupt, the ACU will stay there until all partitions are checked for character transfer requests. This works as follows: The signal that causes a jump to interrupt from BG Ø, is the INTerrupt flip-flop being set. This indicates that one or more IOCs have a character transfer request. The ACU enters interrupt and addresses whatever partition is indicated by the X counter. If the partition that is addressed by the ACU has a request, the return signal INT-REQ is generated, and the ACU jumps to IT 5 and services the request. If there is no INT-REQ generated, the X counter is incremented (the D and H counters are also incremented at this time). The process continues, servicing all partitions in sequence, until the D and H counters reach 20, indicating that a full circle has been made. The ACU then jumps back to BEGIN.

One character is transfered for each requesting partition, each time the ACU enters INTerrupt. After the full interrupt circle is completed (D & H= 20), the ACU returns to BEGIN. If the INT signal is still active because of a "fill" type IOC operation, or because of a request that was raised after the counter had passed the partition but before reaching BG, the ACU will jump back into INTerrupt to service the transfer. Successive transfers by the same partition are prevented by the Partition Lockout flip-flop, forcing the ACU back to BG (where the PAR-LKOUT is cleared), and consequently allowing other partition interrupts between successive requests from the same partition. FAC transfers are made between states of the IT function, and do not follow the rules explained above.

3-4.2 READ/WRITE

The READ/WRITE process is accomplished either through an Input/Output Channel (IOC), or through the File Access Channel (FAC). In either case, the entire process is handled through the ACU for character transfers to and from memory. Because the IOC and FAC are quite different in many respects, the two discussions are given seperately. Each presentation gives general interface characteristics, but it should be noted that individual device design can modify specific actions. Unique characteristics of devices are given in sections of this book that describe the device.

IOC INTERFACE

The ACU provides and accepts identical signals to and from all partitions. While these signals may have different meanings for individual IOCs, the ACU action does not vary from partition to partition. The one, limited, exception to the above statement is the SET MODE instruction that is limited to partition zero. Not all IOC produce all of the interface signals, but certain responses are common to all. A brief description of the IOC interface signals, and their uses is given below.

In using the signals listed below, the IOC has three options other than READ/WRITE that can be envoked. These three option signals are listed first because of the extensive changes that they will cause in the overall operation.

- TERM-RD - Terminate Read. An IOC option that can be used to end a READ operation prematurly. The TERM-RD signal is not acted upon by the ACU unless the instruction has the non-fill bit. When the non-fill bit is present, and TERM-RD is received, the ACU sets LAST (in the IOC) ending the operation without entering any more characters into memory. If the non-fill bit is not present, the IOC will enter blanks for the remainder of the instruction character count. These blanks are converted to zeros by the ACU if the transfer is made under a READ CONTROL (LOAD) instruction.

- INH-TIMEOUT - Inhibit Timeout. Prevents the ACU from switching partitions after the normal 37.5 ms and a sucessful branch. An IOC with this option can monopolize the ACU for extended periods. However, a software instruction BRANCH & SWITCH will break the monoply.

- OUT-REQ - Out Request. An IOC option that can be given to the ACU during a READ operation to reverse the data transfer. When OUT-REQ is active (logic Ø), the ACU sends a character to the IOC from memory, even though the instruction may be a READ. The actual character transfer is through the normal INTerrupt routine, and OUT-REQ must be active on a character-by-character basis.

- P-LIM - Partition Limit. BCD signal from the IOC that determine the partition size of the IOC. The P-LIM signals come from hardwire jumpers on thr IOC card that occupies card slot F in the ACU module, or E, G, J, or L in an Expansion module. The BCD number represents the partition size in thousands of characters.

- PRIV-CHAN - Priveledged Channel. A signal that is within the Model 20 only. In the Model 20 (only) a portion of common memory can be specified (by jumpers on the RBA card) that requires a PRIV-CHAN patch on the IOC before it can enter that memory area.

3-4.2 READ/WRITE

IOC INTERFACE (Continued)

- SEL-DIG and SEL-GROUP - These signals uniquely select an IOC by its physical position in the system. The SEL-DIG and SEL-GROUP signals are generated by the X counter within the ACU. The selection lines are shown in the X counter portion of an earlier part of this section.

- IO BUSY and P/IO BUSY - IO BUSY is the marker that indicates to the ACU when the IOC is operating on, or processing input/output data, and cannot accept new instructions. When a READ or WRITE instruction is given to an IOC, the ACU presets the IO BUSY flip-flop in the IOC by using the P/IO BUSY signal.

- IO BUSY can be reset, or cleared, by the IOC for a number of reasons, depending upon the nature of the IOC. However, when IO BUSY is reset, it is a signal to the ACU that the partition can be serviced. Status is posted by the IOC after every input/output operation is complete.

- INTERRUPT and INT-REQ - These two signals are IOC generated. They differ only in that INTERRUPT is the direct signal from the IOC INTERRUPT flip-flop, and INT-REQ is gated by response to being selected by the ACU (ON-LINE).

  INTERRUPT or INT-REQ informs the ACU that the IOC is ready to transfer a character (either into or out of memory). All data transfers through the IOC to or from peripherals are accomplished through INTERRUPT, one character at a time.

- INP DATA - A set of six lines over which character bits are sent from the IOC to the ACU. After an input/output operation has been completed, the IOC status character is also sent on the same lines.

- OUT-DATA and IOC DATA - The OUT-DATA lines carry character bits 1 through 5 from the ACU to the IOC. The IOC DATA lines carry bits 6 and 7 from the ACU.

- IOS-TO-MN - The enabling signal for the IOC output buffer or shift register. This signal releases the character bits from the IOC onto the ACU M and N lines.

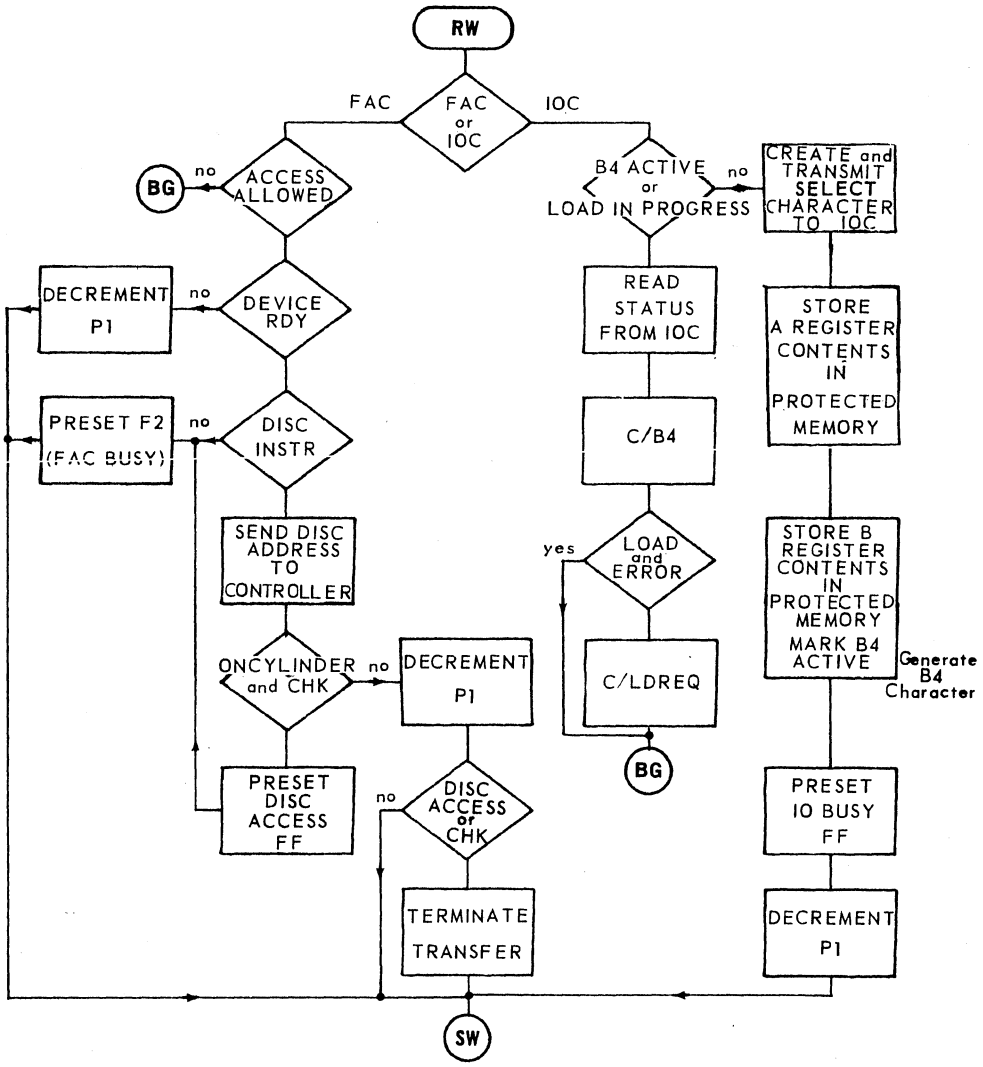
- C/INT - Clear Interrupt. Generated by the ACU when the IOC interrupt request has been answered. C/INT resets the INTERRUPT flip-flop in the IOC.

- LOAD-IOS - The ACU signal that is used to strobe a character into the IOC input register or buffer. The initial IOC Select Character is also strobed to the IOC by LOAD-IOS, followed in that case by the P/IO BUSY signal.

- P/LAST - Generated by the ACU when the instruction character count is exhausted, or when the IOC produces TERM-RD during a non-fill READ instruction.

- SERVICE-REQ - Service Request. An IOC signal that is usually from operator action at a peripheral or from an incomming (ringing) communication circuit. The signal is posted to theACU, allowing a branch on service request if the software program contains that instruction. If the branch on service request instruction is not present, the SERVICE-REQ signal has no effect on the ACU operation.

- C/SVRQ - Clears the service request when it is answered or by system reset.



LOGIC FLOW CHART

ACU READ/WRITE

3-4.2 READ/WRITE

IOC INTERFACE (Continued)

LOAD-REQ and P/LOAD-REQ - An IOC flip-flop output that can be considered as a functional part of the ACU. Each IOC has a LOAD-REQ flip-flop that is unique to the partition, but only those partitions that can load program are able to set the flip-flop. The ACU signal P/LOAD-REQ will set the flip-flop whenever an error is found in the software program. This is a direct result of the CHECK signal in the ACU.

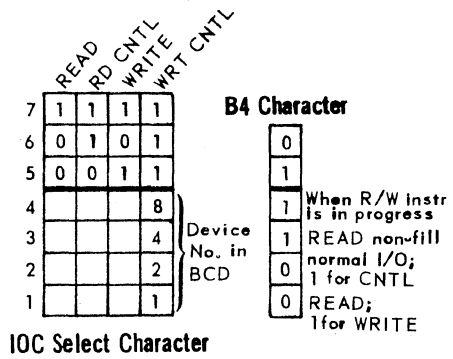
C/LOAD-REQ - Clear Load Request. Generated by the ACU and given to the IOC when the ten character "bootstrap" instruction has been successfully loaded. Some IOCs cannot load program and must simulate the process by placing good (normal) status on the INP-DATA lines and resetting IO BUSY. The ACU generates C/LOAD-REQ in this case because the instruction is considered complete if IO BUSY is reset.

CHECK and P/CHECK - CHECK indicates that some error in the software program has been detected. All IOCs have a CHECK flip-flop that is unique to the partition, but can be considered as a functional part of the ACU. When the ACU finds an error in the program, such as an address that is too large for the partition size, or an invalid instruction, the P/CHECK signal is sent to the IOC. Some IOCs have the ability to set CHECK because of an impossible instruction (for that IOC) or because of an impossible sequence of instructions. The ACU always interprets CHECK as a program error, and returns with a READ CONTROL (LOAD) instruction.

OPERATION

A READ/WRITE operation starts in BG 7, where the F code from an instruction that was pulled in BG 3 and 4 is strobed to the Function Counter. This causes a logic jump to the indicated function, which in this example is a READ/WRITE. The general logic flow while operating in READ/WRITE is shown on the opposing page. It is assumed that to reach this point in the operation that all checks for Interrupt, IO BUSY, power fail, etc have been made.

IOC READ or WRITE instructions must be fetched at least twice, once to initiate the operation, and once to discover that it has ended and status must be taken. The actual character transfer process is handled through the interrupt routine while the ACU is servicing other partitions. When a READ or WRITE instruction is initiated, the ACU sends an IOC Select Character to the IOC (see the inset) and sets the IO BUSY flip-flop. IO BUSY keeps the ACU from entering the partition until all of the characters are transfered, or the operation is ended by the IOC resetting IO BUSY. During initiation of the R/W, the ACU also places a 1-bit in the 4th bit position of the B4 character (in protected memory). The P count is also decremented ten counts so that the same instruction will be pulled when the ACU next services the partition.



After the operation is completed (through interrupt), the IO BUSY flip-flop is reset by the IOC to signal to the ACU that it is no longer involved in an I/O operation. The next time that the ACU attempts to service

3-4.2 READ/WRITE

OPERATION (Continued)

the partition, it is not turned away by IO BUSY. The usual checks for interrupt, power fail, etc. are made, the P count is brought out of protected memory, and used as the address for the instruction pulling. This is the same P count that was decremented and stored into protected memory when the READ/WRITE instruction was initialized. Because the P count was decremented, the same instruction is pulled again. However, this time, the 1-bit in the 4th position of the B4 character tells the ACU that an I/O instruction was already in progress, and status must be taken.

The ACU reads the character that is on the M and N lines, and interprets it as the status report from the IOC. This character was assembled in the IOC and made available before the IO BUSY flip-flop was reset. The Select Character that initiates the instruction, and the status character are the only character transfers between an IOC and the ACU that are not through the interrupt process. When the status character is taken by the ACU, the condition code flip-flops are set to the indicated status. The ACU then returns to BG where the next instruction is pulled. The next instruction in sequence should be a BRANCH on condition (dictated by software standards), but there is no hardware enforcement of these standards. Bad status will pass undetected if it is not tested by BRANCH instructions. After a BRANCH & SWITCH or BRANCH and timeout, the status of the condition code flip-flops is stored in the 7-bits of P1, P2 and P3.

When the partition is serviced again by the ACU, the P count is retrieved (in SW) before the instruction is pulled. The previous status (before the partition was switched) is restored to the condition code flip-flops from the 7-bits of the P characters from protected memory. The status can then be tested by a BRANCH instruction for another condition, or may eventually be replaced by status from a following instruction. A summary of I/O status conditions is given below.

Condition Code	STATUS	ZERO	MINUS	CARRY
1	ERROR or FAULT	0	1	-
2	NORMAL	1	-	-
3	FLAG	0	0	-
4	FAULT	0	1	1

- ERROR indicates that the device may have received erroneous data.
- NORMAL indicates no unusual condition.
- FLAG indicates a condition that has various meanings according to the design definition of the particular device.
- FAULT indicates that either a no response or FAULT response was received from the selected device. An IOC (or FAC) will not continue giving data to a unit after determining a FAULT condition.

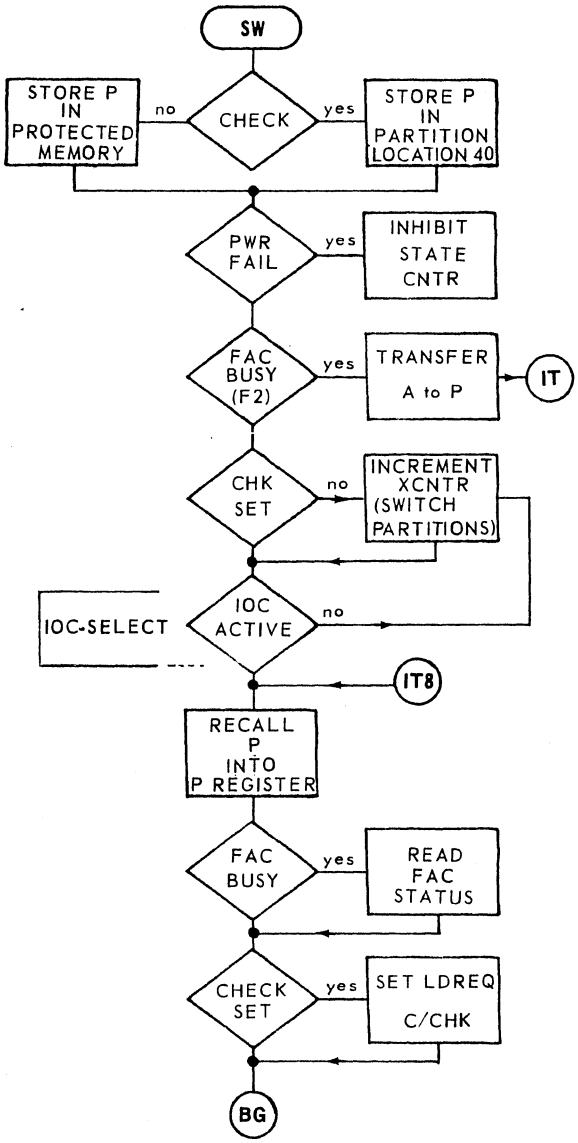
3-4.2 READ/WRITE (Continued)

FAC READ/WRITE

An FAC READ/WRITE differs from an IOC READ/WRITE, in that if all conditions are right, the instruction is pulled only once. The instruction pulling (in BG) is identical to an IOC operation, up to the point where a jump is made to READ/WRITE. The READ/WRITE function has seperate steps for IOC and FAC operations. Steps Ø through 9 are IOC, steps Ø, and 10 through 16 are disc/FAC, and steps Ø and 10 are non-disc FAC operations.

Step Ø in R/W test that the operation is an FAC, and that the operation is allowed by the FAC Protect Character. The FAC operation is determined by K1 remaining reset (as determined by the lowest bit in LB), and the access to FAC devices is determined by the A4 character of the A-protected address. All allowed FAC operations jump from R/W, step Ø, to R/W, step 10. In step 10, the FAC device number (from LA in the instruction) is sent to the FAC controllers, and if they are not busy, they send back an acknowledgement. If an acknowledgement is not received (because the controller is busy, the selected tape drive is rewinding, etc.) the ACU jumps to SWITCH and services the next partition in normal sequence. For any FAC device other than a disc, an acknowledgement causes the F2 flip-flop to be set, indicating that the FAC is busy. The ACU then jumps to SW, and soon to Interrupt, where the transfers will be carried out.

A disc address is more complicated, and takes six more steps to direct and verify the head positions. If any of the specified portions of the address (drive number, cylinder, etc.) are not acknowledged, the ACU jumps to SW, and services the next partition in sequence. Each time the partition is serviced, the same R/W instruction is pulled and attempted. A disc R/W instruction may be pulled many times before it can be completed. The disc controller will not complete all acknowledgements until the heads are on cylinder. At that time, the ACU is forced into Interrupt until the disc transfer is complete. While in the Interrupt function, the ACU can service interrupt requests from other partitions until the RES-MEM signal is raised by the disc controller. RES-MEM stops the state clock, preventing further ACU action in the normal states. The disc transfers are made "between states" of Interrupt, and are completed before the state clock is allowed to run again.



LOGIC FLOW CHART

ACU SWITCH

3-4.3 SWITCH

SWITCH is used by the ACU to perform the "housekeeping" steps that are needed to stop processing instructions in one partition, and move to the next partition. The ACU jumps to SWITCH for a variety of reasons that roughly fall into three groups. If the ac power is failing, the ACU jumps to Switch and ends operation in the active partition before the stored power (in the power supply) is depleted. If an error is detected within a partition, and continued operation would be useless, the ACU steps to the next partition. The third general reason for switching partitions is time. Each partition is alloted approximately 37.5 ms of processing time. When the 37.5 ms has been used, the ACU will switch partitions after the next successful BRANCH. Some I/O devices, such as the MDTS IOC, can inhibit the switching feature, and can hold the ACU indefinately (until the IOC releases the INH-SW signal). Other than the 37.5 ms time consideration, the ACU will switch partitions after initiating a relatively long operation within an I/O device. This operation could be a "seek" on the disc, or a READ/WRITE operation in an IOC that will be completed by the IOC through the INTerrupt process.

The SWITCH function (shown in the diagram to the left) marks the partition inactive as it stores the P count, moves to the next partition, and pulls the P count for that partition.

System start up and shut down is in SW 2, where failing power is detected. The ACU waits in that state until power returns, than after a system reset, processing starts in the next sequential partition.

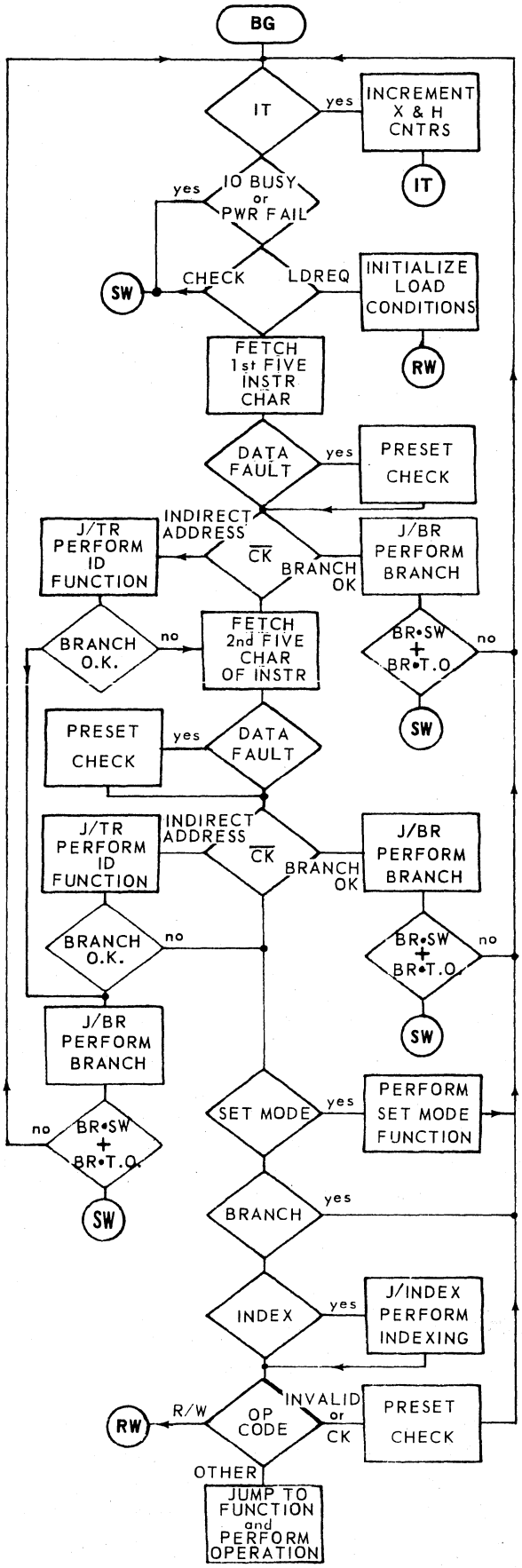
3-4.4 BEGIN

BEGIN is entered shortly after the ACU switches to the partition, and again before each instruction is pulled from memory. It is a general starting place where tests are made for Interrupt requests, failing power, a busy IOC, check condition (data fault), and load request. See the logic flow chart on the following page.

In BEGIN, the instruction is pulled from memory in two groups of five characters each. The bits and groups in the instruction are placed into registers and tested for an invalid code, or data fault. An invalid code is a binary 2 or 3 in the Model 20, and only a binary 3 in a Model 21. A data fault is the lack of a 5-bit in any character (within the instruction) or greater than a binary nine in the lower four character bits for a Model 20. The Model 21 does not require the 5-bit, but does require that no instruction word character contains greater than binary nine in the lower four bits.

Once a function is determined, the ACU jumps to the hardware function that is necessary to perform the operation. Certain branches can be made after only the first five instruction characters have been pulled from memory. In that case, the second half of the instruction is left in memory, and ignored.

There are four functions that appear to be performed within BEGIN, but only one of these, SET MODE, is actually completed within the function. The others, BRANCH, INDEX, and INDIRECT ADDRESS (not valid in the Model 20) cause the ACU to jump to the proper function to perform the operation. However, when the operation is complete, the ACU returns to BEGIN and continues as before.

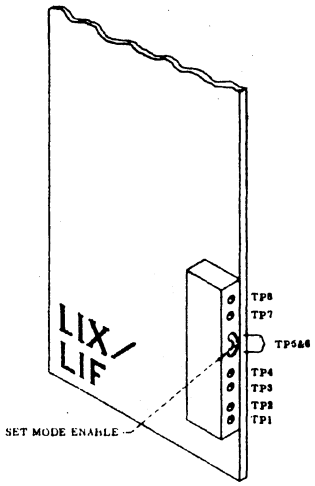


LOGIC FLOW CHART
BEGIN

3-4.4 BEGIN (Continued)

SET MODE (F=1010)

Set Mode is a limited means by which software instructions can duplicate the System Reset and Inhibit Switch functions that are ordinarily only available from the Test Panel. Set Mode is only useable from partition Ø, and even then only if the enable jumper is installed on the LIF/LIX card (see inset). The System Reset that is generated by the SET MODE operation does not reset the ACU module, but does reset all other modules.



The Inhibit Switch condition that can be generated by the Set Mode instruction remains until it is cleared by a second operation under Set Mode. The small table below shows the ACU response to the IA, and IB bits of the instruction word, while operating under the Set Mode instruction. The term not Ø means that the IA or IB digits are any binary number other than zero.

	IA		IB	
	Ø	Not Ø	Ø	Not Ø
INH-SW	Clear	Preset	-	-
I/O RST	-	-	No	Yes

Example:

The operator wishes to load a software program into partition 1, but partition 1 is an MDTSIOC, and has no program loading facilities. The program address for partition 1 is loaded into a known place in Common Memory (in this example 0400).

From partition zero, with the Set Mode enabled, the instruction word that is shown below is given. The Set Mode portion of the instruction initiates an I/O reset, and sets the INH-SW flip-flop.

F3	F2	F1	F0	AC	IA1	IA0	IB1	IB0	BC
1	0	1	0	0	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0
P	0	P	0	0	P	P	P	P	0

Generate I/O reset Set INH-SW

1	0	0	0	1	0	0	0	0	1
1	1	1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	1	0	0	0	1
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0	0	1
P	0	4	0	P	5	0	0	0	U

Transfer 5 characters from location 0400 (in Common) to location 0005 (in Common).

The next instruction is to transfer five characters (a new P count) to address 0005 in common, the protected P address for partition 1. A final instruction, P0P0000000, is given. This is a second Set Mode instruction for clearing the INH-SW flip-flop.

On the next normal service of partition 1, the ACU pulls the P number that was placed there under Set Mode, and goes to that address for the instruction to be acted upon. Setting at the P address that was transfered, should be a "bootstrap" instruction for loading program into partition 1 from the disc, tape, or other sources.

Condition codes are not affected by the Set Mode instruction.

3-4.5 INDIRECT ADDRESS

Indirect address (not possible in a Model 20) is a function that substitutes a four character field from another part of memory in place of the specified A or B instruction address. If indirect addressing is used, the A or B address directs the ACU to the location of the four character substitute that is to be used. The four characters are not actually transfered into the instruction word, but are brought into the hardware register(s) by a normal non-destructive (ACU) read routine. Once this process is accomplished, the ACU jumps back into Begin to complete the original instruction, using the substitute address or addresses that are in the hardware registers.

The IDA bit (the 5-bit above LA) causes indirect addressing in the A address of the instruction if IDA=Ø. IDB controls indirect addressing of the B address in the same way. The A address and the B address can be indirectly addressed individually or both in the same instruction without interaction between them.

3-4.6 INDEX

Although INDEX is a hardware function, it is a subroutine that is performed during BEGIN that modifies the A and/or B address of the instruction by adding the contents of an index register to the address or addresses. The ACU jumps out of BEGIN to perform the steps that are necessary to index, then it returns to BG to complete the instruction. The index registers are not special hardware devices, but are specific areas of partition memory that are assigned for that purpose. Each partition has three of these assigned register addresses that are located at 0011 through 0014, 0021 through 0024, and 0031 through 0034 relative (partition) address. The index register character positions can be written into or read from with no restrictions. However, when an instruction requires indexing, the contents of those positions are considered as the register contents, and are added to the A and/or B instruction address as required. Indexing numbers must pass all DATA FAULT tests.

The IA and IB bits within the instruction word control which of the three areas in core, if any, are to be used for indexing. The IA and IB digits represent the binary value of the 10s digit of the index register location. The table below shows this relationship.

IA1 IB1	IA0 IB0	Binary Value	Index Register
0	0	0	none
0	1	1	11-14
1	0	2	21-24
1	1	3	31-34

Neither the index digits or the A or B addresses in core memory are changed by the indexing operation. The addition is accomplished in hardware registers, leaving the characters in memory untouched. The numeric parts (lower four bits) of the contents of the specified index register are brought out, one digit at a time, and added to the contents of the A and/or B hardware register. The contents of one index register can be used to modify either one or both of the A and B addresses of the same instruction word, as the index characters are not cleared or destroyed by use.

Because indexing adds numerically to an address, it can cause address errors by trying to specify an address that is greater than the allotted memory size.

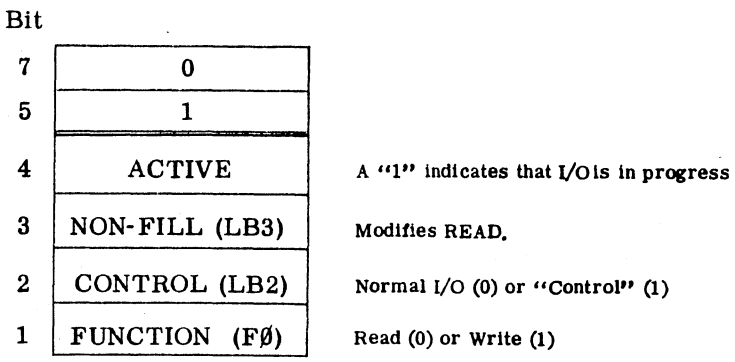
3-5.0 INSTRUCTION SET

3-5.1 READ (00)

F = 0000
LA = Device I.D. Number
Only numbers 0 through 9 may be used: device #0(0000) of the FAC is the Disc Controller; devices 1 through 4 of the FAC are tape drives.
LB = Variant
LB = 0(0000) for "Read File Access Channel"
LB = 1(0001) for "Read I/O Channel"
LB = 5(0101) for "Read, Non-Fill, I/O Channel"

Bit 1 determines whether the operation will be IOC or FAC.
Bit 2 will cause the Load light to light on the selected peripheral (if there is a Load light).
Bit 2 does not change the operation in any way.
Bit 3 determines whether or not the operation will be non-fill.

A = Memory Address of start of record
B = Number of characters to be read for all except disc. Address of disc address for disc.
AC = Mark that the A Address is in the Common Area.
BC = Mark that the B Address is in the Common Area if B is the address of the disc address. Otherwise BC is ignored.
IA,
IB = Indicate indexing. The hardware will perform any indicated indexing.



B4 DIGIT

CONDITION CODES (STATUS). Numbers indicate BRANCH variants.

(1) ERROR or FAULT

Error indicates that erroneous data may have been received; it is derived from hardware error-checking circuitry. Fault indicates that data transmission was incomplete, due to a faulty device. If a FAULT occurs before the transfer of data is complete, the IOC will signal the ACU to "Terminate Read" and the ACU will either fill the field with Øs from the IOC or terminate, depending on the Non-Fill bit from LB.

(2) NORMAL

(3) FLAG

FLAG indicates something unusual. It is defined by the selected device:

Typewriter: ALERT key
Disc: Marked Record

(4) FAULT

(A test for Branch variant 4 will separate the two conditions of Branch variant 1.)

		ZERO	MINUS	CARRY
(1)	ERROR or FAULT	0	1	-
(2)	NORMAL	1	-	-
(3)	FLAG	0	0	-
(4)	FAULT	0	1	1

OPERATION - READ/IOC

Data from the selected device will fill an area of the memory starting at A and running continuously to A+B-1, modulo-10K. The meaning of "modulo-10K" is shown in the second example.

Example:
A = 0007
B = 0006
Six characters will be entered.
They will occupy locations 7 through 12.

0007	0008	0009	0010	0011	0012
R	E	C	O	R	D

Example:
A = 9950
B = 0112
Processor size is 10K. One hundred twelve characters will be entered. The first fifty will occupy 9950 through 9999. The next sixty-two will occupy locations 0000 through 0061. Wrap around occurs only when the partition size is 10K: with smaller partitions, address error occurs.

Provision is made in the hardware for various operator actions.

(1) The operator may "terminate entry". If the "Non-Fill" bit in LB is 0, the hardware will fill the remainder of the field with blanks.

Example:
A program contains a 100-character field where customer names are entered. The last name entered was CHRISTOPHER JOHNSON. The operator next enters JOE DOE from an alpha-numeric keyboard and then depresses the "ENTER" key, which terminates the entry. When the operator terminates, the field reads

JOE DOEPHER JOHNSON

The hardware completes the entry with blanks:

JOE DOE ¢¢¢¢¢¢¢ (etc.)

(2) The operator may activate the "Repeat and Error" operation by depressing the "ERROR" key (previous section). The field will still be completed with blanks before the instruction can be repeated, except in a "READ-NON-FILL".

(3) If the selected device is wired to request LOAD (device 0 only), the operator may initiate a load. If the "Non-Fill" bit in LB is 0, the entry will be completed with blanks before the request to load is honored.

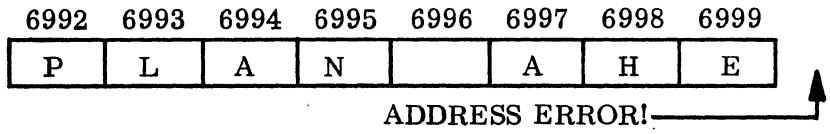
The above examples are modified if LB = 5, which indicates READ-Non-Fill. In that case, the unused portion of the field is not filled with blanks; instead the B Address in the Protected Area of Memory is left at the count where the READ was terminated and indicates the number of remaining characters in the field.

The FAULT condition provides the means by which a program can by-pass an inoperative peripheral. FAULT will cause the field to be filled with blanks so that the ACU may proceed; the condition FAULT can be detected by a BRANCH, which should follow every I/O instruction.

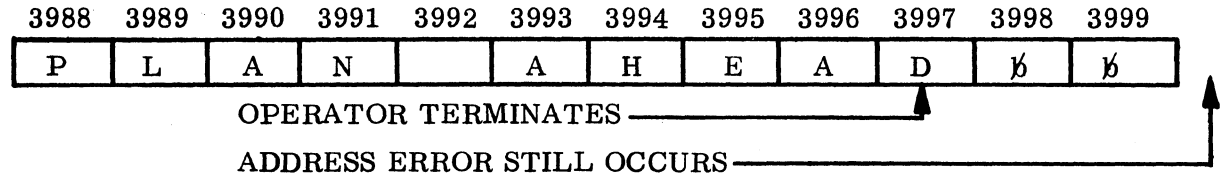
For example, if a card reader has no cards but is otherwise in operating order, there is no FAULT; the reader merely sends "Busy" to the IOC, holding up instruction execution. A faulty card reader is one that is not plugged in, not turned on, or not in operating condition. Other examples of FAULT will occur if the program addresses a non-existent peripheral or if it tries to read from an output device. In all but the last case the IOC will time out after trying to get a response from the selected peripheral. In the last case it is possible for the output device to be wired to send "FAULT" to the IOC if it is asked to read. The IOC can respond to the FAULT instantly without waiting for time out.

For partitions that are less than 10K in size, it is possible for the field specified by A and B to be partially or completely outside the partition. The hardware will not detect this condition until the first time that it tries to perform a core cycle outside of the partition. Hence the portion of the field that lies within the partition will be filled according to the above rules before the machine finds the address error. Address error causes the machine to automatically go to Load. Condition Codes are not posted.

Example:
A = 6992
B = 0010
Partition size is 7K.



Example:
A = 3988 (AC)
B = 0014
The size of the Common Area is only 4K.



Clearly, it is important for the programmer to know the size of the Common Area as well as the size of his own partition.

OPERATION - READ FAC

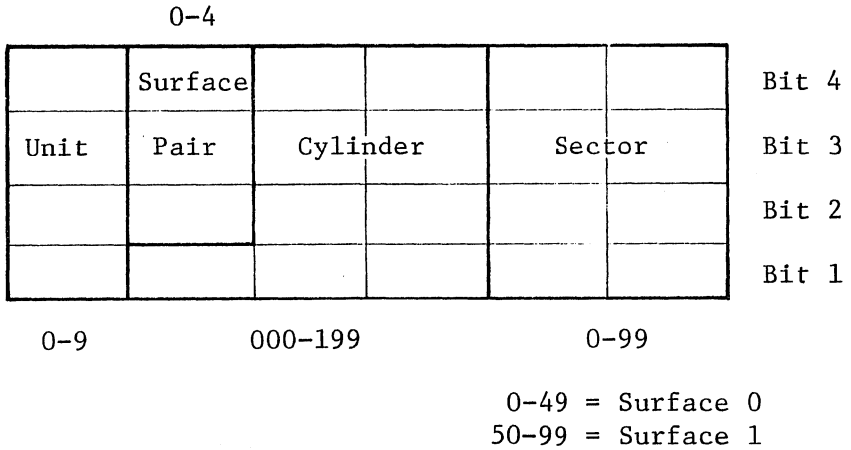
Data from the selected device will fill an area of the memory starting at A and running continuously to A+B-1, modulo-10K, except if the selected device is a disc. Data from a disc fills an area of the memory from A to A+99, modulo-10K. Unlike I/O, there are no "operator actions", so the amount of data (record length) is always defined by the field length. There is no bit conversion, as the data is in the internal machine form. Read non-fill is not allowed.

The READ must be completed before the ACU goes to the next program step. The ACU will try repeatedly to select an FAC device until it receives an acknowledge from the FAC. The FAC determines the FAULT condition just as the IOC does for I/O operations. Likewise, the ACU may encounter an address error while executing an FAC operation, just as for I/O.

If the FAC Protect Character indicates that the READ FAC is prohibited, the instruction will be ignored by the ACU and there will be no indication to the operator or programmer.

For the operation READ DISC, the B Address gives the core location where the disc address starts. The hardware will use six consecutive characters, starting at B, for the disc address. Only the bits 1-4 are used, and these must form a binary number from 0 through 9.

The figure shows the disc address as the disc hardware interprets it. The six-digit disc address allows access to 10^6 records. Simply incrementing the address will allow access to 100 records per head position. The amount of storage available in a given installation determines the upper limit of the disc address.



DISC ADDRESS

The disc hardware will record all "1"s or some other distinctive mark in a bad spot on the disc and set FLAG. Detection of the mark during a DISC READ will likewise cause the FLAG condition after the READ has been completed. The programmer thus has a means of branching to alternate addresses to avoid bad spots on the disc.

3-5.2 WRITE

F = 0001
LA = Device I.D. Number
Only numbers 0 through 9 may be used: device 0(0000) of the FAC is the Disc Controller; devices 1 through 4 of the FAC are tape drives.
LB = Variant
LB = 0(0000) for "Write File Access Channel"
LB = 1(0001) for "Write I/O Channel"
LB = 2(0010) for "Write Control, File Access Channel"
LB = 3(0011) for "Write Control, I/O Channel"

Bit 1 determines whether the data will be sent to an IOC or the FAC.
Bit 2 determines whether it will be a "normal" or a "control" output.
Bits 3 and 4 of LB are not used, and should always be 0.

A = Memory Address of start of record
B = Number of characters to be written for all except disc. Address of disc address for disc.
AC = Mark that the A Address is in the Common Area
BC = Mark that the B Address is in the Common Area if B is the address of the disc address. Otherwise BC is ignored.

CONDITION CODES (STATUS). Numbers indicate BRANCH variants.

(1) ERROR or FAULT

Error indicates that the output (or FAC) device may have received erroneous data. Fault indicates that there was either no response or a response of FAULT from the selected device. The IOC or FAC will not attempt to write anything further after deciding that there is a fault.

(2) NORMAL

(3) FLAG

Flag indicates something unusual. It is defined by the selected device.

(4) FAULT

(A test for Branch variant 4 will separate the two conditions of Branch variant 1.)

		ZERO	MINUS	CARRY
(1)	ERROR or FAULT	0	1	-
(2)	NORMAL	1	-	-
(3)	FLAG	0	0	-
(4)	FAULT	0	1	1

OPERATION-WRITE IOC. Data from an area of the memory starting at A and running continuously to A+B-1, modulo-10K, will be transmitted to the selected peripheral. The significance of the "modulo-10K", which is inherent in the size of the memory partitions, is shown in the second example under paragraph 3F1b. Output bit conversion is explained in Section 2C2 for both WRITE and WRITE CONTROL; the only difference between the two operations is the different bit conversion scheme.

The WRITE must be completed before the ACU goes to the next program step. A printer that is out of paper will indicate to the IOC that it is busy, halting program execution, until the operator takes some action that will allow the WRITE to finish.

Fault is defined in a manner similar to the definition for input devices. An output device that fails to acknowledge signals from the IOC is considered to be faulty. Note that the printer in the above example is not faulty--it acknowledges the IOC and sends back busy.

An address error may occur during output just as it may occur during input.

OPERATION-WRITE FAC. Data from an area of the memory starting at A and running continuously to A+B-1, modulo-10K will be transmitted to the selected device except if the selected device is a disc. Data to the disc is the 100-character record starting at A and running continuously to A+99, modulo-10K.

The WRITE must be completed before the ACU goes to the next program step. The ACU will try repeatedly to select an FAC device until it receives the acknowledge from the FAC. The FAC determines the FAULT condition just as the IOC does for I/O operations. Likewise, the ACU may encounter an address error while executing an FAC operation, just as for I/O.

For the operation WRITE DISC, the B Address gives the core location where the disc address starts.

The disc hardware will record all "1"s or some other distinctive mark in a bad spot on the disc and set FLAG. The determination that a spot is bad will be made by the disc hardware after several unsuccessful attempts to write and check read. Branch on FLAG could be used to locate an alternate disc address from a table or algorithm, and the data could be recovered the same way in READ. If the FAC Protect Character indicates that the WRITE FAC is prohibited, the instruction will be ignored by the ACU and there will be no indication to the operator or programmer.

Write control is not used during WRITE DISC, but it can be used to rewind tape drives, etc.

3-5.3 MOVE ADDRESS (03)

F = ØØ11
LA, LB = Number of address characters to be transferred. LA is the 10s digit, and LB is the unit digit. LA=Ø, LB=Ø means 100 characters.
A = Address of MSD of field to be moved.
B = Address of MSD of the destination.
AC= Indicates the A address is in Common if AC=1.
BC= Indicates destination address is in Common if BC=1.
IA, IB = Indexing for A or B addresses.
IDA, IDB = Indirect addressing for the A and B fields respectively.

Move Address (Address Transfer) is not a valid instruction in a Model 20, but is valid in all Model 21 type processors. MOVE ADDRESS transfers bits 1 through 5 of an entire data field (up to 100 characters), one character at a time, from one location in memory to another. The transfer begins at the Most Significant Digit (MSD) as specified by the A address in the instruction. The destination address is specified by the B address in the instruction. The 7-bits of the characters in the B field are not changed when the lower bits are entered from the A field. In effect the residual 7-bits that are in the B field before transfer, are merged with the transfered bits. The AC and BC bits in the instruction word are the same as for other instructions, where a 1-bit in the position designates that the address (A or B) is in the Common area of memory.

The Move Address instruction is not limited to any specific number of characters that can be transferred except that the maximum is 100 (specified by 00) and the minimum number is 01. The LA and LB portions of the instruction word specify this quantity.

Indexing and Indirect addressing can be specified in the Move Address instruction, and will be accomplished before the address transfer is made.

For the operation of the transfer process, see the instruction TRANSFER, which is the hardware function under which Move Address is accomplished.

CONDITION CODES (STATUS)

Condition code 1 will be set if the Least Significant Digit (LSD) of the transferred field sets the MINUS flip-flop (specifying a Common address).. Condition code 3 will be set if the LSD is positive (specifying a partition address). The Move Address instruction will never end in condition codes 2 or 4.

3-5.4 ADD (04) & SUBTRACT (07)

F = 0100/0111
LA = Length of A Field
LA = 0 through 9, where LA = 0 indicates a length of 10.
LB = Length of B Field
LB = 0 through 9, where LB = 0 indicates a length of 10.
LB $\geq$ LA
A = Address of MSD of A Field
B = Address of MSD of B Field
AC = Mark that the A Address is in the Common Area
BC = Mark that the B Address is in the Common Area
IA,IB = Indicate Indexing

CONDITION CODES (STATUS). Numbers indicate BRANCH variants.

(1) MINUS (and non-zero)

(2) ZERO

(3) PLUS (and non-zero)

(4) OVERFLOW

		ZERO	MINUS	CARRY
(1)	MINUS (and non-zero)	0	1	-
(2)	ZERO	1	-	-
(3)	PLUS (and non-zero)	0	0	-
(4)	OVERFLOW	-	-	1

OPERATION B$\pm$A$\rightarrow$B (LB $\geq$ LA). The contents of the A Field adds to, or subtracts from, the contents of the B Field according to the rules of algebra. The answer replaces the former contents of the B Field. The contents of A remain unchanged. In the LSD of B, bit 7 indicates the sign of the answer and bit 5 is made 1: all other zone bits are left unchanged from the original contents in both A and B. The final states of the condition FFs indicate the status of the answer in B.

There is a SUBTRACT FF which starts set if the function code is SUBTRACT (0111) and starts reset if the function code is ADD (0100). The POSITIONING algorithm is used to count the A and B Addresses to the LSDs of the A and B Fields. If bit 7 in the LSD of A is "1", SUBTRACT is complemented; likewise if bit 7 in the LSD of B is "1". Like signs leave SUBTRACT unchanged. Bit 5 in the LSD of B is forced to "1" and bit 7 is left unchanged, so the (initial) sign of the answer is the "sign of B".

Only Bits 1-4 are combined in the adder according to the indication of the SUBTRACT FF. An attempt is made to correct the resulting four bits, digit-by-digit, to BCD. In "machine add" (SUBTRACT reset, regardless of function code), any combination over 9 is added to 6 (0110) once before being written into core.

Examples:

1.	2	0010
	+2	+0010
	4	0100

2.	3	0011
	+9	+1001
	12	1100
	+6	+0110
	C2	C0010

3.	9	1001
	+9	+1001
	18	C0010
	+6	+0110
	C8	C1000

4.	(14)	1110
	+8	+1000
	C6	C0110
	+6	0110
	C(12)	C1100

Example 3 looks reasonable, but notice how the hardware must treat the first CARRY: It is not added to the least-significant bit during correction, but is instead tacked onto the final answer. Example 4 shows that if a digit in A and/or B is greater than 9, the result may be greater than 9 after correction.

Machine subtract is accomplished by adding the 15s complement of each "A" digit to the corresponding "B" digit. Carry starts set for the first (LSD) digit; thereafter, its absence or presence indicates whether or not there was a "borrow". Any digit combination less than 0 is corrected by adding to 10.

Examples:

		C
1.	2	0010
	-2	+1101
	0	C0000

Note that CARRY remains set, which is the normal condition (no "borrow").

		C
2.	3	0011
	-9	+0110
B	(10)	1010
	+(10)	+1010
B	4	~~C~~0100

The hardware resets CARRY to indicate a "borrow", regardless of the bit-by-bit carry.

		C
3.	(14)	1110
	-8	+0111
	6	C0110

		C
4.	8	1000
	-(14)	+0001
	B(10)	1010
	+10	+1010
B	4	~~C~~0100

		C
5.	2	0010
	-(14)	+0001
B	4	0100
	+(10)	+1010
B	(14)	1110

If CARRY is reset after all digits of A and B have been combined, there was an overdraft subtraction ($|A| > |B|$). The sign in B and the condition FF indication are complemented, and (B) subtracted from zero. Overdraft subtraction is always corrected, regardless of the values of LA and LB.

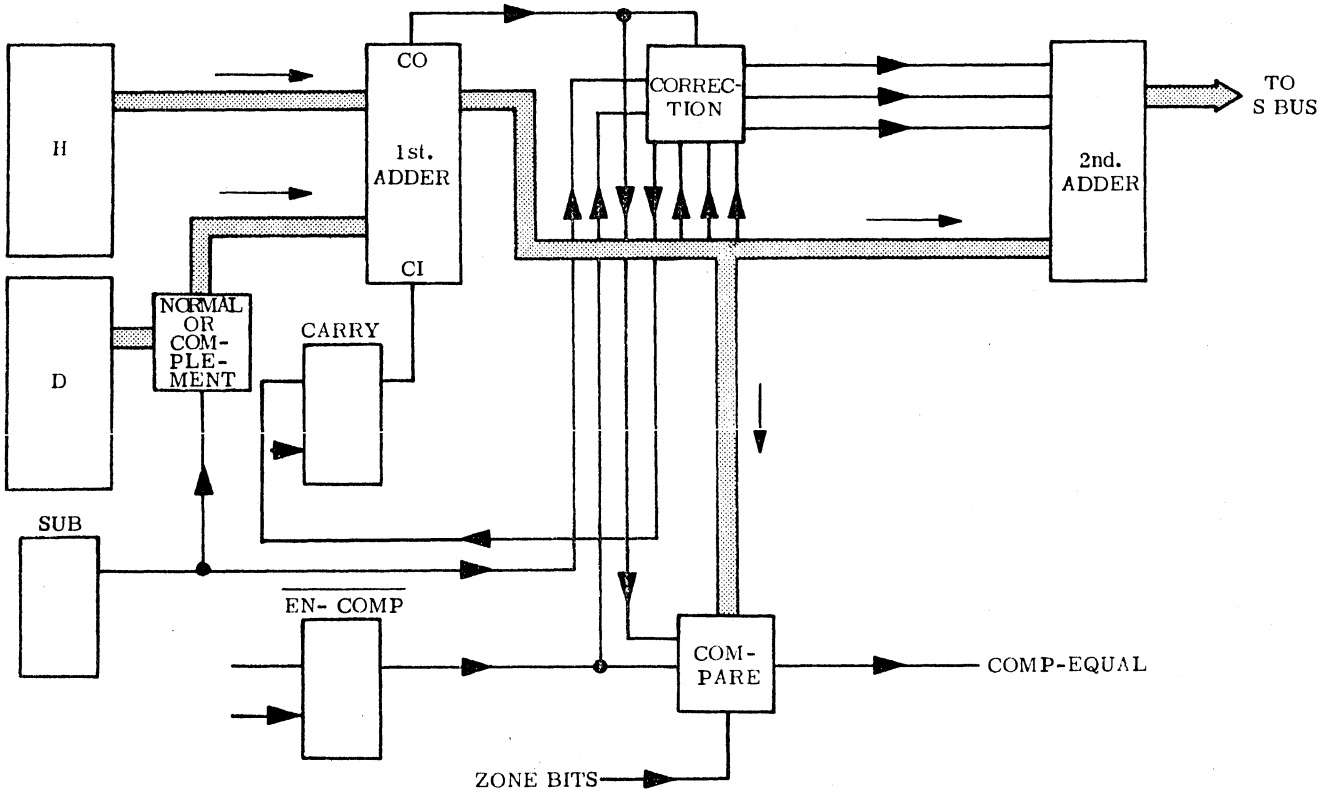
The condition OVERFLOW occurs only after a machine add. If LA = LB, an overflow indicates that a 1 was truncated from the MSD of the answer and the rest of the digits of the answer are in B.

If LA $<$ LB, the answer is derived as if the A Field were extended to the left with zeros until LA = LB. OVERFLOW may still occur and the missing digit will be 1.

If LA $>$ LB, the answer is derived only as far as the length of B permits, and the most-significant digits of A are ignored. OVERFLOW is not set just because LA $>$ LB; it will be set only if there is a CARRY (of 1) beyond the answer.

ADDER HARDWARE

The "adder" is made up of two separate binary adder chips and their associated circuitry. The two digits to be added are set into the D and H Registers. The outputs of these registers go to the first adder chip, along with the output of the CARRY FF. (If the SUBTRACT FF is set, the output of the D Register is complemented before it goes to the first adder.) The first adder supplies the uncorrected sum to the second adder, and a group of gates provides the correction factor. The second adder provides the corrected sum to the S bus. The carry from the second adder is always ignored.



BLOCK DIAGRAM, ADDER LOGIC

The rules for correction are as follows:

IF:	Then add to uncorrected sum in second adder:	
$\overline{\text{SUBTRACT}} \cdot \overline{(>9+\text{CARRY})}$	0	
$\overline{\text{SUBTRACT}} \cdot (>9+\text{CARRY})$	6	(Set CARRY FF if not already set)
$\text{SUBTRACT} \cdot \overline{\text{CARRY}}$	0	
$\text{SUBTRACT} \cdot \text{CARRY}$	10	

During the COMPARE function, the first adder is used to check for an unequal compare between the low order four bits of the two characters being compared. The zone bits are compared in another group of gates (NOT an adder). All corrections are disabled during COMPARE.

3-5.5 DIVIDE (05)

F = 0101
LA = Length of the divisor
LA = 0 through 9, where LA = 0 indicates a length of 10
LB = Length desired for quotient
LB = 0 through 9, where LB = 0 indicates a length of 10
A = Address of MSD of the divisor
B = Address of MSD of the dividend, which is replaced by the answer
AC = Mark that the A Address is in the Common Area
BC = Mark that the B Address is in the Common Area
IA,IB = Indicate Indexing

CONDITION CODES (STATUS). Numbers indicate BRANCH variants.

(1) MINUS (and non-zero)

(2) ZERO

(3) PLUS (and non-zero)

(4) OVERFLOW

OVERFLOW occurs if the first (most significant) digit of the dividend is equal to, or greater than, the first digit of the divisor. (The B address of the instruction addresses what is initially the MSD of the dividend; A, the MSD of the divisor.)

		ZERO	MINUS	CARRY
(1)	MINUS	0	1	-
(2)	ZERO	1	-	-
(3)	PLUS	0	0	-
(4)	OVERFLOW	-	-	1

OPERATION (B'÷A⟶B). The contents of the B' field (dividend) are divided by the contents of the A field (divisor). The quotient replaces the first LB digits of the dividend, leaving the last LA digits as the true remainder. The length of B' (the dividend) is equal to LA + LB.

Bit 5 of the LSD of the dividend is forced to be a "1"; bit 7 is left alone. Hence that part of the dividend that remains after division (the remainder) will have the proper sign. The sign of the quotient is placed (again with a "1" in the 5 bit) above the LSD of the quotient (core address B+LB-1, modulo-10K). All other zone bits of the quotient are made 01 (bits 7 and 5, respectively), whereas all other zone bits of the remainder and all bits in A are left alone. The final states of the Condition FFs indicate the status of the quotient.

The programmer must choose the B Address so that the proper B' will be assumed by the ACU. Since the MSD of the divisor must be greater than the MSD of the dividend, a problem such as 4 ÷ 2, for example, must be set up as 04 ÷ 2. This is necessitated by the method used to position the A and B "pointers" for the first subtraction, as illustrated in the following sequence:

Example 1: LA = 1 LB = 2	Example 2: LA = 2 LB = 4	Example 3: LA = 2 LB = 1

(Arrows show position of B "pointer")

	Ex. 1	Ex. 2	Ex. 3
START (After POSITIONING): B' =	123	123456	123
EXTEND B' FIELD BY LA: (At this point, check signs and store sign of answer in E2)	123	123456	123
EXTEND B' FIELD BY 1:	123	123456	123
COUNT B ADDRESS BACK LB TIMES:	123	123456	123
BEGIN REPEAT SUBTRACTIONS:	123 -X	123456 -XX	123 -XX

Choice of the proper B Address is best illustrated by the use of an example.

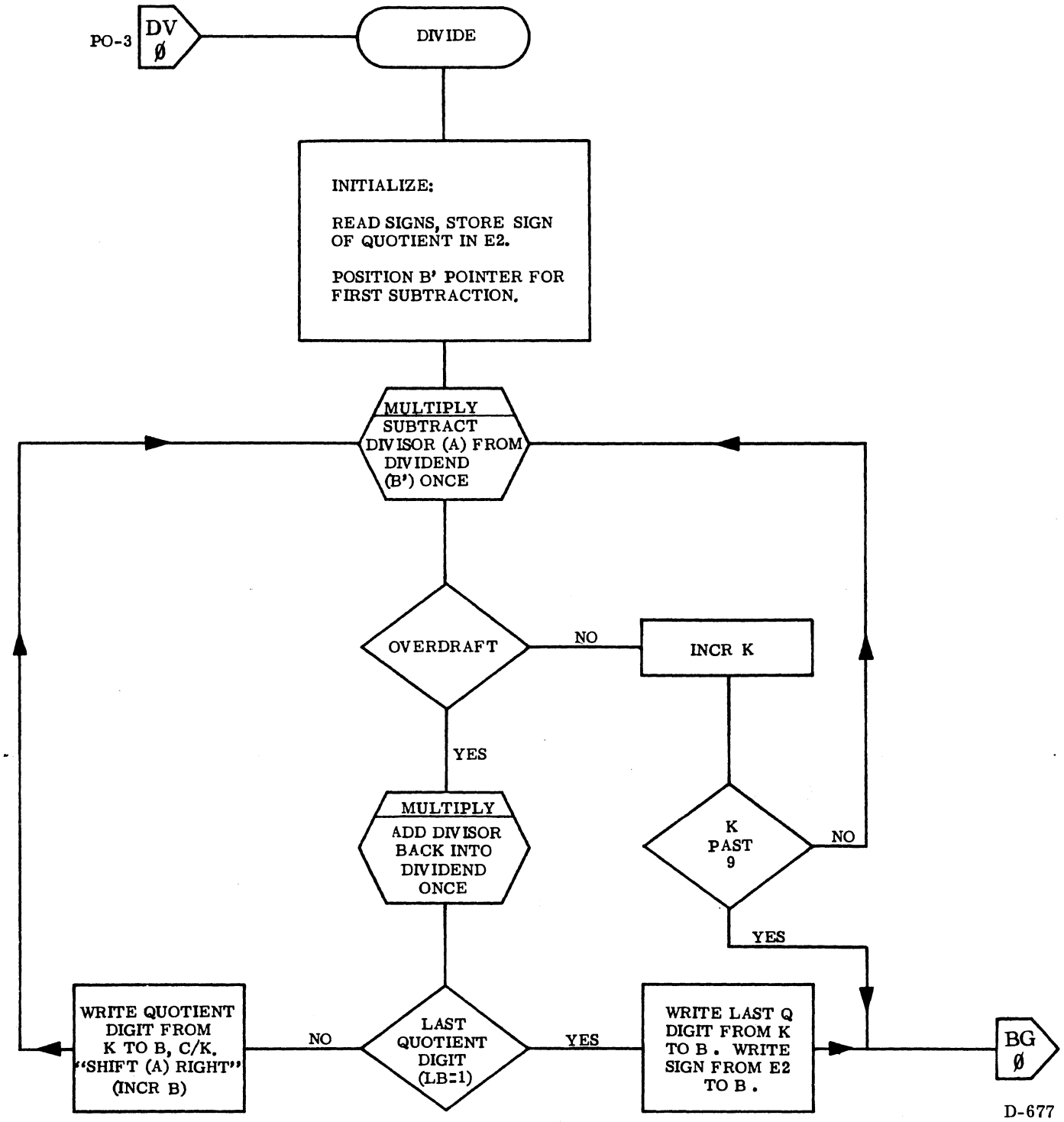
Assume that a "4" is stored in memory as shown:

999	1000	1001
0	4	X

If it is desired to divide the 4 by 2, the B Address must be specified as 999, and not 1000, since the dividend is equal to LA + LB, and must be at least two digits long. This is illustrated by comparing the results after choosing each of the two addresses.

LA = 1, LB = 1	(B = 999)	(B = 1000)
START (After POSITIONING):	B = 04	4X
EXTEND B' FIELD BY LA: (Check signs)	04	4X
EXTEND B' FIELD BY 1:	04	4X
COUNT B ADDRESS BACK LB TIMES:	04	4X
BEGIN SUBTRACTIONS:	04 -2	4X -2

It is obvious from this comparison that if the B Address is chosen to be 1000, not only will the initial subtraction occur more than 9 times, resulting in OVERFLOW, but also the wrong digit will be checked for the sign of the dividend.



SIMPLIFIED FLOW CHART, DIVIDE

3-5.5 DIVIDE (Continued)

After the pointers are positioned, repeat subtractions occur. For every subtraction that does not overdraft (CARRY remains set), 1 is added to K. When an overdraft occurs, (A) is added back into (B'), B is incremented once (moving the B' pointer one digit to the right), the quotient digit in K is written into the now-vacant MSD position of B', and the process repeats.

If the MSD of B' is too large (as in 4X ÷ 2), K will attempt to go over 9 (during the first group of repeat subtractions) before an overdraft occurs. This terminates the divide immediately and causes the OVERFLOW condition to be set. When this occurs the higher order digits of B' have been reduced by 10 x (A), and the MINUS, ZERO, and PLUS indicators have no meaning.

The subtractions are actually carried out by the same logic used in MULTIPLY. Thus, a divide operation continually jumps back and forth between the DIVIDE and MULTIPLY functions.

The flowchart on the opposite page shows the major logic actions during the divide operation.

3-5.6 MULTIPLY (06)

F = 0110
LA = Length of the multiplicand
LA = 0 through 9 where LA = 0 indicates a length of 10
LB = Length of the multiplier
LB = 0 through 9 where LB = 0 indicates a length of 10
A = Address of MSD of the multiplicand
B = Address of MSD of the multiplier, which is replaced by the answer
AC = Mark that the A Address is in the Common Area
BC = Mark that the B Address is in the Common Area
IA,IB = Indicate Indexing

CONDITION CODES (STATUS). Numbers indicate BRANCH variants.

(1) MINUS (and non-zero)

(2) ZERO

(3) PLUS (and non-zero)

		ZERO	MINUS	CARRY
(1)	MINUS	0	1	-
(2)	ZERO	1	-	-
(3)	PLUS	0	0	-

OPERATION A x B→B' The contents of the A Field (multiplicand) are multiplied by the contents of the B Field (multiplier). The answer replaces the former contents of the area of memory starting at B (MSD) and running to B + LA + LB - 1, modulo-10K. It is convenient to refer to the field occupied by the answer as the "expanded B Field", or B'.

In B' the zone bits of every character except the LSD are made 01 (bits 7 and 5, respectively). The 5 bit in the LSD is also made 1, but the 7 bit indicates the sign of the answer. All bits in A are left unchanged. The final states of the Condition FFs indicate the status of the answer in B'.

The hardware B register is counted up LB-1 times so that it addresses the LSD position of the B field. The LSD of the multiplier is read into the hardware K register and then the core location is made zero (01 0000). A and B registers are counted up LA more times. At each location in B' a zero is written into core.

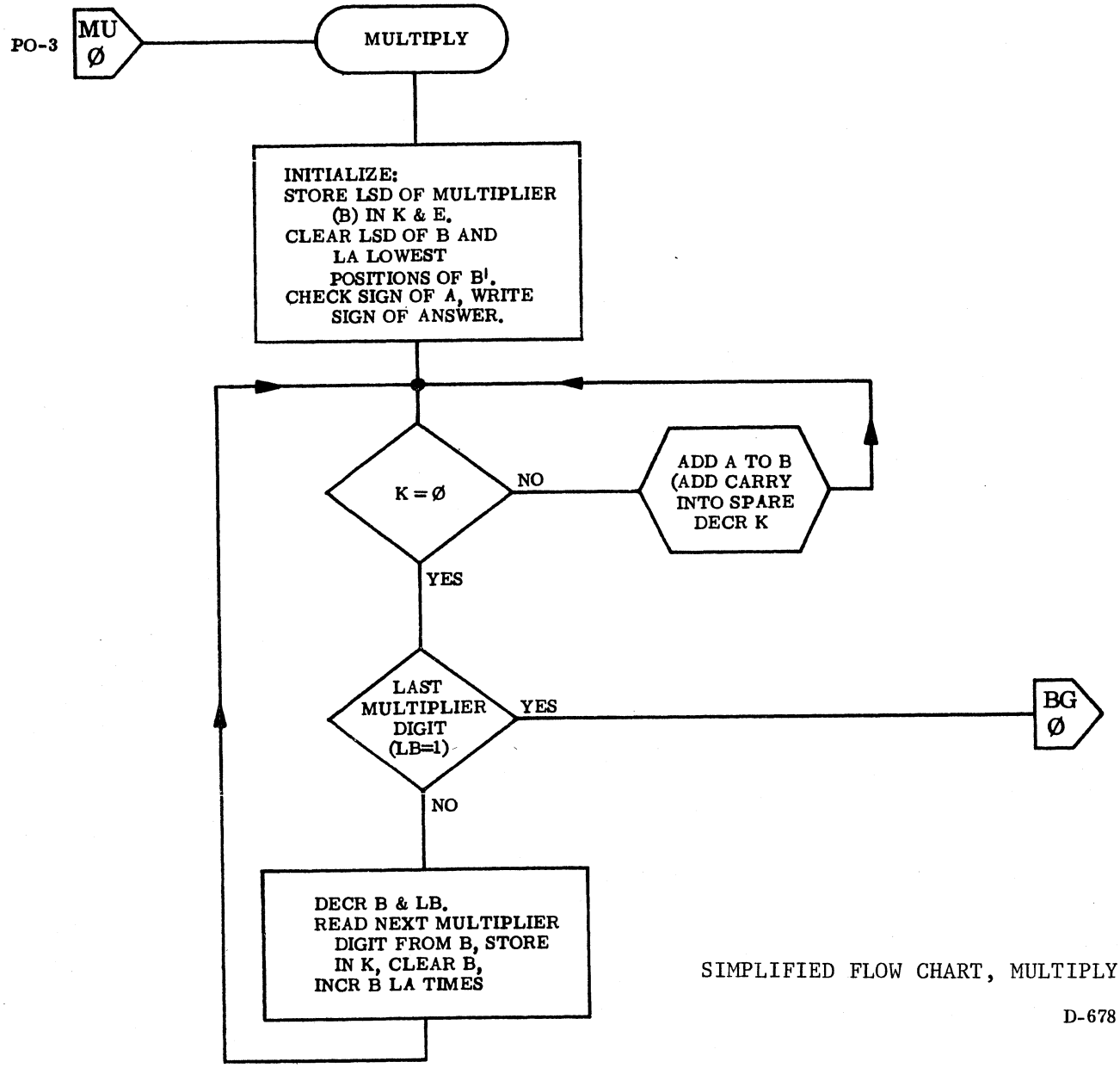
Example:	B = 1 2 3 4 (LB = 4) A = 2 6 (LA = 2)	
Following the above operations:	B' = 1 2 3 0 0 0 A = 2 6	K = 4
A is then added to B' K times:	B' = 1 2 3 1 0 4 A = 2 6	K = 0
The operation is repeated for the next digit of the multiplier	B' = 1 2 0 1 0 4 A = 2 6	K = 3
Then	B' = 1 2 0 8 8 4 A = 2 6	K = 0

3-5.6 MULTIPLY (Continued)

In all, K x A is added into the proper digits of B' a number of times equal to LB, once for each position in the original B Field, just as would be done with pencil and paper.

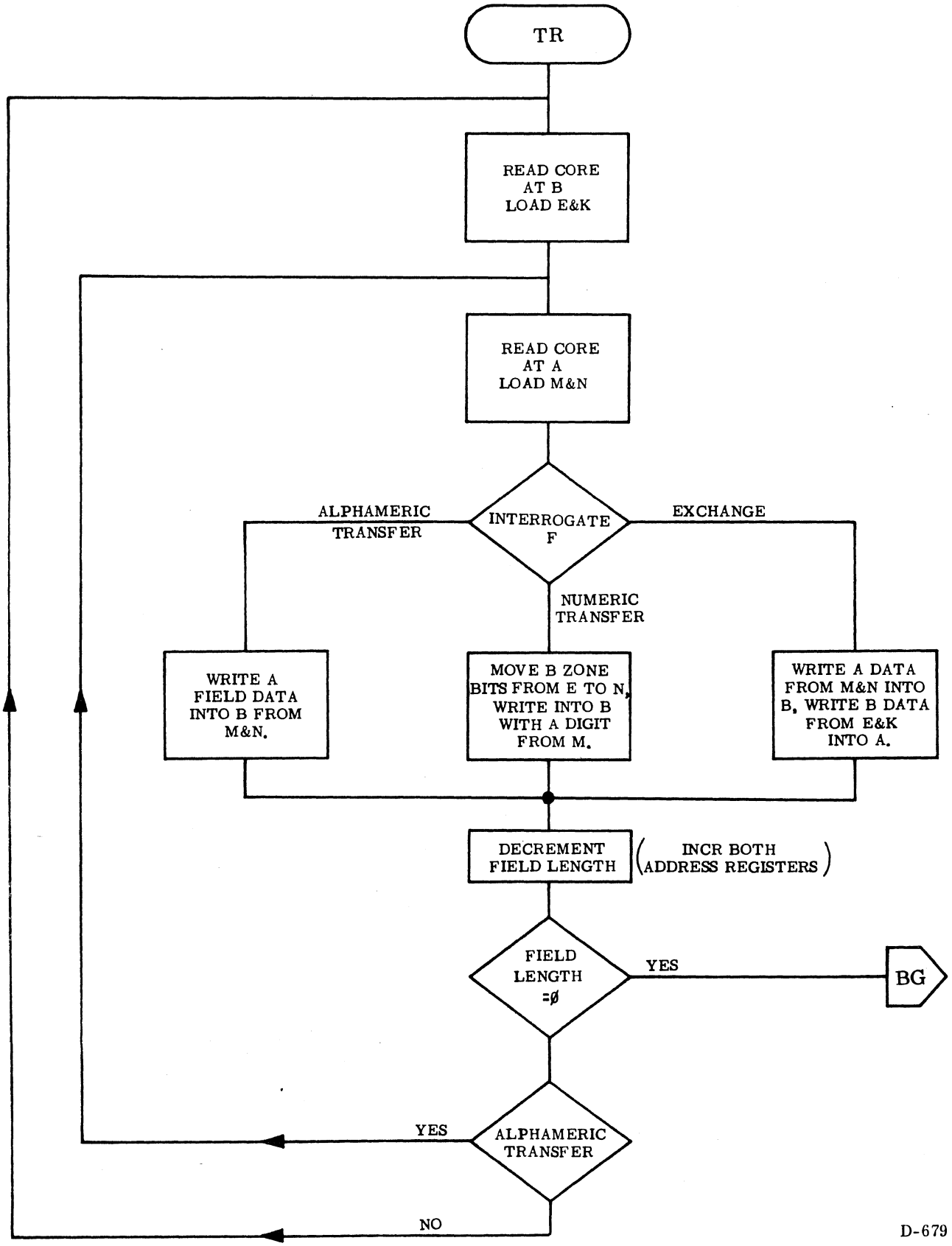
```
          2 6
x 1 2 3 4   (LB = 4)
    1 0 4
  0 7 8       LB = 4
  0 5 2
0 2 6
0 3 2 0 8 4
```

Notice how each digit of the multiplier is replaced by a zero, in turn, so that the overflow of K x A has a place to go. The length of the B'Field is arranged by the hardware so that there is no overflow condition following any multiply.



SIMPLIFIED FLOW CHART, MULTIPLY

D-678



FLOW CHART, TRANSFER

3-5.7 TRANSFER (08) MOVE NUMERIC (09) and EXCHANGE (15)

F = 1000/1001/1111
LA,LB = Length of field to be transferred, where LA is the 10's digit and LB is the units.
(Hence LA = 4, LB = 6 means field length = 46 ;
LA = 0, LB = 0 means field length = 100)
A = Address of MSD of A Field
B = Address of MSD position of B Field
AC = Mark that the A Address is in the Common Area
BC = Mark that the B Address is in the Common Area
IA,IB = Indicate Indexing

CONDITION CODES (STATUS). No condition FFs are affected.

OPERATION (see figure). The TRANSFER function is used by three different instructions--Transfer, Numeric Transfer, and Exchange.

(1) Transfer A→B. A Transfer instruction causes each character in the A Field to be duplicated into its corresponding position in the B Field, starting at the MSD and continuing under the control of LA and LB. The very first operation is to read core at B--this step is included in the TRANSFER function only for Numeric Transfer and Exchange, and it is not needed in normal Transfer.

Next the Main Memory is read at the A address, leaving the character in M and N. The B register is then used to address core, and the A-character is written into memory at the B address. Then the field length (in LA and LB) is decremented, and both address registers (A and B) are incremented. The entire process repeats for each character, until the field length is exhausted.

(2) Numeric Transfer A_n→B. During Numeric Transfer, each B Field character is read and stored in the E and K registers. Next, the A Field character is read into M and N, and the B-character zone bits are gated from E into N, replacing the A-character zone bits. Finally, the A-character numerics (in M) and the B-character zone bits (in N) are written into memory at B. Field length is decremented and both address registers are incremented, and the process is repeated.

(3) Exchange A⇄B. During Exchange, each B Field character is read and stored in E and K, just as in Numeric Transfer. Then all six bits of the A-character are read into M and N, the B Field is addressed, and the entire A-character is written into memory at B. Following this, the B-character is gated into M and N, from where it is written into memory at A. Field length is then decremented, the A and B registers are incremented, and the cycle is repeated until the field length is exhausted.

3-5.8 BRANCH (11)

F = 1011
LA = Branch variant that must be satisfied in order for the instruction count to be replaced by the A Address (by the B Address for LA = 6 or 7).
LB = Branch variant that must be satisfied in order for the instruction count to be replaced by the B Address (except for LA = 7).
A = A Address
B = B Address
AC = Mark that the A Address is in the Common Area.
BC = Mark that the B Address is in the Common Area.
IA,IB = (Ignored) Branch addresses are not indexed

CONDITION CODES (STATUS). Branch does not set any condition codes -- it reads them. It leaves the condition FFs unchanged, so one Branch instruction can follow another. A table is provided following this description that shows the relationship of machine status and branch variants.

OPERATION. There are basically two types of Branch instructions, 5-character and 10-character instructions. Two different 5-character branches can be contained within the regular 10-character instruction format.

In BEGIN, the first five characters of the instruction are fetched; both LA and LB hardware registers are loaded with the LA part of the instruction, and both A and B hardware registers are loaded with the A Address. If the condition indicated by the LB register matches the states of the Condition FFs (BR-OK), the instruction count in the P Register is replaced by the contents of the B Register.

If a branch is not made after the first five characters are fetched, the second five are pulled. Now only LB and B are loaded, and LB is tested again.

Regardless of the value of the LSD of the Branch address, P0 is set to 0 when P is loaded, so any branch that occurs will be to the start of an instruction.

After B has replaced P, the ACU will test for switch and timeout:

(1) If LB = 8, Jump to SWITCH

(2) If TIMEOUT, Jump to SWITCH

(3) If LB $\neq$ 8 and $\overline{\text{TIMEOUT}}$, Jump to BEGIN

3-5.8 BRANCH (Continued)

(1) 5-Character Branches. (A→P or B→P). A 5-character Branch may occur when either the LA or the LB portion of a regular 10-character instruction is equal to 1, 2, 3, 4, 5, or 8. See Figure 3-26. If LA or LB is equal to 0 or 9, that portion of the 10-character instruction is a no op (see exception under Branch if SVRQ).

(2) 10-Character Branches. If the LA portion of a Branch instruction is equal to either 6 (Branch and Transfer) or 7 (Branch if Service Request), all ten characters must be pulled before any branch can take place. The LB portion of an instruction does not normally contain a 6 or 7; no branch can occur to the B address if LB = 7, and LB = 6 allows only a "Branch if Service Request" to occur.

(a) Branch and Transfer (P→(A), B→P). If LA = 6, the LB condition must be met in the normal way. A successful Branch & Transfer results in the P Register count being stored in bits 1-4 of four consecutive core locations, starting at address A. The PC bit is transferred to the 7 bit, along with a "1" in the 5 bit, when the last transfer (P0, the LSD) is made; otherwise, the method of transfer, being the same as that used in Numeric Transfer, leaves the zone bits at A undisturbed. After the P→(A) transfer has occurred, the contents of the P Register are replaced by the contents of the B Register.

The LA = 6 logic does not affect the BR-OK logic: it simply enables the P→(A) transfer after the LB variant has determined that the branch may occur.

(b) Branch if Service Request (SVRQ). If LA = 7, the LB variant must not have any effect on whether or not the branch will occur; accordingly, LB must be programmed as a 0 or 9 and the branch will then occur only if there is a request for service by some peripheral device connected to the IOC.

A successful Branch if SVRQ causes the I.D. number of the requesting I/O device to be transferred from the buffer in the IOC to bits 1-4 at core location A. The mechanism is the same as Numeric Transfer, so the zone bits at A are not disturbed. Then the contents of the P Register are replaced by the contents of the B Register.

The LB = 1-5 logic that functions while the second half of a Branch instruction is being retrieved is not disabled by LA = 7 (Branch if SVRQ). Therefore a Branch if SVRQ instruction must specify LB as either a 0 or a 9 in order to prevent a branch when there is no Service Request. If LB is not a 0 or 9, a branch could occur, depending on LB and the Condition FFs, and a meaningless character will be transferred from the IOC to Main Memory.

3-5.8 BRANCH (Continued)

BRANCH MODIFIER (LA or LB in LB REG.)	CONDITION FFs			STATUS			
	ZERO	MINUS	CARRY	I/O*	ARITH or FNF	EDIT	COMPARE
1	0	1	-	ERROR or FAULT	MINUS	MINUS	LOW
2	1	-	-	NORMAL	ZERO	ZERO	EQUAL
3	0	0	-	FLAG	PLUS	PLUS	HIGH
4	-	-	1		OVERFLOW		
4	-	1	1	FAULT			
5	UNCONDITIONAL						
8	UNCOND. & SWITCH						
0,9	NO-OP						

*Normally, test for Branch modifier 1 precedes test for modifier 4.

5-CHARACTER INSTRUCTIONS

10-CHARACTER INSTRUCTIONS

$\overline{6}$ $\overline{7}$	BR & TRANSFER IF LB	(LA = 6)
0,6,9	BR IF SVRQ	(LA = 7)

BRANCH VARIANT CHART

3-5.9 EDIT (12)

F = 1100
LA,LB = Length of field to be edited, where LA is the ten's digit and LB is the unit's. (Hence LA = 4, LB = 6 means field length = 46; LA = 0, LB = 0 means field length = 100).
A = Address of MSD of field to be edited.
B = Address of MSD position of field that contains the editing mask and to which (A) will be transferred.
AC = Mark that the A Address is in the Common Area
BC = Mark that the B Address is in the Common Area
IA,IB = Indicate Indexing

CONDITION CODES (STATUS). Numbers indicate BRANCH variants.

(1) MINUS (and non-zero)

(2) ZERO

(3) PLUS (and non-zero)

		ZERO	MINUS	CARRY
(1)	MINUS	0	1	-
(2)	ZERO	1	-	-
(3)	PLUS	0	0	-

The Condition FFs tell whether the edited data is positive, negative, or all zeros. Every digit is checked, and a negative sign (7 bit) in any digit will cause MINUS to set. Likewise, any non-zero digit will cause ZERO to reset.

When the data is either zero or positive, the hardware automatically converts the memory position immediately following the location in B where the last digit from A was written to a blank. When the data is negative, this last mask character remains unchanged. (If a Minus sign is desired, it must initially be made a part of the mask.) This "extra" character used by the Edit instruction must be taken into consideration when memory assignments are being made: fields cannot be contiguous, but must have a "space" between them.

3-5.9 EDIT (Continued)

OPERATION, A→B, UNDER CONTROL OF B. The B Field is the editing mask and final resting place for the edited data. The original A Field is left as it was (unless fields overlap).

Starting at the MSD positions of A and B, the contents of A are transferred to B under control of the symbols in B (see chart). A is assumed to contain only the digits 0 through 9: the only hardware test of the A data is to determine the first non-zero digit. When data is written from A to B, the zone bits are made 0,1.

The first non-zero digit in A is the "first significant digit". All digits to the left are "non-significant", and all digits to the right are "significant". Significance is also established by a Zero (01 0000) in the B mask, regardless of the contents of A. Non-significant digits are not transferred to B. The instruction is terminated only after all digits in A have been transferred to B.

CHART OF MASK CHARACTERS

If the digit in B is	And no Signif, (B) becomes	And Signif, (B) becomes
@	¢	¢
ZERO	numeric equiv of (A)	numeric equiv of (A)
,./-	previous (B)*	(left alone)
all other	(left alone)	numeric equiv of (A)

*Unpredictable until one of the other conditions in this chart has been encountered, causing "previous (B)" to be defined.

CHART OF MASK CHARACTERS

FIGURE 3-27

Example:
A = 0123456789P
B = $¢¢,¢¢¢,¢¢0.00- (Mask)
B = $12,345,678.90- (After execution)

Example:
A = 111069
B = 00-00-00 (Mask)
B = 11-10-69¢ (After execution)

Example:
A = 5678
B = $0.00- (Mask)
B = 56.78¢ (After execution)

Example:
A = 00004000V0001234
B = ¢,¢¢¢,¢¢¢,¢¢¢,¢¢0.00@- (Mask)
B = ¢¢¢¢¢¢400,060,001.23¢¢ (After execution)

3-5.10 FORM NUMERIC FIELD (13)

F = 1101
LA = Length of A Field
LA = 0 through 9, where LA = 0 indicates a length of 10
LB = Length of B Field
LB = 0 through 9, where LB = 0 indicates a length of 10
LB ≥ number of numerics in A
A = Address of MSD of A Field
B = Address of MSD of B Field
AC = Mark that the A Address is in the Common Area
BC = Mark that the B Address is in the Common Area
IA,IB = Indicate Indexing

CONDITION CODES (STATUS). Numbers indicate BRANCH variants.

(1) MINUS (and non-zero)

(2) ZERO

(3) PLUS (and non-zero)

(4) OVERFLOW

		ZERO	MINUS	CARRY
(1)	MINUS	0	1	-
(2)	ZERO	1	-	-
(3)	PLUS	0	0	-
(4)	OVERFLOW	-	-	1

3-5.10 FORM NUMERIC FIELD (Continued)

OPERATION A→B (numerics only). FORM NUMERIC FIELD is somewhat the inverse of EDIT. A is read from right to left (LSD first) and only the numerics 0-9 (01 0000 - 01 1001) are extracted from the alpha-numeric A Field and transferred to the B Field, with one exception.

The exception occurs in the LSD: in this case, negative digits (P through Y = -0 through -9) are also transferred to B. The first non-blank character, no matter what it is, determines the sign of B. P through Y, or the Minus sign (00 1101), will all cause the sign of B to be negative, but only P-Y will be written into B. Any other non-blank will cause B to be positive, but only the digits 0-9 will be written into B. This is summarized in the chart below. Blanks are ignored.

First non-blank character	Character written into B	MINUS FF
0-9	0-9	Remains reset
P-Y	P-Y	Sets
Minus sign	Nothing written (Preset 7 bit)	Sets
Any other	Nothing written	Remains reset

After the first non-blank, only the digits 0-9 (not P-Y) are transferred to B. All other characters (including blanks) are ignored.

If all numerics in A are transferred before the B Field is filled, the remaining MSD positions of B are filled with zeros. If, on the other hand, the B Field is filled before all numerics in A are transferred, OVERFLOW is set.

Example: A = $5,128.53- (LA = 10)
B = 000051285S (LB = 10)

Example: A = 12AB3C4D (LA = 8)
B = 00001234 (LB = 8)

Example: A = 32XY413P (LA = 8)
B = 32413P (LB = 6)

Example: A = 12345678 (LA = 8)
B = 345678 (LB = 6)
(OVERFLOW)

3-5.11 COMPARE (14)

F = 1110
LA,LB = Length of the fields to be compared, where LA is the ten's digit and LB is the unit's. The fields are the same length. (For example, LA = 4, LB = 6 means both fields are 46 characters long; LA = 0, LB = 0 indicates length = 100.)
A = Address of MSD of field to be compared
B = Address of MSD of reference field
AC = Mark that the A Address is in the Common Area
BC = Mark that the B Address is in the Common Area
IA,IB = Indicate Indexing

CONDITION CODES (STATUS). Numbers indicate BRANCH variants.

(1) LOW
(A) < (B)

(2) EQUAL
(A) = (B)

(3) HIGH
(A) > (B)

		ZERO	MINUS	CARRY
(1)	LOW	0	1	-
(2)	EQUAL	1	-	-
(3)	HIGH	0	0	-

3-5.11 COMPARE (Continued)

OPERATION A : B (Six bits). The contents of A are compared to the contents of B by subtracting each character in B from its corresponding character in A. The ACU always does a "machine subtract", starting at the MSD and continuing under control of LA and LB or until a pair of unequal characters are detected. The contents of A and B remain unchanged: the only result of the Compare function (instruction) is the setting of the proper status indicators.

The SUBTRACT and CARRY flip-flops are preset to start. Then each A character is read and set into H (numeric bits) and E (zone bits). Next the corresponding B character is read and its numeric bits are set into D. The zone bits remain in N for the comparison.

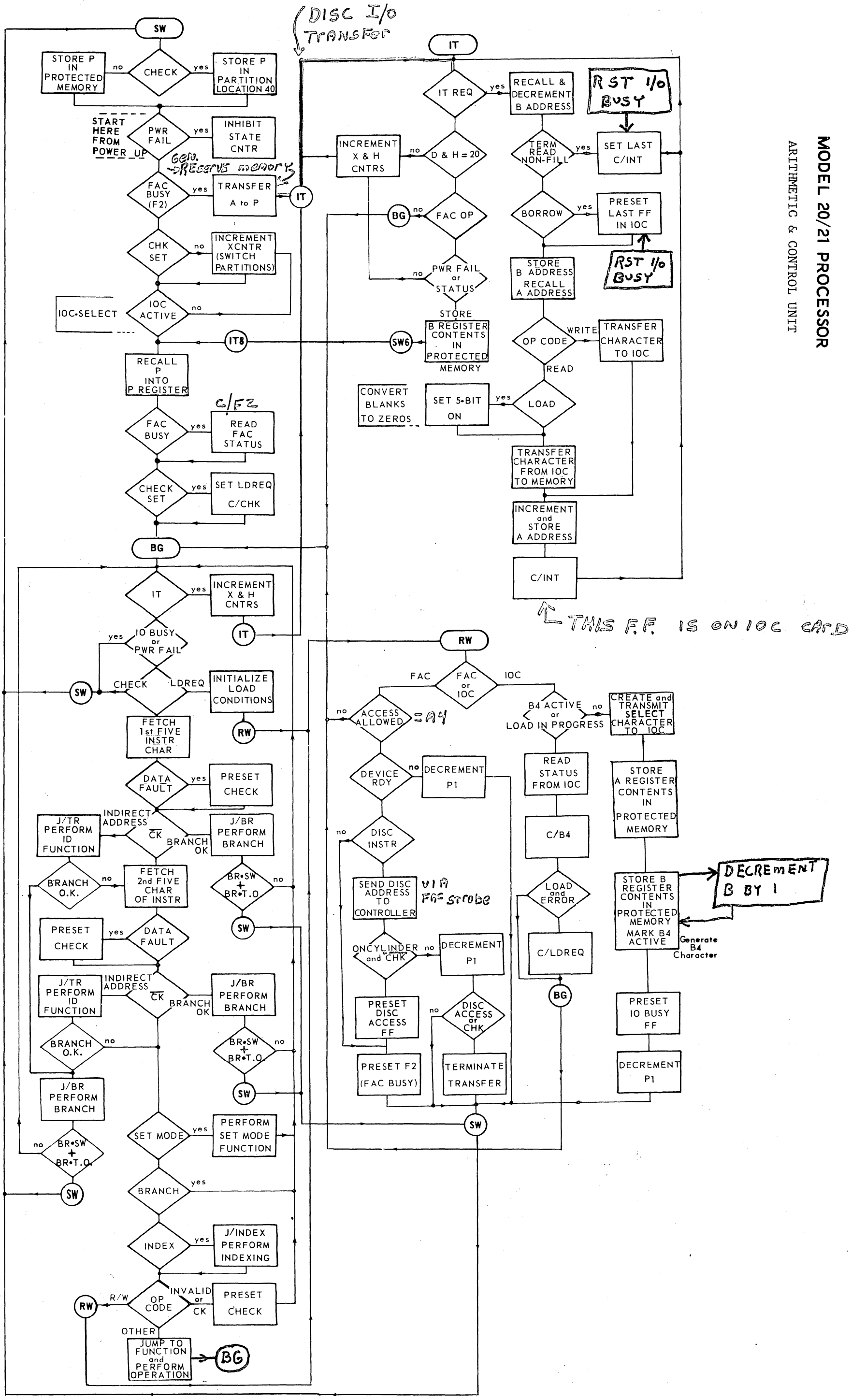
The numeric bits are compared by adding (H) (A digit) to the 15's complement of (D) (B digit) in the same 1st adder used for math functions (the correction is disabled since the output of the second adder is not used). The zone bits are compared in a group of gates used solely for this purpose. This group of gates not only blocks COMP-EQ when the zone bits are not alike, but also determines which digit has the greater binary value. If the A digit is greater, CARRY remains set: if the B digit is greater, CARRY resets, which causes MINUS to set.

If the two characters compare, COMP-EQ remains true, the field length (in LA and LB) is decremented, the A and B addresses are incremented, and the operation repeats. As long as COMP-EQ remains true, the cycle repeats until all characters have been compared. If both fields contain identical data, ZERO and CARRY both remain set and the ACU jumps to BEGIN.

If two characters do not compare, ZERO is reset and either CARRY or MINUS is set. The function is terminated immediately, and the ACU jumps to BEGIN.

Examples:	ZERO	MINUS	CARRY	CONDITION
A = 11P B = 119	0	0	(1)	HIGH
A = 000012GHJPQRSTZ4 B = 000012GHJPQRSTZ4	1	(0)	(1)	EQUAL
A = 000A9SH B = 000B000	0	1	(0)	LOW
A = 0098765 B = 0B00000	0	1	(0)	LOW

Parentheses (1) denotes conditions not tested by BR-OK logic.


SW
STORE P IN PROTECTED MEMORY
no
CHECK
yes
STORE P IN PARTITION LOCATION 40
START HERE FROM POWER UP
PWR FAIL
yes
INHIBIT STATE CNTR
Gen. Reserve memory
FAC BUSY (F2)
yes
TRANSFER A to P
IT
CHK SET
no
INCREMENT XCNTR (SWITCH PARTITIONS)
IOC-SELECT
IOC ACTIVE
no
IT8
RECALL P INTO P REGISTER
C/F2
FAC BUSY
yes
READ FAC STATUS
CHECK SET
yes
SET LDREQ C/CHK
BG
IT
yes
INCREMENT X & H CNTRS
IT
yes
IO BUSY or PWR FAIL
CHECK
LDREQ
SW
INITIALIZE LOAD CONDITIONS
RW
FETCH 1st FIVE INSTR CHAR
DATA FAULT
yes
PRESET CHECK
INDIRECT ADDRESS
CK
BRANCH OK
J/TR PERFORM ID FUNCTION
J/BR PERFORM BRANCH
BRANCH O.K.
no
FETCH 2nd FIVE CHAR OF INSTR
BR•SW + BR•T.O
no
SW
PRESET CHECK
yes
DATA FAULT
INDIRECT ADDRESS
CK
BRANCH OK
J/TR PERFORM ID FUNCTION
J/BR PERFORM BRANCH
BRANCH O.K.
no
BR•SW + BR•T.O.
no
SW
J/BR PERFORM BRANCH
BR•SW + BR•T.O.
no
SW
SET MODE
yes
PERFORM SET MODE FUNCTION
BRANCH
yes
INDEX
yes
J/INDEX PERFORM INDEXING
RW
R/W
OP CODE
INVALID or CK
PRESET CHECK
OTHER
JUMP TO FUNCTION and PERFORM OPERATION
BG
DISC I/O TRANSFER
IT
IT REQ
yes
RECALL & DECREMENT B ADDRESS
RST 1/O BUSY
INCREMENT X & H CNTRS
no
D & H = 20
TERM READ NON-FILL
yes
SET LAST C/INT
BG
no
FAC OP
BORROW
yes
PRESET LAST FF IN IOC
no
PWR FAIL or STATUS
STORE B ADDRESS RECALL A ADDRESS
RST 1/O BUSY
STORE B REGISTER CONTENTS IN PROTECTED MEMORY
SW6
OP CODE
WRITE
TRANSFER CHARACTER TO IOC
READ
CONVERT BLANKS TO ZEROS
SET 5-BIT ON
yes
LOAD
TRANSFER CHARACTER FROM IOC TO MEMORY
INCREMENT and STORE A ADDRESS
C/INT
THIS F.F. IS ON IOC CARD
RW
FAC
FAC or IOC
IOC
no
ACCESS ALLOWED
=A4
B4 ACTIVE or LOAD IN PROGRESS
no
CREATE and TRANSMIT SELECT CHARACTER TO IOC
DEVICE RDY
no
DECREMENT P1
READ STATUS FROM IOC
STORE A REGISTER CONTENTS IN PROTECTED MEMORY
no
DISC INSTR
C/B4
SEND DISC ADDRESS TO CONTROLLER
VIA F&S Strobe
LOAD and ERROR
STORE B REGISTER CONTENTS IN PROTECTED MEMORY MARK B4 ACTIVE
DECREMENT B BY 1
Generate B4 Character
CYLINDER and CHK
no
DECREMENT P1
C/LDREQ
BG
PRESET DISC ACCESS FF
DISC ACCESS or CHK
no
PRESET IO BUSY FF
PRESET F2 (FAC BUSY)
TERMINATE TRANSFER
DECREMENT P1
SW

SECTION 4

CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

TABLES

4-1.0 INTRODUCTION

The multi-terminal IOC (MT IOC), and associated line units coordinate communication between the ACU and any one of a maximum of ten peripheral devices. Any peripheral devices that interface to a line unit can be parallel connected to one of the two-wire lines that are the entry/exit circuit to the MT IOC. However, the maximum of ten line units cannot be exceeded for any one MT IOC. For simplification, further reference to the MT IOC in this section will be shortened to IOC.

When the IOC is not active with an instruction, each peripheral is selected in turn, and interrogated for a service request. Between service request inquiries, the device designated as zero (usually a workstation) is querried for a load request. In this way any peripheral can request communication, and device zero can request to load new program.

The arithmetic and control unit (ACU) can initiate an instruction in the form of a select character, to any individual peripheral device. To do this, the device number is included in the select character, and is responded to only by the device that has that number designation. Device designations are mechanical settings of switches or jumpers, and must be coordinated with the software program at the time of installation.

Parallel data bits from the ACU are converted to bit-serial characters, and transmitted over a two-wire line to all line units (line units sharing the same IOC are parallel connected).

The IOC and line unit are very similar in design and operation. They operate in four basic modes: read, write, select, and escape. Operation is sequenced by 16 states (Ø through 15), that much of the time, are clocked simultaneously in the line unit and IOC. A processor WRITE instruction causes the IOC to transmit, and the selected line unit to receive. A processor READ instruction causes the IOC to select a particular line unit; then receive the data that the line unit transmits.

The MT IOC consists of two printed circuit cards, CH1 and CH2, and occupies two adjacent card slots in the model 20 processor. The line unit is considered a part of the peripheral, and derives its power from the peripheral power supply. The IOC can be thought of as a "master", and the line unit as a "slave" that are connected by a two-wire transmission line.

4-2.0 DATA FORMAT

Data transmission between the MT IOC and peripherals is bit serial, and asynchronous by character. Each character contains a start bit, seven ASCII character bits, and two parity check bits. Bits are recognized by the time relationship to the starting pulse. Transmission line polarity is reversed to indicate the beginning and end of each bit time (sometimes referred to as "clock" time). Within a character, the end of one bit is the beginning of the next. A bit time with a transition (polarity reversal) at the beginning and end is a zero bit. A bit time with an additional transition at mid-bit, is a 1 bit. Instantaneous polarity (that is to say, the dc voltage) is only important in that it detects a reversal transition.

Figure 4-1 shows a sample of an IOC/line unit exchange, as seen on an ocilloscope. The ocilloscope, in this case was connected directly to the line terminals at the processor end of the two-wire line. The characters that are shown are deletes (all 1s) sent by the line unit, and answered by two acks from the IOC. This exchange is normal during a READ instruction, if the device is a workstation or other slow operating device.

Notice that the IOC transmissions are offset in voltage from the line unit transmissions. The IOC drives the line (ST.NEG.) away from zero, or allows it to return for each transition, while the line unit is transformer coupled, and swings the line voltage away from a floating value. Figure 4-2 is an idealized example of a few characters to show the relationship of transitions to the character bit structure. In normal reference, the voltage transitions that occur at TØ are called clocks, and the mid-bit transitions are called data transitions.

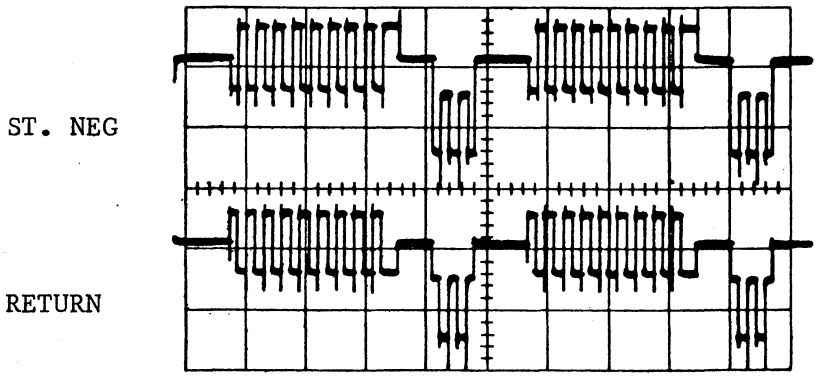


Figure 4-1 DATA EXCHANGE

MT IOC & LINE UNIT

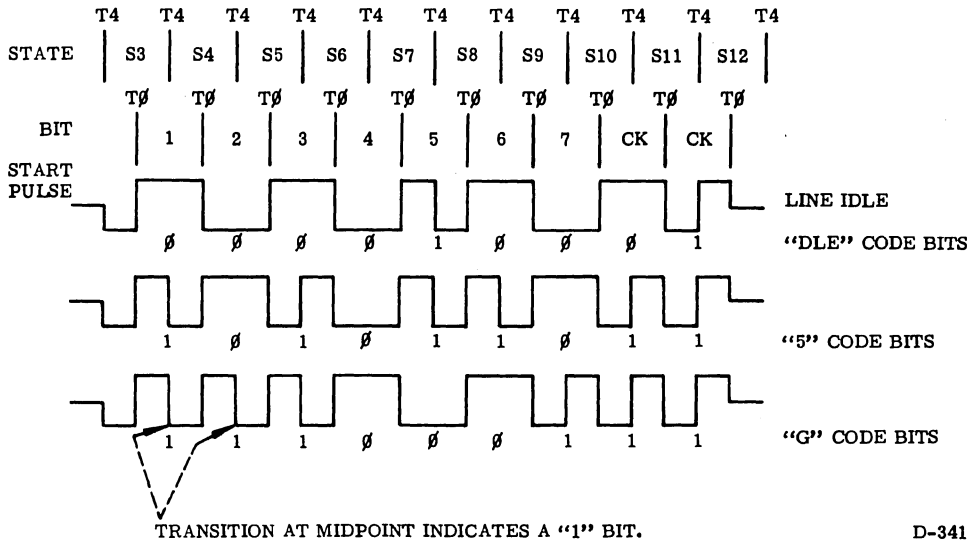


Figure 4-2 DATA TRANSMISSIONS

4-2.1 DATA TRANSFER

Figure 4-3 shows a typical exchange between the IOC and line unit. The sequence of events shown in the example are as follows:

- The IOC sends a DLE code onto the line (1), setting the SELECT flip-flop in all connected line units.
- Four bit times later, the IOC sends a "select" character (2) that contains the device number that is desired, and the "instruction", or operation to be performed. In the example the select character is from a READ instruction that originated in the software program.
- The selected device furnishes the "DEVICE ON" signal to the line unit, and the line unit acknowledges the IOC transmission with two 1s (3).
- The line unit requests data from the peripheral, and if a character is not present soon enough, the line unit sends a DELETE code to fill time (4).
- The received character is checked for parity and the proper number of bits. The IOC acks with two 1s. If for some reason, the receiving register can not be emptied soon enough, the 1s are repeated until the register is clear. This holds off any additional characters that might be ready for transmission at the other end. The continous 1s are called busy bits (5).

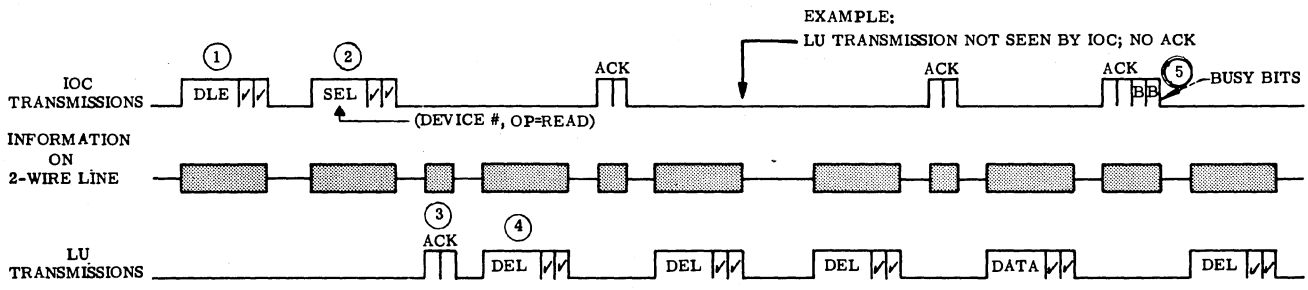


Figure 4-3 IOC/LINE UNIT TRANSMISSIONS

4-3.0 POLLING & SELECTION

The MT IOC memory partition within the processor can operate under any of the legal processor instructions. However, because the MT IOC is an input/output (I/O) device, data can also be transmitted and received, to and from line unit peripherals. All I/O instructions are given to the IOC in the form of an I/O select character. The IOC receives the select character, sets the necessary hardware into action, and re-transmits the select character to the line unit. When no instruction is present from the ACU, the IOC generates two similar characters (one at a time) that are used as polling questions. The illustration below (figure 4-4) shows a graphic diagram of the select character. The first four columns of the figure show the possible variations of the select character as it is received from the ACU. The last two columns show the two polling questions that are hardware generated by the IOC.

The line unit cannot initiate communication, although an operator originated service request or load request will appear to be answered immediately. During polling, the IOC issues an invitation for service, and alternately invites device zero to indicate a load request. If either of these requests are present in the device, the line unit acknowledges the invitation; otherwise no acknowledgement is made. The acknowledging device will be selected and given the proper instruction in the form of a select character.

For the following discussion, the term "polling" is considered the invitational questions mentioned above, even though selection is a part of the polling operation. Selection, on the other hand, refers to an operation that is given to the line unit because of a software instruction, even though the instruction may have been fetched because of a service request.

Whether polling or selecting, a data link escape (DLE) is sent onto the line by the IOC, setting all SELECT flip-flops in the connected line units. A select character is then sent to all units, and the number is compared internally by the peripheral logic. The device in which the number agrees is the selected device, and it responds with an acknowledgement. A non-response of the polling questions is a NO answer to the polling question.

An afirmative response to the service request question sets the SVRQ flip-flop in the IOC. The ACU detects the SVRQ signal, and if the software contains a branch on service request instruction, a branch is made. If no branch is present, the request will go unheeded.

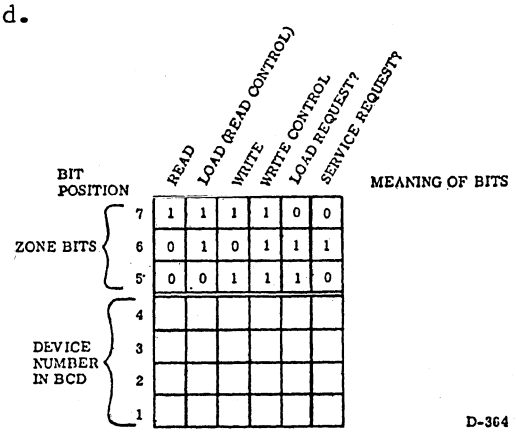


Figure 4-4 SELECT CHARACTER

4-3.1 POLL COUNTER

The poll counter specifies the device number to which a service request poll is made. The output of the decimal poll counter is sequentially gated onto the WRITE-INFO line during transmission of the select character that is sent to the line unit. The poll counter is incremented before each service request poll, and held if the poll is acknowledged. However alternate polls are to device zero for a load request inquiry; these are not controlled by the poll counter, but are forced by the LOAD flip-flop. The LOAD flip-flop is toggled to alternate states with each polling transmission.

During polling, the output of the poll counter is gated onto the OUT-DATA lines, and consequently onto the S bus. If the polling inquiry is acknowledged, the number from the poll counter is available for software use.

4-3.2 RETRIAL

An ACU generated select character (instruction) that is not answered within approximately three bit times is re-transmitted by the IOC. The first RETRIAL (repeated transmission) starts a timeout sequence that allows the select character to be transmitted about 15 times before the IOC times out in FAULT status. A normal data character that is not acknowledged will be repeated approximately 35 times before the IOC times out from lack of response. The difference is not in the timing, but selection requires a two-character transmission (DLE, then the select character). During polling, the IOC generated character is not re-transmitted.

4-3.3 TIMEOUT

Both the IOC and line unit contain timeout circuits. If the timeout is allowed to complete, the TIMEOUT flip-flop will be toggled at the next T3 time (T4 time in the line unit). The IOC will timeout from lack of selection response (as explained above) or from lack of character acknowledgement from the line unit during a READ instruction. The line unit times out in similar circumstances. It too retries data transmissions if there is no response from the IOC. The line unit will also timeout if the attached device is inoperative, and does not respond.

Line unit timeout causes a jump to the ESCAPE mode. And since the line unit can not transmit in ESCAPE, the IOC times out from lack of response (acknowledgements) from its transmissions to the line unit. Once timeout has occurred, the line unit must be selected again for communication to continue.

IOC timeout also causes a jump to the ESCAPE mode, where the instruction is completed in one of three ways, and FAULT status is posted. If a WRITE instruction is in progress, the INTerrupt flip-flop is held set, and the characters that are received from the ACU are not sent to the line unit. This causes a quick run-out of the instruction character count. If timeout occurs during a READ instruction, the IOC sends the TERM-READ signal to the ACU, holds the INTerrupt flip-flop set, and inhibits the IOS-TO-MN (the data shift to the processor). If the instruction contains a non-fill bit (LB=5), the ACU sets LAST in the IOC, that initiates status retrieval without filling the alloted data field. If the instruction does not contain the non-fill bit, the remainder of the character count is filled with blanks. If the instruction was a READ CONTROL, and the non-fill bit is not present, the field is filled, but the blanks are converted by ACU hardware to zeros.

4-3.3 TIMEOUT (Continued)

The peripheral will usually be much slower than the IOC logic response, and provision is made to prevent timeout between characters. Once the instruction is in progress, fill bits, or characters are used to prevent timeout. During a WRITE exchange, a character is sent to the line unit, and is held ready until the peripheral device accepts it. While the line unit is waiting for the character to be accepted by the peripheral, it sends a continuous series of one bits. The first two one bits are considered by the IOC as acknowledgement, and the following (busy) bits hold off the transmission of the next character, and also prevent the timeout circuits from completing. In a similar situation during READ, the line unit sends a DELete character (seven 1s, and two check bits that are also 1s). The delete character is acknowledged by the IOC with two one bits. This exchange may occur many times between data characters, if the peripheral is hand operated, such as a workstation, etc.

4-3.4 LOCKOUT

Special consideration is given to prevent monopolization of the IOC by any one peripheral device. After each I/O operation, the LOCKOUT flip-flop is set in the IOC, preventing immediate re-access to the same device. The IOC must poll device zero for a load request, and one device (whatever number is in the poll counter) for a service request, before LOCKOUT is reset. If the preceding I/O operation was initiated by a branch on service request, the poll counter will have incremented one count, and must circulate through every other number before returning to the same device. However if the previous I/O operation was initiated by the software program, the poll counter will continue from the number that was ready to be polled when the instruction arrived.

LOCKOUT is set initially, upon power up after power failure, and by system reset.

4-4.0 IOC & LINE UNIT TIMING

Logic sequencing in the IOC and line unit is coordinated by signals from the time counter and state counter that are contained in each unit. The time and state counter circuits in the IOC are nearly identical to those of the line unit. However, the frequency source for the two units is different. IOC timing is normally driven by the IOC-HF-CLK signal from the ACU, and can be optionally patched for low speed operation that is driven by the IOC-LF-CLK signal. The coresponding frequency in the line unit is generated by a self-contained 450Khz crystal oscillator. If low frequency operation is desired in the line unit, the oscillator output is channeled through a counter that is configured to act as a frequency devider. Simultaneous low speed, and high speed operation is not compatible among devices connected to the same IOC. All peripherals must be patched to operate at the frequency of the IOC.

4-4.1 TIME COUNTER

The time counter is capable of counting to a binary 15, but all counts above 7 are used only as a time delay. Time counts 0, 1, 3, 4, 5, 6, and 7 are decoded and used by the IOC and line unit logic for gating and sequencing. Normally, the counter increments to 7, and is then reset. However, during states 2, 12, and 13, normal counting is interrupted or modified. The special counts for these states are given below.

- S2: During READ for the IOC or WRITE for the line unit, the counter increments toward a binary 15, but is reset if a clock (line transition) is received. (The line transition would be the beginning of a received transmission)

- S2: For the IOC during WRITE, the count is modified. Although the counter input is triggered, it is held reset, repeating TØ, until the INTerrupt flip-flop is reset by the ACU.

- S12: The counter increments to 15, and around to zero, providing a time delay.

- S13: Counts toward a binary 15, but may be reset by a clock (line transition) on the two-wire line at any time after T5 for the line unit or T7 for the IOC, and before the completed count of 15.

- S15: During READ, the line unit counter counts around to Ø, and can reset at T7 or T4.

Figure 4-5 shows the timing relationship of the various parts of the time counter. Notice that the X flip-flop gates the time decoder, causing an equal "dead" time between T times. The illustration also shows the state counter and the associated decoders. Transitions between states are also gated by the X flip-flop, producing a "dead" T-time between the state counts.

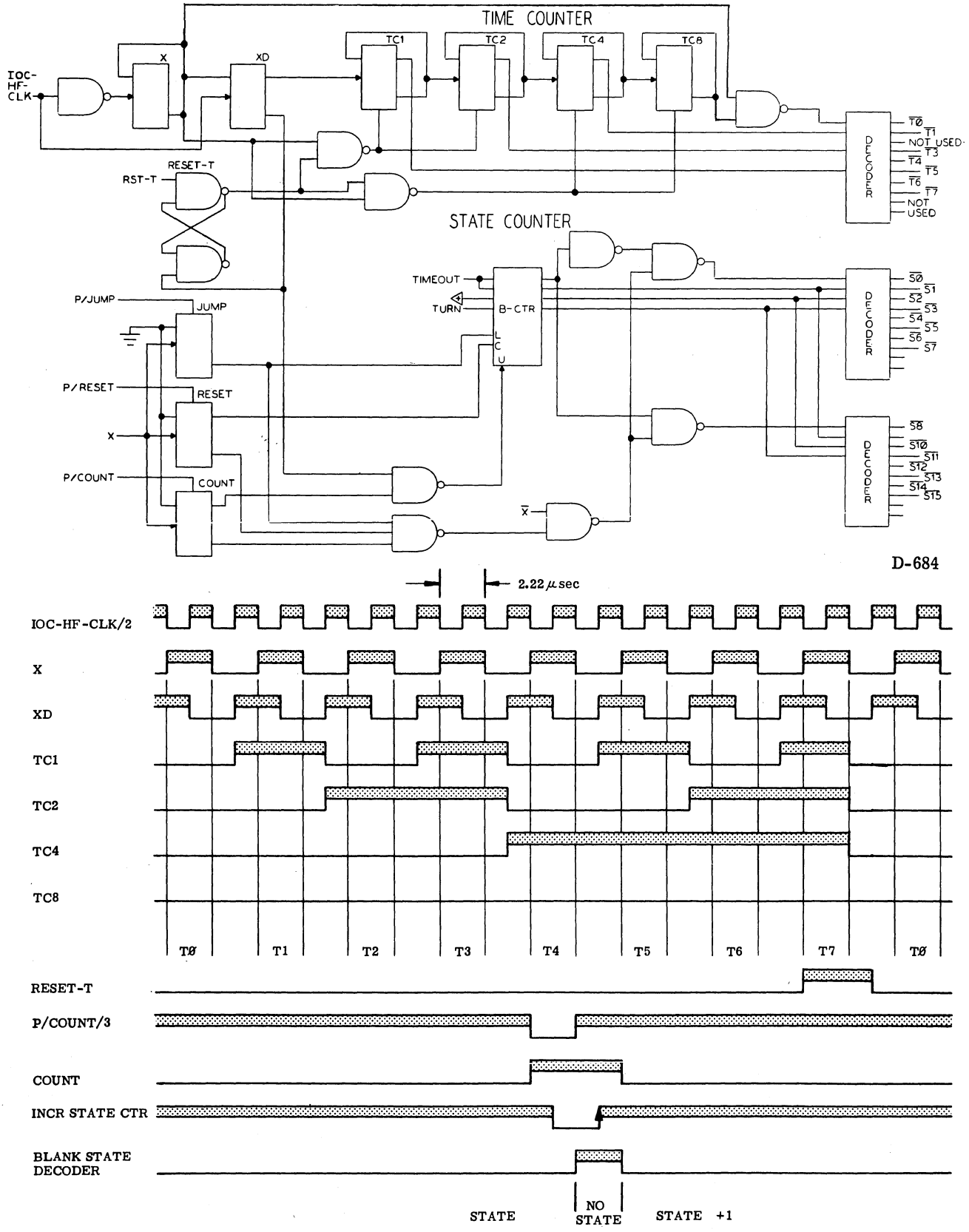


Figure 4-5. BASIC IOC TIMING

4-4.2 STATE COUNTER

The state counter normally increments each T4 time. However, certain logic conditions and decisions can force the IOC or line unit to jump states, or reset the state counter to zero. Table 4-1 lists the states, and the time within the state that the counter may jump, reset, or increment normally. The times listed in the table are the only times that these actions can take place.

Line unit and IOC states reflect similar use in escape, and nearly opposite uses in select, read, and write. Tables 4-2 and 4-3 show (in summary form) the use of the states in the line unit and the IOC.

Table 4-1. STATE CHANGES

LINE UNIT STATE	IOC STATE	JUMP	RESET	COUNT
S0	S0			T4
S1	S1		T4	T4
S2 WRITE (receive)	S2: READ			ANY**
S2 READ (send)	S2: WRITE			T0
S3 through S11	S3 through S11		T4	T4
	S12	T7	T4	T4
	S13,S14	T4	T3	T4
	S15	T0	T7	T3
S12		T4	T4	T4
S13,S14			T3	T4
S15		T4	T7	T3,T4*

* T4 is for line unit only
**Resets time counter with first clock transition
Count state at the first T4 following TCTR reset

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4-4.3 SYNCHRONIZATION

Bit recognition within incomming data is time dependent, requiring the transmitter and receiver to be synchronized. Both the IOC and line unit are timed by similar frequency sources, but small circuit differences, or temperature, may vary from one unit to the next. Because of this, the beginning of each transmission re-synchronizes the receiver with the incomming data.

While rough synchronization is achieved in SØ, as the transmitting end waits for the line to be quiet, the precision timing synchronization is accomplished in state 2.

In S2 the state counter of the receiver is disabled because the P/COUNT signal is held until the first clock transition appears on the line. When the clock transition occurs, the time counter is reset, releasing the LATCH flip-flop that has been holding the state counter. The simultaneous release of the state counter,

Table 4-2. IOC STATES AND FUNCTIONS

	ESCAPE	SELECT	WRITE	READ
SØ	Wait for incomming "busy bits"	Not Used	Wait for incomming "busy bits", etc. to stop.	
S1	Make sure line is quiet		Make sure line is quiet.	
S2	Idle	Check for type of sel.char. (ldrq, svrq,or ACU sel.	Wait for ACU to give next char. (INTERR)	Wait for 1st clock, sync timing to incomming data.
S3 to S9	Transmit DLE to all line units	Transmit I/O sel. char. to all LUs.	Transmit data char. to selected LU.	Receive data char. from selected LU.
S10 S11	Transmit check Ø and check 1.	Transmit two check bits		Receive two check bits.
S12		Idle		Wait for no clock.
S13 S14	Jump to SELECT "Run out instr.	Wait for first ack 1 Receive second ack 1		Transmit 1st ack 1. Set INTERR, xmit 2nd ack, wait for INTERR.
S15	Reset to start	Jump to ESCAPE,READ or WRITE.	Test for LAST, set INTERR	Idle

Table 4-3. LINE UNIT STATES AND FUNCTIONS

	ESCAPE	SELECT	WRITE	READ
SØ	Wait for incomming data to stop.	Not Used	Monitor for status request. Wait for incomming data to stop.	
S1	Make sure line is quiet.		Make sure line is quiet.	
S2	Wait for 1st clock, sync to incomming data.			Request data from peripheral unit.
S3 to S9	Shift all received codes into LS	Shift I/O sel. char. into LS.	Shift data char. into LS.	Transmit data char. to IOC.
S10 S11	Receive two check bits, check parity.			Transmit check bits
S12	Check parity, check for DLE.	Check parity, compare device# check for ldreq or svrq.	Check parity	Idle
S13	Not Used	Transmit 1st ack 1		Wait for 1st ack
S14		Transmit 2nd ack.	Transmit 2nd ack, sen data to peripheral.	Receive 2nd ack.
S15		Jump to ESCAPE, READ, or WRITE, reset STATUS.	Test for EOT.	Monitor for zeros.

4-4.3 SYNCHRONIZATION (Continued)

and the resetting of the time counter synchronizes the receiving logic with the incomming clock transition. The character length, being relatively short, assures that synchronization will remain well within tolerance for the time needed. Each new character re-synchronizes the logic.

4-5.0 READ/WRITE LOGIC

4-5.1 IOC WRITE & LINE UNIT READ LOGIC

Line transitions during data transmissions are generated by a D type flip-flop, feeding one line driver amplifier for each of the two sets of transmission lines. A simplified diagram of the transmission components is shown in figure 4-6. The line unit and IOC differ in that the IOC directly drives the transmission line, while the line unit is transformer coupled to the transmission line.

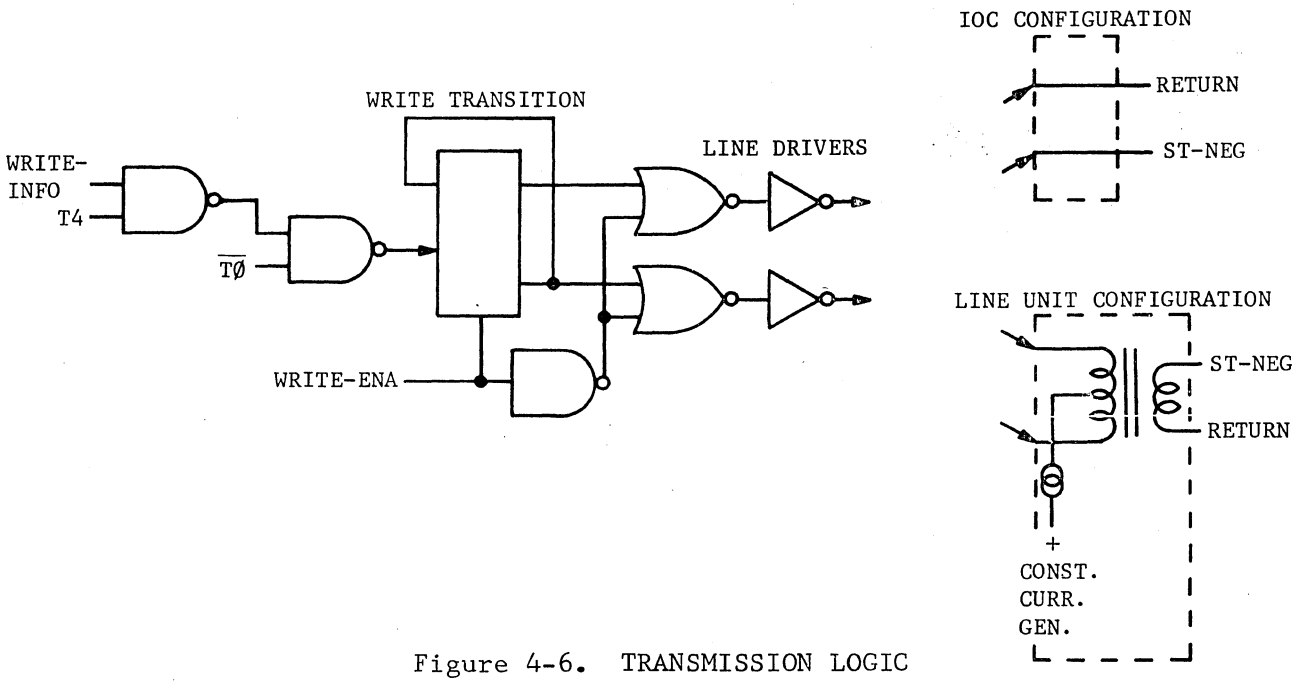

Figure 4-6. TRANSMISSION LOGIC

The WRITE-ENAble signal is developed whenever data is to be transmitted. Table 4-4 shows the state and mode combinations and the reason that WRITE-ENAble is developed. The IOC conditions are shown in block type, and the line unit conditions are shown in italics. The absence of the WRITE-ENA signal resets the WRITE TRANSITION flip-flop, returning it to an initial state. This allows each transmission to begin by forcing the ST. NEG. line in a negative direction. With WRITE-ENAble active, each TØ toggles the WRITE TRANSITION flip-flop, reversing the input signals to the line drivers. The WRITE-TRANSITION flip-flop is also toggled at T4 time if the WRITE-INFO signal is active at that time. The WRITE-INFO signal becomes active if a 1 bit is to be transmitted.

Table 4-4. WRITE ENABLE DEVELOPMENT

	MODE			
State	Escape	Select	Write	Read
S3-S9	DLE Character	I/O Sel. Character	Data Character	*Data, Delete, or Unit Seprator*
S10-S11	Check Bits			*Check Bits*
S13-S14	*ACK "1"s*			ACK "1"s

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4-5.1 IOC WRITE & LINE UNIT READ LOGIC (Continued)

The CH1 card contains nine gates, any of which can develop WRITE-INFO. Two of these gates act as one large AND gate, and are used in developing WRITE-INFO as data is shifted out of IOS. The other seven gates are used by the logic to manufacture bits when necessary. The methods of developing WRITE-INFO in the IOC are summarized below.

S3 to S9	Data
S5 STATUS	3 bit (EOT code)
S7 ESCAPE	5 bit (DLE code)
S7 POLL LOAD	5 bit (load request)
S8 POLL ESCAPE	6 bit (load request)
S10 CK1	CK1 bit
S11 CK1	CK2 bit
S13	Ack 1 (first)
S14	Ack 1 (second)

4-5.2 IOC READ & LINE UNIT WRITE LOGIC

Each voltage transition on the two-wire line produces the READ-SIGnal, a short, positive pulse. Figure 4-7 shows a simplified diagram of the receive logic, and the timing of some of the signals that are involved. Three flip-flops, WINDOW, CLOCK, and DATA, monitor the READ-SIGnal to determine whether each incomming pulse is a clock pulse (a normal bit-time transition) or a data pulse (a 1 bit).

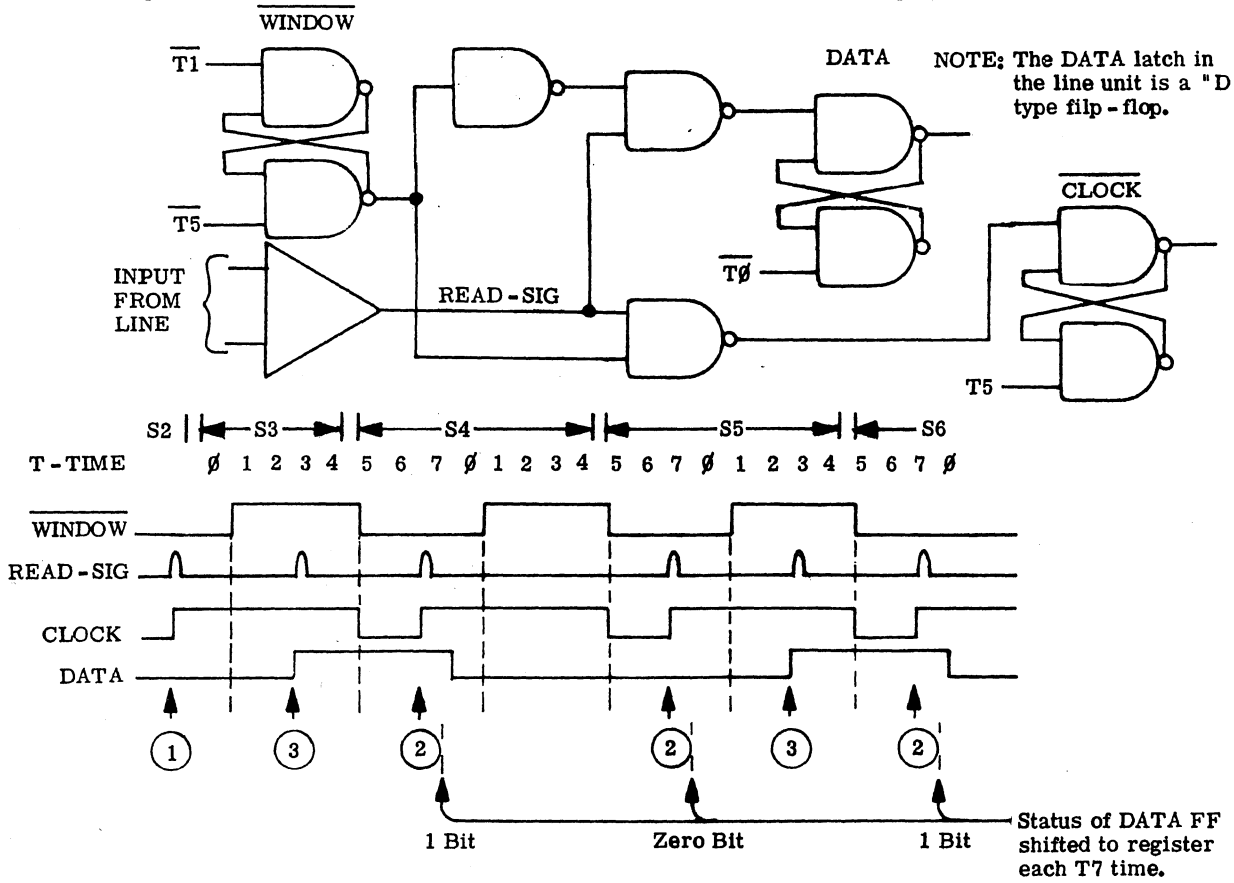


Figure 4-7. RECEIVE LOGIC D-364

4-5.2 IOC READ & LINE UNIT WRITE LOGIC (Continued)

Before the first pulse is received, the logic waits in S2 with the WINDOW flip-flop reset. The first pulse received (1) sets the CLOCK flip-flop, and synchronizes the time counter and the state counter with the incomming data. After the first pulse, any pulse occurring within the time of T5 through TØ (2) sets the CLOCK flip-flop, and is recognized as a clock pulse. This is the period where the WINDOW flip-flop is reset. Any pulse occurring during T1 through T4 (3) (when the WINDOW flip-flop is set) is recognized as a data pulse, or a 1 bit.

The full 7-bit ASCII character is loaded into the shift register by entering the output of the DATA flip-flop each T7 time, in states 4 through 10. The DATA flip-flop also supplies information to the parity check logic. The CLOCK flip-flop output is tested each T4 time (S3 through S11) to be certain that all nine clock pulses are properly received. The WINDOW and CLOCK flip-flops are also used in SØ and S1 to check (at T4 time) for the absence of clock pulses.

4-5.3 PARITY FLIP-FLOPS

Character parity is created during transmission, and checked while receiving (and during STATUS retrieval by the IOC) by two flip-flops, CK1 and CK2. The CK1 and CK2 flip-flops operate identically in the line unit and the IOC when checking parity. However, the nomenclature is reversed; they are called $\overline{CK1}$ and $\overline{CK2}$ in the line unit. The following explanation uses CK1 and CK2 except in operations that are unique to the line unit, where the CK1 and $\overline{CK2}$ designations are used. Initially, when checking parity, CK1 is reset, and CK2 (called $\overline{CK2}$ in the line unit) is set. As the character is sent or received, each 1 bit is shifted through the two flip-flops, and their associated gates, changing the set/reset configuration. When the character is complete, the condition of CK1 and CK2 is observed for parity.

A character containing no 1 bits leaves CK1 and CK2 in their initial set and reset condition. However, when the first 1 bit is shifted through, CK2 changes state (CK1 is left unchanged). Thereafter, each clock (bit time) changes the state of both flip-flops, unless another 1 bit is shifted through. If a second 1 bit is shifted through, CK1 changes state and CK2 does not. Each subsequent 1 bit alternately toggles either CK1 or CK2. Zeros between 1 bits reverse the state of both flip-flops if they are alike (both set, or both reset), and leave them as is if they are in opposite states (one set, and the other reset). In summary:

- A character of all zeros causes no change in CK1 or CK2.
- The first 1 bit, and each alternate 1 bit thereafter, toggles CK2. This is true even if the 1 bits are interspersed by zeros.
- The second 1 bit, and each alternate 1 bit thereafter, toggles CK1, even if the 1 bits are interspersed by zeros.
- After the first 1 bit, zeros toggle both CK1 and CK2 if their states are alike, and neither if their states are not alike.

Applying this to a seven digit character, we see that CK1 and CK2 are toggled so that in the end state (S12) the CK1 flip-flop represents even parity for the odd numbered character bits (1, 3, 5, and 7). The CK2 flip-flop represents the parity for the [redacted] ODD numbered bits.

4-5.3 PARITY FLIP-FLOPS (Continued)

Parity of received characters is checked in S12, where both the CK1 and CK2 flip-flops must have returned to their initial states ($\overline{CK1}$/CK2) to indicate good parity. Good parity creates the signal $\overline{CKNG}$, allowing the exchange to continue normally. If the $\overline{CKNG}$ signal is not produced, the state counter is reset, and the character is not acknowledged. The $\overline{CKNG}$ (parity) signal in the IOC is available for test at test point 5 on the CH1 card.

Parity is generated during transmission by checking CK1 in S10, and again in S11. If CK1 is found to be set in S10, a 1 bit is transmitted, creating even parity for the even numbered bits (2, 4, and 6). If CK1 is found set in S11, a 1 bit is transmitted, creating even parity for the odd numbered bits (1, 3, 5, and 7). The toggling action of CK1 and CK2 cause CK1 to reflect the state of both flip-flops, by reading it in two successive timing states. Figure 4-8 shows several examples of character codes, and how the set/reset condition of CK1 and CK2 are affected. Notice that in S11, CK1 always reflects the configuration that CK2 had in S10.

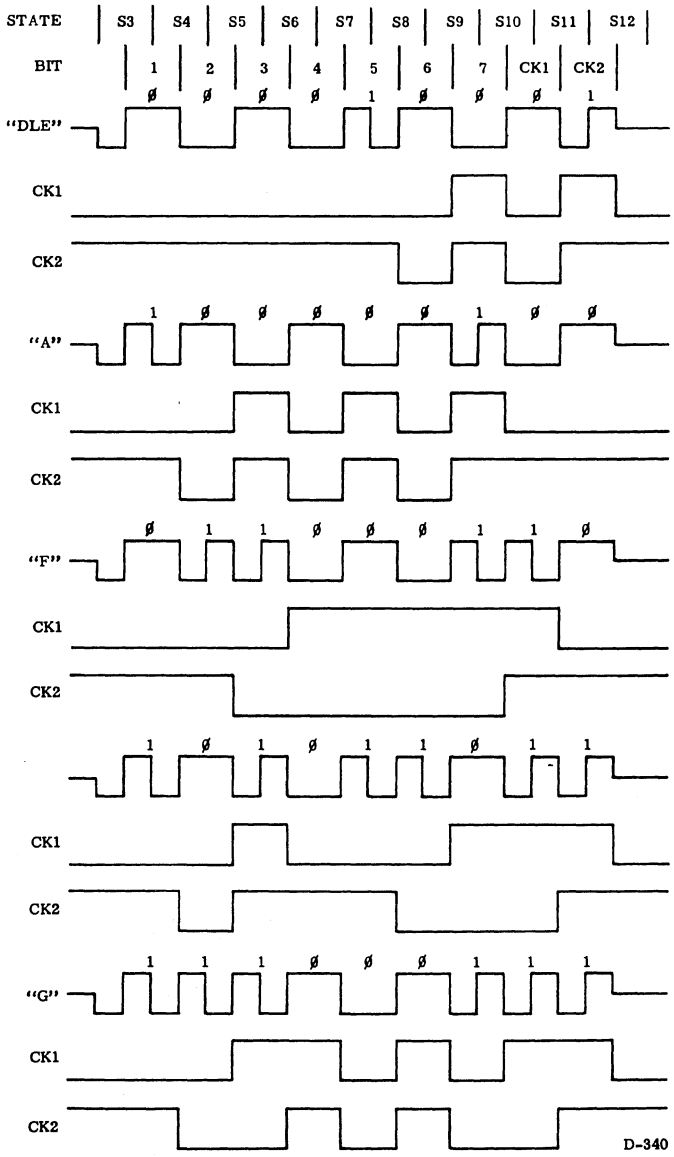


Figure 4-8. PARITY CHECKING

4-5.3 PARITY FLIP-FLOPS (Continued)

SPECIAL LINE UNIT USES FOR CK1 AND $\overline{CK2}$

Other than checking character parity in receive, and generating parity bits when sending, the CK1 and $\overline{CK2}$ flip-flops in the line unit perform two seperate functions. They generate an eighth bit, representing even character parity for the character that is passed to the peripheral device. This is done by controlling the 8-BIT flip-flop. CK1 and $\overline{CK2}$ also detect the status request from the IOC when a READ operation is ended.

To create the parity bit for the character that is passed to the peripheral device, the configutation of CK1 and $\overline{CK2}$ is checked in S10. If both CK1 and $\overline{CK2}$ are set, or if they are both reset, an odd number of 1 bits have been detected. If this is the case, a logic 1 is put onto the eighth bit line by the 8-BIT flip-flop (a cross latch). If CK1 and $\overline{CK2}$ are in opposite states during S10, an even number of 1 bits has been detected, and the parity bit is left at logic zero.

When CK1 and $\overline{CK2}$ are used to detect zeros (a status request from the IOC), CK1 is set initially, and $\overline{CK2}$ is reset initially. This is opposite the configuration for checking character parity. CK1 and $\overline{CK2}$ are preset to this condition during S13 and S14. If zeros are received in SØ, they are detected as follows:
The first zero toggles $\overline{CK2}$ setting it. The second zero toggles CK1 resetting it. When this happens, the trigger to the flip-flops is disabled (by the CK1/$\overline{CK2}$ configuration) and further zeros are ignored. However, the line unit is held in SØ until clock transitions stop. Normal data characters would not begin to arrive until S3, making it impossible to mistake data for status request.

4-6.0 STATUS

When the instruction character count is exhausted, the ACU activates P/LAST, setting the LAST flip-flop in the IOC. During a READ operation (the IOC is receiving), the next character received after LAST is set, is acknowledged by sending the two ack 1s, then seven zeros. During a WRITE operation (the IOC is sending), an End Of Transmission (EOT) code is sent if LAST is set. In either case, the line unit requests and fetches status from the peripheral device, and transmitts it to the IOC. The status character makeup is shown (without the parity check bits) in figure 4-9. The meanings of the terms are explained below.

Transmit or receive parity is not reflected directly in the status character. If character parity is bad, the character is re-transmitted until it is received properly, or until the transmitting device times out in FAULT status.

Bit	Meaning
7	Ø
6	1
5	Ø
4	Repeat if error
3	$\overline{\text{Fault}}$
2	Flag
1	Error

Bits 5, 6, and 7 of the status character are always this value.

Figure 4-9. I/O STATUS CHARACTER

- $\overline{\text{FAULT}}$ indicates that no fault has been detected by the line unit. Fault may occur from timeout, or from problems within the peripheral. Transmission problems are also detected as fault; never as error.

- FLAG is an indication from the peripheral that there is something unusual. The type of unusual state depends upon the design of the particular device. It may even be an operator key to allow the softwate to branch on flag.

- ERROR is the result of a signal from the peripheral, and the nature of the meaning depends upon the peripheral design.

- REPEAT IF ERROR is a function of the type of peripheral, rather than the status of the transmission. For example, a keyboard is the type peripheral that can repeat an entry if there were an error; a paper tape reader is not.

4-7.0 INTERFACE SIGNALS

Data enters the MT IOC from the processor on a parallel bus, and is gated by the SEL-DIGIT, and SEL-GROUP signals. Data from the IOC to the processor is also parallel, but is converted to the internal six-bit code by the bus connections. During transfer of the I/O select character, the ACU holds the IOC-DATA-7 line at a constant logic 1. Figure 4-10 shows a simplified block diagram of the data lines at the ACU/IOC interface. Complete interface signals for both the IOC and line unit are shown in figures 4-11, and 4-12. The signal uses are listed below.

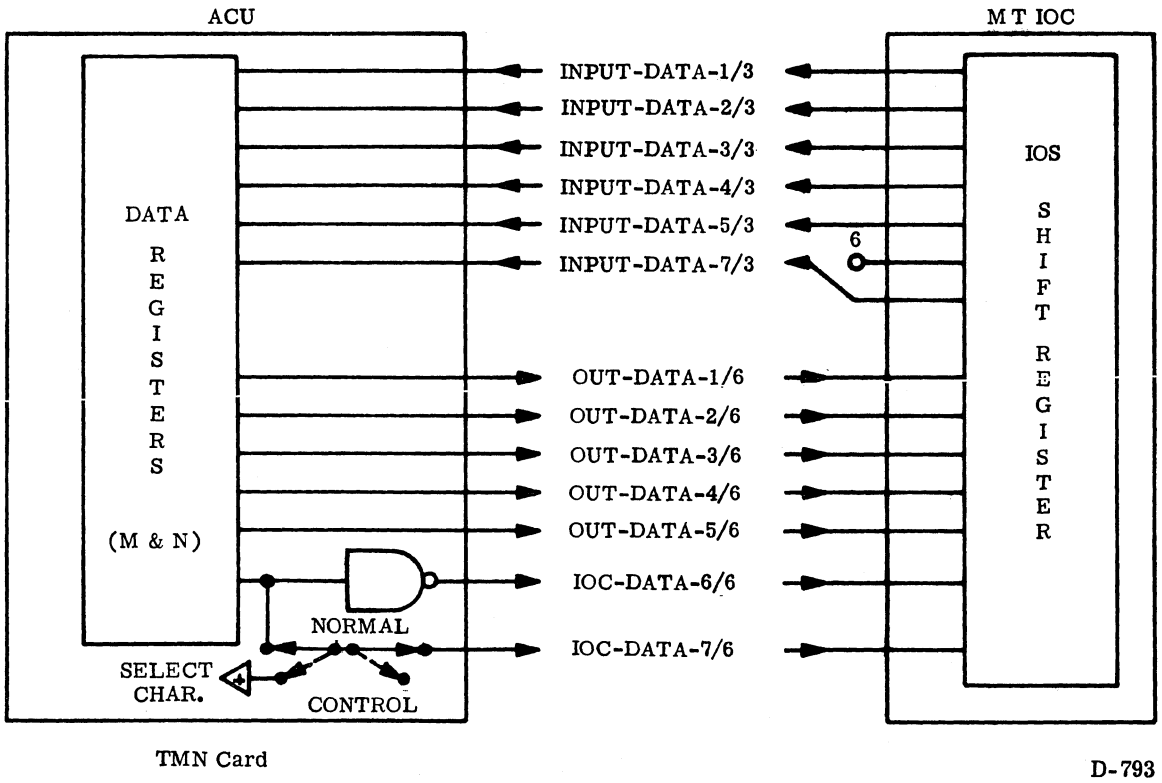


Figure 4-10. I/O DATA LINES

4-7.1 ACU/IOC SIGNALS

The processor provides and accepts identical interface signals, to and from all I/O channels. These signals are placed on a common bus, and gated to the individual I/O by the SEL-DIG and SEL-GROUP signals. The signal descriptions that follow are specific, concerning their use in the MT IOC, but may also contain general information on the use by other I/O types.

- P-LIM - The Partition LIMit signals determine the memory allotment, or partition size. The BCD number is controlled by hard wire jumpers on the CH2 card, and can be any number from one to ten. The number specifies the partition size in thousands of characters.

- PRIV-CHAN - The PRIVileged CHANnel signal is enabled by jumpering test points 7 and 8 on the CH1 card. It allows the IOC to access the privileged area of common memory. This is a user option.

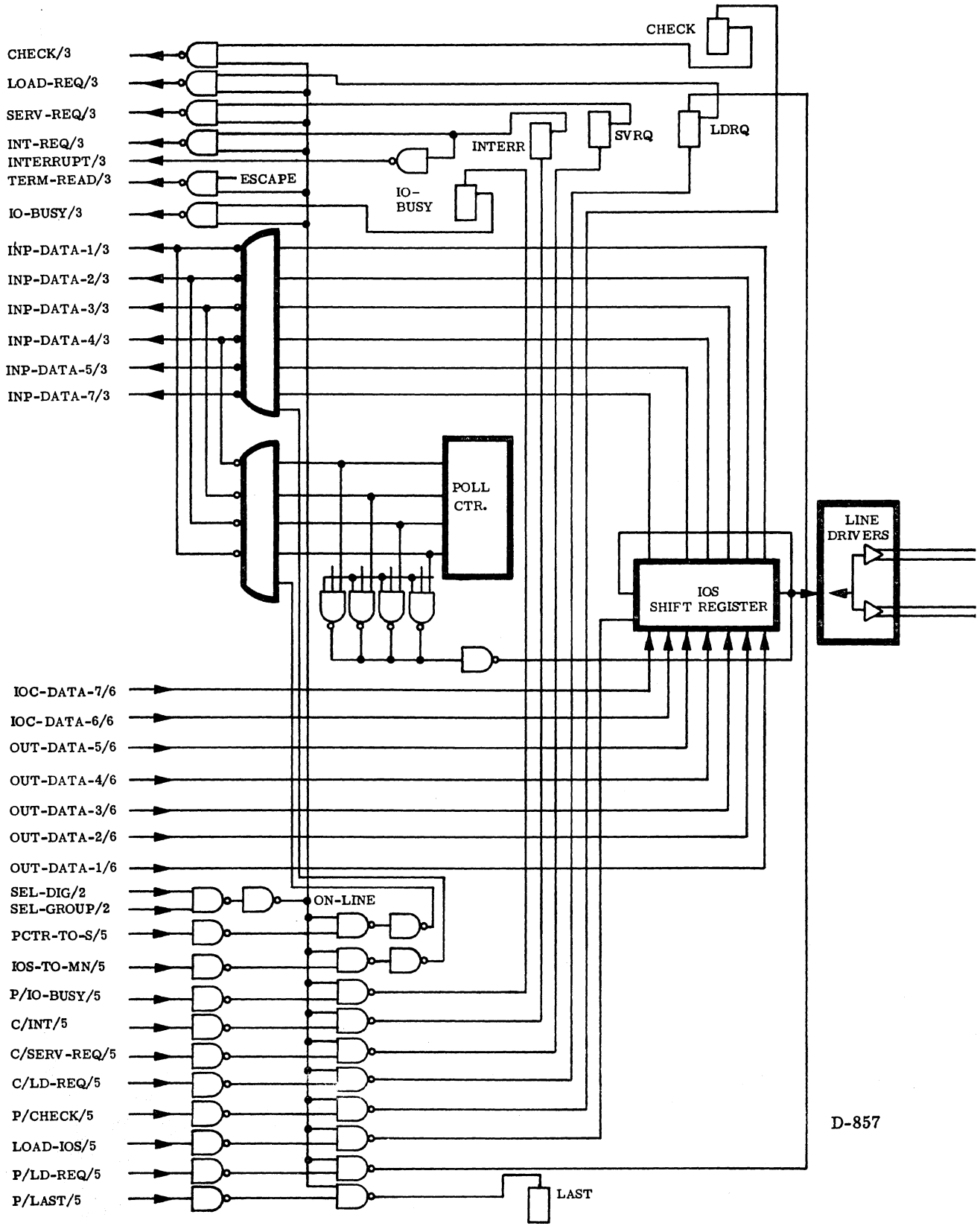


Figure 4-11. BLOCK DIAGRAM ACU/IOC INTERFACE

MT IOC & LINE UNIT

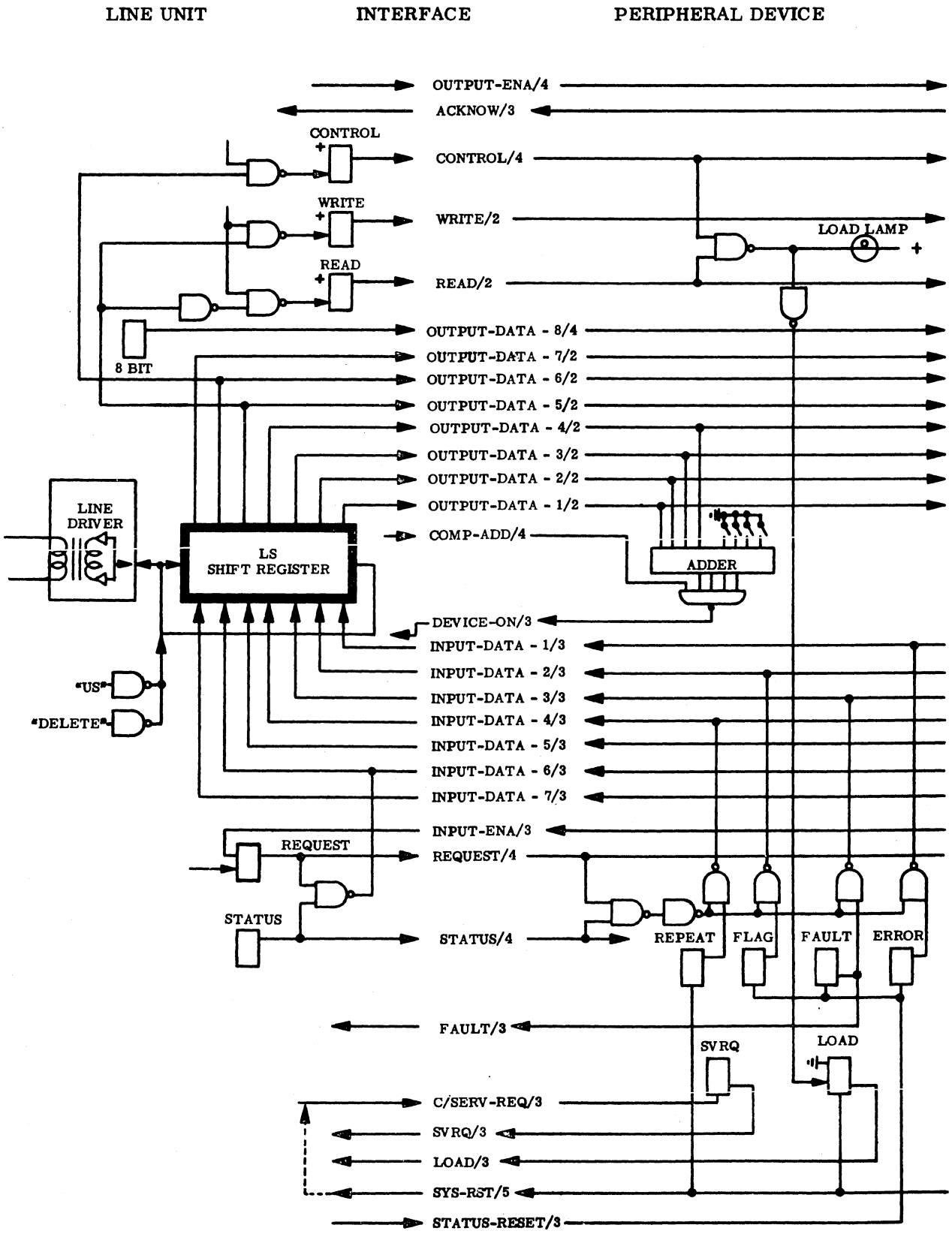


Figure 4-12. LINE UNIT/PERIPHERAL INTERFACE

4-7.1 ACU/IOC SIGNALS (Continued)

- CHECK and P/CHECK - CHECK is a signal to the ACU indicating that a program error has been made. The ACU determines when a program error has been made, and sets the CHECK flip-flop with the P/CHECK signal. Although it is only for ACU use, the CHECK flip-flop is located in the IOC, because it is a function of the partition. CHECK is always followed by a READ CONTROL select character from the ACU.

- LOAD-REQ and P/LOAD-REQ - The preset LOAD-REQuest signal from the ACU is given when a data fault, or program error (CHECK) is found. If the CHECK signal is received by the ACU (even though the CHECK was generated by the ACU) the P/LOAD-REQ signal is returned to the IOC.

- LOAD-REQ - LOAD REQuest is a signal from the output of an IOC flip-flop. It can be set in the MT IOC if an acknowledgement is received after a poll for load request.

- C/LOAD-REQ - Clear load request is generated by the ACU, and given to the IOC upon completion of program loading (READ CONTROL).

- SVRQ - Service request is the signal given to the ACU by the IOC when a peripheral of the partition needs to branch to a new or different instruction. The hardware only sets a flip-flop, but a normal software program is designed to allow a branch when SVRQ is set. Service request is NOT to be confused with INTERRUPT, where only one character exchange is requested.

- C/SERV-REQ - Clear service request is an ACU activated signal. It is given to the IOC when a service request is answered (by the arrival of a new instruction). The C/SERV-REQ signal can also be an indirect result of the SYS-RST signal in the ACU module.

- INT-REQ and INTERRUPT - These two signals are IOC generated. They differ only in that INTERRUPT is a direct signal from the IOC flip-flop, and INT-REQ is gated by ON-LINE (from SEL-DIG and SEL-GROUP). INTERRUPT indicates to the ACU that the IOC is ready to transfer a single character (either into or out of memory). All input/output data is transfered through INTERRUPT, one character at a time.

- IO-BUSY and P/IO-BUSY - IO-BUSY is a marker to the ACU that the channel has an input/output instruction, and is operating independantly upon that instruction. The ACU sets IO-BUSY (using the P/IO-BUSY signal) whenever the IOC is given a READ, READ CONTROL, WRITE, or WRITE CONTROL select character. IO-BUSY can be reset for a variety of reasons, but when it is reset, it is an indication to the ACU that the I/O instruction has been completed.

- INP DATA - A set of six parallel data lines upon which the IOC data enters the ACU.

- OUT-DATA and IOC-DATA - The OUT-DATA lines cary bits 1 through 5 fron the ACU to the IOC. The IOC-DATA lines cary bits 6 and 7 fron the ACU to the IOC.

4-7.1 ACU/IOC SIGNALS (Continued)

- IOS-TO-MN - An ACU signal to the IOC, gating or enabling data from the IOC output register to the INP-DATA and IOC-DATA lines. The ACU uses this signal to read data or status into the M and N registers.

- C/INT - Generated by the ACU when an interrupt request is satisfied. The INTERRUPT flip-flop is cleared by this signal.

- SEL-DIG and SEL-GROUP - These signals are decoded from outputs that are generated by the X counter within the ACU. Each partition is uniquely selected by the SEL-DIGit and SELect GROUP signals. Any selection requires one digit line, and one group line to be active.

- LOAD-IOS - Generated by the ACU to strobe data from the OUT-DATA lines into the IOC shift register. LOAD-IOS precedes the P/IO BUSY signal when the IOC receives the select character.

- P/LAST - Generated by the ACU when the character count that was specified in the instruction is exhausted. P/LAST is also generated by the ACU if TERM-READ is received, and the non-fill bit is present.

- TERM-READ - A signal from the IOC that causes a premature cancellation of a READ operation that is in progress.

4-7.2 LINE UNIT/PERIPHERAL SIGNALS

- COMP-ADD - Sent to the peripheral by the line unit to indicate that a select character is on the data lines, and the device number should be compared with the assigned number of the peripheral.

- CONTROL - Signal to the peripheral that the line unit has decoded either a READ CONTROL, or WRITE CONTROL from the select character.

- SVRQ and C/SVRQ - Service request comes from the peripheral SVRQ flip-flop. The flip-flop is cleared by the C/SVRQ signal that is generated by the line unit upon receiving another select character. This is different than the IOC flip-flop that is cleared when a branch is made.

- OUTPUT-ENA - Output enable strobes the character that is in the line unit shift register (LS) onto the output data lines.

- READ - A signal from the reset side of the $\overline{\text{READ}}$ flip-flop. READ indicates that a READ or READ CONTROL operation has been decoded from the select character.

- REQUEST - A signal from the line unit indicating that a character (or status) is requested from the peripheral.

- STATUS - Always accompanied by REQUEST, status indicates that the status character is needed from the peripheral.

- STATUS-RESET - Clears the status flip-flops or cross latches within the peripheral. This signal is generated only after the device has been selected with a new operation, and has confirmed selection with DEVICE-ON.

4-7.2 LINE UNIT/PERIPHERAL SIGNALS (Continued)

- WRITE - Set by decoding a WRITE or WRITE CONTROL operation from the select character.
- ACKNOW - A response from the peripheral to the line unit, indicating that the character that was presented on the data lines has been accepted by the peripheral device.
- DEVICE-ON - A response signal from the peripheral device, indicating that the device number in the select character is the same as the assigned number of the peripheral.
- FAULT - A signal from the peripheral, indicating transmission problems, such as a device selected that is in a local condition, or problems within the peripheral device itself. The particular type of problem that is indicated is dependant upon the design characteristics of the particular device. FAULT is the only status indication that can be given to the line unit while the active operation is still in progress.
- INPUT-ENA - Gates one character from the peripheral onto the input lines. It appears to be a response to REQUEST, if the peripheral character is ready when the signal arrives.
- LOAD - A signal from the peripheral, indicating a request to load instructions into memory. Load is only valid if it comes from the peripheral designated as device zero.
- SYS-RST - An initialization signal given to the line unit from the peripheral during turn-on.

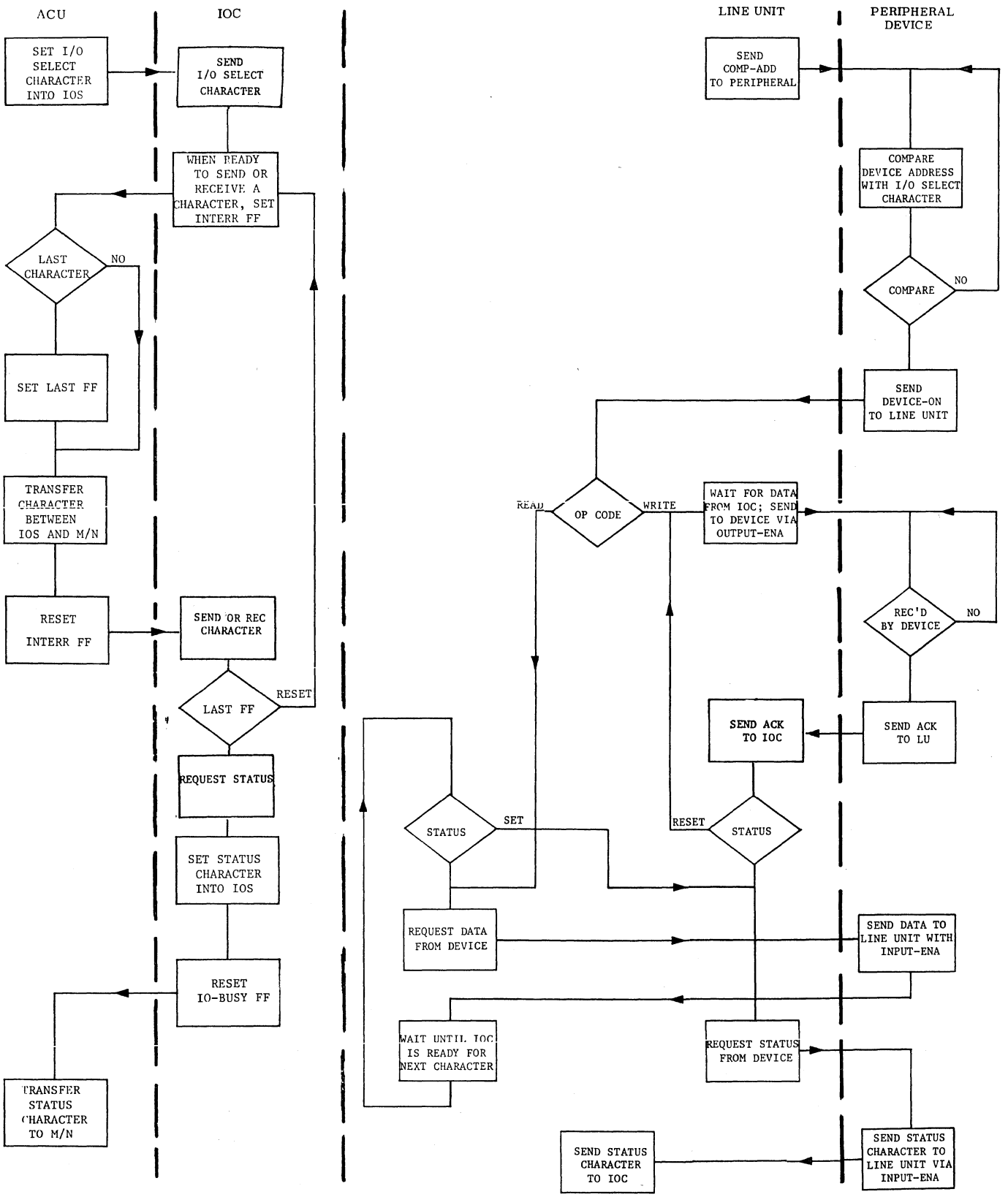


Figure 4-13. ACU TO PERIPHERAL FLOW OF OPERATIONS

4-8.0 SEQUENCE OF OPERATIONS

The normal sequence of ACU/IOC and line unit/peripheral interface operation is shown in the simplified flow chart in figure 4-13. Device selection and status retrieval are the same in all cases, but different signals are used for data transfer, depending upon whether a READ or WRITE is being performed.

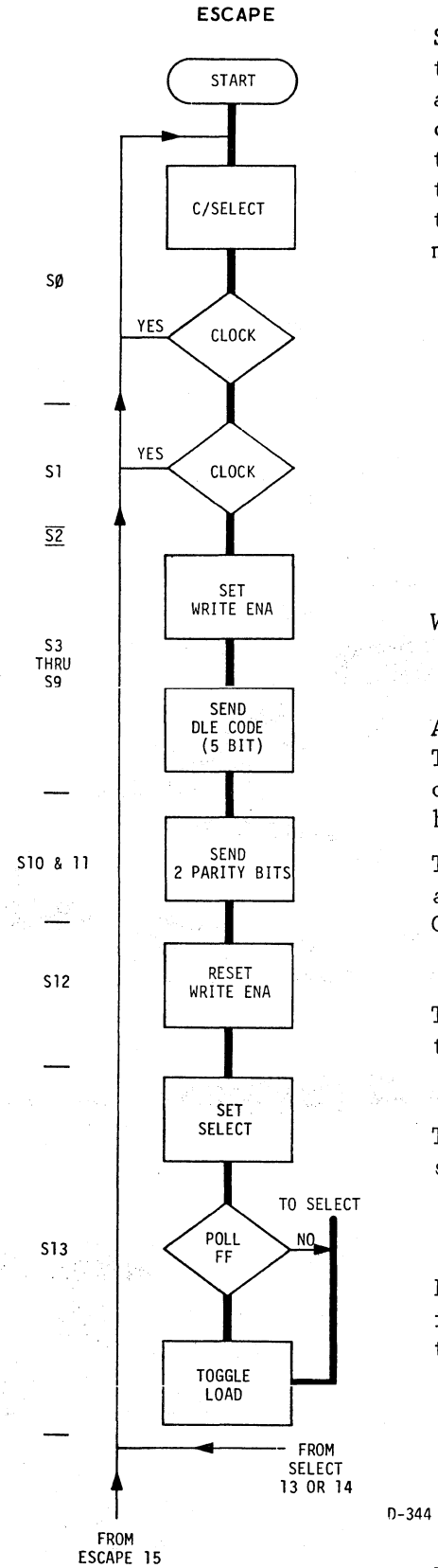
4-8.1 IOC OPERATION

The following pages contain figure 4-14, and is a detailed explanation of the overall IOC flow diagram. The darker connection lines between boxes indicate the flow of interest for the accompanying explanation. Sections of the flow chart are repeated to show the various paths that are taken to accomplish different things.

The explanation is an example of a typical polling sequence, that comes upon a service request. A WRITE instruction is returned (by the software program) in response to the service request. The WRITE instruction is followed by a READ, and last of all the status procedure is shown.

The status portion of the example shows only the decisions that are necessary for status retrieval. The status procedure is somewhat different for a WRITE and a READ operation, and are shown seperately.

The entire example in figure 4-14 assumes that a normal software program is resident in the partition, and that all hardware is operating normally. Each sheet of the figure is given a sheet number for reference within the example. The composite IOC flow chart is given in figure 4-15, and is an overall reproduction of the logic boxes that are given in the example.



SØ unconditionally clears the SELECT flip-flop. The two-wire line is monitored for any transitions. Any activity during this time (SØ and S1) causes the state counter to reset, and to begin counting again. Normally the line would be quiet, but if the last operation was terminated prematurely, a line unit could still be trying to send the remainder of its data (with no acknowledgements, the line unit will soon timeout).

WRITE-ENAble is set in preparation to transmission.

A DLE code is transmitted onto the line to all line units. The DLE is all zeros, except for the 5 bit that is placed onto the WRITE INFO line by gates on the CH1 card. This happens during S7 in the ESCAPE mode.

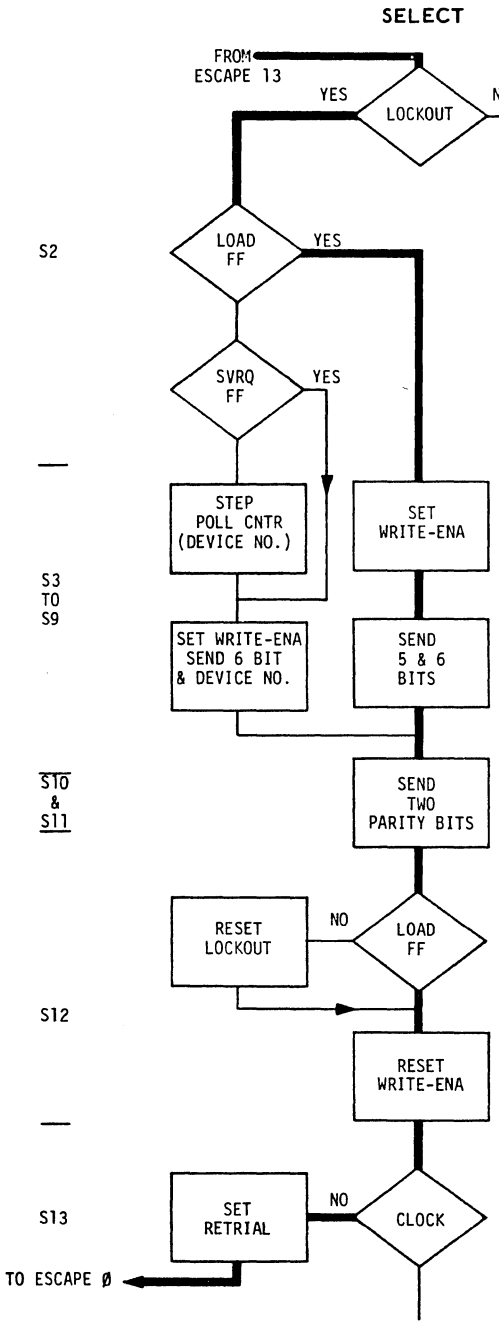
Two parity bits are generated by CK1, one in state 10, and another in S11 (CK1 in S11 reflects the status that CK2 had in S10).

The WRITE-ENAble signal is removed, finishing the transmission.

The SELECT flip-flop is set, preparing the IOC to attempt selection of one of the possible peripheral devices.

Before leaving ESCAPE, if the IOC is polling, the LOAD flip-flop is toggled. LOAD alternates states with each toggle, and is toggled only in S13 if the IOC is polling.

Figure 4-14. DETAILED IOC FLOW CHART (Sheet 1)



Sheet 1

D-349

Polling device zero for a load request.

If the IOC has just completed a READ or WRITE operation, the LOCKOUT flip-flop will be set. This causes at least one poll for service request, and one poll for load request, before looking for a possible new instruction. The dotted box (IO BUSY) would indicate that a new instruction had arrived from the processor, if IO BUSY were set.

From start-up, the initial poll is for LDREQ, as the LOAD flip-flop was toggled set before leaving ESCAPE.

The load request poll is transmitted. The poll counter is not used to put the zero device number onto the lower four bits.

All seven clock transitions are sent, and during S7 and S8, mid transitions are sent to make the 5 and 6 bits of the character a 1.

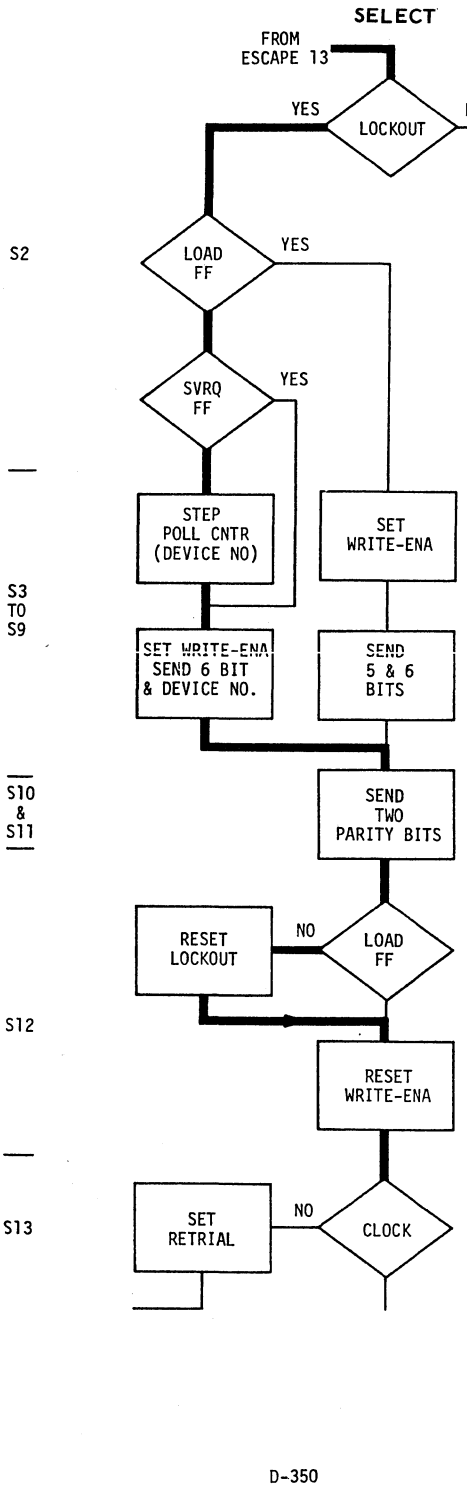
Two parity bits are added; for the load request poll, both parity bits are 1s.

The transmission is ended by resetting WRITE-ENA, and checking the LOAD flip-flop. Because this is the first poll, LOAD will be set, and LOCKOUT will remain set, until both polls are made.
C/LOCLOUT = S12·$\overline{\text{LOAD}}$·$\overline{\text{ESCAPE}}$

The IOC looks for a reply from device zero. Only the polled device answers, and only then if it has a request (in this case, load request).

1. A non-reply (no clock) would, for ordinary data, cause a retrial sequence, but in this case it does not, because the IOC is polling. When the POLL flip-flop is set, and RETRIAL (a cross latch) tries to set, it is held both set, and reset by the two logic paths. Essentially, RETRIAL is considered reset during S13 if POLL is set.
2. If device zero has a load request, the IOC will receive a clock, a data transition, and another clock. The decision block here is only the first clock.

Figure 4-14. (sheet 2)



Poll for service request.

After completing the initial portion of ESCAPE (sheet 1) the IOC returns to SELECT. This is the second poll (the first was for load request) and LOCKOUT is not yet reset. The LOAD flip-flop was toggled before leaving ESCAPE.

Because the SERV-REQ flip-flop is not set, the poll counter is advanced to the next device number.

The service request poll is sent by clocking the line in each state from S3 to S9, placing a mid-bit transition during S8 for the 6 bit of the polling question. As the character is clocked onto the line, the device number is gated from the poll cntr.

The two parity bits are added by gating the status of CK1 onto the line in S10, and again in S11.

Because the LOAD flip-flop is reset, the LOCKOUT flip-flop is reset.

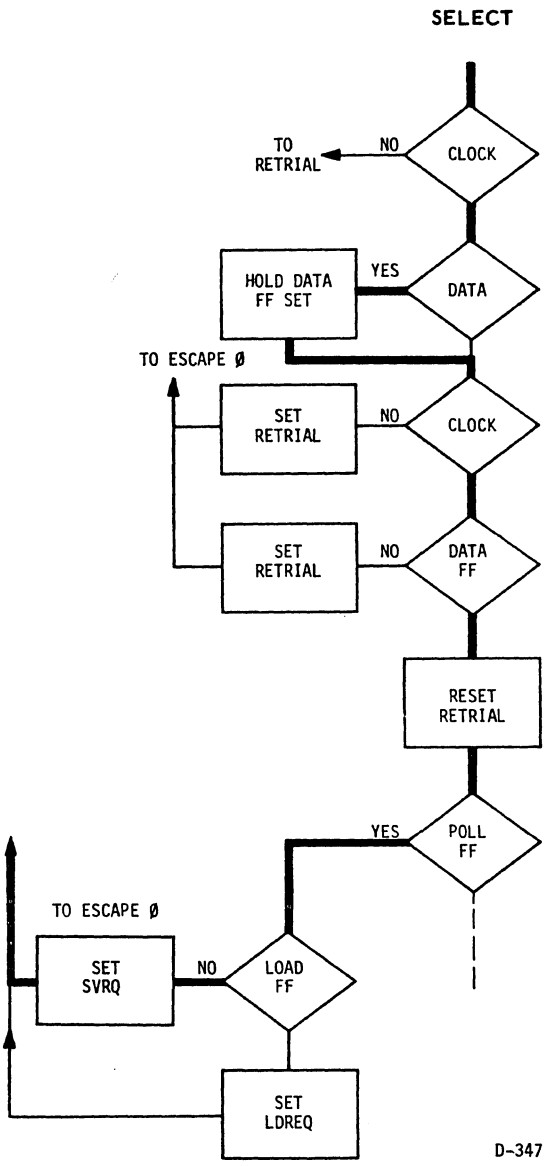
$LOCKOUT = S15 \cdot \overline{ESCAPE} + \overline{TURN\text{-}ON}$

$C/LOCKOUT = S12 \cdot \overline{ESCAPE} \cdot \overline{LOAD}$

A clock transition here means that the IOC is receiving the first part of an ack from the device that was just queried for service request. If no clock is detected, the device did not have a service request, and the IOC returns to ESCAPE Ø. The RETRIAL flip-flop (a cross latch) is always set here, but if POLL is set, RETRIAL is also held reset in S13. Because The IOC is polling, the state counter jumps to ESCAPE Ø, leaving RETRIAL reset.

Figure 4-14 (sheet 3)

The polled device responds to the Service Request inquiry.



When a select character is sent to a particular device, the IOC listens for an acknowledgement. The ack comes as a clock, a data transition, and another clock. Actually, the device sends two sets like this (two 1s) but the IOC only uses one.

If any of the transitions are missing, the process is repeated. However, if the IOC is polling, the device will have to wait until all other devices are polled, before it gets another try.
The mid-bit transition in the ack 1 holds the DATA flip-flop set. When the ack is completed, the DATA flip-flop is checked to verify that a 1 bit was received.

When the acknowledgement is verified, RETRIAL is reset. RETRIAL may not be set, but it is toggled reset anyway.

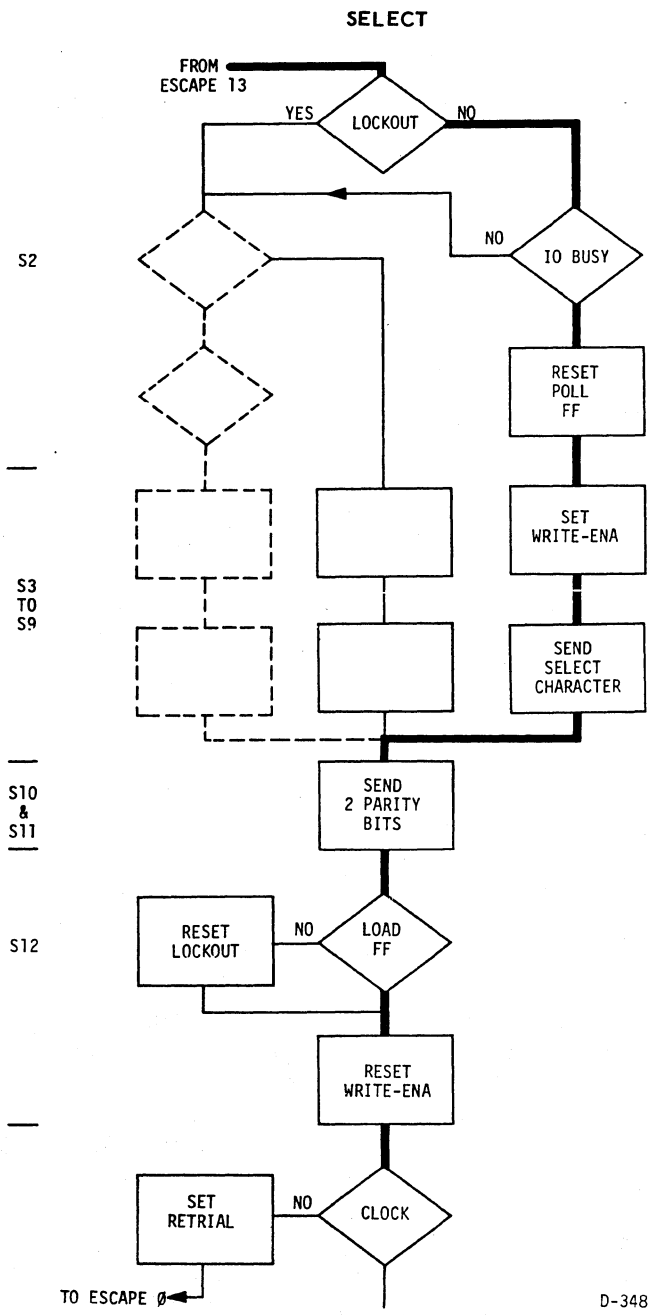
Because in this case the IOC was polling, the ack means that the device either has a load request, or a service request. The LOAD flip-flop is the key here; if LOAD is set, the ack is an answer to the load request inquiry, otherwise the answer is for a service request.

The proper flip-flop is set (SVRQ in this example) informing the processor of the request. The poll counter is locked, and the IOC continues to poll device zero for a possible load request, and the same device that answered, for a service request. This continues until the IOC receives an instruction, and IO BUSY is set.

NOTE: If the IOC were not polling, the ack received here would be from selection. The device would be receiving an instruction, and neither LOAD or SVRQ would be set. This situation is covered in later pages of this flow chart,

Figure 4-14 (sheet 4)

An instruction arrives from the ACU.



The IOC looks for a possible instruction from the ACU. The service request that was set on sheet 4 of this example has allowed a program branch. The ACU will return with an instruction for the device that answered the service request inquiry.
When the instruction, in the form of an I/O select character, is given to the IOC, the ACU sets IO BUSY. This is detected, and polling is discontinued.

If the instruction has not arrived, the IOC returns to polling, but the poll counter is not changed. Notice on sheet 2, that if the service request flip-flop is set, the poll counter is not stepped.

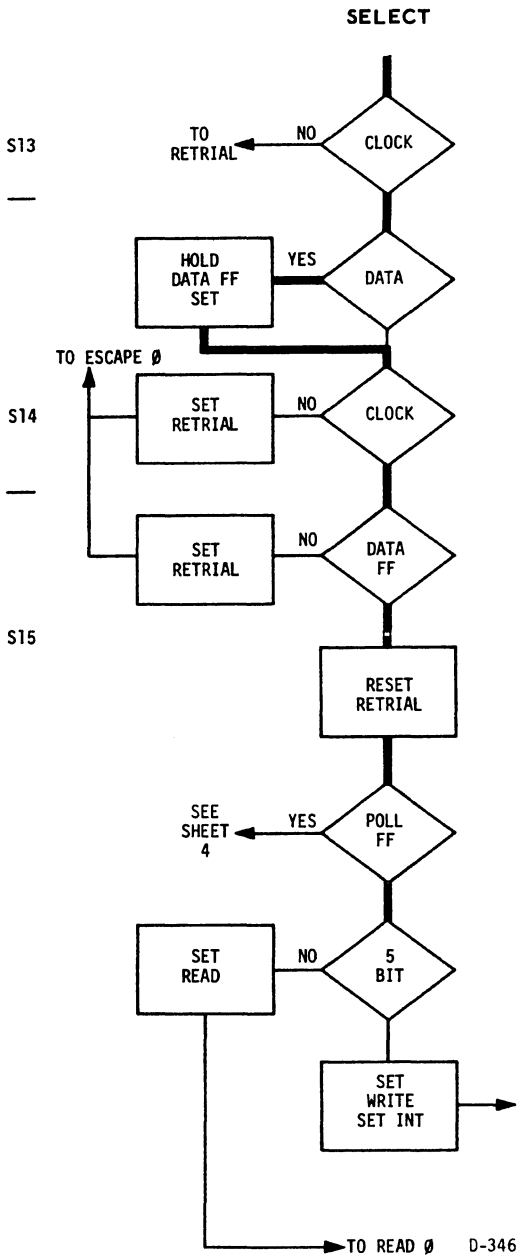
The select character in IOS is clocked onto the line, bit serially. The character is not lost, because the shift register is ring shifted to preserve the data for retrial, if necessary.

The parity bits are added to the character, gated from the CK1/CK2 circuit.

A clock transition on the two-wire line means that the selected line unit is acknowledging the select character.

Figure 4-14 (sheet 5)

The device acknowledges the select character.



The ack is received (clock, data, clock).

The DATA flip-flop is set by the mid-bit transition on the incomming clocks.

Receiving the clock transition after the data transition is the final verification that an ack has been received.

The DATA flip-flop is checked, and RETRIAL is toggled reset.

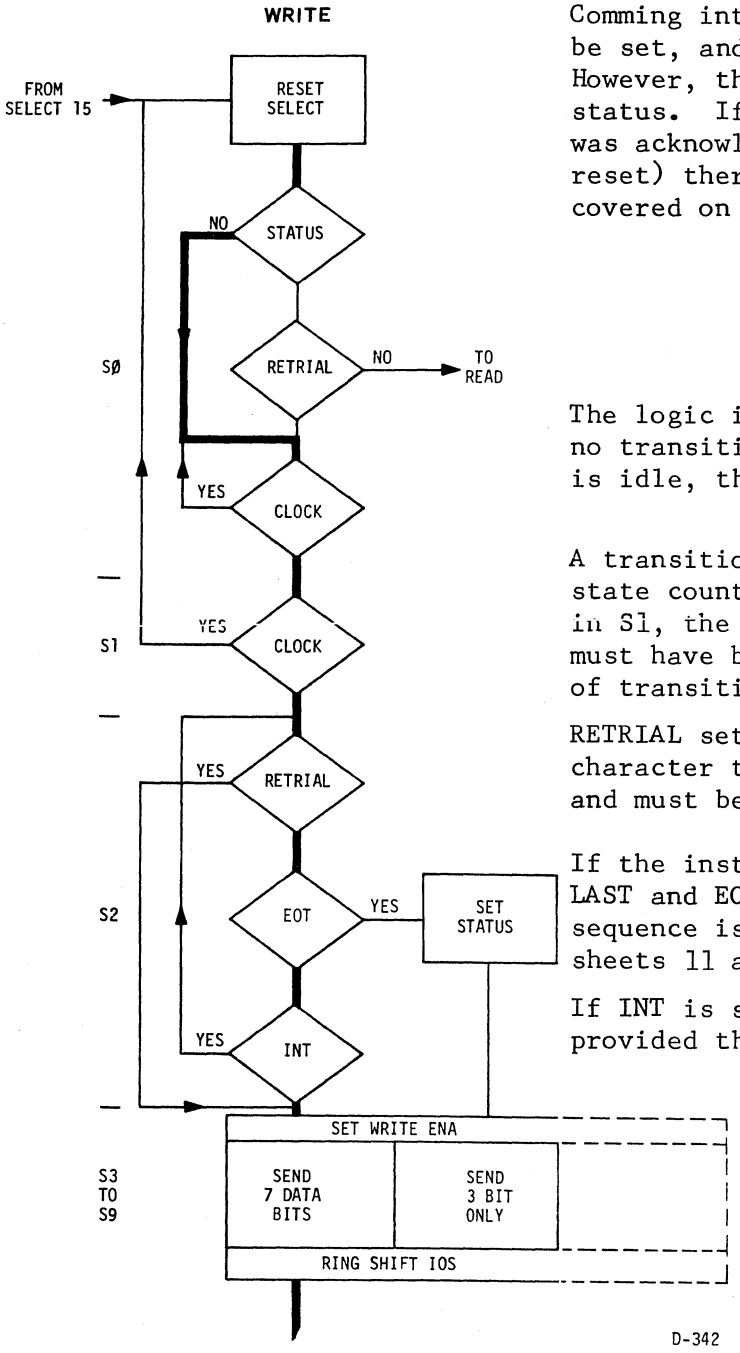
When the IOC is not polling, the ack is a response to an instructional select character that was sent to a particular device. This instruction was pulled from memory by the ACU because of a branch on service request. A select character need not be requested, it can result from an instruction in the normal program sequence.

The select character that is in the shift register is examined for a 5 bit (the select character remained in the register because it was ring shifted when the character was sent). Other than the polling questions (that are not applicable here) the 5 bit can only mean that the instruction is a WRITE or WRITE CONTROL. No 5 bit means a READ or READ CONTROL.

For this example, a WRITE instruction is illustrated on sheets 7 and 8 of this flow chart. A READ instruction is illustrated on sheets 9 and 10.

Figure 4-14 (sheet 6)

The IOC transmits data



Comming into WRITE, the status flip-flop will not be set, and the retrial decision is bypassed. However, the WRITE loop re-enters here to read status. If STATUS is set, and the status request was acknowledged (as indicated by RETRIAL being reset) there would be an exit to READ. Status is covered on sheets 11 and 12 of this example.

The logic is confined to state zero until there are no transitions on the two-wire line. Once the line is idle, the state is shifted to S1.

A transition on the line during S1 forces the state counter to reset. If there is no transition in S1, the operation continues. To leave S1, there must have been two states (SØ and S1) that are free of transitions on the line.

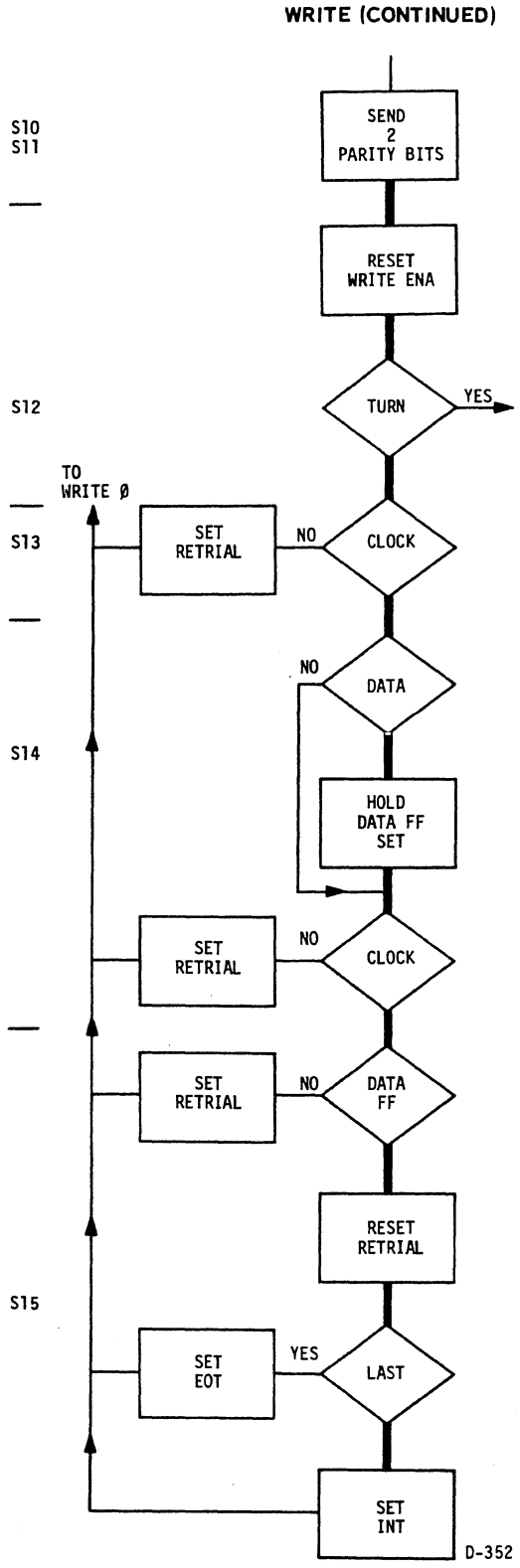
RETRIAL set at this time would mean that the last character that was transmitted was not acknowledged, and must be transmitted again.

If the instruction character count was exhausted, LAST and EOT are set, and the status request sequence is started. Status request is covered on sheets 11 and 12 of this example.

If INT is set here, it means that the ACU has not provided the next character. The IOC waits for the character, or timeout, whichever comes first (a timeout forces a jump to S14).

A normal data transmission sends the 7 ASCII bits, ring shifting IOS to retain the character for a possible retry. If the character count had caused the ACU to set LAST, EOT, and STATUS, the character that is transmitted is an EOT (all zeros, except for the 3 bit).

Figure 4-14 (sheet 7)



Parity bits are added, as needed, to the character. Under certain conditions this character could be the request to the line unit for status.

TURN is set when the instruction character count is exhausted during a READ operation. This causes a status request to be sent to the peripheral. At this point in a WRITE operation, if TURN is found set, the IOC makes a "turn-around" to receive (read) the status character.

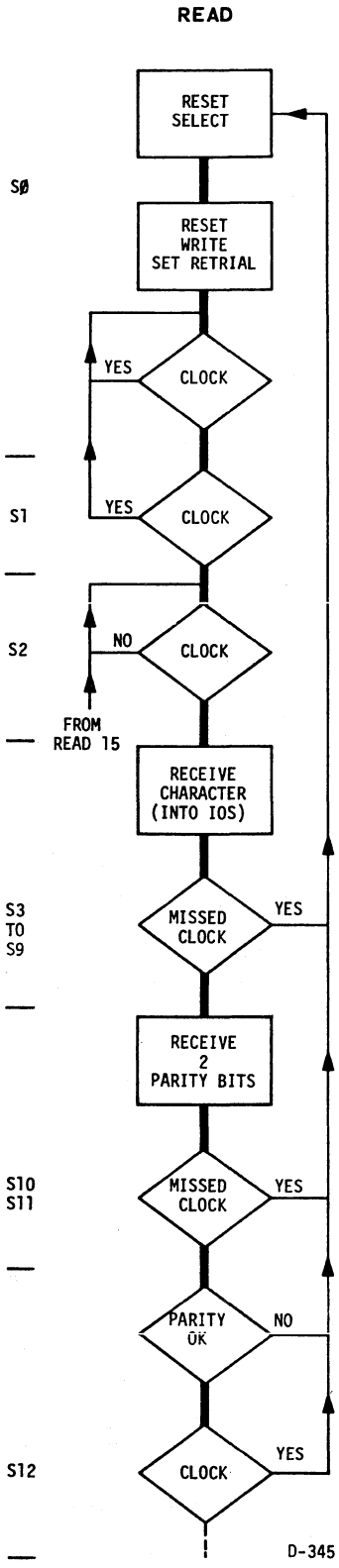
If exit is not made to receive the status character, an acknowledgement (clock, data, clock) is expected from the device.

If the ack is not received, RETRIAL is set.

When the instruction character count is exhausted, LAST is set. This sets the EOT flip-flop in preparation to sending an EOT character to the peripheral.

If the character count is not exhausted, INT is set for the next character from memory. The logic then jumps to WRITE Ø to get the character, and transmit it.

Figure 4-14 (sheet 8)



RETRIAL is set at the beginning of the READ loop, and reset when the character is received properly.

The two-wire line is monitored for two bit-times, and must be idle. The state counter is reset if a transition appears on the line during this time.

After two bit-times with no transitions, the IOC waits for the first transition of the line unit transmission.

Seven bits (including any zeros) are serially clocked into IOS during states 3 through 9.

Any state without a transition in this period (S3 through S9) causes the state counter to reset. The character will not be acknowledged by the IOC, and the line unit will have to re-transmit it.

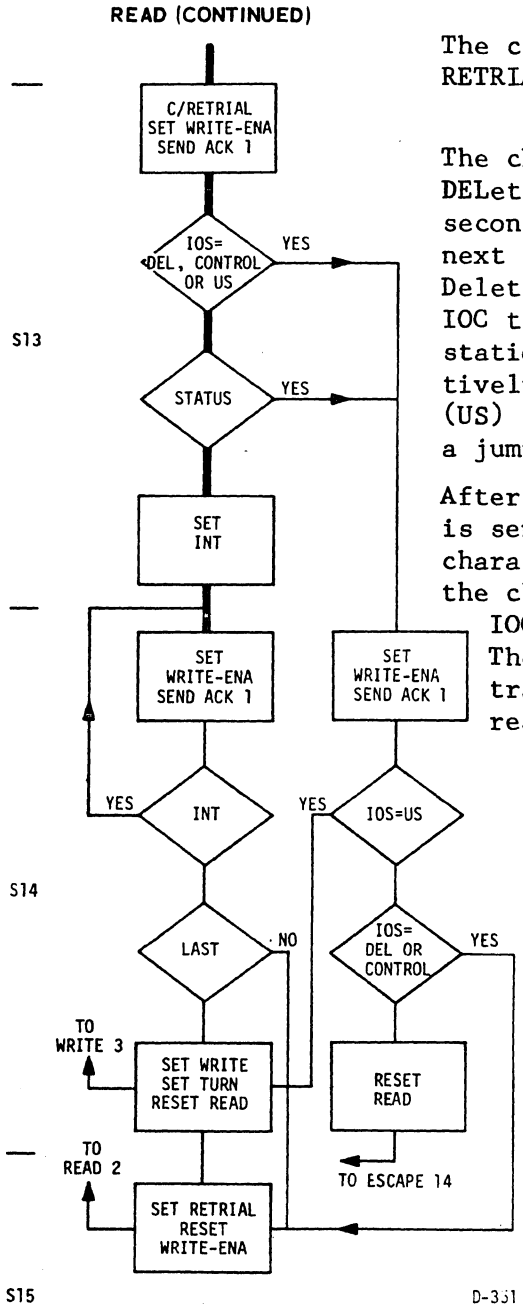
The two character parity bits are received.

States 10 and 11 must each contain at least one transition, or the state counter will reset.

Good character parity is indicated by the $\overline{\text{CKNG}}$ signal.

One or more extra transitions (after S11) cause the state counter to reset.

Figure 4-14 (sheet 9)



The character and parity bits have been received, and RETRIAL is reset. The IOC sends an ack to the line unit.

The character that was just received is examined. A DELete (all 1 bits), or a control character causes a second ack to be transmitted, and a return to S2 for the next character. The DELete is not given to the ACU. Delete is used by peripherals as a time fill, to prevent IOC timeout. Devices that require keyboard entry (workstations, etc.) will send many deletes during the relatively long delay between characters. A unit seperator (US) at this point causes a premature ending (below) and a jump to WRITE (to transmit status).

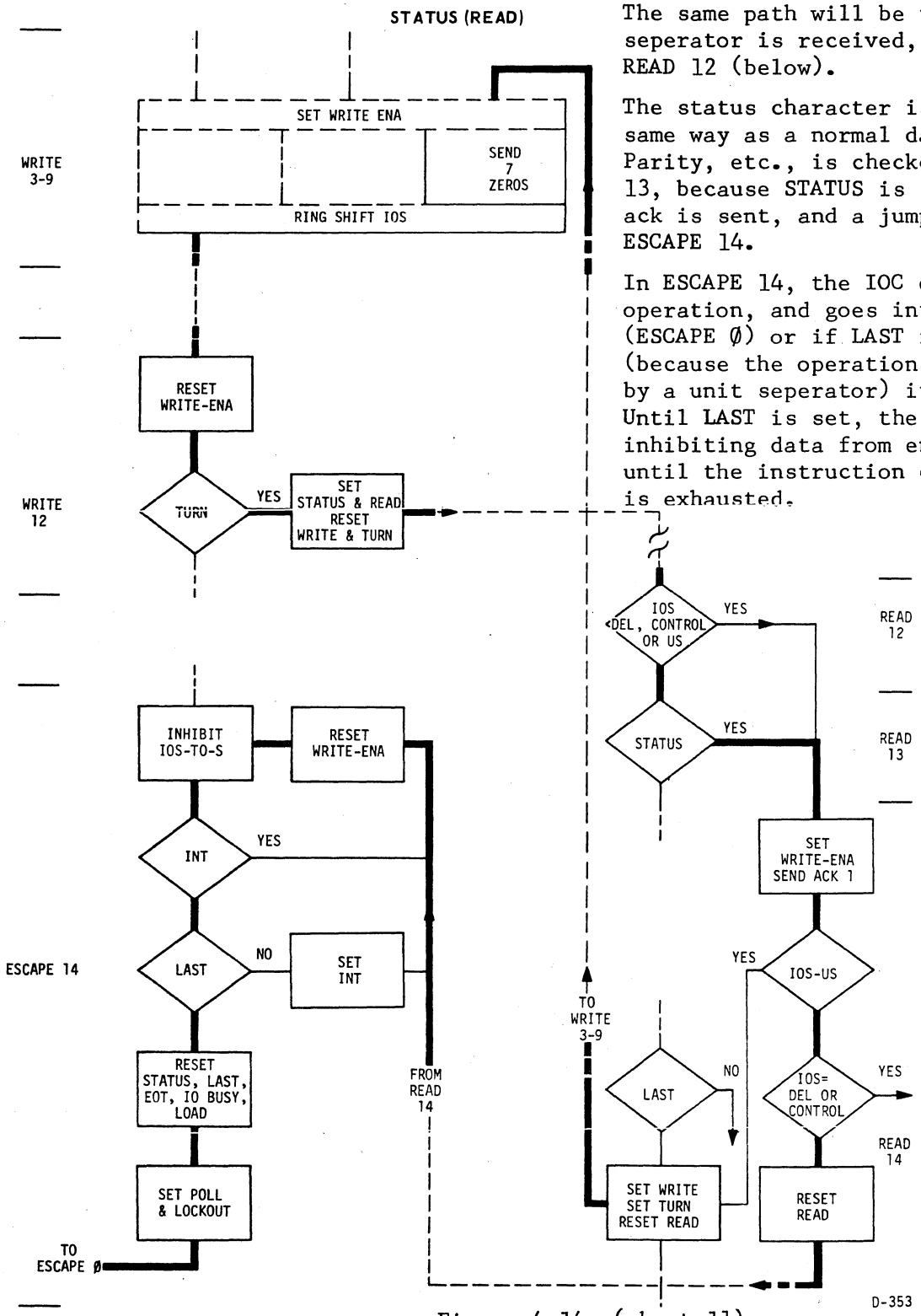
After a normal character, INT is set, and the second ack is sent. When the ACU answers the interrupt request, the character now in IOS will be placed into memory. Until the character is safely in memory, and INT is reset, the IOC is held in state 14, and the ack is repeated. The repeated acks (busy bits) keep the line unit from transmitting the next character until the IOC is ready to accept it.

LAST (in the left hand column) is set by the ACU if the instruction character count is exhausted. If LAST is set at this time, the IOC jumps to state 3 of WRITE, where a request for status will be made.
If LAST is not set, the IOC returns to S2 (READ) and receives the next character.

IOC timeout (approximately 20 to 35 ms) starts when RETRIAL is set. However, normal character exchanges and/or deletes will not allow timeout, because it is restarted in S15 when RETRIAL is set.

Figure 4-14 (sheet 10)

When LAST is found set in READ 14 (below), the IOC jumps to WRITE, and sends a status request (seven zeros). Because TURN was set before leaving READ, another jump is made from S12, back to READ, and setting the STATUS flip-flop on the way.

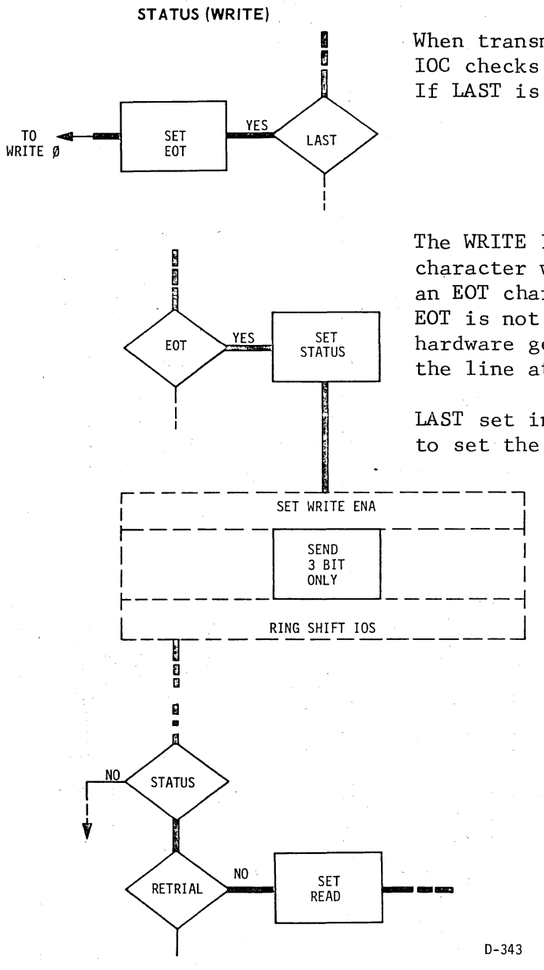


The same path will be taken if a unit seperator is received, and detected in READ 12 (below).

The status character is received in the same way as a normal data character. Parity, etc., is checked, and in READ 13, because STATUS is set, the second ack is sent, and a jump is made to ESCAPE 14.

In ESCAPE 14, the IOC either ends the operation, and goes into polling (ESCAPE Ø) or if LAST is not set (because the operation was ended by a unit seperator) it sets INT. Until LAST is set, the loop continues, inhibiting data from entering the ACU until the instruction character count is exhausted.

Figure 4-14 (sheet 11)



When transmitting (WRITE operation), the IOC checks the LAST flip-flop in S15. If LAST is set, the EOT flip-flop is set.

The WRITE loop continues, and when a character would be transmitted (S3 - S9), an EOT character is sent instead. The EOT is not a character from memory, it is hardware generated by gating the bits onto the line at the proper times.

LAST set in S15 sets EOT, causing STATUS to set the next time through S2. When the EOT is transmitted to the line unit, the next character that is received from the line unit will be status.

After the EOT is transmitted, the acks are verified, and all regular checks are made. When the IOC returns to SØ, STATUS being set causes a jump to READ. In READ, the status character is received, and checked. Status receiving and checking is shown on the previous sheet of this example.

Figure 4-14 (sheet 12)

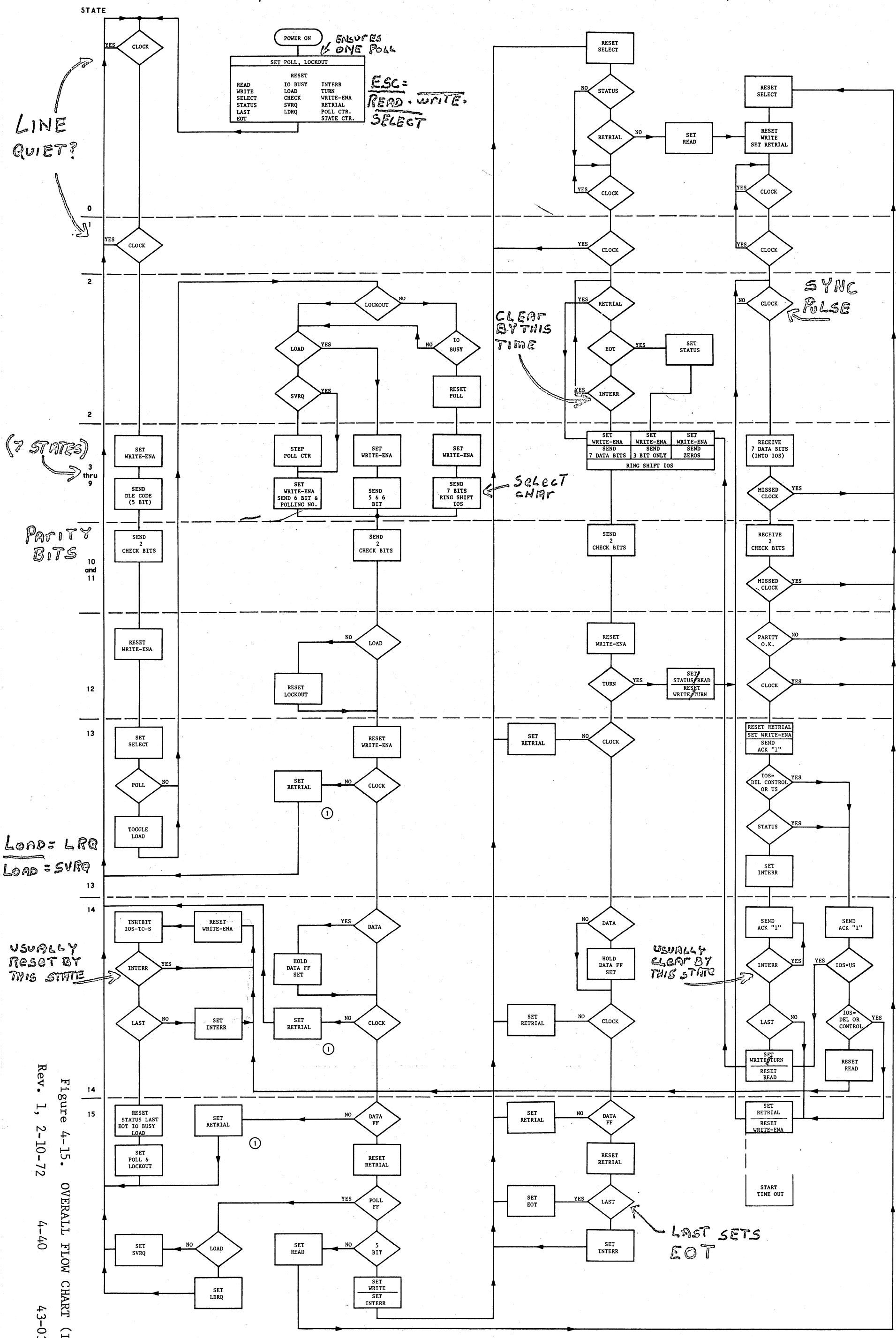


Figure 4-15. OVERALL FLOW CHART (IOC)

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(1) Except when polling; reset SELECT, and return to ESCAPE Ø.

NOTE: Timeout can occur at any time, causing a jump to ESCAPE.

4-8.2 LINE UNIT OPERATION

Overall line unit operation is simplified to a logic flow chart that is shown in figure 4-16. The explanation below is a brief summary of decisions that are shown within the flow chart, and the actions taken by the logic. As with the IOC, the line unit operates in four distinct modes; READ, WRITE, ESCAPE, and SELECT. Operation is very similar to that of the IOC, and only the differences are pointed out in the explanation below.

ESCAPE

In ESCAPE, the line unit ensures that the two-wire line is inactive, by monitoring the line during two consecutive character times (SØ and S1). In S2, the line unit waits for the first clock transition to arrive. The character, and check bits, are shifted into LS (shift register) and the transmission is checked for missing clocks (transitions), and for proper parity. If the transmission was good, and the received character is a DLE, the line unit logic enters the SELECT mode. Otherwise, if the character is not a DLE, or if the transmission was garbled, the logic returns to SØ, and begins to monitor the line again.

SELECT

Upon entering SELECT, the state counter jumps to S2, and the line unit waits for the first clock transition. The character is received by clocking the bits into LS, and it is checked for missing transitions, and for proper parity. If the character is a DLE, the state counter returns to SELECT, state 2, and awaits another character. If the character is not a DLE, it must be a select character, so the device number is compared with the assigned number of the peripheral. If DEV-ON becomes active, it means that the comparison was good, and this is the device that is being selected. However, if DEV-ON is not active, a jump to ESCAPE, state zero, is made, and the line unit waits for the next idle period on the line.

Assuming that DEVice ON is active, the select character must be one of three possibilities: a service request enquiry, an instruction (in the form of a select character), or a load request enquiry (if this is device zero). If the select character is either a load request, or a service request enquiry, and the corresponding flip-flop (LDREQ or SVRQ) is not set within the peripheral, the line unit reverts to ESCAPE, state zero. However, if the proper flip-flop is set, indicating that there is a request, two acks are sent, one in S13, and one in S14. The two acks will also be sent in response to a READ, WRITE, READ CONTROL, or WRITE CONTROL select character. In S15, the peripheral status flip-flops are cleared (from the previous transaction), and the type of instruction (READ, WRITE, etc.) is decoded to determine the operation.

If the select character that was received is an IOC polling enquiry, the line unit returns to ESCAPE,state zero, after acknowledging the character. Normal software programming will allow a branch on service request, and an I/O select character will return shortly for the requesting device. If the inquiry was a load request, a READ CONTROL select character will follow soon after the ack is made.

4-8.2 LINE UNIT OPERATION (Continued)

WRITE

Line unit WRITE or WRITE CONTROL means "receive characters from the IOC". Receiving is nearly identical to that in the IOC. In S13, S14, and S15 the data lines to the peripheral are disabled if an EOT (status request) is received. The lines are also disabled if the peripheral device is reporting FAULT status. FAULT status is the only status indication that can be reported during the active portion of an operation.

The normal character loop returns to S2 where the next character will arrive from the IOC. The loop continues until the IOC sends a status request (EOT). If FAULT is active the same loop applies, but the data lines to the peripheral are inhibited for the remainder of the operation. When the status request arrives, the line unit jumps to SØ instead of S2. When the line is free of activity, the line unit sets the STATUS flip-flop and enters the status mode.

READ

Line unit READ (send) is similar to the action of the IOC during WRITE. However, The CK1 and $\overline{CK2}$ flip-flops are used to check for zeros (status request for a read operation) that may arrive in SØ. In S3 through S9, where the data bits are transmitted, LS (the shift register) is ring shifted to retain the character, in the event that a retrial is necessary. Character acknowledgement is received in S13 and S14, as a clock transition, a data transition, and another clock transition.

During character transmission, if a FAULT or LOAD REQUEST has been generated by the peripheral, a unit seperator code (US) is sent to the IOC, terminating the READ operation.

If the peripheral is not ready to transmit the next character, the DELETE flip-flop will be set, and a DEL character will be transmitted.

STATUS

When receiving, LS is constantly checked for an EOT code. An EOT causes the line unit to request status from the peripheral, and transmit it to the IOC.

When transmitting the last character of a READ operation, the character is acknowledged by two 1s, and seven zeros from the IOC. The two 1s are received by the line unit in states 13 and 14 (although only one of the 1s is needed) and the state counter counts around to zero. During states 13 and 14, CK1 is set, and $\overline{CK2}$ is reset. With the two flip-flops in this configuration, any zeros arriving cause them to toggle (see SPECIAL LINE UNIT USES FOR CH1 AND $\overline{CK2}$). When two consecutive zeros are detected in SØ, status is requested from the peripheral, and is the next character to be transmitted.

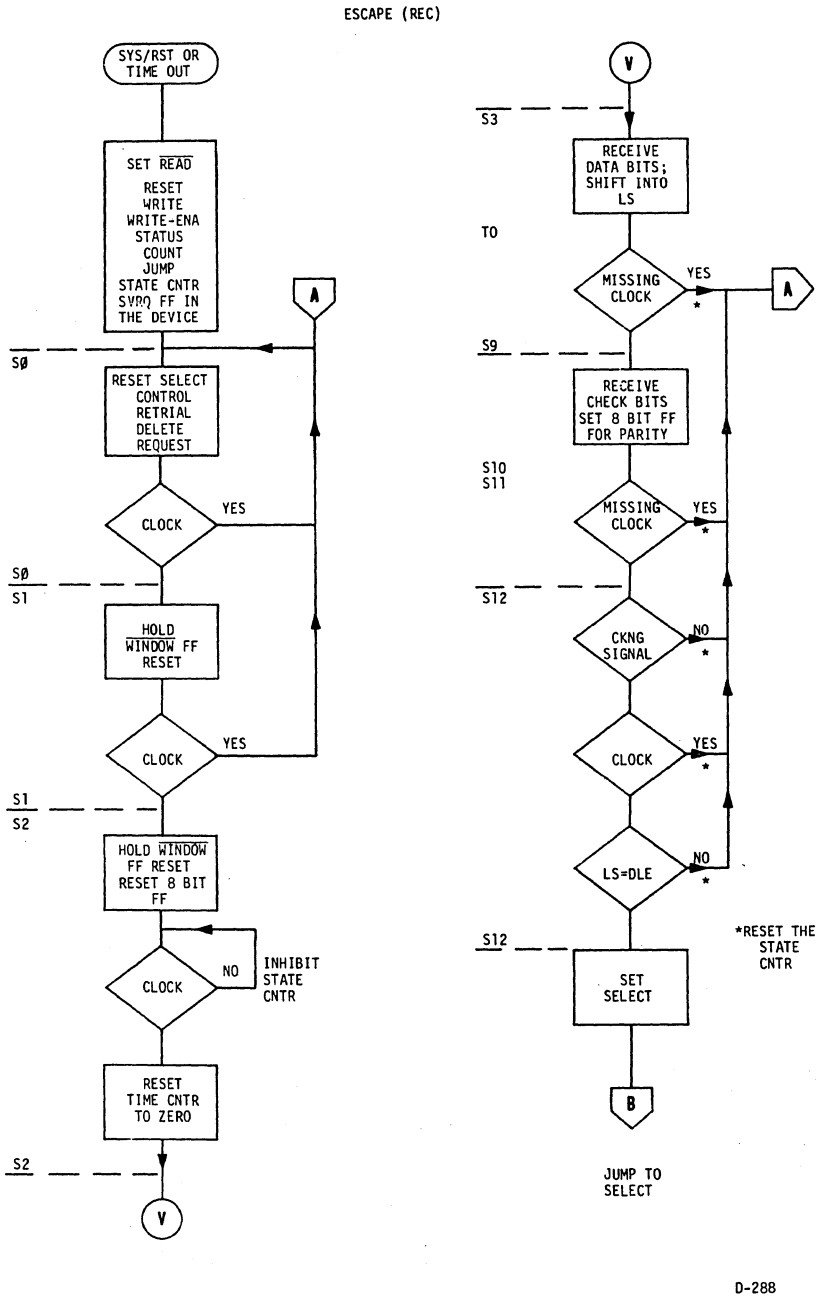


Figure 4-16. LINE UNIT OPERATION

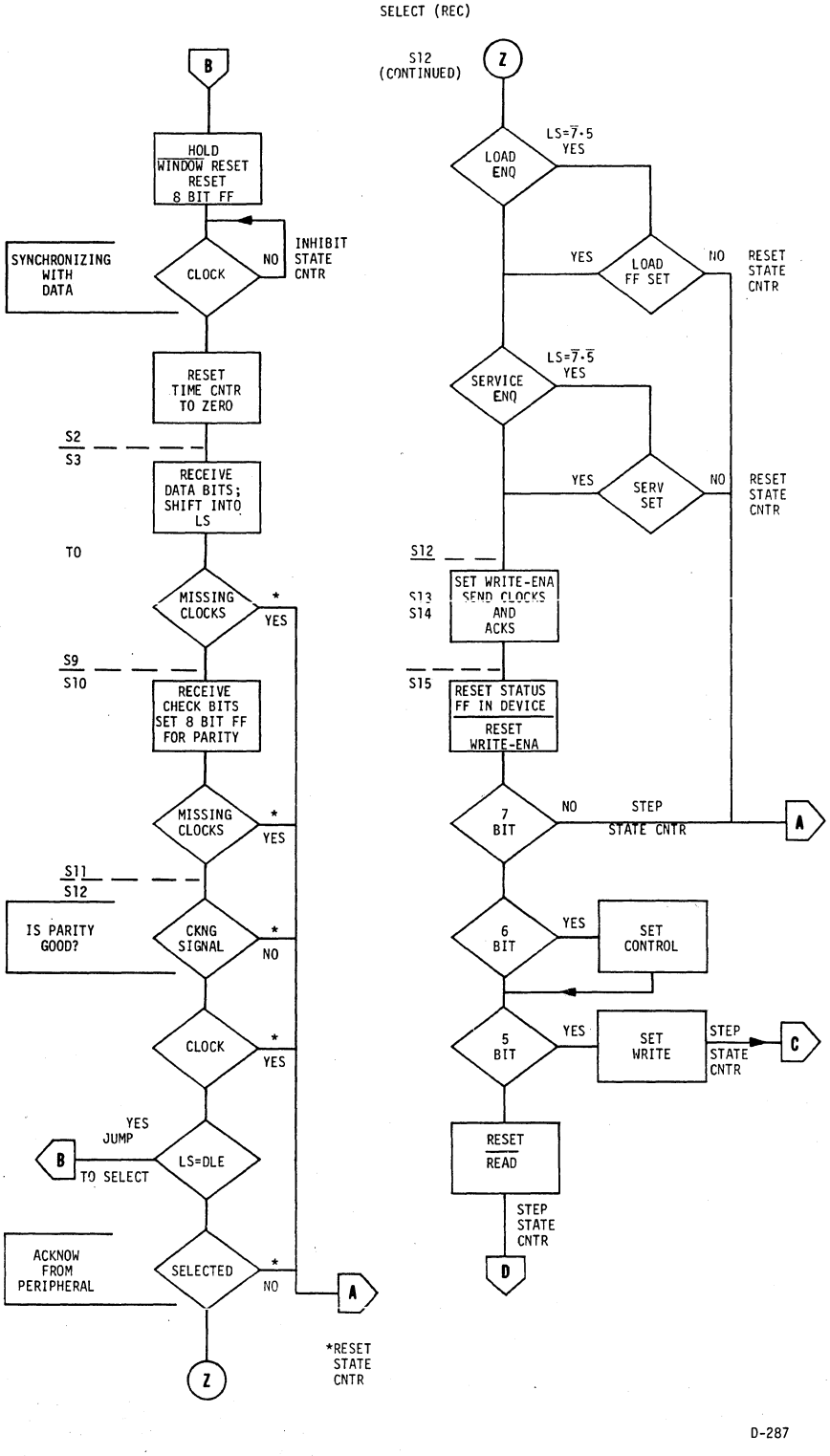


Figure 4-16. (Continued)

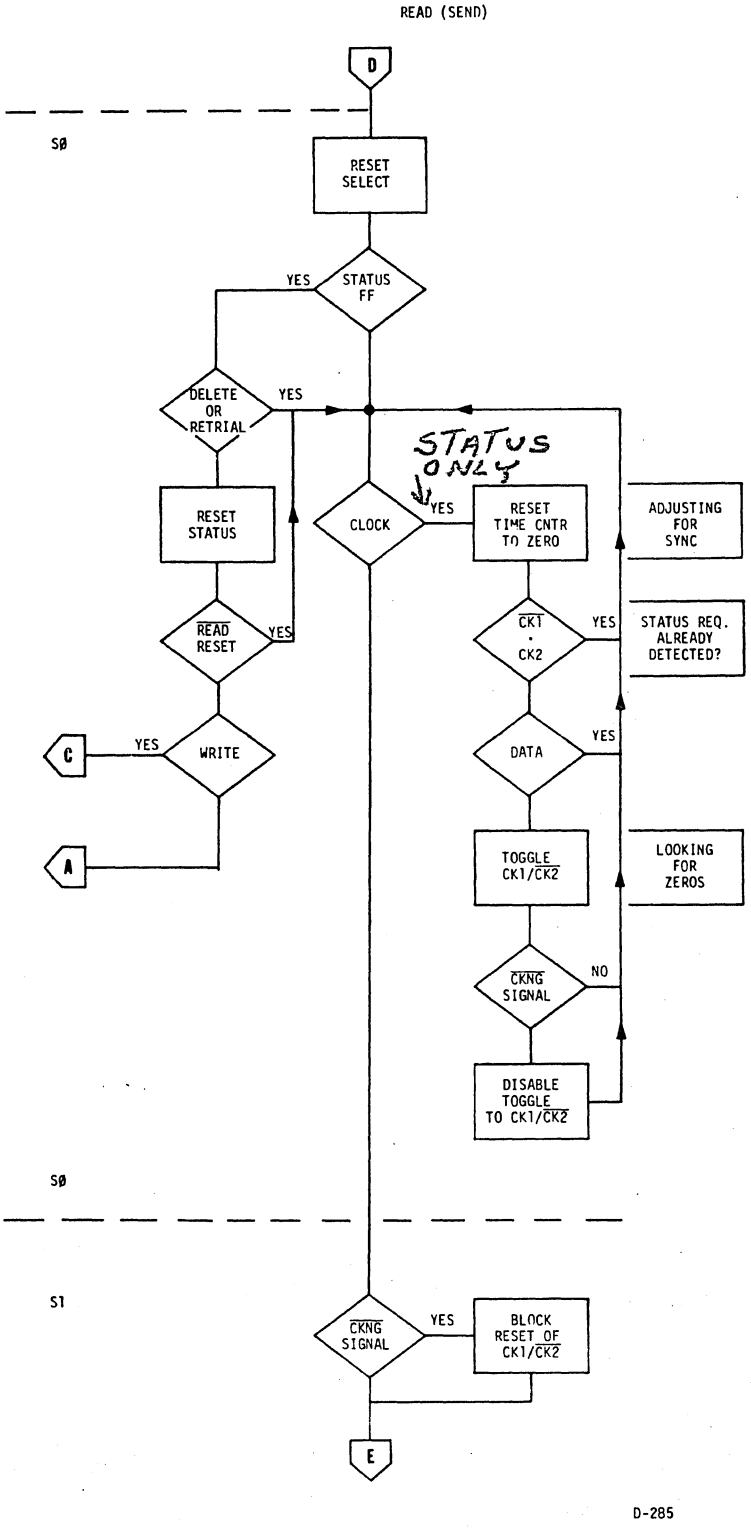


Figure 4-16 (Continued)

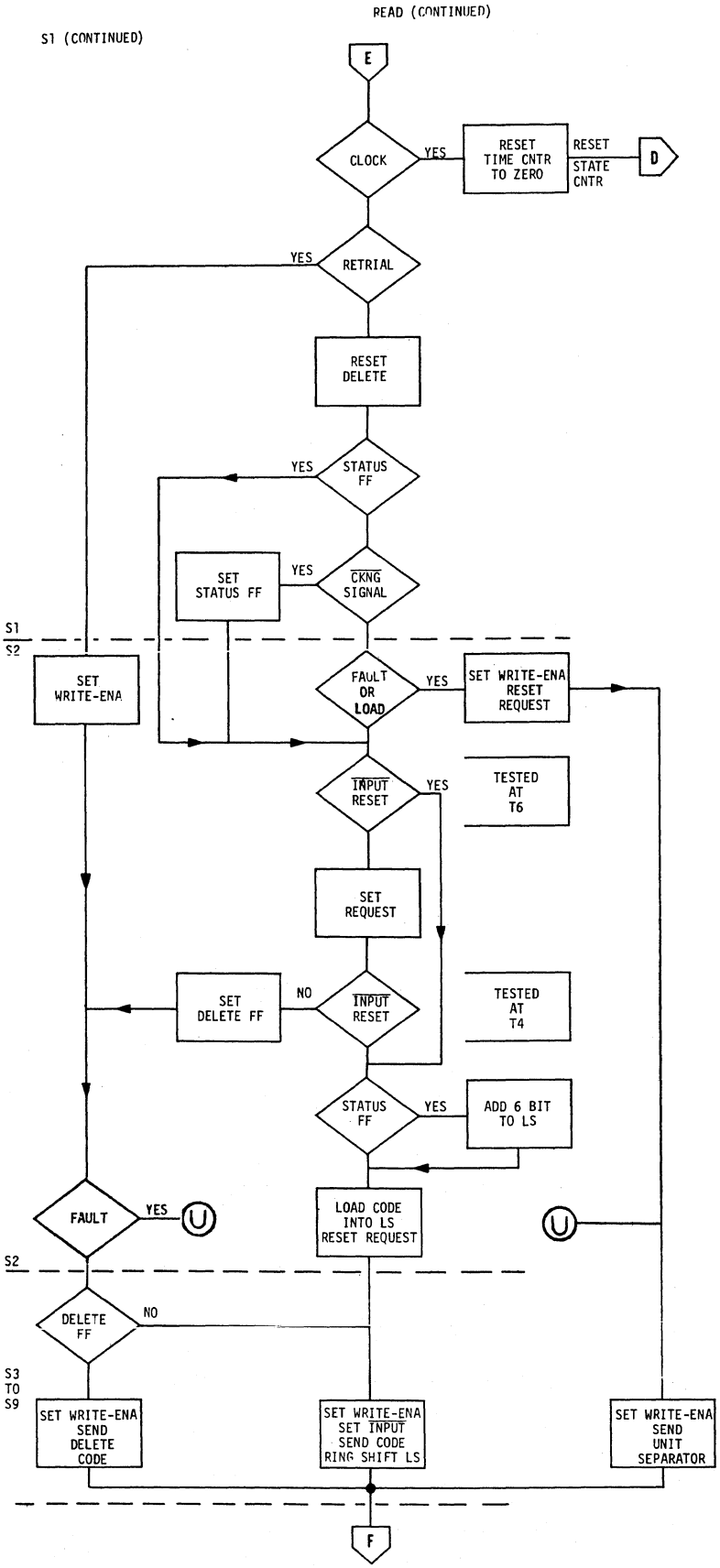


Figure 4-16 (Continued) D-284

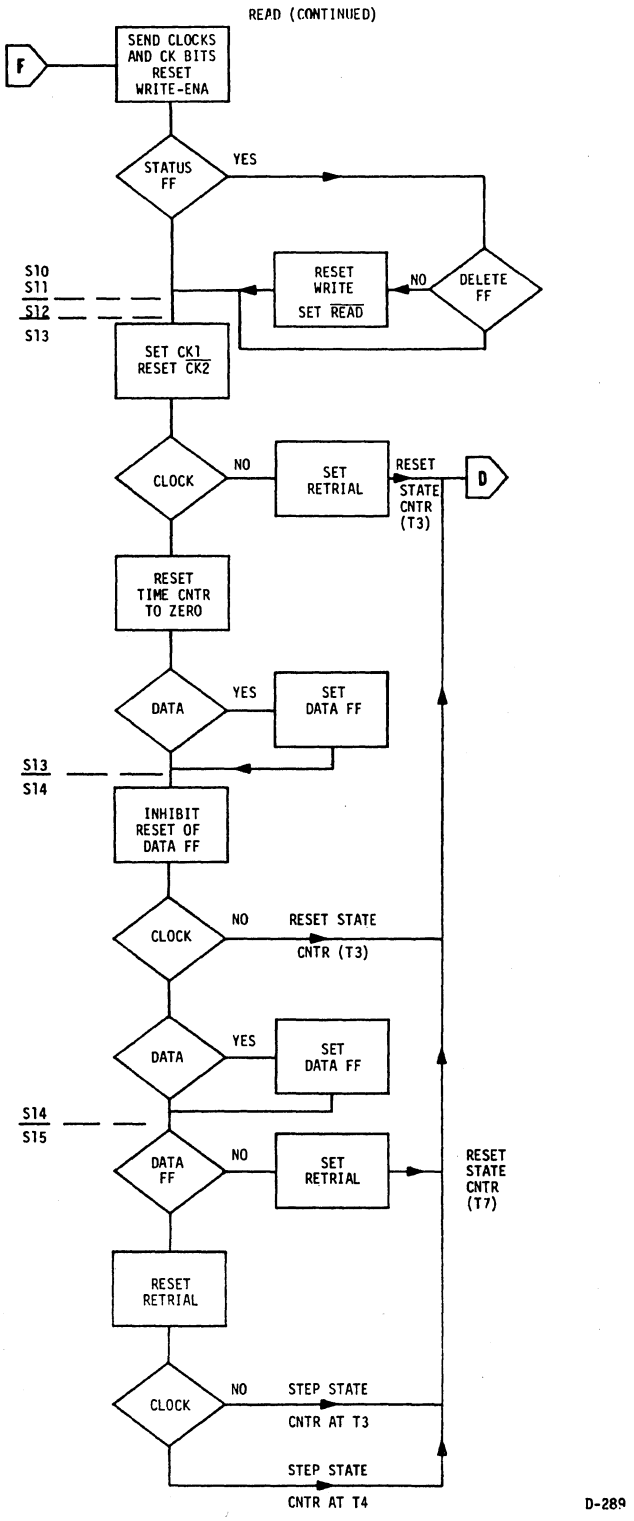


Figure 4-16. (Continued)

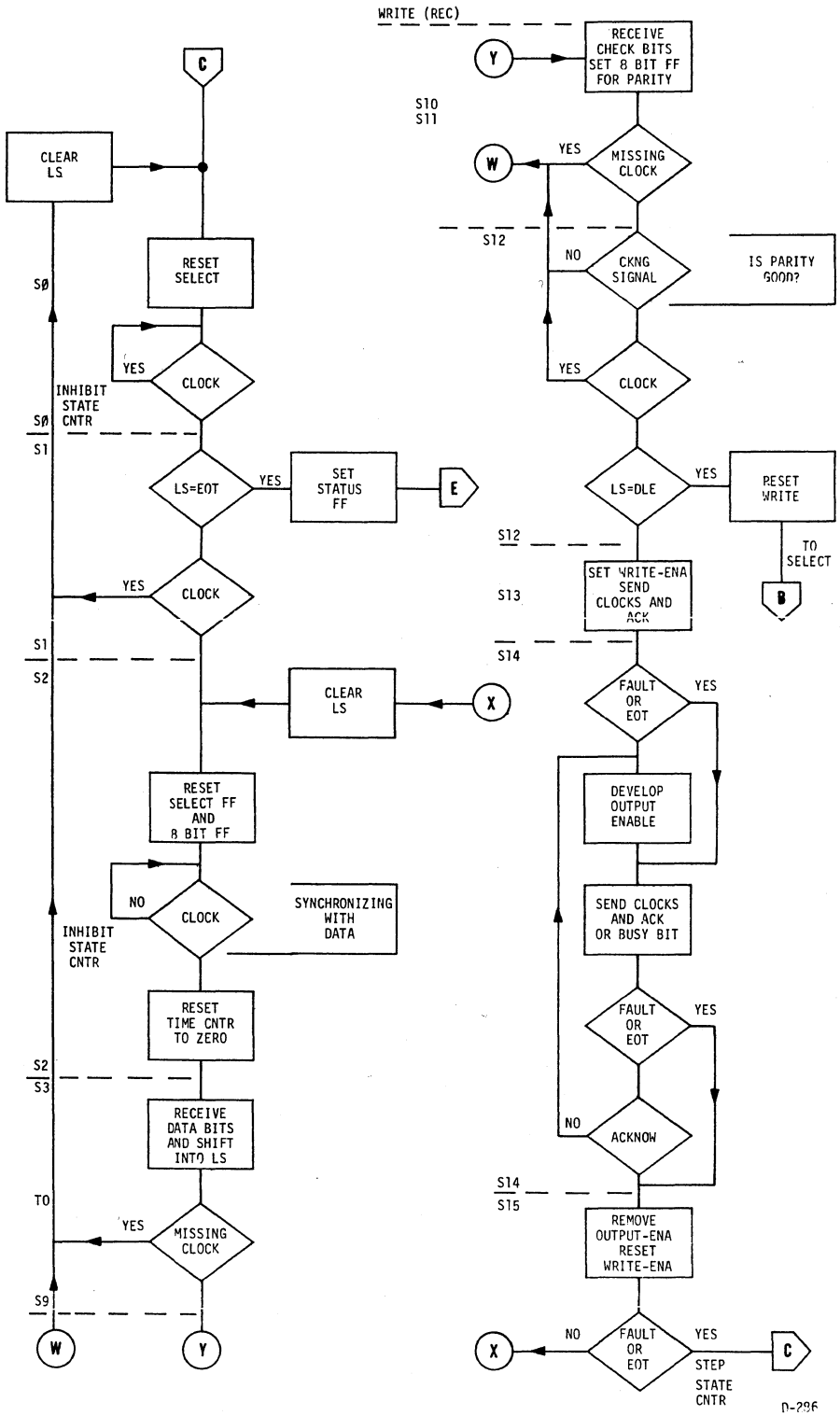


Figure 4-16. (Continued)

4-9.0 TEST POINTS

Figure 4-17 shows the card-edge test points that are available on the IOC and line unit. The line unit signals at TP3 and TP4, on LU1, are almost identical, except for the source point. The TP4 signal is a direct tap to the set side of the RETRIAL cross latch. There are no other connections to the set side of that latch. The signal at TP3 is inverted once from the reset side of the same latch. While the RETRIAL signal is used extensively, the inverted signal at TP3 is used (after another inversion) to qualify the input to the TIMEOUT flip-flop.

The remainder of the available test points are labeled with the signal name at the point of test.

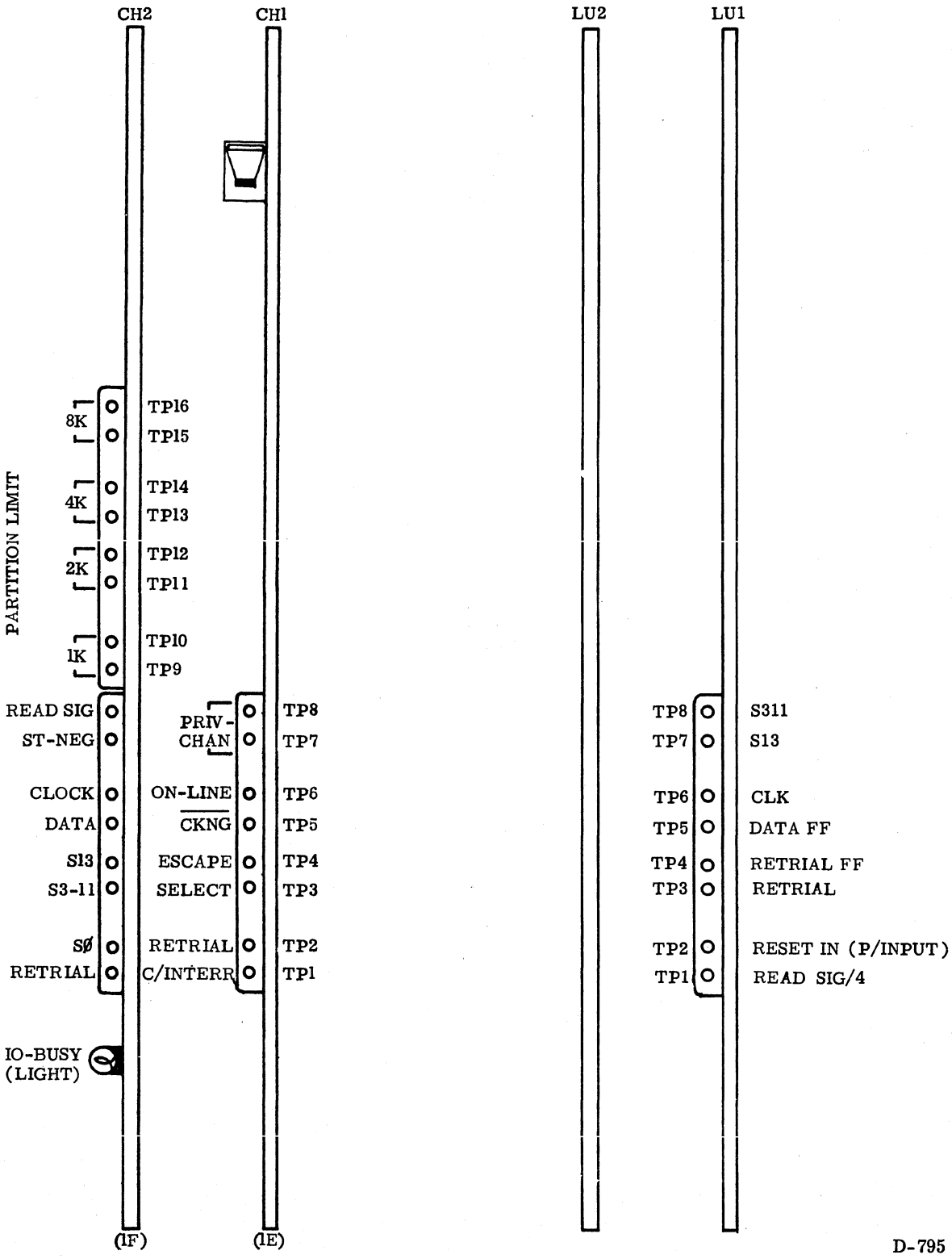


Figure 4-17. LINE UNIT & IOC TEST POINTS

4-10.0 MT IOC/LINE UNIT GLOSSARY

NAME	TYPE	SOURCE	DEFINITION/USE
CHECK	XL	CH1	Set by the ACU if an error is found in the software program. When CHECK has been set, the next instruction for that partition will be a READ CONTROL (LOAD).
CK1,CK2 CK1,CK2	Dffs Dffs	CH1 LU1	Test or generate character parity. The line unit flip-flops have additional duties (see PARITY FLIP-FLOPS in the main body of the text).
CLOCK CLOCK	XL XL	CH2 LU1	Set by detecting a transition on the two-wire line during T1. Verifies the beginning and end of each bit time of a character.
CONTROL	XL	LU1	Set when the decoded select character is a WRITE CONTROL, or a READ CONTROL instruction.
COUNT COUNT	Dff Dff	CH2 LU2	Enables an increment of the state counter at the proper times.
DATA DATA	XL Dff	CH2 LU1	Set by detecting a transition on the two-wire line during T5 (mid-bit). Indicates that a 1 bit has been received.
DELAY	Dff	CH1	Holds the IOC in S14 until the next T4 time after INT is reset by the processor.
DELETE	XL	LU1	Set when the line unit is to send a DELete character. The delete character is used to prevent timeout while the peripheral is accepting the received character.
EOT	XL	CH1	Set by LAST during a WRITE operation. Causes the IOC to send an EOT character to the line unit, indicating that the instruction character count is exhausted, and status is requested.
HOLD	Dff	CH1	A part of the CK1/CH2 parity detection circuit in the IOC. HOLD acts as a buffer for the parity circuit.
$\overline{\text{INPUT}}$	Dff	LU1	Indicates that the peripheral has a code ready for the line unit. $\overline{\text{INPUT}}$ resets to allow the code to enter from the peripheral.
IOS	SHREG	CH2	Shift register for the IOC.
IO BUSY	Dff	CH1	Set by the processor when an I/O select character is given to the IOC. IO BUSY remains set during the entire course of the instruction, as an indicator to the ACU that the IOC is still active with an I/O operation. The operation is ended when the IOC resets IO BUSY.

INTERR	Dff	CH1	Set by the IOC when a character must be transfered to, or from memory. The IOC always transfers only one character each time INTERRupt is set. INTERRupt is reset (cleared) by the ACU when the request is answered.
JUMP JUMP	Dff Dff	CH2 LU2	Loads the state counter with a binary two. This causes a jump to S2 when the state becomes active.
LAST	Dff	CH1	Set by the ACU when the instruction character count is exhausted.
LATCH LATCH	XL XL	CH2 LU2	Prevents repeated resetting of the time counter.
LOAD	Dff	CH1	Remembers the polling interrogation. If the polling question is acknowledged, LDRQ (another flip-flop) is set.
LDRQ	Dff	CH1	Set when device zero requests to load new instructions into memory. Reset when the ACU returns with a READ CONTROL select character.
LOCKOUT	XL	CH1	Prevents immediate re-use of the IOC by the same peripheral device. LOCKOUT is set after completing an operation, and must be followed by a polling pair.
LS	SHREG	LU1	Input/output shift register for the line unit.
POLL	XL	CH1	Starts a polling sequence. Once POLL is set, a poll must be made for service request, and another for load request. The two must be made, even if the service request poll was answered affirmatively.
POLL CNTR	DCTR	CH2	Determines the device (peripheral) that is to be polled for service request. The output of the poll counter is also gated to the processor for software use.
READ	XL	CH2	Set by a read select character.
$\overline{\text{READ}}$	Dff	LU1	Set when the line unit is receiving; reset when the line unit is transmitting.
REQUEST	XL	LU1	Signal to the peripheral requesting the next character.
RESET RESET	Dff Dff	CH2 LU2	Clears the state counter, causing a jump to SØ.
RESET-T RESET-T	XL XL	CH2 LU2	Resets the time counter.

RETRIAL RETRIAL	XL XL	CH1 LU1	Causes an unanswered transmission to be repeated (except during the polling sequence).
SELECT	XL	CH1	Set during the initial contact with a peripheral. It is set for each polling operation, and each ACU initiated select character.
SELECT	Dff	LU1	Set in S12 of the ESCAPE mode to allow the peripheral selection operation.
STATUS	XL	CH1	Set during the status collection procedure.
STATUS	XL	LU1	Set upon receiving an EOT code during a WRITE, or upon receiving two or more zeros during SØ of READ.
STATE CNTR STATE CNTR	BCTR BCTR	CH2 LU2	Creates orderly subdivisions of the operating modes. See the paragraph on TIMING for details.
STATE DCDR STATE DCDR		CH2 LU1	Decodes the binary count of the state counter, creating the individual signals needed for logic control.
SVRQ	Dff	CH1	Set by the IOC when one of the peripherals requests service. The IOC knows that service is requested when the polling question is acknowledged.
S410 S410	Dff Dff	CH2 LU1	Set during states four through ten. This is the period where data is sent or received.
$\overline{\text{TIMEOUT}}$	Dff	CH2	Triggered by T3 time, and qualified by an r/c circuit that is charged by the signal RETRIAL. If retrials are made, the circuit slowly charges to a level that allows $\overline{\text{TIMEOUT}}$ to reset.
$\overline{\text{TIMEOUT}}$	Dff	LU1	The same use and input circuit as the IOC flip-flop, but is triggered every T4 time.
TIME CNTR TIME CNTR	Dffs Dffs	CH2 LU2	Aseries of four flip-flops that create the bit times when transmitting or receiving characters.
TIME DCDR TIME DCDR		CH2 LU1	Decodes the output of the time counter, providing individual signals for logic control.
TURN	XL	CH1	Set during a READ operation if the ACU sets LAST. Causes the IOC to "turn around" and request status.
$\overline{\text{WINDOW}}$ $\overline{\text{WINDOW}}$	XL XL	CH2 LU1	Determines the time when line transitions are observed.
WRITE WRITE	XL Dff	CH2 LU1	Set during a WRITE operation.

WRITE-ENA	XL	CH1	Indirectly enables the line driver, allowing voltage to appear on the two-wire line.
WRITE TRANS	Dff	CH2	Controls the line transitions during data transmission.
WRITE TRANS	Dff	LU2	
XFF	Dff	CH2	
XDFF	Dff	CH2	Part of the general timing and sequencing logic
XFF	Dff	LU2	
XDFF	Dff	LU2	
XTAL CNTR	DCTR	LU2	A divide circuit that is used only when the line unit is patched for low speed operation.

SECTION 5

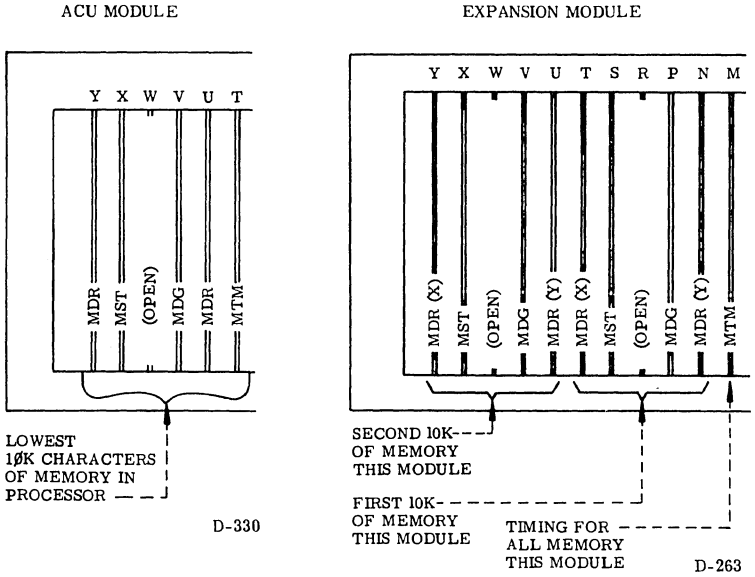
CONTENTS

LIST OF ILLUSTRATIONS

5-1.0 GENERAL

The model 20 processor main memory provides random access magnetic-core storage for a minimum of 10,000 6-bit characters, and can be expanded (within normal main-frame capabilities) to a maximum of 110,000 6-bit characters of storage. The basic 10K-character storage is physically located in the ACU module, along with the drivers, timing, and selection circuitry that is necessary for the memory to function.

There are four circuit card types that make up the main memory complex: MTM, MDR, MST, and MDG. As the memory capacity of the system is expanded, MDR, MST, and MDG cards must be added as a 10K unit. Two MDR cards are needed for each 10K unit, one for the X drive, and one for the Y drive (these drives will be explained in later paragraphs). Each expansion module that contains memory storage must contain one MTM card, but only one MTM card is needed for the maximum capacity (20K) of that expansion module. Refer to the figures below for the placement of the individual circuit cards. Memory cards will only be found in the ACU and Expansion modules, as the FAC module cannot accommodate core memory.



To avoid addressing problems, the memory capacity should be expanded in an orderly manner. If an expansion module is to contain only 10K of memory, the cards should be placed in the lower alphabetic positions (see the INSTALLATION section of this manual for details). The table below shows the capacity of each expansion module as the total system capacity is enlarged.

MEMORY CHARACTERS	ACU	EXP.#1	EXP.#2	EXP.#3	EXP.#4	EXP.#5
10K	10K	-	-	-	-	-
20K	10K	10K	-	-	-	-
30K	10K	20K	-	-	-	-
40K	10K	20K	10K	-	-	-
50K	10K	20K	20K	-	-	-
60K	10K	20K	20K	10K	-	-
70K	10K	20K	20K	20K	-	-
80K	10K	20K	20K	20K	10K	-
90K	10K	20K	20K	20K	20K	-
100K	10K	20K	20K	20K	20K	10K
110K	10K	20K	20K	20K	20K	20K

5-1.1 CORE MEMORY CYCLES

A core memory cycle always reads, then writes. The read process destroys the bit information in core, so if the data is to remain stored in memory, it must be re-entered during the write portion of the cycle. This is exactly what happens when the ACU is reading from memory for an internal operation, or to transmit a character during a software WRITE instruction. However, when the ACU enters new data into a core position, the area is "cleared" by the read portion of the core cycle, and the new bit is entered during the write portion of the cycle.

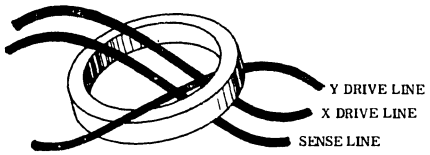
The ACU initiates a core memory cycle by activating CM-CYCLE/1, and the TMN card supplies all additional time sequences for the operation.

5-2.0 CORE MAGNETS

Magnetic core memory in the model 20 processor is an OEM (other equipment manufacture) product, and is un-repairable as such. However, memory cell failure is rare; most memory difficulties can be traced to faulty steering diodes, selection logic, timing circuits, or other problems. To best understand the supporting circuitry for the memory stack, it is advisable to know the basic workings, and requirements of the memory cell itself.

MAGNET OPERATION

The basic core magnet that is used in the model 20 memory stack is shown below in the simplified illustration of a single bit position. The doughnut shaped



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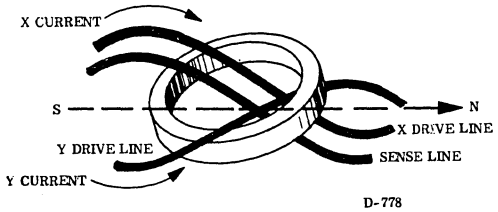
circle is a magnetizable ferrite material. This material is chosen because it resists partial magnetization. In other words, the core can be loosley compared to a flip-flop - it is polarized in one direction or the other, but never neutral. The wires shown running through the core are common to many other identical core bits, and are explained in later paragraphs.

To magnetize the core bit, current is passed through both the X and Y lines. Each line carries half of the magnetizing current. The effect is shown in the figure below. The magnetic force resulting from the two half-currents is illustrated



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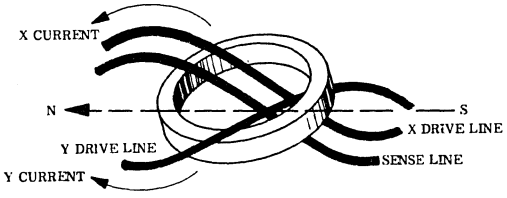
by the dotted arrow through the core.

By reversing the direction of current flow in both the X and Y lines, the North/South polarity of the magnet is reversed.



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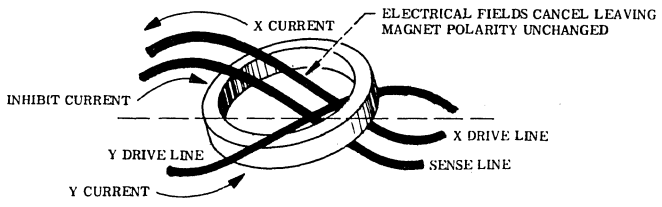
Notice, that the half-current of both the X and Y drive lines must be polarized in the same direction to reverse the magnet direction. A half-current in either the X or Y line, without the other line being active, will not change the polarity of the core magnet.

When information is to be entered into a particular core location, the X and Y lines are always activated as if to "charge", or polarize the magnet to a 1 bit. If the bit position is to be a zero bit, an additional current is passed through the dual-purpose sense/inhibit line. This current opposes the electrical field set up by the X drive, and effectively only the Y drive remains. Hence, the half-current of the Y drive alone is not suffecient to reverse the magnetic polarity.



5-3.0 CORE CYCLE OPERATION

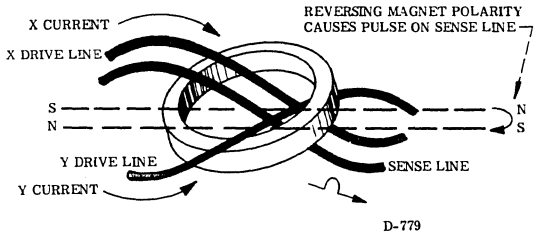
The memory cycle always reads the contents of the core (even ifthe information is not used), then writes into the same area. All six bits of a data character are read simultaneously, and written simultaneously. The terms "read" and "write" as used in reference to main memory, are opposite to the assumption gained from the operation, or function code within the ten character instruction word. The concept can be kept straight if the Arithmetic and Control Unit, ACU, is considered the basic unit. In other words, the ACU reads, and the ACU writes. During a WRITE instruction, the ACU reads from memory to write, or transmit, the character to an IOC or FAC device.

5-3.1 READ/WRITE

To read from core, the core magnet is charged (magnetized) in one direction. To write a 1 bit into the same core position, it is charged in the opposite direction. Both operations are identical, except for the direction of current flow. If the bit position is to remain a zero, the current flow is inhibited during the write portion of the memory cycle, and the core magnet remains charged in the read direction.

READ (EXAMINE CONTENTS)

During the read portion of the core memory cycle, the inhibit/sense line is monitored. When a core magnet is charged in the read direction, an impulse is generated by the reversal of field, if the core was previously in the write, or 1 bit condition. If the core was not previously a 1 bit, the magnet would already be polarized in the read direction, and no impulse is generated by the read portion of the cycle (see the figure below). In this way bits are retrieved from storage.



Many operations only want to examine the contents of core, not alter it. In those cases, an impuls comming from the core magnet, must be recorded (in a flip-flop or latch) during the read portion of the core cycle, and the information used during the write (record) portion of the cycle, to re-enter the 1 bit in that location.

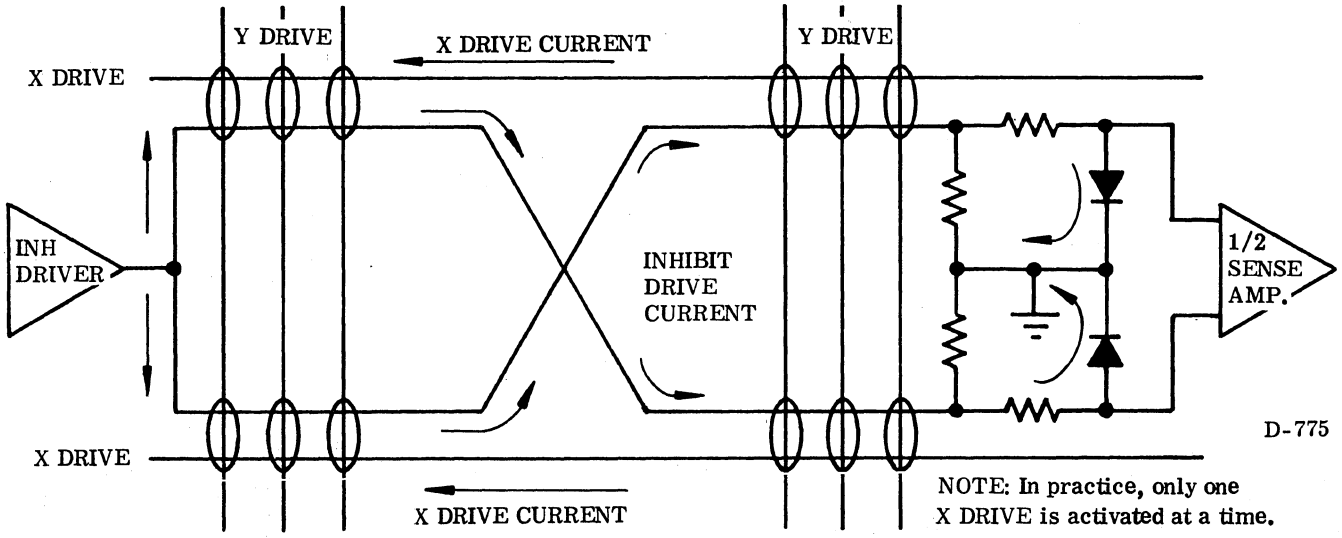
The read process in a ferrite core is "destructive", and data information must be re-entered during the write portion of the core cycle. If information is not re-entered, the core bit position will remain polarized in the zero-bit direction. However, remember that the recording of a 1 bit is the "natural" flow of events, and the inhibit circuitry must be working to record a zero bit.

WRITE (RECORD)

If data is to be entered into core without regard to what might be there already, the inhibit/sense line is not monitored during the read portion of the memory cycle. The read portion of the core cycle proceeds normally, polarizing the core in the zero direction. Then during the write (record) portion of the cycle, the bit information is stored. As explained earlier, a 1 bit is recorded by reversing the magnet polarity, and a zero bit activates the inhibit amplifiers, preventing the polarity reversal.

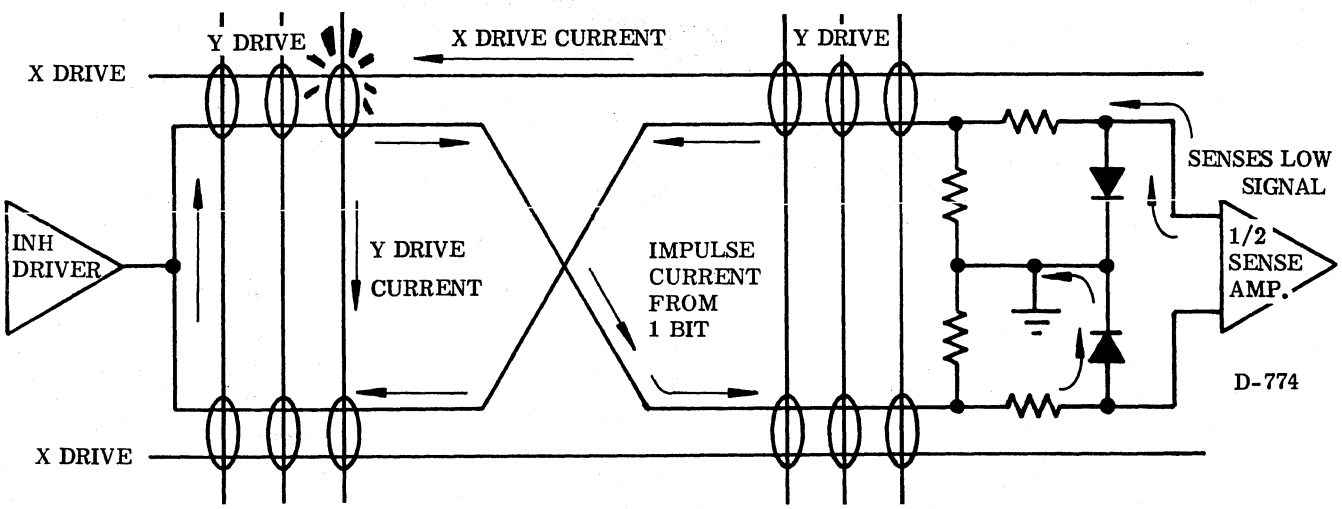
5-4.0 SENSE/INHIBIT LINES

During the write portion of a core cycle, Inhibit current is passed through the dual-purpose sense/inhibit line if the bit on that plane is not to be recorded as a 1 bit. The figure below shows a simplified illustration of the inhibit-current flow through the circuit, and how it is used to cancel the X drive current, and prevent magnetization of selected core positions. The sense amplifier is protected

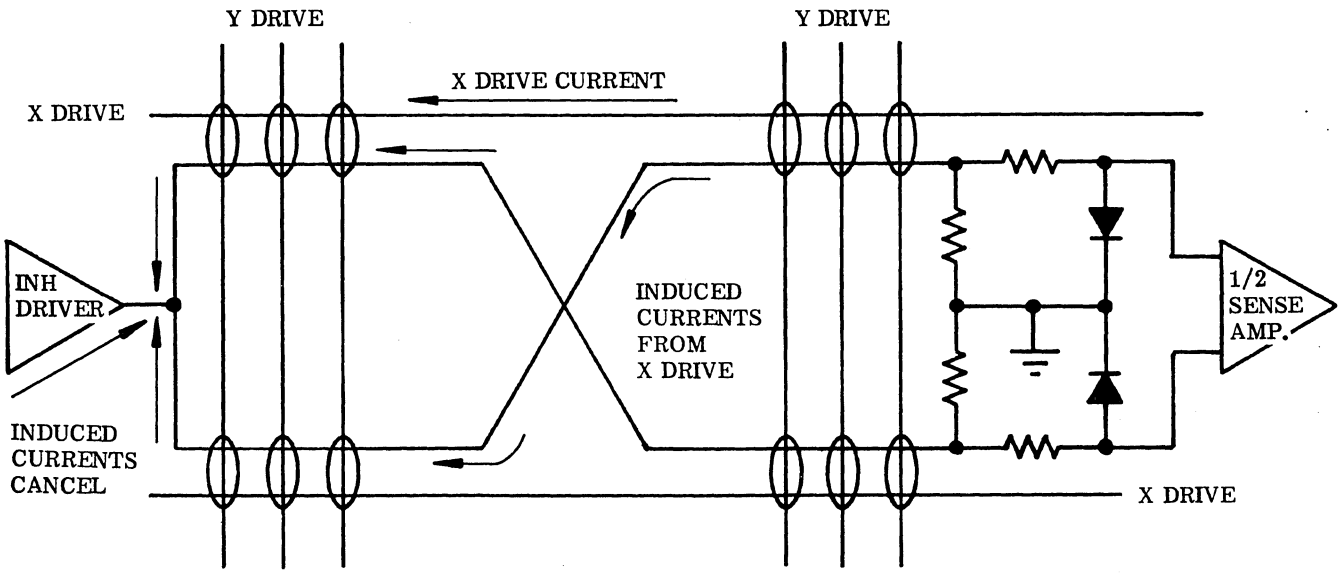


during this time by the two diodes in the entrance network. The diodes do not interfere with a read pulse during the read process, because the sense line is used as a loop at that time, and only one diode is needed at any one time. Either of the amplifier input legs can detect the negative-going read pulse, as it is the difference in voltage that supplies the amplifier input.

The following figure shows the path of an impulse that is detected from a 1 bit in core during the read portion of the core memory cycle. Notice that one diode completes the circuit to ground, while the other ignores the pulse. If a core position were selected from the other side of the loop, where the sense line is crossed, the 1 bit impulse would travel in the opposite direction. However, only the roles of the two diodes would be reversed, and the other leg of the sense amplifier would detect the impulse.



The sense/inhibit lines are crossed every 50 cores to prevent "false" bits from inductive pickup. Because the sense line and the X drive lines are parallel, an induced current is created in the sense line during the read portion of the core memory cycle. By crossing the lines, the induced current is canceled; the effect is shown in the illustration below. The sense amplifier that is used is a dual unit, and the portion that is shown in the figure represents only half of the actual unit. There six dual sense amplifiers for each 10K characters of memory storage.



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5-5.0 MAIN MEMORY LOGIC

Figure 5-1 shows a block diagram of the logic flow through the main functions of the main memory complex, and the interface signals from the ACU. Notice that main memory interfaces only with the ACU, and all addressing data transfers must pass through the ACU logic. Memory within the expansion modules is identical to the memory that resides in the ACU module; only the address selection numbers change from one physical location to another.

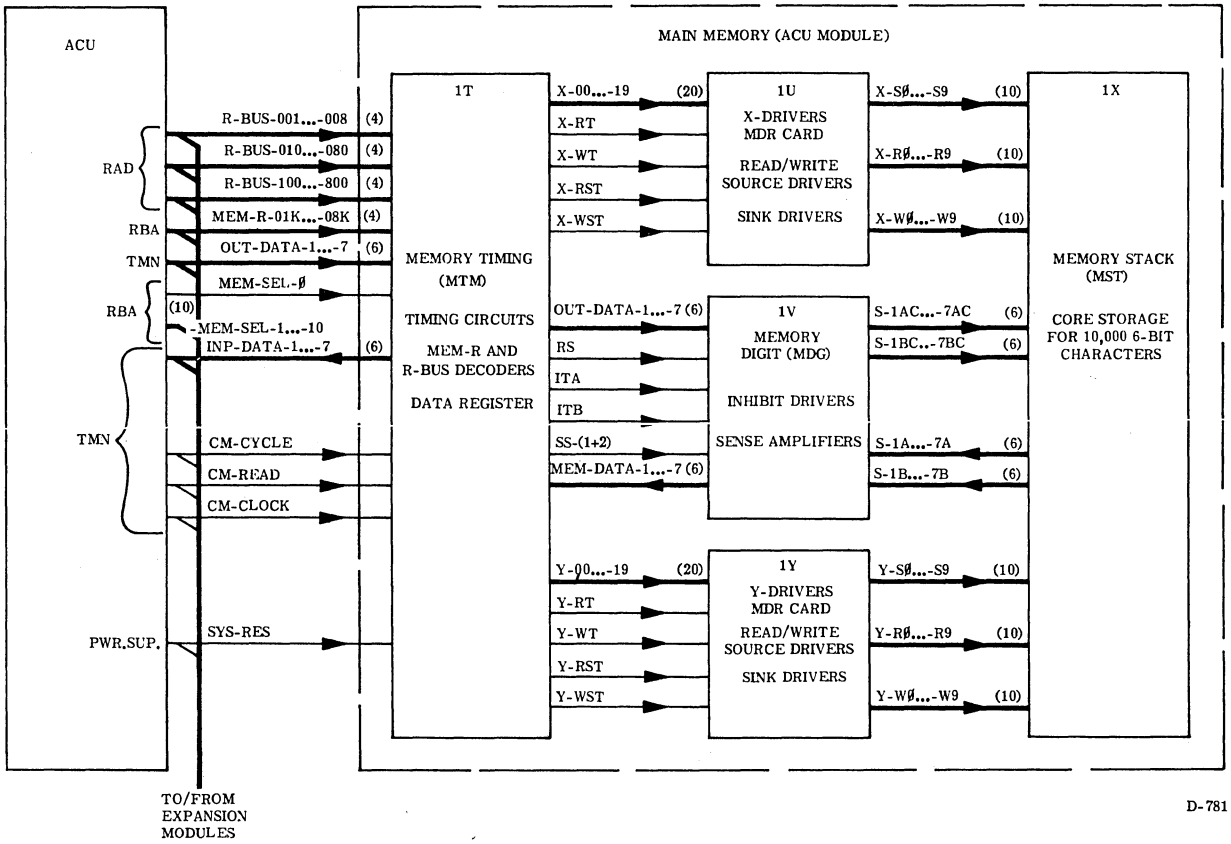


Figure 5-1 MAIN MEMORY BLOCK DIAGRAM

5-5.1 INTERFACE SIGNALS

Interface lines between the ACU and main memory carry all information that is necessary to select a character position in memory, examine that character, and record the same or different data in that location. The interface signal lines are listed below, and a brief description of the function that is performed by the line is given in the right hand column.

NOTE: The addressing described here is the actual memory address, not the relative partition address. The difference between the two types of addresses is discussed in Section 3 of this manual (Main Memory Addressing Structure).

ADDRESSING SIGNAL LINES

R-BUS-(001 - 800)	Three groups of four lines that provide the unit, tens, and hundreds digits of memory addresses in BCD form.

ADDRESSING SIGNAL LINES (Continued)

MEM-R-(01K - 08K)	Four lines providing the thousands digit of the memory address in BCD form.
MEM-SEL-(0 - 10)	Eleven lines that select one of eleven main memory modules. This is the ten-thousands digit of the memory address.

DATA SIGNALS

OUT-DATA-(1 - 7)	Six parallel lines from the ACU that supply one character at a time to main memory. The bits are named 1, 2, 3, 4, 5, and 7; the bit 6 portion of the ASCII character is not stored in memory.
INP-DATA-(1 - 7)	Six parallel lines from main memory that supply one character at a time to the ACU.

CONTROL SIGNALS

CM-CYCLE	A logic signal from the ACU to main memory, initiating a Core Memory cycle.
CM-READ	A logic signal from the ACU. This lead is activated to a logic 1 at the beginning of a READ operation. It is normally at logic zero, and remains at logic zero throughout a core memory WRITE operation. It is not related to the read and write portions (half cycles) that are part of every memory operation that is explained earlier.
CM-CLOCK	A continous 9Mhz square wave supplied to main memory from the ACU. It is derived from, and is in phase with the ACU-CLOCK timing signal.
SYS-RES	System Reset line that paralizes main memory during a manual reset, or power up and power down sequences. The signal produces Inhibit-Time-A (ITA/1) and Inhibit-Time-B (ITB/1). These two signals enable all of the inhibit drivers in the memory system, preventing memory alteration during reset.

5-5.2 MAIN MEMORY CIRCUIT CARDS

Each main memory circuit card performs one or more specific operations of the memory storage and retrieval process. The following paragraphs give a brief description of the duties and the contents of each card type.

MDR

The Memory Driver card (MDR) supplies all of the sink drivers (groups of ten lines) and source drivers (individual lines) with the current that is needed for one drive axis. There is one MDR card to drive the X axis, and one to drive the Y axis. The driver circuits are discrete component switching amplifiers, one driver for each sink line, and one for each source line. All of the drivers on a single MDR card draw from one current regulated source, that is part of the MDR circuitry. This regulator is carefully maintained at 300ma, and could cause unreliable memory action if the regulator circuit is not working properly.

MDG

The Memory DiGit card (MDG) contains the inhibit drivers and sense amplifiers that determine the Ø or 1 bit-record in the selected position of core. There are six dual-sense amplifiers and twelve inhibit drivers. The sense amplifiers are integrated circuit chips, but the inhibit drivers are discrete components.

One inhibit driver and one-half of one dual sense amplifier supply the bit information for one 5,000 bit core matrix (bit plane). In other words, a bit plane is one character-bit position in each of 5,000 seperate memory addresses.

MTM

The Memory Timing (MTM) card supplies all memory timing for one processor module. It also decodes memory selection information, and passes it to the driver circuits. Data pulses from the sense amplifiers (on the MDG card) are also given to the MTM card for temporary storage in cross latches. The data is stored long enough for the ACU to accept it on the INP-DATA lines.

The MTM receives the master timing signal, CM-CLK/6, from the ACU. It also receives the command for a core memory cycle from the ACU (CM-CYCLE/1). CM-CYCLE/1 can be tested at test point 1, in the terminal block on the MTM card.

Timing and interface signals comming from the MTM card are listed on the following page. A simplified illustration of some of the main timing elements is shown in figure 5-2.

MTM SIGNALS

X-00 to -19	The X-00 to X-09 signals select one of the ten X read/write source drivers. These signals are the output of a one-in-ten decoder, the input of which is the units digit (in BCD) from the R-BUS. X-10 to X-19 signals select one of the ten X read/write sink drivers. These signals are the outputs of a one-in-ten decoder, the input of which is the tens digit (in BCD) from The R-BUS.
X-RT	X-Read Time is a memory timing signal that enables all X read source drivers during the read portion of each memory cycle.
X-WT	X-Write Time is a memory timing signal that enables all X write source drivers during the write portion of each memory cycle.
X-RST	X-Read Source Time is a memory timing signal that enables all X read sink drivers during the read portion of each memory cycle.
X-WST	X-Write Sink Time is a memory signal that enables all X sink drivers during the write portion of each memory cycle.
Y-00 to -19	The Y-00 to Y-09 signals select one of the ten Y read/write source drivers. These signals are the output of a one-in-ten decoder, the inputs to which are the hundreds digit (in BCD) from the R-BUS. Y-10 to Y-19 signals select one of ten Y read/write sink drivers. These signals are the output of a one-in-ten decoder, the input to which is the thousands digit from the base adder (MEM-R-01K to -08K).

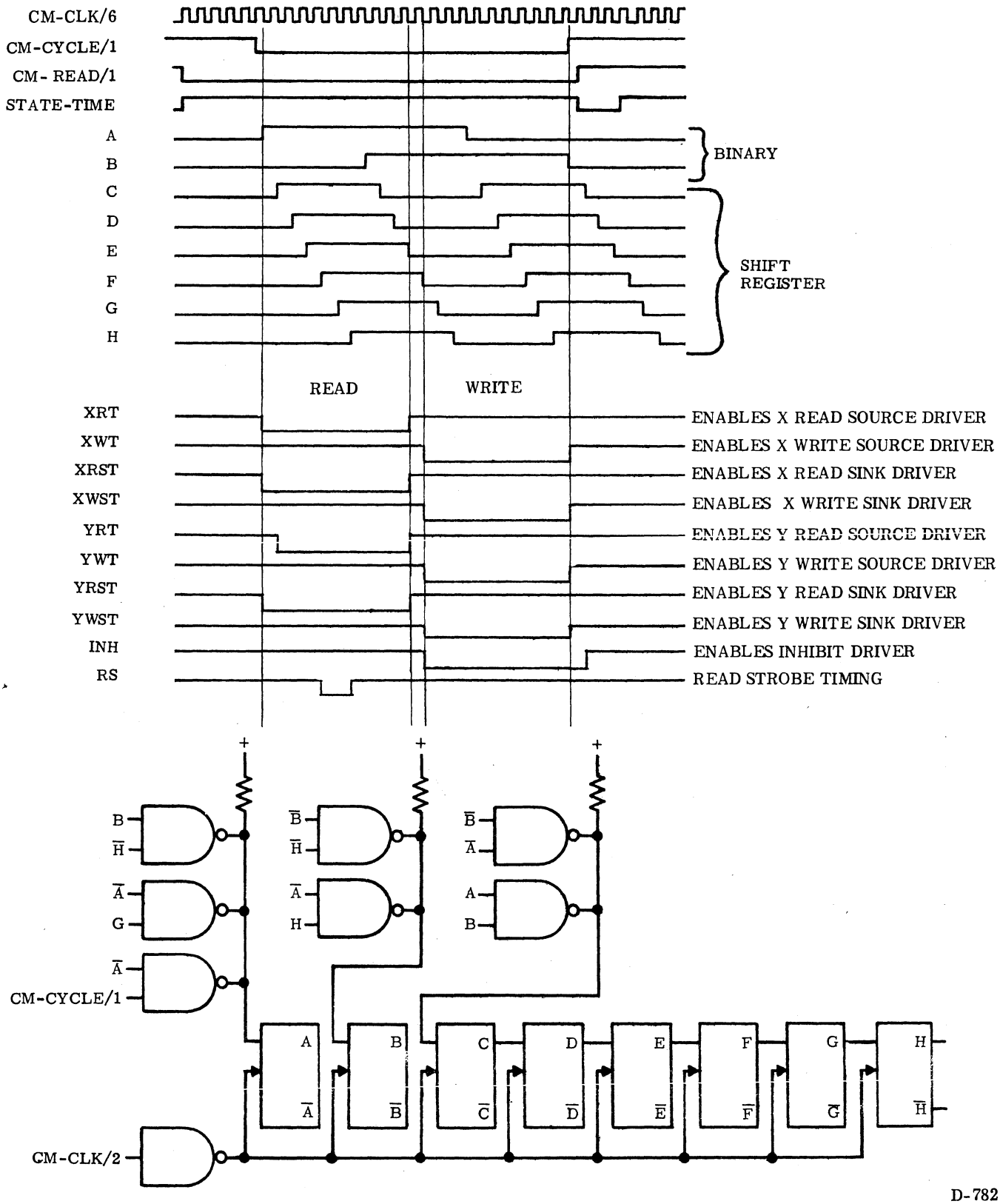


Figure 5-2 MAIN MEMORY TIMING

5-2.2 MAIN MEMORY CIRCUIT CARDS (Continued)

MST

At present, two configurations of MST cards are used in the model 20 processor. They are interchangeable without adjustment of any kind. The physical appearance is slightly different, but they are electrically identical.

The MST card contains the actual memory cores for ten thousand characters, and the steering diodes that seperate the read and write functions in that group of cores. The core matrix is arranged in six mats of 10,000 bits each, where one bit in each of the six mats is selected simultaneously. Because each mat has its own sensing and inhibit circuit, the selected bits can be recorded, or read seperately (not seperately in reference to time, but each bit contains individual information).

An individual character address (the same location on each 10K mat) is located by activating the proper source and sink drivers. This process is described in a later paragraph, titled Address Selection.

Each 10K core mat contains a sense/inhibit line that threads through every core in that mat. The sense line parallels the X drive lines, and physically crosses to a new line after every 50 cores.

5-6.0 ADDRESS SELECTION

To locate an address in main memory, five selection decisions are made: the memory stack, Y sink driver, Y source driver, X sink driver, and X source driver.

The MEM-SEL signal selects the proper memory stack. This is really selecting one of eleven possible MST cards that are distributed throughout the processor mainframe. Each MST card represents and contains all addresses within a ten thousands digit of memory addressing. For example, the third MST card (located in expansion module number 1) would contain all addresses from 20,000 to and including 29,999. The 10K digit is a single memory module selection, as already stated. However, the remainder of address selection takes place simultaneously on each of the six memory bit-planes.

The Y sink switches, activated by decoded MEM-R-01K to MEM-R-08K signals from the ACU, select one of ten groups of ten Y drive lines. Each selected Y sink group represents and contains all of the possible addresses within the particular thousands digit. For example, if the sixth Y sink group is selected, any address is available between 5,000 and 5,999 inclusive. Remember that this address is completely within the MST card that was selected by the 10K digit. The Y sink groups are not physically located in numerical order, but do have a progressive sequence (see figure 5-3).

The Y source switches select an individual Y drive line. This completes the Y portion of the addressing selection. The desired address can be any of the 100 cores along the selected Y drive line.

The X sink switches select one of ten groups of ten X drive lines. Each of these X sink groups contains the addresses within the tens digit selected. For example, X sink group 3 contains addresses 20 to 29 inclusive. The X sink groups, like the Y sink groups, are not physically located in numerical order (see fig. 5-3).

An individual X drive line is selected by the X source switches. The intersection of of the X drive line and the selected Y drive line is the unique core bit that was specified by the address.

Address selection is simultaneous in all six of the bit planes (areas) of core, for each character that is read into or written from core. The read and write drivers are common to all six of the bit planes, and always activate the read current, then the opposite-flowing write current in all six bit planes during each core memory cycle (see MEMORY TIMING). Sense amplifiers and inhibit drivers, however, are unique to a particular bit plane, so that the bit information can be read seperately, and the indivudal lines can be inhibited as needed during the write portion of the core cycle.

Figure 5-4 is an expanded illustration of the addressing and sense/inhibit circuitry on a portion of the MST card. The sense amplifiers and inhibit drivers are not a part of the MST card, but are shown here to gain an overall concept of the memory scheme.

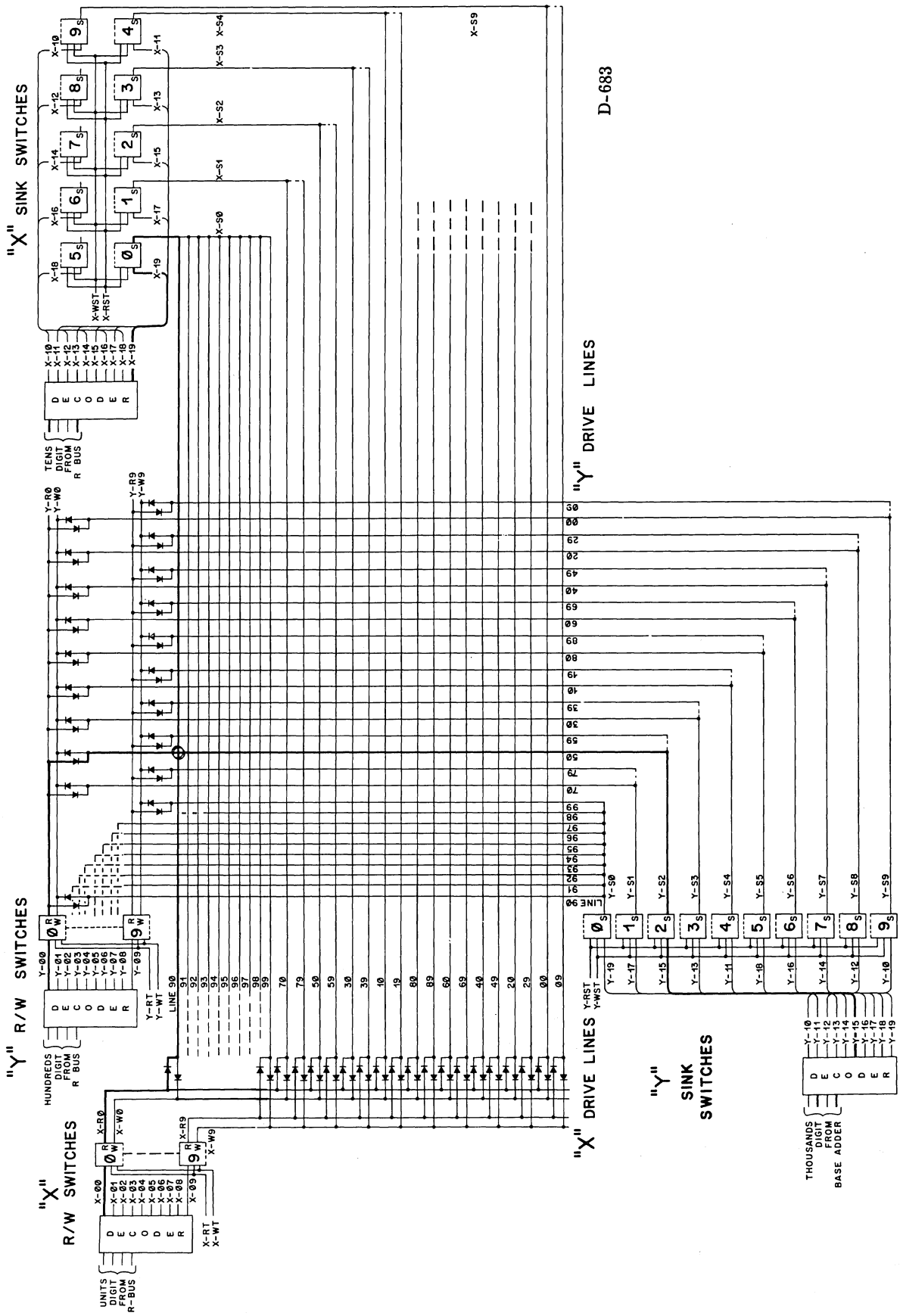


Figure 5-3 MEMORY SELECTION, BLOCK DIAGRAM

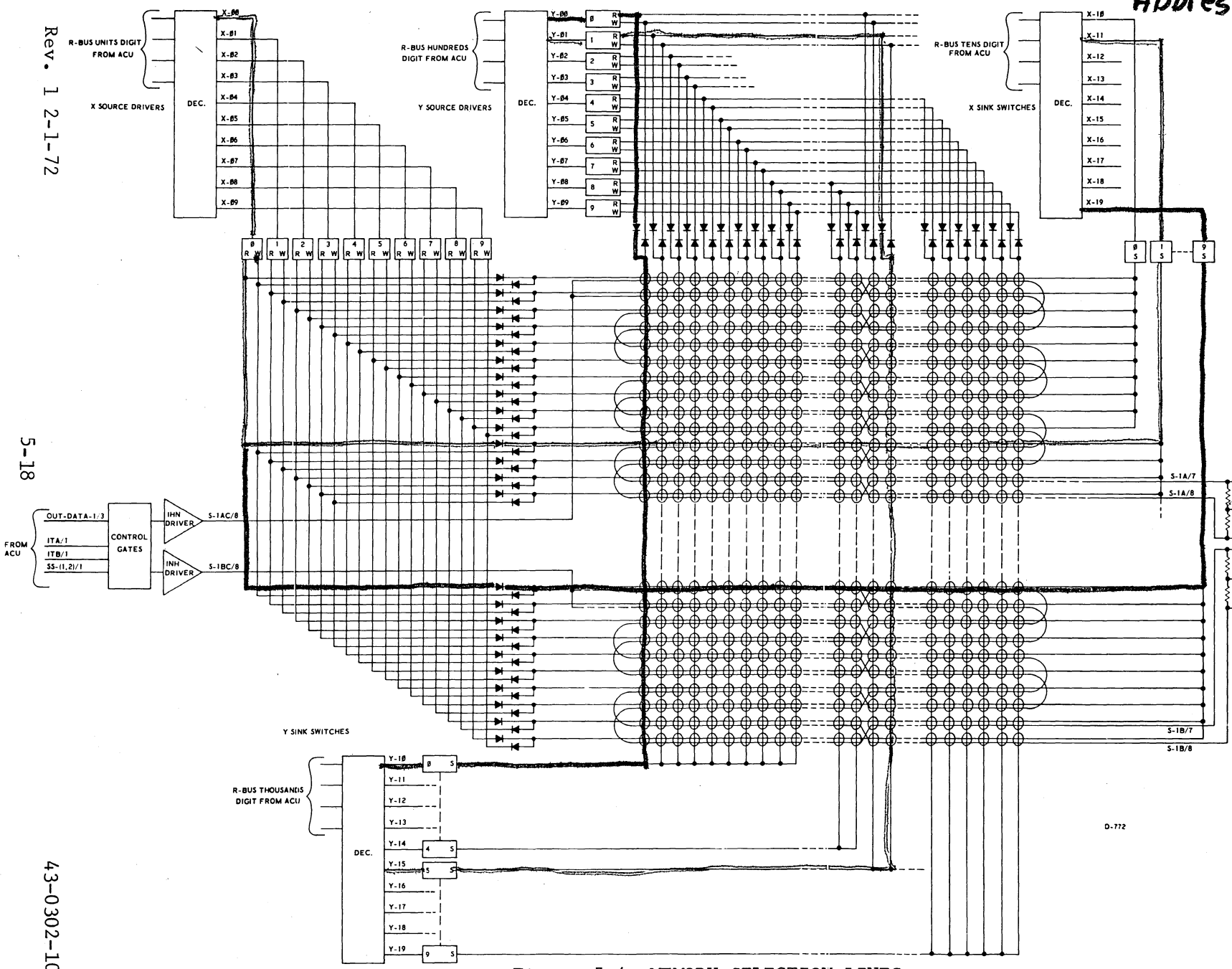
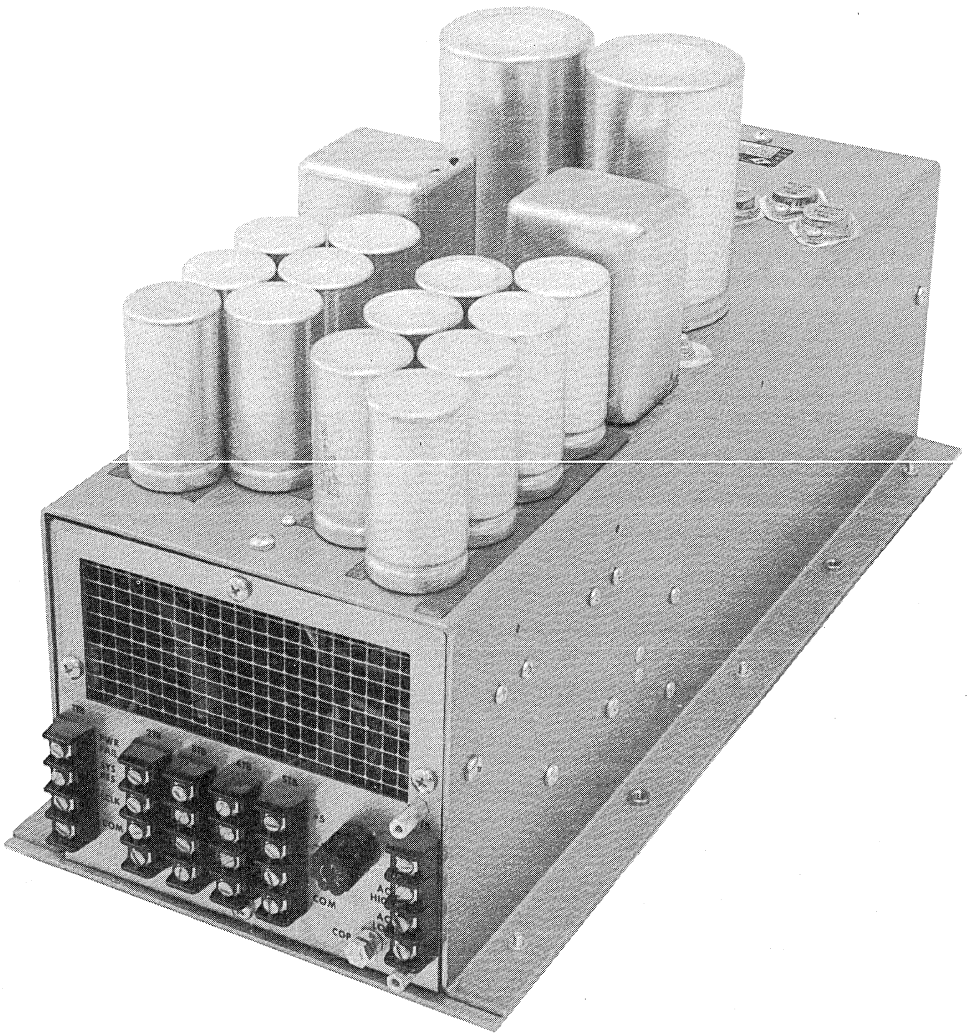


Figure 5-4 MEMORY SELECTION LINES

SECTION 6

9001306 PROCESSOR POWER SUPPLY

SECTION CONTENTS



THE 9001306 POWER SUPPLY

FIGURE 6-1

SECTION 6, 9001306 PROCESSOR POWER SUPPLY

A. GENERAL DESCRIPTION

The 9001306 Processor Power Supply, Figure 6-1, is a high-current, low voltage regulated supply. It is designed to be mounted in the Processor console. It operates from a single phase, 115-volt, 50- or 60-Hz power line, and produces three separate output voltages. It also produces two logic signals used for sequencing purposes during power-up and power-down cycles to ensure automatic and safe turn on and turn off, and a timing signal.

The output voltages developed are +5 VDC, +15 VDC, and -12 VDC. The two logic signals are called System Reset (SYS-RES/7) and Power Fail (PWR-FAIL/7), and the timing signal is Line Clock (LCLK/8). System Reset exists in the active state (low) when the DC output voltages are almost below specified tolerance. Power Fail is active (low) when the AC line has dropped below 93 volts. Because the regulated supplies have large energy storage, the outputs will stay up for a brief time even when the AC line voltage is falling rapidly. Line Clock is a pulse train at line frequency (60 Hz) with about a 50% duty cycle.

B. INPUT/OUTPUT SPECIFICATIONS

The supply is designed to operate on a line voltage of 94.5 to 132 volts. The regulating circuits are designed to accommodate this range of input voltage. When operating normally, the supply is designed to draw about 7 amperes from the AC line (this is, of course, a function of load). The power line is fused for 10 amperes. Each unit is equipped with a normally-closed thermal switch in the AC input line that will open if the ambient temperature rises above 140°F. Operating temperatures are from 0°C to 60°C (32°F to 140°F). Storage temperatures are from -51°C to 71°C (-60°F to 160°F). In both cases the relative humidity may range from 5% to 95%.

Figure 6-2 illustrates the power output ranges for the three DC circuits.

	+5	+15	-12	UNITS
VOLTAGE	+5	+15	-12	VOLTS
ADJUST RANGE	±3%	±2%	NA	
REGULATION	±3%	+1.2%	++17%	
OVERVOLTAGE TRIGGER	125±10%	125±10%	NA	
REVERSE VOLTAGE PROTECTION	YES	YES	NA	
CURRENT	30	11	4	AMPS
STATIC LOAD	0-100%	0-100%	0-100%	
DYNAMIC VARIATIONS	25%	5 AMP	25%	
TRANSITION TIME	10	1	10	μSEC
OVERCURRENT PROTECTION	YES	YES	YES	

POWER OUTPUT SPECIFICATIONS

FIGURE 6-2

The +5-volt and the +15-volt outputs are protected with an overvoltage circuit (SCR crowbar). The crowbar will trigger at the voltage thresholds shown in Figure 6-2 for internally or externally caused overvoltages. The crowbar operation turns off the control units and latches so that interruption of the AC input power is necessary for a restart. All three outputs are protected against short circuits (overcurrent) to the extent that the power supply will not be damaged by such occurrences on any or all outputs.

C. LOGIC SIGNALS

During system turn on, SYS-RES/7 and PWR-FAIL/7 should be active (low) before any of the regulated DC outputs reach one volt. When all DC outputs are up to normal value, SYS-RES/7 goes high. PWR-FAIL/7 then goes high one msec or more after this. The total turn on time, from application of input power to PWR-FAIL/7 going high should be less than two seconds.

During system turn off, PWR-FAIL/7 goes low when loss of input power is detected. After PWR-FAIL/7 goes low, at least 20 msec must elapse before SYS-RES/7 goes low. SYS-RES/7 goes low just before any of the power outputs go out of normal operating tolerance.

D. CIRCUIT DESCRIPTION

A block diagram is shown in Figure 6-3. The AC input is rectified and filtered to produce 150 VDC which is applied to both regulators. The +5 VDC and +15 VDC outputs are sensed, and the control units initiate a "pump-up" cycle if the outputs fall below their nominal value. Also shown is the auxiliary supply (+AUX) consisting of a small transformer and rectifier. A portion of the 60 Hz output of this transformer supplies the line clock (LCLK) trigger.

Certain signals are generated for use wholly within the power supply itself. Several of these are listed below.

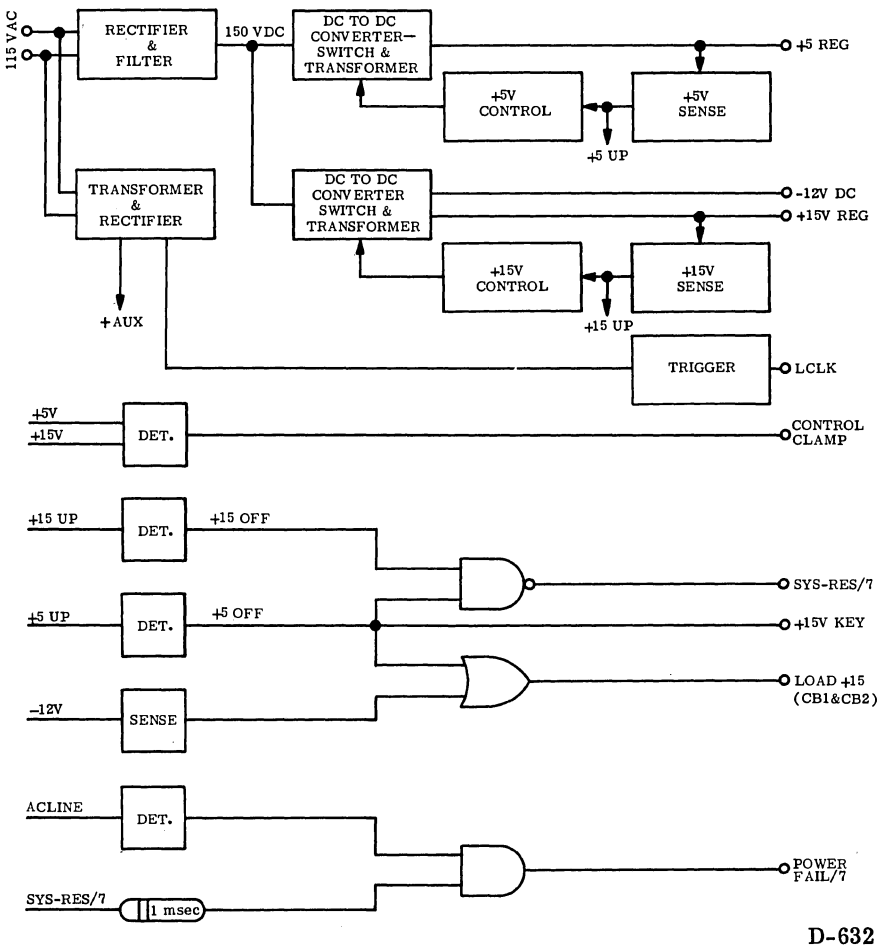
(1) CONTROL CLAMP: Inhibits +5VDC or +15 VDC control signals.

(2) CB1 and CB2: Loads +15 VDC output with extra 1.5 amp.

(3) PULSE WIDTH: DC level to increase or decrease length of on-time part of duty cycle.

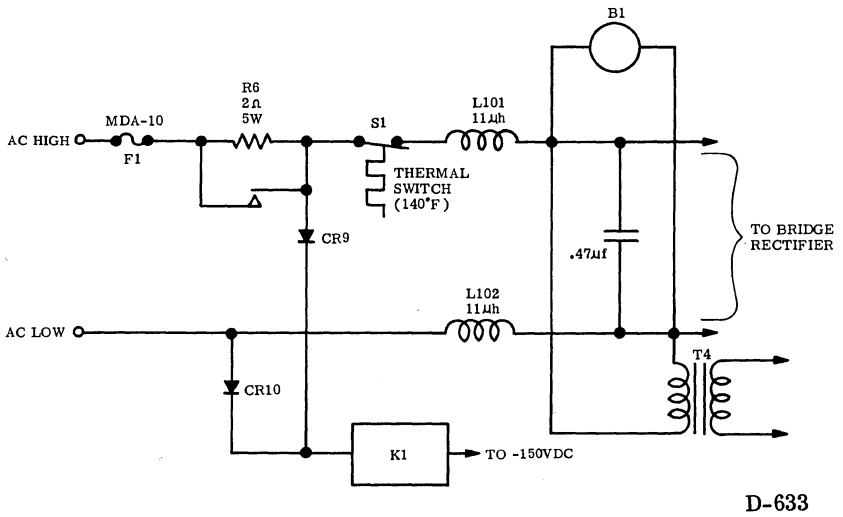
(4) +15V KEY: Inhibits +15 VDC control unit.

(5) +5V UP and +15V UP: Signals developed when supply is low to initiate a pump-up cycle.



BLOCK DIAGRAM

FIGURE 6-3



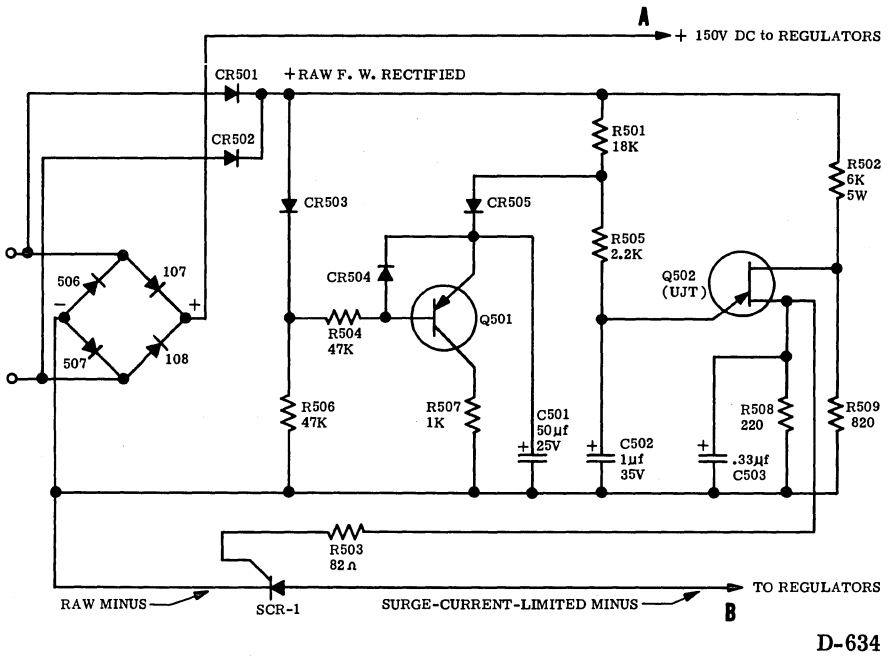
INPUT CIRCUIT

FIGURE 6-4a

1. AC INPUT CIRCUIT

The power line is connected to two terminals of a four-terminal connector, labeled AC HIGH and AC LOW. The high side is fused for 10 amperes as shown in Figure 6-4a. The 2-ohm resistor limits initial input current and is bypassed by the relay when line current settles down. (In later models this relay and 2-ohm resistor are replaced by a silicon-controlled rectifier: see description below.) Also in the high side of the line is the thermal switch which opens if the ambient temperature rises to greater than 140°F. Two 11 μh inductances and a .47 μf capacitor function to reduce switching transients generated within the supply. Directly across the line at this point is the blower motor, used to circulate cool air through the supply.

The surge-limiting circuit, shown in Figure 6-4b, replaces the relay, and is factory installed in serial numbers 9682 and up; it may be installed as a modification on 9615 and below. Two additional diodes, CR501 and CR502, provide full-wave rectified voltage for the circuit. With 115 VAC at the input line, the peak rectified voltage rises to 163 volts at this point.



SURGE LIMITING CIRCUIT

FIGURE 6-4b

Circuit operation revolves around the silicon-controlled rectifier, SCR1. When power is first applied, the SCR is not allowed to fire until very late in the half cycle, perhaps at 175°. The main power supply storage capacitors, C19 and C20, can accept only a small charge, since the line voltage is very small at this time. For the next several half-cycles, the SCR is turned on earlier and earlier and therefore the storage capacitors charge gradually toward their final value. Without this circuit action, the inrush, or surge, current would be very large. When the DC voltage has stabilized, the SCR is then fired at about 70° or 80° all during normal operation.

The gate of SCR1 is fired from Q502, the unijunction transistor. Q502 turns on and fires SCR1 when C502 has charged up to a value high enough to forward bias the emitter of Q502. The voltage to which C502 can charge during each half cycle is determined by the voltage across C501. When power is first applied, C501 "steals" charging current away from C502, preventing any appreciable C502 voltage. C502 charges up more slowly than it otherwise would, and this alters the turn-on point of the UJT relative to the full-wave rectified voltage. After approximately 1 second, C501 charges to a value that reverse-biases CR505, and then Q502 operates every 70° or 80° every half-cycle.

Q501 has the primary purpose of limiting the ultimate voltage across C501 to a value only slightly more positive than the ultimate voltage across C502, thus ensuring that CR505 is back-biased, and C501 is kept out of the UJT circuit after the supplies are up to their nominal value.

2. +5-VOLT REGULATOR

In this power supply, regulation is accomplished by the method known as "Self-oscillating Switching Regulation". A switching regulator operates much differently than the more conventional series or shunt regulator types. The following description is given to help the reader understand the basic principles of switching regulators, and should not be interpreted as being necessarily a description of the Friden power supply. Following the general description, the Friden supply is then discussed in detail.

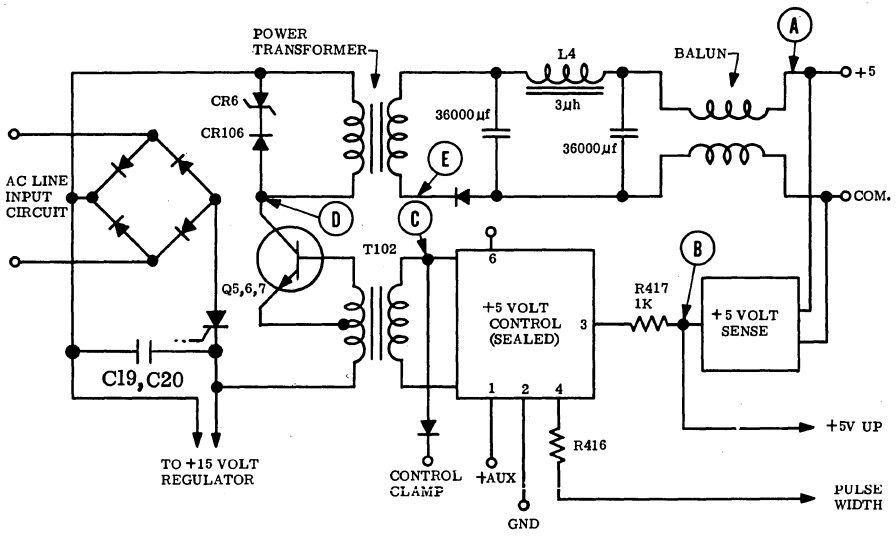
a. SWITCHING REGULATOR PRINCIPLES. Switching regulators in general operate on the principle of the average value of a train of rectangular pulses. For example, a perfectly symmetrical square wave (50% duty cycle) operating between ground and +10 volts has an average DC voltage of 5 VDC. By varying the duty cycle, the average DC value will be changed. A 33% duty cycle will produce an average of 3.3 volts; a 75% duty cycle yields 7.5 volts, etc.

Generally, switching regulators operate upon this principle, with additional circuitry that senses the regulated output and a control circuit that determines if, and when, a switching cycle is required. The sense circuitry determines whether or not the output has fallen below some predetermined value, and if so, it generates a signal to signify this fact. The control circuit then turns on the switch and initiates the "pump-up cycle". Now, with the switch closed, the DC source is connected to the regulator output, and the output rises.

Several basic methods of implementing this circuit action are used. In one, the regulated output itself determines when the switch goes on and when it goes off. This circuit, called a "Self-oscillating Switching Regulator", produces switching cycles that have variable on and off cycle lengths. In another circuit, the modified self-oscillating type, the switch-on time is relatively fixed, while the off time is determined by the regulated output. Still another circuit, the "Synchronously-driven" type, uses an externally generated sawtooth or triangular waveform to be compared with the regulated output. A comparison amplifier is used to compare each voltage, and the intersection of the sawtooth with the regulated output determines the duty cycle.

While the details of circuit operation differ in the various circuits, they nevertheless operate on the fundamental principle of the average value of the output (switched) waveform, with some types having additional provisions for energy storage during the off time.

b. PROCESSOR POWER SUPPLY. The processor power supply operates as a fixed-length switching regulator (modified self-oscillating type). However, many additional features have been added to make it compatible with the overall system requirements. A simplified diagram is shown in Figure 6-5. The +5 VDC regulated output is sensed by a voltage detector, and when the output falls below an acceptable value, the signal +5 UP is generated. This signal is presented to a sealed control unit, and a fixed-length pump-up cycle is initiated. The actual switch-on time is on the order of 25 or 30 μsec. During this time, the power transformer is used to store this pulse of energy in its core: the transformer is "loaded" by energizing its primary winding.



SIMPLIFIED 5-VOLT REGULATOR

FIGURE 6-5

The switch is then turned off, and the stored magnetic energy is allowed to discharge (or "dump"), not back into the switch, but rather into the transformer's secondary circuit, thus increasing the sagging output voltage. If the load is very heavy, another cycle is initiated very quickly, but if the load is light, the next cycle will not start for a relatively long time, when the output falls too low again.

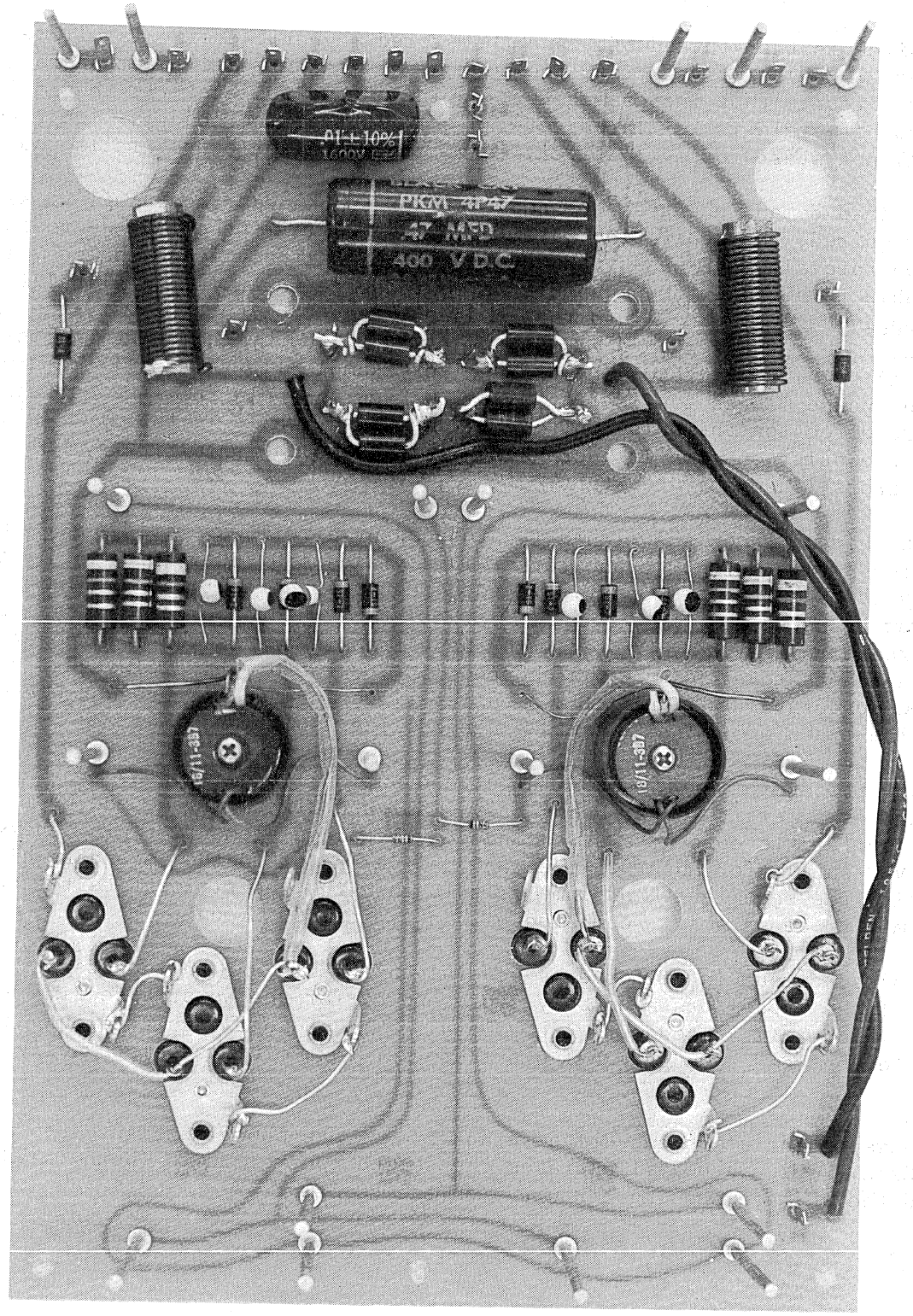
As the load demand changes, the repetition rate changes accordingly. As more current is required, the repetition rate increases, while if the load decreases, the repetition rate also decreases. However, as the AC line voltage changes, it would be desirable to be able to compensate to some degree for this. A signal is generated in the supply called Pulse Width that causes the control unit to vary the "fixed" on time such that the regulated output is not affected by the changing line voltage. That is, if the line voltage is constant, for example 115 VAC and it remains at this value, the pulse length is fixed at 25 to 30 μsec. Should the line voltage vary in the upward direction the pulse-on time is decreased, while if the line voltage decreases, the pulse-on time is increased. This keeps the total energy delivered to the regulators reasonably constant.

The DC voltage that is switched is produced by a full-wave bridge rectifier and is filtered by two 3000 μf capacitors. This yields 150 VDC and is the main source of energy storage for the supply. In each regulator circuit the 150 VDC is switched by 3 power transistors (Q2 through Q7) that are turned on or off by the sensing and control circuitry. In series with these transistors is the main power transformer that acts to step down the chopped 150 VDC to something closer to the required DC output value. This allows easier filtering and more reasonable switching rates. The transformer also provides needed line isolation.

The power transformer is not a large, conventional type with an iron core. Instead, it has a ferrite core, being very small and light for the energy it must deliver. The ferrite core acts as an inductive storage element, taking energy from the 150 VDC source for about 25 μsec and delivering it to the secondary circuit over essentially the same length of time. It is the high repetition rate that allows the transformer to be so small, compared with a typical 60 Hz unit.

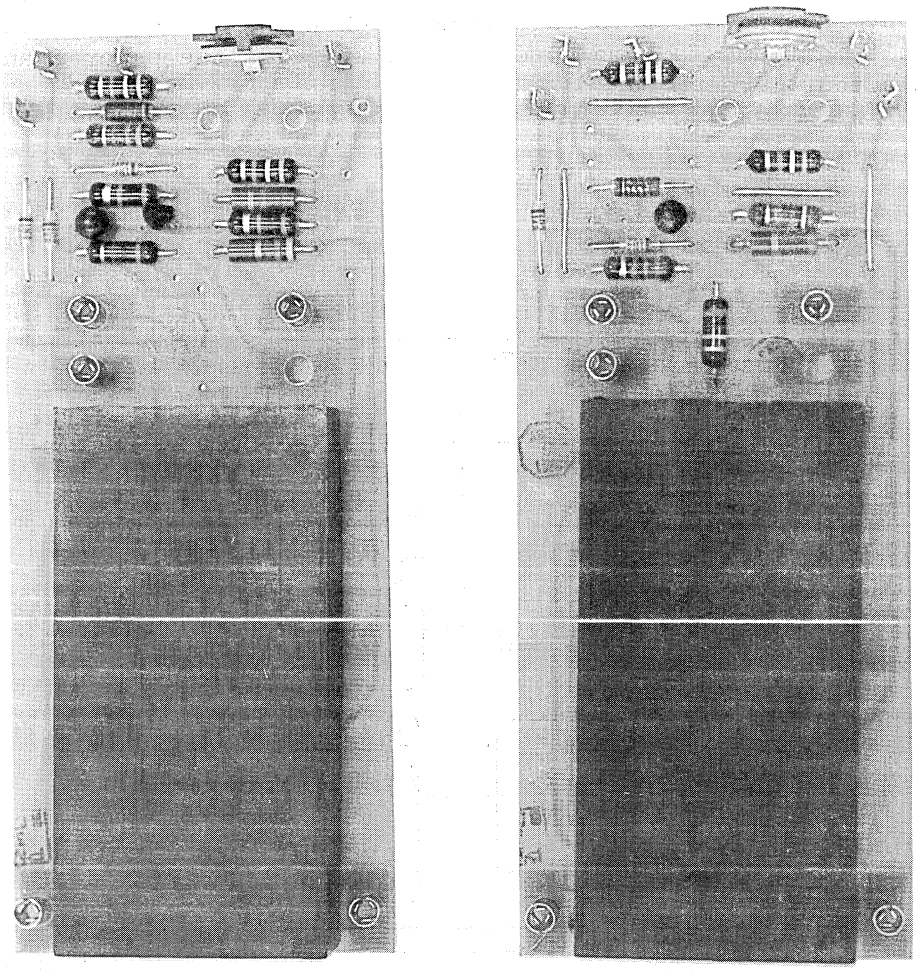
The pulsed output is filtered by several capacitors and an inductor to remove ripple. These capacitors need only store energy for the worst-case time between pump-up cycles ($\approx$1.4 msec with light load). The +5-volt regulated output is delivered to the load through a balun transformer that minimizes internally-generated noise.

The power transistors and driver transformers are shown in Figure 6-6 mounted on the PC Card. Figure 6-7 illustrates the sealed control units (both +5 VDC and +15 VDC) and the voltage sensing circuitry on the PC Card.



SWITCHING TRANSISTORS AND DRIVERS ON PC CARD

FIGURE 6-6



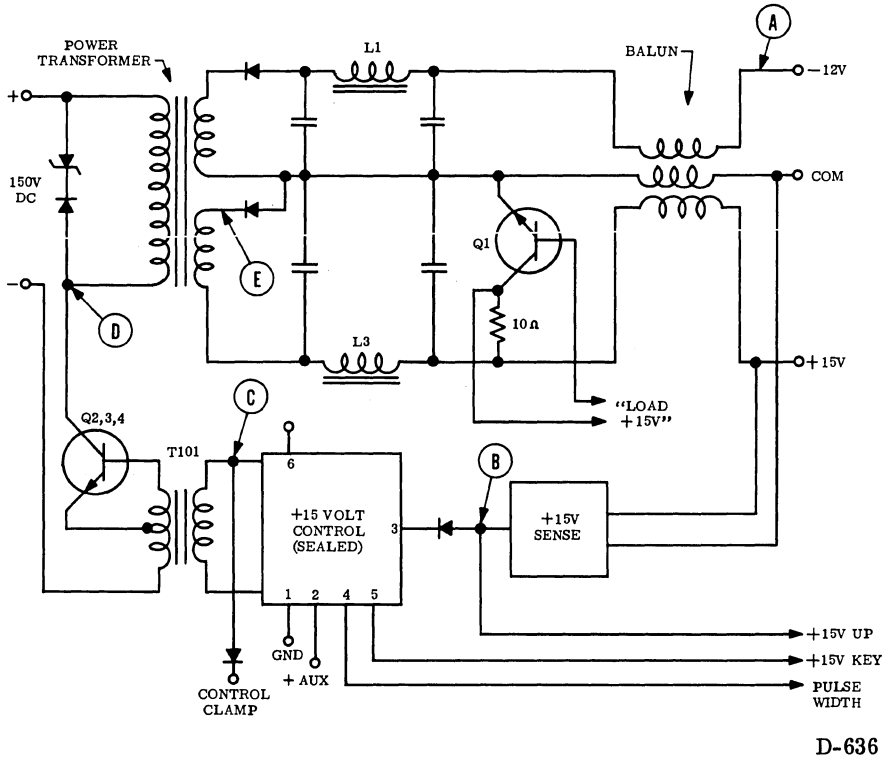
(+5) (+15) and (-12)

SEALED CONTROL UNITS: +5-VOLT (LEFT) AND +15-VOLT (RIGHT)

FIGURE 6-7

3. +15-VOLT AND -12-VOLT CIRCUIT

This circuit, shown in Figure 6-8, is similar to the +5-volt regulator, hence only the differences will be discussed. This power transformer has two secondary windings, one for -12 VDC and one for +15 VDC. As before, the outputs are filtered and sent out through a balun transformer. Since only the +15 VDC output is regulated, only this output is sensed for voltage level. When the +15 volt output falls too low, the control unit initiates a pump-up cycle and triggers the power transistors, which raises the DC output level.



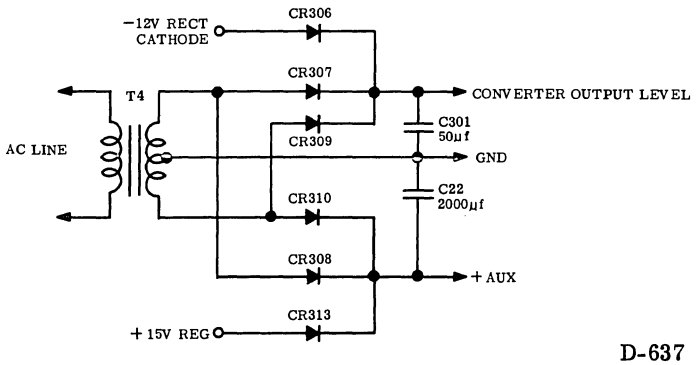
SIMPLIFIED +15 VOLT REGULATOR

FIGURE 6-8

A transistor (Q1) is in series with a 10-ohm, 25-watt resistor across the +15 VDC output. When Q1 is on, an additional load of 1.5 amperes is provided for the supply when -12 VDC is low. Should the situation exist where the load on the +15 VDC supply were zero, and if a load existed on the -12 VDC output, it would drop nearly to zero due to the low repetition rate of the +15 VDC regulator. This additional load causes the repetition rate of the regulator to be held to a minimum of about 700 Hz, assuring adequate drive to the -12 VDC side.

4. +AUX SUPPLY

This unregulated supply shown in Figure 6-9 consists of T4 (24 volts, center tapped) and two separate rectifier circuits. One of these (+AUX) is filtered by a 2000 µf capacitor (C22), and its output is about 15 to 17 VDC. The main purpose of this supply is to provide voltage during a power up cycle, before the regulated circuits provide full output. If this output falls below +15 VDC, CR313 conducts and holds the voltage to no less than 15 volts.

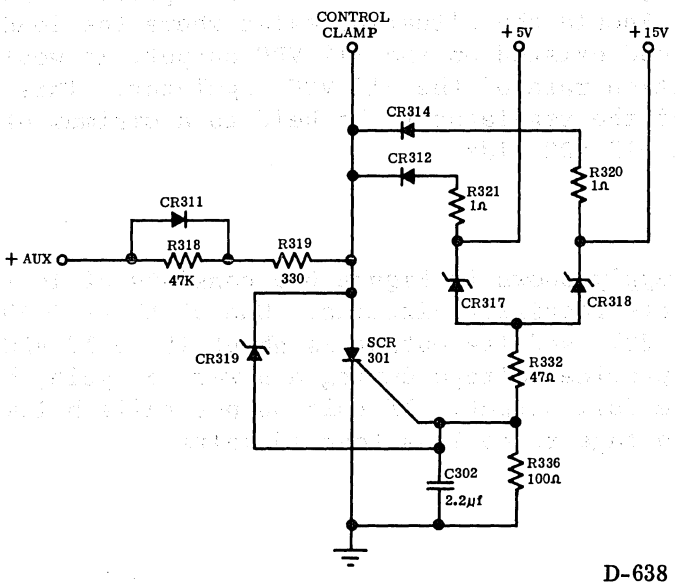


+AUX SUPPLIES

FIGURE 6-9

The other DC output is filtered with a 50 µf capacitor (C301) and this line is labeled Converter Output Level. During the time prior to the full regulator outputs, this line supplies DC voltage (about 17 volts) to the Power Fail circuitry. After the regulated supplies are up to normal value, CR306 connects this line to the converter output of the -12-volt supply. The level is now several volts more positive than the rectifier output and this pulls the line up to about +20 volts. This back-biases the two small rectifier diodes and effectively removes them from the circuit.

Because the converter output is directly proportional to the voltage across the storage capacitors (C19 and C20) a more or less direct sensing of total energy storage occurs. When this voltage falls, due to a power failure, the Power Fail circuit senses this and PWR-FAIL/7 goes low. The system begins a shut-down routine to preserve data.



OVER-VOLTAGE CROWBAR

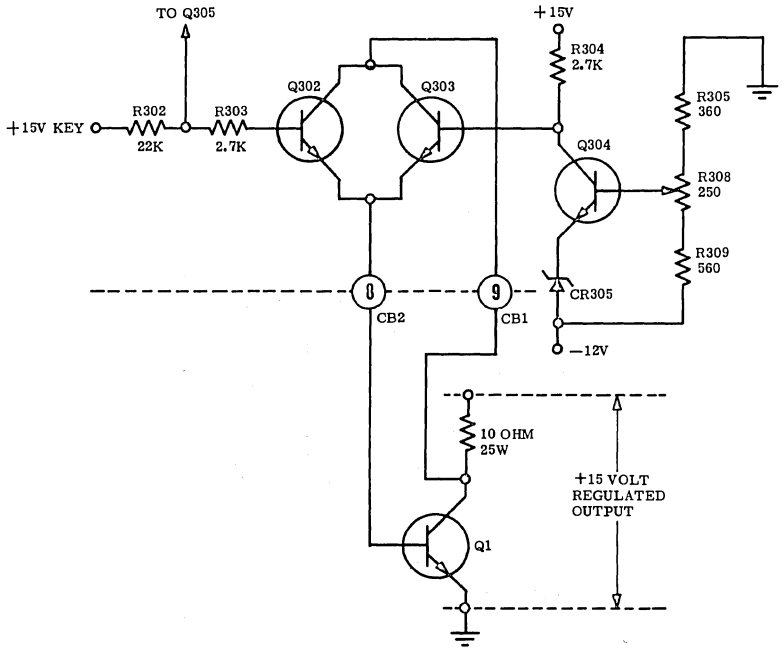
FIGURE 6-10

5. OVER-VOLTAGE CROWBAR

This circuit, Figure 6-10, operates if either the +5 VDC or the +15 VDC supply is over tolerance. Either CR317 or CR318 will avalanche if such a condition exists, and these will in turn fire the SCR. This pulls the Control Clamp line to ground and stops both the +5 VDC and the +15 VDC regulators from operating. A network from the anode of the SCR to +AUX serves to latch the SCR, and when this occurs the main power must be removed and reapplied to delatch the SCR.

6. CURRENT BALANCE

This circuit, Figure 6-11, performs two functions, the end result of which is to shunt a 10-ohm resistor across the +15 VDC output. If the -12 VDC output becomes too low in value, Q304 turns off and the emitter of Q303 goes high. This turns on Q1 in the +15 VDC output and draws an extra 1.5 amperes. This increases the repetition rate and "pumps-up" the -12V side.



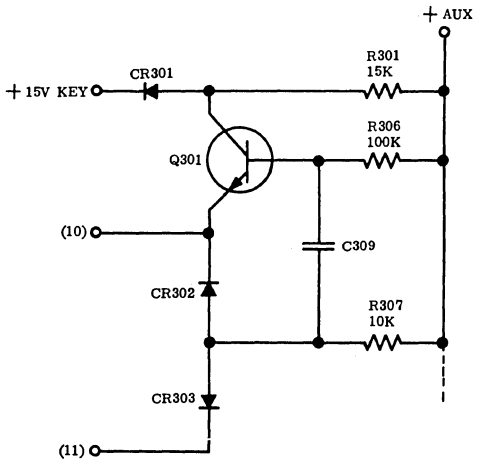
CURRENT BALANCE CIRCUIT

FIGURE 6-11

If the +5 VDC regulator is below normal value, Q305 is on and turns on Q302, performing the same function of loading the +15 VDC regulator to more quickly drop the voltage to zero. At the same time, +15V KEY is produced to disable the 15-volt regulator. The current balance adjustment is set to make Q304 barely conduct (see Adjustment Section). If -12 VDC drops too low in value, CR305 extinguishes and Q304 goes off.

7. -12 VOLT CURRENT LIMIT

Q301, Figure 6-12, serves to sense for the current flowing in the -12 VDC circuit. If current is normal, Q301 is on and the signal +15V KEY is low (CR301 back-biased). If load current increases beyond its limit, Q301 is turned off and its collector rises toward a positive voltage. This stops the +15 VDC regulator and prevents damage to this supply. The load current is sensed by the voltage drop across CR3.



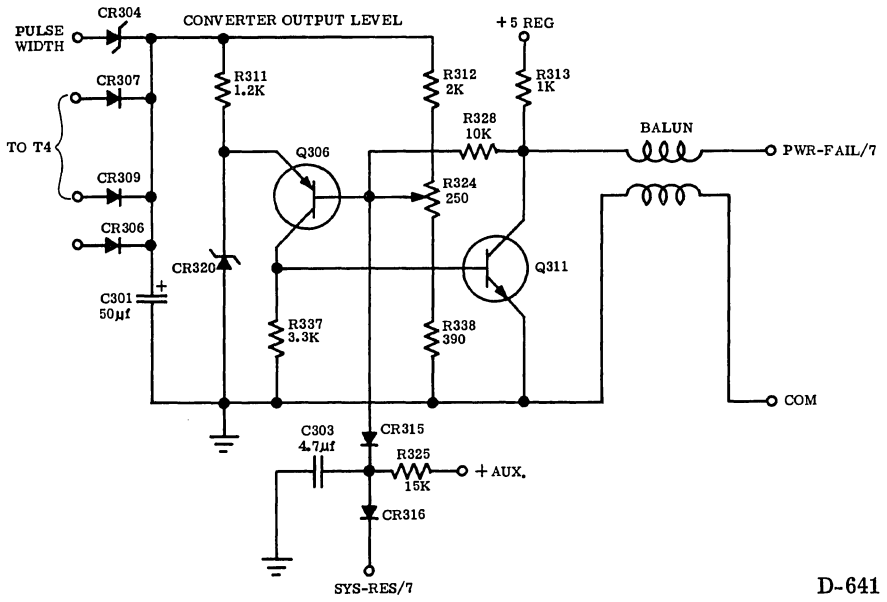
+15V KEY CIRCUIT

FIGURE 6-12

The emitter and base of Q301 are connected to CR3, hence the voltage drop due to excessive current will be seen by the transistor. Because current is driven into this circuit in large, narrow pulses, at the switching rate, the drop across CR3 consists of relatively narrow pulses with a varying repetition rate. C309, then, AC-couples this negative-going pulse train into the base of Q301, turning it off if DC current is excessive.

8. POWER FAIL DETECTOR

When the supply is operating normally, PWR-FAIL/7 is high and Q311 is therefore off (Figure 6-13). R324 is adjusted so that as the AC line voltage increases from below to 93 volts, PWR-FAIL/7 just goes high. This signal will also go low through CR316 and CR315 if SYS-RES/7 goes low.



POWER FAIL CIRCUIT

FIGURE 6-13

During turn on, the two +AUX supplies provide voltage to the SYS-RES/7 detectors and the PWR-FAIL circuits, to drive both signals low before the regulated outputs go above 1 volt. During turn off, PWR-FAIL/7 goes active at least 20 msec prior to SYS-RES/7 going active.

The following detailed circuit description is divided into three sections: Power-Up, Power Normal, and Power Down, since circuit operation is different in each case.

a. POWER-UP OPERATION. Because the two logic signals are inter-related, both are described below. Refer to Figures 6-13 and 6-14. Prior to initial energizing of the supply, all voltages are zero, of course. As the power switch is thrown on, the regulated outputs cannot function, since there is no 150 VDC to operate on as yet. However, assuming that input line voltage is 115 VAC, +AUX rises to approximately +17 VDC, as does the other small output voltage labeled "Converter Output Level".

R325 and CR316 provide V_{CC} for Q312 (SYS-RES/7). Thus, SYS-RES/7 goes low before any DC regulator begins to function. Since the cathode of CR316 is low, CR315 conducts and both Q306 and Q311 turn on hard: PWR-FAIL/7 is also kept active during this time.

When the regulated DC outputs reach their specified levels, the +5 VDC and +15 VDC detectors in the System Reset circuitry cause Q312 to turn off; SYS-RES/7 goes high. This removes the ground clamp from CR316, and it immediately back-biases. At this instant C303 begins to charge toward the "Converter Output Level" voltage (≈20 VDC). The charging time constant is on the order of 2 msec, so in perhaps 1 msec the voltage has risen to slightly more than 5.0 volts. CR316 again is forward biased (through R326) and capacitor voltage is clamped to about 5.7 volts.

As C303 charges to a value more positive than that set by R324, CR315 reverse biases and Q306 turns off. Note that from the time SYS-RES/7 goes high to the time PWR-FAIL/7 goes high, about 1 msec elapses due to the charging delay of C303. This delay is one requirement of the power supply specifications.

b. POWER NORMAL OPERATION. With the DC output voltages at their normal values both signals are high. The emitter of Q306 is at 3.3 VDC (via CR320) and the base voltage is slightly more positive than this. Q306 is off and its collector is at ground, forcing Q311 off and maintaining PWR-FAIL/7 high.

The operation of the two small rectifier circuits is related to PWR-FAIL/7 and SYS-RES/7, and is not completely straightforward, nor is their operation immediately evident from a cursory examination of the circuit. +AUX (Figure 6-9) is connected to the +15 VDC regulated output through CR313. Normally, this diode is reverse-biased, since +AUX is approximately +17 VDC. However, if line voltage should drop, and cause +AUX to therefore drop below 15 VDC, CR313 conducts and holds this line up to no less than 15.0 VDC as long as the +15-volt regulator functions. This maintains proper operation during a power down sequence.

During normal operation, the other small rectifier (CR307 and CR309) is actually not supplying energy to the circuit (the two diodes are reverse-biased). They only function during the first 1 or 2 seconds of a power up sequence. As soon as the +15 VDC regulator produces a normal output, CR306 conducts and lifts this line to about +20 VDC. CR306 returns to the cathode of the -12 VDC rectifier diode, which has a waveform that goes both positive and negative at various times. The positive swing of this waveform is sufficient to cause the "Converter Output Level" line to rise to +20 VDC, thus removing CR307 and CR309 from the circuit. Henceforth, the voltage at this point is a direct reflection of the charge stored on C19 and C20, the main storage capacitors for the regulators, since the positive excursion of the waveform is directly proportional to the voltage across C19 and C20. If line voltage drops sufficiently, the +20 VDC level drops and triggers the power fail circuit.

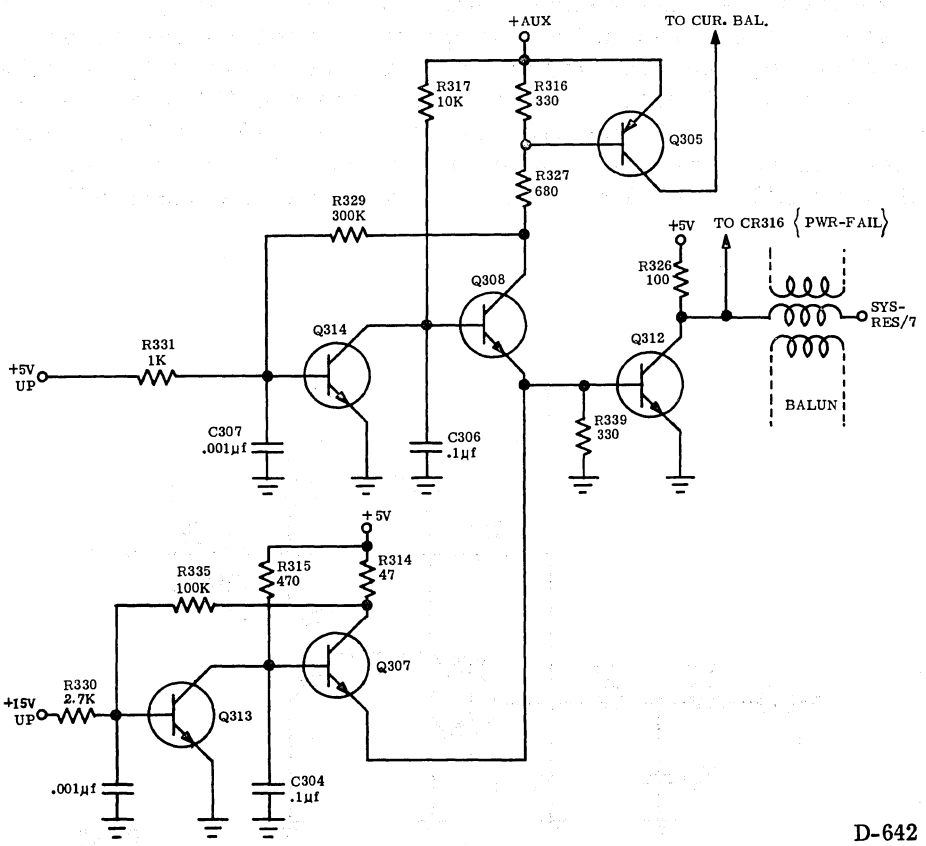
c. POWER-DOWN OPERATION. If AC line voltage should fail during operation, or simply drop below 93 VAC, the two supply lines ("+AUX" and "Converter Output Level") drop accordingly. However, the regulated outputs (+5 VDC and +15 VDC), as well as the -12 VDC output, will continue to function. The energy storage of C19 and C20 is sufficient to maintain proper operation for at least 20 msec. Since the SYS-RES/7 detectors are still functioning, the first thing to happen is that the voltage across the voltage divider (R312, R324, and R338) will drop due to the source at CR306. Q306 will turn on and PWR-FAIL/7 goes low. This signals the computer to begin the power down instruction, safely storing data to prevent its loss.

C19 and C20 continue to provide energy and the switching regulators compensate for energy loss by increasing the repetition rate to keep the outputs up to their normal value. After at least 20 msec, either the +5 VDC or the +15 VDC regulator (depending on the load) will begin to go out of specification. Its corresponding detector will transfer and SYS-RES/7 goes low, signifying that the DC output voltages are too low to be useful. When the +5 VDC supply drops out, the current balance circuit is triggered to load the +15 VDC output, ensuring that it drops to zero rapidly.

During a deliberate power down cycle the action is essentially the same as described above.

9. SYSTEM RESET DETECTOR

This circuit is shown in Figure 6-14. If both regulated outputs are within tolerance, SYS-RES/7 is high. If the pulse train from either supply indicates that the regulator is not functioning properly, either detector turns on and lifts the base of Q312 more positive: SYS-RES/7 goes low.



SYSTEM RESET CIRCUIT

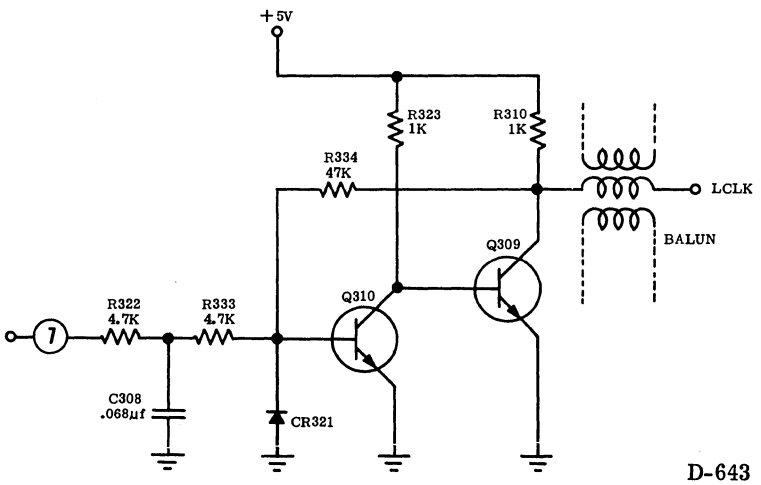
FIGURE 6-14

The sequential operation of the signal SYS-RES/7 is discussed in the immediately preceding section, since the two signals SYS-RES/7 and PWR-FAIL/7 are interrelated. The following discussion, then, covers the detector circuits.

Each detector is basically a Schmitt trigger circuit, used to obtain sharp rise times from a slowly-changing waveform. During normal operation, Q307 and Q308 are off, which allows the base of Q312 to be at ground; SYS-RES/7 is high. At the same time, Q313 and Q314 are on, maintaining the correct bistable condition of the trigger circuits.

If each of the regulated supplies has a normal output, the repetition rate will be some intermediate value. The pulse width at the input to either detector will therefore be of some intermediate value. The input to each trigger circuit is an RC integrator, and the positive pulses are spaced close enough together so as to appreciably charge the integrating capacitors. If the voltage at this point is greater than .7 or .8 volt, the transistors will be on. With Q313 and Q314 on, Q307 and Q308 are off, which allows SYS-RES/7 to be high.

When either regulated output begins to drop in value, the switching control unit will begin to shorten the time between pump-up cycles. Now, at one particular value of switching rate, the corresponding integrator cannot charge to enough voltage to hold its transistor on, and the trigger circuit regeneratively switches to the opposite state. The base of Q312 is lifted positive and SYS-RES/7 goes low. As this happens, PWR-FAIL/7 is forced low through CR315 and CR316 (if not already low). With normal conditions prevailing, the cause of low DC voltages will be low line voltage, hence PWR-FAIL/7 usually goes low 20 msec or more before SYS-RES/7.



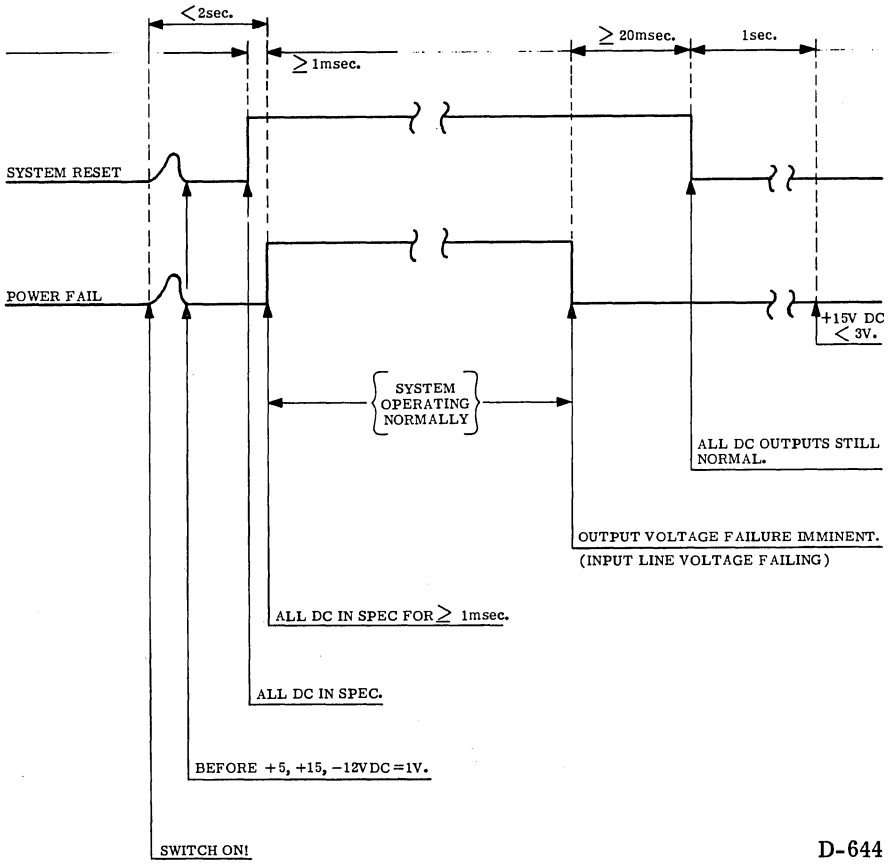
LCLK TRIGGER CIRCUIT
FIGURE 6-15

10. LINE CLOCK TRIGGER

In Figure 6-15, a portion of the secondary voltage of T4 is applied to a squaring circuit. The output is a 60 Hz square wave with a duty cycle of about 50%. LCLK is used for synchronization purposes in certain peripheral equipment, and does not start until +5 VDC starts up.

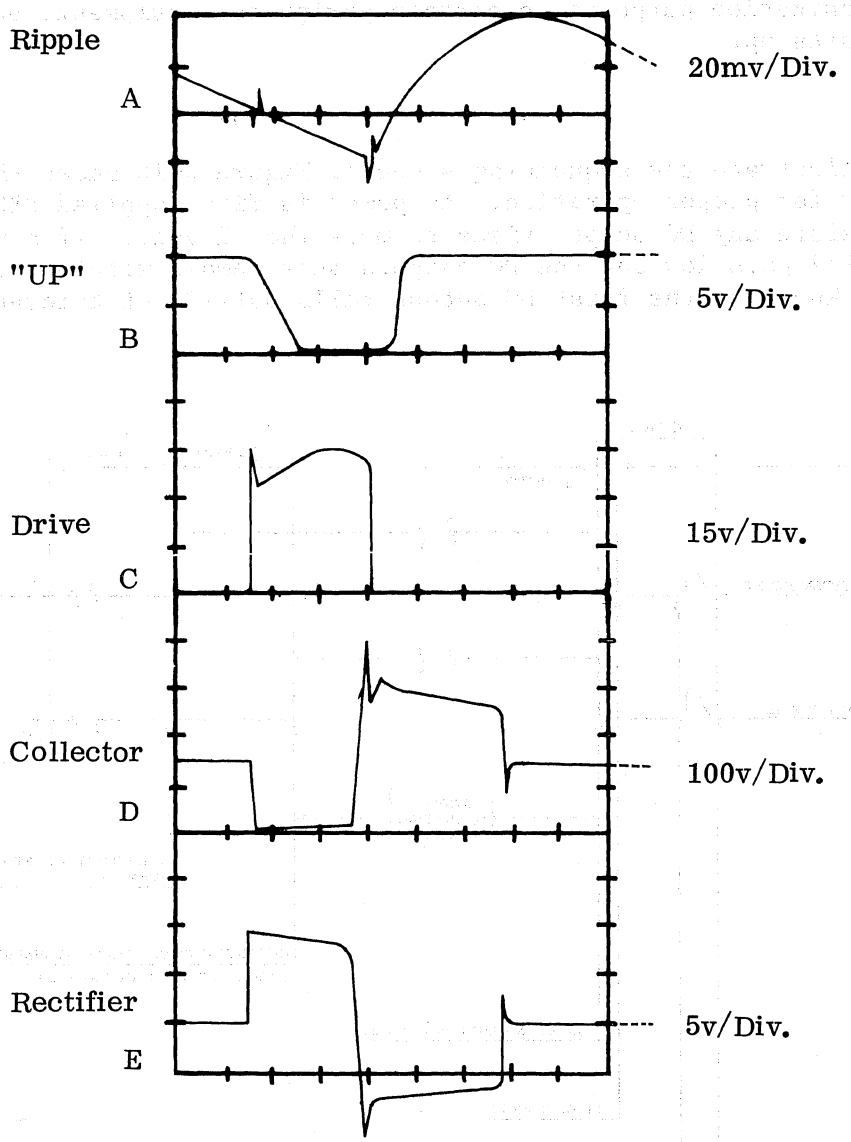
11. SEQUENCING

To further illustrate the sequencing signals, Figure 6-16 shows the waveforms and timing necessary for proper operation. As power is first applied SYS-RES/7 and PWR-FAIL/7 go low before any DC output rises to more than 1 volt. If a power failure is sensed, PWR-FAIL/7 goes low and the DC outputs must remain within tolerance for at least 20 msec. Then, as the first DC output falls outside of tolerance, SYS-RES/7 goes low.



SEQUENCE WAVEFORMS

FIGURE 6-16



POWER SUPPLY WAVEFORMS

FIGURE 6-17

12. POWER SUPPLY WAVEFORMS

The waveforms shown in Figure 6-17 can be viewed at the five places listed below.

A. The regulated output terminal in reference to common.

B. The +5V-UP or the +15V-UP signal applied as the input to the sealed control unit.

C. The high-side output of the sealed control unit.

D. The collectors of the switching transformers.

E. The cathode end of the rectifier diode.

13. SUPPLEMENTARY POWER SUPPLY

Some applications of System Ten require the use of dual supplies where there are more than 3 modules used. In these cases, the output terminals for COMMON and SYS-RES/7 shall be strapped together. PWR-FAIL/7 is to be connected separately. In such applications the rules for signal sequencing shall still apply for all outputs.

14. MANIFOLD DESIGNATIONS

MANIFOLD NO.	NAME	DEFINITION
1	Ground	Internal power supply common
2	+5V UP	Control Signal: high = no cycle low = initiate cycle
3	Pulse Width	Signal voltage proportional to capacitor (C19 & C20) voltage.
4	Control Clamp	Output from over-voltage crowbar.
5	AC1	Secondary of T4.
6	+AUX	Rectified output of T4.
7	AC2	Secondary of T4.
8	CB2	Current balance output.
9	CB1	Current balance output.
10	-12V Rect. Anode	-12VDC rectifier anode.
11	-12V Rect. Cathode	-12VDC rectifier cathode.
12	+15V UP	Control Signal: high = no cycle low = initiate cycle
13	+15V KEY	Inhibit +15 VDC control unit.
14	-12V	Internal -12VDC regulated.
15	+15V	Internal +15VDC regulated.
16	+5V	Internal +5VDC regulated.

E. INTERIM ADJUSTMENT PROCEDURE (PIONEER POWER SUPPLY)

1. ADJUSTMENT LOCATIONS

Figures 6-18 and 6-19 illustrate the terminal strip appearance and input/output terminal locations, as well as the locations of the adjustment potentiometers for the +5 VDC and +15 VDC regulators. The -12 VDC current balance adjustment and the Power Fail adjustment are located on the sequence board. The bottom cover must be removed to make the last two adjustments.

2. +5 VDC ADJUSTMENT

Locate the +5 VDC potentiometer (Figure 6-18). A digital voltmeter must be used for this measurement.

a. Connect the digital voltmeter between the +5 VDC output terminal and output common (NOT chassis).

b. Input voltage (AC) set to 115 volts if a variac is available. If not, connect directly to the power line.

c. Ensure that all DC outputs have approximately 3/4 of full load.

d. Clockwise rotation of the control increases output voltage.

Adjustment ranges are 4.850 volts minimum and 5.150 volts maximum. Adjust within these limits, but as close to 5.000 volts as possible.

3. +15 VDC ADJUSTMENT

Locate the +15 VDC potentiometer (Figure 6-18). A digital voltmeter must be used for this adjustment.

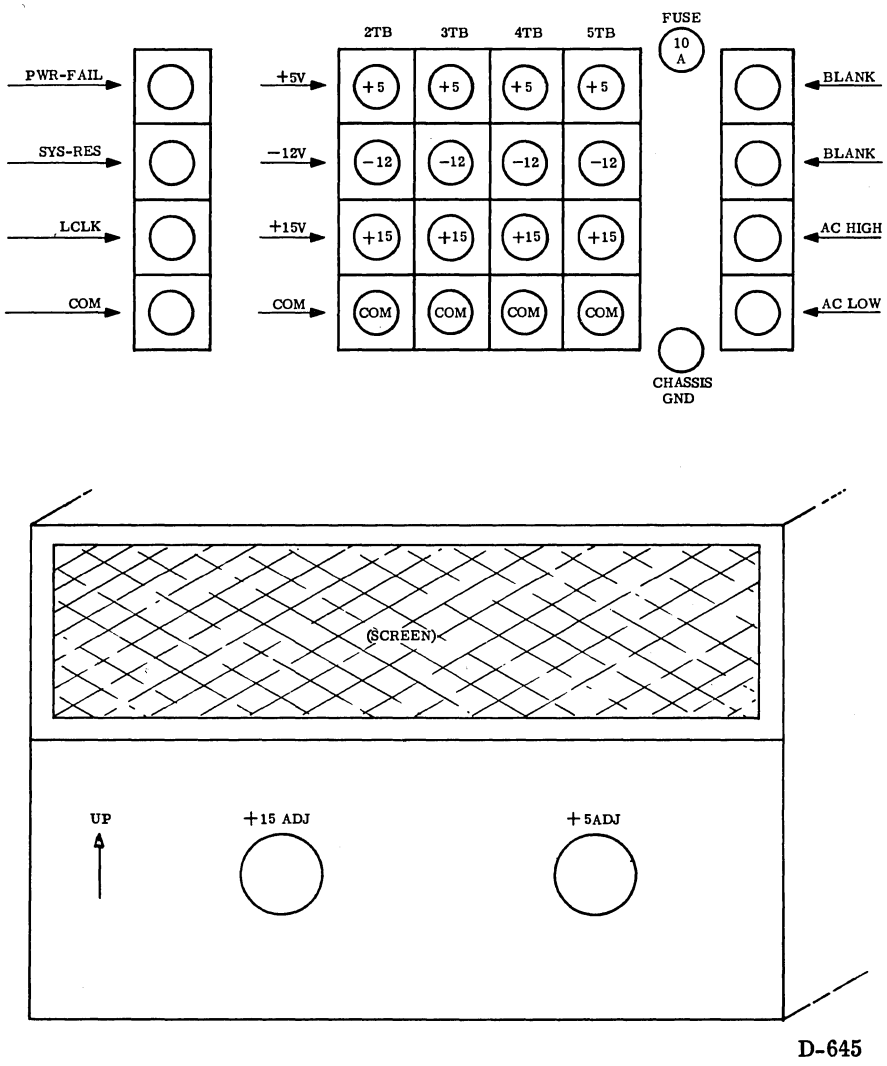
a. Connect the digital voltmeter between the +15 VDC output and output common (NOT chassis).

b. Input AC line voltage set to 115 VAC if a variac is available. If not, connect directly to the line.

c. Ensure that all DC outputs have approximately 3/4 full load.

d. Clockwise rotation of the control increases output voltage.

Adjustment ranges are 14.70 volts minimum to 15.30 volts maximum. Adjust within these limits, but as close to 15.00 volts as possible.

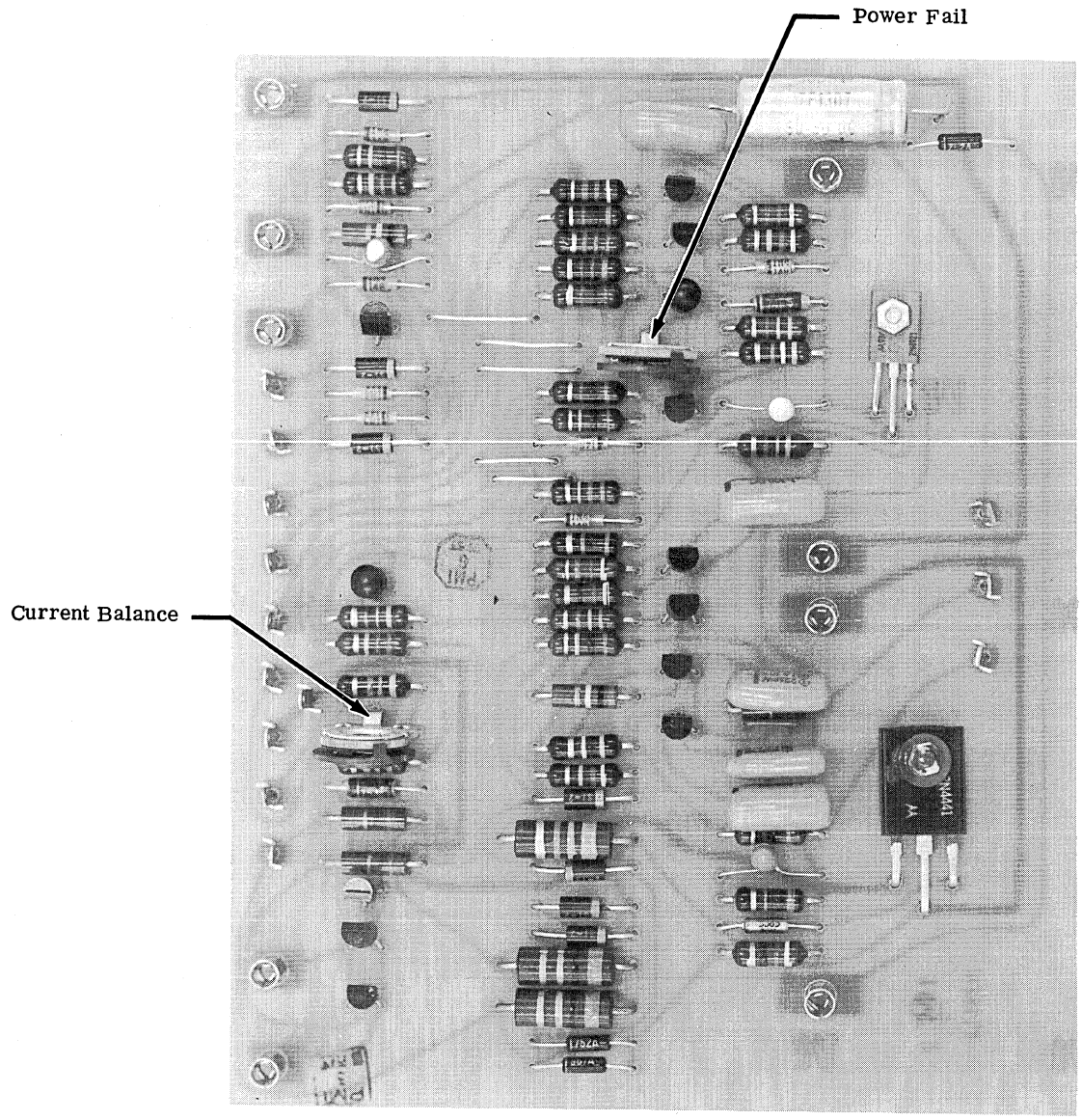


TERMINAL AND ADJUSTMENT LOCATIONS

FIGURE 6-18

4. -12 VDC CURRENT BALANCE ADJUSTMENT

Locate the current balance potentiometer on the sequence card (Figure 6-19).



PWR-FAIL/7 AND CURRENT BALANCE ADJUSTMENTS

FIGURE 6-19

a. Remove all output connections (NO LOAD).

b. Connect an oscilloscope between the -12 VDC output terminal and the output common (NOT chassis).

c. AC line voltage to be 115 VAC if possible.

d. Clockwise rotation of the control increases the repetition rate of the 15 VDC regulator. Adjust the regulator to obtain a repetition rate of 700 Hz (1.4 msec pulse period) measured on the -12 VDC output.

5. POWER FAIL ADJUSTMENT

The following adjustment probably will not have to be made in the field. It is included only for information purposes or in the event of absolute necessity. A variac is required for this adjustment.

a. Locate the Power Fail potentiometer on the sequence card (Figure 6-19).

b. All DC outputs to be loaded with approximately 3/4 full load.

c. AC voltmeter to be connected to the AC line input terminals.

d. A DC voltmeter or DC-coupled oscilloscope (free-running) connected between Power Fail output and output common.

e. Clockwise rotation of the control increases the line voltage point at which the circuit transfers (high to low, or low to high).

f. Insert variac in the AC line. Adjust for less than 93 VAC (85 to 90 volts). Slowly increase input voltage. At 93 volts input, Power Fail should go from low (ground) to high (+5 VDC). This occurs just as the voltage crosses the 93 volt level. Conversely, when line voltage is decreased from above to below 93 volts, the circuit output should go from high to low. Adjust the control to attain this circuit operation.

6. FINAL ADJUSTMENT

After the supply is installed in an operating computer system, the +5 VDC and +15 VDC outputs may be slightly adjusted for optimum voltage, using a digital voltmeter, with actual system load.

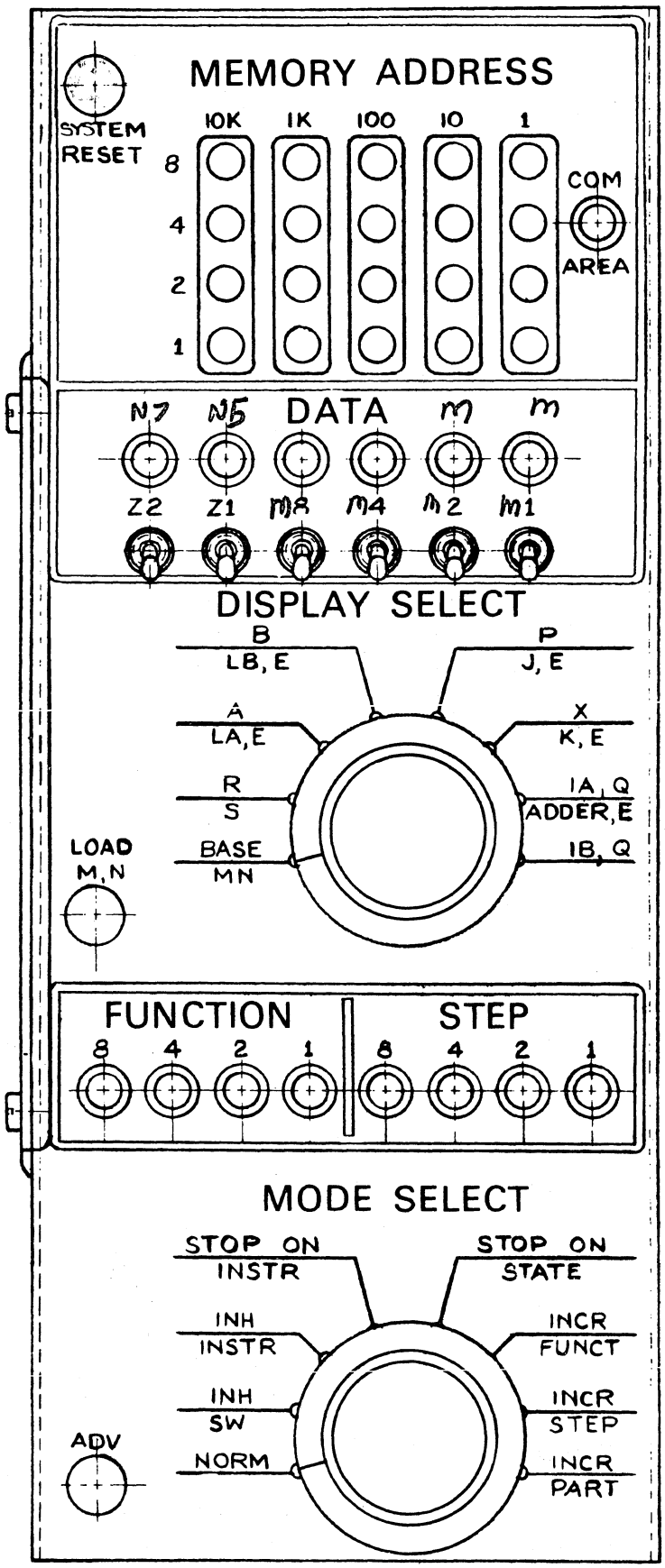
SECTION 7

TEST PANEL

SECTION CONTENTS

LIST OF ILLUSTRATIONS

TEST PANEL



TEST PANEL

FIGURE 7-1

A. GENERAL DESCRIPTION

The Test Panel is shown in Figure 7-1. The lamps are used to display various ACU register conditions. The position of the Display Select switch determines what will be displayed in the lamps. The Mode Select switch permits modification of ACU operation to enable closer study of a particular aspect.

1. "MODE SELECT" AND "ADVANCE" SWITCHES

Although most positions of the Mode Select switch require depression of the Advance pushbutton to accomplish test panel functions, the Mode Select switch is often used independently. Switching the Mode Select switch through those positions requiring an Advance pushbutton depression has no effect on the hardware if Advance is not operated.

a. NORM (Normal operation). This position allows normal ACU operation. It can be considered the "off" position of the Mode Select switch. Returning the switch to this position restores normal operation. This is the only position in which NORMAL partition switching can occur. The Advance pushbutton has no function when the Mode Select switch is on NORM.

b. INH SW (Inhibit partition switching). This position prevents regular partition switching, but allows normal processing in a single partition. The partition count increment in INTERRUPT is not affected, so any I/O operation already in progress when this condition is initiated will be completed normally. The Advance pushbutton has no effect in this mode.

Normal partition switching is inhibited in this and in all other positions of the Mode Select switch except NORM.

c. INH INSTR (Inhibit instruction fetch). This mode prevents fetching any instructions. All in-process I/O operations will be completed. The Advance pushbutton has no effect. This mode provides an orderly method of shutting down the system.

d. STOP ON INSTR (Stop after instruction fetch). This mode stops ACU operation after retrieval of each instruction. When the Advance pushbutton is operated, the ACU executes the instruction, pulls the next instruction, and then stops. The Display Select switch can be used to display each instruction as it is pulled.

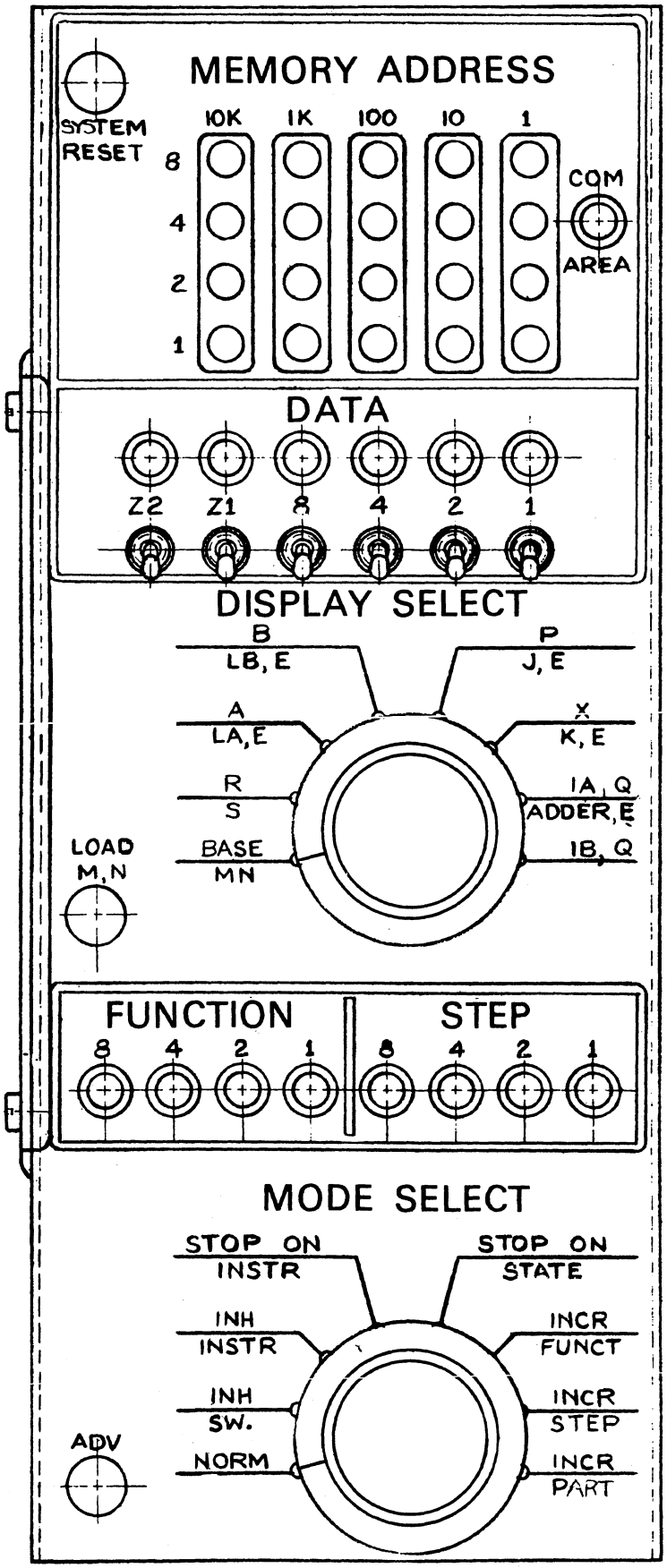
This setting uses the INSTR-STOP signal to halt the ACU. Note that operation actually stops in the state <u>after</u> that in which INSTR-STOP appears. The ACU will stop in one of the following three states:

BG-5	All instructions other than a successful Branch.
BR-0	Successful Branch instructions.
PO-0	Add, Subtract, Multiply, Divide, and Form Numeric Field.

Note that those instructions requiring POSITIONING cause an extra stop in PO-0: in this case, the Advance pushbutton must be operated twice to pull the next instruction.

e. STOP ON STATE (Stop at beginning of each State). The ACU executes one state each time the Advance pushbutton is operated. The Display Select switch can be manipulated to display the desired data in each state.

TEST PANEL



TEST PANEL
(FIGURE 7-1)

NOTE: Extreme care must be exercised when using any of the following three Mode Select settings, as system operation may be severely affected, requiring extensive corrective steps.

f. INCR FUNC (Increment the Function Counter). Each Advance pushbutton operation increments the Function Counter once, enabling selection of any function. No ACU operation occurs within a given function.

g. INCR STEP (Increment the Step Counter). Each Advance pushbutton operation increments the Step Counter once, enabling selection of any step. No ACU operation occurs within a given step. This setting must be used to select the "service states", PO-4, 5, and 6.

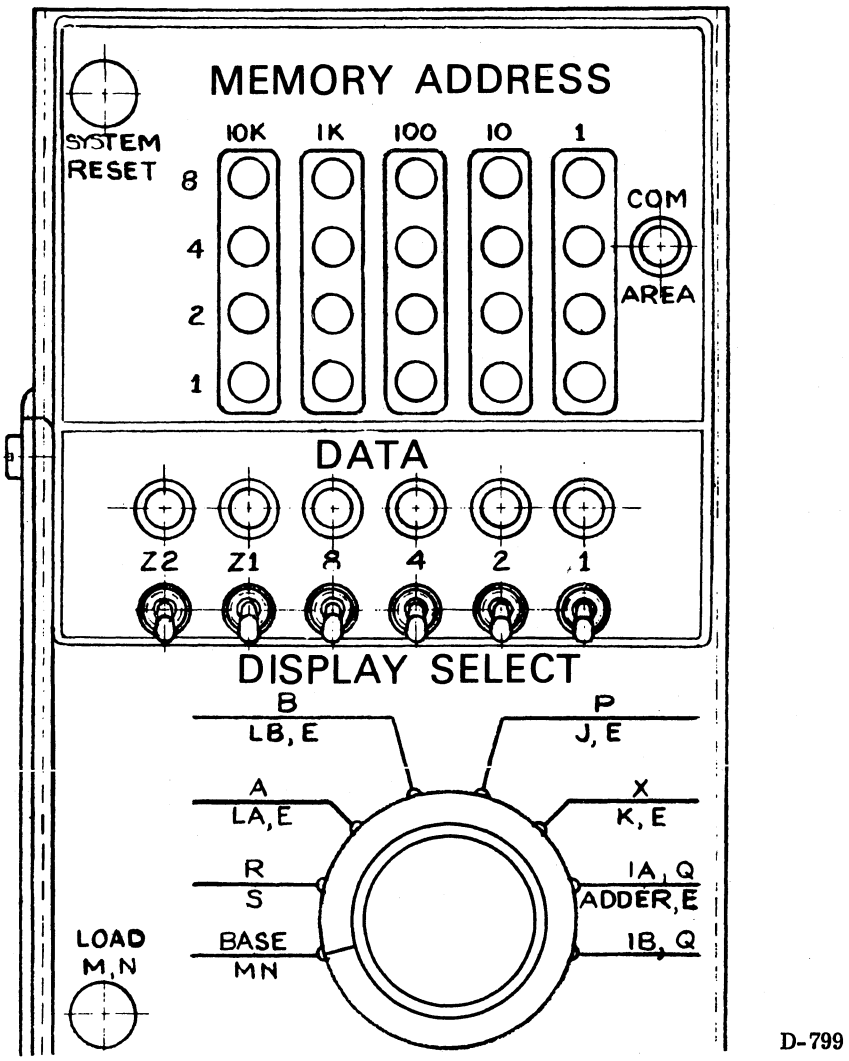
h. INCR PART (Increment the partition count). Each Advance pushbutton operation increments the X Counter once, enabling selection of any partition. No processing occurs.

2. "FUNCTION" AND "STEP" INDICATORS. The Function and Step indicators accurately indicate the "state" present in the ACU whenever it is stopped. Figure 7-2 compares the Function codes displayed by the Test Panel to the F codes.

INSTRUCTION	F REGISTER				FUNCTION	FCB				MNEMONIC
	F3	F2	F1	F0		8	4	2	1	
READ	0	0	0	0	READ/WRITE	0	0	0	0	RW
WRITE	0	0	0	1	READ/WRITE	0	0	0	1	RW
(Not Used)	0	0	1	0	INTERRUPT	0	0	1	0	IT
(Not Used)	0	0	1	1	SWITCH	0	0	1	1	SW
ADD	0	1	0	0	ADD/SUBT	0	1	0	0	AS
DIVIDE	0	1	0	1	DIVIDE	0	1	0	1	DV
MULTIPLY	0	1	1	0	MULTIPLY	0	1	1	0	MU
SUBTRACT	0	1	1	1	(Not Used)	0	1	1	1	
TRANSFER	1	0	0	0	TRANSFER	1	0	0	0	TR
NUM. TRANSFER	1	0	0	1	INDEX	1	0	0	1	IX
(Not Used)	1	0	1	0	BEGIN	1	0	1	0	BG
BRANCH	1	0	1	1	BRANCH	1	0	1	1	BR
EDIT	1	1	0	0	EDIT	1	1	0	0	ED
FORM NUM. FIELD	1	1	0	1	FRM NUM FLD	1	1	0	1	FN
COMPARE	1	1	1	0	COMPARE	1	1	1	0	CO
EXCHANGE	1	1	1	1	POSITION	1	1	1	1	PO

COMPARISON OF INSTRUCTION CODE TO FUNCTION CODE

FIGURE 7-2



	DISPLAY SELECT POSITION	DISPLAY LAMPS							
		DATA		MEMORY ADDRESS					
		1-2-4-8	Z1-Z2	10K	1K	100	10	1	Common
1	BASE/MN	M	N	Y1	Y0				
2									
3	A/LA, E	LA	E		A3	A2	A1	A0	AC
4	B/LB, E	LB	E		B3	B2	B1	B0	BC
5	P/J, E	J	E		P3	P2	P1	P0	PC
6	X/K, E	K	E				X1	Q Q+5	$(X0)$ $\overline{(X0)}$
7	IA, Q/Adder, E	Adder	E				1A	Q	
8	IB, Q						1B	Q	

DISPLAY LAMP DECODING

FIGURE 7-3

3. "DISPLAY SELECT" SWITCH, DISPLAY LAMPS

The position of the Display Select switch determines what information is to be displayed in the Memory Address and Data display lamps. The register or information noted above the line at each Display Select position will appear in the Memory Address lamps; that information noted below the line will appear in the Data lamps. Information to be displayed in the Memory Address lamps is gated onto the R bus and then to the lamp drivers. Information appearing in the Data lamps can come directly from M and N or from the S bus. LA, LB, K, E, etc., are gated onto the S bus for display, so that the contents of M and N are not disturbed. In all cases, the lamps will light only when the ACU is stopped.

Figure 7-3 summarizes the information appearing in the various lamps for each setting of the Display Select switch.

4. "LOAD M, N" AND "DATA" SWITCHES

The Load M,N and six Data switches are used in conjunction with the Mode Select switch and the "service states", PO-4, 5, and 6, to read data presently stored in core or to write new data into core.

A code is loaded into M and N by setting the Data switches to the desired code and then depressing the Load M, N pushbutton, The Display Select switch must be set on BASE/MN. This is due to the fact that the loading of M and N is a hardware "OR" function, and any bit either in the Data switches OR on the S bus will be set into M and N when the pushbutton is depressed. Setting the Display Select switch on BASE/MN prevents gating any information onto the S bus.

This feature is used in PO-4 to load the A register (MSD first) with the relative address of the MSD position of the field to be read from or written into. It is also used in PO-6 to vary the data being written into core. It can also be used to load a code into M and N at any time the ACU is stopped, in order to change a given operation in some particular way.

5. "SYSTEM RESET" SWITCH

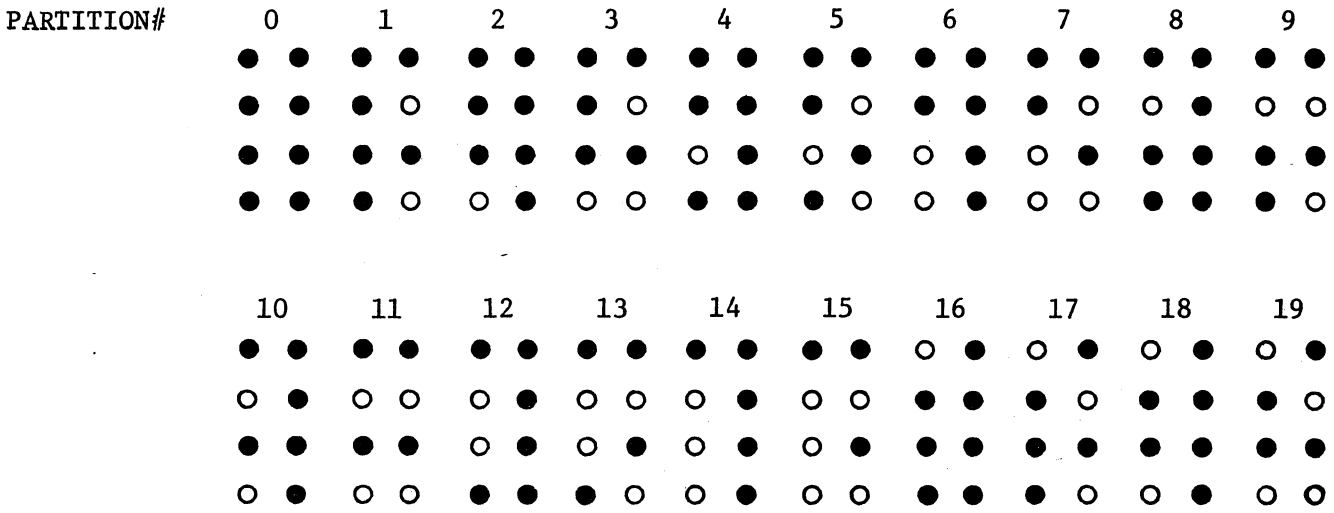
Depressing the SYSTEM RESET pushbutton has the same effect on the hardware as detection of a power failure. It conditions all major registers and counters to their "reset" state and sets the Function and Step Counters to SW-2.

6. READ/WRITE PROCEDURE

The procedure for reading data from core or writing data into core via the Test Panel is the same for the first eight steps, since these steps have to do only with addressing the desired memory location.

a. ADDRESSING MAIN MEMORY FROM THE TEST PANEL. The procedure for addressing Main Memory is as follows:

(1) Set the Display Select switch to X/K,E. Set the Mode Select switch to INCR PART and operate the Advance switch to select the desired partition. The two right-hand rows of Memory Address Display lamps will exhibit the partition number as follows:



(2) Set the Mode Select switch to INCR FUNC and operate the Advance pushbutton to select POSITIONING (FUNCTION = 1111).
(3) Set the Mode Select switch to INCR STEP and operate the Advance pushbutton to select PO-4 (STEP = 0100).
(4) Set the Mode Select switch to STOP ON STATE. Depress the Advance pushbutton once. (This executes the Q = 0 portion of PO-4, which performs no logic function.)
(5) Set the Display Select switch to BASE/MN. Set the Data switches 1, 2, 4, and 8 to the BCD equivalent of the MSD of the relative memory address desired. Depress Load M,N once. Depress Advance, This executes the Q = 1 portion of PO-4.

PO-4

Q = 0	No Function
Q = 1	Load A3
Q = 2	Load A2
Q = 3	Load A1
Q = 4	Load A0

(6) Set the Display Select switch to A/LA,E, and check to see that the code in the Data switches is properly loaded into A3. Return the Display Select switch to BASE/MN.
(7) Operate the proper data switches to select the A2 digit of the relative address desired. Depress Load M,N once and Advance once. If desired, set the Display Select switch to A/LA,E and check the display lamps to see that the code in M is correctly loaded into A2. Return the Display Select switch to BASE/MN.
(8) Repeat step 7 two more times for the A1 and A0 digits of the relative address. Set the Display Select switch to A/LA,E and check the display lamps to see that the desired address is in A. After the Q = 4 portion of PO-4 is executed, the ACU will automatically step to PO-5.

b. READING FROM MAIN MEMORY VIA THE TEST PANEL. After having addressed the desired Main Memory location, data can be read from memory as follows:

(1) Be certain that the ACU is in PO-5 (FUNCTION = 1111, STEP = 0101), and that the Mode Select switch is set to STOP ON STATE.
(2) Set the Display Select switch to BASE/MN. Depress the Advance pushbutton once. Read the character from memory in the Data display lamps.
(3) Depress the Advance pushbutton once for each character to be read. The character will be displayed in the Data lamps. (The data will be written back into core undisturbed.)

c. WRITING INTO MAIN MEMORY FROM THE TEST PANEL. After having addressed the desired Main Memory location, data can be written into memory as follows:

(1) Be certain the ACU is in PO-6 (FUNCTION = 1111, STEP = 0110). To get past PO-5, it will be necessary to set the Mode Select switch on INCR STEP and depress the Advance pushbutton once. Set the Mode Select switch back to STOP ON STATE.
(2) Set the Display Select switch to BASE/MN. Operate the proper Data switches to represent the 6-bit character to be written into memory. Depress Load M, N once.
(3) Depress the Advance pushbutton once.
(4) Repeat step #3 once each time the same character is to be written into memory. Repeat steps 2 and 3 for each different character to be written.

d. TERMINATING THE READ/WRITE PROCEDURE. When reading and/or writing by the Test Panel is complete, it is necessary to set the Mode Select switch to INCR FUNC and depress the Advance pushbutton in order to get out of POSITIONING.

SECTION 8

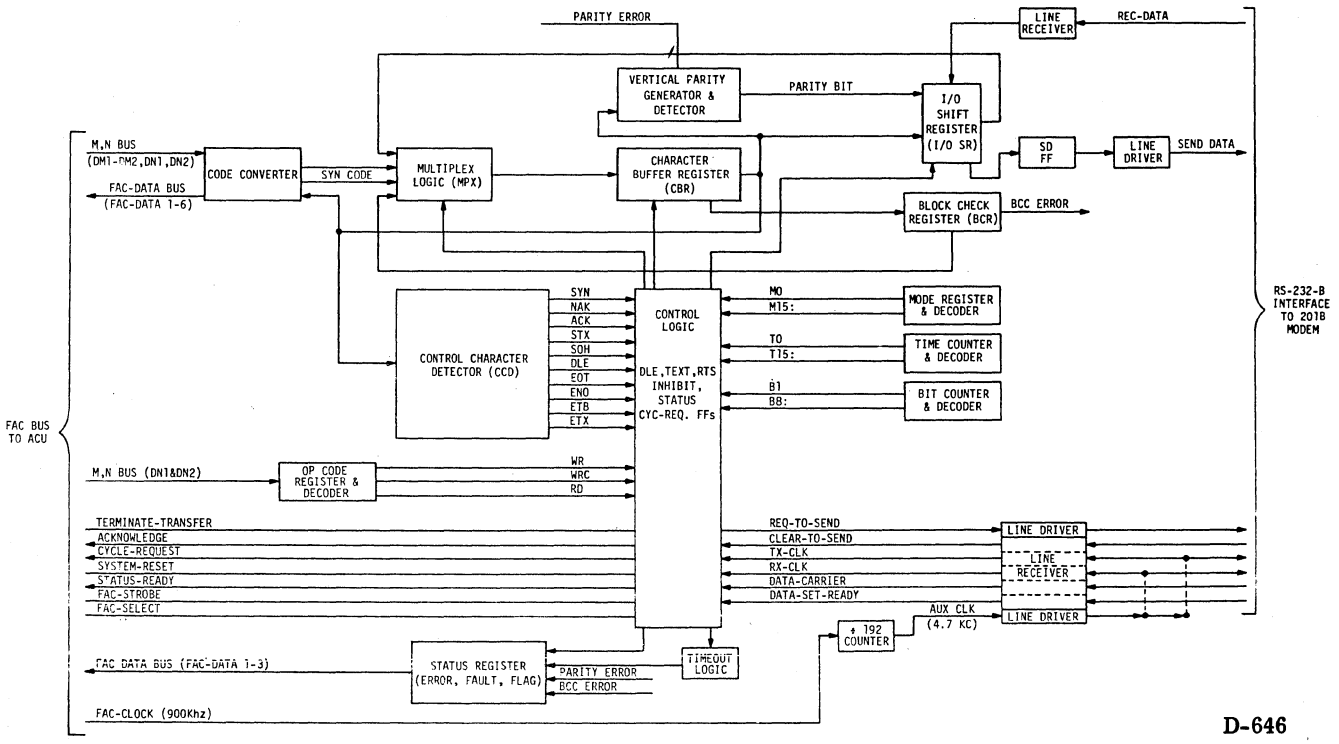
ON LINE COMMUNICATIONS ADAPTER

SECTION CONTENTS

SECTION 8

ON LINE COMMUNICATIONS ADAPTER

LIST OF ILLUSTRATIONS



OLCA BLOCK DIAGRAM

FIGURE 8-1

A. GENERAL DESCRIPTION

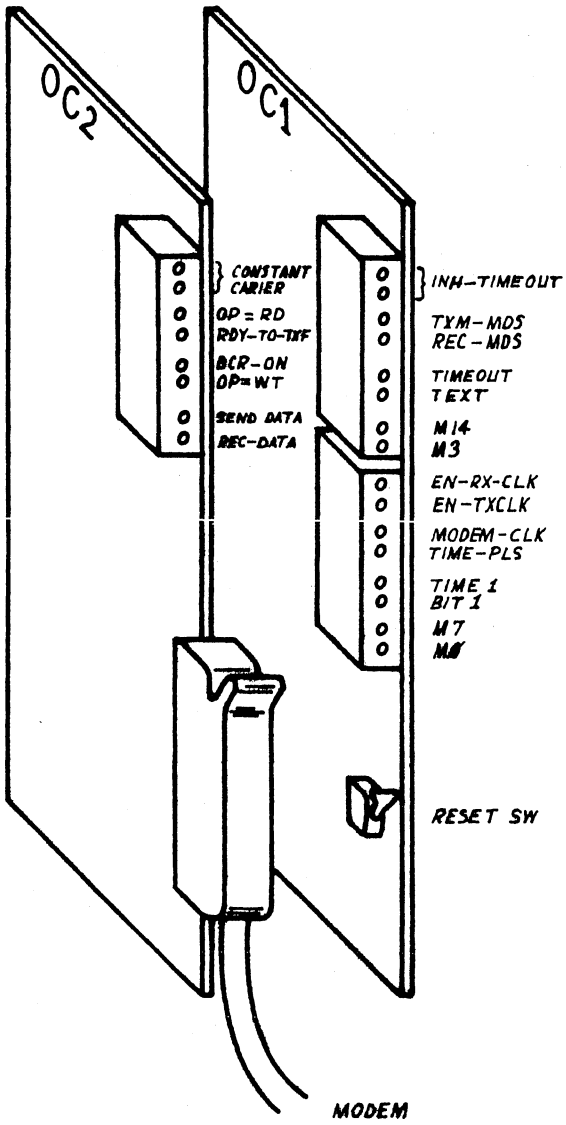
The On Line Communications Adapter (OLCA) couples the File Access Channel (FAC) of the central processing unit to a foreign computer, through telephone modems and communications system. It converts voltages and logic levels to compensate for differences between the processor and the modem. It also manufactures line control codes needed to format messages to the foreign computer, and provides synchronization and decoding of messages received. In addition, it checks character parity (vertical redundancy) and message blocks (horizontal redundancy) to assure the validity of the data transferred over the communication line. Figure 8-1 shows a block diagram of the basic functions of the OLCA.

An available option of the OLCA is a direct connection cable to the foreign computer, if the physical proximity permits.

1. PHYSICAL CHARACTERISTICS

The OLCA is physically contained on two printed circuit cards in the FAC module of the processor. Card OC1 occupies position 4V, and OC2 occupies position 4W. Figure 8-2 is an illustration of the two OLCA cards, and the test points that are brought to the edge of each card. Table 8-1 lists the test point assignments for the two cards.

Both cards connect to the processor through normal FAC module connectors. In addition, the OC2 card connects to a 30-pin front edge connector for interface with the modem.



D-800

OLCA TEST POINTS

FIGURE 8-2

TABLE 8-1 TEST POINT ASSIGNMENTS

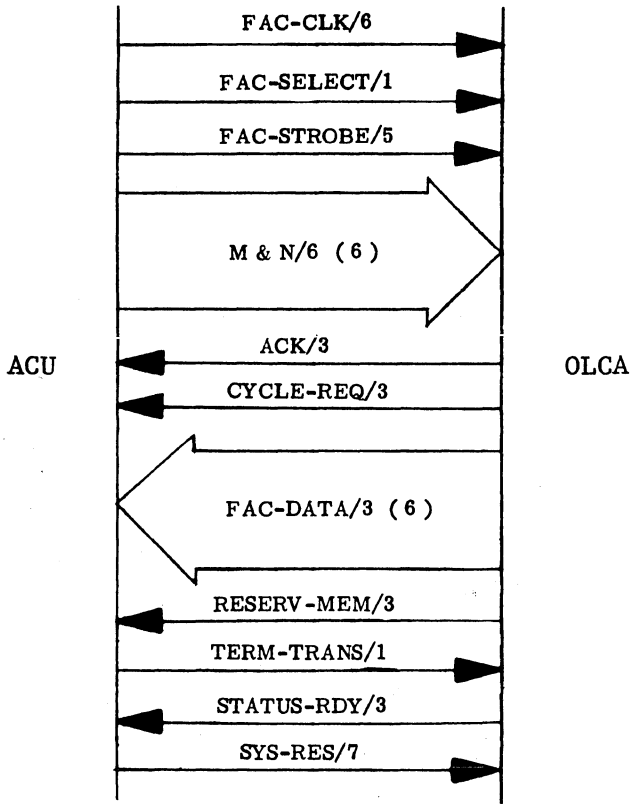
CARD	TEST POINT	NAME	FUNCTION
OC1	1	MO	IDLE MODE
OC1	2	M7	EXIT MODE
OC1	3	BIT 1	BIT 1
OC1	4	TIME 1	TIME 1
OC1	5	TIME-PLS	TIME COUNTER TRIGGER
OC1	6	MODEM-CLK	ACTIVE MODEM CLOCK
OC1	7	EN-TX-CLK	IN TRANSMIT
OC1	8	EN-RX-CLK	IN RECEIVE
OC1	9	M3	RECEIVE MODE
OC1	10	M14	TRANSMIT MODE
OC1	11	TEXT	TEXT FF SET
OC1	12	TIMEOUT	TIMEOUT HAS OCCURRED
OC1	13	REC-MDS	MODES 1-5
OC1	14	TXM-MDS	MODES 6, 8-14
OC1	15,16	INHIBIT TIMEOUT PAIR	INHIBITS TIMEOUT IN REC
OC2	1	REC-DATA	RECEIVED DATA
OC2	2	SEND-DATA	TRANSMITTED DATA
OC2	3	OP-WRT	OP=WRITE OR WRITE CNTL
OC2	4	BCR-ON	ACCUMULATE IN BCR
OC2	5	RDY-TO-TXF	OP IN PROGRESS
OC2	6	OP=READ	OP=READ
OC2	7,8	CONSTANT CARRIER PAIR	FORCES RTS TO ON STATE

B. INTERFACE

The OLCA resides in the FAC module, and interfaces with the FAC signals. Data is transferred from the ACU through the M and N registers. The OLCA acquires the services of the ACU on a priority basis (as will any FAC device) by setting CYCLE-REQuest. When the CYCLE-REQuest is made, the ACU shuts off STATE-CLK, suspending normal operation, and performs an FAC cycle.

1. INTERFACE SIGNALS

The OLCA interface signals (Figure 8-3) and their meanings are given below.



INTERFACE SIGNALS

FIGURE 8-3

a. ACU SIGNALS:

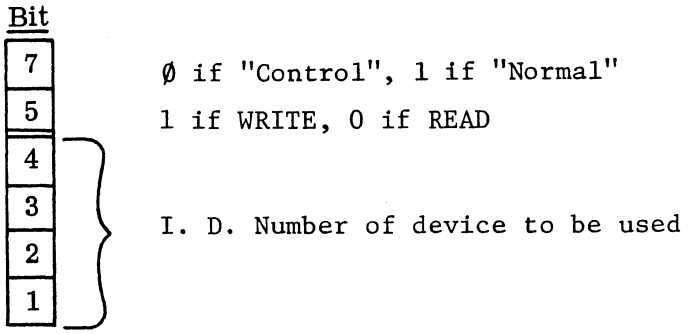
M & N/6	- Six lines carrying data from the ACU.
FAC-STROBE/5	- Strobes data between ACU and FAC device; provides timing for other operations.
FAC-SELECT/1	- Informs FAC devices that the character in the M/N Registers is a device selection character.
TERM-TRANS/1	- Tells FAC device to terminate the data transfer and to provide status.
FAC-CLK/6	- Continuous 900 KHz signal in phase with the ACU clock. (One cycle = 1.11 μsec.)
SYS-RES/7	- De-selects FAC device or controller and resets it to its turn-on condition.

b. OLCA SIGNALS

FAC-DATA/3	- Six lines carrying data to the ACU.
ACK/3	- Positive response to selection signals.
CYCLE-REQ/3	- Request to transfer a character to or from Main Memory.
RESRV-MEM/3	- Halts normal ACU operation and reserves access to Main Memory for FAC transfers.
STATUS-RDY/3	- Status character is ready on the FAC-DATA lines.

2. DEVICE SELECTION

The permanently assigned device address for the OLCA is 8. The ACU places an FAC Select character (Figure 8-4) in the M and N registers, and sends the FAC-SELECT and FAC-STROBE signals to all devices. If the OLCA is ready, it responds with an ACK/3 signal, and the ACU sets the F2 flip-flop denoting "FAC busy" and enabling subsequent FAC transfer operations.

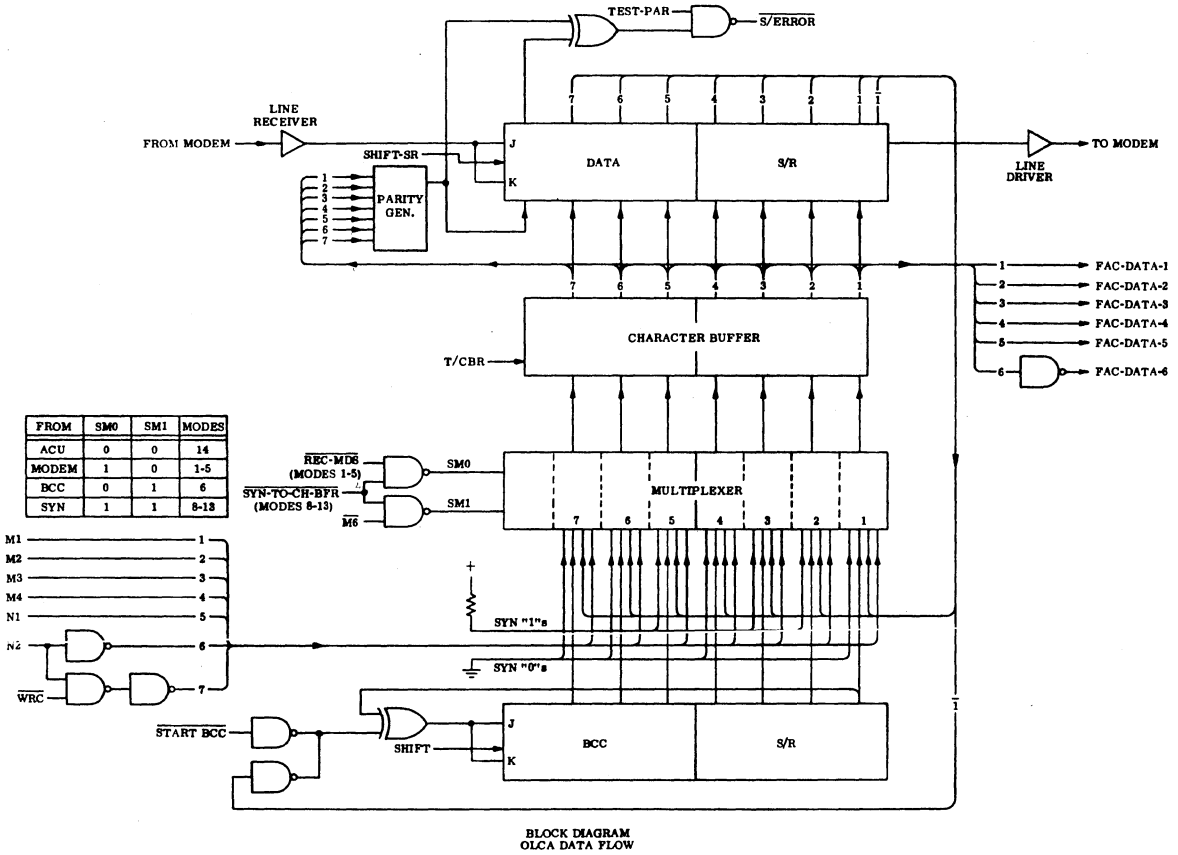


FAC "SELECT" CHARACTER

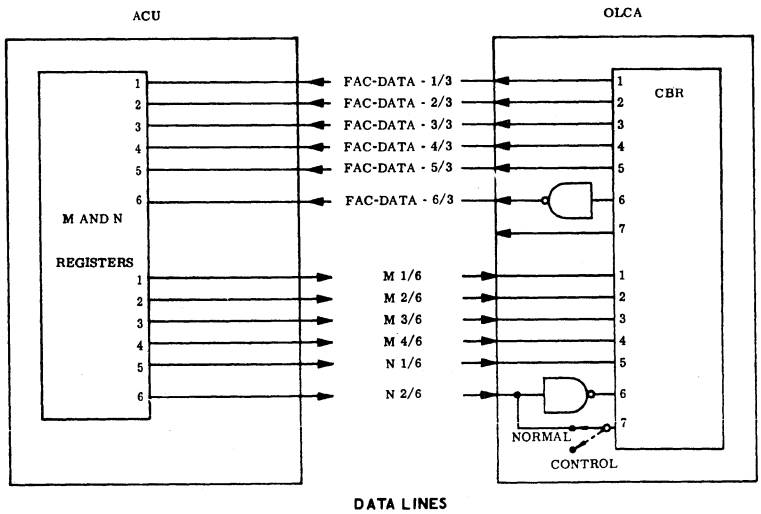
FIGURE 8-4

3. DATA FLOW

A simplified block diagram of OLCA data flow is given in Figure 8-5. The character bit lines 1 through 5 enter and exit without change. However the six bit is inverted both on entry and exit. The OLCA seven bit is created from the six bit and the WRITE CONTROL line; it is dropped when data is passed to the ACU. Figure 8-5 shows a graphic representation of the data bit changes in the OLCA interface.



BLOCK DIAGRAM
OLCA DATA FLOW



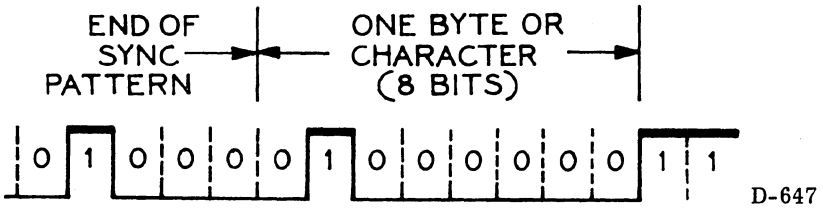
OLCA DATA FLOW

FIGURE 8-5

C. BINARY SYNCHRONOUS COMMUNICATIONS

1. INTRODUCTION

The binary synchronous communications (BSC) system transmits data as a serial stream of standard USASCII binary digits (see Figure 8-6). Active receiving stations are locked in step with the transmitter by recognizing a specified sync pattern (SYN SYN) that starts each transmission. When communicating with foreign computers (not Friden) a minimum of 6 SYN's must be sent to assure bit phase then character phase. The Friden System depends upon the modem to acquire bit phase, and requires only two contiguous (adjacent and continuous) SYN's to set character phase.



SYNCHRONOUS DIGITS

FIGURE 8-6

Data link control characters are used to supervise data link operation, and provide system flexibility. For example, with the proper use of control characters, a data link may operate point to point (two stations only) or multi-point (more than two stations).

BSC may use private-line or switched (dial-up) two wire systems, or four wire systems with a constant carrier. However, message transmission is always in one direction at a time.

2. DATA LINK

A data link is: the communications channel, the data sets (or line adaptors), and the communications-control portion of each of the stations on the channel. Each data link is a separate entity with complete message compatibility throughout the link. Terminal equipment may vary from a basic send/receive reader/printer to a control unit serving several input/output devices, or it may be a processor interconnected to the communications line.

When the data link operates on a point to point basis, transmission is between the two stations only. However, if the data link is not permanently connected, as leased lines etc., any station on the switching network is available on a point to point basis.

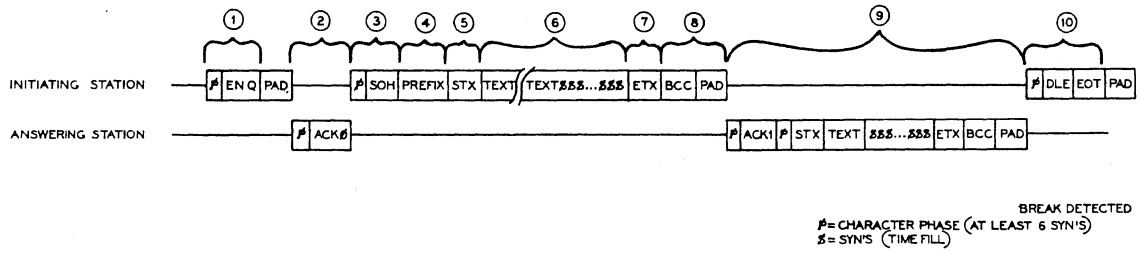
Multi-point data links operate between one master unit and one or more receiving units. Control is maintained by the master unit. Transmission in a multi-point system is initiated by selection or polling from the master unit.

3. BSC OPERATION

In a point to point system a situation can occur where both stations may attempt to acquire the line simultaneously. To minimize this possibility, a station can be given a (program) priority, where the higher priority station will not answer if it is ready to send. An ENQ (enquiry) is sent onto the line by the station wishing to transmit. There are three possible answers to an ENQ: ACKØ, NAK, and WABT. ACKØ (really DLE Ø) is an affirmative reply, indicating that the receiving station is ready. NAK is a definite and final negative response, indicating either the previous message was garbled, or the receiver is not ready for data. WABT (wait before transmitting) is a temporary not ready condition and may be responded to by program. Any reply, however, must be preceeded by character phase.

A multi-point system polls and selects from the master station (a pre-assigned controlling station). Polling, an "invitation to send", is transmitted from the master station to a specific remore station. Selection is a "prepare to receive" notification from the master station to one or more remote stations.

Each station in the data link is assigned a unique primary identification for polling and selection. If stations in the data link have multiple input and output capabilities, the identification may contain up to seven characters. The first character would be the station identity, and additional characters may indicate specific components desired (such as punch, type, record, etc.). Once a station responds affirmatively, message transmission can start. Message text is transmitted in blocks, and preceeded by an STX (start of text) character (see Figure 8-4). Each block of text (except the last) is immediately followed by an ETB (end of transmission block) character. The last block of text in a message is immediately followed by an ETX (end of text) character.



INSTRUCTIONS TO INITIATING OLCA STATION

1. Write Control
2. Read
3. Write Control
4. Write
5. Write Control
6. Write
7. Write Control
8. Automatic Hardware Action
9. Read
10. Write Control

MESSAGE FORMAT

FIGURE 8-7

If desired, a message text can be preceded by an SOH (start of heading) character and a prefix containing auxiliary information (e.g., station control, priority) pertaining to the following text block.

4. ERROR CHECKING

a. VRC

Each transmitted character is given odd parity and is checked for parity at the receiving end. In the binary synchronous system, character parity is called Vertical Redundancy Check. If bad character parity is detected the parity flip-flop is set to indicate bad status. Message acknowledgement is controlled by program, but bad status is usually given as a NAK reply.

b. BCC

The entire text block is checked in another way. Each of the parallel bit lines between the buffer and the shift register is monitored by a separate flip-flop. The flip-flop is toggled if a one bit is present, and not toggled if a zero bit is present. At the end of the message block these seven flip-flops represent the odd/even accumulation of the 1's that have been transmitted through that particular character bit position. When an ETB or ETX is detected, the states of the seven flip-flops are transmitted (this is the Block Check Character, or BCC). If the lateral number of 1 bit is even,, the flip-flop is back to the initial or zero state, and if the number is odd the flip-flop is opposite, causing a 1 bit to be transmitted in the BCC.

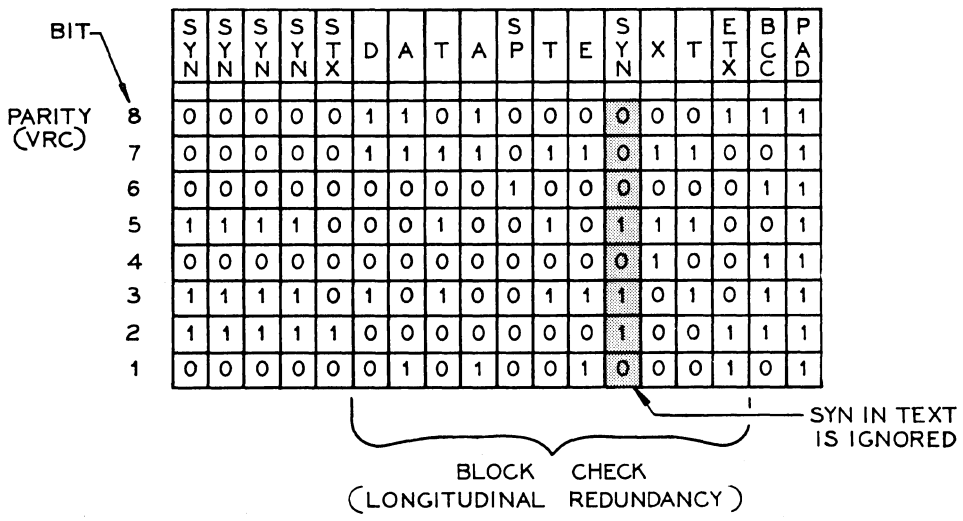


FIGURE 8-8

Meanwhile the receiver checks each data line in the same manner, and compares the receiver block check to the BCC received, setting FAULT if the two do not compare. The block check character (BCC) is not necessarily a USASCII character (except by accident), but the eighth (parity) bit in the BCC is odd parity for that character

only, and not a longitudinal accumulation of all parity bits. Figure 8-8 shows a small message block, and the parity checks that are made. In the example, there is included a hardware generated SYN between text characters to illustrate that SYN's within the text are ignored. Except for character phase at the beginning of a message, SYN's are time fillers, and are not a part of text or parity checks. In a half duplex system a pad character (all 1's) follows all transmissions. The pad character ensures complete transmission of the last significant character before the transmitter shuts off. In a constant carrier system the pad character is transmitted constantly while the station is receiving (over the other half of the line).

5. DATA-LINK CONTROL

The OLCA uses the following eleven control codes to maintain order of operation.

SYN--Synchronous Idle

Establishes synchronism, and is a time-fill, in the absence of data or control characters, to maintain synchronism.

SOH--Start of Heading

Precedes a block of heading characters. A heading consists of auxiliary information (such as routing and priority) that may be necessary for the system to process the text portion of the message. The SOH character is not included in the block check count.

STX--STart of Text

Precedes a block of text characters. Text is that portion of a message, treated as an entity, to be transmitted to the ultimate destination without change. STX also terminates a heading. The STX character is not included in the block check count.

ETB--End of Transmission Block

Indicates the end of a group (block) of characters started with SOH or STX. The blocking structure is not necessarily related to the processing format. The block-check character is sent immediately following ETB, ETB requires a reply indicating the receiving station's status (ACK 0, ACK 1, or NAK) ETB character bits are included in the block check count.

ETX--End of Text

Terminates a block of characters started with STX and transmitted as an entity. The block-check character is sent immediately following ETX. ETX requires a reply indicating the receiving station's status. ETX character bits are included in the block check count.

EOT--End of Transmission

Indicates the conclusion of a message transmission, which may contain one or more blocks, including text and associated headings. It causes a reset of all stations on the line.

ENQ--Enquiry

Used as a request for a response, to obtain identification and/or an indication of station status (ACK 0, NAK, etc.). It can also be used to obtain a repeat transmission of a reply, if a transmission was not received when expected or was garbled.

ACK 0, ACK 1--Affirmative Acknowledgement

These replies indicate the previous block was accepted and the receiver is ready to accept the next block of the transmission.

ACK 0 and ACK 1 are each made up of two USASCII characters: a DLE followed by the corresponding digit. Thus: ACK0=DLE,0, ACK 1=DLE,1.

Single ACK's, or alternating ACK 0 and ACK 1 replies may be used. ACK 1 and ACK 0 provide for sequential checking of a series of replies. Thus it is possible to maintain a running check to ensure that each reply corresponds to the immediately preceding message block. (NOTE: ACK 0 is used as the positive reply to normal selection.)

NAK--Negative Acknowledgement

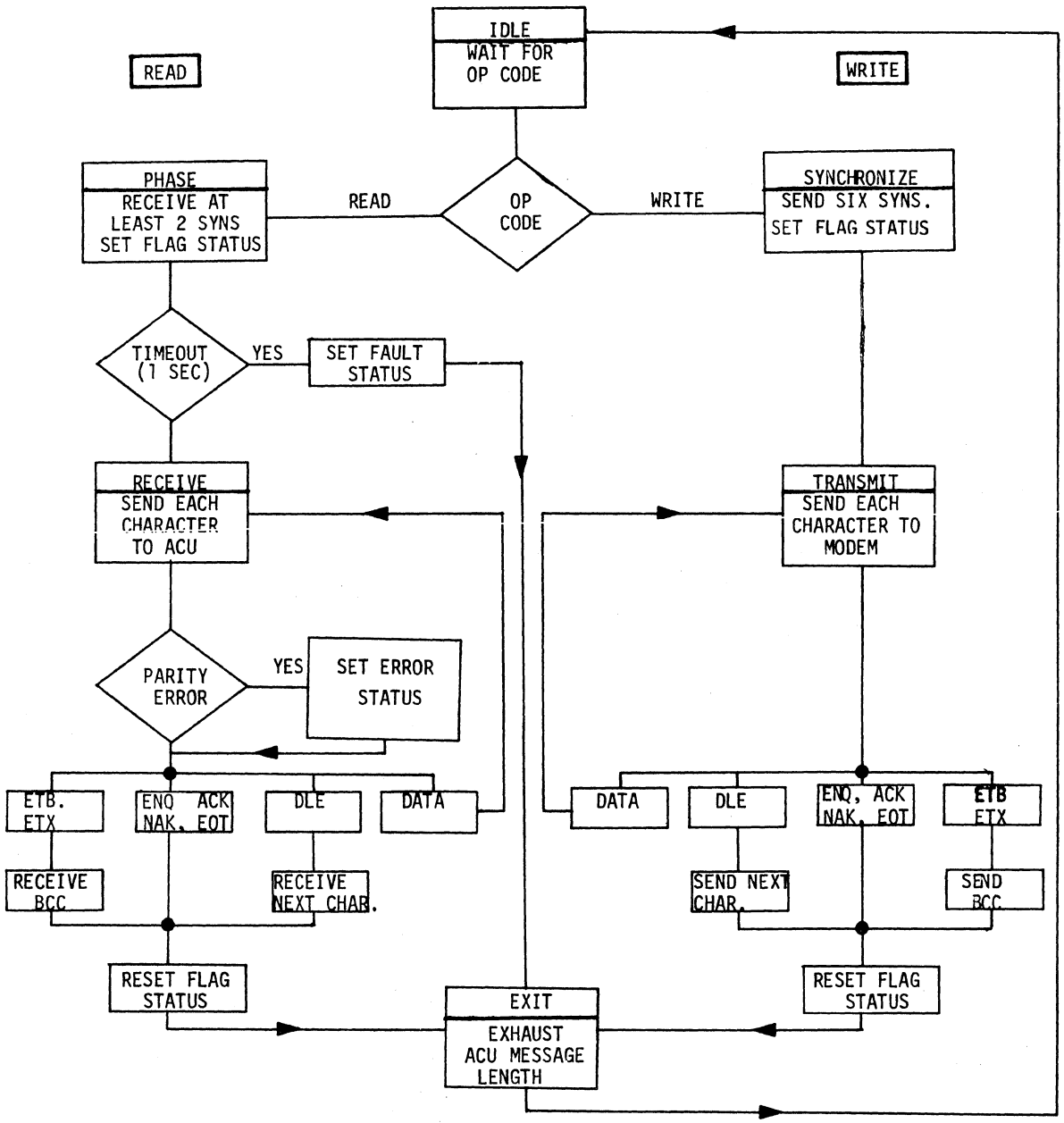
Indicates that the previous block was unacceptable, and the receiver is ready to accept a retransmission of the erroneous block. It is also the "not-ready" reply to a station selection.

DLE-Data-Link Escape

A control character used exclusively to provide supplementary line control signals.

Alternating Affirmative Acknowledgements

WABT--Wait-Before-Transmit-Sequence - a temporary not-ready condition.



FLOW CHART, BASIC OPERATION

GENERAL OPERATION FLOW CHART

FIGURE 8-9

D. OLCA GENERAL OPERATION

The OLCA has two active operating conditions, when the processor is READing, and when the processor is WRITEing. When either of these instructions are finished, the OLCA goes to the EXIT condition, then to IDLE, where it waits for a new instruction from the processor. Figure 8-9 is a simplified flow chart of the general operation of the OLCA.

When the OLCA begins any instruction, FLAG is set. Only if the message block is completed, and the BCC transferred, is FLAG reset. Message completion is detected by receiving an ending character (see DATA LINK CONTROL).

1. IDLE

During IDLE, no data is transferred, and the OLCA is waiting for instructions. If a READ op is received, the OLCA enters the READ condition; a WRITE op places the OLCA in the WRITE condition.

2. READ

The READ condition can be considered in two parts; PHASE, and RECEIVE.

a. PHASE. The OLCA needs at least two consecutive SYN characters to lock into character phase with the incoming signals from the modem. If it is communicating with a foreign computer, the OLCA will usually receive more than two SYN's. All SYN's received after character phase is established are ignored, except as time fillers to retain synchronization. If the two required SYN's are not received within approximately 1 second, the OLCA "times out", sets FAULT status, and goes to the EXIT condition.

b. RECEIVE. In RECEIVE, each character code is received, bit serially from the modem, tested for odd parity, tested for Data Link Codes, and sent to the ACU through the FAC-DATA Lines.

3. WRITE

The WRITE condition, like READ, can be considered in two states, SYNCHRONIZE and TRANSMIT.

a. SYNCHRONIZE is the preface to each transmission where six SYN's are sent, allowing the foreign computer to acquire bit synchronization, then character synchronization. There is no pause between this state and TRANSMIT, as synchronization must be kept.

b. TRANSMIT is the normal sending of data and Data Link Control characters. Each character received on the FAC bus is converted to a standard odd parity eight-bit character. It is also tested for any of the Data Link Control characters that may cause special actions.

E. DETAILED OPERATION

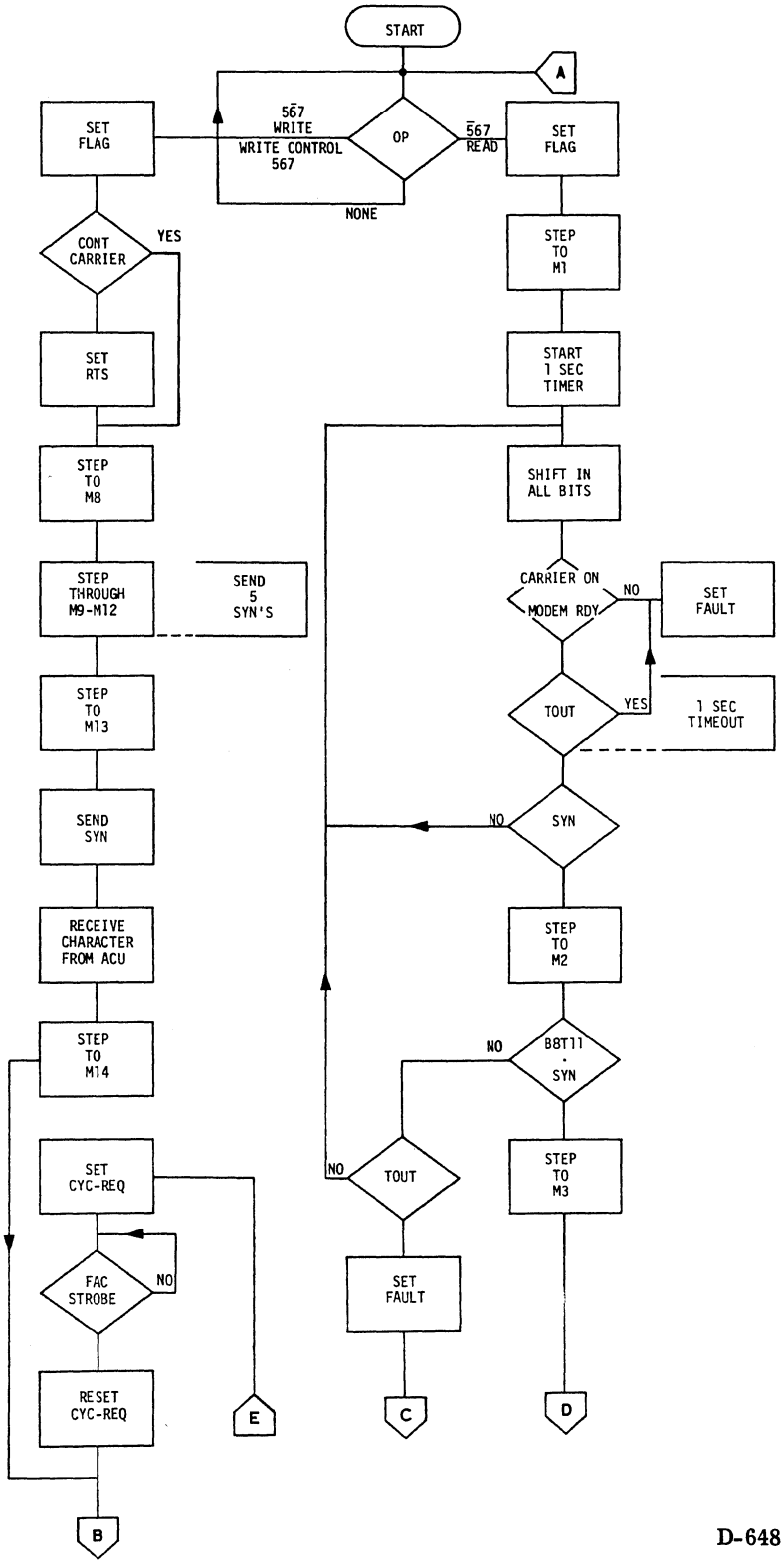
Operation of the OLCA can be detailed as 16 functional states or modes. The following information is arranged to step through each mode, analyzing the important functions within the operation. Overall concept of system operation is given in Figure 8-10, which is a functional flow chart of OLCA logic actions. A quick reference table of general activities within each mode is given below. In actual operation, the states do not occur in numerical order.

MODE	GENERAL OPERATION
Ø	Idle, waiting for instructions.
1	Phase, first of two for acquiring character phase.
2	Confirm Phase, character phase is established.
3	Receive, data is accepted from foreign source.
4	Receive Block Check Character.
5	Compare BCC.
6	Transmit Block Check Character.
7	EXIT, ends active op code, and steps to mode Ø.
8 through 12	Transmit five SYN characters for synchronization.
13	Transmit sixth SYN for synchronization.
14	Transmit data.
15	Transmit pad character.

1. MØ, IDLE

An inactive state where the OLCA is waiting for instructions from the processor. It is neither transmitting or receiving data. The DLE, TEXT, and INHIBIT flip-flops are reset during MØ (at B1-16 time). During MØ the bit counter is held at one. Each T8 time the op code register is tested for READ, WRITE, or WRITE CONTROL. If an instruction is detected, the mode is stepped at the following B1-T3 time. A WRITE or WRITE CONTROL causes the OLCA to enter the first synchronize state (M8). A READ instruction places the OLCA in the PHASE state (M1).

Other IDLE mode (MØ) functions are independent of time. If the Modem-ready signal is not present when the FAC instruction arrives, the OLCA steps to the EXIT mode (M7).



D-648

OLCA LOGIC FLOW

FIGURE 8-10

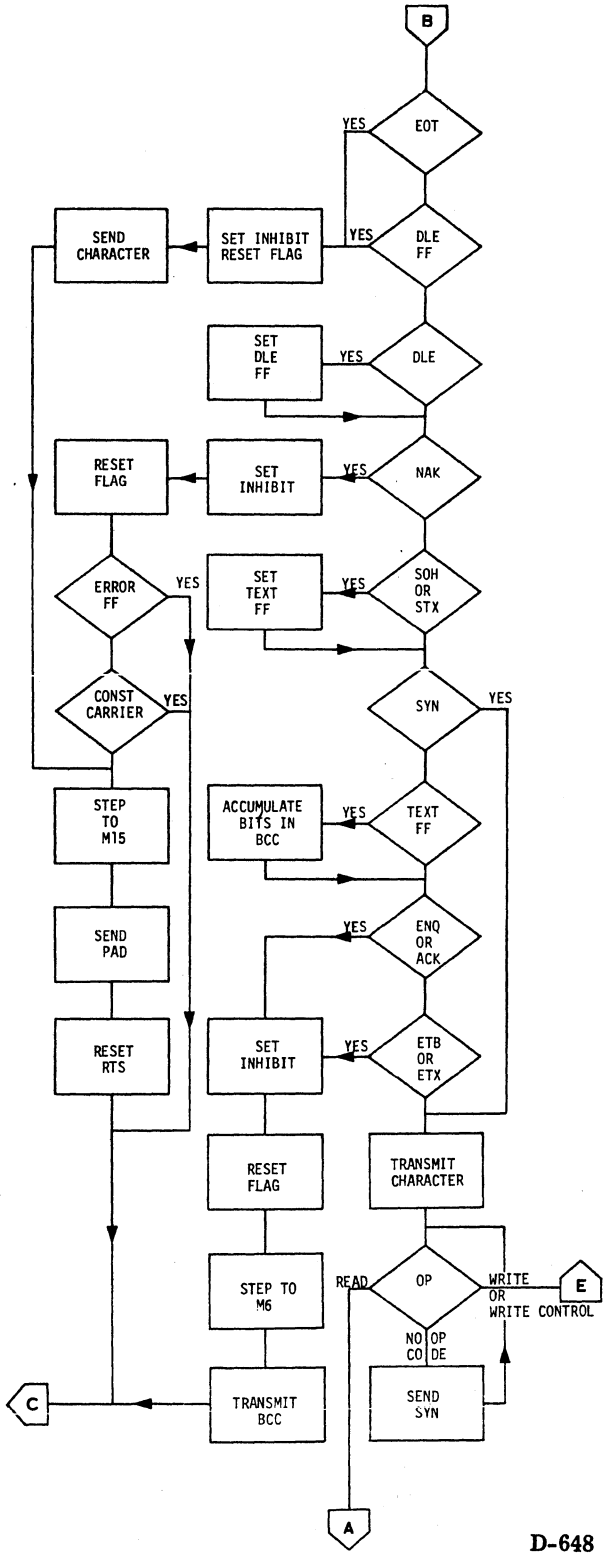


FIGURE 8-10 (cont.)

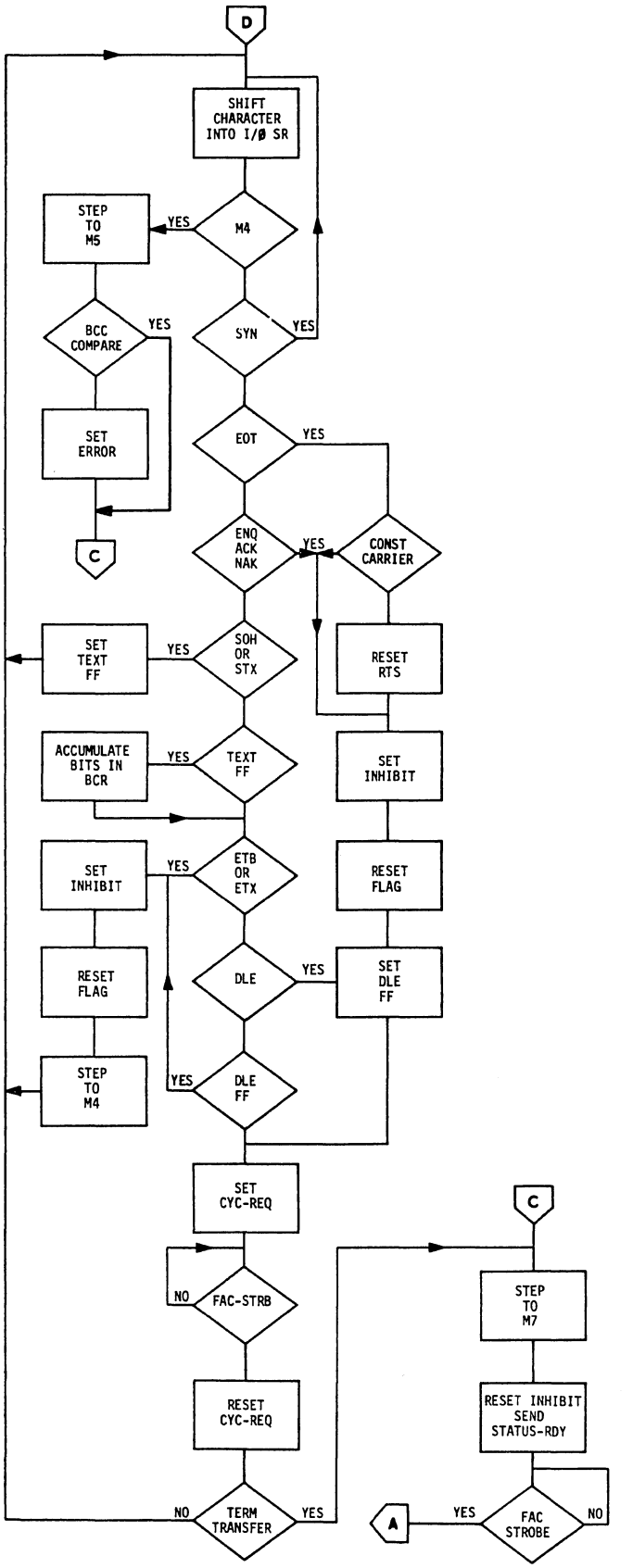


FIGURE 8-10 (cont.) D-648

2. M1, PHASE

The first of two states where the OLCA is establishing character phase with the incoming data. Data from the REC-DATA line is serially shifted into the I/O shift register. Each bit time (at T10) a test for the SYN code is made. When the register contains one SYN code, the mode is stepped to M3, Confirm Phase (at B1-T3). Tentative character phase is established at this time. If either the DATA-CARRIER or DATA-SET-READY signals are not present in M1, the OLCA transfers to EXIT (M7), and sets FAULT.

3. M2, CONFIRM PHASE

Following detection of the first SYN in mode 1, eight more bits are counted into the register and tested for a SYN. If the character (or scramble of bits) is not a SYN, the mode counter is decremented to MØ, and the Phase process starts again (the READ op would still be active). Once character phase is established, the mode changes to receive (M3) at B8-T11.

A time limit of one second (±30%) is given to establish character phase. If it is not established in that time, FAULT and TOUT (timeout) flip-flops are set and the EXIT mode (M7) is entered.

4. M3, RECEIVE

Characters are shifted bit serially into the I/O Shift Register. SYN codes are not transferred to the processor, and are not Accumulated in the block check character. An SOH or STX code sets the TEXT flip-flop and thereafter all one bits (except those in SYN's) are accumulated in the block check.

Receiving an ETB or ETX stops the block check, and causes a transfer to transmit (M4). However the ETB or ETX character is included in the block check accumulation.

A terminating character (EOT, ENQ, ACK, or NAK) causes a transfer to EXIT, however FLAG is reset.

A DLE and any character following is equivalent to a terminating character.

Any of the block ending (ETB, ETX) or terminating characters reset FLAG, and set INHIBIT, which in turn inhibits STATUS-READY. This prevents a new FAC operation before the OLCA has terminated the previous operation.

An EOT causes the RTS (request to send) signal to clear.

5. M4, RECEIVE BCC

Entered only after receiving an ETB or ETX on the REC-DATA line. During this mode the block check character (from the foreign computer) is received, and shifted into the I/O Shift Register. The mode is then stepped to M5.

6. M5, COMPARE BCC

The block check character is the last eight bits of the received data message. It is compared with the contents of the OLCA block check register, and if the two are not identical, ERROR is set. In any case, EXIT is entered at B8-T11 time.

7. M8 THROUGH M12, SYNCHRONIZE

Before each transmission the OLCA automatically inserts six SYN characters. The first five SYN's are sent in modes 8 through 12, then a transfer is made to M13.

8. M13, END SYNCHRONIZATION

The last of six SYN's is transmitted, and the first character from the ACU is fetched. At B8-T8 time, the mode is stepped to M14 (Transmit).

9. M14, TRANSMIT

The OLCA enables CYCLE-REQUEST (at B1-T11), receives a six bit character from memory (through the M and N bus), converts it to the standard USASCII eight bit-odd parity character, and transmits it. After each character, the op code register is checked to verify that the WRITE or WRITE CONTROL instruction is still there. If so, transmission continues; if not, SYN's are inserted as time fillers until the op returns. If a READ op is present, the mode is stepped to MØ.

As in Receive, an SOH or STX sets the TEXT flip-flop, and all following characters (except SYN's) are accumulated in the block check. An ETB or ETX causes a transfer to M6 (Transmit BCC).

A DLE sets the DLE flip-flop, and when the next character arrives, the two are considered a terminating code. Any terminating code (EOT, ENQ, ACK, or NAK) resets FLAG, and is a normal ending. Any block ending (ETB, ETX) or terminating code sets INHIBIT.

An EOT causes a transfer to M15 (Transmit Pad), providing the OLCA is not operating continuous carrier.

An ENQ or ACK character causes a transfer to EXIT.

NAK can be a negative response to selection, or an indication of an error in the last received message. In the case of an error in the previous message, the ERROR flip-flop will still be set, and a NAK will cause a transfer to EXIT. In the case of a negative response (ERROR not set) a NAK initiates a transfer to M15 (Transmit Pad).

10. M6, TRANSMIT BCC

Occurs only after an ETB or ETX is sent. At the following B8-T8 time, FLAG is reset, and the mode stepped to EXIT.

11. M15, TRANSMIT PAD

Only used when not operating continuous carrier. A pad character of all 1's is transmitted to ensure enough carrier length to complete the message, and turn-off procedures. After the pad is transmitted, the RTS (request to send) signal is cleared, and the OLCA transfers to the EXIT mode.

12. M7, EXIT

Ends an active op by automatically returning STATUS-READY to the processor, independent of the TERMINATE-TRANSFER signal from the ACU. When the ACU has read the status character, the OLCA steps to MØ (Idle).

The EXIT mode is entered when a terminating character is detected (either while transmitting or receiving), or if FAULT is set.

13. STATUS

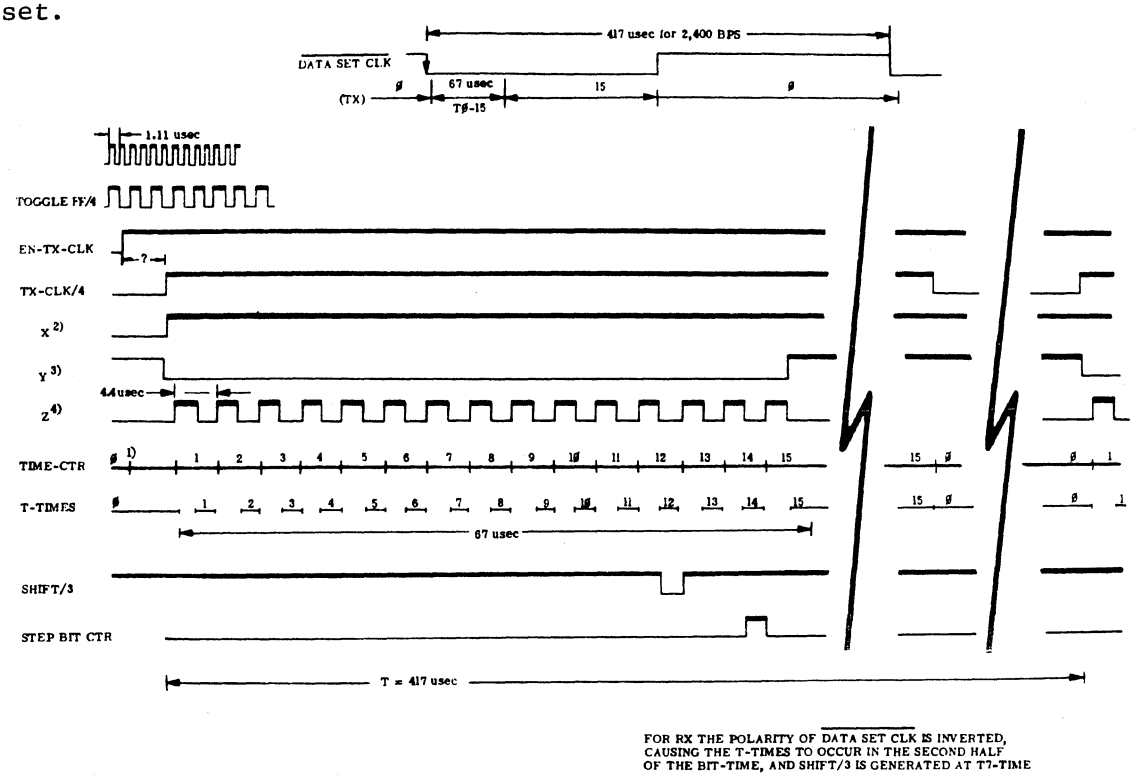
Three status indications can be given by the OLCA, ERROR, FAULT, and FLAG. These conditions will be set by the following:

a. ERROR is set if a parity error is detected during reception, however, the message is not interrupted. An unequal block check also sets ERROR. ERROR cannot be set during a WRITE instruction.

b. FAULT is set if the OLCA times out, or if the modem is inoperative.

c. FLAG indicates an incomplete message block, either sending or receiving. FLAG is set before each instruction, and reset when an ending character is received.

NOTE: If the OLCA times out before finishing a message, both FLAG, and FAULT will remain set.



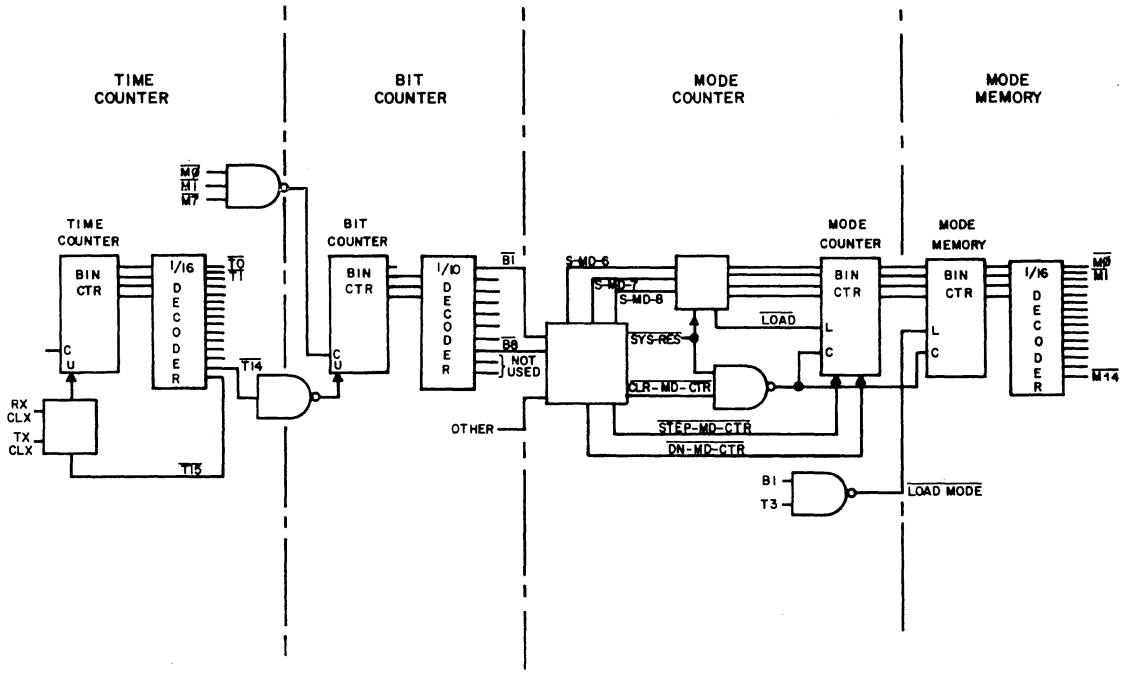
OLCA TIMING CHAIN

FIGURE 8-11

14. TIMING

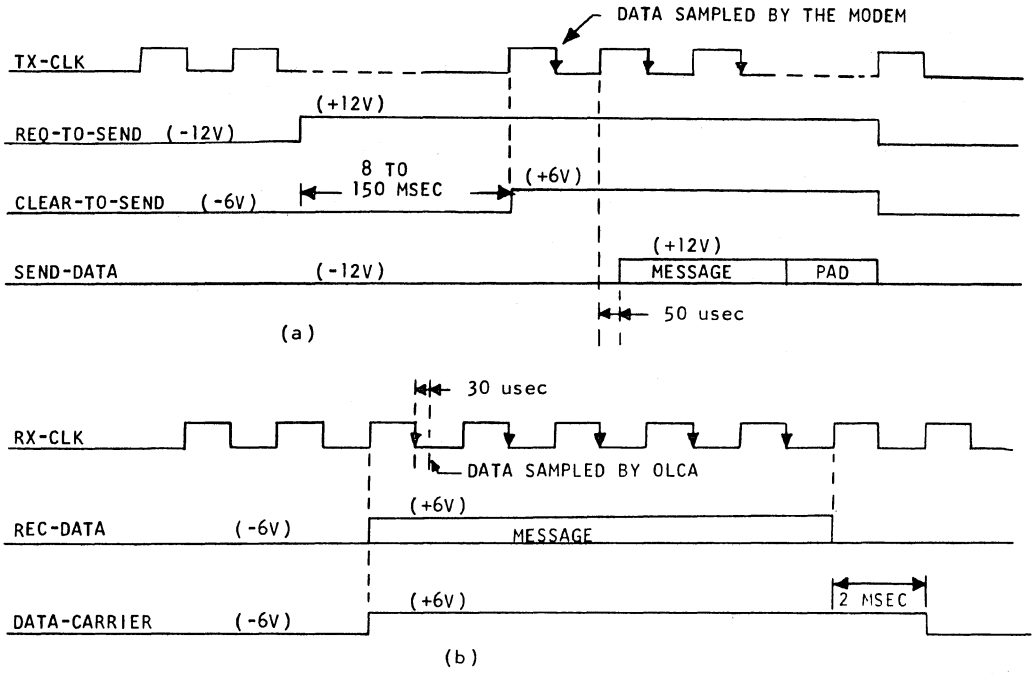
The basic timing signals used by the OLCA are shown in Figure 8-11. These timing signals originate from a variety of sources. Figure 8-12 shows the basic timing elements of the OLCA. The basic clock is the FAC-CLK signal (900 KHz) provided by the ACU. When sending or receiving, an individual bit is gated by the TX-CLK or RX-CLK signal from the modem, both of which cycle at the rate of 2400 bits/sec. The T0-T15 signals, occurring at 4.4 sec intervals, enable the OLCA to complete all of its operations well within the time allotted by the modem clocks, so that the modem never waits for the OLCA. The result is that data is actually transmitted at the rate of 2400 bps.

Timing is also dependant upon the two interfaces (modem and ACU). Figure 8-13 shows the timing relationship involved in the interface operation.

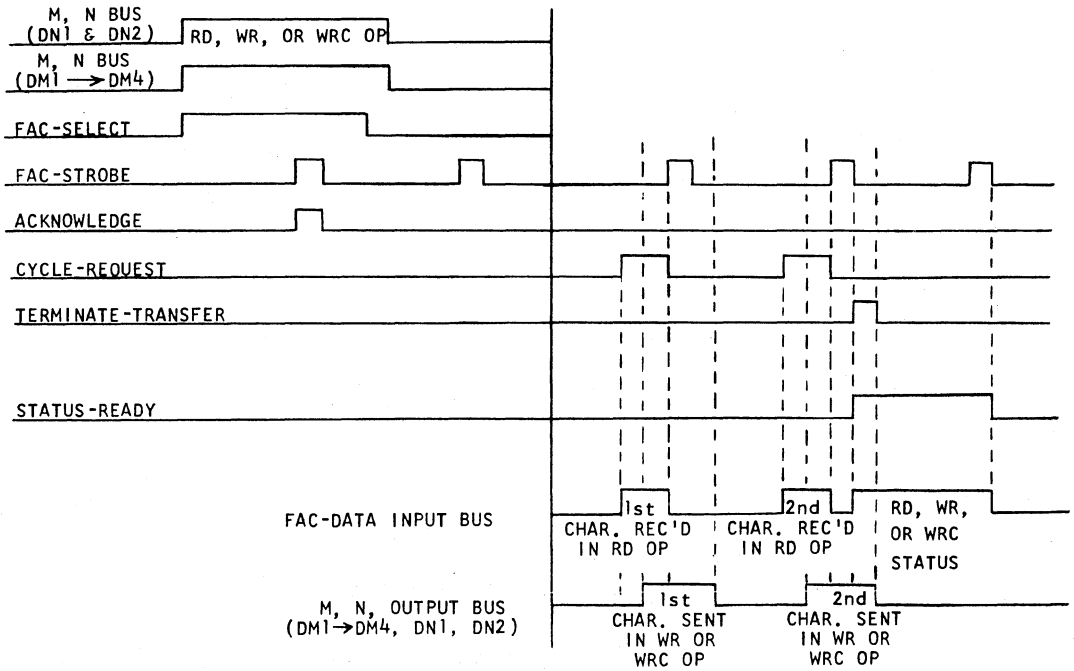


OLCA TIMING BLOCK DIAGRAM

FIGURE 8-12



RS-232-B INTERFACE TIMING



FAC BUS TIMING

FIGURE 8-13

F. GLOSSARY

BCR - Block Check Register; for horizontal redundancy check.

Bit Counter
Bit Decoder - Defines 8 bit positions (B1 through B8) relative to Modem timing. Corresponds to the 8 USASCII bits.

CBR - Character Buffer Register; a temporary storage for 7 bit characters during input and output operations. When transmitting, the next character to be sent is generated and stored in the character buffer register. When receiving, the character is assembled and stored in the character buffer register until it can be transferred to the processor.

Control Character Detector - Two decoder chips for detecting control character codes in the character buffer.

CYC-REQ - Cycle Request; a signal to the ACU requesting an FAC cycle to transfer data.

DIV-6 CTR
DIV-12 CTR - A divide by 192 counter for timing when directly connected to a foreign computer. Divides the 900 KHz FAC-CLOCK signal to produce 4.7 KHz AUX-CLOCK signal.

DLE - Flip-Flop that is set when a DLE code is transmitted or received.

ERROR - Reports parity or transmission errors.

FAULT - Reports when the Modem is not ready, or when the OLCA times out.

FLAG - Reports when an inappropriate terminating condition occurs.

HRC - Horizontal redundancy check; block check.

INHIBIT - Inhibits STATUS READY until Mode 7, T12.

Mode Counter - Decodes conditions for mode changes;
Mode Memory - Buffer for Mode Counter; allows decoder to load at selected times.
Mode Decoder - Decodes states (modes) Ø-15 from mode counter.

I/O SHIFT REGISTER - Serial/parallel converter for input and output data during WRITE, WRITE CONTROL, and READ operations. Receives serial data from REC-DATA line in READ, and parallel data from the character buffer when in WRITE, or WRITE CONTROL. Sends serial data onto SEND-DATA line when transmitting.

MPX - Multiplex Logic; operated by control logic, it determines which of four data sources will be gated to the character buffer register. In WRITE, data can come from the FAC OUT-DATA lines, or a SYN can be inserted for time fill (to retain synchronization), or the Block Check Character can be inserted. In READ, data comes from the I/O Shift Register.

Op Code Decoder - Decodes the OP codes from processor

Op Code Register - Temporary storage for incoming instructions from the ACU.

PARITY GEN - Generates character parity (odd) when sending, and checks character parity when receiving.

PER - Parity Error flip-flop; reports errors in either VRC or HRC.

RDY-TO-TXF - Ready to transfer; OLCA is ready for next character from the ACU when transmitting.

RTS - Request to send flip-flop; generates signal to modem.

RXFF - Causes DATA-SET-CLK to follow RX-CLK during READ Modes (M1, 2, 3, and 4).

SD - Send Data flip-flop; sets and resets to create data bits on the send data line - is fed by the I/O Shift Register.

STOP-CNT - Stop Count

STATUS - Qualifies status bits to the FAC-DATA lines.

TEXT - Set by an SOH or STX being transmitted or received; starts Block Check accumulation.

Time Counter - Generates sixteen time slots of approximately 2.2 μsec each for every Modem bit interval. Between these time slots are dead times of approximately 2.2 μsec.

Time Decoder - Decodes timing signals for sequencing.

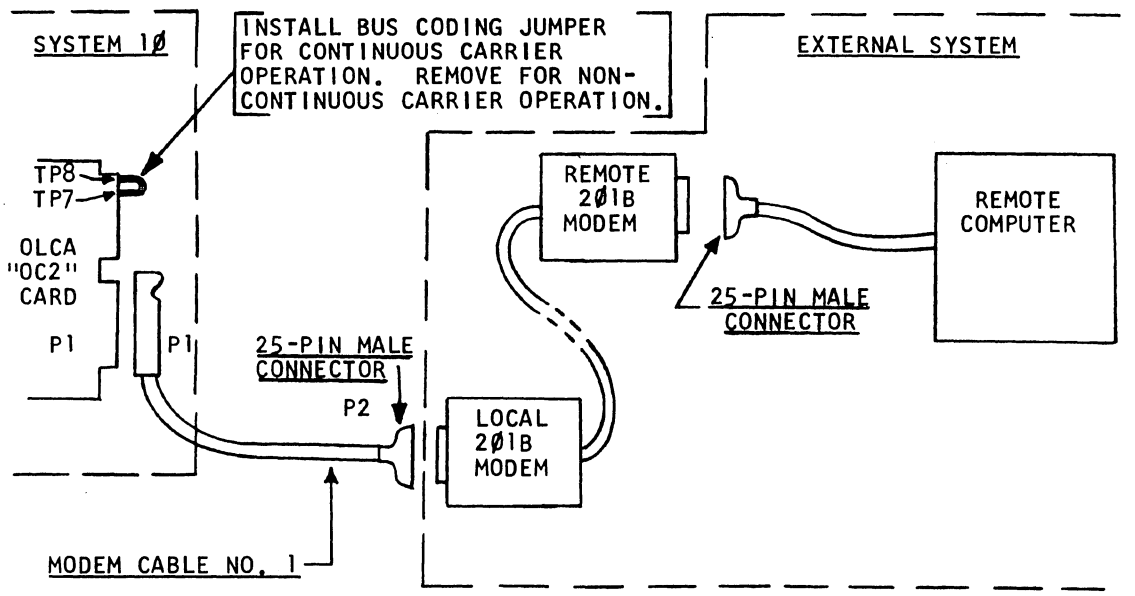
TIMEOUT - One-shot allows approximately one second to acquire character phase. Terminates a READ operation in FAULT.

TOUT - Timeout flip-flop; set by TIMEOUT one-shot.

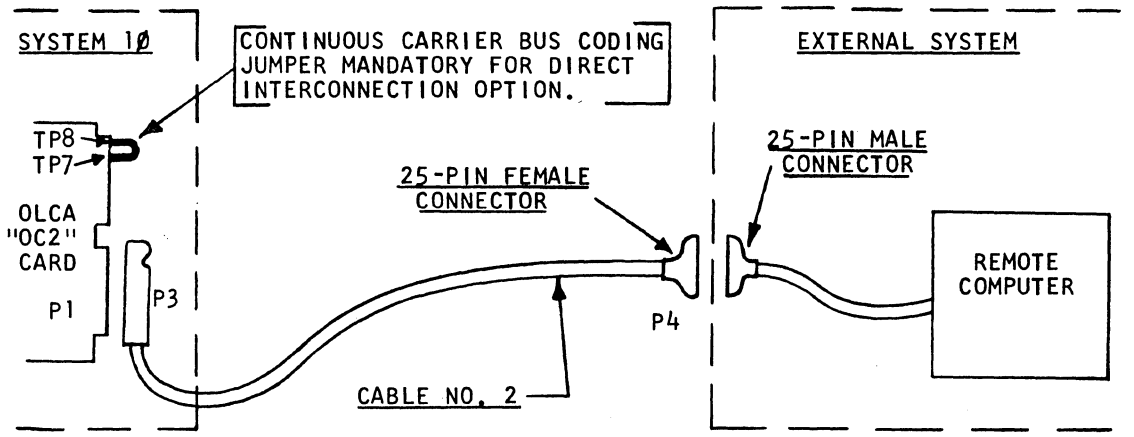
TXFF - Causes DATA-SET-CLK to follow TX-CLK during all modes except M1, 2, 3, and 4.

VRC - Vertical redundancy check; odd character parity.

G. REFERENCE



(a) STANDARD INSTALLATION

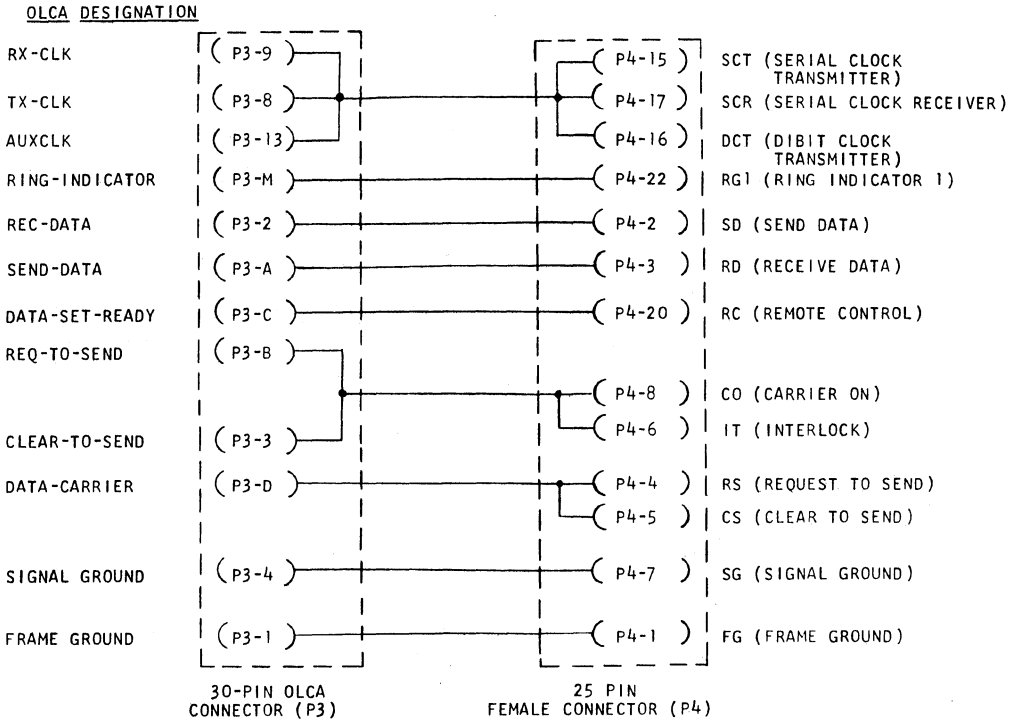


(b) DIRECT INTERCONNECTION OPTION

INSTALLATION OPTIONS

INSTALLATION OPTIONS

FIGURE 8-14



CABLE ARRANGEMENT FOR DIRECT INTERCONNECTION OPTION

CABLE ARRANGEMENT FOR DIRECT INTERCONNECTION OPTION

FIGURE 8-15

OLCA TIMING M0 AND M1

MODE	MØ - IDLE	M1 - PHASE
DESCRIPTION	WAITING FOR OP CODE - BIT CLK: TX-CLK	DETECT 1st SYN - BIT CLK: RX-CLK
B1-T3	LOAD MODE MEMORY	LOAD MODE MEMORY
B1-T6	CLEAR DLE, TEXT, AND INHIBIT FF's	
B1-T7	-	SHIFT I/O SR
	OP = READ → STEP MODE RDY-TO-SEND → S-M8	-
B1-T9	-	LOAD CBR
B1-T1Ø	-	CD = SYN → STEP MODE
B1-T11		$\overline{\text{CARRIER-ON}} + \overline{\text{MODEM-RDY}}$ → S-FAULT, S-M7
B1-T12	SHIFT I/O SR (DUMMY)	

NOTES:

1. In MØ and M1, the Bit Counter is held constant at B1.
2. RDY-TO-TXF · MODEM-RDY · MØ → S-M7 (Not time dependant)
3. OP = WR-WRC MØ → S-RTS.
4. OP = READ MØ → Trigger Timeout.
5. In M1, If TOUT → S-FAULT.
6. RDY-TO-SEND = (OP=WR-WRC) · CLR-TO-SEND.
7. See Table 8-2 Notes 1, 2, and 4.

OLCA TIMING M2 AND M3

MODE / DESCRIPTION	M2 - CONFIRM PHASE DETECT 2nd SYN - IF FAIL, GO TO M1 - BIT CLK: RX-CLK	M3 - RECEIVE RECEIVE BIT SERIAL - XFER IN PARALLEL TO FAC BIT CLK: RX-CLK
B1-T3	LOAD MODE MEMORY	LOAD MODE MEMORY
B1-T7	SHIFT I/O SR	SHIFT I/O SR
B1-T14	STEP BIT CTR	STEP BIT CTR
B8-T7	SHIFT I/O SR	SHIFT I/O SR
B8-T8	LOAD CBR LOAD CB	LOAD CBR
B8-T9	-	CD=EOT → C-RTS TEXT → START BCC
B8-TØ	-	CD=SOH-STX → S-TEXT CD=SYN → STOP BCC CD=ETB-$\overline{\text{ETX}}$ → STEP MD LAST • $\overline{\text{SYN}}$ → R-FLAG CD=$\overline{\text{ENDING}}$ • $\overline{\text{SYN}}$ → S-M7 CD=SYN → S-CYC-REQ
B8-T11	CD=SYN → STEP MODE CD=$\overline{\text{SYN}}$ → DN-MODE CHECK PARITY	NOT-RDY-TXF • $\overline{\text{LAST}}$ → CLR MODE OP=WR-WRC → CLR MODE CHECK PARITY
B8-T12	-	CD=DLE → S-DLE
B8-T14	STEP BIT CTR	STEP BIT CTR

NOTES:

1. M3 • LAST → S-Inhibit.
2. In M2, If TOUT → S-FAULT.
3. See Table 8-2 Notes 1, 2, and 3.

OLCA TIMING M4 AND M5

MODE	M4-RECEIVE BCC	M5-COMPARE BCC
DESCRIPTION	RECEIVE BCC - BIT CLK: RX-CLK	COMPARE CONTENTS OF BCR WITH BCC - BIT CLK: TX-CLK
B1-T3	LOAD MODE MEMORY	LOAD MODE MEMORY
B1-T5	-	TEST BCC BITS
B1-T7	SHIFT I/O SR	SHIFT I/O SR
B1-T14	STEP BIT CTR	STEP BIT CTR
B7-T1Ø	-	TEST BCC CHARACTER
B8-T5	-	TEST BCC BITS
B8-T7	SHIFT I/O SR	SHIFT I/O SR
B8-T8	LOAD CBR	LOAD CBR
B8-T11	STOP BCC STEP MODE CHECK PARITY	S-M7
B8-T14	STEP BIT CTR	STEP BIT CTR

NOTES:

1. For all Bit Times, M5 • T5 → test BCC bits.
2. See Table 8-2 Notes 1, 2, and 3.

OLCA TIMING M8 → M13

MODE	M8 → M12-SYNCHRONIZE	M13-END SYNCHRONIZATION
DESCRIPTION	SEND 5 SYN's - BIT CLK: TX-CLK	SEND LAST SYN - BIT CLK: TX-CLK
B1-T3	LOAD MODE MEMORY	LOAD MODE MEMORY
B1-T6	LOAD CBR WITH SYN	LOAD CBR WITH SYN
B1-T9	CD=SYN → STOP BCC	CD=SYN → STOP BCC
B1-T1Ø	LOAD I/O SR WITH SYN	LOAD I/O SR WITH SYN
B1-T11	-	S-CYC-REQ
B1-T12	SHIFT I/O SR	SHIFT I/O SR
B1-T14	STEP BIT CTR	STEP BIT CTR
B8=T8	STEP MODE CTR	STEP MODE CTR
B8-T12	SHIFT I/O SR	SHIFT I/O SR
B8-T14	STEP BIT CTR	STEP BIT CTR

NOTES:

1. MPX SET FOR SYN-TO-CBR for M8 → M12, and M13 • B1 • T6.
2. M13 • LAST → S-INHIBIT.
3. See Table 8-2 Notes 2, 3, 4, 5, and 6.

OLCA TIMING M14 AND M6

MODE	M14 - TRANSMIT	M6 - TRANSMIT BCC
DESCRIPTION	TRANSMIT DATA BIT SERIAL-BIT CLK: TX-CLK	TRANSMIT BCC-BIT CLK: TX-CLK
B1-T3	LOAD MODE MEMORY	LOAD MODE MEMORY
B1-T6	-	LOAD CBR WITH BCC
B1-T8	EOT-NAK → STEP MODE CD=ETB-ETX → $\overline{\text{S-M6}}$ CD=ENDING • $\overline{\text{SYN}}$ → R-FLAG CD=ENDING • $\overline{\text{SYN}}$ • $\overline{\text{EOT-NAK}}$ → S-M7 TEXT → START BCC	-
B1-T9	CD=SYN → STOP BCC CD=DLE → S-DLE CD=SOH-STX → S-TEXT	CD=SYN → STOP BCC (DUMMY)
B1-T1Ø	LOAD I/O SR	LOAD I/O SR (DUMMY)
B1-T11	$\overline{\text{RDY-TO-TXF}}$ → $\overline{\text{S-CYC-REQ}}$ RDY-TO-TXF • $\overline{\text{STATUS}}$ → LOAD CBR	-
B1-T12	SHIFT I/O SR	SHIFT I/O SR
B1-T14	STEP BIT CTR	STEP BIT CTR
B8-T8	OP-READ → CLR MODE	R-FLAG STEP MODE
B8-T12	SHIFT I/O SR	SHIFT I/O SR
B8-T14	STEP BIT CTR	STEP BIT CTR

NOTES:

1. In M6, MPX is set for BCC to CBR.
2. M14 • LAST → S-INHIBIT.
3. See Table 8-2 Notes 2, 3, 4, 5, and 6.
4. EOT-NAK = EOT + NAK • $\overline{\text{ERROR}}$.

OLCA TIMING M15 AND M7

MODE	M15 - TRANSMIT PAD	M7 - EXIT MODE
DESCRIPTION	TRANSMIT PAD WHEN RTS IS TO BE DEACTIVATED - BIT CLK: TX-CLK	TERMINATE OP CODE BY RETURN OF STATUS BIT CLK: TX-CLK
B1-T3	LOAD MODE MEMORY	LOAD MODE MEMORY
B1-T12	SHIFT I/O SR	R-INHIBIT SHIFT I/O SR RDY-TO-TXF • $\overline{\text{STATUS}}$ → S-STATUS
B1-T14	STEP BIT CTR	-
B8-T8	S-M7 C-RTS	
B8-T12	SHIFT I/O SR	
B8-T14	STEP BIT CTR	

NOTES:

1. In M7, the Bit Counter is held at B1.
2. M7 • STATUS • FAC-STROBE → CLR MODE.
3. See Table 8-2 Notes 2, 3, 4, and 5.

OLCA TIMING, MISC NOTES

NOTES:

1. For M1 through M5, shift I/O SR every bit time at T7.
2. TOUT is held reset by all except M1 and M2.
3. In M2 through M6, and M8 through M15, step bit counter every T14.
4. In MØ, and M6 through M15, shift I/O SR every T12 independent of bit time.
5. For M6, and M8 through M14, if $\overline{\text{MODEM-RDY}}$ + RTS · $\overline{\text{MØ}}$ · $\overline{\text{CLR-TO-SEND}}$, then S-FAULT and S-M7 independent of bit time.
6. NOT-RDY-TXF · M14 · $\overline{\text{ENDING}}$ → SYN-TO-CBR.
7. REC-MODES: 1, 2, 3, 4 and 5.
8. RX-MODES: 1, 2, 3 and 4.
9. TXM-MODES: 6, 8, 9, 10, 11, 12, 13 and 14.
10. $\overline{\text{MODEM-RDY}}$ → S-FAULT.
11. FAC-STROBE · STATUS → C-FAULT.
12. OP = READ · ACKNOWLEDGE → C-ERROR.
13. SYS-CLR → C-FAULT, C-FLAG, C-RDY-TO-TXF, C-ERROR, C-RTS, C-CYC-REQ, C-OP-CODE, C-STATUS.
14. SYS-CLR = SYSTEM-RESET + (Manual Switch S1 "ON").
15. ACKNOWLEDGE → LOAD OP CODE, S-FLAG.

USASCII MESSAGE FORMAT

Data Messages

1. (SYN) ... (SYN) (STX) (Data Message) (ETB or ETX) (BCC)

2. (SYN) ... (SYN) (SOH) (Heading) (STX) (Data Message) (ETB or ETX) (BCC)

1. (SYN) ... (SYN) (NAK)

2. (SYN) ... (SYN) (ACK)

3. (SYN) ... (SYN) (DLE) ( ), where = EOT, Ø or 1.

4. (SYN) ... (SYN) (EOT)

5. (SYN) ... (SYN) (ENQ)

6. (SYN) ... (SYN) (β) (ENQ), where β = alphanumeric character sequence

NOTE: (SYN) ... (SYN) = 6 or more SYN's for OLCA in transmit. At least 2 SYN's are required.

SECTION 9

MDTS IOC

SECTION CONTENTS

LIST OF ILLUSTRATIONS

SECTION 9

MDTS IOC

TABLES

SECTION 9, MDTS IOC

A. INTRODUCTION

The MDTS I/O channel supervises communication between the ACU portion of the central processor and a maximum of ten data terminals. Each terminal electrically connects to the I/O through a unique two-wire pair.

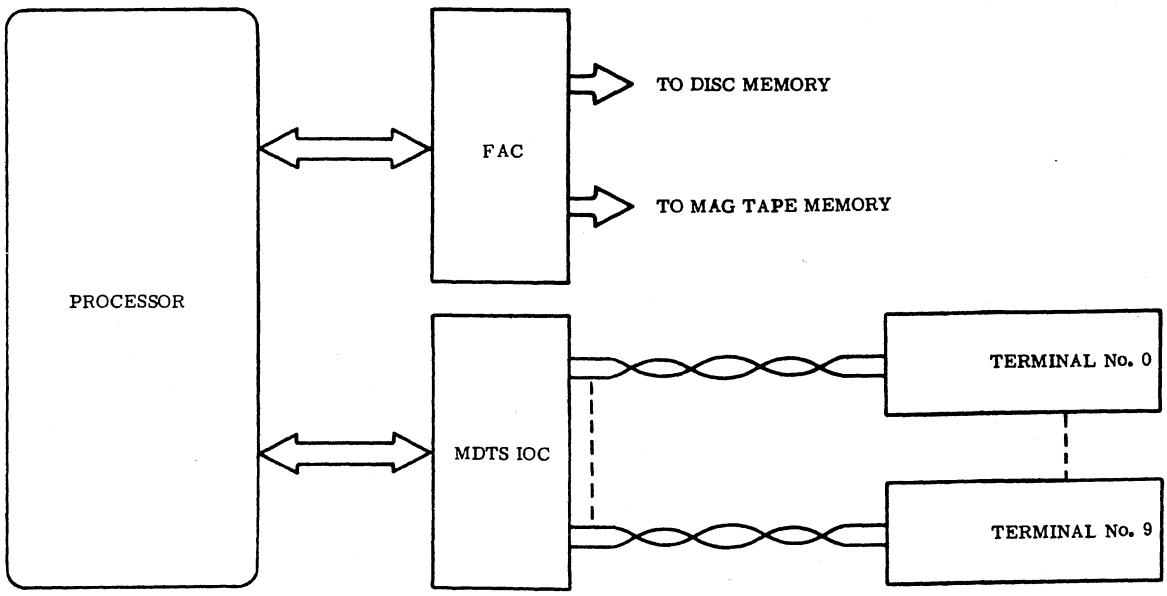
All communication is initiated by the data terminal. If one or more replies or acknowledgements are to be made, they are transmitted from the I/O immediately following the terminal message. Normally disconnect is made by the terminal, but the I/O will time out and return to polling if the terminal does not disconnect within 7 bit times after the IOC reply is completed.

Figure 9-1 shows the relationship of the terminals to the other units of System Ten. Information comming to the MDTS I/O must be placed in Main Memory before entering other recording devices.

An overall block diagram of MDTS logic action is shown in figure 9-2.

B. PROCESSOR/MDTS IOC COMMUNICATION

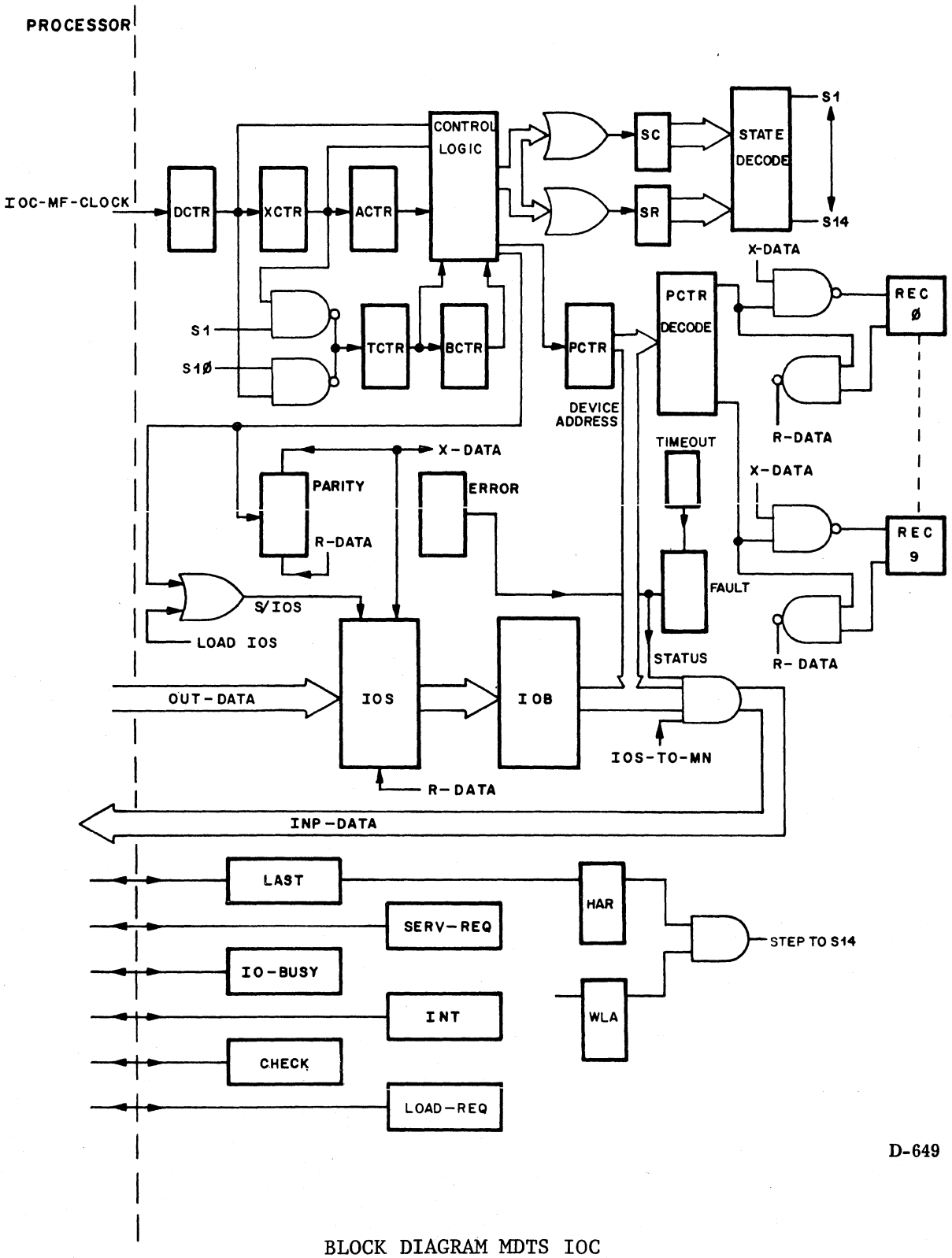
All MDTS IOCs are parallel-buss interfaced to the Arithmetic Control Unit (ACU) within the Processor. Interface signals are common to all I/O channels. The Processor selects only one IOC at a time, with which it then communicates on the common bus; all other (unselected) IOC's are blocked from the bus. Figure 9-2 shows the interface signals between the MDTS IOC and the Processor.



D-688

MDTS SYSTEM

FIGURE 9-1

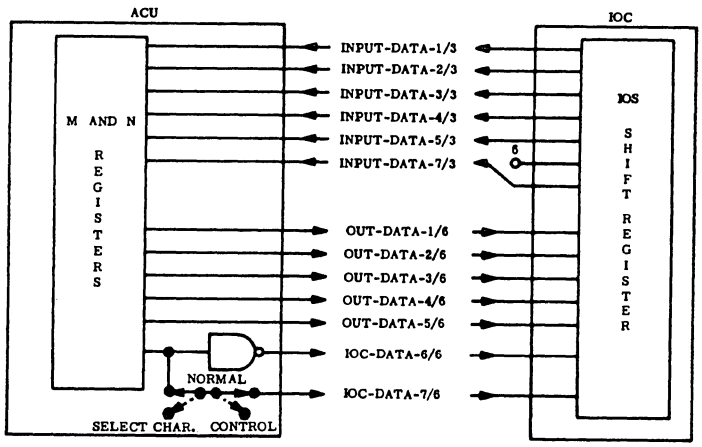


BLOCK DIAGRAM MDTS IOC

FIGURE 9-2

1. INTERFACE SIGNALS

The "digit" and "group" signals from the Processor uniquely select any particular IOC and develop the ON-LINE signal, enabling all Processor/IOC interface signals except the INTERRUPT and data lines. INTERRUPT and data lines are enabled during the working cycle of the IOC, and are used to implement data transfer to and from the Processor. The data lines are shown in Figure 9-3.



I/O DATA LINES D-793

FIGURE 9-3

a. ACU SIGNALS

(a) C/INT/5: Clears the INTERR FF in the IOC after a character has been transferred between the ACU and the IOC.

(b) C/LD-REQ/5: Clears the LDRQ FF in the IOC at the completion of a Load function.

(c) C/SERV-REQ/5: Clears the SVRQ FF in the IOC after a Branch if Service Request instruction has been executed.

(d) IOC-MF-CLK/2: A 300 KHz clock signal providing the basic timinggfor the IOC logic circuits.

(e) IOS-TO-MN/5: Gates the contents of the IOS shift register in the IOC onto the S bus.

(f) LOAD-IOS/5: Loads the data on the OUT-DATA and IOC-DATA lines into IOS.

(g) PCTR-TO-M/5: Gates the contents of the poll counter onto the S bus.

(h) P/CHECK/5: Presets the CHECK FF in the IOC when a detectable error (ad0 dress error, invalid op code, or data fault) has occurred in the Processor.

(i) P/IO-BUSY/5: Presets the IO-BUSY FF in the IOC at the initiation of a READ or WRITE instruction.

(j) P/LAST/5: Presets the LAST FF in the IOC when the ACU character count is exhausted or when a Read, non-fill is terminated.

(k) P/LD-REQ/5: Presets the LDRQ FF in the IOC when the ACU initiates a Load (READ CONTROL) operation.

b. IOC SIGNALS

(a) CHECK/3:	Output of the CHECK FF.
(b) INTERRUPT/3:	Output of the INTERR FF (not gated by ON-LINE), indicating to the ACU that at least one IOC is ready for a data transfer.
(c) INT-REQ/3:	Output of the INTERR FF gated by ON-LINE, indicating that the active IOC is ready for a data transfer.
(d) IO-BUSY/3:	Output of the IO-BUSY FF; indicates that the active partition is engaged in an I/O transfer operation.
(e) LOAD-REQ/3:	Output of the LDRQ FF; indicates that the next I/O operation will be a Load (Read Control).
(f) SERV-REQ/3:	Output of the SVRQ FF; indicates that one of this IOCs peripherals has a service request.

2. MDTS IOC OPERATION

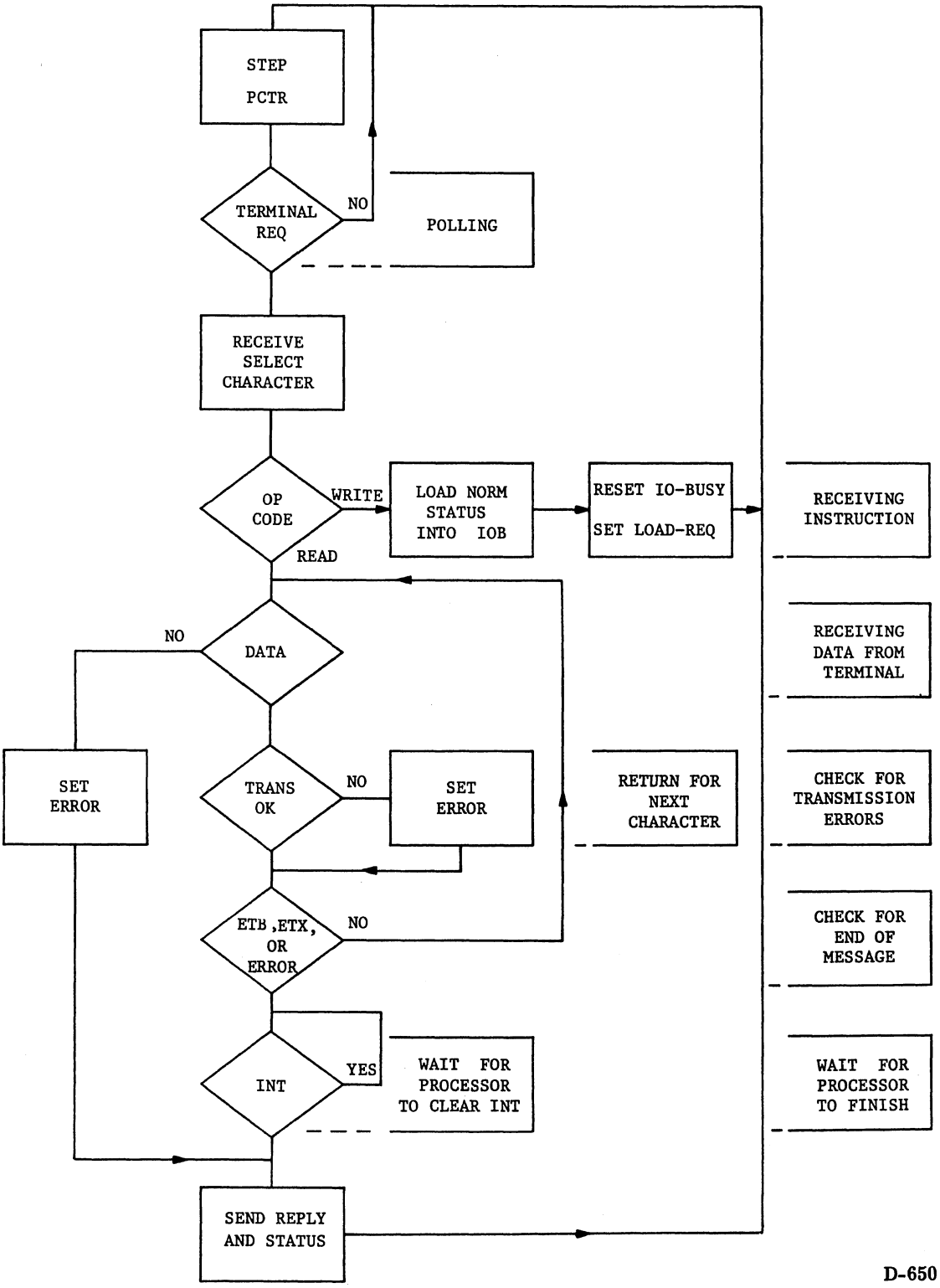
A simplified flow chart of MDTS IOC operation is shown in Figure 9-4, a more detailed flow chart is given in Figure 9-5. Normal IOC operation is interrupted if a program error is detected, and CHECK is set. If the terminal disconnects prematurely, TIMEOUT is set, and the message is reported as FAULT status. The I/O then polls the next terminal for a service request. The IOC will set CHECK, forcing the program to restart if a WRITE instruction is given at any time other than directly after the execution of a READ instruction.

The I/O program is started by the Processor recognizing a data fault, and setting LOAD-REQ. The ACU then puts a READ CONTROL select character into IOS, and sets IO-BUSY. Ordinarily a "bootstrap" instruction would be entered from the IOC, but the MDTS IOC cannot load program. Instead, the IOC loads normal status into the buffer, and resets IO-BUSY. This starts the processor's normal program routine; it goes to location zero, and carries out whatever instruction is there.

The MDTS IOC does not count states sequentially. The state counter is organized into rows and columns, and state changes to the next ascending number are coincidental.

S1 and 2 are trancient states for starting program, and when the IOC returns to S1 from an operation, CHECK and LDREQ are examined, and the IOC moves to S3.

In S3 the IOC circulates, polling each terminal for a service request. If RDATA is high when a terminal is selected, SERV-REQ is set, and the IOC steps to S0. The Poll Counter (PCTR) can only count when the IOC is in S3, and is "locked on" the requesting terminal when the state is changed.



SIMPLIFIED FLOW CHART

FIGURE 9-4

In S0 the IOC waits, with SERV-REQ set, for an instruction from the ACU (the instruction that started at location zero). The ACU parallel shifts the instruction, a select character, into IOS, and presets IO-BUSY. The IOC examines the op code (bits 5, 6, and 7) of the select character, and executes the instruction.

(1) If the instruction is a READ ($\overline{5}\cdot\overline{6}\cdot7$) the IOC waits for the ACU to go off-line, then steps to S4.
(2) If the instruction is a WRITE CONTROL ($5\cdot6\cdot7$), the IOC loads IOB with normal status and waits for the ACU to go off-line.
(3) If the instruction is a WRITE or READ CONTROL, CHECK is set and the IOC returns to S1.

When the IOC is off-line, IO-BUSY is reset (clearing FAULT and ERROR), and the state is stepped to S1. S1 is a transcient state, and the IOC will ultimately step through to S3 (polling). The poll counter is stepped one count upon entering S3.

The IOC in S4 lowers the X-DATA line acknowledging the service request, and allowing the terminal to start transmission. When the start transition occurs, the IOC clears the bit counter, the T-counter, and PARITY, and steps to S5. If the start transition does not occur within four bit times (S4 flip-flop), the IOC steps to S8, setting ERROR.

Norma-ly the IOC arrives in S5, and serially shifts the character from the terminal into IOS. The character is shifted into IOS by clocking nine times. The start bit is shifted through, and off the end of the register. PARITY is toggled once for each 1 bit. One tenth bit time later at B9 T1 the IOC steps to S6.

In S6 the IOC checks the incoming character for possible transmission errors such as:

(1) Bad parity (8 USACII bits have even parity; entire character transmission has odd-parity).
(2) Lack of a stop bit (RDATA low).
(3) INTerrupt set (the previous character has not been transferred to memory).
(4) LAST set (wrong character count for a READ instruction).

Any of the above conditions set ERROR. At B9 T2, the IOC steps to S7.

In S7 the character is parallel shifted into IOB. If the character is not an ETB or an ETX, or if ERROR is not set, the IOC sets INTerrupt, and returns to S4 for another character. However if ERROR is set, or the character is an ETB or an ETX, the IOC sets iNTerrupt and steps to S11.

To reach S11, the message is complete, or an ERROR has been made. In either case the IOC waits for the ACU to clear INTerrupt and go off line, the state counter is then stepped to S8. In S8 RDATA is monitored for one full character count (B9·T9). If RDATA is high, and no zeros occur in this time, ACTR is held clear, status is laaded into IOB, IO-BUSY is reset, and the IOC steps to S9. The status character loaded into IOB is dependent upon the state of the ERROR flip-flop.

If a zero is detected on the RDATA line during the 9 bit character count, it means that the state was forced to S8 because of an ERROR in transmission in S4, and characters are still coming. The IOC handles this situation by resetting BCTR and TCTR

each time a zero is detected. When RDATA stays high for a full character count, indicating that the message has completed, the IOC loads status (in this case ERROR) resets IO-BUSY and steps to S9.

Normally the IOC reaches S9, and waits for the ACU to initiate a reply to the terminal. The reply, a WRITE, or WRITE CONTROL, is recognized when the ACU presents the select character, setting IO BUSY. ERROR and FAULT are cleared when the P/IO BUSY signal is received. The device number (LA) of the select character is examined. IF it is odd (has a bit in the lowest position), the WLA flip-flop is set. The WLA flip-flop allows another reply message after this one is completed, and has no effect upon the IOC logic at this time.

If the R-DATA line drops during S9, indicating a premature terminal disconnect, TIMEOUT and FAULT are set, forcing the IOC to S3. If the instruction received in S9 is a READ or READ CONTROL, the CHECK flip-flop is set, and the IOC returns to S1 to restart the program.

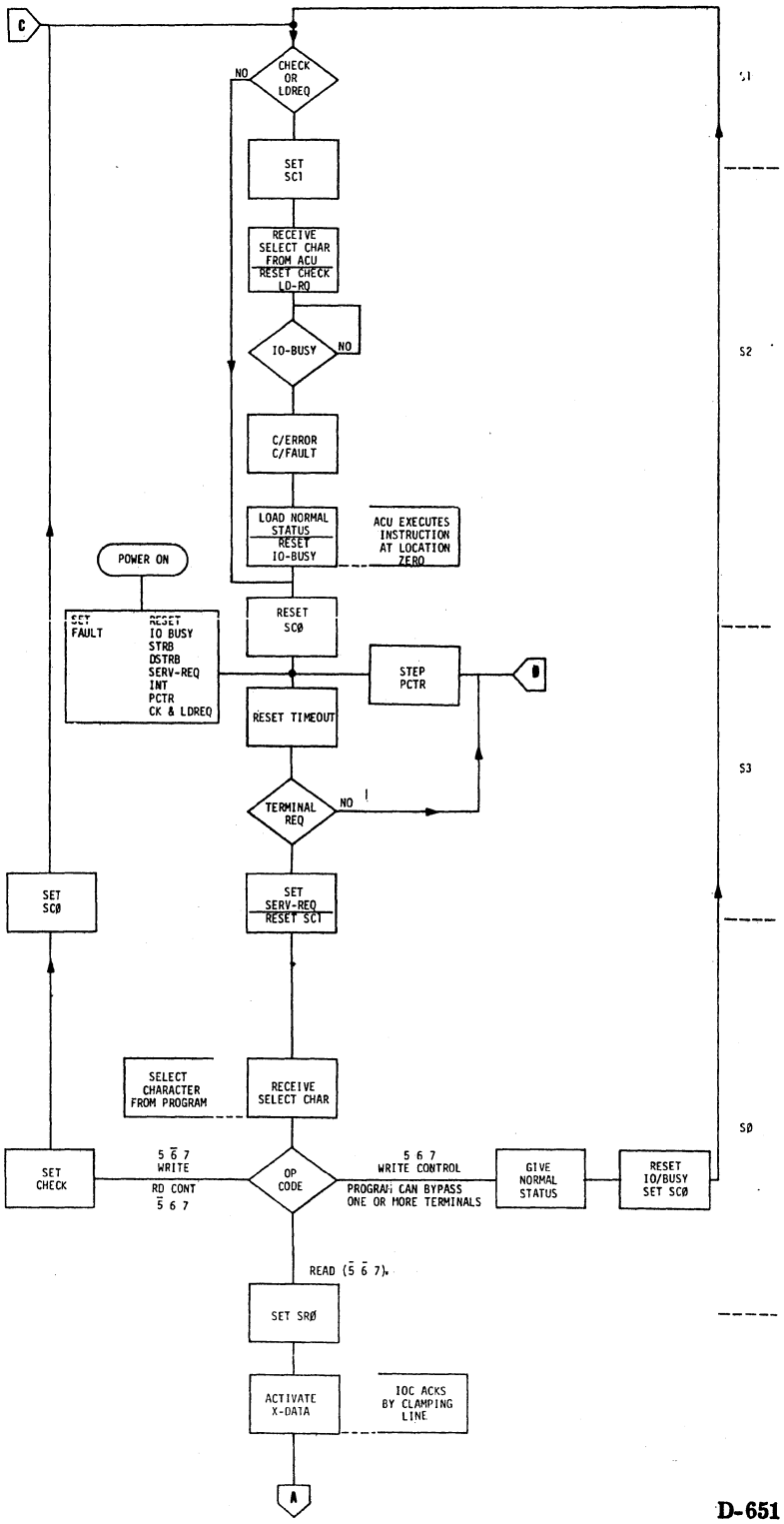
When all the above checks are made, the IOC steps to S10.

No action occurs in S10 until INTerrupt is reset by the ACU, indicating that the first character of the reply has been loaded into IOS. The BCTR and TCTR are allowed to count to B9 T9, serially shifting the character onto the X-DATA line, and to the terminal. When B9 T9 is reached, the LAST flip-flop is examined to determine if the ACU has indicated that this character is the end of this message. If LAST is not set, the IOC sets INTerrupt again, and is ready for the next character. If LAST is set, the IOC status is loaded into IOB, and IO BUSY is reset. If the WLA flip-flop is set, the IOC returns to S9 for another reply message from the ACU, otherwise, the IOC steps to S14. Fault status will be reported if the R-DATA signal is not presett in S10.

When the last reply message is complete, and the IOC has stepped to state 14, it waits for the terminal to disconnect. When the R-DATA signal dissapears, indicating that the terminal has disconnected, the IOC steps to S2, and consequently to S3, where it resumes polling. If the terminal does not disconnect within approximately 260ms, the BRK one-shot times out causing the IOC to return to S3, and the PCTR to increment one count.

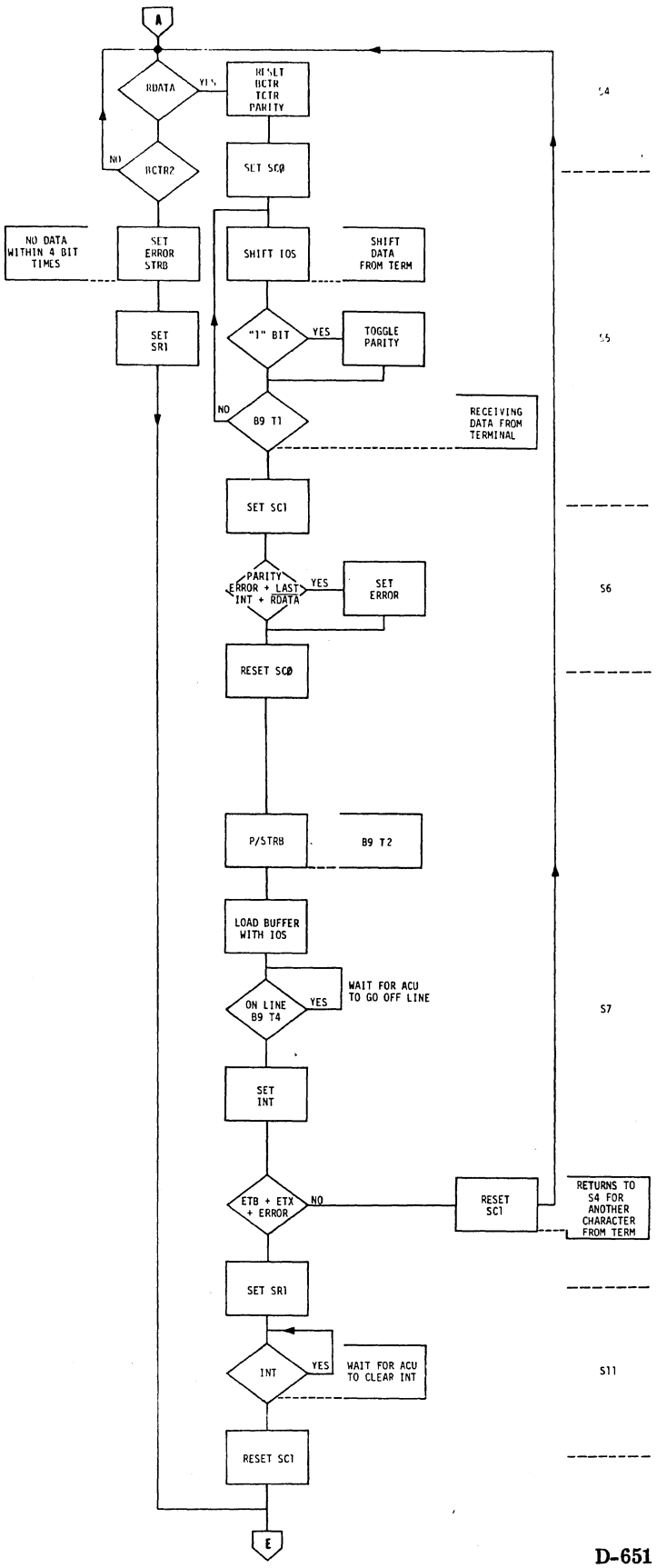
X-DATA is held active during states 4, 5, 6, 7, 8, 9, and 11. In S4 it is the acknowledgement of service request to the terminal, and must be held during the received message.

If in any state the CHECK flip-flop is set (because the ACU finds a program error) the IOC is forced to S2, and FAULT status is set. FAULT status is also set if the execution of an instruction is attempted in the wrong sequence.



MDTS IOC FLOW CHART

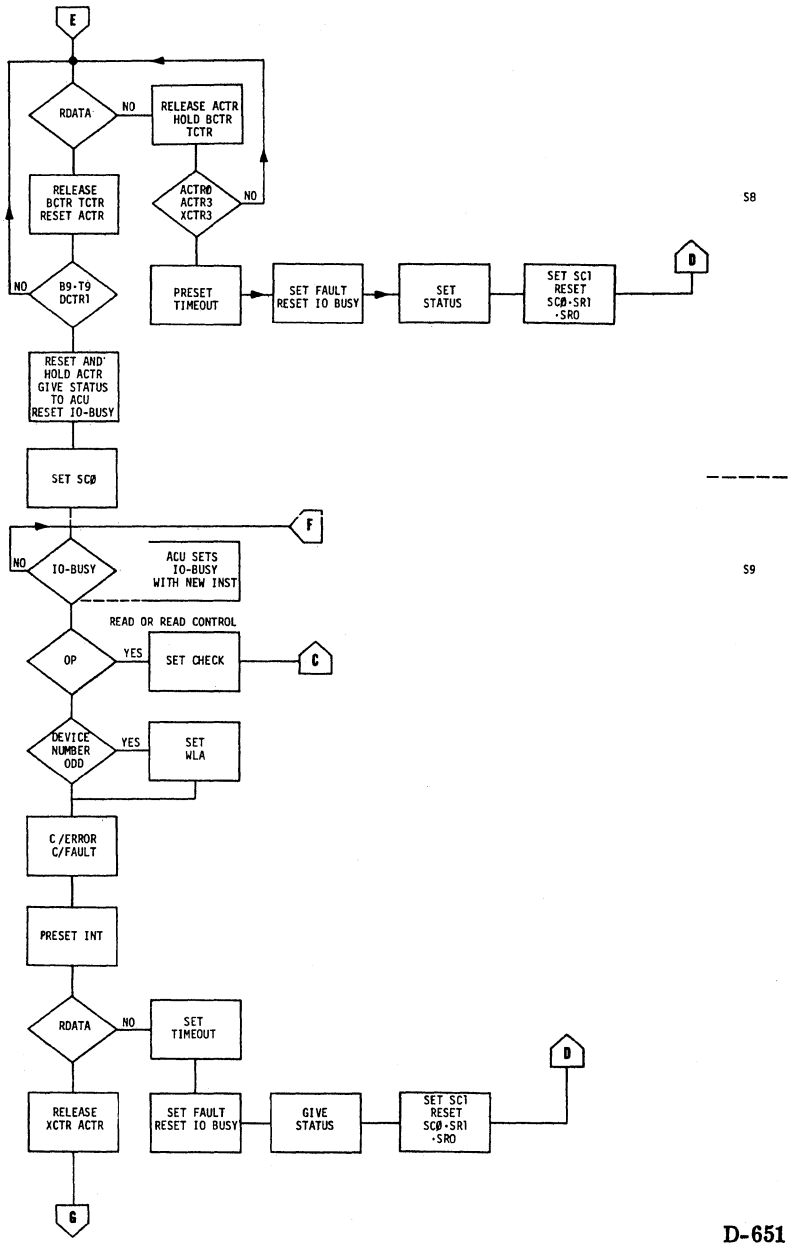
FIGURE 9-5



D-651

MDTS IOC FLOW CHART (Cont.)

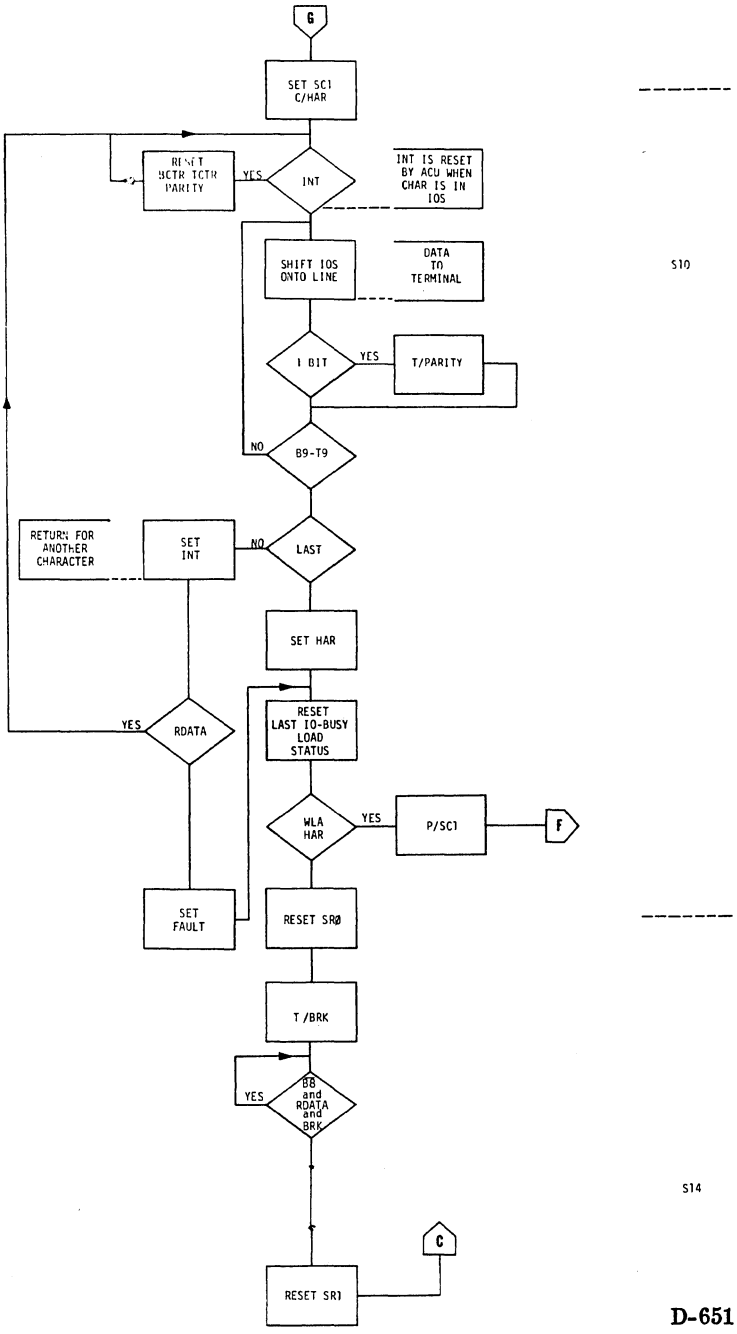
FIGURE 9-5



D-651

MDTS IOC FLOW CHART (Cont.)

FIGURE 9-5



D-651

MDTS IOC FLOW CHART (Cont.)

FIGURE 9-5

3. MANUAL CONTROLS

a. SWITCHES: Printed circuit card CH3 contains one manual switch (see Figure 9-6), the IOC-ENABLE switch. This switch allows a manual reset of the I/O channel without resetting the entire processor.

The IOC-ENABLE switch, as shown in the up (on) position, allows normal operation of the IOC. In the down (off) position the IOC is reset, clearing all flip-flops.

b. SWITCH OPERATION: Momentarily place the IOC-ENABLE switch in the down (off) position to initialize the IOC.

c. PARTITION SIZE: The partition size of the MDTS IOC is regulated by wire jumpers at the front edge of printed circuit card CH4. Jumpers in the proper hole pairs select the partition size in 1K (BCD) steps to a maximum of 10K. Figure 9-6 shows the jumper block on printed circuit card CH4.

CAUTION - Parition sizes must be considered carefully, or program problems may occur from conflicting partition limits.

C. MDTS IOC COMMUNICATION

1. INTRODUCTION

Each terminal has a separate two wire transmission line pair, connected to the MDTS IOC. Voltage isolation is provided within the transmit/receive logic circuits in the IOC (on card CH4). The IOC completes an entire message transaction. When it is not occupied in data transfer, the IOC circulates through a polling routine, looking for a service request from any of the connected terminals.

2. MESSAGE FORMAT

Messages from the terminal are grouped by transaction and daily closing (or other convenient interval). Transaction groups are preceeded by the USASCII STX code, and ended with an ETB (end transmit block). Closing data is also preceeded by the STX code, but ended with an ETX code. Figure 9-7 shows a typical message series.

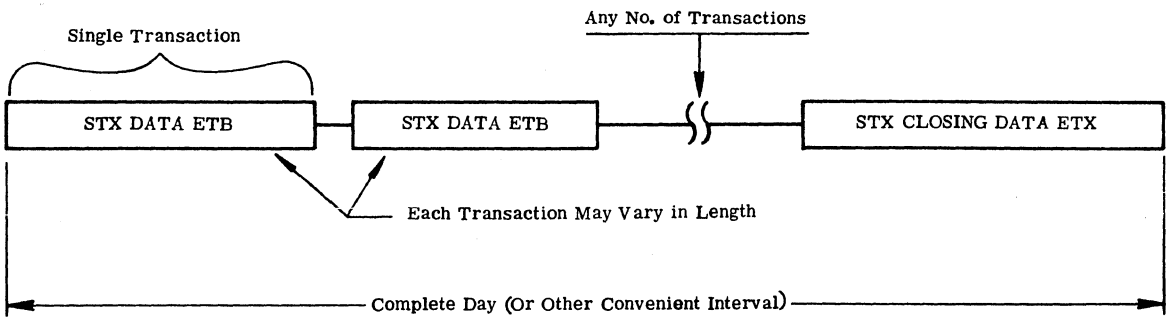
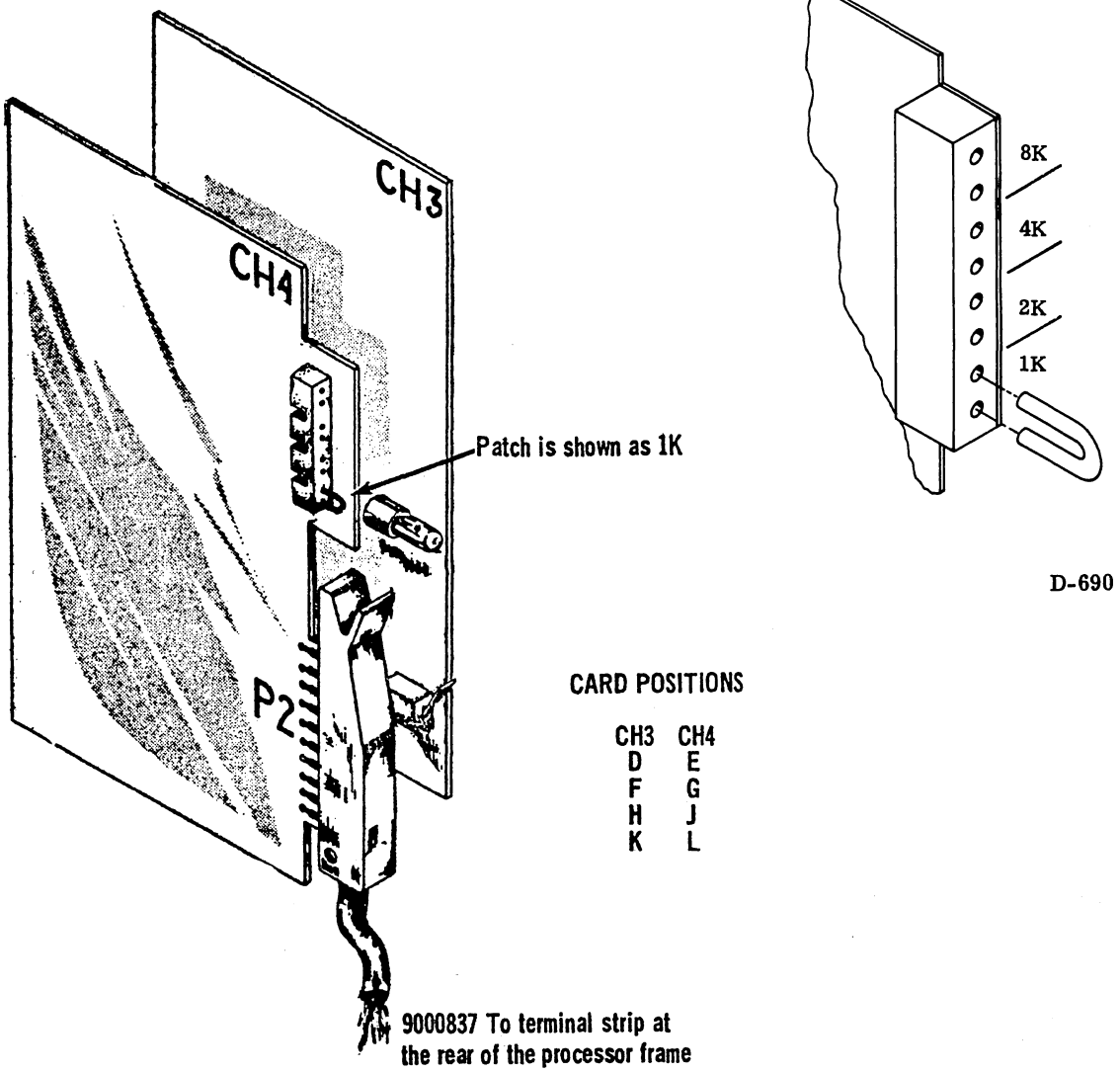


FIGURE 9-7



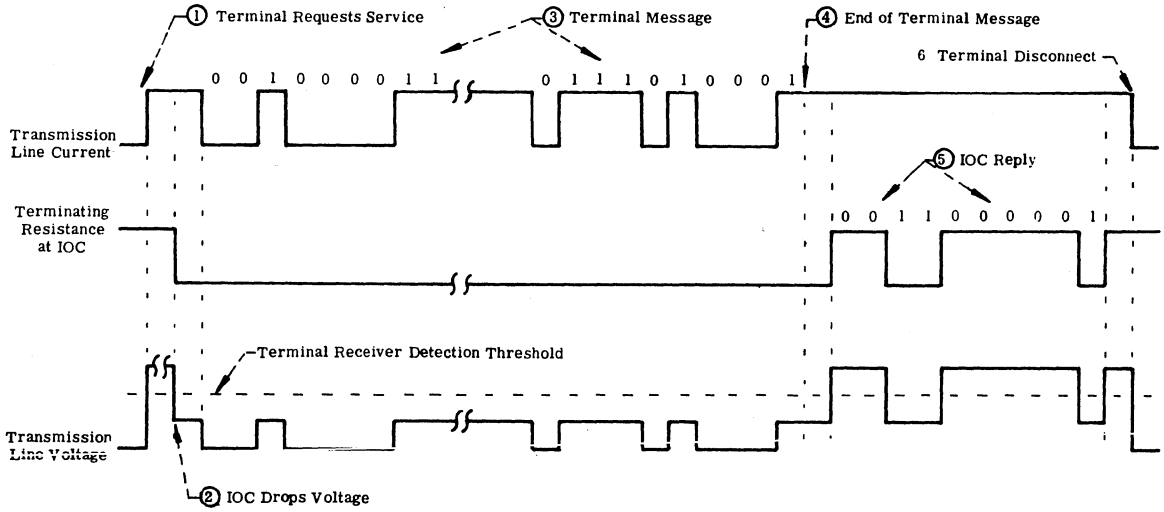
MANUAL CONTROLS

D-802

FIGURE 9-6

3. CHARACTER TRANSMISSION

USASCII character bits are transmitted serially, least significant bit first, at a 1200 bit/second rate from the terminal to the IOC, and at a 120 bit/second rate from the IOC to the terminal. Each terminal independently initiates the data transfer by raising the voltage on the two-wire data line from a quiescent zero volts to approximately 15 volts. Figure 9-8 shows a typical message transaction between a terminal and the IOC.



SIGNAL FORMAT

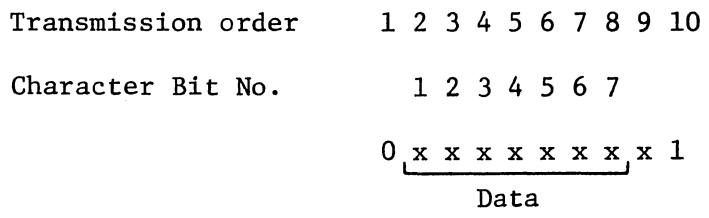
FIGURE 9-8

The IOC, in its polling sequence in state 3, finds the voltage high, and by logic, enables the receiving channel. This changes the line impedance, dropping the line voltage to approx. 5 volts ②. The terminal recognizes the drop in voltage as an acknowledgement from the IOC. If the acknowledgement does not come, the terminal will time out, and try again.

When the acknowledgement occurs (the transmission line voltage drops to approximately 5 volts) the terminal starts transmitting data bits ③ . The terminal drops the line voltage to zero for a binary 0, and returns the line to approximately 5 volts for a binary 1. When the terminal message is complete ④ , the IOC replies ⑤ by fluctuating the transmission line voltage between the 5 volt level (a binary 0 from the IOC) and the 15 volt level (a binary 1). Notice in Figure 9-8 that the initiating pulse may vary in length, according to the response of the IOC. For practical purposes, the initial 15 volt signal from the terminal can be considered a request for service, and the drop to 5 volts can be considered an acknowledgement that the IOC is ready to accept data. Therefore, if the IOC is already busy with another data exchange, the 15 volt signal will remain unanswered until the IOC is free, and selected by the ACU. A timeout starts in the terminal upon request for service, but is of ample length (11 seconds) to allow even lengthy transactions to complete before timing out.

4. DATA TRANSFER

Each character contains 7 USASCII bits, a parity bit, one start and one stop bit. Timing is syncronized by the start and stop bits that begin and end each character. Parity is transmitted and checked in each character, but cannot be reported until the message is complete. However upon detection of bad parity (or other transmission problems) the IOC sets ERROR, and does not transfer the remainder of the message to the Processor. When the terminal message is complete the IOC can then reply with status. The character bit sequence is shown, in the order of transmission, in Figure 9-9.



TRANSMISSION CHARACTER

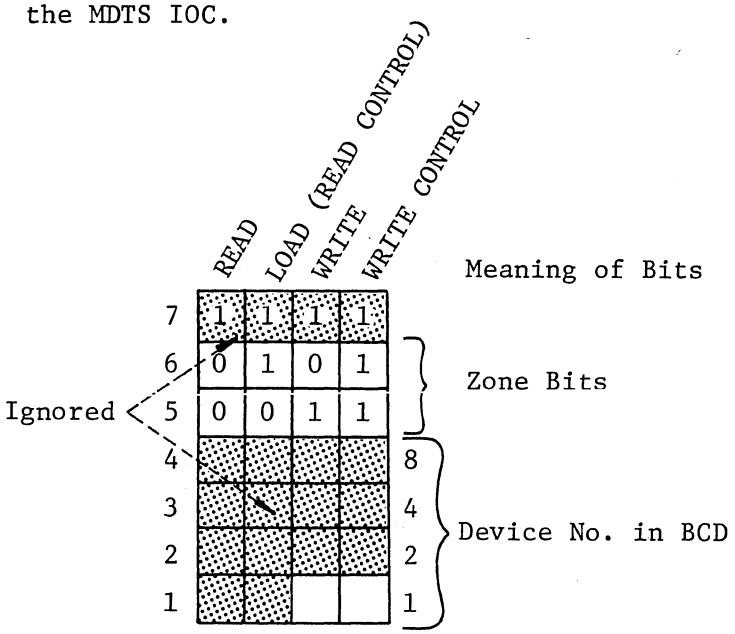
FIGURE 9-9

Notice in Figure 9-9 that:

(1) The start bit of each character is always a zero.
(2) The stop bit is always a 1.
(3) Data information uses the seven USASCII bits and one parity bit.
(4) Normally the six bit is the inverted seven bit, except for CONTROL operations.

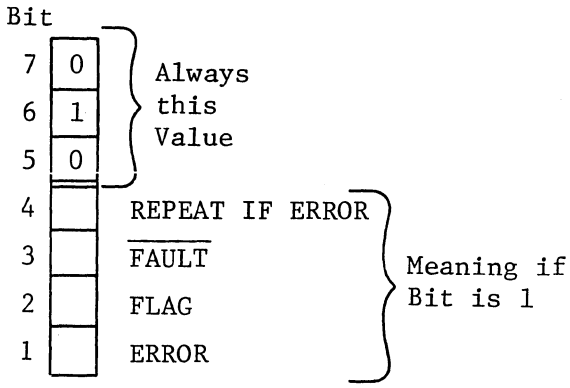
5. SELECT CHARACTER

When the MDTS IOC sets SERVice-REQuest, or LOAD-REQuest, the processor replies with an instruction, in the form of a Select Character. The MDTS IOC uses the 5, and 6 bits to determine which instruction is required. The lowest bits of the Select Character are used by the MDTS IOC to chain replies to the terminal under succeeding WRITE or WRITE CONTROL instructions. Any even number is the last reply; any odd number requires another reply message to the terminal before disconnecting. Figure 9-10 shows the possible variations in instructions within the Select Character as used by the MDTS IOC.



SELECT CHARACTER

FIGURE 9-10



I/O STATUS CHARACTER

FIGURE 9-11

6. STATUS

a. ERROR status (see Figure 9-11) is given whenever one of the following conditions o occur.

(1) Bad parity.
(2) Lack of a stop bit in the character.
(3) If for some reason a character is received before the previous character is transferred into main memory (in the processor).
(4) If the number of data characters exceeds the number given in the READ instruction.

b. FAULT, is set by any of the following conditions:

(1) The processor finds a program error.
(2) The terminal disconnects prematurely.
(3) A WRITE or WRITE CONTROL instruction is given at any time other than directly following the execution of a READ instruction (unless WLA is set).
(4) Power interruption (SYS-RES).

7. POLLING

The MDTS polling operation occurs in state 3, when the IOC is not occupied with a data transaction. The Poll Counter (PCTR) consecutively increments, when toggled by a timing signal from the D-counter (or by BRK if it times out in S14). The Poll Counter output supplies the input to a decoder, and is also gated onto the INP-DATA lines. The decoded poll count is inverted and gated with the output of the corresponding receiving circuit. If the selected terminal is not requesting service (no voltage on the SIG-HIGH line) the RDATA line is forced to a logic zero. However if a terminal is requesting service when it is selected, the RDATA line stays high, causing the IOC logic to set SERV-REQ.

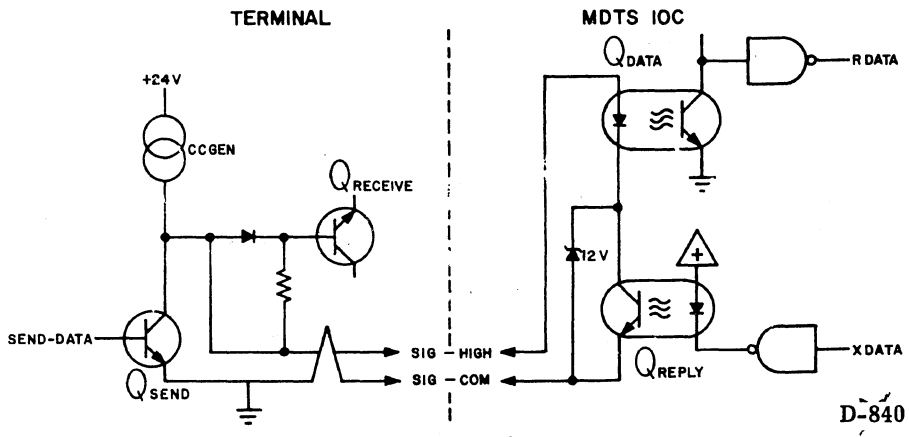
8. TRANSMIT/RECEIVE LOGIC

figure 9-12 is a simplified illustration of the transmit/receive link between each terminal and the IOC, and illustrates the explanation below. The terms Q Reply, Q Send, etc., do not appear in the Schematic diagrams, but are shown as descriptive aids for this explanation.

The terminal initiates transmission by raising SEND-DATA to a logic 1. Qsend (in Figure 9-12) is biased to apply approximately 15 volts to the transmission line. At the IOC end, the light emitting diode, which is a part of Qdata, generates light, causing the photo transistor to conduct, raising the inverted signal, R-DATA, to a logic 1. Qreceive in the terminal senses the 15 volt level on the line, but does not act at this time.

The IOC sets SERV-REQuest, and when the ACU returns with a READ instruction the IOC raises X-DATA to a logic 1. X-DATA causes Qreply to bypass the 12v Zener diode that has been limiting the transmission line voltage. The drop in transmission voltage places Qreceive (in the terminal) below detection threshold, informing the terminal that the IOC has responded to the request. IOC X-DATA is held high by logic until the terminal message is completed.

When the terminal message is complete, the line is left high, allowing the IOC to reply. The IOC transmits to the terminal by removing the X-DATA signal (for a 1 bit) allowing the line voltage to rise above the detection threshold level of Qreceive (in the terminal), and returning again for a zero bit. When the IOC message is complete, X-DATA is removed, and soon after, the terminal disconnects, returning the line to zero.



SIMPLIFIED TRANSMIT/RECEIVE LINK

FIGURE 9-12

a. PHOTO COUPLING

Problems from possible voltage differences between any of the terminals and the ACU are avoided by electrically isolating the data transmission line. Photo coupling devices are used for isolation in the MDTS I/O. These photo couplers are an integral encapsulated unit, and are not repairable. The internal circuit compares to a photo conductor and a light source. In this particular case, the photo conductor is an NPN surface, where light photons replace the normal transistor base current, to stimulate the movement of "holes" across the junction. The internal light source is an electrically separate diode structure that emits coherent light when current is passed through the doped PN junction.

The most useful feature of optical coupling is the complete voltage isolation between the input and output. For service considerations the photo-transistor has parameters similar to that of a conventional NPN transistor.

9. PARITY

The parity flip-flop is toggled once for each 1 bit received or transmitted. In state 6, the flip-flop is examined, and if parity is bad the ERROR flip-flop is set. Parity for the USASCII 8 bit code is even. But because the transmission contains a stop bit, parity for the entire ten bit transmission is odd.

10. STATE COUNTER

Four D flip-flops (SR0, SR1, SC0, and SC1) comprise the state counter. States are more related to events than to timing. Most transition of states require only one flip-flop to set or reset. A logic truth table is shown for the state counter in Table 9-1. Table 9-2 shows a matrix relationship of the SC (state column) and SR (state row) flip-flops to the IOC states and actions.

MDTS STATE COUNTER TRUTH TABLE

TABLE 9-1

STATE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
SR0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
SR1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
SC0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
SC1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1

NOTE: States 12, 13, and 15 are not used.

STATE COUNTER MATRIX

TABLE 9-2

	SC=0	SC=1	SC=2	SC=3
SR=0	S0 WAIT FOR INSTRUCTION	S1 TRANSIENT	S2 RECOVER	S3 SCAN TERMINALS
SR=1	S4 WAIT FOR START TRANSITION	S5 SHIFT CHARACTER	S6 TEST CHARACTER	S7 LOAD IOB
SR=2	S8 WAIT FOR END OF TRANSMISSION	S9 WAIT FOR WRITE INSTRUCTION	S10 TRANSMIT REPLY	S11 WAIT FOR IOB EMPTY
SR=3	S12 NOT USED	S13 NOT USED	S14 WAIT FOR DISCONNECT	S15 NOT USED

STATE CHANGES

FROM	TO	ARE CAUSED BY
SØ	S4	READ
SØ	S1,S2	$\overline{\text{WRITE}}$
S2	S3	$\overline{\text{CHECK}}$ or $\overline{\text{LDREQ}}$
S3	SØ	RDATA
S4	S8	$\overline{\text{S4FF}}$
S4	S5	$\overline{\text{RDATA}}$
S5	S6	B9T1
S6	S7	$\overline{\text{B9T2}}$
S7	S4	$\overline{\text{ETB/ETX}}$ or $\overline{\text{ERROR}}$
S7	S11	$\overline{\text{ETB}}$/ETX or ERROR
S11	S8	$\overline{\text{INT}}$
S8	S3	B4TØ and $\overline{\text{RDATA}}$
S8	S9	$\overline{\text{B9T9}}$
S9	S3	$\overline{\text{RDATA}}$
S9	S10	IO BUSY
S10	S9	DEVICE # ODD ($\overline{\text{WLA}}$) and LAST
S10	S14	$\overline{\text{DEVICE}}$ # EVEN ($\overline{\text{WLA}}$) and LAST or FAULT
S14	S2	$\overline{\text{RDATA}}$

11. TIMING

MDTS I/O Channel timing is provided, for the major part, by five counters and two flip-flops, DCTR, XCTR, TCTR, ACTR, BCTR, STRB, and DSTRB. All of the counter IC chips are identical, but the two DCTR chips are wired to count differently. Figure 9-13 shows the timing signals, and their relationship to other IO operations.

The D-Counter (DCTR) is connected as two divide by five counters. The input to the DCTR is the 300 KHz medium frequency clock signal from the ACU. Five timing frequencies are used from the DCTR, the slowest of which is 12 KHz.

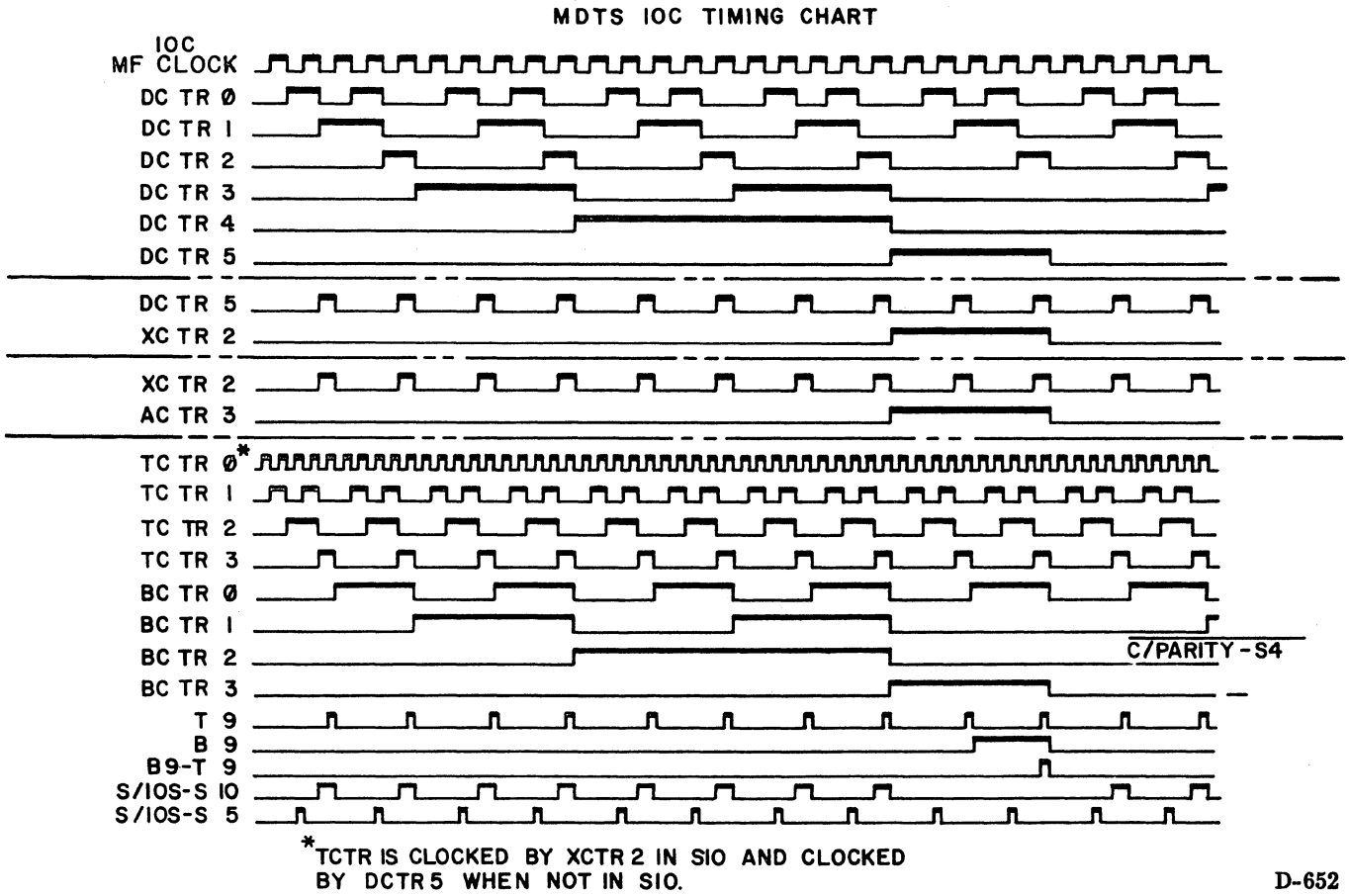
The X-Counter (XCTR) input is the 12 KHz output of the DCTR. The XCTR is connected as a divide by ten counter producing a 1.2 KHz output.

The A-Counter (ACTR) is also a divide by ten counter, used to detect a terminal timout during IOC transmission; sets TIMEOUT.

The T-Counter (TCTR) drives the Bit Counter (BCTR) with its divide by ten output. Other outputs from the TCTR give decimal fractions of a bit time. TCTR input is the 12 KHz output of the DCTR when transmission is from terminal to IOC, or the 1.2 KHz output of the XCTR when transmission is from IOC to terminal (in S10). Signals from the TCTR shift the IOS shift register, toggle the parity checker, and control transitions between states.

The Bit Counter (BCTR) is driven by the TCTR and divides by ten to provide bit times and timing signals.

Strobe (STRB) and delayed strobe (DSTRB) are D flip-flops that provide timing signals for state transitions and other control functions. STRB and DSTRB are set simultaneously shortly after the IOC is ON-LINE to the ACU. STRB is reset by timing after a fixed interval, but DSTRB is only reset when the IOC is not ON-LINE.



MDTS IOC TIMING

FIGURE 9-13

12. LOGIC FUNCTION LOCATION

The MDTS IOC logic is contained in two printed circuit cards, CH3 and CH4. The major flip-flops, counters, and registers are defined in the table below.

LOGIC FUNCTION LOCATIONS

TABLE 9-3

LOC	LOGIC	USED FOR
CH3	BRK	Time out to allow escape from defective terminal (in S14).
	SRO FF	
	SR1 FF	State Counter
	SCO FF	
	SC1 FF	
	State Decoder	Decodes 8 of the 13 used states that are used.
	S4 FF	Used with other timing to qualify that terminal transmission has started within 4 bit times in state 4.
	ARM-INT FF	One qualification for setting INTerrupt.
	DCTR	General Timing.
	XCTR	
	ACTR	Detects premature terminal disconnect.
	TCTR	Bit timer and other general timing.
	BCTR	
	*IO-BUSY	Set by processor when entering characters.
	*INT	Tells processor that IOC is ready for character.
	*LAST	Set by processor when last (final) character in count arrives.
	*SERV-REQ	Tells processor the IOC has a service request.
	*CHECK	Set by processor if error in program.
	IOC-ENABLE sw	Allows IO reset without resetting entire ACU.
	FAULT-RECEIV-ING FAULT	
	*LOAD-REQ	Preset by ACU for program restart.
	TIMEOUT	Detects premature terminal disconnect.
CH4	IOS	Shift register.
	IOB	Buffer.
	PCTR	Poll Counter - increments only one count at a time.
	ERROR	Remembers error and determines status.
	PARITY	Checks/creates parity of transferred characters.
	STRB	Strobe and Delayed Strobe are set simultaneously, STRB is
	DSTRB	reset by timing, but DSTRB is not reset until the IOC is off line.
	OUT-SEQ	Toggles FAULT if characters are loaded in the wrong sequence.
	HAR	Set by LAST, on completion of find reply to terminal.
	WLA	Set by odd device number in select character of reply (WRITE) to terminal; indicates another reply must follow before disconnect.

*Interfaces with processor.

13. CARD POSITIONS

IOC cards may be placed in any of the card positions listed below. However, these same card positions may also contain other devices or input/output variations.

CARD POSITIONS

TABLE 9-4

		CH3	CH4	Partition
*ACU MODULE		1E	1F	0
EXPANSION MODULE NO.	1	3D 3F 3H 3K	3E 3G 3J 3L	1 2 3 4
	2	5D 5F 5H 5K	5E 5G 5J 5L	5 6 7 8
	3	7D 7F 7H 7K	7E 7G 7J 7L	9 10 11 12
	4	6D 6F 6H 6K	6E 6G 6J 6L	13 14 15 16
	5	8D 8F 8H	8E 8G 8J	17 18 19

*While it is possible for the MDTS IOC to operate in the ACU module, it is not a normal system configuration.

D. SIGNAL AND TERM GLOSSARY

ACTR	A-counter; senses terminal timeout; sets TIMEOUT.
ACU	Arithmetic Control Unit.
ARM-INT	Cross latch for qualifying interrupt.
BCTR	Bit Counter; a timing signal.
B9·T1	Bit 9 and time 1.
BRK	One shot fired upon entry to S14 times out in 260ms, or 3 character times.
CHECK	Processor interface; indicates program error.
D/CHECK	Qualification to set CHECK; caused by out of sequence (OUT-SEQ) instructions.
DSTRB	Delayed Strobe; state/timing control - associated with on-line.
ERROR	Indicates trouble in character transmission. Reset by next IO BUSY pulse.
ETB/ETX	End of message or end of block of messages; signal is generated when ETB or ETX is in IOB.
FAULT	Preset by SYS-RES (pwr. fail); set by TIMEOUT, and reset by next IO-BUSY pulse.
HAR	Flip-flop, set upon completion of reply message (by LAST).
IO-BUSY	The active partition is engaged in IO transfer.
IOC	Input/Output channel (or controller).
IOC-MF-CLOCK	Medium frequency clock signal (300 KHz) from processor.
INH-TO/3	Inhibit timeout signal to ACU; qualified when IOC is online (selected) but IO BUSY is not set.
INP-DATA	Data interface with processor.
IOS	IOC shift register.
IOS-TO-MN	Gates IOS contents onto S bus in processor.
INT	Interrupt; tells processor that the IOC has a character to transfer to memory.
LAST	Indicates last (final) character of count; preset by ACU.

LOAD-REQ	Starts program; if set during instruction, causes a jump to S1.
M/IOS	Changes IOS from parallel to serial operation.
MDTS	Modular data transaction system.
ON-LINE	The IOC is selected and active.
OP	Operation code; 5, 6, and 7 bits of select character.
OUT-SEQ	Set if IOS is loaded in the wrong sequence.
PARITY	Signal from parity flip-flop; sets ERROR.
PCTR	Poll Counter.
PCTR-TO-M	BCD output of poll counter to processor.
P-LIM	Parition limit (size).
PRIV-CHAN	Active IOC can enter Privileged memory section.
RDATA	Received data; high for a 1 bit.
S1, S2, etc.	Decoded states of the IOC state counter.
SC0 SC1	State counter flip-flops (two of four)
SIG-HIGH SIG-COM	Two wire pair for data transmission to and from the terminal.
SERV-REQ	Indicates the IOC has a service request.
SR0 SR1	State counter flip-flops (two of four).
STRB	State/timing control; associated with on-line.
TCTR	Time counter.
TURN-ON	Power up signal.
USASCII	United States of America Code for Information Interchange.
XCTR	Counter for general timing.
XDATA	Transmitted data logic; high for zero, low for 1 bit.

SECTION 10

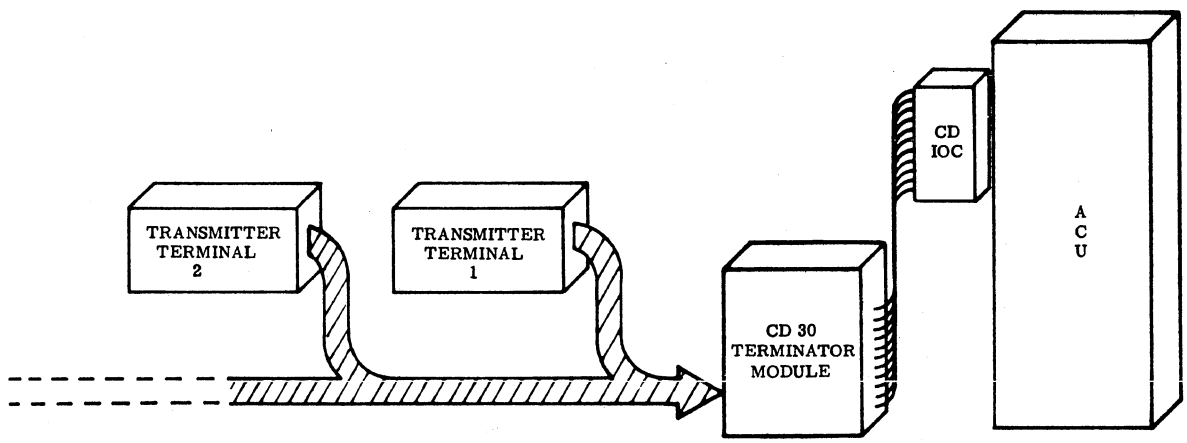
COLLECTADATA 30 IOC AND TERMINATOR

SECTION CONTENTS

SECTION 10

COLLECTADATA 30 IOC AND TERMINATOR

LIST OF ILLUSTRATIONS



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SYSTEM CONCEPT

10-1

SECTION 10, COLLECTADATA 30 IOC AND TERMINATOR

A. GENERAL DESCRIPTION

The Collectadata 30 IOC and Terminator Module functionally replace the model 3031 Collectadata receiver consol. They allow direct interface of the electromechanical-relay transmitters with the Model 20 processor. A system concept of the Collectadata 30 IOC and Terminator is shown in figure 10-1. The Collectadata IOC does not monopolize the processor, and is compatable with other time sharing partitions of System Ten (including other Collectadata 30 IO's). Incomming Collectadata information can be immediately processed and/or stored for use in any System Ten data management program.

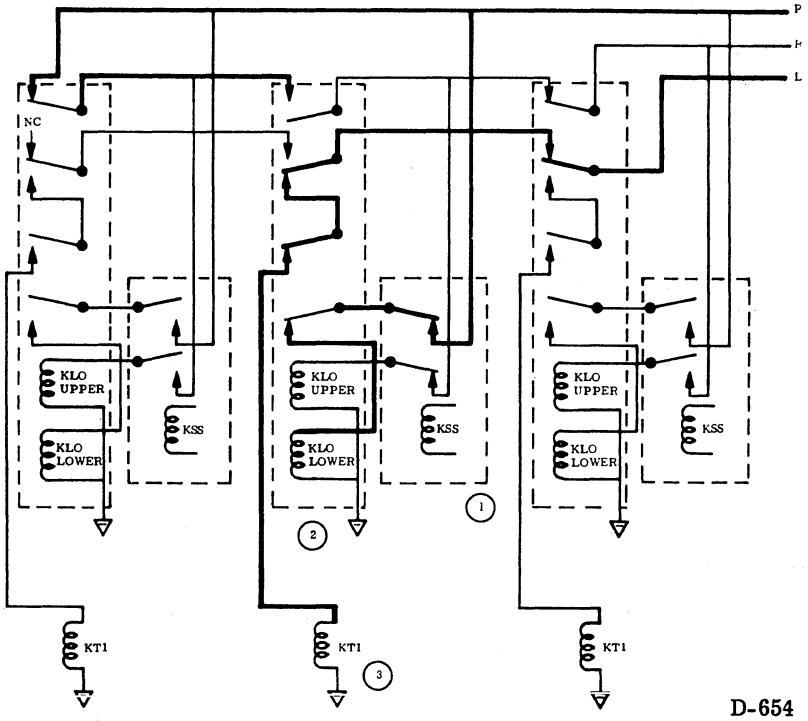
The IOC/ACU interface is similar to most other IO channels, and is described in detail in the following paragraphs. The Terminator Module converts the incomming 90 volt signals to 5 volt levels, and outgoing 5 volt signals to 90 volt levels. Each outgoing signal line has a relay that is directly associated with the control flip-flop for that line. When the flip-flop is set, the relay is closed, placing 90 volts (from an internal power supply) onto the line.

Data from the Collectadata Terminals is character coded in the Friden System Code, that is a modified BCD code. conversion to standard USACII code is accomplished by software.

All transmitter terminals can be forced to the Attendance Mode by command from the ACU. However, any single transaction can be specified as Attendance Mode by the first character of the transmission, if the transmitter Attendance Mode switch os ON, or if the Clock-in-out switch is operated.

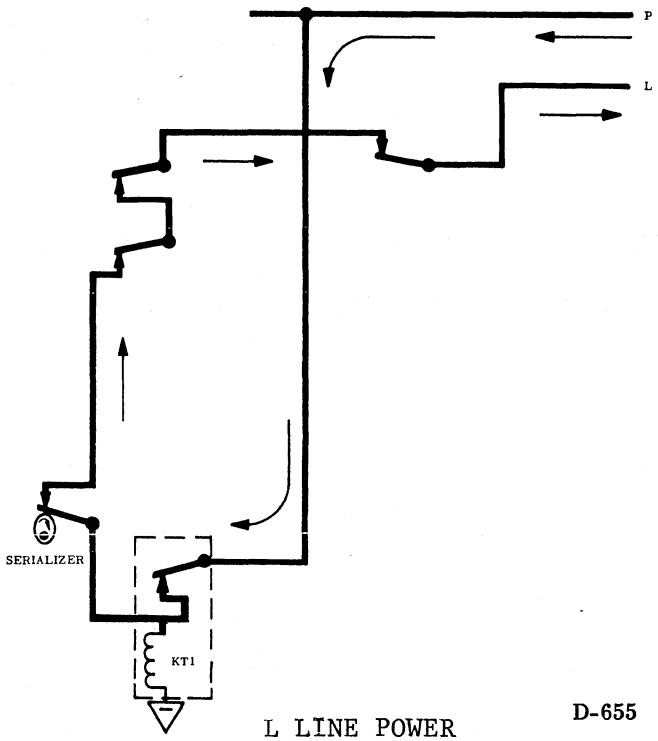
The Collectadata 30 IOC communicates with only one transmitter terminal at a time, and while priority is controlled by the IOC, the priority schedule is incorporated in the transmitters. Data characters are parallel transfered to the IOC at approximately 30 characters per second (the rate may vary slightly from one transmitter to the next).

Each incomming character is examined for odd character praity, and reported as ERROR status if bad. A reply is returned to the transmitter (except in the Attendance Mode) that releases the transmitter from the line. The transmitter disconnects automatically without a reply when in the Attendance Mode.



PRIORITY SCHEME

FIGURE 10-2



L LINE POWER

FIGURE 10-3

B. PRIORITY SCHEME

NOTE: The explanation given here is in no way intended to supersede the detailed information given in the Collectadata System Manual. Instead, it gives a broad guide to the basic principles involved, and the responses that are expected from certain IOC/Terminator signals.

The transmitter terminals are numbered progressively along the main cable, with the lowest number (T1) as the closest to the Terminator. In the case of simultaneous requests for the line, the lowest number gains priority. Once the first priority is set, the progression goes to the next higher number that is requesting service. Service is given to the next higher number until the highest number is reached. Priority then goes to the lowest number, and the sequence is started again. Terminals requesting service during the transmission cycle of another transmitter gain priority as if the request were simultaneous with all other waiting terminals.

To accomplish the priority scheme, the transmitter depends upon response from the Terminator (controlled by the IOC). figure 10-2 is a simplified illustration of the major elements of the transmitter priority scheme.

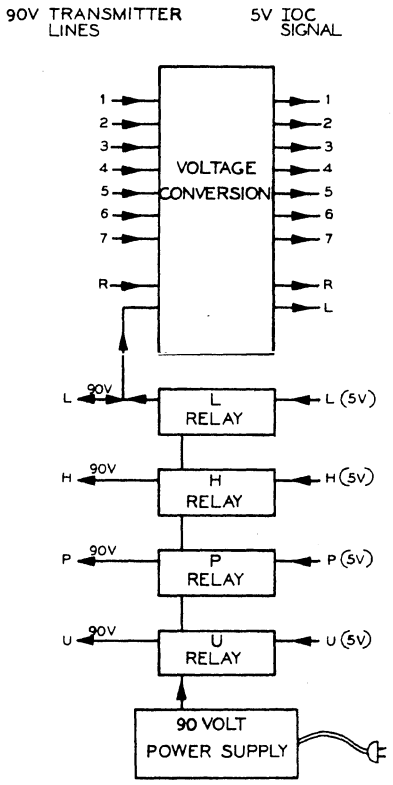
As the transmitter attempts to acquire the line, its KSS relay (1) tries to activate the KLO relay (2) . If no higher numbered transmitter has accessed the line, the KLO relay activates, opening a series circuit, and preventing other transmitters closer to the receiver (Terminator) from operating their KLO relays. The center transmitter in the illustration is shown as having acquired the line. However, notice that the initial activation circuit for KLO (shown by the dotted line) is opened by picking KLO. But another pair of KLO contacts complete a circuit to the lower coil of KLO, and the relay is held. KLO is a double coil relay. All other transmitters are now excluded from the line. The lower numbered transmitters cannot pick KLO, because of the disconnect in the R line, and the higher numbered transmitters cannot pick KT1, because of the disconnect in the L line. However the L line is not active at this time.

As an installation modification to the Collectadata cable wiring, the R line is extended to the Terminator from its junction with the nearest transmitter T line. KLO operating causes the R line to lose power, indicating to the IOC that a Service Request is in progress.

The IOC reports the Service Request to the ACU, and receives an instruction. The IOC then activates the L line. The active L line allows the transmitter to complete the priority acquisition. KT1 is picked, causing KT2 to pick, and the transmitter has sole access to the line for up to 10 seconds.

1. L LINE POWER

Shortly after the transmitter acquires the line it transmits data bits to the IOC. When the IOC begins to receive the data bits, it removes the 90 volts from the L line. However the L line does not return to zero. When KT1 was picked, one set of contacts created a return path from the P line to the L line. Now, the IOC begins to monitor the L line for the end of message drop that will appear when the message is complete or aborted. Figure 10-3 shows a portion of the previous figure (again, simplified) to illustrate the transfer of power from the P line to the L line.



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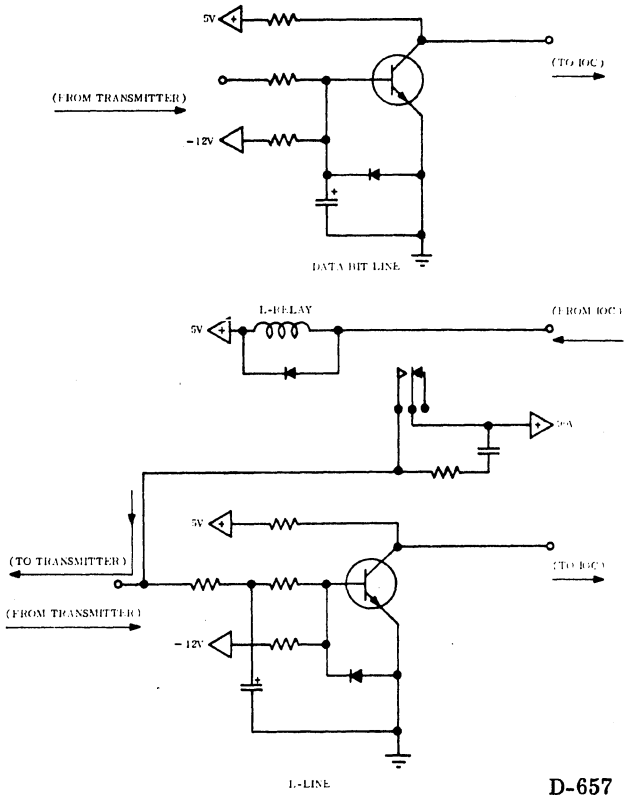

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TERMINATOR BLOCK DIAGRAM

FIGURE 10-4

TERMINATOR VOLTAGE CONVERSION CIRCUITS

FIGURE 10-5

C. TERMINATOR INTERFACE

Five control lines interface between the transmitters and the terminator module, and are controlled by flip-flops within the IOC. Setting the flip-flop cooresponding to a particular line picks a relay that places 90 volts on that line. Table 10-1 gives a brief description of the use of each line.

TABLE 10-1
CONTROL LINES

LINE	USE
R	Service Request (indicated by a negative transition)
U	Attendance Mode (High for Attendance Mode)
P	NAK (removing 90v gives negative reply to transmitter)
H	ACK (90v indicates "good bit" to transmitter)
L	Enable (90v on line allows access by transmitter)

Incomming data bits are converted to integrated circuit voltage levels (5v) by a transistor and diode combination (in the Terminator). The terminator card inverts the signal level, converting 90 volts from the line to Ø volts to the IOC, and Ø volts from the line to 5 volts to the IOC. Figure 10-4 shows a simplified block iiagram of the Terminator module. A typical transmit/receive circuit within the Terminator is shown in figure 10-5. Each terminator module card can accomodate two main cables. The Terminator module can contain as many as nine terminator cards. This means the Terminator module can supply power and voltage conversion for 18 main cables and Collectadata IOC's.

D. TERMINATOR MODULE INSTALLATION/OPERATION

Generally the Collectadata 3000 Terminator Module accepts the receiver end of the main cable directly. However certain precautions must be observed for proper operation and safety to personel and equipment.

1. INSTALLATION

Collectadata 3000 Terminator Module installation must take into account the physical location, the electrical power source, and availability to the service technician. Ample space should be allowed at the rear of the unit to allow the rear door to open fully. If this is done there will be sufficient room for card extenders etc. when servicing. Figure 10-14 shows the receiver connector pin placement, and the lines that are connected to the pins. Figure 10-15 shows the necessary changes to the power line connections, if the terminator is to use a 230 volt ac power source. The list below contains the major points that must be followed when installing a Terminator Module. Additional checks and procedures may be necessary for some installations.

a. The physical location of the Terminator Module and all Collectadata transmitters must be at least 25 feet from the main processor.

b. The ac power source to the Terminator must be a separate circuit from the power source for the Collectadata transmitters.

c. Before the main cable is connected to the Terminator, the R line circuit must be completed from junction box #1 to the receiver plug. This may involve connections at the receiver plug and the cable termination box also. (Receiver plug connections are shown in the reference pages of this section.)

d. Use the upper blade connector on the CDT printed circuit card, if only one cable is to be connected to that card.

e. Remove all power when working on the interior of the Terminator Module or the cable connections to the Terminator.

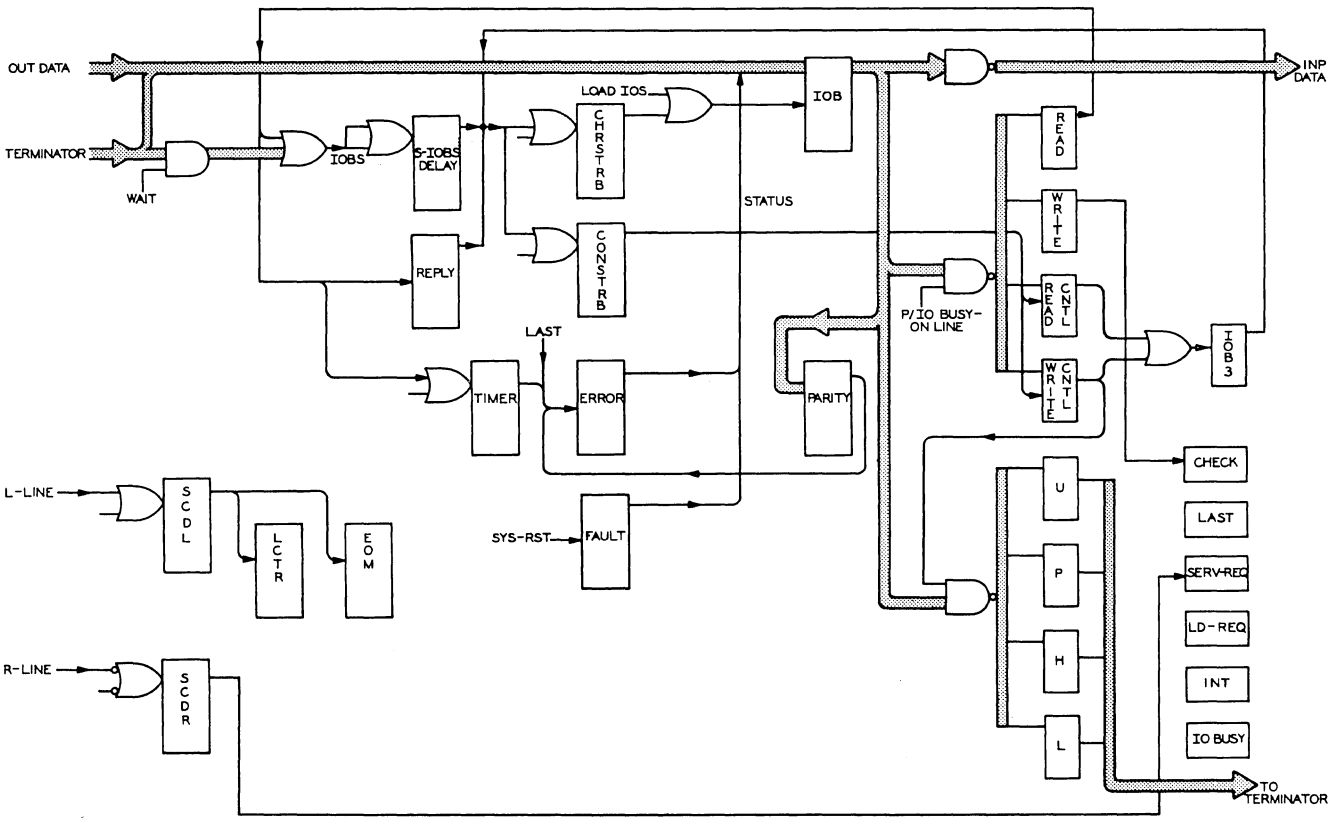
f. Use extreme CAUTION when servicing CDT printed circuit cards on a card extender, as the 90 volt power can easily be shorted to the 5 volt IOC signal lines, and possibly destroy a large portion of the main processor.

2. OPERATION

The only operator action needed is the initial power-on. However the Terminator Module must be powered-up before the processor, and powered-down after the processor.

E. IOC LOGIC

Figure 10-6 is a simplified block diagram of the major components of the Collectadata 30 IOC. Instructions from the ACU or data bits from the Transmitter (converted by the Terminator) enter a common bus to the shift and storage register, IOB. Organized data exits to the ACU through the INP-DATA bus, and terminal control line signals exit through the IOC/Terminator cable. Most of the logic functions are qualified by conditions and signals that are not shown in the illustration. These conditions are explained in later paragraphs.

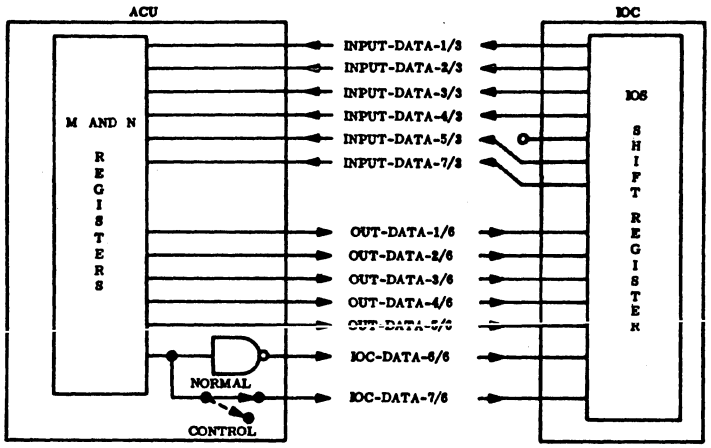


COLLECTADATA 30 BLOCK DIAGRAM

FIGURE 10-6

F. TRANSMISSION FORMAT

The Collectadata-30 uses the Friden System Code (a modified BCD code). This is essectially a seven bit, odd parity code. Parity is checked on the incomming character (from the transmitter) and the parity bit (the 5 bit) is dropped. The lower four bits are presented to the ACU unchanged, and the 6 and 7 bits become the ACU 5 and 7 bits, respectively. Figure 10-7 shows the I/O bit conversion for data characters comming from and going to the ACU. Once the Friden Code is in memory, it is converted to standard USASCII codes by software operation. Special BCD codes, and their Collectadata meanings are shown in the table below.



I/O DATA LINES

FIGURE 10-7

G. SELECTION

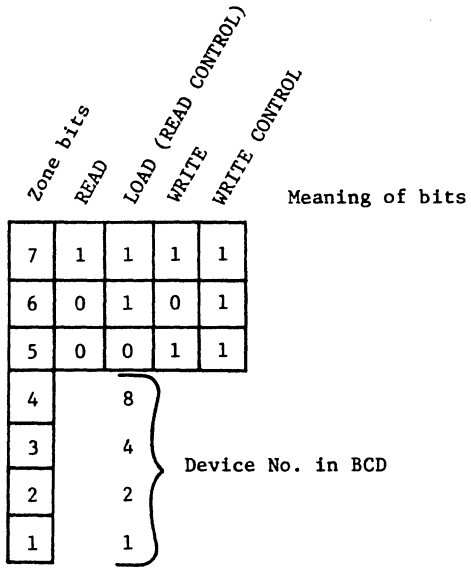
The Collectadata 30 IOC is selected by the Digit and Group lines from the processor. Instructions from the processor are carried in the Select Character (shown in figure 10-8). The actions taken by the IOC for the different instructions are listed below. The device number portion of the select character is used in the WRITE CONTROL instruction to direct a reply to the terminal, or to place all terminals in or out of Attendance Mode.

READ - (after SVRQ from terminal) normal READ (without SVRQ) causes timeout and ERROR, and re-initializes the IOC.

WRITE - Illegal instruction; sets CHECK and terminates instruction.

WRITE CONTROL - ACK or NAK reply, or Attendance Mode control.

READ CONTROL - Normal status is placed in Character Buffer, and instr. terminated by resetting IO BUSY.

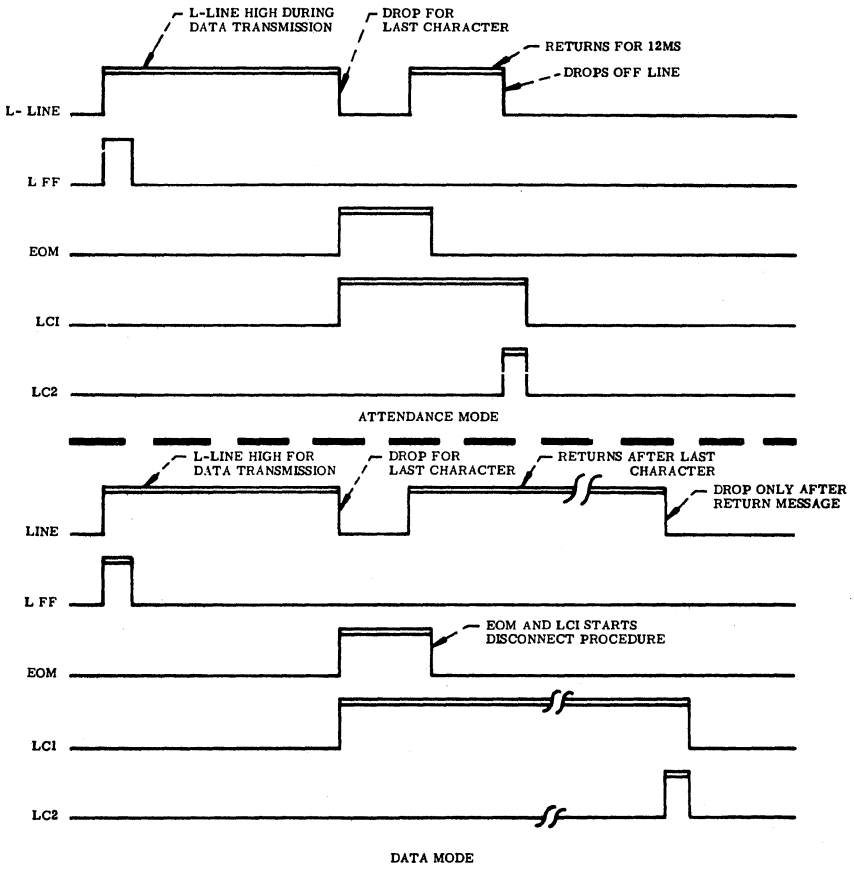


DEVICE NO.

Ø	Place in Data Mode (reset U)
1	ACK (set H)
2	NAK (reset P)
3	Place in Attendance Mode (set U)

SELECT CHARACTER

FIGURE 10-8



L-LINE AND LCTR TIMING

FIGURE 10-9

H. TIMING

Major timing for the Collectadata 30 IOC is controlled by the retriggerable monostable multivibrators, CHRSTRB, CONSTRB, TSERV, and TIMER. The LCTR (L-counter) is also a major timing element consisting of two JK flip-flops configured as a modulo-two counter.

1. LCTR

Input to the L-counter is the L line. The L line stays high during data transfer from the transmitting terminal. As the last character of the message is transmitted, the transmitter momentarily drops the L line (for approximately 12 ms), then the line goes high again. In the Attendance Mode the line will automatically drop again after about 15 ms. The IOC resets the LTCR and IO BUSY upon the second drop. In the Data Mode, the transmitter does not drop the L line voltage until after an ACK or NAK reply, so the IOC resets the LCTR and IO BUSY after the first drop in the L line. Resetting IO BUSY terminates the READ state. Figure 10-9 shows the L-line timing, both in the attendance mode, and the data mode.

2. TIMER

TIMER is a 10 second timeout that is set on entrance to a READ operation. The IOC allows 10 seconds to complete a message from a transmitting terminal. If the TIMER one-shot times out, ERROR is set, and IO BUSY is cleared. The transmitter also contains a ten second timer to drop it off line.

I. INTERFACE SIGNALS

The "digit" and "group" signals from the Processor uniquely select any particular IOC and develop the ON-LINE signal, enabling all Processor/IOC interface signals except the INTERRUPT and data lines. INTERRUPT and data lines are enabled during the working cycle of the IOC, and are used to implement data transfer to and from the Processor. A list of the IOC and ACU interface signals is included in the signal glossary.

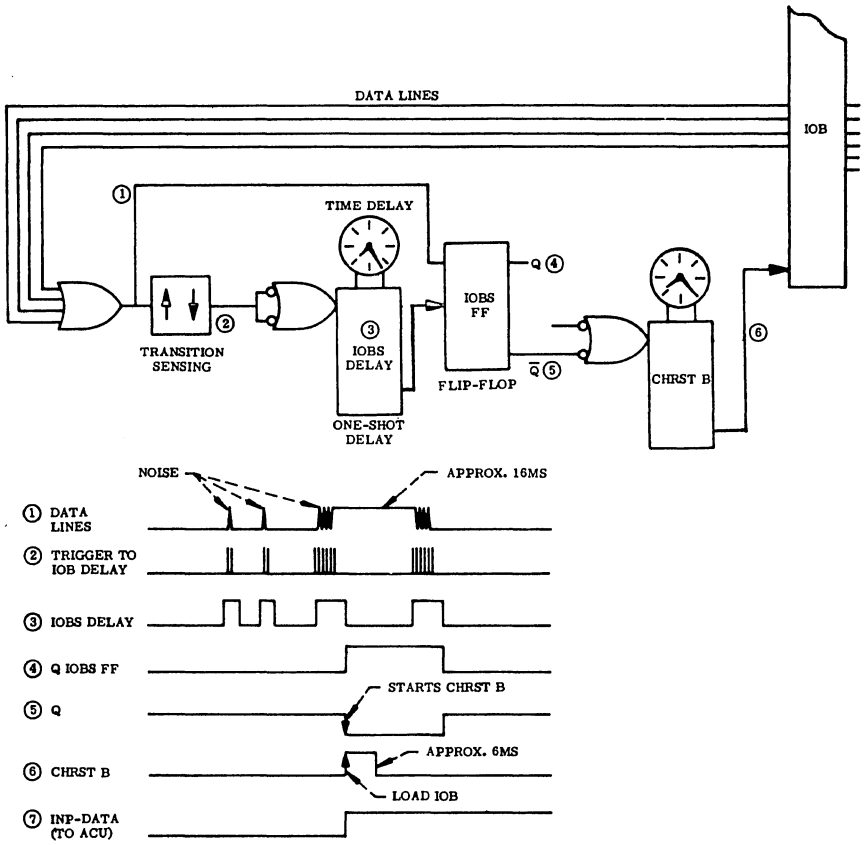
1. TERMINATOR/IOC INTERFACE

Three retriggerable monostable multivibrators (one-shots) protect the Terminator/IOC lines from false noise spikes and contact-bounce noise from the transmitters. They serve to eliminate noise transitions from the IOC lines. The lines that are protected are the L line, the R line, and the data lines. The IOBS DELAY is typical of these circuits, and is described below.

Figure 10-10 shows a simplified graphic representation of the logic action. The input to the IOBS DELAY is an OR'd signal from all of the data lines (only four are shown in the illustration for simplicity). The OR'd signal, and other qualification, is also applied to the enable input of a D flip-flop. A circuit at the input of the one-shot converts negative and positive transitions, to a trigger signal for the one-shot. When a transition appears on the line, the circuit senses either the positive or negative pulse, the one-shot triggers, and a time delay is started. If before the one-shot times out, another transition occurs, it is retriggered, and the time delay is restarted without triggering the D flip-flop. When the one-shot times out (approximately 2 ms after the last trigger) the D flip-flop is triggered, and the level that is present at the enable input is reflected at the Q output. When the Q output goes high, the $\overline{Q}$ output starts the one-shot, CHARSTRB.

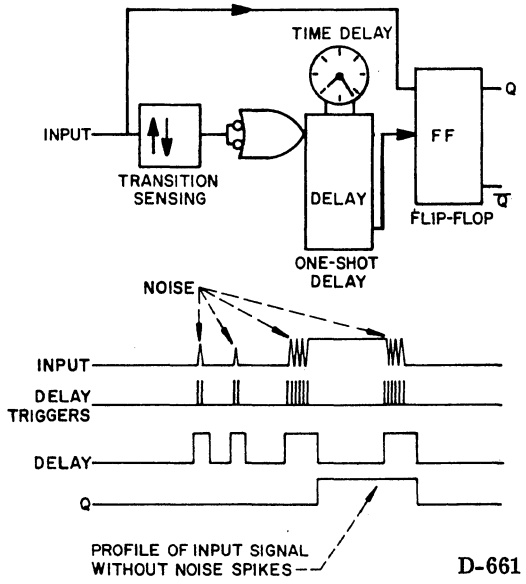
Individual noise spikes may trigger IOBS DELAY, but when it times out, the line has returned to normal. And while the D flip-flop is triggered, the enable has not changed, so the Q output does not change. As the transmitter relay contacts are closing to activate the data lines, IOBS DELAY is triggered by the first noise spike. Subsequent noise retriggers the one-shot, extending the time delay until the line is quiet. When the one-shot finally times out, the line level is reflected at the output of the D flip-flop, and the trigger input of CHRSTRB. Approximately 6 ms later CHRSTRB times out, and IOB is loaded at a time when the line is free of noise. Noise caused by the transmitter relay contacts breaking, triggers the one-shot again. But the D flip-flop does not change state until the delay is complete (approximately 2 ms after the last noise spike).

The R and L line delays (SCDR and SCDL) are similar to the IOBS delay, except that the input to each is a single line. The R and L delays do not feed a second delay strobe. Instead, the output of the D flip-flop reflects the profile of the incomming signal with the noise removed from the leading and trailing edges. Figure 10-11 shows the timing involved.



DATA LINE INTERFACE

FIGURE 10-10



CONTROL LINE INTERFACE

FIGURE 10-11

J. OPERATION

The Collectadata 30 IOC can receive three legal instructions, READ, READ CONTROL, and WRITE CONTROL. If an illegal WRITE instruction is received, CHECK is set and the IOC is re-initialized. Initially all flip-flops are cleared by direct, or indirect action of the IO-RESET signal. The ACU, upon detecting a data fault, places a READ CONTROL (LOAD) select character in the IOC character buffer (IOB), and resets LOAD-REQuest. The IOC, detects the IO-BUSY, and the READ CONTROL select character, Loads normal status and clears IO-BUSY. At this point the IOC is under program control, and will stay under program control until CHECK is set by the IOC, LOAD-REQ is set by the processor, or the IO is reset (manually or by power failure, and re-initialization). Figure 10-12 is a logic flow diagram of the Collectadata 30 IOC.

1. READ CONTROL

A READ CONTROL instruction is expected after a CHECK or LOAD-REQ. However, the IOC will accept a READ CONTROL select character from program. In any case, the operation is terminated by loading normal status into IOB, and clearing IO-BUSY.

2. WRITE CONTROL

A WRITE CONTROL instruction performs one of three actions. It can reply (ACK or NAK) to a Data Mode message, or command all terminals to enter or leave the Attendance Mode. The device number portion of the WRITE CONTROL select character (bits 1 through 4) determine which action is taken. The device numbers, and the actions to be taken, are listed below in table 10-1.

Table 10-1 Device Number Commands

Device No.	Action	Result
Ø	Reset U	All Terminals in Data Mode
1	Set H	ACK
2	Reset P	NAK
3	Set U	All Terminals in Attendance Mode

Any device number greater than three will cause CHECK to set, and the program will be restarted.

3. READ

Reading is the primary purpose of the Collectadata 30 IOC. Hoever when a READ instruction is received from program without first receiving a terminal service request, the 10 second timeout (TIMER) will start, and complete, terminating the READ op, and clearing all flip-flops.

Normally the IOC is inactive until one of the terminals requests service (by lowering the R line). The SERV-REQ flip-flop sets, and through program, the READ select character is placed in IOB. The ACU resets SERV-REQ. READ, CONSERV, L, and TIMER flip-flops are set. READ remains set during the entire READ operation. CONSERV, when set, means the operation is in the Data Mode (the first character of the message may change CONSERV). TIMER is a one-shot that allows 10 seconds on the line for each service request (normal messages will complete in much less time). The L flip-flop raises the L line, allowing the transmitter to access the line.

The IOC waits for a sign of activity on any of the data bit lines, sets CONSTRB (a noise protection delay) and resets L. The L line continues high, because the transmitter, as a part of the priority scheme, holds the L line with power from the P line. The one transmitter now has exclusive use of the IOC (for 10 seconds maximum). The first character of a Collectadata message determines the type of transaction (Data or Time and Attendance). If the binary numeric value of the first character is 13, CONSERV is reset, as the operation is to be in the Attendance Mode. The IOC waits until the transmitter is clear of the data lines (IOBS), then sets INTerrupt.

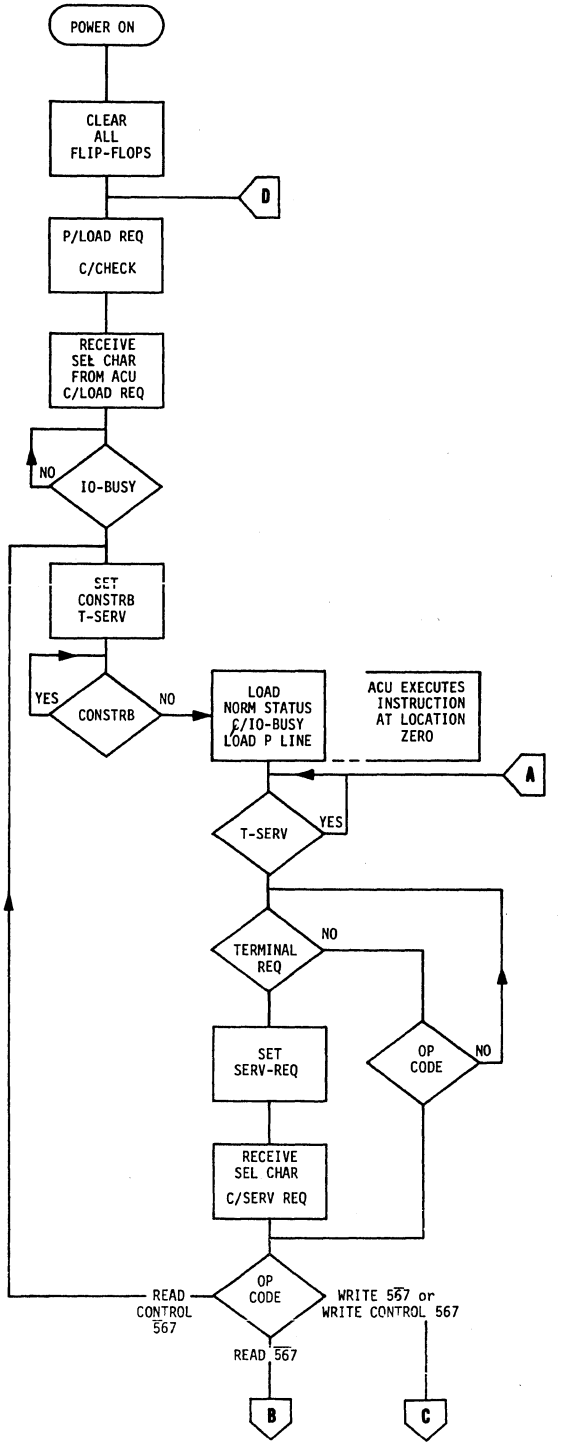
If after INT is set, another character appears on the data lines, ERROR is set, and the op is terminated. However this is a nearly impossible situation, as the processor is many times faster than the Collectadata transmitters.

Parity is checked on each incomming character (from the transmitter), and if it is bad, ERROR is set. LAST is also checked (LAST is set by the processor) and if it is found set, the op is terminated in ERROR status. If all these things are good, and the EOM flip-flop is not set, the IOC returns for another character.

During transmission of the last character of a message, the transmitter momentarily drops the L line (for approximately 12 ms), setting the EOM flip-flop. The drop in the L line also clocks the LCTR (L counter). If the transaction was in the Attendance Mode, the transmitter will drop off the line automatically, clocking the LCTR again. When CONSERV is not set, the second L count terminates the op. With CONSERV set (Data Mode transaction) the IOC must initiate the op termination, and does so after the first L count. CONSTRB is set, and when it times out, the op is terminated.

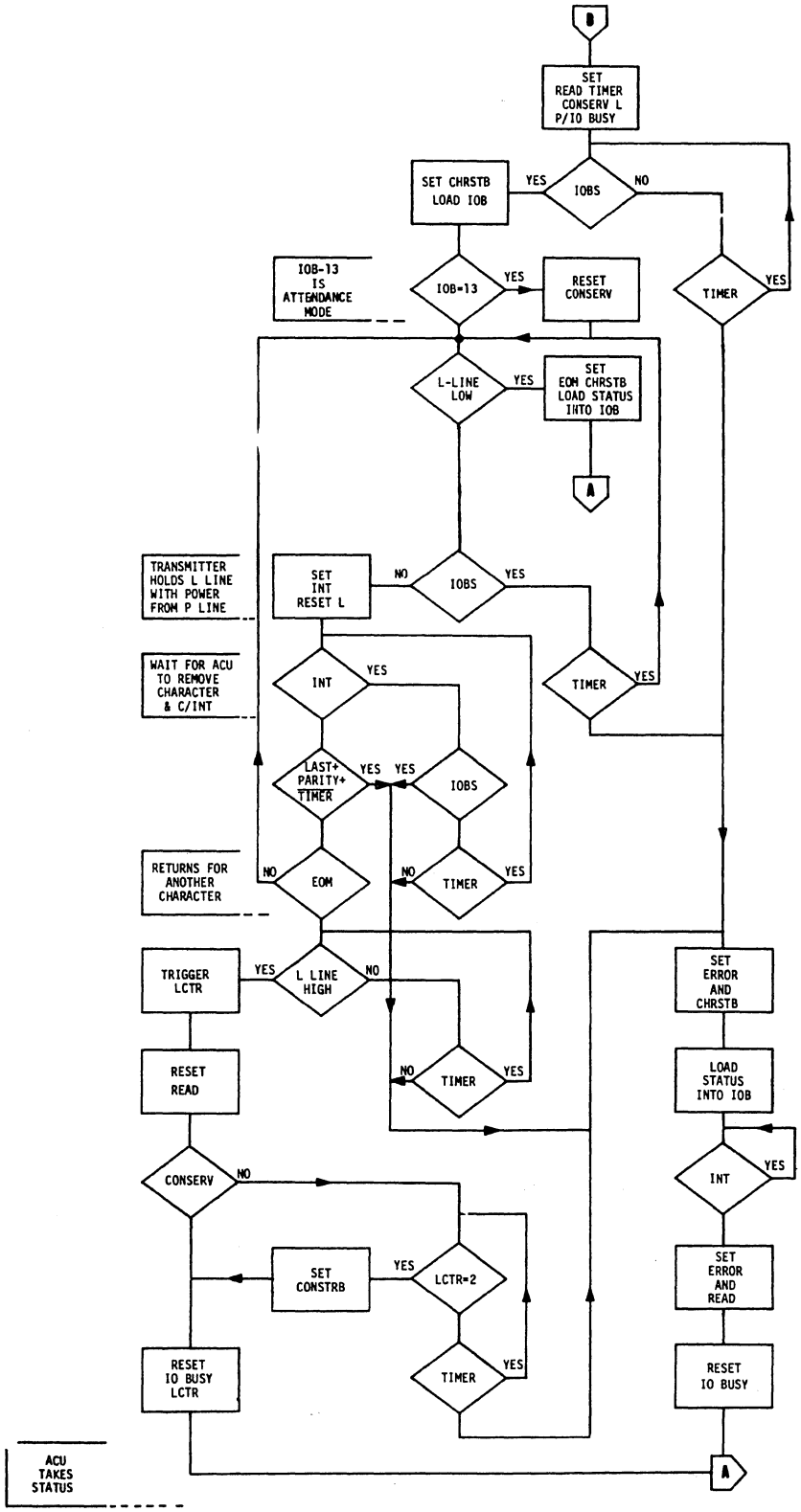
A terminal disconnecting prematurely also drops the L line, starting the termination procedure. In that case the IOC TIMER flip-flop will time out, ending the op in ERROR status.

COLLECTADATA 30 IOC AND TERMINATOR



LOGIC FLOW DIAGRAM

FIGURE 10-12



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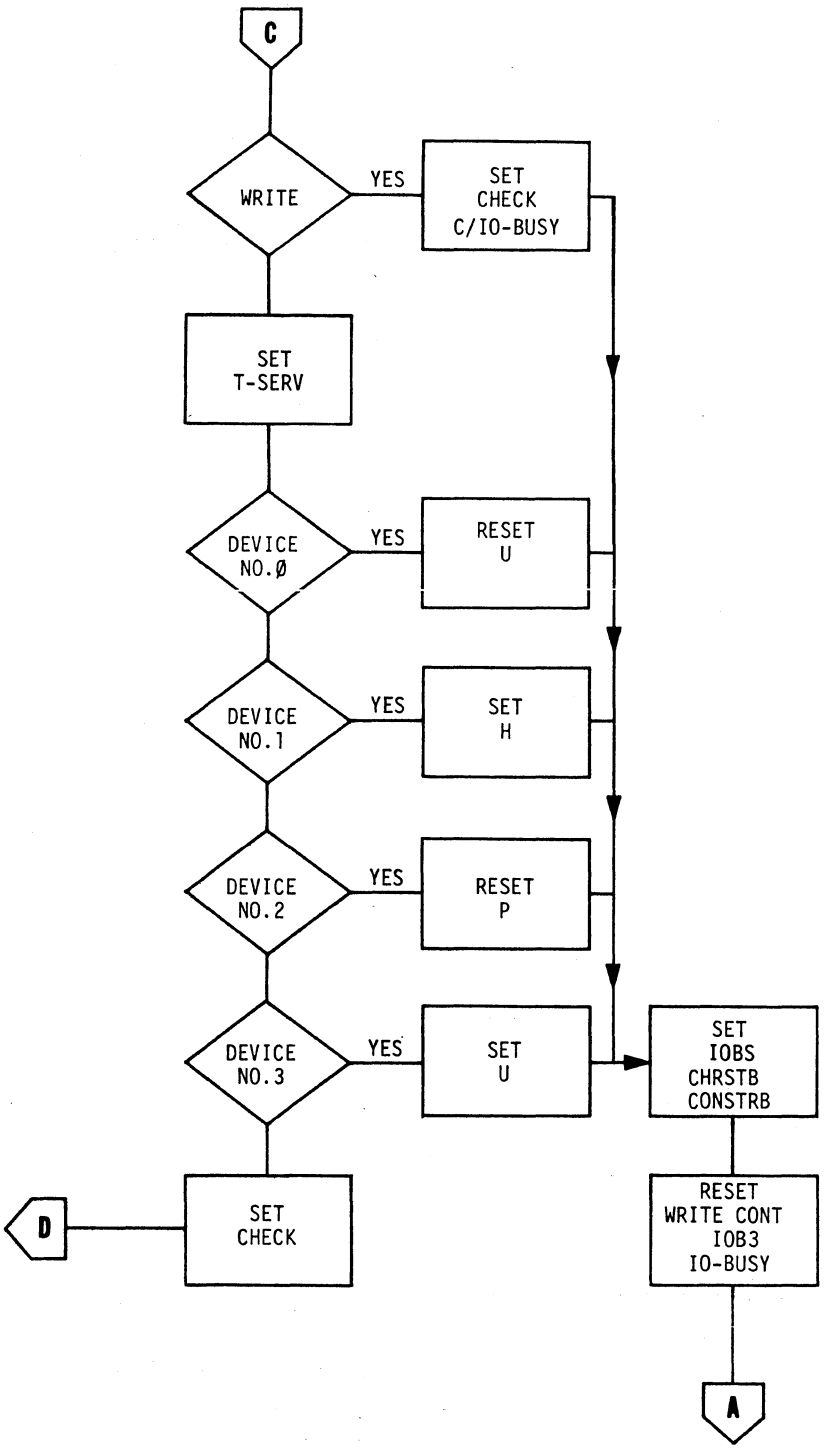
(FIGURE 10-12 cont.)



(FIGURE 10-12 cont.)

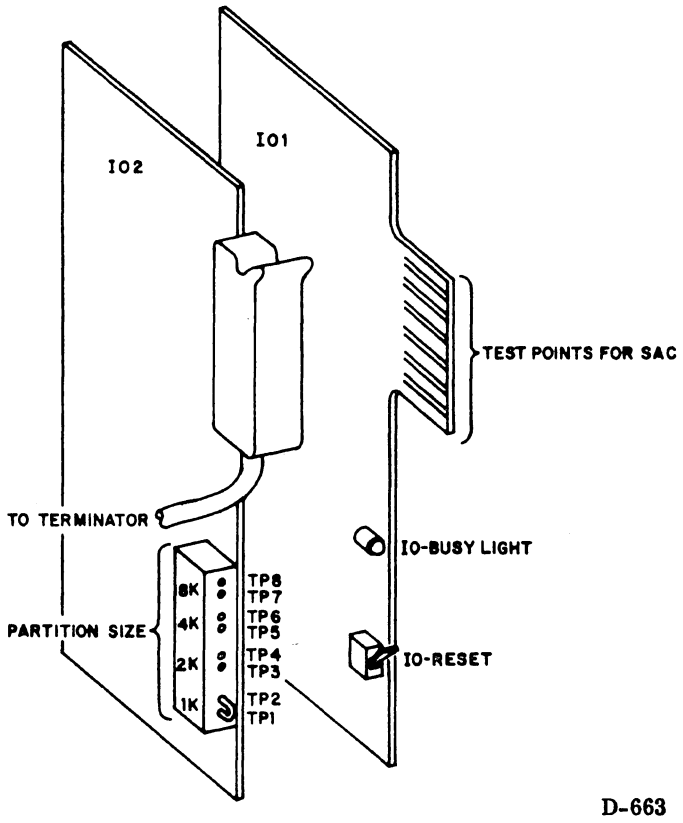
K. MANUAL CONTROLS

I01 - IO RESET - Allows a manual reset of IO channel independant of the main processor.

- IO BUSY LIGHT - Indicates the IO-BUSY signal is active (in INH-SW).
- SAC (service aid card) test points - provision for use of the service aid card.

I02 - PARTITION SIZE - Manual (by jumper) adjustment of partition limit.

Figure 10-13 shows the location of the manual controls, and cable connection to the Terminator.



MANUAL CONTROLS

FIGURE 10-13

L. GLOSSARY

1. INTERFACE SIGNALS

a. ACU SIGNALS

C/INT/5: Clears the INTERR FF in the IOC after a character has been transferred between teh ACU and the IOC.

C/LD-REQ/5: Clears the LDRQ FF in the IOC at the completion of a Load function.

C/SERV-REQ/5: Clears the SVRQ FF in the IOC after a Branch if Service Request instruction has been executed.

IOC-MF-CLK/2: A 300 KHz clock signal providing the basic timing for the IOC logic circuits.

IOS-TO-MN/5: Gates the contents of the IOS shift register in the IOC onto the S bus.

LOAD-IOS/5: Loads the data on the OUT-DATA and IOC-DATA lines into IOS.

PCTR-TO-M/5: Gates the contents of the poll counter onto the S bus.

P/CHECK/5: Presets the CHECK FF in the IOC when a detectable error (address error, invalid op code, or data fault) has occurred in the Processor.

P/IO-BUSY/5: Presets the IO-BUSY FF in the IOC at the initiation of a READ or WRITE instruction.

P/LAST/5: Presets the LAST FF in the IOC when the ACU character count is exhausted or when a Read, non-fill is terminated.

P/LD-REQ/5: Presets the LDRQ FF in the IOC when the ACU initiates the Load (Read CONTROL) operation.

b. IOC SIGNALS

CHECK/3: Output of the CHECK FF.

INTERRUPT/3: Output of the INTERR FF (not gated by ON-LINE), indicating to the ACU that at least one IOC is ready for a data transfer.

INT-REQ/3: Output of the INTERR FF gated by ON-LINE, indicating that the active IOC is ready for a data transfer.

IO-BUSY/3: Output of the IO-BUSY FF; indicates that the active partition is engaged in an I/O transfer operation.

LOAD-REQ/3: Output of the LDRQ FF; indicates that the next I/O operation will be a Load (Read Control).

SERV-REQ/3: Output of the SVRQ FF; indicates that one of this IOCs peripherals has a service request.

c. GENERAL SIGNALS

AM - Attendance Mode

CDL - Flip-flop driven by SCDL; is a part of the delay protection circuit for the L line.

CDR - Flip-flop driven by SCDR; is a part of the noise protection delay circuit for the R line.

CHECK - Status flip-flop set by program error: 1. a WRITE select character, and 2. a WRITE CONTROL with an illegal address.

CONSERV - When set, indicates that the IOC is handling a Data Mode transaction.

CHRSTB - Character Strobe; 6ms one shot. Strobes data or status into the character buffer (IOB).

CONSTRB - Control Strobe; 13 ms one-shot. Detect second service request (on the R line) after an Attendance Mode transaction, and delays the logic to allow for the pick and drop times of the transmitter relays (in READ CONTROL and WRITE CONTROL).

EOM - End of message; detects drop on L line during transmission of last character. Enable normal status to the Character Buffer.

ERROR - Flip-flop set by: 1. bad character parity 2. Timeout 3. INT set when the next character arrives (meaning the last char. has not been taken by the processor). 3. LAST set indicating an incorrect character count for a READ instruction.

FAULT - Flip-flop set by a power failure during an IO operation.

H - Flip-flop; controls the H line. Cleared simultaneously with IO BUSY.

INT - Interrupt; set when the IOC is prepared to transfer a character to or from memory.

I/O BUFFER REGISTER - An 8 bit buffer gated into the INP-DATA bus. The input is either the character bit lines from the transmitter (during READ) or from the OUT-DATA lines from the ACU.

IOB1 through IOB7 - Signals indicating which data positions in IOB are occupied by bits.

IO BUSY - Indicates the I/O Channel is active.

IOBS - Shows presence of data bit on any of the data lines from the transmitters. Fires CHRSTRB, loading the character in IOB.

IOBS DELAY - Retriggerable one-shot; delays character loading until line noise subsides.

IOB3FF - Strobes normal status into IOB during READ or WRITE CONTROL.

L - Flop-flop; controls L line.

LAST - set by the ACU indicating the last (final) character in the program count.

LC1 and LC2 - Count signals from the L Counter (LCTR).

LCTR - L-counter; counts the down transitions on the L line during a READ. Serves to clear IO BUSY, and terminate the READ.

LOAD-REQ - Indicates a reload of the program is required.

P - Flip-flop; controls P line. Cleared simultaneously with IO BUSY.

PARITY - Parallel input chip that checks character parity in READ.

R - Flip-flop; controls R line.

READ - Set by a READ op select character.

RDC - READ CONTROL; set by a READ CONTROL select character.

CONSERV - Flip-flop; set upon entering a READ instruction. Reset if the first character is Attendance Mode. REPLY controls the input of CONSTRB flip-flop during READ.

SERV-REQ - Flip-flop set when a temrinal has requested service.

SCDL - Drives CDL to comprise the delay for L line noise protection. (approx 11ms)

SCDR - Drives CDR to comprise the delay for R line noise protection. (approx 11ms)

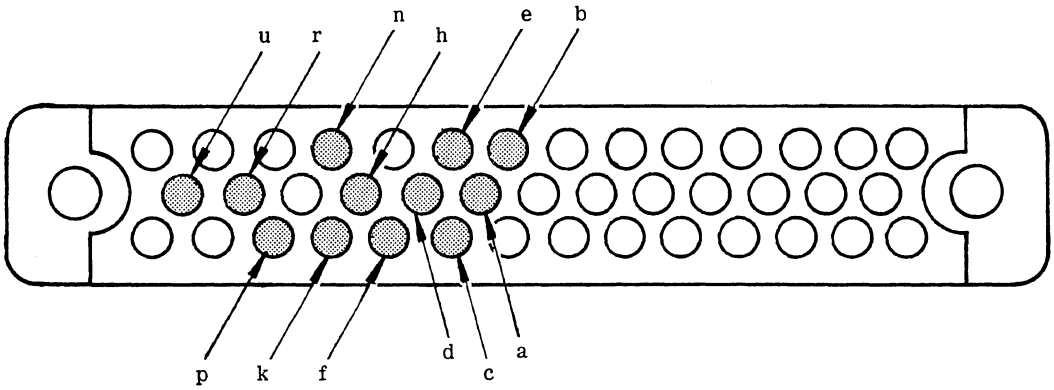
TAM - Terminate Attendance Mode.

TIMER - A 10 second one-shot, initialized on entrance to READ. Sets ERROR and clears IO BUSY if it time out.

TSERV - Toggle Service Request. Detects second service request (on the R line) after a normal Data Mode transaction (not Attendance). Also introduces delay to the logic, allowing for the pick and drop times of the transmitter relays. It is set by WRITE CONTROL or READ CONTROL inst.

X-T/CONSTRB - Second source for toggling CONSTRB (and CHRSTB) qualified by signals to transmitter, ACK, NAK, or IN or OUT of Attendance Mode.

M. REFERENCE



CONNECTOR PIN	SIGNAL NAME
a	Bit 1
b	Bit 2
c	Bit 3
d	Bit 4
e	Bit 5
f	Bit 6
h	Bit 7
k	L-Line
n	N-Line (Ground)
p	P-Line
* r	R-Line
u	U-Line

*R-Line must be located in cable, and connected to plug.

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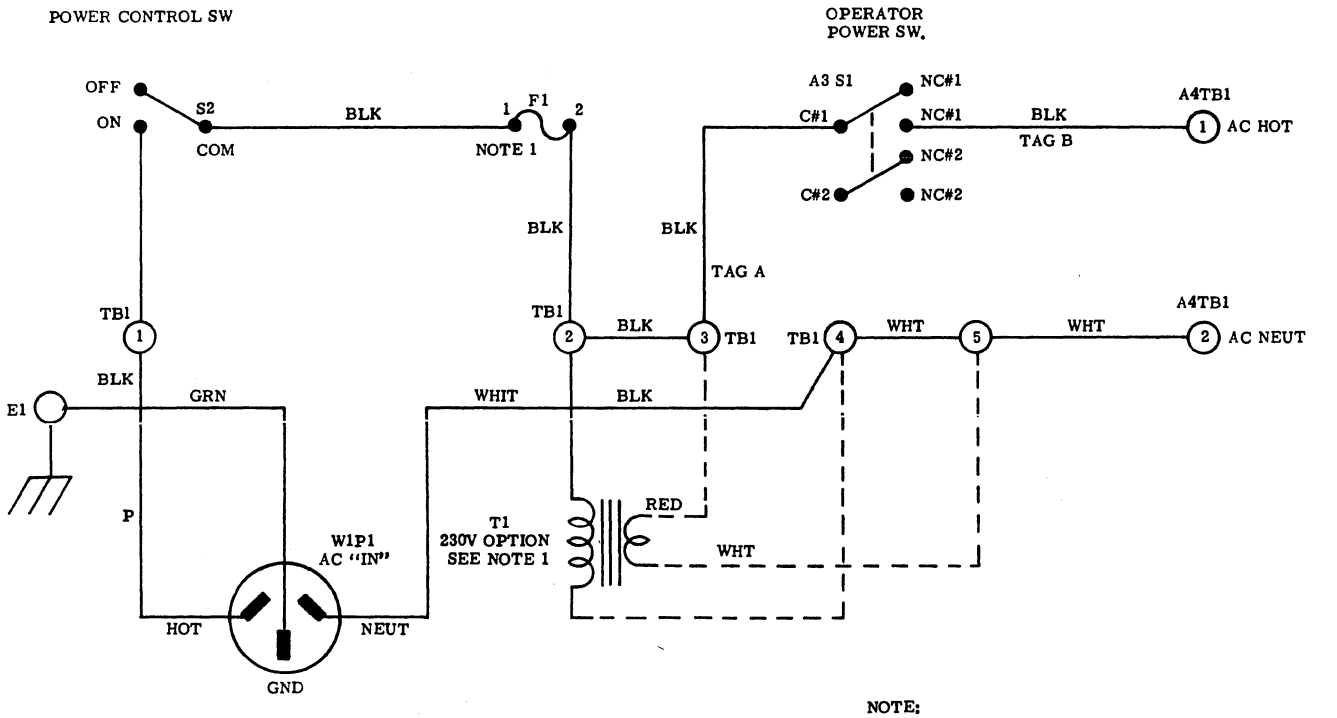
MAIN CABLE PIN CONNECTIONS

FIGURE 10-14



NOTE:

230V OPTION: REPLACE 115V AC POWER CORD WITH 230V CORD, REMOVE JUMPERS BETWEEN TB1-2/TB1-3 & BETWEEN TB1-4/TB1-5, CONNECT TRANSFORMER T1 AS SHOWN & REPLACE FUSE FOR 230V USAGE. REFER TO 9001990 TERMINATOR MODULE UNIT DWG FOR PARTS NOS.

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POWER CONNECTIONS

FIGURE 10-15

SECTION 11

CONTENTS

LIST OF ILLUSTRATIONS

11-1.0 INTRODUCTION

The synchronous communications adapter (SCA) adapts the model 20 processor to a communications environment, where binary synchronous communication (BSC) is used. Because the BSC scheme depends upon line control characters, the SCA can modify characters from memory to become control characters. It can also recognize certain control codes as they are received in incomming messages. However, much of the BSC control character management is software dependent, and is only implemented by the SCA.

The SCA communicates through data sets (commonly called modems) with other SCAs, or other computer systems that are similarly equiped. Transmission can be on private leased lines, or through the public dial system. The SCA can be used with or without the "dial-out" option (CH7), depending upon system requirements. If communication is to only one unit that is less than 50 wire feet away, the local communications option (LCO) can be used instead of the two data sets that are ordinarily required. The LCO is described in the REFERENCE portion of this section.

The SCA can answer, receive, and terminate incoming calls, but requires the CH7 option to automatically dial out. The basic SCA consists of three printed circuit cards, CH5, CH6, and CH8, and requires two adjacient I/O positions within the model 20 processor. However, the position of the CH5 card determines the partition number, and if it is necessary, the SCA can occupy I/O positions 19 and 20 (20 is not addressable by the ACU). Where ever the SCA resides, that partition is dedicated to communication.

The SCA sends and receives continous blocks of message text, using the standard ASCII line control format. As with other I/O channels, the SCA passes information to and from the ACU through parallel data-bus lines. Data is transmitted and received through data sets or the LCO. Several system concepts are outlined in figures 11-1 and 11-4.

Installation configurations will vary from one system requirement to the next. The SCA can be used in a direct, four-wire telephone line system, with, or without constant carrier operation. Or, it can be used with two-wire leased lines without constant carrier. The SCA can be connected to the public dial network as an answer only, or to automatically dial out. When used with the dial network, the constant carrier option should not be used, except under special conditions (such as ASTA). All of these configurations require data sets (modems) to interface to the transmission lines.

The SCA transmits data bits serially from a shift register (IOS) through the SD flip-flop to the modem. It receives data bits serially from the modem into a receiving buffer register (IOR). Figure 11-2 shows a block representation of the data flow within the SCA.

The SCA depends heavily upon software for proper operation. The following text assumes that the proper program is used for the system configuration, and no program errors exist. However there are exceptions to this assumption in the explanations of hardware traps for program error.

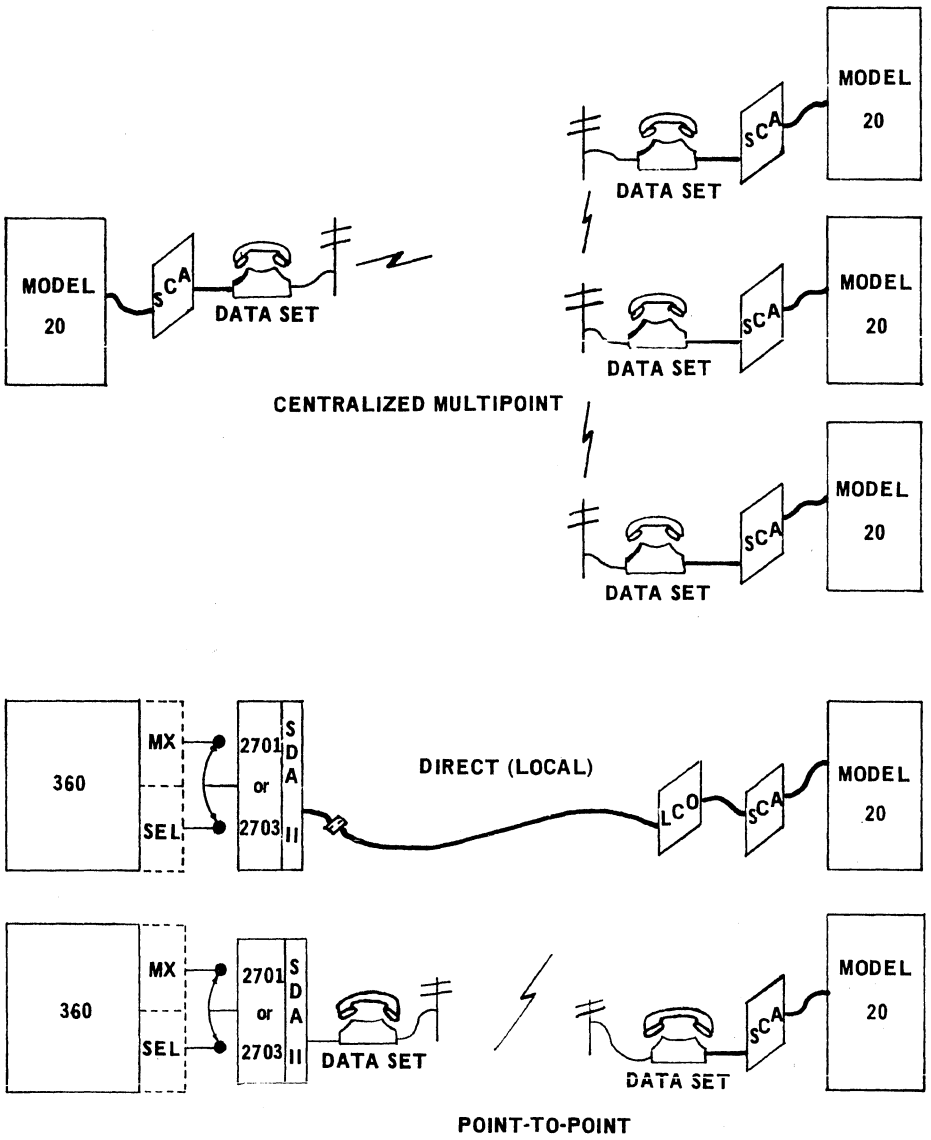


Figure 11-1
SYNCHRONOUS COMMUNICATIONS SYSTEMS

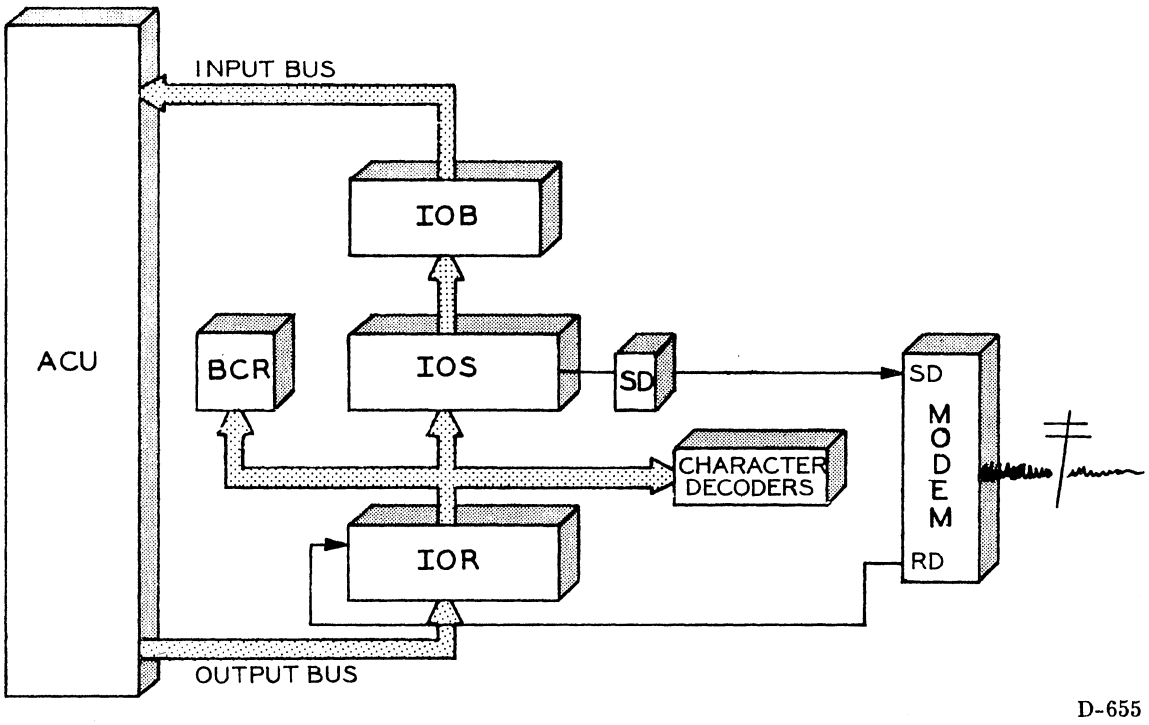


Figure 11-2. DATA FLOW

11-2.0 BINARY SYNCHRONOUS COMMUNICATIONS

The binary synchronous communications (BSC) system is a standard interchange scheme that transmits data as a serial stream of ASCII binary digits (see figure 11-3). Active receiving stations are locked in step with the transmitter by recognizing a specified sync pattern (two SYNs) that start each transmission. When communicating with certain other manufacturers' computers a minimum of six SYN characters must be sent to assure bit phase, then character phase. The SCA depends upon the data set (modem) to acquire bit phase, and requires only two consecutive SYNs to set character phase.

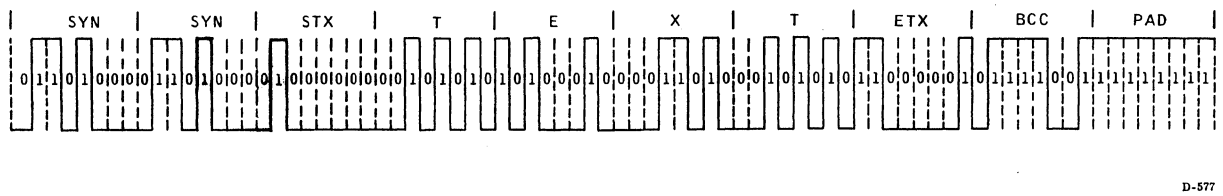


Figure 11-3. SYNCHRONOUS DIGITS

Data link control characters are used to supervise line activities, and provide system flexibility. For example, with the proper use of control characters, one data link can be uniquely selected among many stations of a multi-terminal system.

The SCA can operate as a two-wire point-to-point, four wire point-to-point (with or without constant carrier), or into the public dial network lines. However, in any of these configurations, the message transfer can only be one direction at a time.

11-2.1 DATA LINK

A data link consists of: the communications channel, the data sets (or line adapters), and the communications-control portion of each station on the channel. Each data link is a seperate entity, with complete message compatibility throughout the link. Terminal equipment may vary from a basic send/receive reader-printer, to a control unit serving several input/output devices, or it can be a processor interconnected to another communications system.

Data links can be point-to-point, or multipoint. Point-to-point transmission is between two stations only. However, if the data link interfaces with the dial lines, communication can be made between any number of stations, but always one station at a time.

Multi-point data links operate on leased or privately owned lines. Communication is between one master unit and one or more receiving units. Although there are many possibilities within multi-point systems, the conventional system is controlled by a master station, and all stations communicate with it. Figure 11-4 shows some of the variations in point-to-point and multi-point systems.

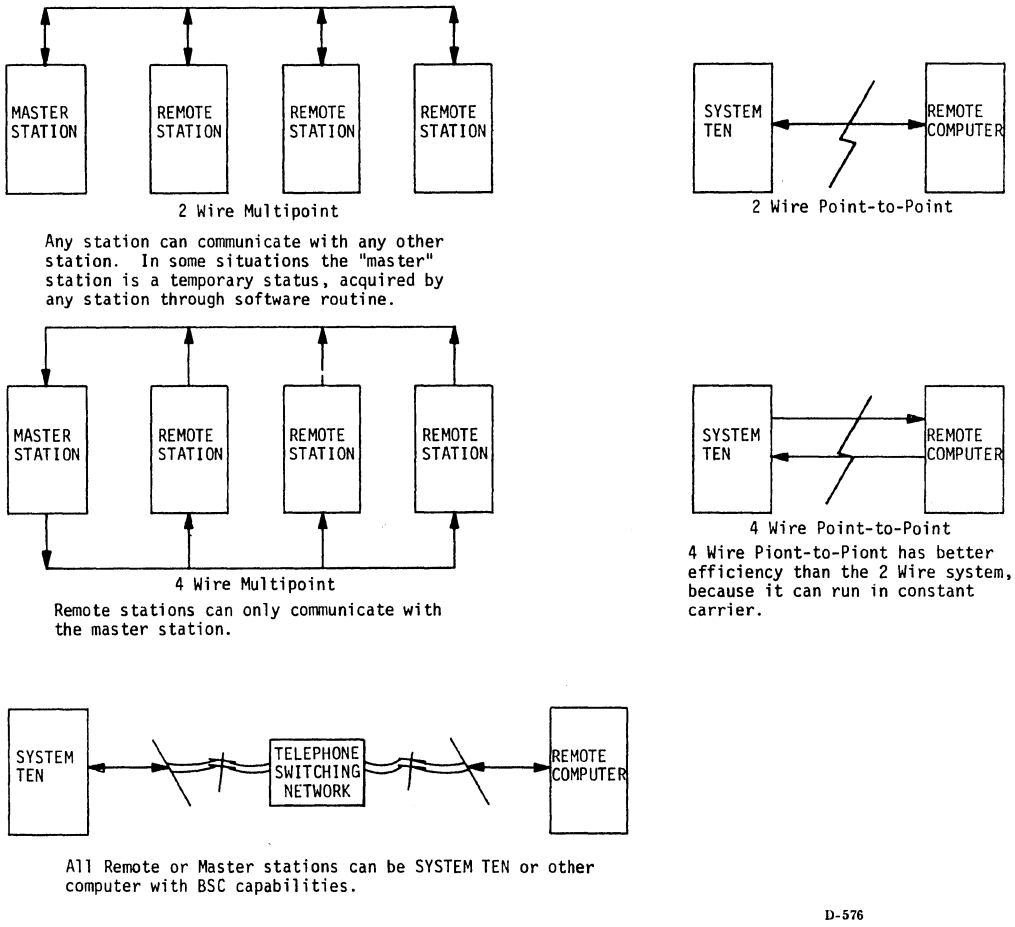


Figure 11-4. SYSTEM VARIATIONS

DATA LINK CONTROL

The SCA uses eleven control codes to maintain orderly operation of the data link. These character codes are transmitted to cause certain actions within the communications system. The particular use of each code is given below.

- SYN - Synchronous idle. Establishes synchronism, and is a time-fill, in the absence of a data or control character.

- SOH - Start of heading. Precedes a block of heading characters. A heading consists of auxiliary information (such as routing and priority) that may be necessary for the system to process the text portion of the message. The SOH character is not included in the block check count.

- STX - Start of text. Precedes a block of text characters. Text is that portion of a message, treated as an entity, to be transmitted to the ultimate destination without change. STX also terminates a heading. The first STX or SOH character is not included in the block-check count.

- ETB - End of transmission block. Indicates the end of a group (block) of characters started with an SOH or STX. The blocking structure is not necessarily related to the processing format. The block-check character is sent

DATA LINK CONTROL (Continued)

immediately following ETB. ETB requires a reply, indicating the receiving station's status (ACK, ACK 0, ACK 1, or NAK). ETB character bits are included in the block-check count.

- ETX - End of text. Terminates a block of characters started with an STX and transmitted as an entity. The block-check character is sent immediately following ETX. ETX requires a reply, indicating the receiving station's status. ETX character bits are included in the block-check count.

- EOT - End of transmission. Indicates the conclusion of a message transmission, which may contain one or more blocks, including text, and the associated headings. It causes a reset of all stations on the line. An EOT must be the first character following synchronization characters, or ERROR is set in the SCA. The exception to this is the DLE EOT combination, which is usually considered a mandatory disconnect, and does not set ERROR.

- ENQ - Enquiry. Used as a request for a response, to obtain identification and/or an indication of station status (ACK, NAK, etc.). It can also be used to obtain a repeat transmission of a reply, if a transmission was not received when expected, or was garboled.

- ACK, ACK Ø, ACK 1 - Affirmative acknowledgement. These replies indicate the previous message block was accepted, and the receiver is ready to accept the next block of transmission.

  ACK Ø and ACK 1 are made up of two ASCII characters, a DLE followed by either a 1 or a Ø.

  Single ACKs or alternating ACK 0 and ACK 1 replies may be used. ACK Ø and ACK 1 provide sequential checking of a series of replies. ACK Ø is used as a positive reply to selection in a multi-station environment.

- NAK - Negative acknowledgement. Indicates that a previous message block was unacceptable, and the receiver is ready to accept re-transmission of the erroneous block. It is also the "not ready" reply to station selection.

- DLE - Data link escape. A control character used exclusively to provide supplementary line control signals. Expresses that a completely new thought or operation follows; a break in routine.

  Also used for alternating affirmative acknowledgements, and WABT (below).

- WABT - Wait before transmitting. A temporary not-ready condition that is to be followed by a prearranged period of time before transmitting. WABT is transmitted as two codes, DLE ?.

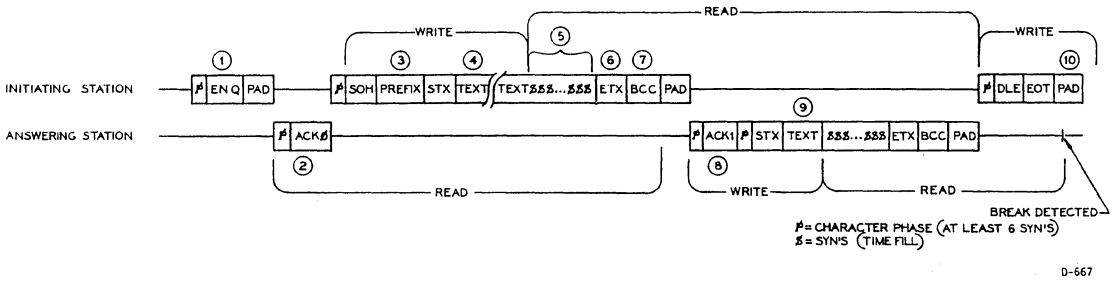
11-2.2 BSC OPERATION

In a point-to-point system, a situation can occur where both stations may attempt to acquire the line simultaneously. This is called contention. To minimize this problem, a station can be given a software priority, where the higher priority station will not answer if it is ready to send when an ENQ is received.

A multi-point system polls and selects from a master station (a pre-assigned controlling station). Polling, an invitation to send, is transmitted from the master to a specific remote station. Selection is a "prepare to receive"notification from the master station to one or more remote stations.

A variation on the multi-point system is the software master/slave configuration. In this system, the master status is acquired through a software priority scheme. Once the master status is acquired, the station remains master until an EOT is transmitted. An EOT relinquishes the master status, and another station can become the master.

In a multi-point system, each station is assigned a unique primary (software) identification for polling and selection. If stations in the data link have multiple input/output capabilities, the identification may contain up to seven characters. The first character would be the station identity, and additional characters may indicate specific components that are desired (such as punch, type, record, etc.). Once a station responds affirmatively, message transmission can start. Message transmission is in continous blocks. An example of message exchange is shown in figure 11-5, below. Remember, each system configuration will have its own format for acquiring the line, or answering. Headings and prefixes can be added if desired, but must be compatable at all stations, and should remain within the ASCII format.



1. Enquiring; is the receiver ready, and the line free to use?
2. Answer; yes.
3. Prefix heading with auxiliary information concerning this message.
4. Message text.
5. Time fill SYN's while waiting for READ instruction.
6. First character of READ instruction is control ETX; transmitted to end message.
7. Block check character.
8. Transmission received O.K. (does not necessarily mean BCC is good).
9. Second text message.
10. EOT ends transmission; is not acknowledged.

Figure 11-5. MESSAGE FORMAT

11-2.3 ERROR CHECKING

VRC

Each character is given odd parity, and is checked for character parity at the receiving end. In the binary synchronous system, character parity is called Vertical Redundancy Check, or VRC. If bad parity is detected in the SCA, the ERROR flip-flop is set to indicate bad status. Message control is a software function, but usually an ERROR condition would be acknowledged with a NAK.

BCC

The entire text block is also checked for accumulated parity. Each of the parallel bit lines between the buffer and shift register is monitored by a seperate flip-flop. The flip-flop is toggled if a 1 bit is present, and not toggled if a zero bit is present. At the end of the message block, these seven flip-flops represent the odd/even accumulation of the 1s that have been transmitted through that particular bit position. When an ETB or ETX is detected, the states of the seven flip-flops are transmitted. This is the Block Check Character, or BCC.

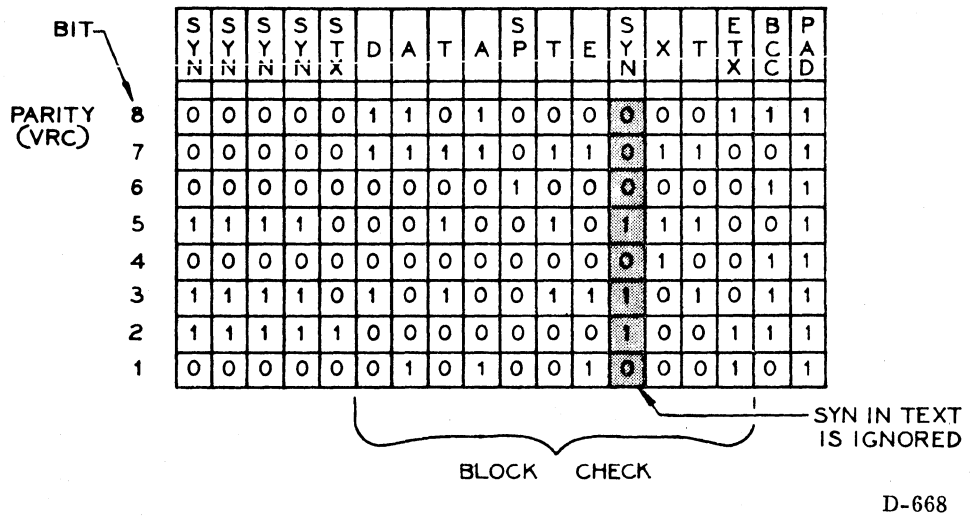


figure 11-6. MESSAGE BLOCK

Meanwhile the receiver has checked each data line in the same manner, and compares the receiver block check to the BCC that was received. In the SCA, ERROR is set if the two do not compare. The block check character is not necessarily an ASCII character (except by accident), and the eighth bit (parity) in the BCC is character parity only, NOT a longitudinal accumulation of all parity bits. Figure 11-6 shows a small message block, and the parity checks that are made. In the example, there is a SYN character that was hardware generated as a time fill. SYN characters within the text are ignored. A pad character of all 1s follows all non-constant carrier transmissions. This allows the data set to properly complete transmission. A constant carrier system has four wires, and 1s are transmitted continuously on two wires, while the station is receiving over the other two wires.

11-3.0 PROCESSOR/SCA INTERFACE

The processor interface signals are common to every I/O partition. Specific uses for interface signals are listed in the reference portion of this section. The data lines to and from the processor are shown below in figure 11-7. Other interface signals are shown in figure 11-8, along with sone of the general routing within the SCA. The illustrations are greatly simplified and should not be mistaken for wiring or logic diagrams.

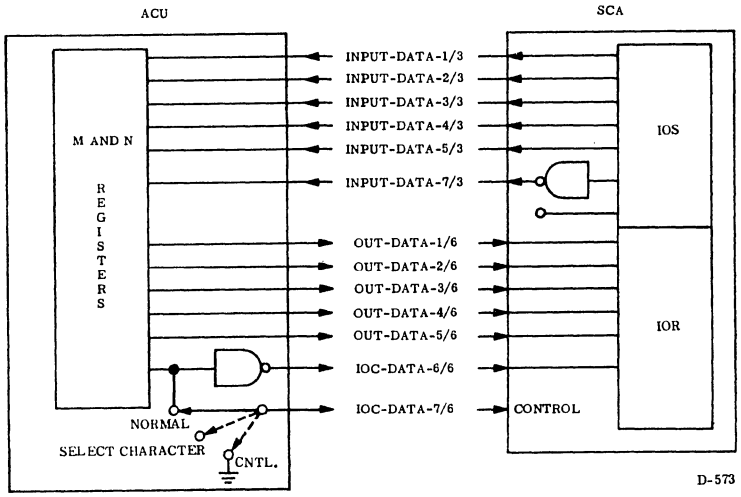


Figure 11-7. DATA LINES

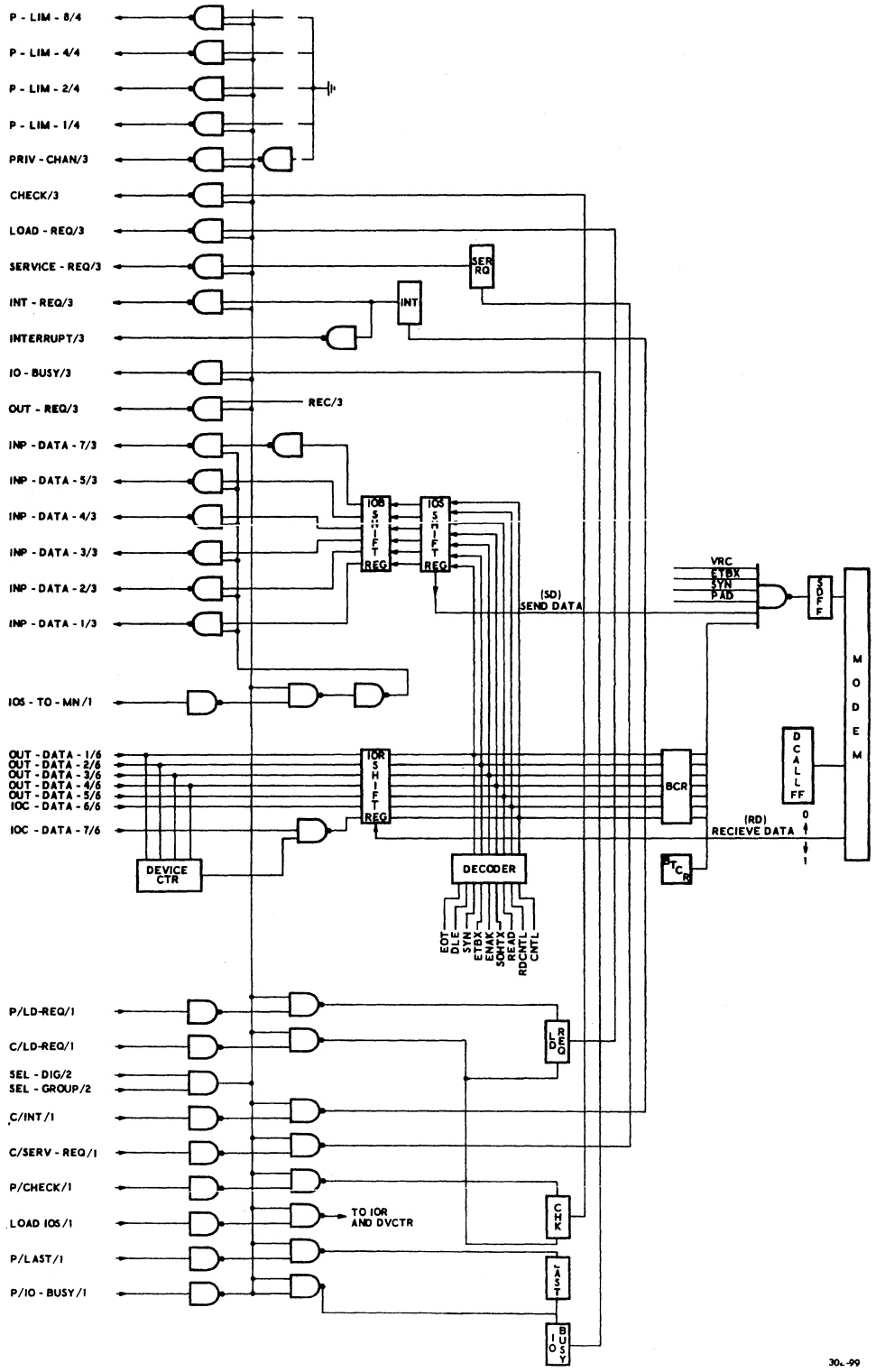


Figure 11-8. SCA INTERFACE

11-4.0 SCA/DATA SET & AUTOMATIC CALLING UNIT INTERFACE

Data set and automatic calling unit connections are made through front-edge connectors on the CH8 and CH7 cards respectively. The data set requires only three signals from the SCA, remote control (RC), request to send (RTS), and send data (SD). The automatic calling unit is supplied through a seperate cable, and requires digit lines and cordination signals from the SCA. Figure 11-9 shows the signal interface; signal definitions are given in the reference portion of this section.

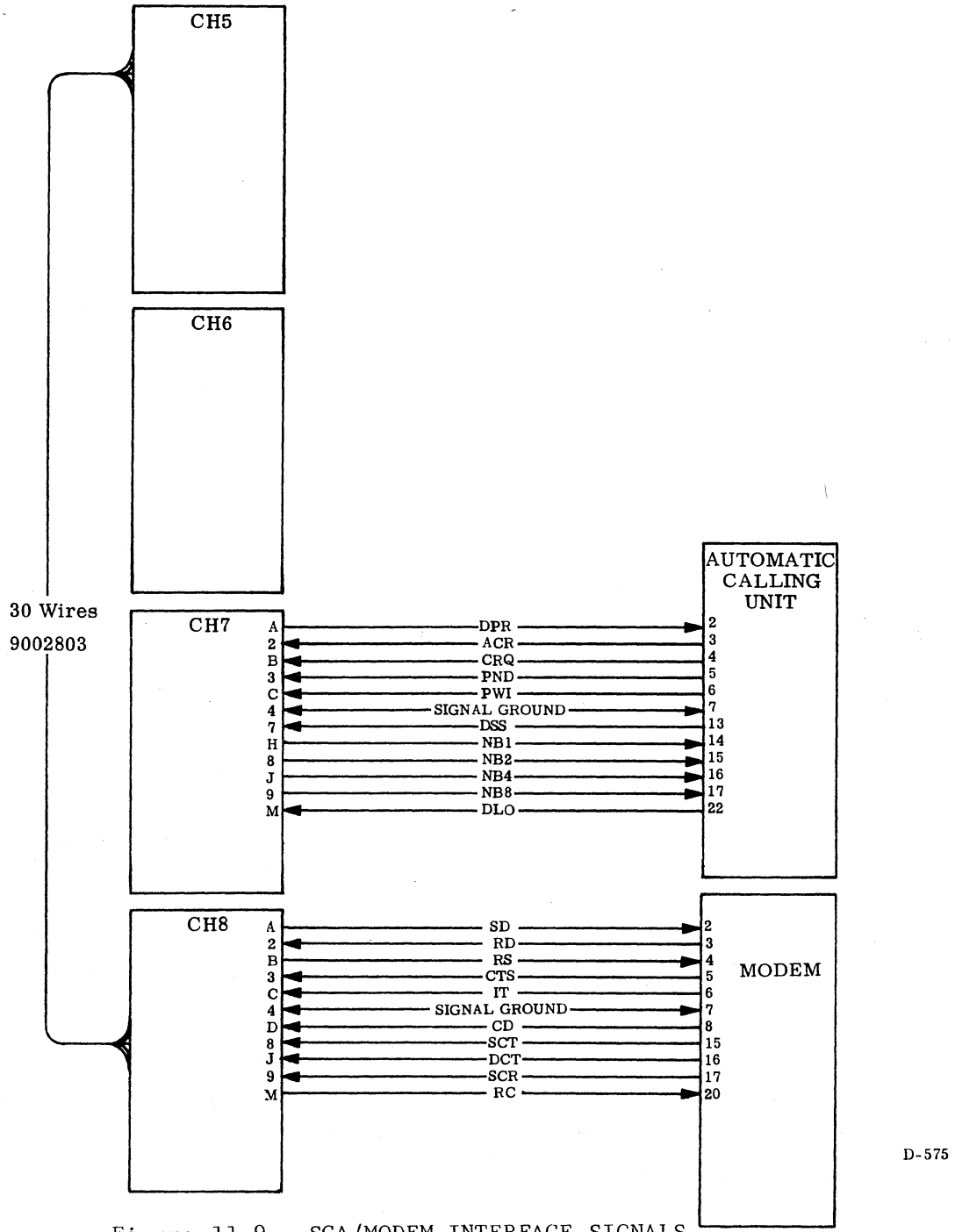


Figure 11-9. SCA/MODEM INTERFACE SIGNALS

11-5.0 SCA OPERATION

The I/O select character, shown below, contains the basic instruction, or operation, in the 5, 6, and 7 bits. The device number (LA) is carried in the lower four bits. The SCA does not have devices to control as other IOs have, so it uses the device number for other purposes. The device number is primarily used by the SCA to set the count for the number of control codes that will be sent at the beginning of an operation. The SCA also uses the device number in a WRITE CONTROL operation to command a hang-up (disconnect), to initiate dial out, or to set (initiate) a constant carrier condition. These uses and controls using the select character bits are discussed in greater detail in the paragraphs that follow. The two tables below show a summary of the conditions that cause the SCA to transmit or receive, and the device numbers that cause special functions under a WRITE CONTROL operation. Each operation, READ, WRITE, READ CONTROL, and WRITE CONTROL, is described in the following paragraphs, showing how the SCA accomplishes these operations.

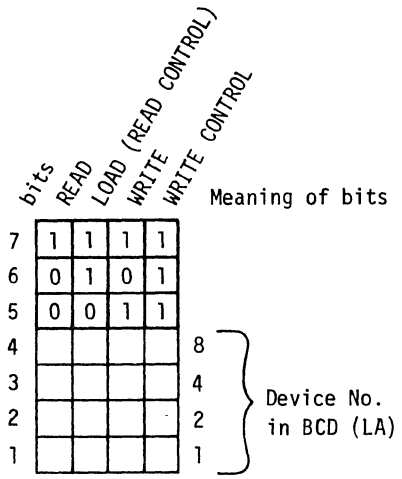


TABLE 11-1 SUMMARY OF FUNCTIONS

TRANSMIT	RECEIVE
WRITE READ and DVCTR>Ø READ CONTROL and DVCTR>Ø	READ and DVCTR=Ø READ CONTROL and DVCTR=Ø

TABLE 11-2 WRITE CONTROL FUNCTIONS

DEVICE COUNTER	FUNCTION
0	SET CONSTANT CARRIER
1	DIAL OUT
2	HANG UP

11-5.1 WRITE CONTROL

WRITE CONTROL is used by the SCA to accomplish the three operations listed in table 11-2. In the case of the dial out operation, the condition is set, and control is relinquished to the dial option, CH7, and the automatic calling unit. When the dialing is completed, or terminated by an abandon call and retry (ACR) signal from the calling unit, control is regained by the SCA, and the operation is terminated. Status conditions are given in a later paragraph.

11-5.2 READ CONTROL

The SCA uses a software (program) READ CONTROL to establish a station address in a multi-point system. There is no normal use for a software READ CONTROL instruction in a point-to-point or dial-up configuration. However if the previous operation in the SCA partition caused CHECK to be set, the processor will present a READ CONTROL select character. This hardware generated select character will not contain digits in the device number positions, and the SCA will only load normal status, and clear the IO BUSY flip-flop.

For multi-point operation, the first operation should be a READ CONTROL select character, with a device number that is greater than zero. This presets LOCKOUT, and causes the SCA to store the device number (from the select character) in the hardware device counter. And because the device count is greater than zero, LOCKOUT is reset, and INTerrupt is set for a character from memory. The character is accepted by the SCA, and stored in the Block-check register as the polling and selection address of the station. As the character is received from memory, the device counter is decremented one count. If the remaining count is still greater than zero, INT is set again for another character. This character will be transmitted as a control code. As long as the device count remains above zero, each character that is received from memory decrements the character count (device counter), and the the 7 bit is made a zero as the character is transmitted. The seven bit being a zero converts the character to a control code. The process is repeated as many times as necessary, until the device count reaches zero. The SCA then waits for a break in transmission on the receive line, sets BREAK, and begins to monitor the incomming bits on the line.

The incomming bits begin shifting through the input register (IOR). If at any time the bit combination in IOR is a SYN character, the COUNT flip-flop is set. The next bits are clocked into IOR as groups of eight. If the group is not a SYN character, COUNT is reset, and the bits are monitored for the first SYN again. The process is repeated, if necessary, until two successive SYNs are detected, and character phase is set (CHPHAS).

Each new character in IOR (after character phase) is checked for a SYN code, and if it is a SYN, it is ignored. Bits 1 through 5 of the first non-SYN character, after character phase, are compared to the polling and selection address that is stored in the block-check register. If the address does not match, the BREAK flip-flop is reset, and the SCA waits for another break in transmission. If, however, the address does match, the block-check register is cleared, and COMPARE is set. The station address in IOR is examined for a 6 bit. If there is no 6 bit, FLAG is preset. This indicates either polling or selection according to prearranged agreement. The SCA relies upon a software response to polling or selection.

Certain character codes are continually watched for when the SCA is receiving. A DLE code sets the DLE flip-flop, as the following character must be considered as a part of a DLE pair. An SOH or STX starts the block-check accumulation. An ETX or an ETB sets the ETBX flip-flop, and the following character is compared to the accumulated character in the block-check register.

11-5.3 READ

A READ instruction is normally used to transmit the ending codes (ETX,ETB, etc) of a previous WRITE operation, then receive data. READ and READ CONTROL are identical, except that the READ instruction does not store and compare a polling and selection address. Instead, if the device counter is greater than zero, the SCA requests characters from memory (one at a time), converts them to control codes, and transmits them. As with the READ CONTROL operation, the device count is decremented with each character transmission, and when it reaches zero, the SCA begins to receive.

Character phase is established by receiving two consecutive SYN codes, starting the receive portion of the READ instruction. A READ instruction should always be terminated by an ending code (such as ETX). If it is not, and the ACU sets LAST (because the instruction character count is exhausted) ERROR will be set.

A READ instruction can be used by an SCA that does not have automatic dialing, and is manually dialled. The RC (remote control) line is set by a READ instruction with a device number (LA) equal to zero. During the manual dialing, the SCA times out, and the instruction is repeated. The timeout/restart loop continues until the dialed station answers. When the remote station answers, the READ instruction is terminated, and can be followed by a WRITE instruction. In the manual dialing configuration, the remote station must be programed to transmit first, when the dial connection is made.

11-5.4 WRITE

The primary purpose of a WRITE instruction is to transmit data to a remote station. Under a WRITE instruction, the SCA can transmit control codes (if the device counter is greater than zero), or it can transmit normal data characters. The SCA cannot receive characters from a remote station under a WRITE instruction.

The processor enters a WRITE instruction by placing the select character into IOR, and setting IO BUSY. The device counter is loaded with the device number (LA) that is present in the select character. At this point a ten-second timeout is started. The DLE and all status flip-flops are cleared in preparation to transmit, and the line is monitored for a break (inactive period). When a break is found, BREAK, INT, and RTS (request to send) are set. The character phase (CHAPHAS) flip-flop is held reset, and a one-second timer is started.

At one second intervals, when transmitting, the one second timer interrupts transmission, and automatically injects two SYN codes. This fulfills certain requirements of some foreign computers (the SCA does not require these when it is receiving). The same flip-flops are toggled when the SCA is preparing to transmit initially. This causes every transmission to be preceded by two hardware generated SYNs.

At this point the SCA is tied to a loop, sending hardware generated SYNs until the ACU loads a character into IOR, or the ten-second timeout expires. The one-second timer is of no consequence if only SYNs are transmitted.

A WRITE instruction with a device number (LA) that is greater than zero is used to transmit control codes at the beginning of a message. A typical example of this is a DLE pair, where the device counter is set to 1, until the first character is transmitted. The first character, the DLE, was stored in memory as a P, and converted during transmission because of the count in the device counter. The device counter

11-5.4 WRITE (Continued)

is decremented with each transmission, causing the character following the DLE to be trasmitted unaltered. Up to nine control codes can be sent at the beginning of a WRITE message. If data is to follow, one of the control codes should be an SOH or STX.

Once an SOH or STX is transmitted, all passing bits are monitored by the block-check register for the parity accumulation. The block-check character is accumulated during a WRITE instruction, but is not transmitted by this instruction.

When the instruction character count (the B field in the instruction word) is exhausted, the LAST flip-flop is set by the P/LAST signal from the ACU. LAST sets ENDD, which sets SYN, causing hardware generated SYNs to be transmitted until a new instruction arrives from the ACU, or until the ten-second timeout expires.

Transmitting a DLE sets the DLE flip-flop, and is described in the paragraph titled DLE. However if a DLE (P) is transmitted while the device counter is not at zero, the character following the DLE is examined for a 5 bit. If a 5 bit is not present, the 7 bit is suppressed to zero, converting the character to control. This happens even if the device counter is at zero during transmission of the character. The combinations shown below illustrate the relationship of the 5 bit in the code.

Bit	DLE Ø	DLE 1	DLE ?		DLE EOT (D)	
7	0 0	0 0	0 0		0 0	
6	0 1	0 1	0 1		0 0	
5	1 1	1 1	1 1	-all have a 5 bit	1 0	-no 5 bit
4	0 0	0 0	0 1		0 0	
3	0 0	0 0	0 1		0 1	
2	0 0	0 0	0 1		0 0	
1	0 0	0 1	0 1		0 0	
	(ACK Ø)	(ACK 1)	(WABT)		(DISCONNECT)	

The second character of a DLE pair is either numeric or an EOT. All numerics (the question mark is in the numeric column) contain a 5 bit, but the EOT does not. The absence of a 5 bit in the character following a DLE indicates that the character is an EOT, and must be sent as a control code. When the EOT is sent, all transmission is terminated without expecting acknowledgement.

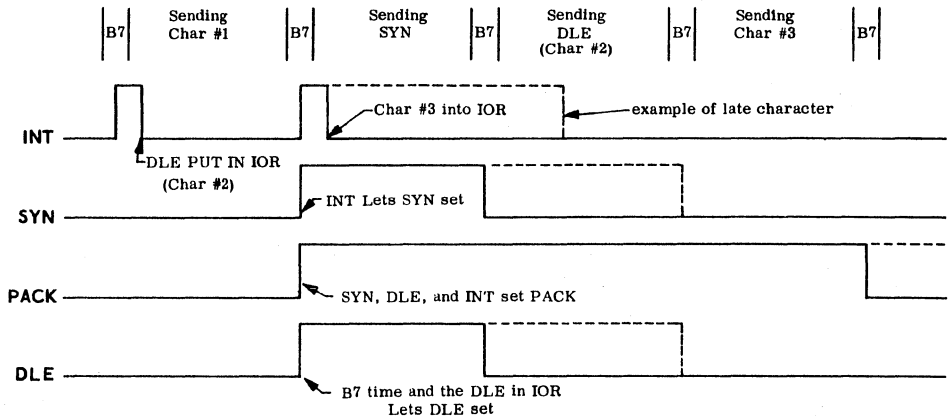
11-5.5 TIMEOUT

Upon entering, and when leaving, each operation (instruction), a ten-second timeout is started. It is also restarted each time the INTerrupt flip-flop is set. This means that the SCA will not timeout when transfering data (unless there is more than ten seconds between characters), and has ten seconds between the end of a WRITE operation and the READ operation that completes the message.

11-5.6 DLE

A DLE code must always be followed by another character, usually an ending code, or the numbers 1 or Ø. If, when transmitting, the SCA detects a DLE, a time fill SYN character is transmitted instead of the DLE. The DLE is held in IOS, and INT is set. Only when the following character from memory is securely into IOR is the DLE transmitted. This ensures that there will be no space or SYN characters between the DLE and the next character. The figure below shows the interaction of the major flip-flops that are involved in the packing of a DLE pair.

During the normal transmission of a character (shown as character #1 in the illustration) a DLE is put into IOR. At the next B7 time, the DLE flip-flop sets. Also at B7 time, INT sets, allowing SYN to set. This sets PACK, and the DLE character is moved to IOS. When the next character arrives, the two characters are sent as a continuous pair. The dotted lines in the figure show an example of a character that is late. If INT is not reset before the next B7 time, an additional SYN is transmitted. Because the contents of IOR and IOS do not change, the DLE flip-flop remains set, extending the PACK preset condition. This situation remains until character #3 is received (or the SCA times out). SYN and DLE reset during the B7 time after the second character of the DLE pair arrives.



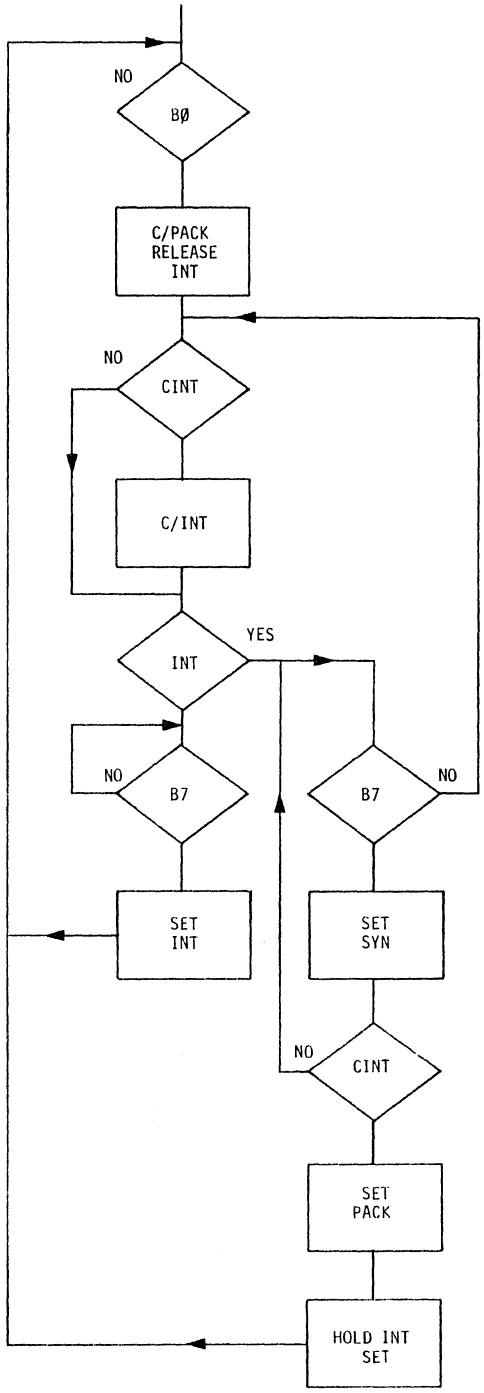
DLE D-670

11-5.7 PACK

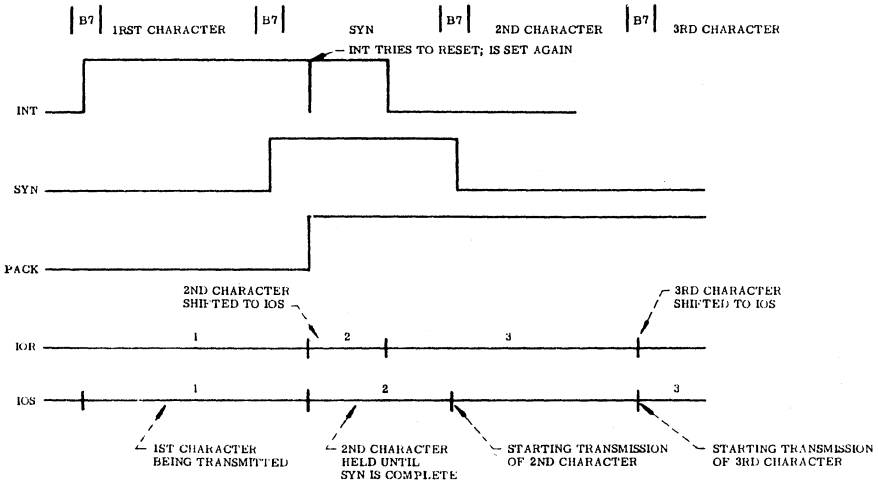
If during a BSC transmission, the processor is unable to supply characters fast enough, a time fill SYN is sent. However, if the late character arrives during the SYN transmission, IOR and IOS are used as buffers to allow more time for fetching the next character. A typical example is shown below, where the late character arrives shortly after the start of the SYN transmission. It is immediately shuttled to IOS, and INT is set again. This calls for the next character before it is needed, allowing extra time for its arrival.

OPERATION

The flow chart below shows the basic elements of the pack operation; timing is shown in the example at the bottom of the page. During WRITE, INT is set each B7 time, requesting the next character. If, by the next B7 time, INT is still set, the SYN flip-flop sets. A time fill SYN is sent to fill the gap. Once SYN and INT are set, PACK is set by the C/INT signal when the ACU puts the character into IOR. The character is immediately passed to IOS, and INT is not allowed to reset. INT resets when the third character (in this example) is loaded into IOR. The next B7 time, character #2 (that has been in IOS) is transmitted. The B7 time following that, the third character is sent. At the next BØ time, PACK resets until it is needed again. In the example below, the numbers along the IOR and IOS lines indicate the positions of the characters.



D-583

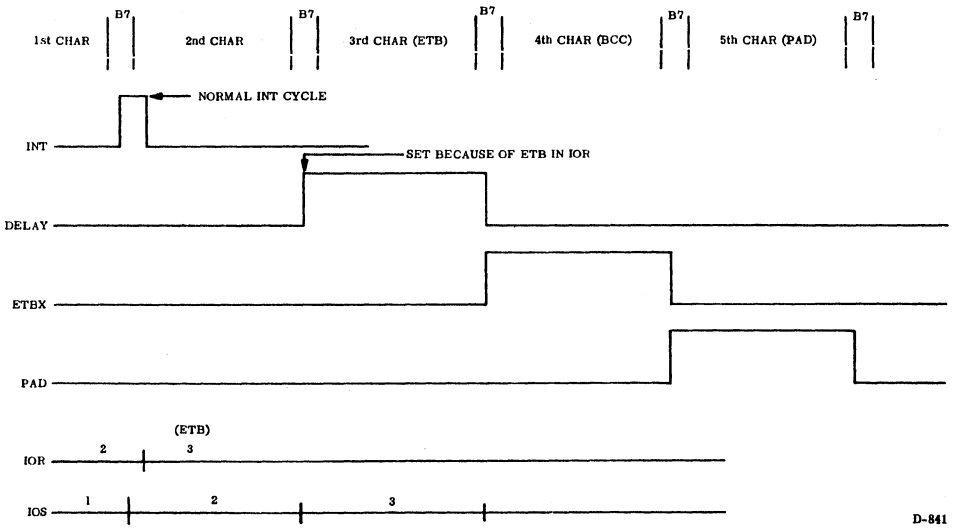


PACK

D-671

11-5.8 DELAY

Each code that is placed into IOR is examined to see if it is an ending character. If the character in IOR is an ending code (ETB or ETX), the DELAY flip-flop is set by the same strobe that moves the character from IOR to IOS. This adds one extra character time to the period between receiving the character from memory, and when it is transmitted. When DELAY resets, the ETBX flip-flop sets, causing the block-check character to be transmitted. ETBX resets, and PAD sets (unless CONCAR is set) causing the pad character, all 1s, to be transmitted. One character time later, the PAD flip-flop resets. An example of the timing that is involved is shown below. The numbers shown in IOR and IOS represent the character that is contained in the register at the time.



11-5.9 FLOWCHART

Figure 11-10 (4 sheets) is a simplified flow chart of SCA operation. As shown on the chart, a device number greater than zero during a READ or WRITE operation causes control codes to be transmitted. The device counter is decremented with each transmission, until the counter is at zero, and normal operation is resumed. This is the process that is used to send the ending code for a WRITE message at the beginning of the following READ instruction.

Figure 11-11 is a simplified flow chart of the general interaction between the ACU and the SCA. The illustration is very general, and for the most part can be applied to the interaction with any I/O channel.

Figure 11-12 is a multipage flow chart of SCA operation. It is taken from the SCA equations, and a detailed explanation is given along side the decision blocks. See figure 11-18 for the overall SCA flowchart.

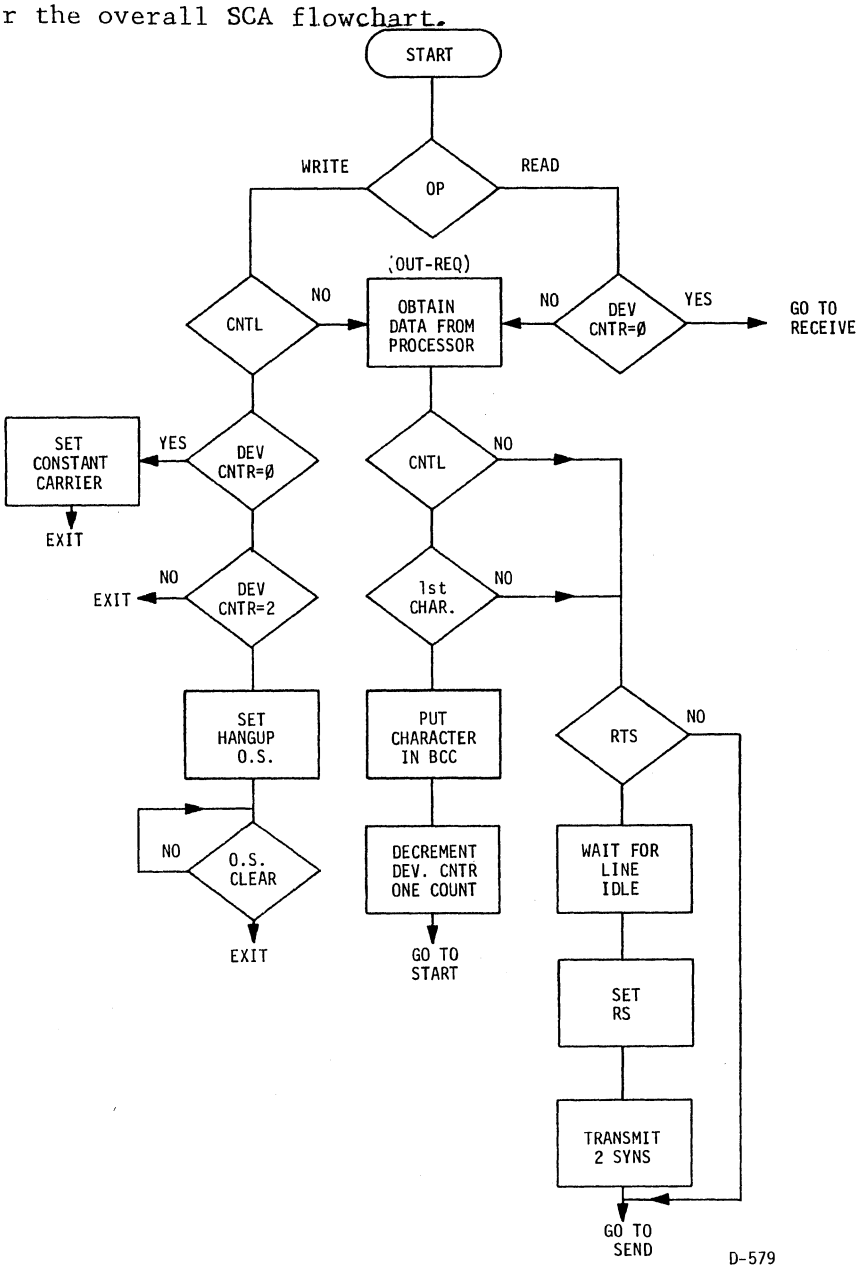


Figure 11-10. SIMPLIFIED FLOW CHART

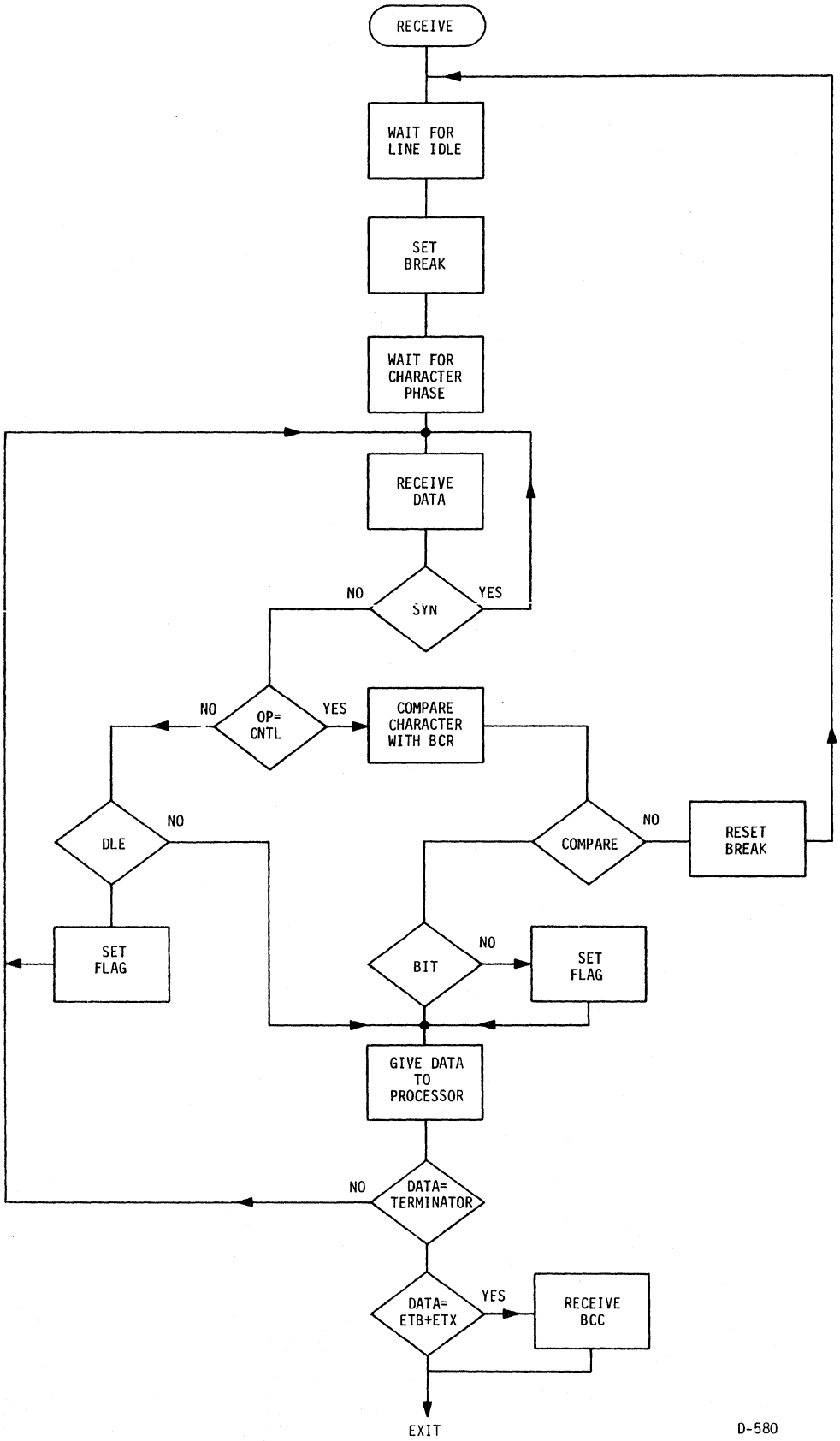


Figure 11-10. (Continued)

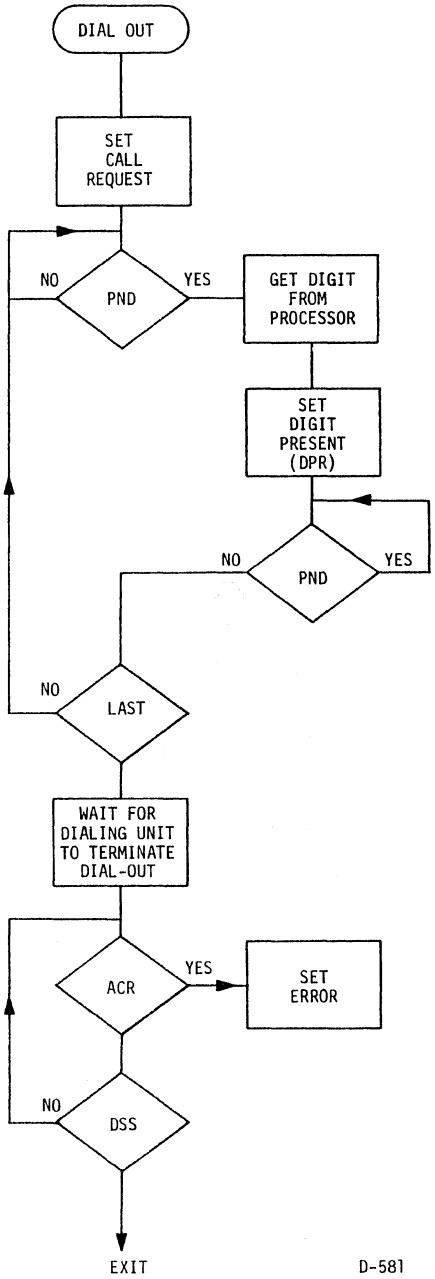


Figure 11-10. (Continued)

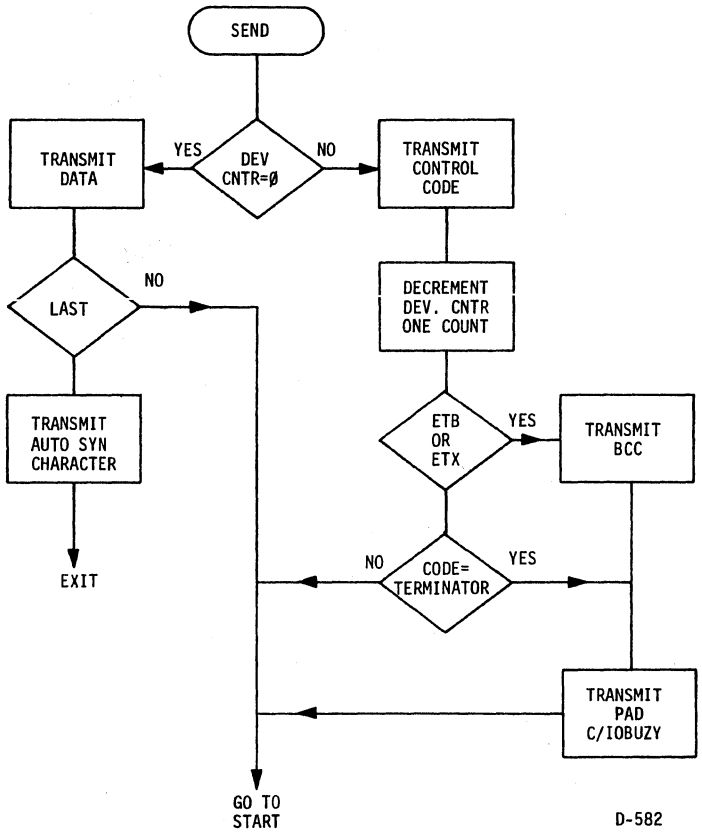
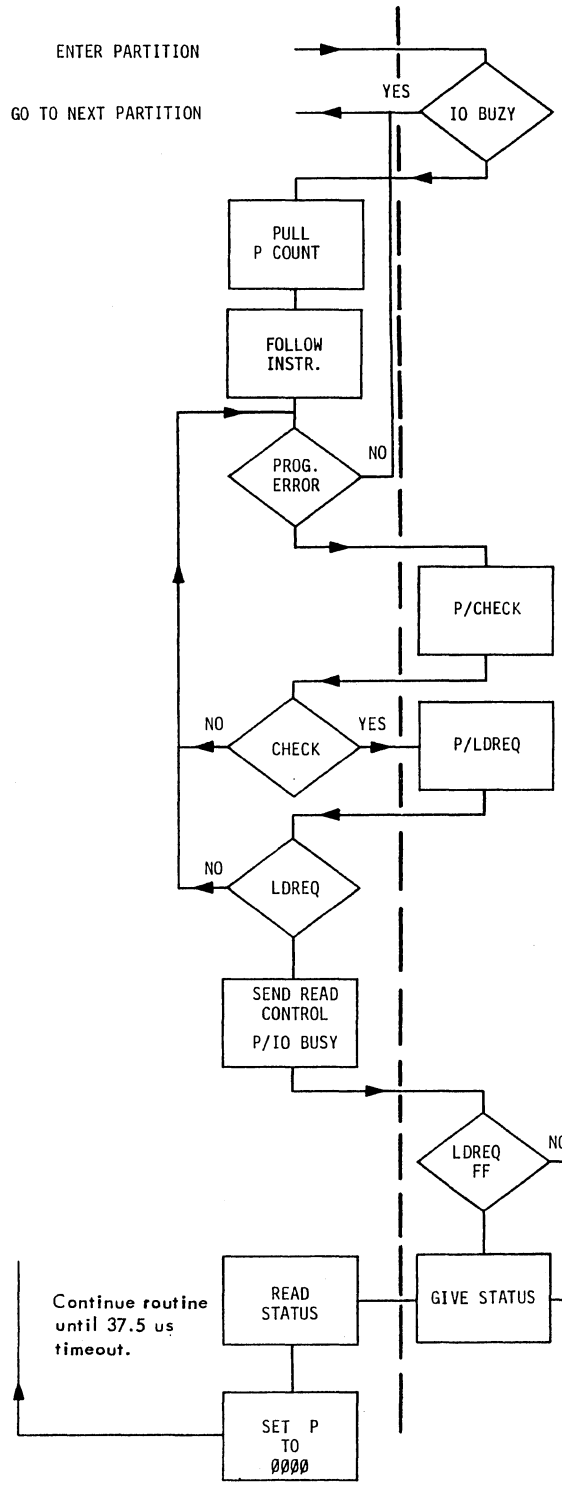


Figure 11-10. (Continued)



This sequence is similar to the operation of all I/O interfaces. The P count is retrieved from the protected area of memory, and the software program is followed from there. In the event that this is the first time the SCA is activated, the P count could be any number. A program error will soon occur (most likely immediately), and the ACU will set CHECK, and return with a READ CONTROL (load).

The SCA detects that a READ CONTROL load condition is different from a READ CONTROL instruction, by the presence of LDREQ. The SCA LDREQ flip-flop cannot be set except by the ACU, because of a CHECK condition. If LDREQ is set when the P/IO BUSY signal arrives, the SCA gives good status and resets IO BUSY. If LDREQ is not set, the IO BUZY flip-flop is allowed to set, as the character must be from a software instruction.

Figure 11-11. INTERFACE OPERATION

INITIALIZATION

The following pages show a step-by-step explanation of the SCA hardware decisions. The SCA logic is arranged to respond to incidents and conditions, rather than times and states. Many of the decision paths that are shown in the flow chart are simultaneous, or nearly so. Some of these places are pointed out in the flow chart where it is important to the logic explanation. It is necessary, in some cases, to take liberties with the flow chart presentation. However, the complete equations (the basis for the flow chart) are listed at the end of this section.

The flow chart is organized into actions that take place, such as "receiving the instruction", "send", etc. These sub-titles are not necessarily modes, or seperate hardware conditions, but are a plain English name for what is going on.

When power is applied to the processor, the SYS-RST signal goes to all I/Os. This general reset, or a manual reset, causes the SCA to clear the flip-flops that are listed in the box below. Other flip-flops are cleared indirectly, but through decisions by the hardware, and are shown later in the flow chart.

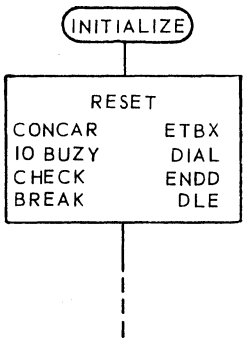


Figure 11-12. SCA FLOW CHART

Sheet -1-

RECEIVING THE INSTRUCTION

The SCA waits for the LOAD IOS signal from the ACU. This signal indicates that a character has been placed into IOR. In this case the character is an I/O select character. The bits are examined to determine if the operation is CONTROL (6 bit), or if the instruction is a READ (no 5 bit). If the operation is a WRITE CONTROL, the 1 and 2 bits are examined, and dial out or hangup may be initiated. The flow continues from page to page, and is self explanitory.

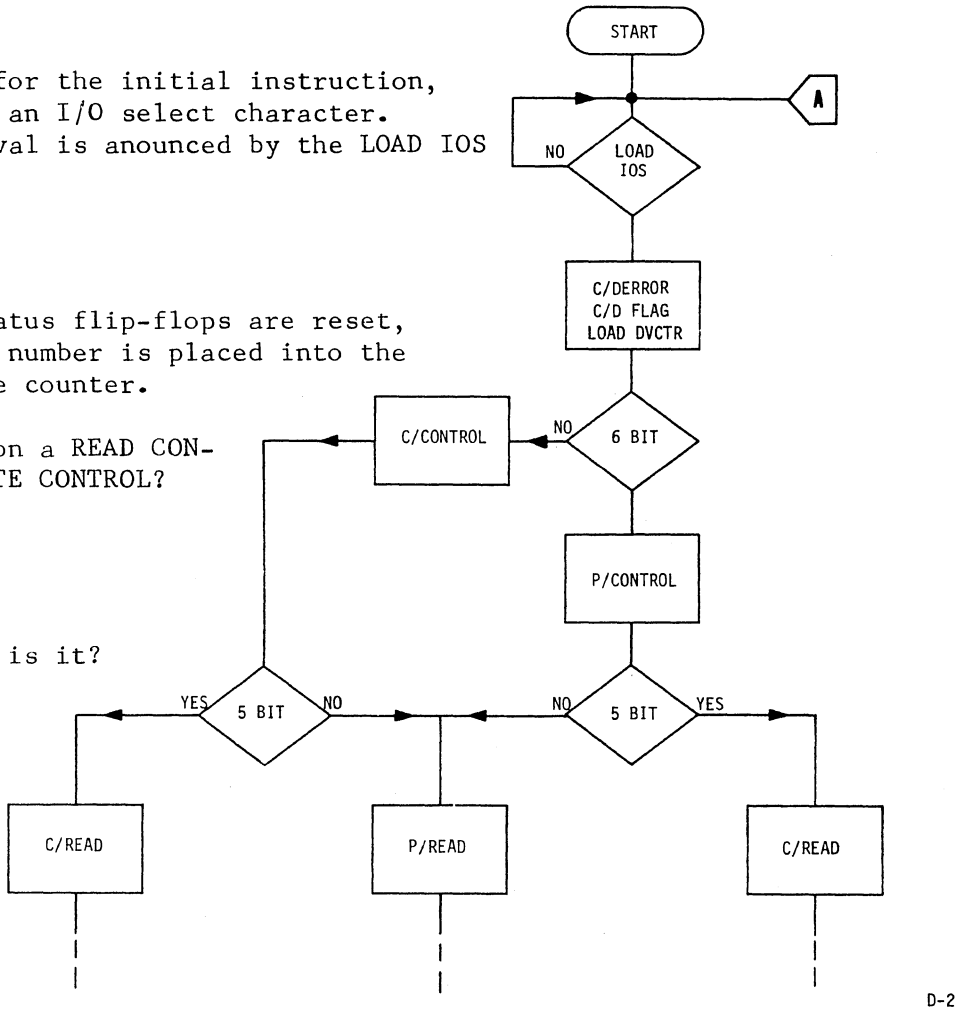
Initialization is complete at this point, and the SCA is ready to receive the operating instructions from the software program.

The SCA waits for the initial instruction, in the form of an I/O select character. Character arrival is anounced by the LOAD IOS signal.

The dialing status flip-flops are reset, and the device number is placed into the hardware device counter.

Is the operation a READ CONTROL, or a WRITE CONTROL?

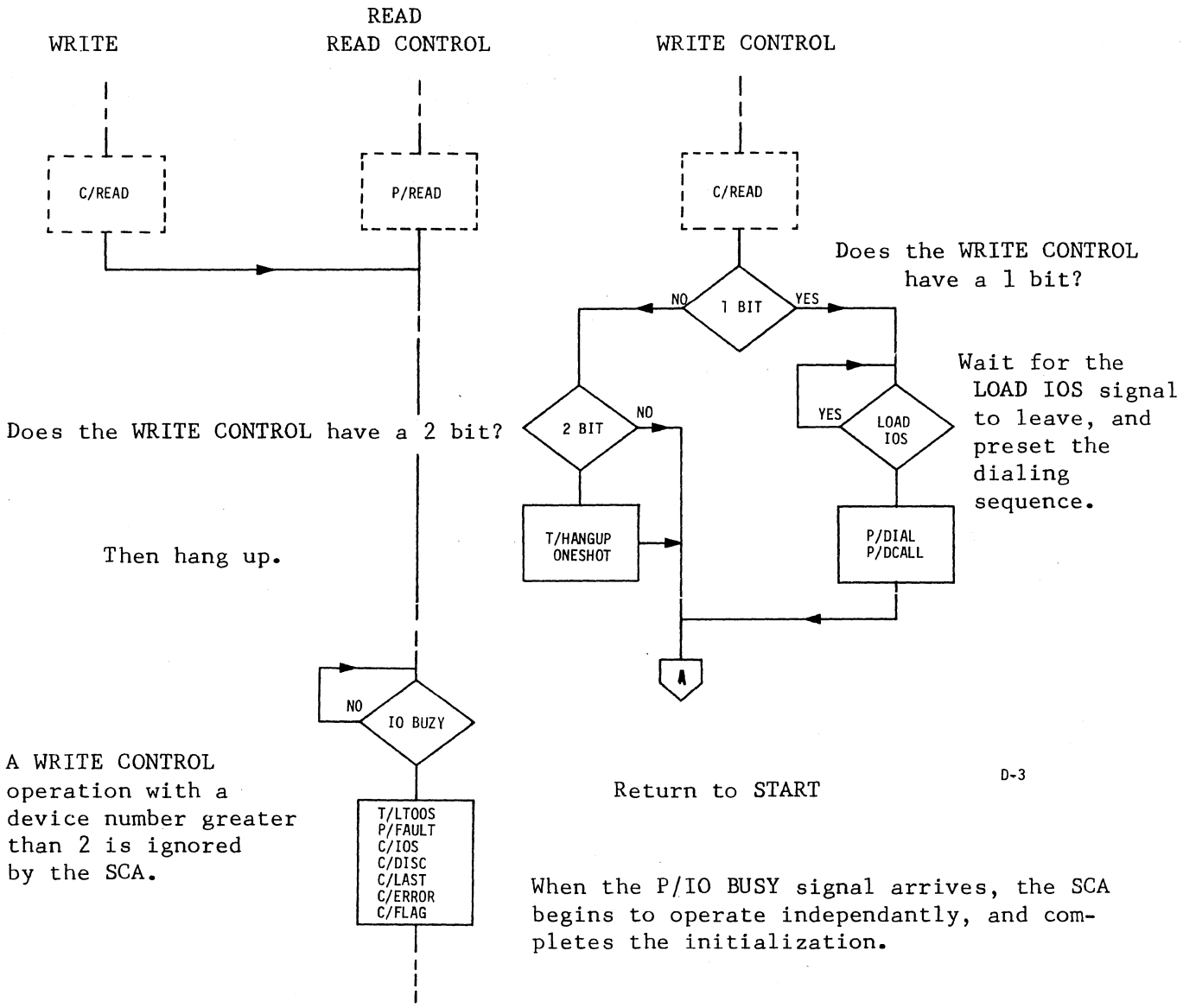
What operation is it?



WRITE READ or READ CONTROL WRITE

Figure 11-12 (Continued)
Sheet -2-

SYNCHRONOUS COMMUNICATIONS ADAPTER

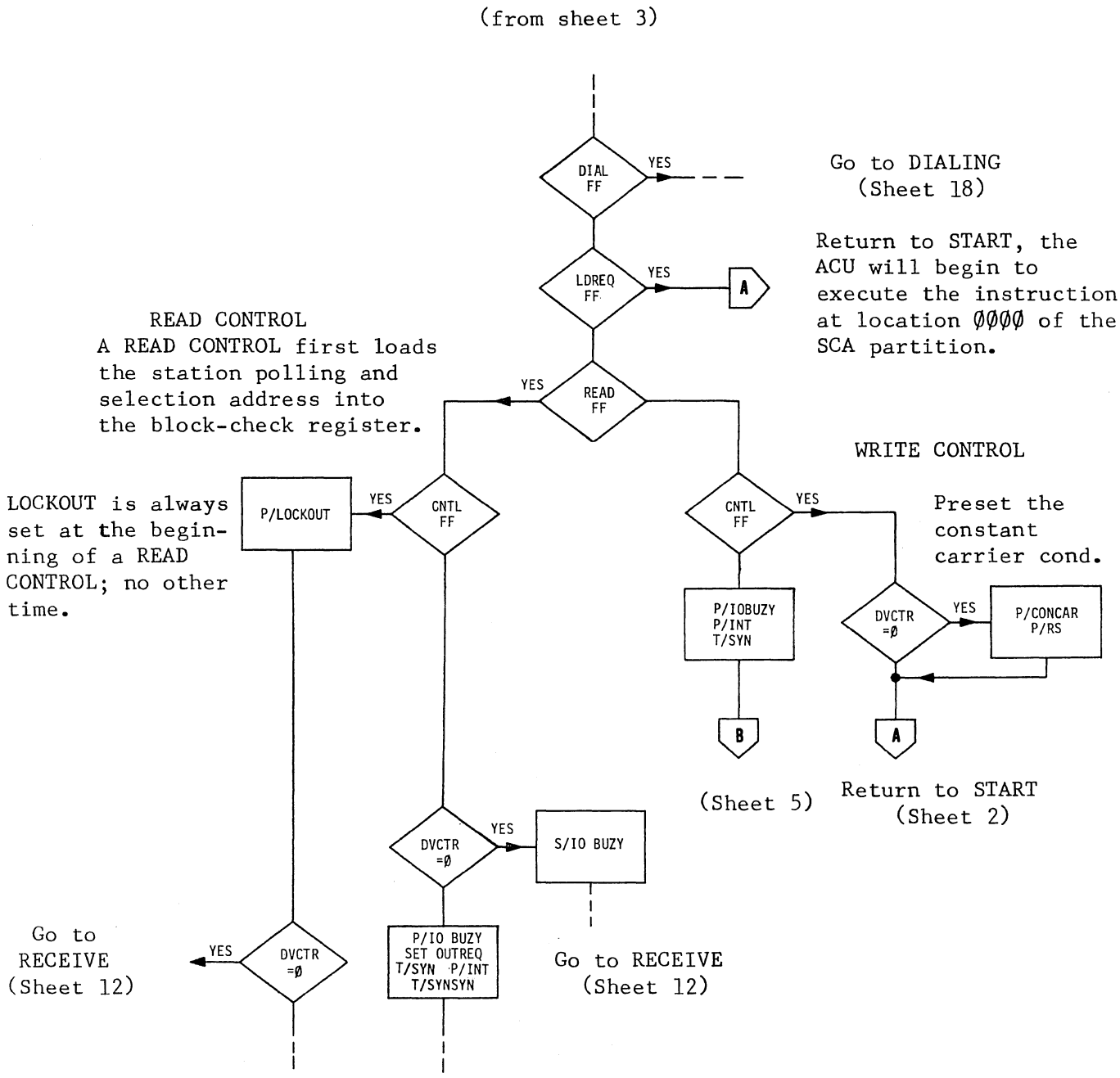


The instruction has been examined, and the proper flip-flops are set. Now a six way decision is made that will determine the basic action to be taken. An important factor in the decision, is the number that is now stored in the device counter. This number was the device number (LA) that was carried by the I/O select character.

(continued on the next sheet)

Figure 11-12 (Continued)

Sheet -3-



READ CONTROL READ/WRITE

NOTE:
A READ CONTROL operation with device number Ø will not install the station address. Consequently, the station cannot be polled or selected.

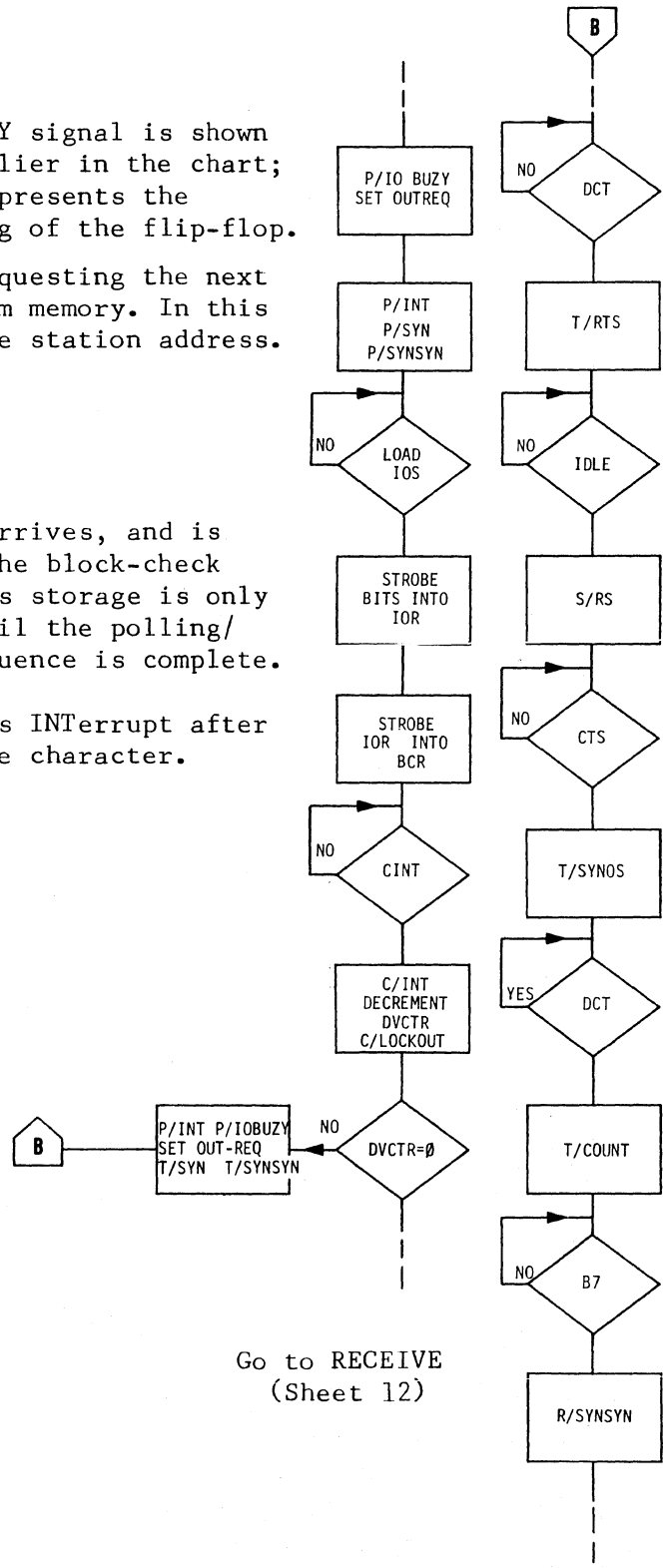
If the instruction is a READ, and the device counter is greater than zero, then control codes must be transmitted. This branch of the chart (next sheet) is preparing to transmit.

Figure 11-12 (Continued)

(Sheet 4)

(Continued from sheet 4)

READ CONTROL READ/WRITE (SEND)



The P/IO BUSY signal is shown arriving earlier in the chart; this block represents the actual setting of the flip-flop.

INT set is requesting the next character from memory. In this case it is the station address.

The address arrives, and is placed into the block-check register. This storage is only temporary until the polling/ selection sequence is complete.

The ACU clears INTerrupt after presenting the character.

DCT is a timing signal. It is SCTDLI divided by two.

Ready to send.

Wait for line to be idle.

Request to send signal to the data set.

Wait for the data set to reply with clear to send.

The SYN one-shot times out in one second, causing two SYN characters to be sent at that time.

Wait for the timing signal to disappear.

If transmission is just starting, the first SYN is being sent at this time.

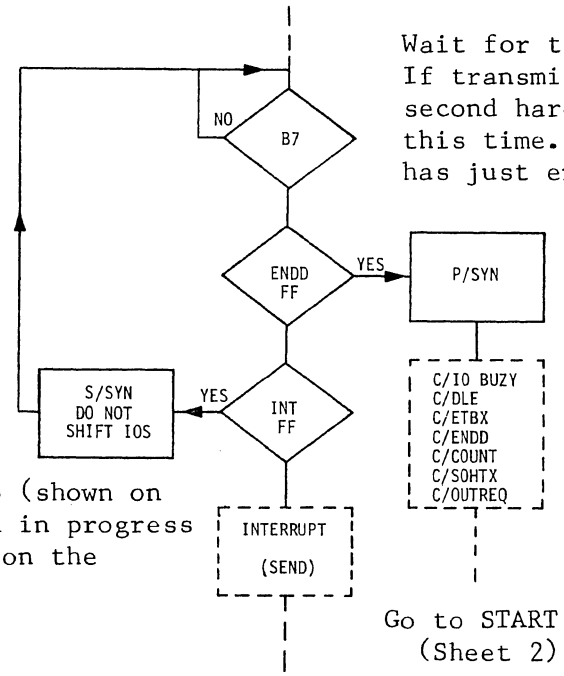
To READ/WRITE (above)

Go to RECEIVE (Sheet 12)

Go to SEND (Sheet 6)

Figure 11-12 (Continued) (Sheet 5)

SEND



Send SYNs until INT is answered.

Wait for the next B7 time. If transmission is just starting, the second hardware SYN is being sent at this time. If not, the previous character has just ended.

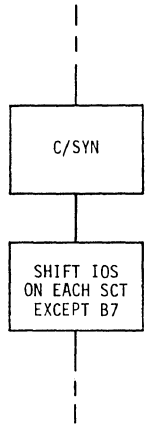
LAST sets ENDD, and if it is set, the operation is cleared.

The INTerrupt loop (shown on sheet 10) has been in progress since INT was set on the previous sheet.

Go to START (Sheet 2)

When INT is cleared, the character is ready for transmission. However, the character code is not lost, and remains in IOR (until it is replaced) even though it is strobed into IOS. Decisions are made concerning the character by examining the bits on the IOR lines.

The SYN transmission is ended. There is no longer a need for time fill, as the character is now ready to send.



D-6

Character bits are shifted out serially. Each B7 time, the shift register is loaded with the next character. Meanwhile, during the parallel shift of the character into IOS (at B7) the bit synchronism is not lost, because at that moment the character parity bit is being added by seperate circuitry.

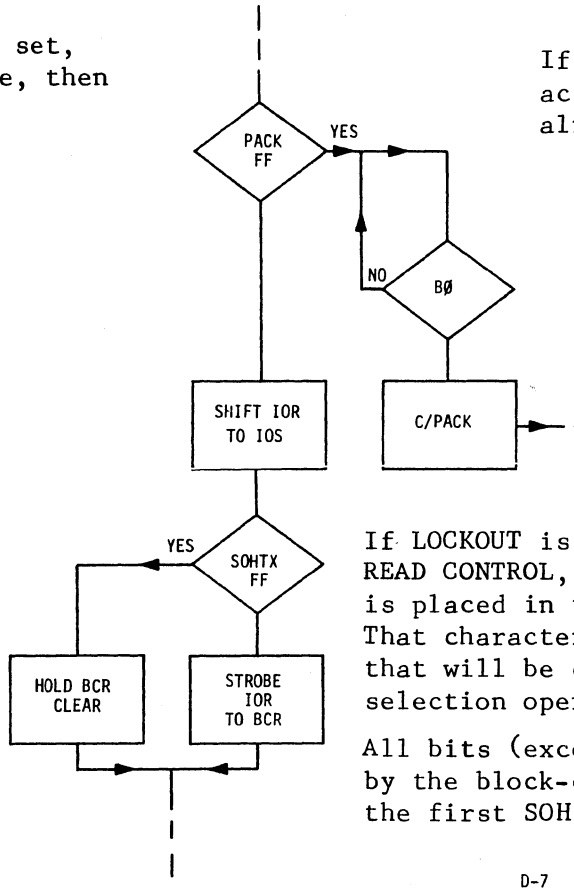
(Continued on next sheet)

Figure 11-12 (Continued)

(Sheet 6)

SEND
(Continued from sheet 6)

If the PACK flip-flop is set, wait for the next BØ time, then clear it.



If PACK is set, the character to be sent is already in IOS.

The first SOH or STX starts the block-check. The character that sets SOHTX is not part of the block-check.

If LOCKOUT is set, the operation is a READ CONTROL, and the next character is placed in the block-check register. That character is the station address that will be compared in the poll/selection operation.

All bits (except SYNs are monitored by the block-check register - after the first SOH or STX.

D-7

(Continued on next sheet)

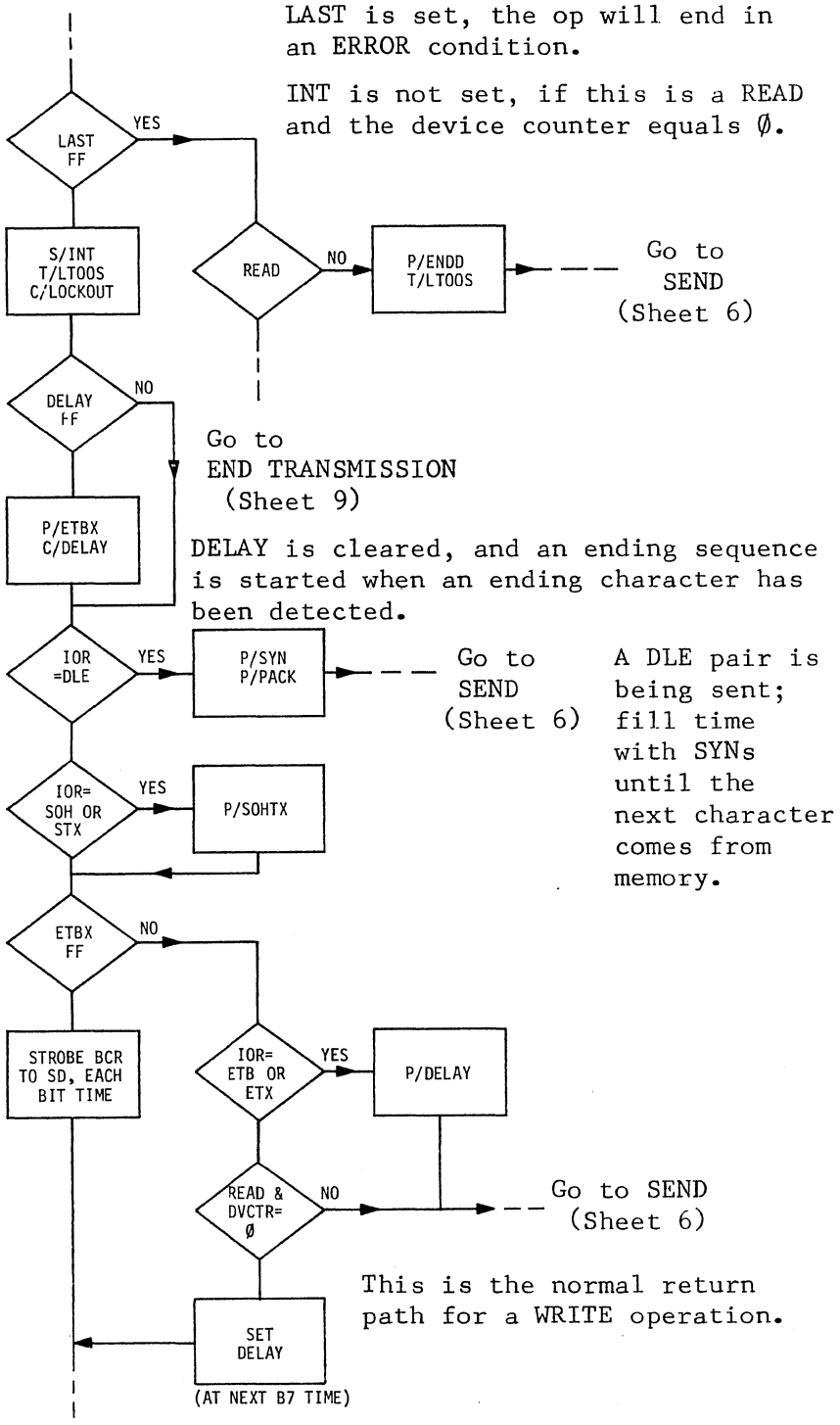
Figure 11-12 (Continued)

Sheet -7-

SEND

(Continued from sheet 7)

The last WRITE character starts a procedure for clearing the operation. ENDD is set, and at the next B7 time, SYN is set(shown on the flow chart at the beginning of SEND).
Hardware SYNs are sent while the operation is cleared, and until the next instruction arrives. The next instruction should be a READ, with a device number greater than zero. The READ will send an ETB or ETX to satisfy the BSC message ending requirements for the preceding WRITE operation.



If this is a READ operation, and LAST is set, the op will end in an ERROR condition.

INT is not set, if this is a READ and the device counter equals Ø.

DELAY is cleared, and an ending sequence is started when an ending character has been detected.

A DLE pair is being sent; fill time with SYNs until the next character comes from memory.

The SOH or STX in IOR indicates the start of the READ (receive) message, and the block-check begins.

An ETB or ETX is the BSC format ending for the preceding WRITE operation. The block-check character is automatically sent after the ending character.

This is the normal return path for a WRITE operation.

D-8

Figure 11-12 (Continued)

(Sheet 8)

END TRANSMISSION

This sequence delays the logic long enough to transmit the last character. It sends a PAD character of all 1s, and switches quickly to receive, or clears the logic, and returns to START. A READ instruction that ends because LAST is set, is in error, and the ERROR flip-flop is set.

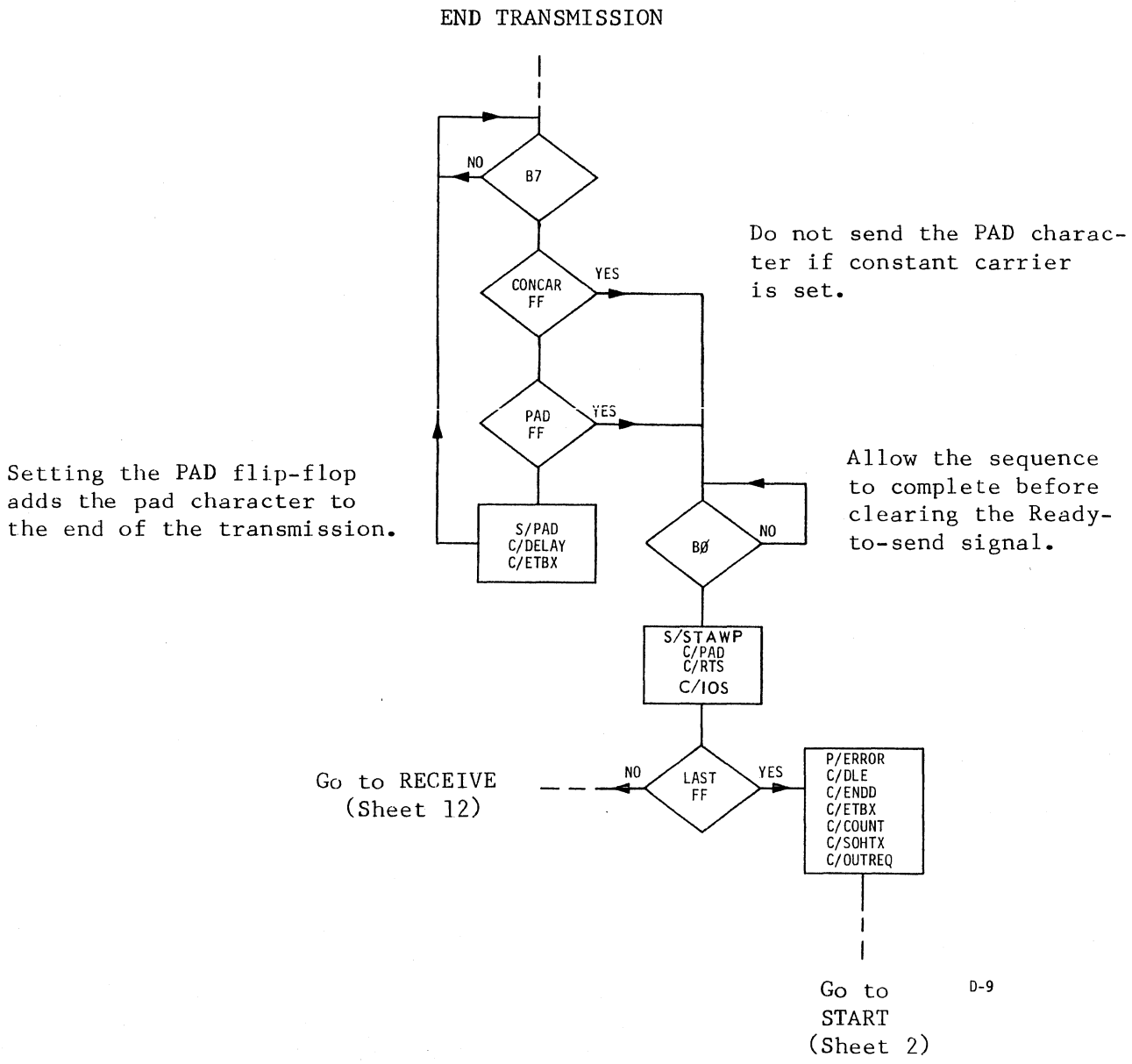


Figure 11-12 (Continued)

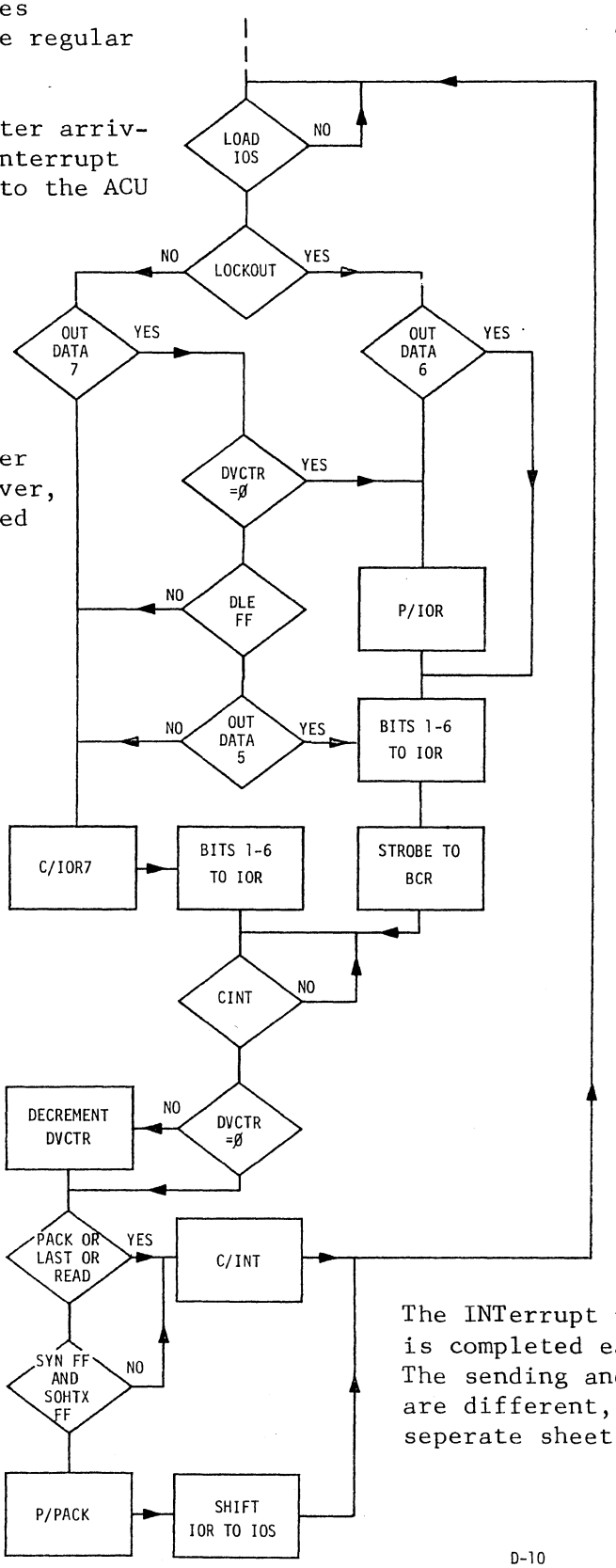
(Sheet 9)

INTERRUPT LOOP (when sending)

This sequence progresses simultaneously with the regular data flow.

LOAD IOS is the character arriving in answer to the interrupt request that was sent to the ACU by the SCA.

If the 7 bit of the character is already zero, the device counter has no influence. However, the DVCTR gets triggered with each transmission until it reaches zero.



The character is put into IOR by the ACU.

If LOCKOUT is set, the operation is READ CONTROL, in other words, polling and selecting.

Store the polling/ select address in the block-check register.

The ACU has delivered the character to the SCA, now it sends the signal to clear the INT flip-flop.

The INT flip-flop is cleared by the signal that arrived above.

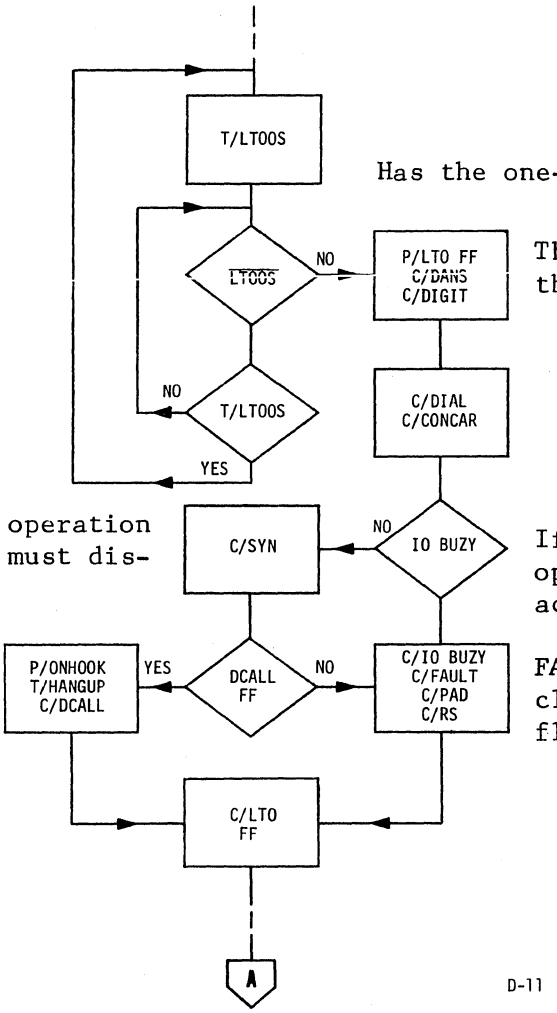
The INTerrupt process is a loop that is completed each time INT is set. The sending and receiving procedures are different, and are presented on seperate sheets of this flow chart.

D-10

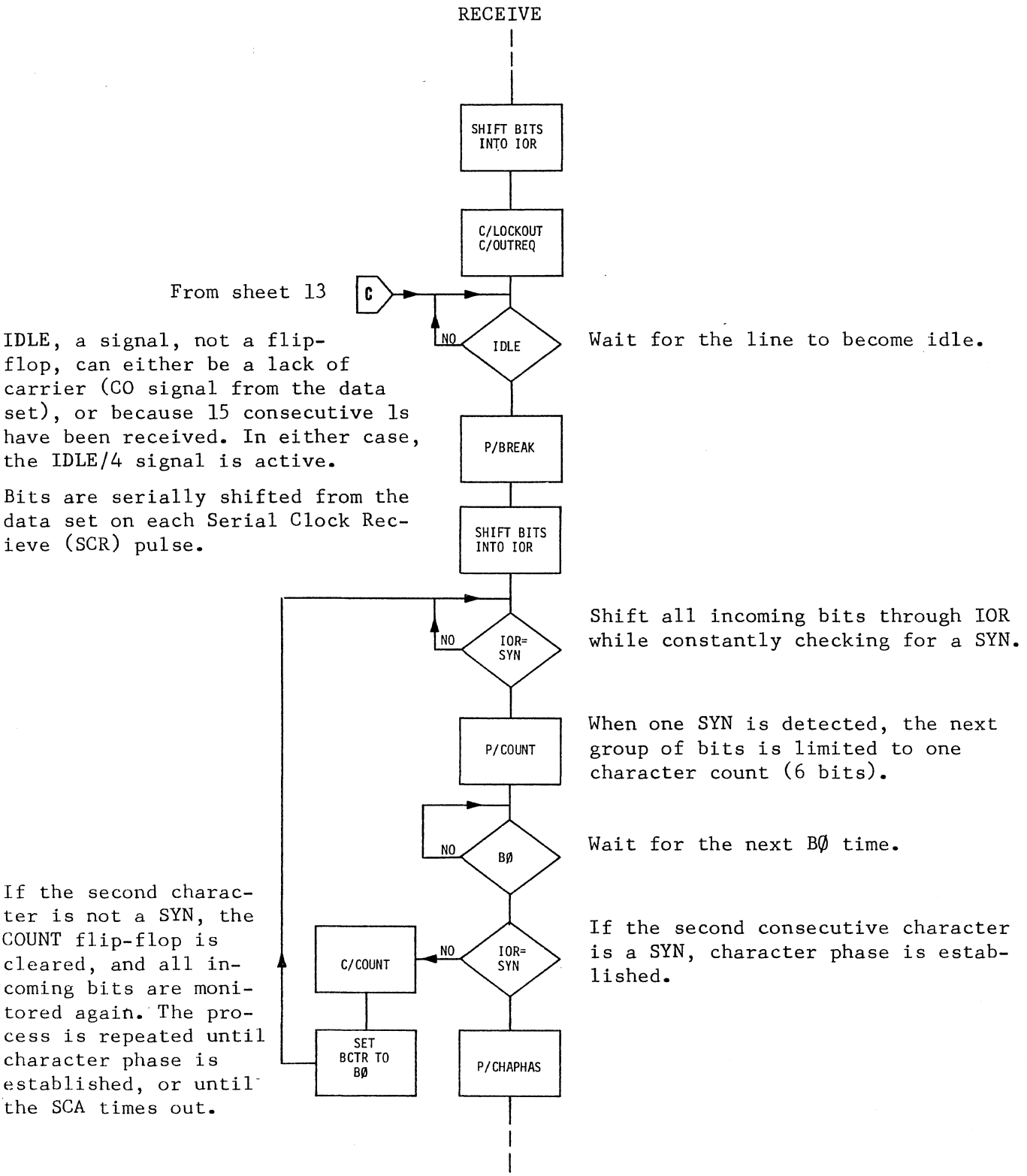
Figure 11-12 (Continued (Sheet 10)

TIMEOUT SEQUENCE

This sequence is a seperate operation within the SCA logic. The LTOOS (long time-out one-shot) is triggered at the beginning of each new instruction. If it times out (approximately 10 seconds), the operation is terminated. LTOOS is toggled for a variety of reasons, such as each time INTerrupt is set, and each time it is toggled, the 10 second time is restarted. This sequence does not cover why LTOOS is toggled, only the fact that it has, or has not been toggled. This sequence is simultaneous with other actions within the SCA, and timeout can come at any time.



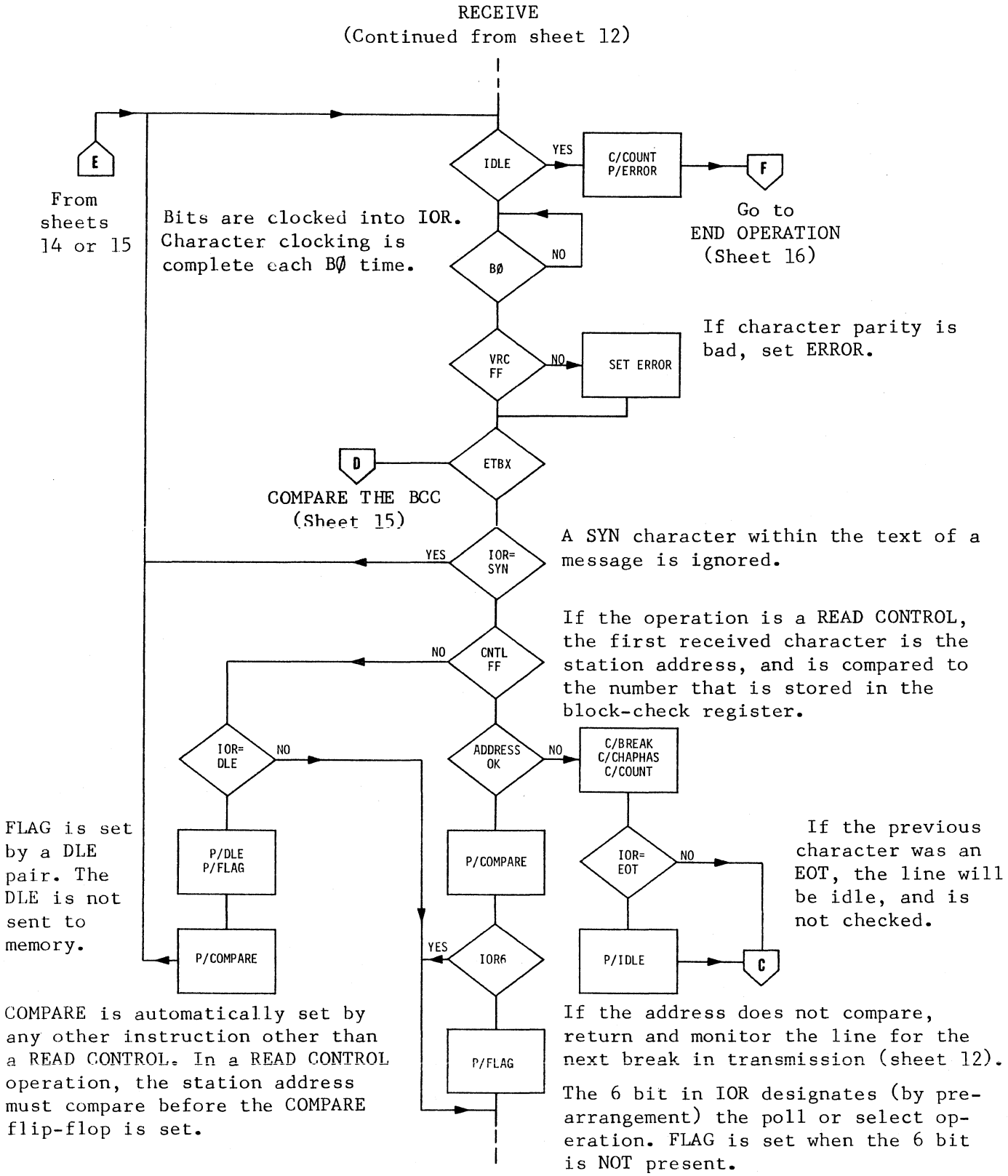
Go to START
(Sheet 2)



(Continued on next sheet)

Figure 11-12 (Continued)

(Sheet 12)



(Continued on next sheet)

Figure 11-12 (Continued) D13

(Sheet 13)

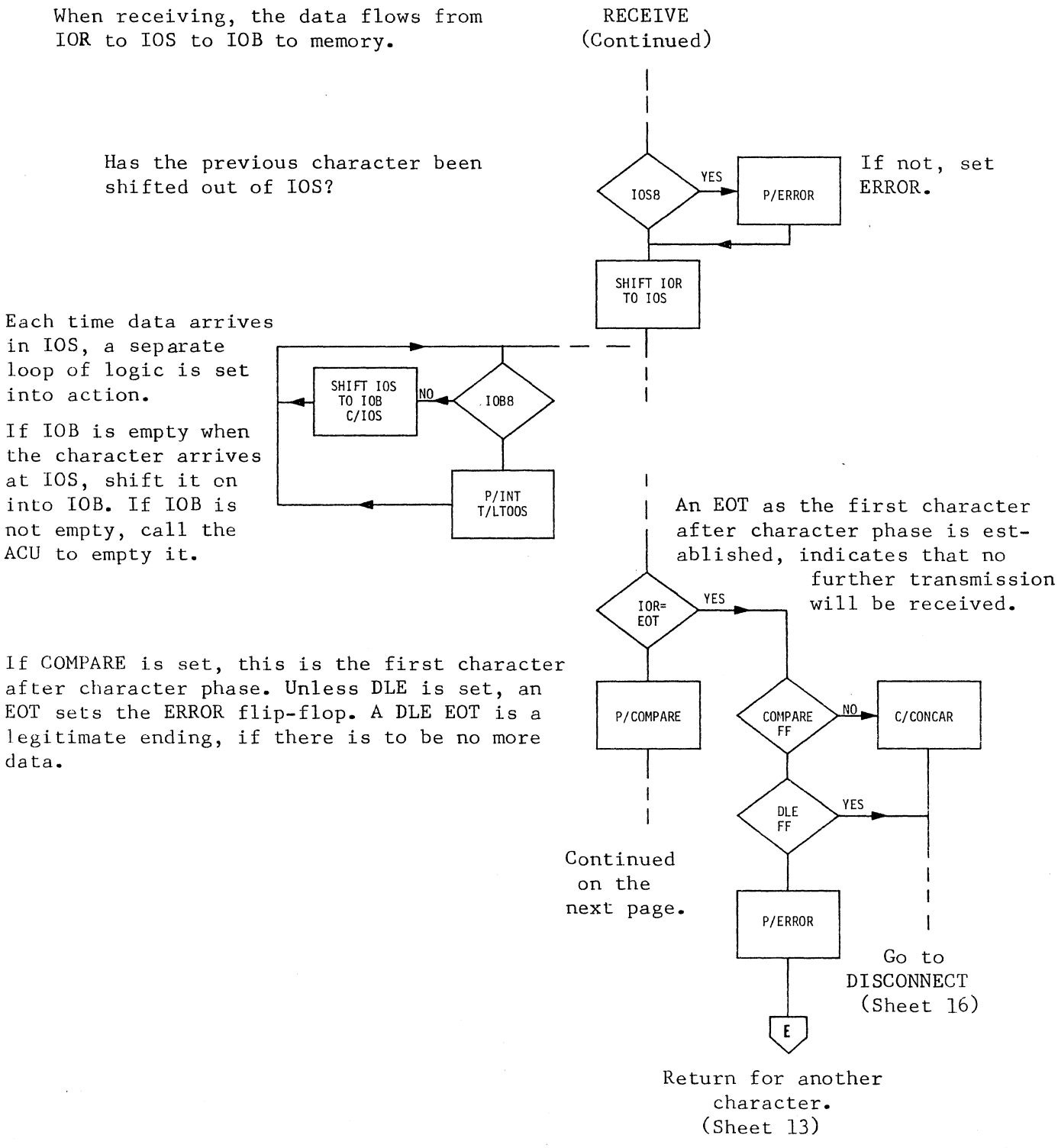
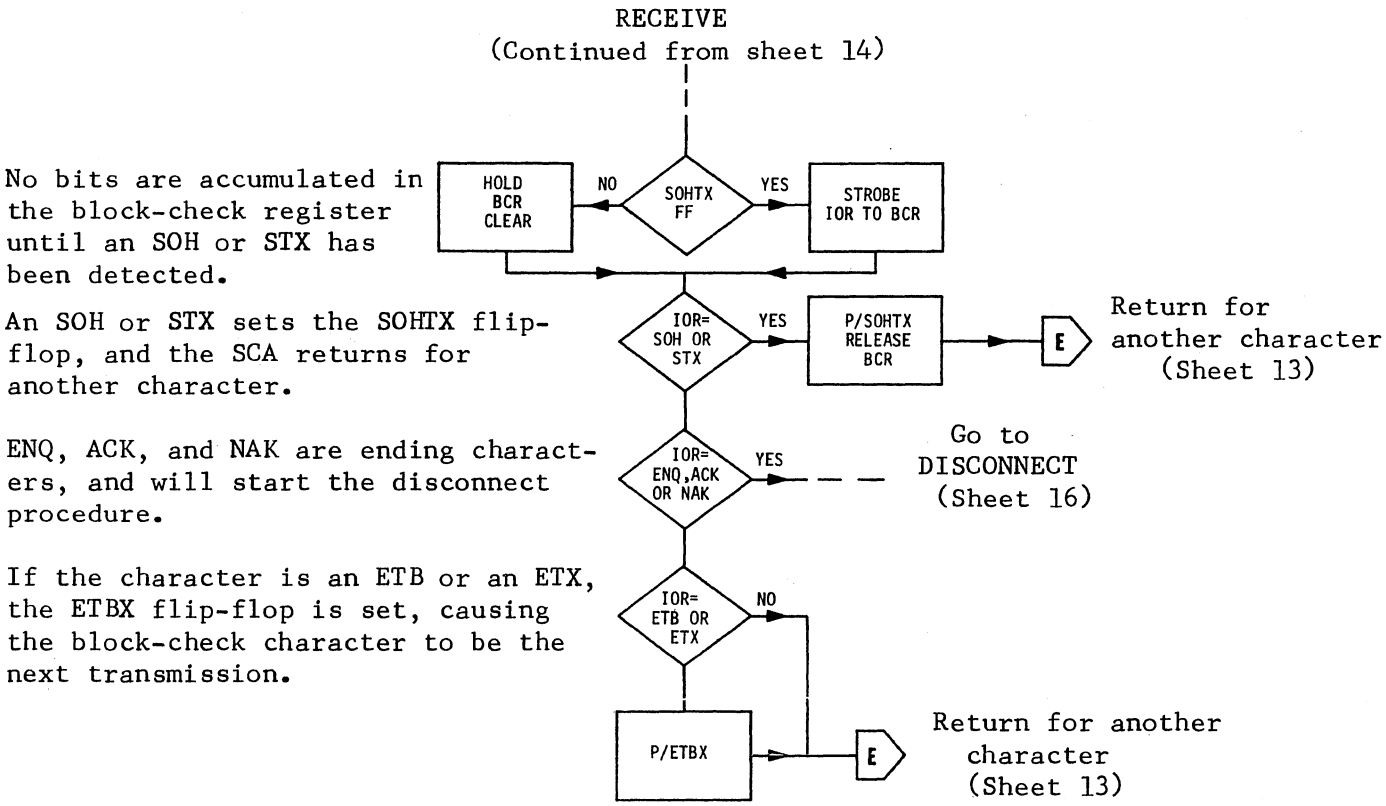


Figure 11-12 (Continued)

(Sheet 14)



A normal message ending for data is followed by the block-check character. When the BCC is received, the bits in IOR are inverted, and added to the contents of the block-check register. If the sum of the addition is zero, the check is O.K., but if not, ERROR is set.

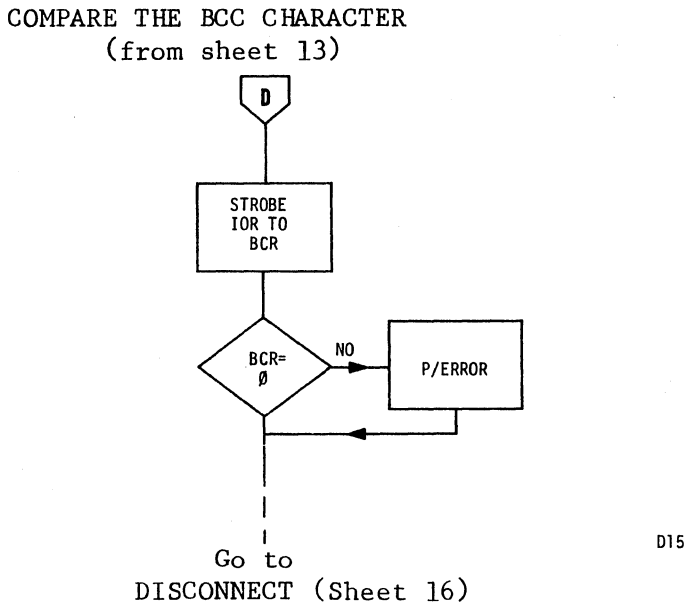


Figure 11-12 (Continued)

(Sheet 15)

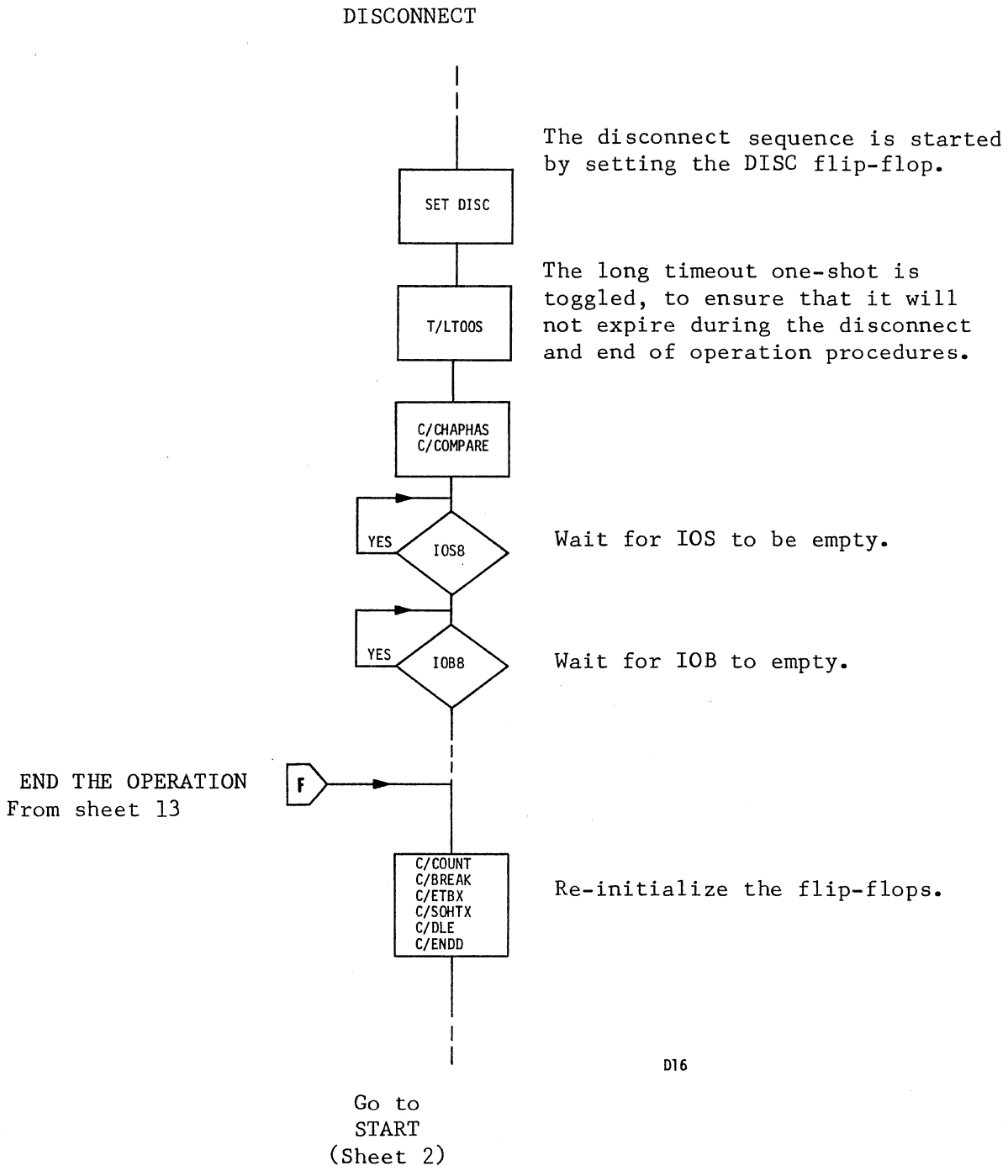
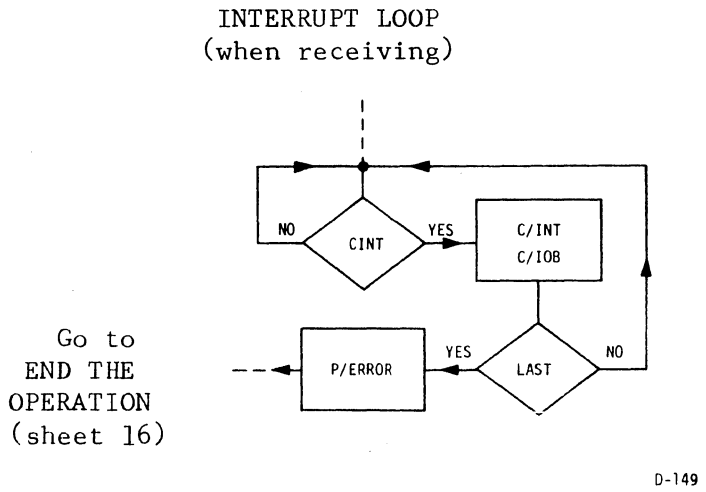


Figure 11-12 (Continued)

(Sheet 16)

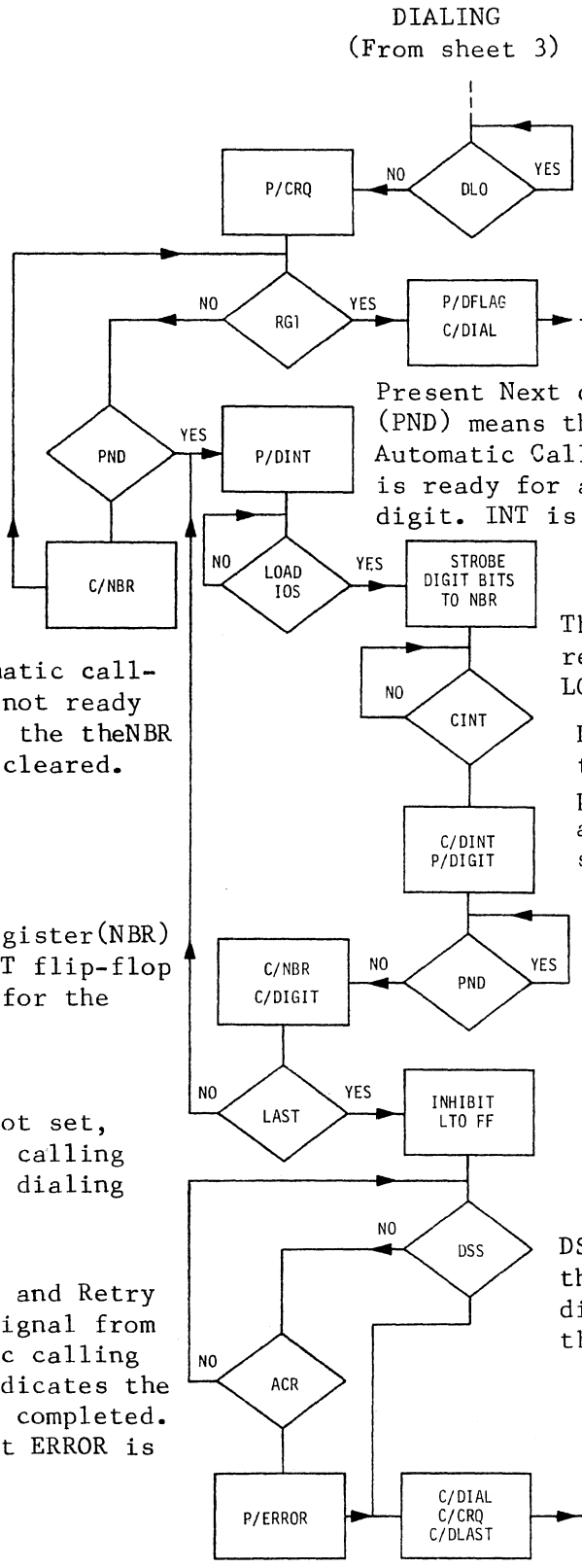


When the Clear Interrupt signal arrives, it indicates that the processor has taken the character. The INT flip-flop is reset, and the IOB register is cleared. After each character is received, LAST is checked. If LAST is found set during receive, the ERROR flip-flop is preset, and the operation is ended. If LAST is not set, the INT sequence starts again for the next character.

The interrupt loop, when receiving, is a simple sequence that is completed while receiving each character. The CINT signal, shown in the illustration above, corresponds to the same logic box on sheet 5 in the RECEIVE branch of the logic flow chart.

Figure 11-12 (Continued)

(Sheet 17)



Data Link Occupied (DLO) is a signal from the Automatic Calling Unit. DLO will also be present if the calling unit is in the "test" mode.

Call Request (CRQ) is preset, informing the calling unit that a call must be made.

RG1 is from the data set, indicating that a call is coming in (ringing). If ringing is present, the incoming call has priority, and Dial Flag is set, and the operation is canceled.

Present Next digit (PND) means that the Automatic Calling Unit is ready for a dialing digit. INT is set.

If the automatic calling unit is not ready for a digit, the theNBR register is cleared.

The dialing digit is strobed into the register (NBR) by the processor signal LOAD IOS.

Dial Interrupt, DINT, is cleared by the processor after the digit is placed in NBR. DIGIT is set, which activates the Digit Present (DPR) signal to the Automatic Calling Unit.

The digit register(NBR) and the DIGIT flip-flop are cleared for the next digit.

The dialing digit is accepted by the dialing unit, and PND is lowered.

If LAST is not set, DINT is set, calling for the next dialing digit.

When the last digit has been accepted, the SCA timeout is held, preventing timeout until the call is answered (which may be as much as 40 seconds, according to the calling unit settings).

DSS is active when the data set is in the data mode. This means that the dialing sequence is completed, and the call is answered.

Abandon Call and Retry (ACR) is a signal from the automatic calling unit that indicates the call was not completed. In that event ERROR is set.

Whether the call is completed, or abandon, the logic is cleared for the next dialing operation.

Figure 11-12 (Continued)

(Sheet 18)

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11-5.10 STATUS

FAULT, ERROR, and FLAG status can be set by the SCA. The conditions for setting each of these is listed below

FAULT

- Timeout from ten seconds of attempted data transmission without a character transfer.
- Timeout from ten seconds of SYNs between op codes.
- Timeout from ten seconds of reception without character phase.
- No power to the data set (data set is inoperative).
- No power to the Automatic Calling Unit (Unit is inoperative).

ERROR

- Receive mode is terminated by LAST.
- A character is received with the buffers full, and cannot be forwarded to the processor before the next character arrives.
- Data loss on the line - either loss of carrier, or 15 consecutive 1s.
- Parity error on any received character.
- EOT code within the text of a message.
- Block-check character does not compare.
- ACR (Abandon Call and Retry) signal from the Automatic Calling Unit - no answer, or the wrong party answered.

FLAG

- The completed operation was a READ CONTROL with no 6 bit in the address. This is only true if the station address compared.
- A DLE is detected during a READ operation.
- The completed operation was a WRITE CONTROL and a call was received as the processor was initiating a call, but before the telephone equipment latched. The processor op is terminated by the incoming call.

11-5.11 TIMING

Basic timing for the SCA is supplied by the IOC-MF-CLK signal from the ACU. The 300kHz frequency is used directly when transmitting, and divided by two when receiving. Character timing is supplied by signals from the data set. The end result is a series of relatively short timing pulses around each transition of the data set timing signal. Figure 11-13 shows the major timing involved when transmitting, and receiving. Signal names are composites, such as SCTDN7CS. This signal is the serial clock transmit naught (low going) at B7 time after the clear to send.

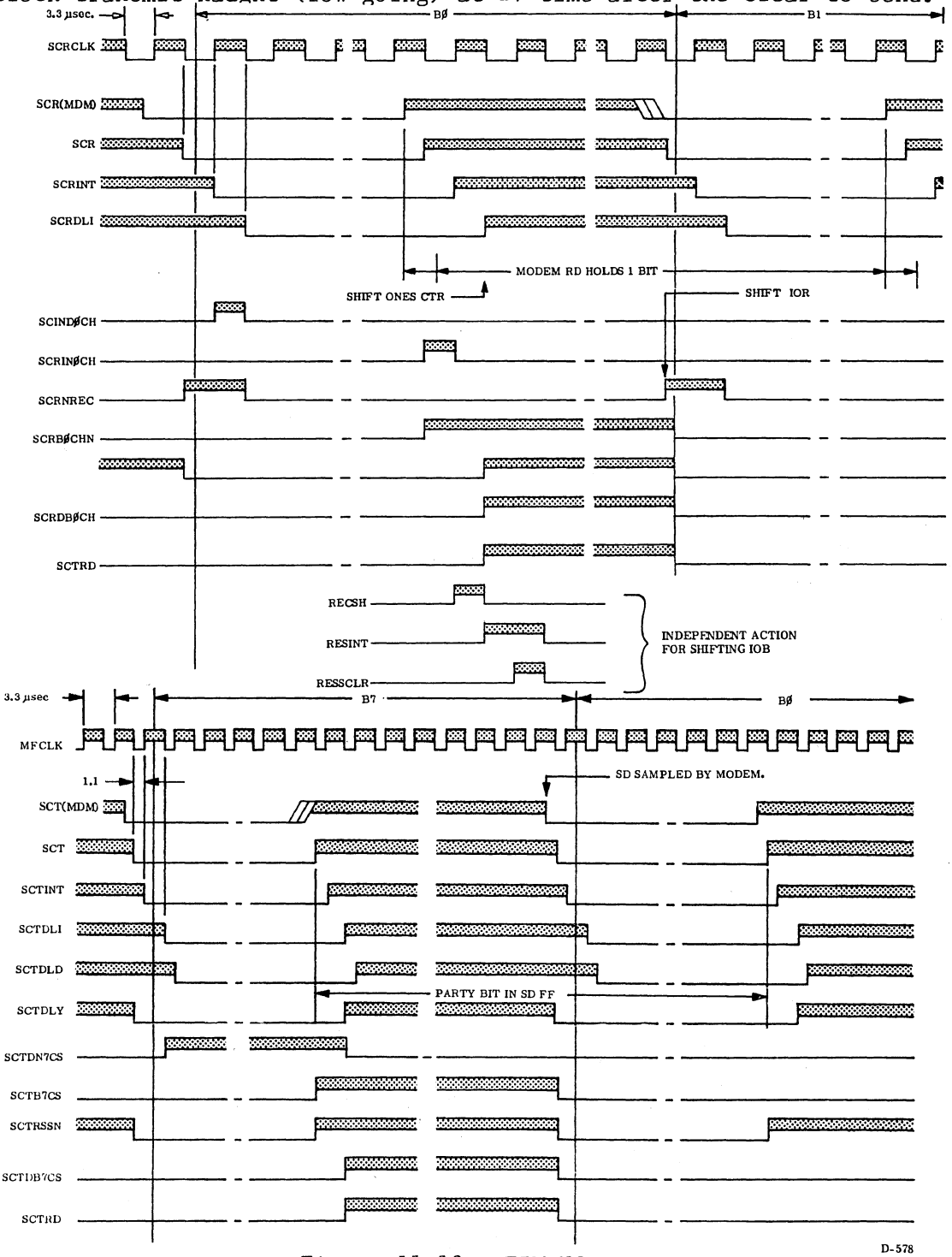


Figure 11-13. TIMING

11-6.0 REFERENCE

11-6.1 SUMMARY OF SCA FUNCTIONS

READ

A READ instruction issued to the SCA can:

- Receive non-control data characters.
- Transmit control characters (a maximum of nine per instruction), then -
- After transmitting control characters, receive non- control characters.

WRITE

A WRITE instruction to the sca can:

- Transmit data chatacters.
- Transmit control characters (up to nine), then -
- After transmitting control characters, transmit non-control data.

READ CONTROL

Used in a multi-station environment to:

- Store, then listen for a unique station address during polling/selection.
- Store, then listen for a station address, then transmit up to nine control characters.

WRITE CONTROL

Causes the SCA to:

- Hang up (disconnect fron the dial system).
- Send dialing digits to the Automatic Calling Unit.
- Set a constant carrier condition.

SOH or STX

Start an accumulation of the block-check. The bits of the first SOH or STX are not included in the block-check.

ETB orETX

Ends the block-check accumulation. The bits of the ETB or ETX character are included in the block-check.

EOT

Encountering an EOT character will:

- Set ERROR if the EOT is within a received message.
- Terminate a READ instruction, if the EOT is the first character after character phase is established.
- Force a "break" condition under a READ CONTROL instruction.
- A DLE EOT combination is a legitimate ending at any time, however, the DLE will set FLAG status.

11-6.1 SUMMARY OF SCA FUNCTIONS (Continued)

ENQ, ACK, or NAK

Any of these codes terminate a READ operation, if the SCA is in the receive mode.

DLE

When transmitted, it causes a "packing" operation, to ensure that the DLE and the character that follows are sent back-to-back.

When receiving a DLE sets FLAG status, and ends the READ operation at the end of the next character. A DLE received during a READ operation is not transfered to memory.

SYN

SYN codes are not transfered to memory while the SCA is in the receive mode.

Two SYN codes are automatically transmitted by the hardware at the beginning of each transmitting operation.

SYN codes are transmitted continuously following a WRITE operation. The message is terminated by the first portion of the following instruction.

An automatic SYN is injected if the character to be transmitted is delayed (from the processor).

Two SYN codes are inserted into transmitted messages at one-second intervals.

One hardware SYN is transmitted at the beginning of the "packing" operation.

11-6.2 MANUAL CONTROLS

Figure 11-14 shows the external connections from the SCA to the data set, and the automatic calling unit. The interconnect cable between CH5 and CH8 must always be connected, whether the automatic dialing is used, or not. Patching connections are listed below.

CONTINOUS CARRIER operation - connect TP7 and TP8 on CH5.

INHIBIT TIMEOUT (inhibits SCA only) - TP3 and TP4 on CH5.

PRIVELEGED CHANNEL - TP5 and TP6 on CH5.

PARTITION SIZE - see figure 11-14.

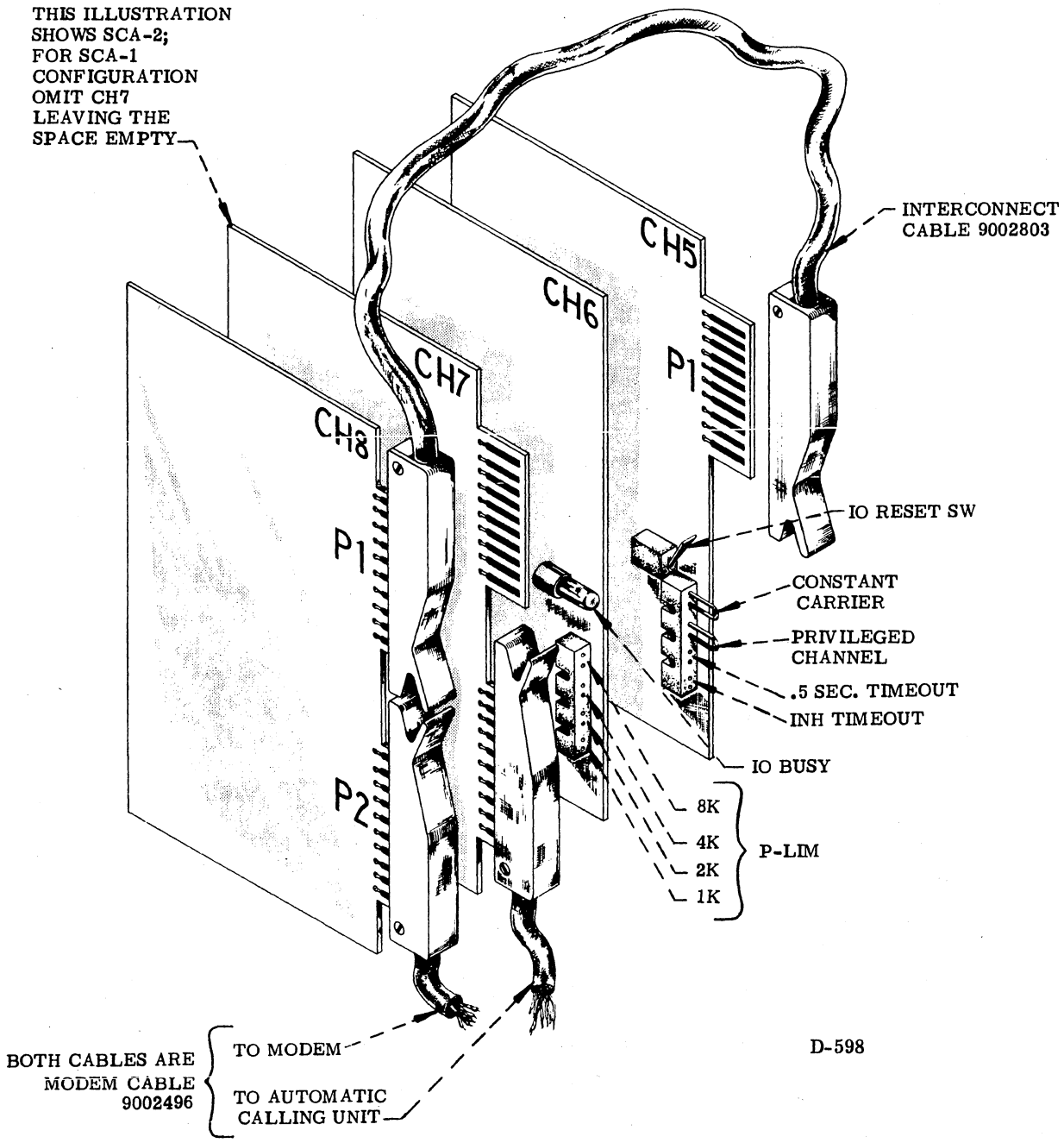


Figure 11-14. EXTERNAL CONNECTIONS

11-6.3 LCO

The Local Communications Option (LCO) is a single card wiring assembly, for use with the SCA, to communicate without data sets to another computer within a short distance (50 cable feet). The second computer can be another model 20, or any other binary synchronous device that uses a standard RS-232B interface (see figure 11-15).

The LCO resides in the odd numbered card position that would ordinarily contain the CH7 card. Because the dial out option is not needed in a local communication situation, the CH7 card is not used, leaving the slot open for the LCO. The LCO simulates the buffering, time delay, and synchronized timing pulses that are normally associated with the data set interface.

Connection from the second computer to the LCO is made through a jumper cable (9004292) from P1 (the upper connection) on the LCO card. The remote end of this cable mates with the other processors data set cable. A second cable (9002803) connects the lower connection (P2) on the LCO to P2 (the lower connection) on CH8. This is the connection on CH8 that would normally connect to the data set.

SCA TEST CONFIGURATION

The LCO can also be used in a local situation for testing and/or verifying SCA operation. When the LCO is used for this purpose, another SCA is temporarily installed in an unused I/O position within the same processor mainframe. The LCO is placed where the CH7 card would normally be. Connection is made from P2, on CH8 (the lower connector) of each SCA to the edge connectors on the LCO card. The option of which SCA connects to P1 or P2 of the LCO is not important, as the circuits are identical. The connections from both SCAs are made through standard 9002803 cable assemblies. Figure 11-16 shows the LCO in both the test configuration and the communications configuration.

LCO OPERATION

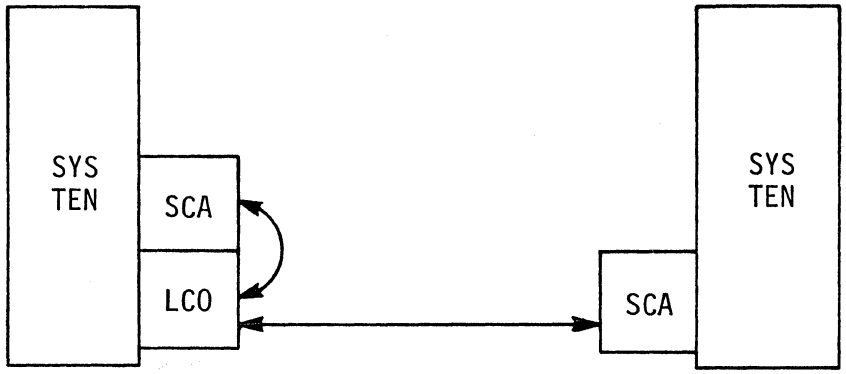
The LCO operates at speeds of 300, 600, 1200, 2400, 4800, and 9600 bits per second. Speed is manually selected by placing a jumper wire in the terminal block position that is labeled with the desired speed.

LCO LOGIC

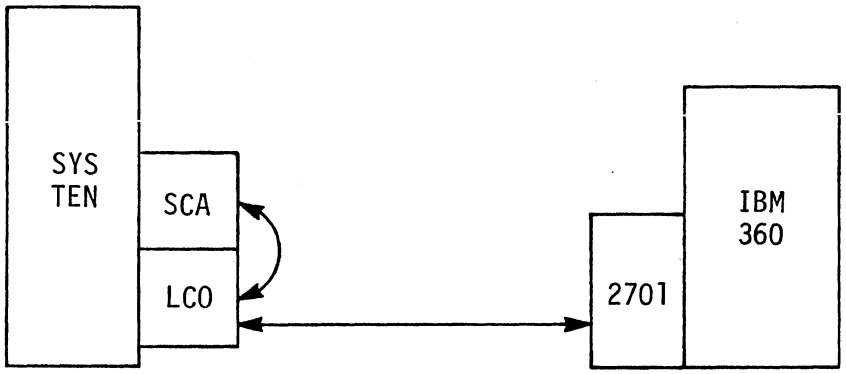
Data set interface signals are received by the LCO, delayed, and used to propigate the coresponding data set signal at the output. For example, the RS (Request to Send) signal is brought to the qualification side of a D flip-flop. When the proper clocking signal (SCT) is received from the internal LCO logic, the flip-flop sets, creating the CTS (Clear To Send) signal which is amplified and returned to the requesting unit. Synchronization and internal clocking is maintained by a crystal controlled oscilator within the LCO. The basic oscilator frequency is divided by a series of D flip-flops, and both the SCT (Serial Clock Transmit) and SCR (Serial Clock Receive) signals are derived from this source.

Data is steped serially through a shift register (one for each direction) that acts as a time delay and buffer. The time delay is approximately seven and one half bit times. The delay in milliseconds will depend upon the speed setting.

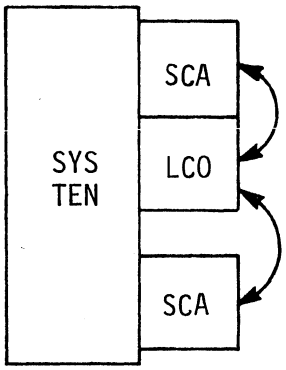
Figure 11-17 shows a simplified block diagram of the LCO, and the internal timing.



SYSTEM TEN-TO- SYSTEM TEN



SYSTEM TEN-TO- FOREIGN SYSTEM

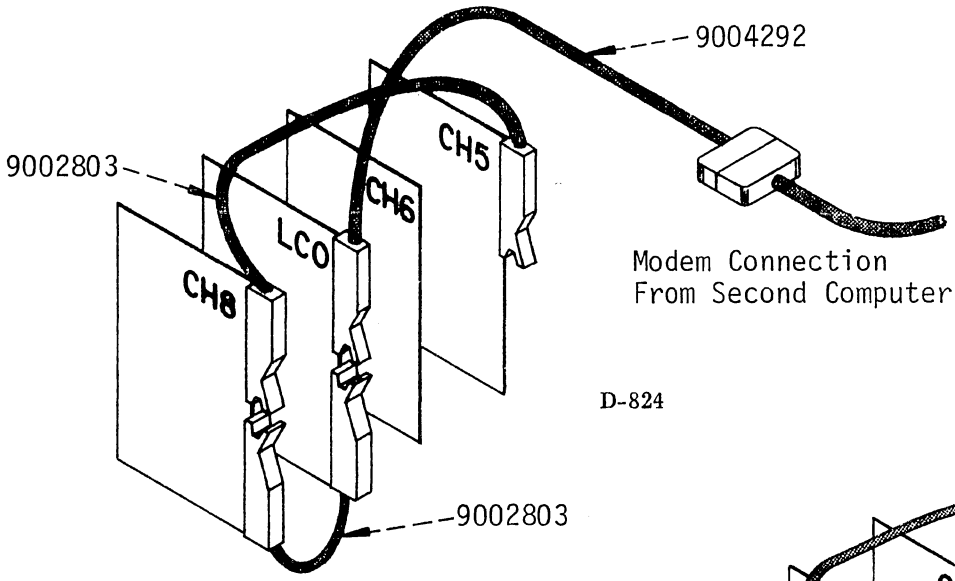


SYSTEM TEN
LOCAL SCA TEST

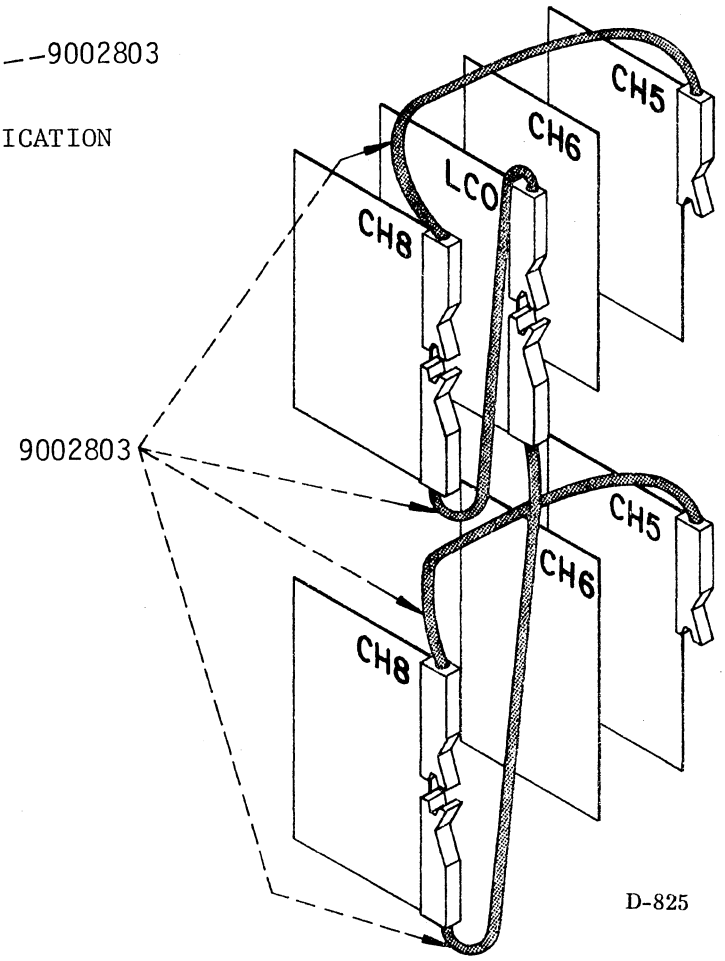
D-852

Figure 11-15. LCO CONFIGURATIONS

SYNCHRONOUS COMMUNICATIONS ADAPTER

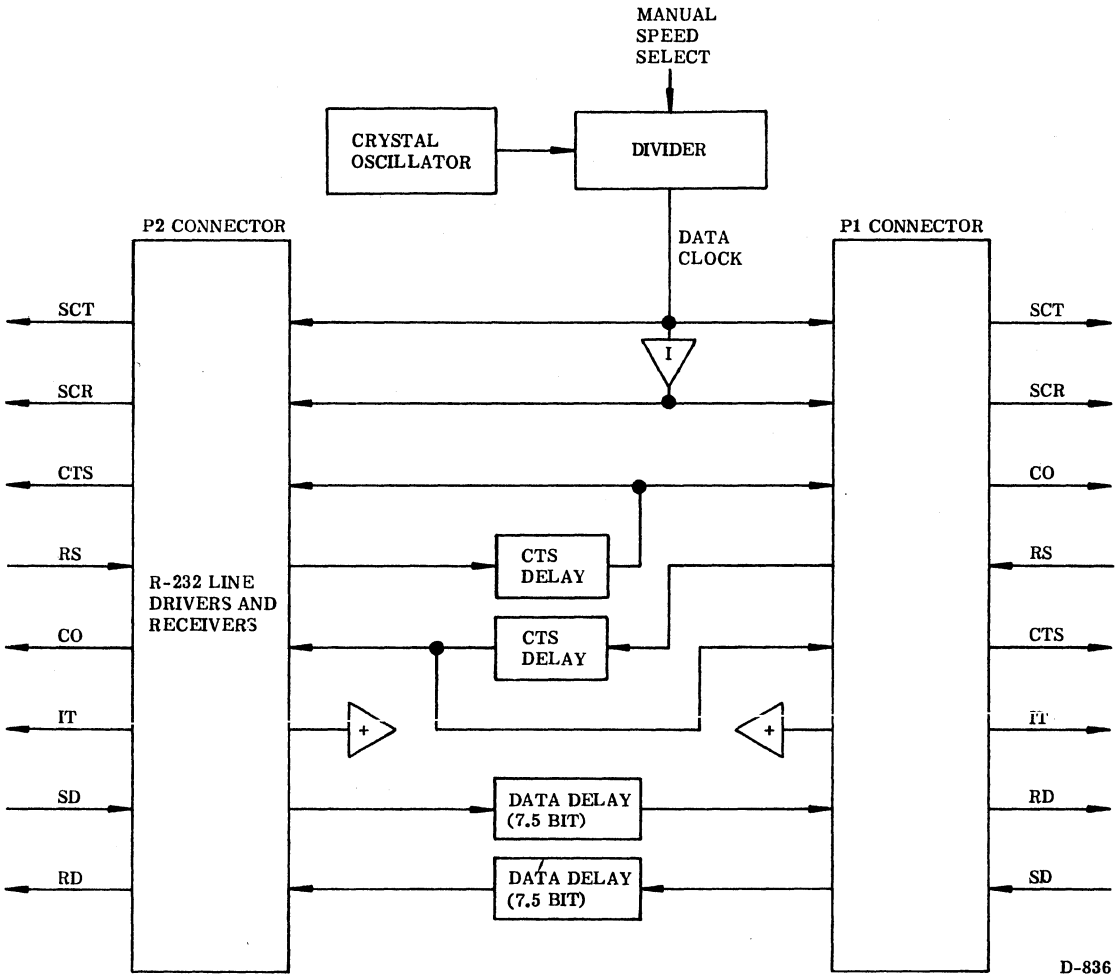


COMMUNICATION APPLICATION



SCA TO SCA TEST
CONFIGURATION

Figure 11-16. LCO CONNECTIONS



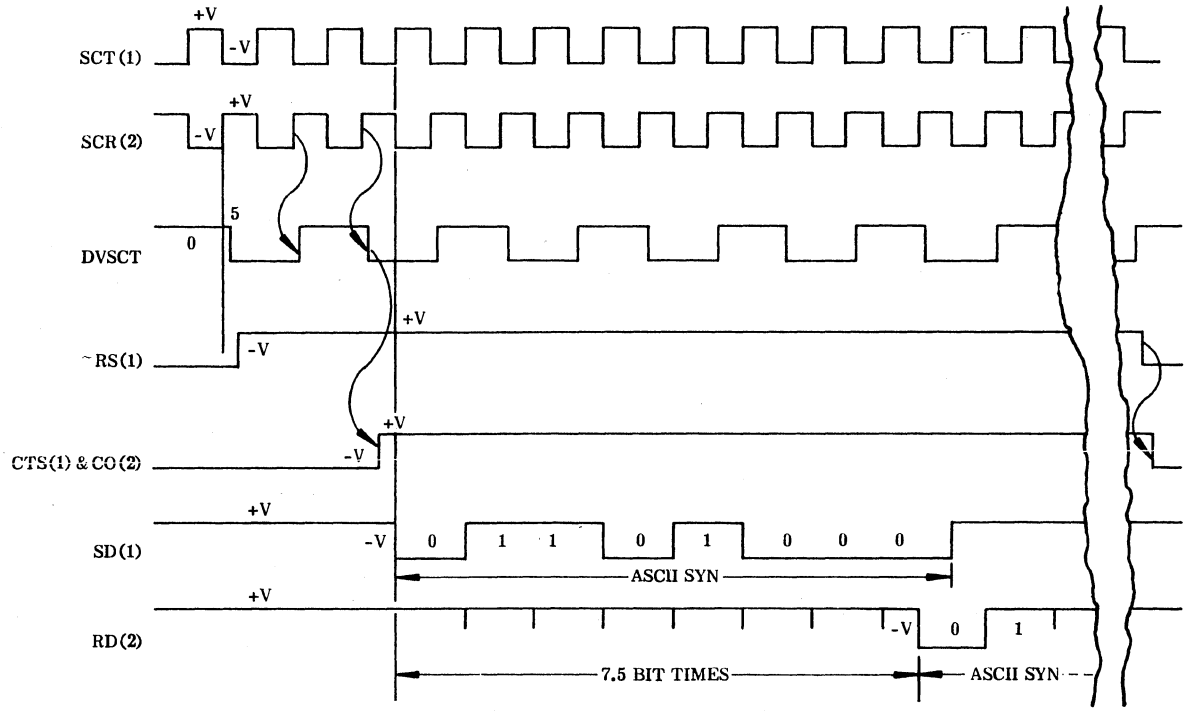


Figure 11-17. LCO BLOCK DIAGRAM

11-6.4 GLOSSARY

NAME	TYPE	SOURCE	DEFINITION
ACR	SIG.	MODEM	Abandon Call and Retry - Indicates to the SCA that dialing has not been completed in the desired time. This timeout is adjustable on the calling unit from 7 to 40 seconds. When interfacing with the SCA, the automatic calling unit must contain the "Y" option. If it does not, the ACR signal will appear each time dialing is attempted. The ACR signal sets ERROR in the SCA.
ACU	—	—	Arithmetic Control Unit - Part of processor.
A.C.U.	—	—	Automatic Calling Unit (Telephone Co. name for their dialing unit).
BCRT1 BCRT2	CNTR	CH6	Provides a short pulse for triggering the BCR after delay from initiating pulse.
BCR1 through BCR7	FF	CH6	Individual JK FFs to create, and check, block-check character. Also used to store selection address.
BCTR	SHREG	CH6	Block-check register.
BREAK	FF	CH5	Loss of carrier, or receive 15 consecutive one bits .
CHARACTER PHASE	—	—	Synchronism of characters between transmitter and receiver. Caused by receiving 2 SYN's.
CHECK	FF	CH5	Indicates Program Error; is set by ACU.
CHPHAS	FF	CH5	Character Phase - recognizes and remembers that character phase has occurred.
CNTR	FF	CH6	Control detection, either READ CONTROL or WRITE CONTROL.
CO	SIG.	MODEM	Carrier On-Off - When no carrier is present, this lead will be negative. The lead will become positive within 9ms of the time that a carrier signal is received (from the distant station).
COMPARE	FF	CH5	Used to pull first character and check for READ CONTROL. Favorable address compare.

NAME	TYPE	SOURCE	DEFINITION
CONCAR	FF	CH5	Constant Carrier - Set by software. Holds RS FF for constant carrier operation.
CONSTANT CARRIER	—	— s	Either a full-duplex system, with data flow in two directions simultaneously (not used by the SCA), or a half-duplex system, where the transmitter pads with all 1's onto the line while receiving on the other side of the line. A constant carrier system must have four wires and only two stations.
COUNT	FF	CH5	Allows only 8 bits to enter IOR at any one time.
CRQ	XLATCH	CH7	Call Request - Activated by the SCA when initiating a dialing procedure.
CTS	SIG.	MODEM	Clear To Send - Has a negative potential at all times when the data set (modem) is active, but not transmitting. A positive potential appears on the CTS line approximately 150ms after a positive potential is applied to the RS lead. The delay is allowed for echo suppression, and to allow the distant receiver to establish synchronization. In special cases, where a very short two-wire line is used, the 150ms time delay can be shortened to about 8 1/2 ms.
DCT	SIG.	MODEM	Dibit Clock Transmit - A square wave signal from the modem for synchronization at the dibit (character bit) rate.
DLO	SIG.	MODEM	Data Line Occupied- Reports to the SCA that the communication line (telephone or leased) is busy. The calling unit will ignore a request for service (CQR) if the line is busy. The DLO line is also active if the calling unit is in the test mode.
DPR	SIG.	CH7	Digit Present - Signal from the SCA indicating that a number has been presented to the calling unit on the digit leads.
DSS	SIG.	DIAL-ING UNIT	Data Set Status - The automatic calling unit activates this lead to report that the data set (modem) is in the data mode.
DCALL	XLATCH		Turns ON remote control (RC) signal to modem indicating incoming call is being answered by the SCA, or that a call is being initiated by the SCA.

NAME	TYPE	SOURCE	DEFINITION
DELAY	FF	CH5	Adds one period of time between receipt of terminating code and completion of transmission.
DERROR	XLATCH	CH7	Records ERROR status for dial out operation.
DFLAG	XLATCH	CH7	Records FLAG status for dial out operation.
DIAL	FF	CH7	Equivalent to IO-BUSY for dial out operation.
DIGIT	XLATCH	CH7	Used to hold digit present (DPR) signal to modem.
DINT	FF	CH7	Equivalent to INTerrupt for dial out operation.
DISC	FF	CH5	Delays clear of IO BUSY while processor takes last character (through INTerrupt) "Disconnect".
DLAST	XLATCH	CH7	Equivalent to LAST for dial out operation.
DLE	FF	CH5	Detects DLE.
EOTIDLE	FF	CH8	Presets fifteen ones into the ones counter when an EOT code is received during a polling operation. Forces a BREAK condition for immediate resynchronization after the EOT code.
ENDD	FF	CH5	Set by LAST - character count is exhausted. Delays logic to allow complete transmission.
ERROR	FF	CH5	Set if: Read op is ended by LAST, bad parity (VRC or LRC), aborted dialing sequence, EOT within message, data loss on line, or character can not be passed to ACU.
ETBX	FF	CH5	Indicates end of text, or end of block. Causes block check character to be sent.
FAULT	XLATCH	CH5	Cross latch for status. - Set on SCA time-out, or if modem or dialing unit is without power.
FLAG	FF	CH6	Set when a DLE is received, or if dialing is interruped by an incomming call, or in a multi-station environment to indicate poll or select.
FULL DUPLEX	—	—	A system where Data transmission is in two directions simultaneously. A full-duplex system is also constant carrier, and requires four wires. The SCA cannot operate full duplex.
HALF DUPLEX	—	—	A system where the data transmission must cease in one direction before starting in the other direction. Can be two-wire, or four wire (for faster "turn around").

NAME	TYPE	SOURCE	DEFINITION
HANG UP	ONE SHOT	CH8	Disconnect from line signal. Opens RC lead to modem, and keeps SCA channel busy for 150 ms.
IO BUZY	FF	CH5	Set when the SCA is in an actual operation.
IOS	SHREG	CH6	Shift Register.
IT	SIG.	MODEM	Interlock - This lead is at a positive 6 volts when the data set is prepared to send or receive data. When the lead returns to zero volts, the data set is inoperative.
LAST	XLATCH	CH5	Set by processor for last (final) character.
LDREQ	XLATCH	CH5	Load Request.
LOKOUT	FF	CH5	Preset when starting READ CONTROL (used to get polling and selection address from memory to register). Prevents transmission of first character.
LTOFF	FF	CH5	Late Timeout Flip-Flop - Timeout generator, provides 3.3 μsec pulse for LTD signal.
LTOOS	ONE SHOT	CH5	Late Timeout One Shot - Drive LTOFF. Provides a ten second timeout.
MODEM	—	—	Unit for converting binary data to tone modulations for transmission on telephone lines. Accepts two bits before transmitting either, then sends both. Modem is abbreviation for Modulator/Demodulator.
NB1 through NB8	XLATCH	CH7	Digit Leads - A four-bit binary representation of the dialing digit from the SCA. The leads represent the binary value of the number; NB1 is a binary one, NB8 is a binary eight, etc.
ON HOOK	FF	CH8	Provides an automatic hangup of the dial connection if Late Time Out occurs during a period when the SCA is not performing an I/O operation.
ONES CTR	FFs	CH8	Counts 15 ones for break indication.
OUT-REQ	SIG.	CH6	Causes ACU to supply character from memory during a READ operation.

NAME	TYPE	SOURCE	DEFINITION
PACK	FF	CH5	Holds DLE until next character can be sent directly following; also packs character into shift register if auto SYN was sent because character was late.
PAD	FF	CH5	Lengthens transmission by sending a pad character of all 1's - preventing premature shutoff on 2 wire systems. Pad is disabled by const. car.
PIOB	SIG.	CH5	A combination of P/IOBUSY and ON LINE. Has no relationship to the buffer, IOB.
PND	SIG.	DIAL-ING UNIT	Present Next Digit - A signal to the SCA that the calling unit is ready to accept the next dialing digit.
PWI	SIG.	DIAL-ING UNIT	Present Indication - A signal that is present from the calling unit when it is operational.
RC	SIG.	CH8	Remote Control - Active when answering an incoming call, or when dialing out. This line is released for approximately 150ms for hangup. RC and RR (remote release) are connected in the modem cable, if this connection is not present, the modem will not lock in the data mode.
RD	SIG.	MODEM	Receive Data - The SCA receives data, bit serially, from this line. A positive polarity represents a binary zero; a negative polarity represents a binary one.
READ	FF	CH6	See text for use. Indicates active op is READ.
RECSH	FF	CH6	Timing related to shifting IOS to IOB, and clearing IOS.
RESINT	FF	CH6	
RESSCLR	FF	CH6	
RG1	SIG.	MODEM	Ring Indicator 1 - Indicates to the SCA that an incomming call is ringing. In the SCA, it sets SERVice REQuest, branching the software program to accept data.
	Se		
RS	SIG.	CH8	Request To 1Snd - A positive potential is applied to this line during data transmission. A negative potential is applied when the transmission ends. When using a two-wire configuration, this line also transfers the data set (modem) from transmit to receive. The positive transition (controlled by the SCA) should be coincident with the positive going transition of the DCT (dibit clock transmit) signal.

NAME	TYPE	SOURCE	DEFINITION
RTS	FF	CH5	Establishes times when the SCA logic requires the Request to Send (RS) signal to the modem. The SCA request can be swamped by continuous carrier requests.
SCTDLD	FF	CH6	Serial Clock Transmit Delayed.
SD	FF	CH6	Send Data - The SCA applies transmitted data to the SD line bit serially. A positive polarity represents a binary zero; a negative polarity represents binary one.
SCR	SIG.	MODEM	Serial Clock Receive - A square wave similar to the SCT signal, but is synchronized with the modem receiver timing. Data bits are received by the SCA in synchronism with the positive transition, and transmitted by the modem near the negative transition.
SCRCLK SCRINT SCRDLI	FF FF FF	CH8 CH8 CH8	Serial Clock Receive Sub-divisions, Generates series of pulses near the transitions of modem signal, Related to trigger for clock check register.
SCT	FF	CH8	Serial Clock Transmit - A square wave from the data set (modem) transmitter timing circuits. It is used by the SCA to synchronize data transfer with the modem timing. Data bits are provided by the SCA near the positive transition, and transmitted by the modem near the negative transition.
SCTDLD SCTDLI SCTINT	FF FF FF	CH6 CH8 CH6	Serial Clock Transmit Sub-divisions, Generates series of pulses near the transitions of the modem signal.
SOHTX	FF	CH5	Start of heading or start of text.
STAWP	FF	CH5	Clears RTS FF after suitable delay.
SVRQ	XLATCH	CH8	Service Request FF. Modem has indicated ringing is present.
SYN	FF	CH5	Transmits time filler SYN's.
SYNOS	ONE SHOT	CH5	SYN One Shot - One second timer for SYNSYN FF. Sends 2 SYN's every one second.
SYNSYN	FF	CH5	Controls SYN FF - To produce 2 hardware SYNs.

NAME	TYPE	SOURCE	DEFINITION
VRC	—	—	Vertical Redundancy Check - Odd parity in each character.
TERMINATING CODE	—	—	Any of the ending characters - ETB, ETX, ENQ, EOT, ACK, NAK, and DLE (with any following character).

11-6.5 SCA EQUATIONS

KEY:
C/ = clear; dc reset.
D/ = qualification for input to a D flip-flop.
P/ = preset; dc set.
T/ = trigger; clock.

ACUTO = $\overline{(CRQ \cdot CINT \cdot ON \cdot LINE)}$

ADDRBAD = $((\overline{5BCR=\emptyset}) + \overline{VRC}) \cdot \overline{COMPARE}$

C/BCR = NIL + $\overline{SOHTX} \cdot \overline{READCNTL}$
T/BCR = BCRT2
BCR=Ø = 5BCR · BCR(7) · $\overline{BCR(6)}$ · SOHTX
R7CTS = B7 · CTS
D/BCRT1 = ALWAYS
C/BCRT1 = $\overline{BCRT2}$
T/BCRT1 = BCRTRIG
D/BCRT2 = BCRT1
T/BCRT2 = MFCLK
C/BCTR = $\overline{COUNT}$
T/BCTR = SCRNREC + SEND · $\overline{SCTINT}$

C/BREAK = $\overline{REC}$
D/BREAK = $\overline{ADDRBAD}$
T/BREAK = CYSYNN
P/BREAK = REC · IDLE

BCRTRIG = LOKOUT · LOADIOS + SCINDØCH · $\overline{IORSYN}$ + SCRDBØCH · $\overline{IORSYN}$ · CNTL · T/VRC + $\overline{READCNTL}$ · (PACK + RTS · B7 · $\overline{SYN}$ · IOS(8) · DELAY · SCT · SCTDLD)

C/CHECK = SYSRST + P/LDREQ · ON LINE
P/CHECK = P/CHECK · ON LINE

C/CHPHAS = $\overline{BREAK}$ · SCRNREC + $\overline{REC}$ + DISC · BØ
D/CHPHAS = COUNT · IORSYN
T/CHPHAS = SCRBØCHN

CINT = C/INT · ON LINE

CNSYNN = SCRINØCH · $\overline{IORSYN}$ · CNTL

D/CNTL = $\overline{IOR(6)}$
T/CNTL = $\overline{LIOSBZYN}$

C/COMPARE = $\overline{CHPHAS}$
D/COMPARE = $\overline{CNTL}$ + $\overline{ADDRBAD}$
T/COMPARE = CNSYNN + $\overline{CNTL}$ · SCRDBØCH · $\overline{IORSYN}$

P/CONCAR = CONSCAR · PIOB · DVCTR=Ø
C/CONCAR = $\overline{LTO}$
D/CONCAR = $\overline{EOTT}$ · CONCAR
T/CONCAR = SCTRD

CONSCAR = $\overline{READ\ CNTL}$

C/COUNT = NIL + IDLE REC + REC · $\overline{BREAK}$
D/COUNT = REC · IORSYN + $\overline{REC}$ · CTS
T/COUNT = DCT · CTS · SCTDLY + SCRBØCHN
P/COUNT = COUNT · SEND

P/CRQ = $\overline{DLO \cdot DIAL}$
C/CRQ = $\overline{DIAL}$

CTS = CTSMDM·RTS·IDLE
CSYN = ETBX + PAD + LTO + $\overline{SEND}$ + LDREQ

DATA = RD·$\overline{RTS}$ + SD·RTS

P/DCALL = DIAL + REC + JUMPER
C/DCALL = SYSRST + HANGUPOS

D/DCT = $\overline{DCT}$
T/DCT = SCTDLI
C/DELAY = ETBX + PAD + $\overline{RTS}$
D/DELAY = $\overline{SYN}$·(DVCTR=Ø + LAST)·READ·$\overline{PACK}$
T/DELAY = SCTDB7CS

P/DERROR = ACR
C/DERROR = T/DIAL

P/DFLAG = DIAL·SVRQ
C/DFLAG = T/DIAL

D/DIAL = OUTDATA5·IOCDATA6·OUTDATA1·$\overline{OUTDATA2}$·$\overline{OUTDATA3}$·$\overline{OUTDATA4}$
T/DIAL = $\overline{T/DIAL}$
C/DIAL = DSS + DERROR + LTO + DFLAG

Note: The signal DIAL= $\overline{ONLINE \cdot LOADIOS \cdot IO\ BUSY}$

P/DIGIT = $\overline{CINT \cdot ON \cdot LINE}$
C/DIGIT = $\overline{DIAL + PND}$

D/DINT = ALWAYS
T/DINT = PND·CRQ·$\overline{DLAST}$
C/DINT = CINT·ON·LINE

C/DISC = PIOB
D/DISC = (ETBX + DLE + LAST + IOREANK + DISC + EOTT·$\overline{READCNTL}$)·XCNTLRD
T/DISC = SCRINØCH

P/DLAST = $\overline{P/LAST}$·ON LINE
C/DLAST = $\overline{CRQ}$

C/DLE = $\overline{IOBUSY}$
D/DLE = IORDLE
T/DLE = SCTRD

DLEINT = PACK + DLE·INT

DPR = PND·DIGIT

LOAD/DVCTR = $\overline{LIOSBZYN}$
COUNT/DVCTR = CINT·($\overline{DVCTR=Ø}$)

C/ENDD = $\overline{\text{IOBUSY}} + \overline{\text{READ}}$
D/ENDD = LAST·SYN·PACK
T/ENDD = SCTDB7CS

P/EOTIDLE = BØ·EOTT·READCNTL
T/EOTIDLE = $\overline{(\text{SCR}\cdot\overline{\text{SCRINT}})}$
EOTT = IOREOT·COMPARE

C/ERROR = PIOB
D/ERROR = IOREOT·COMPARE·$\overline{\text{DLE}}$ + ERROR + ETBX·$\overline{(\text{BCR=Ø})}$ + $\overline{\text{VRC}}$·XCNTLRD
P/ERROR = REC·LAST + $\overline{\text{DISC}}$·(IOS(8)·$\overline{\text{IORSYN}}$·SCINDØCH + IDLE·CHPHAS)
T/ERROR = SCRINØCH

C/ETBX = PAD + $\overline{\text{IOBUSY}}$
D/ETBX = DELAY·IORETBX + CHPHAS·IORETBX
T/ETBX = SCTB7CS·SCINT + SCRDBØCH + ETBX

ETBXSYN = $\overline{(\overline{\text{IORSYN}}\cdot\overline{\text{ETBX}})}$

P/FAULT = LTO
C/FAULT = PIOB

P/FLAG = DLE·$\overline{\text{CNTL}}$·REC
C/FLAG = PIOB
D/FLAG = CNTL·$\overline{\text{IOR6}}$
T/FLAG = COMPARE

T/HANGUPOS = DCALL·ACR + ONHOOK·$\overline{\text{MFCLK}}$ + T/DIAL·$\overline{\text{DIAL}}$·OUTDATA2·OUTDATA5·IOCDATA6

IDLE = $(\overline{\text{CO}} + \text{ONES} = 15)\cdot\text{IT}$

INPUT DATA 1 = (IOB(1)·IOBUZY + ERROR·$\overline{\text{IOBUZY}}$)·IOSTMN
INPUT DATA 2 = (IOB(2)·IOBUZY + $\overline{\text{FLAG}}$·$\overline{\text{IOBUZY}}$)·IOSTMN
INPUT DATA 3 = (IOB(3)·IOBUZY + $\overline{\text{FAULT}}$·$\overline{\text{IOBUZY}}$)·IOSTMN
INPUT DATA 4 = IOB(4)·IOBUZY IOSTMN
INPUT DATA 5 = IOB(5)·IOSTMN
INPUT DATA 6 = $\overline{\text{IOB(6)}}$·IOSTMN
INPUT DATA 7 = $\overline{\text{IOB(6)}}$·IOSTMN

P/INT = $\overline{\text{READ}}$·PIOB·($\overline{\text{CNTL}}$ + DVCTR(1)) + READ·PIOB·$\overline{(\text{DVCTR=Ø})}$ + IOB(8)
C/INT = CINT·SEND·($\overline{\text{SYN}}$ + IOS(8) + LAST + $\overline{\text{SOHTX}}$) + READ·CINT·IOB(8) + $\overline{\text{IOBUZY}}$
T/INT = $\overline{\text{SCTDB7CS}}$
D/INT = INT + ($\overline{\text{SYN}}$ + LOKOUT)·$\overline{\text{LAST}}$·$\overline{\text{PACK}}$·($\overline{\text{READ}}$ + $\overline{(\text{DVCTR=Ø})}$) +IORDLE

INTERRUPT/3 = DINT

INTREQ/3 = DINT·ON LINE

C/IOB = $\overline{\text{REC}}$ + CINT
SHIFT/IOB = RECSH
MODE/IOB = NEVER - LOADS ONLY

P/IOBUZY = PIOB·$\overline{\text{CONSCAR}}$·$\overline{\text{LDREQ}}$

C/IOBUZY = $\overline{\text{COUNT}}$·ERROR·CHPHAS + LTO + DISC·REC·$\overline{\text{CHPHAS}}$·$\overline{\text{IOS(8)}}$·$\overline{\text{IOB(8)}}$ + LAST·REC

D/IOBUZY = SEND·$\overline{\text{ENDD}}$·IOBUZY

T/IOBUZY = SCTB7CS

IOBUSY/3 = (HANGUPOS + DIAL)·ON LINE

C/ONES = LTO + $\overline{\text{RD}}$·SCRDLY

T/ONES = RD·$\overline{\text{SCRDLY}}$·$\overline{\text{(ONES=15)}}$

S/15 ONES = P/EOTIDLE·EOTIDLE·SCRDLI

SHIFT/IOR = LOADIOS·ON LINE + SCRNREC

MODE/IOR = REC

INPUT/IOR7 = OUTDATA7 (DVCTR=Ø + $\overline{\text{IOBUSY}}$ + DLE·OUTDATA5) + $\overline{\text{OUTDATA6}}$·LOKOUT

SHIFT/IOR = LOADIOS·ONLINE+SCRNREC

MODE/IOR = REC

IOR8S = $\overline{\text{IOR(8)}}$ + SEND

IORCNTL = $\overline{\text{IOR(7)}}$·$\overline{\text{IOR(6)}}$·$\overline{\text{IOR(4)}}$·$\overline{\text{ETBX}}$

IORDLE = IORCNTL·IOR(5)·$\overline{\text{IOR(3)}}$·IORNB1B2·IOR8S

IOREANK = IORCNTL·IOREB1B2·IOR(3)·($\overline{\text{IOR(5)}}$·IOR(8) + $\overline{\text{IORSYN}}$·IOR(5)·$\overline{\text{IOR(8)}}$)

IOREB1B2 = $\overline{\text{IOR(2)}}$·IOR(1) + IOR(2)·$\overline{\text{IOR(1)}}$

IOREOT = IORCNTL·$\overline{\text{IOR(5)}}$·IOR(3)·$\overline{\text{IOR(8)}}$·IORNB1B2·CHPHAS

IORETBX = IORCNTL·IOR(2)·IOR(1)·IOR(8)·(IOR(3)·IOR(5) + $\overline{\text{IOR(3)}}$·$\overline{\text{IOR(5)}}$)

IORNB1B2 = $\overline{\text{IOR(2)}}$·$\overline{\text{IOR(1)}}$

IORSOTX = IORCNTL·IOREB1B2·$\overline{\text{IOR(5)}}$·$\overline{\text{IOR(3)}}$·IOR8S·$\overline{\text{SYN}}$

IORSYN = IORCNTL·IOR(5)·IOR(3)·IOR(2)·$\overline{\text{IOR(1)}}$·$\overline{\text{IOR(8)}}$

C/IOS = PIOB + STAWP + $\overline{\text{RESSCLR}}$

SHIFT/IOS = $\overline{\text{COUNT·SCTRSSN·(B7·IOS(8))}}$ + PACK + IOSRECSH

MODE/IOS = (B7 + SYN + CHPHAS)

IOSRECSH = $\overline{\text{ETBXSYN}}$·SCRINØCH·$\overline{\text{IORDLE}}$·XCNTLRD

IOSTMN = IOS-T-MN·ON LINE

P/LAST = P/LAST·ON LINE

C/LAST = PIOB

C/LDREQ = SYSRST + C/LDREQ·ON LINE

P/LDREQ = P/LDREQ·ON LINE

LIOSBZYN = LOADIOS·ON LINE·$\overline{\text{IOBUSY}}$

C/LOKOUT = REC
P/LOKOUT = PIOB·READCNTL
D/LOKOUT = NEVER
T/LOKOUT = INT

LTO = SYSRST + PWI + LTOFF ·MFCLK

D/LTOFF = $\overline{\text{LTOOS}}$·($\overline{\text{NIL}}$ + OPDIAL)·ON LINE + COUNT·SEND·$\overline{\text{(RTS IDLE)}}$
T/LTOFF = MFCLK

T/LTOOS = (ENDD + ACUTO + INT + DISC + PIOB + LTOFF)·($\overline{\text{NIL}}$ + OPDIAL)

P/NBR1 = ON LINE·LOADIOS·OUTDATA1
C/NBR1 = $\overline{\text{PND}}$

P/NBR2 = ON LINE·LOADIOS·OUTDATA2
C/NBR2 = $\overline{\text{PND}}$

P/NBR4 = ON LINE·LOADIOS·OUTDATA3
C/NBR4 = $\overline{\text{PND}}$

P/NBR8 = ON LINE·LOADIOS·OUTDATA4
C/NBR8 = $\overline{\text{PND}}$

NIL = $\overline{\text{SYN}}$·$\overline{\text{IOBUSY}}$

C/ONES = LTD+$\overline{\text{RD}}$·SCRDLY
T/ONES = RD·SCRDLY·$\overline{\text{(ONES = 15)}}$
SET 15 ONES = P/EOTIDLE·EOTIDLE·$\overline{\text{SCRDLI}}$

D/OHHOOK = $\overline{\text{IOBUSY}}$
T/ONHOOK = LTO

OPDIAL = DIAL·$\overline{\text{DLAST}}$ + $\overline{\text{DIAL}}$·DCALL

OUTREQ3 = $\overline{\text{REC}}$·ON LINE

D/PACK = (SYN·$\overline{\text{READ}}$·$\overline{\text{LAST}}$ + RACK)·SOHTX
T/PACK = $\overline{\text{CINT}}$
P/PACK = SYN·DLEINT
C/PACK = $\overline{\text{SYN}}$·BØ

C/PAD = $\overline{\text{RTS}}$
D/PAD = ETBX + DELAY·$\overline{\text{IORETBX}}$
T/PAD = SCTDN7CS

PIOB = P/IOBUSY·ON LINE

PSYN = (CNTL (DVCTR=1 + $\overline{\text{READ}}$) + $\overline{\text{CNTL}}$ READ $\overline{\text{DVCTR=Ø}}$)

RC = DCALL

RDCNTL = READ·CNTL

D/READ = $\overline{IOR(5)}$
T/READ = LIOSBZYN

REC = READ·DVCTR=Ø·$\overline{RTS}$·IOBUZY

C/RECSH = $\overline{RESINT}$
D/RECSH = IOB(8)·IOS(8)·REC
T/RECSH = MFCLK

D/RESINT = $\overline{RECSH}$
T/RESINT = MF·CLK

C/RESSCLR = $\overline{RESINT}$
D/RESSCLR = RESINT
T/RESSCLR = $\overline{MFCLK}$
C/RS = $\overline{RTS}$
P/RS = RTS·IDLE + CONCAR + JUMPER

T/RTS = $\overline{RTS}$·DCT
D/RTS = $\overline{SYN}$
C/RTS = $\overline{SEND}$ + STAWP· $\overline{B7CTS}$

SCIND = SCRDLI·$\overline{SCRINT}$

SCINDØCH = SCIND·BØ·CHPHAS

SCR/D = $\overline{SCRPRE}$
T/SCR = $\overline{MFCLK}$

SCRCH = SCR·CHPHAS

SCRBØCHN = SCR·BØ·$\overline{CHPHAS}$·REC

D/SCR H = SCRDCH·BØ

SCRDCH = SCRDLY·SCRCH

D/SCRDLI = $\overline{SCRINT}$
T/SCRDLI = $\overline{MFCLK}$

SCRDLY = SCRDLI·SCR

SCRINØCH = BØ·CHPHAS·SCR·$\overline{SCRINT}$

D/SCRINT = SCR
T/SCRINT = MFCLK

SCRMIDCH = SCRINT·$\overline{SCRPRE}$.REC
SCRNREC = $\overline{SCR}$·REC·SCRDLI

D/SCRPRE = SCRMDM
T/SCRPRE = MFCLK

```
D/SCT          = SCTMDM
T/SCT          = MFCLK

D/SCTDLD       = SCTINT + SEND
T/SCTDLD       = MFCLK

SCTB7CS        = SCT·B7CTS

SCTDB7CS       = SCTDLY·SCTB7CS

D/SCTDLI       = SCT
T/SCTDLI       = MFCLK

SCTDLY         = SCTDLI·SCT

SCTDN7CS       = SCTDLI·B7CTS

D/SCTINT       = SCT
T/SCTINT       = MFCLK

SCTRD          = SCTDB7CS + SCRDBØCH

SCTRSSN        = SCT·RTS·SYN

SEND           = SYN + REC·IOBUSY

P/SD           = RTS + STAWP
D/SD           = IOS(1)·SYN·ETBX·B7 + B7·VRC + SYN·(B1 + B2 + B4) + ETBX·
                 (BØ·BCR(1) + B1·BCR(2) + B2·BCR(3)+B3·BCR(4)+B4·BCR(5)+
                 B5·BCR(6) + B6·BCR(7))+B7·PAD
T/SD           = SCT·CTS·COUNT

C/SOHTX        = COUNT
D/SOHTX        = SOHTX + IORSOTX
T/SOHTX        = SCTRD

C/STAWP        = RTS
D/STAWP        = ALWAYS
T/STAWP        = PAD·BØ+PAD·(CONCAR+JUMPER)

P/SVRQ         = RG1·HANGUPOS
C/SVRQ         = ON LINE·C/SERV REQ + LTO + REC + HANGUPOS

C/SYN          = CSYN
P/SYN          = SYNSYN + DLEINT·SEND·IORDLE
D/SYN          = READ·ENDD·SEND + LOKOUT + INT·IOS(8)
T/SYN          = TSYN

T/SYNOS        = SYNSYN·CTS

C/SYNSYN       = CSYN
P/SYNSYN       = PIOB·PSYN
D/SYNSYN       = SYNOS
T/SYNSYN       = TSYN
```

$$TSYN = IOBUZY \cdot SCTDN7CS$$

$$C/VRC = PAD \cdot \overline{B6}$$

$$P/VRC = REC \cdot CHPHAS$$

$$T/VRC = \overline{SCRMIDCH + SCTDLY \cdot SEND}$$

$$D/VRC = \overline{(B\emptyset \cdot SYN + B\emptyset \cdot \overline{DATA} + \overline{B\emptyset} \cdot VRC \cdot DATA + \overline{B\emptyset} \cdot \overline{VRC} \cdot \overline{DATA})}$$

$$XCNTLRD = COMPARE + \overline{CNTL}$$

$$5BCR=\emptyset = \overline{BCR(1)} \cdot \overline{BCR(2)} \cdot \overline{BCR(3)} \cdot \overline{BCR(4)} \cdot \overline{BCR(5)} \cdot (IOR(6) + IOR(7))$$

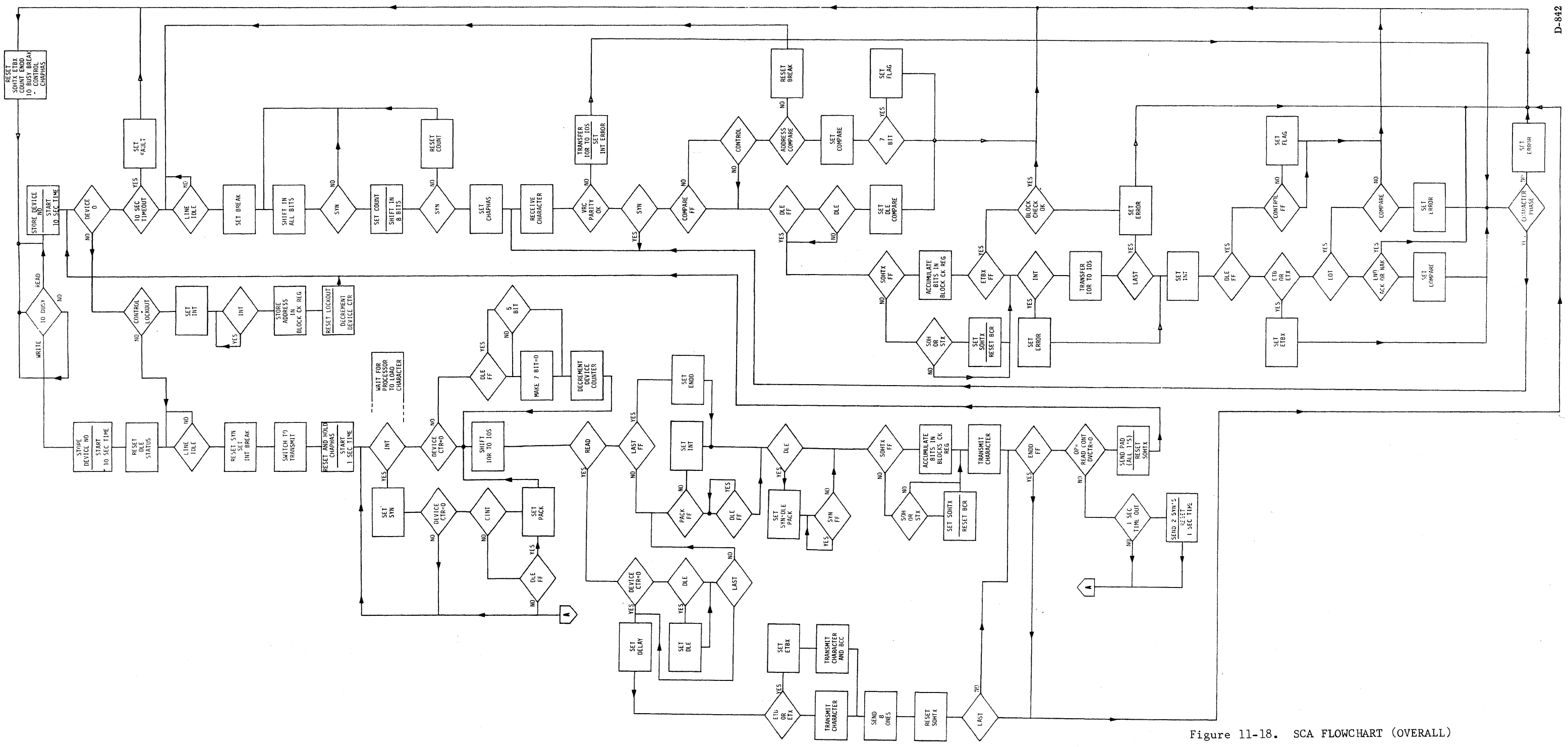


Figure 11-18. SCA FLOWCHART (OVERALL)

SECTION CONTENTS

12-1.0 INTRODUCTION

The disc controller interfaces the Model 20/21 Processor with a variety of disc storage units. The number of disc units can vary with customer requirements up to a maximum of ten unit addresses. In the case of Model 40 and Model 42 disc drives, the unit address is one complete drive unit. A Model 44 contains four volumes; each volume is addressed as a unit, and contains the same data storage capabilities as a single Model 40. The disc units are limited to specific electro-mechanical operations, and are slaves to the commands that are issued by the disc controller. Generally stated, a disc unit (drive) can READ, WRITE, and SEEK - at the specific request of the controller.

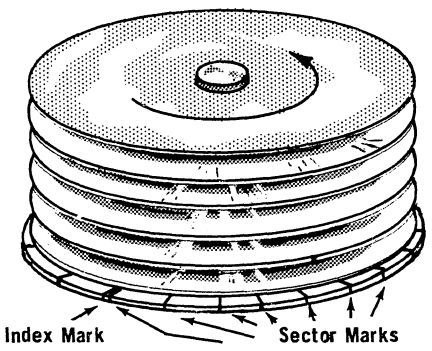
A series of ten FAC-STROBEs, and the proper accompanying information, control the selection and verification of the disc controller, the disc unit, and the cylinder, or track, address. If the controller is busy or the heads are not located over the desired cylinder (track) the instruction is restored to memory, and will be repeated when the partition is serviced by the ACU again. Depending upon the total program load, and the distance the heads may have to seek, an instruction may be pulled many times before it is completed. This process is described in detail in the text that follows.

12-2.0 DATA LOCATION

The desired cylinder location is given to the disc unit by the controller, and the mechanical movement and counting of tracks is done mostly by the disc unit. When movement is completed, the disc unit reports that it is ONCYLINDER, and the controller directs a sector search. Sector pulses are sent to the controller through interconnecting cables, and the sector location is calculated by the controller. One of the sector marks on the disc pack has an index mark closely following the sector mark. By counting the sector pulses after the index marker, a sector number can be located. The illustration shows the sector disc at the bottom of a disc pack.

SECTOR COUNTER

The sector counter on the DDC card is incremented by pulses from sector marks, and is reset by an index mark which is similar to the sector mark except for a closer spacing. The counting progression is not by units, but by a modified tens count. This progression places four sectors between sucessive numbers, allowing enough time between successive numbers for a new instruction. In this way continous data can be written on progressively higher numbered sectors. The counter starts at 00; the next numbers are 10, 20, 30, and 40. The units digit is then steped one, and the next five sectors are 01, 11, 21, 31, and 41. The progression continues until the series of five sectors is 09, 19, 29, 39, and 49, and the counter is reset to 00 again (by the index mark).



The table below shows the relationship of the physical placement to the sector counter assignments.

PHYSICAL SECTOR LOCATION	ACTUAL SECTOR																				
1 - 5	00	10	20	30	40	21 - 25	04	14	24	34	44	41 - 45	08	18	28	38	48
6 - 10	01	11	21	31	41	26 - 30	05	15	25	35	45	46 - 50	09	19	29	39	49
11 - 15	02	12	22	32	42	31 - 35	06	16	26	36	46						
16 - 20	03	13	23	33	43	36 - 40	07	17	27	37	47						

12-2.0 DATA LOCATION (Continued)

SECTOR FORMAT

Each sector of the disc pack is recorded with information that allows the controller to synchronize with the data and verify the track number. The sector format is as follows:

- A leader of six ASCII space characters (36 zero bits) for clock sync.
- One ASCII underscore character (6 one bits). These bits are used for character synchronization.
- A one-character cylinder, or track, address (modulus 64). This is repeated on all of the sectors of the same cylinder.
- The data field of one hundred characters (600 bits).
- One Longitudinal Redundancy Check Character (LRCC). The LRCC makes the total number of one bits in each bit position an even number.
- A trailer of all one bits. The trailer is continous until the next sector pulse is detected, which is usually 4 to 6 characters.

12-3.0 INSTRUCTIONS

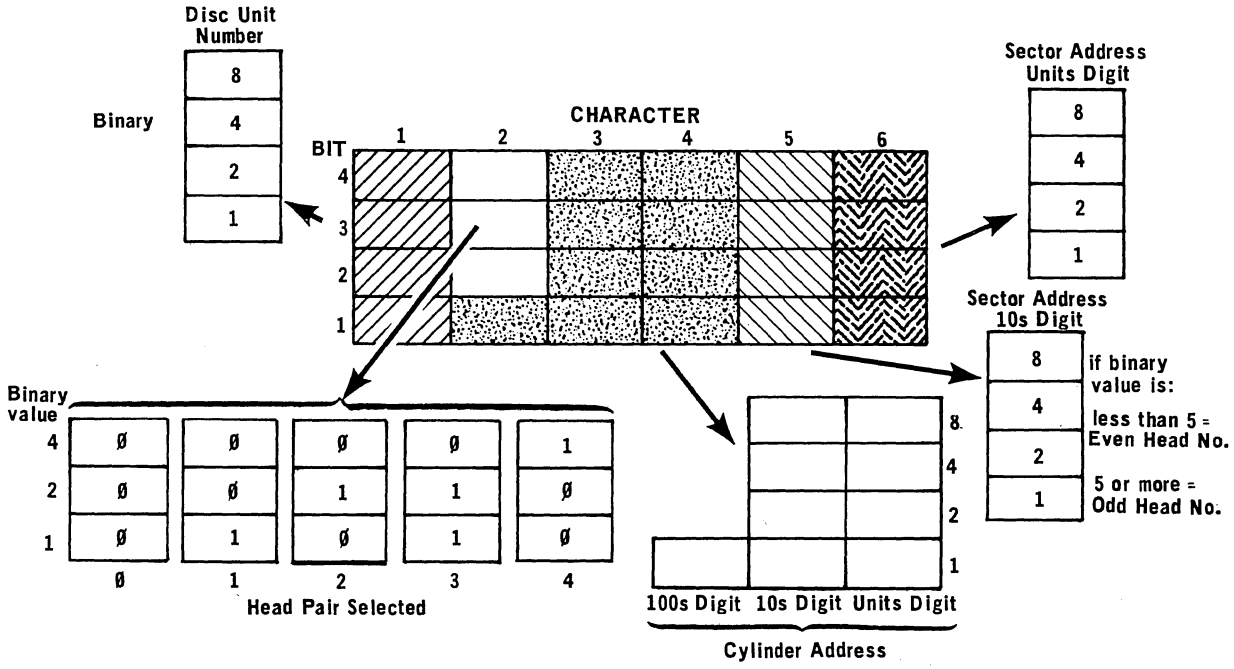
The partition hosting the controller request can operate under any of the processor instructions that are available to a normal input/ output channel. The disc controller however, responds to only three instructions, READ, WRITE, and WRITE CONTROL. The WRITE CONTROL instruction is only effective in controllers that contain a DXH card rather than a DRH card. The DXH controller must use a WRITE CONTROL instruction to initialize a previously unrecorded disc pack; the DRH controller treats a WRITE CONTROL as a normal WRITE.

The instruction word makeup for disc addressing is slightly different than I/O to memory addressing because there are two distinct addresses that are requried, the ACU memory address, and the data location on the disc pack. The ACU address is specified by the "A" field of the instruction word, as it is in any I/O read or write operation. The binary number in the "A" field locates the beginning (MSD) of the field of data that is to be entered into or extracted from memory. When LA=Ø and LB=Ø or 2, the instruction is requesting the disc controller, and the number of data characters that will be transfered is hardware set at 100. The "B" field of the disc instruction specifies the location in ACU memory of a six-character disc address. This address contains the disc unit number, cylinder number, head number, and sector number. A diagram of the six-character disc address is shown at the top of the opposing page.

The disc address is processed through the ACU data fault logic and must conform to the data fault standards. For the Model 20 each character must contain a 5-bit, and the lower four bits must not exceed a binary value of 9. For the Model 21, the 5-bit is not required, but the lower four bits must not exceed a binary 9. The 7-bit is ignored in the disc address.

If the system is operating under the DMF Disc Management Facility, the disc addressing will be the same, but is accomplished by the program.

12-3.0 INSTRUCTIONS (Continued)



SIX-CHARACTER DISC ADDRESS

12-4.0 STATUS

At the end of each completed data transfer, the controller reports the success or failure of the operation through the FAC Status character. The inset shows the status character bits and the meaning that is interpreted by the ACU. If FAULT status occurs, the operation is ended immediately without data transfer. After a WRITE operation, the ERROR and REPEAT if error bits are forced by hardware to cause the instruction to be repeated for the read-check operation. A read-check that does not prove good causes the WRITE to be repeated. However, after three unsuccessful tries at writing in a sector, a "blot" is written in the sector and FLAG is set. If a "blot" is read on a sector that is addressed by program, FLAG is set. A summary of status conditions is given below. These status conditions are meaningful only if the program tests for the conditions through the BRANCH variants.

Bit	
6 (N2)	(not used)
5 (N1)	(not used)
4 (M4)	REPEAT if ERROR
3 (M3)	$\overline{\text{FAULT}}$
2 (M2)	FLAG
1 (M1)	ERROR

FAC STATUS CHARACTER

ERROR - Forced by hardware to cause read-check, bad data compare during read-check, wrong track ID during READ, accumulated LRCC does not compare with LRCC from disc.

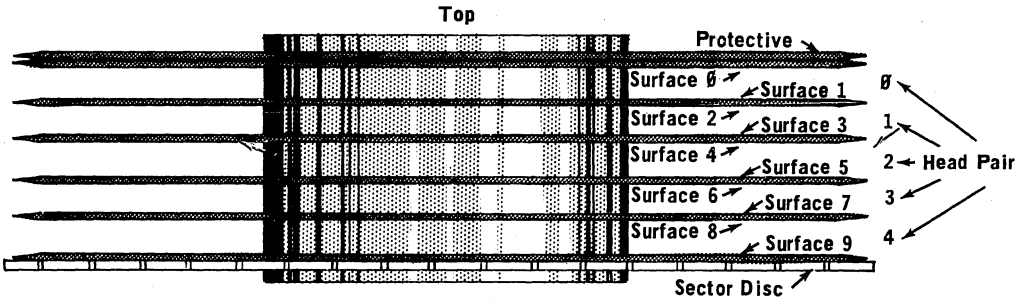
FLAG - Blot is read or written.

FAULT - Releases the processor immediately. Disc unit problems: no power, not online, disabled, speed too fast or slow, file unsafe.

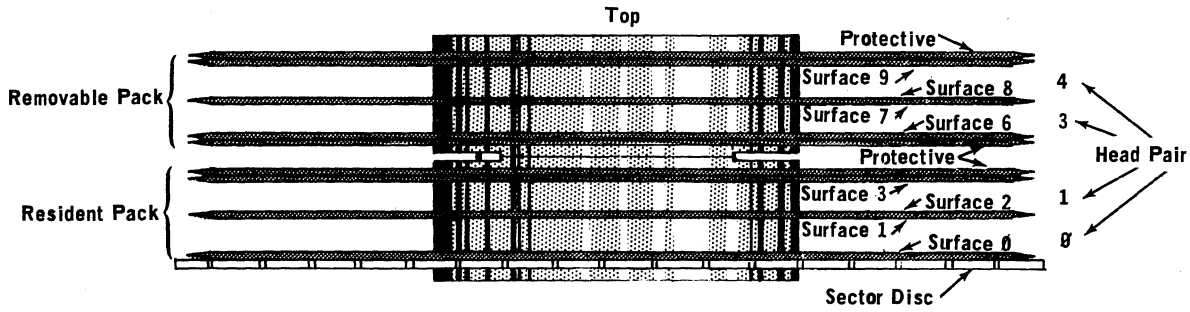
REPEAT - Forced with ERROR to cause read-check. Also allows retries when data compare or LRCC is bad.

12-5.0 DISC PACKS

There are three pack configurations currently used in the field. Each pack type is unique to the model drive on which it is used. The packs that are used on the Model 40 and Model 42 disc drives are similar in physical appearence except that the Model 42 pack seperates into upper and lower parts (that are interchangable with the corresponding parts of other Model 42 packs). The illustrations below show that the physical location of the data address differs between the two models. Also, the two middle surfaces, 4 and 5, are not used on the Model 42 pack.



MODEL 40

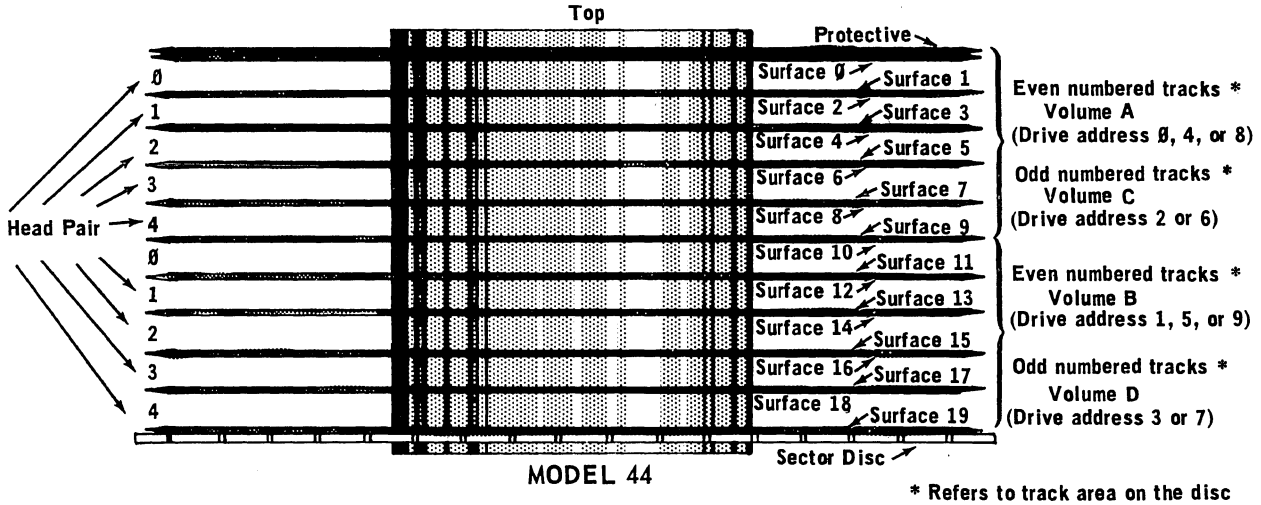


MODEL 42

While the surface address are reversed between the Model 40 and Model 42, the cylinder, or track, addreses are the same. The tracks are numbered from 00 at the outer edge to 199 for the track nearest the hub. Sector addresses within each track are identical between models.

Addresses on the Model 44 disc pack (shown on the opposing page) are similar to those on a Model 40 disc pack, except that there are twice as many surfaces, and twice as many tracks on each surface. The controller addresses all of the disc units in the same manner. The Model 44 accepts four unit addresses (called volumes in the Model 44) as if they were seperate drives. As shown in the figure, the addresses of volume A are on the top five discs (ten surfaces). The tracks are spaced .005" center-to-center, but head movement within a volume is .010". This makes the addresses of one volume on every other track, rather than successive tracks. Volume equivelents of disc unit addresses are determined at the time of installation by where the cables are connected.

12-5.0 DISC PACKS (Continued)



MODEL 44

* Refers to track area on the disc surface, not the cylinder address.

12-6.0 DISC CONTROLLER OPERATION

The following is an overall system description of the ACU, controller and disc unit, with emphasis on the controller. The disc unit that is used in the description is the Model 40; other models may vary slightly in method, but the effect and results are the same.

12-6.1 FAC MODULE SELECTION

The processor begins to service the partition by reading the ten character instruction word from memory. This instruction was located by examining the address in the P register. For the first part of this explanation, the instruction is assumed to be a WRITE.

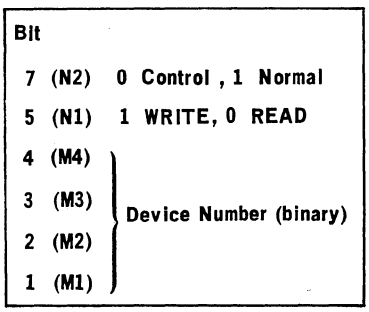
After the processor has pulled the instruction (in BEGIN) and determined that it is a READ/WRITE operation, the ACU completes the necessary internal operations and jumps to R/W Ø. In R/W Ø, the LB portion of the instrution is examined, and if LB=Ø or 2 (or any even number) the operation is within the File Access Channel, or FAC (other operations take place in R/W Ø, but do not directly affect the controller at this time). The ACU pulls the FAC Protect Character (also known as the A4 character) from protected memory. The FAC Protect Character governs the extent of FAC activities that can be performed by the active partition.

12-6.2 DEVICE SELECTION

If the operation (in the instruction that was just pulled) is allowed by the FAC Protect Character, the ACU jumps to R/W 10 (if the operation is not allowed, the instruction becomes no-op with no indication to the operator). In R/W 10, the ACU sends the FAC Select Character to all FAC devices (on the M and N lines). Only the device that matches the number in the lower four bits (M1, M2, M3 and M4) will respond. The lower four bits were extracted from LA of the instruction in

12-6.2 DEVICE SELECTION (Continued)

R/W Ø; the disc controller is device Ø. The FAC Select Character is shown in the inset at the right of the page. In a controller that contains a DRH card, the WRITE CONTROL operation is considered a normal WRITE. In a controller that contains a DXH card, the WRITE CONTROL is used to initialize a previously unwritten pack.



FAC SELECT CHARACTER

12-6.3 WRITE INSTRUCTION

When the FAC Select Character is presented, the disc controller may be busy with internal functions that are left over from an operation that is just completed. In that case the ACU does not receive an acknowledgement, and decrements the P count by ten, so the instruction will be repeated when the partition is serviced again. If the controller is selected, a signal called M=Ø is generated, and the controller acknowledges the action and sets its own A counter (which was initially at A=15) to A=Ø. As soon as the acknowledgement is received, the ACU steps from R/W 10 to R/W 11; the controller remains in A=Ø. In R/W 11 the B address of the instruction in core (the six-character disc address) is located, and the first character is placed on the M and N lines, followed closely by an FAC-STROBE. The controller, promped by the FAC-STROBE, accepts the character, stores it (on the DCF card) and increments the A counter to A=1. The number (character) that was just transfered is the disc unit number for the first part of the controller selection process. As the A counter steped to A=1, the decoded number was forwarded to the DDC cards, selecting one half of one DDC card. This effectively selects one disc unit (or volume) because of the data cable cable connections.

The SELECT signal becomes MODSEL in the drive. If the drive has power, is ONLINE, and the ENA/DISABLE switch is in the ENA position, the signal SELECTED is developed in the disc unit. SELECTED becomes ECHO in the controller.

If FILE UNSAFE or SEEK INComplete are active, FAULT would be set. However, FAULT is a special case, and is discussed later in the text. RDY and ONLINE must be active to complete the unit selection. RDY is active after the brush cycle and the first seek are completed when the unit is first powered up, and stays active when the carriage is not moving. ONLINE becomes FSLCTD in the controller.

When the ACU steps to R/W 12, it sends the partition number to the controller along with an FAC-STROBE. The partition number is presented to the DDC card as a binary number on the M and N lines. The binary weighting of the bits that are from the M and N lines is explained in a later paragraph (see page 12-22). The explanation is accompanied by a table of the partition numbers.

The partition number is compared by the controller to the contents of the P (partition) register on the selected half of the DDC card. If the P register contains all 1s, or is the same number that is now on the M and N lines, or if the timeout oneshot has expired, the controller sends an ACK to the ACU. All 1s in the P register indicates that the drive is not in use by any partition. If the number in the P register is the same as the incomming partition number, it indicates that a seek was started, and an attempt is being made to complete the operation (if

12-6.3 WRITE INSTRUCTION (Continued)

the disc unit has finished seeking). The timeout oneshot is set when a partition first reserves a drive. If for some reason the operation is not completed within 1.8 seconds, the unit is considered available to any partition that requests it.

An acknowledgement to the ACU in R/W 12, A=1 means the requested drive is available for use by the active partition. If there is no acknowledgement, the operation is postponed until conditions are right. The instruction is ended, in that case, but before the P count is stored in protected memory, it is decremented by ten characters so the same instruction will be pulled the next time the partition is serviced. Eventually (a very short time in human terms) the instruction will be pulled, the drive will be ready and available and the operation will proceed. An ACK will be given in R/W 12, and the selection continues. The ACK that is given to the ACU by the controller overlaps the last portion of the FAC-STROBE that brought the partition number. As the FAC-STROBE leaves, the decending transition increments the A counter in the controller to A=2. In the meanwhile, during A=1, the time between sector pulses was determined by the WRITE COUNTER, and the proper oscillator was chosen to match the speed of rotation in the drive. This part of the operation only happens during a WRITE operation.

In A=2 the ACU has stepped to R/W 13 (because of the ACK in R/W 12) and sends the partition number again. This time no checks are made, and no acknowledgement is made. The controller stores the partition number in the partition register of the selected half of the DDC card. The C and D registers in the controller are cleared to accept new data. The controller A counter increments to A=3 as the FAC-STROBE pulse falls.

SEEK

The ACU steps to R/W 14. In R/W 14 the Q counter (in the ACU) is used to send the remaining five characters of the disc address from the B core address. With the Q counter at Q=Ø (R/W 14) the ACU sends the second character of the disc address, which is the most significant digit of the cylinder address, and the head pair number. The character is accepted by the controller (in A=3) and the upper three bits (M2, M3, and M4) are strobed (by FAC-STROBE) into the head register. The lowest bit (M1) is put into the C register as the first portion of the cylinder number. At the same time, the controller generates TAG 1 and FB 3 for the disc drive. These two signals cause the disc drive to clear its head register. Providing there are no FAULT conditions, the controller increments to A=4 on the downward transition of the FAC-STROBE pulse. In the processor, the Q counter steps to Q=1. The next character of the disc address is placed on the M and N lines, and an FAC-STROBE is given. This character is the tens digit of the cylinder address, and is placed into the C register along with the output of an adder that is converting the decimal number that is received to a binary number in the C register. During A=4, the CAR (Cylinder Address Register) value from the disc unit is loaded into the D register. If there are no FAULT conditions, the A counter increments to A=5 on the downward transition of the FAC-STROBE. The Q counter in the ACU increments to Q=2 (still in R/W 14).

The ACU sends the next character, which is the least significant digit of the cylinder address. This is loaded by the controller into the C register, along with the conversion factor from the first two digits, and completing the cylinder

12-6.3 WRITE INSTRUCTION

SEEK (Continued)

address in binary form. As the FAC-STROBE signal falls, the A counter increments to A=6; the Q counter in the ACU goes to Q=3. The ACU sends the next character from memory. This is the most significant digit (MSD) of the sector number, and the odd or even value of the head pair. If the MSD is less than 5 the head is even numbered; if the MSD is 5 or more, the head number is odd. This part of the selection is made by ring-shifting the digit and head number back onto itself.

In A=6 the difference between the value in the D register (the current cylinder address from the disc unit) and the value in the C register (the desired cylinder address from software) is determined to see if a seek is necessary. The determination is made by complementing (with the 9s complement) the value in D, and adding it to the contents of the C register. If there is a carry from the adder, FAYC is set, and will cause a forward seek by bringing up FBØ to a logic 1. If FAYC is not set, FBØ is a logic Ø; either no seek is necessary or a backward seek (to a lower track number) will be made. The added number is re-loaded into the D register. If no FAULT conditions are present, the A counter increments to A=7 and the processor Q counter goes to Q=4 on the downward transition of FAC-STROBE.

In A=7, TAG 3 is generated, causing the disc drive to load the head number into its head register, and enter the value of FBØ into the direction flip-flop. While this is going on, the ACU sends the next character, which is the LSD, or units digit, of the sector number. This digit, along with the MSD that was received in A=6, is placed into the controller sector register. Also in A=7, a decision is made to add or not to add the compliment to the contents of the D register. If FAYC is set, the value in D is the true value. And since the disc unit requires the compliment value, the number must be complimented before it is sent. The decision to seek is also made in A=7 if D does not equal zero. On the falling transition of FAC-STROBE, the A counter is incremented to A=8, the processor Q counter is incremented to Q=Ø, and the ACU steps to R/W 15.

In R/W 15 the ACU loads the processor B register with a value of 100, the hardware-fixed number of characters that will be transfered in a disc record. The processor cycle is very short for this operation, and no FAC-STROBE is sent. The ACU steps to R/W 16.

In R/W 16 an FAC-STROBE is sent to the controller, which when qualified by A=8, sets A8ON. A8ON allows the controller to continue operating for a time, even though under some conditions, the ACU may disconnect. The FAC-STROBE that is received in A=8 also loads a value of 240 into the controller character counter. If TERM-TRANS is active at this time, the requesting partition has been reading or writing (the DISC ACCESS flip-flop is set) and is asking for a second seek. The TERM-TRANS signal clears the controller and the instruction is not completed until the partition is serviced again. If the DISC ACCESS flip-flop in the ACU is not set, and a seek is required, the controller continues the seek sequence. In either case, the ACU decrements the tens digit of the P count, and stores it away (in SW3), then switches out to service other partitions (while the seek is being made). Notice that a seek is not started if the partition is requesting a second seek. However, when the partition is serviced again, the DISC ACCESS flip-flop will have been reset, and the seek will be started (providing another

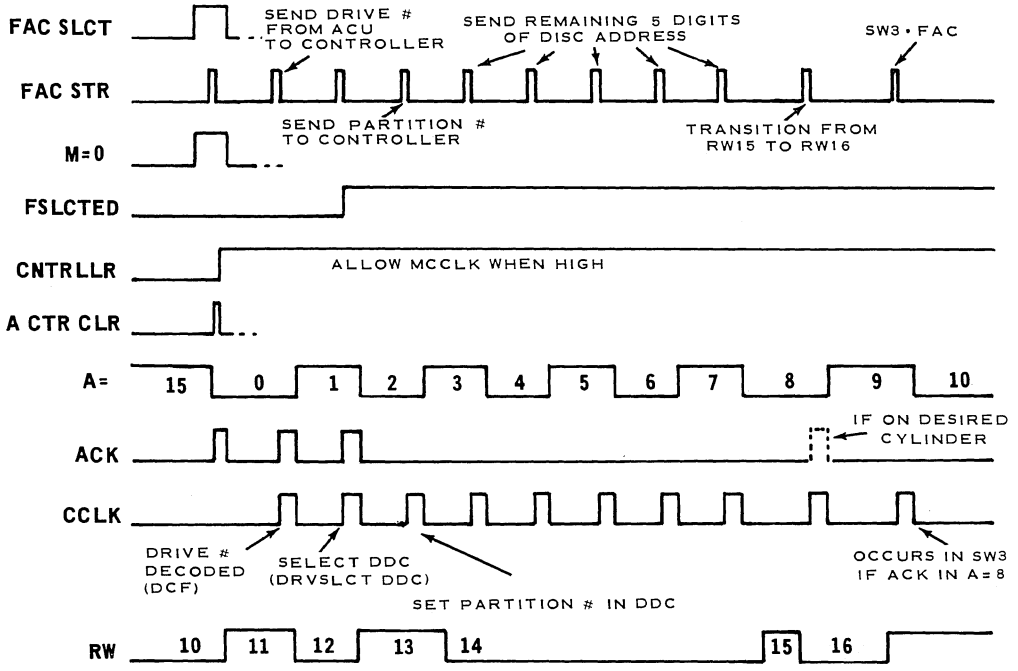
12-6.3 WRITE INSTRUCTION

SEEK (Continued)

partition has not reserved the drive in the meanwhile, and started a seek). As the FAC-STROBE (from the beginning of R/W 16) falls away, the A counter increments to A=9.

In A=9, the seek command is given. The character counter is enabled, and once it is started, it will continue to run. The character counter is driven by the bit counter (BC) every BC6 time. The character counter was initially loaded with a value of 240 (in A=8); when it reaches 242 (CC2MOD16) with A8ON and ONCYP not set, TAG 2 is generated. TAG 2 sets the value in the C register (the cylinder address) onto the file bus lines, so that the disc drive can load the CAR (Current Address Register). This is the only way the CAR is changed; the disc unit can only clear it. The TAG and BUS values are withdrawn as the character count is increased from 242. The count continues to be incremented until it reaches 246 (CC6MOD16). At that time TAG 4 becomes active. Tag 4 sets the difference compliment (from the D register) onto the file bus lines. The disc drive loads the difference register. Continuing to count, the character counter reaches 248 (CC8MOD16). CC8MOD16 and not ONCYLINDER generates Tag 1 (Control), and FB 2, telling the disc drive to seek. The RDY signal is withdrawn by the disc unit as the seek is started. The character counter reaches 255, and one count later CCCARY is generated. CCCARY and D≠Ø and A8ON sets DELTA RST, clearing the controller. DELTA RST sets STATUS RST, and the A counter is forced to a value of 15, or IDLE. The disc controller is now free for use by other partitions. The time in A=9 when a seek is being initiated is the situation that could be found in R/W 10, where the controller is busy. This situation is the exception rather than the rule, and only a small delay is experienced because the instruction is repeated when the partition is serviced again.

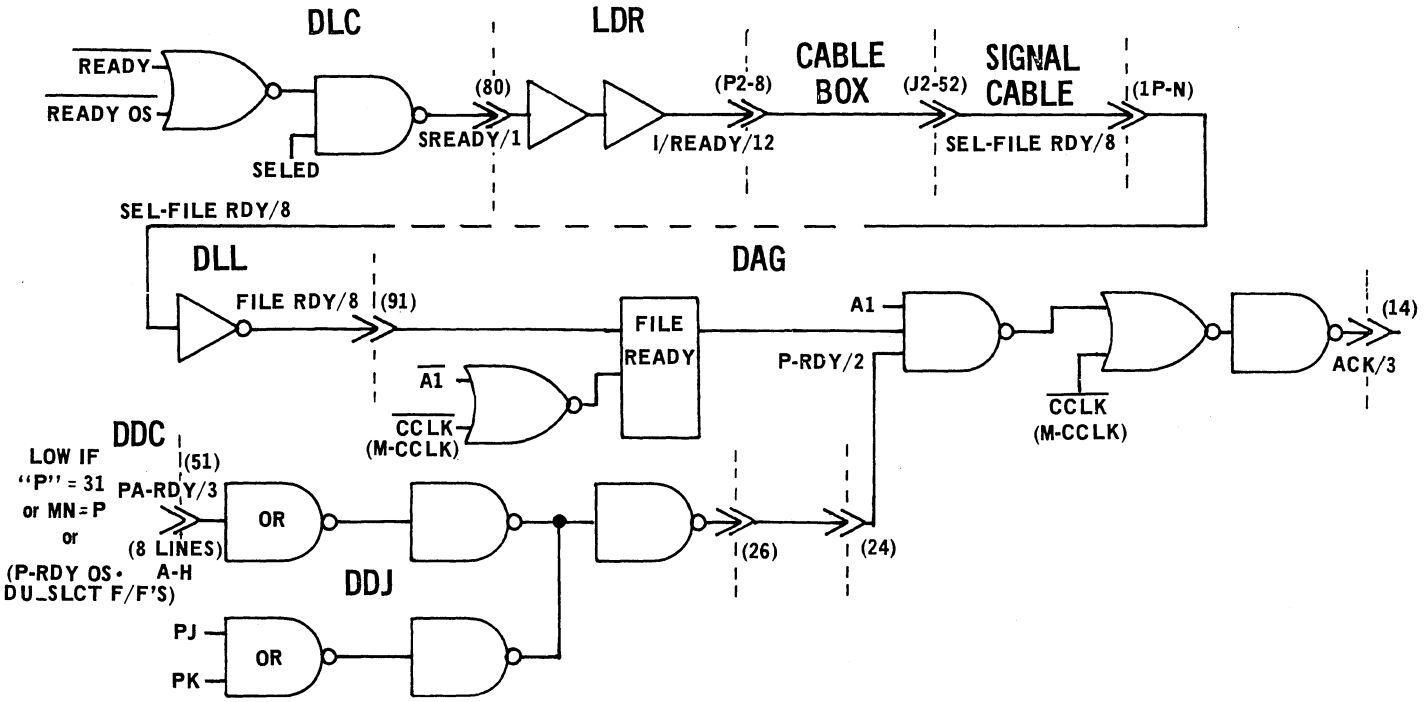
The timing chart below is a summary of the relationship of the signals that are involved in a normal select and seek operation.

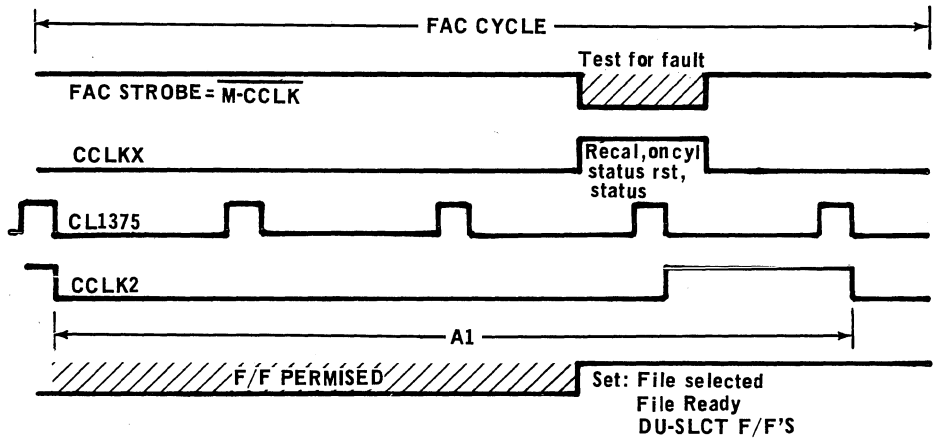


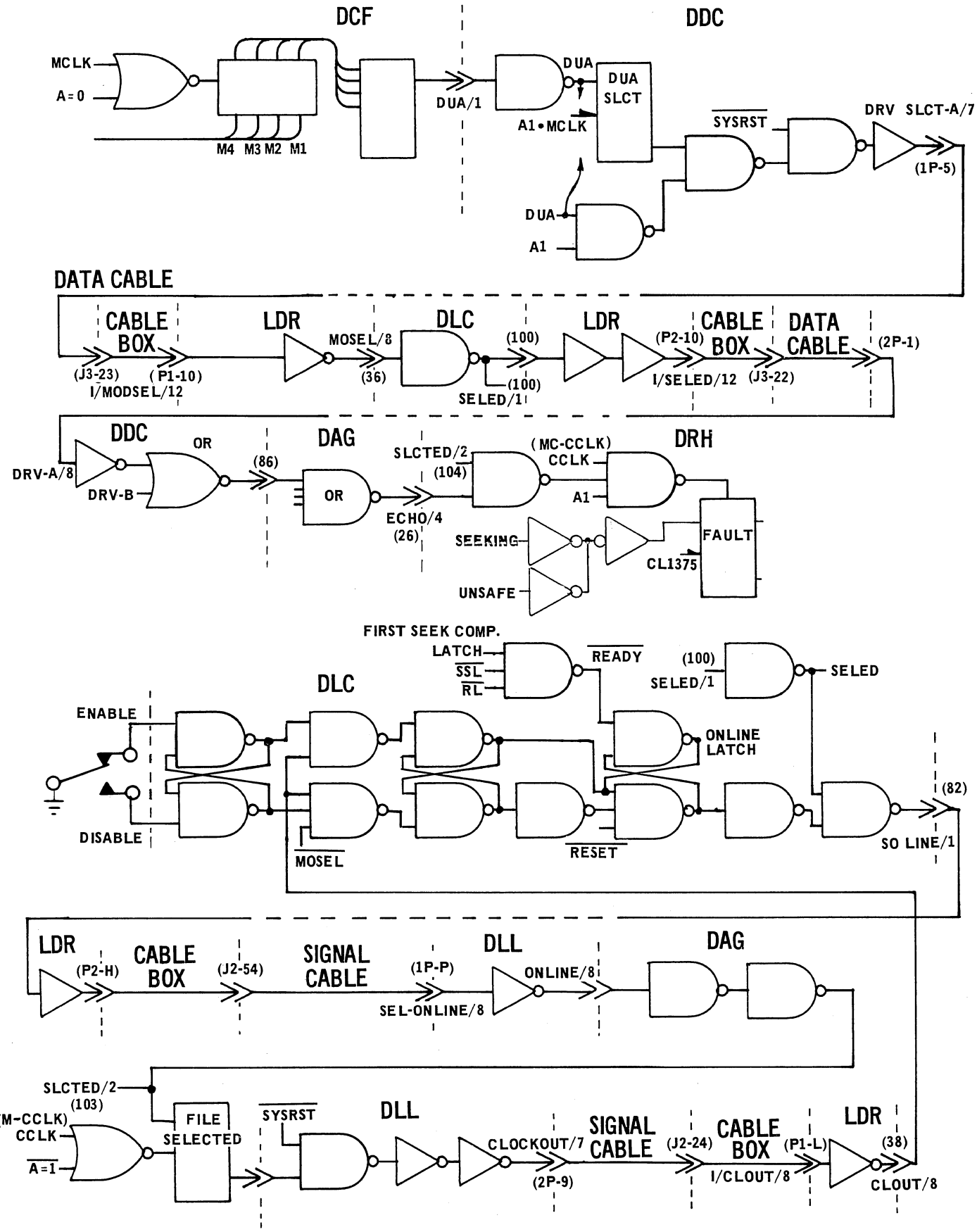
12-6.3 WRITE INSTRUCTION

SEEK (Continued)

The logic diagrams on these two pages show the logic that is involved in the seek process and the check for FAULT. The logic that is shown is simplified, and is physically a part of both the disc unit and the controller. The disc unit logic is part of a Model 40. If other models are used, the same signals are produced in a similar manner.






DCF
DDC
MCLK
A=0
M4 M3 M2 M1
DUA/1
DUA
DUA SLCT
A1•MCLK
SYSRST
DRV SLCT-A/7
(1P-5)
DUA
A1
DATA CABLE
CABLE BOX
(J3-23)
(P1-10)
I/MODSEL/12
LDR
MOSEL/8
(36)
DLC
(100)
(100)
SELED/1
LDR
(P2-10)
CABLE BOX
I/SELED/12
(J3-22)
DATA CABLE
(2P-1)
DDC
OR
DRV-A/8
DRV-B
(86)
DAG
OR
SLCTED/2
(104)
ECHO/4
(26)
(MC-CCLK)
CCLK
A1
DRH
SEEKING
UNSAFE
FAULT
CL1375
FIRST SEEK COMP.
LATCH
SSL
RL
READY
(100)
SELED/1
SELED
DLC
ENABLE
DISABLE
MOSEL
RESET
ONLINE LATCH
(82)
SO LINE/1
LDR
(P2-H)
CABLE BOX
(J2-54)
SIGNAL CABLE
(1P-P)
SEL-ONLINE/8
DLL
ONLINE/8
DAG
SLCTED/2
(103)
(M-CCLK)
CCLK
A=1
FILE SELECTED
SYSRST
DLL
CLOCKOUT/7
(2P-9)
SIGNAL CABLE
(J2-24)
CABLE BOX
I/CLOUT/8
(P1-L)
LDR
(38)
CLOUT/8

12-6.3 WRITE INSTRUCTION (Continued)

ON CYLINDER

The disc unit heads may be on cylinder as a matter of chance, but more likely a seek was initiated earlier and is now complete, or another READ or WRITE was made within the same cylinder location. A partition can READ or WRITE within the same cylinder without limitation if no sucessful branches in program are made, and the monoply is lost only when a seek must be made. During this time, the ACU does not pull new instructions; only I/O data transfers are serviced in INTerrupt.

In R/W 16, A=8, if a seek is not necessary, the B count in the processor is decremented by one count, making the number 99. The controller gives an ACK to the ACU indicating that the disc is oncylinder, and a data transfer is about to take place. The ACU jumps to SWitch, giving an FAC-STROBE to the controller. The ACU transfers the contents of the P register to P-protected, then transfers the contents of the ACU A register to the P register. The A register in the ACU must be emptied, as it may be used for core address during INTerrupt cycles for I/O channels. The P register in the ACU is used to address core for the FAC device (in this case the disc controller).

Within the controller, the character counter is loaded with a value of 240. This will be counted to allow time for the necessary operations before data is transfered. On the downward transition of the FAC-STROBE signal, the A counter is incremented to A=9.

In A=9 with the disc oncylinder, CONTROL is set. CONTROL brings up TAG 1. FB 5 is generated, which is the "select head" line. The character counter continues to count until CCCARY is generated (at 255) clearing A8ON. With A8ON reset (and no FAULT conditions) the next FAC-STROBE increments the A counter to A=10. That FAC-STROBE is provided when the ACU steps from SW3 to INTerrupt, looking for interrupt requests before the FAC transfer begins. There will be a small wait for CCCARY, as the character counter takes longer than the time that is required by the ACU in SWitch. When CCCARY does take place, and the heads are still on cylinder, DELTA SEARCH is set. DELTA SEARCH allows a search for the particular sector that is being addressed. By comparing the value from the sector register in the disc controller to the sector counter on the DDC card, the sector can be located. When the count is equal, SCMP (sector compare) is set, bringing up FSCMP (File Sector Compare). FSCMP brings up RES-MEM so that the ACU will stop in INTerrupt (by stopping the State Clock) and be dedicated only to the disc transfer.

WRITE LEADER

In A=10, the signals $\overline{\text{RDS}}$ and FSCMP produce BUS Ø. BUS 5 is also active at this time, selecting the head in the disc head register. With the character counter setting at zero (because it had reached CCCARY) when FSCMP became active, the bit counter started running. The bit counter increments the character counter each BC6 time. The bit counter itself is incremented by CL1375. Initially the BX and BY registers are cleared, and when the bit counter and characters are running, the contents of BY are strobed to BX each BC6 time. The BX register is clocked onto the WRITE DATA coax from the DDC card. Thirty six zeros are sent out as a leader by holding the BY register clear. This transfers all zeros to the BX register each BC6 time. When the character count reaches 5, and the bit count is 5, the BY register is preset to all 1s. One bit count later at BC6, BY is strobed to BX and the character counter is incremented to CC=6. The cylinder address lower digits

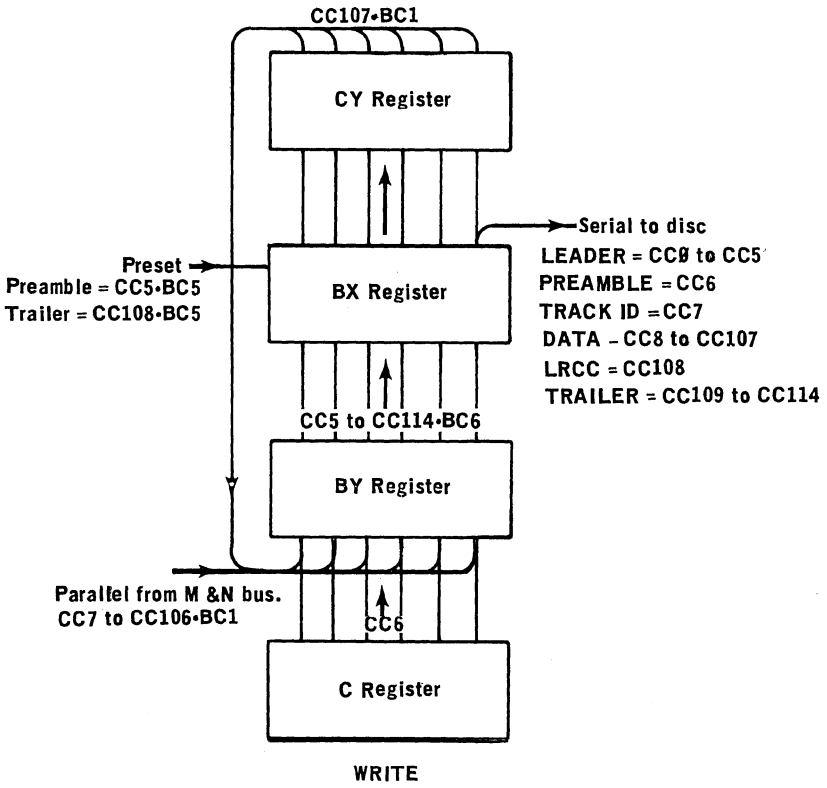
12-6.3 WRITE INSTRUCTION

WRITE LEADER (Continued)

(2, 3, 4, 5, 6, and 7) are loaded into the BY register from C, the cylinder register. The C1 digit remains in the C register and was used during the seek, but is not written on the disc because the track ID is limited to six bits of information. The C1 digit is the most significant bit of the cylinder address and the likelihood of a track error of exactly 64 is very small. The figure is a simplified illustration of the data flow between registers.

WRITE DATA

As the bit counter steps from BC6, the AFTER6 flip-flop is set, indicating that the controller is in a data mode, and is ready to write data. CY is cleared when the character counter reaches CC=7, and BC6 time. CY-REQ is set, requesting a character from the ACU. The character arrives with FAC-STROBE and is placed into the BY register. FAC-STROBE resets CY-REQ. This process continues throughout the data portion of the recording process. Each BC6 time, CY-REQ is set, BY is strobed to BX, and at BC1 time the value in BY is strobed to CY for the LRCC accumulation.

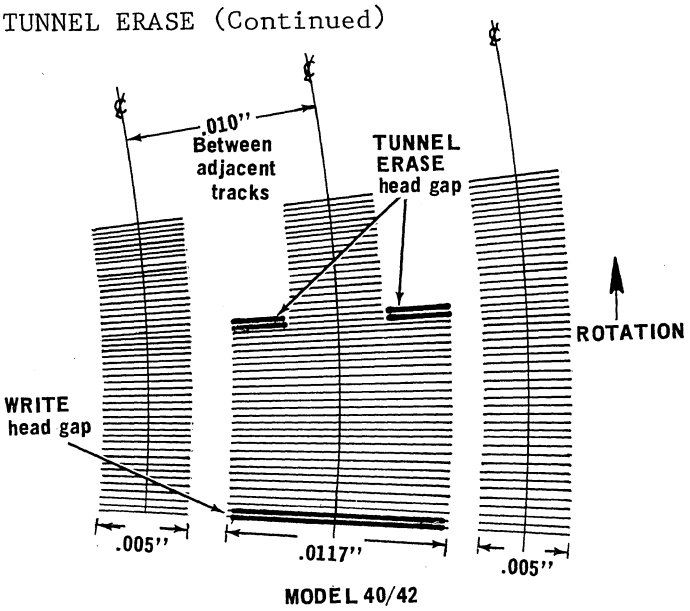


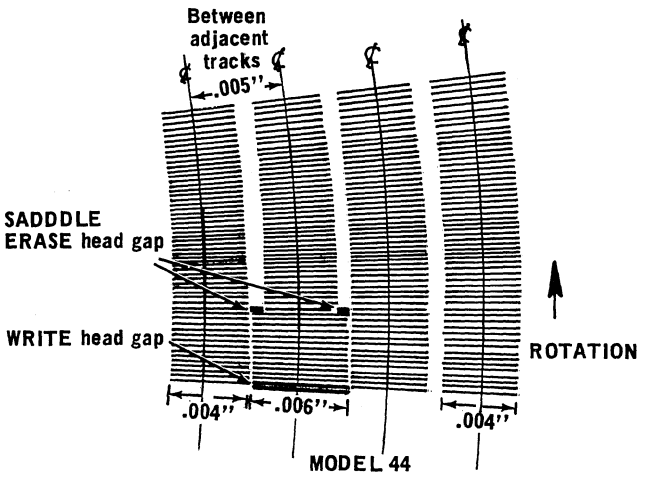
TUNNEL ERASE

Data that is written on the disc surface is recorded by a head that is wider than is necessary. It is also wider than normal track spacing would allow. The extreme edges of a recorded track on any magnetic media are not sharply defined, and add little to the quality of the reproduced signal. Consequently, after the track is recorded (written) the recording track on the disc is "trimmed" by a tunnel erase procedure (called "saddle erase" in the Model 44). The effective width of the recording (write) head in the Model 40 and Model 42 is slightly less than .012" (.0117), and is .006" on the Model 44. In both cases the track is trimmed to .005" wide with a center-to-center spacing of .010" for the Model 40 and Model 42, and .005" for the Model 44. The illustrations at the top of the following page show an example of a track that is being recorded and "trimmed". In the actual hardware, the erase heads are spaced farther behind the recording head. However the relative size and spacing of the tracks are drawn to approximately 100:1 scale.

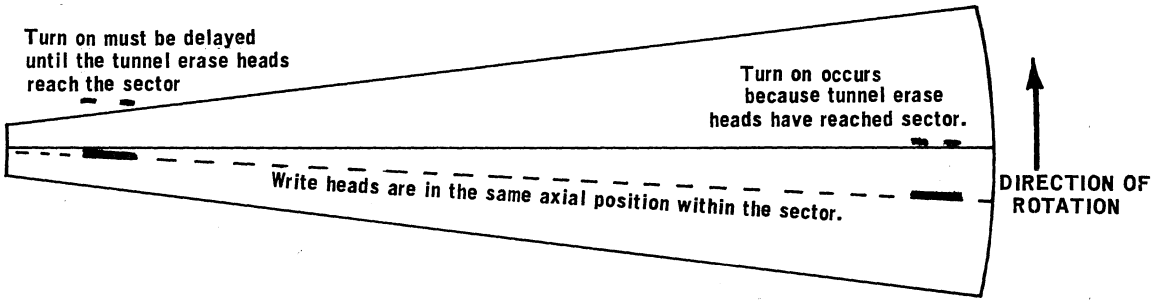
12-6.3 WRITE INSTRUCTION

TUNNEL ERASE (Continued)



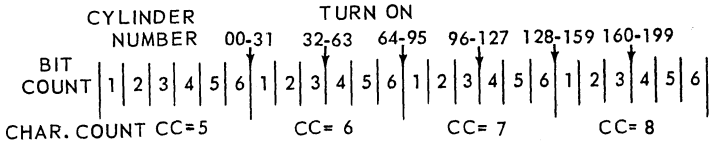


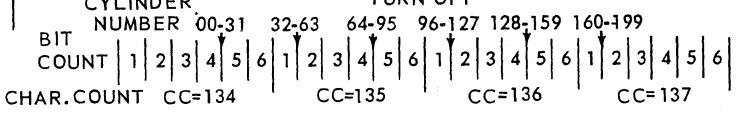
Because the track diameter is less toward the center tracks and greater toward the outer tracks, the surface speed and bit density varies. The tunnel erase heads have a mechanically fixed space behind the recording head (.045" for the Model 40 and Model 42). The figure below illustrates that, while a delay is needed before the erase heads reach the sector, the delay is different for the inner and outer tracks. The figure is exaggerated to show this effect. With the record heads at



the same axial position, the erase heads reach the sector much earlier in the outer tracks than in the inner tracks. Once it is started, the tunnel erase takes the same amount of time to cover the sector, so the beginning and end of the tunnel erase is delayed by the same amount of time.

The turn-on and turn-off time for the tunnel erase heads is controlled by the cylinder number and the character counter. This computation is done, and the control signals generated, on the DCF card by the TNNL flip-flop and decoding gates. The turn-off delay is identical to the turn-on delay, making the tunnel erase time approximately equal to a sector time. The cylinder numbers are divided into six groups, and the turn/off times are shown in the chart below.





12-6.3 WRITE INSTRUCTION (Continued)

WRITE TRAILER

When the character count reaches 107 (six characters in the leader, one character preamble, and 100 data characters) the AFTER6 flip-flop is reset. With the character counter at 107, BC6, and $\overline{RDS}$ (indicating a WRITE operation) the contents of CY register (the LRCC) is loaded into BY. Writing still continues by strobing BY to BX as it has been. At CC=108, and BC5 in a WRITE operation ($\overline{RDS}$) the BY register is preloaded with all 1s. At this point, BY is no longer loaded by clocking bits into it. Instead, the 1s remain, and each BC6 time the BX register is filled with all 1s. The result is that a continous string of 1 bits is written on the disc until the next sector pulse is detected (which is usually 4 to 6 character times).

When the sector pulse is detected, FSCMP being set causes the character counter to be loaded with a value of 128. The sector pulse resets FSCMP, which withdraws FBØ. The character counter continues for the tunnel erase process. The ACU stays in INTerrupt, servicing INTerrupt requests from other partitions, while it waits for STATUS-RDY from the disc controller. At a character count of 136, and BC6 time, the STATUS flip-flop is set. STATUS develops STATUS-RDY which is recognized by the processor in IT 3, causing it to jump to SWitch. In SW 6 it will restore itself by reloading the P register, then stepping to SW 7 where the status is pulled by FAC-STROBE. The FAC-STROBE generates a clock signal (CCLK2) within the controller. With CCLK2, FAC-STROBE, and STATUS set in A=10, the STATUS RESET flip-flop is set, which will clear the controller. STATUS RESET causes the A counter to be loaded with a value of A=15, the idle state, and all conditions that were set within the controller are cleared. With $\overline{RDS}$, indicating a WRITE operation has just been completed, the WRITE TALLY counter is incremented at the time status is given. The WRITE TALLY counter is not cleared by STATUS RESET when the rest of the controller is cleared. Meanwhile the ACU looks at the status indication. If this was the first time the WRITE operation was completed, the status indication will have been forced by the controller to ERROR and REPEAT IF ERROR. This forces the instruction to be pulled again for the check read operation.

12-6.4 READ INSTRUCTION

The READ process is identical to the WRITE process, up to controller state A=9. To reach A=9, the ACU has just left R/W 16, the heads are on cylinder, and the proper head is selected. During a READ operation RDS is set, giving FB 1 instead of FB Ø. As the controller left A=8 to go to A=9, the character counter was loaded with a value of 240. It is allowed to count incrementing each BC6 time. Meanwhile the ACU is in SWitch, storing P and loading the contents of the A register (in the processor) into the P register (to free the A register for IOC data transfer in INTerrupt) then it jumps to INTerrupt. As the jump is made, an FAC-STROBE is given to the controller. Providing there are no FAULTs, the A counter (in the controller) steps to A=10 on the downward transition of FAC-STROBE.

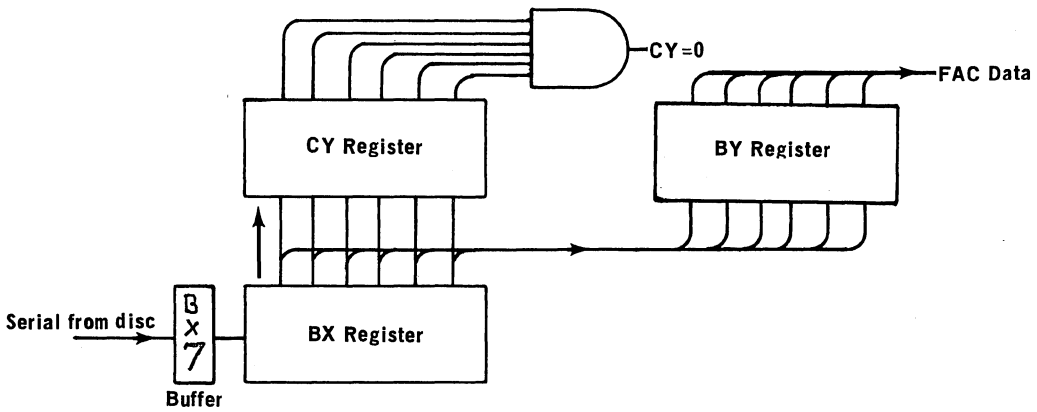
In A=10 the signal CCCARY is produced by the character counter (see ONCYLINDER for details on how this happens). CCCARY, when the heads are on cylinder, sets the flip-flop DELTA SEARCH. DELTA SEARCH allows the controller to begin looking for the proper sector. When the proper sector is reached, and FSCMP is set, A8ON is reset. FB 1 is active at this time, and the controller is looking for a com-

12-6.4 READ INSTRUCTION (Continued)

pare of the track ID that will be read from the disc. Before the track ID is read however, the leader and preamble must be detected, and the controller must be synchronized to the incomming data. This is done by the de-serializer network on the DMK card and the BX register.

The de-serializer network consists of WINDOW, MISSING CLK, DATA 1, and DATA 2 flip-flops. As the leader clocks come into the controller, they are placed in the BX register, the serial-in-serial-out register. BX was set to all 1s at the beginning of the READ operation. When the leader clocks have filled BX with all zeros, the Read State Counter is incremented to S1. No further action is taken until the preamble enters BX, making the contents all 1s again. A signal called BX=63 is generated, and the Read State Counter is advanced to state 2; the character counter is set to CC=6. At the next BC6 time, the one-character track ID has been read, and is compared with the track address. The track address is in BY (from the C register) and the character from the disc is in BX. If they do not compare, TRACK CHK is set. TRACK CHK generates ERROR status.

After the track ID, data begins to come into the controller. The illustration below shows the flow that takes place during a READ operation. Each character



READ

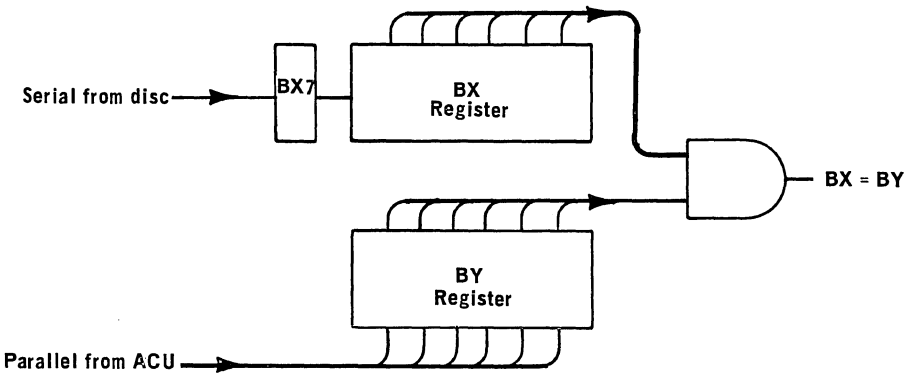
comes serially into the BX register and at BC6 time it is parallel strobed to BY. Each BC1 time the contents of BY is strobed to CY for the LRCC accumulation. When the character is transfered to BY (at BC6 time) the CY-REQ signal is raised to the ACU. The ACU checks FØ, and if FØ is off (logic Ø) the operation is a READ, and the character is taken from the controller. When receiving data from the disc, the BX register has an extra flip-flop (BX7) that acts as a timing buffer for the incomming bits. BX7 is used only during the serial transfer into the register and is not strobed to the BY register.

When 100 characters are transfered from the disc (CC=107) the LRCC is read from the disc. This is done while the ACU is picking up the last data character. At CC=108, BC1 time, the LRCC character from the disc is strobed from BY to CY. If the result is zero, the LRCC comparison is correct. When the sector pulse arrives, the character counter is set to 128. At this point, the closeout is identical to a WRITE operation (see the last paragraph of ONCYLINDER).

12-6.5 CHECK READ

After each WRITE operation, ERROR and REPEAT IF ERROR status is set by the controller. This causes the ACU to ignore the ERROR status and repeat the same instruction.

The WRITE instruction is received by the controller, but because the RDS flip-flop was set at the end of the WRITE (recording) operation, the controller now reads from the disc instead. The ACU still follows the WRITE instruction, sending a character from memory each time CY-REQ is raised by the controller. The character from memory is compared to the character from the disc to verify that the information was written properly on the disc. The illustration below shows the flow of



COMPARE

data in the compare circuits. All 100 characters of data are compared - one by one. The LRCC is accumulated from the ACU data and compared with the LRCC from the disc. If any character does not compare, ERROR is set and reported in the status character at the end of the operation. When ERROR is reported, the REPEAT IF ERROR is also reported unless the Write Tally Counter has reached a count of three. If the Write Tally Counter has reached three, the BLOT circuitry is placed into effect (see BLOT below). During a standard (not Check Read) the Read Tally Counter is incremented to keep track of the number of retries. During Read Check the Read Tally Counter is not toggled, as this function is taken care of by the Write Tally Counter during the WRITE operation.

BLOT

Each WRITE instruction has a Check Read operation as described above. If the Check Read does not compare, the WRITE operation is repeated, followed by another Check Read. Each time the WRITE operation is performed, the Write Tally Counter is incremented. When the Write Tally Counter reaches 3, a signal is generated called WTC3. It is assumed at this point that the sector that is being written is a bad sector on the disc. A bad sector is marked with a BLOT.

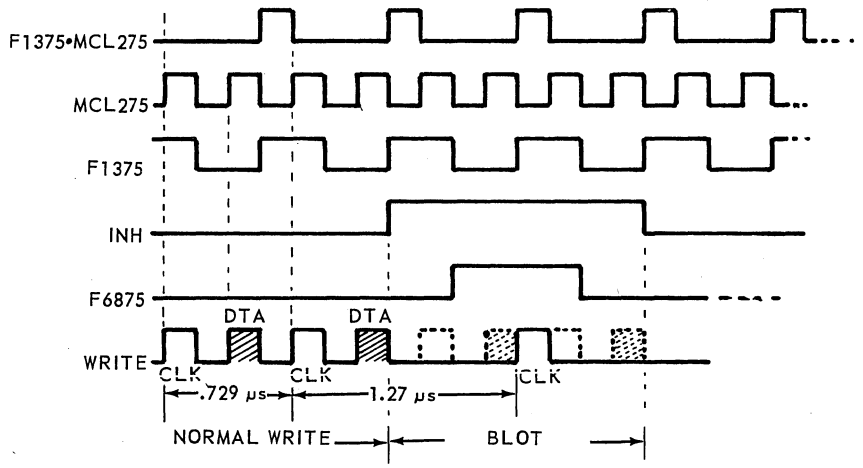
A BLOT is a unique spacing of spacing of clock pulses that are 1.27 usec appart. The spacing causes the missing clock oneshot to time out when the sector is read, setting FLAG status to signify a bad sector.

The BLOT is generated by two JK flip-flops on the DMK card that "stretch" the timing between clock pulses. The Model 40 and 42 use these clocks directly, but the Model 44 constructs a BLOT pattern of its own, which is reconverted when it is read back by a Model 44. The timing relationship of the BLOT waveform to the

12-6.5 CHECK READ

BLOT (Continued)

signals that generate it is shown in the figure below. The first part of the waveform shows a normal WRITE pattern for all 1s. The dotted blocks in the second half of the waveform are the expected clocks and data pulses. Notice that the BLOT clocks are spaced so that they do not come at either a normal clock or data pulse time.



12-6.6 DXH READ-BEFORE-WRITE

The DXH card has the special ability to test the track ID before data is written on the disc. However this means that the disc pack that is used with a controller containing a DXH card must be initialized by writing the track ID on every sector. A pack that is only partially written on will cause FLAG status each time a blank sector is selected for a READ or a WRITE.

When a write instruction is received by a disc controller that contains a DXH card, a flip-flop called TRKRD (track read) is set. TRKRD is unique to the DXH card and forces the Read Tally Counter to a count of three (RTC3). It also sets RDS, ERROR, and REPEAT IF ERROR so that the first operation will be a READ (similar to a Check Read) and the instruction will be repeated. When the heads are reported on cylinder, the FSCMP flip-flop is forced set by the first available sector, causing it to be read. The preamble is detected as it is in a normal READ operation, and the track ID from the disc is brought into the BX register. This character is compared with the cylinder number that is in the BY register (brought there from the C register).

If the track ID compares, RDS and FSCMP are reset, and the instruction is ended in ERROR and REPEAT IF ERROR status, causing the instruction to be repeated again. When the instruction is pulled again by the ACU, the heads will be found on cylinder, and DELTA SEARCH is set. The sector is found by the sector counter and the operation continues as a normal WRITE. The Check Read operation follows every normal WRITE operation the same as it does with a DRH card.

If when the read-before-write comparason is made, the track ID does not compare (in Read State 2), the controller sets TRACK CHECK, directs the disc unit to re-

12-6.6 DXH READ-BEFORE-WRITE (Continued)

calibrate, and aborts the instruction in ERROR status.

The read-before-write is made in the first available sector. If it occurs that sector is a blot or is not recorded, the controller can not synchronize with the leader and preamble, and the missing clocks do not allow the Read State Counter out of state zero. In this case the BLOT-RTRY flip-flop is set, and the instruction is ended in ERROR and REPEAT IF ERROR. FLAG was also set because of the blot or unrecorded sector, but the FLAG status is not seen by the ACU because of the ERROR and REPEAT IF ERROR. The instruction will be repeated.

When the instruction is pulled again, the heads are found on cylinder and DELTA SEARCH is set (RDS remains set from the last operation). Because the BLOT-RTRY flip-flop is set, TRKRD is not set and FSCMP is not forced as it was on the first attempt at reading the track ID. Instead, the proper sector is located and the track ID is read (after synchronizing on the leader). The track ID is compared to the desired number in the BY register and the instruction is ended. FLAG status is set if the controller is unable to synchronize on the leader because of missing clocks; the assumption is that the sector is either a blot or is unrecorded. ERROR and REPEAT IF ERROR remain set at the end of a good compare, so that the instruction will be pulled again and repeated as a normal WRITE.

12-6.7 WRITE CONTROL

A WRITE CONTROL instruction to a disc controller that contains a DRH card will be treated as a WRITE instruction; the control bit is only acted upon by the DXH card. When a WRITE CONTROL instruction is received by a disc controller that contains a DXH card, the control bit disables the special read-before-write features within the DXH card, and the instruction is treated as a WRITE instruction in the DRH card. There will be no read-before-write check of the track ID, and data will be written on the selected sector.

12-7.0 LOGIC CARDS

The following descriptions list the major fumctions and features of the individual logic cards within the Disc Controller.

12-7.1 DDC

Dual Disc Controller. Each half of the DDC card is complete within itself. The unit address selection (fed by the DD register on the DCF card), partition register and sector counter are located within the one half of the card that interfaces the individual drive address. The interface to the drive address is through one of the two edge connectors and a cable. A drive address for the Model 40 and Model 42 is one complete drive unit; a drive address in a Model 44 is one of the four volumes.

The partition number of the requesting partition is stored in the P register of the DDC card that interfaces to the requested drive. The number (partition) is sent to the controller as a binary number on the M and N lines. However, the N1 bit is the least significant bit (binary weight of 1) and the M1, M2, M3, and M4 bits are assigned binary weights of 2, 4, 8, and 16 respectively. The N2 bit is not used for the partition number. The chart at the left of the page shows the partition number codes as they would arrive in binary form from the ACU. When a disc drive is not in use by any partition, the partition register in the DDC card is cleared to an all 1s condition. A partition reserves a disc address throughout the seek and data transfer process. If the seek and data transfer are not completed within a period of four seconds, a timeout oneshot fires and that unit address is available to any partition that requests it.

Partition Number	Binary Code				
	M4	M3	M2	M1	N1
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16	1	0	0	0	0
17	1	0	0	0	1
18	1	0	0	1	0
19	1	0	0	1	1

12-7.2 DMK

The DMK circuitry controls the master timing for the entire Disc Controller. There are three crystal controlled oscillators that are individually selected according to variations in spindle rotation speed from unit to unit. The clock select circuits, clock seperator circuits, and BLOT gates are located on the DMK card.

CLOCK SELECT

Only one of the three crystal controlled oscillators are used at any one time and only during a WRITE operation; the clock pulses for a READ operation come from the disc. A counter samples the clock pulses during WRITE operations, and selects

12-7.2 DMK

CLOCK SELECT (Continued)

the oscillator that will provide approximately 685 pulses from MCL1375 between sector pulses. The table below shows the relationship of spindle speed to the oscillator that will be selected. If the MCL1375 pulses do not fall within the

Spindle RPM	Flip-flop	Oscillator	MCL1375 Pulses/sector
2345 - 2455	MIDSEL	2.75 Mhz	672 - 703
2289 - 2345	HIGHSEL	2.68 Mhz	656 - 671
2455 - 2510	LOWSEL	2.81 Mhz	704 - 719

Nominal spindle speed is 2400 RPM ±2.3%

chart, SRVLIMIT is generated, setting FAULT, because the spindle speed is outside normal limits. Decoded MCL1375 pulses are used to generate SRVNULL that is used in the FSCMP logic.

CLOCK SEPERATOR

During a READ operation, the seperator circuits are synchronized by the clocks and data bits from the leader that is being read from the disc. The first pulse sets RDCLK, firing two oneshots, one for the data window, the other for detecting missing clocks. On the downward transition of the first clock pulse, WINDOW is set, conditioning the clock input to DATA 1. Any data pulses that appear now will be stored in the master portion of the JK flip-flop and be reflected at the output when WINDOW is reset. WINDOW is reset when the oneshot expires, approximately .50 us after the onset of the first pulse. The output of DATA 1 is transfered to DATA 2 by the next pulse from the disc, which will be a clock pulse. The output of DATA 2 is sent to the BX register. In this way, any pulse that appears beyond the end of the clock pulse, and before WINDOW is reset, is considered a data pulse, or a 1 bit. If the time between pulses exceeds 1.0 us, the missing clock oneshot expires, setting RDCHK and incrementing the BLOT counter (clocks should appear every .729 us). If 16 of these timeouts occur, the BLOT counter overflows, setting FLAG status.

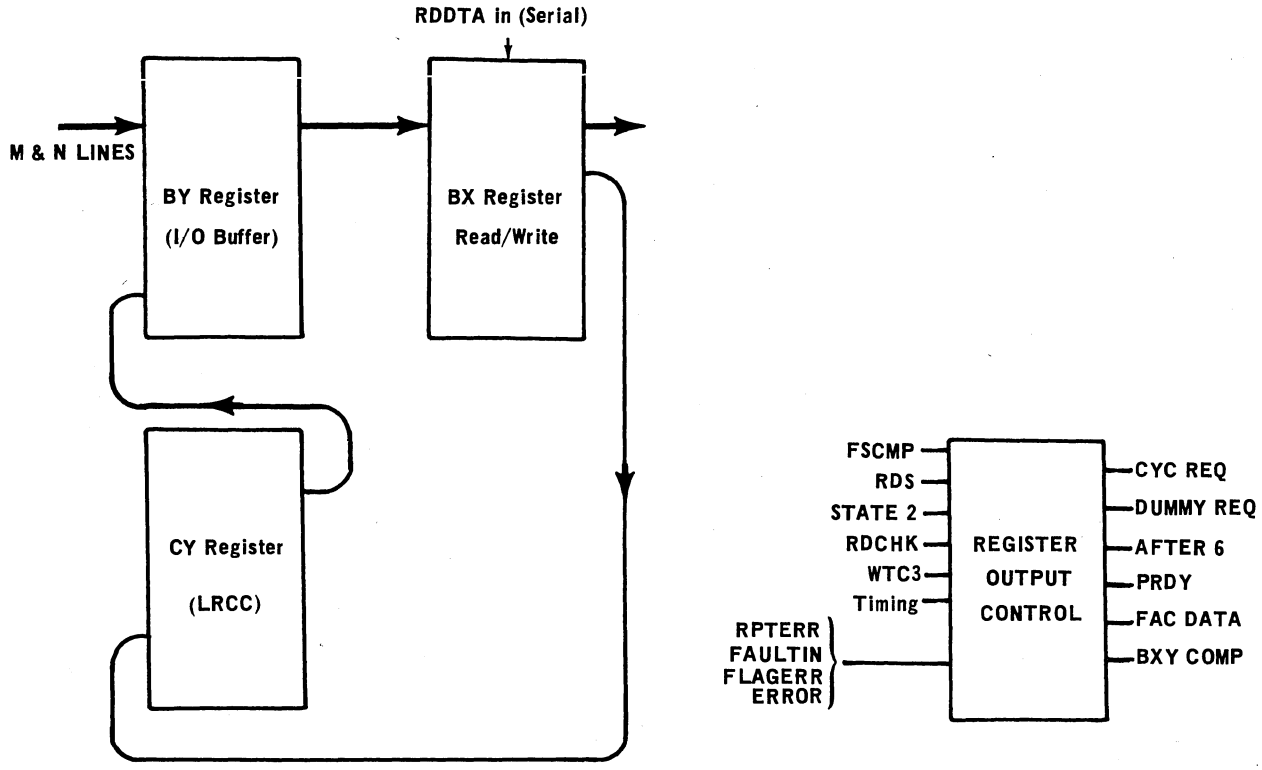
TEST SWITCH

The test switch on the DMK card should be in the downward position for normal operation. In the upward position, the STATUS-RDY signal is inhibited, and the controller is locked-up if any of the error condition flip-flops are set, RDCHK, DTAERR, TRKCHK, FLAG, or FAULT. The controller resumes normal operation when the switch is returned to the downward position.

12-7.3 DDJ

The DDJ card contains the buffering and parity check logic, BX, BY, and CY registers and the CYCLE-REQuest logic. The register uses and operation is explained in the paragraphs that deal with the overall operation of the controller. A short summary of each register use is given in the GLOSSARY at the end of this section. CYCLE-REQ is normally generated by CYCRQST, however if an error is detected during a READ operation, DMMYREQ is raised for the remainder of the operation. This is because in an error situation, clock pulses will not necessarily continue to come from the disc to trigger normal cycle requests. CYCLE-REQ must be held until the one hundred requests have been made, so that the ACU will raise TERMTR (terminate transfer). Terminate transfer is needed by the controller to clear the logic for the next operation.

The block diagram is a simplified summary of the main logic on the DDJ card.



DDJ CARD

12-7.4 DAG

The DAG card contains the file bus and tag control, the A counter, cylinder address conversion, and difference address computation.

FILE BUS & TAG LINES

Only one tag line can be active at any one time. The tag line sets the type of information that is represented by the file bus lines. The four basic types of information that will be presented on the file bus lines are: Control, Set cylinder, Head and direction, and Set difference. The table below shows the file bus meaning under each of the tag line settings. Notice that the cylinder difference is presented as the 1s compliment of the actual number, indicated as NOT before the digit.

FILE BUS	TAG 1 CONTROL	TAG 2 SET CYLINDER	TAG 3 HEAD & DIRECTION	TAG 4 SET DIFFERENCE
Ø	WRITE	CYL 128	FORWARD	NOT 128
1	READ	CYL 64		NOT 64
2	SEEK	CYL 32		NOT 32
3	RESET HEAD REGISTER	CYL 16		NOT 16
4	ERASE	CYL 8	HEAD 8	NOT 8
5	SELECT HEAD	CYL 4	HEAD 4	NOT 4
6	RETURN TO ØØØ	CYL 2	HEAD 2	NOT 2
7	ADVANCE HEAD	CYL 1	HEAD 1	NOT 1

12-7.5 DRH/DXH

The DRH logic card has been superseded by the DXH version of the same card. Both cards contain the same basic logic, with some additions and variations that make the DXH different.

The TRKRD and BLOT-RTRY flip-flops are unique to the DXH card and are explained in an earlier paragraph. The DRH and DXH cards contain the sector clocking and sector search logic, the bit counter, Read State Counter, the Read and Write Tally counters, the BLOT counter, and the status flip-flops.

The DRH/DXH card implements the sector search after the heads are on cylinder. After sector compare is made, the interplay between DLTASRCH and SECSRCH imposses a 70us delay before the operation is allowed to continue. This is accomplished by inhibiting FSCMP.

BIT COUNTER

The Bit Counter is used for internal timing and sequencing. It consists of three flip-flops, BC1X, BC2X, and BC3X. The flip-flop settings are not a simple progression, but are organized as a "Johnson" counter where only one flip-flop changes state for any one count. The flip-flop decoding is given in the inset table. The bit counter will always count (from the CL1375 signal) whenever the decoded value of the bit count is anything other than BC1, or if the character counter is not equal to zero. Normal reset state for the bit counter is BC1.

BC3X	BC2X	BC1X	
0	0	0	BC1
1	0	0	BC2
1	1	0	BC3
1	1	1	BC4
0	1	1	BC5
0	0	1	BC6

READ STATE COUNTER

The Read State Counter is two flip-flops, RDSTE 1 and RDSTE 2, and is capable of counting from states 0 to 3. State 0 is the normal reset state. The Read State Counter steps to S1 during a read operation if six zeros are detected in the leader. It stays in S1 until the six 1s are detected in the preamble, then it steps to S2 to read the track ID. When the track ID is compared, S3 is entered for the data transfer. The S3 state is held until after the LRCC is compared, or if a TRKCHK is made during the operation, S3 is held through STATUSRT to increment the Read Tally Counter.

BLOT COUNTER

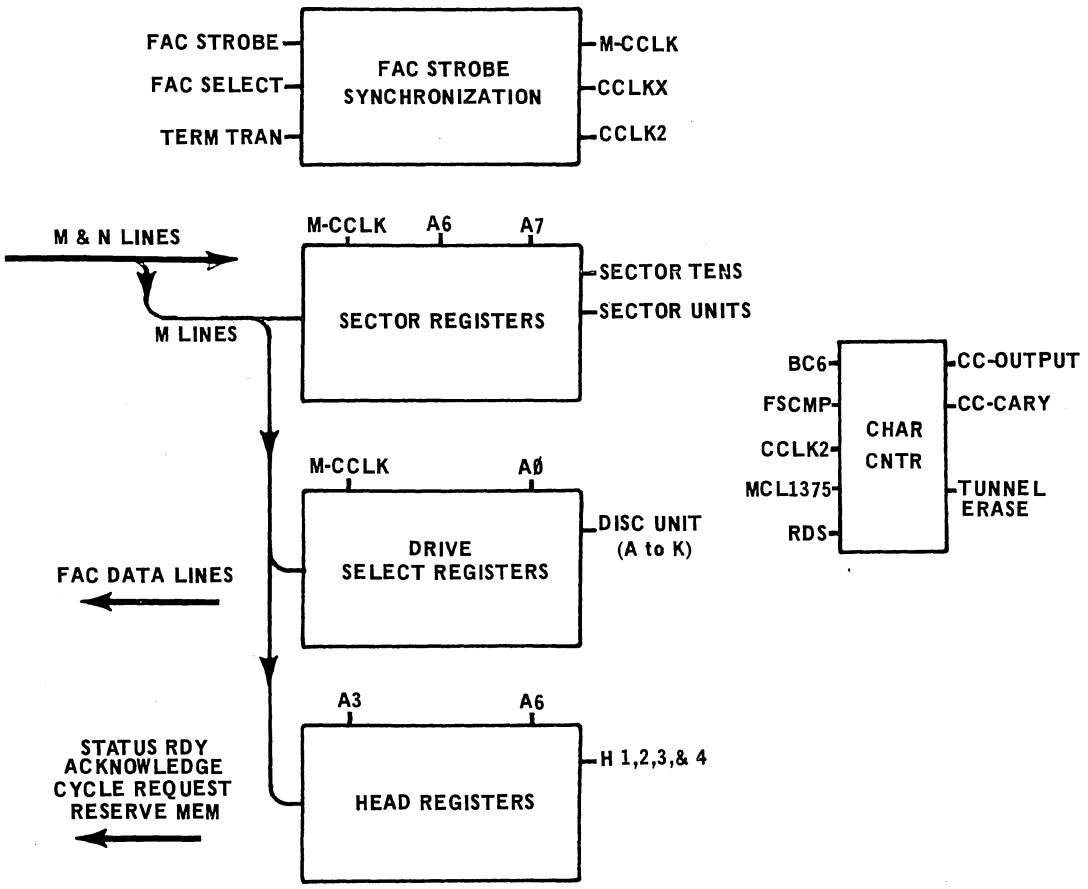
The Blot Counter is a modulus 16 binary counter. None of the counter outputs are used except for the carry. A BLOT is detected because the clock pulses from the disc are spaced longer apart than normal data bits. When the Blot Counter carry signal becomes active, it means that 16 or more missed clocks (longer than normal spaces between clocks) have been detected. BLTCARRY presets FLAG status.

12-7.6 DCF

The DCF card contains the clock synchronizing logic for the controller/ACU timing interface, the data inputs (M & N lines) from the ACU, the character counter, head register, disc drive (DD) register, sector register and the tunnel erase logic.

The controller is synchronized with the ACU by gating the FAC-STROBE signal with the internal controller clock signals. The FAC-STROBE is inhibited from the controller until the CNTRLLR flip-flop is set. CNTRLLR gets set by the downward transition of FAC-STROBE if the controller is being selected (i.e. FAC-SELECT and device number zero on the M & N lines).

A simplified block diagram of the major logic on the DCF card is shown below.



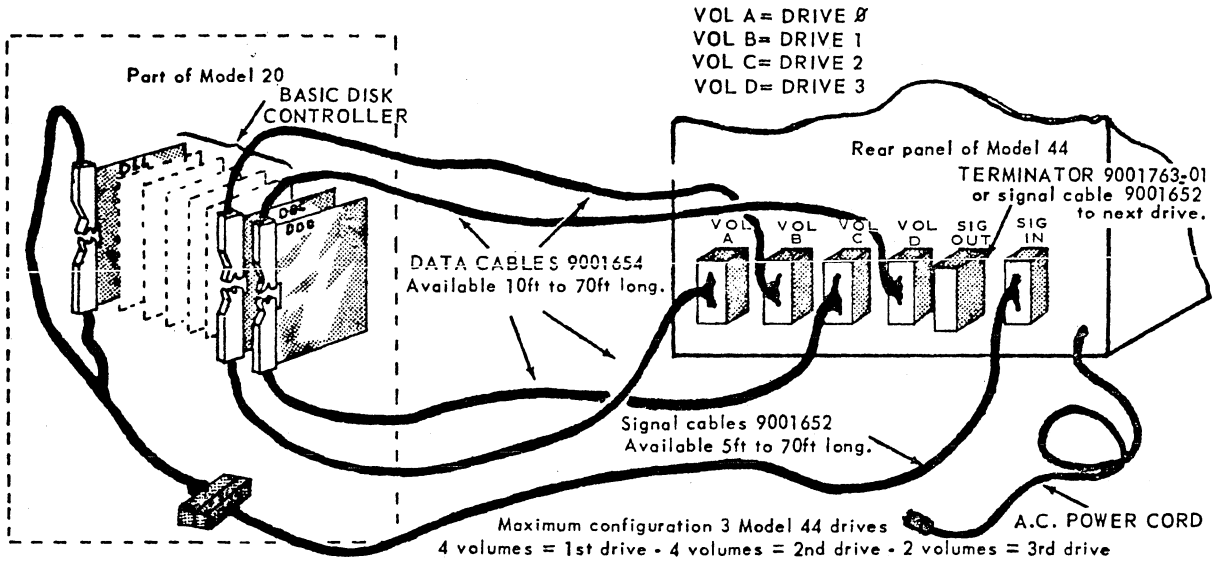
DCF

12-7.7 DLL

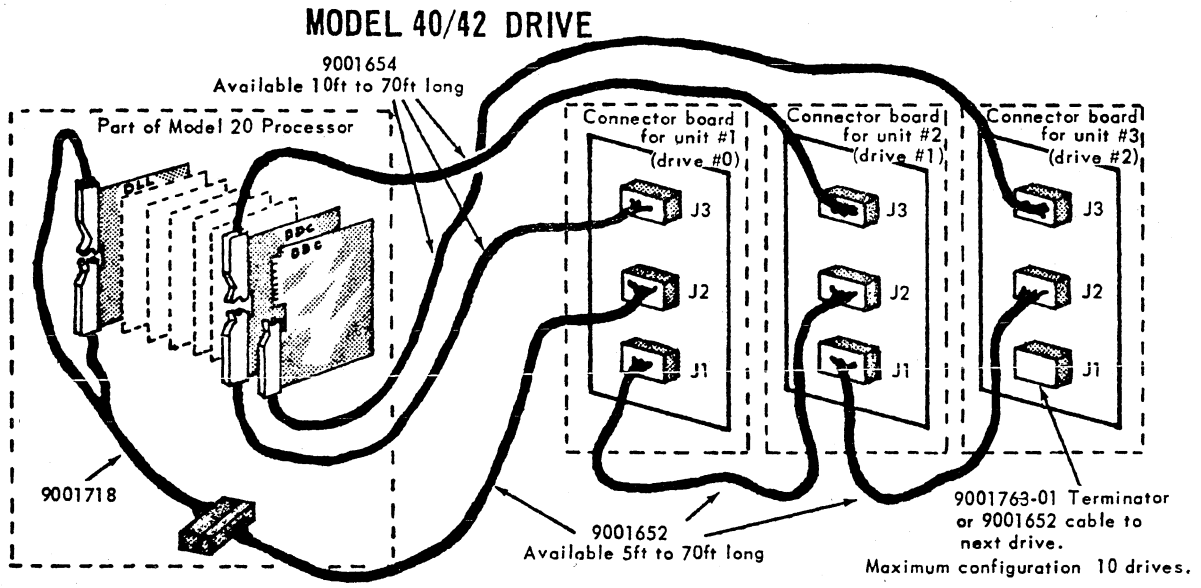
The DLL card provides the line drivers and receivers and the +3v and -3v power supplies for the drivers and the terminator block at the last drive of the series. The line drivers are the power boost that is needed for signals that are sent and received over the interconnecting cables.

12-8.0 INSTALLATION

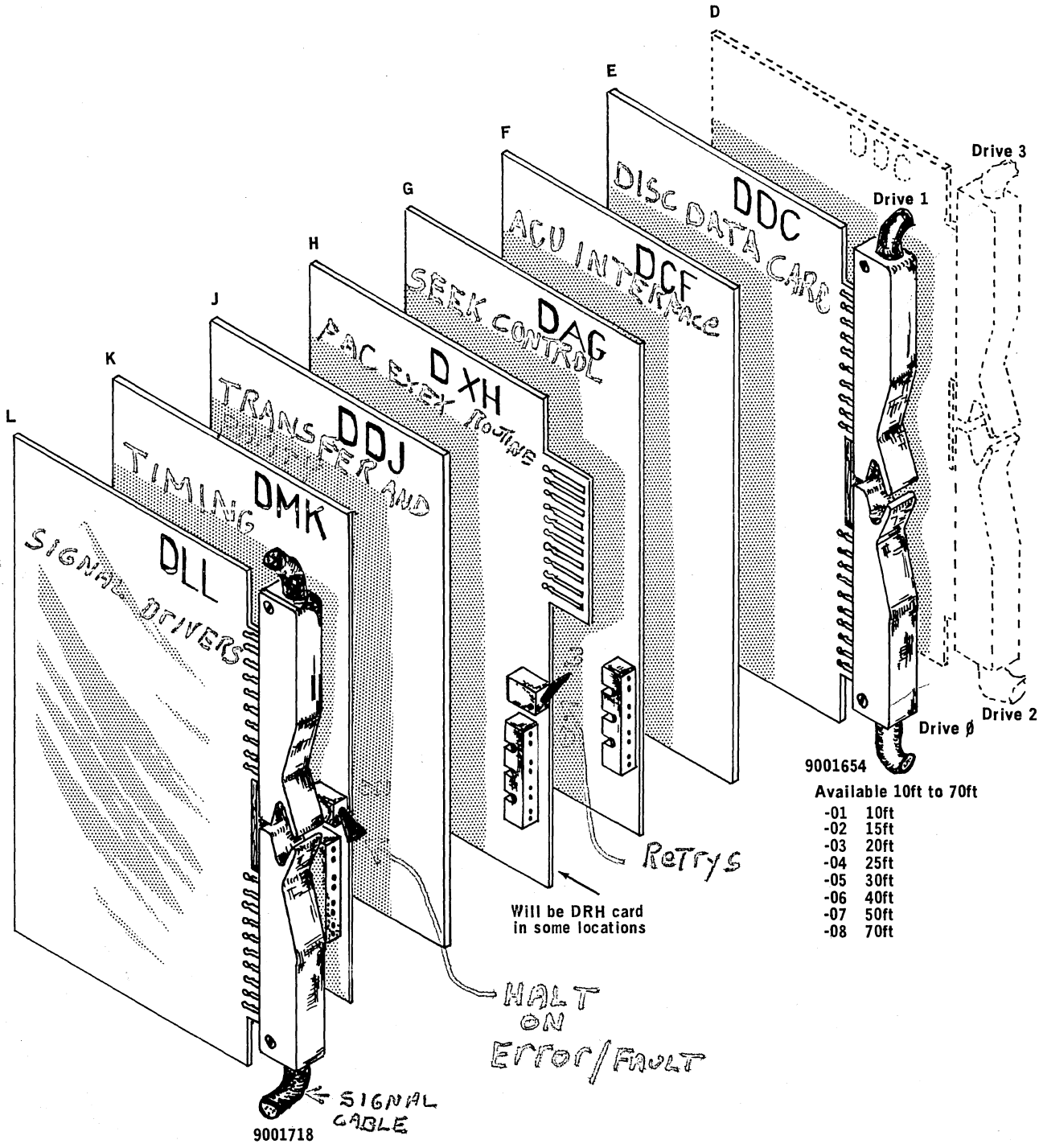
The cable connections for the Disc Controller are shown in the issustration below. Card positions are shown on the opposing page. Be sure that all connections are secure, and that the cables are not strained or pinched.



MODEL 44 DISK DRIVE CONNECTIONS



12-8.0 INSTALLATION (Continued)



DISC CONTROLLER CARD POSITIONS

12-9.0 GLOSSARY

NAME	TYPE	SOURCE	DEFINITION
A-CNTR-CL	Sig	DAG	"A" counter clear. Sets the A counter to Ø from count of 15.
A=	Sig	DAG	Decoded A counts. Counts Ø through 10, and 15 are decoded. The A counter is the controller State Counter, and synchronizes the controller to the ACU.
ACK	Sig	DAG	Acknowledge signal from the controller to the ACU.
AFTER 6	JKff	DDJ	Active during a WRITE operation, after six character counts. Indicates that the preamble is completed. Stays set until CC=107; then the LRCC is written.
AW AX AY	Adder	DAG	AW and AX are used to convert decimal to binary; AY is used to detect difference.
AØ-CCLK	Sig	DCF	A=Ø and controller clock. Loads the DU register with the drive number.
A8ON	Dff	DAG	A=8 and $\overline{\text{ONCYLP}}\cdot\overline{\text{FAULT}}$ Allows a seek sequence if $\overline{\text{ONCYL}}$ or set up for a READ/WRITE if ONCYLP.
BC	Dffs	DRH	Three flip-flops that comprise a bit counter. Bit counts are 1 through 6.
BLOT	Sig	DMK	A unique timing of clock pulses.
BLOT	CNTR	DRH	A modulus 16 counter that is triggered by the missing-clock oneshot. When the counter overflows, a bad sector has been read. FLAG is set to indicate the bad sector.
BLOT-RTRY	Dff	DXH	Set when a sector contains missing clocks during the read-before-write portion of a WRITE operation.
BX	Dffs	DDJ	Buffer X register - outputs 1 through 7. Serial-in or serial-out buffer for data to and from the disc.
BX=63	Sig	DDJ	Indicates that the preamble has been received, making the contents of BX all 1s.
BXYCMP	Sig	DDJ	Buffer X and Y compare. Used to determine if the track ID from the disc compares with the requested track number.
BY	Dffs	DDJ	Buffer Y register - outputs 1 through 6. A one character buffer for READ/WRITE.
CAB	Sig	DLL	Cylinder Address Bus. Derived from the CA-BUS signals that are sent from the disc unit to indicate where the heads are. Outputs 1 through 7.
CA-BUS	Sig	DISC	Cylinder address inputs to the DLL card telling the controller where the heads are (binary 1 to 128).
CREG	SHREG	DAG	Cylinder Register - lines numbered 1 through 7.

12-9.0 GLOSSARY (Continued)

CCCARY	Sig	DCF	Character counter carry - overflow of the character counter. Indicates that the 70ms timeout (for read-amplifier recovery) following read selection has been completed. Also allows seek sequence out.
CC=	Sig	DCF	Character counts
CCLK2	Dff	DCF	Controller clock 2 (synchronized). Part of M-CCLK generation.
CCLKX	Dff	DCF	Part of master controller clock M-CCLK generation.
CC2MOD16	Sig	DCF	Modulus 16 count from the character counter. Indicates that the chacter count is 242.
CC6MOD16	Sig	DCF	Mod 16 count for a character count of 246.
CC8MOD16	Sig	DCF	Character count of 248.
CLKSW	JKff	DMK	Part of the master clock synchronization circuits.
CLOCK-OUT	Sig	DLL	Clock out to the disc. Derived from FSLCTED. When the disc drive is selected and CLOCK-OUT is active to the disc unit, the drive cannot be disabled manually by the ENA/DISABLE switch.
CNTRL	Dff	DAG	Activates TAG 1 when set. Brought up by ONCYLP on the DRH/DXH card.
CNTRLLR	Dff	DCF	Controller flip-flop. Gates FAC-STROBEs into CCLK, CCLKX, and CCLK2. Synchronizes the controller with the ACU timing (see the text section on the DCF card).
CYCLE-REQ	Sig	DDJ	Cycle Request. A=10•CYC-RQST. Informs the ACU that the controller is ready for a data transfer.
CY-RQST	JKff	DDJ	Generates CLCLE-REQ.
CY-	JKffs	DDJ	Six flip-flops that make up the CY register. The CY register is used for LRCC accumulation during READ/ WRITE operations.
CYLINDER	Term	-	The same track number or position on all disc surfaces. All heads are simultaneously positioned on cylinder; the individual track is selected as one of the surfaces (heads) within the cylinder.
CY=Ø	Sig	DDJ	Indicatas that the CY register equals zero. This is the "good" signal for the LRCC on a READ operation.
D	Dffs	DAG	Eight flip-flops that act as a Difference register. This register is used to store the disc current address, then is complimented and added to the contents of the C register to determine direction and length of seek.
DDIFFØ	Sig	DAG	Indicates that the difference register equals zero, and that a seek is not required.

12-9.0 GLOSSARY (Continued)

DLTA-RST	Dff	DRH	Delta reset flip-flop. Generally clears the controller logic.
DLTASRCH	Dff	DRH	In combination with SECSRCH, FSCMP is inhibited until after the 70us timeout that is required on HDSEL. DLTASRCH is a link between CCCARY and SECSRCH, and is used to buffer CCCARY until SECSRCH can be turned on (i.e. anytime SECPLSE is off).
DMMYREQ	Dff	DDJ	Dummy Request. When the controller has progressed beyond A=9, and an error occurs, the 100 cycle requests must be completed. The dummy request is held until the ACU sends the TERM-TRANS pulse that is needed to clear the partition register in the DDC card.
DRV-A	Sig	DISC	A signal to the DDC card indicating that the A portion of the card is connected to a disc unit.
DRV-B	Sig	DISC	A signal to the DDC card that indicates a disc drive is connected to the B portion of the card.
DRV-A-B	Sig	DDC	Indicates that one of the disc units on that particular card is selected.
DRV-SLCT	Sig	DDC	Derived from DU-SLCT flip-flops. It is given to the disc unit (A through K) as a select signal from the DD register.
DTAERR	JKff	DRH DXH	Set when the LRCC is not correct. Causes a hardware repeat-if-error (for three tries). The DXH card has a switch that will disable this retry feature.
DUA	Sig	DCF	Disc unit A. There are a total of ten of these outputs from the decoder (A through K). The letter designations can be translated to drive numbers zero through 9.
DU()SLCT	Dff	DDC	Select signal for disc units. The () can be Ø - 9.
D1 - D8	Dffs	DAG	Difference register. Indicates the difference between the head position (that is being reported by the disc unit) and the cylinder address that is required.
ECHO	Sig	DAG	Indicates that the selected disc unit has power, and the cables are connected.
ERROR	Sig	DRH	READ+WRITE+RPTERR•STATUS•$\overline{\text{FLAG}}$
FAC	Term	-	File Access Channel. The portion of the processor that interfaces with magnetic tape, disc, and OLCA communication.
FACSLCT	Sig	DCF	FAC-SELECT inverted (from the ACU).
FAC-SELECT	Sig	ACU	Informs all FAC devices that the ACU operation is within the FAC portion of the processor.
FAC-DATA	Sig	DDJ	These six (1-6) lines are inverted from the Y buffer signals, and originate from the information that the ACU put on the M and N bus.

12-9.0 GLOSSARY (Continued)

FAC-STROBE	Sig	ACU	This is the "go do it" signal from the ACU. FAC-STROBE is given to FAC devices whenever information is placed onto, or taken from the M and N lines. It is inverted by the controller on the DCF card for internal use by the controller.
FAULT	JKff	DRH	Reports an unacceptable condition at the addressed disc drive.
FAULTINV	Sig	DRH	STATUS•$\overline{\text{FAULT}}$
FAYC	Dff	DAG	Direction of seek. Set when the direction is forward; reset when the seek direction is reverse.
FB-	Sig	DAG	File bus lines are common to all units, but the lines only affect the selected unit. TAG lines (1-4) control the type of data that is on the file bus lines. File bus lines are numbered FBØ through FB7, and carry the following information. If the active TAG line is: TAG 1 = Control TAG 2 = Set Cylinder TAG 3 = Head & Direction TAG 4 = Set Difference
FILE-BUS	Sig	DLL	The file bus signals (above) that are amplified and placed onto the lines to the disc units.
FILERDY	Sig	DLL	Reports that the disc unit has completed the start-up sequence and is not seeking.
FREADY	Dff	DAG	Qualified by FILERDY (above). The flip-flop remembers the file ready condition.
FLAGERR	Sig	DRH	FLAG•STATUS
FLAG	JKff	DRH	Set because of a bad sector on the disc pack.
FSCMP	Dff	DRH	Final Sector Compare. Set when there is a sector compare during delta search.
FSLCTD	Dff	DAG	File Selected - qualified by timing and ONLINE. Means that the selected unit is in a ready status.
F1375	Sig	DMK	1.375 MHz clock pulses. Data clock frequency.
F6875	Sig	DMK	.6875 MHz clock pulses.
HIGHSEL	Sig	DMK	Output of a D flip-flop. This signal selects one of the three possible oscillator frequencies, to compensate for differences in the rotational speed of the disc unit spindle.
H-	Sig	DCF	Head register outputs 1-4.
INTRRGTE	Sig	DAG	A combination of Partition Ready (PRDY) and File Ready (FREADY) indicating that selection is possible.

12-9.0 GLOSSARY (Continued)

INCONT	Sig	DLL	Incomming Control, a dc ground signal to the first drive on the line. The data cable from the disc unit must be connected to the split connector on the DLL card to enable the disc unit to power up.
INDXMRKA INDXMRKB	Sig	DISC	Each DDC card receives index marker pulses from two seperate disc drives (providing both units are connected). The A signal is from the first unit (lower connector), and the B signal is from the second unit (upper connector) of the DDC card. Additional units (on other DDC cards) will have designations C to K, but the internal signals from each DDC card are still considered A and B.
INSEQ	Sig	DLL	Provides +15v to the power up sequencing relay in the first disc drive unit. Additional disc units are sequenced from the first drive.
LOWSEL	Dff	DMK	One of three frequencies that can be selected to compensate for differences in the rotational speed of the disc drive spindle.
LRCC	Term	-	The Longitudinal Redundancy Check Character (LRCC) is an accumulation of bit information throughout the entire data message (the 100 characters within one sector). Each bit position within the message is made to contain an even number of 1 bits. This is done by adding a 1 bit in the cooresponding bit position (or not adding, as the case may be). The resulting collection of bits is recorded as a character, the LRCC.
M1-C to M4-C	Sig	DCF	Outputs of the M register that are double inverted for further use within the disc controller logic.
MCL	Term	-	Master Clock.
MCL1375	Sig	DMK	1.375 MHz clock pulses.
MCL275	Sig	DMK	2.75 MHz clock pulses.
M-CCLK	Sig	DCF	Master Clock - the product of two D flip-flops, CCLKX and CCLKZ, gated with FAC-STROBE.
MEQLØ	Sig	DCF	M register equals zero.
MIDSEL	Sig	DMK	One of three frequencies that can be selected to compensate for differences in the rotational speed of the disc unit spindle.
MISSCLK	OS	DMK	A oneshot (re-triggerable monostable multivibrator) that detects when a clock pulse has been missed. When reading a blot, the missed clock is a part of detecting the blot.
MREG-	Sig	ACU	The inputs 1-4 from the M bus to the M register on the DCF card.
N-C	Sig	DCF	Outputs 1 and 2 of the N register (double inverted).

12-9.0 GLOSSARY (Continued)

NREG-	Sig	ACU	Inputs 1 and 2 to the disc controller.
NSEQ	Sig	DLL	In sequence to disc. Consists of +15v with a diode and a 1K resistor to allow disc power up.
ONCYLP	Dff	DRH	On Cylinder Proceed. Set when the seek is completed and all else is well.
ONLINE	Sig	DLL	Comes from SEL-ONLINE, a disc signal that is sent after the brush cycle is completed (from start up) if the drive is enabled.
PA 1 to PA 5	Dffs	DDC	Partition register. All flip-flops within the partition register are set when the register (or more specifically the disc unit that is represented by the particular register) is not reserved. The flip-flops are set to represent the requesting partition number when the drive is reserved.
PARTITION TIMEOUT	OS	DDC	If for some reason a partition reserves the use of a disc drive, by initiating a seek, and does not return within 1.8 seconds, this timeout will expire. When the one shot has timed out, the next requesting partition need not match the number that is set in the partition register to receive acknowledgement.
PB 1 to PB 5	Dffs	DDC	Partition register for the B portion of the DDC card. See PA 1 to PA5, above.
PRDY	Sig	DDJ	An "or" of all ten P()-RDY signals. Means that the partition register is either all 1s, or that the number in the partition register compares with the entering partition.
PA-RDY PB-RDY	Sig	DDC	A composite signal indicating that all of the partition register flip-flops are set, or that the partition number under comparason matches the number in the partition register. PA-RDY is from the A portion of the DDC card, and PB-RDY is from the B portion.
RDCLK	Dff	DMK	Read Clock - timing signal for READ operations. Derived from recorded clocks on the disc.
RDCHK	JKff	DRH	Read Check. Set ehenever an ERROR or FLAG condition occurs.
RDDTA	Sig	DMK	Read Data signal that has been squared up. This is the signal that represents data comming from the disc unit heads.
RDGTE	JKff	DRH	Read Gate. Set by sector compare; knocked down by the next sector pulse.
RDS	Dff	DRH	Set when reading from the disc (read select); reset when writing to the disc. This is so, even during a WRITE instruction. RDS has only an indirect relationship to the software instruction, and is used to force a read during the check read operation.

2-9.0 GLOSSARY (Continued)

RDSTE 1 RDSTE 2	Dff	DRH	Generates read states Ø through 3 for subroutines within the read cycle.
RDSIG-A RDSIG-B	Sig	DISC	Signal to the A or B portion of the DDC card within the controller. Comes from the read heads on the disc unit.
RDWRITE	Dff	DRH	Read/write flip-flop. This condition can be overpowered by setting the RDS flip-flop. However, RDWRITE remains set throughout a WRITE instruction. The set/reset state of RDWRITE is determined by the instruction, not by the temporary operation within an instruction.
RDWTE	Sig	DRH	Signal from the REWRITE flip-flop.
READ	Sig	DDC	Signal to the selected disc drive, telling it to read.
RESRV-MEM	Sig	DDJ	Qualified by sector compare and controller state A=10, this signal monopolizes the processor until the data transfer is complete.
RPTERR	Sig	DRH	Repeat If Error. Part of a hardware forced re-read scheme that is brought into play when an error is found in data.
RTC	Dffs	DRH	Two flip-flops that count the number of re-tries when an error or repeat is forced. The counter will count to a maximum of three before FLAG is set.
SA-SB-CMP	Sig	DDC	Signal used to cause the alternate compare of A and B drives during the sector compare sequence.
SCMP	Sig	DRH	Active when the sector compare is made.
SECMRK-A	Sig	DISC	The sector pulse from drive A of the two possible drives on the DDC card.
SECMRK-B	Sig	DISC	The sector pulse from drive B of the two possible drives on the DDC card.
SECPLSE	Sig	DRH	The sector pulse that has been synchronized with the master clock timing (MCL1375).
SECT-A-B	Sig	DDC	Reflects the sector pulse of the selected (A or B portion of the DDC card). The selection between the A or B drive is made by the signals DUA or DUB.
SECTOR	Sig	DRH	The sector output (reading) from one disc unit.
SEEK-INC	Sig	DLL	A controller signal that is derived from the disc unit signal SEL-SK-INC. It means that the seek was not completed in the alloted time.
SEL-FILERDY	Sig	DISC	The selected disc unit is powered up, and has completed the brush cycle. It does not mean that the disc unit is not in use, only that the unit is ON, and not seeking.
SEL-ONLINE	Sig	DISC	Verification that the selected disc unit is connected, powered up, and the ENA/DISABLE switch is in the ENABLE position.

12-9.0 GLOSSARY (Continued)

SEL-SK-INC	Sig	DISC	Indicates that the seek was not completed in the alloted time.
SEL-UNSAFE	Sig	DISC	Signal from the selected disc unit indicating that one or more of the following things are wrong. 1. More than one head is selected. 2. Head selected without ready. 3. Write current and not write gate. 4. Erase current and not erase gate. 5. Write gate and not write current. 6. Read gate and not ready, and either write gate or erase gate. 7. High or low dc voltages. 8. Loss of line voltage. The File Unsafe condition will de-select the heads, and turn off the read and write gates.
S()CMP	Sig	DDC	Taken from the disc signal SA-SB-CMP. It means that the unit that is indicated, (), has a sector compare.
SLCTED	Sig	DAC	Selected - double inverted signal from ONLINE. Means that the selected drive has power and has completed the brush cycle and first seek, and that the ENA/DISABLE switch is in the ENABLE position.
SR-	Sig	DCF	Sector register outputs 1 through 7. Developed from MREG and timing signals. SR- is the sector address that is distributed to the DDC cards for compare.
SRVLIMIT	Sig	DMK	Servo Limit. Indicates that the speed of rotation is too fast or too slow. If SRVLIMIT becomes active during an operation, the operation is aborted in a FAULT status. SRVLIMIT is created only during WRITE operations.
SRVNUL	Sig	DMK	Servo Null. Aborts a WRITE operation in FAULT status if the speed of rotation goes above or below set limits.
S-SRT	Sig	DRH	Status or System Reset. A general reset condition that is used to clear the previous operation in the controller. It can come from SYS-RST, which is an ACU signal, or after status is given by the controller, meaning that the operation is complete.
STATE-	Sig	DRH	Decoded states Ø through 3 from two D flip-flops, RDSTE 1 and RDSTE 2. Controls sub-routines within the read cycle.
STATUS	Dff	DRH	Controls the STATUS-RDY line to the ACU. When STATUS is set, the FAC-DATA lines contain the controller status character.
STATUS-RDY	Sig	DRH	See STATUS.

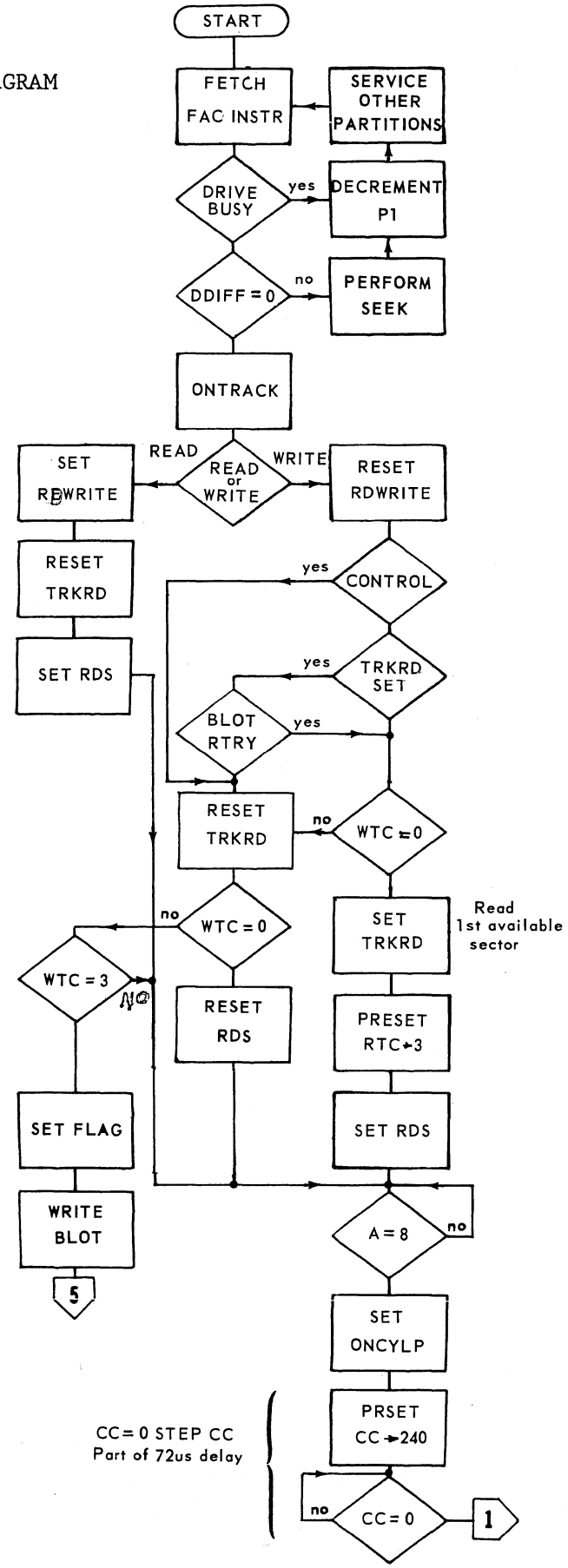
12-9.0 GLOSSARY (Continued)

STATUSRT	Sig	DRH	Status Reset, a disconnect and reset signal. Linked to DLTARST which is used when it is impossible to complete a read/write operation in one controller cycle (such as when a seek is initiated).
SYS-RST	Sig	ACU	System Reset signal. Active after a power failure or a manual reset of the system.
SYSRST	Sig	DRH	From SYS-RST.
TAG-	Sig	DAG	Tag lines 1 through 4 determine what signals are placed on the file bus lines to the disc units. The TAG designations are listed below. TAG 1 = Control. TAG 2 = Set cylinder. TAG 3 = Head and direction. TAG 4 = Set difference.
TAG-DIFF TAG-CYL TAG-HD TAG-CNTRL	Sig	DLL	Tag signals are level converted for transmission on the data lines. Also thee signals are ANDed with the SYS-RES signal
TERM-TRANS	Sig	ACU	This pulse is sent by the ACU when 100 cycle requests have been made and completed. It is needed by the controller to clear the partition number in the partition register of the DDC card.
TERMTR	Sig	DCF	Comes directly from the signal TERM-TRANS.
TNNL	JKff	DCF	Controls the tunnel erase portion of the read/write head. TNNL set and reset times are computed from the cylinder address and the sector pulse.
TRKRD	Dff	DXH	Track Read. Set by a WRITE instruction, it forces a read and compare of the track ID in the first available sector after the heads are on cylinder.
TRACK ID	Term	-	Track number identification is a six-bit character that is written directly after the preamble of each data sector (on the disc pack). The track ID is modulus 64, and refers to the actuator position relative to track ØØØ. Track ID is different from cylinder address only in that track refers to a concentric location on one disc surface; cylinder address is the same track location on all surfaces.
TRCHK	JKff	DRH	When the track ID is read from the disc surface, it is compared to the track (cylinder) address in the controller register. If the comparason is bad, a re-try is made. After the third re-try, TRCHK isset, indicating that the heads are over the wrong track. A re-calibrate is forced, and ERROR is set.
TSTSW	Dff	DMK	Controlled by a manual switch. Used to locate problems by holding the situation when bad status is reported.

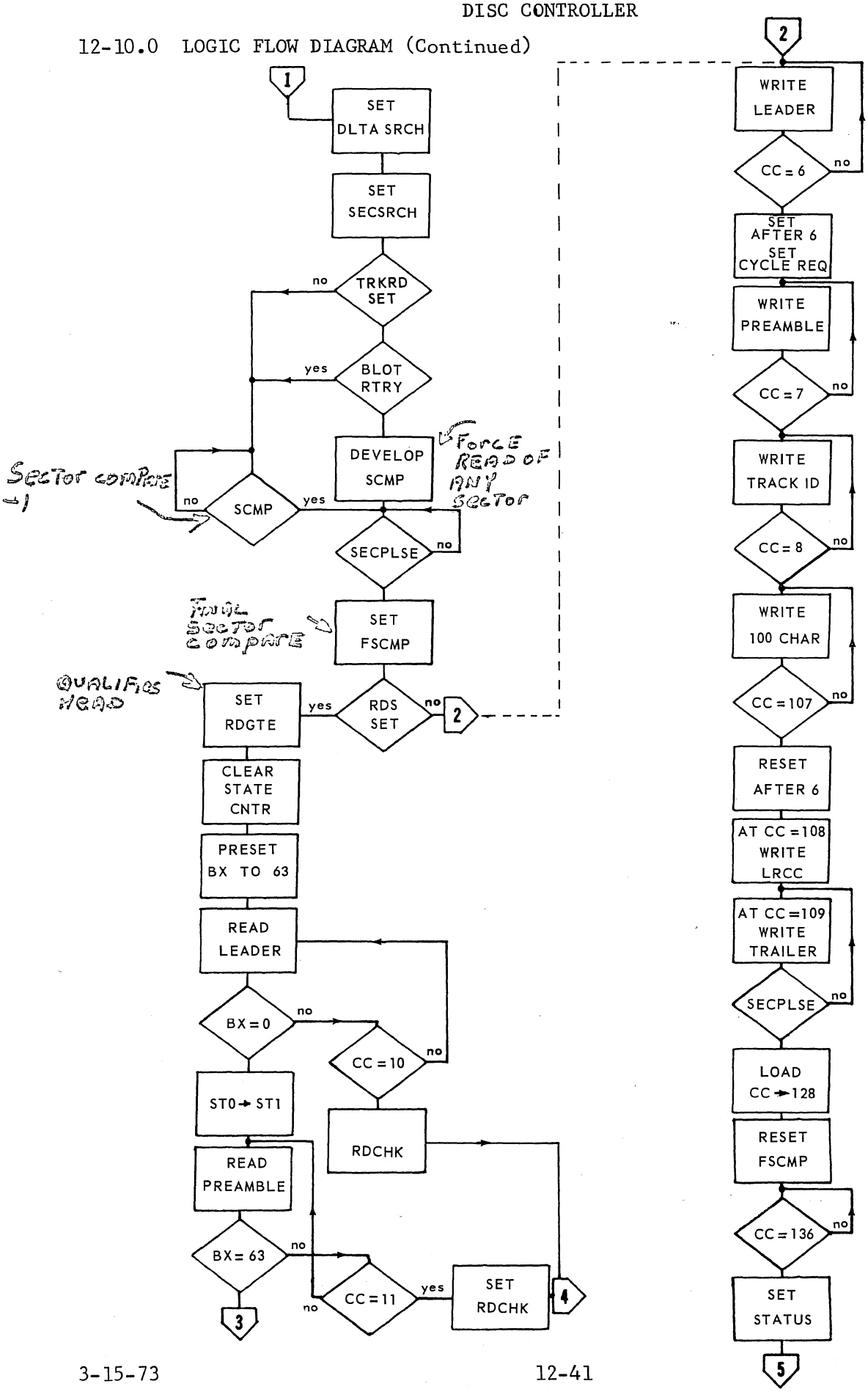
12-9.0 GLOSSARY (Continued)

TWPRGRD	Sig	-	Used to designate the ground wire of a twisted pair.
UNDER64	Sig	DCF	$\overline{CC7}+\overline{CC8}\cdot FSCMP$
UNSAFE.	Sig	DLL	Level converted signal from the disc signal. See SEL-UNSAFE.
WRITE	Sig	DMK	Control signal to the DDC card, where it will be directed to the selected disc drive.
WRITE-A	Sig	DDC	Signal from the DDC card to the disc unit that is controlled by the A portion of the card.
WRITE-B	Sig	DDC	Signal from the DDC card to the disc unit that is controlled by the B portion of the card.
WRS	Sig	DRH	A name given to the reset side of the RDS flip-flop. This signal is the same as $\overline{RDS}$.
WTC3	Sig	DRH	Write Tally Counter 3. The write tally counter consists of two D flip-flops. In conjunction with RDWRITE and RDS flip-flops. writing is attempted three times (and checked by read-after-write) before a blot is put onto a sector (if the recording was bad). WTC 3 indicates that the third attempt has been made.
X140	Sig	DRH	Pulse when the preamble is detected.

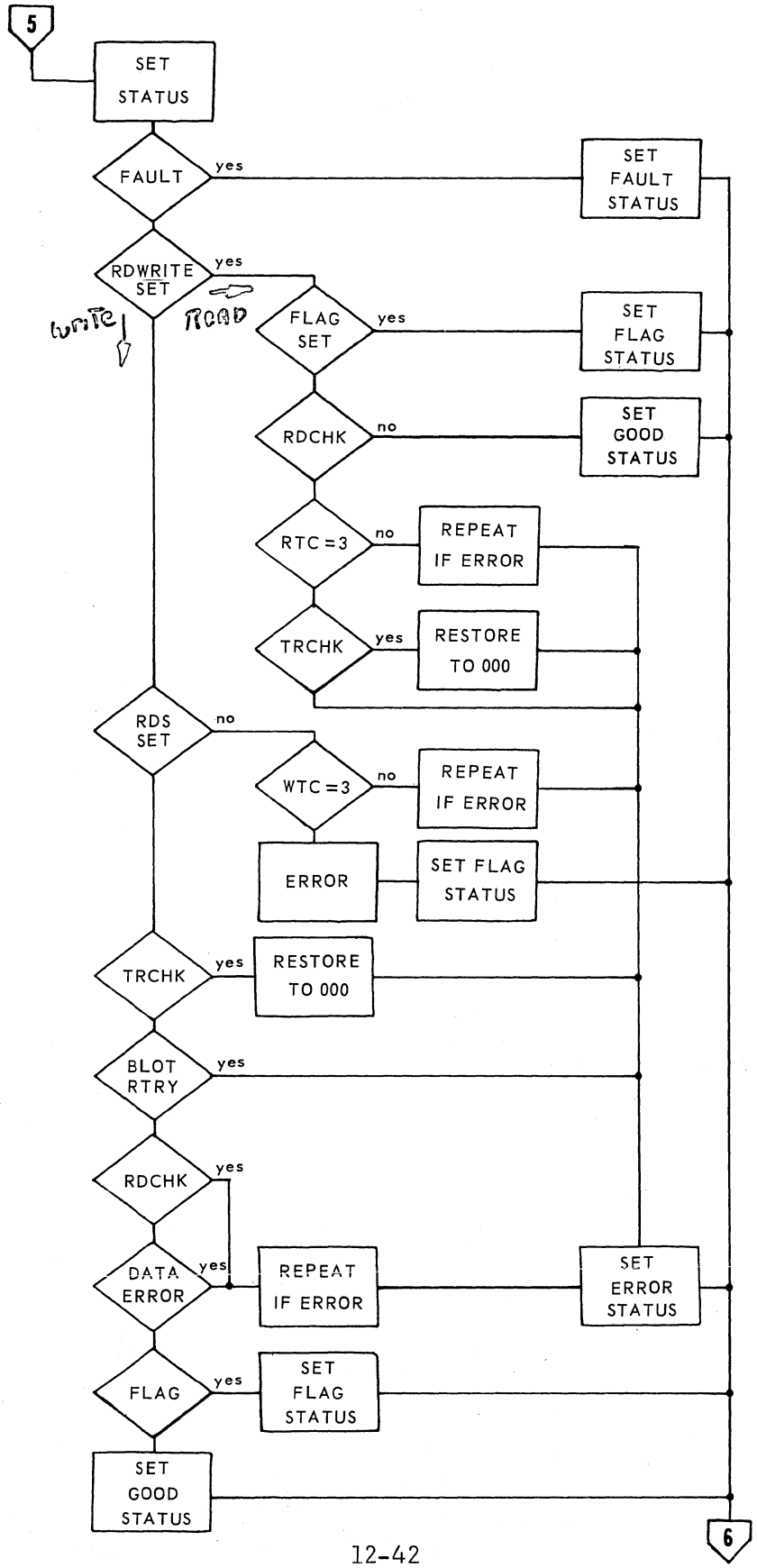
12-10.0 LOGIC FLOW DIAGRAM



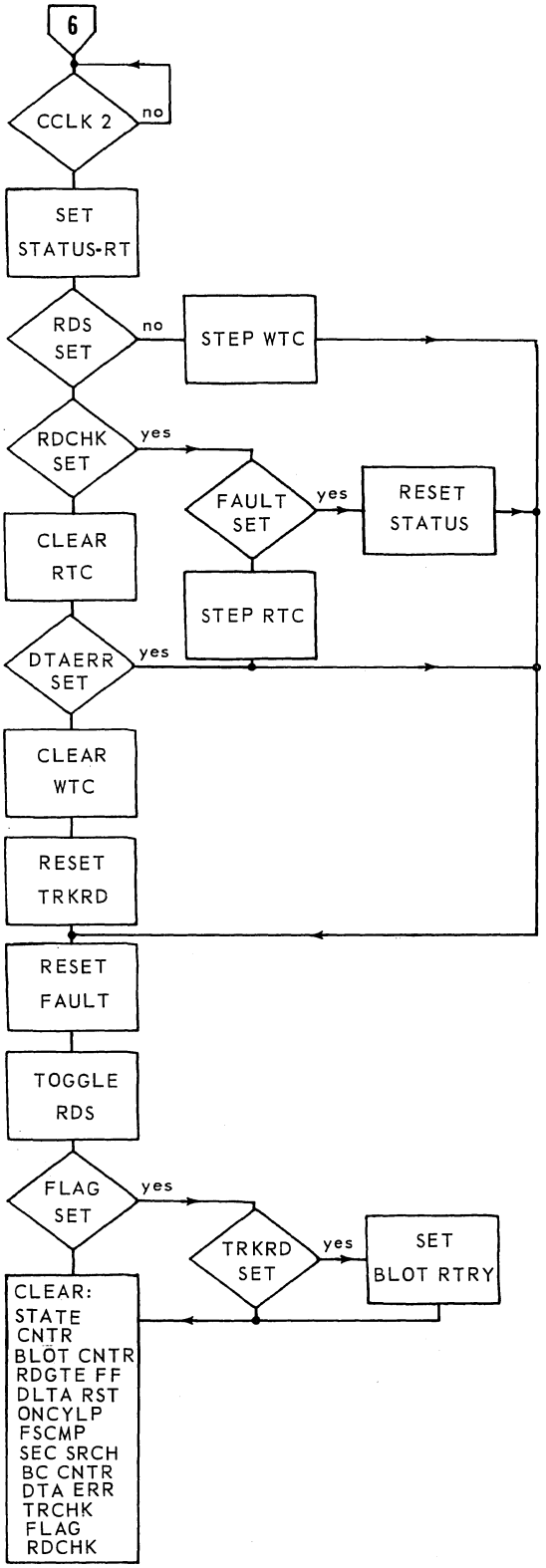
12-10.0 LOGIC FLOW DIAGRAM (Continued)



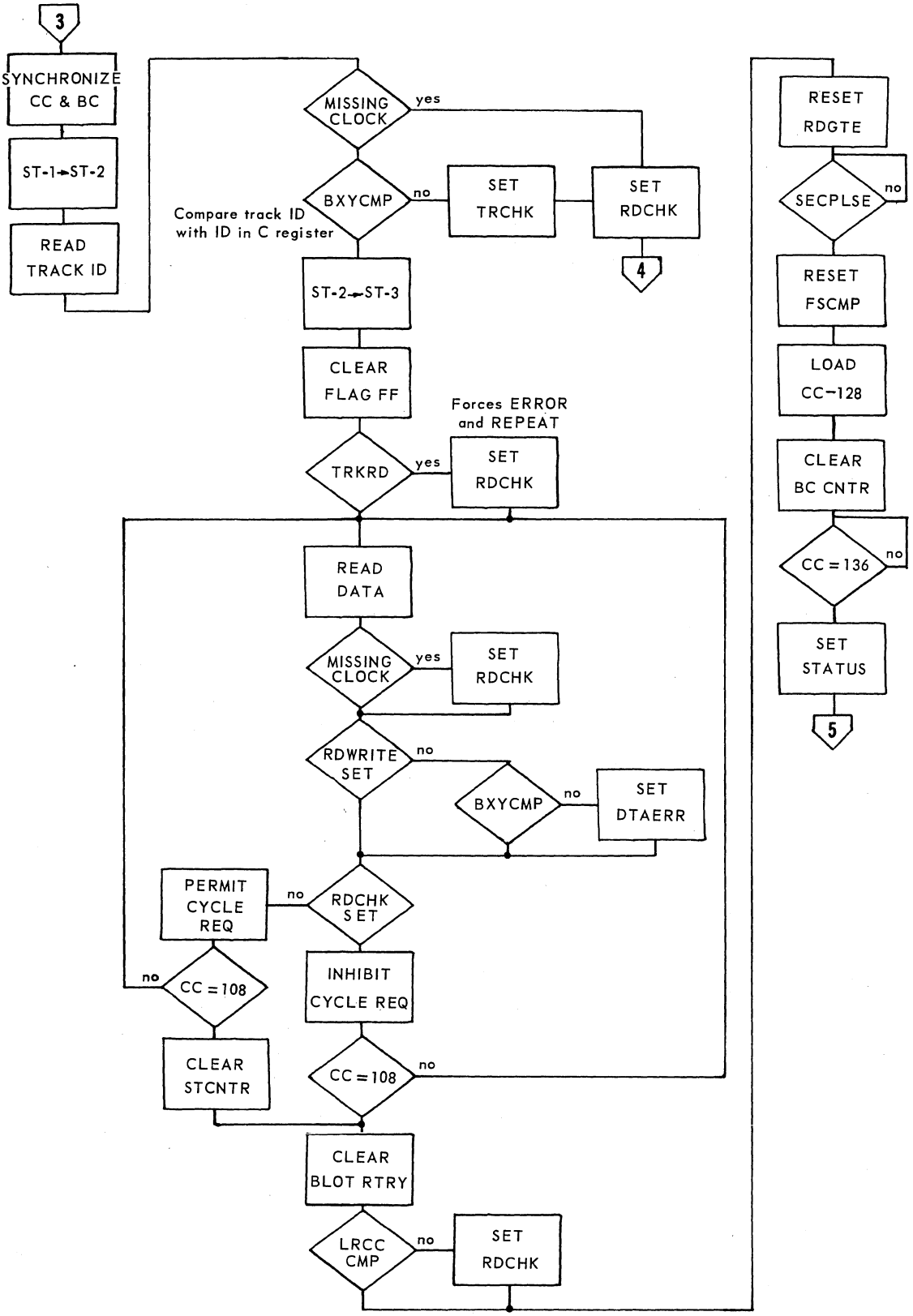
12-10.0 LOGIC FLOW DIAGRAM (Continued)



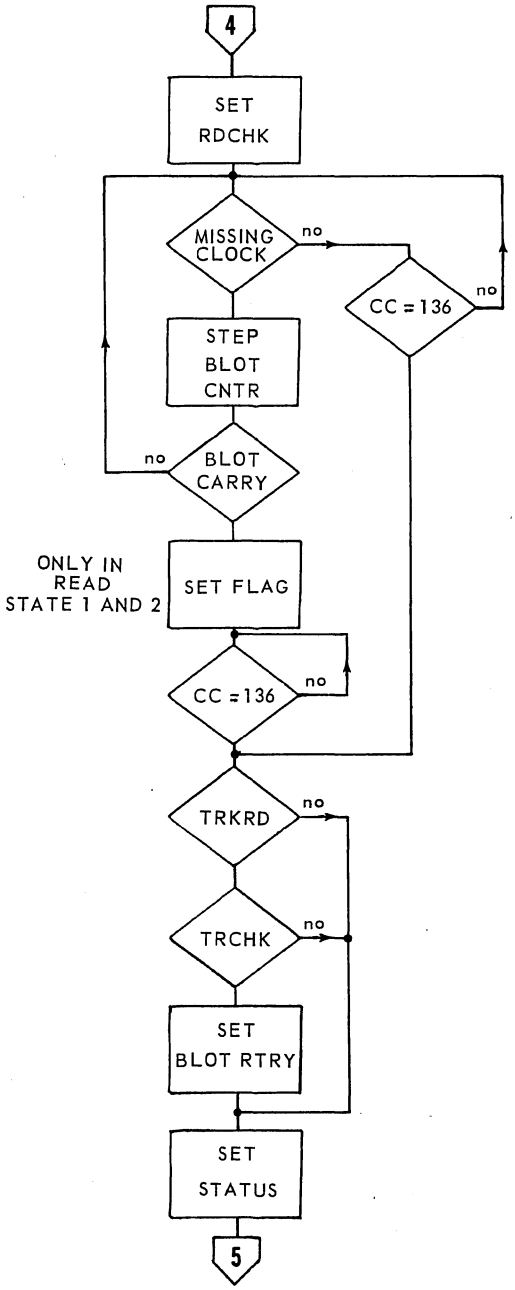
12-10.0 LOGIC FLOW DIAGRAM (Continued)



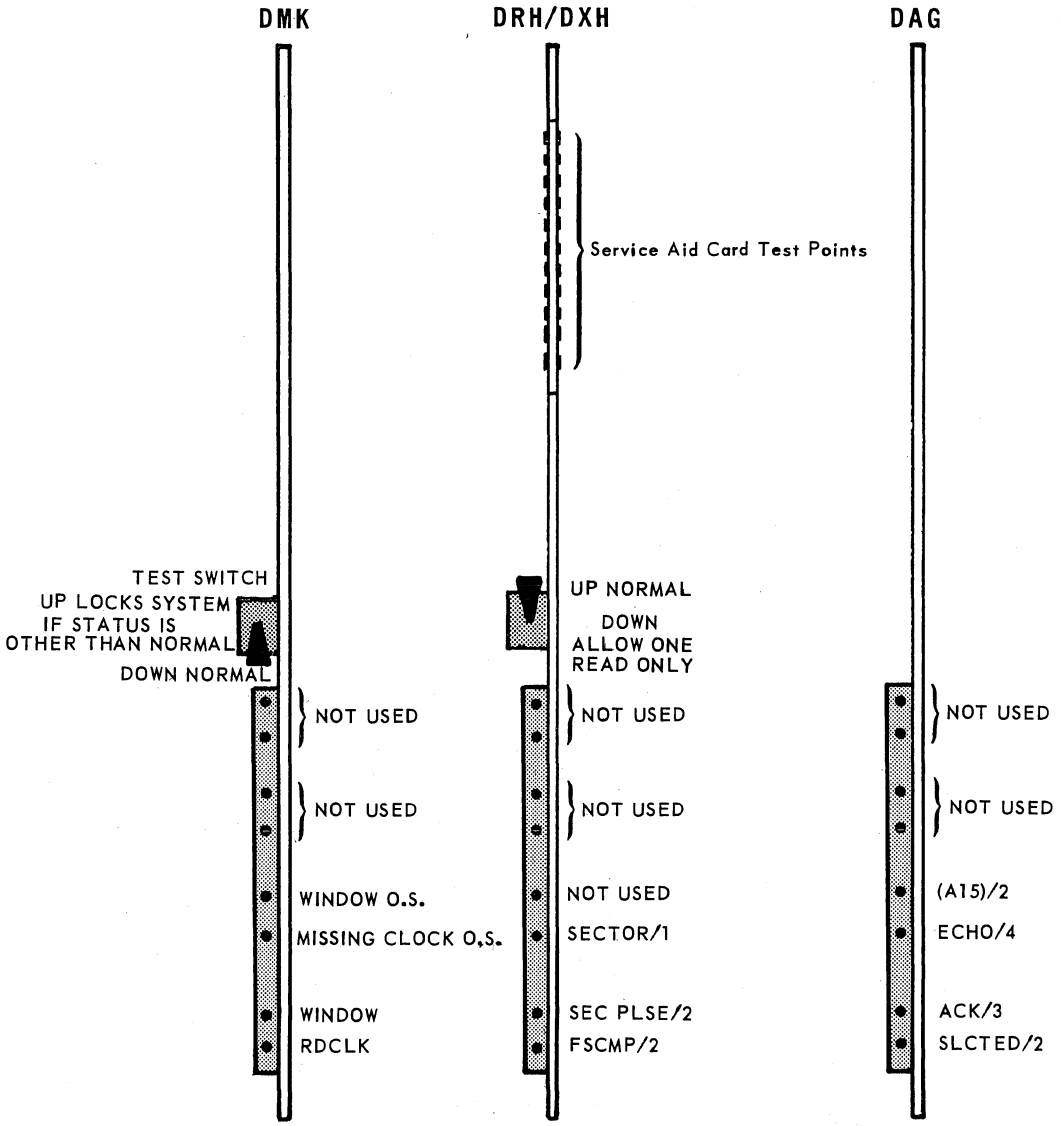
12-10.0 LOGIC FLOW DIAGRAM (Continued)



12-10.0 LOGIC FLOW DIAGRAM (Continued)



12-11.0 TEST POINTS



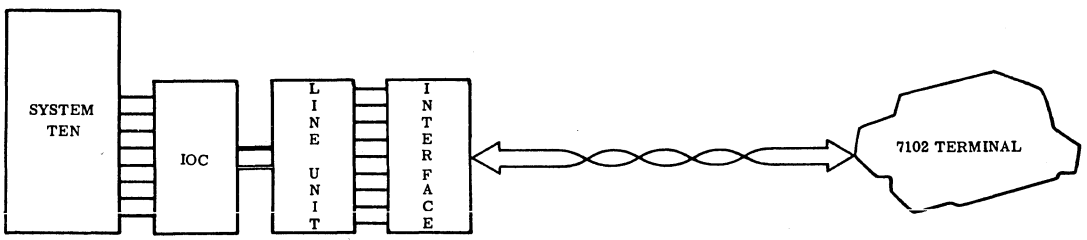
DISC CONTROLLER TEST POINTS

SECTION 14

7102 INTERFACE

SECTION CONTENTS

LIST OF ILLUSTRATIONS



SYSTEM CONCEPT

FIGURE 14-1

SECTION 14, 7102 INTERFACE

A. INTRODUCTION

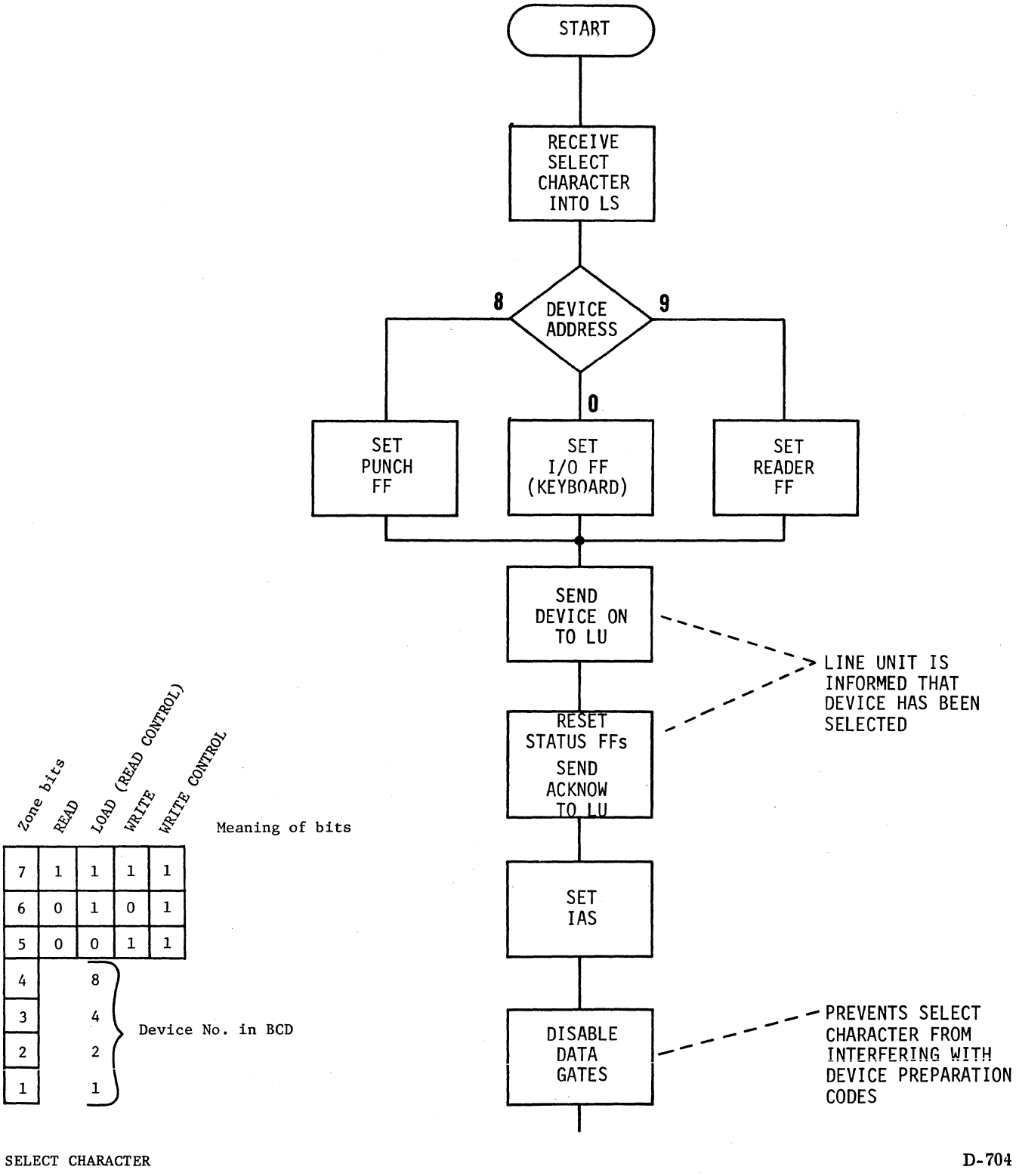
The 7102 Interface functionally converts the Teletype (TTY) compatable operation of the 7102 Terminal to asynchronous communication with the Central Processor, through a standard MT I/O Channel.

Line Unit cards LU1, and LU2 are a functional part of the interface operation. Three additonal cards (FEN, FII, and FTI) are required to generate special codes and conditions for compatability with standard I/O operations. The 7102 terminal is essentially reset before each I/O operation as a safeguard against unwanted settings that may have been performed manually. The interface assumes that the operator has toggled the manual switches. For example, before each new WRITE instruction, the printer-on signal is sent to the 7102 Terminal, even if a WRITE instruction has just ended. A basic system concept of the 7102 Interface in reference to the Processor and Terminal is shown in Figure 14-1.

The overall communication between the 7102 interface and the processor is the nine bit transmission (seven USASCII, and two parity bits) exchange between the Line Unit and the IOC. Odd/even bit parity checks and character codes are identical to all other Line Unit interfaced peripherals. The Keyboard, Printer, Punch, or Reader are selected by the processor as desired. Figure 14-2 shows the select character for selecting the different devices, and the logic actions before data is transferred.

1. INTERFACE 7102 TERMINAL COMMUNICATION

Communication between the 7102 Interface, and the 7102 Terminal, is the TTY (Teletype) compatable system of the 7102 Terminal itself. USASCII character codes are used, but the transmission format and mark/space voltage levels are different from that of the Line Unit/IOC communication. A mark (a 1 bit) in this case is -12 volts and a space (a zero bit) is approximately +5 volts.

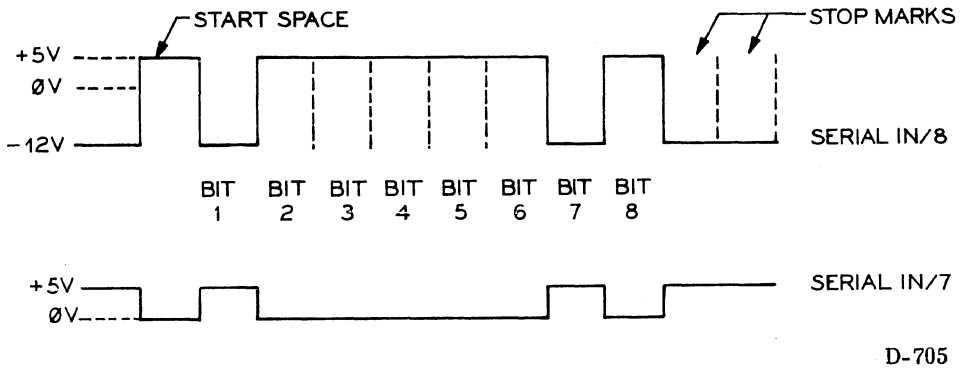


DEVICE SELECTION

FIGURE 14-2

1. INTERFACE 7102 TERMINAL COMMUNICATION (Cont.)

Each character begins with a start space, and is ended (after the parity bit) with two stop marks. Voltage levels are converted to integrated circuit tolerance levels by a one-transistor inverter/leveler circuit in the SERIAL-IN and SERIAL-OUT lines. A typical character transmission from the 7102 Terminal to the Interface is shown in Figure 14-3. The converted signal on the SERIAL-IN line is also shown for comparison.



TYPICAL CHARACTER FORMAT

FIGURE 14-3

2. 7102 INTERFACE/LINE UNIT COMMUNICATION

Interface signals and data are shifted between the Line Unit and the Interface through the parallel interface shown in Figure 14-4. The Line Unit continually monitors IOC transmission, awaiting selection. When one of the 7102 devices are selected, communication is activated. The general usage of some of the Line Unit Interface signals is given in the following paragraph.

3. INTERFACE SIGNALS

Seven INPUT-DATA lines carry data into LS. Eight OUTPUT-DATA lines carry data and the parity bit to the 7102 Interface.

a. LINE UNIT SIGNALS

(a)	COMP-ADD/4:	COMPARE-ADDRESS is sent to the 7102 Interface along with the I/O Select Character to determine whether or not this is the device being selected.
(b)	CONTROL/4:	Output of the CONTROL FF, indicating that the operation being performed is a WRITE Control or a Load (READ Control).
(c)	C/SERV-REQ/3:	Clears the SVRQ FF in the 7102 Interface.
(d)	OUTPUT-ENA/4:	Strobes data in LS into interface shift register.
(e)	READ/2:	Output of READ FF, indicates that a READ operation is being performed.
(f)	REQUEST/4:	Output of REQUEST FF, asks for input data from the 7102 Interface.
(g)	STATUS/4:	Output of STATUS FF, requests status character from 7102 Interface.
(h)	STATUS-RESET/3:	Clears status FFs in the 7102 Interface after selection and prior to data transfer.
(i)	WRITE/2:	Output of WRITE FF, indicates that a WRITE operation is being performed.

b. PERIPHERAL SIGNALS

(a)	ACKNOW/3:	Response to OUTPUT-ENA informs Line Unit that output character has been accepted by the 7102 Interface.
(b)	DEVICE-ON/3:	Response to COMP-ADD, informs Line Unit that address of this peripheral device compares to address contained in I/O Select Character
(c)	FAULT/3:	Output of FAULT FF in 7102 Interface.
(d)	INPUT-ENA/3:	Response to REQUEST signal, gates data character into LS.
(e)	LOAD/3:	Output of LOAD FF in 7102 Interface.
(f)	SVRQ/3:	Output of SVRQ FF in 7102 Interface.
(g)	SYS-RST/5:	Initializes Line Unit upon turn-on.

B. OPERATION

For the most part the 7102 Interface is a passive device, waiting for commands or data from the Processor or the 7102 Terminal. The 7102 Interface initiates no action except those required by Processor initiated IOs (via the IOC and Line Unit) or by initiations from the 7102 Terminal. Some characters are passed through the interface to the receiver, after voltage and format changes. Other characters or commands require a certain device on or off, and these commands are generated within the interface (on the FEN card) before allowing data transfers. The major activities of the 7102 Interface are described below, and refer to the flow chart in Figure 14-9, and the system block diagram, Figure 14-10, at the end of this section.

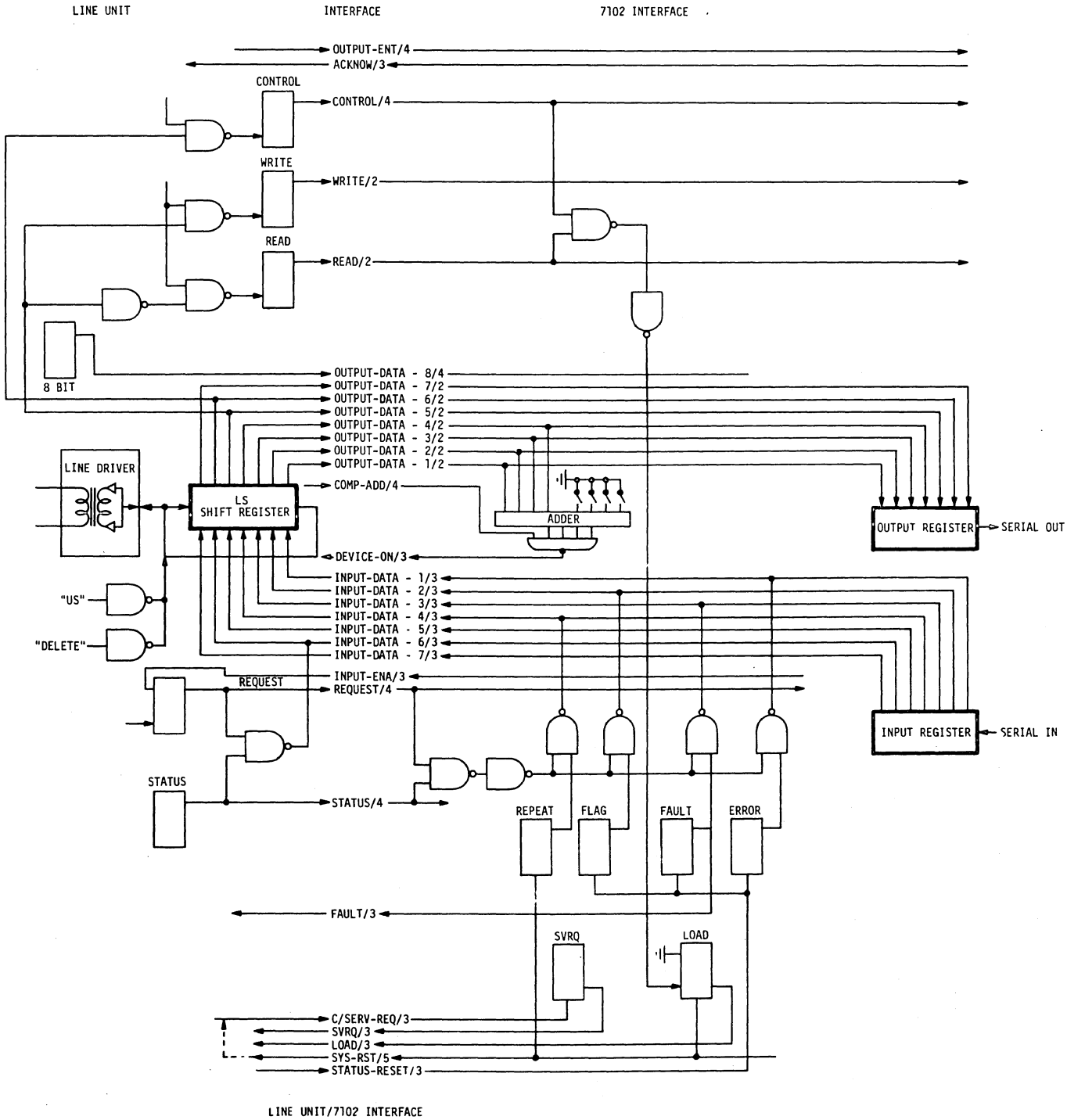

LINE UNIT
INTERFACE
7102 INTERFACE
OUTPUT-ENT/4
ACKNOW/3
CONTROL
CONTROL/4
WRITE
WRITE/2
READ
READ/2
8 BIT
OUTPUT-DATA - 8/4
OUTPUT-DATA - 7/2
OUTPUT-DATA - 6/2
OUTPUT-DATA - 5/2
OUTPUT-DATA - 4/2
OUTPUT-DATA - 3/2
OUTPUT-DATA - 2/2
OUTPUT-DATA - 1/2
LINE DRIVER
LS
SHIFT REGISTER
COMP-ADD/4
ADDER
OUTPUT REGISTER
SERIAL OUT
DEVICE-ON/3
INPUT-DATA - 1/3
INPUT-DATA - 2/3
INPUT-DATA - 3/3
INPUT-DATA - 4/3
INPUT-DATA - 5/3
INPUT-DATA - 6/3
INPUT-DATA - 7/3
"US"
"DELETE"
REQUEST
INPUT-ENA/3
REQUEST/4
INPUT REGISTER
SERIAL IN
STATUS
STATUS/4
REPEAT
FLAG
FAULT
ERROR
FAULT/3
SVRQ
LOAD
C/SERV-REQ/3
SVRQ/3
LOAD/3
SYS-RST/5
STATUS-RESET/3
LINE UNIT/7102 INTERFACE

FIGURE 14-4

1. BREAK AND LOCAL

The 7102 operates either in a LOCAL mode, where all signals are contained within the 7102, or NOT LOCAL, where the keyboard and tape reader transmit to the processor, and the typebar/printer and punch receive from the processor. The BREAK switch, through circuitry in the interface, changes the operation from local to not local. Each successive depression of the BREAK key (for 1/4 second or more) toggles the mode of operation in and out of local. Visual indication is given to the operator by the 7102. The printer types a left-hand paren, (, when the unit is in LOCAL, and a right-hand paren,), when the unit is ready to converse with the computer. Local/not local switching circuitry is located on Card FII in the 7102 Interface. Local switching is one of the conditions where the unit must generate and execute special commands to prepare for I/O activities with the processor. In this case the printer is turned on, the punch is turned off, and the paren is typed.

During the time the 7102 is in LOCAL, communication to and from the Line Unit is blocked. The FAULT flip-flop remains set, until the 7102 is out of LOCAL, preventing character loading from the interface to the Line Unit shift register. REM-LOCAL flip-flop prevents character loading in the opposite direction during this time. A general description of generating a character, and switching to LOCAL is given below.

a. BREAK TO LOCAL

When the BREAK key is depressed, the clock is started, and with the exception of the STP (stop) bit position, the input shift register is loaded with 1's. The STP bit position is loaded with a zero. The interface begins receiving the break, a constant zero, as a normal character. The one bits that were loaded by the first clock pulse shift through and out. The zero is shifted through until it is detected by CMI. The clock is stopped, and the register is placed in the parallel mode, as it is with any normal character. However, a normal character would have two stop marks at this point, making SERIAL IN/7 high. With no stop marks (SERIAL IN/7 still low) and the CMO signal active, the BREAK/3 signal is qualified, and LOCAL is set.

When the BREAK key is released, the signal from the 7102 becomes a mark, and through interaction of the D and E flip-flops, the printer-on code is put on the OPR (output register) lines. The clock is started, shifting the printer-on code from the output register to the 7102. When the character is completely shifted out, the clock is stopped, and the printer is turned on. The D flip-flop resets causing the P and Q flip-flops to place the punch off code onto the OPR lines. The clock is restarted, the character is shifted out, and the punch is turned off and the clock stopped. P resetting causes the L and M flip-flops to send the left parenthesis code, (, to the 7102.

b. BREAK FROM LOCAL

When the BREAK key is depressed, and the local flip-flop is set, a routine similar to the Break To LOCAL is performed. The READ and WRITE lines are then checked. If neither line is active, the right parenthesis code is sent to the 7102. If the READ or WRITE lines are active the interface waits for STATUS, then sends the right parenthesis to the 7102.

c. CONTROL QUESTION MARK (?)

As an interrogation of the local/on-line status, the 7102 Interface may receive a write control select character, followed by a question mark. The hardware examines the status, and if LOCAL is set, FAULT status is given. The write control, or any legal message, will report FAULT status when the 7102 is in LOCAL, but the question mark inhibits the OUT-DATA lines, and will not print the ? whether or not the 7102 is in LOCAL. If however, LOCAL is not set, normal status is given to the Line Unit verifying on-line status to the program.

2. PUNCH OR I/O (PRINTER AND KEYBOARD)

For easy reference, the keyboard/printer portion of the 7102 terminal is referred to as the I/O device. If either the punch or the I/O device are selected, the acknowledge and data transfer are inhibited temporarily, and DEVICE-ON is sent to the Line Unit. The flip-flop for the particular device is set (i.e. I/O FF or PUNCH FF). After preparations are made, such as printer-on, or punch-on, etc., the acknowledge and data transfer are restored.

a. I/O WRITE

A normal write character is parallel strobed from the Line Unit to the output register. The clock is started, and the character is serially shifted out to the 7102. When the character shift is complete, ACKNOW is given to the Line Unit, and the interface is ready for another character. WRITE character codes are received, and relayed until the Line Unit requests status. When status is requested the interface disconnects the register from the Line Unit, turns the 7102 printer off, and when the register is empty, it sends status.

b. WRITE CONTROL

A WRITE CONTROL can be a horizontal tab, carriage return, back space, or an asterick (load horizontal tab counter). Normal interface actions are inhibited during these activities so that special operations can be performed. The flow chart in Figure 14-9 generalizes the action of these events. For a more detailed explanation of the workings of these codes, see the paragraph of that heading (i.e. see HORIZONTAL TAB for analysis of that action).

c. PUNCH

Punch selection is similar to the I/O device, but if the instruction is a READ (a punch cannot read) FAULT status is sent, and the interface waits for another instruction.

WRITE CONTROL characters are forwarded to the punch as data characters. However, if the printer has been manually activated, control codes received by the printer (such as carriage return, etc.) will be performed by the printer.

d. I/O READ

A READ instruction, or a READ CONTROL command cause the printer-on code to be sent to the 7102. A normal READ causes an E code to be sent to the 7102 (after checking to be sure the output register is empty). A READ CONTROL causes an L code to be sent.

d. I/O READ (Cont.)

In either case, the operator then hits a data key on the 7102 keyboard, and the character bits are received by the interface. Each bit is serially clocked into the register until Count Mode goes low, indicating a full character is in the register. The character (from the 7102) is tested for STX, SOH, ETX, and DLE. The SOH and DLE set status flip-flops ERROR and FLAG respectively, and the ETX sets SERV-REQ. If the character is an STX (load request) the LOAD flip-flop is set, but also the READ and CONTROL lines from the Line Unit are examined. If both READ and CONTROL are active, the ERROR flip-flop is set.

After examination for control codes, the character is passed to the Line Unit, and the REQUEST signal going away shows that the Line Unit has taken the character; INPUT-ENA is reset. If the Line Unit is not requesting status, the interface returns to the ENTER DATA state, and waits for the next incoming character from the 7102. When the program count is exhausted, and the Line Unit requests STATUS, the interface disconnects the register from the Line Unit, turns the printer off, and when the register is empty, it sends status, then waits for another instruction.

e. LOAD (READ CONTROL)

If any of the characters coming from the 7102 are an STX, the LOAD-REQuest flip-flop is set. If when LOAD-REQ is set, READ and CONTROL are active (these are the Line Unit Signals) the ERROR flip-flop is set. In any case when LOAD-REQ is set the Line Unit terminates the action by sending a unit separator to the I/O channel. Shortly after LOAD-REQ is set the ACU returns a READ CONTROL instruction. The READ and CONTROL signals become active, clocking LOAD-REQ reset as the leading edge of the signals enter. When the output register is empty, the printer-on code is sent to the 7102, and again when the register is empty, an L is sent.

The operator hits a data key on the 7102 keyboard and the character bits are serially clocked into the register. When the character shift is complete (Count Mode going low), the register is placed in a parallel mode, and providing the Line Unit is requesting data, the character is parallel transferred to the Line Unit shift register. The interface waits for the character to be taken away (REQUEST going away) and if status is not requested it returns for another character. If status is requested, the input register is disconnected from the Line Unit, the 7102 printer is turned off, and the operation terminated by sending status.

3. READER

After determining that the 7102 is not in LOCAL, and the reader is addressed, the READER flip-flop is set and DEVICE-ON is sent to the Line Unit.

a. WRITE INSTRUCTION

A WRITE instruction is not a valid code to the reader. FAULT is set, status is given to the Line Unit, and the interface returns to wait for a new instruction.

b. WRITE CONTROL

A write control instruction to the reader is acknowledged without sending the code to the 7102. Status is given when requested, as in any normal transfer. This allows the ? under write control to be answered with good status, if the 7102 is not in LOCAL.

c. READ

A READ instruction is examined for parity, and ERROR is set if parity is bad. If the instruction is a READ CONTROL, FAULT status is sent to the Line Unit, and the interface returns for another instruction. When a normal READ instruction is received, the reader-on code is sent to the 7102 (after making sure the input register was empty).

The reader sends data, which is serially clocked into the shift register, one character at a time. As the last bit of a character enters the register, the Count Mode signal converts the register to a parallel shift mode (see RECEIVE). The Line Unit requesting data, and the full register cause INPUT-ENAble to parallel strobe the character into the Line Unit. The interface waits for REQUEST to leave, indicating the Line Unit has taken the character, before resetting INPUT-ENA-le. If status is not requested, the next character is clocked into the register as before. Character transfer is repeated until the program count is exhausted, and status is requested. With the Line Unit requesting status, the message is over. The register is disconnected from the Line Unit, status is given, and the interface returns for another instruction.

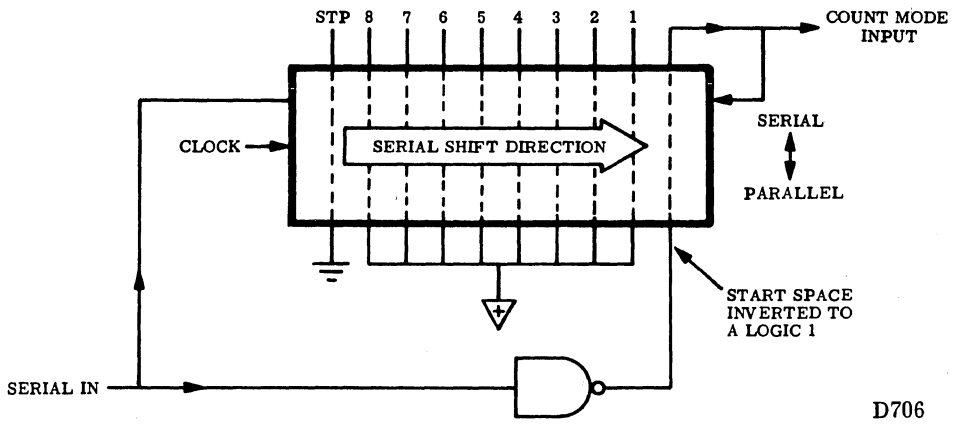
4. RECEIVE

The input shift register (IPR) is initially in the parallel shift mode (COUNT MODE low). The IPR data lines are preset to parallel load all bit positions with a logic 1, except the stop bit (STP) which is loaded with a logic zero. The start pulse of the incoming character (from the 7102) starts the timing clock to the shift register.

The inverted start pulse is placed on the lower order bit position. This is a detection position for character length. Figure 14-5 shows a graphic representation of the shift register, and the logic levels that are hardware loaded.

4. RECEIVE (Cont.)

When the first clock pulse arrives, the register is loaded with the hardware levels, and the inverted start space. The logic 1 from the inverted start space is detected, causing CMI (Count Mode Input) to go high, and the register to operate in serial.



INPUT SHIFT REGISTER

FIGURE 14-5

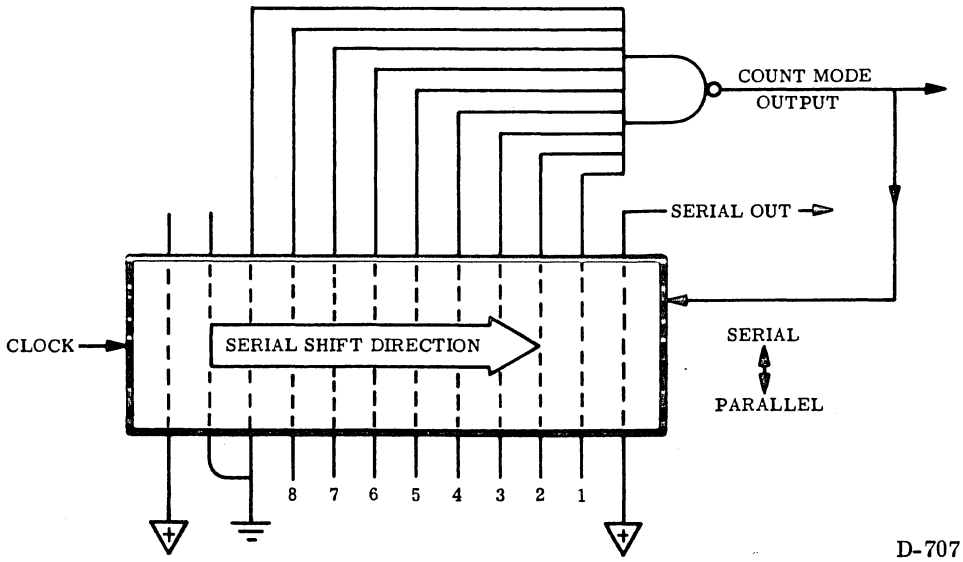
The following clock pulses shift the 1's off the end of the register, and the information into the register. When the zero that was initially loaded into the STP bit position is detected by Count Mode, the register changes to parallel operation, the clock is stopped, and INput-ENAble is sent to the Line Unit. The Line Unit accepts the character without changing the interface register, and the sequence is set to start again on the next start pulse.

5. TRANSMIT

COUNT MODE OUTPUT (CMO) is the signal that determines the parallel or serial operation of the output shift register, and is generated by the bits contained in the register. The parallel output of the register is monitored by a nand gate. If all eight character bits, and the first stop bit position are a logic 1, CMO becomes low, placing the shift register in the parallel mode. If one or more of the bits are logic zero, CMO is high, and the register operates in serial.

5. TRANSMIT (Cont.)

When a character is on the OPR (output register) lines, and is ready for transmission to the 7102, the clock is started. Figure 14-6 shows a graphic representation of the shift register, and the hardware logic levels that are loaded into it. The first clock pulse to reach the register parallel strobes the preset levels into the register, and the start bit directly onto the output line (SERIAL OUT). As is shown in the illustration, the two stop bit positions are loaded with zeros, and the highest order bit is held at logic 1.



OUTPUT SHIFT REGISTER

FIGURE 14-6

When the zero in the higher order position (one of the stop bits) is strobed into the register, CMO (Count Mode Output) goes high, and the register is in the serial mode. The clock pulses that follow, shift the bits through the register, and out onto the line (SERIAL OUT). As the bits are shifted out, the 1's created in the highest order position fill the register. When the register is all 1's, CMO becomes low, the clock is stopped, and the register is placed in parallel operation. The bits are not parallel transferred because the clock has stopped. Notice that if the character had been all 1's, it would still be shifted through because of the two stop bit zeros. Serial Out remains at logic zero (from the last stop mark).

Before the logic levels are sent to the 7102, there is a double inversion, and a volaage level shift. The 7102 mark condition is appriximately -12 volts and a space approximately +5 volts.

6. SPECIAL CODES

Some I/O operations cause the 7102 Interface to generate and transmit codes to prepare the 7102 Terminal for incoming instructions. Some of the same codes, and others, can also originate in program. If the control codes come from the processor, the 7102 Interface forwards the code as a character (after changing the mark/space voltage levels to TTY compatable). Table 14-1 shows a list of the 7102 control codes. The codes marked by an asterick (*) can be generated internally by the 7102 Interface in preparation for specific I/O operations. The flip-flops required to generate these codes are also listed in the table. The specific operations, requiring code generation, and preparation, are given in Table 14-2. The sequence of the generated codes is also given in the same table.

Internal codes are all developed in a similar manner, each by a pair of flip-flops. A typical truth table for one pair of the code generating flip-flops is shown in Table 14-3.

Control codes can also originate from the keyboard of the 7102. Table 14-4 is a list of operator generated codes (from the 7102), and the action that is taken by the 7102 Interface when one of these codes is received.

7102 CONTROL CHARACTERS

TABLE 14-1

	CHARACTER	H	M	I	* SI	* DC1	* DC2	* SO	DC3	* DC4	* E	* L	* (	*)
BIT	7	0	0	0	0	0	0	0	0	0	1	0	0	1
	6	0	0	0	0	0	0	0	0	0	0	0	0	0
	5	0	0	0	0	1	1	0	1	1	0	0	0	0
	4	1	1	1	1	0	0	1	0	0	0	1	1	1
	3	0	1	0	1	0	0	1	0	1	1	0	0	0
	2	0	0	0	1	0	1	1	1	0	0	0	1	1
	1	0	1	1	1	1	0	0	1	0	1	1	0	0
	(FLIP-FLOPS)				D E	D E	D E	H I		P Q	F G	J K	L M	N O
	Inst. to 7102	BACKSPACE	CARRIAGE RETURN	HORIZONTAL TAB	PRINTER ON	READER ON	PUNCH ON	PRINTER OFF	READER OFF**	PUNCH OFF	ENTER	LOAD	LOCAL	NOT LOCAL

*Preparation codes that can be generated by the interface.
**The reader turns off only if the DC3 code is read by the reader itself.

SEQUENCE OF INTERNALLY GENERATED CODES

TABLE 14-2

OPERATION	CODE SEQUENCE
READ Device Ø	Printer on, E
READ Device 9	Reader on
WRITE Device Ø	Printer on
LOAD (from ACU)	Printer on, L
WRITE Device 8	Punch on
BREAK.LOCAL	Printer on,), Printer off
BREAK.$\overline{\text{LOCAL}}$	Printer on, Punch off, (
STATUS.PUNCH OFF	Printer off
STATUS.PUNCH [illegible]N	Punch off

TYPICAL TRUTH TABLE

TABLE 14-3

D	E	
0	0	Normal reset state
1	0	Code to shift register
1	1	Code loaded and transmitted
0	1	Permiss next code in sequence

OPERATOR GENERATED CODES

TABLE 14-4

CONTROL CHARACTER	DETECTED CHARACTER	ACTION
@	DLE	Set FLAG
A	SOH	Set ERROR
B	STX	Set LOAD
C	ETX	Set SVRQ

7. BACKSPACE AND CARRIAGE RETURN

The mechanical reaction time of the 7102 requires a time delay for either the backspace or carriage return. As there is no possible indication to the interface concerning the carriage position, a maximum delay time is allowed for each carriage return. The carriage return delay is approximately 1.21 seconds, and the backspace delay is only 200 milliseconds more than a normal character time, or approximately 310 ms total.

a. BACK SPACE

When a backspace code is detected (on Card FTI) the ACKNOW signal to the Line Unit is inhibited. Because of this the code remains on the OPR (output register) lines, and OUTPUT-ENAble from the Line Unit stays active. The backspace code is loaded and transmitted to the 7102 as a normal character. With OUTPUT-ENA active and the character still on the OPR lines, the character would be retransmitted, but transmission is now inhibited (INH-SER-OUT). The character is serially shifted out (to nowhere), reloaded and shifted again. A delay counter (on the FTI Card) is incremented each time a character is completely shifted out, until the counter reaches three. With the count of three, the delay is terminated, and ACKNOW given to the Line Unit.

b. CARRIAGE RETURN

A carriage return is similar to the backspace operation, except that the code is ring-shifted in the output register 12 times before the delay is terminated.

8. HORIZONTAL TAB

The interface receives a control asterick (*) from the processor. The next two characters received are loaded into the tens and units counters respectively as binary representations of the tab count. The horizontal tab command can come immediately or may follow at some later time. Once loaded, the tab counters decrement once for each character or space received or transmitted, and increment once for each backspace transmitted or received.

When the horizontal tab command is received (CONTROL I), the interface inhibits the ACKNOW signal to the Line Unit, sends space codes to the 7102, and decrements the counter once for each transmission. When the tab count is exhausted, the ACKNOW signal is given to the Line Unit, and the interface is ready for the next operation.

9. STATUS

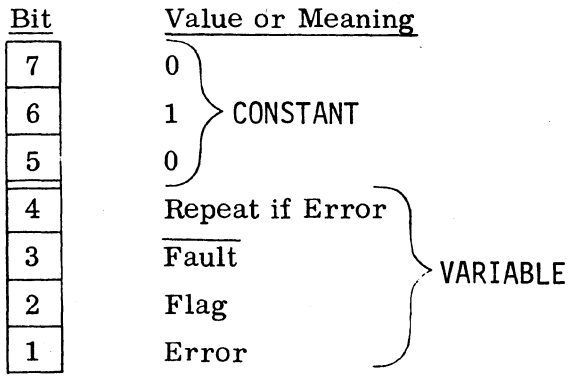
When status is requested by the Line Unit the interface sends a printer off, and a punch-off, code to the 7102, and loads the status bits into the Line Unit shift register. The status character is shown in Figure 14-7 and the meanings are as follows:

ERROR - (1) A parity error was received.
(2) The Line Unit did not request data in READ.
(3) The Line Unit failed to request status.
(4) The operator sent a control A (SOH).
(5) The operator terminated the instruction with a load request.
(6) Line Unit failed to accept character before next one comes along.

FLAG - (1) Operator sent control @ (DLE).

FAULT - (1) Reader not on for READ instruction.
(2) Reader is on for a WRITE instruction.
(3) Punch on for a READ instruction.
(4) 7102 is in LOCAL.
(5) Reader is on and READ CONTROL (LOAD) instruction is given.

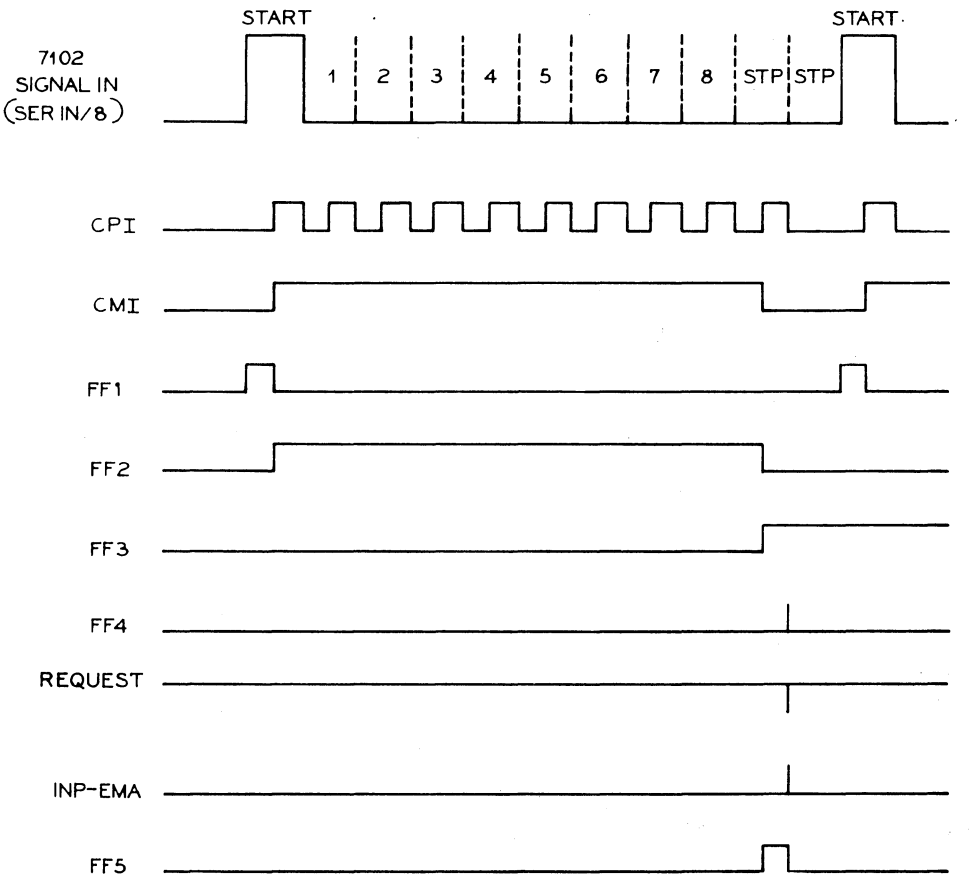
REPEAT IF ERROR -
(1) 7102 interface is not ON.



I/O STATUS CHARACTER

FIGURE 14-7

7102 INTERFACE



TIMING SIGNALS

FIGURE 14-8

C. OPERATOR REQUIREMENTS

1. POWER-ON

Place the 7102 color switch in the XMIT-RECV position. Turn on the 7102 power. If the computer has been off, a left paren, (, will be typed when the computer is powered up and the 7102 will be in LOCAL. Power to the 7102 Interface is supplied from the processor power supply.

2. LOCAL/NOT LOCAL

If a left paren, (, was typed, the 7102 is in LOCAL. If not, it may be placed in LOCAL by depressing the BREAK key for 1/4 second or more. When the key is released the paren will be typed. To remove the 7102 from LOCAL, depress the BREAK key again (for at least 1/4 second) and when the key is released, a right paren will be typed. This indicates that the 7102 is out of LOCAL. If the processor is not looped into a program an L will be typed directly following the).

3. LOAD

When a hardware load is requested by the processor, the interface will generate, and the 7102 will print an L. If the operator wishes to request a LOAD condition, simultaneously press the CONTROL switch, and the letter B.

4. ENTER

If the processor requests an entry, the interface will generate, and the 7102 will type an E. The operator must then enter the characters required by program. NOTE: Letter characters may be tyeed in upper or lower case, but numbers must be typed in lower case. The processor always leaves the basket shift in upper case; release the basket shift before intering numbers.

5. RESET

Under certain illegal operating conditons (accidental misoperation) the flip-flop sequencing may become disoriented. If such conditions should appear, press the 7102 Interface reset on the FEN card.

D. TIMING

Basic timing for the 7102 Interface is located on the FTI circuit card and generated by a 440 Khz crystal oscillator. Two D flip-flops, connected in a divide-by-four circuit, feed three divide-by-ten counters. The resulting clock signal (CP OUT/4 and CP IN/4) is 110 Hz. Clock signals are gated to the transmit or receive shift registers, and are called CLOCK RUN IN/3 and CLOCK RUN OUT/3. Figure 14-8 shows some of the timing involved in the input and output register shifting.

E. LOGIC LOCATION

The 7102 Interface contains three printed circuit cards, FII, FTI, and FEN. The basic function of each card is outlined below.

1. FII

Contains the receive logic. Receives asynchronous serial input from the 7102 Terminal, and parallel shifts it to the Line Unit. The FII Card also contains decoding for special codes from the 7102.

2. FTI

Contains the transmit logic. Receives parallel codes from the Line Unit and transmits them asynchronously to the 7102. The FTI Card also contains logic for decoding certain codes from the Line Unit.

3. FEN

Contains code development logic for transmission to the 7102 to prepare it for IO operations. Also contains manual reset switch for the Interface.

4. HORIZONTAL TAB LOGIC LOCATION

The card location for the functional parts of the horizontal tab operation is given below.

FII - Horizontal Tab Counter
Load Control
ACU Countdown Logic
Zero Count Logic
ACKNOW/3 and SEND SPACE/3 Logic

FTI - 7102 Count DN Logic
Normal Count DN Logic

FEN - Data Disable Gates

F. SIGNAL GLOSSARY

ACK/2 - Gated to the FEN card at the beginning of transmission to the processor. Disables internal codes. Also gated to the Line Unit as ACKNOW.

ACKNOW - Informs the Line Unit that the character has been accepted and re-transmitted.

$\overline{C2}$ and $\overline{CL2}$ - Timing signals for backspace and carriage return delays.

CP IN - Clock Pulse Input - gated clock signal for input register.

CP OUT - Clock Pulse Output - gated clock signal for output register.

CLOCK RUN IN - Timing for shift registers.

CLOCK RUN OUT - Timing for shift registers.

CMI - Count Mode Input - Determines serial or parallel mode of register.

CMO - Count Mode Output - Determines serial or parallel mode ofrregister.

DOWN COUNT - Decrements counter in horizontal tab count.

HTC - Horizontal tab count.

IAS - Inhibit Acknowledge Strobe - stops normal code transfers while special preparation codes are generated and sent to the 7102. Also prevents ACKNOW during the same time.

INH-SER-OUT - Inhibit Serial Out - Prevents repeated transmission of BS or CR codes during delay cycle.

LOAD HIGH - Signal to load the tens counter for HTC.

LOAD LOW - Signal to load the ones counter for HTC.

PE - Parity Error.

REM LOCAL - Set by LOCAL; not reset until interface completely recovers from local. Blocks data gates from the Line Unit and holds FAULT set.

SC-STROBE and CMO - Qualifies transmission of internal codes.

SEND OK - Generated by several sources to qualify INP ENA.

SERIAL OUT - Data serial line to the 7102 Terminal.

STROBE - Developed for code transmission - initiates CLOCK RUN OUT/3.

?C/3 - Control question mark - Prevents transmission of question mark code when not in LOCAL.

ZERO COUNT - Signal that horizontal tab count is exhausted.

G. REFERENCE

1. 7102 INTERFACE SIGNAL LIST

SIGNAL NAME	POINT	POINT
*C/3	FTI-91*	FEN-91
?C/3	FTI-30*	FEN-30
A/3	FTI-93*	FEN-93
ACK/4	FTI-102*	FEN-102
ACKNOW/3	FTI-41*	LU1-41
B/3	FTI-95*	FEN-95
BREAK+LOC/3	FII-25*	FEN-25
BREAK+LOC/4	FII-23*	FEN-23
C/SERV REQ/3	FII-67	FEN-67
C/SERV REQ/3	FEN-67	LU1-67*
√C/SERV REQ/3	LU1-67*	LU2-67*
√C/READ/3	LU1-99	LU2-99*
CLOCK RUN IN/3	FII-39*	FTI-39
CM-0/3	FTI-40*	FEN-40
CM-0/4	FTI-38*	FEN-38
COMP ADD	FTI-55	LU1-55*
√COMP ADD	LU1-55*	LU2-55
√COND REC	LU1-8*	LU2+8
CONTROL/3	FTI-92	FEN-92
CONTROL/4	FII-68	FTI-68
CONTROL/4	FTI-68	FEN-68
CONTROL/4	FEN-68	LU1-68*
CP-IN/4	FII-5	FTI-5*

√ Related signal, but not a direct part of the 7102 Interface.

1. 7102 INTERFACE SIGNAL LIST (Cont.)

SIGNAL NAME	POINT	POINT
DEVICE ON/3	FII-45*	LU1-45
DOWN COUNT/3	FII-24*	FTI-24
ERROR/4	FII-18	FTI-18*
ERROR D/3	FII-15*	FTI-15
ERROR SW/3	FIT-32*	FTI-32
FAULT/3	FTI-42*	LU1-42
FAULT/4	FII-20	FTI-20*
FLAG/2	FII-58*	NOT USED
√HLD LATCH/3	LU1-7*	LU2-7
HTC/3	FTI-28*	FEN-28
IA8/3	FTI-96	FEN-96*
I/O ON/1	FTI-27*	FEN-27
I/O ON/2	FII-19	FTI-19*
I/O ON/2	FTI-19	FEN-19
INPUT DATA1/3	FII-46*	FEN-46
INPUT DATA2/3	FII-47*	FEN-47
INPUT DATA3/3	FII-48*	FEN-48
INPUT DATA4/3	FII-49*	FEN-49
INPUT DATA5/3	FII-50*	FEN-50
INPUT DATA6/3	FII-51*	FEN-51
INPUT DATA7/3	FII-52*	FEN-52
INPUT DATA8/3	FII-22	NOT USED
INP ENA/3	FII-74*	FEN-74
INP ENA/3	FEN-74	LU1-74
√JUMP/3	LU1-98	LU2-98*
√JUMP+RESET/3	LU1-102	LU2-102*
√JUMP+RST/4	LU1-101	LU2-101*
√LATCH/3	LU1-18	LU2-18*
√LATCH/4	LU1-19	LU2-19*
LOAD/2	FII-57	NOT USED
LOAD/3	FII-43*	LU1-43
LOCAL/3	FII-35*	FEN-35
LOCAL2/4	FII-37*	FEN-37
0/3	FTI-29	FEN-29*
OK/4	FII-17	FEN-17*
OPR1/3	FTI-79	FEN-79*
OPR2/3	FTI-80	FEN-80*
OPR3/3	FTI-81	FEn-81*
OPR4/3	FTI-82	FEN-82*
OPR5/3	FTI-83	FEN-83*
OPR6/3	FTI-84	FEN-84*
OPR7/3	FTI-85	FEN-85*
OPR8/3	FTI-86	FEN-86*
OUTPUT DATA1/2	FTI-59	FEN-59
OUTPUT DATA1/2	FEN-59	LU1-59*
OUTPUT DATA2/2	FTI-60	FEN-60
OUTPUT DATA2/2	FEN-60	LU1-60
OUTPUT DATA3/2	FTI-61	FEN-61

√ Related signal, but not a direct part of the 7102 Interface.

1. 7102 INTERFACE SIGNAL LIST (Cont.)

SIGNAL NAME	POINT	POINT
OUTPUT DATA3/2	FEN-61	LU-61*
OUTPUT DATA4/2	FTI-62	FEN-62
OUTPUT DATA4/2	FEN-62	LU1-62*
OUTPUT DATA5/2	FTI-63	FEN-63
OUTPUT DATA5/2	FEN-63	LU1-63*
OUTPUT DATA6/2	FTI-64	FEN-64
OUTPUT DATA6/2	FEN-64	LU1-64*
OUTPUT DATA7/2	FTI-65	FEN-65
OUTPUT DATA7/2	FEN-65	LU1-65*
OUTPUT DATA8/2	FTI-66	FEN-66
OUTPUT DATA8/2	FEN-66	LU1-66*
OUTPUT ENA/4	FTI-69	FEN-69
OUTPUT ENA/4	FEN-69	LU1-69*
√P/JUMP/3	LU1-15*	LU2-15
√P/RESET/3	LU1-14*	LU2-14
√P/COUNT/3	LU1-16*	LU2-16
PUNCH ON/2	FTI-26*	FEN-26
READER ON/2	FTI-34*	FEN-34
READ/2	FII-72	Fen-72
READ/2	FEN-72	LU1-72*
√READ SIG/4	LU1-22	LU2-22*
REM LOC/4	FTI-98	FEN-98*
REQUEST/4	FII-7Ø	FEN-7Ø
REQUEST/4	FEN-7Ø	LU1-7Ø*
√RETURN	LU1-1Ø6	LU2-1Ø6*
√RETURN	LU2-1Ø6*	TB2-B1
√RST-T/3	LU1-17*	LU2-17
√S12/4	LU1-1Ø*	LU2-1Ø
√S13/3	LU1-9*	LU2-9
SC1/2	LU1-97	LU2-97*
SC2/2	LU1-96	LU2-96*
SC4/2	LU1-95	LU2-95*
SC8H/4	LU1-94	LU2-94*
SC8L/4	LU1-93	LU2-93*
SEND SPACE/3	FTI-88*	FEN-88
SERIAL IN/8	FII-6	TB1-A1*
SERIAL OUT/8	FTI-77*	TB1-B1
SET ERROR/4	FII-21*	FTI-21
SET IO/3	FT1-94*	FEN-94
SET PUNCH/3	FTI-9Ø*	FEN-9Ø
START NEG	LU1-1Ø5	LU2-1Ø5*
START NEG	LU2-1Ø5*	TB2-A2
STATUS/4	FII-71	FEN-71
STATUS/4	FEN-71	LU1-71*
STATUS RESET/3	FII-54	FTI-54
STATUS RESET/3	FTI-54	LU1-54*
STATUS RESET/3	LU1-54*	LU2-54
STROBE/3	FTI-89	FEN-89*
SVRQ/2	FII-56*	NOT USED

√ Related signal, but not a direct part of the 7102 Interface.

1. 7102 INTERFACE SIGNAL LIST (Cont.)

SIGNAL NAME	POINT	POINT
SVRQ/3	FII-44*	LU1-44
SYS RES/5	FII-53	FTI-53
SYS RES/5	FTI-53	FEN-53
SYS RES/5	FEN-53	LU1-53
SYS RES/5	LU1-53	LU2-53
SYS RES/5	LU2-53	TB4-A2*
SYS RES/6	FII-33	FTI-33
SYS RES/6	FTI-33	FEN-33*
TØ/4	LU1-13*	LU2-13
T4/3	LU1-11*	LU2-11
TC1/2	LU1-92	LU2-92*
TC2/2	LU1-91	LU2-91*
TC4/2	LU1-9Ø	LU2-9Ø*
TC8/4	LU1-89	LU2-89*
TURN ON/3	LU1-56*	LU2-56
UP COUNT/3	FII-75*	FTI-75
WRITE/2	FTI-73	FEN-73
WRITE/2	FEN-73	LU1-73*
√WRITE ENA/4	LU1-1Ø4*	LU2-1Ø4
√WRITE INFO/3	LU1-1Ø3*	LU2-1Ø3
√XTAL IN	LU1-6	LU2-6*
√XTAL CUT	LU1-5	LU2-5*
√XXD/3	LU1-2Ø	LU2-2Ø*
ZERO COUNT/3	FII-76	FTI-76*
GROUND	FII-1&2	FTI-1&2
GROUND	FTI-1&2	FEN-1&2
√GROUND	FEN-1&2	LU1-1&2
√GROUND	LU1-1&2	LU2-1&2
GROUND	FII-1Ø9&11Ø	FTI-1Ø9&11Ø=
GROUND	FTI-1Ø9&11Ø	FEN-1Ø9&11Ø
GROUND	FEN-1Ø9&11Ø	LU1-1Ø9&11Ø
√GROUND	LU1-1Ø9&11Ø	LU2-1Ø9&11Ø
+5 VOLTS	FII-3&4	FTI-3&4
+5 VOLTS	FTI-3&4	FEN-3&4
+5 VOLTS	FEN-3&4	LU1-3&4
√+5 VOLTS	LU1-3&4	LU2-3&4
+5 VOLTS	COMMON BUS	TB4-A1*
√+15 VOLTS	LU1-1Ø7&1Ø8	LU2-1Ø7&1Ø8
√+15 VOLTS	LU1-1Ø7&1Ø8	TB4-B2*
-12 VOLTS	FTI-1Ø6	TB4-B1

√ Related signal, but not a direct part of the 7102 Interface.

CENTRAL PROCESSING UNIT

7102 INTERFACE

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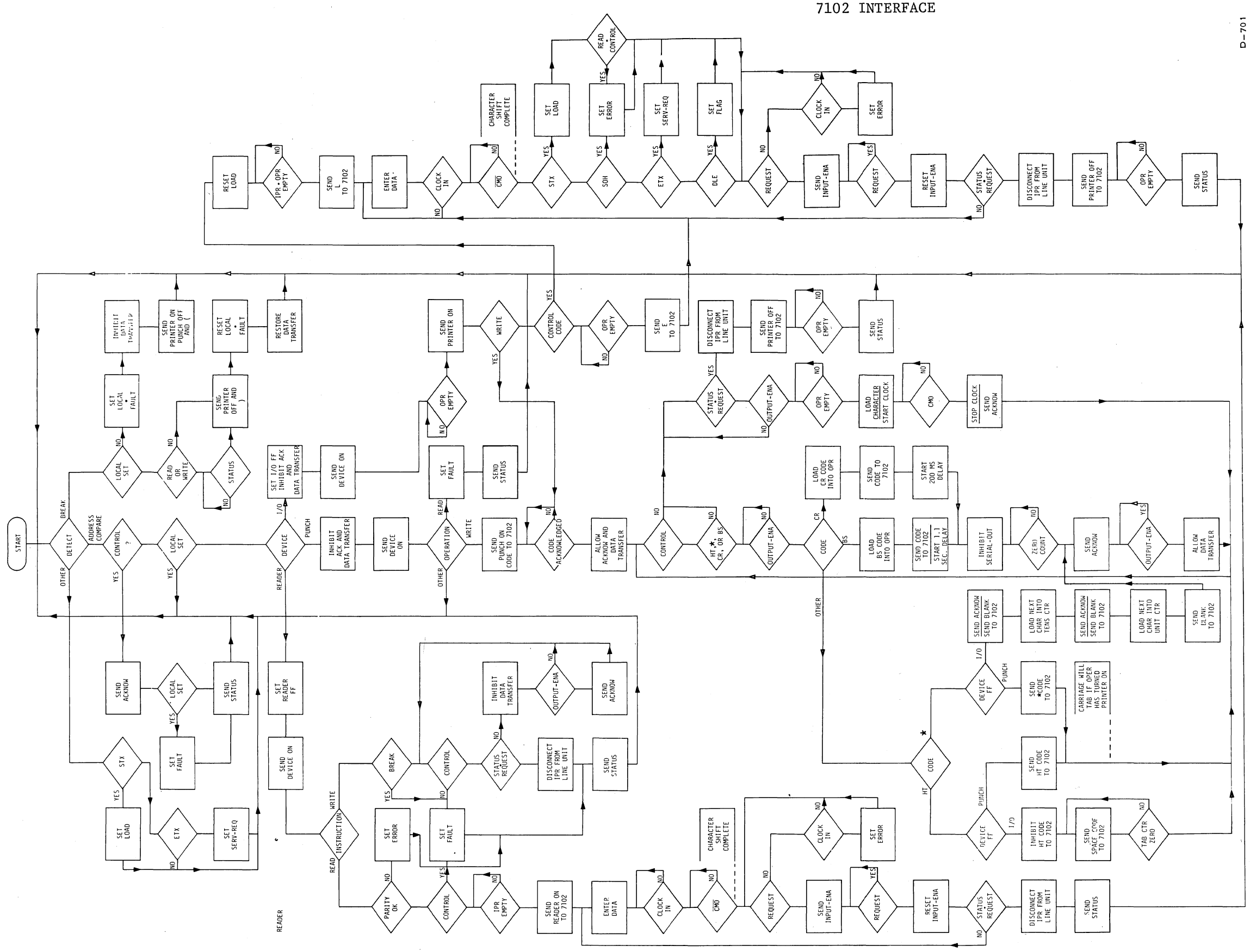
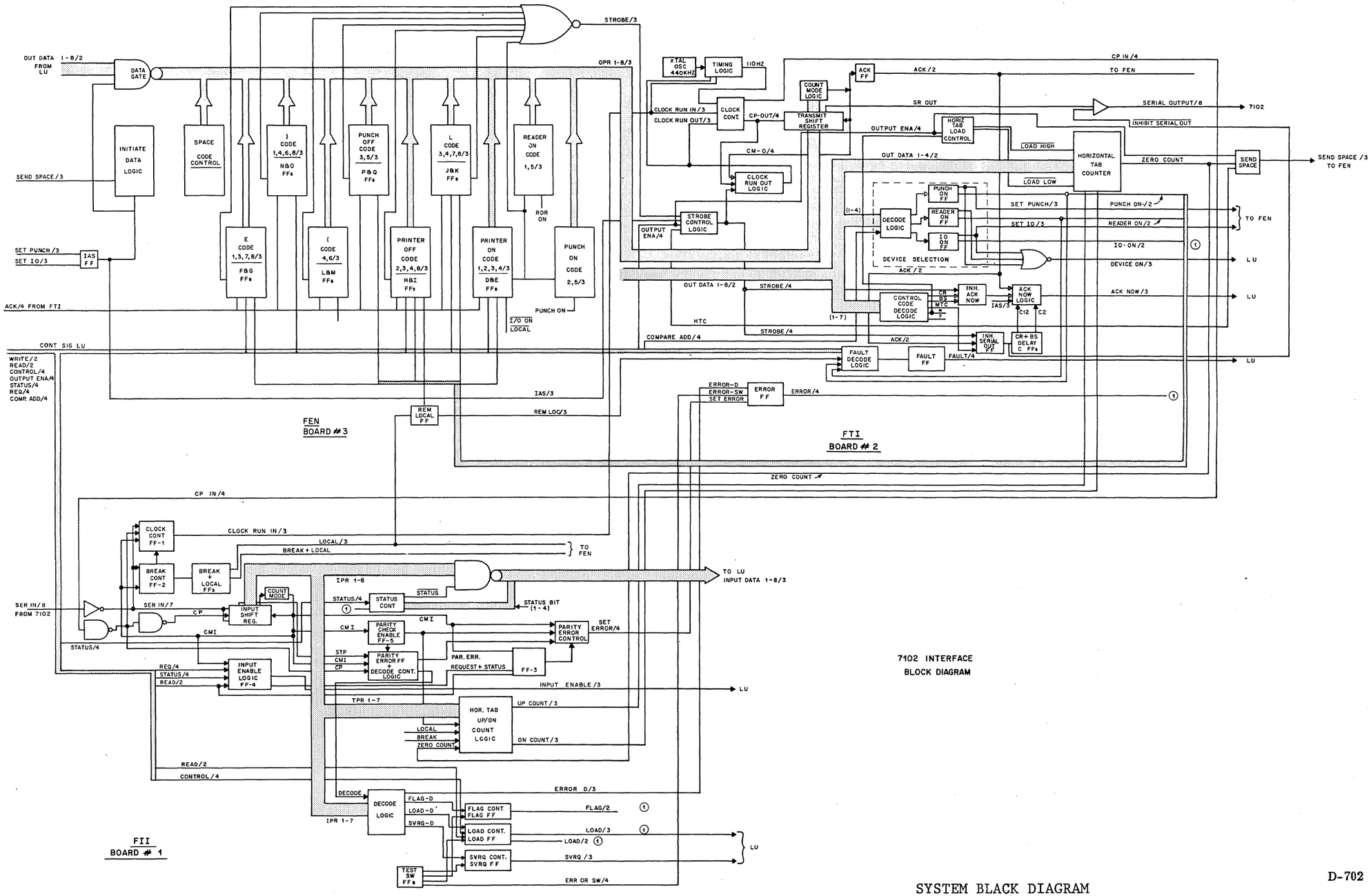


SYSTEM FLO DIAGRAM

FIGURE 14-9



7102 INTERFACE
BLOCK DIAGRAM

SYSTEM BLACK DIAGRAM

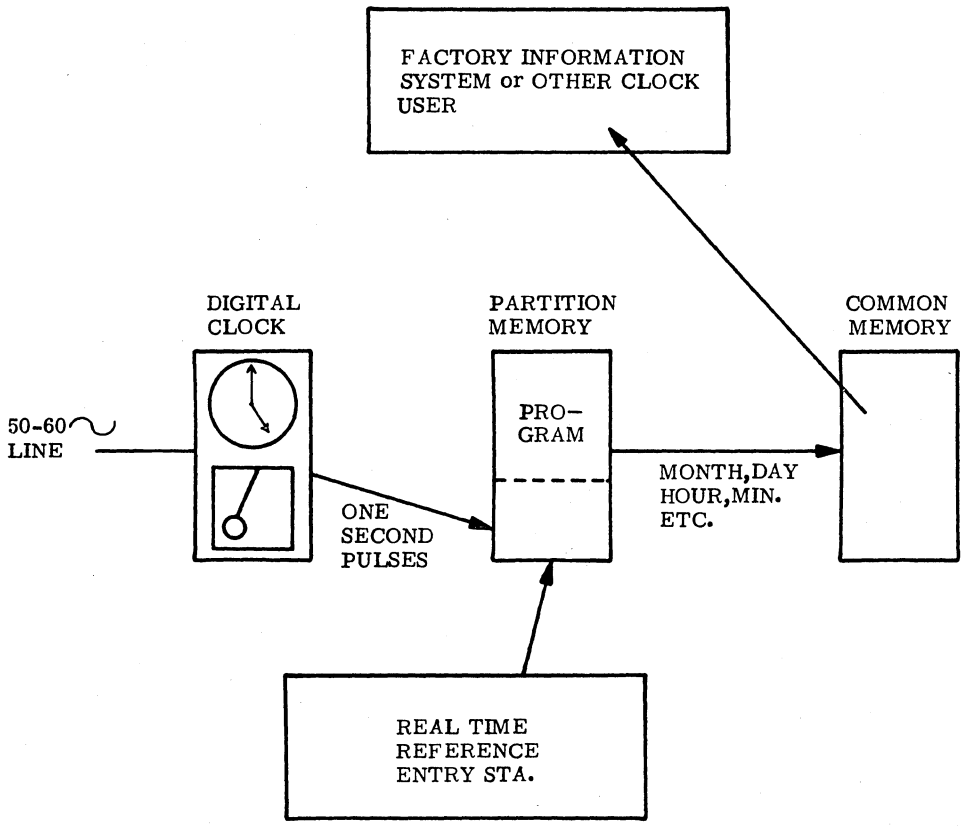
FIGURE 14-10

SECTION 15

DIGITAL CLOCK

SECTION CONTENTS

LIST OF ILLUSTRATIONS



SYSTEM CONCEPT

FIGURE 15-1

SECTION 15, DIGITAL CLOCK

A. INTRODUCTION

The Digital Clock is a "real time" reference generator for the processor and its peripherals. Residing in any of the processor I/O positions, the Digital Clock is also the central control for the Line Switching Unit. The Digital Clock also contains provision for synchronization with an external clock source.

The Digital Clock produces one number every second, and offers it to the ACU by setting SERVice-REQuest. Normally the service request is answered by a READ instruction, and the number is used to update a program routine. This program routine may create other time increments such as decimal parts of an hour, minutes, hours, days, etc., or the number may simply update an ascending program sequence.

If for some reason the service request can not be answered within the one second interval, the next count increases the offered number by one, and the service request remains set. The number that is offered can be increased to the count of nine (although that would be unusual). Upon the count of ten, FLAG is set, indicating the need for an external time update. Simply stated, if FLAG is not set in the Digital Clock partition, the accumulated program count is accurate to within nine seconds.

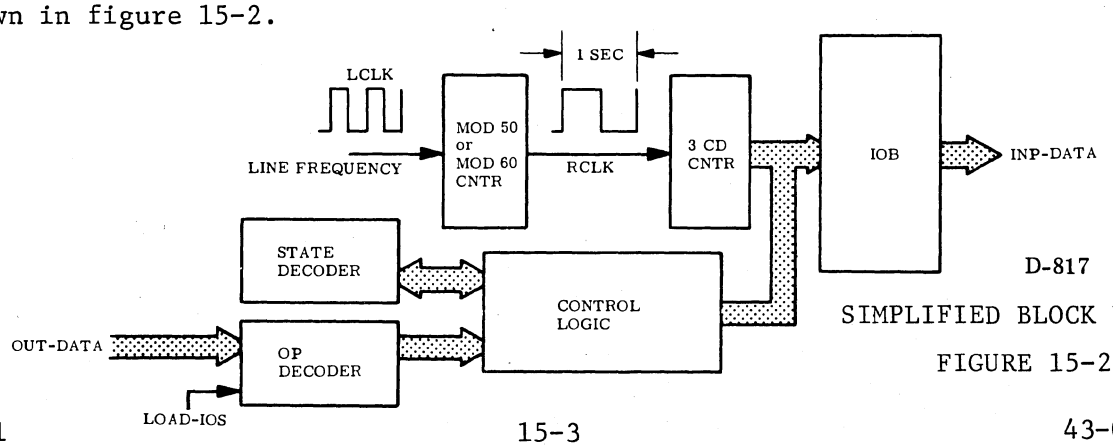
Synchronization with an external time source is accomplished when the external clock interface places a BCD number on the INP-DATA lines of the Digital Clock. When the next service request is answered by the ACU, the BCD number is stored in memory for reference by the software. The storage and use of the synchronization cue from the external clock interface is similar to the device number storage and use by the Multi-terminal IOC.

When the Digital Clock receives a load request with no device number (READ CONTROL) from the ACU, it sets normal status, and clears IO BUSY. This causes the ACU to start a set of instructions beginning at location 0000 in the Digital Clock partition. If a proper device number (LA) is a part of the READ CONTROL instruction, the Line Switching Unit can be made to switch to "standby", or back to "normal", or a relay will close for ten seconds, activating a separate warning.

The Digital Clock can not transmit data, consequently if it receives a WRITE or WRITE CONTROL instruction, the CHECK flip-flop is set, and the instruction is terminated by clearing IO BUSY.

B. OPERATION

The Digital Clock divides the 50 or 60 Hz power-line frequency by the base number (50 or 60) to arrive at one-second pulses. The internal one-second pulse signal is RCLK, and one full cycle of RCLK is one second long. Basic Digital Clock operation is shown in figure 15-2.



SIMPLIFIED BLOCK DIAGRAM

FIGURE 15-2

The line frequency counters are prewired at the time of installation to divide the power frequency into one second pulses. Figure 15-3 shows both configurations of the frequency dividers, and the basic logic that is involved. Three JK flip-flops, SDF1, SDF2, and SDF3 divide the basic line frequency by 5 or 6, according to the configuration, and the signal is fed to a modulo ten counter that completes the frequency division.

The expanded block diagram in figure 15-4 shows some of the individual logic actions. Notice that the State Counter is synchronized to the IOC-LF-CLK signal from the ACU.

The advance for the State Counter is controlled by the PCR flip-flop. The PCR flip-flop can only be set (actually preset) if both the State Counter toggle signal (T/S) and the IOC-LF-CLK signal are present at the same time. As a result, the State Counter only advances in synchronism with the IOC-LF-CLK. The State Counter can be cleared, however, by IO-RST, a new instruction, or if IO BUSY is not present in S1.

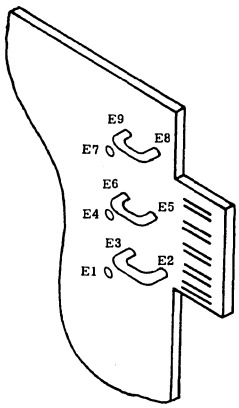
IOB is the output buffer register, and consists of four D type flip-flops. Each flip-flop represents one of the four lower order bit lines of the INP-DATA bus. The contents of IOB can either be the BCD number that is to be transfered to the ACU, or the status character for the Digital Clock.

1. LOGIC ACTION

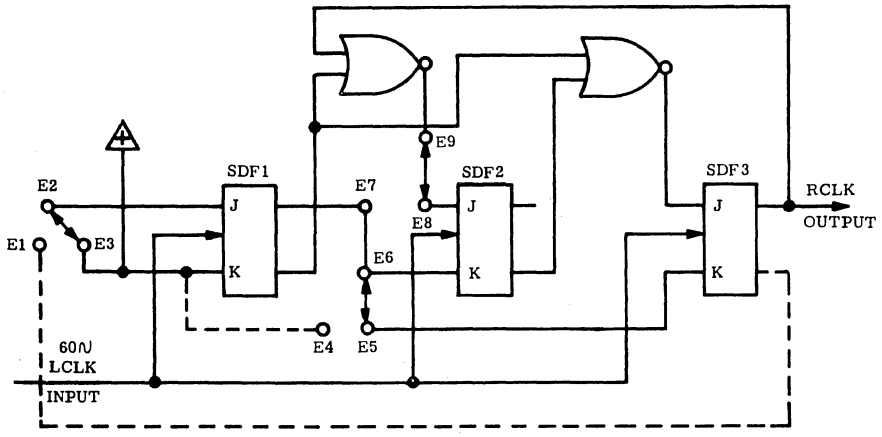
Figure 15-5 is a flow chara of the basic Digital Clock logic operation. The paragraphs below explain the processes shown in the chart.

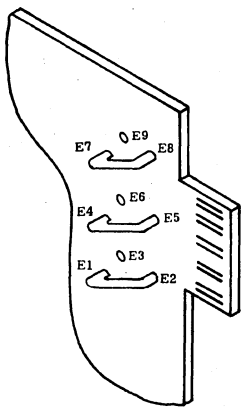
During power-up, either initially, or after a power failure, all flip-flops are reset. This clears the FAULT bit (bit3) and leaves an indication of FAULT status. No further action is taken until the first RCLK pulse arrives. The leading edge of the RCLK pulse sets SERV-REQ, and toggles the BCD counter (incrementing it). As RCLK leaves, the falling edge of the pulse toggles the START flip-flop, initiating the State Counter (SCTR). START is cleared by the State Counter stepping to S1. In S1 the BCD counter is checked, and if the count is greater than 9, FLAG is set. If when S1 is entered, IO BUSY is not already set, the State Counter is cleared, and the initial sequence begins again (however the BCD counter is not cleared). Normally IO Busy is set (by the ACU) long before the Digital Clock steps to S1, as the ½ second interval is quite long compared to processor speeds. However the BCD counter is incremented every second, and SERV-REQ remains set until it is answered. When the service request is answered, and IO BUSY is set, the State Counter is free to step from S1 to S2 during the next one second sequence.

DIGITAL CLOCK

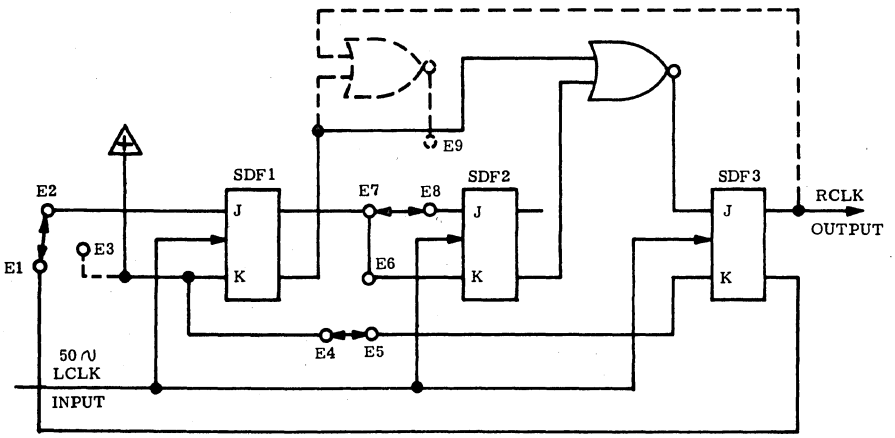


60





50Ω



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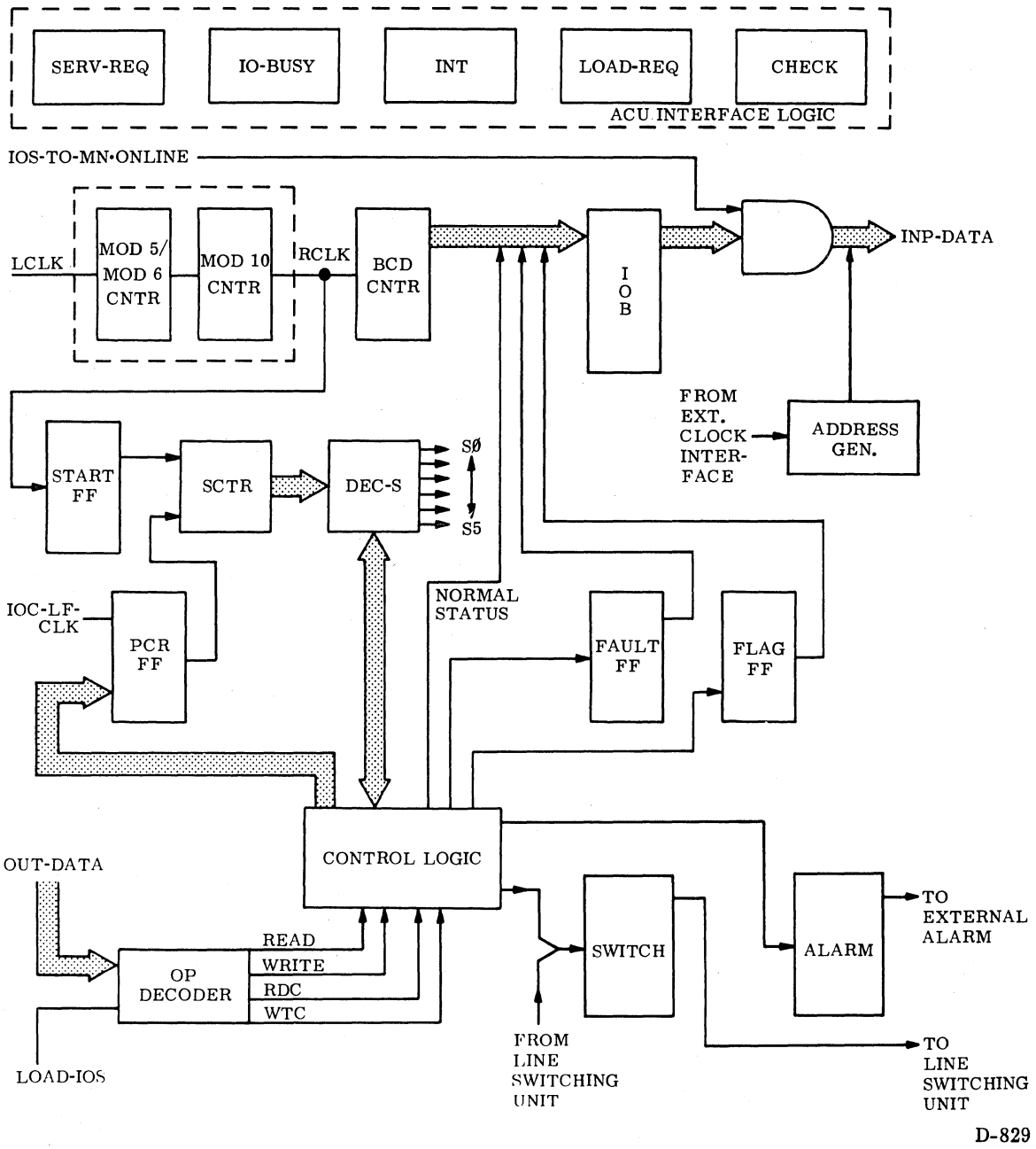
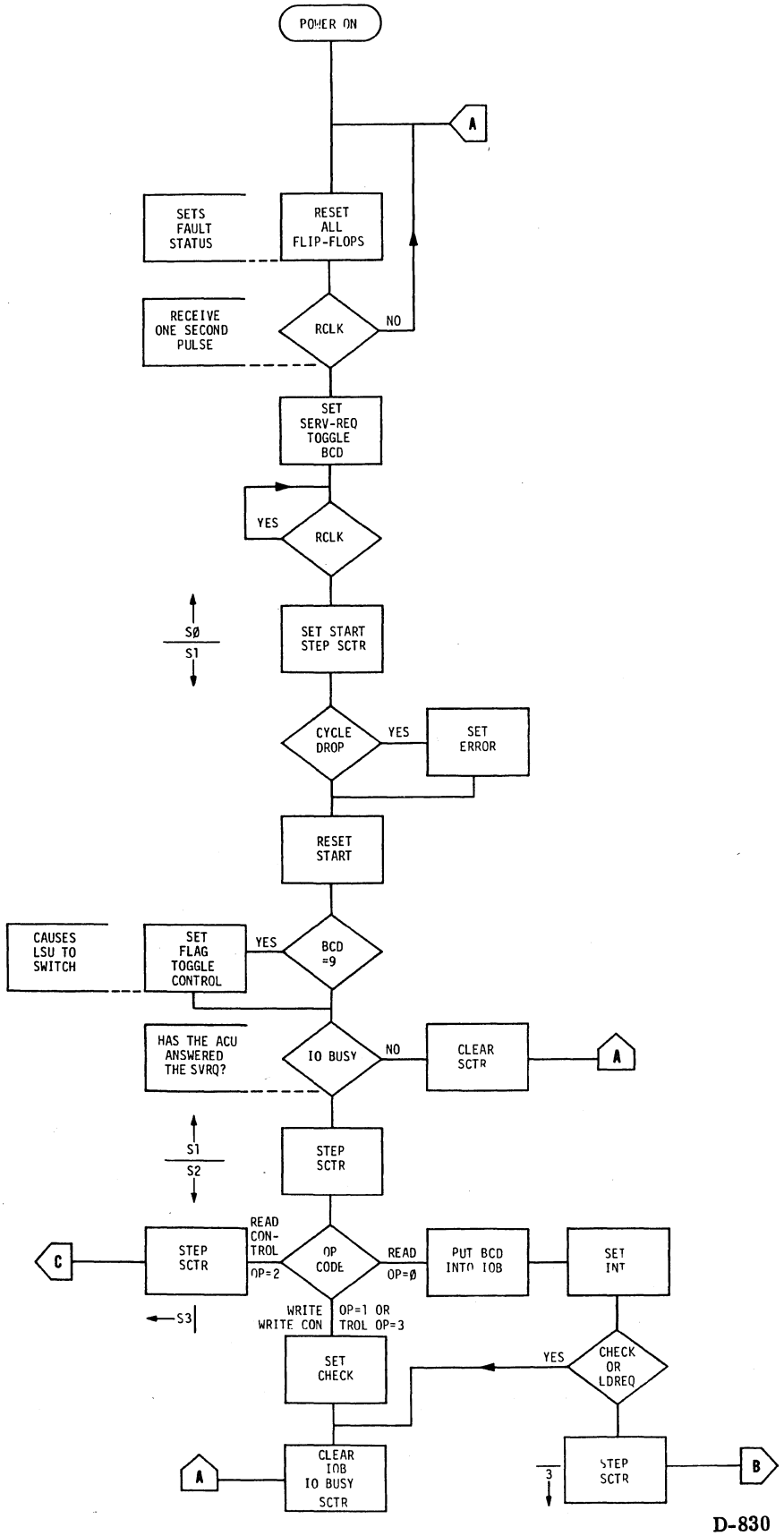
ONE SECOND TIMER

FIGURE 15-3



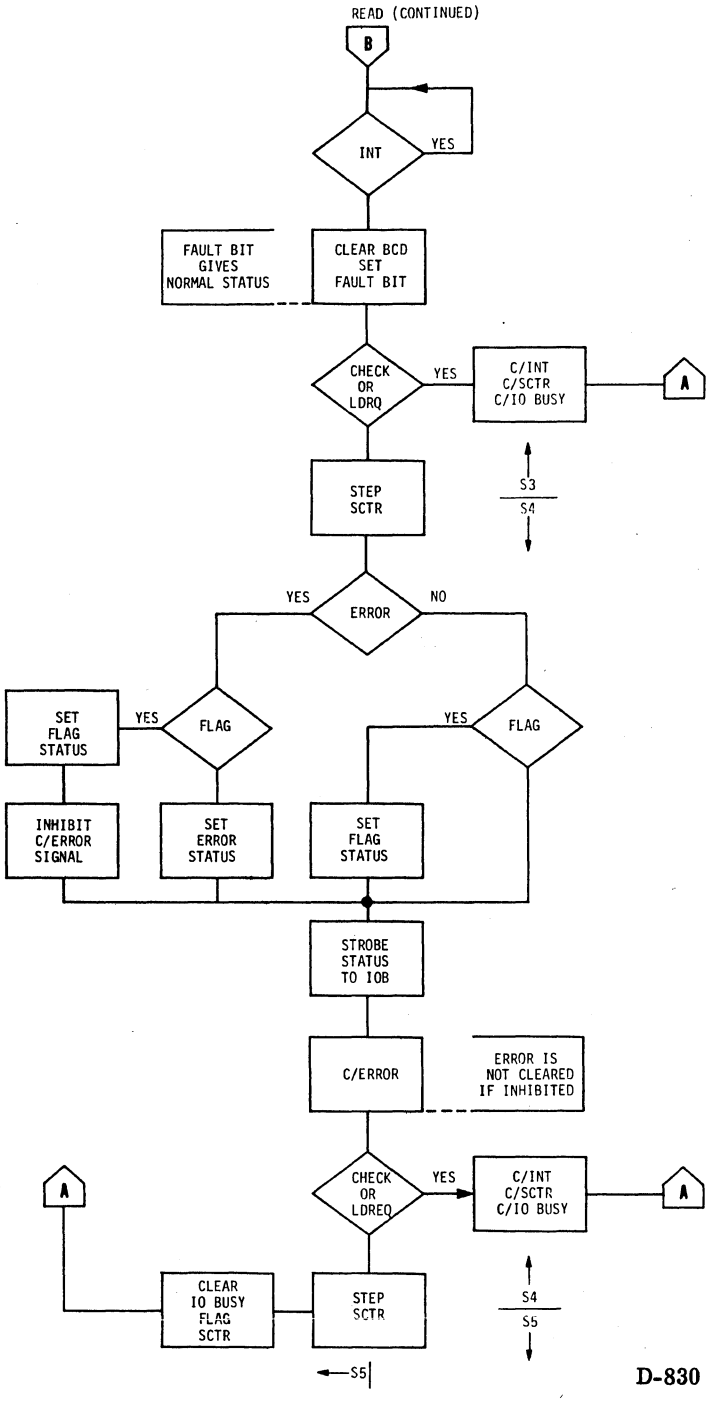
BLOCK DIAGRAM

FIGURE 15-4



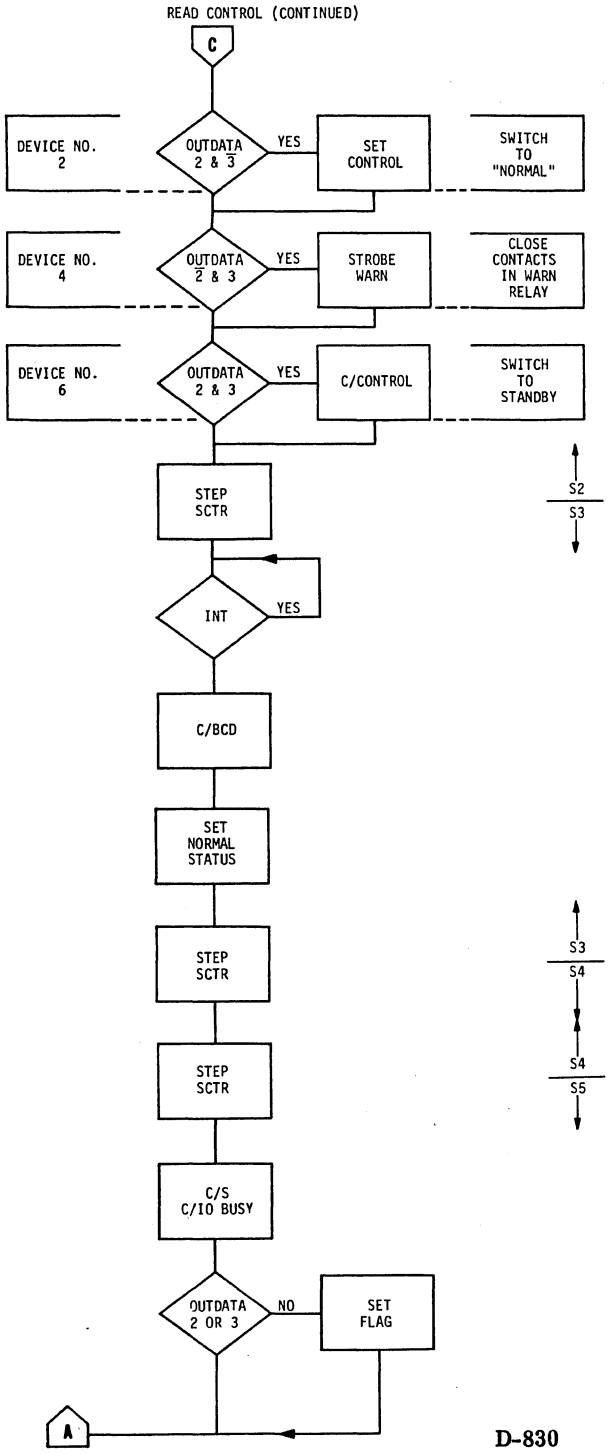
DIGITAL CLOCK LOGIC FLOW

FIGURE 15-5



DIGITAL CLOCK LOGIC FLOW (Cont.)

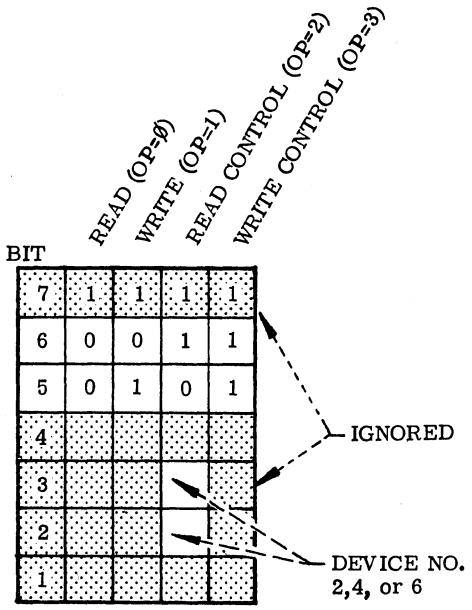
FIGURE 15-5



DIGITAL CLOCK LOGIC FLOW (Cont.)

FIGURE 15-5

In S2 the Digital Clock receives an op code instruction in the form of a select character from the ACU. The LOAD-IOS signal from the processor strobes the character into the op code register. The op code register, in this case, is two D flip-flops, OP1 and OP2. These two flip-flops monitor the 5 and 6 bit lines respectively of the OUT-DATA bus. Only the 5 and 6 bits have significance to the Digital Clock, except for the second and third bits (binary 2 and 4) of the device number (LA). The select character is shown below, indicating the bit combinations that cause Digital Clock actions.



DEVICE NO.	ACTION
0,1, 8 or 9	SET FLAG
2 or 3	RESET CONTROL (SWITCH)
4 or 5	SET WARN
6 or 7	SET CONTROL

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WRITE or WRITE CONTROL instructions are illegal to the Digital Clock, and cause CHECK to set, clearing IOB, the State Counter, and IO BUSY.

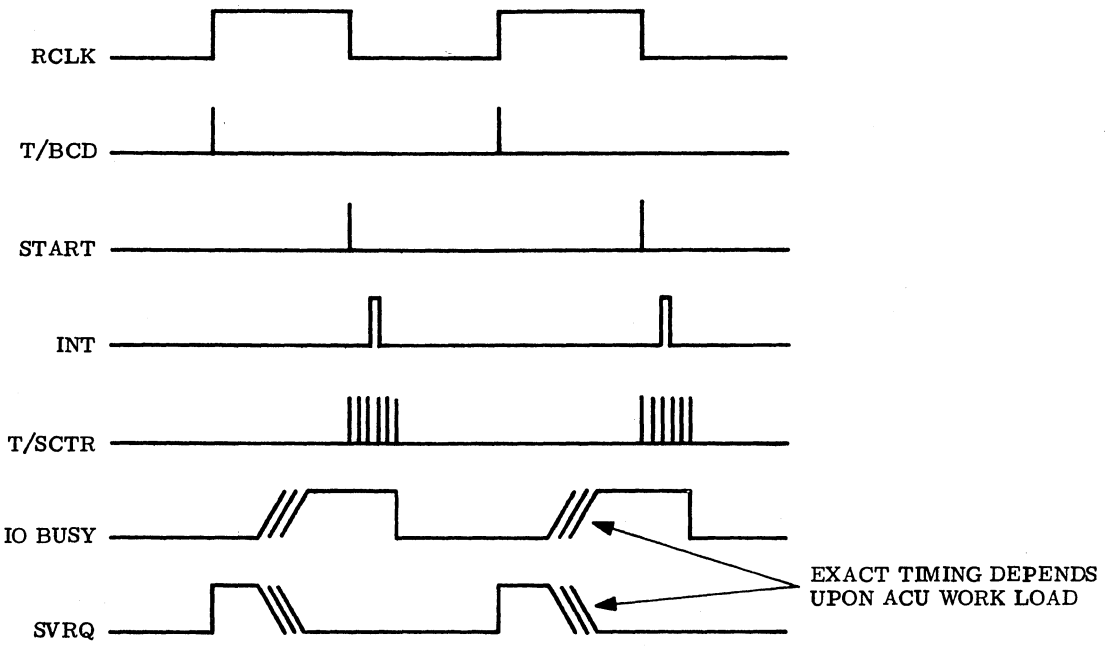
A READ CONTROL instruction with a device number zero will follow an operation that has set CHECK or LOAD REQUEST. A READ CONTROL with a device number 2 through 7 originates within the software, and causes the action listed in the illustration above. A READ CONTROL with a device number other than 2 through 7 sets FLAG. When a READ CONTROL instruction is received by the Digital Clock, LA (the device number) is examined and implemented. Status is placed into IOB, and the state counter and IO BUSY are cleared. No data is transferred by a READ CONTROL instruction.

Normal response to a service request is a READ instruction. When the READ instruction is received, the number that is in the BCD counter is placed into IOB, and INTerrupt is set. The processor takes the BCD number from IOB, and resets INT, clearing the BCD counter and setting the FAULT bit for normal status. In S4, status is loaded into IOB, and S5, the State Counter, FLAG, and IO BUSY are cleared. Clearing IO BUSY causes the ACU to take the status that was loaded into IOB, and the operation is complete, until the next RCLK pulse.

If the Digital Clock has an External Clock Interface connection, it will receive update numbers from the external clock. These numbers, and the update times, vary with the type of external clock, and the software must be programmed for the proper inputs. Each update time (every hour, 12 hours, etc) the external clock interface places a BCD number on the INP-DATA lines to the processor. When the next service request is answered, the BCD number is taken by the ACU to be used by the software. If the BCD correction number comes while the Digital Clock is waiting for service, the seconds counter will be cleared, but service request will not. As with regular operation, the seconds count, if any, will be added to the BCD correction by software. If the Digital Clock is executing a READ instruction when the update number arrives, the correction will be placed on the INP-DATA lines, but the seconds count will not be cleared.

If CHECK or LOAD REQUEST is set by the processor during a READ operation, the operation is terminated by resetting IO BUSY, and the Digital Clock is re-initialized.

a. CYCLE DROP. As protection against missing power cycles, the Digital Clock tests each cycle from the line. A retriggerable monostable multivibrator (one-shot) is triggered at the beginning of the cycle. The timeout for the one-shot is slightly longer than one cycle. If the one-shot times out, a cycle has been missed, and ERROR is preset.



APPROXIMATE TIMING FOR NORMAL CIRCUMSTANCES D-831

FIGURE 15-6

Figure 15-6 shows the timing relationship of some of the major elements within the Digital Clock. The exact timing for setting IO BUSY and resetting SERV-REQ depends upon the availability at that particular time to the ACU. The timing as shown assumes that a service request is answered in a reasonable time with a normal READ instruction. Abnormal situations are described in the OPERATION description.

The listing below shows an expanded view of the events during each state time. However the aCU actions that are listed are dependant upon the work load of the processor, and its ability to respond at the proper times.

SØ
SERV-REQ set; BCD incremented; ACU sets IO BUSY, resets SERV-REQ, and sends SELECT CHARACTER; START is set, causing SCTR to step to S1.

S1
START is reset; IO BUSY is checked (if not set, SCTR is cleared).

S2
BCD contents strobed into IOB; INTerrupt is set.

S3
ACU takes character and resets INT; BCD cleared.

S4
Status strobed into IOB.

S5
IO BUSY reset, SCTR cleared; FLAG reset (if it is set).

C. MANUAL OPERATION

1. Line Frequency

The Digital Clock is wire jumpered at the time of installation to accept either 50 or 60 Hz. Connections for the line frequency determination are given in the early part of this section.

2. Partition Size

Digital Clock partition size is determined by jumpers on the test point block at the front edge of the printed circuit card. Figure 15-7 shows the jumpers which are used to obtain the various partition sizes.

3. IO Reset

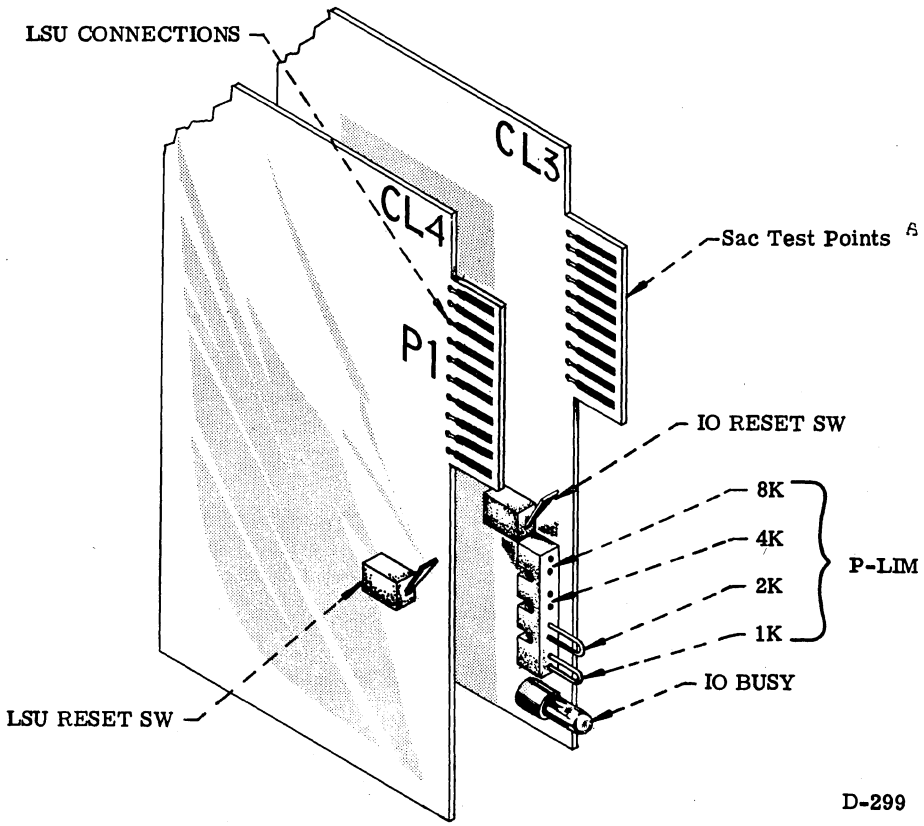
The Digital Clock can be manually reset by momentarily depressing the IO RESET switch at the front edge of the printed circuit card.

4. IO BUSY Indicator

There is an indicator light at the front face of the Digital Clock printed circuit card that lights when the IO BUSY flip-flip is set.

5. Manual Switch Control (CL4)

Causes LSU to Switch when in the down position.



DIGITAL CLOCK

FIGURE 15-7

D. GLOSSARY

BCD	Counter for storing the 1 second increments from RCLK. Stores up to 9 counts before FAULT is set.
CHECK	Status flip-flop; set when the IOC detects a WRITE or WRITE CONTROL select character.
C/S	Clear the state counter.
CYCLE-DROP	Detection of a missing cycle in the power line.
DEC-S	State Decoder; decodes 6 mutually exclusive states.
ERROR	Set when a cycle drop is detected.
FAULT	Set when BCD Counter is cleared to produce the 3 bit needed to indicate normal status. Recovery from a power failure will indicate FAULT status.
FLAG	Status flip-flop set by one of three conditions: 1. BCD reaches a count of 9. 2. Following the execution of a READ CONTROL instruction. 3. When INTERRUPT is set during RCLK pulse, indicating the BCD character is inaccurate.
INTERRUPT	Set when the second-count character is ready to be transferred to the ACU.
IO BUSY	Set when the channel is active.
IOB1 through IOB4	Buffer register, IOB, contains seconds count, or status for ACU. IOB numbers correspond to the lower four bits of the INP-DATA bus.
IOC-LF-CLK	45kHz signal from the ACU; drives synchronism for State Counter.
IO-RESET	Switch and RS latch for manual reset of IO.
LCLK	Line frequency signal from power supply (50 or 60 Hz).
LOAD REQ	Indicates that reloading of the program is required.
MOD IO CTR	Divides the output of the Mod 5 or Mod 6 ctr by 10.
OP1 and OP2	OP register; stores binary representation of op instructions from ACU.
PCR	Synchronizes the State Counter with the IOC-LF-CLK.
READ	READ signal, decoded from OP1 and OP2.
RCLK	One second pulse for basic timing.

RDC	READ CONTROL signal decoded from OP1 and OP2.
SØ, through S5	Decoded states from DEC-S.
SCTR	State Counter.
SERV REQ	Set by rising edge of RCLK; calls up ACU for time character.
SF1, SF2, SF3	Parts of Mod 5 or Mod 6 counter.
START	JK master slave to initiate the State Counter in SØ. It is triggered by the falling edge of RCLK, and cleared in S1.
T/INT	Toggle Interrupt.
T/S	Toggle the State Counter.
WTC	WRITE CONTROL signal decoded from OP1 and OP2.

E. LINE SWITCHING UNIT

1. GENERAL

The Line Switching Unit is a free standing device for shifting moduler data transaction systems (MDTS), or manufacturing information systems (MIS) terminals from one processor to another processor that acts as a "standby" unit. The Line Switching Unit (LSU) has a self contained power supply, and requires 115vac or 220vac power to operate.

The LSU is internally divided into two modules, each capable of switching 90 terminals. The module division is electrical, not mechanical. Generally, one module resides in the upper card cage, and one module in the lower card cage. But in a maximum terminal configuration one card from the upper module resides in the lower card cage (see figure 15-8). Both modules may be controlled from one source, and switch simultaneously, or they may be controlled by separate and independant sources. The control signals for switching originate in the Digital Clock unit of the "normal" processor.

Either or both of the two modules within the LSU can switch less than the maximum number of terminals. However, all units within one module are switched at the same time (with the exception of manual switches that control individual boards). A module can contain from zero to nine individual switching boards (ISB), each capable of switching ten terminals. The switching load of one module or board need not be balanced with the other. Figure 15-9 shows two of the possible switching configurations. In the dual configuration each processor is the "standby" unit for the other. The single standby configuration has a portion (or all) of the processor that is in reserve. In either configuration, the IOC that is in reserve is not used until switching takes place. The illustration shows the entire module switching into one IOC. In practice, one IOC accommodates the output of one ISB.

2. ISB

The Individual Switching Board (ISB) is a printed circuit card containing five mechanical relays, and a toggle switch. The toggle switch, when in the "down" position, switches all five relays on that board to the "standby" position.

Each relay contains four sets of SPDT form C contacts. Both the SIG-HIGH and SIG-COM lines from the terminal are switched, consequently one relay will switch two terminals. The armature contact (C) of the contact set is connected to the data terminal line. The normally open (NO) and normally closed (NC) contacts are connected to the "standby" and "normal" processors, respectively. When the relay coil is activated (by the switching signal) the armature connects to the normally open contact, switching the terminal to the standby processor.

3. CONTROL AND ALARM SIGNALS

Terminal boards 19 and 20 at the rear of the LSU (see figure 15-10) contain the control signals to, and from the Digital Clock, and extensions of a set of contacts from the power-fail relay within the LSU.

The power-fail contacts are available for use by the customer to activate an alarm or other indicator if the LSU power fails. When the power to the LSU fails, the relay coil de-energizes, and the contacts close. The maximum rating of these contacts is 15 volts at 1 ampere.

The Digital Clock SWITCHing relay (located within the Digital Clock) has two sets of contacts that are extended to the LSU through the switching control cable. One set of contacts operates the relay coils on the individual switching boards, and also operates an audible alarm at the rear of the LSU. The second set of relay contacts (SPDT) are available for customer use, providing the maximum rating of 15 volts at 1 ampere is not exceded.

The Digital Clock also contains a software-controlled relay that is extended to the LSU through the switching control cable. The action of this (WARNing) relay is independant of switching action, and is strictly software controlled. The WARNing relay contacts are for customer use, and are rated at 15 volts at 1 ampere.

Data terminal inputs to the LSU are connected through terminal strip pairs TB1 through TB18. Figure 15-11 shows the cable routing scheme for these connections.

4. MANUAL CONTROLS

The LSU contains two toggle switches, a fuse holder, and an audible alarm. All of these are located on the rear panel, behind the door. In addition, each ISB card contains a manual switch that can cause the relays (all five) on that board to switch.

The audible alarm sounds a tone of approximately 2900 cycles per second, with an intensity of 80 decibles, if the switching signal is present at either module. If the alarm is not desired, it can be disabled, using the alarm "off" position of the adjacent toggle switch.

An auxiliary power switch (directly above the fuse holder) is provided to remove power from the LSU during servicing.

The four lighted switches manually control switching of the two modules. The lighted indicator shows the switched or standby status of that module, and pressing the unlighted indicator switches the module to that status. These switches send control signals to flip-flops in the controlling Digital Clock, and will have no predictable effect upon switching if the Digital Clock is without power, or not functioning properly.

The manual toggle switch at the front of the ISB card enables the energizing coils for the relays on that board. The switching position is "down", causing that one card to switch to the "standby" status.

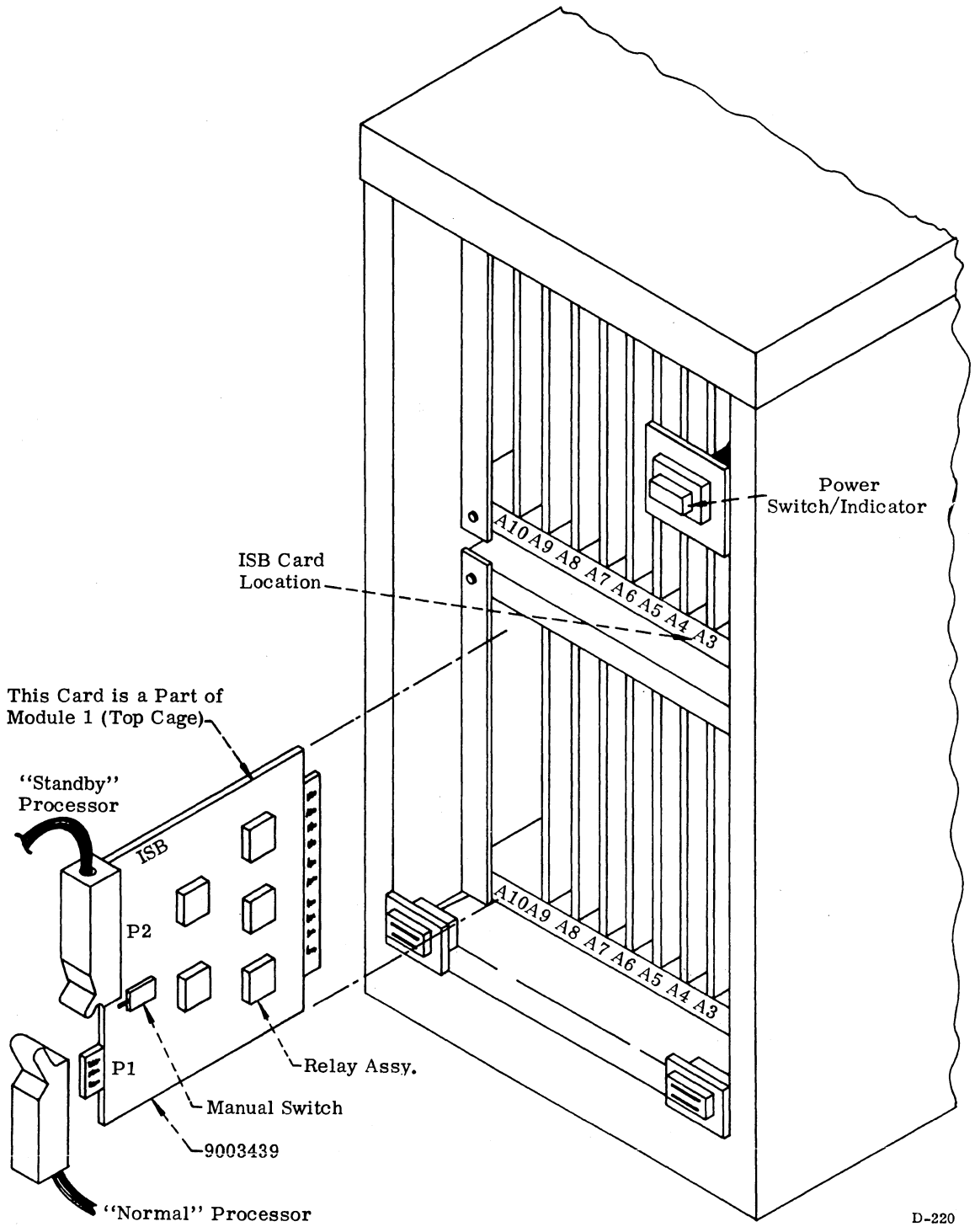
5. REPAIR CONSIDERATIONS (LSU)

If the Line Switching Unit is switched by the Digital Clock because of problems within the "normal" processor, care must be taken in the repair approach. The controlling Digital Clock must not be removed, or the edge connector disturbed, until the ISB cards controlled by it are manually switched.

When the LSU is switched, the entire current of the switching relay coils (up to 90 relays) passes through the edge connector and relaxed contacts of the SWITCH relay in the Digital Clock. This means that if the edge connector of the Digital Clock is removed, (after the LSU has switched) the LSU will switch back to the "normal" processor (the one that is ailing). To prevent this, the technician must determine which module is controlled by the "down" Digital Clock, and manually switch all of the ISB cards within that module, or modules, to the downward position. When this is completed, the controlling Digital Clock can be disconnected.

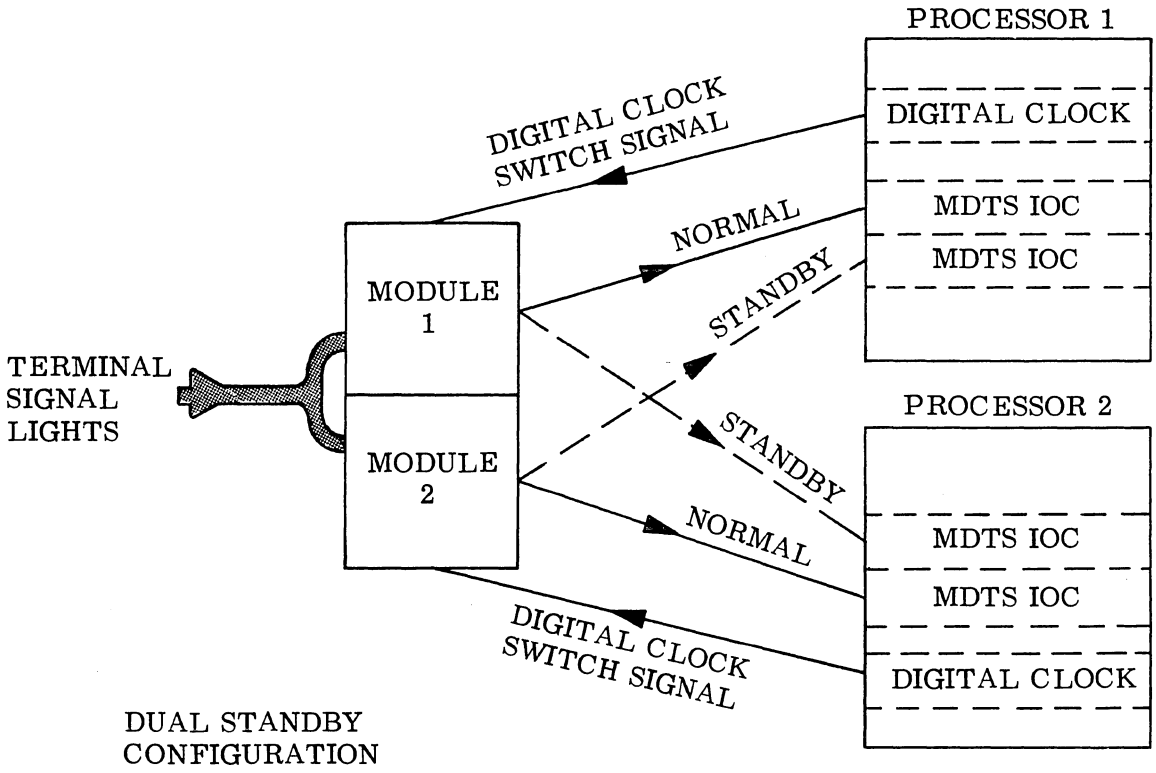
CAUTION

The lighted pushbuttons at the rear of the LSU WILL NOT switch the ISB cards or keep them from switching, if the controlling Digital Clock is disabled, or disconnected. These switches only send controlling signals to a flip-flop within the Digital Clock.

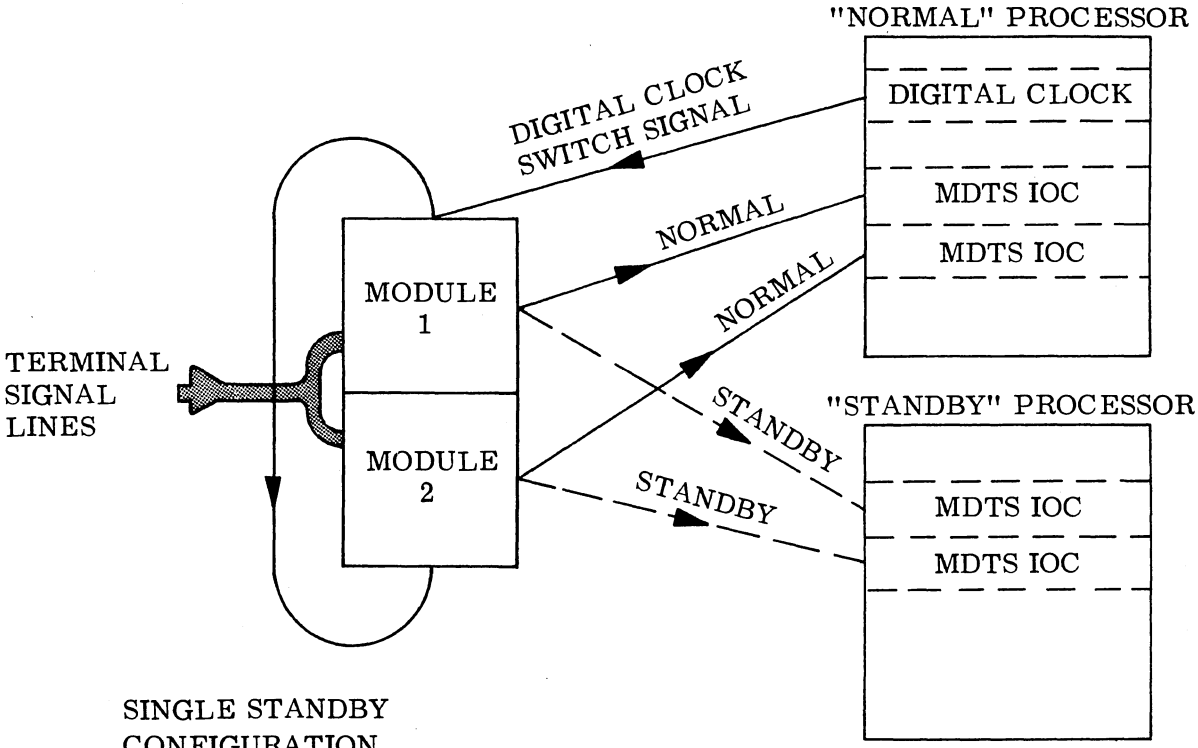


LINE SWITCHING UNIT

FIGURE 15-8



DUAL STANDBY CONFIGURATION



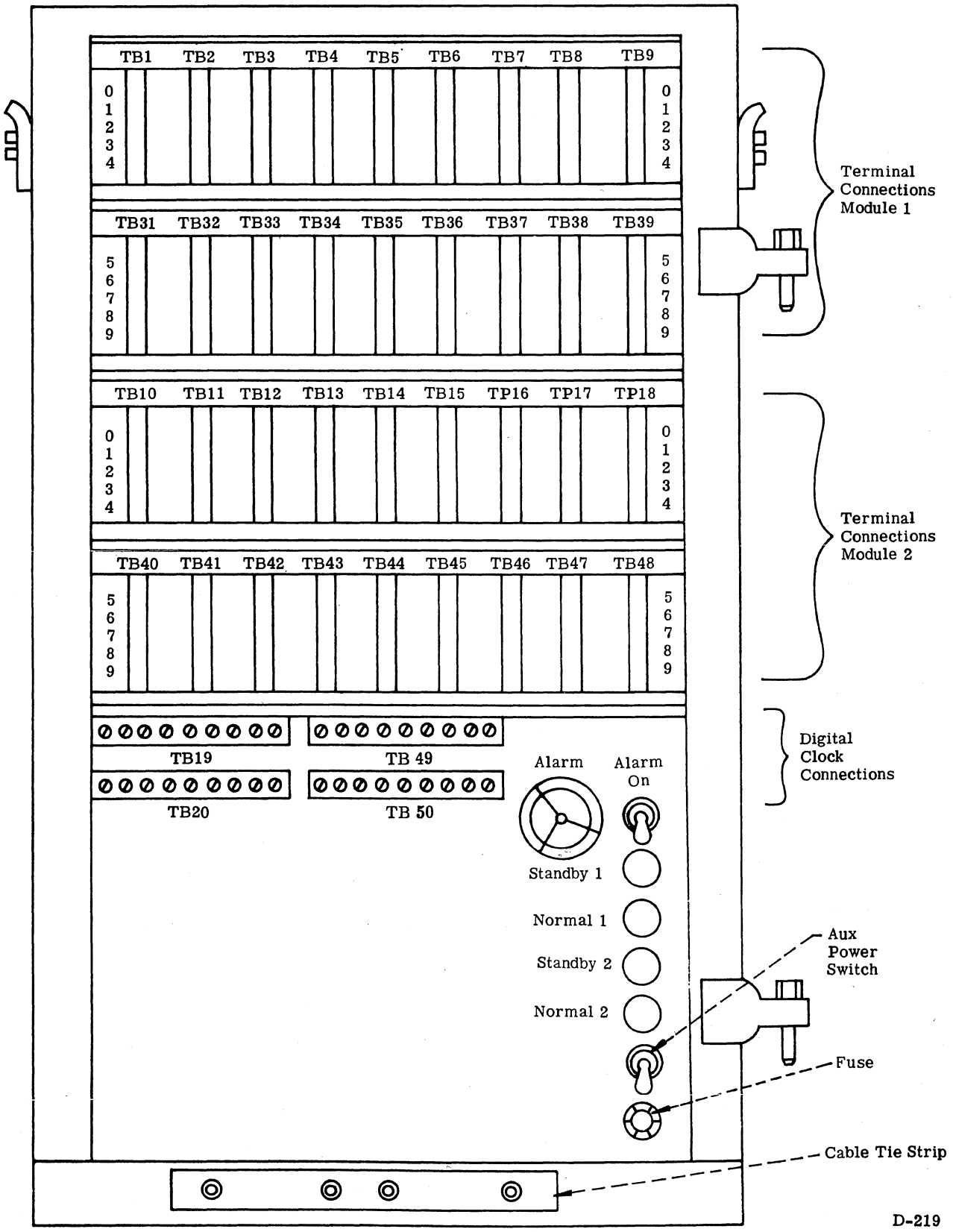
SINGLE STANDBY CONFIGURATION

SWITCHING CONFIGURATIONS

D-204

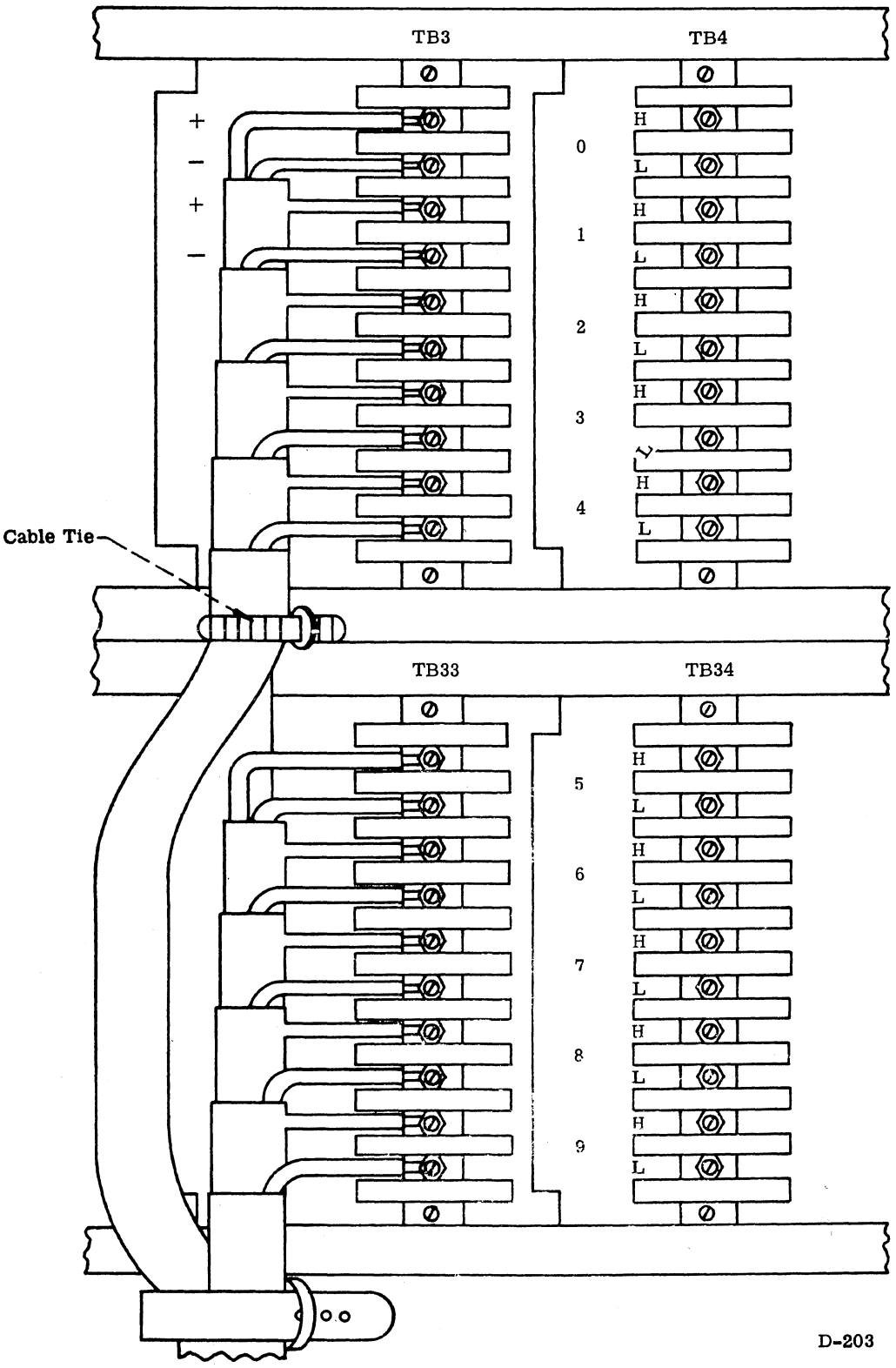
FIGURE 15-9

DIGITAL CLOCK



LSU REAR VIEW

FIGURE 15-10



LSU INPUT TERMINALS

FIGURE 15-11

SECTION 16

CONTENTS

LIST OF ILLUSTRATIONS

ASYNCHRONOUS TERMINAL ADAPTER

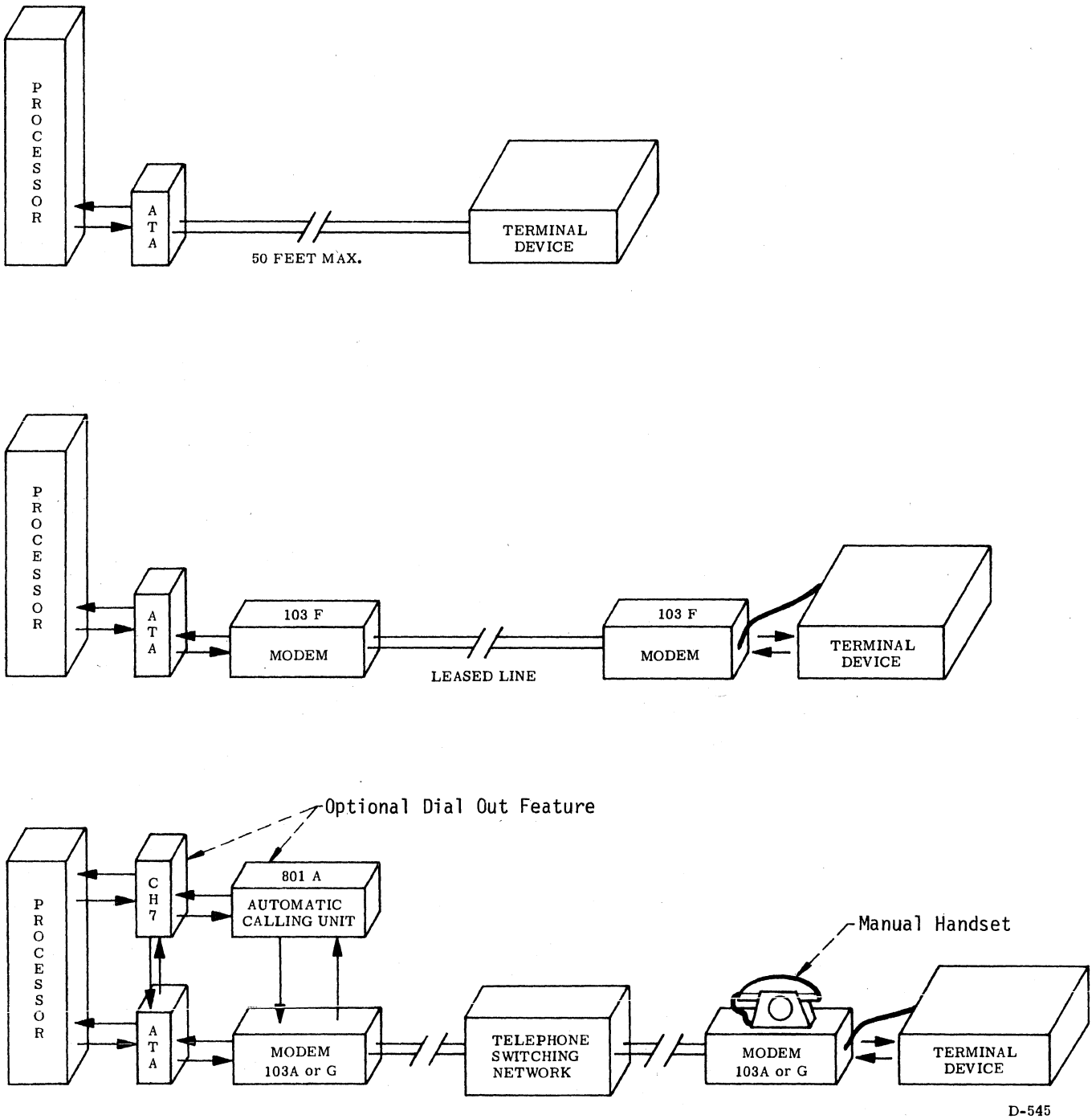


Figure 16-1. ATA CONFIGURATIONS

16-1.0 INTRODUCTION

The Asynchronous Terminal Adapter (ATA) interfaces the model 20 processor to any of a series of communications terminals meeting EIA interface specifications RS-232-B or RS-232-C. A partial list of these terminals includes Model 33, 35, and 37 Teletypewriters, Friden model 7102 communication terminal, and Memorex model 1240 communication terminal.

NOTE: If the model 33 Teletypwriter is used, it must contain the parity option, for even character parity.

Any one of these terminals can be directly connected, or remotely connected through data sets (modems). Using a Bell System 103 data set, or the equivalent, the ATA can connect to the public telephone dial network. Automatic dial-out can be added to an ATA that is connected to the dial network. Figure 16-1 show the basic system variations in which the ATA can be used.

The ATA uses standard 7-bit ASCII characters, transmitted asynchronously, with a nominal bit rate of 110, 150, 200, or 300 bits per second. Each character contains 10 bits (except at the 110 bps rate). The character begins with one start bit, followed by the 7 ASCII character bits, and one stop bit. At the 110 bps rate, an additional stop bit is included for compatability with terminals operating at that speed. The ATA bit rate is manually selectable, and should be considered a semi-permanent, or installation type adjustment.

16-2.0 INSTALLATION

The basic ATA resides in any of the two-card I/O positions in the model 20 processor. If the automatic dial-out option is used (CH7, part no. 9005440), an additional I/O position must be provided on one side or the other of the ATA. This means that if the dial-out feature is used, the ATA cannot occupy partition zero. The ATA partition number is governed by the position of the TA1 card, and is not affected by the presence, or absence of, the CH7 card. In a fully loaded system, the ATA can be placed in partition 19 (positions H and J in expansion module 5), and the CH7 card can be placed in position K. Position K is not addressable by the ACU, but can be used by the CH7 card, as it is connected to the ATA through front-edge connections.

Figure 16-2 shows the ATA, and the necessary interconnecting cables. The configuration that is shown includes the automatic dial-out option. If the dial option is not used, the edge connector on TA2 is not used. Connection is made from the edge connector on TA1 to a Bell 103 modem, or equivalent, or directly to a terminal if it is located within 50 cable feet.

NOTE: When installing or replacing either of the two basic ATA cards (TA1 or TA2), be sure to check all manual settings: P-LIM, PRIV-CHAN, bit rate, timeout interval, and control character input.

16-2.1 MANUAL SETTINGS

Six manual settings are available to service personel, allowing the logic configuration to be varied with individual installations. Jumpers for partition size (P-LIM), and prilileged area patching (PRIV-CHAN) are shown in figure 16-2. The remaining settings are summarized in table 1, and described below.

ASYNCHRONOUS TERMINAL ADAPTER

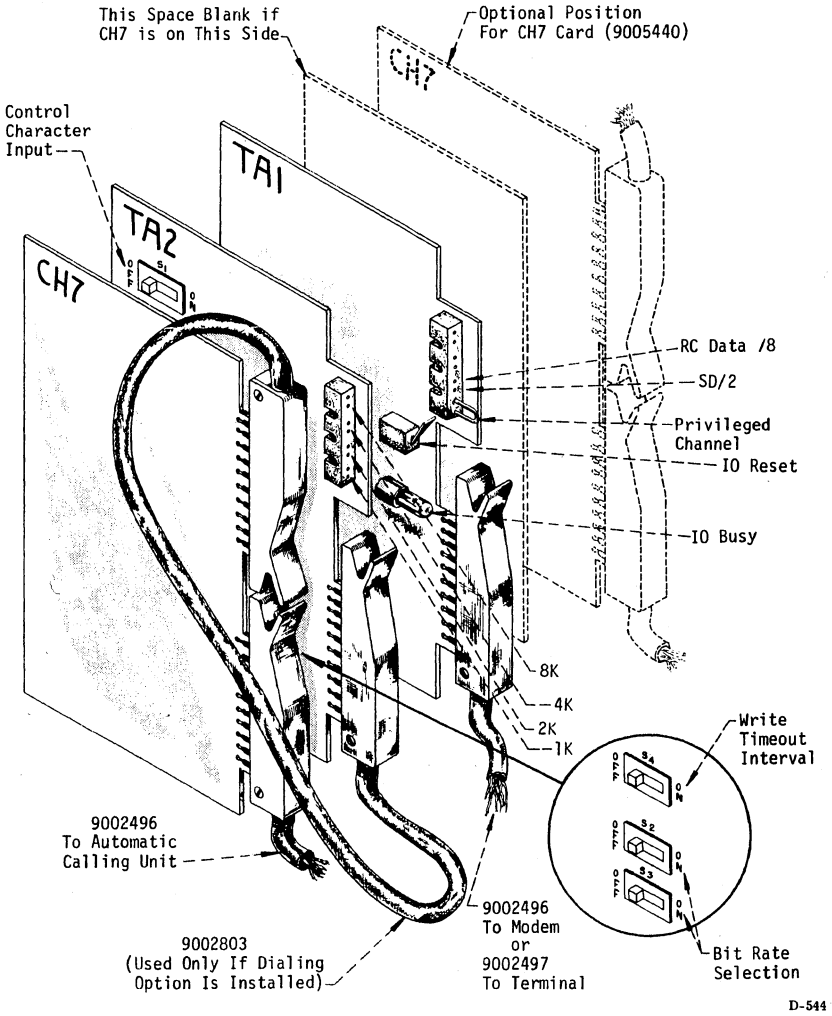


Figure 16-2. MANUAL SETTINGS

Table 16-1. ATA Manual Settings

CONTROL CHARACTER INPUT	S1 (TA2)	off		Control characters (columns 0 and 1 of the ASCII chart) are not transfered to memory during READ operations.
		on		Control characters during READ will not perform internal functions, but will be entered into memory.
BIT RATE	S2,S3 (TA2)	S2	S3	Bit Rate
		off	off	110 bps
		off	on	150 bps
		on	on	200 bps
		on	off	300 bps
WRITE TIMEOUT INTERVAL	S4 (TA2)	off		WRITE timeout interval - 1.8 sec. minimum
		on		WRITE timeout interval - 1.0 sec. minimum
MANUAL RESET (momentary)	S5 (TA1)	off		Normal operation
		on		ATA is initialized to IDLE state.

- P-LIM jumpers adjust the memory allotment for the ATA partition. Partition limits are a system consideration, and should be adjusted accordingly.

- PRIV-CHAN is installed to allow access to the Privileged area of memory.

- CONTROL CHARACTER INPUT in the ON position, allows incoming control characters (such as US, EM, ESC, SUB, and CAN) to be stored in memory as the character equivalents in columns 4 and 5 of the ASCII chart; no other action is taken. In the OFF position the codes are decoded, and the appropriate action is taken. This allows mechanical actions, such as form feed, line feed, etc. to occur without the codes entering memory. Horizontal Tab, and Carriage Return do not perform internal ATA functions.

- BIT RATE determines the speed of operation in bits per second.

- WRITE TIMEOUT INTERVAL allows time to complete mechanical actions, and only applies to WRITE CONTROL characters.

- RESET is the manual I/O reset that allows a reset of the ATA without resetting the entire processor.

ASYNCHRONOUS TERMINAL ADAPTER

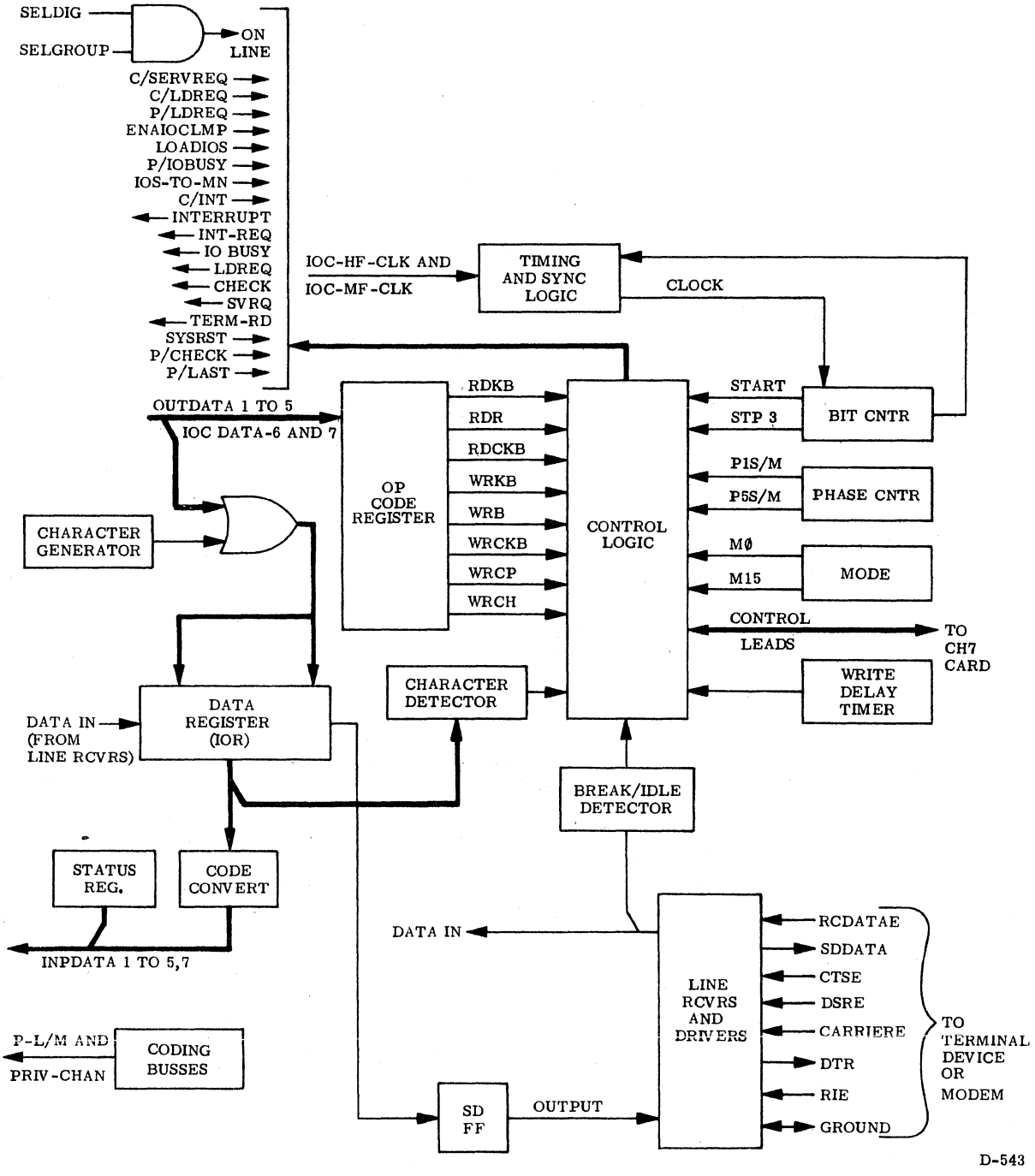


Figure 16-3. ATA SIMPLIFIED BLOCK DIAGRAM

16-3.0 OPERATION

The ATA is limited to communication with only one terminal at a time, but a terminal such as a 7102 may have other devices as an integral part of the machine. Provision is made to control a paper tape reader, and a paper tape punch as part of the terminal. When under control of the processor, the ATA assumes that some of the manual control on the terminal could have been toggled to unknown states. Therefore, when an operation commences, control characters are hardware generated to activate, or de-activate, the proper device for the instruction. At the close of an operation, the terminal is returned to an idle state, by turning off the punch, etc. However, when data is read from a paper tape, the ATA does not send a reader-off code. Conditions require that the reader-off code (DC3) must be read from the tape, or the reader must be stopped manually. Figure 16-3 shows a simplified block diagram of the control logic that performs the functions other than data transfer.

ATA logic operation allows the terminal operator to temporarily "break" from computer data exchange, to a stand alone "local" condition. In this local condition the terminal can be used within any of its capabilities without affecting the processor or software program. For example, the 7102 terminal can be used in the local condition, to punch a paper tape record of data or software program that will be used at a later time, or by another system. The operator is in full control of the local/online status of the terminal, and can change from one condition to the other at any time, by depressing the BREAK key for a short time. At each transition from local to online, or fron online to local, an operator cue is printed to verify the condition. A parenthesis, (, indicates the terminal is in the local condition, and a closing parenthesis,), indicates the terminal is online. In this case, online means that the terminal is directly relating to the processor, through the ATA.

16-3.1 OPERATOR ENTRY

When the software program requires an entry from the terminal, or if the program needs re-loading (because CKECK was set), an operator cue is transmitted and printed to inform the terminal operator of the need. There are two cues for operator entry: E, for enter (a READ instruction), and L, for load (a READ CONTROL instruction).

16-3.2 LOCAL/ONLINE

To change the terminal status from online to local, or back to online, the operator must depress the BREAK key for a short time. The ATA toggles between local and online whenever a "break" is detected. A break is an interruption of the transmission that is caused by depressing the BREAK key, for a time greater than one character length. The actual time is approximately 200 milliseconds, quite short, in relation to human speed.

The operator is made aware of the change into or out of local when open or closed parenthesis are automatically typed by the printer. Service request, and load request are made while the terminal is in the local condition, and are explained below.

16-3.3 SERVICE REQUEST

In most software programs, the operator has the option of branching to a new instruction in the program, or back to the beginning of the program, by setting a service request condition. Service request is set in the ATA, by first placing

16-3.3 SERVICE REQUEST (Continued)

the terminal in local, then entering a SUB code as the first character in the local condition. The terminal can be immediately returned to the online condition (at the operator's option), or local operations may be performed before going back online. However, the first operation after recovering from local, will be the service request that was set while in local. The operator can not cancel, or reset, the service request, once it is set.

16-3.4 LOAD REQUEST

Operator initiated load request is similar to the service request procedure. The terminal is placed into the local condition, and an ESC code is entered as the first character in local. The terminal can be returned to the online condition immediately, or after local operations are performed. However, as with service request, the first operation that is performed after recovery from local, is the load request that was set while in local. The printer will type an L, indicating to the operator that a ten character instruction word is needed from the terminal. The ten characters may be entered from the keyboard, or the operator can manually activate the paper tape reader that will read the characters.

If a unit seperator (US) or end of media (EM) code is given to the ATA as the first character after the L is printed for load request, ten zeros will be loaded into location ØØØØ in the ATA partition.

LOAD REQUEST may be automatically set by the processor if a program error is found. The L is printed in the same manner as an operator initiated load request. And ten characters must be loaded in the same manner as for the operator initiated load request.

16-4.0 LOGIC SEQUENCES

16-4.1 TIMING

To accomplish a specific objective, the ATA enters a basic mode of operation. For example, the entire operation of sending a printer-on command to the terminal is contained in mode 3. The mode is subdivided into bit times and phases, with the phases containing the individual timing signals.

During a WRITE operation, a delay is provided (WRDLYTO) at certain times to allow completion of mechanical actions within the terminal. Mechanical movements, such as carriage return, temporily suspend the normal timing within the ATA. The exact delay is selectable between 1.0 and 1.8 seconds by S4 on the TA2 card (see MANUAL SETTINGS).

16-4.2 MODES

The ATA generates 16 modes (basic logic conditions) that are subdivided by other phases and timing signals. Three of the modes (M5, M11, and M15) are not used, and can be disregarded in this discussion. Each mode performs a specific operation in the series of events that are needed to complete an instruction. Table 16-2 shows a brief reference list of the mode operations, and the modes to which the ATA can move next.

Table 16-2. MODE USES

MODE	USE	EXIT TO
MØ	Idle, or dialing	M3 or M6
M1	Send punch-off code (DC4)	MØ
M2	Send printer-off code (SO)	MØ
M3	Send printer-on code (SI)	M4, M8, or M12
M4	Transmit data, or control characters	M1, or M2
M5	Not used	-
M6	Send punch-on code (DC2) or reader-on (DC1)	M4, or M7
M7	Receive data	M2
M8	Send L or E to terminal	M7
M9	Send) to terminal	M10
M10	Send printer-off code (SO)	MØ
M11	Not used	-
M12	Send (to terminal	M13
M13	Receive first character of local mode	M14
M14	Reside in local until "break" is detected	M9
M15	Not used	-

The descriptions that follow are a more detailed accounting of the general actions within each mode.

- MODE Ø, with one exception, is an idle state. The ATA waits for an instruction from the processor. Data is neither sent, or received in MØ. If a dialing operation is initiated, the ATA remains in MØ while the CH7 card completes the dialing sequence. Characters are transferred during dialing (the dialing digits), but go directly to the CH7 card, and the remainder of the ATA is unaffected.

16-4.2 MODES (Continued)

When the I/O select character is received in MØ, the ATA moves to either M3, or M6, depending upon the instruction in the processor. A WRITE instruction that is directed to the punch, or a READ instruction that is directed to the paper tape reader, causes a jump to M6. All other operations (except dial, or hang up) cause the ATA to enter M3.

- MODE 1 is entered after transmitting data or control codes to the terminal (in M14). In M1, a punch-off code (DC4) is sent to the paper tape punch. To accomplish this, the character is shifted (parallel) from the processor OUT-DATA lines into IOR. The start bit is injected into the SD flip-flop, and the character is shifted serially from IOR to the SD flip-flop. The parity bit is added (from the VRC flip-flop), and one or two stop bits are added (according to the selected bit rate). The ATA then moves to MØ

- MODE 2 is entered after transmitting or receiving data to or from a terminal. The printer-off code (SO) is sent to the keyboard printer, and the ATA moves to MØ. The printer-off code sent in M2 should not be confused with the printer-off code generated in another mode when returning from local.

- MODE 3 is entered directly from the idle state (MØ), and sends a printer-on code (SI) to the keyboard printer. After the printer is turned on, the ATA can enter M4, to transmit data, M8 to send an enter or load cue to the terminal, or M12 to send the local cue, if the terminal is going into local.

- MODE 4 is entered from M3, where the printer was turned on, or from M6, where the punch was turned on. M4 is used to transmit (write) data to the terminal. A brief description of character transmission is given in the paragraph describing M1. After data is transmitted (and LAST is set), the ATA enters M2 if the data was printed, or M1 if the data was punched.

- MODE 5 is not used.

- MODE 6 is entered directly from MØ when the ATA is to read or punch paper tape. If the instruction is to READ, the reader-on code (DC1) is transmitted to the terminal, and the ATA exits to M7. If the instruction is to punch (a WRITE instruction), the punch-on code (DC2) is sent, and the ATA exits to M4.

- MODE 7 is used to receive data from the terminal. The ATA monitors the receive data line (from the modem or from the terminal). Bits are shifted into IOR, and when the character is completely assembled, it is passed in parallel to the processor. When the data transfer is complete, the ATA enters M2, where the printer is turned off.

- MODE 8 is used to transmit a prompting cue to the terminal operator. An E is generated and printed if the instruction is a READ, or an L is generated and printed if the instruction is a READ CONTROL. Once the prompting cue is transmitted, the ATA enters M7, where data from the keyboard is received.

16-4.2 MODES (Continued)

- MODE 9 is used to generate and print the online cue,), that is sent to the terminal upon leaving the local condition. M9 is entered after a "break" is found while residing in M14. When the online cue has been transmitted, the ATA enters M10, where the printer is turned off.

- MODE 10 is entered from M9, and is used to transmit the printer-off code (SO) to the terminal. The printer-off code is also transmitted in another mode, but M10 is used exclusively when returning from local. After the printer is turned off, and the IO BUZY flip-flop is in the reset state, the ATA enters MØ.

- MODE 11 is not used.

- MODE 12 is entered from M3, and is used to transmit the local, or off line code, (, to the terminal. This indicates to the terminal operator that the keyboard printer is under local operation. After the off line cue is transmitted, the ATA enters M13, where a check for load request and service request is made.

- MODE 13 is the initial portion of the local condition. The ATA waits in M13 for the first character from the terminal. If the first character in local is a SUB code, the SVRQ flip-flop is set; if the first character in local is an ESC code, LDREQ is set. If the first character from the terminal after entering local is not ESC or SUB, no flip-flops are set. In any case, after receiving the first character in local, the ATA enters M14, the residing local mode. The ATA will also enter M14 from M14, if the BREAK key is depressed for 200 ms or longer.

- MODE 14 is the residing local, or off line, mode. M14 is entered after the first local character is received, and evaluated. The ATA remains in M14 until a "break" is detected from the terminal. When a break is detected, the ATA enters M9, where the online cue is transmitted.

- MODE 15 is not used.

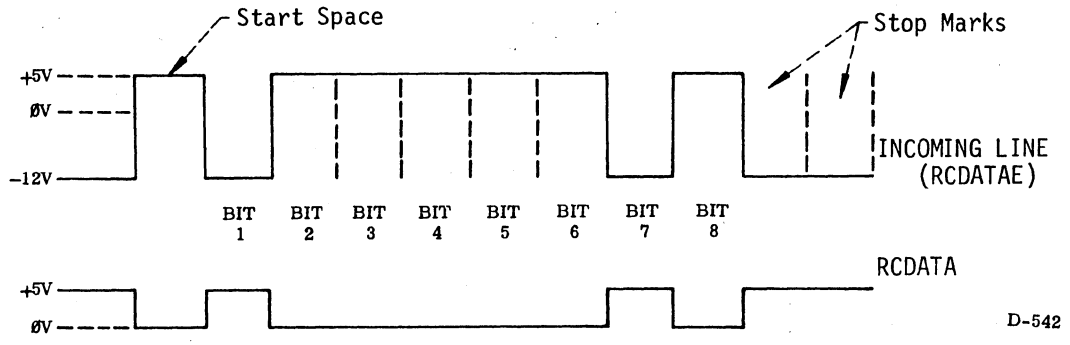
16-4.3 PHASES

Phases are subdivisions of transmit or receive bit times. Each bit time, including the start and stop bits, contains five timing pulses near the beginning, and after a pause, another series of five pulses around the midpoint of the bit time. These pulses are named P1S through P5S for the beginning pulses, and P1M through P5M for the midpoint pulses. In many cases, the phase signals are combined with bit signals for spcific timing purposes. These combined signals have names such as DATA8P1M, meaning, the first phase pulse of the mid-bit group in data bit 8.

16-5.0 TTY TRANSMISSION

The ATA transmission scheme is "teletype" compatable. A "mark" condition is where a 1 bit is being transmitted on the line, and a "space" condition is a zero bit. The voltage levels on the transmission line can vary widely, but are normalized by entry logic of the ATA. A mark condition on the transmission line is - 5v to - 25v, and a space is + 5v to + 25v. The voltage level between + 3v and - 3v is an indeterminate area, and is not used.

The mark/space signals are inverted as they enter the ATA. One-bits (marks) become high signals (+ 5v), and zero-bits (spaces) become low signals (Øv). The figure below shows a letter A as it might appear on the transmission line from a terminal (in this example, the terminal is a 7102). The lower trace shows the converted voltage levels that are used by the ATA.



16-5.1 INTERFACE CONTROL LINES

Control signals are OFF when the control line is in the negative voltage condition, and ON when the line is positive. Two variations to this rule are the "fail-safe" lines that are at a positive voltage when ON, but are considered OFF when the voltage is at zero, because the unit loses power, or the cable is disconnected. These two lines are the Data Set Ready (DSR) and Data Terminal Ready (DTR) lines.

TTY terminals are equiped with a BREAK key, that in this case, is used to transfer the terminal into, or out of a local status. The operation of the online/local transfer circuit is explained in the paragraph below.

16-5.2 BREAK DETECTOR

The ATA places the terminal into or out of local each time a "break" is detected on the transmission line. A break is defined as: a space longer than one character, at the slowest bit transmission rate, followed by an idle period (mark) of at least the same length. A space condition is created by an interruption of the line; the line remains in a mark condition when idle.

If the terminal is connected through modems, a loss of carrier prevents break detection, regardless of changes on the transmission line.

The break detection circuitry is located on the TA1 card, and consists of four D flip-flops, and one re-triggerable monostable multivibrator (one-shot). These are DATASN, DATADL, BREAK, LOCAL, and TIMR.

16-5.2 BREAK DETECTOR (Continued)

HOW IT WORKS

DATASN and DATADL are copies of RCDATA that are synchronized with ACUCLK. DATADL is delayed from DATASN by one half cycle of ACUCLK. The LOCAL and BREAK flip-flops are reset by initialization (INIT), and DATASN and DATADL assume the state of RCDATA within one cycle of ACUCLK (ACUCLK is either 300, or 450kHz). A change in RCDATA causes DATASN and DATADL to acquire opposite states for a short time following the change. When this occurs, one or the other of the two gates that monitor DATASN and DATADL, will develop a trigger signal for TIMR. Figure 16-4 shows the break circuitry, slightly simplified for clarity. Gate A (in the illustration) detects logic level transitions from zero to one, and gate B detects transitions from one

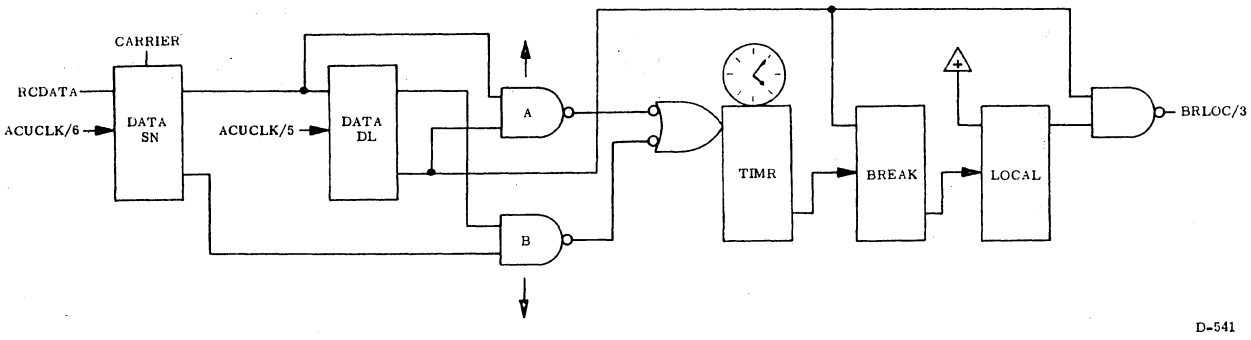


Figure 16-4. BREAK DETECTOR

to zero, triggering TIMR each time a transition occurs. When RCDATA does not change for a period greater than 200ms (approximately), TIMR expires, triggering the BREAK flip-flop. RCDATA remains high when the line is idle. Thus, when BREAK is triggered, it does not set, because the D input is low.

When the terminal operator depresses the BREAK key, requesting a break to, or from local, the RCDATA lead becomes low, and stays that way until the key is released. With RCDATA low, DATASN and DATADL will become, and remain reset. TIMR expires after about 200ms, and BREAK is toggled set. Notice, that to this point, the trigger to the LOCAL flip-flop has remained high, but is now low. LOCAL has not triggered because it requires a positive going transition to clock it.

Releasing the BREAK key returns RCDATA to the idle condition (a steady high), and the change in RCDATA re-triggers TIMR. When the idle condition prevails for approximately 200ms, TIMR expires, resetting BREAK. When BREAK resets, it toggles the LOCAL flip-flop to a set condition.

Multiple transitions on the transmission line that may be caused by contact bounce are ignored by the ATA. The "space" interval must be continuous for the 200ms time that it takes TIMR to expire, as TIMR is re-triggered by each transition. Once the space, or break, period is qualified, any mark, or idle, period of 200ms will toggle the LOCAL flip-flop, even if many transitions have occurred between the two periods.

16-5.2 BREAK DETECTOR (Continued)

A break from local requires the same break/idle conditions that are needed to enter local. The LOCAL flip-flop is always toggled set, and is dc reset by other operations within the logic. When the BREAK flip-flop is set by a break qualification on the transmission line, an autowrite sequence starts, trying to return the terminal from local status. But BRLOC/3 is generated by BREAK and LOCAL, inhibiting the sequence. When the BREAK key is released, the BREAK flip-flop is allowed to reset, and the autowrite sequence is allowed to complete. The autowrite sequence sends a printer-on code, prints), and sends a printer-off code. During mode 10, when the ATA sends the printer-off code, the LOCAL flip-flop is cleared, and the terminal is online.

16-6.0 LOGIC OPERATION

The ATA receives all instructions through the I/O select character that is given to it by the processor. As with all I/O devices, any legitimate ACU instruction can be accomplished within the partition (by the ACU), but the ATA is only concerned with input/output instructions, and operates as an independant device. All transfers to and from memory are handled, one character at a time, by the standard INTerrupt scheme.

Table 16-3 shows a summary of the actions that take place, and the device that is selected, by the binary number in the lower four bits of the I/O select character. Figure 16-5 shows a simplified flow chart of the basic ATA operation, and its reaction to interface conditions.

Table 16-3. ATA INSTRUCTION DEVICE NUMBERS

INSTRUCTION	Device no. (LA)	DEVICE	NOTES
READ	Ø or 2 9	Keyboard Reader	A READ instruction to any other device prevents the ATA from accepting the instruction. The IO BUZY flip-flop is not allowed to set, and the instruction "falls through".
READ CONTROL	Ø or 2	Keyboard	If the reader is manually activated, the tape characters will be read onto the transmission line, and appear as if they are coming from the keyboard.
WRITE	Ø or 2 8	Typebar printer Punch	A WRITE instruction to a read type device is not accepted by the ATA. The instruction "falls through" (see note above).
WRITE CONTROL	Ø 1 2 8	Printer Dial Hangup Punch	A time delay is provided for all WRITE CONTROL instructions to the printer.

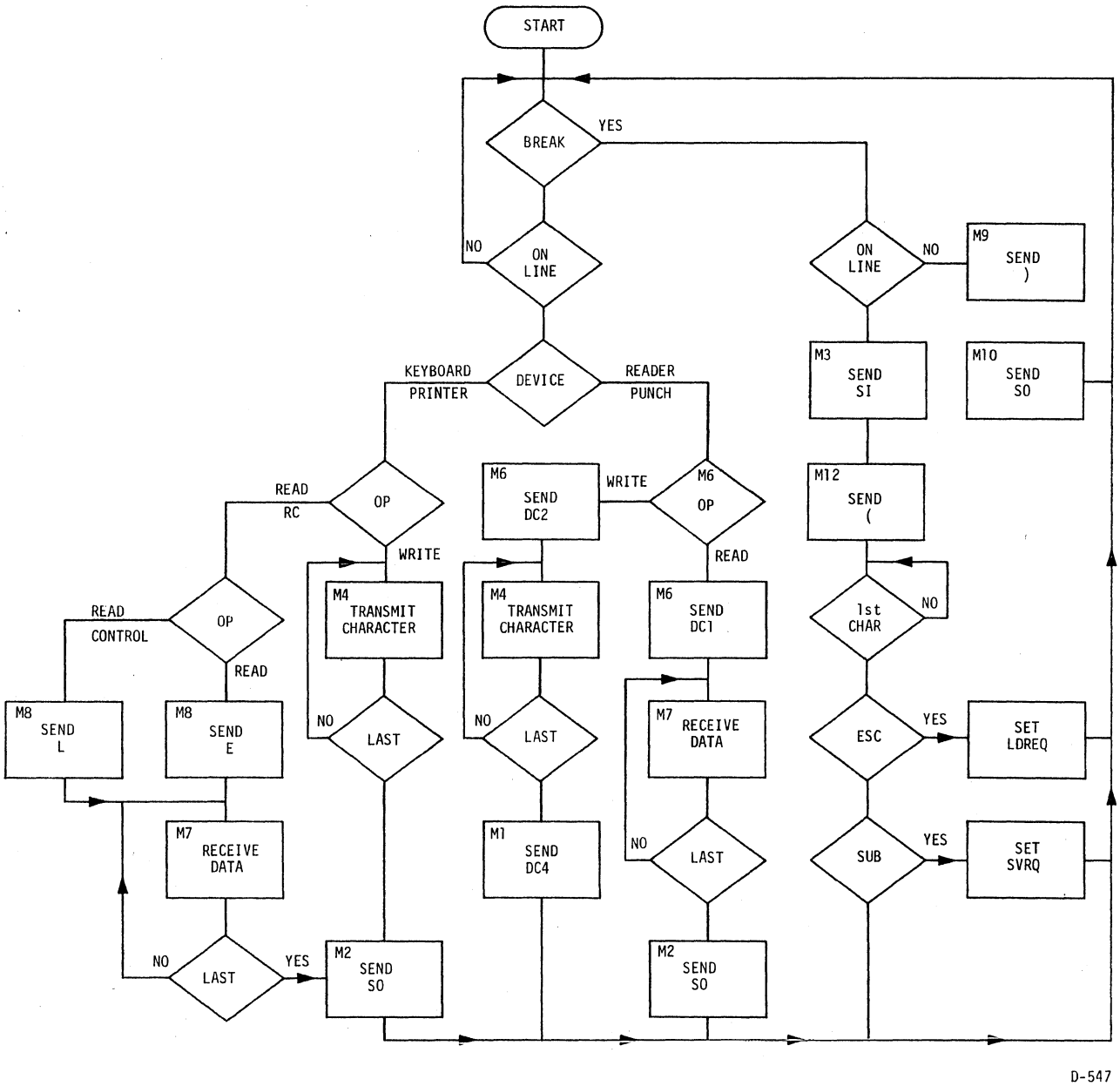


Figure 16-5. SIMPLIFIED LOGIC FLOW

16-6.1 SPECIAL CODES

The ATA detects certain codes that cause special actions. Other codes are generated by the ATA hardware to command device functions, and print one of two operator cues. The table below lists the codes that have meaning, and the special conditions that apply to the situation.

Table 16-4. SPECIAL CODES

CODE	ACTION
	RECEIVE
US or EM	EM sets FLAG; US does not. Both terminate a READ or READ CNTL. In the case of READ CONTROL, the ten character instruction word position will be filled with all zeros (not NULs) if the US or EM is the first character entered. A READ may be filled with NULL codes, or may not be filled at all, according to the non-fill bit (LB=5) in the READ instruction.
CAN	Sets both REPEAT and ERROR if received in a READ or READ CONTROL operation.
ESC	Sets LOADREQ if it is the first character that is detected after entering local.
SUB	Sets SVRQ if it is the first character in local.
	TRANSMIT
HT, FF, BS, VT, CR, LF	Allow a time delay to complete mechanical action (WRDLYTO).
(	Operator cue that the terminal is in LOCAL.
)	Operator cue that the terminal is online.
SI	Used to turn on the terminal printer when a WRITE operation is received, or when an operator cue is to be printed.
E	Operator cue that keyboard (or reader) entry is needed.
L	Operator cue that a ten character instruction word must be entered from the keyboard (or reader).
SO	Turns off the printer after READ or WRITE operations.
DC1	Reader-on command, caused by READ, device no. 9.
DC2	Punch-on command, caused by WRITE, device no. 8.
DC4	Punch-off command, sent at the conclusion of a WRITE operation to the punch.

16-6.2 STATUS INDICATIONS

At the close of each instruction, the ATA reports status by placing the output of the status flip-flops onto the processor INP-DATA lines. The four status indicators can be used to show any unusual conditions that may have developed during the term of the instruction. Table 16-5, below, shows the conditions under which the flip-flops will be set.

Table 16-5. STATUS INDICATIONS

STATUS	INSTRUCTION	CAUSE
ERROR	READ	Receiving a CAN character, a parity error, no start bit, no stop bit, or a data overwrite. NOTE: CAN sets both ERROR and REPEAT.
	READ CONTROL	Same as READ.
	WRITE	Not used.
	WRITE CONTROL	Set by ACR (Abandon Call & Retry) during DIAL.
FLAG	READ	Receiving an EM code.
	READ CONTROL	Same as READ.
	WRITE	Not used.
	WRITE CONTROL	Set by ringing indication during DIAL.
FAULT	READ	Loss of DSR (Data Set Ready), CARRIER, or CTS (Clear To Send). Or if an I/O instruction is active while the terminal is in LOCAL.
	READ CONTROL	Same as READ.
	WRITE	Same as READ.
	WRITE CONTROL	Same as READ, except that the CTS signal is not required during DIAL. During DIAL, a loss of power to the Automatic Calling Unit, or a disconnected cable will provide FAULT status.
REPEAT	READ	Receiving a CAN character. NOTE: CAN sets both ERROR and REPEAT.
	READ CONTROL	Same as READ.
	WRITE	Not used.
	WRITE CONTROL	Not used.

16-7.0 ATA GLOSSARY

NAME	TYPE	SOURCE	DEFINITION
ACR*	SIG	Auto dial unit	Abandon Call & Retry signal is sent by the Automatic Calling Unit when a dialing attempt is not completed satisfactorily.
ACUCLK	SIG	TA2	Direct copy of IOC-MF-CLK or IOC-HF-CLK, according to the bit-rate switch settings.
AUTOWR1 AUTOWR2	FF FF	TA1 TA1	Automatic mode transfer function, changes the basic state, or mode, of the ATA. D/AUTOWR1=$\overline{\text{GOTOM8}}$+STROP+GOMOAD+GOTOM1+GOTOMØ+GOM12M9 T/AUTOWR1=$\overline{\text{ACUCLK}}$ C/AUTOWR1=AUTOWR2 D/AUTOWR2=AUTOWR1 T/AUTOWR2=ACUCLK
BHICLK	FF	TA2	Part of a divide-by-seventeen network, that has either IOC-MF-CLK or IOC-HF-CLK input, and produces signals for further division into timing signals. The clock rate is governed by S2 and S3 on TA2. D/BHICLK=$\overline{\text{HICLK(2)}}$·HICLK(3)·HICLK(4)·HICLK(5) T/BHICLK=$\overline{\text{ACUCLK}}$
BIT	CNTR	TA2	Loaded with a binary 7 by $\overline{\text{ENA1}}$, BIT is incremented by CLOCK. The output of BIT is decoded into signals that indicate serial bit positions relative to the leading edge of the start bit. Load/BIT=$\overline{\text{ENA1}}$ Count/ BIT=CLOCK
BLOCK	FF	TA1	Terminates the operation in FAULT status. Indicates that the modem is not ready, or the terminal is in LOCAL when the op code arrives. T/BLOCK=PIOB D/BLOCK=BREAK+$\overline{\text{BEGIN}}$ C/BLOCK=LOADIOS·ONLINE·$\overline{\text{DIAL}}$·$\overline{\text{IO BUZY}}$ P/BLOCK=LOCAL·PIOB
BMIDCLK	FF	TA2	Similar to BHICLK, part of timing signal division network.
BREAK	FF	TA1	Records the break/idle sequence on the terminal line when the terminal is entering or leaving local. BREAK serves as a buffer for the LOCAL flip-flop. D/BREAK=$\overline{\text{DATADL}}$ T/BREAK=$\overline{\text{TIMR}}$
BS	-	-	Backspace character (ASCII).

*Indicates that the signal is from or goes to the modem or calling unit.

16-7.0 ATA GLOSSARY (Continued)

B1TOB7	SIG	TA2	Active during bits 1 through 7 of the character transfer.
CAN	-	-	Cancel character (ASCII).
CARRIERE*	SIG	MODEM	Carrier Detector (CD) signal from the modem. In other modems this signal is called Carrier On/Off (CO). When the CD signal is on (positive) a carrier is being received from the distant modem. In the 103A data set, the CD and CS signals are simultaneous.
CHECK	XLATCH	TA1	Set by the processor when a program error is detected. Reset by PLDREQ (Preset LDRQ) signal or by INITialization. P/CHECK=ONLINE•PCHECK C/CHECK=PLDREQ•ONLINE+INIT
CLOCK	SIG	TA2	Signal used to increment BIT. CLOCK starts low, then goes high, triggering BIT. CLOCK=ENA2•$\overline{\text{LOWCLK(4)}}$•J6+$\overline{\text{LOWCLK(3)}}$•J6•ENA2
CONTROL CHARACTER	-	-	Any ASCII character having both the 6 and 7 bits =Ø. Used for line disipline, and mechanical actions.
CR	-	-	Carriage Return character (ASCII).
CTSE*	SIG	MODEM	Clear to Send (CS) signal from the modem. When the CS line is on (positive) the modem has established contact with the distant modem, and data can be applied to the Transmit Data line (SDDATA).
DATABIT1	SIG	TA2	Decoded from BIT counter; indicates BIT=9.
DATABIT7	SIG	TA2	Decoded from BIT counter; indicates (BIT=15)•$\overline{\text{CLOCK}}$
DATABIT8	SIG	TA2	Decoded from BIT counter; indicates BIT=Ø
DATADL	FF	TA1	Buffer between received data (DATASN) and the one-shot (TIMR) for detecting a break. It is a delayed copy of RCDATA.
DATASN	FF	TA1	Receives data from the modem (RC Data line); produces a synchronized copy of RCDATA.
DATA1P2M	SIG	TA1	Combined DATABIT1 and PHASE2M signals.
DC1 DC2 DC3 DC4	-	-	ASCII control codes for device turn on/off, etc.
DEL	-	-	Delete character (ASCII).

16-7.0 ATA GLOSSARY (Continued)

DIAL	FF	CH7	Set by DIAL op code (WRC and LA=1) in the ATA. Activates the CH7 card, and the automatic dialing.
DIO	-	-	Direct Interconnection Option.
DPHCTL	FF	TA1	Receives a count from PHCTL that is ACUCLK divided by two; produces an output that is a delayed copy of PHCTL. Both counts are used for phase control. The phase control and counter produce a burst of 5 pulses at the beginning of each bit time, and another 5 pulses at the midpoint of each bit time. The two groups of pulsesare seperated by a "dead" time. Pulses near the start are designated P1S to P5S; pulses near the midpoint are P1M to P5M. Bit and phase information are combined to create signals such as DATA1P2M and ENDWRP1S.
DSRE*	SIG	MODEM	Data Set Ready (DSR) signal from the modem. When DSR is on (positive) the modem is connected to the telephone line, has its power, and is in the data mode. The data mode is defined as not idle, not in talk, test, or local condition.
DTR*	SIG	TA1	Data Terminal Ready signal is derived from the TR signal from TA2. When the DTR signal is on (positive) the modem is allowed to enter and remain in the data mode. DTR must remain at a positive potential to allow automatic answering of incoming calls, and when the modem is manually placed in the data mode. The ATA commands the modem to disconnect the line (hang up) by lowering the DTR signal to zero.
E	-	-	Enter cue to the terminal operator.
EDGE	SIG	TA1	$\overline{\text{DATASN}}$•DATADL
EM	-	-	End of Media character (ASCII).
ENA1 ENA2	FF FF	TA1 TA1	Used to synchronize the BIT CLK with the leading edge of a character, both in send and receive. T/ENA1=$\overline{\text{ACUCLK}}$ T/ENA2=ACUCLK D/ENA1=RUN D/ENA2=ENA1 C/ENA1=BREAK•LOCAL
ENABZY	SIG	TA2	Enables the D input of the IO BUZY flip-flop. It is generated by the presence of a valid instruction to the ATA, preventing IO BUZY from setting if the instruction is invalid.
ENDRD	SIG	TA1	Last character bit of each received code.Usually qualified with other signals such as phase. EXAMPLE: ENDRDP4M= and of STPBIT and P4M.

16-7.0 ATA GLOSSARY (Continued)

ENDWR	SIG	TA2	Last character bit of each transmitted code. Sometimes qualified with phase signals.
WNDRDP3M	SIG	TA1	P3M•STPBIT1 - composite signal used to end a READ operation.
ERROR	XLATCH	TA2	Set during a READ or READ CONTROL instruction, because of a parity error, no start bit, no stop bit, receiving a CANcel character,or if a character arrives before the processor has accepted the previous one. P/ERROR=REPEAT•$\overline{\text{CANREC}}$+RECP1M•STPBIT1•$\overline{\text{DATASN}}$+DATASN• STARTP1M•RECMDS+ RECMDS•$\overline{\text{DATA1P1M}}$•IORA+ $\overline{\text{RECMDS}}$•DATA8P1M•(VRC•$\overline{\text{DATASN}}$+$\overline{\text{VRC}}$•DATASN) C/ERROR=$\overline{\text{M13}}$•ENA1+INIT+MØ•PIOB
ESC	-	-	ESCape character (ASCII).
FF	-	-	Form Feed character (ASCII).
FAULT	FF	TA2	Fault is set by communications problems, such as loss of carrier, data set not ready, etc., or if the operation is active while the terminal is in local. P/FAULT=INIT+$\overline{\text{DSR}}$•IO BUZY+IO BUZY•BLOCK+P1FAULT C/FAULT=PIOB T/FAULT=BREAK•IO BUZY D/FAULT=ALWAYS
FLAG	XLATCH	TA2	Flag is set when the ATA receives an EM code. FLAG is not set by any condition during transmission. Flag is set during a dialing operation if an incoming call "rings" the line before the dialing is completed. The incoming call takes priority.
FLDIOS	SIG	TA2	Trigger for OPCODE. FLDIOS=ONLINE•LOADIOS•($\overline{\text{IOBUZY}}$+$\overline{\text{DIAL}}$)
FILL	SIG	TA2	Fill is one of the qualifications for the TERM-READ signal to the processor, and the "run-out" process that is associated with it. FILL=$\overline{\text{WRCH}}$•(REPEAT+FLAG+FAULT)
GATE	FF	TA1	Gate is used to control PHCTL by clearing it, and stopping the phase count. Gate is triggered by a composite signal that is relative to ENA2 and the LOWCLK matrix. T/GATE=$\overline{\text{DBCLK}}$•HOLD D/GATE=$\overline{\text{GATE}}$ C/GATE=$\overline{\text{ENA1}}$

16-7.0 ATA GLOSSARY (Continued)

GOTOM1	SIG	TA1	Forces the logic to mode 1.
GOTOM3	SIG	TA1	Forces the logic to mode 3.
GOTOM6	SIG	TA1	Forces the logic to mode 6.
GOTOM8	SIG	TA1	Forces the logic to mode 8.
GOTOM9	SIG	TA1	Forces the logic to mode 9.
GOM12M9	SIG	TA1	Forces the logic to mode 9 or 12.
GOMOAD	SIG	TA1	Forces the logic to mode 2, 3, or 10.
INIT REQ	SIG	TA1	Indicates that this partition has requested an INTerrupt cycle. When the processor receives the INTerrupt signal, it steps through all partitions until the active INT REQ line is found.
HICLK	SHREG	TA2	See BHICLK.
HLDMØ	FF	TA2	Prevents the ATA from leaving mode Ø when the modem is not ready. T/HLDMØ=$\overline{\text{ACUCLK1}}$ D/HLDMØ=$\overline{\text{DSR}}$+P1FAULT
HT	-	-	Horizontal Tab character (ASCII).
INIT	SIG	TA2	A general reset signal (INITialize) for the ATA. INIT=MRESET+WRCH•$\overline{\text{DSR}}$
INT	FF	TA1	INTerrupt flip-flop to signal the processor that there is a character that needs to be transfered to, or from memory. D/INT=$\overline{\text{NEVER}}$ T/INT=$\overline{\text{CINT}}$ C/INT=$\overline{\text{IO BUZY}}$ P/INT=$\overline{\text{LAST}}$•$\overline{\text{IOR(7)}}$•M4•$\overline{\text{WRDLYTO}}$+M7•$\overline{\text{LCNTL}}$•DATA7P4M
INTERRUPT	SIG	TA1	Signal given to the processor to indicate a need for an INTerrupt cycle.
I/O	-	-	Term used to signify Input/Output.
IO BUZY	FF	TA1	Set by the processor when the ATA is given the I/O select character, and begins to perform independantly. Reset by the ATA when the operation is complete. An instruction that is ended prematurly is "run out" before IO $\overline{\text{BUZY}}$ is reset. T/IO BUZY=$\overline{\text{PIOB}}$ D/IO BUZY=OPRD+OPWR+WRCH•$\overline{\text{DIO}}$ C/IO BUZY=STOP+BLOCK•LAST•CINT

16-7.0 ATA GLOSSARY (Continued)

IOC	-	-	Input/Output Channel. Any of the processor interfacing devices (contained within the processor mainframe) that allow the exchange of data, into or out of the processor memory.
IOR	SHREG	TA2	IOR is the main data shift register for the ATA. All data entering or leaving the ATA must pass through IOR.
IORA	SIG	TA2	Activity bit for IOR when the ATA is receiving. When IORA becomes active, the serially received character is completely assembled in IOR.
IORCLR	SIG	TA1	IOR clear=INIT+DATA7P4M•XMITMDS+ENDRDP4M•RECMDS•$\overline{INT}$+ M7•CINT
IOR7	SIG	TA2	When the 7 bit position of IOR is filled (with a 1 bit) during transmit, the register is considered active.
IORMD	SIG	TA1	Used to control the serial/parallel mode of IOR. IORMD (shift)=$\overline{NEWMD}$•$\overline{M4A}$+$\overline{INT}$
J6	SIG	TA2	At a logic 1 when the manual switch, S2, is OFF; at logic zero (low) when S2 is ON. J6 is part of the LOWCLK matrix.
KBRD	SIG	TA2	Generated by a READ or READ CONTROL operation to the keyboard.
L	-	-	LOAD cue to the terminal operator. Each READ CONTROL instruction (select character) causes the ATA to send a printer-on (SI), and print an L.
LAST	XLATCH	TA1	Set by the processor (ACU) when the instruction word count is exhausted. P/LAST=P/LAST•ONLINE ($\overline{P/LAST}$ is a signal from the ACU) C/LAST=ONLINE•LOADIOS•$\overline{IO\ BUZY}$•DIAL
LCNTL	SIG	TA2	Generated when the character in IOR is a DELete or a control character.
LDIOS	SIG	TA2	ONLINE•LOADIOS
LF	-	-	Line Feed character (ASCII).
LOADREQ	XLATCH	TA1	Set as an indication to the processor that the terminal needs to load program. The processor can also set load request if an error in the software program is found. P/LOADREQ=ONLINE•P/LDREQ+SETLDREQ C/LOADREQ=C/LDREQ•ONLINE+INIT

16-7.0 ATA GLOSSARY (Continued)

LOCAL	FF	TA1	Places the ATA terminal into or out of the local (off-line) mode. It is toggled by the break detection circuitry. T/LOCAL=BREAK D/LOCAL=ALWAYS C/LOCAL=INIT+M10·AUTOWR1
LOWCLK	BCTR	TA2	Part of the timing pulse network associated with the start and stop bits (see BHICLK).
MIDCLK	SHREG	TA2	See LOWCLK and BHICLK.
MODE	SHREG	TA1	Part of a mode register/counter. Determines the basic operation performed (see text for detailed explanation).
MØ	SIG	TA1	Mode zero.
M13	SIG	TA1	Mode 13.
MRESET	SIG	TA1	One source of initialization; derived from SYS-RST or IO RESET.
MTX	SIG	TA1	Transmit mode; enables the data gates to IOR. MTX=LASTDEL·M4
NUL	-	-	ASCII character containing all zero bits; sometimes called blanks.
ONLINE	SIG	ACU	Indicates the partition is active and selected. ONLINE=SEL-DIG·SEL-GROUP
OP	-	-	Operation - resulting from an input/output instruction, and given to the ATA as an I/O select character.
OPCODE	FF SHREG	TA2	Actually a shift register, a flip-flop, and a decoder combination. It is commanded by data bits from the processor, and is the primary source of ATA operating modes.
OPRD	SIG	TA1	OPRD=KBRD+RDR (keyboard or tape READ).
P/LDREQ	SIG	ACU	Processor signal to the ATA indicating a need to load program. P/LDREQ can be considered as a response to CHECK that was set because the ACU found an error in the software program.
P1FAULT	SIG	TA1	Presets FAULT and enables the D input to HLDMØ. P1FAULT=($\overline{\text{CARRIER}}$+$\overline{\text{CTS}}$)·ENABZY+$\overline{\text{PWI}}$
PHASE(1)	SIG	TA1	Line from the binary 1 output of the PHASE counter. Not to be confused with the P1 output of the PHASE decoder.

16-7.0 ATA GLOSSARY (Continued)

P1M	SIG	TA1	Output signal from the PHASE decoder. Indicates the first phase of the mid-bit pulse.
PHCTL	FF	TA1	See DPHCTL.
PIOB	SIG	TA1	P/IO BUSY•ONLINE.
PRIV-CHAN	SIG	TA1	If enabled by a jumper, it allows the entry of the ATA partition into the priveleged area of common memory.
PUNCHOP	SIG	TA2	Active when the instruction is a WRITE or WRITE CONTROL to the paper tape punch portion of the terminal.
RCDATAE*	SIG	MODEM	Received data signal from the modem. It is held in the mark condition (negative voltage) when the modem is idle.
RD	-	-	READ instruction.
RDC	-	-	READ CONTROL instruction.
RDCKB	-	-	READ CONTROL from the keyboard. This operation is preceeded by a printer-on (SI) code, and the letter L. The next entry from the keyboard will be loaded into memory as program.
RDKB	-	-	READ from the keyboard.
RDR	-	-	READ from the reader (paper tape).
RECMDS	SIG	TA1	Receive mode (M7 or M13).
REPEAT	XLATCH	TA2	Set by receiving a CANcel character. REPEAT is the fourth bit of the status character (repeat if error). S/REPEAT=CAN•$\overline{M13}$•RECMDS•ENDRDP3M C/REPEAT=PIOB+INIT
RUN	JKFF	TA1	General timing and control (see ENA1/ENA2). T/RUN=$\overline{EDGE}$+$\overline{RECMDS}$ (following EDGE•RECMDS) J/RUN=ALWAYS K/RUN=$\overline{RUN}$ P/RUN=IOR(7)•XMITMDS•($\overline{ENA1}$•$\overline{STPWR}$) C/RUN=INIT+CUTOFF
RIE*	SIG	MODEM	Ringing Indication (RI), also called RG1 and RG2 in other modems. When it is ON (positive), RI indicates that an incoming call is ringing on the line.
SD*	FF	TA1	Fluctuates with data bits, driving the Send Data line (through an operational amplifier).

16-7.0 ATA GLOSSARY (Continued)

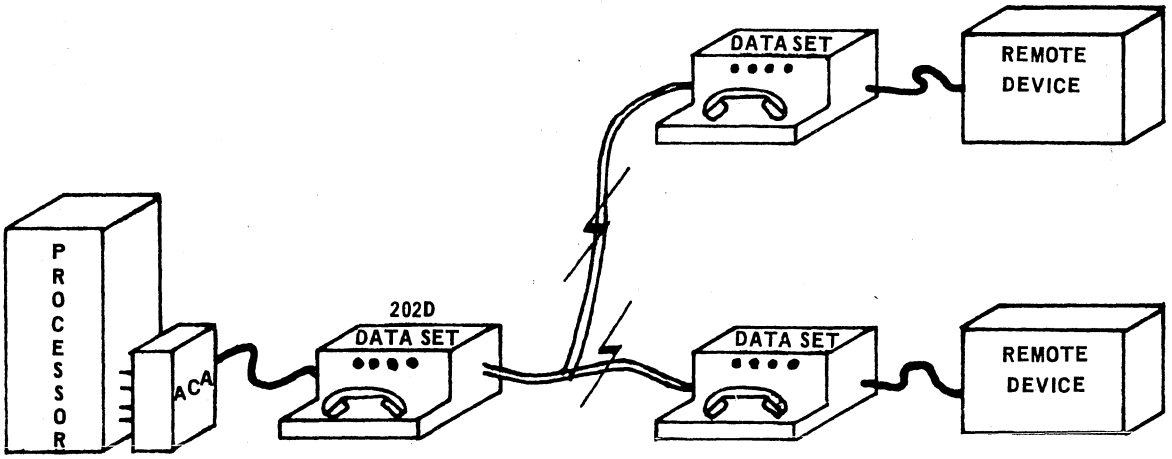
SDDATA*	SIG	TA1	Send Data, called Transmit Data (TD) at the modem. This line can only be active when the Clear To Send line (CTSE) is at a positive voltage. When the transmit data line is at a negative voltage, a mark, or 1 bit, is indicated; when it is at a positive voltage, a spsce is indicated.
SETSVRQ	SIG	TA2	SETSVRQ/3=SUB•M13•$\overline{\text{ERROR}}$•RECMDS•ENDRDP3M (SUB is a decoded signal from IOR).
SETLDREQ	SIG	TA2	SETLDREQ/3=ESC•M13•$\overline{\text{ERROR}}$•RECMDS•ENDRDP3M (ESC is a decoded signal from IOR).
SHIOR	SIG	TA1	Trigger signal for the IOR shift register.
SI	-	-	Shift In character (ASCII) used by the ATA to cause the terminal printer to be turned on.
SO	-	-	Shift Out charactet (ASCII) used to turn off the terminal printer.
START	SIG	TA2	A decode of the start bit for each character that is transmitted or received. It is developed on TA2, and used on TA1.
STOP	SIG	TA1	Developed at the end of an operation, or during initialization, to clear the binary counter in the MODE matrix.
STPBIT	SIG	TA2	Timing relative to the leading edge of the character stop bit.
SUB	-	-	SUBstitute character (ASCII).
SVRQ	FF	TA1	Set whenever the terminal operator wishes to branch to a new place in the software program, as defined in the software instructions. T/SVRQ=RIE (ring indication from the modem) DSVRQ=ALWAYS P/SVRQ=SETSVRQ C/SVRQ=INIT+(C/SVRQ•ONLINE+$\overline{\text{CARRIER}}$)•(DIO+TR)
TERM	SIG	TA1	When a US or EM character is received, TERM is developed (by FILL) to "run out" the remainder of the instruction character count. INTerrupt is held set until the processor sets LAST, and the operation ends. TERM=$\overline{\text{LAST}}$•FILL•IO BUZY
TERMREAD	SIG	TA1	Terminate READ signal to the processor. TERMREAD/3=ONLINE•FILL•OPRD

16-7.0 ATA GLOSSARY (Continued)

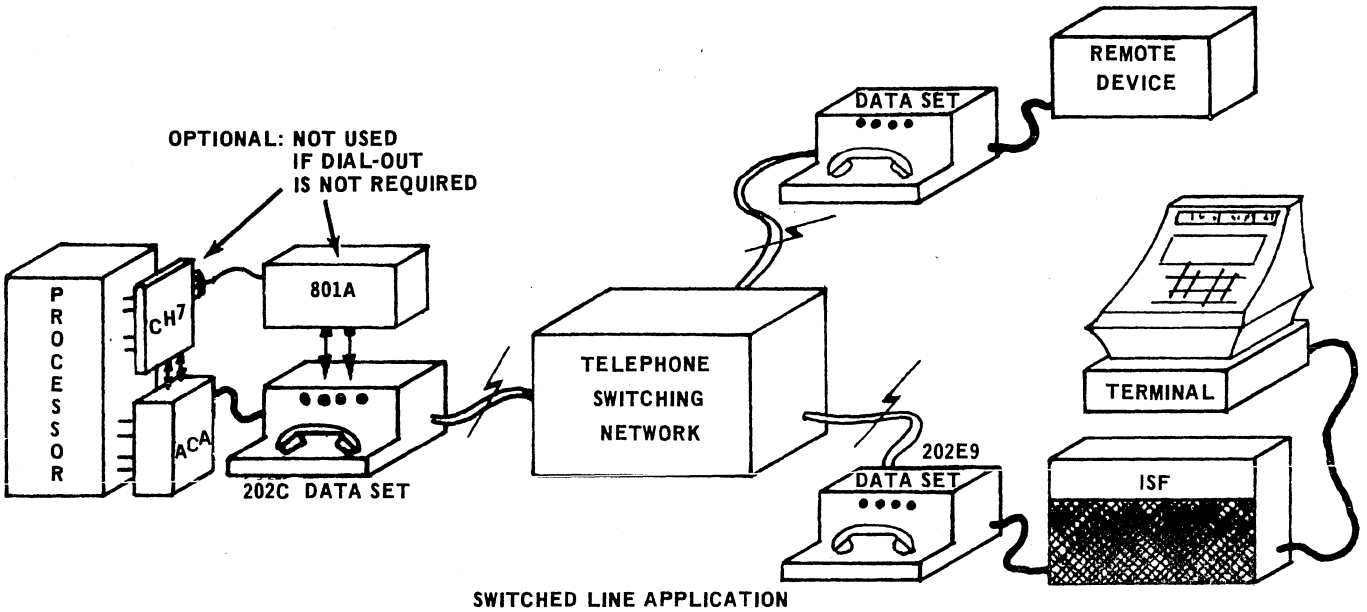
TIMR	OS	TA1	Times the break/local duration on the RCDATA line to allow the terminal operator to place the terminal into, or out of LOCAL operation. T/TIMR=DATASN·DATADL+DATASN·DATADL (If TIMR does not receive a toggle within approximately 200ms, it will time out).
TR*	XLATCH	TA2	Supplies the Terminal Ready signal to the modem.
US	-	-	Unit Seperator character (ASCII). Used to prematurly end a READ operation. A US code from the terminal causes the INTerrupt signal (not the flip-flop) to be held ON, until LAST is set.
VRC	JKFF	TA1	Checks character parity of received data. Also generates parity for transmitted data.
WRDLYTO	OS	TA2	Used for a time delay following the transmission of carriage return and other codes that require time-consuming mechanical action.

SECTION 17
CONTENTS

LIST OF ILLUSTRATIONS



LEASED LINE POINT-TO-POINT, OR MULTIPOINT CENTRALIZED



SWITCHED LINE APPLICATION

Figure 17-1. ACA APPLICATIONS

17-1.0 INTRODUCTION

The Asynchronous Communications Adapter (ACA) enables the model 20 processor to transmit and receive asynchronous data, at an instruction selectable rate of 1800, 1200, 600, 300, or 150 bits per second. Character codes are all seven-bit ASCII, with an additional start bit, a parity bit, and a stop bit. Odd or even parity is hardware checked and generated, but is selectable by the software program.

Communication is intended for either direct-connected leased lines, or through the public dial network. However, in either case, a data set (modem) is required. The remote device can be any asynchronous device using ASCII line format, including another ACA, or it can be an Individual Store and Forward unit (ISF). Figure 17-1 shows the basic ACA configurations.

The ACA can answer incoming calls from the dial system lines without requiring the dial-out option (CH7), and manually dialed calls can be made if the remote (called) device is programmed to accomodate the operation. However, if dialed calls are to originate from the software program, the dial-out option (CH7) must be used in conjunction with an Automatic Calling Unit (801A or equivalent).

The communication format and line dicipline is ASCII, except when receiving data in the ISF mode. The ISF mode is a special case, and is described in later paragraphs.

The ACA does not automatically hang up when an instruction ends, either normally, or because it was aborted. A software instruction (WRITE CONTROL, LA=2) must be issued to cause hangup.

ASYNCHRONOUS COMMUNICATIONS ADAPTER

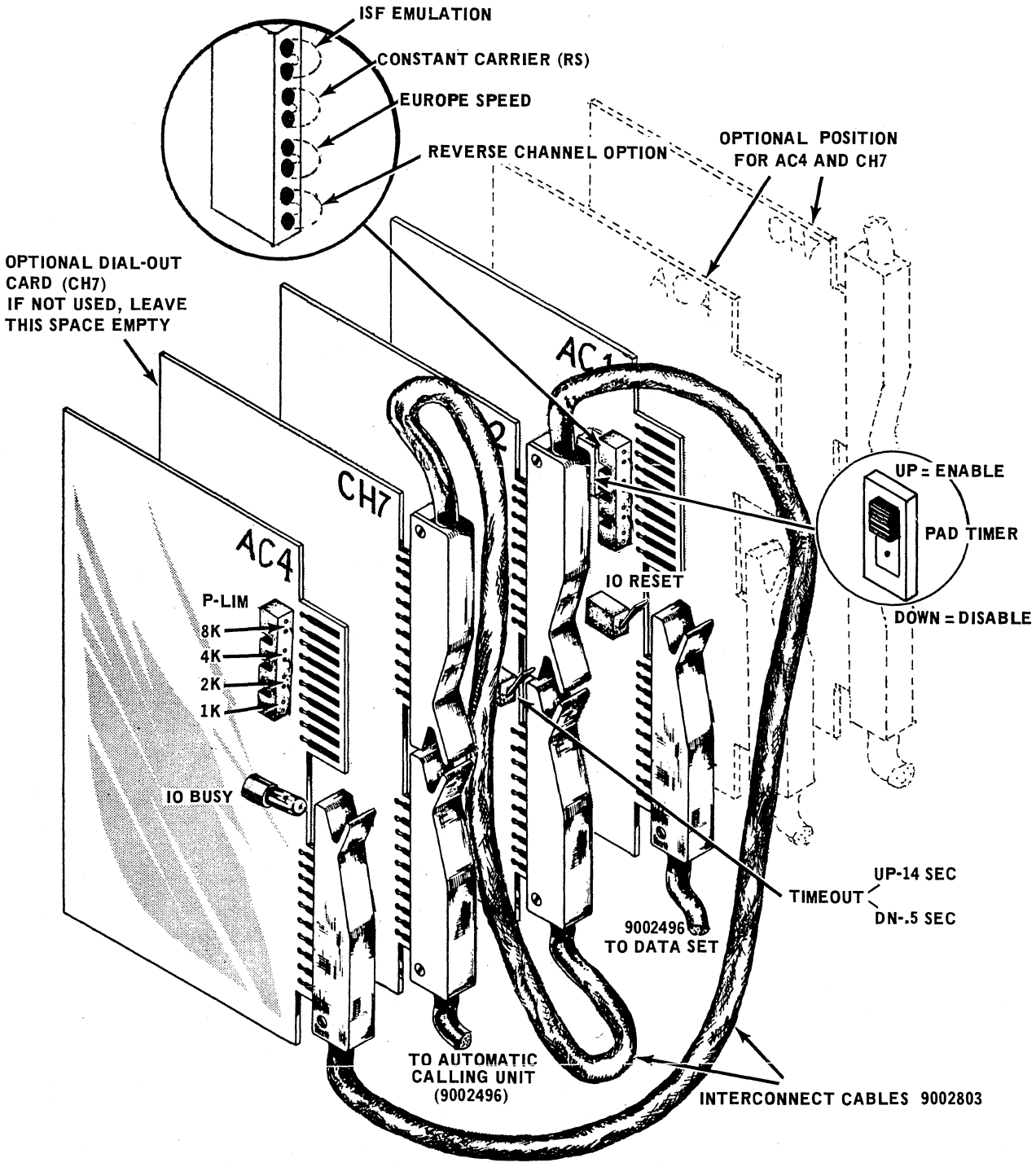


Figure 17-2. ACA CONNECTIONS

17-2.0 INSTALLATION

The ACA physically occupies two adjacent I/O positions within any of the expansion modules of the model 20 processor. Figure 17-2 shows the relationship of the three ACA printed circuit cards, and the optional dial-out card (CH7). AC1 and AC2 must occupy one I/O position, and are always placed as a pair. AC4 and CH7 are also a pair, with the space left blank if the CH7 card is not used. The partition number of the ACA is determined by the position of the AC1 card, and is not affected by the optional position of the AC4/CH7 pair. The table below is a listing of the possible positions for each card.

CARD	POSITION
AC1	D,F,H, or K
AC2	E,G,J, or L
CH7	D,F,H, or K
AC4	E,G,H, or L

If the ACA is placed in a fully configured system, where all possible I/O positions are needed, it should be installed in partition 19 (positions H and J in expansion module 5). The AC4 and CH7 cards can then be placed in the unaddressable K and L positions of expansion module 5.

17-2.1 MODEMS

The 202C, D and E modems (or their equivalent) that are used by the ACA telephone line communication, have a reverse channel capability. This is sometimes called the SUPERvisory lead, as that is the general purpose for which it is used. The ACA only uses the supervisory lead when receiving from an ISF, or in a special case where the ACA is emulating an ISF. The reverse channel is a superimposed signal that travels opposite to the regular data signals. Because of this, the speed capability of the reverse channel is limited to 5 Baud (five changes per second).

17-2.2 ISF EMULATION

The ACA can be programmed and configured to electrically appear as an ISF unit. In this configuration, a Bell System 202E9 modem, or equivalent (the same model that is used by the ISF) is used at the ACA end of the communications link. The software program can be designed to exercise an incalling ACA in a diagnostic routine, or transmit a standard ISF message. In this way field personel can verify the operation of the ISF mode of an ACA.

When the ACA is emulating an ISF, SVRQ is set by an incoming reverse channel signal. The service request is monitored by software for simulation of ISF type reaction to the supervisory lead.

17-2.3 AUTOMATIC CALLING UNIT

The Automatic Calling Unit (A.C.U.), if used, is normally optioned to enter the data mode when the received answer tone is detected. For ISF use, the A.C.U. must be optioned to wait until the end of the answer tone before releasing control. Also, the call termination option should be set to hang up when the Call Request (CQR) line is dropped by the ACA.

17-3.0 INSTRUCTIONS TO THE ACA

The Arithmetic and Control Unit (ACU) can accomplish any valid instruction within the ACA partition. However, the ACA itself is only concerned with input/output (I/O) instructions. These I/O instructions are given to the ACA in the form of an I/O Select character, and the discussion of instructions within this section refers to operations that are directed by the I/O Select character. A diagram of the I/O Select character is shown below.

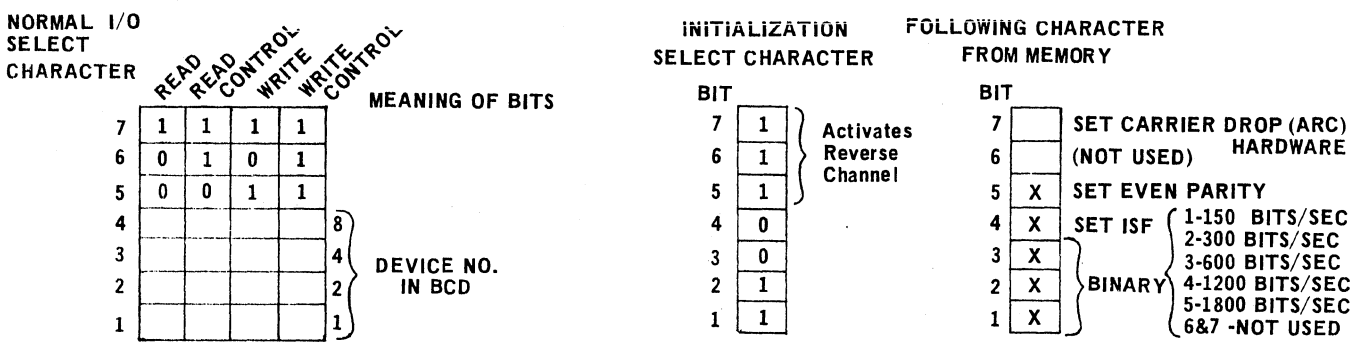
The first instruction after power up, or reset must be initialization. The initialization process is described in a later paragraph.

In READ, READ CONTROL, and WRITE instructions, the device number (LA) causes the ACA to transmit that number of characters (the number specified by the binary value of LA) as control codes. The characters are received from memory as normal characters, but the seventh bit is forced to zero during transmission. Characters are extracted from memory under a READ or READ CONTROL instruction because the OUT-REQ line to the processor is activated when the LA counter within the ACA contains any number greater than zero. The OUT-REQ line forces a temporary WRITE condition within the processor logic. When the required number of control characters have been transmitted, the instruction returns to its normal state. A WRITE instruction will continue sending characters, but the control conversion will not be made; a READ or READ CONTROL instruction will begin receiving. The READ CONTROL instruction is used only in a multi-station environment to establish and recognize a station address. The first character of a READ CONTROL instruction is used for identification, and is not transmitted, regardless of the number specified by LA.

17-3.1 INITIALIZATION

After power down, or system or I/O reset, the ACA requires an initialization procedure before it will accept any operation. Once initialization is made, the parameters that are set, remain throughout all following instructions until a new initialization is made, or initialization is lost because of power failure, or reset.

Initialization consists of a WRITE CONTROL instruction with an LA (device number) of 3, followed by one regular character from memory (through INTerrupt) that sets the bit rate, odd or even parity, or the ISF operating mode. A regular instruction must follow initialization if the ACA is to read or write, etc. Any valid I/O instruction can be given following proper initialization, however, the bit rate, parity, and operation mode (ISF) must be compatable, or errors will occur during the operation. Parameters set by initialization can be changed by issuing a WRITE CONTROL, LA=3, followed by a character that designates the new configuration.



17-3.1 INITIALIZATION (Continued)

If an instruction other than WRITE CONTROL, LA=3 is given to the ACA before proper initialization, the instruction will be terminated by resetting IO BUSY, and FLAG status will be posted. The illustration at the bottom of the opposing page shows the options that are available when the ACA is initialized. The 7 bit of the initialization character is used to enable hardware that causes a 500ms drop in the reverse channel signal when a carrier drop is detected. For ISF operation a reinitialization must be made after dialing. Dialing to an ISF must be done under any initialization that does not contain a 7 bit in the initialization character. After the dial connection is made, the ACA is reinitialized using a reverse slant (\) character that sets the speed, parity, ISF mode, and the ARC hardware.

17-3.2 READ (NON-ISF)

A READ instruction is temporarily converted to a WRITE operation if the I/O Select character contains a device number greater than zero. The binary number of characters specified by the device number are transmitted as control codes, and the ACA returns to a receive mode. If data does not arrive within approximately 14 seconds after receiving the READ instruction, the ACA times out in FAULT status.

Normal READ instructions are ended by receiving one of the ASCII ending codes, ETB, ETX, ENQ, ACK, ACK, NAK, EOT, or a DLE and one character following. A READ instruction that is terminated without one of these characters (by setting LAST), will produce FLAG status. FLAG status disables all other status indications, and will be the only status indication when set, even if ERRORs were also made. If a READ instruction is ended by exhausting the instruction character count (setting LAST), FLAG will be reported. This means that the memory field alloted for a READ instruction must contain the re-mapped equivalent of any control characters that will be sent (as specified by LA), a space that is at least one character longer than the expected message, and one additional space for the BCC.

A READ instruction will remain active in the receive mode for approximately 14 seconds without data. After 14 seconds without data, the ACA times out, and posts FAULT status. The instruction is ended by resetting the IO BUSY flip-flop. The 14 second timer is re-started each time a character is transfered to (or from) memory.

17-3.3 READ CONTROL

READ CONTROL instructions are used only by stations in a multi-station private line network (except for one specific use in the ISF mode). The number that is specified by the device number (LA) of the READ CONTROL select character is used to bring characters from memory to establish a station address, and transmit a "handshake" format. The procedure is similar to that of a READ instruction. The device number, being greater than zero, causes a temporary WRITE condition within the processor, by activating the OUT-REQ line. However, instead of transmitting the first character, it is stored in the ACA Station Identifier (SI) register. At this point the CONTROL function is ended by clearing the CNTL flip-flop, and the operation becomes a READ. If the device number was greater than 1, the remaining number of characters are transmitted as control codes, by surpressing the seventh bit. A READ CONTROL, LA=Ø will cause the ACA to time out, except in the ISF mode, as no

17-3.3 READ CONTROL (Continued)

station address will be installed, and the CNTL (control) flip-flop will not be reset. Timeout occurs after approximately 14 seconds without data.

When the specified number of control characters have been sent, the OUT-REQ line is dropped, allowing the processor to return to a READ configuration. The ACA then compares every incoming character with the one character station address that is stored in the SI register. If a matching character is found, the ACA locksinto a receive mode, and passes the incoming data, including the matching character, to memory (through normal INTerrupt procedures) until: LAST is set, or an ending code is received, or 14 seconds have elapsed without data, and the ACA times out.

Ordinarily ACA station addresses are carefully chosen from seldom used characters, so that the address will not accidentally appear in the text of another station's transmission. However, if the station address does appear on the line accidentally, the ACA will begin receiving data from that point in the message. It is wise to use a password such as ∝012ENQ, and check the password with the program (∝=address).

17-3.4 WRITE

A WRITE instruction to the ACA causes characters to be transmitted until the character count that is specified in the instruction is exhausted, and LAST is set. If a WRITE instruction arrives with a device number (LA) greater than zero, that number of characters will be converted to control codes as they are sent.

The ACA can timeout during a WRITE operation, if the modem is not functioning, or if there is a 14 second pause without data. This condition causes FAULT status to be set.

FLAG is the only status that can be set during a WRITE operation, and only then if the ACA is not initialized. Any instruction that is attempted before initialization will set FLAG status.

17-3.5 WRITE CONTROL

A WRITE CONTROL instruction is used to initialize the ACA, as discussed in the previous pages. However, after initialization, a WRITE CONTROL instruction with a device number equal to 1 is used to initiate dialing (if the automatic dialing option is a part of the ACA configuration). A WRITE CONTROL instruction with a device number equal to 2 is used to HANG UP (disconnect) the dial connection. This instruction is the only way the ACA will hang up (other than manual intervention at the data set). Any WRITE CONTROL with LA=5, 6, or 7 will cause the reverse channel signal to drop and stay OFF until another instruction is received.

17-3.6 DIALING

Dialing is a WRITE CONTROL instruction that contains a device number (LA) equal to 1. The dialing digits are called from memory in the normal INTerrupt manner (by the CH7 card), and the instruction is ended when the processor sets LAST. Dialing can also be terminated by the automatic calling unit, because of excessive delay in some portion of the dialing procedure. This timeout will give the ACA an Abandon Call & Retry (ACR) signal, resulting in ERROR status.

The CH7 card decodes the WRITE CONTROL, LA=1 instruction directly from the processor OUT-DATA lines (with the aid of T/DIAL from the ACA), and performs the

17-3.6 DIALING (Continued)

interrupt and transfer functions independant of the ACA. During the dialing operation, the ACA is in the IDLE mode, and is inhibited from other actions by the signal DIAL that is generated by the CH7 card. When dialing is complete, or terminated, the DIAL signal is lowered, and normal ACA operations can continue.

When dialing is completed, the ACA must receive an I/O instruction before it can communicate. Because of the inherent 250ms modem delay, there is usually enough time to receive an instruction, and be ready for incoming data. If, however, data starts arriving before the instruction is active, it is ended in ERROR. This condition is called a message overrun, and is described in another part of this section.

17-3.7 STATUS

ACA status is given to the processor at the completion of each instruction. The status character, shown below, has the same bit designations as any I/O status character. However, if the ACA ERROR flip-flop is set while operating in the ISF mode, the Transmission Status Character will be generated, and passed to memory before status is given. The TSC only applies to ERROR status in the ISF mode, and is explained in the ISF portion of this section.

BIT		VALUE, OR MEANING
7	0	CONSTANT
6	1	
5	0	
4	X	NOT USED BY THE ACA
3	X	$\overline{\text{FAULT}}$
2	X	FLAG
1	X	ERROR

STATUS CHARACTER

REPEAT IF ERROR - Not used by the ACA.

FAULT - Timeout. In some cases this could be the data set or automatic calling unit inoperative (loss of power, etc,)

FLAG - The ACA was not initialized.
LAST was set while receiving data.
An incoming call was received while dialing out.

ERROR (non-ISF) - The Abandon Call and Retry ,ACR signal was received while dialing out.
No start bit was detected on one or more received characters.
No stop bit was detected on one or more received characters.
Bad character parity.
Block check bad.
Character is received before the previous one is accepted by the processor.
LAST is set, and no ending character is received.
Message overrun - instruction not active when data arrives.
Carrier drop, or Dataset error.

17-4.0 ISF MODE

ACA operation in the ISF mode can be considered as a seperate configuration. While some of the parameters are common to the non-ISF mode, there are many special conditions for the ISF case. The general description below discusses the ACA actions primarily, but must necessarily describe some of the general ISF functions.

When the ISF data set is called by the ACA, the DSR, CTS, and SUPER-REC DATA signals become active. If the CTS and SUPER-REC DATA signals are not active, the ISF will not transmit. If the ISF activity counter is at zero, a constant string of EOTs are transmitted as soon as the data set signals will allow. If the activity counter is not at zero, the ISF must start the tape and perform internal functions that usually take a very short time, but can extend to almost 30 seconds. When the ISF has data, a hardware generated SOH is sent immediately after the ISF receives the necessary data set signals. If the ISF encounters a tape splice, or other delays, the ACA may time out more than once.

If the ISF is part of a master/slave configuration, the master ISF is the first unit to report (transmit data) when dialing is completed. If the master ISF has no data, the master status is passed on to the next ISF in the slave chain. The ISF does NOT transmit an SOH or an EOT when passing control to the next unit. If the next ISF does not have data,control is passed doen the line again, without any transmissions. The process is repeated, passing control down the line, until a unit is found that has data. That unit will immediately send the hardware generated SOH, and procede normally. When more than one slave has data (which is the usual condition) the first unit with data transmitts the contents of its tape, and passes control down the line. Meanwhile, after receiving data from the previous unit, the ACA times out (STO) after about 37ms without data. While the next slave ISF is getting the tape started, etc., the ACA is receiving another READ instruction. In the rare case that a tape splice is encountered, the ACA may timeout again (LTO) in approximately 14 seconds. In the extreme case the ACA may time out twice, before data is received by the third instruction. Notice, however, that the dial connection is not lost by timeout, and only another READ instruction is needed for the ISF polling to continue.

17-4.1 READ (ISF MODE)

A READ instruction in the ISF mode always follows a dialing operation, or another READ instruction as explained above. Dialing can be manual, or automatic, if the proper options are supplied. In the ISF mode a READ instruction causes the ACA to enter the receive mode of operation. Any digits in the LA portion of the I/O Select character will cause the ACA to attempt to transmit, and because transmission is impossible in the ISF mode, it will time out. If no data characters have been received (not even an SOH), the ACA will time out (LTO) in approximately 14 seconds. However, once a data character is received in the ISF mode, the ACA will time out in approximately 37ms, and end the operation by resetting IO BUSY. This is the normal ending when receiving data in the ISF mode, but all other conditions must be correct, such as message length, parity, etc, or ERROR status will be reported.

If data begins to arrive before the READ instruction is active, the ACA captures the first character in the data register, and sets the ERROR flip-flop. When the READ becomes active, the captured character is given to the processor, and the operation is ended, and the ERROR status is reported.

17-4.1 READ (ISF MODE) (Continued)

If an ISF unit (not part of a master/slave configuration) is polled by the ACA, and has no data, the entire memory field that is specified by the READ instruction will fill with Ds, and FLAG status will be posted. The Ds are re-mapped EOTs that are sent in a constant string by an ISF without data. The FLAG status results from LAST being set, while the EOTs are still coming.

A READ instruction in the ISF mode is not ended by an ASCII ending code, but if an EOT, ETB, or ETX is not received in the message, the fact is recorded as an ERROR, and reported in the Transmission Status Character (TSC).

Each incoming character is checked for even parity (the ISF mode requires even parity), and if the parity is bad, ERROR is set, and the reverse channel signal is dropped. The drop in the reverse channel causes the ISF unit to repeat the transmission from the last inter record gap. ACA timeout is suspended while the 500ms reverse channel drop is in progress, and because ERROR is set in the ISF mode, the TSC is generated, and given to memory. If the parity error is recorded on the ISF tape, the process could be repeated indefinately, and the software program must be designed to ward against it. A forced READ can be made in a situation like this by issuing a READ CONTROL. Under a READ CONTROL, the data will be accepted, reverse channel generation will be inhibited, and any characters with parity errors will be discarded, and replaced by a circumflex (^).

17-4.2 READ CONTROL (ISF)

A READ CONTROL instruction is issued to the ACA in the ISF mode to force the logic to continue reading incoming data, even though errors are made. The READ CONTROL (while in the ISF mode) disables the logic that would ordinarily drop the reverse channel signal when an error is detected. However, when a character parity error is detected during an ISF READ CONTROL, the character in error is not sent to memory, but is replaced by a hardware generated circumflex code (^).

The device number (LA) in the I/O select character must always be zero, when operating in the ISF mode. If it is not, the ACA will attempt to transmit, and consequently time out (after 14 seconds).

17-4.3 ERROR (ISF)

An ERROR that is set during ISF READ causes the reverse channel to be lowered for 500ms, and the ISF to repeat data. The ACA timeout circuits are suspended while the reverse channel drop is in progress.

Any ERROR in the ISF mode generates the Transmission Status Character shown at the right. The TSC is given to memory directly before status is posted. Bits that are present in the character indicate the meaning shown; the absence of the bit has the opposite meaning. For example, if bit 3 is not present, the message did not contain an ending code.

Transmission Status Character

BIT

1 – Indicates that even though an error was made, the received data qualifies as a message by containing more than eight characters.

2 – Data set error. A momentary loss of either the DSR or CO (Carrier On) signal from the data set.

3 – Indicates that even though an error was made, there was a good ending code (ETB, ETX, or EOT).

4 – A parity error was detected, or a start bit was not detected in one or more of the characters, or a stop bit was not detected in one or more of the characters.

5 – Character overrun. A new character is received before the previous character has been removed (INTerrupt is still set).

7 – Message overrun. Characters arriving before the READ instruction is effective (LOCKOUT is set).

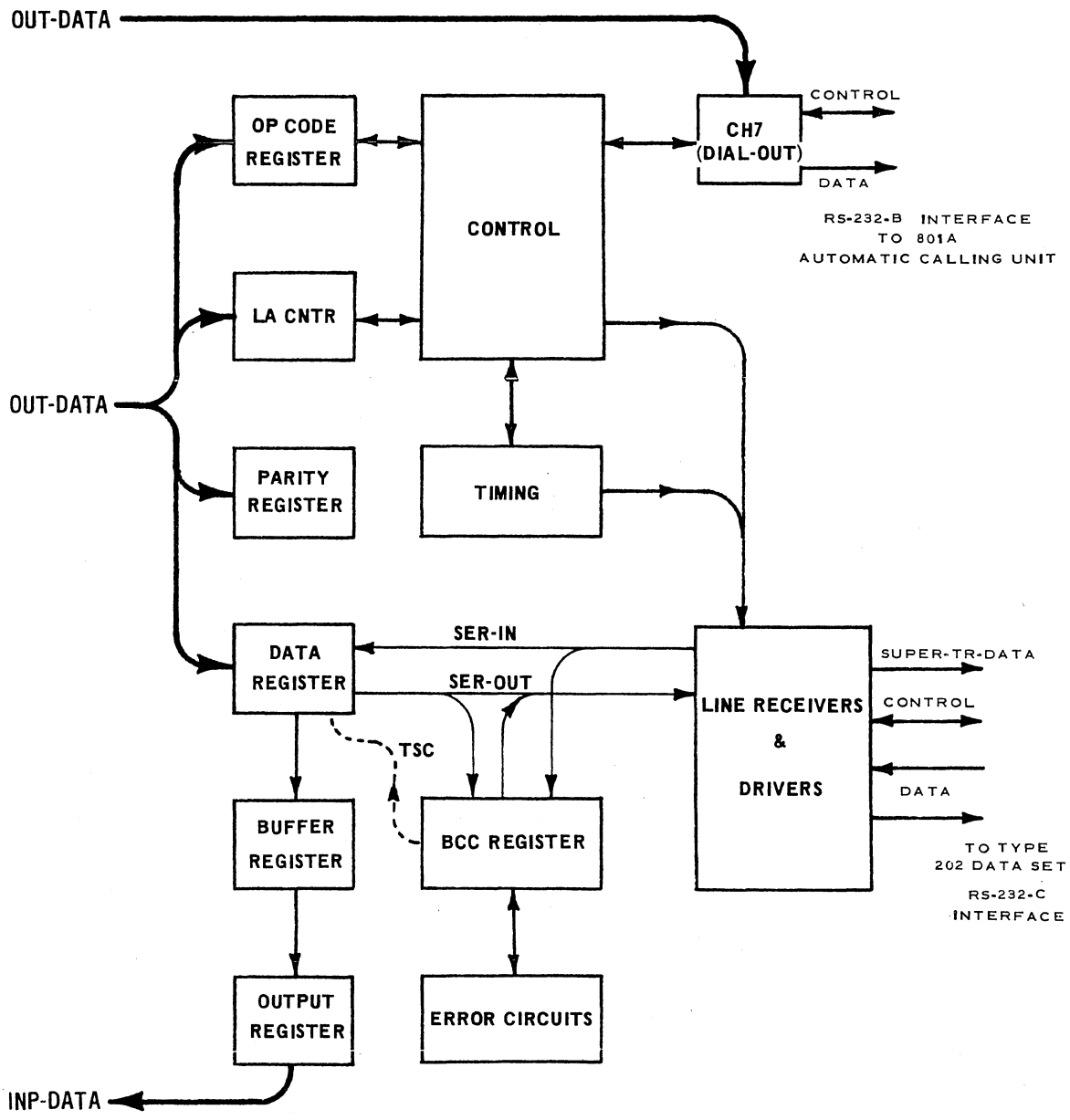
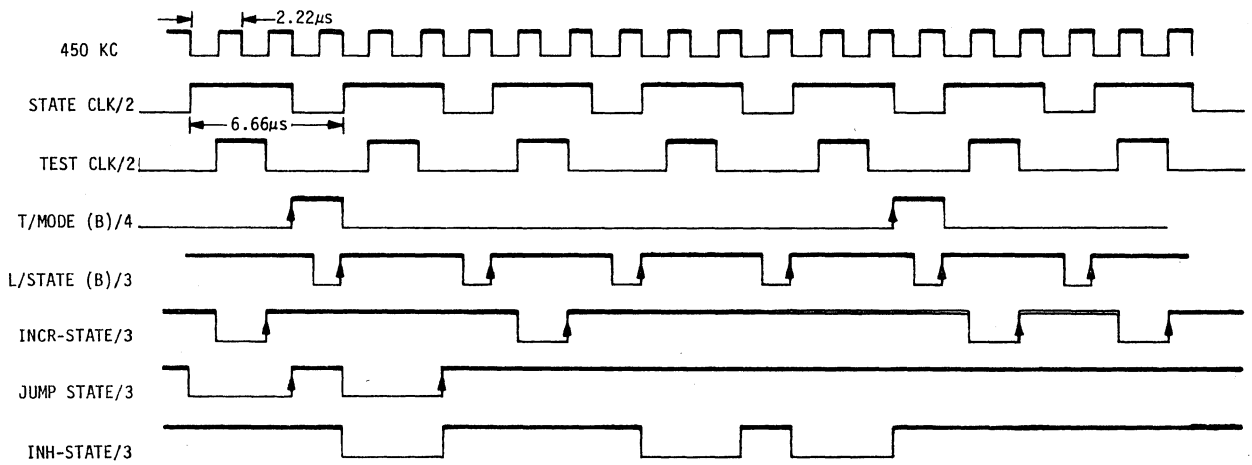


Figure 17-3. SIMPLIFIED LOGIC FLOW

17-5.0 ACA LOGIC FLOW

Figure 17-3 shows a simplified block diagram of some of the ACA logic flow. The "control" circuitry in the illustration refers to the actual gating of signals, and has little relationship to CONTROL operations, as specified in the I/O select character. While timing is simplified to one box in the figure, the operation of the mode and state circuits is described in the following paragraphs.

Timing within the ACA is disciplined by four basic modes: START, IDLE, RECEIVE, and TRANSMIT. These modes are further divided into a series of states. The START mode contains eight states, Ø through 7, IDLE contains 15 states, Ø through 14, TRANSMIT contains only four states, Ø through 3, and the RECEIVE mode contains eight states, Ø through 7. Dialing is accomplished by the CH7 card within the IDLE mode, and no other ACA functions are in progress during the dialing procedure. Figure 17-4 shows some of the general timing signals that are used within the ACA. The overall flowchart shown in figure 17-5 shows the major logic actions, as taken from the ACA algorithms. Operations within the modes and states is described in the paragraphs that follow.



NOTE: 1) JUMP STATE/3 overrides INH-STATE/3 and INCR-STATE/3
2) INH-STATE/3 overrides INCR-STATE/3
3) T/MODE (B)/4 only if L/MODE BUF signal is present
4) L/STATE (B)/3 is a constant pulse
5) INCR-STATE/3 is a constant pulse if no INH-STATE/3 signal is present

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Figure 17-4. ACA TIMING

17-5.1 START

The START mode clears most of the ACA flip-flops, and assures that only a WRITE CONTROL, LA=3 initialization is made. State zero of the START mode is only entered after an I/O reset, or a system reset. Remember though, there is a system reset with every turn-on, or power-up after a power failure (even a momentary failure). Entry is made into the START mode from IDLE, if the select character is a WRITE CONTROL, LA=3, for re-initialization.

In state Ø of the START mode, the ACA inhibits the state counter until the I/O Select character arrives from the processor. When the select character arrives, the OP-REGister and LA CNTR are loaded from the bits in the character. Soon after the select character arrives, the processor sets IO BUSY, that in turn releases the inhibit on the state counter.

State 1 clears the STATUS-RDY flip-flop, and sets FLAG. If the select character does not indicate a WRITE CONTROL, a jump is made to state 6, where the instruction is aborted (and FLAG remains set). If the operation is a WRITE CONTROL, the state counter increments normally to S2.

State 2 checks for a binary 3 in the device number (LA) portion of the select character (the device number was loaded into the LA CNTR in state Ø). State 2 can also be entered directly from IDLE 6, and a possibility exists that INTerrupt is set. If the INT-REQ signal is active, the state counter is inhibited until the interrupt is serviced.

In state 3, the ACA clears the data register, and sets INTerrupt, in preparation for the initialization character from memory. It then steps to S4.

S4 is a waiting state. The state counter is inhibited until the initialization character arrives from memory. The key signal here is the TRANSfer flip-flop; until it sets, the state counter is inhibited.

To reach state 5, the initialization character must have already arrived. The TRANS flip-flop is cleared, and the character is loaded into the INIT register. State 5 is the normal exit from the START mode, and the IDLE code is loaded into the MODE register, the state counter is cleared, and the MODE Buffer (B) is loaded from the mode register, putting the logic into the IDLE mode. FLAG is reset, and good status is posted.

State 6 is a closeout condition, where the first instruction was not initialization. Status is posted (FLAG was already set in S1) and IO BUSY is cleared. When the TRANS flip-flop is set, indicating that the ACU has taken the status indication, the ACA steps to S7.

State 7 clears the state counter, re-loads the START code into the mode buffer (MODE (B)), and returns to SØ.

17-5.2 IDLE

IDLE Ø is the normal returning point for an already initialized ACA. The entire IDLE mode can be considered as a bookeeping mode. Entry can be made from START, RECEIVE, TRANSMIT, or another part of the IDLE mode. Clearing signals are sent to

17-5.2 IDLE (Continued)

the termination flip-flops, resetting them if they are set. These signals are derrived from the TCLK signal which also qualifies the step to S1.

State 1 sets status, clears LAST and IO BUSY, and waits for the status character to be taken by the ACU. When the status character is taken, the TRANS flip-flop is set, and the state counter is allowed to increment.

State 2 clears the STATUS-RDY flip-flop, and the state counter is stepped to S3.

In state 3, the ACA waits for an instruction from the ACU. The instruction arrives in the form of an I/O Select character, and the ACU sets IO BUSY. The select character is loaded into the OP REGister, and the LA counter, and the state counter is incremented.

State 4 (in the IDLE mode) is a time when no logic action takes place. At the end of the normal state time, the state counter increments.

If, in state 5, the operation is not a WRITE CONTROL, the state count jumps to S8. If the operation is a WRITE CONTROL, the counter steps to S6. The TRANS flip-flop is cleared unconditionally by entering IDLE 5.

State 6 implements either a hangup, a new initialization (jump to START 2), or waits for dialing to be completed (by the CH7 card).

State 7 is a closeout state for a WRITE CONTROL operation. If the device number of the select character was 5, 6, or 7, FLAG is set. In any case, the state counter is cleared, sending the logic to SØ.

State 8 is entered from IDLE 5, or 13, or from TRANSMIT 3. The data register is cleared for a data character that will come later. If the ACA is transmitting, or acquiring a station address under a READ CONTROL, the state counter is inhibited until the character arrives from memory. If LD-REQ is set, the state counter is cleared, returning the logic to SØ.

In state 9, the short timeout (STO) oneshot is cleared, if the 14 second timeout has not occurred. If LOCKOUT is set, the state count is inhibited.

State 10 checks for the end of a READ or READ CONTROL operation (receiving). If a receiving operation is ending, a jump is made to S6 of RECEIVE, where the operation is ended.

S 11 checks to see if the LA CNTR is greater than zero. If it has been decremented to zero, the control conversion flip-flop (CCON) is cleared for the remainder of the operation. If the operation is a READ or a READ CONTROL, and the LA CNTR is at zero, a jump is made to SØ in RECEIVE.

In S 12, the INT flip-flop is set, because one or more characters must be transmitted (LA is still greater than zero). The state count is held, until the INTerrupt is serviced, as signified by TRANS setting.

In S 13, if the operation is a READ CONTROL, the character (that just arrived

17-5.2 IDLE (Continued)

from memory) is placed into the Station Identifier (SI) register, and the CNTL flip-flop is reset. At this point, the READ CONTROL operation becomes a simple READ. MATCH is set, so that when the aca enters RECEIVE, the first incoming character will be compared with the station address. If the operation was not a READ CONTROL, preparations are being made to transmit a character. The TRANSMIT code is loaded into the mode register, and the CHAR-DCDR is enabled. An SOH or STX will start the block check accumulation, and an ETX or ETB will stop the accumulation, and set the BCC RDY flip-flop. In any case, if the LA CNTR is greater than zero, it is decremented one count.

State 14 clears the state counter, loads MODE(B) from MODE, and the ACA is in the TRANSMIT mode.

17-5.3 TRANSMIT

The TRANSMIT mode has only four states (Ø, 1, 2, and 3), as most of the character checking was done in the IDLE mode. Only one character is transmitted for each entry into the TRANSMIT mode, and a return is made to the IDLE mode for the next character.

In state Ø, the character parity bit is loaded into the data register, and the Request To Send (RTS) signal is sent to the data set). The state counter is held until the Clear To Send (CTS) signal returns (the Data Set Ready signal must also be active).

As the step is made into S1, the IDLE code is loaded into the mode register. The character is shifted out in ten serial bits. If the LA CNTR is at zero when the shifting is complete (SHCOMP), the pad timer is triggered as the state is stepped.

In state 2, if LAST or READ are set, the state counter is held until the pad timer expires. Then the contents of the BCC register are gated into the data register. If LAST or READ are not set, the BCC is gated to the data register immediately.

The BCC is only used if the message is complete. This is detected by the BCC-RDY signal that may have been set in ID 14 if the character was an ETX or an ETB. In this case, the logic does not return to IDLE for another character, but loops back into TR Ø, where the block check character will be transmitted.

There are three ways of leaving the TRANSMIT mode: timeout, looping to IDLE for the next character, and an exit to IDLE Ø where status can be taken. The two exits to the IDLE mode are determined by the LAST flip-flop. If LAST is set, the exit is to ID Ø, to present status.

When an exit is made from TRANSMIT because of timeout, FAULT is set, and TRANS is cleared. Because TRANS is cleared, the logic progression is held in IDLE (after status is taken) until the next instruction (I/O Select character) arrives.

17-5.4 RECEIVE

The RECEIVE mode is entered during a READ or READ CONTROL operation, from the IDLE mode, after any needed control characters have been transmitted (in other words, when LA=Ø). The exception to this is when TERM is set, and the operation is to be prematurly ended by jumping directly to states 6 and 7 of RECEIVE.

In SØ, the request to send signal is dropped, by clearing the CA flip-flop. The reverse channel signal (RCH) is triggered, but unless the ACA is operating under ISF initialization, the RCH oneshot is held clear by a seperate signal, and will not set. Timeout is checked constantly while the character is being clocked into the data register (one bit at a time). If the 14 second long tomeout (LTO) expires, the state is cleared, and a signal is created (GOTOIDLE) that forces a jump to ID Ø. A normal receive operation does not timeout, and the ACA is held in SØ until the character is completely shifted into the data register. At the next TCLK, the character is sent on, into the buffer register, and the state is stepped one count. If LAST is set during this time, and the ACA is not operating in the ISF mode, the operation will be closed out, by jumping to state 6. The TERM flip-flop can also cause the operation to close out. TERM can be already set, or it will be set if the short timeout (STO) expires. TERM causes an examination of the last character to determine the disposition of the BCC, before closing out the operation.

In S1, the logic is checked for ISF operation. If the ACA is operating in the ISF mode, LTO is triggered, and the state counter is cleared to SØ where the next character will start arriving. This loop is completed once for each character that is received in the ISF mode. The ISF operation ends when STO expires. During the entire receive operation, there are parallel circuits that are checking for parity errors, minimum message length, etc., and these circuits set conditions that are examined at a later time. If a DLE, ETB, or an ETX has been received, TWO-CHAR-TERM will be set, and if it is, the TERM flip-flop is set at this time. Also checked in S1, is the MATCH flip-flop. MATCH will be set if the ACA is operating under a READ CONTROL instruction, in a multi-station environment, and must compare the incoming character with the stored address.

S2 is used only in a READ CONTROL operation to check the station address; all other operations step through S2 without action.

In S3, the character is checked for starting or ending codes, so the block check will be started, accumulated, or ended according to the code that is received.

S4 either clears the data register, and returns to SØ, for the next character, or if LAST or TERM are set, a jump is made to S6 to close out the operation.

S5 clears the state counter on the normal loop to SØ to receive the next character. If the operation is ending, S5 is bypassed.

S6 is a general close out for the receive operation. The IDLE code is loaded into the mode register in preparation for the mode change. If an error was made while in the ISF mode, the TSC is brought from the BCC register (where it was assembled) to the data register. If LAST is set, there is a possibility of an overrun, and FLAG is set, inhibiting INT, because no more characters can be taken by memory. If TERM is set, it is cleared by the next TCLK. If LAST is not set, the state is inhibited until the registers are empty, and the close out can be completed in S7.

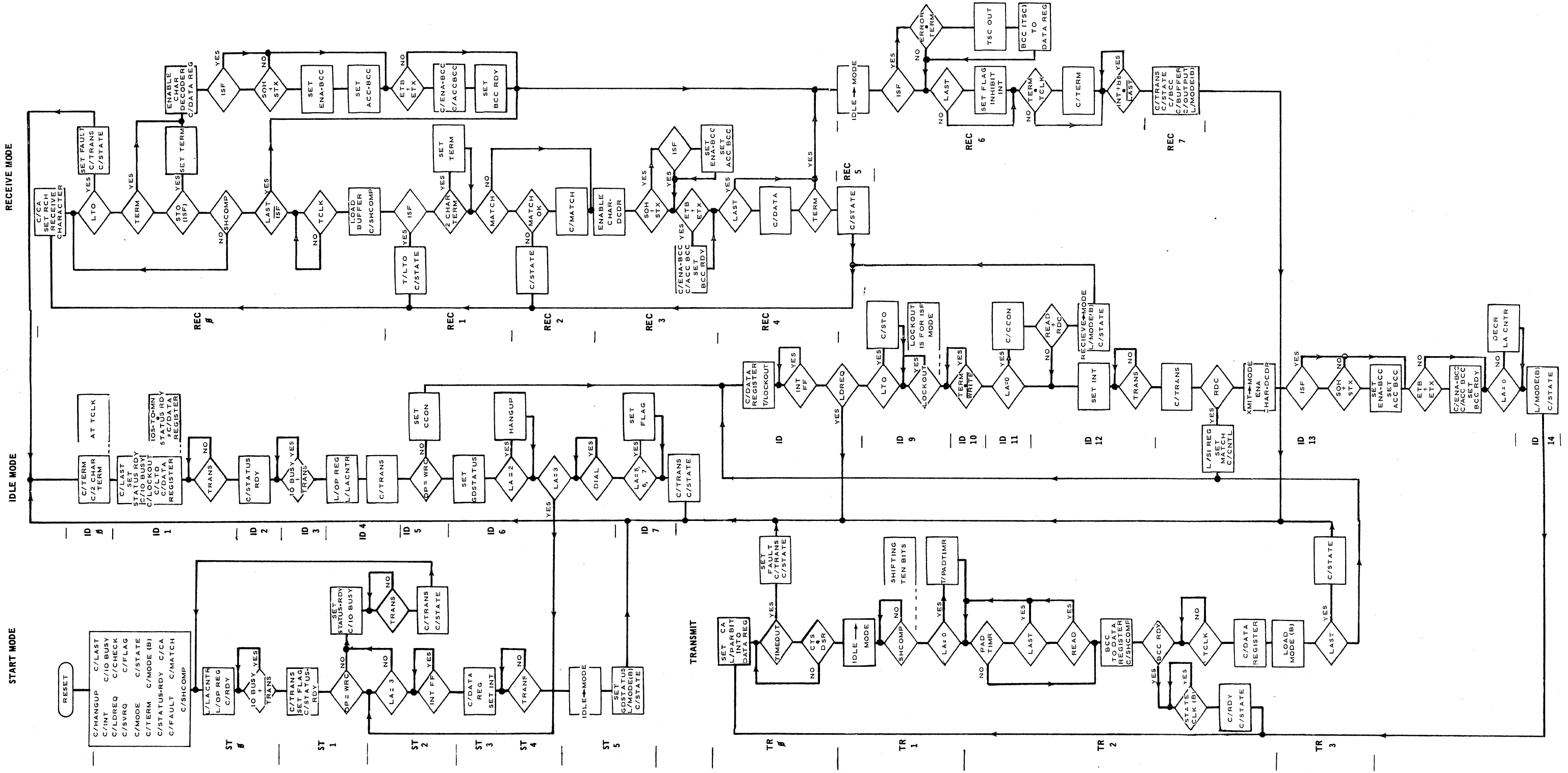


Figure 17-5. ACA LOGIC FLOW

17-6.0 GLOSSARY

NAME	SOURCE	TYPE	DEFINITION
ACR	AUTO DIAL UNIT	SIG	Abandon Call & Retry - Indicates something went wrong during the automatic dialing. The problem could be a line disconnect, no carrier tone on the answered number, or other difficulties related to dialing. ACR sets ERROR in the ACA.
ACC BCC	AC2	FF	Accumulate the BCC. One of three flip-flops dealing with the BCC register. It starts a block check of the data bits.
ACUTO	CH7	SIG	Indicates that the automatic dialing unit has timed out. This timeout interval is an adjustable duration, and should be verified at the time of installation, or if trouble occurs. The adjustment is within the automatic calling unit, (telephone equipment), and is detailed in the technical literature for that unit.
ARC/1	AC2	SIG	Automatic Reverse Channel - a pulse of approximately 500ms duration, that is generated by a "oneshot" (retriggerable monostable multivibrator). ARC causes a drop in the reverse channel signal because of error detection, or if it was enabled during initialization, because of a carrier drop.
BCC -- DATA REG	AC1	SIG	TR2+REC6•TSC-OUT causes a parallel load of the block check character (from the BCC register) to the data register.
BCC-RDY	AC2	FF	Indicates that the block check character is ready to send onto the line, in the transmit mode, or ready to compare with the received BCC character in the receive mode.
BCCREG	AC2	SHREG	Two shift registers in which the BCC character is stored and compared.
BUFFER	AC4	CNTR	Data buffer register, loads and dumps parallel only.
B8/2	AC4	SIG	The eighth bit of the buffer register is used as an activity bit. When B8 is present, the buffer register has been loaded.
CA	AC1	FF	Receives its name from the lead designation on the modem, or data set. Activated by Transmit/SØ, the CA flip-flop drives the logic for the Request To Send (RTS) signal. CA is cleared by Receive mode.

CARRIER	MODEM (CF)	SIG	When the CARRIER signal is ON (positive voltage), the modem has detected a tone carrier from the distant modem. If the carrier tone dissappears, even momentarily, CARRIER will drop, and the ACA will report ERROR.
CHAR DCDR	AC2	DCDR	Decodes the special control characters that are used in the asynchronous communications system (ENQ, ACK, NAK, SOH, STX, ETB, ETX, EOT, and DLE).
CHECK	AC1	FF	Can only be preset by the processor when the ACA is ONLINE, and the arithmecic and control unit has found an error in the software program. CHECK indirectly causes LDREQ to set, which restarts the program by setting good status, and clearing IO BUSY (forcing a jump to memory location ØØØØ).
CTS	MODEM (CB)	SIG	Clear To Send appears approximately 250ms after the modem has received the Request To Send (RTS) signal. It is an indication that the modem is ready to accept data for transmission.
C/BCC/3	AC1	SIG	Clears the BCC register, and the data register.
C/CCON/3	AC1	SIG	Clears the control conversion flip-flop (CCON). The CCON flip-flop surpresses the seventh data bit to logic zero whenever the LA CNTR does not equal zero.
C/DATA REG/3	AC1/AC2		Signal that has many sources, and is used to clear the data register.
C/INT/3	ACU	SIG	Clears the INT flip-flop when the ACU has completed a character transfer after an interrupt request.
C/MATCH	AC1	SIG	Resets the MATCH crosslatch.
C/NC	AC2	FF	CONTROL/NOT CONTROL flip-flop.
C/RDY/3	AC1	SIG	Clears the BCC-RDY flip-flop. C/RDY= $\overline{\text{ST-CLK}}\cdot\overline{\text{TR2}}\cdot$BCC-RDY
C/TERM/4	AC1	SIG	(IDLE Ø+REC 6)·TERM·TCLK clears the termination flip-flop.
DATA-IN/4	AC1	SIG	Signals from the RC-DATA line (from the modem) that are also qualified by the carrier signal. DATA-IN is disqualified if a reverse channel pulse is in progress.
DATA-RATE SEL	AC1	SIG	Derrived from an output of the initialization flip-flops. Used only with European modems that require a data rate selection signal.

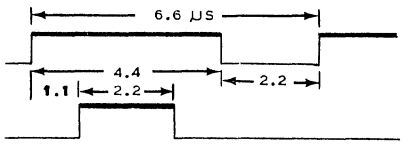
DECR-LA/3	AC1	SIG	Decrements the LA CNTR on AC2 each time a character is transmitted.
DIAL	CH7	SIG	Indicates that the ACA is in the dialing mode. DIAL is a flip-flop, located on the CH7 card, and takes its qualification signals directly from the processor OUT-DATA lines. The trigger for the flip-flop is furnished by the ACA (T/DIAL signal from the AC2 card). DIAL will only set if the select character is a WRITE CONTROL with LA=1, and the trigger signal is present.
DSR	MODEM (CC)	SIG	Data Set Ready means that the modem is in the receive mode, and ready to receive data from the distant modem. The Data Terminal Ready (DTR) signal must be active before the DSR signal will appear.
(DS)ERROR	AC1	SIG	Data set error = $\overline{\text{CARRIER}}+\overline{\text{DSR}}$ If the ACA is in the ISF mode when this signal becomes active, bit 2 will be set in the Transmission Status Character (TSC). The BCC register is used to assemble the TSC in the ISF mode.
DTR/3	AC2	SIG	Data Terminal Ready tells the modem that the ACA is activated, initialized, and ready (has an I/O instruction).
ENA-CHAR-DCDR	AC1	SIG	Enable the character decoder signal is active during three states of ACA operation to allow character decoding: IDLE 12 (before transmitting), RECIEVE 3 (to decode the received character), and ISF RECEIVE Ø (to decode an expected SOH).
ENA-CLK	AC2	FF	While much of the clocking circuitry runs constantly, the character clocking circuits are started by ENAble CLocK when the start bit of a character is detected. ENA-CLK remains active to sample 10 bits, then drops, because of a carry signal from the bit counter.
HANGUP	AC1	FF	D=NEVER P=S/$\overline{\text{HANGUP}}$ C=$\overline{\text{DSR}}$ T=C/MODE(B)
IDLE	AC1	SIG	Qualified signal output from the MODE(B) flip-flops. It indicates that the ACA is in the IDLE mode.
ID9	AC1	SIG	Idle mode, state nine.
IDLE	AC1	DCDR	Binary-to-decimal decoder for the unique states within the IDLE mode.

IO BUSY	AC1	FF	Set by any input/output instruction. IO BUSY is set by the processor, and remains set until the I/O operation is completed (or aborted), and is then reset by the ACA logic.
IOC-HF-CLK/3	ACU	SIG	Main timing signal from the processor (450kHz).
INT	AC1	FF	Interrupt is set by the ACA when a character transfer, to or from the processor, is required.
ISF/2	AC2	SIG	The output from an initialization code quad-latch. When ISF/2 is at a logic 1, the ACA is presenting the characteristics to communicate with an ISF unit.
LA=Ø/4	AC2	SIG	Decoded output of the LA CNTR. Indicates that the device number (LA) inthe instruction was zero, or that the number of characters specified by LA has been transmitted, and the LA CNTR has been decremented to zero.
LA	AC2	DCDR	Decoder for the LA counter.
LA CNTR	AC2	CNTR	Decimal counter that stores and counts down the LA portion (device number) of the I/O select character. The LA counter is also used to count the first eight characters from an ISF unit, to qualify a valid message length.
LAST	AC1	FF	Set by the processor when the character that is about to be transfered is the final count of the number specified for the instruction field.
LDREQ	AC1	FF	Set only by the processor after a data check. LDREQ loads good status, and clears IO BUSY, causing the program to restart from location ØØØØ in the ACA partition.
LA=5+6+7/4	AC2	SIG	Decoded output of the LA CNTR: sets FLAG.
LOAD BUF/3	AC2	SIG	Load the buffer register. The buffer register is two binary up/down counters that are only allowed to parallel load. They are loaded only when shifting is completed, and at the next TSTCLK pulse.
LOCKOUT	AC2	FF	Used only in the ISF mode to indicate that data is arriving without the ACA having an active instruction (ERROR status will be posted). LOCKOUT also delays the next instruction until the data stops comming. This is done by triggering the reverse channel signal to the ISF.

LTO	AC2	OS	Long Time Out. A 14 second timeout that is set at the beginning of an operation, and re-triggered by the C/INT signal when the processor services a character transfer. The LTO will not expire if the trigger signals are more frequent than the 14 second duration that is re-started with each trigger. If approximately 14 seconds pass with no data transfer, the LTO expires, setting FAULT, and the ACA must receive a new instruction before proceding.
L/INIT-CODE STCODE	AC1	SIG	The clock, or trigger, signal for the quad-latch on AC2 that receives the initialization code. The quad latch is essentially four D flip-flops in one chip.
MATCH	AC2	XL	Only the reset side of the MATCH crosslatch is used, creating the signal $\overline{\text{MATCH}}$/4. During a READ CONTROL instruction (a multi-station environment) MATCH is set while the ACA is waiting to receive the station address. When the proper address arrives, and a favorable comparason is made, MATCH is reset, making the $\overline{\text{MATCH}}$ line a logic 1.
MATCH-OK/4	AC4	SIG	Becomes a logic 1 when the station address compares (in a multi-station environment). MATCH-OK/4 can only appear during a READ CONTROL instruction.
MF	AC2	SIG	The reset lead of one of the initialization code flip-flops. MF indicates that the ACA is operating in the Medium Frequency range (1200 bps). The MF signal is used differently in the United Kingdom and Europe configurations, and is not used in the United States.
MODE	AC1	FF	Two D flip-flops that are loaded with one of the four possible mode conditions, Start, Idle, Transmit, or Receive.
MODE(B)	AC1	FF	Two D flip-flops that act as buffers for the MODE flip-flops. The MODE flip-flops can be preset or cleared without changing the ACA mode. At a precise time, the conditions in MODE are clocked into MODE(B).
MSG	AC2	FF	Message. The LA counter and decoder are used to count incomming characters during ISF READ. Eight characters constitute a minimum valid transaction from an ISF unit, and when the eight characters have arrived, the MSG flip-flop sets to indicate a valid message is received. The MSG indication is not used except when an error is made (in the ISF mode), and the Transmission Status Character is generated.

ONLINE	AC1	SIG	Indicates that the ACA is being addressed by the processor (SEL-DIGIT and SEL-GROUP).
OP=RDC/3	AC2	SIG	Indicates that the active instruction in the ACA is a READ CONTROL. The signal comes from the OP REG, which is two D flip-flops.
OP=RD+RDC	AC2	SIG	Output of the reset side of the W/R OP REG flip-flop. When OP=RD+RDC is at a logic 1, the active instruction within the ACA is either a READ or a READ CONTROL.
OP=WRC/3	AC2	SIG	Indicates that the ACA is working under a WRITE CONTROL instruction.
O8/2	AC2	SIG	Activity bit of the output register. When the O8/2 signal is active, the output register has been loaded. The output register is a binary up/down counter that is only allowed to load parallel.
PAD TIMER	AC2	OS	Creates approximately 4ms delay to the CA signal Request To Send line) turnoff after the last character has been sent. If the RTS signal is dropped too soon, the last bits of the character may not be transmitted properly by the modem.
REC	AC1	DCDR	Binary-to-decimal decoder for the unique states within the receive mode.
RESET/2	AC1	SIG	From the SYS-RST/7 of from the manual I/O RESET switch on AC1. Resets the logic to the turn-on state.
RCØ	AC1	SIG	Receive mode, state zero.
RC-DATA/7	MODEM (BB)	SIG	Direct lead from the modem, it carries the incoming data. The data is later qualified with CTS to produce the DATA-IN signal.
RCH	AC2	OS	Generates a 500ms pulse for automatic reverse channel (ARC). Used only during ISF operation (see SUPER-TR DATA).
RC/2	AC1	SIG	Indicates that the ACA is in the receive mode.
RC1	AC1	SIG	Indicates that the ACA is in state 1 of the receive mode.
RC6/4	AC1	SIG	Receive mode; state 6.

RTS	AC1	SIG	Request To Send. Controlled by the CA flip-flop, RTS is the signal that is used to activate the modem for data transmission. RTS must be answered with Clear To Send (CTS) before transmission can begin.
SAMPLE	AC2	FF	Generates a 110ns pulse (approximately) for mid-bit sampling (at 1200bps, the sample is taken at approximately the 2/3 point of the bit). During receive, there are ten pulses to sample; during transmit, eleven pulses are present to provide equal time for ten bits.
SD	AC2	FF	Send Data is a signal to the modem data line. It follows the OUT-DATA signal at S-CLK (SAMPLE) time. The SD flip-flop remains set when the ACA is not in the transmit mode (a modem requirement).
SDDATA	AC1	SIG	The SEND-DATA/2 signal is amplified and inverted for presentation to the modem, and is called SDDATA/7.
SEND-DATA/2	AC2	SIG	Comes from the SD flip-flop, and is the data line to the modem, furnishing it with serial data bits. SD is preset, holding the line in a mark condition, when the ACA is not in the transmit mode.
SERV-REQ/2	AC1	SIG	SERV-REQ/3 is the same signal, but is qualified by ONLINE. SERV-REQ/2 is the set output of the SVRQ flip-flop.
$\overline{\text{SHCOMP}}$	AC2	XL	Shift not complete. Data is shifted ten times before the bit counter causes $\overline{\text{SHCOMP}}$ to set, indicating that all ten bits are in the data register.
STATE-CLK/2	AC4	SIG	Main clocking signal, is approximately 6us per each complete cycle.
STATE CNTR	AC1	CNTR	Source of the ACA states that are decoded by the START, IDLE, TR, and REC decoders.
START	AC1	DCDR	Binary-to-decimal decoder for the unique states within the start mode.
STO	AC2	OS	Short Time Out. Approximately 37us interval timer, that is started by incoming data.
SUPER-TR DATA	AC1	SIG	Used only during an ISF READ instruction, and only then if an ERROR is made. The SUPER-TR DATA line causes the modem to drop the reverse channel indication that will make the ISF rewind to the last inter-record gap.

SVRQ	AC1	FF	P/SVRQ=RCH•TP7/TP8 (TP7/TP8=ISF EMULATION) C/SVRQ=IO RESET+ONLINE•C/SERV-REQ D/SVRQ=RCH T/SVRQ=RING•IDLE•$\overline{TP7/TP8}$, then $\overline{RING}+\overline{IDLE}$ Service request is only set after initialization, in the IDLE mode, and when there is an incoming call. An incoming call is ignored once the ACA has entered either the receive or transmit mode. However, if test points 7 and 8 on AC1 are connected, The ACA is emulating an ISF, and SVRQ will be pre-set by the SUPER-RECEIVED DATA (reverse channel signal.
S/CCON/3	AC1	SIG	Sets the CCON flip-flop (see CCON).
S/FLAG/3	AC1	SIG	Presets the FLAG flip-flop.
S/GD-STATUS	AC1	SIG	Resets FLAG and ERROR, and sets the FAULT flip-flop at the beginning of each new instruction.
S/INTERRUPT/3	AC2 AC4	SIG	Presets the INT flip-flop on AC1. S/INTERRUPT/3 is the same signal line as 08/2, but is used in the logic zero condition. In other words, when 08/2 goes to a logic zero, the INT flip-flop is preset.
S/STATUS-RDY/3	AC1	SIG	Presets the STATUS-RDY flip-flop on AC2. Also clears the IO BUSY flip-flop.
TCLK/2	AC4	SIG	Test Clock is an internal timing signal that is of the same frequency, but of shorter duration, than ST-CLK. TCLK is completly contained within the time of STCLK as shown below. 
T/DIAL	AC2	SIG	Qualified by LOAD-IOS, and ONLINE, the signal triggers the DIAL flip-flop on the CH7 card. DIAL will not necessarily set, unless the WRITE CONTROL, LA=1 qualifications are present on the processor OUT-DATA lines.
TERM	AC2	FF	Terminates a receive mode. P/TERM=STO+(ETX+ETB+EOT)•$\overline{ISF}$
TERM/2	AC2	SIG	Output of the TERM flip-flop - causes the ACA to end the active recieve mode.
TRØ	AC1	SIG	State zero of the transmit mode.

TR1	AC1	SIG	An inverted output of the 1 position (decimal) of the transmit state decoder. All state decoders are binary-to-decimal conversions.
TR/2	AC1	SIG	Indicates that the ACA is in the transmit mode.
TR	AC1	DCDR	Binary-to-decimal decoder for the unique states within the transmit mode.
TRANS	AC2	FF	TRANSfer is cleared during the "handshake" procedure between the processor and the ACA. This can be for an interrupt transfer, or when the I/O select character is transfered. TRANS remains reset until the single data (or select) character transfer is complete, then it sets. When TRANS sets, the state counter is qualified to increment.
TSC OUT/3	AC2	SIG	Transmission Status Character Out. Used only if a transmission error is detected in the ISF READ configuration. TSC OUT=ERROR•TERM•ISF
TWO CHAR TERM	AC2	XL	Used in conjunction with the CHAR DCDR to indicate that a DLE has been received, and the end of the message has two characters (the DLE and a character following). Also used in the non-ISF case for ETX(BCC) or ETB(BCC) endings.
T/SI-REG	AC1	SIG	Loads the station identifier into the register. Under a READ CONTROL instruction, the first character is called from memory (through INT) because the device number (LA) is greater than zero. This character is installed in the SI (station identifier) register for later comparason with the first character of incoming data.
W/R OPREG	AC2	FF	WRITE/READ flip-flop. Set during a WRITE or WRITE CONTROL instruction, and reset during a READ or READ CONTROL instruction.

17-7.0 ACA ALGORITHMS

START

ENTRY	STATE	DESCRIPTION	REMARKS	EXIT
ST7 POWER ON	Ø	L/LA CNTR C/RDY	IF ST: C/RCH LOAD IOS•ONLINE+IOS-TO-MN•ONLINE•STATUS RDY+IOS-TO-MN•ONLINE•REC•$\overline{\text{TERM CH}}$	
	1	C/TRANS IF OP≠WRC: JUMP TO STATE 6	C/TRANS: CLEARS STATUS RDY	 ST 6
ID6	2	IF LA≠3: JUMP TO STATE 6 IF INT-REQ: INH-STATE		ST 6
	3	S/INTERRUPT C/DATA REG.		
	4	IF $\overline{\text{TRANS}}$: INH-STATE		
	5	L/STCODE C/TRANS IDLE -- MODE S/GDSTATUS C/STATE L/MODE(B)		 ID Ø
ST1	6	S/STATUSRDY C/IO BUSY IF $\overline{\text{TRANS}}$: INH-STATE	C/IO BUSY: C/LAST STATUSRDY IOS-TO-MN C/DATA REG.	
	7	C/STATE L/MODE(B) C/TRANS		 ST Ø

ASYNCHRONOUS COMMUNICATIONS ADAPTER

IDLE

ENTRY	STATE	DESCRIPTION	REMARKS	EXIT
ST 5 TR 3 ID 8 TR Ø REC Ø REC 7	Ø	C/TERM	C/TERM•TCLK: C/TWO CHAR TERM C/TERM FF	
	1	C/LAST C/IO BUSY S/STATUS RDY IF $\overline{\text{TRANS}}$: INH-STATE	S/STATUS RDY: C/LTO C/LO BIT FF STATUS RDY•IOS-TO-MN CLEARS DATA REG.	
	2	C/TRANS	C/TRANS: CLEARS STATUS RDY	
	3	IF $\overline{\text{TRANS}}$+IO BUSY: INH-STATE	LOAD IOS•ONLINE•$\overline{\text{IOBUSY}}$: L/OPREG L/LA CNTR	
	4			
	5	C/TRANS IF OP≠WRC: S/CCON JUMP TO STATE 8		ID 8
	6	S/GDSTATUS IF LA=3: JUMP TO START JUMP TO STATE 2 IF LA=2: S/HANGUP IF DIAL: INH-STATE		ST 2
	7	C/TRANS C/STATE IF LA=5,6,or 7: S/FLAG		
ID 5 TR 3 ID 12	8	C/DATA REG. IF INT REQ: INH-STATE IF LDREQ: C/STATE		ID Ø
	9	IF LOCKOUT: INH-STATE IF LTO: C/STO		
	10	IF TERM•(RD+RDC): GO TO REC JUMP TO STATE 6		REC 6

ASYNCHRONOUS COMMUNICATIONS ADAPTER

IDLE (Continued)

ENTRY	STATE	DESCRIPTION	REMARKS	EXIT
	11	IF LA=Ø: C/CCON IF (LA=Ø)•(RC+RDC): RECEIVE -- MODE C/STATE L/MODE(B) C/CA		REC Ø
	12	S/INTERRUPT IF $\overline{\text{TRANS}}$: INH-STATE		
	13	C/TRANS IF OP=RDC: L/SI REG. JUMP TO STATE 8 IF OP=$\overline{\text{RDC}}$: TRANSMIT -- MODE ENA CH DCDR IF LA≠Ø: DECREMENT LA	L/SI REG: S/MATCH C/CNTL	ID 8
	14	C/STATE L/MODE(B)		TR Ø

ASYNCHRONOUS COMMUNICATIONS ADAPTER

TRANSMIT

ENTRY	STATE	DESCRIPTION	REMARKS	EXIT
ID 14	Ø	PARITY BIT -- DATA REG. S/CA IF $\overline{CB \cdot CC}$: INH-STATE IF TIMEOUT: GO TO IDLE/Ø S/FAULT C/STATE C/TRANS	INITIALIZE MODEM STX,SOH: CLOCKS ENA-BCC BIT TO ENA-BCC FF ETX,ETB: C/ENA-BCC FF	ID Ø
TR 2	1	IDLE -- MODE IF $\overline{SHCOMP}$: INH-STATE	TRIGGER PAD TIMER IF LA=Ø THIS STATE ENABLES THE SHIFTING TIMING CIRCUIT.	
	2	IF PAD TIMER•(LAST+READ): INH-STATE BCC -- DATA REG IF BCC RDY: C/STATE IF BCC RDY•$\overline{\text{STATE CLK (B)}}$: C/RDY IF TEST CLK: C/DATA REG.	TRAILING EDGE OF SHCOMP CLOCKS ACC BCC TRAILING EDGE OF ACC BCC CLOCKS BCC RDY BCC -- DATA REG: C/SHCOMP PAD TIMER= 4.5msec.	TR Ø
	3	L/MODE (B) IF ACU LAST: C/STATE IF $\overline{\text{ACU LAST}}$: JUMP TO STATE 8		ID Ø ID 8

ASYNCHRONOUS COMMUNICATIONS ADAPTER

RECEIVE

ENTRY	STATE	DESCRIPTION	REMARKS	EXIT
ID 9	Ø	IF SHCOMP: INH-STATE IF LTO: S/FAULT C/TRANS C/STATE GO TO IDLE IF STO: S/TERM IF LAST•$\overline{\text{ISF}}$: JUMP TO STATE 6 IF TERM: ENA CH DCDR JUMP TO STATE 6 IF ENA CH DCDR•STATE: C/DATA REG	STARTING BIT ENABLES SHIFTING TIMING STX+SOH•$\overline{\text{ISF}}$: S/ENA-BCC FF ETX+ETB: C/ENA-BCC FF TRAILING EDGE OF SHCOMP CLOCKS ENA-BCC -- ACC-BCC IF REC: C/CA (RTS) S/RCH IF SHCOMP•TCLK: L/BUFFER	ID Ø REC 6
	1	L/BUFFER IF ISF: C/STATE, T/LTO IF $\overline{\text{ISF}}$•$\overline{\text{MATCH}}$: JUMP TO S3 IF $\overline{\text{ISF}}$•TWO CHAR TERM: S/TERM	IF BCC RDY: C/RDY IF BUFFER IS LOADED: C/SHCOMP	REC Ø REC 3
	2	IF $\overline{\text{MATCH OK}}$: C/STATE IF MATCH OK: C/MATCH		REC Ø
REC 1	3	ENA CH DCDR IF LAST: JUMP TO STATE 6	STX+SOH•$\overline{\text{ISF}}$: S/ENA-BCC FF ETX+ETB: C/ENA-BCC FF	REC 6
	4	C/DATA IF TERM: JUMP TO STATE 6		REC 6
	5	C/STATE		REC Ø
ID 4	6	IDLE -- MODE IF INT+B8•$\overline{\text{LAST}}$: INH-STATE IF LAST: INH INT, S/FLAG IF TERM•TCLK: C/TERM	IF TSC OUT•TERM: BCC -- DATA IF ERROR•TERM•ISF: TSC OUT	
	7	C/TRANS C/STATE C/DATA REG. C/BCC L/MODE (B) C/BUFFER C/OUTPUT		ID Ø

REFERENCE

SECTION CONTENTS

BITS b7 b6 b5 →					0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b4	b3	b2	b1	Column / Row	0	1	2	3	4	5	6	7
0	0	0	0	0	NUL	DLE	SP	0	@	P	'	p
0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
0	0	1	0	2	STX	DC2	"	2	B	R	b	r
0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
0	1	1	1	7	BEL	ETB	'	7	G	W	g	w
1	0	0	0	8	BS	CAN	(	8	H	X	h	x
1	0	0	1	9	HT	EM	)	9	I	Y	i	y
1	0	1	0	10	LF	SUB	*	:	J	Z	j	z
1	0	1	1	11	VT	ESC	+	;	K	[	k	{
1	1	0	0	12	FF	FS	,	<	L	\	l	¦
1	1	0	1	13	CR	GS	-	=	M	]	m	}
1	1	1	0	14	SO	RS	.	>	N	^	n	~
1	1	1	1	15	SI	US	/	?	O	_	o	DEL

D-832

USASCII CODE CHART

FIGURE A-1

A. USASCII CODE

1. CONTROL CHARACTERS

NUL	Null
SOH	Start of Heading (CC)
STX	Start of Text (CC)
ETX	End of Text (CC)
EOT	End of Transmission (CC)
ENQ	Enquiry (CC)
ACK	Acknowledge (CC)
BEL	Bell (audible or attention signal)
BS	Backspace (FE)
HT	Horizontal Tabulation (punched card skip) (FE)
LF	Line Feed (FE)
VT	Vertical Tabulation (FE)
FF	Form Feed (FE)
CR	Carriage Return (FE)
SO	Shift Out
SI	Shift In
DLE	Data Link Escape (CC)
DC1	Device Control 1
DC2	Device Control 2
DC3	Device Control 3
DC4	Device Control 4 (Stop)
NAK	Negative Acknowledge (CC)
SYN	Synchronous Idle (CC)
ETB	End of Transmission Block (CC)
CAN	Cancel
EM	End of Medium
SUB	Substitute
ESC	Escape
FS	File Separator (IS)
GS	Group Separator (IS)
RS	Record Separator (IS)
US	Unit Separator (IS)
DEL	Delete

NOTE: (CC) Communication Control
(FE) Format Effector
(IS) Information Separator

2. GRAPHIC CHARACTERS

Column/Row	Symbol	Name
2/0	SP	Space (Normally Non-Printing)
2/1	!	Exclamation Point
2/2	"	Quotation Marks
2/3	#	Number Sign
2/4	$	Dollar Sign
2/5	%	Percent
2/6	&	Ampersand
2/7	'	Apostrophe (Closing Single Quotation Mark)
2/8	(	Opening Parenthesis
2/9	)	Closing Parenthesis
2/10	*	Asterisk
2/11	+	Plus
2/12	,	Comma
2/13	-	Hyphen (Minus)
2/14	.	Period (Decimal Point)
2/15	/	Slant
3/10	:	Colon
3/11	;	Semicolon
3/12	<	Less Than
3/13	=	Equals
3/14	>	Greater Than
3/15	?	Question Mark
4/0	@	Commercial At
5/11	[	Opening Bracket
5/12	\	Reverse Slant
5/13	]	Closing Bracket
5/14	^	Circumflex
5/15	_	Underline
6/0	`	Grave Accent (Opening Single Quotation Mark)
7/11	{	Opening Brace
7/12	|	Vertical Line
7/13	}	Closing Brace
7/14	~	Overline (Tilde, General Accent)

3. DEFINITIONS

a. GENERAL

(CC) COMMUNICATION CONTROL: A functional character intended to control or facilitate transmission of information over communication networks.

(FE) FORMAT EFFECTOR: A functional character which controls the layout or positioning of information in printing or display devices.

(IS) INFORMATION SEPARATOR: A character which is used to separate and qualify information in a logical sense. There is a group of four such characters, which are to be used in a hierarchical order.

b. CONTROL CHARACTERS

NUL (Null): The all-zeros character which may serve to accomplish time fill and media fill.

SOH (Start of Heading): A communication control character used at the beginning of a sequence of characters which constitute a machine-sensible address or routing information. Such a sequence is referred to as the "heading". An STX character has the effect of terminating a heading.

STX (Start of Text): A communication control character which precedes a sequence of characters that is to be treated as an entity and entirely transmitted through to the ultimate destination. Such a sequence is referred to as "text". STX may be used to terminate a sequence of characters started by SOH.

ETX (End of Text): A communication control character used to terminate a sequence of characters started with STX and transmitted as an entity.

EOT (End of Transmission): A communication control character used to indicate the conclusion of a transmission, which may have contained one or more texts and any associated headings.

ENQ (Enquiry): A communication control character used in data communication systems as a request for a response from a remote station. It may be used as a "Who Are You" (WRU) to obtain station status, or both.

BEL (Bell): A character for use when there is a need to call for human attention. It may control alarm or attention devices.

BS (Backspace): A format effector which controls the movement of the printing position one printing space backward on the same printing line. (Applicable also to display devices.)

HT (Horizontal Tabulation): A format effector which controls the movement of the printing position to the next in a series of predetermined positions along the printing line. (Applicable also to display devices and the skip function on punched cards.)

LF (Line Feed): A format effector which controls the movement of the printing position to the next printing line. (Applicable also to display devices.) Where appropriate, this character may have the meaning "New Line" (NL), a format effector which controls the movement of the printing point to the first printing position on the next printing line. Use of this convention requires agreement between sender and recipient of data.

VT (Vertical Tabulation): A format effector which controls the movement of the printing position to the next in a series of predetermined printing lines. (Applicable also to display devices.)

FF (Form Feed): A format effector which controls the movement of the printing position to the first predetermined printing line on the next form or page. (Applicable also to display devices.)

CR (Carriage Return): A format effector which controls the movement of the printing position to the first printing position on the same printing line. (Applicable also to display devices.)

SO (Shift Out): A control character indicating that the code combinations which follow shall be interpreted as outside of the character set of the standard code table until a Shift In character is reached.

SI (Shift In): A control character indicating that the code combinations which follow shall be interpreted according to the standard code table.

DLE (Data Link Escape): A communication control character which will change the meaning of a limited number of contiguously following characters. It is used exclusively to provide supplementary controls in data communication networks.

DC1, DC2, DC3, DC4 (Device Controls): Characters for the control of ancillary devices associated with data processing or telecommunication systems, more especially switching devices "on" or "off". (If a single "stop" control is required to interrupt or turn off ancillary devices, DC4 is the preferred assignment.)

NAK (Negative Acknowledge): A communication control character transmitted by a receiver as a negative response to the sender.

SYN (Synchronous Idle): A communication control character used by a synchronous transmission system in the absence of any other character to provide a signal from which synchronism may be achieved or retained.

ETB (End of Transmission Block): A communication control character used to indicate the end of a block of data for communication purposes. ETB is used for blocking data where the block structure is not necessarily related to the processing format.

CAN (Cancel): A control character used to indicate that the data with which it is sent is in error and is to be disregarded.

EM (End of Medium): A control character associated with the sent data which may be used to identify the physical end of the medium, or the end of the used or wanted portion of information recorded on a medium. (The position of this character does not necessarily correspond to the physical end of the medium.)

SUB (Substitute): A character that may be substituted for a character which is determined to be invalid or in error.

ESC (Escape): A control character intended to provide code extension (supplementary characters) in general information interchange. The Escape character itself is a prefix affecting the interpretation of a limited number of contiguously following characters.

FS (File Separator), GS (Group Separator), RS (Record Separator). and US (Unit Separator): These information separators may be used within data in optional fashion, except that their hierarchical relationship shall be: FS is the most inclusive, then GS, then RS, and US is least inclusive. (The content and length of a File, Group, Record, or Unit are not specified.)

DEL (Delete): This character is used primarily to "erase" or "obliterate" erroneous or unwanted characters in perforated tape. (In the strict sense, DEL is not a control character.)

B. GLOSSARY

1. TERMS

ACU	Arithmetic and Control Unit. Equivalent to what is called the Central Processing Unit in most computers.
Active	"Active" is the term used to refer to the user, his IOC, or his partition in the Main Memory, whose program is being executed by the ACU at a given moment.
BCD	Binary Coded Decimal. Four bits are necessary and sufficient to represent each of the decimal digits 0 through 9 in binary; hence an n-digit decimal number is represented in BCD by n groups of four bits. For example, 14 is 0001 0100 in BCD.
Character	One alpha, numeric, or special symbol, however coded. In the memory, six bits; in USASCII, seven bits.
Common Area	The low-order portion of Main Memory. Common Area size is determined by patching in the ACU, and can be from 1K to 10K, in increments of 1K. Includes Protected Area and Privileged Area.
FAC	File Access Channel. Parallel interface connecting the ACU with the memory file controllers.
FF	Flip-Flop.
Field	One or more contiguous characters in memory used to represent a specific category of data. A field may contain one or more words.
IOC	Input/Output Controller.
LSD	Least Significant (right-most) Digit.
LU	Line Unit.
MM	Main Memory.
MSD	Most Significant (left-most) Digit other than zero.
Partition	A division of the Main Memory. The memory is not physically partitioned, but the hardware controls the addressing of the entire memory in such a way that the memory can be thought of as being partitioned. One of the partitions is called the Common Area; the rest, numbered from 0 through 19, are each reserved exclusively for one user. This term is also used to refer collectively to a Main Memory partition, its associated IOC, and its possible peripheral units.

Peripheral	An input/output device connected to the ACU via an IO channel.
Privileged Area	The high-order portion of the Common Area. Only privileged users may read or write within this area, where "privileged user" is defined by a signal wire from the IOC. The lower limit address of the Privileged Area is selected by jumpers in the ACU and may be from 0 to 9K, in increments of 1K.
Processor	That which processes. In this case, that which electronically processes data, e.g., the Central Processing Unit. To avoid confusion, the word processor is not assigned a specific meaning in this publication nor is it used in place of any other specifically defined term.
Protected Area	The lower order 300 positions of the Common Area. This area is protected by the hardware against being written into by program. The hardware requires the data in this area in order to operate on a time-shared basis.
User	One who utilizes the ACU at the system level. Thus a user has at his disposal: 1. One partition for his exclusive use. 2. One I/O channel for his exclusive use. 3. Access to the Common Area. 4. Up to ten I/O devices. 5. Possible use of the memory file. 6. All processing capability of the ACU on a time-shared basis. 7. Possible use of the Privileged Area.
Word	One or more contiguous alpha/numeric characters, which, when taken together, form an entity.

2. SIGNAL NAME

a. ARITHMETIC/CONTROL UNIT (ACU) MODULE

SIGNAL NAME	TYPE	SOURCE	DEFINITION
A-DECR/3	G	LRW,LDA, LAR	A-DECREMENT causes the count in the A Register to be reduced by 1. The trailing edge of the signal initiates the decrement.
A-INCR/3	G	LRW,LDA, LAR	A-INCREMENT causes the count in the A Register to be increased by 1. The trailing edge of the signal initiates the increment.
A-OUT/3	G	LRW,LIF, LDA,LAR	A-OUT causes the contents of the A register to be gated onto the R-BUS for addressing main memory.
ACK/1 ACK/3	DFF G	TMN DAG,TC1 OC2	ACKNOWLEDGE is a signal generated by an FAC control device in response to select signals from the ACU.
ACTIVE-TO-S/4	G	LRW	ACTIVE-TO-S gates onto the S-BUS those bits of LB and the function code that are needed to make up the B4 digit (ACTIVE, NON-FILL, CONTROL, FUNCtion).
ACU-LD-REQ/2	DFF	LIF	ACU-LOAD-REQUEST flip-flop is enabled by LOAD-REQ/3 and is toggled by SCB-STR/1. The output signal indicates that the active partition requests to enter one 10-character instruction commencing at 0000 relative address.
ACU-SV-REQ/2	DFF	LIF	ACU-SERVICE-REQUEST flip-flop is enabled by SERV-REQ/3 and toggled by SCB-STR/1. The output signal indicates that the active partition's program or operator has initiated a service request.
ADD-GR-300/4	G	RAD	ADDRESS-GREATER-THAN-300 signal indicates that the address on the R-BUS $\geq$ 300, or that X-OUT signal is present.
ADDER-TO-S/3	G	LDA,LAR, LIF	ADDER-TO-S signal gates the output of the arithmetic adder onto the S-BUS.
ADR-ERR/2	G	TMN	ADDRESS-ERROR signal indicates that the relative address on the R-BUS is in error for one of the following reasons: R-BUS number exceeds partition limit (P-LIM), R-BUS number exceeds common area limit, R-BUS number addresses privileged area (Not a priviledged user), or R-BUS number identifies protected area for a Read instruction.

SIGNAL NAME	TYPE	SOURCE	DEFINITION
ADR-INH/3	G	TST	ADDRESS-INHIBIT is a test signal that prevents adding the base address to the relative address so that the relative address may be observed on the test panel.
B-DECR/3	G	LRW,LDA, LAR	B-DECREMENT causes the count in the B Register to be reduced by 1. The trailing edge of the signal initiates the decrement.
B-INCR/3	G	LRW,LDA, LAR	B-INCREMENT causes the count in the B Register be increased by 1. The trailing edge of the signal initiates the increment.
B-OUT/3	G	LRW,LIF, LDA,LAR	B-OUT causes the contents of the B Register to be gated onto the R-BUS for addressing main memory.
BORROW/4	G	RAD	BORROW signal indicates that the number in the A or B Register is 0000 and that the A-DECR/3 or B-DECR/3 signal is present. When the decrement signal is removed, the count changes to 9999.
BR-OK/4	G	RDA	BRANCH-OK signal is produced when the conditions satisfy the branch variants (LA and/or LB).
C/CARRY/3	G	LDA,LAR	CLEAR-CARRY signal resets the CARRY flip-flop (one of the three condition flip-flops).
C/CONDS/1	DEC	LIF	CLEAR-CONDITION Signal presets NORMAL (EQUAL) condition: The ZERO FF is set; MINUS and CARRY FFs are reset. This signal is generated before the ACU commences the execute any instruction other than Branch.
C/D/4	G	LAR	CLEAR-D signal resets the D Register.
C/DH/3	G	LRW,LIF	CLEAR-DH resets both the D and H Registers.
C/E/4	G	LDA	CLEAR-E signal resets the E Register.
C/F/3	G	TST,LIF	CLEAR-F signal resets the F (function) Register and index registers IA and IB. This signal also loads the base address of the active partition into the Z Registers in the base adder.
C/F2/3	G	LDA,LAR	CLEAR-F2 signal resets the flip-flop where the F2 bit of the function code is stored.
C/F3/3	G	LDA	CLEAR-F3 signal resets the flip-flop where the F3 bit of the function code is stored.

SIGNAL NAME	TYPE	SOURCE	DEFINITION
C/H/4	G	LAR	CLEAR-H signal clears the H Register.
C/IA/3	G	LIF	CLEAR-IA signal clears the IA index register: IAØ and IA1.
C/INT/1	G	LRW	CLEAR-INTERRUPT signal resets the INTERRUPT FF in the active IOC.
C/K/3	G	LDA,LAR	CLEAR-K signal resets the K Register (located in the TMN card).
C/LD-REQ/1	G	LRW	CLEAR-LOAD-REQUEST signal resets the active IOC's LDRQ FF.
C/M/3	G	LRW,LDA	CLEAR-M signal resets the M Register (memory buffer) flip-flops M1, M2, M3, and M4.
C/MINUS/3	G	LDA	CLEAR-MINUS signal resets the MINUS flip-flop (one of the three condition FFs).
C/P/3	G	LIF	CLEAR-P signal resets the P (hardware) Register. This signal also resets the A, J, and LA Registers, resets BØ, B2, B3 flip-flops, loads B1 flip-flop, and K and LB Registers, and sets condition flip-flops to normal or equal condition.
C/SERV-REQ/1	G	LDA	CLEAR-SERVICE-REQUEST signal resets the active IOC's SVRQ FF.
C/SUB/3	G	LIF,LAR	CLEAR-SUBTRACT signal resets the SUBTRACT and the CARRY flip-flops.
C/TIMEOUT/2	G	LRW	CLEAR-TIMEOUT signal resets the 37.5-ms Timeout circuit. If the TIMEOUT FF is set, this signal resets it.
C/ZERO/3	G DEC	LDA LAR	CLEAR-ZERO signal resets the ZERO flip-flop (one of the condition flip-flops).
CARRY/1	DFF	RDA	CARRY signal is used during arithmetic operations and as storage for the "Repeat-if-error" bit of a Read instruction. In Add operations, the CARRY flip-flop is set when the sum of two digits is greater than nine. In Subtract operations, the CARRY flip-flop is set first, and is cleared when the difference is less than zero (borrow).

SIGNAL NAME	TYPE	SOURCE	DEFINITION
CHECK/3	G	CH1,CH3, CH5,IO1, CL3	CHECK signal is produced by a flip-flop in the active IOC when an address error, invalid function (op) code, or detectable data fault occurs. When this signal is present it causes the address in the P hardware register to be stored in location 40 and initiates a Read Control (Load).
CLK-IN/6	G	TMN or External oscillator	CLOCK-IN is the master clock input from which all timing signals within the processor are derived. This signal is usually obtained from CLK-OUT/6.
CLK-OUT/6	G	TMN	CLOCK-OUT is a 9 MHz oscillator output that is normally applied to CLK-IN/6 by a jumper between TP7 and TP8.
CLOCK/4	G	CH2	CLOCK is a signal produced by a flip-flop in the IOC when the IOC receives a clock pulse from the line unit.
CM-CLK/6	G	TMN	CORE-MEMORY-CLOCK is a 9-MHz oscillator output identical to CLK-OUT/6. CM-CLK/6 provides the basic memory timing signal to the MTM circuit card.
CM-CYCLE/1	G	TMN	CORE-MEMORY-CYCLE is the signal that enables one core memory cycle (Read or Write one character).
CM-READ/1	G	TMN	CORE-MEMORY-READ signal determines whether the core memory cycle operation is Read (Logic 0) or Write (logic 1).
COMP-EQ/4	G	RDA	COMPARE EQUAL signal is logic 1 at the start of a Compare operation, and changes to logic 0 if any difference is detected between the two fields being compared.
CONDS-TO-S/2	G	LRW	CONDITIONS-TO-S signal, together with the Q counter outputs, gates the settings of the condition flip-flops onto the S-BUS. CARRY is gated out when Q=1; MINUS, when Q=2; and ZERO, when Q=3. This signal also enables L/N for gating the conditions into the N Register (N2), and P-OUT signal which sortes the contents of the P register in main memory.
COUNT-PC/4	G	CH1	COUNT-POLL-COUNTER is a signal that causes the poll count within an IOC to be incremented.

SIGNAL NAME	TYPE	SOURCE	DEFINITION
CR/2	G	TMN	CYCLE-REQUEST is a flip-flop signal that causes normal ACU processing to be suspended while an FAC main memory cycle is in progress. The CR FF is clocked at the end of state time.
CYCLE-REQ/3	G	DDJ,TC1, OC2	CYCLE-REQUEST is a signal from the FAC that informs the ACU of an imminent FAC main memory cycle. At the end of the next STATE TIME this signal causes the CR flip-flop to set.
DATA-FAULT/4	G	TMN	DATA-FAULT signal is produced if the instruction character retrieved from core contains a binary value greater than nine in the lower four bits, or if the 5-bit is not logic 1.
DATA/4	G	CH2	DATA is a flip-flop signal from the IOC. This signal is produced each time the IOC detects a data transition on the 2-wire line from the line unit to the IOC.
DIS-SEL-3/9 DIS-SEL-4/9 DIS-SEL-5/9 DIS-SEL-6/9 DIS-SEL-7/9 DIS-SEL-8/9	SW	TST	DISPLAY-SELECT signals originated in Test Panel switches and connect through the TST card to the motherboard. These signals gate selected register outputs onto the S-BUS.
DISPLAY-E/3	G	TST	DISPLAY-E develops the E-TO-S signal for gating the states contents of the E1 & E2 flip-flops onto the S BUS for display on the Test Panel. (The condition of the E Register is not set into the N Register.)
D2/3	G	RDA	D2 is the binary 2 output of the D Counter. It is produced in INTERRUPT state when all 20 IOCs have been checked for an interrupt request.
E-TO-S/3	G	LRW,LDA, LAR	E-TO-S signal gates the states of the E1 and E2 flip-flops onto the S-BUS for entry into the N Register.
EN-COMP/1	DEC	LDA	ENABLE-COMPARE signal gates the resetting of the EN-COMP FF, which enables selected gates used in the COMPARE function.
EN-CR/3	G	LIF	ENABLE-CYCLE REQUEST signal is developed in INTERRUPT state during FAC instructions to allow the FAC to set the CR FF.

SIGNAL NAME	TYPE	SOURCE	DEFINITION
EN-IOC-LMP/6	G	TST	ENABLE-IOC-LAMPS is developed when the Mode Select switch on the Test Panel is in any position other than "Normal." This signal and IO-BUSY lights a lamp on CH2 card of the active IOC.
EN-STOP/4	G	TST	ENABLE-STOP is a Test Panel signal that sets the STOP FF at the end of STATE-TIME. The STOP FF inhibits the STATE-CLOCK to stop normal processing.
EN-300-ACC/3	G	RAD	ENABLE-300-ACCESS is generated when the R-BUS address is 0300 or greater, or when the address is in the user's partition.
ESCAPE/3	G	CH1	ESCAPE is the IOC mode from which all operations start.
F=BRANCH/3	G	RBA	FUNCTION=BRANCH signal is produced when the F Register contains the code for a Branch instruction (1011).
FAC-CLK/2	G	TMN	FAC-CLOCK is a continuous 900 KHz clock that is in phase with the ACU clock.
FAC-DATA-1/3 FAC-DATA-2/3 FAC-DATA-3/3 FAC-DATA-4/3 FAC-DATA-5/3 FAC-DATA-6/3	G	DDJ,TC2, OC2	FAC-DATA signals from the FAC module enter the ACU through the TST card. The FAC-TO-S signal gates FAC-DATA from TST card onto the S-BUS.
FAC-INH/3	G	RDA	FAC-INHIBIT prevents the ACU from executing an FAC instruction as directed by the "A4" character. The ACU procedure to the next sequential instruction.
FAC-SELECT/3	G	LRW	FAC-SELECT, with FAC-STROBE, selects the FAC device corresponding to the address on the OUT-DATA lines and deselects the previously used device.
FAC-STROBE/1	G	TMN	FAC-STROBE gates data form the OUT-DATA lines into the selected FAC device and causes the device to advance to the next sequential step or state.
FAC-TO-S/2 FAC-TO-S/3	G T	TMN LRW	FAC-TO-S gates the information on the FAC-DATA lines onto the S-BUS for entry into the M and N registers.

SIGNAL NAME	TYPE	SOURCE	DEFINITION
FCB-H/1	G	LIF	FUNCTION COUNTER BUFFER-HIGH denotes that the FCB contains a count between 8 and 15.
FCB-L/1	G	LIF	FUNCTION COUNTER BUFFER-LOW denotes that the FCB contains a count between Ø and 7.
FCB-1/2 FCB-2/2 FCB-3/2 FCB-4/2	CTR	LIF	FUNCTION COUNTER BUFFER outputs supply the number stored in the Function Counter to the various function decoders and state decoders.
FUNC-INCR/3	G	TST,LRW	FUNCTION-INCREMENT causes the number stored in the Function Counter to be increased by 1. The increment occurs only in RW15 or when it is initiated by the Test Panel.
F0/6 F1/6 F2/6 F3/6	G	RBA	F register outputs, representing the Function code (Op code).
GND			Ground.
IA-OUT/1	DEC	LIF	IA-OUT signal gates the contents of the IA Index Address Register (IA1 & IA0) onto the 10s of the R-BUS.
IAZ/3	G	RBA	IA ZERO indicates that the IA0 and IA1 flip-flops are reset, so that the A Address will not be indexed.
IB-OUT/1	DEC	LIF	IB-OUT signal gates the contents of the B Index Address Register (IB1 & IB0) onto the 10s line of the R-BUS.
IBZ/3	G	RBA	IB ZERO indicates that the IB0 and IB1 flip-flops are reset, so that the B Address will not be indexed.
INH-INP/3	G	CH1	INHIBIT-INPUT is a signal in the IOC which causes the IOC to send NULs or "blanks" to the ACU.
INH-INSTR/2	DFF	TST	INHIBIT-INSTRUCTION is a test panel signal that causes the ACU to switch partitions whenever it attempts to retrieve a new instruction.
INH-SW/1	DFF	TST	INHIBIT-SWITCH is a Test Panel signal that prevents incrementing the partition counter in SWITCH; all other actions that are a part of SWITCH take place. It also permits writing into the protected area of Main Memory.

SIGNAL NAME	TYPE	SOURCE	DEFINITION
INH-TO/3	G	CH3,IO1, CL3	INHIBIT-TIMEOUT is an IOC signal that prevents setting the TIMEOUT FF. It is produced enabled by a jumper on the IOC.
INP-DATA-1/3 INP-DATA-2/3 INP-DATA-3/3 INP-DATA-4/3 INP-DATA-5/3 INP-DATA-7/3	G	CH2,MTM, CH4,CH6, IO2,CL4	INPUT-DATA lines carry the 6-bit input characters to the ACU from the active IOC or from Main Memory.
INST-STOP/3	G	LIF	INSTRUCTION-STOP is a signal developed by the ACU which causes ACU operation to stop after retrieval of each instruction when the Test Panel is in the STOP ON INSTR mode.
INTERRUPT/3	G	CL3	INTERRUPT is an FF signal from the IOC that the IOC is ready for a character transfer between the ACU and the IOC.
INT-REQ/3	G	CH1,CH3, CH5,IO1, CL3	INTERRUPT REQUEST is developed in the IOC when its INTERR FF is set, and the IOC is selected (INTERRUPT/3·ON-LINE/4→INT-REQ/3).
IO-BUSY/2 IO-BUSY/3	DFF G	CH1,CH3, CH5,IO1, CL3	IO-BUSY is an FF from the IOC that indicates that the channel is engaged in an I/O operation.
IO-SEL/2	G	RBA	IO-SELECTED that the position designated by the X Counter does, in fact, have an IOC connected, and that this IOC specifies a partition size of not greater than 11K.
IOC-DATA-6/2	G	TMN	IOC-DATA-6 is the 6-bit of the output character from the ACU to the IOC. It is always the inverse of the N2 FF condition.
IOC-DATA-7/2	G	TMN	IOC-DATA-7 is the 7-bit of the output character from the ACU to the IOC. It is the same logic state as the N2 FF for normal WRITE, but is always a logic 0 for WRITE control.
IOC-HF-CLK/2	G	TMN	IOC-HIGH FREQUENCY-CLOCK is a 450 KHz clock that provides the basic timing for several types of IOCs.
IOC-LF-CLK/2	G	TMN	IOC-LOW FREQUENCY-CLOCK is a 45 KHz clock that provides timing signals for some types of IOCs.
IOC-MF-CLK/2	G	TMN	IOC-MEDIUM FREQUENCY-CLOCK is a 300 KHz clock that provides timing signals for some types of IOCs.

SIGNAL NAME	TYPE	SOURCE	DEFINITION
IOF-TO-S/4	G	LRW	I/O FUNCTION-TO-S signal gates the I/O "Select" character onto the S-BUS for transmission to the IOC.
IOS-TO-MN/1	G	LRW	IOS-TO-M and N gates one character (data or status) from the IOS shift register in the IOC onto the S-BUS for entry into the M and N Registers.
IOSDEC/3	G	CH2	IOS-DELETE signal is produced when the IOS shift register in the IOC contains the USASCII Delete code.
IOSUS/3	G	CH2	IOS-UNIT SEPARATOR signal is produced when the IOS shift register in the IOC contains the USASCII Unit Separator code.
ITA/1	G	MTM	INHIBIT TIME A is a memory timing signal that enables the inhibit switches serving half of the memory cores in each bit "plane".
ITB/1	G	MTM	INHIBIT TIME B is a memory timing signal that enables the inhibit switches serving the half of the memory cores in each bit "plane" that are not enabled by ITA.
J/BEGIN/3	G	LRW,LDA, LAR	JUMP TO BEGIN sets the code for the BEGIN function (1010) into the Function Counter.
J/DIVIDE/3	G	LAR	JUMP TO DIVIDE sets the code for the DIVIDE function (0101) into the Function Counter.
J/INTERRUPT/3	G	LRW	JUMP TO INTERRUPT sets the code for the INTERRUPT function (0010) into the Function Counter.
J/MULT/3	G	LAR	JUMP TO MULTIPLY sets the code for the MULTIPLY function (0110) into the Function Counter.
J/STEP-0/3	G	LDA,LAR	JUMP TO STEP-(0-14) sets the code for the corresponding step into the Step Counter.
J/STEP-1/3	G	LDA,LAR	
J/STEP-3/3	G	LDA	
J/STEP-4/3	G	LRW,LDA,LAR	
J/STEP-5/3	G	LRW,LAR	
J/STEP-6/3	G	LRW,LDA,LAR	
J/STEP-7/3	G	LAR	
J/STEP-10/3	G	LRW,LAR	
J/STEP-12/3	G	LAR	
J/STEP-14/3	G	LAR	
J/SWITCH/3	G	LRW,LDA	JUMP TO SWITCH sets the code for the SWITCH function (0011) into the Function Counter.

SIGNAL NAME	TYPE	SOURCE	DEFINITION
JK-IOS/4	G	CH1	JK-IOS is the serial data input to the IOS shift register. It is the result of the LU-caused transitions sensed by the IOC on the 2-wire transmission line.
J-TO-S/3	G	LRW,LDA, LAR	J-TO-S gates the count in the J Counter onto the S-BUS and into the M Register.
JUMP/2	DFF	CH2	JUMP is a flip-flop signal from the IOC that signifies when the IOC State Counter is ready to jump to a different state.
J1/2	DCTR	TMN	J1 is the 1-bit output of the J Counter. It holds the 1 bit of the B4 character while in INTERRUPT, to show whether the I/O function in progress is a READ ($\overline{J1}$) or a WRITE (J1).
J3-TERM-RD/3	G	TMN	J3-TEMRINATE-READ signal is a combination of TERM-READ and the "non-fill" bit (bit 3 of the B4 character) stored in J3. It intiates immediate termination of a READ function.
K-DECR/3	G	LAR	K-DECREMENT signal causes the count in the K Counter to be reduced by 1. The trailing edge of the signal initiates the decrement.
K-INCR/3	G	LAR	K-INCREMENT signal causes the count in the K Counter to be increased by 1. The trailing edge of the signal initiates the increment.
K-TO-S/3	G	LRW,LDA, LAR	K-TO-S signal gates the number stored in the K Counter onto the S-BUS for entering into the M Register.
K1/3	G	TMN	K1 is the "1" bit output of the K Counter. It holds the 1 bit of the LB digit in READ/WRITE, denoting whether the READ/WRITE function being performed is I/O (K1) or FAC ($\overline{K1}$).
L/A/3	G	LRW,LIF, LDA	LOAD A signal and the Q Counter outputs causes the code in the M Register to be entered into the A Register.
L/B/4	G	LIF	LOAD B signal and the Q Counter outputs causes the code in the M Register to be entered into the B Register.
L/B2/3	G	LRW	LOAD B2 signal is used in disc instructions to automatically set the B address to 0100 (B2 set and B0, B1, and B3 reset).

SIGNAL NAME	TYPE	SOURCE	DEFINITION
L/CONDS/2	G	LRW	LOAD CONDITIONS signal and the Q Counter outputs enter the state of the N2 FF into the status indicator flip-flops (ZERO, MINUS, & CARRY). The information is derived from the P Address portion of the protected area of core.
L/D/3	G	LIF,LDA, LAR	LOAD D causes the code in the M Register to be entered into the D Register.
L/E/3	G	LRW,LDA, LAR	LOAD E causes the states of the N1 and N2 flip-flops to be entered into the E1 and E2 flip-flops, respectively.
L/F/2	G	LIF	LOAD F signal and the Q Counter outputs enter function code from the N2 FF into the F Register. The information is obtained from the function b bits in the instruction being retrieved from main memory.
L/H/3	G	LIF,LDA, LAR	LOAD H causes the code stored in the M Register to be entered into the H Counter.
L/I/2	G	LIF	LOAD I signal and the Q Counter outputs enter the index code from the N2 FF into the IA and IB Registers. The information is derived from the indexing bits in the instruction being retrieved from main memory.
L/J/3	G	RDA,LRW	LOAD J causes the code in the M Register to be entered into the J Register.
L/K/3	G	RDA,LRW, LDA,LAR	LOAD K causes the code in the M Register to be entered into the K Register.
L/LA/3	G	LDA,LAR	LOAD LA causes the code in the M Register to be entered into the LA Register.
L/LB/3	G	LDA,LAR	LOAD LB causes the code in the M Register to be entered into the LB Register.

SIGNAL NAME	TYPE	SOURCE	DEFINITION
L/M/3 L/M/6	G G	TST,RAD RDA	LOAD M signal enters the code on the four least significant lines of the S-BUS into the M Register. It is generated by the Test Panel and by the following signals: ACTIVE-TO-S ADDER-TO-S FAC-TO-S IOS-TO-MN PCTR-TO-M R-TO-S X-TO-S (J-TO-S and K-TO-S also load M, but do not develop L/M.)
L/N/3 L/N/6	G G	TST,RAD, LDA RDA	LOAD N signal enter the data on the two most significant lines of the S-BUS into the N Register. It is generated by the Test Panel and by the following signals: CONDS-TO-S E-TO-S FAC-TO-S IOF-TO-S IOS-TO-MN R-TO-S X-TO-S
L/P/3	G	LRW,LDA	LOAD P signal and the Q Counter outputs enter the contents of the M Register into the P Register.
LA-DECR/3	G	LDA,LAR	LA-DECREMENT causes the count in the LA Counter to be reduced by 1. The trailing edge of the signal initiates the decrement.
LA=0/1	DEC	RDA	LA=0 indicates that the LA Counter is clear.
LA=1/1	DEC	RDA	LA=1 indicates that the LA Counter contains a binary count of 1.
LA=6/1	DEC	RDA	LA=6 indicates that the LA Counter contains a binary count of 6.
LA=7/1	DEC	RDA	LA=7 indicates that the LA Counter contains a binary count of 7.
LATCH/3 LATCH/4	G	CH2	LATCH is a flip-flop signal generated in the IOC to allow only one reset of the Time Counter in any one state of the State Counter.

SIGNAL NAME	TYPE	SOURCE	DEFINITION
LB/DECR/3	G	LDA,LAR	LB-DECREMENT causes the count in the LB Counter to be reduced by 1. The trailing edge of the signal initiates the decrement.
LB=0/1	G	RDA	LB=0 indicates that the LB Counter is clear.
LB=1/1	DEC	RDA	LB=1 indicates that the LB Counter contains a binary count of 1.
LB=8/1	DEC	RDA	LB=8 indicates that the LB Counter contains a binary count of 8.
L-CLK/8		P.S.#1	LINE-CLOCK is a 60 Hz square wave produced by the power supply for use by the Digital Clock.
LIM-ERR/2	ADD	RBA	LIMIT-ERROR signal results when the relative address on the R-BUS exceeds the limit assigned to the selected partition or common area. It is also generated if a non-privileged user attempts to address privileged area. It inhibits memory cycles and develops ADR-ERR/2.
LOAD-BASE/3	G	LRW	LOAD-BASE is derived from System Reset, but has a faster rise time, permitting the base address to be properly loaded into the base adder.
LOAD-FAC/4	G	LRW	LOAD-FAC causes 3.0 μsec STATE-TIMEs whether or not core memory cycles are occurring, and develops FAC-STROBE.
LOAD-IOS/1	G	LRW	LOAD-IOS provides the single clock pulse necessary to enter the code from the OUT-DATA lines into the IOS shift register of the active IOC.
LOAD-REQ/3	G	CH1,CH3, CH5,IO1, CL3	LOAD-REQUEST informs the ACU that the active IOC requests to enter one 10-character instruction into address 0000 of its parition.
LONG-CYCLE/3	G	LRW	LONG-CYCLE extends STATE-TIME to 3.0 μsec without requiring a memory cycle.
MEM-DATA-1/3 MEM-DATA-2/3 MEM-DATA-3/3 MEM-DATA-4/3 MEM-DATA-5/3 MEM-DATA-7/3	SENSE AMP	MDG	MEMORY-DATA signals from the memory sense amplifiers condition the corresponding data buffer FFs in the memory timing unit to be triggered by Read Strobe.
MEM-R-01K/2 MEM-R-02K/2 MEM-R-04K/2 MEM-R-08K/2	ADD	RBA	MEMORY-01K-08K signals are produced by the Base Adder and contain the thousands digit of the true address in BCD form

SIGNAL NAME	TYPE	SOURCE	DEFINITION
MEM-R-10K/2 MEM-R-20K/2 MEM-R-40K/2 MEM-R-80K/2	ADD	RBA	MEMORY-10K-80K signals are produced by the base adder and contain the ten-thousands digit of the true address in BCD form. (These signals are not required for addressing, but are used only for the Test Panel display.)
MEM-SEL-Ø/1 MEM-SEL-1/1 MEM-SEL-2/1 MEM-SEL-3/1 MEM-SEL-4/1 MEM-SEL-5/1 MEM-SEL-6/1 MEM-SEL-7/1 MEM-SEL-8/1 MEM-SEL-9/1 MEM-SEL-1Ø/1	DEC	RBA	MEMORY-SELECT-Ø-1Ø signals determine which one of the eleven possible Main Memory modules is to be addressed.
MINUS/2	DFF	RDA	MINUS is one of the condition flip-flops in the ACU.
M-IOS/3	G	CH1,CH3	MODE-IOS determines the mode of data entry into the IOS shift register in the IOC. When M-IOS/3 is high, it permits parallel loading of data into the IOC (from the ACU): when it is low, it permits serial loading of data (from within the IOC).
M1/6 M2/6 M3/6 M4/6	G	TMN	M Register (four cross-coupled latches) makes up the buffer for the lower four bits of INP-DATA, FAC-DATA, and data present on the S-BUS.
N1/6 N2/6	G	TMN	N Register (two cross-coupled latches) makes up the buffer for the upper two bits (zone bits) of INP-DATA, FAC-DATA, and data present on the S-BUS.
ON-LINE/4	G	CH1,CH3, CH5,IO1, CL3	ON-LINE is a signal generated in an IOC when that IOC is "selected", or "active".
OUT-DATA-1/3 OUT-DATA-7/3 OUT-DATA-1/6 OUT-DATA-2/3 OUT-DATA-3/3 OUT-DATA-4/3 OUT-DATA-5/3 OUT-DATA-7/3	G	TMN MTM	OUTPUT-DATA lines convey the 6-bit coded character from the ACU to the IOC or to Main Memory. (OUT-DATA-7/6 goes to Main Memory only, since the 7 bit is converted before being sent to the IOC.)

SIGNAL NAME	TYPE	SOURCE	DEFINITION
OUT-REQ/3	G	CH6	OUTPUT-REQUEST is a signal from the IOC to the ACU. IF the ACU receives an OUT-REQ during a READ, the operation is converted to a WRITE, allowing transmission of an ACKnowledge signal to a modem.
P/CARRY/3	G	LDA,LAR	PRESET CARRY sets the CARRY FF.
P/CHECK/1	G	LIF	PRESET CHECK sets the CHECK FF in the active IOC, when type of error or unusual operation has occurred.
P-COM/3	G	RAD	P-COMMON is the flip-flop in the P Register used to signify that the P Register is addressing the common area of Main Memory.
P/COUNT/3	G	CH1	PRESET COUNT sets the COUNT FF in the active IOC, to enable the State Counter in that IOC.
P/F2/3	G	LRW,LAR	PRESET F2 sets the F Register F2 FF.
P/F3/3	G	LRW,LIF, LAR	PRESET F3 sets the F Register F3 FF.
P-INCR/3	G	LRW,LIF	P-INCREMENT causes the count in the P Register to be increased by 1. The trailing edge of the signal initiates the increment.
P/INH-SW/1		LIF	
P/IO-BUSY/1	G	LRW	PRESET IO-BUSY sets the active IOC IO-BUSY FF.
P/JUMP/3	G	LRW	PRESET JUMP sets the active IOC JUMP FF.
P/LAST/1	G	LRW	PRESET LAST sets the active IOC LAST FF, signaling the end of an I/O operation.
P/LD-REQ/1	G	LRW	PRESET LOAD-REQUEST sets the active IOC LDRQ FF when the ACU initiates a Load operation.
P-LIM-TO-S/4	G	LRW	PARTITION-LIMIT-TO-S signal and the Q Counter outputs gate the BCD digit representing the partition limit onto the S-BUS for entry into the M Register, for storing into the protected area of Main Memory, under control of the Q Counter.
P-LIM-1/4 P-LIM-2/4 P-LIM-4/4 P-LIM-8/4	G	CH2,CH4, CH6,IO2, CL3	PARTITION-LIMIT is a BCD representation of size of the active partition in thousands. It is set by installing jumpers on one of the IOC cards.
P/MINUS/3	G	LDA,LAR	PRESET MINUS sets the MINUS FF in the ACU.

SIGNAL NAME	TYPE	SOURCE	DEFINITION
P/N1/3	G	LRW,LAR	PRESET N1 sets the N1 FF in the N (Memory buffer) Register. This often signifies a numeric or instructional character.
P/RESET/3	G	CH1	PRESET RESET is a signal developed in the active IOC that sets the RESET FF in that IOC.
P/SUB/3	G	LDA	PRESET SUBTRACT sets the SUBTRACT FF and the CARRY FF in the ACU.
PARTITION=Ø/3	G	RBA	PARTITION=Ø is produced when the ACU is operating in partition Ø. This signal is used to enable Set Mode.
PCTR-TO-M/1	G	LDA	POLL COUNTER-TO-M gates the contents of the Poll Counter from the active IOC onto the S-BUS for entry into the M Register.
P-INCR/3			
P-OUT/3			
PO-3/1	DEC	LDA	POSITIONING-3 denotes that the current state is the #3 step of the POSITIONING function.
PRIV-CHAN/3	G	CH1,CH3, CH5,IO1, CL3	PRIVILEGED-CHANNEL is an IOC signal denoting that the active IOC is allowed access to the Privileged portion of the Common Area in Main Memory.
PWR-FAIL-Ø/3	G	TST	POWER-FAILURE-Ø is the reset output of the SYSTEM-RESET FF. It develop PWR-FAIL/4 and causes the IO-BUSY+PWR-FAIL FF to set at SCB-STR time.
PWR-FAIL-1/3		P.S.#1	POWER-FAILURE-1 is developed by the main power supply when power begins to fail. It develops PWR-FAIL/4 and causes the IO-BUSY+PWR-FAIL FF to set at SCB-STR time.
PWR-FAIL-2/3		P.S.#2	POWER-FAILURE-2 is developed by the supplementary power supply when power begins to fail. It develops PWR-FAIL/4 and causes the IO-BUSY+PWR-FAIL FF to set at SCB-STR time.
PWR-FAIL/4	G	LIF	POWER-FAILURE signal is developed by either PWR-FAIL-Ø, PWR-FAIL-1, or PWR-FAIL-2, and causes the PWR-FAIL FF in the ACU to set.

SIGNAL NAME	TYPE	SOURCE	DEFINITION
P1-DECR/3	G	RDA,LRW	P1-DECREMENT causes the count in the P Register P1 character to be reduced by 1. The trailing edge of the signal initiates the decrement.
Q-DECR/2	G	LIF	Q-DECREMENT causes the count in the Q Counter to be recuded by 1. The trailing edge of the signal initiates the decrement.
Q-INCR/3	G	LRW,LIF, LDA	Q-INCREMENT causes the count in the Q Counter to be increased by 1. The trailing edge of the signal initiates the increment.
Q-OUT/6	G	RBA	Q-OUT gates the contents of the Q Counter onto the units lines of the R-BUS.
Q=Ø/2 Q=1/2 Q=2/2 Q=3/2 Q=4/2	G	RAD	Q=Ø-4 specifies the particular count contained in the Q Counter. These signals are used for sequencing certain 4- and 5-part operations.
R-BUS-1K/2 R-BUS-2K/2 R-BUS-4K/2 R-BUS-8K/2	G	RAD	R-BUS-1K-8K are four lines that hold the BCD character representing the thousand's digit of the relative address.
R-BUS-COM/3	G	RAD	R-BUS-COMMON denotes that the address presently on the R-BUS is in the Common Area of Main Memory rather than in the active IOC's partition.
R-BUS-001/2 R-BUS-002/2 R-BUS-004/2 R-BUS-008/2	G	RAD	R-BUS-001-008 are four lines that hold the BCD character representing the units digit of the Main Memory address.
R-BUS-010/2 R-BUS-010/3 R-BUS-020/2 R-BUS-020/3 R-BUS-040/2 R-BUS-040/3 R-BUS-080/2 R-BUS-080/3	G G G G G G G G	RAD RBA RAD RBA RAD RBA RAD RBA	R-BUS-010-080 are four lines that hold the BCD character representing the tens digit of the Main Memory.
R-BUS-100/2 R-BUS-200/2 R-BUS-400/2 R-BUS-800/2	G	RAD	R-BUS-100-800 are four lines that hold the BCD character representing the hundreds digit of the Main Memory.

SIGNAL NAME	TYPE	SOURCE	DEFINITION
R-TO-S/3	G	LRW,LIF, LDA	R-TO-S signal and the Q Counter outputs gate the contents of the R-BUS onto the S-BUS for entry into the M Register.
READ/3	G	LRW,LIF, LDA	READ signal enables a Main Memory Read cycle.
RESRV-MEM/3	G	DDJ	RESERVE-MEMORY is a signal level from the FAC that causes the ACU to stop normal processing and to allow only the FAC to use the Main Memory.
RETRIAL/3 RETRIAL/4	G	CH1	RETRIAL is a flip-flop in the IOC that enables retransmission of a character to the line unit if the line unit fails to acknowledge the prior transmission.
RETURN-1/8 RETURN-2/8	RES	CH2	RETURN-1-2 are the "return" half of the two 2-wire transmission lines associated with a given IOC.
RS/5	G	MTM	READ STROBE is a memory timing signal that strobes the MEM-DATA signals from the sense amplifiers into the memory output buffer flip-flops.
RST-T/3	G	CH1	RESET-TIME is a flip-flop signal in the IOC that resets the T (Time) Counter to TØ.
RW-11,14/4	G	LRW	READ/WRITE-11,14 is developed during steps 11 and 14 of READ/WRITE to yield P/CHECK when there is a DATA/FAULT during retrieval of a disc address from Main Memory.
S-BUS-1/3 S-BUS-2/3 S-BUS-3/3 S-BUS-4/3 S-BUS-5/3 S-BUS-7/3	G	TST,RDA, RAD	S-BUS-1-7 are the six lines in the ACU that receive the FAC output data. The S-BUS data is applied to the M & N Registers and data from the ACU hardware registers.
S-1A/7 S-1A/8	DIODE	MST	SENSE-1A is the digit line (sense/inhibit wire) threaded through the first half of the 1-bit cores in Main Memory.
S-1AC/8	RES	MDG	SENSE-1A COMMON is the mid-point (2,500 cores on each side) at which S-1A/7 and S-1A/8 meet. It is also the output of the 1-bit "A" inhibit driver.

SIGNAL NAME	TYPE	SOURCE	DEFINITION
S-1B/7 S-1B/8	DIODE	MST	SENSE-1B is the digit line (sense/inhibit wire) threaded through the latter half of the 1-bit cores in Main Memory.
S-1BC/8	RES	MDG	SENSE-1B COMMON is the mid-point (2,500 cores on each side) at which S-1B/7 and S-1B/8 meet. It is also the output of the 1-bit "B" inhibit driver.
S-2A/7 S-2A/8 S-2AC/8 S-2B/7 S-2B/8 S-2BC/8	DIODE RES DIODE RES	MST MDG MST MDG	These signals are the 2, 3, 4, 5 and 7-bit equivalents of the 1-bit signals described previously. Refer to the preceding for definitions.
S-3A/7 S-3A/8 S-3AC/8 S-3B/7 S-3B/8 S-3BC/8	DIODE RES DIODE RES	MST MDG MST MDG	
S-4A/7 S-4A/8 S-4AC/8 S-4B/7 S-4B/8 S-4BC/8	DIODE RES DIODE RES	MST MDG MST MDG	
S-5A/7 S-5A/8 S-5AC/8 S-5B/7 S-5B/8 S-5BC/8	DIODE RES DIODE RES	MST MDG MST MDG	
S-7A/7 S-7A/8 S-7AC/8 S-7B/7 S-7B/8 S-7BC/8	DIODE RES DIODE RES	MST MDG MST MDG	
S=Ø/1	DEC	TMN	S=Ø signal indicates that the code presently on the S-BUS is equal to a binary zero.
S=1/1	DEC	TMN	S=1 signal indicates that the code presently on the S-BUS is equal to a binary 1.

SIGNAL NAME	TYPE	SOURCE	DEFINITION
S=9/1	DEC	TMN	S=9 signal indicates that the code presently on the S-BUS is equal to a binary 9.
SC-DECR/3	G	LRW,LAR	STEP COUNTER-DECREMENT causes the count in step counter to be decreased by 1. The trailing edge of the signal initiates the decrement.
SC-INH/3	G	LRW,LDA, LAR	STEP COUNTER-INHIBIT signal inhibits the normal step counter increment signal that occurs at 3T time.
SCB-STR/1	DFF	TMN	STEP COUNTER BUFFER-STROBE appears during the .33 μsec "dead" time between states to gate the Step Counter into the Step Counter Buffer. This signal also gates the condition of the Function Counter into the Function Counter Buffer. Under certain circumstances it strobes 9 other ACU FFs.
SCB-1/1 SCB-2/1 SCB-3/1 SCB-4/2	G CTR	LIF	SCB-1-4 are the outputs of the Step Counter Buffer which, along with the Function Counter Buffer outputs, are decoded into the various states.
SEL-W/2 SEL-X/2 SEL-Y/2 SEL-Z/2	G	RBA	SELECT-W,X,Y,Z are the Select Group signals, decoded from the X Counter outputs. Along with the Select Digit signals, they determine which one of the 20 possible partitions is to be "active".
SEL-Ø/2 SEL-1/2 SEL-2/2 SEL-3/2 SEL-4/2	G	RBA	SELECT-Ø-4 are the Select Digit signals, decoded from the X Counter outputs. Along with the Select Group signals, they determine which one of the 20 possible partition is to be "active".
SEND/4	G	CH1	SEND is a signal within the IOC that is present the IOC is transmitting to the line unit.
SERV-REQ/3	G	CH1,CH3, CH5,IO1, CL3	SERVICE-REQUEST causes the $\overline{\text{ACU-SV-REQ}}$ FF to reset when the active IOC has a service request.
SM-INHSW/1	DFF	LIF	SET-MODE-INHIBIT-SWITCH is a flip-flop signal that is present when the Inhibit Switch option of Set Mode is being used.
SS/1	G	MTM	STACK SELECT is the memory timing card output that selects the proper core module according to the MEM-SEL signal valid at the time. (This is a single signal in the ACU module since only one core stack is used.)

SIGNAL NAME	TYPE	SOURCE	DEFINITION
ST-NEG-1/7 ST-NEG-2/7	RES	CH2	START-NEGATIVE is the "send" side of the two-wire transmission line between the IOC and the line unit. The "1" and "2" denote that there are two pairs of wires available at each IOC. Each ST-NEG line goes negative, with respect to the corresponding RETURN line, at the first clock of each transmission.
STATE-CLK/5	G	TMN	STATE-CLOCK is developed from STATE-TIME, and gates the individual signals out of the State decoders. Inhibiting the STATE-CLOCK output suspends normal ACU operation.
STATE-TIME/6	G	TMN	STATE-TIME is a timing signal that develops STATE-CLOCK, SCB-STR, and other signals. It is .777 μsec long for "regular" states and 3.0 μsec long for states that require core memory cycles. There is always .33 μsec of "dead" time between STATE-TIMES. STATE-TIME is never inhibited, so it is available even when normal processing is suspended (STATE-CLOCK off).
STATUS-IN/4	G	LRW	STATUS-IN sets or resets the condition flip-flop (ZERO, MINUS, and CARRY) according to the status code in the M Register.
STATUS-RDY/1 STATUS-RDY/3	DFF G	TMN DRH,TC1, OC2	STATUS-READY is a signal from the FAC indicating that the selected device has its status character on the data lines, ready for input to the ACU.
STEP-INCR/3	G	TST	STEP-INCREMENT is a Test Panel signal that causes the count in Step Counter to be increased by one. The trailing edge of the signal initiates the increment.
STOP/2	G	TMN	STOP is a flip-flop signal from the ACU which inhibits the STATE-CLK output when so dictated by the settings of the Test Panel switches.
SUB/3	G	RDA	SUBTRACT is a flip-flop signal that is produced whenever the ACU is in a "machine subtract" condition. Whenever the SUBTRACT FF changes state, the CARRY FF assumes the same state.
SW2/2	G	LRW	SWITCH 2 indicates that the ACU is in step 2 of the SWITCH function.

SIGNAL NAME	TYPE	SOURCE	DEFINITION
SYS-RES/1 SYS-RES/7	G XSTR	LIF TST P.S.#1	SYSTEM-RESET is developed when the System Reset button on the Test Panel is depressed or when the power supply is cycling up or cycling down. It halts all ACU operation and places an ACU in its initial state: (1) Sets FC and SC to SW-2. (2) Resets XØ & X1 to address partition Ø. (3) Resets base adder (Y1) to partition Ø. (4) Resets F2 FF, Q Counter, ADDR-INH FF. (5) Sets ALLOW-INSTR, INSTR-STOP FFs. (6) Resets IOC & initiates polling.
SØ/1 SØ/4	DEC G	CH2	STATE Ø in the IOC timing.
S1/4	G	CH2	STATE 1 in the IOC timing.
S2/3 S2/4	DEC G	CH2	STATE 2 in the IOC timing.
S3/4	G	CH2	STATE 3 in the IOC timing.
S5/4	G	CH2	STATE 5 in the IOC timing.
S7/4	G	CH2	STATE 7 in the IOC timing.
S8/4	G	CH2	STATE 8 in the IOC timing.
SlØ/1	DEC	CH2	STATE 1Ø in the IOC timing.
S11/1	DEC	CH2	STATE 11 in the IOC timing.
S12/1 S12/4	DEC G	CH2	STATE 12 in the IOC timing.
S13/1 S13/4	DEC G	CH2	STATE 13 in the IOC timing.
S14/1 S14/4	DEC G	CH2	STATE 14 in the IOC timing.
S15-ESC/3	G	CH1	STATE-15-ESCAPE signal is produced by the IOC when it is in State 15 of Escape mode. In this state operations end and the IOC resets to starting conditions.
S15/4	G	CH2	STATE 15 in the IOC timing.
S311/4	G	CH2	STATE 311 is a signal that is present during all states, 3 through 11, in the IOC timing.

SIGNAL NAME	TYPE	SOURCE	DEFINITION
S410/4	DFF	CH2	STATE 410 is a signal that is present during all states, 4 through 10, in the IOC timing.
S412/3	G	CH2	STATE 412 is a signal that is present during all states, 4 through 12, in the IOC timing.
T/E2/4	G	LAR	TOGGLE E2 causes the E2 FF to change state. The toggle occurs at the leading edge of the signal.
T/MINUS/4	G	LAR	TOGGLE MINUS causes the MINUS FF to change state. The toggle occurs at the leading edge of the signal.
T/SUB/6	G	LAR	TOGGLE SUBTRACT causes the SUBTRACT FF to change state. The toggle occurs at the leading edge of the signal. The CARRY FF also changes state if it was in the same state as was SUBTRACT.
TERM-READ/3	G	CH1	TERMINATE-READ/3 is developed in the active IOC to inform the ACU that a READ operation has been terminated by the operator at the active peripheral, the IOC then provides blanks to the ACU to fill the input data field in Main Memory.
TERM-TRANS/1 TERM-TRANS/2	G	RAD LRW	TERMINATE-TRANSFER informs the selected FAC device that the data transfer is complete (or postponed) and that a status character is required.
TIME-OUT/3 TIME-OUT/4	DFF	CH2	TIME-OUT is an IOC signal that terminates an I/O instruction after a given transmission has been unsuccessfully attempted for a specified length of time.
TIMEOUT/2	DFF	TST	TIMEOUT is a flip-flop signal in the ACU that is initiated after a partition has been serviced for 200 msec. This condition is detected only in BRANCH, where a jump to SWITCH occurs.
TURN-ON/4	G	CH1,CH3	TURN-ON is an IOC signal developed by SYS-RES that initializes the IOC, resetting all necessary flip-flops and placing the IOC into the "Escape" mode.
TURN/4	G	CH1	TURN is a flip-flop in the IOC that causes a rapid turn-around in the direction of transmission when the IOC detects a unit separator code or when the last item of data is received by the IOC. This turn-around enables the IOC to send a "request for status" back to the line unit.

SIGNAL NAME	TYPE	SOURCE	DEFINITION
TØ/4 T3/4 T4/4 T5/4 T6/1 T7/4	G G G G DEC G	CH2	TØ-7 are the timing pulses in the IOC. Each is 2.2 μsec long and there is an equal length of time between signals.
WRITE-ENA/4	G	CH1	WRITE-ENABLE is an IOC signal that "turns on" the IOC transmitter each time a code or an "ACK" is to be sent to the line unit.
WRITE-INFO/3	G	CH1	WRITE-INFORMATION is an IOC signal that causes toggling of the WRITE TRANSITION FF in the IOC whenever a logic 1 bit is to be sent to the line unit.
WRITE-PC/3	G	CH1	WRITE-POLL COUNTER is an IOC signal that gates the setting of the Poll Counter into the IOS shift register for transmission to the line unit.
WRITE/3	G	LRW,LDA, LAR	WRITE enables a Main Memory write cycle.
X-CLK/2	G	CH2	X-CLOCK is an IOC signal that resets the time counter to TØ when a clock from the line unit is sensed, after the time counter cycle has been extended to allow the IOC to wait for a clock.
X-INCR/3	G	TST,LRW, LIF	X-INCREMENT causes the count in the X Counter to be increased by 1. The trailing edge of the signal initiates the increment.
X-OUT/2 X-OUT/3	G G	LRW RAD	X-OUT signal gates the contents of the X1 Counter onto the R-BUS, and gates either the Common Area limit or the Priviledged Area lower limit into the base adder (depending on the IOC patching) so that the Protected Area of core may be addressed.
X-RST/1	G	MTM	X-READ SINK TIME is a memory timing signal that enables all X Read Sink drivers during the "READ" portion of a memory cycle.
X-RT/1	G	MTM	X-READ TIME is a memory timing signal that enables all X Read Source drivers during the "READ" portion of a memory cycle.

SIGNAL NAME	TYPE	SOURCE	DEFINITION
X-RØ/8 X-R1/8 X-R2/8 X-R3/8 X-R4/8 X-R5/8 X-R6/8 X-R7/8 X-R8/8 X-R9/8	XSTR	MDR	X-RØ-9 are the outputs of the ten X Read Drive (Source) drivers in the memory module.
X-SØ/7 X-S1/7 X-S2/7 X-S3/7 X-S4/7 X-S5/7 X-S6/7 X-S7/7 X-S8/7 X-S9/7	XSTR	MDR	X-SØ-9 are the outputs of the ten X Sink drivers in the memory module.
X-TO-S/4	G	LRW	X-TO-S is used in conjunction with X-OUT to gate the number of the active partition out of the X Counter onto the S-BUS and into the M and N Registers. The code in the X1 counter is set into M and the state of the XØ FF is set into N1. N2 remains reset.
X-WST/1	G	MTM	X-WRITE SINK TIME is a memory timing signal that enables all X Sink drivers during the "WRITE" portion of a memory cycle.
X-WT/1	G	MTM	X-WRITE TIME is a memory timing signal that enables all X Write Source drivers during the "WRITE" portion of a memory cycle.
X-WØ/8 X-W1/8 X-W2/8 X-W3/8 X-W4/8 X-W5/8 X-W6/8 X-W7/8 X-W8/8 X-W9/8	XSTR	MDR	X-WØ-9 are the outputs of the X Write Drive (Source) drivers in the memory module.

SIGNAL NAME	TYPE	SOURCE	DEFINITION
X-ØØ/1 X-Ø1/1 X-Ø2/1 X-Ø3/1 X-Ø4/1 X-Ø5/1 X-Ø6/1 X-Ø7/1 X-Ø8/1 X-Ø9/1	DEC	MTM	X-ØØ-Ø9 select one of the ten X Read/Write Source drivers. These signals are the output of a one-in-ten decoder, the input to which is the BCD units digit from the R-BUS.
X-10/1 X-11/1 X-12/1 X-13/1 X-14/1 X-15/1 X-16/1 X-17/1 X-18/1 X-19/1	DEC	MTM	X-1Ø-19 select one of the ten X Read/Write Sink drivers. These are the output of a one-in-ten decoder, the input to which is the BCD tens digit from the R-BUS.
XØ/2	DFF	RBA	XØ is a flip-flop signal in the ACU (part of the X Counter) that determines which group of digits, 0-4 or 5-9, the Q Counter will address in the protected area of core. It is also used in decoding the SELECT-GROUP signals.
Y-RST/1	G	MTM	Y-READ SINK TIME is a memory timing signal that enables all Y Sink drivers during the "Read" portion of a memory cycle.
Y-RT/1	G	MTM	Y-READ TIME is a memory timing signal that enables all Y Read Source drivers during the "Read" portion of a memory cycle.
Y-RØ/8 Y-R1/8 Y-R2/8 Y-R3/8 Y-R4/8 Y-R5/8 Y-R6/8 Y-R7/8 Y-R8/8 Y-R9/8	XSTR	MDR	Y-RØ-9 are the outputs of the ten Y Read Drive (Source) drivers in the memory module.

SIGNAL NAME	TYPE	SOURCE	DEFINITION
Y-SØ/7 Y-S1/7 Y-S2/7 Y-S3/7 Y-S4/7 Y-S5/7 Y-S6/7 Y-S7/7 Y-S8/7 Y-S9/7	XSTR	MDR	Y-SØ-9 are the outputs of the ten Y Sink drivers in the memory module.
Y-WST/1	G	MTM	Y-WRITE SINK TIME is a memory timing signal that enables all Y Sink drivers during the "Write" portion of a memory cycle.
Y-WT/1	G	MTM	Y-WRITE TIME is a memory timing signal that enables all Y Write Source drivers during the "Write" portion of a memory cycle.
Y-WØ/8 Y-W1/8 Y-W2/8 Y-W3/8 Y-W4/8 Y-W5/8 Y-W6/8 Y-W7/8 Y-W8/8 Y-W9/8	XSTR	MDR	Y-WØ-9 are the outputs of the Y WRITE Drive (Source) drivers in the memory module.
Y-ØØ/1 Y-Ø1/1 Y-Ø2/1 Y-Ø3/1 Y-Ø4/1 Y-Ø5/1 Y-Ø6/1 Y-Ø7/1 Y-Ø8/1 Y-Ø9/1	DEC	MTM	Y-ØØ-Ø9 select one of the ten Y Read/Write Source drivers. These signals are the output of a one-in-ten decoder, the input to which is the BCD hundred's digit from the R-BUS.
Y-1Ø/1 Y-11/1 Y-12/1 Y-13/1 Y-14/1 Y-15/1 Y-16/1 Y-17/1 Y-18/1 Y-19/1	DEC	MTM	Y-1Ø-19 select one of the ten Y Read/Write Sink drivers. These signals are the output of a one-in-ten decoder, the input to which is the thousand's digit from the base adder.

SIGNAL NAME	TYPE	SOURCE	DEFINITION
ZERO/3	G	RDA	ZERO is one of the condition flip-flops in the ACU.
0001-TO-M/3	G	LRW,LIF	0001-TO-M causes a binary 1 to be set into the M Register.
01-TO-N/3	G	LRW,LDA, LAR	01-TO-N causes the E1 FF (5 bit) to set and the E2 FF (7 bit) to reset.
1-BIT/2	SR	CH2	1-BIT is the binary 1 output of the IOS shift register in the IOC. Each bit in a code appears at this output sequentially as the code is shifted out of IOS.
1ØØ-OUT/4	G	LRW	100-OUT places a binary 1 on the hundred's portion of the R-BUS when it is desired to address the 100-199 portion of the protected area of Main Memory.
2ØØ-OUT/4	G	LRW	
11-TO-N/3	G	LDA,LAR	11-TO-N causes both the E1 and E2 FFs to set, denoting a 5 bit and a 7 bit.
2T/2	G	TMN	2T is an ACU timing signal that occurs 333 nanoseconds after STATE TIME begins, and lasts for 222 nsec.
3T/5	G	TMN	3T is an ACU timing pulse that occurs during the last 222 nsec of STATE-TIME.
40-OUT/4	G	LRW	40-OUT occurs after an error, to address locations 40-44 of the active partition. It does this by applying a binary 4 to the ten's portion of the R-BUS.
5-BIT/2	SR	CH2	5-BIT is the 5-bit output of the IOS shift register in the IOC. It is used to test the I/O function code to determine whether the I/O function is a READ or a WRITE.

C-1.0 MODEL 20 PROCESSOR INSTALLATION

This section describes the technical installation procedures and requirements for the Model 20 Processor and the I/O devices and FAC controllers that are part of the processor mainframe assembly.

C-1.1 DELIVERY INSPECTION

Immediately after the equipment is delivered it must be inspected for indications of damage and for completeness of shipment. If any damage is noted, DO NOT unpack the equipment until an authorized representative of the carrier is present. If a portion of the shipment is missing, notify the carrier immediately.

C-1.2 UNPACKING

The Model 20 Processor is shipped in a protective plastic shroud, and air shipments are attached to a wooden skid. Shipments within the contenent of North America will usually not include the wooden skid. Figure C-1 shows the packing arrangement that is used for air shipments. Remove the packing material in the order given below, ignoring the first two instructions if the shipment arrives without the wooden skid.

- Remove the four bolts that secure the unit to the skid.
- Carefully slide the processor off the skid.
- Position the unit in the location where it is to be installed.
- Remove the plastic shroud and all external shipping tape.
- Remove any side panels that are necessary to complete unpacking (be sure to place the panels where they will not be damaged).
- Attach the glides (feet) and level the unit by adjusting the feet up or down.
- Carefully remove the filament tape from each card cage. Note and/or repair any damage that is noted.
- Check the motherboard pins and main connections to be sure that none of the pins touch each other or a voltage bus.
- Verify that all printed circuit cards are the proper revision level and are installed in the proper slots. Check also that the printed circuit cards are properly seated in the motherboard connector. Figure C-2 shows card positions within the processor modules.
- Check the documentation to be sure it is complete and for the proper revision level for each printed circuit card.

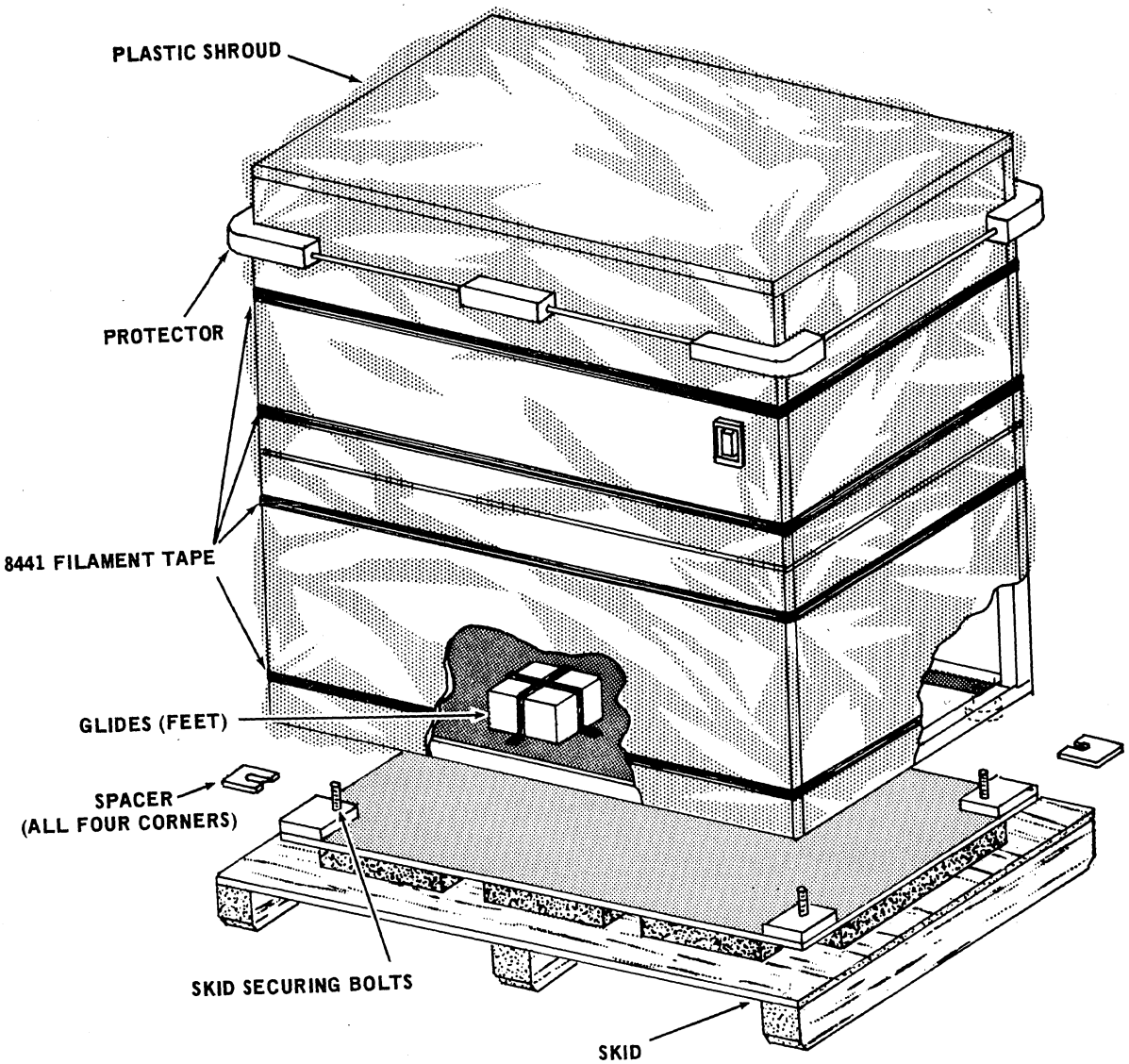


Figure C-1. MODEL 20 (AIR) SHIPMENT CONFIGURATION

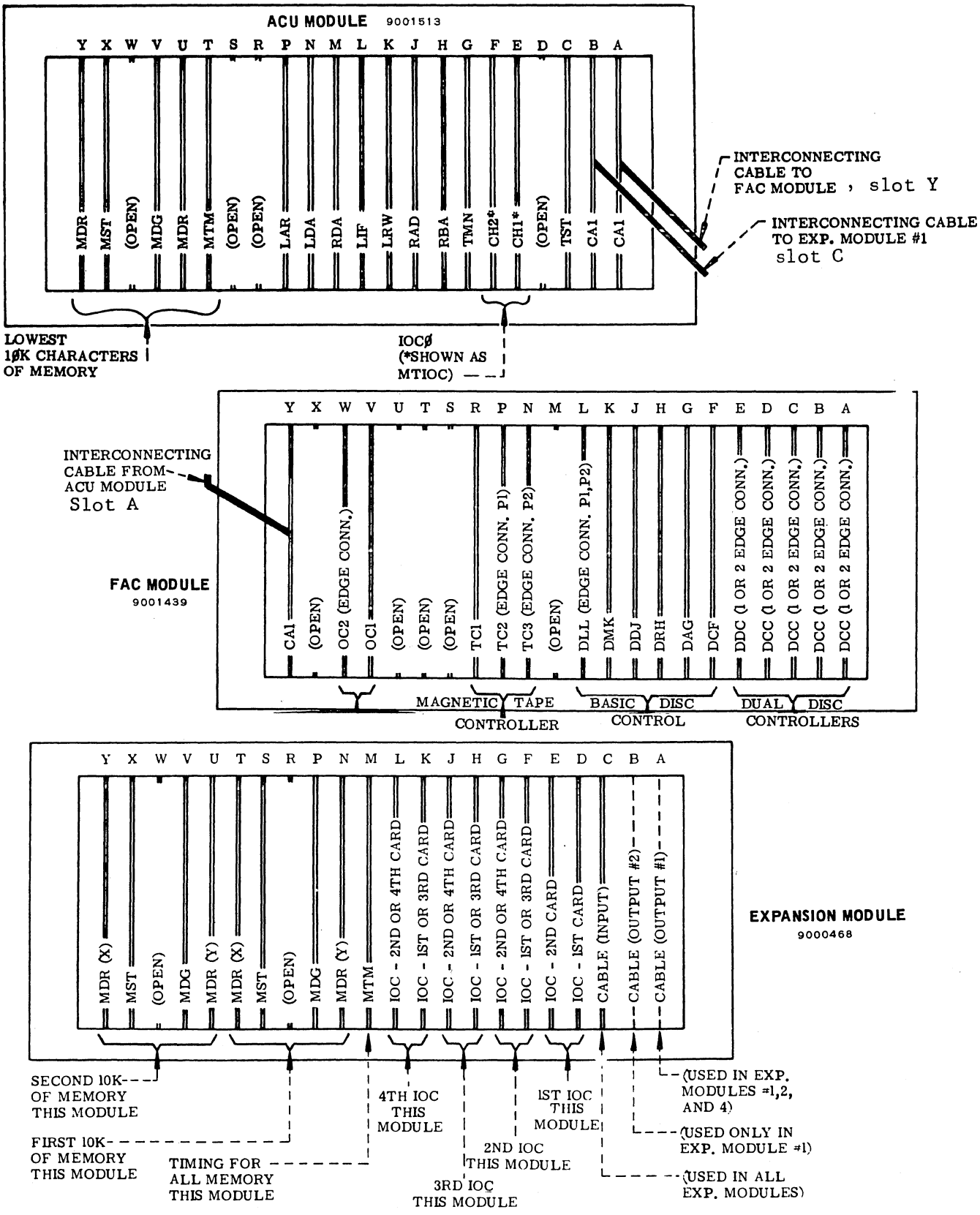


Figure C-2. CARD LOCATIONS

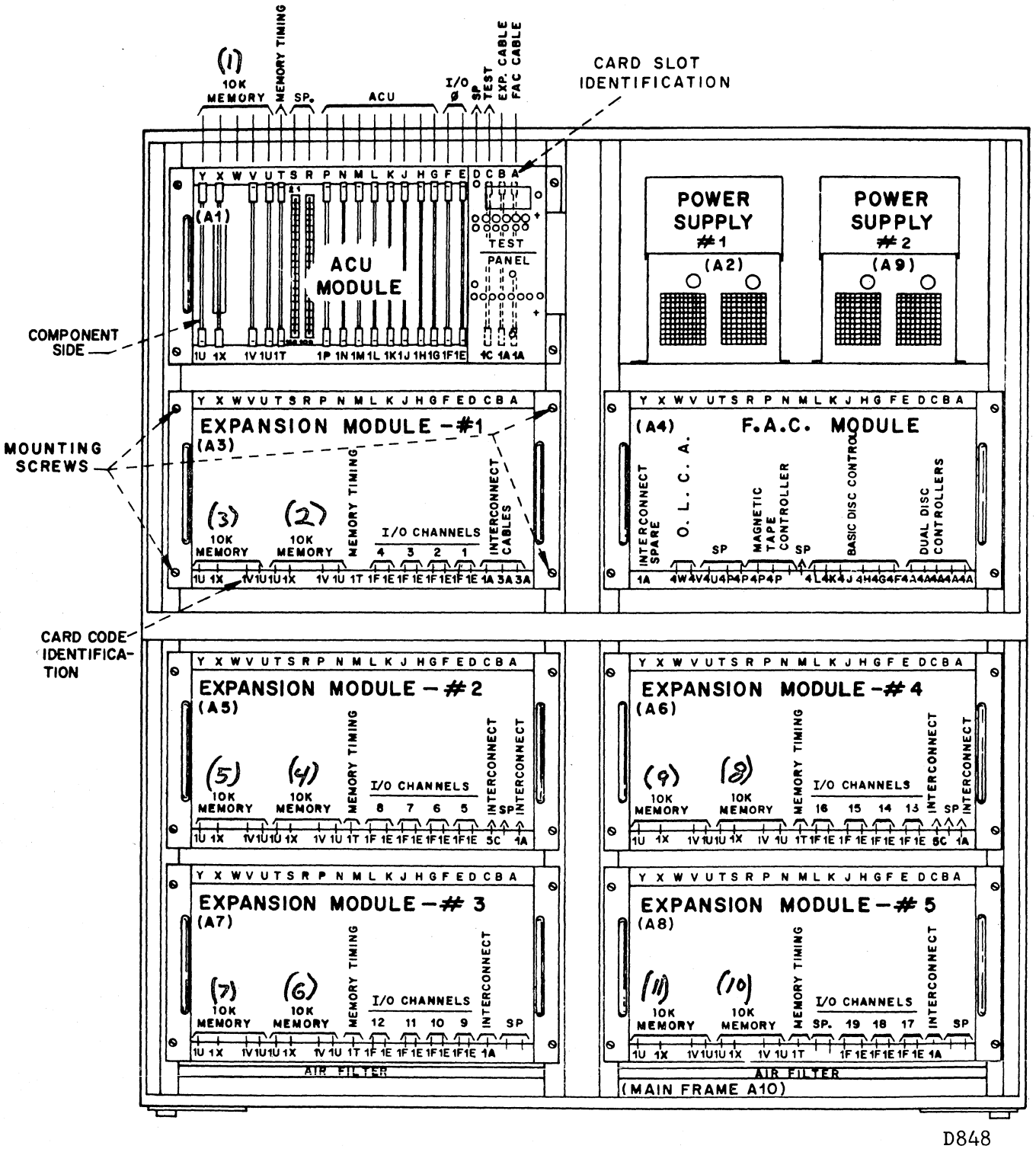


Figure C-3. PROCESSOR MODULE ARRANGEMENT

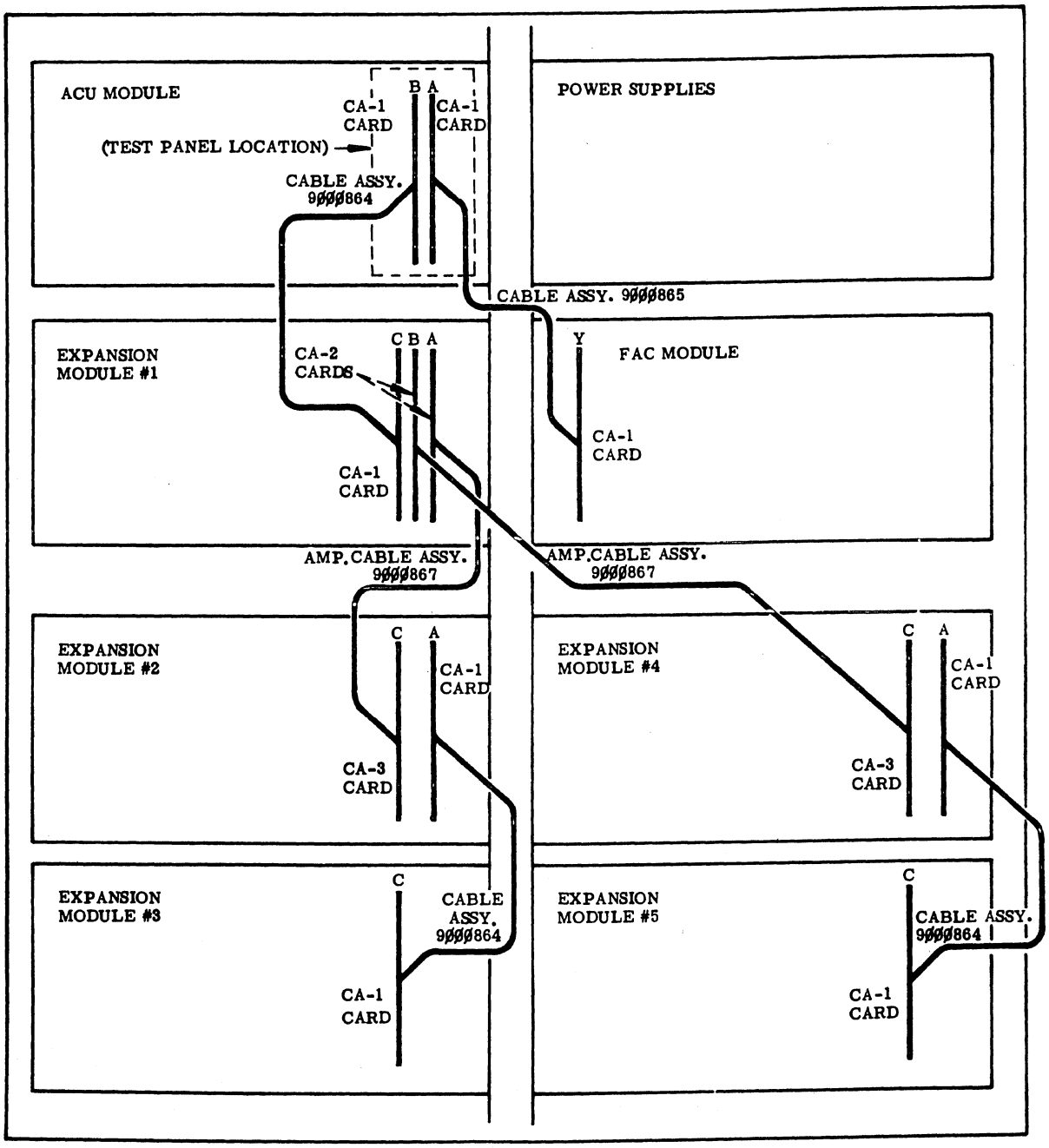


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Figure C-4. INTERCONNECTING CABLES

C-1.3 INSTALLING EXPANSION MODULES

If an additional expansion module must be installed, determine the correct location for the module and slide it into place. Secure the module unit into place with the four screws that are supplied with the module shipment. Modules must be added in numerical order as shown in figure C-3.

Circuit cards should be installed as necessary, referring to the individual memory or I/O applications. An expansion module can be used for additional memory, or for additional I/Os, or both. However, both are not necessary for one or the other to operate satisfactorily.

Signal cables are connected by plugging into the card slots from the front of the processor. Figure C-4 shows the proper cable numbers for the various connections. Be sure when installing the 9000867 amplifier cable that the CA2 end is placed at the source (expansion module #1).

Connect the power bus inputs and the ground bus connections at the rear of the processor. The black wire connects to the upper terminal (+15v), the red wire connects to the center terminal (+5v), and the yellow wire connects to the lower terminal (-12v).

The ACU module, the FAC module, and expansion module #1 (directly below the ACU module) are supplied by the power supply nearest the ACU module (power supply #1). If a second expansion module is added, a second power supply must also be added. The second power supply furnishes power to all additional expansion modules.

CAUTION

Never make power connections or insert or remove expansion cables or printed circuit cards while the processor is energized.

C-1.4 INSTALLING POWER SUPPLY NO. 2

Power supply no. 2 supplies operating voltages for expansion modules 2 through 5. Install the power supply as follows.

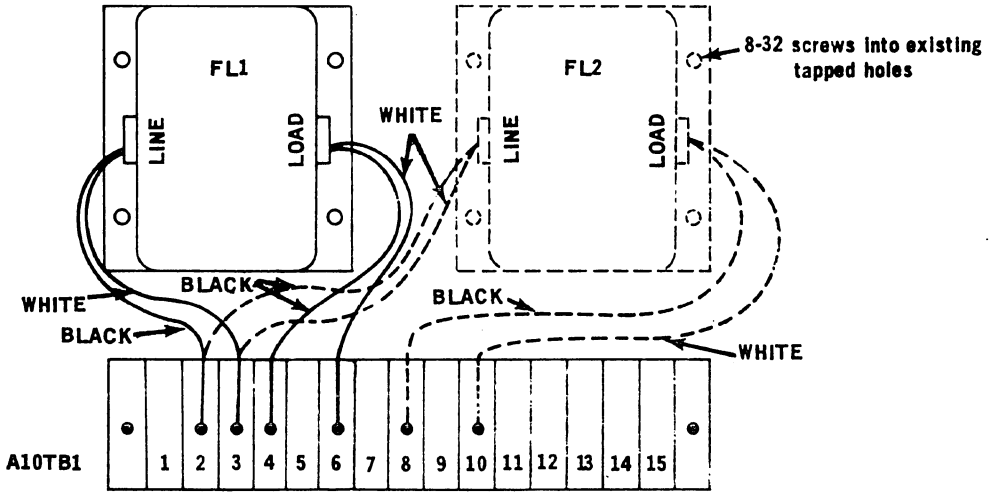
WARNING

Remove all power from the processor before servicing the line filters, power supplies, ac wiring harness, or blowers.

- To install the four power supply mounting screws it is necessary to remove or loosen the FAC module. With the power OFF, remove the three voltage input wires (black, red, and yellow), and the two ground bus connections (black).
- Remove the four mounting screws that hold the FAC module to the front frame.
- Remove the retaining bar and FAC device cables, if they are present.
- Carefully remove the FAC module; avoid damage to the motherboard or to the protruding connector pons.
- Set the power supply into place and secure it with the four screws. These screws pass upward through the frame into captive nuts on the power supply.

C -1.4 INSTALLING POWER SUPPLY NO. 2 (Continued)

- Replace the FAC module and secure it with the four mounting screws in front.
- Install the line filter (part no. 9003291) next to the other line filter. Use the 8-32 screws (2749) that are provided, and the tapped holes that were meant for this purpose.
- Remove the cover from the adjoining terminal block, and connect the filter wires as shown below.



- Release the cable connections that are tied back at the power supply, remove the protective shrink tubing on the connector lugs, and make the connections as follows.
  - Green wire from A9E1 (ground) to A2E1 (ground on power supply no. 1).
  - Black wire tagged "H" (ac high) to (A9)7TB-3.
  - White wire tagged "G" (ac low) to (A9)7TB-4.
  - White wire tagged "A" from PWR-FAIL (A9)1TB-1 to A1TB1-2 (ACU module).
  - White wire tagged "E" from SYS-RST (A9)1TB-2 to (A2)1TB-2 (pwr. sup. 1)

    NOTE: LCLK (A9)1TB-3 is not connected to power supply no. 2.
  - (A9)1TB-4, 2TB-4, 3TB-4, 4TB-4 and 5TB-4 to processor ground bus.
  - Black wires from (A9)2TB-3, 3TB-3, 4TB-3, 5TB-3 (+15v) to modules A5, A6, A7, and A8.
  - Yellow wires from (A9)2TB-2, 3TB-2, 4TB-2, and 5TB-2 (-12v to modules A5, A6, A7, and A8.
  - Red wires from (A9)2TB-1, 3TB-1, 4TB-1, and 5TB-1 (+5v) to modules A5, A6, A7, and A8.
- Re-install all printed circuit cards and cables, making sure all connections are secure.
- CHECK and ADJUST the power supply voltages when the processor is first turned on, following the instructions that are given in a later part of this section.

C-1.5 INSTALLING ADDITIONAL MEMORY MODULES

Each expansion module is capable of holding two 10K-character memory modules. When only one of the 10K modules is to be installed, the circuit cards should be placed into card positions M, N, P, S and T. If the second 10K of memory is added, positions U, V, X and Y are also used. The MTM circuit card serves all 20K of memory.

C-1.6 INSTALLING ADDITIONAL IOCs

Generally an MTIOC will occupy partition Ø (in the ACU module). Other IOCs can be placed there, but only if the intent is to control the entire system. External line connections to the MTIOC and Digital Clock are made through the terminal blocks at the rear of the motherboard as shown in the inset of figure C-5. Only those partitions that contain an MTIOC or Digital Clock will have connections to these blocks. The Digital Clock requires connections only to the top terminal block, but the MTIOC requires that both upper and lower blocks are connected. If only one line connection is needed into the MTIOC, the unused terminals must be terminated by a 100 ohm resistor.

All other I/Os are externally connected through front edge connectors. The MDTS IOC cable terminates at a special connection strip at the edge of the processor frame. If additional MDTS IOCs are installed, these terminal strips must also be installed. Place the new strip next to the number on the frame that cooresponds to the partition number of the IOC. Figure C-6 shows the terminal strip installation and cable entry for the MDTS or MIS systems.

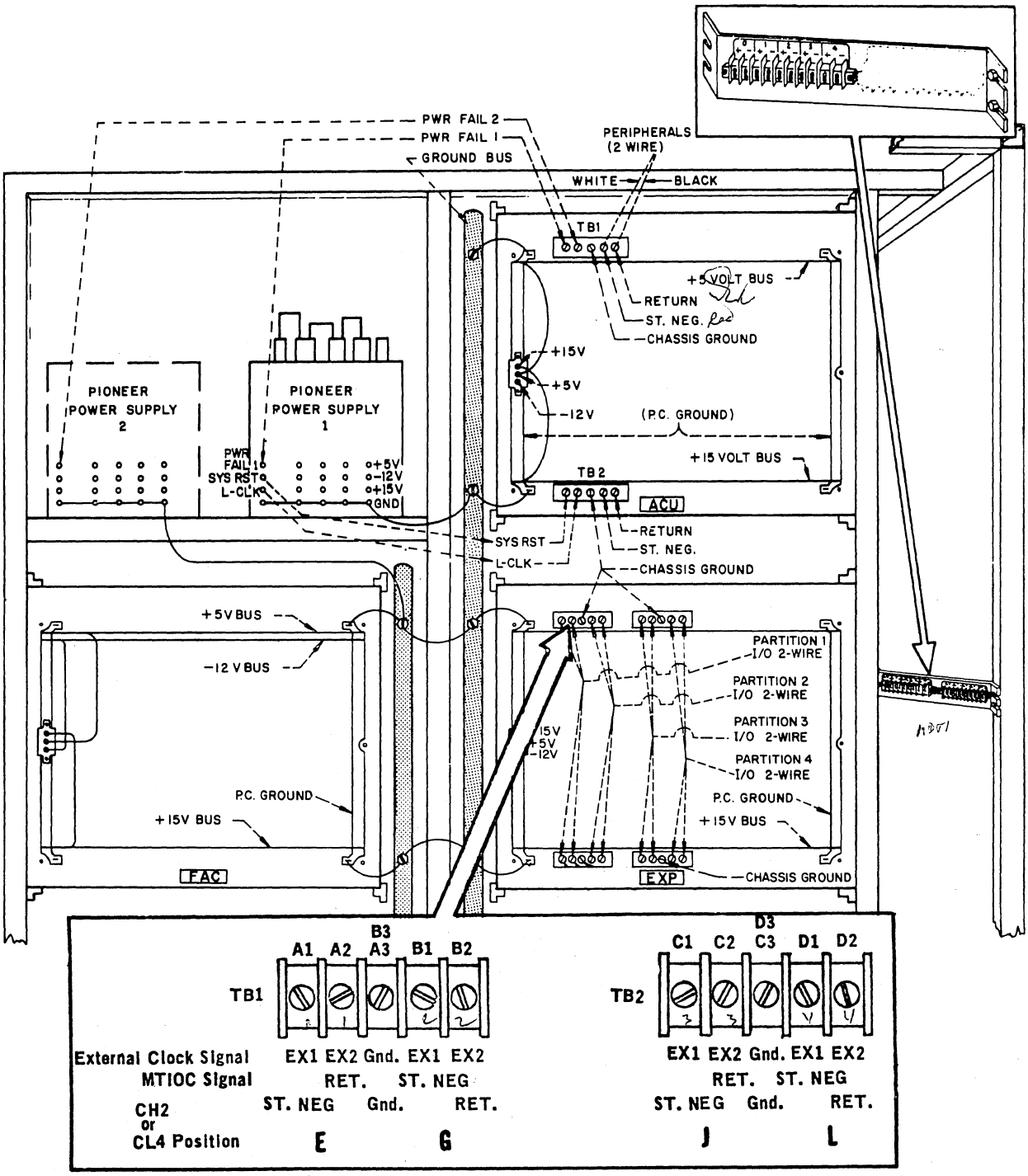


Figure C-5 . PROCESSOR CONNECTIONS

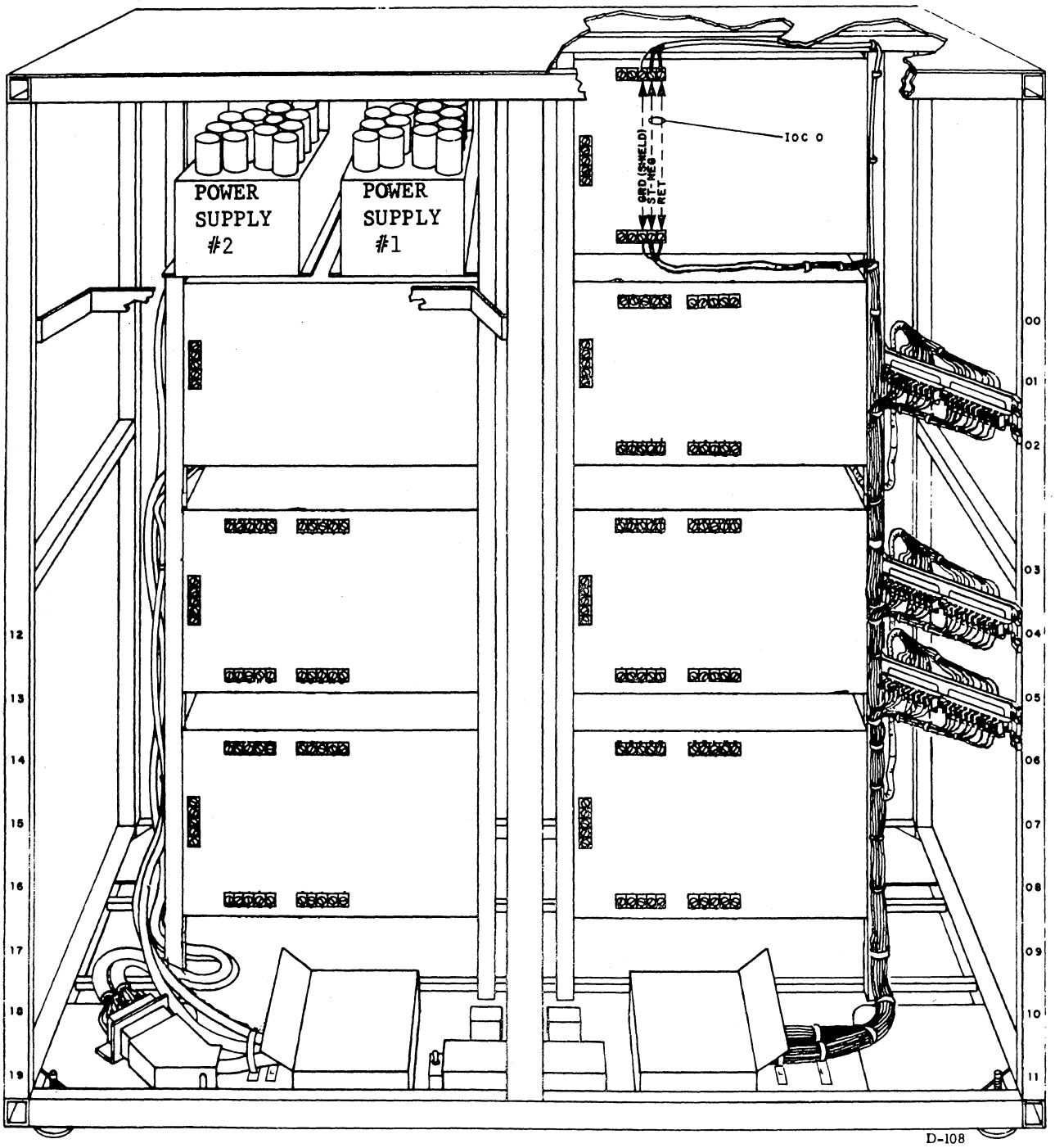


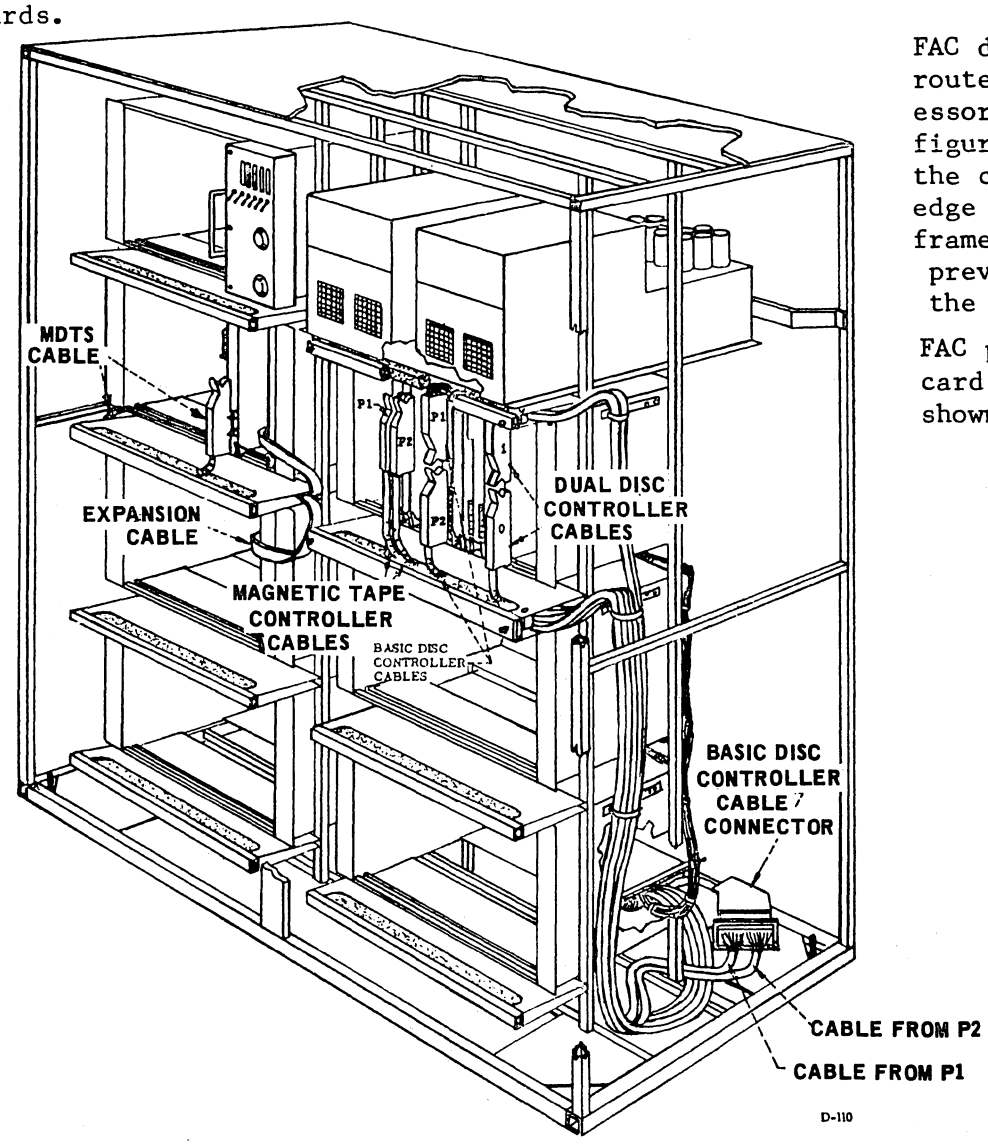
Figure C-6. MODEL 20 PROCESSOR I/O LINE CABLEING

C-1.7 CONNECTING FAC CABLES

Remote connection of FAC devices is given in the instruction manual that deals with the particular device. The illustrations are repeated on the following page for convience.

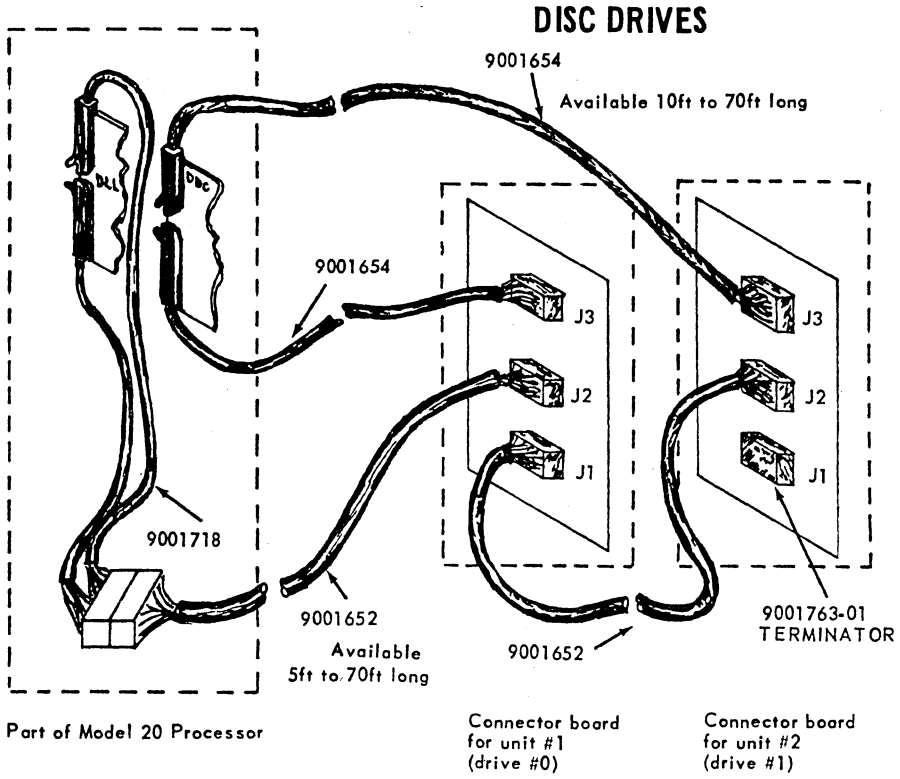
Disc drive cables are "daisy chained" from the basic disc controller to the last unit. The last unit in the daisy chain must contain a terminator assembly in the unused controller cable position (J1). In addition to the basic controller cable, each disc drive has a direct cable connection to one half of one of the dual disc controller (DDC) printed circuit cards. The lower edge-connector of the DDC card should be used first if there are an odd number of disc drives.

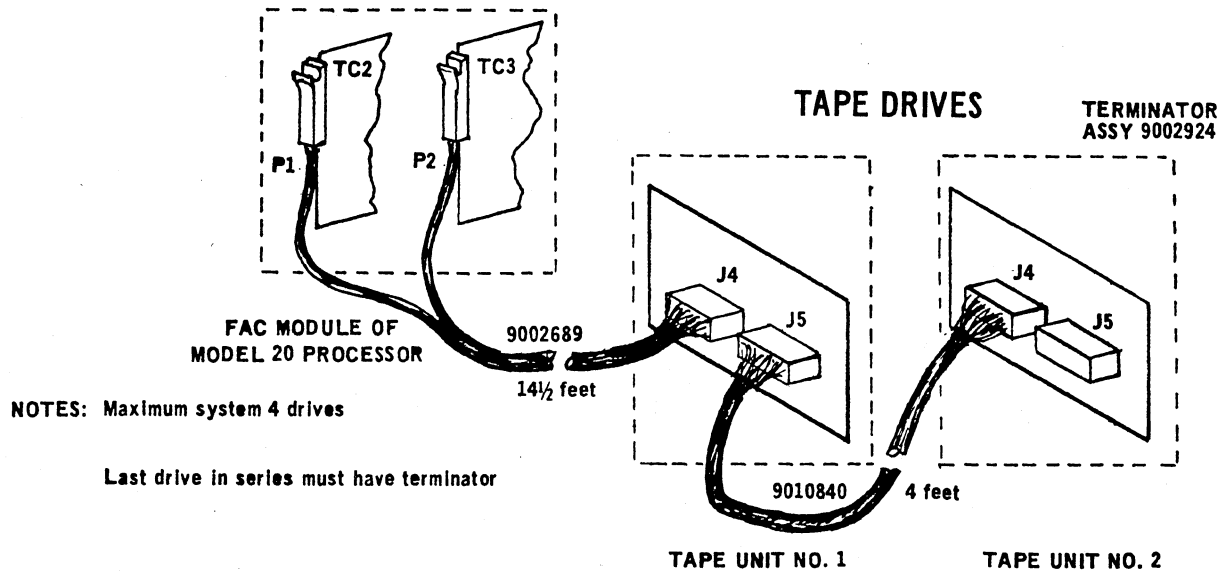
Tape controller cables "daisy chain" similar to the disc drive cables. The last unit in the series (even if only one tape drive is used) must contain a terminator assembly in the unused connector position (J5). Unlike the disc drive, the tape controller cable connects to two adjacent printed circuit cards. The cable is routed from the lower cable channel to the upper edge-connectors on the TC2 and TC3 cards.



FAC device cables are routed within the processor as shown in the figure. Be sure that the cable ties at the edge of the processor frame are secured to prevent any strain on the card connections.

FAC printed circuit card positions are shown in figure C-2.


DISC DRIVES
9001654
Available 10ft to 70ft long
DLL
DDC
9001654
J3
J2
J1
J3
J2
J1
9001718
9001652
Available
5ft to 70ft long
9001652
9001763-01
TERMINATOR
Part of Model 20 Processor
Connector board
for unit #1
(drive #0)
Connector board
for unit #2
(drive #1)


TC2
TC3
P1
P2
TAPE DRIVES
TERMINATOR
ASSY 9002924
J4
J5
J4
J5
FAC MODULE OF
MODEL 20 PROCESSOR
9002689
14½ feet
NOTES: Maximum system 4 drives
Last drive in series must have terminator
9010840
4 feet
TAPE UNIT NO. 1
TAPE UNIT NO. 2

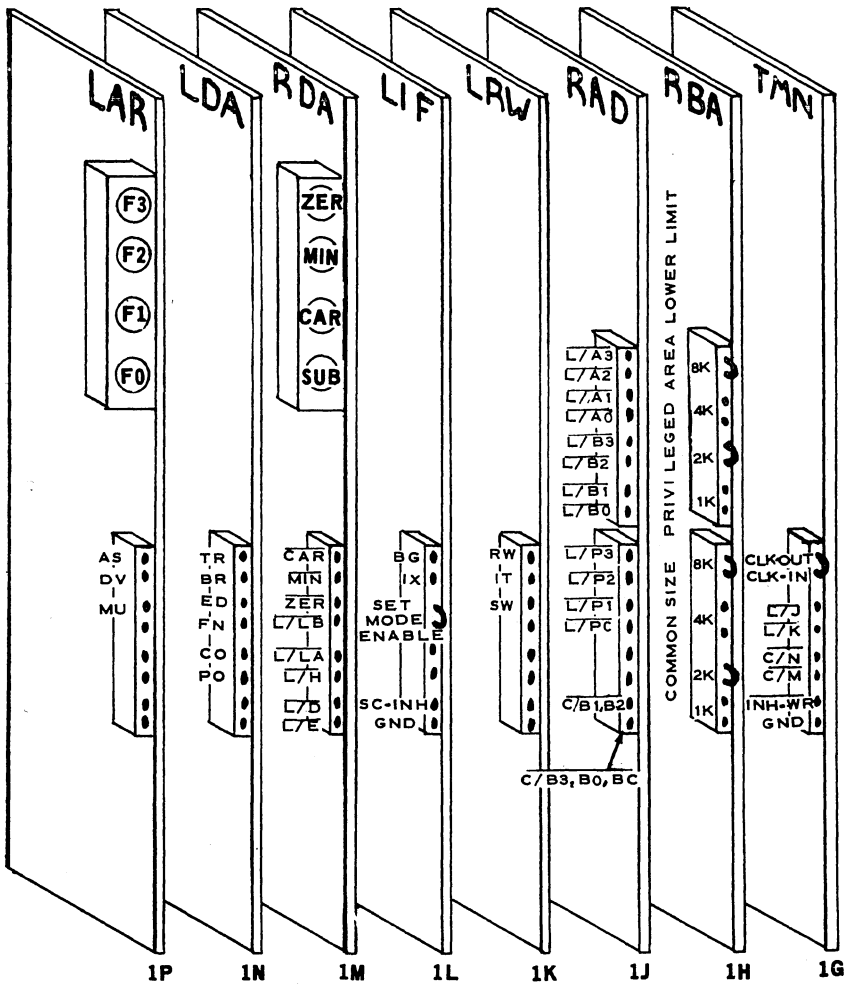
C-1.8 PATCHING

After installing, and before testing the system, the internal hardware patches must be installed to set the common area size, priveleged area, and memory size for partitions. Memory sizes are a system consideration, and must be regulated to the overall system requirements.

The figure below shows the options that are available within the ACU section of the processor. The patching that is shown in the example allows partition zero to control program through the SET MODE option, the size of the common area is 10K, and there is no privileged area. Notice that the privileged area lower limit is in reality the upper limit of the non-privileged area in commom memory.

NOTE

The CLK-IN/CLK-OUT jumper must remain as shown for the processor to operate. Removing this jumper will disable the timing circuits, and consequently the entire processor.



C-1.9 POWER INPUT

The Model 20 Processor and its peripherals are supplied with a standard U-ground line cord that will plug into any UL approved wall outlet. It is recommended that each piece of equipment in the processor room be supplied with a separate 20 amp service. At no time should the processor, or peripherals share an electrical circuit with a noise generating source such as motors, neon signs, or other similar devices.

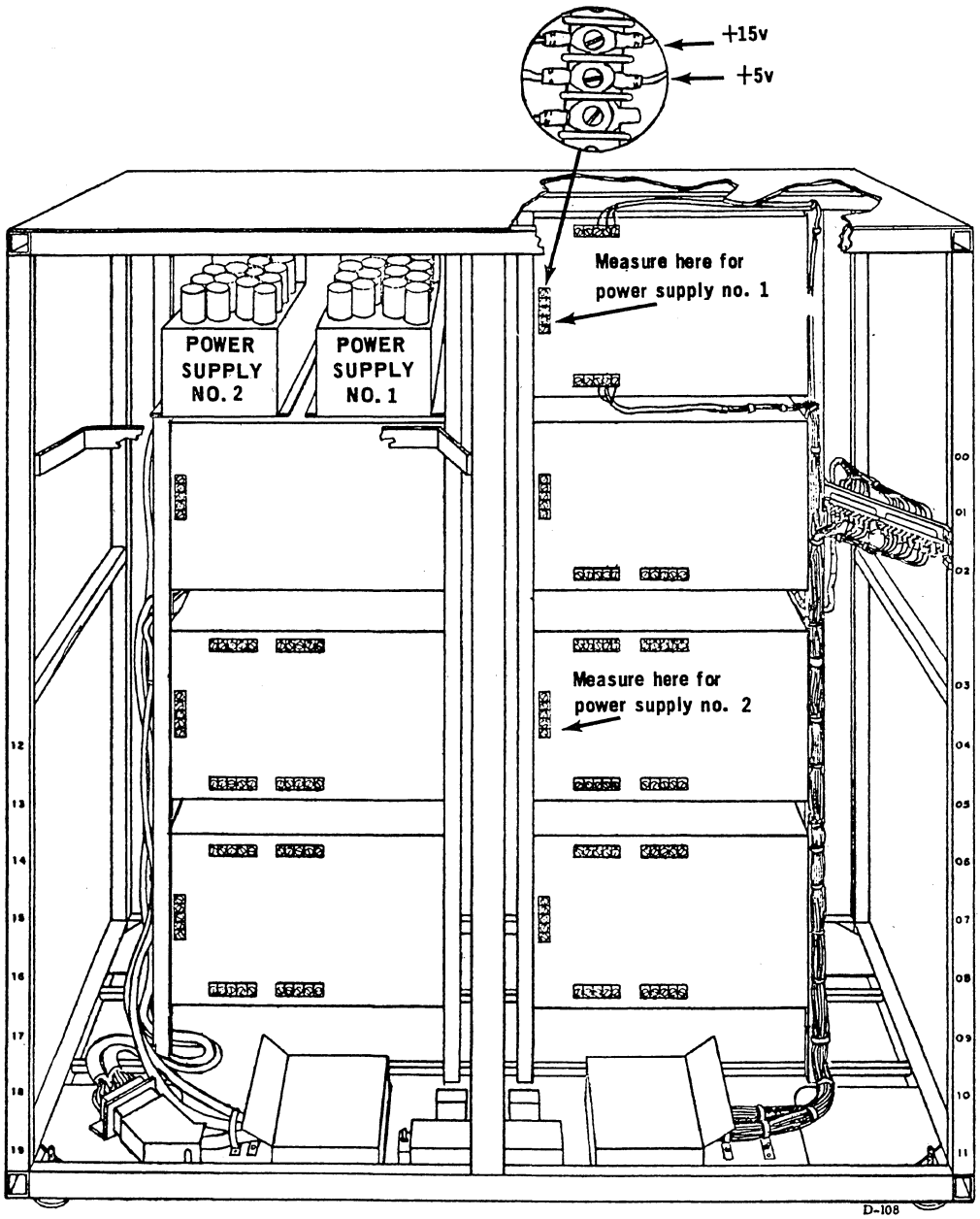
C-1.10 PRE ACTIVATION CHECKS

Before applying power to any of the equipment, verify the following items:

- That all printed circuit cards are in their proper place, and securely seated in the motherboard connector.
- All switches in the system are either OFF, or in a normally inactive position.
- Verify that peripheral device number assignments are correct. Typically, the workstation is device zero to allow "bootstrap" entry.
- Review the service letters for the equipment that is installed. However, unless a service letter specifically directs it, do not modify the equipment until after the initial operational checkout.
- When power is applied to the Model 20 Processor, check the internal dc voltages. Refer to the following paragraphs for voltage specifications; adjust if necessary.

C-1.11 PROCESSOR VOLTAGE ADJUSTMENTS

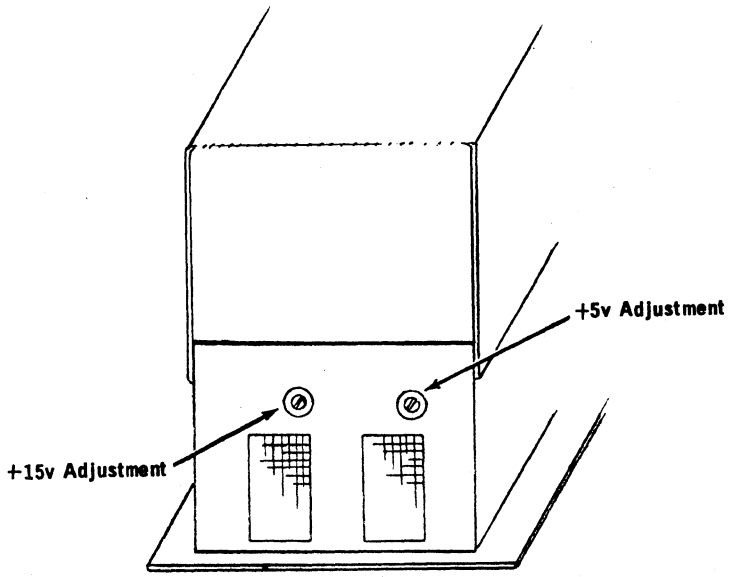
Each of the two power supplies within the Model 20 Processor must be adjusted sepatately, as the two are completely independent with the exception of the RESET lead. All adjustments are made under normal operating load conditions, and the voltage measurements must be made at the places shown on the illustration below. Always use a digital voltmeter for these measurements.



ADJUSTING

Check the voltage first, in the place that is shown in illustration on the opposing page. The voltages must be +5v ± .150v and +15v ± .30v. Adjust either or both voltages if they are not within this range. Adjust as given below.

- Remove the upper-right front panel from the processor (the one that contains the ON/OFF button).
- Using a small screwdriver, snap out the small adjustment covers on the power supply that is to be adjusted (see the figure below).
- Connect a digital voltmeter probe to the +5v terminal at the rear of the ACU module. Connect the digital voltmeter return lead to the processor ground bus connection, NOT to the chassis or frame.
- Adjust the +5v potentiometer (at the front of the power supply) until the digital voltmeter reads between 4.850 and 5.150 volts. Peak the reading at 5.000, or as near as is practical.
- Move the digital voltmeter probe to the +15v terminal at the rear of the ACU module (this is the terminal directly above the +5v connection).
- Adjust the +15v potentiometer (at the front of the power supply) until the digital voltmeter reads between 14.70 and 15.30 volts. Peak the reading as near to 15.00 as is practical.
- Replace the adjustment hole cover buttons, and disconnect the digital voltmeter leads.



POWER SUPPLY FRONT VIEW

D. FIGURES AND TABLES

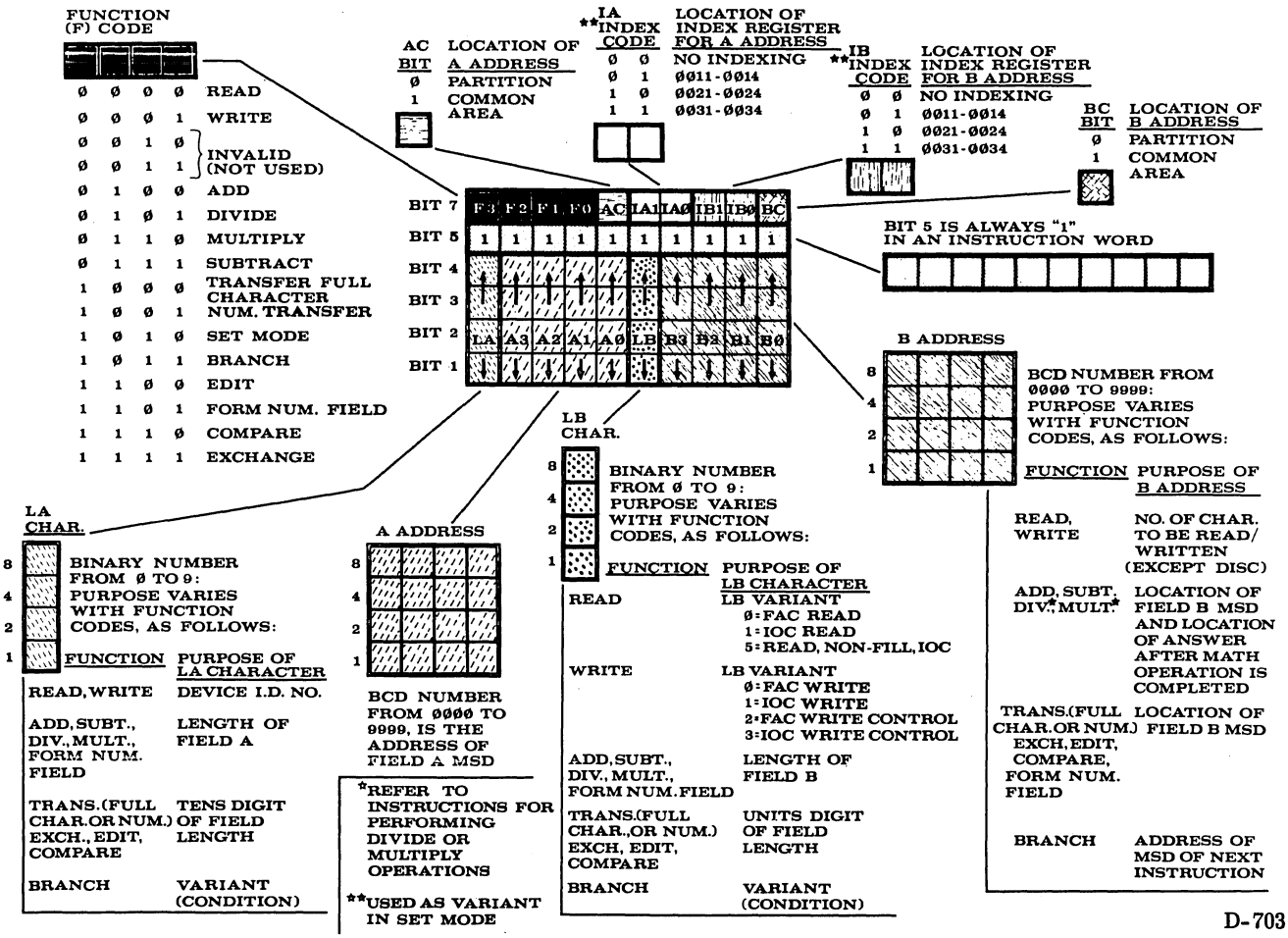


TABLE OF BRANCH VARIANTS

LA OR LB CHARACTER	CONDITION FFs ZERO	MINUS	CARRY	CONDITION CODE MEANING R/W	ARITH OR FN	EDIT	COMPARE
1	0	1	-	ERROR OR FAULT	MINUS	MINUS	LOW
2	1	-	-	NORMAL	ZERO	ZERO	EQUAL
3	0	0	-	FLAG	PLUS	PLUS	HIGH
4	-	1†	1	FAULT	OVERFLOW	-	-
5	-	-	-	UNCONDITIONAL BRANCH			
6††	-	-	-	BRANCH AND TRANSFER			
7††	-	-	-	BRANCH IF SERVICE REQUEST			
8	-	-	-	UNCONDITIONAL BRANCH AND SWITCH			
9,0	-	-	-	NO OPERATION			

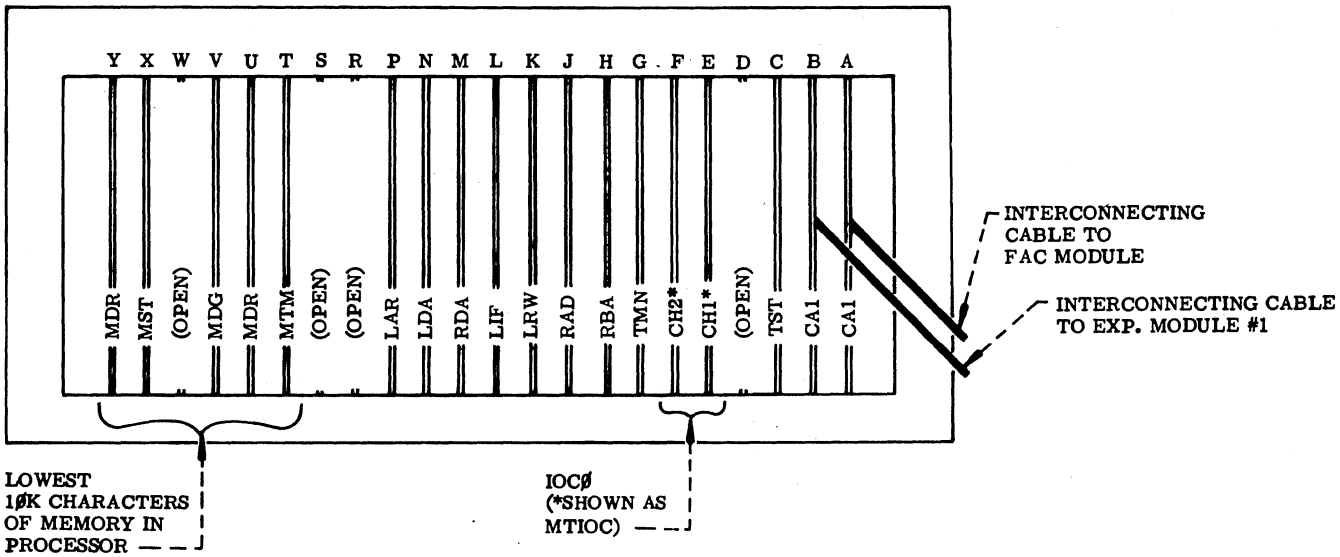
To determine the contents of the condition flip-flops perform one or more branch instructions. Any other instruction resets the condition flip-flops.

†For FAULT condition the MINUS output may be either logic 0 or logic 1; for OVERFLOW condition the MINUS output is logic 1.

††Variants 6 and 7 are used only in LA position of a 10-character Branch instruction. When LA=6, LB may be 1 through 5,8,9, or 0. The LB variant determines the condition that allows the Branch and Transfer to occur. When LA=7, LB must be either 9 or 0.

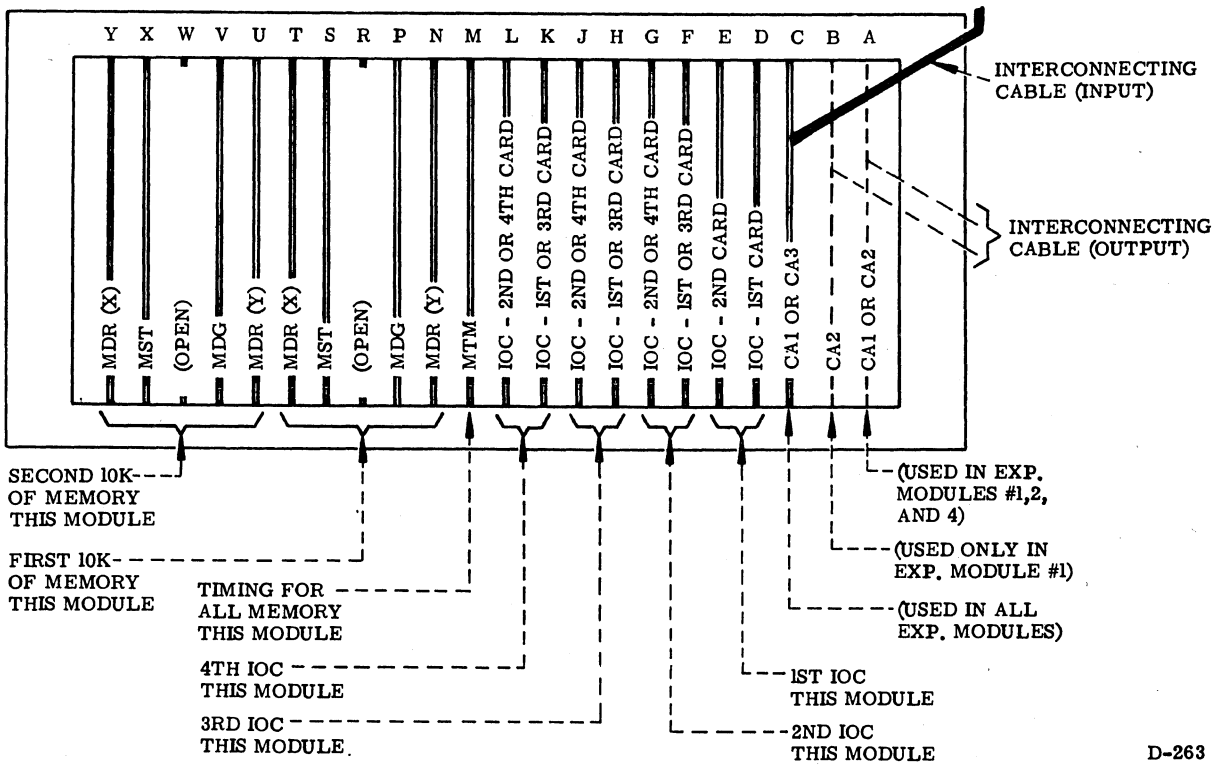
INSTRUCTION WORD SUMMARY

FIGURE D-1



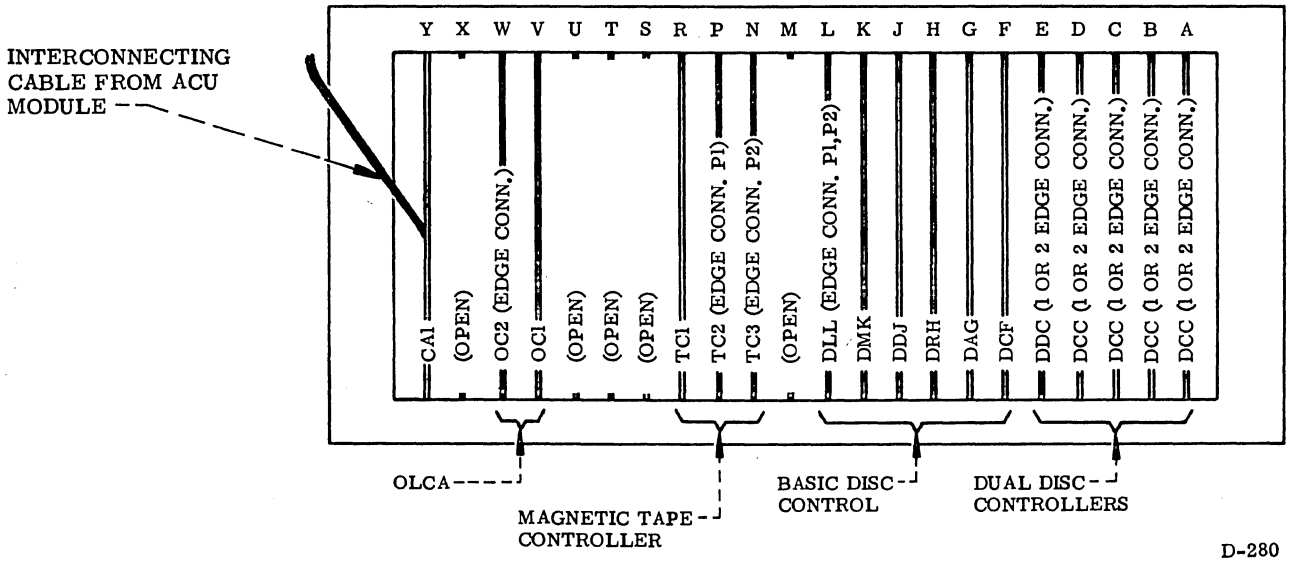
ACU MODULE CIRCUIT CARD LOCATIONS

FIGURE D-2



EXPANSION MODULE CIRCUIT CARD LOCATIONS

FIGURE D-3



FAC MODULE CIRCUIT CARD LOCATIONS

FIGURE D-4

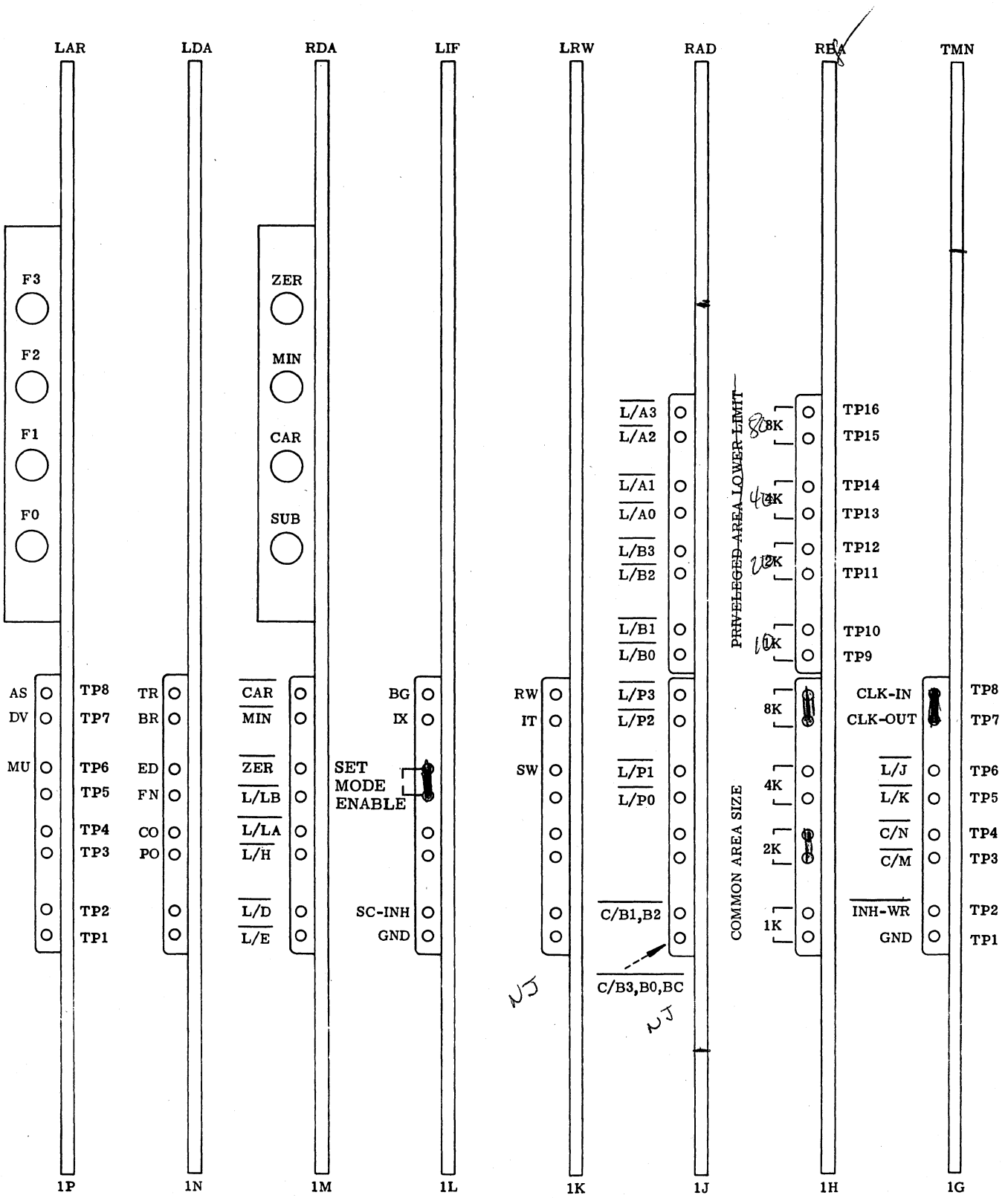
CIRCUIT CARD TYPE	CIRCUIT CARD NAME, CONTENTS, PURPOSE	CARD POSITIONS ACU	EXP	FAC
CA1	Cable connector (Non-amplifying).	A,B	A,C	Y
CA2,CA3	Driver cable connector.	---	A,B,C*	---
TST	Test panel circuit card.	C	---	---
TMN	Timing: J, K, M, and N registers.	G	---	---
RBA	Registers, Base Address: F, IA, IB, Y, and Z registers; X counter.	H	---	---
RAD	Registers, Addressing: A, B, and P registers; FFs for AC, BC, PC bits; Q counter.	J	---	---
LRW	Logic, Read/Write: Decoders for FW, IT, and SW; DISC-ACCESS, PWR-FAIL, and INT-REQ FFs.	K	---	---
LIF	Logic, Instruction Fetch: Decoders for BG and IX; function and state counters; FFs for ACU-LD-RQ, IO-BUSY+PWR-FAIL, INTERRUPT, and FAC-CHECK.	L	---	---
RDA	Registers, Data: LA, LB, D, and H registers; condition FFs (ZERO, MINUS, CARRY), EN-COMP, SUB, E1, and E2 FFs.	M	---	---

*Driver cables connect from Expansion Module #1 to Expansion Modules #2 and #4. CA2 connectors are inserted into Expansion Module #1; CA3, into Expansion Modules #2 and #4.

CIRCUIT CARD TYPE	CIRCUIT CARD NAME, CONTENTS, PURPOSE		CARD POSITIONS ACU	EXP	FAC
LDA	Logic, Data Operations: Decoders for BR, CO, ED, FN, PO, and TR.		N	---	---
LAR	Logic, Arithmetic: Decoders for AS, DV, and MU.		P	---	---
MTM	Memory Timing: MEM-R- line and R-BUS decoders; A through H FFs; LATCH-1 through -5, and -7.		T	M	---
MDR	Memory Driver: (Two required to provide X and Y drive for each 10K-character memory module.) Read/Write source drivers and sink drivers.		U&Y	N&T U&Y	---
MDG	Memory Digit: Inhibit drivers and sense amplifiers for one 10K-character memory module.		V	P,V	---
MST	Memory Stack: Core memory for 10K 6-bit characters.		X	S,X	---
	**********				
DDC	Dual Disc Controller: Control logic for two disc drive units.		---	---	A,B,C, D,E
DCF	Clock, Disc Controller.	Basic DISC CONTROLLER	---	---	F
DAG			---	---	G
DRH	Read/Write, Disc Controller.		---	---	H
DDJ	Data Control, Disc Controller.		---	---	J
DMK	Master Disc Controller.		---	---	K
DLL	Line Disc Controller.		---	---	L
TC1		MAGNETIC TAPE CONTROLLER	---	---	R
TC2			---	---	P
TC3			---	---	N
OC1		ON-LINE COMMUNICATION ADAPTER	---	---	V
OC2			---	---	W
	**********				

CIRCUIT CARD TYPE	CIRCUIT CARD NAME, CONTENTS, PURPOSE	CARD POSITIONS ACU	EXP	FAC
CH1	MULTI-TERMINAL IOC (MTIOC)	E	D,F,H, or K	---
CH2		F	E,G,J, or L	---
CH3	MDTS IOC	E*	D,F,H, or K	---
CH4		F*	E,G,J, or L	---
CH5	SYNCHRONOUS COMMUNICATIONS ADAPTER (SCA1 without CH7 card; SCA2 with CH7 card. The CH7 card adds automatic dialout capability.)	---	D,F,H or K	---
CH6		---	E,G,J or L	---
CH7		---	D,F,H or K	---
CH8		---	E,G,J, or L	---
CL3	DIGITAL CLOCK	E*	D,F,H, or K	---
CL4		F*	E,G,J, or L	---
IO1	COLLECTADATA 30 IOC	D*	D,F,H, or K	---
IO2		F*	E,G,J, or L	---
TA1	ASYNCHRONOUS TERMINAL ADAPTER (ATA) May include CH7 card for automatic dialout capability.	E*	D,F,H, or K	---
TA2		F*	E,G,J, or L	---
(CH7)		---	(F,H, or K)	---
AC1	ASYNCHRONOUS COMMUNICATION ADAPTER (ACA) May include CH7 card for automatic dialout capability.	---	D,F,H, or K	---
AC2		---	E,G,J, or L	---
AC4		---	E,G,J or L	---

*Normally, the ACU module (partition Ø) will contain an MTIOC. However, other IOCs may be installed in the ACU module unless there are more than two circuit cards.



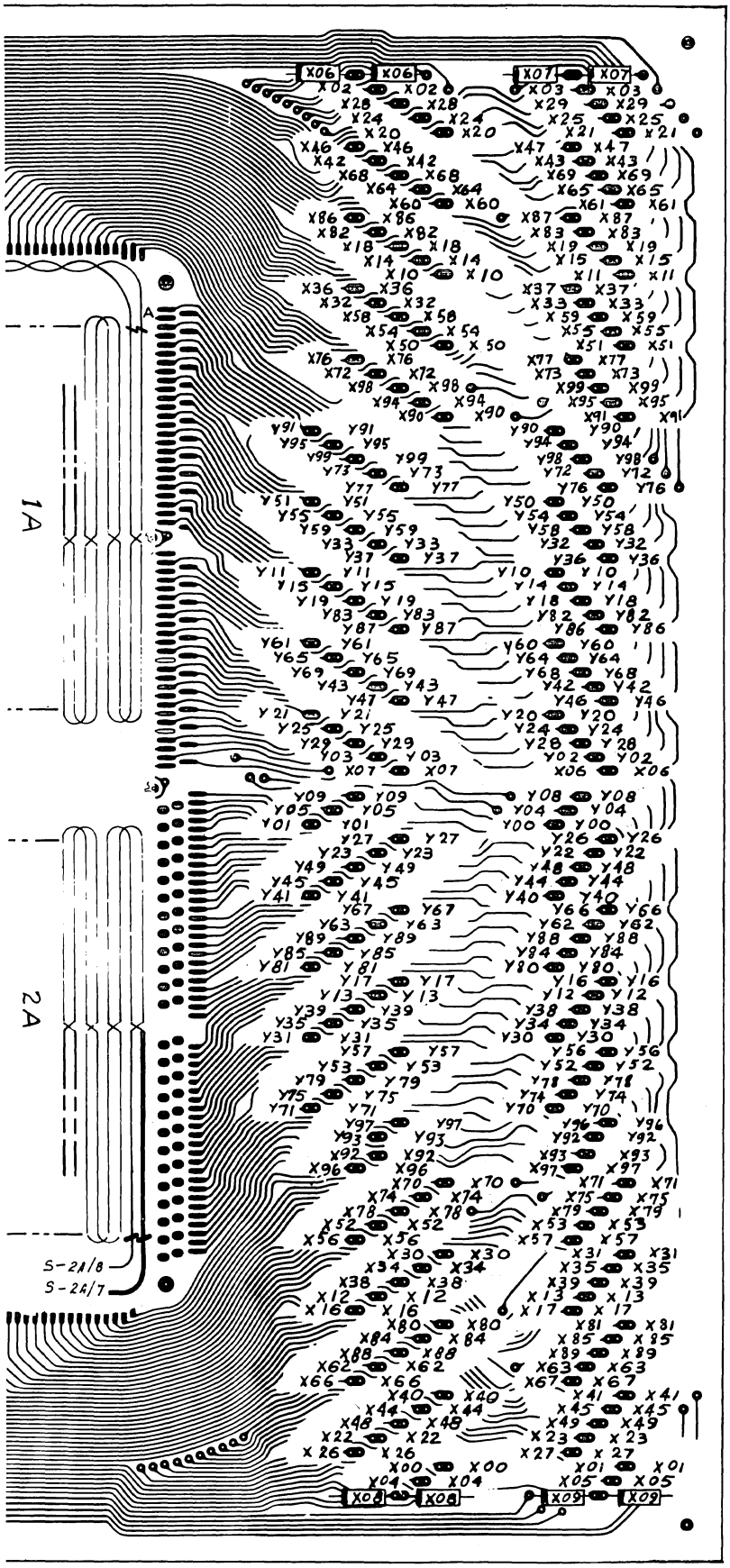
TEST POINT LOCATIONS
ACU MODULE

D-623

FIGURE D-4

MEMORY DIODE LOCATIONS

FIGURE D-5



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CAUTION: PRELIMINARY - For Information Only - Under No Circumstances should this information be used as a basis for installing any equipment.

E. ENVIRONMENTAL REQUIREMENTS

1. GENERAL REQUIREMENTS

(1) Operating temperature range: 60°F to 90°F.
(2) Operating relative humidity range: 20% to 80%.
(3) Primary supply voltage: 105 ± 10%, 115 volts ± 10%, or 120 volts ± 10% at 47-63 Hz.

NOTE: A 2:1 stepdown transformer is planned for use in machines to be installed outside the U.S.A.

2. APPROXIMATE POWER DISSIPATIONS

(1)	Basic Processing Unit	700 watts
(2)	Memory Timing Unit	4 watts
(3)	10K Core Memory	15 watts
(4)	I/O Channel (Type 1 or 2)	15 watts
(5)	MDTS I/O Channel	15 watts
(6)	Basic Disc Controller	45 watts
(7)	Dual Disc Controller	5 watts
(8)	Supplementary Power Supply	500 watts
(9)	Interconnecting Cable with Drivers	5 watts
(10)	Expansion Module	0 watts
(11)	FAC Module	0 watts
(12)	Interconnecting Cable	0 watts

Power dissipation information is not yet available for other units to be mounted within the CPU cabinet. In any case, the maximum dissipation will be limited by the power supply rating to no more than 1800 watts.

3. FIRE PROTECTION

The equipment will be installed domestically in compliance with the National Fire Protection Association's Standard for the Protection of Electronic Computer/Data Processing Equipment (NFPA No. 75-1968). This standard requires the use of disconnecting means at exit doors which disconnect power to all electrical equipment, other than lights, in that room. This disconnecting means must also disconnect the ventilation system serving the room if it is a data processing (i.e., computer) room only.

4. THIRD WIRE GROUND

A third wire ground must be provided in the power distribution system. This third wire should provide a single, common grounding point for all central system equipment (i.e., CPU, Disc Files, and magnetic tape drives). The current-carrying capacity of this third wire will be specified by the controlling electrical code and will have to equal that of the two-wire power distribution circuit it accompanies.

REFERENCE SECTION F CONTENTS

INTRODUCTION

The Algorithms are a detailed listing of the logic actions within each state of the ACU. A state, as defined here, is the unique intersection of a function and a step, and is sometimes subdivided by the Q counter into (sub) steps within a state. In certain states, minor actions may not be included, but in all cases the key conditions are given for logic decisions.

The Algorithms are organized by function, and progressive steps within a function. The column headings on each page are explained below. The overall ACU block diagram is useful as an auxilliary aid when reading the state charts (Algorithms).

ENTRY - the step and/or function from which a jump could have been made to the state under consideration. If no state or function is listed, entry is made only from the preceding step.

STEP - the decoded step number.

OPERATION - a plain English description of the action taking place. Because of space limitations, the description is abbreviated.

SIGNALS - a list of actions taken in the step, possible signal combinations, and the alternate action that is taken for these variations. All actions in this column (except those within parentheses) are performed on the PC card listed at the top of the page.

EXAMPLE (from AS 2):

```
B-OUT (bring the B address from the B register to the R bus)
ADDER-TO-S (move the adder contents to the S bus)
WRITE (active signal when ACU is placing data into core)*
B-DECR (decrement the B register one count)
LB-DECR (decrement LB once)

If F3.F2.MINUS (the signal combination - one of four listed)
 11-TO-N (put one bits in both N1 and N2)
```

REMARKS - additional hints to active signals and logic actions that are a direct result of the action listed in the SIGNALS column.

EXITS - a listing of all possible jumps. If no exits are listed, the next step in order must be performed. Many jumps repeat a short series of steps until increment or decrement allows a jump qualification to another function.

Prefix letters are used in some cases, and these are defined below.

D/ - the enable input of a D type flip-flop.
P/ - preset, or dc set, a flip-flop.
C/ - clear, or dc reset, a flip-flop.
T/ - toggle, or clock pulse, to a register or flip-flop.
L/ - load, such as parallel load a register.
J/ - jump to another function and/or step.

* READ and WRITE in the state charts appear to be reversed. However the strict definition of "the ACU READS, or the ACU WRITES" also applies here.

SWITCH (SW)

LOGIC CARD: LOGIC READ/WRITE (LRX)
LOCATION: 1K
FUNCTION CODE BUFFER (0011) SW 1 of 2

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
BG 1 BG 2 BR 5 RW 9 RW 1Ø RW 11 RW 12 RW 16 Step 1	Ø	Transfer P to M,N	CONDS-TO-S R-TO-S If (Q=Ø): P-LIM-TO-S P-INCR Ø1-TO-N	CONDS-TO-S: P-OUT (R-TO-S)($\overline{Q=Ø}$): L/N Q=Ø: P-LIM Q=1: P3, Carry Q=2: P2, Minus Q=3: P1, ZERO Q=4: PØ, PC (PØ=1) = Partition Inactive	
	1	Store P in Core	WRITE Q-INCR If $\overline{\text{CHECK}}$: X-OUT If CHECK: 4Ø-OUT If ($\overline{Q=4}$): SC-DECR	X-OUT or 4Ø-OUT gives Q-OUT (P5 in zone bits)	Step Ø
START	2	Detect Power Failure	If PWR-FAIL: SC-INH	Upon detection of power failure, the ACU is held in this state. System reset starts here. (Clears Q,F2,X and FAC-CHECK)	
	3	A to P for FAC	If F2: A-OUT R-TO-S L/P Q-INCR SC-INH If (Q=4): LOAD-FAC J/INTERRUPT	F2 = FAC BUSY Q=Ø: -- Q=1: A3 to P3 Q=2: A2 to P2 Q=3: A1 to P1 Q=4: AØ to PØ AC to PC A5 to P5 LOAD-FAC: Releases FAC DISC CONTROLLER: If ON CYLINDER.FAULT: J/A=10 After FAC Strobe	IT Ø

SWITCH (SW)

LOGIC CARD: LOGIC READ/WRITE (LRX)
LOCATION: 1K
FUNCTION CODE BUFFER (0011) SW 2 of 2

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
Step 5	4	Increment Partition Number	C/TIMEOUT C/Disc Access-FF If $\overline{\text{INH-SW}}.\overline{\text{CHECK}}$: X-INCR	C/TIMEOUT: Clear F Clear IA,IB Load Z X-INCR: X-Incr H-Incr	
	5		If $\overline{\text{IO-SEL}}$: SC-DECR		Step 4
IT 8	6	Load P & Conditions	X-OUT READ L/P L/CONDS Q-INCR C/FAC-DONE If (Q=4): C/M If $\overline{(Q=4)}$: SC-INH	Q=Ø: -- Q=1: P3, Carry Q=2: P2, Minus Q=3: P1, Zero Q=4: PØ,PC,P5 (PØ=Ø) = Partition Active	
	7	Exit for normal Switching Check for FAC Done and Power Failure	J/BEGIN If F2: FAC-TO-S STATUS-IN LOAD-FAC If CHECK: P/LD-REQ	M1 = Error $\overline{\text{M2}}$ = Flag $\overline{\text{M3}}$ = Fault M4 = Repeat if Error F3 indicates PWR FAIL STATUS-IN: If M1 + $\overline{\text{M3}}$ + F2.F3: P/MINUS C/ZERO If (M1.M4 + F3.(LA=Ø).F2).3T: P1-DECR If $(\overline{\text{M3}}.\overline{\text{F3}})$: P/CARRY If M2: C/ZERO P/LD-REQ resets CHECK in the IOC	BG Ø

BEGIN (BG)

LOGIC CARD: LOGIC INSTRUCTION FETCH (LIX)
LOCATION: 1L
FUNCTION CODE BUFFER (1010) BG 1 of 4

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
AS 5 BR 5 CO 3 CO 4 DV 5 DV 1Ø ED 5 FN 1 IT 2 MU 15 RW Ø RW 3 SW 7 TR 3 Step 5 Step 6 BG 5	Ø	Test for Interrupt	C/DH C/F If INTERRUPT: X-INCR J-INTERRUPT If FAC-CHECK.3T: P/CHECK	C/DH.2T: Clear D Clear H C/F: Clear F Clear IA,IB LOAD Z X-INCR: X-Incr H-Incr	IT Ø
	1	Test for Power Failure or IO Busy	C/FAC-CHECK If IO-BUSY + PWR-FAIL + INH-INSTR: J/SWITCH		SW Ø
	2	Test for Load Request	ØØØ1-TO-M If ACU-LD-REQ: C/P P/F3 J/Read, Write If CHECK.$\overline{\text{ACU-LD-REQ}}$: J/SWITCH	C/P: Clear P Clear A Clear J Clear LA Clear B3,B2,BØ Clear Conditions Load B1 L/K L/LB	RW Ø SW Ø

BEGIN (BG)

LOGIC CARD: LOGIC INSTRUCTION FETCH (LIX)
LOCATION: 1L
FUNCTION CODE BUFFER (1010)

BG 2 of 4

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS

	3	Fetch Characters Ø-4 of Instruction	P-OUT
			READ
			L/F (3T)
			L/A
			L/B (3T)
			Q-INCR
			P-INCR
			
			If $\overline{(Q=4)}$: SC-INH
			If M > 9·3T: P/$\overline{CHECK}$
			If (Q=4)·$\overline{M > 9}$·$\overline{CHECK}$·
			E1·(BR-OK):J/BRANCH
			If (Q=4):INST-STOP(3T)
			: STOP
			If Q=Ø: $\overline{L/E1}$
			If Q=4·$\overline{E1}$·$\overline{CHECK}$: C/ID
			J/TRANSFER
			J/STEP 5
				Q=Ø : L/E1
				
				(Q=Ø).Load F:
				Load LA,J,LB,F3
				
				Q=1: Load A3,B3,F2
				
				Q=2: Load A2,B2,F1
				
				Q=3: Load A1,B1,FØ
				
				Q=4: Load AØ,BØ
				AC,BC
				A5,B5
				$\overline{E1}$=Indirect Addressing
					
					TR 5
					BR Ø

TR 7	4
	
	(Cont)
		Fetch Characters 5-9 of Instruction	P-OUT
			READ
			L/I
			L/B (3T)
			Q-INCR
			P-INCR
			
			If $\overline{(Q=4)}$: SC-INH
			If M > 9·3T: P/$\overline{CHECK}$
			If (Q=4)·$\overline{M > 9}$·$\overline{CHECK}$·
			E1·(BR-OK):J/BRANCH
			If (Q=4): INST-STOP(3T)
			
			If Q=Ø: $\overline{L/E1}$
			If Q=4·$\overline{E1}$·$\overline{CHECK}$: P/ID
			J/TRANSFER
			J/STEP 5
				(Q=Ø).Load I:
				Load LB,K,IA1
				
				Q=1: Load B3,IAØ
				
				Q=2: Load B2,IB1
				
				Q=3: Load B1,IBØ
				
				Q=4: Load BØ,BC,B5
					
					TR 5
					BR Ø

BEGIN (BG)

LOGIC CARD: LOGIC INSTRUCTION FETCH (LIX)
LOCATION: 1L
FUNCTION CODE BUFFER (1010) BG 3 of 4

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
	4 (Cont)	Set Mode	If $\overline{IAZ}$: D/SM-INHSW If F3.$\overline{F2}$.F1.$\overline{F\emptyset}$. (Q-4).$\overline{CHECK}$. PARTITION=$\emptyset$. E-SM: T/SM-INHSW If F3.$\overline{F2}$.F1.$\overline{F\emptyset}$. (Q≠4).$\overline{CHECK}$. PARTITION-$\emptyset$ E-SM.$\overline{IBZ}$: SYS-RES	F3.$\overline{F2}$.F1.$\overline{F\emptyset}$=Set Mode E-SM: Jumper on LIF. (Enables Set Mode) SYS-RES to I/O & Main Memory Only, Not to ACU.	
TR 7	5	Set Mode & Test for Indexing	If (F=BRANCH + F3.$\overline{F2}$.F1.$\overline{F\emptyset}$. E-SM): J/BEGIN If $\overline{(F=BRANCH)}$. $\overline{(F3+F2+F1+F\emptyset)}$ $\overline{(IAZ+IBZ)}$: J/INDEX		BG $\emptyset$ IX $\emptyset$

BEGIN (BG)

LOGIC CARD: LOGIC INSTRUCTION FETCH (LIX)
LOCATION: 1L
FUNCTION CODE BUFFER (1010) BG 4 of 4

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS

IX 3	6	Jumps for Arith. Op. or Invalid Opcodes or Exchange or Indirect Address	C/CONDS
			C/DH
			
			If (F2.$\overline{F1}$.FØ+ (F3.F2)).$\overline{CHECK}$:
			J/Positioning
			MATH INST-STOP (3T)
			
			If ($\overline{F2}$.F1.$\overline{FØ}$+CHECK):
			J/BEGIN
			P/CHECK
			
			If (F3.F1.FØ+$\overline{F2}$.F1.FØ):
			J/Transfer
			DATA MANIPULATION
				C/CONDS:
				Clear MINUS
				Clear SUBTRACT
				Preset ZERO
				
				C/DH:
				Clear H
				Clear D
				
				NOTE:
				CARRY follows SUBTRACT
				
				Arith. Op:
				4,5,6,7 or 13(FN)
				
				Invalid Op:
				2, (10)
				Address Transfer : 3
				
				Exchange: 15
					PO Ø
					BG Ø
					TR Ø

	7	Strobe F to Function Counter	F3,F2,F1-To-FC	RW: Ø,1 TR: 8,9 ED: 12 CO: 14	RW Ø TR Ø ED Ø CO Ø

INTERRUPT (IT)

LOGIC CARD: LOGIC READ/WRITE (LRX)
LOCATION: 1K
FUNCTION CODE BUFFER (0010) IT 1 of 4

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
BG Ø SW 3 Step 1 Step 3 Step 6 Step 13	Ø			Step for timing considerations	
	1	Service IOC Interrupts Poll Partitions	If INT-REQ: J/STEP 5 If $\overline{\text{INT-REQ}}.\overline{\text{D2}}$: X-INCR SC-DECR	X-INCR: X-Incr H-Incr D2 indicates D & H Count = 2Ø	 Step 5 Step Ø
	2	Trap for FAC not Busy	If $\overline{\text{F2}}$: J/BEGIN	F2 indicates FAC BUSY	 BG Ø
	3	Traps for Power Fail and FAC Done	C/DH If PWR-FAIL: P/F3 TERM-TRANS If $\overline{\text{PWR-FAIL.}}$ $\overline{\text{STATUS-RDY}}$: X-INCR J/INTERRUPT	C/DH.2T: Clear D Clear H F3 Indicates PWR-FAIL	 IT Ø
	4	Exit for Power Fail and FAC	P/FAC-DONE Q-INCR J/STEP 7		 IT 71

INTERRUPT (IT)

LOGIC CARD: LOGIC READ/WRITE (LRX)
LOCATION: 1K
FUNCTION CODE BUFFER (0010) IT 2 of 4

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
Step 1	5	Recall B (into A)	X-OUT 1ØØ-OUT READ L/A Q-INCR If (Q=Ø).3T: L/J If $\overline{(Q=4)}$: SC-INH	Q=Ø: B4 to J Q=1: B3 to A3 Q=2: B2 to A2 Q=3: B1 to A1 Q=4: BØ to AØ BC to AC B5 to A5	
	6	Test for Last Character	A-DECR If BORROW + J3-TERM-RD: P/LAST If J3-TERM-RD: J/INTERRUPT C/INT		IT Ø
Step 4 Step 8	7	Transfer A to K,E	If $\overline{\text{FAC-DONE}}$: A-OUT If FAC-DONE: B-OUT R-TO-S L/K L/E If (Q=Ø): J-TO-S Ø1-TO-N	R-TO-S.$\overline{Q=Ø}$: L/N Q=Ø: J to K,Ø1 to E Q=1: A3 to K Q=2: A2 to K Q=3: A1 to K Q=4: AØ to K	

INTERRUPT (IT)

LOGIC CARD: LOGIC READ/WRITE (LRX)
LOCATION: 1K
FUNCTION CODE BUFFER (0010) IT 3 of 4

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
	8	Store B	X-OUT 1ØØ-OUT K-TO-S E-TO-S WRITE Q-INCR If $\overline{(Q=4)}$: SC-DECR If (Q=4):FAC-DONE: J/SWITCH J/STEP 6	(B5 in zone bits)	 Step 7 SW 6
	9	Recall A (into A)	X-OUT 2ØØ-OUT READ L/A Q-INCR If $\overline{(Q=4)}$: SC-INH	Q=Ø: --- Q=1: Load A3 Q=2: Load A2 Q=3: Load A1 Q=4: Load AØ,AC,A5	
	1Ø	Transfer Data Between Core and IOC	A-OUT A-INCR Q-INCR If J1 + OUT-REQ: READ If J1 + OUT-REQ: LOAD-IOS (3T) If $\overline{J1}.\overline{OUT-REQ}$: IOS TO-MN WRITE If ACU-LD-REQ: P/N1	J1: Send data to IOC $\overline{J1}$: Obtain data from IOC	

INTERRUPT (IT)

LOGIC CARD: LOGIC READ/WRITE (LRX)
LOCATION: 1K
FUNCTION CODE BUFFER (0010) IT 4 of 4

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
Step 12	11	Transfer A to K & E	A-OUT R-TO-S L/K L/E	R-TO-S.$\overline{Q=\emptyset}$: L/N Q=1: A3 to K Q=2: A2 to K Q=3: A1 to K Q=4: AØ to K,AC to E	
	12	Store A	X-OUT 2ØØ-OUT K-TO-S E-TO-S WRITE Q INCR If ($\overline{Q=4}$): SC-DECR	(A5 in zone bits)	Step 11
	13	Service Next Partition	C/INT J/INTERRUPT		IT Ø

READ/WRITE (RW)

LOGIC CARD: LOGIC READ/WRITE (LRX)
LOCATION: 1K
FUNCTION CODE BUFFER (0000) RW 1 of 4

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
BG 2 BG 7	Ø	Check FAC Protect Character	X-OUT 2ØØ-OUT READ If $\overline{K1}$.$\overline{FAC\text{-}INH}$: J/STEP 1Ø If $\overline{K1}$.FAC-INH: J/BEGIN	$\overline{K1}$ = FAC Instruction	Step 1Ø BG Ø
	1	Recall (B4) Check for Active Bits	X-OUT 1ØØ-OUT READ B-DECR If ($\overline{M4}$.$\overline{M2}$) + (F3.M4): J/STEP 4	F3 = Load in Progress M2.$\overline{M4}$ = Load Active M4 = I/O Active	Step 4

	2	IOC Sends Status to Condition FF's	IOS-TO-MN
			STATUS-IN
			LONG-CYCLE
				M1 = Error
				$\overline{M2}$ = Flag
				$\overline{M3}$ = Fault
				M4 = Repeat if Error
				
				STATUS-IN:
				
				If M1 + $\overline{M3}$ + F2.F3:
				P/MINUS
				C/ZERO
				
				If (M1.M4 + F3.(LA=Ø).F2.3T:
				P1-DECR
				
				If ($\overline{M3}$.$\overline{F3}$):
				P/CARRY
				
				If M2:
				C/ZERO	

	3	Erase I/O and Load Active Bits Status Exit	X-OUT 1ØØ-OUT C/M Ø1-TO-N WRITE J/BEGIN If F3.$\overline{MINUS}$: C/LD-REQ	(B4 = ØØØØ)= No Active Bits	BG Ø

READ/WRITE (RW)

LOGIC CARD: LOGIC READ/WRITE (LRX)
LOCATION: 1K
FUNCTION CODE BUFFER (0000) RW 2 of 4

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
Step 1	4	Send Device Number & Command to IOC	J-TO-S IOF-TO-S LOAD-IOS (3T) Q-INCR	J-TO-S Device # IOF-TO-S: If $\overline{F3 + LB2}$: 1 to N2 If FØ : 1 to N1	
Step 6	5	Transfer A to M,N	A-OUT R-TO-S	R-TO-S.$\overline{Q=Ø}$: L/N	
	6	Store A	X-OUT 2ØØ-OUT WRITE Q-INCR If ($\overline{Q=4}$): SC-DECR	Q=Ø: -- Q=1: A3 Q=2: A2 Q=3: A1 Q=4: AØ,AC (A5 in zone bits)	Step 5
Step 8	7	Transfer B to M,N	B-OUT R-TO-S If (Q=Ø): ACTVE-TO-S	R-TO-S.$\overline{Q=Ø}$: L/N ACTIVE-TO-S: If F3: 1 to M4 If LB3: 1 to M3 If F3 + LB2: 1 to M2 If FØ: 1 to M1	
	8	Store B	X-OUT 1ØØ-OUT WRITE Q-INCR If ($\overline{Q=4}$): SC-DECR If Q=Ø: 01-TO-N	Q=Ø: B4(Active Bits) Q=1: B3 Q=2: B2 Q=3: B1 Q=4: BØ,BC (B5 in zone bits)	Step 7
	9	IOC Exit	J/SWITCH If F3 + $\overline{ACU-LD-REQ}$: P/IO-BUSY If $\overline{ADR-ERR}$.$\overline{CHECK}$.3T: P1-DECR		SW Ø

READ/WRITE (RW)

LOGIC CARD: LOGIC READ/WRITE (LRX)
LOCATION: 1K
FUNCTION CODE BUFFER (0000) RW 3 of 4

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
Step Ø	1Ø	Send Device Number & Command to FAC Check if Device is Ready	J-TO-S IOF-TO-S FAC-SELECT LOAD-FAC If $\overline{ACK}$: J/SWITCH If ACK.$\overline{LA=Ø+LA=8}$: P/F2 B-DECR J/SWITCH If $\overline{ACK}$.$\overline{CHECK}$. $\overline{ADR-ERR}$.3T: P1-DECR	J-TO-S = Device # IOF-$\overline{TO-S}$: If $\overline{F3 + LB2}$: 1 to N2 If FØ : 1 to N1 LA=Ø+LA=8=Disc/1011 Interface F2 = FAC BUSY DISC CONTROLLER: J/A=Ø AFTER FAC STROBE	SW Ø
	11	Send Disc Unit # to FAC Check if Unit is Ready	B-OUT READ LOAD-FAC B-INCR If $\overline{ACK}$: J/SWITCH If $\overline{ACK}$.$\overline{CHECK}$. $\overline{ADR-ERR}$.3T: P1-DECR	DISC CONTROLLER: J/A=1 AFTER FAC STROBE 16 device numbers possible. M>9 and 5-bit not checked at this time	SW Ø
	12	Send Partition # to FAC Check if Accepted	X-OUT X-TO-S LOAD-FAC If $\overline{ACK}$: J/SWITCH If $\overline{ACK}$.$\overline{CHECK}$. $\overline{ADR-ERR}$.3T: P1-DECR	DISC CONTROLLER: J/A=2 AFTER FAC STROBE	SW Ø

READ/WRITE (RW)

LOGIC CARD: LOGIC READ/WRITE (LRX)
LOCATION: 1K
FUNCTION CODE BUFFER (0000) RW 4 of 4

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
	13	Send Partition # to FAC Again	X-OUT X-TO-S LOAD-FAC	Disc Controller: J/A=3 After FAC Strobe	
	14	Send Disc Address TO FAC	B-OUT READ LOAD-FAC B-INCR Q-INCR If DATA-FAULT.3T: P/CHECK If ($\overline{Q=4}$): SC-INH	Q=Ø:Cyl. Add. to FAC Q=1:Cyl. Add. to FAC Q=2:Cyl. Add. to FAC Q=3:Sec. Add. to FAC Q=4:Sec. Add. to FAC Disc Controller: J/A=4,5,6,7, and 8 After each FAC strobe DATA-FAULT=M>9+$\overline{5\text{-bit}}$	
	15	Set B Address to 1ØØ	ØØØ1-TO-M L/B2 FUNC-INCR	L/B2: Load B2 Clear B3,B1,BØ	
	16	Test for Disc on Cylinder Test for CHECK	B-DECR J/SWITCH LOAD-FAC If ACK.$\overline{\text{CHECK}}$: P/F2 P/Disc Access-FF If $\overline{\text{ACK}}$.$\overline{\text{CHECK}}$. $\overline{\text{ADR-ERR}}$.3T: P1-DECR If ($\overline{\text{ACK}}$.Disc Access-FF.3T)+ CHECK: TERM-TRANS	F2 = FAC BUSY TERM-TRANS: Clear Disc Disc Controller: J/A=9 After FAC Strobe	SW Ø

BRANCH (BR)

LOGIC CARD: LOGIC DATA OPERATIONS (LDX)
LOCATION: 1N
FUNCTION CODE BUFFER (1011) BR 1 of 2

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
BG 3 BG 4	Ø	Test for Branch Variant	If (LA=6): Q-INCR If $(\overline{LA=6}).(\overline{LA=7})$: J/STEP 4	(LA=Ø) = Branch and Transfer (LA=7) = Branch on Service-Request	Step 4
Step 3	1	Read Zone Bits of A	A-OUT READ L/E		

	2	Transfer Poll Cntr or P to M,N	P-OUT
			R-TO-S
			If $(\overline{Q=Ø})$: L/E1
			If (Q=Ø): PCTR-TO-M
			If (Q=4): L/E
				R-TO-S•$(\overline{Q=Ø})$: L/N
				Q=Ø: Poll Cntr to M
				Q=1: P3 to M
				Q=2: P2 to M
				Q=3: P1 to M
				Q=4: PØ to M,PC to N	

	3		A-OUT WRITE Q-INCR A-INCR E-TO-S If (Q=Ø): C/SV-REQ If $(\overline{Q=Ø}).(\overline{Q=4})$: J/STEP 1		Step 1
Step Ø	4	Transfer B to P	B-OUT R-TO-S L/P Q-INCR If (Q=4): C/M If $(\overline{Q=4})$: SC-INH	Q=Ø: -- Q=1: B3 to P3 Q=2: B2 to P2 Q=3: B1 to P1 Q=4: Zero to PØ, BC to PC B5 to P5 R-TO-S•$(\overline{Q=Ø})$: L/N	

BRANCH (BR)

LOGIC CARD: LOGIC DATA OPERATIONS (LDX)
LOCATION: 1N
FUNCTION CODE BUFFER (1011) BR 2 of 2

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
	5	Test for Switch	If (LB=8): J/SWITCH If TIME-OUT: J/SWITCH If $\overline{(LB=8)}.\overline{TIME\text{-}OUT}$: J/BEGIN	(LB=8) = Branch and Switch	 SW Ø BG Ø

TRANSFER (TR)

LOGIC CARD: LOGIC DATA OPERATIONS (LDX)
LOCATION: 1N
FUNCTION CODE BUFFER (1000)

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
BG 6 BG 7 Step 3	Ø	Read B	B-OUT READ L/K L/E	F-bits: 1ØØØ = Transfer (T) 1ØØ1 = Numeric-Transfer (N) 1111 = Exchange (X) ØØ11 = Address Transfer (AT)	
Step 3	1	Read A	A-OUT READ If $\overline{F3}$: L/E1	$\overline{F3}$ = Address Transfer (Move Address)	
	2	Write A into B	B-OUT WRITE B-INCR If $\overline{F3}.\overline{F2}.\overline{FØ}$+F3·LA=Ø.LB=1: E-TO-S If $\overline{F3}$: C/ZERO If $\overline{F3}$.LA=Ø.LB=1·N2: P/MINUS	$\overline{F2}$.FØ = Numeric Transfer P/MINUS qualified by 3T.	

	3	If Exchange Write B into A	A-OUT
			K-TO-S
			E-TO-S
			A-INCR
			LB-DECR
			
			If F2:
			WRITE
			
			If FØ:
			J/STEP Ø
			
			If (LB=Ø):
			LA-DECR
			
			If $\overline{FØ}.\overline{(LA=Ø).(LB=1)}$:
			J/STEP 1
			
			If (LA=Ø).(LB=1):
			J/BEGIN
				F2 = Exchange	Step Ø
					Step 1
					
					BG Ø

TRANSFER (TR)

LOGIC CARD: LOGIC DATA OPERATIONS (LDX)
LOCATION: 1N
FUNCTION CODE BUFFER (1000)

TR 2 of 2

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
Step 5	4	Read B	B-OUT B-INC READ		
BG 3 BG 4	5	Store Indirect Address	X-OUT 2ØØ-OUT Q-INC If $\overline{Q=Ø}$: WRITE If $\overline{Q=4}$: SC-DECR	Q=Ø: skip over A4or B4 Q=1: L/A3 or B3 Q=2: L/A2 or B2 Q=3: L/A1 or B1 Q=4: L/AØ or BØ Q=5: L/AC or BC L/A5 or B5 as zone bits	TR 4
	6	Load A.B+B with Indirect Address	X-OUT 2ØØ-OUT Q-INCR L/B READ If $\overline{ID}$: L/A If Q=4.BR-OK: J/BRANCH INST-STOP If $\overline{Q=4}$: SC-INH	Always load B; Load A if $\overline{ID}$	BR Ø Step 7
	7	Return to Begin	J/BEGIN If $\overline{ID}$: J/STEP 4 If ID: J/STEP 5		BG 4 BG 5

INDEX (IX)

LOGIC CARD: LOGIC INSTRUCTION FETCH (LIF,LIX)
LOCATION: 1L
FUNCTION CODE BUFFER (1001)

IX 1 of 2

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
BG 5 Step 2	Ø	Read B's Index Register	IB-OUT READ L/D If $\overline{(Q=Ø)}$.M>9: P/CHECK If (Q=4): C/SUBTRACT	Q=Ø: -- Q=4: iØ to D Q=3: i1 to D Q=2: i2 to D Q=1: i3 to D	
	1	Index B Field	B-OUT R-TO-S L/H	Q=Ø: -- Q=4: BØ to H Q=3: B1 to H Q=2: B2 to H Q=1: B3 to H	
	2	Store New B Field	ADDER-TO-S L/B (3T) Q-DECR If $\overline{(Q=1)}$.$\overline{IBZ}$: J/STEP Ø	Q=Ø: -- Q=4: Load BØ Q=3: Load B1 Q=2: Load B2 Q=1: Load B3	Step Ø
Step 5	3	Read A's Index Register	IA-OUT READ L/D If IAZ: J/BEGIN J/STEP 6 If $\overline{(Q=Ø)}$.M>9: P/CHECK If (Q=4): C/SUBTRACT	Q=Ø: -- Q=4: iØ to D Q=3: i1 to D Q=2: i2 to D Q=1: i3 to D	BG 6
	4	Index A Field	A-OUT R-TO-S L/H	Q=Ø: -- Q=4: AØ to H Q=3: A1 to H Q=2: A2 to H Q=1: A3 to H	

INDEX (IX)

LOGIC CARD: LOGIC INSTRUCTION FETCH (LIF,LIX)
LOCATION: 1L
FUNCTION CODE BUFFER (1001) IX 2 of 2

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
	5	Store New A Field	ADDER-TO-S L/A Q-DECR J/STEP 3 If (Q=1): C/IA	Q=ØL -- Q=4: Load AØ Q=3: Load A1 Q=2: Load A2 Q=1: Load A3	Step 3

EDIT (ED)

LOGIC CARD: LOGIC DATA OPERATIONS (LDA,LDX)
LOCATION: .1N
FUNCTION CODE BUFFER (1100) ED 1 of 2

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS

BG 7
Step 4
Step 6
	Ø	Read Mask
		
		Test Mask
			B-OUT
			READ
			C/MINUS
			
			If (M,N=@):
			J/STEP 6
			
			If (M,N=@).3T:
			C/K
			C/E
			
			If $\overline{F3}$.(M,N=.-,/):
			SC-INH
			
			If $\overline{F3}$.(M,N=.-,/).3T:
			B-INCR
			
			If F3.(M,N=.-,/):
			J/STEP 6
			
			If (M,N = ZERO).3T:
			C/F3
				F3 = No Significance
				
				ZERO Code is a 6 bit code (Ø1ØØØØ)
					Step 6

	1	Store B in K & E	L/K L/E		
	2	Read A	A-OUT READ A-INCR If N2: P/MINUS If ($\overline{M=Ø}$).3T: C/ZERO C/F3	Preset MINUS is qualified by 3T	
	3	If Significance Write A into B	B-OUT Ø1-TO-N B-INCR If $\overline{F3}$: WRITE	$\overline{F3}$ = Significance	

EDIT (ED)

LOGIC CARD: LOGIC DATA OPERATIONS (LDA,LDX)
LOCATION: 1N
FUNCTION CODE BUFFER (1100) ED 2 of 2

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
	4	Test LA & LB	LB-DECR If (LB=Ø): LA-DECR If $\overline{(LA=Ø).(LB=1)}$: J/STEP Ø		Step Ø
	5	Write Blank if Last Digit of A is Positive	B-OUT L/N C/M J/BEGIN If $\overline{MINUS + ZERO}$: WRITE	L/N Clears N	BG Ø
Step Ø	6	Write K & E into B	B-OUT K-TO-S E-TO-S WRITE B-INCR J/STEP Ø		Step Ø

FORM NUMERIC FIELD (FN)

LOGIC CARD: LOGIC DATA OPERATIONS (LDA,LDX)
LOCATION: 1N
FUNCTION CODE BUFFER (1101) FN 1 of 1

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS

PO 3
Step 3
	Ø	READ A	A-OUT
			READ
			L/K
			A-DECR
			LA-DECR
			
			If F2.((M,N = P-Y)+
			(M,N = MINUS)):
			P/MINUS
			
			If (F2.(M,N = P-Y)+
			(M,N = Ø-9)).3T:
			P/CARRY
			
			If ($\overline{\text{F2.(M,N = P-Y)+}}$
			$\overline{\text{(M,N = Ø-9))}}$:
			J/STEP 3
				F2 = First Non-blank
				
				Preset MINUS is
				qualified by 3T
				
				For Non-digits
				go to Step 3
					Step 3

Step 4	1	Test LB	If (LB=Ø).$\overline{\text{F3}}$: J/BEGIN If MINUS.F3: 11-TO-N	F3 = First Digit	BG Ø
	2	Write B	B-OUT K-TO-S WRITE B-DECR LB-DECR C/F3 If ($\overline{\text{M=Ø}}$).3T: C/ZERO		

Step Ø	3	Test LA	If ($\overline{\text{M,N = SPACE}}$):
			C/F2
			
			If ($\overline{\text{LA=Ø}}$):
			J/STEP Ø
					Step Ø

	4	Write in Zeros	C/K C/CARRY Ø1-TO-N J/STEP 1	Write in zeroes if digits in A field less than B field	Step 1

POSITIONING (PO)

LOGIC CARD: LOGIC DATA OPERATIONS (LDA, LDX)
LOCATION: 1N
FUNCTION CODE BUFFER (1111) PO 1 of 1

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
BG 6	Ø	Postiion A to LSD + 1	A-INCR LA-DECR If ($\overline{LA=1}$): SC-INH		
	1	Position B to LSD + 1	B-INCR LB-DECR If ($\overline{LB=1}$): SC-INH		
	2	Restore LA from J Back A & B to LSD	J-TO-S L/LA A-DECR B-DECR		
	3	Restore LB from K Exits	K-TO-S L/LB F3,F2-TO-FC If $\overline{F3}$.FØ: P/SUB	F3,F2-TO-FC: If $\overline{F1.FØ}$: F1,FØ to FC $\overline{F3}$.FØ: DV or SUB	 AS Ø DV Ø MU Ø FN Ø
Via Test Panel	4	Service Steps	L/A Q-INCR If ($\overline{Q=4}$): SC-INH	Q=Ø: --- Q=1: Load A3 Q=2: Load A2 Q=3: Load A1 Q=4: Load AØ,AC,A5 (A5 in LDX only) Load A Register	
	5	Service Steps	A-OUT READ A-INCR SC-INH	Read core addressed by A Register	
	6	Service Steps	A-OUT WRITE A-INCR SC-INH	Write core addressed by A Register	

ADD/SUBRACT (AS)

LOGIC CARD: LOGIC ARITHMETIC (LAR)
LOCATION: 1P
FUNCTION CODE BUFFER (0100) AS 1 of 2

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
PO 3 Step 3	Ø	Read A	A-OUT READ L/D A-DECR LA-DECR If F2.N2.3T: T/SUB	F2 = First Digit Note: CARRY follows SUBTRACT	
Step 4 Step 6	1	Read B	B-OUT READ If F3: L/D If $\overline{F3}$: L/H If $\overline{F3}$.F2.N2.3T: T/SUB T/MINUS	F3 = Overdraft correction	
	2	Write B	B-OUT ADDER-TO-S WRITE B-DECR LB-DECR If F2: P/N1 If F3.F2.MINUS: 11-TO-N If F3.F2.$\overline{MINUS}$: Ø-TO-N If ($\overline{S=Ø}$).3T: C/ZERO	ADDER-TOTS: GIVES CARRY IN	

ADD/SUBTRACT (AS)

LOGIC CARD: LOGIC ARITHMETIC (LAR)
LOCATION: 1P
FUNCTION CODE BUFFER (0100) AS 2 of 2

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
	3	Test LB Test LA	C/F2 If (LB Ø): J/STEP 5 If $\overline{F3}$.($\overline{LB=Ø}$).($\overline{LA=Ø}$): J/STEP Ø	F3 = Overdraft Correction	 Step 5 Step Ø
	4	Finish B Field	C/D J/STEP 1		 Step 1
	5	Restore Test for Overdraft	K-TO-S L/LB If SUB.CARRY: P/F3 If ($\overline{SUB}$ + F3): J/BEGIN If F3.3T: C/SUB		 BG Ø

	6	Position B to LSD	P/F3
			P/F2
			P/CARRY
			C/H
			B-INCR
			K-TO-S
			K-DECR
			
			If ($\overline{S=1}$):
			SC-INH
			
			If (S=1).3T:
			T/MINUS
			
			If (S=1):
			J/STEP 1
					
					Step 1

MULTIPLY (MU)

LOGIC CARD: LOGIC ARITHMETIC (LAR)
LOCATION: 1P
FUNCTION CODE BUFFER (0110) MU 1 of 3

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
PO 3 Step 15	Ø	Read Multiplier	B-OUT READ P/N1 L/K L/E		
Step 2	1	Write Zero	B-OUT C/M Ø1-TO-N WRITE If $\overline{F2}$: J/STEP 14	F2 = First Digit	Step 14
	2	Extend B Field by LA	B-INCR LA-DECR If $\overline{(LA=1)}$: SC-DECR		Step 1
	3	Read Sign of Multiplicand	A-OUT READ If N2.3T: T/E2		
	4	Write Sign of Answer	B-OUT C/M E-TO-S WRITE J/STEP 12 If N2: P/MINUS	Preset MINUS is qualified by 3T	Step 12
Step 14	5	Position A & B to LSD	A-INCR B-INCR LA-DECR If $\overline{(LA=1)}$: SC-INH		

MULTIPLY (MU)

LOGIC CARD: LOGIC ARITHMETIC (LAR)
LOCATION: 1P
FUNCTION CODE BUFFER (0110)

MU 2 of 3

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
DV 3 DV 6	6	Restore LA	J-TO-S L/LA		
Step 9	7	Read A	A-OUT READ L/D		
	8	Read B	B-OUT READ L/H		
	9	Write Partial Product Test LA	B-OUT ADDER-TO-S WRITE B-DECR A-DECR LA-DECR If $(\overline{S=\emptyset}).\overline{F\emptyset}.3T$: C/ZERO If $(\overline{LA=1})$: J/STEP 7	$\overline{F\emptyset}$ = Multiply Adder-TO-S: Gives Carry In	Step 7
	1Ø	Carry into Spare	C/D B-OUT READ L/H		
	11	Answer into Spare	B-OUT ADDER-TO-S WRITE If $(\overline{S=\emptyset}).\overline{F\emptyset}.3T$: C/ZERO If FØ: J/DIVIDE J/STEP 4	FØ = Divide	DV 4

MULTIPLY (MU)

LOGIC CARD: LOGIC ARITHMETIC (LAR)
LOCATION: 1P
FUNCTION CODE BUFFER (0110) MU 3 of 3

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
Step 4 Step 13	12	Restore LA	J-TO-S L/LA If $\overline{F2}$; J/STEP 14	F2 = First Digit	 Step 14
	13	Position A & B to MSD	C/F2 A-DECR B-DECR LA-DECR If $(\overline{LA=1})$: SC INH If (LA=1): SC-DECR		 Step 12
Step 1 Step 12	14	Test Multiplier	K-TO-S K-DECR If $(\overline{S=\emptyset})$: J/STEP 5		 Step 5
	15	Test LB	B-DECR LB-DECR If $(\overline{LB=1})$: J/STEP $\emptyset$ If (LB=1): J/BEGIN		 Step $\emptyset$ BG $\emptyset$

DIVIDE (DV)

LOGIC CARD: LOGIC ARITHMETIC (LAR)
LOCATION: 1P
FUNCTION CODE BUFFER (0101)

DV 1 of 3

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
PO 3	Ø	Extend B Field by LA	B-INCR LA-DECR If $\overline{(LA=1)}$: SC-INH		
	1	Read Sign of Dividend	B-OUT READ P/N1 L/E B-INCR		
	2	Read Sign of Divisor	A-OUT READ If N2.3T: T/E2		
	3	Position B to Start Subtrac-tion	K-TO-S B-DECR K-DECR If $\overline{(S=1)}$: SC-INH If (S=1): J/MULT J/STEP 6		MU 6
MU 11	4	Restore LA Test for Correction	J-TO-S L/LA If $\overline{SUB}$: J/STEP 7		Step 7

DIVIDE (DV)

LOGIC CARD: LOGIC ARITHMETIC (LAR)
LOCATION: 1P
FUNCTION CODE BUFFER (0101) DV 2 of 3

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
	5	Test for Overdraft Test for Divide Error	K-TO-S If CARRY: K-INCR If $\overline{\text{CARRY}}$ T/SUB If CARRY.(S=9): J/BEGIN		BG Ø
Step 9	6	Position A & B to LSD	A-INCR B-INCR LA-DECR If $\overline{(\text{LA=1})}$: SC-INH If (LA=1): J/MULT J/STEP 6		MU 6
Step 4	7	Test LB	C/CARRY LB-DECR If (LB=1): J/STEP 1Ø		Step 1Ø
	8	Write Inter-mediate Quotient	T/SUB B-OUT K-TO-S Ø1-TO-N WRITE B-INCR If $\overline{(\text{S=Ø})}$.3T: C/ZERO		
	9		C/K J/STEP 6		Step 6

DIVIDE (DV)

LOGIC CARD: LOGIC ARITHMETIC (LAR)
LOCATION: 1P
FUNCTION CODE BUFFER (0101) DV 3 of 3

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
Step 7	1Ø	Write Last Quotient	B-OUT K-TO-S E-TO-S WRITE J/BEGIN If N2: P/MINUS If $(\overline{S=Ø}).3T$: C/ZERO	Preset MINUS is qualified by 3T —	BG Ø

COMPARE (CO)

LOGIC CARD: LOGIC DATA OPERATIONS (LDA,LDX)
LOCATION: 1N
FUNCTION CODE BUFFER (1110) CO 1 of 1

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
BG 7 Step 4	Ø	Read A into H & E	A-OUT READ L/H L/E A-INCR P/SUB		
	1	Read B into D	B-OUT READ L/D B-INCR If COMP-EQ: J/STEP 4		Step 4
	2	Carry In	ADDER-TO-S		
	3	Set Conditions	C/ZERO J/BEGIN If $\overline{\text{CARRY}}$: P/MINUS		BG Ø

Step 1	4	Test LA &
		LB
			LB-DECR
			J/STEP Ø
			
			If (LB=Ø):
			LA-DECR
			
			If (LA=Ø).(LB=1):
			J/BEGIN
					Step Ø
					BG Ø

SWITCH (SW)

LOGIC CARD: LOGIC READ/WRITE (LRW)
LOCATION: 1K
FUNCTION CODE BUFFER (0011) SW 1 of 2

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
BG 1 BG 2 BR 5 RW 9 RW 1Ø RW 11 RW 12 RW 16 Step 1	Ø	Transfer P to M,N	CONDS-TO-S R-TO-S If (Q=Ø): P-LIM-TO-S P-INCR	CONDS-TO-S: P-OUT Q=Ø: P-LIM Q=1: P3, Carry Q=2: P2, Minus Q=3: P1, ZERO Q=4: PØ, PC (PØ=1) = Partition Inactive	
	1	Store P in Core	WRITE Q-INCR If $\overline{\text{CHECK}}$: X-OUT If CHECK: 4Ø-OUT If $(\overline{Q=4})$: SC-DECR	X-OUT or 4Ø-OUT gives Q-OUT	Step Ø
START	2	Detect Power Failure	If PWR-FAIL: SC-INH	Upon detection of power failure, the ACU is held in this state. System reset starts here. (Clears Q,F2,X and FAC-CHECK)	
	3	A to P for FAC	If F2: A-OUT R-TO-S L/P Q-INCR SC-INH If (Q=4): LOAD-FAC J/INTERRUPT	F2 = FAC BUSY Q=Ø: -- Q=1: A3 to P3 Q=2: A2 to P2 Q=3: A1 to P1 Q=4: AØ to PØ AC to PC LOAD-FAC:Releases FAC DISC CONTROLLER: If ON CYLINDER•$\overline{\text{FAULT}}$: J/A=10 After FAC STROBE	IT Ø

SWITCH (SW)

LOGIC CARD: LOGIC READ/WRITE (LRW)
LOCATION: 1K
FUNCTION CODE BUFFER (0011) SW 2 of 2

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
Step 5	4	Increment Partition Number	C/TIMEOUT C/Disc Access-FF If $\overline{\text{INH-SW}}.\overline{\text{CHECK}}$: X-INCR	C/TIMEOUT: Clear F Clear IA,IB Load Z X-INCR: X-Incr H-Incr	
	5		If $\overline{\text{IO-SEL}}$: SC-DECR		Step 4
IT 8	6	Load P & Conditions	X-OUT READ L/P L/CONDS Q-INCR C/FAC-DONE If (Q=4): C/M If $\overline{(Q=4)}$: SC-INH	Q=Ø: -- Q=1: P3, Carry Q=2: P2, Minus Q=3: P1, Zero Q=4: PØ, PC (PØ=Ø) = Partition Active	
	7	Exit for normal Switching Check for FAC Done and Power Failure	J/BEGIN If F2: FAC-TO-S STATUS-IN LOAD-FAC If CHECK: P/LD-REQ	M1 = Error $\underline{M2}$ = Flag $\overline{M3}$ = Fault M4 = Repeat if Error F3 indicates PWR FAIL STATUS-IN: If M1 + $\overline{M3}$ + F2.F3: P/MINUS C/ZERO If (M1.M4 + F3. (LA=Ø).F2).3T: P1-DECR If $(\overline{M3}.\overline{F3})$: P/CARRY If M2: C/ZERO	BG Ø

BEGIN (BG)

LOGIC CARD: LOGIC INSTRUCTION FETCH (LIF)
LOCATION: 1L
FUNCTION CODE BUFFER (1010) BG 1 of 4

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
AS 5 BR 5 CO 3 CO 4 DV 5 DV 1Ø ED 5 FN 1 IT 2 MU 15 RW Ø RW 3 SW 7 TR 3 Step 5 Step 6 BG 5	Ø	Test for Interrupt	C/DH C/F If INTERRUPT: X-INCR J-INTERRUPT If FAC-CHECK.3T: P/CHECK	C/DH.2T: Clear D Clear H C/F: Clear F Clear IA,IB LOAD Z X-INCR: X-Incr H-Incr	IT Ø
	1	Test for Power Failure or IO Busy	C/FAC-CHECK If IO-BUSY + PWR-FAIL + INH-INSTR: J/SWITCH		SW Ø
	2	Test for Load Request	ØØØ1-TO-M If ACU-LD-REQ: C/P P/F3 J/Read, Write If CHECK.$\overline{\text{ACU-LD-REQ}}$: J/SWITCH	C/P: Clear P Clear A Clear J Clear LA Clear B3,B2,BØ Clear Conditions Load B1 L/K L/LB	RW Ø SW Ø

BEGIN (BG)

LOGIC CARD: LOGIC INSTRUCTION FETCH (LIF)
LOCATION: 1L
FUNCTION CODE BUFFER (1010)

BG 2 of 4

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
	3	Fetch Characters Ø-4 of Instruction	P-OUT READ L/F (3T) L/A L/B (3T) Q-INCR P-INCR If $\overline{(Q=4)}$: SC-INH If DATA-FAULT.3T: P/CHECK If (Q=4).$\overline{\text{DATA-FAULT}}$. (BR-OK): INST-STOP (3T) J/BRANCH	Data-Fault: ((M GR 9) + $\overline{\text{N1}}$) (Q=Ø).Load F: Load LA,J,LB,F3 Q=1: Load A3,B3,F2 Q=2: Load A2,B2,F1 Q=3: Load A1,B1,FØ Q=4: Load AØ,BØ AC,BC	BR Ø

	4
	
	(Cont)
		Fetch Characters 5-9 of Instruction	P-OUT
			READ
			L/I
			L/B (3T)
			Q-INCR
			P-INCR
			
			If $\overline{(Q=4)}$:
			SC-INH
			
			If DATA-FAULT.3T:
			P/CHECK
			
			If (Q=4).$\overline{\text{DATA-FAULT}}$.
			(BR-OK):
			J/BRANCH
			
			If (Q=4):
			INST-STOP (3T)
			
			(Continued)
				(Q=Ø).Load I:
				Load LB,K,IA1
				
				Q=1: Load B3,IAØ
				
				Q=2: Load B2,IB1
				
				Q=3: Load B1,IBØ
				
				Q=4: Load BØ,BC
					BR Ø

BEGIN (BG)

LOGIC CARD: LOGIC INSTRUCTION FETCH (LIF)
LOCATION: 1L
FUNCTION CODE BUFFER (1010) BG 3 of 4

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
	4 (Cont)	Set Mode	If $\overline{IAZ}$: D/SM-INHSW If F3.$\overline{F2}$.F1.$\overline{F\emptyset}$. (Q-4).$\overline{CHECK}$. PARTITION=Ø. E-SM: T/SM-INHSW If F3.$\overline{F2}$.F1.$\overline{F\emptyset}$. (Q=4).$\overline{CHECK}$. PARTITION-Ø E-SM.$\overline{IBZ}$: SYS-RES	F3.$\overline{F2}$.F1.$\overline{F\emptyset}$=Set Mode E-SM: Jumper on LIF. (Enables Set Mode) SYS-RES to I/O & Main Memory Only, Not to ACU.	

	5	Set Mode & Test for Indexing	If (F=BRANCH +
			F3.$\overline{F2}$.F1.$\overline{F\emptyset}$.
			E-SM):
			J/BEGIN
			
			If ($\overline{F=BRANCH}$).
			($\overline{F3+F2+F1+F\emptyset}$)
			($\overline{IAZ+IBZ}$):
			J/INDEX
					BG Ø
					
					IX Ø

BEGIN (BG)

LOGIC CARD: LOGIC INSTRUCTION FETCH (LIF)
LOCATION: 1L
FUNCTION CODE BUFFER (1010) BG 4 of 4

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
IX 3	6	Jumps for Arith. Op. or Invalid Opcodes or Exchange	C/CONDS C/DH If $\overline{(F2.\overline{F1}.F\emptyset+}$ $\overline{F3.F2)}$.CHECK: J/Positioning INST-STOP (3T) If ($\overline{F2}$.F1+CHECK): J/BEGIN P/CHECK If F3.F1.FØ: J/Transfer	C/CONDS: Clear MINUS Clear SUBTRACT Preset ZERO C/DH: Clear H Clear D NOTE: CARRY follows SUBTRACT Arith. Op: 4,5,6,7 or 13(FN) Invalid Op: 2,3,(1Ø) Exchange: 15	PO Ø BG Ø TR Ø
	7	Strobe F to Function Counter	F3,F2,F1-To-FC	RW: Ø,1 TR: 8,9 ED: 12 CO: 14	RW Ø TR Ø ED Ø CO Ø

INTERRUPT (IT)

LOGIC CARD: LOGIC READ/WRITE (LRW)
LOCATION: 1K
FUNCTION CODE BUFFER (0010) IT 1 of 4

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
BG Ø SW 3 Step 1 Step 3 Step 6 Step 13	Ø			Step for timing considerations	
	1	Service IOC Interrupts Poll Partitions	If INT-REQ: J/STEP 5 If $\overline{\text{INT-REQ}}.\overline{\text{D2}}$: X-INCR SC-DECR	X-INCR: X-Incr H-Incr D2 indicates D & H Count = 2Ø	 Step 5 Step Ø
	2	Trap for FAC not Busy	If $\overline{\text{F2}}$: J/BEGIN	F2 indicates FAC BUSY	 BG Ø
	3	Traps for Power Fail and FAC Done	C/DH If PWR-FAIL: P/F3 TERM-TRANS If $\overline{\text{PWR-FAIL.}}$ $\overline{\text{STATUS-RDY}}$: X-INCR J/INTERRUPT	C/DH.2T: Clear D Clear H F3 Indicates PWR-FAIL	 IT Ø
	4	Exit for Power Fail and FAC	P/FAC-DONE Q-INCR J/STEP 7		 IT 71

INTERRUPT (IT)

LOGIC CARD: LOGIC READ/WRITE (LRW)
LOCATION: 1K
FUNCTION CODE BUFFER (0010)

IT 2 of 4

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS

Step 1	5	Recall B (into A)	X-OUT
			1ØØ-OUT
			READ
			L/A
			Q-INCR
			
			If (Q=Ø).3T:
			L/J
			
			If ($\overline{Q=4}$):
			SC-INH
				Q=Ø: B4 to J
				Q=1: B3 to A3
				Q=2: B2 to A2
				Q=3: B1 to A1
				Q=4: BØ to AØ
				BC to AC	

	6	Test for Last Character	A-DECR If BORROW + J3-TERM-RD: P/LAST If J3-TERM-RD: J/INTERRUPT C/INT		IT Ø

Step 4
Step 8
	7	Transfer A to K,E	If $\overline{\text{FAC-DONE}}$:
			A-OUT
			
			If FAC-DONE:
			B-OUT
			
			R-TO-S
			L/K
			L/E
			
			If (Q=Ø):
			J-TO-S
			
			If ($\overline{Q=4}$):
			Ø1-TO-N
				Q=Ø: J to K,Ø1 to E
				Q=1: A3 to K,Ø1 to E
				Q=2: A2 to K,Ø1 to E
				Q=3: A1 to K,Ø1 to E
				Q=4: A4 to K,Ø1 to E	

INTERRUPT (IT)

LOGIC CARD: LOGIC READ/WRITE (LRW)
LOCATION: 1K
FUNCTION CODE BUFFER (0010) IT 3 of 4

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
	8	Store B	X-OUT 1ØØ-OUT K-TO-S E-TO-S WRITE Q-INCR If $\overline{(Q=4)}$: SC-DECR If (Q=4):FAC-DONE: J/SWITCH J/STEP 6		Step 7 SW 6
	9	Recall A (into A)	X-OUT 2ØØ-OUT READ L/A Q-INCR If $\overline{(Q=4)}$: SC-INH	Q=Ø: --- Q=1: Load A3 Q=2: Load A2 Q=3: Load A1 Q=4: Load AØ, AC	
	1Ø	Transfer Data Between Core and IOC	A-OUT A-INCR Q-INCR If J1 + OUT-REQ: READ If J1 + OUT-REQ: LOAD-IOS (3T) If $\overline{J1}.\overline{OUT\text{-}REQ}$: IOS TO-MN WRITE If ACU-LD-REQ: P/N1	J1: Send data to IOC $\overline{J1}$: Obtain data from IOC	

INTERRUPT (IT)

LOGIC CARD: LOGIC READ/WRITE (LRW)
LOCATION: 1K
FUNCTION CODE BUFFER (0010) IT 4 of 4

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
Step 12	11	Transfer A to K & E	A-OUT R-TO-S L/K L/E If ($\overline{Q=4}$): Ø1-TO-N	Q=1: A3 to K,Ø1 to E Q=2: A2 to K,Ø1 to E Q=3: A1 to K,Ø1 to E Q=4: AØ to K,AC to E	
	12	Store A	X-OUT 2ØØ-OUT K-TO-S E-TO-S WRITE Q INCR If ($\overline{Q=4}$): SC-DECR		Step 11
	13	Service Next Partition	C/INT J/INTERRUPT		IT Ø

READ/WRITE (RW)

LOGIC CARD: LOGIC READ/WRITE (LRW)
LOCATION: 1K
FUNCTION CODE BUFFER (0000) RW 1 of 4

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
BG 2 BG 7	Ø	Check FAC Protect Character	X-OUT 2ØØ-OUT READ If $\overline{K1}$.$\overline{FAC\text{-}INH}$: J/STEP 1Ø If $\overline{K1}$.FAC-INH: J/BEGIN	$\overline{K1}$ = FAC Instruction	Step 1Ø BG Ø
	1	Recall (B4) Check for Active Bits	X-OUT 1ØØ-OUT READ B-DECR If ($\overline{M4}$.$\overline{M2}$) + (F3.M4): J/STEP 4	F3 = Load in Progress M2.$\overline{M4}$ = Load Active M4 = I/O Active	Step 4

	2	IOC Sends Status to Condition FF's	IOS-TO-MN
			STATUS-IN
			LONG-CYCLE
				M1 = Error
				$\underline{M2}$ = Flag
				$\overline{M3}$ = Fault
				M4 = Repeat if Error
				
				STATUS-IN:
				
				If M1 + $\overline{M3}$ + F2.F3:
				P/MINUS
				C/ZERO
				
				If (M1.M4 + F3.(LA=Ø).F2.3T:
				P1-DECR
				
				If ($\overline{M3}$.$\overline{F3}$):
				P/CARRY
				
				If M2:
				C/ZERO	

	3	Erase I/O and Load Active Bits Status Exit	X-OUT 1ØØ-OUT C/M Ø1-TO-N WRITE J/BEGIN If F3.$\overline{MINUS}$: C/LD-REQ	(B4 = ØØØØ)= No Active Bits	BG Ø

READ/WRITE (RW)

LOGIC CARD: LOGIC READ/WRITE (LRW)
LOCATION: 1K
FUNCTION CODE BUFFER (0000) RW 2 of 4

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
Step 1	4	Send Device Number & Command to IOC	J-TO-S IOF-TO-S LOAD-IOS (3T) Q-INCR	J-TO-S Device # IOF-TO-S: If $\overline{F3 + LB2}$: 1 to N2 If FØ : 1 to N1	
Step 6	5	Transfer A to M,N	A-OUT R-TO-S		
	6	Store A	X-OUT 2ØØ-OUT WRITE Q-INCR If ($\overline{Q=4}$): Ø1-TO-N SC-DECR	Q=Ø: -- Q=1: A3 Q=2: A2 Q=3: A1 Q=4: AØ,AC	Step 5
Step 8	7	Transfer B to M,N	B-OUT R-TO-S If (Q=Ø): ACTVE-TO-S	ACTVE-TO-$\overline{S}$: If $\overline{F3}$: 1 to M4 If LB3: 1 to M3 If F3 + LB2: 1 to M2 If FØ: 1 to M1	
	8	Store B	X-OUT 1ØØ-OUT WRITE Q-INCR If ($\overline{Q=4}$): Ø1-TO-N SC-DECR	Q=Ø: B4(Active Bits) Q=1: B3 Q=2: B2 Q=3: B1 Q=4: BØ,BC	Step 7
	9	IOC Exit	J/SWITCH If F3 + $\overline{ACU-LD-REQ}$: P/IO-BUSY If $\overline{ADR-ERR}$.$\overline{CHECK}$.3T: P1-DECR		SW Ø

READ/WRITE (RW)

LOGIC CARD: LOGIC READ/WRITE (LRW)
LOCATION: 1K
FUNCTION CODE BUFFER (0000) RW 3 of 4

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
Step Ø	1Ø	Send Device Number & Command to FAC Check if Device is Ready	J-TO-S IOF-TO-S FAC-SELECT LOAD-FAC If $\overline{ACK}$: J/SWITCH If ACK.($\overline{LA=Ø}$): P/F2 B-DECR J/SWITCH If $\overline{ACK}$.$\overline{CHECK}$. $\overline{ADR-ERR}$.3T: P1-DECR	J-TO-S = Device # IOF-$\overline{TO-S}$: If $\overline{F3 + LB2}$: 1 to N2 If FØ : 1 to N1 (LA=Ø) = Disc F2 = FAC BUSY DISC CONTROLLER: J/A=Ø AFTER FAC STROBE	SW Ø
	11	Send Disc Unit # to FAC Check if Unit is Ready	B-OUT READ LOAD-FAC B-INCR If DATA-FAULT.3T: P/CHECK If $\overline{ACK}$: J/SWITCH If $\overline{ACK}$.$\overline{CHECK}$. $\overline{ADR-ERR}$.3T: P1-DECR	DISC CONTROLLER: J/A=1 AFTER FAC STROBE	SW Ø
	12	Send Partition # to FAC Check if Accepted	X-OUT X-TO-S LOAD-FAC If $\overline{ACK}$: J/SWITCH If $\overline{ACK}$.$\overline{CHECK}$. $\overline{ADR-ERR}$.3T: P1-DECR	DISC CONTROLLER: J/A=2 AFTER FAC STROBE	SW Ø

READ/WRITE (RW)

LOGIC CARD: LOGIC READ/WRITE (LRW)
LOCATION: 1K
FUNCTION CODE BUFFER (0000) RW 4 of 4

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
	13	Send Partition # to FAC Again	X-OUT X-TO-S LOAD-FAC	Disc Controller: J/A=3 After FAC Strobe	
	14	Send Disc Address TO FAC	B-OUT READ LOAD-FAC B-INCR Q-INCR If DATA-FAULT.3T: P/CHECK If $\overline{(Q=4)}$: SC-INH	Q=Ø:Cyl. Add. to FAC Q=1:Cyl. Add. to FAC Q=2:Cyl. Add. to FAC Q=3:Sec. Add. to FAC Q=4:Sec. Add. to FAC Disc Controller: J/A=4,5,6,7, and 8 After each FAC strobe	
	15	Set B Address to 1ØØ	ØØØ1-TO-M L/B2 FUNC-INCR	DISC CONTROLLER: J/A=9 AFTER FAC STROBE L/B2: Load B2 Clear B3,B1,BØ	
	16	Test for Disc on Cylinder Test for CHECK	B-DECR J/SWITCH LOAD-FAC If ACK.$\overline{\text{CHECK}}$: P/F2 P/Disc Access-FF If $\overline{\text{ACK}}.\overline{\text{CHECK}}.$ $\overline{\text{ADR-ERR.3T}}$: P1-DECR If $\overline{(\text{ACK.Disc Access-FF.3T})}$+ CHECK: TERM-TRANS	F2 = FAC BUSY TERM-TRANS: Clear Disc Disc Controller: J/A=9 After FAC Strobe	SW Ø

BRANCH (BR)

LOGIC CARD: LOGIC DATA OPERATIONS (LDA)
LOCATION: 1N
FUNCTION CODE BUFFER (1011) BR 1 of 2

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
BG 3 BG 4	Ø	Test for Branch Variant	If (LA=6): Q-INCR If $\overline{(LA=6)}.\overline{(LA=7)}$: J/STEP 4	(LA=6) = Branch and Transfer (LA=7) = Branch on Service-Request	Step 4
Step 3	1	Read Zone Bits of A	A-OUT READ		
	2	Transfer Poll Cntr or P to M,N	P-OUT R-TO-S If (Q=Ø): PCTR-TO-M	Q=Ø: Poll Cntr to M Q=1: P3 to M Q=2: P2 to M Q=3: P1 to M Q=4: PØ to M,PC to N	
	3		A-OUT WRITE Q-INCR A-INCR If (Q=Ø): C/SV-REQ If $\overline{(Q=Ø)}.\overline{(Q=4)}$: J/STEP 1		Step 1
Step Ø	4	Transfer B to P	B-OUT R-TO-S L/P Q-INCR If (Q=4): C/M If $\overline{(Q=4)}$: SC-INH	Q=Ø: -- Q=1: B3 to P3 Q=2: B2 to P2 Q=3: B1 to P1 Q=4: Zero to PØ, BC to PC	

BRANCH (BR)

LOGIC CARD: LOGIC DATA OPERATIONS (LDA)
LOCATION: 1N
FUNCTION CODE BUFFER (1011) BR 2 of 2

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
	5	Test for Switch	If (LB=8): J/SWITCH If TIME-OUT: J/SWITCH If $\overline{(LB=8)}.\overline{TIME\text{-}OUT}$: J/BEGIN	(LB=8) = Branch and Switch	 SW Ø BG Ø

TRANSFER (TR)

LOGIC CARD: LOGIC DATA OPERATIONS (LDA)
LOCATION: 1N
FUNCTION CODE BUFFER (1000) TR 1 of 1

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
BG 6 BG 7 Step 3	Ø	Read B	B-OUT READ L/K L/E	F-Bits: 1ØØØ = Transfer (T) 1ØØ1 = Numeric- Transfer (N) 1111 = Exchange (X)	
Step 3	1	Read A	A-OUT READ		
	2	Write A into B	B-OUT WRITE B-INCR If $\overline{F2}$.FØ: E-TO-S	$\overline{F2}$.FØ = Numeric Transfer	

	3	If
		Exchange
		Write B
		into A
			A-OUT
			K-TO-S
			E-TO-S
			A-INCR
			LB-DECR
			
			If F2:
			WRITE
			
			If FØ:
			J/STEP Ø
			
			If (LB=Ø):
			LA-DECR
			
			If $\overline{FØ}$.$\overline{(LA=Ø).(LB=1)}$:
			J/STEP 1
			
			If (LA=Ø).(LB=1):
			J/BEGIN
				F2 = Exchange	Step Ø
					Step 1
					
					BG Ø

INDEX (IX)

LOGIC CARD: LOGIC
LOCATION: 1L
FUNCTION CODE BUFFER (1001)

IX 1 of 2

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
BG 5 Step 2	Ø	Read B's Index Register	IB-OUT READ L/D If $\overline{(Q=Ø)}$.DATA-FAULT: P/CHECK If (Q=4): C/SUBTRACT	Q=Ø: -- Q=4: iØ to D Q=3: i1 to D Q=2: i2 to D Q=1: i3 to D	
	1	Index B Field	B-OUT R-TO-S L/H	Q=Ø: -- Q=4: BØ to H Q=3: B1 to H Q=2: B2 to H Q=1: B3 to H	
	2	Store New B Field	ADDER-TO-S L/B (3T) Q-DECR If $\overline{(Q=1)}$.$\overline{IBZ}$: J/STEP Ø	Q=Ø: -- Q=4: Load BØ Q=3: Load B1 Q=2: Load B2 Q=1: Load B3	Step Ø
Step 5	3	Read A's Index Register	IA-OUT READ L/D If IAZ: J/BEGIN J/STEP 6 If $\overline{(Q=Ø)}$.DATA-FAULT: P/CHECK If (Q=4): C/SUBTRACT	Q=Ø: -- Q=4: iØ to D Q=3: i1 to D Q=2: i2 to D Q=1: i3 to D	BG 6
	4	Index A Field	A-OUT R-TO-S L/H	Q=Ø: -- Q=4: AØ to H Q=3: A1 to H Q=2: A2 to H Q=1: A3 to H	

INDEX (IX)

LOGIC CARD: LOGIC INSTRUCTION FETCH (LIF)
LOCATION: 1L
FUNCTION CODE BUFFER (1001) IX 2 of 2

ENTRY	STEP	OPERATION	SIGNALS	REMARKS	EXITS
	5	Store New A Field	ADDER-TO-S L/A Q-DECR J/STEP 3 If (Q=1): C/IA	Q=Ø: -- Q=4: Load AØ Q=3: Load A1 Q=2: Load A2 Q=1: Load A3	Step 3

G. MAINTENANCE

The processor maintenance program is outlined in the following paragraphs. Preventive maintenance procedures include those operations that detect and correct minor discrepancies before they become equipment failures. When a failure does occur, the corrective maintenance procedures outline the steps to follow in restoring the equipment to operational status.

1. REFERENCES

Reference information is available in other sections of this service manual, in the System Ten Evaluation Program Manual (TP-271SL), and in the documentation package (logic diagrams, etc.) shipped with the processor. Diagnostic programs prove the ability of the processor to perform normal functions and aid in the detection and isolation of failures. Since these programs are updated as new information becomes available, refer to the Diagnostic Bulletins for the latest information.

2. TOOLS REQUIRED

The following tools are required in servicing the processor.

ITEM	PART NO.	ORDERING INFORMATION
Card Extender	T-19004	Shipped with processor; also available from Service Materials, San Leandro
Service Aid Card	T-19002	Available from Service Materials, San Leandro
Oscilloscope Tektronix 453	AT-18622	Available from Service Materials, San Leandro

ADDITIONAL TEST EQUIPMENT FOR DISTRICT. In addition to the above tools, each district service center should have a Digital Voltmeter, AT-19028 (also available from Service Materials, San Leandro).

3. SAFETY PRECAUTIONS

Personal safety cannot be overemphasized. To ensure your own safety observe the following precaution when servicing the processor.

WARNING

Dangerous voltages exist in the processor. Always turn off the ac power switch located at the center rear of the processor base plate before servicing ac harness, blowers, or line filters. When servicing the ac primary wiring, always remove the ac line cord from the power outlet.

In addition, there are practices that could result in damage to the equipment.

CAUTION

1. Never remove or insert circuit cards or interconnecting cables when the processor is energized.
2. Refer to section 15 before disconnecting the Line Switching Unit control cable.

4. PREVENTIVE MAINTENANCE

The prime objective of any maintenance activity is to provide maximum machine availability to the customer. Every preventive maintenance operation should assist in realizing this objective. Unless a preventive maintenance operation cuts machine downtime, it is unnecessary.

Preventive maintenance should be performed on the processor every 6 months or 1000 operating hours, whichever occurs first. The preventive maintenance operations are outlined in the following table.

Visual inspection is the first step in every scheduled maintenance operation. Always look for corrosion, dirt, wear, burns, binds, and loose connections. When a discrepancy is found it should be corrected at once.

ITEM	ACTION REQUIRED
Air filters	Clean filters with vacuum, or wash filters with soap and water and dry thoroughly.
DC Voltages	Measure the dc voltage outputs of both power supplies. Adjust only those voltages that are out of tolerance.
Circuit card	Review all service letters pertaining to the processor. Modify circuit cards as required to conform to the service letter information. If more than one modification is to be made, check the processor for normal operation after each modification.
Diagnostic tests	Run the diagnostic programs recommended in the System Ten Evaluation Program Manual (TPA-271SL).

5. CORRECTIVE MAINTENANCE

When an equipment failure occurs, perform the following steps to isolate the trouble. If the trouble is isolated to a circuit card, replace the circuit card with one that is known to be good. For any other than minor troubles that can be repaired at the branch, send the defective circuit card to the service center for repair.

a. Check power supply voltages from each power supply. Power Supply #1 provides the operating voltages for the ACU Module, FAC Module, and Expansion Module #1. All other modules are serviced by power supply #2. If all voltages are within tolerance specified in section 6, proceed to the next test.

b. If the processor is capable of loading and executing instructions, use the diagnostic programs to isolate the trouble. In some situations the diagnostic programs can isolate the trouble to a defective circuit card. Refer to the System Ten Diagnostic Program Manual, TPA-271SL.

c. Using the test panel, enter and execute one or more instructions. The test panel information is provided in section 7. When a defective indication for any state is observed, refer to the equipment documentation and to section 3 for information on the circuits involved.

d. The Service Aid Card may also be used for monitoring equipment operation. The following table provides the significance of each indication obtained from using the Service Aid Card.

DATA LAMP	CIRCUIT CARD				
	CH1	CH2	LU1	DRH	CL3
1	SELECT FF	TC8	TC8	RDCHK	RCLK
2	WRITE FF	TC4	TC4	DTAERR	SVRQ
3	READ FF	TC2	TC2	TRCHK	FAULT
4	STATUS FF	TC1	TC1	FLAG	BCD8
5	LDRQ FF	ST1	ST8	FAULT	BCD4
6	SVRQ FF	ST2	ST4	UNSAFE	BCD2
7	INT FF	ST4	ST2	SEEKING	BCD1
8	LAST FF	ST8	ST1	A=15	CHECK
9	IO BUSY FF	TURN ON	SEL FF	STATE Ø	OP1
10	TURN FF	GND	WRITE FF	$\overline{\text{STATE 1}}$	OP2
11	CHECK FF	GND	READ FF	STATE 2	LCLK
12	POLL FF	GND	STATUS FF	STATE 3	IO BUSY
13	GND	GND	REQUEST	RDWRTE	INT
14	GND	GND	OUTPUT ENA	RDS	START
15	GND	GND	FAULT & LOAD	STATUS	LDREQ
16	GND	GND	OPEN	DLTARST	FLAG