8-Channel Programmable Interface

Manual

Sigma Information Systems Anaheim, CA

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Section 1 - General Description

1.1 INTRODUCTION

This manual supplies the information needed to install and operate the SCD-DLV11J/8 8-channel serial line interface module manufactured by Sigma Information Systems, Anaheim, California. The material is arranged into the following sections:

SECTION 1 - GENERAL INFORMATION. This section contains a general description of the interface module, along with features. Specifications are included.

SECTION 2 - INSTALLATION. This section contains the switch selection and associated register formats for device and vector address assignments, baud rates and line parameters. Cabling and backplane installation is included.

SECTION 3 - PROGRAMMING CONSIDERATIONS. This section contains the address/vector formats and register formats for transmit and receive control/status and buffer registers.

APPENDIX A - The appendix lists the bus signals and their associated pin assignments.

1.2 GENERAL DESCRIPTION

The SCD-DLV11J/8 is a dual-wide asynchronous interface between the LSI-11 bus and up to eight standard serial I/O devices. It is software compatible with DEC* operating systems and diagnostics designed for the DLV11J. It plugs directly into any dual Q bus* slot.

Sigms's SCD-DLV11J/8 has switch selectable address (160000 to 177776) and vector (000 to 776) assignments. Once the initial address and vector are assigned, all eight channels are contiguous except the console channel which, if selected, resides at 177560 with vector at 60.

All channels share a programmable baud rate with a switch selectable default value. Baud rates range from 50 to 19.2K buad. The SCD-DLV11J/8 supports only RS-232C devices with all channels sharing switch selectable line parameters.

The interface module includes two 12-foot, 4-channel cables, each with four DB25P connectors. An optional rackmount panel provides convenient mounting for the eight DB25P connectors.

1.3 FEATURES

The following are some of the features of the SCD-DLV11J/8P.

- Eight asynchronous serial lines can be supported on one dual-wide module.
- The module is plug compatible with LSI-11 backplanes and plugs directly into any Q bus slot without backplane modification.
- The interface is software compatible with operating systems and diagnostics designed for the DLV11J.
- Baud rate is programmable with a switch selectable default value.
- Device address and vector assignments are switch selectable.
- Line parameters are switch selectable.

*DEC and Q bus are registered trademarks of Digital Equipment Corporation.

1.4 SPECIFICATIONS

Power Requirements:	+5VDC AT 2.0A 12VDC at 0.2A
Device Address:	Switch selectable 160000-177776 (Console = 177560)
Vector	Switch selectable 000-776 (console = 60)
Baud Rate:	Programmable per channel 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 3400, 3600, 4800 7200, 9600 and 19.2K
Line Parameters:	Switch selectable. Shared by all channels
Data Bit:	7 or 8
Parity:	Odd, even or none
Stop Bit:	1 or 2
Operation:	Full duplex
Interface Type:	RS-232C
Bus Load:	One DC load
Cables:	Includes two 12-ft, 4-channel cables, each with four DB25P connectors. Terminals require null modem cables with DB25S connectors to SCD-DLV11J/8P and associated terminal connectors.
Optional Panel:	Mounts the eight DB25P connectors for convenient rear rackmount cabling to RS-232C devices.
Installation:	Plugs directly into any standard Q bus slot that provides continuous BIAK1 and BIAKO lines.
Dimensions:	Single dual-wide module: 5.2"W x 8.9"H (13.2cmW x 22.8cmH)
Temperature	
Operating:	0°C to 50°C
Storage:	-40°C to 85°C
Humidity:	10% to 90% noncondensing

Section 2 - Installation

2.1 UNPACKING AND INSPECTION

The SCD-DLV11J/8P is shipped in a special packing carton designed to keep the module from vibrating and to give it maximum protection during shipment. The packing carton should be retained in case the unit requires reshipment.

Unpack the SCD-DLV11J/8P and visually inspect it for any damage that may have occurred during shipment. If any damage has occurred notify Sigma Information Systems immediately.

Verify that the factory set switches are set correctly according to Figure 2-1.

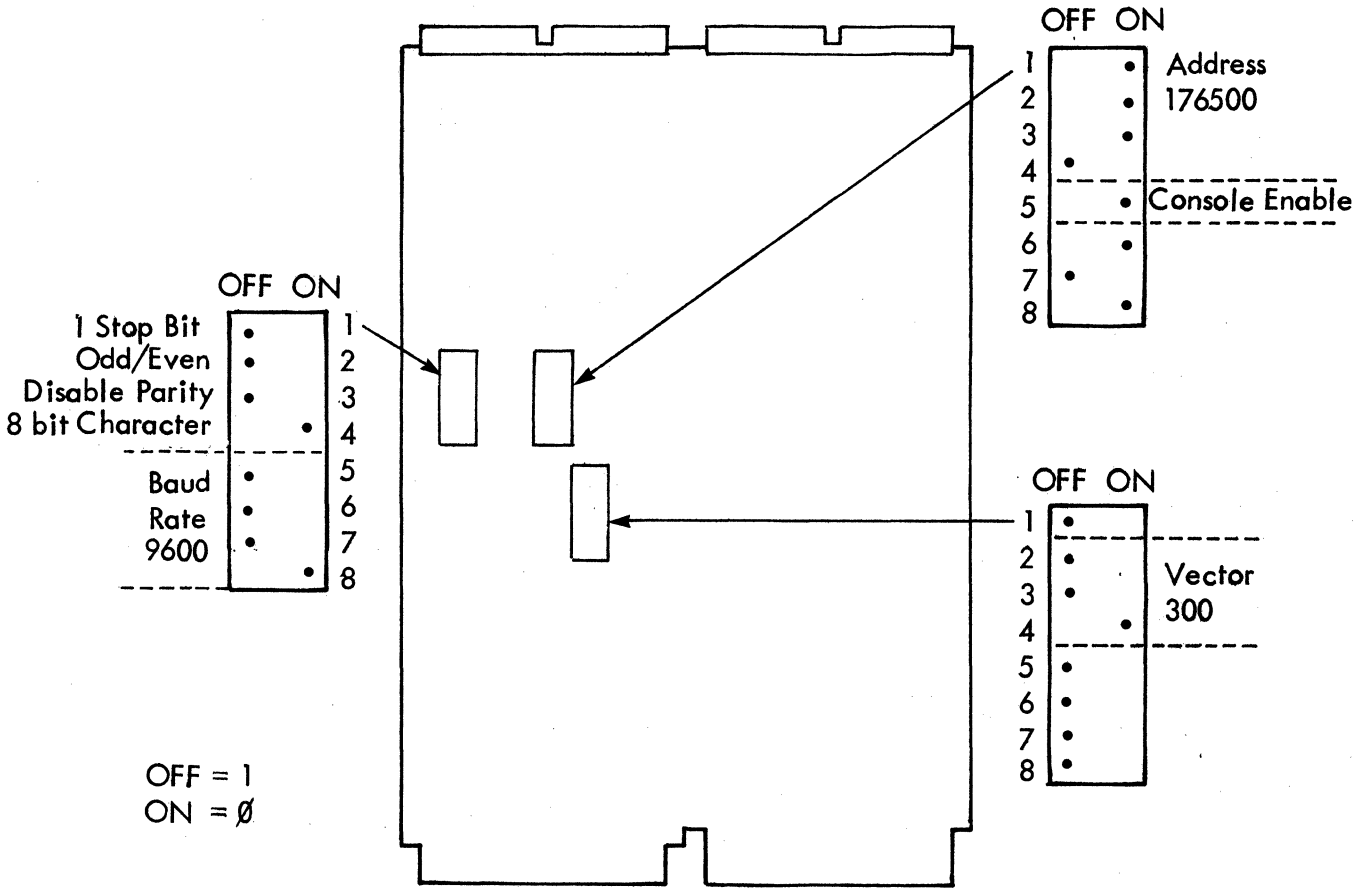
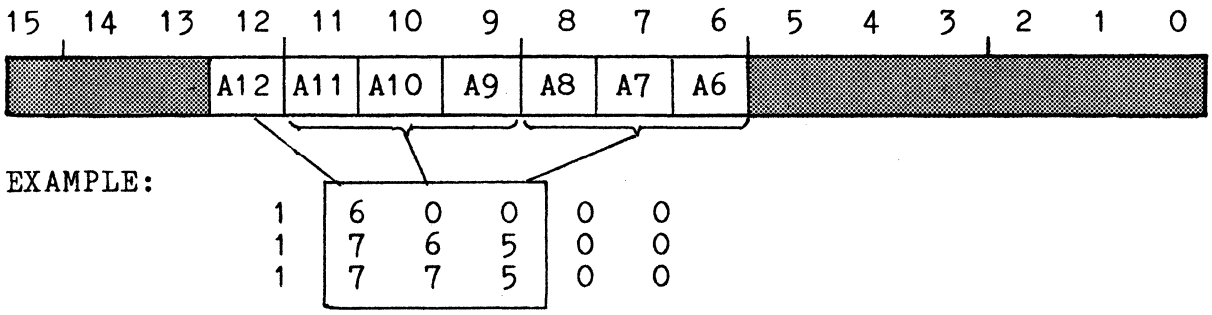


FIGURE 2-1: COMPONENT LOCATIONS SHOWING FACTORY CONFIGURATIONS

2.2 ADDRESS SELECTION

The SCD-DLV11J/8P has switch selectable device addressing in the range of 160000 to 177776 (octal). Once an initial address is assigned, the remaining seven channels are contiguous except the console which, if selected, resides at 177560 as channel 7. Refer to Section 3.1 for a description of the device address and vector interrupt assignments. The initial address format is shown below.



Significant address bits set by SW3

The initial address is determined with significant address bits A6-A12 set by switch SW3. Some examples follow in Table 2-1.

ADDRESS SET BY SW3	ADDRESS BITS A12	A11	A10	A9	A8	A7	A6
	SW3-POSITIONS 1	2	3	4	8	7	6
1 764 00	1	1	1	0	1	0	0
*1 765 00	1	1	1	0	1	0	1
1 766 00	1	1	1	0	1	1	0

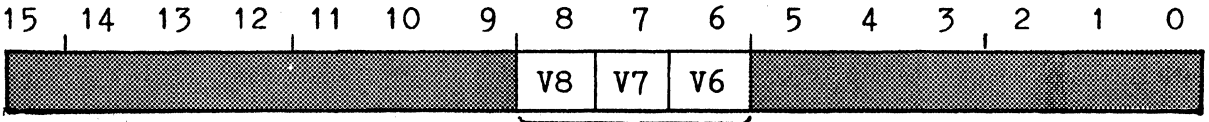
*Factory preset

0 = ON
1 = OFF

TABLE 2-1: EXAMPLE ADDRESS SELECTION

2.3 VECTOR SWITCH SELECTION

The SCD-DLV11J/8P has switch selectable vector assignments in the range of 000-776 (octal). Once the initial vector is assigned the remaining seven vectors are contiguous except the console which, if assigned, resides at 60 as channel 7. The initial vector format is shown below.



EXAMPLE:

Significant vector bits set by SW1

The initial vector is determined by significant vector bits V6-V8 set by switch SW1. Some examples follow in Table 2-2.

VECTOR SET BY SW1	VECTOR BITS V8	V7	V6
	SW1 POSITIONS 4	3	2
2 00	0	1	0
*3 00	0	1	1
6 00	1	1	0

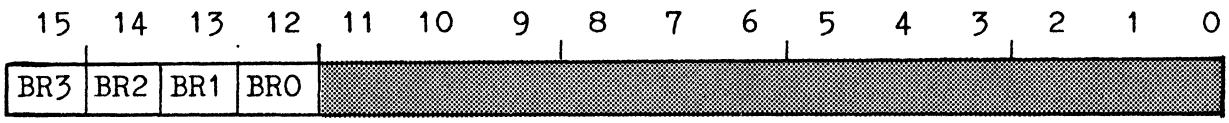
*Factory present

0 = ON
1 = OFF

TABLE 2-2: VECTOR SELECTION EXAMPLES

2.4 BAUD RATE SELECTION

All channels share the same programmable baud rate. The baud rate format is shown below.



where BR0-BR3 define programmable baud rates and SW2 defines default switch selectable baud rates as shown in Table 2-3.

BAUD RATE	XCSR BITS 15	14	13	12
	SW2 POSITIONS 5	6	7	8
50	0	0	0	0
75	0	0	0	1
110	0	0	1	0
134.5	0	0	1	1
150	0	1	0	0
200	0	1	0	1
300	0	1	1	0
600	0	1	1	1
1200	1	0	0	0
1800	1	0	0	1
2400	1	0	1	0
3600	1	0	1	1
4800	1	1	0	0
7200	1	1	0	1
9600*	1	1	1	0
19.2K	1	1	1	1

*Factory present

0 = ON
1 = OFF

TABLE 2-3: BAUD RATE SELECTION

2.5 LINE PARAMETERS SWITCH SELECTION

All eight channels share the same line parameters. The start bit is 1, but data bit, parity and stop bits can be assigned via switch SW2 as shown in Table 2-4.

LINE PARAMETER	SW2 POSITION	DEFINITION
CHARACTER LENGTH	4	0 = 7 BITS, *1 = 8 BITS
PARITY	3 2	*0 = DISABLE PARITY, 1 = ENABLE PARITY 0 = ODD PARITY, 1 = EVEN PARITY
STOP BITS	1	*0 = 1 STOP BIT, 1 = 2 STOP BITS

*Factory preset

0 = ON
1 = OFF

TABLE 2-4: LINE PARAMETERS SWITCH SELECTION

2.6 CONSOLE SELECTION

The console, if selected, is assigned channel 7. The SCD-DLV11J/8P is shipped with the console enabled. To disable the console set switch SW3-5 as shown in Table 2-5.

SW3-5	CONSOLE STATUS
0	DISABLE
*1	ENABLE

*Factory preset 0 = ON
1 = OFF

TABLE 2-5: CONSOLE ENABLE

2.7 BREAK RESPONSE

Channel 7 can be configured to either bootstrap, halt (console emulation mode), or have no response to a receive break condition. A bootstrap operation upon a receive break condition causes the CPU to execute the bootstrap program strating at the memory location defined by the power-up mode jumpers of the CPU. A halt operation unpon a receive break condition causes the processor to halt and the console octal debugging technique (ODT) microcode to be invoked. Configurations are shown in Table 2-6.

BREAK RESPONSE	E1-E2	E1-E3
None	OUT	OUT
Boot	IN	OUT
Halt	OUT	IN

TABLE 2-6: BREAK CONFIGURATIONS

2.8 CABLING

The SCD-DLV11J/8P has two 40-pin connectors and is supplied with two cables, each terminating in four DB25P connectors. The 40-pin connectors and associated 25-pin terminating connector pin assignments are defined in Table 2-6.

SIGNAL	DESCRIPTION	25-PIN DB25P	40-PIN CONNECTOR LINE NUMBER 0 4	1 5	2 6	3 7
Transmit Data	Data transmitted from SCD-DLV11J/8 to terminal	3	33	23	13	3
Receive Data	Data received by SCD-DLV11J/8P from terminal	2	38	28	18	8
Clear to Send	Signal sent by device to SCD-DLV11J/8 to indicate readiness for transmitted data	5	34	24	14	4
Ground	Signal Ground	1,7	39	25	12	5
Ground	Protective Ground	1,7	32	22	15	2

TABLE 2-7: CABLE PIN ASSIGNMENTS

The SCD-DLV11J/8P provides a Clear to Send input which can be driven by the attached serial line device to cause the SCD-DLV11J/8P channel to stop transmitting. The common use for this feature is with a printer that does not support XON-XOFF, but does provide a buffer full signal. This buffer status signal can be used to assert the CTS signal and effectively control transmission of data to the printer from the SCD-DLV11J/8P.

Cabling to terminals requires null modem cables with DB25S sockets between the SCD-DLV11J/8P connectors and associated terminal connectors.

2.9 MODULE INSTALLATION

The SCD-DLV11J/8P plugs directly into any Q bus slot, providing BIAK1 and BIAKO lines from the interface to the CPU are continuous. Bus signals and associated pin assignments are listed in Appendix A.

2.10 RACKMOUNT PANEL (OPTION)

An optional rackmount panel provides convenient mounting for the eight DB25P connectors. The panel is illustrated in Figure 2-2.

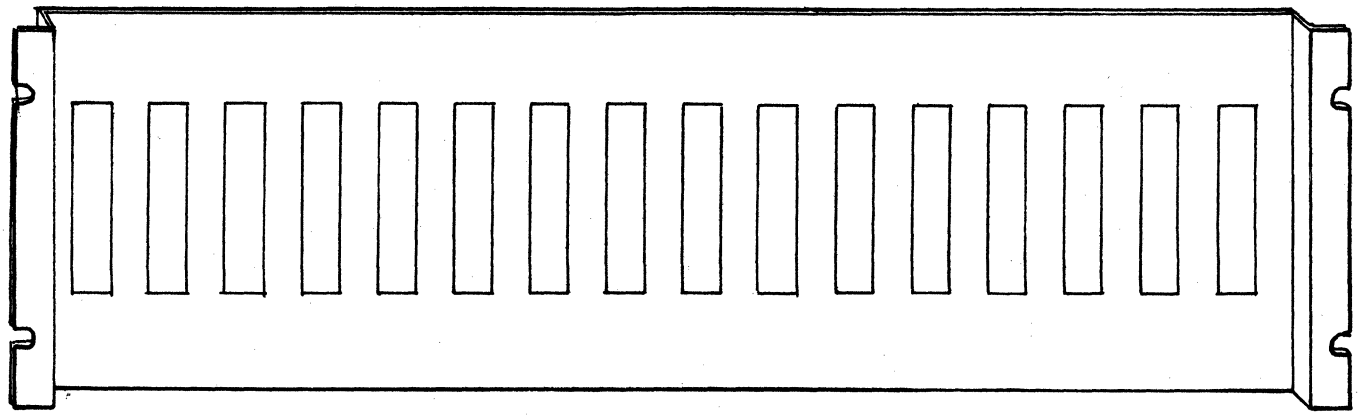


FIGURE 2-2: RACKMOUNT CONNECTOR PANEL

Section 3 - Programming Considerations

3.1 INTRODUCTION

The SCD-DLV11J/8P is controlled by four device registers per channel for a total of 32 device registers. The four device registers provided for each of the eight channels are:

RCSR	Receive Control/Status Registers
RBUF	Receive Buffer
XCSR	Transmit Control/Status Register
XBUF	Transmit Buffer

With the exception of the console channel, the device registers are assigned in a contiguous block by setting the address of channel 0. If the SCD-DLV11J/8P is used as the console device, channel 7 is assigned the console address and vector. If the SCD-DLV11J/8P is not used as the console, channel 7 is assigned as the last contiguous address set. Table 3-1 illustrates an initial address and vector assignment with contiguous locations.

ADDRESS	REGISTER	VECTOR	CHANNEL
176500	RCSR	300	0
176502	RBUF		
176504	XCSR	304	0
176506	XBUF		
176510	RCSR	310	1
176512	RBUF		
176514	XCSR	314	1
176516	XBUF		
176520	RCSR	320	2
176522	RBUF		
176524	XCSR	324	2
176526	XBUF		
176530	RCSR	330	3
176532	RBUF		
176534	XCSR	334	3
176536	XBUF		
176540	RCSR	340	4
176542	RBUF		
176544	XCSR	344	4
176546	XBUF		
176550	RCSR	350	5
176552	RBUF		
176554	XCSR	354	5
176556	XBUF		
176560	RCSR	360	6
176562	RBUF		
176564	XCSR	364	6
176566	XBUF		
176570*	RCSR	370	7
176572	RBUF		
176574	XCSR	374	7
176576	XBUF		

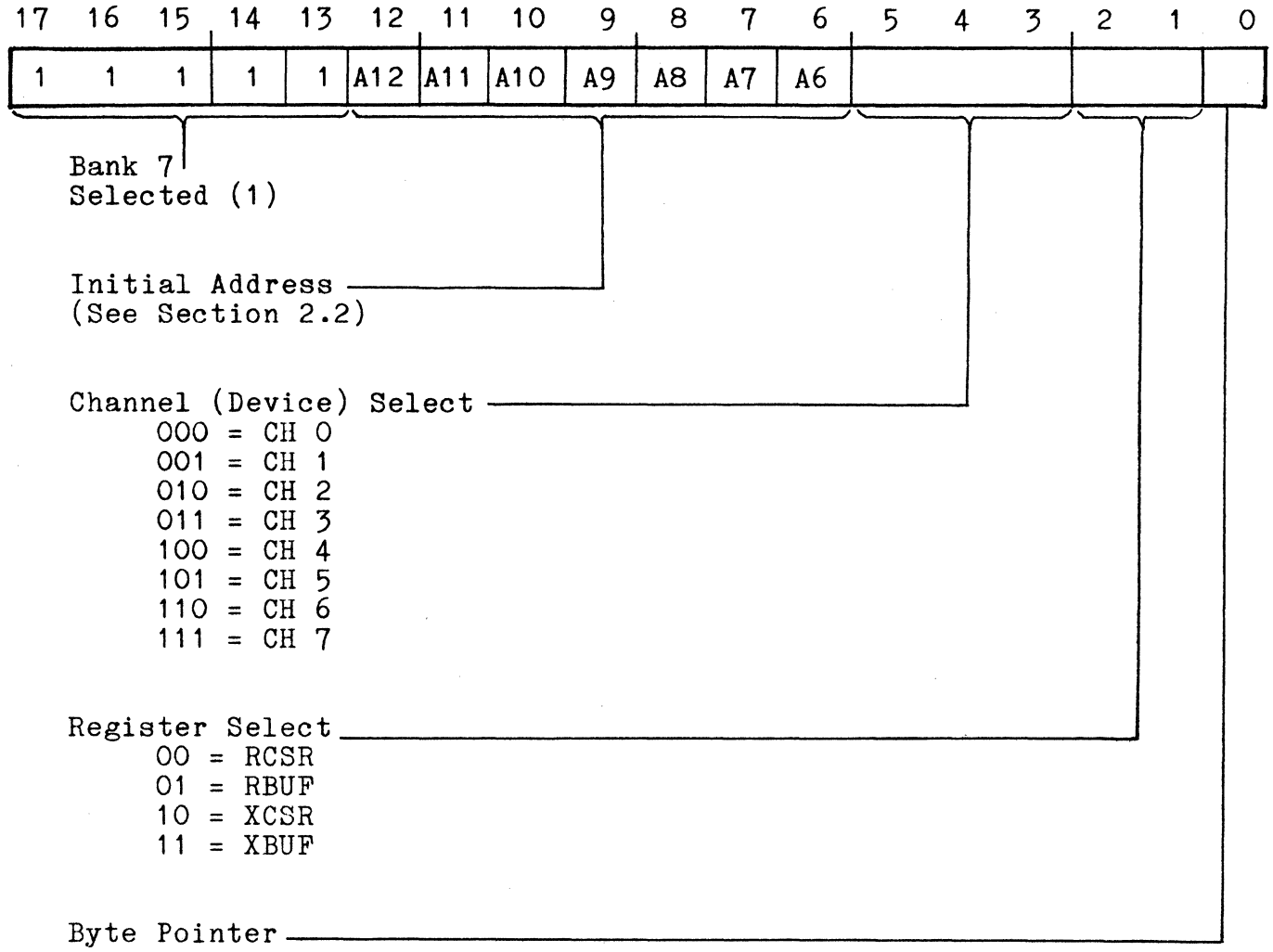
*If the console is selected it resides at channel 7 and the last four addresses in this table are:

177560	RCSR	60	7
177562	RBUF		
177564	XCSR	64	7
177566	XBUF		

TABLE 3-1: STANDARD ADDRESS AND VECTOR ASSIGNMENTS

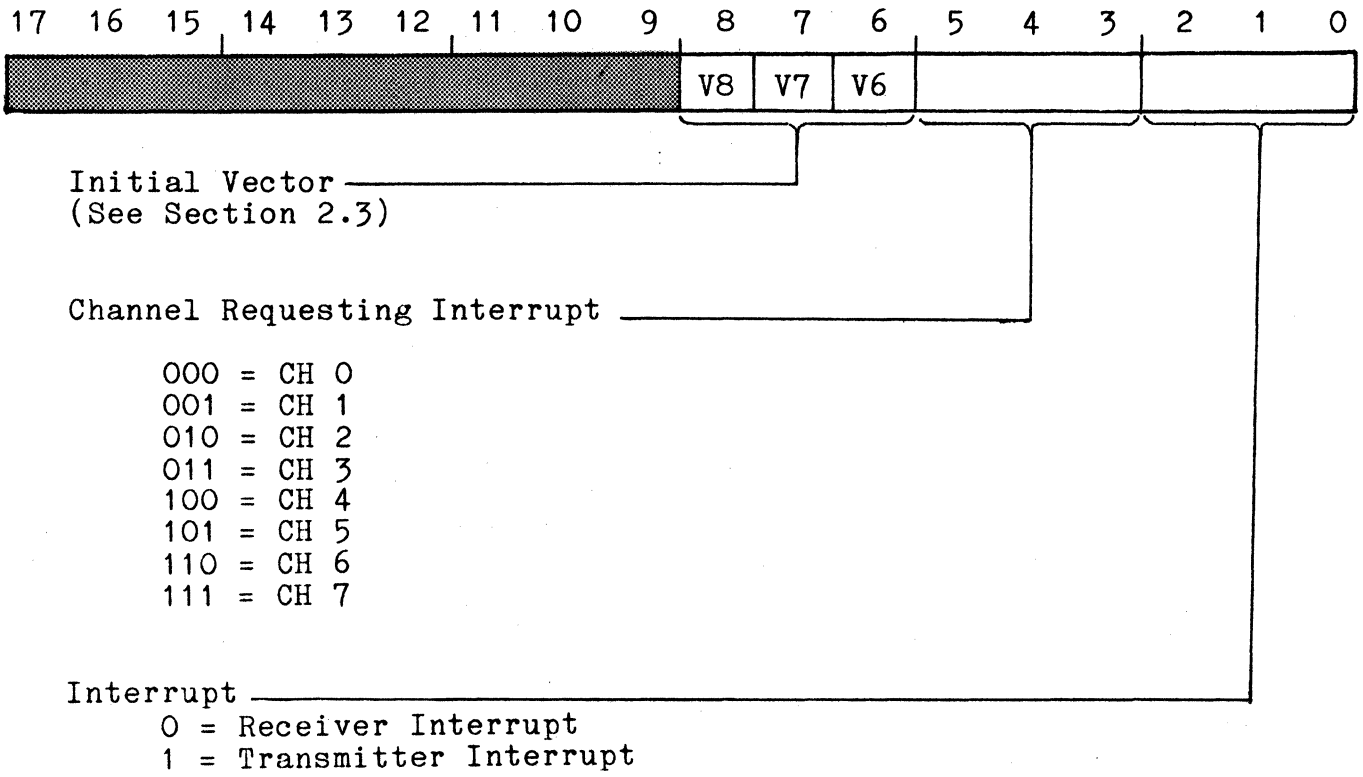
3.2 DEVICE ADDRESS FORMAT

The address configurations are listed in Table 3-2.



3.3 VECTOR INTERRUPT FORMAT

The interrupt vector format is shown below.

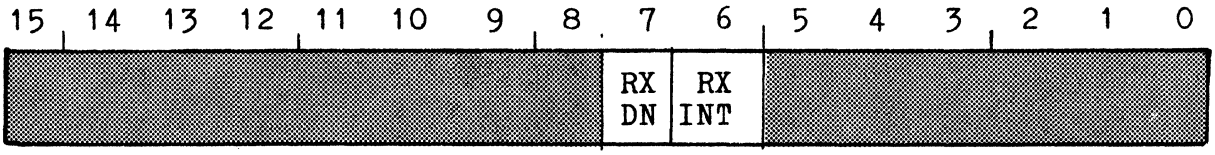


All bits not used are read as 0.

3.4 WORD FORMATS

The four word formats, one for each device register within a channel, are described in the following sections.

3.4.1 Receive Control/Status Register (RCSR)

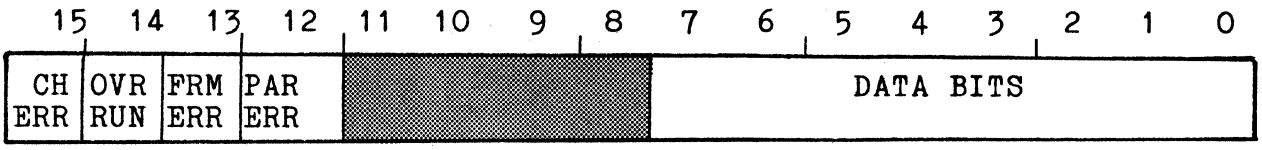


RX DN RECEIVER DONE. Set when an entire character has been received and is ready for input to the CPU. Cleared when RBUF is read or BINIT L signal goes true. If RX INT (bit 6) is set, setting RX DN starts an interrupt sequence. Read only.

RX INT RECEIVER INTERRUPT ENABLE. Set under program control to generate a receiver interrupt request (when a character is ready for input to the processor signified by bit 7 being set). Cleared under program control or by BINIT signal. Read/write.

All bits not used are read as 0.

3.4.2 Receiver Buffer (RBUF)



CH ERR — CHANNEL ERROR STATUS. Logical OR of bits 14, 13, and 12. Read only.

OVR RUN — OVERRUN ERROR. When set, indicates that the reading of the previously received character was not completed (receiver done not cleared) prior to receiving a new character. Cleared by BINIT signal. Read only.

NOTE: When "back-to-back" characters are received, one full character time is allowed from the time instant receiver done (bit 7) is set to the occurrence of an overrun error.

FRM ERR — FRAMING ERROR. When set, indicates that the character read had no valid stop bit. Cleared by BINIT signal. Read only.

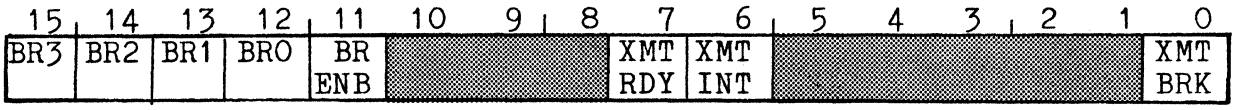
PAR ERR — PARITY ERROR. When set, indicates that the parity received does not agree with the expected parity. This bit is always 0 if no-parity operation is configured for the channel. Read only.

NOTE: Error bits remain valid until the next character is received, at which time the error bits are updated.

DATA BITS — DATA BITS. Contains seven or eight data bits in a right-justified format. Bit 7 = 0 when 7 data bits are enabled. Read only.

All bits not used are read as 0.

3.4.3 Transmit Control/Status Register (XCSR)



BR3-BRO — PROGRAMMABLE BAUD RATE SELECT. When set, these bits choose a baud rate from 50-19.2K baud. See section 2.4. Write only.

BR ENB — PROGRAMMABLE BAUD RATE ENABLE. Must be set in order to select a new baud rate indicated by bits 12-15. Write only.

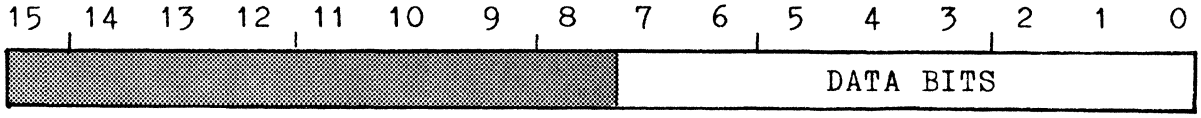
XMT RDY — TRANSMIT READY. Set when XBUF is empty and can accept another character for transmission. It is also set by INIT, during power-up or during a reset instruction. Read only.

XMT INT — TRANSMIT INTERRUPT ENABLE. Set under program control when it is desired to generate a transmitter interrupt request when transmitter is ready to accept a character for transmission. Cleared under program control, during power-up or reset instruction. Read/write.

XMT BRK — TRANSMIT BREAK. Set or reset under program control. When set, a continuous space level is transmitted. However, transmit done and transmit interrupt can still operate, allowing software timing of break. When not set, normal character transmission can occur. Cleared by BINIT. Read/write.

All bits not used are read as 0.

3.4.4 Transmit Buffer (XBUF)



Bits 0-7 contain the seven or eight right-justified data bits. Loaded under program control for serial transmission. Bits not used are read as 0.

CONNECTOR A		CONNECTOR B	
PIN	SIGNAL NAME	PIN	SIGNAL NAME
AA1	Not Used	BA1	BDCOK H
AB1	Not Used	BB1	Not Used
AC1	Not Used	BC1	Not Used
AD1	Not Used	BD1	Not Used
AE1	Not Used	BE1	Not Used
AF1	Not Used	BF1	Not Used
AH1	Not Used	BH1	Not Used
AJ1	GND	BJ1	GND
AK1	Not Used	BK1	Not Used
AL1	Not Used	BL1	Not Used
AM1	GND	BM1	GND
AN1	Not Used	BN1	Not Used
AP1	BHALH	BP1	Not Used
AR1	Not Used	BR1	Not Used
AS1	Not Used	BS1	Not Used
AT1	GND	BT1	GND
AU1	Not Used	BU1	Not Used
AV1	Not Used	BV1	+5VDC
AA2	+5VDC	BA2	+5VDC
AB2	Not Used	BB2	Not Used
AC2	GND	BC2	GND
AD2	+12VDC	BD2	Not Used
AE2	BDOUT L	BE2	BDAL2 L
AF2	BRPLY L	BF2	BDAL3 L
AH2	BDIN L	BH2	BDAL4 L
AJ2	BSYNC L	BJ2	BDAL5 L
AK2	Not Used	BK2	BDAL6 L
AL2	BIRQL	BL2	BDAL7 L
AM2	BIAKI L	BM2	BDAL8 L
AN2	BIAKO L	BN2	BDAL9 L
AP2	BBS7 L	BP2	BDAL10 L
AR2	BDMGI L	BR2	BDAL11 L
AS2	BDMGO L	BS2	BDAL12 L
AT2	BINIT L	BT2	BDAL13 L
AU2	BDALO L	BU2	BDAL14 L
AV2	BDALI L	BV2	BDAL15 L

BUS SIGNALS AND PINS ASSIGNMENTS