BUFFERED 300 LPM
LINE PRINTER
Technical Manual

SDS 900056A (OEM)

SCIENTIFIC DATA SYSTEMS

1649 Seventeenth Street, Santa Monica, California

1 October 1964

LINE/PRINTER **MODEL dp/p-3310**

INSTRUCTION MANUAL

NUMBER 201787-1

REVISION B

JULY 30, 1964

data products corporation

8535 WARNER DRIVE CULVER CITY, CALIFORNIA

LIST OF EFFECTIVE PAGES

Title Page	30 July 1964
ii	30 July 1964
iii and iv	Original
v to ix	30 July 1964
x	Original
xi to xvi	30 July 1964
1-0 to 1-8	Original
2-1 to 2-4	Original
3-1 to 3-22	Original
4-1 to 4-72	Original
4-73 to 4-75	30 July 1964
4-76 to 4-79	Original
4-80 and 4-81	30 July 1964
4-82 to 4-99	Original
4-100/101	30 July 1964
5-1	Original
5-2	30 July 1964
5-3 and 5-4	Original
5-5 and 5-6	30 July 1964
5-7 to 5-9	Original
5-10 and 5-11	30 July 1964
5-12 to 5-14	Original
5-15	30 July 1964
5-16 to 5-31	Original
5-32	30 July 1964
5-33 to 5-35	Original
5-36	30 July 1964
5-37 to 5-40	Original
5-41	30 July 1964
5-42	Original
5-43	30 July 1964
6-1 to 6-4	Original

Logic Diagrams	
1 and 2	Original
3	30 July 1964
4 to 20	Original
21	30 July 1964
22	Original
23	30 July 1964
24	Original
25 and 26	30 July 1964
27 to 29	Original
30 to 38	30 July 1964
39 to 41	Original
Card Schematic Drawings	
1A to 3D	Original
4C	30 July 1964
5A	Original
6A	30 July 1964
7D to 21P	Original
21V	30 July 1964
22C and 27B	Original
28B	30 July 1964
29A	Original
31B	30 July 1964
Card Assembly Drawings	
1A	30 July 1964
2A	Original
3D and 4C	30 July 1964
5A to 21P	Original
21V	30 July 1964
22C and 27B	Original
28B	30 July 1964
29A	Original
31B	30 July 1964

TABLE OF CONTENTS

SECTION V - MAINTENANCE

LIST OF ILLUSTRATIONS

SECTION V - MAINTENANCE

SECTION VI - DIAGRAMS

Figure I-O. Buffered LINE/PRINTER dp/p-3310, Front View

SECTION I

GENERAL DESCRIPTION

1-1. SCOPE

1-2. This manual describes installation, operation, theory of operation, and maintenance of the buffered LINE/PRINTER, Model No. dp/p-3310, designed and manufactured by Data Products Corporation, 8535 Warner Drive, Culver City, California.

1-3. PURPOSE AND BASIC PRINCIPLES

1-4. PURPOSE

1-5. The purpose of the printer is to accept binary coded information from a data source and produce printed copy at 300 lines per minute on all standard print media.

1-6. BASIC PRINCIPLES

1-7. Printing is accomplished by means of a rotating character drum and a bank of 132 linear-motion print hammers. The drum passes 64 different characters, in lines of 132 each, past the hammer bank. Upon command, the selected print hammers impact the paper against the ribbon and onto the appropriate character typeface as it passes the print position.

1-8. The data source supplies the printer with character data and command signals. The characters are supplied sequentially for storage in the printer buffer. The buffer will accept one complete line at a time (up to 132 characters). The printing of the stored data (one line) is as follows. The entire data output from the buffer is sequentially compared with the code of the character line passing

the hammer bank and re-stored in the buffer (the character line code is supplied by a code wheel on the character drum). Each time a match occurs, a signal is sent to the proper hammer driver receivers for storage. Prior to the appearance of the next line of characters at the hammer bank, the hammer driver receivers outputs are applied to associated hammer drivers. The hammer drivers pulse their respective hammers and cause the approaching drum character to be printed at the selected positions. This sequence is repeated for each line of characters on the drum until all the data in the buffer (one line) has been printed. The data source then reloads the buffer.

1-9. PHYSICAL DESCRIPTION

1-10. The buffered LINE/PRINTER, shown in Figures 1-0 and 5-2, consists of two major assemblies: the printer chassis and the electronics gate. The printer chassis contains the paper-feed assembly, the drum-gate assembly, the hammer-bank assembly, and the control-panel assembly. The electronics gate contains power supplies, power-sequencing relays, a maintenance test panel, and card-cage assemblies.

1-11. PRINTER CHASSIS

1-12. Paper-Feed Assembly. The paper-feed assembly is mounted on the printer-chassis base. This assembly contains the four tractors that physically support and move the paper between the drum gate and the hammer bank.

1-13. Drum-Gate Assembly. The drum-gate assembly is mounted at

the front of the printer chassis. This assembly contains the character drum used in the printing. The character-code code wheel and photo-diode assembly is mounted at the left end of the character drum. A ribbon-feed assembly, mounted on each side of the character drum, provides a moving ribbon between the character drum and the hammer bank.

1-14. Hammer-Bank Assembly. The hammer-bank assembly is mounted on top of the printer chassis and is directly opposite the character drum. The hammer-bank assembly contains the hammers which provide printing impacts.

1-15. Control-Panel Assembly. The control-panel assembly is mounted to a rigid frame on the left-hand side of the printer chassis. The face of the control panel, containing the operating switches and indicators, is flush-fitted against a cut-out portion of the printer-chassis cover.

1-16. ELECTRONICS GATE.

1-17. Power Supplies. Power supplies are located in the right half of the electronics gate. One unregulated supply provides -30V for the power-sequencing relays and +6V for the indicators. One of two regulated power supplies provides -30V for the hammer drivers; the other supply provides both -20V and +20V for the printer.

1-18. Power-Sequencing Relays. The power-sequencing relays provide the proper sequencing of power while energizing and de-energizing the printer. The power for the relays is provided, through interlocks on the voltage-regulator cards, by

the unregulated -30V power supply.

1-19. Maintenance Test Panel. The MAINTENANCE TEST PANEL is located on the top, right-hand side of the electronics gate. This panel provides maintenance checks of the printer.

1-20. Card-Cage Assemblies. Four card-cage assemblies are located in the electronics gate. These cages provide mechanical mounting and interconnecting wiring for the printed-circuit cards.

1-21. The printed-circuit cards contain all circuitry necessary for printer logic and DC voltage generation and regulation. Figure 5-5 lists all of the card types employed in the printer; pertinent information is included. For card locations, see Logic Drawing No. 41 in Section VI.

1-22. REFERENCE DATA

1-23. Pertinent reference data is listed in Figure 1-1.

Figure 1-1. Reference Data

GENERAL	
(a) Printing Rate	300 lines per minute
(b) Characters Per Line	132
(c) Characters Per Inch	10
(d) Lines Per Inch	6
(e) Line to Line Spacing	0.167 inches $\pm$0.015 inch
(f) Character Types	64
(g) Character Drum Speed	360 rpm
(h) Paper Line Advance Time	30 milliseconds maximum from initiation of motion command to paper stop.

Figure 1-1. Reference Data (cont'd.)

(i) Paper Feed	Tractor type, using a pair of tractors above and below the print position.
(j) Paper Feed Speed	20 in. per second, min.
(k) Paper Format	17-25/32 in. max. width, prints on 13.2 in. width in the center of a 17-25/32 in. form.
(l) Paper Dimensions	Standard (½ in. hole centers) edge punched fan fold paper from 3.5 to 17-25/32 in. in width and up to 22 in. in form length.
(m) Paper Types	Up to six parts, 12 lb. bond; tabulating card (0.007 in.) plus a second record sheet; single copy min. weight - 15 lb. bond.
(n) Paper Loading	Print drum pivots forward, paper is drawn upward through a large opening between the drum housing and the hammer bank.
(o) Horizontal Alignment	Manual control allows for positioning paper any place within 17-25/32 in. feed area. Vernier controls are provided for adjustment of up to ±one character while operating.
(p) Vertical Alignment	Continuous manual control of ±one line while operating.
(q) Character Typeface	Open face, Gothic style (special Data Products Corporation font). Each character is nominally 0.100 in. high and 0.060 in. wide (magnesium drum), or 0.095 in. high and 0.065 in. wide (beryllium drum).
(r) Character Spacing	Horizontal character spacing is 0.100 ±0.005 in. between centers. The max. accumulative error from nominal horizontal spacing is no more than ±0.010 in. per 132 character line.

Figure 1-1. Reference Data (cont'd.)

(s) Line Straightness	No character deviates more than ±0.010 in. from a straight line drawn parallel to the line of characters
(t) Core Storage	132 8-bit characters (one line)
INPUT-OUTPUT LINES	
Input Lines	
(a) data	6 data lines carry binary codes of characters to be printed and paper instructions
(b) Character Strobe pulse	A Character Strobe pulse initiates clock pulses which control the loading operation. An end of line pulse follows last character of a line of characters indicating that all information to be printed on that line has been sent. A paper-instruction active level initiates paper motion in the printer which will not stop until the paper-instruction level goes inactive
(c) Parity	An odd parity bit provides parity information for the accompanying character code
(d) Paper Instruction	A Paper-Instruction level indicates that the input received on the data lines is a Paper-Motion instruction for the paper tape loop or is a Paper-Count instruction
(e) Paper Count	A Paper-Count level indicates that the paper-instruction input (see d) received on the data lines is a Paper-Count instruction for the paper-motion counter
(f) Override	An Override level allows printer to continue loading and printing one line after standby condition has been initiated.

Figure 1-1. Reference Data (cont'd.)

(g) End of Line	An End-of-Line signal is provided to indicate that the last character for the line has been sent.
(h) Off Line	This signal illuminates the OFF LINE indicator.
(i) Input Error	This signal illuminates the INPUT ERROR indicator.
Output Lines	
(a) Send Data	A Send-Data level indicates to the data source that the printer is available to receive data. After each character is received, the Send Data level switches to the busy level for 8 usec and then returns to the send-data condition.until another character is received. After the End-of-Line signal is received, it switches to the busy level until line has been printed
(b) Parity Error	A Parity Error indicates that last line received by printer contains parity error
(c) Printer Ready	The Printer Ready level is provided to indicate that the printer is ready for printing
(d) Bottom of Form	A low signal is sent to the external equipment whenever channel 7 of the paper tape reader indicates that the bottom of the form is in printing position
POWER REQUIREMENTS	
AC	115 VAC $\pm$10%, 60 CPS $\pm$1CPS, Single Phase, 750W

Figure 1-1. Reference Data (cont'd.)

PHYSICAL CHARACTERISTICS	
(a) Dimensions	Width - 47.5 in.
	Depth - 24.5 in.
	Height - 47 in.
(b) Weight	675 lbs.
(c) Cabinet Color	Normally Data Products Corporation Blue and Gray.
ENVIRONMENTAL CONDITIONS	
(a) Operating Limits	50 to 100 degrees fahrenheit
	20 to 80 percent relative humidity
(b) Storage Limits	2 to 125 degrees fahrenheit
	20 to 95 percent relative humidity

SECTION II

INSTALLATION

2-1. INTRODUCTION

2-2. This section contains unpacking, installation, and input-output cabling information for the printer; preliminary operational checks are also included.

2-3. UNPACKING PROCEDURE

2-4. The printer is shipped on a reusable pallet and may remain on the pallet during a receiving check-out to facilitate any necessary reshipment. A shipping bolt (6, figures 5-8 and 5-9) must be removed before the drum gate can be opened. A portion of the pallet (a wooden block) must be removed before opening the electronics gate. The electronics gate must then be supported in the open position (the end of the previously removed wooden block can be used for this purpose).

2-5. The printer, after being unpacked, should be visually examined for damage. Report any damages at once to the shipping company. Do not disturb factory adjustments while positioning and installing.

2-6. INSTALLATION

2-7. The required installation space is illustrated in figure 2-1. Data and power cables are connected, under the left side-panel, to the electronics gate. Cooling air enters from the bottom of the electronics gate. The four supporting feet are individually adjustable and should be altered as necessary

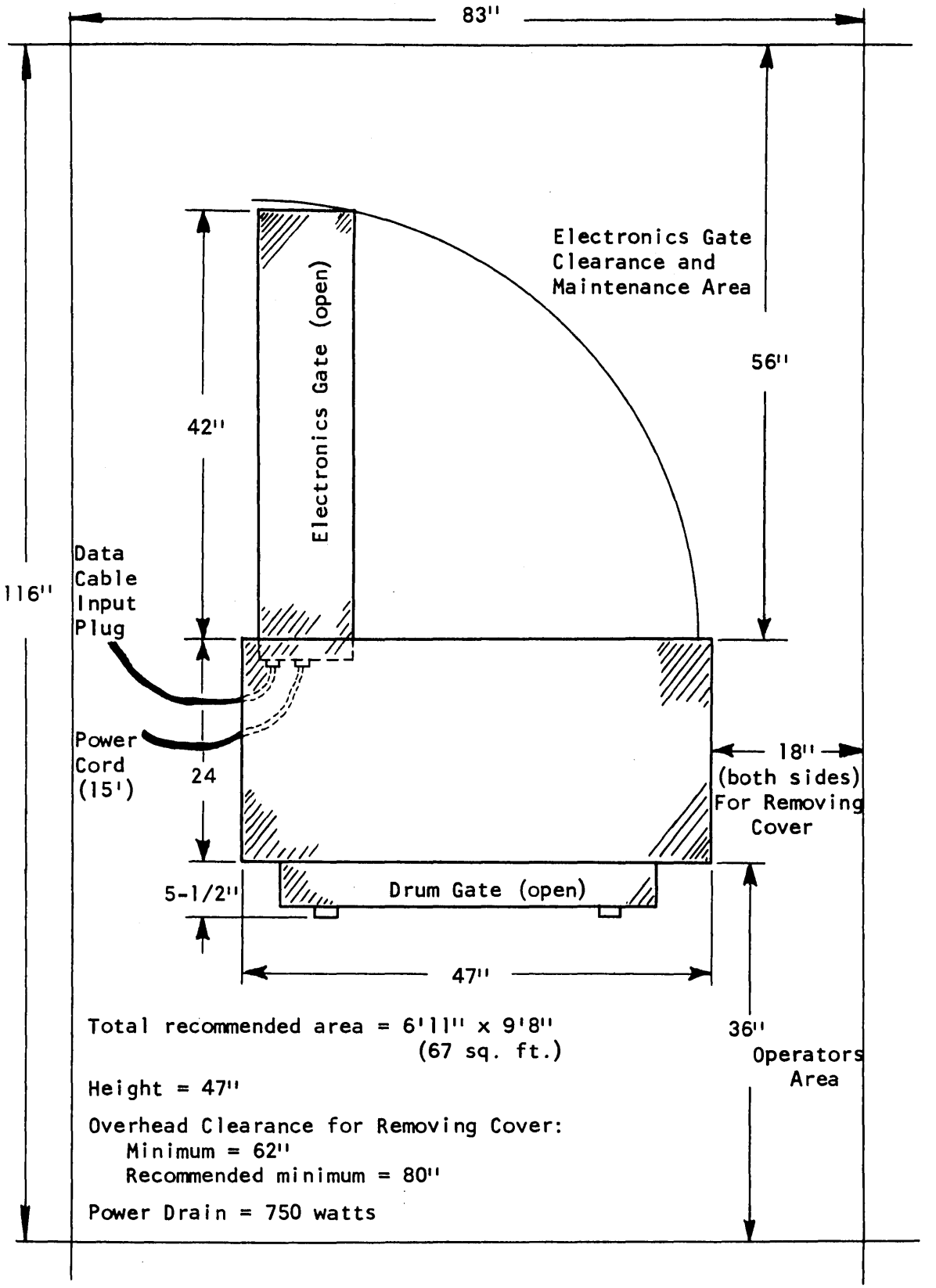


Figure 2-1. Printer Installation Diagram (top view)

to stabilize the printer.

2-8. INPUT-OUTPUT CABLING

2-9. Data And Control Signal Connections. The input-output signal connector information is shown on Logic Drawing No. 27 in Section VI.

2-10. Power Input Connections. A three-wire (AC, AC return, and ground) power input is required. The AC line must be connected in series with the circuit breaker.

2-11. PRELIMINARY CHECKS

2-12. The following steps should be performed in sequence when installing the printer:

(a) Perform a visual inspection of printer.

(b) Ensure that all printed-circuit cards are firmly in place.

(c) Connect power cable. (Note that the AC line is connected in series with circuit breaker.)

(d) Set HAMMER INHIBIT switch on MAINTENANCE TEST PANEL to HALT.

(e) Set remaining toggle switches on MAINTENANCE TEST PANEL to their center positions.

(f) Press POWER ON switch on control panel. POWER ON indicator should light.

(g) Measure all DC voltages by setting rotary switch on MAINTENANCE TEST PANEL to each position and observing indication on voltmeter. If any voltages are incorrect, voltage alignment procedures should

be performed (refer to Section V).

NOTE

THIS VOLTMETER DOES NOT PROVIDE AN ACCURATE INDICATION OF THE VOLTAGE. IT SHOULD BE USED AS A GENERAL INDICATOR ONLY.

(h) Reset HAMMER INHIBIT switch to RUN.

2-13. OPERATING CHECKS

2-14. The printer should be operationally checked by performing a standard printing operation using the data source (refer to Section III).

SECTION III

OPERATION

3-1. INTRODUCTION

3-2. This section contains operating procedures for the printer. The procedures include preliminary operating procedures (opening drum gate, installation and removal of ribbon, replacing and adjusting paper and paper-tape loops) and control panel operation. Programming information is also included.

3-3. PRELIMINARY OPERATING PROCEDURES

3-4. The preliminary operating procedures consist of removal and replacement of ribbon, replacement and adjustment of paper and paper-tape loops, and opening drum gate. The drum gate opening procedure is included since this a necessary step when replacing ribbon or paper.

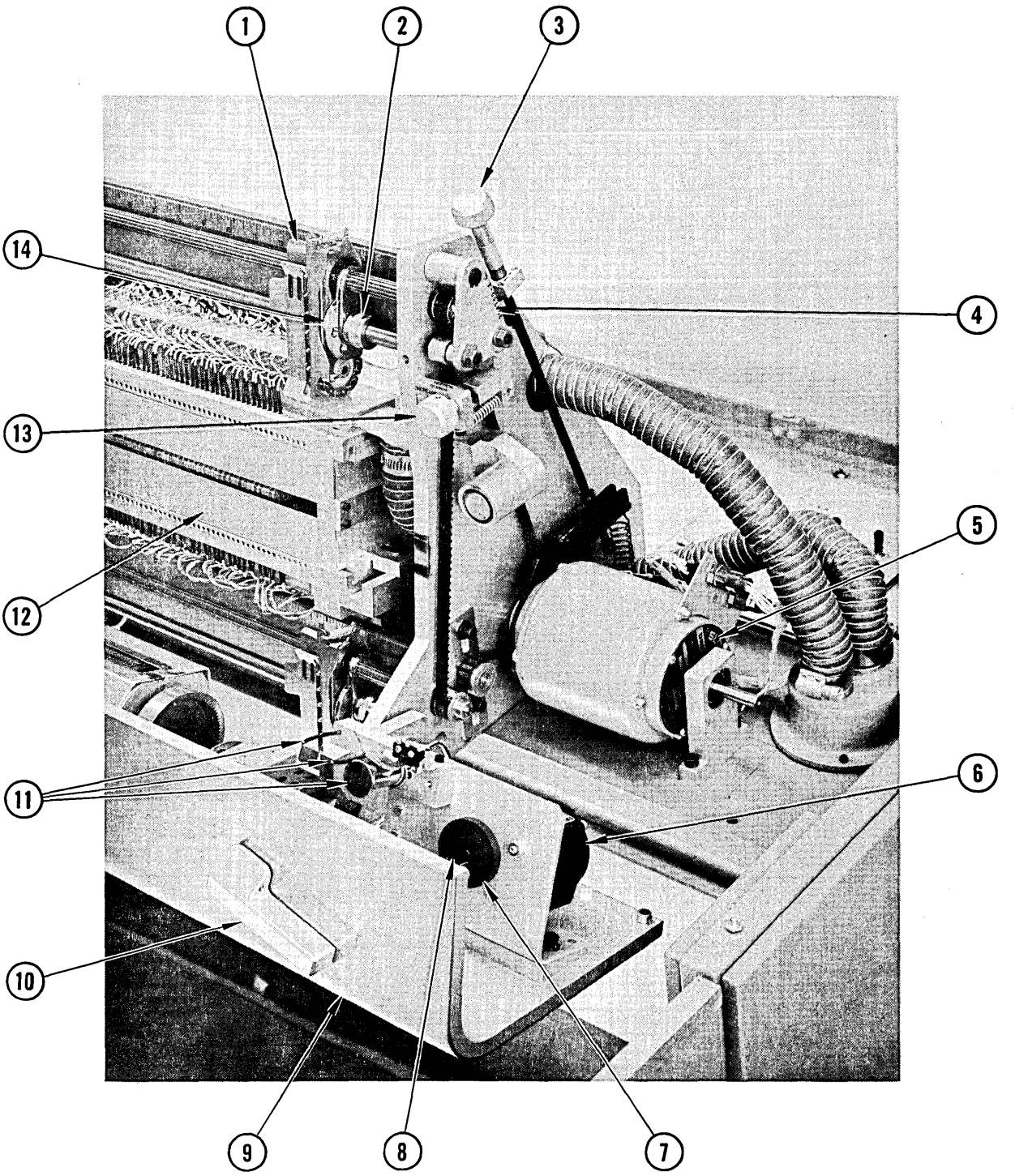
3-5. Opening Drum Gate. The drum gate is opened as follows:

(a) Turn both drum handles outward (10, figure 3-1; and 8, figure 3-2) and pull down to open drum gate to mid-position.

(b) Lift slide-latch (6, figure 3-2) to lower drum gate to lowest position.

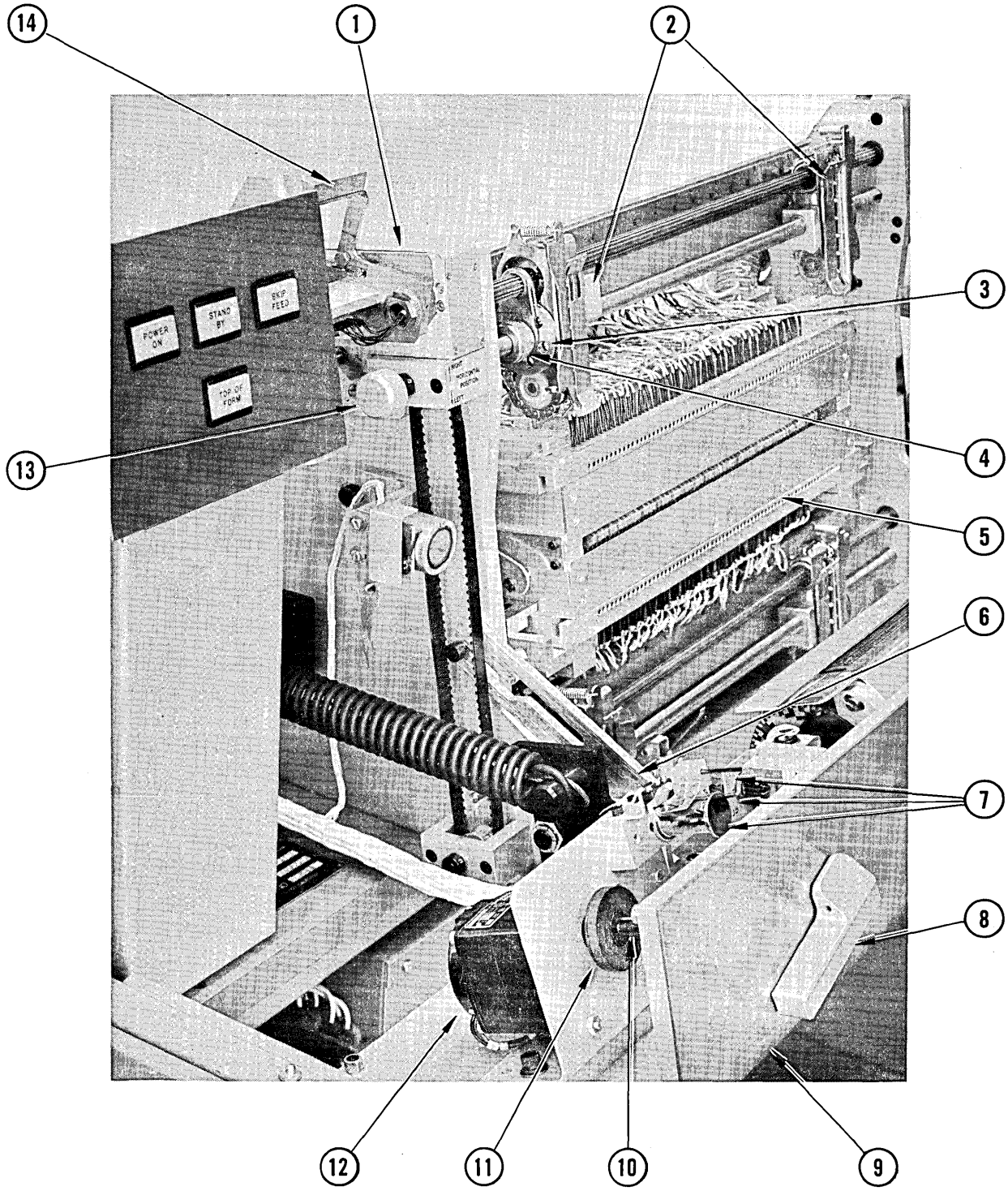
3-6. Ribbon Installation and Removal.

3-7. Ribbon Installation. The two ribbon spools are held in place by permanent magnets. (The ribbon may be loaded with the full spool on either side). Installation of the ribbon is as



1. Pressure Plates
2. Tractor Clamp
3. VERTICAL POSITION Control
4. Tension Plate
5. Stepping Motor
6. Right Ribbon Motor
7. Spool Holding Magnet
8. Ribbon-Motor Shaft
9. Drum Gate
10. Drum-Gate Handle
11. Right Ribbon Guides
12. Hammer Bank
13. VERTICAL TENSION Adjust
14. Horizontal Position Fine Adjustment

Figure 3-1. Printer Operating Controls (Right Side)



1. Paper-Tape Reader
2. Pressure Plates
3. Horizontal Position Fine Adjustment
4. Tractor Clamp
5. Hammer Bank
6. Slide
7. Left Ribbon Guides
8. Drum-Gate Handle
9. Drum Gate
10. Ribbon-Motor Shaft
11. Spool Holding Magnet
12. Left Ribbon Motor
13. HORIZONTAL POSITION Control
14. Paper-Tape-Reader Handle

Figure 3-2. Printer Operating Controls (Left Side)

follows:

(a) Press POWER ON control to off.

(b) Open drum gate to lowest position.

(c) Place full spool onto either ribbon-motor shaft (8, figure 3-1; and 10, figure 3-2) so that ribbon unwinds from bottom of spool as illustrated in figure 3-3.

(d) Thread ribbon as illustrated and connect to empty spool.

(e) Wind about two feet of ribbon onto empty spool by hand.

(f) Close drum gate.

3-8. Ribbon Removal. The ribbon is removed as follows:

(a) Press POWER ON control to off.

(b) Open drum gate to lowest position.

(c) Pull full ribbon-spool forward, clear of spool holding magnet (7, figure 3-1; and 11, figure 3-2).

(d) Unthread ribbon from drum gate and wind remaining ribbon onto full spool.

(e) Unhook end of ribbon from empty spool.

3-9. Paper Loading and Adjustment.

3-10. Paper Loading. Paper loading is accomplished as follows:

(a) Open drum gate to lowest position.

(b) Loosen tractor clamp (2, figure 3-1; and 4, figure 3-2); position two left tractors at "0" reading on scale; position two right tractors for width of paper.

Tighten tractor clamps, and open pressure plates (1, figure 3-1; and 2, figure 3-2).

(c) Place paper on shelf under drum gate.

(d) Insert end of paper up, between drum gate and hammer bank (9 and 12, figure 3-1).

(e) Position holes over cogs on top two tractors; close pressure plates.

(f) Position holes over cogs on bottom two tractors; close pressure gates.

(g) Adjust paper as necessary by following the instructions of paragraphs 3-11 and 3-12.

3-11. Paper Tension Adjustment. The horizontal-paper-tension adjustment is accomplished by adjusting the four fine adjustment controls on both sides of each shaft (3, figure 3-2) to remove horizontal slack in paper. The vertical-paper-tension adjustment is accomplished by rotating the VERTICAL TENSION control (13, figure 3-1) to remove all slack in the paper. Maximum vertical tension is required to obtain the best printing.

NOTE

THIS IS AN IMPORTANT ADJUSTMENT.
THE PAPER MUST BE TAUT. (BUT
NOT SO THAT THE HOLES TEAR.)

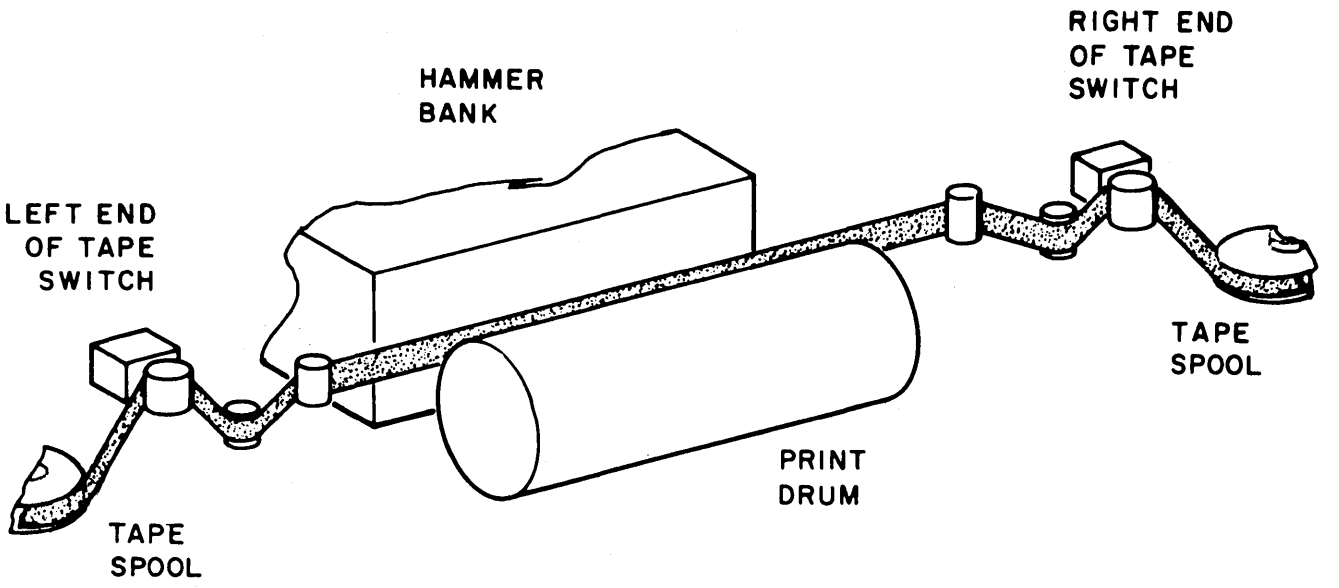


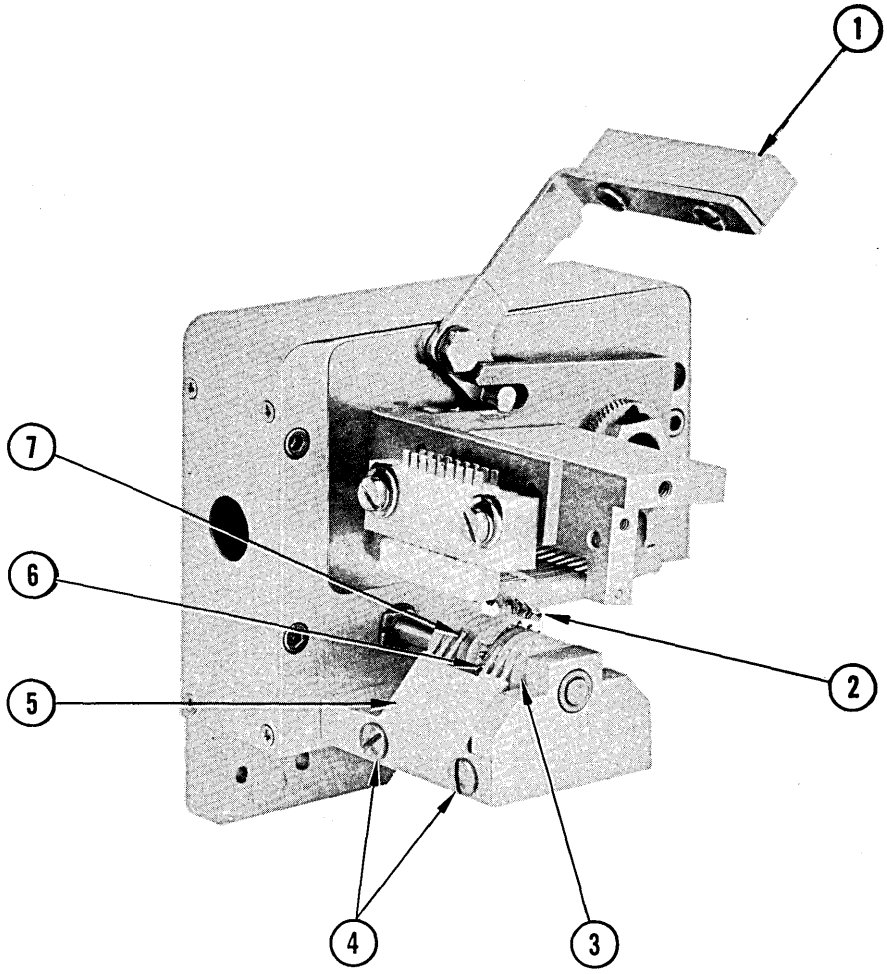
Figure 3-3. Ribbon Threading Diagram

3-12. Paper Position Adjustment. The paper can be adjusted after being inserted into the printer, to allow printing at a certain position on the paper (such as a form). Rotate the HORIZONTAL POSITION control (13, figure 3-2) and/or the VERTICAL POSITION control (3, figure 3-1) to position paper the desired amount.

NOTE

IT MAY BE NECESSARY TO ADJUST PAPER-TAPE READER AFTER PERFORMING VERTICAL POSITIONING OF THE PAPER. (REFER TO PARAGRAPH 3-14, e AND f.)

3-13. Paper-Tape Loop Installation. The paper-tape is positioned in the reader (see figure 3-4) with reference to the position of the paper. Insert the paper-tape loop as instructed in paragraph 3-14.



1. Handle
2. Sprockets
3. Nylon Roller
4. Shroud Bolts
5. Shroud
6. Guide Teeth
7. Set Screw

Figure 3-4. Paper-Tape Reader (Wires Removed)

3-14. (a) Position top-of-form position of the paper (paragraph 3-10) into printing position.

(b) Raise handle (1, figure 3-3) to clear sprockets from nylon roller.

(c) Insert paper-tape loop in reader so that hole in channel 1 is just past sprocket (figure 3-5, a); position guide holes in tape over guide teeth.

(d) Close handles, clamping paper-tape in reader.

(e) Press TOP OF FORM control; paper should move to the next top-of-form position.

(f) Press TOP OF FORM control again; if paper moves one line rather than to next top-of-form position, the nylon roller must be adjusted to position paper-tape properly (paragraph 3-15).

3-15. Paper-Tape-Reader Adjustment. The hole in channel 1 of the tape must stop just past the sprocket (figure 3-5, a) after TOP OF FORM has been selected. Incorrect stopping position results in hole stopping directly under sprocket (figure 3-5, b) and the next top-of-form selection will result in just one line of paper motion. Nylon roller (3, figure 3-3) is adjusted by loosening set screw (7, figure 3-3), rotating roller desired amount, and tightening set screw.

3-16. OPERATION

3-17. All necessary operating controls and indicators are located on the control panel of the printer. The nomenclature and function

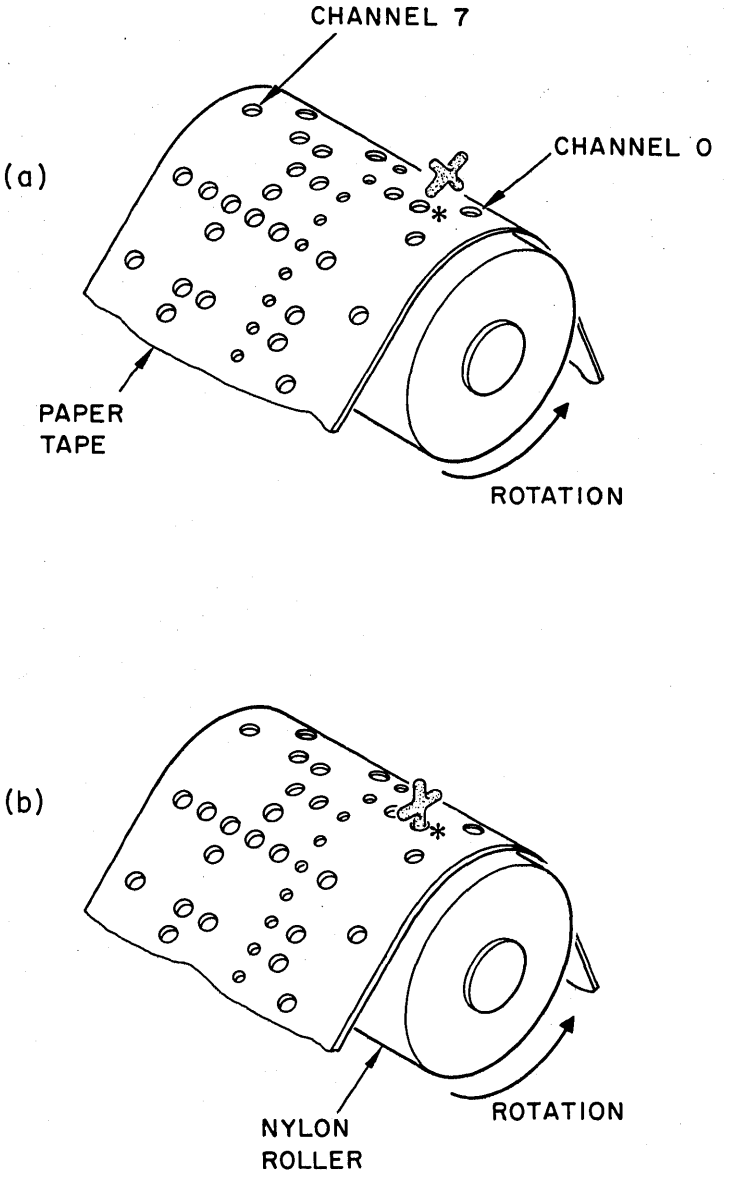


Figure 3-5. Tape Reader Adjustment

of each of these controls and indicators is tabulated in figure 3-6. The control panel is illustrated in figure 3-7.

Figure 3-6. Operating Panel Controls and Indicators Table

NOMENCLATURE	FUNCTION
POWER ON	The POWER ON control/indicator controls the main power to the printer. When pressed on, the switch supplies AC power to the fans, the drum motor, and the DC power supplies. The relay supply in turn supplies power to the sequencing relays. The indicator lights when pressed on and remains lighted until pressed off.
READY	The READY control/indicator lights when pressed on (indicating that the printer is ready for printing) and remains lighted until pressed off. The READY control/indicator, when pressed on enables the Send Data Signal, indicating to the external equipment that the printer is not in a standby condition and is ready to print. Each time the control is pressed on, a reset signal is sent to clear the printer parity condition.

Figure 3-6. Operating Panel Controls and Indicators Table (cont'd.)

NOMENCLATURE	FUNCTION
TOP OF FORM	The TOP OF FORM control/indicator is a momentary switch that provides a control of the paper drive. When pressed, paper will advance until a signal is generated by channel 1 of the paper tape loop. The TOP OF FORM indicator will light when paper reaches top of form (channel 1) position.
MANUAL OFF LN	The MANUAL OFF LN control/indicator provides a switching function for the external equipment. The indicator is lighted when the switch is closed.
TAPE/CARD	The TAPE/CARD control/indicator provides a switching function for the external equipment. The TAPE indicator is lighted when the switch is open; the CARD indicator is lighted when the switch is closed.
FORMAT/SPACE	The FORMAT/SPACE control/indicator provides a switching function for the external equipment. The FORMAT indicator is lighted when the switch is closed; the SPACE indicator is lighted when the switch

Figure 3-6. Operating Panel Controls and Indicators Table (cont'd.)

NOMENCLATURE	FUNCTION
FORMAT/SPACE	is open.
OFF LINE	The OFF LINE indicator provides an indicating function for the external equipment. The indicator lights when a high signal is received from the external equipment.
INPUT ERROR	The INPUT ERROR indicator provides an indicating function for the external equipment. The indicator lights when a high signal is received from the external equipment.
PRINT FAULT	The PRINT FAULT indicator lights whenever a parity error occurs.

3-18. Printer-Ready Condition. The printer is placed in the ready condition, ready to accept and print input data, by accomplishing the following two steps:

(a) Press fully and then release the POWER ON control/indicator (figure 3-7). Observe that the indicator is lighted.

(b) Press fully and then release the READY control/indicator (figure 3-7). Observe that the indicator is lighted. The printer is now ready to accept and print input data.

3-19. Printer-Standby Condition. The printer is placed in the standby condition from the ready condition by pressing fully and then releasing the READY control/indicator (figure 3-7).

3-20. Printer-Off Condition. The printer may be placed in the off-condition from either the ready or standby condition by pressing fully and then releasing the lighted POWER ON control/indicator.

NOTE

After placing printer in power-off condition, allow 10 seconds to elapse prior to again placing printer in ready-condition. Failure to observe this precaution may cause the -30 volt d-c power supply fuse (F4) to open.

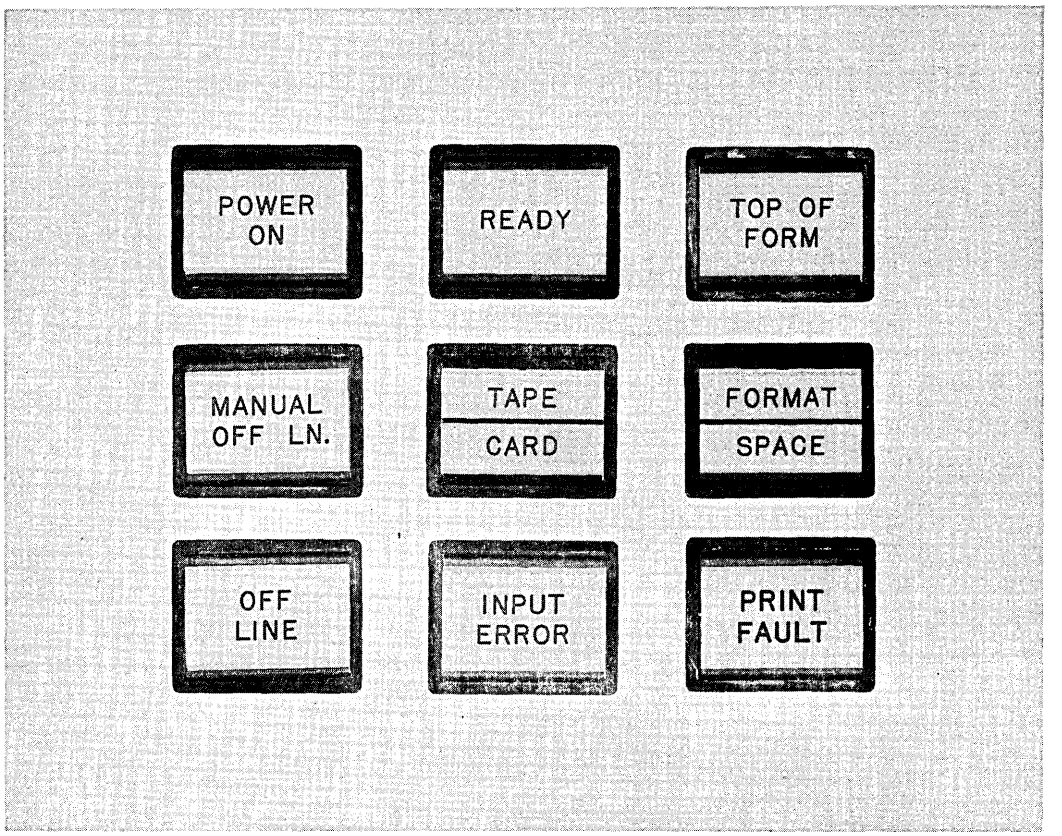


Figure 3-7. Printer Control Panel

3-21. PROGRAMMING INFORMATION

3-22. Interface Signals

3-23. A description of the computer-printer interface signals is as follows:

(a) Send Data. This signal from the printer is true to indicate that the printer is ready to receive new information or to feed paper. As each character is strobed into the printer this line will become false, and will stay false until the printer is ready for the next character (8 usec).

(b) Character Strobe. This pulse from the computer indicates to the printer that character or paper feed information is on the Input Data lines. This signal can be applied to the printer only when the Send Data signal is true, and must be of at least one usec duration.

(c) Input Data. These seven lines transmit character or paper feed information to the printer and must be active with, or before, the Character Strobe (refer to b, above). These lines must remain active for a minimum of two microseconds following the leading edge of the Character Strobe.

(d) Parity Bit. This bit is included with the input data. All character information is checked for odd parity (across all seven bits) prior to printing. Detection of a Parity Error initiates the following:

(1) Printing of the line is terminated.

(2) The address register is cleared.

(3) The Send Data signal becomes true to indicate that the printer is ready to re-load the character information for the line.

(4) The Parity Error signal to the computer becomes true.

(e) End Message. This signal is transmitted with the last character to be printed on a line. The signal must not become true within 2.0 usec following the last Character Strobe, and must be held true for at least 8 usec.

NOTE

THERE IS NO OVERFILL DETECTION IN THE PRINTER.

(f) Parity Error. This signal from the printer is true to indicate detection of a Parity Error. It is made false by the next Character Strobe or by operating the READY switch on the printer control panel.

(g) Paper Instruction. This signal to the printer must be true when the least significant three bits of the Input Data lines contain Tape-Mode or Count Mode paper feed information (refer to paragraph 3-24). This signal must be made active with, or before, an accompanying Character Strobe (for the Tape Mode), and must remain active for a minimum of two microseconds following the leading edge of the Character Strobe.

NOTE

NO INTERLOCKS ARE PROVIDED TO PREVENT THE PRINTER FROM MOVING PAPER WHILE THE UNIT IS PRINTING. THEREFORE, NO PAPER FEED SIGNALS SHOULD BE APPLIED WHEN THE SEND DATA LINE IS FALSE.

(h) Paper Count. A pulse on this line initiates a count mode paper feed if the Paper Instruction signal is true. This signal must be applied with, or before, the corresponding three lines count bits are placed on the Input Data lines and must have a duration of at least one usec. If this signal is false, the true Paper Instruction signal selects tape mode (refer to paragraph 3-24).

(i) Override. This signal is applied to the printer to override the READY switch. When the override signal is true, and the READY switch is placed in the STANDBY position, Send Data signals will continue to be generated and normal printer operation will continue.

CAUTION

THE DATA-SOURCE OVERRIDE SIGNAL, IN OVERRIDING THE PRINTER READY SWITCH, ALSO OVERRIDES THE FOLLOWING TWO SAFETY FEATURES OF THE PRINTER: 1) THE NO-PAPER SWITCH, AND 2) THE DRUM-GATE-OPEN SWITCH. THEREFORE, WHEN UTILIZING THE OVERRIDE SIGNAL, THE FOLLOWING PROGRAMMING PROVISION SHOULD BE MADE: AFTER PRINTING EACH

LINE AND PRIOR TO STARTING THE EXTERNAL DATA SOURCE, THE OVERRIDE SIGNAL SHOULD BE MADE FALSE. IF THE PRINTER SEND DATA SIGNAL BECOMES FALSE AT THIS TIME, DO NOT START THE EXTERNAL DATA SOURCE.

(j) Bottom of Form. This line to the computer is false when a hole is detected in channel 7 of the paper tape (indicating that the bottom of the form has not yet been reached).

(k) Blank and Space. When an octal 12 (SPACE) or 60 (BLANK) is applied on the INPUT DATA lines, no printing is done in the corresponding positions on the line. Parity is checked for these codes and a parity error results in the same actions as with a data parity error. Internal printer operation is identical for both of these codes.

3-24. Paper Feed Modes

3-25. Paper Feed Tape Mode. The paper is driven until a hole in the 8-channel paper tape loop is in the position indicated by the three least significant bits applied on the Input Data lines. (See figure 3-8). The tape reader is not interrogated when the instruction is applied; a minimum of one line is always spaced. The other three data bits are not checked or used; parity is not checked. This operation requires a true Paper Instruction signal and a CHARACTER STROBE.

Figure 3-8. PAPER INSTRUCTIONS

OCTAL	INPUT DATA lines			TAPE MODE	COUNT MODE
	2^2	2^1	2^0		
0	0	0	0	Tape Channel 0	Space 0 lines
1	0	0	1	Tape Channel 1	Space 1 lines
2	0	1	0	Tape Channel 2	Space 2 lines
3	0	1	1	Tape Channel 3	Space 3 lines
4	1	0	0	Tape Channel 4	Space 4 lines
5	1	0	1	Tape Channel 5	Space 5 lines
6	1	1	0	Tape Channel 6	Space 6 lines
7	1	1	1	Tape Channel 7	Space 7 lines

3-26. Paper Feed Count Mode. The tape is driven from zero to seven spaces as indicated by the three least significant bits applied on the Input Data lines. (See figure 3-8). A count of zero results in no spacing. The other three data bits are not checked or used; parity is not checked. This operation requires a true Paper Instruction signal, a Character Strobe, and a Count signal.

3-27. Overprinting.

3-28. Overprinting. Paper is not advanced automatically before or after a line is printed. Absence of a paper feed instruction between transmission of characters for two lines results in an overprint.

3-29. Timing.

3-30. Figure 3-9 shows the basic elements of printer timing.

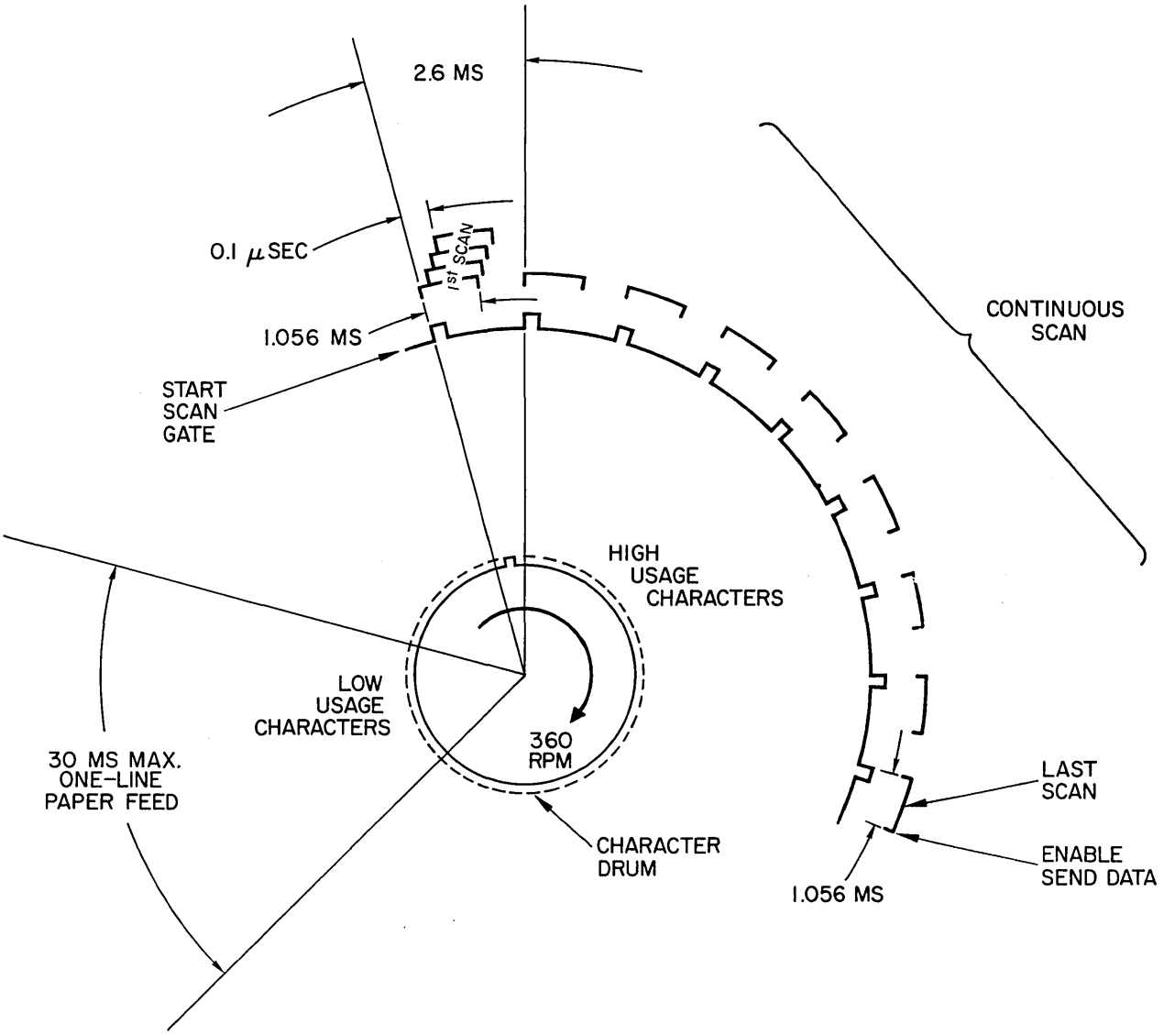


Figure 3-9. Print Timing

The description is as follows.

(a) Coincidence of a 384-cps 0.1-usec gate initiates the first character scan.

(b) This gate initates subsequent character scans, one for each character.

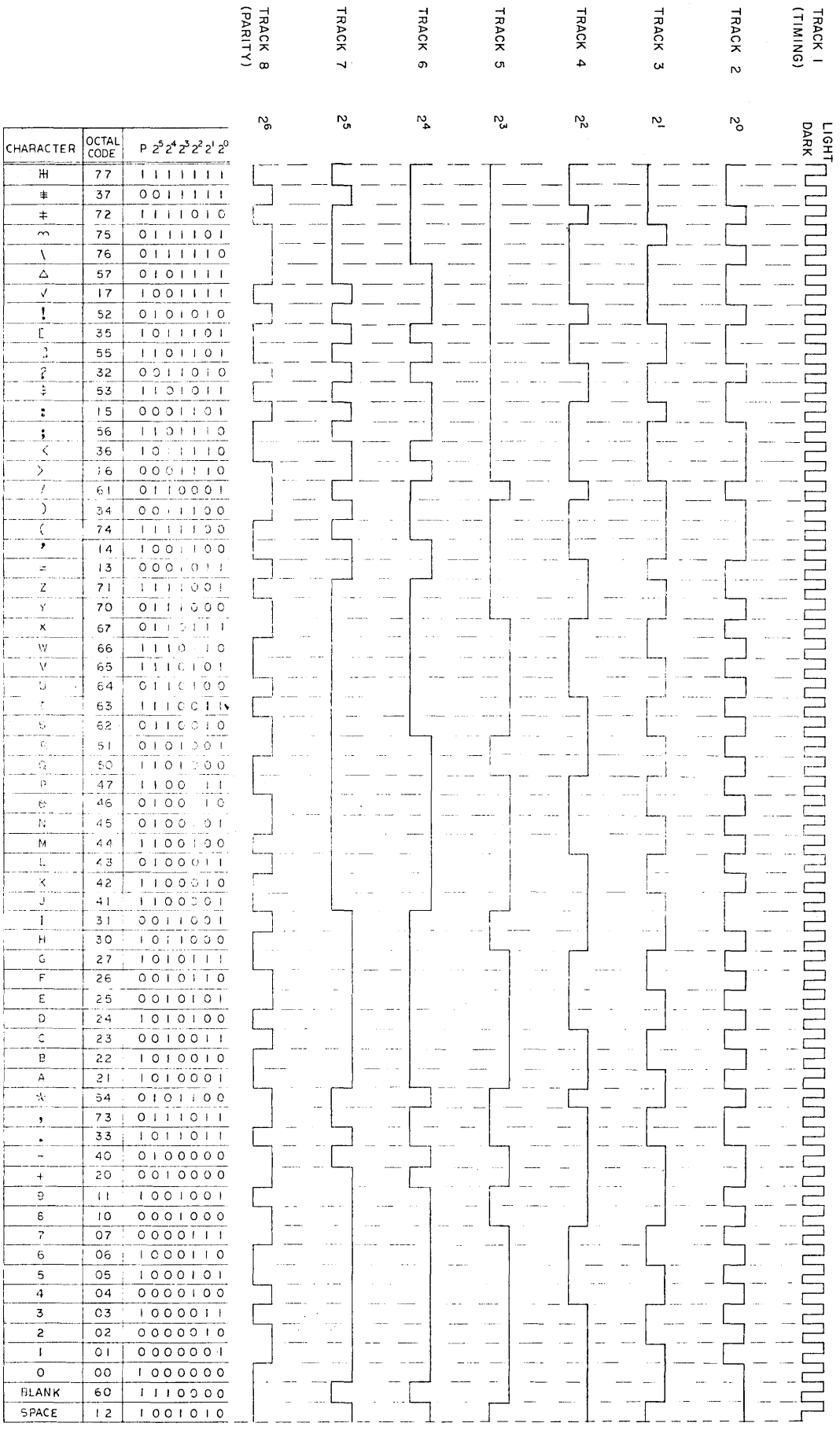
(c) A flag (sentinel bit) is reset when a character is printed. Therefore, as soon as the last character scan is completed, regardless of the amount of print drum rotation since the End Message signal, the Send Data signal becomes true.

(d) Low-usage characters are grouped together on the print drum. Therefore, with the paper advanced when these characters are passing the hammer, and data transmitted during the paper advance time, a continuous rate of approximately 360 lines per minute can be maintained.

(e) The paper feed advances the paper one line space in 30 msec. When the paper is to be advanced more than one line with a single paper feed instruction, the paper speed stabilizes at 20" per second (approximately 8 and 1/3 msec. per line).

3-31. Character-Drum Code Wheel.

3-32. Figure 3-10 provides character-drum code-wheel timing and coding information.



CHARACTER	OCTAL CODE	P 2^5 2^4 2^3 2^2 2^1 2^0
##	77	1 1 1 1 1 1 1 1
#	37	0 0 1 1 1 1 1 1
≠	72	1 1 1 1 0 1 0
~	75	0 1 1 1 1 0 1
\	76	0 1 1 1 1 1 0
Δ	57	0 1 0 1 1 1 1
√	17	1 0 0 1 1 1 1
!	52	0 1 0 1 0 1 0
[	35	1 0 1 1 1 0 1
]	55	1 1 0 1 1 0 1
?	32	0 0 1 1 0 1 0
÷	53	1 1 0 1 0 1 1
:	15	0 0 0 1 1 0 1
;	56	1 1 0 1 1 1 0
<	36	1 0 1 1 1 1 0
>	16	0 0 0 1 1 1 0
/	61	0 1 1 0 0 0 1
)	34	0 0 1 1 1 0 0
(	74	1 1 1 1 1 0 0
'	14	1 0 0 1 1 0 0
=	13	0 0 0 1 0 1 1
Z	71	1 1 1 1 0 0 1
Y	70	0 1 1 1 0 0 0
X	67	0 1 1 0 0 1 1
W	66	1 1 1 0 0 1 0
V	65	1 1 1 0 1 0 1
U	64	0 1 1 0 1 0 0
T	63	1 1 1 0 0 1 1
S	62	0 1 1 0 0 1 0
R	61	0 1 0 1 0 0 1
Q	60	1 1 0 1 0 0 0
P	47	1 1 0 0 0 1 1
O	46	0 1 0 0 0 1 0
N	45	0 1 0 0 0 0 1
M	44	1 1 0 0 1 0 0
L	43	0 1 0 0 0 1 1
K	42	1 1 0 0 0 1 0
J	41	1 1 0 0 0 0 1
I	31	0 0 1 1 0 0 1
H	30	1 0 1 1 0 0 0
G	27	1 0 1 0 1 1 1
F	26	0 0 1 0 1 1 0
E	25	0 0 1 0 1 0 1
D	24	1 0 1 0 1 0 0
C	23	0 0 1 0 0 1 1
B	22	1 0 1 0 0 1 0
A	21	1 0 1 0 0 0 1
*	54	0 1 0 1 1 0 0
,	73	0 1 1 1 0 1 1
.	33	1 0 1 1 0 1 1
-	40	0 1 0 0 0 0 0
+	20	0 0 1 0 0 0 0
9	11	1 0 0 1 0 0 1
8	10	0 0 0 1 0 0 0
7	07	0 0 0 0 1 1 1
6	06	1 0 0 0 1 1 0
5	05	1 0 0 0 1 0 1
4	04	0 0 0 0 1 0 0
3	03	1 0 0 0 0 1 1
2	02	0 0 0 0 0 1 0
1	01	0 0 0 0 0 0 1
0	00	1 0 0 0 0 0 0
BLANK	60	1 1 1 0 0 0 0
SPACE	12	1 0 0 1 0 1 0

Figure 3-10. Timing Diagram, 64 Character Code Wheel

SECTION IV

THEORY OF OPERATION

4-1. INTRODUCTION

4-2. This section contains the theory of operation of the Model dp/p-3310 buffered LINE/PRINTER. The theory discussions in this section are divided into the following three catagories: (1) general theory, (2) detail theory, and (3) printed-circuit cards and d-c power supplies theory. Mnemonic information, logic formulae, and a detailed block diagram are also included in this section.

4-3. GENERAL THEORY

4-4. Circuits and Elements, Block Description

4-5. The LINE/PRINTER, for purposes of explanation, is divided into the following ten functional elements: (1) memory register, (2) address register, (3) core buffer, (4) character drum and code wheel, (5) compare logic, (6) hammer logic, (7) paper drive and control, (8) ribbon drive and control, (9) output signal logic, and (10) timing and control. These elements are shown in figure 4-1.

4-6. Memory Register. The memory register, during the loading cycle, receives the input data-and-parity bits or paper feed instruction bits from the computer and transfers this information to the core buffer or paper tape register, respectively. During the printing cycle, the memory register receives the read-out character information from the core buffer for transmission to

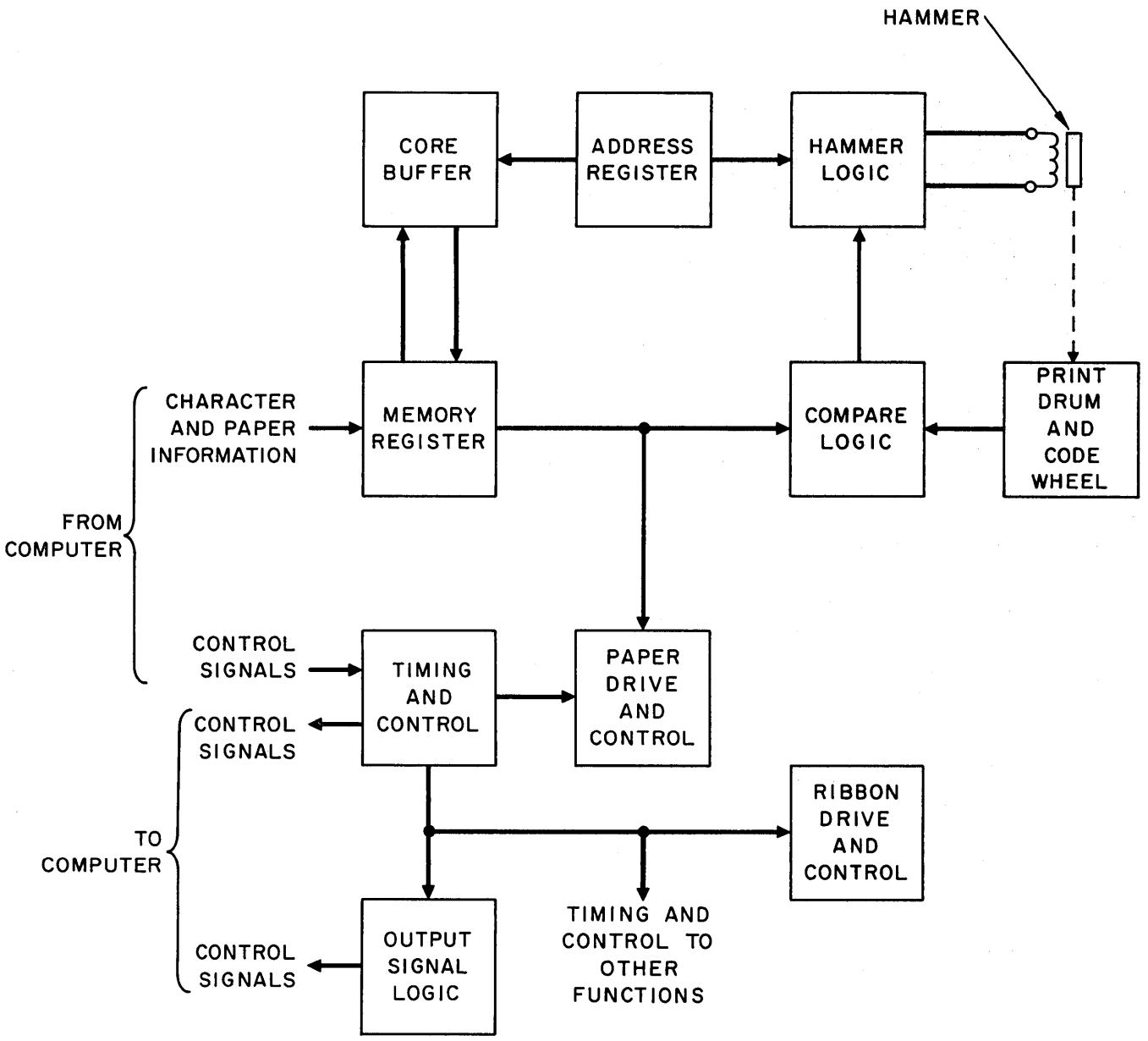


Figure 4-1. Simplified Block Diagram

the compare logic, and re-stores it into the buffer. This register also holds and controls a sentinel bit. (The sentinel bit is added to the character information during initial storage, and removed if the character is compared before re-storing).

4-7. Address Register. The address register is an 8-bit binary counter. The address held in this register at any time corresponds to both a core buffer location and to a particular hammer.

4-8. Core Buffer. The core buffer, during the loading cycle, sequentially receives and stores the 132 characters from the memory register. (This corresponds to one printed line.) During the printing cycle,the core buffer unloads and re-stores information from,and to,132 unique locations in accordance with the address register contents. Timing signals are provided by the control circuitry.

4-9. Character Drum and Code Wheel. The character drum contains 64 lines of unique characters spaced equally about the circumference of the drum. Each line contains 132 equally spaced characters of the same type. An attached optical code wheel contains seven binary-code tracks which continuously indicate which line of characters is in printing position, and the state of the associated parity bit. An eighth track on the code wheel provides timing information. Photo-diodes and amplifiers convert the print drum character positions into digital information, and provide timing signals to sequence printer operations.

4-10. Compare Logic. The compare logic receives the print drum character position from the code wheel circuitry, and the core

buffer character information from the memory register. The compare logic then compares the data for equality and parity and determines when a character is to be printed.

4-11. Hammer Logic. The hammer logic contains decoding and selection circuitry to select particular hammers in accordance with address register information and compare logic signals. Hammer driver receivers, which operate as memory elements for the hammers; and hammer drivers, which switch the currents to actuate the individual hammers, are also contained in this hammer logic.

4-12. Paper Drive and Control. The paper drive motor is stepped in response to current switching in its field coils. The paper drive control circuitry switches these currents in response to paper feed instructions contained in the paper feed tape loop. This circuitry also drives the paper to the top of form position when the top of form switch (on the control panel) is actuated.

4-13. Ribbon Drive and Control. The ribbon drive motors maintain continuous tension in the ribbon, and drive the ribbon in a skewed path relative to the line of characters on the print drum. The control circuits operate the drive motors as necessary, and reverse the drive direction at both ends of the ribbon.

4-14. Output Signal Logic. The output signal logic provides outputs to the computer to indicate ability of the printer to receive information. These circuits also transmit printer status information to the computer.

4-15. Timing and Control Circuits. The timing and control circuits

contain a gated 500-kc clock, control flip-flops, and AND gates. These circuits produce the timing and control signals that are necessary to sequence the various modes of printer operation.

4-16. Power Supplies. The power supplies generate the various d-c voltages required by the printer logic, and the various lamp voltages. Control circuitry provides automatic sequencing of power supply turn-on and turn-off operations.

4-17. Circuits and Elements, Functional Description.

4-18. The following paragraphs provide a functional description of the printer operation.

4-19. Character Loading. Figure 4-2 shows the printer elements which are in use during the loading of character information from the computer. These elements operate as follows:

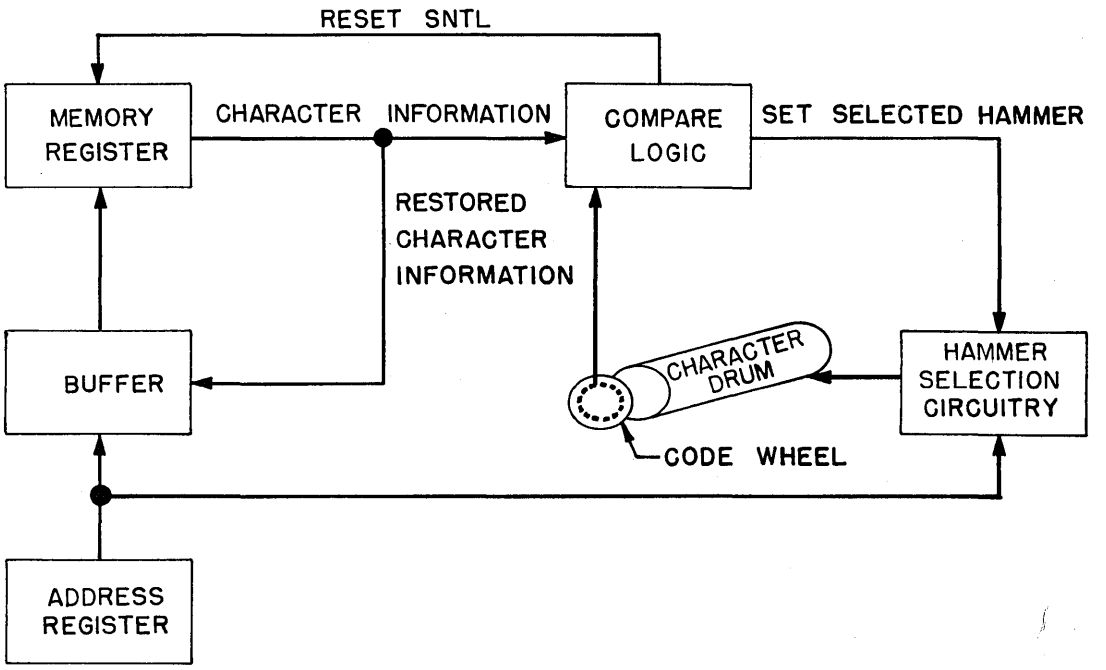
(a) Prior to loading of character information for a line, the address register and the memory register are reset.

(b) A Send Data signal from the printer indicates to the computer that the printer can accept character information.

(c) The six data bits and corresponding odd parity bit are applied to the printer on seven input lines.

(d) The Character Strobe from the computer initiates the loading of the character, disables the Send Data signal to the computer, and enables the printer 500-kc clock.

LOADING



COMPARING AND PRINTING

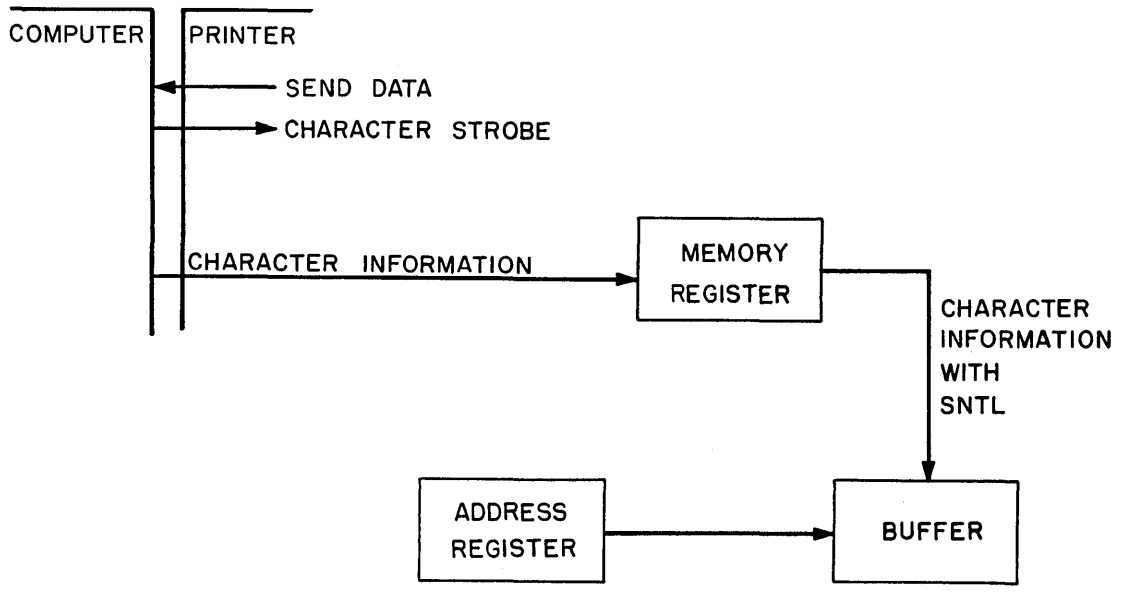


Figure 4-2. Printer Operation, Simplified

(e) A clock pulse strobes the information on the seven input lines into the seven corresponding memory register stages and sets a sentinel flip-flop in the 8-bit memory register.

(f) During information loading, each address of the core buffer, as sequentially selected by the address register, is first cleared and then loaded.

(g) The first character strobed into the 8-bit memory register is loaded into the core buffer at the all-zeros address. (The address of a loaded character also establishes the line position of the character when printed; thus, the character at the all-zeros address (first address) will be the first character on the printed line).

(h) Following the loading of information into the core buffer, the address register is advanced by one, and the Send Data signal is again enabled.

(i) Subsequent Character Strobe pulses cause the repetition of the above-described cycle 131 times (at which time a full line has been loaded into the buffer). Note that each time a character is loaded into the core buffer, a ONE sentinel bit is also generated and loaded with the character. During the transmission of the last character, and End of Line signal from the computer disables the Send Data signal until the stored line has been printed.

4-20. Printing. Figure 4-2 shows the printer elements which are in use during comparing and printing of a line. The operation is as follows:

(a) Prior to printing a line, the address register and the memory register are reset. Each of the characters in the core buffer is accompanied by its transmitted parity bit and a ONE sentinel bit (the sentinel bit was added during loading by printer circuitry).

(b) Figure 4-3 shows the printer timing which is derived from the character drum code wheel. At the left of the figure, the code wheel data outputs are shown switching to the code which indicates that the character 'N' is approaching the hammer bank.

(c) A Pure Code strobe pulse initiates a 0.1-usec delay to ensure correct character read-out from the code wheel. The Start Scan Gate (Reset Ribbon Drive pulse) is then generated. Since the printer is in the print mode, the generation of this gate enables the 500-kc clock and initiates a Character Scan. A Character Scan consists of 132 read-and-compare cycles as described in step d, below.

(d) The core buffer now operates in its load-and-re-store mode. The character in the core buffer at the all-zeros address is transferred into the memory register. The ONE sentinel bit in the memory register (accompanying the character) indicates that the character

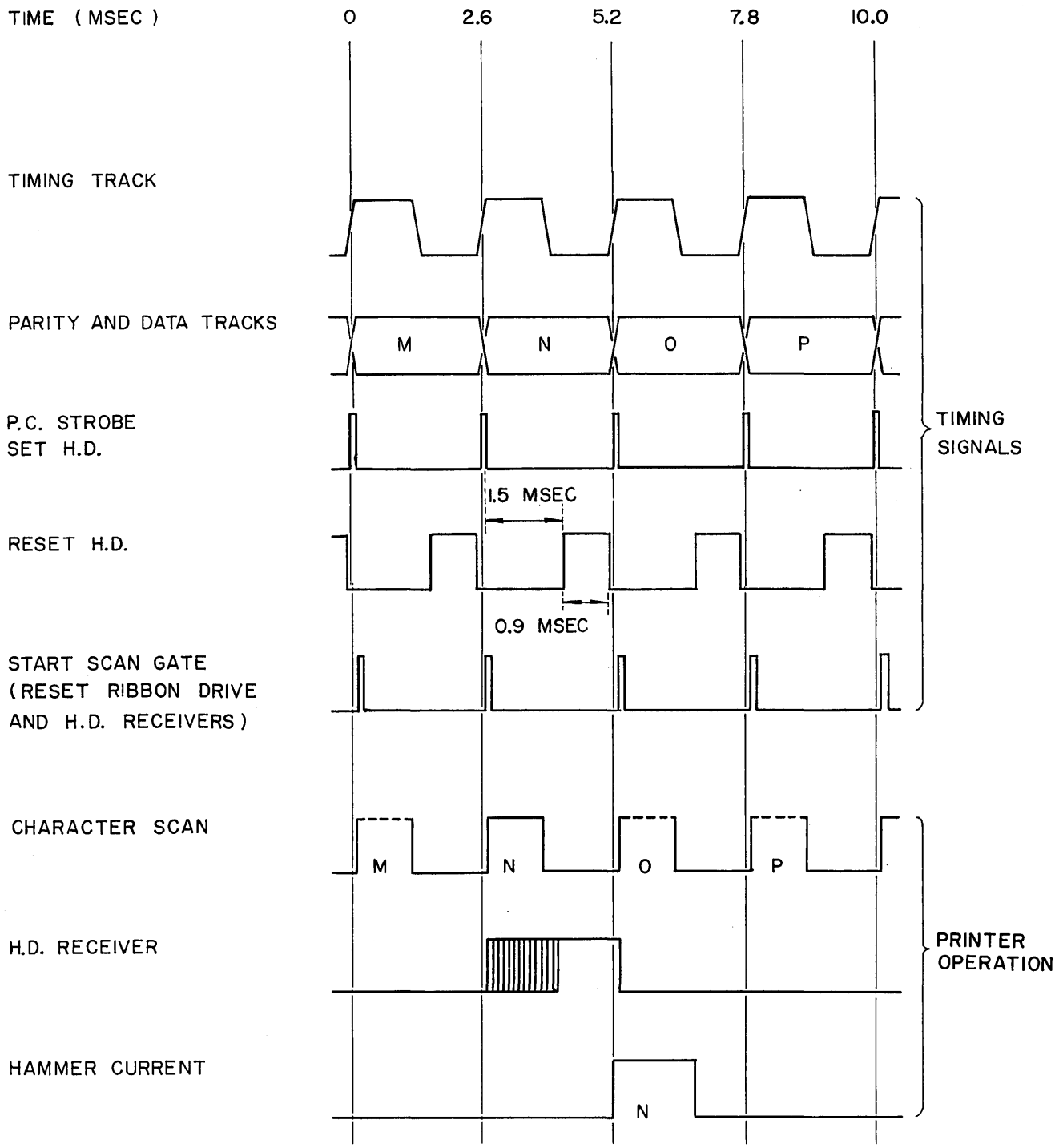


Figure 4-3. Printer Timing

information has not been printed. The six data bits of the all-zeros-address character are then compared with the six corresponding data bits (character 'N') from the code wheel. If these two 6-bit words are unequal, the ONE sentinel bit sets the sentinel indicating flip-flop (FF_S). With no character comparison, the data bits, parity bit, and ONE sentinel bit in the memory register are re-stored into the core buffer at the all-zeros address. The memory register is now reset, the address register is advanced by one, and the above steps are repeated for a total of 132 times. At the conclusion of the 132 cycle, the address register is reset, and the 500-kc clock is disabled. One complete character scan has now been performed. During a Character Scan, if the Sentinel bit in the memory register is ONE and the character in the memory register is equal to the code-wheel character, the parity of the 6-bit memory register character word is checked. When the parity is correct, the ONE Sentinel bit is reset to ZERO to indicate, during subsequent Character Scans, that the character has been printed. As shown in figure 4-3, the hammer driver receiver corresponding to the address of the character is energized. Each Start Scan gate initiates a 132-cycle character scan as described above. At the end of each character scan, the state of the sentinel

indicating flip-flop is sensed. A set Sentinel indicating flip-flop indicates that unprinted characters remain in the core buffer. The Sentinel indicating flip-flop is then reset. If the indicating flip-flop is reset when sensed, all characters for the line stored in the buffer have been printed. The printer is ready to accept more character information or paper drive information. A parity error detected during the preceding printing operation will terminate printing immediately, apply a parity error signal to the computer, and switch the printer to the loading condition.

(e) As shown in figure 4-3, the one or more hammer drivers for a particular character are set when the address register holds the corresponding address. The next Set Hammer Driver pulse switches on the hammer currents. The hammer driver receivers are reset by the Reset Hammer Driver signal, which is coincident with the next start scan gate. The Hammer Drivers signal resets all energized hammer drivers (the actual time of impact of the hammer follows the hammer current turn-off).

4-21. DETAIL THEORY

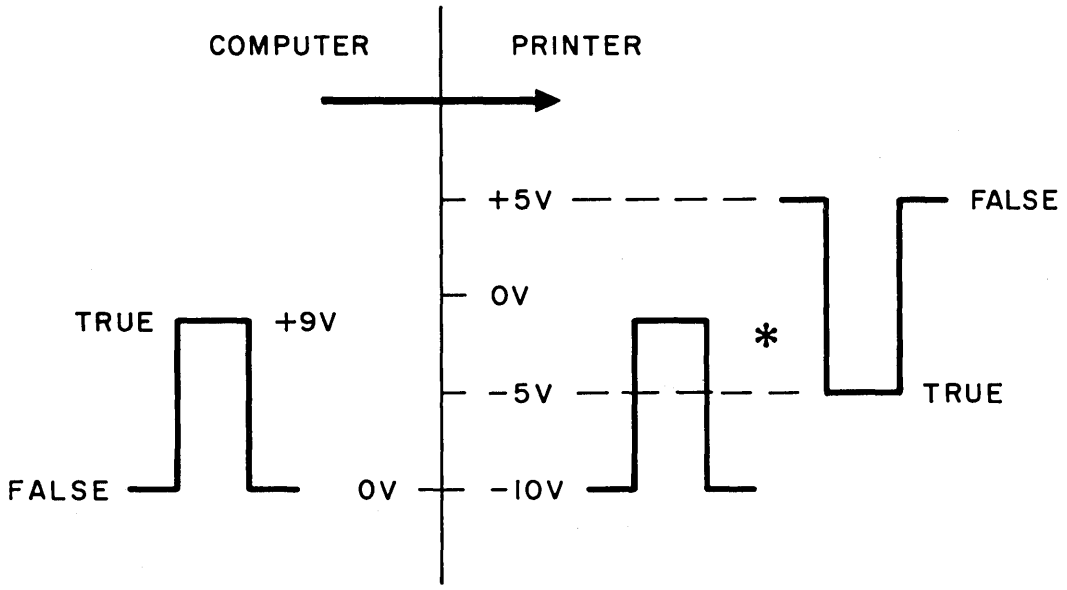
4-22. The following paragraphs provide detailed operational theory of the various functions of the printer. The detail theory, divided into printer functional areas, appears in the following paragraphs in the order listed: (1) logic levels and polarities,

(2) timing, (3) memory register, (4) address register, (5) core buffer, (6) compare circuits, (7) hammer drivers and receivers, (8) paper drive circuitry, (9) ribbon drive and Control, (10) timing distributor, (11) output signal logic, (12) control logic, (13) printer clear operation, (14) printer overall operation, and (15) power circuitry. Logic diagrams, referenced in the following paragraphs, are located in Section VI. Refer also to the detailed block diagram at the rear of this section.

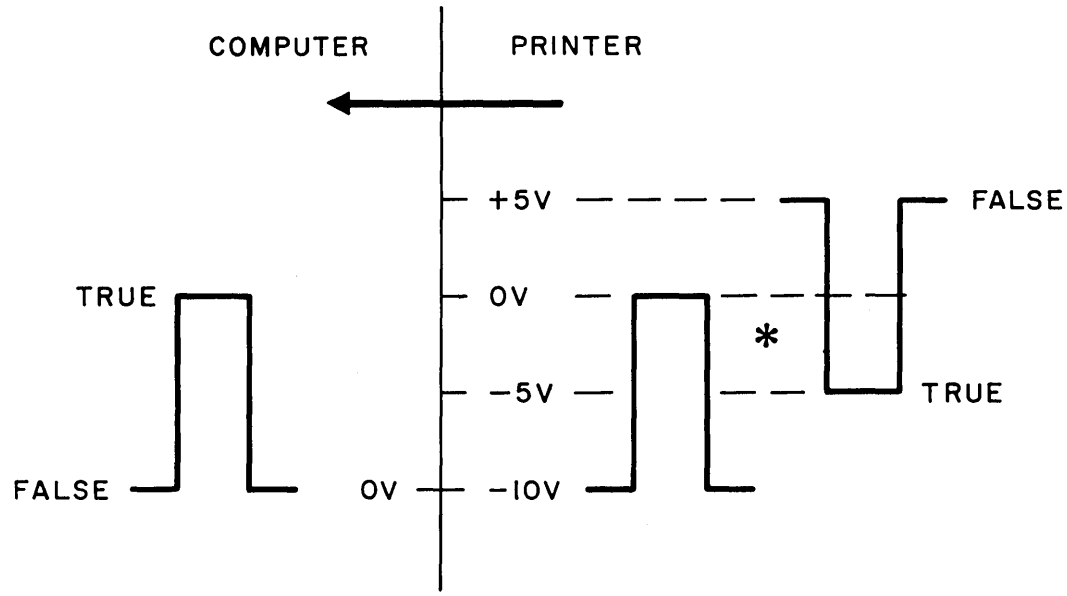
4-23. Logic Levels and Polarities

4-24. The printer operates internally with +5 volts and -5 volts for ZERO and ONE, respectively. The computer input signals to the printer are 0 volts and +9 volts for ZERO and ONE, respectively. Matching of these signals is accomplished as shown in figure 4-4. The printer -10 volt d-c power supply output is supplied through the input-output connector to the computer, and is connected to the computer 0-volt line. Input signals thus appear as -10 volt and -1 volt signals to the printer at the interface. Input signals are applied to logic receivers, which are essentially differential amplifier circuits. The printer applies -5 volts d-c to these circuits as the reference voltage, and inverts the output. The output is then at the printer logic levels.

4-25. Conversely, the printer logic levels are +15 and -5 volts with reference to the computer. These signals are applied to the computer through output drivers which have the clamp voltages connected to the -10 volt printer d-c power supply. The output



(a) INPUT SIGNALS



(b) OUTPUT SIGNALS

* LOGIC RECEIVERS PERFORM LEVEL SHIFTING WITHIN PRINTER.

Figure 4-4. Logic Levels and Polarities

signals are switched between 0 volts and -10 volts in the printer, and appear at the computer as 0 volts and +10 volts for ZERO and ONE, respectively.

4-26. Timing.

4-27. The printer contains two timing sources: The timing track on the character-drum code wheel, and a gated 500-kc clock. The code-wheel timing track provides one pulse per drum character; thus, with a 64-character drum operating at 360 RPM (6 RPS), a 384-cps (approximately 2.6 ms) signal is generated. This signal is delayed and amplified, as necessary, for various printer functions.

4-28. The gated 500-kc clock in the timing distributor, when enabled, produces four timing pulses (T1, T2, T3, and T4), each separated by 2-usec intervals. This 4-pulse sequence is continuous until the clock is disabled. The timing clock also provides core buffer timing. Operation is generally as follows (a detailed description of the Timing Distributor is found elsewhere in this section).

(a) When loading information from the computer, the Character Strobe enables the clock. The clock is self-disabled by T4. Thus, the clock generates one 4-pulse sequence to time the loading of each input character.

(b) During a character scan, the clock operates continuously for 132 4-pulse sequences and is then disabled.

4-29. Memory Register

4-30. General. (See Logic Diagram 33). The memory register

receives 7-bit data words from the computer during data-loading operations, for subsequent transfer to the core buffer. Three-bit paper tape instructions are also held in the memory register, and are transferred to the paper tape register directly from the memory register. During character scan operations, the memory register holds the read-out data of the core buffer for comparison with the code wheel bits (the compared data is subsequently re-stored into the core buffer.

4-31. Input Data Input. During the turn-on sequence and at the completion of each character loading operation, a T4 timing pulse clears all memory register stages. With FF_R set (printer ready for data-loading operation) a T1 timing pulse is applied to the seven logic receivers (acting as AND gates) connected to the inputs of the seven memory register flip-flops. Incoming data from the data source is also applied to the logic receivers. Each logic receiver to which the data source applies a ONE sets its corresponding memory register flip-flop. Logic receivers to which ZEROs are applied allow their respective memory register flip-flops to remain in the reset (ZERO) state. During each character loading cycle, timing pulse T2 accompanied by the set FF_R and reset FF_{pf} outputs is applied to the eighth logic receiver (Sentinel). The output of the Sentinel logic receiver will then set the memory register Sentinel flip-flop. (The set FF_R signal indicates that the printer is in the data-loading operation; the reset FF_{pf} signal indicates that the input data received during T1 time was not a paper feed instruction.

4-32. Core Buffer Input. During the compare and print operation the eight memory register flip-flops receive inputs from the core buffer read-amplifiers (acting as AND gates). With FF_R reset, indicating the compare and print operation, the T1 timing pulse is applied as a strobe pulse to the read amplifiers. Read amplifiers receiving readout signals corresponding to stored ONEs set the corresponding memory register flip-flops. Read amplifiers which receive readout signals corresponding to stored ZEROs allow their corresponding memory register flip-flops to remain reset.

4-33. Address Register

4-34. General. (See figure 4-5 and logic diagram 34). The address register is an 8-bit binary counter with a cascaded carry to each stage. The register is cleared by a signal from the control circuitry which resets each stage.

4-35. Core Buffer Addressing. The address register holds the address of the core buffer location into which character data is being loaded, or from which it is being unloaded. The register operates in cycles from 0 (count 1) to 131 (count 132).

4-36. Hammer Addressing. Each address, in addition to corresponding to a unique core buffer address, also corresponds to a particular hammer address; the address register stage outputs are applied to both the core buffer decoding circuits and to the hammer address decoders.

4-37. The address register logic also determines when the count of 131 has been reached (when 132 cycles have been completed).

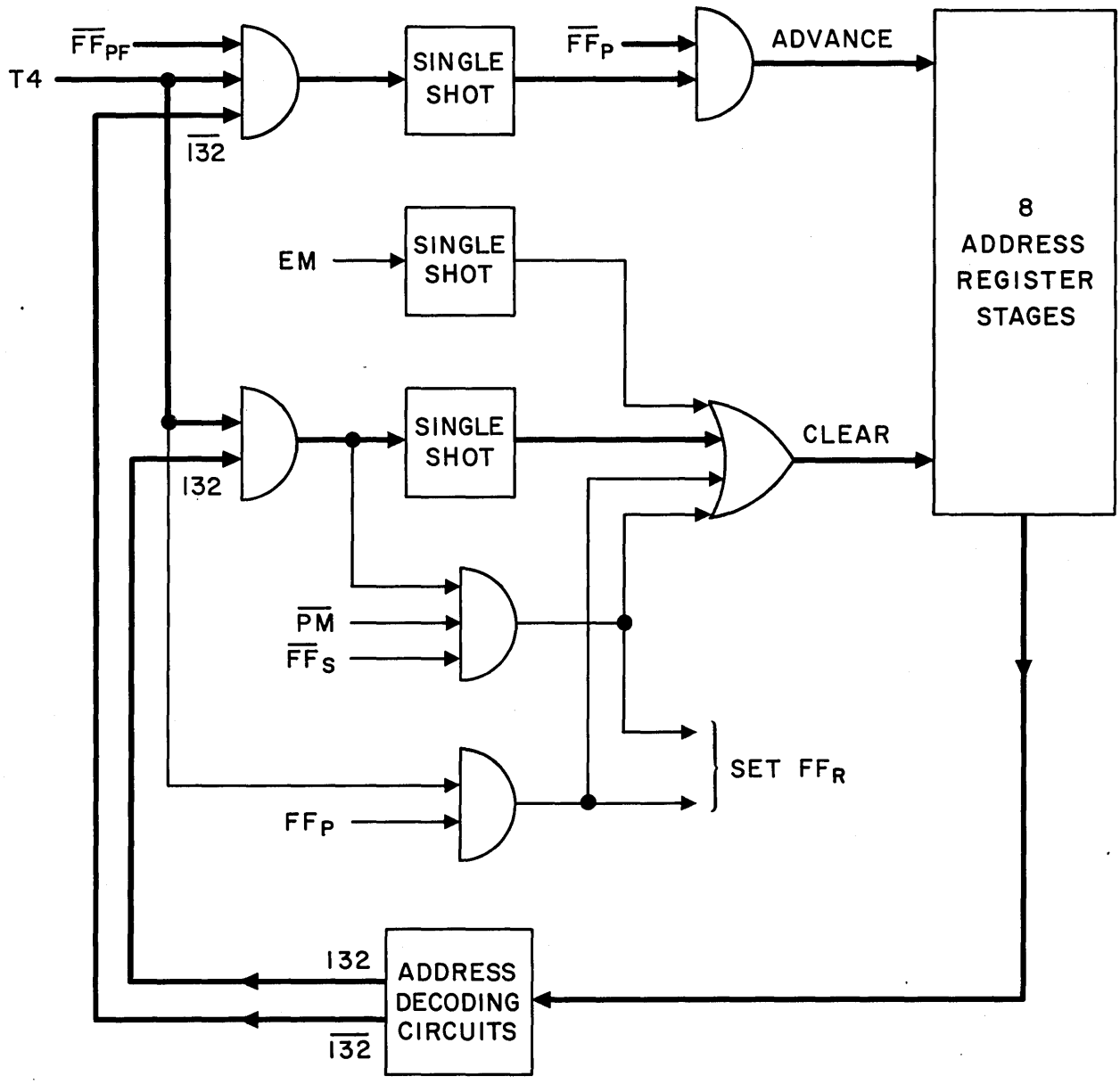


Figure 4-5. Address Register Logic

At the end of each character scan of 132 sequential addresses, the address register is cleared.

4-38. Core Buffer.

4-39. General. The core buffer stores all information for a complete line (during loading), and is scanned once for each character on the drum (during the compare and print cycle). The core buffer is controlled by the address and accepts data from, and applies data to, the memory register.

4-40. Core Operation. Core buffer operation is based on the properties of the magnetic cores which enable them to store and unload data. Each magnetic core is intersected by four windings: the X drive winding, the Y drive winding, the inhibit winding, and the sense winding. The X and Y drive windings intersect all cores at a particular address, the inhibit winding is used only when storing data, and the sense winding is used only when unloading data.

4-41. Each core operates with a hysteresis loop as shown in figure 4-6. With one turn through each core, a current $-I_2$ will drive the core to the ZERO state as shown. Removal of this current returns the core to its magnetized state $-H_1$. A current of the opposite direction $+I_2$, applied to a core in the ZERO state, will switch it to the ONE state, as shown. This is the current produced by two equal drive currents applied to the core. Cores on active X or Y drive windings which receive only one drive current $+I_1$ or $-I_1$ are not switched.

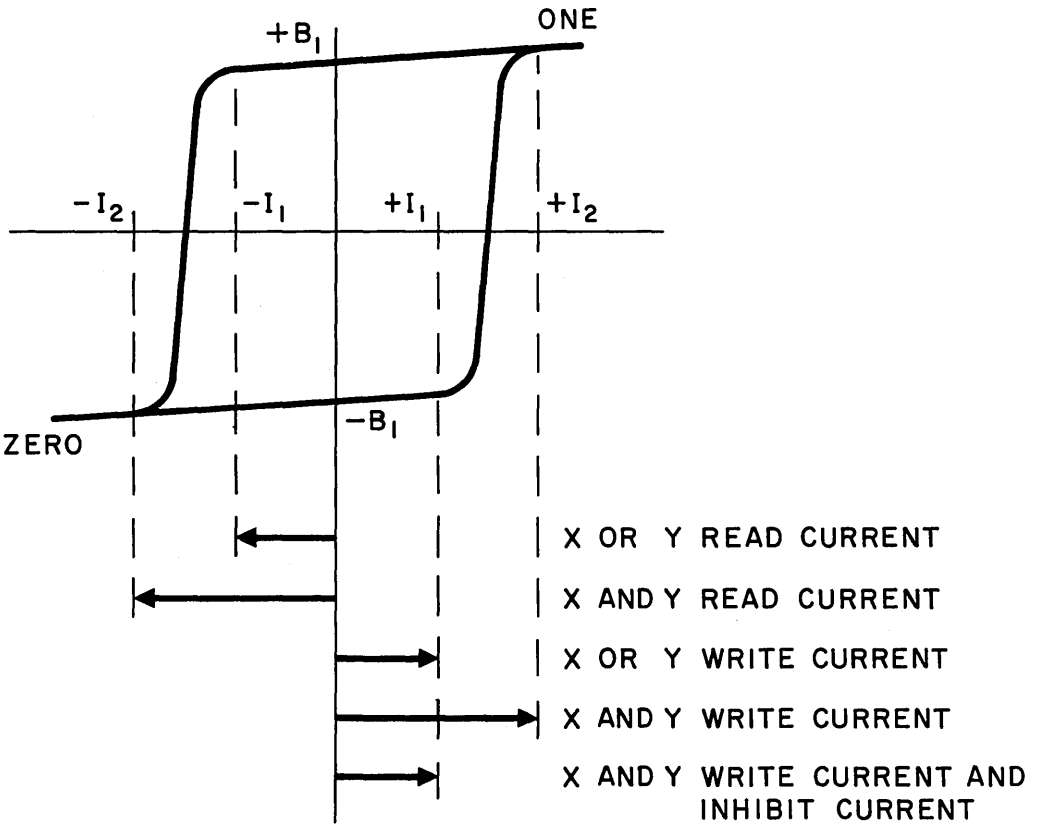


Figure 4-6. Magnetic Core Hysteresis Loop

4-42. The inhibit current, when applied, is approximately equal to a drive current and is applied in a direction to oppose the action of the drive currents. Thus, when an inhibit current and the two drive currents are applied to a core in its ZERO state, it is not switched. Removal of these currents leaves the core in its ZERO state.

4-43. Unloading of the information contained in a magnetic core is accomplished by applying read drive currents, which are equal to the write drive currents, but flow in the opposite direction. (No inhibit currents are applied during unloading). Application of the read drive currents thus drives all cores to their ZERO states as previously described. All cores in a plane are intersected by a sense winding, in which a core changing its magnetization induces a signal. As shown in figure 4-7, application of read drive currents to a core in the ZERO state drives the core in the direction in which it is already magnetized, with a small flux change. A small signal is induced in the sense winding. However, when the read drive currents switch a core from its ONE state to its ZERO state, a large flux change is produced.

4-44. The sense winding produces a double-ended signal. Due to the method of routing the various windings, the readout signals may be of either polarity. The read amplifiers reject the small signals produced from a ZERO readout and amplify the larger signals produced by ONE readouts. Thus, a core is capable of loading, storing, and unloading a ZERO or a ONE. Each core is driven to its ZERO state (cleared) just prior to loading new information.

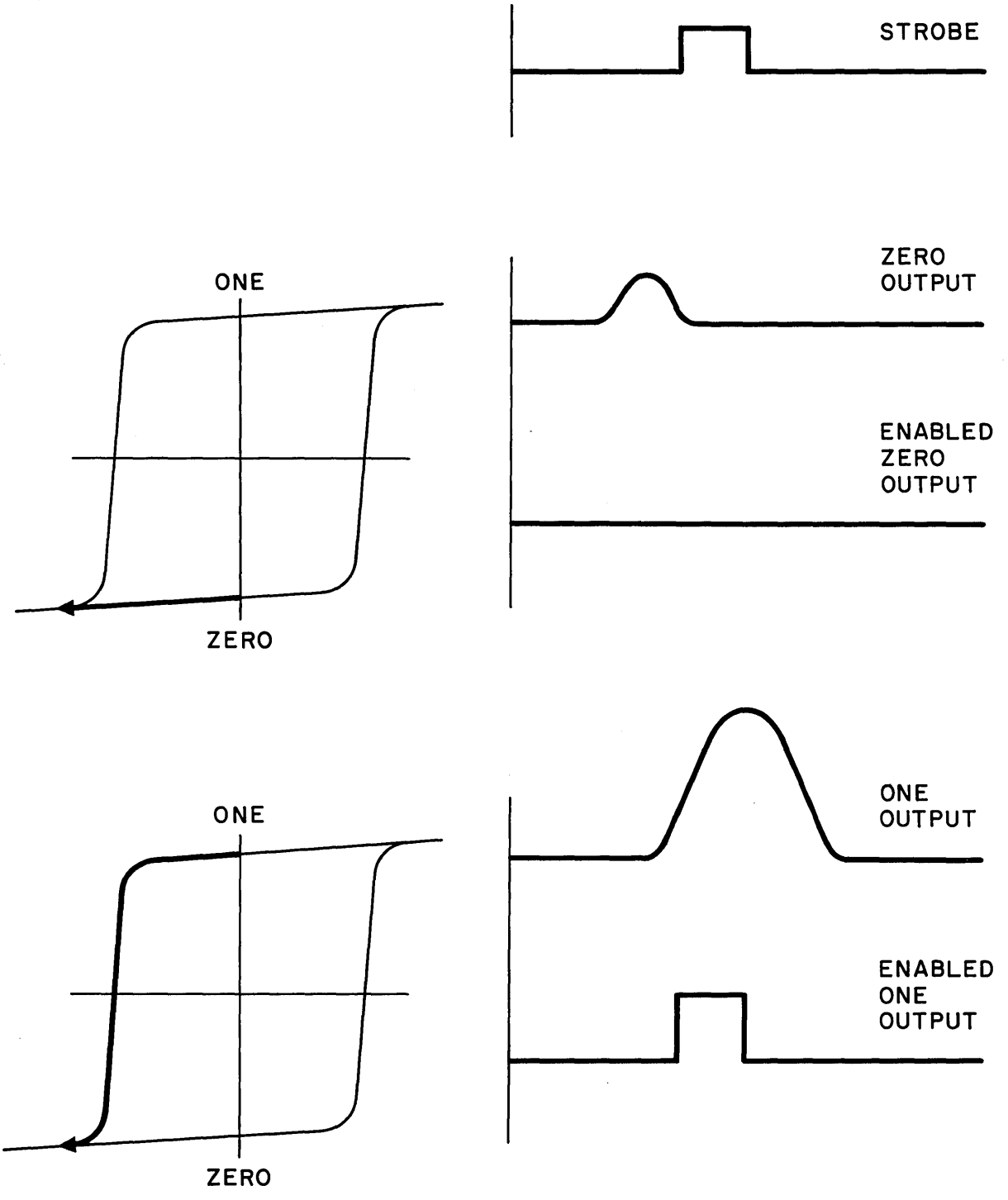


Figure 4-7. Magnetic Core Readout Signals

The readout of information is destructive; thus, when information is read from the core storage for comparison, it is re-stored into the cores by a load cycle.

4-45. Buffer Operation. The core buffer stores 132 8-bit words. Each word is comprised of six data bits, a parity bit, and a sentinel bit. Thus, eight cores are located at each address location of the buffer. The intersections of the eight X drive lines (X0 through X7) with the 17 Y drive lines (Y0 through Y16) provide a total of 136 addresses (only 132 of these are used).

4-46. The three address register stages which hold the three least significant address bits control the eight X drive lines; the five address register stages which hold the other five address bits control the 17 Y drive lines. The identification of each drive line corresponds to the binary number held in the corresponds to the binary number held in the corresponding part of the address register.

4-47. Address Clearing (Input Data Loading). The first character to be printed on a line is always transmitted with all address register stages reset (holding ZEROs). Thus, the selection switches which control drive lines X0 and Y0 are enabled. (Refer to simplified information loading schematic, figure 4-8). Read currents turned on at this time are routed through the X0 and Y0 drive lines, and drive the eight intersected cores to their ZERO states.

4-48. Writing (Input Data Loading). The address register contents are not changed between the read and write core buffer

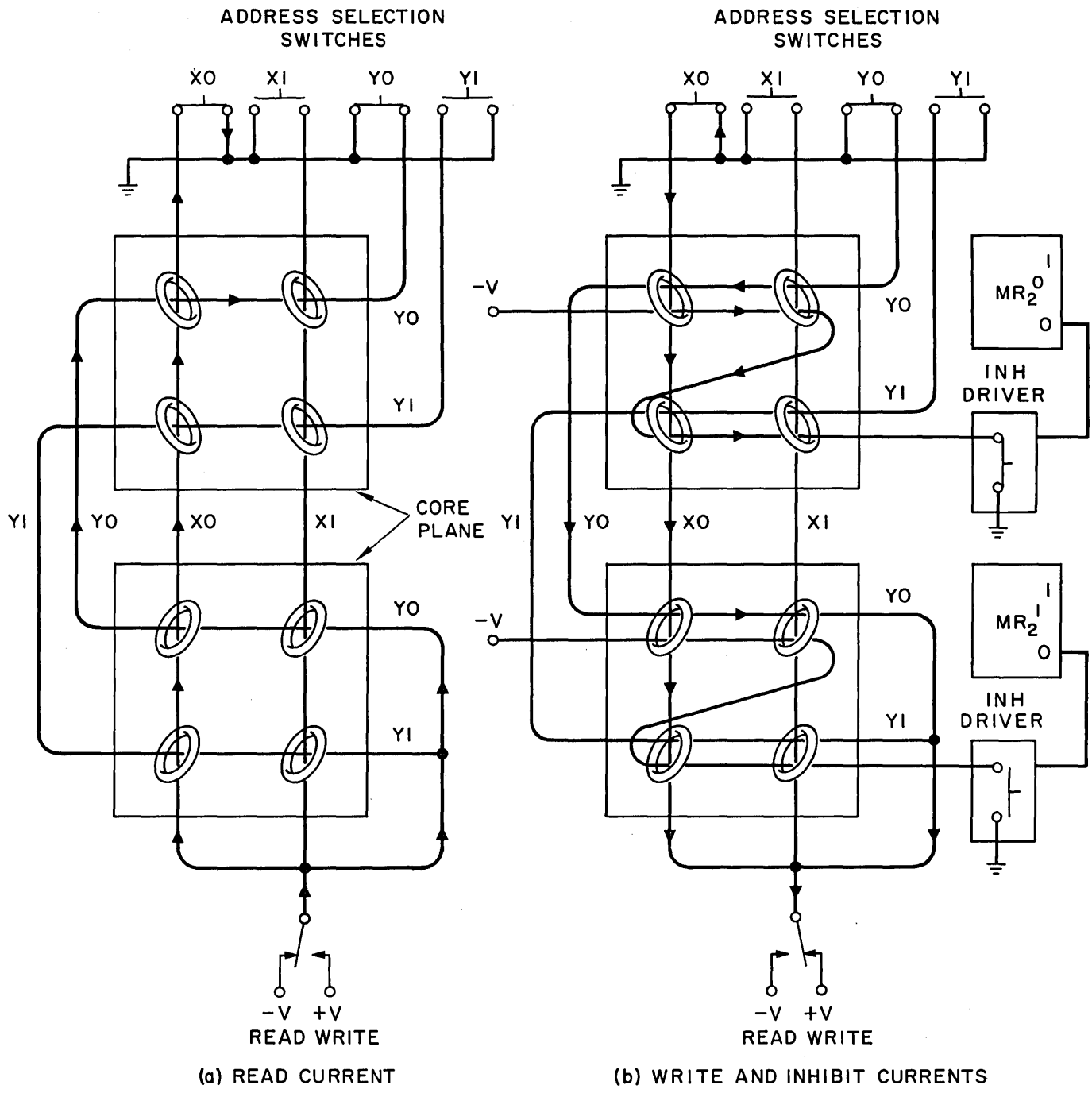


Figure 4-8. Simplified Information Loading Schematic

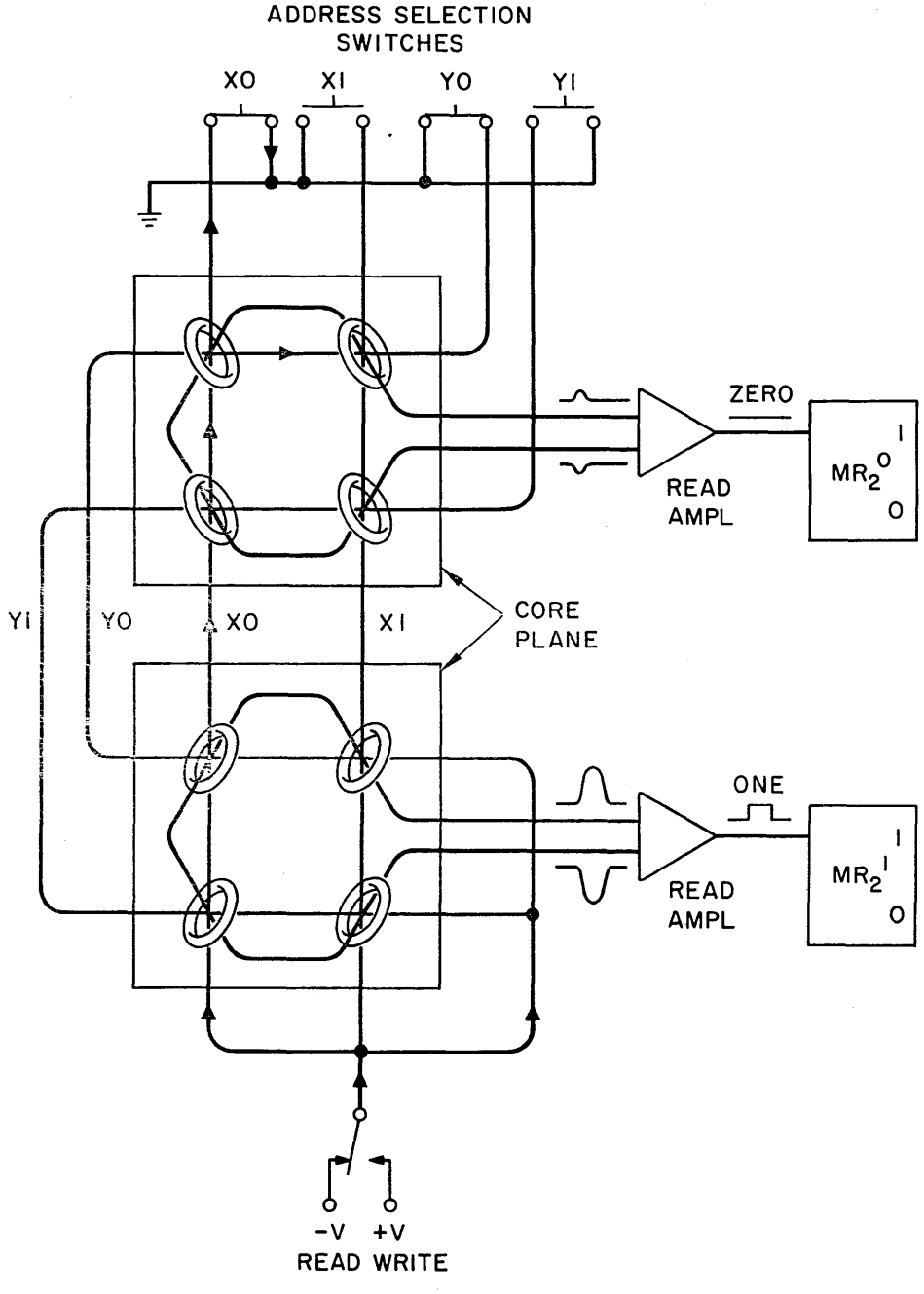
modes. The X0 and Y0 selection switches remain enabled. Following turn-on of the inhibit currents in those core planes in which ZEROs are to be loaded, the write drive currents are switched on. The X0 and Y0 selection switches route write drive currents through the eight cores which were driven to their ZERO states by the read drive currents. The write drive currents are approximately equal to the read drive currents. However, their direction is opposite to the read current direction; the write current tend to drive the eight cores to their ONE states. Cores in which inhibit current is not enabled are switched to ONEs. Inhibit current flows in the inhibit windings of the other cores; these cores are not switched. Since inhibit currents are driven through the cores corresponding to reset (ZERO) memory register stages, the eight cores at this address now hold the same information as the memory register stages.

4-49. Subsequent Address Clearing and Writing (Input Data Loading). Following the above cycle, the memory register is cleared, the address register is advanced by one, and new information is placed in the memory register. The least significant bit of the address register is now a ONE; all other address bits are ZEROs. The X0 selection switch is disabled; the X1 selection switch is enabled. The Y0 selection switch remains enabled since the most significant address register bits remain unchanged by this count.

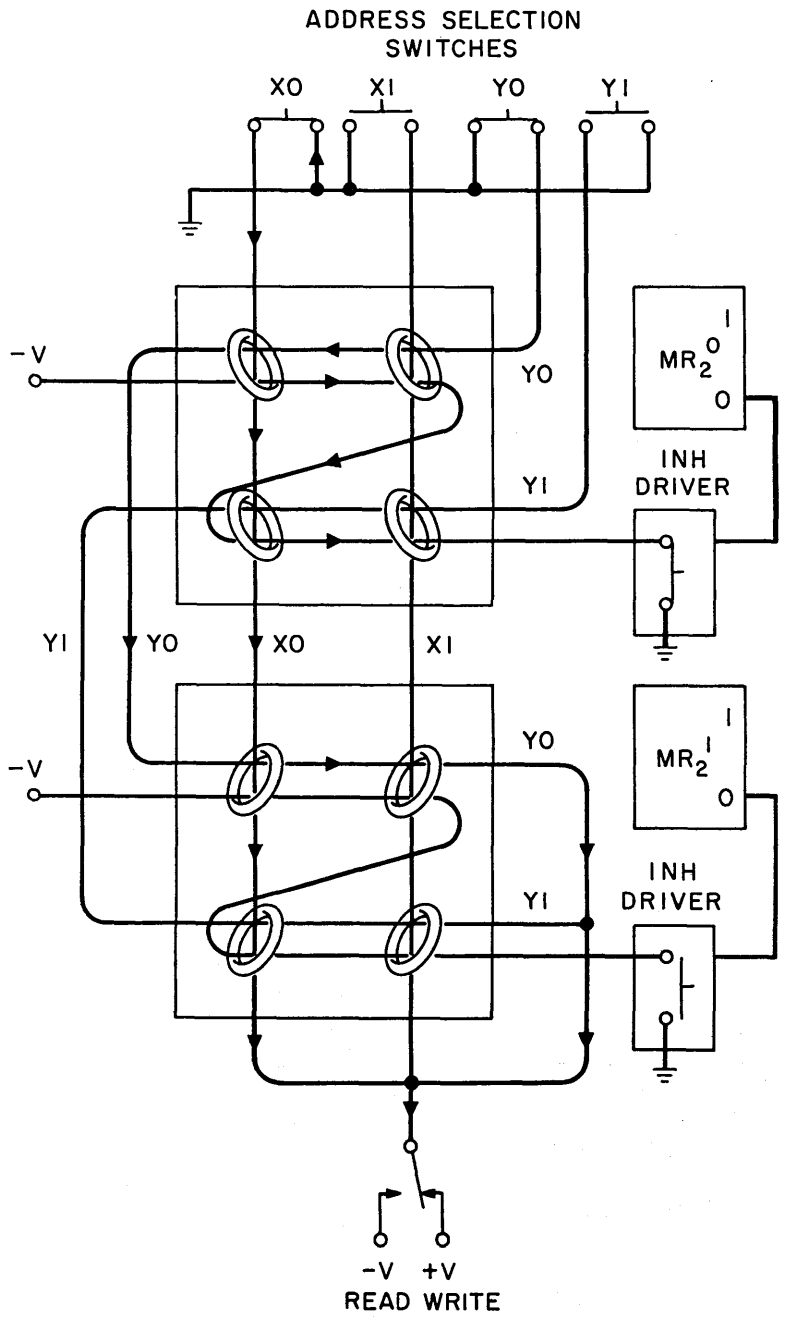
4-50. Read drive current is again switched on. The eight cores which are intersected by the X1 and Y0 drive lines are driven to their ZERO states, inhibit drivers corresponding to set (ONE)

memory register stages switch on inhibit currents, and write drive currents switch the intersected cores in which no inhibit current flows. These cycles are continued until 132 addresses have been loaded.

4-51. Unloading Buffer Data (Compare and Print). Unloading (reading) of the core buffer contents is similar to the above process, and takes place as follows (refer to simplified information unloading schematic, figure 4-9). With the address register reset, the X0 and Y0 switches are again selected. The read drive currents are switched on and are routed through the X0 and Y0 drive lines. The read-out signals are enabled, and the amplified and enabled read-out signals are applied to the corresponding memory register stages. Cores in which enabled inhibit drivers had provided an opposing inhibit current flow are not switched. The corresponding memory register flip-flops remain reset due to the low-amplitude read-out signals which are rejected by the read amplifiers. Cores in planes in which no inhibit current flowed (the corresponding memory register stages held ONEs) switch to their ZERO states and produce high-amplitude read-out signals. The resultant read amplifier output signals set the corresponding memory register flip-flops. The memory register stages now hold the same information which was stored when the address register held ZEROs during the input data loading sequence. As determined by the compare logic operation (refer to paragraph 4-53), the sentinel bit may be reset at this time. Otherwise, the memory register contents



(a) READ CURRENT



(b) WRITE AND INHIBIT CURRENTS

Figure 4-9. Simplified Information Unloading Schematic

are unchanged and inhibit currents are again switched on in the cores which held ZEROs. The write drive currents then re-store this read-out information (with the sentinel bit modified as necessary) into the cores at same address.

4-52. This cycle is repeated at each address (X1-Y0, X2-Y0,... X2-Y16, X3-Y16). This completes one character scan. Thus, with the exception of the sentinel bits which may be changed between the switching of read and write currents, the core buffer contains the same information at the end of a character scan as it contained when the character scan was started. Character scans are continued until one (character scan) is completed where all re-stored sentinel bits are ZERO. Three exceptions exist to the above and are as follows:

(a) END MESSAGE: When this signal is received, during Input data loading, before the count of 131 (the 132nd address), the address register is cleared. This has no effect on character scan cycles.

(b) PAPER INSTRUCTION: The address register is not advanced following loading of a paper instruction. The information at this address (all ZEROs) is not used and is replaced with character information before a character scan.

(c) PARITY ERROR: The address register is cleared to all ZEROs when a parity error is detected during a character scan.

4-53. Compare Circuits

4-54. General. (See detailed block diagram and logic diagram 35). The compare circuits become functional during the character scan cycles which are generated during the compare and print mode (refer to paragraph 4-20). The six code-wheel data bits are compared, by exclusive OR gates, with the six information bits in the memory register. A ONE output results when these two 6-bit words are equal. This output is then applied to the Parity Enabling AND gate along with the true output of FF_{SNTL2} (which is a ONE if the character has not been previously processed) and the false output of FF_P (which is a ONE if no parity error has been detected).

4-55. The output of the Parity Enabling AND gate is applied to the FF_P AND gate (which includes, as additional inputs, timing pulse T2 and the false output of FF_R). The inverted parity comparison from the code-wheel and memory-register is also applied to the FF_P AND gate. The parity comparison input is inverted so that when all other inputs to the FF_P AND gate are true, then a true parity comparison will disable the AND gate and prevent the generation of a set signal to the Parity Error flip-flop (FF_P). However, when a false parity comparison is produced (and all inputs to the FF_P AND gate are true), the AND gate is enabled, FF_P is set, and the following events occur: (1) Character Scanning is terminated, (2) the Address Register is cleared, (3) the Send Data signal becomes true to indicate that the

printer is ready to re-load the character information for the line, and (4) the Parity Error signal to the computer becomes true.

4-56. The output of the Parity Enabling AND gate is also applied to the Reset MR Sentinel AND gate (which also includes, as additional inputs, timing pulse T2 and the false output of FF_R). The Reset MR Sentinel AND gate (when all other inputs are true) is enabled or disabled by a true or false parity comparison, respectively. The enabled output of the Reset MR Sentinel AND gate resets the Sentinel flip-flop (FF_S) in the memory register and is also inverted and applied to the Decode Strobe AND gate. The other input to the Decode Strobe AND gate is the false output of the Space Decode AND gates. (The purpose of the Space Decode AND gates is to prevent the printing of certain selected characters, thus causing a space, instead of the compared character, to appear on the printed line). The output of the enabled Decode Strobe AND gate triggers a 1.0 usec single-shot which in turn generates a Set Ribbon Drive Signal and, after inversion, a Decode Strobe. These two signals (Set Ribbon Drive and Decode Strobe) are the primary outputs of the compare circuitry and result only when the following condicions are true: (1) FF_{SNTL2} is set, (2) FF_P is reset, (3) FF_R is reset, (4) The six memory register data bits are each equal to the corresponding code wheel data bits, (5) The memory register data word parity is correct, and (6) The memory register does not contain a character selected to provide a space.

4-57. Character-Drum Code Wheel

4-58. The character-drum code wheel (attached to, and aligned with, the character drum) is a plastic disc containing eight circular tracks. Each track consists of clear and opaque areas which, when illuminated by a light source, produce binary optical codes. Six of these tracks provide the character codes (one bit per track) of the drum characters with which they are aligned, thus indicating which line of characters on the character drum is in print-position. The seventh track provides the parity bit which accompanies each of the character codes. The eighth track provides timing information.

4-59. The optical outputs of the eight tracks are sensed by a bank of eight photo-diodes to produce electrical readouts. The output of the timing track photo-diode is delayed and prevents the readout of the character code photo-diodes while the information is changing. The character information corresponding to each readout of the code wheel is shown in Figure 10 of Section III.

4-60. Hammer Drivers and Receivers.

4-61. Each hammer driver receiver circuit receives a unique combination of three input lines from the hammer address decoder. These are as follows:

(a) One of two zone lines.

(b) One of nine card select lines.

(c) One of eight circuit select lines.

4-62. The zone select lines correspond to the state of address register bit AR6. If this bit is a ZERO, the 68 hammer driver receivers in zone 1 are selected.

4-63. Eight hammer driver receivers are contained on a card. Lines which enable one card enable eight hammer driver receivers; lines which enable two cards enable 16 hammer driver receivers. Each of these nine card select lines corresponds to a unique condition of the states of address register bits $AR2^3$, $AR2^4$, $AR2^5$, and $AR2^7$.

4-64. The eight circuit select lines each correspond to a particular condition of the states of the three least significant address register bits, and also contain the compare circuitry Decode Strobe output. Thus, one zone select line is always enabled, one card select line is always enabled, and one circuit select line is enabled only if a Decode Strobe is received from the compare logic. The hammers corresponding to these signals are shown in Figure 4-10.

4-65. Hammer Operation.

4-66. Each hammer, when energized, prints a character in its corresponding character position. The particular character printed is dependent on the print drum position when the hammer is energized.

4-67. As shown in Figure 4-11, a hammer assembly consists of the hammer, a flag which contains a flat-wire coil, and two springs which serve as the flag assembly mechanical supports and also conduct the coil current.

4-68. No current normally flows in the coil, which is positioned in the permanent magnetic field. An enabling input from a hammer driver receiver, at the time that a set pulse is applied to all hammer drivers, drives a current through the flag coil. This

FIGURE 4-10. HAMMER ADDRESSES.

ZONE	CARD SELECT	CIRCUIT SELECT 1	2	3	4	5	6	7	8
1	1 & 9	1	2	3	4	5	6	7	8
	2 & 10	9	10	11	12	13	14	15	16
	3 & 11	17	18	19	20	21	22	23	24
	4 & 12	25	26	27	28	29	30	31	32
	5 & 13	33	34	35	36	37	38	39	40
	6 & 14	41	42	43	44	45	46	47	48
	7 & 15	49	50	51	52	53	54	55	56
	8 & 16	57	58	59	60	61	62	63	64
2	1 & 9	65	66	67	68	69	70	71	72
	2 & 10	73	74	75	76	77	78	79	80
	3 & 11	81	82	83	84	85	86	87	88
	4 & 12	89	90	91	92	93	94	95	96
	5 & 13	97	98	99	100	101	102	103	104
	6 & 14	105	106	107	108	109	110	111	112
	7 & 15	113	114	115	116	117	118	119	120
	8 & 16	121	122	123	124	125	126	127	128
1	17	129	130	131	132				

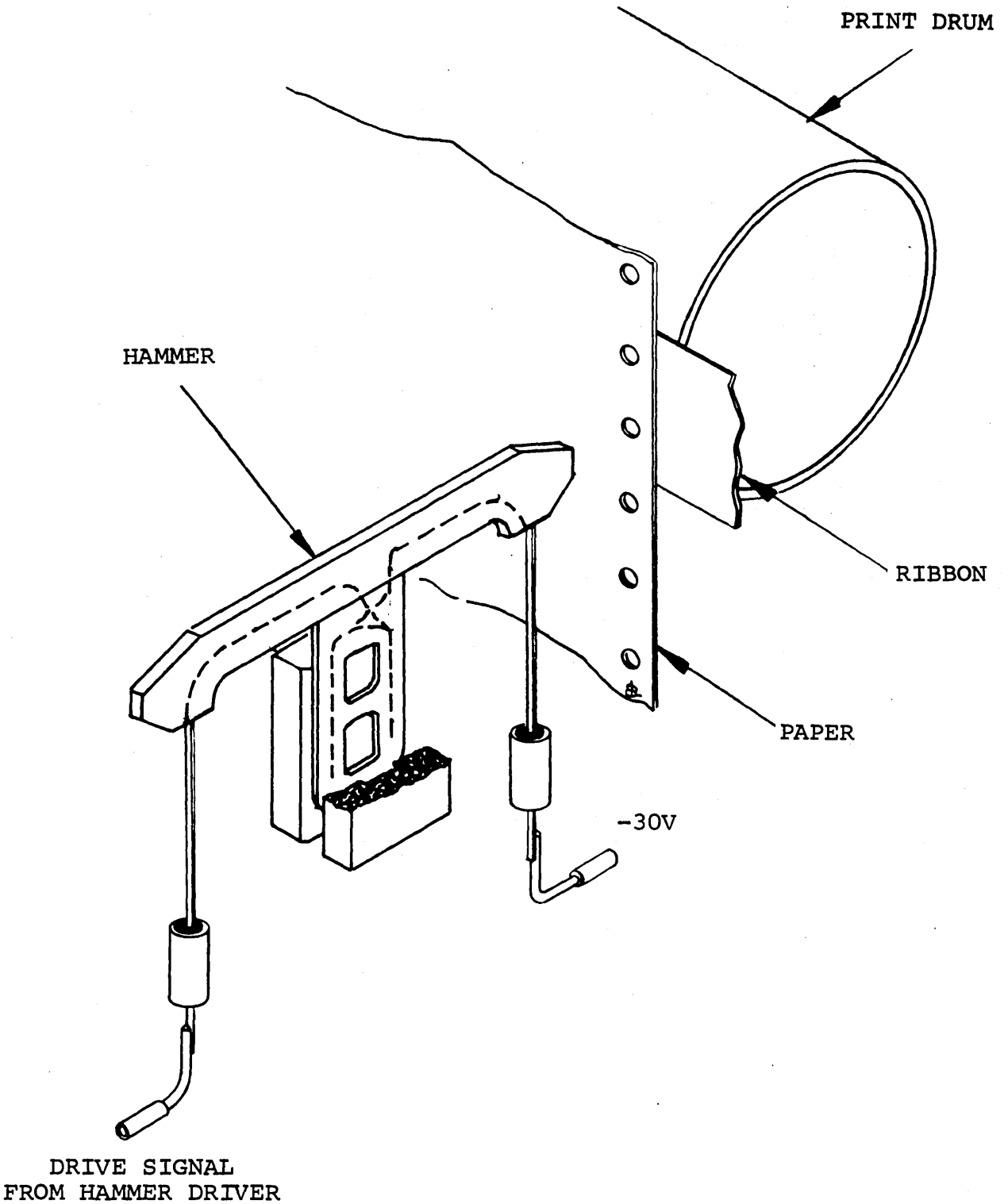


Figure 4-11. Hammer Operation Diagram

current, operating in the magnetic field, drives the hammer assembly toward the drum. A reset pulse applied to all hammer drivers terminates the coil current; a diode in the hammer driver circuit provides a path for the induced current when the coil is open-circuited. The time between the set and reset pulses is 1.5 usec. (Current is terminated before the hammer strikes the paper).

4-69. Paper Control Circuitry

4-70. Paper Stepping Motor. The paper is advanced by a stepping motor which has 200 discrete positions per revolution. Due to the paper drive mechanism, four steps correspond to the 1/6-inch printer line spacing.

4-71. The motor torque is controlled by the application of current to its four field coils. Currents are supplied to these fields by the 2-stage paper control register (PCR) consisting of flip-flops PCR A and PCR B. Two of the four coils are thus energized at any one time. Stepping of the motor results from sequencing of the PCR flip-flops.

4-72. The position of the two-track code wheel attached to the stepping motor shaft is detected by two photo-diodes. The code wheel is opaqued except for two tracks. Each track contains 100 clear areas and is otherwise opaque. The clear areas on the two tracks are displaced from one another by 1/200 of a revolution. The paper drive requires 1/50 of a motor revolution for each 1/6-inch paper line space. Since the motor in its stopped position is with an inside track detected, each alternate inside track represents the motor stopped positions.

4-73. Figure 4-12 shows the paper stepping motor logic. With no paper being driver, flip-flops PCR A and PCR B are reset and the inside track photo-diode amplifier provides a true output which is held disabled by a count other than two in the PDR register. As shown in Figure 4-13, four unique position-torque curves exist for the motor. Each curve corresponds to one of the four conditions of the A and B flip-flop states. Since the A and B true and false outputs each energize a particular motor field, each of the four conditions of the states of these two flip-flops produces a particular position-torque curve.

4-74. Position 1 in Figure 4-13 indicates the position of the motor with no paper being driven. The A and B flip-flops are both reset, and the $\overline{A}\cdot\overline{B}$ curve applies. Any tendency of the motor to be moved in the CCW (counter-clockwise) direction produces an opposing CW (clockwise) torque. A CCW torque will be generated to resist any tendency to move the motor in a CW direction.

4-75. Thus, with the A and B flip-flops reset and the PDR (paper delay register) decoded output not equal to two, the inside track true output is disabled. A PDR=2 output from the PDR decoder enables the inside track signal, which sets PCR A. As shown in Figure 4-13, the motor now operates on the $\overline{A}\cdot\overline{B}$ position-torque curve. With the motor in this position, a torque is generated which drives the motor in the CW direction.

4-76. The torque decreases as the motor position changes. As the motor approaches a displacement of 1/200 of a revolution (1/4 of a line space), the outside track photo-diode generates a true output which is enabled and sets PCR B.

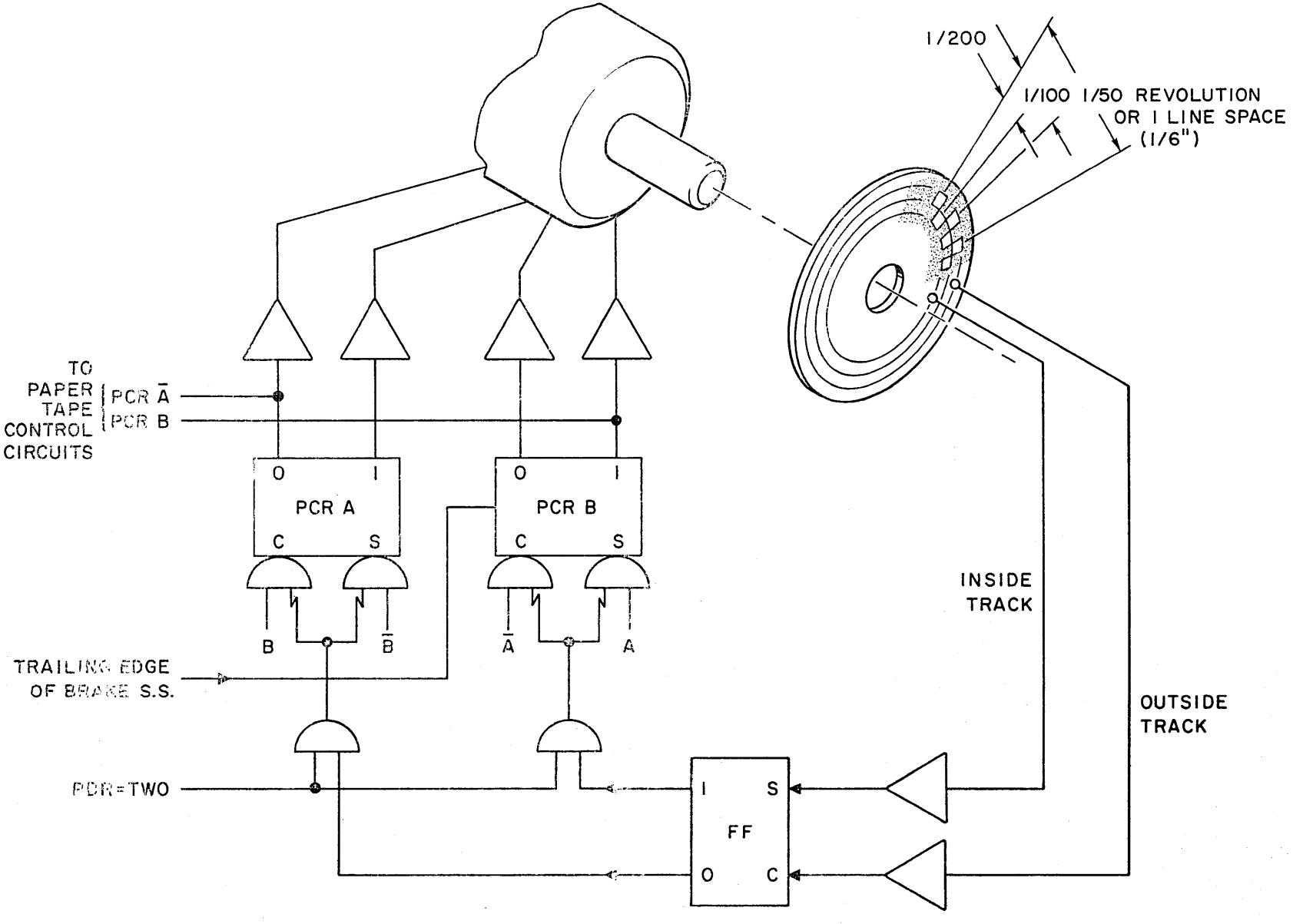


Figure 4-12. Stepping Motor Logic

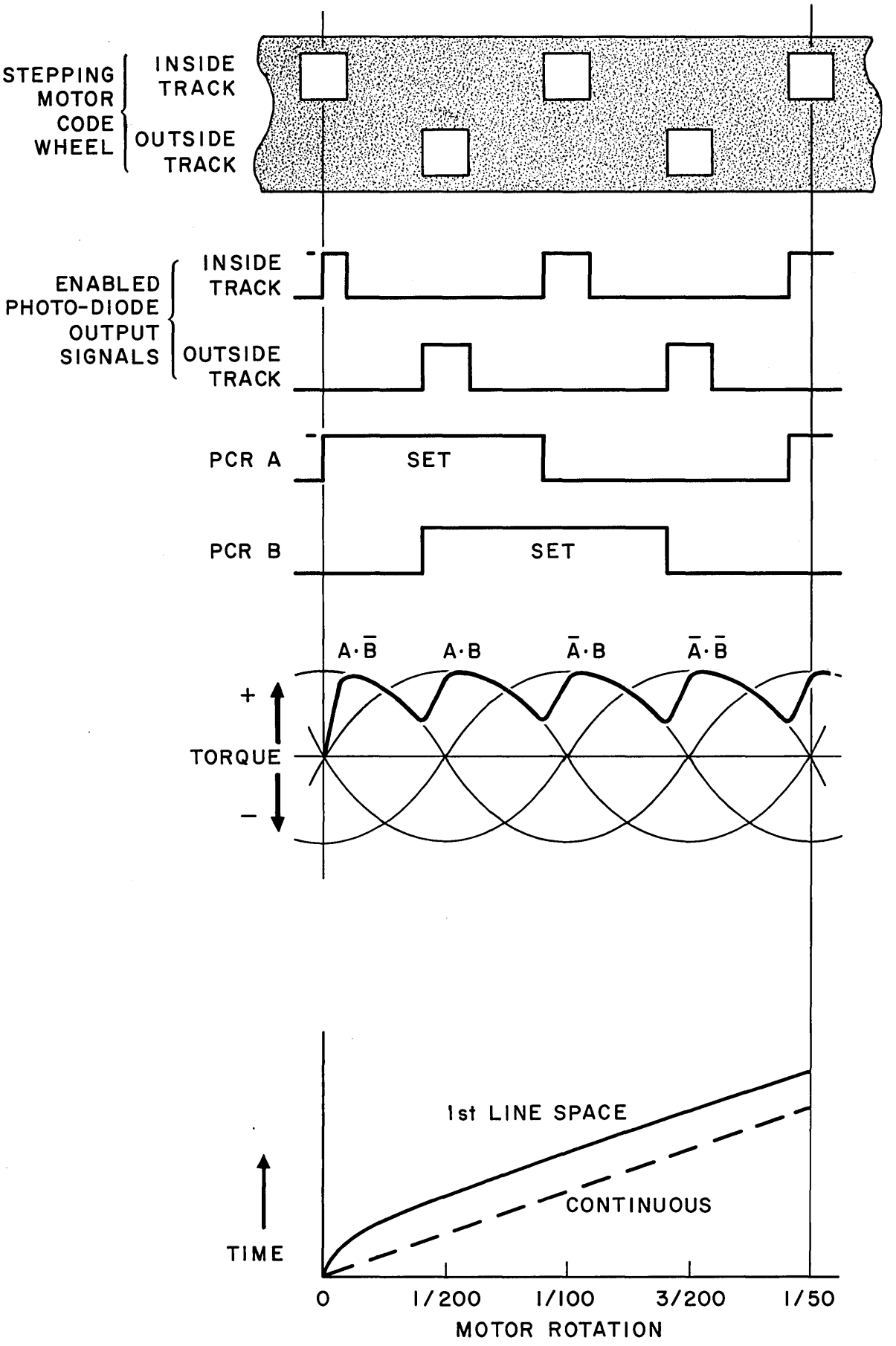


Figure 4-13. Stepping Motor Operation

4-77. The motor operates on the A•B position-torque curve for 1/200th of a revolution. With A and B set, the next inside track signal clears A. The paper drive control logic is interrogated when A is cleared and B is set. When spacing is not to be terminated, motor operation continues on the $\overline{A}$•B curve until the outside track clears B. The motor approaches a constant speed as it is continually pulsed by the switching of A and B in the A•$\overline{B}$, $\overline{A}$•B, and $\overline{A}$•$\overline{B}$ sequence.

4-78. Motor braking operation is shown in Figure 4-14. At approximately 1/2 line space the $\overline{A}$ and B signals are applied to the paper drive logic circuits and, when motor spacing is to be terminated, the brake single-shot is triggered.

4-79. As shown by the dashed lines in Figure 4-12, continuation of normal motor operation until the $\overline{A}$•$\overline{B}$ count is reached results in oscillation about the full line space position due to the inertia of the motor and paper drive mechanism. Thus, when the motor is to be stopped, the brake single-shot is triggered. This signal steps the PDR counter and thus prevents the photo-diode output signals from driving the PCR flip-flops. The motor operates on the solid line as shown. With no switching at the 3/4-line space position, the motor inertia carries it into the negative-torque region. The inertia of the motor and paper drive is opposed by the negative torque. The trailing edge of the BRAKE SS signal then clears PCR B, and the motor operates on the $\overline{A}$•$\overline{B}$ curve. The nominal setting of the brake single-shot is nine ms. With correct adjustment of this circuit for the optimum transition point from the $\overline{A}$•B to the $\overline{A}$•$\overline{B}$

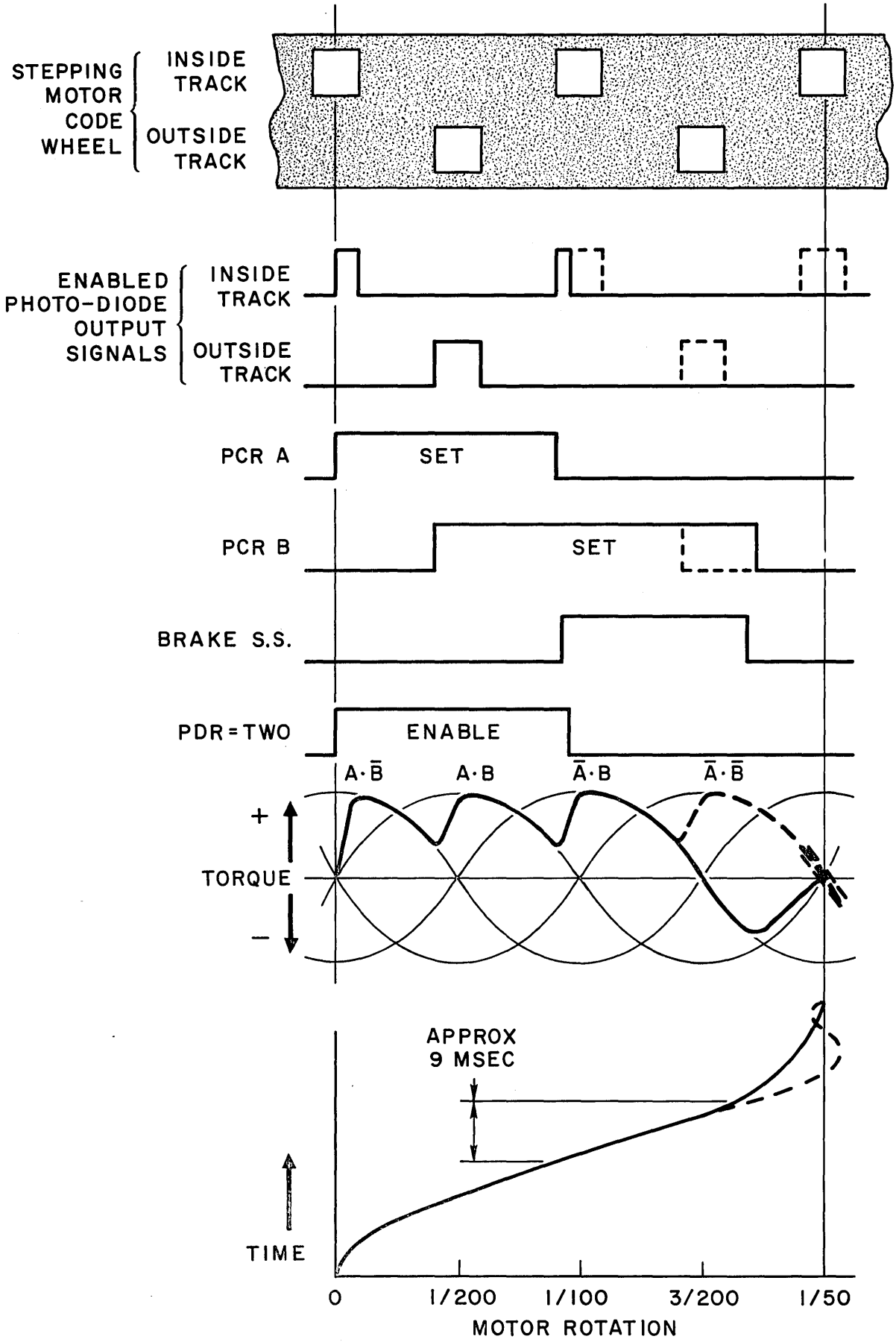


Figure 4-14. Stepping Motor Braking

operation, motor rotation and corresponding paper movement from a single space will be terminated with the smooth motion shown by the solid line. Due to the higher speed and greater kinetic energy of the motor and paper drive mechanism following the first line space, continuous operation is terminated with an operation between the two time-motion curves shown.

4-80. Paper Delay Register. (See Figure 4-15). The paper delay register (PDR) enables the paper control register (PCR) to drive the paper stepping motor, and generates a time delay during the time that the paper drive is stopping.

4-81. The paper delay register consists of four flip-flops which count in either of two sequences. The four stages are normally reset. A count from this condition can be initiated only by a TOP OF FORM instruction or by a PAPER INSTRUCTION (paper tape or paper count operation). The first pulse drives the register to a count of one. With the register at the count of one, the 384-cps PC (Pure Character) Strobe signal from the print drum code wheel timing track is enabled and drives the register to a count of two. The PC Strobe gate is now disabled.

4-82. As described under paper stepping operation, a count of two from the PDR decoder initiates paper stepping motor operation. At the $\overline{A} \cdot B$ step of the PCR register, the paper drive control logic controls paper motion as follows:

(a) For a paper count or a tape advance of two or more continuous lines: enable Set Level PDR 2^3.

(b) To terminate paper advance: trigger brake single-shot.

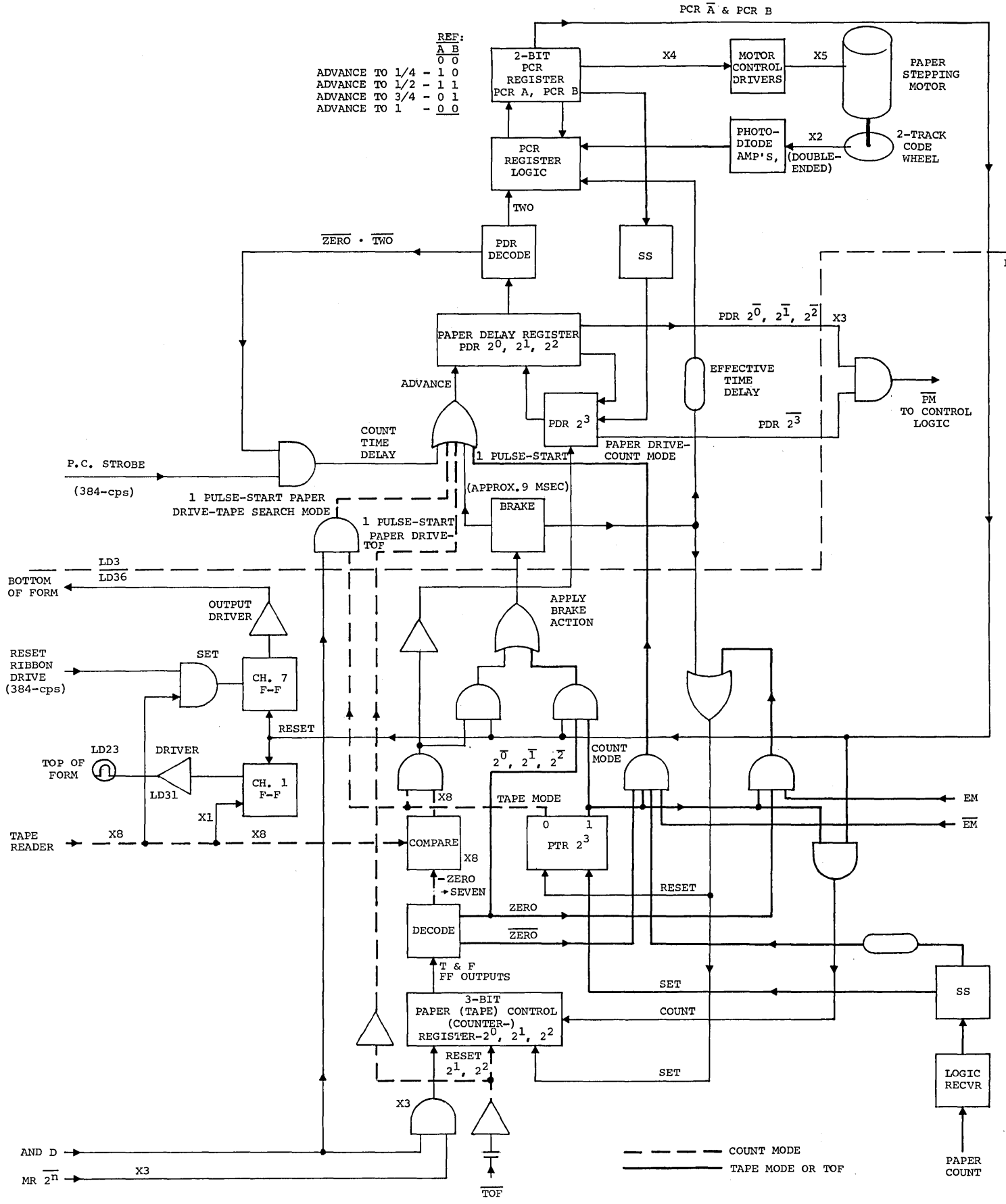


Figure 4-15. Paper Drive, Simplified Logic Diagram

4-83. When the paper stepping motor is to be stopped, the brake single-shot is triggered, which drives the PDR register to the count of three. The PC Strobe pulses are again enabled, until either four or eight of these pulses return the PDR register to the count of zero. When the four bits of the PDR are reset, the $\overline{PM}$ ($\overline{PAPER\ MOVING}$) signal is generated by the paper drive logic. This time delay is as follows:

(a) Advance paper one line space with paper tape control: with the brake single-shot triggered on the first line space, PTR 2^3 is not set. The time delay until a true $\overline{PM}$ signal is generated is approximately 10 to 13 ms from the time that the brake single-shot is triggered.

(b) Paper count or advance paper two or more line spaces with a continuous operation: the PDR 2^3 flip-flop is set, which initially inhibits the PDR 2^2 reset. This requires four additional PC Strobe pulses. The time delay to allow for the additional paper drive settling time required is thus increased by four PC Strobe pul pulses. From the Brake single-shot pulse, a total delay of approximately 20-23 ms is generated before the $\overline{PM}$ signal is true.

4-84. Paper Tape Control. (See Figures 4-15 and 4-16). The functions and normal states of the paper tape control flip-flops are as follows:

(a) PTR 2^0, PTR 2^1, and PTR 2^2: these flip-flops comprise the paper tape control counter-register, and are initially set.

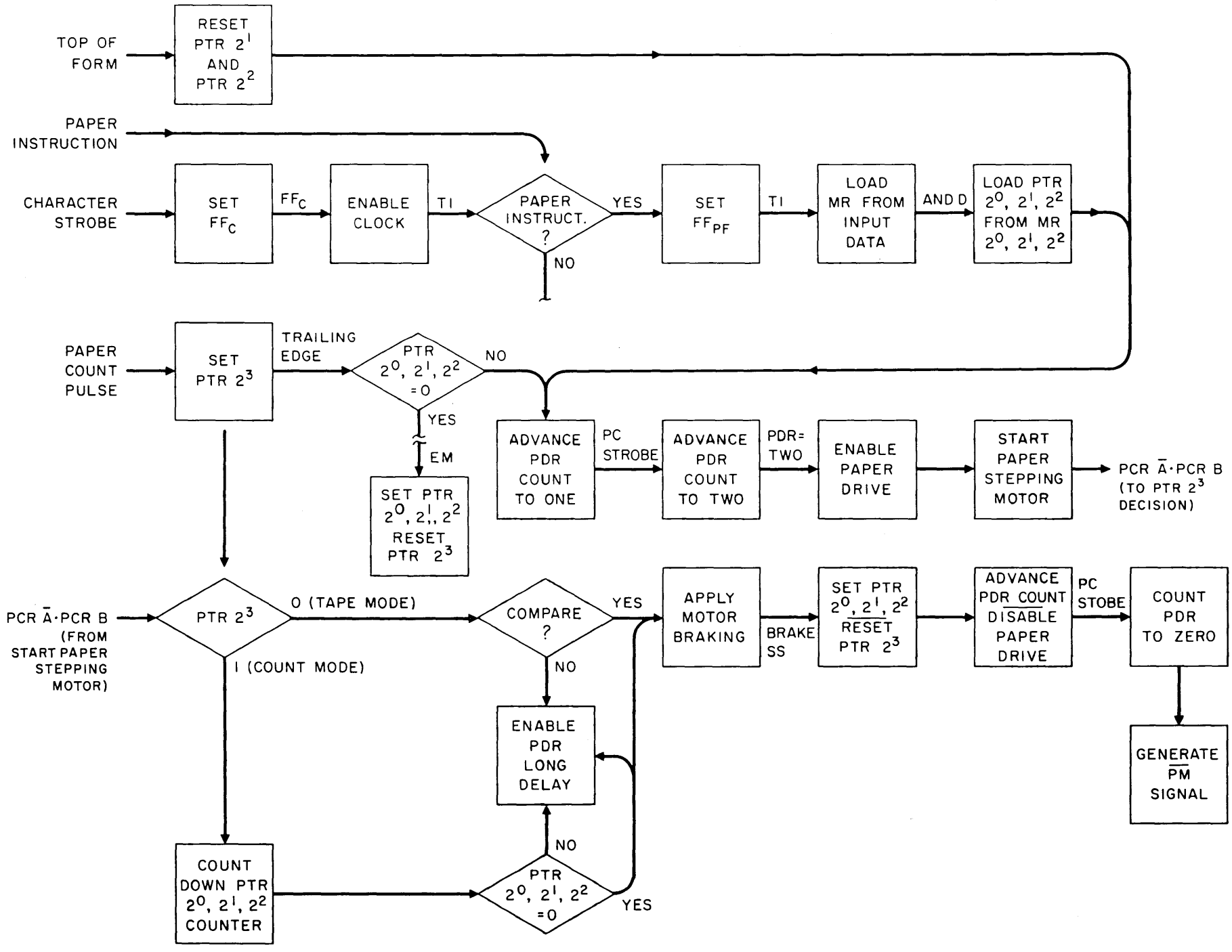


Figure 4-16. Paper Drive, Simplified Flow Chart

These flip-flops operate as a 3-bit data-storage register with PTR 2^3 reset, and operate as a 3-bit count-down counter when PTR 2^3 is set.

(b) PTR 2^3: this flip-flop is reset for paper tape operations, and is set for paper count operations.

(c) Ch.1: this flip-flop is set when a hole is sensed in channel 1 in the tape when the paper stepping motor is operating. It is reset by a paper advance with no hole in channel 1.

(d) Ch.7: this flip-flop is set whenever a hole is sensed in channel 7 in the tape.

4-85. Top of Form Sequence. This sequence is initiated when the TOP OF FORM switch on the printer control panel is depressed or by a command from the computer (applied to the Input Data lines). The paper and tape are advanced one or more line spaces until a hole is sensed in channel 1 of the paper tape. This sequence operates as follows:

(a) The TOP OF FORM switch, when depressed, holds a corresponding flip-flop set. The flip-flop false output applies a clear pulse to PTR 2^1 and PTR 2^2, a reset pulse to PTR 2^3, and an advance pulse to the PDR register.

(b) The PTR register now holds a count of one and enables a corresponding compare gate. The channel 1 output from the tape reader is applied to this gate.

(c) The advance pulse to the PDR register initiates paper stepping motor drive as preciously described. At each

1/2 line space (1/100th of a motor revolution) the PCR $\overline{A}$·PCR B output from the stepping motor logic interrogates the paper control logic.

(d) The reset PTR 2^3 (tape/count) flip-flop enables the comparator output. When no comparison is detected, a true Set Level PDR 2^3 signal provides for the long braking delay. No brake signal is generated.

(e) When a hole is detected in channel 1, the tape reader channel 1 output sets the Ch.1 flip-flop, which lights the indicator lamps in the TOP OF FORM indicating switch. The tape control logic comparator detects the comparison between the PDR register contents of one and the hole in channel 1 of the tape. The PCR $\overline{A}$·PCR B signal generates a Set Brake single-shot signal. The paper is stopped. The Brake single-shot pulse sets the PTR 2^0, PTR 2^1, and PTR 2^2 flip-flops.

4-86. Paper Tape Sequence. A paper tape sequence is similar to a top of form sequence, with the exception that the detected tape channel is variable, and is defined by information applied to the Input Data lines.

4-87. A Character Strobe applied with a true Paper Instruction signal initiates the following actions:

(a) The Character Strobe pulse sets flip-flop FF_C.

(b) Set flip-flop FF_C enables the 500-kc clock.

(c) With FF_R set, as required to load data or instructions, the T1 timing pulse strobes the Paper Instruction input

line. With a true signal on this line, flip-flop FF_{PF} (the paper feed flip-flop) is set.

(d) At this time T1 also strobes the ID (input data) lines. The three lines used for the character information least significant three bits transmit tape hole position. The memory register is loaded with the input information. (All memory register input gates are strobed; the other three data bits and the parity bits are loaded but not used.)

(e) Set flip-flops FF_R and FF_{PF} generate the AND D signal. This signal transfers the three least significant memory register bits to the paper control logic by resetting PTR register stages corresponding to memory register stages which hold ZEROs.

(f) With PTR 2^3 reset (indicating a paper tape search operation), an advance pulse is applied to the reset PDR register. The paper stepping motor is started.

(g) The three information bits in the PTR register enable one of the eight comparator gates. The set PTR 2^3 flip-flop enables the comparator output. As in the top of form sequence, paper is advanced until a comparison is detected between the PTR register contents (as applied on the input data lines) and a hole in the tape. At this time, the paper stepping motor braking action is applied.

4-88. Paper Count Sequence. In the paper count sequence, paper is advanced a number of lines equal to information transmitted to the printer on the input data lines. If the count of zero is applied, paper drive motion is inhibited. The sequence is as follows:

(a) The Character Strobe sets flip-flop FF_C.

(b) Set flip-flop FF_C enables the 500-kc clock.

(c) With FF_R set, as required to load data or instructions, the T1 timing pulse strobes the Paper Instruction input line. With a true signal on this line, flip-flop FF_{PF} (the paper feed flip-flop) is set.

(d) At this time T1 also strobes the ID (input data) lines. The three lines used for the character information least significant three bits transmit the number of lines to be counted. The memory register is loaded with the input information. (All memory register input gates are strobed; the other three data bits and the parity bits are loaded but not used.

(e) Set flip-flops FF_R and FF_{PF} generate the AND D signal. This signal transfers the three least significant memory register bits to the paper control logic by resetting PTR register stages corresponding to MR stages which hold ZEROs.

(f) A Paper Count signal leading edge sets tape/count flip-flop PTR 2^3. This enables the count mode in which the comparator is disabled, the PTR counter-register operates in its count-down mode, and the PTR contents are interrogated for zero.

(g) The trailing edge of the Paper Count pulse interrogates the PTR counter contents. If the three information stages are reset at this time, indicating a count of zero paper line spaces, the Paper Count pulse is inhibited from advancing the PDR register. No paper motion occurs. The EM (end message) signal following the loading of the next line returns the four PTR flip-flops to their initial states, and disables the Advance PDR Count logic while the flip-flops are being switched.

(h) With a count of one through seven in the PTR counter, an advance pulse is applied to the PDR register at this time. The paper stepping motor is started.

(i) With tape/count flip-flop PTR 2^3 set (in the count state) the 1/2-line space PCR signals count the PTR counter down by one for each line space and interrogate the result. (With the comparator disabled by the set PTR 2^3, the long-delay flip-flop PDR 2^3 in the paper delay register is set.) When the interrogate signals count the PTR counter to zero, the brake single-shot is triggered.

(j) The Brake single-shot pulse terminates the paper feed and returns the PTR register stages and tape/count flip-flop PTR 2^3 to their initial states.

4-89. Bottom of Form. The tape reader channel 7 output is interrogated by the 384-cps Reset Ribbon Drive pulses derived from the print drum code wheel timing track. A hole in channel 7 of the

tape enables set pulses to the CH.7 flip-flop. This flip-flop is reset when the PCR A flip-flop in the stepping motor logic is reset (at approximately 1/2 line space). The inverted output signal is applied through an output driver to the computer. Thus, this signal is false when a channel 7 tape hole is sensed.

4-90. Ribbon Drive and Control.

4-91. (See logic diagrams 3 and 25; and Figure 4-17). The two ribbon drive motors maintain ribbon tension, and drive the ribbon in accordance with signals from the ribbon drive control circuitry. This circuitry moves the ribbon during printing or paper drive operations and reverses the direction of ribbon motion at each end of the reel.

4-92. When power is initially applied to the ribbon drive circuitry, relay K9 or K10 will be energized. The PDR register will be cleared by the clear signal and the ribbon drive flip-flop will be cleared. Ribbon drive relay K11 is de-energized and applies current to both ribbon drive motors to maintain ribbon tension.

4-93. Assume relay K9 energized. Ribbon motion caused by setting of the ribbon drive flip-flop will then be toward the left. Detection of the rivet at the end of the ribbon closes the right-hand switch, energizes relay K10, open-circuits the K9 relay coil, and completes a circuit from relay K11 to the right drive motor. Subsequent ribbon motion is to the right until the left-hand switch detects the rivet. Relay K9 will then be energized and relay K10 will be de-energized. Thus, ribbon direction is automatically reversed whenever the end of the ribbon is reached.

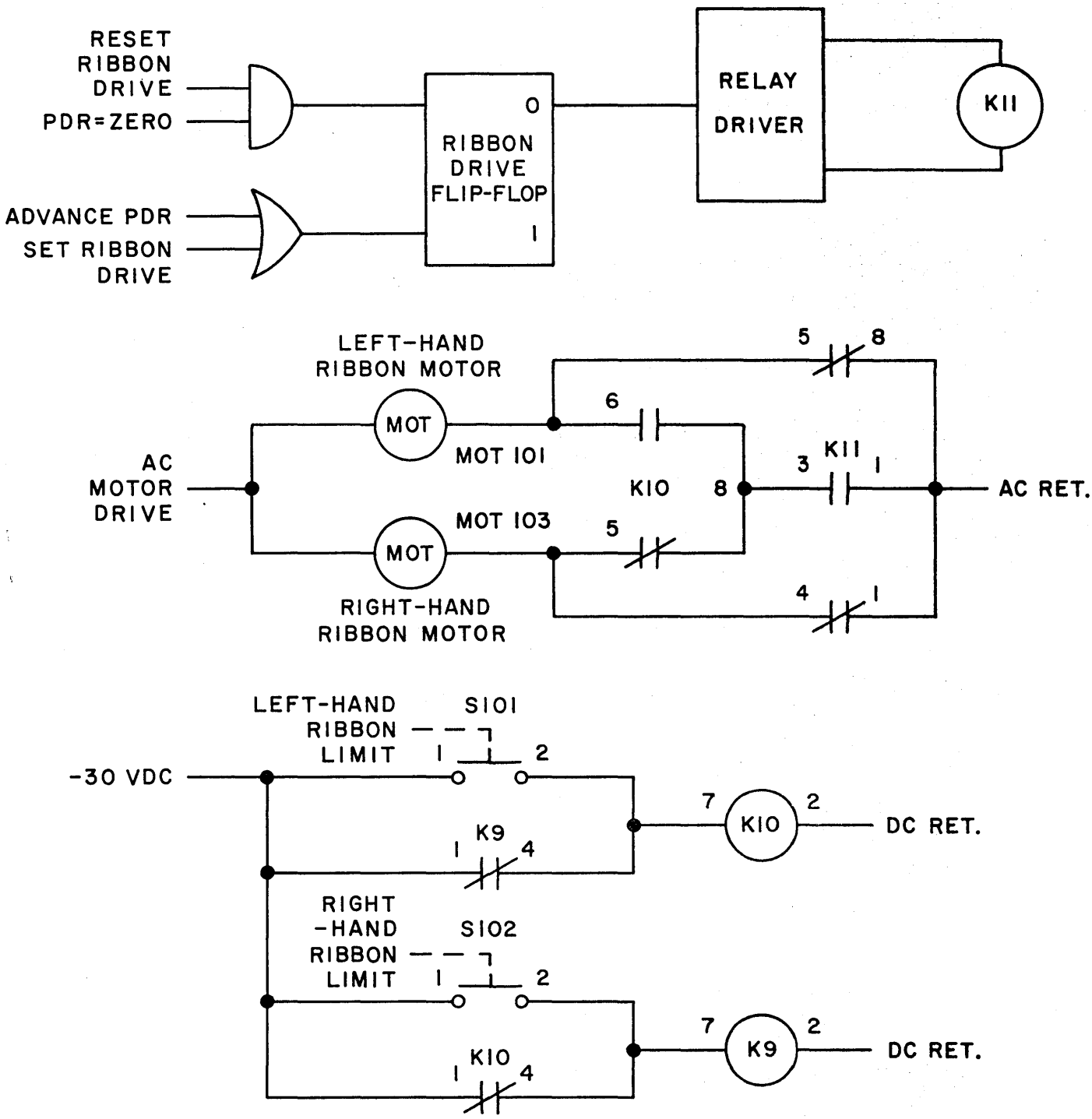


Figure 4-17. Ribbon Drive Circuitry

4-94. Ribbon motion is initiated by the ribbon drive flip-flop which is normally held reset by Reset Ribbon Drive pulses derived from the code wheel timing track. These pulses are enabled by the PDR counter when the first three stages are reset.

4-95. Application of a count pulse to the PDR counter sets the ribbon drive flip-flop. This flip-flop, through a driver, energizes relay K11, which applies current to one motor as determined by relay K10. The ribbon drive flip-flop is also set by a signal indicating that printing will be done by the next character on the print wheel. Ribbon motion continues until the first enabled Reset Ribbon Drive signal resets the ribbon drive flip-flop.

4-96. The ribbon is held in tension whenever printer power is on. Ribbon motion is continuous during printer operation. When the printer is inactive (not being operated by printing or paper-spacing commands), ribbon motion is stopped.

4-97. Timing Distributor.

4-98. (See logic diagrams 22 and 31). The timing distributor generates the timing signals necessary to sequence the core buffer scan cycles, and to step the printer control logic.

4-99. The clear pulse, applied after turn-on from the power supply sequencing circuitry, clears flip-flops FF_D and FF_E. The clear signal also clears FF_V and FF_C, which holds the 500-kc clock disabled.

4-100. Setting of FF_V, with FF_R cleared, or setting of FF_C, enables the adjustable 500-kc clock, which generates 0.5-usec pulses. The first output pulse sets FF_D; FF_E remains cleared. This pulse

is also applied, through a 0.5-usec delay line, to four gates. Each of these gates receives a decoded output of flip-flops FF_D and FF_E. With FF_D set and FF_E cleared, timing pulse T1 is generated.

4-101. The next clock pulse sets FF_E; FF_D remains set. The delayed clock pulse generates timing pulse T2. Similarly, the next clock pulse clears FF_D; the delayed clock pulse generates timing pulse T3. The next clock pulse clears FF_E and generates T4.

4-102. During the 2-usec interval in which FF_D is set and FF_E is cleared (reset), a read current timing signal is applied to the core buffer X and Y read current drivers. Similarly, during the time that FF_D is reset and FF_E is set, a write current timing signal is applied to the core buffer X and Y write current drivers.

4-103. Timing pulse T2 is applied to the core buffer to initiate inhibit current driver operation. The flip-flop FF_E true output is applied to the inhibit current logic. When flip-flop FF_E is reset, the positive-going true output is the end inhibit timing signal.

4-104. Due to flip-flops FF_V, FF_R, and FF_C, which enable and disable the clock, the clock can only be disabled by actions resulting from a T4 timing pulse. Thus, whenever the clock is enabled, an integral number of four timing pulses (T1, T2, T3, and T4) results.

4-105. Output Signal Logic (see logic diagram 38).

4-106. The output signals control the sequencing of character information and Paper Instruction transfers to the printer.

4-107. Figure 4-18, a flow chart, shows the Send Data and associated signal generation. The Ready relay in the power supply control circuitry must be energized for all printer operations. When this relay is not energized, the Send Data, Printer Ready signal to the computer, and PRINTER READY indicator on the printer control panel are all held disabled. With paper detected by No Paper switch S31, and READY switch S90 closed, the PRINTER READY indicator is turned on. With these conditions, and with the HALT/RUN switch on the printer maintenance panel in the RUN position, a true Printer Ready signal is applied to the computer.

4-108. The heavy lines in Figure 4-18 indicate the normal generation of the Send Data signal. Following the clear sequence, flip-flop FF_R is set and flip-flop FF_C is reset. The Send Data signal is a ONE. Flip-flop FF_C is set at the start of each character transfer to the printer by the Character Strobe. Flip-flop FF_C is reset, following the loading of the character, by timing pulse T4. Thus, the Send Data signal is disabled during each 8-usec character-loading cycle.

4-109. Flip-flop FF_R is cleared at the end of the loading of all characters of a line by the End Message signal. It is set when all characters in the core buffer have been printed (no ONE sentinel bits remain in the core buffer). Thus, the reset flip-flop FF_R disables the Send Data signal when a line is being printed. Following the loading of a Paper Instruction, flip-flop FF_R is not set until paper motion has been terminated. Thus, FF_R also disables the Send Data line during the execution of a paper feed operation.

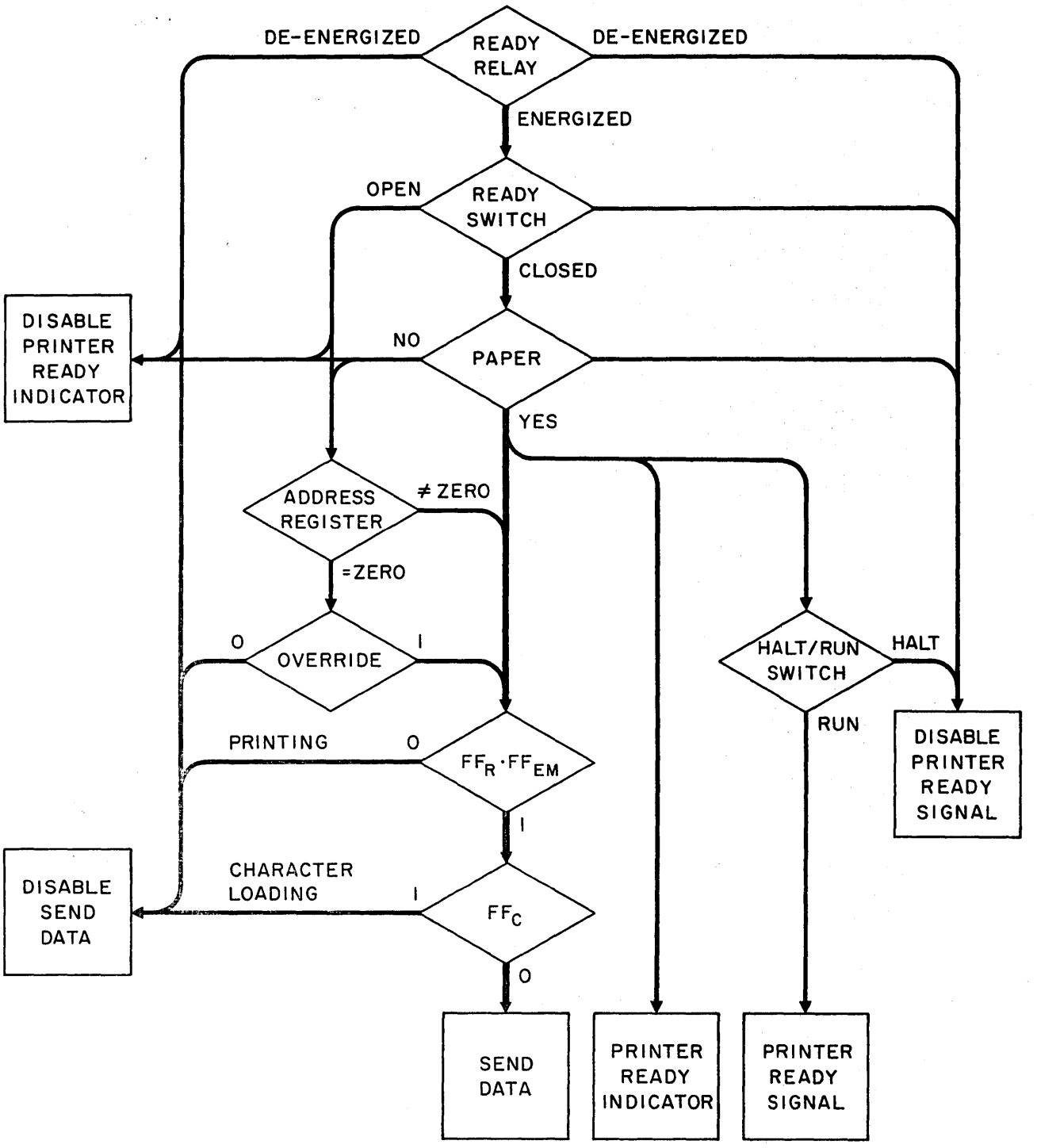


Figure 4-18. Output Signals Flow Chart

4-110. READY switch S90 on the printer control panel is used to switch the printer between its operating and standby conditions. With this switch in its READY position and paper detected by the No Paper switch S31, the indicator lamps of the READY switch are lighted.

4-111. Printer operation is dependent on the conditions necessary to maintain the Ready relay (K8) energized, and is not dependent on the READY switch (S90) position. The No Paper switch detects the absence of paper when sufficient paper exists to print several lines. To prevent disabling printer operation when the READY switch is operated during printer operation, or when the paper switch operates during printer operation, the address register stage outputs are decoded. If the address register is not cleared, indicating that a complete line of character information has not been transmitted, this decoded signal permits enabling of the Send Data signal to permit completion of the line being processed.

4-112. With the printer ready to load a new line (address register cleared, FF_R set, and FF_C reset) an Override signal from the computer enables the Send Data signal even though the No Paper switch indicator no paper and/or the READY switch is in the standby position.

4-113. Control Logic. (See logic diagram 32).

4-114. The control logic consists of eight flip-flops and their associated gates which, in conjunction with timing pulses and input signals, control various printer operations. These flip-flops are defined in the following paragraphs.

4-115. Flip-flop FF_R is the Ready for Loading flip-flop which differentiates between the information-loading and compare-and-print operating modes.

4-116. Paper feed flip-flop FF_{PF} is set during loading of Paper Instruction information.

4-117. FF_C, the Character Strobe flip-flop, is set by each Character Strobe signal received from the computer with the transmission of print data or a Paper Instruction. With FF_{PF}, FF_C generates the AND D signal during PAPER INSTRUCTION loading.

4-118. Flip-flop FF_{EM} is set by the Clear signal following printer turn-on. During operation, it is reset by the leading edge of the End Message signal from the computer, and is set when FF_R is set by the FF_R positive-going false output. The true outputs of the FF_R and FF_{EM} flip-flops are ANDed together. This signal, applied to the output signal logic which generates the Send Data signal, inhibits the Send Data signal when an End Message signal has been received.

4-119. Flip-flop FF_V synchronizes the character scan cycles with the print drum operation (determines that the character-drum code is pure, i.e., Virgin). As shown on Figure 4-3, the Reset Ribbon Drive pulse occurs 0.2 ms following the timing track output signal. Thus, setting of FF_V by the Reset Ribbon Drive pulse ensures that previous character information has been cleared from the hammer driver receivers, and that sufficient time exists for a complete character scan before the hammer currents are turned on.

4-120. Parity flip-flop FF_P, when set, indicates that a parity error has been detected in the character information read out from the core buffer.

4-121. Sentinel flip-flop FF_S is set during Character Scan cycles to indicate detection of a sentinel bit. Thus, a set FF_S flip-flop at the end of a Character Scan indicates unprocessed character information exists in the core buffer.

4-122. FF_{SNTL2} (see logic diagram 34) is set during Character Scan cycles when a sentinel bit is read from the core buffer, and applies a signal to the compare logic to indicate that the information being compared has not been previously processed. (FF_{SNTL}, which is a part of the memory register, is cleared at this time when a comparison has been detected.)

4-123. Printer Clear

4-124. Clearing of the printer following turn-on is initiated by a Clear pulse from the power supply sequencing circuitry. The resulting state of the printer control flip-flops, in conjunction with the printer logic, prepares the printer for operation.

4-125. The Clear pulse sets up various flip-flops as shown in Figure 4-19. With flip-flop FF_R reset and a $\overline{PM}$ signal from the reset PDR (paper drive register) flip-flops, a Reset Ribbon Drive pulse sets FF_V. The 500-kc clock is enabled. Since FF_{PF} and FF_V are cleared by the Clear pulse, each T4 signal advances the address register by one.

4-126. When the count of 131 (the 132nd core buffer storage location) is reached, the 132 signal, in conjunction with timing pulse T4, does the following:

FIGURE 4-19. PRINTER CLEAR

LOGIC	FLIP-FLOPS	CLEAR PULSE	FIRST T4	CLEAR SEQUENCE
PAPER COUNT REGISTER	PCR A PCR B	0 0		
PAPER DRIVE REGISTER	$PDR2^0$ $PDR2^1$ $PDR2^2$ $PDR2^3$	0 0 0 0		
TIMING DISTRIBUTOR	FF_D FF_E	0 0		
CONTROL	FF_R FF_{PF} FF_C FF_{EM} FF_V FF_P FF_S FF_{SNTL2}	0 0 0 1 0 0 0	0	1
MEMORY REGISTER	FF_{SNTL} $MR2^0$ thru $MR2^6$		0 0	
PAPER TAPE CONTROL	PTR 2^0 - PTR 2^2 PTR 2^3 CH.1 CH.7	0 0 0		= BOF
ADDRESS REGISTER	2^0 - 2^7			0
INHIBIT DRIVE	INHIBIT FF	0		

(a) Disables the address register advance pulse logic.

(b) Generates a clear pulse which clears the address register.

(c) Enables the FF_V reset pulse.

(d) With FF_S reset, generates a FF_R set pulse.

NOTE

IF THE PRINTER IS SHUT DOWN BEFORE COMPLETING ITS OPERATION, STORED SENTINELS MAY CAUSE A PRINT-OUT WHEN THE PRINTER IS TURNED ON.

4-127. Set flip-flop FF_R and with FF_R set and FF_V reset, the 500-kc clock is disabled.

4-128. Typical Printer Operation

4-129. (See Figure 4-20). Typical operation of the printer during the loading of a line of characters to be printed as follows:

(a) Information is set up on the ID (input data) lines and a Character Strobe pulse from the computer sets FF_C. Set flip-flop FF_C disables the Send Data line and enables the 500-kc timing distributor clock.

(b) Timing pulse T1 applies a reset pulse to parity flip-flop FF_P.

(c) Timing pulse T1, with FF_R set (indicating loading from the computer), strobes the Input Data and Paper Instruction input lines, sets FF_{SNTL}, and strobes the PAPER FEED input line. The previously cleared memory register now holds the input data (six bits and parity bit) from the computer. With an enabling signal on the Paper Instruction line, flip-flop FF_{PF} is now set

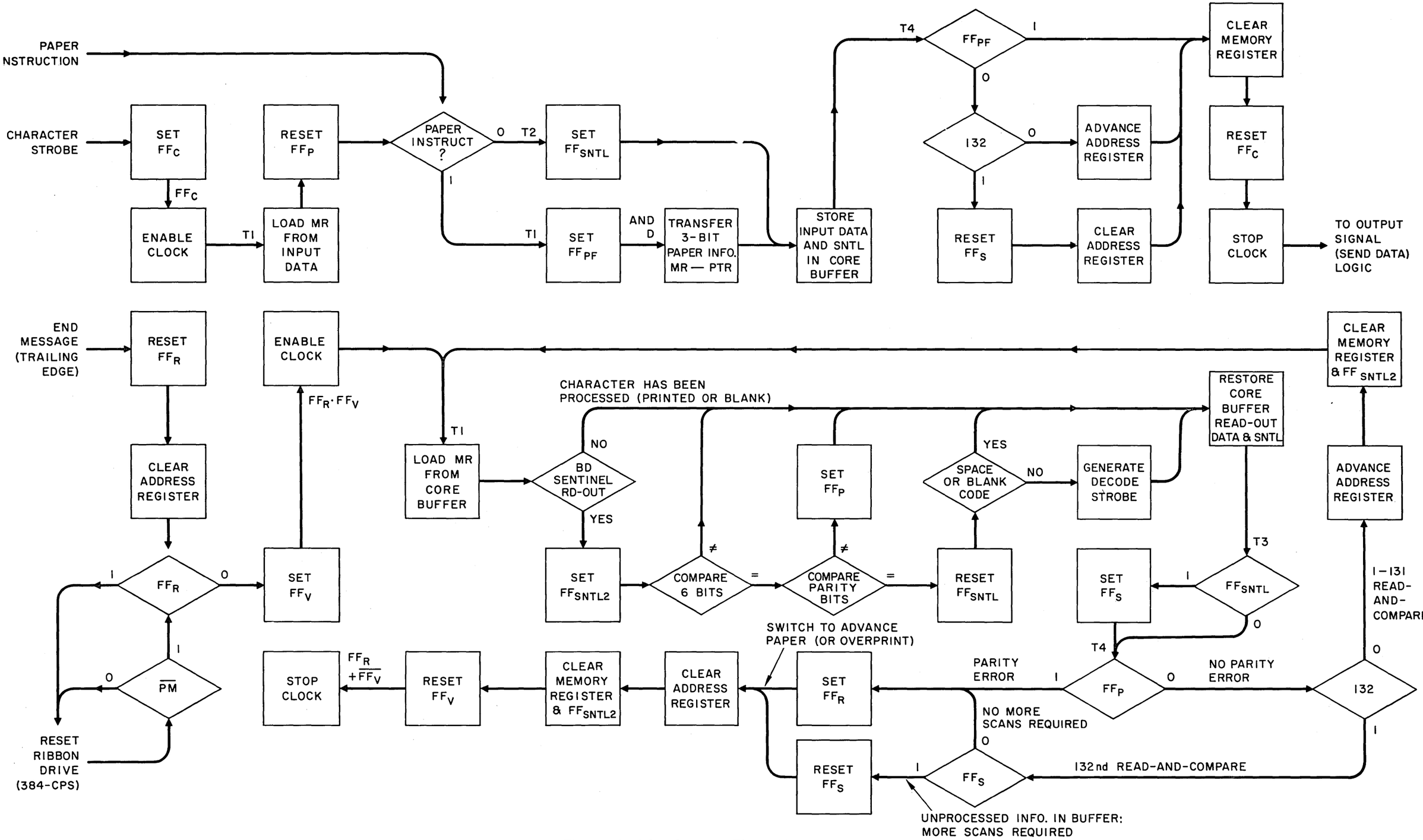


Figure 4-20. System Flow Chart

and the three least significant memory register stages hold paper feed information.

(d) Set flip-flops FF_C and FF_{PF} generate the AND D signal which initiates actions as described in paragraph 4-88.

(e) The core location corresponding to the address register contents is now cleared.

(f) With no enabling Paper Instruction signal FF_R is set and FF_{PF} is reset. Timing pulse T2 sets FF_{SNTL}.

(g) Timing pulse T2 also sets the Inhibit flip-flop which initiates inhibit currents in cores corresponding to reset (ZERO) MR stages.

(h) Timing pulse T3, with FF_{SNTL} set, sets flip-flop FF_S.

(i) Timing pulse T4 clears FF_C, disabling the clock clears the memory register including FF_{SNTL}, and applies a reset pulse to FF_{SNTL2}. When the address register contents are from 0 to 130 inclusive, timing pulse T4 applies an advance pulse to the address register. Reset flip-flop FF_C enables the Send Data signal to the computer. The above cycle is repeated.

(j) When the address register contains a 131 and the T4 pulse is generated, operation is the same as described above with the exception that a Clear pulse is applied to the address register and flip-flop FF_V is cleared.

4-130. A typical read-and-compare cycle is as follows:

(a) With FF_R cleared, timing pulse T1 enables the eight read amplifiers. Where a ONE has been stored in a core

at the selected address, the corresponding MR stage is set. Where a ZERO has been stored, the MR stage remains cleared. The memory register now holds the six data bits, the parity bit, and the sentinel bit.

(b) Timing pulse T2 sets the Inhibit flip-flop and, with FF_R cleared, compares the memory register contents with the six code wheel bits. If these bits are not equal, no action results. If a comparison results, the parity bits are compared.

(c) If the data bits compare, the parity bits are compared. If the code wheel parity bit and memory register parity bit are unequal, Parity flip-flop FF_P is set.

(d) If the two 6-bit words and the parity bits are equal FF_{SNTL} is cleared. If FF_P is cleared and FF_{SNTL2} is set at this time, the memory register is checked to determine whether it contains 12_8 or 60_8. If neither of these codes is present, the Decode Strobe is generated.

(e) As previously described, four or eight hammer driver receivers have, both, enabling zone select and enabling card select signals from the address decoding at this time. The Decode Strobe, in conjunction with decoded address bits AR 2^0, AR 2^1, and AR 2^2, provides an enabling signal to one of these partially-selected hammer driver receivers.

(f) The hammer driver receiver is now set.

(g) Write drive current is now generated. With the inhibit currents flowing in cores corresponding to ZEROs in the memory register, the previously read-out ONEs are restored into the core buffer at their original address.

(h) Timing pulse T3 sets FF_S if FF_{SNTL} is in its set state at this time.

(i) Timing pulse T4 clears memory register stages 0 through 6, FF_{SNTL}, and FF_{SNTL2}.

(j) When the 132nd address (100011) has not been reached, the following actions (steps k and l) occur.

(k) If FF_P is see (a parity error has been detected) FF_V is reset. The clock is disabled.

(l) If FF_{PF} is reset, an advance pulse is applied to the address register.

(m) If the address register reads 131 at this time, the following actions occur:

  (1) If FF_{PF} is cleared, the address register is cleared and returns to all ZEROs.

  (2) If FF_S is not set, flip-flop FF_R is set. If FF_S is not set and the address is 131, then the counter is cleared and ready is set. If FF_S is set and count is 131 and FF_{PF} is not set then the counter is cleared, FF_V is cleared, and the clock stops as a result of FF_V being cleared.

(3) Flip-flop FF_V is cleared. The clock is stopped.

(n) A delayed T4 pulse clears FF_{PF} and, if the address register reads 131 at this time (130 when the T4 pulse was applied), FF_S is cleared.

4-131. The above cycle is thus repeated until an End Message signal is received. All hammer driver receivers corresponding to the next character on the print drum, as indicated by the code wheel bits, are set. A complete character scan thus takes 132 cycles x 8.0 usec/cycle = 1.056 milliseconds maximum. At the end of a Character Scan, the core buffer retains the information received from the computer, the address register is cleared, and the clock is stopped.

4-132. Power Sequencing and Distribution

4-133. Sequencing (General). Sequencing of the power supplies is provided by the power sequencing relays. Figure 4-21 illustrates the order of sequencing and the on-time of the power sequencing relays and power supplies when the printer is energized. Figure 4-22 illustrates the sequence and on-time when the printer is de-energized.

4-134. Sequencing Logic. Relays K1, -2; and K3, -4 make up a pair of relay flip-flops. Relays K6 and K7 act as gates which connect the relays in the proper manner for counting forward (sequence on) or reverse (sequence off). Relay K5 serves the function of placing the relay flip-flops in the proper cleared state when power is sequencing on. Relay K8 is in parallel with relay K2 to provide additional sequencing contacts.

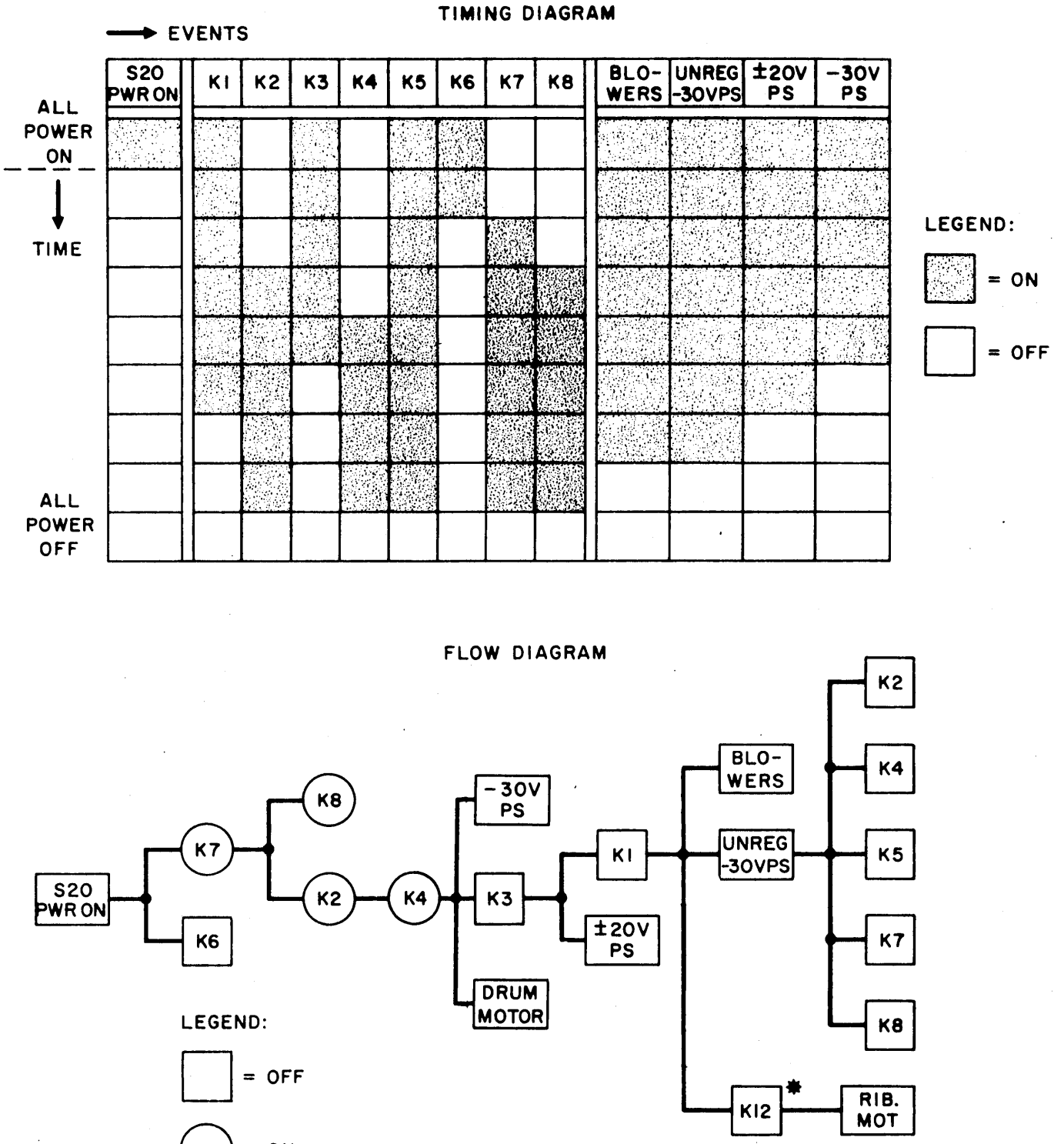


Figure 4-21. Power-Off Sequence Diagram

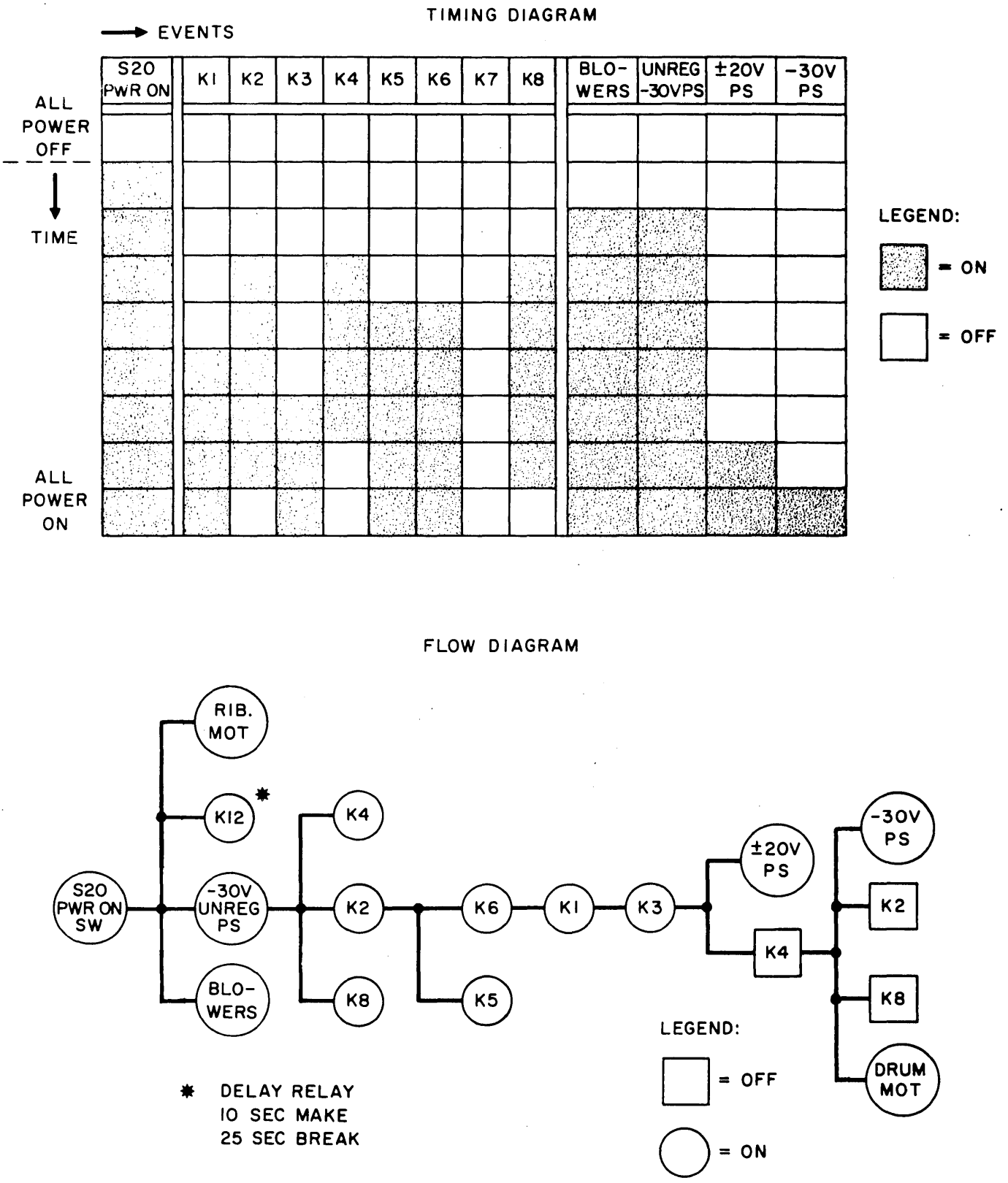


Figure 4-22. Power-On Sequence Diagram

4-135. Sequence On. When POWER ON switch S20 (see figures 4-21 and 4-23) is pressed on, power is supplied to the blowers (B101 through B106); ribbon motors; relay K12; the unregulated -30V relay supply; and the unregulated +6V lamp supply. The output of the unregulated -30V relay power supply starts the sequencing. Relays K2, K4, and K8 are energized. Current through contacts 1 and 3 of K4 energizes relay K5 and allows current through S20 to energize K6. Closed contacts 6 and 8 of K6 allow the current to continue through to the coil of K1. With K1 energized, current now passes through the contacts of K1 and K6 to the coil of K3. Contacts 6 and 8 of K1 parallel contacts 4 and 5 of S20. Closed contacts 6 and 8 of K3 connect the line voltage to the +, and -20V power supply while interrupting the energizing current to K4. Opening contacts 5 and 8 of K4 energize the -30V power supply, drum motor, and B107. With K1 energized, the opening contacts 1 and 3 of K4 cause K2 and K8 to drop out. The capacitor across the coil of K2 provides a delay for the -15V to the hammers.

4-136. Sequence Off. When POWER ON switch S20 (see figures 4-22 and 4-23) is pressed off, current is applied to the coil of K7 through the contacts of K5 and S20. At the same time, current to the coil of K6 is interrupted by S20, causing K6 to drop out. The now closed contacts of K7 permit the current to continue through CR2 to the coils of K2 and K8. The current that passed through contacts 1 and 3 of K5, 1 and 4 of K2, and 6 and 8 of K6 now passes through contacts 1 and 3 of K5, 1 and 3 of K2, and 6 and 8 of K7, energizing K4. The opening contacts 1 and 4 of K4 causes K3 to drop out. Opening

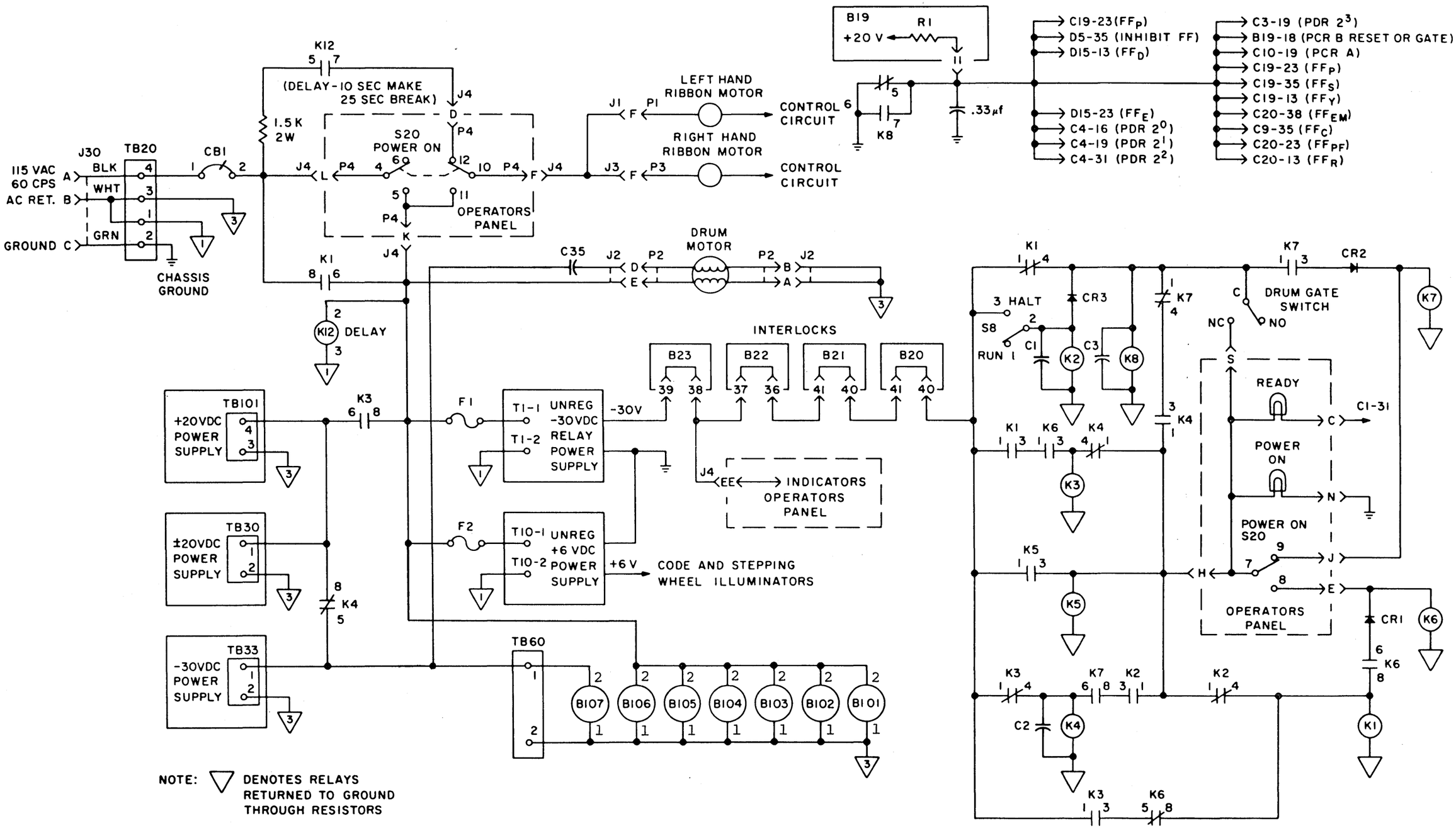


Figure 4-23. Sequencing and AC Distribution Diagram

contacts 5 and 8 of K4 de-energize the -30V power supply, drum motor, and B107. The two open sets of contacts of K3 disconnect power to both the +20V and -20V power supplies and to K1. Opening the contacts of K1 that paralleled S20 removes power to the blowers and the unregulated -30V relay and +6V lamp supplies. With power to the unregulated -30V relay supply removed, the remaining relays drop out. Reduced current to ribbon motors is routed through the 1.5K, 2W resistor and contacts of K12 for 25±5 seconds. This delay keeps a tension on the ribbon and prevents the ribbon from being drawn into the still spinning character drum.

4-137. D-C Distribution. D-c distribution is shown in figures 4-24, 4-25, and 4-26.

4-138. PRINTED-CIRCUIT CARD AND D-C POWER SUPPLY DESCRIPTIONS

4-139. The following paragraphs contain detailed description of the printed-circuit cards, the control panel, the power supply control system, and the power supplies utilized in the printer. When a card contains several similar circuits, one will be described as typical. For example, circuit 100 may be described, in which case Q1 in circuit 100 will be referred to as Q101.

4-140. Hammer Driver 1A (See Dwg. No. 200182).

4-141. Six hammer driver circuits are located on one card. Each circuit produces a firing pulse to the hammer upon receipt of a set pulse and an input signal. The duration of the output pulse is determined by the time between the set and the reset pulses.

4-142. In the quiescent state Q101 and Q102 are cut off. When a high level is applied to the input and a high set pulse occurs,

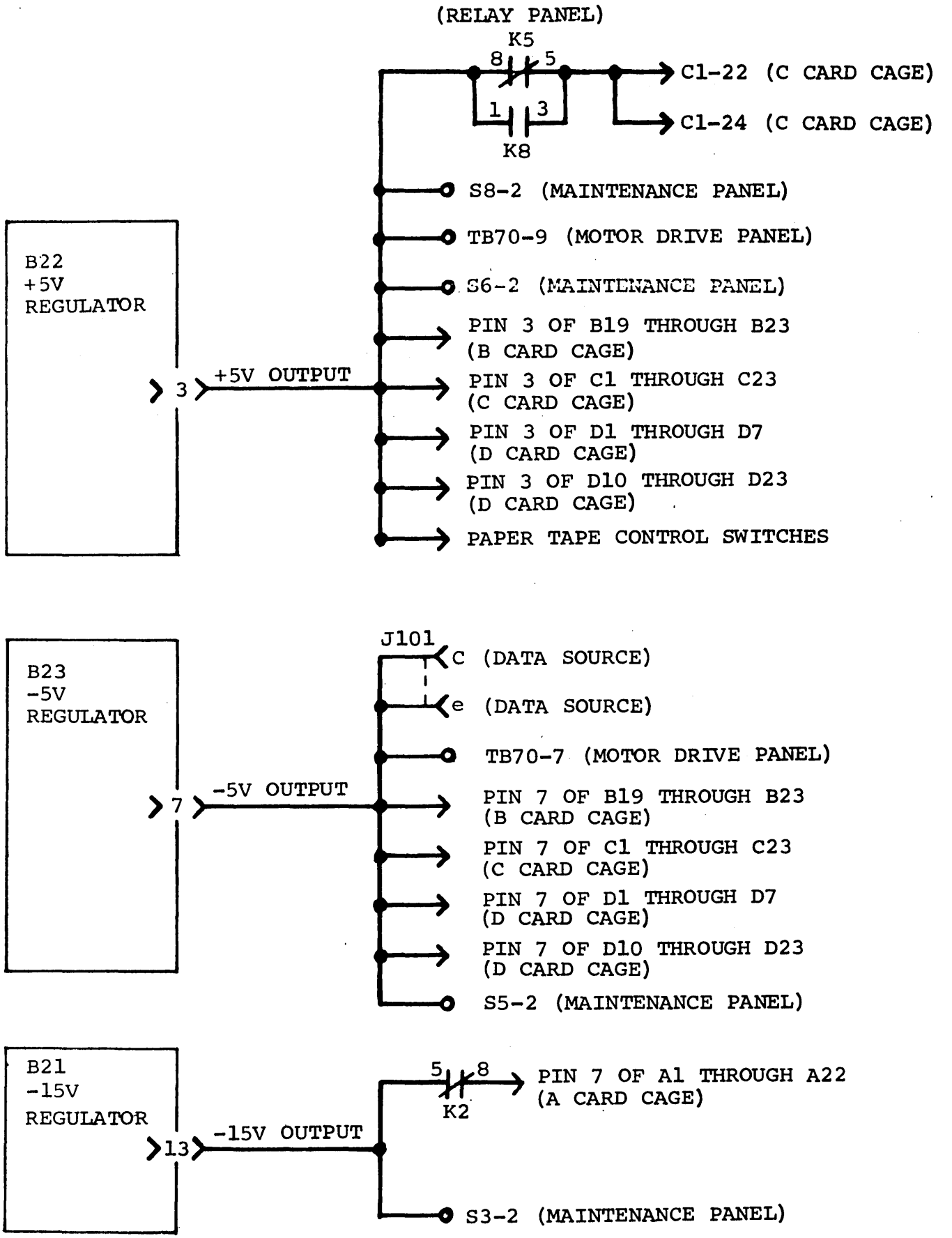
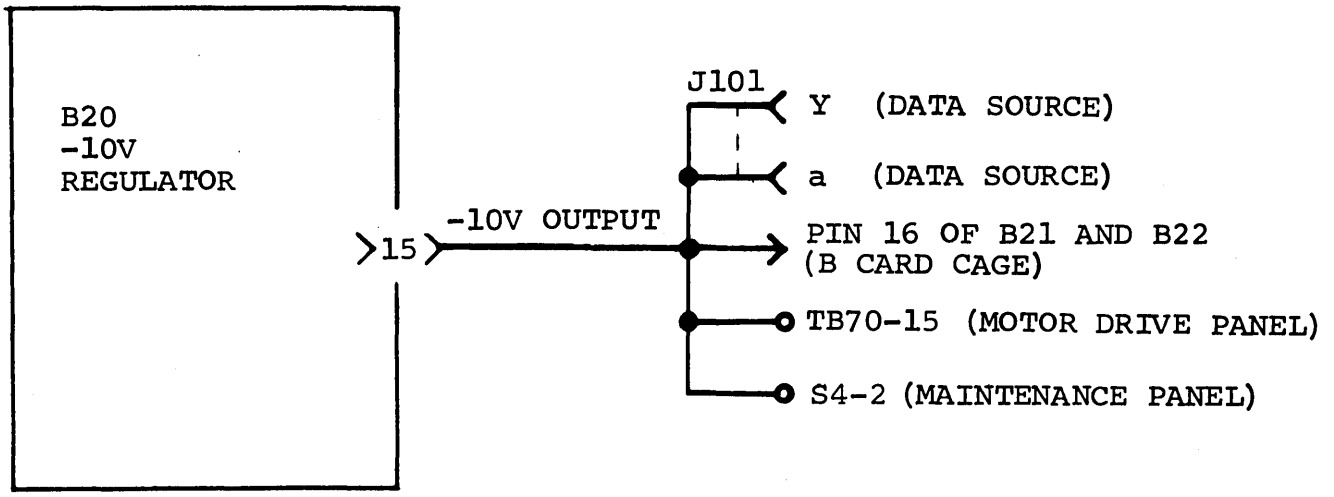
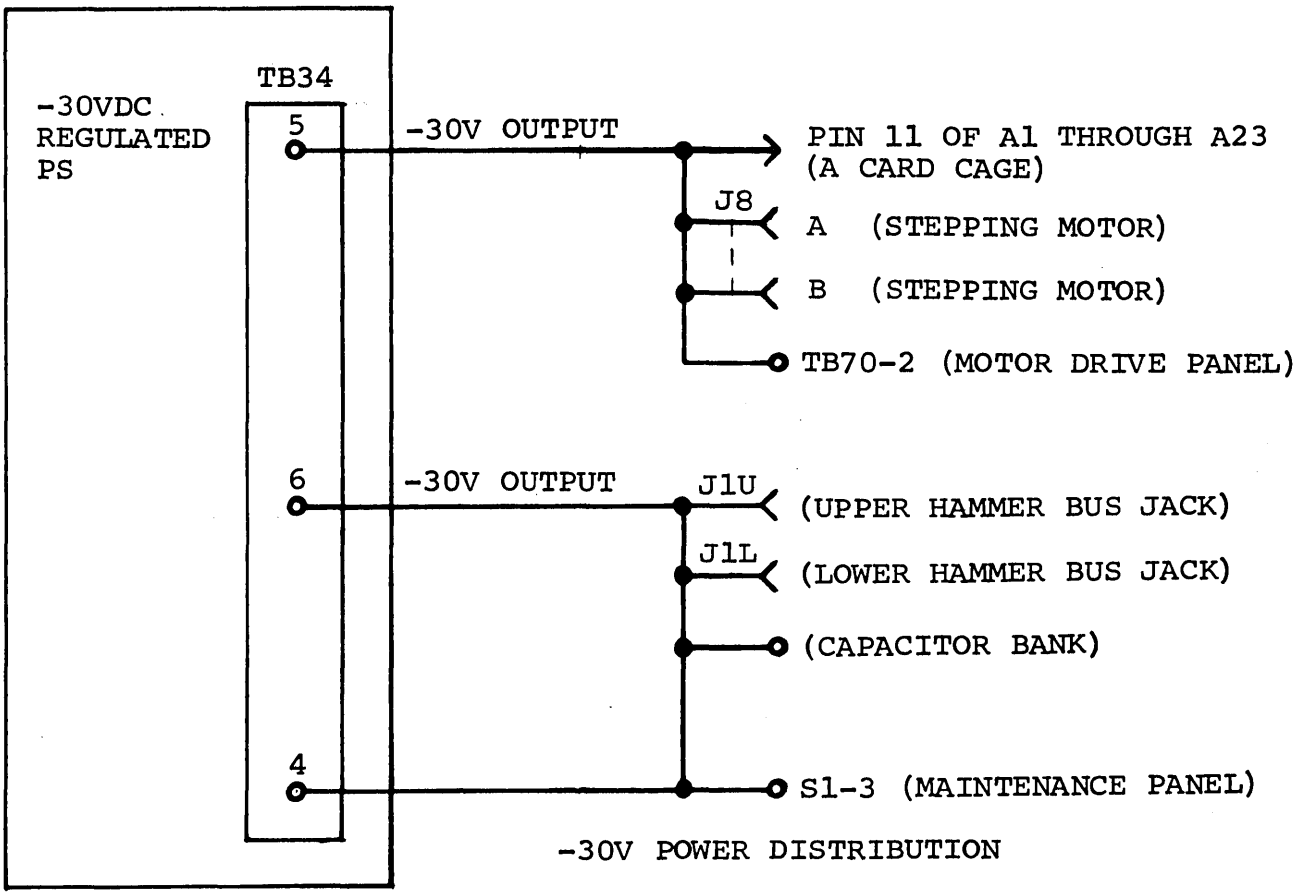


Figure 4-24. +5V, -5V, & -15V DC Distribution



-10V POWER DISTRIBUTION



-30V POWER DISTRIBUTION

Figure 4-25. -10V & -30V DC Distribution

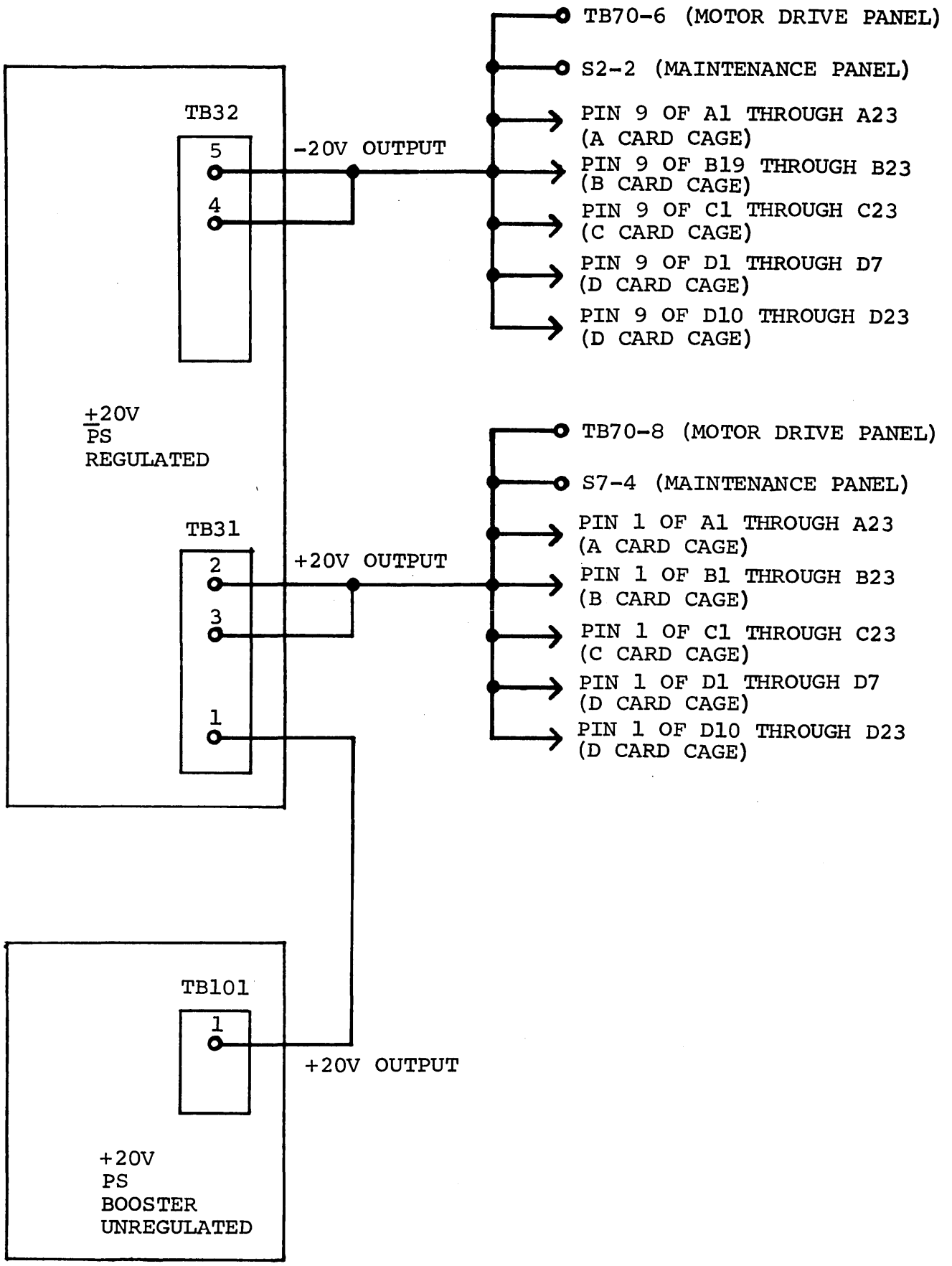


Figure 4-26. ±20V DC Distribution

the Q101 base becomes positive. Q101 conducts and applies a negative voltage to the Q102 base, driving that transistor to saturation. The current through Q102 now fires the corresponding hammer.

4-143. When a low signal is applied to the reset input, Q101 cuts off. Q102 is no longer forward biased and cuts off. The hammer driver is now reset and does not provide a firing pulse to the hammer.

4-144. Hammer Driver Receiver 2A (see Dwg. No. 200190).

4-145. The hammer driver receiver card consists of eight latching circuits. Each circuit receives a three-term decoded low input (zone select, circuit select 1, and card select) that sets the latching circuit. This circuit can be set independently of the decoded input by applying a positive voltage (high signal) to the circuit select 2 input. The hammer driver receiver circuit remains set until positive reset pulse (high signal) is applied to the reset input.

4-146. In the quiescent state, Q101 is cut off and presents an open circuit at the output. When the three-term decoded input is enabled or a high positive circuit select 2 signal is applied, Q102 conducts heavily and presents a high positive voltage at the output (the circuit is now reset).

4-147. Paper Feed Control 3D (see Dwg. No. 202071).

4-148. This card consists of three Schmitt trigger circuits (circuits 100, 200, and 500), four inverter circuits (circuits 600 through 900), an OR gate (circuit 300), and a driver amplifier (circuit 400).

4-149. The Schmitt trigger circuits produce a positive output when the input reaches a certain threshold value and maintains that output until the input falls below the threshold.

4-150. A rising voltage applied to the base of Q101 will cause Q101 to cut off when the voltage reaches a certain value. Q101's collector voltage will drive Q102 into conduction and produce a positive circuit output which is clamped at five volts. The positive signal on the collector of Q102 is coupled by C1 so that Q101 will not change state in response to small negative transients or noise.

4-151. Driver amplifier circuit 400 is a switch which supplies ground to energize a relay. A positive signal applied to the circuit input will cause Q402 to conduct and provide a ground path through output A for the load relay. Diode CR1 isolates the relay's inductive "kick".

4-152. Inverter circuits 600 through 900 provide ground outputs when negatively biased and outputs clamped at -5 volts when positively biased.

4-153. Circuit 300 is a positive OR circuit.

4-154. (Deleted.)

4-155. (Deleted.)

4-156. Hammer Driver Power Amplifier 5A (see Dwg. No. 200173).

4-157. This card is comprised of five power amplifier circuits. These circuits are used to amplify the set and reset hammer driver pulses and the zone select level.

4-158. The input signal is inverted by Q101 and power amplified by emitter followers Q102 and Q103.

4-159. Nor Gate 6A (see Dwg. No. 200232).

4-160. This card consists of seven NOR circuits. Each NOR circuit produces a -5 volt output when one or more of the inputs is positive and a +5 volt output when all of the inputs are negative.

4-161. Flip-Flop 7A (see Dwg. No. 200194).

4-162. The flip-flop card is comprised of three flip-flop circuits. The flip-flop circuit consists of two PNP transistors (Q102 and Q103). Amplification and inversion of the two outputs is provided by Q101 and Q104.

4-163. The flip-flop is set when Q103 is conducting and Q102 is cut off. This condition is obtained by applying a positive pulse

to the set 2 input while the set level input is at 0 volts or by applying a positive level to the set 1 input. The pulse is then differentiated and applied to the base of Q102, biasing Q102 to cut off. The negative going output at the Q102 collector is coupled to the Q103 base through C102, R105 and R108. This biases Q103 to saturation. The positive potential at the Q103 collector is inverted by Q104 and applied to the true output as -5 volts due to the clamping action of CR108. A common bias network provides a small positive bias level for the common emitters of all three flip-flop circuits.

4-164. Flip-Flop 7D (see Dwg. No. 200911).

4-165. The flip-flop card is comprised of 3 flip-flop circuits. The flip-flop circuit consists of two PNP transistors (Q102 and Q103). Amplification and inversion of the two outputs is provided by transistors Q101 and Q104. The flip-flop is set when Q102 is conducting and Q103 is cut off. This condition is obtained by applying a positive pulse to the set 2 input while the level input is at 0 volts or by applying a positive level to the set 1 input. The pulse is then differentiated and applied to the base of Q103, biasing Q103 to cut-off. The negative going output at the Q103 collector is coupled to the Q102 base through C103, R107 and R108. This biases Q102 to saturation. The positive potential at the Q2 collector is inverted by Q104 and applied to the true output as -5 volts due to the clamping action of CR112.

4-166. Decode 8A (see Dwg. No. 200224).

4-167. This card consists of 17 low-level AND gates. These circuits decode the address to select the proper hammer. The output

of any one AND gate will be negative only when all its inputs are negative.

4-168. Decode 8E (see Dwg. No. 201374).

4-169. This card contains five 3-term low-level AND gates, eight two-term low-level AND gates and two inverter circuits. The AND gates decode the address to select a specific address in the matrix. The output of any one AND gate will be negative only when all its inputs are negative.

4-170. Comparator 10E (see Dwg. No. 201410).

4-171. The comparator card consists of six EXCLUSIVE-OR gates (circuits 100 through 600) whose outputs are applied to one low-level inverting AND gate (circuit 800) and one EXCLUSIVE-OR gate (circuit 700) whose output is applied to an inverter (circuit 900).

4-172. Q101 and associated components comprise a positive-signal EXCLUSIVE-OR gate. When inputs A and B are both negative, the R101-R102-R103 voltage divider applies a negative level to the Q101 base. The greater negative levels applied to the anodes of diodes CR101 and CR102 prevent current flow through transistor Q101. The Q101 collector is now clamped to -5 volts by CR103. If the outputs of circuits 100 through 600 and input A, B, C, and D are negative, Q801 is forward biased and its collector output is +5 volts. Similarly, when inputs A and B are both positive, CR101, CR102 and Q101 are reverse-biased and the collector of Q101 is clamped to -5 volts.

4-173. If inputs A and B are unequal (one high and the other low) the R1-R2-R3 voltage divider junction voltage applied to the Q101

base is lower than the Q101 emitter voltage. Q101 is now saturated and its positive collector is now clamped at -5 volts by CR805.

4-174. Q901 is an emitter follower which power amplifies any signal applied at input A of circuit 900.

4-175. Output Driver 11A (see Dwg. No. 200220).

4-176. The output driver card contains ten inverter amplifier circuits. These circuits provide amplification and inversion for various signals.

4-177. Multivibrator 12A (see Dwg. No. 200240).

4-178. The multivibrator card is comprised of three multivibrator circuits, an inverter, an emitter follower and a positive AND gate.

4-179. The multivibrator circuit is a standard single shot multivibrator. In its quiescent state, Q201 and Q203 are biased to cut off while Q202 is biased to saturation. In this condition, the true output is at +5 volts and the false output is negative. A positive input pulse biases Q201 on, the emitter output of Q201 causes Q202 to cut off, which in turn biases Q203 into saturation. The Q203 collector is coupled to the Q202 base through C202 to keep Q202 biased to off. The R-C time of C202, R202, and R203 is such that after 0.5 msec., Q102 will again be biased into saturation. The circuit will then assume its quiescent condition.

4-180. The Q501 inverter circuit provides an output between +5 and -5 volts which is an inversion of the input.

4-181. Emitter follower Q301 power amplifies the input signal.

4-182. Q101 and associated circuits form a positive AND gate.

4-183. Logic Receiver 13D (see Dwg. No. 201572).

4-184. The logic receiver card consists of 10 level shifter circuits and ONE strobe circuit. This card provides level shifting to allow various input signals to drive the printer circuitry.

4-185. Negative time logic input signals are applied to the Q101 base while the Q102 base is clamped at a voltage midway between the ONE and ZERO logic levels. Positive true logic input signals are applied to the Q102 base or a negative-going signal is applied to the Q101 base (when the strobe circuit is not connected to the level shifter), Q103 conducts and the output is +5 volts. If these input signals do not occur, Q103 is cut off and the output is clamped to -5 volts by CR102.

4-186. If a level shifter is connected to the strobe circuit, its output remains clamped at -5 volts even though input signals are applied unless a positive strobe signal is applied to the base of Q1101. When this positive strobe signal occurs, Q1101 cuts off and removes a +5 volt disabling level from the Q101 - Q102 emitters. This signal allows the Q101 or Q102 base signals to control the conduction of Q3.

4-187. Logic Driver 21M (see Dwg. No. 201405).

4-188. The logic driver card consists of 14 high-level AND gates, three low-level inverting AND gates and one inverter. These circuits are connected as a binary counter to advance the address register sequentially.

4-189. The CR1-CR2 AND gate (typical of the 14 high-level gates) is enabled when both inputs are high to produce a high output. The

CR30-CR31-Q1 low-level inverting AND gate (typical of the 3 inverting AND gates) is enabled when both inputs are low to produce a high output. The Q3 inverter circuit reverses the input to produce either a +5 or -5 volt output.

4-190. Logic Driver 21N (see Dwg. No. 201454).

4-191. This card consists of eight low-level AND gates, two low-level inverting AND gates, one low-level OR gate, and one inverting amplifier.

4-192. The outputs of the eight low-level AND gates (CR1-CR32) are applied to the low-level OR gate (CR33-CR40). When one or more of the low-level AND gates is enabled, a negative-going Q7 emitter signal is produced. This signal is applied to the low-level AND gate (CR41-CR42-CR43) which, when enabled, forward biases Q1. When Q1 conducts, its positive collector voltage reverse biases inverting amplifier Q2. The collector of Q2 is then clamped to -5 volts by CR46. This negative voltage is now applied to the low-level AND gate (CR47-CR48-CR49) which, when enabled, drives Q3 to saturation. When Q3 conducts, its collector voltage is positive.

4-193. Logic Driver 21P (see Dwg. No. 201478).

4-194. This card consists of three selection switches (circuits 100 and 900), four gates (circuits 300, 400 and 500), one amplifier (circuit 800) and three indicator switches (circuits 200, 600, and 700).

4-195. The selection switches are connected in series with the drive lines and either open or close one end of the drive current circuits. Each switch is selected by a particular combination of address bits. In the quiescent state, Q101 and Q102 are cut off. When low-level AND gate CR101-CR102 is enabled, Q101 is driven to saturation. The positive Q101 collector voltage now forward biases Q102, closing that switch to complete one end of the drive current circuit.

4-196. Circuits 300, 400, and 500 are used as either high level OR gates or low level AND gates.

4-197. Circuits 200, 600, and 700 are connected in series with indicators. A high level, applied to the base, keeps switch Q201 cut off (open) and the indicator does not light. A low level, applied to the base, drives switch Q201 to saturation (closed) and the indicator lights. A low level, applied to the base, keeps Q601 and Q602 cut off and the indicator does not light. A high level, applied to the Q601 base, drives switch Q602 to saturation (closed) and the indicator lights.

4-198. Logic Driver 21V (see Dwg. No. 202496).

4-199. Card 21V consists of a level-changing input gate, and five AND gates. The circuits together produce the Send Data and Printer Ready signals. The level-changing circuit changes the data source's +10-volt TRUE and 0-volt FALSE logic levels. A -5 volt reference is applied to the base of Q1; applied to the base of Q2 is the data source Override signal. As long as the Override is false (0 volt) the gate CR9, CR10, and CR11 is enabled. When the Override is true (+10 volts) gate CR9, CR10, and CR11 will be disabled and gate CR13, CR14, CR15, and CR16 will be enabled despite the printer's not being on zero count or the absence of paper or an unready indication from the READY switch.

4-200. NAN Gate 22C (see Dwg. No. 201438).

4-201. The NAN gate card consists of ten NAN circuits and one inverter. Each NAN circuit produces a -5 volt output when both inputs are positive and a +5 volt output when one or both of the inputs is negative.

4-202. Sense Amplifier 27B (see Dwg. No. 201686).

4-203. This card consists of four read amplifiers, one voltage reference circuit (common to the four read amplifiers), and one strobe amplifier which is common to the four read amplifiers.

4-204. Each sense amplifier receives core turnover signals through a sense winding and provides an amplified output signal when enabled by the read strobe pulse. The ends of one sense winding are connected, through T101, to the bases of Q101 and Q102.

4-205. The opposite-polarity (differential) output signals applied to the bases of Q101 and Q102 appear, amplified and inverted, at the collectors of the two transistors and are directly coupled to the transistors Q103 and Q104 of the next stage. The Q103 and Q104 outputs are applied to the base of inverter Q105. The reference voltage for Q105 is established by the setting of R602 which controls the emitter voltage of Q601 (R602 is adjusted so the sense amplifiers will amplify a minimum ONE and not amplify a maximum ZERO). The Q105 collector voltage is applied to the base of inverter Q106. When Q106 conducts, the output is +5 volts. When Q106 is cut off, the output is clamped to -5 volts by CR107.

4-206. In the quiescent state, Q501 is conducting and shorts out any signal received from the collectors of Q103 or Q104. The output is now clamped to -5 volts by CR107.

4-207. When a negative read strobe signal occurs, Q501 is cut off. Now any positive signals at the collectors of Q103 or Q104, greater than the reference voltage at the Q105 base, reverse biases Q105. This drives Q106 to saturation and the output is now +5 volts.

4-208. Inhibit Driver 28B (see Dwg. No. 201469).

4-209. This card consists of eight inhibit drivers and three inverters. The inhibit drivers are connected in series with the inhibit lines and either upon open or close the inhibit current

circuit. Each inhibit driver is selected by the low-level common strobe input from the inhibit flip-flop and the low input 2 (false output of either memory register or sentinel flip-flop).

4-210. In the quiescent state, Q101 is conducting heavily and Q102 is cut off. When the inputs to the low-level AND gate CR101-CR102 are both low, the conduction of Q101 decreases and applies a negative voltage to the base of Q102. This drives Q102 to saturation and completes the inhibit current path.

4-211. Inverter Q901 produces a positive output when low-level AND gate CR901-CR902-CR903 is enabled and when a low-level is applied to input 4. Inverter Q1001 produces a negative output, due to the clamping action of CR1004, when one of the inputs to high-level OR gate CR1001-CR1002-CR1003 is high.

4-212. Selection Switch 29A (see Dwg. No. 301329).

4-213. This card consists of 11 selection switches. These switches are connected in series with the drive lines and either open or close end of the drive current circuits. Each switch is selected by a particular combination of address bits.

4-214. In the quiescent state, Q101 and Q102 are cut off. When low-level AND gate CR21-CR22 is enabled, Q101 is driven to saturation. The positive Q101 collector voltage now forward biases Q102, closing that switch to complete one end of the drive current circuit.

4-215. Clock/Timing 31B (see Dwg. No. 201774).

4-216. This card consists of the read and write drive current source circuits, four low-level AND gates, and the gated clock circuits.

4-217. In the quiescent state, Q5 is cut off, Q6 and Q8 are saturated, and Q7 and Q9 are cut off. When a negative signal is received from enabled low-level AND gate CR23-CR24, Q5 conducts.

4-218. Its negative-going collector voltage appears at the emitter of Q6 and Q8. This forward biases Q7 and Q9 which supply the read currents to the X and Y drive lines.

4-219. When a negative signal is received from enabled low-level AND gate CR27-CR28, Q10 conducts. Its positive-going collector voltage appears at the emitters of Q11 and Q13. This forward biases Q12 and Q14 which supply the write currents to the X and Y drive lines.

4-220. The gated clock circuit produces a free running square wave output when a negative signal level is applied to one of the OR gate inputs (CR8, CR9, or CR10). This negative signal causes Q3 to be biased to cut off, thereby permitting the emitter coupled astable multivibrator to oscillate. The frequency of oscillation is determined by the selection of the emitter coupling capacitance and the setting of R5. The multivibrator output pulse is inverted and level standardized by Q4 and applied to the output.

4-221. Delay Line 33C (see Dwg. No. 201485).

4-222. This card consists of seven 0.5 usec delay lines, four emitter followers, one indicator switch and one emitter follower which has a high-level AND gate at its input.

4-223. Each delay line provides a 0.5 usec delay. The four emitter followers provide power amplifications. Q1401 provides power amplification when all inputs to CR1401, CR1402 and CR1403 are high.

Q1301 is connected in series with an indicator. When the switch is closed, by applying a negative signal to the base of Q1301, the indicator lights.

4-224. -5V Regulator 99A (see Dwg. No. 200418).

4-225. The -5V regulator card consists of one shunt regulator circuit. Electrons flow from the -20 volt source through an external resistor into the regulator card at the -5V output. Any change in the output voltage is applied to the base of Q4. This change in voltage is amplified by difference amplifier Q3-Q4. The output from the difference amplifier (Q3 collector) is coupled through emitter follower Q2 and applied to the base of shunt regulator Q1. This voltage change at the Q1 base either increases or decreases the conduction of Q1 to make up for the original change in voltage. The output voltage can be varied by switching in external margin circuits when the card is installed in the equipment.

4-226. +5V Regulator 99B (see Dwg. No. 200255).

4-227. The +5V regulator card consists of one shunt regulator circuit. The +5V output is connected through an external resistor to the +20 volt supply. Any change in the output voltage is applied to the base of Q4. This change in voltage is amplified by difference amplifier Q3-Q4. The output from the difference amplifier (Q4 collector) is coupled through emitter follower Q2 and applied to the base of shunt regulator Q1. This voltage change at the Q1 base either increases or decreases the conductor of Q1 to make up for the original change in voltage. The output voltage can be varied by switching in external margin circuits when the card is installed in the equipment.

4-228. -10V Regulator 99D (see Dwg. No. 200422).

4-229. The -10V regulator card consists of one series regulator. Any change in the output voltage is amplified by differential amplifier Q3-Q4. The difference amplifier output is coupled through emitter follower Q2 and applied to the base of series regulator Q1. This voltage change at Q1 base alters the output current to oppose the original change in voltage. The output voltage can be varied by switching in external margin circuits when the card is installed in the equipment.

4-230. -15V Regulator 99E (see Dwg. No. 200426).

4-231. The -15V regulator consists of one series regulator. Any change in the output voltage is amplified by differential amplifier Q3-Q4. The difference amplifier output is coupled through emitter follower Q2 and applied to the base of series regulator Q1. This voltage change at Q1 base alters the output current to oppose the original change in voltage. The output voltage can be varied by switching in external margin circuits when the card is installed in the equipment.

4-232. -30 Volt Power Supply. (See logic diagram 30). The -30 volt d-c power supply utilizes a unijunction transistor relaxation oscillator to operate the silicon controlled rectifiers (SCRs) which control the power supply output. Low-power regulator components are mounted on a printed circuit board in the power supply assembly.

4-233. The output voltage is applied to the Q5-Q4 differential amplifier where the voltage from the voltage-adjusting potentiometer

R34 is compared with the fixed voltage drop across zener diode CR8. The output voltage from the Q4 collector is driven negative as the output voltage decreases.

4-234. Current flows from power transformer T1 to the external power supply load through CR1 and CR4 when CR4 is conducting, and alternately through CR3 and CR2 when CR2 is conducting. The output voltage is filtered by C1, L1, and the external capacitor bank; R2 is the bleeder resistor. The voltage drop across current-sensing resistor R2 is proportional to the power supply output current. The output current is increased as the duty cycle of the SCRs is increased.

4-235. Two negative control voltages are provided by low-power transfer T2. The output of its full-wave bridge rectifier is applied to the R7-CR7-CR6-C1 circuit, which develops the negative d-c voltage for the Q4-Q5 differential amplifier. The rectifier output is also applied to the resistor R2-zener diode CR5 circuit. The applied voltage is shown by the dotted lines in figure 4-27(d). The solid line shows the clipped voltage at the R2-CR5 junction. This voltage is the operating voltage for the Q1 relaxation oscillator circuit.

4-236. Unijunction transistor Q1 and its associated components comprise the relaxation oscillator. With Q1 cut off, capacitor C1 charges through resistor R5 and transistor Q2. When capacitor C1 is charged sufficiently, emitter current flow into Q1 starts. The unijunction transistor then starts to operate in its negative-resistance mode. As the current flow in the C1-Q1-T1 circuit

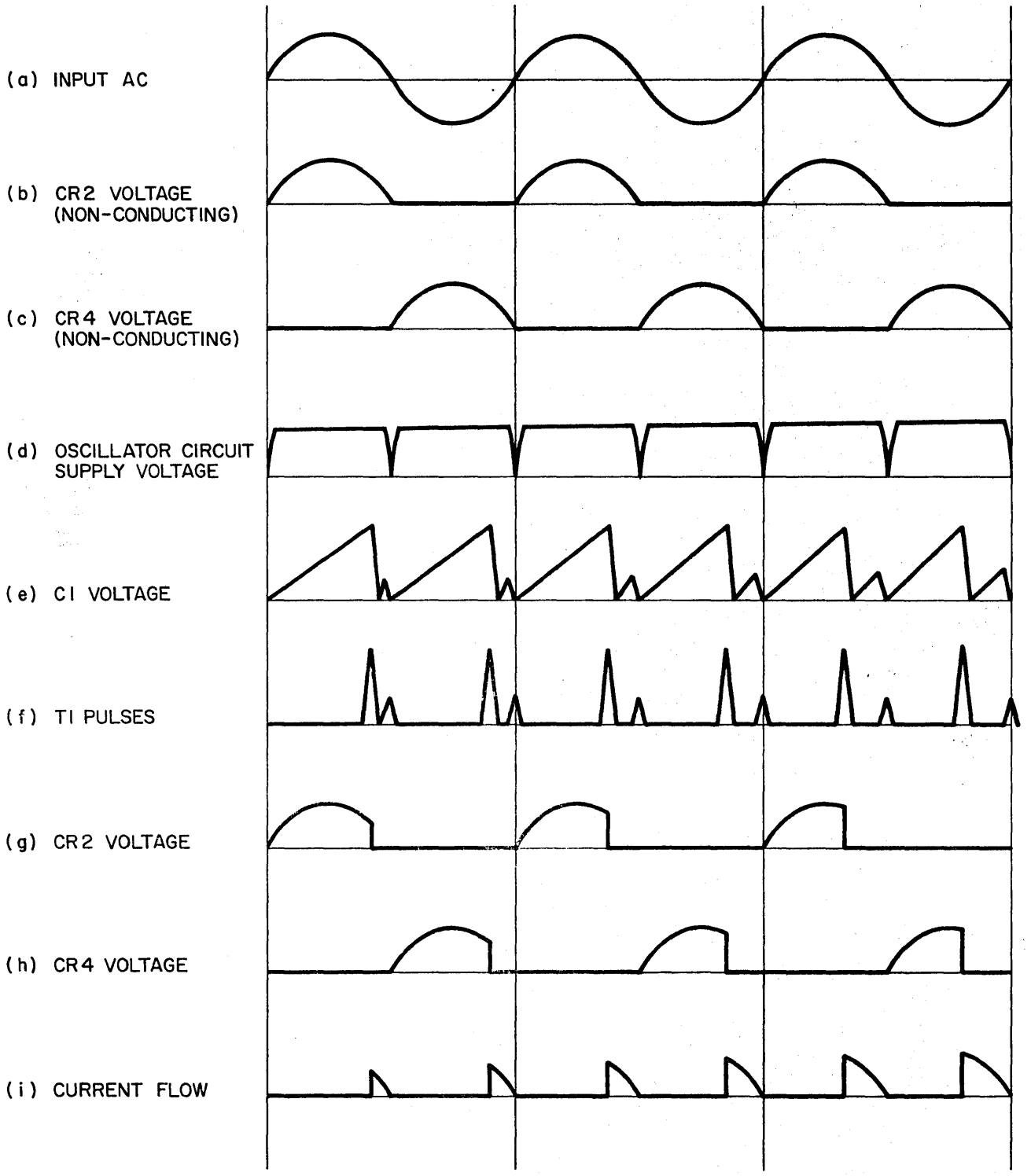


Figure 4-27. Power Supply Waveforms

increases, the resistance of this circuit through Q1 decreases. Capacitor C1 is discharged. The Q1 base voltage decreases open-circuiting the C1 discharge path through Q1.

4-237. As the end of a half-cycle is reached, capacitor C1 normally has a small charge. The oscillator circuit supply voltage and Q1 base voltages decrease toward zero volts, increasing the Q1 forward bias until Q1 again operates in its negative-resistance mode and discharges C1. Thus, at the start of each half-cycle C1 has no charge. The operation of the relaxation oscillator circuit is synchronized with the power supply input a-c voltage.

4-238. During the next half-cycle, capacitor C1 again charges through R5 and Q2 until Q1 conducts. The time required for C1 to charge sufficiently to forward-bias Q1 is determined by the transistor Q2 collector current. This is varied by the Q2 base current, which is controlled by the differential amplifier output signal. The voltage across capacitor C1 with a negative-going Q2 base voltage is shown in figure 4-27(e).

4-239. The discharge of C1 through Q1 generates a pulse in a pulse transformer T1 winding in series with as shown in figure 4-27(f). The output pulses from the other two windings are applied to the gate inputs of SCRs CR2 and CR4. Pulses applied between half-cycles have no affect on the SCRs since no voltage is applied across either SCR at this time.

4-240. The voltages appearing across the SCRs when they are non-conducting are shown in Figure 4-27(b) and (c). As shown in Figure 4-27(g) and (h), the transformer-coupled oscillator output

pulses drive the forward-biased SCR into its conducting state. As the power supply load increases, the resultant differential amplifier negative-going output decreases the C1 charge time as previously described. The SCR firing angle (number of degrees of a cycle that the SCR conducts) is increased.

4-241. Figure 4-27(i) shows the combined current from the two SCRs in response to an increasing external load.

4-242. With normal output currents, current-limiting transistor Q3 is normally cut off and has no effect on circuit operation. The voltage developed across current-sensing resistor R2 is applied through a silicon diode to the Q3 base. An excessive current surge during turn-on or overload forward-biases Q3. Conducting transistor Q3 limits the negative value of the differential amplifier output voltage which is applied to the Q2 base, and charges a capacitor. A diode limits the voltage across the capacitor. The discharge time of the capacitor is of sufficient length to provide limiting action during the next half-cycle of applied a-c voltage. Thus, continuous excessive current surges during power supply turn-on and overload conditions are prevented. When the load decreases, Q3 is cut off and the capacitor is discharged. The differential amplifier output voltage is applied directly to the Q2 base.

4-243. +, and -20 Volt Power Supply. (See logic diagram 29). This power supply consists of two identical power supply circuits with a common power transformer. These power supply circuits include voltage-regulating and current-limiting circuits. Low-power circuitry for each individual supply is located on a printed circuit board in the supply.

4-244. The -20 volt circuitry is typical of both circuits. Current from the power transformer T1 secondary winding flows through rectifier diodes CR1 and CR2, parallel series-regulating transistors Q1 and Q2, 0.5-ohm equalizing resistors R1 and R2, and the positive-voltage output. The -20 volt supply positive-voltage output is connected to the printer signal ground. The T1 center-tap is connected directly to the negative output.

4-245. The -SENSE and +SENSE terminals are externally connected to the -20 volt and signal ground outputs respectively. Differential amplifier Q10-Q11 compares an adjustable proportion of the output voltage with the voltage drop across zener diode CR10.

4-246. A low-power T1 secondary winding, diodes CR6 and CR7, and capacitor C3 provides an unregulated control voltage. Resistor R8 and zener diode CR11 provide a positive operating voltage for the differential amplifier and for transistor Q9. The amplified voltage-difference signal from the Q10 collector is amplified and inverted by transistor Q9. The Q9 output is amplified and inverted by Q8. With diode CR5 conducting, the Q8 emitter voltage is applied to Q3. Transistor Q3 supplies base current to Q1 and Q2.

4-247. A tendency of the output voltage to decrease results in the following:

(a) With reference to the negative output, the Q10 base voltage is driven more negative than the Q11 base voltage.

(b) The total current flow through the differential amplifier remains constant; less current flows through Q11

and resistor R11. A more positive voltage is applied to the Q9 base.

(c) Transistor Q9 is driven toward saturation and drives Q8 toward cutoff.

(d) The positive-going Q8 collector voltage is applied through diode CR5 to the Q3 base.

(e) The Q3 base current is increased. Since the Q3 emitter current is the total base current of the two series-regulating transistors, current flow is increased through Q1 and Q2 and the external load. The original voltage is restored. The above steps are proportional actions; no appreciable voltage variation appears at the power supply output. An increase in the output voltage results in the opposite power supply regulating actions.

4-248. Operation of the current-limiting circuits is as follows:

(a) The voltage drop across current-equalizing resistor R1 is proportional to the power supply output current. The negative connection of this resistor, which is the power supply positive output, is connected to the Q7 emitter.

(b) Zener diode CR8 and resistor R3 maintain a fixed voltage across current-adjustment potentiometer R33. The voltage drop from the positive side of resistor R1 to the Q7 base is thus a constant voltage. Potentiometer R33 is adjusted so that Q7 is normally cut off.

(c) An increase in output current causes an increased voltage drop across resistor R1. With reference to the Q7 emitter, the Q7 base voltage is driven more positive. Transistor Q7 is forward biased.

(d) Current flow through Q7 increases to limit the Q3, Q1, and Q2 currents. This action is proportional and operates only during the time that the power supply load is excessive.

4-249. The +20 volt d-c in the printer is supplied by two power supplies. An unregulated +20 volt supply continuously supplies power to the +20 vdc busses. The regulated power supply senses the combined outputs of both supplies, and regulates its output to maintain a regulated voltage of +20 vdc.

4-250. Unregulated +20 Volt D-C Power Supply. (See logic diagram 28). This supply consists of power transformer T1. full-wave bridge rectifier CR1 through CR4, and resistor R1. The output of this circuit utilizes the bleeder resistor R6-1 and filter capacitor C5 contained in the regulated supply assembly (see logic diagram 29).

4-251. Margin Voltages. Margin voltages are applied to any or all power supplies in all combinations from switches on the maintenance panel.

4-252. Margin-voltage operation of all supplies and regulators is similar; the -30 volt supply operation is described below.

4-253. The output voltage is sensed by a voltage divider consisting of resistor R16, voltage-adjusting potentiometer R34, and

resistor R18 (see Schematic No. 30), connected across the power supply output. The proportion of the output voltage applied to the differential amplifier is dependent on the ratio of the resistances on both sides of the potentiometer center tap.

4-254. Placing margin switch S1 in the LOW position (see logic diagram 24) places resistor R6 in parallel with resistor R16. The apparent sensed voltage to the differential amplifier is driven positive. To maintain equilibrium conditions, the regulator then decreases the output voltage.

4-255. Conversely, placing margin switch S1 in its HIGH position connects resistor R7 in parallel with resistor R18 and decreases the resistance on the negative side of the voltage divider. This is detected as an apparent decrease in the output voltage. The regulator increases the power supply output voltage. With the circuit resistance used, voltage shifts of $\pm$5 percent are required to maintain equilibrium.

4-256. Voltage Metering. Each power supply and regulator output voltage can be measured by the d-c voltmeter on the maintenance panel. The meter is placed in its OFF position, or connected to a particular voltage by 3-deck VOLTAGE SELECT wafer switch S9 (see Schematic No. 24).

4-257. Decks B and C of switch S9 select the required connections for the polarity of the voltage to be checked. Level A selects the voltmeter range. With switch S9 in the +5V, -5V, or -10V position resistor R8 is in series with the meter; the 20-volt scale is used for these voltages. When the other voltages are applied to

the meter, resistor R9 is in series with the meter; the 40-volt scale is used.

4-258. Each voltage is applied to the meter through a calibrating potentiometer which is initially adjusted to provide accurate meter operation for each voltage.

4-259. +6 Volt Unregulated Lamp Supply. (See logic diagram 25). The +6 vdc power supply generates the d-c voltage for the lamps which are used with the printer code wheels and photo-diodes.

4-260. With relay K3 energized, 115-volt a-c is applied through fuse F2 to the primary winding of power transformer T10. The 6-volt a-c output from the T10 secondary winding is applied to the CR20 through CR23 full-wave bridge rectifier. The positive rectified output is filtered by capacitor C31.

4-261. -30 Volt Unregulated Relay Supply. (See logic diagram 25). The -30 vdc relay power supply supplies the d-c power to operate the power supply sequencing relays.

4-262. Relay K3 applies 115-volt a-c through fuse F1 to the power transformer T1 primary winding. The a-c output from the T1 secondary winding is applied to the CR24 through CR27 full-wave bridge rectifier. Potentiometer R20 is initially adjusted to maintain the output at -30 volts d-c. Capacitor C30 provides filtering of the output voltage.

4-263. PRINTER MNEMONIC INFORMATION, LOGIC FORMULAE, AND DETAILED BLOCK DIAGRAM.

4-264. Mnemonic Information

4-265. Figure 4-28 provides a description of the various mnemonic terminology associated with the printer.

FIGURE 4-28. PRINTER MNEMONIC INFORMATION

SIGNAL TYPE	MNEMONIC	SIGNAL NAME	SIGNAL DESCRIPTION
Control Flip-Flops	FF_R	Ready For Loading Flip-Flops	1=Load char. or paper info. from computer. 0=Printing.
	FF_{PF}	Paper Feed Flip-Flop	Transfers paper feed info. bits to paper drive logic & inhibits char. information loading functions.
	FF_C	Character (Strobe) Flip-Flop	Enables 500-kc clock for char. or paper feed info. loading.
	FF_{EM}	End Message Flip-Flop	Disables SEND DATA signal after loading of last char.
	FF_V	Virgin Flip-Flop	Synchronizes char. scans with print drum & code wheel position.
	FF_P	Parity (Error) Flip-Flop	Indicates that a parity error has been detected.
	FF_S	Sentinel (Indicator) Flip-Flop	Indicates that one or more sentinels have been detected during a char. scan.
	FF_{SNTL2}	Sentinel-2 Flip-Flop	Holds sentinel bit during compare operation.
Memory Register Stages (8)	FF_{SNTL}	Sentinel Flip-Flop	Holds sentinel bit.
	$MR2^0-2^6$	Memory Register 2^n	Holds input data for storage or transfer; holds buffer read-out data for comparison & restoration.

FIGURE 4-28. PRINTER MNEMONIC INFORMATION (cont'd.)

SIGNAL TYPE	MNEMONIC	SIGNAL NAME	SIGNAL DESCRIPTION
Address Register Stages (8)	$AR2^0-2^7$	Address Bits 2^n	Sequentially-driven count-up counter which holds core buffer and hammer addresses.
Paper Drive Registers	PTR 2^0-2^2	Paper (Tape) Register Bits 2^n	Tape mode: holds tape channel info. Count mode: operates as count-down counter.
	PTR 2^3	Paper (Tape) Register 2^3 Bit	0=tape mode; 1=count mode
	PDR 2^0-2^3	Paper Delay Register Bits 2^n	With PTR 2^3=0, PTR 2^0-2^2 operates as normal binary count-up counter. With PTR 2^3=1, total count to return to zero is increased.
	PCR A	Paper Count Register (Bit A)	Register is counted to sequence application of torque to stepping motor.
	PCR B	Paper Count Register (Bit B)	
Misc. Flip-Flops	TOF	Top of Form Flip-Flop	Converts switch output to logic signal.
	CH. 1	Channel 1 Flip-Flop	Indicates detection of tape hold in Channel 1 (Top of form channel)
	CH. 7	Channel 7 Flip-Flop	Indicates detection of tape hold in Channel 7 (Bottom of form channel)
Data Bits	$ID2^0-2^2$	Input Data 2^n	Input low-order 3 bits of char. info., or input paper feed info.
	$ID2^3-2^5$	Input Data 2^n	Input high-order 3 bits of char. info.

FIGURE 4-28. PRINTER MNEMONIC INFORMATION (cont'd.)

SIGNAL TYPE	MNEMONIC	SIGNAL NAME	SIGNAL DESCRIPTION
	ID^6	Input Data 2^6	Input (odd) parity bit for 6 char. input bits
	BD_{SNTL}	Buffer Data Sentinel Bit	Sense winding output of stored sentinel bit
	$BD2^0$-2^5	Buffer Data Bits 2^n	Sense winding output of stored char. bit
	$BD2^6$	Buffer Data Bit 2^6	Sense winding output of stored (odd) parity bit
	$CC2^0$-2^5	Code Wheel Bits 2^n	Code Wheel Data Bits
	$CC2^6$	Code Wheel Bit 2^n	Code Wheel Parity Bit (Odd)
Timing Flip-Flops	FF_D FF_E	FF_D FF_E	Counter which operates to sequence timing pulses.
Signals	AND D	AND D	Indicates loading of paper feed instructions.
	PM	Paper Moving	Inhibits SEND DATA signals and character scans until paper motion is stopped.
	132	132	Indicates that address register holds 132nd address.
Address Decode Signals	DECODE A1 DECODE B4 DECODE B0 DECODE B5	$\overline{AR1}\cdot\overline{AR2}$ $\overline{AR5}\cdot\overline{AR6}\cdot\overline{AR7}$ $\overline{AR5}\cdot\overline{AR6}\cdot AR7$ $\overline{AR3}\cdot\overline{AR4}$	Partial decoded outputs of Address Register (Decode A1•Decode B4 $\cdot 2^0=131$; Decode B0 Decode B5$\cdot 2^{\overline{0}}\cdot 2^{\overline{1}}\cdot 2^{\overline{2}}=0$)

FIGURE 4-28. PRINTER MNEMONIC INFORMATION (cont'd.)

SIGNAL TYPE	MNEMONIC	SIGNAL NAME	SIGNAL DESCRIPTION
Core Buffer Drive Lines	X0-X7	X^n	X (read & write) drive (current) lines
	Y0-Y16	Y^n	Y (read & write) drive (current) lines

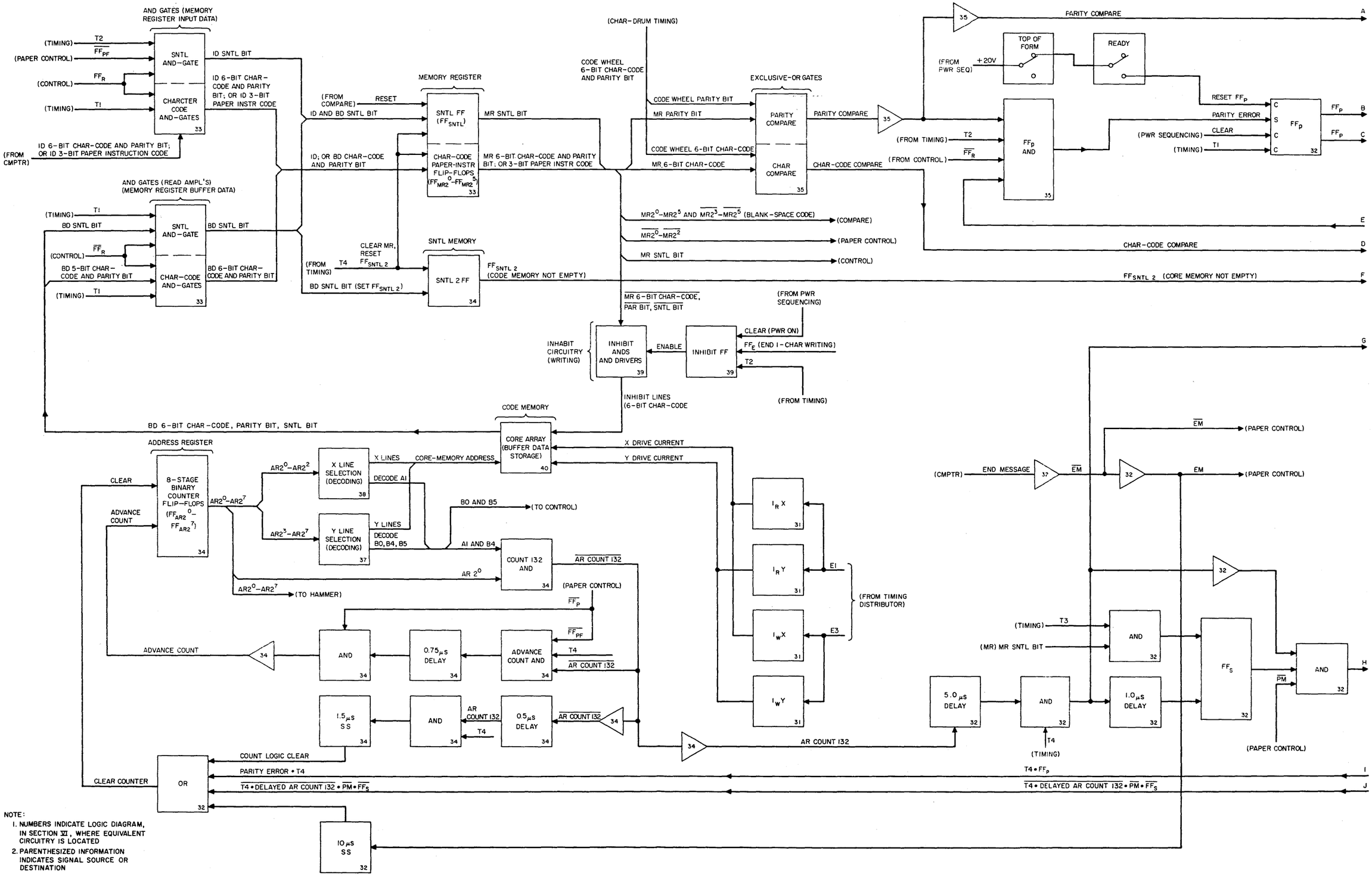
4-266. Logic Formulae

4-267. (Deleted.)

4-268. Detailed Block Diagram

4-269. Figure 4-30 is a detailed block diagram of the printer.

FIGURE 4-29. LOGIC FORMULAE
(Deleted)



NOTE:

1. NUMBERS INDICATE LOGIC DIAGRAM, IN SECTION XII, WHERE EQUIVALENT CIRCUITRY IS LOCATED
2. PARENTHESIZED INFORMATION INDICATES SIGNAL SOURCE OR DESTINATION

Figure 4-30 Printer Detail Block Diagram

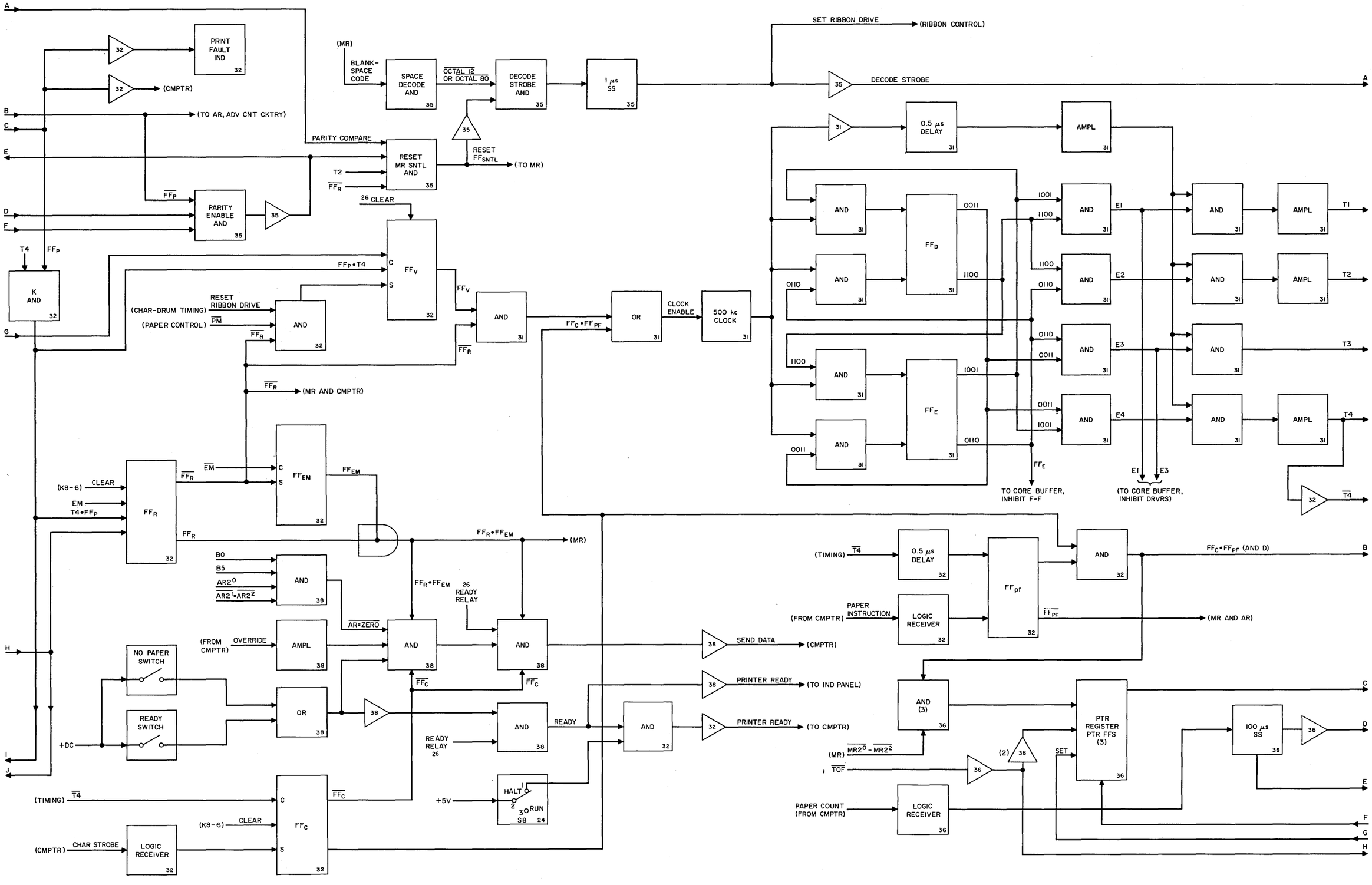


Figure 4-30. Printer Detail Block Diagram

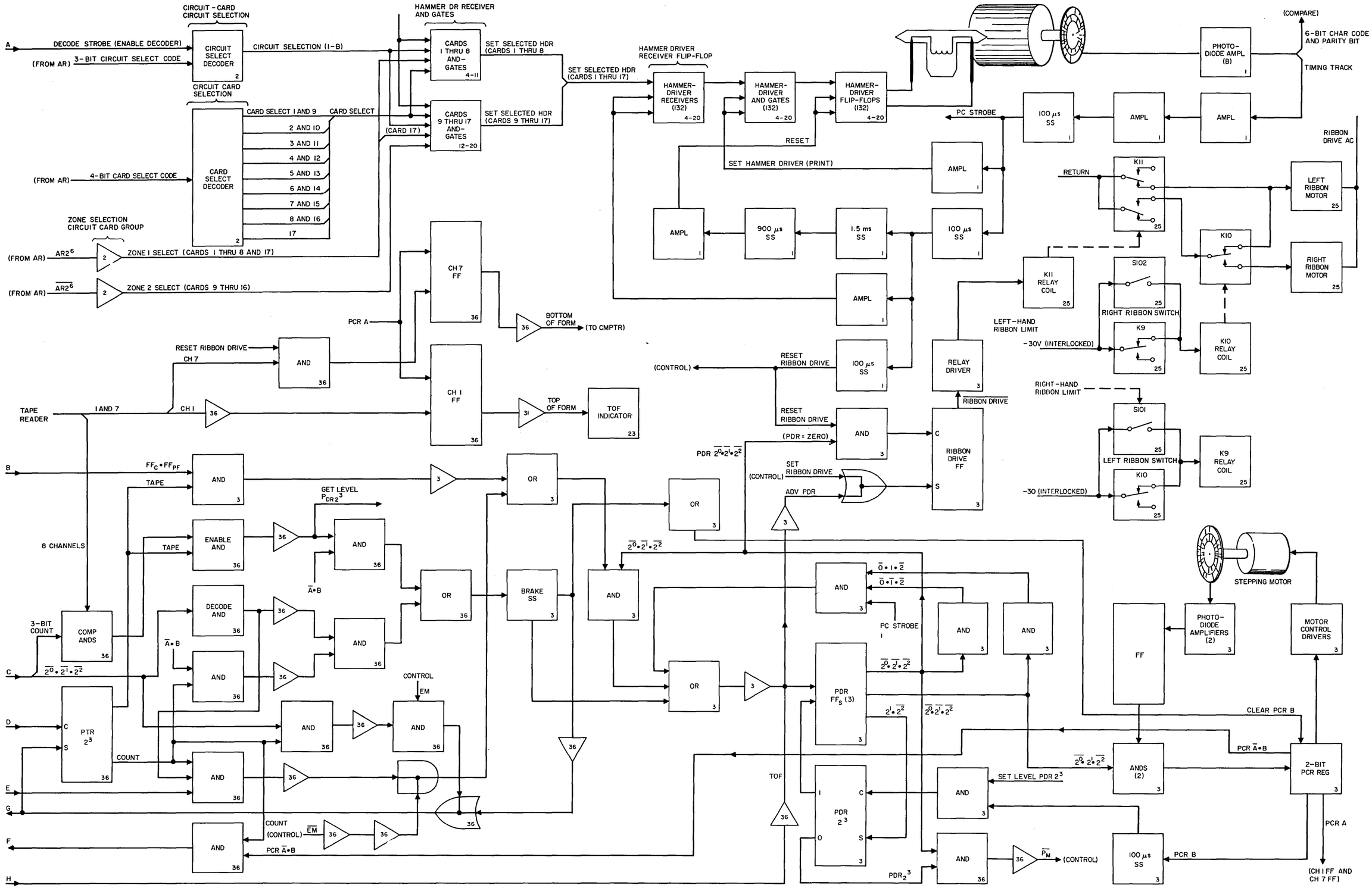


Figure 4-30. Printer Detail Block Diagram

SECTION V

MAINTENANCE

5-1. INTRODUCTION

5-2. This section contains maintenance and repair information for the printer. Recommended test equipment, replacement procedures, adjustment procedures, preventive maintenance information, and a list of suggested spares is also provided.

5-3. TEST EQUIPMENT AND SPECIAL TOOLS

5-4. Figure 5-1 lists recommended test equipment and special tools required to properly service the printer.

FIGURE 5-1. TEST EQUIPMENT AND SPECIAL TOOLS

NOMENCLATURE	MANUFACTURER AND PART NUMBER
Oscilloscope	Tektronix, Inc. Type 34A or 545 or equivalent
Preamplifier	Tektronix, Inc. Type CA Plug-in or equivalent
Multimeter	Triplet, Model 630-APL or equivalent
Differential DC Voltmeter	John Fluke Mfg. Company, Inc. Model 803B or equivalent
Extender Board	Data Products Corporation 201578-1
Card Puller	Data Products Corporation 200653-1
Torque Wrench Assembly	Data Products Corporation 200863-1
Hammer Bank Spacing Gauge	Data Products Corporation 200844-2
Insertion Tool, Pull Test Type	Data Products Corporation 380375-2

5-5. FUSES, CIRCUIT BREAKER, AND MAINTENANCE TEST PANEL

5-6. Fuses and Circuit Breaker

5-7. The printer is protected by four fuses and one circuit breaker, located on the frount of the electronics gate, and are accessible from the rear of the printer (see figure 5-2). F1, a 0.5A fuse, protects the -30V unregulated supply. F2, a 1.0A fuse, protects the +6V unregulated supply. F3, a 10A fuse, protects the +20V and -20V power supply. F4, a 10A fuse protects the -30V power supply. CB1, a 20A circuit breaker, is connected in series with the primary power input to the breaker.

CAUTION

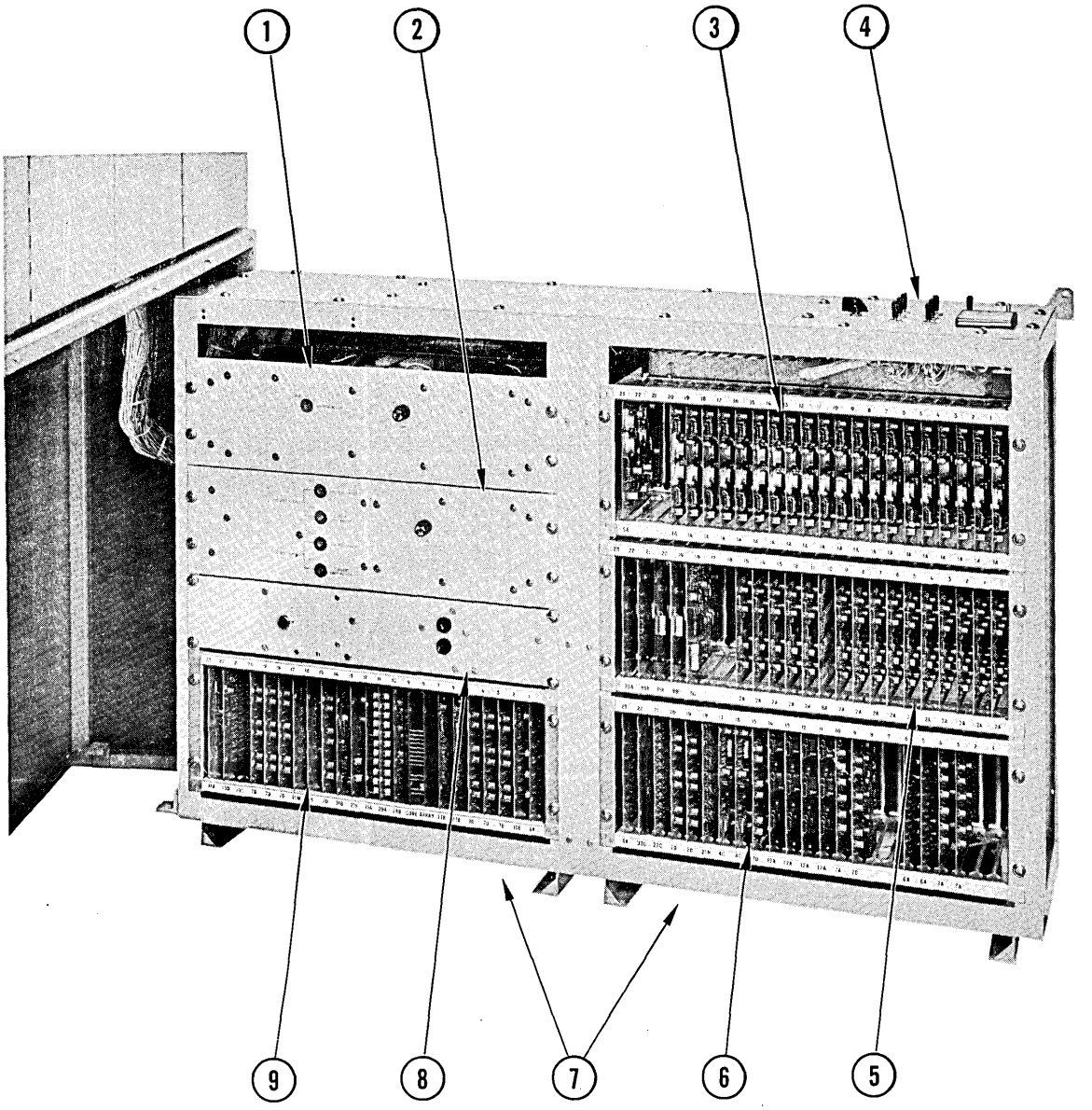
REPLACEMENT FUSES MUST BE FAST BLOW

5-8. MAINTENANCE TEST PANEL

5-9. The following maintenance controls and indicators are located on the MAINTENANCE TEST PANEL on top of the electronics gate (see figure 5-3).

(a) The HAMMER INHIBIT switch is connected to a sequencing relay that controls the -15 volts to the hammer drivers. Setting this switch to HALT interrupts the -15 volts, thus disabling the hammer drivers; this also disables the Printer Ready signal to the external equipment.

(b) The voltmeter provides an indication of the magnitude of the supply voltages used in the printer. The voltage applied to the meter is selected by the VOLTAGE SELECT rotary switch.



1. -30 Volt Power Supply
2. ±20 Volt Power Supply
3. Card Cage A
4. Maintenance Test Panel
5. Card Cage B
6. Card Cage C
7. Blower-Filter Locations
8. +6V and -30V Unregulated Power Supplies
9. Card Cage D

Figure 5-2 Electronics Gate (Front View)

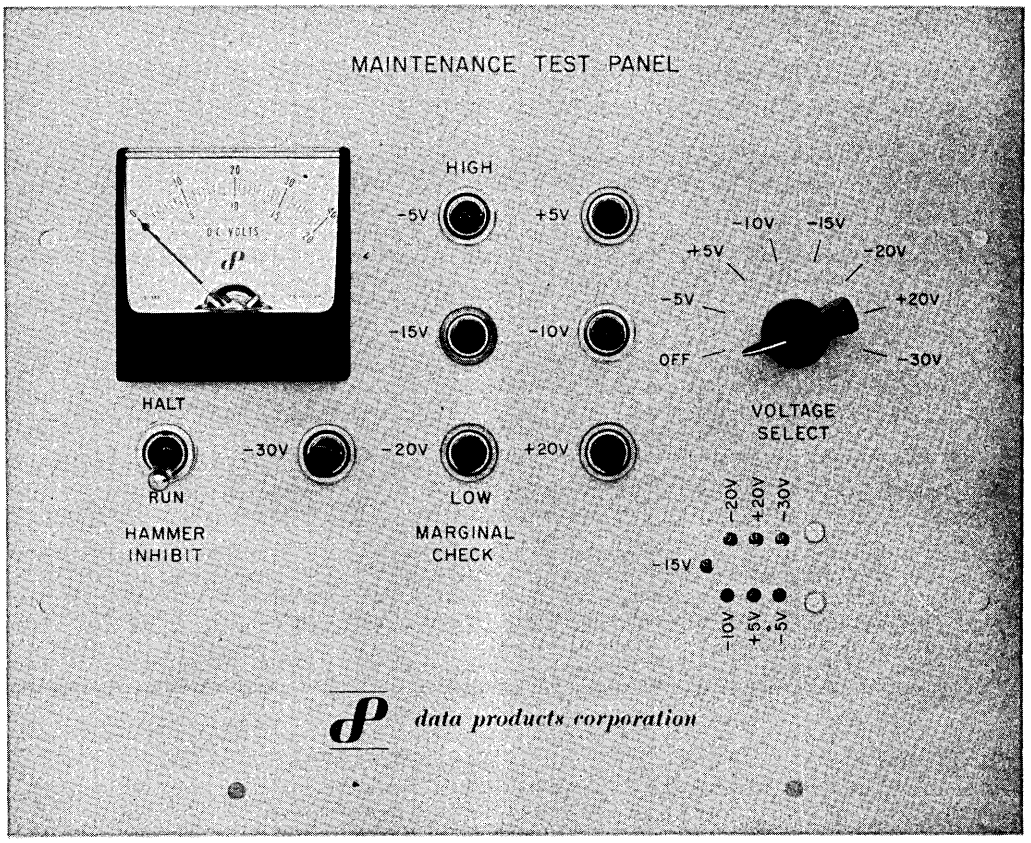


Figure 5-3. Maintenance Control Panel

(c) The seven MARGINAL CHECK toggle switches located beside the voltmeter provide margin-voltage testing of the printer. Setting one of the switches to HIGH causes the related supply voltage to increase its numeric value by five percent. Setting the switch to LOW causes the voltage to decrease its numeric value by five percent.

(d) The screwdriver adjustments located below the VOLTAGE SELECT rotary switch are used to adjust the voltmeter indication and do not affect the actual value of the supply voltages.

5-10. PREVENTIVE MAINTENANCE

5-11. Daily, weekly, monthly, and semi-annual preventive maintenance checks are provided in the following paragraphs, (5-12 through 5-15).

5-12. The following checks should be performed daily:

(a) Using a test program, print every character in every position while making margin check of each voltage. The test program should be run once with all MARGINAL CHECK switches set to HIGH and once will all the switches set to LOW.

(b) Check character-code code-wheel phasing (refer to paragraph 5-40).

5-13. The following checks should be performed weekly:

(a) Clean character drum with trichloroethylene or equivalent.

(b) Clean both code wheels and both lamps with a piece of cotton or soft cloth.

(c) Check sense amplifier discrimination level. Refer to paragraph 5-41.

(d) Check tractor alignment. Ensure that the two upper and the two lower tractors are in phase with each other. Ensure that the lower tractors are in phase with the upper tractors. Refer to paragraph 5-42.

(e) Check speed of paper feed. Continually feed paper making sure that the paper is moving 20 to 25 inches per second. (refer to paragraph 5-43 if speed is incorrect). Then run a test pattern printing characters in all positions and check the registration of each line. If registration is poor (indicating that the paper is not stopping properly), check the brake single-shot setting (C14-400) and adjust for best registration (approximately 8.5 to 9.0 ms).

5-14. The following checks should be performed monthly:

(a) Check output of photo-diodes in the paper-feed circuitry. Refer to paragraph 5-43.

(b) Check all internal timing (multivibrator settings). Refer to paragraph 5-44.

(c) Check output of photo-diodes on the character-code code wheel. Outputs should be from 3 to 12V. If not, adjust lamp so they are. If this doesn't help, replace the defective diodes.

(d) Check electronics gate air filter; if clogged replace (refer to figure 5-23).

5-15. The following checks should be performed semi-annually:

(a) Check the distance between the drum and hammer bank. It should be set for 0.085 inches. Refer to paragraph 5-45.

(b) Check all back-stop adjustments (hammer alignment) and adjust if necessary. Refer to paragraph 5-49.

(c) Check paper-drive belt tension (refer to paragraph 5-50). Make sure that belt is not cracking or deteriorating.

(d) Check tractors by disconnecting the belt and rotating by hand to make sure they are not binding.

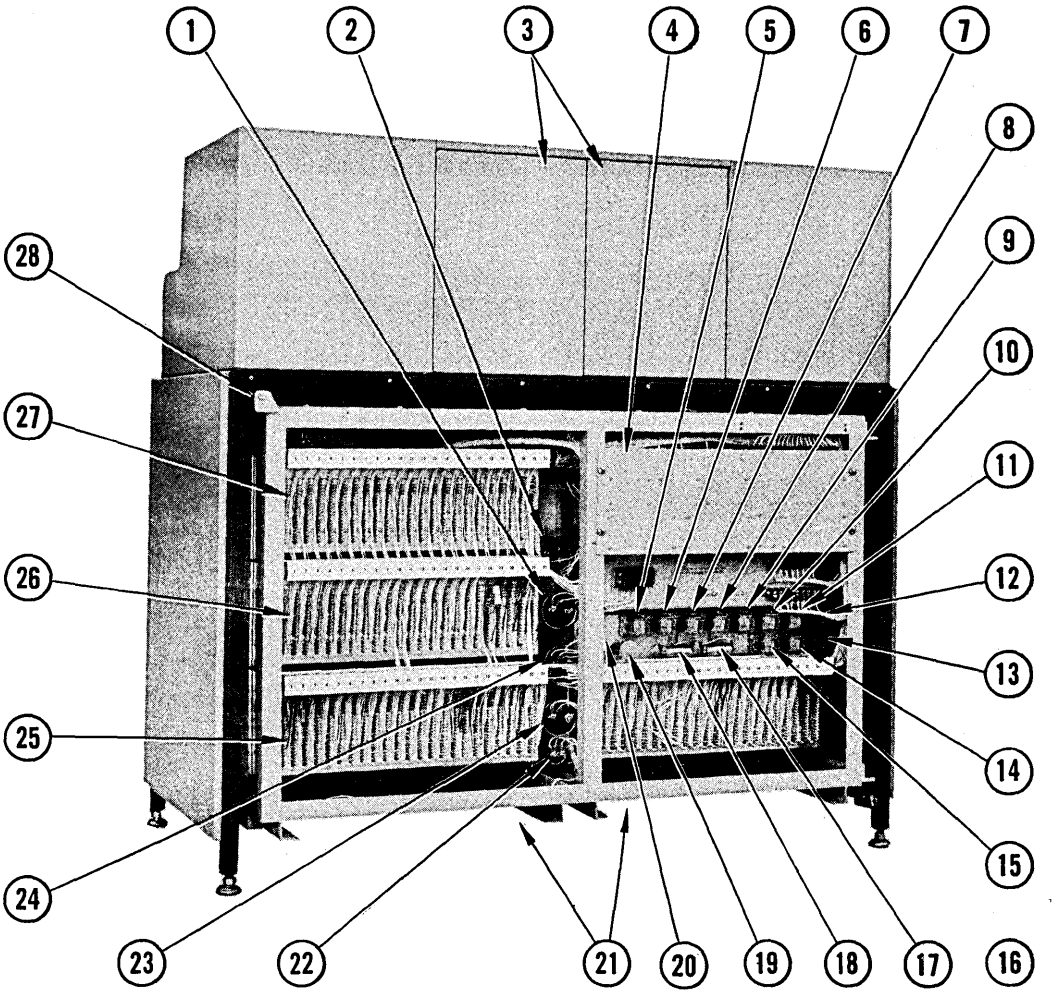
5-16. INSPECTION

5-17. The printer should be inspected for mechanical defects before employing more advanced trouble-shooting procedures. Make sure that nuts and bolts are tight, that the unit is not physically damaged, and that no wires have been torn accidentally from the equipment. Ensure that electrical connectors and printer-circuit cards are firmly in their receptacles.

5-18. PRINTED-CIRCUIT CARDS

CAUTION

1. NEVER REMOVE OR INSERT PRINTED-CIRCUIT CARDS WITHOUT FIRST MAKING CERTAIN THAT THE POWER IS OFF. FAILURE TO DO THIS MAY RESULT IN DAMAGE TO THE INSERTED CARD OR TO OTHER CARDS IN THE PRINTER.
2. THE PRINTED-CIRCUIT-CARD SOCKETS ARE NOT KEYED, SO IT IS POSSIBLE TO INSERT A PRINTED-CIRCUIT CARD IN THE WRONG SLOT. USE CONSTANT CARE TO AVOID THIS (SEE LOGIC DRAWING NO. 41). IF THE CARD IS IN THE WRONG SLOT DAMAGE MAY RESULT AND THE SYSTEM WILL NOT OPERATE. ASCERTAIN THAT ALL CARDS ARE FIRMLY SEATED IN THEIR RECEPTACLES.



1. Capacitor C32
2. Capacitor C31
3. Door Pressure Points
4. Motor-Driver Panel
5. Relay K1
6. Relay K2
7. Relay K3
8. Relay K4
9. Relay K5
10. Relay K6
11. Relay K7
12. Relay K8
13. Relay K11
14. Relay K10
15. Relay K9
16. Card Cage D
17. Capacitor C10
18. Capacitor C11
19. Capacitor C2
20. Capacitor C1
21. Blower Filter Locations
22. Capacitor C30
23. Capacitor C34
24. Capacitor C33
25. Card Cage C
26. Card Cage B
27. Card Cage A
28. Electronics Gate Fastening Bolt

Figure 5-4. Printer Rear View (Skin Removed)

5-19. The following paragraphs provide location, handling, cleaning, and repair information for the printer printed-circuit cards.

5-20. Card Locations. See figures 5-2 and 5-4 for position of card cages. Refer to logic drawing no. 41, section VI, for card locations. Card type number and assembly-drawing revision letter is stamped on each card. Figure 5-5 contains cross-reference information for all cards used in the printer.

5-21. Card Handling Procedures. The printed-circuit cards are designed to operate on very low power levels. Consequently their contacts are sensitive to dirt, dust, moisture, and corrosion. They should not be inserted into the unit without cleaning (refer to the following paragraph, 5-22).

5-22. Card Cleaning. The printed-circuit cards are cleaned in the following manner:

(a) Clean between the contacts with a soft brush moistened in trichlorethylene or equivalent.

(b) Ensure that no metal particles are lodged between the contacts.

Figure 5-5. PRINTED-CIRCUIT CARD, NAME AND TYPE NUMBER

NOMENCLATURE	CARD TYPE NUMBER	SCHEMATIC DRAWING NO.	ASSEMBLY DRAWING NO.
Hammer Driver	1 A	200182	200185
Hammer Driver Receiver	2 A	200190	200193

FIGURE 5-5. PRINTED-CIRCUIT CARD, NAME AND TYPE NUMBER (cont'd.)

NOMEMCLATURE	CARD TYPE NUMBER	SCHEMATIC DRAWING NO.	ASSEMBLY DRAWING NO.
Paper Feed Control	3 D	202071	202074
Photo Diode Amplifier	4 C	202075	202078
Hammer Driver Power Amplifier	5 A	200173	200176
NOR Gate	6 A	200232	200235
Flip Flop	7 A	200194	200197
Flip Flop	7 D	200911	200914
Decode	8 A	200224	200227
Decode	8 E	201374	201377
Comparator	10 E	201410	201413
Output Driver	11 A	200220	200223
Multivibrator	12 A	200240	200243
Logic Receiver	13 D	201572	201575
Logic Driver	21 M	201405	201408
Logic Driver	21 N	201454	201457
Logic Driver	21 P	201478	201481
Logic Driver	21 V	202496	202497
NAN Gate	22 C	201438	201441
Read Amplifier	27 B	201686	201689
Inhibit Driver	28 B	201469	201472
Selection Switch	29 A	201329	201332
Clock/Timing	31 B	201419	201422
Delay Line	33 C	201485	201488

Figure 5-5. PRINTED-CIRCUIT CARD, NAME AND TYPE NUMBER (cont'd.)

NOMENCLATURE	CARD TYPE NUMBER	SCHEMATIC DRAWING NO.	ASSEMBLY DRAWING NO.
-5V Regulator	99 A	200418	200421
+5V Regulator	99 B	200255	200258
-10V Regulator	99 D	200422	200425
-15V Regulator	99 E	200426	200429

5-23. Card Repair Procedures. The printed-circuit cards can be serviced using conventional shop practices. Values of circuit components and voltages applied to the cards can be found in the schematic diagrams of Section VI of this manual.

CAUTION

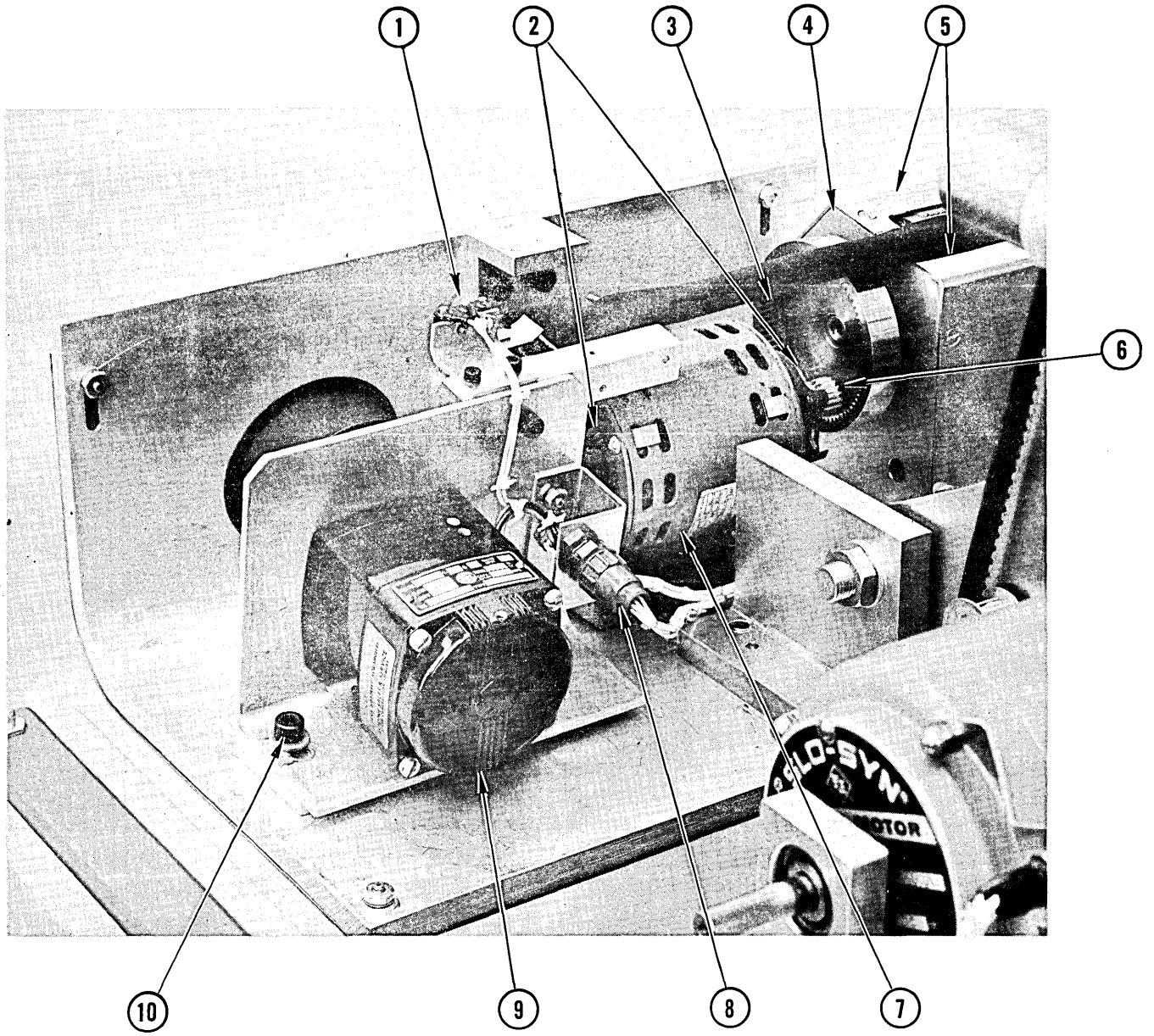
When replacing transistors replace transistor so that tab on case is aligned with tab on printed circuit. Observe polarity markings on diodes and capacitors. Replacing components improperly could result in damage to the card or to other circuits.

5-24. REPLACEMENT PROCEDURES

5-25. Replacement procedures are provided by listing the removal procedures for the applicable items. An item that has been removed should be replaced by the reverse sequence listed in the instructions unless otherwise specified. The applicable adjustment procedures should be performed whenever an item has been replaced.

5-26. CHARACTER DRUM REPLACEMENT. The character drum replacement procedure is as follows:

(a) Open drum-gate assembly to lowest position.
(b) Loosen and lift ribbon clear of character-drum assembly.
(c) Remove clamp (2, figure 5-6) at each end of drum motor.
(d) Move drum motor away from character drum until spur gear (6, figure 5-6) is clear of internal gear (3, figure 5-6).



1. Right-Hand Ribbon Switch
2. Drum-Motor Clamps
3. Internal Gear
4. Upper Bearing Cap (one at each end of character drum)
5. Shrouds
6. Spur Gear
7. Drum Motor
8. Connector P3
9. Right-Hand Ribbon Motor
10. Ribbon-Drive-Bracket Clamp Screw

Figure 5-6. Drum-Motor and Ribbon-Drive Assembly

(e) Remove two shrouds (5, figure 5-6 and 1, figure 5-7) from over character drum.

(f) Remove two screws holding each upper bearing cap (4, figure 5-6).

(g) Remove one screw (3, figure 5-7) holding upper-bearing cap to diode mounting plate at left end of character drum.

(h) Remove both upper bearing caps.

CAUTION

DRUM GATE MUST BE HELD SECURELY IN OPEN POSITION WHILE REMOVING CHARACTER DRUM TO PREVENT SPRING FROM RETURNING DRUM GATE TO CLOSED POSITION.

(i) The character drum with code wheel attached can now be lifted straight up and clear of drum-gate assembly.

5-27. HAMMER REPLACEMENT. Hammer replacement procedure is as follows (removal procedure is listed in steps a thru g; replacement procedure is listed in steps h thru k):

Removal Procedure

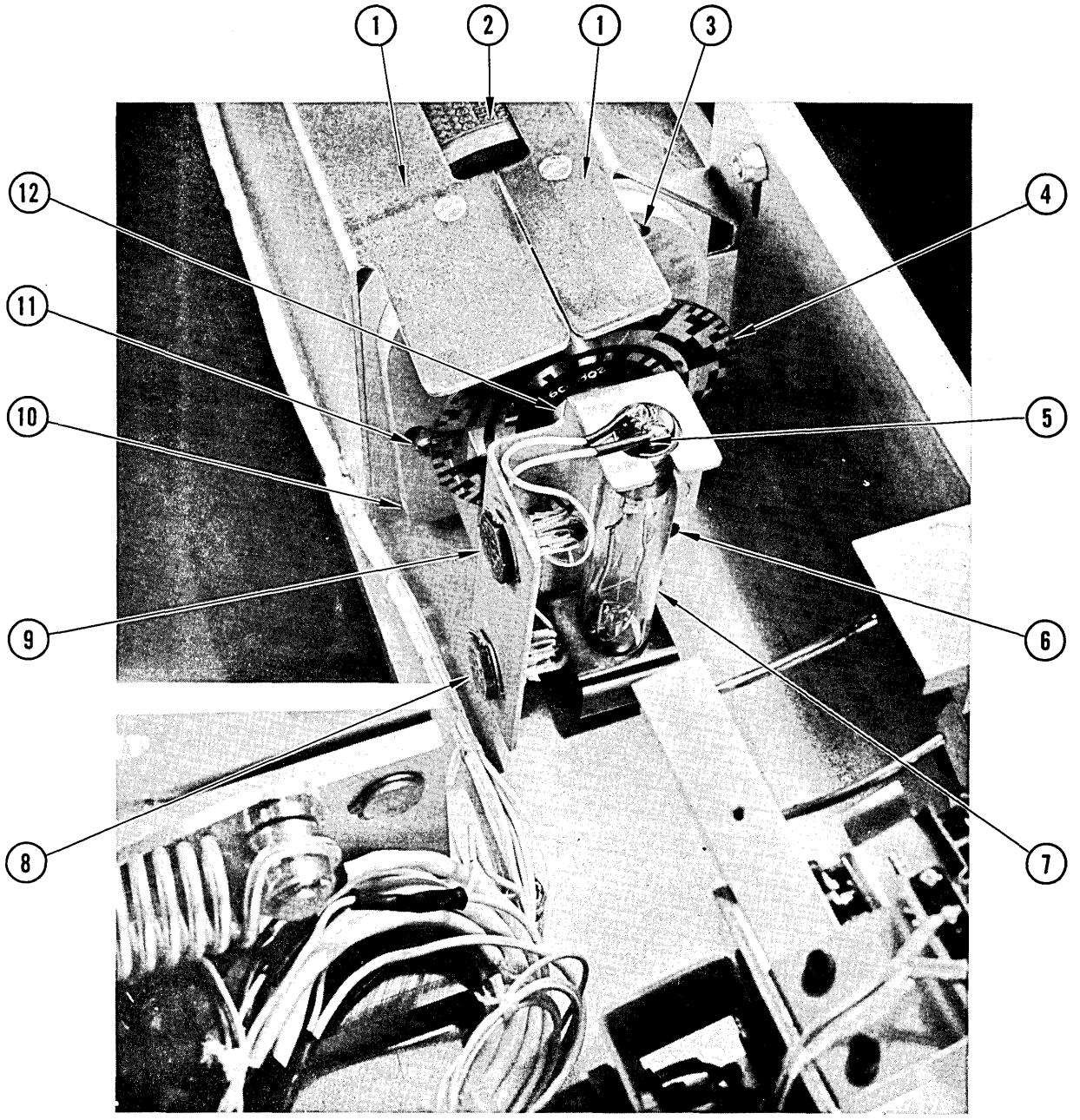
(a) Open drum-gate assembly to lowest position.

(b) Remove two upper screws on each connecting plate (6, figure 5-8).

(c) Move upper paper tractors to their maximum width.

(d) Swing front of upper hammer-bank assembly up and back.

(e) Remove two hammer contact-pins, one on each side of hammer bank connector (5, figure 5-8), from hammer-bank connector assembly (1, figure 5-8).



1. Character-Drum Shrouds
2. Character Drum
3. Clamp Screw (1 of 3)
4. Character Code Wheel
5. Lamp Lead Wires
6. Holding Screw
7. Lamp
8. Connector J6 (P6 disconnected)
9. Connector J5 (P5 disconnected)
10. Fine Phasing Adjustment
11. Clamp Screw (1 of 3)
12. Code-Wheel Holding Nut (not shown)

Figure 5-7. Character-Code Photo-Diode Assembly

1. Upper Connector-Assembly
2. Hammer-Leg Set Screw
3. Ground Connector
4. -30 Volt Connector
5. Hammer Contact-Pin (3 shown)
6. Connecting Plates

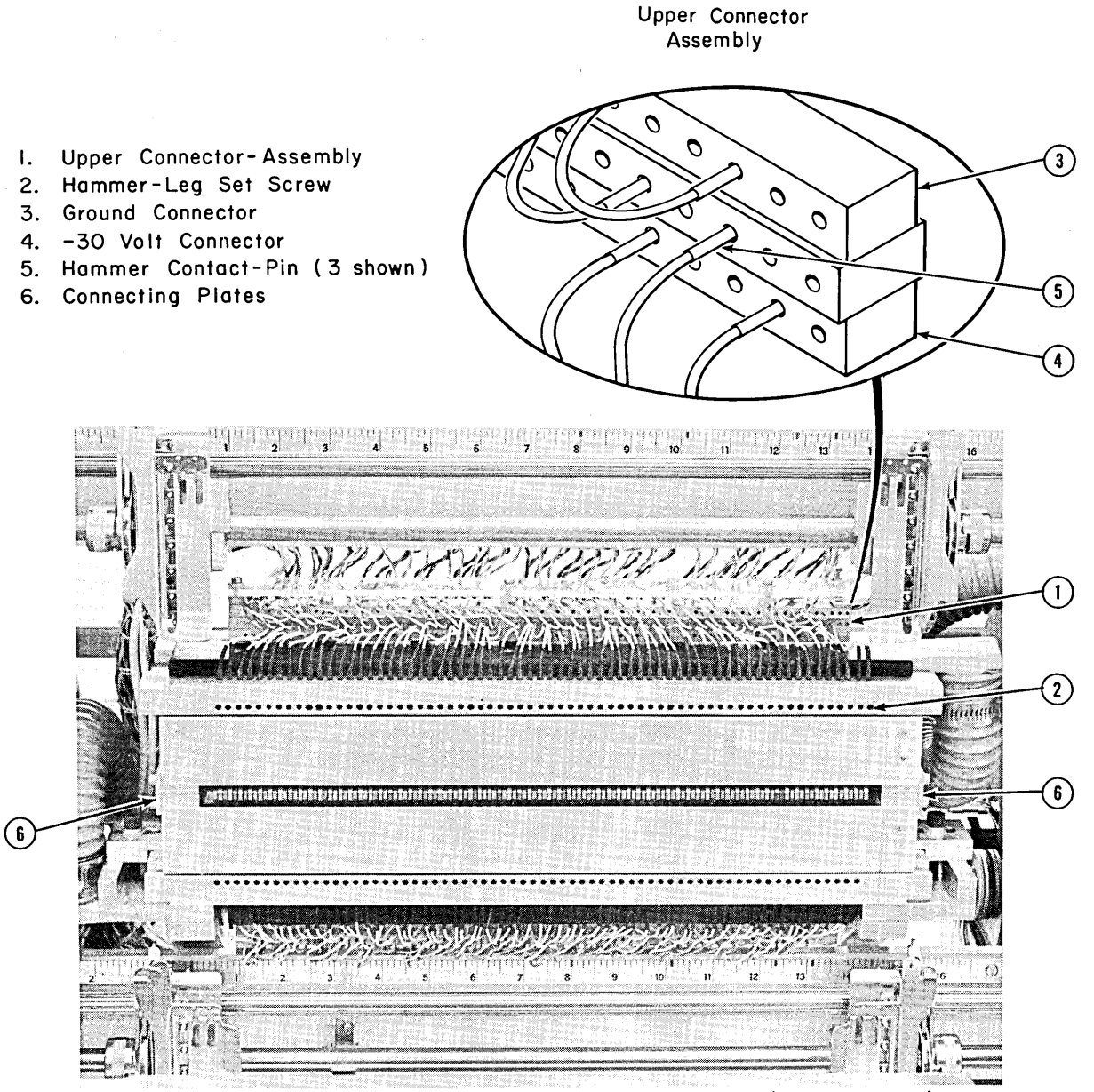


Figure 5-8. Hammer-Bank Assembly (Front View)

(f) Loosen one set screw (2, figure 5-8) holding each hammer leg of hammer being removed.

(g) Using torque wrench assembly (figure 5-1), remove hammer (the two wires and contact pins will be pulled through hammer leg mounting holes).

Replacement Procedure

(h) Insert new hammer into position.

(i) Tighten two set screws (step f) to 75-to-80 inch-ounces using torque wrench assembly listed in figure 5-1.

(j) Loosen set screws and re-tighten to 30-to-35 inch-ounces.

(k) Paint end of set screws (see following note) with STA-TITE (or equivalent) and let set for 4-to-8 hours before operating.

NOTE

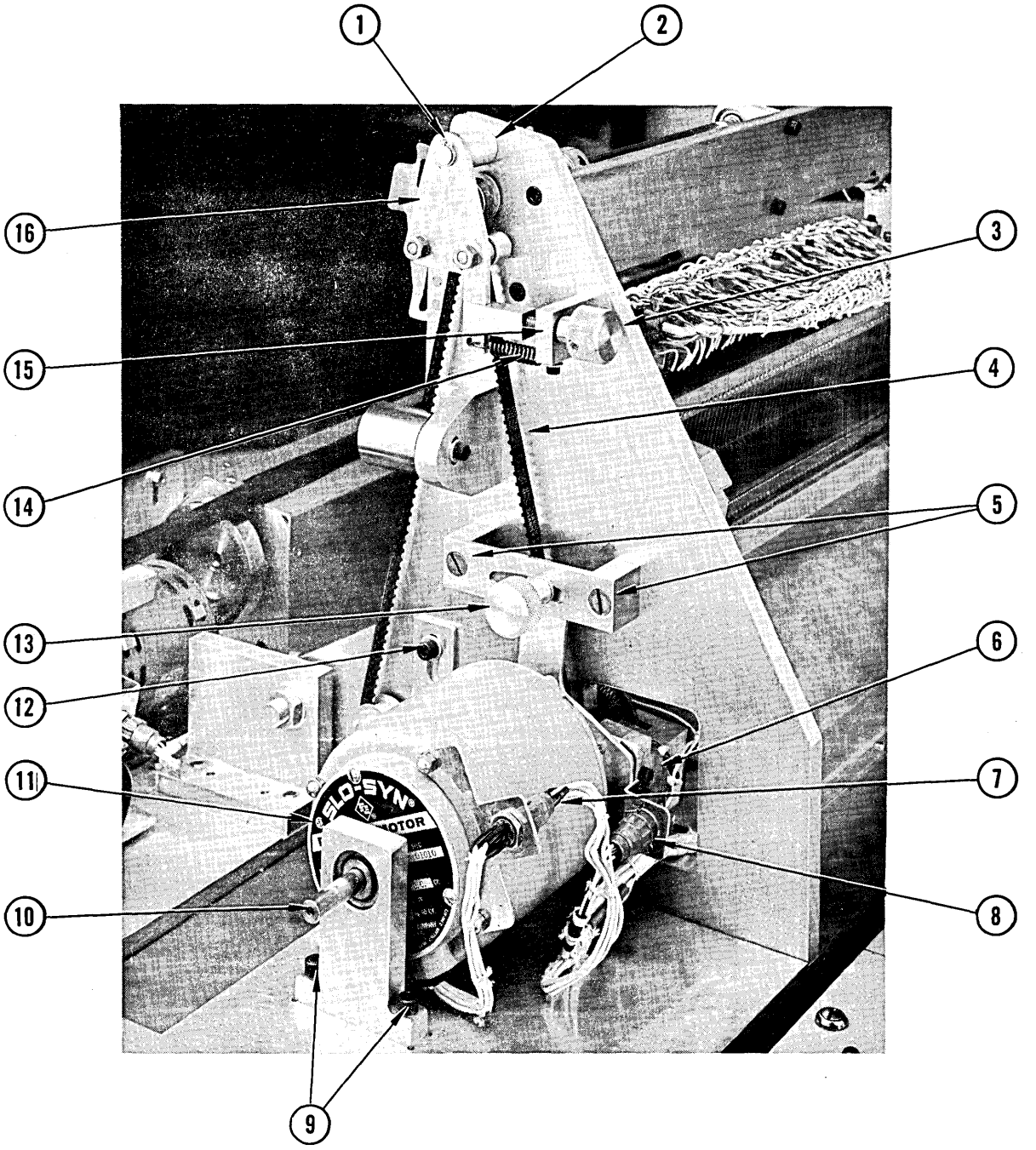
THE PRINTER CAN BE OPERATED IMMEDIATELY AFTER REPLACING HAMMER WITHOUT PERFORMING STEP k. IF THIS IS DONE, REPEAT STEPS j AND k WHEN PRINTER OPERATION IS COMPLETE.

5-28. PAPER-DRIVE BELT REPLACEMENT (Serial numbers P1 through P21). The paper-drive belt replacement procedure for printer serial numbers P1 through P21 is as follows:

(a) Remove stepping photo-diode assembly (paragraph 5-33).

(b) Remove stepping code-wheel assembly (paragraph 5-34).

(c) Loosen belt by removing idler-bearing bolts (12, figure 5-9) and sliding idler bearing down.



1. C Ring
2. Hinge Pin
3. Vertical Tension Adjust
4. Paper-Drive Belt
5. Positioning-Bracket Screws
6. Photo-Diode-Assembly Holding Screws
7. Connector P8
8. Connector P7
9. Stepping-Motor-Bracket Screws
10. Stepping-Motor Shaft
11. Stepping Motor
12. Idler-Bearing Bolts
13. Vertical Position Control
14. Spring
15. Vertical-Tension Bracket
16. Tension Plate

Figure 5-9. Paper-Feed Assembly, Right End (Serial Numbers P1 thru P21)

(d) Remove positioning-bracket screws (5, figure 5-9).

(e) Remove motor-bracket screws (9, figure 5-9).

(f) Move the motor and motor-bracket together, away from paper-feed assembly; this will remove the motor-shaft bearing (code wheel end) from its mount. (The lower portion of the belt can now be removed from obstructions).

(g) Loosen vertical-tension bracket (15, figure 5-9) by removing two bolts.

(h) Rotate tension plate (16, figure 5-9) forward and remove belt.

5-29. PAPER-DRIVE BELT REPLACEMENT (Serial numbers P22 and on). The paper-drive belt replacement procedure for printer serial numbers P22 and on is as follows:

(a) Remove stepping photo-diode assembly (paragraph 5-33).

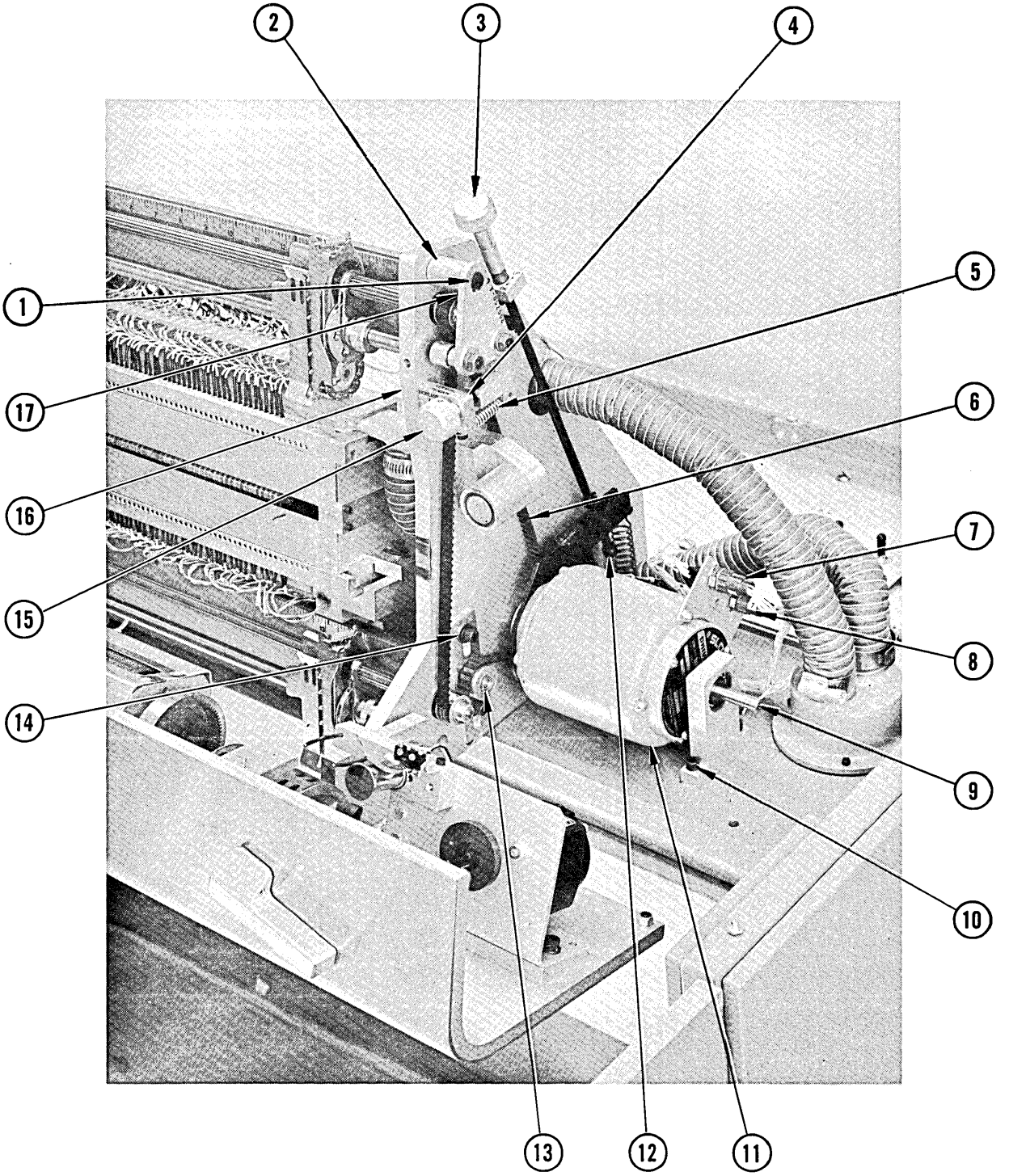
(b) Remove stepping code-wheel assembly (paragraph 5-34).

(c) Loosen belt by removing idler-bearing bolts (14, figure 5-10) and sliding idler bearing down.

(d) Remove shaft stop (12, figure 5-10); rotate VERTICAL POSITION control until vertical positioning shaft is clear of bracket on motor.

(e) Remove motor-bracket screws (10, figure 5-10).

(f) Move the motor and motor-bracket together, away from paper-feed assembly; this will remove the motor-shaft bearing (code wheel end) from its mount. (The lower portion of the belt can now be removed from obstructions).



1. C Ring
2. Hinge Pin
3. VERTICAL POSITION Control
4. Vertical-Tension Bracket
5. Spring
6. Paper-Drive Belt
7. Connector P8
8. Connector P7
9. Stepping-Motor Shaft
10. Stepping-Motor-Bracket Screws
11. Stepping Motor
12. Vertical-Positioning-Shaft Stop
13. Idler Bearing
14. Idler-Bearing Bolts
15. VERTICAL TENSION Adjust
16. Vertical-Tension-Bracket Bolts (not shown)
17. Tension Plate

Figure 5-10. Paper-Feed Assembly, Right End (Serial Numbers P22 and On)

(g) Loosen vertical-tension bracket (4, figure 5-10) by removing two bolts (16, figure 5-10; and 4, figure 5-9).

(h) Rotate tension plate (17, figure 5-10) forward and remove belt.

5-30. TRACTOR-ADJUST BELT REPLACEMENT. The procedure for the tractor-adjust belt replacement is as follows:

(a) Remove two screws from top bracket and two from bottom bracket (3 and 6, figure 5-11 and 5-12).

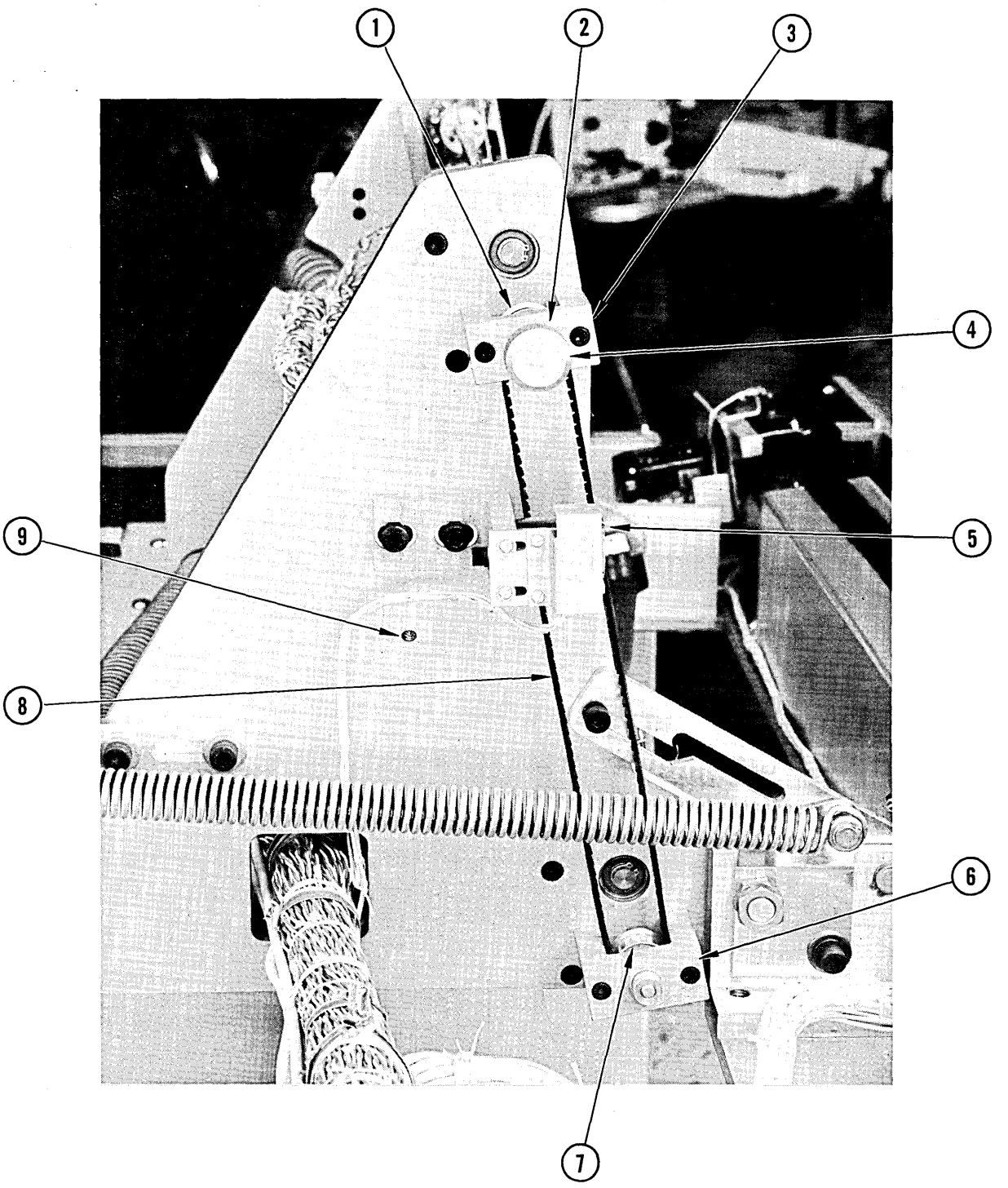
(b) Rotate HORIZONTAL POSITION control (10, figure 5-11; and 4, figure 5-14) counter-clockwise until top and bottom tractor-shaft end assemblies (1 and 7, figures 5-11 and 5-12) are clear of tractor shafts.

(c) Remove and replace tractor-adjust belt (8, figures 5-11 and 5-12).

(d) Hold both tractor-shaft end assemblies against tractor shafts and rotate HORIZONTAL POSITION control clockwise so that both assemblies are threaded on shaft ends by the same amount.

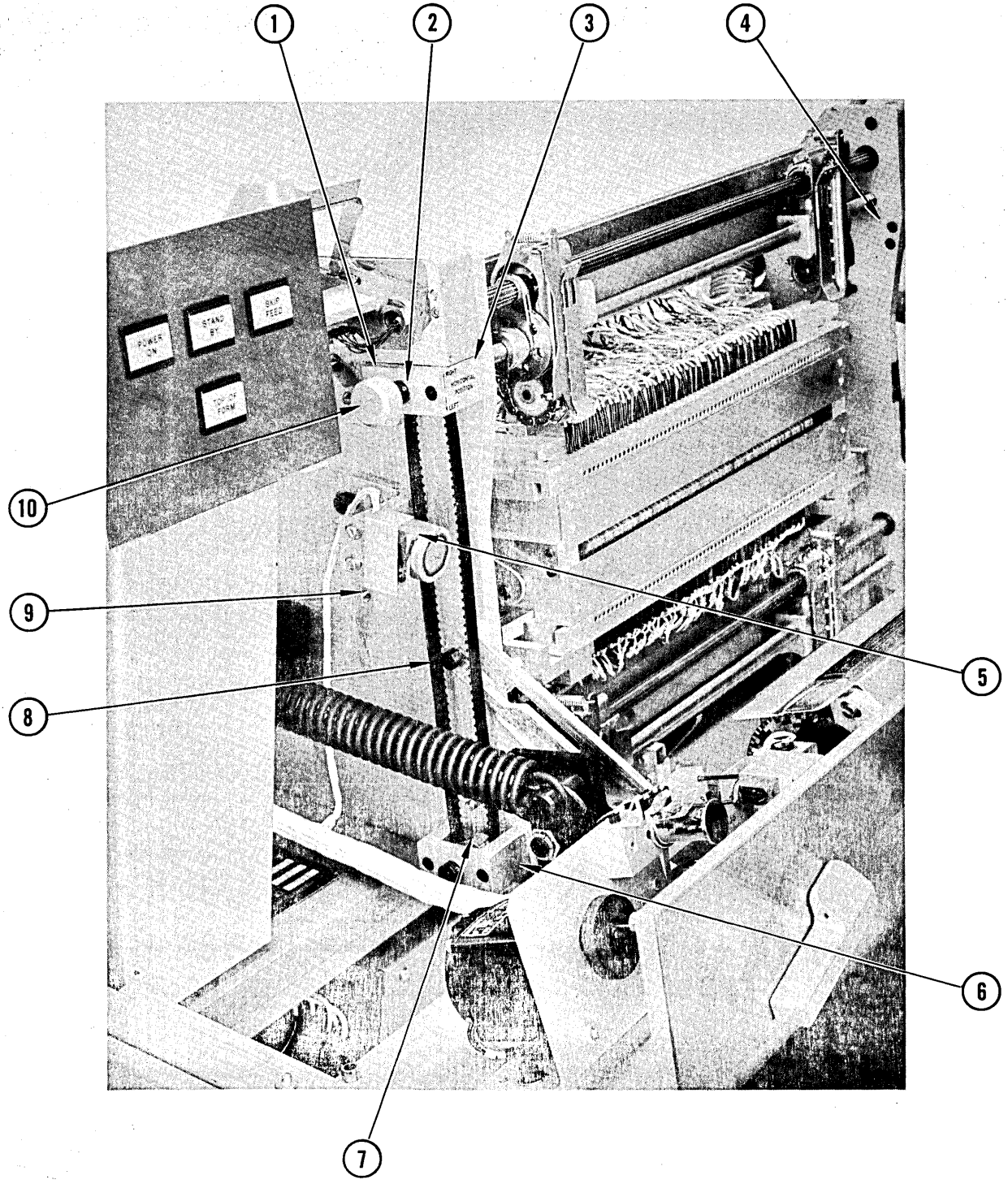
(e) Rotate HORIZONTAL POSITION control clockwise until top and bottom end assemblies are all the way in.

(f) If both end assemblies are not all the way in, loosen set screw or remove pin (2, figure 5-11 and 5-12) and rotate bottom end assembly fully clockwise by rotating belt. Slide upper pulley flush against inside of upper bracket and tighten set screw (or replace pin).



1. Top Tractor-Shaft End Assembly
2. Set Screw (not shown)
3. Top Bracket
4. HORIZONTAL POSITION Control
5. Drum-Open Switch
6. Bottom Bracket
7. Bottom Tractor-Shaft End Assembly
8. Tractor-Adjust Belt
9. Shipping-Bolt Location

Figure 5-11. Paper-Feed Assembly, Left End (Serial Numbers P1 thru P21)



1. Top Tractor-Shaft End Assembly
2. Pin
3. Top Bracket
4. Vertical-Tension-Bracket Bolts
5. Drum-Open Switch
6. Bottom Bracket
7. Bottom Tractor-Shaft End Assembly
8. Tractor-Adjust Belt
9. Shipping-Bolt Location
10. HORIZONTAL POSITION Control

Figure 5-12. Paper-Feed Assembly, Left End (Serial Numbers P22 and On)

5-31. RIBBON REPLACEMENT. Refer to Section III for ribbon replacement procedure.

5-32. STEPPING-CODE LAMP REPLACEMENT. The stepping-code lamp replacement procedure is as follows:

(a) Remove and replace stepping-code lamp.

(b) Refer to paragraph 5-43 (b) to align stepping-code lamp after replacement.

5-33. STEPPING PHOTO-DIODE REPLACEMENT. The stepping photo-diode is replaced as follows:

(a) Remove connector P7 (8, figures 5-9 and 5-10).

(b) Remove two holding screws (2, figure 5-13) while holding photo-diode assembly.

CAUTION

CARE MUST BE EXERCISED TO AVOID SCRATCHING SURFACE OF THE CODE WHEEL.

(c) Carefully slide photo-diode assembly away from code wheel and remove.

5-34. STEPPING-CODE-WHEEL ASSEMBLY REPLACEMENT. The procedure for the stepping-code-wheel assembly replacement is as follows:

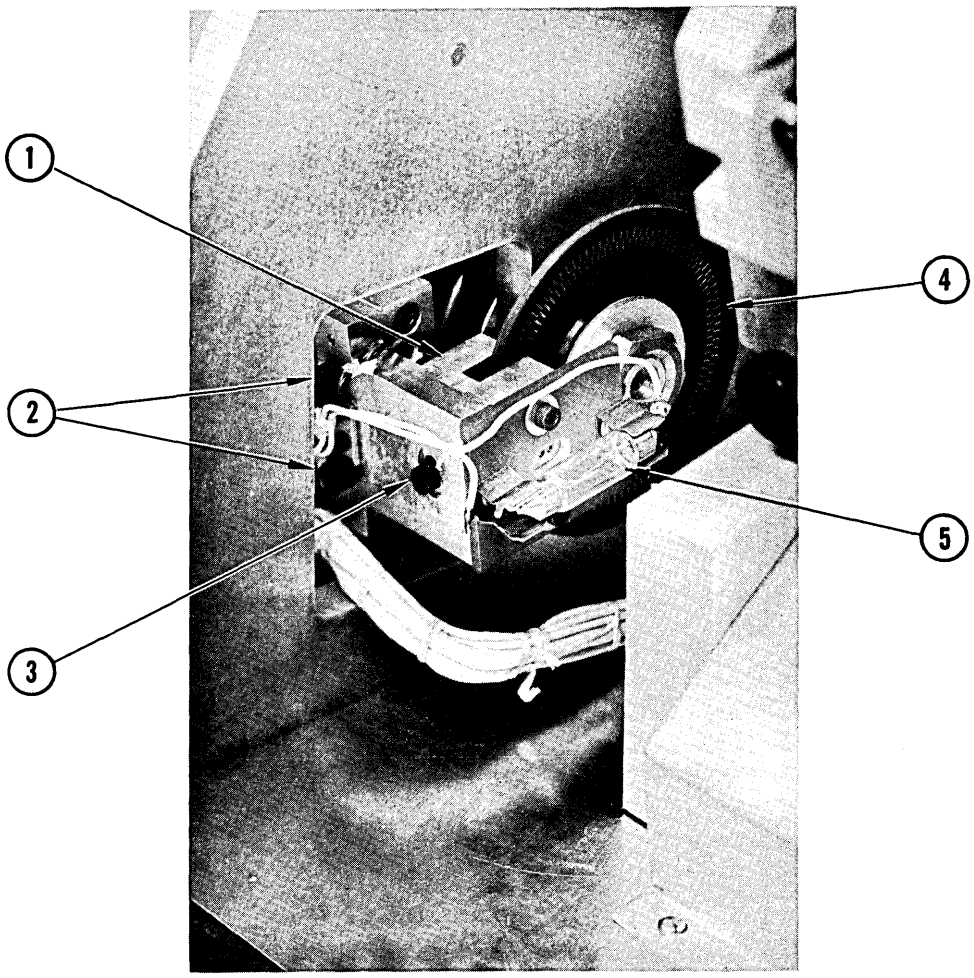
(a) Remove photo-diode assembly (refer to paragraph 5-33).

(b) Loosen two set screws (6, figure 5-14).

(c) Remove stepping-code-wheel assembly (8, figure 5-14).

CAUTION

DO NOT DISASSEMBLE STEPPING-CODE-WHEEL ASSEMBLY. IF CODE WHEEL IS DISASSEMBLED, IT MUST BE ALIGNED WITH STEPPING MOTOR AT THE FACTORY.



1. Photo-Diode Holder
2. Holding Screws
3. Adjusting Screw
4. Stepping Code-Wheel
5. Lamp

Figure 5-13. Stepping Photo-Diode Assembly

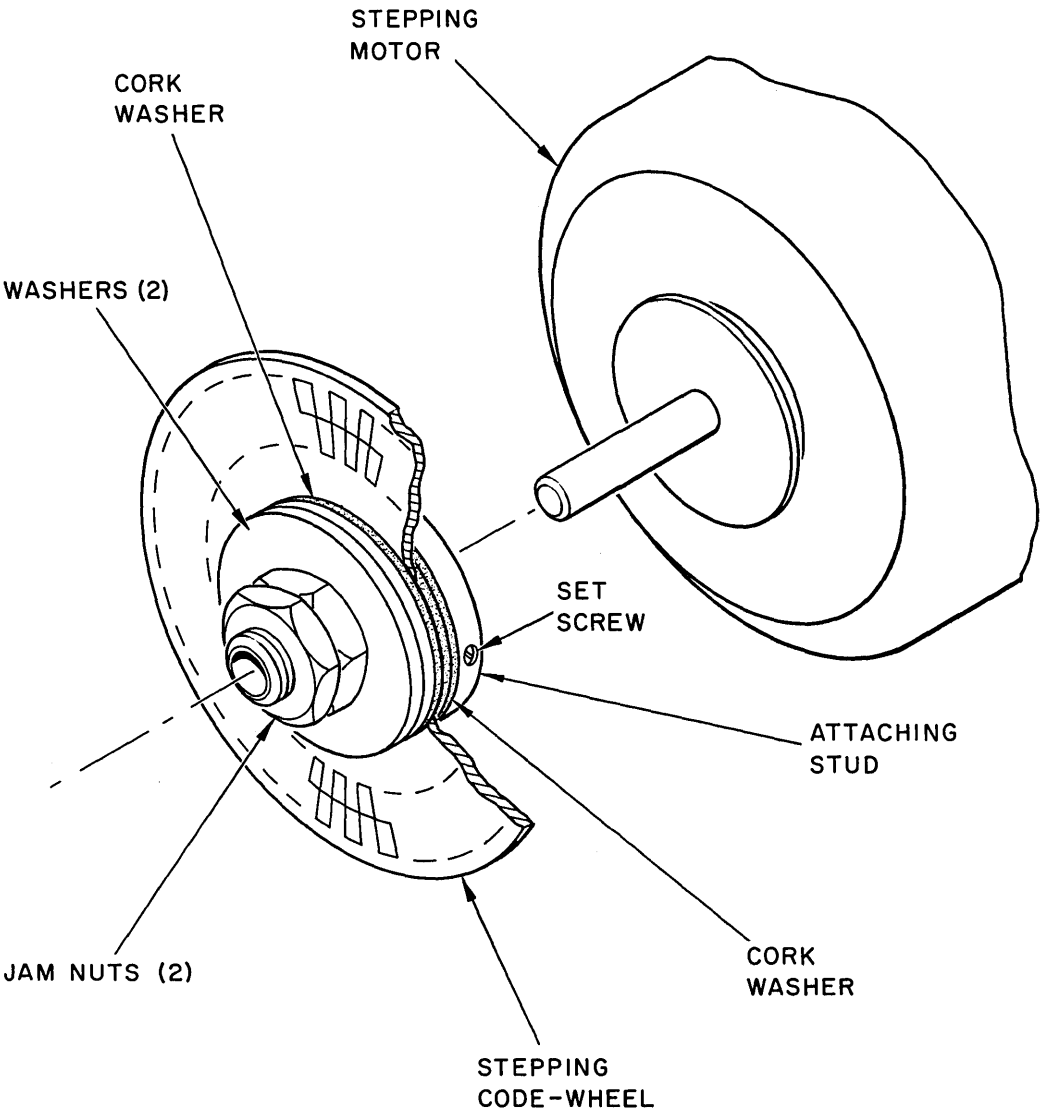


Figure 5-14. Stepping Code-Wheel Assembly

5-35. CHARACTER-CODE LAMP REPLACEMENT. The character-code lamp replacement procedure is as follows:

(a) Unsolder two wires from character-code lamp (5, figure 5-7).

(b) Remove and replace character-code lamp, and re-solder the two wires (removed in Step a).

(c) Refer to paragraph 5-40 (d) to align character-code lamp after replacement.

5-36. CHARACTER-CODE PHOTO-DIODE REPLACEMENT. The character-code photo-diode replacement procedure is as follows:

CAUTION

CARE MUST BE EXERCISED TO AVOID SCRATCHING SURFACE OF THE CODE WHEEL.

(a) Remove connectors P5 and P6 (8 and 9), figure 5-7) while holding character-code photo-diode assembly.

(b) Remove two counter-sunk holding screws (6, figure 5-7).

(c) Withdraw photo-diode assembly from recess and swing it clear of code wheel.

5-37. CHARACTER-CODE CODE WHEEL REPLACEMENT. The replacement procedure for the character-code code-wheel is as follows:

(a) Remove character drum (refer to paragraph 5-26).

(b) Remove code wheel.

(c) When replacing code wheel, rotate wheel to align proper code with a character on the character drum; and re-adjust the phasing (refer to paragraph 5-40).

5-38. ADJUSTMENT PROCEDURES

5-39. Adjustment procedures for the printer are contained in the following paragraphs. Location of the adjustments is facilitated by the referenced figures. Some of these adjustment procedures are referenced in the preventive maintenance instructions, and are the only adjustments required at periodic intervals. All other adjustments are to be made only when referenced in the replacement procedures.

5-40. CHARACTER-CODE CODE-WHEEL PHASING ADJUSTMENT. The phasing adjustment can be checked by printing one character at all addresses and observing the printed characters. Phasing is necessary if either the top or the bottom of the character does not print clearly. The procedure is as follows (steps a through e are the coarse adjustment, steps f through i are the fine adjustment).

Coarse Adjustment

(a) Loosen code-wheel holding nut (12, figure 5-7).

(b) Rotate code wheel (4, figure 5-7) to align proper code with a character on character drum (2, figure 5-7).

(c) Tighten code-wheel holding nut.

(d) Rotate lamp (7, figure 5-7) to obtain maximum negative signal at C17-22. (This is the timing track output shown on logic diagram 1 in Section VI).

(e) If additional adjustment is necessary, perform character-code code-wheel fine adjustment procedure.

Fine Adjustment

(f) Print one character at all addresses continually.

(g) Loosen three clamp screws (3, figure 5-7) and rotate fine phasing adjustment (10, figure 5-7) until character prints clearly.

(h) Tighten clamp screws.

(i) If fine phasing cannot be adjusted adequately by this method, set fine phasing adjustment to its mid-position and perform character-code code-wheel coarse adjustment procedure (steps a through e).

5-41. READ-AMPLIFIER ADJUSTMENT. All of the read-amplifier circuits on one printed-circuit card are adjusted by one control. The adjustment is made while viewing logical ONE and ZERO signals being amplified in any one of the read-amplifier circuits. The adjustment is accomplished as follows:

(a) Select on of the eight bits.

(b) Connect oscilloscope to collector of Q3 or Q4 of the read-amplifier circuit corresponding to the selected bit (circuit 100, 200, 300, or 400 on one of the 27B printed-circuit cards).

(c) Load the printer with data that will result in a series of logical ONEs and ZEROs for the selected bit.

(d) Program the printer so that the data will continually load and unload the core buffer. (During the unload cycle the data will pass through the read-amplifier).

(e) Adjust R602 so that the discrimination level (indicated by the notch in the leading edge of the waveform (figure 5-15) is midway between a minimum logical ONE and a maximum logical ZERO.

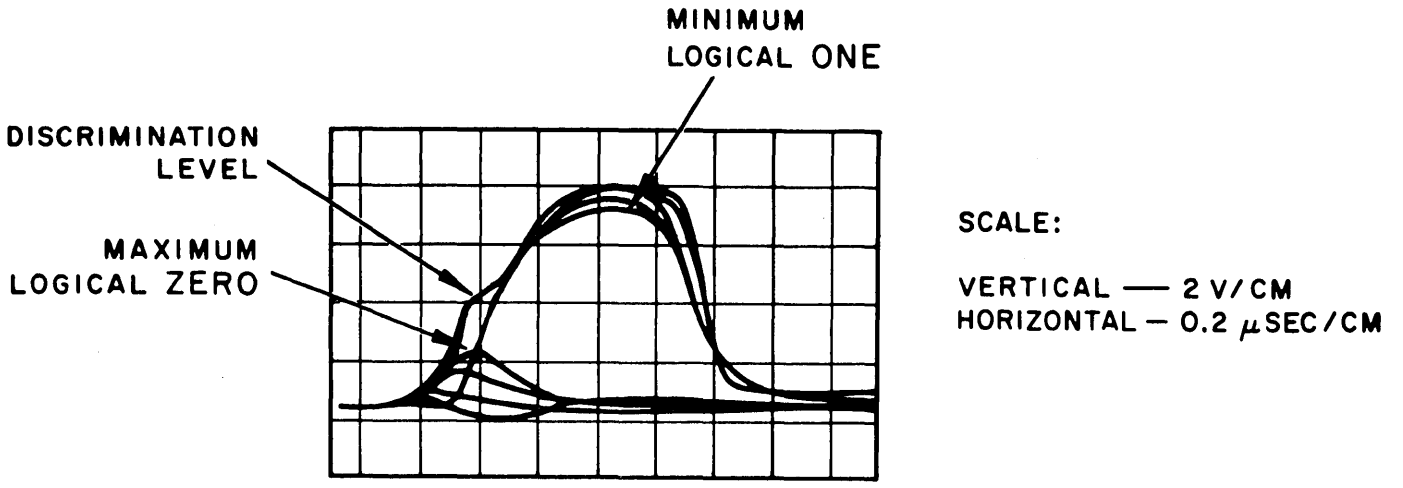


Figure 5-15. Sense-Amplifier Second-Stage-Output Waveform

5-42. TRACTOR PHASING. The four paper-drive tractors should be kept in phase in the following manner: (1) the two upper tractors aligned with each other, (2) the two lower tractors aligned with each other, and (3) the lower pair aligned with the upper pair. Two tractors on the same shaft are aligned by setting any one cog on each tractor to an identical mark on each tractor assembly. A tractor can be rotated independent of the shaft after loosening the holding screws. Tractor alignment can be checked by printing on lined or ruled paper and observing the printed-line relationship to the ruled line.

5-43. PHOTO-DIODE AMPLIFIER ADJUSTMENT. The two photo-diode amplifiers in the paper-control circuitry (C16-500 and C17-500) should be adjusted in the following manner:

(a) Disconnect stepping-motor plug P8 (7, figures 5-9 and 5-10).

(b) Measure input signal of each amplifier with oscilloscope (C16 pin 23 and C17 pin 23) while rotating stepping-motor shaft (10, figure 5-9). Signal amplitude should vary from 5 to 13 volts. Rotate stepping-motor lamp in its socket to obtain approximately equal (within 2 volts) maximum voltage from both photo diodes.

(c) Reconnect P8; place paper-feed circuitry in slewing mode (continuous feed).

(d) Adjust R510 of C16 so that the trailing edge of the output (C16 pin 21) occurs at the half-amplitude point of the trailing edge of the input (C16 pin 23) signal (see figure 5-16).

(e) Adjust R510 of C17 so that the output of flip-flop PCR B (C10 pin 36) is phase-shifted 90 degrees from the output of PCR A (C10 pin 38). (See figure 5-17).

(f) Loosen photo-diode-assembly adjusting screw (3, figure 5-13).

(g) Slide photo-diode block up or down as required to obtain a 4-ms duration output from flip-flops PCR A and PCR B (figure 5-17). This will result in 20 inch-per-second paper feed speed.

5-44. MULTIVIBRATOR ADJUSTMENT. Three multivibrator circuits are located on each 12B printed-circuit card. One trimpot (R3) in each of these circuits provides adjustment of the multivibrator output pulse. The adjustment is accomplished by varying the trimpot

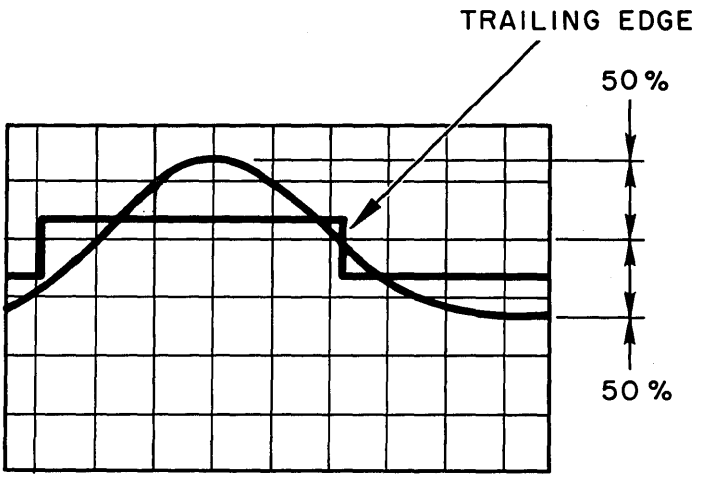


Figure 5-16. Photo-Diode Amplifier input/output Waveform

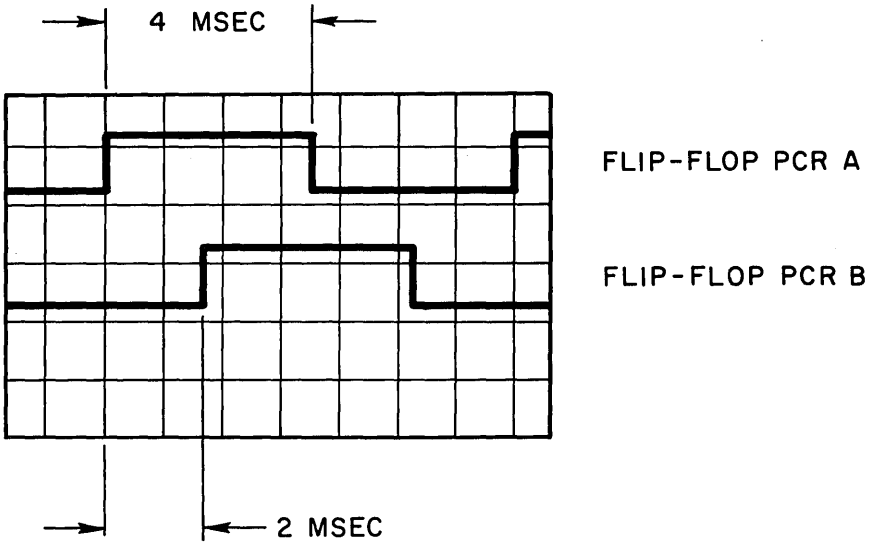


Figure 5-17. A-B Flip-Flop Outputs

to acquire the pulse widths listed in figure 5-18. Adjust the multivibrator in sequence given.

Figure 5-18. MULTIVIBRATOR ADJUSTMENT

CIRCUIT LOCATION	TEST POINT	PULSE WIDTH	REMARKS
C11-200	C11-12	200 us ±5%	
C12-200	C12-13	200 us ±5%	
C12-400	C12-24	100 us ±5%	
C13-400	C13-24	1300 us ±5%	
C13-200	C13-14	400 us ±5%	
C14-400	C14-24	8 to 12 ms	Adjust while stepping paper
C14-200	C14-14	100 us ±5%	Adjust while stepping paper
C11-600	C11-34	1 us ±5%	Adjust while printing or stepping paper on command from external data source
C12-600	C12-34	1.5 us ±5%	
C14-600	C14-33	1 us ±5%	
C13-600	C13-34	1 us ±5%	
C11-400	C11-24	100 us ±5%	
D21-200	D21-13	100 us ±5%	
D21-400	D21-24	100 us ±5%	Adjust while stepping paper
D21-600	D21-34	1 us ±5%	

5-45. HAMMER BANK ADJUSTMENT

5-46. The hammer bank is aligned at the factory and no further adjustment should be necessary. However; if the hammer bank is loosened accidentally so that the gap is not set properly (refer

to paragraph 5-15, a) the applicable hammer-bank adjustments of paragraphs 5-47 (vertical adjustment) and 5-48 (horizontal adjustment) should be performed.

5-47. The hammer-bank vertical adjustment is accomplished as follows.

(a) Loosen hammer-bank holding clamps (see figure 5-19).

(b) Loosen lock nut and rotate hammer-bank adjustment screws so that, with hammer bank flush against ends of screws, there is a 0.085-inch gap between ends of hammers and character drum with hammers in their neutral positions.

(c) The 0.085-inch gap should be measured at each end of hammer bank with a suitable thickness gauge (see figure 5-1).

(d) Tighten lock nut on adjustment screws; tighten holding clamp.

5-48. The hammer-bank horizontal adjustment is accomplished as follows.

(a) Loosen hammer-bank holding clamps. (See figure 5-10).

(b) The hammer bank should be manually positioned to align hammers with their respective row of characters on character drum.

(c) Tighten hammer-bank holding clamps.

5-49. HAMMER ALIGNMENT. Individual hammer-alignment is accomplished as follows.

(a) Connect oscilloscope to hammer-driver output. (The

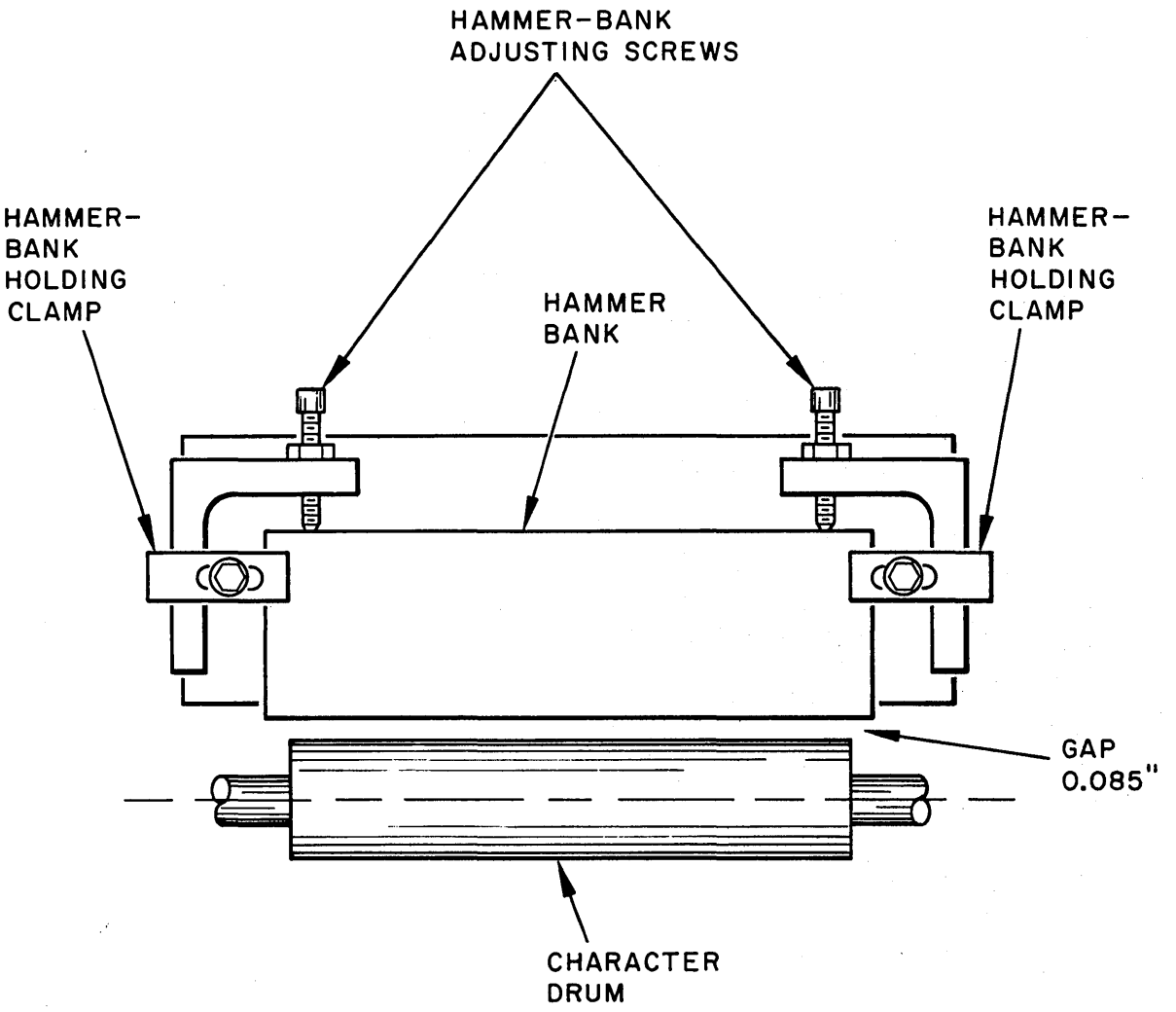


Figure 5-19. Hammer-Bank Adjustment Diagram

to paragraph 5-15, a) the applicable hammer-bank adjustments of paragraphs 5-47 (vertical adjustment) and 5-48 (horizontal adjustment) should be performed.

5-47. The hammer-bank vertical adjustment is accomplished as follows.

(a) Loosen hammer-bank holding clamps (see figure 5-19).

(b) Loosen lock nut and rotate hammer-bank adjustment screws so that, with hammer bank flush against ends of screws, there is a 0.085-inch gap between ends of hammers and character drum with hammers in their neutral positions.

(c) The 0.085-inch gap should be measured at each end of hammer bank with a suitable thickness gauge (see figure 5-1).

(d) Tighten lock nut on adjustment screws; tighten holding clamp.

5-48. The hammer-bank horizontal adjustment is accomplished as follows.

(a) Loosen hammer-bank holding clamps. (See figure 5-10).

(b) The hammer bank should be manually positioned to align hammers with their respective row of characters on character drum.

(c) Tighten hammer-bank holding clamps.

5-49. HAMMER ALIGNMENT. Individual hammer-alignment is accomplished as follows.

(a) Connect oscilloscope to hammer-driver output. (The

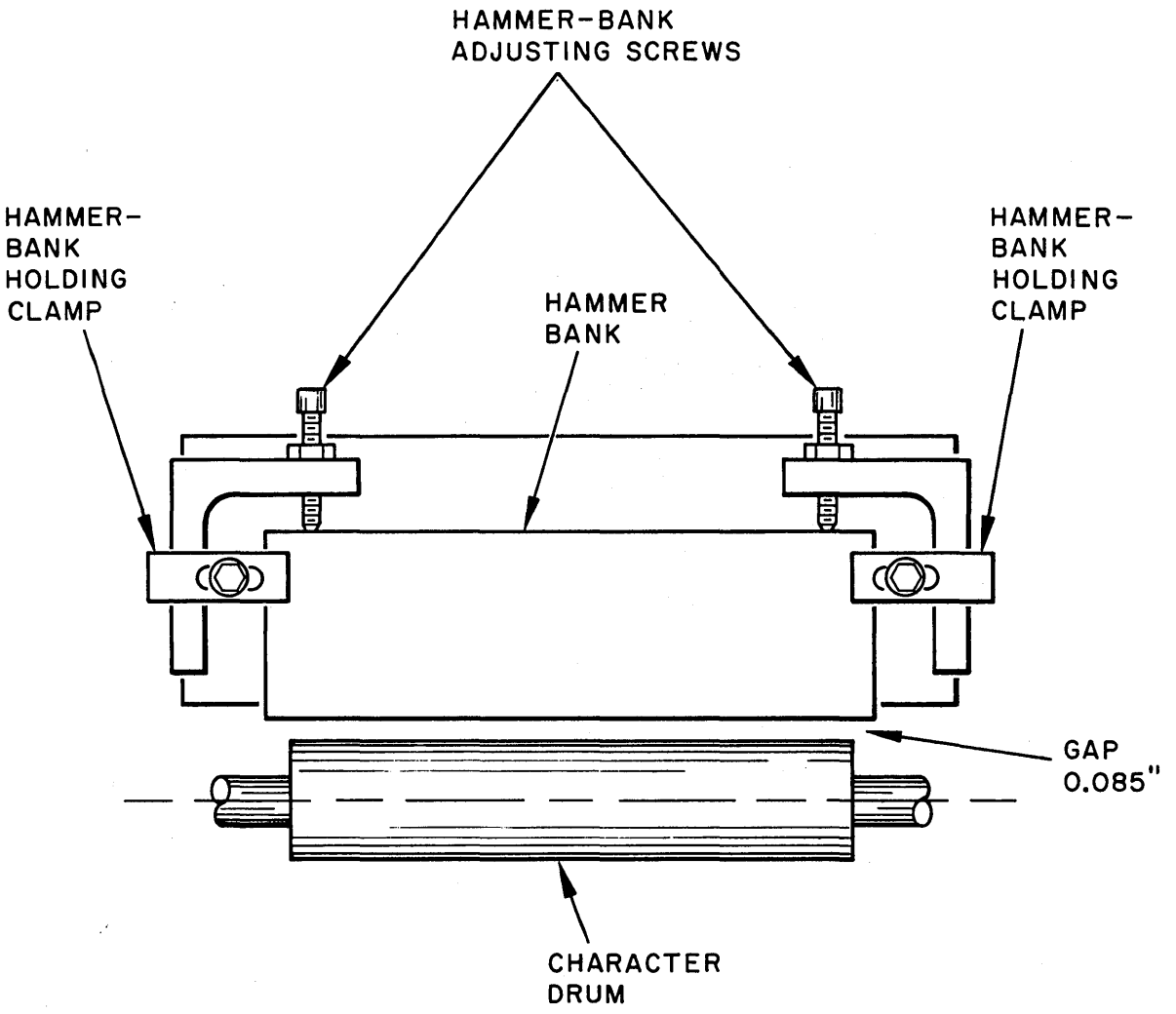


Figure 5-19. Hammer-Bank Adjustment Diagram

numbered outputs on logic diagrams 4 through 20 indicate number of the hammer).

(b) Set the drive pulse for 1.5 ms firing time. The drive-pulse duration is set for all hammers by adjusting C13-400 (refer to paragraph 5-44). This will result in a free-fly time of approximately 800 usec.

(c) Hammer-impact time is adjusted while printing on single-part paper. Adjust the first hammer for a free-flight time of 800 usec (see figure 5-20). Mark the point of hammer impact on the oscilloscope with a grease pencil. Adjust the remaining hammers so that the impact occurs at the same time as the first hammer.

(d) Hammer free-flight time is adjusted by rotating hammer-backstop set screw (1 and 7, figure 5-21).

DPC-52

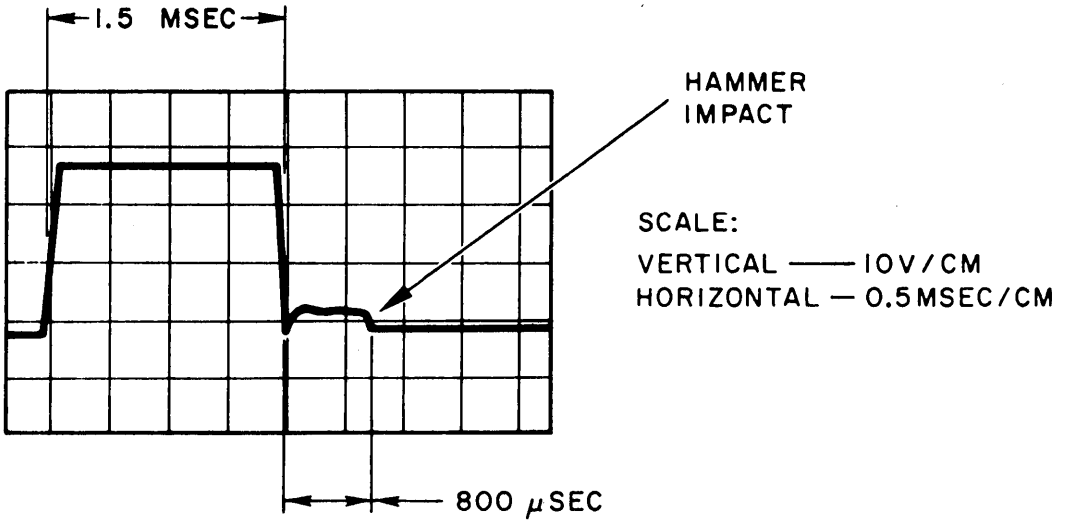


Figure 5-20. Hammer-Firing-Pulse Waveform

1. Hammer Leg Set Screw

2. Hammer Bank Positioning Control

3. Hammer Backstop Set Screw

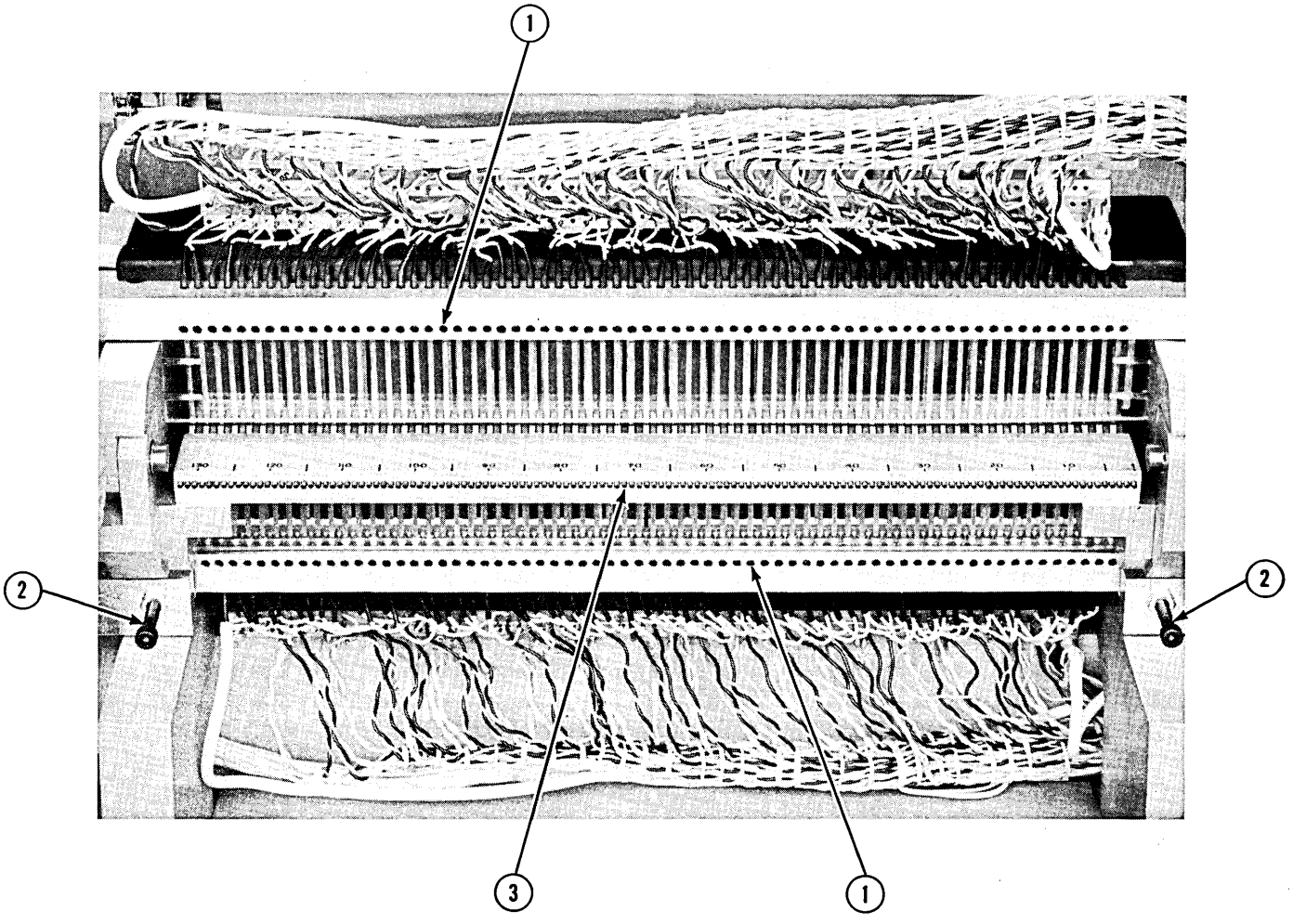


Figure 5-21 Hammer Bank (Rear View)

5-50. Paper-Drive-Belt Tension Adjustment. The tension of the paper-drive belt is adjusted by applying 7 pounds pressure, upward, against the bottom of the idler bearing bracket (13, figure 5-10) after loosening the two idler-bearing bolts (12, figure 5-9; and 4, figure 5-7.

5-51. Power Supply Adjustments

5-52. Voltage Adjustments (-30V, -20V and +20V Power Supplies). The voltage adjustments for the -30V, -20V and +20V power supplies are accompanied by connecting the differential DC voltmeter to the output of the power supply and adjusting the applicable control. The VOLTAGE ADJUST controls for these three power supplies are located on the front of the electronics gate (figure 5-2). If dropping resistor R20 (logic diagram no. 25) is ever replaced it should be adjusted for a 30-volt nominal output.

5-53. Current Limit Adjustments (+20V and -20V Power Supply). The CURRENT LIMIT ADJUST for the +20 VOLT and -20 VOLT supplies should be accomplished in the following manner.

(a) Disconnect power-supply outputs from the printer.

(b) Connect an adequate load to output terminals. The load must consist of the equivalent of a variable resistor with an end-to-center resistance of 4 ohms and a minimum power rating of 200 watts.

(c) Connect a DC ammeter in series with the load. The ammeter should have a center-scale reading of approximately 5 amps.

(d) Connect a differential DC voltmeter in parallel with output terminals and energize power supply.

(e) Set VOLTAGE ADJUST control R30 (+20V supply) or R32 (-20V supply) for a 20V indication on voltmeter.

(f) Adjust +20V supply load resistance for a 5 amp indication on ammeter. Adjust -20V supply load resistance for a 5 AMP indication on ammeter.

(g) Turn CURRENT LIMIT ADJUST control counter-clockwise until voltage drops below 20 volts, then rotate CURRENT LIMIT ADJUST control clockwise until voltage is just 20 volts.

(h) Disconnect power and all test fixtures.

(i) Reconnect power supply outputs to printer.

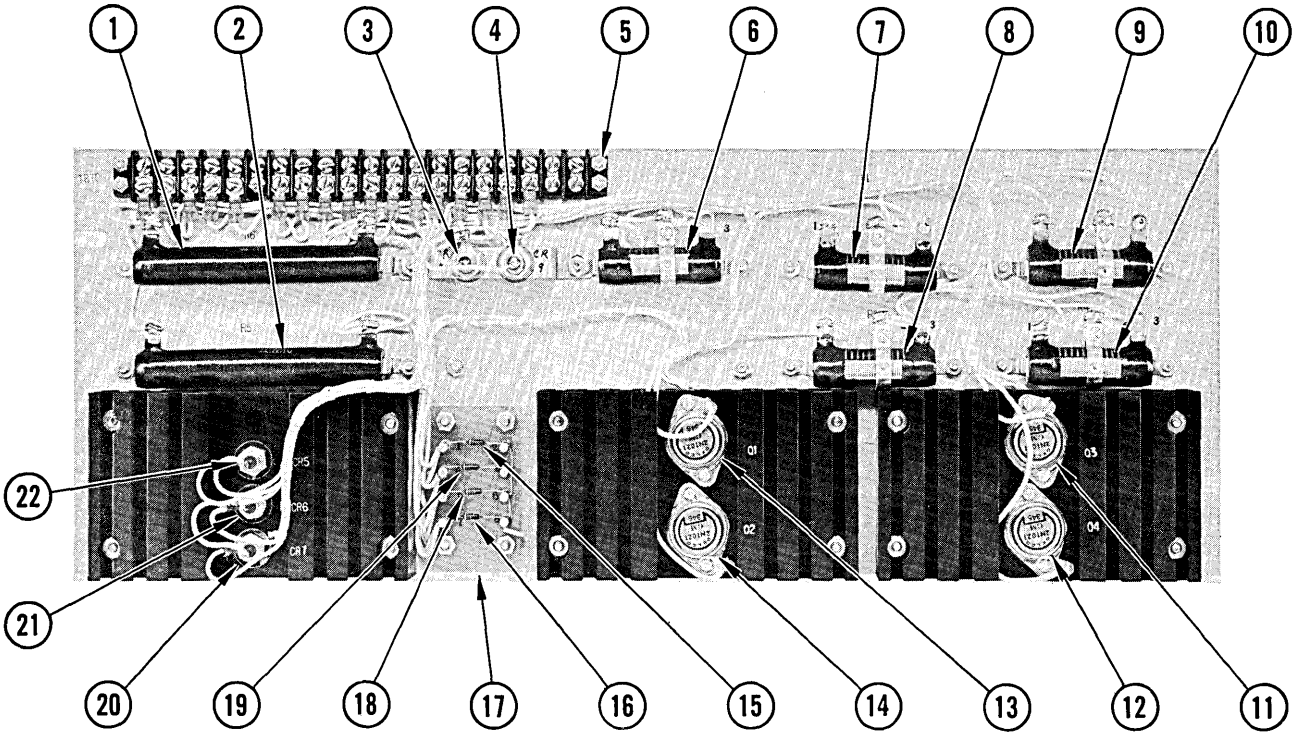
5-54. Voltage Regulator Adjustment. The DC voltages derived from the voltage-regulator cards are monitored by the panel voltmeter located on the MAINTENANCE TEST PANEL (figure 5-3). If any of the DC voltages appear to be out of adjustment the following steps should be performed.

(a) Connect a differential DC voltmeter to output pin of voltage-regulator card.

(b) Vary voltage-adjust trimpot on printed-circuit card to acquire proper voltage indication on voltmeter.

(c) Set VOLTAGE SELECTION switch on MAINTENANCE TEST PANEL, figure 5-3, to voltage being adjusted.

(d) Vary voltage-adjust trimpot located on test panel to acquire proper voltage indication on differential DC voltmeter.



1. R6	12. Q4
2. R5	13. Q1
3. CR8	14. Q2
4. CR9	15. CR1
5. TB70	16. CR4
6. R7	17. TB15
7. R1	18. CR3
8. R2	19. CR2
9. R3	20. CR7
10. R4	21. CR6
11. Q3	22. CR5

Figure 5-22. Motor-Driver Panel

5-55. Clock Adjustment. The clock adjustment is accomplished as follows. Adjust R505, on the 31B printed-circuit card at position D14, for a 2.0 usec repetition rate. The repetition rate can be measured at D14, pin 41.

5-56. Motor-Driver Panel Adjustments. The following resistors, located on the motor-driver panel (figure 5-22), are set at the factory. Adjustment is normally required only if one of the resistors is replaced.

(a) Adjust motor-driver current setting resistors R1-R4 (5 ohms, 25W) to 3.25 ohms.

(b) Adjust -10V bleeder resistor R7 (50 ohms, 50W) to 20 ohms.

(c) Adjust -6V bleeder resistor R7 (50 ohms, 25W) to 13 ohms.

(d) Adjust -2.5V shunt dropping resistor (50 ohms, 50W) for maximum resistance.

5-57. Recommended Spares

5-58. A list of recommended spares is provided in figure 5-23.

Figure 5-23. LIST OF RECOMMENDED SPARES

CARD NO.		PART NO.	QUANTITY
1A	Hammer Driver	200185-1	2
2A	Hammer Driver Receiver	200193-1	2
3D	Paper Feed Control	202074-1	1
4C	Photo Diode Amplifier	202078-1	1

Figure 5-23. LIST OF RECOMMENDED SPARES (cont'd.)

CARD NO.		PART NO.	QUANTITY
5A	Hammer Driver Power Amplifier	200176-1	1
6A	NOR Gate	200235-1	1
7A	Flip-Flop	200197-1	1
7D	Flip-Flop	200914-1	1
8A	Address Decode	200227-1	1
10E	Comparator	201413-1	1
11A	Output Driver	200223-1	1
12A	Multivibrator	200243-1	1
13D	Logic Receiver	201575-1	1
21M	Logic Driver	201408-1	1
21N	Logic Driver	201457-1	1
21P	Logic Driver	201481-1	1
21V	Logic Driver	202497-1	1
22C	NAN Gate	201441-1	1
27B	Read Amplifier	201689-1	1
28B	Inhibit Driver	201472-1	1
29A	Selection Switch	201332-1	1
31B	Clock/Timing	201777-1	1
33C	Delay Line	201488-1	1
99A	-5V Regulator	200421-1	1
99B	+5V Regulator	200258-1	1
99D	-10V Regulator	200425-1	1
99E	-15V Regulator	200429-1	1

FIGURE 5-23. LIST OF RECOMMENDED SPARES (cont'd.)

DESCRIPTION	PART NO.	QUANTITY
Timing Belt (paper stepping)	30138 x 3/8p	1
Timing Belt (tractor adjust)	250-XLW037	1
Fuse, 0.5A, 3AG		5
Fuse, 1.0A, 3AG		5
Fuse, 10A, 3AG		5
Hammer, Center Flag	200406-1	4
Hammer, End Flag	200406-2	8
Lamp, Illumination	Chicago Lamp, CM8-56	1
Lamp, Illumination	VW, N-17-723-1	2
Lamp, Switch Indicator	GE 327	5
Photo Diode	H61	2
Relay	1R-1215-G24, 24VDC or GPRTPX-60T	1
Ribbon		2
Set Screw, Nylock Cup Point	No. 2, NC-56, 1/4	13
±20V Power Supply		
Control Assembly	200865-1	1
Rectifier, Silicon	1N3210	2
Transistor, Silicon	15104	2
Transistor, Silicon	15204	2
-30V Power Supply		
Control Assembly	202419-1	1

FIGURE 5-23. LIST OF RECOMMENDED SPARES (cont'd.)

DESCRIPTION	PART NO.	QUANTITY
Rectifier, Silicon	1N3208	1
Rectifier, Silicon Controlled	2N684	2
Filter, Air	American Filler Co., Louisville, Ky., Model D1	4

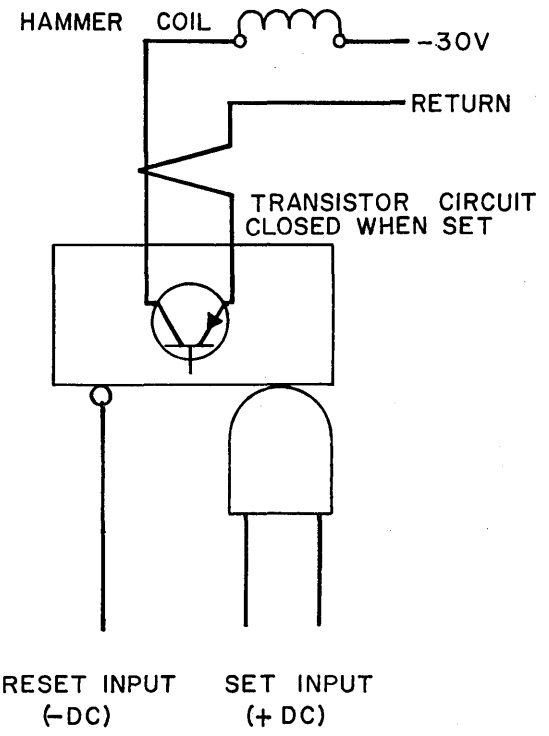
SECTION VI

DRAWINGS

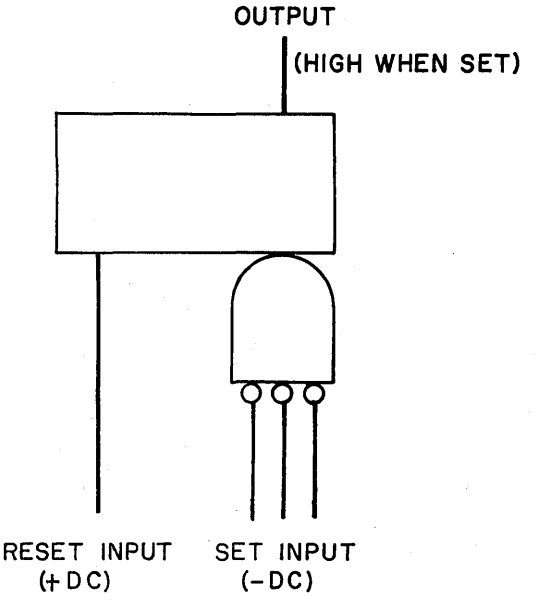
6-1. GENERAL

6-2. This section contains schematic and assembly drawings of all printed circuit cards, and all logic diagrams of the printer. Figure 6-1 illustrates symbols used in the logic diagrams. A complete listing of all drawings in this section appears in the List of Illustrations at the front of the manual.

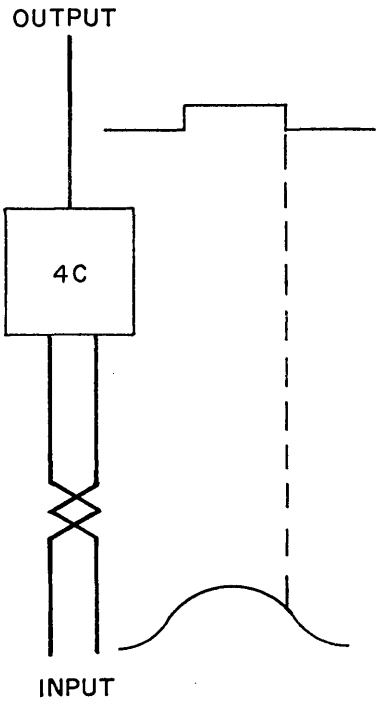
(1) HAMMER DRIVER 1A



(2) HAMMER DRIVER RECEIVER 2A



(3) PHOTO DIODE AMPLIFIER 4C



(4) FLIP FLOP 7A AND 7B

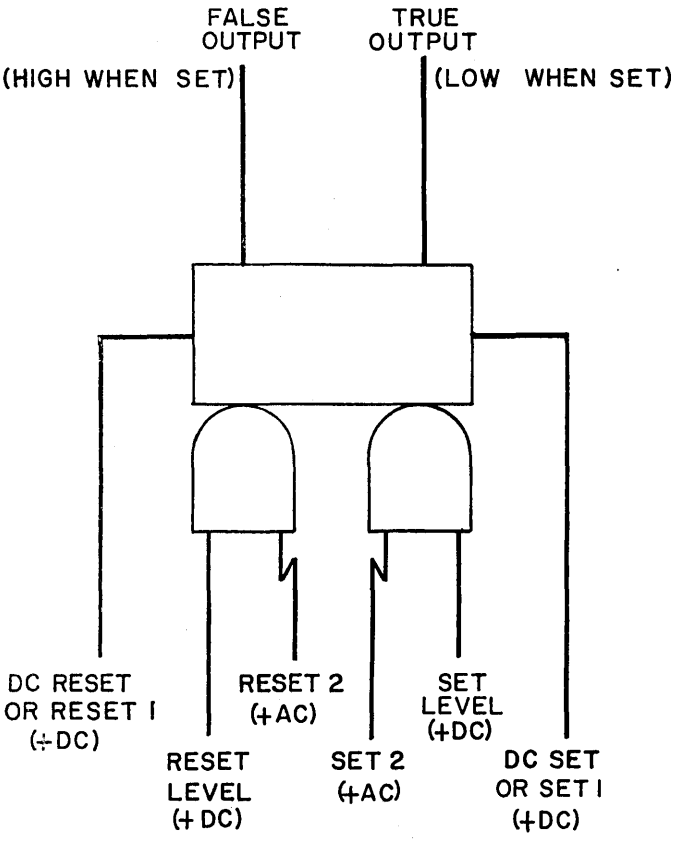
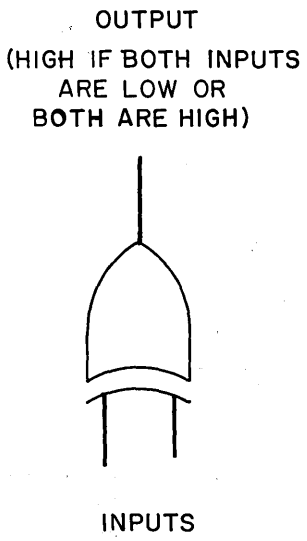
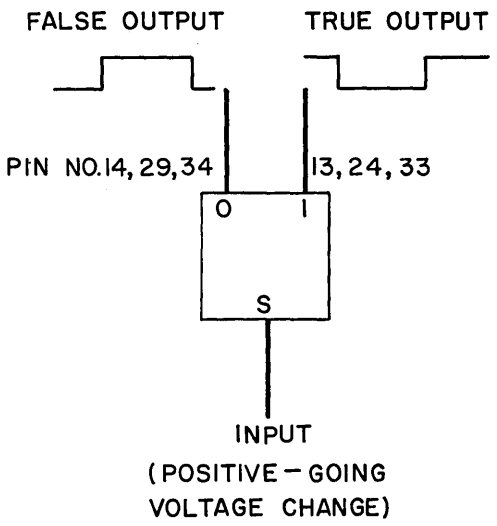


Figure 6-1. Logic Diagram Symbols

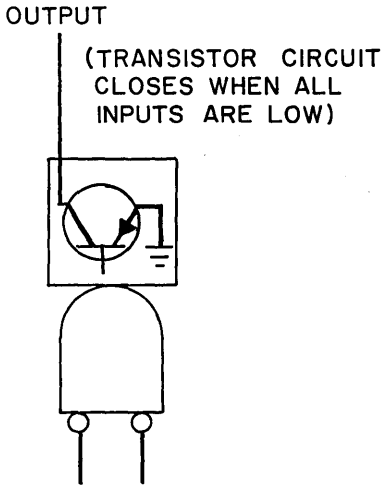
(5) COMPARATOR 10E



(6) MULTIVIBRATOR 12A



(7) INHIBIT DRIVER 28B



(8) SELECTION SWITCH 29A

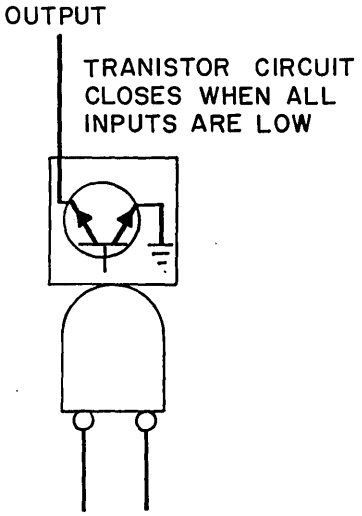
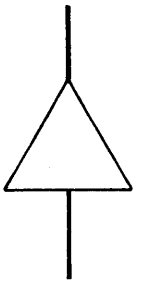
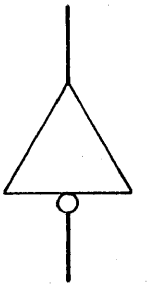
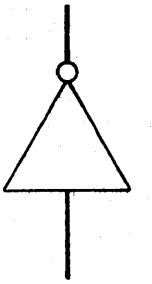
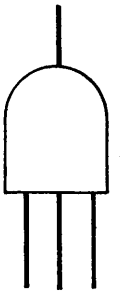
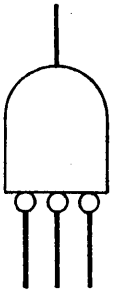
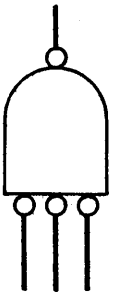
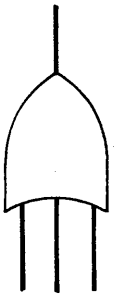
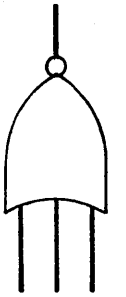
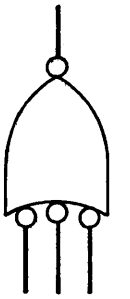
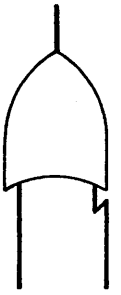


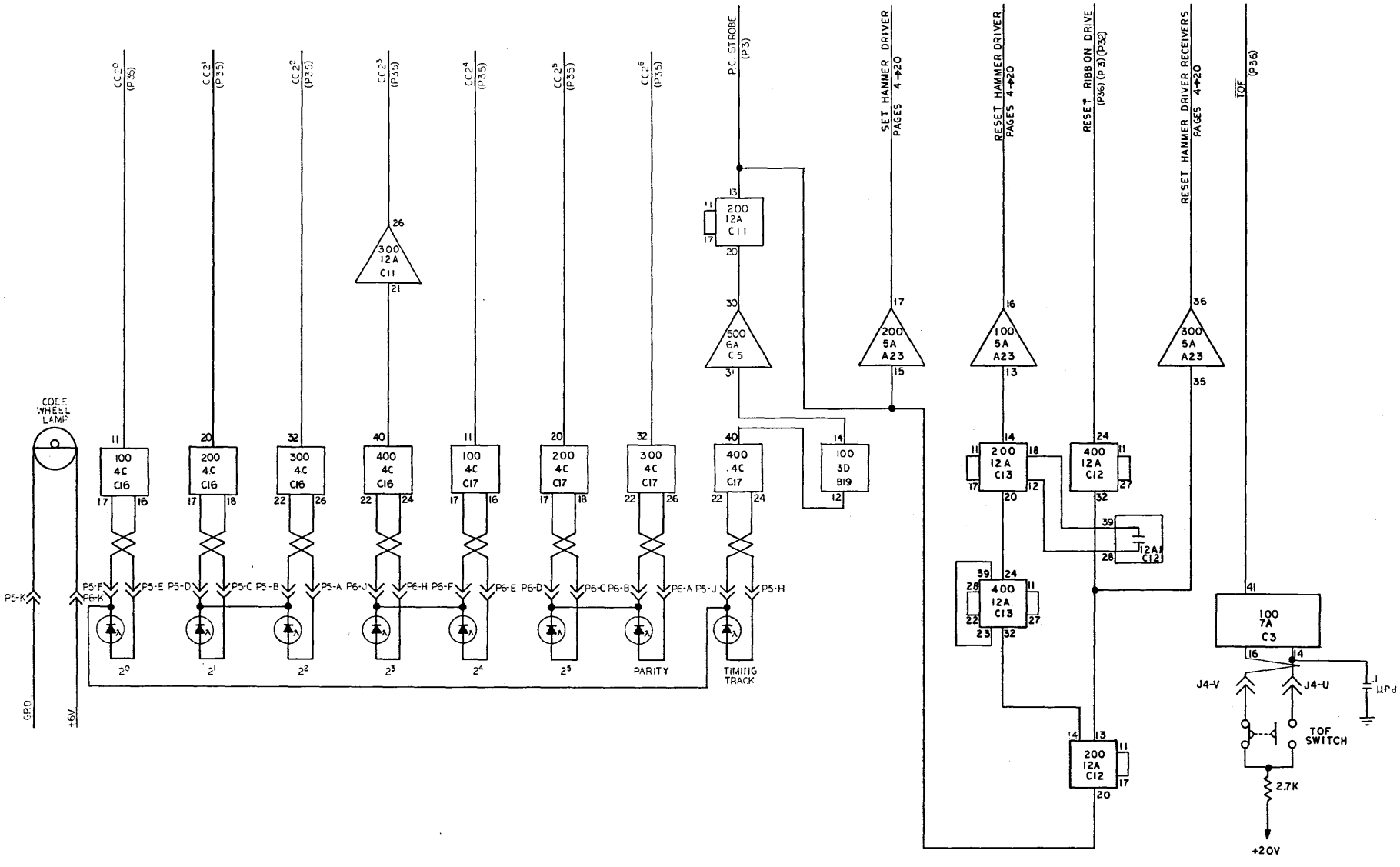
Figure 6-1. Logic Diagram Symbols

(9)

	HIGH INPUTS CAUSE HIGH OUTPUT	LOW INPUTS CAUSE HIGH OUTPUT	HIGH INPUTS CAUSE LOW OUTPUT	LOW INPUTS CAUSE LOW OUTPUT
AMPLIFIER	5A 6A 12A 21P 	6A 8E 10E 11A 21P 33C 	3B 5A 6A 12A 21N 	
AND GATE	13D 	6A 21N 21U 22C 27B 28B 		8A 8E 21N 21P 21U 
OR GATE	21P 		6A 21U 	
OR GATE 7AC 7DC INPUT	3B 			

CARD TYPES THAT PROVIDE THESE LOGIC FUNCTIONS ARE LISTED BY EACH SYMBOL

Figure 6-1 Logic Diagram Symbols

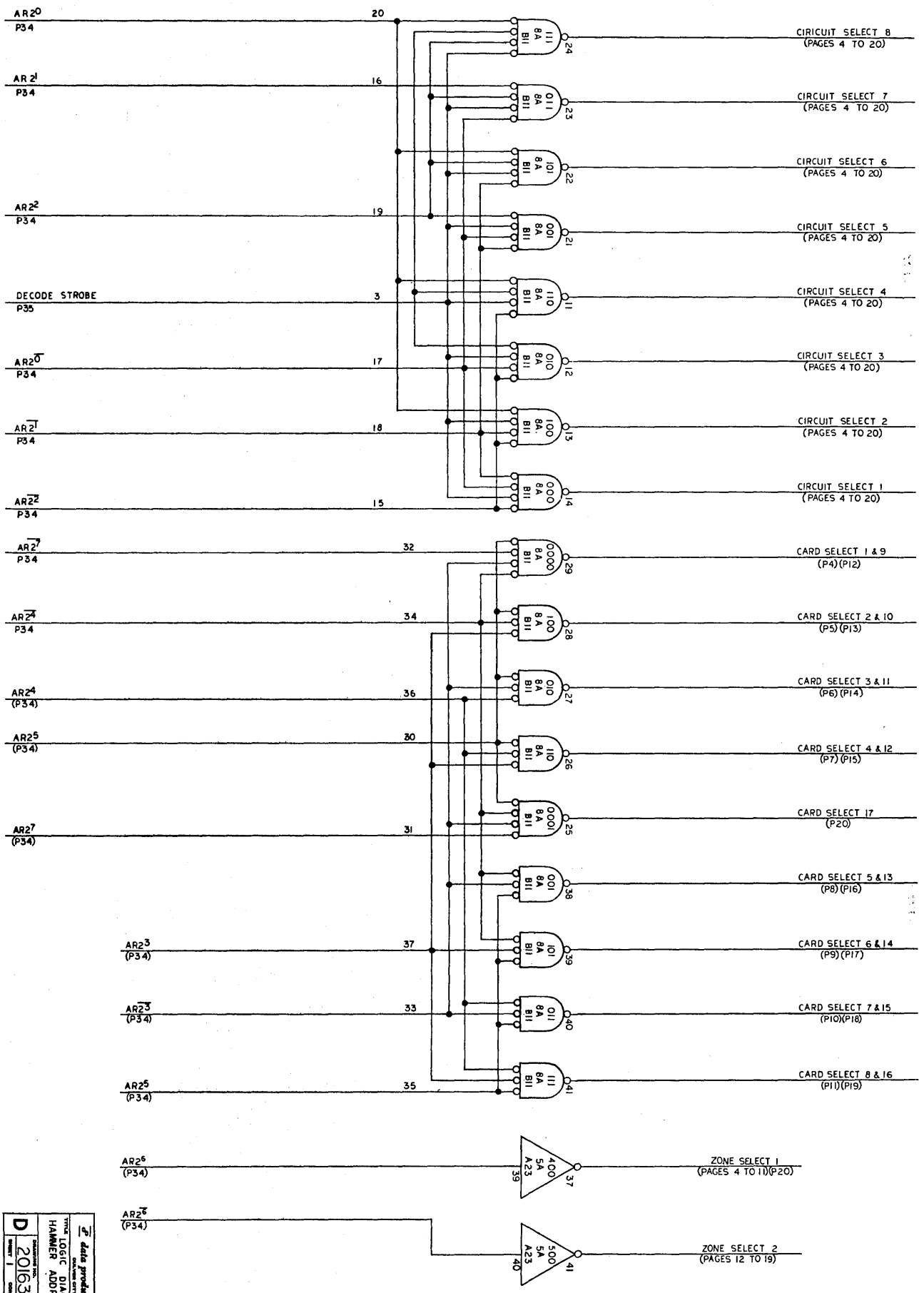


data products corporation
CULVER CITY, CALIFORNIA

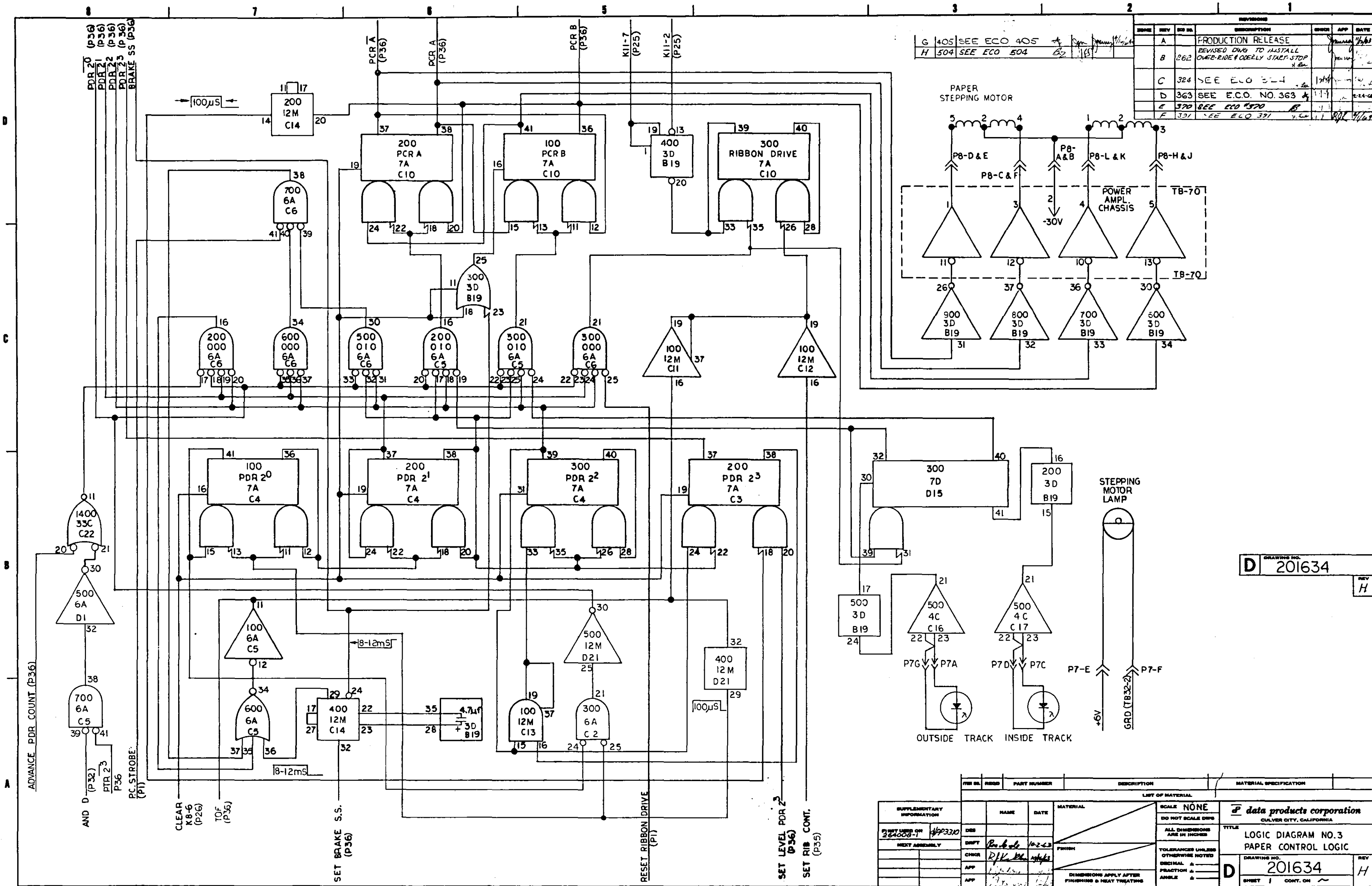
TITLE LOGIC DIAGRAM-NO. 1
TIMING AND PHOTO DIODE AMR

D 201632 0

SHEET 1 CONT. ON



data products corporation
TITLE LOGIC DIAGRAM — NO. 2
HAMMER ADDRESS DECODE
D 201633
SHEET 1
REV B



REVISIONS

ZONE	REV	ECO NO.	DESCRIPTION	CHECK	APP	DATE
	A		PRODUCTION RELEASE			
	B	262	REVISED DWG TO INSTALL OVER-RIDE & ODERLY START-STOP			
	C	324	SEE ECO 324			
	D	363	SEE E.C.O. NO. 363			2-24-64
	E	370	SEE ECO #370			
	F	391	SEE ECO 391			
	G	405	SEE ECO 405			
	H	504	SEE ECO 504			

data products corporation
CULVER CITY, CALIFORNIA

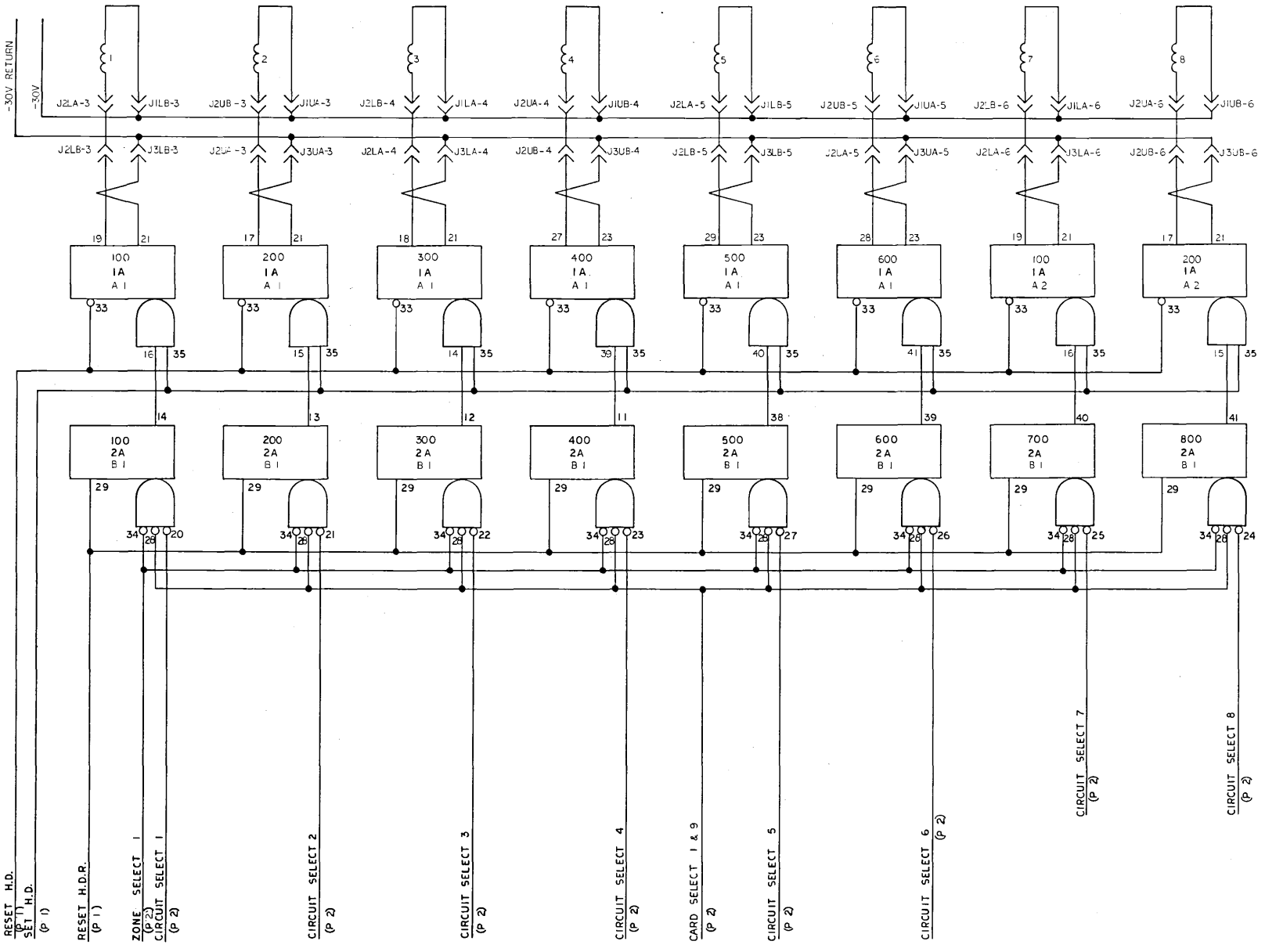
TITLE: LOGIC DIAGRAM NO.3 PAPER CONTROL LOGIC

DRAWING NO. D 201634 REV H

SCALE NONE — SHEET 1 — CONT. ON ~

FIRST USED ON 264008-1 — DP3310

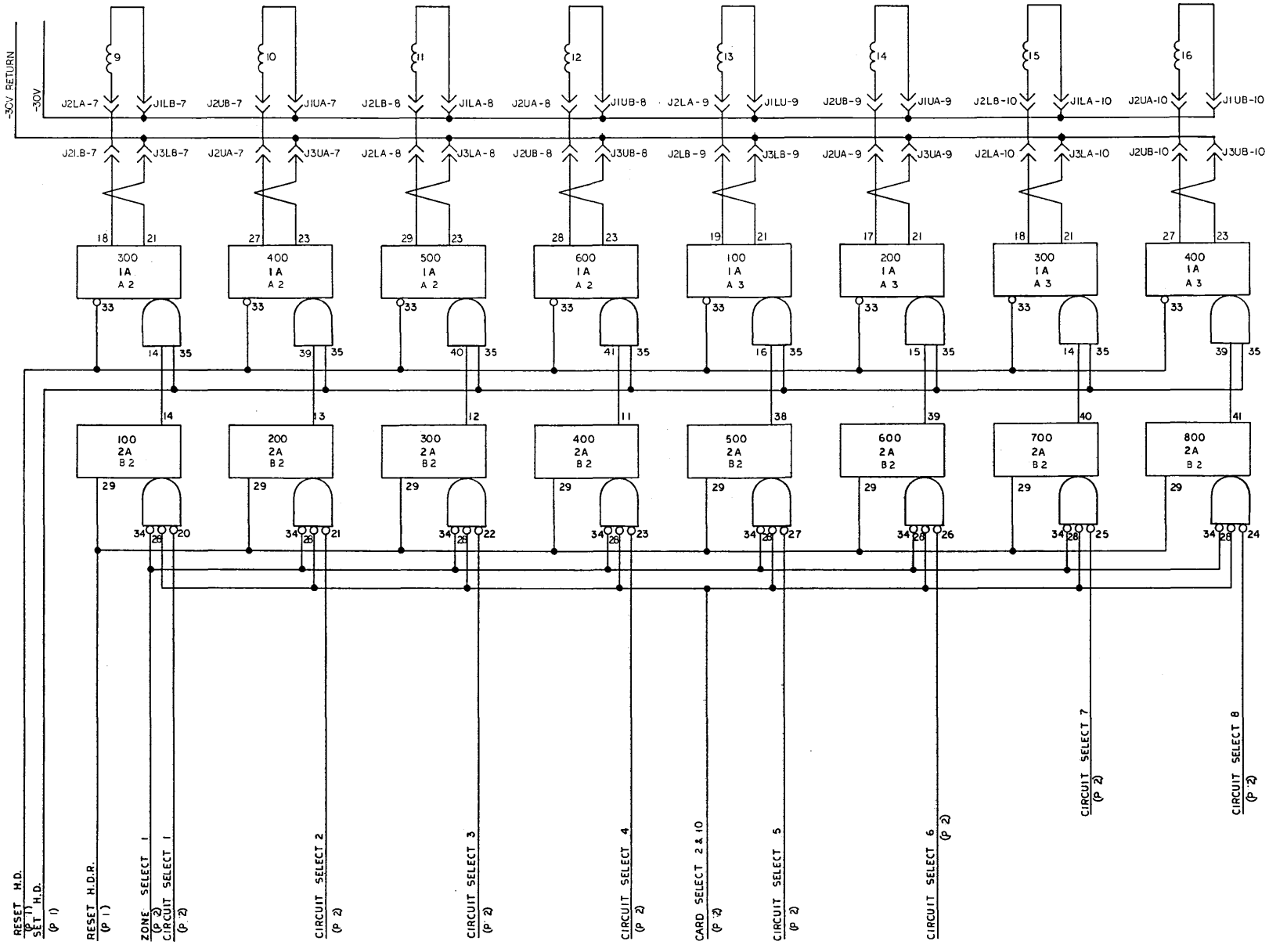
DRFT 10-2-63



data products corporation
CULVER CITY, CALIFORNIA

TITLE LOGIC DIAGRAM NO. 4
HAMMER DRS & REC 1 TO 8

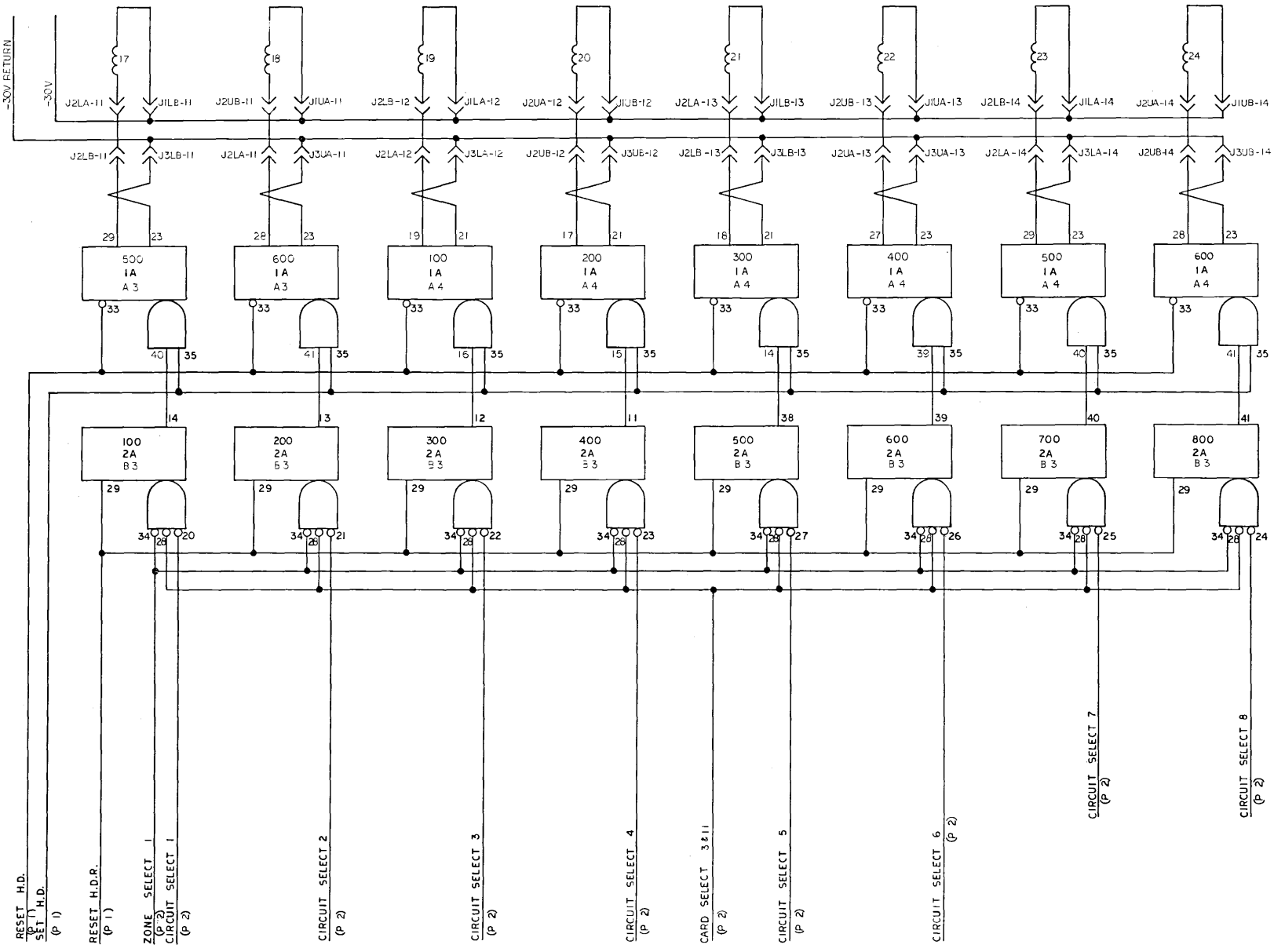
D | DRAWING NO. 201635 | REV A
SHEET 1 | CONT. ON



data products corporation
CULVER CITY, CALIFORNIA

TITLE LOGIC DIAGRAM NO 5
HAMMER DRS & REC 9 TO 16

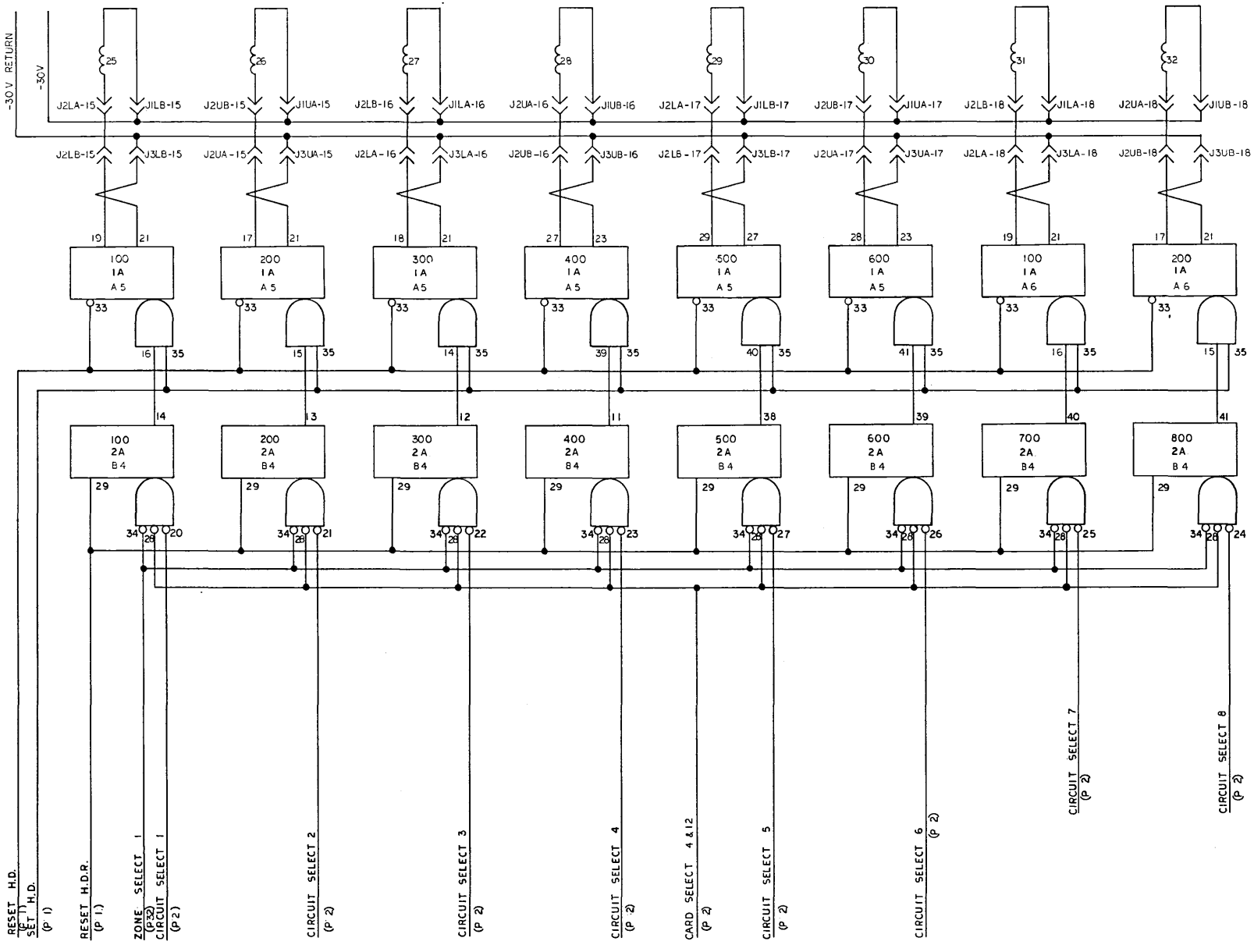
D | DRAWING NO. 201636 | REV A
SHEET 1 CONT. ON



data products corporation
CULVER CITY, CALIFORNIA

TITLE
LOGIC DIAGRAM NO. 6
HAMMER DRS. & REC. 17 TO 24

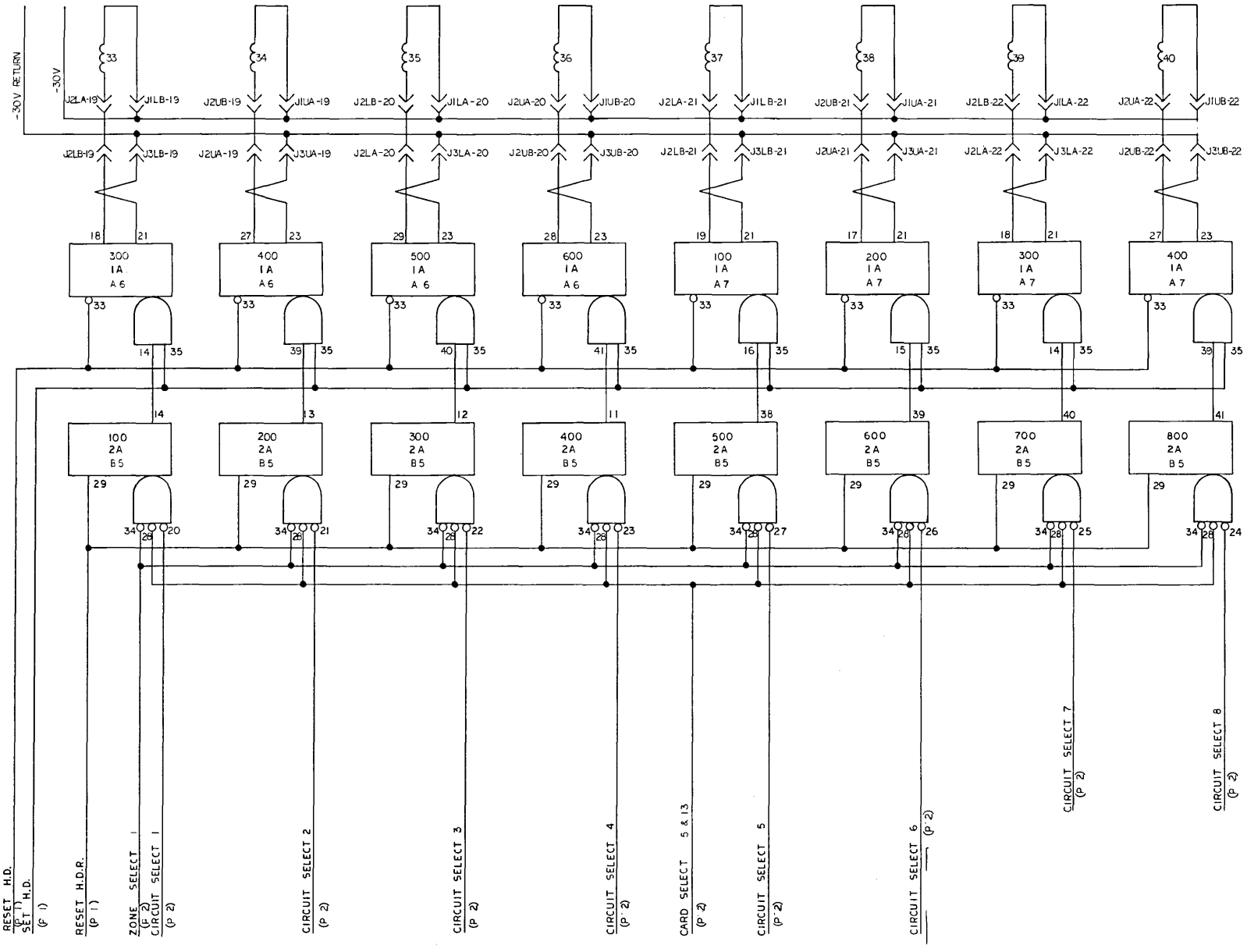
D | DRAWING NO. 201637 | REV A
SHEET 1 | CONT. ON



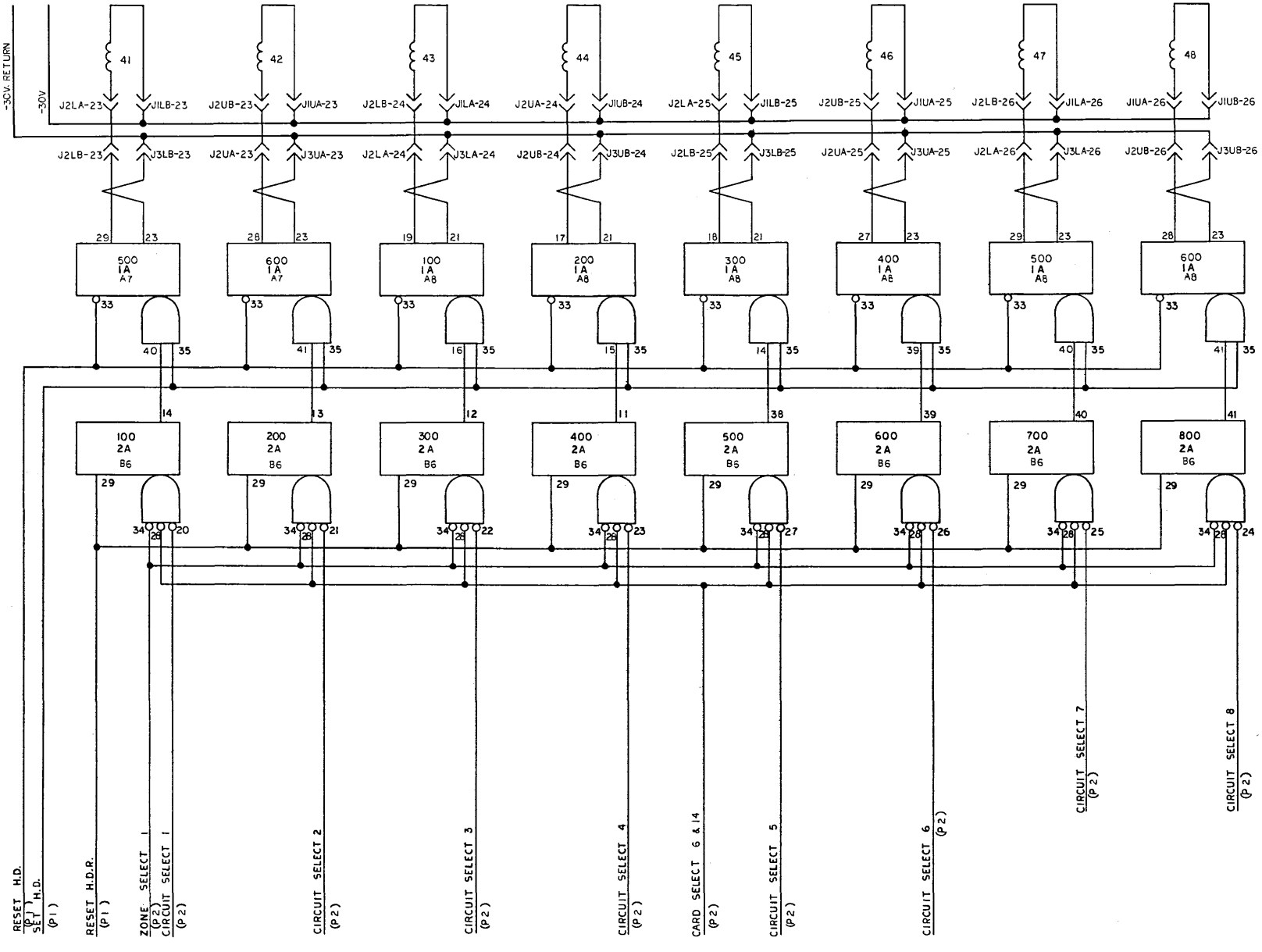
data products corporation
CULVER CITY, CALIFORNIA

TITLE: LOGIC DIAGRAM NO. 7
HAMMER DRS. & REC. 25 TO 32

D	DRAWING NO. 201638	REV A
	SHEET 1 CONT. ON	



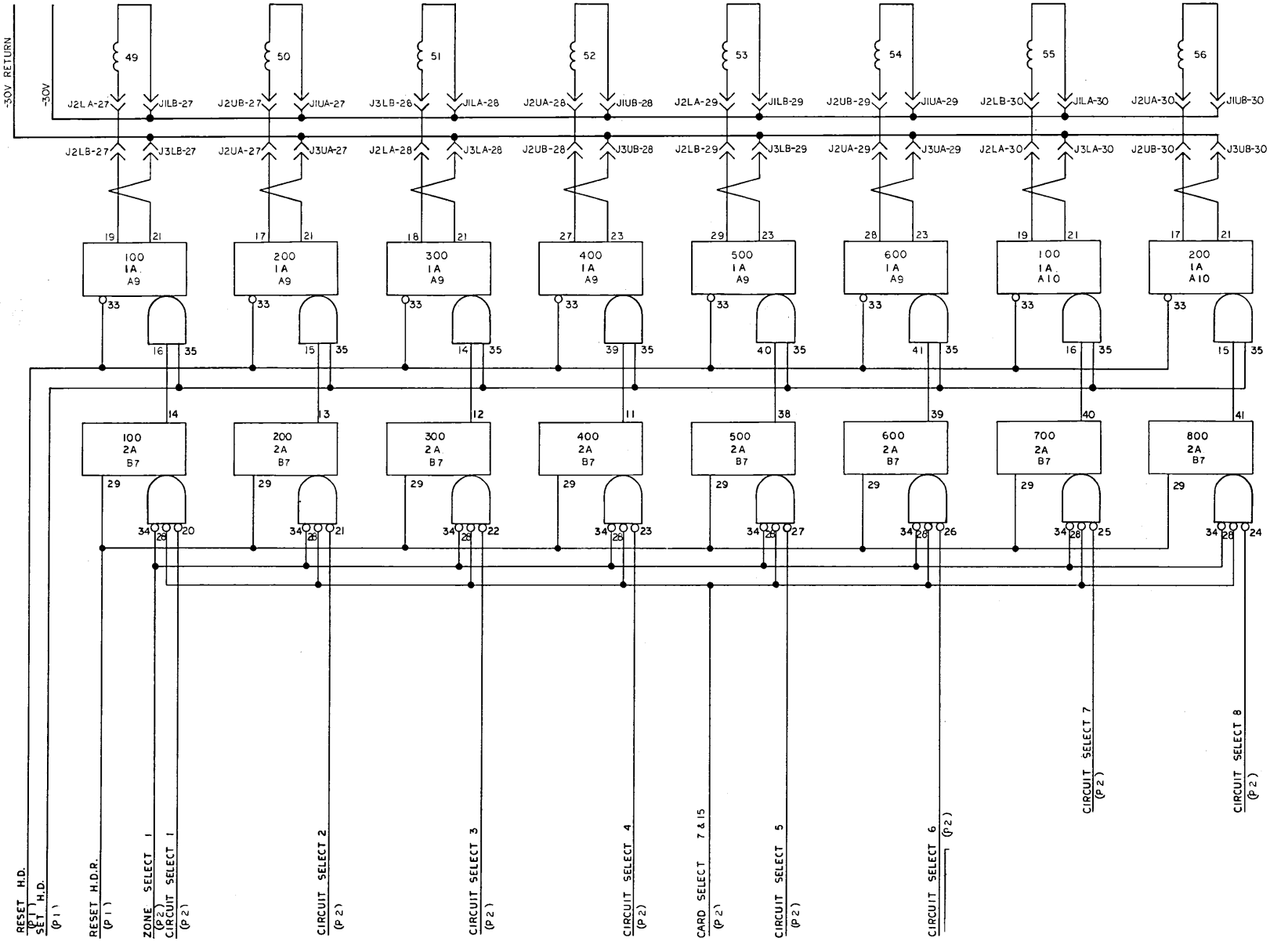
data products corporation — CULVER CITY, CALIFORNIA	
TITLE	LOGIC DIAGRAM NO. 8 HAMMER DRS. & REC. 33 TO 40
D	DRAWING NO. 201639 — REV A
	SHEET 1 — CONT. ON



data products corporation
CULVER CITY, CALIFORNIA

TITLE: LOGIC DIAGRAM NO. 9
HAMMER DRS & REC 41 TO 48

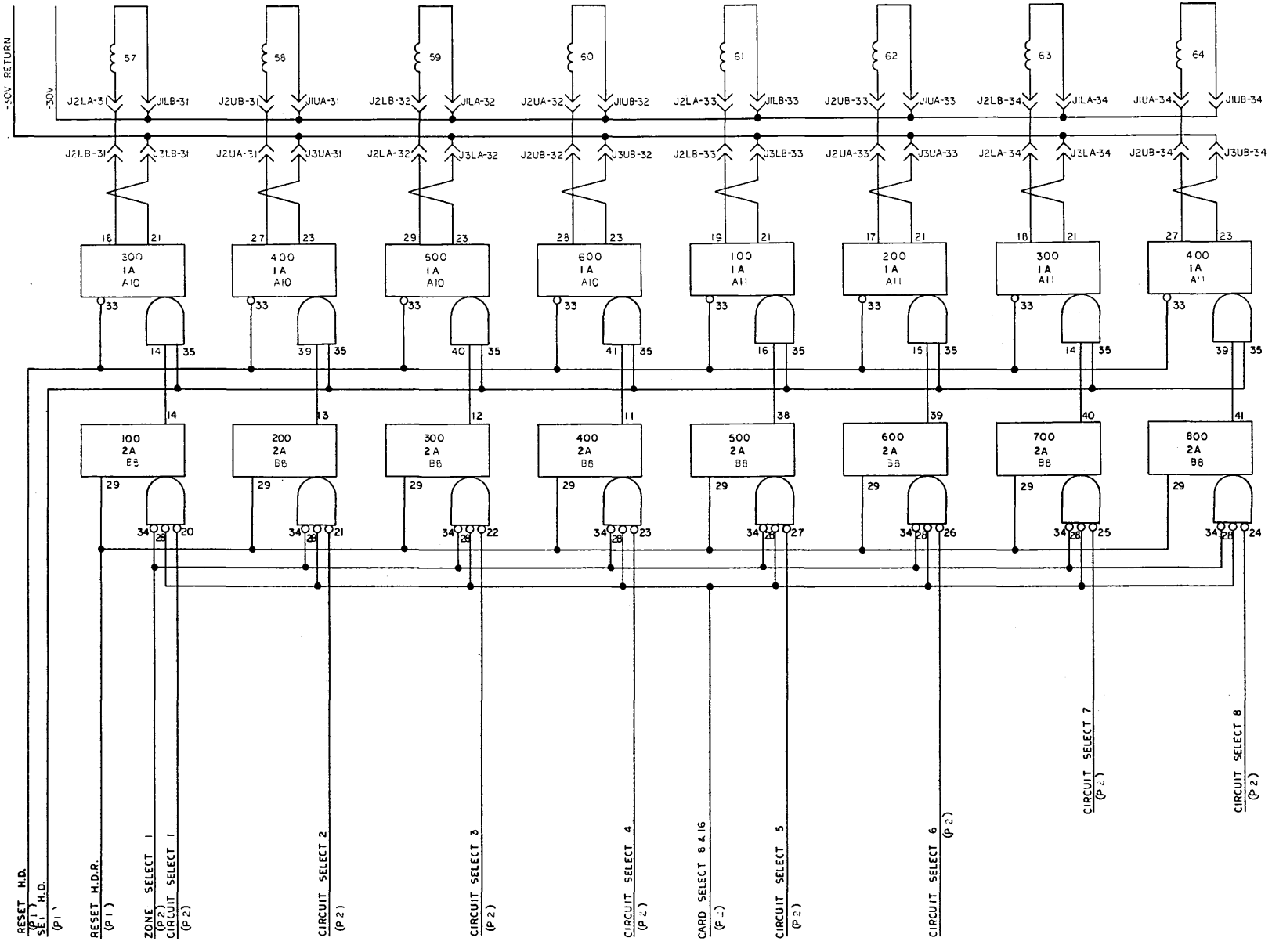
D | DRAWING NO. 201640 | REV A
SHEET 1 | CONT. ON



data products corporation
CULVER CITY, CALIFORNIA

TITLE
LOGIC DIAGRAM NO. 10
HAMMER DRS. & REC. 49 TO 56

D | DRAWING NO. 201641 | REV A
SHEET 1 | CONT. ON

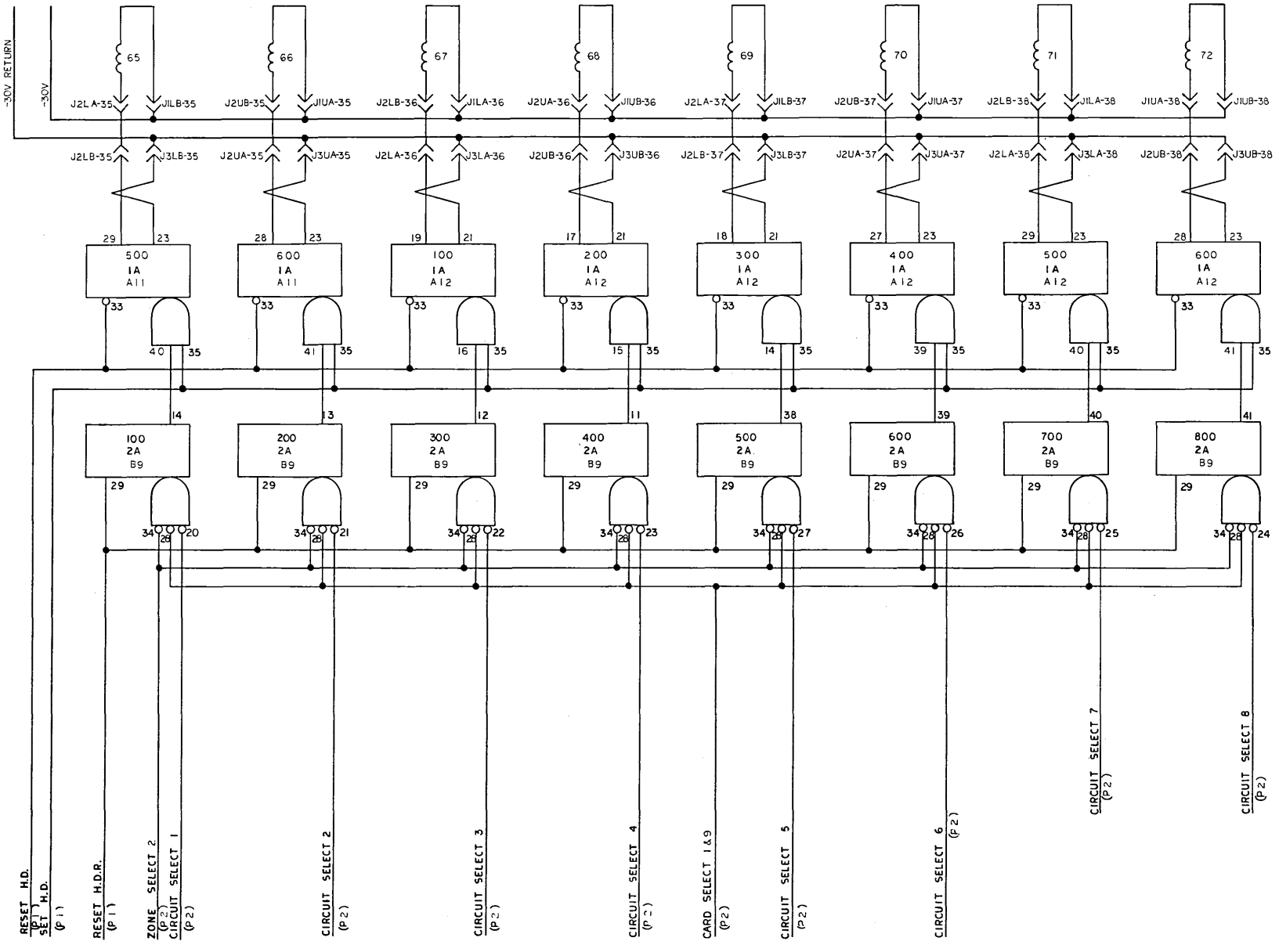


data products corporation
CULVER CITY, CALIFORNIA

TITLE
LOGIC DIAGRAM NO. 11
HAMMER DRS. & REC. 57 TO 64

D | DRAWING NO. 201642 | REV A

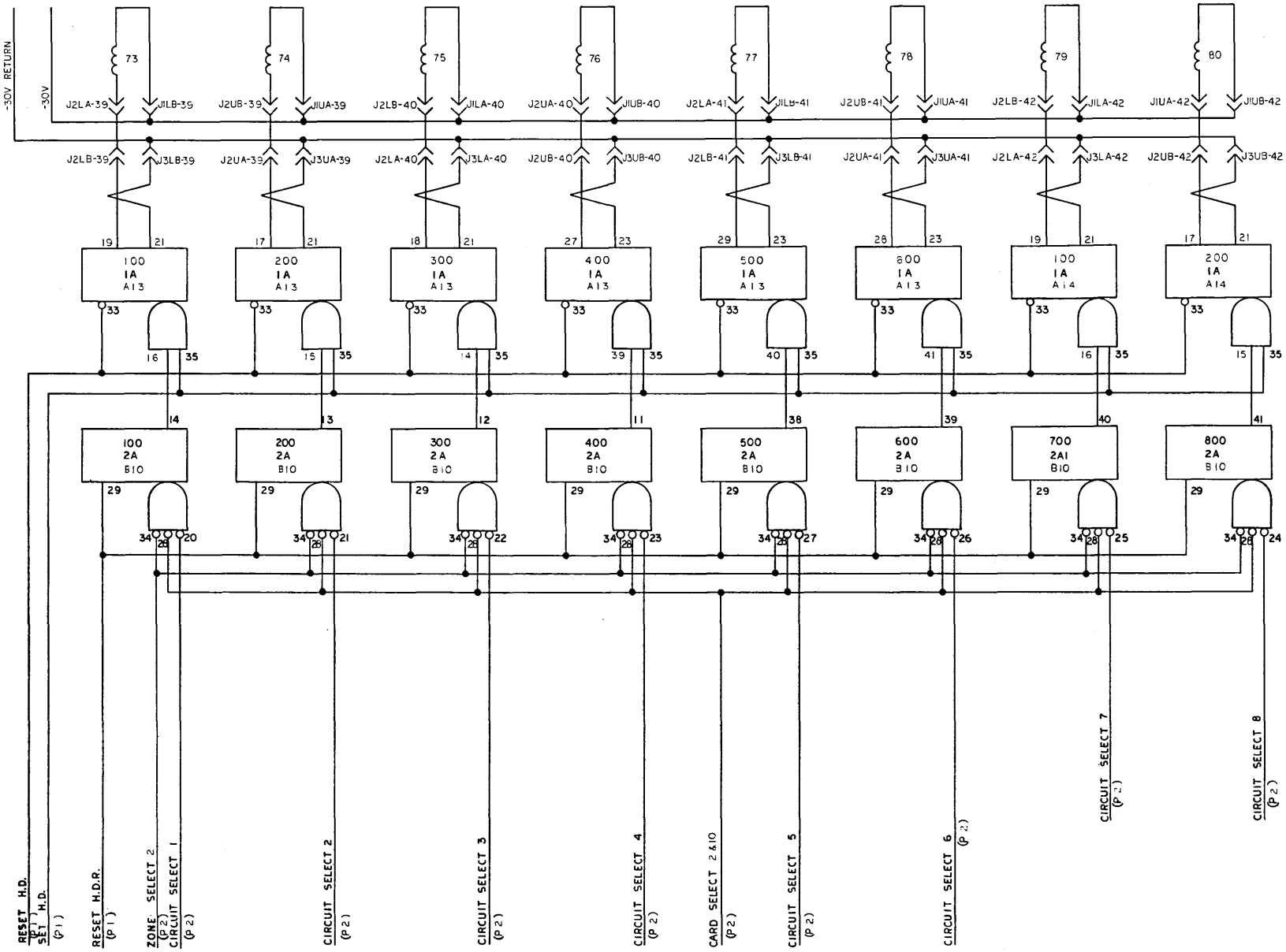
SHEET 1 | CONT. ON



data products corporation
CULVER CITY, CALIFORNIA

TITLE
LOGIC DIAGRAM NO. 12
HAMMER DPS. & REC. 65 TO 72

D | DRAWING NO. 201643 | REV A
SHEET | CONT. ON

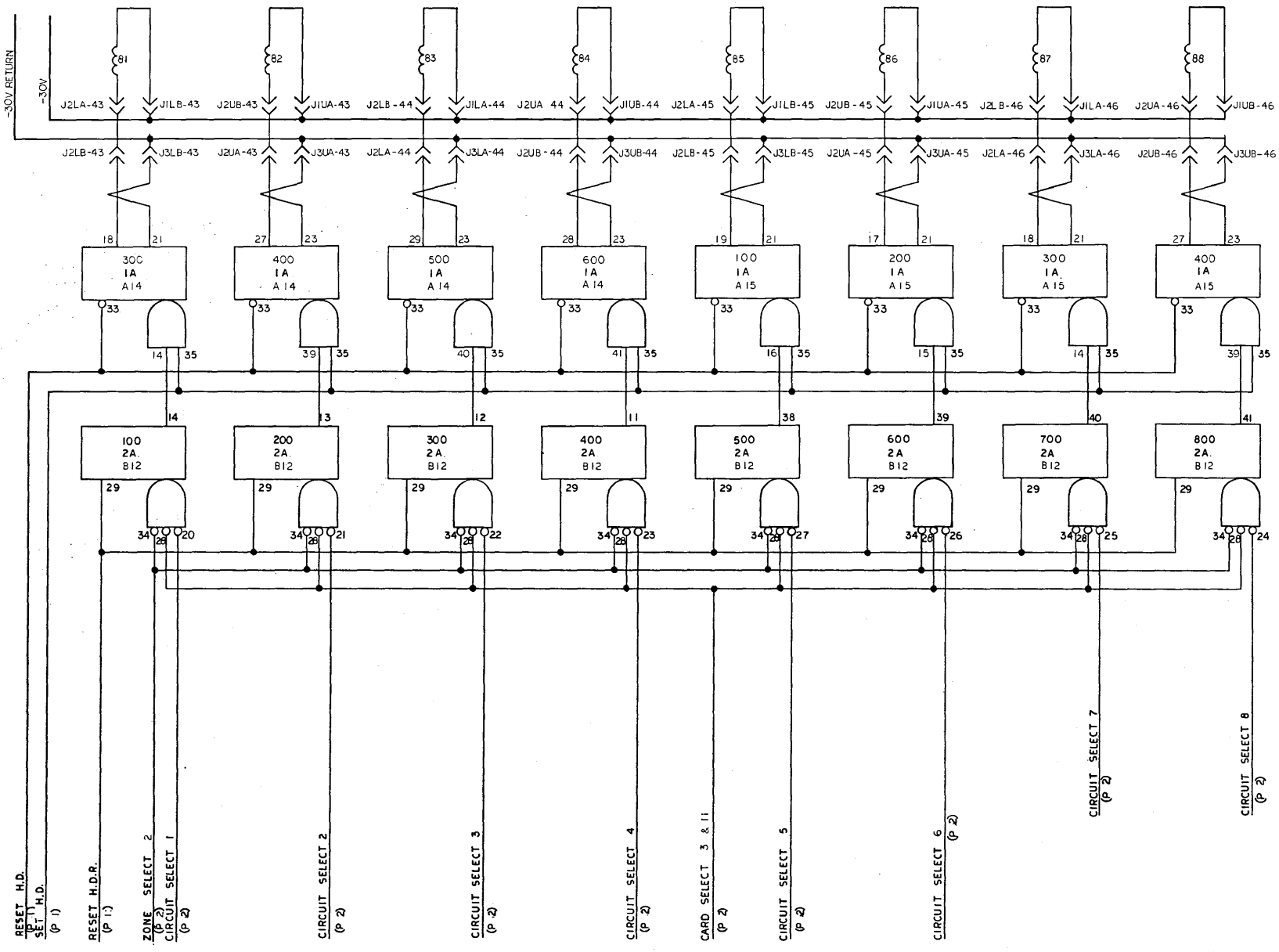


data products corporation
CULVER CITY, CALIFORNIA

TITLE LOGIC DIAGRAM NO. 13
HAMMER DRS & REC 73 TO 80

D | DRAWING NO. 201644 | REV A

SHEET 1 | CONT. ON

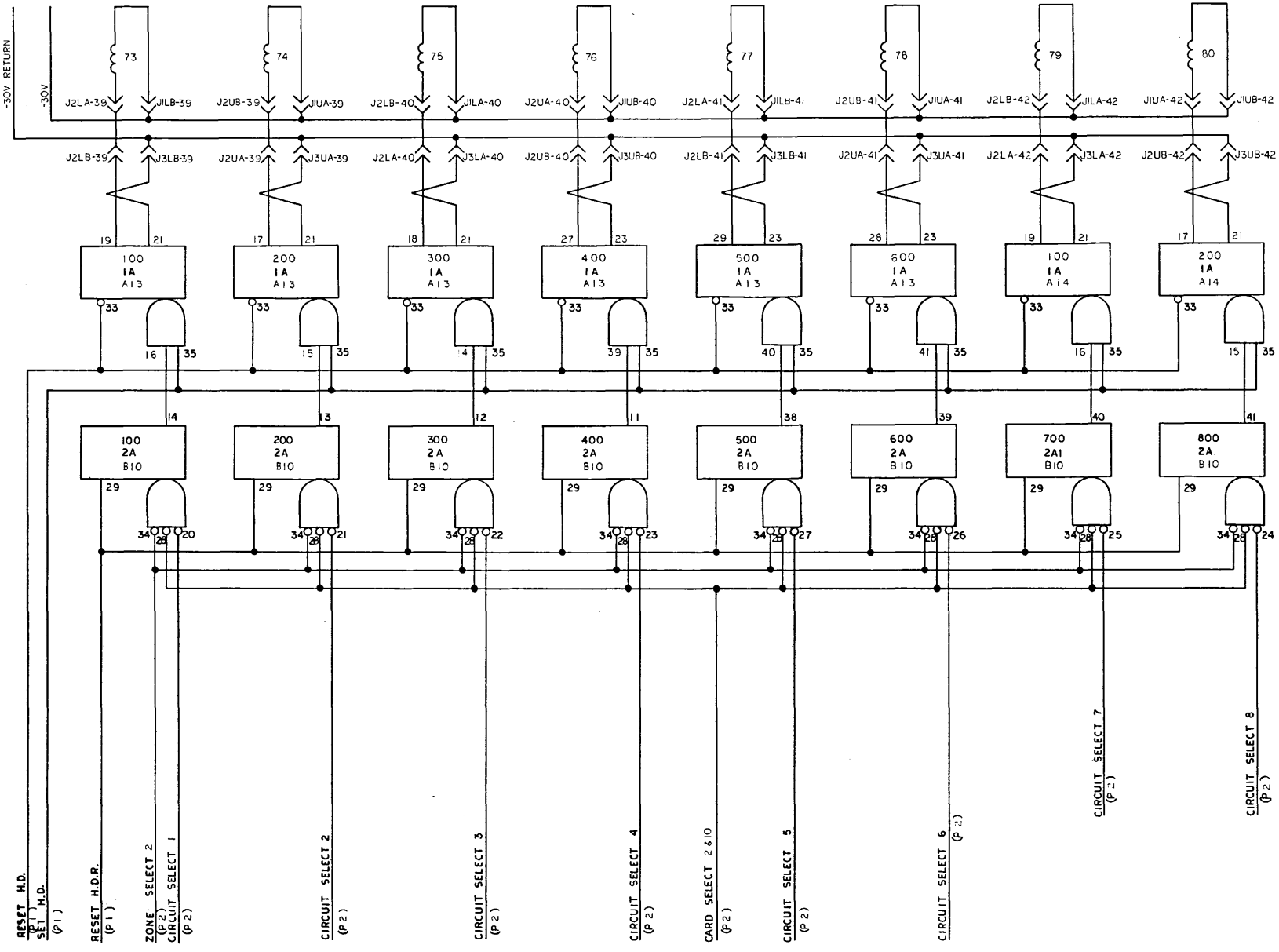


data products corporation
CULVER CITY, CALIFORNIA

TITLE LOGIC DIAGRAM NO 14
HAMMER DRS & REC 81 TO 88

D | DRAWING NO. 201645 | REV A

SHEET 1 CONT. ON

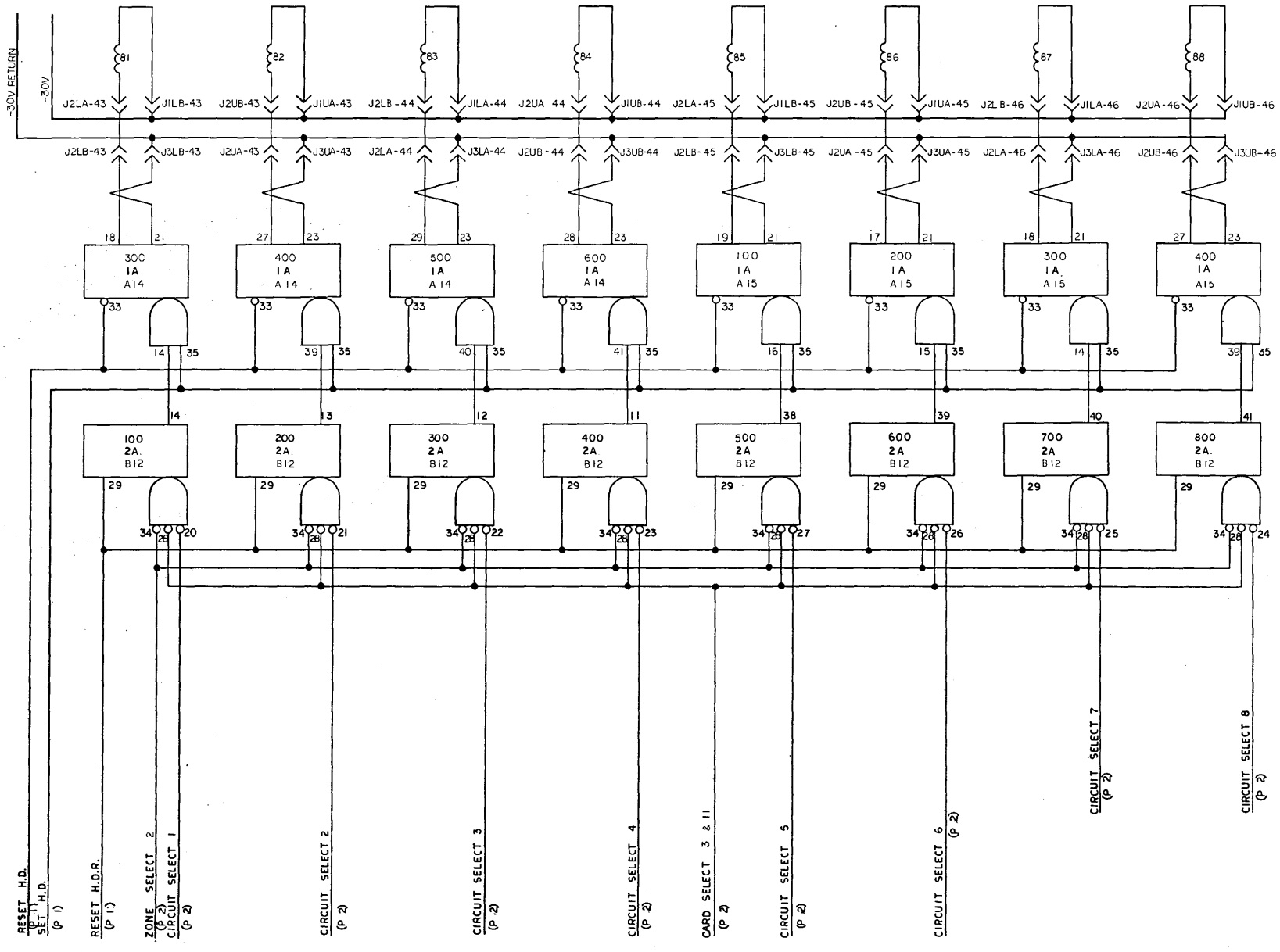


data products corporation
CULVER CITY, CALIFORNIA

TITLE LOGIC DIAGRAM NO. 13
HAMMER DRS & REC 73 TO 80

D | DRAWING NO. 201644 | REV A

SHEET 1 CONT. ON

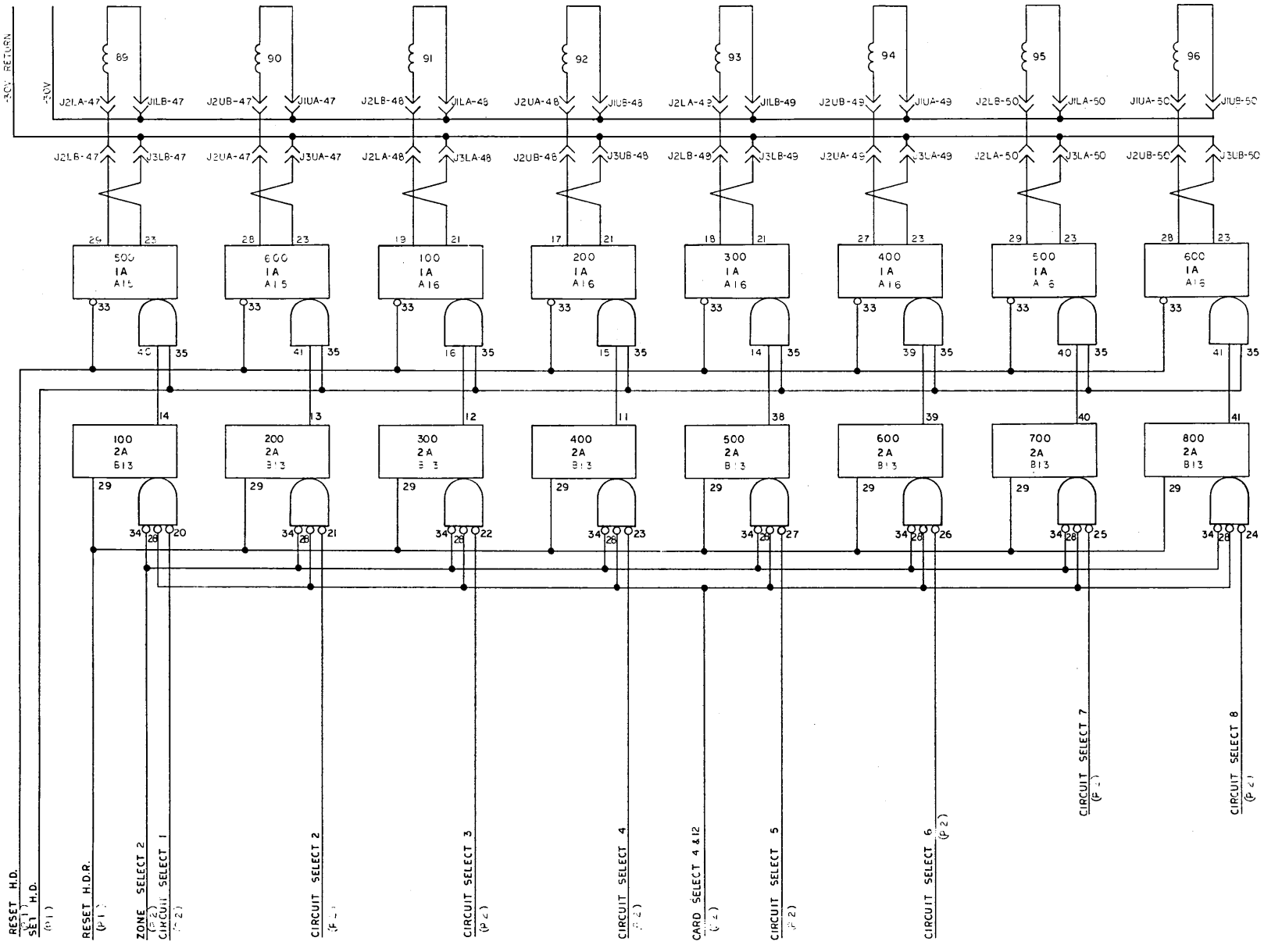


data products corporation
CULVER CITY, CALIFORNIA

TITLE: LOGIC DIAGRAM NO 14
HAMMER DRS & REC 81 TO 88

D | DRAWING NO. 201645 | REV A

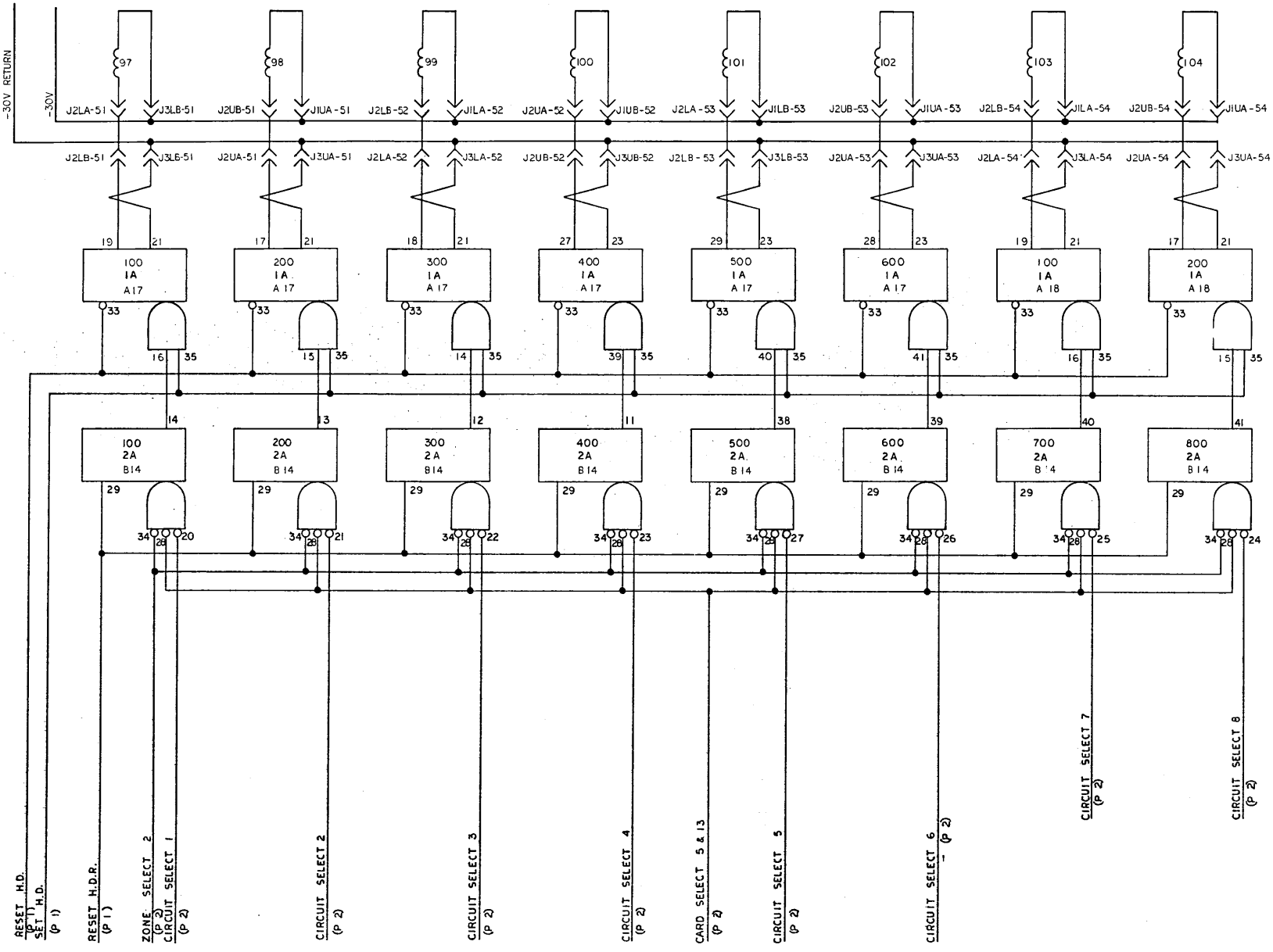
SHEET 1 | CONT. ON



data products corporation
CULVER CITY, CALIFORNIA

TITLE: LOGIC DIAGRAM NO. 15
HAMMER DRS & REC 89 TO 96

D | DRAWING NO. 201646 | REV A
SHEET 1 CONT. ON



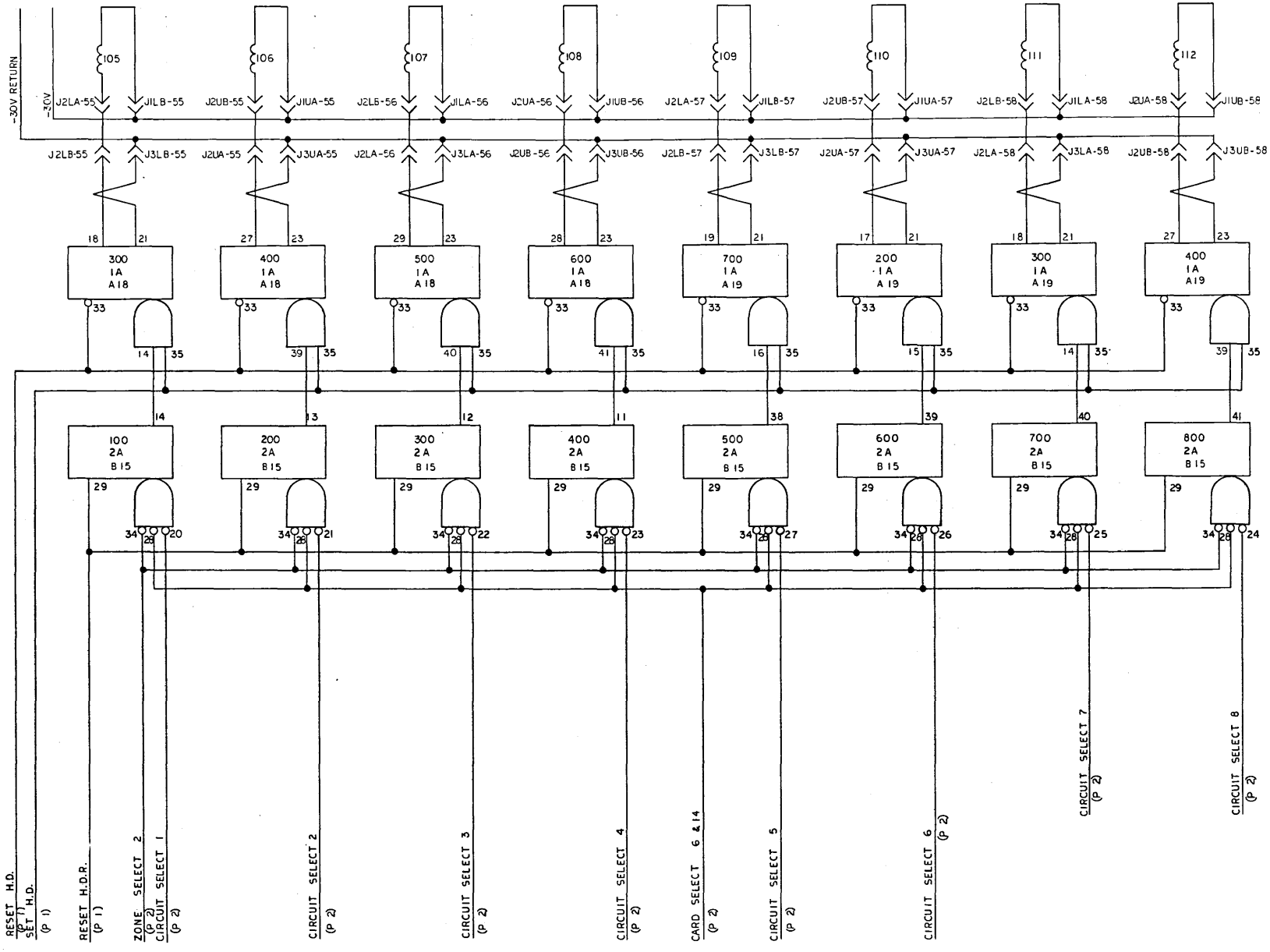
data products corporation
CULVER CITY, CALIFORNIA

TITLE: LOGIC DIAGRAM NO 16
HAMMER DRS & REC 97 TO 104

D | DRAWING NO. 201647 | REV A

SHEET 1 | CONT. ON

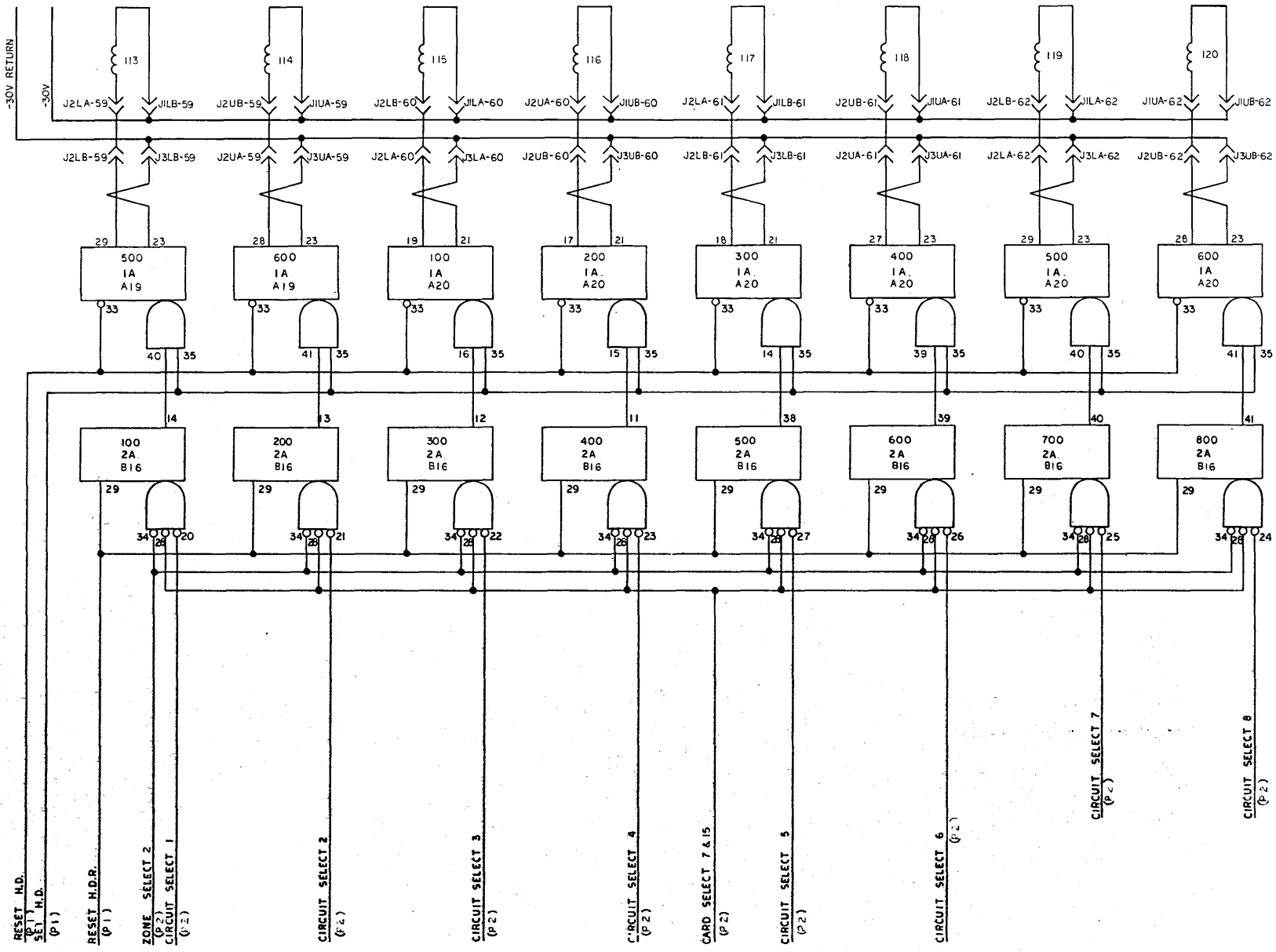
1



data products corporation
CULVER CITY, CALIFORNIA

TITLE
LOGIC DIAGRAM NO 17
HAMMER DRS & REC 105 TO 112

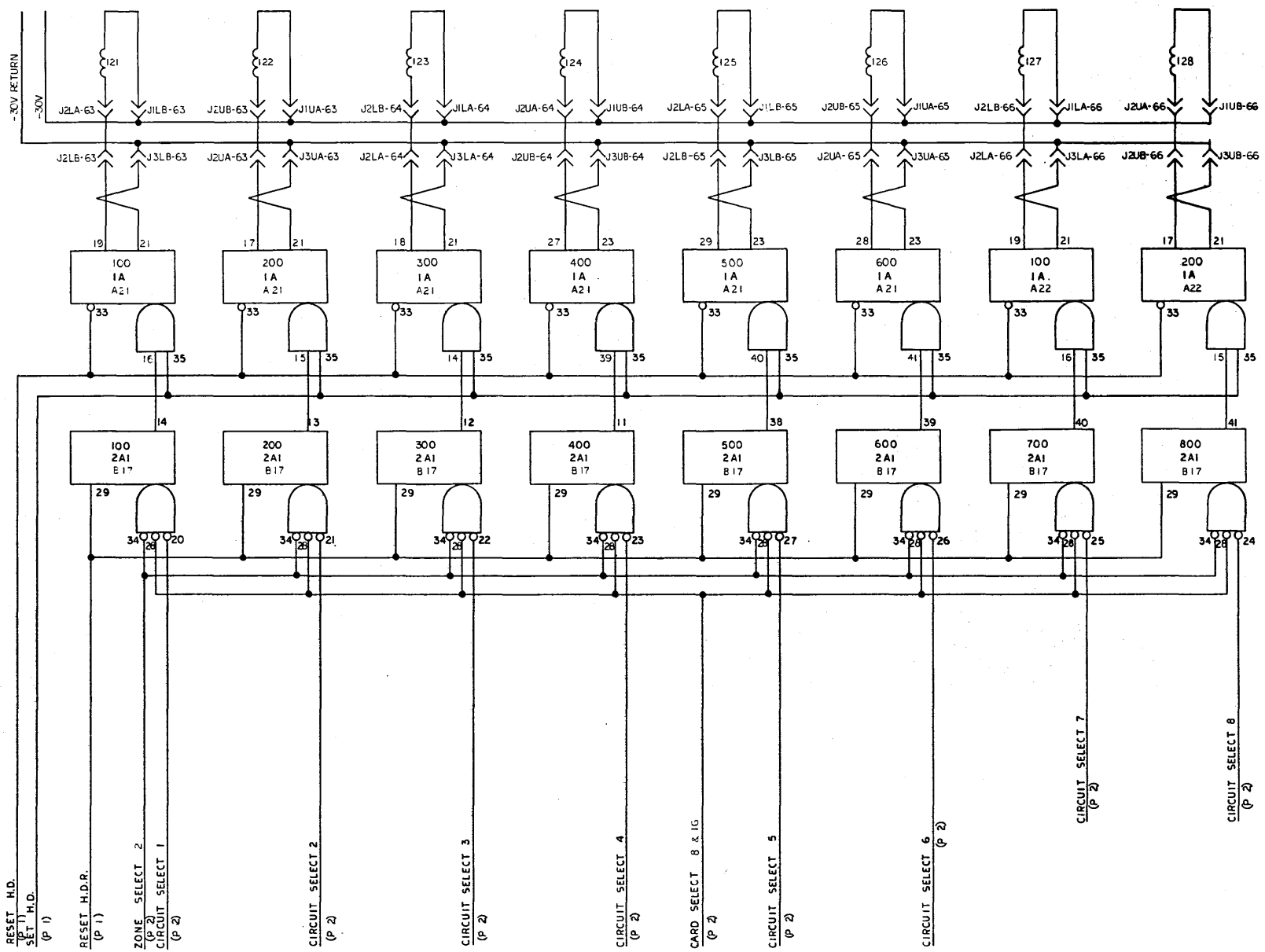
D | DRAWING NO. 201648 | REV A
SHEET 1 | CONT. ON



data products corporation
CULVER CITY, CALIFORNIA

TITLE: LOGIC DIAGRAM NO 18
HAMMER DRS & REC 113 TO 120

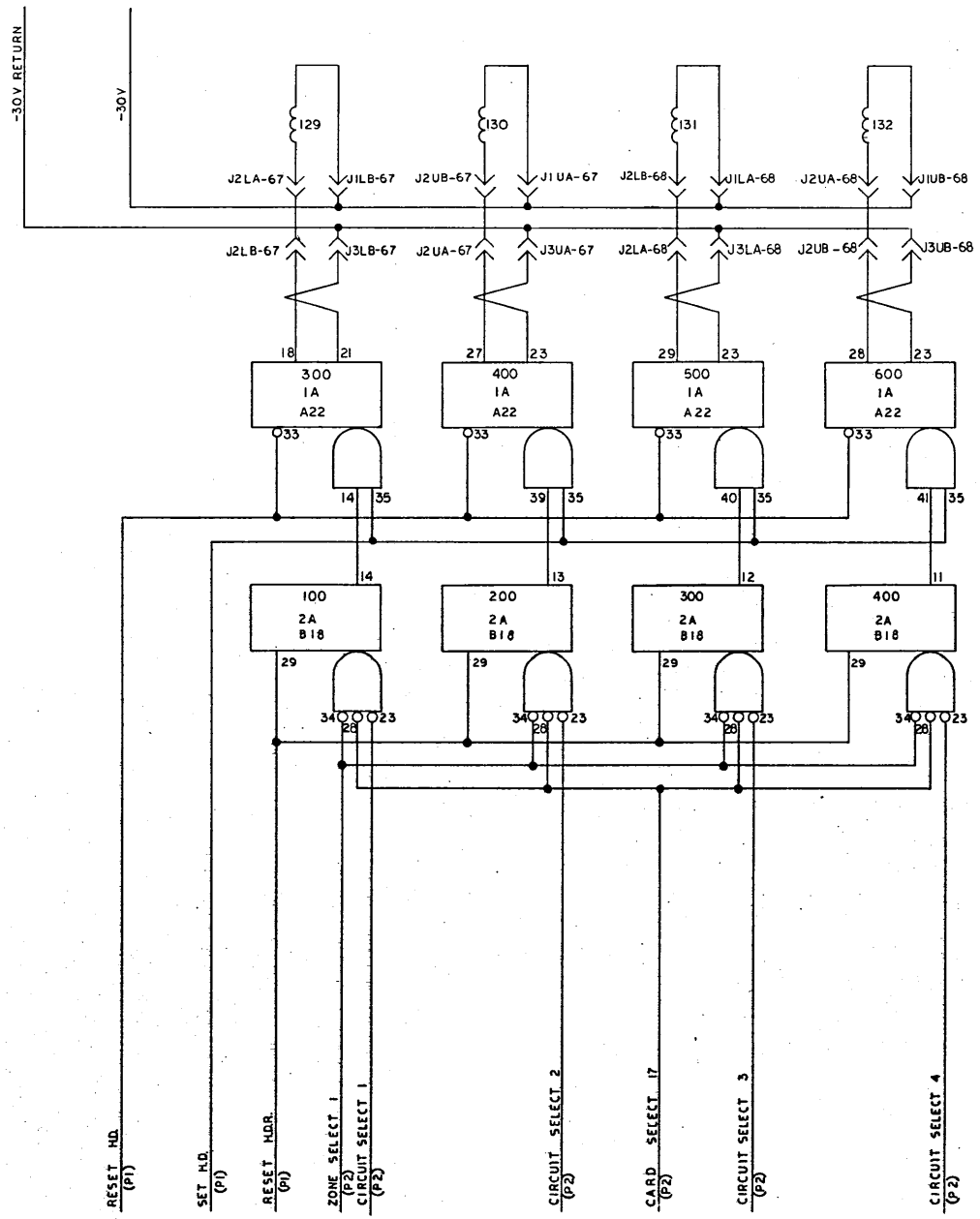
D | 201649 | A



data products corporation
CULVER CITY, CALIFORNIA

TITLE: LOGIC DIAGRAM NO. 19
HAMMER DRS & REC 121 TO 128

D	DRAWING NO. 201650	REV A
	SHEET 1 CONT. ON	

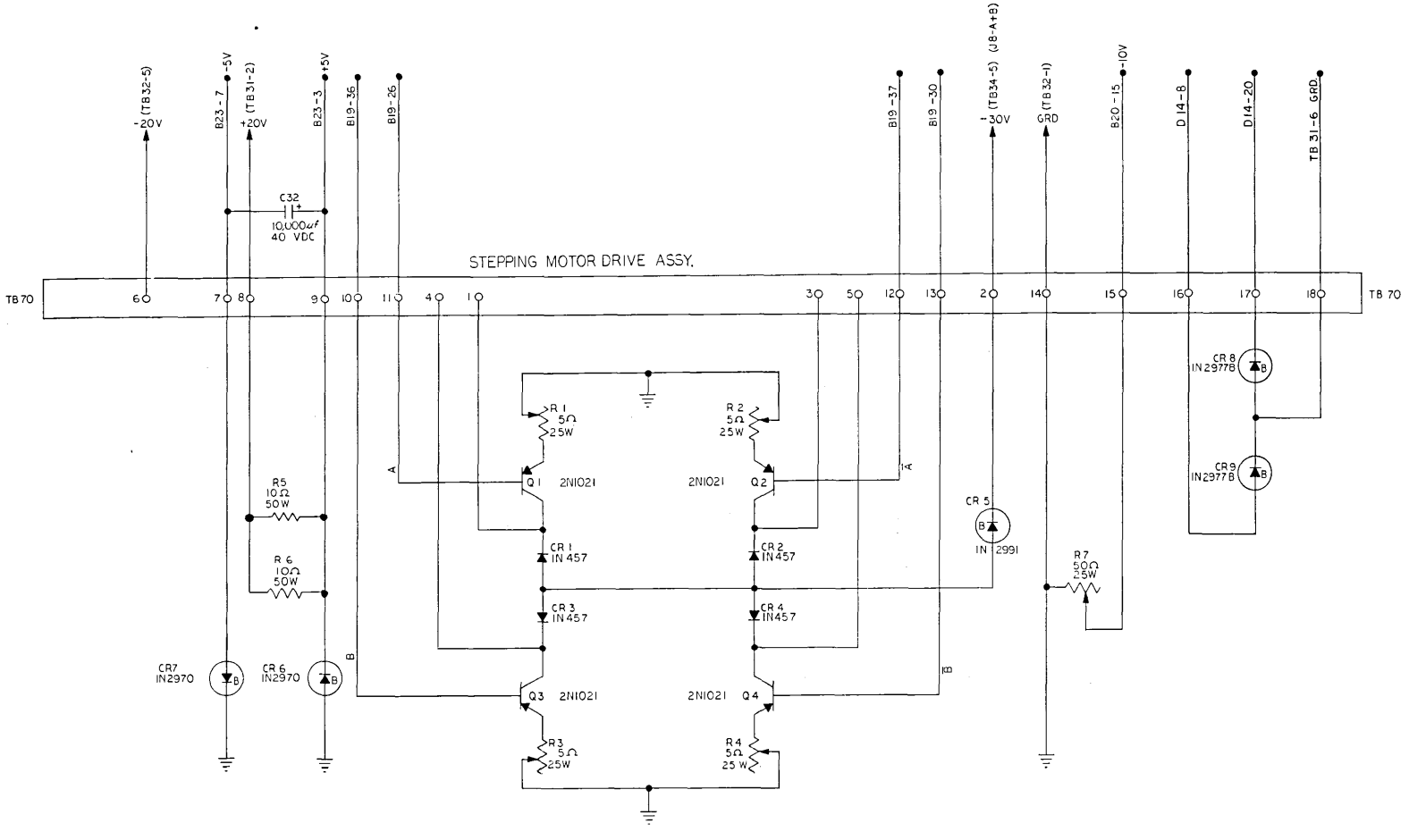


data products corporation
CULVER CITY, CALIFORNIA

TITLE: LOGIC DIAGRAM NO.20
HAMMER DRS & REC. 129 TO 132

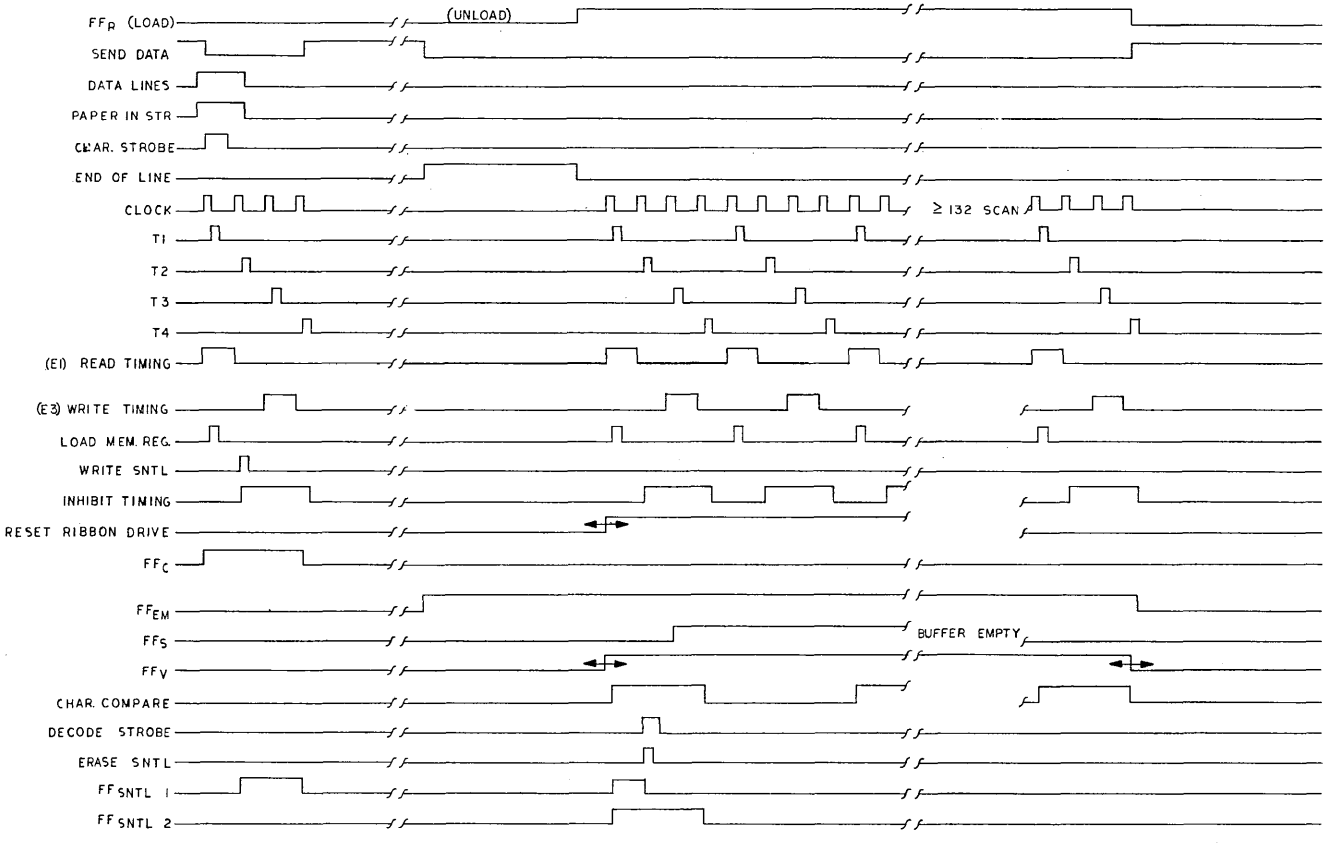
D | DRAWING NO. 201651 | REV. A

SHEET 1 | CONT. ON



D	DRAWING NO. 201652	REV D

SCALE NONE DO NOT SCALE DWG ALL DIMENSIONS ARE IN INCHES TOLERANCES UNLESS OTHERWISE NOTED DECIMAL ± FRACTION ± ANGLE ±	data products corporation CULVER CITY, CALIFORNIA TITLE SCHEMATIC DIAGRAM NO.21 PAPER FEED	
	D DRAWING NO. 201652 SHEET 1 CONT. ON ~	REV D



NOTES: UNLESS OTHERWISE SPECIFIED.

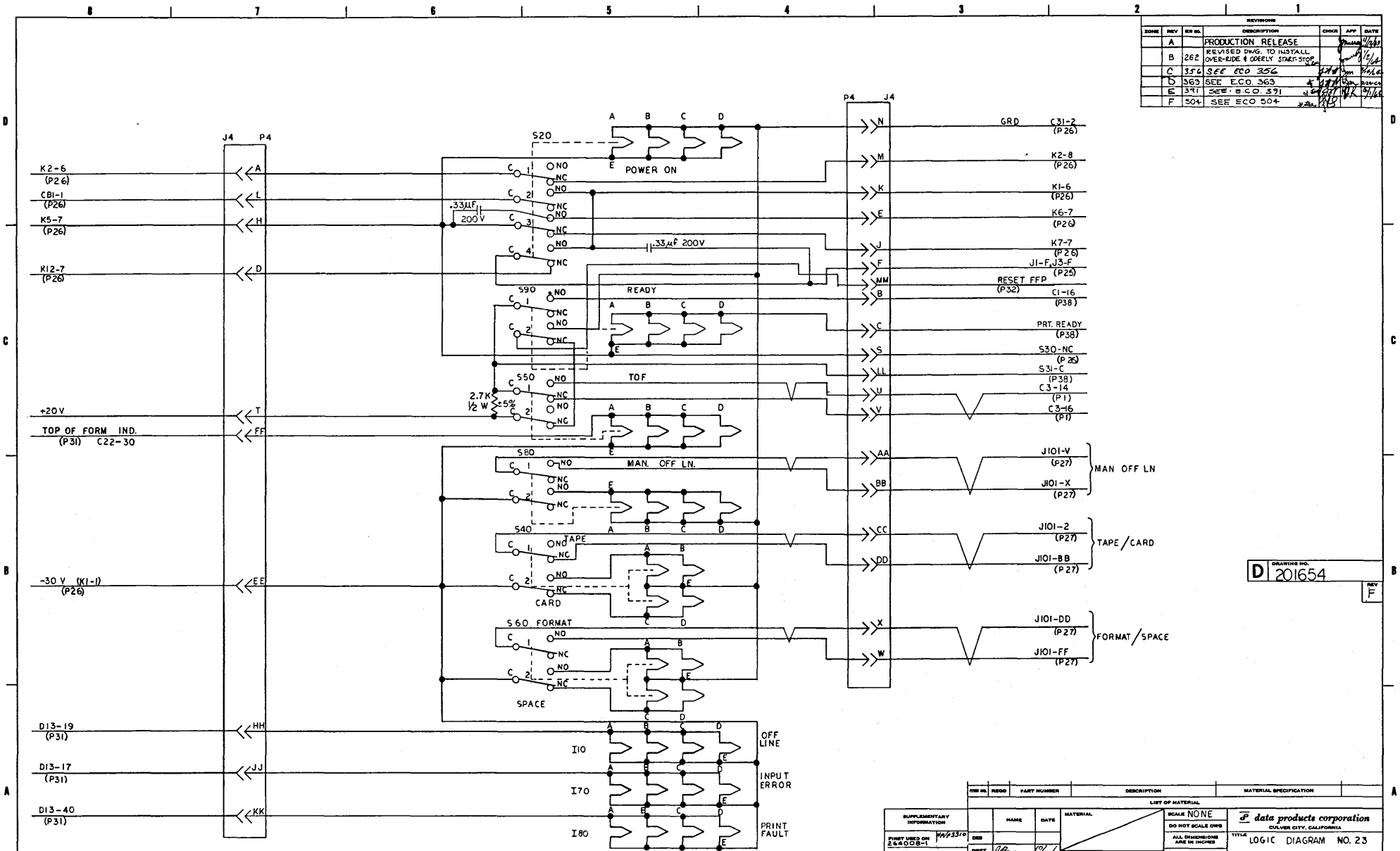
1. ALL WAVE FORMS ARE SHOWN TRUE POSITIVE FOR CLARITY.

data products corporation
CULVER CITY, CALIFORNIA

TITLE TIMING DIAGRAM
PRINTER BUFFER

D | DRAWING NO. 201653 | REV A

SHEET 1 CONT. ON



ZONE	REV	ECR NO.	DESCRIPTION	CHKR	APP	DATE
	A		PRODUCTION RELEASE			11/1/63
	B	262	REVISED DWG. TO INSTALL OVER-RIDE & ODDERLY STAFF-STOP			11/1/64
	C	356	SEE ECO 356			3/1/65
	D	363	SEE ECO. 363			3/1/65
	E	391	SEE ECO. 391			7/1/65
	F	504	SEE ECO 504			11/1/67

D 201654 REV F

NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL LAMPS ARE CHICAGO MINIATURE NO. 327 OR EQUIVALENT.

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

LIST OF MATERIAL

SUPPLEMENTARY INFORMATION
FIRST USED ON 264008-1 10/15/64
NEXT ASSEMBLY

	NAME	DATE
DES		
DRFT		10/15/64
CHKR		11/4/64
APP		11/4/64
APP		11/4/64

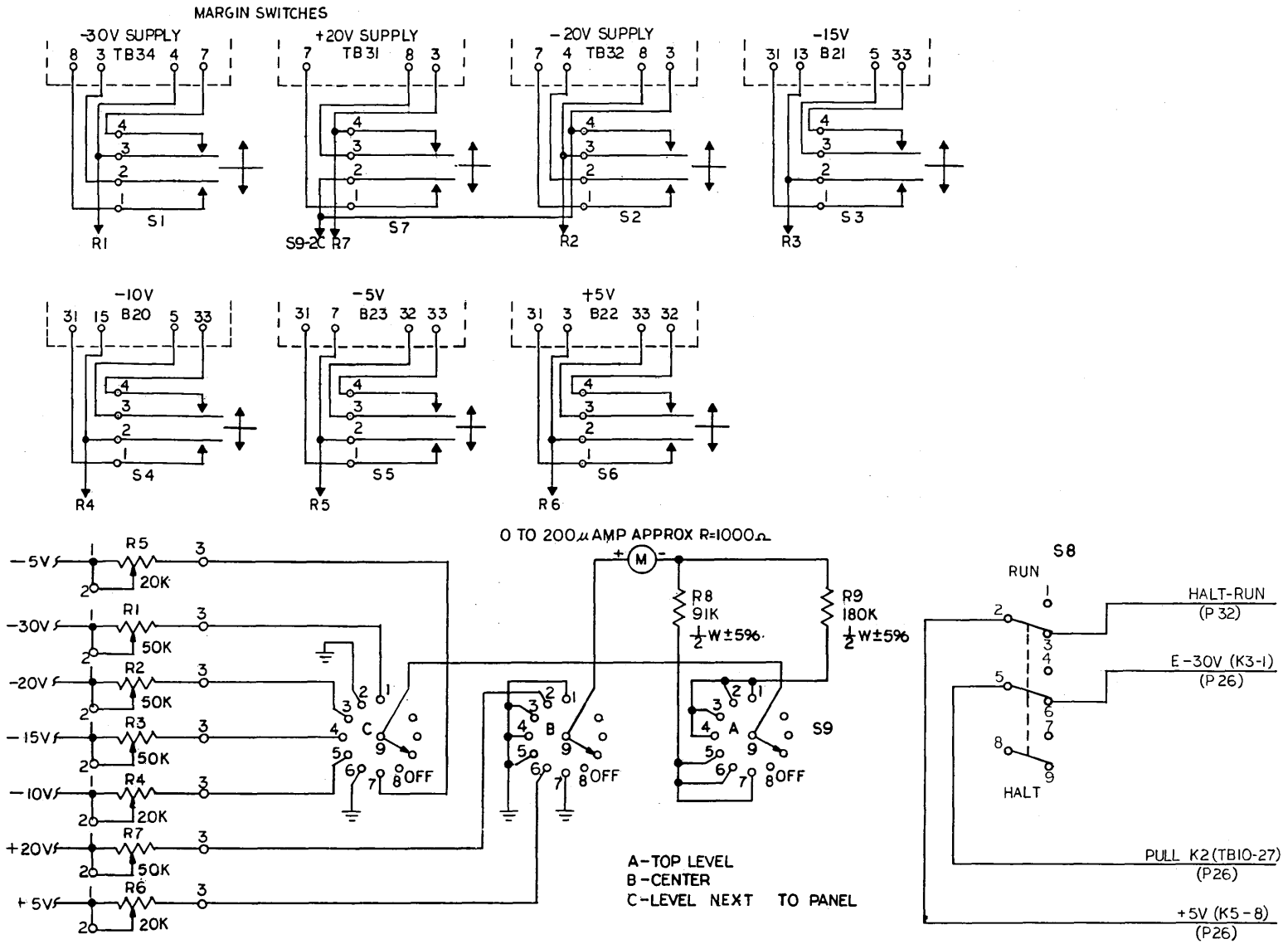
MATERIAL
FINISH
DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

SCALE NONE
DO NOT SCALE DWG
ALL DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL ±
FRACTION ±
ANGLE ±

data products corporation
CULVER CITY, CALIFORNIA

TITLE LOGIC DIAGRAM NO. 23
CONTROL PANEL

D DRAWING NO. 201654 REV F
SHEET 1 CONT. ON

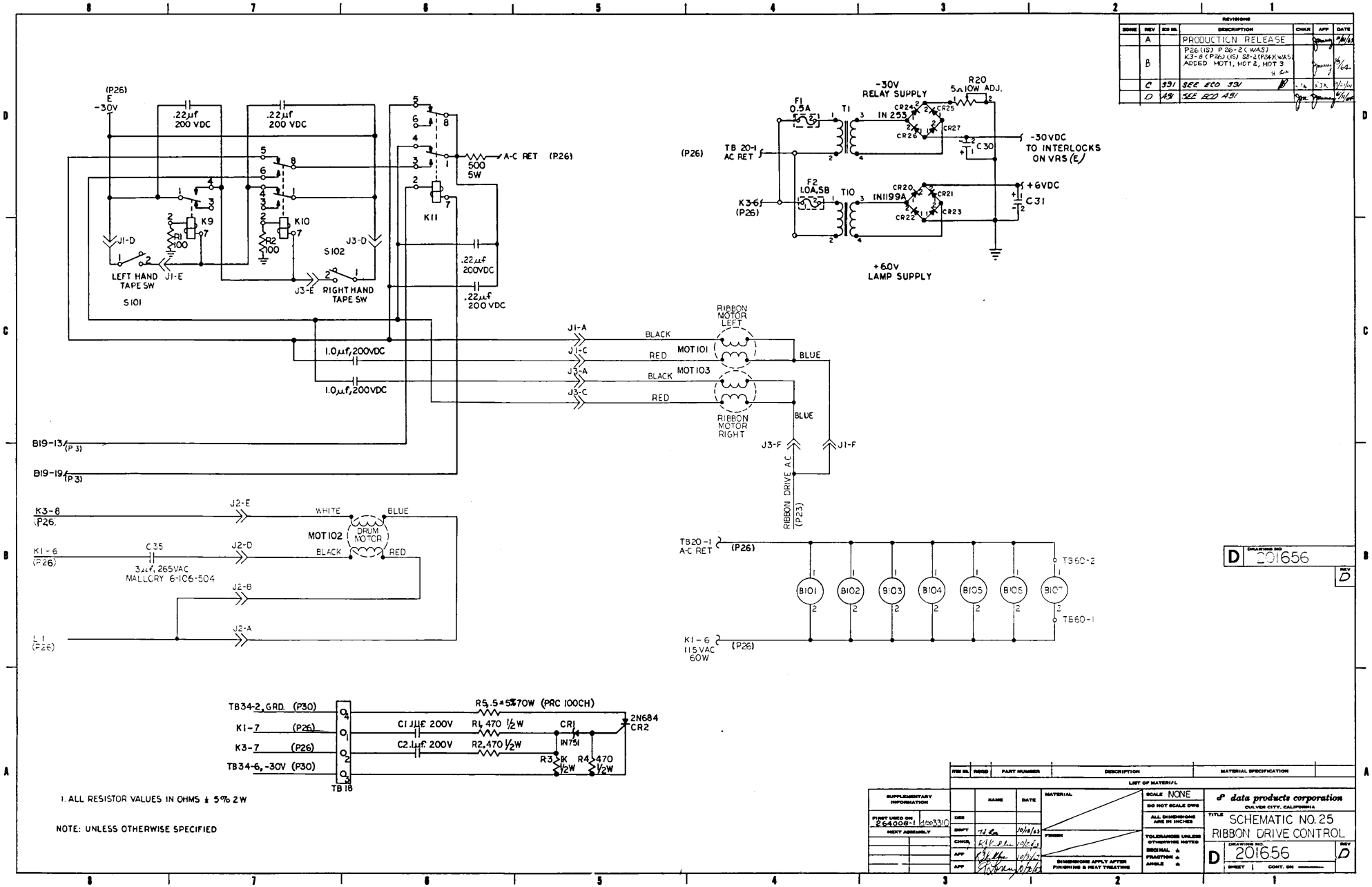


1. ALL POTENTIOMETERS ±10% 1/2 WATT
NOTE: UNLESS OTHERWISE SPECIFIED

dP data products corporation
CULVER CITY, CALIFORNIA

TITLE: SCHEMATIC NO.24
MAINTENANCE PANEL

C | DRAWING NUMBER 201655 | REV. B



ZONE	REV	ECO NO.	DESCRIPTION	CHKR	APP	DATE
	A		PRODUCTION RELEASE			9/6/63
	B		P26 (15) P 26-2 (WAS) K3-8 (P26) (15) 58-2 (P24) (WAS) ADDED MOT1, MOT 2, MOT 3			9/64
	C	331	SEE ECO 331			7/1/64
	D	491	SEE ECO 491			6/1/66

D 201656 REV D

1. ALL RESISTOR VALUES IN OHMS ± 5% 2W

NOTE: UNLESS OTHERWISE SPECIFIED

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

LIST OF MATERIAL

SUPPLEMENTARY INFORMATION		NAME	DATE
FIRST USED ON 264008-1 dtd 3310	DES		
NEXT ASSEMBLY	DRFT	T.L.	10/8/63
	CHKR	K.K. P.L.	10/8/63
	APP		10/8/63
	APP		10/8/63

MATERIAL — FINISH — DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

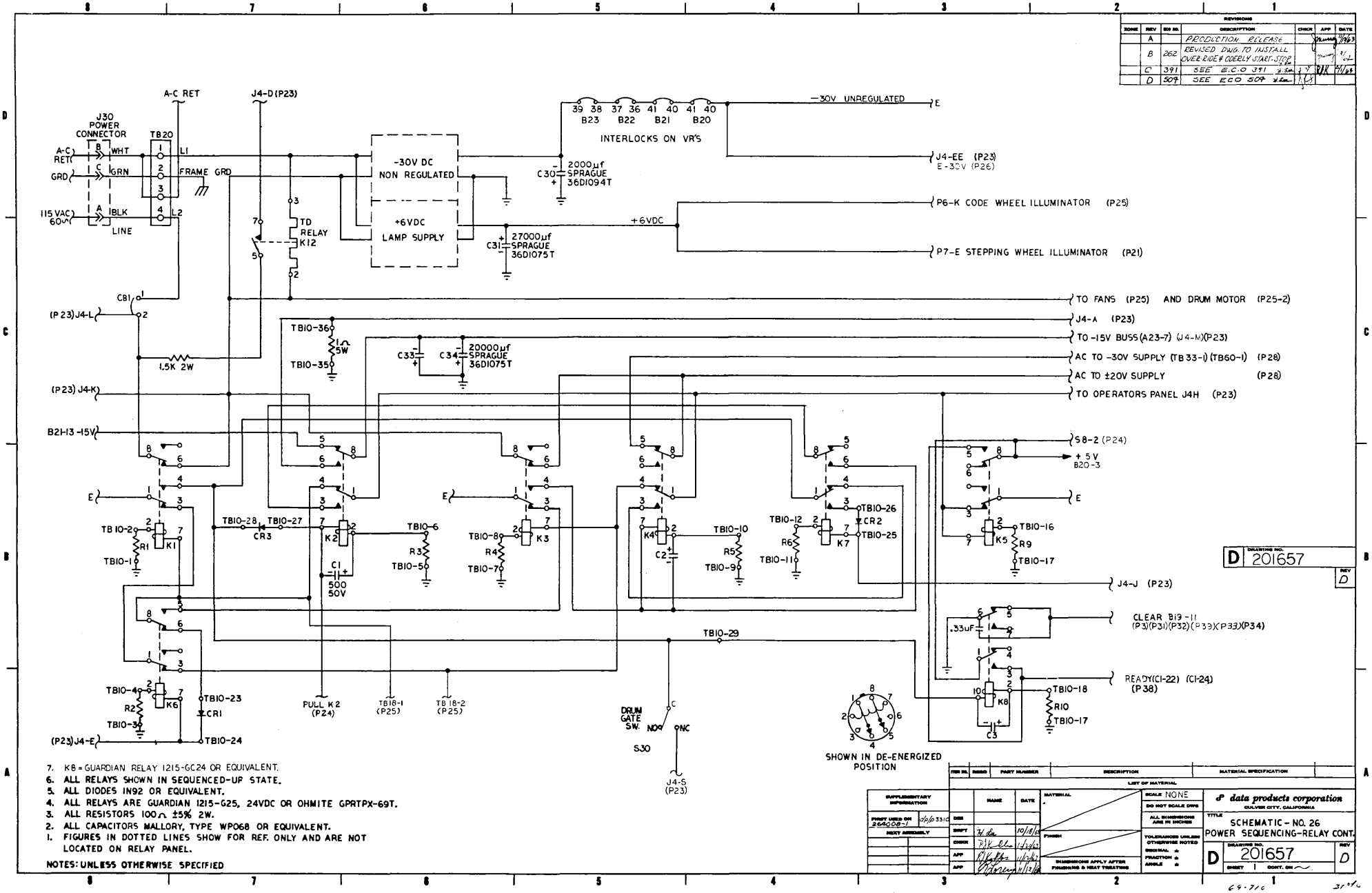
SCALE NONE — DO NOT SCALE DWG — ALL DIMENSIONS ARE IN INCHES — TOLERANCES UNLESS OTHERWISE NOTED — DECIMAL ± — FRACTION ± — ANGLE ±

data products corporation
CULVER CITY, CALIFORNIA

TITLE SCHEMATIC NO. 25
RIBBON DRIVE CONTROL

DRAWING NO. D 201656 REV D

SHEET 1 CONT. ON ——



7. K8 = GUARDIAN RELAY 1215-GC24 OR EQUIVALENT.
6. ALL RELAYS SHOWN IN SEQUENCED-UP STATE.
5. ALL DIODES IN92 OR EQUIVALENT.
4. ALL RELAYS ARE GUARDIAN 1215-G25, 24VDC OR OHMITE GPRTPX-69T.
3. ALL RESISTORS 100Ω ±5% 2W.
2. ALL CAPACITORS MALLORY, TYPE WP068 OR EQUIVALENT.
1. FIGURES IN DOTTED LINES SHOW FOR REF. ONLY AND ARE NOT LOCATED ON RELAY PANEL.

NOTES: UNLESS OTHERWISE SPECIFIED

ZONE	REV	ECO NO.	DESCRIPTION	CHECK	APP	DATE
	A		PRODUCTION RELEASE			11/63
	B	262	REVISED DWG. TO INSTALL OVER-RIDE & COERLY START-STOP			3/64
	C	391	SEE E.C.O 391			11/64
	D	509	SEE ECO 509			

	NAME	DATE
DES		
DRFT	H. Lee	10/8/63
CHKR	R.K. Lee	11/13/63
APP	R.K. Lee	11/13/63
APP	[illegible]	11/13/63

SUPPLEMENTARY INFORMATION: FIRST USED ON 264000-1 dp/p 331C; NEXT ASSEMBLY

MATERIAL | FINISH | DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

SCALE NONE | DO NOT SCALE DWG | ALL DIMENSIONS ARE IN INCHES | TOLERANCES UNLESS OTHERWISE NOTED: DECIMAL ± | FRACTION ± | ANGLE ±

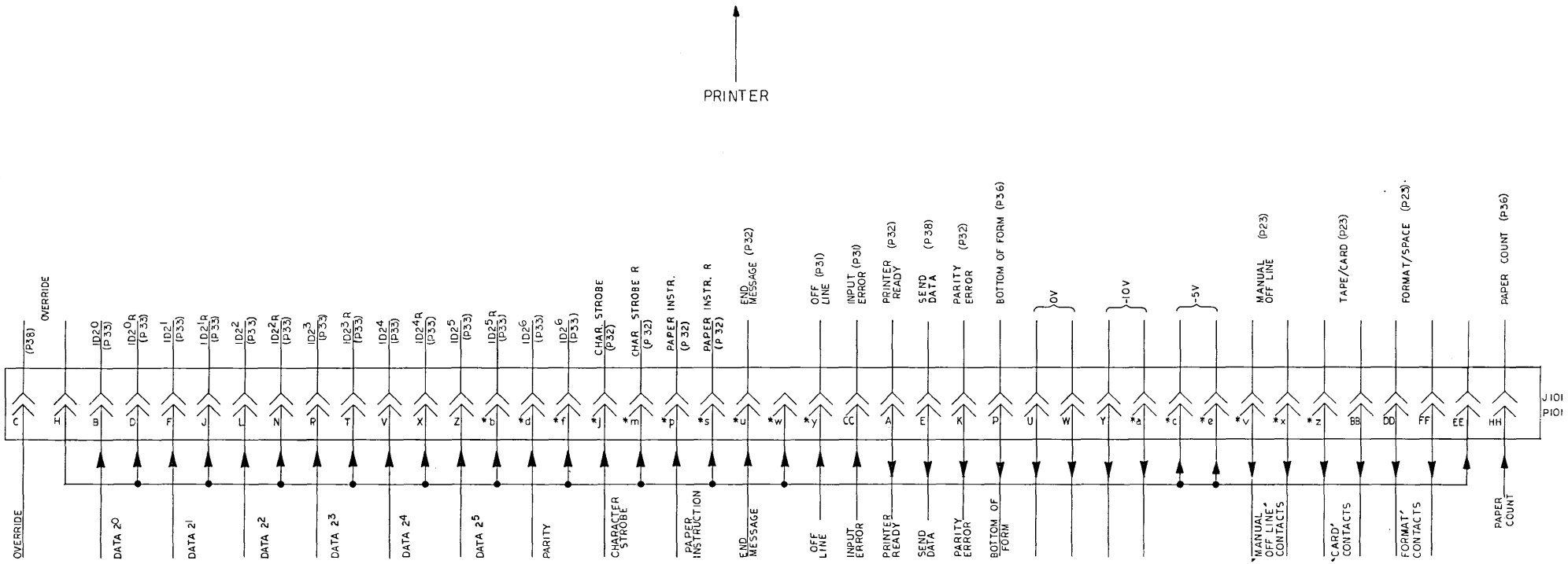
d data products corporation
CULVER CITY, CALIFORNIA

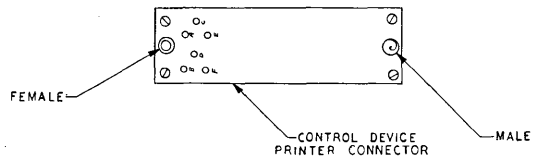
TITLE: SCHEMATIC - NO. 26
POWER SEQUENCING-RELAY CONT.

D 201657 REV D

SHEET 1 CONT. ON ~

69-716 31 1/2

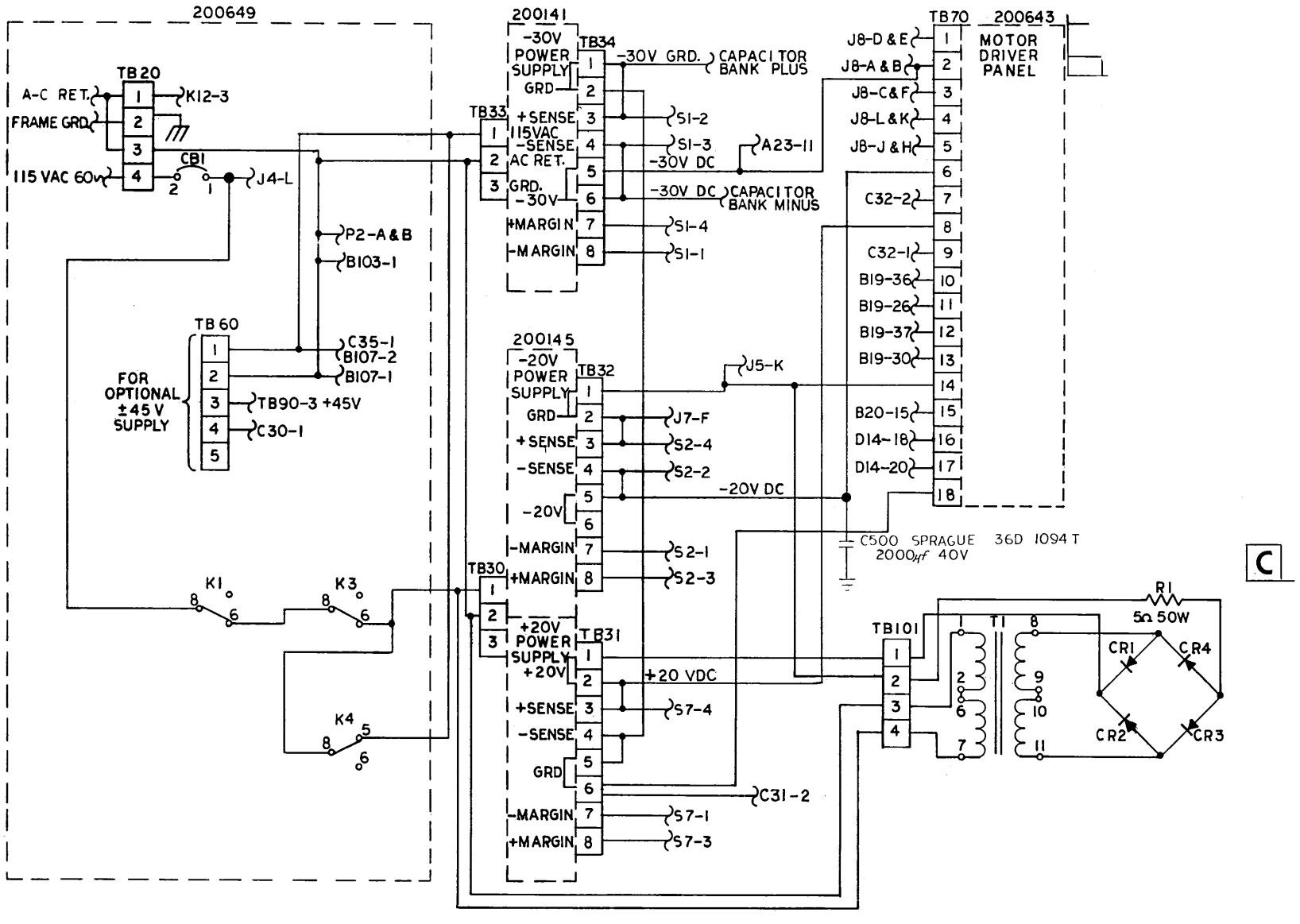




4. CONTROL DEVICE USE 100-1020P FOR JUMPERS IN NOTE #3, WITH EXCEPTION TO INSTALLATION OF ONE WIRE IN A PIN THEN USE 100-1022P.
3. PINS H,D,J,N,T,X,*b,*f,*m,*s,*w,*c,*e,EE TO BE JUMPERED ON CUSTOMER PLUG. USE 22 AWG WIRE STRANDED.
2. CONTROL DEVICE GRD TO BE CONNECTED TO PINS Y&*a, USE 22AWG WIRE, STRANDED.
1. CONNECTOR TYPE WINCHESTER ELECTRONICS 50P JTCH-1.

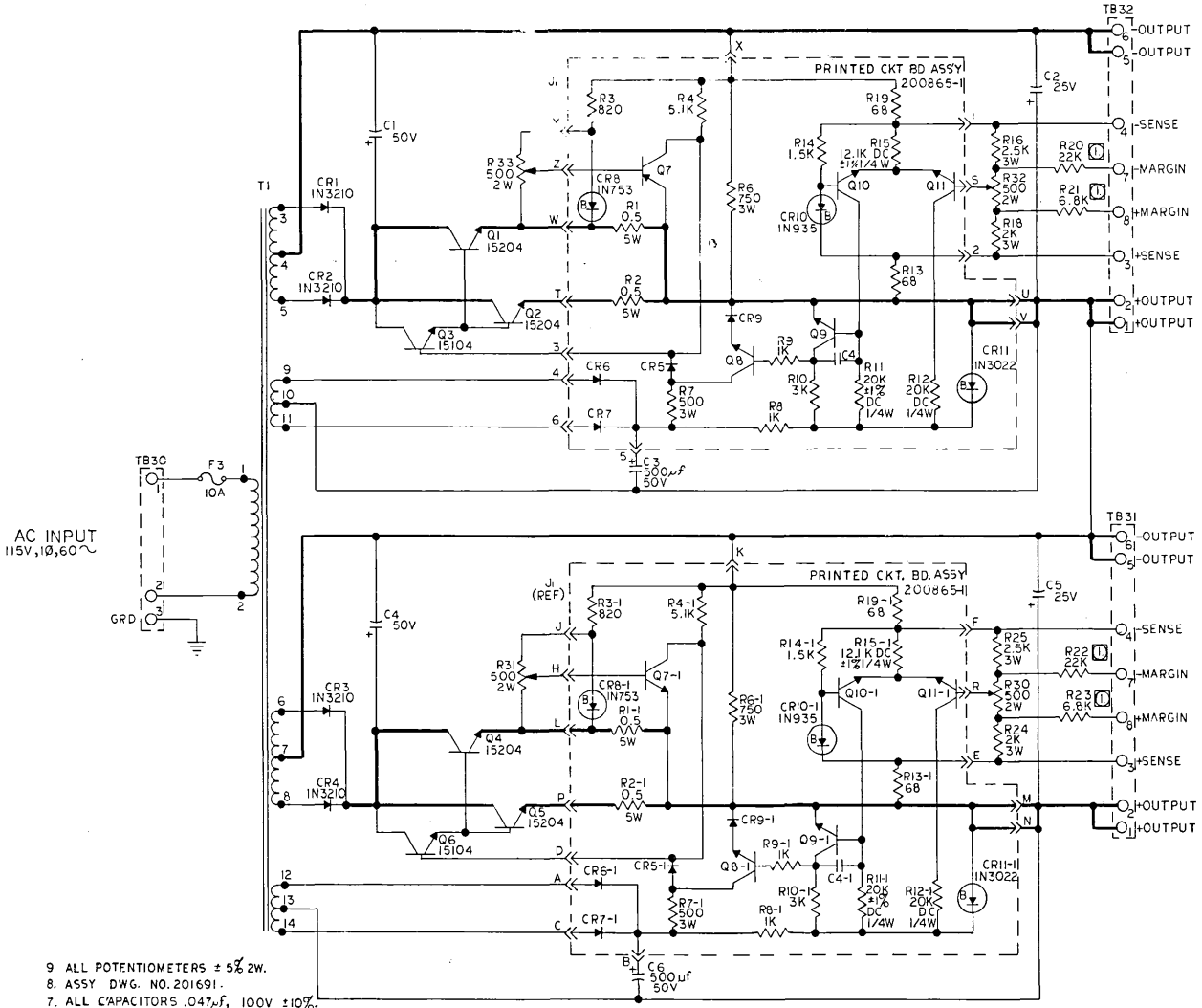
NOTES: UNLESS OTHERWISE SPECIFIED.

data products corporation, CULVER CITY, CALIFORNIA		
TITLE LOGIC DIAGRAM — 27 INPUT/OUTPUT CONNECTOR		
D	DRAWING NO. 201658	REV C
	SHEET 1 CONT. ON	



2. DRAWING NO. FOR POWER SUPPLIES ARE SHOWN ABOVE DOTTED BLOCKS.
1. DOTTED BLOCKS SHOWN FOR REFERENCE ONLY.
NOTES: UNLESS OTHERWISE SPECIFIED.

data products corporation CULVER CITY, CALIFORNIA	
TITLE	DIAGRAM NO. 28 TERMINAL BUS. INTERCONNECTION
C	DRAWING NO. 201770 SHEET 1 CONT. ON —
REV	C



OUTPUT NO.1
-20V, 5A DC

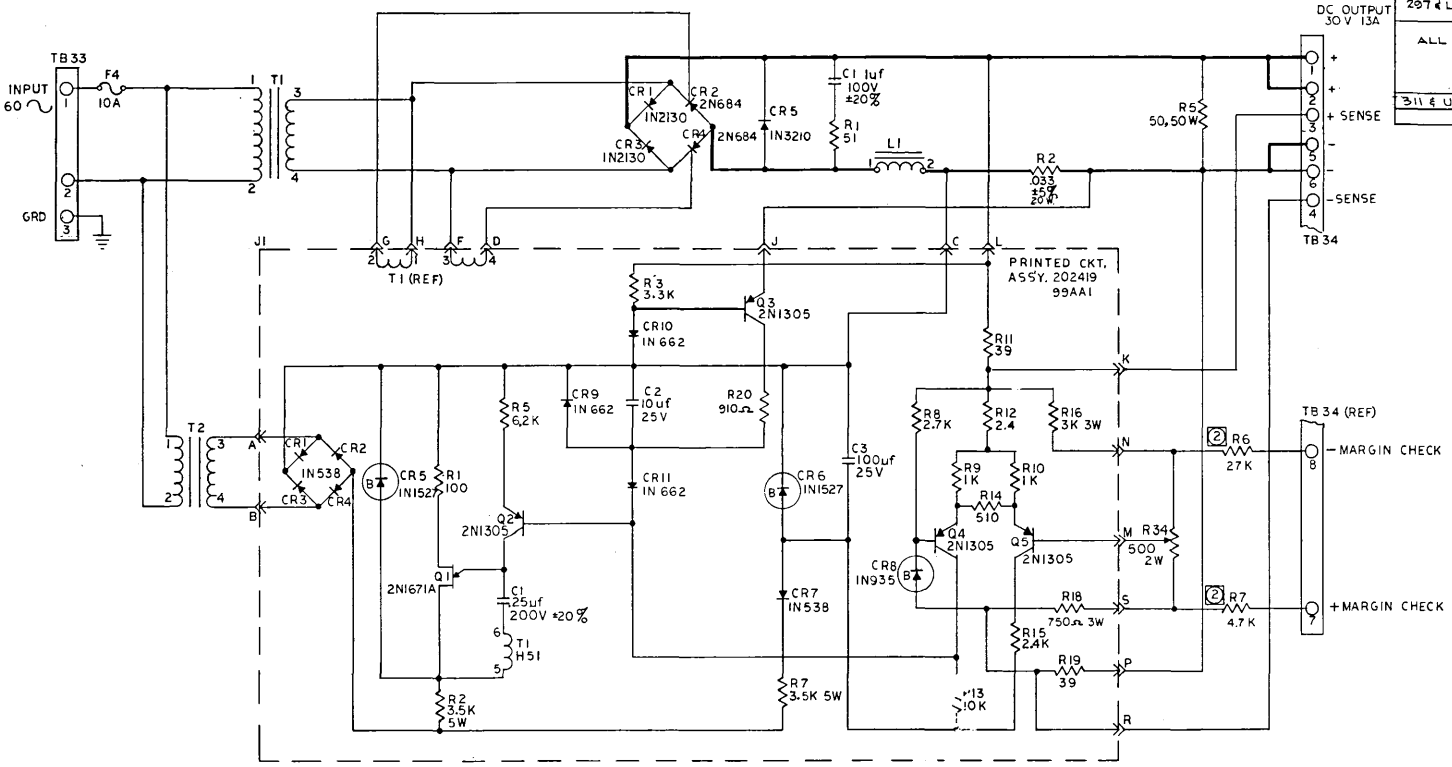
OUTPUT NO.2
+20V, 5A DC

9 ALL POTENTIOMETERS ± 5% 2W.
8. ASSY DWG. NO. 201691.
7. ALL CAPACITORS .047µf, 100V ±10%
6. ALL ELECTROLYTIC CAPACITORS 10,000µf +50%-10%.
5. ALL RESISTOR VALUES IN OHMS ±5% 1/2W
4. ALL TRANSISTORS 2N1304.
3. ALL DIODES IN538.
2. PLUS MARGIN CHECK SWITCH CONNECTS 3 & 8 (TB31 & 32)
MINUS MARGIN CHECK SWITCH CONNECTS 4 & 7 (TB31 & 32)
(1) INDICATES APPROXIMATE COMPONENT VALUES
—— ACTUAL VALUES DETERMINED IN FINAL TEST.

NOTES: UNLESS OTHERWISE SPECIFIED.

D DRAWING NO. 201659 REV C

SCALE NONE	data products corporation, CULVER CITY, CALIFORNIA
DO NOT SCALE DWG	
ALL DIMENSIONS ARE IN INCHES	TITLE SCHEMATIC NO. 29 POWER SUPPLY ±20V
TOLERANCES UNLESS THERWISE NOTED .XX DECIMAL ± FRACTION ± ANGLE ° ±	D DRAWING NO. 201659 REV C SHEET 1 CONT. ON ——



A.D.C. SERIAL EFFECTIVITY	ZONE	REV	ECO NO.	REVISIONS DESCRIPTION	CHKR	APP	DATE
123 & UP				PRODUCTION RELEASE			9/21/64
195 & UP		A		R18 WAS 250Ω, R16 WAS 2K, CR8 WAS IN753 R8 WAS 2.4K			12/4/64
		B	216	NOTE 4: 1955Y NO MARS 201689 R6.			11/27/64
257 & UP				R6 WAS 16K, R7 WAS 1.6K R18 WAS 1K.			
297 & UP		C	381	CR5 WAS IN 3208, R6 WAS 27K, R7 WAS 8.2K.			
ALL				RELOCATED R20, WAS ACROSS C2; C2 WAS 500uf 3V, CR9 WAS CD4662, CR10 WAS R4, 51 OHMS, CR11 WAS R6, 1K; R20 WAS 39Ω.			9/1/64
311 & UP		D	401	CR1 & CR3 WERE IN3210			5/19/65
		E	429	SEE ECO 429			5/19/65

4. ASSEMBLY DWG. NO. 201690.
3. MINUS MARGIN CHECK SWITCH CONNECTS TO 3 & 8 (TB34). PLUS MARGIN CHECK SWITCH CONNECTS TO 4 & 7 (TB34).
[2] COMPONENT VALUES ARE APPROXIMATE. ACTUAL VALUES DETERMINED IN FINAL TEST.
1. ALL RESISTOR VALUES IN OHMS ±5% 1/2W.
NOTES: UNLESS OTHERWISE SPECIFIED.

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

LIST OF MATERIAL

SUPPLEMENTARY INFORMATION		NAME	DATE
FIRST USED ON 254001-1	DES		
NEXT ASSEMBLY	DRFT	J. Duffy	11/5/63
	CHKR	G. Evans	10/5/64
	APP	[illegible]	10/5/64
	APP	[illegible]	11/29/65

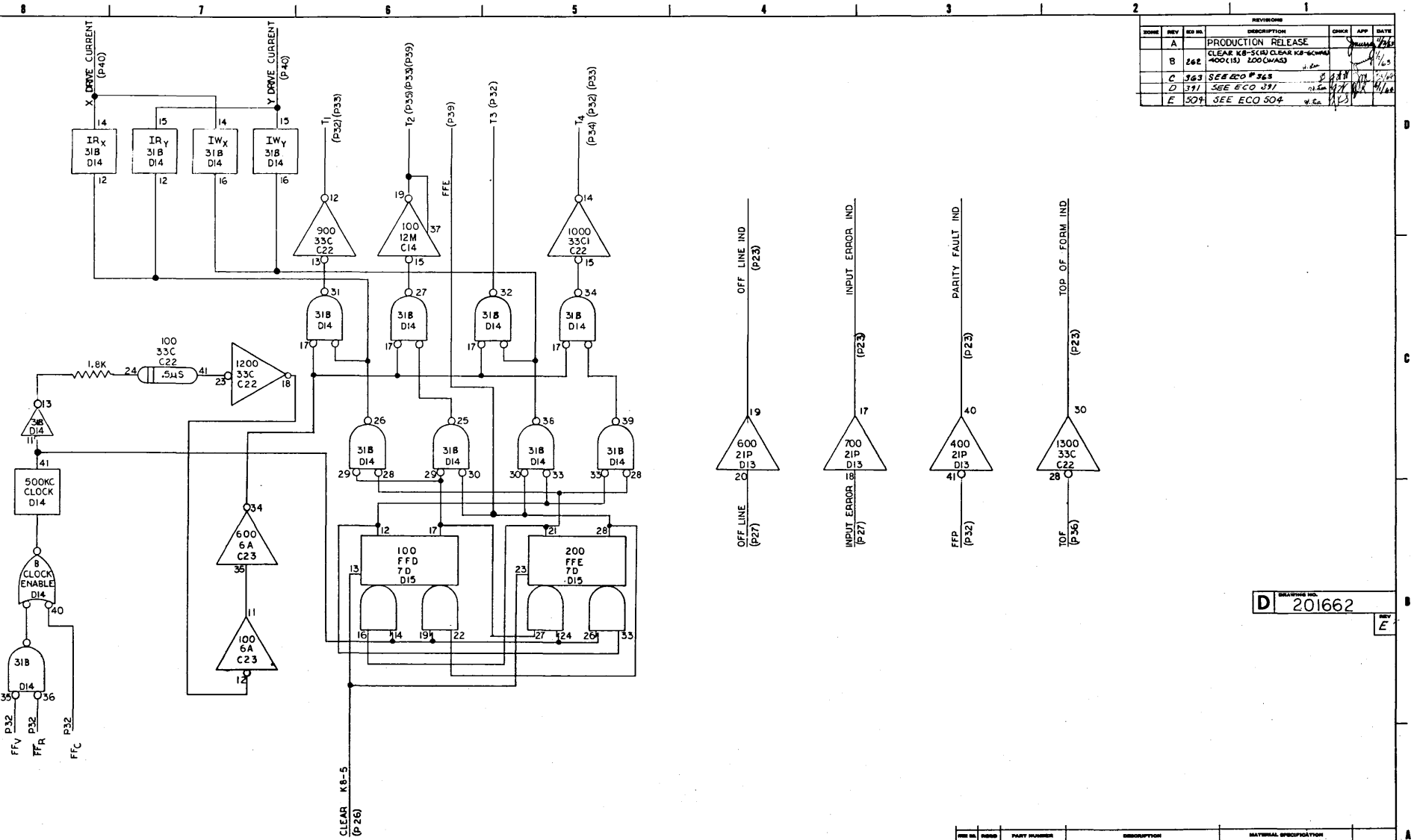
MATERIAL / FINISH / DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

SCALE NONE — DO NOT SCALE DWG — ALL DIMENSIONS ARE IN INCHES — TOLERANCES UNLESS OTHERWISE NOTED: DECIMAL ±, FRACTION ±, ANGLE ±

data products corporation
CULVER CITY, CALIFORNIA

TITLE: SCHEMATIC NO. 30 POWER SUPPLY-30V

D — DRAWING NO. 201660 — REV E — SHEET 1 — CONT. ON —



ZONE	REV	ECO NO.	DESCRIPTION	CHK'R	APP'D	DATE
	A		PRODUCTION RELEASE			9/26/63
	B	262	CLEAR K8-5(IN) CLEAR K8-6(IN) 400(IS) 200(WAS)			11/6/63
	C	363	SEE ECO # 363			2/19/64
	D	391	SEE ECO 391			4/1/64
	E	504	SEE ECO 504			

D 201662 REV E

SUPPLEMENTARY REPRESENTATION		NAME	DATE
NEXT ASSEMBLY	DES		
	DRFT	RON COLE	9-26-63
	CHK'R	R Keller	10/4/63
	APP'D	R Keller	10/4/63
	APP'D	Tommy	11/26/63

MATERIAL / FINISH / DIMENSIONS APPLY AFTER PLATING & HEAT TREATING

SCALE NONE — DO NOT SCALE DWG — ALL DIMENSIONS ARE IN INCHES — TOLERANCES UNLESS OTHERWISE NOTED: DECIMAL ±, FRACTION ±, ANGLE ±

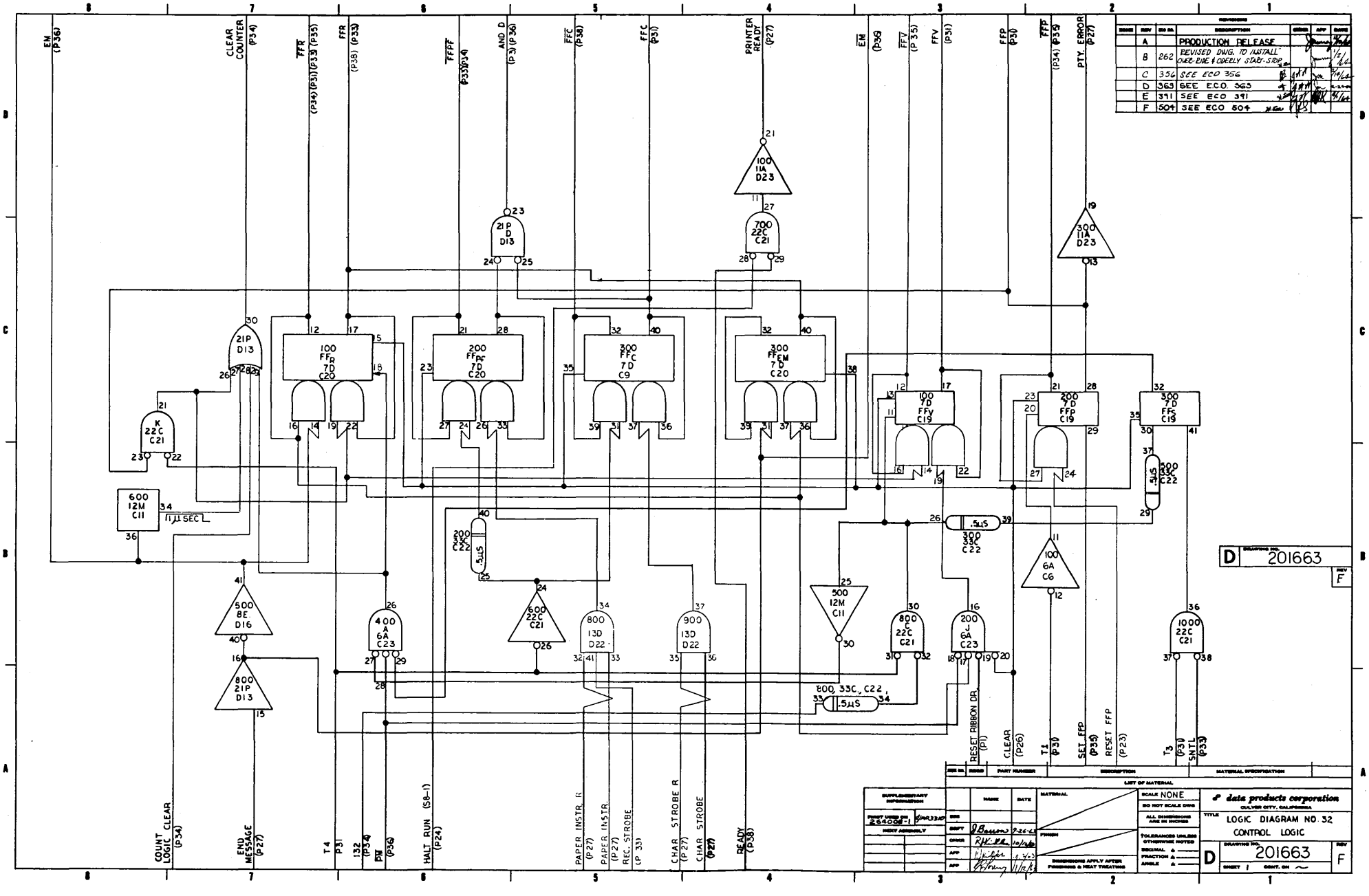
LIST OF MATERIAL

REF DES	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

data products corporation, CULVER CITY, CALIFORNIA

TITLE: LOGIC DIAGRAM NO. 31 TIMING DISTRIBUTOR

D 201662 REV E — SHEET 1 CONT. ON ~



REVISIONS					
ZONES	REV	ECO NO.	DESCRIPTION	APP'D	DATE
	A		PRODUCTION RELEASE		
	B	262	REVISED DWG. TO INSTALL OVER-RIDE & QUIETLY START-STOP		
	C	356	SEE ECO 356		
	D	363	SEE ECO 363		
	E	391	SEE ECO 391		
	F	504	SEE ECO 504		

SIZE	DRAWING NO.	REV
D	201663	F

SUPPLEMENTARY INFORMATION		NAME	DATE
PRINT NUMBER 264008-1	DRN		
NEXT ASSEMBLY	CHKD	R.K. Ree	10/1/68
	APP		
	APP		

MATERIAL
FINISH
DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

SCALE NONE
DO NOT SCALE DWG
ALL DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL ± .
FRACTION ± .
ANGLE ± °

data products corporation
CULVER CITY, CALIFORNIA

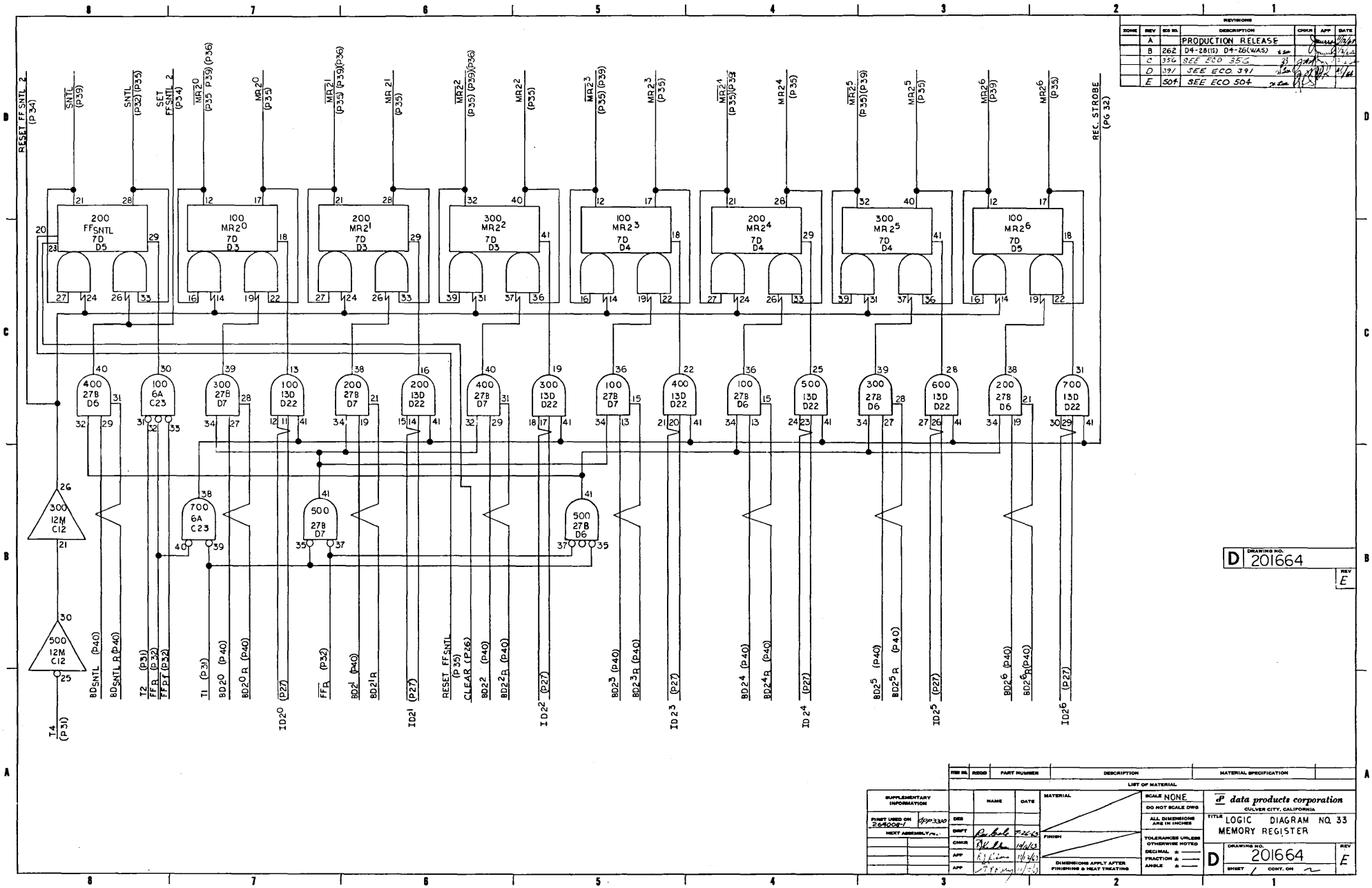
TITLE
LOGIC DIAGRAM NO. 32
CONTROL LOGIC

SIZE	DRAWING NO.	REV
D	201663	F

SHEET 1 CONT. ON ~

LIST OF MATERIAL

SIZE	ZONES	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION



ZONE	REV	ECO NO.	DESCRIPTION	CHKR	APP	DATE
	A		PRODUCTION RELEASE			11/7/62
	B	262	D4-28(15) D4-26(WAS)			11/14/62
	C	356	SEE ECO 356			11/14/62
	D	391	SEE ECO 391			11/28/62
	E	504	SEE ECO 504			11/28/62

REVISIONS

D DRAWING NO. 201664 REV E

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

LIST OF MATERIAL

SUPPLEMENTARY INFORMATION		NAME	DATE
FIRST USED ON 264008-1	DES		
NEXT ASSEMBLY	DRFT		
	CHKR		
	APP		
	APP		

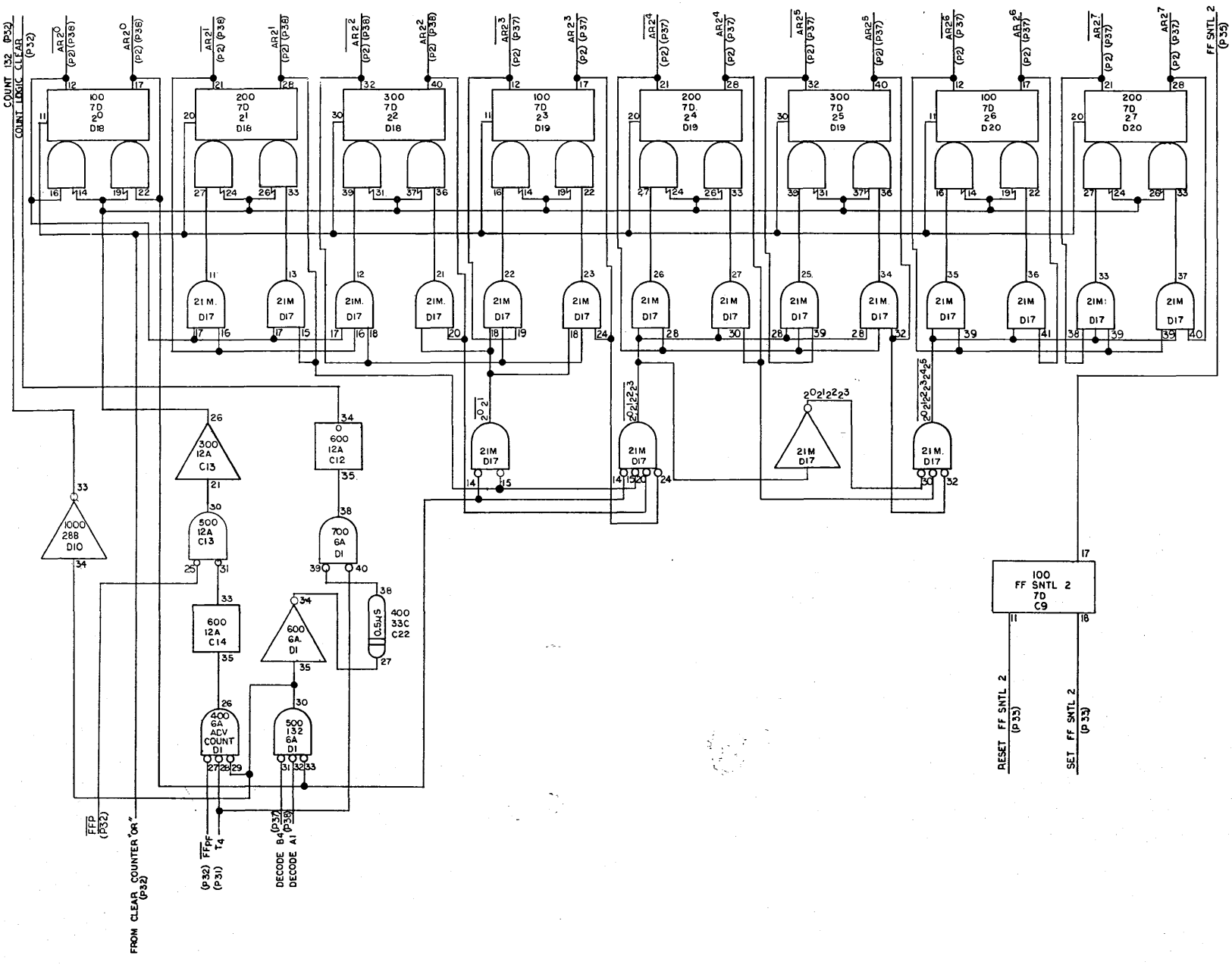
MATERIAL
FINISH
DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

SCALE NONE
DO NOT SCALE DWG
ALL DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL ±
FRACTION ±
ANGLE ±

data products corporation
CULVER CITY, CALIFORNIA

TITLE LOGIC DIAGRAM NO 33
MEMORY REGISTER

D DRAWING NO. 201664 REV E
SHEET 1 CONT. ON

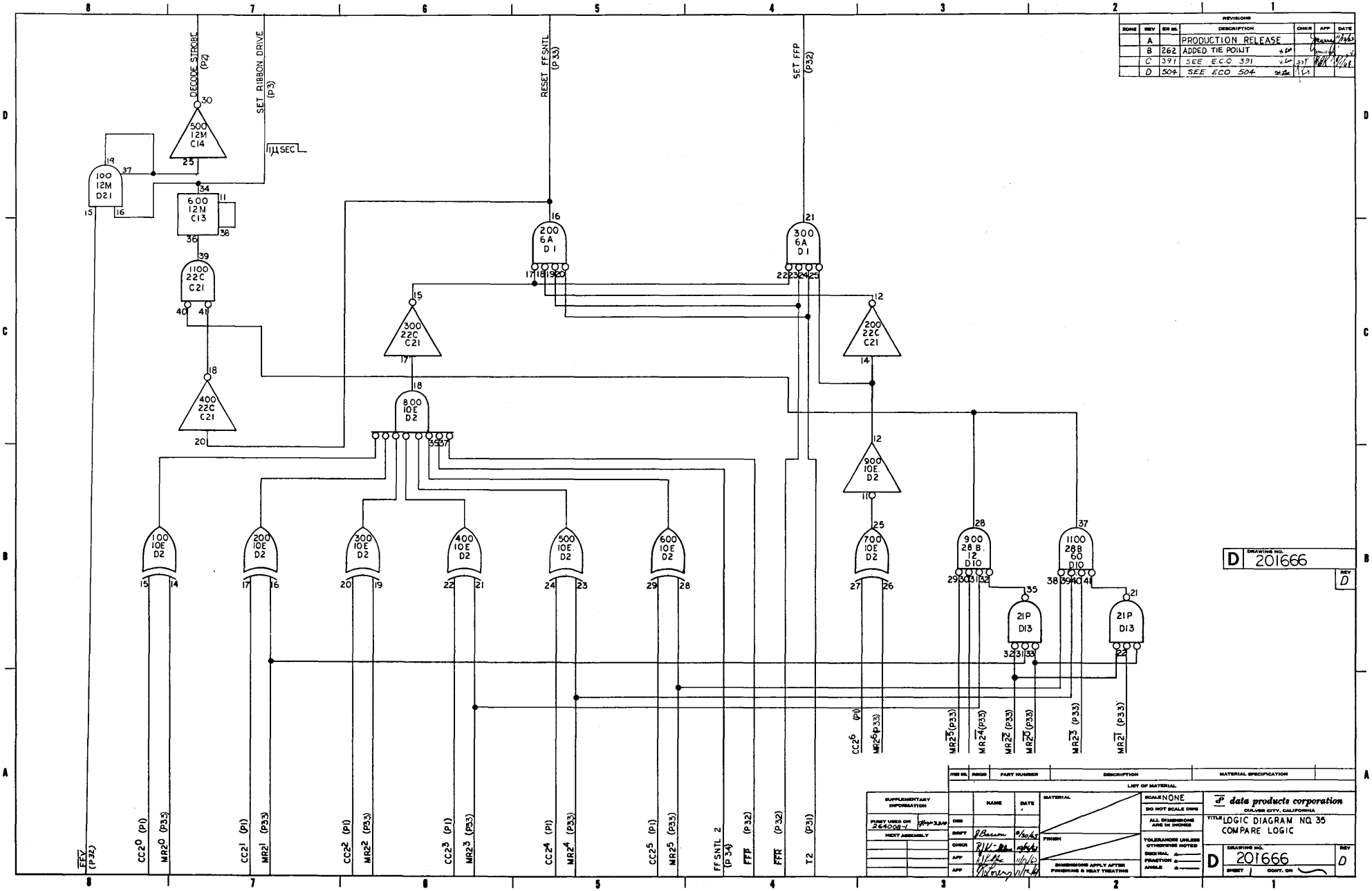


data products corporation
CULVER CITY, CALIFORNIA

TITLE
LOGIC DIAGRAM NO. 34
ADDRESS REGISTER

D | DRAWING NO. 201665 | REV C

SHEET 1 CONT. ON



ZONE	REV	ECO NO.	DESCRIPTION	CHK'R	APP	DATE
	A		PRODUCTION RELEASE			
	B	262	ADDED TIE POINT			
	C	391	SEE E.C.O. 391			
	D	504	SEE ECO 504			

REVISIONS

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

LIST OF MATERIAL

	NAME	DATE
DES		
DRFT	J Barron	4/30/62
CHK'R		
APP		
APP		

SUPPLEMENTARY INFORMATION
FIRST USED ON 264008-1
NEXT ASSEMBLY

MATERIAL
FINISH
DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

SCALE NONE
DO NOT SCALE DWG
ALL DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL ±.
FRACTION ±.
ANGLE ±.

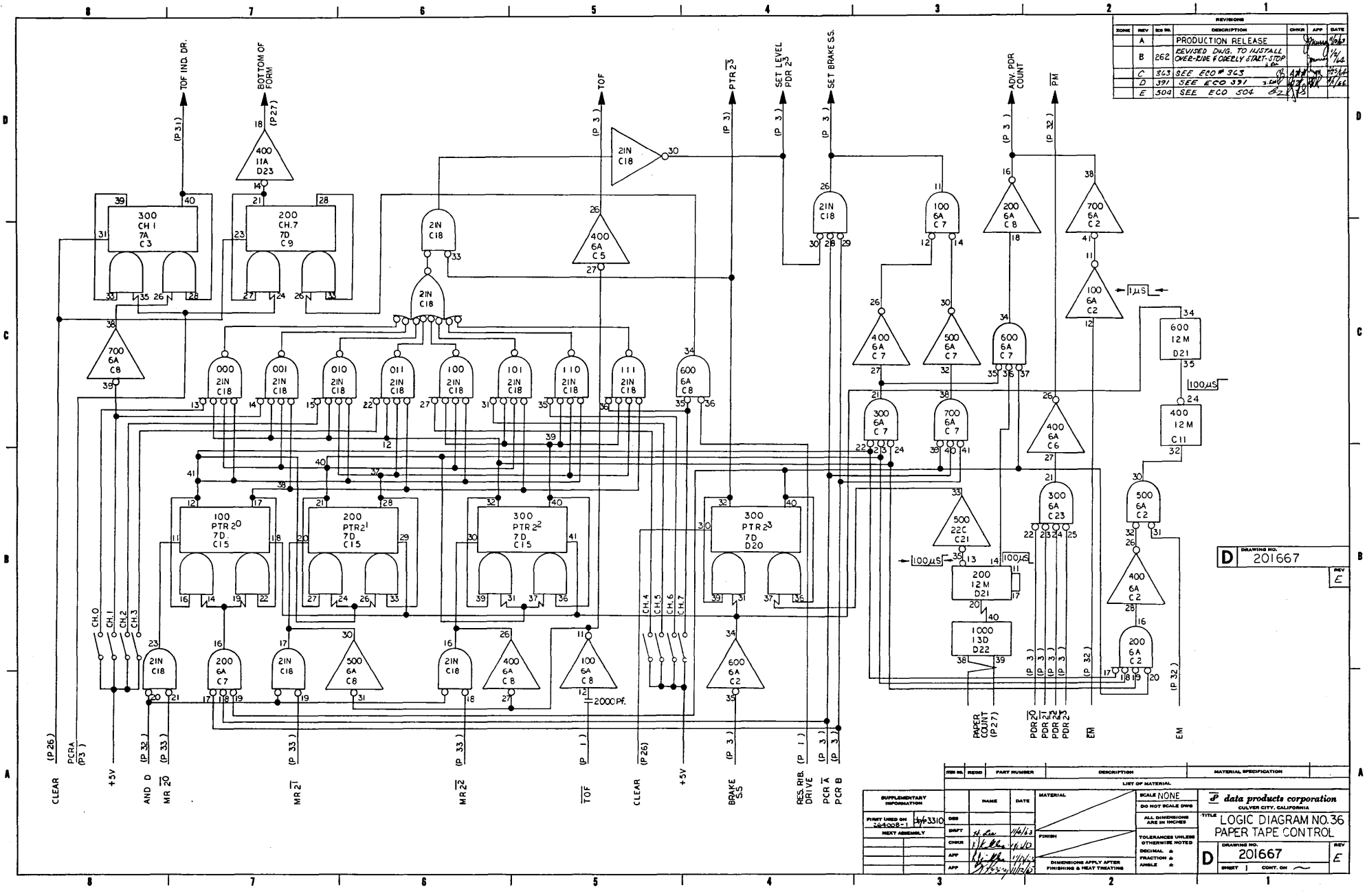
data products corporation
CULVER CITY, CALIFORNIA

TITLE LOGIC DIAGRAM NO. 35
COMPARE LOGIC

D 201666 REV D

SHEET 1 CONT. ON

D 201666 REV D



ZONE	REV	ECO NO.	DESCRIPTION	CHKR	APP	DATE
	A		PRODUCTION RELEASE			
	B	262	REVISED DWG. TO INSTALL OVER-RIDE & DDELY START-STOP			
	C	343	SEE ECO # 343			
	D	391	SEE ECO 391			
	E	304	SEE ECO 304			

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

LIST OF MATERIAL

SUPPLEMENTARY INFORMATION
FIRST USED ON 264008-1 4/6/3310
NEXT ASSEMBLY

	NAME	DATE
DES		
DRFT	H. Lee	11/4/63
CHKR		
APP		
APP		

MATERIAL
FINISH
DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

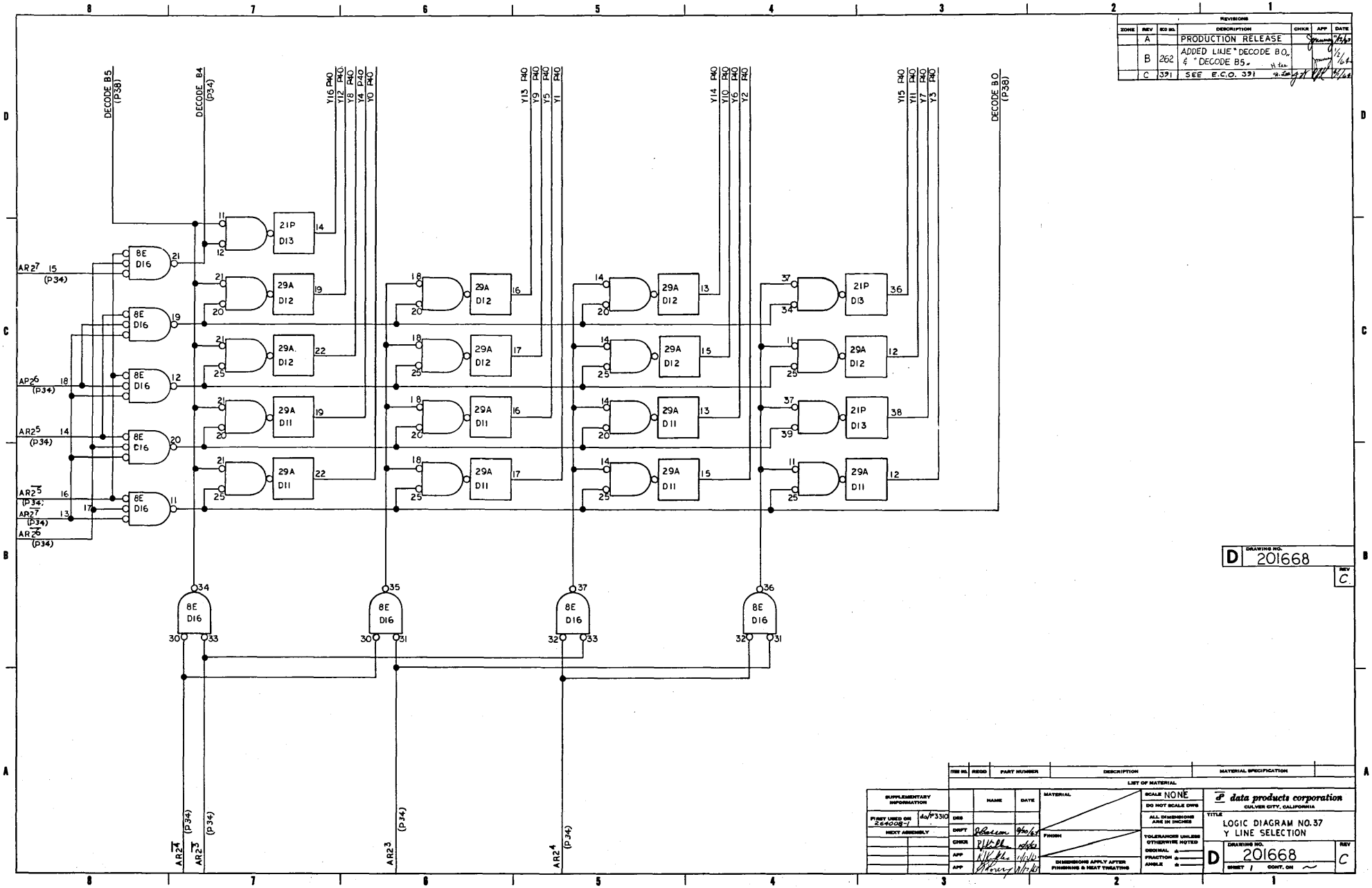
SCALE NONE
DO NOT SCALE DWG
ALL DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL ±
FRACTION ±
ANGLE ±

data products corporation
CULVER CITY, CALIFORNIA

TITLE LOGIC DIAGRAM NO. 36
PAPER TAPE CONTROL

D DRAWING NO. 201667 REV E
SHEET 1 CONT. ON

D DRAWING NO. 201667 REV E



ZONE	REV	ECO NO.	REVISIONS DESCRIPTION	CHKR	APP	DATE
	A		PRODUCTION RELEASE			12/62
	B	262	ADDED LINE "DECODE B0" & "DECODE B5"			1/64
	C	391	SEE E.C.O. 391			5/66

D DRAWING NO. 201668 REV C

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

LIST OF MATERIAL

SUPPLEMENTARY INFORMATION
FIRST USED ON 264008-1 do/P330
NEXT ASSEMBLY

	NAME	DATE
DES		
DRFT	Peterson	9/6/67
CHKR	R.Wells	10/6/67
APP	R.Wells	10/9/67
APP	Mowry	10/9/67

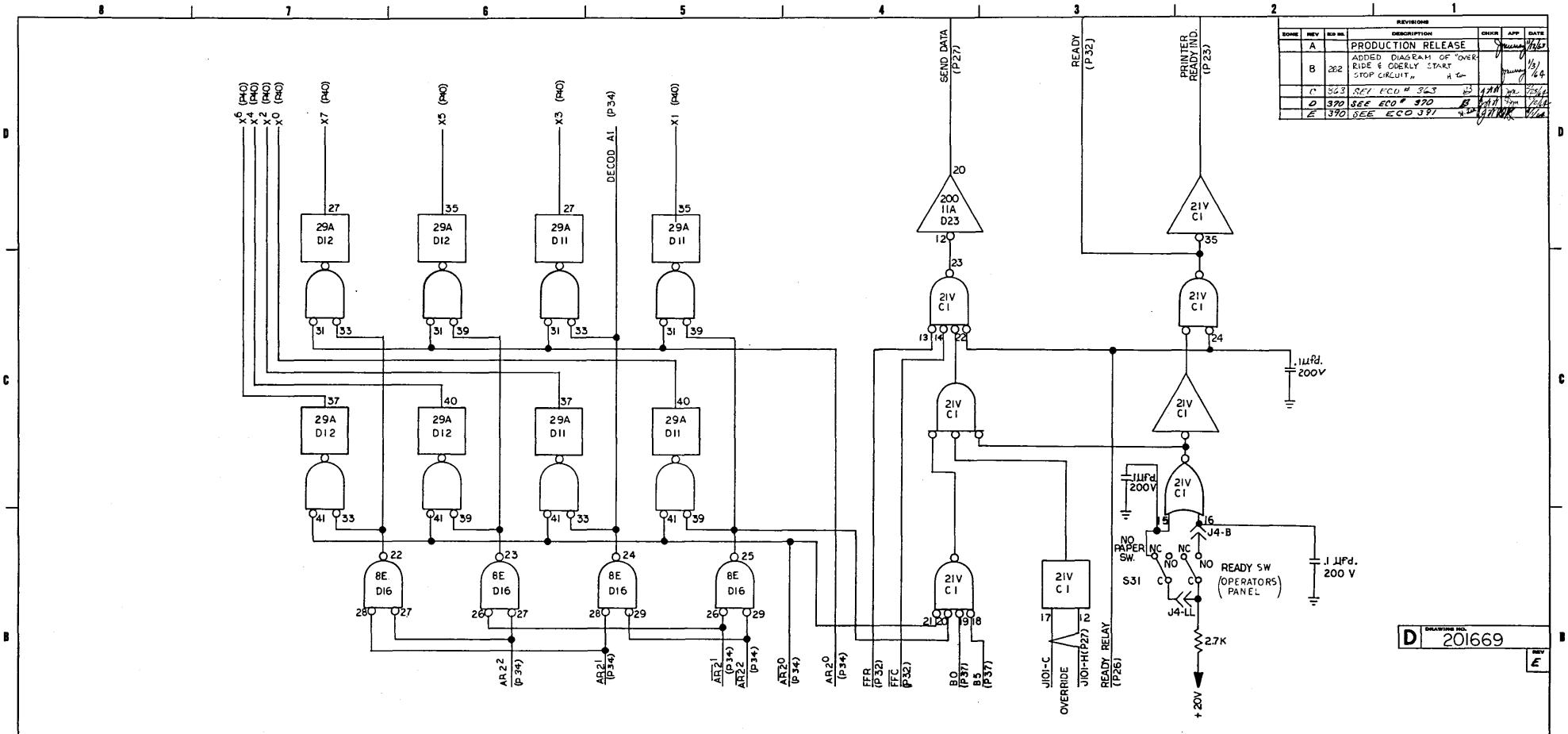
MATERIAL
FINISH
DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

SCALE NONE
DO NOT SCALE DWG
ALL DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL ±
FRACTION ±
ANGLE ±

data products corporation
CULVER CITY, CALIFORNIA

TITLE
LOGIC DIAGRAM NO. 37
Y LINE SELECTION

D DRAWING NO. 201668 REV C
SHEET 1 CONT. ON



ZONE	REV	ECO NO.	DESCRIPTION	CHKR	APP	DATE
	A		PRODUCTION RELEASE			
	B	262	ADDED DIAGRAM OF "OVERRIDE & OBERLY START STOP CIRCUIT"			
	C	363	SEE ECO # 363			
	D	370	SEE ECO # 370			
	E	390	SEE ECO 391			

D 201669 E

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

LIST OF MATERIAL

SUPPLEMENTARY INFORMATION

FIRST USED ON 4e/P3310 C64008-1

NEXT ASSEMBLY

	NAME	DATE
DES		
DRFT		9-30-63
CHKR		10/4/63
APP		10/7/63
APP		11/13/63

MATERIAL

FINISH

DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

SCALE NONE

DO NOT SCALE DWG

ALL DIMENSIONS ARE IN INCHES

TOLERANCES UNLESS OTHERWISE NOTED

DECIMAL ±

FRACTION ±

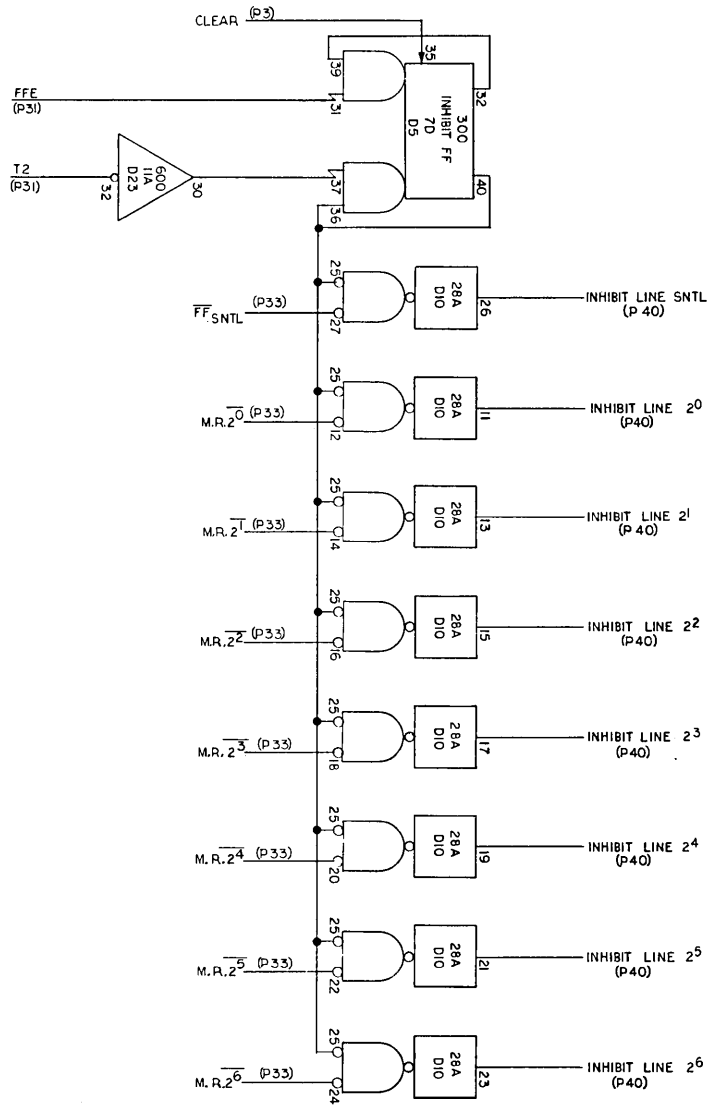
ANGLE ±

data products corporation
CULVER CITY, CALIFORNIA

TITLE
LOGIC DIAGRAM NO. 38
X LINE SELECTION

D 201669 E

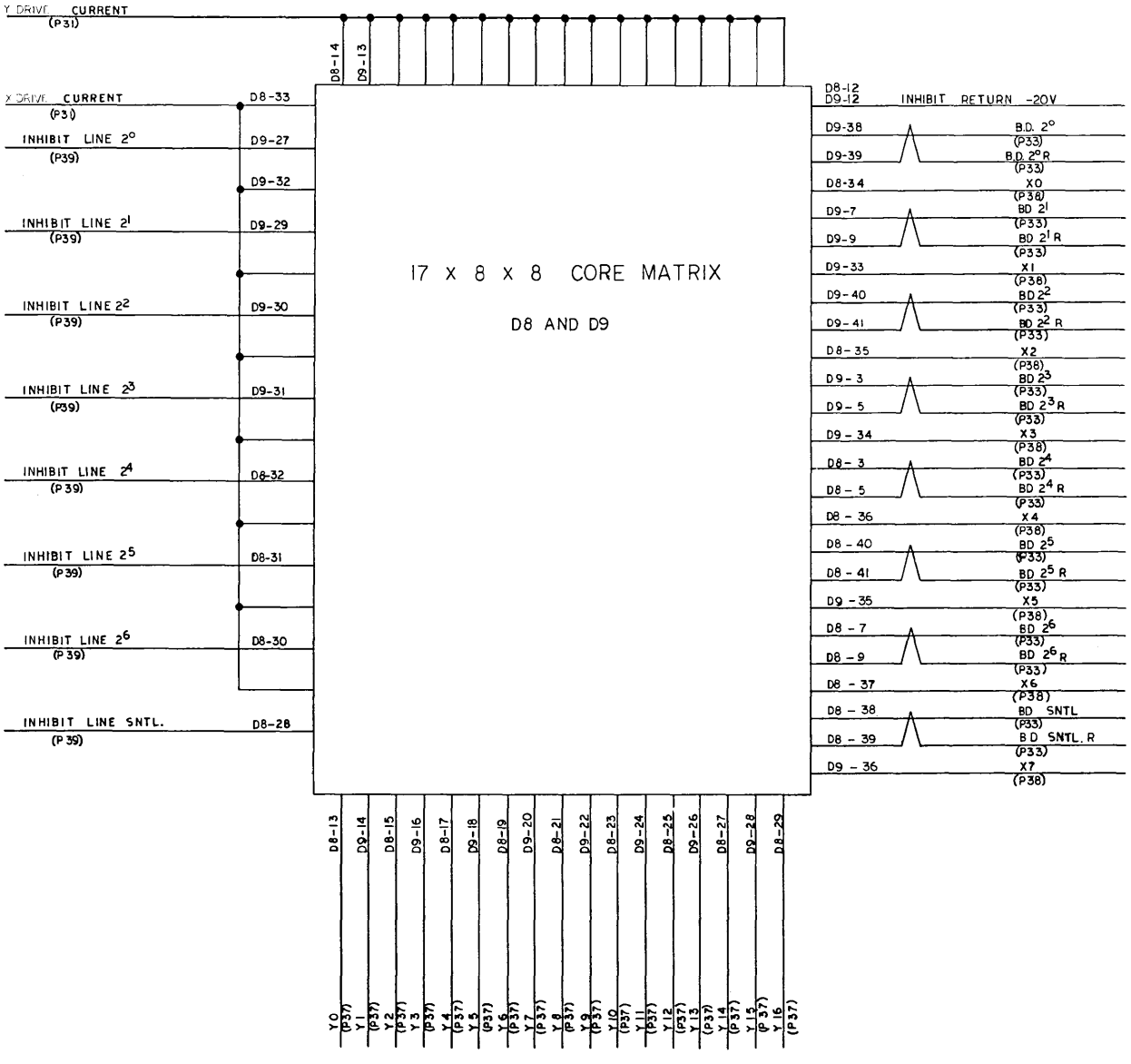
SHEET 1 CONT. ON



data products corporation
COLVER CITY, CALIFORNIA

TITLE: LOGIC DIAGRAM NO. 39
INHIBIT DRIVE

D | DRAWING NO. 201670 | REV A
SHEET 1 | CONT. ON ~

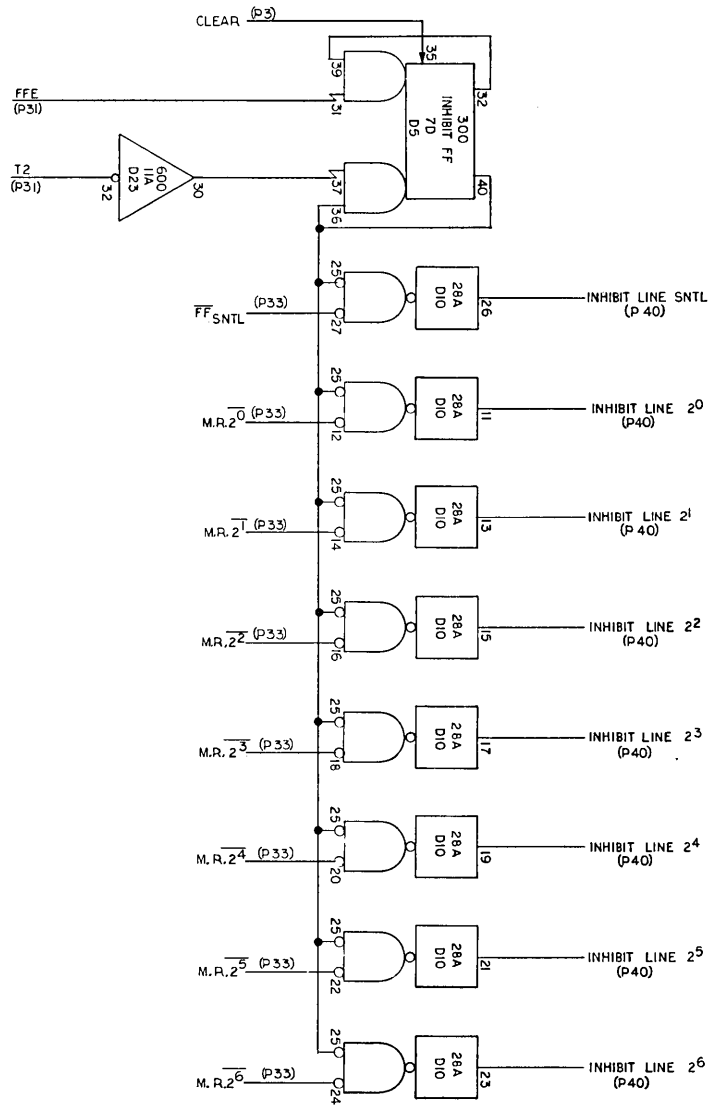


data products corporation
CULVER CITY, CALIFORNIA

TITLE LOGIC DIAGRAM NO. 40
CORE MATRIX

D | DRAWING NO. 201671 | REV A

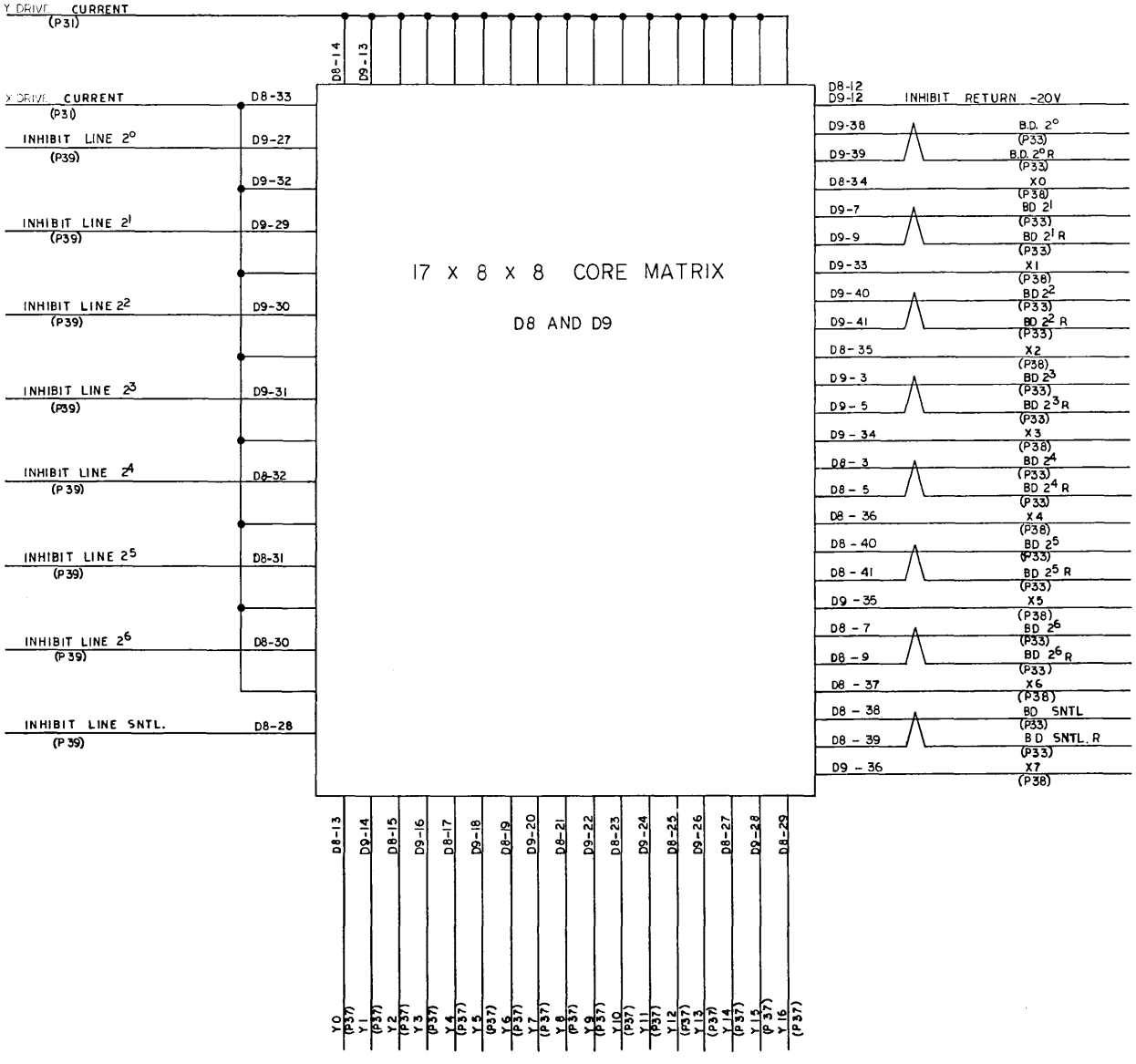
SHEET 1 CONT. ON



data products corporation
CULVER CITY, CALIFORNIA

TITLE
LOGIC DIAGRAM NO. 39
INHIBIT DRIVE

DRAWING NO. 201670
SHEET 1 CONT. ON ~
REV A
D

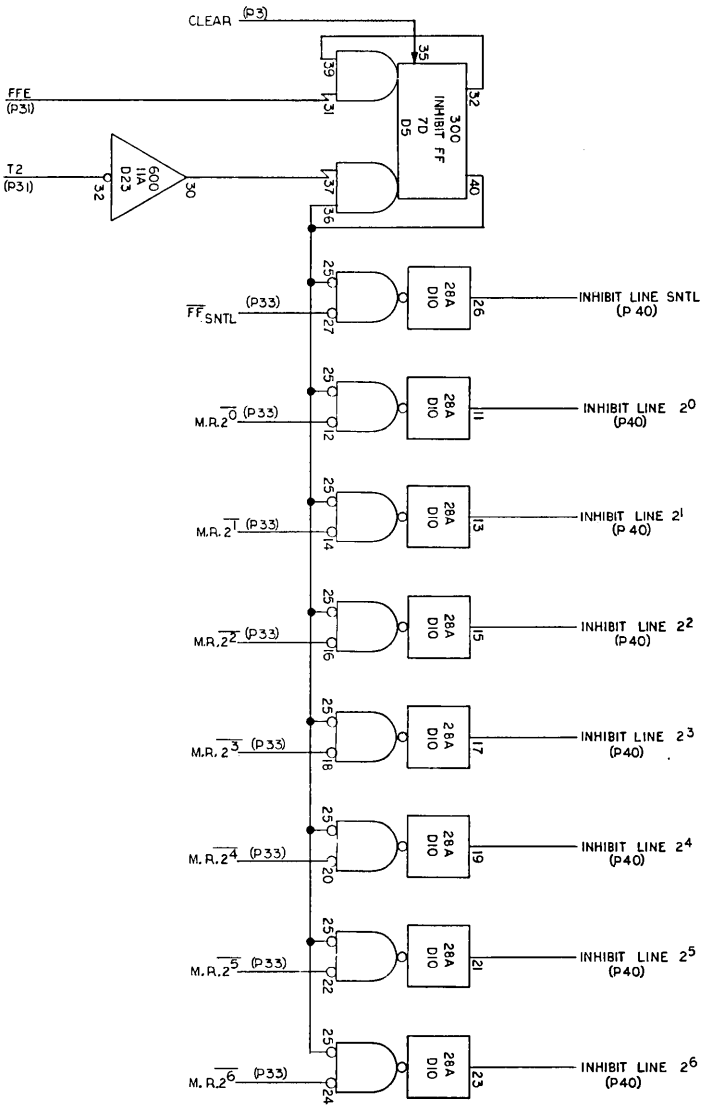


data products corporation
CULVER CITY, CALIFORNIA

TITLE: LOGIC DIAGRAM NO. 40
CORE MATRIX

D | DRAWING NO. 201671 | REV A

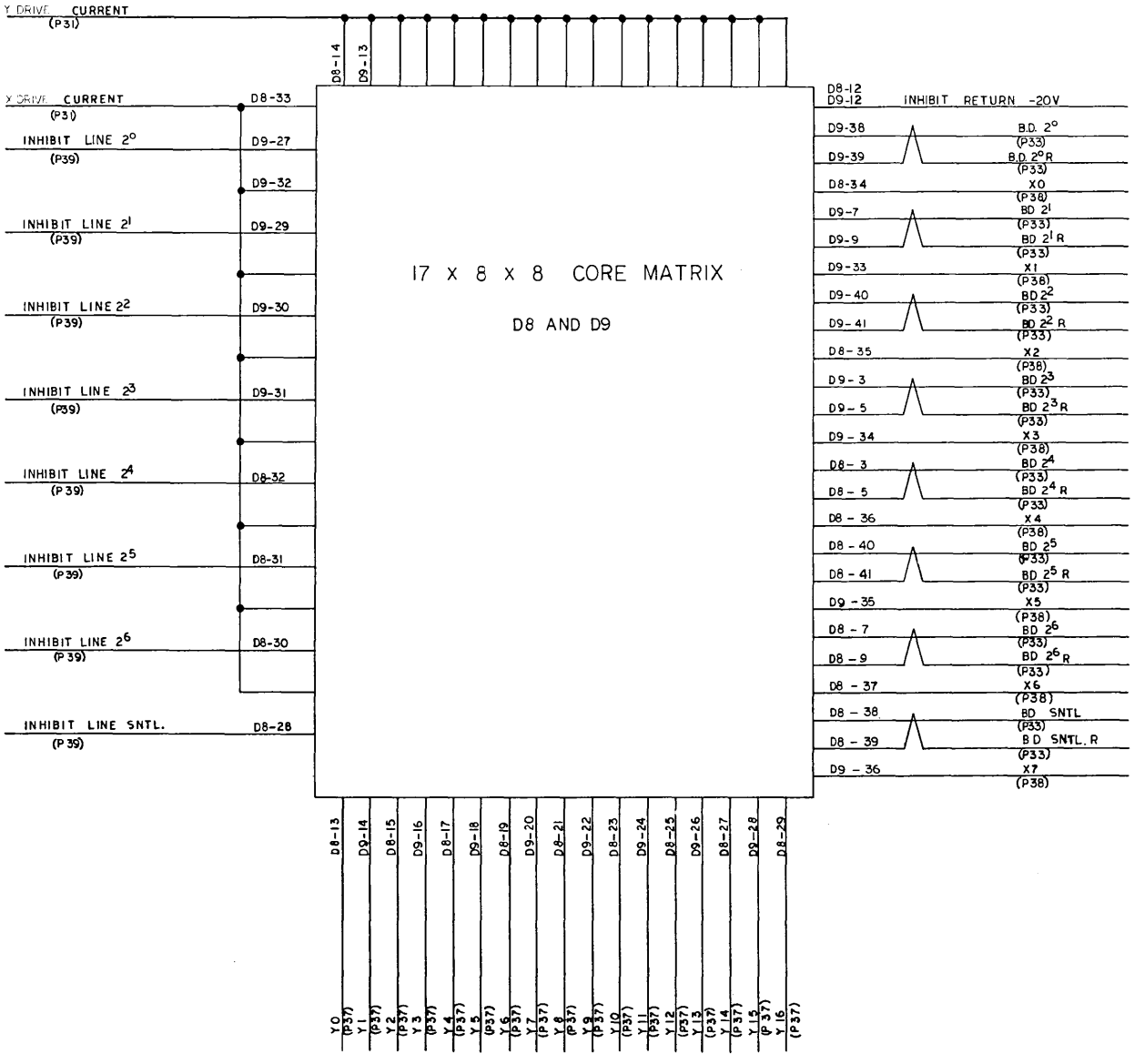
SHEET 1 | CONT. ON



data products corporation
CULVER CITY, CALIFORNIA

TITLE: LOGIC DIAGRAM NO. 39
INHIBIT DRIVE

D | DRAWING NO. 20670 | REV A
SHEET 1 | CONT. ON ~



data products corporation
CULVER CITY, CALIFORNIA

TITLE: LOGIC DIAGRAM NO. 40
CORE MATRIX

D | DRAWING NO. 201671 | REV A

SHEET 1 | CONT. ON

REVISIONS					
ZONE	REV	ECO NO.	DESCRIPTION	CHKR	APP	DATE
	A		PRODUCTION RELEASE			7/9/68
	B	324	REVISED PAGE NO. PIN NO. ON CARD 19 (B CAGE) 4C WAS 4B ON CARD 16 & 17 (C CAGE) ON SHEET 2			
	C	356	SEE ECO #356			
	D	369	SEE ECO #369			
	E	370	SEE ECO #370			
	F	391	SEE ECO 391			
	G	443	SEE ECO 443 P.C.			
	H	504	SEE ECO 504			

A

CARDS 1 THRU 22		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CKT.	OUTPUT PIN	1A	1A	1A	1A	1A	1A	1A	1A	1A	1A	1A	1A	1A	1A	1A	1A	1A	1A	1A	1A	1A	1A	5A
100	19	HMR. 1-P4	7-P4	13-P5	19-P6	25-P7	31-P7	37-P8	43-P9	49-P10	55-P10	61-P11	67-P12	73-P13	79-P13	85-P14	91-P15	97-P16	103-P16	109-P17	115-P18	121-P19	127-P19	P1-16
200	17	2-P4	8-P4	14-P5	20-P6	26-P7	32-P7	38-P8	44-P9	50-P10	56-P10	62-P11	68-P12	74-P13	80-P13	86-P14	92-P15	98-P16	104-P16	110-P17	116-P18	122-P19	128-P19	P1-17
300	18	3-P4	9-P5	15-P5	21-P6	27-P7	33-P8	39-P8	45-P9	51-P10	57-P11	63-P11	69-P12	75-P13	81-P14	87-P14	93-P15	99-P16	105-P17	111-P17	117-P18	123-P19	129-P20	P1-36
400	27	4-P4	10-P5	16-P5	22-P6	28-P7	34-P8	40-P8	46-P9	52-P10	58-P11	64-P11	70-P12	76-P13	82-P14	88-P14	94-P15	100-P16	106-P17	112-P17	118-P18	124-P19	130-P20	P2-37
500	29	5-P4	11-P5	17-P6	23-P6	29-P7	35-P8	41-P9	47-P9	53-P10	59-P11	65-P12	71-P12	77-P13	83-P14	89-P15	95-P15	101-P16	107-P17	113-P18	119-P18	125-P19	131-P20	P2-41
600	28	6-P4	12-P5	18-P6	24-P6	30-P7	36-P8	42-P9	48-P9	54-P10	60-P11	66-P12	72-P12	78-P13	84-P14	90-P15	96-P15	102-P16	108-P17	114-P18	120-P18	126-P19	132-P20	

B

CARDS 1 THRU 10, 12 THRU 18		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CKT.	OUTPUT PIN	2A	2A	2A	2A	2A	2A	2A	2A	2A	2A	8A	2A	2A	2A	2A	2A	2A	2A	3D	99D	99AE	99B	99A
100	14	HMR. 1-P4	9-P5	17-P6	25-P7	33-P8	41-P9	49-P10	57-P11	65-P12	73-P13	P2-24 23 22 21 11 12 13 14 29 28 27 26 25 38 33 P2-40	81-P14	89-P15	97-P16	105-P17	113-P18	121-P19	129-P20	P1-14	-10V PIN 15	-15V PIN 13	+5V PIN 3	-5V PIN 7
200	13	2-P4	10-P5	18-P6	26-P7	34-P8	42-P9	50-P10	58-P11	66-P12	74-P13		82-P14	90-P15	98-P16	106-P17	114-P18	122-P19	130-P20	P3-36				
300	12	3-P4	11-P5	19-P6	27-P7	35-P8	43-P9	51-P10	59-P11	67-P12	75-P13		83-P14	91-P15	99-P16	107-P17	115-P18	123-P19	131-P20	P3-25				
400	11	4-P4	12-P5	20-P6	28-P7	36-P8	44-P9	52-P10	60-P11	68-P12	76-P13		84-P14	92-P15	100-P16	108-P17	116-P18	124-P19	132-P20	P3-13				
500	38	5-P4	13-P5	21-P6	29-P7	37-P8	45-P9	53-P10	61-P11	69-P12	77-P13		85-P14	93-P15	101-P16	109-P17	117-P18	125-P19		P3-17				
600	39	6-P4	14-P5	22-P6	30-P7	38-P8	46-P9	54-P10	62-P11	70-P12	78-P13		86-P14	94-P15	102-P16	110-P17	118-P18	126-P19		P3-30				
700	40	7-P4	15-P5	23-P6	31-P7	39-P8	47-P9	55-P10	63-P11	71-P12	79-P13		87-P14	95-P15	103-P16	111-P17	119-P18	127-P19		P3-36				
800	41	8-P4	16-P5	24-P6	32-P7	40-P8	48-P9	56-P10	64-P11	72-P12	80-P13		88-P14	96-P15	104-P16	112-P17	120-P18	128-P19		P3-37				
																				P3-26				

D 201822 REV H

5. NUMBERS FOLLOWING PAGE NUMBERS ARE OUTPUT PINS FOR THAT CKT.
4. A NUMBER PRECEDED BY P INDICATES PAGE AND NUMBER.
3. BLOCKS MARKED THRU INDICATE NO CKT. ON CARD.
2. CARD 11 ON B CAGE HAS ONLY ONE CKT. BUT 16 OUTPUT PINS.
1. P1, P2, ETC. INDICATE PAGE NO., CKT. IS LOCATED ON.

NOTE: UNLESS OTHERWISE SPECIFIED

ITEM NO.	QUANTITY	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

LIST OF MATERIAL

SUPPLEMENTARY INFORMATION: FIRST USED ON 66908-1, 4/6/3310; NEXT ASSEMBLY

	NAME	DATE
DES		
DRFT	H. Lee	11/21/63
CHKR	J. Evans	11/21/63
APP	W. Klein	11/21/63
APP	R. Levy	12/16/63

MATERIAL / FINISH / DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

SCALE NONE
DO NOT SCALE DWG
ALL DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE NOTED: DECIMAL ±, FRACTION ±, ANGLE ±

data products corporation, CULVER CITY, CALIFORNIA

TITLE: LOGIC DIAGRAM NO.41 CARD LOCATION

D DRAWING NO. 201822 REV H

SHEET 1 CONT. ON 2

REVISIONS					
ZONE	REV	ECO NO.	DESCRIPTION	CHKR	APP	DATE
			SEE SHEET 1			

C

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
21V	6A	7A	7A	6A	6A	6A	6A	7D	7A	12M	12M	12M	12M	7D	4C	4C	21N	7D	7D	22C	33C	6A
P38-	P36-11	P1-41	P3-41/36	P3-11	P32-11	P36-11	P36-11	SNTL2 P34-17	P3-41/36	P3-19	P3-19	P3-19	P31-19	P36-12/17	P1-11	P1-11	P36-30	P32-17	P32-12		P31-41	P31-11
	P36-16	P3-32/38	P3-37/38	P3-16	P3-16	P36-16	P36-16	P36-21/28	P3-37/38	P1-13	P1-13/14	P1-14	P3-14	P36-21/28	P1-20	P1-20	P36-26	P32-21/28	P32-21/28	P35-12	P32 40	P32-16
	P3-21	P36-39/40	P3-39/40	P3-21	P3-21	P36-21	P34-21	P32-32/40	P3-39/40	P1-26	P33-26	P34-26		P36-32/40	P1-32	P1-32	P36-16	P32-32	FFEM P32-32/40	P32-21	P32-39	P36-31
	P36-26			P36-26	P36-26	P36-26	P36-26			P36-24	P1-24	P1-24	P3-29/24		P1-40	P1-40	P36-17			P35-15	P34-38	P32-26
	P36-30			P1-30	P3-30	P36-30	P36-30			P32-25	P33-30	P34-30	P35-30		P3-21	P3-21	P36-23			P35-18	P32-37	P33-30
	P36-34			P3-34	P3-34	P36-34	P36-34			P32-34	P34-34	P35-34	P34-33							P36-33		P31-34
	P36-38			P3-38	P3-38	P36-38	P36-38													P32-24	"	P33-38
																				P32-27	P32-34	
																				P32-30	P31-12	
																				P32-36	P31-14	
																				P35-39	P31-18	
																					P31-30	
																					P3-11	

D

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
6A	10E	7D	7D	7D	27B	27B	CORE	ARRAY	28B	29A	29A	21P	31B	7D	8E	21M	7D	7D	7D	12M	13D	11A
P32-11	P35	MR2[0] P33-12/17	MR2[3] P33-12/17	MR2[6] P33-12/17	P33-36	P33-36			P39-23	P37-16	P37-16	P37-36	IRX P31-14	FFD P31-12/17	P37-21	P34-11	P34-12/17	P34-12/17	P34-12/17	P35-19	P33-13	P32-21
P35-16	P35	MR2[1] P33-21/28	MR2[4] P33-21/26	SNTL P33-21/28	P33-38	P33-38			P39-21	P37-17	P37-17	P37-38	IRY P31-15	FFE P31-21/28	P37-19	P34-13	P34-21/28	P34-21/28	P34-21/28	P36 13/14	P33-16	P32-20
P35-21	P35	MR2[2] P33-35/40	MR2[5] P33-32/40	INHIBIT P39-32/40	P33-39	P33-39			P39-19	P37-13	P37-13	P32-30	IWX P31-14	P3-32/40	P37-12	P34-12	P34-32/40	P34-32/40	P36 32/40		P33-19	P32-19
P34-26	P35				P33-40	P33-40			P39-17	P37-15	P37-15	P31-40	IWY P31-15		P32-38	P34-21				P3-29	P33-22	P36-18
P3-30	P35				P33-41	P33-41			P39-15	P37-22	P37-22	P35-21	CLOCK P31-41		P32-41	P34-22				P3-30	P33-25	
P34-34	P35						P40 MATRIX	P40 MATRIX	P39-13	P37-19	P37-19	P31-19	P31-(13)		P32-20	P34-23				P36-34	P33-28	P39-30
P34-38	P35-25								P39-11	P37-12	P37-12	P31-17	P31-31		P32-11	P34-26					P33-31	
	P35-18								P39-26	P38-27	P38-27	P32-16	P31-27		P35-34	P34-27					P32-34	
	P35-12								P35-28	P38-35	P38-35	P37-14	P31-32		P37-35	P34-25					P32-37	
									P34-33	P38-40	P38-40	P32-23	P31-34		P37-37	P34-34					P36-40	
									P35-37	P38-37	P38-37	P35-35	P31-38		P37-36	P34-35						
													P31-25		P38-16	P34-36						
													P31-26		P38-23	P34-33						
													P31-39		P38-24	P34-37						
															P38-25							

D DRAWING NO. 201822 REV H

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

LIST OF MATERIAL

SUPPLEMENTARY INFORMATION		NAME	DATE
FIRST USED ON 2640028-1	DES		
NEXT ASSEMBLY	DRFT		
	CHKR		
	APP		
	APP		

MATERIAL / FINISH — DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

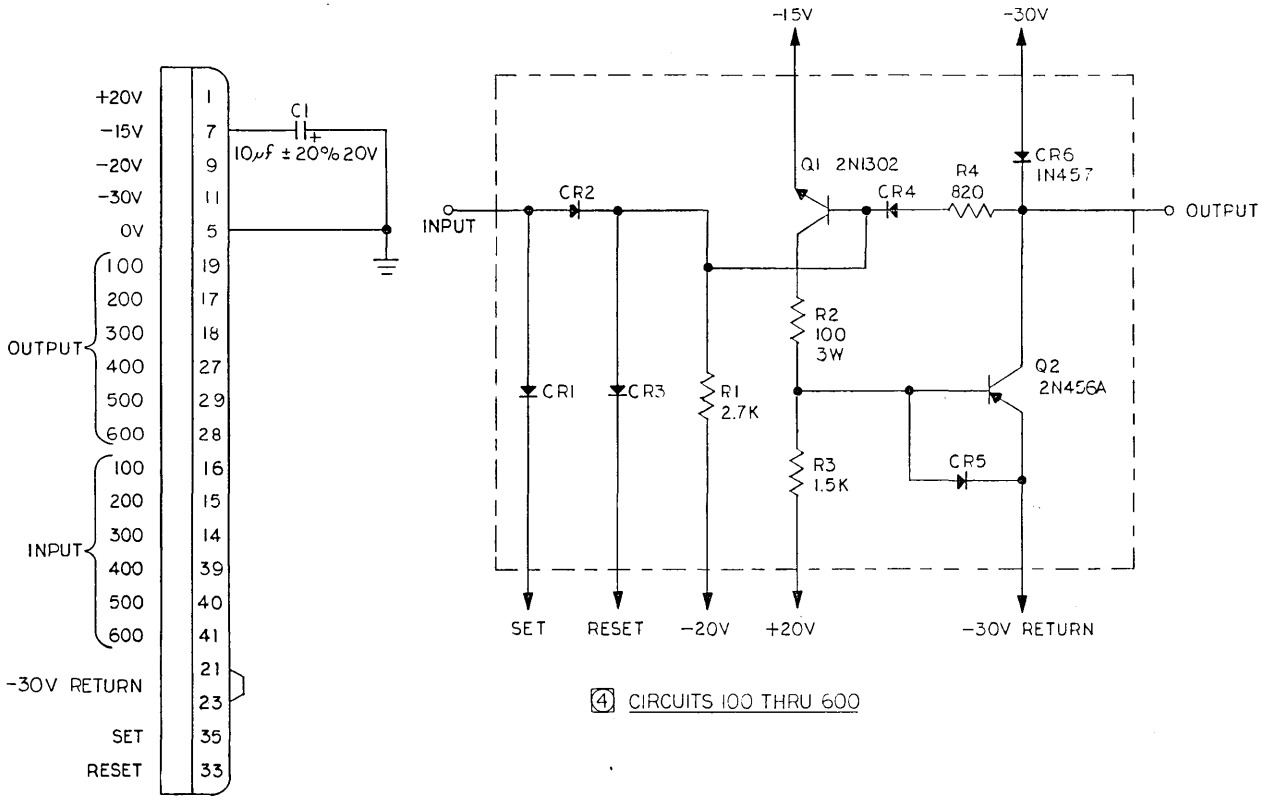
SCALE NONE — DO NOT SCALE DWG — ALL DIMENSIONS ARE IN INCHES — TOLERANCES UNLESS OTHERWISE NOTED — DECIMAL ± — FRACTION ± — ANGLE ±

data products corporation
CULVER CITY, CALIFORNIA

TITLE LOGIC DIAGRAM NO. 41 CARD LOCATION

D DRAWING NO. 201822 REV H

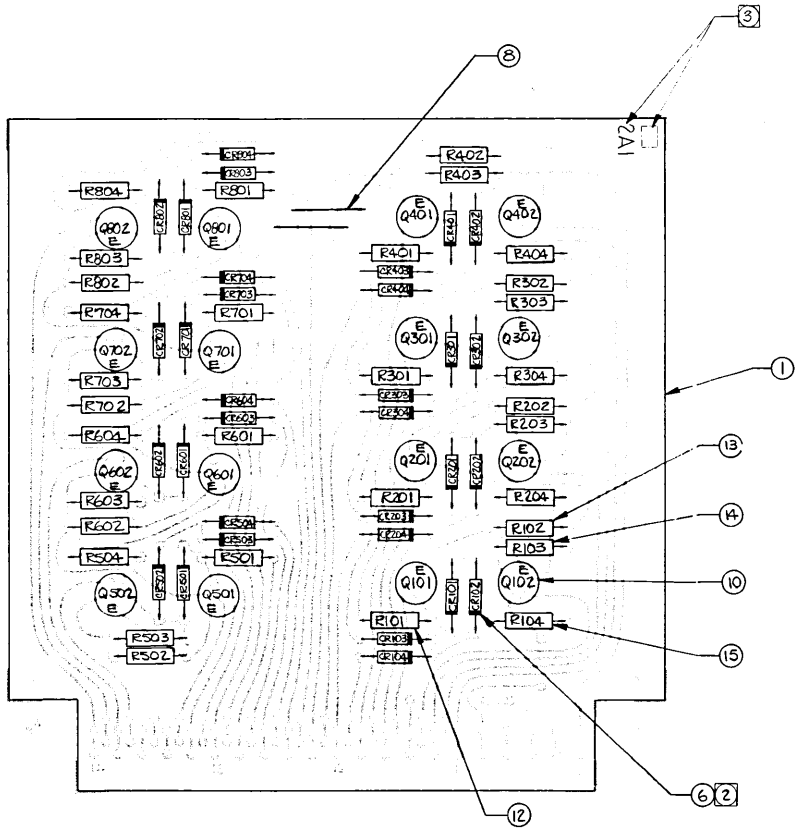
SHEET 2 CONT. ON ~



[4] CIRCUITS 100 THRU 600

[4] REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE PART DESIGNATION WITH THE SUBASSEMBLY DESIGNATION
3 ASSEMBLY DRAWING NO. 200185
2 ALL DIODES CGD 1307
1 ALL RESISTOR VALUES IN OHMS ± 5% $\frac{1}{2}$ W
NOTE: UNLESS OTHERWISE SPECIFIED

data products corporation CULVER CITY, CALIFORNIA		
TITLE: SCHEMATIC HAMMER DRIVER 1A2		
	DRAWING NUMBER C 200182	REV. D



ITEM	PART NO.	REQD	DESCRIPTION
18			
17			
16			
15	EB1235	8	RESISTOR 12K ±5%, ½W(AB) R104-R804
14	EB3335	8	" 33K " R103-R803
13	EB3925	8	" 3.9K " R102-R802
12	EB6825	8	RESISTOR 6.8K ±5%, ½W(AB) R101-R801
11			
10	2N1303	16	TRANSISTOR (T.I.) Q, ALL
9			
8		A/R	JUMPER, WIRE (#22)
7			
6	CGD1307	32	DIODE (CLEVITE) CR, ALL
5			
4			
3			
2			
1	200192-1	1	PROCESSED BOARD- HAMMER DRIVER RECEIVER 2A1

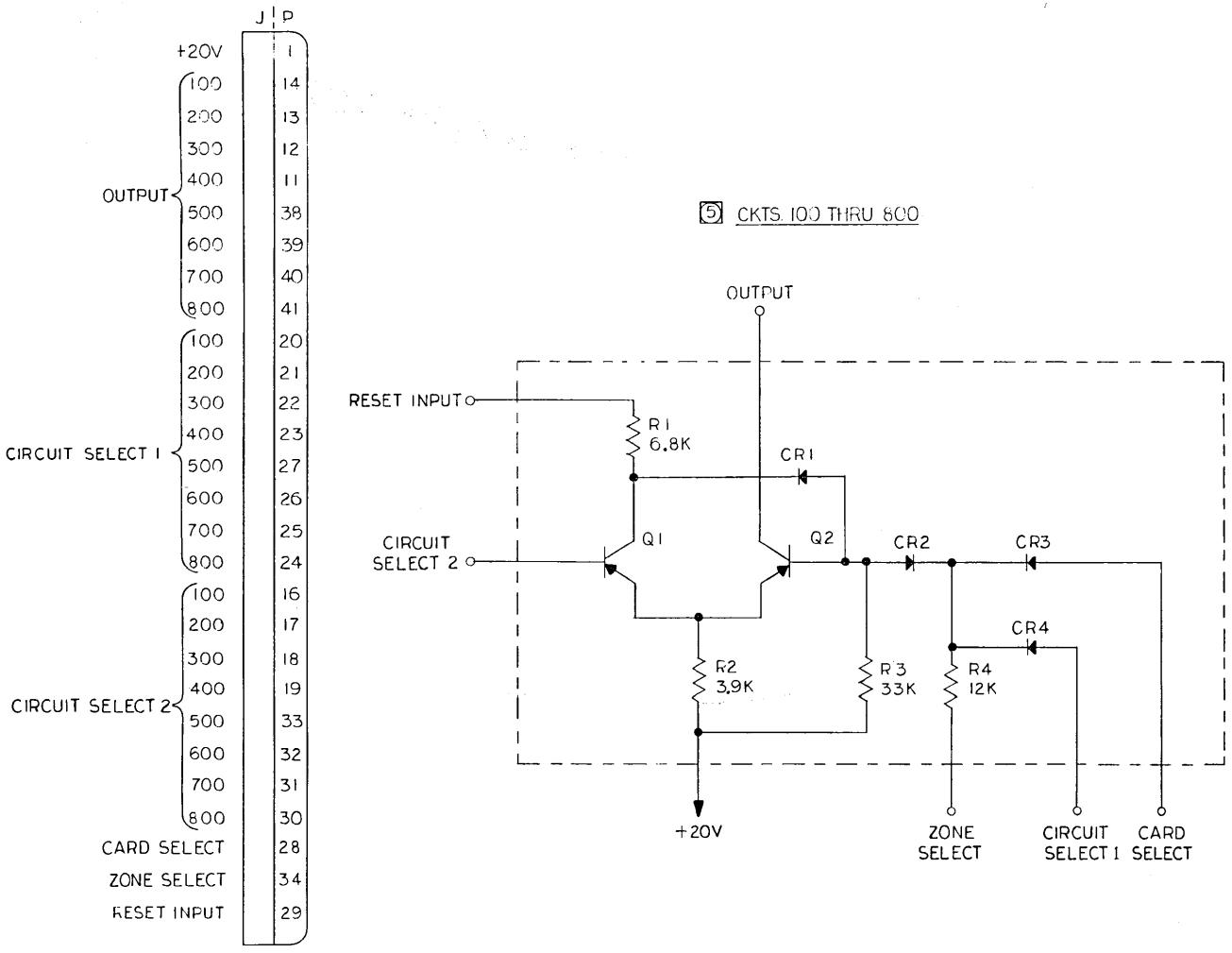
[5] STAMP BOARD TYPE, 2A1, AND CURRENT ASSY REV. LETTER IN UPPER RIGHT CORNER OF BOARD AS SHOWN, 1/8 HIGH.
[4] STRIPE ON DIODE, INDICATES DIRECTION OF CATHODE.
1. SCHEMATIC DRAWING NO. 200190.

NOTES: UNLESS OTHERWISE SPECIFIED

d data products corporation
CULVER CITY, CALIFORNIA

TITLE: CIRCUIT BOARD ASSY-
HAMMER DR. RECEIVER 2A1

		DRAWING NUMBER	REV:
	D	200193	C

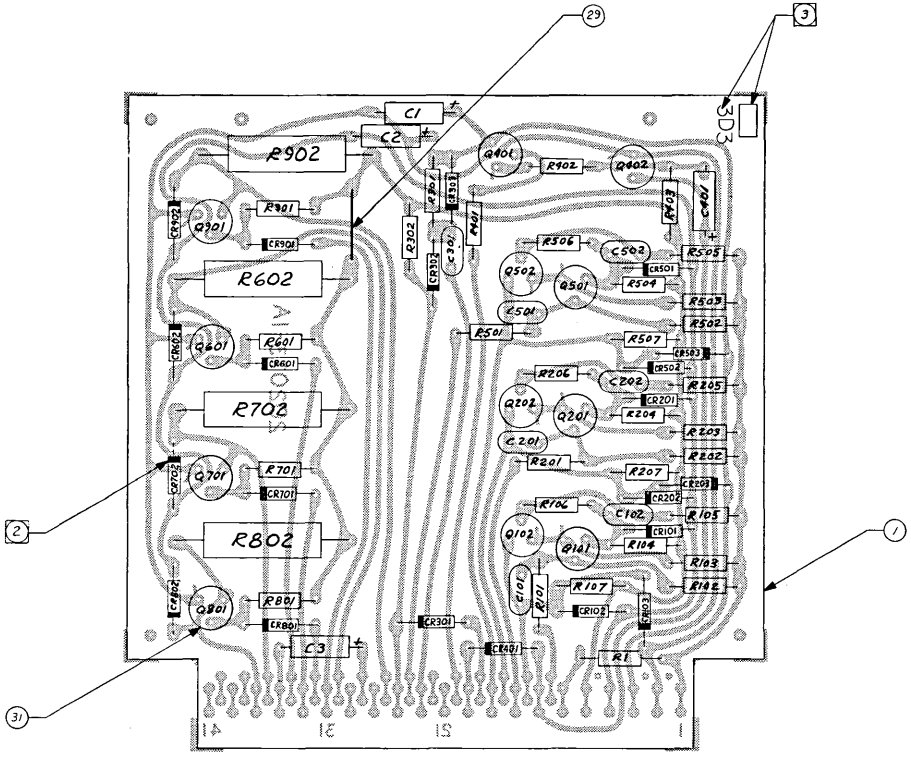


[5] REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE PART DESIGNATION WITH THE SUBASSEMBLY DESIGNATION

4. ASSEMBLY DRAWING NO. 200193
3. ALL DIODES CGD 1307
2. ALL TRANSISTORS 2N1303
1. ALL RESISTOR VALUES IN OHMS ± 5% $\frac{1}{2}$ W

NOTE: UNLESS OTHERWISE SPECIFIED

data products corporation CULVER CITY, CALIFORNIA			
TITLE: SCHEMATIC HAMMER DRIVER RECEIVER 2A1			
	C	DRAWING NUMBER 200190	REV. B



3 MARK BOARD TYPE NO. AND CURRENT ASSY. REVISION LETTER IN UPPER RIGHT CORNER OF BOARD AS SHOWN 1/8 HIGH, COLOR, BLACK.

2 STRIPE ON DIODE INDICATES CATHODE —▶|—

1. FOR CIRCUIT SEE SCHEMATIC DWG NO.202071

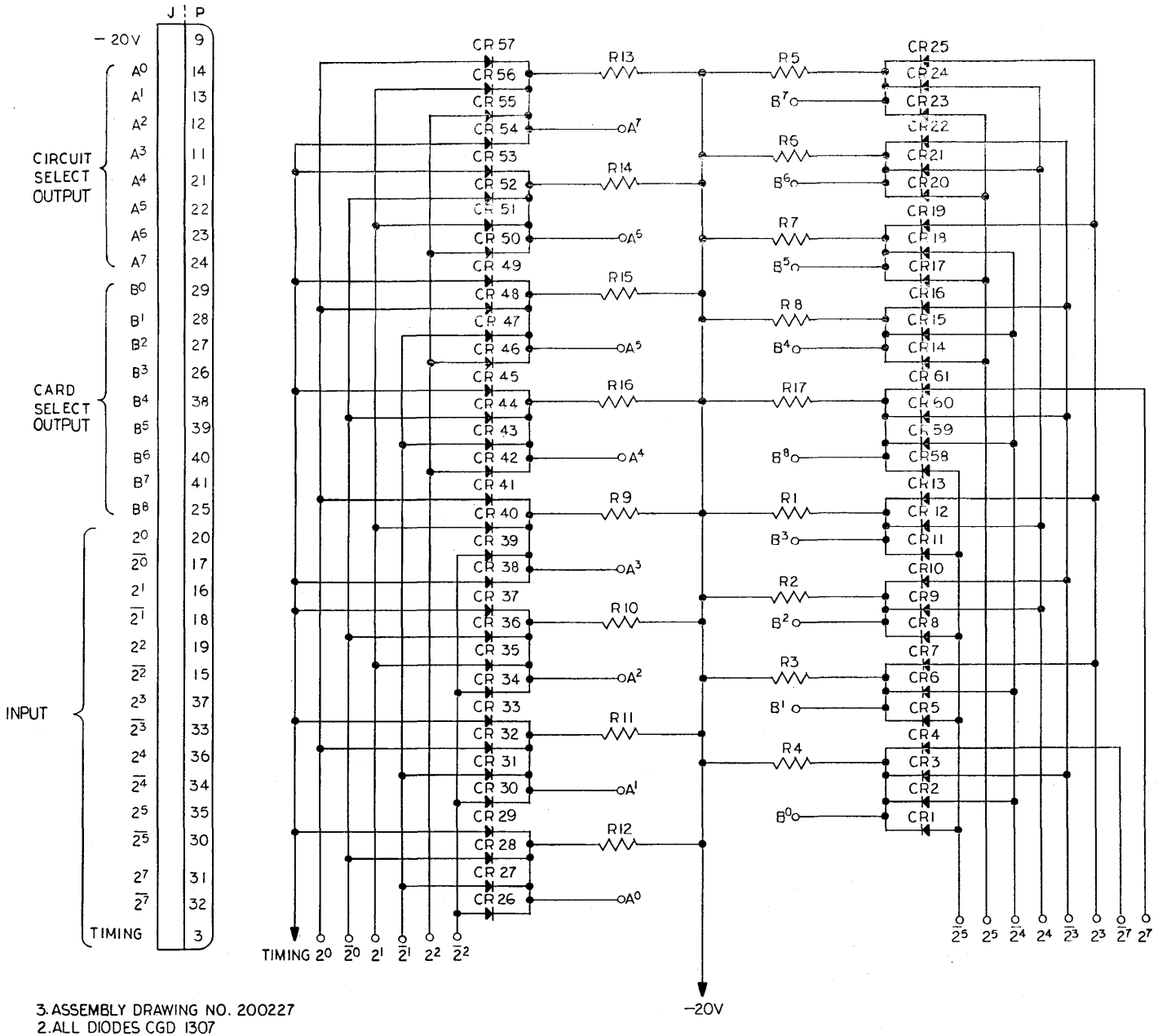
NOTES: UNLESS OTHERWISE SPECIFIED.

data products corporation
CULVER CITY, CALIFORNIA

TITLE: CIRCUIT BOARD ASSY. 3D3
PAPER FEED CONTROL

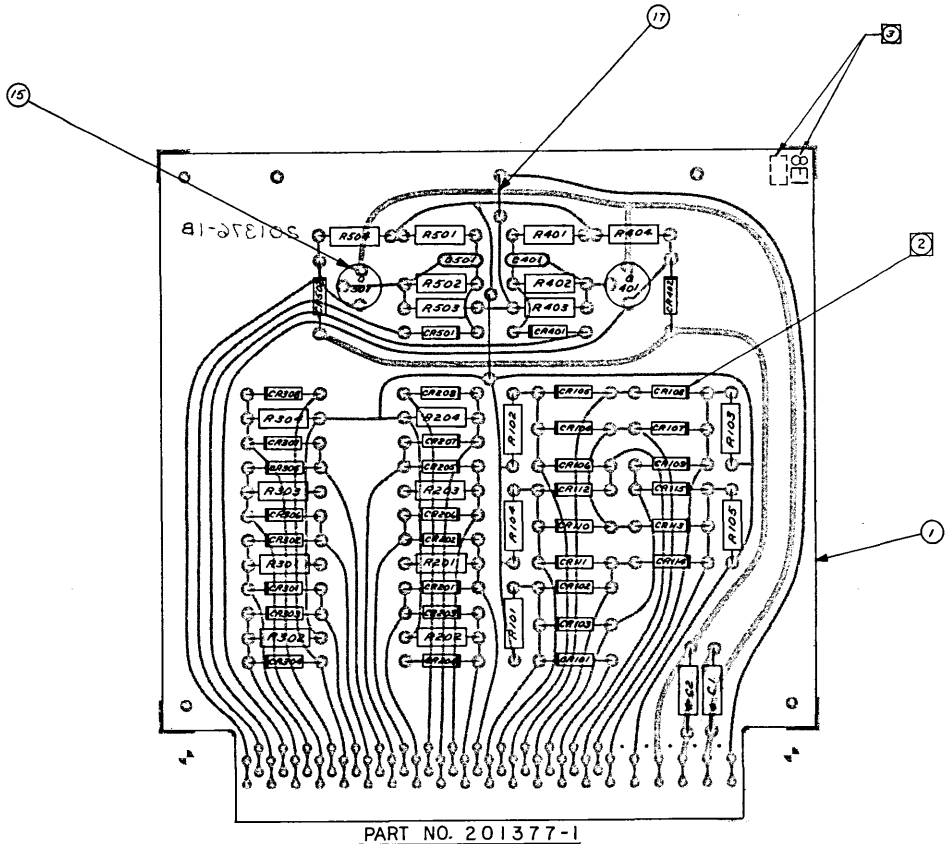
D | DRAWING NO. 202074 | REV E

SHEET 1 | CONT. ON ——



3. ASSEMBLY DRAWING NO. 200227
2. ALL DIODES CGD 1307
1. ALL RESISTORS 6.8K ± 5% ½ W
NOTE: UNLESS OTHERWISE SPECIFIED

data products corporation CULVER CITY, CALIFORNIA		
TITLE: SCHEMATIC DECODE 8A1		
	DRAWING NUMBER C 200224	REV. B



PART NO. 201377-1

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION
17	A/R		WIRE (22GA)	
16				
15	2	RC-05030-IN	TRANSIPAD (ROBINSON)	
14	2	2N1303	TRANSISTOR	Q401, Q501
13				
12	2	EB4725	RESISTOR 4.7K ⅛W ±5% (A.B.)	R404, R504
11	2	EB3925	RESISTOR 3.9K ⅛W ±5% (A.B.)	R402, R502
10	2	EB6225	RESISTOR 6.2K ⅛W ±5% (A.B.)	R401, R501
9	2	EB2735	RESISTOR 27K ⅛W ±5% (A.B.)	R403, R503
8	13	EB4735	RESISTOR 47K ⅛W ±5% (A.B.)	R101-R304
7				
6	35	200505-1	DIODE	CR101-CR502
5				
4	2	DM15-621J	CAPACITOR 620 pf ±5% 300V	C401, C501 (ARCO)
3	2	1300D106F003B2	CAPACITOR 10 µf 20V ±20% (SPRAGUE)	C1, C2
2				
1	1	201376-1	PROCESSED BOARD DECODE 8E	

data products corporation
CULVER CITY, CALIFORNIA

TITLE ASSEMBLY DECODE 8E1

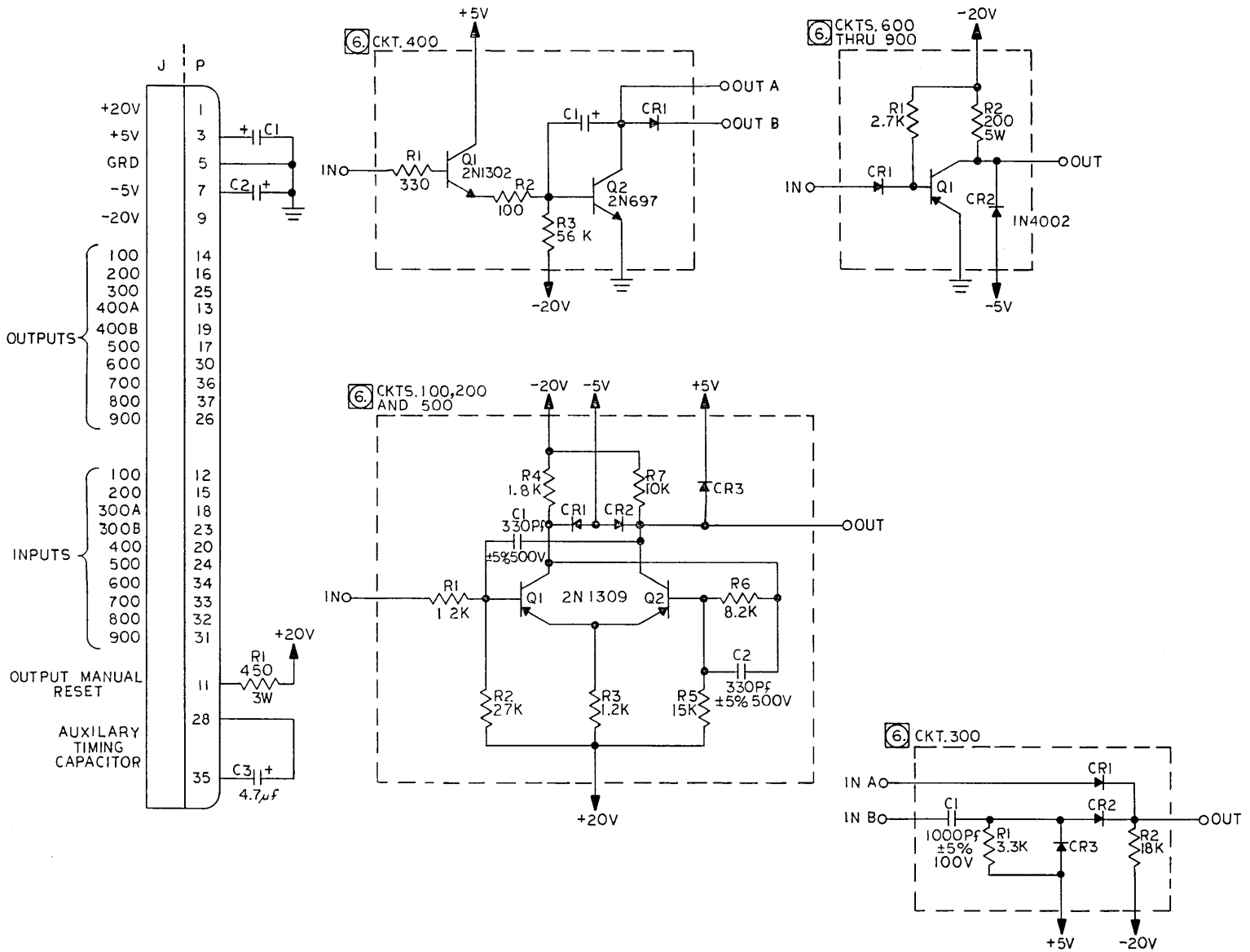
D | DRAWING NO. 201377 | REV B

SHEET 1 CONT. ON —

9 STAMP BOARD TYPE 8E1 AND CURRENT ASS'Y REV. LETTER ⅛" HIGH BLACK IN UPPER RIGHT CORNER
2 STRIPE ON DIODE INDICATES CATHODE. —|>|—

1. SCHEMATIC DRAWING NO. 201374.

NOTES: UNLESS OTHERWISE SPECIFIED



6 REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE PART DESIGNATION WITH THE SUBASSEMBLY DESIGNATION.

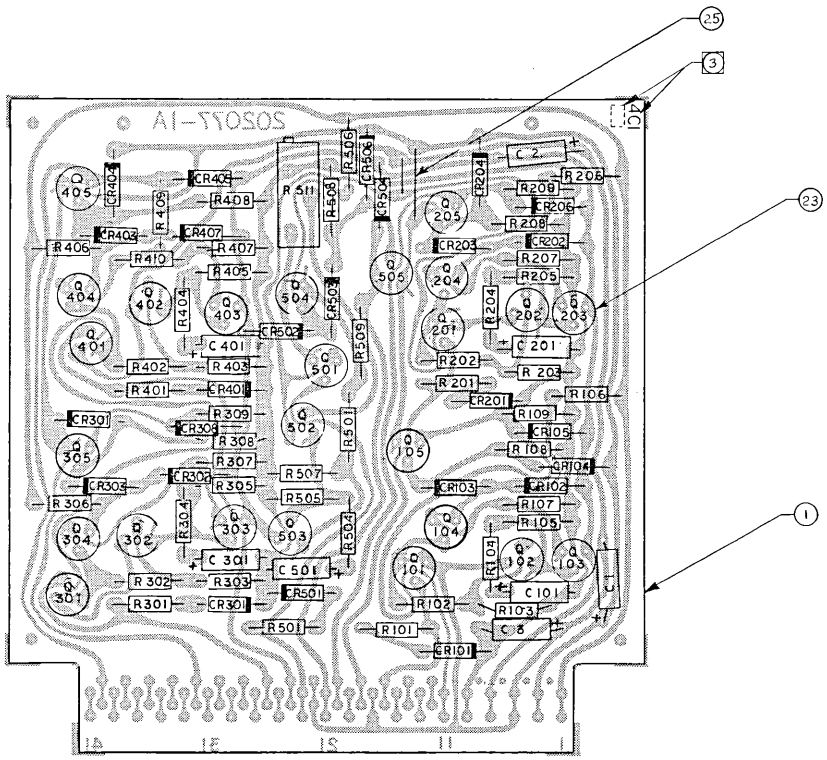
5. ASSEMBLY DRAWING NO. 202074
4. ALL CAPACITORS 10μf, ±20% 20V
3. ALL DIODES 200505-1
2. ALL TRANSISTORS 2N1303
1. ALL RESISTOR VALUES IN OHMS ±5%, 1/2W

NOTES: UNLESS OTHERWISE SPECIFIED.

data products corporation
CULVER CITY, CALIFORNIA

TITLE SCHEMATIC 3D3
PAPER FEED CONTROL

C | DRAWING NO. 202071 | REV B
SHEET 1 CONT. ON —



[3] MARK BOARD TYPE NO. AND CURRENT ASSY. REVISION LETTER IN UPPER RIGHT CORNER OF BOARD AS SHOWN 1/8 HIGH, COLOR, BLACK.

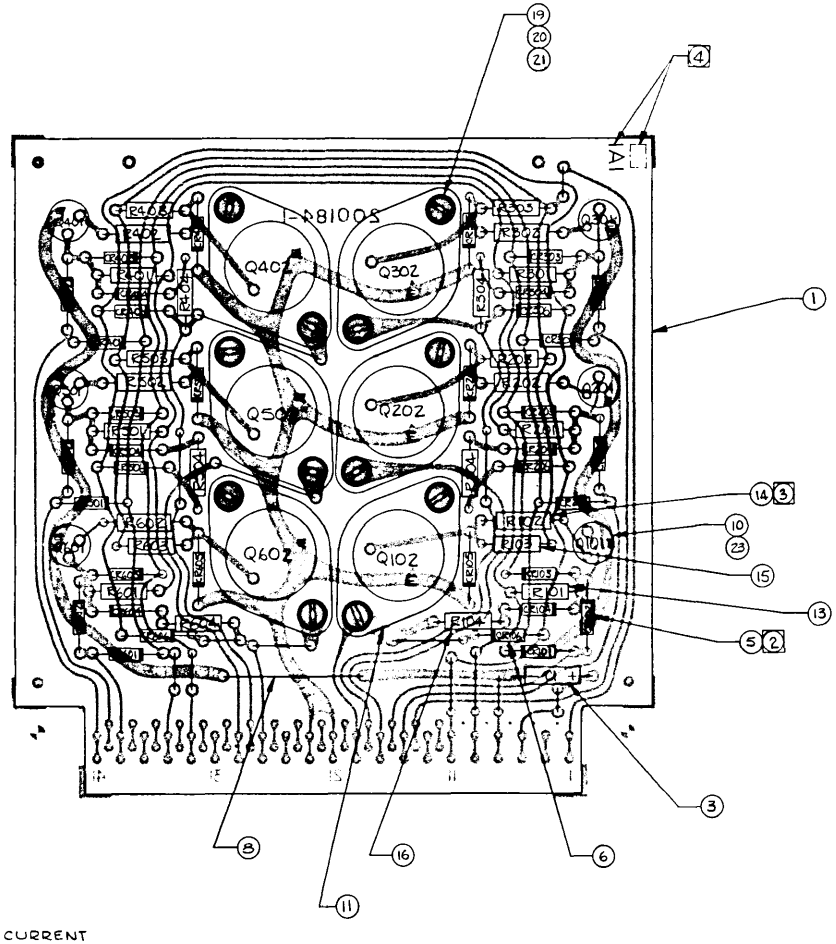
[2] STRIPE ON DIODE INDICATES CATHODE —▷|—

1. FOR CIRCUIT SEE SCHEMATIC DWG NO. 202075.

NOTES: UNLESS OTHERWISE SPECIFIED.

dp data products corporation, CULVER CITY, CALIFORNIA		
TITLE: CIRCUIT BOARD ASSY. PHOTO DIODE AMPL. 4CI		
D	DRAWING NO. 202078	REV D
	SHEET 1 CONT. ON ——	

NO.	E.C.O. NO.	REVISION	APP'D.	DATE
A		LIMITED USAGE RELEASE		4/6/62
B		PRODUCTION RELEASE		9/7/62
C	295	IC 2N456A WAS 2N457A IC 1A2 WAS 1A1		11/15/62
D	457	J.F. ECO 397		2/4/63



4 STAMP BOARD TYPE, 1A1, AND CURRENT ASSY. REV. LETTER IN UPPER RIGHT HAND CORNER OF BOARD AS SHOWN, 1/8 HIGH.
3 ITEM 14 SHALL BE ELEVATED FROM BOARD 1/16.
2 STRIPE ON DIODE, INDICATES DIRECTION OF CATHODE.
1. SCHEMATIC DRAWING NO. 200182

NOTES: UNLESS OTHERWISE SPECIFIED

DRAWING NUMBER D 200185 REV. D

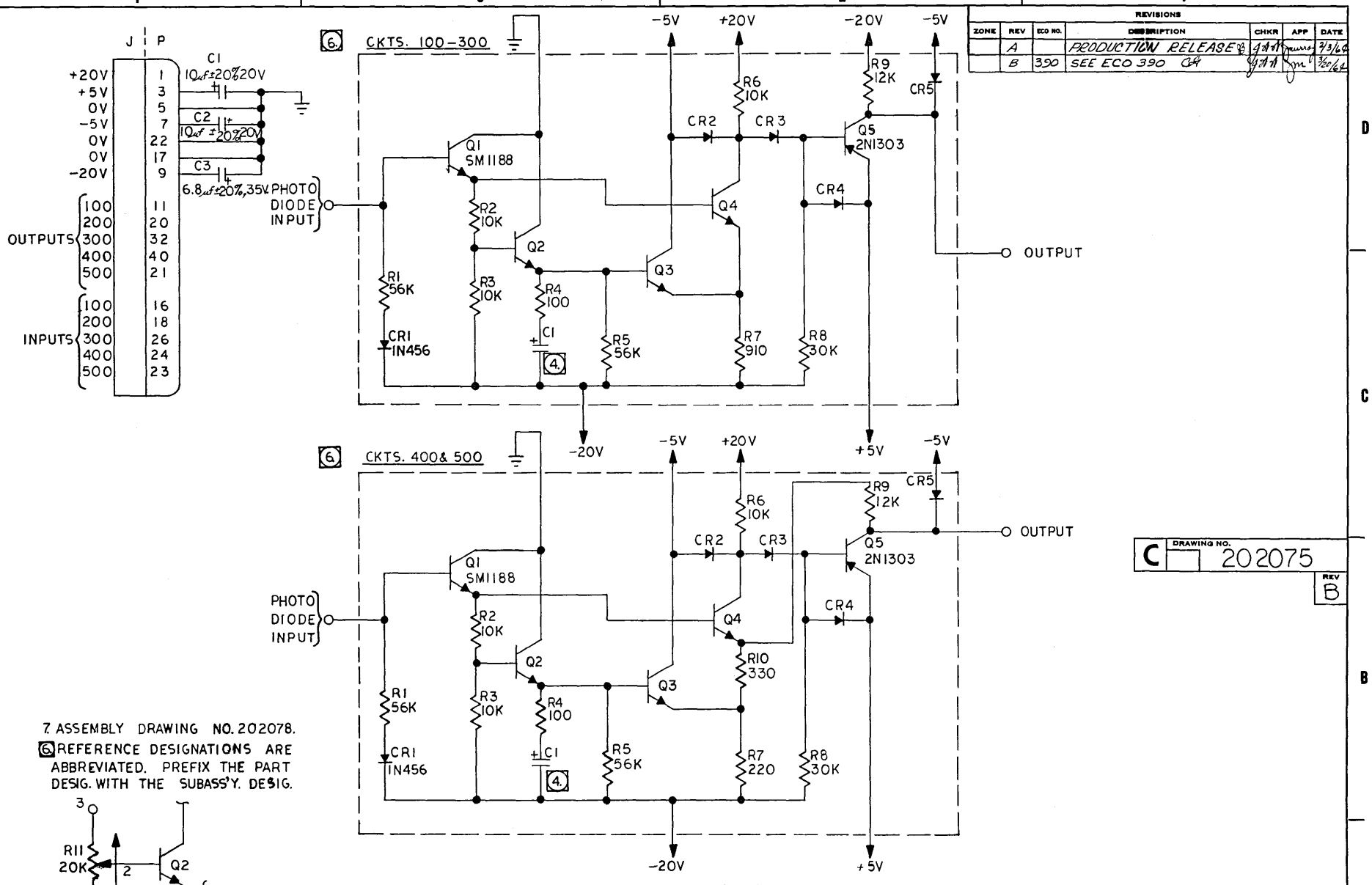
ITEM	PART NO.	REQ'D	DESCRIPTION
29			
28			
27			
26			
25			
24			
23	603090	6	TRANSIPAD (F.D. ADAMS)
22			
21	4-40	12	NUT - PLAIN HEX, CAD PLATE
20	NO. 4	24	WASHER - EXTR. TOOTH, CAD PLATE
19	4-40 x 5/16	12	SCREW - PAN HEAD, CAD PLATE
18			
17			
16	EB8215	6	RESISTOR 820Ω, ±5%, ½W (AB) R104-R604
15	EB1525	6	1.5K, ±5%, ½W (AB) R103-R603
14	VAL 3-100	6	100Ω, 3W (TRU-OHM) R102-R602
13	EB2725	6	RESISTOR 2.7K, ±5%, ½W (AB) R101-R601
12			
11	2N456A	6	TRANSISTOR (DELCO) Q102-Q602
10	2N1302	6	TRANSISTOR (T.I.) Q101-Q601
9			
8		A/R	JUMPER, WIRE (#22)
7			
6	1N457	6	DIODE (T.I.) CR106 THRU CR606
5	CG01307	30	DIODE (CLEVITE) CR101-CR105 THRU CR601-CR605
4			
3	150D106X0020B2	1	CAPACITOR, 10μf ±20% 20V (SPRAGUE) C1
2			
1	200184-1	1	PROCESSED BOARD - HAMMER DR. 1A2

	dp/P 3500	MATERIAL:	SCALE: 2/1
NEXT ASSY.	USED ON		TOLERANCES UNLESS OTHERWISE NOTED
DES. BY		FINISH:	DECIMAL ±
DR. BY	12/7/62		FRACTION ±
CHD. BY	6/7/63		ANGULAR ±
APP. BY			DIMENSIONS APPLY AFTER PLATING & HEAT TREATING
APP. BY			SHEET 1 OF 1

dp data products corporation
CULVER CITY, CALIFORNIA

TITLE: CIRCUIT BOARD ASSY HAMMER DRIVER 1A2

DRAWING NUMBER D 200185 REV. D



7. ASSEMBLY DRAWING NO. 202078.

6. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE PART DESIG. WITH THE SUBASS'Y. DESIG.

5. ON CKT. 500 R2 & R3 ARE POTENTIOMETER R11.

4. CAPACITOR C1 ON CKT. 500, .047μf ± 10%, 200V.
CAPACITOR C1 ON CKTS. 100-400, 10μf ±20%, 20V.

3. ALL RESISTOR VALUES IN OHMS ± 5% 1/2W.

2. ALL TRANSISTORS 2N1302.

1. ALL DIODES 200505-1.

NOTES: UNLESS OTHERWISE SPECIFIED.

REVISIONS

ZONE	REV	ECO NO.	DESCRIPTION	CHKR	APP	DATE
	A		PRODUCTION RELEASE	gbh	[illegible]	2/3/64
	B	390	SEE ECO 390 C4	gbh	jm	2/20/64

C DRAWING NO. 202075 REV B

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

LIST OF MATERIAL

SUPPLEMENTARY INFORMATION		NAME	DATE
FIRST USED ON 252003-2 dp/p3310	DES		
NEXT ASSEMBLY	DRFT	Barron	1/27/64
	CHKR	gbhickman	28 JAN 1964
	APP	B Tanigucki	2/3/64
	APP	R K Merry	2/3/64

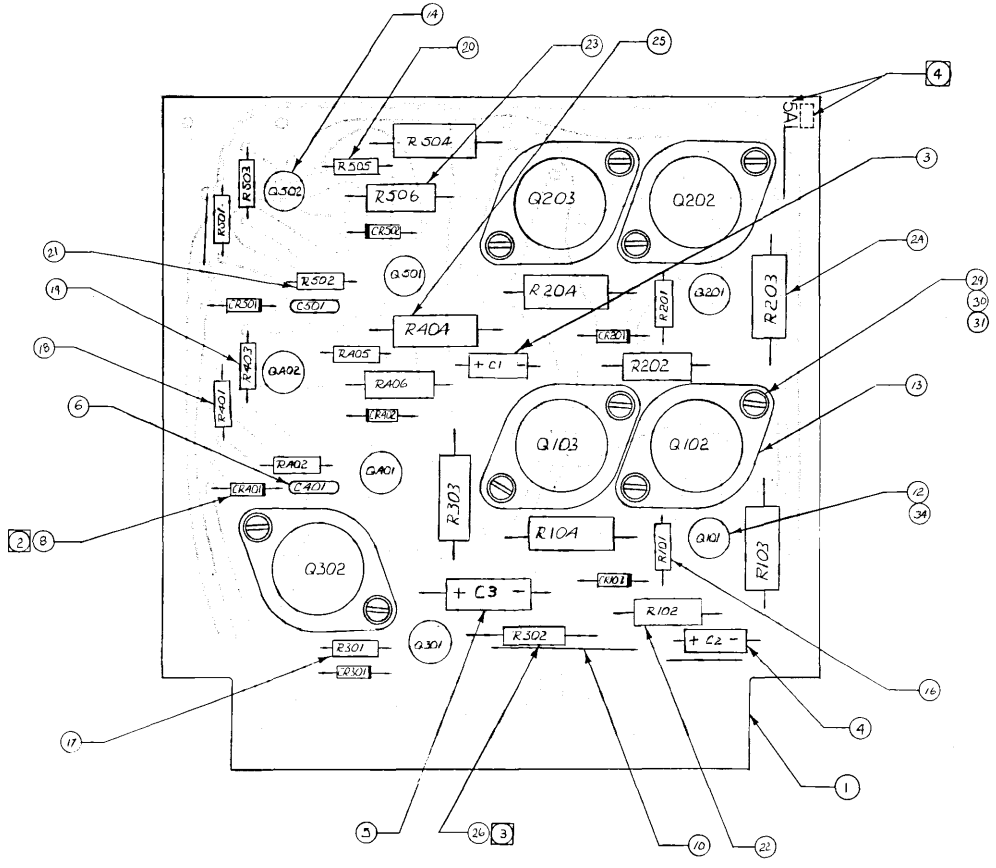
MATERIAL
FINISH
DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

SCALE
DO NOT SCALE DWG
ALL DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL
FRACTION
ANGLE

data products corporation
CULVER CITY, CALIFORNIA

TITLE SCHEMATIC 4C1
PHOTO DIODE AMPLIFIER

C DRAWING NO. 202075 REV B
SHEET CONT. ON



34	100068	7	TRANSIPAD
33			
32			
31	A-40	10	NUT-PLAIN HEX, CAD PLATE
30	NOA	20	WASHER-EXTR. TOOTH, CAD PLATE
29	4-40 X 1/4	10	SCREW-PAN HEAD, CAD PLATE

28			
27			
26	242E5015	1	RESISTOR 500Ω ± 5% 3W(SPRAGUE) R302
25	HB1225	2	1.2K ± 5% 2W(AB) R404, R504
24	HB1525	5	1.5K ± 5% 2W(AB) R204, R304, R404, R503, R505
23	GB3325	2	3.3K ± 5% 1W(AB) R406, R506
22	GB1525	2	1.5K ± 5% 1W(AB) R102, R202
21	EB1525	2	1.5K ± 5% ½W(AB) R402, R502
20	EB2205	2	22Ω ± 5% ½W(AB) R405, R505
14	EB1235	2	12K ± 5% ¼W(AB) R403, R503
18	EB4325	2	4.3K ± 5% ¼W(AB) R401, R501
17	EB3325	1	3.3K ± 5% ¼W(AB) R301
16	EB6825	2	RESISTOR 6.8K ± 5% ¼W (AB) R101, R201
15			
14	2N1384	4	TRANSISTOR Q401, Q402, Q501, Q502
13	2N456A	5	TRANSISTOR Q102, Q103, Q203, Q202, Q302
12	2N1303	3	TRANSISTOR Q101, Q201, Q301
11			
10		A/R	WIRE #22 GA.
9			
8	CGD1307	7	DIODE CR101 - CR502
7			
6	DM15-331-J	2	CAPACITOR 330 pf ± 5% 500V (ARCO) C401, C501
5	150D226X0035R2	1	CAPACITOR 22 μf ± 20% 35V (SPRAGUE) C3
4	150D106X0020B2	1	CAPACITOR 10 μf ± 20% 20V (SPRAGUE) C2
3	500D685T005S2	1	CAPACITOR 6.8 μf ± 20% 35V (SPRAGUE) C1
2			
1	200175-1	1	PROCESSED BOARD, HAMMER DR. POWER AMP. SA1
ITEM	PART NO.	REQ'D	DESCRIPTION

4 STAMP BOARD TYPE SA1, AND CURRENT ASSY. REV. LETTER IN UPPER RIGHT HAND CORNER OF BOARD AS SHOWN, 1/8" HIGH.

3 ITEM 26 SHALL BE ELEVATED 1/4" FROM BOARD.

2 STRIPE ON DIODE, INDICATES DIRECTION OF CATHODE.

1 SCHEMATIC DRAWING NO. 200173.

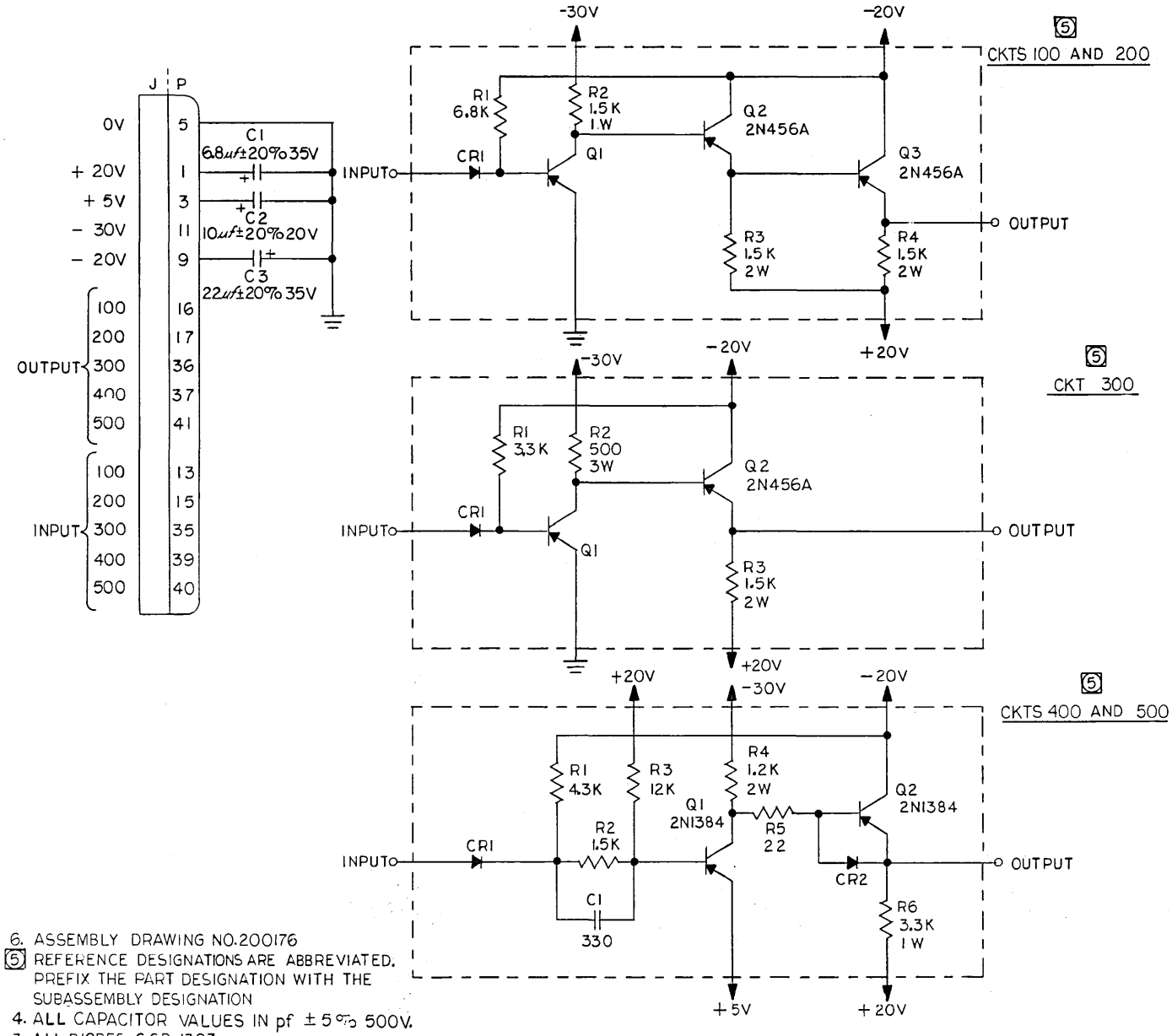
NOTE: UNLESS OTHERWISE SPECIFIED

data products corporation
CULVER CITY, CALIFORNIA

TITLE: CIRCUIT BOARD ASSY-
HAMMER DR. POWER AMP SA1

D | DRAWING NUMBER 200176 | REV. B

NO.	E.C.O. NO.	REVISION	APP'D.	DATE
B		REDRAWN-PRODUCTION RELEASE		



6. ASSEMBLY DRAWING NO.200176
5. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE PART DESIGNATION WITH THE SUBASSEMBLY DESIGNATION
4. ALL CAPACITOR VALUES IN pf ± 5% 500V.
3. ALL DIODES CGD 1307
2. ALL RESISTOR VALUES IN OHMS ± 5% ½ W
1. ALL TRANSISTORS 2N1303

NOTE UNLESS OTHERWISE SPECIFIED

NEXT ASS'Y.	dp/p3300	USED ON	
DES. BY			
DR. BY	KUBOTA	12-4-62	
CKD. BY		5-2-63	
APP. BY		5-10-63	
APP. BY		5-10-63	

MATERIAL:

FINISH:

SCALE: NONE

TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL ±
FRACTION ±
ANGULAR ±
DIMENSIONS APPLY AFTER PLATING & HEAT TREATING

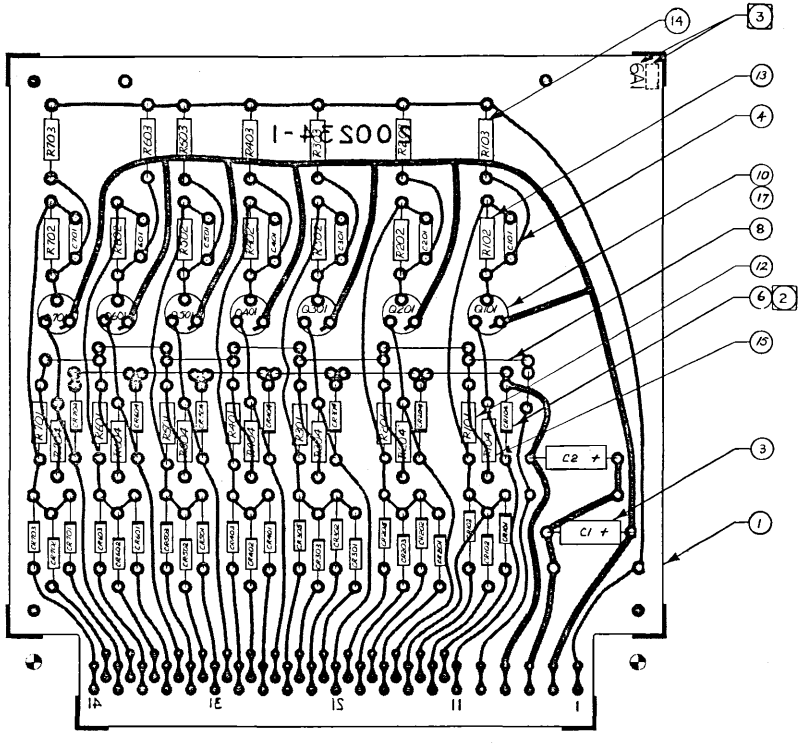
SHEET | OF |

data products corporation
CULVER CITY, CALIFORNIA

TITLE: SCHEMATIC HAMMER DRIVER POWER AMP. 5A1

DRAWING NUMBER C 200173 REV. B

DRAWING NUMBER C 200173 REV. B



PART NO. 200235-1

ITEM	REQD	PART NO.	DESCRIPTION	REF. DESIGNATION
20				
19				
18				
17	7	RC05090-IN	TRANSIPAD (ROBINSON)	
16				
15	7	EB2725	RESISTOR 2.7K ±5% 1/2W (A.B.)	R104 - R704
14	7	EB1235	↑ 12K ±5% 1/2W (A.B.)	R103 - R703
13	7	EB1525	↓ 1.5K ±5% 1/2W (A.B.)	R102 - R702
12	7	EB4325	RESISTOR 4.3K ±5% 1 2W (A.B.)	R101 - R701
11				
10	7	2N1303	TRANSISTOR	Q101 - Q701
9				
8	A/R		WIRE #22 GA.	
7				
6	30	CGD 1307	DIODE	CR101 - CR701, CR102 - CR702, CR103 - CR703, CR104 - CR704, CR205, CR305
5				
4	7	DM15-621J	CAPACITOR 620 pf ±5% 300V (ARCO)	C101 - C701
3	2	150D106*C02082	CAPACITOR 10 µf ±20% 20V (SPRAGUE)	C1, C2
2				
1	1	200234-1	PROCESS BOARD, NOR GATE 6A1	

p data products corporation
CULVER CITY, CALIFORNIA

TITLE: CIRCUIT BOARD ASSY- NOR GATE 6A1

D | DRAWING NUMBER 200235 | REV. B

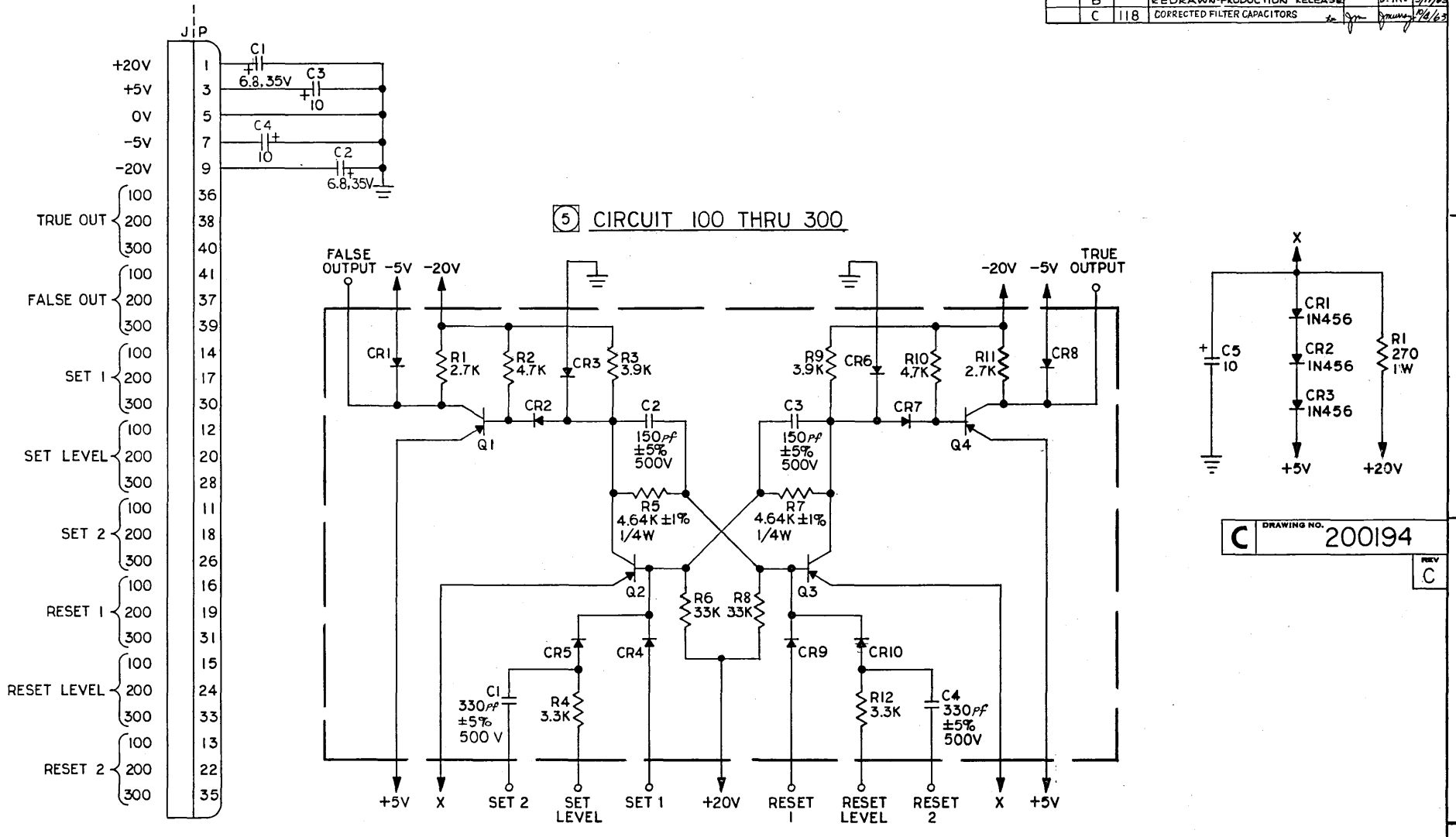
[3] STAMP BOARD TYPE 6A1, AND CURRENT ASSY. REV. LETTER IN UPPER RIGHT HAND CORNER OF BOARD AS SHOWN, 1/8" HIGH

[2] STRIPE ON DIODE INDICATES CATHODE.

1. SCHEMATIC DRAWING NO 200232

NOTE: UNLESS OTHERWISE SPECIFIED

REVISIONS						
ZONE	REV	ECO NO.	DESCRIPTION	CHKR	APP	DATE
	B		REDRAWN-PRODUCTION RELEASE			5/17/63
	C	118	CORRECTED FILTER CAPACITORS			10/8/63



C	DRAWING NO. 200194	REV C

6. ASSEMBLY DRAWING NO. 200197.
5. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE PART DESIGNATION WITH THE SUBASSEMBLY DESIGNATION.
4. ALL CAPACITOR VALUES IN $\mu f \pm 20\%$ 20V.
3. ALL DIODES CGD 1307.
2. ALL TRANSISTORS 2N1303.
1. ALL RESISTOR VALUES IN OHMS ±5% 1/2W.

NOTES: UNLESS OTHERWISE SPECIFIED

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

LIST OF MATERIAL

SUPPLEMENTARY INFORMATION		NAME	DATE
FIRST USED ON	dp/P 3300	DES	
NEXT ASSEMBLY		DRFT	V. TILL 5-1-63
		CHKR	5-8-63
		APP	5-8-63
		APP	5-10-63

MATERIAL / FINISH

DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

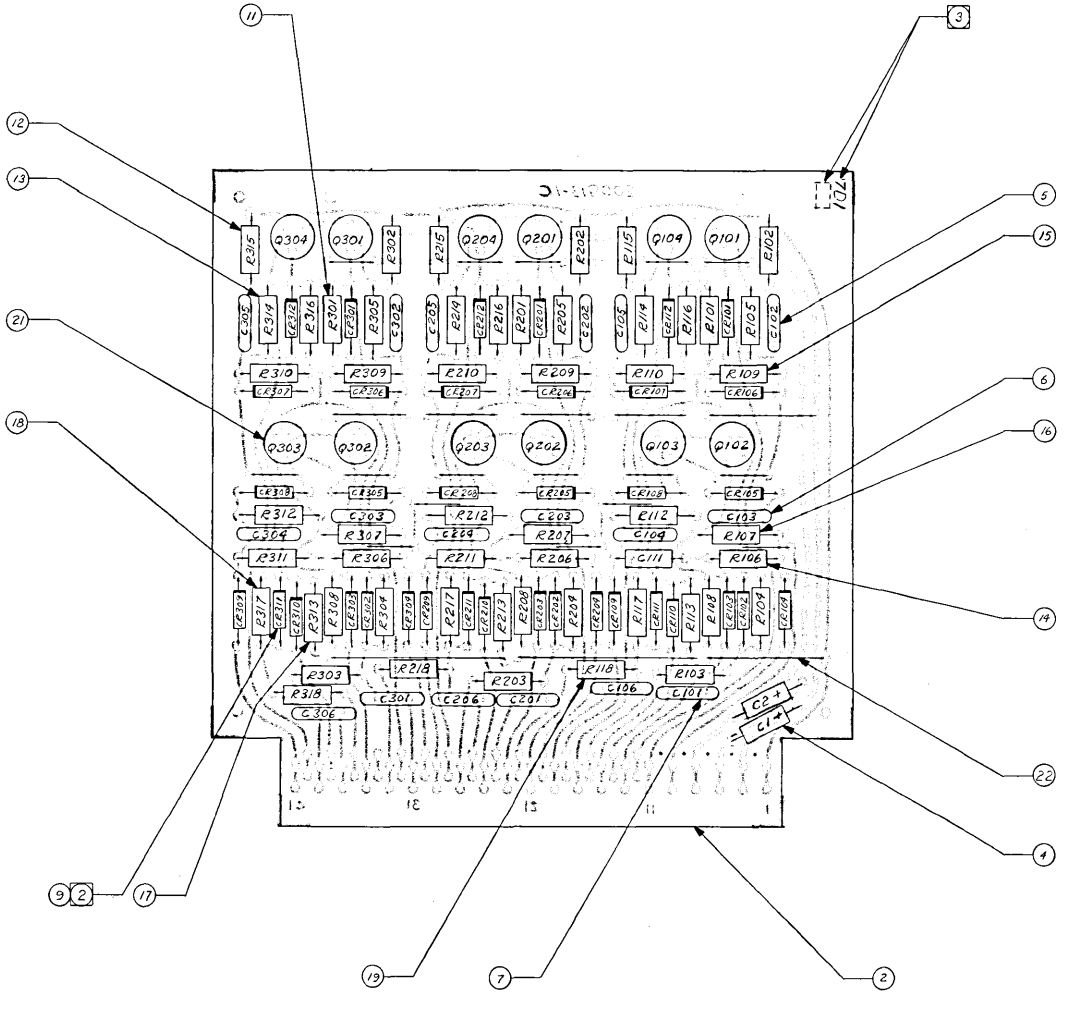
SCALE NONE
DO NOT SCALE DWG
ALL DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL ±
FRACTION ±
ANGLE ±

data products corporation
CULVER CITY, CALIFORNIA

TITLE: SCHEMATIC FLIP FLOP 7A2

C	DRAWING NO. 200194	REV C

SHEET 1 CONT. ON



3. STAMP BOARD TYPE 7D1, AND CURRENT ASSY. REV. LETTER IN UPPER RIGHT HAND CORNER OF BOARD AS SHOWN, BLACK, 1/8" HIGH.

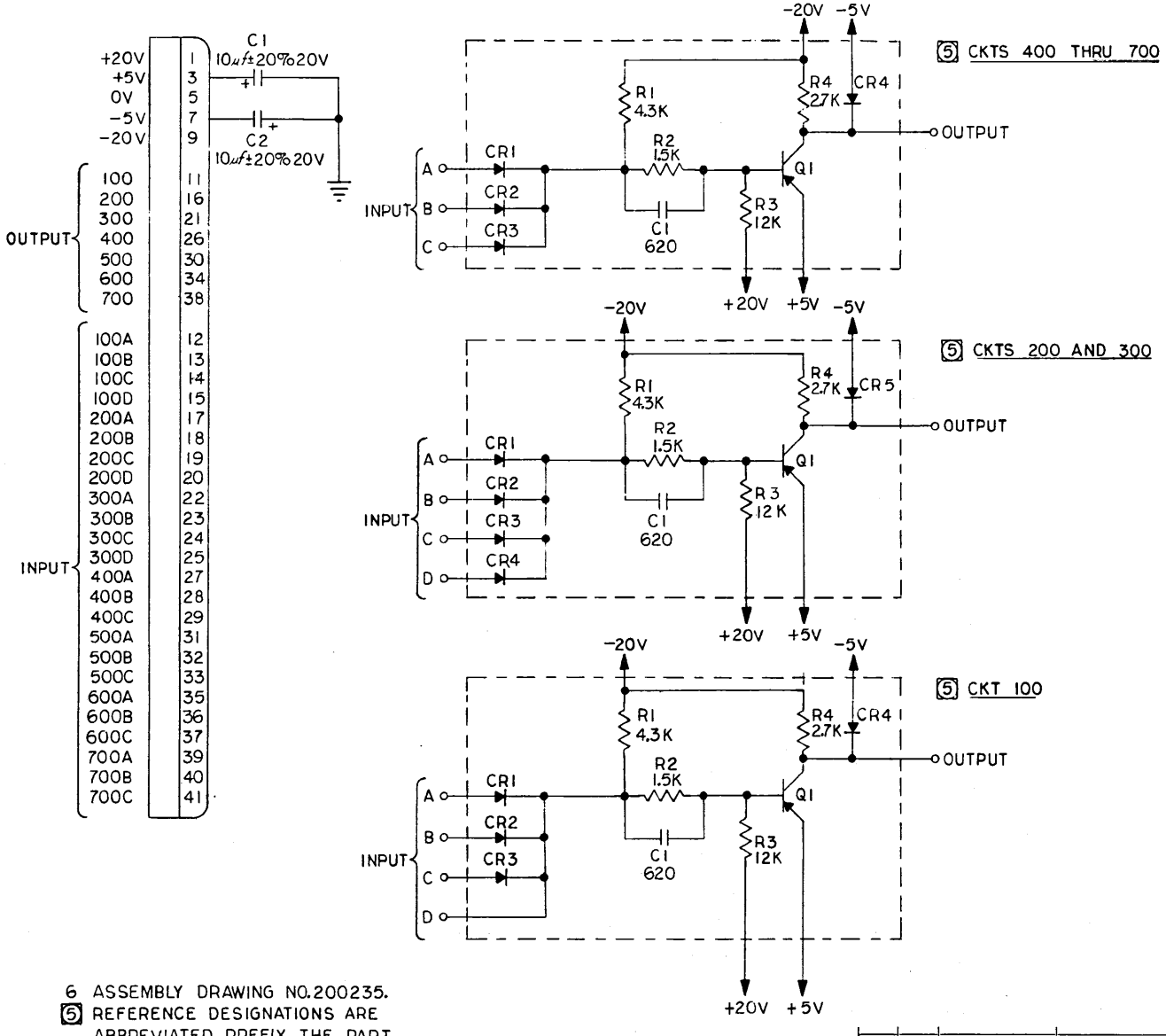
2. STRIPE ON DIODE INDICATES CATHODE. -|▶|-

1. SCHEMATIC DRAWING NO. 200911

NOTES: UNLESS OTHERWISE SPECIFIED.

data products corporation, CULVER CITY, CALIFORNIA	
TITLE: ASSEMBLY FLIP FLOP 7D1	
D	DRAWING NO. 200914 — REV C
	SHEET 1 CONT. ON —

REVISIONS						
ZONE	REV	ECO NO.	DESCRIPTION	CHKR	APP	DATE
	B		REDRAWN - PRODUCTION RELEASE		B.M.S.	5/17/63
1/A	C	413	SEE ECO 413	B.Heere		5/28/63



6 ASSEMBLY DRAWING NO. 200235.
5 REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE PART DESIGNATION WITH THE SUBASSEMBLY DESIGNATION.
4 ALL CAPACITOR VALUES IN Pf ±5% 300V.
3 ALL DIODES CGD 1307.
2 ALL TRANSTORS 2N1303.
1 ALL RESISTOR VALUES IN OHMS ± 5% 1/2W.
NOTE: UNLESS OTHERWISE SPECIFIED

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

LIST OF MATERIAL

SUPPLEMENTARY INFORMATION		NAME	DATE
FIRST USED ON	DES		
NEXT ASSEMBLY	DRFT	ELB	4/11/63
	CHKR		5-2-63
	APP		5-10-63
	APP		5-10-63

MATERIAL
FINISH
DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

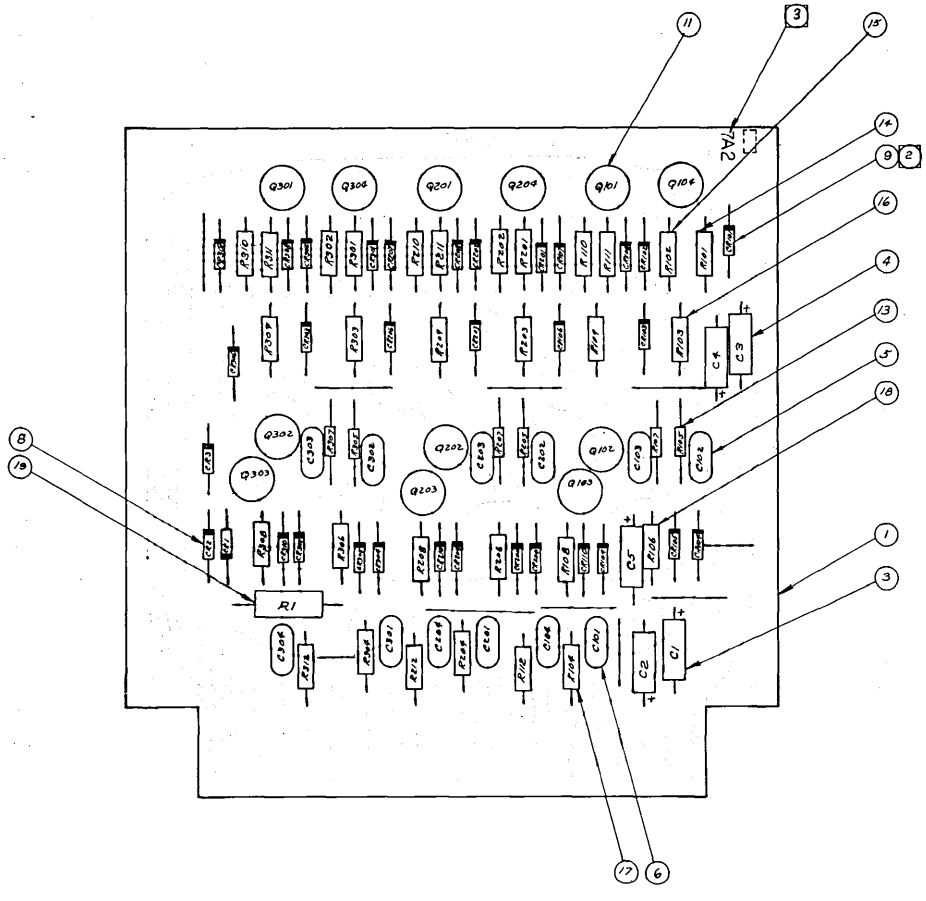
SCALE NONE
DO NOT SCALE DWG
ALL DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL ±
FRACTION ±
ANGLE ±

data products corporation
CULVER CITY, CALIFORNIA

TITLE
SCHEMATIC
NOR GATE 6A2

DRAWING NO. C 200232 REV C
SHEET CONT. ON

C DRAWING NO. 200232 REV C



PART NO 200197-1

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION
19	1	6B 2715	RESISTOR - 870 Ω ±5% 1W (BB)	R1
18	6	EB 3335	RESISTOR - 33K ±5% ½W (BB)	R104, R204, R304, R108, R208, R308
17	6	EB 3325	RESISTOR 3.3K ±5% ½W (BB)	R104, R204, R304, R112, R212, R312
16	6	EB3925	3.9K ±5% ½W (BB)	R103, R203, R303, R103, R209, R309
15	6	EB4725	4.7K ±5% ½W (BB)	R102, R202, R302, R110, R210, R310
14	6	EB2725	2.7K ±5% ½W (BB)	R101, R201, R301, R111, R211, R311
13	6		RESISTOR 4.64K ±1% ½W (TI)	R105, R205, R305, R107, R207, R307
12				
11	12	2N1303	TRANSISTOR	Q101 THRU Q304
10				
9	30	200505-1	DIODE	CR101 THRU C310
8	3	IN456	DIODE	CR1, CR2, CR3
7				
6	6	DM15-331J	CAPACITOR 330 pf ±5% 500V (APCO)	C101 C201 C301, C104 C204 C304
5	6	DM15-151J	150 pf ±5% 300V (RACO)	C102 C202 C302, C103, C203, C303
4	3	150D106X0020B2	10 µf ±20% 20V (SPRAGUE)	C3, C4 & C5
3	2	150D685X0020B2	CAPACITOR-6.8 µf ±20%, 35V (SPRAGUE)	C1 & C2
2				
1	1	200196-1	PROCESS BOARD-FLIP FLOP 7A2	

[3] STAMP BOARD TYPE 7A2 AND CURRENT ASSY REV LETTER IN UPPER RIGHT CORNER AS SHOWN 1/8" HIGH.

[2] STRIPE ON DIODE INDICATES CATHODE.

1. SCHEMATIC DWG NO 200194

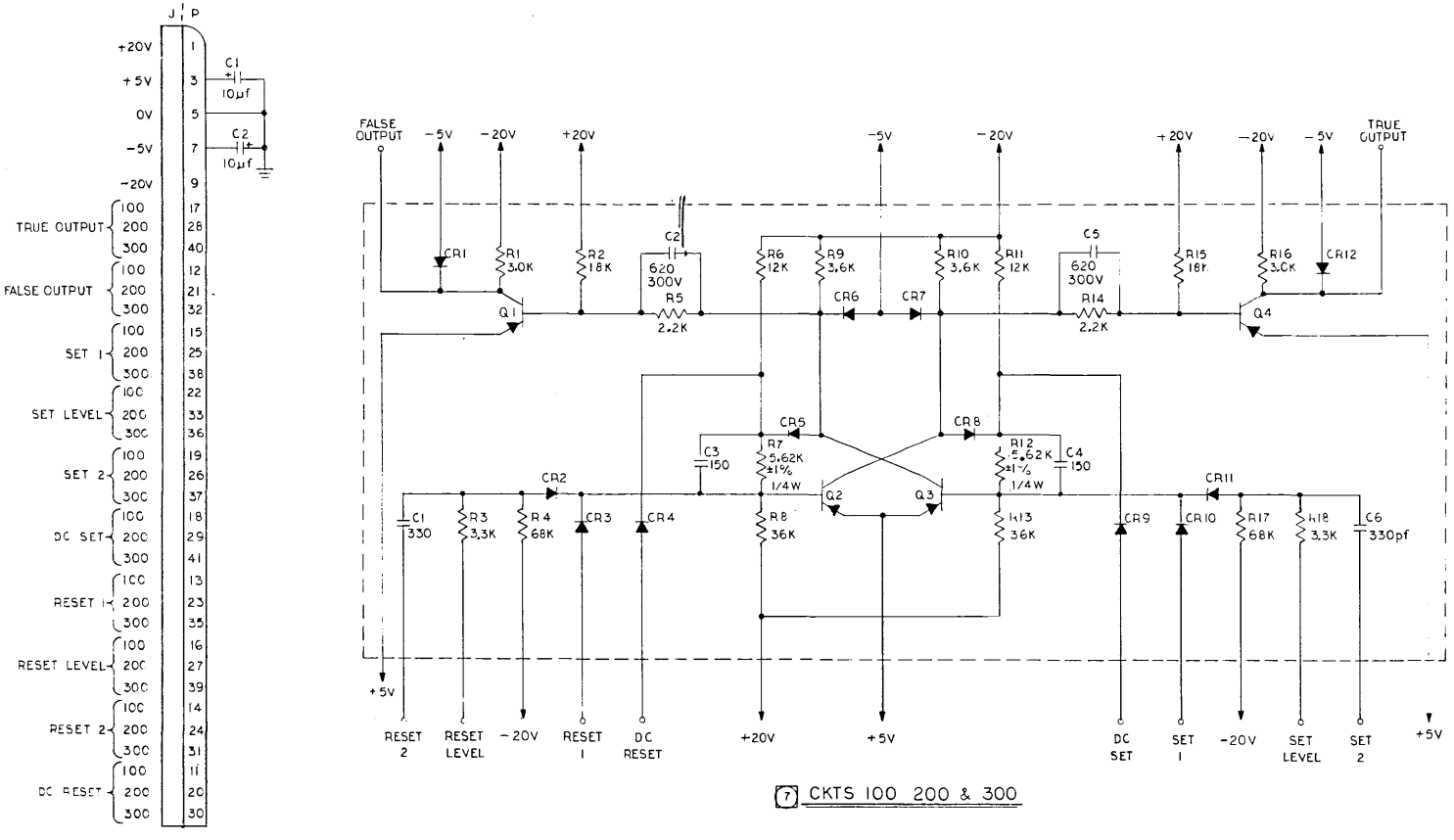
NOTES: UNLESS OTHERWISE SPECIFIED.

d data products corporation
CULVER CITY, CALIFORNIA

TITLE
CKT BD ASSY
FLIP FLOP 7A2

SIZE	DRAWING NO.	REV
D	200197	D

SHEET 1 CONT. ON ~



7 CKTS 100 200 & 300

7 REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE PART DESIGNATION WITH THE SUBASSEMBLY DESIGNATION

6 ASSEMBLY DWG NO. 200914

5 ALL 10uf CAPACITORS, ±20%, 20V

4. ALL CAPACITOR VALUES IN pf, ±5%, 500V

3. ALL RESISTOR VALUES IN OHMS, ±5%, 1/2W

2. ALL DIODES 200505-1

1. ALL TRANISTORS 2N1303

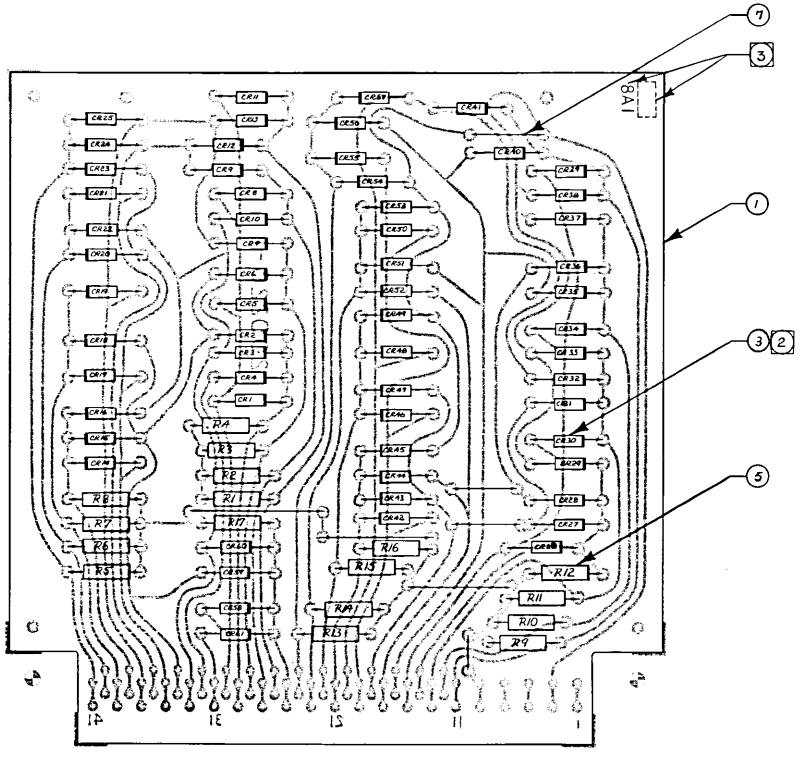
NOTES: UNLESS OTHERWISE SPECIFIED.

data products corporation
CULVER CITY, CALIFORNIA

TITLE SCHEMATIC — FLIP FLOP 7D1

D | DRAWING NO. 200911 | REV B

SHEET 1 CONT. ON ~



8			
7		A R	WIRE (#22)
6			
5	EB 6825	17	RESISTOR 6.8K ± 5% ¼W (AB) R1-R17
4			
3	CGD 1307	61	DIODES (CLEVITE) CR1-CR61
2			
1	200226-1	1	PROCESSED BOARD DECODE BA1
ITEM	PART NO	REQD	

dP data products corporation
CULVER CITY, CALIFORNIA

TITLE: CIRCUIT BOARD ASSY-
DECODE BA1

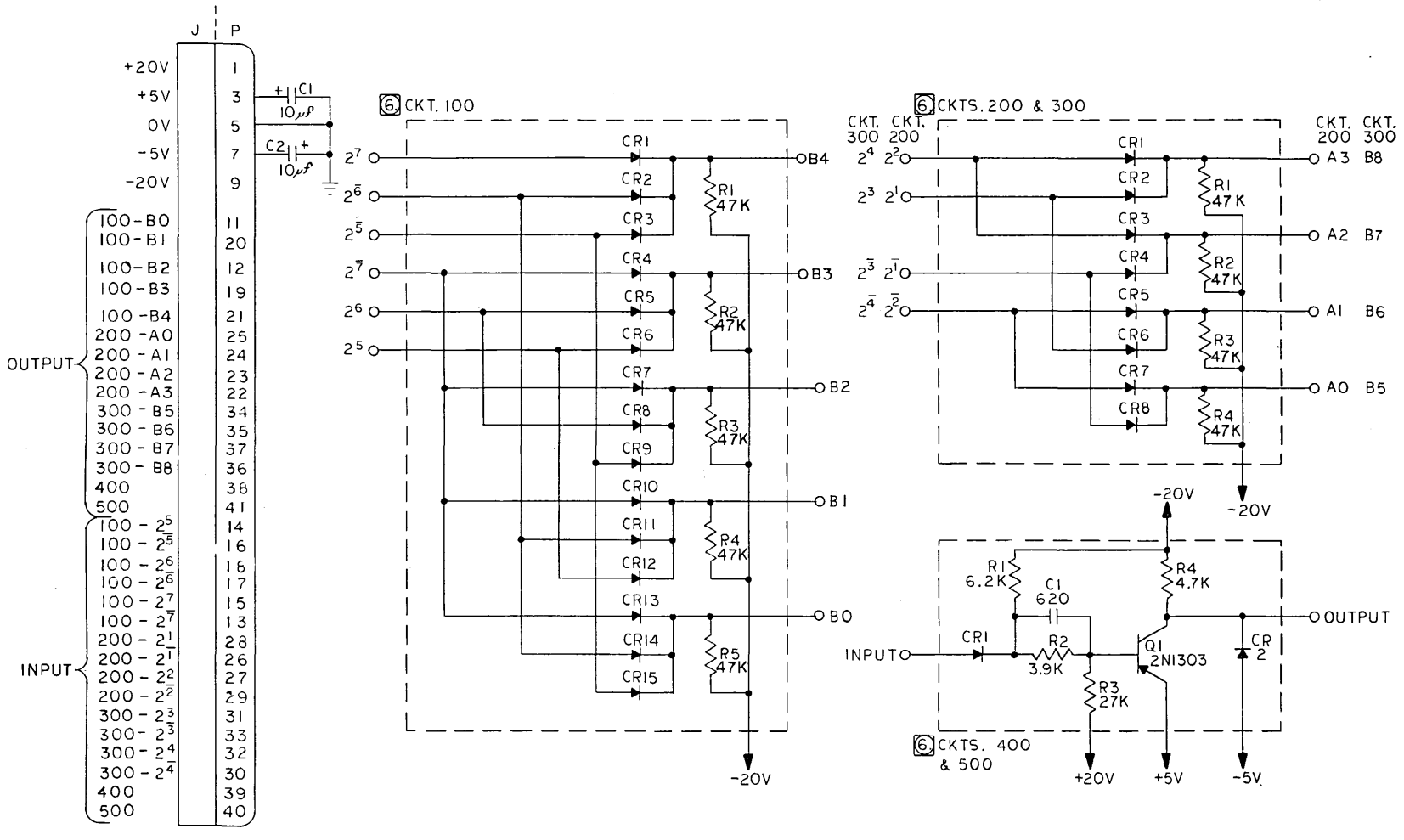
D | DRAWING NUMBER 200227 | REV. B

[3] STAMP BOARD TYPE 8A1, AND CURRENT ASSY. REV. LETTER IN UPPER RIGHT HAND CORNER OF BOARD AS SHOWN, 1/8" HIGH.

[2] STRIPE ON DIODE INDICATES DIRECTION OF CATHODE.

1. SCHEMATIC DRAWING NO. 200224.

NOTE: UNLESS OTHERWISE SPECIFIED.

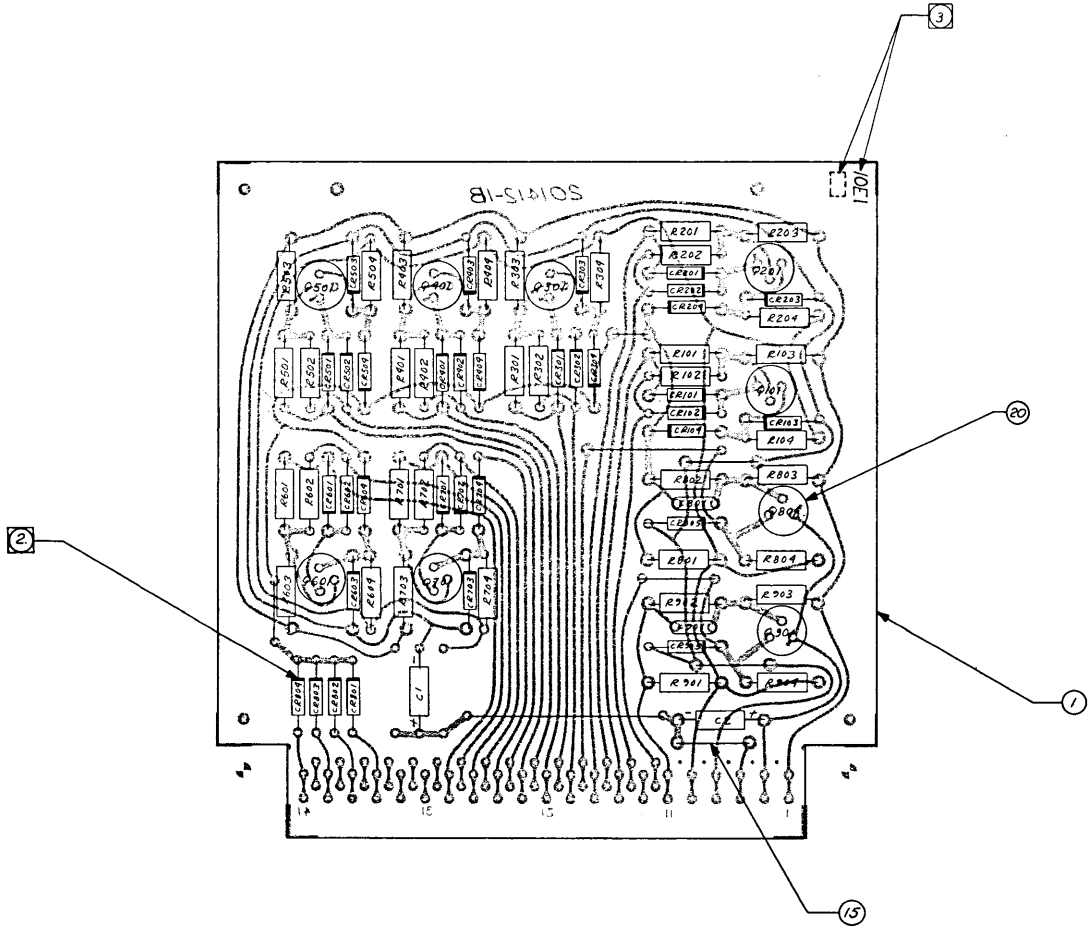


6 REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE PART DESIGNATION WITH THE SUBASSEMBLY DESIGNATION.

5. ASSEMBLY DRAWING NO. 201377.
4. ALL 10μf CAPACITORS ±20% 20V
3. ALL CAPACITOR VALUES IN PF±5% 300V.
2. ALL RESISTOR VALUES IN OHMS ±5% 1/2W
1. ALL DIODES 200505-1

NOTES: UNLESS OTHERWISE SPECIFIED.

dP data products corporation CULVER CITY, CALIFORNIA		
TITLE SCHEMATIC DECODE 8E1		
C	DRAWING NO. 201374	REV B
	SHEET 1 CONT. ON 1	



PART NO. 201413-1

21				
20	9	RL05090-1N	TRANSIPAD (ROBINSON)	
19				
18				

17	9	2N1303	TRANSISTOR	Q1 ALL CKTS.
16				
15	A/R		WIRE (22 GA.)	
14				
13	7	EB3335	RESISTOR 33K ½W ±5% (A.B.)	R3, CKTS. 100 - 700
12	9	EB1235	RESISTOR 12K ½W ±5% (A.B.)	R9, CKTS. 100 - 700, R803, R903
11	14	EB6825	RESISTOR 6.8K ½W ±5% (A.B.)	R1, R2, CKTS. 100 - 700
10	2	EB4325	RESISTOR 4.3K ½W ±5% (A.B.)	R801, R901
9	2	EB2725	RESISTOR 2.7K ½W ±5% (A.B.)	R804, R904
8	2	EB1525	RESISTOR 1.5K ½W ±5% (A.B.)	R802, R902
7				
6	34	200505-1	DIODE	CR101 - CR905
5				
4	2	DM15-621J	CAPACITOR 620pF ±5% 300V (ARCO)	C801, C901
3	2	150D106X9002DB2	CAPACITOR 10μF ±20% 20V (SPRAGUE)	C1, C2
2				
1	1	201412-1	PROCESSED BD. COMP. 10E	
ITEM NO.	RECOM	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

3. STAMP BOARD TYPE 10E1, AND CURRENT ASSY. REV. LETTER IN UPPER RIGHT HAND CORNER OF BOARD AS SHOWN ⅛" HIGH BLACK.
2. STRIPE ON DIODE INDICATES CATHODE
1. SCHEMATIC DWG. NO. 201910.

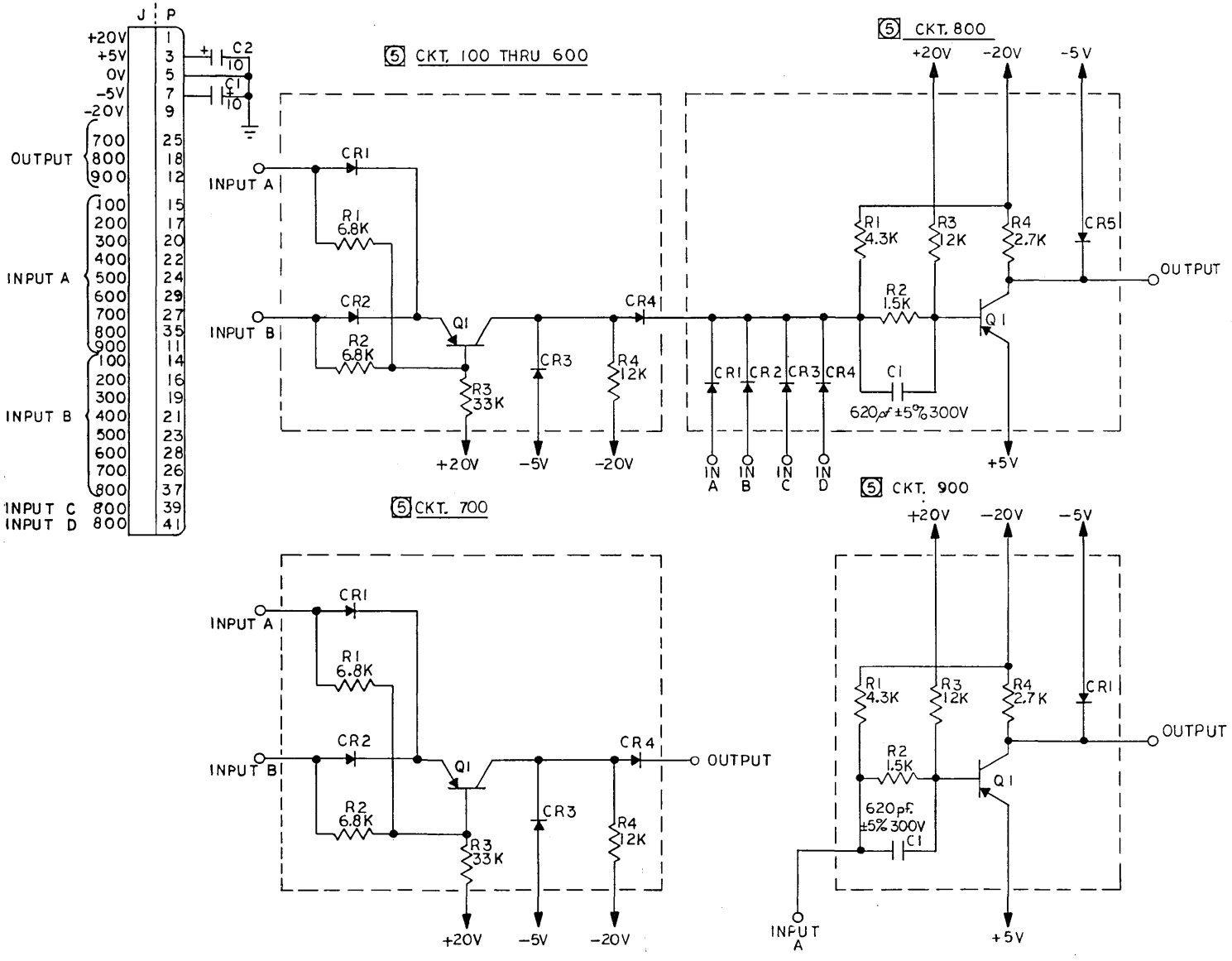
NOTES: UNLESS OTHERWISE SPECIFIED.

data products corporation
CULVER CITY, CALIFORNIA

TITLE ASSEMBLY
COMPARATOR 10E1

D | DRAWING NO. 201413 | REV C

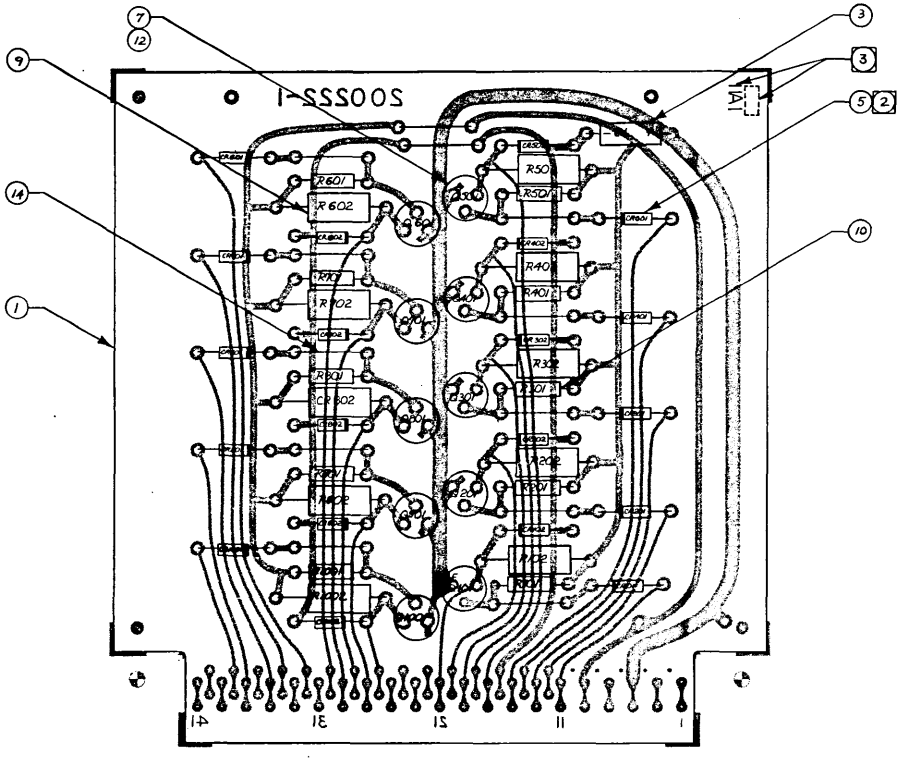
SHEET 1 CONT. ON ——



6. ASSEMBLY DRAWING NO. 201413.
5. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE PART DESIGNATION WITH THE SUBASSEMBLY DESIGNATION.
4. ALL CAPACITOR VALUES IN μf ±20% 20V.
3. ALL DIODES 200505-1.
2. ALL TRANSISTORS 2N1303.
1. ALL RESISTOR VALUES IN OHMS ±5% 1/2W.

NOTES: UNLESS OTHERWISE SPECIFIED.

data products corporation, CULVER CITY, CALIFORNIA	
TITLE: SCHEMATIC COMPARATOR 10E1	
C	DRAWING NO. 201410
SHEET / CONT. ON	REV B



ITEM	PART NO.	REQD	
20			
19			
18			
17			
16			
15			
14		AR	WIRE #22 GA.
13			
12	RC-T05090-IN	10	TRANSIPAD (ROBINSON)
11			
10	E83325	10	RESISTOR 3.2K ±5% ½W (RB) R101-R1001
9	GB1025	10	RESISTOR 1K ±5% 1W (RB) R102-R1002
8			
7	2N1303	10	TRANSISTOR Q101-Q1001
6			
5	CGD1307	20	DIODE CR101-CR1001 , CR102-CR1002
4			
3	ISD1206XC0202	1	CAPACITOR .10 mfd ±20% 20V (Sprague) C1
2			
1	200222-1	1	PROCESSED BOARD OUTPUT DRIVER 11A1

data products corporation
CULVER CITY, CALIFORNIA

TITLE: CIRCUIT BOARD ASSY-
OUTPUT DRIVER 11A1

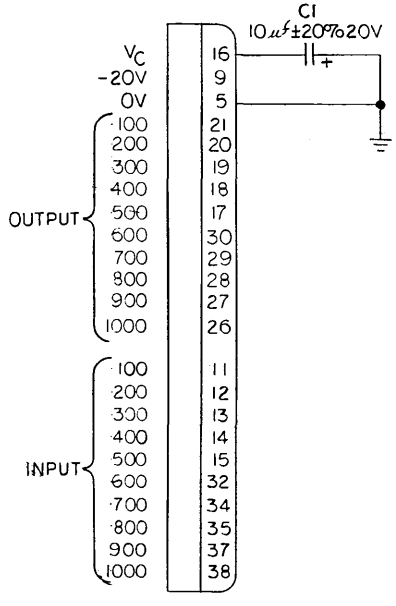
D | DRAWING NUMBER 200223 | REV. B

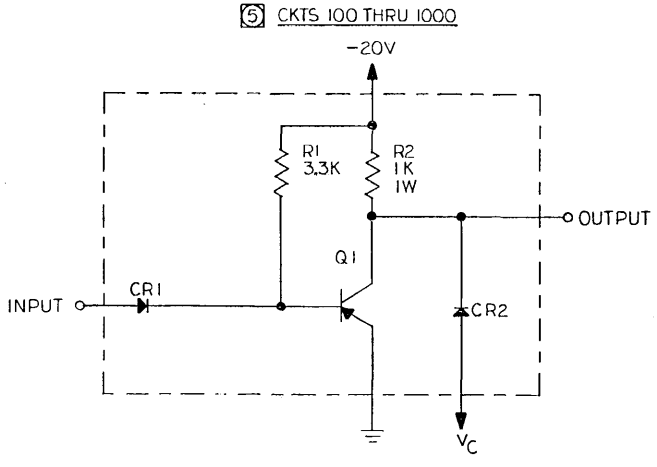
3 STAMP BOARD TYPE 11A1, AND CURRENT ASSY. REV. LETTER IN UPPER RIGHT HAND CORNER OF BOARD AS SHOWN. 1/8" HIGH.

2 STRIP ON DIODE INDICATES DIRECTION OF CATHODE.

1. SCHEMATIC DRAWING NO. 200220

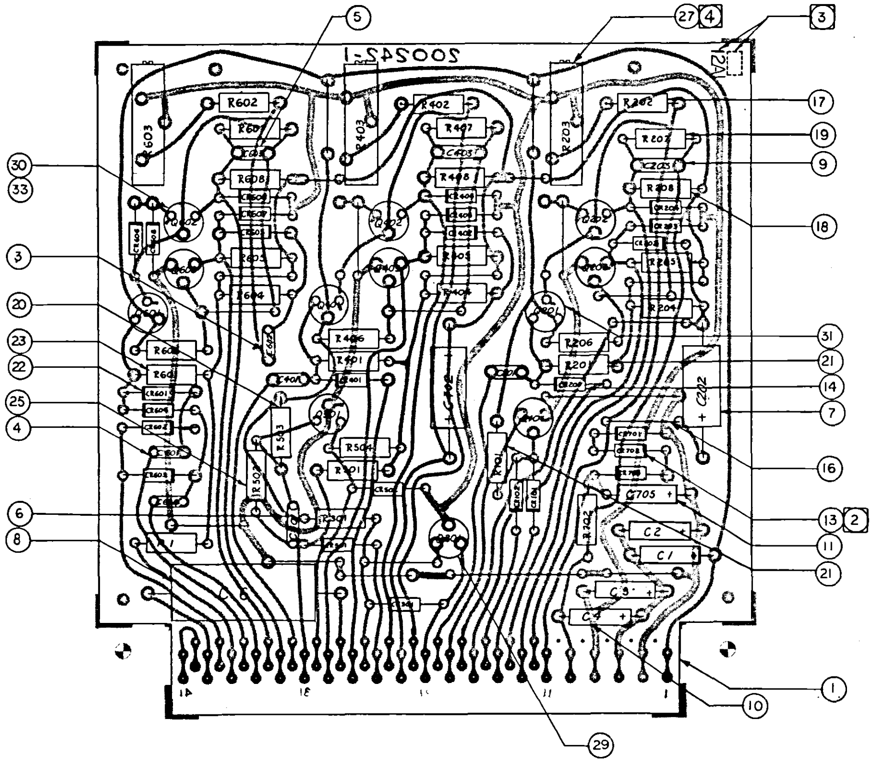
NOTE: UNLESS OTHERWISE SPECIFIED





5 REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE PART DESIGNATION WITH THE SUBASSEMBLY DESIGNATION
4. ASSEMBLY DRAWING NO. 200223
3. ALL TRANSISTORS 2N1303
2. ALL DIODES CGD1307
1. ALL RESISTOR VALUES IN OHMS ± 5% $\frac{1}{2}$ W
NOTE: UNLESS OTHERWISE SPECIFIED

data products corporation CULVER CITY, CALIFORNIA			
TITLE: SCHEMATIC OUTPUT DRIVER I IA1			
	C	DRAWING NUMBER 200220	REV. B



ITEM	REQ'D	PART NO.	DESCRIPTION	REF. DESIGNATION
33	12	RC-TO5090-IN	TRANSIPAD (ROBINSON)	
32				
31	4	2N1302	TRANSISTOR	Q101, Q201, Q401, Q601
30	2	2N1499A	TRANSISTOR (SPRAGUE)	Q602 Q603
29	6	2N1303	TRANSISTOR	Q202, Q203, Q402, Q403, Q301, Q501
28				
27	3	3067P1-502	RESISTOR, VARIABLE 5K (BOURNS)	R203, R403, R603
26				
25	1	EB 8215	RESISTOR 820Ω ±5% 1/2W (AB)	R502
24	2	EB 2735	RESISTOR 27K ±5% 1/2W (AB)	R201, R401
23	3	EB 1835	RESISTOR 18K ±5% 1/2W (AB)	R206, R406, R606
22	2	EB 1035	RESISTOR 10K ±5% 1/2W (AB)	R301, R601
21	1	EB 8225	RESISTOR 82K ±5% 1/2W (AB)	R101
20	1	EB 6825	RESISTOR 6.8K ±5% 1/2W (AB)	R503
19	3	EB 3025	RESISTOR 3K ±5% 1/2W (AB)	R207, R407, R607
18	13	EB 2725	RESISTOR 2.7K ±5% 1/2W (AB)	R204, R205, R208, R404, R405, R408, R501, R504, R604, R605, R608, R702, R1
17	3	EB 1225	RESISTOR 1.2K ±5% 1/2W (AB)	R202, R402, R602
16	A/R		WIRE 22 GA.	
15				
14	22	CGD1307	DIODE	CR101 — CR603
13	3	1N456	DIODE	CR701, CR702, CR703
12				
11	3	150D106X002082	CAPACITOR 10µf ±20% 20V (SPRAGUE)	C2, C3 C705
10	2	150D685X003582	CAPACITOR 6.8µf ±20% 35V (SPRAGUE)	C1, C4
9	2	DM19-2023	CAPACITOR 2000 pf ±5% 500V (ARCO)	C203, C403
8	1	2WFP33	CAPACITOR .33µf ±10% 200V (SPRAGUE)	C6
7	2	2WFP10	CAPACITOR .1µf ±10% 200V (SPRAGUE)	C202, C402
(E) 6	1	DM15-621J	CAPACITOR 620 pf ±5% 300V (ARCO)	C501
5	1	DM15-101J	CAPACITOR 100 pf ±5% 500V (ARCO)	C603
4	2	DM15-151J	CAPACITOR 150 pf ±5% 500V (ARCO)	C601, C604
3	3	DM15-331J	CAPACITOR 330 pf ±5% 500V (ARCO)	C201, C401, C602
2				
1	1	200242-1	PROCESS, BOARD MULTIVIBRATOR 12A2	

4. TRIMPOTS SHALL BE ASSEMBLED ON CARDS AFTER SOLDERING OPERATIONS ARE COMPLETED TO PREVENT FLUX AND CLEANING SOLVENTS ENTERING TRIMPOTS

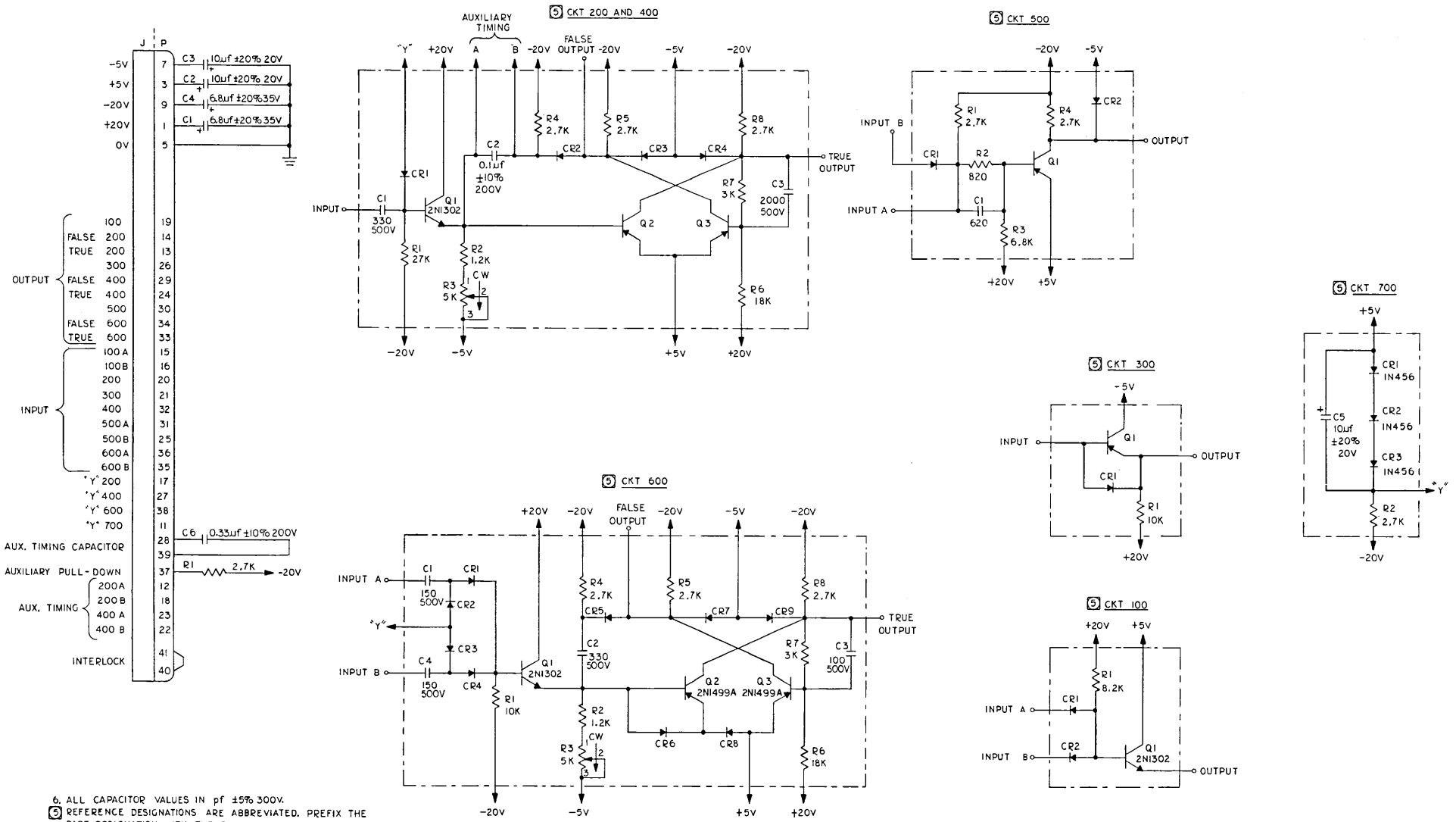
3. STAMP BOARD TYPE 12A2, AND CURRENT ASSY. REV. LETTER IN UPPER RIGHT HAND CORNER OF BOARD AS SHOWN, 1/8" HIGH

2. STRIPE ON DIODE INDICATES DIRECTION OF CATHODE

1. SCHEMATIC DWG. NO. 200240

NOTE: UNLESS OTHERWISE SPECIFIED

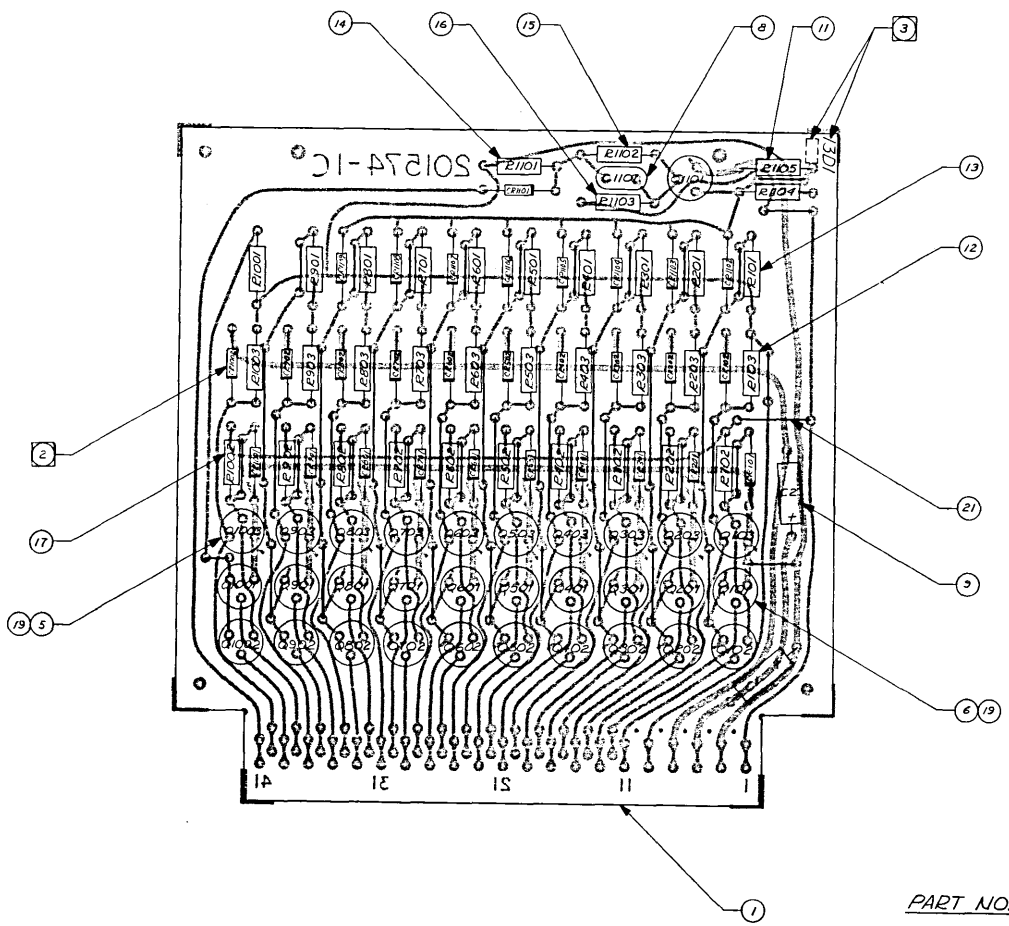
data products corporation
CULVER CITY, CALIFORNIA
TITLE: CIRCUIT BOARD ASSY- MULTIVIBRATOR 12A2
CAT. D | DRAWING NUMBER 200243 | REV. E



6. ALL CAPACITOR VALUES IN pf ±5% 300V.
5 REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE PART DESIGNATION WITH THE SUBASSEMBLY DESIGNATION.
4. ASSEMBLY DRAWING NO. 200243
3. ALL DIODES CGD 1307
2. ALL TRANSISTORS 2N1303
1. ALL RESISTOR VALUES IN OHMS ±5% $\frac{1}{2}$W

NOTE: UNLESS OTHERWISE SPECIFIED

dp data products corporation, CULVER CITY, CALIFORNIA	
TITLE	SCHEMATIC MULTIVIBRATOR 12A2
D	DRAWING NO. 200240 — REV D
	SHEET — CONT. ON



PART NO. 201575-1

22				
21	A/R		WIRE (22GA.)	
20				
19	31	RC-05090-JN	TRANSIPAD (ROBINSON)	
18				

17	10	EB8225	RESISTOR 8.2K 1/2W ±5% (A.B.)	R102 - R1002
16	1	EB1535	15K	R1103
15	1	EB1825	1.8K	R1102
14	1	EB3325	3.3K	R1101
13	11	EB3925	3.9K	R101 - R1001, R1104
12	10	EB4725	4.7K	R103 - R1003
11	1	EB5625	RESISTOR 5.6K 1/2W ±5% (A.B.)	R1105
10				
9	2	150D106X002082	CAPACITOR-10μf ±20% 20V (SPRAGUE)	C1, C2
8	1	DM15-621J	CAPACITOR-620pf ±5% 300V (APCO)	C1101
7				
6	20	2N1302	TRANSISTOR	Q101 - Q1002
5	11	2N1303	TRANSISTOR	Q103 - Q1003, Q1101
4				
3	29	200505-1	DIODE	CR101 - CR1109
2				
1	1	201574-1	PROCESSED BD.-LOGIC REC.	13D
ITEM NO.	NUMBER	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

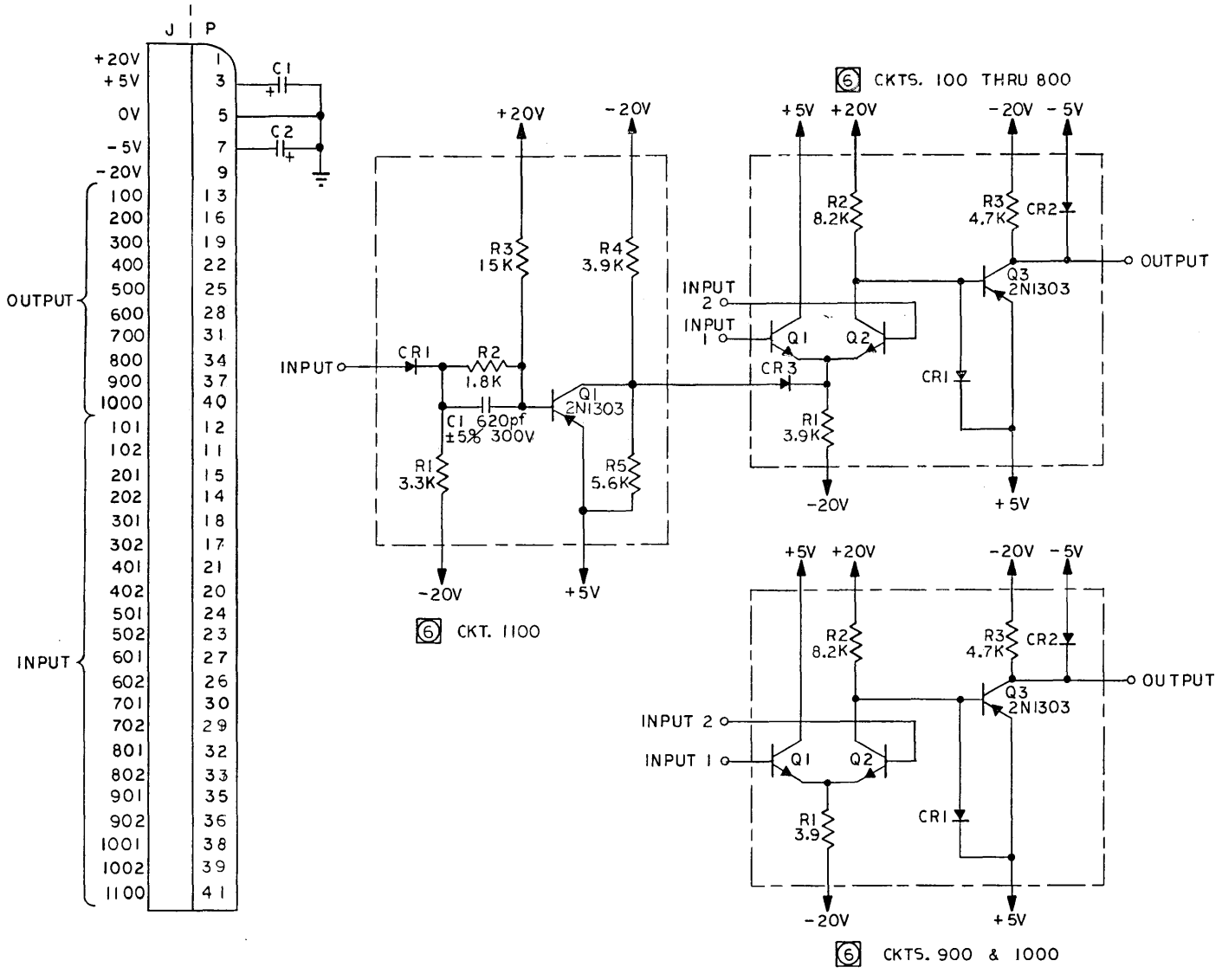
(3) STAMP BOARD TYPE 13D1, AND CURRENT ASSY. REV. LETTER IN UPPER RIGHT HAND CORNER OF BOARD AS SHOWN, 1/8" HIGH BLACK.
(2) STRIPE ON DIODE INDICATES CATHODE. →|
1. SCHEMATIC DWG. NO. 201572

NOTES: UNLESS OTHERWISE SPECIFIED.

data products corporation
CULVER CITY, CALIFORNIA

TITLE: CKT. BD. ASSEMBLY
LOGIC REC. 13D1

D | DRAWING NO. 201575 | REV B
SHEET 1 CONT. ON —

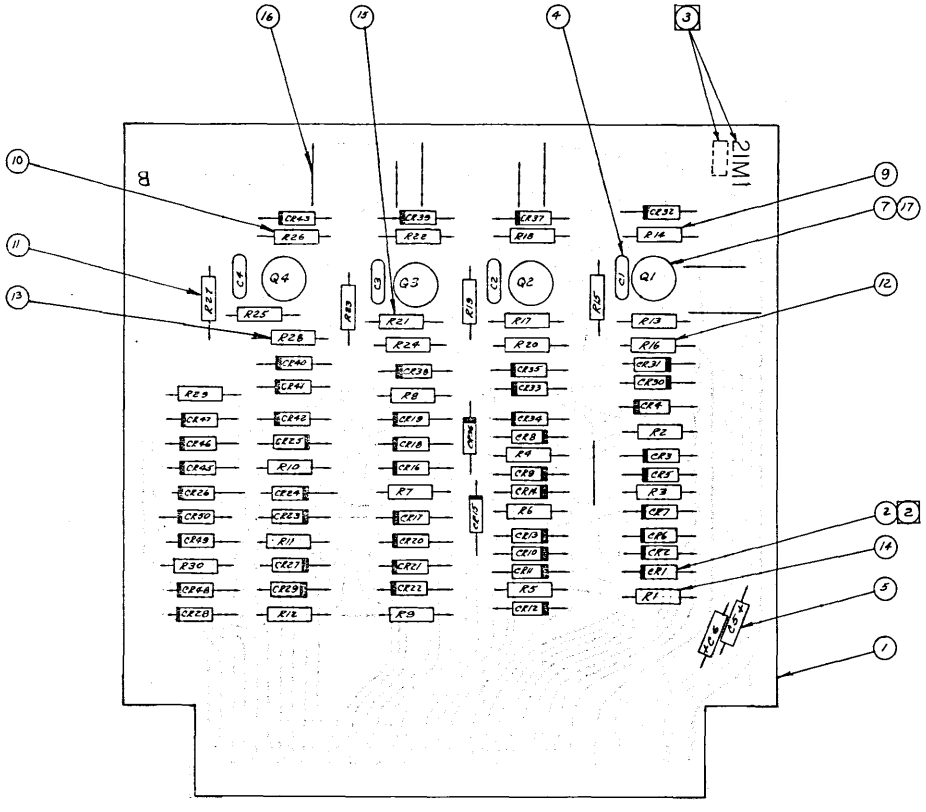


6 REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE PART DESIGNATION WITH THE SUBASSEMBLY DESIGNATION.

5. ASSEMBLY DRAWING NO. 201575.
4. ALL CAPACITORS 10μf ±20%, 20V.
3. ALL TRANSISTORS 2N1302.
2. ALL RESISTOR VALUES IN OHMS, ±5%, 1/2W.
1. ALL DIODES 200505-1.

NOTES: UNLESS OTHERWISE SPECIFIED.

data products corporation, CULVER CITY, CALIFORNIA	
TITLE	SCHEMATIC LOGIC RECEIVER 13D1
C	DRAWING NO. 201572 — REV C
	SHEET 1 CONT. ON ~



PART NO. 201408-1

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION
17	4	RC05D90-1N	TRANSIPAD (ROBINSON)	
16	1/2		WIRE - 22 AWG	
15	2	EB3935	RESISTOR - 39K ¼W ±5% (AB)	R21 & R25
14	16	EB2735	RESISTOR-27K ¼W ±5% (AB)	R1-R13, R17, R29, R30
13	2	EB1035	RESISTOR-10K ¼W ±5% (AB)	R24 & R28
12	2	EB7525	RESISTOR- 7.5K ¼W ±5% (AB)	R16 & R20
11	2	EB6225	RESISTOR - 6.2K ¼W ±5% (AB)	R23 & R27
10	4	EB4725	RESISTOR - 47K ¼W ±5% (AB)	R15, R19, R22, R26
9	2	EB2725	RESISTOR-2.7 ½W ±5% (AB)	R14, R18
8				
7	4	2N1303	TRANSISTOR	Q1 - Q4
6				
5	2	150D6X1002DB2	CAPACITOR - 10 µF ±20% 20V (APCO)	C5, C6
4	4	DM15-620J	CAPACITOR-620 µµF ±5% 300V	(SPRAGUE) C1, C2, C3, C4
3				
2	50	200505-1	DIODE	CR1 - CR50
1	1	201407-1	PROCESS BOARD LOGIC DRIVER 2IM	

3 STAMP BOARD TYPE 2IM1 AND CURRENT ASSY REV LETTER IN UPPER RIGHT CORNER AS SHOWN 1/8" HIGH, BLACK.

2 STRIPE ON DIODE INDICATES CATHODE. -|▶|-

1. SCHEMATIC DRAWING NO. 201405.

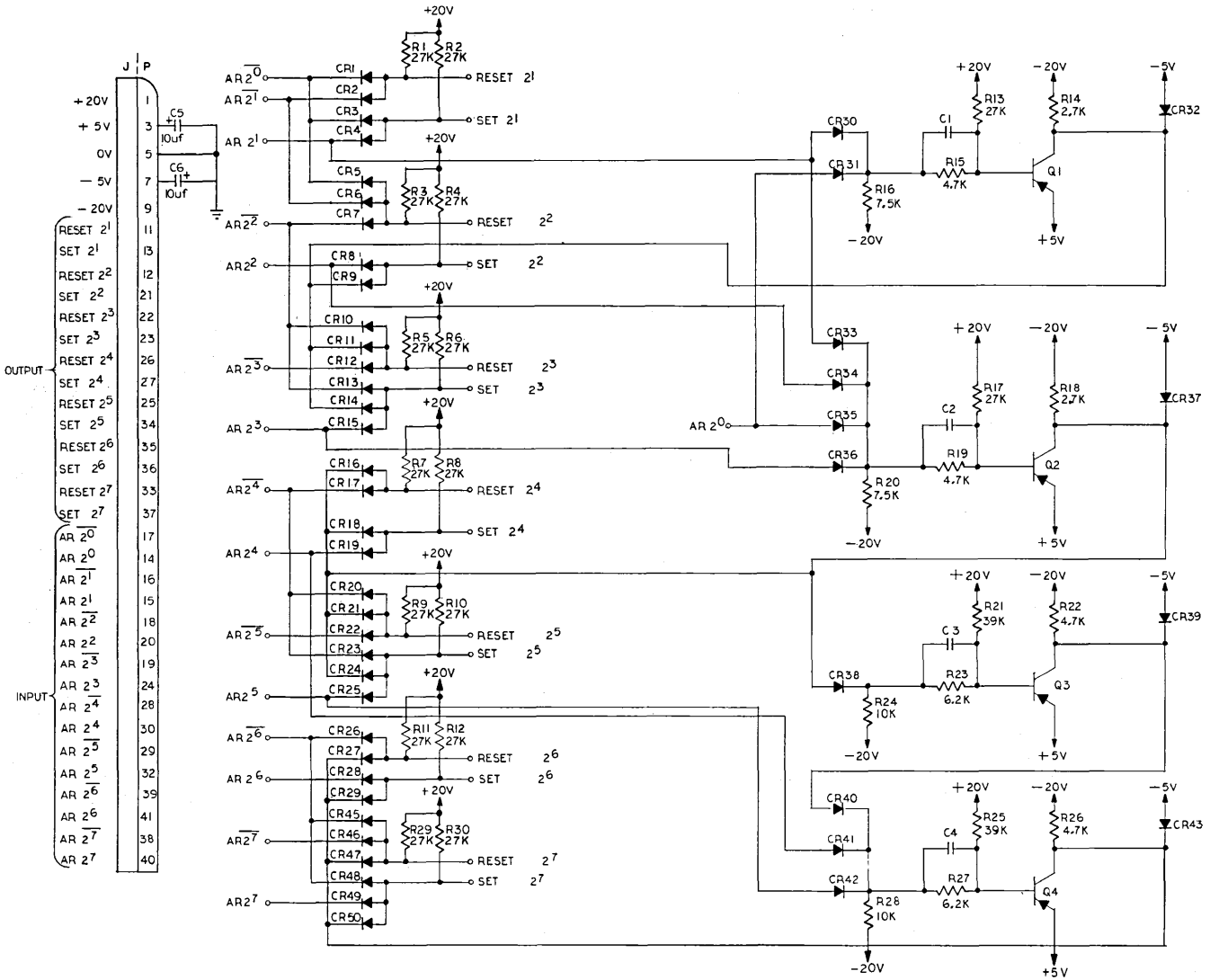
NOTES: UNLESS OTHERWISE SPECIFIED.

data products corporation
CULVER CITY, CALIFORNIA

TITLE
ASSEMBLY—
LOGIC DRIVER 2IM1

D | DRAWING NO. 201408 | REV C

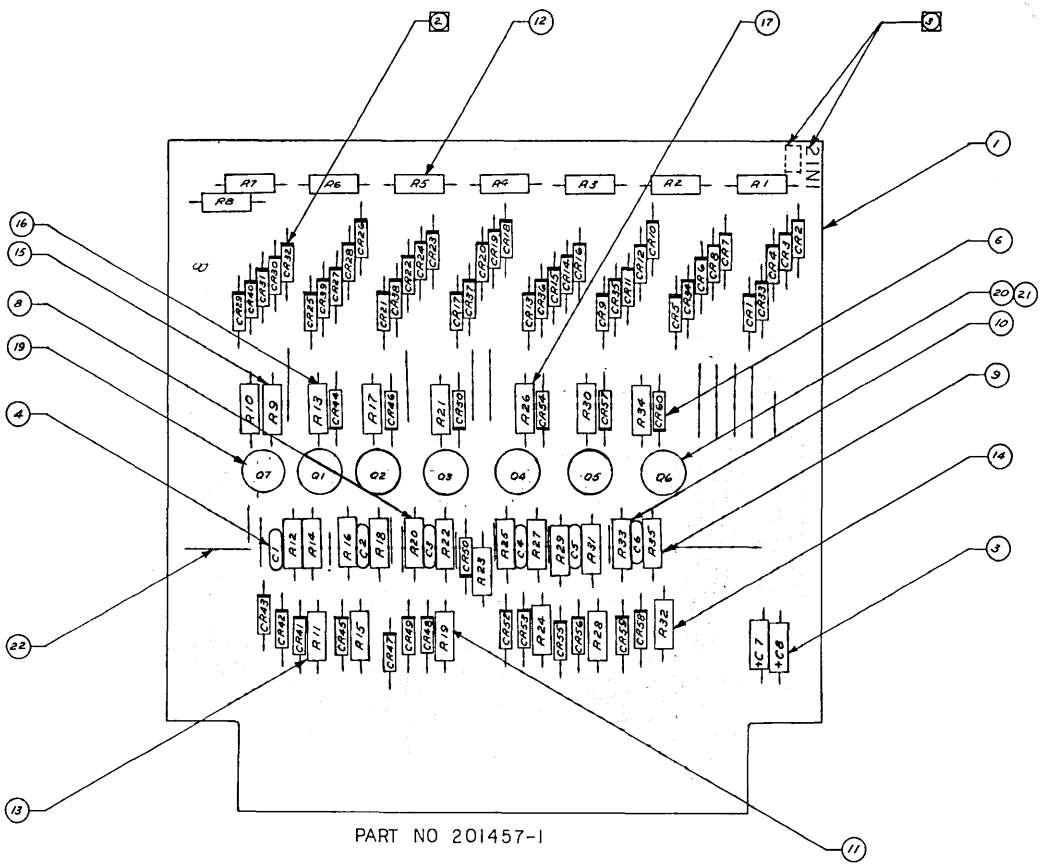
SHEET 1 CONT. ON ~



6. ASSEMBLY DRAWING NO. 201408.
5. ALL 10μf CAPACITORS, ±20%, 20V
4. ALL CAPACITORS 620pf, ±5%, 300V.
3. ALL RESISTOR VALUES IN OHMS ±5%, 1/2 W.
2. ALL DIODES 200505-1.
1. ALL TRANSISTORS 2N1303.

NOTES: UNLESS OTHERWISE SPECIFIED.

data products corporation, CULVER CITY, CALIFORNIA	
TITLE	SCHEMATIC LOGIC DRIVER 21MI
D	DRAWING NO. 201405 — REV B
SHEET	CONT. ON



PART NO 201457-1

22	A/R		WIRE (22 GA)		
21	7	RC05090-IN	TRANSIPAD (ROBINSON)	ALL	
20	6	2N1303	TRANSISTOR	Q1 - Q6	
19	1	2N1302	TRANSISTOR	Q7	
18					
17	3	EB3335	RESISTOR 33K ½ W ±5% (A.B.)	R26, R30, R34	
16	3	EB2735	RESISTOR 27K ½ W ±5% (AB)	R13, R17, R21	
15	1	EB1535	RESISTOR 15K ½ W ±5% (AB)	R9	
14	3	EB8225	RESISTOR 8.2K ½ W ±5% (AB)	R24, R28, R32	
13	2	EB7525	RESISTOR 7.5K ½ W ±5% (A.B.)	R11, R15	
12	10	EB6825	RESISTOR 6.8K ½ W ±5% (A.B.)	R1 - R8, R10, R23	
11	1	EB6225	RESISTOR 6.2K ½ W ±5% (A.B.)	R19	
10	3	EB5625	RESISTOR 5.6K ½ W ±5% (AB)	R25, R29, R33	
9	8	EB4725	RESISTOR 4.7K ½ W ±5% (A.B.)	R12, R14, R16, R18, R22, R27, R31, R35	
8	1	EB3925	RESISTOR 3.9K ½ W ±5% (AB)	R20	
7					
6	60	200505	DIODE	CR1 - CR60	
5					
4	6	DM15-621J	CAPACITOR 620 pf ±5% 300V	C1 - C6 (ARCO)	
3	2	150D106X0020B2	CAPACITOR 10 µf ±20% 20V	C7, C8 (SPRAGUE)	
2					
1	1	201456-1	PROCESSED BOARD LOGIC DRIVER 2IN		
ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION	

data products corporation
CULVER CITY, CALIFORNIA

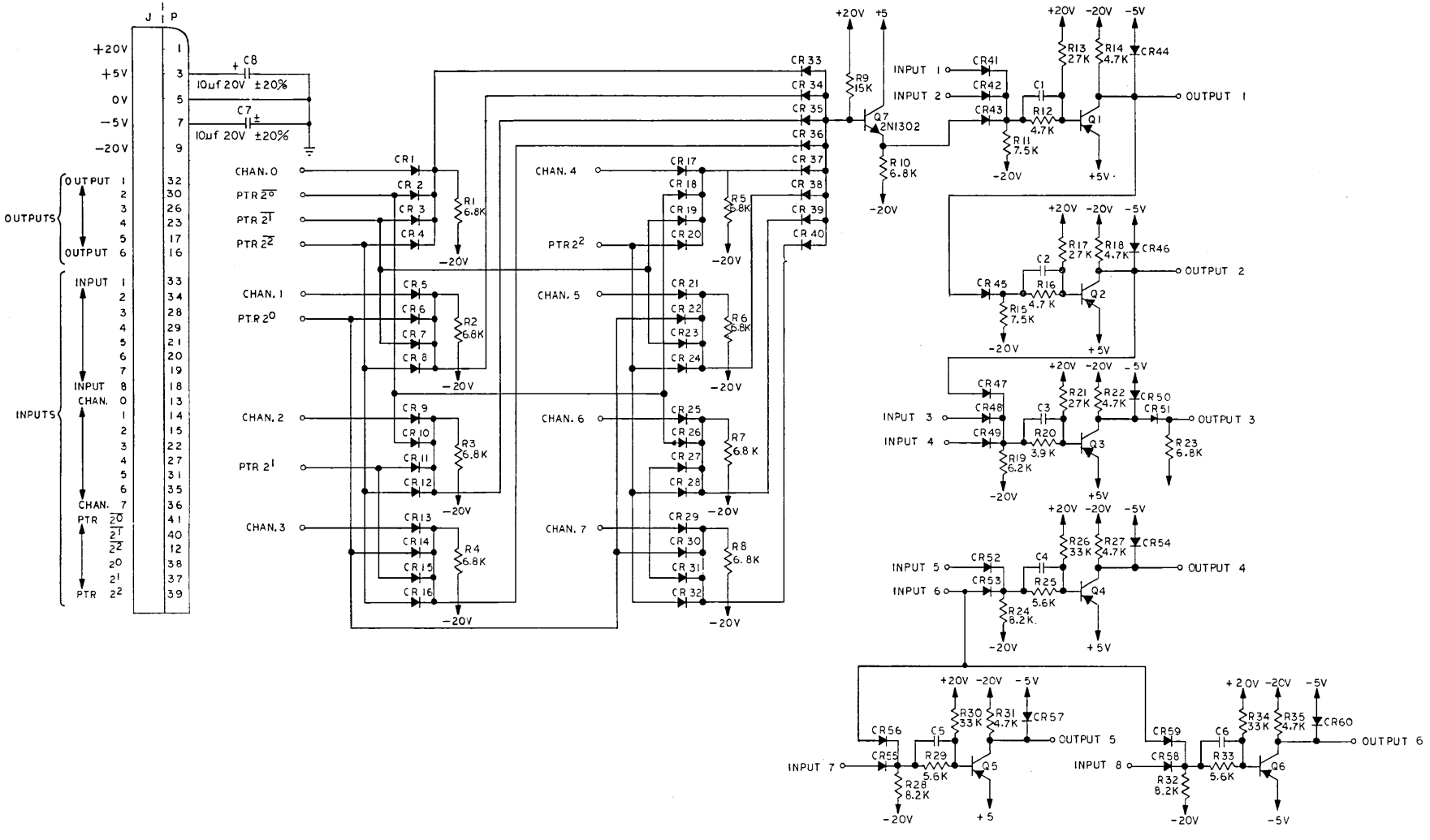
TITLE ASSEMBLY
LOGIC DRIVER 2IN1

D | DRAWING NO. 201457 | REV C

SHEET 1 CONT. ON —

1. STAMP BOARD TYPE 2IN1 AND CURRENT ASSEMBLY REV. LETTER 1/8" HIGH BLACK, IN UPPER RIGHT CORNER.
2. STRIPE ON DIODE INDICATES THE CATHODE.
3. SCHEMATIC DRAWING NO. 201454.

NOTES: UNLESS OTHERWISE SPECIFIED.



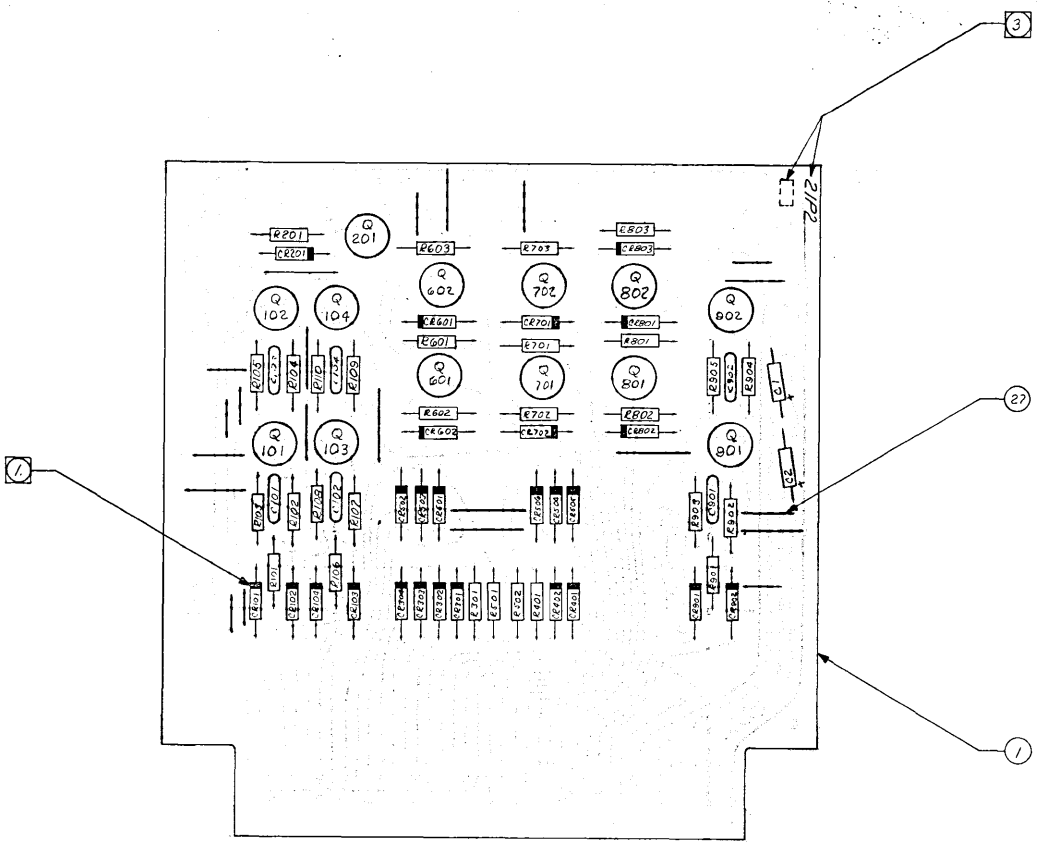
5. ASSEMBLY DRAWING NO. 201457.
4. ALL CAPACITORS 620pf ±5% 300V.
3. ALL RESISTOR VALUES IN OHMS, ±5%, 1/2W.
2. ALL DIODES 200505-1.
1. ALL TRANSISTORS 2N1303.

NOTES: UNLESS OTHERWISE SPECIFIED.

data products corporation
CULVER CITY, CALIFORNIA

TITLE: SCHEMATIC
LOGIC DRIVER 21N1

DRAWING NO. 201454
SIZE D
REV C
SHEET | CONT. ON ~



PART NO. 201481-1

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION
27	A/R		22 GAGE WIRE	
26				
25	13	RC05090-1N	TRANSIPAD (ROBINSON)	
24				
23	3	EB1235	RESISTOR 12K ±5% ½W (13)	R103, 108, 903
22				
21	3	EB6825	6.8K	R301, 501, 502
20	3	EB5125	5.1K	R101, 106, 901
19	1	EB4725	4.7K	R803
18	7	EB2725	2.7K	R102, 107, 601, 701, 801, 902, 401
17	4	EB1825	1.8K	R602, 702, 802, 201
16	3	EB6815	680Ω	R104, 109, 904
15	3	EB2215	220Ω	R105, 110, 905
14	2	EB2705	27Ω	R603, 703
13				
12				
11	4	2N1303	TRANSISTOR	Q101, 103, 802, 901
10	3	2N1302		Q601, 701, 801
9	3	2N1169		Q102, 104, 902
8	3	2N1924	TRANSISTOR	Q201, 602, 702
7				
6	26	200505-1	DIODE	CR101 – 902
5	3	DM15 102J	CAPACITOR 1000pF ±5% 100V (ARCO)	C103, 104, 902
4	2	150D106X0020B2	CAPACITOR 10μF ±20% 20V (SPRAGUE)	C152
3	3	DM15-621J	CAPACITOR 620pF ±5% 300V (ARCO)	C101, 102, 901
2				
1	1	201480-1	PROCESSED BOARD LOGIC DRIVER 21P	

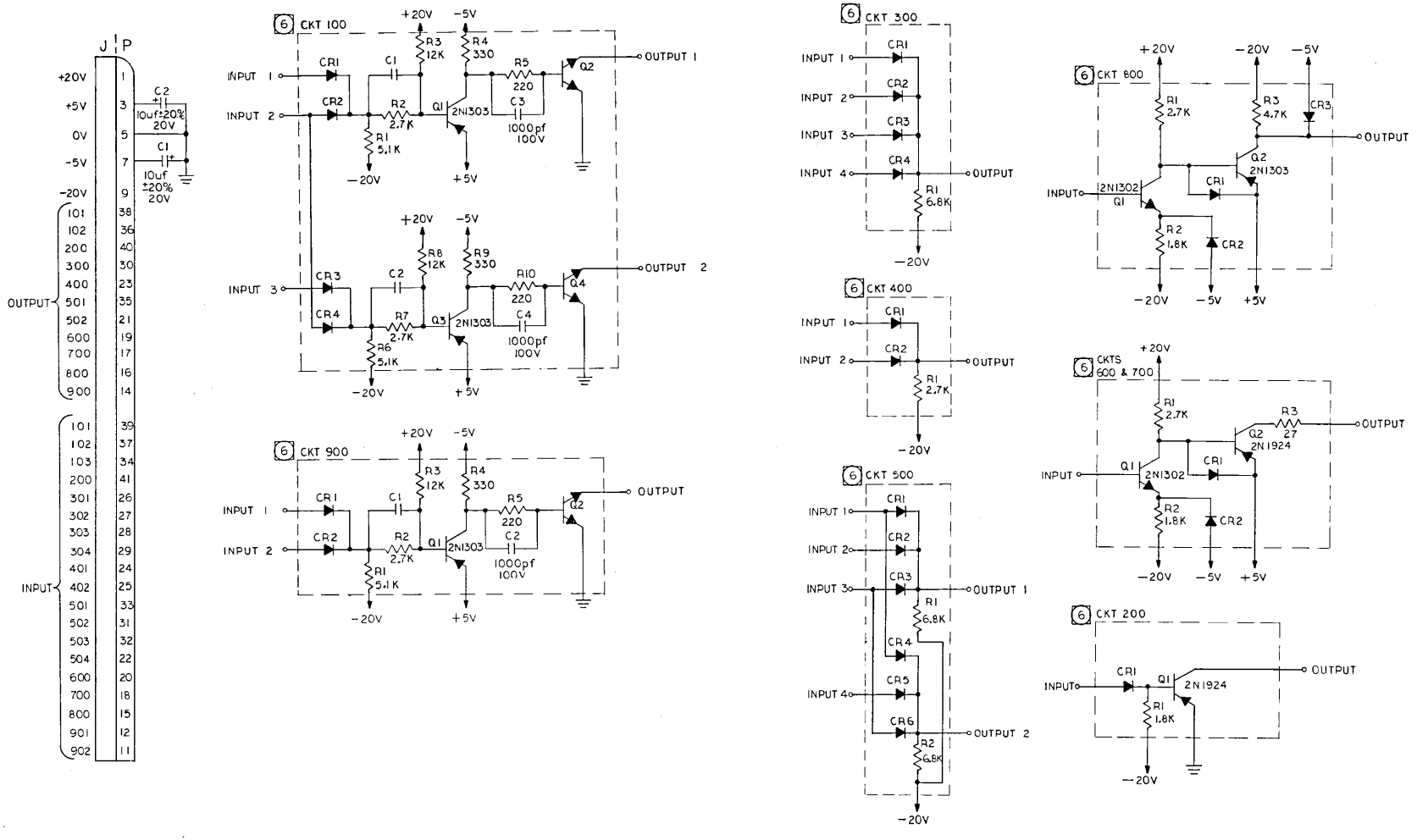
data products corporation
CULVER CITY, CALIFORNIA

TITLE: CRT. BOARD ASSY. LOGIC DRIVER 21P2

DRAWING SIZE: D | DRAWING NO.: 201481 | REV: G | SHEET 1 | CONT. ON

3. STAMP BOARD TYPE 21P1, AND CURRENT ASSY. REV. LETTER IN UPPER RIGHT HAND CORNER OF BOARD AS SHOWN 1/8" HIGH BLACK.
2. SCHEMATIC DRAWING NO. 201478.
1. STRIPE ON DIODE INDICATES CATHODE

NOTES: UNLESS OTHERWISE SPECIFIED.



6 REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE PART DESIGNATION WITH THE SUBASSEMBLY DESIGNATION.

5. ASSEMBLY DWG. NO. 201481.
4. ALL CAPACITORS 620pf ±5%, 300V.
3. ALL RESISTOR VALUES IN OHMS, ±5%, 1/2W.
2. ALL DIODES 200505-1.
1. ALL TRANSISTORS 2N1169.

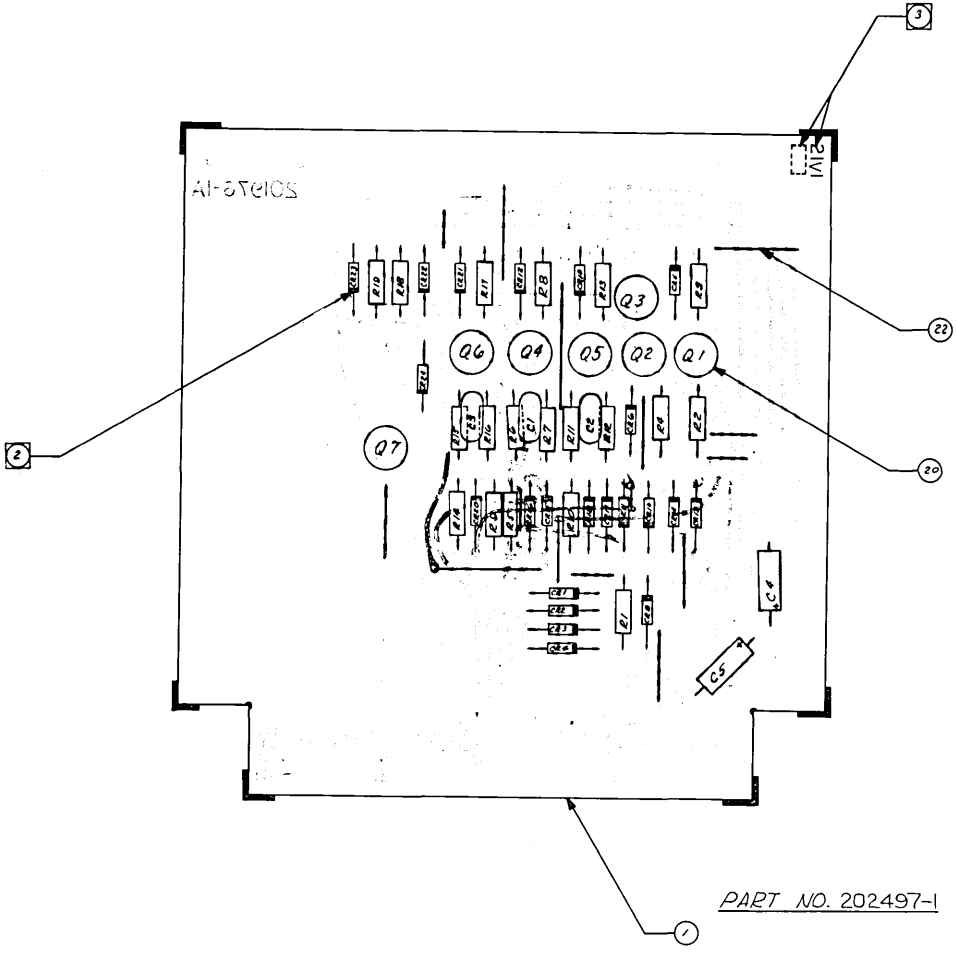
NOTES: UNLESS OTHERWISE SPECIFIED.

data products corporation
CULVER CITY, CALIFORNIA

TITLE: SCHEMATIC — LOGIC DRIVER 21P2

D | DRAWING NO. 201478 | REV G | SHEET 1 | CONT. ON ~

REVISIONS						
ZONE	REV	ECO NO.	DESCRIPTION	CHK'R	APP	DATE
	A		PRODUCTION RELEASE			
	B	402	SEE ECO 402			



PART NO. 202497-1

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	REFERENCE DESIG	VENDOR PART NO.
			LIST OF MATERIAL		
22	A/R		22 GAGE WIRE		
21					
20	7		TRANSIPAD (ROBINSON)		RC05080-IN
19					
18	1		RESISTOR - 18K ½W ±5% (A.B.)	R19	EB1835
17	3		RESISTOR - 27K ½W ±5% (A.B.)	R7, R12, R16	EB2735
16	3		RESISTOR - 6.2K ½W ±5% (A.B.)	R5, R10, R14	EB6225
15	4		4.7K	R4, R8, R13, R17	EB4725
14	1		8.2K	R3	EB8225
13	4		3.9K	R2, R6, R11, R15	EB3925
12	3		RESISTOR - 6.8K ½W ±5% (A.B.)	R1, R9, R18	EB6825
11					
10	1		TRANSISTOR	Q7	2N1024
9	4		TRANSISTOR	Q3, Q4, Q5, Q6	2N1303
8	2		TRANSISTOR	Q1, Q2	2N1302
7					
6	22	200505-1	DIODE	CR1 THRU CR24	
5					
4	2		CAPACITOR-10 mF ±20% 20V (SPRAGUE)	C4, C5	150D106F0020B2
3	3		CAPACITOR-620PF ±5% 300V (ELMENCO)	C1, C2, C3	DM15-621J
2					
1	1	201976-1	PROCESSED BOARD, LOGIC DRIVER 21VI		

D DRAWING NO. 202497 REV B

3. MARK BOARD TYPE NO. AND CURRENT ASSY. REVISION LETTER IN UPPER RIGHT CORNER OF BOARD AS SHOWN 1/8 HIGH, COLOR, BLACK.
2. STRIPE ON DIODE INDICATES CATHODE
1. FOR CIRCUIT SEE SCHEMATIC DWG NO. 202496

NOTES: UNLESS OTHERWISE SPECIFIED.

SUPPLEMENTARY INFORMATION		NAME	DATE
FIRST USED ON 6400 S/N 4633/0	DES		
NEXT ASSEMBLY 201939	DRFT	Thomson	5/14/63
	CHKR		
	APP	Youngquist	5/14/63
	APP		

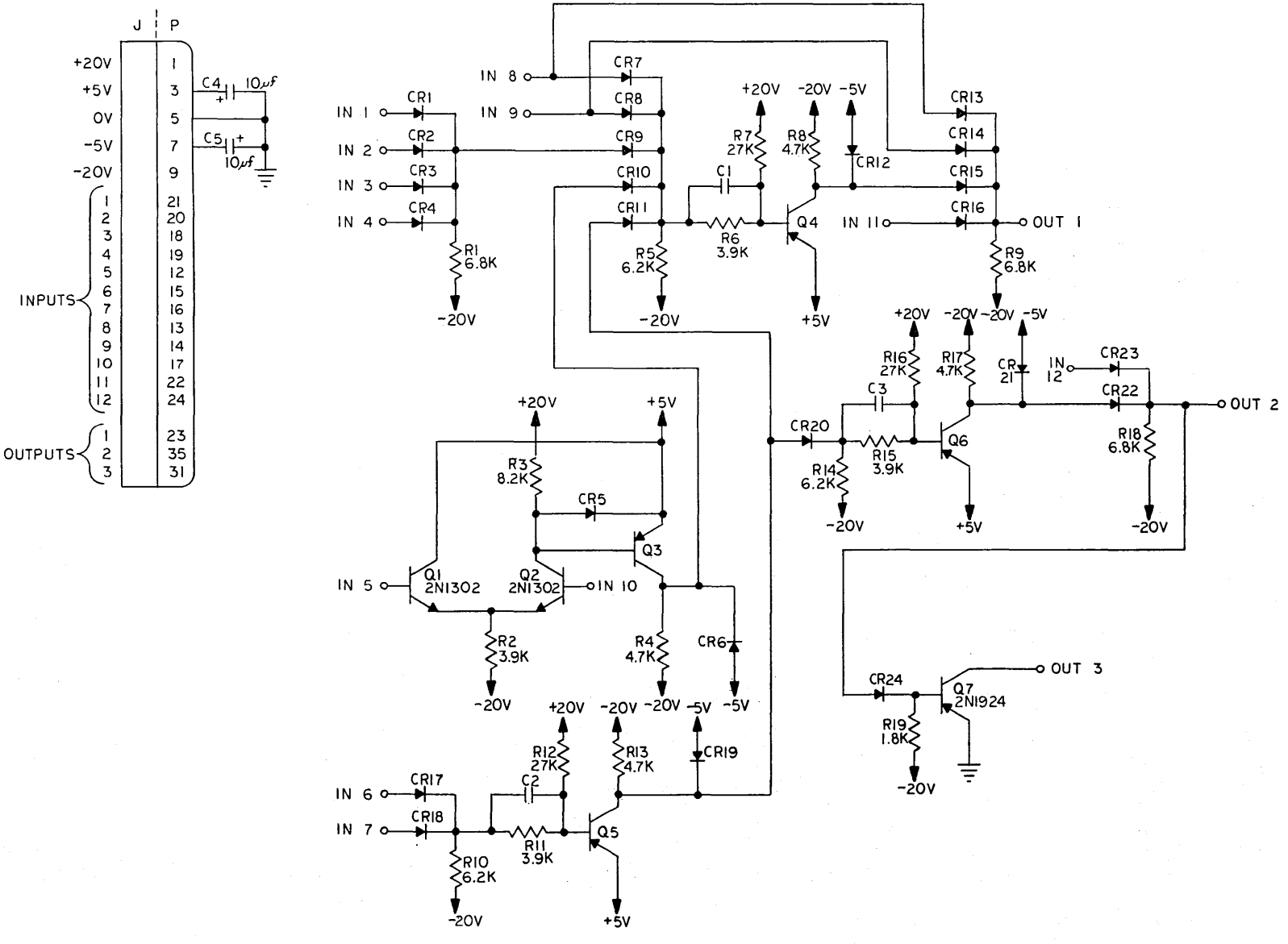
MATERIAL
FINISH
DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

SCALE 2 X 1
DO NOT SCALE DWG.
ALL DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL ±
FRACTION ±
ANGLE ±

data products corporation
CULVER CITY, CALIFORNIA

TITLE CIRCUIT BOARD ASSY. LOGIC DRIVER 21VI

D DRAWING NO. 202497 REV B
SHEET 1 CONT. ON



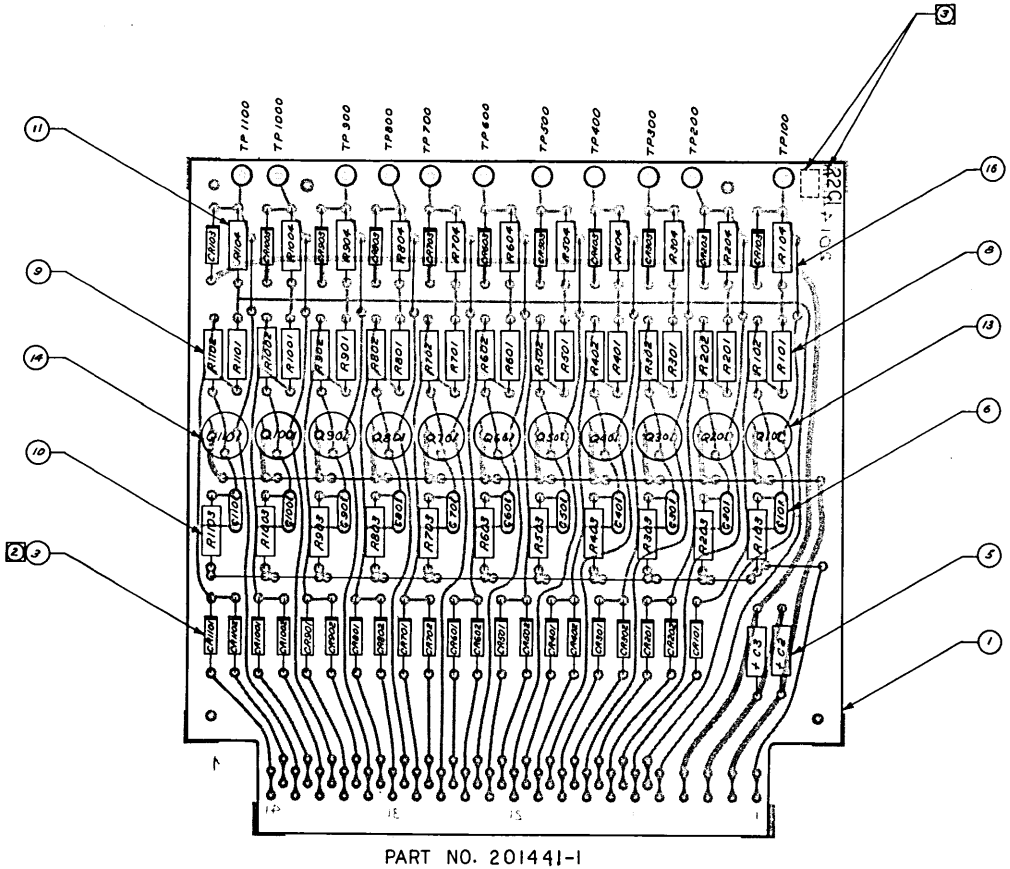
6. ASSEMBLY DRAWING NO. 201977
5. ALL 10μf CAPACITORS ±20% 20V
4. ALL CAPACITORS 620Pf ±5% 300V
3. ALL RESISTOR VALUES IN OHMS ±5% 1/2W
2. ALL DIODES 200505-1
1. ALL TRANSISTORS 2N1303

NOTES: UNLESS OTHERWISE SPECIFIED.

data products corporation
CULVER CITY, CALIFORNIA

TITLE SCHEMATIC
LOGIC DRIVER 2101

C | DRAWING NO. 201974 | REV B
SHEET 1 CONT. ON ——



PART NO. 201441-1

SEE NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION
17				
16	A/R		WIRE 22GA.	
15				
14	11	RC05090-1N	TRANSIPAD (ROBINSON)	
13	11	2N1303	TRANSISTOR	Q101-Q1101
12				
11	11	EB4725	RESISTOR 4.7K ±5% ½W (A.B.)	R104-R1104
10	11	EB2735	RESISTOR 27K ±5% ½W (A.B.)	R103-R1103
9	11	EB3925	RESISTOR 3.9K ±5% ½W (A.B.)	R102-R1102
8	11	EB6225	RESISTOR 6.2K ±5% ½W (A.B.)	R101-R1101
7				
6	11	DM15-621J	CAPACITOR 620pf ±5% 300V(ARCO)	C101-C1101
5	2	1500106X0020B2	CAPACITOR 10uf ±20% 20V	C2, C3
4				
3	32	200505-1	DIODE	
2				
1	1	201440-1	PROCESSED BOARD NAN GATE 22C	

data products corporation
CULVER CITY, CALIFORNIA

TITLE: ASSEMBLY
NAN GATE 22CI

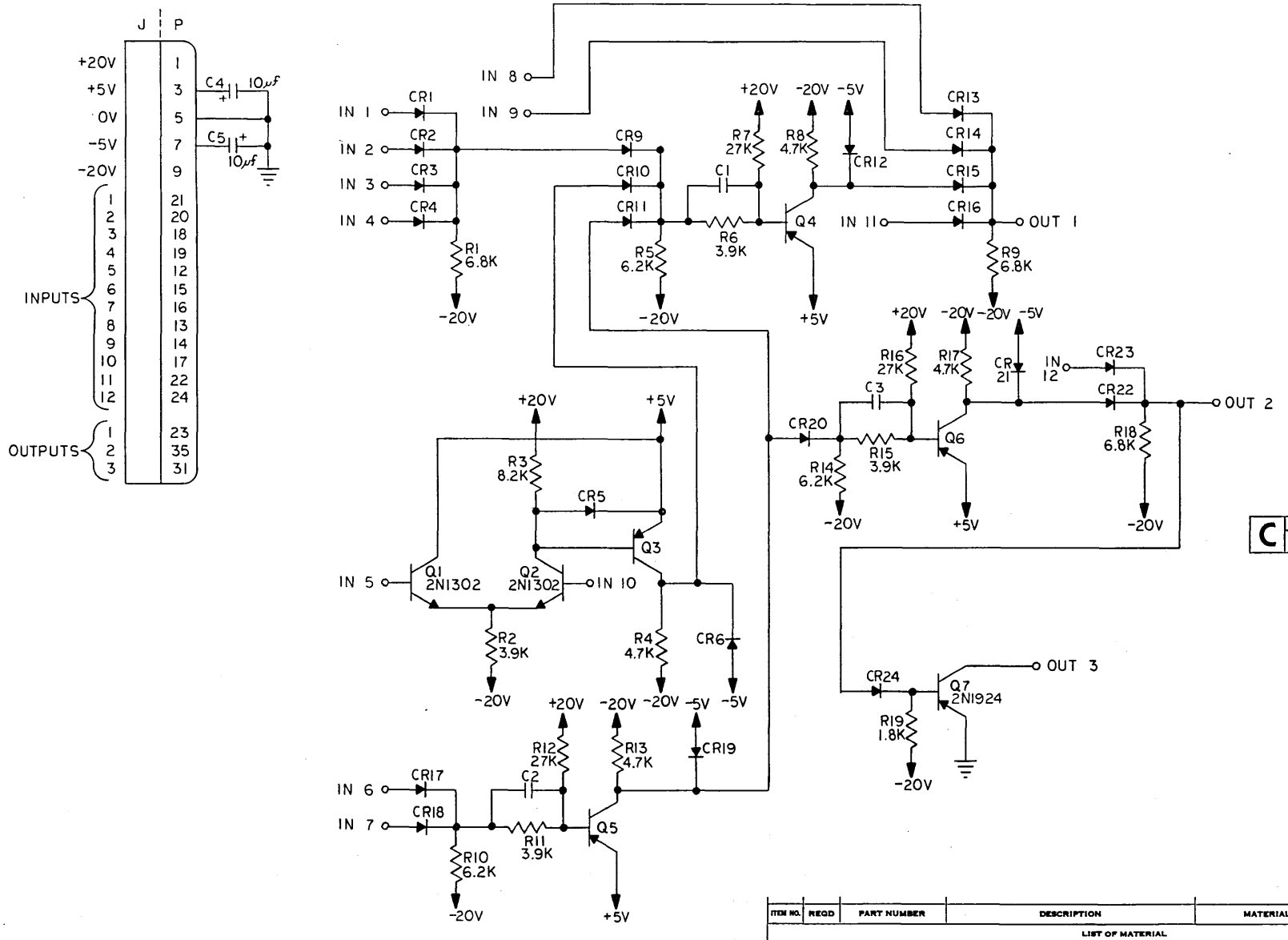
D | DRAWING NO. 201441 | REV D

SHEET 1 | CONT. ON —

⑤ STAMP BOARD TYPE 22CI AND CURRENT ASS'Y. REV. LETTER 1/8" HIGH BLACK IN UPPER RIGHT CORNER.
② STRIPE ON DIODE INDICATES CATHODE. ⊣▮⊢

NOTES: UNLESS OTHERWISE SPECIFIED.
1. SCHEMATIC DRAWING NO. 201438.

REVISIONS						
ZONE	REV	ECO NO.	DESCRIPTION	CHKR	APP	DATE
	A		PRODUCTION RELEASE			3/24/64



C	DRAWING NO. 202496	REV A

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

LIST OF MATERIAL

SUPPLEMENTARY INFORMATION		NAME	DATE
FIRST USED ON 264008-1	dp/p 3310	DES	
NEXT ASSEMBLY		DRFT	J. Roper 12/9/63
201977		CHKR	J. Kellerman 1-10-64
		APP	R. Weigale 1/9/64
		APP	H. Baum 1/10/64

MATERIAL

FINISH

DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

SCALE NONE

DO NOT SCALE DWG

ALL DIMENSIONS ARE IN INCHES

TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL ± ——
FRACTION ± ——
ANGLE ± ——

data products corporation
CULVER CITY, CALIFORNIA

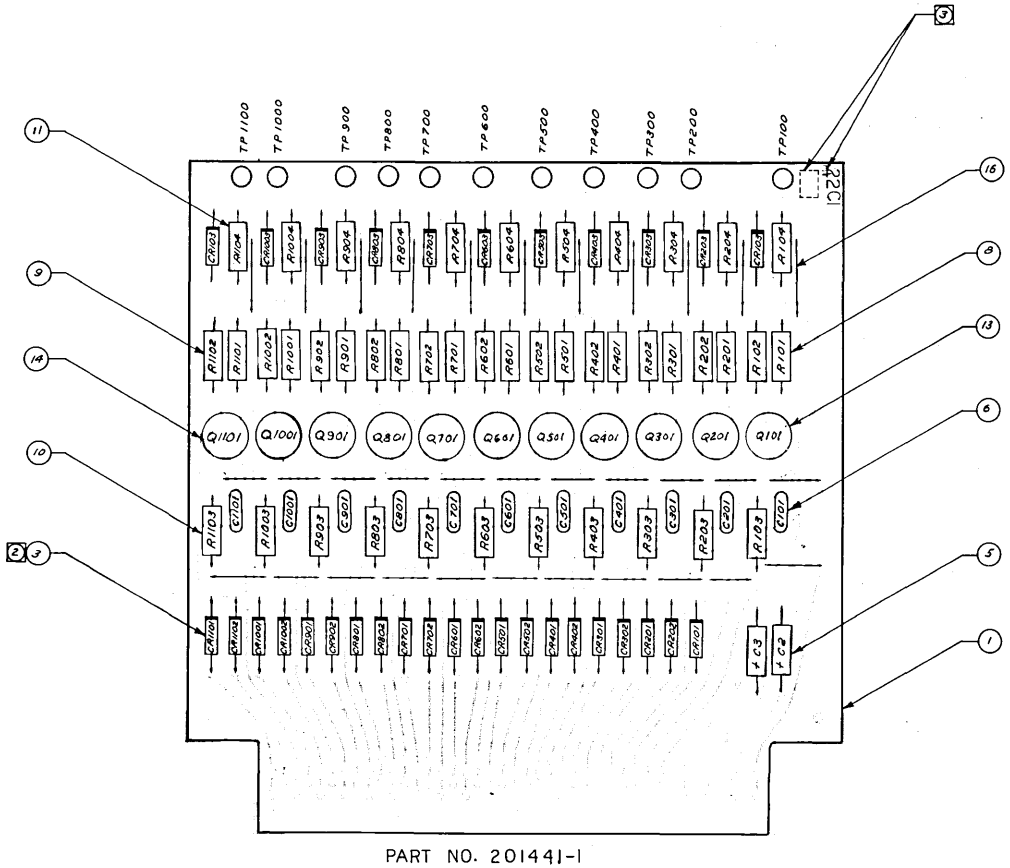
TITLE SCHEMATIC
LOGIC DRIVER 2IV1

C	DRAWING NO. 202496	REV A

SHEET 1 CONT. ON ——

6. ASSEMBLY DRAWING NO. 201977
5. ALL 10μf CAPACITORS ±20% 20V
4. ALL CAPACITORS 620PF ±5% 300V
3. ALL RESISTOR VALUES IN OHMS ±5% 1/2W
2. ALL DIODES 200505-1
1. ALL TRANSISTORS 2N1303

NOTES: UNLESS OTHERWISE SPECIFIED.



PART NO. 201441-1

17				
16	A/R		WIRE 22GA.	
15				
14	11	RC05D30-IN	TRANSIPAD (ROBINSON)	
13	11	2N1303	TRANSISTOR	Q101-Q1101
12				
11	11	EB4725	RESISTOR 4.7K ±5% ½W (A.B.)	R104-R1104
10	11	EB2735	RESISTOR 27K ±5% ½W (A.B.)	R103-R1103
9	11	EB3925	RESISTOR 3.9K ±5% ½W (A.B.)	R102-R1102
8	11	EB6825	RESISTOR 6.2K ±5% ½W (A.B.)	R101-R1101
7				
6	11	DM15-621J	CAPACITOR 620pf ±5% 300V(ARCO)	C101-C1101
5	2	1500106X0020B2	CAPACITOR 10mf ±20% 20V(SPRAG	C2, C3
4				
3	32	200505-1	DIODE	
2				
1	1	201440-1	PROCESSED BOARD NAN GATE 22C	
ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

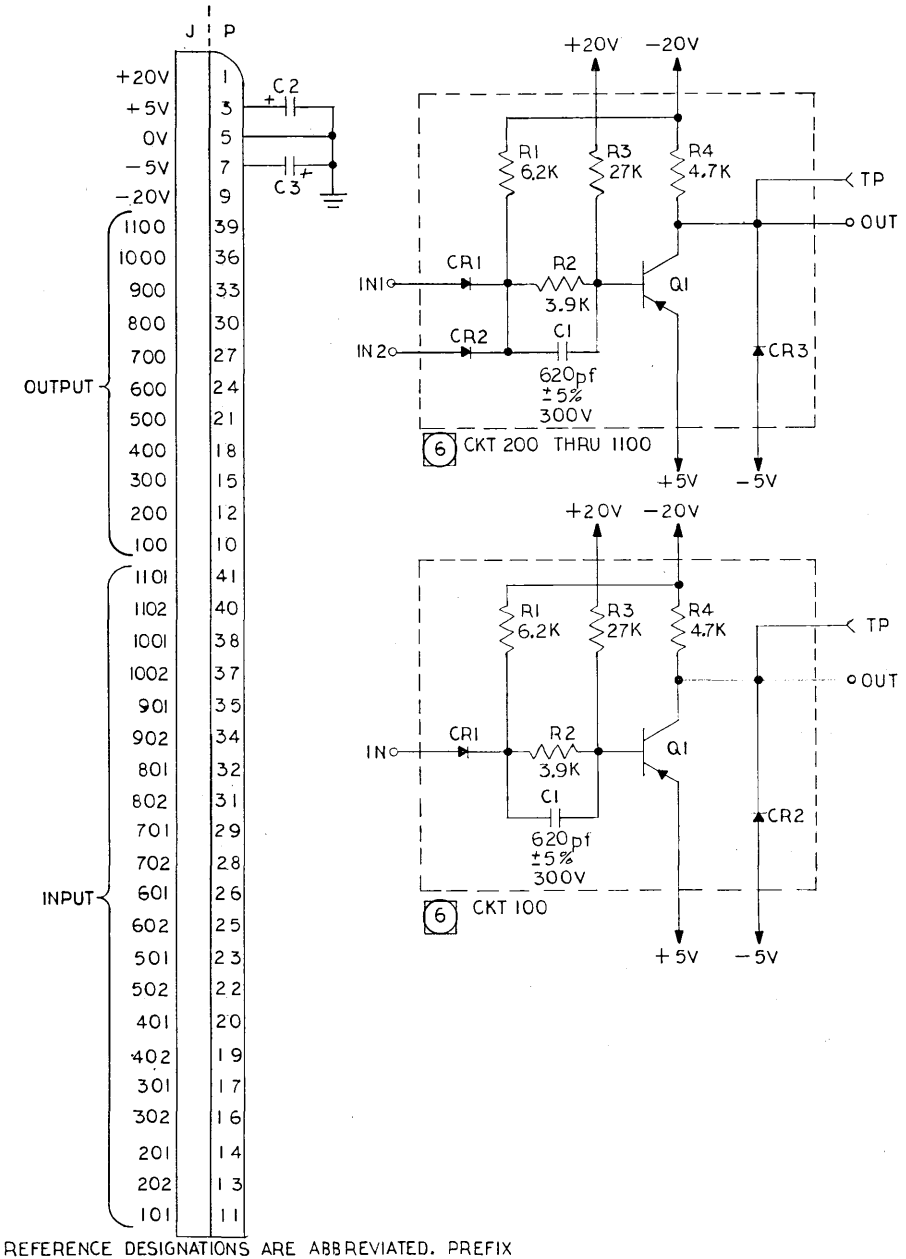
data products corporation
CULVER CITY, CALIFORNIA

TITLE ASSEMBLY
NAN GATE 22CI

D | DRAWING NO. 201441 | REV D
SHEET 1 CONT. ON —

(3) STAMP BOARD TYPE 22CI AND CURRENT ASS'Y. REV. LETTER 1/8" HIGH BLACK IN UPPER RIGHT CORNER.
(2) STRIPE ON DIODE INDICATES CATHODE. -|▶|-

NOTES: 1. SCHEMATIC DRAWING NO. 201438.
UNLESS OTHERWISE SPECIFIED.



6 REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE PART DESIGNATION WITH THE SUBASSEMBLY DESIGNATION.

5 ASSEMBLY DWG. NO. 201441.

4. ALL DIODES 200505-1

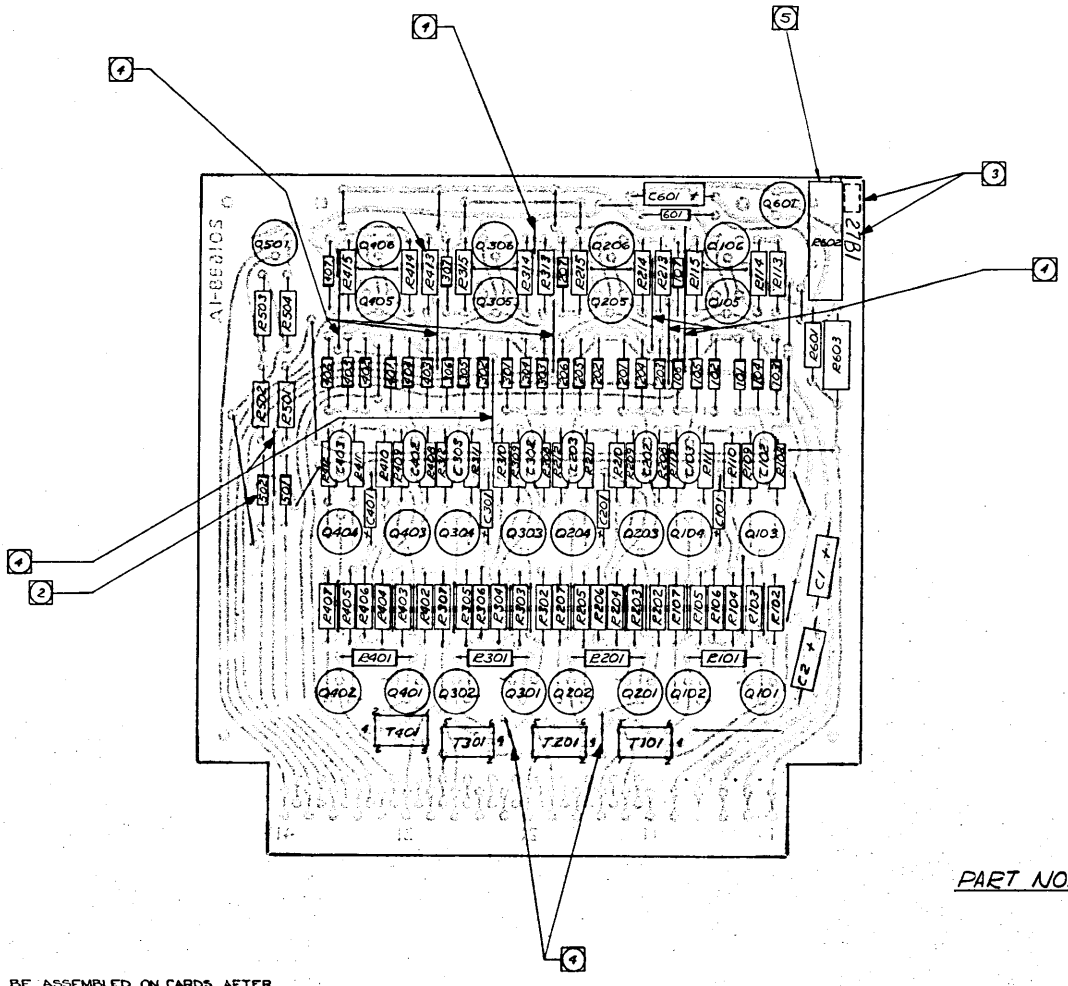
3. ALL TRANSISTORS 2N1303

2. ALL CAPACITORS 10uf, ±20%, 20V.

1. ALL RESISTOR VALUES IN OHMS ±5%, 1/2W.

NOTES: UNLESS OTHERWISE SPECIFIED.

data products corporation CULVER CITY, CALIFORNIA	
TITLE: SCHEMATIC NAN GATE 22C1	
C	DRAWING NO. 201438 SHEET CONT. ON
	REV B



34	A/R		WIRE (22 GA.)		
33					
32	26	RC-05090-WJ	TRANSIPAD		
31					
30	1	EB5125	RESISTOR	5.1K 1/2W ±5% (AB)	R503
29	4	EB3935		39K	R113, R213, R313, R413
28	12	EB1235		12K	R104-R404, R106-R406, R114-R414
27	5	EB6225		6.2K	R101-R501
26	1	EB4725		4.7K	R504
25	4	EB6825		6.8K	R115-R415
24	4	EB1225		1.2K	R110-R410
23	1	EB1025		1K	R502
22	1	EB8215		820Ω 1/2W ±5% (AB)	R601
21	8	CDM 1/8 1.47K		1.47K ±1%	R102-R402, R107-R407
20	8	CDM 1/8 1K		1K ±1%	R108-R408, R112-R412
19	16	CDM 1/8 221		221Ω ±1%	R103-R403, R105-R405, R109-R409, R111-R411
18	1	GB1025	RESISTOR	1K 1W ±5% (A-B)	R603

17	1	3067P-1-501	RESISTOR 500Ω TRIMPOT (BOURNS)	R602
16				
15	4	150D105X0035A2	CAPACITOR 1μf ±20% 35V (SPRAGUE)	C101-C401
14	3	150D106X0035B2	CAPACITOR 6.8μf ±20% 35V (SPRAGUE)	C1, C2, C601
13	8	DM15 471J	CAPACITOR 470pf ±5% (ARCO)	C102-C403
12				
11	1	2N7064	TRANSISTOR	Q501
10	1	2N1303	TRANSISTOR	Q601
9	16	2N1499A	TRANSISTOR	Q101-401, Q105-405, Q102-402, Q106-406
8	8	2N2048	TRANSISTOR	Q103-Q403, Q104-Q404
7				
6	1	1N751	DIODE	CR601
5	30	200554-1	DIODE	CR101-CR502
4				
3	4	QAXHA	TRANSFORMER (TECHNITROL)	T101-T401
2				
1	1	201688-1	BOARD, PROCESS-READ AMP.	278
REQ'D.	REV'D	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

PART NO. 201689-1

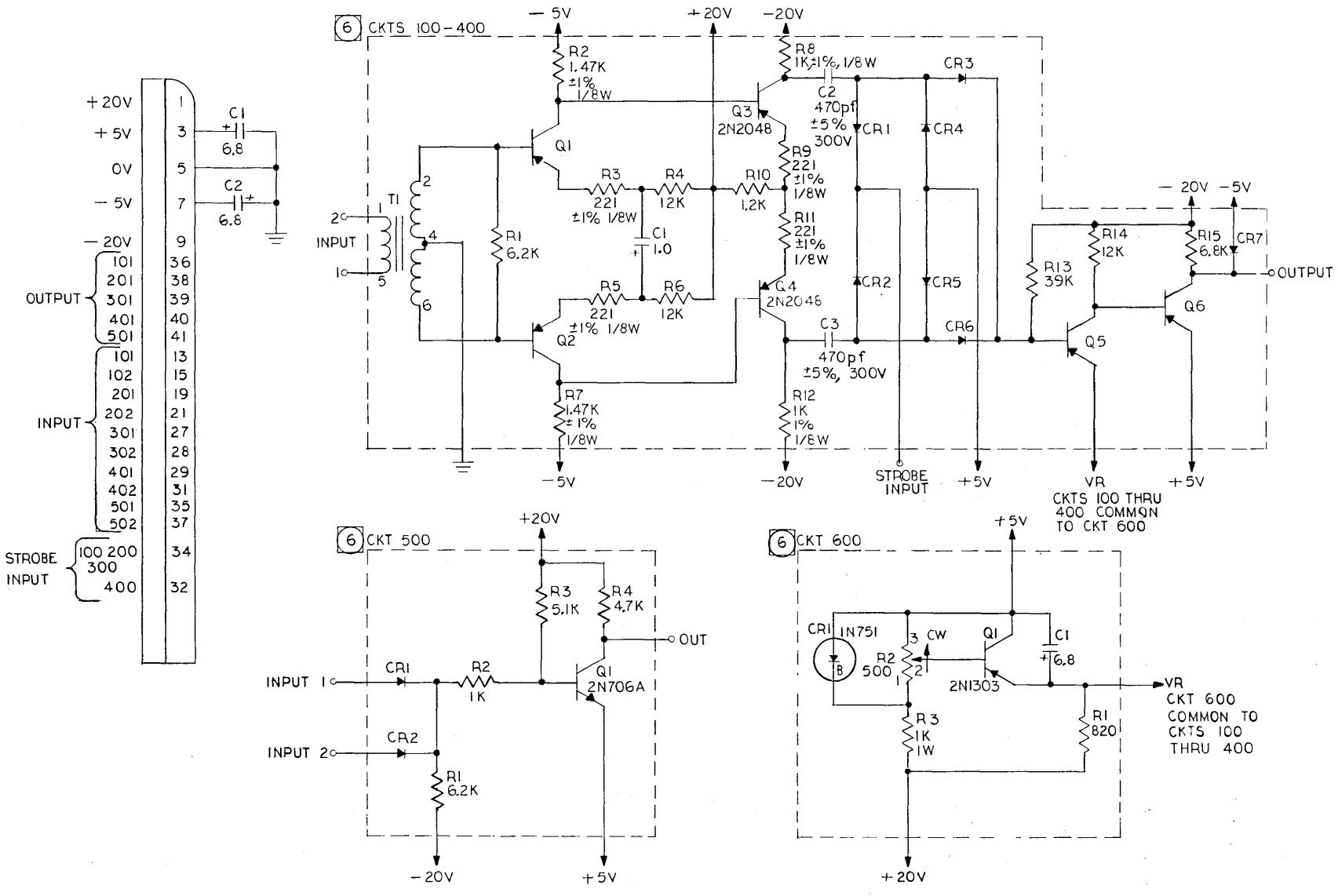
5. TRIMPOTS SHALL BE ASSEMBLED ON CARDS AFTER SOLDERING AND CLEANING OPERATIONS ARE COMPLETED TO PREVENT FLUX AND CLEANING SOLVENTS ENTERING TRIMPOTS.
4. SLEEVE JUMPER
3. STAMP BOARD TYPE 27BI, AND CURRENT ASSY. REV. LETTER IN UPPER RIGHT HAND CORNER OF BOARD AS SHOWN, 1/8" HIGH, BLACK.
2. STRIPE ON DIODE INDICATES CATHODE. -|+|-
1. SCHEMATIC DWG. NO. 201686

NOTES: UNLESS OTHERWISE SPECIFIED.

data products corporation
CULVER CITY, CALIFORNIA

TITLE CKT. BD. ASSEMBLY
READ AMP 27BI

D | DRAWING NO. 201689 | REV G
SHEET 1 | CONT. ON ———

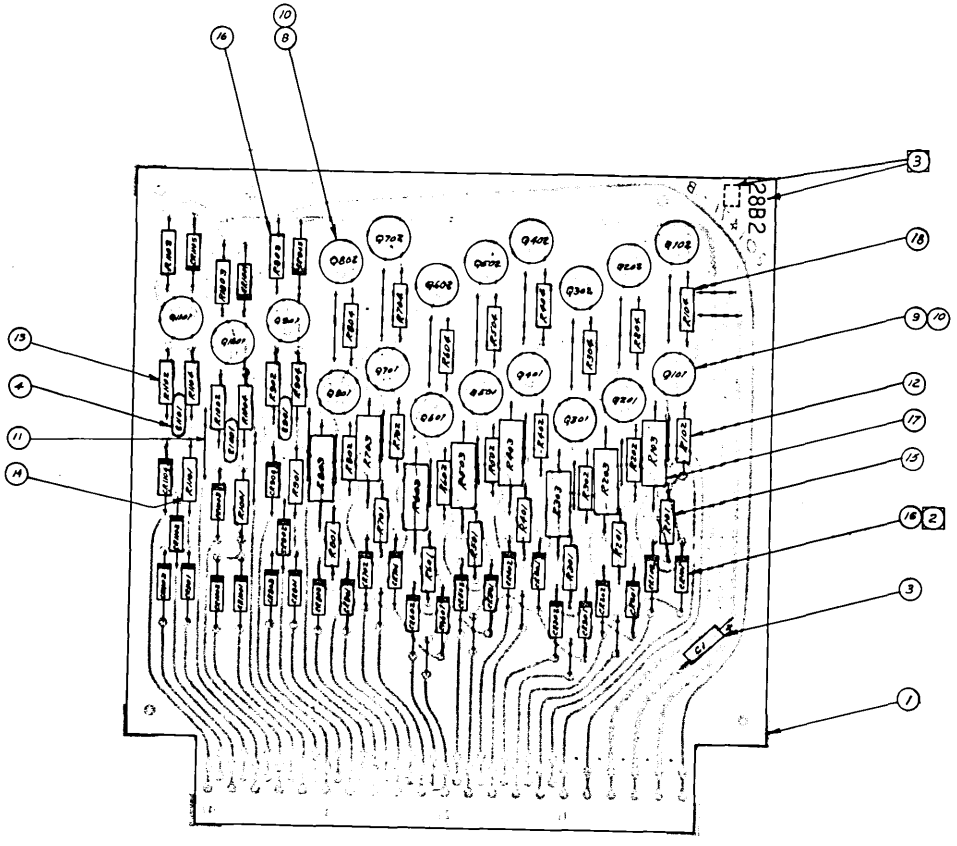


7. ASSEMBLY DWG NO 201689.
6. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE PART DESIGNATION WITH THE SUBASSEMBLY DESIGNATION.
5. ASSEMBLY DWG NO 201689
4. ALL CAPACITOR VALUES IN uf, ±20%, 35V.
3. ALL DIODES 200505-1.
2. ALL RESISTOR VALUES IN OHMS, ±5%, 1/2 W.
1. ALL TRANSISTORS 2N1499A.

NOTES: UNLESS OTHERWISE SPECIFIED

data products corporation	CULVER CITY, CALIFORNIA
TITLE	SCHEMATIC READ AMPLIFIER 2781
C	DRAWING NO. 201686
REV	D
SHEET 1	CONT. ON ~

REVISIONS					
ZONE	REV	ECO NO.	DESCRIPTION	CHKR	APP	DATE
	C		REDRAWN TO STANDARD FORMAT. NO CHG WAS A SIZE PRODUCTION RELEASE			12/1/63
	D	332	R809 WAS R809 ONLY			2/19/64
	E	421	SEE ECO. # 421			9/4/64
	F	460	SEE E.C.O. #460			11/1/64



PART NO 201472-1

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION
18	8	RW59V1101	RESISTOR-1000Ω 5W ±5% (CORNING)	R104 – R804
17	8	EB1025	RESISTOR-1K, 1W ±5% (AB)	R103, 203, 303, 403, 503, 603, 703, 803
16	3	EB2735	RESISTOR-27K, ½W ±5% (AB)	R903, 1003, 1103
15	8	EB1035	RESISTOR-10K ½W ±5% (AB)	R101, 201, 301, 401, 501, 601, 701, 801
14	3	EB7525	RESISTOR-7.5K, ½W ±5% (AB)	R901, 1001, 1101
13	6	EB4725	RESISTOR-4.7K, ½W ±5% (AB)	R902, 904, 1002, 1004, 1102, 1104
12	8	EB2215	RESISTOR-220Ω ½W ±5% (AB)	R102, 202, 302, 402, 502, 602, 702, 802
11				
10	19	RC-05030-IN	TRANSIPAD (ROBINSON)	
9	8	2N1302	TRANSISTOR-	Q101 – Q801
8	11	2N1303	TRANSISTOR-	Q901, Q1001, Q1101, Q102 – Q802
7				
6	30	200505-1	DIODE	CR101 – CR1106
5				
4	3	DM15-621J	CAPACITOR-620μμF ±5% 300V (APCO)	C901, C1001, C1101
3	1	150D687X0020B2	CAPACITOR-10μF ±20% 20V (SPRAGUE)	C1
2				
1	1	201471-1	PROCESSED BOARD – 28B	

LIST OF MATERIAL

D DRAWING NO. 201472 REV F

1. STAMP BOARD TYPE 28B2 AND CURRENT ASSY REV LETTER IN UPPER RIGHT CORNER AS SHOWN ⅛" HIGH, BLACK.
2. STRIPE ON DIODE INDICATES CATHODE.
1. SCHEMATIC DRAWING NO. 201469.

NOTES: UNLESS OTHERWISE SPECIFIED.

SUPPLEMENTARY INFORMATION		NAME	DATE
FIRST USED ON 232002-1 Mfg 3310	DES		
NEXT ASSEMBLY 201751	DRFT	Parker	9-7-63
	CHKR	J. Rogers	12-16-63
	APP	[illegible]	12/17/63
	APP	[illegible]	12/17/63

MATERIAL / FINISH — DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

SCALE 2-1 — DO NOT SCALE DWG — ALL DIMENSIONS ARE IN INCHES — TOLERANCES UNLESS OTHERWISE NOTED: DECIMAL ±, FRACTION ±, ANGLE ±

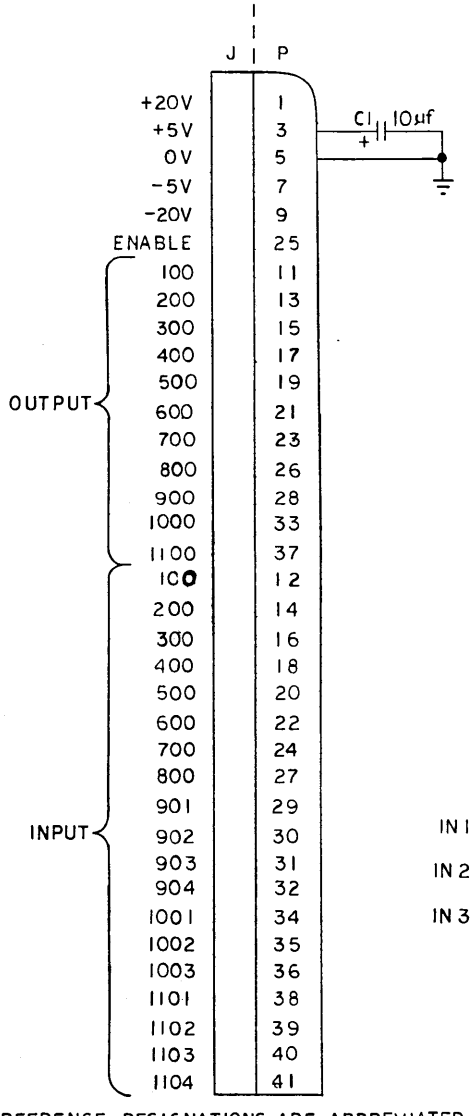
data products corporation
CULVER CITY, CALIFORNIA

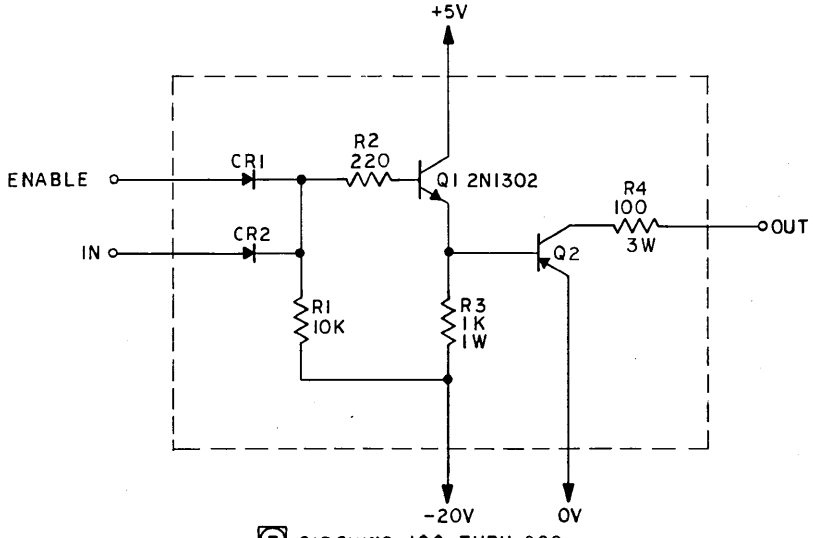
TITLE: ASSEMBLY — INHIBIT DRIVER 28B2

D DRAWING NO. 201472 REV F

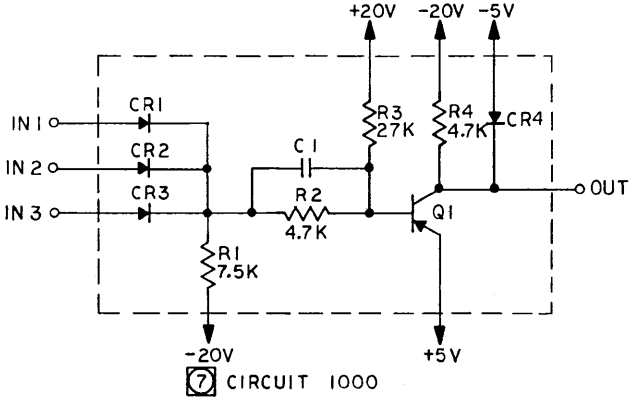
SHEET 1 CONT. ON —

REVISIONS						
ZONE	REV	ECO NO.	DESCRIPTION	CHKR	APP	DATE
	B		PRODUCTION RELEASE REDRAWN FROM 'B' SIZE			12/9/63
	C	460	ADDED CR5 TITLE WAS 28B1			7/11/64

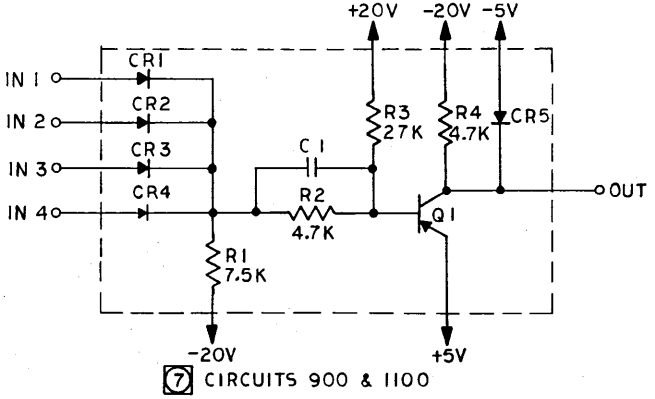




(7) CIRCUITS 100 THRU 800



(7) CIRCUIT 1000



(7) CIRCUITS 900 & 1100

C DRAWING NO. 201469 REV C

(7) REFRENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE PART DESIGNATION WITH THE SUBASSEMBLY DESIGNATION.

6. ASSEMBLY DRAWING NO. 201472.
5. ALL 10µf CAPACITORS ±20% 20V.
4. ALL CAPACITORS 620pf ±5% 300V.
3. ALL RESISTOR VALUES IN OHMS ±5% 1/2W.
2. ALL DIODES 200505-1.
1. ALL TRANSISTORS 2N1303

NOTES: UNLESS OTHERWISE SPECIFIED.

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

LIST OF MATERIAL

SUPPLEMENTARY INFORMATION

FIRST USED ON 252003-1 dpp3310

NEXT ASSEMBLY

	NAME	DATE
DES		
DRFT	J. Griffith	9/13/63
CHKR	J. Murray	12-2-63
APP	[illegible]	12-9-63
APP	[illegible]	12/9/63

MATERIAL

FINISH

DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

SCALE NONE

DO NOT SCALE DWG

ALL DIMENSIONS ARE IN INCHES

TOLERANCES UNLESS OTHERWISE NOTED

DECIMAL ± —

FRACTION ± —

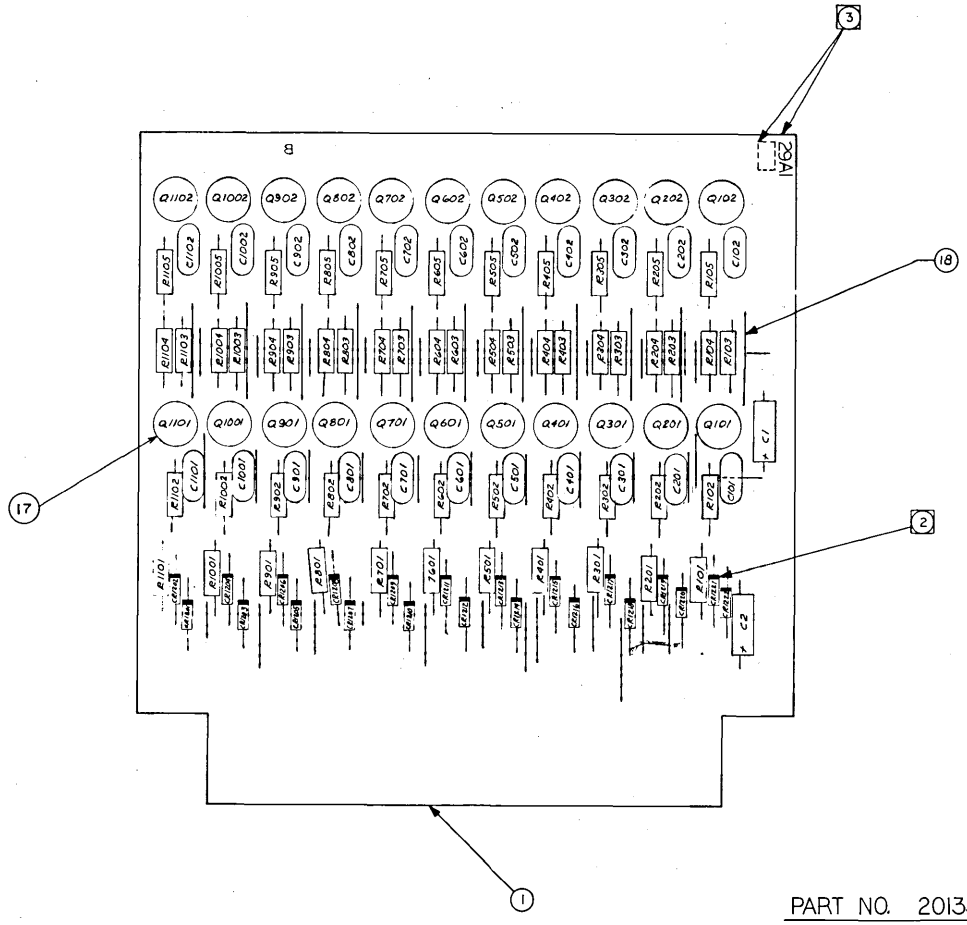
ANGLE ±

data products corporation
CULVER CITY, CALIFORNIA

TITLE SCHEMATIC — INHIBIT DRIVER 28B2

C DRAWING NO. 201469 REV C

SHEET 1 CONT. ON ~



PART NO. 201332-1 REV. B

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION
18	AR		WIRE 22 AWG SOL TINNED	
17	22	PC03090-1N	TRANSIPAD (ROBINSON)	
16	11	2N1169	TRANSISTOR	Q102-Q1102
15	11	2N1303	TRANSISTOR	Q101-Q1101
14				
13				
12	11	EB2725	RESISTOR-2.7K ±5% ½W (AB)	R102-R1102
11	11	EB5125	RESISTOR-5.1K ±5% ½W (AB)	R101-R1101
10	11	EB1235	RESISTOR-12K ±5% ½W (AB)	R103-R1103
9	11	EB2215	RESISTOR-220Ω ±5% ½W (AB)	R105-R1105
8	11	EB3315	RESISTOR-330Ω ±5% ½W (AB)	R104-R1104
7				
6	22	200505-1	DIODE	CR1201-CR1222
5	11	DM15-102J	CAPACITOR-1000pf ±5% 100V (ARCO)	C102-C1102
4	11	DM15-621J	CAPACITOR-620pf ±5% 300V (ARCO)	C101-C1101
3	2	150D106X0020B2	CAPACITOR-10μf 20V (SPRAGUE)	C1, C2
2				
1	1	201331-1	PROCESSED BOARD - 29A	

4. USE SLEEVING AS REQUIRED.
3. STAMP BOARD TYPE 29AI AND CURRENT ASSY REV LETTER IN UPPER RIGHT CORNER AS SHOWN 1/8" HIGH BLACK
2. STRIPE ON DIODE INDICATES CATHODE. -|◀|-
1. SCHEMATIC DWG NO 201329.

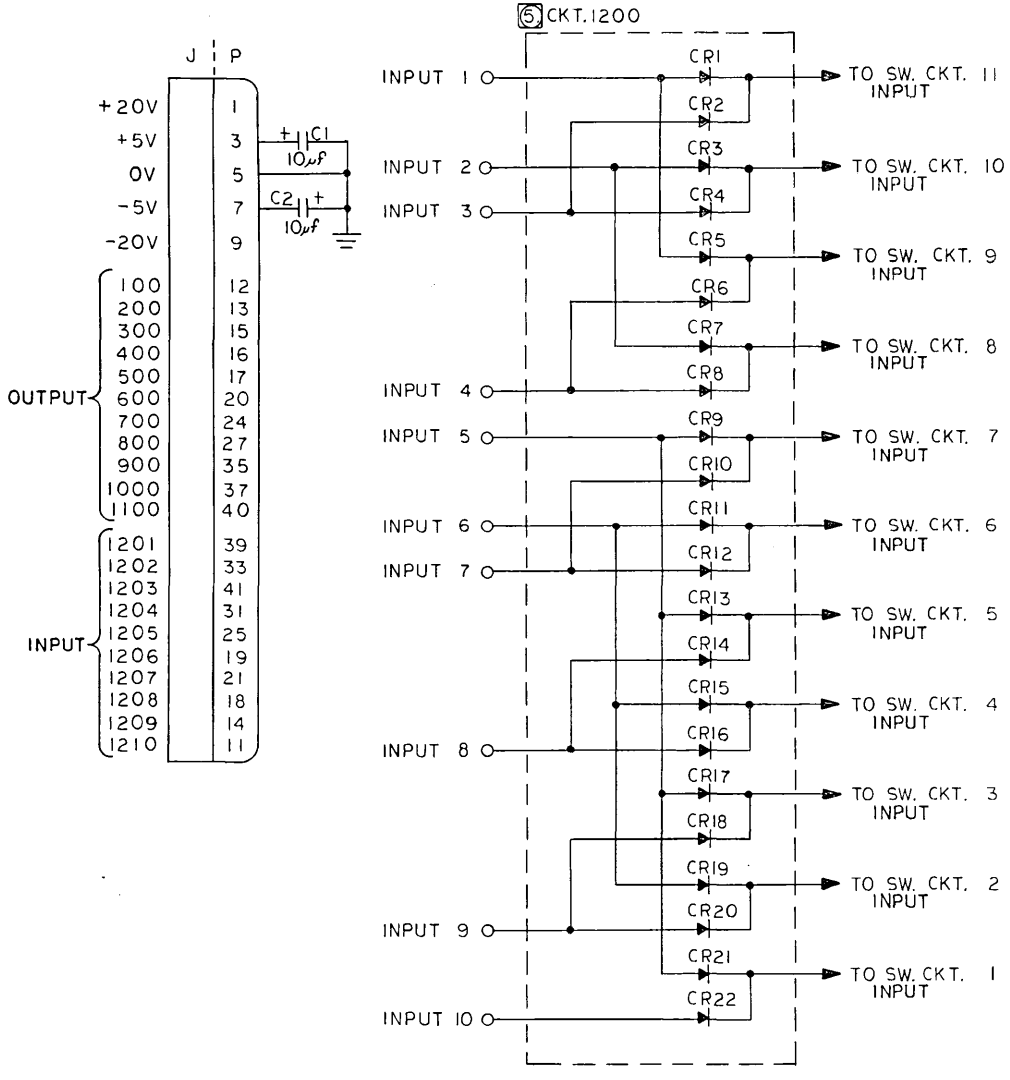
NOTES: UNLESS OTHERWISE SPECIFIED.

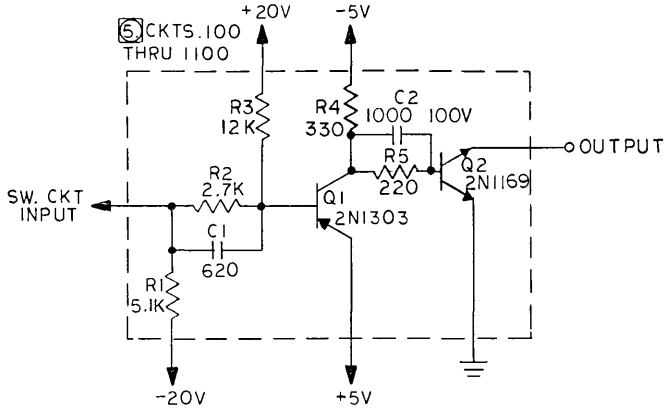
data products corporation
CULVER CITY, CALIFORNIA

TITLE: ASSEMBLY-
SELECTION SWITCH 29A1

D | DRAWING NO. 201332 | REV C

SHEET 1 CONT. ON ~



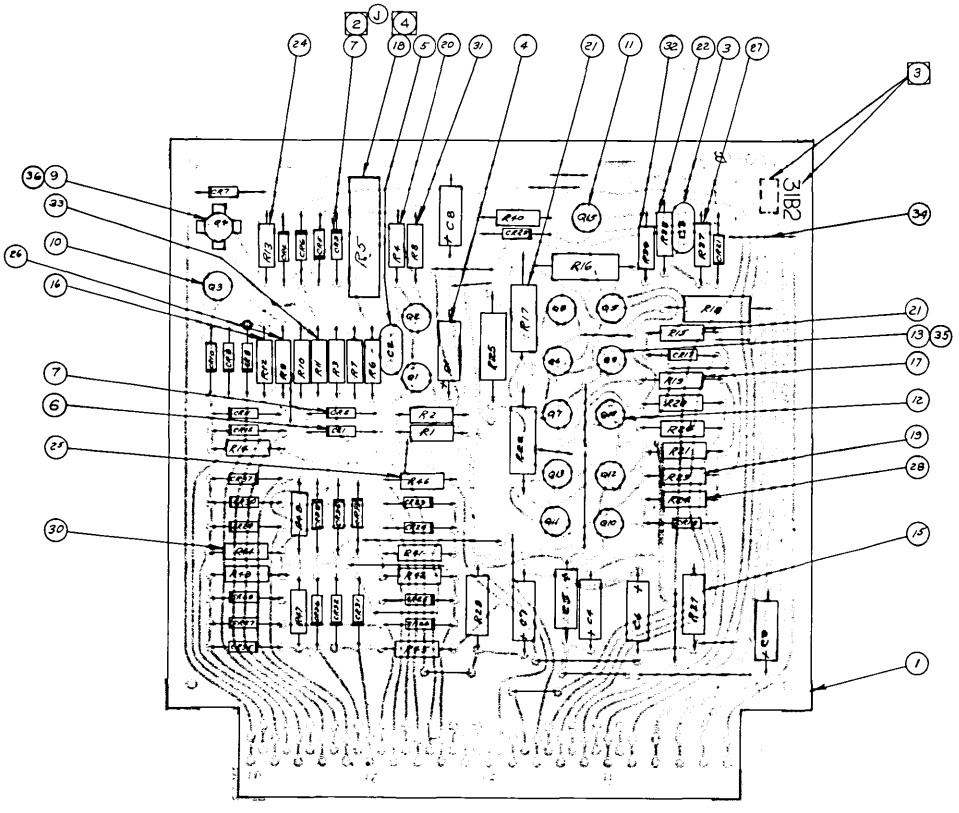


6. ASSEMBLY DRAWING NO. 201332
5 REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE PART DESIGNATION WITH THE SUBASSEMBLY DESIGNATION.
4. ALL 10μf CAPACITORS ±20% 20V
3. ALL CAPACITOR VALUES IN μf ±5% 300V
2. ALL RESISTOR VALUES IN OHMS ±5% 1/2W
1. ALL DIODES 200505-1

NOTES: UNLESS OTHERWISE SPECIFIED.

data products corporation CULVER CITY, CALIFORNIA		
TITLE SCHEMATIC SELECTION SWITCH 29A1		
C	DRAWING NO. 201329 SHEET 1 CONT. ON ———	REV C

REVISIONS						
ZONE	REV	E.C.O. NO.	DESCRIPTION	CHKR	APP	DATE
	F		REDRAWN TO STD FORMAT NO CHANGE, WAS "B" SIZE PRODUCTION RELEASE			12/1/64
	G	331	CHANGED: ITEM #3 PART NO. WAS DM19-621J IS DM15-621J			2/3/65
	H	343	ITEM 20 WAS EB6825 IS EB6815			2/19/65
	J	349	SEE E.C.O. #349			2/19/65
	K	378	SEE E.C.O. #378			9/3/65
	L	391	SEE E.C.O.	DK	DK	9-24-65



PART NO. 201777-1

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION
36	1	100069	TRANSIPAD	
35	19	RC05090-IN	TRANSIPAD	
34	A/R		WIRE 22 AWG	
33	1	EB3335	RESISTOR-33K ± 5% ½W (BR)	R11
32	1	EB1235	12K	R35
31	2	EB1035	10K	R8, R10
30	8	EB6825	6.8K	R19, R41-45, R47, R48
29	1	EB5125	5.1K	R3
28	1	EB4725	4.7K	R24
27	1	EB4325	4.3K	R37
26	2	EB3925	3.9K	R7, R9
25	1	EB2725	2.7K	R46
24	2	EB2225	2.2K	R2, R13
23	2	EB1825	1.8K	R15, R40
22	2	EB1525	1.5K ± 5% ½W (BR)	R6, R38
21	5	GB1025	1K ± 5% 1W (BR)	R14, R12, R10, R22, R25
20	1	EB6815	680Ω ± 5% ½ (BR)	R4
19	2	EB1025	1K ± 5% ½W (BR)	R1, R23
18	1	3067-P	RESISTOR - 500Ω BOURNS	R5
17	4	2826805	RESISTOR-68Ω ± 5% 3W (SPRAGUE)	R17, R20, R21, R26
16	1	EB1835	RESISTOR-18K ± 5% ½W (BR)	R12
15	2	GM3905	RESISTOR-39Ω ± 2% 3W	R27, R28
14				
13	2	2N1307	TRANSISTOR	Q7, Q9
12	2	2N1306		Q12, Q14
11	6	2N1303		Q10, Q11, Q13, Q15, Q1, Q2
10	4	2N1302		Q3, Q5, Q6, Q8
9	1	2N984	TRANSISTER	Q4
8	1	1N456	DIODE	CR3
7	30	200505-1	DIODE	CR2, CR4-CR14, CR17-CR38
6	1	T1-T1	DIODE	CR1
5	1	DM15-471J	CAPACITOR-470 pF ± 5% 300V (R.P.CO)	C2
4	7	CS20106X0020A2	CAPACITOR-10 μF ± 20% 20V (SPRAGUE)	C1, C4 THRU C9
3	1	DM15-621J	CAPACITOR 620pf ± 5% 300V (ARCO)	C3
2				
1		201776-1	PROCESS-BD CLOCK TIMING 318	

LIST OF MATERIAL

D 201777 REV L

4 TRIMPOTS SHALL BE ASSEMBLED ON CARDS AFTER SOLDERING AND CLEANING OPERATIONS ARE COMPLETED TO PREVENT FLUX AND CLEANING SOLVENTS ENTERING TRIMPOTS

3 STAMP BOARD TYPE 3181 AND CURRENT ASSY REV LETTER IN UPPER RIGHT CORNER AS SHOWN 1/8 HIGH BLACK.

2 STRIPE ON DIODE INDICATES CATHODE.

1 SCHEMATIC DWG NO 201774.

NOTES: UNLESS OTHERWISE SPECIFIED.

SUPPLEMENTARY INFORMATION		NAME	DATE
FIRST USED ON 252003-1 11/8/3310	DES		
NEXT ASSEMBLY	DRFT	Rob Lob	12/3/65
201751-1	CHKR	J. Regan	12/16/65
	APP	S. Trevethan	12/17/65
	APP	W. Warren	12/17/65

MATERIAL

FINISH

DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

SCALE 2:1

DO NOT SCALE DWG

ALL DIMENSIONS ARE IN INCHES

TOLERANCES UNLESS OTHERWISE NOTED

DECIMAL ± .....

FRACTION ± .....

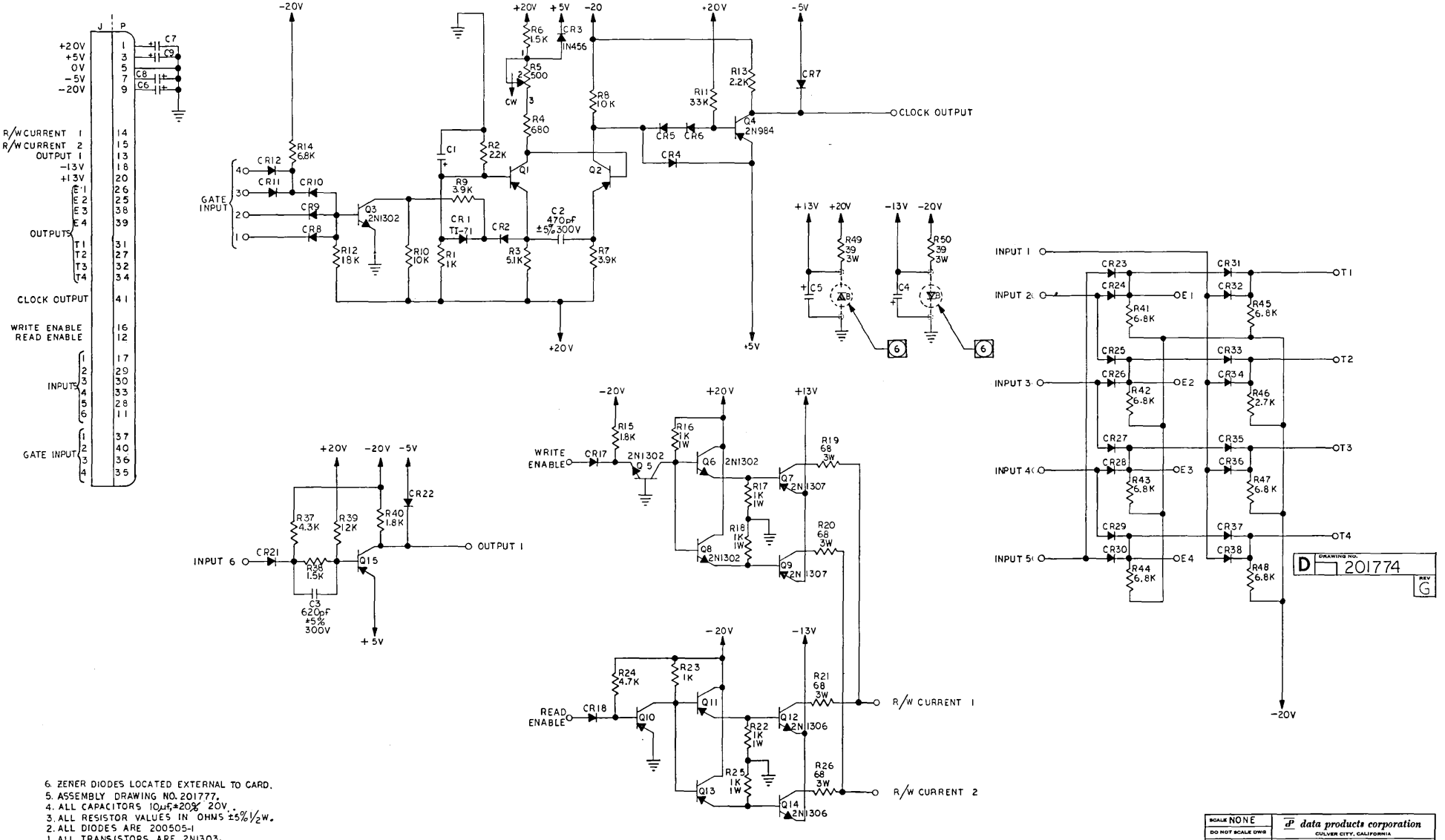
ANGLE ± .....

data products corporation
CULVER CITY, CALIFORNIA

TITLE CKT BOARD ASSY CLOCK TIMING 3182

D 201777 REV L

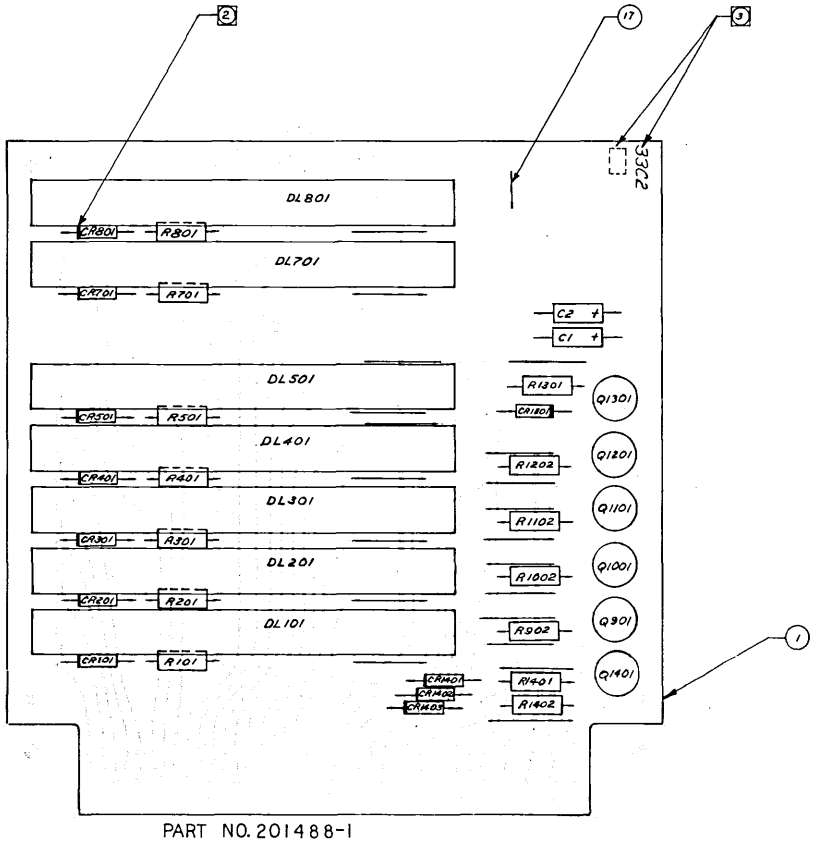
SHEET CONT. ON



6. ZENER DIODES LOCATED EXTERNAL TO CARD.
5. ASSEMBLY DRAWING NO. 201777.
4. ALL CAPACITORS 10μf ±20% 20V.
3. ALL RESISTOR VALUES IN OHMS ±5% 1/2W.
2. ALL DIODES ARE 200505-1
1. ALL TRANSISTORS ARE 2N1303.

NOTES: UNLESS OTHERWISE SPECIFIED.

SCALE NONE	data products corporation, CULVER CITY, CALIFORNIA
DO NOT SCALE DWG	
ALL DIMENSIONS ARE IN INCHES	TITLE: SCHEMATIC CLOCK TIMING 3182
TOLERANCES UNLESS OTHERWISE NOTED: DECIMAL ±, FRACTION ±, ANGLE ±	DRAWING NO. D 201774 REV G
	SHEET / CONT. ON



PART NO. 201488-1

17	A/R		WIRE (22GA.)	
16	1	2N1924	TRANSISTOR	Q1301
15	6	RC05090-1N	TRANSIPAD (ROBINSON)	ALL
14	1	2N1302	TRANSISTOR	Q1401
13	4	2N1304	TRANSISTOR	Q901 - Q1201
12				
11	1	EB4725	RESISTOR 4.7K ½W ±5% (A.B.)	R1401
10	4	EB2725	RESISTOR 2.7K ½W ±5% (A.B.)	R902 - R1202
9	1	EB6825	RESISTOR 6.8K ½W ±5% (A.B.)	RM02
8	8	EB1825	RESISTOR 1.8K ½W ±5% (A.B.)	R101 - R801, R1301
7				
6	11	200505-1	DIODE	CR101 - CR1403
5	7	CZ5GTS-1800-50	DELAY LINE .5MS (TECHNITROL)	DL 101 - DL 108
4				
3	2	150D106X0020BA	CAPACITOR 10μf ±20% 20V	C1 - C2 (SPRAGUE)
2				
1	1	201487-1	PROCESSED BOARD DELAY LINE 33C	
DWG NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

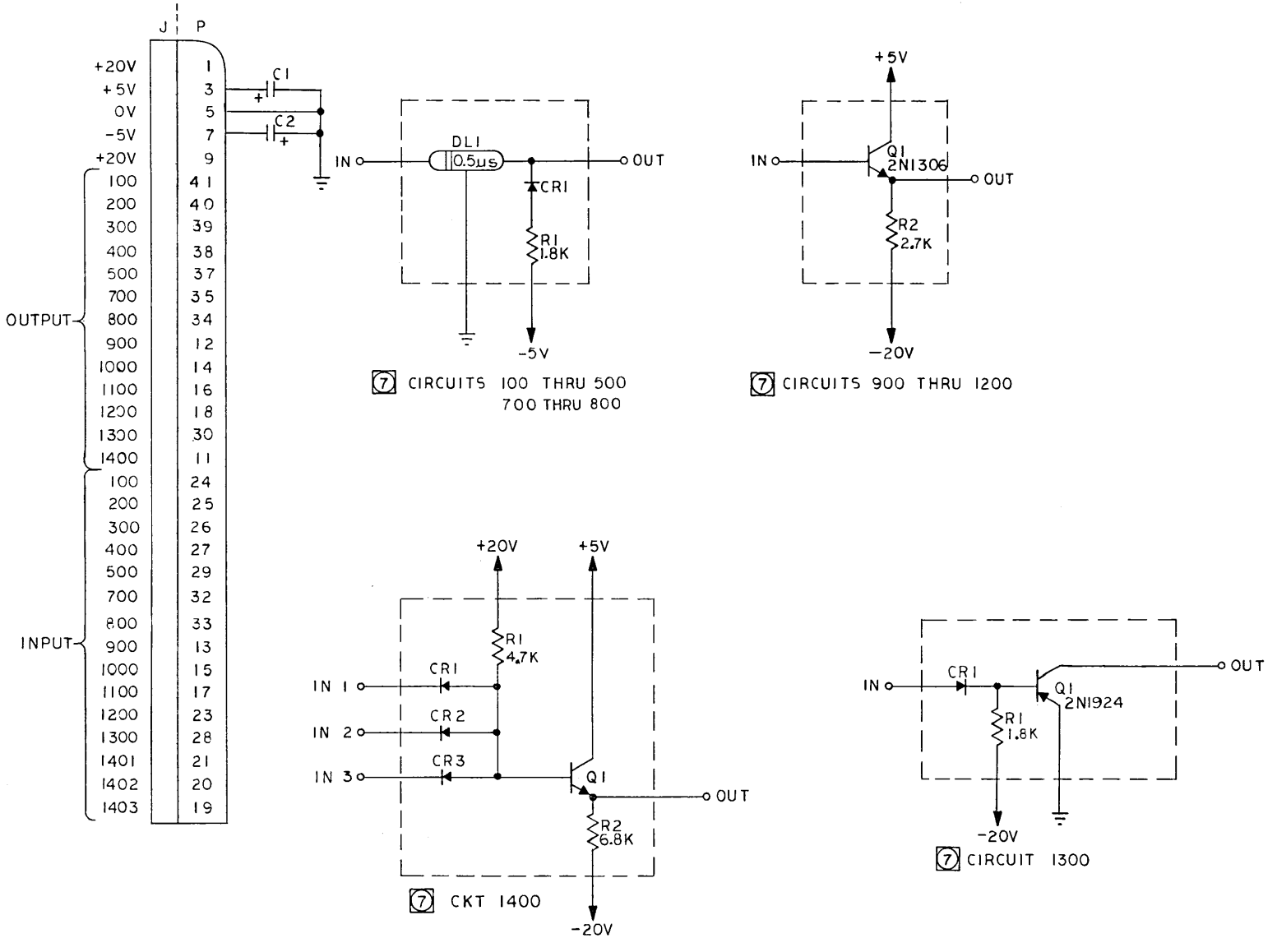
3 STAMP BOARD TYPE 33C1 AND CURRENT ASS'Y REV. LETTER IN UPPER RIGHT HAND CORNER AS SHOWN 1/8" HIGH BLACK.
2 STRIPE ON DIODE INDICATES CATHODE —▶|—
1 SCHEMATIC DRAWING NO. 201485.

NOTES: UNLESS OTHERWISE SPECIFIED.

data products corporation
CULVER CITY, CALIFORNIA

TITLE ASSEMBLY
DELAY LINE 33C2

D | DRAWING NO. 201488 | REV K
SHEET 1 CONT. ON —

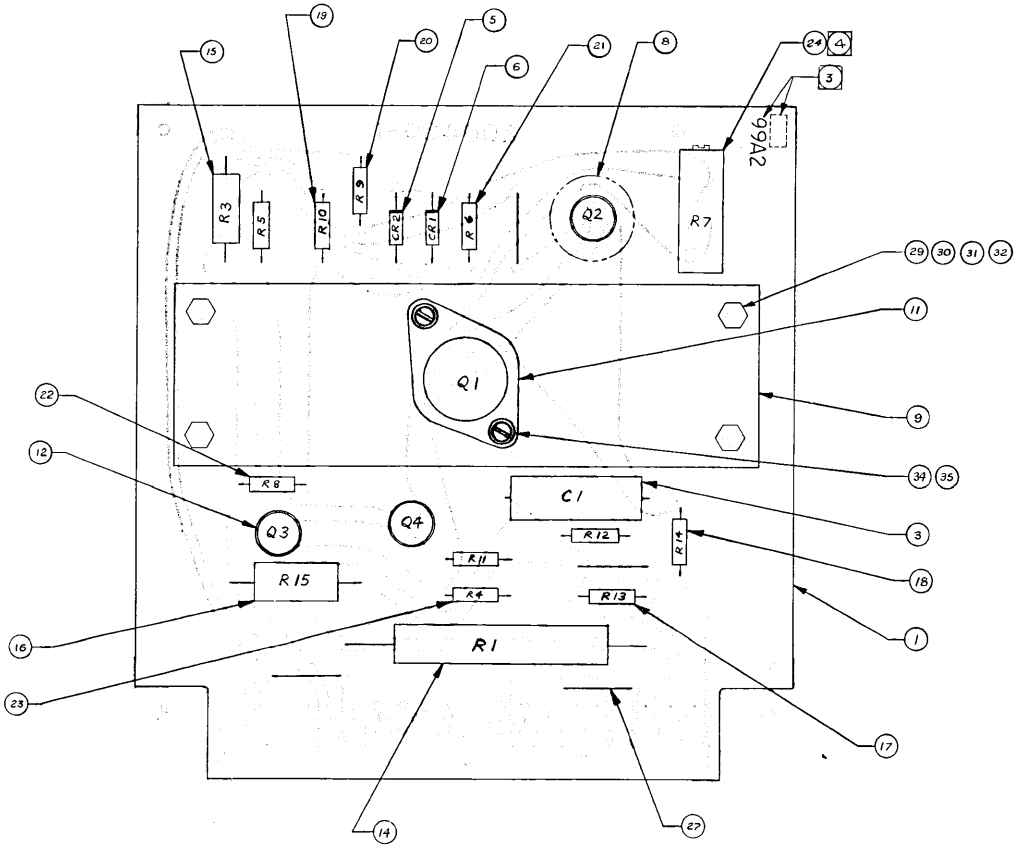


7 REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE PART DESIGNATION WITH THE SUBASSEMBLY DESIGNATION.

6. ASSEMBLY DRAWING NO. 201488.
5. DELAY LINE, TECHNITROL C25GTS-1800-50.
4. ALL RESISTOR VALUES IN OHMS. ±5%, 1/2W.
3. ALL DIODES, 200505-1.
2. ALL CAPACTORS, 10µf ±20% 20V.
1. ALL TRANSISTORS, 2N1302.

NOTES: UNLESS OTHERWISE SPECIFIED.

data products corporation CULVER CITY, CALIFORNIA	
TITLE	SCHEMATIC – DELAY LINE 33C2
C	DRAWING NO. 201485 SHEET | CONT. ON ~
REV	G



35	2		WASHER — FLAT #4	
34	2		WASHER — LOCK, INT, TOOTH #4	
33				
32	4		WASHER - FLAT #6	
31	4	103	INSULATOR (WAKEFIELD)	
30	4		NUT - HEX 6-32	
29	4		SCREW - PAN HD, 6-32 X 3/8 LONG	
28				
27	A R		WIRE 22 AWG	
26				
25				
24	1	3067P-1-101	RESISTOR VARIABLE 100Ω (BOURNS)	R7
23	1	EB3925	RESISTOR 3.9K ±5% 1/2W (AB)	R4
22	3	EB1015	RESISTOR 100Ω ±5% 1/2W (AB)	R5, R8, R12
21	1	EB2215	RESISTOR 220Ω ±5% 1/2W (AB)	R6
20	1	EB1025	RESISTOR 1K ±5% 1/2W (AB)	R9
19	1	EB3915	RESISTOR 390Ω ±5% 1/2W (AB)	R10
18	2	EB2225	RESISTOR-2.2K ±5% 1/2W (AB)	R11 R14

17	1	EB1035	RESISTOR - 10K ±5% 1/2W (AB)	R13
16	1	H85615	RESISTOR - 560Ω ±5% 2W (AB)	R15
15	1	GB 5605	RESISTOR - 56Ω ±5% 1W (AB)	R3
14	1		RESISTOR - 2Ω 10W (TRU OHM)	R1
13				
12	3	2N1303	TRANSISTOR	Q2, Q3, Q4
11	1	2N456 A	TRANSISTOR	Q1
10				
9	1	200679-1	HEAT SINK	
8	1	NF207	HEAT CLIP - (WAKEFIELD)	
7				
6	1	IN754 A	DIODE - 6.8V	CR1
5	1	IN456	DIODE	CR2
4				
3	1	2WF-P22	CAPACITOR-22uF ±10% 200V (SPRAGUE)	C1
2				
1	1	200420-1	PROCESS BOARD -5 VOLTAGE REG 99 A2	
ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

[4] TRIMPOTS SHALL BE ASSEMBLED ON CARDS AFTER SOLDERING AND CLEANING OPERATIONS ARE COMPLETED TO PREVENT FLUX AND CLEANING SOLVENTS ENTERING TRIMPOTS

[3] STAMP BOARD TYPE 99A2, AND CURRENT ASSY. REV. LETTER IN UPPER RIGHT HAND CORNER OF BOARD AS SHOWN, 1/8 HIGH

[2] STRIPE ON DIODE INDICATES DIRECTION OF CATHODE

1. SCHEMATIC DRAWING NO. 200418

NOTES: UNLESS OTHERWISE SPECIFIED

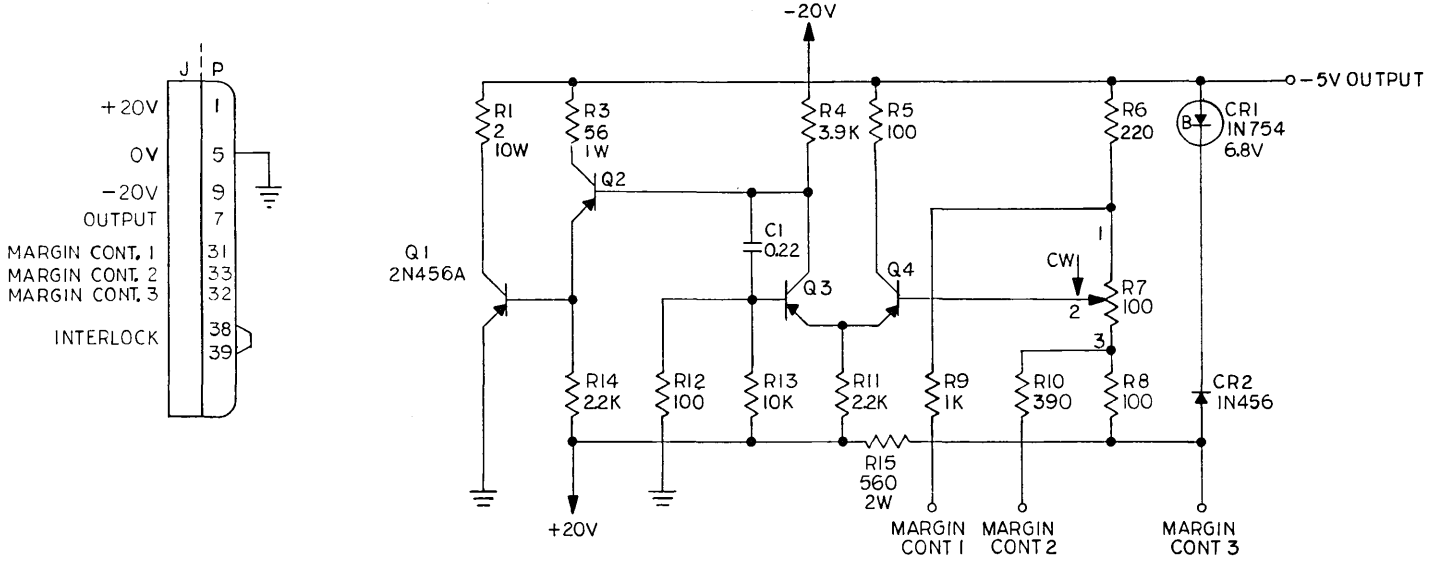
PART NO. 200421-1

data products corporation
CULVER CITY, CALIFORNIA

TITLE CIRCUIT BOARD ASSY -5 VOLT REG. 99A2

D | DRAWING NO. 200421 | REV E

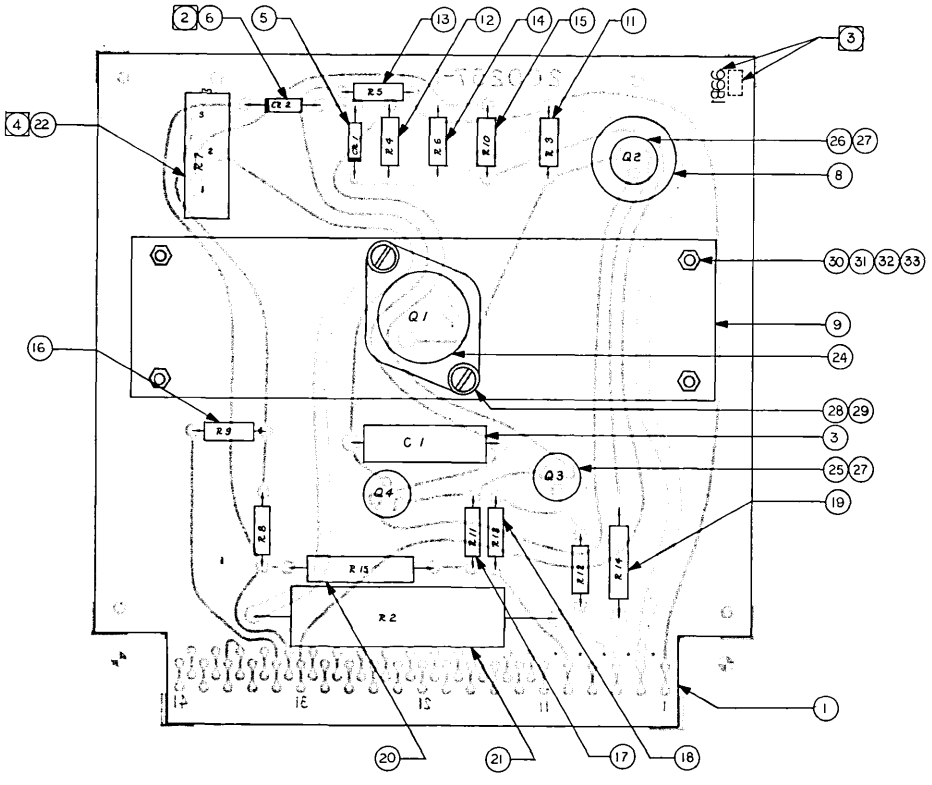
SHEET 1 | CONT. ON —



5. EXTERNAL DROPPING RESISTOR REQUIRED AT OUTPUT.
4. ASSEMBLY DRAWING NO 200421
3. ALL CAPACITOR VALUES IN μf ±10% 200V.
2. ALL TRANSISTORS 2N1303
1. ALL RESISTOR VALUES IN OHMS, ± 5% 1/2W.

NOTE: UNLESS OTHERWISE SPECIFIED

dp data products corporation CULVER CITY, CALIFORNIA		
TITLE SCHEMATIC – –5 VOLTAGE REGULATOR 99A2		
C	DRAWING NO. 200418 SHEET CONT. ON	REV C



ITEM NO.	REQD	PART NUMBER	DESCRIPTION	
33	4		#6 FLAT WASHER	
32	4	103	INSULATOR (WAKEFIELD)	
31	4		#6 HEX. NUT	
30	4		#6 SCREW	
29	2		#4 INTER TOOTH LOCK WASHER	
28	2		#4 FLAT WASHER	
27	3	RC-05090-IN	TRANSIPAD (ROBINSON)	
26	1	2N1303	TRANSISTOR	Q2
25	2	2N1302	TRANSISTOR	Q3, Q4
24	1	2N456A	TRANSISTOR	Q1
23				
22	1	3067P-1-101	RESISTOR, VARIABLE 100Ω (BOURNS)	R7
21	1	4737	RESISTOR 2Ω ±5% 10W (OHMITE)	R2
20	1	HB5615	560Ω ±5% 2W (A.B)	R15
19	1	GB5605	56Ω ±5% 1W (A.B)	R14
18	1	EB1035	10K ±5% 1/2W (A.B)	R13
17	1	EB2225	2.2K ±5% 1/2W (A.B.)	R11
16	1	EB3315	330Ω ±5% 1/2W (A.B)	R9
15	1	EB1825	1.8K ±5% 1/2W (A.B)	R10
14	1	EB2215	220Ω ±5% 1/2W (A.B)	R6
13	1	EB3925	3.9K ±5% 1/2W (A.B.)	R5
12	3	EB1015	100Ω ±5% 1/2W (A.B)	R4, R8, R12
11	1	EB1525	RESISTOR 1.5K ±5% 1/2W (A.B)	R3
10				
9	1	200679-1	HEAT SINK	
8	1	NF207	HEAT CLIP (WAKEFIELD)	
7				
6	1	IN456	DIODE	CR2
5	1	IN754	DIODE, ZENER 6.8V	CR1
4				
3	1	2WF-P22	CAPACITOR .22μf ±10% 200V (SPRAGUE)	C1
2				
1	1	200257-1	PROCESS BOARD, +5V REG. 99B1	

4. TRIMPOTS TO BE ASSEMBLED ON CARDS AFTER SOLDERING AND CLEANING OPERATIONS ARE COMPLETED TO PREVENT FLUX AND CLEANING SOLVENTS ENTERING TRIMPOTS
3. STAMP BOARD TYPE 99B1, AND CURRENT ASSY. REV. LETTER IN UPPER RIGHT HAND CORNER OF BOARD AS SHOWN. 1/8" HIGH
2. STRIPE ON DIODE INDICATES DIRECTION OF CATHODE
1. SCHEMATIC DWG. NO. 200255

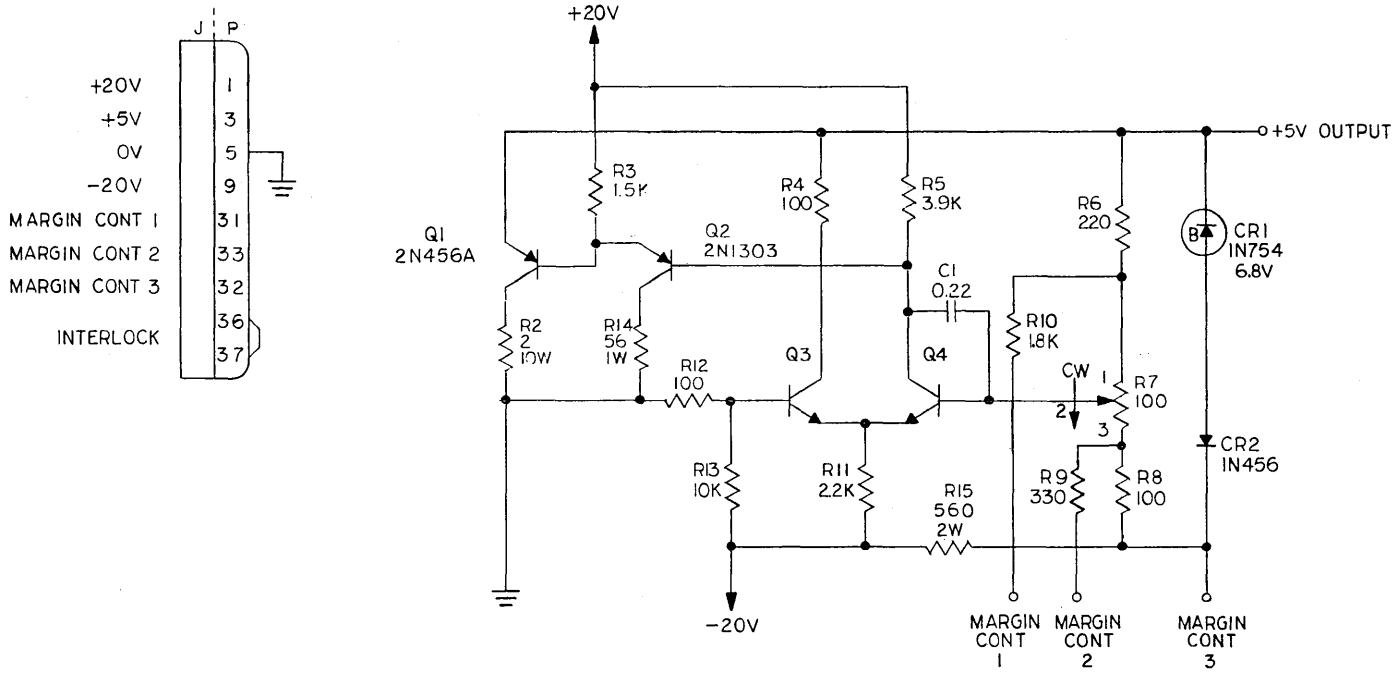
NOTE: UNLESS OTHERWISE SPECIFIED

data products corporation
CULVER CITY, CALIFORNIA

TITLE CKT. BD. ASSY. +5 VOLTAGE REGULATOR 99B1

SIZE	DRAWING NO.	REV
D	200258	D

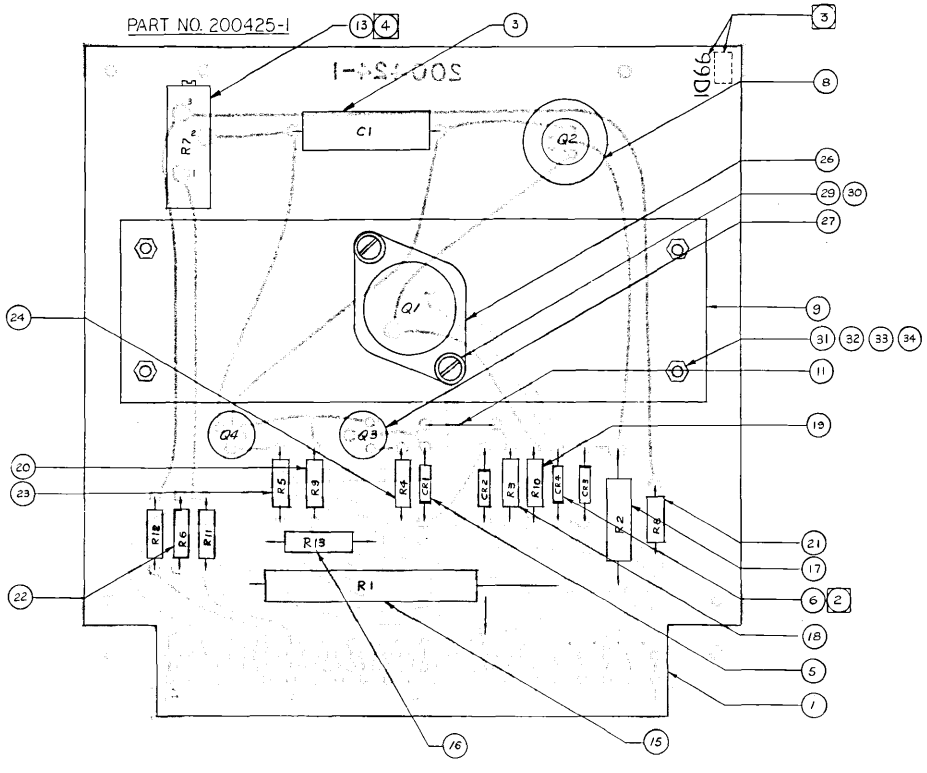
SHEET 1



5. EXTERNAL DROPPING RESISTOR REQUIRED AT OUTPUT.
4. ASSEMBLY DRAWING NO. 200258
3. ALL CAPACITORS VALUES IN $\mu f \pm 10\%$ 200V
2. ALL TRANSISTORS 2N1302
1. ALL RESISTOR VALUES IN OHMS, $\pm 5\%$ $\frac{1}{2}$W

NOTE: UNLESS OTHERWISE SPECIFIED

data products corporation, CULVER CITY, CALIFORNIA			
TITLE: SCHEMATIC- +5 VOLTAGE REGULATOR 9981			
	C	DRAWING NUMBER 200255	REV. B



ITEM NO.	REQD	PART NUMBER	DESCRIPTION	REF. DESN.
39	4		PAN HD. SCREW 6-32 x 3/8 LG.	
33	4		HEX. NUT 6-32	
32	4	103	INSULATOR (WAKEFIELD)	
31	4		#6 FLAT WASHER	
30	2		#4 INTER TOOTH LOCK WASHER	
29	2		#4 FLAT WASHER	
28				
27	3	2N1303	TRANSISTOR	Q2, Q3, Q4
26	1	2N456A	TRANSISTOR	Q1
25				
24	2	EB 1015	RESISTOR 100Ω ±5%, 1/2W (AB)	R4, R11
23	2	EB 2025	RESISTOR 2K ± 5% 1/2W (AB)	R5, R12
22	1	EB 8205	RESISTOR 82Ω ±5% 1/2W (AB)	R6
21	1	EB 4315	RESISTOR 430Ω ±5% 1/2W (AB)	R8
20	1	EB 8215	RESISTOR 820Ω ±5% 1/2W (AB)	R9
19	1	EB 4715	RESISTOR 470Ω ±5% 1/2W (AB)	R10
18	1	EB 2715	RESISTOR 270Ω ±5% 1/2W (AB)	R13
17	1	HB 1015	RESISTOR 100Ω ±5% 2W (AB)	R2
16	1	4387	RESISTOR 75Ω ±5% 3W (OHMITE)	R13
15	1		RESISTOR 15Ω, 10W (TRU OHM)	R1
14				
13	1	3067P-1-201	RESISTOR, VARIABLE 200Ω (BOURNS)	R7
12				
11	A/R		WIRE #22 GA.	ALL
10				
9	1	200679-1	HEAT SINK	
8	1	NF 207	HEAT CLIP (WAKEFIELD)	
7				
6	3	IN 456	DIODE	CR2, CR3, CR4
5	1	IN 754A	DIODE 6.8V	CR1
4				
3	1	2WF-P10	CAPACITOR .1μf ±10% 200V (SPRAGUE)	C1
2				
1	1	200424-1	PROCESS BOARD, -10V. REG. 99DI	

[4] TRIMPOTS SHALL BE ASSEMBLED ON CARDS AFTER SOLDERING AND CLEANING OPERATIONS ARE COMPLETED TO PREVENT FLUX AND CLEANING SOLVENTS ENTERING TRIMPOTS

[3] STAMP BOARD TYPE 99DI, AND CURRENT ASSY. REV. LETTER IN UPPER RIGHT HAND CORNER OF BOARD AS SHOWN, 1/8 HIGH

[2] STRIPE ON DIODE INDICATES DIRECTION OF CATHODE

1. SCHEMATIC DRAWING NO. 200422

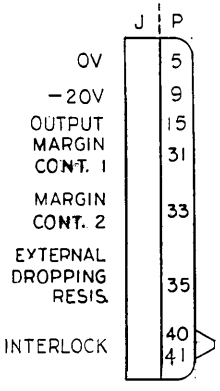
NOTE: UNLESS OTHERWISE SPECIFIED

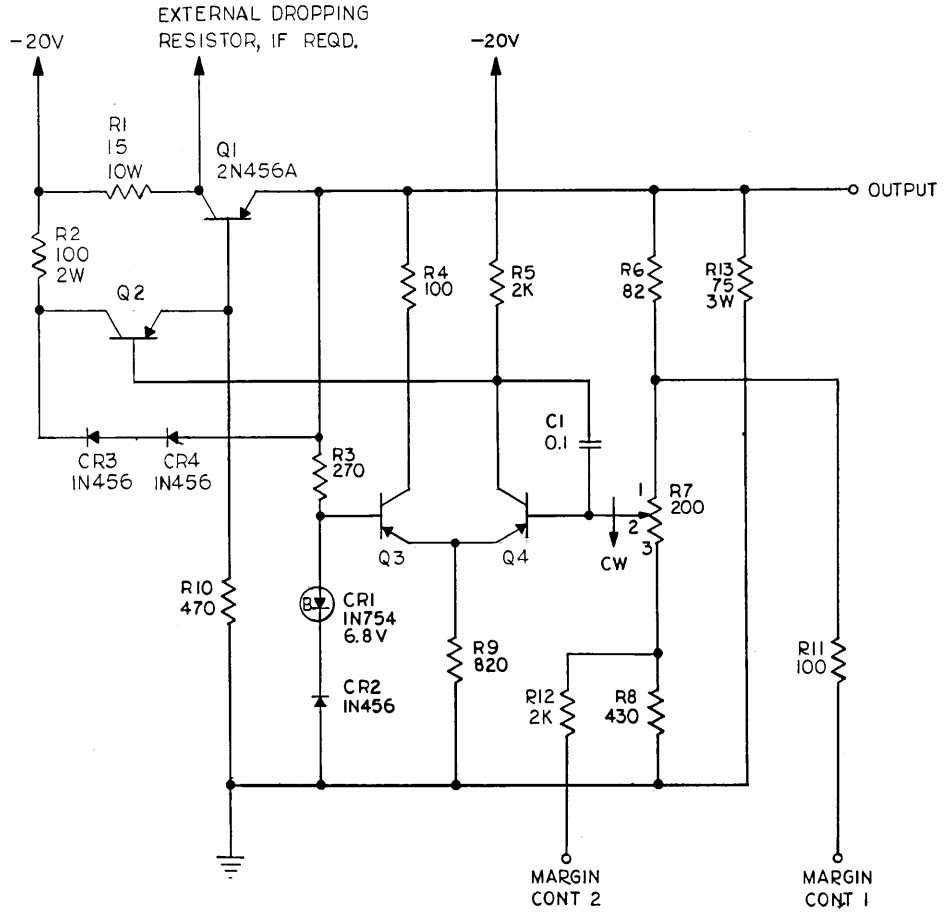
data products corporation
CULVER CITY, CALIFORNIA

TITLE: CKT. BOARD ASSY.
-10 VOLT REGULATOR 99DI

D | DRAWING NO. 200425 | REV D
SHEET 1 | CONT. ON —

NO.	E.C.O. NO.	REVISION	APP'D.	DATE
B		REDRAWN-PRODUCTION RELEASE	P. MC	5-17-63
C	107	±10% 200V WAS ±10% 20V	for Murray	5-9-63





	C	DRAWING NUMBER 200422	REV. C

4. ASSEMBLY DRAWING NO. 200425
3. ALL CAPACITOR VALUES IN μf ±10% 200V
2. ALL RESISTOR VALUES IN OHMS ± 5% $\frac{1}{2}$ W
1. ALL TRANSISTORS 2N1303
NOTE: UNLESS OTHERWISE SPECIFIED

	dp/p 3300	
NEXT ASSY.	USED ON	
DES. BY		
DR. BY	KUBOTA	12-9-62
CKD. BY	Murray	5-8-63
APP. BY		5-14-63
APP. BY		5-14-63

MATERIAL:
FINISH:

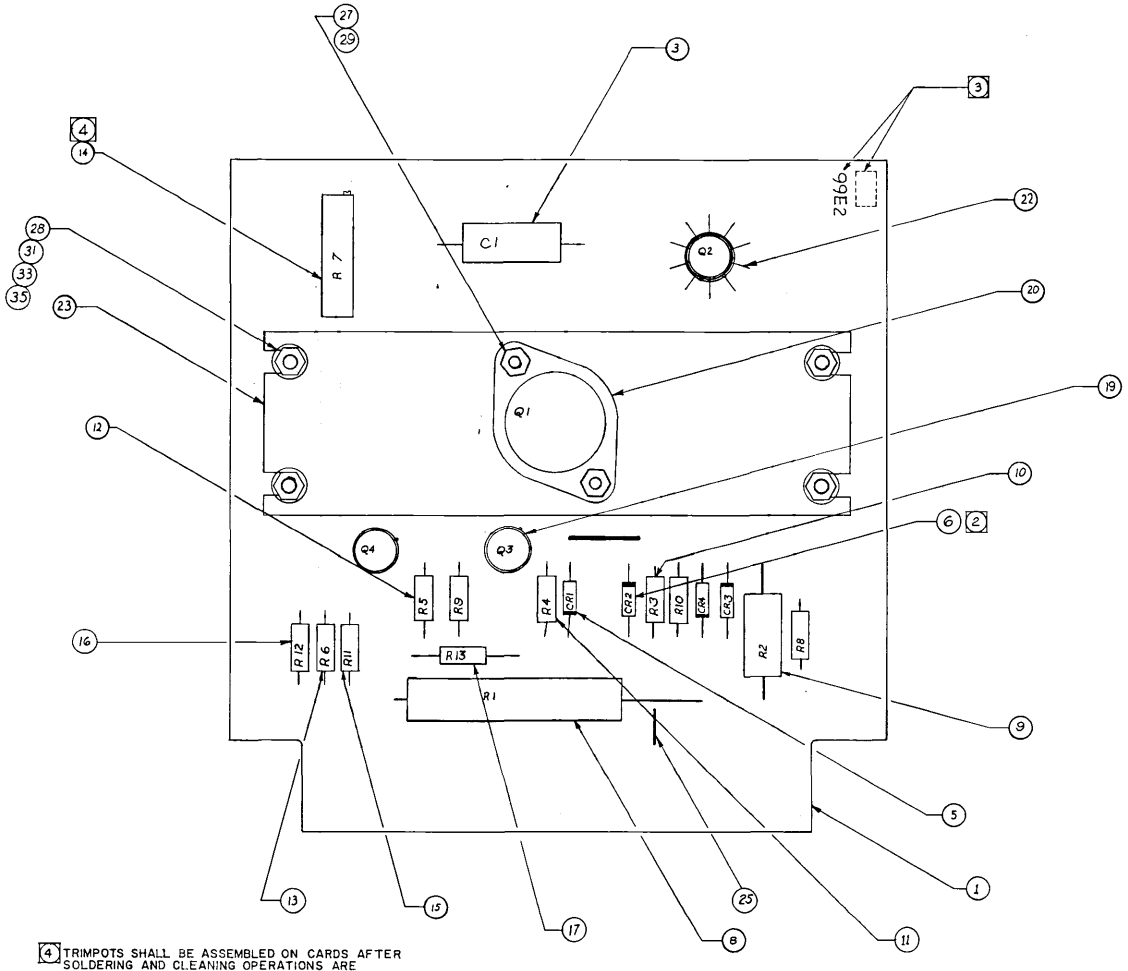
SCALE: NONE
TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL ±
FRACTION ±
ANGULAR ±
DIMENSIONS APPLY AFTER PLATING & HEAT TREATING
SHEET 1 OF 1

data products corporation
CULVER CITY, CALIFORNIA

TITLE: SCHEMATIC
-10 VOLT REGULATOR
99D1

	C	DRAWING NUMBER 200422	REV. C

PART NO. 200429-1



ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION	
35	4	103	INSULATOR (WAKEFIELD)		
34					
33	4	———	HEX NUT 6-32		
32					
31	4	———	PAN HD SCREW 6-32 x 3/8 LG		
30					
29	2	———	#4 INTERTOOTH LOCK WASHER		
28	4	———	#6 FLAT WASHER		
27	2	———	#4 FLAT WASHER		
26					
25	A/R	———	WIRE #22		
24					
23	1	200679-1	HEAT SINK		
22	1	NF207	HEAT CLIP (WAKEFIELD)		
21					
20	1	2N456A	TRANSISTOR	Q1	
19	3	2N1303	TRANSISTOR	Q2,3,4	
18					
17	1	242E1515	RESISTOR 150Ω ±5%,3W(SPRAGUE)	R13	
16	1	EB3925	3.9K ±5%, ½W (A.B.)	R12	
15	1	EB4725	4.7K ±5%, ½W (A.B.)	R11	
14	1	3067P-1-101	VARIABLE 100Ω (BOURNS)	R7	
13	2	EB4315	430Ω ±5% ½W (A.B.)	R6,8	
12	2	EB8215	820Ω ±5% ½W (A.B.)	R5,9	
11	1	EB4715	470Ω ±5%, ½W (A.B.)	R4	
10	2	EB6815	680Ω ±5%, ½W (A.B.)	R3,10	
9	1	HB4705	47Ω ±5%, 2W (A.B.)	R2	
8	1	4746	RESISTOR 4Ω 10W (OHMITE)	R1	
7					
6	3	IN456	DIODE	CR2,3,4	
5	1	IN754A	DIODE	CR1	
4					
3	1	2WF-P10	CAP .1μf ±10%, 200V (SPRAGUE)	C1	
2					
1	1	200428-1	PROCESSED BOARD -15 VOLT REGULATOR 99E2		

4 TRIMPOTS SHALL BE ASSEMBLED ON CARDS AFTER SOLDERING AND CLEANING OPERATIONS ARE COMPLETED TO PREVENT FLUX AND CLEANING SOLVENTS ENTERING TRIMPOTS

3 STAMP BOARD TYPE 99E2, AND CURRENT ASSY. REV LETTER IN UPPER RIGHT HAND CORNER OF BOARD AS SHOWN, 1/8 HIGH

2 STRIPE ON DIODE INDICATES DIRECTION OF CATHODE.

1. SCHEMATIC DRAWING NO. 200426.

NOTES: UNLESS OTHERWISE SPECIFIED

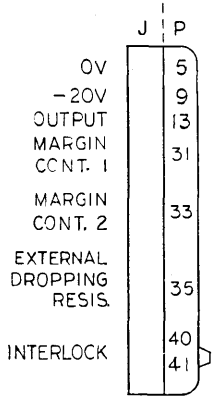
dp data products corporation
CULVER CITY, CALIFORNIA

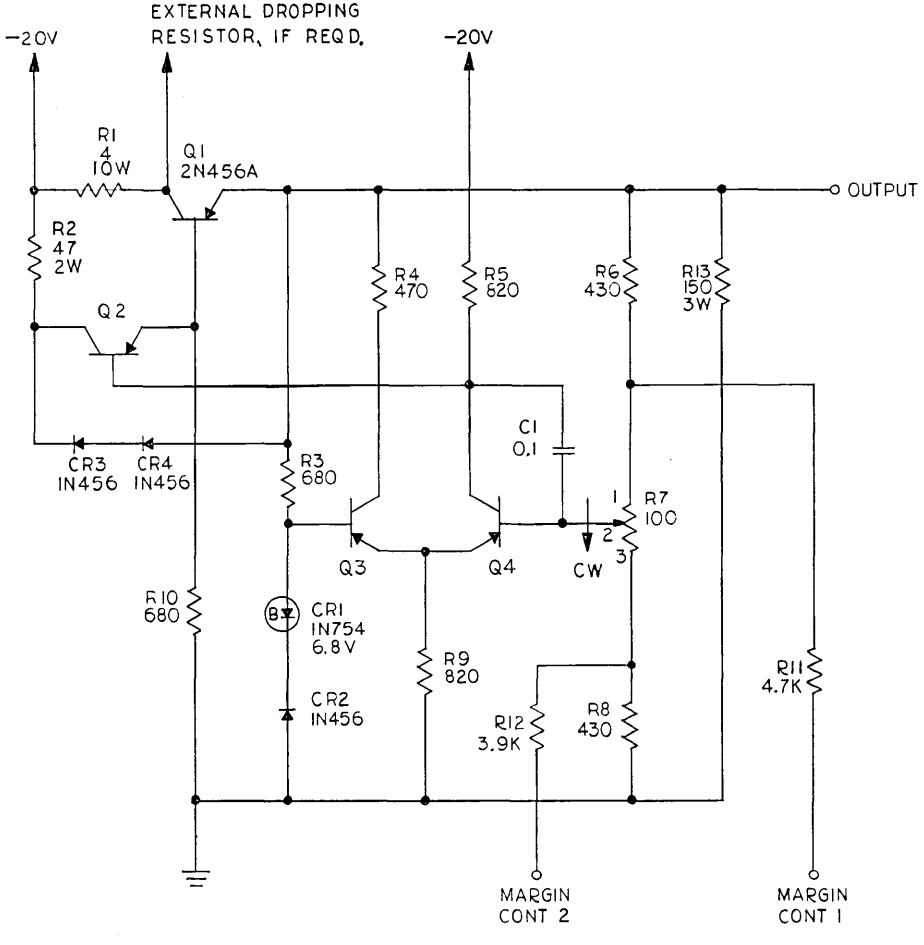
TITLE CKT. BOARD ASSY.
-15 VOLT REGULATOR 99E2

D | DRAWING NO. 200429 | REV D

SHEET 1 CONT. ON ——

NO.	E.C.O. NO.	REVISION	APP'D.	DATE
B		REDRAWN; R1 WAS 2Ω 10W BOARD WAS 99E1		5-2-63
C		PRODUCTION RELEASE	G.M.S	5-17-63





	C
DRAWING NUMBER	200426
REV.	C

4. ASSEMBLY DRAWING NO. 200429.
3. CAPAPACITOR VALUES IN μf ±10% 20V.
2. ALL RESISTOR VALUES IN OHMS ± 5% $\frac{1}{2}$ W.
1. ALL TRANSISTORS 2N1303.
NOTE: UNLESS OTHERWISE SPECIFIED.

	dp/p 3300	
NEXT ASS'Y.	USED ON	
DES. BY		
DR. BY	KUBOTA	12-9-62
CKD. BY		5-8-63
APP. BY		5-14-63
APP. BY		5-14-63

MATERIAL:

FINISH:

SCALE: NONE

TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL ±
FRACTION ±
ANGULAR ±
DIMENSIONS APPLY AFTER PLATING & HEAT TREATING

SHEET | OF |

data products corporation
CULVER CITY, CALIFORNIA

TITLE: SCHEMATIC
-15 VOLT REGULATOR
99E2

DRAWING NUMBER	REV.
C 200426	C

INSTRUCTIONS FOR UPDATING MANUALS IN ACCORDANCE WITH FIELD CHANGE ORDER NO. 2035 OR NO. 2036

When Data Products Corporation Field Change Order No. 2035 or No. 2036 is accomplished, Instruction Manual 201787-1, Revision B, is to be updated to Preliminary Revision C. To accomplish the updating, the following steps should be performed on each of the two manuals accompanying each SDS Buffered LINE/PRINTER.

1) On the title page:

   a) Write in ink, immediately above the words "REVISION B", the words "Preliminary Revision C".

   b) Line out the words "REVISION B".

   c) Write in ink, immediately above the date "JULY 30, 1964", the date "August 18, 1964".

   d) Line out the date "JULY 30, 1964".

2) Place supplied page iia immediately after the title page.

3) Replace the pages listed on page iia with those supplied.

PRELIMINARY REVISION C NOTE

This preliminary Revision C of Data Products Corporation Instruction Manual 201787-1 is issued in order to facilitate immediate incorporation of the following revised data:

Figure 5-18. MULTIVIBRATOR ADJUSTMENT Page 5 - 32

Logic Diagrams 1, 3, 23, 26, 31, 32, 33, 34, 35, 36, 39 and 41

Assembly Drawing 12M (replaces 12A)

Schematic Drawing 12M (replaces 12A)

Other material in the manual, affected by this revised data, will be updated and incorporated in the final release of Revision C of this manual.

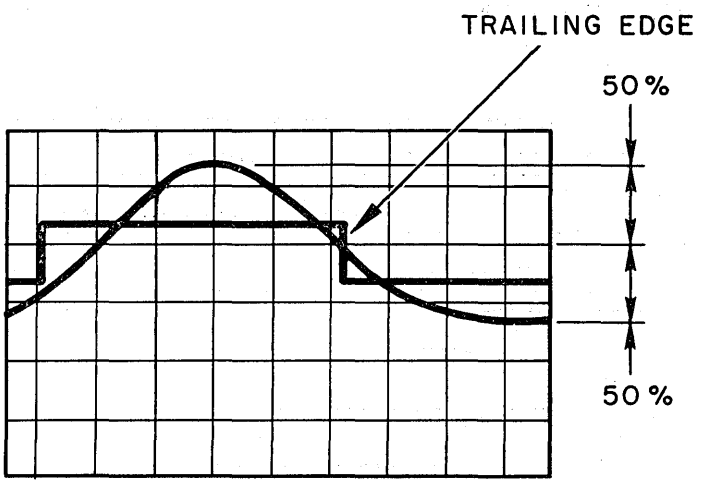


Figure 5-16. Photo-Diode Amplifier input/output Waveform

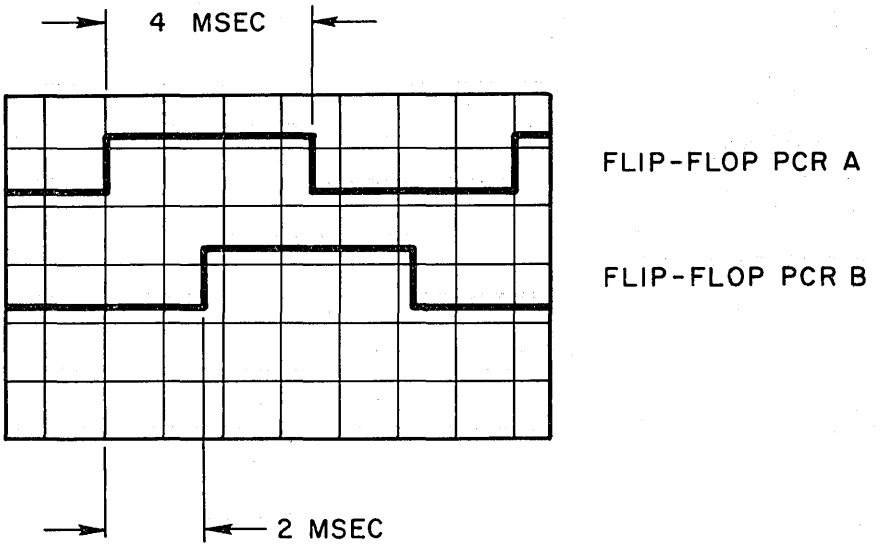


Figure 5-17. A-B Flip-Flop Outputs

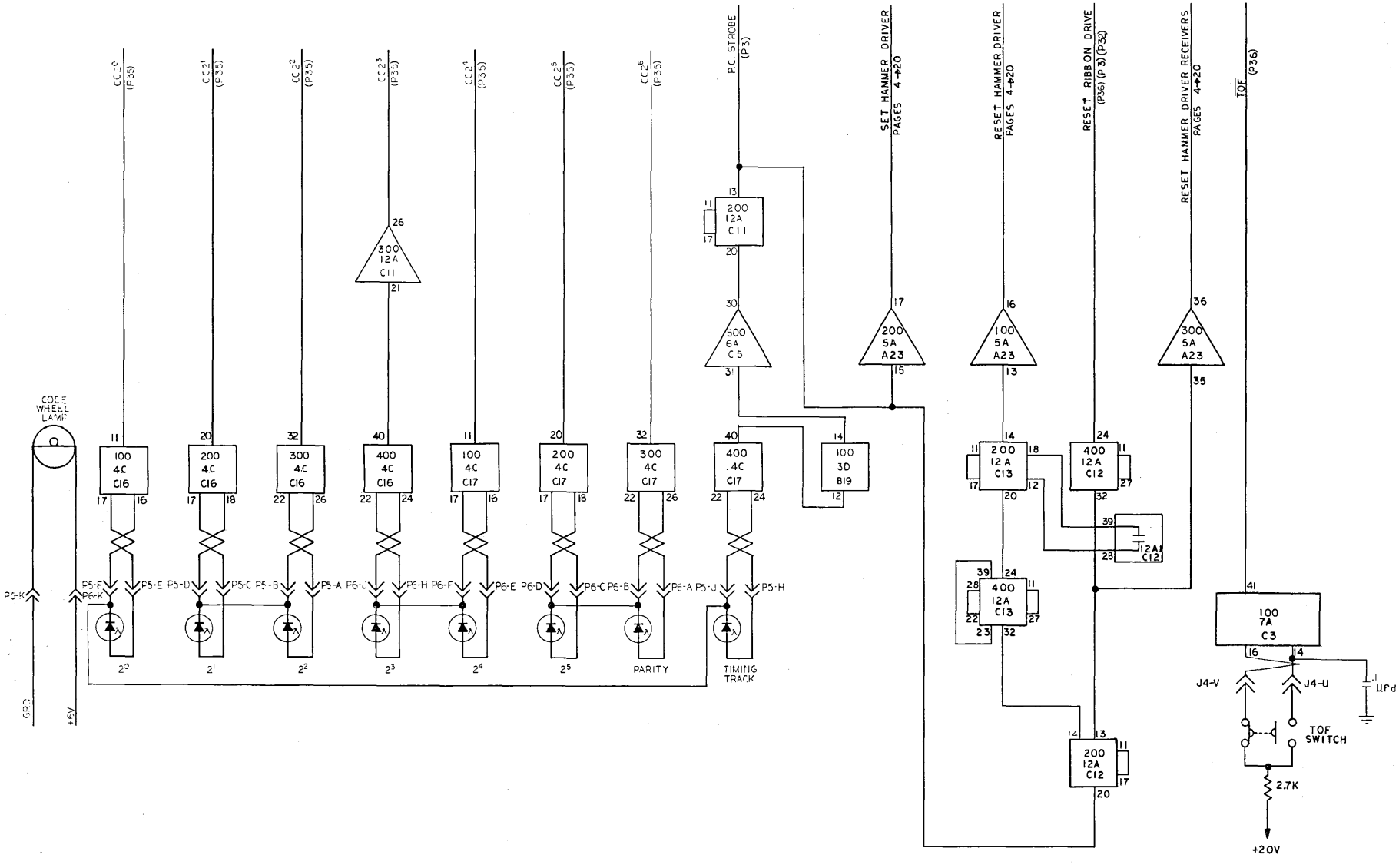
to acquire the pulse widths listed in figure 5-18. Adjust the multivibrator in sequence given.

Figure 5-18. MULTIVIBRATOR ADJUSTMENT

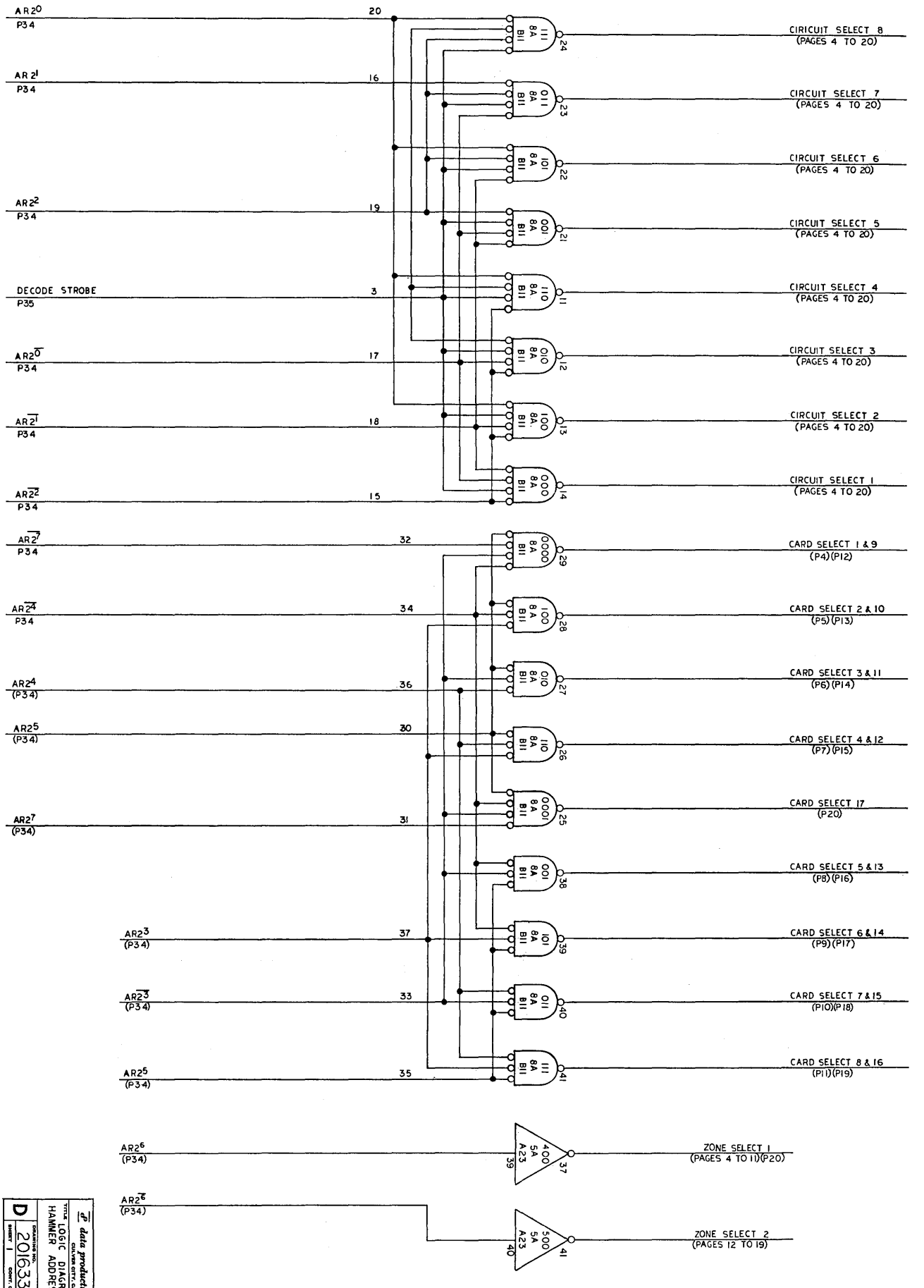
CIRCUIT LOCATION	TEST POINT	PULSE WIDTH	REMARKS
C11-200	C11-12	200 us ±5%	
C12-200	C12-13	200 us ±5%	
C12-400	C12-24	100 us ±5%	
C13-400	C13-24	1300 us ±5%	
C13-200	C13-14	400 us ±5%	
C14-400	C14-24	8 to 12 ms	Adjust while stepping paper
C14-200	C14-14	100 us ±5%	Adjust while stepping paper
C11-600	C11-34	1 us ±5%	Adjust while printing or stepping paper on command from external data source
C12-600	C12-34	1.5 us ±5%	
C14-600	C14-33	1 us ±5%	
C13-600	C13-34	1 us ±5%	
C11-400	C11-24	100 us ±5%	
D21-200	D21-13	100 us ±5%	
D21-400	D21-24	100 us ±5%	Adjust while stepping paper
D21-600	D21-34	1 us ±5%	

5-45. HAMMER BANK ADJUSTMENT

5-46. The hammer bank is aligned at the factory and no further adjustment should be necessary. However; if the hammer bank is loosened accidentally so that the gap is not set properly (refer



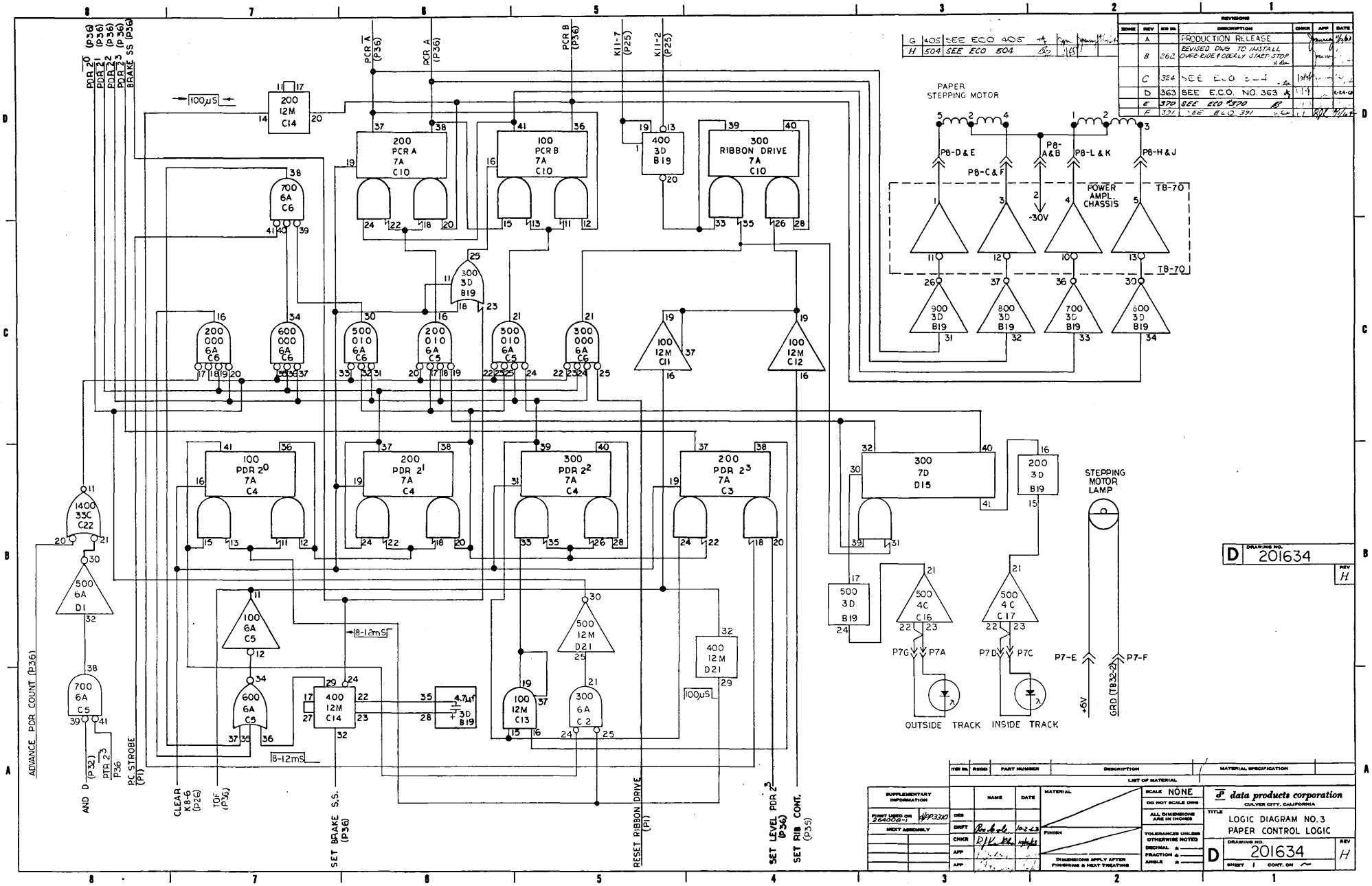
data products corporation — CULVER CITY, CALIFORNIA	
TITLE	LOGIC DIAGRAM-NO. 1 TIMING AND PHOTO DIODE AMP
D	DRAWING NO. 201632 — REV 0 — SHEET 1 — CONT. ON



data products corporation
CULVER CITY, CALIFORNIA

TITLE LOGIC DIAGRAM — NO.2
HAMMER ADDRESS DECODE

D | DRAWING NO. 201633 | SHEET 1 | CONT. ON | REV B



ZONE	REV	ECR NO.	DESCRIPTION	CHKD	APP	DATE
	A		PRODUCTION RELEASE			
	B	262	REVISED DWG TO INSTALL OVER-RIDE & CORRECTLY START-STOP			
	C	324	SEE ECO 324			
	D	363	SEE E.C.O. NO. 363			
	E	370	SEE ECO #370			
	F	391	SEE ECO 391			
	G	405	SEE ECO 405			
	H	504	SEE ECO 504			

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

LIST OF MATERIAL

SUPPLEMENTARY INFORMATION
FIRST USED ON 264008-1 #992330
NEXT ASSEMBLY

	NAME	DATE
DES		
DRFT		10-2-63
CHKR		
APP		
APP		

MATERIAL
FINISH
DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

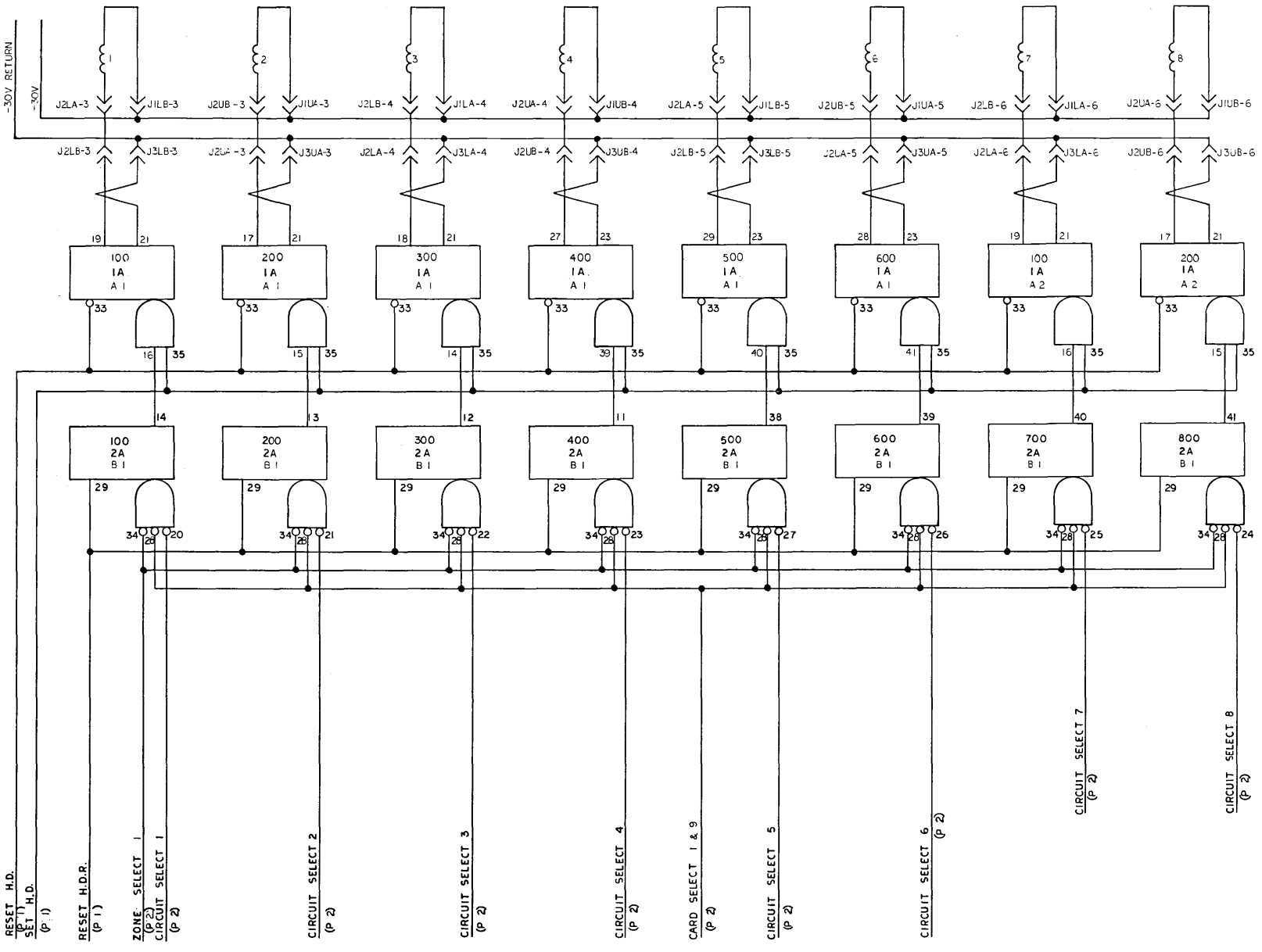
SCALE NONE
DO NOT SCALE DWG
ALL DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL ±
FRACTION ±
ANGLE ±

data products corporation
CULVER CITY, CALIFORNIA

TITLE
LOGIC DIAGRAM NO. 3
PAPER CONTROL LOGIC

DRAWING NO. D 201634 REV H
SHEET 1 CONT. ON

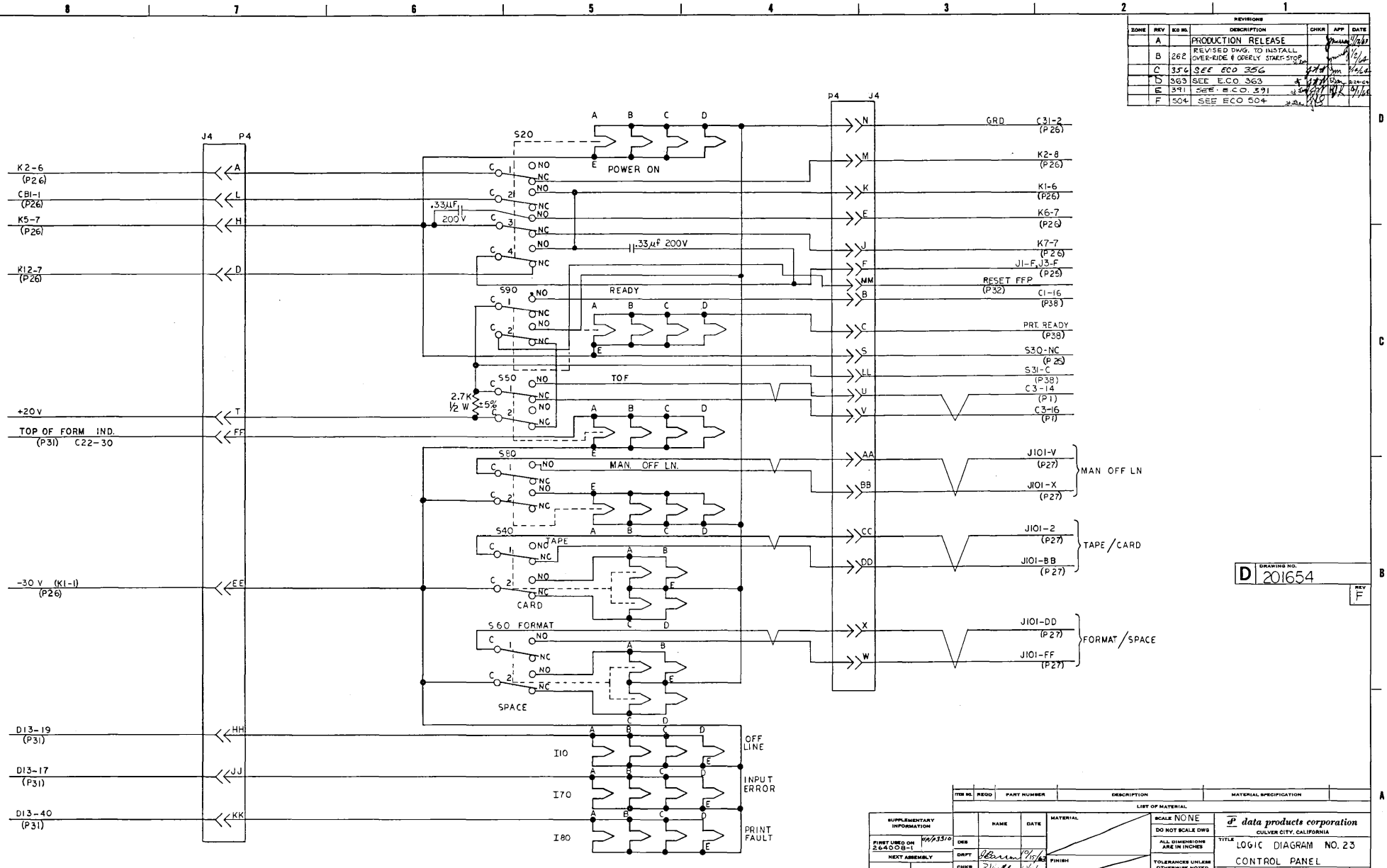
D 201634 REV H



data products corporation
CULVER CITY, CALIFORNIA

TITLE LOGIC DIAGRAM NO. 4
HAMMER DRS & REC 1 TO 8

D | DRAWING NO. 201635 | REV A
SHEET 1 | CONT. ON



ZONE	REV	ECO NO.	DESCRIPTION	CHKR	APP	DATE
	A		PRODUCTION RELEASE			11/1/62
	B	262	REVISED DWG. TO INSTALL OVER-RIDE & ODERLY START-STOP			11/1/62
	C	356	SEE ECO 356			9/4/63
	D	363	SEE E.C.O 363			9/24/63
	E	391	SEE E.C.O. 391			01/64
	F	504	SEE ECO 504			

1. ALL LAMPS ARE CHICAGO MINIATURE NO. 327 OR EQUIVALENT.

NOTES: UNLESS OTHERWISE SPECIFIED.

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

LIST OF MATERIAL

SUPPLEMENTARY INFORMATION

FIRST USED ON 264008-1 NEXT ASSEMBLY 10/23/62

	NAME	DATE
DES		
DRFT	H Barron	9/15/63
CHKR	R Klein	9/24/63
APP		11/4/63
APP		11/12/63

MATERIAL

FINISH

DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

SCALE NONE

DO NOT SCALE DWG

ALL DIMENSIONS ARE IN INCHES

TOLERANCES UNLESS OTHERWISE NOTED

DECIMAL ±

FRACTION ±

ANGLE ±

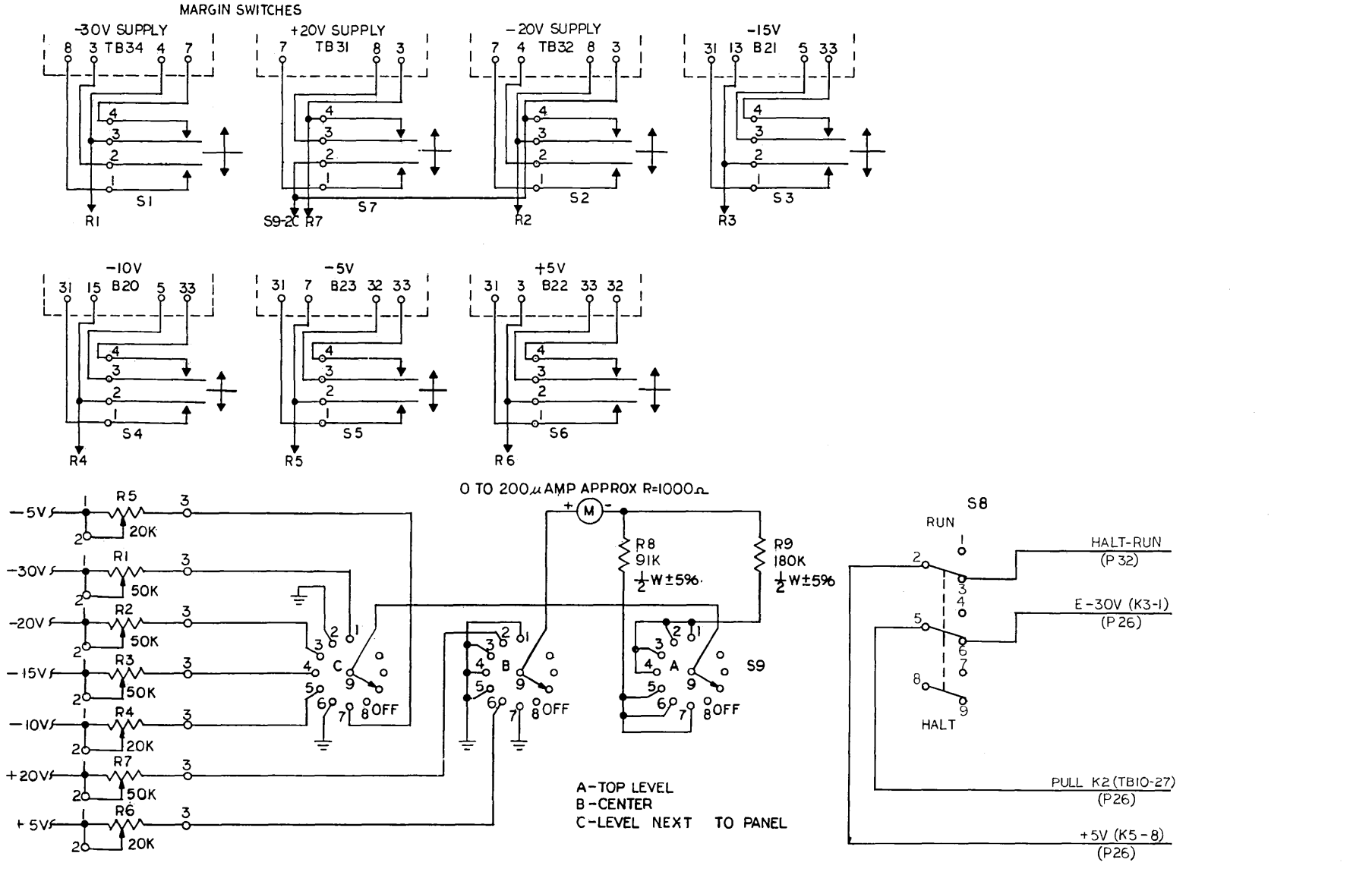
data products corporation
CULVER CITY, CALIFORNIA

TITLE LOGIC DIAGRAM NO. 23
CONTROL PANEL

D 201654 REV F

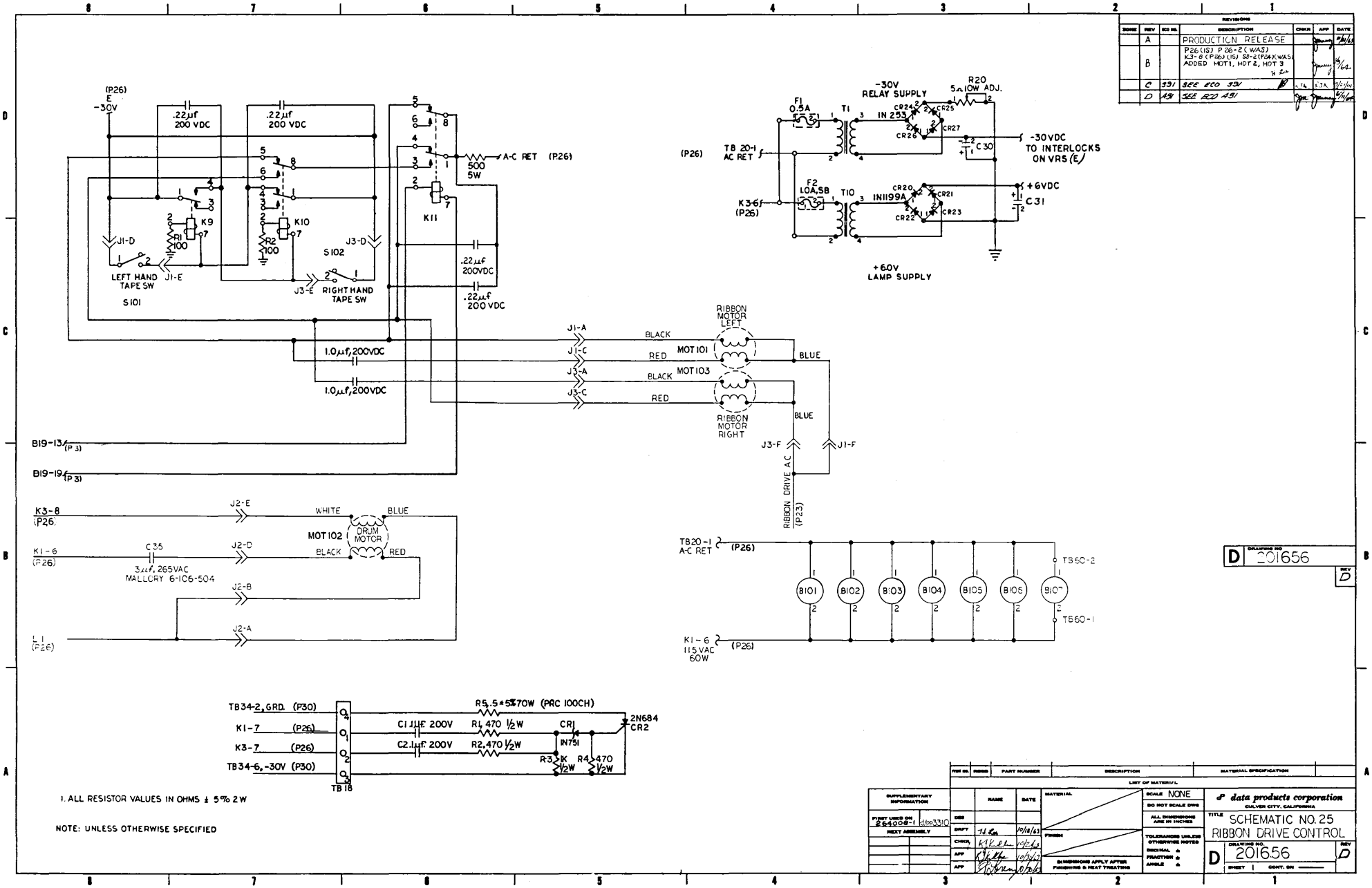
SHEET 1 CONT. ON

D 201654 REV F



1. ALL POTENTIOMETERS ±10% 1/2 WATT
NOTE: UNLESS OTHERWISE SPECIFIED

data products corporation CULVER CITY, CALIFORNIA			
TITLE: SCHEMATIC NO.24 MAINTENANCE PANEL			
	C	DRAWING NUMBER 201655	REV. B



ZONE	REV	ECO NO.	DESCRIPTION	CHKD	APP	DATE
	A		PRODUCTION RELEASE			9/6/62
	B		P26(1S) TO P26-2 (WAS) K3-8 (P26) (1S) TO 3B-2 (P24) (WAS) ADDED MOT1, MOT2, MOT3			9/6/62
	C	331	SEE ECO 331			9/14/62
	D	491	SEE ECO 491			6/6/63

1. ALL RESISTOR VALUES IN OHMS ± 5% 2W

NOTE: UNLESS OTHERWISE SPECIFIED

NAME	DATE
DRAFT	10/8/63
CHKD	10/8/63
APP	10/8/63
APP	10/8/63

SCALE NONE

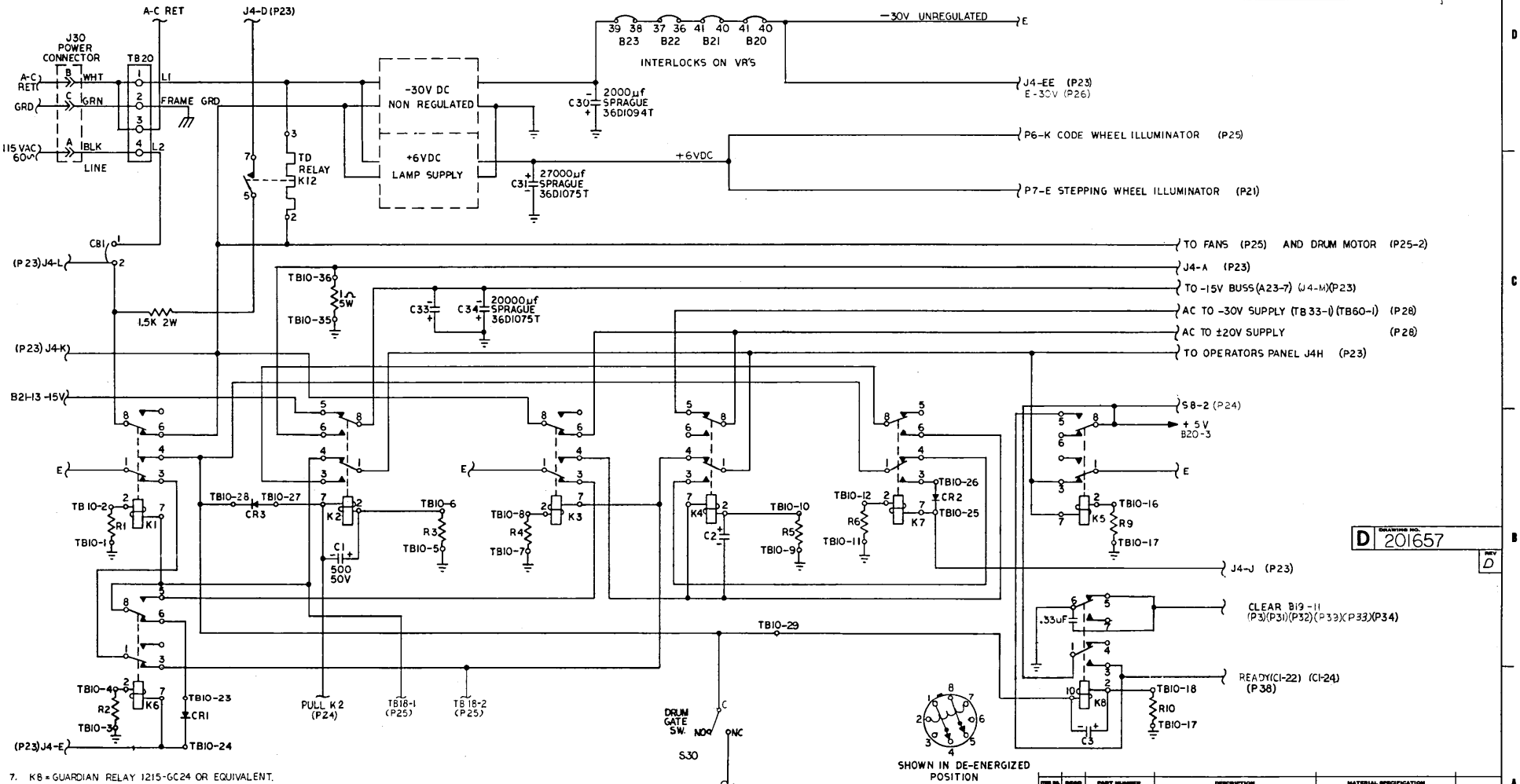
data products corporation
CULVER CITY, CALIFORNIA

TITLE SCHEMATIC NO. 25
RIBBON DRIVE CONTROL

DRAWING NO 201656 REV D

SHEET 1 CONT. ON

D 201656 REV D



7. K8 = GUARDIAN RELAY 1215-GC24 OR EQUIVALENT.
6. ALL RELAYS SHOWN IN SEQUENCED-UP STATE.
5. ALL DIODES IN92 OR EQUIVALENT.
4. ALL RELAYS ARE GUARDIAN 1215-G25, 24VDC OR OHMITE GPRTPX-69T.
3. ALL RESISTORS 100Ω ±5% 2W.
2. ALL CAPACITORS MALLORY, TYPE WP068 OR EQUIVALENT.
1. FIGURES IN DOTTED LINES SHOW FOR REF. ONLY AND ARE NOT LOCATED ON RELAY PANEL.

NOTES: UNLESS OTHERWISE SPECIFIED

ZONE	REV	ECO NO.	DESCRIPTION	CHKR	APP	DATE
	A		PRODUCTION RELEASE			11/1/63
	B	262	REVISED DWG TO INCL. A.C. OVERRIDE & CORRECTLY START-STOP			9/1/64
	C	391	SEE E.C.O 391			11/64
	D	509	SEE ECO 509			

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

LIST OF MATERIAL

SUPPLEMENTARY INFORMATION
FIRST USED ON 264008-1 dtd 9/3/64
NEXT ASSEMBLY

	NAME	DATE
DES		
DRFT	M. Lee	10/8/64
CHKR	R.K. Lee	11/4/64
APP		
APP		11/12/64

MATERIAL
FINISH
DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

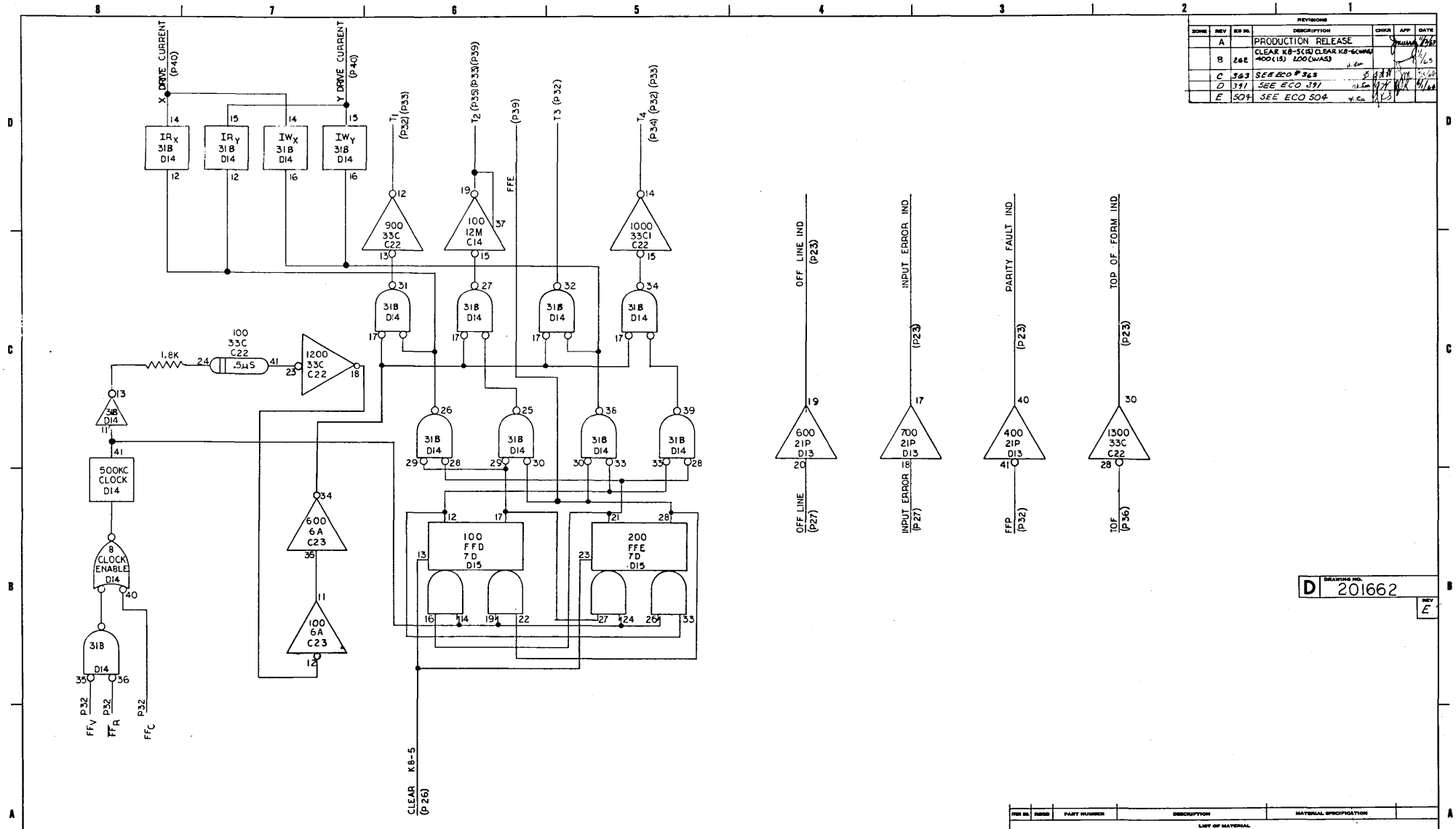
SCALE NONE
DO NOT SCALE DWG
ALL DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL ±
FRACTION ±
ANGLE ±

data products corporation
CULVER CITY, CALIFORNIA

TITLE
SCHEMATIC - NO. 26
POWER SEQUENCING-RELAY CONT.

D 201657 REV D
SHEET 1 CONT. ON ~

69-716 31 1/2



ZONE	REV	ECO NO.	DESCRIPTION	CHKR	APP	DATE
	A		PRODUCTION RELEASE			
	B	262	CLEAR K8-5(R) CLEAR K8-6(WAS) 400(15) 400(WAS)			
	C	363	SEE ECO # 363			
	D	391	SEE ECO 391			
	E	504	SEE ECO 504			

D 201662 REV E

ITEM NO.	QUAN	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

LIST OF MATERIAL

SUPPLEMENTARY INFORMATION

FIRST USED ON 2640008-1 #PP3310

NEXT ASSEMBLY

	NAME	DATE
DES		
DRFT	RON COLE	9-26-63
CHKR		10/2/63
APP		10/2/63
APP		11/12/63

MATERIAL

FINISH

DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

SCALE NONE

DO NOT SCALE DWG

ALL DIMENSIONS ARE IN INCHES

TOLERANCES UNLESS OTHERWISE NOTED

DECIMAL ±

FRACTION ±

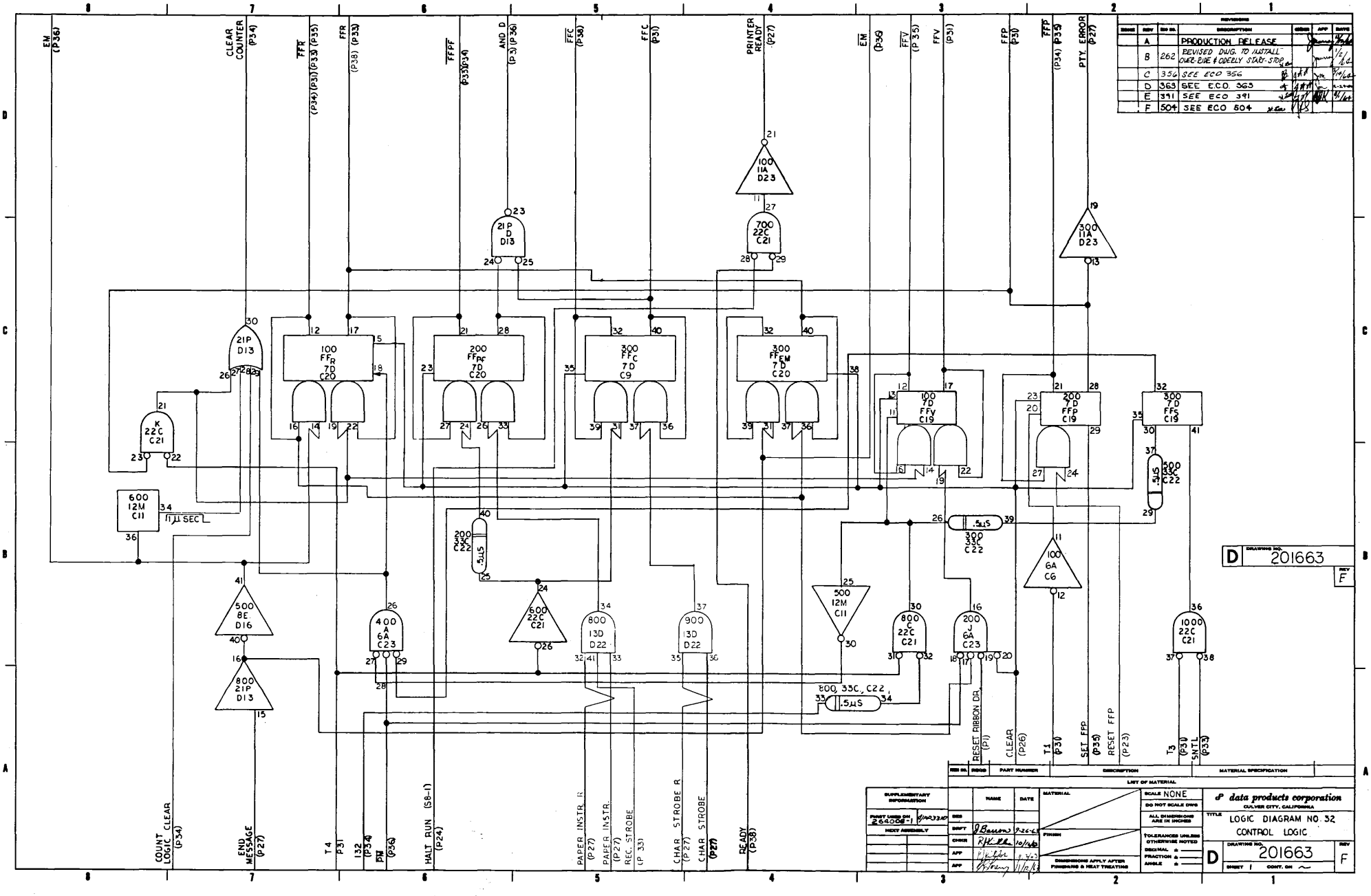
ANGLE °

data products corporation
CULVER CITY, CALIFORNIA

TITLE LOGIC DIAGRAM NO. 31
TIMING DISTRIBUTOR

D 201662 REV E

SHEET 1 SHT. OF ~



ZONE	REV	ECO NO.	DESCRIPTION	ORDER	APP	DATE
	A		PRODUCTION RELEASE			
	B	262	REVISED DWG. TO INSTALL OVER-TIME & ODELLY STAB-STOP			
	C	356	SEE ECO 356			
	D	363	SEE ECO 363			
	E	391	SEE ECO 391			
	F	504	SEE ECO 504			

D 201663 REV F

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

LIST OF MATERIAL

SUPPLEMENTARY INFORMATION		NAME	DATE
FIRST USED ON 264008-1	DES		
NEXT ASSEMBLY	DRFT	J Bauer	9-26-68
	CHKR	RH Miller	10/1/68
	APP		
	APP		

MATERIAL — FINISH — DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

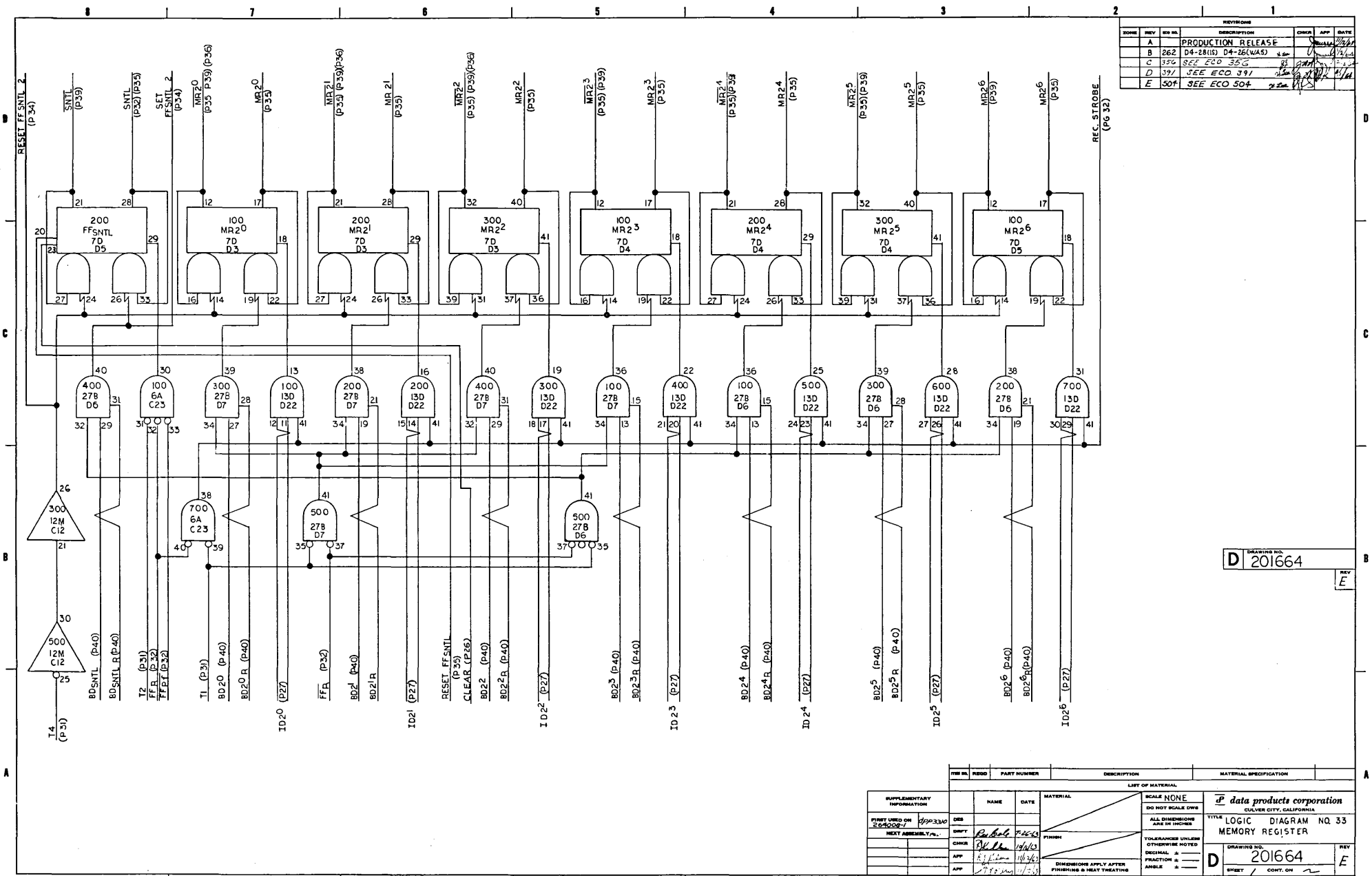
SCALE NONE — DO NOT SCALE DWG — ALL DIMENSIONS ARE IN INCHES — TOLERANCES UNLESS OTHERWISE NOTED: DECIMAL ±, FRACTION ±, ANGLE ±

data products corporation
CULVER CITY, CALIFORNIA

TITLE: LOGIC DIAGRAM NO. 32 CONTROL LOGIC

D 201663 REV F

SHEET 1 CONT. ON ~



ZONE	REV	ECO NO.	DESCRIPTION	CHKR	APP	DATE
	A		PRODUCTION RELEASE			
	B	262	D4-28(IS) D4-26(WAS)			
	C	356	SEE ECO 356			
	D	391	SEE ECO 391			
	E	504	SEE ECO 504			

D 201664 REV E

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

LIST OF MATERIAL

SUPPLEMENTARY INFORMATION		NAME	DATE
FIRST USED ON 264008-1 dpp3330	DES		
NEXT ASSEMBLY	DRFT	Richards	7-26-63
	CHKR	Richards	10/4/63
	APP	K J Lima	11/1/63
	APP	[illegible]	11/1/63

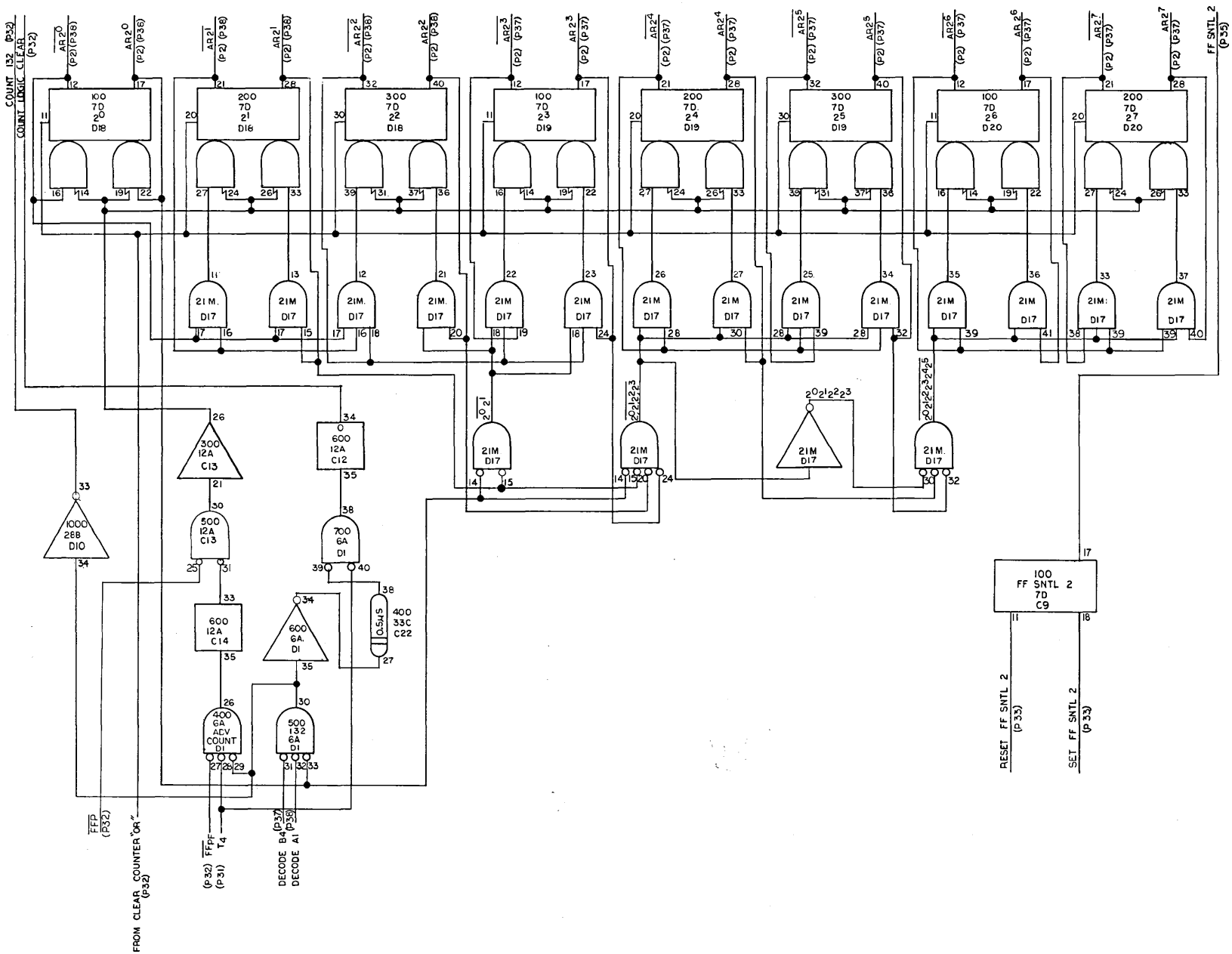
MATERIAL — FINISH — DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

SCALE NONE — DO NOT SCALE DWG — ALL DIMENSIONS ARE IN INCHES — TOLERANCES UNLESS OTHERWISE NOTED: DECIMAL ± — FRACTION ± — ANGLE ±

data products corporation
CULVER CITY, CALIFORNIA

TITLE: LOGIC DIAGRAM NO. 33
MEMORY REGISTER

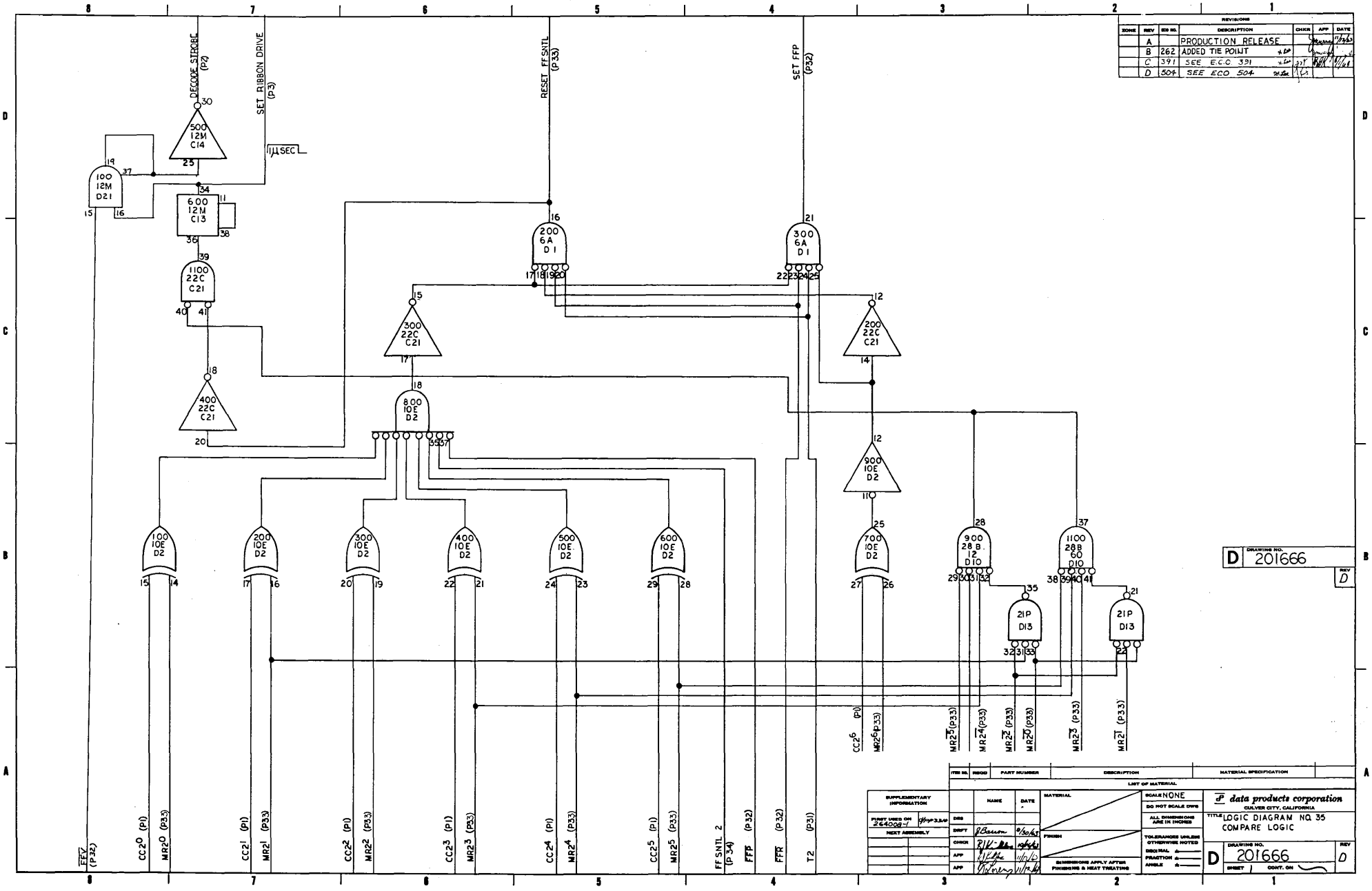
D 201664 REV E
SHEET 1 CONT. ON



data products corporation
CULVER CITY, CALIFORNIA

TITLE
LOGIC DIAGRAM NO. 34
ADDRESS REGISTER

D	DRAWING NO. 201665	REV C
	SHEET 1 CONT. ON ~	



REVISIONS					
ZONE	REV	ECO NO.	DESCRIPTION	CHKR	APP	DATE
	A		PRODUCTION RELEASE			
	B	262	ADDED TIE POINT			
	C	391	SEE E.C.O 391			
	D	504	SEE ECO 504			

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

LIST OF MATERIAL

SUPPLEMENTARY INFORMATION		NAME	DATE
FIRST USED ON 2640081 Mfgr 3340	DRS		
NEXT ASSEMBLY	DRFT	R Barron	8/30/67
	CHKR	RLK	10/6/67
	APP	RLK	11/10/67
	APP	[illegible]	11/28/67

MATERIAL — FINISH — DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

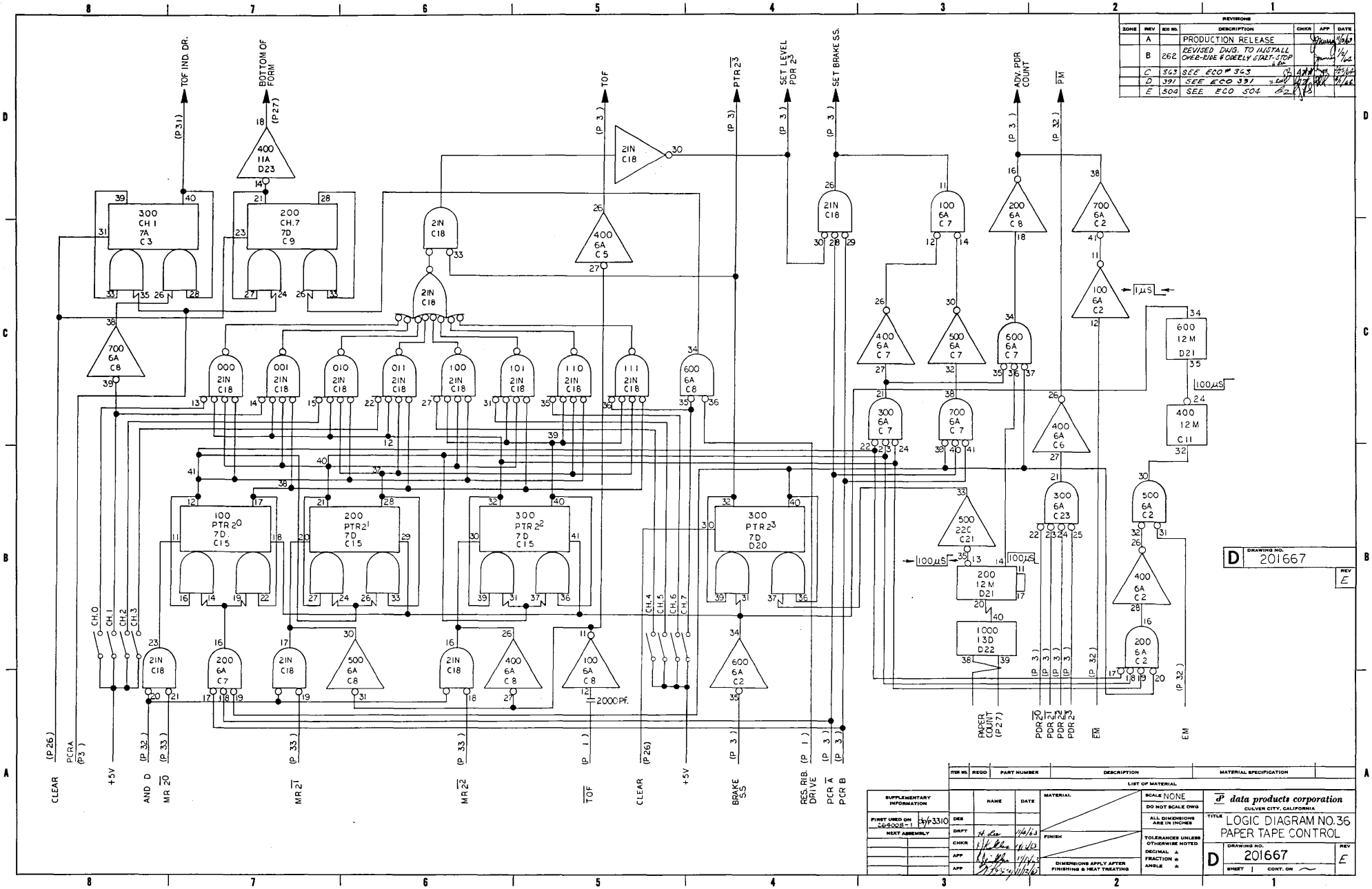
SCALE NONE — DO NOT SCALE DWG — ALL DIMENSIONS ARE IN INCHES — TOLERANCES UNLESS OTHERWISE NOTED: DECIMAL ±, FRACTION ±, ANGLE ±

data products corporation
CULVER CITY, CALIFORNIA

TITLE LOGIC DIAGRAM NO 35
COMPARE LOGIC

DRAWING NO. 201666 — REV D — SHEET 1 — CONT. ON

D DRAWING NO. 201666 REV D



REVISIONS					
ZONE	REV	ECO NO.	DESCRIPTION	CHKR	APP	DATE
	A		PRODUCTION RELEASE			11/26/62
	B	262	REVISED DWG. TO INSTALL OVER-RIDE & ORDERLY START-STOP			1/4/63
	C	363	SEE ECO # 363			4/24/63
	D	391	SEE ECO 391			9/1/63
	E	504	SEE ECO 504			8/2/65

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

LIST OF MATERIAL

SUPPLEMENTARY INFORMATION		NAME	DATE
FIRST USED ON 64008-1	DES		
NEXT ASSEMBLY	DRFT	H. Lau	11/6/62
	CHKR		11/9/62
	APP		11/14/62
	APP		11/26/62

MATERIAL — FINISH — DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

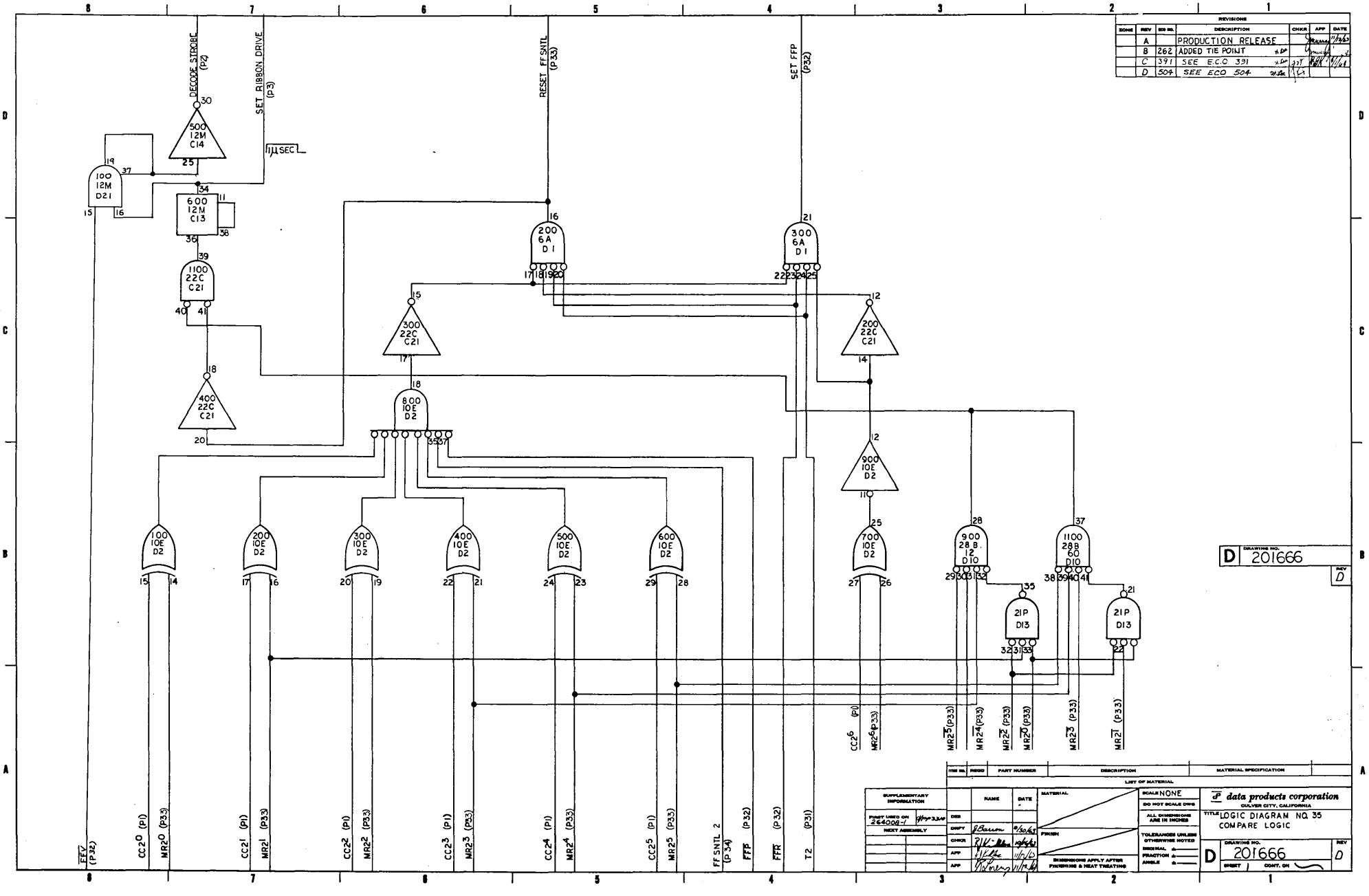
SCALE NONE
DO NOT SCALE DWG
ALL DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL ±
FRACTION ±
ANGLE ±

data products corporation
CULVER CITY, CALIFORNIA

TITLE LOGIC DIAGRAM NO. 36
PAPER TAPE CONTROL

D DRAWING NO. 201667 REV E
SHEET 1 CONT. ON ~

D DRAWING NO. 201667 REV E



ZONE	REV	ECO NO.	DESCRIPTION	CHKR	APP	DATE
	A		PRODUCTION RELEASE			
	B	262	ADDED TIE POINT			
	C	391	SEE E.C.O 391			
	D	504	SEE ECO 504			

ITEM NO.	QTY	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

LIST OF MATERIAL

	NAME	DATE
DES		
DRFT	J Barron	8/30/67
CHKR	R W Miller	10/6/67
APP	W Kelly	11/1/67
APP	W Mooney	11/2/67

SUPPLEMENTARY INFORMATION
FIRST USED ON 2640081-1 Rev 334
NEXT ASSEMBLY

MATERIAL
FINISH
DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

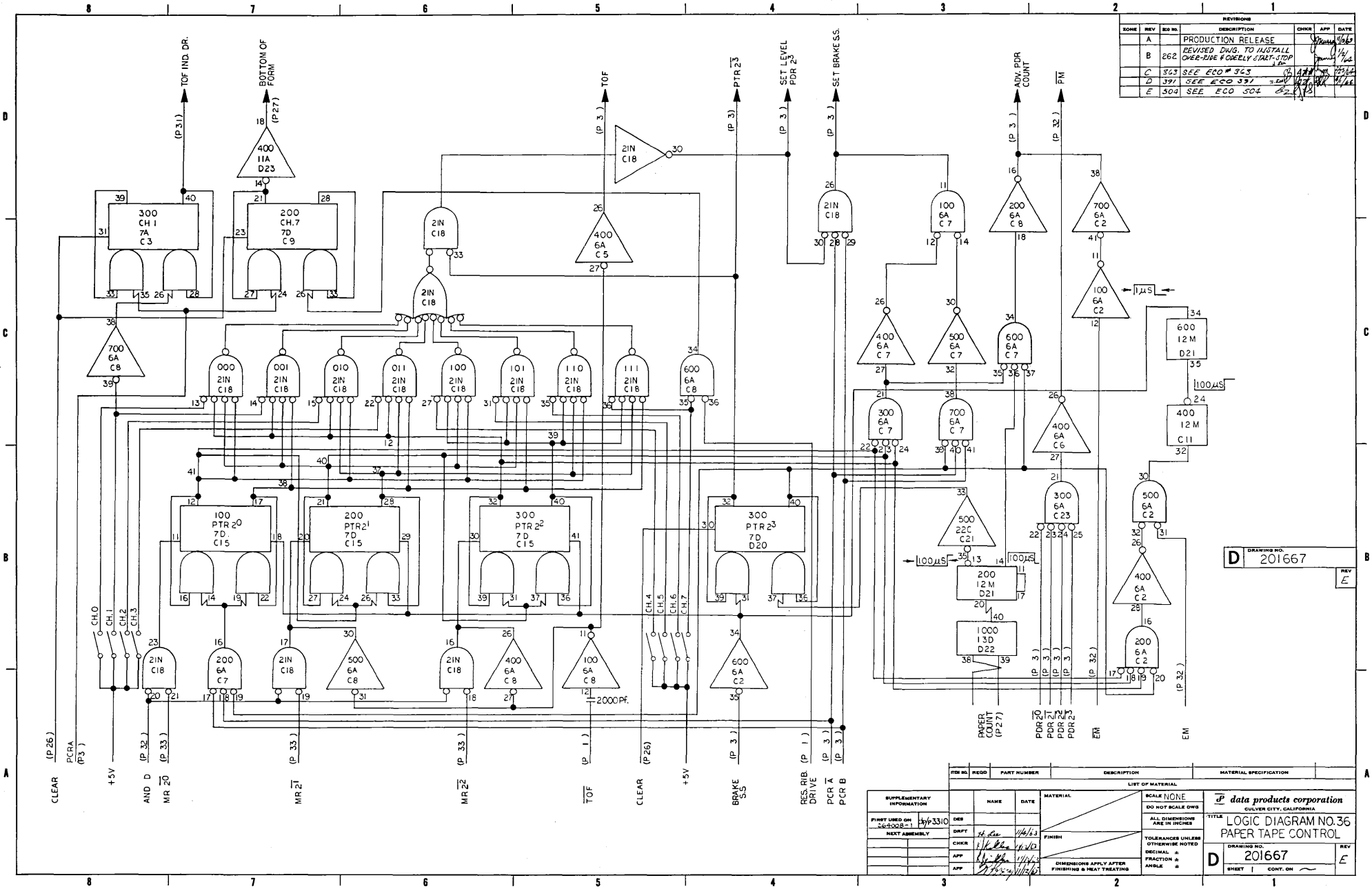
SCALE NONE
DO NOT SCALE DWG
ALL DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE NOTED
ORIGINAL ±
FRACTION ±
ANGLE ±

data products corporation
CULVER CITY, CALIFORNIA

TITLE LOGIC DIAGRAM NO. 35
COMPARE LOGIC

D DRAWING NO. 201666 REV D
SHEET 1 CONT. ON

D DRAWING NO. 201666 REV D



REVISIONS						
ZONE	REV	ECO NO.	DESCRIPTION	CHKR	APP	DATE
	A		PRODUCTION RELEASE			11/26/63
	B	262	REVISED DWG. TO INSTALL OVER-RIDE & ORDERLY START-STOP			1/3/64
	C	363	SEE ECO # 363			12/3/64
	D	391	SEE ECO 391			11/1/66
	E	504	SEE ECO 504			

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

LIST OF MATERIAL

SUPPLEMENTARY INFORMATION		NAME	DATE
FIRST USED ON 264008-1	DES		
NEXT ASSEMBLY 30/P 3310	DRFT	H. Lee	11/6/63
	CHKR		11/6/63
	APP		11/6/63
	APP		11/12/63

MATERIAL — FINISH — DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

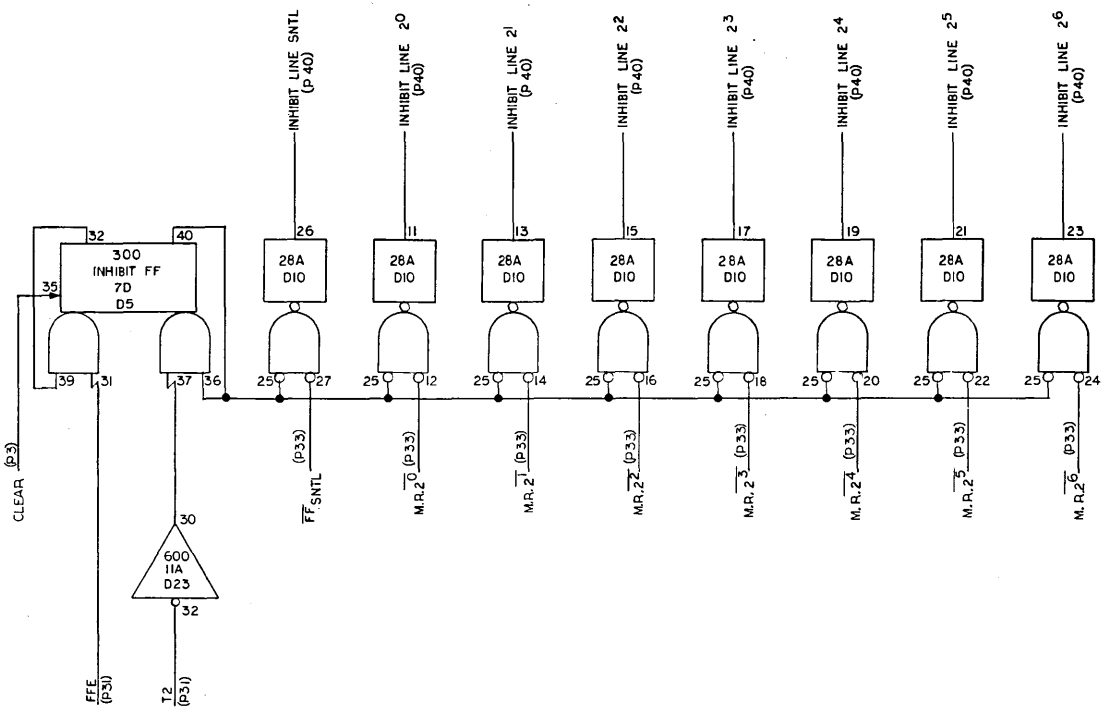
SCALE NONE
DO NOT SCALE DWG
ALL DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL ±
FRACTION ±
ANGLE ±

data products corporation
CULVER CITY, CALIFORNIA

TITLE LOGIC DIAGRAM NO. 36
PAPER TAPE CONTROL

D DRAWING NO. 201667 REV E
SHEET 1 CONT. ON ~

D DRAWING NO. 201667 REV E

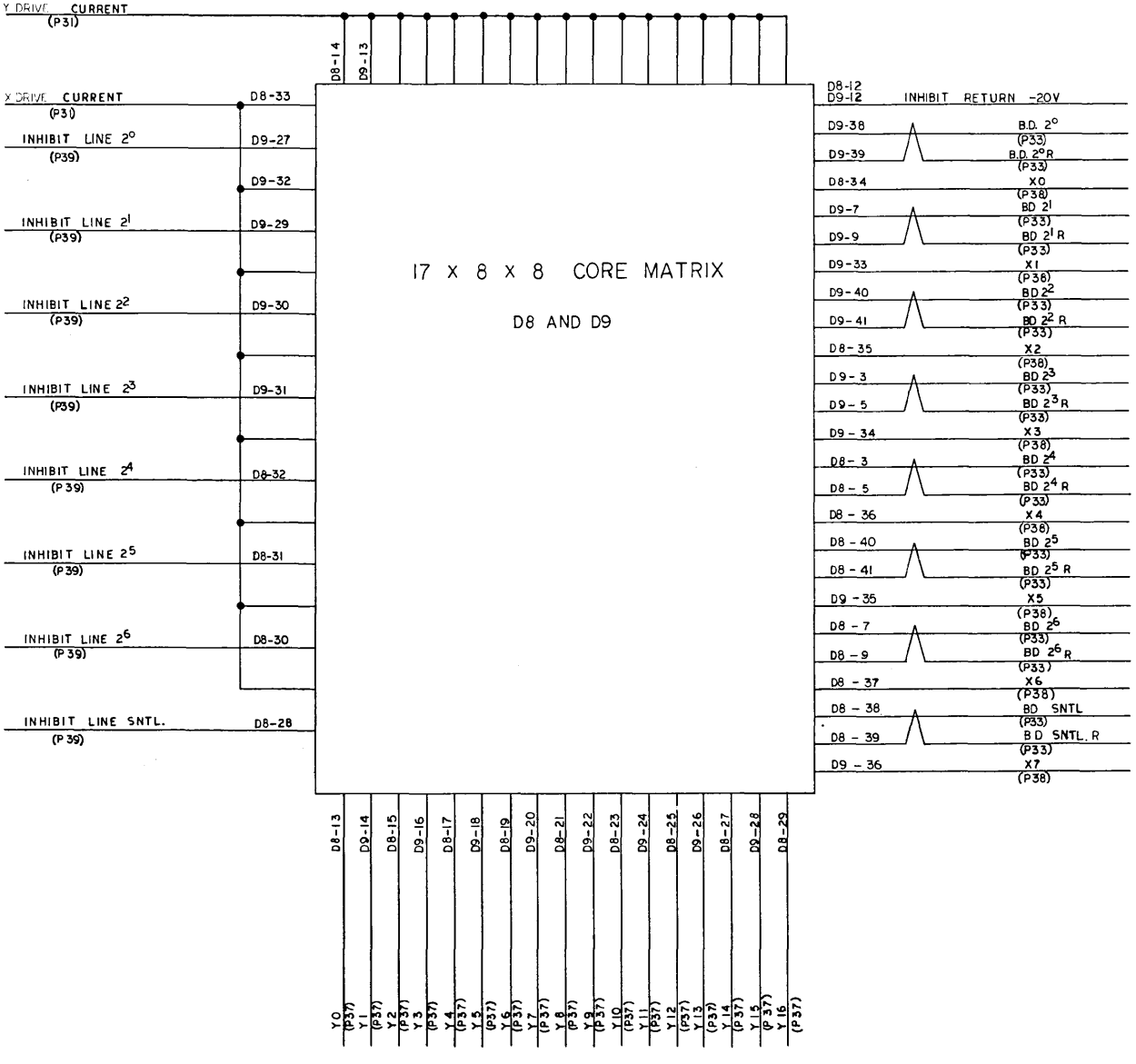


data products corporation
CULVER CITY, CALIFORNIA

TITLE
LOGIC DIAGRAM NO. 39
INHIBIT DRIVE

D | DRAWING NO. 201670 | REV A

SHEET 1 CONT. ON ~



data products corporation
CULVER CITY, CALIFORNIA

TITLE LOGIC DIAGRAM NO. 40
CORE MATRIX

D | DRAWING NO. 201671 | REV A

SHEET 1 CONT. ON

REVISIONS					
ZONE	REV	ECO NO.	DESCRIPTION	CHKR	APP	DATE
	A		PRODUCTION RELEASE			12/7/62
	B	324	REVISED PAGE NO., PIN NO ON CARD 19 (B CAGE) (C WAS 48 ON CARD 16&17 (C CAGE) ON SHEET 2			6/6/63
	C	356	SEE ECO #356			8/6/63
	D	363	SEE ECO #363			8/16/63
	E	370	SEE ECO #370			9/13/63
	F	391	SEE ECO 391			11/6/63
	G	443	SEE ECO 443 RC			1/31/64
	H	504	SEE ECO 504			

A

CARDS 1 THRU 22		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CKT.	OUTPUT PIN	1A	1A	1A	1A	1A	1A	1A	1A	1A	1A	1A	1A	1A	1A	1A	1A	1A	1A	1A	1A	1A	1A	5A
100	19	HMR. 1-P4	7-P4	13-P5	19-P6	25-P7	31-P7	37-P8	43-P9	49-P10	55-P10	61-P11	67-P12	73-P13	79-P13	85-P14	91-P15	97-P16	103-P16	109-P17	115-P18	121-P19	127-P19	P1-16
200	17	2-P4	8-P4	14-P5	20-P6	26-P7	32-P7	38-P8	44-P9	50-P10	56-P10	62-P11	68-P12	74-P13	80-P13	86-P14	92-P15	98-P16	104-P16	110-P17	116-P18	122-P19	128-P19	P1-17
300	18	3-P4	9-P5	15-P5	21-P6	27-P7	33-P8	39-P8	45-P9	51-P10	57-P11	63-P11	69-P12	75-P13	81-P14	87-P14	93-P15	99-P16	105-P17	111-P17	117-P18	123-P19	129-P20	P1-36
400	27	4-P4	10-P5	16-P5	22-P6	28-P7	34-P8	40-P8	46-P9	52-P10	58-P11	64-P11	70-P12	76-P13	82-P14	88-P14	94-P15	100-P16	106-P17	112-P17	118-P18	124-P19	130-P20	P2-37
500	29	5-P4	11-P5	17-P6	23-P6	29-P7	35-P8	41-P9	47-P9	53-P10	59-P11	65-P12	71-P12	77-P13	83-P14	89-P15	95-P15	101-P16	107-P17	113-P18	119-P18	125-P19	131-P20	P2-41
600	28	6-P4	12-P5	18-P6	24-P6	30-P7	36-P8	42-P9	48-P9	54-P10	60-P11	66-P12	72-P12	78-P13	84-P14	90-P15	96-P15	102-P16	108-P17	114-P18	120-P18	126-P19	132-P20	

B

CARDS 1 THRU 10, 12 THRU 18		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CKT.	OUTPUT PIN	2A	2A	2A	2A	2A	2A	2A	2A	2A	2A	8A	2A	2A	2A	2A	2A	2A	2A	3D	99D	99AE	99B	99A
100	14	HMR. 1-P4	9-P5	17-P6	25-P7	33-P8	41-P9	49-P10	57-P11	65-P12	73-P13	P2-24	81-P14	89-P15	97-P16	105-P17	113-P18	121-P19	129-P20	P1-14	-10V PIN 15	-15V PIN 13	+5V PIN 3	-5V PIN 7
200	13	2-P4	10-P5	18-P6	26-P7	34-P8	42-P9	50-P10	58-P11	66-P12	74-P13	23 22	82-P14	90-P15	98-P16	106-P17	114-P18	122-P19	130-P20	P3-36				
300	12	3-P4	11-P5	19-P6	27-P7	35-P8	43-P9	51-P10	59-P11	67-P12	75-P13	21 11	83-P14	91-P15	99-P16	107-P17	115-P18	123-P19	131-P20	P3-25				
400	11	4-P4	12-P5	20-P6	28-P7	36-P8	44-P9	52-P10	60-P11	68-P12	76-P13	12 13	84-P14	92-P15	100-P16	108-P17	116-P18	124-P19	132-P20	P3-13				
500	38	5-P4	13-P5	21-P6	29-P7	37-P8	45-P9	53-P10	61-P11	69-P12	77-P13	14 29	85-P14	93-P15	101-P16	109-P17	117-P18	125-P19		P3-17				
600	39	6-P4	14-P5	22-P6	30-P7	38-P8	46-P9	54-P10	62-P11	70-P12	78-P13	28 27	86-P14	94-P15	102-P16	110-P17	118-P18	126-P19		P3-30				
700	40	7-P4	15-P5	23-P6	31-P7	39-P8	47-P9	55-P10	63-P11	71-P12	79-P13	26 25	87-P14	95-P15	103-P16	111-P17	119-P18	127-P19		P3-36				
800	41	8-P4	16-P5	24-P6	32-P7	40-P8	48-P9	56-P10	64-P11	72-P12	80-P13	38 33 P2-40	88-P14	96-P15	104-P16	112-P17	120-P18	128-P19		P3-37				
																				P3-26				

D 201822 REV H

5. NUMBERS FOLLOWING PAGE NUMBERS ARE OUTPUT PINS FOR THAT CKT.
4. A NUMBER PRECEDED BY P INDICATES PAGE AND NUMBER.
3. BLOCKS MARKED THRU INDICATE NO CKT. ON CARD.
2. CARD 11 ON B CAGE HAS ONLY ONE CKT. BUT 16 OUTPUT PINS.
1. P1, P2, ETC. INDICATE PAGE NO., CKT. IS LOCATED ON.

NOTE: UNLESS OTHERWISE SPECIFIED

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

LIST OF MATERIAL

SUPPLEMENTARY INFORMATION: FIRST USED ON 22500E-1 NEXT ASSEMBLY 22P3310

	NAME	DATE
DES		
DRFT	H. Sears	11/27/62
CHKR	J. Evans	12/7/62
APP	W. K. Klee	12/7/62
APP	R. K. Long	12/7/62

MATERIAL | FINISH | DIMENSIONS APPLY AFTER PLATING & HEAT TREATING

SCALE NONE — DO NOT SCALE DWG — ALL DIMENSIONS ARE IN INCHES — TOLERANCES UNLESS OTHERWISE NOTED: DECIMAL ± , FRACTION ± , ANGLE ±

data products corporation, CULVER CITY, CALIFORNIA

TITLE: LOGIC DIAGRAM NO.41 CARD LOCATION

D 201822 REV H — SHEET 1 CONT. ON 2

REVISIONS					
ZONE	REV	ECO NO.	DESCRIPTION	CHKR	APP	DATE
			SEE SHEET 1			

C

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
21V	6A	7A	7A	6A	6A	6A	6A	7D	7A	12M	12M	12M	12M	7D	4C	4C	21N	7D	7D	22C	33C	6A
P38-	P36-11	P1-41	P3-41/36	P3-11	P32-11	P36-11	P36-11	SNTL2 P34-17	P3-41/36	P3-19	P3-19	P3-19	P31-19	P36-12/17	P1-11	P1-11	P36-30	P32-17	P32-12		P31-41	P31-11
	P36-16	P3-32/38	P3-37/38	P3-16	P3-16	P36-16	P36-16	P3621/28	P3-37/38	P1-13	P1-13/14	P1-14	P3-14	P36-21/28	P1-20	P1-20	P36-26	P32-21/28	P32-21/28	P35-12	P32 40	P32-16
	P3-21	P3639/40	P3-39/40	P3-21	P3-21	P36-21	P34-21	P32-32/40	P3-39/40	P1-26	P33-26	P34-26		P36-32/40	P1-32	P1-32	P36-16	P32-32	FFEM P32-32/40	P32-21	P32-39	P36-31
	P36-26			P36-26	P36-26	P36-26	P36-26			P36-24	P1-24	P1-24	P3-29/24		P1-40	P1-40	P36-17			P35-15	P34-38	P32-26
	P36-30			P1-30	P3-30	P36-30	P36-30			P32-25	P33-30	P34-30	P35-30		P3-21	P3-21	P36-23			P35-18	P32-37	P33-30
	P36-34			P3-34	P3-34	P36-34	P36-34			P32-34	P34-34	P35-34	P34-33							P36-33		P31-34
	P36-38			P3-38	P3-38	P36-38	P36-38													P32-24	"	P33-38
																				P32-27	P32-34	
																				P32-30	P31-12	
																				P32-36	P31-14	
																				P35-39	P31-18	
																					P31-30	
																					P3-11	

D

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
6A	10E	7D	7D	7D	27B	27B	CORE	ARRAY	28B	29A	29A	21P	31B	7D	8E	21M	7D	7D	7D	12M	13D	11A
P32-11	P35	MR2^{0} P33-12/17	MR2^{3} P33-12/17	MR2^{6} P33-12/17	P33-36	P33-36			P39-23	P37-16	P37-16	P37-36	IRX P31-14	FFD P31-12/17	P37-21	P34-11	P34-12/17	P34-12/17	P34-12/17	P35-19	P33-13	P32-21
P35-16	P35	MR2^{1} P33-21/28	MR2^{4} P33-21/26	SNTL P33-21/28	P33-38	P33-38			P39-21	P37-17	P37-17	P37-38	IRY P31-15	FFE P31-21/28	P37-19	P34-13	P34-21/28	P34-21/28	P34-21/28	P3613/14	P33-16	P32-20
P35-21	P35	MR2^{2} P33-32/40	MR2^{5} P33-32/40	INHIBIT P39-32/40	P33-39	P33-39			P39-19	P37-13	P37-13	P32-30	IWX P31-14	P3-32/40	P37-12	P34-12	P34-32/40	P34-32/40	P36 32/40		P33-19	P32-19
P34-26	P35				P33-40	P33-40			P39-17	P37-15	P37-15	P31-40	IWY P31-15		P32-38	P34-21				P3-29	P33-22	P36-18
P3 -30	P35				P33-41	P33-41			P39-15	P37-22	P37-22	P35-21	CLOCK P31-41		P32-41	P34-22				P3-30	P33-25	
P34-34	P35						P40 MATRIX	P40 MATRIX	P39-13	P37-19	P37-19	P31-19	P31-(13)		P32-20	P34-23				P36-34	P33-28	P39-30
P34-38	P35-25								P39-11	P37-12	P37-12	P31-17	P31-31		P32-11	P34-26					P33-31	
	P35-18								P39-26	P38-27	P38-27	P32-16	P31-27		P35-34	P34-27					P32-34	
	P35-12								P35-28	P38-35	P38-35	P37-14	P31-32		P37-35	P34-25					P32-37	
									P34-33	P38-40	P38-40	P32-23	P31-34		P37-37	P34-34					P36-40	
									P35-37	P38-37	P38-37	P35-35	P31-38		P37-36	P34-35						
													P31-25		P38-16	P34-36						
													P31-26		P38-23	P34-33						
													P31-39		P38-24	P34-37						
															P38-25							

D DRAWING NO. 201822 REV H

ITM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION
			LIST OF MATERIAL	

SUPPLEMENTARY INFORMATION		NAME	DATE
FIRST USED ON P64009-1 10/1/3310	DES		
NEXT ASSEMBLY	DRFT		
	CHKR		
	APP		
	APP		

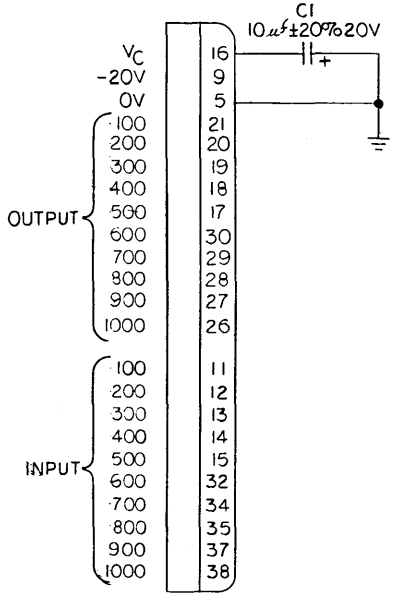
MATERIAL / FINISH / DIMENSIONS APPLY AFTER FINISHING & HEAT TREATING

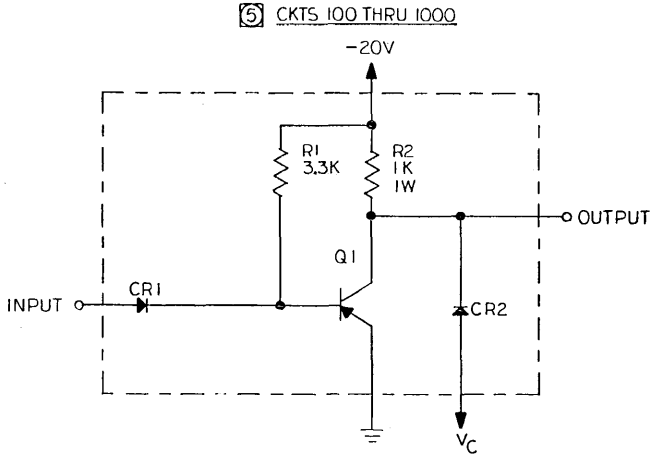
SCALE NONE — DO NOT SCALE DWG — ALL DIMENSIONS ARE IN INCHES — TOLERANCES UNLESS OTHERWISE NOTED: DECIMAL ±, FRACTION ±, ANGLE ±

data products corporation, CULVER CITY, CALIFORNIA

TITLE: LOGIC DIAGRAM NO. 41 CARD LOCATION

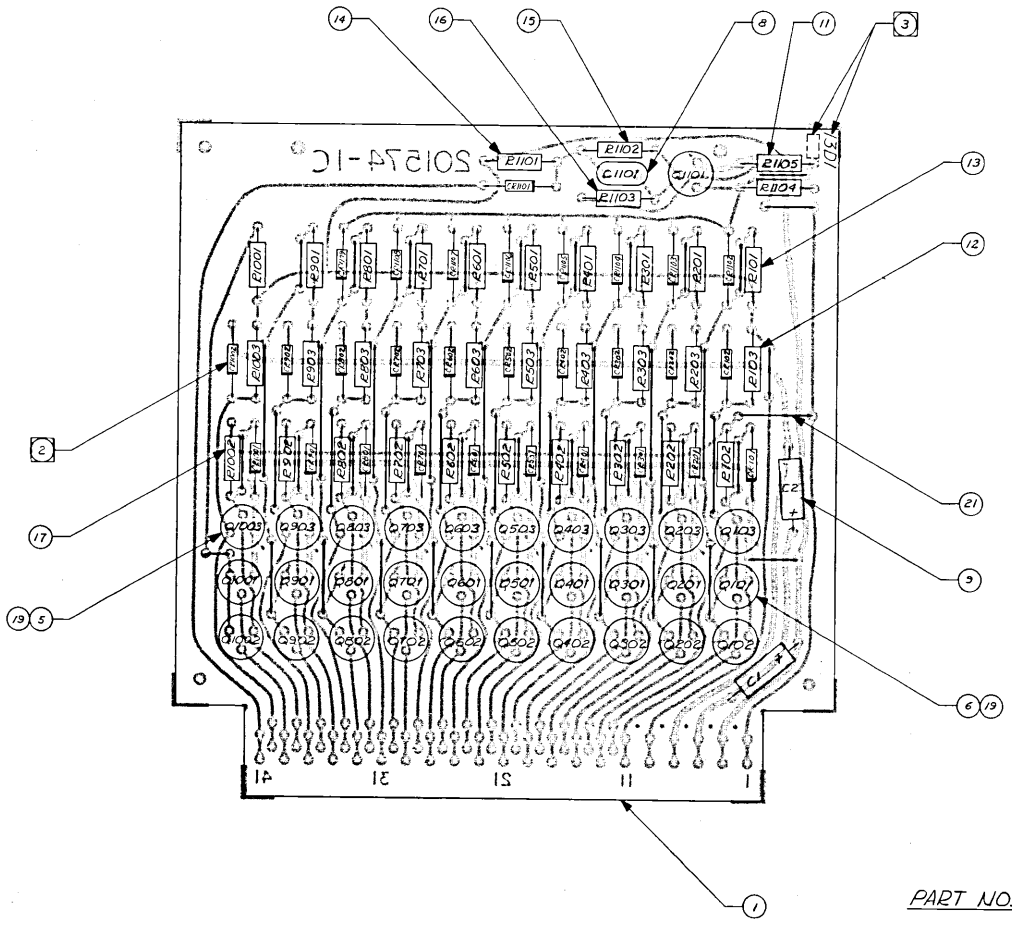
D DRAWING NO. 201822 REV H SHEET 2 CONT. ON ~





5 REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE PART DESIGNATION WITH THE SUBASSEMBLY DESIGNATION
4. ASSEMBLY DRAWING NO. 200223
3. ALL TRANSISTORS 2N1303
2. ALL DIODES CGD1307
1. ALL RESISTOR VALUES IN OHMS ± 5% $\frac{1}{2}$ W
NOTE: UNLESS OTHERWISE SPECIFIED

data products corporation CULVER CITY, CALIFORNIA	
TITLE:	SCHEMATIC OUTPUT DRIVER I IAI
C	DRAWING NUMBER 200220 REV. B



PART NO. 201575-1

22				
21	A/R		WIRE (22GA.)	
20				
19	31	RC-05090-IN	TRANSIPAD (ROBINSON)	
18				

17	10	EB8225	RESISTOR 8.2K 1/2W ±5% (A.B.)	R102 - R1002
16	1	EB1535	15K	R1103
15	1	EB1825	1.8K	R1102
14	1	EB3325	3.3K	R1101
13	11	EB3925	3.9K	R101 - R1001, R1104
12	10	EB4725	4.7K	R103 - R1003
11	1	EB5625	RESISTOR 5.6K 1/2W ±5% (A.B.)	R1105
10				
9	2	150D106X9002B2	CAPACITOR-10μF ±20% 20V (SPRAGUE)	C1, C2
8	1	DM15-621-J	CAPACITOR-620pF ±5% 300V (APCO)	C1101
7				
6	20	2N1302	TRANSISTOR	Q101 - Q1002
5	11	2N1303	TRANSISTOR	Q103 - Q1003, Q1101
4				
3	29	200505-1	DIODE	CR101 - CR1109
2				
1	1	201574-1	PROCESSED BD.-LOGIC REC.	13D
ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION

3. STAMP BOARD TYPE 13D1, AND CURRENT ASSY. REV. LETTER IN UPPER RIGHT HAND CORNER OF BOARD AS SHOWN, 1/8" HIGH BLACK.
2. STRIPE ON DIODE INDICATES CATHODE.
1. SCHEMATIC DWG. NO. 201572

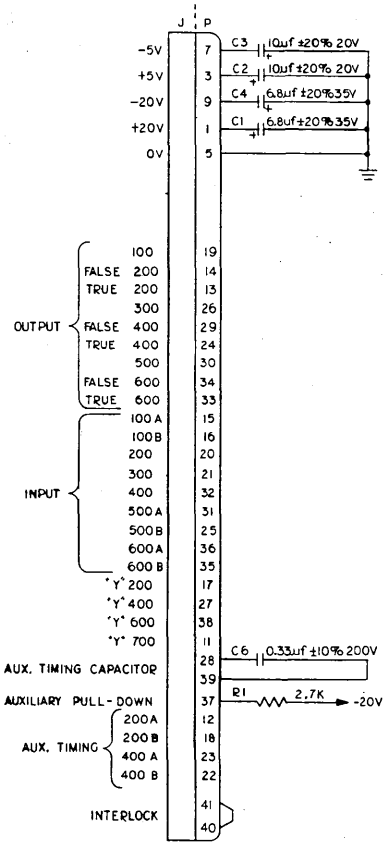
NOTES: UNLESS OTHERWISE SPECIFIED.

data products corporation
CULVER CITY, CALIFORNIA

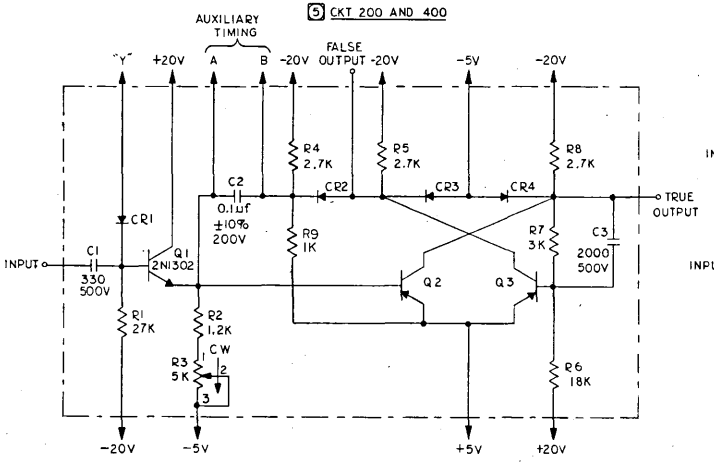
TITLE CKT. BD. ASSEMBLY
LOGIC REC. 13D1

D | DRAWING NO. 201575 | REV B
SHEET 1 CONT. ON —

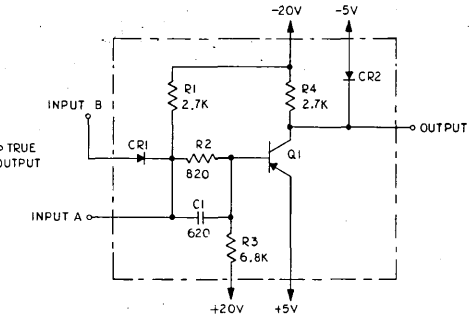
REVISIONS						
ZONE	REV	ECO NO.	DESCRIPTION	CHKR	APP	DATE
	A		PRODUCTION RELEASE	EJ		1/17/64



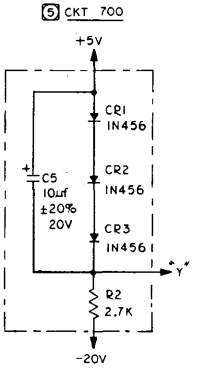
5 CKT 200 AND 400



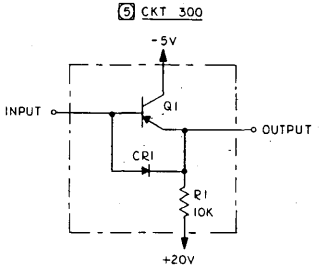
5 CKT 500



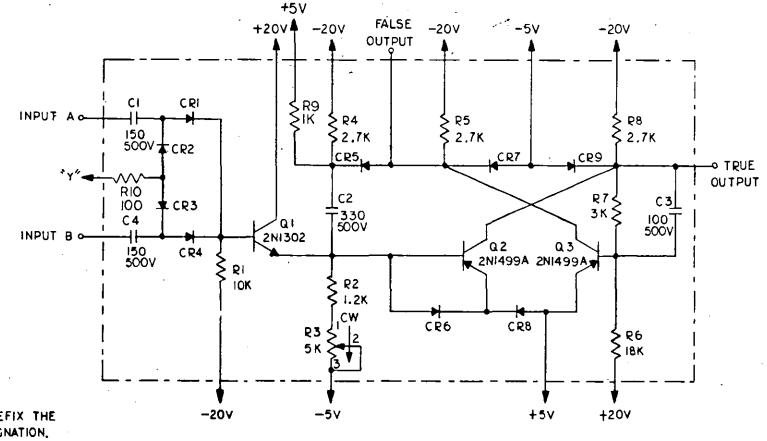
5 CKT 700



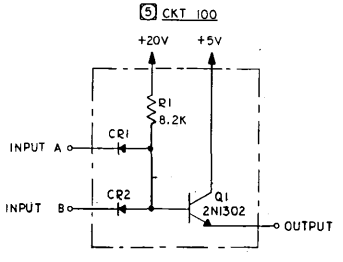
5 CKT 300



5 CKT 600



5 CKT 100



D 203690 A

6. ALL CAPACITOR VALUES IN pf ±5% 300V.
5. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE PART DESIGNATION WITH THE SUBASSEMBLY DESIGNATION.
4. ASSEMBLY DRAWING NO. 203963
3. ALL DIODES C&D 1307
2. ALL TRANSISTORS 2N1303
1. ALL RESISTOR VALUES IN OHMS ±5% 1/2W

NOTE: UNLESS OTHERWISE SPECIFIED

ITEM NO.	REQD	PART NUMBER	DESCRIPTION	MATERIAL SPECIFICATION
			LIST OF MATERIAL	

SUPPLEMENTARY INFORMATION		NAME	DATE
FIRST USED ON 203300	ENG		
NEXT ASSEMBLY	DRFT	P.S. Jervis	12/13/63
	CHKR	EJ Coates	1/17/64
	APP		
	APP	D.W. Hall	1/24/64

MATERIAL
FINISH
DIMENSIONS APPLY AFTER PLATING & HEAT TREATING

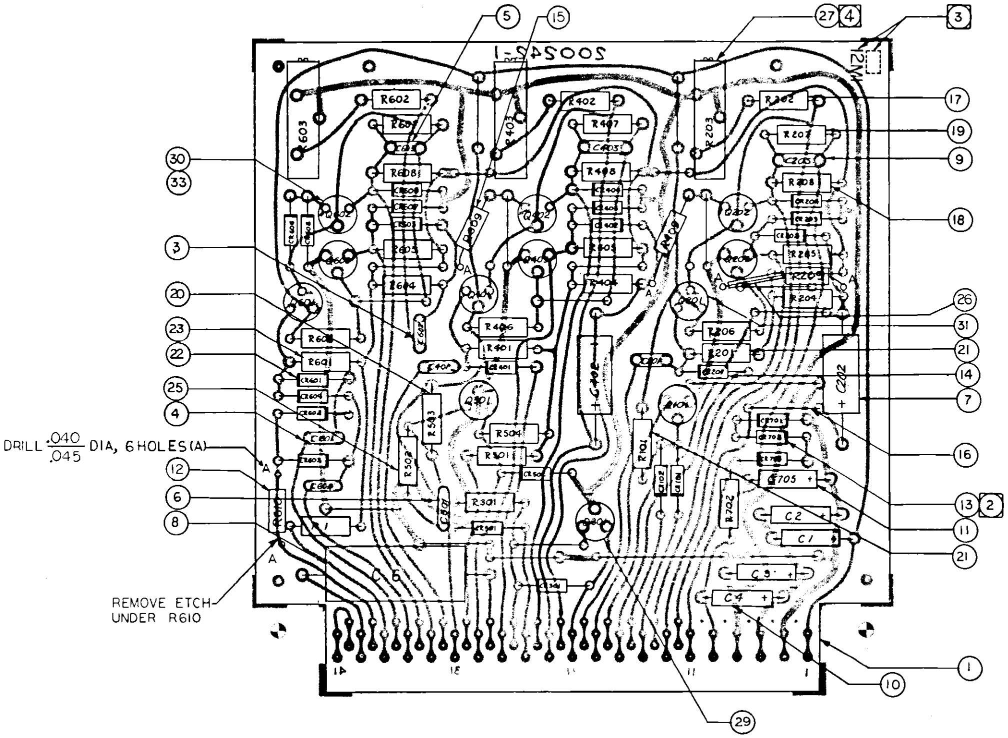
SCALE NONE
DO NOT SCALE DWG
ALL DIMENSIONS ARE IN INCHES
TOLERANCES UNLESS OTHERWISE NOTED:
DECIMAL ±
FRACTION ±
ANGLE ±

data products corporation
CULVER CITY, CALIFORNIA

TITLE
SCHEMATIC
MULTIVIBRATOR 12M1

D 203690 A
SHEET

NO.	E.C.O. NO.	REVISION	APP'D.	DATE
A		PRODUCTION RELEASE		



33	12	K-TO5090-IN	TRANSIPAD (ROBINSON)	
32				
31	4	2N1302	TRANSISTOR	Q101, Q201, Q401, Q601
30	2	2N1499A	TRANSISTOR (SPRAGUE)	Q602 Q603

CAT. D 203693 REV. A

ITEM	REQ'D	PART NO.	DESCRIPTION	REF. DESIGNATION
29	6	2N1303	TRANSISTOR	Q202, Q203, Q402, Q403, Q301, Q501
28				
27	3	3067P-1-502	RESISTOR, VARIABLE 5K (BOURNS)	R203, R403, R603
26	A/R		SLEEVING	
25	1	EB 8215	RESISTOR 820Ω ±5% 1/2W (AB)	R502
24	2	EB 2735	RESISTOR 27K ±5% 1/2W (AB)	R201, R401
23	3	EB 1835	RESISTOR 18K ±5% 1/2W (AB)	R206, R406, R606
22	2	EB 1035	RESISTOR 10K ±5% 1/2W (AB)	R301, R601
21	1	EB 8225	RESISTOR 8.2K ±5% 1/2W (AB)	R101
20	1	EB 6825	RESISTOR 6.8K ±5% 1/2W (AB)	R503
19	3	EB 3025	RESISTOR 3K ±5% 1/2W (AB)	R207, R407, R607
18	13	EB 2725	RESISTOR 2.7K ±5% 1/2W (AB)	R204, R205, R208, R404, R405, R408, R501, R504, R604, R605, R608, R702, 81
17	3	EB 1225	RESISTOR 1.2K ±5% 1/2W (AB)	R202, R402, R602
16	A/R		WIRE 22 GA.	
15	3	EB1025	RESISTOR 1K ±5% 1/2W (AB)	R209, R409, R609
14	22	CGD1307	DIODE	CR101 — CR608
13	3	1N456	DIODE	CR701, CR702, CR703
12	1	EB1015	RESISTOR 100Ω ±5% 1/2W (A.B)	R610
11	3	150D106X0020B2	CAPACITOR 10μf ±20% 20V (SPRAGUE)	C2, C3 C705
10	2	150D685X0035B2	CAPACITOR 6.8μf ±20% 35V (SPRAGUE)	C1, C4
9	2	DM19-202J	CAPACITOR 2000 pf ±5% 500V (ARCO)	C203, C403
8	1	2WFP33	CAPACITOR .33μf ±10% 200V (SPRAGUE)	C6
7	2	2WFP10	CAPACITOR .1μf ±10% 200V (SPRAGUE)	C202, C402
(E) 6	1	DM15-621J	CAPACITOR 620 pf ±5% 300V (ARCO)	C501
5	1	DM15-101J	CAPACITOR 100 pf ±5% 500V (ARCO)	C603
4	2	DM15-151J	CAPACITOR 150 pf ±5% 500V (ARCO)	C601, C604
3	3	DM15-331J	CAPACITOR 330 pf ±5% 500V (ARCO)	C201, C401, C602
2				
1	1	200242-1	PROCESS, BOARD MULTIVIBRATOR RA2	

dp/p 3300	
NEXT ASS'Y.	USED ON
DES. BY	
DR. BY	D.K. Davis 8/13/64
CKD. BY	E. Jacinto 8/17/64
APP. BY	
APP. BY	R. Kelly 8/17/64

MATERIAL:

FINISH:

SCALE: 2/1

TOLERANCES UNLESS OTHERWISE NOTED
DECIMAL ±
FRACTION ±
ANGULAR ±
DIMENSIONS APPLY AFTER PLATING & HEAT TREATING

SHEET 1 OF —

data products corporation
CULVER CITY, CALIFORNIA

TITLE: CIRCUIT BOARD ASSY- MULTIVIBRATOR 12MI

CAT. D DRAWING NUMBER 203693 REV. A

4. TRIMPOTS SHALL BE ASSEMBLED ON CARDS AFTER SOLDERING OPERATIONS ARE COMPLETED TO PREVENT FLUX AND CLEANING SOLVENTS ENTERING TRIMPOTS
3. STAMP BOARD TYPE 12 MI, AND CURRENT ASSY. REV. LETTER IN UPPER RIGHT HAND CORNER OF BOARD AS SHOWN, 1/8" HIGH
2. STRIPE ON DIODE INDICATES DIRECTION OF CATHODE
1. SCHEMATIC DWG. NO. 203690

NOTE: UNLESS OTHERWISE SPECIFIED