RADIO CORPORATION OF AMERICA | ELECTRONIC DATA PROCESSING | CAMDEN, N.J.

SYSTEM REFERENCE MANUAL

RCA 3301 REALCOM EDP

ELECTRONIC DATA PROCESSING SYSTEMS

A BROAD RANGE OF SPEEDS AND CAPABILITIES TO MATCH MANY USER REQUIREMENTS

System Reference Manual

94-16-000
SEPTEMBER, 1967

The information contained herein is subject to change without notice. Revisions may be issued to advise of such additions/and/or corrections.

This manual has been reprinted to include all previous revisions released through December 1966.

The following revision has been issued to this manual:

94-16-000-1 (September 1967)

TABLE OF CONTENTS

RCA
3301
SYSTEM

I RCA 3301 SYSTEM

INTRODUCTION

The RCA 3301 Electronic Data Processing System is an all-purpose system designed to cover a broad range of capability for data processing applications, with inherent characteristics including priority interrupt, which make it readily adaptable for the ever-expanding area of communications. Implemented by a scratch-pad memory in the nanosecond cycle range and a very high order of multi-level simultaneity, the RCA 3301 retains in its design the proven logical concepts of the RCA 301 System, and establishes compatibility with this junior system.

Nominally a medium class system in price range, the RCA 3301 advances the state of the art for all solid-state, stored program digital data processors by virtue of its outstanding versatility, dependability, expansibility and compatibility.

VERSATILITY

- High Speed Memory cycle of 1.5 microseconds.
- Multi-level processing via five operating modes plus fully buffered printed and punched card output.
- Instruction access in 1.93 microseconds.
- Micro Magnetic Memory access or regeneration in less than 214 nanoseconds.
- Automatic priority interrupt system.
- Numerous Input/Output options.
- Powerful instruction repertoire including:

  Parallel transfer by decades (10-character sets)

  Hardware multiply and divide

  Bit manipulation involving Boolean Algebra

  Simplified numeric editing

- Direct and Indirect Addressing plus Index Registers for address modification.
- Minimized operator intervention through a simplified console and Operating System.

DEPENDABILITY

- Logic concepts based on solid foundation of the customer-tested RCA 301.
- Error detection and recovery.
- Built in and programmed accuracy controls.

EXPANSIBILITY

- Memory expansible from 40,000 to 160,000 characters.
- Additional Input/Output Devices:

  Up to 24 Magnetic Tape Stations

  A Second Printer, Card Reader and Card Punch

- Increased speeds (i.e., 15KC to 33KC or 41.7KC or 60KC or 83.4KC or 120KC tapes)

COMPATIBILITY

- Permits operation of RCA 301 programs thus:

  Makes available wide range of tested software.

  Opens door to user-developed programs.

- Instruction repertoire is an extended set of RCA 301 instructions.
- Internal representation identical to the RCA 301.
- Similar devices utilized by both systems.

ELEMENTS OF THE SYSTEM

Elements of the RCA 3301 Electronic Data Processing System comprise a Processor, High Speed Memory and appropriate Input/Output Devices with their corresponding Control Modules. The Control Modules control various Input/Output Devices, generally one for each device used in a system. Control Modules are installed only when their associated Input/Output devices are added to the system.

The Processor is a general purpose, stored program digital machine which includes the following: Program Control, Micro Magnetic Memory, Console with Console Typewriter and Power Supply. Program Control interprets and executes the instructions of the program stored in High Speed Memory, controls the Interrupt System and performs automatic accuracy checks. The Micro Magnetic Memory is a 200-character magnetic core scratch-pad memory used for selective register storage and temporary storage during interrupt and other logical operations. The Console contains an operator's section designed to monitor normal operation of the system by means of a Console Typewriter; and a concealed section with sliding cover, containing the necessary indicators and buttons for maintenance. The Power Supply distributes power to the Processor, Control Modules, and certain Input/Output Devices which require d-c or regulated a-c power. A supplemental Power Supply is available for systems which may require it.

The decimally addressed High Speed Memory (HSM) is a random access, magnetic core, modular designed device having a capacity of 40,000 to 160,000 alphanumeric characters available in increments of 20,000.

Card Readers process cards photoelectrically and serially at maximum rates of 900 or 1470 cards per minute. Demand card reading may be accomplished in the Binary or Translate form.

The Card Punch is a buffered device for punching 80 column cards in either Binary or Translate format at the rate of up to 300 cards per minute.

Two models of the On-Line Printer are available, one printing 120 characters per line and the other printing 160 characters per line. Printing of 47 selected characters occurs at rates up to 1000 lines per minute; printing of 64 characters occurs at rates up to 800 lines per minute.

A variety of Paper Tape Devices are featured for reading and punching 5, 6, 7 or 8-Channel paper tape. The Paper Tape Reader/Punch is a single device for reading and punching at the rate of 100 characters per second (CPS). The Paper Tape Reader reads tape at the rate of up to 1000 CPS. The Paper Tape Punch punches tape at the rate of 100 CPS model. Gapless tape, tape with odd, even, or no parity and tape with advanced sprocket holes may be read and punched.

Magnetic Tape Stations are available in five models: Model 681 with a read/write rate of up to 120,000 alphanumeric characters per seconds (CPS); Model 3484 with read/write rate of up to 60,000 alphanumeric CPS; Model 3485 with a read/write rate of up to 120,000 alphanumeric CPS; Model 582 with a read/write rate of up to 66,667 alphanumeric CPS; and Model 581 with a read/write rate of up to 33,333 alphanumeric CPS. Tape stations are operated through a 2X6 or 2X12 Dual Tape Channel. Up to 24 Tape Station may be operated within the system. Model 3484 and 3485 are compatible with the 7330, 727 and 729 tape stations.

The Data Drum Memory (DDM) provides large capacity, high speed storage for data and computer programs. The Drum is available in six different storage capacities as follows: Model 3464-1 - 327,680 char.; Model 3464-2 - 655,360 char.; Model 3464-3 - 1,310,720 char.; Model 3464-4 - 1,638,400 char.; Model 3464-5 - 1,966,080 char.; and Model 3464-6-2,621,440 char. The drum is 10" in diameter and contains from 128 to 1024 tracks.

The Model 3488 Random Access Computer Equipment provides mass storage in excess of 5.4 billion characters. Data recorded on magnetic cards is accessible in a fraction of a second. These cards are stored in magazines which may be substituted and interchanged in a matter of seconds.

The optional High Speed Arithmetic Unit provides increased computational capabilities through "wired in" fixed and floating point arithmetic, and an addressable 16-digit Accumulator-Product Remainder.

The Data Exchange Control (DXC) enables computer-to-computer communication with another RCA 3301 or an RCA 301. Data transmission may be bi-directional, but only one direction at a time. Data transmission may be initiated by either computer. An RCA 3301 System may include a maximum of two Data Exchange Controls.

The Communications Mode Control (CMC) permits on-line data input/output between an RCA 3301 and data communication lines. An additional mode of simultaneity is included exclusively for the transfer of data in either direction between communication lines and the Processor. The CMC provides for the servicing of 20 to 160 buffer terminated lines (in increments of 20) on either a single or dual scan rate basis. The Video Data Terminal serves as a remote device capable of facilitating remote inquiry systems.

The Communications Control (CC) permits an RCA 3301 to communicate via telephone lines with another computer or remote terminal. Two high speed demand communication lines may be used for sending or receiving, one direction at a time, at rates varying from 1200 to 40,800 bits per second. Manual or automatic dialing of the remote receiving location is permissible.

The Video Data Terminal (VT) is a cathode-ray tube display device which enables an operator to communicate directly with a processor over voice grade communications circuits. A four-row keyboard associated with each VT enables the operator to compose and display messages

containing up to 480 characters prior to transmitting this information to the processor. Transmission and reception of data can be set for either 120 or 180 cps.

The Video Data Interrogator (VI) is similar to the Video Data Terminal in appearance, operation and application. It is normally used under circumstances where several video displays are required at a given location and can share a common communication line to a processor.

The Interrogator Control Terminal (IT) is the control device for up to 8 Video Data Interrogators. It provides a common memory for servicing the VI's and provides the interface between the communication circuit and the processor.

The Digital Clock is a peripheral device which transmits, upon program demand, the time of day in hours, minutes and seconds to the High Speed Memory.

RCA 3301 SOFTWARE SYSTEM

The Software set supplied with the RCA 3301 System includes:

1. A series of Programming Languages and Translators for converting these languages to RCA 3301 machine code (i.e. Assembly System, COBOL and FORTRAN).

2. An Operating System to control the physical environment of the computer.

3. A comprehensive Service Program System incorporating the standard operations performed in a majority of computer installations. These include Peripheral Conversion, Utility, and Program Library Maintenance programs.

4. A Sort/Merge System incorporating advanced techniques which affords the user great flexibility and speed in its use.

5. A program to augment compatibility with the RCA 301.

ORGANIZATION OF DATA

The following definitions describe the various levels of data organization with the RCA 3301 Data Processing System:

BIT:	A bit is a single binary digit, having a value of either zero or one.
CHARACTER:	An RCA 3301 character consists of six information bits and one parity bit combined to represent a decimal digit, a letter of the alphabet, a punctuation or other special mark, or a control symbol.
ITEM:	An item consists of such characters as are necessary to specify a particular unit of information (a numerical quantity, an alphabetic name, a street address, a stock number, etc.). In many cases an item is preceded by a symbol to define its beginning.
RECORD:	A record consists of one or more related items.
LINE:	A line is composed of characters that are to be printed across a single horizontal line on the On-Line Printer. Console Typewriter, or Video Display devices.
BLOCK:	A block is a consecutive group of at least three characters on magnetic or paper tape preceded and followed by an unrecorded area called an "interblock gap". It may consist of one or more records.
FILE:	A file consists of any number of related records. On magnetic tape a file may consist of several tapes or a part of one tape. Files are terminated with an End File Symbol (EF).

VARIABLE LENGTH RECORDING

Data storage in the RCA 3301 system incorporates true variable length recording.

Data storage in a true variable length system does not have the limitations imposed by fixed variable systems. For example, in order to store data of a varying nature in a computer using fixed word length, redundant zeros or spaces are used to fill out the incomplete words. In the RCA 3301, the use of control symbols and the ability to address each character location individually permits the length of any item in any record to be in strict accordance with that item's actual character count. This allows for total variability of item and record length but does not preclude the use of fixed or fixed variable lengths.

In each of these categories: fixed, fixed variable, and variable, the method of internal storage is extended to the external storage. Therefore, if redundant fill characters of the fixed and fixed variable systems are utilized within the computer, they would also appear on magnetic tape or other intermediate storage devices. By utilization of true variable length in the RCA 3301 system, a file requires less recording surface, and therefore, can be entered into or written from the computer in less time.

RCA 3301 CODE

The RCA 3301 System employs a binary code using seven binary digits, or bits, to represent each RCA 3301 character. Of the seven bits which make up each of the characters, the highest order bit (2^6) is the parity bit. The parity bit is used as an accuracy control check. Normally, the total number of "1" bits of each character must equal an odd number or an error results. The remaining six bits are the information bits, with a unique configuration of bits representing each character.

Bit Position	P	2^5	2^4	2^3	2^2	2^1	2^0
Bits	X	X	X	X	X	X	X

(where X = 0 or 1)

For ease in presentation, the bit configurations of the RCA 3301 Code are divided into four groups with the zone bits (2^5 and 2^4) designating the group, as follows:

RCA 3301 CODE GROUP

	2^5	2^4	2^3	2^2	2^1	2^0
Group I	0	0	X	X	X	X
Group II	0	1	X	X	X	X
Group III	1	0	X	X	X	X
Group IV	1	1	X	X	X	X

The following table shows the bit configuration for each character. The parity bit (2^6) is not shown in this table, but is inserted in each configuration to indicate an odd parity count.

GROUP I	GROUP II	GROUP III	GROUP IV				
2^5 2^4	2^5 2^4	2^5 2^4	2^5 2^4	2^3	2^2	2^1	2^0
0 0	0 1	1 0	1 1				
0	&	- (Minus)	"	0	0	0	0
1	A	J	/	0	0	0	1
2	B	K	S	0	0	1	0
3	C	L	T	0	0	1	1
4	D	M	U	0	1	0	0
5	E	N	V	0	1	0	1
6	F	O	W	0	1	1	0
7	G	P	X	0	1	1	1
8	H	Q	Y	1	0	0	0
9	I	R	Z	1	0	0	1
␣ (Space)	+	[(EI)	÷ (EB)	1	0	1	0
#	.	$	,	1	0	1	1
@	;	*	%	1	1	0	0
(	:	> (ED)	↑ (ISS)	1	1	0	1
)	'	< (EF)	=	1	1	1	0
e	C_R (+0)	10	⌑	1	1	1	1

On 80 column cards, the group is designated by the presence or absence of zone punches. Group I has no zone punch. Group II has a Y zone punch, Group III has an X zone punch, and Group IV has a 0 zone punch.

Appendix VIII contains a complete listing of each RCA 3301 character with its corresponding printed symbol representation, bit configuration, and card code. Where appropriate, characters are represented in this manual by printed symbol rather than the above internal code.

II THE PROCESSOR

HIGH SPEED MEMORY

The purpose of the decimally addressable High Speed Memory (HSM) is the storage of programs and data. High Speed Memory size ranges from 40,000 to 160,000 alphanumeric characters in increments of 20,000 characters. The High Speed Memory is 10 characters, or 70 bits (seven bits per character), in depth. Each 20,000 characters of memory consists of seventy 100 x 20 matrices of magnetic cores comprising 140,000 bits. HSM is constructed so that 10 characters in consecutive memory locations may be accessed concurrently. Each group of 10 locations is called a "decade". A decade consists of 10 consecutive HSM locations beginning at XXX0 and ending with XXX9.

Each HSM location is individually addressable and can store one alphanumeric character. Each location is identified by a four-character address. From left to right, the four characters of the address are referred to as the C_0, C_1, C_2 and C_3 positions. To accommodate HSM addresses beyond 10,000 with a four character address, the system utilizes a zone bit convention. The 2^4 and 2^5 (zone) bits of the C_0 and C_1 positions of the HSM address designate multiples as follows:

	C_0		C_1		C_2		C_3	
	2^5	2^4	2^5	2^4	2^5	2^4	2^5	2^4
0000 – 9999	0	0	0	0	0	0	0	0
10,000 – 19,999	0	1	0	0	0	0	0	0
20,000 – 29,999	1	0	0	0	0	0	0	0
30,000 – 39,999	1	1	0	0	0	0	0	0
40,000 – 49,999	0	0	0	1	0	0	0	0
50,000 – 59,999	0	1	0	1	0	0	0	0
60,000 – 69,999	1	0	0	1	0	0	0	0
70,000 – 79,999	1	1	0	1	0	0	0	0
80,000 – 89,999	0	0	1	0	0	0	0	0
90,000 – 99,999	0	1	1	0	0	0	0	0
100,000 – 109,999	1	0	1	0	0	0	0	0
110,000 – 119,999	1	1	1	0	0	0	0	0
120,000 – 129,999	0	0	1	1	0	0	0	0
130,000 – 139,999	0	1	1	1	0	0	0	0
140,000 – 149,999	1	0	1	1	0	0	0	0
150,000 – 159,999	1	1	1	1	0	0	0	0

The lowest address in HSM is always 0000. In a system with a 40,000 character HSM the highest address is Z999, representing memory location 39,999. For an 80,000 character HSM the second 40,000 characters are addressed from 0&00 (40,000) to ZI99 (79,999). The highest address in a system with a 160,000 memory is ZZ99 (159,999). Appendix II contains a chart of memory locations and addresses in 1000 character increments.

Diagrammatic representations of portions of the HSM used throughout this manual follows:

6715	6716	6717	6718	6719
A	B	C	D	E

The HSM address of each location is shown in the upper portion of the diagram, with the characters stored in each location shown in the lower portion.

The memory cycle is 1.5 microseconds. This means that up to ten characters may be addressed, brought into the Memory Register, and regenerated in their original locations every 1.5 microseconds.

Location 0000 - 0225 are reserved as Standard Locations for use by hardware and software. Specific use is made of the following locations:

0206 - 0209	Arithmetic - Temporary storage of address.
0212 - 0215	STA
0216 - 0219	STP
0222 - 0225	STPR

THE BASIC INSTRUCTION

FORMAT AND STORAGE

Each instruction is comprised of 10 characters with the format:

0	N	AAAA	BBBB
Operation Code	N Character	A Address	B Address

The first character (0) identifies the operation or command. The second character (N) indicates a count, symbol, or an I/0 device symbol. In some cases N is used in conjunction with (0) to develop a two-character Operation Code. Generally, the four-character A Address refers to a HSM location, and the four-character B Address refers to another HSM location. In some instructions, however, only a portion of the A Address or B Address is used, or one part of the address may designate one value and the other part another value. The components of the A Address are referred to as A_0, A_1, A_2, A_3, and the components of the B Address as B_0, B_1, B_2, B_3.

Instructions are stored sequentially in HSM. Each instruction is stored in 10 consecutive memory locations starting with XXX0 and ending with XXX9. The Operation Code is therefore placed in the first character of a decade. The processing of each instruction includes an access and execution cycle. During execution, data is manipulated internally by decade, diad or character depending on the particular instruction involved. A diad is two consecutive HSM locations beginning with an even address.

INSTRUCTION ACCESS

Instruction Access is the process of bringing an instruction out of the HSM locations in which it has been stored and placing its components into the proper registers. Only after this occurs can an instruction be interpreted and executed by the Program Control. Instruction Access is accomplished in one machine cycle and requires 1.93 microseconds.

An entire instruction (one decade) is transferred in parallel into the ten-character Memory Register. The Operation Code is then sent to the Normal Operation Register; the N Character to the N Register; the A Address to the A Register; and the B Address to the B Register. This process occurs in the Normal Mode and requires 1.93 microseconds unless indexing and/or indirect addressing is specified. Indexing is indicated by the zone bits of the C_2 character of the A and/or B Addresses and always precedes indirect addressing.

DIRECT AND INDIRECT ADDRESSING

When the least significant character (LSC) of an address is written as a number, i.e., the zone bits are 00, the address is a direct address. Direct addresses establish the initial register settings for instructions in which they are employed. An address is an indirect address when the LSC has zone bits of 01, thus forming the characters "&" through "I" in place of the numbers "0" through "9". During the Instruction Access process, the contents of the HSM location addressed by that indirect address replace it in the register. If the replacing address is also an indirect address, it too will be replaced in the register by the contents of the memory locations it addresses. The initial register settings for any instruction are not established until both the A and B registers have been supplied with direct addresses. An indirect address must address the least significant diad of another address. Each indirect address requires an additional 3.0 microseconds.

REPEAT FEATURE

Repeating an instruction is accomplished by the Repeat (RPT) instruction in conjunction with certain instructions which are repeatable. A repeatable instruction may be repeated from one to 14 times as specified by N. If the N character of the RPT is zero, the repeatable instruction will be executed but not repeated. If the N character of the RPT is one, then the repeatable instruction will be performed twice. The Repeat feature allows the programmer to make use of final register settings when re-executing the repeatable instruction. Each repeatable instruction, when repeated, requires an additional 3.0 microseconds when the Repeat Register exceeds zero, and requires no additional time when the Repeat Register equals zero. Repeatable instructions are identified by REP in the Special Features column of Appendix VII Summary of Instructions.

MICRO MAGNETIC MEMORY

The Micro Magnetic Memory (MMM) is a fast, compact magnetic core device used for selective high speed register storage and temporary storage during interrupt and other logical operations. MMM has a capacity of 200 seven-bit characters, divided into 50 locations, four characters in depth. The speed of this memory permits the reading from one MMM location into the Micro Magnetic Memory Register or the writing from the Micro Magnetic Memory Register to one MMM location within 214 nanoseconds (one time pulse).

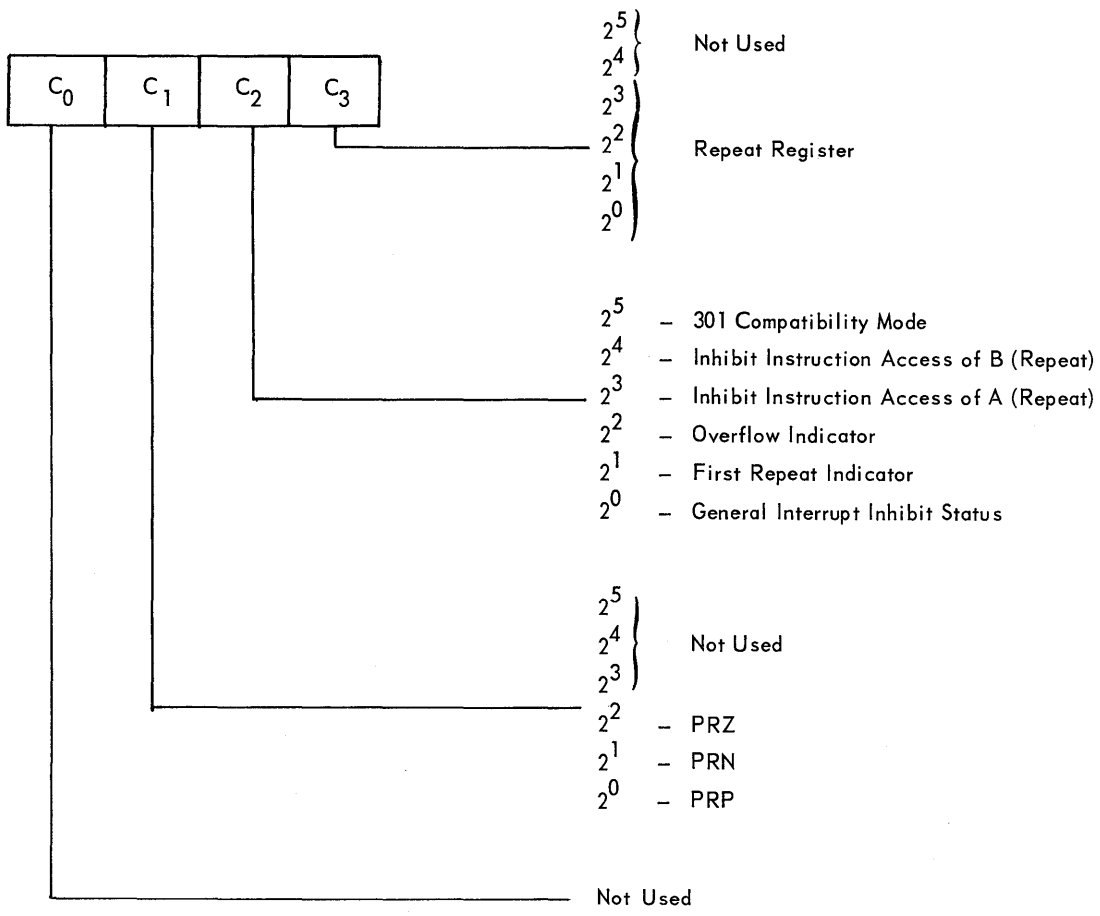
Each location is addressable by a specific N character in the Load and Store Register instructions. Below is a list by function of the four-character locations:

P Register	General Interrupt Routine Entry
A Register	Real-Time Interrupt Routine Entry
B Register	Stop P (Computer Stop Address)
S Register	Multiply/Divide (MD1)
T Register	Multiply/Divide (MD2)
C Register	Multiply/Divide (MD3)
E Register	Multiply/Divide (MD4)
P (General Interrupt)	P (Real-Time Interrupt)
A (General Interrupt)	A (Real-Time Interrupt)
B (General Interrupt)	B (Real-Time Interrupt)
STA (General Interrupt)	STA (Real-Time Interrupt)
STP (General Interrupt)	STP (Real-Time Interrupt)
Control Register (General Interrupt)	Control Register (Real-Time Interrupt)
STPR (General Interrupt)	STPR (Real-Time Interrupt)
Op and N (Simo 1 instruction)	Op and N (Simo 2 instruction)
A Address (Simo 1 instruction)	A Address (Simo 2 instruction)
B Address (Simo 1 instruction)	B Address (Simo 2 instruction)
Index Field 1	Increment Field 1
Index Field 2	Increment Field 2
Index Field 3	Increment Field 3

The Op and N locations have the following format:

C_0C_1	Zero (00)
C_2	Operation Code
C_3	N Character

The Control Register locations have the following format:



PROGRAM CONTROL

Program Control is the logical and arithmetic control unit of the system. It interprets and executes the instructions stored in the High Speed Memory, directs the sequence of operations within the system, controls operation of the Input/Output devices, and performs automatic accuracy checks. Program Control includes a number of specialized components. Those which are of interest to the programmer are briefly discussed below. Figure II-1 indicates the interrelationship of these specialized components and depicts the flow through the Processor.

REGISTERS AND INDICATORS

The Memory Register (MR) has a capacity of 10 characters. Input to this register comes from the HSM or from the Interchange. Output from the register goes to the HSM or to the Interchange.

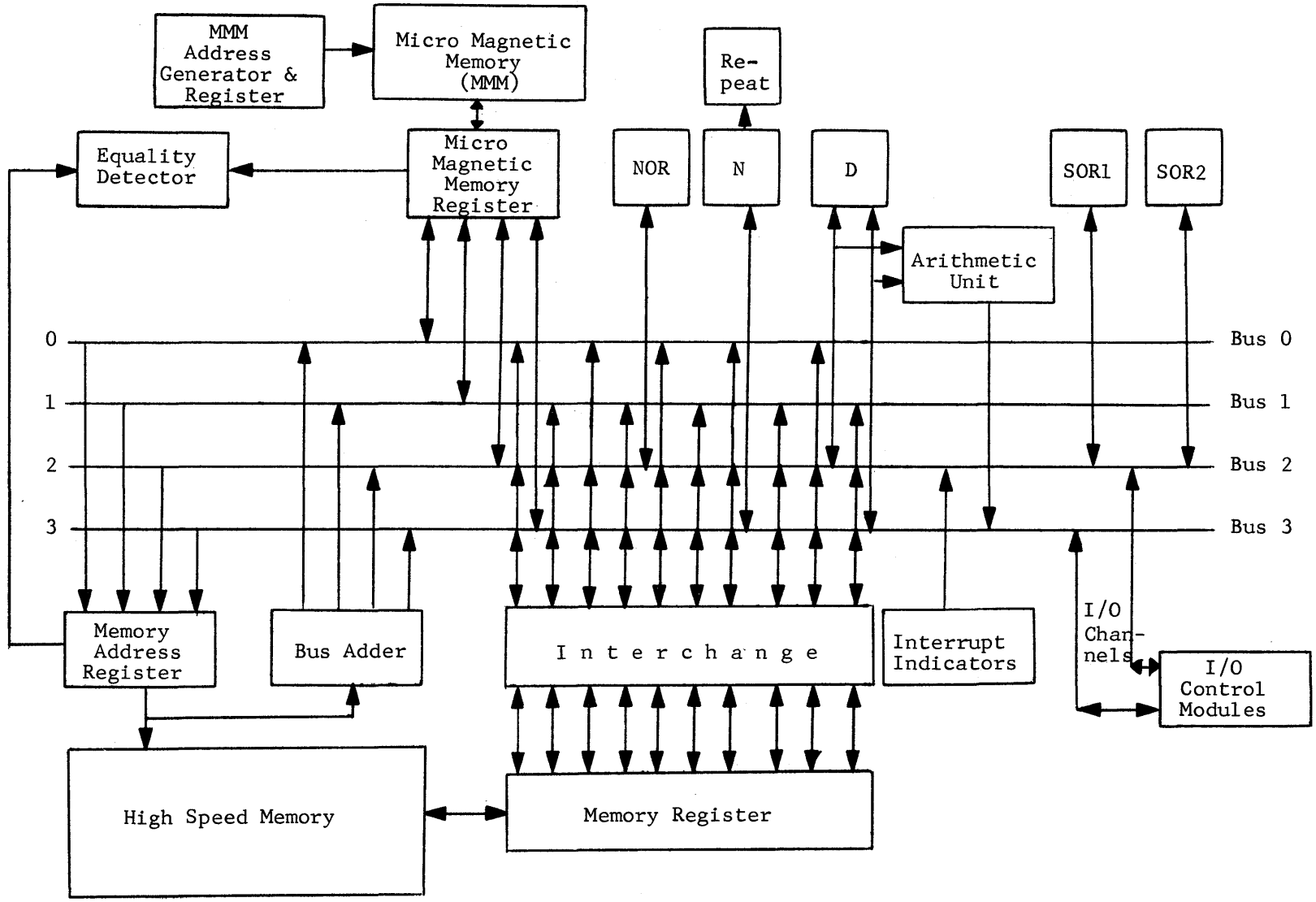


Figure II-1. RCA 3301 Processor Schematic

The Interchange links the Memory Register with the Central Data Bus. It selects the proper bus or busses to which characters are transferred from the Memory Register according to the operation being performed.

The Bus Adder is used to modify the contents of the various address registers. The Bus Adder can increment or decrement the contents of these registers by one or two and increment by ten, or leave them unchanged, thus permitting register contents to be directly related to the currently processed characters, diads, or decades.

The Memory Address Register (MAR) stores the address of the HSM location to be processed. The Capacity of this register is four characters.

The Central Data Bus is a four character pathway between the Interchange, Processor registers, and I/0 channels. The particular pathways used are determined primarily by the Interchange. The individual pathways are specified as Bus 0, Bus 1, Bus 2, and Bus 3 in Figure II-1.

The Equality Detector is used to compare register contents. When the contents of two registers are equal, an indicator is set to notify the Processor that the instruction-defined sector has been processed, and the instruction can be terminated.

The Micro Magnetic Memory Register (MMMR) has a capacity of four characters. Input to the register comes from the Micro Magnetic Memory or from the Central Data Bus. Output from the register goes to the Central Data Bus, the Equality Detector and the Micro Magnetic Memory.

The Micro Magnetic Memory Address Generator and Register has a capacity of one character. It stores the address of the four-character MMM location to be processed.

The Normal Operation Register (NOR) has a capacity of one character. It holds the operation code of the instruction currently being executed in the Normal Mode. Input to the register is from the Memory Register (during Instruction Access). Output from the register is to the Central Data Bus.

The N Register has a capacity of one character. It holds a count, a selected symbol, or a symbol designating an Input/Output device. Input to the register is from the Memory Register (during Instruction Access) and from the Central Data Bus. Output from the register is to the Central Data Bus. An I/O Device Symbol enters the I/O channel from the Central Data Bus.

The Repeat Register has a capacity of one character. It is used by the Repeat instruction to store the count. Input to the Register is from the N Register during a Repeat instruction.

The D Register has a capacity of two characters. It is used in performing arithmetic instructions, comparisons, and temporary storage. The character locations are called D_2 and D_3 since they receive their data from Bus 2 and Bus 3 respectively.

The Arithmetic Unit is a one-character adder which receives one character from D_2 and one character from D_3 within the D Register, performs the addition or subtraction (by complementing) and places the result on Bus 3 of the Central Data Bus.

The Simultaneous Operation Register 1 (SOR1) has a capacity of one character. It holds the operation code of the instruction currently being processed or last initiated (if mode is unoccupied) in the Simo 1 Mode.

The Simultaneous Operation Register 2 (SOR2) has a capacity of one character. It holds the operation code of the instruction currently being processed or last initiated (if mode is unoccupied) in the Simo 2 Mode.

The Previous Result Indicators (PRI's) are a set of indicators which can assume one of three different states: Previous Result Positive (PRP), Previous Result Zero (PRZ), and Previous Result Negative (PRN). The PRI's indicate the resultant sign of an arithmetic operation and record comparison results. The PRI's are set in most of the arithmetic instructions and in certain logical, search, transfer and compare operations. The PRI's may be sensed by use of the Conditional Transfer of Control instruction.

The following registers are contained in the Micro Magnetic Memory:

The A Register has a capacity of four characters. It receives the A Address of an instruction, and when necessary, holds the address of each character being processed in the Normal Mode.

The B Register has a capacity of four characters. It receives the B Address of an instruction, and when necessary, holds the address of each character being processed in the Normal Mode.

The P Register has a capacity of four characters and holds the HSM Address of the next instruction in sequence.

The S Register has a capacity of four characters and receives the A Address of a Simo 1 instruction.

The T Register has a capacity of four characters and receives the B Address of a Simo 1 instruction.

The C Register has a capacity of four characters and receives the A Address of a Simo 2 instruction.

The E Register has a capacity of four characters and receives the B Address of a Simo 2 instruction.

AUTOMATIC STORAGE OF FINAL CONTENTS OF THE A REGISTER (STA)

STA is an automatic operation which occurs at the conclusion of selected instructions. When STA is performed, the final contents of the A Register are automatically stored in the High Speed Memory locations 0212-0215. This permits the subsequent use of the final A Register contents. Instructions which perform STA are identified in the Special Features column of Appendix VII. To preserve the final A Register contents of all other instructions, the Store Register instruction may be used.

AUTOMATIC STORAGE OF CONTENTS OF P REGISTER (STP)

STP is an operation which may occur whenever control is to be transferred; that is, whenever the next instruction to be performed is not the one stored immediately following the current instruction. STP automatically stores the contents of the P Register in standard High Speed Memory locations 0216-0219. The stored address is 0010 greater than the address of the

instruction which effected this transfer of control. Instructions which perform STP are listed in the Special Features column of Appendix VII.

MACHINE CYCLES

The Processor has two machine cycles: a 1,50 microsecond machine cycle consisting of seven pulses; a 1.93 microsecond machine cycle consisting of nine pulses. Pulse rate for the Processor is 214 nanoseconds. Instruction Access of all instructions employs the 1.93 microsecond machine cycle. The majority of instructions employ the 1.50 microsecond machine cycle in their execution process. All input/output instructions and a few arithmetic and data handling instructions use the 1.93 microsecond machine cycle for execution.

MODES OF OPERATION

Up to five instructions may be executed simultaneously by the Processor in addition to any independent operations. This is accomplished by five operating modes:

Normal Mode

Simultaneous Input/Output Mode 1 (Simo 1)

Simultaneous Input/Output Mode 2 (Simo 2)

Simultaneous Input/Output Mode 3 (Simo 3)

Communications Mode Control (CMC) Mode

The Normal, Simo 1 and Simo 2 Modes are standard features on all processors. The CMC Mode is an optional mode of simultaneity for use exclusively with the CMC device. Simo 3 Mode is an optional mode of simultaneity and is limited to magnetic tape and random access devices.

Instruction Access for all instructions occurs in the Normal Mode. From the Operation Code, the Processor determines the mode of execution for each instruction. All processing instructions are executed in the Normal Mode. Input/Output instructions, except those associated with the CMC, are executed in one of the Simultaneous Modes. When a Simo 1 instruction is accessed:

1. The contents of the Normal Operation Register (NOR) are transferred to the Simultaneous Operation Register 1 (SOR_1).

2. The contents of N are transferred to the particular control module identified by N.

3. The contents of the A Register are transferred to the S Register.

4. The contents of the B Register are transferred to the T Register.

Immediately upon transfer of the instruction from the Normal to the Simo 1 Mode, the Normal Mode is free to accept the next instruction. Except for utilizing a different set of registers, a Simo 2 instruction functions similarly.

When Instruction Access occurs on an Input/Output instruction, but the mode specified is occupied, the Busy or Inoperable Interrupt Indicator is set, and interrupt occurs.

Simultaneous operation is achieved by permitting the modes to obtain a machine cycle when requested. Restrictions are placed on the frequency of machine cycles required by the I/O devices to insure concurrent operation.

INTERRUPT

Interrupt is an automatic operation, performed by computer hardware in conjunction with software, causing a temporary break in the operating sequence. Interrupt is provided to facilitate the following functions:

1. Real-Time programming
2. Servicing of multiple Input/Output devices
3. Error recovery procedures
4. Program Testing procedures
5. 301 Compatibility

There are two levels of interrupt: General and Real-Time. General Interrupt takes priority over standard processing. Real-Time Interrupt takes priority over General Interrupt and standard processing. Conditions that cause interrupt, and the number of the indicator which is set, are as follows:

Real-Time	General
1 - Systems Error	6 - Programmed Interrupt
2 - CMC Service Request	7 - Arithmetic Error
3 - (Reserved for Future Enhancement)	8 - Overflow
4 - External Interrupt	9 - Off-Line Operation Complete
5 - Console Request	10 - 301 Compatibility
	11 - Busy or Inoperable
	12 - Simo 3 Terminated Abnormally
	13 - Simo 2 Terminated Abnormally
	14 - Simo 1 Terminated Abnormally
	15 - Simo 3 Terminated Normally
	16 - Simo 2 Terminated Normally
	17 - Simo 1 Terminated Normally
	18 - Program Test

Two 7-location areas in the Micro Magnetic Memory are specified for storage of machine conditions during interrupt. One area is set aside for Real-Time Interrupt and the other for General Interrupt. Stored during interrupt and restored after interrupt are the following registers and conditions:

A Register, B Register, P Register

STA, STP, PRI settings

Repeat Register, STPR (Repeat)

Repeat condition for A and B Addresses

General Interrupt Inhibit Status

Overflow Indicator

301 Compatibility Switch Setting

The storage of the required machine conditions at the time of interrupt requires 9.43 microseconds. Restoring the registers and indicators to their original condition at Return After Interrupt requires 12.64 microseconds.

IMPLEMENTATION

Within the Processor is a set of indicators which are used to record the reason for interrupt as the condition occurs. After an Interrupt Indicator has been set, the actual interruption occurs as soon as the Normal Mode is free, providing there is no prohibitive inhibit. The Normal Mode is free either after completion of an instruction processed in the Normal Mode or at the time an I/O instruction shifts from the Normal to the Simo 1 or Simo 2 Mode for processing. Once interrupt starts, an inhibit is set by hardware which will prevent any subsequent interrupt except by a higher priority condition. Interrupts may also be inhibited by instruction.

When a Real-Time Condition causes interrupt, the status of the Processor at the time of interrupt is stored in the Real-Time storage areas of MMM and the Real-Time/General Inhibit is set. The Real-Time/General Inhibit will prevent any subsequent interrupt from taking place. When a General Condition causes interrupt, the status of the Processor at the time of interrupt is stored in the General storage areas of MMM and the General Inhibit is set. The General Inhibit will prevent any subsequent interrupt due to General Conditions but will permit any Real-Time interrupt to take place. If conditions which would cause interrupt occur while interrupt is inhibited, the particular Interrupt Indicator is still set. If an Interrupt Indicator is set when the inhibit is removed, interrupt takes place at that time. Upon interrupt taking place, program control is transferred to the instruction address that has been preset in the General Interrupt Routine Entry location of MMM if a General Interrupt or to the Real-Time Interrupt Routine Entry if a Real-Time Interrupt.

An Interrupt Routine (software) is executed at this point to identify the cause of interrupt and take appropriate action. The Scan Interrupt instruction facilitates the examination and the resetting of the Interrupt Indicators. The Control Interrupt Logic (CIL) instruction aids in controlling interrupt by setting and removing interrupt inhibits. At the completion of the Interrupt Routine, executed during an interrupt, the stored registers, indicators and standard locations are restored and the inhibits reset by the use of the Return After Interrupt function of the CIL instruction. The area to be used for restoration is selected from the status of the Real-Time Inhibit.

If the Real-Time Inhibit is set, the Processor is restored to the conditions recorded in the Real-Time Interrupt storage area of MMM and the Real-Time Inhibit is removed. If the interrupt sequence was from standard processing directly into Real-Time, the General Inhibit is also removed. If, however, the interrupt sequence was from General into Real-Time Interrupt, the General Interrupt is not removed. This is indicated by the Real-Time Control Register (2^0 of C_2) within MMM.

If the Real-Time Inhibit is not set, the Processor is restored to conditions recorded in the General Interrupt storage area of MMM, and the General Inhibit is removed.

If a Stop-On-Interrupt toggle switch is set on the Auxiliary Console (See Figure III-4) and the corresponding interrupt occurs while the Real-Time/General Inhibit is set, the processor will ignore the inhibit and the interrupt will take place.

CONDITIONS AND INDICATORS

Systems errors which set the Systems Error Indicator include parity errors in the Processor, illegal Operation Codes and addressing outside of the physical size of HSM.

The CMC Service Request indicates that program intervention is requested by the Communications Mode Control.

The External Interrupt Indicator is set by the Data Exchange Control and/or Communications Control.

The Console Request Indicator is set by depressing the Console Request button on the Operator's Console.

The Programmed Interrupt Indicator is set by the Programmed Interrupt instruction.

The Arithmetic Error Indicator is set when the divisor is less than or equal to the dividend in a Divide instruction.

The Overflow Indicator is set when an add or subtract overflow occurs.

The Off-Line Operation Complete Indicator is set when off-line operations are complete. Devices that set this indicator are as follows:

Device	Operation
Buffered Card Punch	Punching complete (buffer available)
Buffered Printer	Printing complete (buffer available)
Random Access	Select complete
Console Typewriter	Carriage return complete

The 301 Compatibility Indicator is set during Instruction Access of 301 I/0 instructions and other selected 301 instructions providing the 301 Compatibility Mode has been specified by the CIL instruction. Refer to Section XVI for details.

The Busy or Inoperable Indicator is set if an I/0 instruction addresses a Mode, Device or Control which is busy or inoperable. See Error Detection and Recovery in Section XV for specific conditions.

The Simo 1 Terminated Abnormally indicates that the last instruction in the Simo 1 Mode terminated in a manner requiring attention. See Error Detection and Recovery.

The Simo 2 Terminated Abnormally indicates that the last instruction in the Simo 2 Mode terminated in a manner requiring attention. See Error Detection and Recovery.

The Simo 3 Terminated Abnormally indicates that the last instruction in the Simo 3 Mode terminated in a manner requiring attention. See Error Detection and Recovery.

The Simo 1 Terminated Normally indicates that the Simo 1 Mode is free for a new instruction.

The Simo 2 Terminated Normally indicates that the Simo 2 Mode is free for a new instruction.

The Simo 3 Terminated Normally indicates that the Simo 3 Mode is free for a new instruction.

The Program Test Indicator provides program control over the Processor during program testing. Setting or removing this mode of operation is controlled by the CIL instruction. When the Program Test Mode is specified, and the Processor is not in an inhibit status, each instruction except the RAI option of the CIL instruction sets the Program Test Indicator, and and interrupt occurs after instruction execution.

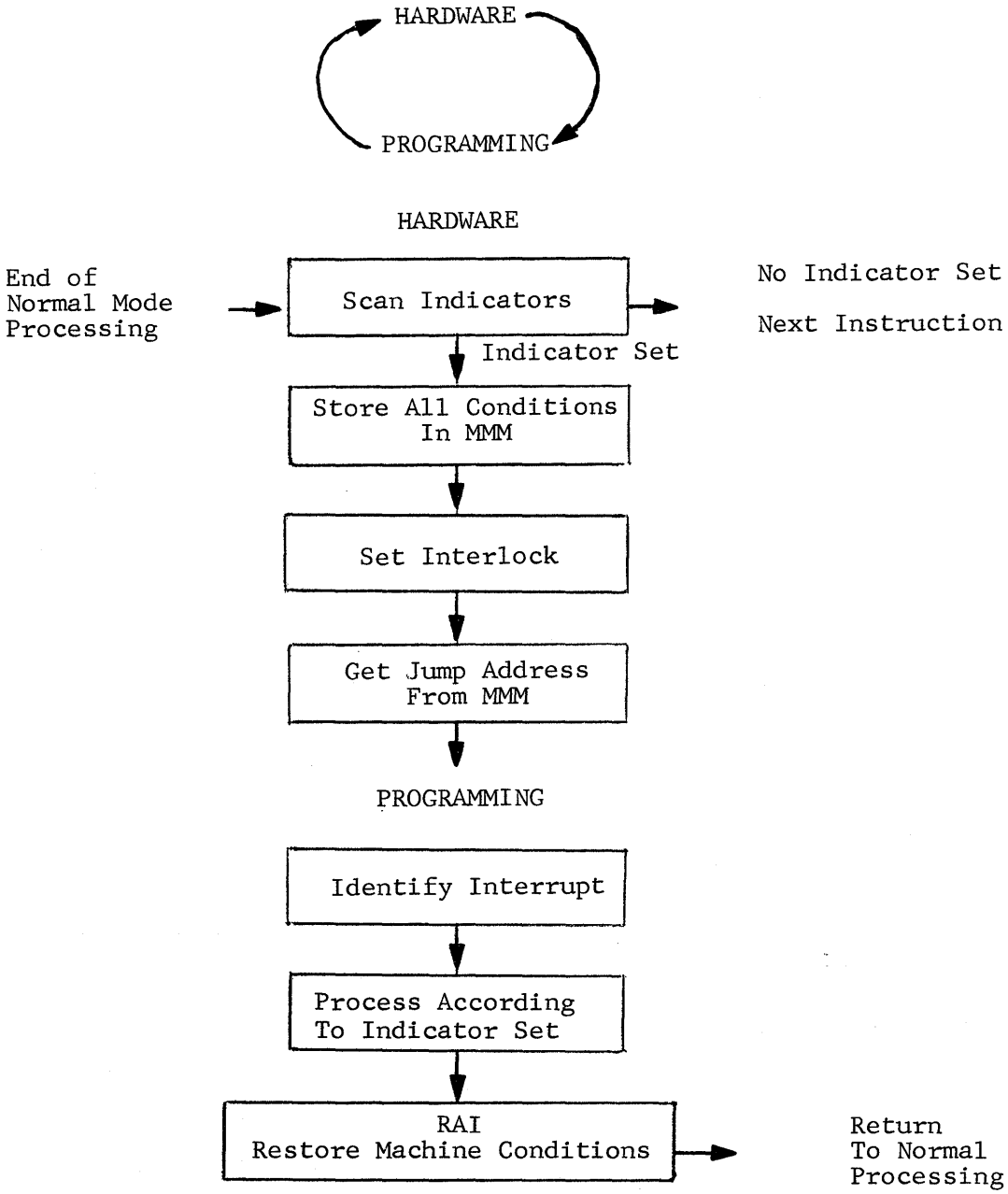


Figure II-2. Interrupt Processing

INDEXING (ADDRESS MODIFICATION)

Three Index Fields and three associated Increment Fields are available for address modification. These Index and Increment Fields, each four characters in length, are contained in the Micro Magnetic Memory and are designated as follows:

Index Field 1	Increment Field 1
Index Field 2	Increment Field 2
Index Field 3	Increment Field 3

Indexing is indicated by the 2^4 and 2^5 bits of C_2 of the A and/or B Addresses as follows:

Index Option	Bit Position 2^5	Bit Position 2^4
No Indexing	0	0
Index Field 1	0	1
Index Field 2	1	0
Index Field 3	1	1

All 3301 instructions may be indexed with the following exceptions:

Test Device - A Address will not be indexed; B Address may be indexed.

Control Device Simo 1
Control Device Simo 2 } - A and B Addresses cannot be indexed.

Control CMC
Halt } - A and B Addresses cannot be indexed.

Unconditional Transfer of Control } - A and B addresses cannot be indexed.

Indexing always precedes indirect addressing. Indexing occurs on the original address before the direct address is accessed and takes 1.93 microseconds per indexed address. The address referenced by an Indirect Address must not contain an Index bit or a Systems Error may occur.

Incrementing of Index Fields is accomplished via the Tally instruction by specifying the desired N character as follows:

N Character Option	Bit Position 2^5	Bit Position 2^4	Bit Position 2^3
No incrementing required	0	0	0
Increment Index Field 1	0	0	1
Increment Index Field 2	0	1	0
Increment Index Field 3	1	0	0

Any combination of incrementing is permitted with one Tally instruction. Incrementing takes 1.93 microseconds per incremented field.

Indexing and incrementing utilize a four-character adder designed to operate in accordance with 3301 addresses. All Addresses, Index Fields, and Increment Fields must be positive since the adder performs strictly adding functions. The four-character adder cycles on 160,000 regardless of the physical size of HSM as the following example indicates:

Address	159,000	Z''00
Index Field	2,000	2000
Result	1,000	1000

The ability to decrement an address is provided by using the complement of 160,000 as the Index Field quantity. For example, address 50,000 would be decremented by 2,000 in the following manner:

Address	50,000	&&00
Index Field	158,000	Y''00
Result	48,000	8&00

III THE CONSOLE

CONSOLE

GENERAL DESCRIPTION

The RCA 3301 Processor includes a separate, dual control with two consoles: an Operator Console to provide operator-machine communications; and a Maintenance Console to provide maintenance capabilities.

OPERATOR CONSOLE

The Operator Console consists of a typewriter and a minimum of control switches, buttons, and display lights. Used in conjunction with RCA-developed software, the Console Typewriter provides documented standard operator/machine communications.

CONSOLE TYPEWRITER

The Console Typewriter is a keyboard printing device which provides, under program control, direct input to and output from the Processor. The maximum output rate is 924 characters per minute. Up to 85 pica characters may be printed per line (10 characters per inch) on single or multiple sheet stock up to 11 inches wide.

The Typewriter's forty-four keys accommodate the printing of sixty-three characters when the keys are activated either manually or by signals received from the Processor. Twenty-six alphabetics, ten numerics, and twenty-seven special symbols are shown on Figure III-1.

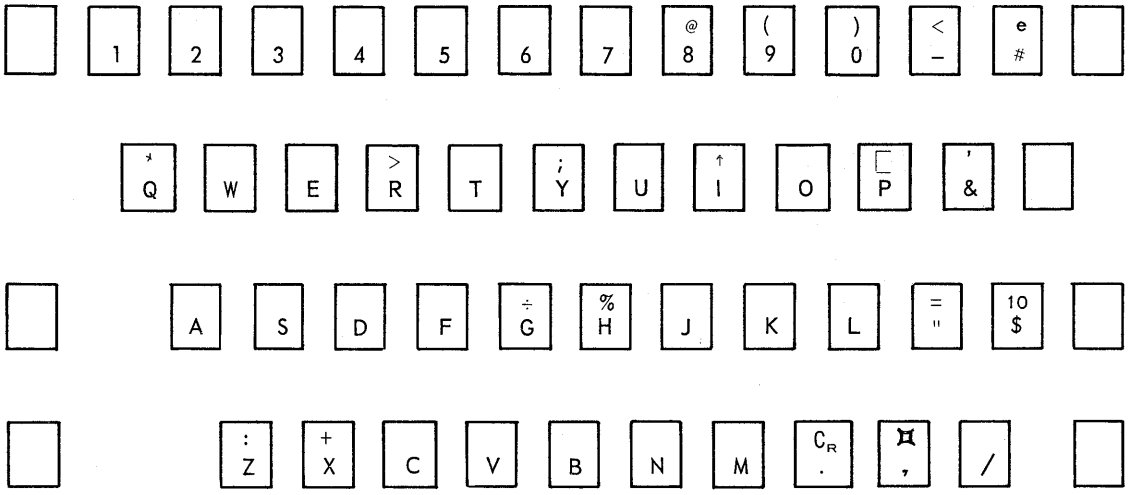


Figure III-1. Console Typewriter Keyboard

The Typewriter has several functional keys which may be operated manually:

Tab

Backspace

Shift (two keys, one at the left, the other at the right)

Lock (refers to shift)

Index (vertical paper movement)

Clear-Set (Tab)

Margin Release

On-Off (Power)

Space Bar (transmits a Space character to the Processor)

Carriage Return

Carriage return also occurs upon reading or writing when A/B Equality is encountered or upon depression of the Release Button.

An Encoder translates the individual key depressions into code signals and sends them to the Processor. A Decoder translates the code signals received from the Processor into codes which actuate the corresponding print functions. Whenever incorrect parity is received by the Decoder, the error symbol (letter e) is printed.

CONSOLE CONTROLS

The lights, buttons, and switches are arranged in two groups. The first group is located on the Maintenance Console but is accessible to the operator. This group includes the following:

MASTER OFF: Depression of this button turns off the DC power supply without disturbing the main power for the System.

POWER ON: Depression of this button turns on the main power supply.

POWER OFF: Depression of this button turns off the main power supply.

MARGINAL CHECK

OVERHEAT WARNING (LIGHT)

D. C. READY

The second group of indicators and switches are located on the Operator's panel (see Figure III-2) and include the following:

ALTERATION SWITCHES

These four independent switches are set and reset manually. When set, a corresponding internal indicator can be interrogated by the CTC instruction.

CANCEL

The operator depresses the Cancel button to terminate data entry and to indicate cancellation of erroneous information. Release and Cancel buttons are locked and unlocked in conjunction with the Keyboard.

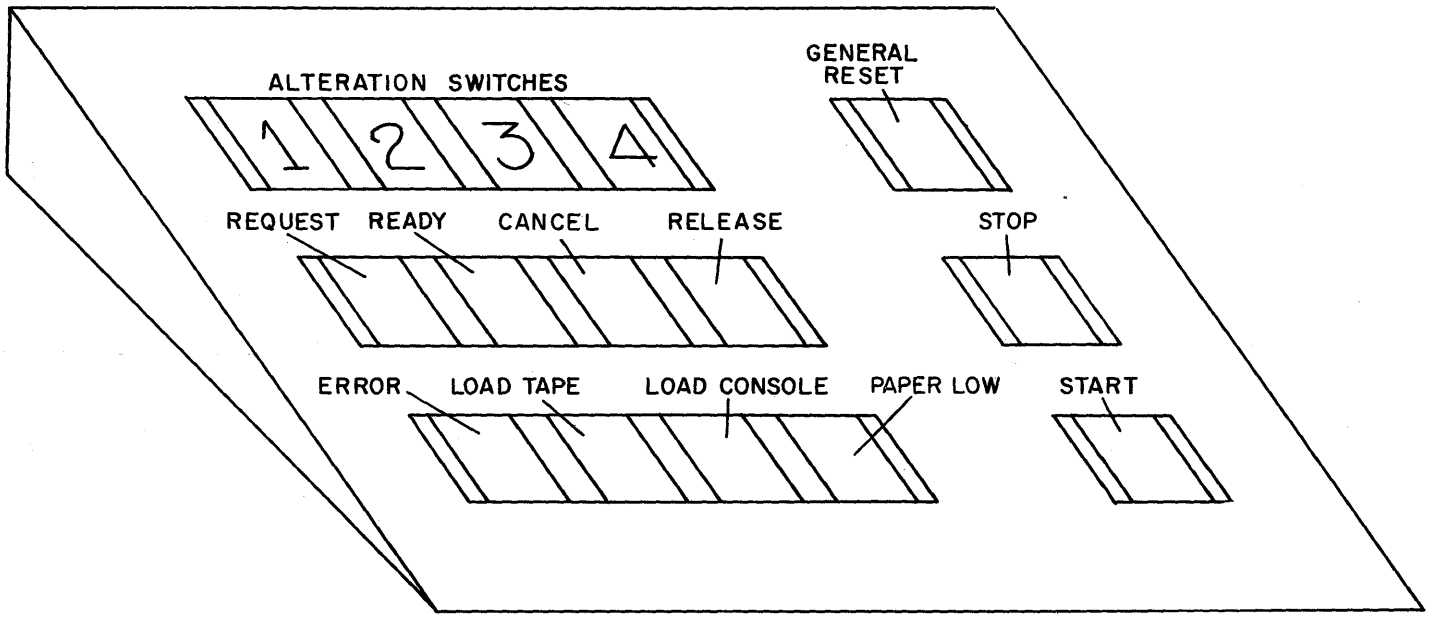


Figure III-2. Operator's Console

READY LIGHT

This light indicates that the Typewriter Keyboard is unlocked, and that the operator may begin to key in data.

REQUEST

Depression of this button by the operator sets the Console Interrupt Indicator and causes program interrupt.

RELEASE

The operator depresses this button to indicate the end of data transmission. This causes the instruction to terminate, releases the mode, locks the Keyboard (including the Release and Cancel buttons) and causes an automatic carriage return.

ERROR (LIGHT)

This light indicates that the machine has stopped upon the detection of double Systems Error, or upon detection of a read instruction parity error when the program load function is exercised.

LOAD TAPE AND LOAD CONSOLE

These two load buttons enable the program load function to be executed either from Magnetic Tape Station #6 or the Console Typewriter. Depression of the Load button causes the Processor to generate a Read Forward instruction from the selected input device into HSM location 0000. Upon successful completion of the read, Interrupt Indicators are not set, and the Processor automatically transfers program control to location 0000.

PAPER LOW (LIGHT)

When lit this indicates that the paper supply for the Console Typewriter is low.

STOP (BUTTON)

Depression of the Stop button brings the Processor to an orderly halt at the completion of the execution of the instruction occupying the Normal Mode. Instructions occupying the Simo modes continue to completion, the P Register is stored in the STOP P location of MMM, and the Stop light is illuminated. This light is also illuminated after a Halt instruction is executed.

GENERAL RESET

Depression of this button clears the Interrupt Register, clears the interrupt inhibits, resets error indicators including those present in Control Modules, and resets all registers not in MMM.

START

Depressing this button causes the Processor to start operation, under program control, with the execution of the instruction addressed by the P Register.

CONSOLE OPERATION

Depressing the Console Request button sets the Console Interrupt Indicator and causes a Real-Time Interrupt. An interrupt program then directs a read instruction to the Typewriter. This read instruction causes the Typewriter Ready light to be lit, unlocks the Typewriter Keyboard, and permits the operator to key in information.

Characters are entered into HSM serially as initially indicated by the A Register. Depressing the Release button by the operator effects normal termination of the instruction. If, however, the Cancel button is depressed or a parity error (PE) is detected, the read instruction is terminated immediately, and the Mode Terminated Abnormally Interrupt Indicator is set.

The read instruction also terminates abnormally if A/B equality is reached prior to depression of the Cancel or Release button. Standard programming procedures specify that the read-in area should exceed the size of the information entered into HSM. This permits operator verification of the typed data prior to instruction termination via depressing the Cancel or Release button. Termination of the instruction from any cause locks the Keyboard. The Test Device (TDV) instruction may be used to determine the reason for an abnormal mode termination.

Output to the Console from the Processor is by the use of write instructions which unlock the Typewriter Keyboard. Characters are transmitted serially to the Typewriter until A/B equality

is reached. Parity errors detected during writing cause the Mode Terminated Abnormally Interrupt Indicator to be set and interrupt to occur after A/B equality has been reached. When the carriage return is completed, the Off-Line Operation Complete Interrupt Indicator is set and interrupt occurs.

INSTRUCTIONS

Instructions utilized for programming the Console Typewriter are:

Read Forward Simo 1 (RF1)	Read Forward Simo 2 (RF2)
Write Simo 1 (WR1)	Write Simo 2 (WR2)
Test Device (TDV)	

These instructions are presented by function under the headings: (1) Reading, (2) Writing, and (3) Testing the Device.

GENERAL DESCRIPTION

The Read Forward Simo 1 (RF1) or Read Forward Simo 2 (RF2) instruction reads information into HSM from the Console Typewriter. Reading begins with the first typed character and normally terminates when the Release signal is received.

FORMAT

OPERATION - 4 (RF1) or 5 (RF2)

N - = (Equal)

A ADDRESS - HSM location to receive the first character.

B ADDRESS - HSM location to receive the last character.

DIRECTION OF OPERATION

Characters are transferred into HSM left to right.

OUTLINE OF OPERATION

One character is transferred to the HSM location specified by the S or C Register. The register is then incremented by one, and the cycle is repeated. The instruction either terminates normally when the Release button is depressed, or abnormally when the Cancel button is depressed, or upon detection of a parity error or A/B equality.

FINAL SETTINGS

$(S)_f$ or $(C)_f$ = HSM location one to the right of the last character read.

$(T)_f$ or $(E)_f$ = $(B)_i$

WRITING

GENERAL DESCRIPTION

The Write Simo 1 (WR1) or Write Simo 2 (WR2) instruction transfers a specified series of consecutive characters from HSM and prints them on the Console Typewriter until A/B equality is reached.

FORMAT

OPERATION - 8 (WR1) or 9 (WR2)

N - = (Equal)

A ADDRESS - HSM location of first character to be written.

B ADDRESS - HSM location of last character to be written.

DIRECTION OF OPERATION

Characters are transferred from HSM left to right.

OUTLINE OF OPERATION

One character is transferred from the HSM location specified by the S or C Register to the Typewriter. The S or C Register is incremented by one, and the cycle is repeated. The instruction terminates when A/B equality is reached. Parity errors detected during writing cause a Mode Terminated Abnormally Interrupt Indicator to be set and interrupt to occur after A/B equality.

FINAL SETTINGS

$(S)_f$ or $(C)_f$ = HSM location one to the right of the last character written.

$(T)_f$ or $(E)_f$ = $(B)_i$

GENERAL DESCRIPTION

The Test Device (TDV) instruction tests the desired status and transfers control if the condition or conditions being tested are present.

FORMAT

OPERATION - S

N - = (Equal)

A ADDRESS - Specifies the function to be performed as follows:

Character	Bit Position	Symbol	Test Function
A_0	2^0	1	Is the Typewriter inoperable?
A_0	2^1	2	Is the Typewriter operating?
A_0	2^2	4	Has a Console Request been received?
A_0	2^3	8	Is there a parity error on read or write?
A_0	2^4	&	Has a message cancel been received?
A_1	2^2	4	Has A/B equality been received?

Unused characters must be zeros and are not to be used by programming.

B ADDRESS - HSM location of the next instruction to be executed if the condition(s) being tested is (are) present.

SPECIAL CONDITIONS

STP is performed if a condition specified by the A Address is present.

FINAL SETTINGS

$(A)_f = (A)_i$

$(B)_f = (B)_i$

MAINTENANCE CONSOLE

The RCA 3301 Maintenance Console (see Figure III-3) is used by on-site RCA Engineering personnel to analyze computer malfunctions and to expedite systems preventive maintenance checkouts. This Console provides the means for manually or automatically monitoring and controlling functions of the Processor and I/O devices. The contents of HSM, MMM, or various registers may be manually changed or displayed. Sufficient indicators, buttons, and switches are provided to satisfy engineering needs. The Maintenance Console is concealed when not in use for equipment check-out. Table III-1 identifies the indicators and switches of the Maintenance Console illustrated in Figure III-3.

Table III-1. Maintenance Console Indicators and Switches

SWITCH OR INDICATOR	DESCRIPTION
INT1 thru INT18	Interrupt Indicators
ME1	Miscellaneous Error 1
ME2	Miscellaneous Error 2
CE	Card Error
BE	Buffer Error
WE	Write Error
RE	Read Error
DNF	Device Does Not Follow
SAE	Switch Address Error
ALR	Alarm Reset
STLE	Status Level Parity Error
MMME	Micro Magnetic Memory Parity Error
MRPE	Memory Register Parity Error
MASP	Interrupt Indicators
PRP	Previous Result Positive
PRN	Previous Result Negative
PRZ	Previous Result Zero
AL1	Alarm Inhibit
Digit Switch	Control Micro Magnetic Memory Selection
E	E Register
C	C Register
T	T Register
S	S Register
B	B Register
A	A Register
P	P Register
ARITHFF	Arithmetic Flip-Flop
MISCFF	Miscellaneous Flip-Flop
NOR	Normal Operation Register
N	N Register
D	D Register
MMMR	Micro Magnetic Memory Register
MR	Memory Register
STL	Status Level Register
ISIM	Inhibit Simultaneity
STLR	Status Level Repeat
DINT	Disable Interrupt
BAI	Bus Adder Inhibit
WRM	Write To Memory
RDM	Read from Memory
OCSP	One Cycle Stop
ICSP	Instruction Complete Stop
S1ER	S1 Status Level Error
ADI	Address Instruction (Also Set for Divide)
ACP	Address Compare (Also Set for Divide or Multiply)
S2RD	Read-in Progress in Simo 2
S2WD	Write-in Progress in Simo 2
MSP	Machine Stop
CFN1	Control Flip-flop #1
CFN2	Control Flip-flop #2
CFN3	Control Flip-flop #3
GENRES	General Reset
START	Start
2OK	Set 301 Compatibility Mode
COMP	Complement
ICAR	Initial Carry
SCAR	Sum Carry
C0	Bus "0" Switches
S1RD	Read-in Progress in Simo 1
S1WD	Write-in Progress in Simo 1
DEB	Program Debug
INHR	Inhibit Real Time Interrupt
RTSTR	Real Time Store (Interrupt)
GENSTR	General Store (Interrupt)
S2ER	S2 Status Level Error
D2M	D2 Register Minus Sign
D3M	D3 Register Minus Sign
RZ	Result Zero
MN2	Counts Multiplier Digits Processed and Counts Cycles During a Divide
MN1	
MN0	
C1	Bus "1" Switches
S3ER	S3 Status Level Error
FT	First Time-MSC Functions in Many Instructions
LT	Last Time-MSC Functions in Many Instructions
MIER13	Multiplier Register-Use in Multiply and Divide
MIER12	
MIER11	
MIER10	
C2	Bus "2" Switches
301	Used when Running a 301 Program
INHB	Inhibit Staticizing B Register During Repeat
INHA	Inhibit Staticizing A Register During Repeat
SCAR2	Sum Carry 2
FREP	First Cycle of Repeatable Instruction
INHG	Inhibit General Interrupt
NER	Normal Mode Error
FLDN	Control Flip-flop-Used in Execution of Multiply
CMIER	Complement Multiplier
MIER23	Multiplier Register-Use in Multiply and Divide
MIER22	
MIER21	
MIER20	
C3	Bus "3" Switches
S3RD	Read-in Progress in Simo 3
S3WD	Write-in Progress in Simo 3
NR3	N Repeat Register
NR2	
NR1	
NR0	

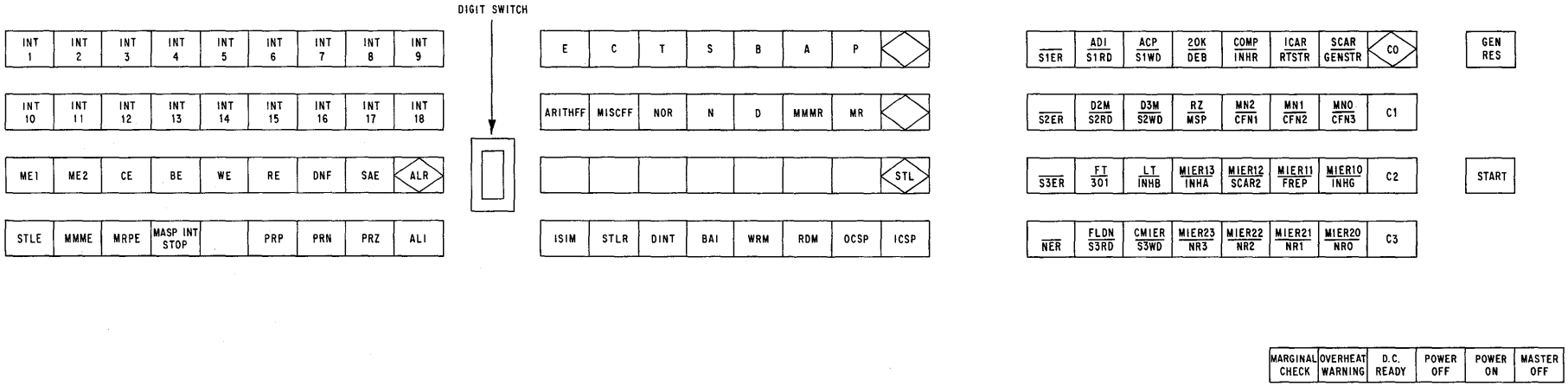


Figure III-3. Maintenance Console

ARITHMETIC AND MISCELLANEOUS FLIP-FLOP DISPLAY

The displaying of the arithmetic flip-flops and other general flip-flops is done by way of the Bus Lights C0, C1, C2, and C3 located in the right bank of indicators on the Maintenance Console. These Bus Lights, in addition to their normal functions, display the flip-flops in accordance with the settings of the ARITHFF and MISCFF Switches located in the middle bank of indicators on the Maintenance Console.

With both the ARITHFF and MISCFF switches Off, the Bus Lights display in accordance with their normal function.

With the ARITHFF switch On, the Bus Lights display those flip-flops designated on the upper portion of the right bank of indicators on the Maintenance Console.

With the MISCFF Switch On, the Bus Lights display those flip-flops designated on the lower portion of the right bank of indicators on the Maintenance Console.

This feature permits only the displaying of these flip-flops. Flip-flops cannot be set from the console.

STORING AND DISPLAYING MODE RESPONSIBLE FOR INTERRUPT 1

This feature provides the ability to store and then to display the mode in which a machine error occurs. Four flip-flops, S1ER, S2ER, S3ER, and NER, provide this capability. The condition of these flip-flops is indicated by the 2^6 position of the Bus Lights.

With the MISCFF switch On, the Bus Lights display the following functions:

Flip-Flop	Function
S1ER	Set if error occurs during S1 status level.
S2ER	Set if error occurs during S2 status level.
S3ER	Set if error occurs during S3 status level.

STORING THE CAUSE OF INTERRUPT 1

Upon entering Interrupt 1, the condition which caused the interrupt will be stored in the C0 character of the Real Time Interrupt Control Register in Micro Magnetic Memory when machine conditions are stored away at interrupt time. This condition is available to the program for use in software or display via the Console Typewriter. If general interrupt occurs and Real Time 1 occurs during I_1 to I_5, this condition will also be present in the General Interrupt Control Register in Micro Magnetic Memory.

The condition causing interrupt will be indicated by setting the bits of C0 as follows:

Bit Set	Condition
2^0	301 I/O instruction when not in 301 Compatibility Mode
2^1	Illegal Operation Code of 3304 Operation Code in a 3303 Processor
2^2	Memory Address Overflow
2^3	Memory Parity Error
2^4	Micro Magnetic Memory Parity Error
2^5	Status Level Error

AUXILIARY CONSOLE

The Auxiliary Console (see Figure III-4) is a portable unit which measures approximately 10-1/2" wide, 7" high, and 9-1/2" deep and can be placed on the console immediately behind the Console Typewriter. It is connected by cable to a connector inside the console. The front panel of the unit contains six memory address digi-switches, seven toggle switches used in conjunction with the digi-switches, and 18 interrupt stop toggle switches.

If a given switch is on when the machine condition selected by the switch occurs, the processor will come to an orderly halt. This means that all Simo instructions go to completion and the current status level in the Normal Mode completes in a manner which permits the continuance of the program by simply pressing the START button.

Note: The switches should be set before starting a program or during a halt; they should not be set with the program running.

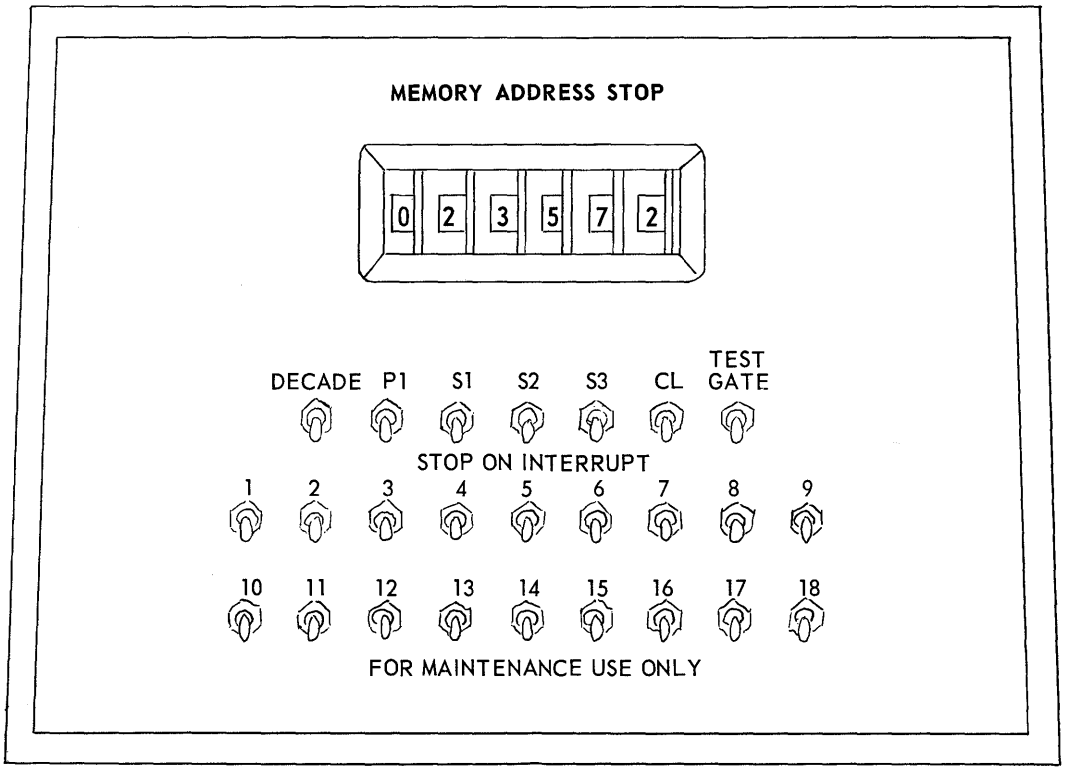


Figure III-4. Auxiliary Console

MEMORY ADDRESS STOP (MASP)

The MASP control consists of six digi-switches and seven toggle switches which occupy the upper portion of the Auxiliary Console control panel. These are set manually and provide the processor with the ability to stop its operation when a predetermined High Speed Memory address is encountered in the Memory Address Register (MAR).

1. DIGI-SWITCHES

The address manually set into the six digi-switches designates the memory address at which the processor will halt. These switches are used in conjunction with the seven toggle switches.

The digi-switches denote HSM addresses from 000,000 through 159,999. The four least significant digits of the digi-switches denote decimal digits from 0000 to 9999. The two most significant digits of the digi-switches have a zone bit notation and extend the addressing scheme above 9999 as follows:

Digi-switch	Address
00XXXX	0000- 9999
01XXXX	10000- 19999
02XXXX	20000- 29999
03XXXX	30000- 39999
10XXXX	40000- 49999
11XXXX	50000- 59999
12XXXX	60000- 69999
13XXXX	70000- 79999
20XXXX	80000- 89999
21XXXX	90000- 99999
22XXXX	100000-109999
23XXXX	110000-119999
30XXXX	120000-129999
31XXXX	130000-139999
32XXXX	140000-149999
33XXXX	150000-159999

where X = any digit from 0 through 9.

2. TOGGLE SWITCHES

The seven toggle switches are set manually to select the conditions under which the MASP function is enabled, as follows:

DECADE

This switch, when on, conditions the processor to halt on a decade address. The least significant digit of both the MAR and the digi-switches is ignored in address comparison. The DECADE switch functions in conjunction with the other switches. If this switch is off, the processor halts on either a character or diad address as explained in the following descriptions of the other switches. The processor comes to an orderly halt after the status level is completed.

P1

If the P1 status level loads a HSM address into the MAR equal to the address indicated by the digi-switches, the processor will come to an orderly halt after the instruction has been staticized. No indirect addressing nor indexing will be performed. This switch is decade-oriented regardless of the setting of the DECADE switch, therefore, the least significant digit of both the MAR and the digi-switches is ignored. This means that addressing of any location within that decade will cause the stop.

S1

If the MAR (during the S1 status level) addresses HSM with an address equal to the address indicated by the digi-switches, the processor will come to an orderly halt. If the DECADE switch is on, comparison will be on a decade basis, the LSD of the address being ignored. If the DECADE switch is off, the comparison will be on the basis of either a character or a diad, depending on whether the S1 status level is handling either a character or a diad.

S2

Same as for S1 above, except for S2 status level.

S3

Same as for S1 above, except for S3 status level.

CL

If the MAR (during any command level) contains an address equal to the address indicated by the digi-switches, the processor will come to an orderly halt at the completion of the status level. Comparison will be made on the basis of character or decade, depending on the setting of the DECADE switch.

TEST GATE

This switch permits the gating of two internal conditions to be selected by maintenance personnel. The gating is performed by means of clip leads. If the two conditions are present, the processor will come to an orderly halt whenever the MAR contains an address equal to the address indicated by the digi-switches. Comparison will be made on the basis of character or decade, depending on the setting of the DECADE switch.

The P1, S1, S2, S3, CL, and TEST GATE switches are all OR'ed together, permitting any combination of these conditions to be enabled simultaneously.

The fourth indicator from the left of the bottom row in the left bank of indicators on the Maintenance Console, has been labeled to read MASP INT STOP. Any halt caused by MASP will light the MASP INT STOP indicator.

STOP ON INTERRUPT

The Stop On Interrupt control consists of 18 toggle switches which occupy the lower portion of the Auxiliary Console control panel. These are set manually and provide the processor with the ability to stop its operation when a predetermined interrupt condition occurs. The switches are numbered from 1 through 18. Following is a listing of the interrupt conditions selected by the 18 toggle switches.

Real-Time

1 - Systems Error
2 - CMC Service Request
3 - (Reserved for Future Enhancement)
4 - External Interrupt
5 - Console Request

6 - Programmed Interrupt
7 - Arithmetic Error
8 - Overflow
9 - Off-Line Operation Complete
10 - 301 Compatibility
11 - Busy or Inoperable
12 - Simo 3 Terminated Abnormally
13 - Simo 2 Terminated Abnormally
14 - Simo 1 Terminated Abnormally
15 - Simo 3 Terminated Normally
16 - Simo 2 Terminated Normally
17 - Simo 1 Terminated Normally
18 - Program Test

If a predetermined interrupt condition occurs, the processor will come to an orderly halt. All Simo Modes will go to completion. The Normal Mode will halt at the end of the instruction which set the interrupt and, in such condition, that pressing the START button will cause the program to continue in the same path it would have taken had the Stop On Interrupt toggle switch not been set. However, the program will halt after each instruction until the interrupt is cleared or until the switch is reset.

If a Stop On Interrupt toggle switch is set and the corresponding interrupt occurs while interrupt is inhibited under program control, the processor will come to an orderly halt.

A halt caused by Stop On Interrupt will light the corresponding Interrupt Stop indicator on the left bank of the Maintenance Console, and will also light the MASP INT STOP indicator on the Maintenance Console.

IV INSTRUCTIONS

INTRODUCTION

Instructions are presented by major function, classified as follows: (1) Data Handling, (2) Arithmetic and Logical, (3) Decision and Control, and (4) Input/Output. For ease of reference, instructions within each major function are in alphabetic order by name.

DATA HANDLING INSTRUCTIONS

These are non-arithmetic instructions for the manipulation of data stored in HSM. Functions performed by these instructions include: (1) filling a portion of HSM with a selected symbol, (2) transferring data from a sending to a receiving area, (3) numeric editing, and (4) character code translation. Operational control by symbol, address and count is provided. Data manipulation is bi-directional. A "left" in the instruction name signifies movement starting with the lefthand character, and a "right" signifies movement starting with a righthand character.

ARITHMETIC AND LOGICAL INSTRUCTIONS

Of these instructions, four are for decimal arithmetic on data, two are decimal arithmetic on addresses and three for logical operations. All decimal instructions for data operate in accordance with algebraic rules and are designed to handle operands of equal length. The instructions used for data arithmetic perform addition, subtraction, multiplication and division on numeric data. The instructions used for address arithmetic provide incrementing and decrementing capabilities specifically for four-character HSM addresses. The logical instructions are used to alter the bit configuration of an operand.

On numeric operands, a sign is indicated by the 2^5 bit of the least significant digit (LSD). When a "1" bit is present in the 2^5 position, the sign is negative. Otherwise, it is assumed to be positive.

DECISION AND CONTROL INSTRUCTIONS

These instructions perform the following functions: (1) influence the sequence of operation, conditionally or unconditionally, (2) data and address comparison, (3) control of and communications with the Interrupt system, (4) two-way communications between MMM and HSM, (5) repetition of an instruction or a group of instructions, and (6) stop the Processor.

INPUT/OUTPUT INSTRUCTIONS

These instructions enable the Processor to communicate with the Input/Output devices. They consist of five basic functions that are executed in either the Simo 1 or Simo 2 mode plus one instruction which tests the status of an I/0 device. The following instructions are included:

Instruction Name	Mnemonic	Operation Code
Control Device Simo 1	CD1	2
Control Device Simo 2	CD2	3
Read Forward Simo 1	RF1	4
Read Forward Simo 2	RF2	5
Read Reverse Simo 1	RR1	6
Read Reverse Simo 2	RR2	7
Write Simo 1	WR1	8
Write Simo 2	WR2	9
Erase Simo 1	ER1	*
Erase Simo 2	ER2	>
Test Device	TDV	S

The Operation Code designates the primary function and mode of operation for execution while the N Character specifies the I/0 device and/or Control Module. Read reverse instructions are only for magnetic and paper tape devices, and the erase instructions are for magnetic tape devices. Input/Output instruction descriptions are presented with each particular device and cover associated options. Corresponding instructions for the Simo 1 Mode and Simo 2 Mode are covered within the same description since they operate similarly except for mode.

INSTRUCTION DESCRIPTION

Information pertaining to each instruction is presented under the headings listed below. When necessary, a special explanation is included:

Instruction Name (with Mnemonic in parenthesis)

General Description

Format

Direction of Operation (optional)

Special Conditions (optional)

Outline of Operation (optional)

Final Settings

Example (optional)

SPECIAL CONDITIONS

Features and conditions that apply to certain instructions are indicated under this heading. These include the automatic storage of STA and STP, PRI's, whether an instruction is repeatable, and overflow and interrupt conditions.

OUTLINE OF OPERATION

An Outline of Operation subsection supplements the General Description prefacing the instruction. Internal logic is described not in every detail, but only to the extent necessary: (1) to help the user gain a better understanding of Computer operation, (2) to permit the user to modify the instructions and their application for individual problem solution, and (3) to enable the user to develop advanced programming techniques.

FINAL SETTINGS

Final register settings plus the settings of the Previous Result Indicators (if applicable) are specified under this heading. Register settings are designated as follows:

$(A)_i$ = Initial register contents after Instruction Access.

$(A)_f$ = Final register contents.

$(S)_f$ or $(C)_f$ and $(T)_f$ or $(E)_f$ refer to the final register settings of an I/0 instruction terminating in either the Simo 1 or Simo 2 Mode.

EXAMPLE

Whenever possible, the examples that accompany the instruction include representation of the affected portion or portions of HSM.

V DATA HANDLING INSTRUCTIONS

FLOAT DOLLAR SIGN TO NON-ZERO NUMERIC (FDN)

GENERAL DESCRIPTION

This instruction fills consecutive locations within a designated sector of HSM with space symbols until a non-zero numeric character is encountered, and then inserts a dollar sign one location to the left of this first non-zero numeric character. A dollar sign is inserted in the rightmost location of the sector if no numeric characters (1-9) are encountered.

FORMAT

OPERATION - , (Comma)

N - $ (Dollar Sign)

A ADDRESS - Leftmost HSM location to be searched.

B ADDRESS - Rightmost HSM location to be searched.

DIRECTION OF OPERATION

Left to right.

SPECIAL CONDITIONS

STA is performed.

PRI's are set.

OUTLINE OF OPERATION

The character specified by the A Register is examined. If this is other than a numeric character (1-9), a space symbol is transferred to the HSM location specified by the A Register. The A and B Registers are compared. If equal, a dollar sign is inserted, and the instruction terminates. If unequal, the A Register is incremented by one, and the cycle is repeated.

When a non-zero numeric is encountered, the A Register is decremented by one, the dollar sign contained in the N Register is then transferred to the HSM location specified by the A Register, and the operation ceases.

If the HMS location specified by the A address contains a non-zero numeric, the dollar sign is floated to $A_i - 1$.

FINAL SETTINGS

$(A)_f = (B)_i$, if a non-zero numeric character is not found.

$(A)_f$ = HSM location containing the Dollar Sign if a non-zero numeric character is found.

$(B)_f = (B)_i$

PRP is set if a non-zero numeric is found.

PRZ is set if a non-zero numeric is not found.

EXAMPLE

Instruction: , $ 8550 8556

HSM Before Execution:

8550	8551	8552	8553	8554	8555	8556
0	0	1	0	8	7	5

HSM After Execution:

8550	8551	8552	8553	8554	8555	8556
–	$	1	0	8	7	5

Final Settings: $(A)_f$ = 8551 $(B)_f$ = 8556 PRP is set.

GENERAL DESCRIPTION

This instruction searches through the contents of successive HSM locations between and including two specified addresses looking for the absence of a specified symbol. The operation ceases when the rightmost location is reached or upon detecting the absence of the specified symbol.

FORMAT

OPERATION - K

N - Specified symbol.

A ADDRESS - Leftmost HSM location to be searched.

B ADDRESS - Rightmost HSM location to be searched.

DIRECTION OF OPERATION

Left to right.

SPECIAL CONDITIONS

STA is performed.

PRI's are set.

OUTLINE OF OPERATION

Initially PRZ is set. The A Register is compared with the B Register. The character specified by the A Register is then compared with the N Register. The A Register is incremented by one, and based on the above two comparisons one of the following occurs:

1. If the character specified by the A Register is not equal to N, and this is the first character checked; PRN is set, the A Register is decremented by two, and the instruction terminates.

2. If the character specified by the A Register is not equal to N, and this is not the first character checked; PRP is set, the A Register is decremented by two, and the instruction terminates.

3. If both comparisons prove equal; the A Register is decremented by one, and the instruction terminates.

4. If the character specified by the A Register is equal to N, but the A Register is not equal to the B Register; the cycle is repeated.

FINAL SETTINGS

If a character is found not equal to the specified symbol (N)

$(A)_f$ = One HSM address to the left of that character.

$(B)_f = (B)_i$

If all characters searched are equal to the specified symbol (N)

$(A)_f = (B)_i$

$(B)_f = (B)_i$

PRN is set when the first character searched is not equal to N.

PRZ is set when all characters searched are equal to N.

PRP is set if a non-specified symbol is found in the designated HSM area after a character equal to the specified symbol (N) has been found.

EXAMPLE

Instruction: K 0 5000 5008

HSM Before and After Execution:	5000	5001	5002	5003	5004	5005	5006	5007	5008
	0	0	0	0	0	6	0	4	0

Final Settings: $(A)_f$ = 5004 $(B)_f$ = 5008 PRP is set.

GENERAL DESCRIPTION

This instruction searches through the contents of successive HSM locations between and including two specified addresses looking for the absence of a specified symbol. The operation ceases when the leftmost location is reached or upon detecting the absence of the specified symbol.

FORMAT

OPERATION - L

N - Specified symbol.

A ADDRESS - Rightmost HSM location to be searched.

B ADDRESS - Leftmost HSM location to be searched.

DIRECTION OF OPERATION

Right to left.

SPECIAL CONDITIONS

STA is performed.

PRI's are set.

OUTLINE OF OPERATION

Initially PRZ is set. The A Register is compared with the B Register. The character specified by the A Register is then compared with the N Register. The A Register is decremented by one, and based on the above two comparisons, one of the following occurs:

1. If the character specified by the A Register is not equal to N, and this is the first character checked; PRN is set, the A Register is incremented by two, and the instruction terminates.

2. If the character specified by the A Register is not equal to N, and this is not the first character checked; PRP is set, the A Register is incremented by two, and the instruction terminates.

3. If both comparisons prove equal; the A Register is incremented by one, and the instruction terminates.

4. If the character specified by the A Register is equal to N, but the A Register is not equal to the B Register; the cycle is repeated.

FINAL SETTINGS

If a character is found not equal to the specified symbol (N)

$(A)_f$ = One HSM address to the rignt of that character.

$(B)_f = (B)_i$

If all characters searched are equal to the specified symbol (N)

$(A)_f = (B)_i$

$(B)_f = (B)_i$

PRN is set if the first character searched is not equal to N.

PRZ is set when all characters searched are equal to N.

PRP is set when a non-specified symbol is found in the designated HSM area after a character equal to the specified symbol (N) has been found.

EXAMPLE

Instruction: L – 4009 4001

HSM Before and After Execution:	4001	4002	4003	4004	4005	4006	4007	4008	4009
	0	3	0	9	–	–	–	–	–

Final Settings: $(A)_f$ = 4005 $(B)_f$ = 4001 PRP is set.

GENERAL DESCRIPTION

This instruction inserts a specified symbol into each HSM location between and including two given addresses.

FORMAT

OPERATION - J

N - Specified Symbol.

A ADDRESS - Leftmost HSM location to be filled.

B ADDRESS - Rightmost HSM location to be filled.

DIRECTION OF OPERATION

Left to right.

OUTLINE OF OPERATION

The symbol in the N Register is transferred to the HSM location specified by the A Register. The A Register is compared with the B Register. If equal, the A Register is incremented by one, and the instruction terminates. If unequal, the A Register is incremented by one, and the cycle is repeated.

FINAL SETTINGS

$(A)_f = (B)_i + 1$

$(B)_f = (B)_i$

EXAMPLE

Instruction: J 0 8001 8009

HSM Before Execution:

8000	8001	8002	8003	8004	8005	8006	8007	8008	8009	8010
1	2	3	4	5	1	2	3	4	5	A

HSM After Execution:

8000	8001	8002	8003	8004	8005	8006	8007	8008	8009	8010
1	0	0	0	0	0	0	0	0	0	A

Final Settings: $(A)_f$ = 8010 $(B)_f$ = 8009

SYMBOL FILL TO NON-ZERO NUMERIC (SFN)

GENERAL DESCRIPTION

This instruction fills consecutive locations within a designated sector of HSM with a specified symbol until a non-zero numeric character is encountered.

FORMAT

OPERATION - , (Comma)

N - Specified symbol. Any symbol except the Dollar Sign may be specified (see FDN instruction).

A ADDRESS - Leftmost HSM location to be searched.

B ADDRESS - Rightmost HSM location to be searched.

DIRECTION OF OPERATION

Left to right.

SPECIAL CONDITIONS

STA is performed.

PRI's are set.

OUTLINE OF OPERATION

The contents of the HSM location specified by the A Register are examined. If this is other than a numeric character (1-9), the symbol in N is transferred to the HSM location specified by the A Register. The operation ceases when a non-zero numeric character is found or when the A Register equals the B Register. Otherwise, the A Register is incremented by one, and the cycle is repeated.

FINAL SETTINGS

$(A)_f = (B)_i$, if a non-zero numeric character is not found.

$(A)_f$ = HSM location of the first non-zero numeric character found.

$(B)_f = (B)_i$

PRP is set if a non-zero numeric is found.

PRZ is set if a non-zero numeric is not found.

EXAMPLE

Instruction: , – 4055 4060

HSM Before Execution:

4054	4055	4056	4057	4058	4059	4060	4061
5	0	0	0	1	5	7	–

HSM After Execution:

4054	4055	4056	4057	4058	4059	4060	4061
5	–	–	–	1	5	7	–

Final Settings: $(A)_f$ = 4058 $(B)_f$ = 4060 PRP is set.

TRANSFER BY COUNT LEFT (TCL)

GENERAL DESCRIPTION

This instruction transfers a specified number of consecutive characters from one HSM (sending) area to another HSM (receiving) area. It may be used to transfer from one to 45 characters.

FORMAT

OPERATION - M

N - Number of characters (0-45) to be transferred. See Appendix III.

A ADDRESS - HSM location of leftmost character in sending area.

B ADDRESS - HSM location of leftmost character in receiving area.

DIRECTION OF OPERATION

Left to right.

SPECIAL CONDITIONS

Instruction is repeatable.

OUTLINE OF OPERATIONS

The N Register is examined. If zero, the instruction terminates. If other than zero, the character specified by the A Register is transferred to the HSM location specified by the B Register. The A and B Registers are incremented by one, the N Register is decremented by one, and the cycle is repeated.

FINAL SETTINGS

$(A)_f$ = HSM location one to the right of the last character in sending area.

$(B)_f$ = HSM location one to the right of the last character in receiving area.

EXAMPLE

Instruction: M 4 4000 4005

HSM Before Execution:	4000	4001	4002	4003	4004	4005	4006	4007	4008	4009
	B	A	L	L	–	–	–	–	–	–

HSM After Execution:	4000	4001	4002	4003	4004	4005	4006	4007	4008	4009
	B	A	L	L	–	B	A	L	L	–

Final Settings: $(A)_f$ = 4004 $(B)_f$ = 4009

GENERAL DESCRIPTION

This instruction transfers a specified number of consecutive characters from one HSM (sending) area to another HSM (receiving) area. It may be used to transfer from one to 45 characters.

FORMAT

OPERATION - N

N - Number of characters (0-45) to be transferred. See Appendix III.

A ADDRESS - HSM location of rightmost character in sending area.

B ADDRESS - HSM location of rightmost character in receiving area.

DIRECTION OF OPERATION

Right to left.

SPECIAL CONDITIONS

Instruction is repeatable.

OUTLINE OF OPERATION

The N Register is examined. If zero, the instruction terminates. If other than zero, the character specified by the A Register is transferred to the HSM location specified by the B Register. The A, B, and N Registers are decremented by one, and the cycle is repeated.

FINAL SETTINGS

$(A)_f$ = HSM location one to the left of the last character in sending area.

$(B)_f$ = HSM location one to the left of the last character in receiving area.

EXAMPLE

Instruction: N 4 4003 4008

HSM Before Execution:

4000	4001	4002	4003	4004	4005	4006	4007	4008	4009
B	A	L	L	–	–	–	–	–	–

HSM After Execution:

4000	4001	4002	4003	4004	4005	4006	4007	4008	4009
B	A	L	L	–	B	A	L	L	–

Final Settings: $(A)_f = 3999$ $(B)_f = 4004$

GENERAL DESCRIPTION

This instruction transfers non-edited, numeric data to an edit field inserting edit symbols during the process. A mask containing spaces and properly positioned edit symbols must first be transferred to the edit field. An ISS in the edit field causes a space to be generated in its location; all other nonspace characters remain in their corresponding locations within the edit field. If the data to be edited is negative, PRN is set. All zone bits of data to be edited are removed before the character is transferred to the edit field.

FORMAT

OPERATION - ÷

N - Number of characters (0–45) to be transferred and edited. See Appendix III.

A ADDRESS - HSM location of the rightmost character of the edit (receiving) field.

B ADDRESS - HSM location of the rightmost character of the non-edited (sending) field.

DIRECTION OF OPERATION

Right to left.

SPECIAL CONDITIONS

STA is performed.

PRI's are set.

OUTLINE OF OPERATION

Initially, PRZ is set. The N Register is examined. If zero, the instruction terminates. If not zero, the character specified by the B Register is transferred to the D_3 portion of the D Register.

If this is the first character (LSC) transferred, a check is made for a negative quantity. If negative, PRN is set, and the zone bits of the LSC are removed.

The B and the N Registers are then decremented by one. The character specified by the A Register is transferred to the D_2 portion of the D Register. This character is examined and one of the following occurs:

1. If a space, the character in D_3 is transferred to the HSM location specified by the A Register.

2. If an ISS, a space character is transferred to the HSM location specified by the A Register.

3. If not a space or an ISS, the character in D_2 is transferred to the HSM location specified by the A Register.

The A Register is then decremented by one. If the character in D_3 was not transferred, the character now specified by the A Register is examined in the D_2 Register, and the cycle continues until D_3 is transferred. When D_3 is transferred, the character specified by the B Register is examined, and the cycle is repeated until N is zero.

FINAL SETTINGS

$(A)_f = (A)_i$ - (N count + number of edit symbols encountered)

$(B)_f = (B)_i$ - N count

PRN is set if data to be edited is negative; otherwise PRZ is set.

EXAMPLE

Instruction: ÷ 8 8560 4019

HSM Before Execution:

8550	8551	8552	8553	8554	8555	8556	8557	8558	8559	8560
–	–	–	,	–	–	–	.	–	–	•

HSM Before and After Execution:

4010	4011	4012	4013	4014	4015	4016	4017	4018	4019	4020
–	–	0	0	1	8	7	5	3	M	–

HSM After Execution:

8550	8551	8552	8553	8554	8555	8556	8557	8558	8559	8560
0	0	1	,	8	7	5	.	3	4	–

Final Settings: $(A)_f$ = 8549 $(B)_f$ = 4011 PRN is set.

GENERAL DESCRIPTION

This instruction transfers consecutive characters from one HSM (sending) area to another HSM (receiving) area until a specified symbol is both transferred and sensed.

FORMAT

OPERATION - #

N - Any specified symbol after which to stop transferring.

A ADDRESS - HSM location of leftmost character in sending area.

B ADDRESS - HSM location of leftmost character in receiving area.

DIRECTION OF OPERATION

Left to right.

SPECIAL CONDITIONS

STA is performed.

Instruction is repeatable.

OUTLINE OF OPERATION

The character specified by the A Register is compared with the symbol in the N Register. The character specified by the A Register is then transferred to the HSM location specified by the B Register, and the A and B Registers are incremented by one. If the above comparison proved equal, the instruction terminates. If the above comparison proved unequal, the cycle is repeated.

FINAL SETTINGS

$(A)_f$ = HSM location one to the right of the specified symbol in the sending area.

$(B)_f$ = HSM location one to the right of the specified symbol in the receiving area.

EXAMPLE

Instruction: # • 2000 2006

HSM Before Execution:

2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
$	1	2	3	•	–	–	–	–	–	–

HSM After Execution:

2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
$	1	2	3	•	–	$	1	2	3	•

Final Settings: $(A)_f = 2005$ $(B)_f = 2011$

GENERAL DESCRIPTION

This instruction transfers consecutive characters from one HSM (sending) area to another HSM (receiving) area until a specified symbol is both transferred and sensed.

FORMAT

OPERATION - P

N - Any specified symbol after which to stop transferring.

A ADDRESS - HSM location of rightmost character in sending area.

B ADDRESS - HSM location of rightmost character in receiving area.

DIRECTION OF OPERATION

Right to left.

SPECIAL CONDITIONS

STA is performed.

Instruction is repeatable.

OUTLINE OF OPERATION

The character specified by the A Register is compared with the symbol in the N Register. The character specified by the A Register is then transferred to the HSM location specified by the B Register, and the A and B Registers are decremented by one. If the above comparison proved equal, the instruction terminates. If the above comparison proved unequal, the cycle is repeated.

FINAL SETTINGS

$(A)_f$ = HSM location one to the left of the specified symbol in the sending area

$(B)_f$ = HSM location one to the left of the specified symbol in the receiving area.

EXAMPLE

Instruction: P $ 2010 2004

HSM Before Execution:

2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
–	–	–	–	–	–	$	1	2	3	•

HSM After Execution:

2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
$	1	2	3	•	–	$	1	2	3	•

Final Settings: $(A)_f = 2005$ $(B)_f = 1999$

GENERAL DESCRIPTION

This instruction transfers a specified number of consecutive decades from one HSM (sending) area to another HSM (receiving) area. It may be used to transfer from one to 45 decades. A decade is 10 consecutive HSM locations beginning at XXX0 and ending with XXX9.

FORMAT

OPERATION - $_{10}$ (Subscript$_{10}$)

N - Number of decades (0-45) to be transferred. See Appendix III.

A ADDRESS - HSM location of leftmost decade in sending area.

B ADDRESS - HSM location of leftmost decade in receiving area.

DIRECTION OF OPERATION

Left to right.

SPECIAL CONDITIONS

Instruction is repeatable.

OUTLINE OF OPERATION

The N Register is examined. If zero, the instruction terminates. If not zero, the decade specified by the A Register is transferred to the decade specified by the B Register. The A and B Registers are incremented by ten, the N register is decremented by one, and the cycle is repeated.

The rightmost digit is ignored in the A and B addresses.

FINAL SETTINGS

$(A)_f = (A)_i + 10n$

$(B)_f = (B)_i + 10n$

n = number of decades transferred.

EXAMPLE

Instruction: $_{10}$ 1 5000 4010

HSM Before Execution:

4010	4011	4012	4013	4014	4015	4016	4017	4018	4019
–	–	–	–	–	–	–	–	–	–

HSM Before and After Execution:

5000	5001	5002	5003	5004	5005	5006	5007	5008	5009
0	0	0	0	1	8	7	5	3	4

HSM After Execution:

4010	4011	4012	4013	4014	4015	4016	4017	4018	4019
0	0	0	0	1	8	7	5	3	4

Final Settings: $(A)_f = 5010$ $(B)_f = 4020$

GENERAL DESCRIPTION

This instruction translates characters from one bit configuration to another by the use of a translate table. The instruction translates from one to 45 consecutive characters in memory. Each character to be translated is used to generate the two rightmost digits of the address within the table that holds the translated equivalent. The leftmost location of the translate table must end in 00.

FORMAT

OPERATION - A

N - Number of characters (0–45) to be translated. See Appendix III.

A ADDRESS - HSM location of leftmost character to be translated and the result area.

B ADDRESS - HSM location of leftmost character of translate table (must end in 00).

DIRECTION OF OPERATION

Left to right.

SPECIAL CONDITIONS

The instruction is repeatable.

OUTLINE OF OPERATION

The N Register is examined. If zero, the instruction terminates. If not zero, the table address of the translated equivalent is developed as follows:

The 2^5, 2^4 and 2^3 bits of the character to be translated are converted to a numeric (0-7) which becomes the B_2 digit of the table address. The 2^2, 2^1 and 2^0 bits are converted to a numeric (0-7) which becomes the B_3 digit of the table address. The original B_0 and B_1 characters plus the newly developed B_2 and B_3 digits comprise the table address. The character at this address is read out of the translate table and transferred to the HSM location specified by the A Register. The A Register is incremented by one, N is decremented by one, and the cycle is repeated.

FINAL SETTINGS

$(A)_f$ = HSM location one to the right of the last character translated.

$(B)_f = (B)_i$

EXAMPLE

(501 to 3301 code conversion)

Instruction: A 2 8203 5700

HSM Before Execution:

8203	8204
1100001 ("B" in 501 Code)	1010100 ("1" in 501 Code)

Partial Table:

...	5724	...	5741	...	
	0000001		1010010		

Translation Process

B Address 5700 — Character 0 100 001

Table Address: 5 7 (B_0 B_1) — 4 1 (B_2 B_3)

HSM After Execution:

8203	8204
1010010 ("B" in 3301 Code)	0000001 ("1" in 3301 Code)

Final Settings: $(A)_f = 8205$ $(B)_f = 5700$

VI ARITHMETIC AND LOGICAL INSTRUCTIONS

GENERAL DESCRIPTION

This instruction performs decimal addition on four-character operands. It may be utilized to add two four-character addresses or to increment an address. Since addresses are always positive and since incrementing is a positive action, both operands should be positive. A positive sum is stored in the HSM locations originally occupied by the augend. Since the C_0C_1 characters of HSM addresses above 40,000 are not in ascending order by character, this instruction checks and, if necessary, makes the proper adjustment to C_1 to obtain the correct sum. Indirect addresses may be processed with this instruction.

FORMAT

OPERATION - +

N - +

A ADDRESS - HSM location of least significant digit (LSD) of the augend and sum.

B ADDRESS - HSM location of least significant digit (LSD) of the addend.

DIRECTION OF OPERATION

Right to left.

SPECIAL CONDITIONS

Instruction is repeatable.

PRI's are set.

OUTLINE OF OPERATION

The LSD of each operand is transferred from HSM and sent to the Arithmetic Unit. A sum is developed and inserted in the HSM location specified by the A Address. The A Register and B Register are decremented by one, and the cycle is repeated until the operation is performed four times. If there is no carry from the zone bits in the addition of the C_0 characters, the instruction terminates. If a carry results, the C_1 character of the sum is pulled out of HSM, and its zone bits are corrected by the addition of the carry bit from the zone bits of C_0.

If the result exceeds 159,999, an address equivalent to the excess over 160,000 is developed by a wrap-around to the beginning of HSM. For example, 130,000 plus 35,000 equals 5,000. When this occurs, the Overflow Indicator is set. If an indirect address is indicated by a "1" bit in the 2^4 position of the LSD of either operand, a "1" bit is generated in the corresponding position of the sum.

If either or both operands contain index bits, the result will contain the identical index bits. (Bits are "or" ed together.) For example, if the A operand specifies Index Field 1, and the B operand specifies Index Field 2, the result will specify Index Field 3.

FINAL SETTINGS

$(A)_f = (A)_i - 4$

$(B)_f = (B)_i - 4$

PRP is set if the sum is positive.

PRZ is set if the sum is zero.

EXAMPLE

Instruction: + + 8015 9704

HSM Before Execution:

8012	8013	8014	8015
3	Z	9	9

Numeric Equivalent	Internal Representation
123,999	3Z99
+ 0,010	+ 0010
124,009	4"09

HSM Before and After Execution:

9701	9702	9703	9704
0	0	1	0

HSM After Execution:

8012	8013	8014	8015
4	"	0	9

Final Settings: $(A)_f$ = 8011 $(B)_f$ = 9700 PRP is set.

GENERAL DESCRIPTION

This instruction performs decimal addition in accordance with algebraic rules, producing a sum, which is stored in the HSM locations originally occupied by the augend. Leading zeros are not suppressed in the sum. The two operands must be equal in length and may not exceed 45 characters per operand. Zone bits are ignored in any operand digit other than the least significant digit (LSD). A negative sum is indicated by the presence of a one bit in the 2^5 position of the LSD.

FORMAT

OPERATION - +

N - Number of characters (0-45) in each operand. See Appendix III.

A ADDRESS - HSM location of LSD of augend and sum.

B ADDRESS - HSM location of LSD of addend.

DIRECTION OF OPERATION

Right to left.

SPECIAL CONDITIONS

Instruction is repeatable.

PRI's are set.

Overflow conditions are handled as follows:

When adding single-character operands, the 2^4 bit in both operands will be ignored. If the add results in a carry, the 2^4 bit is not set in the sum, the Overflow Indicator is set, the Overflow Interrupt Indicator is set, and interrupt occurs.

When adding multi-character operands, if overflow occurs, the 2^4 bit of the most significant digit is not generated in the result, the Overflow Indicator is set, the Overflow Interrupt Indicator is set, and interrupt occurs.

OUTLINE OF OPERATION

The contents of the N Register are examined. If zero, the instruction terminates. If other than zero, the character specified by the A Register and the character specified by the B Register are fed into the Arithmetic Unit, and the resulting sum is stored back at the HSM location specified by the A Address. The A, B, and N Registers are decremented by one, and the cycle is repeated.

The sign of the sum is initially set to the sign of the augend. If the operands have unlike signs, the addend is complemented (10's complement), and addition occurs. The sum is cor-

rect unless the addend is larger than the augend in absolute value, in which case the result is recomplemented, and the sign is changed.

A one bit in the 2^4 position of the LSD of an operand will be carried into the corresponding bit position of the sum. This provides 301 Compatibility in handling indirect addresses of less than 40,000.

FINAL SETTINGS

$(A)_f$ = HSM location one to the left of the MSD of the sum.

$(B)_f$ = HSM location one to the left of the MSD of the addend.

PRP is set if the sum is positive.

PRZ is set if the sum is zero.

PRN is set if the sum is negative.

EXAMPLE

Instruction: + 5 6006 6012

HSM Before Execution:

6001	6002	6003	6004	6005	6006	6007	6008	6009	6010	6011	6012
A	4	2	5	0	3	T	0	8	9	7	1

HSM After Execution:

6001	6002	6003	6004	6005	6006	6007	6008	6009	6010	6011	6012
A	5	1	4	7	4	T	0	8	9	7	1

Final Settings: $(A)_f$ = 6001 $(B)_f$ = 6007 PRP is set.

GENERAL DESCRIPTION

This instruction performs decimal division with a sixteen-digit dividend and an eight digit divisor in accordance with algebraic rules producing an eight-digit quotient. The quotient is stored in the eight most significant character positions of the dividend. The remainder is stored in the eight least significant character positions of the dividend. Leading zeros are not suppressed in the quotient or remainder area. The LSD of the quotient contains the sign. The LSD of the remainder takes the sign of the dividend. The sign of the divisor is determined by its LSD. The sign of the dividend is positive unless one or more of the sixteen digits is negative.

The divisor must be larger in magnitude than the first 8 digits of the dividend. Fractional division is performed with the machine decimal point to the left of the MSD of the divisor, dividend and quotient. Shifting of operands for the division process and decimal point accounting are program responsibilities. Multiply/Divide locations of MMM are used in the division operation.

The sign of the quotient is determined by comparing the sign of the LSD of the divisor with the sign bit of each digit of the dividend. The sign of the quotient will be positive unless:

1. The sign of the LSD of the divisor is negative, and all dividend digits are positive, or

2. The sign of the LSD of the divisor is positive, and the sign of any dividend digit is negative.

Whenever the numeric portion of the nine most significant characters of the dividend is zero, the sign of the quotient and remainder will be positive and the PRI indicator will be set to zero. The numerical values of both the quotient and remainder will be correct.

FORMAT

OPERATION - +

N - . (Period)

A ADDRESS - HSM location of the LSD-8 of the dividend and the LSD of the quotient.

B ADDRESS - HSM location of the LSD of the divisor.

DIRECTION OF OPERATION

The quotient digits are placed in HSM left to right. The remainder digits are placed in HSM right to left.

SPECIAL CONDITIONS

The PRI's are set.

Except for use in determining sign, all zone bits will be stripped and ignored in the execution of the divide.

If the divisor is not larger in magnitude than the dividend, the Arithmetic Error Interrupt Indicator is set, and interrupt occurs. The dividend is destroyed but can be reconstructed (providing the operands are unequal) through programming by addition of the 9's complement of the dividend area (Ai-7 to Ai + 1) to the divisor. The sign of the dividend, as it appeared prior to the error, is indicated by the PRI's.

If the numeric portion of the character is other than 0-9, it may be possible to create the Arithmetic Error and Interrupt mentioned above, depending on the bit configuration of the two digits involved in the subtraction. Otherwise, the result will be invalid with no error condition indicated.

OUTLINE OF OPERATION

The logical sequence of the divide is as follows: The divisor is subtracted from the dividend one character at a time until a remainder is developed which is less than the divisor. A count is kept of the number of subtractions required and is used to form the initial digit of the quotient. At the completion of this cycle, the appropriate registers and counters are updated, the remainder is used to form a new dividend, and the cycle is repeated until the 8-digit quotient has been formed.

MICROMAGNETIC MEMORY USAGE

MD1 is initially set to the HSM location of the MSD of the remainder area. As each quotient digit is developed, MD1 is incremented by one and provides the HSM address for the LSD of portion of the dividend from which the divisor is to be subtracted.

MD3 maintains the HSM location of the dividend digit being processed. When the appropriate quotient digit is developed, the contents of MD3 are used as the storage address of the quotient digit in HSM.

MD4 is used to hold $(B)_i$ throughout the division process. This HSM address is the reference for the location of the LSD of the divisor when a subtraction cycle begins.

FINAL SETTINGS

$(A)_f = (A)_i$

$(B)_f = (B)_i - 9$

PRZ is set if the quotient equals zero.

PRN is set if the quotient is unequal to zero, and the signs of the operands are unequal.

PRP is set if the quotient is unequal to zero, and the signs of the operands are equal.

EXAMPLE #1 - DIVISION PROBLEM

Problem: $\frac{\$3120.00}{52} \quad \frac{\text{(Annual Salary)}}{\text{(\# of Weeks)}} = \$60.00$ Weekly Salary

Instruction: + . 5818 7007

HSM Before and After Execution:

7000	7001	7002	7003	7004	7005	7006	7007
5	2	0	0	0	0	0	0

HSM Before Execution:

	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
58	0	0	3	1	2	0	0	0	0	0	0	0	0	0	0	0

HSM After Execution:

	11	12	13	14	15	16	17	18	19	20	22	22	23	24	25	26
58	0	0	6	0	0	0	0	0	0	0	0	0	0	0	0	0

Final Settings: $(A)_f$ = 5818 $(B)_f$ = 6998 PRP is set.

PLACEMENT OF OPERANDS AND DECIMAL POINT DETERMINATION

In order to make the divisor larger in magnitude, "# of Weeks" was positioned in the divisor field left justified and "Annual Salary" was positioned in the dividend field right justified.

The number of digits between the problem decimal point and the machine decimal point of an operand is the Scale Factor (SF). Location of the problem decimal point in the quotient may be determined as follows:

Quotient SF = Dividend SF - Divisor SF

Divisor = * 52.000000 Dividend = * 003120.00 Quotient = * 0060.0000

* Machine decimal point Problem decimal point

EXAMPLE #2 - DIVISION WITH REMAINDER

Instruction: + . 5039 6012

HSM Before and After Execution:

6005	6006	6007	6008	6009	6010	6011	6012
6	5	7	0	8	2	6	0

HSM Before Execution:

	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
50	3	7	2	4	1	0	0	6	0	0	0	0	0	0	0	0

HSM After Execution:

	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
50	5	6	6	7	6	2	9	3	0	3	7	1	9	8	2	0

Final Settings: $(A)_f$ = 5039 $(B)_f$ = 6003 PRP is set.

EXAMPLE #3

Instruction: + . 6860 2008

HSM Before and After Execution:

	01	02	03	04	05	06	07	08
20	0	0	0	0	1	2	0	0

HSM Before Execution:

	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68
68	0	0	"	0	0	0	0	0	1	4	4	0	0	0	0	0

HSM After Execution:

	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68
68	0	0	0	1	2	0	0	-	0	0	0	0	0	0	0	-

Final Settings: $(A)_f$ = 6860 $(B)_f$ = 1998 PRN is set.

GENERAL DESCRIPTION

This instruction performs bit manipulation on a designated number of consecutive characters by extracting "1" bits from an original operand according to the bit configuration of a modifier. It operates on operands of equal length according to the rules specified under the "Outline of Operation" below.

FORMAT

OPERATION - T

N - Number of characters (0-45) in each operand. See Appendix III.

A ADDRESS - HSM location of rightmost character of the original operand and the result.

B ADDRESS - HSM location of rightmost character of the modifier.

DIRECTION OF OPERATION

Right to left.

SPECIAL CONDITIONS

PRI's are set

Instruction is repeatable

OUTLINE OF OPERATION

The N Register is examined, and if zero, the instruction terminates. If not zero, the character specified by the A Register is combined bit by bit with the character specified by the B Register. This bit manipulation is performed according to the following rules:

Bit in Original Operand	Bit in Modifier	Bit in Result
0	0	0
0	1	0
1	0	0
1	1	1

All six information bits of each operand enter the operation. The proper parity for each result character is generated as part of this instruction. The result of the combination is placed in the HSM location specified by the A Register. The A, B, and N Registers are decremented by one, and the cycle is repeated.

FINAL SETTINGS

$(A)_f$ = HSM location one to left of the leftmost character of the result.

$(B)_f$ = HSM location one to the left of the leftmost character of the modifier.

PRP is set if at least one of the information bits in the result is a one.

PRN is set if all the information bits in the result are zero.

EXAMPLE

Instruction: T 2 1001 1003

HSM Before Execution:

1000	1001	1002	1003
(0)	(P)	(7)	(V)
1 00 0000	1 10 0111	0 00 0111	1 11 0101

HSM After Execution:

1000	1001	1002	1003
(0)	(N)	(7)	(V)
1 00 0000	0 10 0101	0 00 0111	1 11 0101

Final Settings: $(A)_f$ = 0999 $(B)_f$ = 1001 PRP is set.

GENERAL DESCRIPTION

This instruction performs bit manipulation on a designated number of consecutive characters. It operates on operands of equal length according to the rules specified under the "Outline of Operation" below.

FORMAT

OPERATION - U

N - Number of characters (0-45) in each operand. See Appendix III.

A ADDRESS - HSM location of rightmost character of original operand and result.

B ADDRESS - HSM location of rightmost character of the modifier.

DIRECTION OF OPERATION

Right to left.

SPECIAL CONDITIONS

Instruction is repeatable.

OUTLINE OF OPERATION

The N Register is examined. If zero, the instruction terminates. If not zero, the character specified by the A Register is combined bit by bit with the character specified by the B Register. This bit manipulation is performed according to the following rules:

Bit in First Operand	Bit in Second Operand	Bit in Result
0	0	0
0	1	1
1	0	1
1	1	0

All six information bits of each operand enter the operation. The proper parity for each result character is generated as part of this instruction. The result of the combination is placed in the HSM location specified by the A Register. The A, B, and N Registers are decremented by one, and the cycle is repeated.

FINAL SETTINGS

$(A)_f$ = HSM location one to the left of the leftmost character of the result.

$(B)_f$ = HSM location one to the left of the leftmost character of the modifier.

EXAMPLE

Instruction: U 2 1003 1005

HSM Before Execution:

1002	1003	1004	1005
(0) 1 00 0000	(7) 0 00 0111	(S) 0 11 0010	(E) 0 01 0101

HSM After Execution:

1002	1003	1004	1005
(S) 0 11 0010	(B) 1 01 0010	(S) 0 11 0010	(E) 0 01 0101

Final Settings: $(A)_f$ = 1001 $(B)_f$ = 1003

GENERAL DESCRIPTION

This instruction performs bit manipulation on a designated number of consecutive characters by inserting "1" bits from a modifier into the original operand. It operates on equal length operands according to the rules specified under the "Outline of Operation" below.

FORMAT

OPERATION - Q

N - Number of characters (0-45) in each operand. See Appendix III.

A ADDRESS - HSM location of rightmost character of original operand and result.

B ADDRESS - HSM location of rightmost character of the modifier.

DIRECTION OF OPERATION

Right to left.

SPECIAL CONDITIONS

Instruction is repeatable.

OUTLINE OF OPERATION

The N Register is examined. If zero, the instruction terminates. If not zero, the character specified by the A Register is combined bit by bit with the character specified by the B Register. This bit of manipulation is performed according to the following rules:

Bit in Original Operand	Bit in Modifier	Bit in Result
0	0	0
0	1	1
1	0	1
1	1	1

All six information bits of each operand enter the operation. The proper parity for each result character is generated as part of this instruction. The result of the combination is placed in the HSM location specified by the A Register. The A, B, and N Registers are decremented by one, and the cycle is repeated.

FINAL SETTINGS

$(A)_f$ = HSM location one to the left of the leftmost character of the result.

$(B)_f$ = HSM location one to the left of the leftmost character of the modifier operand.

EXAMPLE

Instruction: Q 2 4003 4005

HSM Before Execution:

4002	4003	4004	4005
(0) 1 00 0000	(7) 0 00 0111	(1) 0 00 0001	(E) 0 01 0101

HSM After Execution:

4002	4003	4004	4005
(1) 0 00 0001	(G) 1 01 0111	(1) 0 00 0001	(E) 0 01 0101

Final Settings: $(A)_f$ = 4001 $(B)_f$ = 4003

GENERAL DESCRIPTION

This instruction performs decimal multiplication on eight-character, fixed-length operands in accordance with algebraic rules producing a 16-digit product. Leading zeros are not suppressed in the product. The most significant eight digits of the product are stored at the B Address. The least significant eight digits are stored in the HSM locations immediately to the right of the B Address. An absolute add to the entire product may be specified by storing a numeric quantity in the least significant eight digits only of the product area. If an absolute add is not desired, the eight locations to the right of the B Address must be zero filled. The sign of the product is indicated by the 2^5 bit of both the least significant digit (LSD) of the B Address result and the LSD of the eight-character portion of the result stored to the right of the B Address. A zero product is developed as a positive, 16-digit product. The Multiply/Divide locations of MMM are used in the multiplication operation.

FORMAT

OPERATION - +

N - $

A ADDRESS - HSM location of the LSD of the multiplicand.

B ADDRESS - HSM location of the LSD of the multiplier and the LSD of the eight most significant digits of the product.

DIRECTION OF OPERATION

Right to left.

SPECIAL CONDITIONS

PRI's are set.

If invalid operands are used, the following occurs:

1. The sign of the result is determined by comparing the sign of the LSD of the multiplicand with the sign bit of each digit of the multiplier. The sign of the product will be positive unless; (1) the sign of the LSD of the multiplicand is negative, and all multiplier digits are positive; or (2) the sign of the LSD of the multiplicand is positive, and the sign of any multiplier digit is negative.

2. Except for use in determination of sign, all zone bits are stripped and ignored in the execution of the multiply. An exception situation occurs when the multiplier contains zeros in the least significant positions. In this case the corresponding least significant digits of the product will be unchanged from their pre-executed state except the LSD.

3. If the numeric portion (2^0-2^3) of the character is other than 0-9, the resulting product is invalid, and no error condition is indicated.

OUTLINE OF OPERATION

The logical sequence of the multiply is as follows: The LSD of the multiplier is examined. If less than six, the eight-digit multiplicand is added, a single digit at a time using the one-character adder, to the least significant positions of the product area a number of times equal to the multiplier digit. If the LSD of the multiplier is greater than five, the multiplicand is effectively multiplied by ten by a carry to the next multiplier digit, and the multiplicand is subtracted from the product a number of times equivalent to the difference between the multiplier digit and 10.

At the completion of this cycle, the appropriate registers and counters are updated so that the next digit of the multiplier and the proper position of the partial product are indicated. The cycle repeats itself until all eight digits of the multiplier are exhausted and the entire 16-digit product has been formed.

MICRO MAGNETIC MEMORY USAGE

MD1 is initially set to the HSM address of the LSD of the product (Bi + 8). As each multiplier digit is exhausted, MD1 is decremented by one and provides the HSM address for the LSD of each new partial product.

MD2 contains the address of the LSD of the 16-digit product throughout the multiplication process. MD2 provides a reference to the LSD of the product in case a minus zero result develops, in which case the minus sign in the LSD is changed to a plus sign.

MD3 is initially set to the address specified by MD1 when a new multiplier digit is brought into the process. As each digit of the multiplicand is added into or subtracted from the partial product, MD3 is decremented by one. This process continues until the respective partial product is finished.

MD4 holds the initial A Address throughout the multiplication process. This address is the reference for the location of the LSD of the multiplicand each time a new multiplier digit enters the operation.

FINAL SETTINGS

$(A)_f = (A)_i - 8$ if multiplier is not zero.

$(A)_f = (A)_i$ if multiplier is zero.

$(B)_f = (B)_i - 8$.

PRZ is set if the product equals zero.

PRP is set if the product is unequal to zero, and the signs of the operands were equal.

PRN is set if the product is unequal to zero, and the signs of the operands were unequal.

EXAMPLE

Instruction: + $ 8518 9357

HSM Before and After Execution:

8511	8512	8513	8514	8515	8516	8517	8518
0	0	1	1	1	1	1	1

HSM Before Execution:

	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65
93	0	0	2	2	2	2	2	2	0	0	0	0	0	0	0	1

HSM After Execution:

	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65
93	0	0	0	0	0	2	4	6	9	1	3	0	8	6	4	3

Final Settings: $(A)_f$ = 8510 $(B)_f$ = 9349 PRP is set.

SUBTRACT ADDRESS (SAD)

GENERAL DESCRIPTION

This instruction performs decimal subtraction on four-character operands. It may be utilized to subtract two four-character addresses, or to decrement an address. Both operands should be positive. The difference is stored in the HSM locations originally occupied by the minuend. Since the C_0C_1 characters of HSM addresses above 40,000 are not in ascending order by character, this instruction checks, and if necessary, makes the proper adjustment to C_1 to obtain the correct difference. This instruction will handle indirect addresses.

FORMAT

OPERATION - - (minus)

N - +

A ADDRESS - HSM location of least significant digit (LSD) of the minuend and difference.

B ADDRESS - HSM location of least significant digit (LSD) of the subtrahend.

DIRECTION OF OPERATION

Right to left.

SPECIAL CONDITIONS

Instruction is repeatable.

PRI's are set.

OUTLINE OF OPERATION

The LSD of each operand is transferred from HSM and sent to the Arithmetic Unit. A difference is developed and inserted into the HSM location specified by the A Address. The A Register and B Register are decremented by one, and the cycle is repeated until the operation is performed four times. If there is no carry from the zone bits in the development of the C_0 character of the difference, the instruction terminates. If a carry results, the C_1 character of the difference is pulled out of HSM, and its zone bits adjusted by the carry bit from the zone bits of C_0.

When the difference of the operands normally would create a result less than zero, the actual result produced will be in the form of a wrap-around address to the top of HSM. For example, 20,000 minus 30,000 equals 150,000. This sets the Overflow Indicator. If an indirect address is indicated by a "1" bit in the 2^4 position of the LSD of either operand, a "1" bit is generated in the corresponding position of the sum.

If either or both operands contain bits, the result will contain the identical index bits. (Bits are "or" ed together.) For example, if the A operand specifies Index Field 1, and the B operand specifies Index Field 2, the result will specify Index Field 3.

FINAL SETTINGS

$(A)_f = (A)_i - 4$

$(B)_f = (B)_i - 4$

PRP is set if the difference is positive.

PRZ is set if the difference is zero.

PRN is set if the difference is a wrap-around address.

EXAMPLE

Instruction: – + 8015 9704

HSM Before Execution:

8012	8013	8014	8015
4	"	0	9

HSM Before and After Execution:

9701	9702	9703	9704
0	0	1	0

	Numeric Equivalent	Internal Representation
	124,009	4"09
	– 0,010	–0010
	123,999	3Z99

HSM After Execution:

8012	8013	8014	8015
3	Z	9	9

Final Settings: $(A)_f$ = 8011 $(B)_f$ = 9700

SUBTRACT DATA (SDT)

GENERAL DESCRIPTION

This instruction performs decimal subtraction in accordance with algebraic rules, producing a difference, which is stored in the HSM locations originally occupied by the minuend. Leading zeros are not suppressed in the difference. The two operands must be equal in length, and may not exceed 45 characters per operand. Zone bits are ignored in any operand digit other than the least significant digit (LSD) and most significant digit (MSD). A negative difference is indicated by the presence of a one bit in the 2^5 position of the LSD.

FORMAT

OPERATION - - (Minus)

N - Number of characters (0-45) in each operand. See Appendix III.

A ADDRESS - HSM location of LSD of minuend and difference.

B ADDRESS - HSM location of LSD of the subtrahend.

DIRECTION OF OPERATION

Right to left.

SPECIAL CONDITIONS

Instruction is repeatable.

PRI's are set.

Overflow conditions are handled as follows:

When subtracting single character operands, the 2^4 bit in both operands will be ignored. If the subtract results in a carry, the 2^4 bit is not set in the difference, the Overflow Indicator is set, the Overflow Interrupt Indicator is set, and interrupt occurs. If overflow occurs when subtracting multi-character operands, the 2^4 bit of the most significant digit is not generated in the result, the Overflow Indicator is set, the Overflow Interrupt Indicator is set and interrupt occurs.

OUTLINE OF OPERATION

The contents of the N Register are examined. If zero, the instruction terminates. If other than zero, the character specified by the A Register and the character specified by the B Register are fed into the Arithmetic Unit, and the resulting difference is stored back at the HSM location specified by the A ADDRESS. The A, B, and N Registers are decremented by one, and the cycle is repeated.

The sign of the difference is initially set to the sign of the minuend. If the operands have like signs, the 10's complement of the subtrahend is added to the minuend. The result is correct

unless the subtrahend was larger in absolute value, in which case the result is recomplemented, and the sign is changed. If the operands have unlike signs, the operands are added.

A one bit in the 2^4 position of the LSD of an operand will be carried in the corresponding bit position of the difference. This provides 301 compatibility in handling indirect addresses of less than 40,000.

FINAL SETTINGS

$(A)_f$ = HSM location one to the left of the MSD of the difference.

$(B)_f$ = HSM location one to the left of the MSD of the subtrahend.

PRP is set if the difference is positive.

PRZ is set if the difference is zero.

PRN is set if the difference is negative.

EXAMPLE

Instruction: – 5 6006 6012

HSM Before Execution:

6001	6002	6003	6004	6005	6006	6007	6008	6009	6010	6011	6012
A	4	2	5	0	3	T	0	8	9	7	1

HSM After Execution:

6001	6002	6003	6004	6005	6006	6007	6008	6009	6010	6011	6012
A	3	3	5	3	2	T	0	8	9	7	1

Final Settings: $(A)_f$ = 6001 $(B)_f$ = 6007 PRP is set.

VII DECISION AND CONTROL INSTRUCTIONS

GENERAL DESCRIPTION

This instruction determines the relative magnitude of two HSM addresses and indicates the result of this comparison by setting one of the Previous Result Indicators. Subtraction is performed on two four-character operands, but the difference is not returned to HSM. Since the C_0C_1 characters of HSM addresses above 40,000 are not in ascending order by character, this instruction checks and, if necessary, makes the proper adjustment to C_1 in determining the relative magnitude.

FORMAT

OPERATION - - (minus)

N - (period)

A ADDRESS - HSM location of rightmost character of minuend.

B ADDRESS - HSM location of rightmost character of subtrahend.

DIRECTION OF OPERATION

Right to left.

SPECIAL CONDITIONS

Instruction is repeatable.

Although addresses should always be positive, negative operands may be processed. The following chart indicates the resulting PRI settings based upon the size and sign of the operands:

	A > B		A = B		A < B	
	B–	B+	B–	B+	B–	B+
A –	PRN	PRN	PRZ	PRN	PRP	PRN
A +	PRP	PRP	PRP	PRZ	PRP	PRN

OUTLINE OF OPERATION

One character from each operand is transferred from HSM into the Arithmetic Unit where a subtraction is performed. The subtraction is performed four times. The PRI's are set, but the result is not stored back into HSM.

FINAL SETTINGS

$(A)_f = (A)_i - 4$

$(B)_f = (B)_i - 4$

PRI settings are as follows if the sign of both operands is positive:

PRP is set if the contents of A are greater than the contents of B.

PRN is set if the contents of A are less than the contents of B.

PRZ is set if the contents of A are equal to the contents of B.

EXAMPLE

Instruction: – . 7786 7780

HSM Before and After Execution:	7777	7778	7779	7780	7781	7782	7783	7784	7785	7786
	F	2	3	4	M	6	F	2	2	8

Final Settings: $(A)_f$ = 7782 $(B)_f$ = 7776 PRN is set.

GENERAL DESCRIPTION

This instruction is used to determine the relative magnitude of two operands of equal length. Neither operand is altered by the operation. The instruction terminates upon an unequal character comparison, or when N is exhausted. The resulting PRI settings permit alternate sequence of action.

FORMAT

OPERATION - Y

N - Number of characters (0-45) to be compared. See Appendix III.

A ADDRESS - HSM location of leftmost character of first operand.

B ADDRESS - HSM location of leftmost character of second operand.

DIRECTION OF OPERATION

Left to right.

SPECIAL CONDITIONS

PRI's are set.

OUTLINE OF OPERATION

Initially PRZ is set. The N Register is examined. If zero, the instruction terminates. If not zero, the character specified by the A Register is compared with the character specified by the B Register. If the characters are equal, the A and B Registers are incremented by one, the N Register is decremented by one, and the cycle is repeated. If the character specified by the A Register is larger than the character specified by the B Register, the A and B Registers are incremented by one, PRP is set, and the instruction terminates. If the character specified by the A Register is smaller than the character specified by the B Register, the A and B Registers are incremented by one, PRN is set, and the instruction terminates.

FINAL SETTINGS

$(A)_f$ = HSM location one to the right of the last character compared in the first operand.

$(B)_f$ = HSM location one to the right of the last character compared in the second operand.

PRP is set if the contents of A is greater than the contents of B.

PRN is set if the contents of A is less than the contents of B.

PRZ is set if the contents of A is equal to the contents of B.

EXAMPLE

Instruction: Y 5 2000 2006

HSM Before and After Execution:	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010
	1	2	4	5	6	–	1	2	3	6	9

Final Settings: $(A)_f = 2003$ $(B)_f = 2009$ PRP is set.

GENERAL DESCRIPTION

This instruction senses the condition of an indicator and chooses one of three possible instruction sequences to follow depending upon the condition encountered. The Previous Result, EF/ED, Overflow, Simo 1 and Simo 2 Indicators and the Alteration Switches can be sensed individually by this instruction. The A Address, B Address and, if required, the next instruction in sequence are used to specify the alternate sequences. Sensing the EF/ED Indicators applies only for Magnetic Tape Devices and is included here for 301 compatibility purposes (See TDV instruction).

FORMAT

OPERATION - W

N - Designates indicator or switch to be sensed.

A and B
ADDRESSES - Address of next instruction to be processed when the condition specified exists.

INDICATOR OR SWITCH	N	A ADDRESS	B ADDRESS	NEXT INSTRUCTION
Previous Result	1	PRP Set	PRN Set	PRZ Set
Previous Result Zero	+ (Plus)	PRZ Set	Zero (0000)	PRZ Not Set
Overflow	2	Set	Not Set	
Simo 1	4	Read in process	Write in process	Mode unoccupied
Simo 2	$	Read in process	Write in process	Mode unoccupied
Simo 1 EF/ED	– (Minus)	Set	Not Set	
Simo 2 EF/ED	8	Set	Not Set	
Alteration Switch #1	A	Set	Not Set	
Alteration Switch #2	]	Set	Not Set	
Alteration Switch #3	#	Set	Not Set	
Alteration Switch #4	&	Set	Not Set	

SPECIAL CONDITIONS

STP is performed if the condition specified by the A or B Address is present.

OUTLINE OF OPERATION

The N character is examined. The condition is sensed and if the third condition (specified under Next Instruction) is present the instruction terminates. If the first or second conditions (specified under A Address and B Address) are present then the contents of either the A or B Register, as indicated above, are transferred to the P Register after the contents of the P Register are transferred to STP.

FINAL SETTINGS

$A_f = A_i$

$B_f = B_i$

GENERAL DESCRIPTION

This instruction controls and implements the operation of the Interrupt System.

FORMAT

OPERATION - [(Open Bracket)

N - Specifies function to be performed as follows:

SYMBOL	FUNCTION
]	Set General Inhibit
0 (Zero)	Set General/Real-Time Inhibit
1	Remove General/Real-Time Inhibit
#	Remove Real-Time Inhibit
- (Minus)	Return After Interrupt (RAI)
+	Set 301 Compatibility Mode (20K)
&	Set 301 Compatibility Mode (40K)
(Period)	Remove 301 Compatibility Mode
$	Set Program Test Mode
A	Remove Program Test Mode

A ADDRESS - Zero (0000). Not to be used by programming.

B ADDRESS - Zero (0000). Not to be used by programming.

OUTLINE OF OPERATION

The N Register is examined, and the function indicated is performed as follows:

1. If N =] (Close Bracket) interrupt is inhibited on all General Interrupt conditions. Any General Interrupt condition will set the designated Interrupt Indicator, but interrupt will not occur until the inhibit has been removed.

2. If N = 0 (Zero), interrupt is inhibited on all General and Real-Time conditions. Any General or Real-Time Interrupt condition will set the designated Interrupt Indicator, but interrupt will not occur until the inhibit has been removed.

3. If N = 1, the inhibit on General and Real-Time Interrupt conditions is removed. Any General or Real-Time Interrupt Indicators either already set or set subsequently will cause interrupt.

4. If N = # (Number), the inhibit on Real-Time Interrupt conditions is removed. Any Real-Time Interrupt Indicators already set or set subsequently will cause interrupt.

5. If N = - (Minus), all registers and indicators that were stored in the standard locations of the Micro Magnetic Memory at the time of interrupt will be restored to their pre-interrupted condition. The Micro Magnetic Memory area utilized to restore the Processor is determined by the present status of the Real-Time Inhibit. The corresponding inhibit is also removed.

6. If N = + (Plus), the 301 Compatibility Mode (20K) is set. This causes the Processor to interrupt prior to execution of each I/0 instruction by setting the 301 Compatibility Interrupt Indicator. The Compatibility Routine then handles the execution of the I/0 instruction. This causes the data add and subtract instructions to function differently also (see 301 Compatibility Section). If interrupt is prohibited, the interrupt bit will not be set. Overflow handling will be in the 3301 Mode.

7. If N = & (ampersand), the 301 Compatibility Mode (40K) is set.

8. If N = . (Period), the 301 Compatibility Mode is removed.

9. If N = $ (Dollar), the Processor is conditioned so that every instruction, with the exception of the CIL instruction specifying the Return After Interrupt (RAI) function, sets the Program Test Interrupt Indicator and causes interrupt to occur after execution of that instruction. Unless inhibited, interrupt occurs at the end of the CIL instruction specifying this option. If interrupt is prohibited, the interrupt bit will not be set.

10. If N = A, the Program Test mode is removed.

FINAL SETTINGS

$(A)_f = (A)_i$

$(B)_f = (B)_i$

GENERAL DESCRIPTION

This instruction inhibits any further instructions from entering the registers for execution. If the Input/Output Modes are unoccupied, the computer stops immediately. If any of these modes are occupied, the instruction(s) will be completed before stopping.

FORMAT

OPERATION - . (Period)

N - . (Period)

A ADDRESS - Unused. May contain any legitimate address.

B ADDRESS - Unused. May contain any legitimate address.

FINAL SETTINGS

$(A)_f = (A)_i$

$(B)_f = (B)_i$

LOAD REGISTER (LDR)

GENERAL DESCRIPTION

This instruction places the contents of four consecutive HSM locations (two diads) into a specified Micro Magnetic Memory location.

FORMAT

OPERATION - C_R (Credit)

N - Symbol for specific MMM location as follows:

LOCATION SYMBOL	CONTENTS OF MMM LOCATION	LOCATION SYMBOL	CONTENTS OF MMM LOCATION
1	P Register	G	STPR (Real-Time Interrupt)
2	A Register	I	General Interrupt Routine Entry
4	B Register	+	A (Simo 1 Instruction)
5	T Register	.	O and N (Simo 1 Instruction)
6	C Register	;	B (Simo 1 Instruction)
7	E Register	:	Multiply/Divide (MD1)
8 (or 3)	S Register	,	Multiply/Divide (MD2)
9	P (General Interrupt)	C_R	Multiply/Divide (MD3)
¬	A (General Interrupt)	J	Multiply/Divide (MD4)
#	STA (General Interrupt)	K	A (Simo 2 Instruction)
@	B (General Interrupt)	L	O and N (Simo 2 Instruction)
(	STP (General Interrupt)	M	B (Simo 2 Instruction)
)	Control Register (General Interrupt)	R	Stop P (P Address on Stop)
e	STPR (General Interrupt)	S	Index Field 1
A	P (Real-Time Interrupt)	T	Increment Field 1
B	A (Real-Time Interrupt)	U	Index Field 2
C	STA (Real-Time Interrupt)	V	Increment Field 2
D	B (Real-Time Interrupt)	W	Index Field 3
E	STP (Real-Time Interrupt)	X	Increment Field 3
F	Control Register (Real-Time Interrupt)	Z	Real-Time Interrupt Routine Entry

A ADDRESS - HSM location of rightmost diad of the two diads which contain the contents to be stored in the MMM location.

B ADDRESS - Zero (0000), or may be used for address constants.

DIRECTION OF OPERATION

Right to left.

OUTLINE OF OPERATION

The contents of the HSM diad addressed by the A Register are stored temporarily in the D Register. The A Address is decremented by two. The contents of the HSM diad now addressed by the A Register and the contents of the D Register are placed in the MMM location designated by the N Register.

The contents of the B Address are accessed and indexing and indirect addressing are performed if the bits are present in the C_2, C_3 characters. If other than address constants are stored in the B address, a Systems Error interrupt may occur.

FINAL SETTINGS

$(A)_f = (A)_i - 2$ if other than A is set.

$(A)_f$ = the contents of HSM as originally addressed by A if A is set.

$(B)_f = (B)_i$ if other than B is set.

$(B)_f$ = the contents of HSM as originally addressed by A if B is set.

EXAMPLE

Instruction: C_R S 6009 0000

Index Field 1 (After Execution): 2450

HSM Before and After Execution:

6006	6007	6008	6009
2	4	5	0

Final Settings: $(A)_f$ = 6007 $(B)_f$ = 0000

PROGRAMMED INTERRUPT (PIN)

GENERAL DESCRIPTION

This instruction causes interrupt by setting the Programmed Interrupt Indicator. Control is transferred to the HSM address specified in the Jump P (Interrupt Routine entry) location of the Micro Magnetic Memory. If either inhibit is set, the next instruction is accessed.

FORMAT

OPERATION - . (Period)

N - Any symbol except a period.

A ADDRESS - Unused. May contain any legitimate address.

B ADDRESS - Unused. May contain any legitimate address.

FINAL SETTINGS

$(A)_f = (A)_i$

$(B)_f = (B)_i$

GENERAL DESCRIPTION

This instruction causes a repeatable instruction to be repeated a specified number of times.

FORMAT

OPERATION - R

N - Number of repeats (0-15). See Appendix IV.

A ADDRESS - If zero (0000) or even, the A Address of a repeatable instruction is not put in the A Register except for the initial execution. If one (0001) or odd, the A Address of a repeatable instruction is put in the A Register each time the instruction is repeated.

B ADDRESS - If zero (0000) or even, the B Address of a repeatable instruction is not put in the B Register except for the initial execution. If one (0001) or odd, the B Address of a repeatable instruction is put in the B Register each time the instruction is repeated.

OUTLINE OF OPERATION

The N character is transferred to the Repeat Register. The contents of the P Register are transferred to 0222-0225, the standard HSM location for storing P in a RPT instruction (STPR). Indicators are set as denoted in the RPT instruction's A and B Addresses specifying whether or not the A and B Addresses of the repeatable instruction are to be put into their respective registers. The instruction following the RPT instruction is put into the registers and executed disregarding the settings of the indicators.

The Repeat Register is examined. If zero, the indicators are reset, and the next instruction is executed. If other than zero, the Repeat Register is decremented by one, and the contents of the HSM locations 0222-0225 (STPR) are transferred to the P Register. The instruction immediately following the RPT instruction is put into the registers as specified by the indicators and is executed. The Repeat Register is examined again and the cycle is repeated.

Non-repeatable instructions may exist between the Repeat and the repeatable instructions.

SCAN INTERRUPT (SIN)

GENERAL DESCRIPTION

This instruction scans the Interrupt Indicators and generates an address constant associated with the first indicator set that was not masked out. After execution the A Register and STA will contain an address for the specific Interrupt Indicator by generating into A_1 A_2 a decimal count representing the symbol for a specific Interrupt Indicator. All Interrupt Indicators, 01-18, may be scanned or a partial scan of indicators, 07-18 or 13-18, is available. Through the use of an Inhibit Mask, indicators that are not to be scanned may be disregarded.

FORMAT

OPERATION - < (Less)

N - Designates the Interrupt Indicators to be scanned as follows:

N = 1 Scan Indicators 13 through 18.

N = 2 Scan Indicators 07 through 18.

N = 3 Scan Indicators 01 through 18.

A ADDRESS - A_0 is set initially by the programmer.

A_1 A_2 A_3 - Zero (000). Not to be used by programming.

B ADDRESS - HSM location of the leftmost character of the Inhibit Mask. The number of characters comprising the mask must equal the N Character count.

The Interrupt Indicators are as follows:

SYMBOL	CONDITION	SYMBOL	CONDITION
01	Systems Error	10	301 Compatibility
02	CMC Service Request	11	Busy or Inoperable
03	Reserved for Future Enhancement	12	Simo 3 Terminated Abnormally
04	External Interrupt	13	Simo 2 Terminated Abnormally
05	Console Request	14	Simo 1 Terminated Abnormally
06	Programmed Interrupt	15	Simo 3 Terminated Normally
07	Arithmetic Error	16	Simo 2 Terminated Normally
08	Overflow	17	Simo 1 Terminated Normally
09	Off-Line Operation Complete	18	Program Test

Note: Interrupt Indicators 12 and 15 are used by Simo 3 Mode (optional).

DIRECTION OF OPERATION

Interrupt Indicators are compared in ascending sequence by decimal count. The Inhibit Mask character(s) and bits within the Mask character(s) are compared left to right.

SPECIAL CONDITIONS

STA is performed.

OUTLINE OF OPERATION

The specified Interrupt Indicators are compared bit by bit with the information bits of the Inhibit Mask. A "1" bit is present in the respective Interrupt Indicator when the condition listed above exists. If the scan is completed without a "1" bit in an Indicator being compared with a "0" bit in the mask, A_1 A_2 then contain their original contents. If a "1" bit in an indicator is compared with a "0" bit, the corresponding indicator will be reset to "0", a two-digit decimal count equivalent to the indicator symbol is generated and placed in the A_1 A_2 positions of the A Register (destroying its original contents), and the instruction terminates. If a "1" bit in an indicator is compared with a "1" bit in the mask, the corresponding indicator remains set, and the instruction continues to scan. The B Register is incremented by one, and the N Register is decremented by one as each set of six Interrupt Indicators is processed. The instruction terminates when N equals zero.

FINAL SETTINGS

$(A_0)_f = (A_0)_i$

$(A_3)_f = (A_3)_i$

$(A_1A_2)_f$ - The decimal count of the first non-masked Interrupt Indicator found to be set.

$(A_1A_2)_f$ = Zero (00), if no Interrupt Indicators were set, or all indicators that were set were masked.

$(B)_f$ = HSM location one to the right of the mask character in which the first indicator was set but not masked; HSM location one to the right of the LSC of the Inhibit Mask if no indicators were set, or all indicators that were set were masked out.

EXAMPLE

Instruction: < 2 4000 6031

Indicators and Contents Before Execution:

07	08	09	10	11	12	13	14	15	16	17	18
0	0	1	0	0	0	0	1	0	1	0	0

HSM Before and After Execution:

6031	6032
(8)	(0)
0 001000	1 000000

Indicators and Contents After Execution:

07	08	09	10	11	12	13	14	15	16	17	18
0	0	1	0	0	0	0	0	0	1	0	0

Final Settings: $(A)_f$ = 4140 $(B)_f$ = 6033

GENERAL DESCRIPTION

This instruction takes the contents of a specified four-character location within Micro Magnetic Memory and places them into four consecutive HSM locations (two diads).

FORMAT

OPERATION - V

N - Symbol for specific MMM location as follows:

LOCATION SYMBOL	CONTENTS OF MMM LOCATION	LOCATION SYMBOL	CONTENTS OF MMM LOCATION
1	P Register	G	STPR (Real-Time Interrupt)
2	A Register	I	General Interrupt Routine Entry
4	B Register	+	A (Simo 1 Instruction)
5	T Register	.	O and N (Simo 1 Instruction)
6	C Register	;	B (Simo 1 Instruction)
7	E Register	:	Multiply/Divide (MD1)
8 (or 3)	S Register	,	Multiply/Divide (MD2)
9	P (General Interrupt)	C_R	Multiply/Divide (MD3)
¬	A (General Interrupt)	J	Multiply/Divide (MD4)
#	STA (General Interrupt)	K	A (Simo 2 Instruction)
@	B (General Interrupt)	L	O and N (Simo 2 Instruction)
(	STP (General Interrupt)	M	B (Simo 2 Instruction)
)	Control Register (General Interrupt)	R	Stop P (P Address on Stop)
e	STPR (General Interrupt)	S	Index Field 1
A	P (Real-Time Interrupt)	T	Increment Field 1
B	A (Real-Time Interrupt)	U	Index Field 2
C	STA (Real-Time Interrupt)	V	Increment Field 2
D	B (Real-Time Interrupt)	W	Index Field 3
E	STP (Real-Time Interrupt)	X	Increment Field 3
F	Control Register (Real-Time Interrupt)	Z	Real-Time Interrupt Routine Entry

A ADDRESS - Address of rightmost diad of the two diads, which is to receive the contents of the MMM location specified by N. When the A Register is selected, the contents of the A Register left by the previous instruction are stored in STA, and the A Address of this instruction is zero or may be used for direct address constants.

B ADDRESS - HSM address of next instruction to be executed if P is being stored. If P is not being stored, the B address is zero (0000) and may be used for storing address constants. If B is stored, only direct address constants may be stored in the B Address.

DIRECTION OF OPERATION

Right to left.

OUTLINE OF OPERATION

The contents of the designated MMM location are stored appropriately. If N selects the P Register, the P Register is stored in the location specified by the A Register, and the contents of the B Register are sent to the P Register.

When any register other than A is stored, the results are stored in the location designated by the A Register contents. When the B Register is selected, the contents of the B Register resulting from the previous instruction are stored. When the A Register is selected, the contents of the A Register resulting from the previous instruction are stored in STA.

When the S or C Register is selected, the rightmost diad of the selected register is placed in the location specified by the A Register. (If an I/O instruction is being executed, the contents of the S or C Register, respectively, may vary before the leftmost diad is stored.

Except when storing the A or B Registers, the contents of the A and B addresses are accessed and indexing and indirect addressing are performed if the bits are present in the C_2, C_3 characters. If, during storing A or B Registers, these bits are present in an address constant, the contents of the specified Register (A or B) are destroyed, and a Systems Error interrupt may occur. If other than address constants are stored in these addresses, a Systems Error interrupt may occur.

If the 301 Compatibility Switch is set and N equal 2 or 4, the instruction will terminate before execution. The 301 Compatibility indicator will be set, and interrupt will occur.

FINAL REGISTER CONTENT

$(A)_f = (A)_i - 2$ if other than A is stored.

$(A)_f = (A)_f$ of previous instruction if A is stored.

$(B)_f = (B)_i$ if other than A or B is stored.

$(B)_f = (B)_f$ of previous instruction if A or B is stored.

EXAMPLE

Instruction: V 4 6009 0000

B Register Contents: 2450

HSM Before Execution:

6006	6007	6008	6009
1	5	6	5

HSM After Execution:

6006	6007	6008	6009
2	4	5	0

Final Settings: $(A)_f = 6007$ $(B)_f = 2450$

GENERAL DESCRIPTION

The Tally instruction decrements a two-character, decimal counter (tally quantity) by one each time the instruction is executed. Incrementing of an Index Field by its associated Increment Field as specified by N is also provided. All three, or any combination of Index Fields, may be incremented by a single Tally instruction. Incrementing may be performed independently or in conjunction with the Tally function. When the tally function is specified, control is transferred to a specified instruction address until the counter is zero. It permits looping through a preceding sequence of instructions by automatically reducing the prestored tally quantity each time control is transferred to the beginning of the sequence. When the tally quantity has been exhausted, the Tally ends, and the instruction following it is performed. The tally quantity must be initialized prior to cycling through the instruction loop. The maximum value of the tally quantity, always a positive numeric, is 99.

FORMAT

OPERATION - X

N - Specifies incrementing options as follows:

$2^0 = 0$ Index Field incrementing and/or Tally function.

$2^0 = 1$ Index Field incrementing only.

Incrementing Option	Bit Position		
	2^5	2^4	2^3
No incrementing required	0	0	0
Increment Index Field 1	0	0	1
Increment Index Field 2	0	1	0
Increment Index Field 3	1	0	0

A ADDRESS - HSM location of diad containing the quantity to be tested.

B ADDRESS - HSM location of the next instruction to be performed if the quantity being tested has not been exhausted.

Unused bit and character positions must be zero and are not to be used by programming.

SPECIAL CONDITIONS

STP is performed only on the transfer of control.

OUTLINE OF OPERATION

The N Register is examined and if $2^{\circ} = 0$, the two-character tally quantity is examined and if equal to "00", the instruction terminates. If other than "00", the tally quantity is decremented by one and stored in the HSM address indicated by the A Register. The P register is stored in STP, and the B Register is transferred to the P Register. If 2^3, 2^4 and 2^5 of N are all "zeros", the instruction terminates. If indexing is specified, the Index Field or fields are incremented by the contents of their corresponding Increment Fields.

If upon examination of the N Register $2^{\circ} = 1$, the instruction ignores the Tally function, performs the Index Field incrementing in accordance with 2^5 2^4 2^3 of the N character, and then drops through to execute the next instruction in sequence. STP is stored during execution. The A and B addresses should contain zeros.

Indexing and incrementing utilize a four-character adder designed to operate in accordance with the 3301 addressing scheme. The adder performs addition only and cycles on 160,000 regardless of the physical size of HSM.

FINAL SETTINGS

$(A)_f = (A)_i$

$(B)_f = (B)_i$

EXAMPLE

Instruction: X & 1020 9000

Description	Before Execution	After Execution
HSM locations 1020 and 1021	09	08
Index Field 2	1030	1150
Increment Field 2	0120	0120

Final Settings: $(A)_f = 1020$ $(B)_f = 9000$

GENERAL DESCRIPTION

This instruction causes an unconditional break in the sequence of instructions. Control is transferred to the instruction location specified by the B Address. The transfer is effected at Instruction Access speed (1.93 us.); however, STP is not performed. Indirect addressing and address modification can not be used with this instruction.

FORMAT

OPERATION - W

N - (period)

A ADDRESS - Zero (0000). Not to be used by programming.

B ADDRESS - HSM location of next instruction to be executed.

OUTLINE OF OPERATION

During Instruction Access the B Address contents are transferred to the P Register.

FINAL SETTINGS

$(A)_f = (A)_i$

$(B)_f = (B)_f$ of previous instruction.

VIII CARD READERS

MODEL 329 CARD READER

GENERAL DESCRIPTION

Two types of card readers are available with 3301 systems; the Model 329-1 reads up to 900 CPM, and the Model 329-2 reads up to 1470 CPM. Both read cards photo-electrically. Either 51 or 80 column cards may be read in either the Translate or Binary Mode. The devices are similar in all respects except card through-put rate.

OPERATION

The Model 329 Card Reader has a Hopper capacity of 2500 cards, and two 2000-card capacity stackers. Cards may be continuously loaded into the hopper or unloaded from either of the two stackers.

When the card has been read, a metal vane directs cards from the transport into either the Main or Reject stacker.

Cards are picked from the hopper by a rotating hammer. The picking mechanism feeds one card through the throat and onto a series of interference rollers. Eighty photo diodes are used in timing the correspondence of a card column and the photo-electric reading head. As the leading edge of the card cuts a timing diode, the corresponding card column is over the data photo diodes.

The Model 329 Card Reader consists of all necessary reading, timing, control and checking circuitry. The mechanism contains its power supply and an operators display panel. The Operators display panel includes a "Stop" button which provides controlled interruption of the card operation.

CONTROL

The Control is responsible for:

1. Determining the mode of operation (Binary of Translate).
2. Transferring data to HSM.
3. Providing accuracy control.
4. Code translation.
5. Routing cards to output stackers.
6. Providing indicators for these conditions; Inoperable, Busy, End File (EF), Photo-Diode Failure and Multi-Punch Error.

INSTRUCTIONS

The Control contains the necessary logic to initiate, control, and provide terminal information for the following instructions:

Read Forward Simo 1 (RF1)	Read Forward Simo 2 (RF2)
Control Device Simo 1 (CD1)	Control Device Simo 2 (CD2)
Test Device (TDV)	

Instructions are presented by function under these headings: (1) Specifying Translate or Binary, (2) Reading Cards, and (3) Testing the Device.

SPECIFYING TRANSLATE OR BINARY

GENERAL DESCRIPTION

The Control Device Simo 1 (CD1) or Control Device Simo 2 (CD2) instruction conditions the Card Reader to read cards in either the Translate or Binary Mode. A mode must be specified prior to the execution of the first card read instruction. The selected mode pertains to all card read instructions that follow. To read cards in another mode requires a control device instruction so specifying.

FORMAT

OPERATION - 2 (CD1) or 3 (CD2)

N - - (minus) if first Card Reader, J if second Card Reader

A ADDRESS - Zero (0000). Not to be used by programming.

B ADDRESS - $B_0B_1B_2$ - Zero (000). Not to be used by programming.

$B_3 = 1$ Binary Mode

$B_3 = 2$ Translate Mode

FINAL SETTINGS

$(S)_f$ or $(C)_f = (A)_i$

$(T)_f$ or $(E)_f = (B)_i$

GENERAL DESCRIPTION

The Read Forward Simo 1 (RF1) or Read Forward Simo 2 (RF2) instruction performs this function. Cards are read in the Translate or Binary Mode as specified by a Control Device instruction. If the Translate Mode is specified, the card columns are automatically translated to the machine code. When the Binary Mode is specified, each card column is split into two six-bit groups with each card column requiring two consecutive HSM locations.

FORMAT

OPERATION - 4 (RF1) or 5 (RF2)

N - - (Minus) if first Card Reader, J if second Card Reader.

A ADDRESS - HSM location to receive the first character. Location must be even.

B ADDRESS - Zero (0000). Not to be used by programming

DIRECTION OF OPERATION

Characters are transferred into HSM left to right.

Cards are read serially beginning with column one.

OUTLINE OF OPERATION

A card is fed from the input hopper and its contents transferred to HSM. In the Translate Mode two characters are transferred in parallel to an HSM diad after the two card columns containing these characters are read and checked. In the Binary Mode two characters are transferred in parallel to an HSM diad after each card column is read and checked. The instruction terminates when the last card column has been read and transferred.

Each column of a card in binary format contains two six-bit characters. Rows four through nine represent one character with the 2^0 bit in row four. Rows twelve (Y) through three represent another character with the 2^0 bit in row twelve.

FINAL SETTINGS

$(S)_f$ or $(C)_f$ = HSM location one to the right of the last character transferred.

$(T)_f$ or $(E)_f = (B)_i$

GENERAL DESCRIPTION

The Test Device (TDV) instruction tests the desired status of the Card Reader. Control is transferred if the condition or conditions being tested are present.

FORMAT

OPERATION - S

N - - (Minus) if first Card Reader, J if second Card Reader.

A ADDRESS - Specifies the test to be performed as follows:

Character	Bit Position	Symbol	Test
A_0	$2^0 = 1$	1	Is device inoperable?
A_0	$2^1 = 1$	2	Is device operating (Busy)?
A_0	$2^2 = 1$	4	Is there a Photo-Diode Failure (PDF)?
A_0	$2^3 = 1$	8	Is there a Multi-Punch Error (MPE)?
A_1	$2^3 = 1$	8	Is the EF Indicator set?

Unused characters must be zeros and are not to be used by programming.

B ADDRESS - HSM location of the next instruction to be executed if the condition(s) being tested is(are) present.

SPECIAL CONDITIONS

STP is performed if the condition(s) specified by the A Address is(are) present.

FINAL SETTINGS

$(A)_f = (A)_i$

$(B)_f = (B)_i$

TIMING

The Model 329-1 reader has a card cycle of 67 ms. The Model 329-2 reader has a card cycle of 40.8 ms. Since each Card Reader is a demand type device, there is no requirement for issuing a read command within a given interval of the card read cycle. For example, if read commands are issued every 80 milliseconds, the rate becomes 750 CPM. The specified Simo Mode is occupied during the entire card cycle, since the trailing edge of the card must be detected to permit the completion of the photo diode tests.

ACCURACY CONTROL

All unread cards are automatically rejected. If the Card Reader is accessed while either busy or Inoperable, the instruction is not executed, the Busy or Inoperable Indicator is set, and the Interrupt occurs. The existence of PDF, MPE or EF is presented to the Processor upon termination of a Read instruction, the "Simo Mode Terminated Abnormally" Indicator is set and interrupt occurs. Any command issued to the device while the "Hold" Light is on will cause the "Busy" or "Inoperable" indicator to be set.

END OF FILE

The Control includes the necessary logic to detect an EF Card. An End of File card is defined as follows:

Translate Mode: X-6-8 punches in column one, columns 2 through 80 contain no punches.

Binary Mode: Rows 9, 7, 6 & 5 of column one contain punches; the remainder of the card contains no punches.

Upon detection of an EF card and termination of a Read instruction, the Control EF Indicator is set. The Control detection logic informs the Processor that an abnormal termination resulted by setting that Interrupt Indicator. Upon receipt of a TDV instruction addressed to this device, the program is informed of the existence of an EF card.

OPERABLE-INOPERABLE

The state of the hopper and stackers will be indicated to the Control by the combined operable-hoppers line. When the hopper becomes empty or the stacker full or both, the Inoperable Indicator in the Control is set. Upon the occurrence of an inoperable condition the Control sets the Busy or Inoperable Interrupt Indicator. The Operable Indicator can be reset only by removal of the condition which caused inoperability. Included are the following conditions:

1. Power failure
2. Reader jam
3. Stacker full
4. Hopper empty

THREE PICK TEST

On Models 329-1 and 329-2 Card Readers three attempts to pick a card are provided. If a card is not successfully picked in 90 ms, the three pick error indication is given and the Mode Terminated Abnormally Interrupt Indicator is set.

BUSY

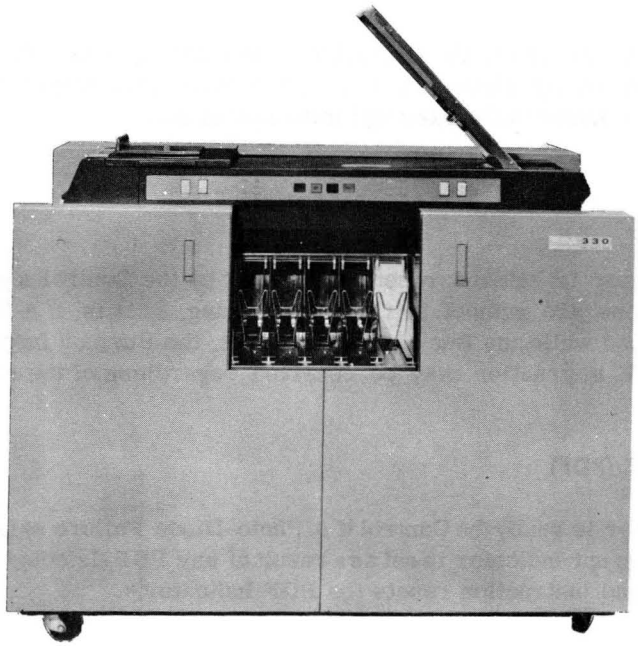
The Busy Indicator is set and reset as required by the Control logic. Card read and control device instructions are subject to the Busy setting. That is, if a RF1, RF2, CD1 or CD2 instruction is issued while the Busy Indicator is set, the Busy or Inoperable Interrupt Indicator is set. The TDV instruction may be received regardless of the state of the Busy Indicator.

PHOTO-DIODE FAILURE (PDF)

The PDF Indicator is set by the Control if a Photo-Diode Failure exists. The Mode Terminated Abnormally Interrupt Indicator is set as a result of any PDF detected, and the card is rejected. The next card read instruction resets the PDF Indicator.

MULTI-PUNCH ERROR (MPE)

The MPE Indicator is set upon detection of an invalid character. An error Character (e) is placed in the HSM character location corresponding to each invalid character detected. The read instruction is carried to completion, and the card is rejected. The Mode Terminated Abnormally Interrupt Indicator is immediately set as a result of any one MPE detected. The next card read instruction resets the MPE Indicator.



MODEL 330 CARD READER-PUNCH

GENERAL DESCRIPTION

The Card Reader-Punch consists of a card reader and card punch in the same cabinet. The reader unit, under program control, will either: (1) automatically convert 80-column Hollerith card code to 3301 code for transfer to memory, or (2) read a card image into memory for processing. Reading occurs a row at a time at rates up to approximately 800 cards per minute. Two read stations permit a hole count accuracy check to be performed. There are three selectable stackers which are under program control on the reader unit.

The punch unit punches 80-column cards in either Hollerith or binary code as specified by the program. Punching is performed at rates up to approximately 250 cards per minute. Verification of the punched data by a post-punch-read is performed on the succeeding card punch cycle.

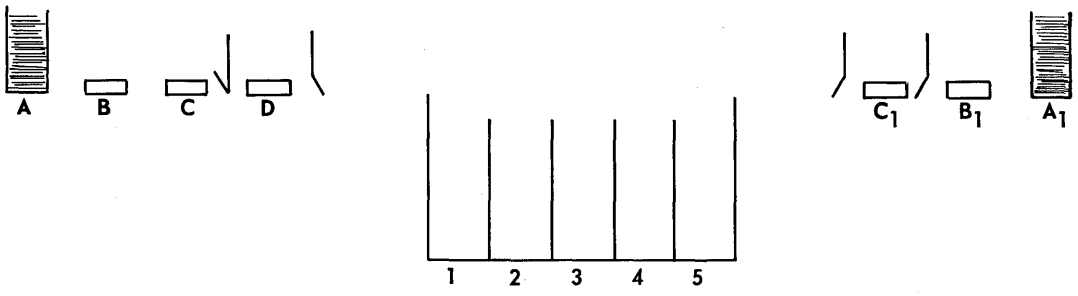
The input hopper of the reader unit holds 3,000 cards, and the input hopper of the Punch Unit holds 1,200 cards.

The Model 330 Card Reader-Punch has the capability of reading and punching cards simultaneously (duplicating cards). Simultaneous card reading and punching operations may not be performed on-line (not under control of the processor).

The Model 3300 Punch and Reader Controller permits operation of the 330 Reader/Punch with the 3301 Processor. The controller contains all the necessary logic for control and accuracy checking.

OPERATION OF READER/PUNCH

MECHANISM SCHEMATIC MODEL 330-1



A. PUNCH HOPPER

B. BLANK STATION

C. PUNCH STATION

D. PUNCH CHECK STATION

1. NORMAL PUNCH STACKER

2. REJECT PUNCH STACKER

3. OPTIONAL READ STACKER

4 REJECT READ STACKER

5. NORMAL READ STACKER

A_1. READ HOPPER

B_1. READ CHECK STATION

C_1. READ DATA STATION

The read unit may select by program any of the three hoppers (3,4, or 5). Cards with detected errors are sent to the Reject Read Stacker. A Stacker Select from the program must be received by the read unit within 10 milliseconds after the card leaves the Read Data Station (C_1).

The Model 330-2 has another station on the read unit called the Select Stacker station. This station would be located between the read station and the hopper. On the 330-2 the hopper select may be issued at any time prior to the next command advancing the transport.

The punch unit does not have a stacker that is program selectable. If a punch error is detected, the card is sent to the reject punch stacker.

CONTROL

The 3300 Controller is responsible for:

1. Determining the mode of operation (Binary of Translate).
2. Transferring data to HSM.
3. Providing accuracy control.
4. Code translation.
5. Routing cards to output stackers.
6. Providing indicators for these conditions; Inoperable, Busy, End File (EF), Read Compare Error and Multi-Punch Error.

INSTRUCTIONS

The Control contains the necessary logic to initiate, control, and provide terminal information for the following instructions:

Read Forward Simo 1 (RF1)	Read Forward Simo 2 (RF2)
Control Device Simo 1 (CD1)	Control Device Simo 2 (CD2)
Test Device (TDV)	

Instructions are presented by function under these headings: (1) Specifying Translate or Binary, (2) Reading Cards, and (3) Testing the Device.

SPECIFYING TRANSLATE OR BINARY

GENERAL DESCRIPTION

The Control Device Simo 1 (CD1) or Control Device Simo 2 (CD2) instruction conditions the Card Reader to read cards in either the Translate or Binary Mode. A mode must be specified prior to the execution of the first card read instruction. The selected mode pertains to all card read instructions that follow. To read cards in another mode requires a control device instruction to specifying.

FORMAT

OPERATION - 2 (CD1) or 3 (CD2)

N - - (minus) if first Card Reader, J if second Card Reader

A ADDRESS - Zero (0000). Not to be used by programming.

B ADDRESS - $B_0B_1B_2$ - Zero (000). Not to be used by programming.

B3

if $2^0(1)$ - read binary

$2^0(0)$ - read translate

if $2^2(1)$ - select stacker 4 } refers to mechanism schematic

$2^3(1)$ - select stacker 3 }

$2^4(0)$ - always false

$2^5(1)$ - advance read transport

FINAL SETTINGS

$(S)_f$ or $(C)_f = (A)_i$

$(T)_f$ or $(E)_f = (B)_i$

READING CARDS

GENERAL DESCRIPTION

The Read Forward Simo 1 (RF1) or Read Forward Simo 2 (RF2) instruction performs this function. Cards are read in the Translate or Binary Mode as specified by a Control Device instruction. If the Translate Mode is specified, the card columns are automatically translated to the machine code. When the Binary Mode is specified, each card column is split into two six-bit groups with each card column requiring two consecutive HSM locations.

FORMAT

OPERATION - 4 (RF1) or 5 (RF2)

N - - (Minus) if first Card Reader, J if second Card Reader.

A ADDRESS - HSM location to receive the first character. Location must be even.

B ADDRESS - Zero (0000). Not to be used by programming.

DIRECTION OF OPERATION

Characters are transferred into HSM left to right.

Cards are read serially beginning with column one.

OUTLINE OF OPERATION

A card is fed from the input hopper and its contents transferred to HSM. In the Translate Mode two characters are transferred in parallel to an HSM diad after the two card columns containing these characters are read and checked. In the Binary Mode two characters are transferred in parallel to an HSM diad after each card column is read and checked. The instruction terminates when the last card column has been read and transferred.

Each column of a card in binary format contains two six-bit characters. Rows four through nine represent one character with the 2^0 bit in row four. Rows twelve (Y) through three represent another character with the 2^0 bit in row twelve.

FINAL SETTINGS

$(S)_f$ or $(C)_f$ = HSM location one to the right of the last character transferred.

$(T)_f$ or $(E)_f$ = $(B)_i$

TESTING THE DEVICE

GENERAL DESCRIPTION

The Test Device (TDV) instruction tests the desired status of the Card Reader. Control is transferred if the condition or conditions being tested are present.

FORMAT

OPERATION - S

N - -(Minus) if first Card Reader, J if second Card Reader.

A ADDRESS - Specifies the test to be performed as follows:

Character	Bit Position	Symbol	Test
A_0	$2^0 - 1$	1	Is device inoperable?
A_0	$2^1 = 1$	2	Is device operating (Busy)?
A_0	$2^2 = 1$	4	Is there a Read Compare Error (RCE)?
A_0	$2^3 = 1$	8	Is there a Multi-Punch Error (MPE)?
A_1	$2^0 = 1$	1	Is the read buffer available?
A_1	$2^3 = 1$	8	Is the EF Indicator set?
A_3	$2^0 = 1$	1	Reset the buffer available Indicator.

Unused characters must be zeros and are not to be used by programming.

B ADDRESS - HSM location of the next instruction to be executed if the condition(s) being tested is(are) present.

SPECIAL CONDITIONS

STP is performed if the condition(s) specified by the A Address is(are) present.

FINAL SETTINGS

$(A)_f = (A)_i$

$(B)_f = (B)_i$

TIMING

The Model 330 Reader Unit has a card cycle of 65 ms. Since the Card Reader is a demand type device, there is no requirement for issuing a Read command within a given interval of of the Card Read cycle. For example, if Read commands are issued every 80 milliseconds, the rate becomes 750 CPM. The specified Simo Mode is occupied during the entire card cycle, since the trailing edge of the card must be detected to permit the completion of the photo diode tests. To maintain a maximum rate of the device another read instruction should be issued within 10 ms. after the previous card was read.

ACCURACY CONTROL

All unread cards are automatically rejected. If the Card Reader is accessed while either busy or Inoperable, the instruction is not executed, the Busy or Inoperable Indicator is set, and the Interrupt occurs. The existence of RCE, MPE or EF is presented to the Processor upon termination of a Read instruction, the "Simo Mode Terminated Abnormally" Indicator is set and interrupt occurs. Any command issued to the device while the "Hold" Light is on will cause the "Busy" or "Inoperable" indicator to be set.

END OF FILE

The Control includes the necessary logic to detect an EF Card. An End of File card is defined as follows:

Translate Mode: X-6-8 punches in column one, columns 2 through 80 contain no punches.

Binary Mode: Rows 9, 7, 6 & 5 of column one contain punches; the remainder of the card contains no punches.

Upon detection of an EF card and termination of a Read instruction, the Control EF Indicator is set. The Control detection logic informs the Processor that an abnormal termination resulted by setting that Interrupt Indicator. Upon receipt of a TDV instruction addressed to this device, the program is informed of the existence of an EF card.

OPERABLE-INOPERABLE

The state of the hopper and stackers will be indicated to the Control by the combined operable-hoppers line. When the hopper becomes empty or the stacker full or both, the Inoperable Indicator in the Control is set. Upon the occurrence of an inoperable condition the Control sets the Busy or Inoperable Interrupt Indicator. The Operable Indicator can be reset only by removal of the condition which caused inoperability. Included are the following conditions:

1. Power failure
2. Reader jam
3. Stacker full
4. Hopper empty
5. Start key open (not primed)
6. Interlock stop
7. Check reset
8. Stop key true (3330-1 only)

BUSY

The Busy Indicator is set and reset as required by the Control logic. Card read and control device instructions are subject to the Busy setting. That is, if a RF1, RF2, CD1 or CD2 instruction is issued while the Busy Indicator is set, the Busy or Inoperable Interrupt Indicator is set. The TDV instruction may be received regardless of the state of the Busy Indicator.

READ COMPARE ERROR (RCE)

The 3300 Controller generates a hole count on a card being read at the read check station and this count is again generated when the card is being read for data. If the two hole counts do not agree, this bit ($A_0 2^2$) is made true and the card with the error is sent to the Read Reject Stacker.

READ BUFFER AVAILABLE

The read unit image buffer is available at all times that "busy" is not true. The read unit control shall make $A_1 2^0$ true at the completion of a read unit machine cycle.

MULTI-PUNCH ERROR (MPE)

The MPE indicator ($A_0 2^3$) is set upon detection of an invalid character. An error character (17_8) is placed in the memory character location corresponding to each invalid character detected. The read instruction continues until all data in the card has been transferred to the processor.

READ INFORMATION PARITY ERROR (RIPE)

The 3300 Controller contains hardware to verify the data handling circuits of the read control. In case the parity of the read buffer data does not agree with the parity of the data going to the processor, $A_0 2^3$ shall be made true. Whenever $A_0 2^3$ is true, due to a Read Information Parity Error, the Read instruction is terminated immediately, one (17_8) is forwarded to the processor and SRA is reported. This indicator ($A_0 2^3$) is reset upon initiation of the next read instruction.

CONTROL

The 3300 Controller contains a full-card Buffer and the necessary logic to initiate, control and provide terminal information for the instructions pertaining to the Card Punch. The Control, in general, is responsible for:

1. Determining the mode of operation.
2. Loading the full-card Buffer.
3. Providing accuracy control.
4. Translating from machine code to card code.
5. Providing sensible indicators for these conditions: Inoperable, Busy, Punch Compare Error and Parity Error.

INSTRUCTIONS

Instructions utilized for programming the Card Punch are:

Write Simo 1 (WR1) Write Simo 2 (WR2)

Test Device (TDV)

These instructions are presented by function under the headings: (1) Punching Cards, and (2) Testing the Device.

PUNCHING CARDS

GENERAL DESCRIPTION

The Write Simo 1 (WR1) or Write Simo 2 (WR2) instruction punches a card in the Translate or Binary Mode with data contained in HSM. The full-card Buffer is loaded, cards are advanced one station, the Buffer is unloaded, and a card is punched.

FORMAT

OPERATION - 8 (WR1) or 9 (WR2)

N - M if first Card Punch, N if second Card Punch.

A ADDRESS - HSM location of first character to be punched (must be even).

B ADDRESS - $B_0B_1B_2$ = Zero (000). Not to be used by programming.

B_3 = 0 Translate Mode.

B_3 = 1 Binary Mode.

DIRECTION OF OPERATION

Characters are transferred from HSM left to right.

Cards are punched one row at a time.

OUTLINE OF OPERATION

In the Translate Mode the 3300 Controller translates each 6-bit character to a 12-bit card character. Characters in locations one through 80 in HSM are translated into their equivalent 12-bit card code and placed in corresponding columns one through 80 of the Buffer for subsequent card punching. Characters are transferred by diad from HSM to the Data Register. Data is transferred to the Buffer by character.

In the Binary Mode the Buffer within the controller is used to combine the 160 six-bit characters into 80 12-bit card characters for subsequent card punching as follows: Characters in even HSM locations are placed in rows four to nine of columns one through 80. Characters in odd HSM locations are placed in rows 12 to three of columns one through 80. Rows 3 and 9 contain the 2^5 bit of their respective characters. Characters are transferred by diad from HSM to the Data Register. Data is transferred to the Buffer by diad.

FINAL SETTINGS

$(S)_f$ or $(C)_f = (A)_i + 80$ (Translate Mode)

$(S)_f$ or $(C)_f = (A)_i + 160$ (Binary Mode)

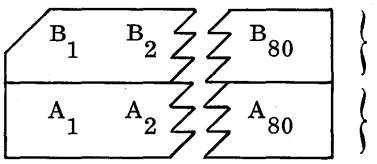
$(T)_f$ or $(E)_f = (B)_i$

EXAMPLES

Instruction: 8 M 0600 0001 (Binary Mode)

80 Column Card

Col. 1 Col. 2 Col. 80



Rows 12 to 3

Rows 4 to 9

HSM Contents

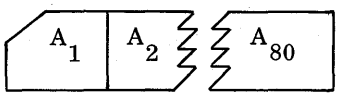
0600	0601	0602	0603 ... 0758	0759
A_1	B_1	A_2	B_2 ... A_{80}	B_{80}

Final Settings: $(S)_f = 0760$ $(T)_f = 0001$

Instruction: 9 M 0600 0000 (Translate Mode)

80 Column Card

Col. 1 Col. 2 Col. 80



HSM Contents

0600	0601	0679
A_1	A_2	A_{80}

Final Settings: $(C)_f = 0680$ $(E)_f = 0000$

TESTING THE DEVICE

GENERAL DESCRIPTION

The Test Device (TDV) instruction tests the desired status of the Card Punch and transfers control if the condition or conditions being tested are present. This instruction also may be used to reset two indicators; however, this function has no effect on the transfer of control.

FORMAT

OPERATION - S

N - M if first Card Punch, N if second Card Punch.

A ADDRESS - Specifies function to be performed as follows:

Character	Bit Position	Symbol	Test or Reset Function
A_0	$2^0 = 1$	1	Is device inoperable?
A_0	$2^1 = 1$	2	Is device operating (Busy)?
A_0	$2^2 = 1$	4	Is there a Punch Compare Error (PCE)?
A_0	$2^3 = 1$	8	Is there a Parity Error (PE)?
A_1	$2^0 = 1$	1	Is Buffer available?
A_2	$2^2 = 1$	4	Reset PCE Indicator.
A_2	$2^3 = 1$	8	Reset PE Indicator.
A_3	$2^0 = 1$	1	Reset Buffer Available Indicator.

Unused characters must be zeros and are not to be used by programming.

B ADDRESS - HSM location of the next instruction to be executed if the condition(s) being tested is(are) present.

SPECIAL CONDITIONS

STP is performed if the condition(s) specified by the A Address is (are) present.

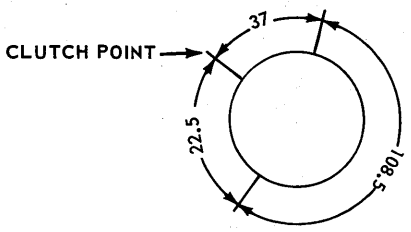
FINAL SETTINGS

$(A)_f = (A)_i$

$(B)_f = (B)_i$

TIMING

The Card Punch has a card cycle of 168 milliseconds which is divided into three time intervals as follows:



108.5 ms. = Punching and punch check time

22.5 ms. = Intercard time

37 ms. = Clutch energizing time

To maintain the maximum rate of 250 cards per minute, the next punch command must be issued during the intercard time. If a punch command is issued after the intercard time, a card cycle is missed, and the punch rate is decreased. After the punch instruction is executed, the device is busy until the intercard time is reached.

ACCURACY CONTROL

OPERABLE-INOPERABLE

The following conditions render the device inoperable (when the device is inoperable, it will not appear busy):

1. Lack of power
2. Empty input hopper
3. Stacker full
4. Malfunction
5. Card jam
6. Not primed

PARITY ERROR (PE)/PUNCH MEMORY PARITY ERROR (PMCE)

Each character transferred from the processor to the 3300 Controller is checked for odd parity. If the parity is not odd for each character, $A_0 2^3$ shall be made true. Detection of a parity error causes the card in the punch station to be routed to the reject stacker.

The punch control also makes a hole count as the punch buffer is being loaded. The punch control makes a second hole count of the data as the buffer unloads. If the two hole counts do not agree, $A_0 2^3$ is made true. Detection of a PMCE causes the card at the punch check station to be sent to the reject stacker.

PUNCH COMPARE ERROR (PCE)

The controller detects a PCE if the hole count at the punch check is not equal to the hole count made when writing into the buffer. If a PCE is detected $A_0 2^2$ is made true. Two cards, one at the punch select and the other at the punch check station are rejected when a PCE is detected.

BUFFER AVAILABLE

Whenever the punch image buffer is available, the punch unit will inform the processor by making $A_1 2^0$ true. This bit will be made false by another write instruction or a Test Device instruction with $A_3 2^0$ true.

ERROR CONDITION SUMMARY TABLE

Device	Condition	Interrupt Indicator Set	Time of Indication	Instruction Termination	Indicator Clearance	Relative to Model II Station	Relative to Model I Station
330 Read Unit	Inoperable (SIO Time) - Lack of Power - Stacker Full - Hopper Empty - Not Primed - Jam - Stop Key True (3330-1 only)	I-11	Initiation of instruction	SIO Time	Causative condition removed	Transport not advanced	Transport not advanced
	Inoperable (Execution Time) - Lack of Power - Jam	SRA	Execution of instruction	At time detected	Causative condition removed	All stations	All stations
	Busy S_1/S_2 Time Read/IOC - Fill	I-11	Initiation of instruction	At time detected	Full cycle complete, not S_1/S_2	All stations if S_1/S_2; read unit if otherwise	All stations if S_1/S_2; read unit if otherwise
	RCE	SRA	Read termination	Read completion	Next I/OC $B_3 2^5(1)$	Card at read select station	Card leaving read data station
	MPE	SRA	Execution of read	Read completion	Next I/OC $B_3 2^5(1)$	Card at read select station	Card leaving read data station
	RIPE	SRA	At time detected	At time detected	Next I/OC $B_3 2^5(1)$	Card at read select station	Card leaving read data station

ERROR CONDITION SUMMARY TABLE (Cont'd)

Device	Condition	Interrupt Indicator Set	Time of Indication	Instruction Termination	Indicator Clearance	Relative to Station	Comments
	Read Buffer Available	I-9	Read fill cycle complete	Completion of I/OC $B_3 2^5(1)$ cycle	IOS $A_3 2^5(1)$/ next IOC with $B_3 2^5(1)$	Card at read select station	
	EF Indicator	SRA	Execution of read	Read completion	Next I/OC $B_3 2^5(1)$	Card at read select station	
330 Punch Unit	Inoperable (S10 Time) - Lack of Power - Stacker Full - Hopper Empty - Not Primed - Jam	I-11	Initiation of next instruction	At time detected	Causative condition removed	Transport not advanced	
	Inoperable (Off-Line) - Jam - Hopper Empty - Stacker Full	I-11	Initiation of next instruction	At time detected	Causative condition removed	All stations	
	Inoperable (Execution of Write)	Mode requires attention	During execution of WS1/WS2.	At time detected	Causative condition removed	Transport not advanced	
	Punch Compare Error	I-11	Initiation of instruction	At time detected	IOS instruction	Card at punch select station	Select and check station cards are rejected

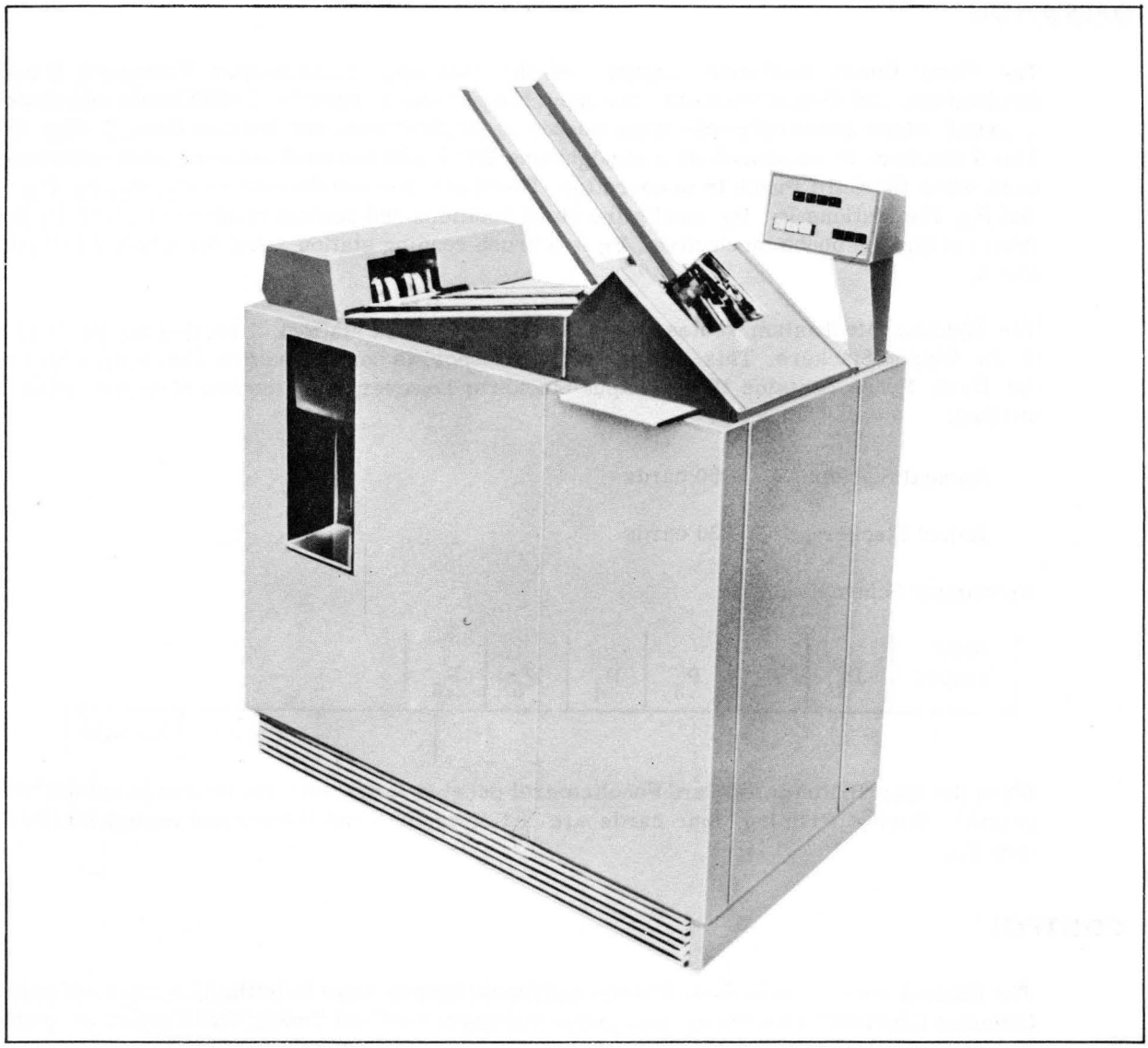
ERROR CONDITION SUMMARY TABLE (Cont'd)

Device	Condition	Interrupt Indicator Set	Time of Indication	Instruction Termination	Indicator Clearance	Relative to Station	Comments
	PE/PMCE	I-11	Initiation of instructions	At time detected	IOS instruction	Punch station if PE punch; check station if PMCE	PCE indication inhibited
	Punch Buffer Available	I-9	Completion of punch cycle		IOS $A_3 2^0$/ next Write instruction	Card at punch station	

CARD
PUNCH

IX CARD PUNCH

Note: For Model 330 Card Punch information, see Section VII - Model 330 Card Reader-Punch. (A)



CARD PUNCH

GENERAL DESCRIPTION

The Card Punch is a buffered device for punching 80 column cards in either Binary or Translate format at the rate of up to 300 cards per minute. The associated Control Module contains a full-card Buffer such that the card punching operation proceeds independently of the Processor as soon as the Buffer is loaded. Marked Sense cards are accepted; however, the marks do not affect punching or punch checking.

OPERATION

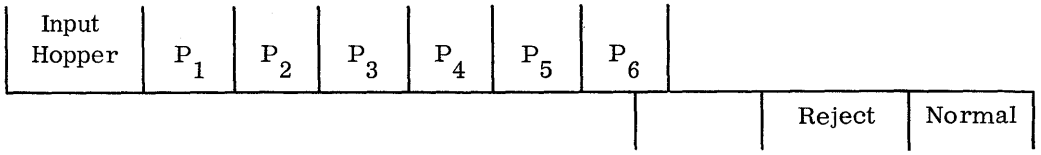
The Card Punch basically consists of the following: Input Hopper, Transport, Ejection Mechanism, and Output Stackers. The Input Hopper has a capacity of 3000 cards and contains a switch which shuts off power if the hopper is empty. Cards are fed face down, 9 edge first. The Transport is composed of a straight line track with six card stations, each containing a card when the Card Punch is in operation. These stations are denoted as P_1, P_2, P_3, P_4, P_5, and P_6. The stations P_1, P_2, and P_3 are blank positions and contain blank cards. The P_4 position contains the punch mechanism. P_5 is a brush reading station, used for a hole count punch check.

The Ejection Mechanism routes cards leaving P_6 (blank station), directing the cards to one of the Output Stackers. This section of the transport is continuous (not clutched). Physically the Card Punch contains three Output Stackers; however, only the two identified below are utilized:

Normal Stacker - 3000 cards

Reject Stacker - 730 cards

Mechanism Schematic:



When the Start Button on the Card Punch control panel is depressed, the device is automatically primed. During Priming, four cards are fed from the Input Hopper and occupy stations P_1 thru P_4.

CONTROL

The Control contains a full-card Buffer and the necessary logic to initiate, control and provide terminal information for the instructions pertaining to the Card Punch. The Control, in general, is responsible for:

1. Determining the mode of operation.
2. Loading the full-card Buffer.
3. Routing the cards to selected stackers.
4. Providing accuracy control.
5. Translating from machine code to card code.
6. Providing sensible indicators for these conditions: Operable, Busy, Punch Compare Error and Parity Error.

INSTRUCTIONS

Instructions utilized for programming the Card Punch are:

Write Simo 1 (WR1)

Write Simo 2 (WR2)

Test Device (TDV)

These instructions are presented by function under the headings: (1) Punching Cards, and (2) Testing the Device.

PUNCHING CARDS

GENERAL DESCRIPTION

The Write Simo 1 (WR1) or Write Simo 2 (WR2) instruction punches a card in the Translate or Binary Mode with data contained in HSM. The full-card Buffer is loaded, cards are advanced one station, the Buffer is unloaded, and a card is punched.

FORMAT

OPERATION - 8 (WR1) or 9 (WR2)

N - M if first Card Punch, N if second Card Punch.

A ADDRESS - HSM location of first character to be punched (must be even).

B ADDRESS - $B_0B_1B_2$ = Zero (000). Not to be used by programming.

B_3 = 0 Translate Mode.

B_3 = 1 Binary Mode.

DIRECTION OF OPERATION

Characters are transferred from HSM left to right.

Cards are punched one row at a time.

OUTLINE OF OPERATION

In the Translate Mode the Control translates each 6-bit character to a 12-bit card character. Characters in locations one through 80 in HSM are translated into their equivalent 12-bit card code and placed in corresponding columns one through 80 of the Buffer for subsequent card punching. Characters are transferred by diad from HSM to the Data Register. Data is transferred to the Buffer by character.

In the Binary Mode the Buffer within the Control is used to combine the 160 six-bit characters into 80 12-bit card characters for subsequent card punching as follows: Characters in even HSM locations are placed in rows four to nine of columns one through 80. Characters in odd HSM locations are placed in rows 12 to three of columns one through 80. Rows 3 and 9 contain the 2^5 bit of their respective characters. Characters are transferred by diad from HSM to the Data Register. Data is transferred to the Buffer by diad.

FINAL SETTINGS

$(S)_f$ or $(C)_f = (A)_i + 80$ (Translate Mode)

$(S)_f$ or $(C)_f = (A)_i + 160$ (Binary Mode)

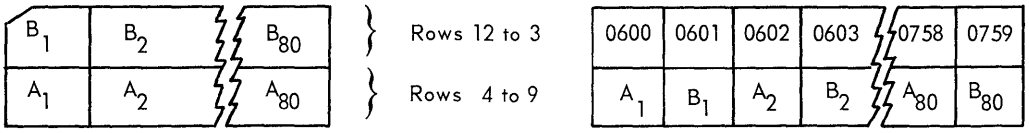
$(T)_f$ or $(E)_f = (B)_i$

EXAMPLES

Instruction: 8 M 0600 0001 (Binary Mode)

80 Column Card

Col. 1 Col. 2 Col. 80



Final Settings: $(S)_f$ = 0760 $(T)_f$ = 0001

Instruction: 9 M 0600 0000 (Translate Mode)

80 Column Card

Col. 1 Col. 2 Col. 80

Final Settings: $(C)_f$ = 0680 $(E)_f$ = 0000

TESTING THE DEVICE

GENERAL DESCRIPTION

The Test Device (TDV) instruction tests the desired status of the Card Punch and transfers control if the condition or conditions being tested are present. This instruction also may be used to reset two indicators; however, this function has no effect on the transfer of control.

FORMAT

OPERATION - S

N - M if first Card Punch, N if second Card Punch.

A ADDRESS - Specifies function to be performed as follows:

Character	Bit Position	Symbol	Test or Reset Function
A_0	$2^0 = 1$	1	Is device inoperable?
A_0	$2^1 = 1$	2	Is device operating (Busy)?
A_0	$2^2 = 1$	4	Is there a Punch Compare Error (PCE)?
A_0	$2^3 = 1$	8	Is there a Parity Error (PE)?
A_1	$2^0 = 1$	1	Is Buffer available?
A_2	$2^2 = 1$	4	Reset PCE Indicator.
A_2	$2^3 = 1$	8	Reset PE Indicator.
A_3	$2^0 = 1$	1	Reset Buffer Available Indicator.

Unused characters must be zeros and are not to be used by programming.

B ADDRESS - HSM location of the next instruction to be executed if the condition(s) being tested is(are) present.

SPECIAL CONDITIONS

STP is performed if the condition(s) specified by the A Address is (are) present.

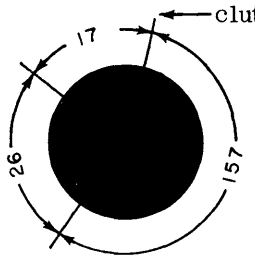
FINAL SETTINGS

$(A)_f = (A)_i$

$(B)_f = (B)_i$

TIMING

The Card Punch has a card cycle of 200 milliseconds which is divided into three time intervals as follows:



157 ms. = Punching and punch check time

26 ms. = Intercard time

17 ms. = Clutch energizing time

To maintain the maximum rate of 300 cards per minute, the next punch command must be issued during the intercard time. If a punch command is issued after the intercard time, a card cycle is missed, and the punch rate is decreased. After the punch instruction is executed, the device is busy until the intercard time is reached.

The Simo Mode is free as soon as the Buffer is loaded. Buffer transfer rate is 36 microseconds per character or diad. In the Translate Mode, transfer to the Buffer is by character (80 Buffer transfers). In the Binary Mode, transfer to the Buffer is by diad (80 Buffer transfers). Therefore, whether the Binary or Translate Mode is specified the Simo Mode is occupied for the same duration.

ACCURACY CONTROL

OPERABLE-INOPERABLE

The following conditions render the device inoperable (when the device is inoperable, it will not appear busy):

1. Lack of power
2. Empty input hopper
3. Stacker full
4. Malfunction
5. Card jam

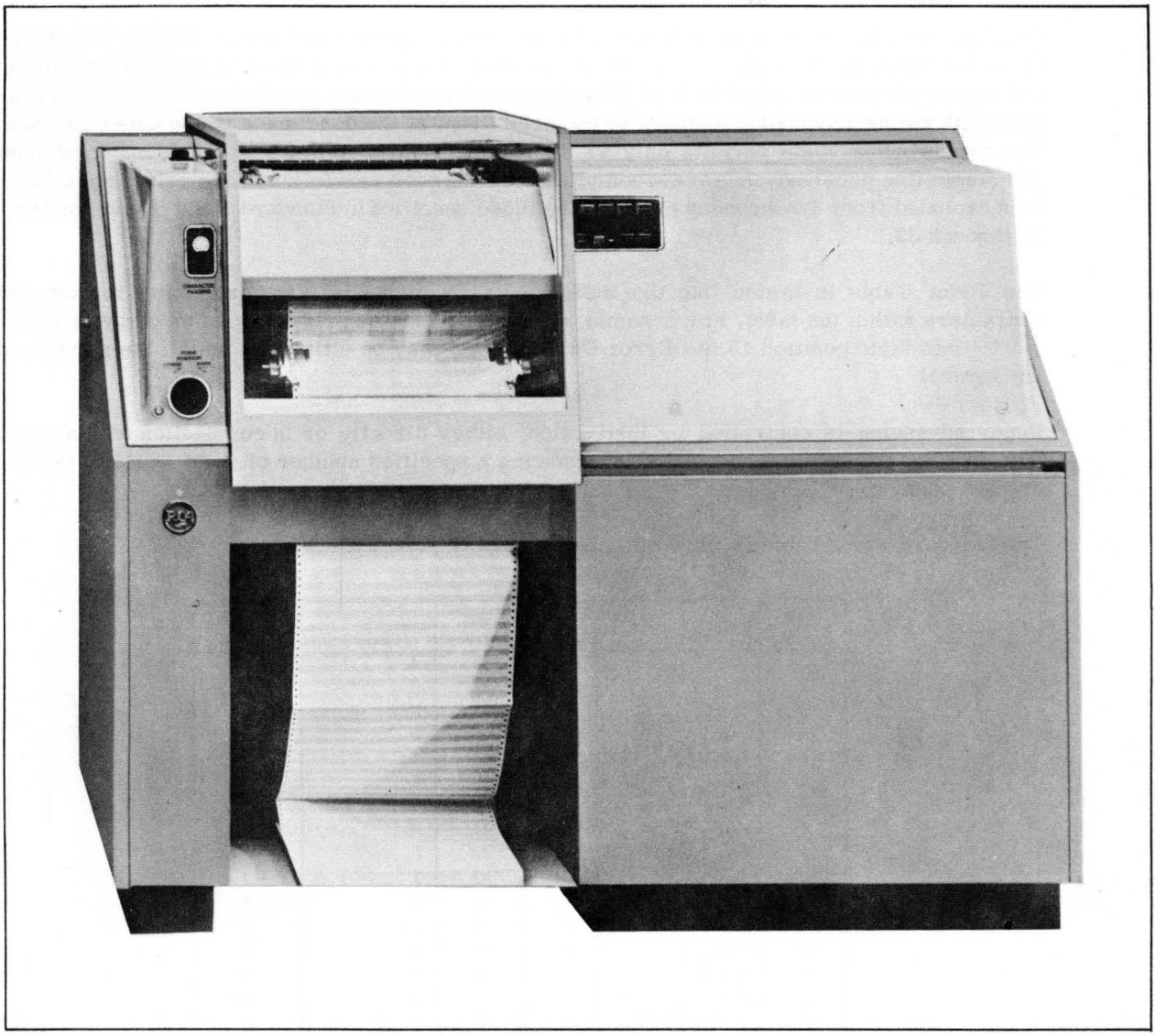
PARITY ERROR (PE)

Errors are detected on the transfer from HSM to Card during the punch cycle. The PE Indicator in the Control is set; the card will be automatically rejected, and punch compare errors will be inhibited. The Busy or Inoperable Interrupt Indicator will be set when the Card Punch is addressed by the next punch instruction.

PUNCH COMPARE ERROR (PCE)

The Control detects a PCE if the hole count at the punch check is not equal to the hole count made when writing into the Buffer, or if an error has been detected in the previous punch cycle. The Busy or Inoperable Interrupt Indicator is set upon detection of this error, and the two cards are automatically rejected. When the Card Punch is addressed by the next punch instruction, the Busy or Inoperable Interrupt occurs.

X ON-LINE PRINTER



ON-LINE PRINTER

GENERAL DESCRIPTION

The Printer is a buffered, transistorized device which prepares output documents from data contained in HSM. The On-Line Buffered Printer System is comprised of two functional units: (1) a 120 or 160 column Printer with a 184 or 224 character Buffer and (2) a Control. The Printer System includes; buffer storage with capacity for a full data line (120 or 160 characters) and a 64-character Print Table, along with all the necessary scan logic, vertical format control, and all the electronics required by the Printer. When the Buffer is fully loaded, print and paper advance options are accomplished offline leaving the Processor free for other processing.

Printing may be accomplished in either the Asynchronous or Synchronous Modes. The Asynchronous Mode permits all 64 symbols on the print drum to be printed in one full revolution, and paper advance to occur in a portion of the next print drum revolution. Scanning can proceed with the next symbol in sequence on the print drum at the conclusion of the paper advance. The Synchronous Mode permits only 47 symbols to be printed since a complete line of print and single line paper advance are accomplished during each revolution of the print drum. Symbols excluded from Synchronous printing are those specified in Standard Print Table positions 16 through 32.

The Print Table is loaded into the Buffer by instruction, and it is permissible to exchange characters within the table. For example, an Asterisk may be printed as a Period by inserting a "*" into table position 15. An Error Character (e) may be utilized to inhibit the printing of any symbol.

Paper advancing is controlled by instruction, either directly or in conjunction with a paper tape loop in the Printer, and includes advancing a specified number of lines, vertical tabbing or page changing.

The Standard Print Table is illustrated below:

Table* Position	Character	Printed Symbol	Table* Position	Character	Printed Symbol
1	Minus	–	33	A	A
2	Plus	+	34	B	B
3	Space		35	C	C
4	Zero	0	36	D	D
5	One	1	37	E	E
6	Two	2	38	F	F
7	Three	3	39	G	G
8	Four	4	40	H	H
9	Five	5	41	I	I
10	Six	6	42	J	J
11	Seven	7	43	K	K
12	Eight	8	44	L	L
13	Nine	9	45	M	M
14	Comma	,	46	N	N
15	Period	.	47	O	O
16	At the Rate Of	@	48	P	P
17	Percent	%	49	Q	Q
18	Colon	:	50	R	R
19	Number	#	51	S	S
20	Dollar Sign	$	52	T	T
21	Close Parenthesis	)	53	U	U
22	Quotation Mark	"	54	V	V
23	Subscript $_{10}$	10	55	W	W
24	Open Parenthesis	(	56	X	X
25	Close Bracket	]	57	Y	Y
26	Semicolon	;	58	Z	Z
27	Greater	>	59	Credit	C_R
28	Divide	÷	60	Apostrophe	'
29	Up Arrow	↑	61	Asterisk	*
30	Open Bracket	[	62	Ampersand	&
31	Less	<	63	Virgule	/
32	Equal	=	64	Lozenge	⌑

*Table positions correspond to print positions on the drum.

Standard vertical spacing is six lines per inch. Options, however, include either a switch permitting manual selection of 6 or 8 lines per vertical inch, or a switch permitting manual selection of 6 or 10 lines per inch. The printer accepts single or multiple sheet fanfold stock, from 4 to 19 inches in width, and up to 17 inches in sheet length, provided length is a multiple of standard sprocket distance.

OPERATION

On command from the Processor a data line (120 or 160 characters) or the Print Table is transferred, serially by diad, to the buffer via the Control. When the Buffer is fully loaded, printing occurs off-line. The Processor is also free during the portion of paper advance that does not overlap buffer loading. The Printer has the further capability to print off-line, under manual control, a pre-stored line of print data for test purposes, with no reference to, or control signals from the Processor or the Control.

The Buffer may be loaded while the paper is advancing. The Printer Busy signal is set at the start of buffer loading and remains set until completion of the last scan. During buffer loading, both the Printer Busy and the Paper Advancing signals are on. A hardware parity check occurs on each buffer access. The scan logic is contained in the Buffer. Scanning for the print drum line that will be next in print position references the data line and the Print Table in buffer storage.

Controls at the printer include a Start/Stop switch for manual operation and Top of Form.

CONTROL

This device enables the Processor to operate the Printer in accordance with the stored computer program. The Control receives data from the Processor and receives and transmits necessary signals to and from the Processor, the Buffer (directly) and the Printer (indirectly). Data is transmitted to the Buffer, where it is accessed by the Printer. Printer status signals transmitted to the Control are used to set appropriate Interrupt Indicators. A hardware parity check is performed on each buffer access (data and table). The Control holds the paper advance information associated with the current buffer loading, and transfers it to the storage in the Printer when required for execution. The Control receives and interprets the B address of a write instruction, directed to the Printer, to determine the function to be performed and the number of characters to be transferred. It receives data from the Processor by diad, and so transfers it to the Buffer.

The Control includes an indicator that is set on completion of the last scan, signifying that the Buffer is available for loading. The Buffer Available Indicator and the Off-Line Operation Complete Interrupt Indicator are set. Both indicators are inhibited when the "load table" option is specified. Buffer available status may be sensed and/or reset by the TDV instruction.

INSTRUCTIONS

The Write Simo 1 (WR1), Write Simo 2 (WR2) and Test Device (TDV) instructions are utilized to program the Printer. These instructions are presented by function as follows: (1) Print and Paper Advance, (2) Paper Advance Only, (3) Table to Buffer, and (4) Testing the Device.

PRINT AND PAPER ADVANCE

GENERAL DESCRIPTION

The Write Simo 1 (WR1) or the Write Simo 2 (WR2) instruction transfers 120 or 160 characters (one line) from HSM to the Buffer, prints a line and advances the paper. The Mode (Synchronous or Asynchronous) and line size (120 or 160) must be specified. By designating 120 characters, the 160-column model Printer will print a 120-character line. For paper advancing either a line count or paper tape loop-control may be specified. Two of the eight channels of the tape loop on the Printer are used for loop-controlled paper advance; the 2^0 channel specifies vertical tabulation, the 2^1 channel specifies page change. Any symbols in table positions 16-32 on the Standard Print Table included in the print line when Synchronous Mode printing is specified, will not be printed.

FORMAT

OPERATION - 8 (WR1) or 9 (WR2)

N - Q if first Printer, R if second Printer

A ADDRESS - HSM location of first character of the line to be printed. A_3 must be even.

B ADDRESS - B_0 = 1 Paper advance according to count specified in B_2.

B_0 = 2 Loop-controlled vertical tabulation.

B_0 = 4 Loop-controlled page change.

B_1 = 0 Asynchronous Mode.

B_1 = 2 Synchronous Mode.

B_2 = Number of lines (0-15) to advance paper. See Appendix IV.

B_3 = 1 Print 120 characters.

B_3 = 2 Print 160 characters.

Unused characters must be zeros and are not to be used by programming.

FINAL SETTINGS

$(S)_f$ or $(C)_f$ = HSM location one to the right of the last character printed.

$(T)_f$ or $(E)_f$ = $(B)_i$

GENERAL DESCRIPTION

The Write Simo 1 (WR1) or the Write Simo 2 (WR2) instruction specifies paper advancing without printing. "No printing" must be specified.

FORMAT

OPERATION - 8 (WR1) or 9 (WR2)

N - Q if first Printer, R if second Printer.

A ADDRESS - Zero (0000). Not to be used by programming.

B ADDRESS - B_0 = 1 Paper advance according to count specified in B_2.

B_0 = 2 Loop-controlled vertical tabulation.

B_0 = 4 Loop-controlled page change.

B_1 = 1 No printing.

B_2 = Number of lines (0-15) to advance paper. See Appendix IV.

B_3 = 0 No HSM to Buffer transfer.

Unused characters must be zeros and are not to be used by programming.

FINAL SETTINGS

$(S)_f$ or $(C)_f = (A)_i$

$(T)_f$ or $(E)_f = (B)_i$

TABLE TO BUFFER

GENERAL DESCRIPTION

The transfer of a 64-character Print Table from HSM to the Buffer is accomplished by either the Write Simo 1 (WR1) or the Write Simo 2 (WR2) instruction. The Print Table may be located in any 64 contiguous HSM positions providing the first table character is in the first position of a diad. "No printing" must be specified.

FORMAT

OPERATION - 8 (WR1) or 9 (WR2)

N - Q if first Printer, R if second Printer

A ADDRESS - HSM location of first character of Print Table. A_3 must be even.

B ADDRESS - B_0 = Zero (0). Not to be used by programming.

B_1 = 1 No Printing.

B_2 = Zero (0). Not to be used by programming.

B_3 = 4 Specifies Print Table.

FINAL SETTINGS

$(S)_f$ or $(C)_f$ = HSM location one to the right of the last character in the Print Table.

$(T)_f$ or $(E)_f$ = $(B)_i$

GENERAL DESCRIPTION

The Test Device (TDV) instruction tests the desired status of the Printer and transfers control if the condition or conditions being tested are present. The instruction also resets the PE Indicator. This reset function has no effect on the transfer of control.

FORMAT

OPERATION - S

N - Q if first Printer, R if second Printer.

A ADDRESS - Specifies function to be performed as follows:

Character	Bit Position	Symbol	Test or Reset Function
A_0	$2^0 = 1$	1	Is device inoperable?
A_0	$2^1 = 1$	2	Is device operating (Busy)?
A_0	$2^2 = 1$	4	Is there a low paper supply?
A_0	$2^3 = 1$	8	Is there a parity error (PE)?
A_0	$2^4 = 1$	&	Is the paper advancing?
A_1	$2^0 = 1$	1	Is Buffer available?
A_2	$2^3 = 1$	8	Resets PE Indicator.
A_3	$2^0 = 1$	1	Resets Buffer Available Indicator.

Unused characters must be zeros and are not to be used by programming.

B ADDRESS - HSM location of the next instruction to be executed if the condition(s) being tested is (are) present.

SPECIAL CONDITIONS

STP is performed if the condition(s) specified by the A Address is (are) present.

FINAL SETTINGS

$(A)_f = (A)_i$

$(B)_f = (B)_i$

TIMING

Nominal printing speed with single-line paper advance is 1000 lines per minute in the Synchronous Mode and 800 lines per minute in the Asychronous Mode.

To maintain the maximum printing speed, the following is necessary:

1. Synchronous Mode must be specified.
2. Single line paper advancing must be performed.
3. The Buffer must be loaded during paper advance time of the previous instruction.

Printing and paper advancing of one line takes 60ms. (45 for printing and 15 for paper advance) in the Synchronous Mode or 75ms. (60 for printing and 15 for paper advance) in the Asynchronous Mode. Multiple line paper advancing is done at the rate of 6.67ms. per line after the first line. Buffer transfer rate is 8 microseconds per diad. The Simo Mode is occupied during Buffer loading time only.

Consecutive spacing shall only be implemented at intervals of 35 milliseconds; i.e., an automatic hardware hold off for 35 milliseconds will be implemented to prevent difficulty incurred by consecutive paper spacing instructions.

ACCURACY CONTROL

HALT BUTTON

Depression of this button sets the device inoperable signal. If a line is in process of printing when the button is depressed, the line is completed; however, the next write instruction directed to the Printer will not be executed, the Busy or Inoperable Interrupt Indicator will be set, and interrupt will occur. The Printer cannot appear operable again until the Halt button is pressed a second time.

LOW PAPER SUPPLY

The Printer includes a low-paper supply photocell, located 22 inches below the print head on the input side, and a Paper-Out Switch located on the output side of the print head. The low-paper signal is set whenever the end of paper supply passes (uncovers) the low paper photocell. A write instruction directed to the Printer after the low-paper signal has been set, will be executed, but on termination of this instruction the Simo Mode Terminated Abnormally Interrupt Indicator is set. The low-paper indicator is reset when the low-paper photocell is covered (indicating replenishment of paper supply), so that no light shows through. Whenever the Paper-Out switch is set, the Printer Inoperable Indicator at the Printer is set, and the Busy or Inoperable Interrupt Indicator is set.

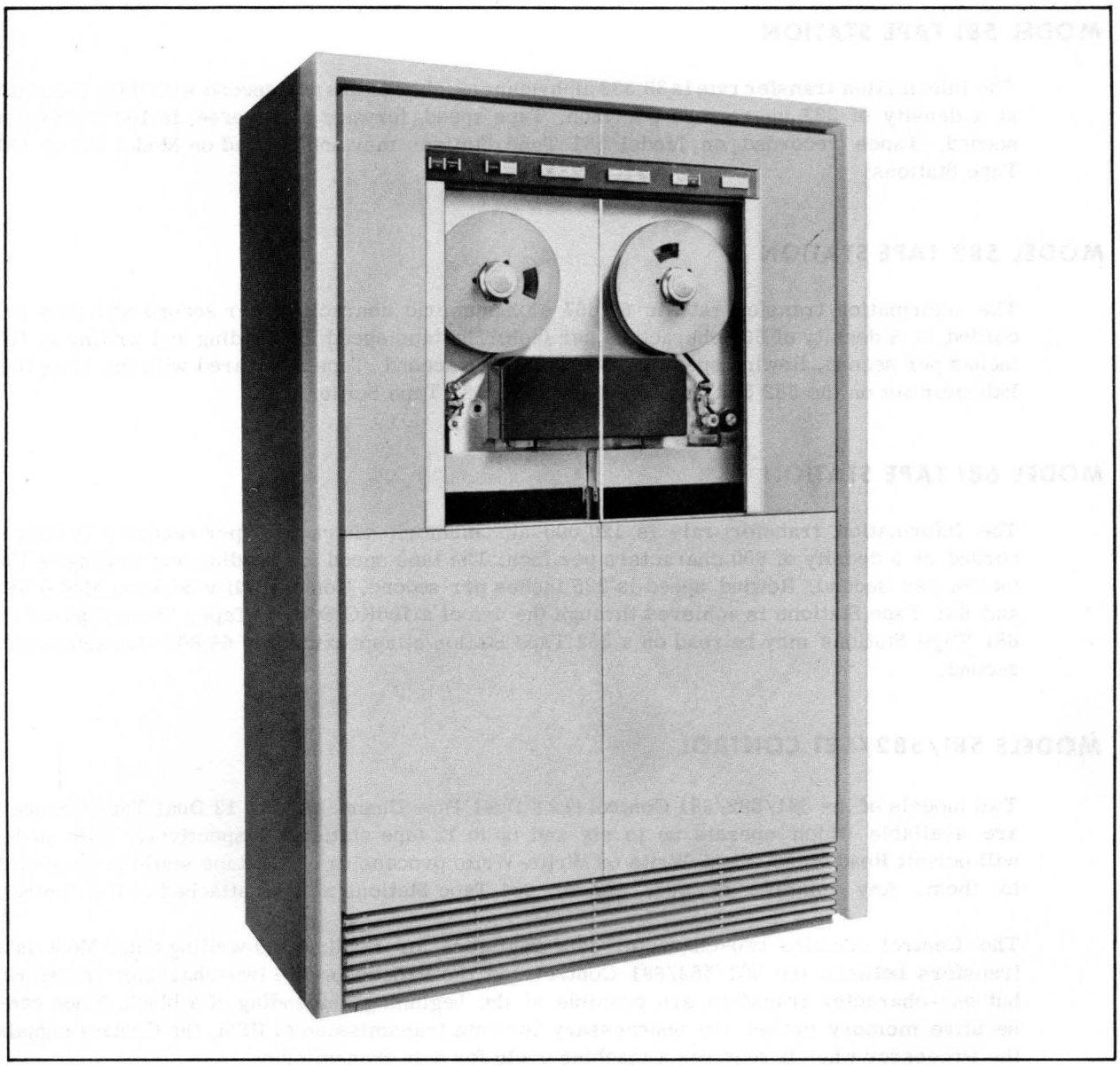
ERROR DETETECTION

If, on attempt to address the Printer in a Write instruction, the Device Inoperable signal is set because of malfunction, device not connected, power off, paper jam or cover open, the Busy or Inoperable Interrupt Indicator is set and Interrupt occurs before execution of the instruction. If, during buffer loading, the Device Inoperable signal is set because of malfunction or power off, the Simo Mode Terminated Abnormally interrupt Indicator is set, and the instruction is terminated immediately. If, during printing and/or paper advancing, the Device Inoperable signal is set because of power off, malfunction, paper jam or cover open, the Busy or Inoperable

Interrupt Indicator is set, and Interrupt occurs before execution of the next Write instruction directed to the device.

A Write instruction directed to a busy Printer (printing or buffer loading) will be interrupted before execution, with the Busy or Inoperable Interrupt Indicator set. A Write instruction directed to the Printer following detection of low-paper supply (low-paper signal set) is executed. On termination of the instruction, the Simo Mode Terminated Abnormally Interrupt Indicator is set.

XI MAGNETIC TAPE DEVICES



MODEL 582 TAPE STATION

GENERAL DESCRIPTION

Magnetic Tape Stations and their associated Control Module(s) are used for reading and writting characters on magnetic tape. Reading is possible in the forward or reverse direction; writing is performed in the forward direction. Three varieties of tape stations are available: Model 581, Model 582 and Model 681. Characters are dually recorded as magnetic spots in rows across the tape. The seven-bit machine code is utilized for character recording with an additional timing bit attached. Variable length format may be employed. Tape reels accommodate 2400 feet of tape. Terminal symbols placed on tape by programmed instruction include: EF signifying the End of a File; and ED signifying the End of (valid) Data on tape.

MODEL 581 TAPE STATION

The information transfer rate is 33,333 alphanumeric characters per second with data recorded at a density of 333 characters per inch. Tape speed, forward or reverse, is 100 inches per second. Tapes recorded on Model 581 Tape Stations may not be read on Model 582 or 681 Tape Stations.

MODEL 582 TAPE STATION

The information transfer rate is 66,667 alphanumeric characters per second with data recorded at a density of 667 characters per inch. The tape speed for reading and writing is 100 inches per second. Rewind speed is 150 inches per second. Tapes prepared with the Long Gap Indicator set on the 582 Stations may be read on 681 Tape Stations.

MODEL 681 TAPE STATION

The information transfer rate is 120,000 alphanumeric characters per second with data recorded at a density of 800 characters per inch. The tape speed for reading and writing is 150 inches per second. Rewind speed is 225 inches per second. Compatibility between Model 582 and 681 Tape Stations is achieved through the use of a 100KC Switch. Tapes thus prepared on 681 Tape Stations may be read on a 582 Tape Station at approximately 66,667 characters per second.

MODELS 581/582/681 CONTROL

Two models of the 581/582/681 Control (2 x 6 Dual Tape Channel or 2 x 12 Dual Tape Channel) are available which operate up to six and up to 12 tape stations, respectively. Each model will permit Read-Read, Read-Write or Write-Write processing on the tape stations connected to them. Any mixture of 581, 582 or 681 Tape Stations may be attached to the Control.

The Control contains two-character data registers for reading and writing data. Most data transfers between the 581/582/681 Control and the Processor are two-character transfers, but one-character transfers are possible at the beginning and ending of a block. Since consecutive memory cycles are unnecessary for data transmission to HSM, the Control signals the Processor when it requires a machine cycle for data transmission.

INSTRUCTIONS

Instructions utilized for programmming the magnetic tape devices are:

Read Forward Simo 1 (RF1)	Read Forward Simo 2 (RF2)
Read Reverse Simo 1 (RR1)	Read Reverse Simo 2 (RR2)
Write Simo 1 (WR1)	Write Simo 2 (WR2)
Erase Simo 1 (ER1)	Erase Simo 2 (ER2)

Control Device Simo 1 (CD1) Control Device Simo 2 (CD2)

Test Device (TDV)

These instructions are presented by function under the headings: (1) Reading Forward, (2) Reading Reverse, (3) Writing (4) Erasing, (5) Rewinding and (6) Testing the Device.

The 24 possible tape stations are instruction addressed and identified as follows:

First 2 x 12				Second 2 x 12			
First 2 x 6		Second 2 x 6		Third 2 x 6		Fourth 2 x 6	
Address Symbol	Station Number	Address Symbol	Station Number	Address Symbol	Station Number	Address Symbol	Station Number
1	01	9	11	A	21	I	31
2	02	¬	12	B	22	+	32
3	03	#	13	C	23	.	33
4	04	@	14	D	24	;	34
5	05	(	15	E	25	:	35
6	06	)	16	F	26	'	36

READING FORWARD

GENERAL DESCRIPTION

The Read Forward Simo 1 (RF1) or Read Forward Simo 2 (RF2) instruction transfers a series of consecutive characters from magnetic tape, moving in a forward direction into HSM. Reading begins with the first character following a gap and ends when the next gap is sensed or the specified HSM area is filled.

FORMAT

OPERATION - 4 (RF1) or 5 (RF2)

N - Specifies Magnetic Tape Station

A ADDRESS - HSM location to receive the first character.

B ADDRESS - HSM location to receive the last character.

DIRECTION OF OPERATION

Characters are transferred into HSM left to right.

OUTLINE OF OPERATION

Initially, a start signal is sent to the Tape Station specified by N. When the Control is ready to transfer characters, a demand is made on the Processor, and two characters from the Data Register are transferred to a HSM diad. If the first character to be transferred addresses an odd diad position, only that character is transferred. The C OR S Register is incremented by two to address the next diad. The cycle is repeated until a gap on tape is encountered or address equality occurs. If address equality occurs before a gap is reached, no further characters are transferred, but the tape continues to move to the next gap.

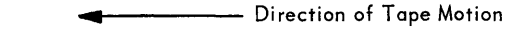
FINAL SETTINGS

$(S)_f$ or $(C)_f$ = HSM location one to the right of the last character read.

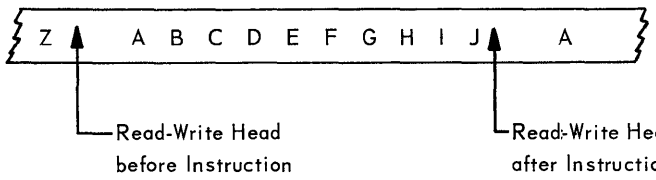
$(T)_f$ or $(E)_f$ = $(B)_i$

EXAMPLE

Instruction: 5 2 6001 6010



Tape on Station 2:



HSM Before Execution:

6000	6001	6002	6003	6004	6005	6006	6007	6008	6009	6010	6011
1	2	3	4	T	U	V	W	X	Y	Z	4

HSM After Execution:

6000	6001	6002	6003	6004	6005	6006	6007	6008	6009	6010	6011
1	A	B	C	D	E	F	G	H	I	J	4

Final Settings: $(C)_f = 6011$ $(E)_f = 6010$

READING REVERSE

GENERAL DESCRIPTION

The Read Reverse Simo 1 (RR1) or Read Reverse Simo 2 (RR2) instruction transfers a series of consecutive characters from magnetic tape moving in a reverse direction into the HSM. The transfer of characters begins with the first character following a gap and ends when the next gap is sensed or the specified HSM area is filled.

FORMAT

OPERATION - 6 (RR1) or 7 (RR2)

N - Specifies Magnetic Tape Station.

A ADDRESS - HSM location to receive the first character.

B ADDRESS - HSM location to receive the last character.

DIRECTION OF OPERATION

Characters are transferred into HSM right to left.

OUTLINE OF OPERATION

Initially, a start signal is sent to the Tape Station specified by N. When the Control is ready to transfer characters, a demand is made on the Processor and two characters are transferred to a HSM diad. If the first character to be transferred addresses an even diad position, only that character is transferred. The S or C Register is decremented by two to address the next diad. The cycle is repeated until a gap on tape is encountered or address equality occurs. If address equality occurs before a gap is reached, no further characters are transferred but the tape continues to move to the next gap.

FINAL SETTINGS

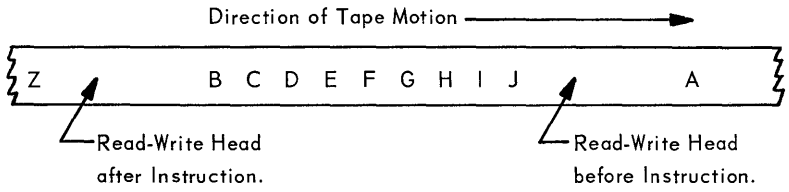
$(C)_f$ or $(S)_f$ = HSM location one to the left of the last character read.

$(E)_f$ or $(T)_f$ = $(B)_i$

EXAMPLE

Instruction: 6 3 8030 8021

Tape on Station #3



HSM Before Execution:

8021	8022	8023	8024	8025	8026	8027	8028	8029	8030	8031
0	0	0	0	0	0	0	0	0	0	0

HSM After Execution:

8021	8022	8023	8024	8025	8026	8027	8028	8029	8030	8031
0	B	C	D	E	F	G	H	I	J	0

Final Settings: $(S)_f = 8021$ $(T)_f = 8021$

WRITING

GENERAL DESCRIPTION

The Write Simo 1 (WR1) or Write Simo 2 (WR2) instruction transfers a specified series of consecutive characters from HSM to a Magnetic Tape Station. Writing of magnetic tape begins after a gap has been generated and ends when the last character has been transferred from the specified HSM area and is recorded on tape.

FORMAT

OPERATION - 8(WR1) or 9(WR2)

N - Specifies Magnetic Tape Station

A ADDRESS - HSM location of first character to be written.

B ADDRESS - HSM location of last character to be written.

DIRECTION OF OPERATION

Characters are transferred from HSM left to right.

Tape movement is forward.

OUTLINE OF OPERATION

Initially, a start signal is sent to the Tape Station specified by N, and the first character or diad of characters (depending on whether A Address is odd or even) is transferred to the Data Register. After an up-to-speed delay, one character at a time is written to tape from the Data Register. When the Data Register requires further loading, a demand is made on the Processor for another diad of characters, and the S or C Register is incremented by two to address the next diad. The cycle is repeated until address equality terminates the operation.

FINAL SETTINGS

$(S)_f$ or $(C)_f$ = HSM location one to the right of the last character written.

$(T)_f$ or $(E)_f$ = B_i

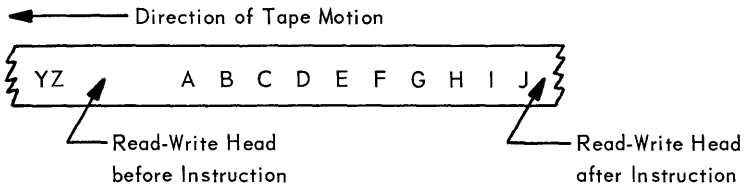
EXAMPLE

Instruction: 9 3 6001 6010

HSM Before and After Execution:

6001	6002	6003	6004	6005	6006	6007	6008	6009	6010
A	B	C	D	E	F	G	H	I	J

Tape on Station #3:



Final Settings: $(C)_f$ = 6011 $(E)_f$ = 6010

ERASING

GENERAL DESCRIPTION

The Erase Simo 1 (ER1) or Erase Simo 2 (ER2) instruction erases a portion of magnetic tape equivalent to the amount of tape utilized in writing the same amount of characters.

FORMAT

OPERATION - *(ER1) or >(ER2)

N - Specifies Magnetic Tape Station

A ADDRESS - Beginning HSM location used for counting the number of characters to be erased.

B ADDRESS - Ending HSM location used for counting the number of characters to be erased.

DIRECTION OF OPERATION

Tape movement is forward.

OUTLINE OF OPERATION

These instructions operate in the same manner as write instructions for magnetic tape with the following exception: No characters are actually written, the tape is merely moved for a period of time that the tape is specified by the A and B addresses. Erasing occurs during the period of time the tape is moving. When address equality is reached, the instruction is terminated immediately. All Read-After-Write errors are ignored. When either a splice or ETW is detected while erasing, the instruction terminates immediately with the Splice Indicator (and ETW Indicator if appropriate) set. If the Splice Indicator is set when the instruction is initiated, splicing is ignored, and erasing is performed in its entirety.

FINAL SETTINGS

$(S)_f$ or $(C)_f$ = One to the right of the last HSM location used to count the erase distance.

$(T)_f$ or $(E)_f$ = $(B)_i$

GENERAL DESCRIPTION

The Control Device Simo 1 (CD1) or Control Device Simo 2 (CD2) instruction causes a specified Magnetic Tape Station to be completely rewound. Once the operation has been initiated, the rewind to BTC or Load Point proceeds totally independent of the Processor, and the designated Simo Mode is free to execute other instructions

FORMAT

OPERATION - 2(CD1) or 3(CD2)

N - Specifies Magnetic Tape Station

A ADDRESS - Zero (0000). Not to be used by programming.

B ADDRESS - $B_0B_1B_2$ = Zero (000). Not to be used by programming.

B_3 = 1 Rewind to BTC (any model Tape Station).

B_3 = 2 Rewind to load point and disconnect on 681 Tape Station. (If this option is used with a 581 or 582 Tape Station, it will be interpreted as a normal rewind.)

B_3 = 4 Rewind one gap.

DIRECTION OF OPERATION

Tape movement is reverse.

OUTLINE OF OPERATION

If the Mode, Control and Tape Station are not busy or inoperable, a rewind command is sent to the Tape Station specified by N, and the Control function designated by B_3 is performed.

FINAL SETTINGS

After rewind is initiated, the registers are available for use by another instruction.

TESTING THE DEVICE

GENERAL DESCRIPTION

The Test Device (TDV) instruction tests the desired status of a specified Magnetic Tape Station and transfers control if the condition or conditions being tested are present. When sensing indicators which are in the 581/582/681 Control by mode, the mode (Simo 1 or Simo 2) must be specified.

FORMAT

OPERATION - S

N - Specifies Magnetic Tape Station

A ADDRESS - Specifies function to be performed as follows:

Character	Bit Position	Symbol	By Mode	Test Function
A_0	$2^0 = 1$	1		Is device inoperable?
A_0	$2^1 = 1$	2		Is tape in motion?
A_0	$2^2 = 1$	4		Has ETW been sensed?
A_0	$2^3 = 1$	8		Is tape positioned on BTC?
A_0	$2^4 = 1$	&		Is tape moving in reverse?
A_0	$2^5 = 1$	-		Is splice detected?
A_1	$2^0 = 1$	1	√	Is there a Parity Error (PE) on read or write?
A_1	$2^1 = 1$	2	√	Is there a Magnetic Tape Alarm (MTA)?
A_1	$2^2 = 1$	4	√	Have A/B Equality and no gap been sensed?
A_1	$2^3 = 1$	8	√	Is the EF/ED Indicator Set?
A_1	$2^4 = 1$	&		Is switch ($\propto$ or β) busy?
A_3	$2^0 = 1$	1		Simo 1 Mode or $\propto$ switch
A_3	$2^1 = 1$	2		Simo 2 Mode or β switch

Unused characters must be zeros and are not to be used by programming.

A_3 must be specified for those functions with a check (√) in the "By Mode" column.

B ADDRESS - HSM location of the next instruction to be executed if the condition(s) being tested is(are) present.

SPECIAL CONDITIONS

STP is performed if the condition(s) specified by the A Address is (are) present.

OUTLINE OF OPERATION

If the A_3 character is "zero", then the device indicators only are being tested. The device indicators are individually picked by the bits of the A_0 character. To execute a TDV instruction to device indicators, it is required that the Tape Station, specified by the N character, be connected to the Processor through the Control switch. If the Tape Station is connected to the switch, the sense will be performed (operating or not). If the Tape Station is not busy, then it will be connected and the sense performed. The test cannot be executed if the Tape Station specified is not or cannot be connected at this time. If the test cannot be performed, the instruction will terminate immediately with a Busy or Inoperable interrupt.

If the A_3 character is not "zero", then the mode indicators only are being tested. The mode indicators are individually picked by the bits of the A_1 character. To execute a TDV instruction to mode indicators, it is not required that the Tape Station, specified by the N character, be connected to the Processor through the Control switch. The N character will, in effect, select the Control Module (each device on the Control Module would select the same Control Module).

RCA 501 and RCA 301 EF and ED symbols will set the EF/ED Indicator.

$(A)_f = (A)_i$

$(B)_f = (B)_i$

TIMING

Many variables are involved in magnetic tape timing. Two generalized formulas plus a specification chart are therefore provided for timing magnetic tape operations.

READING, WRITING or ERASING

$$\text{Time (ms)} = (\#\ \text{Records}) \left[\frac{\frac{\text{Characters/Record}}{\text{Density}}}{\text{Tape Speed (inches/ms.)}} + \frac{\text{Start Time}}{\text{Records/Block}} \right]$$

REWIND (independent operation)

$$\text{Time (ms.)} = (\#\ \text{Records}) \left[\frac{\frac{\text{Characters/Record}}{\text{Density}}}{\text{(Tape Speed)}} + \frac{\frac{\text{Gap Size}}{\text{Records/Block}}}{\text{(Rewind Multiplier)}} \right]$$

TAPE STATION	581	582	681	582 Long Gap	681 (100KC)
Start Time *	3.5	5.5	7.33	11.0	7.33
Density (characters/inch)	333	667	800	667	667
Tape Speed (inches/ms.)	.1	.1	.15	.1	.15
Nominal Gap Size (inches)	.34	.54	1.1	1.1	1.1
Rewind Multiplier	1	1.5	1.5	1.5	1.5

*The Read-After-Write Delay on the 582 and 681 Tape Stations is included.

EXAMPLE #1

Reading one 175 – character record from a 581 Tape Station

$$\text{Time (ms)} = 1 \left[\frac{\frac{175}{333}}{.1} + \frac{3.5}{1} \right]$$

$$= 1 \left[\frac{.526}{.1} + \frac{3.5}{1} \right]$$

$$= 8.76$$

EXAMPLE #2

Rewinding 4000 200 – character records (10 records block) on a 582 Tape Station

$$\text{Time (ms.)} = 4000 \left[\frac{\frac{200}{667} + \frac{.54}{10}}{(.1)\quad(1.5)} \right]$$

$$= 4000 \left[\frac{.3 + .054}{.15} \right]$$

$$= 9440$$

When a write instruction is directed to a Tape Station positioned at BTC, the start time is approximately 55 milliseconds. When the Long Gap Switch is set on a 582, the start time is 9 milliseconds rather than 3.5 milliseconds.

ACCURACY CONTROL

FEATURES

Accuracy control features for the magnetic tape devices include:

1. Dual-Recording. Either of the two recorded spots for a single character may be missing and the bit can still be read.

2. Automatic Read-After-Write. Checks the parity of the character on tape by reading each character after it has been written (582 and 681 only).

3. Parity check on data read.

4. Write Lockout. Prevents writing or erasing of information except on designated reels of tape.

5. End of Reel Stop, Beginning of Tape Control (BTC) and End of Tape Warning (ETW).

6. Rollback and Flaw Detection.

7. Echo check of the write head for data written (581 only).

8. Rewind with Parity Check (581 only).

OPERABLE-INOPERABLE

If, during Instruction Access, the Mode, Control or Tape Station is busy or inoperable, the instruction will terminate immediately with the Busy or Inoperable Interrupt Indicator set. The following conditions render the device inoperable: malfunction, device not connected, and power off.

MODELS 582/681 WRITE LOGIC

As a block of characters is written, leading (Item Separator) and trailing (Equal) guard characters will be automatically placed on it by the Control. If a Read-After-Write error occurs, the write will be terminated after writing a trailing guard character, and the Mode Terminated Abnormally Interrupt Indicator will be set.

When a splice marker is detected while writing, the instruction will be terminated after a trailing guard character is written. An erase instruction will terminate immediately, but a write instruction will not terminate until the read-after-write check is received from the tape station. In either case the Splice Indicator will be set.

MODELS 582/681 READ LOGIC

Guard characters are not transferred to HSM. If the leading and trailing guard characters are present and there are no parity errors, the instruction will terminate normally. If the leading guard character is not present, information will not be transferred to HSM and the appropriate register will not be stepped. At the end of the block of information, the Control will check for the trailing guard character. If it is not present, this block of information will be treated as gap and the read will continue. If the leading guard character was missing but the trailing guard character is present, the tape will be stopped in the gap, and the instruction terminated with the corresponding Mode Terminated Abnormally Interrupt Indicator set. When a read error occurs, the Control replaces the incorrect character with an Error character (e). The corresponding Mode Terminated Abnormally interrupt Indicator is set as the first "e" is placed in HSM; however, the read continues with Error characters replacing all incorrect characters detected.

The same guard logic will be used for reading in reverse, except that the leading guard character is considered the trailing guard character and the trailing guard character is considered the leading guard character. Any one-character block that is not an ED or EF and has at least one guard character will be considered a read parity error (RE). All two-character blocks with at least one guard character will be considered as incorrect parity blocks.

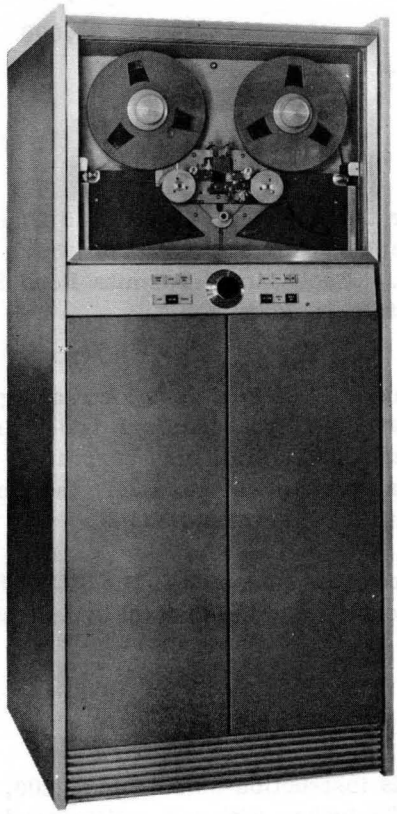
MODEL 581 WRITE LOGIC

The 581 Tape Station does not utilize guard character logic. Information written to a 581 Tape Station is echo checked to insure that proper parity characters are received at the write head. An echo check parity error is considered as an inoperable condition and causes the write to be terminated immediately with the corresponding Mode Terminated Abnormally Interrupt Indicator set; the tape station appears inoperable. When ETW (End Tape Warning) is sensed, the write is not terminated but continues to completion.

MODEL 581 READ LOGIC

When a read error occurs, the Control replaces the incorrect character with an Error character (e). The corresponding Mode Terminated Abnormally Interrupt Indicator is set as the first "e" is placed in HSM; however, the read continues with Error characters replacing all incorrect characters detected. A MTA error occurs on all two-character blocks and on any one-character block that is not an EF or ED.

XII MODEL 3484 AND 3485 TAPE STATIONS



MODELS 3484 AND 3485 TAPE STATIONS

GENERAL DESCRIPTION

Two types of tape stations are available with 3301 Systems; the Model 3484 and the Model 3485. The devices are similar both in appearance and operating techniques; the only difference is in the speeds of the two devices. The Model 3484 and 3485 Tape Stations are tape and reel compatible with 7330, 727 and 729 tape stations. These Tape Stations are capable of reading and writing on 1/2-inch wide, seven-channel, magnetic polyester tape in binary or binary-coded decimal recording. Tapes may also be read and written in RCA recording, and reverse reading is permitted in RCA recording. Information transfer rates are a function of density as follows: (C)

Recording Density (char./inch)	Information Transfer Rate (char./sec)	
	3484	3485
200	15,000	30,000
556	41,700	83,400
800	60,000	'120,000
Tape Speed	75	150
Rewind	150	300

CONTROL

Two Models of the Control for the Model 3484 and 3485 Tape Stations (2 x 6 Dual Tape Channel or 2 x 12 Dual Tape Channel) are available which operate up to six and up to 12 tape stations, respectively. Each model permits Read-Read, Read-Write or Write-Write processing on the tape stations connected.

The Control contains two-character Data Registers for reading and writing data. Most data transfers between the Control and the Processor are two-character (diad) transfers, however, character addressable tape instructions are permitted. Since consecutive memory cycles are unnecessary for data transmission to HSM, the Control signals the Processor when it requires a machine cycle for data transmission.

Two modes of recording are program selectable: The RCA Mode and the Compatible Mode, Recording mode designation is contained in the Control by tape station.

RCA MODE

In the RCA Mode the density is instruction-selectable at 200, 556 or 800 characters per inch. Average gap size is 0.75 inches with a 6 millisecond write up-to-speed delay on the 3484 while gap size is .825 inches with a 3.5 ms write up-to-speed delay for the 3485.

Blocks on tape are preceded by a guard character and followed by a guard character and a longitudinal check character. The guard characters and the longitudinal check character are generated and checked in the Control but do not enter HSM.

Standard RCA 3301 EF and ED symbols are used and upon reading set the EF/ED Indicator.

COMPATIBLE MODE

Binary (odd parity) or BCD (even parity) recording is designated along with Compatible Mode selection. A recording density of 200, 556, or 800 characters per inch must also be specified by program. An average gap length of 0.75 inch is produced by 6 millisecond up-to-speed delays on the 3484 while gap size is .825 inches with a 3.5 ms write up-to-speed delay for the 3485.

When reading in the Compatible Mode, the program is responsible for discarding noise blocks. A noise block results from a physical spot in the skipped area that creates a pulse at the read head. This spot occurs as a result of relocating a written record when a defective section of tape is detected. The following chart depicts the various IBM systems and the maximum noise block size for each:

SYSTEM	NOISE BLOCK SIZE
705 III, 7080	Up to 11 characters
7040, 7044, 7090, 7094	Up to 13 characters
7070, 7072, 7074	Up to 3 words
1401, 1410, 1460, 7010	Up to 13 characters

The End of File (EOF) character $(17)_8$ is recorded as a single character block. In some systems, a 3.75 inch gap precedes the EOF. In other systems the EOF is preceded by a .75 inch gap. A tape can be prepared with a 3.75 inch gap ahead of the EOF with the erase instruction.

Following each block on tape is a longitudinal character.

INSTRUCTIONS

Instructions utilized for programming the magnetic tape devices are:

Read Forward Simo 1 (RF1)

Read Forward Simo 2 (RF2)

Read Reverse Simo 1 (RF1)

Read Reverse Simo 2 (RR2)

Write Simo 1 (WR1)

Write Simo 2 (WR2)

Erase Simo 1 (ER1)

Erase Simo 2 (ER2)

Control Device Simo 1 (CD1)

Control Device Simo 2 (CD2)

Test Device (TDV)

These instructions are presented by function under the headings: (1) Controlling the Device, (2) Reading Forward, (3) Reading Reverse, (4) Writing, (5) Erasing, and (6) Testing the Device.

An Address Selection Dial on each Tape Station permits manual selection of the current tape station symbol. Symbol selection is group-limited in accordance with the Control to which the Tape Station is connected. The 24 possible tape stations are instruction addressed and identified by the Address Selection Dial on each tape station as follows:

First 2 x 12				Second 2 x 12			
First 2 x 6		Second 2 x 6		Third 2 x 6		Fourth 2 x 6	
Address Symbol	Selection Dial Number	Address Symbol	Selection Dial Number	Address Symbol	Selection Dial Number	Address Symbol	Selection Dial Number
1	01	9	11	A	21	I	31
2	02	¬	12	B	22	+	32
3	03	#	13	C	23	.	33
4	04	@	14	D	24	;	34
5	05	(	15	E	25	:	35
6	06	)	16	F	26	'	36

CONTROLLING THE DEVICE

GENERAL DESCRIPTION

The Control Device Simo 1 (CD1) or Control Device Simo 2 (CD2) instruction sets the recording mode and/or density for a specified Magnetic Tape Station or causes the station to be rewound. Mode, density and rewind options may be selected in combination; however, only one of each class may be used at one time. Once the operation has been initiated, the rewind to BTC or Load Point proceeds totally independent of the Processor, and the designated Simo Mode is free to execute other instructions.

FORMAT

OPERATION - 2(CD1) or 3(CD2)

N - Specifies Magnetic Tape Station

A ADDRESS - Zero (0000). Not to be used by programming.

B ADDRESS - B_0 B_1 = Zero (00). Not to be used by programming.

B_2 B_3 = designate control options as follows:

Character	Bit Position	Symbol	Control Option
B_2	$2^0 = 1$	1	Set RCA Mode
B_2	$2^1 = 1$	2	Set Compatible Binary (odd parity) Mode
B_2	$2^2 = 1$	4	Set Compatible BCD (even parity) Mode
B_2	$2^3 = 1$	8	Set for 200 characters/inch density
B_2	$2^4 = 1$	&	Set for 556 characters/inch density
B_2	$2^5 = 1$	-	Set for 800 characters/inch density
B_3	$2^0 = 1$	1	Rewind to BTC
B_3	$2^1 = 1$	2	Rewind to Load Point and disconnect
B_3	$2^2 = 2$	4	Rewind one gap

DIRECTION OF OPERATION

Tape movement is reverse on rewind options.

OUTLINE OF OPERATION

With a rewind option if the Mode, Control and Tape Station are not busy or inoperable, the rewind command is sent to the Tape Station specified by N, and the control function designated by B3 is performed. When a recording mode or density option is specified, the appropriate condition is set up in the Control, and the instruction is terminated immediately.

FINAL SETTINGS

$(S)_f$ or $(C)_f = (A)_i$

$(T)_f$ or $(E)_f = (B)_i$

After a rewind to BTC or Load Point is indicated, the registers are available.

READING FORWARD

GENERAL DESCRIPTION

The Read Forward Simo 1 (RF1) or Read Forward Simo 2 (RF2) instruction transfers a series of consecutive characters from magnetic tape, moving in a forward direction into HSM. Reading begins with the first character following a gap and ends when the next gap is sensed or the specified HSM area is filled.

FORMAT

OPERATION - 4(RF1) or 5(RF2)

N - Specifies Magnetic Tape Station

A ADDRESS - HSM location to receive the first character.

B ADDRESS - HSM location to receive the last character.

DIRECTION OF OPERATION

Characters are transferred into HSM left to right.

OUTLINE OF OPERATION

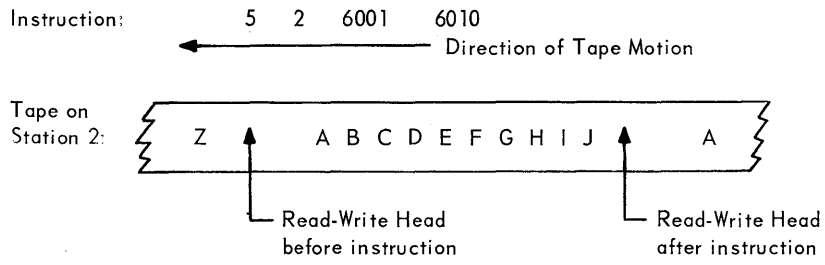
Initially, a start signal is sent to the Tape Station specified by N. When the Control is ready to transfer characters, a demand is made on the Processor and two characters from the Data Register are transferred to a HSM diad. If the first character to be transferred addresses an odd diad position, only that character is transferred. The C or S Register is incremented by two to address the next diad. The cycle is repeated until a gap on tape is encountered or address equality occurs. If address equality occurs before a gap is reached, no further characters are transferred, but the tape continues to move to the next gap.

FINAL SETTINGS

$(S)_f$ or $(C)_f$ = HSM location one to the right of the last character read.

$(T)_f$ or $(E)_f = (B)_i$

EXAMPLE



HSM Before Execution:

6000	6001	6002	6003	6004	6005	6006	6007	6008	6009	6010	6011
1	2	3	4	T	U	V	W	X	Y	Z	4

HSM After Execution:

6000	6001	6002	6003	6004	6005	6006	6007	6008	6009	6010	6011
1	A	B	C	D	E	F	G	H	I	J	4

Final Settings: $(C)_f = 6011$ $(E)_f = 6010$

READING REVERSE

GENERAL DESCRIPTION

The Read Reverse Simo 1 (RR1) or Read Reverse Simo 2 (RR2) instruction transfers a series of consecutive characters from magnetic tape moving in a reverse direction into the HSM. The transfer of characters begins with the first character following a gap and ends when the next gap is sensed or the specified HSM area is filled. These instructions are applicable only when operating in the RCA Mode.

FORMAT

OPERATION - 6(RR1) or 7(RR2)

N - Specifies Magnetic Tape Station.

A ADDRESS - HSM location to receive the first character.

B ADDRESS - HSM location to receive the last character.

DIRECTION OF OPERATION

Characters are transferred into HSM right to left.

OUTLINE OF OPERATION

Initially, a start signal is sent to the Tape Station specified by N. When the Control is ready to transfer characters, a demand is made on the Processor and two characters are transferred to a HSM diad. If the first character to be transferred addresses an even diad position, only that character is transferred. The S or C Register is decremented by two to address the next diad. The cycle is repeated until a gap on tape is encountered or address equality occurs. If address equality occurs before a gap is reached, no further characters are transferred but the tape continues to move to the next gap.

FINAL SETTINGS

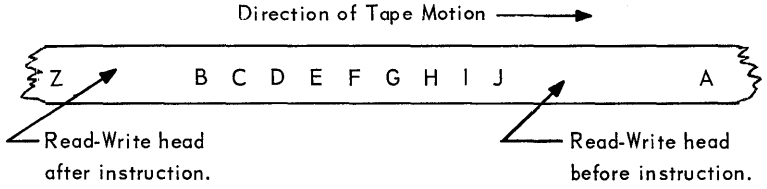
$(C)_f$ or $(S)_f$ = HSM location one to the left of the last character read.

$(E)_f$ or $(T)_f$ = $(B)_i$

EXAMPLE

Instruction: 6 3 8030 8021

Tape on Station #3



HSM Before Execution:

8021	8022	8023	8024	8025	8026	8027	8028	8029	8030	8031
0	0	0	0	0	0	0	0	0	0	0

HSM After Execution:

8021	8022	8023	8024	8025	8026	8027	8028	8029	8030	8031
0	B	C	D	E	F	G	H	I	J	0

Final Settings: $(S)_f = 8021$ $(T)_f = 8021$

WRITING

GENERAL DESCRIPTION

The Write Simo 1 (WR1) or Write Simo 2 (WR2) instruction transfers a specified series of consecutive characters from HSM to a Magnetic Tape Station. Writing of magnetic tape begins after a gap has been generated and ends when the last character has been transferred from the specified HSM area and is recorded on tape.

FORMAT

OPERATION - 8(WR1) or 9(WR2)

N - Specifies Magnetic Tape Station

A ADDRESS - HSM location of first character to be written.

B ADDRESS - HSM location of last character to be written.

DIRECTION OF OPERATION

Characters are transferred from HSM left to right.

Tape movement is forward.

OUTLINE OF OPERATION

Initially, a start signal is sent to the Tape Station specified by N, and the first character or diad of characters (depending on whether A Address is odd or even) is transferred to the Data Register. After an up-to-speed delay, one character at a time is written to tape from the Data Register. When the Data Register requires further loading, a demand is made on the Processor for another diad of characters, and the S or C Register is incremented by two to address the next diad. The cycle is repeated until address equality terminates the operation.

FINAL SETTINGS

$(S)_f$ or $(C)_f$ = HSM location one to the right of the last character written.

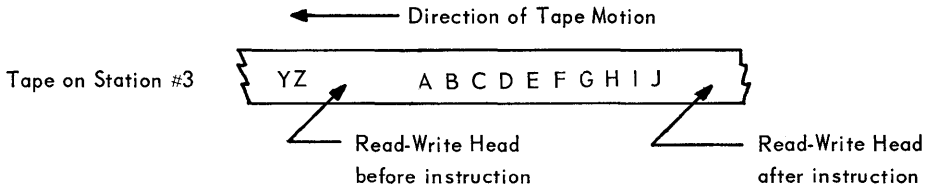
$(T)_f$ or $(E)_f = B_i$

EXAMPLE

Instruction: 9 3 6001 6010

HSM Before and After Execution:

6001	6002	6003	6004	6005	6006	6007	6008	6009	6010
A	B	C	D	E	F	G	H	I	J



Final Settings: $(C)_f = 6011$ $(E)_f = 6010$

ERASING

GENERAL DESCRIPTION

The Erase Simo 1 (ER1) or Erase Simo 2 (ER2) instruction erases a portion of magnetic tape equivalent to the amount of tape utilized in writing the same amount of characters. Erasing is based on the 200 character/inch density.

FORMAT

OPERATION - *(ER1) or > (ER2)

N - Specifies Magnetic Tape Station

A ADDRESS - Beginning HSM location used for counting the number of characters to be erased.

B ADDRESS - Ending HSM location used for counting the number of characters to be erased.

DIRECTION OF OPERATION

Tape movement is forward.

OUTLINE OF OPERATION

These instructions operate in the same manner as write instructions for magnetic tape with the following exception: No characters are actually written; the tape is merely moved for a period of time that the tape is specified to run while writing the number of characters specified by the A and B addresses. Erasing occurs during the period of time the tape is moving. When address equality is reached, the instruction is terminated immediately. All Read-After-Write errors are ignored.

FINAL SETTINGS

$(S)_f$ or $(C)_f$ = One to the right of the last HSM location used to count the erase distance.

$(T)_f$ or $(E)_f = (B)_i$

GENERAL DESCRIPTION

The Test Device (TDV) instruction tests the desired status of a specified Magnetic Tape Station and transfers control if the condition or conditions being tested are present. When sensing indicators which are in the Control by mode, the Mode (Simo 1 or Simo 2) must be specified.

FORMAT

OPERATION - S

N - Specifies Magnetic Tape Station

A ADDRESS - Specifies function to be performed as follows:

Character	Bit Position	Symbol	By Mode	Test Function
A_0	$2^0 = 1$	1		Is device inoperable?
A_0	$2^1 = 1$	2		Is tape in motion?
A_0	$2^2 = 1$	4		Has ETW been sensed?
A_0	$2^3 = 1$	8		Is tape positioned on BTC?
A_0	$2^4 = 1$	&		Is tape moving in reverse?
A_1	$2^0 = 1$	1	√	Is there a Parity Error (PE) on Read or Write?
A_1	$2^1 = 1$	2	√	Is there a Magnetic Tape Alarm (MTA)?
A_1	$2^2 = 1$	4	√	Have A/B Equality and no gap been sensed?
A_1	$2^3 = 1$	8	√	Is the EF/ED indicator set?
A_1	$2^4 = 1$	&		Is Switch (α or β) busy?
A_3	$2^0 = 1$	1		Simo 1 Mode or α Switch
A_3	$2^1 = 1$	2		Simo 2 Mode or β Switch

A_3 must be specified for those functions with a check (√) in the "By Mode" column.

Unused characters must be zeros and are not to be used by programming.

B ADDRESS - HSM location of the next instruction to be executed if the condition(s) being tested is(are) present.

SPECIAL CONDITIONS

STP is performed if the condition(s) specified by the A Address is(are) present.

OUTLINE OF OPERATION

If the A_3 character is "zero", then the device indicators only are being tested. The device indicators are individually picked by the bits of the A_0 character. To execute a TDV instruction to device indicators, it is required that the Tape Station, specified by the N character, be connected to the Processor through the Control switch. If the Tape Station is connected to the switch, the sense will be performed (operating or not). If the Tape Station is not busy, then it will be connected and the sense performed. The test cannot be executed if the Tape Station specified is not or cannot be connected at this time. If the test cannot be performed, the instruction will terminate immediately with a Busy or Inoperable interrupt.

If the A_3 character is not "zero", then the mode indicators only are being tested. The mode indicators are individually picked by the bits of the A_1 character. To execute a TDV instruction to mode indicators, it is not required that the Tape Station, specified by the N character, be connected to the Processor through the Control switch. The N character will, in effect, select the Control Module (each device on the Control Module would select the same Control Module).

FINAL SETTINGS

$(A)_f = (A)_i$

$(B)_f = (B)_i$

TIMING

Many variables are involved in magnetic tape timing. Two generalized formulas plus a specification chart are therefore provided for timing magnetic tape operations.

READING, WRITING or ERASING

$$\text{Time (ms)} = (\#\ \text{Records}) \left[\frac{\frac{\text{Characters/Record}}{\text{Density}}}{\text{Tape Speed (inches/ms.)}} + \frac{\text{Start Time + RAW}}{\text{Records/Block}} \right]$$

REWINDING (independent operation)

$$\text{Time (ms)} = (\#\ \text{Records}) \left[\frac{\frac{\text{Characters/Record}}{\text{Density}}}{\text{(Tape Speed)}} + \frac{\frac{\text{Gap Size}}{\text{Records/Block}}}{\text{(Rewind Multiplier)}} \right]$$

	3485		3484	
Factors	Compatible Mode	RCA Mode	Compatible Mode	RCA Mode
Density (characters/inch)	200,556 or 800	200,556 or 800	200,556 or 800	200,556 or 800
Start Time	3.5ms	3.5ms	6.ms	6.ms
Read-After Write Stop Delay (RAW)	2.ms	2.ms	4.ms	4.ms
Tape Speed (inches/ms.)	.15	.15	.075	.075
Nominal Gap Size	.825	.825	.75	.75
Rewind Multiplier	2.	2.	2.	2.

When a Tape Station is positioned at BTC, the start time is approximately 50 milliseconds.

ACCURACY CONTROL

FEATURES

Accuracy control features include:

1. Automatic Read-After-Write. Checks the parity of the character on tape by reading character after it has been written.

2. Lateral Parity Check. Each character on tape includes a lateral parity bit which is verified in the Control during reading.

3. Longitudinal Check Character. In a Write operation, a longitudinal check character is developed in the Control and follows the block on tape. Each block is checked for longitudinal parity in a Read operation. If any data bit track of the block including the check character is read as having an incorrect number of bits, a parity error results.

4. Write Lockout. Prevents writing or erasing of information except on designated reels of tape.

5. Beginning and end of tape markers and detection logic.

OPERABLE-INOPERABLE

If during Instruction Access the Mode, Control or Tape Station is busy or inoperable, the instruction will terminate immediately with the Busy or Inoperable Interrupt Indicator set. The following conditions render the device inoperable: malfunction, device not connected, and power off.

READ AND WRITE ERRORS

When a read error occurs, the Control replaces the incorrect character with an Error Charactor (e). The corresponding Mode Terminated Abnormally Interrupt Indicator is set as the first Error Character is placed in HSM; however, the read continues with "e"s replacing all incorrect characters detected. If a Read-After-Write error occurs, the write is terminated, and the Mode Terminated Abnormally Interrupt Indicator is set.

GUARD CHARACTER LOGIC (RCA MODE)

As a block of characters is written, leading and trailing guard characters are automatically placed on tape by the Control. When reading, guard characters are not transferred to HSM. If the leading guard character is not present, information will not be transferred to HSM, and the appropriate register will not be stepped. At the end of the block of information, the Control will check for the trailing guard character. If neither are present, and the block does not exceed 15 characters, the block is treated as a gap, and the read continues. If the block exceeds 15 characters when neither guard characters are present, the tape is stopped, and the MTA and Mode Terminated Abnormally Interrupt Indicators are set. If the leading guard character was missing but the trailing one is present, the tape is stopped in the gap, and the instruction is terminated with the corresponding Mode Terminated Abnormally Interrupt Indicator set.

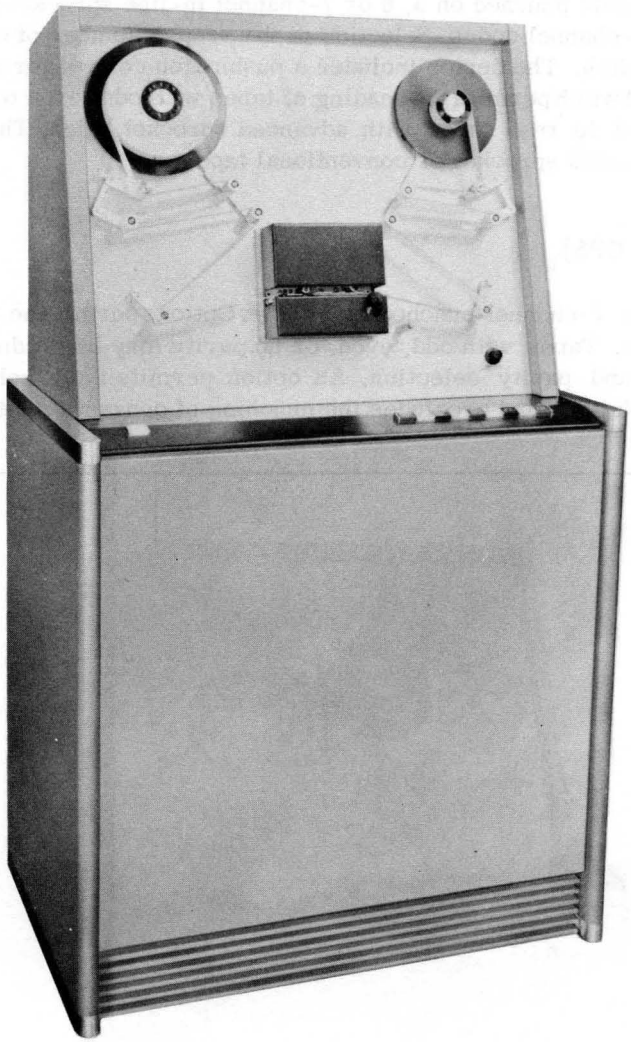
When reading in reverse, the same guard character logic is used.

EOF AND NOISE BLOCKS (COMPATIBLE MODE)

On noise blocks of less than nine characters, the MTA and Mode Terminated Abnormally Interrupt Indicators are set, but the tape is not stopped until a valid gap is reached. On noise blocks of more than eight characters, the Parity Error and Mode Terminated Abnormally Interrupt Indicators are set, and the tape is stopped immediately. Noise blocks of more than eight characters are handled the same as blocks with incorrect parity.

When a block is read that consists of only an EOF $(17)_8$ and is followed by a longitudinal check character, the EF/ED indicator is set. If what appears to be an incorrect parity, one-character block is followed by a longitudinal check character that has a value of $(17)_8$, the EF/ED. Parity Error and Mode Terminated Abnormally Interrupt Indicators will be set. When this occurs, the probability is that the one-character block was an incorrect parity EOF and not noise. At this point, the program decides the course of action.

XIII PAPER TAPE DEVICES



PAPER TAPE READER

GENERAL DESCRIPTION

The RCA 3301 features a variety of devices for reading and punching 5, 6, 7 or 8-channel paper tape. Gapless tape, tape with odd, even, or no parity, and tape with advanced sprocket holes may be read and punched. Paper tape reading and punching may be done simultaneously. These devices are offered at the following rates.

Paper Tape Reader, 1000 CPS (Characters Per Second)

Paper Tape Punch, 100 CPS

Paper Tape Reader/Punch, 100 CPS

PAPER TAPE READER (1000 CPS)

This reader accepts data punched on 5, 6 or 7-channel in-line sprocket paper tape. An option permits reading of 8-channel codes. Selection of the proper number of channels to be read is via a Code Level Switch. The device includes a pushbutton control for reading gapless tapes at 500 CPS. A Parity Switch permits the reading of tapes with odd, even or no parity. A special feature can be added to read tapes with advanced sprocket holes. This feature affords the option of reading advanced sprocket or conventional tape.

PAPER TAPE PUNCH (100 CPS)

This punch produces 7-channel punched paper tape. Options permit the additional punching of 5 or 8-channel codes. Tapes with odd, even, or no parity may be produced. Switches are included for channel and parity selection. An option permits the punching of only 6-channel advanced sprocket hole tape and precludes the punching of conventional tapes.

PAPER TAPE PUNCH

PAPER TAPE READER/PUNCH

PAPER TAPE READER/PUNCH (100 CPS)

This device consists of a 100 CPS Paper Tape Reader and a 100 CPS Paper Tape Punch housed in the same cabinet. Reading and punching of 7-channel paper tape is permitted. Optional features permit the reading and punching of 5 and 8-channel codes. Gapless tapes and tapes with odd, even, or no parity may be read or punched. The device contains controls or switches for parity, channel, and gapless selection. Special features can be added to read and/or punch tapes with advanced sprocket holes. The punching feature excludes punching of conventional tapes; the reading feature does not.

CONTROL

The Control can accommodate the following combinations of paper tape devices:

Paper Tape Reader (1000 CPS)

Paper Tape Reader (1000 CPS) and Paper Tape Punch (100 CPS)

Paper Tape Reader/Punch (100 CPS)

Paper Tape Punch (100 CPS)

Paper Tape codes are inverted by the Control in transmitting to and from HSM. A "zero bit" in HSM becomes a hole on paper tape; a "one bit" in HSM is "no hole" on paper tape (see Figure XIII-1). Exceptions to this process occur when bits are supplied to HSM by the Control, as in the five-level and eight-level modes.

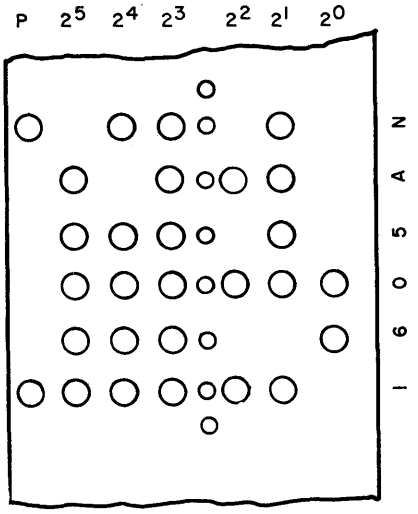


Figure XIII-1. Recording on Paper Tape

The Control contains logic which recognizes the ED and the EF codes. Upon reading of either, the EF/ED Indicator in the Control is set. This indicator is reset by the next Input/Output instruction to the device.

In the 5-channel mode, a zero bit in the 2^5 position (not punched on 5-channel tape) is transmitted to HSM as a zero bit by the Control. Parity is generated and transmitted to HSM. In the 6-channel mode, all six bits are inverted and transmitted to HSM. Parity is generated and transmitted to HSM. In the 7-channel mode, six information bits are inverted, and parity is transmitted to HSM. In the 8-channel mode, each character on tape requires two HSM locations. The 2^0 through the 2^5 bits are inverted and placed in an HSM location along with a generated parity bit. The 2^6 and 2^7 bits are inverted and placed in the next higher HSM location; the remaining four bit positions are filled with "zero bits", and parity is generated.

INSTRUCTIONS

Instructions utilized for programming the paper tape devices are:

Read Forward Simo 1 (RF1)	Read Forward Simo 2 (RF2)
Read Reverse Simo 1 (RR1)	Read Reverse Simo 2 (RR2)
Write Simo 1 (WR1)	Write Simo 2 (WR2)
Test Device (TDV)	

These instructions are presented by function under the headings: (1) Reading Tape Forward, (2) Reading Tape in Reverse, (3) Punching Tape, and (4) Testing the Device.

READING TAPE FORWARD

GENERAL DESCRIPTION

The Read Forward Simo 1 (RF1) or Read Forward Simo 2 (RF2) instruction reads punched paper tape beginning with the first character following a gap (unless gapless tape has been specified) and ends when the next gap is sensed or the specified HSM area is filled.

FORMAT

OPERATION - 4 (RF1) or 5 (RF2)

N - K if first Paper Tape Reader; L if second Paper Tape Reader

A ADDRESS - HSM location to receive the first character.

B ADDRESS - HSM location to receive the last character

DIRECTION OF OPERATION

Characters are transferred into HSM left to right.

Tape movement is forward.

SPECIAL CONDITIONS

If gapless tape has not been specified and A/B equality occurs before a gap is detected, an indicator is set which may be sensed by the TDV instruction.

OUTLINE OF OPERATION

One character is transferred to the HSM location specified by the S or C Register, and the register is incremented by one. The cycle is repeated until a gap on tape is encountered or address equality is reached. If address equality occurs before a gap is reached, no further characters are transferred, but the tape (unless gapless has been specified) continues to move to the next gap.

FINAL SETTINGS

$(S)_f$ or $(C)_f$ = HSM location one to the right of the last character read.

$(T)_f$ or $(E)_f$ = $(B)_i$

GENERAL DESCRIPTION

The Read Reverse Simo 1 (RR1) or Read Reverse Simo 2 (RR2) instruction reads punched paper tape beginning with the first character following a gap (unless gapless tape has been specified) and ends when the next gap is sensed or the specified HSM area is filled.

FORMAT

OPERATION - 6 (RR1) or 7 (RR2)

N - K if first Paper Tape Reader, L if second Paper Tape Reader

A ADDRESS - HSM location to receive the first character.

B ADDRESS - HSM location to receive the last character.

DIRECTION OF OPERATION

Characters are transferred into HSM right to left.

Tape movement is forward.

SPECIAL CONDITIONS

If gapless tape has not been specified and A/B equality occurs before a gap is detected, an indicator is set which may be sensed by the TDV instruction.

OUTLINE OF OPERATION

One character is transferred to the HSM location specified by the S or C Register, and the register is decremented by one. The cycle is repeated until a gap on tape is encountered or address equality is reached. If address equality occurs before a gap is reached, no further characters are transferred, but the tape (unless gapless has been specified) continues to move to the next gap.

FINAL SETTINGS

$(S)_f$ or $(C)_f$ = HSM location one to the left of the last character read.

$(T)_f$ or $(E)_f$ = $(B)_i$

PUNCHING TAPE

GENERAL DESCRIPTION

The Write Simo 1 (WR1) or Write Simo 2 (WR2) instruction is used for this function. Punching begins with the first character addressed and ends when the last character has been transferred from the specified HSM area and is punched on the paper tape. A three-character gap is automatically generated by the Control unless gapless tape has been specified.

FORMAT

OPERATION - 8 (WR1) or 9 (WR2)

N - O if first Paper Tape Punch, P if second Paper Tape Punch.

A ADDRESS - HSM location of first character to be written.

B ADDRESS - HSM location of last character to be written.

DIRECTION OF OPERATION

Characters are transferred from HSM left to right.

OUTLINE OF OPERATION

One character is transferred from the HSM location specified by the S or C Register to the device for punching. The S or C Register is incremented by one, and the cycle is repeated. The instruction terminates when address equality is reached.

FINAL SETTINGS

$(S)_f$ or $(C)_f$ = HSM location one to the right of the last character written.

$(T)_f$ or $(E)_f$ = $(B)_i$

GENERAL DESCRIPTION

The Test Device (TDV) instruction tests the desired status and transfers control if the condition or conditions being tested are present.

FORMAT

OPERATION - S

N - K if first Paper Tape Reader, L if second Paper Tape Reader

O if first Paper Tape Punch, P if second Paper Tape Punch

A ADDRESS - Specifies function to be performed as follows:

Device	Character	Bit Position	Symbol	Test Function
Paper	A_0	$2^0 = 1$	1	Is device inoperable?
Tape	A_0	$2^1 = 1$	2	Is device operating (Busy)?
Reader	A_0	$2^3 = 1$	8	Is there a parity error (PE)?
	A_1	$2^2 = 1$	4	Have A/B equality and no gap been sensed?
	A_1	$2^3 = 1$	8	Is the EF/ED Indicator set?
Paper	A_0	$2^0 = 1$	1	Is device inoperable?
Tape	A_0	$2^1 = 1$	2	Is device operating (Busy)?
Punch	A_0	$2^3 = 1$	8	Is there a parity error (PE)?

Unused characters must be zeros and are not to be used by programming.

B ADDRESS - HSM location of the next instruction to be executed if the condition(s) being tested is(are) present.

SPECIAL CONDITIONS

STP is performed if the condition(s) specified by the A Address is(are) present.

FINAL SETTINGS

$(A)_f = (A)_i$

$(B)_f = (B)_i$

XIV TIMING

SHARING HSM

Simultaneity is achieved by permitting the operating modes to receive a machine cycle for HSM access when requested. This is accomplished through a technique known as "time sharing" and is feasible since Input/Output instructions need to access High Speed Memory for only a fraction of the time they are in progress. For most of their execution times, Input/Output instructions must wait for some mechanical action in the Input/Output device to occur (e.g., card movement, tape movement, print drum revolution, etc.). The percent of time that each I/0 device accesses HSM out of the total execution is given in the following table:

DEVICE	MEMORY ACCESS %
Card Reader Model 329-1 (Translate Mode)	0.12
Card Reader Model 329-2 (Translate Mode)	0.19
Card Punch	0.04
100 CPS Paper Tape Reader/Punch	0.02
1000 CPS Paper Tape Reader	0.19
100 CPS Paper Tape Punch	0.02
120-Column On-Line Printer (Synchronous)	0.19
120-Column On-Line Printer (Asynchronous	0.15
160-Column On-Line Printer (Synchronous)	0.26
160-Column On-Line Printer (Asychronous)	0.21
581 Tape Station	3.22
582 Tape Station	6.43
681 Tape Station	11.58
3484 Tape Station	1.45 4.02 5.79 ‡
3485 Tape Station	2.90 8.05 11.58*
Data Drum Memory	14.38
Random Access Computer Equipment	8.0
Console Typewriter	.01 (Less than)

* Percentages for 30, 83.4, and 120 KC respectively. ‡ Percentages for 15, 41.7, and 60 KC respectively.

For tape stations the percentage is based upon the character transfer rate only and does not include gap time. For random access devices the times are based on transfer rate only and do not include access time.

INTERRUPT

The time expended to store the status of the processor upon interrupt is 9.43 usec.

INSTRUCTION TIMING

The total time required to process an instruction includes both Instruction Access and Instruction Execution. Instruction Access is constant for all instructions, and takes 1.93 microseconds, whereas Instruction Execution varies with the particular instruction. Instruction timing formulas as presented on the following pages include Instruction Access and the storage of STA where applicable. Indirect addressing (3 usec per level) and indexing (1.93 usec) are not included in the instruction timing formulas.

INSTRUCTION TIMING

	INSTRUCTION	OP CODE	TIMING IN MICROSECONDS**	EXPOSITORY NOTES
DATA HANDLING	Float Dollar Sign to Non-Zero Numeric	,	3.43n + 4.93 3.43n + 6.43	Non-zero numeric not found Non-zero numeric found n = no. of HSM locations searched
	Locate Absence of Symbol Left Locate Absence of Symbol Right	K L	1.93n + 6.43	n = no. of selected symbols searched
	Symbol Fill Sector	J	1.5n + 1.93	n = no. of locations filled
	Symbol Fill to Non-Zero Numeric	,	3.43n + 4.93 3.43n + 3.43	Non-zero numeric not found Non-zero numeric found
	Transfer by Count to Edit Field	÷	4.93n+3.43m+4.93	n = no. of characters to be edited m = no. of edit symbols encountered
	Transfer by Count Left Transfer by Count Right	M N	3n + 1.93	n = no. of characters transferred
	Transfer by Symbol Left Transfer by Symbol Right	# P	3n + 4.93	n = no. of characters transferred
	Transfer Decade by Count	10	3n + 1.93	n = no. of decades transferred
	Translate by Table	A	4.5n + 1.93	n = no. of characters to be translated
ARITHMETIC AND LOGICAL	Add Address Subtract Address	+ –	19.93 22.93	no zone correction zone correction
	Add Data Subtract Data	+ –	4.5n + 4.93	n = no. of characters in each operand
	Divide	+	1.65*	Average time
	Logical "And" Logical Exclusive "Or" Logical Inclusive "Or"	T U Q	4.5n + 1.93	n = no. of characters in each operand
	Multiply	+	T(ms) = .143* " .250* " .352* " .455* " .558* " .660* " .762* " .85*	One significant digit in multiplier Two significant digits in multiplier Three significant digits in multiplier Four significant digits in multiplier Five significant digits in multiplier Six significant digits in multiplier Seven significant digits in multiplier Eight significant digits in multiplier
DECISION AND CONTROL	Compare Address	–	19.93	
	Compare Data	Y	3.43n + 1.93	n = no. of characters compared
	Conditional Transfer of Control	W	1.93 6.43	No transfer of control Transfer of control
	Control Interrupt Logic	⊏	1.93 12.63	RAI options not specified Return After Interrupt option specified
	Halt	.	1.93	
	Load Register	C_R	4.93	
	Programmed Interrupt	.	1.93	
	Repeat	R	4.93	
	Scan Interrupt	<	3.43n + 4.93	n = no. of characters scanned

* Average Time is in Milliseconds
** Time includes Instruction Access & STA where applicable

INSTRUCTION TIMING (Cont'd)

	INSTRUCTION	OP CODE	TIMING IN MICROSECONDS **	EXPOSITORY NOTES
Cont.	Store Register	V	4.93 6.85	A Register Other than A Register
	Tally	X	4.93 9.86 5.36	Tally quantity equal to zero Tally quantity greater than zero Incrementing only (Add 1.93 for each Index Field incremented)
	Unconditional Transfer of Control	W	1.93	
I N P U T / O U T P U T	Control Device Simo 1 Control Device Simo 2	2 3	5.78	Physical tape rewind is independent
	Test Device	S	3.85	No transfer of control Transfer of control
	Erase Simo 1 Erase Simo 2 Read Forward Simo 1 Read Forward Simo 2 Read Reverse Simo 1 Read Reverse Simo 2 Write Simo 1 Write Simo 2	* > 4 5 6 7 8 9		Refer to device description in this section

** Time includes Instruction Access & STA where applicable

I/O DEVICE TIMING

CARD READER

Card reading can be performed at the rate of 67 milliseconds per card on the Model 329-1 Card Reader, and at the rate of 40.8 milliseconds on the Model 329-2 Card Reader.

CARD PUNCH

A card can be punched every 200 milliseconds.

ON-LINE PRINTER

Printing and single line paper advance are accomplished in 60 milliseconds in the Synchronous Mode. Printing and single line paper advance are accomplished in 75 milliseconds in the Asynchronous Mode. Paper advancing after the first line is performed at the rate of 6.67 milliseconds per line. Characters are transferred by diad from HSM to the buffer in eight microseconds per diad.

MAGNETIC TAPE DEVICES

Tape densities in characters per inch for Models 581, 582, and 681 are 333, 667 and 800, respectively. Tape speeds, forward or reverse, in inches per second for Models 581, 582 and 681 are 100, 100 and 150, respectively. Start times in milliseconds for Models 581, 582 and 681 are 3.5, 5.5 and 7.33, respectively.

Tape density in characters per inch for the Model 3484 and Model 3485 is 200, 556, and 800. Tape speed in inches per second for the Model 3484 is 75 and the Model 3485 is 150. The start time in milliseconds is 6 for the 3484 and 3.5 for the 3485.

PAPER TAPE DEVICES

Tape density is ten characters per inch; gap size is three characters. Tape speeds in inches per second for the various paper tape devices are as follows:

1000 CPS Paper Tape Reader	100
1000 CPS Paper Tape Reader	50 (gapless tape)
100 CPS Paper Tape Punch	10
100 CPS Paper Tape Reader/Punch	10

DATA DRUM MEMORY

The transfer rate for the Data Drum Memory is 149KC. The average access time is 8.6 milliseconds.

CONSOLE TYPEWRITER

The output rate is up to 924 characters per minute.

XV ERROR DETECTION AND RECOVERY

INTRODUCTION

The design of the RCA 3301 is based upon the philosophy of continuous computer operation. The interrupt facility enables the automatic execution of programmed error recovery procedures.

PROCESSOR

Processor errors are detected by parity checks performed in the HSM or MMM Memory Register, and the machine Status Level Register. One machine error causes the Systems Error Indicator to be set and interrupt to occur. A second machine error prior to the execution of the Control Interrupt Logic instruction causes the Processor to come to an orderly halt, the P Register to be stored at MMM location R, and the Error Indicator on the operator's console to light up.

When an operation code which is illegal to a particular 3301 System is encountered, the Systems Error Indicator is set and interrupt occurs.

When an address beyond the physical size of HSM is detected, during the transfer of data to HSM or extraction of data from HSM, the Memory Register Parity check is inhibited, the Systems Error Indicator is set, and interrupt occurs upon instruction termination. An attempt to transfer non-existent data (source address outside physical HSM) to HSM will result in the generation of parity errors in the destination HSM locations specified. An attempt to transfer data to non-existent HSM locations will not affect actual HSM locations.

Presence of a 2^4 bit in the LSD of an address will cause indirect addressing to occur. Exceptions to this are the UTC instruction, a "drop through" on the CTC instruction, and "no op" conditions.

During data transfer from right to left, decrementation of an address through 0000 will result in an address of 159,999 regardless of Processor HSM size. Conversely, wrap-around to 0000 will occur only after an address of 159,999 has been achieved regardless of the Processor HSM size employed.

If an invalid N character is used in a Load Register instruction, a drop through to the next instruction will result. If an invalid N character is used in a Store Register instruction, a Systems Error interrupt will occur. N characters invalid to the Load and Store instructions are:

& Ampersand	Y	↑
H		= Equal
- Minus	÷	⌑ Lozenge
Q	, Comma	0 Zero (Invalid to Load Register only)
" Quotation Mark	% Per Cent	

If a non-specified N Character is used in either the Conditional Transfer of Control or Control Interrupt Logic instruction, the instruction terminates, and a drop through to the next instruction occurs.

When the N count in an instruction is specified as 0-45, and the symbol used is not as denoted in Appendix III, the effective count will be as noted below:

SYMBOL	COUNT	SYMBOL	COUNT	SYMBOL	COUNT
⌋	10	+	20	⌊	30
#	11	.	21	$	31
@	12	;	22	*	32
(	13	:	23	>	33
)	14	,	24	<	34
e	15	C_R	25	10	35

Exceptions to this are the arithmetics where the N characters (· $ +) determine the operation (i.e., Multiply and Divide are N character variations of the Add Data instruction).

When the N count in an instruction is specified as 0-15, and the symbol used is not as denoted in Appendix IV, the effective count will be:

COUNT	SYMBOL		
0	&	-	"
1	A	J	/
2	B	K	S
3	C	L	T
4	D	M	U
5	E	N	V
6	F	O	W
7	G	P	X
8	H	Q	Y
9	I	R	Z
10	+	⌊	÷
11	.	$	,
12	;	*	%
13	:	>	↑
14	'	<	=
15	C_R	10	⌑

If the numeric portion (2^0 - 2^3 bit positions) of any character entering an arithmetic operation is greater than the range of bit configurations for the digits 0-9 (i.e., 1010 to 1111 inclusive), the instruction is performed, an invalid result is produced, and no error indication is given.

When the Tally instruction addresses a pre-stored tally quantity which illegally contains zone bits, a parity error may result since the 2^5 bit of the LSD and the 2^4 or 2^5 bits of the MSD of the tally quantity are not processed.

When an N character greater than "3" is erroneously specified in the Scan Interrupt instruction, the N Character is repeatedly examined and decremented until N = 3; at which time the scanning of the Interrupt Indicators begins. However, since the B Register is incremented as the N Register is decremented, the wrong Mask character will be accessed.

INPUT/OUTPUT

Detection and recovery information for abnormal Input/Output conditions are covered in chart form by device on the following pages.

If the N character of an instruction addresses an Input/Output device which is non-existent, or the device is not attached to the system, the instruction terminates, and the Busy or Inoperable Interrupt Indicator is set.

If the TDV instruction is attempting to sense a Magnetic Tape Station and both Simo Mode indicators are erroneously specified (i.e., A_3 2^0 = 1 and 2^1 = 1), the instruction terminates, and the Busy or Inoperable Interrupt Indicator is set.

DETECTION OF ABNORMAL I/O CONDITIONS

DEVICE	DEVICE CONDITION	INTERRUPT INDICATOR SET	TIME OF INTERRUPT	INSTRUCTION TERMINATION	INDICATOR CLEARANCE	COMMENTS
CARD READER	Inoperable (In attempt to address device) – Malfunction – Control connected and no device – Power off – Card jam – Hopper empty – Stacker full	Busy or Inoperable	On attempted instruction execution	At time detected	When operable	
	Inoperable (During execution of instruction) – Malfunction – Power off – Card jam – Three pick failure	Mode Terminated Abnormally	During execution of instruction	At time detected	When operable	
	Operating (Busy) This includes mode busy.	Busy or Inoperable	On attempted instruction execution	At time detected	When not busy	
	Multi-Punch Error (MPE) Photo-Diode Failure (PDF)	Mode Terminated Abnormally	Upon completion of instruction	Upon completion of Read Instruction	Next Read Instruction to device	Automatic rejection of card
	EF Indicator	Mode Terminated Abnormally	Upon completion of instruction	Upon completion of Read Instruction	Next Read Instruction to device	
CARD PUNCH	Inoperable (In attempt to address device) – Malfunction – Control connected and no device – Power off – Card jam	Busy or Inoperable	On attempted instruction execution	At time detected	When operable	
	Inoperable (During physical punching) – Card jam – Hopper empty – Stacker full	Busy or Inoperable	On attempted execution of following instruction to device	At time detected	When operable	

DETECTION OF ABNORMAL I/O CONDITIONS (Cont'd)

DEVICE	DEVICE CONDITION	INTERRUPT INDICATOR SET	TIME OF INTERRUPT	INSTRUCTION TERMINATION	INDICATOR CLEARANCE	COMMENTS
CARD PUNCH (Cont)	Inoperable (During write to buffer)	Mode Terminated Abnormally	During execution of instruction	At time detected	When operable	
	Operating (Busy) This includes mode busy	Busy or Inoperable	On attempted instruction execution	At time detected	When not busy	Busy is Reset
	Punch Station Compare Error (PCE) This is an off-line error.	Busy or Inoperable	On attempted execution of second succeeding Punch instruction to device	At time detected	When 2^2 of A_2 character is present in TDV instruction	Automatic rejection of 2 cards. PCE will be inhibited if P.E. on previous cycle.
	Parity Error (PE) (Memory to buffer and buffer to punch error)	Busy or Inoperable	On attempted execution of next Punch instruction to device	At time detected	When 2^3 of A_2 character is present in TDV instruction	Automatic rejection of card. PCE will be inhibited.
	Buffer Available Off-line punching complete	Off-Line Operation Complete	At termination of normal mode instruction		When 2^0 of A_3 character is present in TDV instruction	
PAPER TAPE READER	Inoperable (On attempt to address device) – Malfunction – Control connected and no device – Power off – Tape not threaded – Tape broken – Supply reel exhausted	Busy or Inoperable	On attempted execution of instruction	At time detected	When operable	
	Inoperable (During execution of instruction) – Malfunction – Power off – Tape broken – Supply reel exhausted	Mode Terminated Abnormally	During execution of instruction	At time detected	When operable	
	Operating (Busy) This includes mode busy	Busy or Inoperable	On attempted execution of instruction	At time detected	When not busy	
	Parity Error (PE)	Mode Terminated Abnormally	Upon completion of instruction	Upon completion of Read Instruction	Next Read instruction to device	

DETECTION OF ABNORMAL I/O CONDITIONS (Cont'd)

DEVICE	DEVICE CONDITION	INTERRUPT INDICATOR SET	TIME OF INTERRUPT	INSTRUCTION TERMINATION	INDICATOR CLEARANCE	COMMENTS
PAPER TAPE READER (Cont)	A/B Equality and No Gap Sensed	Mode Terminated Abnormally	Upon completion of instruction	Upon completion of instruction. Tape will continue to gap	Next Read instruction to device	Inhibited for gapless tape
	EF/ED Indicator	Mode Terminated Abnormally	Upon completion of instruction	Upon completion of instruction	Next Read instruction to device	Inhibited for gapless tape
PAPER TAPE PUNCH	Inoperable (On attempt to address device) - Malfunction - Control connected and no device - Power off	Busy or Inoperable	On attempted execution of instruction	At time detected	When operable	
	Inoperable (During execution of instruction) – Malfunction – Power off	Mode Terminated Abnormally	During execution of instruction	At time detected	When operable	
	Operating (Busy) This includes mode busy	Busy or Inoperable	On attempted execution of instruction	At time detected	When not busy	
	Parity Error (PE)	Mode Terminated Abnormally	During execution of instruction	At time detected	Next Write instruction to device	The bad character will be punched. Operator will be required to delete manually
ON-LINE PRINTER	Inoperable (On attempt to address device) - Malfunction - Control connected and no device - Power off - Paper jam - Halt Button	Busy or Inoperable	On attempted execution of instruction	At time detected	When operable	
	Inoperable (During execution of instruction writing to buffer) – Malfunction – Power off	Mode Terminated Abnormally	During execution of instruction	At time detected	When operable	Printing and Paper Advancing will be inhibited

DETECTION OF ABNORMAL I/O CONDITIONS (Cont'd)

DEVICE	DEVICE CONDITION	INTERRUPT INDICATOR SET	TIME OF INTERRUPT	INSTRUCTION TERMINATION	INDICATOR CLEARANCE	COMMENTS
ON-LINE PRINTER (Cont)	Inoperable (During printing or paper advancing) – Malfunction – Power off – Paper jam – Halt Button	Busy or Inoperable	On attempted execution of next Print and/or P.A. instruction to device	At time detected	When operable	
	Operating (Busy) – Line being printed – Buffer being loaded	Busy or Inoperable	On attempted execution of instruction	At time detected	When line is completely printed	
	Low Paper Supply	Mode Terminated Abnormally	At termination of following Write instruction to device	Upon completion of instruction	When paper supply is replenished	Buffer will accept a Write instruction while paper is advancing.
	Paper Advancing Off line	Does not cause interrupt			When paper movement ceases	
	Parity Error (PE) Memory to buffer and buffer to printer error	Busy or Inoperable	On attempted execution of next Write instruction to device	At time detected	When 2^3 of A_2 character is present in TDV instruction	Line with error will be printed
	Buffer Available Off-line printing complete	Off-Line Operation Complete	At termination of the Normal Mode instruction		When 2^0 of A_3 character is present in TDV instruction	
CONSOLE AND CONSOLE TYPE-WRITER	Inoperable (On Attempt to address device) – Malfunction – Control connected and no device – Power off	Busy or Inoperable	On attempted execution of instruction	At time detected	When operable	
	Inoperable (During execution of instruction) – Malfunction – Power off	Mode Terminated Abnormally	During execution of instruction	At time detected	When operable	
	Operating (Busy)	Busy or Inoperable	On attempted execution of instruction	At time detected	When not busy	
	Console Request	Console Request	At termination of the Normal Mode instruction		Next Read instruction to device	

DETECTION OF ABNORMAL I/O CONDITIONS Cont'd)

DEVICE	DEVICE CONDITION	INTERRUPT INDICATOR SET	TIME OF INTERRUPT	INSTRUCTION TERMINATION	INDICATOR CLEARANCE	COMMENTS
CONSOLE AND CONSOLE TYPE-WRITER (Cont)	Parity Error On Read instruction	Mode Terminated Abnormally	During execution of instruction	At time detected	Next I/O instruction to device	
	Parity Errors On Write instruction	Mode Terminated Abnormally	During execution of instruction	Upon completion of instruction	Next I/O instruction to device	Character "e" will be printed for error char.
	Message Cancel	Mode Terminated Abnormally	During execution of instruction	At time detected	Next I/O instruction to device	
	Long Block A/B equality and "Release" not received.	Mode Terminated Abnormally	At termination of instruction	At time detected	Next I/O instruction to device	
MAGNETIC TAPE	Inoperable (On attempt to address device) – Malfunction – Control connected and no device – Power off – Device does not follow	Busy or Inoperable	On attempted execution of instruction	At time detected	When operable	
	Inoperable (During execution of instruction) – Malfunction – Power off – Master Reel ring	Mode Terminated Abnormally	During execution of instruction	At time detected	When operable	
	Operating Tape in forward or reverse motion	Busy or Inoperable	On attempted execution of instruction	At time detected	When brake is applied	
	ETW – Sensed during Write or Erase to 581 Tape Stations	Mode Terminated Abnormally	At termination of instruction	Upon completion of instruction	When Read Reverse or rewind is received by the Control.	
	ETW – Sensed during Write or Erase Instructions (582/681 only)	Mode Terminated Abnormally	During execution of instruction	At time detected	When marker has been passed over in reverse	On 582/681 T.S. the splice indicator will also be set. This indicator will be reset when marker clears photo-sense area

DETECTION OF ABNORMAL I/O CONDITIONS (Cont'd)

DEVICE	DEVICE CONDITION	INTERRUPT INDICATOR SET	TIME OF INTERRUPT	INSTRUCTION TERMINATION	INDICATOR CLEARANCE	COMMENTS
MAGNETIC TAPE (Cont)	ETW – Indicator set before attempting to execute Write or Erase instruction	Mode Terminated Abnormally	At termination of instruction	Upon completion of instruction	When marker has been passed over in reverse (582,681) On 581 when Read Reverse or rewind is received by the Control.	On 582/681 T.S. the splice indicator will also be set. This indicator will be reset when marker clears photo-sense area.
	BTC – Tape positioned on BTC when attempting to execute a Read Reverse or Rewind One Gap instruction is executed, or tape positioned such that no data exists between the head and BTC when either of the above instructions is executed.	Busy or Inoperable	On attempted execution of instruction	At time detected	When off BTC	If on BTC when a rewind to BTC is executed, the instruction will terminate normally.
	BTC-Tape positioned on BTC when attempting to execute a Read, Write or Erase instruction	Mode Terminated Normally	At termination of instruction	Upon completion of instruction	When off BTC	
	Splice – Detected during Write or Erase instruction	Mode Terminated Abnormally	During execution of instruction	At time detected	When splice marker clears photo-sense area	
	Splice – Indicator set when attempting to execute a Write instruction	Busy or Inoperable	On attempted execution of instruction	At time detected	When splice marker clears photo-sense area	
	Splice – Indicator set when attempting to execute an Erase instruction (If splice marker clears photo-sense area at termination of instruction)	Mode Terminated Normally	At termination of instruction	Upon completion of instruction		
	Splice – Indicator set when attempting to execute an Erase instruction (If splice marker does not clear photo-sense area at termination of instruction)	Mode Terminated Abnormally	At termination of instruction	Upon completion of instruction	When splice marker clears photo-sense area	

DETECTION OF ABNORMAL I/O CONDITIONS (Cont'd)

DEVICE	DEVICE CONDITION	INTERRUPT INDICATOR SET	TIME OF INTERRUPT	INSTRUCTION TERMINATION	INDICATOR CLEARANCE	COMMENTS
MAGNETIC TAPE (Cont)	Parity Error (PE) – On Read instruction	Mode Terminated Abnormally	Upon completion of instruction	Upon completion of instruction	Next I/O instruction to the same Control in the same mode	
	Parity Error (PE) On Write instruction (582/681 only)	Mode Terminated Abnormally	During execution of instruction	At time detected	Next I/O instruction to the same Control in the same mode	
	Magnetic Tape Alarm (MTA) CIG, MCP and Echo Check (581 only)	Mode Terminated Abnormally	During execution of instruction	At time detected	Next I/O instruction to the same Control in the same mode	
	A/B Equality and No Gap Sensed	Mode Terminated Abnormally	At termination of instruction	At time detected	Next I/O instruction to same Control in the same mode	
	EF/ED	Mode Terminated Abnormally	At termination of instruction	At time detected	Next I/O instruction to same Control in the same mode	
	TDV Instruction Two tape stations operating and sensing device indicators on a third unit. Device indicators are individually picked by the A_0 char. of the TDV instruction.	Busy or Inoperable	Before execution of instruction	At time detected		If inhibit is on, instruction will drop through as a no op.
DATA EXCHANGE CONTROL	Inoperable on attempt to address device) – Malfunction – Control connected and no device – Power off	Busy or Inoperable	On attempted execution	At time detected	When operable	
	Inoperable (During execution of instruction) – Malfunction – Power.off	Mode Terminated Abnormally	During execution of instruction	At time detected	When operable	

DETECTION OF ABNORMAL I/O CONDITIONS (Cont'd)

DEVICE	DEVICE CONDITION	INTERRUPT INDICATOR SET	TIME OF INTERRUPT	INSTRUCTION TERMINATION	INDICATOR CLEARANCE	COMMENTS
DATA EXCHANGE CONTROL (Cont)	Parity Error – In receiving computer	Mode Terminated Abnormally	Upon completion of instruction	Upon completion of instruction	Next I/O instruction to device	
	Channel Request	External Interrupt	At the end of Normal Mode processing instr.		When Read and Write instructions terminate in both computers	
	Read A/B Equality before Write terminates	Mode Terminated Abnormally	Upon completion of Read instruction	At time detected	Next Read instruction to device	Write holds off
DATA DRUM MEMORY	Inoperable (On attempt to address device) – Malfunction – Control not connected – Power off	Busy or inoperable	On attempted execution of instruction	At time detected	When operable	
	Inoperable (During execution) – Head Address – Malfunction – Power Off – Echo Check	Mode Terminated Abnormally	During execution of instruction	At time detected	When operable	
	Operating (Busy) – Read, Write, Select	Busy or Inoperable	On attempted execution of instruction	At time detected	On next legitimate Read, Write or Select issued	
	Parity Error (Read) – Modulo 256 error	Mode Terminated Abnormally	During execution of instruction	Upon instruction termination	On next select issued	
	Programming Error – Invalid drum address – Improper instruction sequence	Mode Terminated Abnormally	On attempted execution of instruction	At time detected	On next legitimate Select	
	Programming Error – Exceeding system capacity	Mode Terminated Abnormally	During execution of instruction	At time detected	On next legitimate Select	

DETECTION OF ABNORMAL I/O CONDITIONS (Cont'd)

DEVICE	DEVICE CONDITION	INTERRUPT INDICATOR SET	TIME OF INTERRUPT	INSTRUCTION TERMINATION	INDICATOR CLEARANCE	COMMENTS
RANDOM ACCESS COMPUTER EQUIPMENT	Reading or Writing 1. Inoperable on attempt to address device – Address Verification on Select – Card Absent on Select – Malfunction – Power Failure	IR #11	On attempted execution	At time detected	Manual Reset by Operator	When addressing the unit with a Select instruction an 8-10ms indication will also be given
	2. Inoperable during Reading or Writing, or Echo Check during Writing	Mode Terminated Abnormally	During execution of instruction	At time detected	Manual Reset by Operator	
	3. No Block Select given before Read or Write	IR #11	On attempted execution	At time detected	Next Read or Write Select	
	4. Channel busy reading or writing or less than 50us since Block Select	IR #11	On attempted execution	At time detected		
	5. Card Released prior to Read/ Write due to 32 unserviced revolutions	ABN Term.	Upon termination of instruction	At time detected	When unconditional Card Removal command is given	
	6. Preamble Error	ABN Term.	During execution of instruction (Read or Write)	At time detected	Next Read or Write	Instruction is terminated immediately
	7. Parity Error during reading	ABN Term.	After instruction completion	Upon completion of instruction	Next Read or Write	
	8. Read-after-Write error during Writing	ABN Term.	Upon termination of instruction	At time detected	Next Read or Write	
	9. Block 255 exceeded during a Write or Read without A-B Equality	ABN. Term.	At termination of instruction	At time detected	Next Read or Write	
	Card Select 1. Inoperable before Card Select	IR #11	On attempted execution of instruction	At time detected	Manual Reset	
	2. Inoperable during execution of Card Select	IR #9	At time detected	No instruction being executed	Manual Reset	Unit goes inoperable at time of extract if Address Verification error on Card Select
	3. Card released due to exceeding 32 unserviced revolutions	None				When this Select is executed, the extraction will be held off until the "32 Rev" bit is cleared.

DETECTION OF ABNORMAL I/O CONDITIONS (Cont'd)

DEVICE	DEVICE CONDITION	INTERRUPT INDICATOR SET	TIME OF INTERRUPT	INSTRUCTION TERMINATION	INDICATOR CLEARANCE	COMMENTS
RANDOM ACCESS COMPUTER EQUIPMENT (Cont)	Card Select (Cont'd) 4. Channel Busy selecting. Channel is busy for 50us after termination of a Select instruction	IR #11	On attempted execution	At time detected		
	5. Address Verification error on Card selected	IR #11 Interrupt on attempt to execute Read or Write	On attempted execution of next instruction for that card	At time detected	Manual Reset	Card released to magazine
	5A. Address Verification error on Card preselected			At time detected	Manual Reset	Card not extracted
	6. Card Absent			At time detected	Manual Reset	Hdwe. will attempt a second Select
	7. Card Select not permissible	IR #11 B/I	On attempted execution	At time detected		
	8. Magazine Absent	IR #9 Off-line Complete	Not received until 50us after Select is terminated	Upon completion of instruction	Unconditional Card Removal	Removal Command must be given to set the 8-10ms indication to "1."
	Block Select 1. Inoperable before Block Select	IR #11 Busy/Inop.	On attempted execution	At time detected	Manual Reset	
	2. Inoperable during Block Select	IR #9	During execution	At time detected	Manual Reset	
	3. No Card on capstan	IR #11 Busy/Inop.	On attempted execution	At time detected	Next Read, Write or Select	
	4. Card released due to exceeding 32 unserviced revolutions	IR #11 Busy/Inop.	On attempted execution	At time detected	Next Read, Write or Select	32 Revolution Indicator clearance is by issuing an unconditional Card Removal. Block Select not permissible is set when this occurs.
	5. Channel Busy selecting (Busy 50us after select)	IR #11 Busy/Inop.	On attempted execution	At time detected		
	6. Block Select not permissible	IR #11 Busy/Inop.	On attempted execution	At time detected	Next Read or Write	

DETECTION OF ABNORMAL I/O CONDITIONS (Cont'd)

DEVICE	DEVICE CONDITION	INTERRUPT INDICATOR SET	TIME OF INTERRUPT	INSTRUCTION TERMINATION	INDICATOR CLEARANCE	COMMENTS
RANDOM ACCESS COMPUTER EQUIPMENT (Cont)	Miscellaneous Conditions 1. Card released due to 32 unserviced revolutions	IR #9 Off-line Complete	At time detected	No instruction in execution	When unconditional card removal command is given	A card will remain in preselect until 32 revolution bit is set to zero by unconditional card removal command
	2. Select Complete	IR #9 Off-line Complete	When 8-10ms from selected block		Indicator clearance for IR9 is upon honoring it	
	3. Inoperable and card is on capstan	IR #11 Busy/Inop.	On attempted execution of next instruction to device	At time detected	Manual Reset	If possible, the card will leave the capstan when the unit goes inoperable
	4. Read or Write executed with no card on capstan or on the way and no 32 Revolution indication					Read or Write with no card on capstan (and no 32 Rev. indicator) will result in a "Silent Death" condition - the instruction will stay staticized until a card reaches the capstan or the unit goes inoperable.
	5. Inoperable when no instruction is staticized while unit is in Remote.	IR #9	When unit goes inoperable	None	Manual Reset by Operator	
	6. Inoperable when no instruction is staticized while unit is in Local	No interrupt	None	None	Manual Reset by Operator	
	7. I/O Sense to a 3388 Channel that is non-existent or inoperable	IR #11 Busy/Inop.	On attempted execution of instruction	At time detected		This is the only condition that will result in a B/I interrupt when executing an I/O Sense instruction

XVI RCA 301 COMPATIBILITY

GENERAL DESCRIPTION

The RCA 3301 is designed to permit RCA 301 object programs to be run on an RCA 3301 System. This program compatibility is planned so that an RCA 301 user could immediately transfer his existing operations to the more powerful RCA 3301 System, without experiencing the normally inherent growing pains. In addition, this program compatibility is implemented to permit 3301 users to immediately avail themselves of the software previously developed for RCA 301 Systems.

Identical data representation exists on both systems. RCA 301 instructions are a subset of the RCA 3301 instruction repertoire. The following operation codes when programmed alike function identically on either of the systems:

Code	Instruction
A	Translate by Table
K	Locate Absence of Symbol Left
L	Locate Absence of Symbol Right
M	Transfer by Count Left
N	Transfer by Count Right
#	Transfer by Symbol Left
P	Transfer by Symbol Right
J	Symbol Fill Sector
.	Halt (when N character is a period)
Q	Logical Inclusive OR
T	Logical AND
U	Logical Exclusive OR
Y	Compare Data
X	Tally
R	Repeat

Minor incompatibilities, as later enumerated, occur upon execution of the following arithmetic instructions:

Operation Code	Instruction
+	Add Data
-	Subtract Data

Implementation of the RCA 3301 as a more powerful EDP System, especially in the Input/Output and Real-Time areas, dictated the achievement of program compatibility by a combined software-hardware approach. This is accomplished by:

1. 301 Compatibility Switch
2. 3301 Interrupt System
3. 301 Compatibility Program

When the 301 Compatibility Switch is set, under certain conditions, the 3301 Interrupt System automatically transfers control from the 301 object program to a program which handles the minor incompatibilities.

301 COMPATIBILITY SWITCH

An option of the Control Interrupt Logic instruction is used to condition the 3301 to operate in the 301 Compatibility Mode (20K) or (40K). When functioning in this mode, the procedure for adding or subtracting multi-character operands, with respect to the operands most significant digits, varies from the normal 3301 operations as follows:

ADD DATA - SUBTRACT DATA

When running in the 20K Mode, the execution of the Data Add or Data Subtract instructions will function as follows for multi-character operands:

1. Valid results will be produced in the MSD range 0 - 19.
2. No Overflow Interrupt will occur in the MSD range 0 - 19.
3. The Overflow Indicator will be set if the MSD result is in the range 10 - 19, but no Overflow Interrupt will occur.
4. The Overflow Indicator will be set and Overflow Interrupt will occur if the MSD result is over 19.
5. If an end-around-condition is produced from other than 4-character operands with zone bits in the MSD, no re-complementing will occur, the Overflow Indicator will not be set, and Overflow Interrupt will occur. When 4-character operands are present, the Compatibility program will re-complement the sum (or difference), set the PRI's correctly, and immediately return control to the 301 program.

When running in the 40K Mode, the execution of the Data Add or Data Subtract instructions will function as follows for multi-character operands:

1. Valid results will be produced in the MSD range 0-39.
2. No Overflow Interrupt will occur in the MSD range 0-39.
3. The Overflow Indicator will be set if the MSD result is in the range 10-39.
4. The Overflow Indicator will be set and Overflow Interrupt will occur if the MSD result is over 39.
5. If an end-around-condition is produced from other than 4-character operands with zone bits in the MSD, no re-complementing will occur, the Overflow Indicator will not be set, and Overflow Interrupt will occur. When 4-character operands are involved, the Compatibility program will re-complement the sum (or difference), set the PRI's correctly, and immediately return control to the 301 program.

For combinations of operands not mentioned above, the Overflow Indicator is not set and interrupt does not occur.

The PRI's are set to the sign of the result except when condition (5) occurs.

INPUT/OUTPUT INSTRUCTIONS

When the 301 Compatibility switch is set, the following OP Codes cause the instruction to terminate before execution, cause the 301 Compatibility Interrupt Indicator to be set, and cause interrupt to occur.

Operation Code	301 Instruction	Operation Code	Instruction
0	Card Read Normal	B	Print and Paper Advance Normal
1	Card Read Simo	C	Print and Paper Advance Simo
2	Card Punch Normal	D	T rack Select
3	Card Punch Simo	E	CMC or Band Select Record File Mode
4	Tape Read Forward Normal	F	Sector Read Disc Normal
5	Tape Read Forward Simo	G	Sector Read Disc Simo
6	Tape Read Reverse Normal	H	Sector Write Disc Normal
7	Tape Read Reverse Simo	I	Sector Write Disc Simo
8	Tape Write Normal	*	Record File Mode Read
9	Tape Write Simo	%	Record File Mode Write
;	Rewind to BTC, or Input/ Output Control	S	Input/Output Sense

When the 301 Compatibility switch is set, the following options cause the instruction to terminate before execution and set the 301 Compatibility Interrupt Indicator.

OP	N	Instruction Option
W	4	CTC, Simo 1 Indicator
W	8	CTC, Simo 2 EF/ED Indicator
W	-	CTC, Simo 1 EF/ED Indicator
V	2	Store A Register
V	4	Store B Register
V	8	Store S Register
⊡	Any character other than ⊡	Halt

301 ALTERATION SWITCH

The 301 Alteration switch permits a program to sense Breakpoint 4. This alteration permits branching to subroutines when this option is desired.

INTERRUPT SYSTEM

The 3301 Interrupt System enables the 301 Compatibility Program to gain control of the 301 object program when the 301 Compatibility Switch is set, and also when:

1. An Input/Output operation terminates.
2. A device is addressed and either the mode, control, or device referenced is busy or inoperable.
3. Operator intervention is requested via an interrupt from the Console Typewriter.
4. Upon attempted execution of a Programmed Interrupt (301 Halt) instruction.
5. Abnormal overflow condition.

301 COMPATIBILITY PROGRAM

The prime purpose of this program is to insure proper execution of the 301 Input/Output instructions. When a 301 I/O instruction is recognized, it is translated to the proper 3301 format, the correct device character assignment is made, and the instruction is executed. If the instruction specifies the Normal Mode of the 301, a programmed delay retains control in the Compatibility Program until the instruction has been executed. Regardless of the 301 mode specified, the proper registers, indicators, etc., are set as required by the 301 program upon instruction termination.

Other functions of the Compatibility Program are:

1. Type out an error message and halt if a compatibility interrupt is caused by any instruction for peripheral devices not accommodated by the Compatibility Program.
2. Handle error conditions, as later specified under individual device write-ups.
3. Type out a message and halt when a Programmed Interrupt (301 Halt) instruction is executed or when an abnormal overflow condition occurs.

4. Simulate 301 IOS instructions which includes:

   Assignment of the proper 3301 device character

   Performance of the tests indicated

   Return of control to the proper location in the 301 program in accordance with the results of the conditions tested.

301/3301 RESTRICTIONS AND INCOMPATIBILITIES

1. 301 instructions must be decade oriented, i.e., occupy high speed memory positions XXX0-XXX9. The only exception is the 301 Execute function which will be accommodated.

2. 301 Add or Subtract instructions function differently on the 3301 in that:

   Zone bits in any operand digit other than the LSD and MSD are ignored.

   If the numeric portion in any operand digit is invalid (not equal to 0-9), the instruction will be performed, an invalid result will be given, and no error condition will be indicated.

   The 2^4 bit in single character operands will be ignored. If the single character arithmetic results in a carry in the sum (or difference), the 2^4 bit is not set in the result, the Overflow Indicator is set, the Overflow Interrupt Indicator is set, and interrupt occurs. The Compatibility Program will insert the 2^4 bit and return control to the interrupted 301 program.

3. Model 305 (301 40K) Processor users cannot employ the CTC instruction to test for the presence of a second Overflow Indicator being set, with resultant instruction drop through.

4. 3301 buffered I/O Operations (Card Punch, Printer) are not completed until the device, not mode is free. RCA 301 programs dependent upon a mode-free test to insure proper error recovery or program timing may have to change those instructions to test device, not mode, for being busy.

5. 301 programs must not utilize memory wrap-around programming techniques, non-numeric tally quantities, or illogical operation codes; the latter may be executed as a logical operation on the 3301.

6. 301 programs which read into the 301 standard memory area (0000-0229) cannot be executed in the 3301.

7. 301 programs utilizing instructions written for the 301 High Speed Arithmetic Unit will not be accommodated.

8. 301 programs utilizing the following devices will not be accommodated:

   Data Recorder File, Model 361

   MICR Sorter Reader, Model B101

   Communications Mode Control, Model 378 series

   Data Disc File, Model 366

   Data Exchange Control, Model 377

Magnetic Tape Station, Model 729

Videoscan Document Reader, Model 5820

Random Access Computer Equipment, Model 3488

Programs encompassing the following RCA 301 Product line devices will be accommodated:

Card Reader, Models 323, 329-1 and 329-2, 330

Card Punch, Model 330, 334

Paper Tape Reader/Punch, Model 321

Paper Tape Reader, Model 322

Paper Tape Punch, Model 331

Magnetic Tape Stations, Models 381, 382, 581, 582, 3484, 3485

Monitor Printer, Model 338

On-Line Printer, Models 333, 335

Interrogating Typewriter, Model 328

3301 peripheral devices are not always identical to the 301 devices being accommodated. Compatibility problems resulting from these hardware variations and from Compatibility Program implementation are listed below, by I/O function. In addition to specifics cited, equipment inoperability or non-recoverable read or write errors will result in error printouts to the operator.

CARD READ

1. Non-diad-oriented card read instructions are accommodated.
2. 301 Card Release and Stacker Select options are ignored.
3. Binary Mode read instructions are not executed; an error printout will occur if attempted.

CARD PUNCH

1. Non-diad-oriented card punch instructions are accommodated.
2. The punching of other than an 80-character HSM image is handled.
3. The Punch Release and Stacker Selection options are ignored.
4. Binary Mode punch instructions are not executed; an error printout will occur if attempted.

PAPER TAPE READ

1. The 2^5 bit position of a character read from 5-channel paper tape will appear in HSM as a zero.
2. Repeated Tape Read Forward Normal instructions will be performed.

MAGNETIC TAPE READ OR WRITE

1. Read/Write rollback will be automatically performed.
2. Repeated Tape Read Forward normal instructions will be executed.
3. Erase and Backspace functions for the Model 3485 will not be accommodated.

INTERROGATING TYPEWRITER

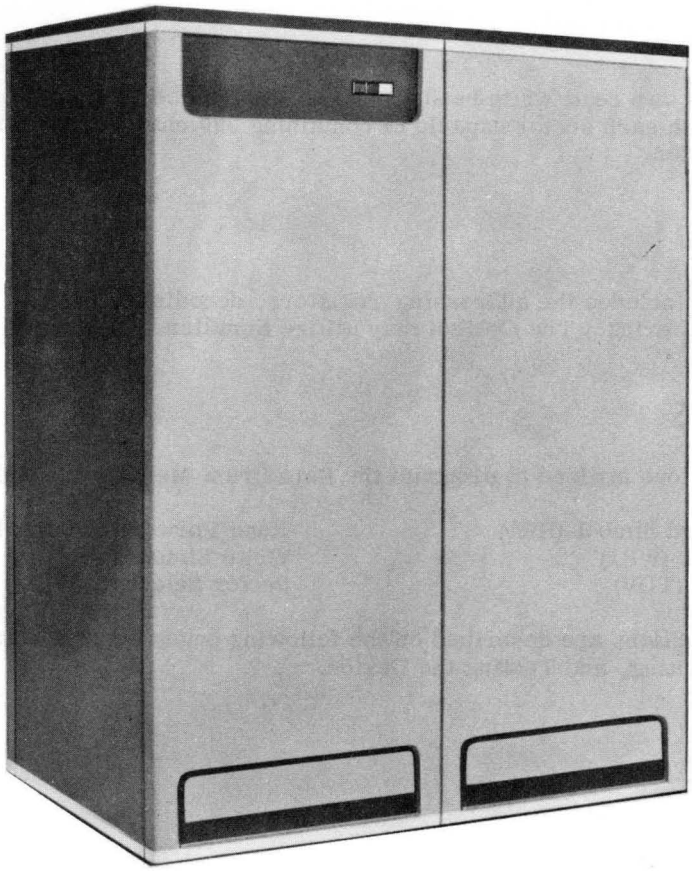
1. Only the 3301 Console Typewriter may be substituted for the 301 Interrogating Typewriter.
2. ED symbols will not cause a carriage return.
3. I/O Sense instructions for the Interrogating Typewriter will be ignored.

PRINTER

When two printers are being used, they must be of the same type; i.e., identical Model Numbers.

RANDOM ACCESS DEVICES

XVII RANDOM ACCESS DEVICES



Data Drum Memory - Model 3464

GENERAL DESCRIPTION

The Data Drum Memory, Model 3464, provides large capacity, high speed storage for data and computer programs. The Drum is available in six different storage capacities as follows:

Model 1 - 327,680 characters
Model 2 - 655,360 characters
Model 3 - 1,310,720 characters
Model 4 - 1,638,400 characters
Model 5 - 1,966,080 characters
Model 6 - 2,621,440 characters

The drum is attached to the processor thru a Control. The drum is approximately 10" in diameter and coated with a magnetic material. The drum contains from 128 to 1024 tracks,

each with its own read/write head, on which data can be read or written. Each track contains 8 sectors with each sector capable of containing 320 characters. Any amount of data may be read or written.

CONTROL

The Control includes the addressing registers, decoding circuitry, necessary control interface, and buffering. The Control may utilize Simultaneous Mode III.

INSTRUCTIONS

The instructions utilized to program the Data Drum Memory include:

Read Forward Simo 1 (RF1)	Read Forward Simo 2 (RF2)
Write Simo 1 (WR1)	Write Simo 2 (WR2)
Test Device (TDV)	Sector Select (SES)

These instructions are described on the following pages under the headings: Sector Selection, Reading, Writing, and Testing the Device.

GENERAL DESCRIPTION

The Sector Select (SES) instruction transfers the address of the track and sector to be accessed to the Control. This instruction must precede every Read and Write instruction. A Read or Write instruction may be executed anytime after the Control has received the track and sector address. This is signified by the termination of the SES instruction.

FORMAT

OPERATION - E
N - [
A ADDRESS - ZEROS (0000). Not to be used by programming
B ADDRESS - 0000 - 8191

The maximum address depends upon the number of tracks in the system. Address limits per the various capacities are as follows:

128 tracks	- 0000 to 1023
256	- 0000 to 2047
512	- 0000 to 4095
640	- 0000 to 5119
768	- 0000 to 6143
1024	- 0000 to 8191

OUTLINE OF OPERATION

The instruction causes the address to be transferred to the Control. The Control will then condition the control electronics to activate the proper read/write head and condition other electronics to accept the next Read or Write instruction.

FINAL SETTINGS

$(A)_f = (A)_i$
$(B)_f = (B)_i$

READING

GENERAL DESCRIPTION

The Read Forward Simo 1 (RF1) or Read Forward Simo 2 (RF2) instruction reads data from one or more sequential sectors to designated HSM locations. Any number of sequential characters may be read with one instruction with HSM size as the only restriction.

FORMAT

OPERATION - 4 (RF1) or 5 (RF2)
N - C
A ADDRESS - The even HSM address to receive the first character.
B ADDRESS - The HSM diad to receive the last two characters.

DIRECTION OF OPERATION

Characters are transferred to HSM left to right.

OUTLINE OF OPERATION

The contents of the sector designated by the previous SES instruction is transferred to a diad buffer in the Control and from there to the HSM location designated by the A Address. The S or C Register is incremented by two after each pair of characters is transferred. When the desired even number of characters has been read, the operation terminates. Any number of character locations may be included between the A and B Addresses. If the number of locations is not a multiple of 320, the remaining characters in the last sector accessed continue to be transferred to the control but not to HSM (see Accuracy Control). The Mode remains busy during this time.

FINAL SETTINGS

$(S)_f$ or $(C)_f$ = HSM location one to the right of the last character transferred.
$(T)_f$ or $(E)_f$ = $(B)_i$

GENERAL DESCRIPTION

The Write Simo 1 (WR1) or Write Simo 2 (WR2) instruction writes data from specified HSM locations to one or more sequential sectors. Any number of sectors may be written with HSM size as the only restriction.

FORMAT

OPERATION - 8 (WR1) or 9 (WR2)
N - C
A ADDRESS - The even HSM address of the first character to be written.
B ADDRESS - The HSM diad of the last two characters to be written.

DIRECTION OF OPERATION

Characters are transferred from HSM from left to right.

OUTLINE OF OPERATION

The HSM diad specified by the A Address is transferred to the Control and from there to the sector previously specified by the SES instruction. The S or C Register is incremented by two, and the next diad is then transferred. The instruction terminates on Address Equality. Any number of character locations may be included between the A and B Addresses but the Control will fill the rest of the final sector accessed with zeros $(0)_2$.

FINAL SETTINGS

$(S)_f$ or $(C)_f$ = HSM location one to the right of the last character written.
$(T)_f$ or $(E)_f$ = $(B)_i$

TESTING THE DEVICE

GENERAL DESCRIPTION

The Test Device (TDV) instruction tests the desired status of the Data Drum Memory and transfers control if the condition or conditions being tested are present.

FORMAT

OPERATION - S
N - [
A ADDRESS - Specifies the test to be performed as follows:

Character	Bit Position	Symbol	Test Function
A_0	$2^0 = 1$	1	Is the device inoperable?
A_0	$2^1 = 1$	2	Is the device busy?
A_0	$2^2 = 1$	4	Is there a programming error?
A_1	$2^0 = 1$	1	Is there a sector parity error?

- A_2 A_3 = Zeros (00)

B ADDRESS - HSM location of the next instruction to be executed if the condition(s) being tested is (are) present.

SPECIAL CONDITIONS

STP is performed if the condition(s) specified in the A Address is (are) present.

FINAL SETTINGS

$(A)_f = (A)_i$
$(B)_f = (B)_i$

TIMING

Access time consists of waiting for the drum to revolve to the point where data is to be read or written. Since the drum rotates at a speed of 3600 rpm (-3%), access, writing and reading rates are as follows:

Access (maximum)	- 17.2 ms
Access (average)	- 8.6 ms
Read/Write one sector	- 2.15 ms
Transfer rate	- 149 kc
HSM interrupt time	- approximately 1 out of every 8 memory cycles.

ACCURACY CONTROL

1. Parity is checked in all character transfers to the drum by the Control. If an error is detected, the Mode Terminated Abnormally Interrupt Indicator is set, and interrupt occurs immediately. The program sensible inoperable indicator is also set.

2. A modulo 256 count is kept on all "1" bits as they are written to each sector on the drum. This count is written following each sector and is checked against the count created during each Read operation. If the B Address of the Read instruction inhibits transfer of a complete sector to HSM, the Control must continue to access the sector so that this check may be performed. If the counts do not agree, the Mode Terminated Abnormally Interrupt Indicator is set, and interrupt occurs. The program sensible sector parity error indicator is also set.

3. A read/write head address character precedes each sector. This is checked against the requested address prior to each Read or Write operation. If this check fails, the Mode Terminated Abnormally Interrupt Indicator is set, and interrupt occurs immediately. The program sensible inoperable indicator is also set.

4. An echo check is performed on each character as it is written to the drum. If an error occurs, the Mode Terminated Abnormally Interrupt Indicator is set, and interrupt occurs immediately. The program sensible inoperable indicator is also set.

5. Programming errors are detected by the Control. These consist of:

   a) An invalid drum address
   b) Exceeding the drum system capacity during a Read or Write operation.
   c) Issuing a Read or Write operation with no Drum Select preceding it.

   These errors cause the Mode Terminated Abnormally Interrupt Indicator to be set, and interrupt to occur. The program sensible program error indicator is also set.

6. The Busy or Inoperable Interrupt Indicator is set, and interrupt occurs if A) the drum is inoperable prior to instruction execution or B) a Drum Select is issued while a Read or Write operation is in progress. The program sensible inoperable and busy indicators, respectively, are also set.

7. The Mode Terminated Abnormally Interrupt Indicator is set, and interrupt occurs if the drum goes inoperable during a Read or Write operation. The program sensible inoperable indicator is also set.

(To Be Supplied)

Random Access Computer Equipment - Model 3488

GENERAL DESCRIPTION

The Model 3488 Random Access Computer Equipment represents a mass storage device in excess of 5.4 billion characters on line to a 3301 processor.

Data is recorded on one side of 16-inch by 4-1/2-inch flexible magnetic cards.

These cards are housed in groups of 256; each group is called a magazine.

Up to 8 magazines are contained in a basic retrieval unit. Eight additional magazines can be added giving the device a maximum of 16 magazines (see figure XVII-1).

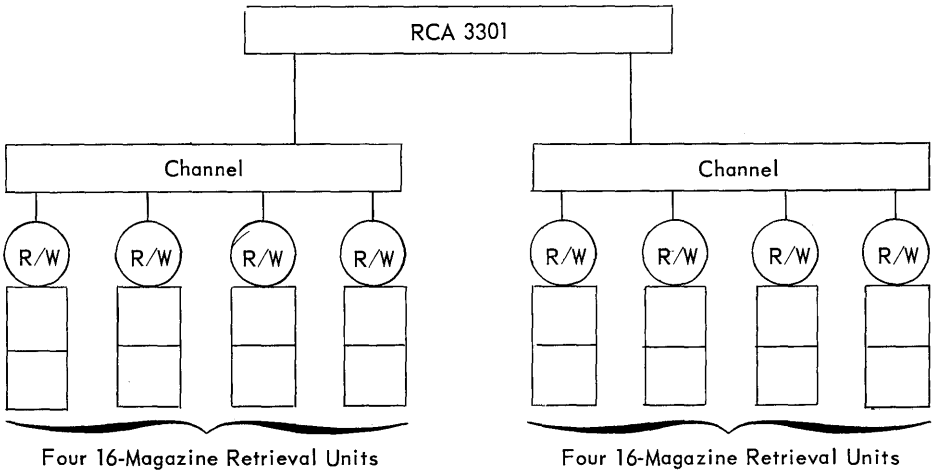


Figure XVII-1. System with Maximum 3488 Configuration (5.4 Billion Characters)

The magazines are removable and interchangeable, and they may be removed from one retrieval unit, inserted, and processed on other 3488 retrieval units.

A card which is program addressable is removed from its magazine by mechanical grips. Once the card enters onto the transport belts (see figure XVII-2) it moves towards the read/write heads located near a revolving drum (capstan) where data can be read or recorded.

A gate located at this point determines whether the card is to be returned to the magazine where it came from, or to remain at the recording station and be circulated under the read/write heads.

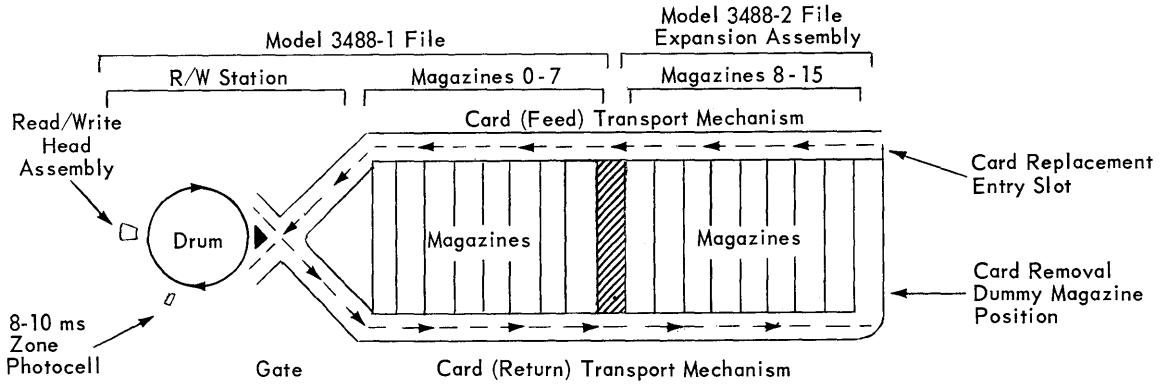


Figure XVII-2. 16-Magazine Retrieval Unit (681.6 Million Characters)

RETRIEVAL ASSEMBLY

Each eight-magazine Retrieval Assembly (3488-1) contains, in addition to the magazines, a card transport mechanism, card selection mechanism, read/write station, and all necessary internal addressing and timing logic. The Expansion Assembly (3488-2) can expand the capacity of the unit to 16 magazines. The Expansion Assembly contains a card transport mechanism and a card selection mechanism.

MAGAZINES

Each magazine contains two decks of 128 uniquely addressed cards. Each deck of cards is contained within a separately-addressable half of a magazine. Addressing is independent of the relative position of the cards within each half-magazine. This eliminates the need for a card to be returned to the exact same position within its deck; it is returned to the end of the deck in the half-magazine from which it was extracted.

CARD TRANSPORT MECHANISM

This Transport (Raceway) mechanism provides the means for physically moving the selected card to the read/write station (card feed) and returning the card to the magazine (card return). If the expansion assembly is added, the expansion assembly transport mechanism feeds into the primary card transport mechanism for movement to and from the read/write station.

CARD FORMAT

BANDS

Each 3488 card contains 128 tracks, each of which runs the full length of approximately 14.5 inches of recording area on the card. The 128 tracks are divided into 64 separately addressable bands of two tracks each. Characters are recorded bit-serial per track. Two tracks are recorded in parallel, each at a density of 700 bits per inch.

BLOCKS

Each band (two tracks) of recorded information is divided into four blocks of 650 seven-bit characters each.

The capacity of the 3488-1 along with the expansion assembly are included below.

Unit	No. of Seven Bit Characters
Block	650
Band (4 Blocks)	2,600
Card (64 Bands)	166,400
Magazine (256 cards)	42.6 million
Retrieval Assembly (8 magazines)	340.8 million
Retrieval Assembly Plus Expansion Assembly (16 magazines)	681.6 million

CONTROL

The Model 3388-4 channel acts as the interface between a 3301 Processor and up to four Model 3488 Random Access Units. Two Model 3388-4 Channels can be used in each 3301 System.

The channel permits one-way transfer of data between one of four random access units and the 3301 processor.

The channel enables selection and reading/recording of magnetic cards contained in a random access unit, under program control. Character parity checking and character buffering are performed in the channel.

The Control includes the addressing registers, decoding circuitry, necessary control interface, and buffering. The Control may utilize simultaneous Mode III.

ADDRESSING

Addressing is a function of the retrieval unit, which contains the required registers as follows:

1. A full register for selection
2. A full register for preselection
3. A magazine address register used to return a card to its associated magazine.

These registers permit overlapping of the selection, preselection, and return of cards.

INSTRUCTIONS

The following instructions are utilized to program the Random Access device:

Select (SES)
Read Forward Simo 1 (RF1)
Read Forward Simo 2 (RF2)
Write Simo 1 (WR1)
Write Simo 2 (WR2)
Test Device (TDV)

These instructions are described on the following pages under the headings:

Select, Reading, Writing, and Testing the Device.

GENERAL DESCRIPTION

The Select (SES) instruction transfers the address of the device, option desired, and card/block number through the Channel to the specified unit. This instruction must precede every Read or Write instruction.

FORMAT

OPERATION - E

N - specifies device number as follows:

$(60)_8$ to $(63)_8$ on First Channel

$(64)_8$ to $(67)_8$ on Second Channel

A ADDRESS - specifies the option to be performed as follows:

Character	Bit Position	Symbol	Option
A_0, A_1			Zeros (00)
A_2	$2^0 = 0$	0	Conditional Card Removal Remove card from the capstan after next Read or Write.
A_2	$2^0 = 1$	1	Leave card on capstan after next Read or Write.
A_2	$2^1 = 1$	2	Unconditional Card Removal Remove card presently on capstan regardless of error condition. This bit overrides all other bits and is independent of Block and Card Select permissible condition. Address is ignored when this option is specified. (The only indicator reset under this condition will be Illegal Operation.)
A_2	$2^2 = 1$	4	Terminate Read presently in progress. (Address is ignored.)
A_2	$2^3 = 0$		Card Select
A_2	$2^3 = 1$	8	Perform Block Selection of the card on the capstan.
A_3	2^0, 2^1, 2^2, 2^3 2^4 2^5		Magazine number (1-16) (binary) Zero (0) Zero (0)

B ADDRESS - specifies the following information:

Characters	Description
B_0, B_1	Four bits of both B_0 and B_1 (2^0 to 2^3) are used to designate the card number. (Total of eight bits for 256 cards.) This address should be considered a continuous eight-bit binary number, of which the least significant four bits are in B_1 and the most significant four bits are in B_0.
B_2, B_3	Four bits of both B_2 and B_3 (2^0 to 2^3) are used to designate block number. (Total of eight bits for 256 blocks.) The address should be considered a continuous eight-bit binary number, of which the least significant four bits are in B_3 and the most significant four bits are in B_2.

OUTLINE OF OPERATION

Card and Block Selects should only be issued when the device will accept them. If the device cannot accept the Select, an Illegal Operation occurs causing the termination of the Select instruction and a Busy/Inoperable interrupt.

A Block Select with no card on the capstan sets the "Illegal Operation" sense bit and a Busy/Inoperable interrupt.

A Select instruction keeps the Channel busy for 50us after the actual termination of the instruction.

If a read is in progress, when an Unconditional Card Removal (UCR) is specified, the read is immediately terminated, and the card is removed. If a write is in progress, the specified Unconditional Card Removal is ignored.

FINAL SETTINGS

$(A)_f = (A)_i$

$(B)_f = (B)_i$

GENERAL DESCRIPTION

The Read Forward Simo 1 (RF1) or Read Forward Simo 2 (RF2) instruction reads data from the device (starting at the block previously selected by the SES instruction) to the designated HSM locations. Any number of consecutive characters may be read with one instruction with HSM size as the only restriction. Transfer of information ends after the last character of block 255 is read or when the specified HSM area is filled, whichever occurs first.

FORMAT

OPERATION - 4 (RF1), or 5 (RF2)

N - specifies device number

$(60)_8$ to $(63)_8$ on First Channel

$(64)_8$ to $(67)_8$ on Second Channel

A ADDRESS - The even HSM address to receive the first character.

B ADDRESS - The HSM diad to receive the last two characters, odd or even address.

DIRECTION OF OPERATION

Characters are transferred to HSM left to right.

OUTLINE OF OPERATION

If all conditions are acceptable, the Read begins when the beginning of the proper block has been reached. The block address register in the device is incremented with each block read.

If A-B Equality is not reached by the completion of reading the last block on the band, the block is incremented by one and, if required, the heads are repositioned. When this occurs, the Channel does not terminate the instruction. The Read continues when the first character of the next block is read. Reads are automatically terminated after block 255. Reading of a complete block is not necessary. A-B Equality can be used to terminate the Read whenever desired.

A Read instruction can be issued anytime after executing a Card Select, or after a legitimate Block Select. The Mode is held up until the instruction is executed.

FINAL SETTINGS

$(S)_f$, $(C)_f$ = HSM location one to the right of the last character transferred.

$(T)_f$, $(E)_f$ = $(B)_i$

GENERAL DESCRIPTION

The Write Simo 1 (WR1) or Write Simo 2 (WR2) instruction writes data from the designated HSM locations to the device (starting at the block previously selected by the SES instruction). Any number of consecutive characters may be written with one instruction with HSM size as the only restriction. Transfer of information ends after the last character of block 255 is written or when the specified HSM area is written, whichever occurs first. When A-B Equality terminates the Write before the end of a block, the remainder of the block is filled with spaces.

FORMAT

OPERATION - 8

N - specifies Device Number

$(60)_8$ to $(63)_8$ on First Channel

$(64)_8$ to $(67)_8$ on Second Channel

A ADDRESS - The even HSM address of the first character to be written.

B ADDRESS - The HSM diad of the last two characters to be written, odd or even address.

DIRECTION OF OPERATION

Characters are transferred from HSM from left to right.

OUTLINE OF OPERATION

If all conditions are acceptable, the Write begins when the beginning of the proper block has been reached. The Write terminates on A-B Equality if it coincides with the end of a block, or at the end of a block in which A-B Equality occurs (filling the block with space characters), or when the end of block 255 is reached.

If A-B Equality is not reached by the completion of recording the last block on the band, the block address is incremented by one and, if required, the heads are repositioned. When this occurs, the Channel does not terminate the instruction. The Write continues when the next block is in position.

FINAL SETTINGS

$(S)_f$, $(C)_f$ = HSM location one to the right of the last character transferred.

$(T)_f$, $(E)_f$ = $(B)_i$

GENERAL DESCRIPTION

The Test Device (TDV) instruction tests the desired status of the device and transfers control if the condition or conditions being tested are present.

FORMAT

OPERATION - S

N - specifies Device Number

$(60)_8$ to $(63)_8$ on First Channel

$(64)_8$ to $(67)_8$ on Second Channel

A ADDRESS - A_0 specifies the tests to be performed as follows:

OPTION 0		
Bit Position	Symbol	Test Functions
$2^0 = 1$	1	Test for Card Select or Preselect Not Permissible.
$2^1 = 1$	2	Test for Channel Busy Reading, Writing, or Processing a Select instruction.
$2^2 = 1$	4	Test for Read or Write Busy (by device).
$2^3 = 1$	8	Test for Block Select Not Permissible.
$2^4 = 1$	&	Test for specified block not within 8-10 ms. from heads.
$2^5 = 0$	-	Not to be used.

OPTION 1		
Bit Position	Symbol	Test Function
$2^0 = 1$	1	Test for parity error, Read-after-Write error, or preamble error (Data Error).
$2^1 = 1$	2	Test for inoperability (includes device inoperable, address verification error, or card absent error)
$2^2 = 1$	4	Test for Card Released due to exceeding 32 unserved revolutions.
$2^3 = 1$	8	Test for Illegal Operation or Magazine Absent.
$2^4 = 1$	&	Test for Block 255 exceeded without A-B equality.
$2^5 = 0$	-	Not to be used.

OPTION 2		
Bit Position	Symbol	Test Function
$2^0 = 1$	1	Test for Block not 6-8ms. from heads.
$2^1 = 1$	2	Test for single bit correction error.
$2^2 = 1$	4	Test for Card Extract count equals limit (set only once).
$2^3 = 1$	8	Test for Card Extract count exceeds limit (set each time card is placed on capstan after count has been exceeded).
$2^4 = 0$ $2^5 = 0$	–	Not to be used.

$-A_1$ = 0 (Not to be used)

$-A_2$ = Specifies Sense Option

= 0 (Option 0)

= 1 (Option 1)

= 2 (Option 2)

$-A_3$ = 0 (Not to be used)

B ADDRESS - HSM location of the next instruction to be executed if the condition(s) being tested is present.

OUTLINE OF OPERATION

The Block Select Not Permissible bit is set by a Select instruction and reset by a Read or Write instruction. If the card is on the capstan when a Read or Write is terminated, Block Select is permissible provided that the card has not been directed to leave the capstan. If a card is not on the capstan but on its return, Block Select is not permissible.

Completion of a card or block selection resets the 8-10ms bit to zero, and it remains reset until a Read or Write is executed.

The Illegal Operation indication is reset by any subsequent instruction to the device, including the Unconditional Card Removal.

The 2^0 bit of Option 2 is reset to zero each time the specified block is within 8-10 ms. from the heads, and then set to one after 6-8 ms.

General Reset automatically resets the following indications, providing all cards are at rest in their magazines:

1. Card Select not permissible.
2. Block Select not permissible.
3. Specified Block not within 8-10 ms.
4. Card Released due to 32 revolutions.
5. Illegal Operation.

General Reset does not reset data error. If General Reset is pressed before all cards are at rest, the device becomes inoperable.

SPECIAL CONDITIONS

STP is performed if the condition(s) specified in the A Address is present.

FINAL SETTINGS

$(A)_f = (A)_i$

$(B)_f = (B)_i$

TIMING

The read/write head assembly, which contains eight pairs of heads (one Read, one Write head for each pair), can be moved to one of sixteen positions. Once positioned, the head assembly is capable of reading or writing to one of four bands, each band containing four blocks.

CARD SELECT TIMING

The Card Select time (308ms nominal, 290ms minimum, 325ms maximum) is the time required to select a specific card from a magazine and place it into position to be extracted onto the raceway. If at this point of time the card can be placed on the capstan, it will be immediately extracted. Approximately 75ms nominal (67-82ms) are required to clear a card from the Pre-select position through the pinch rollers that place it on the raceway. At this point, another card select is permissible. (C)

Timings (all times in milliseconds and are nominal.)

	Position*	Card Select	Card Feed	Card Return	Reload
3488-1	0A	308	136	170	77
	0B/1A		145	182	
	1B/2A		156	196	
	2B/3A		172	209	
	3B/4A		185	222	
	4B/5A		198	235	
	5B/6A		211	248	
	6B/7A		225	262	
	7B		235	275	
3488-2	8A		275	327	
	8B/9A		288	341	
	9B/10A		302	355	
	10B/11A		313	369	
	11B/12A		324	383	
	12B/13A		335	397	
	13B/14A		346	411	
	14B/15A		357	425	
	15B		368	441	

(C)

*where A = 1st half of magazine and
B = 2nd half of magazine

CARD FEED TIME

Card Feed Time is the time required to move a card from the select position until the first block is under the read/write heads.

CARD RETURN TIME

Card Return Time begins when the leading edge of the card passes under the read/write heads.

CARD RELOAD TIME

Card Reload Time is a nominal time required for the card to be reloaded into the designated magazine.

DRUM REVOLUTION TIME

Ⓒ Drum Revolution Time is 58.2ms (38.2ms to pass the card and 20ms for gap time). Each block of 650 characters requires approximately 8ms, and the interblock gap is approximately 1ms.

BLOCK SELECT TIMING

Under nominal operating conditions, it is possible to read or write to the next consecutive block as long as read/write head assembly movement is not required and the Block Select and Ⓒ Read/Write commands are issued no more than 100 μs after the end of the preceding block. It is also possible to issue a no head movement Block Select within the card gap time and be able to Read or Write block 1.

When a Block Select requires that the head be moved anywhere within positions 0 to 7 or anywhere within positions 8 to 15, then 20ms is required to move the head. When movement is made that crosses over these boundaries (i.e., 7 to 8, 0 to 15, 8 to 7, etc.), then 34ms is required to move the head.

ACCURACY CONTROL

ADDRESS VERIFICATION AND CARD ABSENT CHECKING

To determine that the proper half magazine has been selected, a bail sensor micro-switch is activated. This identification of the selected half-magazine is compared with the requested address (Select instruction). To determine that the proper card has been selected, a set of photocells are located on the track in position for reading the binary coded selection notches on the top of the card. This reading is compared with the requested address (Select instruction) before the card is placed on the capstan.

A head position sensor is mounted on the head assembly. A reading from the sensor is compared with the register specifying the requested head position to insure proper head positioning. A constant check is made for proper head positioning while reading or writing. A format notch is used to select the proper block.

An echo check is made while recording to assure that current is flowing through the selected head. Failure of this check is considered an Address Verification error.

A check is made to ascertain that the returning card returns to the magazine that was originally selected.

Both Address Verification and Card Absent error conditions can cause device inoperability.

When the Address Verification error occurs on a card that has been extracted, the device becomes inoperable immediately, and the card is returned to its magazine after one revolution on the capstan. When the Address Verification error occurs on a card that is being selected, the device becomes inoperable at the time the card extract would be attempted. The card is not extracted.

When a Card Absent error occurs (First attempt) normal operation of the unit is allowed until the transport is cleared. Once all the cards are in their magazines, the hardware makes a second attempt to select the card. If the Card Absent indication is received after this attempt, the unit becomes inoperable and the "Inoperable" sense bit is set (See Abnormal Terminations, Chapter XV).

If an attempt is made to select a card from a magazine position that does not contain a magazine, an Illegal Operation indication is given. The fact that a magazine is not present is sensed by a switch located in each magazine position.

AUTOMATIC REMOVAL OF UNSERVICED CARDS

Whenever a card remains unserviced for over 32 revolutions of the capstan, the card is automatically removed, returned to its magazine. The Off-line Operation Complete Interrupt Indicator is set.

READ AND WRITE CHECKING

A Read-after-Write parity check and missing bit check is automatically made as each block is written. Failure of this check causes termination of the Write, and an indication is given.

While reading, each character read is checked for proper parity. Any single bit error in a specific character is automatically corrected before being sent to HSM. If a parity error occurs that cannot be automatically corrected, an $(17)_8$ is transferred to HSM, a parity error indication is set, and the remainder of the information in the block is transferred but may not be valid. If more than one block is being read, information transfer resumes at the beginning of the next block.

ADDRESS DATA CHECKING

Address data is parity checked. When bad parity is detected, the unit automatically becomes inoperable.

PREAMBLE CHECKING

A synchronizing preamble is recorded in front of each block written. At the beginning of a Read and Read-after-Write, this preamble is used to synchronize the operation. If synchronization is not accomplished, a preamble error is indicated.

INTERLOCKS

As soon as the first card is fully extracted, a preselect of a second card can be executed. The second card is not extracted until the first card leaves the capstan. If the card returning is in the raceway (in position to be reloaded into the magazine), the reload is delayed until the extract is completed. If the reload has been started, the extraction is delayed until the reload is completed.

If a card is in the return cycle, and there is a card on the capstan and a preselect is attempted, the preselect command is accepted but not executed until the reload of the card in the return cycle is completed.

If there is a card in the return cycle that has not reached the reload point, and a card is not on the capstan, a card may be selected and extracted immediately, while the card on the return path is delayed in its reload operation. At no time will there be more than two cards in motion.

CARD EXTRACT COUNTER

The Card Extract Counter is mechanized by recording a 15-bit binary number in a special track on the card. During normal operations, the count is read, decremented by one, and rewritten. A check is made to indicate when the count reaches zero. When the count reaches zero, a special (equal) bit is recorded. On the next extraction, the system recognizes the equal bit and records an overflow bit. On all subsequent extractions, overflow is reported and no writing takes place.

These indications can be sensed by use of the Standard-301/3301 Sense instruction, as follows:

Option 2 - $2^2 = 1$ - Test for count equals limit.

$2^3 = 1$ - Test for count has exceeded limit. (This bit is set each time a card is placed on capstan after the count has been exceeded.)

Five toggle switches are used to set up the amount to be prewritten on the card. These switches are located on the rear of the maintenance control panel.

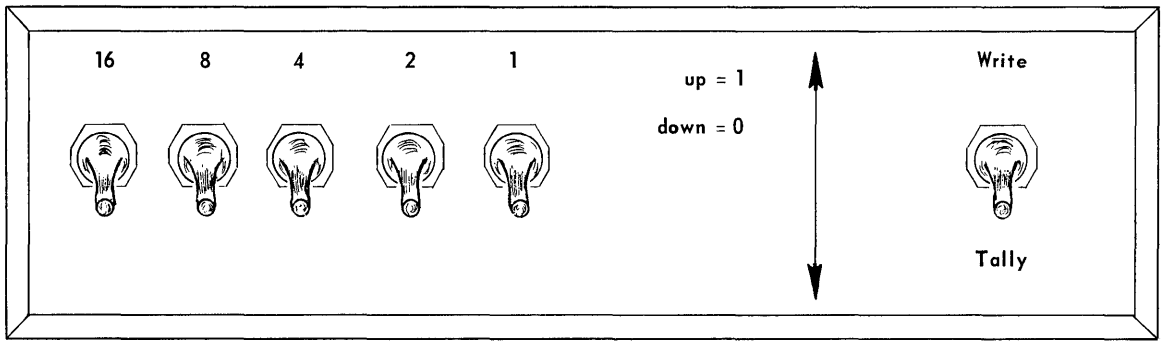
When the Write-Tally switch is in the Write position, every card extracted is prewritten. When the Write-Tally switch is in the Tally position and the device is in "Remote", normal countdown will be performed.

The Tally quantity is always recorded with the 10 least significant bits all 0's. The five high-order bits are recorded in accordance with the switch setting; therefore, the number is 1,024 times N, where N is the number from 0-31, set into the five binary switches. The maximum number that can be recorded is 31 x 1,024, or 31,744.

CARD EXTRACT COUNTER (Cont'd)

All Tally operations occur before the card reaches the Read/Write head on the first pass of the card; therefore, a card circulating on the capstan cannot be initialized by setting the Write-Tally switch to Write; the switch must be set before the card reaches the capstan.

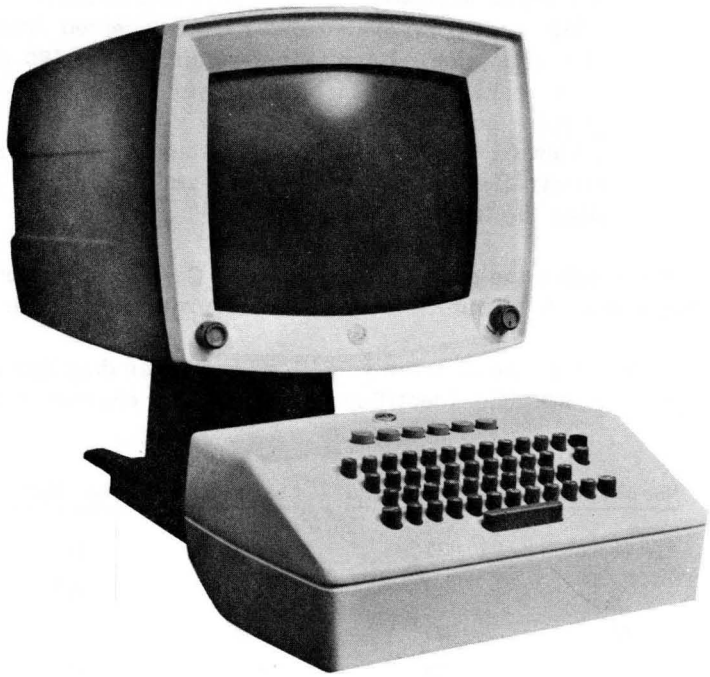
The Controlling switches are as follows:



Note: When the Write-Tally switch is in the Write position, it will cause the amount specified to be written on the card while in either the Local or Remote Mode. Care must be exercised when using this feature in the Remote Mode to avoid overwriting a valid existing Tally count.

VIDEO
DATA
SYSTEMS

XVIII VIDEO DATA SYSTEMS



VIDEO DATA TERMINAL — MODEL 6050

GENERAL DESCRIPTION

The Video Data Terminal (VT), Model 6050, is a remote terminal device which permits long distance communication between a VT operator and the 3301. Inquiries and transactions may be composed, visually verified and, if necessary, corrected before transmission. The response from the 3301 will be displayed and may be retained as long as it is required. The operator of the Video Data Terminal controls all functions by use of a control panel and keyboard.

The VT is available in six models:

Model 6050-11; 12; 13: These models interface the Bell System 202D Data Set on private line telephone circuits or 202C Data Set on the message network. These VT's communicate with the 3301 via the Model 6010 Communication Buffer in a half-duplex mode. Transmission rates are either 120 or 180 cps.

Model 6050-21; 22; 23: These models interface the Bell System 103F Data Set on private line telephone circuits or 103A Data Set on the message network. There is no provision for automatic calling on switched networks or for unattended operation. These VT's communicate with the 3301 via the Model 6020 Communication Buffer in a half-duplex mode at a transmission rate of 10 cps.

All models operate with the American Standard Code for Information Interchange (ASCII). The 6050-11,-12,-13 transmit a character containing 10 bits, 1 start bit, 8 information bits (including one parity bit) and 1 stop bit. The 6050-21,-22,-23 transmit an 11-bit character that has 2 stop bits. The 2^0 bit is transmitted first in both models. A movable cursor (displayed

as an underscore) provides the operator with a continuous indication of the position in which the next character will be entered on the viewer. An associated control panel at each terminal contains a conventional 4-row keyboard, control keys and indicators. A display memory device provides storage for locally generated data, data received from the communication line, timing, and control information. Its maximum capacity is 480 displayable character positions. A maximum of 64 characters can be displayed on the face of the 14 inch video screen. A character generator converts the digital data received from the display memory into video signals for the viewer. A line adapter interfaces the display memory and the data set by converting the bit-parallel characters into bit serial format, adding the character framing bits, and regulating the transmission rate.

The Model 6050 VT's require the use of the Model 6042 Code Translator which translates the ASCII line code to a pseudo 6-bit information code and provides Escape character facilities.

The following model numbers indicate the variations in viewer displays as to character array, size, and spacing. The specific identifications as to the character arrangements are as follows:

Model	No. of Lines	Chars. per Line	Char. Height	Char. Width	Spacing Vert.	Spacing Horiz.
6050-11	15	32	.22"	.18"	.40"	.25"
6050-12	10	48	.15"	.12"	.40"	.17"
6050-13	12	40	.18"	.14"	.40"	.20"
6050-21	15	32	.22"	.18"	.40"	.25"
6050-22	10	48	.15"	.12"	.40"	.17"
6050-23	12	40	.18"	.14"	.40"	.20"

OPERATION

Pressing the WRITE switch places the VT in the Write Mode. The cursor is positioned to the upper left hand corner of the viewer and data is permitted to be written to display memory. (The switch remains illuminated and data is permitted to be entered until the TRANSMIT switch is pressed. Pressing the WRITE switch does not affect display memory). The desired data is entered through the keyboard. As each character is entered, it is written to display memory, displayed upon the viewer, and the cursor advances to the next character position. When the end of a line is reached, the cursor automatically advances to the first position of the next line. If it is desired to advance the cursor to the first position of the next line before reaching the end of a line, the operator may press the RETURN key on the keyboard or the RETURN switch on the control panel. The first operation transfers a RET control character to the display memory while the latter only positions the cursor. After the complete message has been entered, a DD2 (end of transmitted message character) is entered by the operator and the complete message may be visually verified.

When the message is ready to be transmitted and the line connection has been established, the TRANSMIT switch light is pressed. A DD1 is automatically generated and transmitted, followed by the message transmission. The transmission of the DD2 causes the TRANSMIT switch light to be extinguished. The message does not appear on the viewer while transmission is in progress. When transmission is completed the message reappears. If no response is received in a reasonable time, transmission is repeated by again pressing the TRANSMIT switch light.

NULL characters (0000000) which occupy positions in display memory where no data appears, are not transmitted. NULL characters preceding a RETURN character in a line or present in

a line in which no RETURN character appears, are converted to SPACE characters, which are transmitted. NULL characters following a RETURN character in a line are ignored.

Following transmission of a DD2, the VT is switched to the RECEIVE mode and the cursor returned to the beginning of the frame. If no response is received within a reasonable time, the WRITE mode may be activated, and the message retransmitted by pressing the TRANSMIT switch light after making any desired changes.

Receipt of a RETURN character from the processor causes the cursor to move to the first character position of the next line where the next displayable character will appear. The RETURN character will be stored in display memory but will not be displayed.

The arrival of input data begins with an SOM (start of message character). This erases the display memory and returns the cursor to the beginning of the viewer. In the 6050-11 Series each character is stored in display memory, and, when the complete message is received, displayed upon the viewer. When utilizing the 6050-21 Series the characters are displayed immediately as they are received. The receipt of a DD1 (end of received message character) inhibits further input from the line until a DD2 is again transmitted. The receipt of the DD1 does not affect display memory or terminate the transmission line connection.

Display memory may be erased, and the viewer image erased, by pressing the ERASE switch. The RESET switch causes the cursor to be returned to the beginning of the frame. ADVANCE and BACKSPACE keys are available for formatting purposes, and the latter can be used to correct errors. Pressing the ADVANCE key moves the cursor one character position to the right. If the cursor is at the last position in the line, it will move to the first position of the next line. From the last position in the viewer, it will move to the first position in the viewer (upper left hand corner). Pressing the BACKSPACE key will move the cursor one character position to the left. From the first position in the line, it will disappear from the viewer. If depressed again, the cursor will reappear at the last position of the preceding line. From the first position of the viewer the BACKSPACE key must be depressed 4 times to make it appear at the last position of the viewer. The depression of either key does not affect the display memory.

If it is desired to retransmit all or portions of the received message back to the processor, pressing the WRITE switch returns the cursor to the beginning of the frame without changing the contents of display memory. The received data may be edited and additional information entered through the proper operation of the keyboard and cursor controls. The new message can then be transmitted as previously described.

Note: DD1 and DD2 are selectable for each installation, but must be identical to those utilized by the 3301 processor.

The following ASCII graphic characters are not displayed upon the viewer:

[- used as the SOM character.

\ - reserved as the ESCAPE character which is used for the VT. (See Code Translator, Model 6042)

The ASCII control character CR is used as the RETURN character.

ACCURACY CONTROL

All data is checked for even parity as it is read from the display memory. A parity error causes the character generator to produce a brightened area, equivalent to one character space, on the viewer in the position of the errored character.

ASCII control characters other than CR are displayed as blanks and should not be present.

Transmission does not commence when the TRANSMIT switch is pressed unless a DD2 has been previously entered.

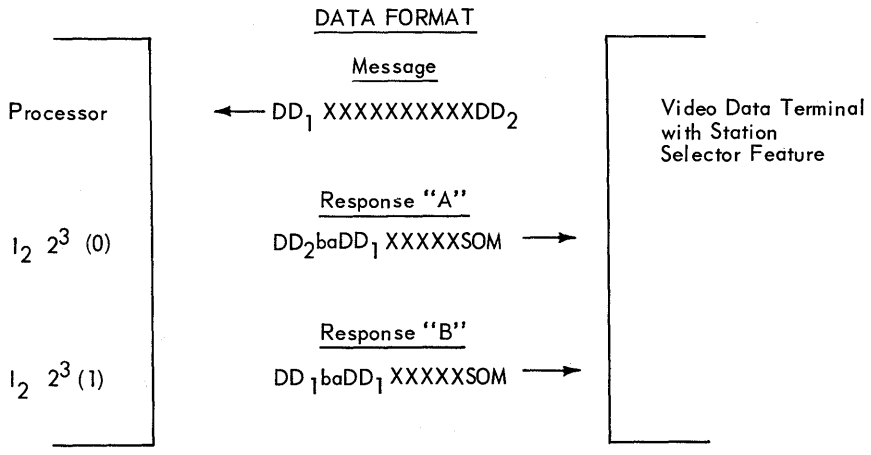
STATION SELECTOR FEATURE

This feature permits the 6050-11,-12,-13 models to be used on multi-station private line circuits where the processor controls all transmissions via the sequential polling of each remote VT.

The processor invites messages from each of the VT's by sending a two character Transmit Start Code (TSC) to the circuit.

The TSC characters are selected from the 32 ASCII characters which have b_7 and $b_6 = 1$. The VT operates in the normal manner except that when the operator presses the TRANSMIT switch, the message is not sent to the processor until that particular VT is selected in the polling cycle.

In 301 and 3301 systems, a DD1 or DD2 character follows the TSC. This TSC can be transmitted along, followed by DD1 or DD2, or it can be added to the processor's response to a service request from a remote VT. In this instance, the processor delivers the request information to a VT which was previously polled and required service. By adding the TSC to the response, the processor polls the next VT in sequence as it delivers the required information to the first device.



Valid Codes – Video Data Terminal

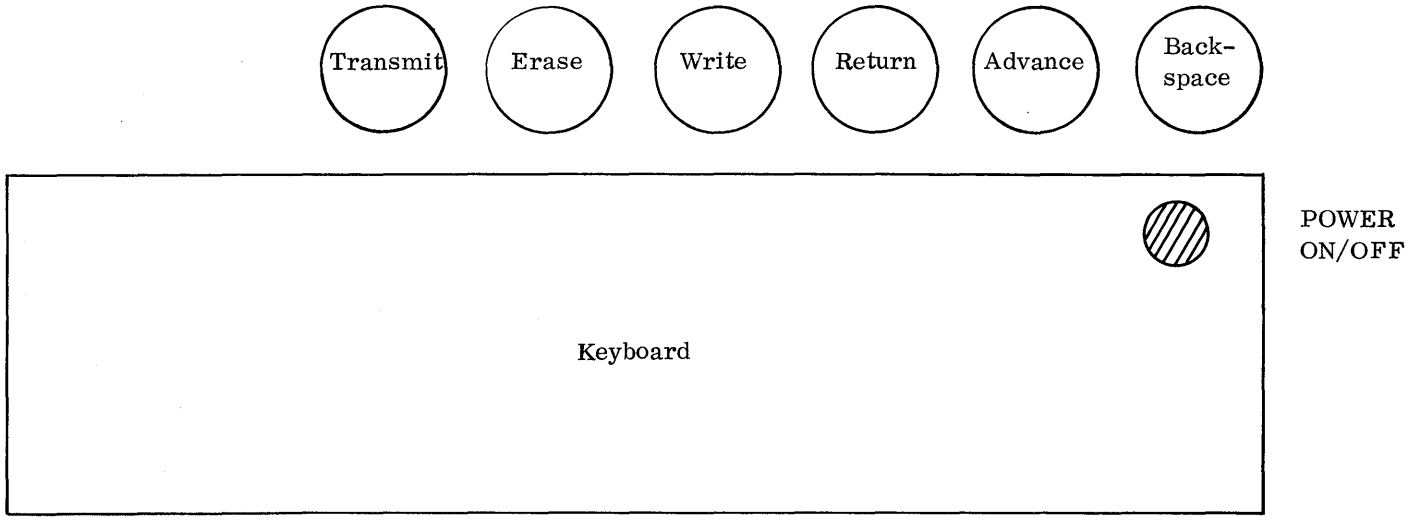
Model 6050-11, 12, 13, 21, 22, 23

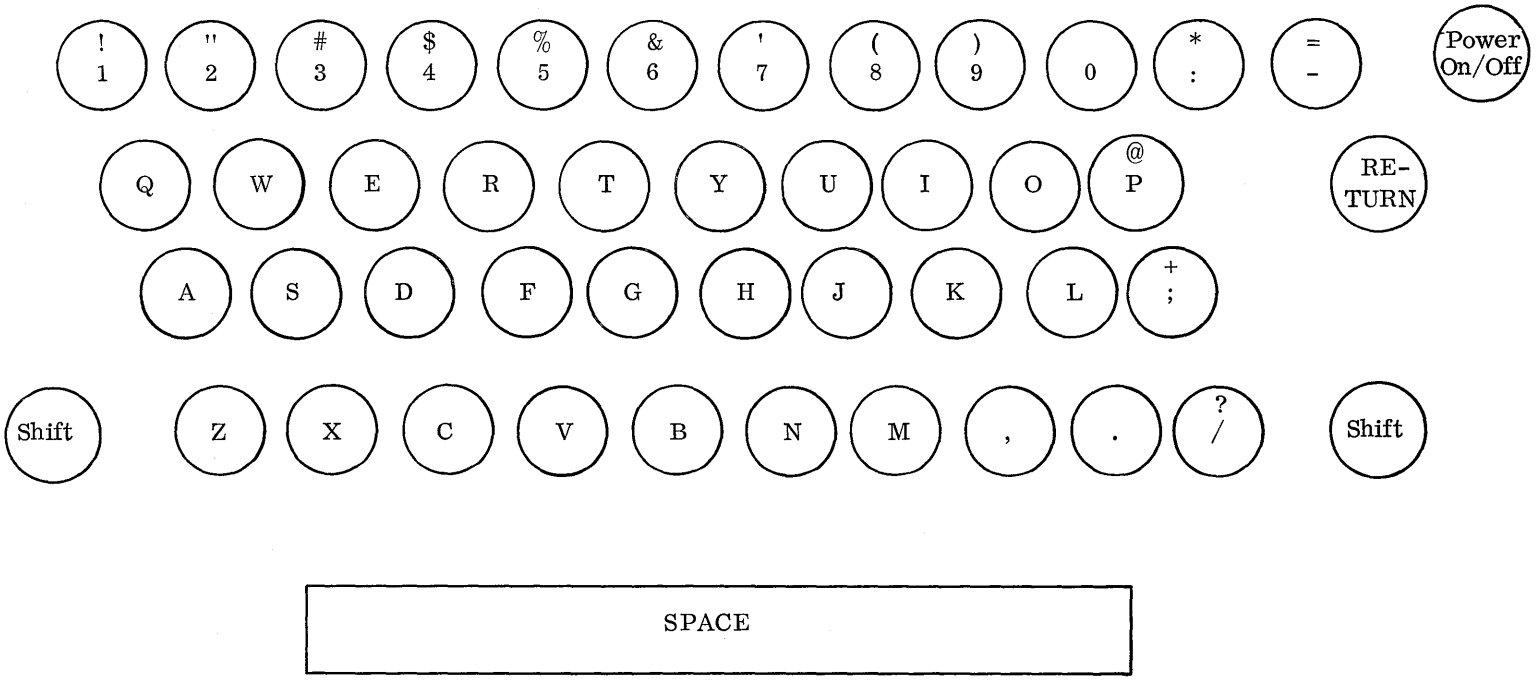
ASCII Code b7 b1	ASCII Graphic Symbol	VT Displayed Symbol	ASCII Code b7 b1	ASCII Graphic Symbol	VT Displayed Symbol
0001101	Return	Note 3			
0100000	space	.	1000000	@	@
0100001	!	!	1000001	A	A
0100010	"	"	1000010	B	B
0100011	#	#	1000011	C	C
0100100	$	$	1000100	D	D
0100101	%	%	1000101	E	E
0100110	&	&	1000110	F	F
0100111	'	'	1000111	G	G
0101000	(	(	1001000	H	H
0101001	)	)	1001001	I	I
0101010	*	*	1001010	J	J
0191011	+	+	1001011	K	K
0101100	,	,	1001100	L	L
0101101	-	-	1001101	M	M
0101110	.	.	1001110	N	N
0101111	/	/	1001111	O	O
0110000	0	0	1010000	P	P
0110001	1	1	1010001	Q	Q
0110010	2	2	1010010	R	R
0110011	3	3	1010011	S	S
0110100	4	4	1010100	T	T
0110101	5	5	1010101	U	U
0110110	6	6	1010110	V	V
0110111	7	7	1010111	W	W
0111000	8	8	1011000	X	X
0111001	9	9	1011001	Y	Y
0111010	:	:	1011010	Z	Z
0111011	;	;	1011011	[	Note 1
0111100	<	<	1011100	\	Note 2
0111101	=	=	1011101	]	]
0111110	>	>	1011110	↑	↑
0111111	?	?	1011111	←	←

Note 1: SOM-Not displayed when generated by processor.
Note 2: Reserved for ESCAPE character (Refer to Code Translator, Model 6042).
Note 3: Not displayed.

CONTROL PANEL

VIDEO DATA TERMINAL, MODEL 6050





Note: All characters shown, both upper and lower case, are displayed except for RETURN.

VIDEO DATA INTERROGATOR, MODEL 6051

GENERAL DESCRIPTION

The Video Data Interrogator (VI) is a manually controlled input/output device which, when used in conjunction with an Interrogator Control Terminal (IT), Model 6077, permits communication between a human operator and a data processor. Inquiries and transactions may be composed, visually verified and corrected, if necessary, prior to transmission. The response from the processor may be displayed on the VI as long as the information is useful. Although the general application of this unit is the same as the Video Data Terminal, Model 6050, it will normally be used when several video displays are required on the same premises and can share a common communication line.

The VI operates with the American Standard Code for Information Interchange (ASCII). The VI viewer uses a 14-inch rectangular cathode-ray tube upon which a maximum of 480 characters can be displayed simultaneously.

A movable cursor (displayed as an underscore) provides a continuous indication to the operator of the position in which the next character will be entered on the viewer. Sixteen prerecorded message formats are instantly available for display to enhance the accuracy and convenience of message composition. A four row keyboard is used for the generation of all data and control characters which are to be transmitted.

MODEL DESIGNATIONS

The Model Number designates the character array in accordance with the table below. All VI's common to an IT must be identical.

VI	IT Option	No. of Lines	Char. Per Line	Char. Ht.	Char. Width	Spacing Vert.	Spacing Horiz.
6051-1	A	15	32	.22"	.18"	.40"	.25"
6051-2	B	10	48	.15"	.12"	.40"	.17"
6051-3	C	12	40	.18"	.14"	.40"	.20"

Included with the keyboard in the control panel is a supplementary panel for all supplementary controls and visual indicators. The entire control panel is packaged to permit its attachment to the front of the viewer or independently positioned on a desk, a pedestal, or a convenient horizontal surface.

A maximum of 64 discrete code combinations can be displayed. Other code combinations can be generated by the keyboard. When these codes and certain others which are specifically "not displayed", are included in data, they will be displayed as blanks. Except where special procedures are in effect requiring the generation of non-displayable characters, the presence of a blank within a line of data indicates a possible typing or formatting error.

OPERATION

Pressing the WRITE switch places the Video Data Interrogator in the Write mode and inhibits the Receive Mode. POWER switches on the IT and viewer must be ON. If it is desired to use one of the pre-recorded formats stored in the IT, the appropriate FORMAT switch is pressed. The selected format is displayed on the viewer, and the cursor positioned to the first character location available for manual entry. The desired data is entered through the keyboard, using the cursor controls, as necessary. As each character is entered, the cursor advances to the next character position available for manual entry, skipping all locations occupied by the pre-recorded format information. When the end of a line is reached, the cursor automatically advances to the first available position of the next line.

If the data entered manually occupies less space than is provided by the selected format and fixed field length is not a system requirement, the cursor may be advanced to the first character position of the next field by pressing the SKIP key. The character generated by depression of the SKIP key may be recognized by the processor program as an item separator. When no pre-recorded format is used, pressing the SKIP key enters the SKIP character in memory and advances the cursor one character position.

If it is desired to advance the cursor to the first available position of the next line before reaching the end of a line, the operator presses the RETURN key on the keyboard which also transfers a RETURN character to the display memory. The RETURN switch in the cursor control section of the panel only positions the cursor; therefore, it will normally be used when no RETURN character is desired, such as while making corrections.

Since each displayable character entered is immediately displayed, many typing errors are discovered as they occur. The BACKSPACE control permits convenient repositioning of the cursor so the errored character may be replaced by the correct character.

After the complete message, including the DD2 end of message character, has been entered, it may be visually verified and any corrections accomplished by using appropriate controls and keys. Changes may be made only to the data entered from the keyboard. Absence of a DD2 in the data area of the display memory will prevent the VI from switching to the Transmit mode.

TRANSMITTING

When the accuracy of the message has been established visually, the TRANSMIT control is pressed. The WRITE mode is disabled and the IT is signalled that the message is ready for transmission. Provided a DD2 is present in display memory, the IT exchanges the necessary signals with its data set and accomplishes transmission of the message, less format information if any, in the following sequence:

DD1 (1st char. to line)	VI Identifier	Format Identifier	Data (up to 479 char. max.)	DD2

After transmission has been completed, the TRANSMIT light is extinguished. While awaiting a response from the processor, the contents of display memory and the displayed image are unchanged. If the computer response is not received within a pre-determined time following the transmission of DD2, a timeout occurs. Flashing of the displayed image notifies the operator that the message must be repeated. The Receive mode is cleared but the contents of display memory and the displayed image remain unchanged. Pressing the WRITE switch is required before further operations can be performed. If the processor response is interrupted (DD1 not received) timeout will occur as above. The flashing image will comprise the received data plus any part of the original inquiry not overwritten.

RECEIVING

The processor, upon servicing the message and composing a response, initiates transmission with the SOM (start of message) character, followed by 2 Format Identifiers. The first Format Identifier selects the pre-recorded message format stored locally, causing it to be written to the memory area associated with the VI receiving the message. The second Format Identifier is used for timing only. If no format is to be used, two "no-format" identifiers will be inserted. The processor response has the following format:

SOM (1st char. in line)	Format Identifier	Format Identifier	Data (up to 479 char. max.)	DD1

As each character is received by the IT, it is stored in display memory and displayed on the viewer, consistent with the format used, if any.

Receipt of the SKIP character causes the succeeding character to be placed in the first position of the next area available for input data. Receipt of the RETURN character causes the succeeding character to be placed in the first available position in the next line. If no format has been selected and a SKIP is transmitted in error by the program, it is stored in display memory and the cursor advances one character position.

The processor terminates its transmission with a DD1 character. The DD1 is displayed, and the WRITE indicator is illuminated, indicating to the operator that the message is complete.

When the displayed data has served its purpose, erasure is accomplished by pressing the ERASE switch. The cursor returns to the beginning of the frame. A new message may be composed by pressing the WRITE switch and repeating the message composition.

If it is desired to alter the received message for re-transmission back to the processor, pressing the WRITE switch returns the cursor to the beginning of the frame without changing the contents of display memory. By proper operation of the cursor controls and the keyboard, the received data may be edited and additional information entered until the new message is composed. Transmission of the new message can then be accomplished as previously described.

Note: DD1 and DD2 are selectable for each installation, but must be identical to those utilized by the 3301 Processor.

The following ASCII graphic characters are not displayed upon the viewer:

[- used as SOM character

\ - reserved as the ESCAPE character - Refer to Model 6042 Code Translator.

ACCURACY CONTROL

All data is checked for even parity in the IT. A parity error results in a brightened area equal to a character space on the viewer in the position of the errored character. When receiving, parity is checked on SOM and Format Identifier codes before storing in display memory. If a parity error is detected, the Receive Mode is terminated and the WRITE indicator is illuminated.

Valid ASCII Graphic Codes – Video Data Interrogator
Model 6051–1, 2, 3

ASCII Code b7 b1	ASCII Graphic Symbol	VI Displayed Symbol	ASCII Code b7 b1	ASCII Graphic Symbol	VI Displayed Symbol
0100000	space	space	1000000	@	@
0100001	!	!	1000001	A	A
0100010	"	"	1000010	B	B
0100011	#	#	1000011	C	C
0100100	$	$	1000100	D	D
0100101	%	%	1000101	E	E
0100110	&	&	1000110	F	F
0100111	'	'	1000111	G	G
0101000	(	(	1001000	H	H
0101001	)	)	1001001	I	I
0101010	*	*	1001010	J	J
0101011	+	+	1001011	K	K
010110	,	,	1001100	L	L
0101101	–	–	1001101	M	M
0101110	.	.	1001110	N	N
0101111	/	/	1001111	O	O
0110000	0	0	1010000	P	P
0110001	1	1	1010001	Q	Q
0110010	2	2	1010010	R	R
0110011	3	3	1010011	S	S
0110100	4	4	1010100	T	T
0110101	5	5	1010101	U	U
0110110	6	6	1010110	V	V
0110111	7	7	1010111	W	W
0111000	8	8	1011000	X	X
0111001	9	9	1011001	Y	Y
0111010	:	:	1011010	Z	Z
0111011	;	;	1011011	[	Note 1
0111100	<	<	1011100	\	Note 2
0111101	=	=	1011101	]	]
0111110	>	>	1011110	↑	↑
0111111	?	?	1011111	←	←

Note 1: SOM – Not displayed when generated by processor.
Note 2: Reserved for ESCAPE character (refer to Code Translator, Model 6042.)

Valid ASCII Control Codes – Video Data Interrogator
Model 6051–1, 2, 3

ASCII Code b7 b1	ASCII Control Function	VI Function
0001010	LF	SKIP
0001101	FF	RETURN

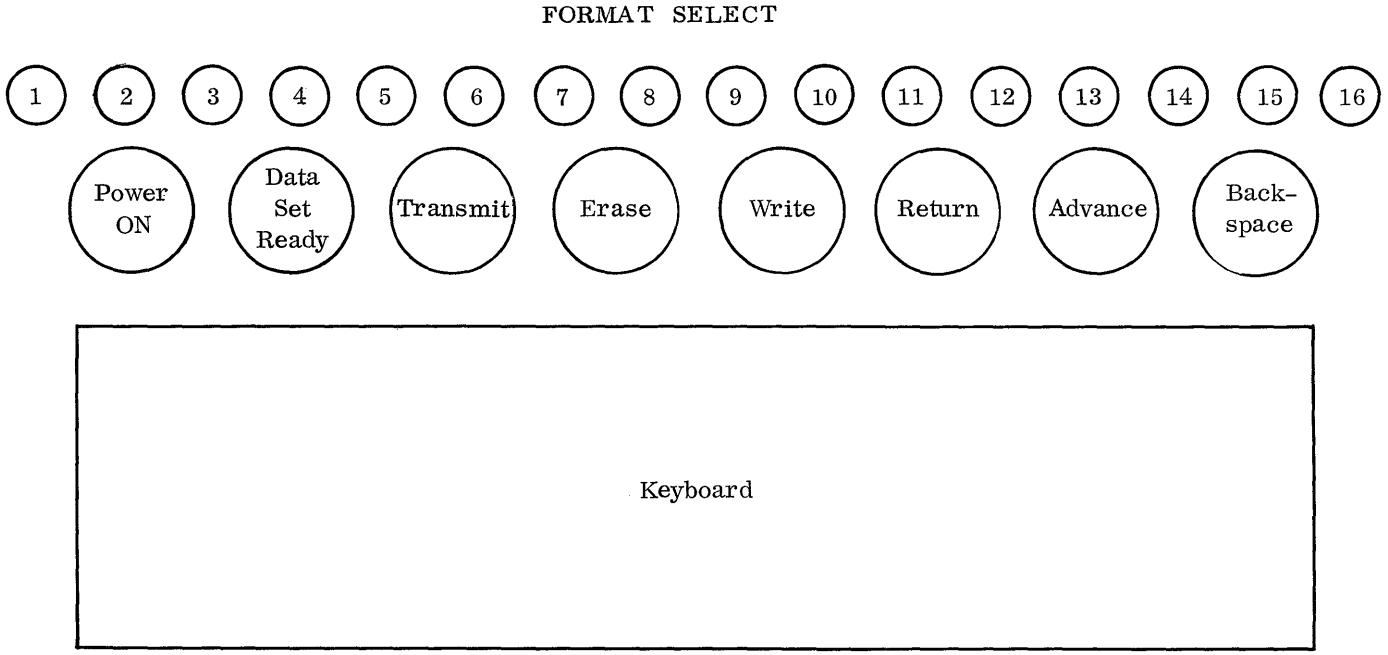
Note: ASCII "NULL" characters (0000000) which occupy locations in memory where no data appears, are neither displayed nor transmitted.

Format Identifier – Video Data Interrogator
Model 6051–1, 2, 3

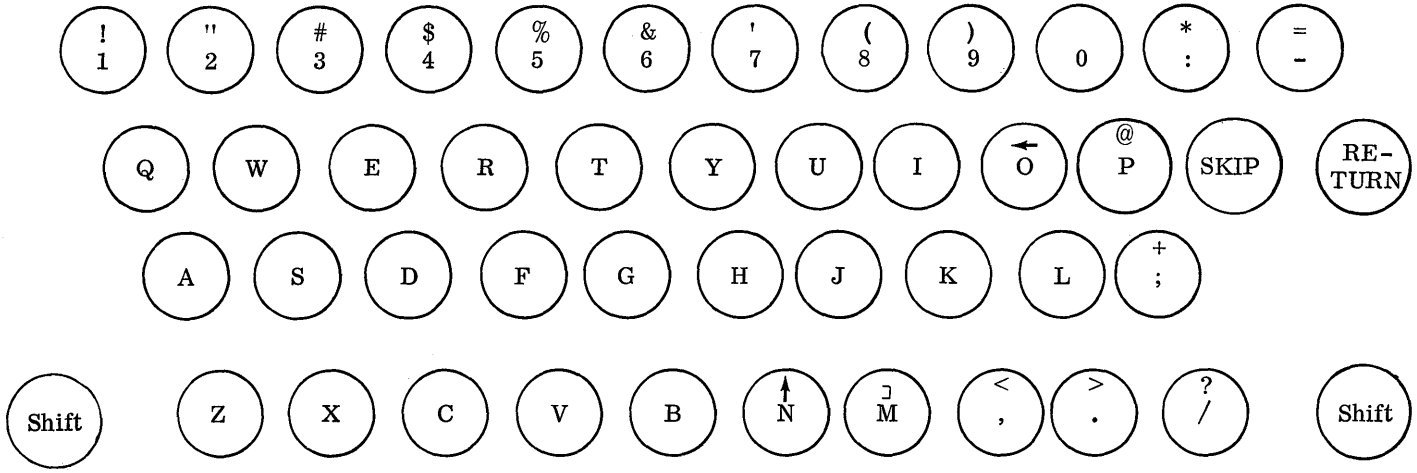
Format No.	Format	ASCII Symbol Generated by VI on Transmission	ASCII Symbols Received by VI from Processor	ASCII Code
		@	@@ (2 char. sequence)	1000000
#1		A	A A (2 char. sequence)	1000001
#2		B	B B (2 char. sequence)	1000010
#3		C	C C (3 char. sequence)	1000011
#4		D	D D (2 char. sequence)	1000100
#5		E	E E (2 char. sequence)	1000101
#6		F	F F (2 char. sequence)	1000110
#7		G	G G (2 char. sequence)	1000111
#8		H	H H (2 char. sequence)	1001000
#9		I	I I (2 char. sequence)	1001001
#10		J	J J (2 char. sequence)	1001010
#11		K	K K (2 char. sequence)	1001011
#12		L	L L (2 char. sequence)	1001100
#13		M	M M (2 char. sequence)	1001101
#14		N	N N (2 char. sequence)	1001110
#15		O	O O (2 char. sequence)	1001111
#16		P	P P (2 char. sequence)	1010000

CONTROL PANEL

VIDEO DATA INTERROGATOR, MODEL 6051



KEYBOARD LAYOUT



Note: All characters shown, both upper and lower case, are displayed except for RETURN.

INTERROGATOR CONTROL TERMINAL – MODEL 6077

GENERAL DESCRIPTION

The Interrogator Control Terminal (IT) provides a common memory and communications terminal along with the required control logic, to service up to eight (8) Video Data Interrogators (VI's), Model 6051. The combination of this unit and an appropriate number of VI's, comprise a Video Interrogation System.

The IT interfaces Bell System 202D Data Set on private line telephone circuits or the 202C Data Set on the message network. This unit communicates with the 3301 via the Model 6010 Communication Buffer in a half-duplex mode. Transmission rates are either 120 or 180 cps. There is no provision for automatic dialing or unattended operation with this unit.

The IT is designated for operation with the ASCII Code. The transmission line character contains 10 bits: 1 start bit, 8 information bits, including parity, and 1 stop bit. The 2^0 bit is transmitted first.

DISPLAY MEMORY

The Display Memory is a rotating magnetic storage device which provides storage for pre-recorded message format information, locally generated data received over the communication channel, as well as timing and cursor control information. The storage capacity of the display memory provides for 480 displayable characters for each of the 8 associated VI's and 16 pre-recorded message formats consisting of up to 481 characters each, including a format identifier which is not displayed. The pre-recorded message formats are accessible by a VI, but can be originally entered or changed only by transmission from the processor.

CHARACTER GENERATOR

The Character Generator converts the digital data and cursor information received from the display memory into video signals for the viewer. One character generator is provided for each interrogator.

OPERATION

TRANSMITTING

The IT sequentially senses the mode of the associated VI's and when one is found to be in the TRANSMIT mode, transmission is initiated. If more than one VI is ready to transmit, they are serviced in sequential order. The connection which permits the transmission of the message generated from a given VI is maintained until the processor response is received, or until a pre-selected period of time has elapsed without a response.

The Transmit mode of a given VI is inhibited in the absence of a DD2 in the corresponding data area of display memory.

The DD2 sets a timer which is reset by the receipt of DD1 from the processor. This timer may be set for a nominal interval of 10, 20, or 30 seconds or may be disabled. The appropriate setting, which may be conveniently made, will be dependent upon the requirements of a particular system. If the DD1 is not received, the timeout causes the displayed image to flash, signalling the operator. Pressing the WRITE switch restores normal operation. The IT continues its scan of the associated VI's.

RECEIVING

The first character received from the processor is the Start of Message (SOM) character. The next character is the Format Identifier which selects the desired pre-recorded message format. A second Format Identifier is included for timing purposes. If format selection is not desired, the "no format" identifier is used. If an invalid format identifier is received, the RECEIVE mode is terminated and the VI is returned to the WRITE mode. The contents of display memory and the displayed image remain unchanged. The text of the message follows which is also displayed. The received message replaces the transmitted message in display memory and is displayed as it is received. The DD1 terminates the RECEIVE mode and resets the cursor to the first available data entry position following the beginning of the frame. The IT continues the scan of the associated VI's.

PRE–RECORDED MESSAGE FORMAT DISPLAY

In response to format selection signals from a VI, the selected format is written to a memory location associated with the selecting VI and displayed until erased. Any combination of VI's may simultaneously select the same or different formats. The format information is recorded in such a manner that it is not possible to position the cursor in a location occupied by a format character. The transmission of format information is inhibited.

PRE–RECORDING OF MESSAGE FORMATS

Operation of the FORMAT WRITE switch shifts the system to the Format Write mode, enabling the initializing or changing of the pre-recorded message formats. One master VI will be designated as the format control station and is used to compose a message to the processor requesting a predetermined format to be recorded. This message must include the format identifier involved. It must be noted at this point that the format identifiers comprehend only the 16 formats recorded in the IT and do not limit any library of formats which may be available through the processor.

The format request message is composed and transmitted in a conventional manner, the content of which is determined by the user program.

The response from the processor follows conventional format including the format identifier supplied in the request. NULL characters are used as required to occupy the data fields and properly position the format headers. Instead of accessing a pre-recorded message format, the operation is altered to record the new format at the prescribed location. When the processor response is complete (indicated by the illumination of the WRITE indicator) it is verified by the master VI operator by his pressing the appropriate format select switch and calling the format to his VI for display. If the response is correct, the FORMAT WRITE switch is returned to OFF and the system returned to normal operation.

DATA DISPLAY

All displayable characters stored on the data tracks are continuously displayed on their respective interrogators. A character may be removed from the display of an operating system only by its replacement by another character (NULL character in the case of erase).

A maximum of 64 discrete code combinations can be displayed. This corresponds to the display capability of the VI.

OPTIONS

Option A - provides for the display on all associated VI's (Model 6051-1) of up to 480 characters in 15 lines of 32 characters per line.

Option B - provides for the display on all associated VI's (Model 6051-2) of up to 480 characters in 10 lines of 48 characters per line.

Option C - provides for the display on all associated VI's (Model 6051-3) of up to 480 characters in 12 lines of 40 characters per line.

Option D - provides an alternate connector to permit direct cabling between the IT and a Communication Buffer Model 6010, eliminating the need for data sets and a communication circuit for distances of up to 50 feet. The cable normally supplied with the 6010 Buffer for data set connection is used for this option.

DATA
EXCHANGE
CONTROL

XIX DATA EXCHANGE CONTROL

GENERAL DESCRIPTION

The Data Exchange Control (DXC) enables an RCA 3301 to communicate with either another RCA 3301 computer equipped with a Data Exchange Control or an RCA 301 computer equipped with a Data Exchange Control, Model 377. Data transmission may be in either direction but in only one direction at a time. Data transmission may be initiated by either computer. An RCA 3301 System may include a maximum of two Data Exchange Controls. Each may communicate with only one DXC in an interconnected system. The maximum distance between controls is 100 feet.

OPERATION (3301 TO 3301)

Communication between two computers via the Data Exchange Control is accomplished by standard 3301 input/output instructions. Several variations of the Test Device (TDV) instruction are used in the signaling computer to test and control the signaled computer. Test functions determine the operability of the computer and DXC, the receive or transmit status of the DXC, and the validity of the data transmitted.

The dual test and control function of the TDV instruction first tests if the signaled computer's DXC has pre-empted the channel. If it has not, the channel is assigned to the signaling computer, and the External Interrupt Indicator is set in the signaled computer. The signaling computer then initiates a read or write in preparation to receive or send data and waits for a response. When interrupt occurs, the signaled computer responds to the signaling computer. Upon testing the status (sending or receiving) of the signaling computer, the signaled computer initiates a response action in the form of a read or write. Transmission of data then occurs based on the action taken by both computers.

INSTRUCTIONS

The following instructions are utilized for programming the DXC:

Read Forward Simo 1 (RF1)	Read Forward Simo 2 (RF2)
Write Simo 1 (WR1)	Write Simo 2 (WR2)
Test Device (TDV)	

These instructions are presented by function under the headings: (1) Testing and Controlling, (2) Sending, and (3) Receiving.

TESTING AND CONTROLLING

GENERAL DESCRIPTION

The Test Device (TDV) instruction tests and/or controls the interconnected computers. Control is transferred if the condition or conditions being tested are present. Options may be performed separately or in combination.

FORMAT

OPERATION - S

N - ÷ if first DXC, , (comma) if second DXC

A ADDRESS - Specifies function to be performed

Character	Bit Position	Symbol	Test or Control Function
A_0	$2^0 = 1$	1	Is the signaled computer or DXC inoperable?
A_0	$2^1 = 1$	2	Is the signaled computer in a receive mode?
A_0	$2^2 = 1$	4	Is the signaled computer in a transmit mode?
A_0	$2^3 = 1$	8	Has a character with incorrect parity been received? (Sending or receiving computer may make test.)
A_1	$2^0 = 1$	1	Has the signaled computer requested the channel?
A_1	$2^2 = 1$	4	Has the receiving computer reached A/B equality before receiving a terminate signal from the sending computer.
A_3	$2^0 = 1$	1	Assigns the channel to the signaling DXC and sets the External Interrupt Indicator in the signaled computer, if the channel has not been pre-empted by the signaled computer.

Unused characters must be zeros and are not to be used by programming.

B ADDRESS - HSM location of the next instruction to be executed if the condition(s) being tested is (are) present.

SPECIAL CONDITIONS

STP is performed if the condition(s) specified by A Address is(are) present.

OUTLINE OF OPERATION

The A_0 A_1 tests are performed, and if any one condition is met, control is transferred to the instruction specified by the B address. If no condition is met, the next instruction in sequence is performed.

The A_3, $2^0 = 1$ option performs a command to the DXC and is used when a computer desires to initiate a data exchange. The channel is assigned to the requesting DXC, a channel-busy flip-flop is set in both DXC's, and the External Interrupt Indicator is set in the signaled computer.

When signaling may be performed by either computer, the A_1 $2^0 = 1$ test must be combined with the command option to insure channel availability.

FINAL SETTINGS

$(A)_f = (A)_i$

$(B)_f = (B)_i$

SENDING

GENERAL DESCRIPTION

The Write Simo 1 (WR1) or Write Simo 2 (WR2) instruction is used for sending data across the transmission channel to an interconnected computer which in conjunction initiates a read command commencing the actual transmission of data.

FORMAT

OPERATION - 8 (WR1) of 9 (WR2)

N - ÷ if first DXC, , (comma) if second DXC

A ADDRESS - HSM location of the first character to be sent. (Must be an even address)

B ADDRESS - HSM location of the last character to be sent. (Must be an even address)

DIRECTION OF OPERATION

Characters are transferred from HSM left to right.

OUTLINE OF OPERATION

When a write instruction is accessed, the transmit mode flip-flop is set in the DXC. When the receive mode flip-flop is set by a read instruction in the other DXC, transmission begins. Data is transferred from HSM a diad at a time until A/B equality is reached by the write instruction. If no errors occurred during transmission, the Mode Terminated Normally Interrupt Indicator is set in the sending computer.

If the read instruction from the receiving computer terminates (resetting the receive mode flip-flop) before the write, the write instruction holds off until the receive mode flip-flop is set by initiation of another read.

FINAL SETTINGS

$(S)_f$ or $(C)_f$ = HSM location two to the right of the last character sent (Normally $B_i + 2$).

$(T)_f$ or $(E)_f = (B)_i$

GENERAL DESCRIPTION

The Read Forward Simo 1 (RF1) or Read Forward Simo 2 (RF2) instruction is used for receiving data across the transmission channel from the sending computer which in conjunction initiates a write command commencing the actual transmission of data.

FORMAT

OPERATION - 4 (RF1) or 5 (RF2)

N - ÷ if first DXC, , (comma) if second DXC

A ADDRESS - HSM location to receive the first character. (Must be an even address)

B ADDRESS - HSM location to receive the last character. (Must be an even address)

DIRECTION OF OPERATION

Characters are transferred into HSM left to right.

OUTLINE OF OPERATION

When the read instruction is accessed, the receive mode flip-flop is set in the DXC. When the transmit mode is set in the sending DXC, transmission begins. The read instruction terminated normally if A/B equality occurs in the sending computer. If the read terminates with A/B equality, but the write has not terminated, an abnormal termination results in the receiving computer; the write continues to occupy the channel until the receive mode flip-flop is set by initiation of another read.

FINAL SETTINGS

$(S)_f$ or $(C)_f$ = HSM location two to the right of the last character received (Normally $B_i + 2$).

$(T)_f$ or $(E)_f = (B)_i$

3301-301 COMMUNICATION

The previous operation and instruction descriptions are amended in the following areas when communication is between an RCA 3301 and an RCA 301.

1. The control options of the Test Device instruction set only the channel busy flip-flop in the 301 DXC, Model 377. However, when the 301 originates the control option of the Input/Output Sense instruction, an interrupt is effected by the 3301 DXC just as if the originating computer were a 3301.

2. The error termination of a read or write instruction sets the appropriate error flip-flops in the DXC which are sensed by program in the 301, and sets the Mode Terminated Abnormally Interrupt Indicator in the 3301.

TIMING

The data transfer rate is up to 311,042 characters per second.

ACCURACY CONTROL

INOPERABLE

If the DXC is inoperable on attempting to address the device, the Busy or Inoperable Interrupt Indicator is set.

When the sending DXC becomes inoperable during data transmission, the following occurs in the:

1. Sending DXC - The write terminates immediately and the Mode Terminated Abnormally Interrupt Indicator is set.

2. Receiving DXC - The read is terminated through abnormal termination of the write, the Inoperable Indicator and the Mode Terminated Abnormally Interrupt Indicator are set.

When the receiving DXC becomes inoperable during data transmission, the following occurs in the:

1. Receiving DXC - The read terminates immediately, and the Mode Terminated Abnormally Interrupt Indicator is set.

2. Sending DXC - The write terminates immediately through the inoperability of the read and sets the Mode Terminated Abnormally Interrupt Indicator and the Inoperable Indicator.

PARITY ERRORS

When a character with incorrect parity is detected by the receiving DXC; a special error character, subscript 10, $(57)_8$ is substituted for that character before it is transferred to HSM; a parity error indicator ($A^0\ 2^3 = 1$) sensible by either computer is set; and the Mode Terminated Abnormally Interrupt Indicator is set in the receiving computer. Transmission proceeds with error characters $(57)_8$ replacing all incorrect characters.

COMMUNICATIONS
MODE
CONTROL

XX COMMUNICATIONS MODE CONTROL

GENERAL DESCRIPTION

The Communications Mode Control (CMC) permits on-line data input/output transmission between the RCA 3301 computer and various remote devices utilizing standard communication line facilities. Each communication line terminates in a buffer unit that provides a proper interface to the CMC. This Control also gives an additional degree of simultaneity so that transfer of data in either direction between communication lines and the Processor may be time-shared with other operations. The CMC permits the servicing of one to 160 buffer-terminated communication lines. The CMC is available in line increments of 20.

COMMUNICATION SYSTEM

The RCA 3301 computer provides communication facilities via the Communications Mode Control (CMC), in conjunction with various Interface Units, Buffers, Data Sets, Transmission Lines and Remote sending/receiving devices (see Figure XX-1).

CMC - Performs function of transferring data characters between various Buffers and the 3301 Computer

Interface Units - Electronic devices used to connect multiple Buffer units. These devices contain common electronic circuitry by which Buffer units may communicate with the CMC.

Buffers - Electronic devices which provide one-character storage areas for data being transferred between the transmission lines and the CMC.

Data Sets - Converter units that change d.c. data signals to a.c. tone signals and vice versa.

Transmission Lines - Communications facilities for transferring data between buffers and remote devices.

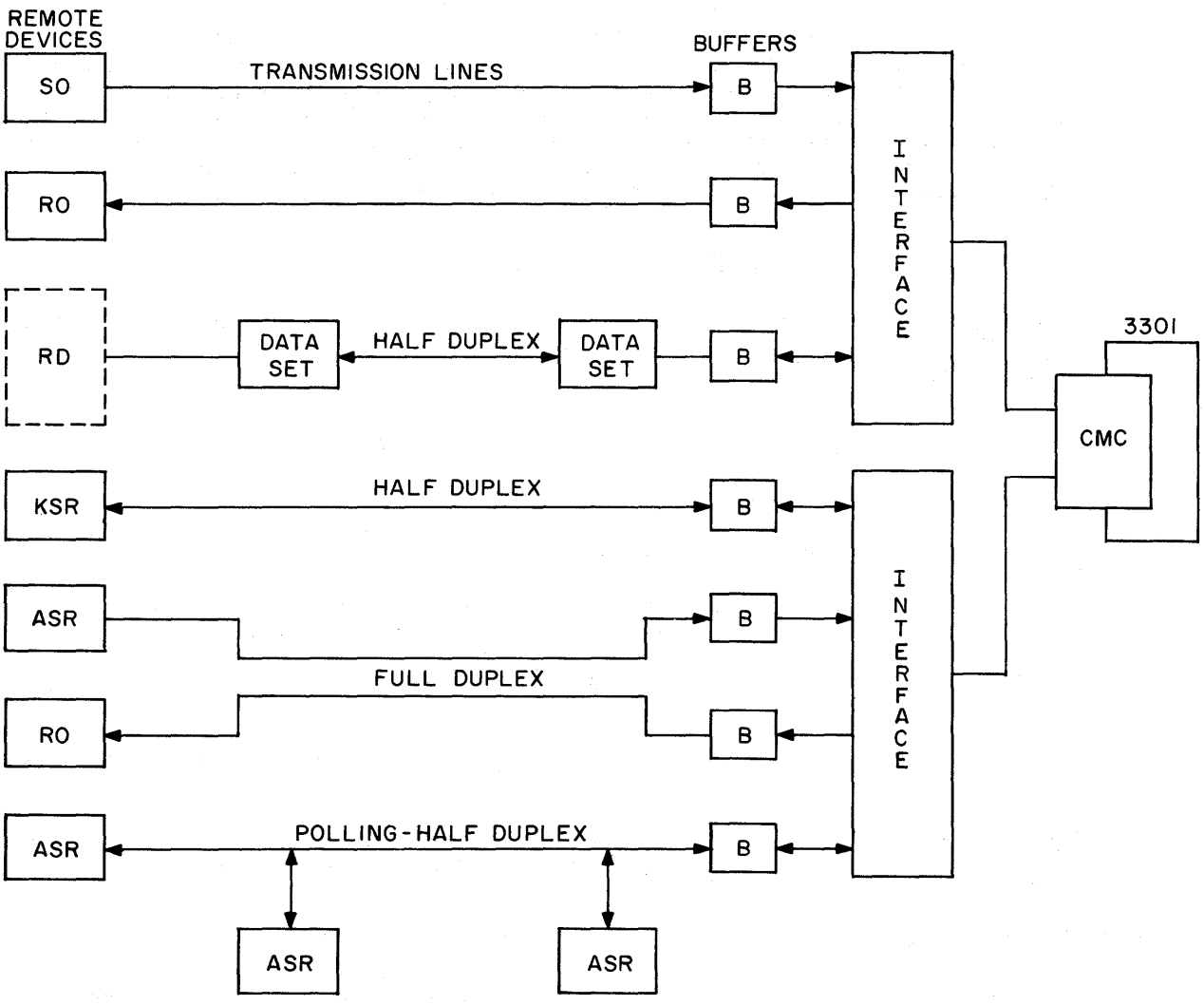
Remote Devices - Units that transmit and/or receive data, such as teletypewriters, paper tape readers, printers, card transceivers, etc.

CMC OPERATION

Data is transmitted from the remote input device via a transmission line to the input line Buffer (Receiver) in bit-serial form; then to the CMC, in bit-parallel form. From the CMC, the data moves into HSM. During the output operation, data follows the same path but in a reverse direction.

The CMC sequentially scans the communication line buffers to determine individual buffer status, i.e., whether it is in the input or output mode; whether it is in a Ready or Not Ready condition. If the Ready condition exists, one character is accepted from the buffer unit for transmission to the 3301, or from the 3301 for transmission to the buffer unit. The scanning is accomplished independently of the computer and the currently operating program. Only one buffer is scanned or serviced at any one time.

Each buffer has an associated 100-character storage area in the 3301 HSM which is called a line slot. Each 100-character memory area holds data being received from or transmitted to a particular line. When action by the program is required to service a line slot, the CMC places the address of the line slot into the Service Table in HSM and sets the CMC Service Request Interrupt Indicator causing an interrupt. Upon interrupt the program accesses the Service Table to obtain the address of the line slot which requires service. Refer to Figure XX-2.



LEGEND

SO	-	SEND ONLY OPERATION
RO	-	RECEIVE ONLY OPERATION
RD	-	REMOTE DEVICE
DATA SET	-	LEASED TELEPHONE LINE OR DIAL TELEPHONE NUMBER
KSR	-	KEYBOARD SEND/RECEIVE
ASR	-	AUTOMATIC SEND/RECEIVE
B	-	BUFFER

Figure XX-1. Sample Communication Network

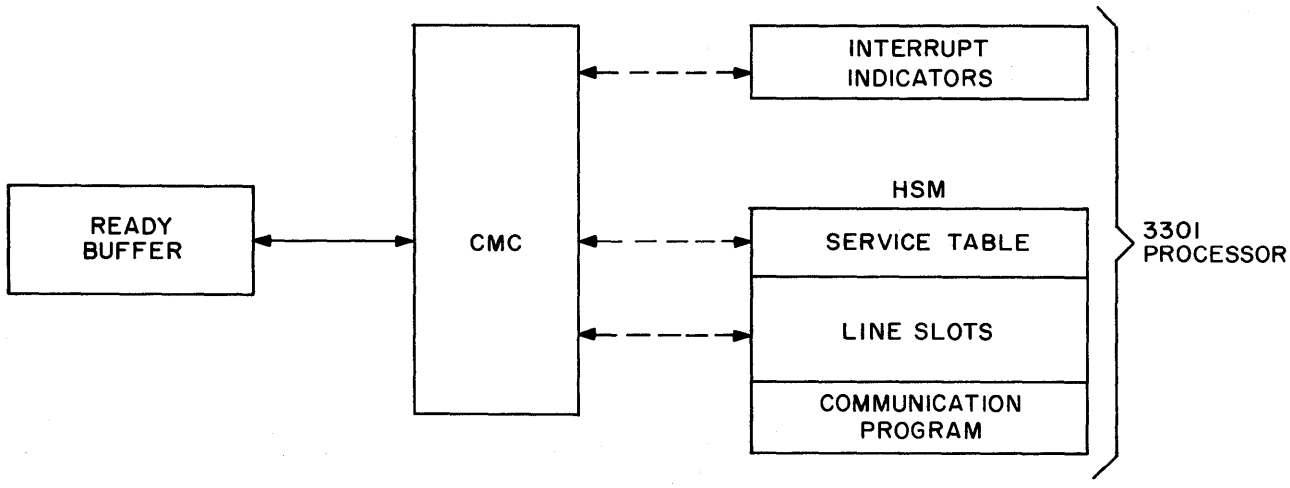


Figure XX-2. CMC - Processor Communication

BUFFER SCANNING

The CMC tests each buffer to determine the following conditions:

READY or NOT READY: Ready means that a character is available to be moved into the CMC from the buffer or that the buffer is prepared to receive a character from the CMC. Not Ready indicates that there is no character to be moved from the buffer to the CMC or that the buffer is not prepared to receive a character from the CMC. Upon finding the buffer Not Ready, the CMC will step to the next buffer in sequence.

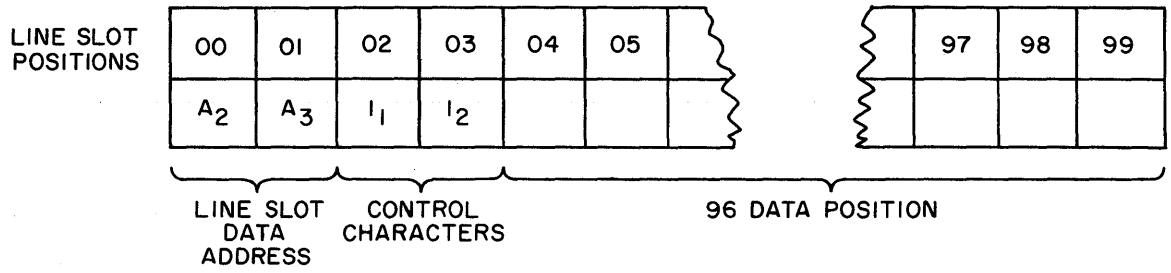
INPUT or OUTPUT: This test determines the input or output status of the buffer and is made simultaneously with the Ready-Not Ready test. If the buffer is found to be Ready, the CMC will perform the appropriate character transfer based on the input/output status of the buffer. Following character transfer, the CMC then scans the next buffer in sequence.

REMOTE OK: When the CMC receives a Ready signal from the buffer, it is also conditioned to receive a Remote OK signal. This informs the CMC that the communications link between buffer and remote device is functioning normally, and that no error was detected on the previous transmission. If the Remote OK signal is not received, the CMC communicates this information to the program.

LINE SLOTS

Line slots are contiguous 100-character HSM segments which hold data being received from, or transmitted to, a particular buffer and line. Line slots for the CMC may be floated anywhere in HSM within a 40,000character block. The first line slot must begin at a HSM address of XX00 and extend to an address of XX99.

Each 100-character line slot is organized as follows:



Positions

00-01 The first two positions in the line slot are used by the CMC to store the two least significant characters (A_2 A_3) of the address where the next data character is to be transferred to/from the line slot. The two most significant characters are determined by the CMC from the scan position, i.e., the particular buffer, being serviced. After a character is transferred, the CMC increments A_2 A_3 by one to establish the next character position to be accessed. The address XX99 is not incremented but is automatically set to XX04.

02 I_1 control character. This position can be considered as the CMC's method of communicating with the program. Generally, the presence of particular bits indicate that particular tests have been made which had a positive result.

03 I_2 control character. This position can be considered as the program's method of communicating with the CMC. Generally, the presence of particular bits indicate particular tests to be performed by the CMC.

04-99 These locations are used to store up to 96 data characters.

SERVICE TABLE

The CMC places in this table the two most significant characters of the address(es) of the line slot(s) which require servicing. A CMC with up to 100 lines uses a 100 character table. A CMC with more than 100 lines utilizes a 200 character table. The address of the Service Table must be a multiple of 1000 and is stored in the CMC. The two least significant digits of the address (A_2 A_3) determine where the CMC is to make the next entry in the table. The CMC will increment A_2 A_3 by "02" after an entry is made. When an entry placed in the last location in the table, A_2 A_3 is automatically set to "00", and the next entry is placed in "00-01".

CMC RECOGNITION CAPABILITIES

The CMC includes circuitry to recognize the following characters and conditions when requested to do so by the I_2 control character.

NTH POSITION

Upon request the CMC can recognize whenever a character has been transferred to/from the last data position in a line slot. In addition, the CMC may be plugboard-wired to recognize a data character transfer to/from a specific position in a line slot. Any data position may be used as Nth, but this position is constant for all line slots within the system. Normally, Nth is chosen to minimize line slot servicing by the program by providing an adequate overflow area to insure that no incoming data is lost.

DATA DELIMITERS

Two characters may be selected by plugboard control which, upon request, will be recognized by the CMC when transferred. Any legitimate 3301 characters may be chosen but will remain constant for all line slots in the system. One use for Data Delimiters is to use them as start and end message indicators.

SHIFT CHARACTERS

Five-level telegraph transmission codes use shift characters to increase the number of characters that may be represented. When requested, the CMC recognizes the shift characters and interprets the characters that follow them accordingly. These characters are plugboard selectable and remain constant throughout the system.

ERRORS

Parity errors are recognized by the CMC upon request. Various remote/transmission errors are automatically recognized.

INPUT/OUTPUT

The CMC and the program can regulate the flow of characters to/from the line slot via the control characters. The CMC will act accordingly.

I_2 CONTROL CHARACTER

In order to transfer a character either to or from a particular line slot, the CMC examines the I_2 character for rules of operation. The bits of this character are set initially by the 3301 program; therefore, the I_2 character can be considered as the program's method of communicating with the CMC. Where a "1" appears in a bit position, the operation associated with that bit position is required on that particular line. Bit combinations are permissible. The following tests are specified via the I_2 character in position "03" of each line slot.

Bit Position	Description
2^5	Test for Nth Position
2^4	Test for Data Delimiter #2 (DD2)
2^3	Test for Data Delimiter #1 (DD1)
2^2	Test for Shift Status
2^1	Test for Parity
2^0	Output Status

TEST FOR NTH POSITION (2^5)

The CMC's ability to recognize Nth position on other than the 96th data position effectively divides a line slot into two parts which, in some cases, may be useful in the orderly handling of messages. Any data position may be designated as the Nth character position, but it must be consistent for all line slots. For example, if a given line were to use position "83" (80th data character) as Nth, then Nth would be "83" for the entire system. The Nth character position is plugboard selectable. The 96th data position (position 99) also functions as an Nth position.

TEST FOR DATA DELIMITER #2 (2^4)

The program can request notification from the CMC whenever a DD2 is recognized by setting this bit to "1". The bit configuration of DD2 is specified by plugboard and must be constant for all line slots in the system. If recognition is not called for, DD2 will be treated as a data character.

TEST FOR DATA DELIMITER #1 (2^3)

The program can request notification from the CMC whenever a DD1 is recognized by setting this bit to "1". If recognition is not called for, DD1 will be treated as a data character. The bit configuration of DD1 is specified by plugboard and must be constant for all line slots in the system.

TEST FOR SHIFT STATUS (2^2)

This bit is normally used with 5-level codes, such as the telegraph (Baudot) code, which employ shift characters (Letters and Figures) to effectively increase the number of distinct characters which can be represented.

On data input, the need for Letters or Figures recognition by the CMC is to determine how the succeeding characters are to be interpreted. Since some figures and letters have the same five-bit configuration, their proper identity is determined by the shift character which preceded them. When this test is called for, the CMC places a "1" bit in the 2^5 of all characters following a Letters Shift Character and a "0" bit in the 2^5 of all characters following a Figures Shift Character. The shift characters are deleted from the input message.

On data output, the 2^2 bit of the I_2 character notifies the CMC that appropriate Letters and Figures Shift Characters must be inserted in the data as changes from upper to lower case, and vice-versa, are made. For example, characters in the line slot containing a "1" bit in the 2^5 position must be interpreted as letters, or lower case, characters. If the last shift character transmitted was Letters, the character (minus the 2^5 and parity bit) is transferred to the buffer. If the last shift character was Figures, a Letters Shift Character is generated by the CMC to precede the data character, permitting the receiving equipment to respond properly.

The bit configurations of the shift characters are specified by plugboard and must be constant for all line slots in the system. If recognition is not called for, shift characters are treated as data characters.

An option is provided which permits operation with telegraph networks utilizing the "Unshift on Space and Letters" feature. In this case the space character acts as a Letters Shift Character except that it is transferred to/from memory.

TEST PARITY (2^1)

This test is used on codes with parity to determine the validity of incoming data. A special error character, subscript$_{10}$ $(57)_8$, is substituted and transferred to HSM for a character received with incorrect parity.

OUTPUT STATUS (2^0)

This bit enables the program to control the transfer data from a line slot to the CMC provided the buffer is output ready. A "0" in this bit position indicates that output is prohibited. The program may set this bit to "1" whenever output is permitted. The CMC, however, will reset this bit to "0" when any of the following conditions occur during an outgoing transmission:

1. Error Recognized (REMOTE NOT OK)

2. DD1 or DD2 Recognized
3. Double Nth Condition Recognized (No program action was taken on the previous recognized Nth condition)
4. Nth Condition Not Requested But Recognized (99th line slot position accessed and Nth recognition not requested)

I_1 CONTROL CHARACTER

The I_1 control character can be considered as the CMC's means for communicating with the program and for storing information for its own use. As discussed under the description of the I_2 character, the CMC can be requested to perform various tests; the results of these tests are recorded in the bits of the I_1 character. Except for the 2^0 position, the bit-by-bit breakdown of the I_1 character has a "one for one" relationship to the bits in the I_2 character. For example, if the 2^5 bit of I_2 requests an Nth test, the 2^5 bit of I_1 is set to "1" when an Nth condition is recognized.

The bit positions of I_1 are as follows:

Bit Position	Description
2^5	Nth Position Recognized
2^4	Data Delimiter #2 (DD2) Recognized
2^3	Data Delimiter #1 (DD1) Recognized
2^2	Shift Character Status
2^1	Error Recognized
2^0	Input Status

NTH POSITION RECOGNIZED (2^5)

The CMC sets this bit to "1" when the 96th data position or a specific Nth location has been serviced during an input or output operation. However, the Nth recognized bit will not be set on input when the Nth location contains a DD2 symbol and will not be set on output if it contains a DD1 or DD2 symbol. If this bit is set to "1", the CMC Service Request Interrupt Indicator is set, and interrupt occurs.

DATA DELIMITER #2 (DD2) Recognized (2^4)

The CMC executes the following operations when a DD2 symbol is recognized;

DD2 Symbol IN

1. DD2 Recognized bit is set to "1."
2. The Input Status bit is set to "1" (prohibit input).

DD2 Symbol OUT

1. DD2 Recognized bit is set to "1."
2. The Output Status bit is set to "0" (prohibit output).

Whenever a DD2 is recognized, the CMC Service Request Interrupt Indicator is set, and interrupt occurs.

DATA DELIMITER #1 (DD1) RECOGNIZED (2^3)

The CMC executes the following operations when a DD1 symbol is recognized:

DD1 Symbol IN

1. DD1 Recognized bit is set to "1"; all other I_1 bits are set to "0."
2. A_2 A_3 is set to "04."
3. DD1 symbol is placed in the line slot at "04."
4. A_2 A_3 is incremented by "01."

DD1 Symbol OUT

1. DD1 Recognized bit is set to "1" - all other I_1 bits are set to "0."
2. The Output Status bit is set to "0" (prohibit output).
3. A_2 A_3 is set to "04."

Whenever a DD1 is recognized, the CMC Service Request Interrupt Indicator is set, and interrupt occurs.

SHIFT CHARACTER STATUS (2^2)

This bit is set and reset by the CMC as follows:

1. When a Letters Shift Character is recognized, the bit is set to "1." If the "Unshift on Space" option is used, and a space character is recognized, this bit is set to "1."
2. When a Figures Shift Character is recognized, the bit is set to "0."

By interrogating the current setting of this bit, the CMC can determine if an incoming data character is to be treated as a letters or figures character; or during outgoing transmission, if it is necessary to generate a Figures or Letters Shift Character. If a shift test is not requested, this bit position is ignored.

ERROR RECOGNIZED (2^1)

This bit position is used by the CMC to record recognition of the following error conditions. Only a parity error condition need be requested to be recognized.

1. Input parity error (if a parity check has been requested by program). In the event of a parity error, the CMC substitutes a $(57)_8$ for the incorrect character, and sets the Error Recognized bit to "1."
2. REMOTE NOT OK response; i.e., failure of CMC to receive a Remote OK signal from the buffer unit. The CMC on a REMOTE NOT OK error takes the following action:

   Input (Receiving data from remote location)

   Place $(57)_8$ character in line slot.

   Set Error Recognized bit to "1."

Output (Transmitting data to remote location)

Set Error Recognized bit to "1."

Prohibit further output from memory by setting Output Status bit ($I_2 2^0$) to "0."

The CMC Service Request Interrupt bit is set if REMOTE NOT OK, and interrupt occurs.

3. A double Nth condition has arisen; i.e., an "Nth" position has been recognized without the program completing its operation of the previous Nth recognition. The CMC on a double Nth condition will take the following action:

   Input

   Set Error Recognized bit to "1."

   Prohibit further input by setting $I_1 2^0$ to "1."

   Output

   Prohibit further output by resetting $I_2 2^0$ to a "0."

   The CMC Service Request Interrupt Indicator is set on a double Nth condition, and interrupt occurs.

4. Nth position accessed (line slot location 99), and program has not requested an Nth test. The CMC takes the following action:

   Input

   Set Error Recognized bit to "1."

   Output

   Set Error Recognized bit to "1."

   Prohibit further output from memory by setting Output Status bit ($I_2 2^0$) to "0."

   In both cases the CMC Service Request Interrupt Indicator is set, and interrupt occurs.

5. Two conditions, considered as CMC malfunctions, are detectable in the CMC and cause only the CMC Service Request Interrupt Indicator to be set. The first condition is the improper counting of status levels. The second is a buffer interface error indicating that a buffer has responded improperly to CMC signals for a prolonged period. When either condition occurs, a two-digit error code, "ee", $(17)_8$ $(17)_8$, is placed in the Service Table instead of the line slot address, and the Error Recognized bit (2^1) is not set.

INPUT STATUS (2^0)

This bit position signifies whether or not a line slot is ready to accept incoming traffic. It is used by the CMC to control transfer of data between the buffer and line slot. A "1" bit denotes that input is prohibited; a "0" bit indicates that input is permitted. Although the program may set this bit to "0" to permit input, the CMC will reset this bit to "1" when any of the following conditions occurs during an incoming transmission:

1. A double Nth condition.
2. DD2 received.

PROGRAM - CMC COORDINATION

When the program services the line slot, making it available for continued access by the CMC, the new status must be communicated to the CMC. HSM access by the CMC is not under program control, nor does the program have any means by which it can determine if the CMC is accessing a particular line slot at a given time. To avoid conflicting operations by the program and the CMC in the setting and resetting of the I_1 and I_2 characters, the program must follow a strict resetting procedure.

Initially, the 2^5, 2^4, and 2^3 bit positions (Nth, DD2 and DD1) of I_1 and I_2 are in a "0-1" condition if these tests are desired. When the test is performed and found positive, the CMC creates a "1-1" condition.

Whenever the program finds a "1-1" condition, it should set the I_2 bit to "0." The CMC is designed so that whenever it finds the 2^5, 2^4, or 2^3 bit positions in I_1 and I_2 in a "1-0" condition, it resets I_1 bit to "0" and the I_2 bit to "1." Thus the CMC automatically creates the initial and desired condition; i.e., "0-1." If these procedures are not followed, invalid processing may result.

The $I_1 2^2$ bit position (Shift Status) is set and reset by the CMC only and need not concern the program. The Errors Recognized bit (I_1 2^1) is reset to "0" by the program. The I_1 and I_2 2^0 bits are reset at the program's discretion depending upon the application involved.

CMC TIMING

Several variables are involved in CMC timing considerations. Among these are memory accesses, CMC scan rates, and HSM interrupt rates.

MEMORY ACCESSES

The following memory accesses (1.93 μs) are required to transfer a character between the 3301 and the CMC:

1. Access A_2 A_3 I_1 I_2
2. Transfer character to/from HSM
3. Replace A_2 A_3 I_1 I_2

If a condition requiring interrupt occurs, this additional memory access is performed:

4. Transfer A_0A_1 (Line Slot Address) to the Service Table

SCAN RATES

The CMC is available in either single or dual scan rate models. Since scan models service all buffers in a continuous sequence. Dual scan models are plugboard-wired to permit high speed lines to be serviced more frequently than low speed lines by:

1. Specifying which contiguous scan positions (from 1 to 20) are to be scanned at a higher rate. These must begin at the first scan position in the system.

2. Selection of the number (1-15) of single scan rate positions to be scanned following each high speed scan.

For example, if the first eight scan positions are wired for the high servicing rate, and the number of single scan rate positions is set to 11, a 40-scan CMC unit would be serviced as follows:

1-8, 9-19, 1-8, 20-30, 1-8, 31-40, 1-8, 9-19, etc.

INTERRUPT RATES

The CMC takes one out of every 6, 10 or 20 machine cycles. A HSM interrupt rate of 1/6, 1/10 or 1/20 is plugboard selectable.

SINGLE SCAN TRANSMISSION RATES

To determine the approximate maximum transmission rate the CMC can handle, solve the following equation:

$$\text{Max. Transmission Rate (in characters per second)} = \frac{1{,}000{,}000 \text{ (Interrupt Rate)}}{7.72 \text{ (No. of Scan Positions)}}$$

The above equation assumes that at every scan position a character is transferred to/from a line slot, and that a condition causing interrupt occurs. The constant (7.72) represents four memory accesses of 1.93 μs each. The time needed to service a line slot does not decrease, however, if memory accesses are less than four.

DUAL SCAN TRANSMISSION RATES

The same equation used to find the Single Scan maximum transmission rates is used with the Dual Scan Series. Here, however, the problem is to find the appropriate interrupt rate. For example: if a system uses 16 300-character per second lines and 48 10-character per second lines, the two plugboard settings may be set as follows:

High Speed Scan - 16 lines

Low Speed Scan - 2 lines

Since only 2 low speed lines are scanned after each high speed scan cycle, each of the 16 high speed lines is scanned 24 times while the 48 low speed lines are scanned once $(\frac{48}{2})$. With this 24:1 ratio, the low speed lines are scanned more frequently than the transmission rate ratio (30:1) warrants. Therefore, timing based on the high speed lines should be used. For timing purposes this system contains 18 high speed lines (16 high speed + 2 low speed per high speed scan cycle). By the equation:

$$300 = \frac{1{,}000{,}000 \text{ (X)}}{7.72 \text{ (18)}}$$

$$X = .0416 \text{ which is less than } \frac{1}{20}.$$

Therefore a $\frac{1}{20}$ interrupt rate may be selected.

INSTRUCTIONS

The following instructions are utilized when using the CMC:

Test Device (TDV)

Control CMC (COC)

TEST DEVICE (TDV)

GENERAL DESCRIPTION

The Test Device (TDV) instruction is used to determine if the CMC is stopped. Control is transferred if the condition tested is present.

FORMAT

OPERATION - S

N - Y

A ADDRESS - $A_0 = 2$ Is the CMC stopped?

A_1 A_2 A_3 must be zeros and are not to be used by programming.

B ADDRESS - HSM location of the next instruction to be executed if the CMC is stopped.

SPECIAL CONDITIONS

STP is performed if the condition specified by the A Address is present.

FINAL SETTINGS

$(A)_f = (A)_i$

$(B)_f = (B)_i$

GENERAL DESCRIPTION

The Control CMC (COC) instruction is used to start the CMC, stop the CMC, and specify the location of the line slots and the Service Table in HSM.

FORMAT

OPERATION - E

N - Y

A ADDRESS - A_0A_1 = Beginning HSM address of last line slot (leftmost two characters).

A_2A_3 = Beginning HSM address of first line slot (leftmost two characters).

B ADDRESS - B_0B_1 = Beginning HSM address of Service Table (leftmost two characters).

B_2 = Zero (0). Not to be used by programming.

B_3 = 0 Start CMC

B_3 = 1 Stop CMC

OUTLINE OF OPERATION

A_2 A_3 must be specified when the start option is included. The A_0 A_1 characters are specified for programming and are not utilized by the CMC. The Service Table and the first line slot must begin at HSM addresses that are a multiple of 1000.

FINAL SETTINGS

$(A)_f = (A)_i$

$(B)_f = (B)_i$

CMC - BUFFER INTERFACE, MODEL 6025

GENERAL DESCRIPTION

This unit contains the transmitters and receivers which provide compatible interchange signals between the CMC and up to ten (10) buffer units. Each Buffer Interface Unit (BIU) is capable of pre-empting 10 CMC scan positions. Four models of the BIU are available as follows:

Model 6025-10: Capable of including one Speed Set.

Model 6025-15: Capable of including one Speed Set and one Timing Set.

Model 6025-20: Capable of including two Speed Sets.

Model 6025-25: Capable of including two Speed Sets and one Timing Set.

Five Speed Sets are available for selection depending upon the models of buffers utilized:

Speed Set #1: 45 and 50 bps

#2: 56 and 74 bps

#3: 74 and 110 bps

#4: 1050 and 1800 bps

#5: 1200 and 1800 bps

CMC SEL signals can be limited to the actual number of buffers in sequence being served by the BIU via a lockout switch. Each BIU contains an Alarm Indicator which is illuminated whenever a buffer is malfunctioning or an error signal is received. A buzzer is associated with the Alarm Indicator which is activated by the same error conditions.

One Timing Set is available for line frequencies of 100 ms. and 400 ms. using a 60 cycle power source. The Speed Set and Timing Set that must be utilized for associated buffers are as follows:

Buffer Model	Speed Set	Timing Set
6002	1	-
6002	2	-
6003	1	-
6003	2	-
6009	3	1
6010	4 or 5	1
6012-11,12	-	1
6012-21,22	4 or 5	1
6013	1	1
6013	2	1
6015	1	1
6015	2	1
6016	-	1
6020	3	1

TELEGRAPH BUFFER, MODEL 6002-6003

GENERAL DESCRIPTION

These buffer units transmit and/or receive data in 5-level code (Model 6002) or 6-level code (Model 6003) over standard telegraph lines. The telegraph transmission line connects the buffers with a remote station(s) equipped with standard telegraph transmitting and/or receiving equipment. One 100-character line slot is reserved in HSM to service each Model 6002 buffer, and each occupies one CMC scan position. The Model 6003 buffer unit is comprised of two independent buffers. Each buffer occupies one scan position, utilizes one line slot, and is capable of transmitting and receiving data.

Model 6002-11

Handles data for domestic telegraph equipment operating at 6, 7.5 or 10 characters per second.

Model 6002-12

Same as 6002-11, with an additional Clear-To-Send function. This function is used with multi-station lines and certain common carrier remote units that require a Clear-To-Send signal before transmitting.

Model 6002-21

Handles data at 6.7 characters per second for transmission via Telex circuits.

Model 6003

Handles data at 5.3 or 6.6 characters per second for special news wire service.

OPERATION

The buffer may operate in one of three modes (receive only, transmit only, or half duplex) determined by a switch setting located on the buffer unit. In each mode the CMC, telegraph buffer and remote equipment communicate with each other via the following control signals:

CMC-TO-BUFFER

Select (SEL)
CMC Ready (CRDY)
DD2 Recognized (DD2R)
DD1 Recognized (DD1R)

BUFFER-TO-CMC

Buffer Status (BSI/BSO)
Buffer Ready (BRDY)
Remote OK (ROK)

REMOTE EQUIPMENT-TO-BUFFER

Receive Data (RD)
Clear-To-Send (CTS) (Model 6002-12 only)

BUFFER-TO-REMOTE EQUIPMENT

Transmit Data (TD)

RECEIVE FUNCTION

Initially, an RD signal indicates to the buffer that data is arriving. The buffer collects the data and assembles it into a character. The CMC, when it advances its scan position to this buffer, sends a SEL signal to the buffer. If there is no complete character assembled, the buffer does not respond with a BRDY signal, and the CMC advances to its next scan position. When a complete character is present following a SEL signal, the buffer responds with BRDY, BSI and ROK signals. The CMC then interrogates the I_1 character in the line slot to see if input is permitted. If not, the CMC advances its scan position and the character is not transferred to the CMC. If input is allowed, the CMC sends a CRDY signal to the buffer. The character is transferred to the CMC and from there to HSM. The above operations occur on a character-by-character basis until input data ceases.

TRANSMIT FUNCTION

The buffer periodically receives SEL signals from the CMC. If no data is being handled by the buffer, it responds with BRDY, BSO, and ROK signals. If the I_2 character in the line slot does not permit output, the CMC advances to its next scan position. Should output be permitted, the CMC sends a CRDY signal and the character to the buffer. The buffer sends a TD signal to the remote device to indicate data is to be transmitted thus inhibiting input.

When data is to be transmitted to a multi-station line via a Switching Control Unit, the Model 6002-12 buffer transmits data only when a CTS signal is received from the control. If this signal is not present when a SEL is received, the BRDY signal is not sent to the CMC, and the CMC advances to its next scan position. Data is transmitted by the above operations on a character-by-character basis until line slot output is exhausted.

HALF DUPLEX FUNCTION

A line may be used for sending and receiving (separately) when the buffer is set to half duplex. The CMC-Buffer-Remote Device communications are the same as those listed in the Receive and Transmit mode. The buffer automatically switches from one mode to the other upon Data Delimiter Recognized signals received from the CMC.

If the buffer is in the Receive mode, and a DD2R signal is received from the CMC, the buffer automatically switches into the Transmit mode. If the buffer is in the Transmit mode, and a DD1R signal is received from the CMC, the buffer automatically switches into the Receive mode.

ACCURACY CONTROL

The Remote OK signal is not sent to the CMC with the BRDY and BSI/BSO signals if there is an "open" transmission line condition or a common carrier equipment malfunction. These conditions are indicated by RD and TD signals that continue for at least "one-character-time". When this occurs, the Interface Unit Buzzer is activated and the buffer inhibits the BRDY signal to the CMC until the condition is corrected. The buffer then returns to its normal operating condition.

COMMUNICATIONS BUFFER - MODEL 6010

GENERAL DESCRIPTION

The Communications Buffer, Model 6010, is used in conjunction with the CMC to couple a 3301 computer to a standard 3KC "voice-grade" communication line, or equivalent, via a digital Data Set unit. Transmission rates range from 105 cps to 180 cps. This buffer may be used in half-duplex operations; it can receive and transmit data, but in only one direction at a time. The buffer occupies one CMC scan position and is associated with one HSM line slot. The transmission line code contains 10 bits per character (1 start bit, 8 information bits, and 1 stop bit). The buffer is capable of handling 5, 6, 7, or 8-level codes via a switch setting located on the buffer. When 7 and 8-level codes are used, a code translator must be used as an interface between the buffer and the Buffer Interface Unit.

Sample remote equipment that may utilize this buffer are the Video Data Terminal, Model 6050-1, and AT&T high speed paper tape terminals (105 cps) such as Dataspeed, Types I and II.

BUFFER MODELS

The Communications Buffer is offered in the following models:

Model 6010-21: Utilizes an AT&T 202 Data Set for private-leased line operations and/or manual dial applications. Transmission rates are up to 120 cps for a dialed call and 180 cps for a leased line connection. The Reverse Channel feature is an installation option available with this model.

Model 6010-22: Utilizes an AT&T 202 Data Set in a dialing network. Dialing may be manual, or automatic if a common carrier Automatic Calling Unit is attached. Unattended Operation, Automatic Disconnect and Reverse Channel features are installation options available with this model. The transmission rate is up to 120 cps.

AT&T Data Set model numbers are shown only as an example. Equivalent Data Sets of other manufacturers may be used. The Model 202 Data Set is asynchronous and speeds "up to" the values mentioned can be obtained.

OPERATION

The Communications Buffer, when operating in a half-duplex mode, is ready to transmit or receive data. If, while in its neutral state, signals are received from the transmission line, the buffer automatically switches to its Receive Mode. Conversely, if while in a neutral state, the CMC recognizes that output is permitted from the HSM Line Slot, the buffer automatically switches to the Transmit Mode.

The CMC, Communications Buffer, and Data Set communicate with each other by the following signals:

CMC-TO-BUFFER	BUFFER-TO-CMC
Select (SEL)	Remote OK (ROK)
CMC Ready (CRDY)	Buffer Status (BSI/BSO)
DD2 Recognized (DD2R)	Buffer Ready (BRDY)
DD1 Recognized (DD1R)	
Parity OK (POK)	

DATA SET-TO-BUFFER	BUFFER-TO-DATA SET
Received Data (RD)	Request Send (RS)
Clear-To-Send (CTS)	Transmit Data (TD)
Supervisory Received Data (SRD)	Supervisory Transmitted Data (STD)

RECEIVE FUNCTION

Initially, an RD signal indicates to the buffer that data is arriving. The buffer collects the data and assembles it into a character. The CMC, as it advances its scan position, sends a SEL to the buffer. If a complete character is not assembled, the CMC advances to its next scan position. If a complete character is present following a SEL signal, the buffer responds with BRDY, BSI, and ROK signals. The CMC then interrogates the I_1 character in the line slot to see if input is permitted. If not, the CMC advances its scan position and the character is not transferred to the CMC. If input is allowed, the CMC responds with a CRDY signal and the character is transferred. The above operations occur on a character-by-character basis until a DD2 is recognized by the CMC. The DD2R signal from the CMC automatically reverts the buffer to its neutral condition.

TRANSMIT FUNCTION

The buffer periodically receives SEL signals from the CMC. If no data is being handled, the buffer responds with BRDY, BSO, and ROK signals. The CMC then examines the I_2 character in the line slot and, if output is not permitted, advances its scan position. If output is permitted, the CMC sends a CRDY signal and the data character to the buffer. An RS signal is now sent by the buffer to the Data Set and, when a CTS signal is returned, the data character is sent to the Data Set and onto the transmission line. The above operations occur on a character-by-character basis until a DD1 or DD2 is recognized by the CMC. The DD2R or DD1R signal from the CMC automatically reverts the buffer to its neutral condition.

AUTOMATIC DISCONNECT

To terminate the line connection when utilizing the Model 6010-22 buffer, a TERM and DD2 signals are transmitted. The DD2R signal from the CMC then causes the line connection to be broken at both the transmitting and receiving stations. The TERM character can be any plugboard selectable data character.

DIALING

Before data may be transferred over the lines, a dialing function must be performed to connect the sending and receiving equipment. (If a private line is used with a point-to-point connection, this may not be necessary.) The dialing of the remote equipment may be done manually or automatically, depending on the type of Data Set utilized. Should 19 seconds elapse after a line connection has been established, and nothing is received from the line, the buffer reverts to its neutral condition.

MANUAL DIALING

When the sending station has data to transmit, the operator dials the remote location by means of a telephone attachment on the Data Set. The operator at the receiving station answers the phone attached to his Data Set and both operators place their respective Data Set in a "DATA" mode by means of a switch. Data transmission may then occur. When data transmission is complete, the operators are notified to hang up their telephones, thus breaking the connection.

The receiving equipment may be placed in an "Unattended" mode by means of a Data Set switch (AUTO). With this switch set, the connection is made automatically without operator intervention at the receiving station.

AUTOMATIC DIALING

An optional dialing feature permits the Transmit mode of the station to use a common carrier Automatic Calling Unit (ACU). This unit is an additional piece of equipment used with the AT&T Data Sets that permits the communication program to automatically dial the remote station when both Data Sets are in the DATA mode.

Automatic dialing message format is as follows:

AAA - 3-digit area code (if required)

TTTTTTT - 7-digit telephone number
The last digit 2^4 must be a "one" bit.

ACCURACY CONTROL

During each CMC selection period, when a buffer is ready, the buffer returns an ROK signal to the CMC unless any of the following error conditions have been detected:

1. *A loss of various signals that indicate that the Data Set is not functioning correctly.

2. *When a no-data timeout occurs. This occurs when there is an interruption of the flow of input data during the data portion of a message.

3. The proper line connection cannot be made when using the Automatic Calling Unit.

4. Receipt of a SRD error signal when using the Reverse Channel Feature: After a line connection is established, the transmitting buffer must recognize a SRD "remote device operable" signal before transmitting. After transmission is in progress, SRD signals are interpreted as error signals by the transmitting buffer. These error signals are generated by the receiving equipment when an input error is recognized.

On error recognition, the buffer inhibits the ROK signal from the CMC on the next SEL only. The buffer then reverts to its neutral condition.

*These conditions activate the buffer error light and the Buffer Interface Unit Buzzer. These Indicators are extinguished either manually, upon re-transmission, upon receiving data, or when the communication line is disconnected.

COMMUNICATIONS BUFFER - MODEL 6012

GENERAL DESCRIPTION

The Communications Buffer is used in conjunction with the CMC to couple a 3301 computer to a standard 3KC "voice grade" communication line, or equivalent, via a Data Set unit. Transmission rates range from 150 cps to 300 cps.

This buffer is used in half duplex operation; it can receive or transmit data but in only one direction at a time. The buffer occupies one CMC scan position and is associated with one HSM line slot.

The transmission line code contains 8 bits per character (6 information bits, 1 parity bit, and 1 control bit). The control bit is added by the buffer to characters received from the computer and deleted from characters which are to be sent to the computer. The transmission line code uses even parity and is the complement of the 3301 computer code. For example, the 3301 character 1000000 is equivalent to the transmission line character 0111111. This code conversion from transmission line code to 3301 code, and vice versa, is handled by hardware.

This buffer may communicate with another Communications Buffer or with the Model 3376 Communications Control Unit, as shown in Figure XX-3.

BUFFER MODELS

The Communications Buffer is offered in the following models:

Model	Dialing	Data Set (*)	Dialed Call Rate	Leased Line Rate
6012-11	Manual	Model 201	250 cps	300 cps
6012-21	Manual	Model 202	150 cps	225 cps
6012-12	Automatic	Model 201	250 cps	Not Used
6012-22	Automatic	Model 202	150 cps	Not Used

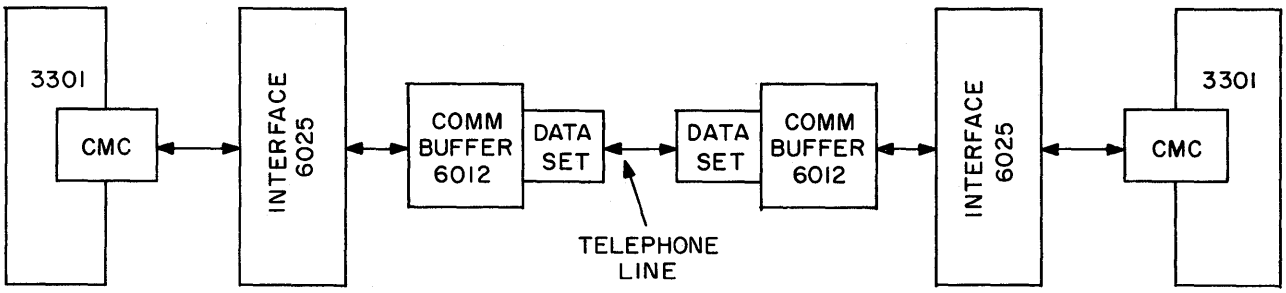
*A common carrier digital Data Set is required to connect the transmission line and buffer. Although AT&T Data Set models are shown in the above chart and described in this section, equivalent Data Sets of other manufacturers may be used. The Model 202 Data Set is asynchronous and accommodates speeds up to the value shown, with minor hardware modification. The Model 201 Data Set is synchronous and operates at a specific speed (sync. supplied by Data Set).

OPERATION

The Communications Buffer may operate in a half duplex mode ready to transmit or receive data. If, while in its neutral state, signals are received from the transmission line, the buffer automatically switches to its Receive mode. Conversely, if while in a neutral state, the CMC recognizes that output is permitted from the HSM line slot, the buffer automatically switches to the Transmit mode.

The CMC, Communications Buffer and Data Set communicate with each other with the following signals:

COMMUNICATION BUFFER TO COMMUNICATION BUFFER



COMMUNICATION BUFFER TO COMMUNICATION CONTROL

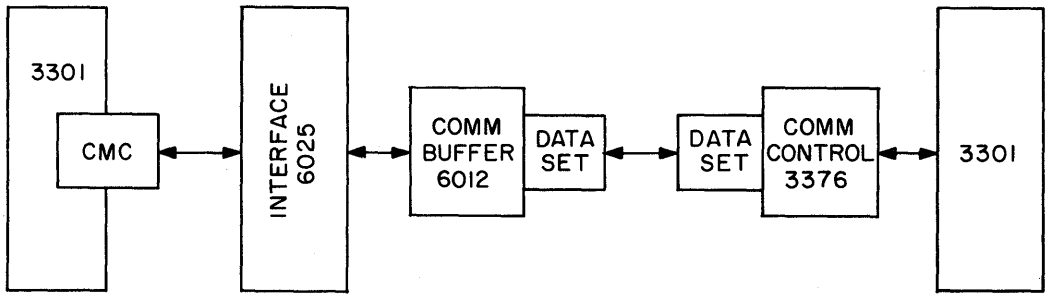


Figure XX-3

CMC-TO-BUFFER	BUFFER-TO-CMC
Select (SEL)	Remote OK (ROK)
CMC Ready (CRDY)	Buffer Status (BSI/BSO)
DD2 Recognized (DD2R)	Buffer Ready (BRDY)
DD1 Recognized (DD1R)	
DATA SET-TO-BUFFER	**BUFFER-TO-DATA SET**
Received Data (RD)	Request Send (RS)
Clear-To-Send (CTS)	
Terminate Transmission (TERM)	

RECEIVE FUNCTION

Initially, a RD signal indicates to the buffer that data is arriving. The buffer collects the data and assembles it into a character. The CMC, as it advances its scan position, sends a SEL to the buffer. If there is no complete character assembled, the buffer does not respond with a BRDY signal, and the CMC advances to its next scan position. If a complete character is present following a SEL signal, the buffer responds with BRDY, BSI, and ROK signals. The CMC then interrogates the I_1 character in the line slot to see if input is permitted. If not, the CMC advances its scan position, and the character is not transferred to the CMC. If input is allowed, the CMC responds with a CRDY signal, and the character is transferred to the CMC.

The above operations occur on a character-by-character basis until a DD2 is recognized by the buffer. The next character received is a Block Parity character which is checked by the buffer. If correct, the DD2 is transferred to the CMC, the CMC sends a DD2R signal to the buffer, and the buffer switches to the Transmit mode. The buffer now transmits an acknowledge signal to the Data Set and line. The next character the CMC delivers to the buffer is a DD1. The DD1R signal returns the buffer to the Receive mode.

TRANSMIT FUNCTION

The buffer periodically receives SEL signals from the CMC. If no data is being handled, the buffer responds with BRDY, BSO, and ROK signals. The CMC then examines the I_2 character in the line slot and, if output is not permitted, advances its scan position. If output is permitted, the CMC sends a CRDY signal and the data character to the buffer. A RS signal is now sent by the buffer to the Data Set and, when a CTS signal is returned, the data character is sent to the Data Set and onto the transmission line.

The above operations continue on a character-by-character basis until a DD2 is transmitted and a DD2R signal is received by the buffer. Block Parity is now transmitted by the buffer, and the buffer switches to a Receive mode. A 1.4 second timer is set, and an acknowledge signal is received by the buffer within this time if no error has occurred.

A 19 second timer is set simultaneously with the 1.4 second timer. If a DD1 is received, and a DD1R signal is returned to the buffer within this time, the buffer is again switched to the Transmit mode.

To return the transmitting and receiving buffers to the neutral conditions, the transmitting computer must send a DD1 to the remote equipment which indicates the end of transmission. The DD1R signal from the CMC turns the buffer into a Receive mode in the transmitting computer and to the Transmit mode in the receiving computer. If TERM and DD1 characters are returned, the line is disconnected, and the buffers revert to their neutral conditions.

BLOCK PARITY

When a message is transmitted by the Communications Buffer, a Block Parity character is generated automatically and transmitted immediately after the DD2 character. The receiving buffer, in turn, develops its own Block Parity character by checking the bit positions of the data as it is received. The receiving buffer then verifies its Block Parity character with the Block Parity character generated by the transmitting buffer.

Block Parity is a single character that contains an indication as to the number of "1" bits (odd or even) that appeared in the 2^0 - 2^5 positions of the characters in the message. Block parity is based on an "even" number of bits. For example, if the number of "1" bits in the 2^0 positions amounted to 43, the 2^0 position of the Block Parity character would be "1".

DIALING

Before data may be transferred over the lines, a dialing function must be performed to connect the sending and receiving equipment. If a private line is used with a point-to-point connection, this may not be necessary. The dialing of the remote equipment may be done manually or automatically.

MANUAL DIALING

When the sending computer has data to transmit, it informs the operator by a printout. The operator then dials the remote location by means of a telephone attachment to the Data Set. The operator at the remote location answers the phone attached to his Data Set, and both operators place their respective Data Sets in a Data mode by means of a switch. The Data mode switch conditions the Data Set to convert the a.c. tone signals into d.c. data signals. Data transmission between computers may then occur. When data transmission is complete, the operators are notified via a printout to hang up their telephones, thus breaking the connection.

The receiving equipment may be placed in an UNATTENDED mode by means of a Data Set switch (AUTO). With this switch set, the connection is made automatically without operator intervention.

AUTOMATIC DIALING

An optional dialing feature permits the Transmit mode of the buffer to use a common carrier Automatic Dialing Unit (ADU). This unit is an additional piece of equipment used with the AT&T Data Set that permits the communication program to automatically dial the remote station when the Data Set is in the Data mode.

Automatic dialing message format:

AAA - 3-digit area code (if required)

TTTTTTT - 7-digit telephone number.
The 2^4 bit of the last digit must be "1".

X - DD2 symbol

ACCURACY CONTROL

During each CMC buffer scan, if the buffer is Ready, it responds to the CMC's Select Signal (SEL) with a Remote OK signal. If the CMC does not receive this Remote OK response, an error condition is indicated. The following conditions will cause the absence of a Remote OK signal from the buffer.

1. If, when using the Automatic Dialing Unit, the receiving station does not answer the call within 40 seconds, or there is a 40 second delay between digits of the phone number as it is received from the CMC.

2. No acknowledge signal has been received from the remote station buffer within 1.4 seconds after the transmitting buffer has sent the Block Parity character.

3. A DD1 is not received from the remote location within 19 seconds after a DD2 was transmitted to the remote station.

4. A parity error is found in a character coming from the transmission line or from the CMC.

5. A Block Parity error is detected for a message received from the transmission line.

6. A DD1 is not received from the CMC within 19 seconds after a DD2 is received.

7. Nothing is received from the line within 19 seconds after a DD1 is transmitted.

8. When receiving data from the transmission line, a "no-data" timeout occurs. That is, more than one character time has elapsed between the completion of one character and the start of the next character.

9. Loss of various signals that indicate that the Data Set is functioning abnormally.

These conditions activate the Interface Unit Buzzer for the duration of the detected condition. After the above action takes place, the buffer returns to its neutral condition. If the buffer is receiving data when the error occurs, further data will not be transferred to the CMC until the start of the next message.

TELEGRAPH POLLING BUFFER, MODEL 6013

GENERAL DESCRIPTION

This buffer unit can transmit and/or receive data in 5-level code over standard telegraph lines at rates of 6, 6.7, 7.5, or 10 characters per second. The buffer may be connected by a telegraph transmission line to standard telegraph transmitting and/or receiving stations or, if a "polling" operation is desired, to an AT&T Out Station Unit, used in an 83B1-2 switching system, or a similar device. Polling is the process by which a remote device on a multi-station line is connected to the processor at the exclusion of the other remote devices.

The basic buffer unit is comprised of two independent buffers. Each of the two buffers occupies one CMC scan position, and each is associated with one CMC line slot. Moreover, each buffer can be used for transmitting and receiving data independently of the other.

OPERATION

The buffer unit is quiescently in a "neutral" state ready to transmit or receive data, but in only one direction at a time. It may operate in one of three modes (Receive only, Transmit only, or Half Duplex). In each mode the CMC, telegraph buffer and remote equipment communicate with each other via the following control signals:

CMC-TO-BUFFER	BUFFER-TO-CMC
Select (SEL)	Buffer Status (BSI/BSO)
CMC Ready (CRDY)	Buffer Ready (BRDY)
	Remote OK (ROK)

REMOTE EQUIPMENT-TO-BUFFER

Receive Data (RD)

Clear-To-Send (CTS)

BUFFER-TO-REMOTE EQUIPMENT

Transmit Data (TD)

RECEIVE FUNCTION

Initially, a RD signal indicates to the buffer unit that data is arriving. The buffer collects the data and assembles it into a character. The CMC, when it advances its scan position to this buffer, sends a SEL signal to the buffer. If there is no complete character assembled, the buffer does not respond with a BRDY signal, and the CMC advances to its next scan position. When a complete character is present following a SEL signal, the buffer responds with BRDY, BSI and ROK signals. The CMC then interrogates the I_1 character in the line slot to see if input is permitted. If not, the CMC advances its scan position, and the character is not transferred to the CMC. If input is allowed, the CMC sends a CRDY signal to the buffer. The character is then transferred to the CMC and from there to HSM. The above operations occur on a character-by-character basis until input data ceases. This is indicated to the buffer by a time span longer than one "character time" during which no data has arrived. The buffer then reverts to its neutral condition.

TRANSMIT FUNCTION

The buffer unit periodically receives SEL signals from the CMC. If no data is being handled by the buffer, it responds with BRDY, BSO, and ROK signals. If the I_2 character in the line slot does not permit output, the CMC advances to its next scan position. Should output be permitted, the CMC sends a CRDY signal and the character to the buffer. The CRDY signal causes the buffer to prohibit input by sending a TD signal to the remote device to indicate data is to be transmitted.

The buffer unit may be wired at installation time to transmit data only when a CTS signal is received from the line. If this signal has not been received when a SEL is received, the BRDY signal is not sent to the CMC, and the CMC advances to its next scan position.

Data is then transmitted by the above operations on a character-by-character basis until line slot output is exhausted. This is indicated to the buffer by a time span longer than one "character time" during which no data has been received from the CMC. The buffer then reverts to a neutral condition.

Data Delimiters are not transmitted by the buffer to the line.

HALF DUPLEX FUNCTION

The buffer unit may be used for sending or receiving (separately). If used in this way, polling of remote devices on multi-station lines is permitted when the proper remote equipment is present. Depending upon the remote controlling equipment, various codes may be transmitted by the 3301 indicating:

1. That certain remote devices may begin to transmit data to the 3301, or

2. That line contact is being made so that the remote devices may receive data from the Processor.

ACCURACY CONTROL

The Remote OK signal is not sent to the CMC with the BRDY and BSI/BSO signals if there is an "open" transmission line condition or a common carrier equipment malfunction. These conditions are indicated by RD and TD signals that continue for at least one "character time". When this occurs, the Interface Unit Buzzer is activated and the buffer inhibits the BRDY signal to the CMC until the condition is corrected. The buffer then returns to its neutral mode.

The Line Monitor Feature is an available installation time option which provides monitor activity on input transmission. A timer is activated every time a DD1R signal is received by the buffer from the CMC. As each character is received following a DD1R, the time is set again. It is deactivated whenever a DD2R signal is received. If time should tun out (one "character time") after receiving a DD1R signal and before receiving a DD2R signal, the ROK signal is not sent to the CMC when the next SEL signal is received. The buffer then immediately reverts to its neutral condition.

ACC_f = Quotient

PR_f = Remainder

PRP is set if the quotient is positive.

PRZ is set if the quotient is zero.

PRN is set if the quotient is negative.

EXAMPLE

Instruction: & 0 4580 4570

HSM Before Execution:

	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87
45	0	0	0	3	2	1	0	0	X	X	0	0	0	0	6	7	8	9

HSM After Execution:

	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87
45	0	0	0	3	2	1	0	0	X	X	2	1	1	4	9	5	3	2

Contents After Execution:

2	1	1	4	9	5	3	2	0	0	0	2	2	8	0	0

Accumulator PR Register

PRP is set.

FLOATING POINT ADD (FLA)

GENERAL DESCRIPTION

This instruction performs floating point decimal addition producing a normalized floating point sum in the Accumulator. Depending upon the conditions specified by the N character, the operands may appear in HSM or in the Accumulator. The sum may be placed in the HSM if it is indicated. The operands are ten characters in length and obey the rules concerning addressing, sign, and overflow as described in the floating point data format description. Mantissa arithmetic may be algebraic or absolute, and rounding of the result is optional.

FORMAT

OPERATION - $

N - as described previously

A ADDRESS - HSM address of the augend and/or sum.

B ADDRESS - HSM address of the addend.

DIRECTION OF OPERATION

Right to left

OUTLINE OF OPERATION

If either mantissa is zero and its exponent is not -99, or if one operand mantissa is not normalized and the other operand is not a floating point zero, the Arithmetic Error Interrupt Indicator is set in the Interrupt Register, and interrupt occurs. If the exponents have like signs, and the B operand exponent is larger (absolute value) than the A operand exponent, an "end around" condition (EAC) occurs. If algebraic arithmetic is indicated, and the mantissas have unlike signs, and the B operand is larger (absolute value) than the A operand, an "end around" condition (EAC) occurs. An exception to this rule is when mantissa alignment is required in which case the EAC is performed during alignment.

Since the result is normalized, overflow can occur only in the exponent. Overflow in the exponent result sets the overflow indicator, the Overflow Interrupt Indicator, and interrupt occurs. The PRI indicators are set in accordance with the sign of the result.

FINAL SETTINGS

$A_f = A_i$.

$B_f = B_i$.

EXP_f = Exponent Result.

PRP is set if the sum is positive.

PRZ is set if the sum is zero.

PRN is set if the sum is negative.

EXAMPLE

Instruction: $ 1 4609 4619

HSM Before Execution:

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19
46	4	6	7	0	3	4	6	9	0	4	3	4	5	6	7	3	4	5	0	1

HSM After Execution:

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19
46	4	6	7	3	8	0	3	6	0	4	3	4	5	6	7	3	4	5	0	1

Accumulator After Execution:

4	6	7	3	8	0	3	6

Exponent Register After Execution:

0	4

PRP is set.

FLOATING POINT SUBTRACT (FLS)

GENERAL DESCRIPTION

This instruction performs floating point decimal subtraction producing a normalized floating point difference in the Accumulator. Depending upon the conditions specified by the N Character, the operands may appear in HSM or in the Accumulator. The difference may be placed in HSM if it is indicated. The operands are ten characters in length and obey the rules concerning addressing, sign, and overflow as described in the floating point data format. Mantissa arithmetic may be algebraic or absolute, and rounding of the result is optional.

FORMAT

OPERATION - :

N - as described previously.

A ADDRESS - HSM address of the minuend and/or difference.

B ADDRESS - HSM address of the subtrahend.

DIRECTION OF OPERATION

Right to left.

OUTLINE OF OPERATION

If either mantissa is zero and its exponent is not -99, or if one operand mantissa is not normalized and the other operand is not a floating point zero, the Arithmetic Error Interrupt Indicator is set, and interrupt occurs.

If the exponents have like signs, and the B operand exponent is larger (absolute value) than the A operand exponent, an "end around" condition (EAC) occurs. If the mantissas have like signs, and the B operand is larger (absolute value) than the A operand, an "end around" condition (EAC) occurs. An exception to this rule is when mantissa alignment is required in which case the EAC is performed during alignment.

Since the result is normalized, overflow can occur only in the exponent. Overflow in the exponent result sets the Overflow Indicator, the Overflow Interrupt Indicator, and interrupt occurs. The PRI indicators are set in accordance with the sign of the result.

FINAL SETTINGS

$A_f = A_i$.

$B_f = B_i$.

EXP_f = Exponent Result.

PRP is set if the difference is positive.

PRZ is set if the difference is zero.

PRN is set if the difference is negative.

EXAMPLE

Instruction: : 9 5830 5820

HSM Before Execution:

	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39
58	1	3	6	7	3	2	0	0	0	K	8	7	3	2	1	0	1	3	0	3

HSM After Execution:

	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39
58	1	3	6	7	3	2	0	0	0	K	8	7	3	2	1	0	1	3	0	3

Accumulator After Execution:

8	7	3	2	0	8	7	6

Exponent Register After Execution:

0	3

PRP is set.

FLOATING POINT MULTIPLY (FLM)

GENERAL DESCRIPTION

This instruction performs floating point decimal multiplication producing a normalized floating point product in the Accumulator. Depending upon the conditions specified by the N character, the operands may appear in HSM or in the Accumulator. The product may be placed in HSM if it is indicated. The operands are ten characters in length and obey the rules concerning addressing and sign as described in the floating point data format description. The product, when stored in memory, will contain 8 digits. Mantissa arithmetic may be algebraic or absolute, and rounding of the result is optional.

FORMAT

OPERATION - "

N - as described previously.

A ADDRESS - HSM address of the multiplicand and/or product.

B ADDRESS - HSM address of the multiplier.

DIRECTION OF OPERATION

Right to left.

OUTLINE OF OPERATION

If a mantissa is zero and its exponent is not -99, or if either operand mantissa is not normalized, the Arithmetic Error Interrupt Indicator is set, and interrupt occurs. If the exponent signs are unlike, and the B operand exponent is larger, an "End Around" condition (EAC) occurs. If there is an exponent overflow, the Overflow Indicator is set, the Overflow Interrupt Indicator is set, and interrupt occurs. The PRI's are set in accordance with the sign of the result.

FINAL SETTINGS

$A_f = A_i$.

$B_f = B_i$.

EXP_f = Exponent Result.

PRP is set if the product is positive.

PRZ is set if the product is zero.

PRN is set if the product is negative.

EXAMPLE

Instruction: " 0 6739 6749

HSM Before Execution:

	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49
67	6	3	1	5	6	7	8	9	0	7	3	4	5	6	7	8	9	6	0	2

HSM After Execution:

	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49
67	2	1	8	3	1	9	7	3	0	9	3	4	5	6	7	8	9	6	0	2

Contents After Execution:

2	1	8	3	1	9	7	3	1	3	8	4	5	9	4	4

Accumulator PR Register

PRP is set.

FLOATING POINT DIVIDE (FLD)

GENERAL DESCRIPTION

This instruction performs floating point decimal division producing a normalized floating point quotient in the Accumulator. Depending upon the conditions specified by the N character, the operands may appear in HSM or in the Accumulator. The quotient may be placed in HSM if it is indicated. The operands are ten characters in length and obey the rules concerning addressing and sign as described in the floating point data format description. Mantissa arithmetic may be algebraic or absolute, and rounding of the result is optional.

FORMAT

OPERATION - /

N - as described previously.

A ADDRESS - HSM address of the dividend and/or quotient.

B ADDRESS - HSM address of the divisor.

DIRECTION OF OPERATION

Right to left.

OUTLINE OF OPERATION

If either mantissa is zero and its exponent is not -99, or if the divisor (B operand) is zero, the Arithmetic Error Interrupt Indicator is set, and interrupt occurs. If the exponent signs are alike and the magnitude of the exponent of the B operand is larger, an "End Around" condition (EAC) occurs. If the exponent overflows, the Overflow Indicator is set, the Overflow Interrupt Indicator is set, and interrupt occurs. Overflow in either operand is ignored. The PRI's are set in accordance with the result.

FINAL SETTINGS

$A_f = A_i$.

$B_f = B_i$.

EXP_f = Exponent Result.

PRP is set if the quotient is positive.

PRZ is set if the quotient is zero.

PRN is set if the quotient is negative.

EXAMPLE

Instruction: / 0 1009 1019

HSM Before Execution:

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19
10	8	3	4	3	2	1	0	1	0	2	3	6	2	0	1	3	2	2	0	1

HSM After Execution:

	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19
10	2	3	0	4	6	7	0	0	0	2	3	6	2	0	1	3	2	2	0	1

PRP is set.

STORE ACCUMULATOR (SAC)

GENERAL DESCRIPTION

This instruction places the contents of the Accumulator, the PR Register and the Exponent Register, as designated by the N character, into HSM. The sign is stored.

FORMAT

OPERATION - Z

N

2^3 = 1 Indicates Accumulator and the PR Register (16 characters) are to be stored.
= 0 Ignored (unless PR Register is to be stored).

2^4 = 1 Indicates both Accumulator and exponent (10 characters) are to be stored as a floating point word.
= 0 Ignored (unless PR Register is to be stored).

2^5 = 1 Indicates Accumulator (8 characters) is to be stored.
= 0 Indicates the PR Register is to be stored. (2^3 and 2^4 must also be "zero").

If the 2^3, 2^4, and 2^5 are erroneously contradictory, the following priority is followed: 2^3 bit overrides 2^4 and 2^5; 2^4 overrides 2^5.

A ADDRESS - HSM address where designated portion is to be stored.

B ADDRESS - Zero (0000). Not to be used by programming.

DIRECTION OF OPERATION

Right to left.

OUTLINE OF OPERATION

The instruction stores the contents of the Accumulator, PR Register, and Exponent Register starting at the HSM address designated by the A Address. The N Character is examined to determine which data is to be stored.

If the 2^3 bit is one, the Accumulator and PR Register characters are stored. The eight characters of the PR Register are stored in the leftmost eight positions of the decade specified by the A Address. The eight characters of the Accumulator are stored in the leftmost eight positions of the decade preceding the decade specified by A.

If the 2^4 bit is one, the Accumulator (eight characters) and Exponent Register (two characters) are stored as a floating point word. If the 2^5 bit is one, the Accumulator is stored. If bits (2^3, 2^4, and 2^5) are all zero, the PR Register (eight characters) is stored.

FINAL SETTINGS

$A_f = A_i - 10$, if Accumulator is stored or if PR Register is stored.

$A_f = A_i - 10$, if Accumulator and Exponent Register are stored.

$A_f = A_i - 20$, if Accumulator and PR Register are stored.

$B_f = B_i$

EXAMPLE

Instruction: Z 8 4570 0000

HSM Before Execution:

	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77
45	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

Contents Before Execution:

1	8	2	9	3	0	4	1	5	2	6	3	7	4	8	1

Accumulator PR Register

HSM After Execution:

	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77
45	1	8	2	9	3	0	4	1	Z	Z	5	2	6	3	7	4	8	1

A_f = 4550

B_f = 0000

SHIFT ACCUMULATOR (SHA)

GENERAL DESCRIPTION

This instruction shifts the Accumulator and the PR Register a specified number of times in either direction. In most cases, eight places will be the maximum shifts desired since this number permits the shifting of the entire contents of the Accumulator or PR Register. In rare cases where more than eight places are desired to be shifted, up to 15 places may be shifted by indicating the number of places in binary notation (use 3301 N Count). Shifts are performed one character at a time. Characters are shifted off the end of the Accumulator and lost, while vacated positions on the other end are filled with zeros. The sign positions in the Accumulator and PR Register are not affected by shifting.

FORMAT

OPERATION - = (Equals)

N

2^3 = 1 Couple Accumulator and the PR Register (shift as one unit)
= 0 Uncouple Accumulator and the PR Register (shift separately)

2^4 = 1 Shift Right
= 0 Shift Left

2^5 = 1 Shift Accumulator
= 0 Shift PR Register

2^3 = 1 and 2^5 = 1, contents of PR Register, including sign, are shifted into Accumulator.

A ADDRESS - Zero (0000). Not to be used by programming.

B ADDRESS - B_0, B_1, B_2 - Zero (000). Not to be used by programming.

B_3 = Number of shifts.

DIRECTION OF OPERATION

As specified by the 2^4 bit of the N character.

OUTLINE OF OPERATION

B_3 of the B Address is transferred to a 4 bit binary Counter where the number of shifts are tallied. The N character is examined, and if 2^5 bit is a "one" and the 2^3 bit is a "one", the quantity in the Counter is ignored, and the contents of the PR Register including sign are moved to the Accumulator. The instruction then terminates. If 2^3 bit of N is "one" and 2^5 bit of N is "zero", the Accumulator and PR Register are coupled and shifted as one unit. If the 2^3 bit of N is "zero", the Accumulator and PR Register are shifted separately, the 2^5 bit of N determining which of the two is to be shifted. When the 2^5 bit of N is "one", the Accumulator is indicated. When the 2^5 bit of N is "zero", the PR Register is indicated. The Counter is reduced by one in each shift status level. If the 2^4 bit of N is "one", all shifts are made to the

right. If the 2^4 bit of N is "zero", all shifts are made to the left. When the counter reaches zero, the instruction is terminated.

FINAL SETTINGS

$A_f = A_i$

$B_f = B_i$

TIMING

Instruction times vary due to the numerous options, conditions, and operand locations that are available. Table XXII-2 reflects the base execution times for the instructions associated with the High Speed Arithmetic Unit. Variances are depicted in Table XXII-3 and must be added, where applicable, to the figures in Table XXII-2 to develop total instruction times. Table XXII-4 contains a timing summary for fixed and floating point operations.

Execution of fixed point and floating point functions operate with a time pulse interval of 147 nanoseconds. A combination of either 4 (.588 msec.) or 5 (.735 msec.) time pulses comprise the High Speed Arithmetic Unit status levels and do not require any access of High Speed memory. Input/Output instructions may use all memory cycles concurrently without delaying these operations. The high speed arithmetic instruction will synchronize with HSM at the beginning of the next memory cycle after execution. This time will vary from 0 to 1 machine cycle (1.93 msec).

Table XXII-2. Base Execution Times

INSTRUCTION	TIME (In Microseconds)
Fixed Point Add	.735
Fixed Point Subtract	.735
Fixed Point Multiply	14.48 (avg.)
Fixed Point Divide	29.99 (avg.)
Floating Point Add (Mantissa only)	.735
Floating Point Subtract (Mantissa only)	.735
Floating Point Multiply (Mantissa only)	14.48 (avg.)
Floating Point Divide (Mantissa only)	
Divisor Larger than Dividend	29.99 (avg.)
Divisor Smaller than Dividend	28.52 (avg.)
Shift Accumulator	.588N + 1.50
Shift PR Register	.588N + 2.088
Shift Accumulator & PR Register Coupled	
Right Shift	1.176N + 2.088
Left Shift	1.176N + 1.50
Shift PR to Accumulator	0.00
Store Accumulator	3.00
Store PR Register	3.00
Store Accumulator and PR Register	6.00
Store Accumulator and Exponent Register	3.00

N = Number of characters shifted

Table XXII-3. Timing Additions

ADDITIONAL TIME FACTORS	TIME (In Microseconds)
Instruction access	1.93
Fetching of operand from Accumulator	0.00
Storing result in Accumulator	0.00
Fetching of fixed point operand from HSM	1.93
Storing of fixed point result to HSM	3.00
Fetching of floating point operand from HSM	3.43
Storing of floating point result to HSM	3.00
Indirect addressing	3.00
Address modification per operand	1.93
Alignment of floating point operand	
Floating point add	.588N
Floating point subtract	.588(N-1) + .735
Normalization of floating point add or subtract	
1 character to be normalized and rounded	.735
1 character to be normalized - no rounding	.588
> 1 character to be normalized	.588N
Normalization of floating point multiply	.588
Normalization of floating point divide	.588
Rounding	
Fixed multiply and floating (add, subtract, multiply)	.735
Rounding	
Fixed divide and floating divide	2.793
End-around-condition	
Fixed (add and subtract) and floating (add and subtract)	.735
End-around-condition for exponent arithmetic	0.00
Exponent arithmetic	1.50

N = number of characters shifted.

Normalization and rounding in floating point add, floating point subtract, and floating point multiply executions occur simultaneously. If both are performed in the same operation, the longer time applies.

Table XXII-4. Timing Summary (Minimum time in microseconds)

OPERATION	FIXED POINT			FLOATING POINT		
	ADD/SUBT	MPY	DIV	ADD/SUBT	MPY	DIV
A ° B → ACC	5.53	20.27	35.78	9.53	28.27	37.31
A ° B → ACC, A	8.53	23.27	38.75	12.53	26.27	40.31
A (or B) • ACC → ACC	4.6	18.34	33.85	6.1	19.84	33.88
A (or B) • ACC → ACC, A	7.6	21.34	36.85	9.10	22.84	36.88
ACC • ACC → ACC	2.67	16.41	31.92	2.67	16.41	30.45
ACC • ACC → ACC, A	5.67	19.41	34.92	5.67	19.41	33.45

The above times include instruction access, fetching of operands (when applicable), and execution timing only.

SIMO 3
MODE

XXIII SIMO 3 MODE

GENERAL DESCRIPTION

Simo 3 provides a third simultaneous I/O mode as an option on the RCA 3301 System. Its use is restricted to Magnetic Tape and Random Access devices. Specific devices which may utilize Simo 3 mode are:

Model 581 Magnetic Tape Station

Model 582 Magnetic Tape Station

Model 681 Magnetic Tape Station

Model 3484 Magnetic Tape Station

Model 3485 Magnetic Tape Station

Model 3464 Data Drum Memory

If a Simo 3 instruction is directed to any device other than above, it will result in a Busy or Inoperable interrupt. The five input/output instructions utilized are:

OP Code	Instruction Name	Mnemonic
B	Control Device Simo 3	(CD3)
D	Read Forward Simo 3	(RF3)
F	Read Reverse Simo 3	(RR3)
H	Write Simo 3	(WR3)
%	Erase Simo 3	(ER3)

Format for these instructions will be identical to the input/output instructions for Simo 1 and Simo 2 Modes.

PROCESSOR ADDITIONS

The inclusion of Simo 3 into an RCA 3301 System involves additions and modifications to the following areas of the Computer: (1) Registers, (2) Micro Magnetic Memory, (3) Interrupt Indicators, and (4) Instructions.

REGISTERS

Additional registers used by Simo Mode 3 are:

Simultaneous Operation Register 3(SOR3) - Holds the operation code.

F Register - Receives four-character A Address.

G Register - Receives four-character B Address.

MICRO MAGNETIC MEMORY

The F Register, G Register, and the last Simo 3 instruction accessed are stored in Micro Magnetic Memory at the following locations:

Location Symbol	MMM Contents
>	F Register
<	G Register
$	Op and N
[	A Address
*	B Address

These additional Micro Magnetic Memory locations are addressable through the Load Register and Store Register instructions.

INTERRUPT INDICATORS

Interrupt Indicators for Simo 3 are:

Symbol	Condition
12	Simo 3 Terminated Abnormally
15	Simo 3 Terminated Normally

These indicators may be addressed (by symbol) with the Scan Interrupt instruction.

MAGNETIC TAPE CONTROL MODULES

In Magnetic Tape Control Modules the two channels are shared by the three Simo Modes as shown in Figure XXIII-1. Simo 1 instructions execute through switch α, Simo 2 instructions through switch β and Simo 3 instructions will execute through α or β depending upon which switch is available. If both switches are available at the same time, Simo 3 will always select α.

It is possible to program in such a manner as to get a Busy or Inoperable interrupt from the Tape Control Module with only a single Tape Station operating. For example, if a Simo 3 instruction is utilizing switch α, a Simo 1 instruction to the same Control Module would cause Busy or Inoperable interrupt. However, a Simo 2 instruction would execute.

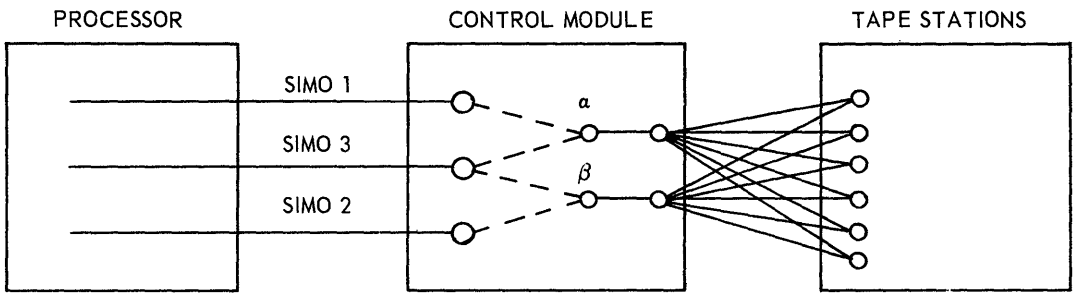


Figure XXIII-1. Functional Diagram of 2x6 Dual Tape Channel

INSTRUCTIONS

The Test Device instruction to the Magnetic Tape Control Module operates in the following manner:

If the A_3 character is "zero", then the device indicators only are being tested. The device indicators are individually picked by the bits of the A_0 character. To execute a TDV instruction to device indicators, it is required that the Tape Station, specified by the N character, be connected to the Processor through the Control switch. If the Tape Station is connected to the switch, the sense will be performed (operating or not). If the Tape Station is not busy, then it will be connected and the sense performed. The test cannot be executed if the Tape Station specified is not or cannot be connected at this time. If the test cannot be performed, the instruction will terminate immediately with a Busy or Inoperable interrupt.

If the A_3 character is not "zero", then the mode indicators only are being tested. The mode indicators are individually picked by the bits of the A_1 character. To execute a TDV instruction to mode indicators, it is not required that the Tape Station, specified by the N character, be connected to the Processor through the Control switch. The N character will, in effect, select the Control Module (each device on the Control Module would select the same Control Module).

To facilitate use of the Simo 3 Mode, the ability to test via the TDV instruction the α or β path of the Magnetic Tape Control Module switch is provided in the following manner:

A_1 Character	A_3 Character	Test Function
$2^4 = 1$	$2^0 = 1$	Is α switch busy?
$2^4 = 1$	$2^1 = 1$	Is β switch busy?

The TDV instruction includes the ability to sense "mode indicators" for Simo 3. The indicators are the same as Simo 1 and 2 with the exception of the switch busy test. This sensible condition does not exist in the Simo 3 Mode indicators. To specify Simo 3 Mode indicators the following test function is provided:

Character	Bit Position	Symbol	Test Function
A_3	$2^2 = 1$	4	Simo 3 Mode

The Conditional Transfer of Control (CTC) instruction is modified to include testing the condition of Simo 3 Mode. The N character is K. Implementation is identical to that of the Simo 1 and Simo 2 modes. The Indicator for Simo 3 is not sensible by the CTC instruction but can be sensed by the Test Device instruction.

XXIV DIGITAL CLOCK

GENERAL DESCRIPTION

The Digital Clock is a peripheral device which transmits, upon program demand, the time of day to High Speed Memory. The output of the Digital Clock is six digits representing tens and unit hours, minutes and seconds and is based upon 24 hour time.

Each output digit consists of four bits. The output of the clock to the Control is bit parallel, digital serial. When a "Read Clock" instruction is accessed, the clock presents the six digits by diad to the Control.

Time settings and adjustments are made by dialing the desired time to the nearest second on a set of six switches. A "Hold Button" gives the facility to manually stop and set the Digital Clock.

CONTROL

The Digital Clock does not have its own Control but utilizes the Control of the Console Typewriter. The Console Typewriter Control modification required for this logic sharing is identified as Special Feature 168. The Control is responsible for:

1. Transferring the time indication to HSM.

2. Code translation (four to six-bit plus parity).

3. Providing program sensible indicators for the busy and operable conditions.

INSTRUCTIONS

The Control shares the logic of the Console Typewriter which contains the necessary logic to initiate, control, and provide terminal information for the following instructions:

Read Forward Simo 1	(RF1)
Read Forward Simo 2	(RF2)
Test Device	(TDV)

Instructions are presented by function under these headings: (1) Reading the Clock, and (2) Testing the Clock.

READING THE CLOCK

GENERAL DESCRIPTION

The Read Forward Simo 1 (RF1) or Read Forward Simo 2 (RF2) instruction performs this function. A time representation of six digits are entered into HSM through use of these instructions. The time, 5:15:32 P.M., is represented as 17:15:32.

FORMAT

OPERATION - 4 (RF1) or 5 (RF2)

N - Z (Denotes Digital Clock)

A ADDRESS - HSM location to receive the first digit. (Must be an even location.)

B ADDRESS - Zero (0000). Not to be used by programming.

DIRECTION OF OPERATION

Digits are transferred into HSM left to right.

OUTLINE OF OPERATION

When a Read instruction is accessed, the Clock Control will interrogate the N character to determine if the instruction is addressed to the Digital Clock. If such is the case, the Control informs the Clock that a read out of the time has been requested. The two four-bit code pertaining to the hours are converted into two six-bit plus parity codes and are transmitted by diad to the Processor. This cycle is repeated three times until all six digits have been transmitted.

FINAL SETTINGS

S_f or C_f = HSM location one to the right of the last digit transferred.

T_f or E_f = B_i

EXAMPLE

Instruction: 4 Z 0600 0000

HSM Before Execution:

0600	0601	0602	0603	0604	0605
0	0	0	0	0	0

Time 8:57:23 A.M.

HSM After Execution:

0600	0601	0602	0603	0604	0605
0	8	5	7	2	3

Final Settings: C_f = 0606 E_f = 0000

GENERAL DESCRIPTION

The Test Device (TDV) instruction tests the desired status of the Digital Clock. Control is transferred if the condition or conditions tested for are present.

FORMAT

OPERATION - S

N - Z (denotes Digital Clock)

A ADDRESS - Specifies the test to be performed as follows:

Character	Bit Position	Symbol	Test
A_0	$2^0 = 1$	1	Is Digital Clock operable?
A_0	$2^1 = 1$	2	Is Digital Clock busy?

Unused characters are zero and not to be used by programming.

B ADDRESS - HSM location of the next instruction to be executed if the condition(s) being tested is (are) present.

SPECIAL CONDITIONS

STP is performed if the condition(s) specified by the A Address is (are) present.

FINAL SETTINGS

$A_f = A_i$

$B_f = B_i$

TIMING

The output rate of the Digital Clock is 33,333 digits per second. When the Clock is undergoing a time change, it will be inaccessible for approximately 70 microseconds.

ACCURACY CONTROL

Since there exists a common Control for the Console Typewriter and Digital Clock, it will be impossible to read the Clock if the Control is servicing the Console Typewriter. The Control Module "Busy" indicator will be set when the Control is servicing either the Typewriter or the Clock. Subsequently, addressed instructions to the Control will be subject to a Busy or Inoperable interrupt if the Control is busy servicing either device. The Control is in a Busy status during time changes.

XXV SWITCHES

(To Be Supplied)

MODEL 347 SWITCH

GENERAL DESCRIPTION

The Tape Switching Unit (Model 347) is a manually controlled device, capable of switching six Tape Station trunks to any one of six machine trunks.

Data and control signals are transferred to and from the machine trunk through the switching unit to the Tape Station trunk.

Switching between the machine trunks and the Tape Station trunks is accomplished through the Control unit. This unit consists of one row of six numerical displays and three rows of six switches per row (See Figure XXV-1). The first row of switches controls the machine trunk selection, the second row provides the disconnect facilities on a perconnection basis, and the third row controls the tape trunk selection. A power ON-OFF switch is provided in the device. The tape switching unit includes a prewired rack which permits additional switching relays (K-347 Expansion Kits) to be added. Its basic 1 x 2 switching capacity can be expanded up to a 6 x 6 switch. The expansion kits can also be installed to form independent switching combinations such as a 2 x 3 and 2 x 2 unit or a 4 x 4 and 2 x 2 unit.

OPERATION

The numerical displays and machine trunks operate as a block.

Pressing a particular machine trunk switch selects that trunk. A Tape Station may be connected to the selected machine trunk by pressing the desired Tape Station selection switch while holding the machine trunk switch pressed. The number of the Tape Station in operation appears on the numerical display over the machine trunk in use. The connection between any Tape Station and machine device may be broken by pressing the Disconnect (◇) Switch under the machine trunk in use. Six machine trunks and six Tape Stations may be used at the same time.

ACCURACY CONTROL

Interlocks are provided to prevent multiple connections between equipment or device trunks. Under certain conditions it is possible to switch devices during a data transfer without an error condition being indicated. Therefore, to prevent loss of data, it is imperative that switching be accomplished only when data is not being transferred between the devices connected through the switch points being controlled.

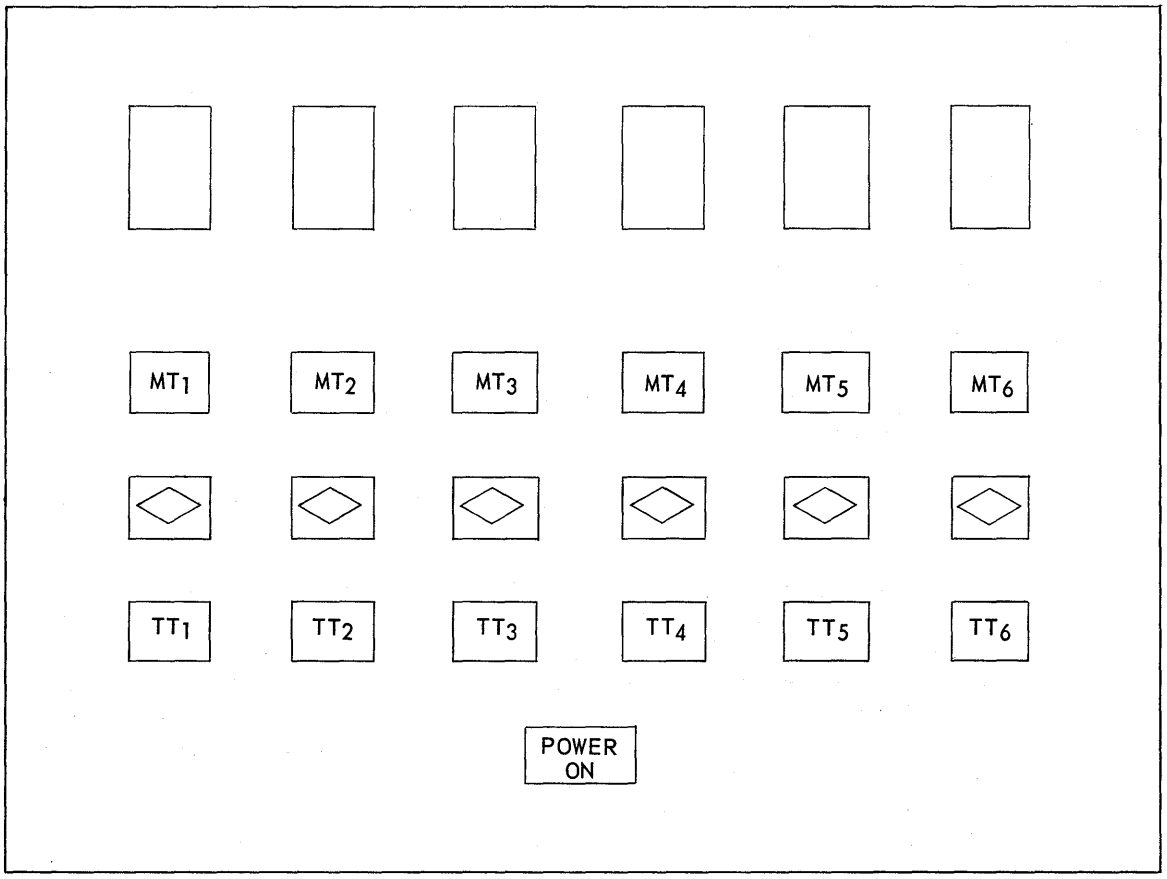


FIGURE XXV-1. CONTROL PANEL

(To Be Supplied)

MODEL 3446 SWITCH

GENERAL DESCRIPTION

The Passive Switch (Model 3446) is a means for making alternate inter-connections between one "User Trunk" and two peripheral devices or two "User Trunks" and one peripheral device (1x2 or 2x1).

In on-line systems, it may be used to switch standby equipment in or out, or from one processor to another.

RCA Tape Stations, CMC-Buffers, Magnetic Drum Units and Random Access Computer Equipment are generally within this device class.

There are two basic versions of the Passive Switch Modules. The 1x2 (Model 3466-1) and 2x2 (Model 3446-2). A 1x2 is not expandable into a 2x2 type of switch.

OPERATION

The Operator Panel consists of a Manual/Remote Switch indicator. This switch is capable of being controlled from a remote point, and it inter-connects the following devices to one control as a 1x2 switch or two control units (Processors) and one device as a 2x1 switch. It can be connected between the following:

Tape Stations and Control

581 and 3383
582 and 3383
681 and 3383
3484 and 3384
3485 and 3385

Random Access Computer Equipment and Control

3488 and 3388

Magnetic Drum Storage and Control

3464 and 3364

Paper Tape Devices and Control

321 and 3321
322 and 3321
331 and 3321

Card Equipment and Control

329 and 3329

Communication Equipment

CMC and BIU (Model 6025)

ACCURACY CONTROL

The Passive Switch Module does not affect standard programming for any device with which it is used, however, to prevent loss of data, switching should only be accomplished when data is not being transferred between the devices connected through the switch point being controlled.

Proper cable lengths have to be surveyed before installing this switch.

APPENDICES

APPENDIX I - GLOSSARY OF TERMS

Access Time. A time interval which is characteristic of a storage device, and is essentially a measure of the time required to communicate with that device. The time interval between (1) the instant at which information is called for from storage and the instant at which it is delivered or (2) the instant at which information is ready for storage and the instant at which it is stored.

Address (noun). An expression, which designates a particular location in a storage or memory device or other source or destination of information.

Absolute Address (Direct Address). The specific label assigned by the machine designer to a particular storage location. To code in absolute means to write a sequence of instructions in a computer code.

Indirect Address. The address of four consecutive memory locations whose contents contain the address of another memory location to be accessed.

Instruction Address. (Line Number, Location). An expression used in coding to denote the address of a stored instruction. NOT a part of the instruction itself.

Symbolic Address. A label expressed in a pseudo-code. To code using symbolic addresses implies that the sequence of instructions must be translated into absolute before being executed by a computer. Relative addresses are those symbolic addresses which are translated into absolute by sequencing from some specific "reference" address.

Bails. A mechanical device used to raise a group of 8 cards, one of which will be extracted to the capstan on the 3488 Random Access Computer Equipment.

Batch. Several groups of items in sequence, each separated by a sentinel.

Beginning of Tape Control (BTC). A "window" placed at the beginning of a magnetic tape, where recording of data is not possible and which can be sensed photo-electrically.

Binary Code. A code composed of a combination of entities each of which can assume one of two possible states. Each entity must be identifiable in time or space.

Binary Notation. A system of positional notation in which the digits are coefficients of powers of the base two.

Binary-to-Decimal Conversion. The mathematical process of converting a binary number to the equivalent quantity in decimal notation. For example: 001=1, 010=2, 011=3, 100=4, 101=5, etc.

Bit. A single binary digit having a value of either zero or one. The word is a contraction of "Binary Digit".

Block. A group of consecutive data considered or transferred as a unit, particularly with reference to input and output. On magnetic and paper tape a block is a group of at least three characters preceded and followed by an unrecorded area called a "gap".

Buffer. A storage device used to compensate for a difference in rate of flow of information or in time of occurrence of events when transmitting information from one device to another, as from an input device to the High Speed Memory, or from the High Speed Memory to an output device.

Bus. A main circuit, channel, or path for the transfer of information.

Capstan. A revolving cylinder, with friction belts, on which a 3488 card is placed for reading/writing.

Card. Any card adapted for being punched in an intelligent array of holes for the storage of information.

Card Column. One of a number of columns in a card into which information is entered.

Card Feed. A mechanism which moves cards one by one into a processing device.

Card Punch. A mechanism which punches cards. An automatic card punch punches cards according to a stored program.

Card Reader. A mechanism that reproduces the information on cards in another form, usually electrical signals.

Card Stacker. A mechanism that stacks cards after they have passed through a machine.

Carry. (1) A condition occurring during addition when the sum of two digits in the same column equals or exceeds the base number. (2) The digit to be added to the next higher column.

Character. One of a set of elementary symbols which may be arranged in ordered aggregates to express information. These include numerics, alphabetics, punctuation marks, control symbols and any other symbols which a computer may read, store or write.

Code (noun). A system of symbols and rules for their use in representing information. A language.

Operation Code. The code representing an operation (add, subtract, transfer, etc.) built into the hardware of the computer.

Complement (noun). A quantity which is derived from a given computer quantity by the following rules:

a. Complement on n (as in tens complement). Subtract each digit of the given quantity from n-1, add unity to the least significant digit, and perform all resultant carries.

b. Complement on n-1 (as in nines complement). Subtract each digit of the given quantity from n-1.

c. Complement on Binary Digits (ones complement) is via inversion (i.e., 1 to 0, 0 to 1).

Constant. A number is said to be a constant if it has the same value under all conditions. For example, in the formula (area of a circle) = Pi (radius)^2, Pi is a constant, equal to 3.14159 which applies to all circles.

Control Symbol. A character used to indicate the beginning or the end of unit of data (item, record, file, etc.).

Counter. A device (register or storage location) for storing integers, permitting these integers to be increased or decreased by units or by an arbitrary integer, and capable of being reset to zero or to an arbitrary integer.

Criterion (Key). A group of characters, usually comprising an item, used to identify a record.

CTC. Conditional transfer of control.

Decade. A unit consisting of 10 consecutive HSM locations beginning at XXX0 and ending with XXX9.

Diad. A unit consisting of two consecutive HSM locations. Each diad begins with an "even" decimal address and ends with the next consecutive "odd" address.

Digit. One of the n symbols of integral value ranging from 0 to n-1, inclusive, in a scale numbering of base n. Examples of various types of digits are: Binary Digits are 0 to 1; Octal Digits are 0 through 7; Decimal Digits are 0 through 9.

Direct Address. The specific label assigned by the machine designer to a particular storage location. Synonymous with Absolute Address.

EB. End of Block Symbol.

ED. End of Data Symbol. A symbol which the computer interprets as meaning there is no data following the symbol. For example, the last character on a magnetic tape is the End Data Symbol.

Edit. To rearrange information. Editing may involve the deletion of unwanted data, the selection of pertinent data, the insertion of invariant symbols such as page numbers and typewriter characters, and the application of standard processes such as zero suppression.

EDP. Electronic Data Processing.

EF. End of File Symbol. A symbol which the computer interprets as meaning all Data pertaining to a file precedes the symbol. For example, the last character in a file is the End File Symbol.

EI. End of Information Symbol.

End-Around-Carry. A carry in which the overflow from the column of highest order is added to the column of lowest order.

End of Tape Warning (ETW). A warning generated by a metal strip or window on the tape indicating that the end of usable tape is near.

Erase.
1. To expunge, wipe out, or destroy stored information, usually without destroying the storage media.
2. To replace all the binary digits in a storage cell by binary zeros.

f. Used as subscript to denote final.

Field. A set of one or more characters which is treated as a whole; a unit of information.

File. The complete group of records to be processed. For example, the data relative to one employee in a payroll application is a record; the total records for all employees constitute a file.

Flip-Flop. A device having two stable states and two output terminals (or types of input signals), each of which corresponds to one of the two states. (The two states may be considered as corresponding to "off" and "on" or to binary 0 and 1.) The circuit remains in either state until it is caused to change to the other state by application of the corresponding signal.

Gap. An unrecorded area on magnetic or paper tape. The gap is used to separate records, blocks or other units of data.

Hardware. The physical equipment such as the mechanical, magnetic, electrical and electronic devices from which a computer is fabricated; the material forming a computer, as distinct from routines.

High Speed Memory (HSM). Magnetic core storage in the Computer. See also Storage.

High Speed Memory (HSM) Location. A unit of magnetic core storage (High Speed Memory) which can store (hold, remember) one character.

i. Used as subscript to denote initial.

Indirect Address. The address of a memory location whose contents contain the address of another memory location to be accessed.

Input. (1) Information transferred into the computer. (2) The device by means of which information is fed into the computer.

Instruction. Information which conveys to a machine where the operands are obtained, what operations to perform, what to do with the result, and sometimes, where to obtain the next instruction.

Instruction Access. The process of bringing an instruction out of HSM and placing the components into the proper registers for execution.

Instruction Code. An artificial language for expressing the instruction to be carried out by a machine.

Interrupt. An automatic operation performed by computer hardware that causes a temporary break in the operating sequence enabling software to service selected functions. Machine conditions are automatically stored at the time of interrupt and restored upon return after interrupt.

Item. An item consists of such characters as are necessary to specify a particular unit of information (a numerical quantity, an alphabetic name, a street address, a stock number, etc.). In many cases an item is preceded by a symbol to define the beginning of each item.

Item Separator Symbol (ISS). Control symbol which may be used to designate the beginning of an item.

Justify. Shift an operand to effect right or left columnar alignment.

KC. Thousand characters per second.

Key. See Criterion.

Line. A line is composed of the characters that are to be printed on a single line on the On-Line Printer or Monitor Printer. Each character space to appear in the printed line decreases the maximum line capacity by one.

Line Printer. A printing device capable of printing an entire line of characters at one time.

Location. Memory storage positions.

LPM. Lines printed per minute.

LSC. Least Significant (rightmost) Character

LSD. Least Significant (rightmost) Digit.

L to R. Left to Right.

Machine Language. The system of coding which a computer "understands" internally.

Magnetic Storage. Any device which makes use of the magnetic properties of materials for the storage of information.

Magnetic Tape. A ribbon of plastic, coated or impregnated with magnetic material on which information may be stored in the form of magnetically polarized areas.

Mask. A pattern consisting of 0 and/or 1 bits, used to alter the bit configuration of an operand.

Memory. See Storage.

Message. The data relative to a single item to be processed. For example, all data relative to a single inventory item is a message. See Record.

Micro Magnetic Memory (MMM). Magnetic core device used for selective register storage and temporary storage during interrupt and other logical operations.

Microsecond. A millionth of a second.

Millisecond. A thousandth of a second.

Mnemonic Code. A pseudo-code in which information, usually instructions, is represented by symbols or characters which are readily identified with the information.

MSC. Most Significant (leftmost) character.

MSD. Most Significant (leftmost) Digit.

n. Number of characters (used in timing).

Nanosecond. A billionth of a second.

Operand. Any one of the quantities entering into an operation.

Output. (1) Information transferred from the computer to external storage. (2) The device to which the computer delivers information.

PA. Paper Advance.

PC. Page Change.

Preamble. A pattern of bits recorded by hardware in front of all blocks as they are written. It is used to synchronize the read timing clock when reading and read-after-write.

PRN. Previous Result Negative Indicator.

PRP. Previous Result Positive Indicator.

PRZ. Previous Result Zero Indicator.

Random Access. Access to storage under conditions in which the next position from which information is obtained, or to which it is delivered, is in no way dependent on the previous one.

Real-Time. The performance of a computation during the actual time that the related physical process transpires in order that results of the computations be useful in guiding the physical process.

Record. A record consists of one or more related items with the amount of information in a record being completely variable.

Register. A storage device with a specifically assigned function and a given unit capacity. Registers in the computer in the RCA 3301 System are of one, two, four or ten character capacity.

Relative Address. An address which specifies a location sequentially relative to a group of addresses but not a specific storage location.

Rewind. Move a tape in a backward direction to BTC or Load Point.

Routine. A set of instructions arranged in proper sequence to cause a machine to perform a desired operation.

R to L. Right to Left.

Sector, Consists of the contiguous HSM locations between any two HSM addresses, or the smallest addressable storage element of a random access device.

Sign Position. The sign of each operand is indicated by the 2^5 bit of the least significant digit (LSD) of each operand. When a "one" bit is present in the 2^5 position, the sign is negative, otherwise it is assumed positive.

Simultaneity. The ability of the computer to execute more than one instruction at the same time.

Software. The totality of programs and routines used to implement the capabilities of computers, such as generators, compilers, assemblers and operating system.

Status Level Register. Keeps the code of the status level being executed.

STA, Store A Register. The automatic storage of the final contents of the A Register.

Start Time. Time between the command to start an input-output device and the reading or writing of the first character.

Storage (Memory). A device into which units of information can be transferred, which will hold this information, and from which the information can be obtained at a later time.

STP. Store P Register. The automatic storage of the final contents of the P Register.

System. An assemblage of equipment units or instructions, or routines, designed to operate as a whole.

Unwind. Move a tape in the forward direction.

Working Storage. A portion of the internal storage reserved for intermediate and partial results during computation.

APPENDIX II - MEMORY LOCATIONS AND ADDRESSES

MEMORY LOCATIONS	ADDRESSES	MEMORY LOCATIONS	ADDRESSES
0000 to 9999	0000 to 9999		
10000 to 10999	&000 to &999	50000 to 50999	&&00 to &I99
11000 to 11999	A000 to A999	51000 to 51999	A&00 to AI99
12000 to 12999	B000 to B999	52000 to 52999	B&00 to BI99
13000 to 13999	C000 to C999	53000 to 53999	C&00 to CI99
14000 to 14999	D000 to D999	54000 to 54999	D&00 to DI99
15000 to 15999	E000 to E999	55000 to 55999	E&00 to EI99
16000 to 16999	F000 to F999	56000 to 56999	F&00 to FI99
17000 to 17999	G000 to G999	57000 to 57999	G&00 to GI99
18000 to 18999	H000 to H999	58000 to 58999	H&00 to HI99
19000 to 19999	I000 to I999	59000 to 59999	I&00 to II99
20000 to 20999	-000 to -999	60000 to 60999	-&00 to -I99
21000 to 21999	J000 to J999	61000 to 61999	J&00 to JI99
22000 to 22999	K000 to K999	62000 to 62999	K&00 to KI99
23000 to 23999	L000 to L999	63000 to 63999	L&00 to LI99
24000 to 24999	M000 to M999	64000 to 64999	M&00 to MI99
25000 to 25999	N000 to N999	65000 to 65999	N&00 to NI99
26000 to 26999	O000 to O999	66000 to 66999	O&00 to OI99
27000 to 27999	P000 to P999	67000 to 67999	P&00 to PI99
28000 to 28999	Q000 to Q999	68000 to 68999	Q&00 to QI99
29000 to 29999	R000 to R999	69000 to 69999	R&00 to RI99
30000 to 30999	"000 to "999	70000 to 70999	"&00 to "I99
31000 to 31999	/000 to /999	71000 to 71999	/&00 to /I99
32000 to 32999	S000 to S999	72000 to 72999	S&00 to SI99
33000 to 33999	T000 to T999	73000 to 73999	T&00 to TI99
34000 to 34999	U000 to U999	74000 to 74999	U&00 to UI99
35000 to 35999	V000 to V999	75000 to 75999	V&00 to VI99
36000 to 36999	W000 to W999	76000 to 76999	W&00 to WI99
37000 to 37999	X000 to X999	77000 to 77999	X&00 to XI99
38000 to 38999	Y000 to Y999	78000 to 78999	Y&00 to YI99
39000 to 39999	Z000 to Z999	79000 to 79999	Z&00 to ZI99
40000 to 40999	0&00 to 0I99	80000 to 80999	0-00 to 0R99
41000 to 41999	1&00 to 1I99	81000 to 81999	1-00 to 1R99
42000 to 42999	2&00 to 2I99	82000 to 82999	2-00 to 2R99
43000 to 43999	3&00 to 3I99	83000 to 83999	3-00 to 3R99
44000 to 44999	4&00 to 4I99	84000 to 84999	4-00 to 4R99
45000 to 45999	5&00 to 5I99	85000 to 85999	5-00 to 5R99
46000 to 46999	6&00 to 6I99	86000 to 86999	6-00 to 6R99
47000 to 47999	7&00 to 7I99	87000 to 87999	7-00 to 7R99
48000 to 48999	8&00 to 8I99	88000 to 88999	8-00 to 8R99
49000 to 49999	9&00 to 9I99	89000 to 89999	9-00 to 9R99

(Cont'd)

MEMORY LOCATIONS	ADDRESSES	MEMORY LOCATIONS	ADDRESSES
90000 to 90999	&-00 to &R99	130000 to 130999	&"00 to &Z99
91000 to 91999	A-00 to AR99	131000 to 131999	A"00 to AZ99
92000 to 92999	B-00 to BR99	132000 to 132999	B"00 to BZ99
93000 to 93999	C-00 to CR99	133000 to 133999	C"00 to CZ99
94000 to 94999	D-00 to DR99	134000 to 134999	D"00 to DZ99
95000 to 95999	E-00 to ER99	135000 to 135999	E"00 to EZ99
96000 to 96999	F-00 to FR99	136000 to 136999	F"00 to FZ99
97000 to 97999	G-00 to GR99	137000 to 137999	G"00 to GZ99
98000 to 98999	H-00 to HR99	138000 to 138999	H"00 to HZ99
99000 to 99999	I-00 to IR99	139000 to 139999	I"00 to IZ99
100000 to 100999	--00 to -R99	140000 to 140999	-"00 to -Z99
101000 to 101999	J-00 to JR99	141000 to 141999	J"00 to JZ99
102000 to 102999	K-00 to KR99	142000 to 142999	K"00 to KZ99
103000 to 103999	L-00 to LR99	143000 to 143999	L"00 to LZ99
104000 to 104999	M-00 to MR99	144000 to 144999	M"00 to MZ99
105000 to 105999	N-00 to NR99	145000 to 145999	N"00 to NZ99
106000 to 106999	O-00 to OR99	146000 to 146999	O"00 to OZ99
107000 to 107999	P-00 to PR99	147000 to 147999	P"00 to PZ99
108000 to 108999	Q-00 to QR99	148000 to 148999	Q"00 to QZ99
109000 to 109999	R-00 to RR99	149000 to 149999	R"00 to RZ99
110000 to 110999	"-00 to "R99	150000 to 150999	""00 to "Z99
111000 to 111999	/-00 to /R99	151000 to 151999	/"00 to /Z99
112000 to 112999	S-00 to SR99	152000 to 152999	S"00 to SZ99
113000 to 113999	T-00 to TR99	153000 to 153999	T"00 to TZ99
114000 to 114999	U-00 to UR99	154000 to 154999	U"00 to UZ99
115000 to 115999	V-00 to VR99	155000 to 155999	V"00 to VZ99
116000 to 116999	W-00 to WR99	156000 to 156999	W"00 to WZ99
117000 to 117999	X-00 to XR99	157000 to 157999	X"00 to XZ99
118000 to 118999	Y-00 to YR99	158000 to 158999	Y"00 to YZ99
119000 to 119999	Z-00 to ZR99	159000 to 159999	Z"00 to ZZ99
120000 to 120999	0"00 to 0Z99		
121000 to 121999	1"00 to 1Z99		
122000 to 122999	2"00 to 2Z99		
123000 to 123999	3"00 to 3Z99		
124000 to 124999	4"00 to 4Z99		
125000 to 125999	5"00 to 5Z99		
126000 to 126999	6"00 to 6Z99		
127000 to 127999	7"00 to 7Z99		
128000 to 128999	8"00 to 8Z99		
129000 to 129999	9"00 to 9Z99		

APPENDIX III - SYMBOLS USED FOR N CHARACTER COUNTS EXCEPT IN REPEAT, SHIFT, WRITE INSTRUCTIONS

N Count	Symbol	N Count	Symbol	N Count	Symbol	N Count	Symbol
0	0	11	A	22	K	33	T
1	1	12	B	23	L	34	U
2	2	13	C	24	M	35	V
3	3	14	D	25	N	36	W
4	4	15	E	26	O	37	X
5	5	16	F	27	P	38	Y
6	6	17	G	28	Q	39	Z
7	7	18	H	29	R	40	÷
8	8	19	I	30	"	41	, (Comma)
9	9	20	– (Minus)	31	/	42	%
10	&	21	J	32	S	43	↑
						44	=
						45	⌧

APPENDIX IV - SYMBOLS USED FOR N CHARACTER COUNTS IN REPEAT, SHIFT, WRITE INSTRUCTIONS

N Count	Symbol	N Count	Symbol	N Count	Symbol	N Count	Symbol
0	0	4	4	8	8	12	@
1	1	5	5	9	9	13	(
2	2	6	6	10	¬	14	)
3	3	7	7	11	#	15	e

APPENDIX V - N CHARACTER SYMBOLS FOR I/O DEVICES

DEVICE DESCRIPTION	N CHARACTER SYMBOLS			
	First Control	Second Control	Third Control	Fourth Control
Magnetic Tape 2 X 6 Dual Tape Channel	1 2 3 4 5 6	9 ¬ # @ ( )	A B C D E F	| + . ; : '
Magnetic Tape 2 X 12 Dual Tape Channel	1 2 3 4 5 6 9 ¬ # @ ( )	A B C D E F | + . ; : '		
Card Reader	–	J		
Card Punch	M	N		
Paper Tape Reader	K	L		
Paper Tape Punch	O	P		
On-Line Printer	Q	R		
Console Typewriter	=			
Communications Mode Control	Y			
Communications Control	%	•		
Data Exchange Control	÷	,		
Data Drum Memory	E| $(52)_8$			

APPENDIX VI - RCA 3301 INSTRUCTION LISTING BY OPERATION CODE

OP CODE	MNEMONIC	INSTRUCTION NAME	COMMENTS	PAGE REF.
2	CD1	Control Device Simo 1		Index - 1
3	CD2	Control Device Simo 2		Index - 1
4	RF1	Read Forward Simo 1		Index - 3
5	RF2	Read Forward Simo 2		Index - 3
6	RR1	Read Reverse Simo 1		Index - 3
7	RR2	Read Reverse Simo 2		Index - 3
8	WR1	Write Simo 1		Index - 4
9	WR2	Write Simo 2		Index - 4
#	TSL	Transfer by Symbol Left		V-15
@	FXA	Fixed Point Add	Scientific	XXII-6
(	FXS	Fixed Point Subtract	Scientific	XXII-8
)	FXM	Fixed Point Multiply	Scientific	XXII-10
&	FXD	Fixed Point Divide	Scientific	XXII-12
A	TBT	Translate by Table		V-21
B	CD3	Control Device Simo 3	Simo 3	XXIII-1
D	RF3	Read Forward Simo 3	Simo 3	XXIII-1
E	COC	Control CMC	CMC	XX-13
E	SES	Sector Select	DDM	XVII-3
F	RR3	Read Reverse Simo 3	Simo 3	XXIII-1
H	WR3	Write Simo 3	Simo 3	XXIII-1
+	ADT	Add Data		VI-3
+	AAD	Add Address		VI-1
+	MPY	Multiply		VI-15
+	DVD	Divide		VI-5
.	HLT	Halt		VII-9
.	PIN	Programmed Interrupt		VII-12
:	FLS	Floating Point Subtract	Scientific	XXII-16
C_R	LDR	Load Register		VII-10
−	SDT	Subtract Data		VI-20
−	SAD	Subtract Address		VI-18
−	CAD	Compare Address		VII-1
J	SFS	Symbol Fill Sector		V-7
K	LAL	Locate Absence of Symbol Left		V-3
L	LAR	Locate Absence of Symbol Right		V-5
M	TCL	Transfer by Count Left		V-10
N	TCR	Transfer by Count Right		V-11
P	TSR	Transfer by Symbol Right		V-17
Q	LIO	Logical Inclusive "OR"		VI-13
R	RPT	Repeat		VII-13
⊏	CIL	Control Interrupt Logic		VII-7
$	FLA	Floating Point Add	Scientific	XXII-14
*	ER1	Erase Simo 1		Index 2
>	ER2	Erase Simo 2		Index 2
<	SIN	Scan Interrupt		VII-14
10	TDC	Transfer Decade by Count		V-19
"	FLM	Floating Point Multiply	Scientific	XXII-18
/	FLD	Floating Point Divide	Scientific	XXII-20
S	TDV	Test Device		Index 4
T	LAN	Logical "AND"		VI-9
U	LEO	Logical Exclusive "OR"		VI-11
V	STR	Store Register		VII-17
W	CTC	Conditional Transfer of Control		VII-5
W	UTC	Unconditional Transfer of Control		VII-21
X	TLY	Tally		VII-19
Y	CDT	Compare Data		VII-3
Z	SAC	Store Accumulator	Scientific	XXII-22
÷	TCE	Transfer by Count to Edit Field		V-13
,	SFN	Symbol Fill to Non-Zero Numeric		V-8
,	FDN	Float Dollar Sign to Non-Zero Numeric		V-1
%	ER3	Erase Simo 3	Simo 3	XXIII-1
=	SHA	Shift Accumulator	Scientific	XXII-24

APPENDIX VII - SUMMARY OF INSTRUCTIONS (DATA HANDLING)

MNEM-ONIC	OP CODE	INSTRUCTION NAME	N CHARACTER	A ADDRESS	B ADDRESS	SPECIAL CONDITIONS
FDN	(Comma)	Float Dollar Sign to Non-Zero Numeric	$	Leftmost HSM location to be searched	Rightmost HSM location to be searched	STA PRI
LAL	K	Locate Absence of Symbol Left	Specified Symbol	Leftmost HSM location to be searched	Rightmost HSM location to be searched	STA PRI
LAR	L	Locate Absence of Symbol Right	Specified Symbol	Rightmost HSM location to be searched	Leftmost HSM location to be searched	STA PRI
SFS	J	Symbol Fill Sector	Specified Symbol	Leftmost HSM location to be filled	Rightmost HSM location to be filled	
SFN	(Comma)	Symbol Fill to Non-Zero Numeric	Specified Symbol (except $)	Leftmost HSM location to be searched	Rightmost HSM location to be searched	STA PRI
TCL	M	Transfer by Count Left	No. of characters (0-45)	HSM location of leftmost char. in sending area	HSM location of leftmost char. in receiving area	REP
TCR	N	Transfer by Count Right	No. of characters (0-45)	HSM location of rightmost char. in sending area	HSM location of rightmost char. in receiving area	REP
TCE	÷	Transfer by Count to Edit Field	No. of characters (0-45)	HSM location of rightmost char. of the edit (receiving) field	HSM location of rightmost char. of the non-edited (sending) field	STA PRI
TSL	#	Transfer by Symbol Left	Symbol after which to stop transferring	HSM location of leftmost char. in sending area	HSM location of leftmost char. in receiving area	STA REP
TSR	P	Transfer by Symbol Right	Symbol after which to stop transferring	HSM location of rightmost char. in sending area	HSM location of rightmost char. in receiving area	STA REP
TDC	10 (Sub 10)	Transfer Decade by Count	No. of decades (0-45)	HSM location of leftmost decade in sending area	HSM location of leftmost decade in receiving area	REP
TBT	A	Translate by Table	No. of characters (0-45)	HSM location of leftmost char. to be translated and the result area	HSM location of leftmost char. of translate table (must end in 00)	REP

APPENDIX VII - SUMMARY OF INSTRUCTIONS (ARITHMETIC AND LOGICAL)

MNEM-ONIC	OP CODE	INSTRUCTION NAME	N CHARACTER	A ADDRESS	B ADDRESS	SPECIAL CONDITIONS
AAD	+	Add Address	+ (Plus)	HSM location of LSD of augend and sum	HSM location of LSD of addend	REP PRI
ADT	+	Add Data	No. of characters (0-45)	HSM location of LSD of augend and sum	HSM location of LSD of addend	REP PRI
DVD	+	Divide	· (Period)	HSM location of LSD of dividend and quotient	HSM location of LSD of divisor	PRI
LAN	T	Logical "And"	No. of characters (0-45)	HSM location of right-most char. of original operand and result	HSM location of right-most char. of modifier	REP PRI
LEO	U	Logical Exclusive "Or"	No. of characters (0-45)	HSM location of right-most char. of original operand and result	HSM location of right-most char. of modifier	REP
LIO	Q	Logical Inclusive "Or"	No. of characters (0-45)	HSM location of right-most char. of original operand and result	HSM location of right-most char. of modifier	REP
MPY	+	Multiply	$	HSM location of LSD of multiplicand	HSM location of LSD of multiplier and LSD of the 8 most significant digits of the product	PRI
SAD	– (Minus)	Subtract Address	+ (Plus)	HSM location of LSD of the minuend and difference	HSM location of LSD of subtrahend	REP PRI
SDT	– (Minus)	Subtract Data	No. of characters (0-45)	HSM location of LSD of minuend and difference	HSM location of LSD of subtrahend	REP PRI

APPENDIX VII - SUMMARY OF INSTRUCTIONS (DECISION AND CONTROL)

MNEM-ONIC	OP CODE	INSTRUCTION NAME	N CHARACTER	A ADDRESS	B ADDRESS	SPECIAL CONDITIONS
CAD	– (Minus)	Compare Address	. (Period)	HSM location of rightmost char. of minuend	HSM location of rightmost char. of subtrahend	PRI
CDT	Y	Compare Data	No. of characters (0-45)	HSM location of leftmost char. of first (minuend) operand	HSM location of leftmost char. of second (subtrahend) operand	PRI
CTC	W	Conditional Transfer of Control	Indicator or switch to be sensed	Address of next instruction when condition exists	Address of next instruction when condition exists	STP
CIL	[(Open Bracket)	Control Interrupt Logic	Specifies function	0000 (Not to be used)	0000 (Not to be used)	
HLT	. (Period)	Halt	. (Period)	Unused	Unused	
LDR	C_R (Credit)	Load Register	MMM location symbol	Rightmost HSM diad containing contents to be stored	0000 (Not to be used)	
PIN	. (Period)	Programmed Interrupt	Any symbol except a period	Unused	Unused	
RPT	R	Repeat	No. of repeats (0-15)	Even=No instruction access of A Addr. when instruction is repeated Odd=Instruction access of A Addr.	Even=No instruction access of B Addr. when instruction is repeated Odd=Instruction access of B Addr.	
SIN	< (Less)	Scan Interrupt	Designates Interrupt Indicators	A_0A_3 To be set initially by programmer A_1A_2 00	HSM location of leftmost char. of inhibit mask	STA
STR	V	Store Register	MMM location symbol	Rightmost HSM diad to receive contents	Address of next instruction if P is stored; otherwise 0000.	
TLY	X	Tally	Incrementing Options	HSM Location of diad containing quantity to be tested or 0000 if only incrementing	Address of next instruction if quantity has not been exhausted or 0000 if only incrementing	STP
UTC	W	Unconditional Transfer of Control	(Period)	0000 (Not to be used)	HSM location of next instruction to be executed	

APPENDIX VII - SUMMARY OF INSTRUCTIONS (INPUT/OUTPUT)

MNEM-ONIC	OP CODE	INSTRUCTION NAME	N CHARACTER	A ADDRESS	B ADDRESS	SPECIAL CONDITIONS
CD1 CD2	2 3	Control Device Simo 1 Control Device Simo 2	Device Symbol	0000 (Not to be used)	$B_0B_1B_2$ = 000 (Not to be used) Card Reader B_3 = 0 Translate Mode B_3 = 1 Binary Mode Magnetic Tape B_3 = 1 Rewind to BTC B_3 = 2 Rewind to Load Point and disconnect B_3 = 4 Rewind 1 gap	
ER1 ER2	* > (Greater)	Erase Simo 1 Erase Simo 2	Magnetic Tape Station Symbol	Beginning HSM location used for counting the no. of chars. to be erased	Ending HSM location used for counting the no. of characters to be erased	
RF1 RF2	4 5	Read Forward Simo 1 Read Forward Simo 2	Device Symbol	HSM location to receive first char. Must be even for Card Reader.	Paper Tape, Magnetic Tape and Console Typewriter HSM location to receive last character Card Reader 0000 (Not to be used)	
RR1 RR2	6 7	Read Reverse Simo 1 Read Reverse Simo 2	Paper Tape or Magnetic Tape Station Symbol	HSM location to receive first char.	HSM location to receive last character	
TDV	S	Test Device	Device Symbol	Specifies the test, set or reset function to be performed	Address of next instruction to be executed if the condition(s) being tested are present	STP

APPENDIX VII - SUMMARY OF INSTRUCTIONS (INPUT/OUTPUT) Cont'd

MNEMONIC	OP CODE	INSTRUCTION NAME	N CHARACTER	A ADDRESS	B ADDRESS	SPECIAL CONDITIONS
WR1 WR2	8 9	Write Simo 1 Write Simo 2	Device Symbol	HSM location of first character to be written, typed or punched. Must be even for card punching and printer buffer loading Paper Advancing – 0000 (Not to be used)	<u>Paper Tape, Magnetic Tape & Console Typewriter</u> HSM location of last character to be written. <u>Card Punch</u> $B_0 B_1 B_2$ = 000 (Not to be used) B_3 = 0 Translate Mode B_3 = 1 Binary Mode <u>On-Line Printer</u> B_0 = 0 Paper advance via count in B_2 B_0 = 1 Loop-controlled vertical tabulation B_0 = 2 Loop-controlled page change B_1 = 0 Asynchronous mode printing B_1 = 1 No printing B_1 = 2 Synchronous mode printing B_2 = Number of lines (0-15) to advance B_3 = 0 No HSM to Buffer Transfer B_3 = 1 Print 120 characters B_3 = 2 Print 160 characters B_3 = 4 Print Table to Buffer	

APPENDIX VIII - RCA 3301 CODES

CHARACTER		PRINTED SYMBOL	MACHINE CODE							CARD CODE PUNCHED ROWS
DESCRIPTION	CODE		P	ZONE		NUMERIC				
			2^6	2^5	2^4	2^3	2^2	2^1	2^0	
Zero	0	0	1	0	0	0	0	0	0	0
One	1	1	0	0	0	0	0	0	1	1
Two	2	2	0	0	0	0	0	1	0	2
Three	3	3	1	0	0	0	0	1	1	3
Four	4	4	0	0	0	0	1	0	0	4
Five	5	5	1	0	0	0	1	0	1	5
Six	6	6	1	0	0	0	1	1	0	6
Seven	7	7	0	0	0	0	1	1	1	7
Eight	8	8	0	0	0	1	0	0	0	8
Nine	9	9	1	0	0	1	0	0	1	9
Space	Sp	]	1	0	0	1	0	1	0	
Number	#	#	0	0	0	1	0	1	1	3,8
At The Rate Of	@	@	1	0	0	1	1	0	0	4,8
Open Parenthesis	(	(	0	0	0	1	1	0	1	5,8
Close Parenthesis	)	)	0	0	0	1	1	1	0	6,8
Error	e	e*	1	0	0	1	1	1	1	7,8
Ampersand	&	&	0	0	1	0	0	0	0	Y
A	A	A	1	0	1	0	0	0	1	Y,1
B	B	B	1	0	1	0	0	1	0	Y,2
C	C	C	0	0	1	0	0	1	1	Y,3
D	D	D	1	0	1	0	1	0	0	Y,4
E	E	E	0	0	1	0	1	0	1	Y,5
F	F	F	0	0	1	0	1	1	0	Y,6
G	G	G	1	0	1	0	1	1	1	Y,7
H	H	H	1	0	1	1	0	0	0	Y,8
I	I	I	0	0	1	1	0	0	1	Y,9
Plus	+	+	0	0	1	1	0	1	0	Y,2,8
Period	.	.	1	0	1	1	0	1	1	Y,3,8
Semicolon	;	;	0	0	1	1	1	0	0	Y,4,8
Colon	:	:	1	0	1	1	1	0	1	Y,5,8
Apostrophe	'	'	1	0	1	1	1	1	0	Y,6,8
Plus zero	+0	C_R	0	0	1	1	1	1	1	Y,0

*Printed only by typewriter.

APPENDIX VIII - RCA 3301 CODES (Cont'd)

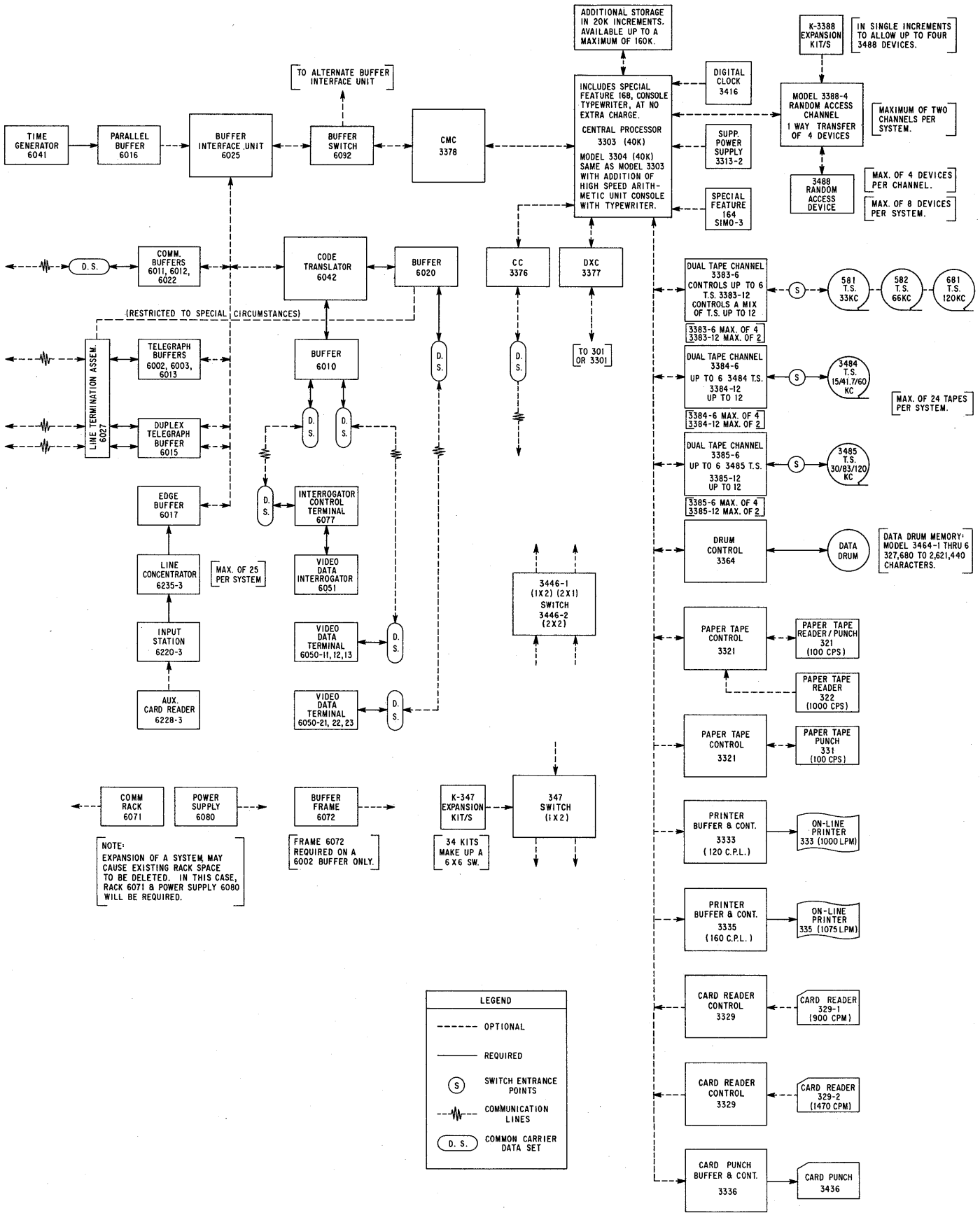
CHARACTER		PRINTED SYMBOL	MACHINE CODE							CARD CODE PUNCHED ROWS
			P	ZONE		NUMERIC				
DESCRIPTION	CODE		2^6	2^5	2^4	2^3	2^2	2^1	2^0	
Minus	–	–	0	1	0	0	0	0	0	X
J	J	J	1	1	0	0	0	0	1	X,1
K	K	K	1	1	0	0	0	1	0	X,2
L	L	L	0	1	0	0	0	1	1	X,3
M	M	M	1	1	0	0	1	0	0	X,4
N	N	N	0	1	0	0	1	0	1	X,5
O	O	O	0	1	0	0	1	1	0	X,6
P	P	P	1	1	0	0	1	1	1	X,7
Q	Q	Q	1	1	0	1	0	0	0	X,8
R	R	R	0	1	0	1	0	0	1	X,9
End Information	EI	[	0	1	0	1	0	1	0	X,2,8
Dollar	$	$	1	1	0	1	0	1	1	X,3,8
Asterisk	*	*	0	1	0	1	1	0	0	X,4,8
End Data	ED	>	1	1	0	1	1	0	1	X,5,8
End File	EF	<	1	1	0	1	1	1	0	X,6,8
Subscript 10	10	10	0	1	0	1	1	1	1	X,7,8
Quotation Mark	"	"	1	1	1	0	0	0	0	X,0
Virgule	/	/	0	1	1	0	0	0	1	0,1
S	S	S	0	1	1	0	0	1	0	0,2
T	T	T	1	1	1	0	0	1	1	0,3
U	U	U	0	1	1	0	1	0	0	0,4
V	V	V	1	1	1	0	1	0	1	0,5
W	W	W	1	1	1	0	1	1	0	0,6
X	X	X	0	1	1	0	1	1	1	0,7
Y	Y	Y	0	1	1	1	0	0	0	0,8
Z	Z	Z	1	1	1	1	0	0	1	0,9
End Block	EB	÷	1	1	1	1	0	1	0	0,2,8
Comma	,	,	0	1	1	1	0	1	1	0,3,8
Percent	%	%	1	1	1	1	1	0	0	0,4,8
Item Separator	●	↓	0	1	1	1	1	0	1	0,5,8
Equal	=	=	0	1	1	1	1	1	0	0,6,8
Lozenge	⌑	⌑	1	1	1	1	1	1	1	0,7,8

APPENDIX IX - GLOSSARY OF EQUIPMENT NOMENCLATURE

Model No.	Description
321	Paper Tape Reader/Punch
322	Paper Tape Reader (1,000 CPS)
329-1&329-2	Card Readers
331	Paper Tape Punch
333	On-Line Printer (120 Columns)
335	On-Line Printer (160 Columns)
347	Tape Switching Unit
581	Tape Station (33 KC)
582	Tape Station (66 KC)
681	Tape Station (120 KC)
3303	Processor-With 40,000 Characters High-Speed Storage
3304	Processor-With 40,000 Characters High-Speed Storage and High Speed Arithmetic Unit
Fea 164	Simultaneous Mode #3
3313-2	Supplemental Power Supply
3321	Paper Tape Control
3329	Card Reader Control
3333	Printer Buffer and Control
3335	Printer Buffer and Control
3336	Card Punch Buffer and Control
3361-2	High-Speed Storage-Expands to 60,000 chars.
3361-3	High-Speed Storage-Expands to 80,000 chars.
3361-4	High-Speed Storage-Expands to 100,000 chars.
3361-5	High-Speed Storage-Expands to 120,000 chars.
3361-6	High-Speed Storage-Expands to 140,000 chars.
3361-7	High-Speed Storage-Expands to 160,000 chars.
3376-11	Communications Control
3376-12	Communications Control
3376-21	Communications Control
3376-22	Communications Control
3376-34	Communications Control
3376-112	Communications Control
3376-122	Communications Control
3376-212	Communications Control
3376-222	Communications Control
3376-342	Communications Control
3377	Data Exchange Control
3378-21	Communications Mode Control, Sgl. Scan (20 line)
3378-41	Communications Mode Control, Sgl. Scan (40 line)
3378-61	Communications Mode Control, Sgl. Scan (60 line)
3378-81	Communications Mode Control, Sgl. Scan (80 line)
3378-101	Communications Mode Control, Sgl. Scan (100 line)
3378-121	Communications Mode Control, Sgl. Scan (120 line)
3378-141	Communications Mode Control, Sgl. Scan (140 line)
3378-161	Communications Mode Control, Sgl. Scan (160 line)
3378-22	Communications Mode Control, Dual Scan (20 line)
3378-42	Communications Mode Control, Dual Scan (40 line)
3378-62	Communications Mode Control, Dual Scan (60 line)
3378-82	Communications Mode Control, Dual Scan (80 line)
3378-102	Communications Mode Control, Dual Scan (100 line)
3378-122	Communications Mode Control, Dual Scan (120 line)
3378-142	Communications Mode Control, Dual Scan (140 line)
3378-162	Communications Mode Control, Dual Scan (160 line)
3383-6	Dual Tape Channel
3383-12	Dual Tape Channel
3385-6	Dual Tape Channel
3385-12	Dual Tape Channel
3387-6	Magnetic Tape Control
3387-12	Magnetic Tape Control
3388-4	Channel
3416	Digital Clock
3425	Tapewriter
3426	Tapewriter-Verifier
3436	Card Punch (300 CPM)
3446	Switch
3464-1	Data Drum Memory
3464-2	Data Drum Memory
3464-3	Data Drum Memory
3464-4	Data Drum Memory
3464-5	Data Drum Memory
3464-6	Data Drum Memory
3484	Tape Station (15/41.7/60KC)
3485	Tape Station (30/83/120 KC)
3488-1	File
3488-2	File Expansion Assembly
6002-11	Telegraph Buffer
6002-12	Telegraph Buffer
6002-21	Telegraph Buffer
6003	Telegraph Buffer
6010-21	Communication Buffer
6010-22	Communication Buffer
6012-11	Communication Buffer
6012-12	Communication Buffer
6012-21	Communication Buffer
6012-22	Communication Buffer
6013	Telegraph Buffer

Model No.	Description
6015	Telegraph Buffer
6016	Parallel Buffer
6020-11	Communications Buffer
6020-12	Communications Buffer
6025-100	Buffer Interface Unit
6025-101	Buffer Interface Unit
6025-210	Buffer Interface Unit
6025-211	Buffer Interface Unit
6025-220	Buffer Interface Unit
6025-221	Buffer Interface Unit
6025-400	Buffer Interface Unit
6025-401	Buffer Interface Unit
6025-411	Buffer Interface Unit
6025-421	Buffer Interface Unit
6025-431	Buffer Interface Unit
6027	Line Termination Assembly
6041	Time Generator
6042	Code Translator
6050-1	Video Data Terminal
6050-2	Video Data Terminal
6071	Communications Rack
6072	Buffer Frame
6080	Power Supply

APPENDIX X
3301 REALCOM SYSTEM
CONFIGURATION CHART



INDEX

INDEX (Cont'd)

INDEX (Cont'd)

INDEX (Cont'd)

Dear Reader:

Have you any comments or suggestions concerning this publication? Are there any omissions or deletions which you feel would enhance its usefulness....are there any errors that should be corrected? If so, we would appreciate it if you would use this form to tell us about it.

CORRECTIONS AND OMISSIONS (Please specify page numbers):

FOLD FOLD

CUT ALONG LINE

ADDITIONS AND DELETIONS (Please specify page numbers):

FOLD FOLD

Name _____

Title _____

Company _____

Address _____

NO POSTAGE REQUIRED IF MAILED IN U.S.A.

STAPLE

STAPLE

FOLD

FOLD

FIRST CLASS
PERMIT NO. 16
CAMDEN, NEW JERSEY

BUSINESS REPLY MAIL

NO POSTAGE STAMP NECESSARY IF MAILED IN THE UNITED STATES

POSTAGE WILL BE PAID BY—

RADIO CORPORATION OF AMERICA
ELECTRONIC DATA PROCESSING
CAMDEN, NEW JERSEY 08101

ATTN: Manager, EDP Methods
Cherry Hill
Bldg. 204-2

OLD

FOLD

CUT ALONG LINE

THE MOST TRUSTED NAME IN ELECTRONICS

Radio Corporation of America