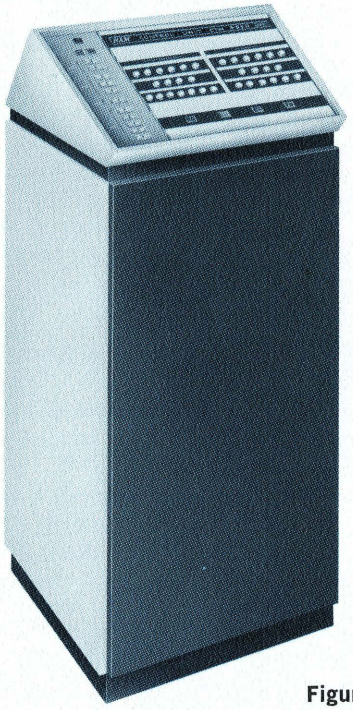
POTTER

PRODUCT DATA
1-104

RAM® CONTROL UNIT MODEL CTM-4550

POTTER INSTRUMENT CO., INC.®

- For Use With Any Data Processing System
- Cartridge Preparation
- Error Detection
- Address Location
- Complete Logic Package



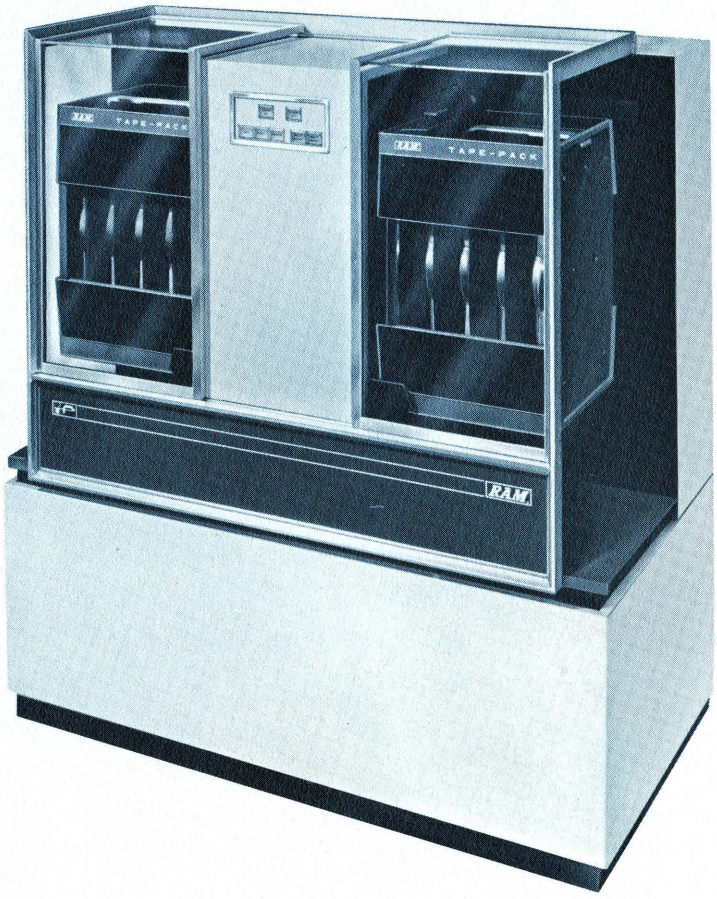


Figure 1. Potter RAM shown with Model CTM-4550 Control Unit

DESCRIPTION

The RAM Control Unit, Model CTM-4550, provides the logic and electronics necessary to adapt the Potter RAM memory system, Model TLM-4550 (see Product Data sheet 1-103), to a standard computer interface. The controller provides for cartridge (TAPE-PACK) preparation, error detection and address location to enable the RAM to be used for data storage for any Data Processing system.

EFFECTIVE: NOVEMBER 30, 1966

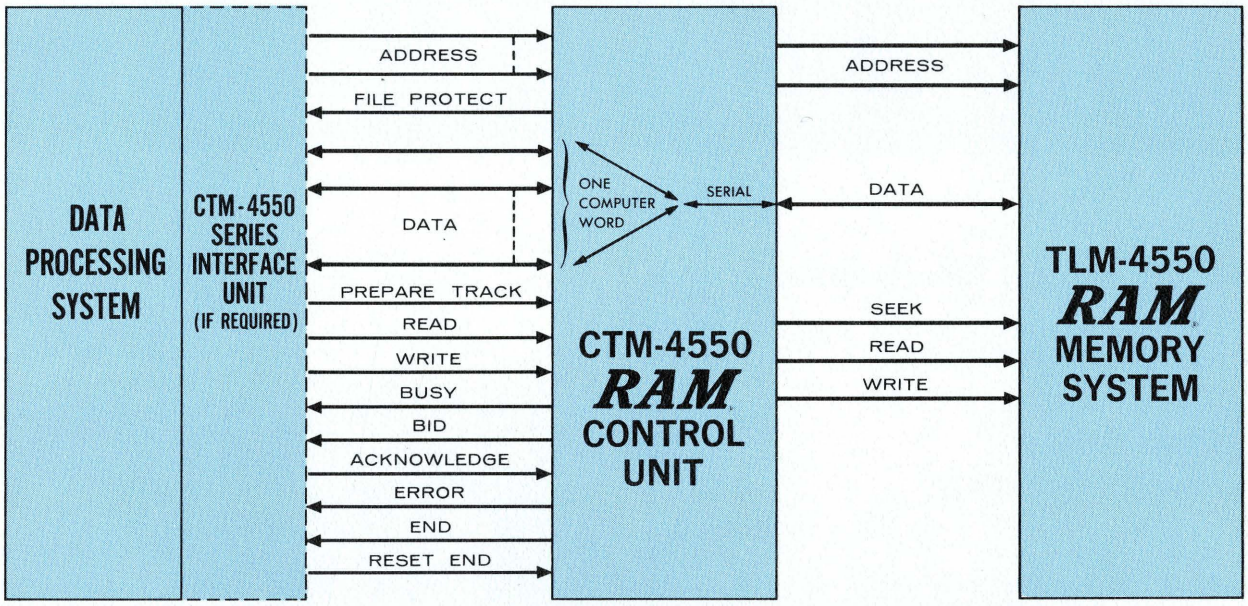


Figure 2. Simplified Functional Diagram — RAM Control Unit Model CTM-4550

DESCRIPTION *continued*

Addressing of RAM

The CTM Control Unit accepts a 14-bit RAM address from the data processor interface, in conjunction with a "read" or "write" command. The fourteen bits comprise the following information:

- left or right cartridge 1 bit
- RAM track 10 bits
- sector on the track 3 bits

The CTM causes the RAM heads to be properly positioned, and locates the correct one of up to 8 sectors on the specified track.

Reading of RAM Sector

In a "read" operation, after sector addressing has been accomplished, the CTM reads the entire sector from the RAM and sends it word-parallel to the data processor interface. Error-checking through word-parity, and a record-length check are performed.

Writing of RAM Sector

In a "write" operation, after sector addressing has been accomplished, the CTM obtains the entire sector word-parallel from the data processor interface, and stores it in the RAM. Parity bits are affixed while writing. A read-after-write check is performed on the complete sector, while writing is being performed.

DESCRIPTION OF CTM OPERATION

A functional block diagram of the CTM Control Unit is presented in Figure 2. With the CTM, a Data Processing system can conveniently cause any of the three operations of read, write, or sectorize to be performed.

Seek and Read

The search logic causes the proper one of the 1792 RAM tracks to be selected. When the RAM head is in position, the stored information on the track is examined by the search logic until the sector ID corresponding to the desired sector is found. The desired information immediately follows the sector ID on the track. This information is decoded and accumulated in the Computer Access Register. Whenever one computer word has been accumulated in the Computer Access Register, a BID signal is sent to the DP System; this instructs the DP System that one word is ready to be transferred out of the CTM; return of the ACKNOWLEDGE signal by the DP System indicates to the CTM that the word has been transferred out. This word-serial transfer operation continues until the end of the sector is reached.

Redundancy bits are stored with the data to insure error-free operation; they are checked and stripped off during reading by the read check logic. If they do not meet the specified criteria, an ERROR is signalled. The redundancy bits consist of parity bits spaced throughout the data.

Seek and Write

SEEK AND WRITE proceeds identically with SEEK AND READ until the proper sector ID is located. At that time, a BID signal is sent to the DP System, indicating that the CTM requires a computer word. The ACKNOWLEDGE signal from the DP System indicates that the word is ready on the data lines. The CTM stores the word into the Computer Access Register, and then transfers it serially to be encoded and written onto the RAM sector. This transfer operation is repeated until the end of the sector is reached.

The Write Check Generator Logic fabricates parity bits and inserts them into the proper places in the data. Simultaneous with writing, the data parity is checked in a read-after-write operation.

Sectorization of RAM Cartridge or Track

RAM cartridges require sectorization before initial use, whenever a tape loop is replaced, and whenever a cartridge or a single track is to be erased and re-used. The result of sectorization of a track is that the track contains 8 sectors; each sector is identified by a stored sector number, and no other data exists on the track. The result of sectorization of a track is as described here regardless of whether the track originally—i.e. before being sectorized—contained data, contained some different number of sectors, or contained nothing. Multiple length records can be written by overwriting unused sector identifiers.

Since inadvertent sectorization could destroy live data, a fully interlocked sectorization operation is provided. A console mode switch is set to "sectorize;" this causes a "sectorize" status line to be sent to the data processing interface, and simultaneously prevents the performing of a normal "read" or "write" operation. The data processor then provides a track address (11 of the 14 address bits) and a "sectorize" command, and the track is automatically sectorized.

Prior to the initiation of a sectorization, the console mode switch is set to SECTORIZE. The eleven bit cartridge-and-track address is placed on the address lines by the DP System, and the SECTORIZE command given. The desired track is located as before. The Sectorization Logic then saturates the track with a recorded pattern, locates the tape splice, and records the ID blocks, dividing the track into precisely equal sectors. The recorded ID blocks contain an ID indicator, plus the address of the sector. The data portion of each sector is erased.

Maintenance Facilities

Built-in maintenance indicators and exercisers are provided to assist in preventive and corrective maintenance on the CTM-RAM system. The combination of these facilities and computer-generated diagnostic programs will provide integrity of data and operation, and minimization of downtime.

ERROR CHECKING FACILITY

Check bits are added by the CTM when writing on the RAM, checked in the read-after-write mode, and checked and stripped from the data when reading from the RAM. There are two checking facilities:

1—Two even-parity bits are added to approximately each two DP System words stored. These two bits represent, respectively, the even parity for all the odd and even bits in the words.

2—In the ID block, the 3-bit sector portion of the address is stored in full duplicate, to provide protection against operation on the wrong sector.

Using this checking scheme, and using as a basis a 24-bit DP System word, an undetected data error can be expected to occur less than once in 3×10^9 records, or once every 100 years, assuming that a block is read every 200 ms for an 8-hour shift, 200 days per year.

Note that the affixing of two parity bits per 48-data bits results in a deterioration of data storage capacity of slightly over 4%.

OPTIONAL ACCESSORIES

Data Processor Interface

The CTM interface logic is compatible with standard computer interface practice. However, in general some hardware is required to exactly match the CTM to a specific computer, either logically or electrically. Interface units are available for this purpose.

Each of these Interface Units (designated Series ITM4550) adapts the CTM to a particular DP System, both logically and electrically.

Sectorization Control

The Sectorization Control Unit attaches to the CTM and relieves the DP System from programming the addresses used for the sectorization operation. Two modes of operation are provided:

Sectorize a Track: One track address is manually selected, and only that track is sectorized.

Sectorize a Cartridge: Each of the 896 tracks in a cartridge is selected in turn, and sectorized.

OPTIONAL ACCESSORIES

continued

Multiple-RAM Unit

This unit allows a group of RAMS to be treated as a single data storage unit. Additional bits are added to the normal 11-bit address to accommodate the additional RAMs; these are decoded and the appropriate RAM unit is connected to the CTM.

CTM Configurations

Two basic controllers are available: one which is 6-bit character oriented and one which is 8-bit byte oriented. The 6-bit oriented controller handles computer words of 12, 18 or 24 bit lengths to be specified by the user.

The 8-bit byte oriented controller can be used directly with interface word lengths which are 8 bits in length. For multiples of 8 bits (e.g. 16-bit computer words), additional buffering must be supplied in the interface.

Input Logic Levels: 1 = +5±1V from a 2k source impedance
0 = 0±.5V at 12 ma

Output Logic Levels: 1 = +5±.25V from a 2k source impedance
0 = .25±.25V at 6 ma

POTTER WORLDWIDE FIELD SERVICE AND LOGISTICS PROGRAMS

Repair centers in strategic locations within the continental United States and abroad have been established to support the entire Potter product line.

Staffed by highly-trained field representatives, these repair centers are equipped to effect on-site installation of equipments and to perform quality repair, maintenance and overhaul.

Supplementing this capability, if a customer prefers to provide his own equipment support, Potter has established standard instruction courses to train customer personnel, either at Potter or in the field.

A Spare Parts Department, backed up by an extremely large inventory, and streamlined order processing, is available for customer convenience and economy. This inventory permits the customer to realize virtual elimination of downtime as well as savings on spare parts dollars by offering expeditious delivery for replaceable parts. Delivery is available in 24 hours to meet customer emergency requirements — within 72 hours for standard parts under normal conditions. Potter also offers provisioning and logistics capabilities to meet all existing military specifications.

The Potter field service and logistics program is one of the finest in the EDP equipment industry. With reliable, quality-engineered equipment, supported by comprehensive field service, Potter guarantees satisfaction.

POTTER INSTRUMENT COMPANY, INC.
151 SUNNYSIDE BOULEVARD • PLAINVIEW, NEW YORK • 516 OVERBROOK 1-3200

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