Monolithic Systems corp.

MAINTENANCE MANUAL

MONOSTORE XI/PLANAR
LSI-11 Add-IN
Semiconductor Memory System

MSC 4501

14 Inverness Drive East, Englewood, Colorado 80110 (303) 770-7400

A B C D E F G H I J K L M

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
A	RELEASED	4/28/76	J.W.
B	REVISED TABLE	5/20/76	J.W.
C	REVISED SECTION V	10/13/76	RW
D	ADDED EQUIP REV LEV. TO SHT 16	12-1-76	TBS.
E	REVISED PER ECO 0586	02-04-77	TBS

REV																														
SHEET																														
REV STATUS OF SHEETS	REV	E	A	A	A	A	E	A	E	A	B	E	E	E	E	A	D													
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16													

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES FRACTIONS DECIMALS ANGLES

MATERIAL

DATE

DRAWN

CHECKED

APPROVED J. Waldenger

APPROVED

MONOLITHIC SYSTEMS CORP.

MONOSTORE XI/PLANAR
LSI-11 Add-In

SIZE	CODE IDENT NO.	DWG NO.
A	51513	100-0046-000

SCALE	REV	SHEET
	E	1

MONOSTORE XI/PLANAR
LSI-11 Add-In

SEMICONDUCTOR MEMORY SYSTEM

C O N T E N T S

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SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

This manual provides information for installing, operating, and maintaining the Monostore XI/Planar LSI-11 add-in memory systems. The material is arranged in five sections as follows:

Section I General Description

This section provides the scope, contents, and arrangement of the manual. A general description and a list of system specifications are also given.

Section II Installation and Operation

Instructions are provided for unpacking, inspecting and installing the memory system.

Section III Theory of Operation

An overall description of the memory system is provided along with a timing diagram to aid in understanding the system and to support troubleshooting.

Section IV Maintenance and Troubleshooting

This section gives recommended general maintenance procedures and troubleshooting information for diagnosing and locating a malfunction.

Section V Drawings

This section contains schematics, assembly and parts list for the memory system.

1.2 GENERAL DESCRIPTION

The Monostore XI/PL LSI-11 Add-in Memory System, P/N 303-0156-XXX, consists of a single planar 16K X 16 memory assembly. All electronics, DC conversion, and semiconductor dynamic N channel memory storage elements are contained on a single printed circuit board. The memory elements are mounted in IC sockets providing for ease of replacement.

All signal interface is made through the DEC LSI-11 I/O bus. Data interfacing is provided by 16 bidirectional data bits. Addressing any one of the 16,384 words is provided by 14 binary address bits, together with command and control information to define the memory mode required.

The memory system uses the +5V, +5VB, and +12V power available on the LSI-11 I/O bus and generates -5V on the board.

The maximum capacity of the board is 16,384 words by 16 bits. The system can also be configured in 4,096 word increments by 16 bits.

The memory can be programmed to use the external refresh command or to inhibit external and run on internal refresh only. It can also be programmed to reply to external refresh commands via the BRPLYL signal.

Critical circuitry is powered from the +5V battery backed up source so that integrity of data is maintained during power fail status.

1.3 MODES OF OPERATION (SLAVE = MEMORY)

Name	Mnemonic	AO line	Function
Data In	BDINL	X	Data from slave to master
Data out	BDOUTL (BWTBTL = 0)	X	Data from master to slave
Data out (byte)	BDOUTL (BWTBTL = 1)	1 0	Bits 0-7 are affected Bits 8-15 are affected
RMW	BDINL BDOUTL	X	Data from slave to master. Master modifies data and transmits data from master to slave. (Can be byte mode on master to slave data)

1.4 SYSTEM SPECIFICATIONS

Characteristics	Specification
Storage capacity	4096 words X 16 bits 8192 words X 16 bits 12288 words X 16 bits 16384 words X 16 bits
Cycle time	600 nsec
Access time	450 nsec
Input power	+5VB, 1.25A +5V, 0.65A +12V, 0.55A
Operating Environment	
Temperature	0^{o} C to $+50^{o}$ C
Relative Humidity	90% maximum without condensation
Physical Dimensions	
Height	8.5 inches
Depth	0.5 inches
Width	10.5 inches

SECTION II

INSTALLATION & OPERATION

2.1 INTRODUCTION

This section contains information for installation and operation of the memory system.

2.2 UNPACKING AND INSPECTION

Carefully remove the memory system from the shipping container. Remove any packing material from the assembly. Inspect the system for any damage or loose connections.

2.3 INSTALLING MEMORY SYSTEM

Insert the memory system into the LSI-11 I/O bus in the ABCD sections.

The memory system is now ready for use.

2.4 I/O SIGNALS

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
AA1	BSPARE 1	BA1	BDCOKH	AA2	+5	BA2	+5
AB1	BSPARE 2	BB1	BPOKH	AB2	-12	BB2	-12
AC1	BSPARE 3	BC1	SSPARE 4	AC2	GND	BC2	GND
AD1	BSPARE 4	BD1	SSPARE 5	AD2	+12	BD2	+12
AE1	SSPARE 1	BE1	SSPARE 6	AE2	BDOUTL	BE2	BDAL2L
AF1	SSPARE 2	BF1	SSPARE 7	AF2	BRPLYL	BF2	BDAL3L
AH1	SSPARE 3	BH1	SSPARE 8	AH2	BDINL	BH2	BDAL4L
AJ1	GND	BJ1	GND	AJ2	BSYNCL	BJ2	BDAL5L
AK1	MSPARE A	BK1	MSPAREB	AK2	BWTBTL	BK2	BDAL6L
AL1	MSPARE A	BL1	MSPAREB	AL2	BIRQL	BL2	BDAL7L
AM1	GND	BM1	GND	AM2	BIAKIL	BM2	BDAL8L
AN1	BDMRL	BN1	BSACKL	AN2	BIAKOL	BN2	BDAL9L
AP1	BHALTL	BP1	BSPARE 6	AP2	BBS7L	BP2	BDAL10L
AR1	BREFL	BR1	BEVNTL	AR2	BDMGIL	BR2	BDAL11L
AS1	PSPARE 3	BS1	PSPARE 4	AS2	BDMGOL	BS2	BDAL12L
AT1	GND	BT1	GND	AT2	BINITL	BT2	BDAL13L
AU1	PSPARE 1	BU1	PSPARE 2	AU2	BDALOL	BU2	BDAL14L
AV1	+5B	BV1	+5B	AV2	BDALIL	BV2	BDAL15L

Slot (Row) C is identical to slot A.
Slot D is identical to slot B.
AF1 (SSPARE 2) and DF1 (SSPARE 7) can be user wired for +12V battery. This option applies to -005,-006,-007, or -008 boards only.

SECTION III

THEORY OF OPERATION

3.1 INTRODUCTION

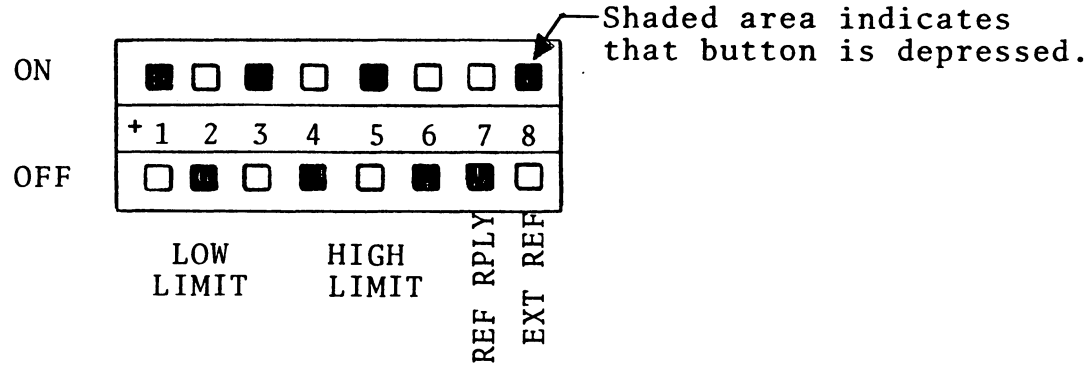
This section describes the overall organization and operation of this MO XI PL LSI-11 Add-in Semiconductor Memory System. The System has a maximum capacity of 16384 words of 16 bits.

This section is organized into the following major parts:

Description	Paragraph
Memory Location Programming	3.2
Address-Channel	3.3
Data Channel	3.4
Timing Circuitry	3.5
DC Converter	3.6

3.2 MEMORY LOCATION PROGRAMMING

The memory location is programmed via switches on the board. The user can program the memory to any location according to the following table.



Example shown is for address 040000(8K) lo limit and 120000 (20K) hi limit (start of last 4K block).
External refresh is operating but system will not reply to refresh command with BRPLYL.

3.2 MEMORY LOCATION PROGRAMMING

MONOSTORE XI/PLANAR LSI-11 ADD-IN PROGRAMMING

STARTING ADDRESS	SWITCH 1	2	3	4	5	6	MSC BOARD MEMORY CAPACITY
000000_8 $0K_{10}$	1	1	1	1	1	1	4K
	1	1	1	1	1	0	8K
	1	1	1	1	0	1	12K
	1	1	1	1	0	0	16K
020000_8 $4K_{10}$	1	1	0	1	1	0	4K
	1	1	0	1	0	1	8K
	1	1	0	1	0	0	12K
	1	1	0	0	1	1	16K
040000_8 $8K_{10}$	1	0	1	1	0	0	4K
	1	0	1	0	1	1	8K
	1	0	1	0	1	0	12K
	1	0	1	0	0	1	16K
060000_8 $12K_{10}$	1	0	0	1	0	0	4K
	1	0	0	0	1	1	8K
	1	0	0	0	1	0	12K
	1	0	0	0	0	1	16K
100000_8 $16K_{10}$	0	1	1	0	1	1	4K
	0	1	1	0	1	0	8K
	0	1	1	0	0	1	12K
	0	1	1	0	0	0	16K
120000_8 $20K_{10}$	0	1	0	0	1	0	4K
	0	1	0	0	0	1	8K
	0	1	0	0	0	0	12K
140000_8 $24K_{10}$	0	0	1	0	0	1	4K
	0	0	1	0	0	0	8K
160000_8 $28K_{10}$	0	0	0	0	0	0	4K

1 = ON
0 = OFF

SIZE	CODE IDENT NO.	DWG NO.
A	51513	100-0046-000
SCALE	REV B	SHEET 10

The computer generated addresses BDAL15L, BDAL14L,BDAL13L, are compared against the programmed switches. If the generated addresses are within the programmed range a memory cycle will be initiated by BSYNCL and BDINL or BDOUTL signals. This circuitry is shown on sheets of the schematic in Section V.

3.3 ADDRESS CHANNEL

When a memory cycle is initiated the information on the lines BDALOL-BDAL15L is immediately latched into a register using the leading edge of BSYNCL.

BDALOL is decoded when a byte mode cycle is to be performed (see ℙ 1.3).

BDAL1L-BDAL6L These address bits are latched and then buffered in order to drive the complete memory array. These address bits are the memory element row addresses. (BDAL1L-BDAL7L are used when a 16K memory element is used.)

BDAL7L-BDAL12L These address bits are multiplexed onto the same internal lines as BDAL1L-BDAL6L at a later time in the cycle. These address bits are the memory element column addresses. (BDAL8L-BDAL14L are used when a 16K memory element is used.)

BDAL13L,BDAL14L These address bits are decoded and buffered to generate the 4K,8K,12K and 16K "row-address-strobe" (RAS/) signals required by the memory elements. The RAS/ pulse then enables only one row of memory elements at any one time thereby preventing interaction of data bits. (BDAL14L,BDAL15L are used when a 16K memory element is used.)

The address channel and RAS/ circuits are shown on sheets 1 and 2 of the schematic in Section V.

3.4 DATA CHANNEL

When a BDOUTL memory cycle (see ℙ 1.3) is performed the write data on the BDALXXL lines is received and buffered

and applied directly to the memory element data inputs. There are no write data registers. The timing of the I/O and memory system is such that write data is loaded into the memory element while data is valid on the I/O lines at the address location latched into registers at the beginning of the cycle (BSYNCL time.)

When a BDINL memory cycle (see ℙ 1.3) is performed the information previously stored in the memory elements is accessed and transmitted onto the BDALOL-BDAL15L lines for use by the computer. There is no read data register, the memory element has an on chip output data register.

A RMW cycle is a combined BDINL and then BDOUTL cycle(see ℙ 1.3).

The data channel circuits are shown on sheets 1 and 2 of the schematic in Section V.

3.5 TIMING CIRCUITRY

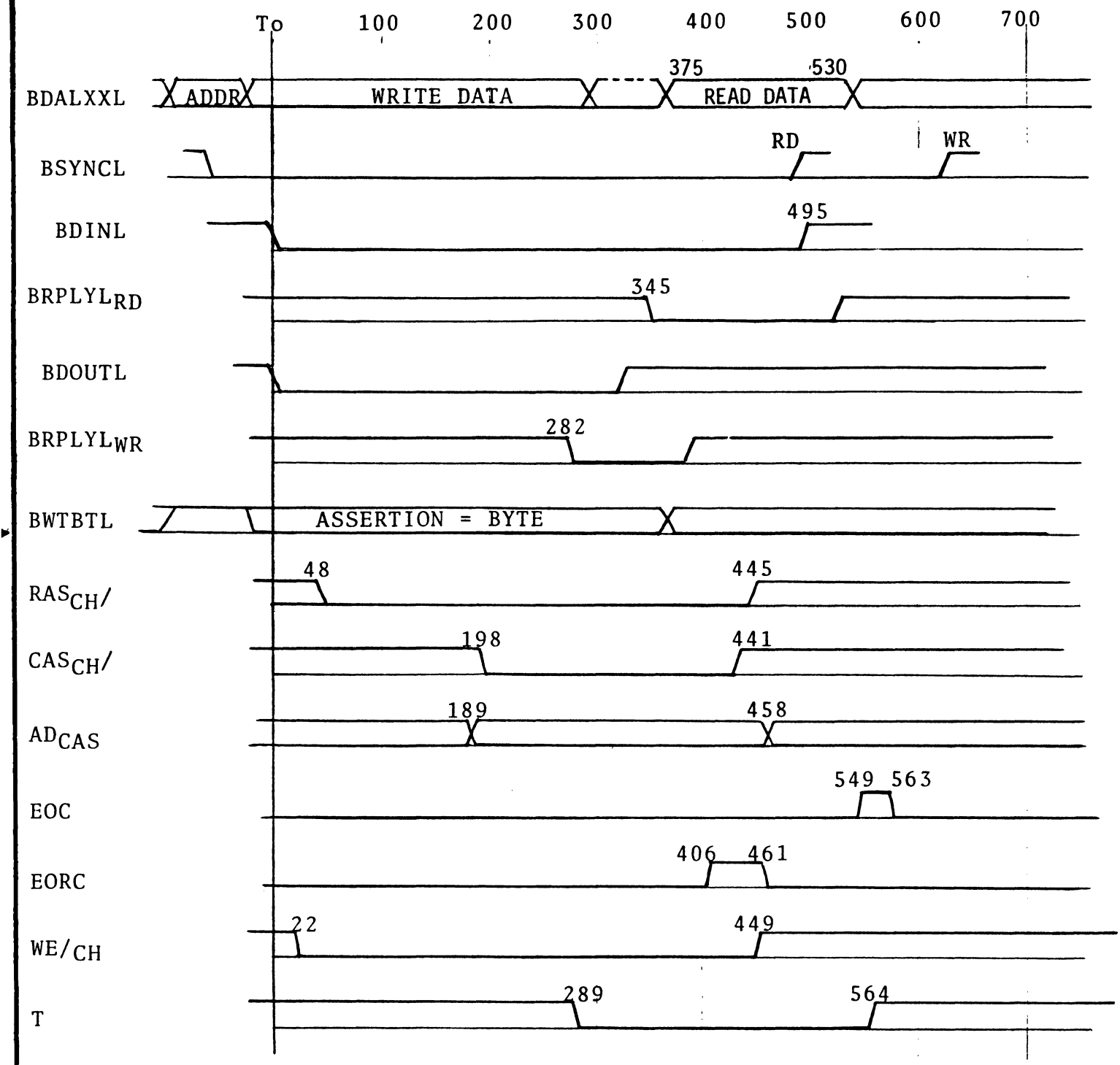
The memory system contains delay line timing circuits which generate, directly or indirectly, all internal and I/O pulses or signals.

The BSYNCL and BDINL or BDOUTL signals are received by the memory system and generate a read or write cycle respectively. If it is a write cycle then BRPLYL is sent back to the master unit signifying receipt of data and address info. If it is a read cycle BRPLYL is delayed until data is on the BDALXXL lines and BRPLYL is then generated telling the master that the data is available.

The circuitry also allows refresh operation to be controlled externally or internally to the memory system. Also the memory can reply to an external refresh command with BRPLYL. Both of the above functions are controlled by switches (see ℙ 3.2). (An invalid operation is to program for internal refresh and allow BRPLYL to respond to a refresh cycle. The computer system will then not function properly.)

The timing circuitry generates pulses according to the following timing diagram:

3.5 TIMING DIAGRAM



	SIZE	CODE IDENT NO.	DWG NO.
	A	51513	100-0046-000
	SCALE	REV E	SHEET 13

There are 2 level transitions which travel down the two delay lines in series. The timing pulses are generated in such a way that the sequence of these transitions and the delay line taps used determine when a pulse will or will not be generated.

The memory elements are dynamic N-channel devices and require refreshing every 2 msec. The memory system uses distributed refresh for internal refresh mode such that a normal cycle may be extended by 700 nsec approximately 2% of the time.

The timing circuitry is shown on sheet of the schematic in Section V.

3.6 DC CONVERTER

The memory system contains a "DC to DC Converter" to convert +12V power to -5V power.

The -5V is generated by first converting the +12V to a nominal 20 Kilo-HZ signal, isolating it, and then rectifying and regulating it for -5V.

The DC converter circuit is shown on sheet of the schematic in Section V.

SECTION IV

MAINTENANCE AND TROUBLESHOOTING

4.1 INTRODUCTION

This section presents troubleshooting instructions for ease of trouble location. Further localization of the trouble is to be found by means of the maintenance drawings in Section V. The theory of operation in Section III should be read and understood, along with a detailed review of the schematics in Section V in order to make effective use of this section.

4.2 PREVENTIVE MAINTENANCE

4.2.1 VISUAL INPSECTION

This inspection includes checking for loose programming wires, components, and discoloration of parts. The inspection should be performed with a minimum of prying or moving of parts.

4.2.2 CLEANING

Cleaning should be limited to removal of excess dust or particles. Never use any abrasive on any part of the gold fingers on the edge connectors. Low pressure compressed air can be used for removing dust or dirt and an aerosol cleaner can be used, with light brushing, to clean the gold contacts.

4.2.3 DC VOLTAGES

The DC voltages should be maintained as follows:

+5V $\pm$ 5% +12V $\pm$ 5% -5V $\pm$ 5%

4.3 TROUBLESHOOTING

To facilitate troubleshooting the following information, cause and effect, can be used to isolate the problem to a particular area. From there on the schematics should be used to determine the exact component that is at fault.

Effect	Cause
Single bit failure all addresses.	Data receiver/driver
Complete byte failure all addresses	BDAL0L circuitry/WE circuitry

Effect	Cause
Complete word failure, all addresses	DC voltages/refresh not working/bus en pulse/BDAL0L circuitry/WE pulse.
Single bit failure, single address.	Memory element
Complete word failure, a 4K section	RAS driver/RAS programming jumpers/address register for A13L and A14L.
Complete byte failure, a 4K section.	RAS driver/RAS programming jumpers/address register for A13L and A14L.
Complete or major part of word failure, 2 addresses	Address receiver/address register/address buffer.
Timeout	Switch programming/BRPLYL not generated/BDAL13L-BDAL15L comparison circuit.
Non-retention of data	Refresh circuit/DC voltages.

SECTION V

DRAWINGS

		EQUIP. REV. LEVEL
ASSEMBLY	303-0156-000	F
SCHEMATIC (LSI-11)	305-0156-000 SHEETS 1 AND 2	
OR		
SCHEMATIC (LSI-11/E1)	305-0156-000 SHEETS 3 AND 4	

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
C	REVISED PER ECO 0489	8/19/76	J.W.
D	REVISED PER ECO 0518	10/13/76	
E	Revised per ECO 0513	11/19/76	
F	Changed Qty. Item #43 From 14 To 10 Per ECO 0551	12/14/76	
G	REVISED PER ECO 0581	2/4/77	
H	REVISED PER ECO 0608	2/24/77	
J	REVISED PER ECO 0615	3/4/77	
K	REVISED PER ECO 0645	5/3/77	

EQUIP. REV. TABLE

DASH # DESIG.	REV.	BATT. VOLT.	NOTE
-001 = 16K x 16	F	12V	
-002 = 12K x 16	F	12V	
-003 = 8K x 16	F	12V	
-004 = 4K x 16	F	12V	
-005 = 16K X 16	F	12VB	2
-006 = 12K x 16	F	12VB	2
-007 = 8K x 16	F	12VB	2
-008 = 4K x 16	F	12VB	2
-009 = 16K x 16	A	12V	3
-010 = 12K x 16	A	12V	3
-011 = 8K x 16	A	12V	3
-012 = 4K x 16	A	12V	3

NOTES:
1.) TABS INDICATE PIN ONE ON ALL I.C.'S AND POSITIVE SIDE ON CAPS.
2.) 12VB IS A USER WIRED BATTERY BACKUP VOLTAGE.
3.) DASH NUMBER FOR OEM CUSTOMER.

REV																															
SHEET																															
REV STATUS OF SHEETS	REV	K	K	H	G	K	J																								
	SHEET	1	2	3	4	5	6																								

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES FRACTIONS DECIMALS ANGLES

MATERIAL

DATE

DRAWN

CHECKED

APPROVED J. Waldinger

APPROVED

MONOLITHIC SYSTEMS CORP.

MSC 4501
ASSEMBLY
MO X1 /PL LSI-11

SIZE	CODE IDENT NO.	DWG NO.
A	51513	303-0156-000

SCALE	REV	SHEET
	K	1 of 6

MSF-1015

QTY/DASH NO.				LIST OF MATERIAL .				ITEM NO.
			ALL	PART NO.	DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	
			1	304-0156-002	P.C. BOARD			1
								2
			8	208-0011-002	RIVETS			3
			11	210-0103-001	I.C. SN7404	U2,5,6,8,9,10,11,12,13 16,33		4
			4	210-0200-001	SN7408 I.C.	U3,4,20,34		5
			1	210-0105-003	SN74S10 I.C.	U7		6
			2	210-0906-003	SN74S85 I.C.	U14,U42		7
			3	210-0100-003	SN74S00 I.C.	U15,17, 36		8
			3	210-0105-001	SN7410 I.C.	U18,46,47		9
			1	210-0908-003	SN74S138 I.C.	U19		10
			1	210-0905-001	SN7483 I.C.	U21		11
			2	210-0716-001	SN74193 I.C.	U22,27		12
			1	210-0307-001	SN7437 I.C.	U23		13
			1	210-0107-003	SN7420 I.C.	U24		14
			3	210-0100-001	SN7400 I.C.	U25, 45,51		15
			1	210-0200-003	SN74S08 I.C.	U26		16
			4	210-0912-003	SN74S153 I.C.	U28,29,30,31		17
			2	210-0803-001	SN7427 I.C.	U32,35		18
			1	210-0504-001	SN74123 I.C.	U37		19
			4	210-0605-001	SN7475 I.C.	U38,39,40,41		20
			1	210-0202-001	SN7411 I.C.	U43		21
			1	210-1102-001	LM304 I.C.	U1		22

SIZE A

CODE IDENT NO. 51513

DWG NO. 303-0156-000

REV K

SHEET 2

MSF-1015

QTY/DASH NO.				LIST OF MATERIAL				ITEM NO.
			ALL	PART NO.	DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	
			1	210-0805-001	I.C. SN7451	U44		23
			1	210-0308-001	SN7438 I.C.	U48		24
			1	210-0804-001	SN7432 I.C.	U49		25
			2	210-1104-002	8640 I.C.	U50,56		26
			4	210-0408-001	DS8641 I.C.	U52,53,54,55		27
								28
			2	223-0001-004	DELAY LINE 9826	DL1, DL2		29
								30
			1	215-0008-006	SWITCH DIP	SW1	8 POSITION	31
								32
			1	216-0003-001	TRANSFORMER	T1	DUAL IN LINE	33
								34
								35
			64	208-0023-001	HEADER, 16 PIN	FOR U101-U164		36
			12	214-0002-025	RES. 10 ¼W, 5%	R7,10,27,28,24,25,18,16 19,21,13,11		37
			1	214-0002-091	RES. 5.6K ¼W, 5%	R6		38
			13	214-0002-065	RES. 470 ¼W, 5%	R5,8,9,12,14,15,17,20, 22, 23,26,39,40		39
			2	214-0002-033	RES. 22 ¼W, 5%	R2,4		40
			1	214-0002-082	RES.. 2.4K ¼W, 5%	R3		41
			1	214-0002-083	RES. 2.7K ¼W, 5%	R1		42
			10	214-0002-073	RES. 1K ¼W, 5%	38,41-44,46-50		43
								44

SIZE A

CODE IDENT NO. 51513

DWG NO. PL 303-0156-000

H

SHEET 3

MSF-1016

QTY/DASH NO. ALL	PART NO.	DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	ITEM NO.
1	214-0002-103	RES. 18K, ¼W, 5%	R45		45
4	214-0002-056	RES. 200 ¼W, 5%	R33-36		46
					47
1	201-0002-066	CAP.0047,50V	C213		48
38	201-0018-002	CAP 2.2μf, 25V	C1-C38		49
58	201-0018-001	CAP 6.8μf, 10V	C39-96		50
113	701-0001-003	CAP .1μf, 50V	C97-C103 C106-C206 C208-C212		51
					52
2	206-0015-001	DIODE IN4934	CR1,2		53
2	217-0004-001	TRANSISTOR 2N3903	Q1,2		54
1	301-0038-001	INDUCTOR 10μH	L1		55
					56
4		ADD JUMPERS (WIRE, 24 GAUGE)	F→H, A→B, K→L, P→R		57
					58
					59
					60
					61
					62
					63
					64
					65
					66

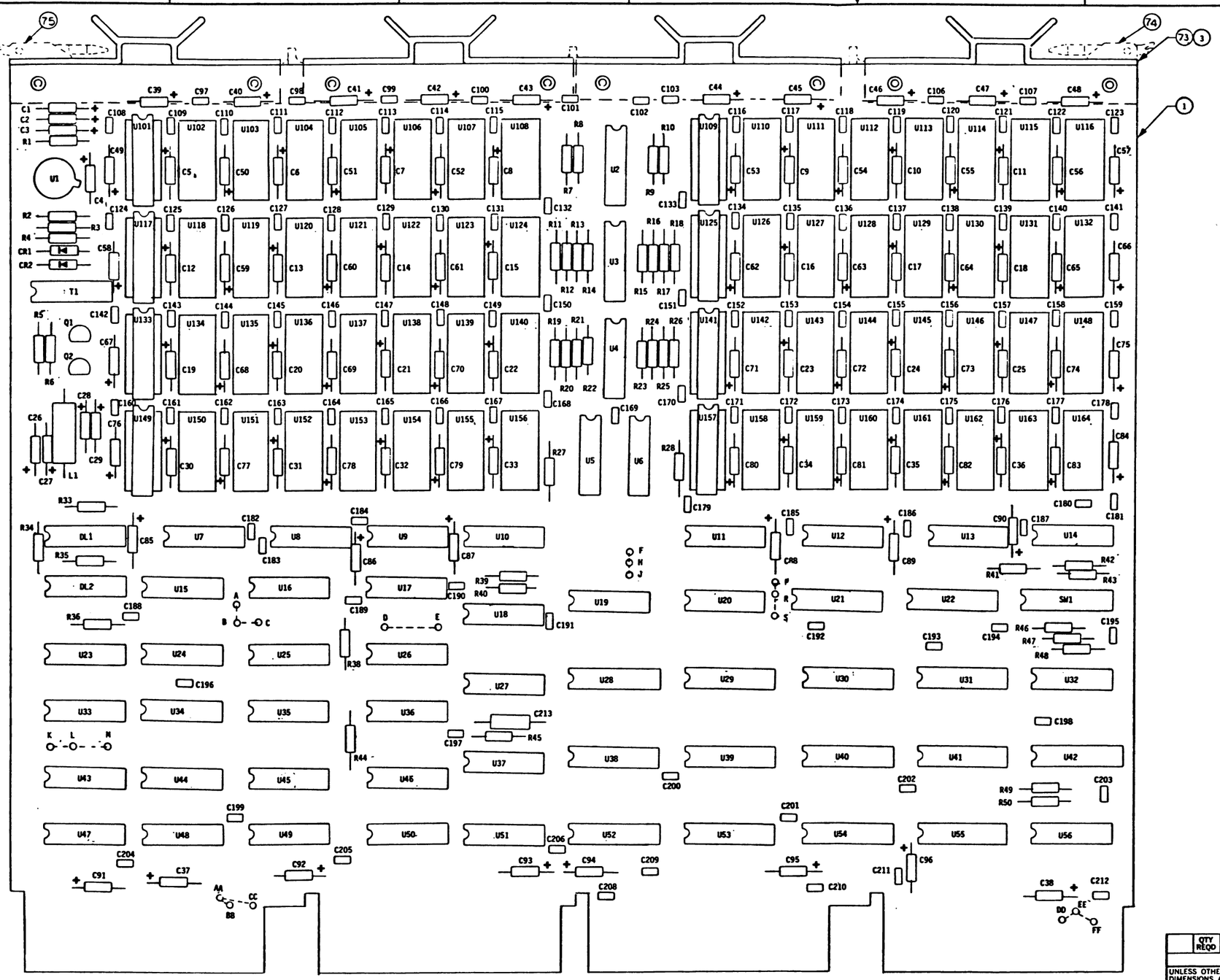
SIZE A | CODE IDENT NO. 51513 | DWG NO. PL 303-0156-000 | G | SHEET 4

MSF—1005

QUANITY PER DASH NO.													LIST OF MATERIAL		ITEM NO.
	-012	-011	-010	-009	-008	-007	-006	-005	-004	-003	-002	-001	PART NO.	DESCRIPTION	
	2	2	2	2					2	2	2	2		ADD JUMPER (20 GA) EE→FF, AA→CC	67
					2	2	2	2						ADD JUMPER (20 GA) EE→DD, AA→BB	68
				64				64				64	210-1000-003	MEM. ELEMENTS MOT. MCM 6604L4 U101-U164	69
			48				48				48		210-1000-003	MEM. ELEMENTS MOT. MCM 6604L4 U117-U164	70
		32				32				32			210-1000-003	MEM. ELEMENTS MOT. MCM 6604L4 U133-U164	71
	16				16				16				210-1000-003	MEM. ELEMENTS MOT. MCM 6604L4 U149-U164	72
					4	4	4	4	4	4	4	4	313-0024-001	CARD PULL	73
	1	1	1	1									302-0122-001	EJECTOR, STIFFENER BAR	74
	1	1	1	1									302-0122-002	EJECTOR, STIFFENER BAR	75
															76
															77

SIZE A | CODE IDENT NO. 51513 | DWG NO. 303-0156-000 | REV K | SCALE | SHEET 5

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

CONTRACT NO.

APPROVALS	DATE
DRAWN TSP	8-19-76
CHECKED	

MATERIAL

FINISH

DO NOT SCALE DRAWING

NEXT ASSY | USED ON

APPLICATION

MONOLITHIC SYSTEMS CORP.

MONO XI/PL LSI-11

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D	51513	303-0156-000	J

SCALE | SHEET 6 OF 6

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	E	ENG RELEASE		
	F	PER ECO 0513	11/23/76	RJH
	G	CHANGED PER ECO 0586	02-04-77	TSP

ARRAY 16K X 16

	13	14	15	16
15	U101	U117	U133	U149
14	U102	U118	U134	U150
13	U103	U119	U135	U151
12	U104	U120	U136	U152
11	U105	U121	U137	U153
10	U106	U122	U138	U154
09	U107	U123	U139	U155
08	U108	U124	U140	U156
07	U109	U125	U141	U157
06	U110	U126	U142	U158
05	U111	U127	U143	U159
04	U112	U128	U144	U160
03	U113	U129	U145	U161
02	U114	U130	U146	U162
01	U115	U131	U147	U163
00	U116	U132	U148	U164
	16K	12K	8K	4K

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION
PARTS LIST			

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FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

NEXT ASSY | USED ON

CONTRACT NO.

APPROVALS	DATE
DRAWN TSP	
CHECKED	

MONOLITHIC SYSTEMS CORP.

SCHEMATIC LSI-11

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D	51513	305-0156-000	G

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

BREFL
CR1
SP380 U50
7437 U23
74S00 U15
ADLA Ø2
1C3 1C6
+5V*
R49 1K
S1
EREFH 1C4
7410 U47
EXT REF REQ 1D4
7408 U20
7432 U49
74S08 U26
RASREF/ 1D3
7404 U16
RREF 1C4
EIREF/ 1C4
7427 U35
7400 U51
BUS EN1 1D8
74123 U37
R45 18K
C213 .0047
AREF/ 1B3
BSYNCLB 1C3
MODEN 1C3
BY 0/1 1A6
BWTBTL AK2
R39 470
R27 10
WE/8-15 3
R40 470
R28 10
WE/0-7 3
BDOUTL AE2
74S10 U7
BDINL AH2
7420 U24
7437 U23
DL2
BO
B1 B5 B7 B10
2D4 2B8
2B8
A8 2B5
R35 200
R36 200
TP5
AD 2B5
A10 2B5
A6 2B5
EORC/ 1A5
B10 2B6
B7 2B6
C
B5 2B6
A5 2B5
DL1
A5 A7 A8 A6
2A8 2C6 2B7 2B6
2D4 1D4
1B2
A0 1D4 2C6
R33 200
R34 200
A10 2C6
M
+5V K L
B1 2B6
A7 2B5
7411 U43
R9 470
R10 10 CAS/ 15 (00-07)
R8 470
R7 10
CAS/ 15 (08-15)
R50 1K
7451 U44
7438 U48
BRPLYL CF2
DF1 +12VB BB
AF1 +12VB DD
DD2 +12V CC
AD2 +12V FF
TP4
AV1, CV1 +5VB
C91, 92, 94, 96 6.8 10V
.1 50V
C102, 169, 183, 188, 189, 191-194, 196, 197, 199, 201, 203-206, 208, 211
GND
TP3
BA2, CA2
C39-49, 57, 58, 66, 67, C75, 76, 84-90, 93, 95 6.8 10V
C97-101, 123, 124, 132, 133, 141, 142, 150, 151, 159, 160, 168, 170, 178, 179, 180, 182, 184-187, 190, 195, 198, 200, 202, 209, 210, 106-108
C103
TP2
AA EE
C5-25, C30-38 2.2 25V
C109, 111, 113, 115, 117, 119, 121, 125, 127, 129, 131, 135, 137, 139, 143, 145, 147, 149, 153, 155, 157, 161, 163, 165, 167, 172, 174, 176, 181, 212
T1
R5 470
R6 5.6K
L1 10µH
Q2 2N3903
Q1 2N3903
CR1 1N4934
CR2 1N4934
R4 22
R3 2.4K
U1 LM304
R2 22
R1 2.7K
C1 2.2 25V
C2 2.2 25V
C3 2.2 25V
C4 2.2 25V
C26 2.2 25V
C27 2.2 25V
C28 2.2 25V
C29 2.2 25V
C50-C56 59-65 68-74 77-83 6.8 10V
.1 50V
C110, 112, 114, 116, 118, 120, 122, 126, 128, 130, 134, 136, 138, 140, 144, 146, 148, 152, 154, 156, 158, 162, 164, 166, 171, 173, 175, 177
-5V
+12V
TP1 TP6
GND
AC2, BC2, CC2, DC2, AM1, BM1, CM1, DM1, BJ1, CJ1, DJ1, AT1, BT1, CT1, DT1

BDMGIL AR2 CR2 AS2 CS2 BDMGOL
BIAKIL AK2 CK2 AK2 CK2 BIAKOL

ARRAY SUPPLY PINOUTS	
SUPPLY	PIN NO.
+5V.	9
+12V.	8
-5V.	1
GND	K

COMPONENT	HIGHEST #	NOT USED
IC'S	U164	U56-U100
CAPACITORS	C212	C160-C170, C207
RESISTORS	R50	R29-R32
TRANSISTORS	Q2	
DIODES	CR2	

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MATERIAL

FINISH

CONTRACT NO.

APPROVALS	DATE
DRAWN TSP	
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MIC SYSTEMS CORP.

SCHEMATIC LSI-11

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D	51513	305-0156-000	G