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SUBJECT: THE CADAC COMPUTER

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Abstract: The CADAC is a slow speed general purpose digital computer designed and built by the Computer Research Corporation of Hawthorne, California. It is an automatic-sequence-controlled, serial machine having a magnetic drum memory. It operates with a word length of 42 binary digits and requires an average of about 70 milliseconds to carry out one command. Fourteen different commands are provided. To avoid conversion problems, all numbers are handled in octal form throughout the machine. Program instructions must be prepared in this form for insertion on a special keyboard and results also are obtained in this form through an output typewriter. Plans were made for future addition of a magnetic tape input and output device.

A goal set for the design of this machine was to minimize the number of vacuum tube circuits used. A large reduction in the number of tubes required was achieved by the use of recirculating registers on the magnetic drum and the use of crystal diode circuits for the logical networks. From an operational standpoint, it appears that the advantages of a fewer number of vacuum tube circuits are offset to some extent by the potential weaknesses in the extensive crystal diode networks. The CADAC has only 195 vacuum tubes but about 2500 crystal diodes.

A unique approach to the system design problem was applied in the development of the CADAC. All operations to be accomplished were first described in logical equations using the notations of Boolean algebra. The set of equations obtained defined the input conditions for each flip-flop and each drum-memory channel for all steps of a command. They, therefore, also defined the configurations of "and" and "or" circuits needed to control the states of the memory elements, so it was a straightforward matter to synthesize the crystal diode networks. The technique of using equations to describe

the system operation not only proved successful in the machine design but it also has been found useful in maintenance and trouble-shooting work.

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1.0 INTRODUCTION

The CADAC is a general purpose slow speed automatic sequence controlled computer designed and built by the Computer Research Corporation of Hawthorne, California, for the Air Force Cambridge Research Laboratories. At the inception of this machine the general attitude of computer engineers was that electronic computers could not be designed with fewer than thousands of electronic tubes without sacrificing useful word length. The Computer Research Corporation departed from this philosophy and has succeeded in building a relatively inexpensive (Fortune magazine quote: "$80,000"), very compact machine. The designs and design techniques that overcame the engineering obstacles met in this computer deserve considerable respect, and the CADAC, as a practical product of these motives and techniques, is of interest to personnel associated with other computer projects.

2.0 LOGICAL CHARACTERISTICS AND DESIGN

2.1 External Characteristics

CADAC, properly programmed, will perform arithmetic and logical manipulations on digital quantities within the range $-(1-8^{-12}) < x < (1-8^{-12})$. It operates with serial techniques on words fourteen octal digits (forty-two binary digits) long with a fixed binary point. There are fourteen three-address commands with a mean operating time of seventy milliseconds per command (about 15 commands per second).

The magnetic drum memory has a capacity for 1023* words with a mean access time of 14 milliseconds. There are 16 channels, each of which contains 64 words around the circumference of the drum.

The input device now associated with the computer is an eight key keyboard on the control panel. These keys are used for entering octal numbers. The output typewriter prints one to four columns of octal figures across a page. Either the contents or the address and contents of any memory register may be printed out. These accessories do not lend themselves readily to decimal computation and the input is both tedious and slow. However, the machine has been wired with internal circuits which will enable it to read in from and read out to an external magnetic tape unit although none was provided with this model.

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* Because of the nature of the multiplication and division process register #0 is not used for a memory location.

2.2 Applications

This machine by virtue of its long word length is capable of obtaining results to a precision of about 11 decimal digits. The three-address-code system, while seemingly redundant to Whirlwind programmers, is necessary to a machine with no arithmetic registers. It also equips the machine to perform certain operations with a saving in the number of registers required for commands. This long word length and economical use of register space, combined with a main storage consisting of 1023 consecutive registers yields a computer potentially adapted to most types of general computation, and with proper external equipment to some types of slow speed control operations.

2.21 Number Representation

Positive and negative numbers, N, are represented with a 2 octal digit sign followed by $N \times 8^{-12}$. The sign convention is:

00 negative number
01 positive number
02 negative number indicating arithmetic overflow
03 positive number indicating arithmetic overflow

The machine interprets all commands as positive numbers when they are modified by arithmetic processes.

2.22 CADAC Order Code

The command is divided into four sections, an instruction consisting of 2 octal digits, and three addresses (m_1, m_2 & m_3) of four octal digits each.

These instructions perform the following functions:

Octal Code	Instruction and Abbreviation
37	Halt: (H) Stop the computer
35	Fill: (F) Read from an external unit during program operation. As yet this order is not defined in either logical design or circuitry.
33	Write addresses and associated words on external tape unit: (P_1) Start with register m_1 and continue for the next n registers where n is m_3. The logical designs and circuitry are complete, but the external unit has not been provided with this model.

31 Type addresses and associated words: (P_2)
The address convention is the same as in the tape order.

27 Write word only on external tape unit: (P_3)
The address convention is the same as above.

25 Type word only: (P_4)
The address convention is the same as above.

23 Test overflow: (T_o)
Investigate the contents of register m_1. If the sign indicates an arithmetic overflow, set the control number to m_3.

21 Test difference: (T)
If the contents of register m_1 is greater than the contents of register m_2 set the control number to m_3.

17 Extract: (E)
From the contents of register m_1, extract those digits which are in coincidence with the binary "ones" of the contents of register m_2 and insert those digits into register m_3, leaving the rest of the contents of register m_3 unchanged.

15 Subtract: (S)
Subtract the contents of register m_2 from the contents of register m_1 and put the difference in register m_3. If the absolute difference exceeds one, indicate an arithmetic overflow.

13 Add: (A)
Add the contents of register m_1 to the contents of register m_2 and put the sum in register m_3. If the absolute sum exceeds one, indicate an arithmetic overflow.

11 Shift: (Sh)
Shift the contents of register m_1, left if the contents of register m_2 is positive or right if the contents of register m_2 is negative, the number of binary digits indicated in the magnitude of the contents of register m_2 (this model will shift as often as the contents of m_2 indicate, extraneous shifts included) and put the shifted result in register m_3. If any

significant digits are shifted off the left end indicate an arithmetic overflow.

7 Multiply: (M)
Multiply the contents of register m_1 by the contents of register m_2 and put the product rounded off to 12 significant octal digits with its proper sign into register m_3. No provision has been made for double register multiplication.

5 Divide: (D)
Divide the contents of register m_1 by the contents of register m_2 and put the quotient rounded off to 12 octal digits with its proper sign in register m_3. If the absolute quotient exceeds one, indicate an arithmetic overflow.

2.23 Operating Instructions

There are sixteen switches, buttons and keys on the control panel.

(1) AC power switch
(1) Drum motor power switch
(1) B/ power on button
(1) B/ power off button
(1) Start computation key
(1) Clear key
(8) Octal digit keys
(1) Tab key which fills octal number in storage
(1) Space key which selects storage position for filling and starting computation

The machine is cycled on in the order: AC Power; Drum motor power; when the drum reaches speed, the stop button is held down and the "B/ on" button is pressed. The typewriter motor is turned on by its own switch at any time.

To fill a program the first storage address is set up by entering the address on the octal keyboard and pushing the "space" button. The contents of the first register is then entered on the octal keyboard and the "tab" button pushed. The machine automatically steps one storage register for each push of the "tab" button so that it is necessary to set up the address of only the first storage register. Any error on the octal keyboard before the "tab" button is pushed can

be remedied by reentering the correct number right on top of the old number, then tabbing. Any error after tabbing can be remedied by setting up the address of the incorrect storage register and replacing the contents with the correct value, then continuing.

To start a computation enter the control number (address of order to be operated on) followed by four zeros and push the space button, then push the "start" button. The "clear" button will halt any operation at any time.

A specimen program is included in the appendix.

2.3 Internal Characteristics

2.31 Building Blocks and Stable States

The two binary states are represented in the machine as two separate dc voltage levels, each of which is maintained by diode clamping throughout the machine. The higher voltage level, E_H, is used to represent a "1" and the lower level, E_L, is used to represent a "0". Four component combinations are used for the logical building blocks utilized by the machine to maintain the logical voltage levels:

(1) The bistable flip-flop which can be set to "0" or "1" but cannot be complemented. It has cathode follower drivers whose outputs are clamped to either of the two voltage levels (see Figure 1).

(2) The logical product circuit ("and" gate), i.e., both inputs must be at the high voltage level for the output to be at the high voltage level. (Figure 2)

(3) The logical sum circuit ("or" gate), i.e., if either input is at the high voltage level then the output will be at the high voltage level. (Figure 3)

(4) The logical negative circuit, i.e., the output voltage is at the high level if the input voltage is at the low level and vice versa. (Figure 4)

Every logical voltage level starts as the output of one side of a flip-flop. These voltage levels are returned through combinations of the sum, product and negative circuits to the inputs of the various flip-flops in the machine. These inputs are termed "propositions", being in effect true or false (one or zero, plus or minus etc.) logical propositions. As the various flip-flops in the machine assume different

combinations of their bistable states, different configurations of voltage levels appear at the various inputs. The table of Figure 5 shows the results obtained from the basic logical operations.

2.32 Clock Pulses and Flip-Flop Triggers

A combination of components of the type indicated in the last paragraph becomes practical when a new stable configuration of voltage levels can be derived from the preceding configuration as a function of it. If a square clock waveform fluctuating between the two logical voltage levels with some standard frequency is introduced, time boundaries between the desired configurations can be developed and defined. The flip-flops can then be triggered by logically multiplying the proposition voltage levels on the inputs of the "one" and "zero" sides of a flip-flop by the clock waveform and passing this through the proper differentiating circuit. If the input proposition is false, i.e., at the lower voltage level, the clock rise and fall will have no effect on the grid of the particular side of the flip-flop in question, but if the input proposition is true, i.e., at the higher voltage level, as the clock pulse falls, the flip-flop will be triggered. Thus the clock provides both a timing system and a dynamic trigger on the grid of a flip-flop tube controlled by the propositions from the network of sum and product circuits.

2.33 Elements Governing Design

The major factors governing the design of the computer were the decisions to use serial operation and magnetic drum storage. The main memory is the magnetic drum 12 inches in diameter rotating on a vertical axis at about 40 rps. It has 22 useful channels: 16 storage channels capable of holding 64 words each, 3 channels associated with three recirculating arithmetic registers, and three channels permanently recorded: the clock pulse channel, a word reference channel, and a start synchronizing pulse channel. Access to the memory is through read-record heads mounted within 0.001 inches of the drum. A channel is selected by means of a flip-flop controlled matrix and the time position identified by comparing the contents of a group of flip-flops against the word reference channel. The permanent channels can only be read from, not read into.

The three recirculating registers each consist of record head and a read head on the same channel located so that a point on the spinning drum passes the record head first. They are spaced and interconnected so that a particular signal, when recorded, will be carried by the drum to the read head,

passed through the circuitry, and rerecorded 42 clock pulses later (Figure 6). The circuitry controlling the record head inputs is the logical diode net which is in turn controlled by the outputs of the read heads of the recirculating registers and of the main storage, and also by the outputs of the control panel. When an arithmetic operation is complete the answer is contained in a recirculating register whence it is immediately transferred to storage and the register cleared. There are no arithmetic registers in the Whirlwind sense; all results must be placed in some storage register immediately. The recirculating registers are used in all arithmetic, searching, and control operations, blending strings of data 42 pulses long as a spinning machine twists many strands into a thread.

2.34 Control

2.341 Nature of Operation Sequences

The execution of a particular coded command consists of several separate operations performed in order: the command must be looked up and identified, memory registers referred to, arithmetic processes completed, and results returned to storage. These operations, logically arranged in a minimum order, take the form of a flow diagram when described pictorially. (Figure 7)

When a program has been filled into storage a control number set, and the start button pushed, the machine proceeds serially through the separate operations as indicated in the flow diagram, first looking up the command, then testing it serially to determine which order to execute, then following through the execution until finished, and finally searching for the next command.

Most of the operations take many separate steps of one word-time (the time it takes 42 clock pulses to pass through a recirculating register, or one sixty-fourth of one revolution of the drum), and for the actual design of the computer a more elaborate flow diagram was drawn indicating each separate operation as a group of steps one word time long. Each separate step is shown as a small box which describes the function it performs and also contains a reference to the configuration of switching necessary in that word time. These steps are numbered consecutively and grouped by operation. At the end of one operation, the operation

starting with the next consecutive step is performed unless the control is transferred to an operation starting with a step having a known, but not consecutive number. This resembles the flow diagram of a normal coded program for a computing machine with commands, conditional subprograms, and subprograms.

2.342 Control of Sequences

As any computer requires a counter to keep track of the address of the next instruction, the CADAC requires a counter to keep track of the process by which it carries out a command. The designers of CADAC called this internal counter a "program counter" and constructed it from eight presetable flip-flops. Most of the 2^8 possible configurations (some are not used) of these flip-flops refer to a step in the master flow diagram, and each configuration can be used to produce a "true" voltage level at any point in the machine. Thus any portion of the diode net can be gated in for one certain step, or for steps which perform identically. However, each step lasts one word time which allows 14 octal digits of three pulses each to pass by. It is necessary to split the words into octal digits in order to isolate the orders from addresses and the signs from magnitudes. Therefore, a four flip-flop counter (the "O" counter) is employed which counts octal digits from 0 to 13, then resets itself again to zero. From this it is possible to gate in any portion of the logical net for any particular octal digit or any group of octal digits of a word time. It is also often necessary to select a particular binary digit in an octal digit. A two flip-flop pulse counter (the "P" counter) is employed which counts pulses from 0 to 2, then resets itself again to zero. From this it is possible to gate in any portion of the logical net to a particular pulse of an octal digit.

2.343 Control in a Specific Operation

For an example of the computer control mechanism, let us see how the machine knows when to use the process which determines the sign of a product. The product sign is a function of the sign digits of the two factors. The logical circuit for this process is synthesizing the function for every pair of pulses that pass through two of the recirculating registers. However, this function is gated further into the net only on the first pulse (P_0) of each octal digit. The function is then gated

to the next level of the net only on the 13th octal digit (0_{12}) of each word time. And finally it is gated onto the record head of the recirculating register which contains the product only during the 52nd (PC #52) step of the master flow diagram, the roundoff step of the multiplication operation.

2.35 Outlining the Circuits

CADAC was designed to be physically small, so a saving in equipment at the expense of requiring the components to serve more than one purpose was feasible. Certain overlapping of components' uses is obvious, since the machine is never printing, selecting a channel, shifting, adding, etc. simultaneously. This necessarily led to very complicated interconnections of the diode network and the flip-flops.

For convenience in determining what interconnections were required, the notation and laws of Boolean algebra were applied to define the inputs of each flip-flop and of each record head in terms of the outputs of the logical flip-flops, the outputs of the three sets of counter flip-flops (P counter, O counter and Program Counter), and the clock pulses. No block diagrams were used at any stage. Equations were written for the inputs of each side of every logical flip-flop and record head for each step in the entire master block diagram. Certain equations reappeared frequently throughout the machine, so each equation was number coded for reference and written on an "operations numbers chart". The separate equations for the inputs of each flip-flop and record head were then combined and reduced to final equations of the apparently most electronically feasible form. Care was taken that no flip-flop was ever pulsed on both grids simultaneously.

From the above mentioned equations an outline of the diode network circuit could be drawn immediately without hesitation. A more complete discussion of this method is "Techniques in the Design of Digital Computers" by Richard E. Sprague of the Computer Research Corporation. A copy is available in the Digital Computer Lab library. Such an outline indicates the relative location of all logical crystals, diodes, resistors, and flip-flop units. Then for the actual circuit design, it is necessary to calculate the proper resistance values and to insert power amplification where needed. This is discussed in section 3.4 of this report.

The equations, combined with the flow diagram, give a complete picture of how the computer operates and, because of their convenient cataloging, they facilitate the location of errors. It is difficult for a person weaned on block diagrams

and their proximity to circuit schematics to appreciate this at first, but only a small amount of familiarization with the technique enables a beginner to apply the method to the building blocks of the CADAC.

3.0 MECHANICAL AND ELECTRONIC CHARACTERISTICS OF CADAC

3.1 Physical Description

The CADAC computer occupies a space of approximately 35 cubic feet and weighs about 500 pounds; it is divided into two sections. The lower section consists of the main power supply, the fan motor, the drum motor, and a smaller selenium-rectifier power supply to deliver the 100 v. D.C. required by the drum motor. A variac on the input to this power supply serves as the motor speed control. The upper section of the computer consists of the 12" diameter magnetic drum, with its associated heads, read-record amplifiers, read-out flip-flop, circulating register flip-flops and clock pulse generator. These circuits are mounted in sub-assemblies located around the drum. Also in this section are the input-typewriter relays. On four large phenolic boards surrounding the upper section of the machine are mounted all the crystal diodes used in the logical diode networks as well as those used for clamping. There are approximately 2500 crystal diodes mounted on these boards. All of the flip-flops and driver tubes not associated with the memory are mounted horizontally around the top of these boards. Most of these tubes are in the circuits of the three counters and their associated drivers. The "logical" voltages for the computing system and those which exist throughout the diode nets are -125 v. (E_H) for "true" (one) and -100 v. (E_L) for "false" (zero). It must be remembered that the computer operates on a non-return-to-zero basis, and that voltage remains constant at -125 v. as long as there is a serial group of one's and -100 when there is a serial group of zero's. These voltages are D.C. coupled throughout the diode nets. If the output of the net is true or at -125, it will gate the negative going edge of a clock pulse, permitting it to trigger one side of a flip-flop.

3.2 Power Supply

The computer requires a power input of 3KVA, 110 v. A.C., 60 cycles. This is non-regulated and comes directly from the power line. All of the inputs to the power transformers are fused with the conventional cartridge type fuses. The power transformers have tapped primaries, and by choice of the proper tap, the system can be operated with any line voltage that falls in the range from 105 volts to 125 volts. The main power supply is of the bridged-

selenium-rectifier type; it delivers ≠300 v. d.c. unregulated. From this voltage, the following regulated d.c. voltages are derived: -300 v. (400 ma.), ≠225 v. (2.6 a), ≠125 (450 ma.), ≠100 (1 a). Operation of the two power switches turns on the filaments of all tubes and energizes the drum and fan motors. Throwing the "d.c. on" switch energizes the master time delay relay which applies the voltages to the computer in the sequence listed above. Incorporated in this power supply is an 884 control circuit which does not permit the time delay relay to energize unless all the voltages are present and are within 5 v. of their proper values with reference to the -300 v. The supplies have conventional series regulators using 6AS7's for the current control tube and a 6AU6 and a VR-105 for voltage control. There is a small additional power supply which supplies -240 v. to a balanced inverter-cathode-follower stage which feeds the drivers for the read-out flip-flops.

The supply for the drum motor is nominally ≠100 v. D.C. which draws a starting current of 3.8 a and a running current of 1.8 a. The A.C. input to the supply is variac controlled to control the speed of drum rotation. The speed is nominally 40 rps but is not especially critical since the 100 kc clock pulses are derived from the permanently recorded clock channel on the drum. The lower limit of drum speed is reached when the amplitude of the read signal is too low to trigger the read-out flip-flop. The upper limit of speed is reached when the frequency of the read-out pulses is so high that flip-flops will not reach their stable states before they are triggered again.

3.3 Vacuum Tubes

There are 195 vacuum tubes in the CADAC, about 30 of which are in the power supply, 65 in the memory circuits and 100 in the arithmetic center. There are 31 flip-flops in this machine for which 12AT7's are used exclusively. Below is a chart of the tube count in the arithmetic unit:

8	decision flip-flops	12AT7
6	decision flip-flop drivers	5687
6	pulse and digit counter flip-flops	12AT7
6	pulse and digit counter flip-flop drivers	5687
5	extra pulse and digit counter flip-flop drivers	5687
8	program counter flip-flops	12AT7
18	program counter flip-flop drivers	50L6
5	typewriter relay drivers	5687
1	memory flip-flop	12AT7
1	memory flip-flop driver	5687
1	carry flip-flop	12AT7
1	carry flip-flop driver	5687
10	cathode follower drivers	12AT7

12 recirculating register flip-flops	12AT7
7 recirculating register flip-flop drivers	5687 and 12AT7
4 phase inverters	12AT7
4 clippers	12AT7
1 start F.F.	12AT7
3 drivers (clock etc.)	5687

The 12AT7 was chosen for use as a flip-flop because it has a high G_m, hence a small grid swing from zero bias to cut-off (0 to -4.5 v.) which makes it quite easy to trigger, and also because it is a miniature. The 5687 was chosen for drivers because it will supply more current with +100 v. on the plate at zero bias (42 ma.) than any other miniature type. For the program counter output, which must deliver more current to the diode nets than the 5687 can provide, the 50L6 was used. This tube will deliver 106 ma. at 100 v. and zero bias. The tubes for the flip-flops and drivers listed above are not especially selected or matched. There is no provision for marginal voltage tests nor are there any particular acceptance tests for tubes. A conventional tube tester is used for determining when tubes should be replaced. The heater voltages for all tubes are applied directly with no warm-up time. With the exception of the 50L6 and 50C5 tubes, nominal values of heater voltage are used. The 50 volt heaters are wired in series-parallel across the line and are operated at about 45 v. Little trouble has been experienced from filament burn-out from these high-voltage-filament type tubes. There has been no data on the reliability of these tubes since the computer has not been operating long enough to gather such data.

The list of tubes associated with the memory is tabulated below:

32 record tubes - main memory	50C5
6 record tubes - E,F,G, one word circulating registers	50C5
19 pre-amps - main memory	6AS6
4 pre-amps - E,F,G, recirculating registers and main memory	12AT7
2 amplifiers for clock	12AT7

Since push-pull recording is employed on every drum channel, the choice of the 50C5's is the most critical. They are carefully selected as a matched pair for both plate current at zero bias and for cut-off voltage. All circuits have been designed so that they will still operate with about 25% decrease in tube emission. Most of the flip-flops feed 5687 drivers whose plates are returned to +225 through their plate load resistance. Since the driver plates are clamped at +100 and +125 volts by means of crystal diodes, the variation in plate current can be quite wide before the plate circuit will fail to switch from one clamped voltage to

the other. Flip-flops are well within their plate dissipation. The 12AT7 flip-flop "on" side with a 12K plate load to -225 v. will normally dissipate about 1 watt and the tube is rated for 2.5 watts per section. The 5687's, however, when conducting, have their plates clamped at -100 v. Under this condition, their dissipation is close to the rated value of 4 watts.

3.4 Crystals and Crystal Nets

3.41 Use of Crystals

Type 1N52 crystal diodes are used almost exclusively throughout the computer both for the logical net and for clamping of driver plate circuits. They are all carefully selected for minimum back current and low forward drop. All diodes are checked and must have less than 3 v. forward drop at 25 ma. For all logical diodes the back current must be less than 100 μa at 25 v. while the clamping diodes are unacceptable unless they pass less than 200 μa back current at 25 v. There is no consideration for crystal noise. The action of the diodes and how they are used can best be shown by an example. In the product circuit (Figure 2) the voltages P_1 and P_2 must both be high or at 125 v. for the output to be high. If either P_1 or P_2 is at -100 v. one of the net diodes will conduct more heavily, lowering the output to -100 v. In the sum circuit (Figure 3) either P_1, or P_2, or both can be high and the output will rise to -125 v.

The logical network of Figure 8, which is a combination of the sum and product nets shown in Figures 2 and 3, expresses the logical proposition $(P_1P_2 + P_3)C$ as its output. If the proposition $(P_1P_2 + P_3)$ is true, i.e., if point Y is at -125 v., point Z will follow the clock input, C, as indicated by the waveforms. The voltage at point Z is differentiated so that a negative pulse coincident with the trailing edge of the clock pulse is obtained to trigger a flip-flop. In considering the forward drop of the diodes in the above circuit, it can be seen that there is just as much gain in d.c. level as there is loss. For example, assuming a 2 v. forward drop, point X will be at 127 v. Point Y will drop again to 125 v. and so forth. From a static point of view at least, it appears that an indefinite string of sum and product terms are possible. For a string of just products, or just sums, however, there will be a definite signal deterioration, depending upon the forward resistance of the diodes and the current permitted to flow through them. In the CADAC, the average forward current is from 5-10 ma. and not more than 7 or 8 terms are used in any one net.

3.42 Computation of Resistor Values

The selection of R_1 (Figure 8) is based on the input capacitance of the following stage and the required time necessary to allow the d.c. level to rise to its final value. When the clock voltage rises from -100 v., it immediately cuts its diode off and the voltage at the junction will rise exponentially toward 225 v.; the time at which it reaches 125 v. is determined by the value of R_1 and the shunt capacitance. For driving one flip-flop, with an assumed input capacitance of 10 $\mu\mu$f, it is found that for R_1 =1 meg, the output voltage reaches its final level in about 3 μs. The worst load condition (when the value of i_1 is greatest) is when the voltages at all the junctions are low. Then $i_1 = \frac{225-100}{R_1} + i_{b_1}$. In this respect the back current of the clock diode is critical, so that this diode is chosen for the minimum back current at 25 v. It is assumed to be 100 μa as a safety factor. R_2 is now selected on the basis that the drop across it should not exceed 100 v. with i_1 flowing through it. Therefore, $R_2 \leq \frac{100}{i_1}$. The greatest i_2 will flow into the sum network when the point X is high so that $i_2 = \frac{125}{R_2} + i_{b_2}$.

Now since R_2 is less than R_1 the back resistance of the diode through which i_{b_2} flows need not be as high as that of the clock diode. Here again the crystal back current is also assumed to be 100 μa. As before, R_3 cannot have a drop of more than 100 v. so $R_1 \leq \frac{100}{I_2}$. The equations for R_1 and R_2 are similar because the values of 125 v. and 100 v. were chosen to be symmetrical between 225 v. and ground. In the same manner currents in the clamping diodes are calculated.

3.5 Other Components

All of the low wattage carbon resistors in the CADAC are 5% Allan-Bradley units. However, in the places where d.c. coupling occurs, such as from a flip-flop to its associated driver, and in cathode follower inputs, 1% Nobeloy precision resistors are used. Standard commercial components are used throughout the computer, including electrolytic capacitors for power supply filters and decoupling networks. The coupling capacitors to flip-flops and those in the memory circuits are mica postage-stamp type. Paper capacitors are also used in several places for decoupling. The relays in the power supply are specialized timing relays, and the typewriter relays are standard 150 v. d.c. Spark suppression across the typewriter relays is necessary, and these relays must

be carefully adjusted to eliminate bouncing of the contacts. No twin contacts on relays or any redundant circuits are used to increase reliability.

3.6 Circuits

3.61 Flip-Flop Circuits

There are 31 flip-flops used in this computer. The circuit diagram of one with its associated driver is shown in Figure 9.

The only load on a flip-flop is a high current driver, which feeds into the diode net. The output of the driver is clamped between -125 and -100 volts. After differentiation and clipping, the input to the grids is a 13-14 volt negative pulse. The -3 v. return of the differentiating circuit is employed to clip out any hash or noise which might be generated in the nets. This reduces the effective negative driving voltage by a few volts, but there is still plenty of amplitude available. The grids are clamped at -8 v. to inhibit negative overshoot in the grid circuit and bring about rapid recovery to its stable state. The plate swing is from -90 to -160 volts, causing the on tube to draw grid current, which tends to stabilize the circuit. With the d.c. coupling employed, the grid swing on the driver is from -40 v. to -0.5 v. There is not much consideration for switch-over time since there will be a minimum of 10 μ s before it is necessary for flip-flops (in combination with other propositions) to gate the trailing edge of the clock pulse. No steps have been taken to insure matched sections in the flip-flop tubes, nor have there been any data taken on tube deterioration and how much unbalance is allowable before failure of the flip-flop occurs.

3.62 Read-Record Circuits

The main memory employs center tapped heads and push-pull recording, with the one's being recorded by one miniature pentode (5OC5) and the zero's by the other. Since the record currents are too large to switch, two record tubes are required for each of the 16 main storage channels. The read signals are taken off the same heads by capacitance coupling to one side of the recording winding. The signals obtained (about 0.4 volt amplitude) are amplified, and gated in 16 6AS6's, all of which have a common plate connection. The read signal is then applied to the "M" (memory) flip-flop which reconstructs the d.c. signal level as recorded on the drum. The read-record circuit is shown in Figure 10. The 5OC5's are critical and are a matched pair, so that the "one" and "zero" record currents are equal. The current is sufficient to

saturate the drum in either direction. If one of the 5OC5's becomes weak there is danger of not erasing the old information on the drum.

Since the fall of the clock pulse initiates both the one and zero record pulses, a delay equivalent to half the length of a clock pulse is necessary in the read-out circuit. Without a delay, the trailing edge of the clock pulse might occur while the "M" flip-flop is switching.

The reading amplifier can tolerate a 10% reduction in gain before the drive to the "M" flip-flop is affected. The bandwidth of the reading amplifier is in the order of 300KC. Most of the plate supply decoupling, shielding, etc. is done in the memory read-out circuit. There is no problem here of p.r.f. sensitivity since d.c. coupling is used in the channel whenever there are unidirectional pulses.

3.63 Cathode-Follower Circuits

In many places throughout the diode net cathode-followers were inserted so as not to invert the logic as does the driver (Figure 11). It has a high impedance input so can be economically used in circuits already working at a high impedance level. It is inherently self-clamping, and when returned to the large negative voltage, the amplitude loss is negligible.

3.64 Permanently Recorded Channels

Special equipment is required in the initial construction of the machine to record the three permanent channels on the drum. The most elaborate of these is the word channel, since the octal digits from 0 to 63 must be recorded circumferentially around the drum. It is also necessary to permanently record the clock channel on the drum. This is done in the following way: a 100 kc sine wave from an accurately calibrated source is fed into a counter which gives an end-carry pulse each 2688th cycle. The speed of the drum is then carefully adjusted to obtain one revolution per end-carry from the counter. When the speed is properly adjusted, the 100 kc signal is recorded for one revolution of the drum. In operation in the computer, the clock pulse is sensed, amplified and applied to a Schmitt circuit which provides the 100 kc square wave as a common "proposition" throughout the logical net.

The other permanently recorded channel is called the start-pulse channel. It gives a pulse at the beginning of every word time. It is used to synchronize the pulse and octal digit counters on the beginning of a word time when the machine is started. Thus the proper timing propositions can be utilized to select any pulse in any given word time, as has been described previously.

4.0 TESTING AND TROUBLE-SHOOTING

4.1 Methods of Trouble-Shooting

It is very difficult in this machine to use standard signal tracing techniques in tracking down trouble. Checking is done by means of the logical equations, from which it can be determined what voltage level must be present at a certain point in the machine at a specific time. For example, if the program counter "hangs up" at a particular block in the flow diagram, one can tell from the equations what sequence of gating is necessary and where the gates should come from, in order for program counter to continue its normal sequence. By referring to the schematic diagram, and by judicious pulling of key crystal diodes on the board, portions of the logical net and circuits can be isolated and the trouble traced.

It is possible to observe what happens, to some extent, by continually repeating a part of the program and watching the waveform of the suspected circuit with an oscilloscope, or one can check voltage levels throughout a part of the net. Suspected diodes can be checked by the crystal checker to see if any deterioration had occurred and if the diodes meet the required standards. Incorporated on the diode board are a group of switches which will permit the program to "jump" into a particular program count, or go on to its completion. By setting another group of switches, the program can be made to jump back into the rest position. In this way any section or step of the flow diagram can be isolated and a cycle can be made to repeat so the action can be observed on an oscilloscope. No push-button pulse checking in this machine is possible as it is in Whirlwind I; the trouble-shooting must be done dynamically. There is no alarm indication in CADAC, and generally speaking, improper functioning of the computer is indicated when no or wrong answers to test programs are typed out on the output typewriter, or unintelligible answers come out, or, of course, when smoke starts pouring out of the machine.

4.2 Difficulties in Trouble-Shooting

The complexity of interconnections among the logical circuits caused the wiring of the diode boards to become rather messy and inaccessible. A technique of using the diode-net resistances to support the bus wire which delivers B/ to the net was used in many places. There was no consistent color coding of the interconnecting wires; this makes them difficult to trace. Vector turret miniature sockets upon which the components associated with the tubes are mounted were used throughout the machine. Although this method assures the rigidity of the components, it does make the tube socket pins and the components inaccessible. The memory and circulating register components were mounted in the form of subassemblies which are subject to vibration of the drum rotation.

Loose and intermittent connections of the diodes in their clips have given rise to some trouble.

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Arnold M. Werlin
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APPROVED E S Rich
E. S. Rich

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Appendix, Page 21
Drawings: A-50870
A-50871
A-50872
A-50873
A-50874

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APPENDIX

Sample CADAC Program

Attached is an example of a CADAC program and the form in which the output typewriter prints results.

I. PROGRAM

The Program is designed to convert a table of coded decimal numbers to octal and to print the address of the coded decimal number with the number, followed by the octal equivalent. The first address of the table is in the m_1 position of register 0410, note 0500. Those positions crossed out are immaterial to the proper operation of the program. The program is started at register #0404.

II. TABLE OF DECIMAL NUMBERS

The table consists of eight numbers coded so that the decimal value is represented by two octal digits according to the following convention.

Decimal #	Coded Equivalent	Decimal #	Coded Equivalent
0	00	5	05
1	01	6	06
2	02	7	07
3	03	8	53
4	04	9	54

The eight values are:

Register	Value	Register	Value
0500	∠.999999	0504	∠.30103
0501	-.5	0505	∠.47712
0502	∠.875	0506	∠.60206
0503	-.0625	0507	∠.69897

III. REQUIRED RESULTS; TABLE OF CODED DECIMAL NUMBERS AND THEIR OCTAL EQUIVALENTS

The CADAC performed the computation according to the program and typed out the required results in about 100 seconds of total operating time.

All of the numbers on the attached page were typed by the CADAC typewriter on the reproducing master. Tables I and II were printed by using a print out from storage routine. Table III is the required results printed from the program. The printed headings were added afterward.

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I. PROGRAM

0404-17041004430405	0405-17051004440435	0406-15043504550442	0407-23044200000411
0410-37050000000000	0411-17040504430430	0412-17040504430431	0413-13044604460436
0414-13044604500442	0415-13044604460440	0416-15044604470441	0417-17043504450437
0420-07044204370454	0421-13045404360436	0422-11043504470435	0423-13044104470441
0424-21044704410417	0425-07044204510442	0426-13044004470440	0427-21045204400416
0430-17050704460436	0431-31050700000000	0432-25043600000000	0433-13040504530405
0434-21044704460405	0435-01000000000000	0436-01545676625256	0437-01000000000000
0440-01000000000022	0441-01000000000003	0442-01777777777777	0443-00777700000000
0444-02777777777777	0445-01700000000000	0446-01000000000000	0447-01000000000003
0450-01631463146314	0451-01063146314632	0452-01000000000020	0453-01000100000000
0454-01000000000000	0455-00777777777777		

II. TABLE OF CODED DECIMAL NUMBERS

0500-01545454545454	0501-00050000000000	0502-01530705000000	0503-00000602050000
0504-01030001000300	0505-01040707010200	0506-01060002000600	0507-01065453540700

III. TABLE OF CODED DECIMAL NUMBERS AND OCTAL EQUIVALENTS

0500-01545454545454	01777777571622	0501-00050000000000	00400000000000
0502-01530705000000	01700000000001	0503-00000602050000	00040000000000
0504-01030001000300	01232101152522	0505-01040707010200	01364222112305
0506-01060002000600	01464202325244	0507-01065453540700	01545676625256

ELECTRONIC BUILDING BLOCKS

FIGURE 1: FLIPFLOP & DRIVERS

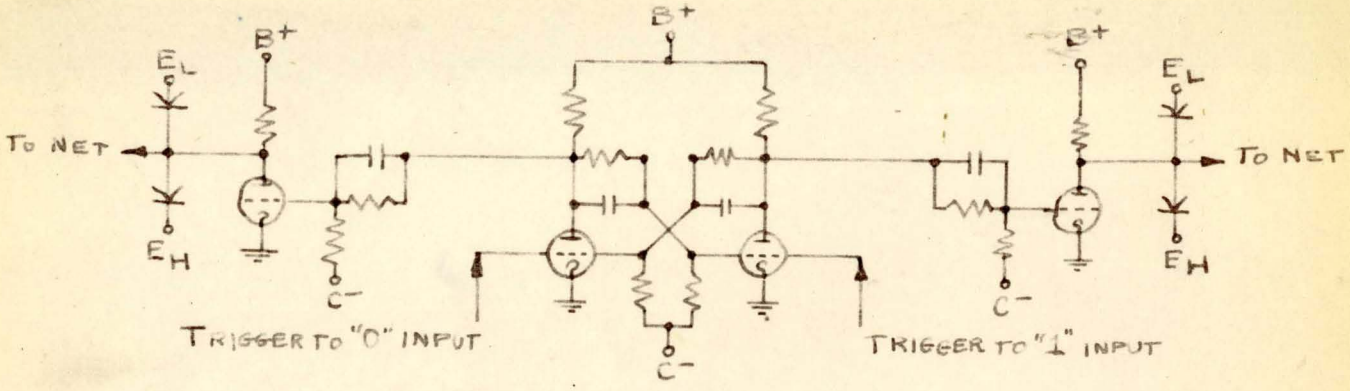

FIGURE 2: PRODUCT

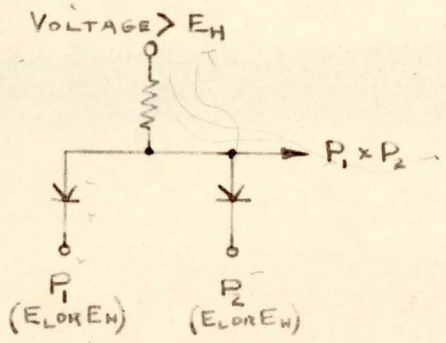

FIGURE 3: SUM

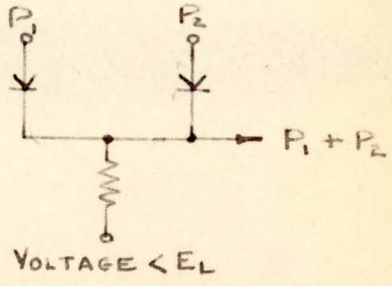

FIGURE 4: NEGATIVE

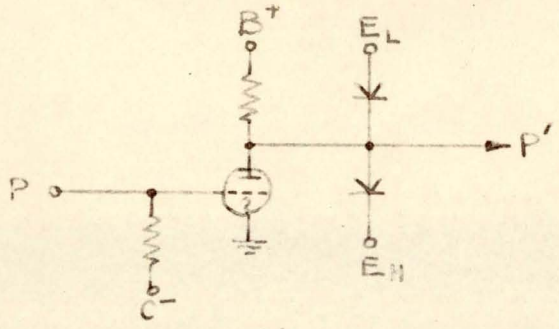

FIGURE 5: TRUTH TABLES OF LOGICAL OPERATIONS

P_1	P_2	$P_1 \times P_2$	$P_1 + P_2$	P_1'
0	0	0	0	1
1	0	0	1	0
0	1	0	1	1
1	1	1	1	0

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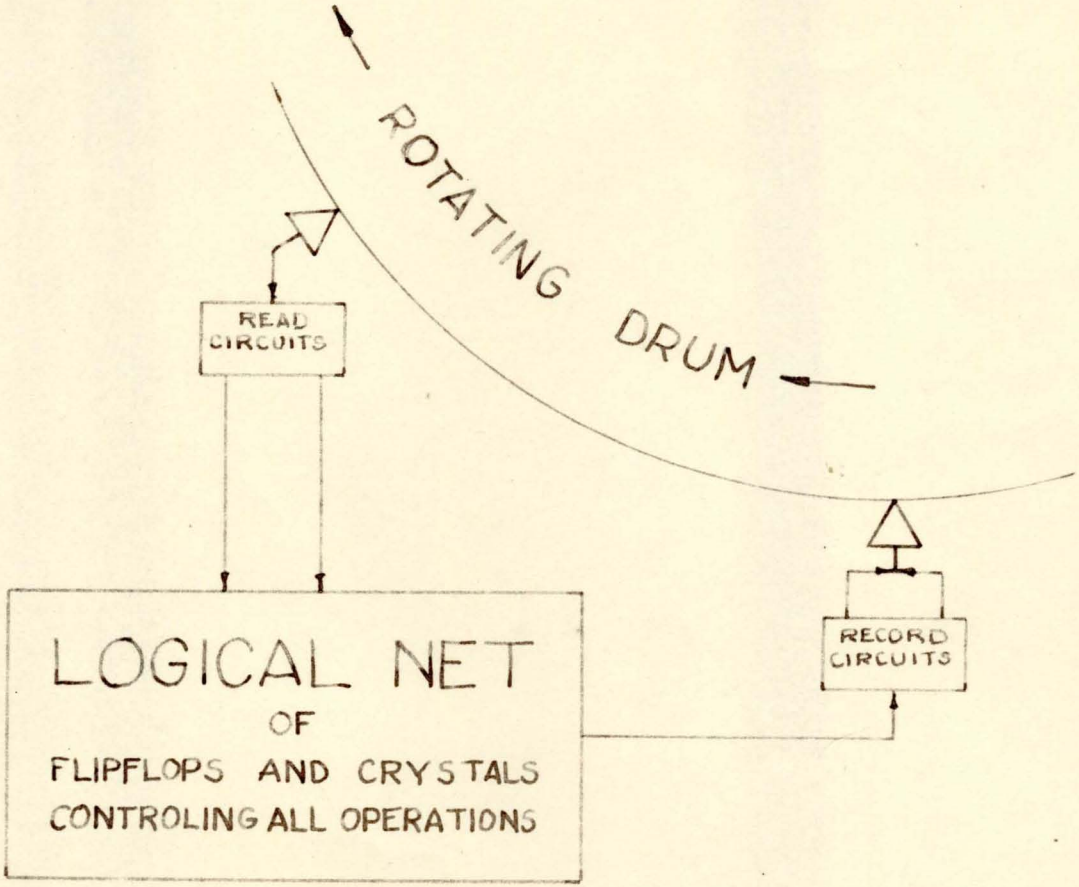
FIGURE 6: DESCRIPTIVE DIAGRAM OF A RECIRCULATING REGISTER



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FLOW DIAGRAM OF INTERNAL OPERATIONS (ABRIDGED)

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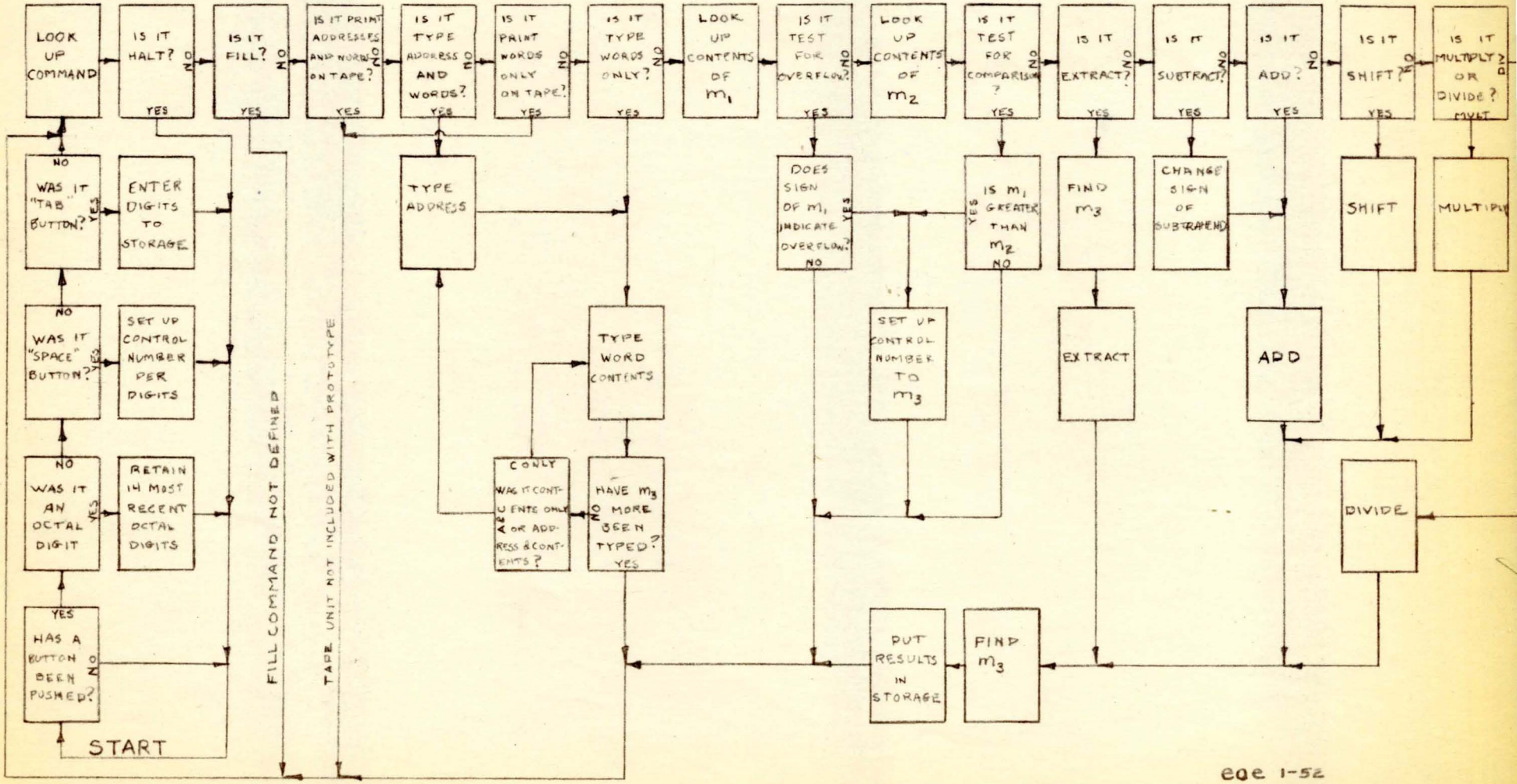
QUARTERLY PROGRESS REPORT NUMBER 2

FIGURE 7:



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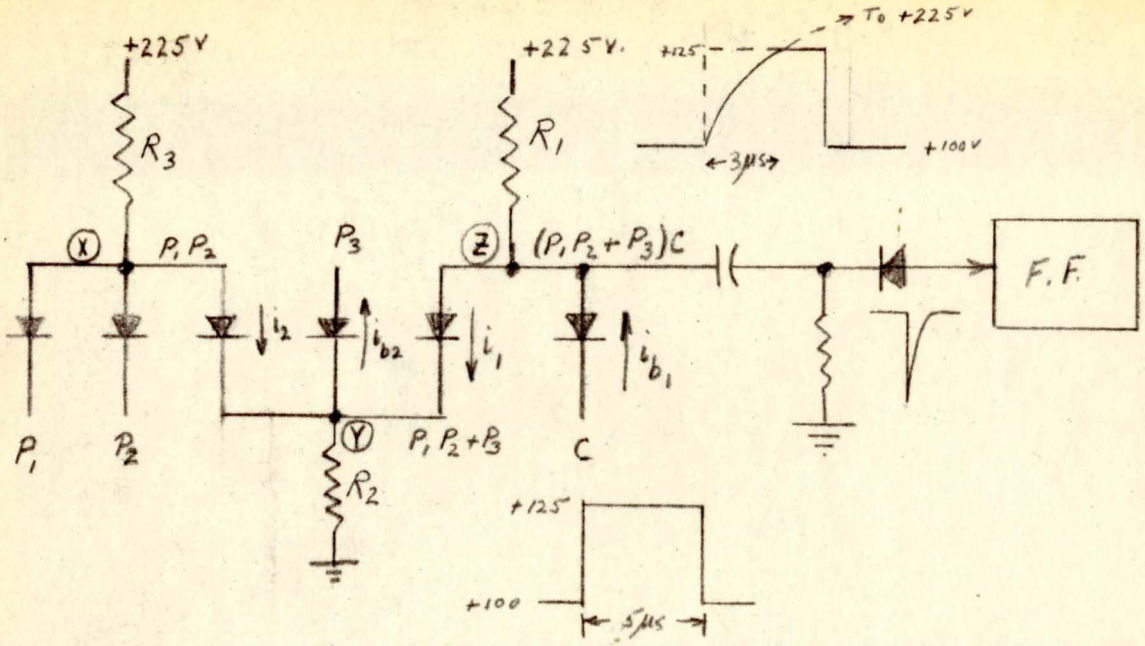
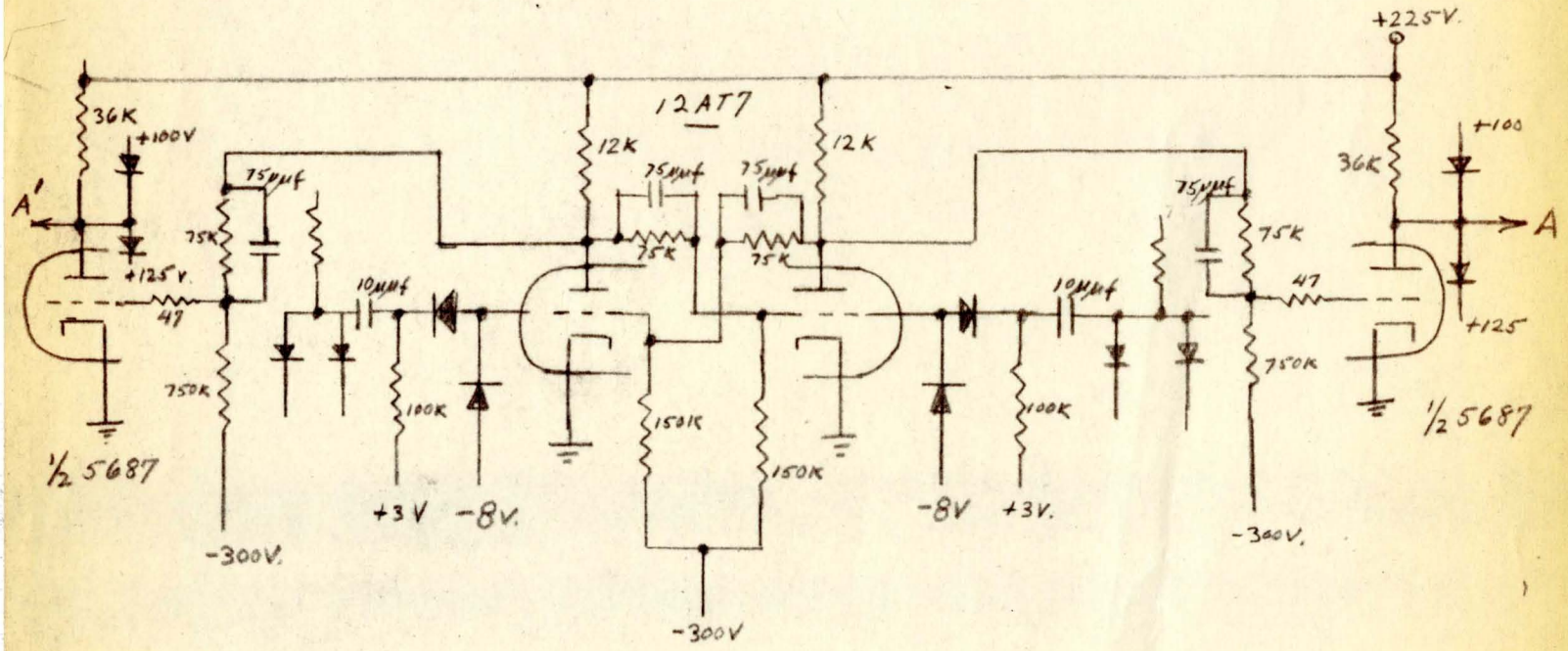


TYPICAL DIODE NET

FIG. 8.



CADAC FLIP-FLOP

FIG. 9.

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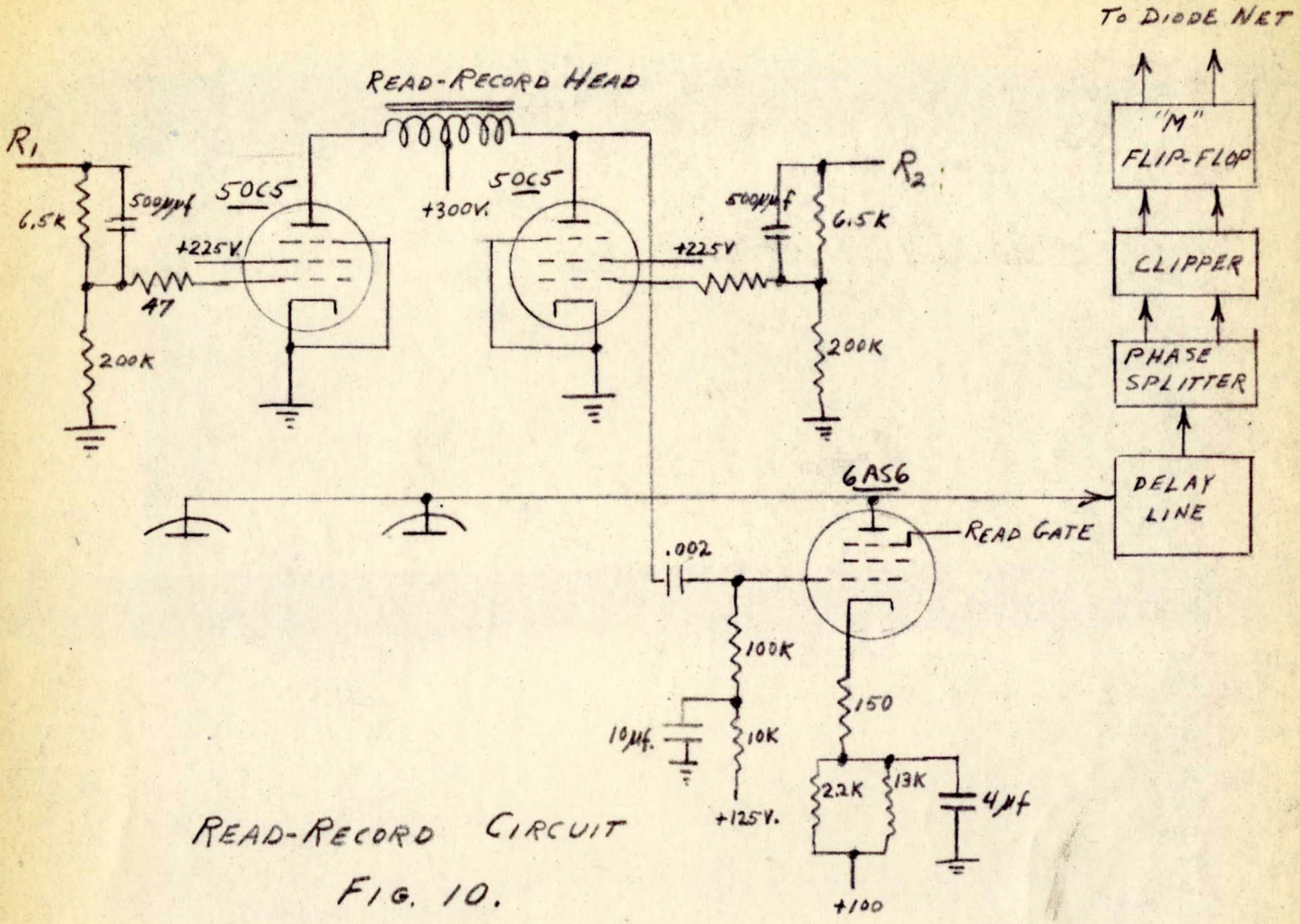
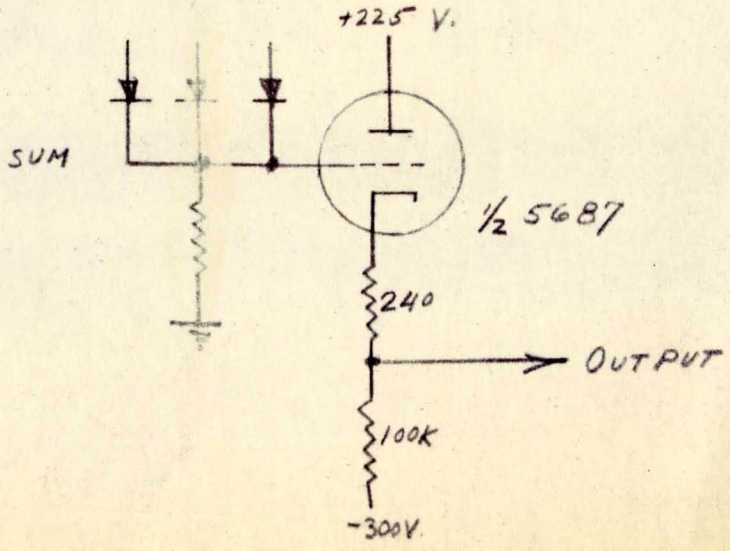


READ-RECORD CIRCUIT

FIG. 10.



CATHODE-FOLLOWER DRIVER

FIG. 11.

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