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8-LINE COMMUNICATION MULTIPLEXER

CONTAINS:

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MACROLINK
8-LINE COMMUNICATION MULTIPLEXER
MANUAL

1. INSTALLATION

This specification covers the installation of the 8-Line COMM MUX (Macrolink PN 200720). The assembly consists of a standard 15"x15" Perkin-Elmer compatible full board and two cable assemblies. The full board may be installed in any available multiplexer bus slot of a standard I/O chassis. Each of the interchangeable internal cables is equipped with four DA-15-P connectors, pin compatible with Perkin-Elmer COMM products. The 8-Line COMM MUX provides 8 independent asynchronous communication channels for use with modems or terminals. This product may be used in 16 or 32 bit CPUs.

1.1 Unpacking

The module and cables should be unpacked carefully and inspected for damage prior to installation. The package and packing material should be saved in the event the module needs to be returned to Macrolink for repair. Claims for shortage or damage must be filed within seven days of receipt of shipment.

1.2 Location

The 8-Line COMM MUX may be installed in any I/O slot (Multiplexer bus) of the computer chassis. After installing the module, remove the RACKO/TACKO strap located on the back panel between terminals 122 and 222, side 1, of the selected slot. This jumper must be replaced if the module is removed for service.

1.3 Cables

The two supplied cables are connected between the cable connectors at the edge of the module and the cable entry panel. These 60-conductor sockets are polarized, and must be connected correctly. Each of the eight COMM channels are marked on the module, and correspond to an individual DA-15-P connector at the end of the cable. Mounting hardware is supplied to locate each connector in the cable entry panel.

1.4 Configuration Options

1.4.1 Baud Rate

Four Baud Rates are available on each module. These rates are independent and may be any value from 50 to 19,200 baud. The baud rates are selected with four-position switches located at the front edge of the module. The baud rates are as follows:

0 = OFF	4 = 134.5	8 = 9600	C = 2400
1 = 19200	5 = 200	9 = 4800	D = 300
2 = 50	6 = 600	A = 1800	E = 150
3 = 75	7 = 2400	B = 1200	F = 110

These four-switch-selected baud rates are not directly connected to a specific channel, but are selected by each channel using the clock bits of output command 2 (see PROGRAMMING section). Each of the 16-position switches selects one of the baud rates.

1.4.1 Dataset Options

Each of the eight channels are grouped into switches S1-4 located at the front of the board as follows:

POSITION	S1		S2		S3		S4	
8	CH7	CL2S	CH5	CL2S	CH3	CL2S	CH1	CL2S
7	CH7	DSRDY	CH5	DSRDY	CH3	DSRDY	CH1	DSRDY
6	CH7	CARR	CH5	CARR	CH3	CARR	CH1	CARR
5	CH7	RING	CH5	RING	CH2	RING	CH0	RING
4	CH6	CL2S	CH4	CL2S	CH2	CL2S	CH0	CL2S
3	CH6	DSRDY	CH4	DSRDY	CH2	DSRDY	CH0	DSRDY
2	CH6	CARR	CH4	CARR	CH2	CARR	CH0	CARR
1	CH6	RING	CH4	RING	CH2	RING	CH0	RING

When the DIP switch is ON, CL2S, DSRDY and CARR will be inactive, i.e., the status bit will be OFF. If these status lines are not connected, the corresponding switch should be ON. The RING status will be active when ON, and **must** be left OFF. To turn the DIP switch ON, press down on the side marked "ON".

1.4.2 Duplex Mode

Each of the eight channels has a switch to enable half or full duplex. Located between U128 and U130, the switch is marked HDX/FDX. The Duplex mode is selected by the Operating System, not the modem or terminal. For OS/16 or OS/32, set all 8 channels to "OFF" for full duplex. The duplex mode is channel independent for special software functions. Press down on the "OFF" side of the switch to select OFF.

1.4.3 Address

One 16-position switch is located at the rear of the module. This switch selects the MSD (most significant digit) of the 16 device addresses used by each module. The following illustrates the address selection:

X'MSD0' = CH0 RCV	X'MSD8' = CH4 RCV
X'MSD1' = CH0 XMIT	X'MSD9' = CH4 XMIT
X'MSD2' = CH1 RCV	X'MSDA' = CH5 RCV
X'MSD3' = CH1 XMIT	X'MSDB' = CH5 XMIT
X'MSD4' = CH2 RCV	X'MSDC' = CH6 RCV
X'MSD5' = CH2 XMIT	X'MSDD' = CH6 XMIT
X'MSD6' = CH3 RCV	X'MSDE' = CH7 RCV
X'MSD7' = CH3 XMIT	X'MSDF' = CH7 XMIT

The address switch can be set from 1 to F.

2. PROGRAMMING

The 8-Line COMM MUX provides eight independent interfaces between the Multiplexer Bus of a Perkin-Elmer processor. These RS-232-C compatible channels will connect a wide variety of Modems or Data Terminals in either half or full duplex mode.

Each of the eight channels has two consecutive addresses: EVEN for Receive and HDX Transmit, and ODD for FDX Transmit. Interrupts are generated for Receive and Transmit of each channel. The 8-Line COMM MUX is fully software compatible with Perkin-Elmer asynchronous communication products.

Each of the eight channels is fully independent. Commands are separate for each channel as are status bits. Each channel may be set to half or full duplex as supported by Operating System software.

2.1 Programming Instructions

Standard processor byte I/O instructions are used to communicate with the 8-Line COMM MUX.

2.1.1 Sense Status

This instruction is used to detect if data transfers are complete and correct, and to detect the status of the data set. The mode and function of the 8-Line COMM MUX modify the Status Register. Tables 1 and 2 should be consulted for proper definition.

2.1.2 Output Command

This instruction is used to change the 8-Line COMM MUX mode from Receive to Transmit, to select data format, select interrupts and to service the Data Set. Two command bytes are required for each channel.

2.1.3 Write Data

This instruction is used to load the Output Register with a byte of data.

2.1.4 Read Data

This instruction will read an assembled byte into the processor.

2.2 Status and Command Bytes

RCV Status		OV	PF	FR	RCR	RBSY	$\overline{\text{DSRDY}}$+OV	CARR	RING
WRT HDX status		0	$\overline{\text{CL2S}}$	0	RCR	TBSY	$\overline{\text{DSRDY}}$	0	RING
WRT FDX Status		0	$\overline{\text{CL2S}}$	0	0	TBSY	0	0	0
CMD1	$\overline{\text{RCV}}$	DIS	EN	DTR	ECHO	RCT/	TRANS	WRT	1
	$\overline{\text{WRT}}$	DIS	EN						
CMD2		CLK B	CLK A	BIT SEL		STOP BIT	PARITY		0

TABLE 1 COMM MUX STATUS & COMMAND DATA

COMM MUX MODE	STATUS MODE
RCV - HDX - EVEN ADDR	RCV
RCV - HDX - ODD ADDR	RCV
RCV - FDX - EVEN ADDR	RCV
RCV - FDX - ODD ADDR	WRT FDX
WRT - HDX - EVEN ADDR	WRT HDX
WRT - HDX - ODD ADDR	WRT HDX
WRT - FDX - EVEN ADDR	RCV
WRT - FDX - ODD ADDR	WRT FDX

TABLE 2 STATUS MODES

STATUS

OV — This bit is set if the current received character overwrites an unread character. The error condition is reset by reading the current character.

PF — This bit is set if the parity of the received character is not equal to the programmed parity. This bit will be inactive if no parity is selected, and will be reset at the end of the next character without error.

FR — This bit is set to indicate that the current received character has no stop bit(s). An all-zero character with this bit set may indicate a line break. This bit will be reset at the end of the next valid transition.

RCR — Reverse Channel Receive (SB). This bit will be active to indicate a line space condition of the half duplex data set. If the data set is not equipped with the Reverse Channel Option, or the Hardware Suppress Option is selected, this bit will be inactive.

RBSY — When this bit is low, the Adapter is ready to transfer data to the processor. If an OV condition occurs, a Read Data instruction must be issued to set the RBSY bit to a high state. This bit is set if Data Set Ready (CC) is off.

EX — OV + PF + FR + $\overline{\text{DATA SET READY}}$. This bit is set if one or more of the previous conditions occur.

CARR — This bit will indicate the state of the CF signal from OFF the data set. When this bit is set, the incoming data is not valid.

RING — This bit will indicate the state of the CE signal from the data set.

$\overline{\text{CL2S}}$ — This bit is set to indicate the state of the CB signal from the data set. When this bit is set, the modem can no longer transmit data.

TBSY — When this bit is low, the Multiplexer is ready to transfer data from the processor. If Clear to Send (CB) is off, or Data Set Ready (CC) is off, or the Multiplexer is full, this bit will be set.

2.3 8-Line COMM MUX Commands

Command 1 This command is selected by setting bit 15. Two commands are required to select the desired operating mode of each channel.

DIS/EN — DIS/EN bits are separate for the Receive and Transmit side. To change DIS/EN on the Receive side, issue a command with WRT:0, and the desired DIS/EN function. To change DIS/EN on the Transmit side, issue a WRT:1 command with the desired DIS/EN function. Because the WRT is gated to the data set as Request to Set, it is essential that a WRT:0 command be followed by a WRT:1 command when in FDX operation. In HDX operation, the odd address has interrupts disabled.

BIT 8	9	Interrupt Mode
0	0	No Change
0	1	Enable
1	0	Disable (Interrupt Queued)
1	1	Disarm

DTR — When this bit is active, the Data Terminal Ready (CD) signal from the COMM MUX to the data set is activated. When on, it allows automatic answering of incoming calls, and allows the data set to remain in the Data mode. If this bit is held off, it does not allow automatic answering of calls and causes and existing connection to be disconnected.

ECHO PLEX — When set, the data received from the data set on the BB line is transmitted back to the data set on the BA line. The COMM MUX will also analyze the character. This bit **must not** be set while transmitting a character, or the character will be corrupted.

RCT/DTB — Reverse Channel Transmit (SA) or Data Terminal Busy for 202C or 103 type data sets. This bit should be set to one to satisfy the RS-232-C requirements. When set, a Mark state will be transmitted on the reverse channel. When reset, a space will be transmitted on the reverse channel. With data sets equipped with the DTB option, the inactive condition of this bit will cause the terminal to be busy and not allow a call to be answered.

TRNS LB — When set, a continuous space will be transmitted to the data set. This bit will override the ECHO-PLEX mode, and will cause transmitted data to be garbled.

WRT — When this bit is set, Request to Send (CA) is gated to the data set if Data Set Ready (CC) is active. When this bit is reset, Request to Send (CA) will deactivate after the last data transfer has been completed. Busy will be forced active during this mode change and will be active until a character is received.

Command 2 This command is selected by resetting bit 15.

CLK A, CLK B: These bits select one of four baud rate switches:

BIT 8	9	SWITCH
0	0	CLK 0
0	1	CLK 1
1	0	CLK 2
1	1	CLK 3

Each "CLK" switch can be set to one of the following baud rates:

0 : OFF	4 : 134.5	8 : 9600	C : 2400
1 : 19200	5 : 200	9 : 4800	D : 300
2 : 50	6 : 600	A : 1800	E : 150
3 : 75	7 : 2400	B : 1200	F : 110

BIT SEL These bits select the number of data bits/characters

BIT 10	11	Number of Data Bits
0	0	5
0	1	6
1	0	7
1	1	8

If less than eight bits are selected, the data must be right-justified before a Write Data is issued. In the Read mode, the data returned to the processor with the Read Data command will be right-justified, with unused bits in a Zero state.

STOP BIT 0 = 1 STOP BIT
1 = 2 STOP BIT

The receiver only samples the first Stop Bit.

BIT 13	14	Parity
1	0	ODD
1	1	EVEN
0	X	NONE

If parity is selected, the transmitter will append a parity bit after the last data bit, and the receiver will examine this bit position for parity agreement. PF status will be set if received parity is not the selected parity. If parity is disabled, a stop bit will reappend after the last data bit, and receiver parity is disabled.

2.4 Interrupts

A list of interrupting conditions is shown in the following table:

STATUS BIT	HDX		FDX	
	RCV	WRT	RCV	WRT
RING -> 1	X	X	X	
CARR OFF -> 1	X		X	
CARR OFF -> 0	X		X	
RCR -> 1	X	X	X	
RCR -> 0	X	X	X	
DSRDY -> 0	X	X	X	
BUSY -> 0	X	X	X	X
$\overline{\text{CL2S}}$ -> 1	X	X		X

3. MAINTENANCE

This specification covers the operation and maintenance of the 8-Line COMM MUX. This product provides 8 independent interfaces between a Perkin-Elmer multiplexer bus and half or full duplex asynchronous data sets and/or local terminals. These 8 RS-232-C channels operate from 50 to 19200 baud.

The entire circuitry of the 8-Line COMM MUX is contained on one 15" X 15" circuit board. The module generates all clock signals and ±10V for the RS-232-C line signals from +5V at 1.8 amp. All interrupt and status logic is controlled by a high-speed microprocessor.

3.1 Schematic Description / CPU Interface

Schematic sheets 1, 2 and 10 show the multiplexer bus interface. This interface consists of 6 sections:

1. I/O Bus Receivers/Drivers
2. Address Decoding
3. Control Decoding
4. Sync Return
5. Status/Data Multiplexers
6. RACKO/TACKO

The I/O bus interface is located on sheet 1, section D4 (1D4) and 2D1. A 74LS240 is used to receive the data from the I/O bus (U5). Two 7438's (U6,23) provide a high current open collector interface to the Perkin-Elmer bus.

U19 (1B3) decodes the MSD of the address. The 4-bit LSD field is latched in U61 (1A4).

Sheet 2 of the schematics contains the control select logic. All 6 of the control lines are received with U4, a 74LS14. Additionally, a set of 74LS138 decoders (sheet 1) decode DAGO, DRGO and CMDGO. U99 (1A1) latches the write command. U70 (1C1) is used as one of eight high true decoders for CMGB1. Sync return (2B2) is delayed 2mS via one shot U2 for data in/out and address decode. All other SYNC functions directly set SYNO.

Multiplexers U7, 24, 8 and 25 on sheet 2 multiplex the status byte and address vector. In addition, these multiplexers are switched into a high-impedence state and the selected UART is placed on the TD151-TD081 bus during read.

Flip-Flop U66 (10A4) latches pending interrupts and U20-3 (10A3) issues ATNO to the CPU. SYNO or SCLRO will reset U66.

3.2 RS-232-C Interface

Sheets 3-6 contain eight sets of RS-232-C control logic and UARTs. Each set of logic has 3 outputs (including serial data) that are controlled by a 74LS175 latch. This latch is set by the decoded CMGA0 signal. An additional output, CA, is delayed by approximately 15mS to allow for the last serial character to be shifted out of the UART.

The UART provides parallel to serial transmit conversion and serial to parallel receive conversion. The UART generates and detect start and stop bits and parity. Both the receive and transmit side of the UART have buffer registers. An overflow bit (OV) will be set if a receive character overwrites an unread receive buffer.

Sheet 8 contains all of the RS-232-C receivers. These 1489A receivers provide a TTL interface to the ± 12V input signals.

3.3 Baud Rate Generation

Sheet 7 contains all the logic for baud rate generation and selection. U146 (7B3) generates multiplexed baud rates that are decoded by U134 (7B2) as a function of HEX switches 0-3. The outputs of U134 (pins 4-7) are the baud rates corresponding to switches 0-3. These rates (16x the data rate) are re-multiplexed by U124-125 (7B1) and decoded by U86-87 (7A1).

U88-89 (7D2) latch the clock bits of command 1 and select, via U106-107 (7D2) the rate for each channel.

3.4 State Machine

All interrupts and status requests are serviced by the state machine (sheet 11). Counters U77, 78 (11C2) step through the microcode located within the three 512x8 PROMs (U63-65). Additionally, as a function of the test inputs of multiplexer U35 (11C3), the program counter can jump to a new starting address.

3.5 Interrupts

Sheet 10 contains all the ARM/DISARM logic and interrupt edge detection. U31 (10D1) stores the interrupt bits, and is examined for each channel during the scan. At the same time, U21-30 (10D4) stores the last state of the status signal. If the last state and current state are not the same, edge logic (11C3) will generate an interrupt. Multiplexers U16, 33 (10D2) select half or full duplex interrupt mode.

3.6 Power Supply

An on-board switch converts +5V to ±9V for use with the RS-232-C drivers. U147 (11A3) generates a 20KHz square wave that drives U135. T1 steps up this voltage to ±9V. No additional regulation is needed.

APPENDIX

MNEMONIC	MEANING	LOCATION
ADRSYN0	ADDRESS SYNC DECODE	1B2
ADRS1	ADDRESS CONTROL FROM CPU	2D4
1ADR1	LSB ADDRESS LATCH	1A3
2ADR1	LSB ADDRESS LATCH	1A3
4ADR1	LSB ADDRESS LATCH	1A3
8ADR1	LSB ADDRESS LATCH	1A3
0BA	CH 0 TRANSMITTED DATA	3C3
1BA	CH 1 TRANSMITTED DATA	3C1
2BA	CH 2 TRANSMITTED DATA	4C3
3BA	CH 3 TRANSMITTED DATA	4C1
4BA	CH 4 TRANSMITTED DATA	5C3
5BA	CH 5 TRANSMITTED DATA	5C1
6BA	CH 6 TRANSMITTED DATA	6C3
7BA	CH 7 TRANSMITTED DATA	6C1
0CA	CH 0 REQUEST TO SEND	3D3
1CA	CH 1 REQUEST TO SEND	3D1
2CA	CH 2 REQUEST TO SEND	4D3
3CA	CH 3 REQUEST TO SEND	4D1
4CA	CH 4 REQUEST TO SEND	5D3
5CA	CH 5 REQUEST TO SEND	5D1
6CA	CH 6 REQUEST TO SEND	6D3
7CA	CH 7 REQUEST TO SEND	6D1
CARR0	MULTIPLEXED CARRIER STATUS	9B3
CARR1	MULTIPLEXED CARRIER STATUS	9B3
0CARR0	CH 0 CARRIER STATUS	8D3

APPENDIX Cont...

MNEMONIC	MEANING	LOCATION
1CARR0	CH 1 CARRIER STATUS	8D3
2CARR0	CH 2 CARRIER STATUS	8C3
3CARR0	CH 3 CARRIER STATUS	8C3
4CARR0	CH 4 CARRIER STATUS	8B3
5CARR0	CH 5 CARRIER STATUS	8B3
6CARR0	CH 6 CARRIER STATUS	8B3
7CARR0	CH 7 CARRIER STATUS	8A3
0CD	CH 0 DATA TERMINAL READY	3D3
1CD	CH 1 DATA TERMINAL READY	3D1
2CD	CH 2 DATA TERMINAL READY	4D3
3CD	CH 3 DATA TERMINAL READY	4D1
4CD	CH 4 DATA TERMINAL READY	5D3
5CD	CH 5 DATA TERMINAL READY	5D1
6CD	CH 6 DATA TERMINAL READY	6D3
7CD	CH 7 DATA TERMINAL READY	6D1
0CLK1	CH 0 16 X BAUD RATE	7C1
1CLK1	CH 1 16 X BAUD RATE	7C1
2CLK1	CH 2 16 X BAUD RATE	7C1
3CLK1	CH 3 16 X BAUD RATE	7C1
4CLK1	CH 4 16 X BAUD RATE	7B1
5CLK1	CH 5 16 X BAUD RATE	7B1
6CLK1	CH 6 16 X BAUD RATE	7B1
7CLK1	CH 7 16 X BAUD RATE	7B1
CL2S0	MULTIPLEXED CLEAR TO SEND	9B3
CL2S1	MULTIPLEXED CLEAR TO SEND	9B3

APPENDIX Cont...

MNEMONIC	MEANING	LOCATION
0CL2S0	CH 0 CLEAR TO SEND	8D1
1CL2S0	CH 1 CLEAR TO SEND	8D1
2CL2S0	CH 2 CLEAR TO SEND	8C1
3CL2S0	CH 3 CLEAR TO SEND	8C1
4CL2S0	CH 4 CLEAR TO SEND	8B1
5CL2S0	CH 5 CLEAR TO SEND	8B1
6CL2S0	CH 6 CLEAR TO SEND	8A1
7CL2S0	CH 7 CLEAR TO SEND	8A1
0CMAG0	CH 0 COMMAND A DECODE	1D2
1CMAG0	CH 1 COMMAND A DECODE	1D2
2CMAG0	CH 2 COMMAND A DECODE	1D2
3CMAG0	CH 3 COMMAND A DECODE	1D2
4CMAG0	CH 4 COMMAND A DECODE	1D2
5CMAG0	CH 5 COMMAND A DECODE	1D2
6CMAG0	CH 6 COMMAND A DECODE	1C2
7CMAG0	CH 7 COMMAND A DECODE	1C2
0CMBG1	CH 0 COMMAND B DECODE	1C1
1CMBG1	CH 1 COMMAND B DECODE	1C1
2CMBG1	CH 2 COMMAND B DECODE	1C1
3CMBG1	CH 3 COMMAND B DECODE	1C1
4CMBG1	CH 4 COMMAND B DECODE	1C1
5CMBG1	CH 5 COMMAND B DECODE	1C1
6CMBG1	CH 6 COMMAND B DECODE	1B1
7CMBG1	CH 7 COMMAND B DECODE	1B1
CMDG0	ADDRESS GATED COMMAND CONTROL FROM CPU	2C3

APPENDIX Cont...

MNEMONIC	MEANING	LOCATION
CPR1	CLOCKED PROCESSOR REQUEST	2D2
D081	BUFFERED DATA FROM CPU	1C3
D091	BUFFERED DATA FROM CPU	1C3
D101	BUFFERED DATA FROM CPU	1C3
D111	BUFFERED DATA FROM CPU	1C3
D121	BUFFERED DATA FROM CPU	1D4
D130	BUFFERED DATA FROM CPU	1A2
D131	BUFFERED DATA FROM CPU	1D4
D141	BUFFERED DATA FROM CPU	1D4
D150	BUFFERED DATA FROM CPU	1C2
D151	BUFFERED DATA FROM CPU	1D4
DAG0	ADDRESS GATED DATA AVAILABLE	2C3
0DAG0	CH 0 DATA AVAILABLE DECODE	1C1
1DAG0	CH 1 DATA AVAILABLE DECODE	1C1
2DAG0	CH 2 DATA AVAILABLE DECODE	1C1
3DAG0	CH 3 DATA AVAILABLE DECODE	1C1
4DAG0	CH 4 DATA AVAILABLE DECODE	1C1
5DAG0	CH 5 DATA AVAILABLE DECODE	1D1
6DAG0	CH 6 DATA AVAILABLE DECODE	1D1
7DAG0	CH 7 DATA AVAILABLE DECODE	1D1
DAT080	DATA BUS FROM CPU	1C4
DAT090	DATA BUS FROM CPU	1D4
DAT100	DATA BUS FROM CPU	1D4
DAT110	DATA BUS FROM CPU	1D4
DAT120	DATA BUS FROM CPU	1D4

APPENDIX Cont...

MNEMONIC	MEANING	LOCATION
DAT130	DATA BUS FROM CPU	1D4
DAT140	DATA BUS FROM CPU	1D4
DAT150	DATA BUS FROM CPU	1D4
DILO	DELAY INTERRUPT LATCH	11B3
DRGO	ADDRESS GATED DATA REQUEST	2D3
0DRGO	CH 0 DATA REQUEST CODE	1D3
1DRGO	CH 1 DATA REQUEST CODE	1D3
2DRGO	CH 2 DATA REQUEST CODE	1D3
3DRGO	CH 3 DATA REQUEST CODE	1D3
4DRGO	CH 4 DATA REQUEST CODE	1D3
5DRGO	CH 5 DATA REQUEST CODE	1D3
6DRGO	CH 6 DATA REQUEST CODE	1C3
7DRGO	CH 7 DATA REQUEST CODE	1C3
DR1	DATA REQUEST CONTROL FROM CPU	2D4
0DR1	CH 0 DATA REQUEST DECODE	3A3
1DR1	CH 1 DATA REQUEST DECODE	3B1
2DR1	CH 2 DATA REQUEST DECODE	4A3
3DR1	CH 3 DATA REQUEST DECODE	4B1
4DR1	CH 4 DATA REQUEST DECODE	5A3
5DR1	CH 5 DATA REQUEST DECODE	5B1
6DR1	CH 6 DATA REQUEST DECODE	6A3
7DR1	CH 7 DATA REQUEST DECODE	6B1
DS081	ADDRESS VECTOR FOR INTERRUPT	1B3
DS091	ADDRESS VECTOR FOR INTERRUPT	1B3
DS101	ADDRESS VECTOR FOR INTERRUPT	1C3

APPENDIX Cont...

MNEMONIC	MEANING	LOCATION
DS111	ADDRESS VECTOR FOR INTERRUPT	1C3
DSRDY0	MULTIPLEXED DATA SET READY	9B3
DSRDY1	MULTIPLEXED DATA SET READY	9B3
0DSRDY0	CH 0 DATA SET READY	8D2
1DSRDY0	CH 1 DATA SET READY	8D2
2DSRDY0	CH 2 DATA SET READY	8C2
3DSRDY0	CH 3 DATA SET READY	8C2
4DSRDY0	CH 4 DATA SET READY	8C2
5DSRDY	CH 5 DATA SET READY	8B2
6DSRDY	CH 6 DATA SET READY	8B2
7DSRDY	CH 7 DATA SET READY	8B2
ENIN1	INTERRUPT ENABLE MEMORY	10D1
ENOUT1	INTERRUPT	10D1
FDX0	HALF DUPLEX	9B3
FDX1	FULL DUPLEX	9B3
FR1	MULTIPLEXED FRAMING ERROR	9B2
0FR1	CH 0 FRAMING ERROR	3C3
1FR1	CH 1 FRAMING ERROR	3C1
2FR1	CH 2 FRAMING ERROR	4C3
3FR1	CH 3 FRAMING ERROR	4C1
4FR1	CH 4 FRAMING ERROR	5C3
5FR1	CH 5 FRAMING ERROR	5C1
6FR1	CH 6 FRAMING ERROR	6C3
7FR1	CH 7 FRAMING ERROR	6C1
ICTR0	INTERRUPT CONTROL ENABLE	11B3

APPENDIX Cont.

MNEMONIC	MEANING	LOCATION
1IL1	LATCHED INTERRUPT CH VECTOR:1	11D3
2IL1	LATCHED INTERRUPT CH VECTOR:2	11D3
4IL1	LATCHED INTERRUPT CH VECTOR:4	11D3
8IL1	LATCHED INTERRUPT CH VECTOR:8	11D3
INT1	INTERRUPT OUTPUT	10D1
INTR1	INTERRUPT REQUEST	10D1
LCTR0	INTERRUPT LATCH CONTROL	11B3
LDR1	CLOCKED DATA REQUEST	9B2
LENIN1	LATCHED ENABLE INTERRUPT	10B1
LENOUT	LATCHED ENABLE INTERRUPT OUTPUT	10B1
LILO	INTERRUPT BUFFER LATCH CONTROL	11B3
LINT1	LATCHED INTERRUPT	10B2
0LTBRE	CH 0 LATCHED TRANSMIT INTERRUPT REQ	9D1
1LTBRE	CH 1 LATCHED TRANSMIT INTERRUPT REQ	9D1
2LTBRE	CH 2 LATCHED TRANSMIT INTERRUPT REQ	9C1
3LTBRE	CH 3 LATCHED TRANSMIT INTERRUPT REQ	9C1
4LTBRE	CH 4 LATCHED TRANSMIT INTERRUPT REQ	9B1
5LTBRE	CH 5 LATCHED TRANSMIT INTERRUPT REQ	9B1
6LTBRE	CH 6 LATCHED TRANSMIT INTERRUPT REQ	9B1
7LTBRE	CH 7 LATCHED TRANSMIT INTERRUPT REQ	9A1
OV1	MULTIPLEXED OVERFLOW FROM UART	9B2
0OV1	CHANNEL 0 OVERFLOW	3C3
1OV1	CHANNEL 1 OVERFLOW	3C1
2OV1	CHANNEL 1 OVERFLOW	4C3
3OV1	CHANNEL 3 OVERFLOW	4C1

APPENDIX Cont...

MNEMONICS	MEANING	LOCATION
4OV1	CHANNEL 4 OVERFLOW	5C3
5OV1	CHANNEL 5 OVERFLOW	5C1
6OV1	CHANNEL 6 OVERFLOW	6C3
7OV1	CHANNEL 7 OVERFLOW	6C1
1PADR1	POLLED ADDRESS:1	11C3
2PADR1	POLLED ADDRESS:2	11C3
4PADR1	POLLED ADDRESS:4	11C3
8PADR1	POLLED ADDRESS:8	11C3
0PAJ1	JUMP ADDRESS 0	11D1
1PAJ1	JUMP ADDRESS 1	11D1
2PAJ1	JUMP ADDRESS 2	11D1
4PAJ1	JUMP ADDRESS 4	11D1
8PAJ1	JUMP ADDRESS 8	11D1
0PCC1	CONDITION CODE SELECT:0	11B1
1PCC1	CONDITION CODE SELECT:1	11B1
2PCC1	CONDITION CODE SELECT2	11B1
PCEN1	INTERRUPT LATCH ENABLE	11C1
PCIN0	INTERRUPT CONTROL	11C1
PCLK0	PROCESSOR CLOCK	7D1
PCLK1	PROCESSOR CLOCK	7D2
0PCT1	CONDITION FIELD MUX 0	11B1
1PCT1	CONDITION FIELD MUX 1	11B1
PCTR1	CONDITION FIELD ENABLE	11B1
PCPAD1	INTERRUPT ADDRESS BUS ENABLE	11C1
PCTR1	CONDITION FIELD ENABLE	11B1

APPENDIX Cont...

MNEMONIC	MEANING	LOCATION
PE1	MULTIPLEXED PARITY ERROR	9B2
0PE1	CH 0 PARITY ERROR	3C3
1PE1	CH 1 PARITY ERROR	3C1
2PE1	CH 2 PARITY ERROR	4C3
3PE1	CH 3 PARITY ERROR	4C1
4PE1	CH 4 PARITY ERROR	5C3
5PE1	CH 5 PARITY ERROR	5C1
6PE1	CH 6 PARITY ERROR	6C3
7PE1	CH 7 PARITY ERROR	6C1
PI1	INTERRUPT DETECT	11C3
PJCC0	JUMP CONDITION CODE	11B1
PJMP0	JUMP ENABLE	11B1
PLRS1	STATUS LATCH CLOCK	11D1
PSATN1	SET ATTENTION FLOP	11D1
PSEN1	INTERRUPT CONTROL	11C1
PSIN1	SET INTERRUPT	11C1
PSYN1	SYNC CONTROL	11C1
PWIM1	INTERRUPT RAM WRITE	11C1
PWSM1	INTERRUPT RAM WRITE	11C1
Q00	BAUD RATE MULTIPLEXED CLOCK 0	7A2
Q10	BAUD RATE MULTIPLEXED CLOCK 1	7A2
RACK0	RECEIVE ACKNOWLEDGE INTERRUPT	10B4
0RCR0	CH 0 REVERSE CHANNEL RECEIVE	8D3
1RCR0	CH 1 REVERSE CHANNEL RECEIVE	8D3
2RCR0	CH 2 REVERSE CHANNEL RECEIVE	8C3

APPENDIX Cont...

MNEMONIC	MEANING	LOCATION
3RCR0	CH 3 REVERSE CHANNEL RECEIVE	8C3
4RCR0	CH 4 REVERSE CHANNEL RECEIVE	8C3
5RCR0	CH 5 REVERSE CHANNEL RECEIVE	8B3
6RCR0	CH 6 REVERSE CHANNEL RECEIVE	8B3
7RCR0	CH 7 REVERSE CHANNEL RECEIVE	8B3
RCR1	MULTIPLEXED REVERSE CHANNEL RECEIVE	9B2
RCTR0	REVERSE CHANNEL TRANSMIT	11B3
0RDAT1	CH 0 RECEIVE DATA	8D1
1RDAT1	CH 1 RECEIVE DATA	8D1
2RDAT1	CH 2 RECEIVE DATA	8C1
3RDAT1	CH 3 RECEIVE DATA	8C1
4RDAT1	CH 4 RECEIVE DATA	8C1
5RDAT	CH 5 RECEIVE DATA	8B1
6RDAT	CH 6 RECEIVE DATA	8B1
7RDAT	CH 7 RECEIVE DATA	8B1
RILO	RESET INTERRUPT LATCH	11B3
RING1	MULTIPLEXED RING	9B2
0RING0	CH 0 RING	8D4
1RING0	CH 1 RING	8D4
2RING0	CH 2 RING	8C4
3RING0	CH 3 RING	8C4
4RING0	CH 4 RING	8B4
5RING0	CH 5 RING	8B4
6RING0	CH 6 RING	8B4
7RING0	CH 7 RING	8A4

APPENDIX Cont...

MNEMONIC	MEANING	LOCATION
RSLAT1	RESET WRITE INTERRUPT LATCH	11C1
0SA	CH 0 REVERSE CHANNEL TRANSMIT DATA	3C3
1SA	CH 1 REVERSE CHANNEL TRANSMIT DATA	3C1
2SA	CH 2 REVERSE CHANNEL TRANSMIT DATA	4C3
3SA	CH 3 REVERSE CHANNEL TRANSMIT DATA	4C1
4SA	CH 4 REVERSE CHANNEL TRANSMIT DATA	5C3
5SA	CH 5 REVERSE CHANNEL TRANSMIT DATA	5C1
6SA	CH 6 REVERSE CHANNEL TRANSMIT DATA	6C3
7SA	CH 7 REVERSE CHANNEL TRANSMIT DATA	6C1
SCLR0B	SYSTEM CLEAR FROM CPU	2C3
SEL0	ADDRESS SELECT	1C2
SEL1	ADDRESS SELECT	1C2
SQAD0	SEQUENCER ADDRESS 0	11B2
SQAD1	SEQUENCER ADDRESS 1	11A2
SQAD2	SEQUENCER ADDRESS 2	11A2
SQAD3	SEQUENCER ADDRESS 3	11A2
SQAD4	SEQUENCER ADDRESS 4	11A2
SR1	STATUS REQUEST CONTROL FROM CPU	2C4
SYN0	SYNC RETURN TO CPU	2B2
TACK0	TRANSMIT ACKNOWLEDGE INTERRUPT	10A2
TBRE1	MULTIPLEXED TRANSMIT BUFFER REGISTER EMPTY	9B2
0TBRE1	CH 0 TRANSMIT BUFFER REGISTER EMPTY	3B3
1TBRE1	CH 1 TRANSMIT BUFFER REGISTER EMPTY	3B1
2TBRE1	CH 2 TRANSMIT BUFFER REGISTER EMPTY	4B3
3TBRE1	CH 3 TRANSMIT BUFFER REGISTER EMPTY	4B1

APPENDIX Cont...

MNEMONIC	MEANING	LOCATION
4TBRE1	CH 4 TRANSMIT BUFFER REGISTER EMPTY	5B3
5TBRE1	CH 5 TRANSMIT BUFFER REGISTER EMPTY	5B1
6TBRE1	CH 6 TRANSMIT BUFFER REGISTER EMPTY	6B3
7TBRE1	CH 7 TRANSMIT BUFFER REGISTER EMPTY	6B1
TD081	THREE STATE DATA BUS BIT 8	2B1
TD091	THREE STATE DATA BUS BIT 9	2B1
TD101	THREE STATE DATA BUS BIT 10	2B1
TD111	THREE STATE DATA BUS BIT 11	2C1
TD121	THREE STATE DATA BUS BIT 12	2C1
TD131	THREE STATE DATA BUS BIT 13	2C1
TD141	THREE STATE DATA BUS BIT 14	2D1
TD 151	THREE STATE DATA BUS BIT 15	2D1
0TDAT1	CH 0 TRANSMIT DATA	3A4
1TDAT1	CH 1 TRANSMIT DATA	3A2
2TDAT1	CH 2 TRANSMIT DATA	4A4
3TDAT1	CH 3 TRANSMIT DATA	4A2
4TDAT1	CH 4 TRANSMIT DATA	5A4
5TDAT1	CH 5 TRANSMIT DATA	5A2
6TDAT1	CH 6 TRANSMIT DATA	6A4
7TDAT1	CH 7 TRANSMIT DATA	6A2
UDR1	MULTIPLEXED DATA READY STATUS	9C2
URCR1	MULTIPLEXED REVERSE CHANNEL RECEIVE	9C4
URING1	MULTIPLEXED RING	9D4
UTBRE1	MULTIPLEXED TRANSMIT BUFFER REGISTER EMPTY	9D1
WRT0	MULTIPLEXED WRITE CONTROL STATUS	9B3

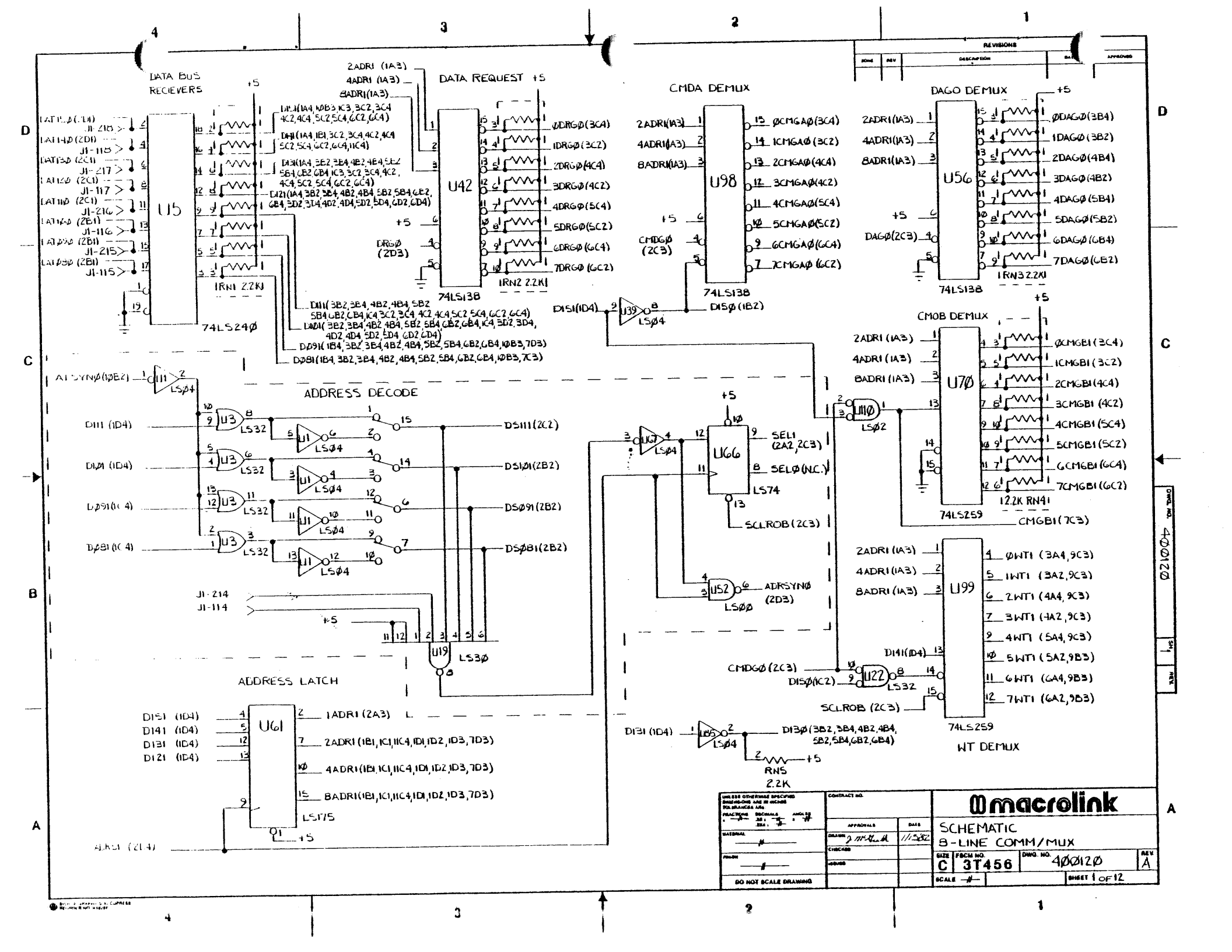
APPENDIX Cont...

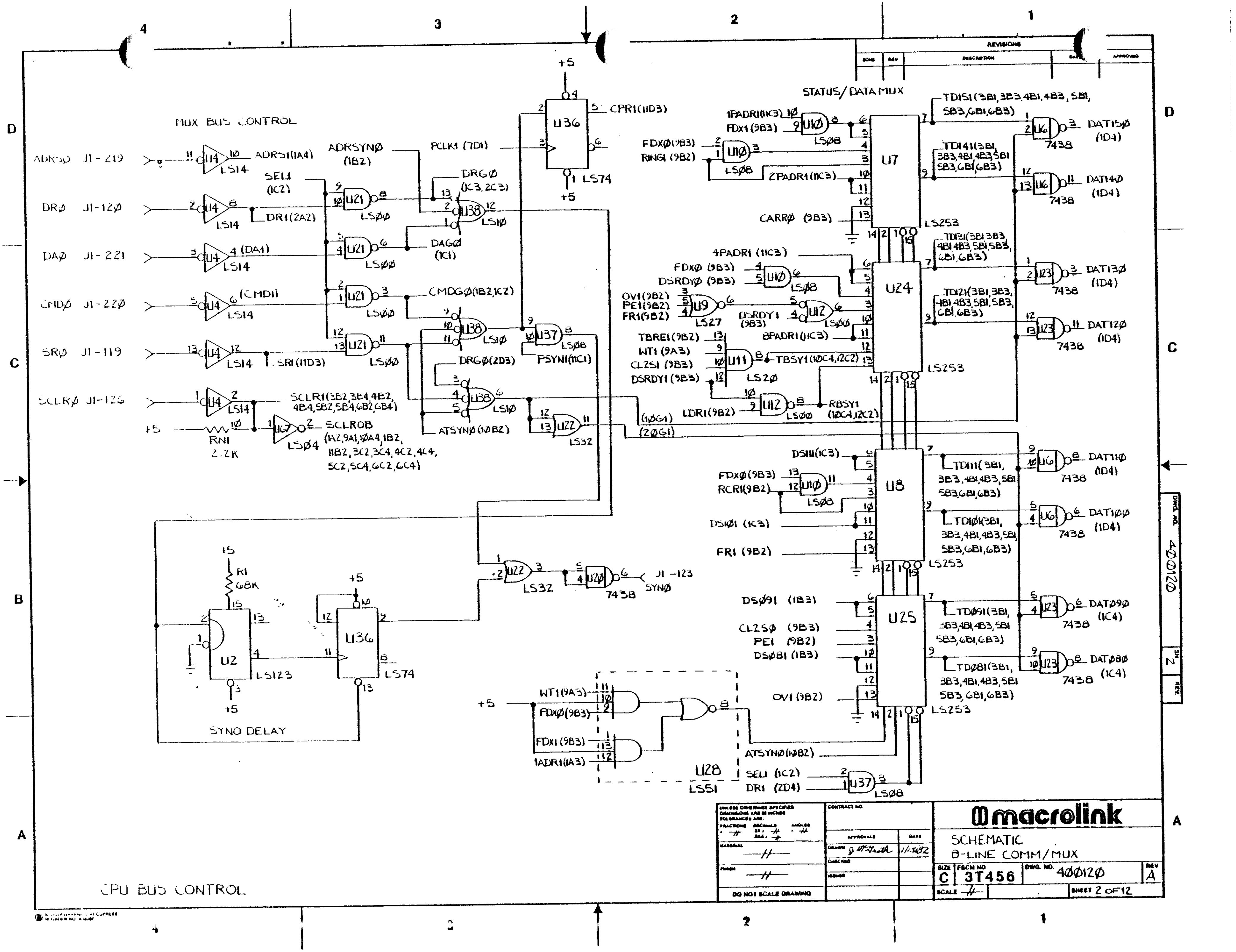
MNEMONIC	MEANING	LOCATION
WRT1	MULTIPLEXED WRITE CONTROL STATUS	9A3
0WRT0	CH 0 WRITE CONTROL STATUS	3B3
1WRT0	CH 2 WRITE CONTROL STATUS	3B1
2WRT0	CH 2 WRITE CONTROL STATUS	4B3
3WRT0	CH 3 WRITE CONTROL STATUS	4B1
4WRT0	CH 4 WRITE CONTROL STATUS	5B3
5WRT0	CH 5 WRITE CONTROL STATUS	5B1
6WRT0	CH 6 WRITE CONTROL STATUS	6B3
7WRT0	CH 6 WRITE CONTROL STATUS	6B1
0WT1	CH 0 WRITE COMMAND	1B1
1WT1	CH 1 WRITE COMMAND	1B1
2WT1	CH 2 WRITE COMMAND	1B1
3WT1	CH 3 WRITE COMMAND	1B1
4WT1	CH 4 WRITE COMMAND	1B1
5WT1	CH 5 WRITE COMMAND	1B1
6WT1	CH 6 WRITE COMMAND	1B1
7WT1	CH 7 WRITE COMMAND	1A1

1WT1	CH 1 WRITE COMMAND	1B1

APPENDIX Cont...

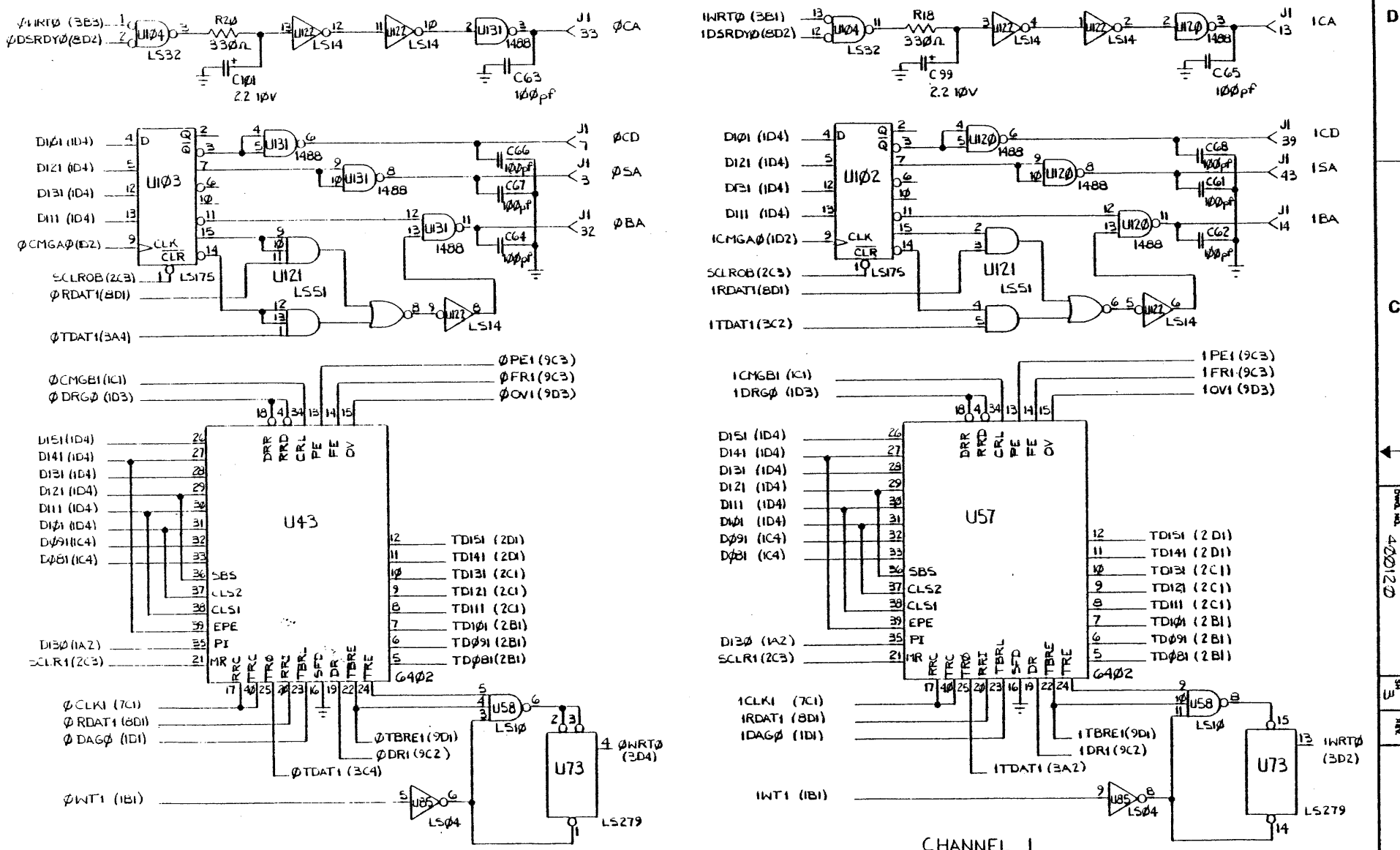
MNEMONIC	MEANING	LOCATION
2WT1	CH 2 WRITE COMMAND	1B1
3WT1	CH 3 WRITE COMMAND	1B1
4WT1	CH 4 WRITE COMMAND	1B1
5WT1	CH 5 WRITE COMMAND	1B1
6WT1	CH 6 WRITE COMMAND	1B1
7WT1	CH 7 WRITE COMMAND	1A1

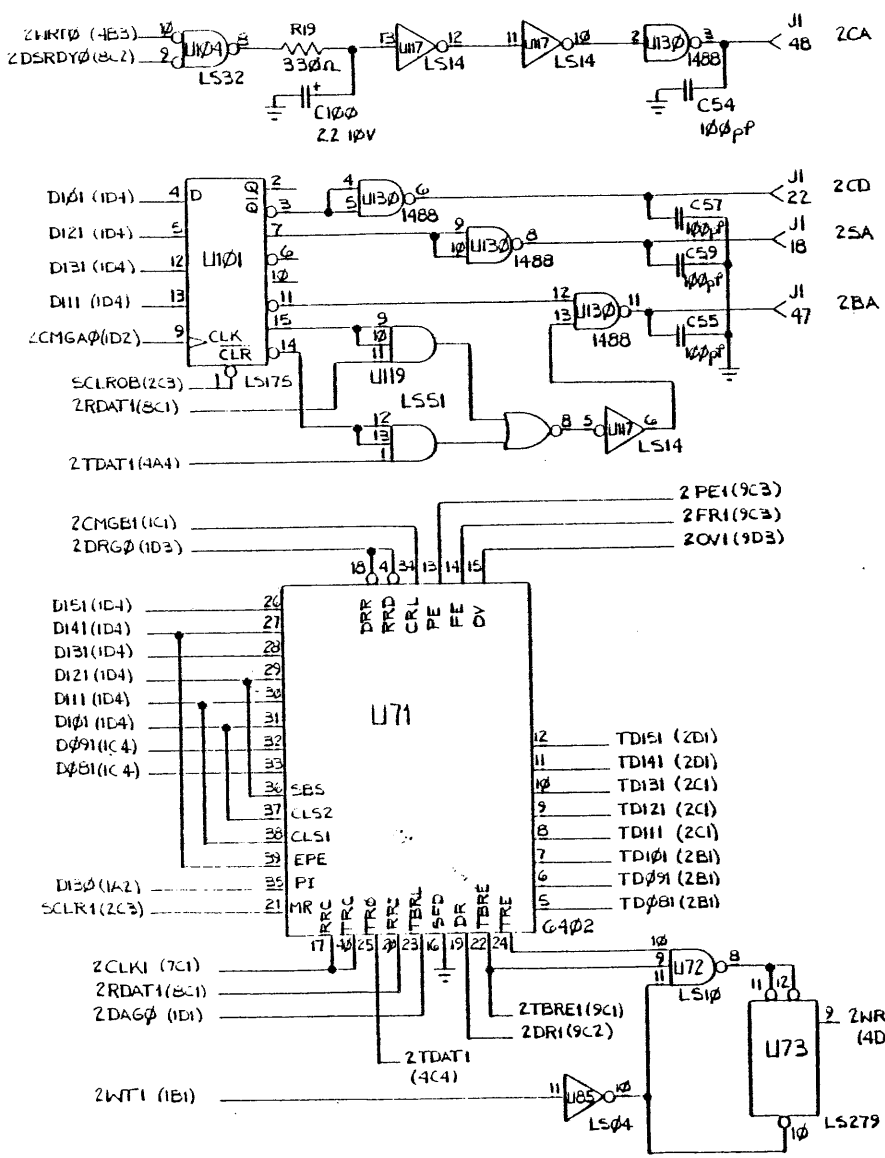

DATA BUS RECIEVERS
U15
74LS240
IRN1 2.2K
DATA REQUEST
U42
74LS138
IRN2 2.2K
CMDA DEMUX
U98
74LS138
DAGØ DEMUX
U56
74LS138
IRN3 2.2K
CMØB DEMUX
U7Ø
74LS259
12.2K RN4
ADDRESS DECODE
ADDRESS LATCH
U61
LS175
U66
LS74
U99
74LS259
WT DEMUX
RN5
2.2K
macrolink
SCHEMATIC
8-LINE COMM/MUX
SIZE C
FSCM NO. 3T456
DWG. NO. 4ØØ12Ø
REV. A
SCALE —
SHEET 1 OF 12
DO NOT SCALE DRAWING



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CONTRACT NO
DRAWN	11/5/82
SCHEMATIC 8-LINE COMM/MUX	macrolink
SIZE C	FSCM NO 3T456
DWG. NO. 400120	REV A
SCALE	SHEET 2 OF 12

DO NOT SCALE DRAWING


REVISIONS
ZONE REV DESCRIPTION APPROVED
ØWRTØ (3B3)
ØDSRDYØ(8D2)
U1Ø4
LS32
R2Ø
33ØΩ
C1Ø1
2.2 1ØV
U122
LS14
U131
1488
C63
1ØØpf
J1
33
ØCA
DIØ1 (1D4)
DI21 (1D4)
DI31 (1D4)
DI11 (1D4)
ØCMGAØ(1D2)
SCLROB(2C3)
ØRDAT1(8D1)
ØTDAT1(3A4)
U1Ø3
CLK
CLR
LS175
U121
LS51
C66
C67
C64
ØCD
ØSA
ØBA
ØCMGB1(1C1)
Ø DRGØ (1D3)
ØPE1 (9C3)
ØFR1(9C3)
ØOV1 (9D3)
DI51(1D4)
DI41 (1D4)
DI31 (1D4)
DI21 (1D4)
DI11 (1D4)
DIØ1 (1D4)
DØ91(1C4)
DØ81(1C4)
U43
DRR RRD CRL PE FE OV
SBS
CLS2
CLS1
EPE
PI
MR
TRC TRO RRC RRI TBRL SFD DR TBRE TRE
64Ø2
TDI51 (2D1)
TDI41 (2D1)
TDI31 (2C1)
TDI21 (2C1)
TDI11 (2C1)
TDIØ1 (2B1)
TDØ91 (2B1)
TDØ81(2B1)
DI3Ø (1A2)
SCLR1(2C3)
Ø CLK1 (7C1)
Ø RDAT1 (8D1)
Ø DAGØ (1D1)
ØTDAT1 (3C4)
ØTBRE1(9D1)
ØDR1 (9C2)
U58
LSIØ
U73
LS279
ØWRTØ (3D4)
ØWT1 (1B1)
U85
LSØ4
CHANNEL Ø
1WRTØ (3B1)
1DSRDYØ(8D2)
R18
C99
C65
1CA
1CD
1SA
1BA
1CMGAØ(1D2)
1RDAT1(8D1)
1TDAT1(3C2)
U1Ø2
U121
1CMGB1 (1C1)
1DRGØ (1D3)
1PE1 (9C3)
1FR1 (9C3)
1OV1 (9D3)
DI3Ø (1A2)
SCLR1(2C3)
1CLK1 (7C1)
1RDAT1 (8D1)
1DAGØ (1D1)
1TDAT1(3A2)
1TBRE1(9D1)
1DR1 (9C2)
1WT1 (1B1)
1WRTØ (3D2)
CHANNEL 1
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
DO NOT SCALE DRAWING
CONTRACT NO
APPROVALS DATE
DRAWN J. McSmith 1/15/82
CHECKED
ISSUED
macrolink
SCHEMATIC
8 LINE COMM/MUX
SIZE C FSCM NO. 3T456 DWG NO. 4ØØ12Ø REV A
SCALE SHEET 3OF12
DWG NO 4ØØ12Ø
SHT
REV



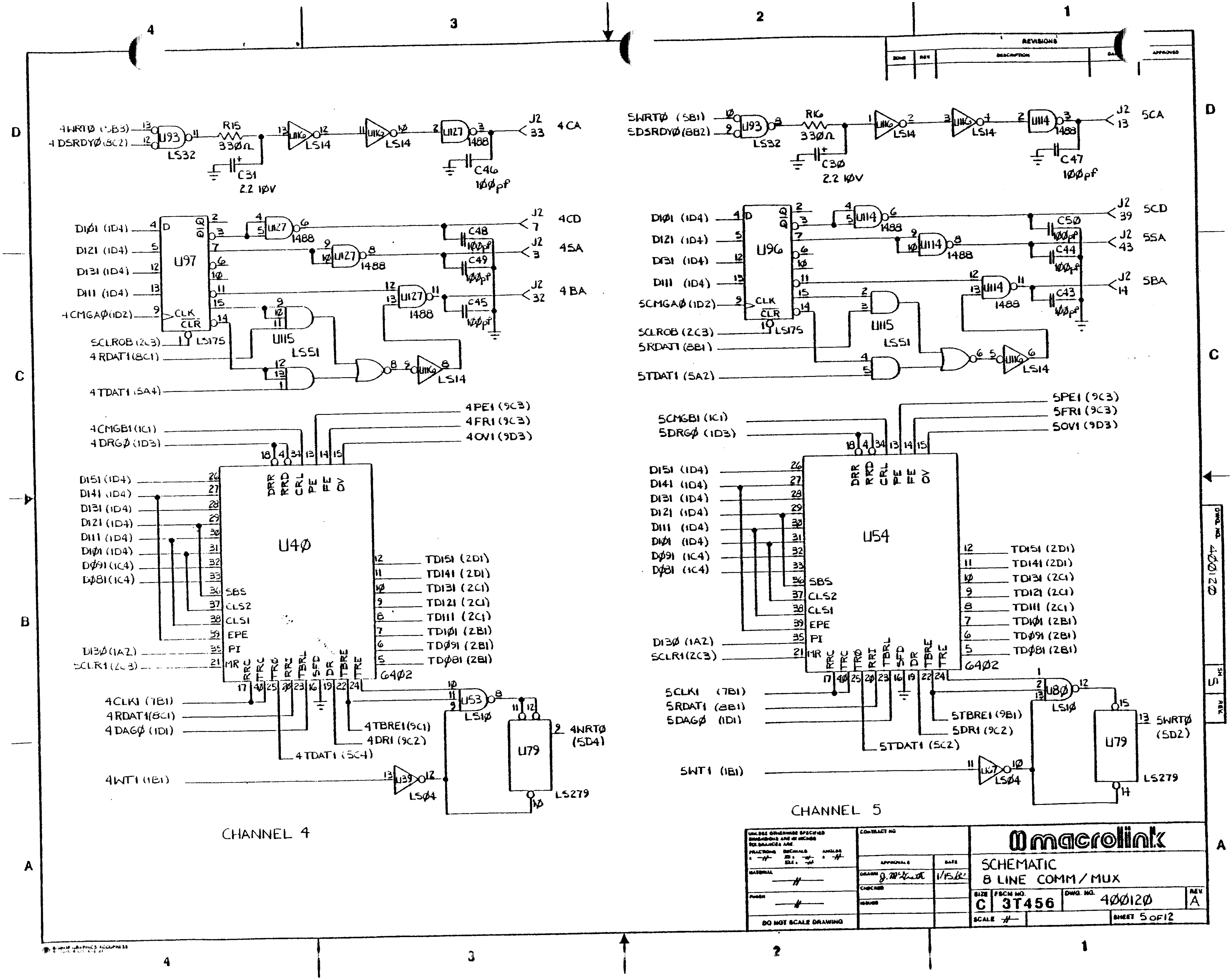
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

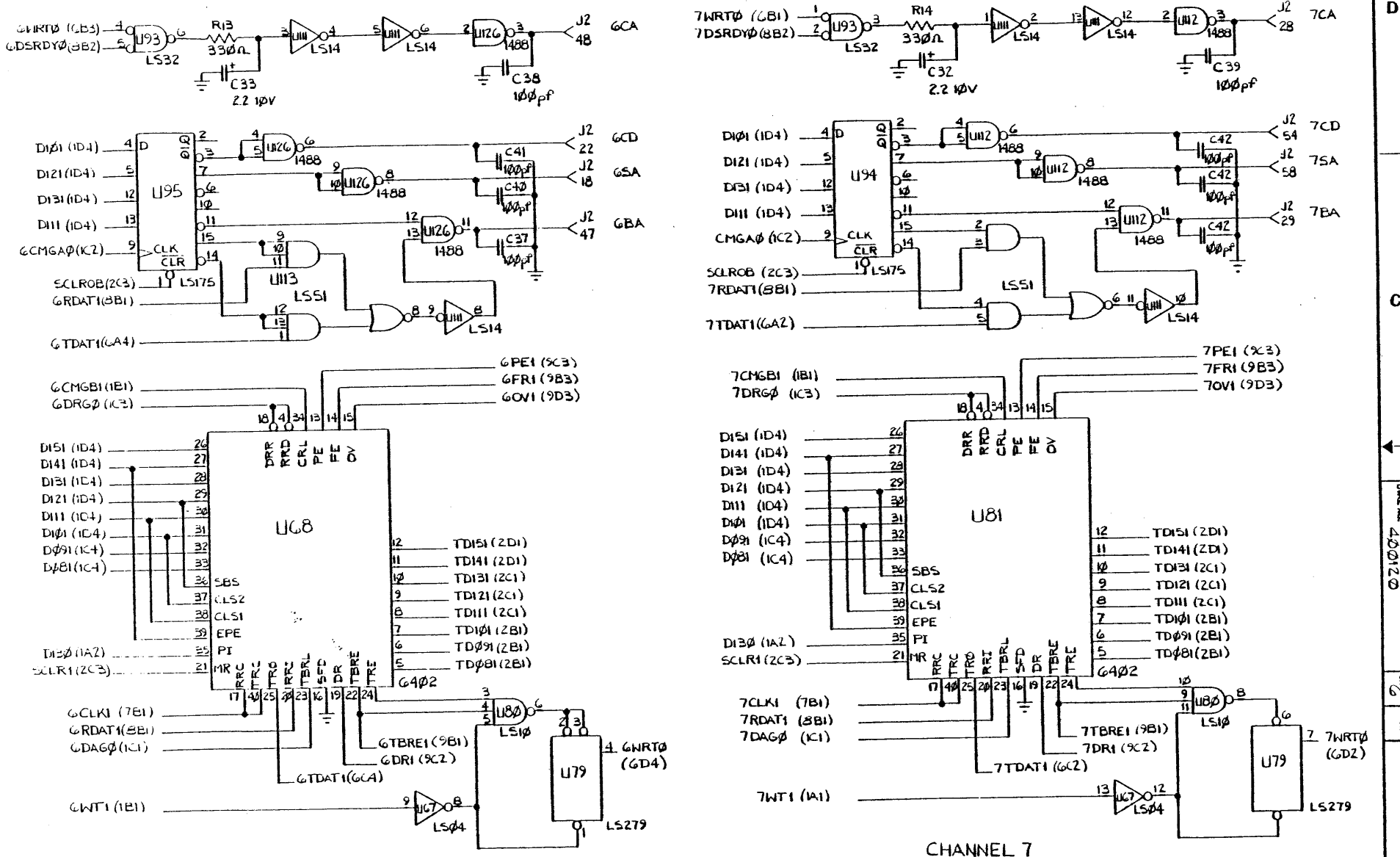
DWG. NO. 4ØØ12Ø

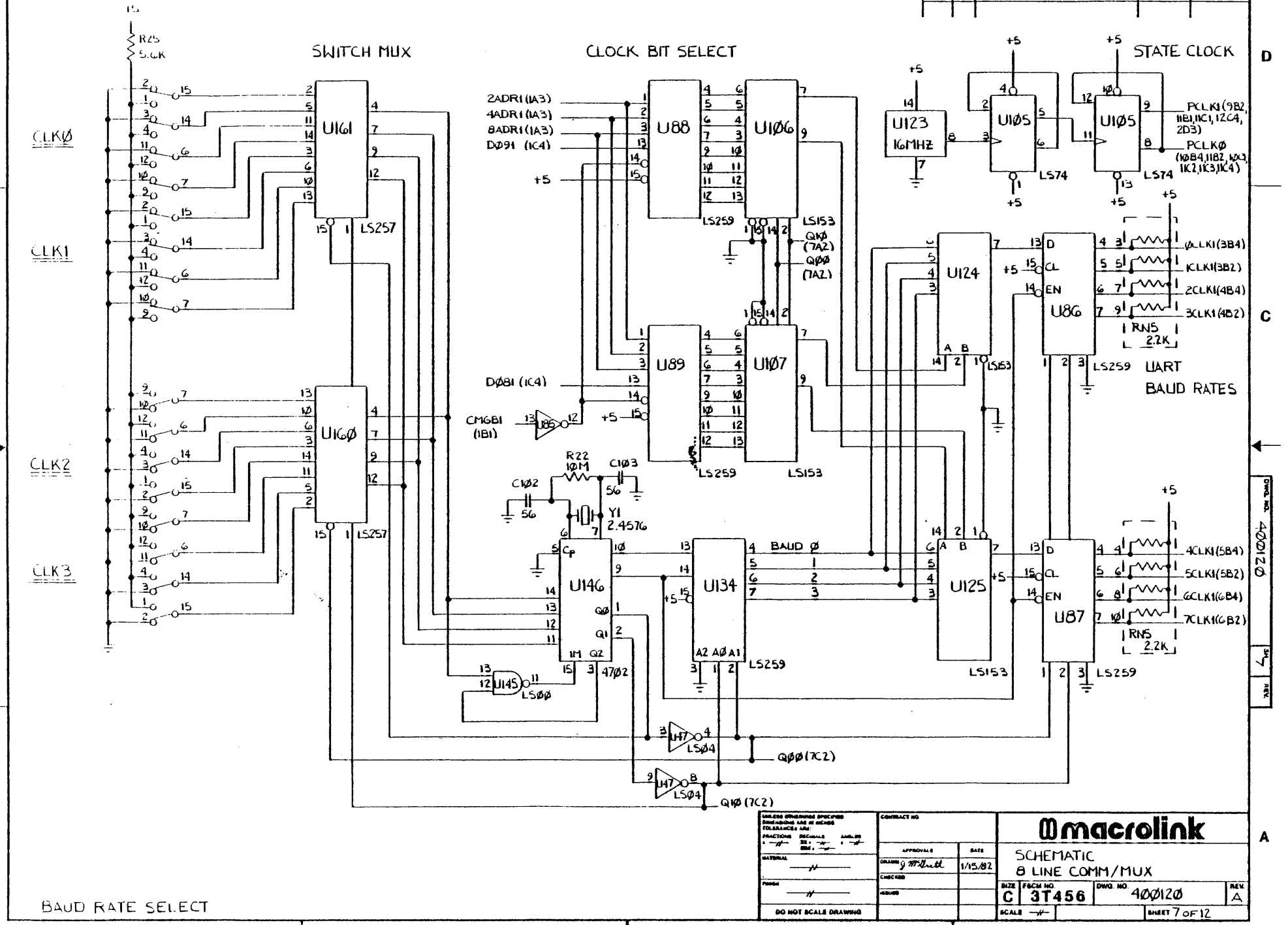
SH. 4

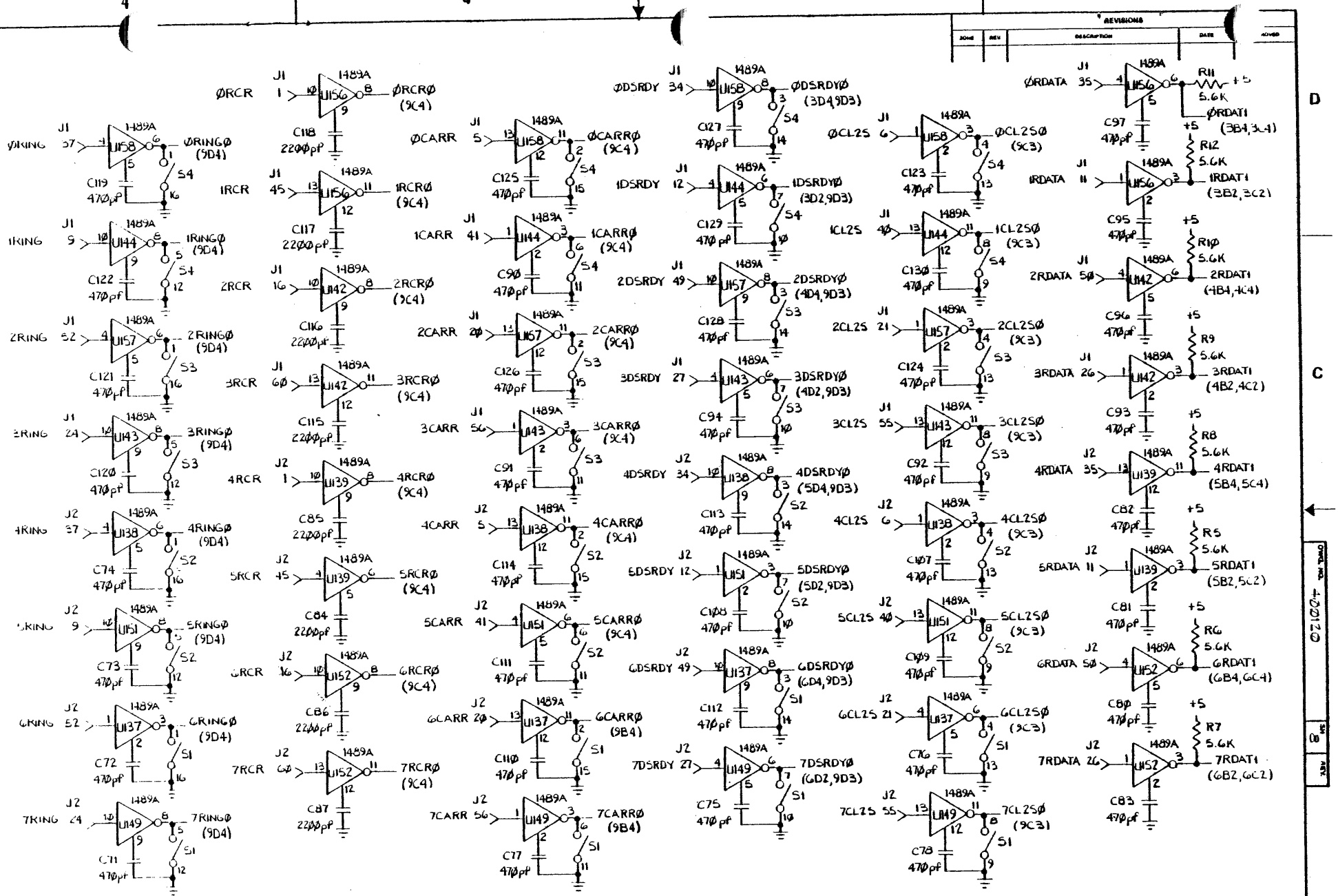
REV.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	CONTRACT NO.	macrolink	
MATERIAL —	APPROVALS	SCHEMATIC	
FINISH —	DRAWN G. Mitchell 1/15/92	8 LINE COMM/MUX	
DO NOT SCALE DRAWING	CHECKED	SIZE C FSCM NO. 3T456	DWG. NO. 4ØØ12Ø REV A
	ISSUED	SCALE —	SHEET 4 OF 12


4WRTØ (5B3)
4DSRDYØ (8C2)
U93
LS32
R15
330Ω
C31
2.2 10V
U116
LS14
U127
1488
C46
100pf
J2
33
4CA
D101 (1D4)
D121 (1D4)
D131 (1D4)
D111 (1D4)
4CMGAØ (1D2)
SCLROB (2C3)
4RDAT1 (8C1)
4TDAT1 (5A4)
U97
LS175
U115
LS51
C48
C49
C45
4CD
4SA
4BA
4CMGB1 (1C1)
4DRGØ (1D3)
4PE1 (9C3)
4FR1 (9C3)
4OV1 (9D3)
U40
6402
TD151 (2D1)
TD141 (2D1)
TD131 (2C1)
TD121 (2C1)
TD111 (2C1)
TD101 (2B1)
TD091 (2B1)
TD081 (2B1)
DI30 (1A2)
SCLR1 (2C3)
4CLK1 (7B1)
4RDAT1 (8C1)
4DAGØ (1D1)
4TBRE1 (9C1)
4DR1 (9C2)
4TDAT1 (5C4)
4WT1 (1E1)
U53
LS10
U39
LS04
U79
LS279
4WRTØ (5D4)
CHANNEL 4
5WRTØ (5B1)
5DSRDYØ (8B2)
R16
C30
C47
5CA
5CD
5SA
5BA
C50
C44
C43
U96
U114
5CMGAØ (1D2)
5RDAT1 (8B1)
5TDAT1 (5A2)
5PE1 (9C3)
5FR1 (9C3)
5OV1 (9D3)
5CMGB1 (1C1)
5DRGØ (1D3)
U54
5CLK1 (7B1)
5RDAT1 (2B1)
5DAGØ (1D1)
5TBRE1 (9B1)
5DR1 (9C2)
5TDAT1 (5C2)
5WT1 (1B1)
U80
U67
5WRTØ (5D2)
CHANNEL 5
REVISIONS
DO NOT SCALE DRAWING
macrolink
SCHEMATIC
8 LINE COMM / MUX
SIZE C
FSCM NO. 3T456
DWG. NO. 400120
REV. A
SHEET 5 OF 12
400120


6WRTØ (6B3)
6DSRDYØ(8B2)
U93
LS32
R13
330Ω
C33
2.2 10V
LS14
U126
1488
C38
100pf
J2
48
6CA
DIØ1 (1D4)
DI21 (1D4)
DI31 (1D4)
DI11 (1D4)
6CMGAØ(1C2)
SCLR0B(2C3)
6RDAT1(8B1)
6TDAT1(6A4)
U95
CLK
CLR
LS175
U113
LS51
C41
C40
C37
J2
22
18
47
6CD
6SA
6BA
6CMGB1(1B1)
6DRGØ (1C3)
6PE1 (5C3)
6FR1 (9B3)
6OV1 (9D3)
DI51 (1D4)
DI41 (1D4)
DI31 (1D4)
DI21 (1D4)
DI11 (1D4)
DIØ1 (1D4)
DØ91 (1C4)
DØ81(1C4)
DI3Ø (1A2)
SCLR1(2C3)
U68
DRR
RRD
CRL
PE
FE
OV
SBS
CLS2
CLS1
EPE
PI
MR
TRC
TRD
RRC
TBRL
SFD
DR
TBRE
TRE
TDI51 (2D1)
TDI41 (2D1)
TDI31 (2C1)
TDI21 (2C1)
TDI11 (2C1)
TDIØ1 (2B1)
TDØ91 (2B1)
TDØ81(2B1)
64Ø2
6CLK1 (7B1)
6RDAT1(8B1)
6DAGØ(1C1)
6TBRE1(9B1)
6DR1 (9C2)
6TDAT1(6C4)
6WT1 (1B1)
U8Ø
LS1Ø
U67
LSØ4
U79
LS279
6WRTØ
(6D4)
CHANNEL 6
7WRTØ (6B1)
7DSRDYØ(8B2)
U93
LS32
R14
330Ω
C32
2.2 10V
LS14
U112
1488
C39
100pf
J2
28
7CA
DIØ1 (1D4)
DI21 (1D4)
DI31 (1D4)
DI11 (1D4)
CMGAØ (1C2)
SCLR0B (2C3)
7RDAT1(8B1)
7TDAT1(6A2)
U94
CLK
CLR
LS175
LS51
C42
J2
54
58
29
7CD
7SA
7BA
7CMGB1 (1B1)
7DRGØ (1C3)
7PE1 (9C3)
7FR1 (9B3)
7OV1 (9D3)
DI51 (1D4)
DI41 (1D4)
DI31 (1D4)
DI21 (1D4)
DI11 (1D4)
DIØ1 (1D4)
DØ91 (1C4)
DØ81 (1C4)
DI3Ø (1A2)
SCLR1(2C3)
U81
DRR
RRD
CRL
PE
FE
OV
SBS
CLS2
CLS1
EPE
PI
MR
TRC
TRD
RRC
TBRL
SFD
DR
TBRE
TRE
TDI51 (2D1)
TDI41 (2D1)
TDI31 (2C1)
TDI21 (2C1)
TDI11 (2C1)
TDIØ1 (2B1)
TDØ91 (2B1)
TDØ81(2B1)
64Ø2
7CLK1 (7B1)
7RDAT1 (8B1)
7DAGØ (1C1)
7TBRE1 (9B1)
7DR1 (9C2)
7TDAT1 (6C2)
7WT1 (1A1)
U8Ø
LS1Ø
U67
LSØ4
U79
LS279
7WRTØ
(6D2)
CHANNEL 7
macrolink
SCHEMATIC
8 LINE COMM/MUX
SIZE C
FSCM NO. 3T456
DWG. NO. 4ØØ12Ø
REV. A
SCALE
SHEET 6 OF 12
DO NOT SCALE DRAWING
CONTRACT NO.
APPROVALS
DATE
1/15/82
DRAWN
CHECKED
ISSUED
MATERIAL
FINISH
REVISIONS
DESCRIPTION
DATE
APPROVED
DWG. NO. 4ØØ12Ø
SH 6
REV. A


SWITCH MUX
CLOCK BIT SELECT
STATE CLOCK
UART BAUD RATES
BAUD RATE SELECT
CLKØ
CLK1
CLK2
CLK3
R25 5.6K
U161
U16Ø
LS257
U88
U89
U1Ø6
U1Ø7
LS259
LS153
2ADR1 (1A3)
4ADR1 (1A3)
8ADR1 (1A3)
DØ91 (1C4)
DØ81 (1C4)
CMGBI (1B1)
U123 16MHZ
U1Ø5
LS74
PCLK1 (9B2, 11B1, 11C1, 12C4, 2D3)
PCLKØ (1ØB4, 11B2, 1ØC3, 11C2, 11C3, 11C4)
U124
U125
U86
U87
ØCLK1(3B4)
1CLK1(3B2)
2CLK1(4B4)
3CLK1(4B2)
4CLK1(5B4)
5CLK1(5B2)
6CLK1(6B4)
7CLK1(6B2)
RNS 2.2K
R22 1ØM
C1Ø3 56
C1Ø2 56
Y1 2.4576
U146
U134
U145
LSØØ
47Ø2
U17
LSØ4
QØØ (7C2)
QØ (7C2)
BAUD Ø
macrolink
SCHEMATIC
8 LINE COMM/MUX
DO NOT SCALE DRAWING
SIZE C
FSCM NO. 3T456
DWG. NO. 4ØØ12Ø
REV. A
SCALE
SHEET 7 OF 12



REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APVD

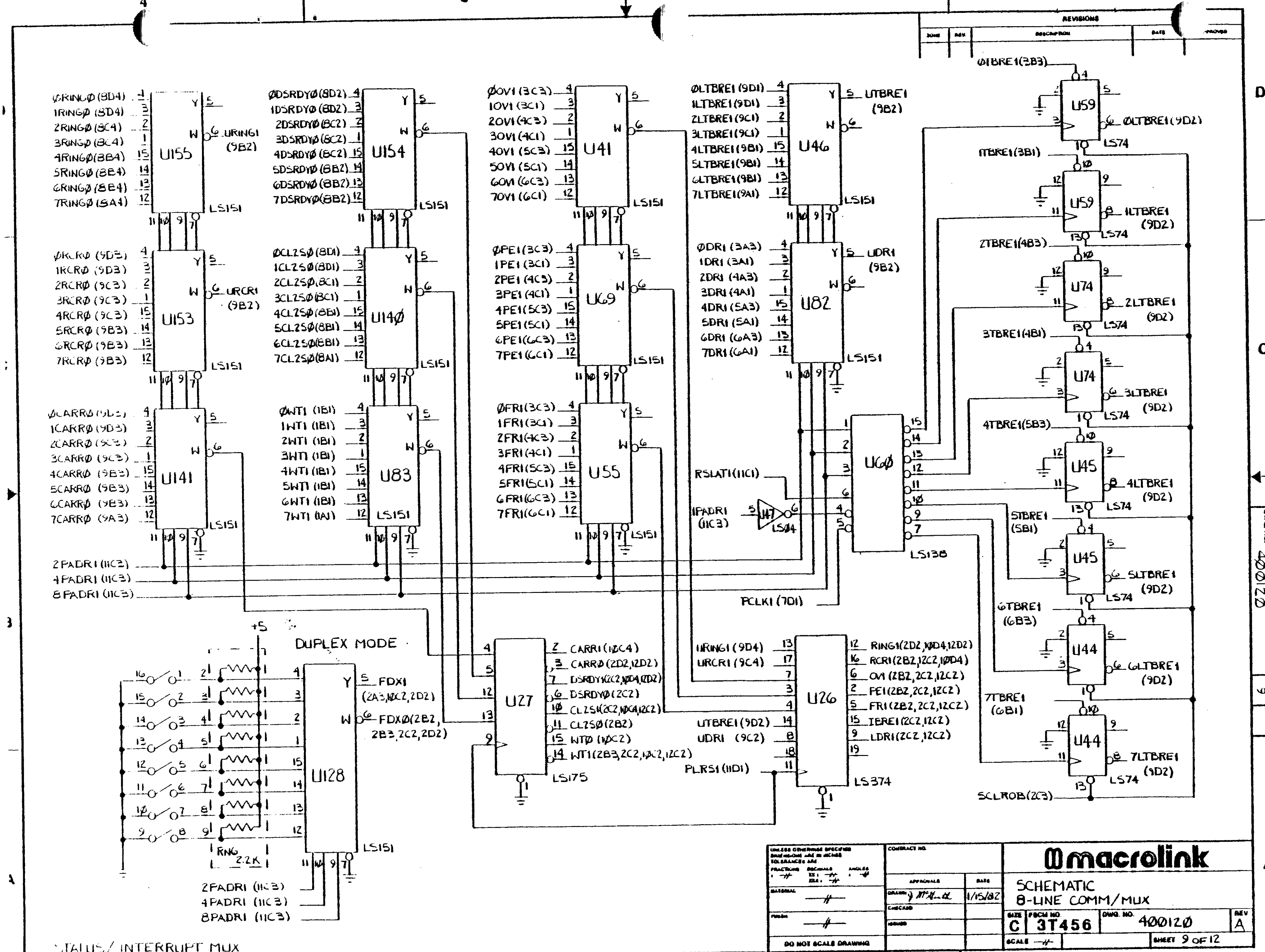
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	CONTRACT NO	macrolink
MATERIAL	APPROVALS	DATE
FINISH	DRAWN	1/15/82
DO NOT SCALE DRAWING	CHECKED	
	ENGR	

SCHEMATIC
8-LINE COMM/MUX

SIZE	FSCM NO.	DWG. NO.	REV.
C	3T456	400120	A

SCALE — SHEET 8 OF 12

OTHER NO. 400120 SH 08 REV.


REVISIONS
ZONE REV DESCRIPTION DATE APPROVED
ØRINGØ(8D4) 1RINGØ(8D4) 2RINGØ(8C4) 3RINGØ(8C4) 4RINGØ(8B4) 5RINGØ(8B4) 6RINGØ(8B4) 7RINGØ(8A4)
U155 LS151 URING1 (9B2)
ØRCRØ(9D3) 1RCRØ(9D3) 2RCRØ(9C3) 3RCRØ(9C3) 4RCRØ(9C3) 5RCRØ(9B3) 6RCRØ(9B3) 7RCRØ(9B3)
U153 LS151 URCR1 (9B2)
ØCARRØ(9D3) 1CARRØ(9D3) 2CARRØ(9C3) 3CARRØ(9C3) 4CARRØ(9B3) 5CARRØ(9B3) 6CARRØ(9B3) 7CARRØ(9A3)
U141 LS151
ØDSRDYØ(8D2) 1DSRDYØ(8D2) 2DSRDYØ(8C2) 3DSRDYØ(8C2) 4DSRDYØ(8C2) 5DSRDYØ(8B2) 6DSRDYØ(8B2) 7DSRDYØ(8B2)
U154 LS151
ØCLZSØ(8D1) 1CLZSØ(8D1) 2CLZSØ(8C1) 3CLZSØ(8C1) 4CLZSØ(8B1) 5CLZSØ(8B1) 6CLZSØ(8B1) 7CLZSØ(8A1)
U14Ø LS151
ØWT1 (1B1) 1WT1 (1B1) 2WT1 (1B1) 3WT1 (1B1) 4WT1 (1B1) 5WT1 (1B1) 6WT1 (1B1) 7WT1 (1A1)
U83 LS151
ØOV1(3C3) 1OV1(3C1) 2OV1(4C3) 3OV1(4C1) 4OV1(5C3) 5OV1(5C1) 6OV1(6C3) 7OV1(6C1)
U41 LS151
ØPE1(3C3) 1PE1(3C1) 2PE1(4C3) 3PE1(4C1) 4PE1(5C3) 5PE1(5C1) 6PE1(6C3) 7PE1(6C1)
U69 LS151
ØFR1(3C3) 1FR1(3C1) 2FR1(4C3) 3FR1(4C1) 4FR1(5C3) 5FR1(5C1) 6FR1(6C3) 7FR1(6C1)
U55 LS151
ØLTBRE1(9D1) 1LTBRE1(9D1) 2LTBRE1(9C1) 3LTBRE1(9C1) 4LTBRE1(9B1) 5LTBRE1(9B1) 6LTBRE1(9B1) 7LTBRE1(9A1)
U46 LS151 UTBRE1 (9B2)
ØDR1(3A3) 1DR1(3A1) 2DR1(4A3) 3DR1(4A1) 4DR1(5A3) 5DR1(5A1) 6DR1(6A3) 7DR1(6A1)
U82 LS151 UDR1 (9B2)
2PADR1 (11C3) 4PADR1 (11C3) 8PADR1 (11C3)
RSLAT1(11C1) 1PADR1 (11C3) U47 LS04
U6Ø LS138
PCLK1 (7D1)
ØTBRE1(3B3) U59 LS74 ØLTBRE1(9D2)
1TBRE1(3B1) U59 LS74 1LTBRE1 (9D2)
2TBRE1(4B3) U74 LS74 2LTBRE1 (9D2)
3TBRE1(4B1) U74 LS74 3LTBRE1 (9D2)
4TBRE1(5B3) U45 LS74 4LTBRE1 (9D2)
5TBRE1 (5B1) U45 LS74 5LTBRE1 (9D2)
6TBRE1 (6B3) U44 LS74 6LTBRE1 (9D2)
7TBRE1 (6B1) U44 LS74 7LTBRE1 (9D2)
SCLROB(2C3)
+5
DUPLEX MODE
RN6 2.2K
U128 LS151 FDX1 (2A3,12C2,2D2) FDXØ(2B2, 2B3,2C2,2D2)
U27 LS175
CARR1(12C4) CARRØ(2D2,12D2) DSRDY1(2C2,10D4,12D2) DSRDYØ(2C2) CLZS1(2C2,10C4,12C2) CLZSØ(2B2) WTØ (10C2) WT1(2B3,2C2,10C2,12C2)
URING1 (9D4) URCR1 (9C4) UTBRE1(9D2) UDR1 (9C2) PLRS1 (11D1)
U26 LS374
RING1(2D2,10D4,12D2) RCR1(2B2,12C2,10D4) OV1 (2B2,2C2,12C2) PE1(2B2,2C2,12C2) FR1(2B2,2C2,12C2) TBRE1(2C2,12C2) LDR1(2C2,12C2)

STATUS / INTERRUPT MUX

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:

CONTRACT NO.

DRAWN 1/15/82

CHECKED

ISSUED

DO NOT SCALE DRAWING

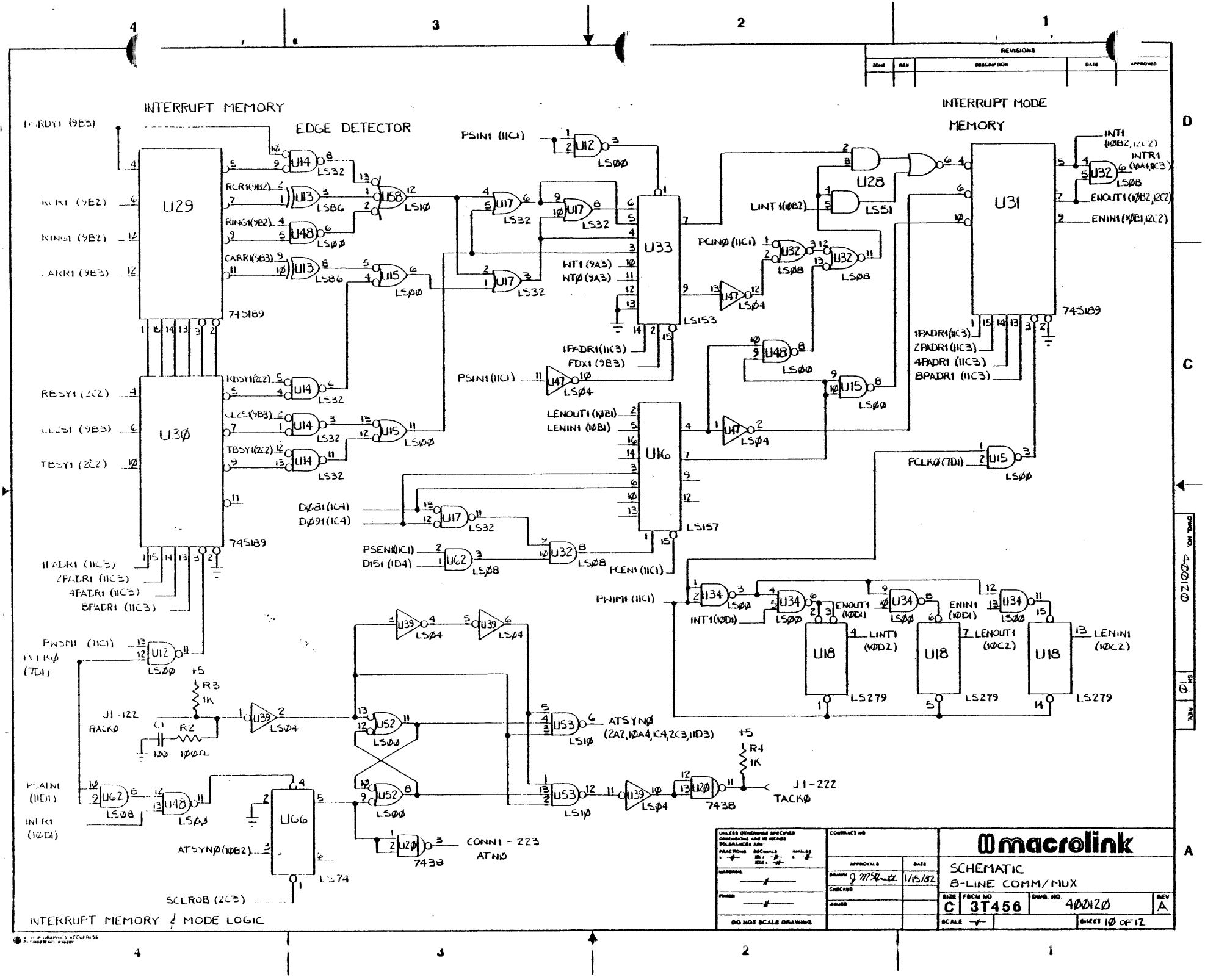
macrolink

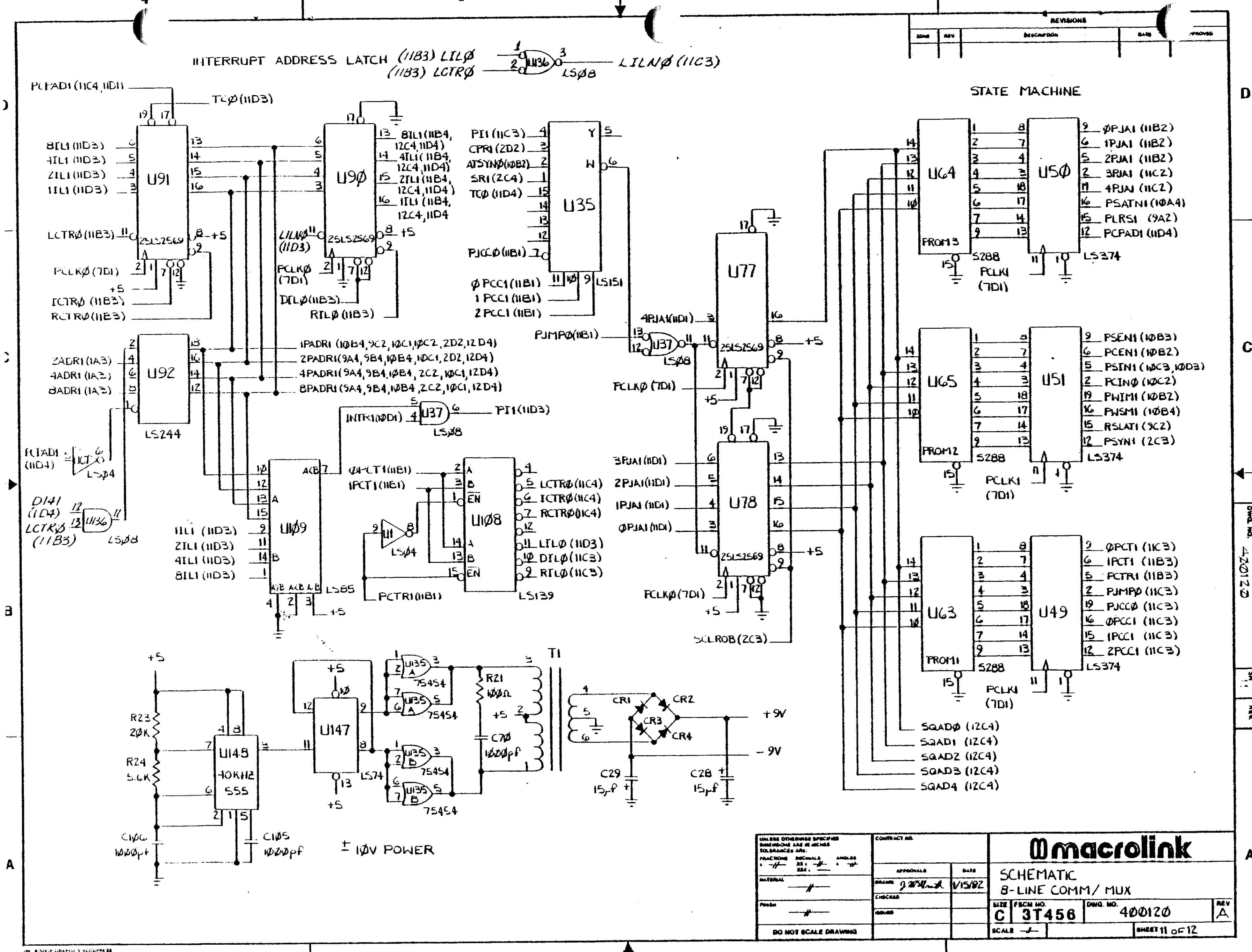
SCHEMATIC
8-LINE COMM/MUX

SIZE	FSCM NO.	DWG. NO.	REV
C	3T456	400120	A

SCALE — SHEET 9 OF 12

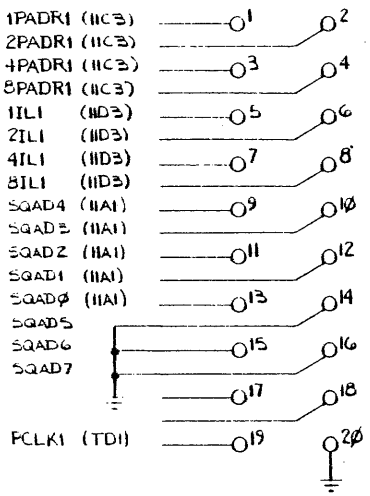
DWG. NO. 400120 SH 9


INTERRUPT MEMORY
EDGE DETECTOR
INTERRUPT MODE
MEMORY
U29
U30
U31
U33
U16
745189
LS153
LS157
U28
LS51
U18
LS279
7438
LS74
INTERRUPT MEMORY & MODE LOGIC
SCHEMATIC
8-LINE COMM/MUX
macrolink
SIZE C
FSCM NO 3T456
DWG NO 400120
REV A
SHEET 10 OF 12
DO NOT SCALE DRAWING

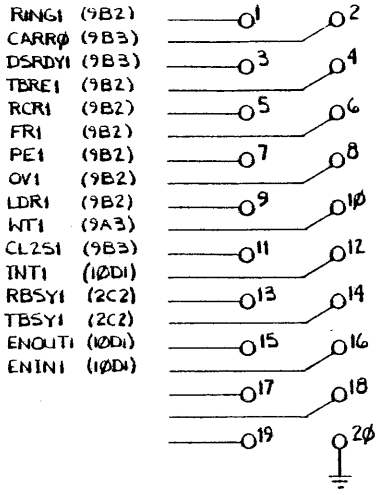

INTERRUPT ADDRESS LATCH
STATE MACHINE
U91
U90
U35
U92
U109
U108
U77
U78
U64
U50
U65
U51
U63
U49
U148
U147
LS244
LS85
LS139
LS151
LS374
5288
PROM3
PROM2
PROM1
LS74
75454
40KHZ
555
T1
CR1
CR2
CR3
CR4
R21 100Ω
C70 1000pf
R23 20K
R24 5.6K
C106 1000pf
C105 1000pf
C29 15μf
C28 15μf
+9V
-9V
± 10V POWER
SQAD0 (12C4)
SQAD1 (12C4)
SQAD2 (12C4)
SQAD3 (12C4)
SQAD4 (12C4)
DO NOT SCALE DRAWING
macrolink
SCHEMATIC
8-LINE COMM/ MUX
C
3T456
400120
A
SHEET 11 OF 12
1/15/82

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

JA1



JB1



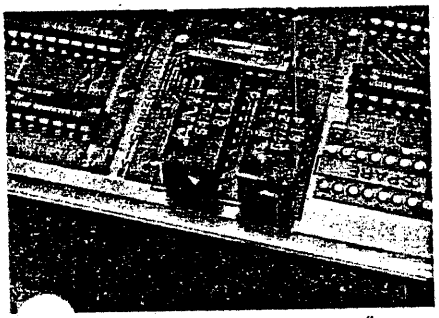
DWG. NO. 400120 SH 12 REV.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± 1/64 DECIMALS .XX ± .01 .XXX ± .005 ANGLES ± 1/2°	CONTRACT NO	macrolink	
MATERIAL —	APPROVALS	DATE	SCHEMATIC 8-LINE COMM/MUX
FINISH —	DRAWN [illegible]	11/5/82	SIZE C | FSCM NO. 3T456 | DWG. NO. 400120 | REV A
DO NOT SCALE DRAWING	CHECKED		SCALE — | SHEET 12 OF 12
	ISSUED		

wh[illegible]he computer is up and running. It's easy to change terminals or modems.

Addresses are easy to set and equally easy to change. With our 2-line PADLA, you set the addresses independently. With QALTA and COMM MUX, just make one setting and all addresses are set consecutively.

Baud Rates can be changed while your system is up—no need to schedule downtime or costly over-time service. Data rates are switch-selectable on QALTA — no need to remove the board. And they're software-controlled on PADLA and COMM MUX. Select any rate from 50 to 19,200 — in *any* combination.



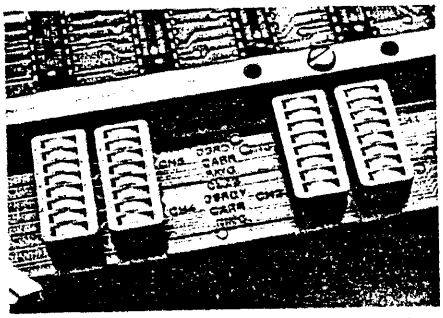
S[illegible]selectable addressing is easy to configure

Additional Macrolink advantages.

Advanced low-power Shottky and CMOS technology delivers the lowest power consumption possible. As a result, you may eliminate the need — and related costs — of an add-on power supply.

To further simplify system integration, each Macrolink COMM product comes with an internal cable that has a DAP15P connector for a pin-to-pin match with host-supplied hardware.

Macrolink provides you with advanced products, priced to give you the most cost-effective COMM solutions. Further, we assure high reliability. Each Macrolink board is thoroughly burned in, computer tested, and backed by a one-year limited warranty. And delivery takes days, instead of months.



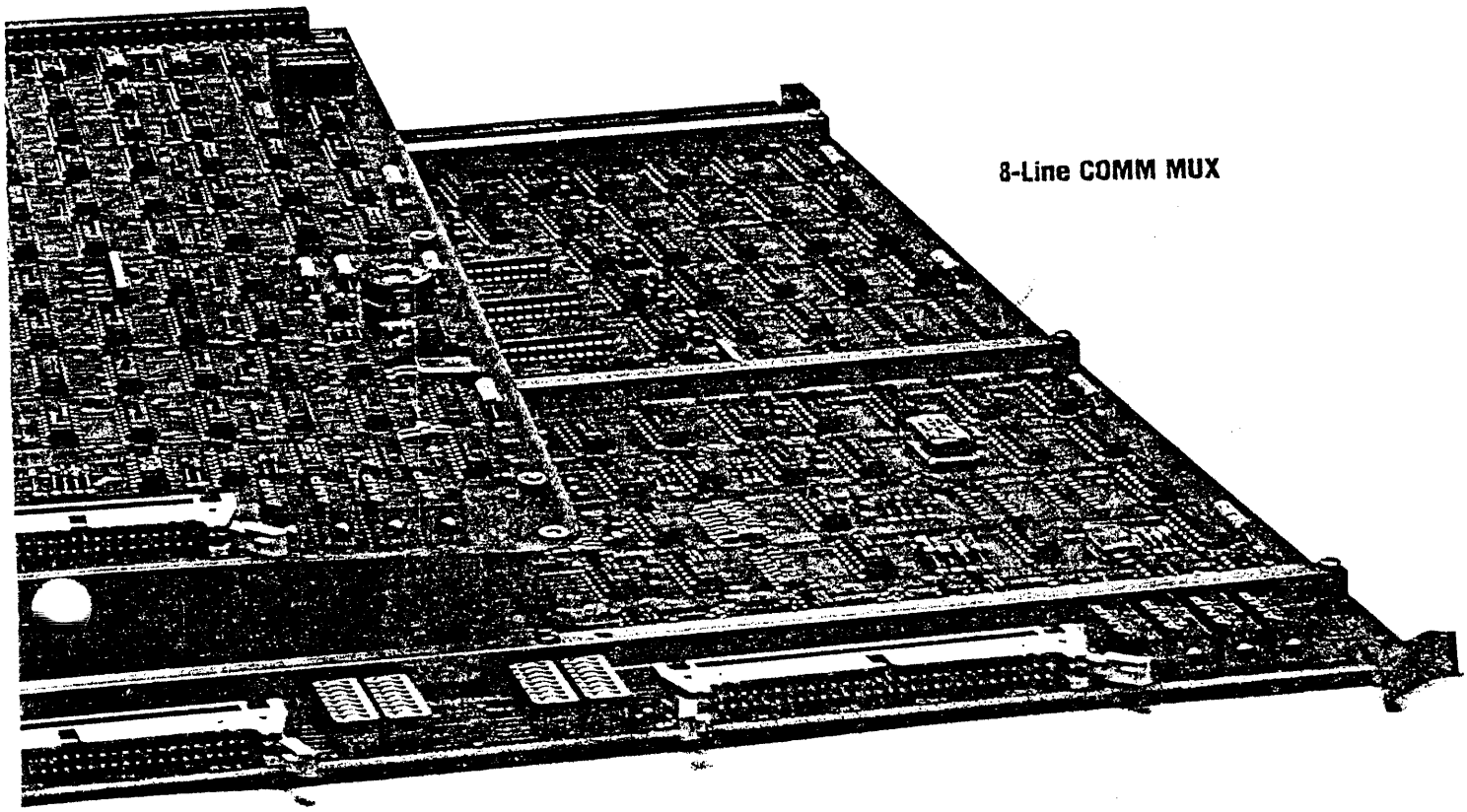
Function switches, accessible from front of board

Strong support.

The above information and specs on the back page will help you make your choice. But don't hesitate to call for application assistance. We're here to help you in every way possible, including application advice, system integration, and on-going technical back-up.

Write or call today for details.

QALTA™



8-Line COMM MUX

COMM Equipment Specifications

	PADLA Product Number 200520	QALTA Product Number 200620	8-Line COMM MUX Product Number 200720
Channels/Unit	2 RS-232-C Channels	4 RS-232-C Channels	8 RS-232-C Channels
Size	Half board	Half board	Full board
Transmission Mode	Serial; asynchronous by character, synchronous by bit. Receiver and transmitter are double buffered.		
Duplex Mode	Individual switches for each channel either half- or full-duplex.	One switch selects either half- or full-duplex for all four channels.	Individual switches for each channel either half- or full-duplex.
Device Address	Two sets of address switches allows independent selection for each channel; each channel requires two consecutive addresses.	Two hexidecimal-coded switches set the starting field of eight consecutive 10-bit addresses. LSD must be either 0 or 8.	One hexidecimal-coded switch sets the starting field of 16 consecutive 10-bit addresses. LSD must be 0.
Baud Rate	Crystal-controlled; switch selected. Available rates include 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600 or 19,200 baud. Either one of two user-designated baud rates may be selected by the clock bit of command 2 for each channel.	Crystal-controlled; switch selected. Available rates include 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600 or 19,200 baud. One switch selects each channel.	Each COMM MUX has four user-designated baud rates that may be selected by the clock bits of command 2 for each channel. The user may switch select any four of the available rates in any combination: 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600 or 19,200 baud.
Serial Format	Program-controlled/character size may be 5, 6, 7 or 8 bits. Parity is odd, even or none. 1 or 2 stop bits (1.5 bits with 5-bit data).		
Dataset Control	Data Terminal Ready (CD), Pin 2; Request to Send (CA), Pin 23; Reverse Channel Transmit (SBA), Pin 6	Reverse Channel Transmit (SBA), Pin 6	Data Terminal Ready (CD), Pin 2; Request to Send (CA), Pin 23; Reverse Channel Transmit (SBA), Pin 6
Dataset Status	Clear to Send (CB), Pin 3 Ring (CE), Pin 9 Carrier (CF), Pin 4 Reverse Channel Receive (SB), Pin 8; Dataset Ready (CC), Pin 12	Dataset Ready (CC), Pin 12	Clear to Send (CB), Pin 3 Ring (CE), Pin 9 Carrier (CF), Pin 4 Reverse Channel Receive (SB), Pin 8; Dataset Ready (CC), Pin 12
Status Disable	CF, CC and CB may be disabled for either channel via switches on the module.	Internal switch permits disabling Dataset Ready lines. An additional switch slaves CARR OFF (bit 06) to Dataset Ready for positive indication of off-line terminal.	CF, CC and CB may be disabled for each channel via switches on the module.
Serial Data	Receive Data (BB), Pin 11 Transmit Data (BA), Pin 14	Receive Data (BB), Pin 11 Transmit Data (BA), Pin 14	Receive Data (BB), Pin 11 Transmit Data (BA), Pin 14
Echoplex	Program-controlled; permits received data to be retransmitted to the terminal, as well as transferred to the CPU.		
Interrupts	Queued on each board. The receive side of the first channel has the highest priority, the transmit side of the last channel has the lowest.		
Bus Load	One-half standard load on the multiplexer bus.		
Power Required	+5 V at 0.5 ampere typical	+5 V at 0.7 ampere typical	+5 V at 1.8 ampere typical
Internal Cable	7½' long, terminated with two DA15P connectors. Pin-compatible with Perkin-Elmer ASYNC products (PASLA, PALS, 2 CH COMM MUX, 8 CH COMM MUX)*	7½' long, terminated with four DA15P connectors. Pin-compatible with Perkin-Elmer ASYNC products (PASLA, PALS, 2 CH COMM MUX, 8 CH COMM MUX)*	Two cables, 7½' long, terminated with four DA15P connectors. Pin-compatible with Perkin-Elmer ASYNC products (PALSA, PALS, 2 CH COMM MUX, 8 CH COMM MUX)*

*Contact Macrolink for Optional Cable Configurations

QALTA Status and Command Byte

	0	1	2	3	4	5	6	7	
	OV	PF	FR	0	BUSY	EX	DSRDY OFF/CARR OFF	0	STATUS
RCV	DIS	EN	X	ECHOPLEX	RCT/DTB	TRANS LB	WRT/READ	1	CMD 1
SEND	DIS	EN							
	X	X	BIT SEL		STOP BIT	PARITY		0	CMD 0

macrolink™

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