SUE 1110A, 1111A, and 1112A PROCESSORS

MAINTENANCE BULLETIN M1110A/11A/12A

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PREFACE

This maintenance bulletin is written primarily for system user and service personnel with backgrounds in digital systems. Refer to Reference Bulletin R1110A/11A/12A for related general information, and to General System Bulletin G3 for a description of the SUE Processor Instruction Sets.

For a description of the microcodes, refer to the micro-assembly list and flow charts for the respective processors as follows:

SUE 1110 Revision C, 8-27-73
SUE 1111 Revision C, 8-24-73
SUE 1112 Revision C, 9-10-73

SUE 1110A/1111A/1112A PROCESSORS
MAINTENANCE BULLETIN

INTRODUCTION

This bulletin contains detailed information about the SUE 1110A, 1111A, and 1112A Processors. SUE 1110A is the general purpose processor, SUE 1111A is the decimal arithmetic processor designed for business applications, and SUE 1112A is the scientific double-precision processor. The three processors are logically identical except for their microprograms stored in Read Only Memories (ROMs), and each can operate both as a central processor unit (CPU) in single and multi-processor systems, and as a secondary processor in multi-processor systems.

The processors are designed to be independent of other system modules and to minimize use of the INFIBUS. They contain their own buses for inter-register transfers, and each operates on data received from either a system memory module or directly from an input-output controller. All three processors perform the basic instruction set used for general purpose applications, and their respective extended instruction sets. The instructions are described in General System Bulletin G3.

All SUE processors perform their respective instructions under control of a microprogram using 36-bit control words. On SUE 1110A the microprogram is stored in nine, 1024-bit ROMs organized in 256 by 4-bit words. These ROMs are addressed in straight 8-bit binary using full on-chip decoding. On SUE 1111A and 1112A, the microprogram is stored in nine 2048-bit ROMs organized in 512 by 4-bit words to accommodate the larger instruction sets of these processors. The 2048-bit ROMs are addressed in straight 9-bit binary with full on-chip decoding.

In addition to the nine ROM control storage microcircuits, each processor contains two 1024-bit ROMs organized in 256, 8-bit control words that form a look-up table. These ROMs are enabled and addressed by the current word from microprogram storage.

DESCRIPTION

Each SUE processor is contained on two, multi-layer printed circuit cards measuring 6-1/4 by 13-1/2 inches. The circuit card containing the arithmetic-logic unit is the CPA. The other card containing the ROM microcircuits and control logic is the CPB. Both cards plug into adjacent slots on the INFIBUS and are interconnected on their back edge by an interconnect module containing either two or three connectors depending on the processor function in the system. The first processor installed in any SUE system is interconnected with the bus controller and assumes central processor functions. Therefore, the interconnect module for the CPU is an ICM containing three connectors. Any secondary processor in the system is interconnected by an IDM module containing two connectors. Neither the ICM nor the IDM circuit cards contain discrete or logical circuit components. They provide only pin-to-pin wiring connections between the circuit cards.

Central processors (interconnected by an ICM) in SUE systems are denoted by a -1 suffix such as 1110A-1. Secondary processors (interconnected by an IDM) are denoted by a -2 suffix such as 1110A-2.

INSTALLATION CONSIDERATIONS

The central processor module is plugged into the INFIBUS immediately to the left of the bus controller (BCU), viewing the chassis from the module insertion end. The CPB must be inserted in the next adjacent slot left of the bus controller, and the CPA must be inserted in the next slot left of the CPB. An ICM circuit card is then plugged into the CPA, CPB and BCU circuit cards to interconnect their back edge connectors (J1).

Secondary processors in multiprocessor systems must be installed in any two adjacent slots left of the CPU, the CPA inserted left of the CPB. An IDM circuit card is then plugged into the CPA and CPB to interconnect their back edge connectors (J1). Location of secondary processors in the chassis is a matter of judgment. Modules closest to the BCU have highest precedence for bus access.

All edge connectors on SUE circuit cards are keyed to avoid improper insertion between the INFIBUS and an interconnect circuit card; but the interconnect circuit cards are not keyed to avoid improper relative locations of CPA and CPB. Refer to CPA and CPB designations etched on the circuit cards when installing processor modules.

PROCESSOR ADDRESS JUMPERS

Jumper connections at J2 and J3 (see Logic Diagram LD2001002161, Sheet 8) are provided on the CPA to encode the address assigned to the processor for addressing by another system module. Four processors can be addressed in a system: binary 00, 01, 10, and 11. An installed jumper encodes binary 0; no jumper a binary 1. In SUE standard practice, the CPU is forced to address 00 by signals CPU0, CPU1 from the BCU through the interconnect module. If the BCU is not connected to the CPU, (i.e. because of an extender card during maintenance) then the CPU address comes only from the jumpers. In that case, and for all secondary processors, both jumpers J2-1, -2 and J3-1, -2 must be connected on the CPA to encode the processor address. Table 1 lists the addresses and corresponding jumpers.

Table 1. Processor Address Jumpers

Processor		Jumpers Installed	
Number	Binary Address	J3-1 to J3-2 (Lower)	J2-1 to J2-2 (Upper)
1 (CPU)	0 0	Yes	Yes
2	0 1	Yes	No
3	1 0	No	Yes
4	1 1	No	No

ROM ADDRESS JUMPERS

On SUE 1111A and 1112A processors, the S register is extended to 12 bits by a third 4-bit synchronous counter component, and address jumpers are installed on the CPB at terminals J2-A1 to J2-A2 and J2-B1 to J2-B2 to extend the most significant ROM address bits as needed to address the larger ROMs. (See Logic Diagram LD2001002169-1 Sheet 2.) The ROM address jumpers are installed on the CPB as indicated in Table 2.

Table 2. ROM Address Jumpers

Processor Model	CPB Jumpers Installed	
	J2-A1 to J2-A2	J2-B1 to J2-B2
1110A	Yes	Yes
1111A	Yes	No
1112A	Yes	No

SINGLE-STEP JUMPER

A jumper is provided on the CPB that allows single-step sequencing through the microcode from the control panel for processor maintenance tests. Jumper J3-1 connected to J3-2 disables the gate that normally enables the run clock, and allows single-step operation only.

LOGIC ORGANIZATION

Figure 1 is a functional block diagram of the processor logic that shows the general data flow within the processor. The blocks in Figure 1 are keyed to the CPA and CPB logic diagrams by the alpha-numeric designations in the upper left-hand corner of each block. The numeric denotes the sheet number on which the related CPA or CPB logic diagram is located.

SUE processors are organized around the arithmetic logic unit (ALU) and ROM microcode control. The Address (A), Transmit (T), and Receive (R) registers are interfaced with the INFIBUS and data from these registers are selectable for

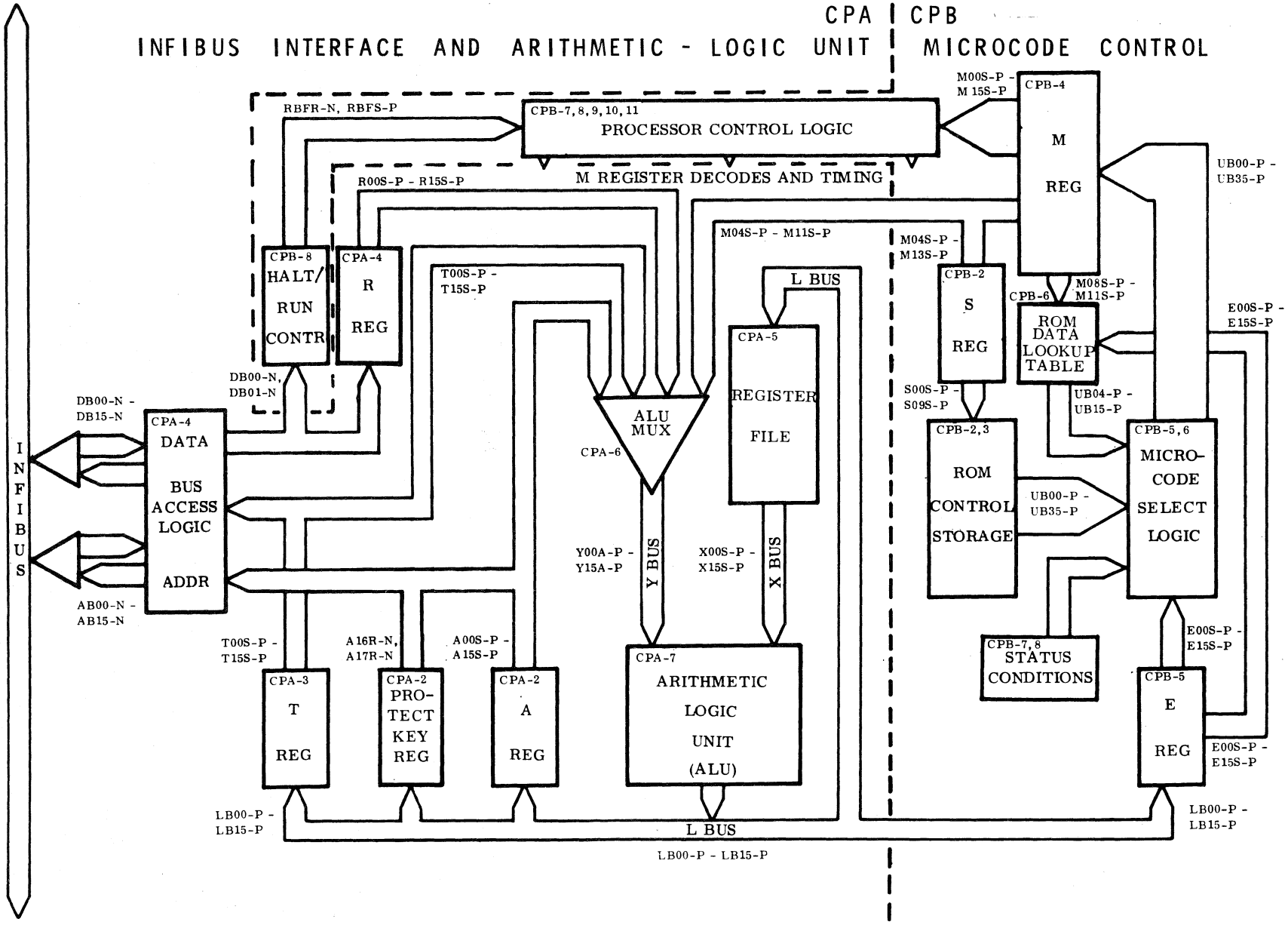


Figure 1. SUE 1110A, 1111A and 1112A Functional Block Diagram

input to the ALU, depending on the decode of the current microcontrol word in the M register. The current word in the M register is decoded to supply control and timing functions throughout the processor.

INFIBUS INTERFACE AND ARITHMETIC LOGIC UNIT (CPA)

The ALU can process two 16-bit operands in parallel received through the X and Y buses. The ALU, ALU multiplexer, and register file all respond to commands from the current microcode word from the M register. The multiplexer responds to the two bit microcode Y field and selects a 16-bit operand from the A, T, or R registers; or a masked literal from the microcode L1-L2 fields for input to the ALU. The other sixteen bit operand is received from one of twelve registers in the register file.

The ALU responds to the A and T fields of the microcode word which specifies one of 16 logical or one of 16 arithmetic functions to be performed. The ALU performs the functions on the two ALU inputs, and on an arithmetic carry-in that adds to the least significant bit position. Output of the ALU is 16 bits that represent the microstep results. The results may be written into the A, T, or E register and/or one of the file registers through the L bus.

The register file consists of twelve 4-by-4 flip-flop arrays that make up twelve 16-bit registers. Decodes of the four-bit microcode X field select one of the twelve registers to read input from the L bus or to write output to the ALU through the X bus. If the X field selects a nonexistent file as input (i.e. bits 15 to 12), then a word containing all ONEs is read out. The twelve registers in the file include the program counter (register R0), seven general registers (R1 through R7), status register (R8), instruction register (R9), and two registers, firmware A and firmware B, that are used to store temporary results. Of the twelve registers, R0 through R9 are accessible to the programmer but access to firmware A and firmware B is not included in the normal instruction repertoire.

Most of the processor interface logic to the INFIBUS is contained on the CPA, but some bus control signals are received by the CPB. Registers A, T, and R are interfaced with the INFIBUS. The A register holds the address that is placed on the INFIBUS to address another system module; the T register holds the data to be transmitted; and the R register receives data from the INFIBUS. All three registers are gated to the ALU for logical or arithmetic combinations with the selected file register.

The interface logic also contains address recognition logic to recognize when the processor is being addressed by another system module to transfer data. The processor responds by receiving or transmitting the contents of the control register if specifically addressed or any other selected file register when the microprogram has properly halted.

Bits A16R-N and A17R-N of the A register are held in two flip-flops that make up the Protect Key register. These bits are available for use in systems equipped with memory protect or bank select/extended memory features.

MICROCODE CONTROL (CPB)

The microcode control logic consists of three registers, Sequence (S), Microcode (M), and Emulation (E); the ROM control storage and microcode select logic; ROM data lookup table; status logic; processor control logic; and halt/run flip-flops. Register S is a twelve bit counter (only eight or nine bits are used) that addresses the ROM control storage and is automatically incremented by a clock pulse to sequence the microprogram. The M register receives the 36-bit microcode control word that specifies both the action of the current microstep and modifications of the next sequential step. M register outputs are decoded into enabling terms and distributed with clock pulses throughout the processor by the processor control logic.

The E register holds sixteen bits which may be tested or used to modify the microcode. E register fields correspond to the macro-instruction word being emulated

and specify instruction code, addressing mode, general register, index register, or a shift count. Bits E3 thru E0 also can operate as a loop counter.

The ROM data lookup table contains 256 eight-bit words. When enabled and addressed by the current microcontrol word in the M register, and a four-bit field from the E register, the table output is ANDed with the literal fields of the next control word from ROM control storage. Other status conditions, when enabled by the current control word, also can be ANDed into the literal fields of the next control word. The microcode select logic forms the AND of the ROM control storage and the other enabled functions and places the control word into the M register. Because of an inherent look-ahead feature in the processor, the next control word is being read while the current word is being executed.

The control register consists of two flip-flops: halt and run. Halt buffers a request to halt that is used by the microcode to enter a halt routine. Run flip-flop controls the clock and may be turned off by the microcode or turned on by writing into the run flip-flop from the INFIBUS. The reset side of the run flip-flop, instead of the set side, asserts the clock enable.

MICROCODE WORD FORMAT

The microcode word format is shown in Figure 2. Fields in the word are related to the organization and functions of the processors. Conditional test and skip or jump microsteps are provided to minimize the length of the microprograms.

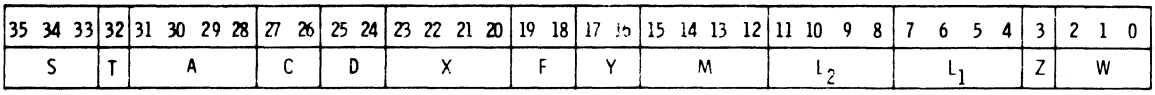


Figure 2. Microcode Word Format

S FIELD, BITS 35 THRU 33: MICROCODE TYPE

Specifies type of microcommand. The type may be a normal sequential step, special command, branch, memory synchronize, or conditional jump command. Values of S cause special interpretation of the D, M and L fields:

S = 0, Sequential step
S = 1, Sequential step and enable special commands
S = 2, Branch
S = 3, Wait for bus access to complete
S = 4, Jump if condition false
S = 5, Jump if condition true
S = 6, Jump if selected bit of T Register is false
S = 7, Jump if selected bit of T Register is true

T FIELD, BIT 32: LOGICAL OR ARITHMETIC FUNCTION
A FIELD, BITS 31 THRU 28: ALU CODE

The four bits of A select one of sixteen logical functions if T = ZERO, or one of sixteen arithmetic functions if T = ONE, to be performed by the ALU as indicated in Tables 3 and 4.

Table 3. ALU Logical Codes, T = 0

A Field Hexidecimal	Logical Function	Description	Symbolic
0	Complement X	Output a 1 for every 0 in X	$\overline{X}$
1	Nor	Output a 1 for every 0 in X and Y	$\overline{X \text{ or } Y}$
2	Mask Y	Output a 1 for every 0 in X and 1 in Y	$\overline{X}$ and Y
3	Clear	Output all ZEROs	0
4	NAND	Output a 1 for every 0 in X or Y	$\overline{X \text{ and } Y}$
5	Complement Y	Output a 1 for every 0 in Y	$\overline{Y}$
6	Exclusive OR	Output a 1 for every bit of X and Y that differ	X $\oplus$ Y
7	Mask X	Output a 1 for every 1 in X and 0 in Y	X and $\overline{Y}$
8	Insert in Y	Output a 1 for every 0 in X or 1 in Y	$\overline{X}$ or Y
9	Equal	Output a 1 for every bit of X and Y that are alike	$\overline{XY}$ or XY
A	Transfer Y	Output a 1 for every 1 in Y	Y
B	AND	Output a 1 for every 1 in X and Y	X and Y
C	ONEs	Output all ONEs	1
D	Insert in X	Output a 1 for every 1 in X or 0 in Y	X or $\overline{Y}$
E	Inclusive OR	Output a 1 for every 1 in X or 1 in Y	X or Y
F	Transfer X	Output a 1 for every 1 in X	X

Table 4. ALU Arithmetic Codes, T = 1

A Field Hexadecimal	Arithmetic Function	Description	Symbolic
0	Increment X	X plus Carry	X+CYIN
1		X or Y plus Carry	X∨Y+CYIN
2		X or Y Not plus Carry Not	$X \vee \overline{Y} + \overline{CYIN}$
3	Carry Skip Test	All ONEs plus Carry	-1+CYIN
4		X plus X and Y Not plus Carry	$X+X \cdot \overline{Y}+CYIN$
5		X or Y plus X and Y plus Carry	X∨Y+X·Y+CYIN
6	Subtract	Subtract Y from X (with or without Carry)	X+Y+CYIN
7		X and Y Not minus 1 plus Carry	$X \cdot \overline{Y}-1+CYIN$
8	Masked Add	X plus X AND Y plus Carry	X+X·Y+CYIN
9	Add	X plus Y plus Carry	X+Y+CYIN
A	Conditionally complement Y by X	Complement Y if X=0 and CYIN = 1 Transfer Y if X=-1 and CYIN = 1	$X \vee \overline{Y}+X \cdot Y+CYIN$
B		X and Y minus 1 plus Carry	X·Y-1+CYIN
C	Shift X left	X plus X plus Carry	X+X+CYIN
D		X or Y plus X plus Carry	X+X∨Y+CYIN
E		X or Y Not plus X plus Carry	$X+X \vee \overline{Y}+CYIN$
F	Decrement X	All ONEs plus X plus Carry	X-1+CYIN

C FIELD, BITS 27 AND 26: CARRY CONTROL

Specifies option of adding or subtracting a Carry-In to the ALU and also controls setting of Carry and Overflow status flip-flops.

If bit T = 0 a logical ALU operation:

C = 0, No change
C = 1, Set Carry Status
C = 2, Clear Carry and Overflow Status
C = 3, Not allowed (results undefined)

If bit T = 1 and an ALU operation with A $\neq$ 2 or 6:

C = 0, No carry in, Carry and Overflow status not changed
C = 1, Carry in, Carry and Overflow status not changed
C = 2, No carry in, Carry and Overflow change enabled
C = 3, Carry in, Carry and Overflow change enabled

If bit T = 1, and an ALU operation with A = 2 or 6:

C = 0, Carry in is a ONE, Carry and Overflow status not changed
C = 1, Carry in is complemented, Carry and Overflow status is not changed
C = 2, Carry in is a ONE, Carry and Overflow status change enabled
C = 3, Carry in is complemented, Carry and Overflow status change enabled

D FIELD, BITS 25 AND 24: DO NEXT ORDER CONTROL

Selects the option of skipping the next micro order either unconditionally or based on the ALU output being all ONEs or the jump condition being met.

If S = 0, 1, 2, or 3 (i.e., bit 35 = 0) :

D = 0, Do next order
D = 1, Do next order if output of ALU is all ONEs
D = 2, Skip next order if output of ALU is all ONEs
D = 3, Skip next order unconditionally

If S = 4, 5, 6, or 7 (i.e., bit 35 = 1):

D = 0, Do next order
D = 1, Do next order if Jump condition is true
D = 2, Skip next order if Jump condition is true
D = 3, Skip next order unconditionally

X FIELD, BITS 23 THRU 20: REGISTER FILE SELECT

Selects one of twelve registers in register file for ALU input and/or to receive output of ALU:

X = 0, Program Counter
X = 1, General Register 1
X = 2, General Register 2
X = 3, General Register 3
X = 4, General Register 4
X = 5, General Register 5
X = 6, General Register 6
X = 7, General Register 7
X = 8, Status Register
X = 9, Instruction Register
X = A, Register A
X = B, Register B
X = C, D, E, F, Literal: FFFF (input only)

F FIELD, BITS 19 AND 18: NEXT ORDER X FIELD SOURCE

Selects source of the address bits for next access to register file. These registers may be selected by the AR and XR fields of the instruction word format, the X field of the microcode, or the least significant bits of an address on the INFIBUS:

F = 0, X field of microcode
F = 1, XR field of instruction ANDed with X field of next micro-order
F = 2, AR field of instruction ANDed with X field of next micro-order
F = 3, Address bits 4 to 1 ANDed with X field of next micro-order

Y FIELD, BITS 17 AND 16: Y INPUT TO ALU SELECT

Selects the R, A or T Registers for input to the ALU. When Y = 3, operates with the M field to enable or disable the transfer of the two microcode literal fields L2 and L1 to the four 4-bit fields of Y:

Y = 0, R register
Y = 1, A register
Y = 2, T register
Y = 3, L Field Control (see M Field)

M FIELD, BITS 15 THRU 12: MULTI FUNCTION

This field operates with other fields for different functions. When Y = 3, it controls mapping of literals L2 and L1 fields to the ALU's Y input. See table 5. When S = 1 and L2 = 7, it specifies the type of shift to perform. When S = 2, it is part of the branch address. When S = 4 or 5, it specifies conditional jump codes. See table 6. When S = 6 or 7, it specifies a bit position in the T register to be tested.

Table 5. Literal Field Input to ALU, Y = 3

M Field (Hexadecimal)	L2 Enabled	L1 Enabled	L2 Enabled	L1 Enabled
	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
M = 0	Yes	Yes	Yes	Yes
M = 1	Yes	Yes	Yes	No
M = 2	Yes	Yes	No	Yes
M = 3	Yes	Yes	No	No
M = 4	Yes	No	Yes	Yes
M = 5	Yes	No	Yes	No
M = 6	Yes	No	No	Yes
M = 7	Yes	No	No	No
M = 8	No	Yes	Yes	Yes
M = 9	No	Yes	Yes	No
M = A	No	Yes	No	Yes
M = B	No	Yes	No	No
M = C	No	No	Yes	Yes
M = D	No	No	Yes	No
M = E	No	No	No	Yes
M = F	No	No	No	No
NOTE: Bits not enabled are ZERO				

S = 1, L2 = 7, Shift Code:

M = 0, 8 Left arithmetic
M = 1, 9 Left logical, linked
M = 2, A Left logical, open
M = 3, B Left logical, closed
M = 4, C Right Arithmetic
M = 5, D Right logical, linked
M = 6, E Right logical, open
M = 7, F Right logical, closed

S = 2: Bits 13 and 12 of the M field are used with L2 and L1 to specify up to a 10-bit branch address.

Table 6. Conditional Jump Codes, S = 4 or 5

M Field, (Hexadecimal)	Conditional Jump Codes	Symbolic
M = 0	Halt flip-flop set	HBFS
M = 1	Interrupt condition false	NEXT
M = 2	Bit 00 of R Register	R00S
M = 3	Class 0, 4, 8, or 12	$\overline{\text{E13S}}$ $\overline{\text{E12S}}$
M = 4	All ONEs flip-flop set	ONES
M = 5	Carry flip-flop set	CRYS
M = 6	Overflow flip-flop set	OVFS
M = 7	Abort flip-flop set	BAES
M = 8	Loop count complete	EMAX
M = 9	Extended Address	E03S
M = A	Indirect Address	E07S
M = B	Byte mode	E11S
M = C	Class 4 to 7, or 12 to 15	E14S
M = D	Not used	-
M = E	Indirect Address	E07S
M = F	Not used	-

S = 6 or 7: M field specifies the bit position ($0\text{-}F_{16}$) of the T Register to be tested.

L2 FIELD, BITS 11 THRU 8: LITERAL FIELD 2

When Y = 3, it is a four-bit literal that is gated to the ALU Y input. See table 4. When S = 1, it is a special command. For S = 2 through 7, L2 represents the most significant bits of the control storage branch or jump addresses. For Z = 1 and L1 = 0, 4, 8, or 12, L2 represents the four most significant bits of the jump table address.

S = 1, Special Command:

L2 = 0, Not used
L2 = 1, Clear RBFS
L2 = 2, Load P key
L2 = 3, Select interrupt
L2 = 4, Enable next order C, V
L2 = 5, Enable next order N, Z, O
L2 = 6, Set HBFS
L2 = 7, Shift (shift type specified by M field)
L2 = 8, Reset abort
L2 = 9, Read word
L2 = A, Write word
L2 = B, Not used
L2 = C, Not used
L2 = D, Read with byte allow
L2 = E, Write with byte allow
L2 = F, Not used

S = 2: L2 represents bits 7, 6, 5 and 4 of the 10-bit branch address. Bits 9 and 8 are contained in the M field. Bits 3 thru 0 are contained in L1.

S = 3, 4, 5, 6, 7: L2 represents bits 7, 6, 5 and 4 of the 8-bit jump address. Bits 3 thru 0 are contained in L1.

L1 FIELD, BITS 7 THRU 4: LITERAL FIELD 1

When Y = 3, it is a four-bit literal that is gated to the ALU Y input. For S = 2 thru 7, it represents the four least significant bits of branch or jump addresses. When Z = 1, L1 field specifies the source to be used to modify the L (or M) fields of the next micro instruction, or it specifies which E register field is to be used as the least significant four bits of the data lookup table address (used to modify the next micro-instruction L field).

Z FIELD, BIT 3: LITERAL ENABLE

When Z = 1 this field is used to enable special interpretation of L2 and L1 fields to select a four-bit field from the E register, or other sources, for generation of special literals on the next micro instruction:

L1, Bits 7 and 6 = 0, Select E03 thru E00

L1, Bits 7 and 6 = 1, Select E07 thru E04

L1, Bits 7 and 6 = 2, Select E11 thru E08

L1, Bits 7 and 6 = 3, Select E15 thru E12

L1, Bits 5 and 4 = 0, Table output to L field (bits 11 to 04)
(table address is L2 with selected E field)

L1, Bits 5 and 4 = 1, Interrupt level to L field bits 8 and 7

L1, Bits 5 and 4 = 2, CPU number to L field bits 10, 9

L1, Bits 5 and 4 = 3, Output bits of E (selected by L1 bits 7 and 6)
to M field, (bits 15 thru 12)

W FIELD, BITS 2 THRU 0: WRITE ALU OUTPUT

Selects register file specified in X field and/or one of A, T, or E registers or loop counter to receive the ALU output. For W = 5, 6, or 7, both the register file and A, T, or E register are selected to receive ALU output, respectively. For W = 0 or 4, the ALU1 signal is copied into the ONEs flip-flop:

W = 0, None
W = 1, A register
W = 2, T register
W = 3, Loop Counter
W = 4, Register file, selected by X
W = 5, Register file selected by X and the A register
W = 6, Register file selected by X and the T register
W = 7, E register and file selected by X

INTERCONNECT MODULE PIN ASSIGNMENTS

Pin assignments for interconnect modules ICM and IDM are listed in Table 7.

Table 7. CPA-CPB Interconnect Module Pin Assignments

Pin Number	Source*	J1-Axx	Load*	Source*	J1-Bxx	Load*	Pin Number
01	-	-	-	-	-	-	01
02	CPA-7	ALU1-P	CPB-7	CPB-7	ARCK-P	CPA-2	02
03	CPB-9	STAT-N	BCU-2	BCU-5	DNOL-P	CPB-9	03
04	CPB-7	SCM3-N	BCU-3	BCU-2	NEXT-N	CPB-7	04
05	BCU-6, CPA-8	CPU0-P	CPA-8, CPB-6	BCU-6, CPA-8	CPU1-P	CPA-8, CPB-6	05
06	BCU-3	IL0R-N	CPB-6	BCU-3	IL1R-N	CPB-6	06
07	CPB-4	ONLN-P	CPA-2	CPB-7	RE03-N	CPA-5	07
08	CPB-4	M10S-P	CPA-6	CPB-7	WE03-N	CPA-5	08
09	-	-	-	CPB-10	XSET-N	CPA-5	09
10	-	-	-	CPB-4	M20S-P	CPA-5	10
11	CPB-4	M11S-P	CPA-6	CPB-4	M08S-P	CPA-6	11
12	-	-	-	CPB-7	RE47-N	CPA-5	12
13	-	-	-	CPB-7	WE47-N	CPA-5	13
14	CPA-7	LB11-P	CPB-5	-	-	-	14
15	CPB-7	RE8B-N	CPA-5	-	-	-	15
16	CPB-7	WE8B-N	CPA-5	CPA-7	LB09-P	CPB-5	16
17	-	-	-	-	-	-	17
18	-	-	-	-	-	-	18
19	CPB-4	M21T-P	CPA-5	CPB-4	M09S-P	CPA-6	19
20	CPA-7	LB08-P	CPB-5	CPB-4	M06S-P	CPA-6	20
21	CPA-7	LB10-P	CPB-5	CPA-7	LB07-P	CPB-5	21
22	-	-	-	CPB-4	M04S-P	CPA-6	22
23	-	-	-	CPB-4	M07S-P	CPA-6	23
24	CPA-2	A16R-N	CPB-6	CPB-4	M05S-P	CPA-6	24
25	CPA-2	A17R-N	CPB-6	CPB-4	M20T-P	CPA-5	25
26	-	-	-	CPB-4	M32T-P	CPA-7, 8	26
27	-	-	-	CPB-4	M28T-P	CPA-7	27
28	-	-	-	CPB-4	M29T-P	CPA-7	28
29	-	-	-	CPB-4	M31T-P	CPA-7	29
30	-	-	-	CPB-4	M30T-P	CPA-7	30
31	-	-	-	CPA-7	LB03-P	CPB-5	31
32	CPA-7	LB04-P	CPB-5	CPB-4	M21S-P	CPA-5	32
33	CPA-7	LB05-P	CPB-5	CPB-7	SCM2-N	CPA-2	33
34	CPA-7	LB06-P	CPB-5	CPB-4	M13R-N	CPA-8	34
35	-	-	-	CPB-7	TSHF-P	CPA-8	35
36	CPA-4	R00S-P	CPB-7	CPB-9	WOLN-P	CPA-4	36
37	CPB-4	M16S-P	CPA-6	CPA-7	LB02-P	CPB-5	37
38	CPB-4	M17S-P	CPA-6	CPA-7	LB00-P	CPB-5	38
39	CPB-7	STSR-P	CPA-3, 8	-	-	-	39
40	CPA-8	SARC-P	CPB-9	CPA-7	LB01-P	CPB-5	40
41	CPB-4	M12S-P	CPA-3, 6, 8	CPA-4	T15R-N	CPB-6	41
42	CPB-7	STSL-P	CPA-3, 8	CPB-9	RDCK-P	CPA-4	42
43	CPB-4	M26S-P	CPA-8	-	-	-	43
44	-	-	-	CPA-4	T00R-N	CPB-6	44
45	CPB-4	M27S-P	CPA-8	CPB-4	M14S-P	CPA-3, 6	45
46	CPA-3	BIT1-N	CPB-7	CPB-4	M13S-P	CPA-3	46
47	-	-	-	-	-	-	47
48	CPA-8	STRC-P	CPB-9	-	-	-	48
49	-	-	-	CPB-10	CKTR-N	CPA-3	49
50	CPA-7	LB15-P	BCU-2, CPB-5	CPB-4	M15S-P	CPA-3, 6	50
51	CPA-7	LB13-P	BCU-2, CPB-5	-	-	-	51
52	CPA-7	LB14-P	BCU-2, CPB-5	CPA-8	OVFS-P	CPB-6	52
53	CPA-7	LB12-P	BCU-2, CPB-5	CPA-8	CRYS-P	CPA-3, CPB-6	53
54	CPB-9	DALE-N	CPB-9	CPB-9, 10	CKTS-P	CPA-8	54
55	-	-	-	-	-	-	55

*The digits in the Source and Load columns refer to the logic diagram sheet number for the circuit card indicated. The logic diagrams for the CPA and CPB are contained in this bulletin, and for the BCU in maintenance bulletin M1810.

DRAWINGS AND PARTS LISTS

The drawings and parts lists that follow in this bulletin are listed below. Each of the logic diagrams is accompanied by a brief description that explains the purpose of the logic in the system, and definitions of key logic terms that originate on the corresponding diagram.

Drawings or Parts List	Drawing Number	Sheets
Arithmetic and Logic Unit CPA, Circuit Card Assembly	2001002161	1
Arithmetic and Logic Unit CPA, Logic Diagram	LD2001002161-1	1 thru 8
Control Board CPB, Circuit Card Assembly	2001002169	1
Control Board CPB, Logic Diagram	LD2001002169-1	1 thru 11
Interconnect Module ICM, Circuit Card Assembly	2001002166	1
Interconnect Dual Module IDM, Circuit Card Assembly	2001002232	1
Arithmetic and Logic Unit CPA, Parts List	PL2001002161-1	2,3
Control Board CPB, Parts List		
SUE 1110A-1, 1110A-2	PL2001002169-5	8,9
SUE 1111A-1, 1111A-2	PL2001002169-6	10,11
SUE 1112A-1, 1112A-2	PL2001002169-8	12,13
Parts List Notes	PL2001002169	14
Wire List	PL2001002169	15
Interconnect Module ICM, Parts List	PL2001002166-0,-1	2,3
Interconnect Dual Module IDM, Parts List	PL2001002232-1	2

PROCESSOR TIMING

Processor timing is shown in figures 3 and 4. Figure 3 shows the arithmetic and logic cycle times, figure 4 shows the halt/file access/start sequence. Timing is controlled by a 150-nanosecond tapped delay line as indicated on CPB logic diagram LD2001002169-1, Sheet 10. Refer to sheet 10 and to sheet 8 of the diagram to correlate the signal mnemonics in figures 3 and 4 with the logic.

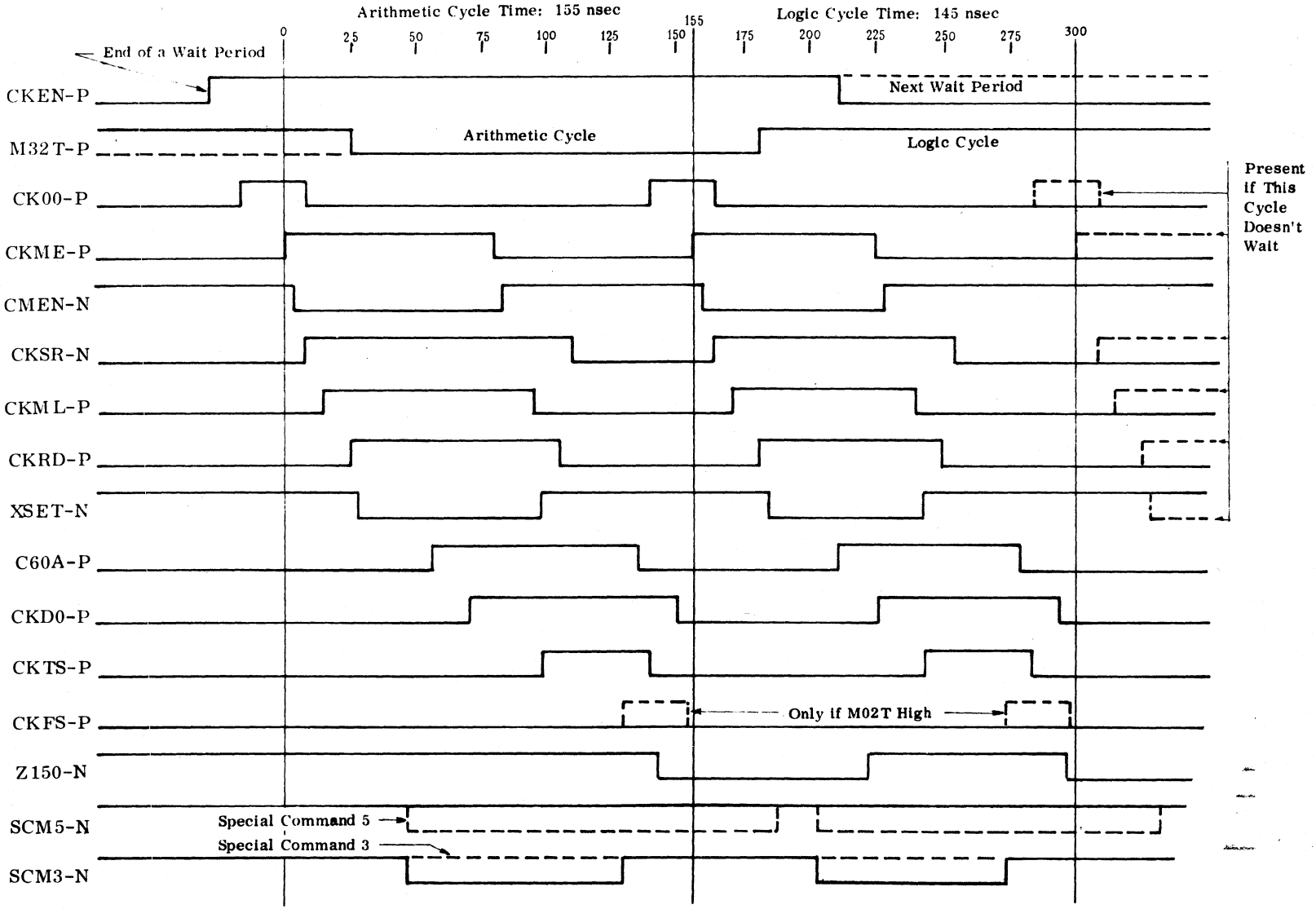


Figure 3. Arithmetic and Logic Cycle Times

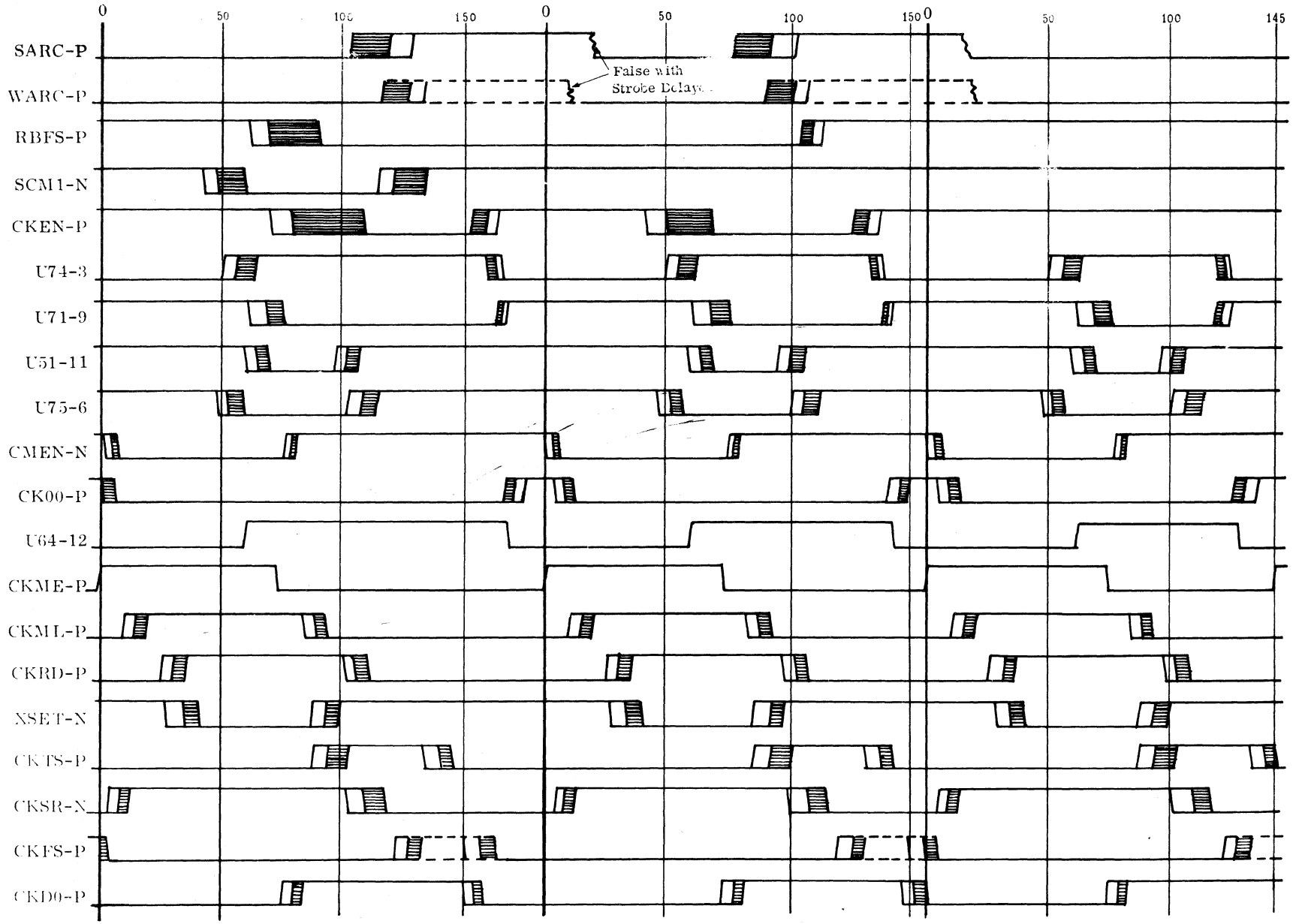
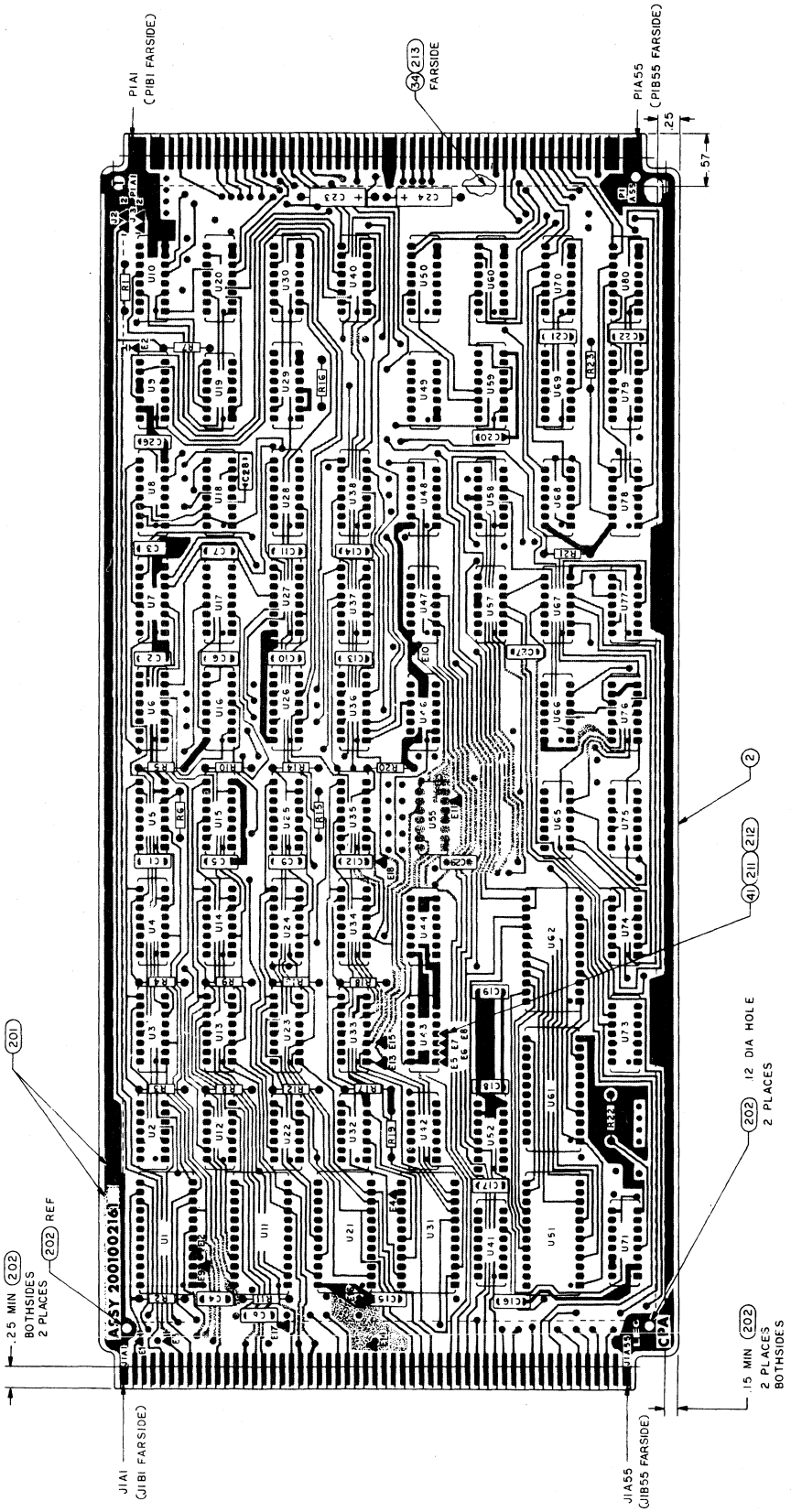


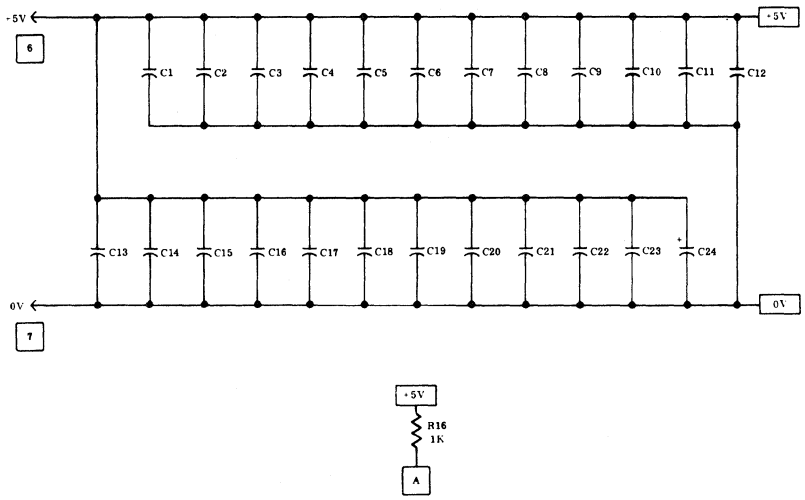
Figure 4. Halt/File Access/Start Sequence Timing



Arithmetic and Logic Unit CPA, Circuit Card Assembly
2001002161, Rev. D, Sheet 1

NOTES:

1. ALL RESISTORS ARE IN OHMS ±2%, 1/4W.
2. ALL NON-POLARIZED CAPACITORS ARE 0.1 μf, +80%, -20%, 50V.
3. ALL POLARIZED CAPACITORS ARE 33 μf, ±20%, 10V.
4. INTEGRATED CIRCUIT PACKAGE TYPE DESIGNATORS ARE ABBREVIATED, FOR COMPLETE PART NUMBER SEE PARTS LIST (REFERENCE LIST ON DRAWING 8001800200).
5. INTEGRATED CIRCUIT PACKAGE POWER PINS ARE: (14 I PIN ICP) PIN 7 0V, PIN 14 +5V; (16 PIN ICP) PIN 8 0V, PIN 16 +5V, EXCEPT BDR AND T153 PIN 7 AND 8 0V, PIN 16 +5V; (24 PIN ICP) PIN 12 0V, PIN 24 +5V.
6. +5V CONNECTOR PINS ARE: P1-A16, A28, A29, A51, B16, B28, B29 AND B51.
7. 0V CONNECTOR PINS ARE: P1-A1, A55, B1 AND B55.



Arithmetic and Logic Unit CPA, Logic Diagram
LD2001002161-1, Rev. C, Sheet 1 of 8

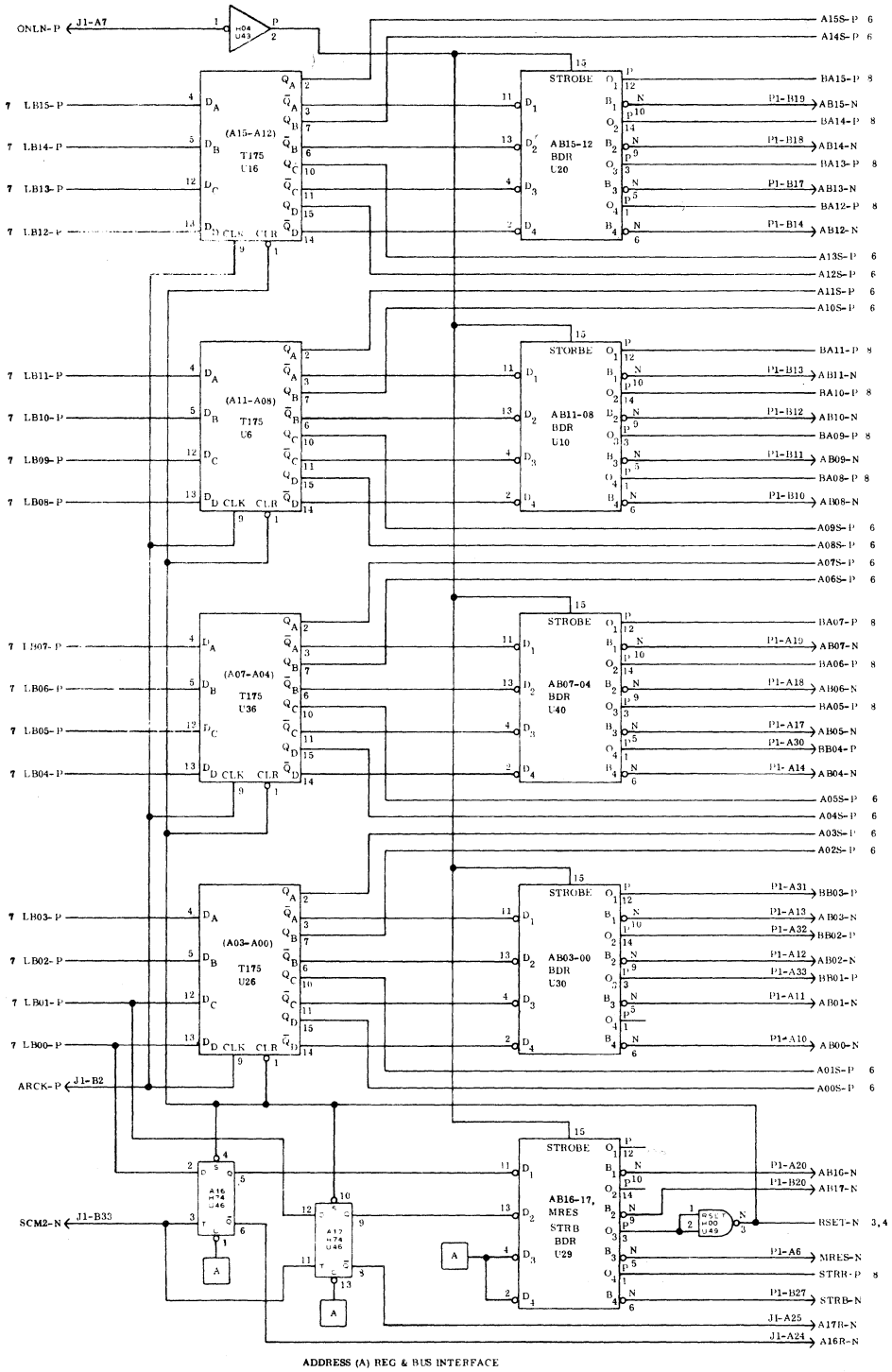
ADDRESS (A) REGISTER AND BUS INTERFACE, CPA (LD2001002161-1, Sheet 2)

The address (A) register serves the following functions:

1. Holds the address sent on the INFIBUS during a memory cycle. The address is gated onto the INFIBUS by ONLN-P which strobes the address bus driver/receivers.
2. Receives outputs from the ALU and provides inputs to the ALU multiplexer. The A register is loaded by ARCK-P.
3. Serves as a working register for the microcode.

KEY SOURCE LOGIC DEFINITIONS

AB00-N thru AB17-N	Negative INFIBUS signals that connect to the address bus drivers/receivers and are used to either send or receive the address.
ARCK-P	Address register clock from CPB, that clocks the address from the ALU into the A register.
A00S-P thru A15S-P	Address register bits sent to the ALU multiplexer inputs.
A16R-N, A17R-N	Protect Key register bits transmitted on INFIBUS lines KEY0 and KEY1, respectively.
BA05-P thru BA15-P	Bus driver/receiver outputs for the 11 high order address bits on the INFIBUS used to recognize when this processor is being addressed by another master device.
BB01-P thru BB04-P	Bus driver/receiver outputs for the four low order bits of a word address used to select the file register (i.e., word) to be accessed when the processor is halted and addressed by another master device such as a control panel.
MRES-N	Master Reset line on the INFIBUS.
ONLN-P	On-Line enabling signal for the address bus drivers that comes from the CPB and is active when the processor is granted the INFIBUS data cycle.
RSET-N	CPA reset signals from master reset on the INFIBUS used to reset all CPA registers except the carry and overflow flip-flops.
SCM2-N	Special Command clock signal to load the Key register flip-flops (A16 and A17) from the two least significant bits of the ALU.
STRB-N	Data cycle strobe on the INFIBUS.
STRR-P	Data cycle strobe received from INFIBUS before the de-skewing delay.



ADDRESS (A) REG & BUS INTERFACE

Arithmetic and Logic Unit CPA, Logic Diagram
LD2001002161-1, Rev. C, Sheet 2 of 8

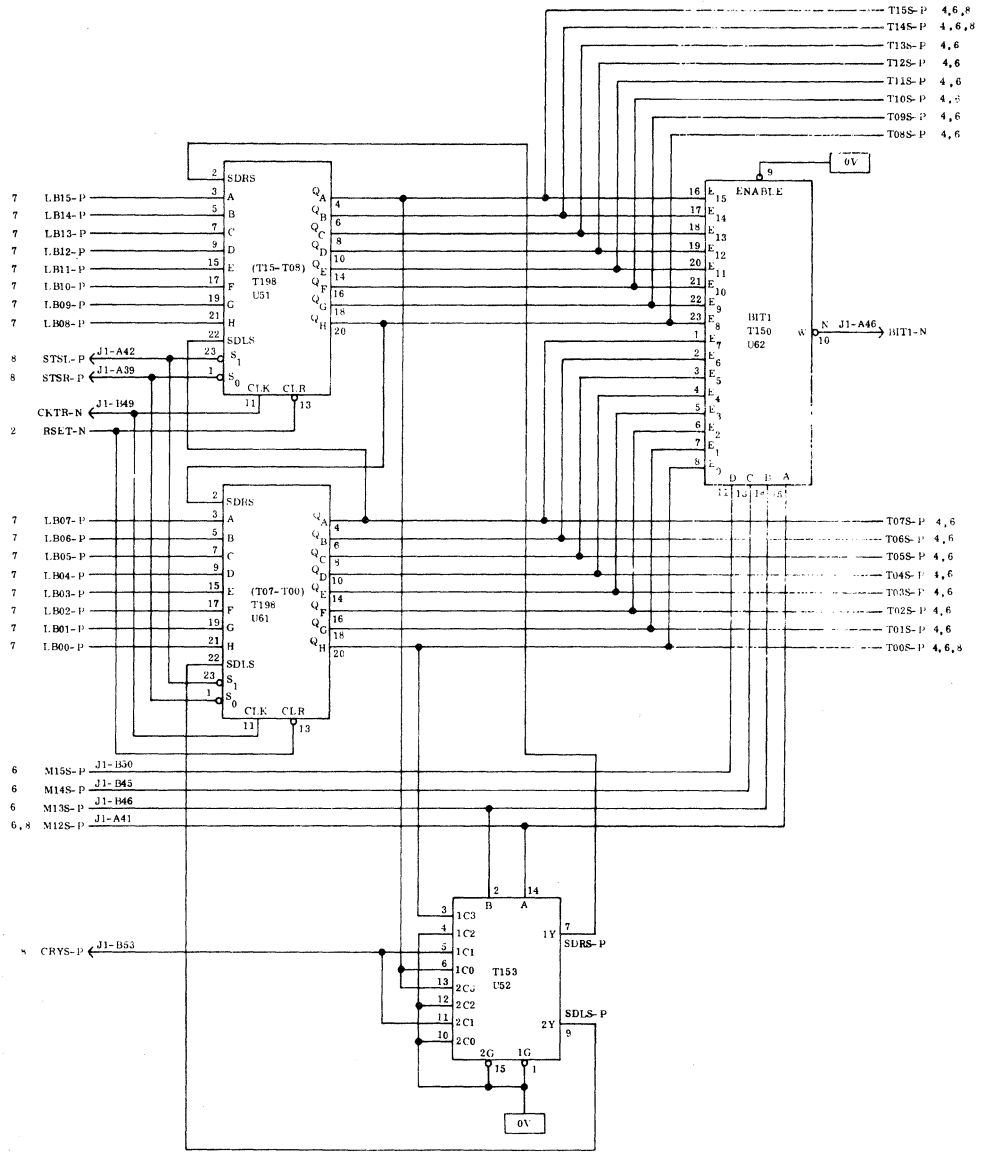
TRANSMIT (T) REGISTER AND BIT TEST, CPA (LD2001002161-1, Sheet 3)

The T-Register holds the data that is sent on the INFIBUS during a memory write cycle. This register may also be selected as an input to the ALU and used for a general working register with shift capability.

The T Register is composed of two coupled 8 bit left/right parallel in/out shift registers (24 pins each). It is clocked by the rising edge of CKTR-N which is free running. Shifting occurs when STSL-P (left) or STSR-P (right) is asserted (low). When neither is asserted, the T-Register outputs remain stable and when both are asserted the ALU outputs (LB00 to LB15) are loaded into the T Register. Shift-in bits are provided at either end by a dual, 4-to-1 multiplexer that selects bit 00, bit 15, the Carry flip-flop or ZERO under control of M12S-P and M13S-P, two of the shift control bits.

KEY SOURCE LOGIC DEFINITIONS

BIT1-N	A bit sampled from the T Register by the 16-to-1 multiplexer. The bit is addressed by M12 through M15 and is used to condition a Jump and Skip in the microcode sequence.
T00S-P thru T15S-P	Transmit Register positive outputs to the ALU 4-Bus Multiplexer and the data inverters feeding the INFIBUS data drivers.
CKTR-N	Clock T Register, a free-running clock to the T Register.
STSL-P, STSR-P	Select T, Shift Left/Right, coded command inputs to designate left shift, right shift, load, or hold.
CRYS-P	Output from the Carry flip-flop used in this logic to allow shifting in the Carry bit.
SDLS-P, SDRS-P	Select Data, Shift Left/Right, the left and right shift inputs to the T Register.
M12S-P thru M15S-P	Control bits from the M Register used as select signals for multiplexers to select the shift-in bits to the T Register or the test output bit for Jump control.



TRANSMIT (T) REG & BIT TEST

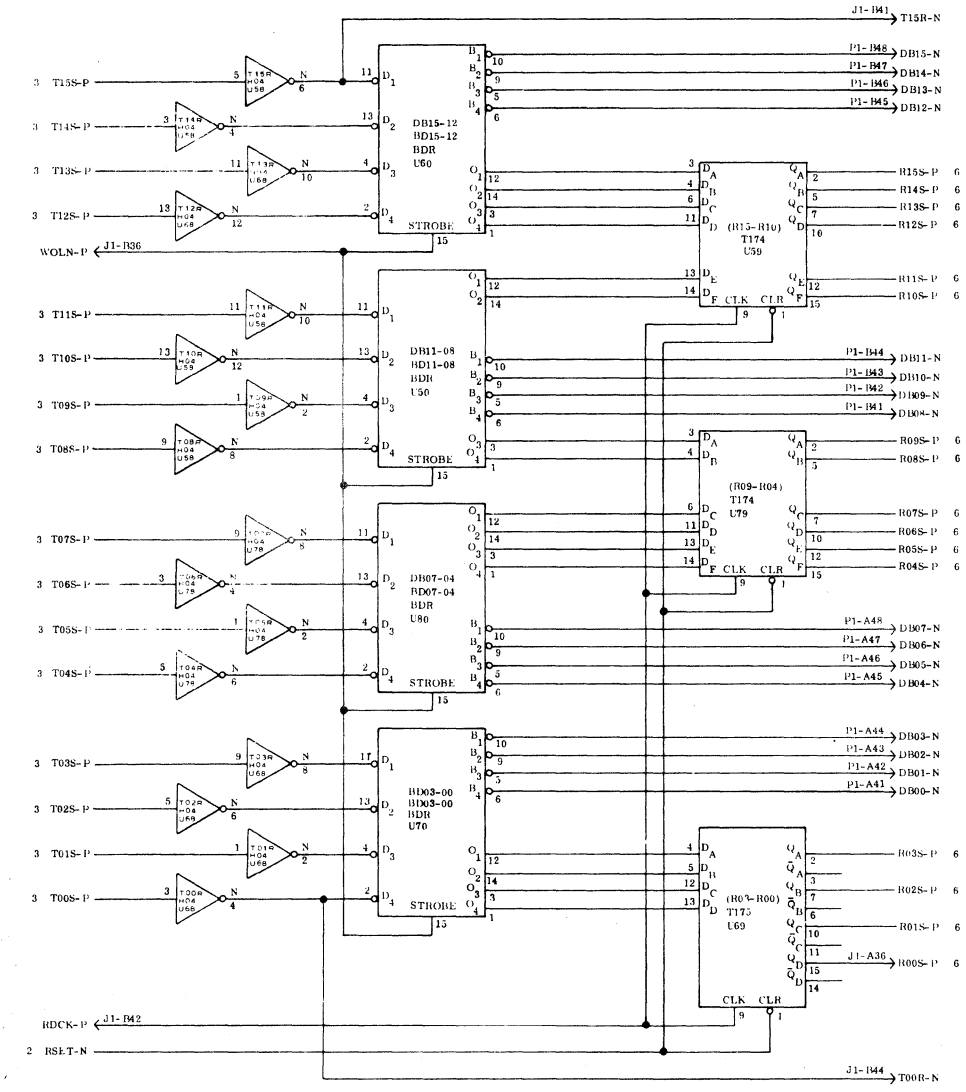
Arithmetic and Logic Unit CPA, Logic Diagram
LD2001002161-1, Rev. C, Sheet 3 of 8

DATA BUS AND RECEIVE (R) REGISTER, CPA (LD2001002161-1, Sheet 4)

The receive (R) register holds data received from the INFIBUS during a memory read cycle and may be selected as an input to the ALU. The R Register positive inputs are from the data bus drivers/receivers which interface negatively to the INFIBUS. The inputs to the bus drivers/receivers are through inverters to the T Register positive outputs.

KEY SOURCE LOGIC DEFINITIONS

DB00-N thru DB15-N	INFIBUS data lines driven and received by their respective bus driver/ receivers.
R00S-P thru R15S-P	R-register outputs to the ALU multiplexer. R00S-P also is an input to the test multiplexer.
RDCK-P	Read Clock, the clock for the R register developed by the interface logic from the read data strobe.
T00R-N, T15R-N	Inverted outputs (least- and most-significant T register bits) that are sent to the CPB to provide status information (i.e. odd and negative) from the T register.
WOLN-P	Write On-Line, the enable signal to the bus driver/receivers that places the T-register data on the INFIBUS data lines during a memory write cycle.
T00S-P thru T15S-P	T register bits that represent the data sent on the INFIBUS during a memory write cycle.



DATA BUS & RECEIVE (R) REG

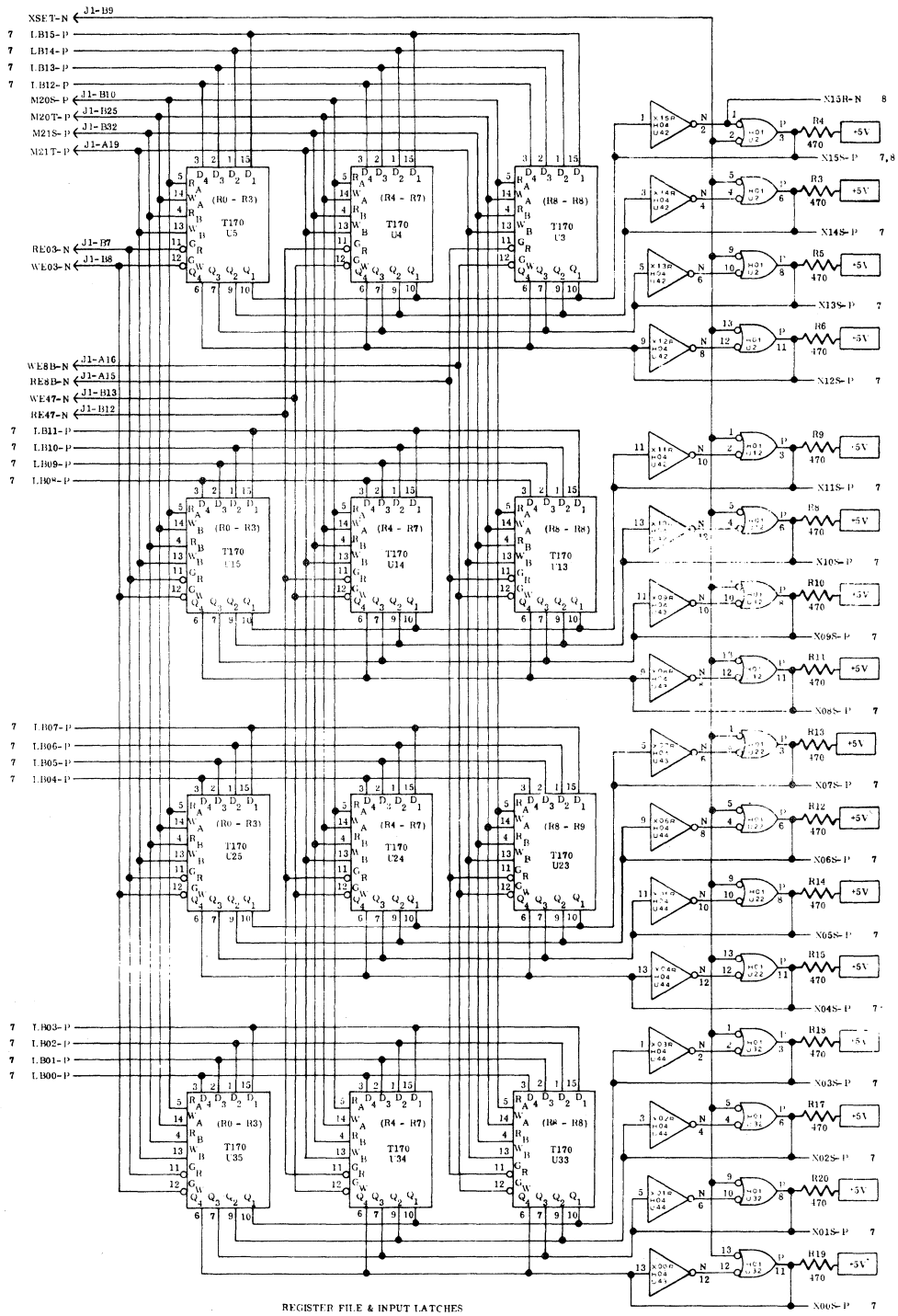
Arithmetic and Logic Unit CPA, Logic Diagram
LD2001002161-1, Rev. C, Sheet 4 of 8

REGISTER FILE AND INPUT LATCHES, CPA (LD2001002161-1, Sheet 5)

The register file comprises three sets of four register file components with each component having a four-bit by four-word capacity. Each set of four components has a sixteen-bit by four-word capacity and together the total file capacity is sixteen bits by twelve words. A word is read from the file by enabling one set of components and addressing one its four words. The outputs of the component sets are open collectors that are AND-connected together and applied to the ALU X inputs. Also, an open-collector latch is connected to each output to maintain the low signals at the X input after the read enable is removed from the register file prior to writing into the same word of the file. The latches, which do not insert a delay into the data paths, are released to go high after the X input is needed no longer.

KEY SOURCE LOGIC DEFINITIONS

M20S-P, M21S-P, M20T-P, M21T-P	M register bits from the X field used to address one of four words in the register file either to be read (M20S-P, M21S-P early) or to be written into (M20T-P, M21T-P late).
RE03-N, RE47-N, RE8B-N	Read enable bits 0 to 3, 4 to 7, and 8 to B decoded from M22 and M23 (X field - early) which enables the read function in one of the three sets of file register components.
WE03-N, WE47-N, WE8B-N	Write enable bits 0 to 3, 4 to 7, and 8 to B decoded from M22 and M23 (X field - late) which enables the write function in one of the three sets of file register components.
XSET-N	The latch control term to either allow the latched (low) signal to unlatch (X SET low) or to keep them latched (X SET high).
X00S-P thru X15S-P, and X15R-N	The X inputs to the ALU composed of the common AND connection of the open collector outputs of the files and latches. X15R-N is the inversion of the sign bit X15S-P. Both of these signals are used to control the overflow logic.



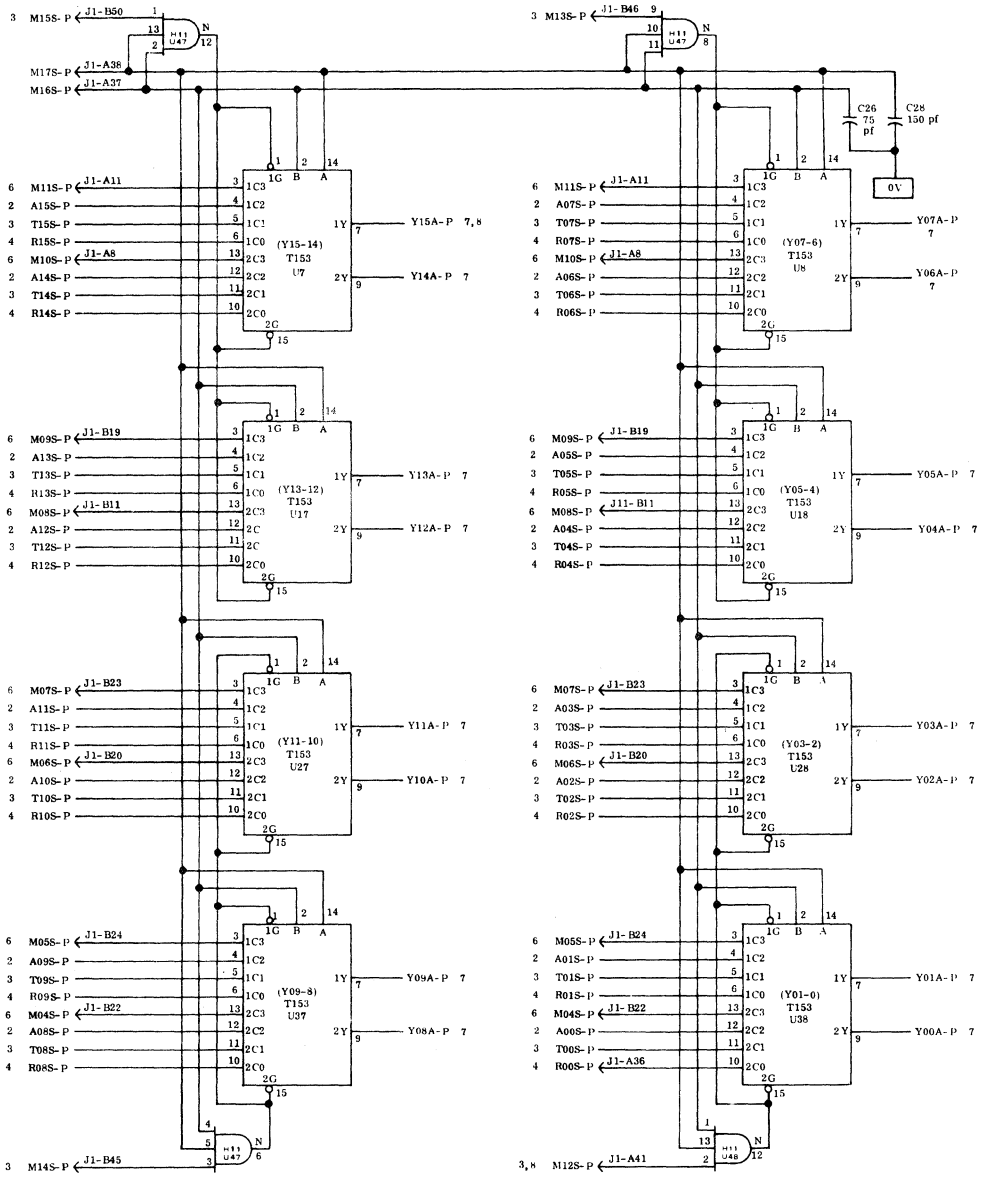
Arithmetic and Logic Unit CPA, Logic Diagram
LD2001002161-1, Rev. C, Sheet 5 of 8

ALU INPUT MULTIPLEXER, CPA (LD2001002161-1, Sheet 6)

The Y inputs to the ALU are taken from eight, dual 4-to-1 multiplexers. The multiplexers, under control of bits 16 and 17 in the M Register, select either one of registers R, A, T, or a zoned literal value from M register field L1 and L2 (bits 4 to 7 and 8 to 11, respectively). Each multiplexer output is enabled in four-bit zones by four AND gates so that all outputs are enabled if any one of registers R, A, or T is selected. However, if the literal fields are selected, the enabling is under control of M field, bits M12 to M15. Outputs of multiplexers not enabled are zero.

KEY SOURCE LOGIC DEFINITIONS

M16S-P, M17S-P	Y field of the M Register that selects the multiplexer input and enables the multiplexer if the literal is not being selected (by forcing the AND enable gate output low).
M12S-P thru M15S-P	M field of the M Register that controls enabling of the multiplexers when the literal value is being selected. For a multiplexer to be not enabled, the literal value must be selected and the corresponding mask bit must be high.
M04S-P thru M11S-P	L1 and L2 fields of the M register used here as an 8-bit literal value for a multiplexer input. The 8 bits are sent to both the most- and least-significant inputs to be enabled under zone control.
R00S-P thru R15S-P, T00S-P thru T15S-P, A00S-P thru A15S-P	The Positive outputs of each of the three working registers R, T, and A used as data to the other three multiplexer inputs.
Y00A-P thru Y15A-P	The positive multiplexer outputs going to the ALU Y inputs. Y15A-P is also used by the overflow detection logic.



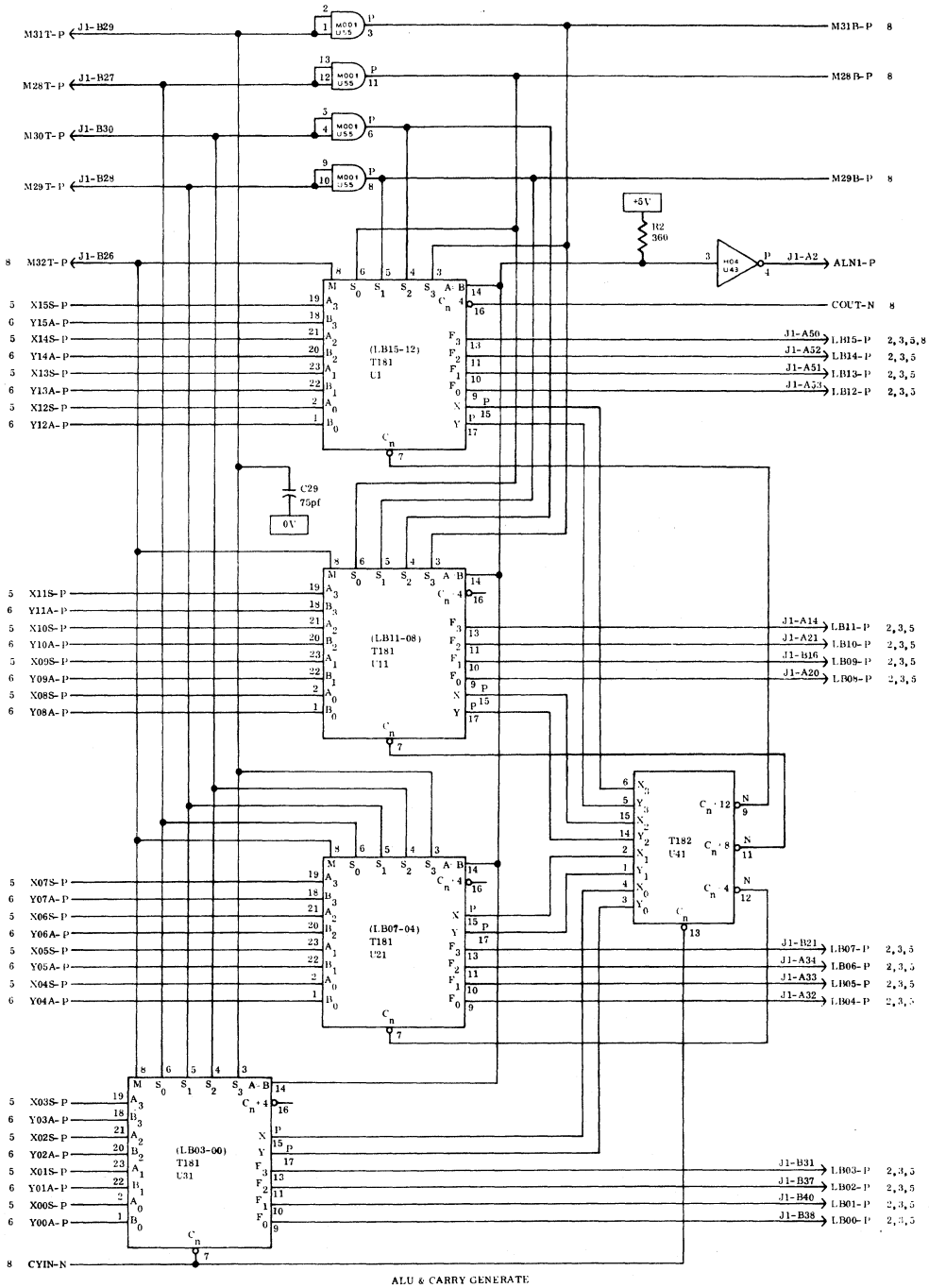
Arithmetic and Logic Unit CPA, Logic Diagram
LD2001002161-1, Rev. C, Sheet 6 of 8

ALU AND CARRY GENERATE, CPA (LD2001002161-1, Sheet 7)

The ALU is the function generator for the processor combining two 16-bit inputs, X and Y, and producing a 16-bit result. Sixteen logical and 16 arithmetic (i.e. involving carry logic) combinations can be made. The type of combination is selected by 5 control inputs. A carry input is accepted and a carry output generated with carry preparation being enhanced by U41, a look-ahead carry generator. An output that indicates when the ALU outputs are all high is used to detect zero and equality under certain algorithms.

KEY SOURCE LOGIC DEFINITIONS

M32T-P	The control input that determines the operation mode: high for logical and low for arithmetic.
M28T-P thru M31T-P, M28B-P thru M31B-P	The control inputs that select the function being generated. The repeaters (MxxB-P) are added to distribute the signal loading and also to drive carry selection, carry store, and overflow detection logic.
CYIN-N	Negative carry input to both the least-significant bit and the carry look-ahead logic.
X00S-P thru X15S-P Y00S-P thru Y15S-P	The ALU function inputs from the register file (X) and the A, T, or R register and literal multiplexer (Y). Y multiplexer for the A, T, or R registers or literal.
LB00-P thru LB15-P	The ALU outputs which constitute a logic bus to distribute the ALU results to the file register and/or one of registers A, T, or E (via the back connector). LB12-P thru LB15-P is also picked up by the BCU from the back connector to store the interrupt enable bits whenever file register 8 (status) is written into. LB15-P also is used by the overflow detection logic.
COUT-N	The negative carry output used to store carry results and to detect overflow.
ALU1-P	The cumulative signal generated by the open collector outputs of all the ALU chips indicating when all the ALU outputs are ONEs (high). It is used by the CPB to control skips and jumps and provide status information.



Arithmetic and Logic Unit CPA, Logic Diagram
LD2001002161-1, Rev. C, Sheet 7 of 8

CARRY AND OVERFLOW, CPA (LD2001002161-1, Sheet 8)

The carry and overflow logic may be affected by arithmetic, logic, or shift operations. Set or reset conditions are combinations of shift control and ALU arithmetic or logic controls. Both operations can occur simultaneously. Also, the same timing signal (CKTS-P) is used on the DC inputs and the clock input, with clocking on the trailing edge.

The following are normal modes of control:

1. LOGIC MODE — M26 sets carry.
2. LOGIC MODE — M27 resets carry and overflow.
3. ARITHMETIC MODE — M27 enables carry load and overflow detection.
4. SHIFT MODE — Either arithmetic or linked shift enables carry load; also, left shift enables overflow detection. Overflow can occur on logical left linked shift. (ALU code 'OF', logical pass X, supresses arithmetic overflow logic.)

SLAVE ADDRESS RECOGNITION, CPA (LD2001002168-1, Sheet 8)

The address lines are monitored to recognize when the processor address space is accessed. The J2 and J3 links are conditionally grounded to detect the number (0, 1, 2, or 3) to which this processor responds. These links are grounded also by the BCU so that the processor which is the CPU, is always addressed as processor ZERO.

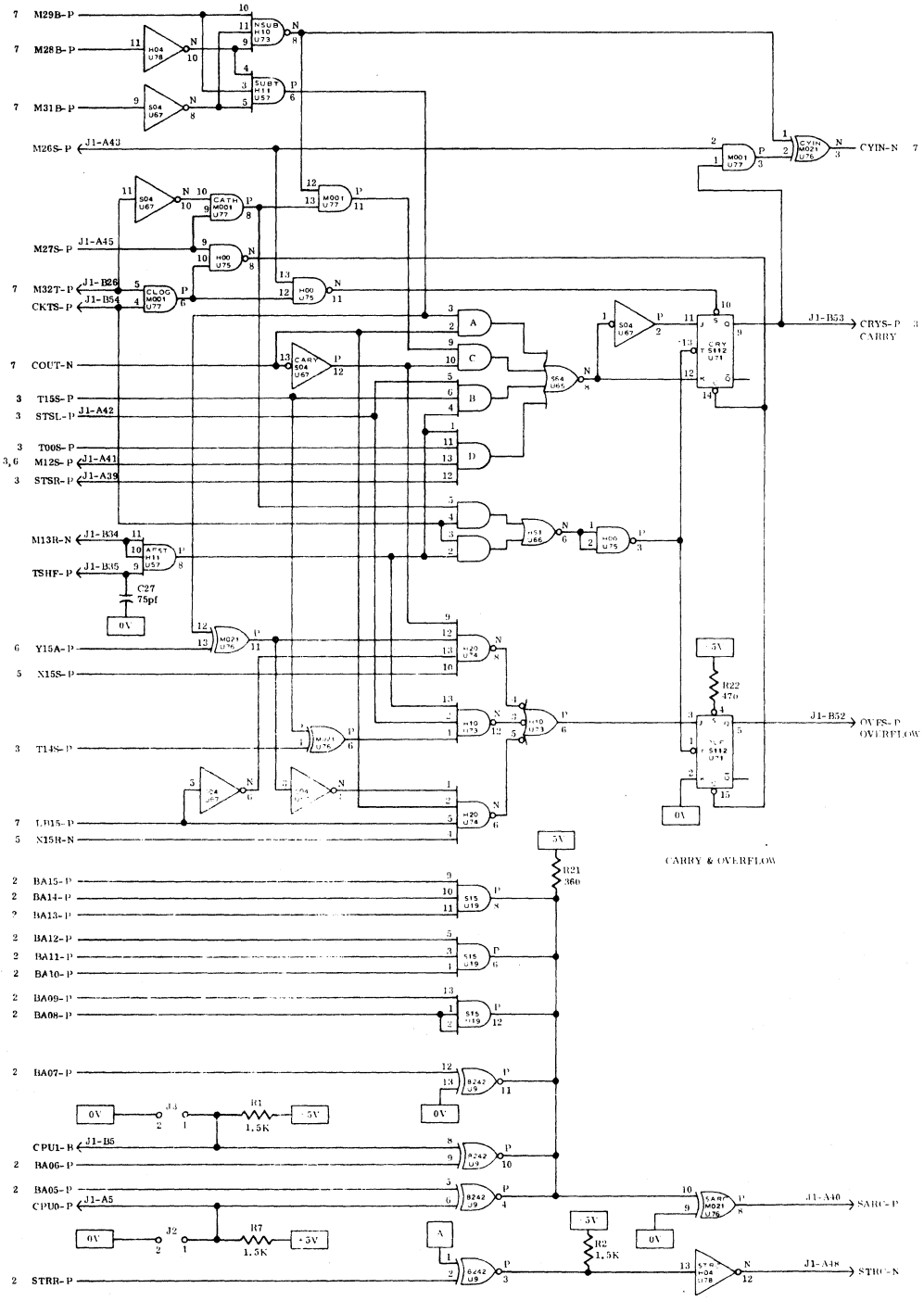
KEY SOURCE LOGIC DEFINITIONS

Carry and Overflow

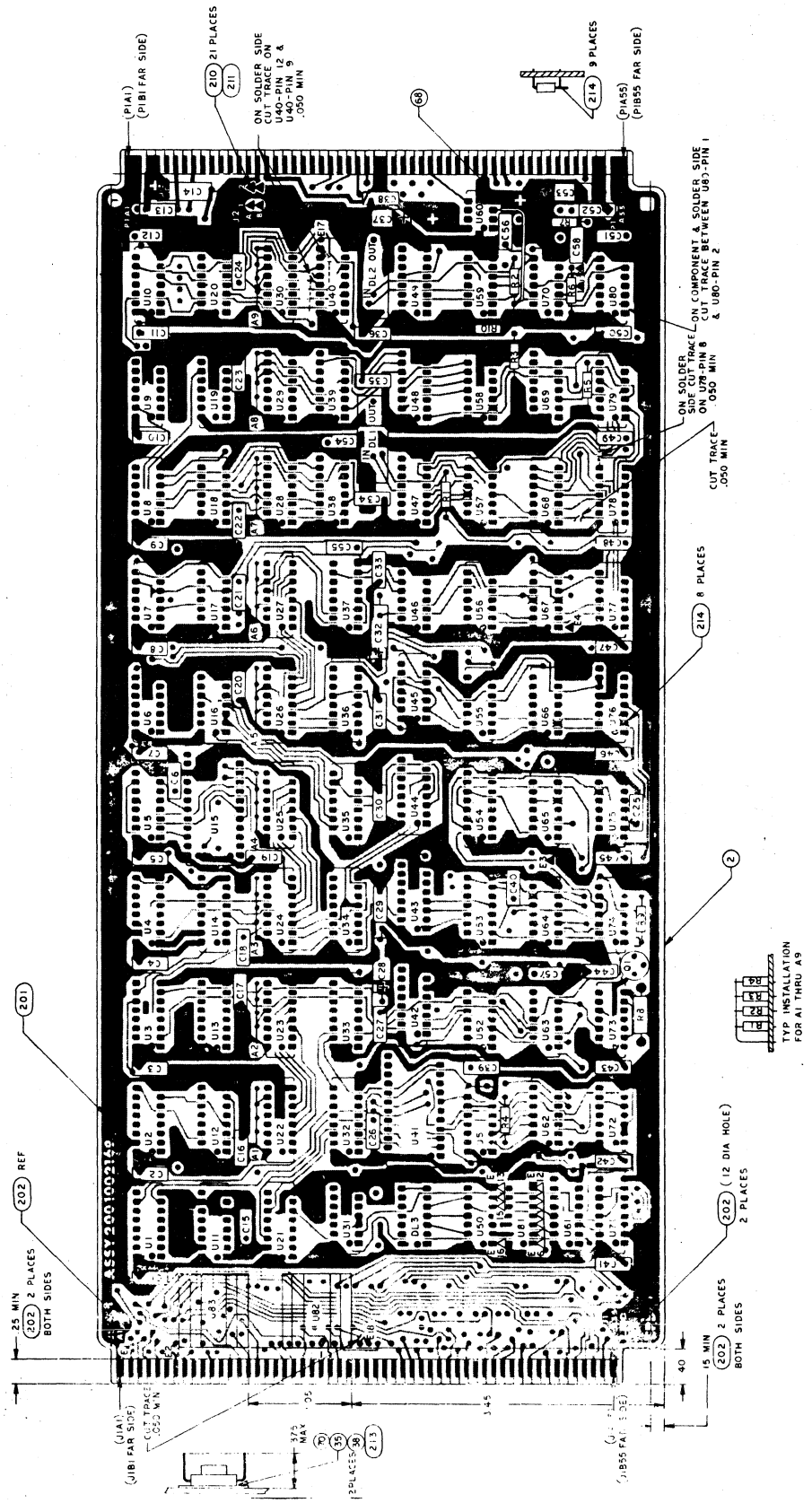
CKTS-P	Clocks ac and dc inputs to both carry and overflow.
CYIN-N	Negative carry input to the ALU logic derived under control of M-Register bits 26, 28, 29 and 31, and the state of the carry flip-flop. Normally, CYIN-N is either ZERO or carry true based on M26S-P (0 or 1, respectively); but when the ALU function code is 2 or 6 (subtract modes), then CYIN-N is either ONE or carry false, respectively.
CRYS-P	Carry flip-flop true output that may be set by M26S-P or reset by M27S-P during a logic cycle (M32T-P = 1); or it may be loaded from the carry output (COUT-N) by M27S-P during an arithmetic cycle (M32T-P = 0). Carry is loaded also during an arithmetic or logical linked shift cycle with data taken from the MSB or LSB of the T register based on left or right shift respectively.
OVFS-P	Overflow flip-flop true output that is reset (along with carry) by M27S-P during a logic cycle. This is the only reset for overflow. Overflow may be set only by either an arithmetic (logical linked) left shift where bits 15 and 14 differ in the T Register, or it may be set by an arithmetic operation when M27S-P is enabling the overflow detection logic. An overflow condition for the add mode occurs either when X, Y, and carry out are all ZERO and the sum is ONE (all for bit 15), or when X, Y, and carry out are all ONE and the sum is ZERO. For subtract mode, overflow occurs either when X and carry out are ZERO, and Y and the sum equal ONE, or when X and carry out are ONE, and Y and the sum equal ZERO.

Slave Address Recognition

SARC-P	Positive signal showing recognition of the processor's address space on the address bus.
STRC-N	The delayed negative strobe output from the INFIBUS which is sent to the CPB with SARC-P to initiate a slave memory cycle when both are asserted.



Arithmetic and Logic Unit CPA, Logic Diagram
LD2001002161-1, Rev. C, Sheet 8 of 8



Control Board CPB, Circuit Card Assembly
2001002169, Rev. D, Sheet 1

NOTES: UNLESS OTHERWISE SPECIFIED

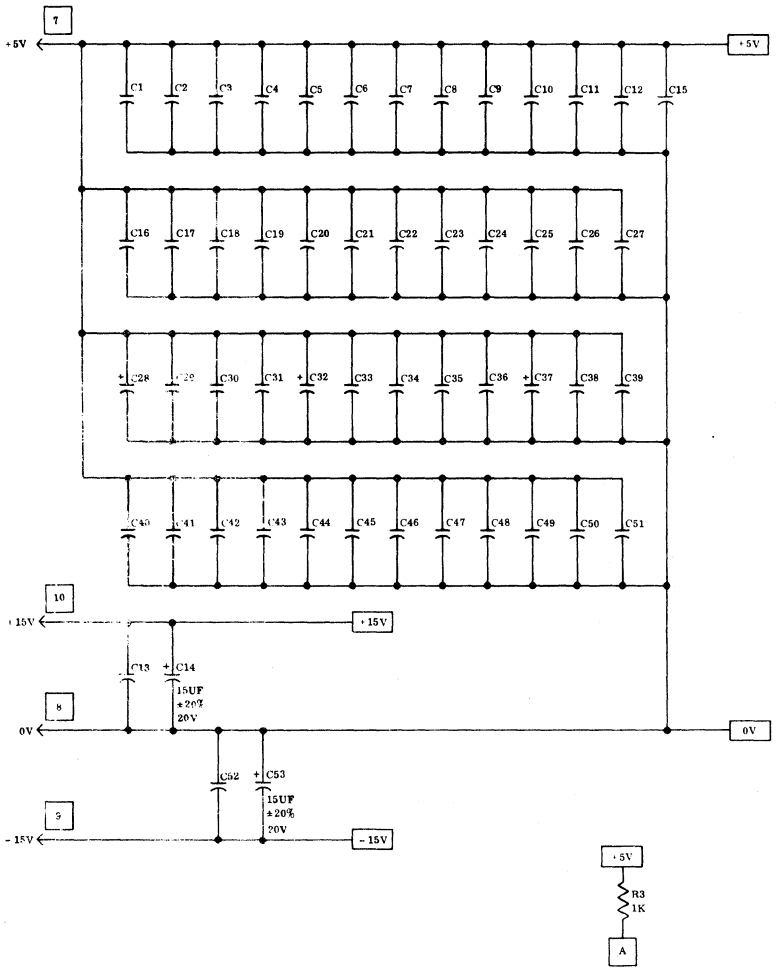
1. ALL RESISTORS ARE IN OHMS, ±2%, 1/4W.
2. ALL RESISTOR CLUSTERS ARE 470 OHMS, ±2%, 1/8W.
3. ALL NON-POLARIZED CAPACITORS ARE 0.1UF, +80%, -20%, 50V.
4. ALL POLARIZED CAPACITORS ARE 33UF, ±20%, 10V.
5. INTEGRATED CIRCUIT PACKAGE TYPE DESIGNATORS ARE ABBREVIATED, FOR COMPLETE PART NUMBER SEE PARTS LIST. (REFERENCE LIST ON DRAWING 8001800200.)
6. INTEGRATED CIRCUIT PACKAGE POWER PINS ARE: (8 PIN ICP) PIN 4 0V, PIN 8 +5V; (14 PIN ICP) PIN 7 0V, PIN 14 +5V; (16 PIN ICP) PIN 8 0V, PIN 16 +5V, EXCEPT BDR, PIN 7 AND 8 0V, PIN 16 +5V; (24 PIN ICP) PIN 12 0V, PIN 24 +5V.

7 +5V CONNECTOR PINS ARE: P1-A16, A28, A29, A51, B16, B28, B29, B51.

8 0V CONNECTOR PINS ARE: P1-A1, A2, A15, A40, A54, A55, B1, B2, B15, B40, B54, B55.

9 -15V CONNECTOR PINS ARE: P1-A52, A53, B52, B53.

10 +15V CONNECTOR PINS ARE: P1-A3, A4, B3, B4.



Control Board CPB, Logic Diagram
LD2001002169-1, Rev. C, Sheet 1 of 11

SEQUENCE COUNTER AND ROMS 1 THRU 9, CPB (LD2001002169-1, Sheets 2 and 3)

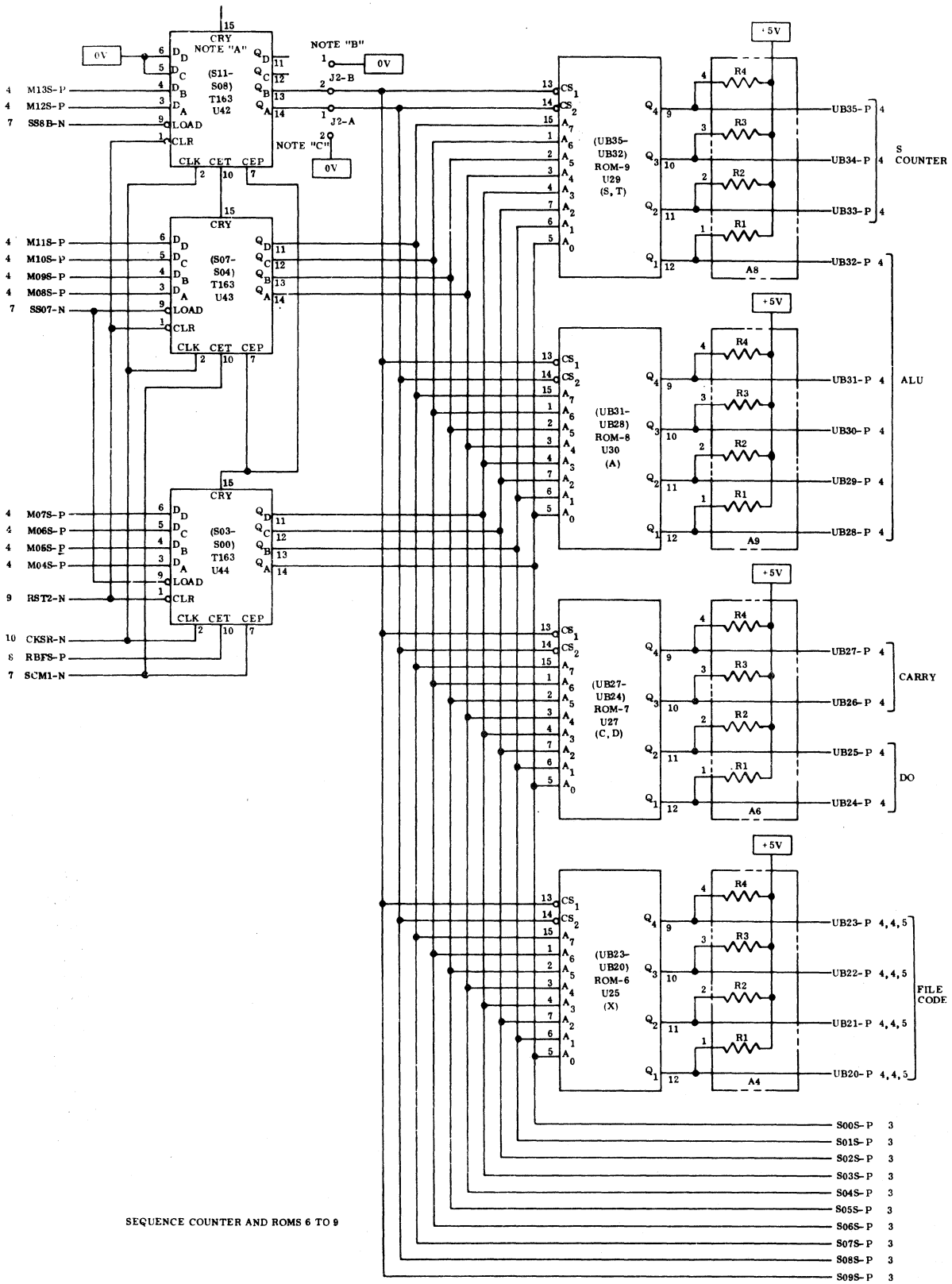
Sheet 2 shows the S register and most significant 4 ROMs; sheet 3 shows the least significant 5 ROMs. Jumper J2-A1,A2 and J2-B1,B2 are installed on SUE 1110 circuit cards to accommodate 8-bit addressing and U42 may not be installed. On SUE 1111 and 1112 circuit cards, U42 is installed and jumper J2-A1,A2 is removed, thereby allowing 9-bit ROM addressing. The ROMs are each 4 bits by 256 words for model 1110 or 512 words for models 1111 and 1112.

The S register is a 12 bit (or 8 bit) counter that normally addresses the ROM sequentially. However, a microcode jump occurs when the S register is loaded from the L1 and L2 (and sometimes M) fields. Also the counter stops incrementing when the Run flip-flop is turned off by a microcode hold (Special Command 1).

KEY SOURCE LOGIC DEFINITIONS

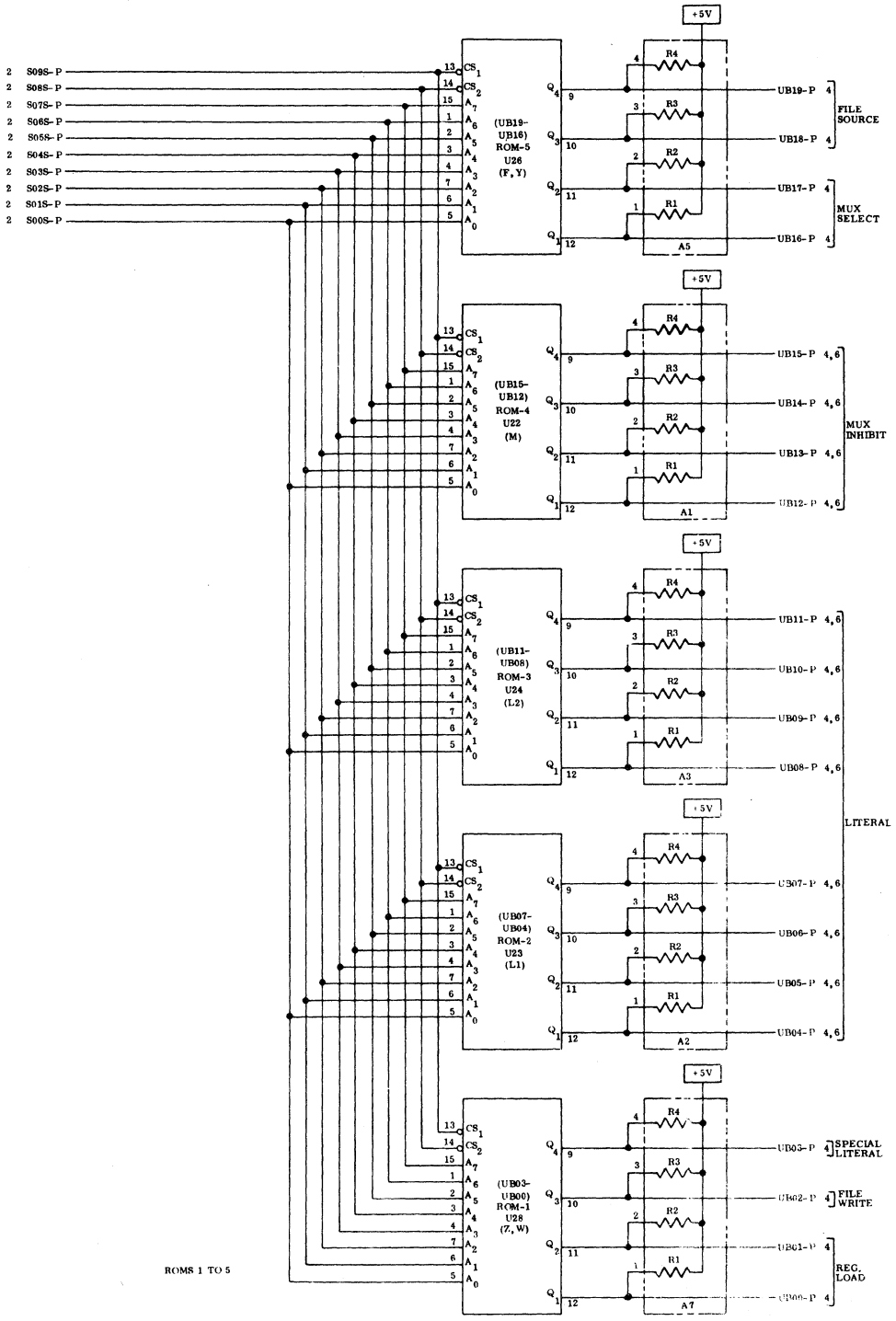
S00S-P thru S09S-P	Sequential S counter outputs used to address and enable the ROM control memory.
SCM1-N, RBFS-P	The two inputs that control counter incrementing. If either signal is low, the counter does not increment.
CKSR-N	The counter clock used for both incrementing and loading.
SS07-N	Used to load the low order 8 bits (L1 and L2 fields, M04 thru M11) on class codes 2 thru 7 (Jump and Conditional Branch).
SS8B-N	Used to load the high order 2 bits (2 LSB's of M field, M12 and M13) on class code 2 (Jump).
UB35-P thru UB00-P	All open collector ROM outputs which go to the M register (sheet 4); many of these ROM outputs may be modified by another open collector output and tied with them.
UB30-P, UB28-P, UB02-P	Tied to some NAND gates to the INFIBUS to modify the micro-command executed while Halted to provide appropriate response to a read or a write request addressing the processor.
UB23-P thru UB20-P	Connected to a 3-to-1 multiplexer that allows the file selection to be modified by either the E register or INFIBUS address lines.
UB11-P thru UB04-P	Connected to 2 table ROMs and some multiplexers to allow modification of the literal fields (L1 and L2) by status information or by tabled information.
UB15-P thru UB12-P	Connected to a multiplexer to allow Branch condition or Shift control (M field) to be controlled from the E register.

NOTE A: THIS CHIP IS INSTALLED FOR ROM SIZES OF 512 OR 1024 WORDS.
NOTE B. THIS JUMPER IS INSTALLED FOR ROM SIZES OF 256 OR 512 WORDS.
NOTE C: THIS JUMPER IS INSTALLED FOR ROM SIZES OF 256 WORDS.



SEQUENCE COUNTER AND ROMS 6 TO 9

Control Board CPB, Logic Diagram
LD2001002169-1, Rev. C, Sheet 2 of 11



Control Board CPB, Logic Diagram
LD2001002169-1, Rev. C, Sheet 3 of 11

MICRO-INSTRUCTION (M) REGISTER, CPB (LD2001002169-1, Sheet 4)

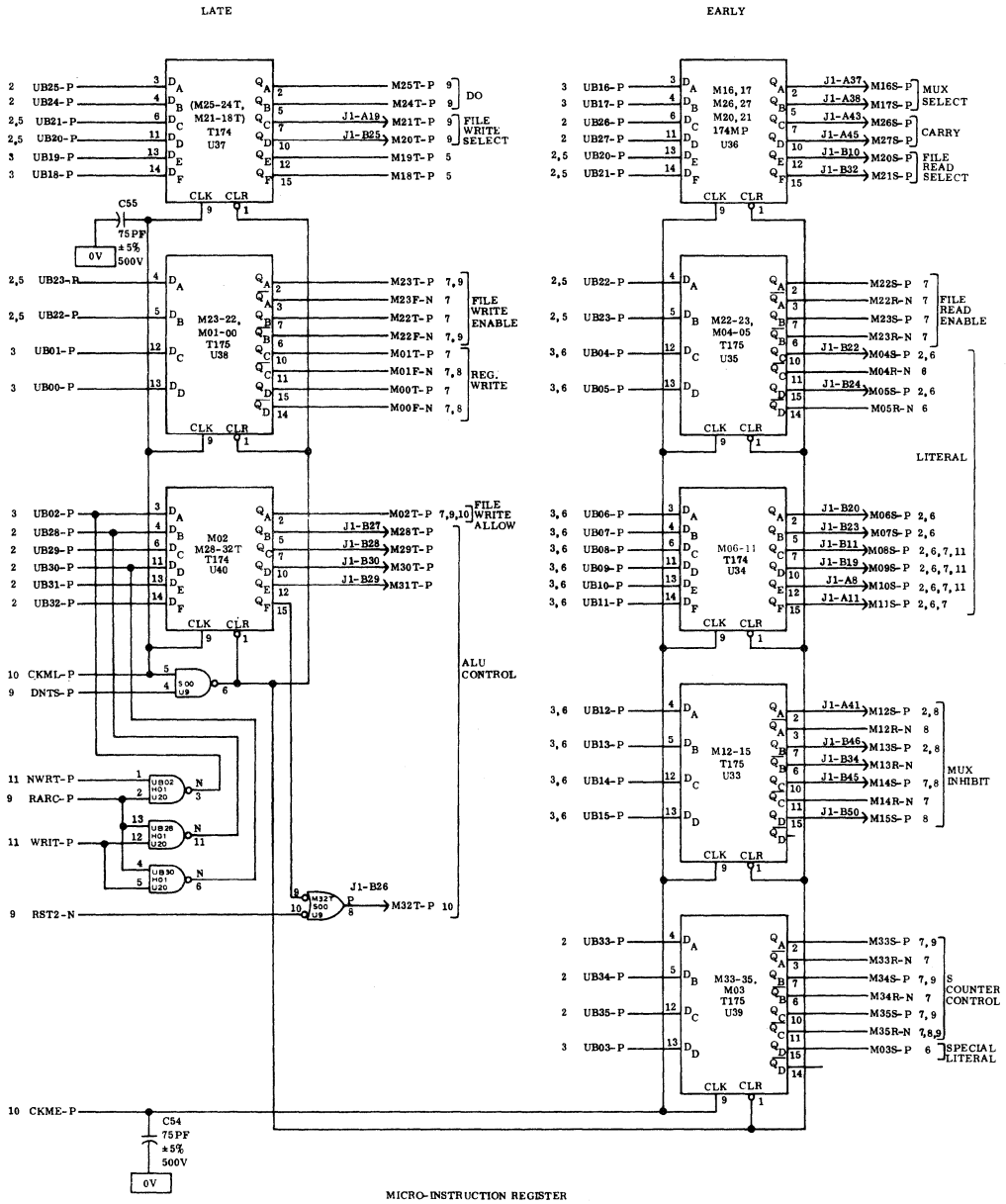
The micro-instruction register is divided into two parts, an early section clocked by the leading edge of CKME-P and a late section clocked by the leading edge of CKML-P (about 20 nanoseconds later). Functions which must be decoded quickly (such as the read file address) are driven by the early section, and functions which must be maintained late in the cycle (such as the write file address) are driven by the late section. The UB lines are the inputs to this register which contains D type flip-flops. Because the file read address and the file write address are derived from the same microcode field, UB20-P thru UB23-P drive inputs of both the early and late sections of the M register. When the DNTS-P signal from the DONT flip-flop is asserted, CKML-P also resets the entire M register by the DC clear inputs.

The following diagram shows the M register bits in each section, and which of the M register flip-flops have complementary outputs available (D) and which have only the singular outputs (S). The diagram also shows field definitions.

3 — 3 2 — 2 1 — 1 0 — 0	Bit
5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0	Number
D D D | | | S S | | D D S S | | S S | D D D D | S S S S | S S D D | D | |	EARLY (S)
| S | S S S S | | S S | D D S S | S S | | | | | | | S D D	LATE (T)
S | T | A | C | D | X | F | Y | M | L2 | L1 | Z | W	FIELD CODE

KEY SOURCE LOGIC DEFINITIONS

M35S-P thru M33S-P, M35R-N thru M33R-N (S Field)	Dual rail outputs decoded to control loading of the S counter and enabling the Special Command logic.
M32T-P (T Field)	Derived from a NAND gate giving the OR of the master reset signal (via RST2-N) and the buffered negation of the ROM output from bit 32 (via U40-15). This forces all machine cycles to be logical during reset since this signal controls the logic/arithmetic mode in the ALU's and in the clock generating logic.
M31T-P thru M28T-P (A Field)	Controls the function in the ALU's on the CPA. They also drive repeaters that share the ALU control load and help control the carry and overflow logic.
M27S-P, M26S-P (C Field)	Controls the carry and overflow logic on the CPA.
M25T-P, M24T-P (D Field)	Controls the logic allowing the DONT flip-flop to be set which gives the skip capability to the microcode.
M23S-P thru M20S-P, M23R-N thru M20R-N (early X Field)	Decoded to read enable the file (23 and 22) and to select the word (21 and 20) to be read from the Register file.
M23T-P thru M20T-P, M23F-N thru M20F-N (late X Field)	Decoded to write enable the file (23 and 22) and to select the word (21 and 20) to be written back to the register file if the file write bit (M02) is on.
M19T-P, M18T-P (F Field)	Used to enable and select inputs to a multiplexer that provides X field modification of the next micro-instruction.
M17S-P, M16S-P (Y Field)	Used to enable and select inputs to the Y input multiplexer for the ALUs.
M15S-P thru M12S-P, M15R-N thru M12R-N (M Field)	Used to select a test condition, address a bit in the T register to test, control the type of shift, select the ZERO zones when using a literal value, and give the two most significant bits of a jump address.
M11S-P thru M04S-P (L2 and L1 Fields)	Used to provide literal values, Jump and Branch addresses, select a special control function (L2), and select a Z control modification of the next micro-instruction.
M03S-P (Z control bit)	Used to enable special modification logic for the M, L2, or L1 fields of the next micro-command.
M00T-P thru M03T-P, M00F-N thru M01F-N (W Field)	Specifies whether or not to write into the file (M03) and/or which of registers T, A, or R to write into (M02, M01).
RARC-P, NWRT-P, WRIT-P	Control modification of the ALU operation and the file write enable to facilitate reading and writing into the file register via the INFIBUS while the processor is halted.



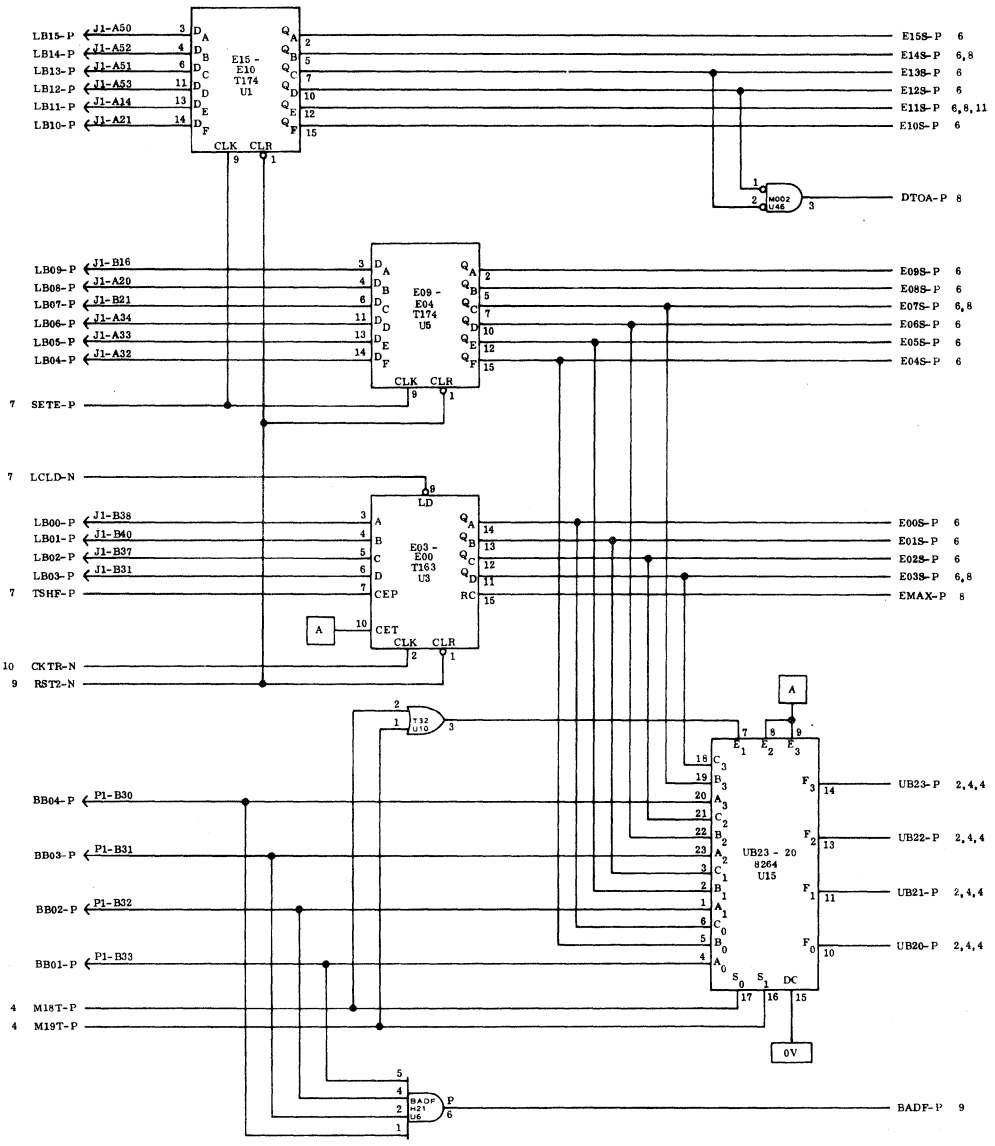
Control Board CPB, Logic Diagram
LD2001002169-1, Rev. C, Sheet 4 of 11

E REGISTER, CPB (LD2001002169-1, Sheet 5)

The E register holds a duplicate of the target instruction to be emulated. Many of its active outputs may be interrogated by a test multiplexer. It is also multiplexed to modify the X or M fields, or to address the table ROM. Bit 11 conditionally controls byte mode memory cycles. The four least significant bits are in a counter component and may be used to control shifts, etc. The maximum value of the counter may also be tested.

KEY SOURCE LOGIC DEFINITIONS

EMAX-P	An input to the test multiplexer indicating when the counter has reached maximum value (i.e. E00 thru E03 are all 1).
DTOA-P	An input to the test multiplexer indicating both E12S-P and E13S-P are low. It is used to differentiate target instruction class codes 0, 4, 8, and A from the rest.
BADF-P	Helps to indicate when register F is being addressed by the INFIBUS so that the control register can be accessed.
E00S-P thru E15S-P	The outputs of the E register going to various steering and test multiplexers.
UB20-P thru UB23-P	The open collectors of the X field input to the M register. The multiplexer (U15) selects 1 of 2 fields from the E register, or 4 low order word address lines from the INFIBUS, or nothing to modify the X field.
SETE-P	The clock to load the 12 most significant bits of the E register from the ALU outputs when M00 thru M02 are all true.
LCLD-N, CKTR-N	The enable and the clock respectively, to load the 4 least significant bits of the E register from the ALU outputs when M00 and M02 are both true.
TSHF-P	The count enable to count up the 4 least significant bits of the E register during a shift operation.



EMULATION INSTRUCTION REGISTOR
AND X FIELD MODIFICATION MULTIPLEXER

Z MODIFICATION AND SPECIAL COMMANDS 4 AND 5, CPB (LD2001002169-1, Sheet 6)

One of four special functions can be enabled by the Z field, bit M03. The particular function is selected by M04 and M05.

Function 3 provides modification of the next M field (M12 to M15) by the output of a multiplexer selecting (under control of M06 and M07) one of the four hexadecimal fields from the E register.

Function 0 uses the same multiplexer output to address 1 of 16 words from a page in a table ROM (U12 and U13). The specific page (1 of 16 in the table) is explicitly addressed by M08 thru M11 in the M register. The table ROM output modifies the L2 and L1 fields of the next micro-instruction.

Function 1 modifies M07 and M08 of the next micro-instruction with the current I/O interrupt level coming from the CPU.

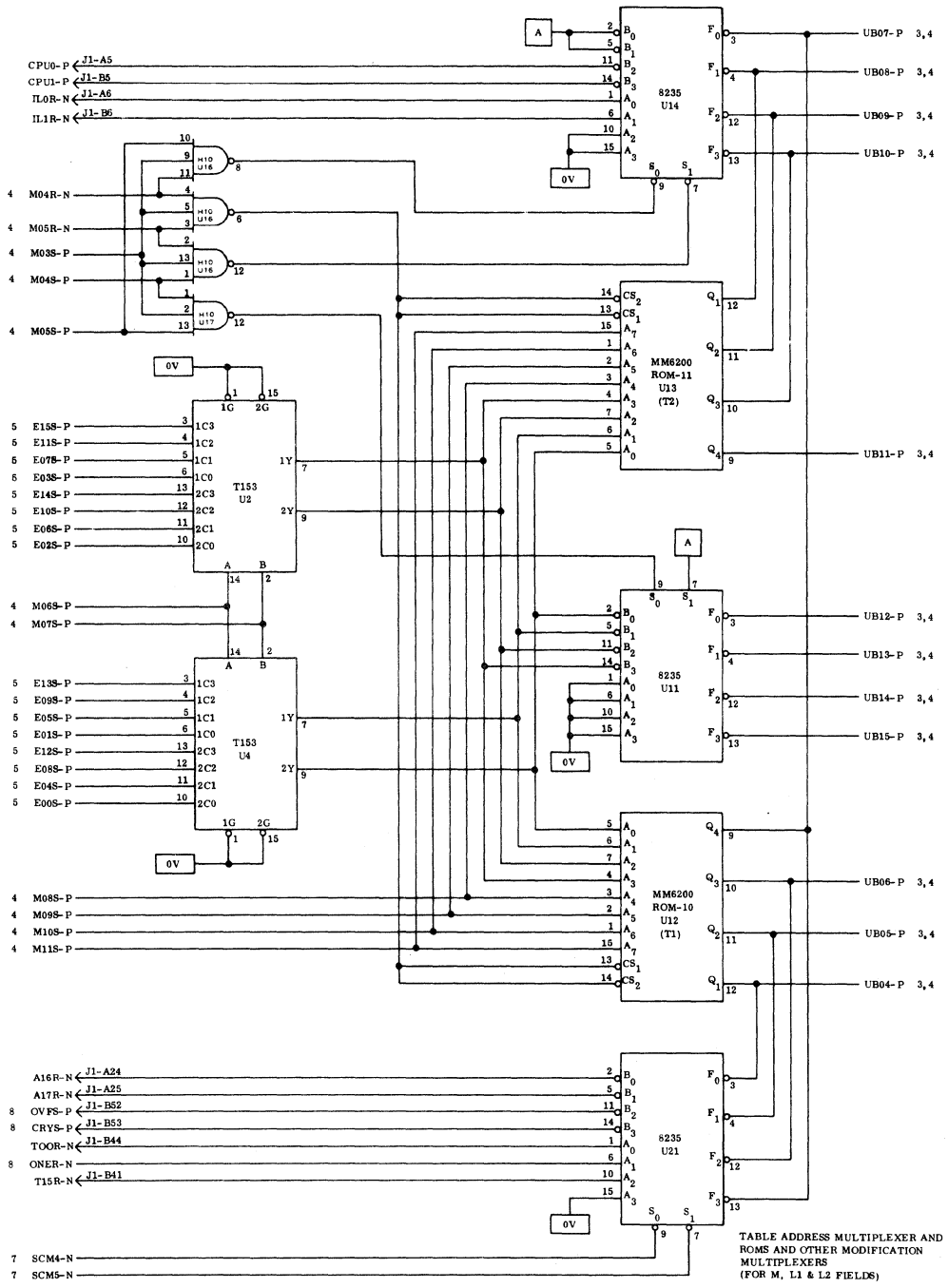
Function 2 modifies M09 and M10 of the next micro-instruction with the processor number.

Special Command 4 modifies M04 thru M07 (L1) of the next micro-instruction with the inverted Key bits (A16R and A17R) and with the Overflow and Carry flip-flops (each in respective order).

Special Command 5 modifies M04 thru M06 of the next micro-instruction with the least significant bit from the register, the output of the All Ones flip-flop, and the most significant bit of the T register (each in respective order).

KEY SOURCE LOGIC DEFINITIONS

UB04-P thru UB15-P	The open collector inputs to the M, L2, and L1 fields of the M register. The ROMs (U12 and U13) and the multiplexers (U11, U14, and U21) may modify these signals as they come into the M register thus giving the modification of the next micro-instruction.



Control Board CPB, Logic Diagram
LD2001002169-1, Rev. C, Sheet 6 of 11

FILE ENABLE TERMS, TEST MULTIPLEXER,... CPB (LD2001002169-1, Sheet 7)

The logic shown on LD sheet 7 performs a variety of functions:

The read and write enable signals (RExx-N and WExx-N) are generated to allow reading from the register files and writing into the files.

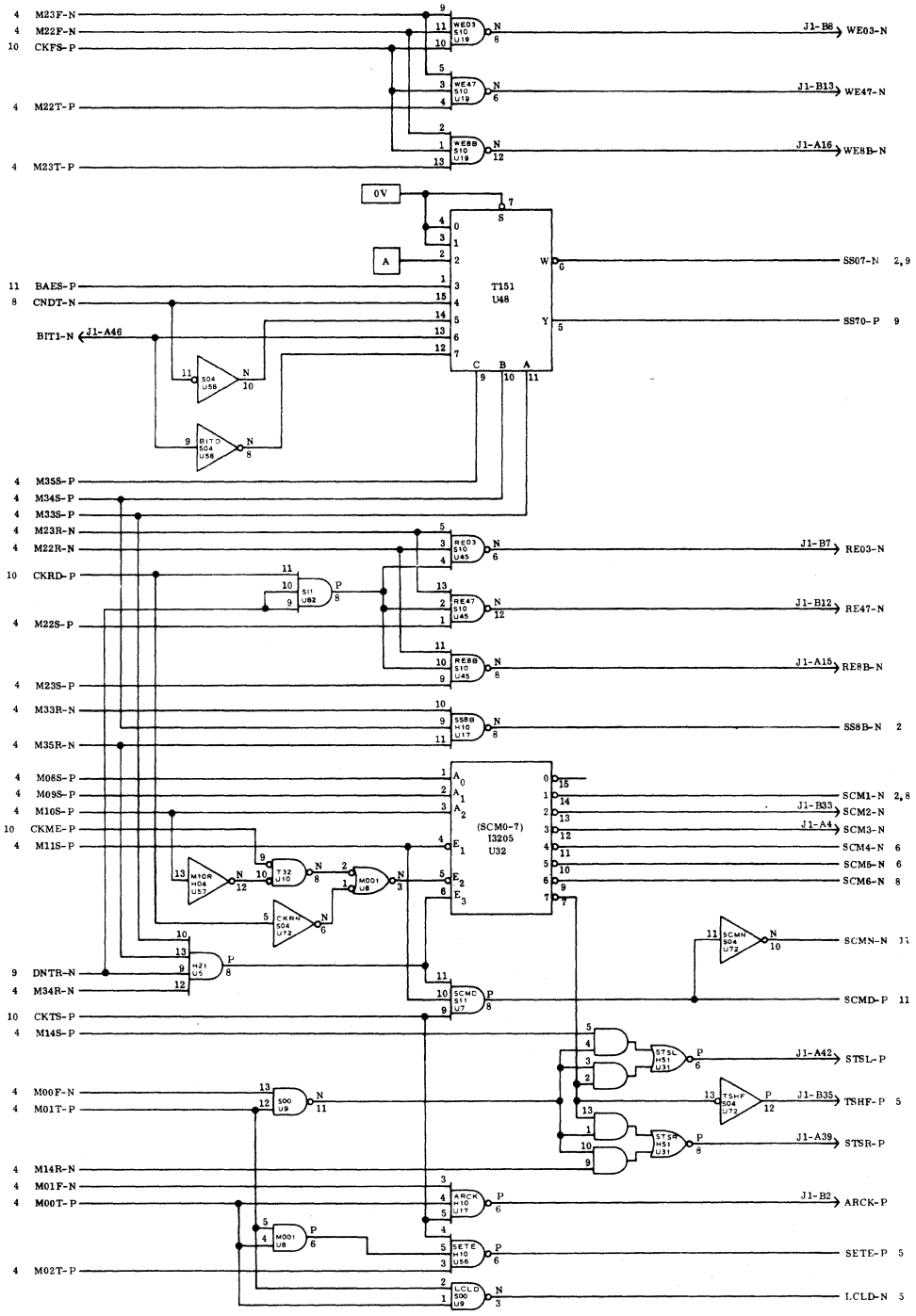
The multiplexer (U48) and gate addressed by the S field code (M33 thru M35) provide the micro-sequence load enable (i.e. branch) controls used to load the sequence counter and Dont flip-flop.

Special Commands (SCMx-N) including shifts and memory accesses, are activated when the S field code equals ONE

The clock enable terms shown in the lower part of the drawing are generated to load the A and E registers.

KEY SOURCE LOGIC DEFINITIONS

ARCK-P	Enabled clock to load the A register from the ALU outputs.
LCLD-N	Loads enable for the four least significant bits of the E Register.
SETE-P	Enabled clock to load the 12 most significant bits of the E Register.
RE03-N, RE47-N, RE8B-N, WE03-N, WE47-N, WE8B-N	Read Enable, Write Enable for the register file.
SCMD-P	Special command to initiate memory access with CKTS-P as clocking term.
SCMN-N	Negation of SCMD-P used to reset the Abort flip-flop on any memory access including no-cycle request.
SCM1-N thru SCM6-N	Specific decodes for special commands 1 thru 6 (active low). Timing for commands 1 thru 3 are different than timing for commands 4 thru 6.
SS8B-N	Decode of Jump Class to enable load of most significant bits of the micro-sequence (S) counter.
STSL-P, STSR-P	Active low T register mode control lines. If both are low the T register loads; if one only is low the T register shifts (left on STSL, right on STSR) and if both are high the T register is stable.
SS07-N, SS70-N	Positive and negative outputs of the micro-sequence control to enable load of eight low order bits of the micro-sequence counter (SS07-N) and to input the Dont flip-flop multiplexer for skip control.
TSHF-P	Special Command 7 (active high) for general shift control.



FILE ENABLE TERMS, TEST MULTIPLEXER, SPECIAL COMMAND DECODE.
REG E AND A CLOCKS AND ENABLE TERMS

Control Board CPB, Logic Diagram
LD2001002169-1, Rev. C, Sheet 7 of 11

JUMP MULTIPLEXER, NEXT FLIP-FLOP, ALL-ONES FLIP-FLOP, ... CPB (LD2001002169-1, Sheet 8)

E register bits and other status are addressed by the M field via the jump multiplexer to determine conditional jumps in the microcode.

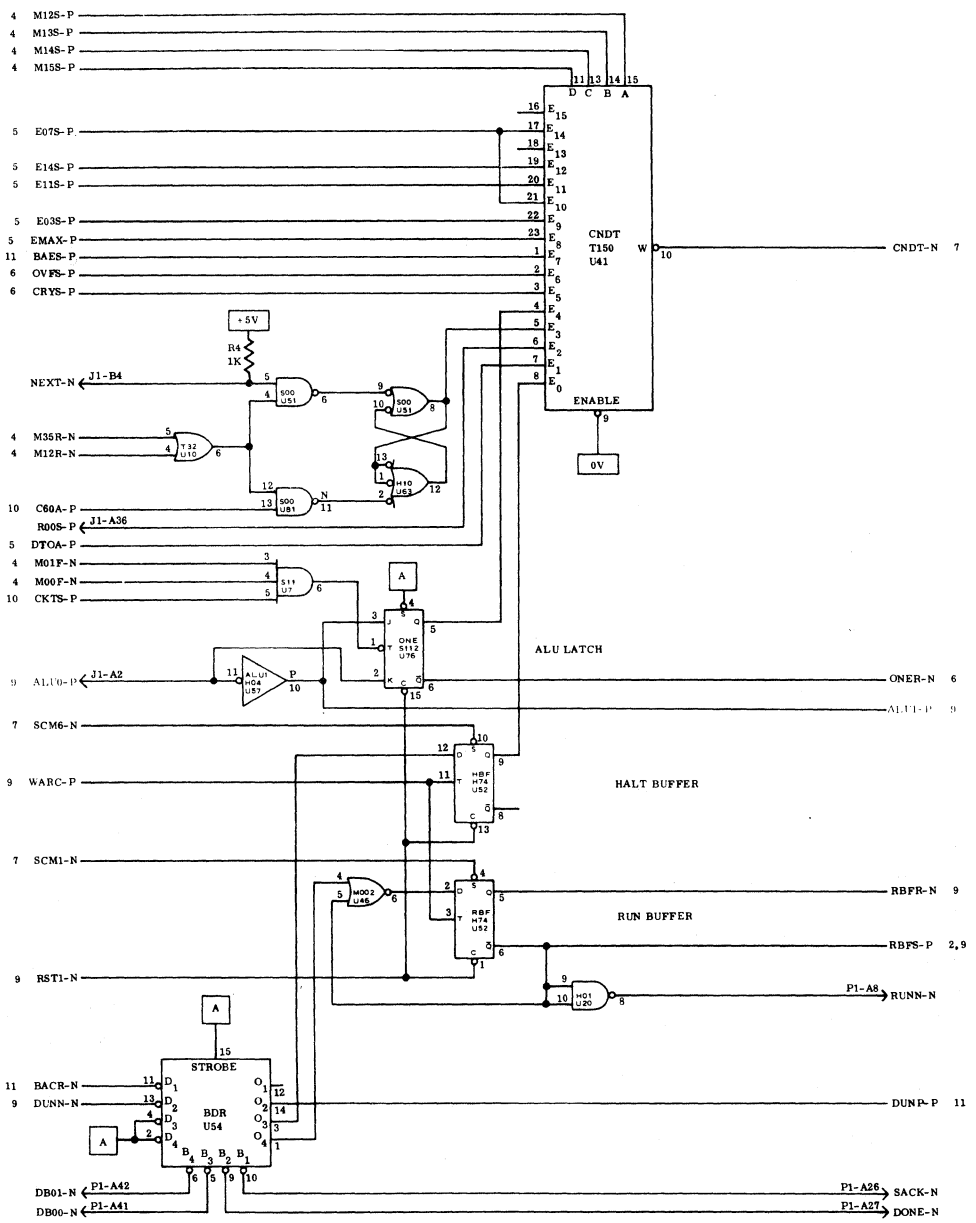
A pending interrupt is buffered in the NEXT flip-flop.

The Halt and Run flip-flops may be loaded from the INFIBUS (however, the Run may be set only from the INFIBUS).

The Ones flip-flop is loaded from the ALU result if none of registers A, T, or R is loaded.

KEY SOURCE LOGIC DEFINITIONS

ALU0-P	The negation of ALU1-P used for the inverse input to the K terminal and to the Dont flip-flop multiplexer U47 (sheet 9).
NEXT-N	The asynchronous signal from the BCU indicating an interrupt is pending. It must be buffered to prevent a race condition in the CNDT-N output.
CNDT-N	The output sampled from various status conditions in the system and used to control conditional branching in the microcode.
DB00-N, DB01-N	The two low order data inputs from the INFIBUS which may be clocked into the control register (Halt and Run flip-flops) to start and stop the operation.
DONE-N	The INFIBUS signal sent when responding as a slave device and received when acting as a master device.
DUNP-P	The received DONE-N signal used to complete a memory cycle and strobe the read data from the INFIBUS.
HALT Buffer	A flip-flop set either externally via the INFIBUS or by the microcode Special Command 6 and that may be interrogated by the microcode to check for a Halt request.
ONER-N	The negative side of the All-Ones flip-flop used to help provide the status to load into the status register via the multiplexer U21 (sheet 9).
RBFR-N, RBFS-P	The outputs of the Run flip-flop used to increment the sequence (S) counter and generate system clocks while running or when halted.
R00S-P	The least significant bit of the R register used as a test input for detecting multi-level indirect addressing.
RUNN-N	Drives the INFIBUS line to light the Run indicator on the control panel.
SACK-N	The INFIBUS signal sent to acknowledge selection of the CPU for the next INFIBUS (memory) cycle.



JUMP TEST MULTIPLEXER, NEXT BUFFER, PART OF INFIBUS INTERFACE, CONTROL AND ALL ONES FLIP FLOPS

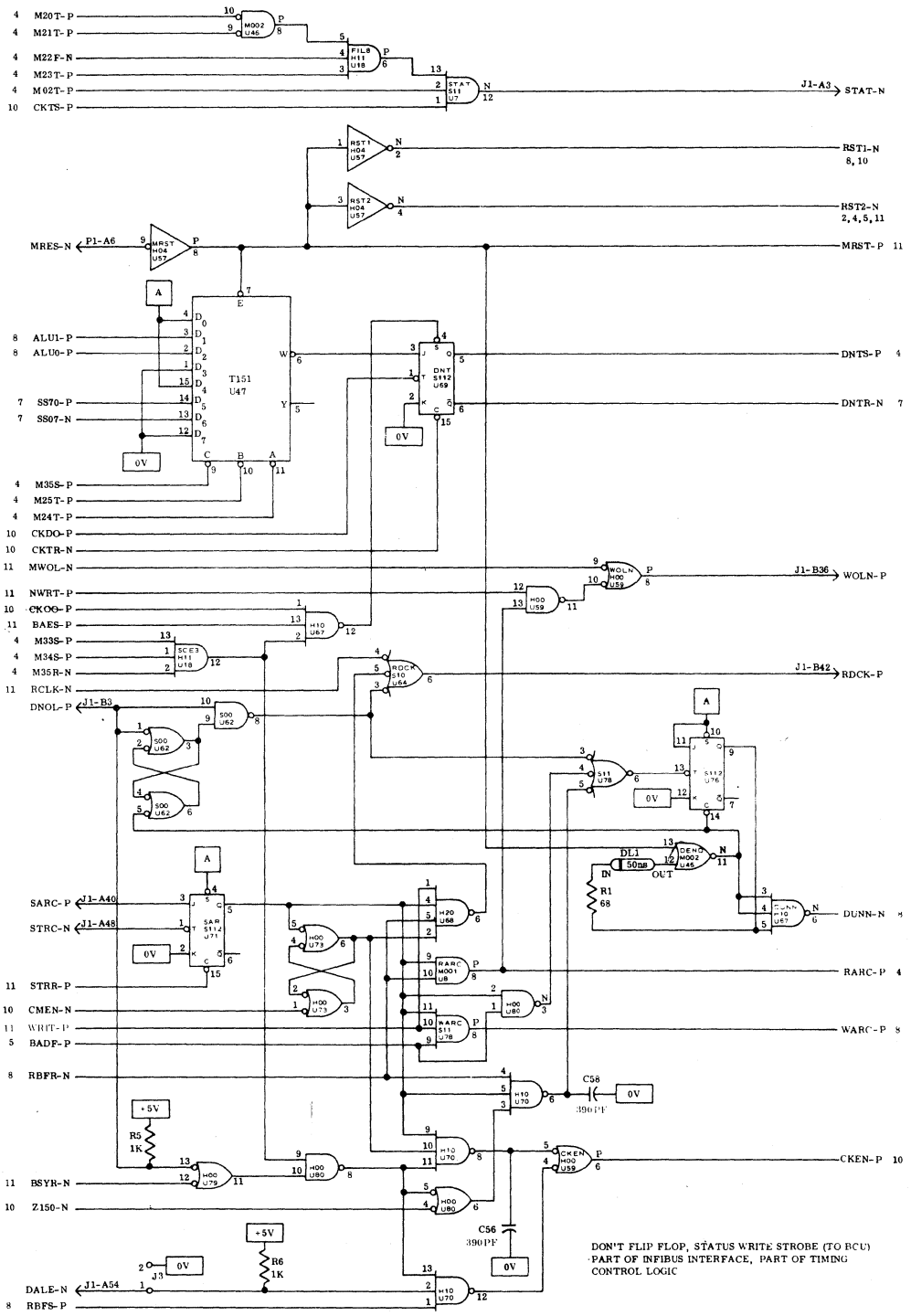
Control Board CPB, Logic Diagram
LD2001002169-1, Rev. C, Sheet 8 of 11

DONT FLIP-FLOP, STATUS WRITE STROBE, ... CPB (LD2001002169-1, Sheet 9)

The logic on LD sheet 9 controls: access to the INFIBUS data lines (WOLN-P, RDCK-P); slave cycles (RARC-P, WARC-P, DUNN-N); clock sequence initiation after a WAIT micro-step (CKEN-P); clearing of M register for NO-OP micro-steps (DNTS-P, DNTR-N); general processor hardware reset (MRST-P, RST1-N, RST2-N); and writing to the interrupt mask flip-flops in the BCU (STAT-N).

KEY SOURCE LOGIC DEFINITIONS

CKEN-P	Interrupts the clock sequence when low. One input (pin 4) allows normal running unless the RUN flip-flop is reset, a Wait micro-step is encountered, or DALE is grounded. The other input allows a single clock sequence to be generated from the INFIBUS interface logic.
DALE-N	Single micro-step control input, when grounded, CKEN must be activated by the control panel Run button (via the INFIBUS and through gate U70, pin 8) to generate individual clock sequences.
DNTS-P, DNTR-N	Outputs of the Dont flip-flop that cause the micro-instruction currently being fetched to be reset as it is buffered in the M register, thus, giving a no-operation.
DNOL-P	The Device Number On Line signal coming from the BCU to indicate that a controller has placed its device number on the INFIBUS data lines for pick up by the CPU.
DUNN-N	A pulse (greater than 50 nanoseconds) generated by reset, or at the end of a processor slave cycle, to signal the completion of the INFIBUS data cycle and strobe the output data in read.
MRST-P	The positive master reset pulse originated by the control panel reset function.
RARC-P	Enables the logic to modify the ALU code and write file bit in the M register during the micro-steps executed with the run flip-flop off (i.e. halted) while acting as a slave device.
RDCK-P	The clock for the R register (in the CPA) to enable data from the INFIBUS to be loaded into the R register.
RST1-N, RST2-N	The negative master reset pulse originated by the control panel reset function.
STAT-N	The signal to the BCU indicating that the status register is being written into. It is used to clock the four most significant bits from the ALU bus into the BCU interrupt mask flip-flops.
WARC-P	Clocks the control flip-flops (Run and Halt) to receive data from the INFIBUS when the control register is written into.
WOLN-P	The write enable to send data from the T register through inverters and bus drivers out onto the INFIBUS data lines.



Control Board CPB, Logic Diagram
LD2001002169-1, Rev. C, Sheet 9 of 11

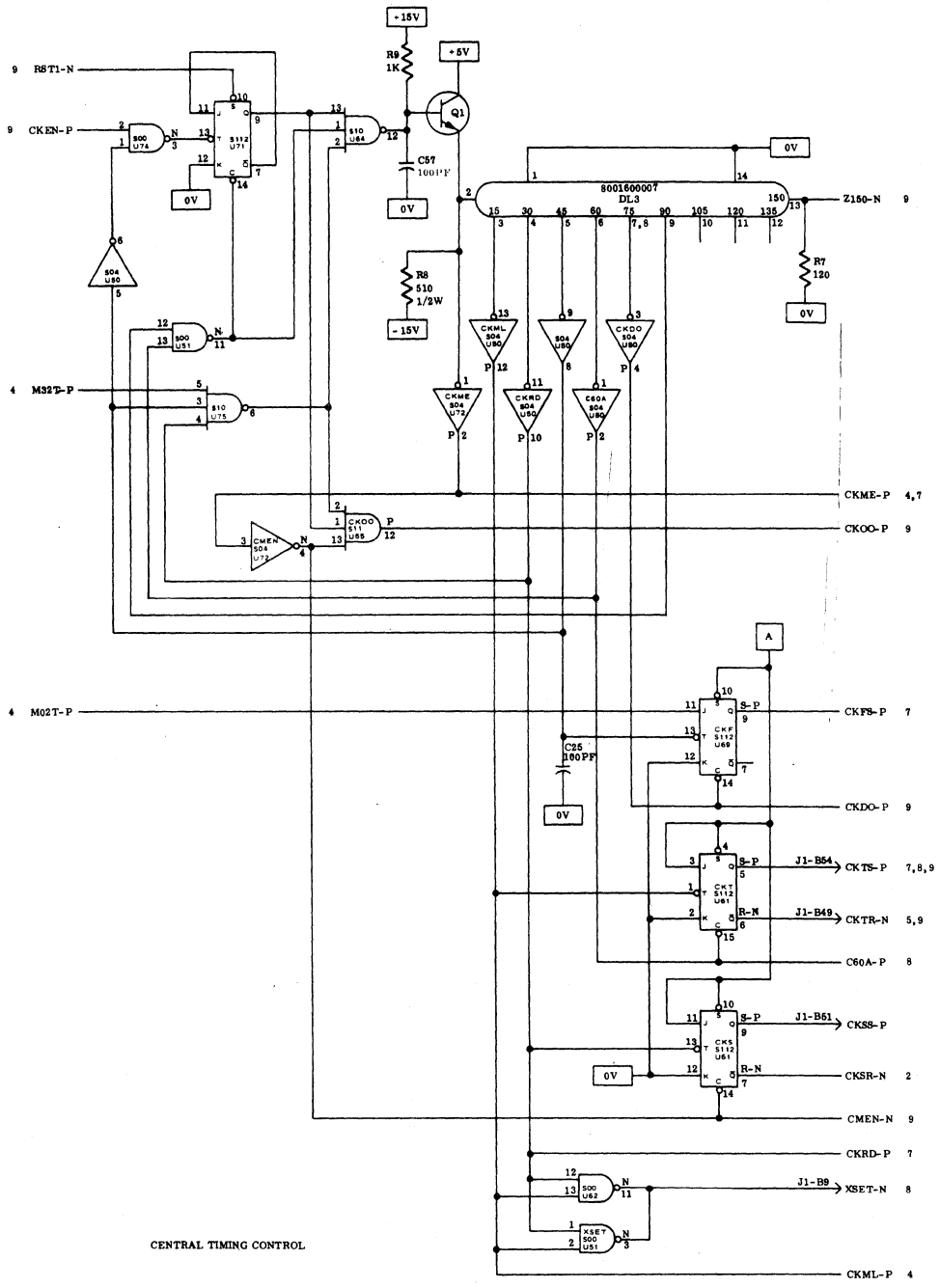
CENTRAL TIMING CONTROL, CPB (LD2001002169-1, Sheet 10)

The various clocking terms are generated from a 150-nanosecond tapped delay line. The delay line is driven by an emitter follower, its outputs are buffered by inverters, and it is terminated with a 120-ohm resistor. The taps are at 15-nanosecond intervals and the various timing relationships needed are derived by combining them with gates and flip-flops and tuning where necessary with capacitors. The basic signal traverses the delay line and recirculates with the opposite polarity to give a length effectively greater than 150 nanoseconds. The recirculation path is controlled by M32T-P to give two basic cycle times for logical ALU operations (shorter) and for arithmetic ALU operations (longer). Circulation is stopped while CKEN-P is low during a Wait micro-step. Short (logic) cycles are forced during the reset pulse (RST1-N). Signal M02T-P is an enabling term for the CKFS-P clock used to write to the file registers.

See figures 3 and 4 at the beginning of the drawing section for clock timing. Figure 3 shows how signals are re-initiated after a wait micro-instruction. The first cycle is arithmetic (155 nanoseconds) and the second cycle is logical (145 nanoseconds). Figure 4 shows the relative timing for a halt, file access, or start sequence.

KEY SOURCE LOGIC DEFINITIONS

C60[illegible]-1	Resets the interrupt buffer (CPB sheet 8) when the NEXT pulse is not present.
CKDO-P	Clocks the Dont flip-flop by its trailing edge late in the cycle. It also clears the CKFS-P flip-flop at the same time.
CKFS-P	Clocks the file write enable (select) terms to generate a short write pulse to the enabled file register components late in the cycle.
CKME-P	Clocks the ROM outputs into the early portion of the M register at the beginning of the cycle. It also extends timing on special commands 4, 5, 6 and 7 (shifts).
CKML-P	Clocks the ROM outputs into the late portion of the M register early in the cycle and clears the entire M register if the Dont flip-flop is set.
CKRD-P	Enables the file read-select gates and controls the timing for special commands 1 through 7.
CKSR-N, (CKSS-P)	Clocks the S counter for incrementing or loading a new ROM address.
CKTR-N, CKTS-P	Used widely to clock the T, E, and A registers, the Dont, Carry, Overflow, Ones, and Memory Control flip-flops and the interrupt MASKS in the Bus Control Unit (BCU).
CK00-P	Sets the Dont flip-flop when a memory abort takes place during a wait condition.
CMEN-N	Resets the NAND latch shown on sheet 9 that is used to interlock controls during slave memory operations.
XSET-N	Controls the file latches between reading the file registers.
Z150-N	Drives a gate to trigger the DUNN-N signal at the end of a slave memory cycle when the processor is halted.



Control Board CPB, Logic Diagram
LD2001002169-1, Rev. C, Sheet 10 of 11

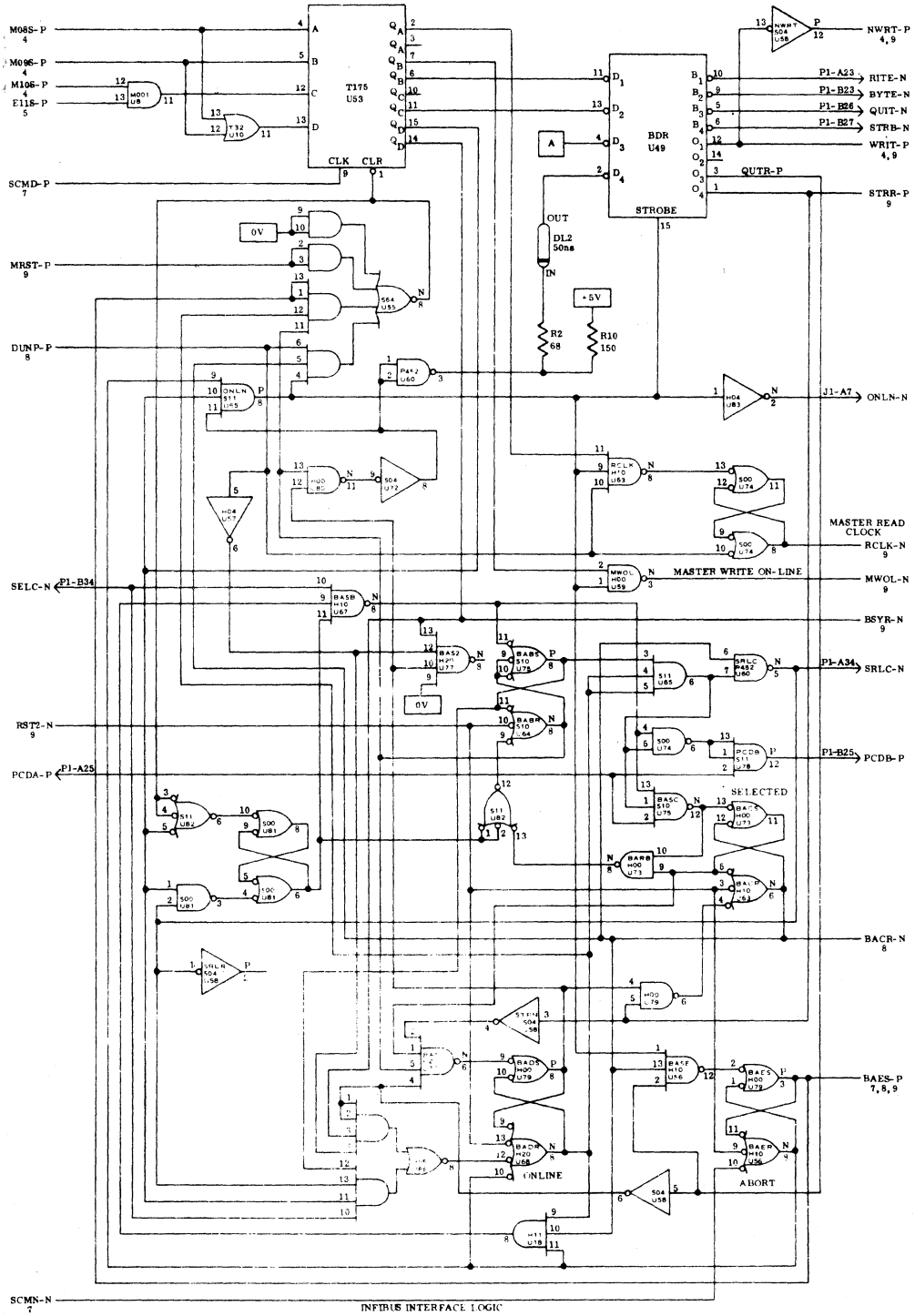
INFIBUS INTERFACE LOGIC, CPB (LD2001002169-1, Sheet 11)

The logic shown on sheet 11 controls the interface between the processor and the INFIBUS during a master memory access cycle. The logic provides the asynchronous interlocks required to maintain the bus dicipline during a read or a write cycle.

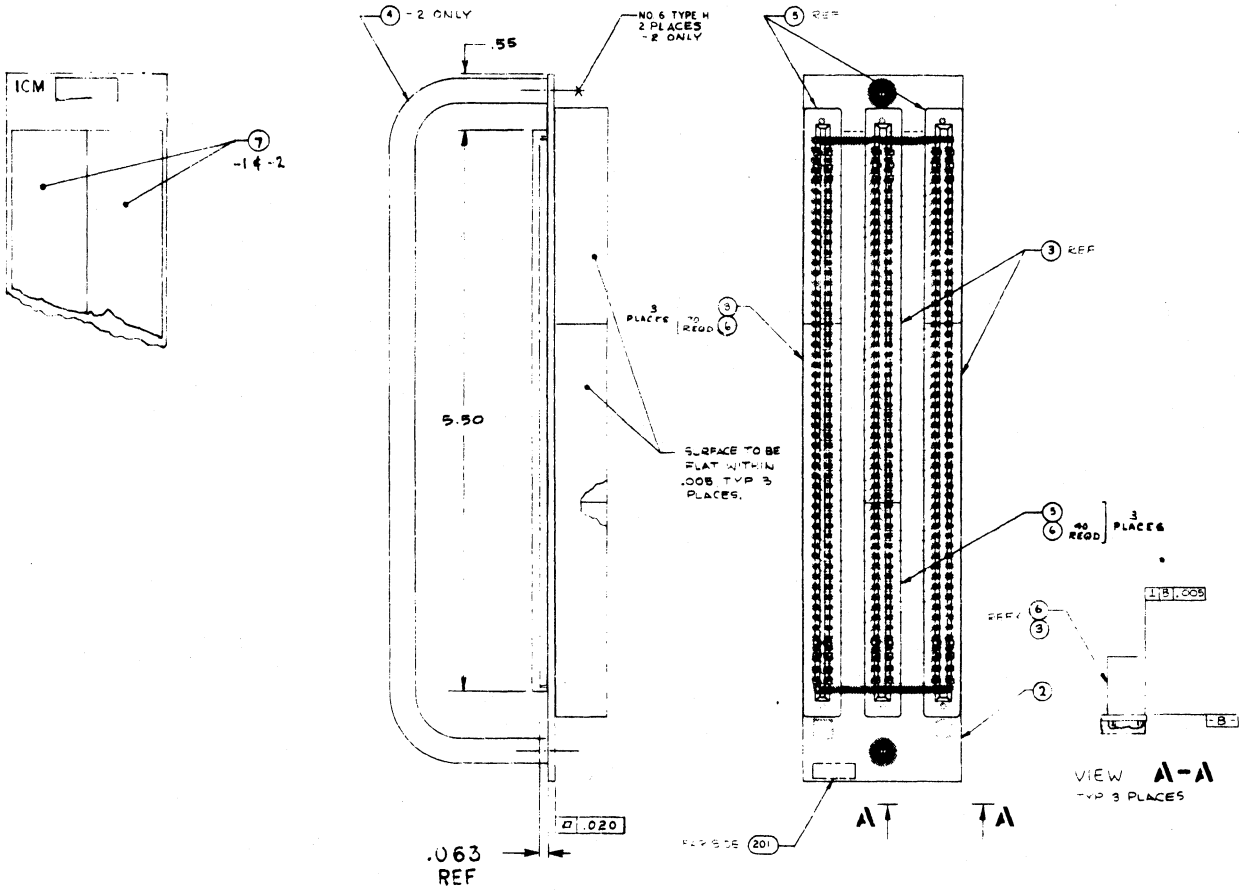
The capability to properly control a read-modify-write (RMW) cycle is not included, but when a RMW cycle is attempted, a write cycle is performed with the T register also writing into the R register via the data bus. Then the write portion of the RMW sequence performs a normal write cycle.

KEY SOURCE LOGIC DEFINITIONS

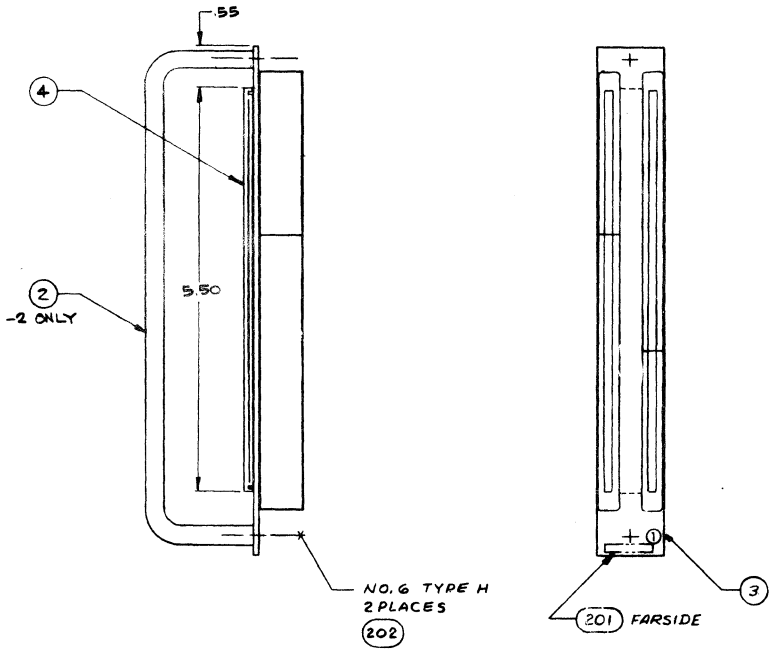
BACR-N	Not selected — used to: enable the INFIBUS request signal (SRLC-N), enable and acknowledge bus selection, and enable either the cycle completion or the abort condition.
BAES-P	The buffered memory abort condition used to cause a jump and skip on a Wait micro-instruction.
BSYR-N	No memory cycle is in progress, allowing normal clock generation to proceed on a Wait micro-instruction.
BYTE-N	The INFIBUS control signal requesting half word memory operation.
MWOL-N	The enabling term generated by the master memory write cycle logic to place data from the T register onto the INFIBUS. MWOL-N is combined with the enabling term for the slave memory read cycle.
NWRT-P, WRIT-P	Write control signals received from the INFIBUS and used during a slave memory cycle to select the ALU operation and to control writing to the control register, the file register, and placing data out on the INFIBUS.
ONLN-N	A general enabling signal for control outputs to the INFIBUS and read, write and abort controls. ONLN-P is true when the processor goes on-line and stays true until the cycle completes or is aborted.
PCDB-P	The outgoing precedence pulse generated by the incoming precedence pulse and disabled by having the proper select conditions and a request waiting.
QUIT-N	The INFIBUS signal that causes the present memory cycle to abort. Generated by the bus controller, it sets the abort flip-flops if the processor is selected and on line.
RCLK-N	The pulse generated by the master memory read cycle logic to clock data from the INFIBUS to the register. It is combined with the clocking term for the slave memory write cycle.
RITE-N	The INFIBUS control signal requesting a write operation to memory.
SRLC-N	Service Request level C on the INFIBUS used to request the next available data cycle from the BCU.
STRB-N	The INFIBUS control signal used to strobe the address, write data and cycle controls sent out from the processor during a master memory cycle.
STRR-P	The strobe received from the INFIBUS and used by the slave cycle to remove the reset from the self address recognition flip-flop (SAR) and used by the master cycle to enable the reset of the selected flip-flop and disable the set of the On-Line flip-flop.



Control Board CPB, Logic Diagram
LD2001002169-1, Rev. C, Sheet 11 of 11



Interconnect Module ICM, Circuit Card Assembly
2001002166, Rev. C, Sheet 1



Interconnect Dual Module IDM, Circuit Card Assembly
2001002232, Rev. B, Sheet 1

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002232-1		IDM-CKT CARD ASSY		USED ON SUE 1110	1
002		000								2
003		001	0001		1001005188-1		CONNECTOR ASSY, IDM			3
004		006	0001		4508 .75 WIDE	04963	FOAM TAPE	3M CO	APPROX INCH REQD	4

Interconnect Dual Module, IDM, Parts List
PL2001002232-1, Rev. B, Sheet 2

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002166-0		ICM-CKT CARD ASSY		PROCUREMENT ONLY	1
002		001	0001		1001004808-1		PRINTED WRG BD, ICM			2
003		003	0001		121-7360-035	71468	INSULATOR, ECP4	ITT CANNON	70 POS (DUAL 35)	3
004		003	0001		121-7360-020	71468	INSULATOR, ECP4	ITT CANNON	40 POS (DUAL 20)	5
005		330	0001		030-7331-001	71468	CONTACT, ECP4	ITT CANNON	.094 THK BD	6

Interconnect Module, ICM, Parts List
PL2001002166-0, Rev. C, Sheet 2

	SYM	QTY REQD	SERIAL NO START	SERIAL NO END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002166-1		ICM-CKT CARD ASSY		USED ON SUE 1110-1	1
002		001	0001		2001002166-0		ICM-CKT CARD ASSY			2
003		000								3
004		000								4
005		000								5
006		000								6
7		012	0001		4508 .75 WIDE	04963	FOAM TAPE	3M CO	APPROX INCH REQD	7

Interconnect Module, ICM, Parts List
PL2001002166-1, Rev. C, Sheet 3

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002161-1		CPA-CKT CARD ASSY		USED ON SUE 1110A-1/1110A-2	1
002		001	0001		1001004810-5		PRINTED WRG BD, CPA		NOTE 213	2
003		003	0001		8001800047-1		ICP		U47,48,57 (74H11)	3
004		002	0001		8001800042-1		ICP		U49,75 (74H00)	4
005		004	0001		8001800043-1		ICP		U2,12,22,32 (74H01)	5
006		006	0001		8001800044-1		ICP		U42,43,44,58,68, 78 (74H04)	6
007		001	0001		8001800046-1		ICP		U73 (74H10)	7
008		001	0001		8001800048-1		ICP		U74 (74H20)	8
009		001	0001		8001800054-1		ICP		U66 (74H51)	9
010		001	0001		8001803200-1		ICP		U67 (74S04)	10
011		001	0001		8001800117-1		ICP		U62 (74150)	11
012		009	0001		8001803165-1		ICP		U7,8,17,18,27, 28,37,38,52 (74153)	12
013		012	0001		8001803178-1		ICP		U3,4,5,13,14,15, 23,24,25,33,34, 35 (74170)	13
014		005	0001		8001803181-1		ICP		U6,16,26,36,69 (74175)	14
		002	0001		8001803195-1		ICP		U51,61 (74198)	15
016		001	0001		8001803121-1		ICP		U46 (74H74)	16
017		001	0001		8001803204-1		ICP		U19 (74S15)	17
018		001	0001		8001803208-1		ICP		U65 (74S64)	18
019		001	0001		8001803212-1		ICP		U71 (74S112)	19
020		002	0001		N74H08N	18324	ICP	SIGNETICS	U55,77	20
021		000	0001		MC3001P	04713	ICP	MOTOROLA	U55,77	20A
021		001	0001		8001803211-1		ICP		U76 (74S86)	21
022		004	0001		8001803183-1		ICP		U1,11,21,31 (74181)	22
023		001	0001		8001803184-1		ICP		U41 (74182)	23
024		001	0001		N8242A	18324	ICP	SIGNETICS	U9	24
025		009	0001		8001800120-1		ICP		U10,20,29,30,40, 50,60,70,80 (BDR)	25
026		002	0001		8001803180-1		ICP		U59,79 (74174)	26
027		018	0001		RL07S471G		RESISTOR	MIL-R-22684/1	R3,4,5,6,R8 THRU R20,R22 .5 IS	27
028		003	0001		RL07S152G		RESISTOR	MIL-R-22684/1	R1,7,23 .5 IS	28
029		002	0001		RL07S361G		RESISTOR	MIL-R-22684/1	R21,2 .5 IS	29
030		000								30
031		003	0001		CM05ED750J03		CAPACITOR	MIL-C-5/18	C26,27,29 .25 IS	31

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL NOTE(S) REF DESIGNATION(S)	FIND NO.
032		002	0001		8001300311-2		CAPACITOR		C23,24 .8 IS	32
033		022	0001		8001300101-1		CAPACITOR		C1 THRU C22 .25 IS	33
034		001	0001		1001005395-1		SHIELD		NOTE 213	34
035		REF	0001		LD2001002161-1		LOGIC DIAGRAM			35
036		A/R	0001		SN60/SN63		SOLDER	QQ-S-571		36
037		022	0001		1005000764-1		PIN, TERMINAL		NOTE 210	37
038		003	0001		22AWG WHT		TUBING (TEFLON)	MIL-I-22129	APPROX INCH REQD	38
039		001	0001		CM05FD151J03		CAPACITOR	MIL-C-5/18	C28 .25 IS	39
040		A/R	0001		RTV 3140	71984	RTV COATING	DOW CORNING	NOTE 211	40
041		048	0001		9003400417-10		WIRE, INSULATED		30AWG WHT APPROX INCH REQD	41
042		000								42
043		000								43
					SPEC/DWG/STD		NOTES:			200
					LECP1049-17		MARKING (IDENTIFY).			201
							AREA TO BE FREE OF SOLDER			202
							TOTAL WARP AND TWIST SHALL NOT EXCEED .010/INCH IN GENERAL AREA AND .005/INCH IN CONNECTOR AREA.			203
							COMPONENTS NOT CALLED OUT BY THEIR FIND NUMBER ON FACE OF DRAWING ARE IDENTIFIED BY THEIR REFERENCE DESIGNATIONS.			204
							MAXIMUM COMPONENT HEIGHT (SIDE 1) .395 MAXIMUM.			205
							PROTRUSION (SIDE 2) .075 MAXIMUM.			206
										207
							MAXIMUM COMPONENT CONFIGURATION DEPICTED ON FACE OF DRAWING. FOR ACTUAL USAGE SEE APPLICABLE PARTS LIST.			208
							SQUARE PAD AND/OR DOT DENOTES PIN 1 OF ICP.			209
							TRIANGLE SYMBOL DENOTES TERMINAL PIN LOCATION.			210
							SPOT BOND JUMPER WIRES FIND NUMBER 41 USING FIND NUMBER 40.			211
							INTERCONNECT WIRING			212
							FROM / TO / REMARKS			
							E1 / E8 / FIND NO. 41			
							E3 / E5 / FIND NO. 41			
							E6 / E2 / FIND NO. 41			
							E7 / E4 / FIND NO. 41			
							E9 / E10 / FIND NO. 41			
							E11 / E12 / FIND NO. 41			
							E13 / E14 / FIND NO. 41			
							E15 / E16 / FIND NO. 41			
							E17 / E18 / FIND NO. 41			
							INSTALL SHIELD (FIND NUMBER 34) AFTER FLOW SOLDER OPERATION.			213

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002169-5		CPB-CKT CARD ASSY		USED ON SUE 1110A-1, 1110A-2	1
002		001	0001		1001004809-5		PRINTED WRG BD, CPB		NOTE 211	2
003		004	0001		8001800042-1		ICP		U59, 73, 79, 80 (74H00)	3
004		001	0001		8001800043-1		ICP		U20 (74H01)	4
005		002	0001		8001800044-1		ICP		U57, 83 (74H04)	5
006		006	0001		8001800046-1		ICP		U16, 17, 56, 63, 67, 70 (74H10)	6
007		001	0001		8001800047-1		ICP		U18 (74H11)	7
008		002	0001		8001800048-1		ICP		U68, 77 (74H20)	8
009		001	0001		8001800049-1		ICP		U6 (74H21)	9
010		001	0001		8001800054-1		ICP		U31 (74H51)	10
011		001	0001		8001800058-1		ICP		U66 (74H55)	11
012		000								12
013		001	0001		8001800117-1		ICP		U41 (74150)	13
014		002	0001		8001800118-1		ICP		U47, 48 (74151)	14
015		002	0001		8001803165-1		ICP		U2, 4 (74153)	15
016		000								16
017		003	0001		8001803173-1		ICP		U3, 43, 44 (74163)	17
018		005	0001		8001803180-1		ICP		U1, 5, 34, 37, 40 (74174)	18
019		005	0001		8001803181-1		ICP		U33, 35, 38, 39, 53 (74175)	19
020		001	0001		8001803121-1		ICP		U52 (74H74)	20
021		004	0001		8001803198-1		ICP		U51, 62, 74, 81 (74S00)	21
022		003	0001		8001803200-1		ICP		U50, 58, 72 (74S04)	22
023		004	0001		8001803202-1		ICP		U19, 45, 64, 75 (74S10)	23
024		004	0001		8001803203-1		ICP		U7, 65, 78, 82 (74S11)	24
025		001	0001		8001803208-1		ICP		U55 (74S64)	25
026		004	0001		8001803212-1		ICP		U61, 69, 71, 76 (74S112)	26
027		001	0001		74R00MP	07933	ICP	RAYTHEON	U9 (74R00)	27
028		000	0001		8001803198-1		ICP		U9 (74S00)	27a
029		001	0001		MC3001P	04713	ICP	MOTOROLA	U8	28
030		001	0001		MC3002P	04713	ICP	MOTOROLA	U46	29
031		001	0001		8001803137-1		ICP		U10 (7432)	30
032		001	0001		8001803218-1		ICP		U32 (74S138)	31
033		001	0001		N8264N	18324	ICP	SIGNETICS	U15	32
034		003	0001		N8235B	18324	ICP	SIGNETICS	U11, 14, 21	33

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
035		001	0001		SN75452P	01295	ICP	TEXAS INSTR INC	U60	34
036		002	0001		AS-143-U-3	06776	SOCKET	ROBINSON NUGENT	NOTE 213	35
037		002	0001		8001800120-1		ICP		U49,54 (BDR)	36
038		001	0001		74R174MP	07933	ICP	RAYTHEON	U36 (174MP)	37
039		000	0001		8001803180-1		ICP		U36 (74174)	37a
040		002	0001		NO.4416X3/4	26066	TAPE	3M CO	.75 X .70 LONG APPROX INCH REQD NOTE 213	38
041		001	0001		RL07S102G		RESISTOR	MIL-R-22684/1	R9 .5 IS	39
042		001	0001		RL20S511G		RESISTOR	MIL-R-22684/2	R8 .6 IS	40
043		001	0001		RL07S121G		RESISTOR	MIL-R-22684/1	R7 .5 IS	41
044		002	0001		RL07S680G		RESISTOR	MIL-R-22684/1	R1,2 .5 IS	42
045		004	0001		RL07S102G		RESISTOR	MIL-R-22684/1	R3,4,5,6 .5 IS	43
046		002	0001		CM04FD101J03		CAPACITOR	MIL-C-5/18	C25,57 .25 IS	44
047		001	0001		8001200001-1		TRANSISTOR		Q1	45
048		02	0001		8001600008-1		DELAY LINE, FIXED		DL1,DL2	46
049		001	0001		8001600007-1		DELAY LINE, TAPPED		DL3	47
050		047	0001		8001300101-1		CAPACITOR		C1 THRU C13, C15 THRU C24, C26,27,29,30,31, C33 THRU C36, C38 THRU C52 .25 IS	48
051		003	0001		8001300311-2		CAPACITOR		C28,32,37 .8 IS	49
052		002	0001		8001300333-2		CAPACITOR		C14,53 .8 IS	50
053		021	0001		1005000764-1		PIN, TERMINAL		NOTE 210	51
054		000								52
055		001	0001		1005000796-41		READ ONLY MEMORY		U28	53
056		001	0001		1005000796-42		READ ONLY MEMORY		U23	54
057		001	0001		1005000796-43		READ ONLY MEMORY		U24	55
058		001	0001		1005000796-44		READ ONLY MEMORY		U22	56
059		001	0001		1005000796-45		READ ONLY MEMORY		U26	57
060		001	0001		1005000796-46		READ ONLY MEMORY		U25	58
061		001	0001		1005000796-47		READ ONLY MEMORY		U27	59
062		001	0001		1005000796-48		READ ONLY MEMORY		U30	60
063		001	0001		1005000796-49		READ ONLY MEMORY		U29	61
064		001	0001		1005000796-26		READ ONLY MEMORY		U12	62
065		001	0001		1005000796-27		READ ONLY MEMORY		U13	63
066		009	0001		1001004974-1		RESISTOR CLUSTER		A1 THRU A9	64
067		A/R	0001		SN60/SN63		SOLDER	QQ-S-571		65
068		REF	0001		LD2001002169-1		LOGIC DIAGRAM			66
069		000								67
070		004	0001		9003400417-10		WIRE, INSULATED		30AWG WHT APPROX FT REQD	68
071		002	0001		CM05ED750J03		CAPACITOR	MIL-C-5/18	C54,55 .25 IS	69
072		A/R	0001		RTV 3140	71984	RTV COATING	DOW CORNING	NOTE 215	70
073		002	0001		CM05FD391J03-		CAPACITOR	MIL-C-5/18	C56,58 .25 IS	71
074		001	0001		RL07S151G		RESISTOR	MIL-R-22684/1	R10	72

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002169-6		CPB-CKT CARD ASSY		USED ON SUE 1111A-1, 1111A-2	1
002		001	0001		1001004809-5		PRINTED WRG BD, CPB		NOTE 211	2
003		004	0001		8001800042-1		ICP		U59, 73, 79, 80 (74H00)	3
004		001	0001		8001800043-1		ICP		U20 (74H01)	4
005		002	0001		8001800044-1		ICP		U57, 83 (74H04)	5
006		006	0001		8001800046-1		ICP		U16, 17, 56, 63, 67, 70 (74H10)	6
007		001	0001		8001800047-1		ICP		U18 (74H11)	7
008		002	0001		8001800048-1		ICP		U68, 77 (74H20)	8
009		001	0001		8001800049-1		ICP		U6 (74H21)	9
010		001	0001		8001800054-1		ICP		U31 (74H51)	10
011		001	0001		8001800058-1		ICP		U66 (74H55)	11
012		000								12
013		001	0001		8001800117-1		ICP		U41 (74150)	13
014		002	0001		8001800118-1		ICP		U47, 48 (74151)	14
015		002	0001		8001803165-1		ICP		U2, 4 (74153)	15
016		000								16
017		004	0001		8001803173-1		ICP		U3, 42, 43, 44 (74163)	17
018		005	0001		8001803180-1		ICP		U1, 5, 34, 37, 40 (74174)	18
019		005	0001		8001803181-1		ICP		U33, 35, 38, 39, 53 (74175)	19
020		001	0001		8001803121-1		ICP		U52 (74H74)	20
021		004	0001		8001803198-1		ICP		U51, 62, 74, 81 (74S00)	21
022		003	0001		8001803200-1		ICP		U50, 58, 72 (74S04)	22
023		004	0001		8001803202-1		ICP		U19, 45, 64, 75 (74S10)	23
024		004	0001		8001803203-1		ICP		U7, 65, 78, 82 (74S11)	24
025		001	0001		8001803208-1		ICP		U55 (74S64)	25
026		004	0001		8001803212-1		ICP		U61, 69, 71, 76 (74S112)	26
027		001	0001		74R00MP	07933	ICP	RAYTHEON	U9 (74R00)	27
028		000	0001		8001803198-1		ICP		U9 (74S00)	27a
029		001	0001		MC3001P	04713	ICP	MOTOROLA	U8	28
030		001	0001		MC3002P	04713	ICP	MOTOROLA	U46	29
031		001	0001		8001803137-1		ICP		U10 (7432)	30
032		001	0001		8001803218-1		ICP		U32 (74S138)	31
033		001	0001		N8264N	18324	ICP	SIGNETICS	U15	32
034		003	0001		N8235B	18324	ICP	SIGNETICS	U11, 14, 21	33

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
035		001	0001		SN75452P	01295	ICP	TEXAS INSTR INC	U60	34
036		003	0001		AS-143-U-3	06776	SOCKET	ROBINSON NUGENT	NOTE 213	35
037		002	0001		8001800120-1		ICP		U49,54 (BDR)	36
038		001	0001		74R174MP	07933	ICP	RAYTHEON	U36 (174MP)	37
039		000	0001		8001803180-1		ICP		U36 (74174)	37a
040		003	0001		NO.4416X3/4	26066	TAPE	3M CO	.75 X .70 LONG APPROX INCH REQD NOTE 213	38
041		001	0001		RL07S102G		RESISTOR	MIL-R-22684/1	R9 .5 IS	39
042		001	0001		RL20S511G		RESISTOR	MIL-R-22684/2	R8 .6 IS	40
043		001	0001		RL07S121G		RESISTOR	MIL-R-22684/1	R7 .5 IS	41
044		002	0001		RL07S680G		RESISTOR	MIL-R-22684/1	R1,2 .5 IS	42
045		004	0001		RL07S102G		RESISTOR	MIL-R-22684/1	R3,4,5,6 .5 IS	43
046		002	0001		CM04FD101J03		CAPACITOR	MIL-C-5/18	C25,57 .25 IS	44
047		001	0001		8001200001-1		TRANSISTOR		Q1	45
048		002	0001		8001600008-1		DELAY LINE, FIXED		DL1,DL2	46
049		001	0001		8001600007-1		DELAY LINE, TAPPED		DL3	47
050		047	0001		8001300101-1		CAPACITOR		C1 THRU C13, C15 THRU C24, C26,27,29,30,31, C33 THRU C36, C38 THRU C52 .25 IS	48
051		003	0001		8001300311-2		CAPACITOR		C28,32,37 .8 IS	49
052		002	0001		8001300333-2		CAPACITOR		C14,53 .8 IS	50
053		021	0001		1005000764-1		PIN, TERMINAL		NOTE 210	51
054		000								52
055		001	0001		1005000856-31		READ ONLY MEMORY		U28	53
056		001	0001		1005000856-32		READ ONLY MEMORY		U23	54
057		001	0001		1005000856-33		READ ONLY MEMORY		U24	55
058		001	0001		1005000856-34		READ ONLY MEMORY		U22	56
059		001	0001		1005000856-35		READ ONLY MEMORY		U26	57
060		001	0001		1005000856-36		READ ONLY MEMORY		U25	58
061		001	0001		1005000856-37		READ ONLY MEMORY		U27	59
062		001	0001		1005000856-38		READ ONLY MEMORY		U30	60
063		001	0001		1005000856-39		READ ONLY MEMORY		U29	61
064		001	0001		1005000796-26		READ ONLY MEMORY		U12	62
065		001	0001		1005000796-27		READ ONLY MEMORY		U13	63
066		009	0001		1001004974-1		RESISTOR CLUSTER		A1 THRU A9	64
067		A/R	0001		SN60/SN63		SOLDER	QQ-S-571		65
068		REF	0001		LD2001002169-1		LOGIC DIAGRAM			66
069		000								67
070		004	0001		9003400417-10		WIRE, INSULATED		30AWG WHT APPROX FT REQD	68
071		002	0001		CM05ED750J03		CAPACITOR	MIL-C-5/18	C54,55 .25 IS	69
072		A/R	0001		RTV 3140	71984	RTV COATING	DOW CORNING	NOTE 215	70
073		002	0001		CM05FD391J03		CAPACITOR	MIL-C-5/18	C56,58 .25 IS	71
074		001	0001		RL07S151G		RESISTOR	MIL-R-22684/1	R10	72

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002169-8		CPB-CKT CARD ASSY		USED ON SUE 1112A-1,1112A-2	1
002		001	0001		1001004809-5		PRINTED WRG BD, CPB		NOTE 211	2
003		004	0001		8001800042-1		ICP		U59,73,79,80 (74H00)	3
004		001	0001		8001800043-1		ICP		U20 (74H01)	4
005		002	0001		8001800044-1		ICP		U57,83 (74H04)	5
006		006	0001		8001800046-1		ICP		U16,17,56,63,67, 70 (74H10)	6
007		001	0001		8001800047-1		ICP		U18 (74H11)	7
008		002	0001		8001800048-1		ICP		U68,77 (74H20)	8
009		001	0001		8001800049-1		ICP		U6 (74H21)	9
010		001	0001		8001800054-1		ICP		U31 (74H51)	10
011		001	0001		8001800058-1		ICP		U66 (74H55)	11
012		000								12
013		001	0001		8001800117-1		ICP		U41 (74150)	13
014		002	0001		8001800118-1		ICP		U47,48 (74151)	14
015		002	0001		8001803165-1		ICP		U2,4 (74153)	15
016		000								16
017		004	0001		8001803173-1		ICP		U3,42,43,44 (74163)	17
018		005	0001		8001803180-1		ICP		U1,5,34,37,40 (74174)	18
019		005	0001		8001803181-1		ICP		U33,35,38,39,53 (74175)	19
020		001	0001		8001803121-1		ICP		U52 (74H74)	20
021		004	0001		8001803198-1		ICP		U51,62,74,81 (74S00)	21
022		003	0001		8001803200-1		ICP		U50,58,72(74S04)	22
023		004	0001		8001803202-1		ICP		U19,45,64,75 (74S10)	23
024		004	0001		8001803203-1		ICP		U7,65,78,82 (74S11)	24
025		001	0001		8001803208-1		ICP		U55 (74S64)	25
026		004	0001		8001803212-1		ICP		U61,69,71,76 (74S112)	26
027		001	0001		74R00MP	07933	ICP	RAYTHEON	U9 (74R00)	27
028		000	0001		8001803198-1		ICP		U9 (74S00)	27a
029		001	0001		MC3001P	04713	ICP	MOTOROLA	U8	28
030		001	0001		MC3002P	04713	ICP	MOTOROLA	U46	29
031		001	0001		8001803137-1		ICP		U10 (7432)	30
032		001	0001		8001803218-1		ICP		U32 (74S138)	31
033		001	0001		N8264N	18324	ICP	SIGNETICS	U15	32
034		003	0001		N8235B	18324	ICP	SIGNETICS	U11,14,21	33

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
035		001	0001		SN75452P	01295	ICP	TEXAS INSTR INC	U60	34
036		003	0001		AS-143-U-3	06776	SOCKET	ROBINSON NUGENT	NOTE 213	35
037		002	0001		8001800120-1		ICP		U49,54 (BDR)	36
038		001	0001		74R174MP	07933	ICP	RAYTHEON	U36 (174MP)	37
039		000	0001		8001803180-1		ICP		U36 (74174)	37a
040		003	0001		NO.4416X3/4	26066	TAPE	3M CO	.75 X .70 LONG APPROX INCH REQD NOTE 213	38
041		001	0001		RL07S102G		RESISTOR	MIL-R-22684/1	R9 .5 IS	39
042		001	0001		RL20S511G		RESISTOR	MIL-R-22684/2	R8 .6 IS	40
043		001	0001		RL07S121G		RESISTOR	MIL-R-22684/1	R7 .5 IS	41
044		002	0001		RL07S680G		RESISTOR	MIL-R-22684/1	R1,2 .5 IS	42
045		004	0001		RL07S102G		RESISTOR	MIL-R-22684/1	R3,4,5,6 .5 IS	43
046		002	0001		CM04FD101J03		CAPACITOR	MIL-C-5/18	C25,57 .25 IS	44
047		001	0001		8001200001-1		TRANSISTOR		Q1	45
048		002	0001		8001600008-1		DELAY LINE, FIXED		DL1,DL2	46
049		001	0001		8001600007-1		DELAY LINE, TAPPED		DL3	47
050		047	0001		8001300101-1		CAPACITOR		C1 THRU C13, C15 THRU C24, C26,27,29,30,31, C33 THRU C36, C38 THRU C52 .25 IS	48
051		003	0001		8001300311-2		CAPACITOR		C28,32,37 .8 IS	49
052		002	0001		8001300333-2		CAPACITOR		C14,53 .8 IS	50
053		021	0001		1005000764-1		PIN, TERMINAL		NOTE 210	51
054		000								52
055		001	0001		1005000856-41		READ ONLY MEMORY		U28	53
056		001	0001		1005000856-42		READ ONLY MEMORY		U23	54
057		001	0001		1005000856-43		READ ONLY MEMORY		U24	55
058		001	0001		1005000856-44		READ ONLY MEMORY		U22	56
059		001	0001		1005000856-45		READ ONLY MEMORY		U26	57
060		001	0001		1005000856-46		READ ONLY MEMORY		U25	58
061		001	0001		1005000856-47		READ ONLY MEMORY		U27	59
062		001	0001		1005000856-48		READ ONLY MEMORY		U30	60
063		001	0001		1005000856-49		READ ONLY MEMORY		U29	61
064		001	0001		1005000796-39		READ ONLY MEMORY		U12	62
065		001	0001		1005000796-40		READ ONLY MEMORY		U13	63
066		009	0001		1001004974-1		RESISTOR CLUSTER		A1 THRU A9	64
067		A/R	0001		SN60/SN63		SOLDER	QQ-S-571		65
068		REF	0001		LD2001002169-1		LOGIC DIAGRAM			66
069		000								67
070		004	0001		9003400417-10		WIRE, INSULATED		30AWG WHT APPROX FT REQD	68
071		002	0001		CM05ED750J03		CAPACITOR	MIL-C-5/18	C54,55 .25 IS	69
072		A/R	0001		RTV 3140	71984	RTV COATING	DOW CORNING	NOTE 215	70
073		002	0001		CM05FD391J03		CAPACITOR	MIL-C-5/18	C56,58 .25 IS	71
074		001	0001		RL07S151G		RESISTOR	MIL-R-22684/1	R10	72

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
200		REF	0001		SPEC/DWG/STD		NOTES:			200
201		A/R	0001		LECP1049-17		MARK PART NUMBER 2001002169-1.			201
202		REF	0001				AREA TO BE FREE OF SOLDER.			202
203		REF	0001				TOTAL WARP AND TWIST SHALL NOT EXCEED .010/INCH IN GENERAL AREA AND .005/INCH IN CONNECTOR AREA.			203
204		REF	0001				COMPONENTS NOT CALLED OUT BY THEIR FIND NUMBER ON FACE OF DRAWING ARE IDENTIFIED BY THEIR REFERENCE DESIGNATIONS.			204
205		REF	0001				MAXIMUM COMPONENT HEIGHT (SIDE 1) .395 MAXIMUM.			205
206		REF	0001				PROTRUSION (SIDE 2) .075 MAXIMUM.			206
207		000								207
208		REF	0001				MAXIMUM COMPONENT CONFIGURATION DEPICTED ON FACE OF DRAWING. FOR ACTUAL USAGE SEE APPLICABLE PARTS LIST.			208
209		REF	0001				SQUARE PAD AND/OR DOT DENOTES PIN 1 OF ICP.			209
210		REF	0001				TRIANGLE SYMBOL DENOTES TERMINAL PIN INSTALLATION.			210
211		REF	0001				FOR ASSEMBLIES -5 AND -9 ADD JUMPER (FIND NO.58) FROM J2A1 TO J2A2 AND FROM J2B1 TO J2B2.			211
212		000								212
213		REF	0001				TAPE DOWN SOCKET FIND NUMBER 35 TO FIND NUMBER 2 USING FIND NUMBER 38 AND FIND NUMBER 70.			213
214		REF	0001				"X" DENOTES ICP LEAD TO BE BENT TO HORIZONTAL POSITION. PRECAUTION SHOULD BE TAKEN NOT TO BREAK OR CRACK LEADS.			214
215		REF	0001				SPOT BOND JUMPER WIRE (FIND NUMBER 68) USING FIND NUMBER 70 TO FIND NUMBER 2.			215
216		REF	0001				CONTINUED ON NEXT PAGE.			216

SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
216						WIRE LIST (215).			216
						REMARKS	FROM	TO	FIND NO.
							U60-2	U60-1	68
							U60-1	U65-11	
							U82-3	U82-4	
							U82-4	U53-1	
							E6	U82-5	
							U82-5	U53-15	
							U82-6	E15	
							E13	E10	
						(214)	U67-11	E11	
							E11	E14	
							E14	U82-2	
							U82-2	U82-1	
							E9	E8	
							E7	U66-13	
						(214)	U66-2	U66-1	
						(214)	U64-9	U82-12	
							U82-13	U73-8	
						(214)	U65-5	U65-4	
							U77-9	U77-7	
							E2	U83-2	
							E3	U83-1	
							U82-11	U50-10	
							U82-8	U45-2	
							U82-10	U82-9	
							U82-9	U69-6	
						(214)	U67-4	E4	
							U47-3	U57-10	
							U47-2	U57-11	
						(214)	U57-11	U76-2	
						(214)	U76-2	E1	
						(214)	U75-9	U75-10	
							U60-3	R2, R10	
							U83-7	U82-7	
							U82-7	E12	
							U83-14	U82-14	
							U83-14	E16	
							U80-2	U70-5	
							U80-1	U78-9	
							U68-1	U78-10	
							U40-9	E17	
							U40-12	E18	68