Publication Number 29-280R01

M80-000 and M80-001
MODEL 80
MAINTENANCE MANUAL

Consists Of:

GENERAL DESCRIPTION		
	General Description	29-280A12
PROCESSOR		
	Processor Installation Specification	01-053A20
	Processor Maintenance Specification	01-053R01A21
MEMORY		
	Memory Maintenance Specification	02-247A21
MEMORY PROTECT		
	Memory Protect Controller Programming Specification	02-248A22
	Memory Protect Controller Installation Specification	02-248A20
	Memory Protect Controller Maintenance Specification	02-248A21
SELECTOR CHANNEL		
	Selector Channel Installation Specification	02-232M01A20
	Selector Channel Maintenance Specification	02-232M01A21
POWER SYSTEM		
	Power System Description	02-261A12
DRAWINGS		
	Model 80 Processor (Reference)	01-053D08
	Cable Information	01-051R03C12
	Central Processing Unit Schematic	35-403R12D08
	Arithmetic Logic Unit Schematic	35-404R06D08
	Input/Output Unit Schematic	35-405R09D08
	Input/Output Unit Locator	35-405R05C12
	Input/Output Unit Locator (M01)	35-405M01D12
	Selector Channel Schematic	02-232M01D08
	Memory Bank Controller Schematic	35-407R07D08
	Memory Storage Unit Schematic	02-247R09D08
	Memory Protect Schematic	02-248R01D08
	Memory Protect Locator	35-408R01D03
	Model 80 Memory Power Supply Schematic	34-014R03D08
	50 Ampere Power Supply Schematic	34-015R02D08
	Power Supply Installation Information	02-261C12
	External Battery Information	39-019C20
	Display Panel Schematic	09-051R07D08

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(1893, 1905)
(1781)
(1918, 1919, 1964)
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(2028, 2047) (2060)

SUPPLEMENT TO MODEL 80 MAINTENANCE MANUAL

Publication Number 29-280R01

Publication Number 29-280R03 consists of a 29-280R01 Manual and this Supplement.

In General Description 29-280A12, Appendix 1, add:

NOTE

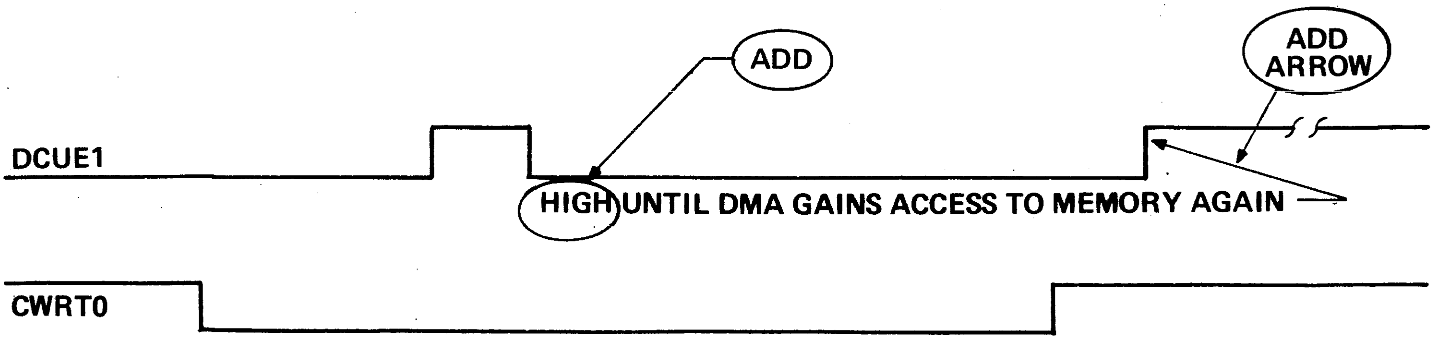
This is a comprehensive list of parts used in INTERDATA equipment. All parts are not used in every system. These parts may or may not be in your particular Processor.

In 01-053R01A21, Sheet 34, Change "AS011" to "AS001".

On Sheet 35, fourth line from top should read:

"IF (AWRT0 AZR01 RZR01) B00:15→0, A00:15→0

In 02-247A21, Sheet 22, Change:


ADD
ADD ARROW
DCUE1
HIGH UNTIL DMA GAINS ACCESS TO MEMORY AGAIN
CWRT0

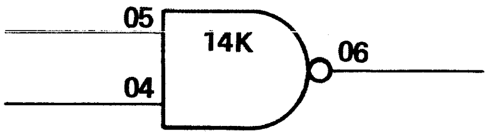
In 02-247A21, Sheet 39, Paragraph 17.1:

Voltage Adjustments should be:

	P15	P22	P5	P5S
1.	15.3*	21.0	5.10	5.10
2.	15.5*	21.0	5.10	5.10
3.	15.4	19.5*	5.10	5.10
4.	15.4	22.5*	5.10	5.10
5.	15.4	21.0	4.85*	5.10
6.	15.4	21.0	5.35*	5.10
7.	15.4	21.0	5.10	4.85*
8.	15.4	21.0	5.10	5.35*
Normal	15.4	21.0	5.10	5.10

In 35-403R10D08, Sheet 1, Area FG1, Change Mnemonics TREPO to TWDTHO and TWDTHO to TREPO.

Sheet 3, Area M2 on 14K: Add Pin 6 designation:



In 35-404R06D08, Sheet 7, Area L4 and 5, Change Mnemonics TREPO to TWDTHO and TWDTHO to TREPO.

Add ACU Component Locator, Sheets 10 and 11 of 35-404D08 and CPU Component Locator, Sheets 11 and 12 of 35-403D08 to manual.

In 02-247A21, Sheet 34, Figure 19: Delete numbers on the four lines between (A)(B) Chip Select Drivers and (A)(B) Half MOS Chip Array.

In 02-247A21, Sheet 39, Paragraph 19.1, in the first and third lines and in Figure 23 title, change 11-127 to 28-015.

Replace Functional Schematic 02-247R09D08 by 02-247R10D08.

In Functional Schematic 34-014R03D08, Sheet 1, change R135 from 7.5K to 12.7K.

Replace Functional Schematic 35-407R07D08 by 35-407R12D08

On Functional Schematic 09-051R07D08: Sheet 1, Area C5: Change SWITCH SW21 PIN DESIGNATIONS as follows:

SW21-03 to	SW21-1W
07	05W
11	09W
00	01
02	03
SW21-04 to	SW21-05
05	06
06	07
08	09
09	10
10	11

Show unused terminals, 04, 08, 12

On Functional Schematic 09-051R07D08, Sheet 1, Area BC8, remove two gates labeled "NOT USED"

On Functional Schematic 02-247R09D08 change the "M01" notation to read "M01 and M02" in the following eight places:

Sheet 1 Area H9, Area A5, Area C5
Sheet 3 Area L5, Area M7
Sheet 4 Area A1
Sheet 5 Area A1
Sheet 7 Area 9F

On Functional Schematic 35-403R12D08 Sheet 3 Area JK1, replace 07J part number with:

NOTE 1
M80 CPU - 07J is 19-047F70
M60 CPU - 07J is 19-084F66

On Functional Schematic 35-404D08 Sheet 0, Area J8, in P. C. Board latest revision box add the notation:

35-404M01

On Functional Schematic 35-404D08, Sheet 9, remove "F" vari numbers from all units on this sheet.
Add 'see table' note above IC 18D and table below:

Add Installation Specification 02-261A20 to manual.

Add Kit Information 39-021C12 to manual.

POS	VARIATION OF 19-084 USED MOD 80	MOD 60
18A	F01	F34
17A	F02	F35
16A	F03	F36
15A	F04	F37
14A	F05	F38
21A	F06	F39
20A	F07	F40
19A	F08	F41
18B	F09	F42
17B	F10	F43
16B	F11	F44
15B	F12	F45
14B	F13	F46
21B	F14	F47
20B	F15	F48
19B	F16	F49
18C	F17	F50
17C	F18	F51
16C	F19	F52
15C	F20	F53
14C	F21	F54
21C	F22	F55
20C	F23	F56
19C	F24	F57
18D	F25	F58
17D	F26	F59
16D	F27	F60
15D	F28	F61
14D	F29	F62
21D	F30	F63
20D	F31	F64
19D	F32	F65

On Functional Schematic 35-405D08,Sheet 6, Area M8, add 'see Note 2' above 00E. Add Note 2

Connect 00E - 13 to 'B151' - Model 80
Connect 00E - 11 to X5 (108-3) Model 60

NOTE

DO NOT USE I/O DEVICE NUMBER X'05' IN YOUR SYSTEM FOR ANYTHING OTHER THAN A LOADER STORAGE UNIT CONTROLLER. DEVICE NUMBER X'05' IS RESERVED FOR THE LSU CONTROLLER, A DEVICE WHICH IS TREATED SPECIALLY BY THE HARDWARE ON POWER-UP OR INITIALIZE SEQUENCES, WHICH AUTOMATICALLY LOADS A NEW PSW AND UP TO 2048 BYTES OF MAIN MEMORY. THE HARDWARE ASSUMES IF DEVICE NUMBER X'05' EXISTS IN A SYSTEM THAT IT IS AN LSU AND THE AUTOMATIC PSW AND MEMORY LOAD SEQUENCE OCCUR ON POWER UP. ACCORDINGLY, EXTRAORDINARY RESULTS CAN OCCUR IF DEVICE NUMBER '05' IS ASSIGNED TO ANY OTHER DEVICE CONTROLLER.

QUICK REFERENCE INDEX

To aid in quickly locating a particular section, the index marks on the edge of this page are aligned with similar marks at the beginning of each section.

GENERAL DESCRIPTION

PROCESSOR

MEMORY

MEMORY PROTECT

SELECTOR CHANNEL

POWER SYSTEM

DRAWINGS

GENERAL DESCRIPTION

MODEL 80 GENERAL DESCRIPTION

Contents

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2. SCOPE 1
3. BLOCK DIAGRAM 2
4. DOCUMENTATION 2
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    4.2 Part Numbering System 3
    4.3 Drawing System 5

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Figure 3. Example of a Schottky Buffer 6
Figure 4. Example of a Logic Board Layout 6
Figure 5. Connector Pin Numbering 7
Figure 6. Functional Schematic Format Drawing 9

MODEL 80
GENERAL DESCRIPTION

The Model 80 combines advanced circuitry and packaging designs to give the user a price/performance optimized machine. The Model 80 is completely upward compatible with INTERDATA Model 3, 4, 5 and 70 Processor user instructions, interrupt handling, input/output formats and control sequencing. Because of this compatability, the Model 80 can use the wide range of existing software and peripheral devices.

The Model 80 offers a comprehensive set of 113 instructions making the system both easy to program and efficient to operate. Through multi-function instructions and direct addressing, coding and debugging time is reduced to a minimum.

Memory is addressable to the eight-bit byte level. Memory is expandable from the basic 16,384 bytes to 65,536 bytes. All memory is directly addressable with the primary instructions, no paging or indirect addressing is required. Of the 16 (16-bit) General Registers used as Accumulators, 15 can also be used as Index Registers. Register-to-Register instructions permit operations between any of the 16 General Registers, eliminating redundant loads and stores.

The Protect Mode of the Model 80 enables Memory Protect and detection of Privileged instructions, and can be activated under program control. This mode is invaluable in process control, data communication, and time-sharing operations to guarantee that a running program cannot interfere with the integrity of the system.

The Model 80 also provides a flexible Input/Output system in addition to conventional means of programmed I/O. In the Automatic I/O Service Mode, the Processor acknowledges all I/O interrupts and automatically performs much of the overhead prior to activating the Interrupt Service Routine. In conjunction with the Automatic I/O Service, an I/O Channel can perform data transfers and signal counting without interrupting the running program until the specified sequence is completed.

Up to four Direct Memory Access Channels (DMAC) can be added to a Model 80 Memory System. These channels operate over a private Memory Bus through a Direct Memory Access Port which is built into the Memory Controller. Two types of Direct Memory Access Channels can be used with the Model 80 System: The Selector Channel, which permits direct data transfer between any standard oriented INTERDATA device controller and memory; and the Direct Memory Access Channel custom designed by the user for special applications.

2. SCOPE

This specification is intended to enable the digital technician to understand the INTERDATA documentation system. Number Notation, the Part Numbering System, and the Drawing System are described. Illustrations are provided to help understand these systems. Other publications which may be of interest to Model 80 users are shown in Table 1.

A cross reference between INTERDATA part numbers and standard industry part numbers for the ICs and transistors is found in Appendix 1.

TABLE 1. RELATED PUBLICATIONS

Title	Publication Number
Universal Clock Instruction Manual	29-265
Users Handbook	29-261
Model 80 Maintenance Manual	29-280*
Multiplexor Bus Buffer Instruction Manual	29-267
8 Line Interrupt Module Instruction Manual	29-268

---

*This General Description is a part of 29-280.

3. BLOCK DIAGRAM

A Model 80 simplified block diagram is shown in Figure 1. The basic Model 80 is a 16-bit digital computer contained on 5 PC boards:

Part No.	Description	Card File Position
35-406	Memory Storage Unit	3
35-407	Memory Bank Controller	4
35-405	IOU Board	5
35-404	ALU Board	6
35-403	CPU Board	7

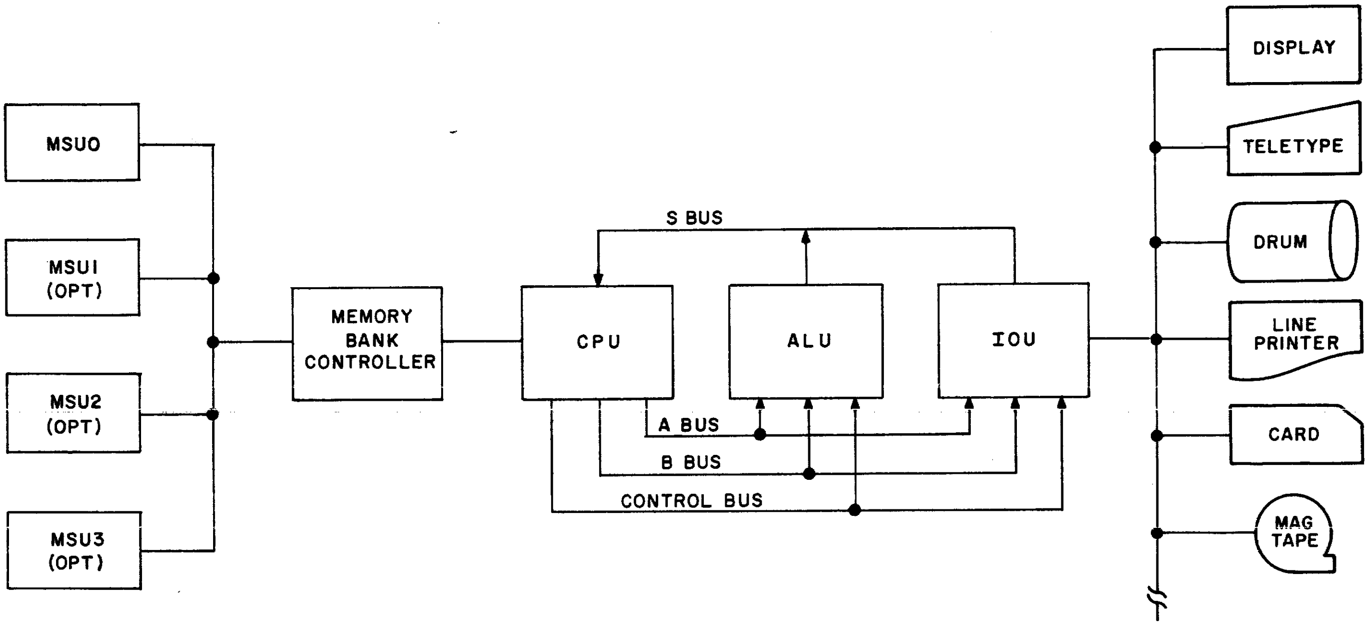

MSUO
MSUI (OPT)
MSU2 (OPT)
MSU3 (OPT)
MEMORY BANK CONTROLLER
S BUS
CPU
ALU
IOU
A BUS
B BUS
CONTROL BUS
DISPLAY
TELETYPE
DRUM
LINE PRINTER
CARD
MAG TAPE

Figure 1. Model 80 Simplified Block Diagram

4. DOCUMENTATION

This section describes the style and conventions used with INTERDATA documentation.

4.1 Number Notation

The most common form of number notation used in INTERDATA documentation is hexadecimal notation. In this system, groups of four binary digits are represented by a single hexadecimal digit. Table 2 lists the hexadecimal characters employed.

TABLE 2. HEXADECIMAL NOTATION DATA

Binary	Decimal	Hexadecimal	Binary	Decimal	Hexadecimal	Binary	Decimal	Hexadecimal
0000	0	0	0110	6	6	1100	12	C
0001	1	1	0111	7	7	1101	13	D
0010	2	2	1000	8	8	1110	14	E
0011	3	3	1001	9	9	1111	15	F
0100	4	4	1010	10	A			
0101	5	5	1011	11	B			

To differentiate between decimal and hexadecimal numbers, hexadecimal numbers are preceded by the letter "X", and the number is enclosed in single quotation marks. Examples of hexadecimal numbers are: X'1234', X'2EC6', X'A340, X'EEFA', and X'10B9'.

4.2 Part Numbering System

INTERDATA parts, drawings, and publications employ a common numbering system. The part number and drawing numbers for drawings which describe the part are related. The publication number is also often related to the part number of the device or program described. Figure 2 shows the format used for INTERDATA part numbers. The fields are described in the following paragraphs.

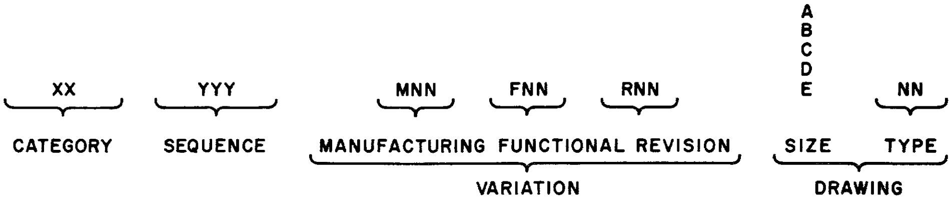


Figure 2. Part Number Format

4.2.1 Category Field. The two-digit Category number indicates the broad class or category to which a part belongs. Typical examples of category number assignments are:

01 - Basic Hardware Systems
02 - Basic Hardware Expansions
03 - Basic Software Systems
04 - Basic Software Packages
05 - Micro-Programs
06 - Test Programs
07 - Subroutines of General Utility
10 - Spare Parts Packages
12 - Card File Assemblies
13 - Panels
17 - Wire and Cables
19 - Integrated Circuits
20 - Transistors
27 - Peripheral Equipment
29 - Manuals
34 - Power Supplies
35 - Assembled Printed Circuit Boards
36 - Electro-Mechanical Devices

4.2.2 Sequence Field. The Sequence number identifies a particular item within the category. Sequence numbers are assigned serially, and have no other significance.

NOTE

The Sequence Field, like all other part number fields, may be lengthened as required. The field lengths shown on Figure 2 are minimum lengths (insignificant zeros must be added to maintain these minimums).

4.2.3 Manufacturing Variation Field. The optional Manufacturing Variation Field consists of the letter "M" followed by two digits.

NOTE

A part number must contain a Category number and a Sequence number. All other fields are optional.

The M Field is used to distinguish between parts which are electrically and mechanically equivalent (interchangeable), but which vary in method of manufacture. For example, if leads are welded instead of soldered on an assembly, the M Field changes.

An important exception to the meaning of the M Field exists for categories related to software. Here the M Field number, when used, indicates the form in which a particular program is presented. For example, define a program as a set of machine instructions. These same identical instructions may be presented on punched cards, paper tape, or magnetic tape; and for any of these they could be in symbolic form. Thus, there are many ways to represent the same identical program. These ways are identified by the M Field numbers as follows:

M01 - Symbolic Punched Cards
M02 - Relative Binary Punched Cards
M03 - Absolute Binary Punched Cards
M04 - Symbolic Magnetic Tape
M05 - Relative Binary Magnetic Tape
M06 - Absolute Binary Magnetic Tape
M07 - Symbolic Punched Paper Tape
M08 - Relative Binary Punched Paper Tape
M09 - Absolute Binary Punched Paper Tape
M10 - Bootstrap Binary Object Punched Paper Tape
M11 - Read-Only-Memory (ROM) Absolute Binary Object Punched Paper Tape
M12 - ROM Wiring and Test Set (ROMWATS) Wiring Punched Paper Tape
M13 - ROMWATS Check Punched Paper Tape
M14 - Eight-Bit Paper Tape
M15 - DROM Absolute Binary Object Punched Paper Tape
M16 - Relocatable Non-Zoned Loader Format Paper Tape
M17 - Absolute Non-Zoned Loader Format Paper Tape
M18 - Non-Zoned Established Task Object Tape

4.2.4 Functional Variation Field. The optional Functional Variation Field consists of the letter "F" followed by two digits. The F Field is used to distinguish between parts which are not necessarily electrically or mechanically equivalent, but which are described by the same set of drawings. For example, a power supply may be strapped internally to operate on either 110 VAC or 220 VAC. Except for this strap, all power supplies of this type are identical. Therefore, strapping option is easily described by a note on the assembly and test specification drawings.

4.2.5 Revision Field. The optional Revision Field consists of the letter "R" followed by two digits. The R Field is used to indicate minor electrical or mechanical changes to a part which do not change the part's original character. R Field changes often reflect improvements. A part with a revision level HIGHER than the one specified will work. A part with a revision level LOWER than specified should not be used.

4.2.6 Drawing Field. The optional Drawing Field consists of a letter from "A" to "E" followed by two digits. The letter indicates the size of the original drawing. The sizes for each letter are:

A - 8½" X 11"
B - 11" X 17"
C - 17" X 22"
D - 22" X 34"
E - 34" X 44"

The two digits indicate the drawing type as follows:

01 - Parts List
02 - Machine Details
03 - Assembly Details
05 - Art Details
06 - Wire Run List
08 - Schematic
09 - Test Specification
10 - Purchase Specification
11 - Bill of Material
12 - Information
13 - Program Listing
14 - Abstracts
15 - Program Description
16 - Operating Instructions
17 - Program Design Specification
18 - Flow Charts
19 - Product Specification
20 - Installation Specification
21 - Maintenance Specification
22 - Programming Specification

4.2.7 Examples. The following list provides some examples of the part numbering system. The numbers were arbitrarily selected, and in most cases are fictitious.

35-060	The 60th printed-circuit board assigned a part number under this system.
35-060M01	A printed circuit board electrically and mechanically interchangeable with the 35-060, but differing in method of manufacture.
35-060F01	A printed-circuit board not electrically and mechanically interchangeable with the 35-060, but described by the same set of drawings.
35-060R01	A revised 35-060 printed-circuit board. Probably supercedes the 35-060.
35-060A01	The 8½ by 11 inch parts list for a 35-060.
35-060B08	The 11 by 17 inch schematic for a 35-060.
06-072	The 72nd utility program assigned a part number.
06-072A13	An 8½ by 11 inch listing of the 06-072 program.
06-072M03	An absolute binary deck of punched cards for the 06-072 program.
06-072A12	An 8½ by 11 inch information drawing on the 06-072 program. Probably a part of the program.
29-060	The 60th manual assigned a number under this system. Note that this number is not referenced in any way to the part number of equipment described in the manual.

4.3 Drawing System

This section describes the drawings provided with INTERDATA equipment. Note that drawings provided with peripheral devices and other purchased items may vary from the system described in this section.

A digital system may be divided into a collection of functionally independent circuits such as memory, Processor, and I/O device controllers. These circuits may or may not be saleable units in their own right, but in the electrical sense they are essentially self contained and capable of performing their function with minimum dependence on other functional circuits in the system. Hence a functional circuit is treated as a building block. Each functional circuit is described electrically by a detailed functional schematic. Each schematic contains a variety of information including type and location of discrete integrated circuits (IC's), pin connections, all interconnections within the schematic connector pin numbers and connections to other schematics. Further, the schematics are drawn to reflect, in an orderly fashion, all logical operations performed by the circuits. Generally, symbols used on schematics conform to MIL-STD-806B.

Registers are named according to the following rules:

1. The register mnemonic name has a maximum of three letters.
2. Each bit in the register is numbered, usually starting at 00 on the left, or most significant position, and continuing to N-1 on the right, where N is the number of bits in the register.
3. The 00 bit is the Most Significant Bit and the N-1 is the Least Significant Bit.

The IC's, mounted directly on the logic board, are represented on the schematic drawings by logic symbols. Each symbol contains the reference designation, device part number (category and sequence), and symbol mnemonic designation. Refer to Figure 3.

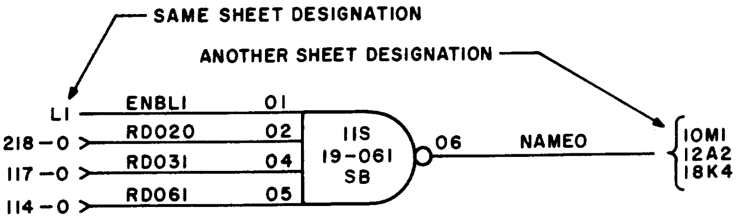

SAME SHEET DESIGNATION
ANOTHER SHEET DESIGNATION
L1
218-0
117-0
114-0
ENBL1
RD020
RD031
RD061
01
02
04
05
11S
19-061
SB
06
NAMEO
10M1
12A2
18K4

Figure 3. Example of a Schottky Buffer

The designations, numbers, and references shown in Figure 3 are:

11S - This indicates the component location on the logic board. Figure 4 illustrates the method generally used to determine component location on a logic board. With the logic board oriented so that the header connectors (Connector 0 and Connector 1) are on the right, the components are lettered from left to right starting in the upper left corner. That is, the first IC in the upper left corner is A01 and the first capacitor is C1. Test points are lettered bottom to top from A-Y (omitting I, O, L, E).

19-061 - The number 19 is the category number of ICs, and the 061 is the sequence number of the component.

SB - Indicates this component is a Schottky Buffer. Some common designations used are:

SA - Schottky AND Gate
SB - Schottky Buffer
SG - Schottky Gate
SGO - Schottky Gate, Open Collector
HG - High Speed Gate
HPO - High Speed Power Gate, Open Collector

L1 - This input lead is from area L1 on the same schematic sheet.

10M1, 12A1, and 18K4 - Indicate outputs to another logic schematic sheet.

218-0, 117-0, and 114-0 - Indicate inputs from Connector 0.

Note that the pin numbers (01, 02, 04, 05, and 06) correspond directly to the actual IC pin numbers.

Figure 4 also shows the locations of the header connectors (Connector 0 and Connector 1) and the cable connectors (Connector 2 and Connector 3). All logic boards always contain Header Connectors 0 and 1, however, any combination (either, both, or none) of cable connectors (Connector 2 and Connector 3) may be provided.

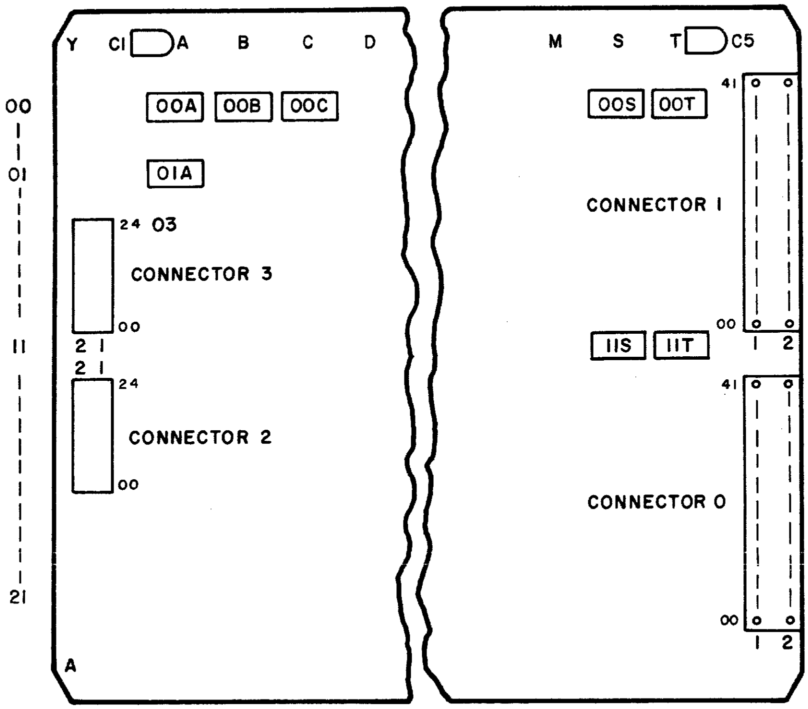

Y
C1
A
B
C
D
M
S
T
C5
00
01
11
21
00A
00B
00C
01A
24 03
CONNECTOR 3
00
2 1
2 1
24
CONNECTOR 2
00
A
00S
00T
41
CONNECTOR 1
00
1 2
11S
11T
41
CONNECTOR 0
00
1 2

Figure 4. Example of a Logic Board Layout

Figure 5 provides the pin numbering scheme for the header and cable connectors. Header connectors always have 2 rows of pins and 42 positions. Cable connectors always have 2 rows of pins but may vary in the number of positions.

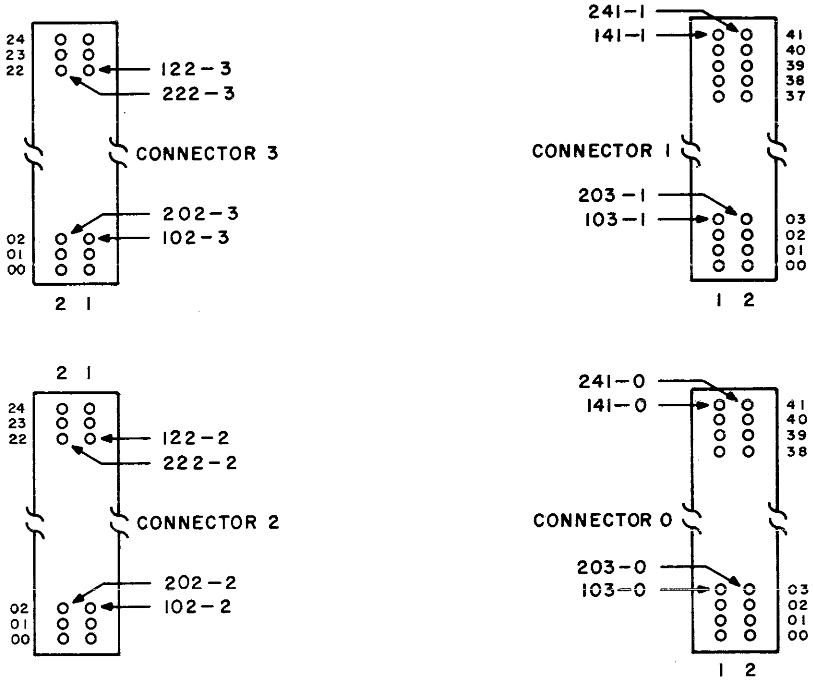


Figure 5. Connector Pin Numbering

A net is defined as an electrical connection between two or more points in a circuit. Ordinarily, a net has an originating end (usually a collector where the signal is generated) and one or more terminating ends. Often it is convenient to assign descriptive mnemonic names to nets as a way of identifying them on schematics. Whether a net is named or not is sometimes arbitrary. However, a net is always assigned a name if:

1. The net is contained on one drawing sheet but is not shown as a complete solid line on that sheet.
2. Part of the net appears on more than one sheet.
3. Part of the net connects with a different schematic.
4. Part of the net leaves a logic board.

If a net is named, the following rules are observed.

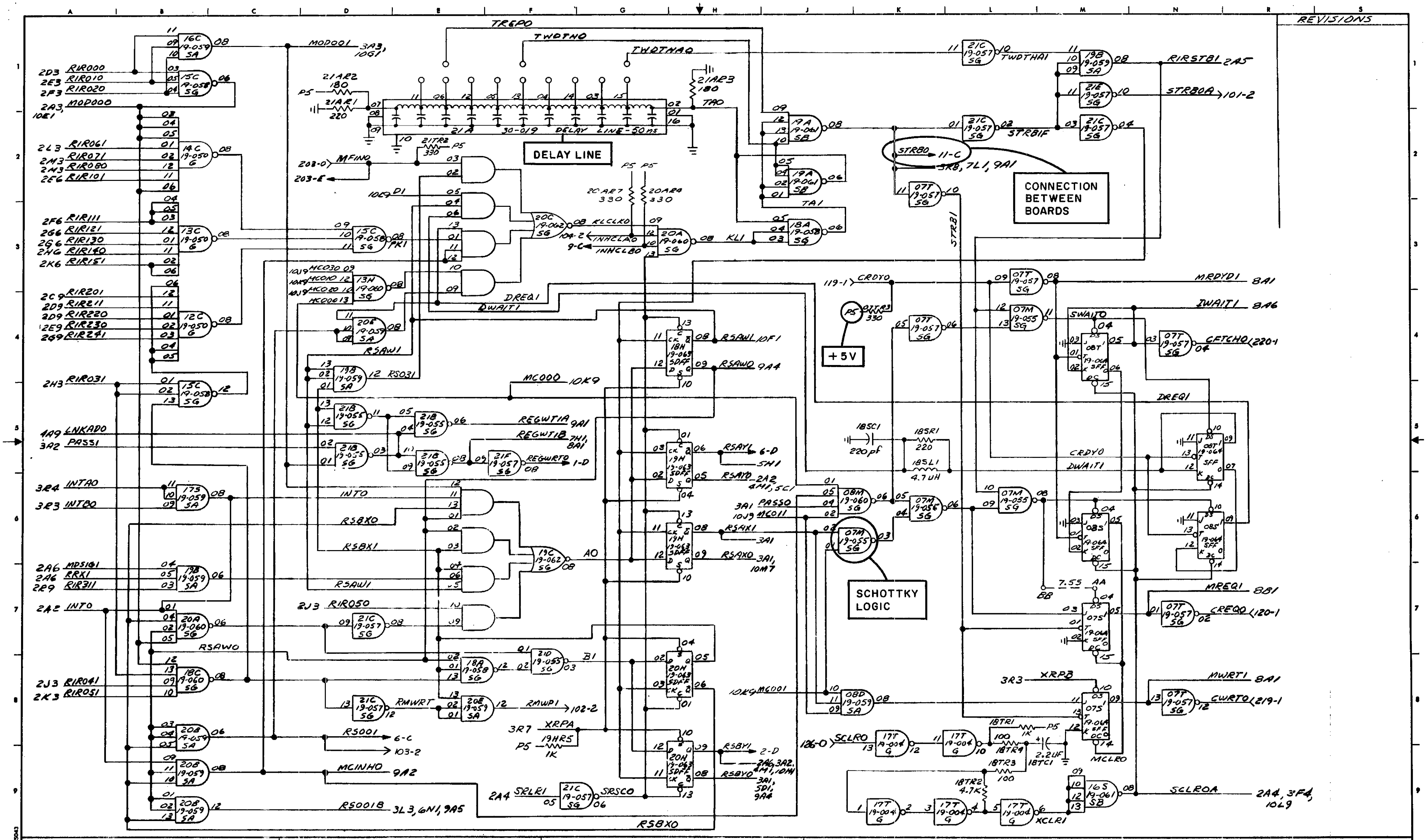
1. All mnemonic names are a maximum of six characters.
2. All decimal digits and upper case letters except the letters "I, O, Q, and Z" are permitted.
3. No other characters permitted.
4. Where possible, mnemonics are descriptive. However, it should be recognized that descriptive names are not always possible and a danger of misinterpreting a mnemonic exists.
5. Mnemonic names are not repeated within a schematic.
6. Every mnemonic is suffixed by a state indicator. This indicator consists of the digit "1" for the logically true state, or the digit "0" for the logically false state. For example, the set side of a flip-flop would have the "1" state indicator, while the reset side would have the "0" state indicator. The state indicator for a function changes each time that function is inverted. Thus, the state indicator permits assigning the same mnemonic to functions that are identical except for an inversion.
7. When a logical function is inverted, an inversion indicator is added after the state indicator. This allows for functionally equivalent, but electrically different nets to have the same mnemonic name. For example, assume a signal NAME1. NAME1 may be inverted to produce NAME0. If NAME0 is then inverted, NAME1A is produced. NAME1 and NAME1A are functionally equivalent, but physically different nets.

Sometimes a net fans-out to many sheets in a schematic. It is also possible for a net to fan-out to sheets in different schematics. In these situations, the net is assigned a mnemonic name. The net is also "zoned" from sheet to sheet to allow for properly identifying the originating and terminating ends of the net. The originating end of a net is defined as the collector at which a signal is generated. All other points to which the net connects are called terminating ends. When a lead leaves a sheet at the originating end, it is zoned to each and every sheet on which the net reappears, by indicating first the page number, followed by the schematic number that contains the page. For example, assume that the gate shown on Figure 3 is on a schematic, Sheet 20. The output, NAME0, appears on Sheets 10, 12 and 18 of the schematic. Note that the schematic number is implied. When a net enters a sheet from another sheet, it is labeled with the same mnemonic name, and is zoned back to the originating end of the net only. Thus, on Figure 3, ENBL1 may, however, have many other terminations in addition to the one shown. Generally then, when a net leaves the sheet where it originates, it is zoned to every other sheet where the net terminates, while the terminating end is zoned only to the originating sheet. Note that in the Model 80 schematics, signals are co-ordinated between sheets only when the sheets are related to the same board. When a signal leaves a board, the back panel map must be used.

When a lead leaves a logic board, it usually does so through a logic board back panel connector pin. These connector pins must be shown on the schematic even if the complete net is shown on one drawing sheet. Only the connector pin number need be indicated under the pin symbol, since the connector number itself is implied by the logic board location number in the logic symbol or in the footnote. Thus, on Figure 3, RD061 enters the logic board on Pin 114 of Header Connector 0.

Figures 6 and 7 are typical schematic sheets with call-outs illustrating many of the conventions described in this section.

The schematic drawings for the basic digital system and some of the more common expansions are commonly included in the rear of the appropriate digital system maintenance manual. Schematic drawings for other expansions are included with the expansion or with the publications that describe the expansion.


REVISIONS
DELAY LINE
21A 30-019 DELAY LINE - 50ns
TREPO
TWOTHO
TWOTHAO
TWOTHAI
RIRSTBI 2A5
STRBOA 101-2
STRBIF
STRB0 11-C 3R8, 7L1, 9A1
CONNECTION BETWEEN BOARDS
SCHOTTKY LOGIC
+5V
MOD001 3A3, 10G1
MOD000
RIR000
RIR010
RIR020
MFIN0
KLCLK0
INHCLA0
INHCLB0
KLI
TA0
TA1
DREQI
DWAITI
CRDY0
MRDYD1 8A1
IWAITI 8A6
SWAIT0
GFETCH0 220-1
RSAWI
RSAW0
RS031
MC000 10K9
REGWTIA 9A1
REGWTIB 7H1, 8A1
REGWRT0 1-D
LNKAD0
PASSI
INTA0
INTB0
INT0
RSBX0
RSBXI
A0
MDSI61
RRKI
RIR311
RIR050
B1
RIR041
RIR051
RMWRT
RMWPI 102-2
RS001 6-C 103-2
MCINH0 9A2
RS001B 3L3, 6N1, 9A5
RSAWI 10F1
RSAW0 9A4
RSAYI 6-D 5H1
RSAY0 2A2 4M1, 5C1
RSAXI 3A1
RSAX0 3A1, 10M7
RSBYI 2-D
RSBY0 2A6, 3A2, 4M1, 10H4 3A1, 5D1, 9A4
XRPA
SRLRI
SRSC0
PASS0
MC011
MC001
MREQI 8B1
CREQ0 120-1
XRPB
MWRTI 8A1
CWRT0 219-1
SCLR0
XCLRI
MCLR0
SCLR0A 2A4, 3F4, 10L9
18SC1 220pf
18SR1 220
18SL1 4.7uH
18TR1 1K
18TR4 100
18TC1 2.2uF
18TR2 4.7K
18TR3 100
21AR2 180
21AR1 220
21AR3 180
21TR2 330
20AR7 330
20AR4 330
07TR3 330
19HR5 1K
P5

NOTES

Figure 6.
Functional Schematic Format Drawing

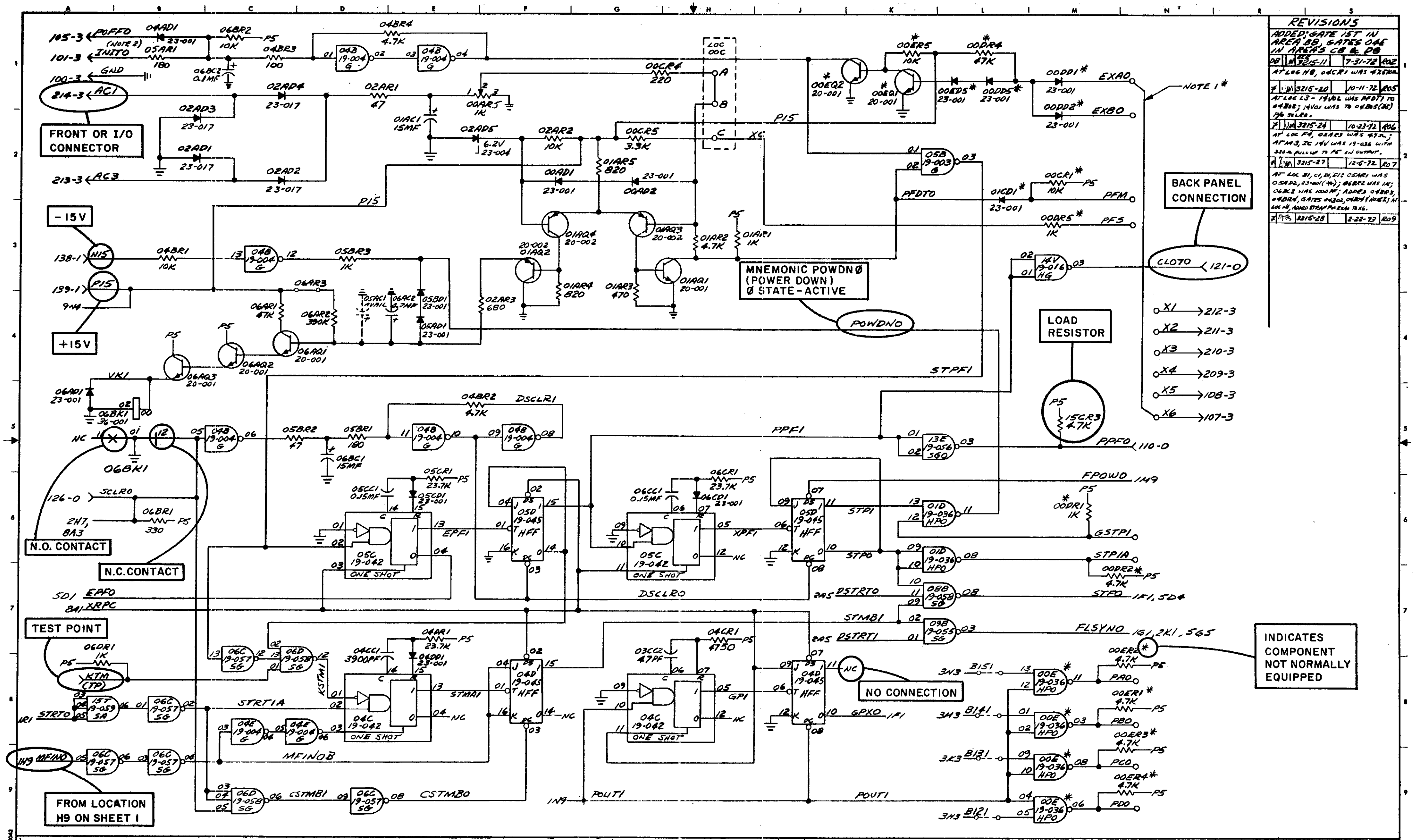
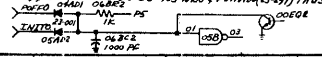

REVISIONS
ADDED; GATE 15T IN AREA B8, GATES 04E IN AREAS C8 & D8
D8 | ECR 3215-11 | 7-31-72 | R02
AT LOC H8, 04CR1 WAS 4.75K
7 | 3215-20 | 10-11-72 | R05
AT LOC L3 - 14V02 WAS PFDT1 TO 04B02; 14V01 WAS TO 04B05(B5) P/O SCLR0.
7 | 3215-24 | 10-23-72 | R06
AT LOC F4, 02AR3 WAS 47Ω; AT M3, IC 14V WAS 19-036 WITH 330Ω PULLUP TO P5 ON OUTPUT.
7 | 3215-27 | 12-5-72 | R07
AT LOC B1, C1, D1, E1: 05AR1 WAS 05AD2, 23-001(+); 06BR2 WAS 1K; 06BC2 WAS 1000PF; ADDED 04BR3, 04BR4, GATES 04B02, 04B04 (NOTE 2); AT LOC N4, ADDED STRAP FM EXA0 TO X6.
7 | 3215-28 | 2-22-73 | R09
105-3 POFF0
(NOTE 2)
101-3 INIT0
100-3 GND
214-3 AC1
213-3 AC3
FRONT OR I/O CONNECTOR
04AD1 23-001
05AR1 180
06BR2 10K
06BC2 0.1MF
04BR3 100
04BR4 4.7K
04B 19-004 G
LOC 00C
A
B
C
00CR4 220
02AD4 23-017
02AD3 23-017
02AD1 23-017
02AD2 23-017
02AR1 47
00AR5 1K
01AC1 15MF
02AD5 6.2V 23-004
02AR2 10K
00CR5 3.3K
01AR5 820
00AD1 23-001
00AD2 23-001
P15
XC
01AQ4 20-002
01AQ3 20-002
01AQ2 20-002
01AQ1 20-001
01AR4 820
01AR3 470
01AR2 4.7K
01AR1 1K
02AR3 680
MNEMONIC POWDNØ (POWER DOWN) Ø STATE - ACTIVE
POWDN0
00EQ2 20-001
00EQ1 20-001
00ER5 10K
00DR4 47K
00ED5 23-001
00DD5 23-001
00DD1 23-001
00DD2 23-001
EXA0
EXB0
NOTE 1
05B 19-003 G
PFDT0
01CD1 23-001
00CR1 10K
PFM
00DR5 1K
PF5
BACK PANEL CONNECTION
14V 19-016 HG
CL070
121-0
-15V
+15V
138-1 N15
139-1 P15
9N4
04BR1 10K
04B 19-004 G
05BR3 1K
06AR3
06AR1 47K
06AR2 390K
05AC1 AVAIL
06AC2 4.7MF
05BD1 23-001
05AD1 23-001
06AQ1 20-001
06AQ2 20-001
06AQ3 20-001
VK1
06AD1 23-001
06BK1 36-001
STPF1
X1 212-3
X2 211-3
X3 210-3
X4 209-3
X5 108-3
X6 107-3
LOAD RESISTOR
P5 15CR3 4.7K
PPF0 110-0
NC
06BK1
04BR2 4.7K
DSCLR1
05BR2 47
05BR1 180
06BC1 15MF
PPF1
13E 19-056 5G0
126-0 SCLR0
2H7, 8A3
06BR1 330
N.O. CONTACT
N.C. CONTACT
05CC1 0.15MF
05CR1 23.7K
05CD1 23-001
05C 19-042 ONE SHOT
EPF1
05D 19-045 HFF
06CC1 0.15MF
06CR1 23.7K
06CD1 23-001
XPF1
DSCLR0
STP1
STP0
FPOW0 1N9
01D 19-036 HP0
00DR1 1K
GSTP1
STP1A
00DR2 4.7K
5D1 EPF0
8A1 XRPC
DSTRT0
08B 19-058 5G
STF0 1F1, 5D4
STMB1
09B 19-055 5G
DSTRT1
FLSYN0 1G1, 2K1, 5G5
INDICATES COMPONENT NOT NORMALLY EQUIPPED
TEST POINT
06DR1 1K
KTM (TP)
06C 19-057 5G
06D 19-058 5G
KSTM1
04CC1 3900PF
04AR1 23.7K
04DD1 23-001
04C 19-042 ONE SHOT
STMA1
04D 19-045 HFF
03CC2 47PF
04CR1 4750
GP1
GPX0 1F1
NO CONNECTION
15T 19-059 5A
1R1 STRT0
STRT1A
04E 19-004 G
MFIN0B
1H9 MFIN0
FROM LOCATION H9 ON SHEET 1
CSTMB1
CSTMB0
1N9
POUT1
3H3 B151
4H3 B141
3K3 B131
3H3 B121
00E 19-036 HP0
00ER2 4.7K PA0
00ER1 4.7K PB0
00ER3 4.7K PC0
00ER4 4.7K PD0

Figure 7.
Functional Schematic Format Drawing

NOTES 1. ASTERISK * INDICATES COMPONENT NOT NORMALLY EQUIPPED ON 35-405M00 & F01M00; CIRCUIT ALWAYS APPEARS ON 35-405M01 & F01M01.

2. INIT0 CIRCUIT APPEARS ONLY ON 35-405M01 & F01M01 (25-368); CIRCUIT IS ON 35-405M00 & F01M00 (25-297) THUS:


POFF0
04AD1
06BR2
23-001
1K
P5
INIT0
05AD2
06BC2
1000 PF
01
05B
03
00EQ2

APPENDIX 1

PART NUMBER CROSS REFERENCE TABLE

INTERDATA Part Number	Type	JEDIC Number
19-001	Dual 4 Input Nand DTL	15861
19-002	Triple 3 Input Nand DTL	15863
19-003	Quad 2 Input Nand DTL	15849N
19-004	Hex 1 Input Nand DTL	15837N
19-005	Dual Power Gate DOC	8633N
19-006	Dual Buffer DTL	1582N
19-007	Flip-Flop DTL	15848N
19-008	Gate Expander Dual 4 Input DTL	15833N
19-009	8 Bit Stack DTL	903059 (Fairchild)
19-010	Differential Compartor LIN	72710L
19-012	Dual 4 Input Buffer TTL	74H40H
19-013	Quad 2 Input Nand DTL	15846
19-014	Dual J-K Flip-Flop DTL	158097N
19-015	Hex Inverter 1 Input	74H04H
19-016	Quad 2 Input TTL	74H00N
19-017	Triple 3 Input TTL	74H10N
19-018	Dual 4 Input TTL	74H20N
19-019	Single 8 Input TTL	MC3015 (Motorola)
19-020	Operational Amplifier LIN	MC1709C (Motorola)
19-021	Quad 2 Input Power DOC	15858N
19-022	Dual J-K Flip-Flop TTL	MC3061P (Motorola)
19-023	Selected Dual Buffer 19-006 with 20-30 nsec. delay DTL	15832N
19-024	Triple 3 Input AND TTL	74H11N
19-025	Dual 4 Input AND TTL	74H21N
19-026	2-2-2-3 Input AND-OR TTL	7475N

INTERDATA Part Number	Type	JEDIC Number
19-027	4 Bit Latch TTL	7475N
19-028	4 Bit Adder TTL	7483N
19-029	Quad Exclusive - OR TTL	7486N
19-030	4 Bit Shift Register TTL	7495N
19-031	One Shot TTL	7412N
19-032	1 out of 10 Decoder TOC	74145N 5445 7445
19-033	Sense Amplifier LIN	7524N
19-034	Retriggerable One Shot TTL	74122N
19-035	4 Bit Counter TTL	74193N
19-036	Quad 2 Input Open Collector TTL	7438N
19-037	High Performance Operational Amp	7748393 (Fairchild)
19-038	Dual 4 line to 1 line Mux TTL	74153
19-039	4 Bit ALU TTL	74181
19-040	Look Ahead Carry TTL	74182
19-041	4 x 4 Register Stack TTL	74170
19-042	Dual Retriggerable One Shot TTL	74123N
19-043	Quad 2 Input Open Collector TTL	74H01N
19-044	Hex Inverter Open Collector TTL	74H05N
19-045	Dual J-K Flip-Flop TTL	74H106
19-046	Quad RS-232C Line Driver	MC1488L (Motorola)
19-047	Quad RS-232C Line Receiver	MC1489AL (Motorola)
19-048	8 Bit Shifter	74198N
19-050	8 Input Nand TTL	74H30
19-051	1024 Bit PROM TTL	74187 (Fairchild)
19-055	Quad 2 Input Nand STTL	74S00
19-056	Quad 2 Input Nand Open Collector STTL	74S03
19-057	Hex 1 Input Inverter STTL	74S04
19-058	Triple 3 Input Nand STTL	74S10
19-059	Triple 3 Input AND STTL	74S11
19-060	Dual 4 Input Nand STTL	74S20

INTERDATA Part Number	Type	JEDIC Number
19-061	Dual 4 Input Buffer STTL	74S40
19-062	2-2-3-4 Input AND-OR Inverter STTL	74S64
19-063	Dual D Edge Triggered Flip-Flop STTL	74S74
19-064	Dual J-K Flip-Flop STTL	74S112
19-065	Quad 2:1 Max Non-inverting STTL	74S157
19-066	Quad 2:1 Mux Inverting STTL	74S158
19-067	4 Bit ALU STTL	74S181
19-068	Carry Look Ahead STTL	74S182
19-069	8 line to 1 line Mux STTL	74151
19-070	4 Bit Syncronous Counter TTL	74161
19-071	Quad D Edge Triggered Flip-Flop	74175
19-072	4 Bit Left/Right Shift Register TTL	74194
19-073	Dual 4:1 Mux Tri-State TTL	8214 (National)
19-074	8 Bit Priority Encoder TTL	9318 (Fairchild)
19-075	16 x 4 Register Stack TTL	3101A (Intel)
19-076	1024 Bit Memory MOS	TM54062
19-077	256 Bit Memory TTL	6531 (Monolithic Memories)
19-078	Dual 4 Input Nand-OC	74S22
19-080	High-Speed PROM	82S29 (Signetics)
19-081	Univ. Asynchronous Receiver/Transmitters	TR1042A (Western Digital)
19-082	2-2-3-4 Input AND-OR Invert Open Collector STTL	74S65
19-083	9 Bit Parity Generator/Checker STTL	82S62 (Signetics)
19-085	Monolithic Timing Circuit	MC1555 (Motorola) NE555V (Signetics)
19-086	741 C DIP Operational Amplifier	U6A7741393 (Fairchild)
19-087	747 DIP Operational Amplifier	U7A774 (Fairchild)
19-088	737 C DIP Operational Amplifier	U6A773393 (Fairchild)
19-089	Dual D Edge Triggered Flip-Flop	74H74
19-090	High Speed (710) Differential Comparator DIP	U6A771093 (Fiarchild)
19-091	Retriggerable Single One Shot	9600 (Fairchild)

INTERDATA Part Number	Type	JEDIC Number
19-092	Negative Voltages Regulator	MC1463R (Motorola)
19-093	Positive Voltages Regulator	MC1469R (Motorola)
19-094	Voltage Regulator	U6A7723393 (Fairchild) MC1723CL (Motorola)
19-095	Linear Positive Voltage Regulator	U9H7805393 (Fairchild)
19-096	First In-First Out Serial Memory 64 Word 4 Bit	3341 (Fairchild)
19-097	Amplifier	LH0002H (National)
19-098	Quad 2:1 Multiplexor Non-Inverting	74157
19-099	Dual Sense Amplifier	75234N
19-100	Driver	75452N
19-101	4-2 Input Buffer	7437N
19-102	6-1 Input Buffer OC	7407N
19-103	1 out of 10 Decoder	7442N
19-104	Current Switch	75325N
20-001	Transistor NPN High Speed Switch	2N3646
20-002	Transistor PNP 500 MA	MPS6534 (Motorola)
20-003	Transistor	2N3902
20-004	Transistor NPN	2N5189
20-006	Transistor NPN 15 Amps 100W T03 case	2N3055 (RCA)
20-007	Transistor NPN 3 Amps	TIP31A
20-008	Transistor PNP 3 Amps	TIP32A
20-009	Transistor Triac 2 Amps 100V	A03001 (Electronic Control Corp).
20-010	Transistor NPN 500 MA Code Driver	2N5845
20-011	Transistor Photo	2N5777
20-012	Transistor PNP High Current Switch	2N2907
20-013	Transistor NPN	2N3303
20-014	Transistor NPN	2N4238
20-015	Transistor PNP	2N4235
20-016	Transistor PNP	2N3740
20-017	Transistor NPN	2N3766

INTERDATA Part Number	Type	JEDIC Number
20-018	Transistor, Power Silicon NPN	2N3054
20-019	Transistor NPN Fast PWR Switch	2N6308 (Motorola)
20-020	Transistor Switching 1 Amp T05 can	2N3725
20-021	Transistor NPN Silicon	MPS3646 (Motorola)
20-022	Transistor NPN	1N1711
20-023	Transistor PNP	2N2905A
20-024	Transistor Switch	2N3776
21-025F01	1K ohm-15 to Common DIP	898-1-1K ohm (Beckman)
21-025F02	470 ohm-15 to Common DIP	898-1-470 ohm (Beckman)
21-025F03	330 ohm-15 to Common DIP	898-1-330 ohm (Beckman)
23-001	Diode High Speed-High Current	1N914
23-002	Diode 5.1 V Zener	1M5.1ZS5 (Motorola)
23-003	Diode 10V Zener	1M10ZS5 (Motorola)
23-004	Diode 6.2 V Zener	1M6.2ZS5 (Motorola)
23-007	Diode Mot Bridge	MDA962-2 (Motorola)
23-008	Diode Int. Rectifier	40HF-5R
23-009	Diode	1N4735
23-010	Diode Int. Rectifier	S1Y1P
23-011	Diode Rectifier	2N681
23-012	Diode Thermister	KA31J1 (Fenwall)
23-013	Diode 9.4V	1N2163
23-014	Diode	1N3880
23-015	Diode	1N3889
23-016	Diode Bridge Recitifer	VS448 (Varo)
23-017	Diode	1N2070
23-018	Diode 18 V Zener	1N4746A
23-019	Diode	1N3615
23-020	Diode 8.2V Zener	1N756A
23-021	Diode 9.1 V Zener	1N757A
23-022	Diode 3.3V Zener	1N746A
23-023	Diode Bridge Rectifier	KBH2506 (General Instrument)

INTERDATA Part Number	Type	JEDIC Number
23-024	Diode, Power Fast Rec. 30 Amps.	1N3909
23-025	Diode, Power Fast Rec. 3 Amps.	A115A (General Electric)
23-026	Triac 600V 30 Amps	2N6162
23-027	Diac 32V	1N5761
23-028	Power SCR Thyristor	2N4441
23-029	Diode	1N4607
23-030	Diode	1N4156
23-031	Diode 6.6 V Zener	1N4736
23-032	Diode 8.8 V Zener	1N4739
23-033	16 Diode Array	45190 (Litton)
30-018	100 nsec. Delay Line 10 taps	30-018 (Princeton Advanced Eng.)
30-019	50 nsec. Delay Line 10 taps	30-018 (Princeton Advanced Eng.)

PROCESSOR

M80-000 AND M80-001
MODEL 80
INSTALLATION SPECIFICATION

1. INTRODUCTION

This specification provides installation information for INTERDATA Model 80 Digital Systems.

The INTERDATA Model 80 Digital System features a highly modular structure which permits configuration to suit the user's exact needs. It provides the means for convenient expansion as the user's requirements grow. This document describes the Processor and expansion chassis, power supply mounting, filler and display panel mounting, and the interconnecting cables. Integrated circuit boards are discussed with respect to cabling and location only. Circuit descriptions of these boards are provided in the appropriate maintenance or instruction manuals. Note that the following discussion assumes that the equipment is mounted in standard INTERDATA cabinets.

2. UNPACKING

To avoid damage to the Model 80 or its peripherals, read the following procedures before starting an installation.

1. Carefully remove each component from its carton or crate, observing any special unpacking instructions included with the component.
2. Inspect all components for physical damage.
3. If the system is shipped from INTERDATA already rack mounted, simply check to insure that all terminals and connectors are secured properly.
4. The Model 80 should be located with sufficient free space (sides and back) to insure unobstructed air flow. A minimum clearance of two inches on each side and six inches at the back is required.

3. MECHANICAL CONFIGURATION

Figures 1 through 4 are intended to familiarize the reader with the mechanical components of a typical INTERDATA Digital System. Dimensions and mounting information are provided for the Basic Cabinet, Chassis Support Rails, Display Panels, and Filler Panels. Note in Figure 4 that while the 5 ¼ inch, 7 inch, and 10 ½ inch Filler Panels and the Display Panel Mount the same way (via retaining brackets), the smaller 1 3/4 inch Filler Panel mounts with spring clips.

4. POWER SUPPLY INSTALLATION

This section describes the installation of the Model 80 Power Supplies. Mounting information and cabling instructions are provided for both the 34-015 Logic Power Supply and the 34-014 Memory Power Supply.

4.1 Mounting

The Power Supplies mount directly behind the Processor and Expansion Chassis. (See Figure 5.) They are attached to the right mounting upright (looking from the rear) via two mounting blocks and two nylon spacers. (See Figure 6.)

WARNING

> Before hinging out the power supplies, the rack levelling feet should be lowered. Up to three power supplies can be hinged out at one time after the levellers are in contact with the floor surface.

The Power Supplies may be swung in or out on their mounting pivots for easy access to the back plane. When they are in the operating position, they are secured by two 10-32 screws which attach to the left mounting upright (viewed from the rear).

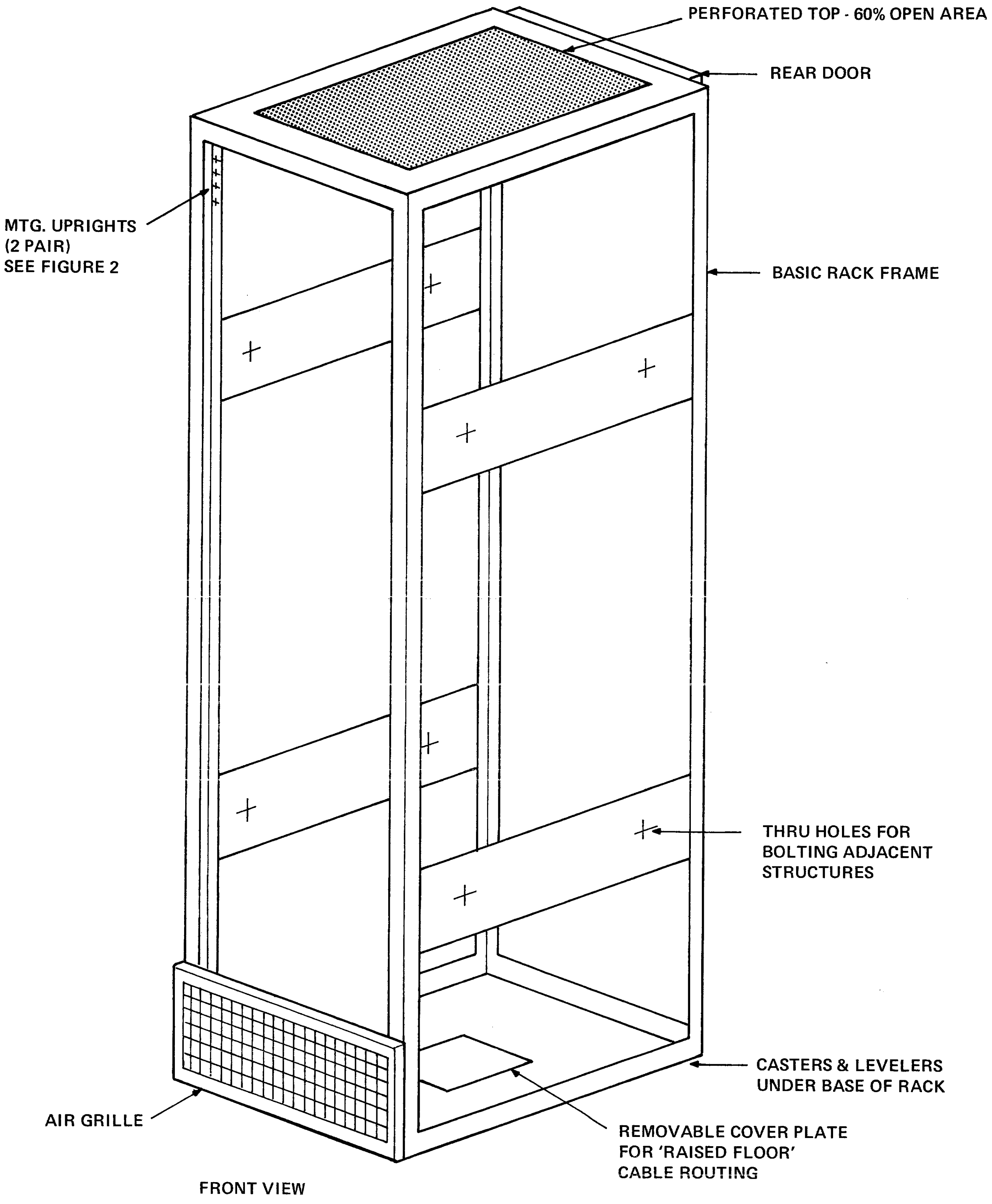
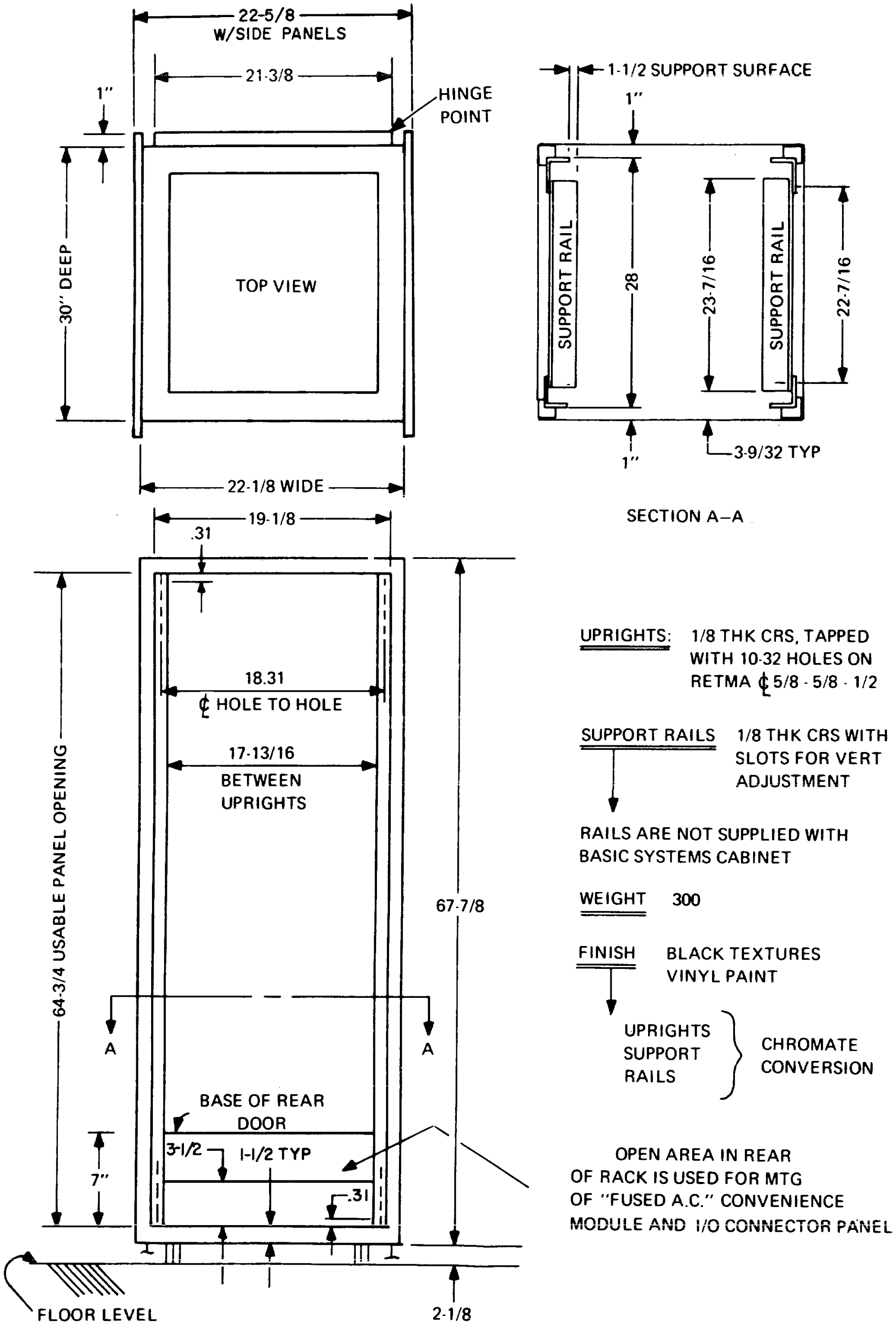

PERFORATED TOP - 60% OPEN AREA
REAR DOOR
MTG. UPRIGHTS
(2 PAIR)
SEE FIGURE 2
BASIC RACK FRAME
THRU HOLES FOR
BOLTING ADJACENT
STRUCTURES
CASTERS & LEVELERS
UNDER BASE OF RACK
AIR GRILLE
REMOVABLE COVER PLATE
FOR 'RAISED FLOOR'
CABLE ROUTING
FRONT VIEW

Figure 1. Basic Cabinet



22-5/8
W/SIDE PANELS
21-3/8
HINGE POINT
1"
30" DEEP
TOP VIEW
22-1/8 WIDE
1-1/2 SUPPORT SURFACE
1"
SUPPORT RAIL
28
23-7/16
SUPPORT RAIL
22-7/16
1"
3-9/32 TYP
SECTION A–A
19-1/8
.31
18.31
℄ HOLE TO HOLE
17-13/16
BETWEEN
UPRIGHTS
64-3/4 USABLE PANEL OPENING
67-7/8
A
A
BASE OF REAR
DOOR
3-1/2
1-1/2 TYP
.31
7"
FLOOR LEVEL
2-1/8

UPRIGHTS: 1/8 THK CRS, TAPPED WITH 10-32 HOLES ON RETMA ℄ 5/8 - 5/8 - 1/2

SUPPORT RAILS 1/8 THK CRS WITH SLOTS FOR VERT ADJUSTMENT

RAILS ARE NOT SUPPLIED WITH BASIC SYSTEMS CABINET

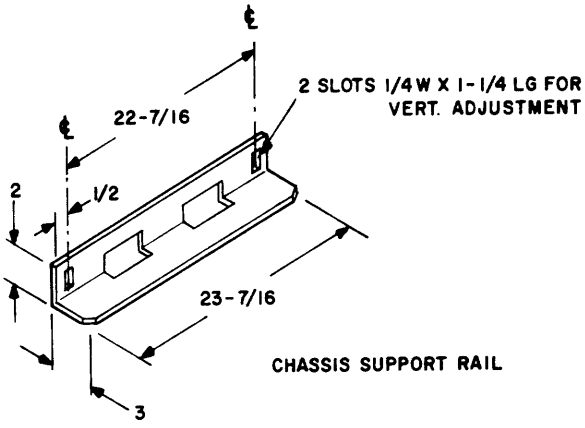
WEIGHT 300

FINISH BLACK TEXTURES VINYL PAINT

UPRIGHTS
SUPPORT RAILS } CHROMATE CONVERSION

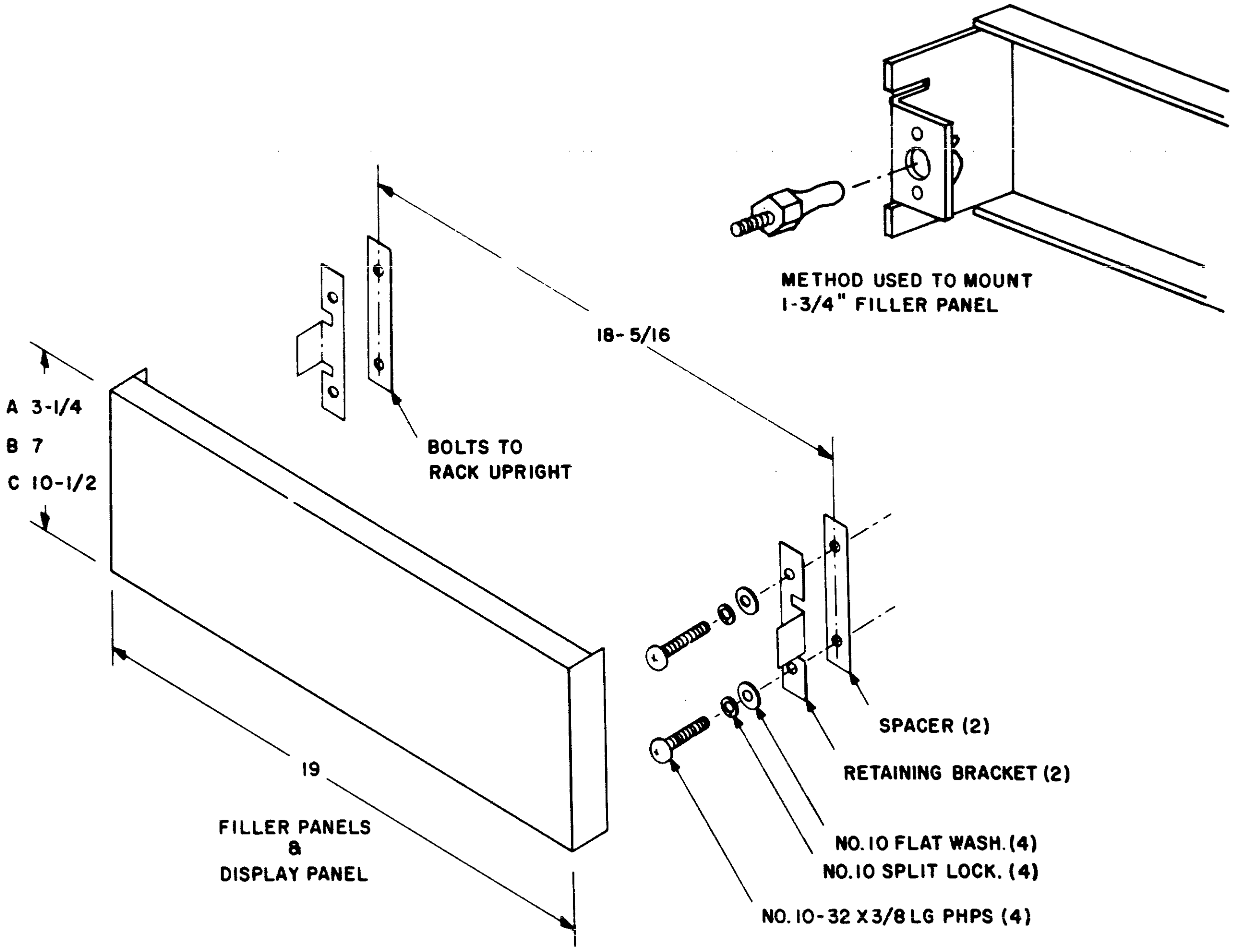
OPEN AREA IN REAR OF RACK IS USED FOR MTG OF "FUSED A.C." CONVENIENCE MODULE AND I/O CONNECTOR PANEL

Figure 2. Basic Cabinet Physical Dimensions



℄
2 SLOTS 1/4 W X 1-1/4 LG FOR VERT. ADJUSTMENT
℄
22-7/16
2
1/2
23-7/16
CHASSIS SUPPORT RAIL
3

Figure 3. Chassis Support Rail



METHOD USED TO MOUNT 1-3/4" FILLER PANEL
18-5/16
A 3-1/4
B 7
C 10-1/2
BOLTS TO RACK UPRIGHT
SPACER (2)
RETAINING BRACKET (2)
19
FILLER PANELS & DISPLAY PANEL
NO. 10 FLAT WASH. (4)
NO. 10 SPLIT LOCK. (4)
NO. 10-32 X 3/8 LG PHPS (4)

Figure 4. Typical Mounting Configuration for Display and Filler Panels

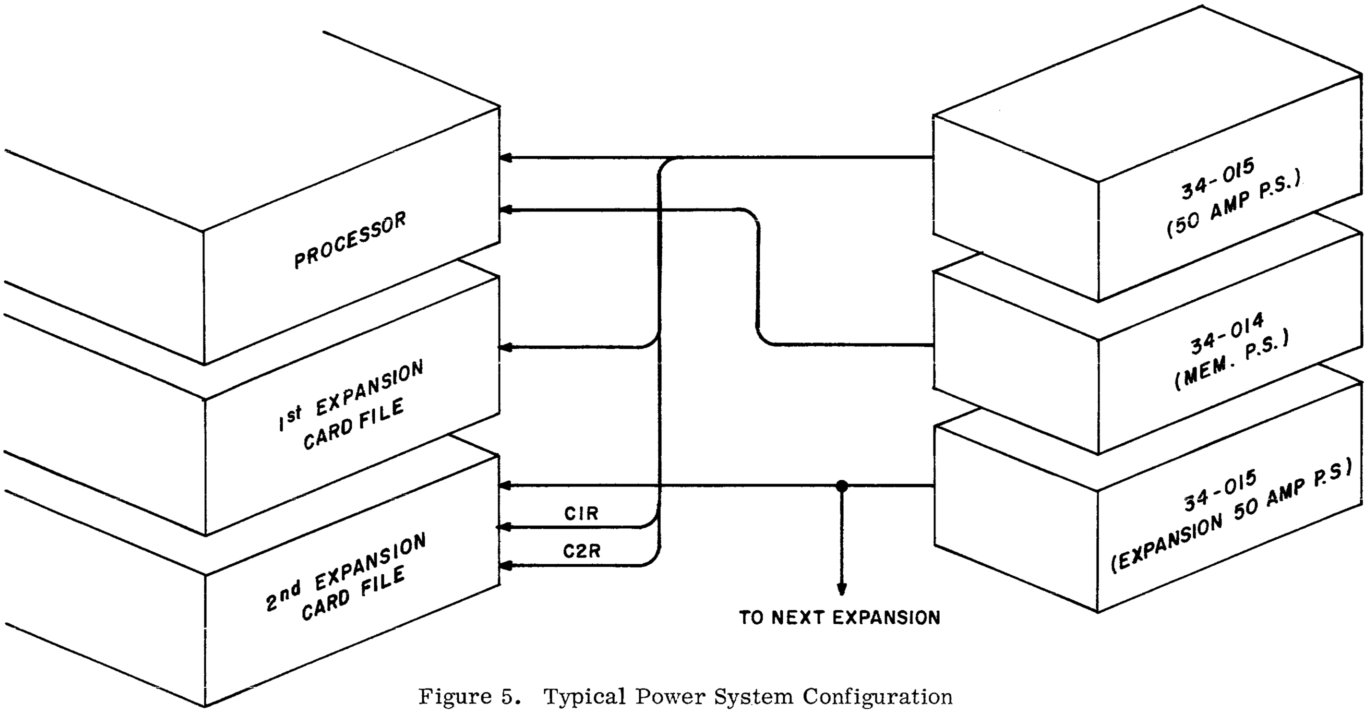

PROCESSOR
1st EXPANSION CARD FILE
2nd EXPANSION CARD FILE
C1R
C2R
TO NEXT EXPANSION
34-015 (50 AMP P.S.)
34-014 (MEM. P.S.)
34-015 (EXPANSION 50 AMP P.S)

Figure 5. Typical Power System Configuration

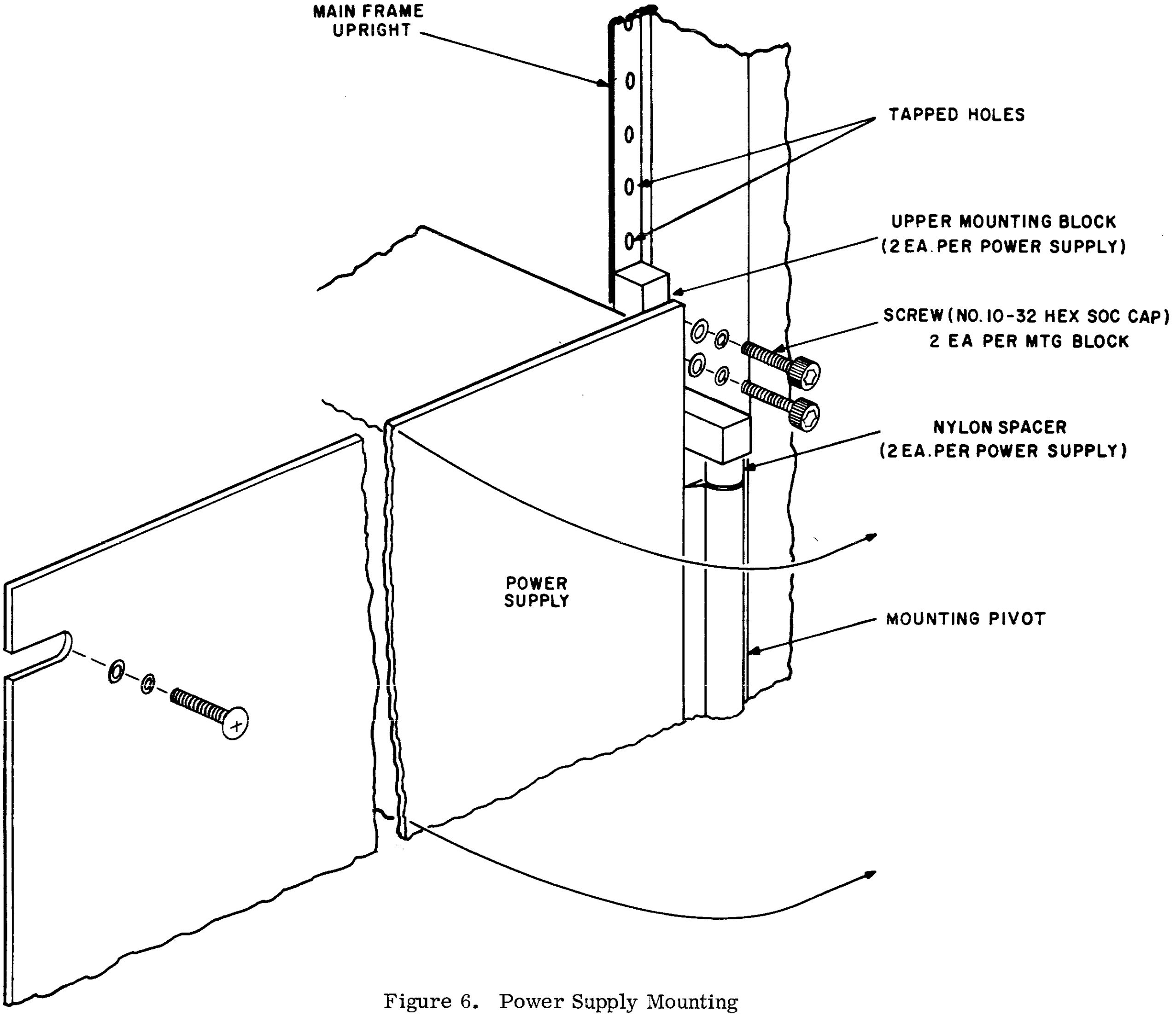

MAIN FRAME UPRIGHT
TAPPED HOLES
UPPER MOUNTING BLOCK (2 EA. PER POWER SUPPLY)
SCREW (NO. 10-32 HEX SOC CAP) 2 EA PER MTG BLOCK
NYLON SPACER (2 EA. PER POWER SUPPLY)
MOUNTING PIVOT
POWER SUPPLY

Figure 6. Power Supply Mounting

4.2 Power Supply/Chassis Cabling

A typical Model 80 Power Supply/Chassis configuration is shown in Figure 7. (The power supplies may be reversed if required.) A cable from each power supply terminates at the Processor and Expansion Chassis back panel as indicated. Refer to the Model 80 Power System Description, 02-261A12, which is contained in the Model 80 Maintenance Manual, Publication Number 29-280 for details. The installation sequence for the Power System is:

1. Mount the power supply chassis. Refer to Figures 5 and 6.
2. Connect the cables to the Processor and Expansion Chassis as shown in Figure 7. Fan power must be connected as shown before system is powered. If no first Expansion Chassis, secure unused connectors to prevent shorting.

5. PROCESSOR AND EXPANSION CHASSIS MOUNTING

Two Expansion Chassis (10 inch and 15 inch) are available for expanding the INTERDATA Digital System. The 15 inch Expansion Chassis has the same overall dimensions as the Processor Chassis. See Sections 3 and 8 on Configuration. The Expansion or Processor Chassis slides into the rack on the two Chassis Support Rails (see Figures 2 and 3) on the front of the rack.

CAUTION

No chassis should be mounted in cantilever fashion. Chassis support rails MUST be used. If a rack cabinet other than an INTERDATA cabinet is used, consult the rack manufacturer for proper support rails.

The chassis support rails are fastened to the mounting uprights of the front and rear of the rack. Slots are provided in the rails to allow vertical adjustment. The Expansion or Processor Chassis are screwed in place at the mounting uprights in front of the rack. All Expansion Chassis mount below the Processor Chassis. Expansion Chassis cabling is discussed later in this document. Figure 8 shows Expansion Chassis location with respect to the filler panel and power supply.

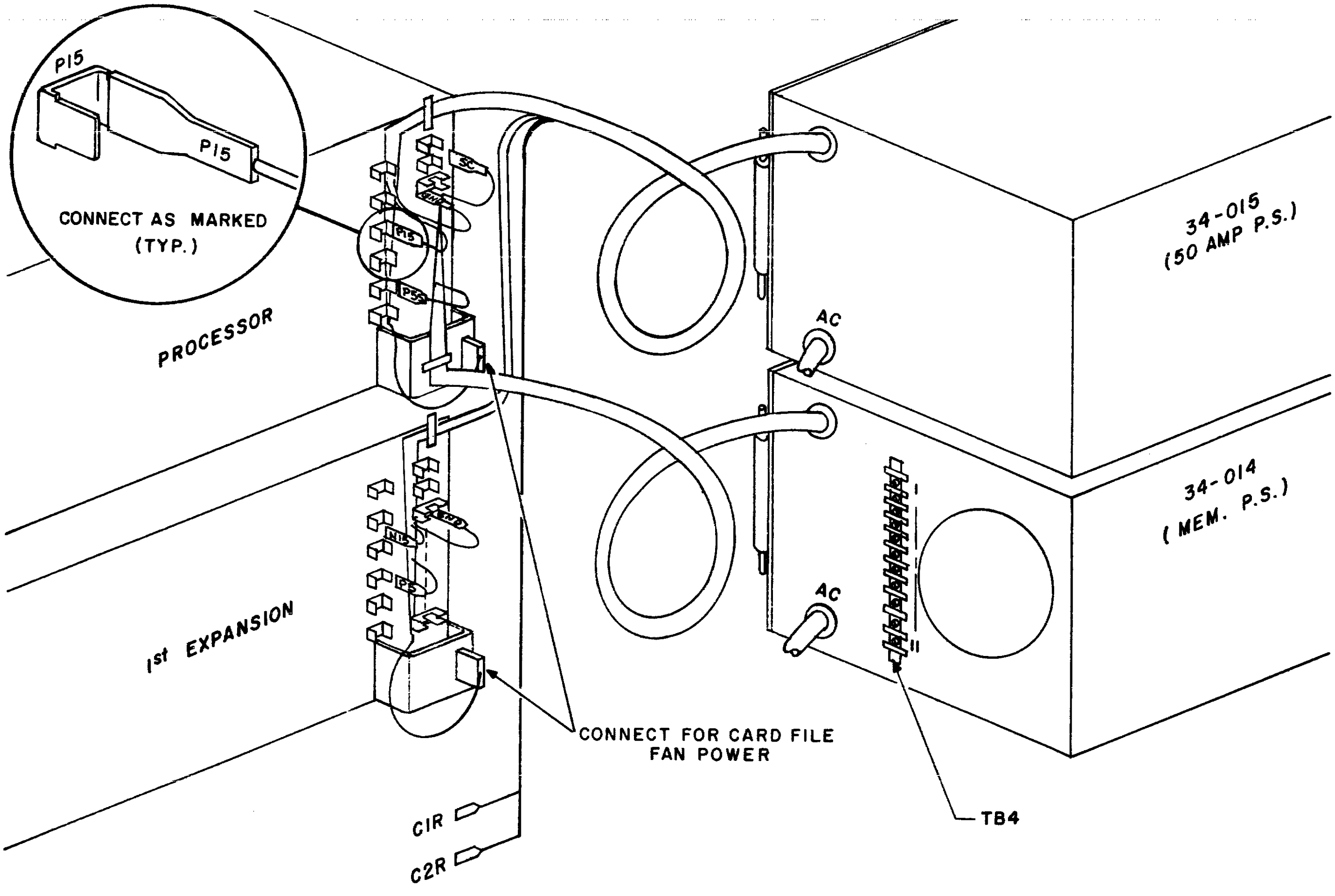


Figure 7. Power System Cabling

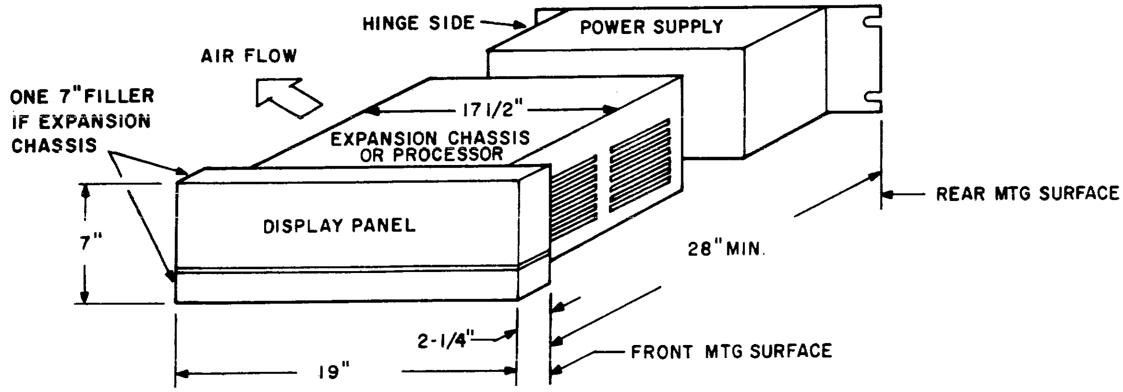


Figure 8. Processor or Expansion Chassis Location

5.1 Processor Installation

The basic Model 80 with 16KB of memory (see Figure 9) is comprised of:

1.	CPU	35-403	slot #7
2.	ALU	35-404	slot #6
3.	IOU	35-405	slot #5
4.	MBC	35-407	slot #4
5.	MSU	35-406	slot #3

The remaining three slots are used to expand memory to the maximum of three additional MSUs or 64 KB of memory. The remaining slots in the basic chassis, after the memory has been expanded, may be used to expand the I/O. Full or halfboard I/O may be plugged into these slots. If a Selector Channel or Multiplexor Bus Buffer (MBFR) is plugged into the basic chassis, all I/O slots on Connector 1 are dedicated to the private Selector Channel or Buffered Bus. Only one of these two devices may be contained in the basic chassis as the private I/O Bus in Connector 1 connects Slots 0, 1, and 2 together.

Figure 9 is a configuration of the Processor Chassis. It is viewed from the Display Panel side, and correlates applicable cables to the associated Processor connectors.

5.2 15 Inch Expansion Chassis

The 15 inch Expansion Chassis contains eight universal expansion slots which can accept combinations of single board peripheral controllers, system modules, selector channels, or user designed interfaces. Included with this chassis are the cooling fans and interconnecting cables. The chassis may be ordered with or without a power supply.

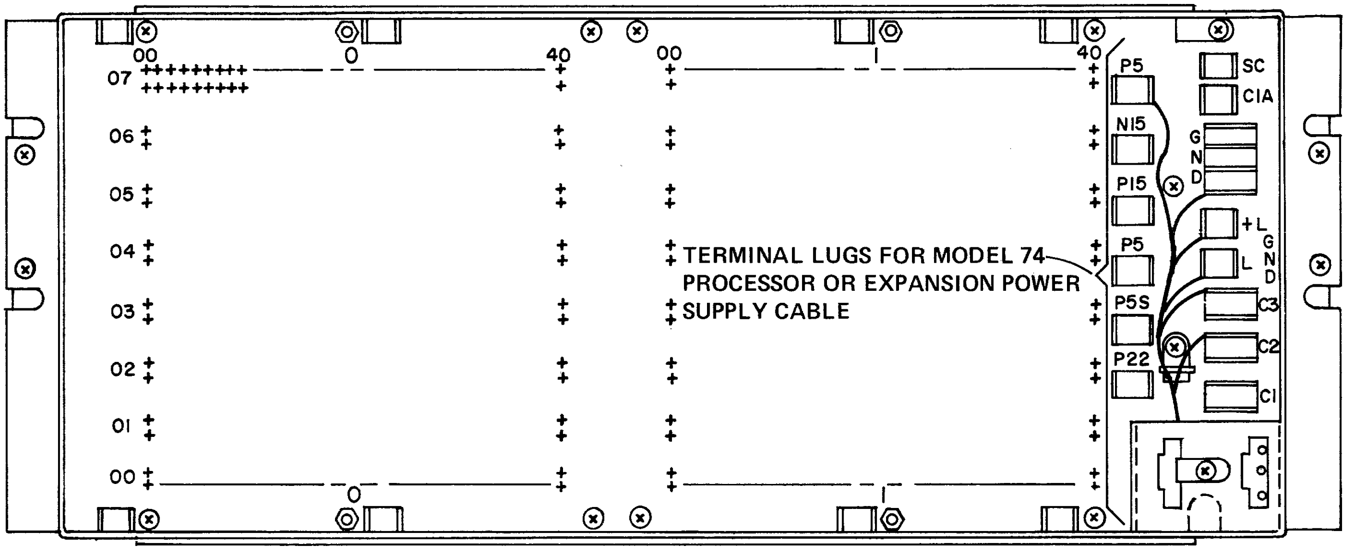
5.2.1 7 and 10 Inch Boards in a 15 Inch Chassis. A 10 inch I/O Controller (provided it does not use Connector 1) may be inserted into a 15 inch chassis via the 02-234 I/O Adapter Kit. (See Figure 10.) One or two 7 inch boards (halfboards) may be inserted into a 15 inch chassis via the 16-398 Half Board Adapter Kit (see Figure 11.) The Half Board Adapter Kit may hold two active 7 inch boards or one active and one blank 7 inch board, depending on requirements. No wiring takes place between the boards and the adapters. The adapters are designed such that the connectors on the boards plug directly into the Expansion Chassis.

5.3 10 Inch Expansion Chassis

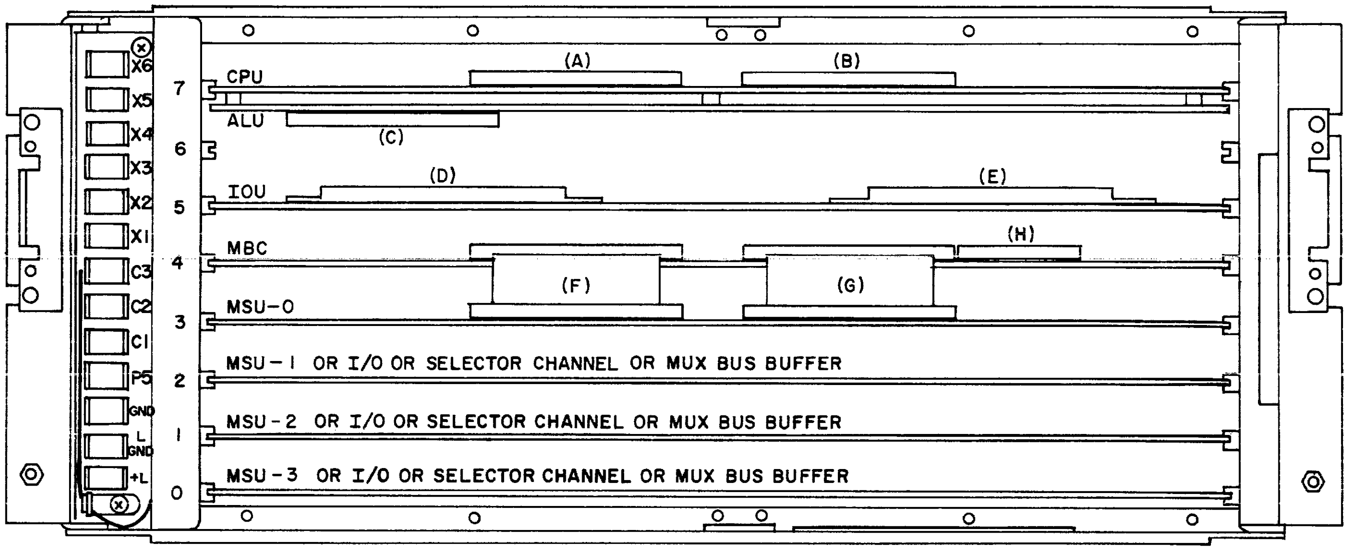
The 10 inch Expansion Chassis contains six 10 inch I/O expansion slots which can accept any combination of up to six 10 inch wire-wrap or copper peripheral controllers, systems, modules, or user designed interfaces. Included with the chassis are the cooling fans and system interconnecting cables. The Power Supply is separate.

6. DISPLAY PANEL INSTALLATION

The Model 80 Display Panel is electrically tied to the Processor via a connector and Faston lugs. The connector is installed on Connector 3 of the IOU board (35-405) and the terminal lugs mate into a terminal strip on the left side of the Processor Chassis. The terminal lugs are identified at the Faston connector and are mated to their corresponding terminal pin (C1, C2, etc.) on the chassis. See Figure 9. The Display Console is physically mounted to the brackets provided on the Processor Chassis. The 1 3/4 inch Filler Panel is mounted directly below the Display Console on the same chassis. Refer to Figure 8.


00
0
40
00
I
40
07
06
05
04
03
02
01
00
0
I
P5
N15
P15
P5
P5S
P22
SC
C1A
GND
+L
L
GND
C3
C2
C1
TERMINAL LUGS FOR MODEL 74 PROCESSOR OR EXPANSION POWER SUPPLY CABLE

Rear View


X6
X5
X4
X3
X2
X1
C3
C2
C1
P5
GND
L GND
+L
7
6
5
4
3
2
1
0
CPU
ALU
IOU
MBC
MSU-0
MSU-1 OR I/O OR SELECTOR CHANNEL OR MUX BUS BUFFER
MSU-2 OR I/O OR SELECTOR CHANNEL OR MUX BUS BUFFER
MSU-3 OR I/O OR SELECTOR CHANNEL OR MUX BUS BUFFER
(A)
(B)
(C)
(D)
(E)
(F)
(G)
(H)

Front View

MODEL 80 PROCESSOR CHASSIS CONFIGURATION			
CONNECTOR	CABLE	FUNCTION	TYPE
(A) CPU-3	DCS OR TEST SET	ROM ADDRESS	RIBBON
(B) CPU-2	DCS OR TEST SET	ROM DATA	RIBBON
(C) ALU-2	TEST SET	TEST	RIBBON
(D) IOU-3	17-152 ASSEMBLY (P/O 09-051)	DISPLAY	BUNDLED WIRE
(E) IOU-2	17-180	TTY	BUNDLED WIRE
(F) MBC-4 to MSU-3	17-191F01	(16KB) MEMORY INTERCONNECT	RIBBON
	17-191F02	(32KB) MEMORY INTERCONNECT	RIBBON
	17-191F03	(48KB) MEMORY INTERCONNECT	RIBBON
	17-191F04	(64KB) MEMORY INTERCONNECT	RIBBON
(G) MBC-3 to MSU-2	17-212F01	(16KB) MEMORY INTERCONNECT	RIBBON
	17-212F02	(32KB) MEMORY INTERCONNECT	RIBBON
	17-212F03	(48KB) MEMORY INTERCONNECT	RIBBON
	17-212F04	(64KB) MEMORY INTERCONNECT	RIBBON
(H) MBC-2	17-192	MEMORY PROTECT	RIBBON

Figure 9. Model 80 Processor Chassis Configuration (Front of Chassis)

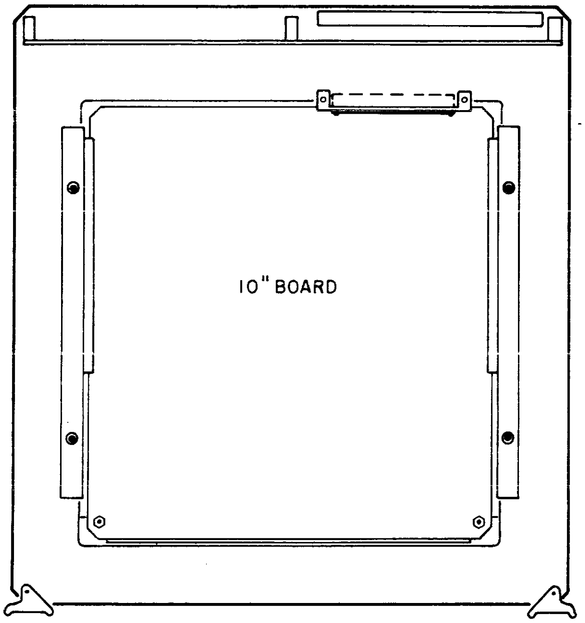


Figure 10. 02-234 I/O Adapter (Top View)

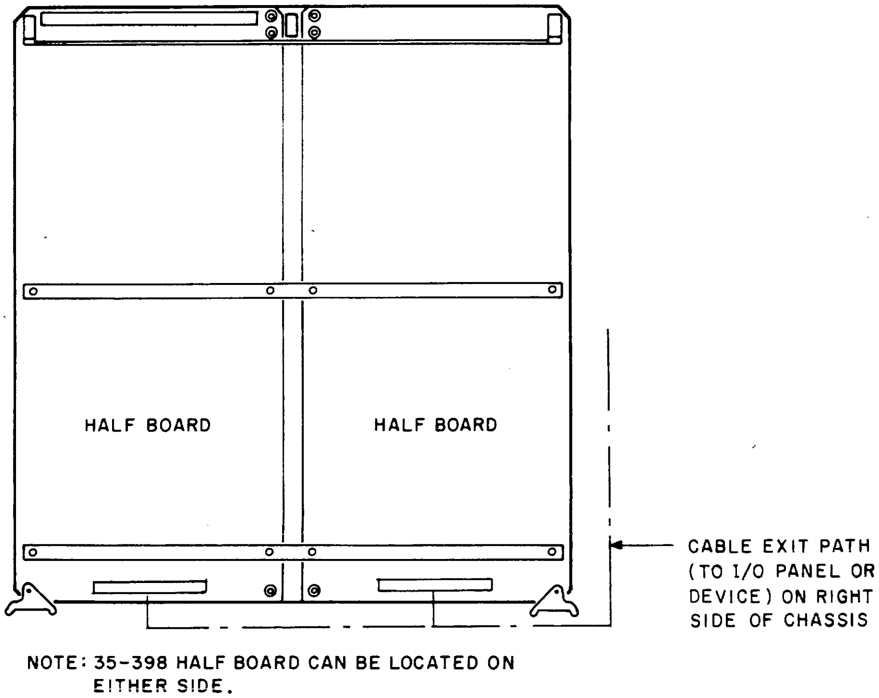

HALF BOARD
HALF BOARD
CABLE EXIT PATH (TO I/O PANEL OR DEVICE) ON RIGHT SIDE OF CHASSIS
NOTE: 35-398 HALF BOARD CAN BE LOCATED ON EITHER SIDE.

Figure 11. 16-398 Half Board Adapter

7. MEMORY INSTALLATION AND EXPANSION

The Memory Bus Controller (MBC) must be installed in Slot 4 of the Processor card file. All Memory Storage Units (MSUs) are installed in adjacent slots in this chassis. See Figure 9. Processor Card File Slots 0, 1, and 2 may also be used for I/O controllers, an MBFR, or a Selector Channel. Note, however, that using these slots reduces the maximum permitted memory size.

8. CONFIGURATION

8.1 System Expansion Chassis

When configuring a multi-chassis system, there are four rules that must be followed:

1. The System Expansion Chassis must be mounted below the basic Processor chassis.
2. All chassis must be contiguous.
3. All 15 inch System Expansion Chassis must be mounted above any 10 inch System Expansion Chassis.
4. Multiboard peripheral device controllers (on 10 inch circuit boards) can only be used in the 10 inch system expansion chassis.

8.2 Circuit Board Distribution

Model 80 Digital Systems may be configured in a variety of ways. However, the following factors must be considered when determining circuit board distribution within the basic Processor and the System Expansion Chassis. See Figure 12.

1. The Selector Channel can be placed in Slot 0, 1, or 2 of the Processor Chassis, or Slots 6, 4, 2, or 0 of the System Expansion Chassis. Only one Selector Channel may be contained in the basic Processor.

2. In the System Expansion Chassis, all contiguous slots on Connector 1 below the position where the SELCH is inserted become SELCH Bus slots. (This only applies within the chassis containing the SELCH.) The SELCH Bus extends down the left side connectors (front view). Note that all device controllers on 10 inch adapter boards connect to the Multiplexor Bus from the right side connectors (front view). Therefore, these device controllers may be inserted in vacant SELCH Bus slots, but will not be on the SELCH bus. This also applies to all 7 inch boards on adapters, installed on the right side. In the Processor Chassis, Connector 1 of Slots 0, 1, and 2 becomes the SELCH Bus when the SELCH is in any of the 3 slots.

3. The SELCH Bus can be extended by cable to any even numbered slot in an I/O chassis adjacent to the chassis containing the SELCH controller.

4. All device addresses are hard-wired on the device controller cards, (device addresses may be changed at option) so that the distribution of I/O device controllers in the chassis normally need only be considered as a matter of priority in the RACKO/TACKO "daisy-chain" and convenience.

5. The 15 inch System Expansion Chassis, and the basic Processor chassis may only be used for single board I/O device controllers unless the interconnection between boards takes place via cables installed on the outer edge of the board. No back panel stitch pattern is provided. For multi-board 10 inch device controllers, the 10 inch System Expansion Chassis must be used.

6. Priority is established by the physical placement within a chassis. Priority for interrupt driven devices should normally be established in order of descending speed, i.e., drum higher than magnetic tape, and card reader higher than a paper tape reader, etc.

7. The Multiplexor Bus Buffer (MBFR) may be installed in the Processor Chassis or Systems Expansion Chassis in any slot that can be used by the SELCH. This creates a Buffered Bus on Connector 1 where the SELCH created a SELCH Bus. (See items 1, 2, and 3 above.) Only one MBFR may be contained in the Processor Chassis. When an MBFR is housed in the Processor Chassis, the Processor SCLRO line must be removed from Connector 1 as this signal is regenerated on the MBFR card. In the System Expansion Chassis, the bus on Connector 1 may be cut into up to five separate sections to accommodate several SELCH and/or MBFR combinations. Each section can be cabled to another chassis and the 2 slot sections can also handle a SELCH or Buffered MUX controller.

NOTE

Connector 1 on Slots 0, 1, and 2 of the Processor Chassis is a common copper bus that cannot be cut. Only a single SELCH or MBFR can be installed in the Processor Chassis.

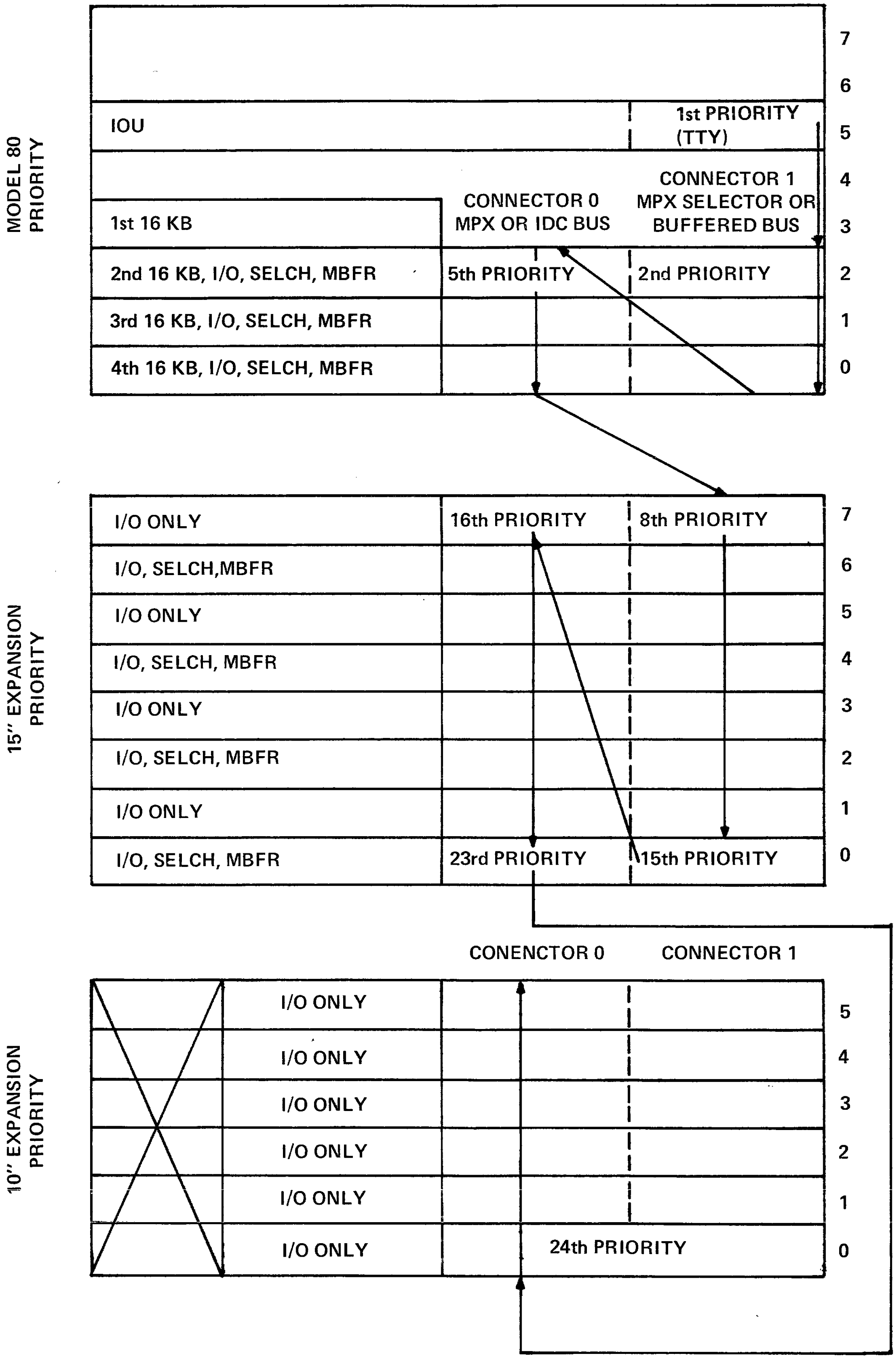

MODEL 80
PRIORITY
IOU
1st PRIORITY (TTY)
CONNECTOR 0 MPX OR IDC BUS
CONNECTOR 1 MPX SELECTOR OR BUFFERED BUS
1st 16 KB
2nd 16 KB, I/O, SELCH, MBFR
5th PRIORITY
2nd PRIORITY
3rd 16 KB, I/O, SELCH, MBFR
4th 16 KB, I/O, SELCH, MBFR
7
6
5
4
3
2
1
0
15" EXPANSION
PRIORITY
I/O ONLY
16th PRIORITY
8th PRIORITY
I/O, SELCH,MBFR
I/O ONLY
I/O, SELCH, MBFR
I/O ONLY
I/O, SELCH, MBFR
I/O ONLY
I/O, SELCH, MBFR
23rd PRIORITY
15th PRIORITY
7
6
5
4
3
2
1
0
CONENCTOR 0
CONNECTOR 1
10" EXPANSION
PRIORITY
I/O ONLY
I/O ONLY
I/O ONLY
I/O ONLY
I/O ONLY
I/O ONLY
24th PRIORITY
5
4
3
2
1
0

Figure 12. System Chassis Configuration and I/O Priority

8.3 Back Panel Wiring

The Acknowledge Control Line from the Processor carries the Interrupt acknowledge (ACK) signal. This line breaks up into a series of short lines to form the "daisy-chain" priority system. The ACK signal must pass through every controller that is equipped with Interrupt Control circuits. Refer to Figure 12 to determine order of priority. Back Panel wiring for interrupt control at a given position is: The Received ACK (RACKO) at Pin 122-1 and the Transmitted ACK (TACKO) at Pin 222-1. The daisy-chain bus is formed by a series of isolated lines which connect Terminal 222-1 of a given I/O position to Terminal 122-1 of the next position (lower priority). On unequipped positions, a jumper shorts 122-1 and 222-1 of the same connector to complete the bus. Back Panels are wired with jumpers from 122-1 and 222-1 must be removed from the Back Panel at that position.

On the IOU board location in the Processor Chassis, the daisy-chain starts at Terminal 220-0 (Slot 5) and normally goes to the Console TTY RACKO, Terminal 238-1 of the same slot. The TTY TACKO (239-1) is wired to Pin 122-1 at Slot 2 and continues through the I/O slots as described previously.

For controllers that occupy several positions, the jumper is removed only at the position where the controller board has ATN/ACK circuits. For details on the various devices, see the appropriate installation specification.

The Multiplexor Channel (I/O Bus), generated by the IOU Board, appears on Connector 0 of the Processor Chassis. It is connected to the copper wiring pattern on Connector 1 by the 17-183 cable. This cable is omitted when the SELCH or MBFR is installed in the Processor Chassis; Connector 1 then has the SELCH or Buffered Bus as the case may be. Connector 1 in Slots 00, 01, and 02 also has unidirectional DMA data busses which are wire wrapped together to form the bi-directional MSD Bus for the memory DMA port. See Figure 13.

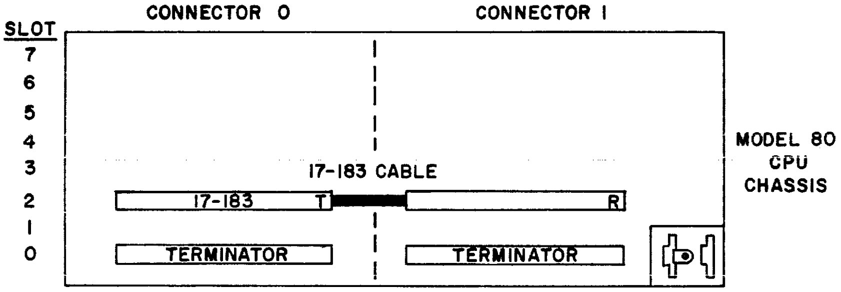


Figure 13. Multiplexor/SELCH Bus Cabling

8.4 System Configuration

System configuration data is provided in the User's Manual, Publication Number 29-261. Typical Configurations are shown in Figure 9.

8.5 Terminators

The termination end of both legs, Connector 0 and 1, of the Multiplexor Bus must have a standard INTERDATA termination card (35-433) installed. These cards are installed on the back panel at the lowest numbered slot of both connectors of the Multiplexor Bus that exists. For example, if a Selector Channel or Bus Buffer is installed in Slot 4 on the first expansion chassis and only the Processor Chassis and one expansion chassis is used in the system, the Multiplexor Bus must be terminated at Slot 0, Connector 0; and Slot 5, Connector 1 of the expansion chassis. In addition, the Buffered Bus or the SELCH Bus should be terminated at Slot 0 and Connector 1 of this chassis.

Depending upon system configuration, any SELCH Bus or Buffered Bus may be terminated by a 15 inch Terminator (35-433) or a 10 inch Terminator (35-434). The choice of terminators depends on the type of chassis in which the last slot of the Bus is present.

8.6 Power Supply Configuration

The 34-015 logic power supply is capable of supplying 50 A of +5 VDC and can be used to drive the Processor and up to two Expansion Chassis at 115 VAC or the basic Processor Chassis and one Expansion Chassis at 230 VAC. The 34-015 and 34-012 supplies may be mixed as described for I/O expansion to reach an optimum power match to any configuration.

9. CABLES

9.1 Power Cable

The standard INTERDATA Cabinet is wired for 20 Amp service. On the main power cable (part of the AC Distribution Panel), the 20 Amp UL plug has one blade perpendicular to the other. A three wire, grounding, 20 Amp, 125 VAC receptable (Hubbel #5362 or equivalent) is required to accept this plug.

9.2 System Expansion Cable

A number of standard cables are available for configuring systems made up of the INTERDATA expansion chassis discussed in Section 4. The choice of cables is dependent upon system configuration. The following cables are available:

1. 17-162 and 17-163: I/O and Memory Expansion Cable

This cable is used to connect the "0" connector field (17-162) and the "1" connector field (17-163) from the Processor to the corresponding connector in the first 15 inch expansion file. The expansion file must be mounted immediately below the basic Processor as these cables contain the DMA bus which is restricted to the first 15 inch expansion.

These cables are always used in pairs.

2. 17-193: I/O Expansion Cable, Connector "0"

This cable is used to connect the "0" connector field between two adjacent 15 inch card files.

3. 17-194: I/O Expansion Cable

This cable is used to connect the "1" connector I/O fields between two adjacent 15 inch card files.

4. 17-216: I/O Expansion Cable, 36 inch Long

This is a 36 inch long cable. It can be used to connect two 15 inch files that are not adjacent.

It must not be used to extend the basic Processor Mux Bus.

It can be used to extend a buffered bus or a SELCH Bus. It plugs into a "1" side connector. The "receiving" end can plug into the "0" or "1" side of the expansion file.

5. 17-214: 15 Inch to 10 Inch Expansion Cable

This cable is used to connect the "0" connector field of a 15 inch card file to a lower adjacent 10 inch card file. It provides an 8 bit I/O bus to the 10 inch card file.

6. 17-166: 15 Inch to 10 Inch I/O Expansion Cable, 36 Inch Long

This cable is used to connect the "1" side of a 15 inch expansion file to a 10 inch expansion file. It provides an 8 bit I/O bus to a 10 inch card file.

It must not be connected to the basic CPU Multiplexor Bus.

It may be driven either by a Selector Channel or a Bus Buffer.

It can be used on the older 10 inch card file, 13 I/O Slots with cards mounted vertically.

7. 17-183: "0" to "1" Connector

This cable can be used to interconnect the "0" field and the "1" field within a 15 inch card file.

It can also be used to connect a "0" side (slot "0") of a file, to the "1" side (slot 7) of the next adjacent file, or vice versa.

8. 17-215: 10 Inch to 10 Inch I/O Expansion Cable

This cable is used to connect 2 adjacent 10 inch card files.

9.3 Typical Configurations

Information Drawing 01-051R03C12 depicts cabling for typical configurations.

10. TESTING

10.1 Standard Test Software

The following software is supplied with the basic Processor to insure that the System is operational:

1.	Processor Test Program	06-106
2.	Memory Test Program	06-003
3.	Floating Point Test	06-108
4.	TTY Test Program	06-004
5.	Memory Hold Test	06-143

10.2 Additional Software

In addition to the test software mentioned above, appropriate test software is supplied with each peripheral. When the system is equipped with the memory parity option, software package 06-144 is provided. The purpose of this routine is to initialize the memory to correct parity when power is initially applied or interrupted to the volatile semi-conductor Memory.

NOTE

> Failure to initialize the complete memory to correct parity may result in erroneous parity errors even where correct parity is contained in the memory locations being referenced because of the "look-ahead" nature of the Model 80 Memory. Use MOS Parity Initialize Program 06-144.

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MAINTENANCE SPECIFICATION

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MODEL 80
MAINTENANCE SPECIFICATION

1. INTRODUCTION

The INTERDATA Model 80 Digital System is a low cost, general purpose system, versatile enough to perform a wide range of industrial control, data processing, and scientific computation. The Model 80 is well suited to the real-time scanning of hundreds of instrument readings, process alarms, and pulse trains. It is particularly useful where larger amounts of main processor time are needed for computation.

1.1 Packaging

The Model 80 Processor is contained in a 19 x 7-1/2 inch RETMA card file allowing eight card positions. The basic Processor with 16KB of semiconductor memory uses five card positions and allows three positions for I/O expansion. One additional card position is used for each 16KB of memory added to the basic configuration, so that the basic Processor with 64KB of memory uses the entire chassis.

1.2 Processor

The Processor is available in two basic configurations, that is, Model 80 with 16,384 byte MOS memory (8,192 x 16 bit words) (Product Number M80-000) and Model 80 with 16,384 byte MOS memory and parity (8,192 x 17 bit words) (Product Number M80-001).

The Processor consists of a double card assembly CPU/ALU (Central Processing Unit/Arithmetic Logic Unit) and an I/O card which generates the I/O Bus and contains the Display Panel controller and Teletype controller.

The Model 80 uses a technique commonly referred to as "emulation" to implement the standard INTERDATA user repertoire. This technique requires a micro-processor, or sub-processor, not apparent to the user, employing one or more of its micro-instructions in sequence to implement one user level instruction.

The Model 80 employs a 32-bit micro-instruction word and 16-bit internal bussing. The basic instruction time of the micro-processor is 200 nanoseconds/instruction. User level instruction execution times are typically 530 nanoseconds for Register to Register (RR) and Register to Storage (RS) type instructions and 1010 nanoseconds for Register to Indexed Memory (RX) type. The basic micro-program is contained in 1,024 words of Read-Only-Memory (ROM).

1.3 Main Memory

The main memory uses MOS/LSI devices for storage. It has an effective access time of approximately 280 nanoseconds. Memory banks can be accessed via the Processor or through an external Direct Memory Access Port (DMA). The external port has a throughput of approximately 5.4 megabytes/second or it may be used as a multiplexed port by up to four devices at a maximum throughput of 4.25 megabytes/second. The packaging consists of a single 15 inch memory controller and one to four storage modules of 16K bytes each, cabled directly to the controller. The DMA connection is via the back panel. The DMA port accommodates the Selector Channel in the multiplexed configuration.

1.4 Control Store

The basic Model 80 uses 1,024 words of ROM control store which is mounted on the ALU board. The control store may be expanded by another 3,072 words of either the Dynamic Control Store (DCS) or ROM by adding additional circuit boards. Three new user instructions are added for manipulating the DCS.

1.5 Power Supply

The volatile semiconductor main memory of the Model 80 is powered by a separate supply that includes built-in battery backup for short term power interrupts and a low power standby mode when the system is shut down. The internal battery is capable of holding the memory's contents, in the low power non-operating mode, for several minutes. For long term memory protection, an external battery or customer supplied 115/230 VAC (±20% at 47-63Hz) can be used.

The memory goes into the low power stand-by mode whenever the Processor is shut down. It does not use the battery or the reliable AC source, however, except on a Primary Power Failure (PPF). The memory power is not controlled by the front panel power switch.

The Model 80 Processor and I/O employ a power supply separate from that of the semiconductor memory.

1.6 Peripherals

The Model 80 interfaces to, and is compatible with, all standard INTERDATA peripheral controllers and controllers designed to the standard INTERDATA Multiplexor Bus. Any number of devices up to 255 can be accommodated, but a maximum of 9 can be interfaced directly to the Multiplexor Bus or to the Selector Channel Bus.

2. INTERNAL ARCHITECTURE

The architecture of the Model 80 encompasses a principle of modules communicating over a common bussing system, directed by instructions from a control memory which specify the module to which an instruction is directed and the function to be performed. In theory, the function of any module is arbitrary and the significance of various instructions take meaning only when applied to a specific module. Thus, a computer achieves a capability and personality determined by what functions can be performed by its complement of modules.

2.1 Modules

The Model 80 accommodates eight modules which communicate over four Processor busses. The basic Processor is comprised of three modules.

1. Central Processing Unit (CPU). The CPU contains the Processor registers. This module controls the user memory, control memory, register gating, and sequencing of instructions.
2. Arithmetic Logic Unit (ALU). The ALU provides the basic arithmetic/logical capability of the Processor. It is capable of 24 instructions including multiply/divide and multiple precision shifting.
3. Input/Output Unit (IOU). The IOU provides the I/O capability of the Processor by generating the standard INTERDATA Multiplexor (I/O) Bus for peripheral communications. In addition, it is capable of various byte manipulations of data presented on the busses.

The architecture accommodates five additional arbitrary modules such as floating point, boolean manipulators, or special nature designs.

2.2 Micro-Instructions

The micro-instruction word is 32-bits long. In addition to the branch and write instructions, there are three types of instructions to the modules. These minimally encoded instructions provide 112 combinations of module/function commands. The micro-instruction can simultaneously direct two operands and a result independently on three of the computer's busses; generate 12-bit immediate field operands; select the address of the next micro-instruction; perform non-encoded micro control of the computer's functions such as reading/writing main memory; incrementing user location and memory address registers; controlling the user status register; and decoding the next user instruction.

2.3 Interrupts

The Model 80 has eight hardware priority interrupts, most of which can be masked by various bits of the Program Status Word (PSW). The occurrence of a recognized interrupt causes the micro-program to trap one of eight specific control store locations associated with the interrupts.

2.4 Registers

The Model 80 has 16 general registers, 15 of which may be used as index registers. In addition, there are eight additional general purpose registers, plus five registers associated with the user level machine control that are available to the micro-programmer.

2.5 Processor Timing

Communications between modules is request/response. Timing is completely asynchronous (rather than quantized) to achieve maximum speeds. In addition, interlocks are provided between the control memories and the CPU to facilitate programming the micro machine. The control module operates on a 10MHz clock, allowing a minimum instruction execution in 200 nanoseconds. Internal timing within the other modules can be selected to best suit the needs of the module.

3. FUNCTIONAL DESCRIPTION OF THE BASIC PROCESSOR

3.1 Processor Busses

The functional characteristics of the Processor can best be described in terms of its registers, busses and related gating. There are four busses which are the key to the modular design philosophy of the Model 80 architecture. Refer to Figure 1. An understanding of the bus structure is necessary to determine how each module of the Processor interrelates, and how the registers and gating of each module contributes to the function of the module it is designed to serve.

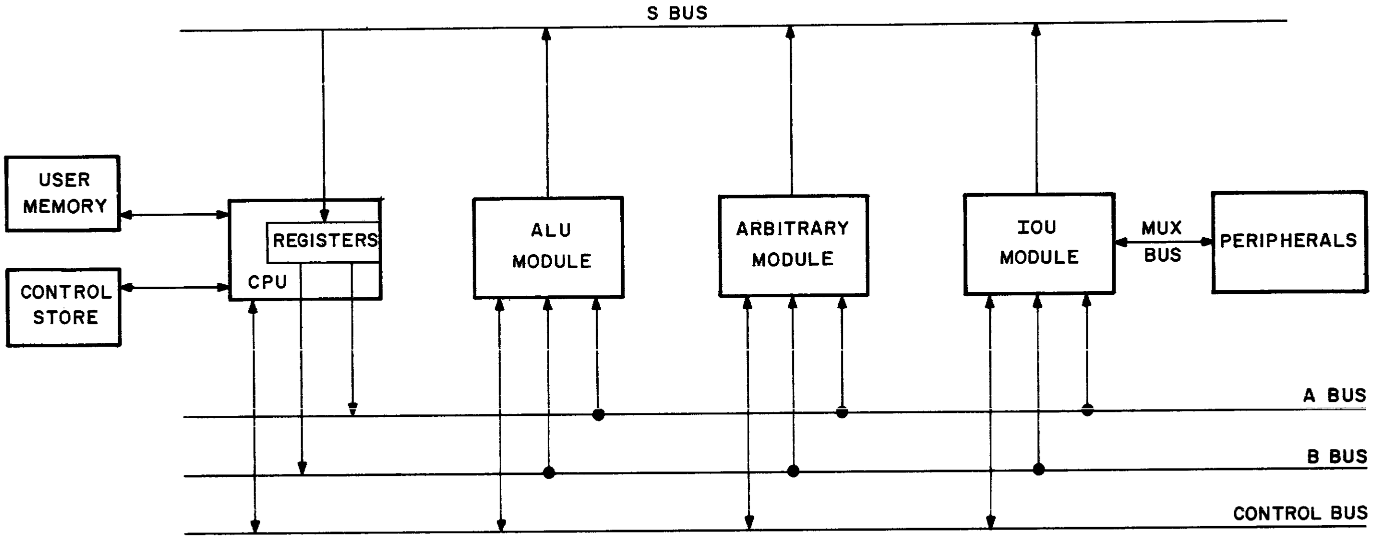


Figure 1. Model 80 Module Concept

3.1.1 Control Bus. The Control Bus of the computer is commanded by the control module and is, in essence, a reflection of that segment of the micro-instruction selecting the function and module to be addressed, plus timing to effect data transfers. Also included is a means for a module to transfer data to the Condition Code of the PSW. The Control Bus signals are described in the following paragraphs:

Module Select Lines (MDSEL0:2). These three lines contain the address of a module for which the current micro-instruction is intended. One of the eight arbitrary modules can be selected by the instruction to perform some function. These three lines reflect Bits 0:2 of the micro-instruction.

Function Select Lines (FSEL0:3). These four lines reflect Bits 16:19 of the micro-instruction and normally select 1 of 16 arbitrary functions to be performed by the selected module.

Start (STRT). STRT signals the modules that data on the busses is valid. It is, in effect, a request from the control module for a response to a micro-instruction. Data is held static on the A and B Busses while STRT is active. The control module holds STRT active until it recognizes a response from the module (MFIN) and has stored the results presented on the S Bus.

Module Finished (MFIN). MFIN is a response to the control module from a selected module indicating that it has recognized STRT and completed the selected function. The selected module gates data and other responses onto the S Bus prior to returning MFIN. The data and responses must be held on the busses until the control removes STRT. This time is indefinite and depends on events within the control module.

Module Signal (MSIG). This is a control signal manipulated by the selected module to indicate some arbitrary condition to the control module. It may be tested by the control module during a normal micro-instruction to the selected device, to control a conditional branch in the micro-program.

Condition Code Bus (SCC, VCC, CCC, GCC, and LCC). SCC signals the control module that the selected module wishes to mainpulate the Condition Code of the Program Status Word. If the micro-programmer has enabled this manipulation, the Condition Code is forced to a status specified by the selected module. The status is unconditionally forced into the CPU flags. This is done concurrent with a normal instruction to the selected module. VCC, CCC, GCC, and LCC specify the status forced into CPU flags and the Condition Code of the Program Status Word and represent overflow, carry, greater than, and less than respectively.

3.1.2 A, B, and S Busses. The A, B, and S Busses are the primary data links between the control and the selected module. Gating of data to/from each of these busses is controlled by the micro-instruction. Most of the registers of the control module can be gated to/from these busses.

Data is selected by the micro-instruction from two independent sources and transmitted to a selected module over the A and B Busses. The module is thus presented simultaneously with two operands. The resulting data is returned to the control module via the S Bus. The destination of the S Bus is selected by the micro-instruction.

3.1.3 Typical Bus Exchange. The use of the A, B, and S Busses can be summarized by the following example.

1. The micro-instruction selects a module (MDSEL0:2), and directs it to perform some function (FSEL0:3).
2. The operands are selected from somewhere in the control module and gated onto the A and B Busses.
3. The control module informs the selected module that all data on the busses is valid and that it may begin (STRT).
4. The selected module performs the function (S) = (A) F (B) and gates the results to the S Bus.
5. The selected module may manipulate the Condition Code via SCC, VCC, GCC, LCC, and CCC.
6. The selected module may signal, for example, that the result of the operation was zero by activating MSIG.
7. The selected module activates MFIN to signal the CPU module that the operation is complete and the results are presented on the S Bus.
8. The control module recognizes MFIN, gates the S Bus to the destination specified by the micro-instruction, and then removes STRT.
9. The selected module deactivates itself when STRT is removed.

3.2 Registers

The following registers are part of the control module although some may reside physically within the ALU.

3.2.1 A Stack/B Stack. The A stack and B stack are a redundant set of register banks containing the 24 general purpose registers of the CPU. The registers are duplicated to allow simultaneous gating of any register in the stack onto either the A Bus or the B Bus. Of these 24 registers, 16 are the user general registers, while the remaining 8 are available to the micro-programmer as desired. These registers are gated onto the A and B Busses and are loaded from the S Bus under control of the micro-instruction.

3.2.2 Memory Data Register (MDR). This register provides the data buffer between the CPU and the user level memory. The MDR can be gated onto the A and B Busses and loaded from the S Bus under control of the micro-instruction. It is, of course, also loaded under control of the memory when a memory read cycle is requested. Hardware interlocks are employed to synchronize the memory to the CPU.

3.2.3 Memory Location Register (MLC). The MLC is a general purpose register which can be gated to either the A or B Bus and loaded from the S Bus, but possesses additional characteristics intended to facilitate the emulation of the user level repertoire. This register can, under micro-control, be incremented by two, incremented by four, and jammed into the Memory Address Register (MAR). This register keeps track of the current instruction location of the emulated machine.

3.2.4 Memory Address Register (MAR). This register contains the address of the user memory that the micro-programmer is reading or writing. The MAR can be loaded from the S Bus under control of the micro-instruction, loaded from the MLC, or incremented by two or four under micro-control. The least significant bit of the MAR is used to control byte steering for the byte-oriented instructions of the user repertoire (refer to Section 4.6). As in the MDR, timing conflicts are resolved by hardware interlocks.

3.2.5 Program Status Word (PSW). The Program Status Word is a 16-bit register which may be gated onto either the A or B Bus and loaded from the S Bus under control of the micro-instruction. Various bits of the PSW are used to enable associated hardware interrupts. PSW Bits 12:15 contain the Condition Code of the user level computer. These bits may be compared and tested against corresponding bits of the user instruction under Module 0 micro-instructions to emulate user branch instructions. In addition, they can be manipulated by any module designed to do so, if they are enabled by the micro-programmer.

3.2.6 User Destination Register, User Source Register (UDR, USR). These two control registers store Bits 9:11 and 12:15 respectively, of the current user level instruction being emulated, and allow the micro-programmer to indirectly reference the general registers selected by the user instruction. The UDR is compared to the PSW Condition Code on certain micro-instructions to emulate user level branches. These registers can be examined by gating them onto the A and B Busses under micro-instruction control. The UDR can also be loaded from the S Bus.

3.2.7 User Instruction Register (UIR), Memory User Destination Register (MUDR), and Memory User Source Register (MUSR). These three registers are loaded with Bits 0:7, 8:11, and 12:15 respectively, of the next user level instruction to be emulated. The eight bit op-code stored in the UIR is used to vector to the emulation sequence for the next user instruction. It is also used to interrogate a ROM which has been configured to decode privileged and illegal user level instructions. The contents of the MUDR and MUSR are transferred to the UDR and USR at the beginning of the next emulation.

3.2.8 ROM Location Register (RLR). This register stores the current address of the control store instruction. It is loaded from the ROM Address Gates (RAG) at the beginning of every instruction except interrupt trap instructions and execute type instructions (explained in the section on micro-programming). The RLR is a 12-bit register allowing direct addressing of the control store up to 4K instructions.

3.2.9 ROM Instruction Register (RIR). This 32-bit register stores the current micro-instruction. The RIR is the focus of control of the CPU.

3.2.10 A Latch/B Latch. The A latch and B latch registers latch the data presented by the control module onto the A and B Busses. They are the data sources for these busses.

3.3 Interrupts

The hardware of the computer provides eight priority interrupts. Each interrupt has a unique trap location associated with it. Recognition of an interrupt causes the instruction stored at its respective trap location to be performed. The RLR contents are preserved to allow the address of the interrupted sequence to be saved, if desired, so that control can be returned at the completion of the interrupt routine. Certain interrupts are enabled/disabled by bits of the PSW.

3.4 Control Store Memory

The Model 80 can accommodate a maximum of 4K x 32 bits of control store memory. The computer allows data as well as instructions to be retrieved from its control memory. This capability expands its versatility by allowing data such as sine tables, translation tables, and matrices to be stored and operated upon efficiently by the micro-programmer.

On models so equipped, the Processor can alter its control store (write into its memory). This capability to store and retrieve data provides the power of a hardware computer at micro-instruction speeds.

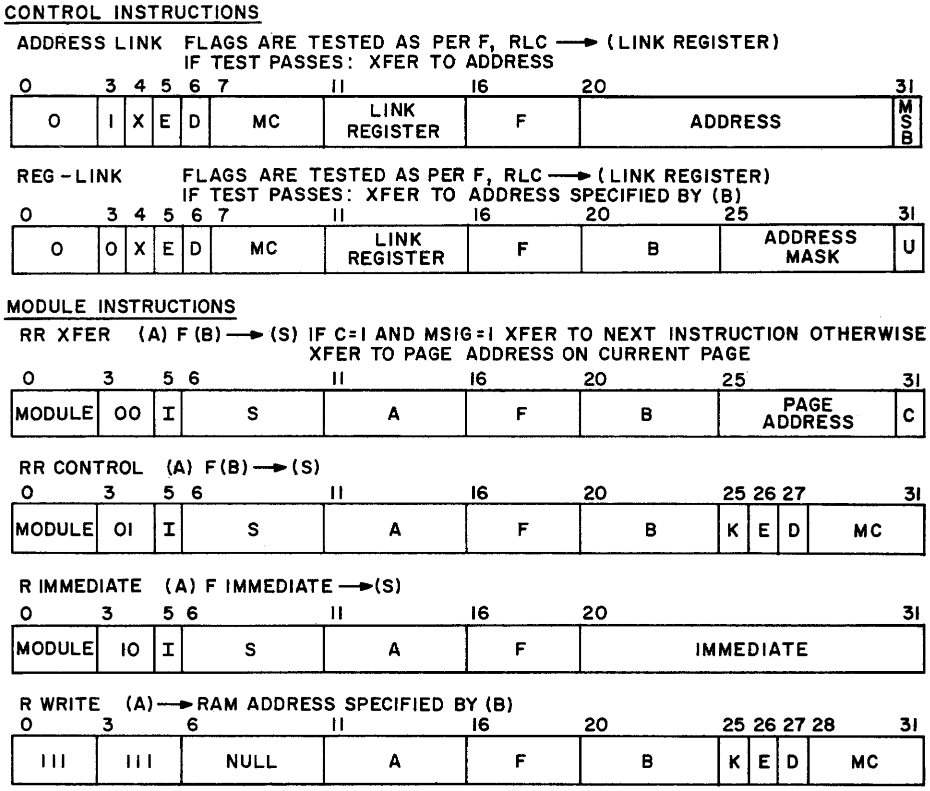
3.5 Microprogramming

The control store of the Model 80 is a 32-bit word memory which may be read indirectly by an instruction to retrieve data, and may be written into by an instruction if it is a writable memory. The basic Model 80 contains a 1,024 x 32 ROM array containing the user repertoire and support programs.

The basic instruction format provides the computer with a three address capability, but various options of the repertoire can modify this to range from two to four. Figure 2 displays the different types of instructions and their modifiers.

The format of the micro-instruction specifies which module is to be addressed, allowing only one module of the computer to be addressed at any one time. All other modules must ignore the communications in process. Bits 0:2 of the instruction selects the module to which the instruction is addressed.

3.5.1 Module 0. Module 0 addresses the control module. As shown in Figure 2, instructions are interpreted differently for Module 0 than the others. In the normal sequence of instructions (e.g., no branches), the hardware of the control module controls the reading of its memories, and gates the registers specified by the instruction. When it is addressed by an instruction, it is for the purpose of a conditional transfer. Module 0 does not manipulate the condition code or Processor flag register.


CONTROL INSTRUCTIONS
ADDRESS LINK FLAGS ARE TESTED AS PER F, RLC ⟶ (LINK REGISTER)
IF TEST PASSES: XFER TO ADDRESS
0 3 4 5 6 7 11 16 20 31
0
I
X
E
D
MC
LINK REGISTER
F
ADDRESS
MSB
REG - LINK FLAGS ARE TESTED AS PER F, RLC ⟶ (LINK REGISTER)
IF TEST PASSES: XFER TO ADDRESS SPECIFIED BY (B)
0 3 4 5 6 7 11 16 20 25 31
0
0
X
E
D
MC
LINK REGISTER
F
B
ADDRESS MASK
U
MODULE INSTRUCTIONS
RR XFER (A) F (B) ⟶ (S) IF C=I AND MSIG=I XFER TO NEXT INSTRUCTION OTHERWISE XFER TO PAGE ADDRESS ON CURRENT PAGE
0 3 5 6 11 16 20 25 31
MODULE
00
I
S
A
F
B
PAGE ADDRESS
C
RR CONTROL (A) F(B) ⟶ (S)
0 3 5 6 11 16 20 25 26 27 31
MODULE
01
I
S
A
F
B
K
E
D
MC
R IMMEDIATE (A) F IMMEDIATE ⟶ (S)
0 3 5 6 11 16 20 31
MODULE
10
I
S
A
F
IMMEDIATE
R WRITE (A) ⟶ RAM ADDRESS SPECIFIED BY (B)
0 3 6 11 16 20 25 26 27 28 31
111
111
NULL
A
F
B
K
E
D
MC

A	SELECTS REGISTER GATE TO A BUS
B	SELECTS REGISTER GATED TO B BUS
S	SELECTS REGISTER TO RECEIVE S BUS
F	SELECTS FUNCTION OF ADDRESSED MODULE
E	ENABLE SETTING OF CONDITION CODE
C	IF SET TRANSFER IS CONDITIONAL
X	EXECUTE
I	B FIELD IS INDIRECT ADDRESS OF DATA
D	DECODE NEXT INSTRUCTION
K	FSEL EXTENSION
U	UNUSED

MC FIELD DESIGNATIONS (MEMORY CONTROL)

00XX	NO MEMORY ACTION
01XX	INSTRUCTION READ
10XX	DATA READ
11XX	DATA WRITE
XX00	NO REGISTER ACTION
XX01	INCREMENT MAR BY TWO *
XX10	INCREMENT MAR AND MLC BY FOUR
XX11	JAM MLC TO MAR

* IF DONE IN CONJUNCTION WITH AN INSTRUCTION READ, THE MLC IS ALSO INCREMENTED BY TWO

Figure 2. Control and Module Instructions

Branch/Execute Instructions. There are two types of transfers recognized by Module 0. The most common is the branch. The Branch (BR) instruction conditionally transfers control of the CPU to a specified address of control memory and proceeds sequentially from there. The second type of transfer, commonly called an execute, transfers control to a single instruction at a specified address of control memory, then normally returns to the original sequence. Any type of instruction may be executed including additional execute instructions to any depth. However, an execute which results in a branch does not return to the continuing sequence. Bit 04 of the instruction determines whether the instruction is a branch or execute type.

Address Link/Register Link. There are two type of Module 0 instructions; address link and register link. They are selected by the state of Bit 03 of the instruction.

The linked transfer is similar in function to the user level Branch and Link (BAL) instruction, and can be used to transfer to subroutines when they may be entered from more than one location. The location of the next sequential instruction, following the transfer, is deposited in the register specified by the Link field of the instruction (Bits 11:15), and a transfer is conditionally executed to the effective address.

When the address link is selected, the transfer address is specified by Bits 20:30, and Bit 31 of the instruction. Bit 30 is the Least Significant Bit (LSB) and Bit 20 is the Most Significant Bit (MSB)-1. Bit 31 of Module 0 instructions is used as the MSB of the address and is implemented in this manner solely because of hardware dictation and should be of no practical concern to the micro-programmer working at the micro-assembler level.

The register link is used when the transfer address is contained in a register. In this instruction, a branch is taken to the location contained in the register specified by the B(3:14). Bits 25:30 of the instruction can be used to mask out these bits of the address contained in the B register. (i.e., If instruction Bits 25:30 are ONES, the B address is unaffected. If they are ZERO, the corresponding bits of the address, contained in the register specified by the B field, are forced to ZERO.)

Conditional Branches. All transfers are conditional upon a state selected by the F field of the instruction. By selective coding of the F field, either the Condition Code of the user level machine or the status of the CPU can be tested. The F field codes are:

F FIELD	MNEMONIC	OPERATION
0000	BALZ	Branch on CPU zero
0100	BALNZ	Branch on CPU not zero
0001	BALL	Branch on CPU less
0101	BALNL	Branch on CPU not less
0010	BALG	Branch on CPU greater
0110	BALNG	Branch on CPU not greater
0011	BALF	Branch if the logical product of user M1 field and PSW (12:15) is zero
0111	BALNF	Branch if the logical product of user M1 field and PSW (12:15) not zero
1000	BALC	Branch on CPU carry
1100	BALNC	Branch on CPU no carry
1001	BALV	Branch on CPU overflow
1101	BALNV	Branch on CPU no overflow
1010	BAL	Branch unconditional
1011	BALA	Arm interrupts and Branch
1110	BDC	Branch and mask console interrupt (no real branch is performed)
1111	BALD	Disarm interrupts and Branch

The control field of Module 0 instructions is discussed in Section 3.5.3.

3.5.2 Non-CPU Instructions. As stated previously, when the module number is not zero, the CPU does not operate on the instruction, and the fields are interpreted differently. The module field (Bits 0:2) and the F field (Bits 16:19) are interrogated individually by the other modules. There are four types of non-CPU instructions selected by Bits 3 and 4 of the instruction.

1. RRX. The RRX is a register-to-register and transfer instruction. It is effectively a four-address instruction in that it gives the register address of the two operands, the register address of the results, and the location for the next sequential instruction.

   The two operands are addressed by the A field (Bits 11:15) and the B field (Bits 20:24). The contents of these two registers are gated respectively to the A Bus and B Bus of the computer.

   The S field (Bits 6:10) selects the destination register to which the results are gated from the S Bus.

   The page address field (Bits 25:30) selects the low order address of the next instruction. The high order bits are taken from the current location address. The C field (Bit 31) being true makes the transfer conditional upon a signal returned by the addressed module at the completion of the instruction. (The ALU, for example, returns the Carry flag as its signal.) If the module signal, which is designated MSIG, is true, and Bit 31 of the micro-instruction is true, the branch does not occur, and the next sequential instruction is executed. Any other condition causes the transfer to be effected.

2. RRC. The RRC is a register-to-register control type instruction. The interpretation of the instruction fields is identical to that of the RRX, with the exception of Bits 25:31 which contained the page address within a RRX instruction. Bits 25:31 of the RRC instruction provide the micro-control of the CPU and are described in Section 3.5.3.

3. RIM. The RIM instruction provides an immediate field for ease of generating constants and bit masks. Immediate, is the term generally used to infer that the immediate contents is the actual operand rather than the address where the operand will be found. This 12-bit immediate field (RIR 20:31) is converted to a 16-bit operand by extending the sign bit (RIR 20) when gating onto the B Bus. The S field and A field of the instruction are interpreted identical to that of the RRX and RRC instructions.

4. RWT. The RWT is the store or write instruction of the repertoire if the CPU is equipped with a writable control store. There are several notable differences pertaining to this instruction.

   — Although the module number cannot be zero, it may be any other configuration, as the CPU never communicates with the other modules.

   — The S field is not interpreted and should be null selected.

   — The F field is not interpreted.

   — The B field addresses the register containing the address to be written into.

   — The A field addresses the register containing the data to be stored in memory.

   — The LSB of the control store address steers the data to the least/most significant half of memory (see Section 5.4).

   Bits 25:31 of the RWT instruction are interpreted as a control field, as in a RRC instruction.

3.5.3 Micro-Control (MC). To facilitate the emulation task of the CPU, certain instructions allow an order of micro-control within the CPU. The instructions possessing this capability are the Module 0, the RRC, and RWT instructions.

MC Field. The MC field is the user memory micro-control which allows various controls over the user memory instruction Location Counter (MLC), the user Memory Address Register (MAR), and the reading and writing of the user memory. The significance of the bits of the MC field are:

MC FIELD	CONTROL
00XX	No memory action
01XX	Instruction read
10XX	Data read
11XX	Data write
XX00	No register action
XX01	Increment MAR by two*
XX10	Increment MLC and MAR by four
XX11	Jam MLC to MAR

There are certain hardware connotations to the MC operations which are not made apparent by the above table.

1. MC 01XX informs the hardware that an instruction read will take place and cause the CPU to read the instruction location plus the next location in anticipation of a full word user instruction. This results in the second half of the user instruction becoming available in the user's Memory Data Register (MDR), and the first half being stored in the CPU hardware for the instruction emulation.

2. The instruction fetch is conditional when used within Module 0 instructions. The read memory is only effected if the operation does not result in a transfer. (This conditioning is used to expedite the emulation of the user branch instruction.)

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*If this combination is done in conjunction with an instruction read, (MC-0101), the MLC is also incremented by two.

3. All of the micro-control is effected before the STRT occurs with the exception of data read and data write. This control is effected after completion of the instruction, which allows the micro-programmer to use the MAR or MDR as a destination and begin a read/write data immediately. It also allows the execution of the increment and jam control and the addressing of the MAR as the destination register simultaneously, which has functional utility.

D Field (Decode Instruction). The D field bit informs the CPU to halt the sequential flow of micro-instructions and begin to emulate the next user instruction. The op-code field of the new user instruction is in the UIR and provides a vector to a control store address where the emulation sequence begins. This implies that the micro-programmer must have done an instruction read in the current or a prior instruction using one of the proper MC field designations. The execution of a decode is conditional when used within Module 0 instructions, and, like the instruction fetch, is only performed if the operation does not result in a transfer.

E. Field. This field is used to Enable (E) or disable changing of the Condition Code of the PSW. When changing is enabled, the Condition Code is changed under control of the module addressed until again disabled by this field. (The ALU, for example, jams its C, V, G and L flags into the Condition Code upon completion of its function.) The meaning of the Condition Code is a function of the module addressed. Flags are disabled at the beginning of an emulation sequence.

K Field. The K field of the micro-instruction is an extension of the F field of the instruction. It is available only on the RRC and RWT instructions and constitutes the control signal (KSIG) to the modules. Its meaning, just as the F field, is defined by the module addressed by the current RRC instruction. The ALU, for example, reinterprets shifts to be double precision when KSIG is active. It is also used to extend the functions of the I/O module.

3.5.4 Control Store Data Storage. Data may be retrieved from the ROM or the Dynamic Control Store (DCS) during execution of RRC, RRX or RIM instructions when the I field bit (instruction Bit 5) is true. When the I field bit is set, the data addressed onto the B Bus is used as the store address of the ROM or DCS, and causes the CPU to replace this data with the addressed data before signaling the addressed module to begin its task. The least significant bit of the B Bus selects either the right or left half of the data for replacement on the bus. This facilitates address calculations and packing of the DCS. The second LSB of the B Bus, therefore, addresses the LSB of the control store.

3.5.5 Interrupts. The hardware of the computer provides eight priority interrupts. Each interrupt has a unique trap location associated with it. Recognition of an interrupt causes the instruction stored at its respective trap location to be performed. The RLR contents are preserved to allow the address of the interrupted sequence to be saved, if desired, so that control can be returned at the completion of the interrupt routine. Certain interrupts can be disabled by bits of the PSW as designated in Table 1. In addition, all interrupts can be enabled/disabled as a group by a micro-instruction. All interrupts not masked by PSW bits are interrogated when a new user level instruction is decoded, regardless of the status of the group enable. The group enable is automatically disabled at the beginning of a user emulation, and must be enabled by instruction if the programmer wishes to recognize interrupts. The following table lists by priority the pertinent information for each interrupt. The external interrupts, 0, 1 and 2 cause an External Interrupt PSW swap.

TABLE 1. INTERRUPT PRIORITY

INTERRUPT	TRAP	MASK
Primary Power Fail	101_{16}	NONE
Machine Malfunction*	102_{16}	PSW 02
Display	103_{16}	NONE
External Interrupt 3 (Data Channel)	104_{16}	PSW 01
External Interrupt 2	105_{16}	PSW 10
External Interrupt 1	106_{16}	PSW 09
External Interrupt 0 (ATN0)	107_{16}	PSW 01
Illegal Instruction	100_{16}	NONE
Privileged Instruction	100_{16}	PSW 07

*This interrupt can have several causes and is discussed further in the I/O section.

3.5.6 Registers. The basic CPU has a register stack containing 16 user registers and 8 general purpose registers for use by the micro-programmer. In addition, the bulk of the remaining CPU registers are also available to the micro-programmer.

A register is available to the micro-programmer if he can address it to one or more of the internal busses. The following Table tabulates the addressable registers and their respective address on the designated bus. Also listed are register mnemonics and descriptions, and the register peculiarities.

TABLE 2. REGISTER ADDRESSING

BUS ADDRESS (HEX)	S BUS	B BUS	A BUS
00:0F (16 General Registers)	UGR	UGR	UGR
10:17*	RGR	RGR	RGR
18	PSW	PSW	PSW
19	MDR	MDR	MDR
1A	MLC	MLC	MLC
1B	MAR	YDP1	YDI
1C	YS	NULL	NULL
1D	YDD	YSI	NULL
1E	YD	YS	YD
1F	YDP1	YX	YDP1

*RGR07 (bus address '17') is designated null register for the S Bus by convention of the micro-assembler.

Register Mnemonics and Descriptions.

MNEMONIC	REGISTER	COMMENT
UGR	User general registers	16 registers manipulated by emulated language
RGR	Micro-level general registers	8 additional GP registers available to the micro-program
PSW	Program Status Word	16 bit register containing interrupt enables and flags
MDR	Memory Data Register	
MLC	Memory Location Counter	Location Counter of emulated program
MAR	Memory Address Register	
NULL	No register selected	Gates 0 to A and B Busses
YS	User source register	Register selected by Bits 12:15 of emulated instruction (contents of USR)
YSI	User source register immediate	Bits 12:15 of the emulated instruction (USR) gated onto B Bus
YX	User index register	Same as YS except NULL gated to A Bus if field is 0 (contents of USR=0)

MNEMONIC	REGISTER	COMMENT
YD	User destination register	Register selected by Bits 8:11 of emulated instruction (contents of UDR)
YDI	User destination register immediate	Bits 8:11 of the emulated instruction (UDR) gated onto the A Bus
YDP1	User destination register plus 1	Register selected by Bit 8:11 of emulated instruction +1 (must be odd)
YDD	User destination register direct	S Bus 12:15 replaces UDR contents

Register Peculiarities. The last four bits of the PSW contain the Condition Code of the emulated computer. In general, these bits can be manipulated by any addressed module unless the PSW is the S Bus destination or their change has been inhibited by the micro-instruction. The individual bits of the PSW which have hardware implications are:

PSW 01	ATN (0) and ATN (3) enable
PSW 02	Machine Malfunction enable
PSW 07	Privilege instruction/Memory Protect enable
PSW 09:10	ATN (1 and 2) interrupt enables
PSW 12	C flag of Condition Code
PSW 13	V flag of Condition Code
PSW 14	G flag of Condition Code
PSW 15	L flag of Condition Code

PSW Bits 3 through 6, and Bit 8, may have significance to the micro-program.

The following additional registers have the indicated capabilities and connotations.

1. The MDR receives data asynchronously from memory.
2. The MDR and MAR being addressed cause the Processor to interlock with memory when they are the source or destinations of the current instruction and the Processor is requesting memory service.
3. The MAR and MLC can be incremented by two or four from the ROM micro-control.
4. The contents of the MLC can be jammed into the MAR by ROM micro-control.

3.5.7 CPU Flags. The CPU contains a flag register which is independent of the PSW flags and is manipulated by any module which attempts to affect the PSW Condition Code by activating the SCC control line of the CPU Control Bus. When the SCC control line is active, the state of the VCC, CCC, GCC and LCC are unconditionally jammed into the CPU flag register and conditionally into the PSW Condition Code. The changing of the PSW is controlled by the microprogrammer by the E field of the micro-instruction. The state of the CPU flags can be individually tested by the Module 0 instructions.

3.5.8 Arithmetic Module (ALU) Programming. The Arithmetic Logic Unit (ALU) is a standard module in the Model 80 hardware. It is addressed as Module 1 in the module field of the instruction and is capable of 20 functions. Communications with the ALU is asynchronous. By design, the ALU is never busy and for the majority of ALU functions, response is within 100 nanoseconds. (This allows an ALU referenced instruction to be completed in 200 nanoseconds.)

For functions which require more than one ALU cycle (i.e., shifts, rotates, and multiply/divide), the ALU does not respond with a finish signal until the completed results are on the S Bus.

Multiply/divide and extended shift operations can be performed only on the 24 general registers and must address the same register pair on both the A and S Busses. The same restrictions that apply to these operations at the user level must be adhered to at the micro level.

A user emulated multiply/divide instruction is micro-coded by selecting the ALU (Module 1); addressing the UDR on the S Bus, the UDRP1 onto the A Bus, the USR onto the B Bus, and the required function code for the operation. When the ALU signals its completion, the results have already been deposited in the UDR.

To implement a shift or rotate instruction, the register to be manipulated is addressed onto the A Bus, the shift count is put onto the B Bus, and the S Bus is addressed to the destination register. For extended shifts, the same register pair must be addressed on both the A and S Busses, the even register being addressed to the S Bus, and the odd register to the A Bus.

The ALU generates valid CPU flags for all instructions. The C flag is gated as MSIG.

F FIELD	OPERATION
0000	Subtract
0001	Add
0010	*Subtract with carry (employs CPU flags)
0011	*Add with carry (employs CPU flags)
0100	Not used
0101	Logical AND
0110	Logical Exclusive OR
0111	Logical OR
1000	*Logical shift right
1001	*Logical shift left
1010	*Rotate right
1001	*Rotate left
1100	*Arithmetic shift right
1101	*Arithmetic shift left
1110	*Signed multiply
1111	Signed divide

*When used in conjunction with the K bit of the RRC instruction, shifts are double precision, multiply is unsigned, and the C, G and L of the PSW are used for add and subtract with carry.

3.5.9 I/O Module Programming. The I/O module performs a multiplicity of functions. In general, it is addressed to communicate with the multiplexor channel. It has the additional capability of performing byte manipulations for the CPU both in conjunction with an I/O exchange and without one. Furthermore, the I/O module contains the Machine Control Register (MCR) which stores machine trouble conditions and interrupts the CPU. The contents of the MCR can be sensed, tested and cleared. Module Number 2 has been assigned to the I/O module.

Multiplexor Channel. The Multiplexor Channel, generated on the I/O module, is operationally identical to the standard INTERDATA Multiplexor Bus in all respects. The Multiplexor Bus is a byte or halfword-oriented I/O system which communicates with up to 255 peripheral devices.

A single instruction from the CPU contains the device address, the encoded function, and up to 16 bits of output data when needed. The Multiplexor Bus generator provides single or multi-cycle operation to address the device, transmit the decoded function, send or receive over 16 bi-directional data lines, and synchronize the exchange.

The normal byte or halfword operation consists of an address cycle and a data cycle. However, during a Read/Write block sequence, the address cycle is not used. For halfword functions (RDH/WDH) with a byte oriented device controller, two data cycles are used to transfer the halfword.

Byte Manipulation. The I/O module has the capability of performing byte manipulation both in conjunction with an I/O operation and without one. The byte steering is under control of the least significant memory address bit in the MAR and also the KSIG line. For halfword operations, this manipulation is inoperative but the double data cycle with packing/unpacking results when the Halfword (HW) test line is inactive.

I/O Module Function Codes. The encoded I/O module functions and the byte manipulations are described in Section 3.7.3.

Machine Control Register (MCR). An interrupt on Machine Malfunction (MMF) is generated when Bit 12, 13, 14, or 15 in the Machine Control Register (MCR) is set. The sense MCR (SMCR) function gates MCR (04:05) to S(04:05), MCR(08:15) to S(08:15), and MCR(12:15) to CC(C, V, G, and L). The CMCR function clears MCR(11:15), where there are ONEs in B(11:15). The system initialize SCLR0 clears all the MCR except the strap bits.

The MCR bits are assigned as follows:

BIT	MNEMONIC	MEANING
MCR15 (L)	EPF	Early PPF
MCR14 (G)	IPF	Instruction parity fail (memory)
MCR13 (V)	DPF	Data parity fail (memory)
MCR12 (C)	IA/STF	Strap selection; either or both [IA=Illegal Address (memory)]
MCR11	STF	STRT time out fail
MCR10	CATN	Console attention (display controller)
MCR09	ARST	Auto restart (strap)
MCR08	Spare	(strap)
MCR05	BNKB	Bank B (testable strap for DCS)
MCR04	BNKA	Bank A (testable strap for DCS)

Start Timer (STRT). The STRT timer (35 microseconds) is activated whenever the CPU sends out the STRT signal to the various system modules (ALU, IOU, etc.) and is cleared by the MFIN signal from the module. Should the time out occur before MFIN arrives, on non D Bus operations, Bit 11 of the MCR is set and a pseudo MFIN signal restarts the CPU clock. If STF is strapped into MCR12, the MMF interrupt is also generated.

In the case of a STRT time out during a D Bus operation, the MCR is not changed. However, the False Sync code (0100/CVGL) is placed on the Condition Code Bus and a pseudo MFIN restarts the CPU clock.

3.6 Processor Block Diagram Analysis

3.6.1 CPU (Figure 3). The architecture of the Processor is structured about four busses which provide intercommunication between the CPU and the remaining modules.

The CPU selects the module via the Control Bus (C Bus), specifies the function, and signals that data is available on the A and B Busses. The addressed module signals when it has completed its function and transmits flag type data back over this bus.

The A Bus and B Bus contain the two operands offered simultaneously to the addressed module to be manipulated. These busses reflect the data captured by the A latch and B latch registers. Most of the CPU registers can be gated onto the A and B Busses.

Data from an addressed module (exclusive of the ALU) is returned to the Processor via the S Bus. This bus is piped onto the ST Bus along with the ALU results to form the true result bus of the CPU. The ST Bus is gated to most of the CPU registers as a source input.

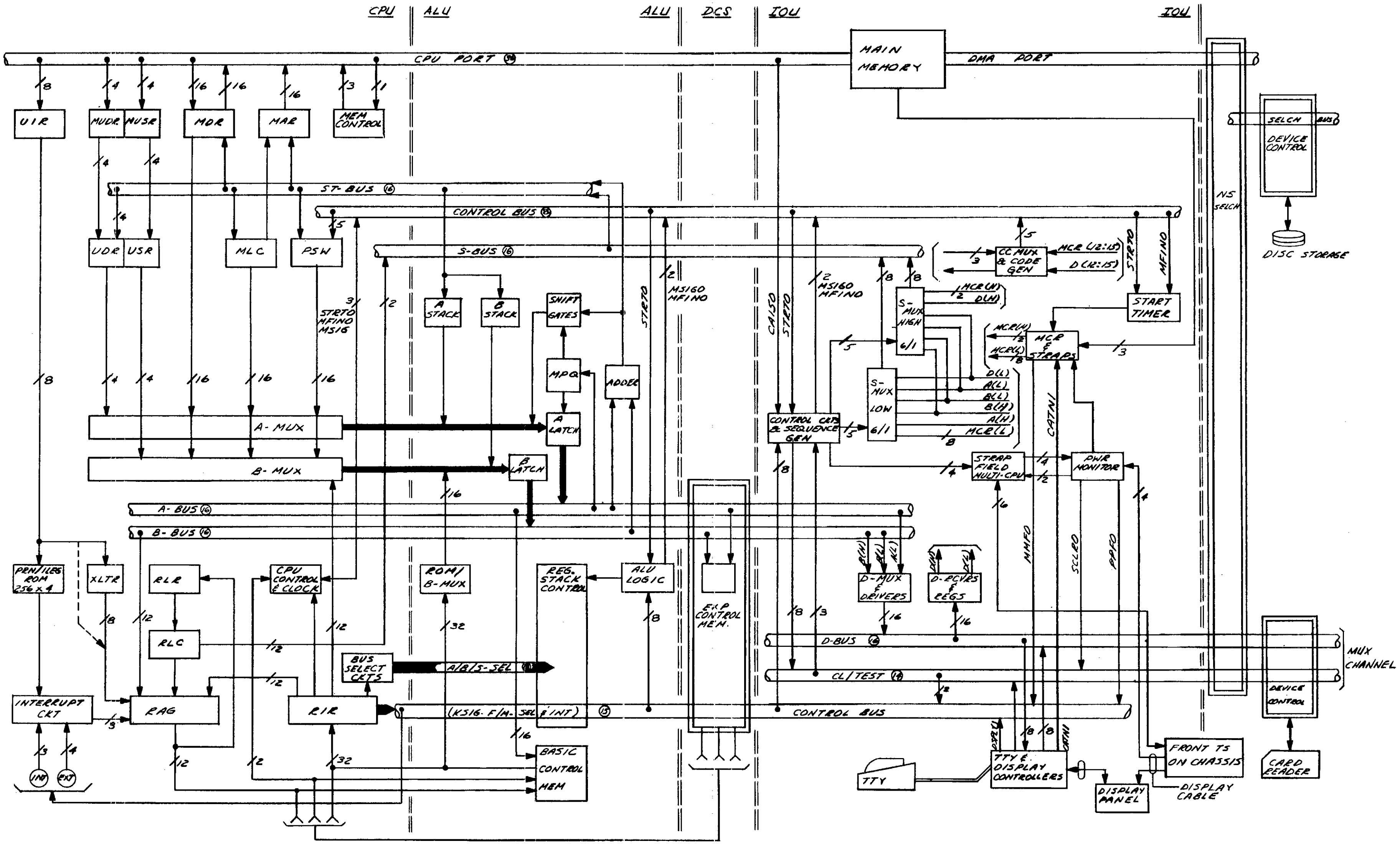
CPU
ALU
ALU
DCS
IOU
IOU
CPU PORT
MAIN MEMORY
DMA PORT
UIR
MUDR
MUSR
MDR
MAR
MEM CONTROL
ST-BUS
CONTROL BUS
S-BUS
UDR
USR
MLC
PSW
A STACK
B STACK
SHIFT GATES
MPG
A LATCH
ADDEC
B LATCH
A-MUX
B-MUX
A-BUS
B-BUS
STRTO MFINO MS16
MS160 MFINO
STRTO
CAISO
STRTO
MS160 MFINO
PRN/ILES ROM 256 x 4
XLTR
RLR
RLC
CPU CONTROL & CLOCK
ROM/ B-MUX
REG. STACK CONTROL
ALU LOGIC
EXP CONTROL MEM.
BUS SELECT CKTS
A/B/S-SEL
INTERRUPT CKT
RAG
RIR
(KS16. F/M. SEL & INT)
CONTROL BUS
BASIC CONTROL MEM
INT
EXT
CONTROL CKTS & SEQUENCE GEN
S-MUX HIGH 6/1
S-MUX LOW 6/1
CC MUX & CODE GEN
MCR (12:15)
D (12:15)
START TIMER
MCR & STRAPS
MCR(H)
MCR(L)
D(H)
D(L)
A(L)
B(L)
B(H)
A(H)
MCR(L)
STRAP FIELD MULTI-CPU
PWR MONITOR
CATNI
MMPO
SCLRO
PPFO
D-MUX & DRIVERS
D-RCVRS & REGS
D-BUS
CL/TEST
TTY
TTY & DISPLAY CONTROLLERS
DISPLAY PANEL
FRONT TS ON CHASSIS
DISPLAY CABLE
NS SELCH
SELCH BUS
DEVICE CONTROL
DISC STORAGE
MUX CHANNEL
DEVICE CONTROL
CARD READER

Figure 3. Model 80 Block Diagram

The ROM Instruction Register (RIR) is a 32-bit register that latches the current instruction read from the control store memory to provide the control gating for each instruction. Data can also be gated from the control memory onto the B Bus for indirect data fetches. One of the many functions performed by the encoded instruction is register gating. This is performed by the select logic to encode the A, B, and S SEL lines, these lines determine which registers are gated onto the A and B Busses, and which register is the S Bus destination.

The ROM Address Gates (RAG) select the address of the control store to be interrogated next. Inputs to the RAG may be the ROM Location Counter (RLC) to select the next instruction, certain bits of the RIR for branching, the B Bus for indirect addressing or branches, the translated vector for the next user instruction to be emulated (XLTR), or interrupt trap address from the interrupt logic.

The ROM Location Register (RLR) preserves the address of the current instruction. It is loaded with the address of the current instruction every time the RIR is loaded, except when the instruction is an interrupt or execute type which do not alter the ROM Location Register. The RLR is gated to the RLC to perform RLR+1 for the next sequential instruction.

The 16 general user registers and the 8 general micro-registers are contained in the A stack and B stack. This is a redundant pair of registers, implemented as such to allow gating of any two registers of the machine simultaneously onto both the A Bus and B Bus. Gating of these stacks is controlled by the A, B, and S SEL lines, just as the other A, B, and S source and destination registers.

The Program Status Word register (PSW) is an architectural feature of the user level machine. Certain bits of the PSW are used to mask interrupts, control the privileged mode of the Processor, and to contain the Condition Code of the user level program. This register can be gated to/from the A, B, and S Busses. The Condition Code portion can also be loaded independently of the register addressing.

The Memory Location Counter (MLC) aids the emulation capability of the Processor. It is used to contain the memory location of the current user level instruction. In addition to being capable of being gated to/from the A, B, and S Busses, this register may be incremented by two, incremented by four, or jammed into the Memory Address Register (MAR) under micro-control of the programmer.

The Memory Address Register (MAR) must contain the address to be used by the main memory for a read/write operation. This register can be loaded from the S Bus or the MLC, and may also be incremented by micro-control of the programmer. The manipulation of this register is interlocked with the memory operation by hardware to remove timing restraints from the micro-programmer.

The Memory Data Register (MDR) is loaded from the S Bus with data to be written into the main memory, or it is loaded from the Memory Data Bus with the contents of the addressed memory on a memory read operation. This register may be gated onto the A or B Bus of the Processor, and, like the MAR, hardware interlocks remove the timing considerations of the memory system from the micro-programmer when this register is referenced.

The User Instruction Register (UIR) stores the eight bit op-code of the next user instruction to be emulated. It is loaded from memory when a read operation is designated as an instruction fetch by the micro-code. The eight bit op-code is translated by the XLTR hardware to a 1/128 vector which designates the beginning address of the emulation sequence for a particular instruction. The eight bit op-code is also gated to a Privileged/Illegal ROM which is coded to detect these types of instructions and cause an interrupt to the Processor.

The Memory User Destination Register (MUDR) and Memory User Source Register (MUSR) store the destination and source fields of the next instruction to be emulated when it is read from memory. This data is transferred to the User Destination Register (UDR) and User Source Register (USR) at the beginning of a new emulation sequence to provide residual control for the instruction.

Memory Control is effected by the micro-control field of the micro-instruction. The ability is provided to cause data read, data write, and instruction read. When an instruction read is designated, the main memory passes to the Processor the data specified by the MAR plus the data at MAR+2. The Processor stores the first 16-bits in UIR, MUDR, and MUSR and the second 16-bits in the MDR in anticipation of a 32-bit instruction. If the instruction is found to be a 16-bit instruction, the contents of the MDR is ignored.

3.6.2 ALU (Figure 3). The ALU is a standard module of the Model 80 and provides the basic arithmetic/logic capability. It communicates with the CPU over the A, B, S, and C Busses in a manner identical to other modules. In reality, the A, B, and ST Busses and the A and B stacks are generated on the ALU board, although conceptually, they belong to the CPU architecture. The ALU takes advantage of its proximity to these resources by manipulating them when implementing shift and multiply/divide type instructions.

The ALU becomes active when it recognizes its address on the Control Bus (Module Number 1), and the CPU signals start (STRT). The function to be implemented is determined from the Control Bus.

ALU functions may be of two types. The simple functions (add/subtract and logical) cause the ALU to immediately return a module finished signal (MFIN). For these type of instructions, the A and B Busses are gated through the ALU, and the required function is performed by sequential gating onto the ST Bus.

For the complex type functions (multiply/divide and shift) the ALU clock is enabled and a hardware sequence is entered to perform the required operation. For these operations, the Multiplier/Quotient Shift Register (MQ) and the A latch registers are used as a 32-bit shift register. The shift gates are used to shift the A Bus or the Sum Bus right or left back into the A latch and onto the A Bus again as determined by the ALU algorithms. In the case of multiply/divide and extended shift type instructions, the ALU stores the most significant half of the completed results before signaling the CPU withMFIN. The least significant half is dumped onto the A Bus from the MQ register and gated through the ALU onto the ST Bus when MFIN is activated.

3.6.3 IOU Board (Figure 3). The IOU board contains the I/O Control, the Display controller, the TTY controller, the Machine Control Register (MCR), the Power Monitor and the Start Timer.

The Display and TTY controllers have access to the CPU via the Multiplexor Channel D Bus and the I/O Control in the same manner as other peripheral device controllers. The Display controller provides a visual display of the contents of all system registers and any main memory location, together with the capability of manually entering data and programs. It shares D Bus drivers/receivers with the TTY controller and signals the CPU directly with the Display (DSPLY) interrupt. The Console Attention (CATN) signal appears as Bit 10 of the MCR.

The TTY controller, which supports the Model 33/35 Teletype, provides serial/parallel conversion and all standard TTY control features. It contains a full character buffer in the receive mode to permit a program service interval of one character time (100 milliseconds). The detailed descriptions of the Display and TTY controllers are covered in Sections 4 and 5.

I/O Control. The I/O Control performs a multiplicity of functions. The main function is to generate Multiplexor Channel D Bus from the CPU busses whenever it is addressed by Module Number 2 and the proper function selections are made. The control also performs byte manipulation for the CPU both in conjunction with an I/O operation and without. Common function decoders also generate signals to sense/clear the MCR (which stores machine malfunction conditions), to set the system Stop flip-flop with a Power Down/Initialize function (FPOW), and to gate four bits of the B Bus (12:15) to the front terminal strip of the chassis for external signaling purposes; e.g., multi-CPU operations.

Four function select lines together with the KSIG line pick 1 of 32 possible functions as shown on Table 3.

TABLE 3. I/O CONTROL FUNCTIONS

FSEL0X		FUNCTION	
	0 1 2 3	KSIG=0	KSIG=1
0	0 0 0 0	RD	RDR
1	0 0 0 1	WD	WDR
2	0 0 1 0	SS	SSR
3	0 0 1 1	OC	OCR
4	0 1 0 0	RDH	*STBR
5	0 1 0 1	WDH	*LBR
6	0 1 1 0	ACK	*LDWAIT
7	0 1 1 1	*SMCR	*CMCR
8	1 0 0 0	RDA	RDRA
9	1 0 0 1	WDA	WDRA
A	1 0 1 0	SSA	SSRA
B	1 0 1 1	OCA	OCRA
C	1 1 0 0	RDHA	*STB
D	1 1 0 1	WDHA	*LB
E	1 1 1 0	DACK	*EXB
F	1 1 1 1	*POW	*POUT

*Functions that do not require operation of the Multiplexor Channel D Bus.

The D Bus functions may be performed with or without an address cycle depending upon the state of FSEL00. KSIG is used to specify register type operations or to distinguish between the halfword functions (RDH/WDH) and some non-D Bus operations (STB/LB).

The function mnemonics are listed below.

MNEMONIC	FUNCTION	COMMENT
RD/RDA	Read Data	byte/indexed
WD/WDA	Write Data	byte/indexed
OC/OCA	Output Command	byte/indexed
SS/SSA	Sense Status	byte/indexed
RDR/RDRA	Read Data	byte/register
WDR/WDRA	Write Data	byte/register
OCR/OCRA	Output Command	byte/register
SSR/SSRA	Sense Status	byte/register
ACK	Acknowledge Interrupt	byte/register
RDH	Read Data Halfword	two data cycles for byte controllers
WDH	Write Data Halfword	two data cycles for byte controllers
DACK	Data Channel Acknowledge	includes an automatic RDH
STB	Store Byte	halfword/indexed
LB	Load Byte	byte/indexed
STBR	Store Byte	halfword/register
LBR	Load Byte	byte/register
SMCR	Sense Machine Control Register	
CMCR	Clear Machine Control Register	
EXB	Exchange B-Bytes	
LDWAIT	Load Wait Flip-Flop	B (00) to FWAIT
POW	Release Initialize Relay	
POUT	Gate Output Pulses	

I/O Control/Operation. When the I/O Control is addressed and given a D Bus function code, it creates a one, two or three cycle Multiplexor Channel operation. The device address on A Bus (08:15) is gated to D Bus (08:15) together with the ADRS control line whenever address type functions are specified. The returned SYN signal terminates the address cycle and initiates the next control function (DA, DR, CMD or SR). Delay timing within each cycle insures that the relationship of the control line and D Bus signals meet the Multiplexor Channel Timing requirements.

The halfword functions (RDH/WDH) have a single data cycle when the Halfword (HW) test line is active and two data cycles when a byte oriented controller is addressed.

Output data is gated from the B Bus to the D Bus. The input data is gated from the D Bus to the input Data Register and then through the S Multiplexor (MUX) to the S Bus. In the case of a sense status operation, Data Register Bits 12:15 are also gated to the Condition Code (CC) Bus via the CC MUX. On all other D Bus operations, four zeros are placed on the CC Bus together with the CC strobe (SCC0). These zeros clear the CPU flag register but do not enter the PSW unless the CPU Enable bit is set.

At the end of the operation, the I/O Control returns a MFIN signal to restart the CPU clock.

The ACK function generates a single cycle on the D Bus while the Data Channel Acknowledge (DACK) function results in simultaneous ADRS and DACK signals followed by an automatic RDH cycle. The active state on the DCR line from the Data Channel selected indicates a request for a memory read, at the address specified by the RDH. The memory read-out data is sent to the Data Channel on a subsequent WDH operation. Should DCR not be active, the CPU sends an RDH function after the termination of the DACK operation. The DCR signal, when present, is gated to the CPU on the MSIG line.

The non-D Bus byte-manipulation functions set up combinational logic in the S MUX. When the decoded STRT signal is received, selected bytes from the A and/or B Bus are gated to the S Bus and the MFIN signal is returned to the CPU. This operation normally removes the CPU clock inhibit before the next clock pulse occurs so no clocks are skipped. Should a malfunction result in a delayed or missing MFIN signal, the clock inhibit is already in effect and the next clock pulse does not occur until MFIN is received at the CPU. The case of the missing MFIN is covered in the section of the Start Timer.

Start Timer. A 35 microsecond timer is started by the STRT signal and cleared by the MFIN signal from any selected module. Should the timer run out before the MFIN signal arrives, a malfunction exits; i.e., non-existant module, circuit trouble, or no SYN return from the Multiplexor Channel. If a D Bus function was called for, the False Sync code (0100/CVGL) is placed on the CC Bus and a pseudo MFIN signal is sent to restart the CPU clock. For a non-D Bus operation, the Start Time Fail (STF) bit is set in the Machine Control Register (MCR 11), and a pseudo MFIN signal is sent to restart the CPU clock. If STF is strapped into MCR 12, the MMF interrupt is also generated.

The timer is inhibited during the Early Primary Power Fail (EPF)/Primary Power Fail (PPF) operation since the initialize relay operate/release times are longer than the timer period. A manual inhibit may also be used when the Model 80 Test Set is in use.

Machine Control Register. The Machine Control Register (MCR) consists of five flip-flops, four straps, and the Console Attention (CATN) lead from the Display controller. MCR bit assignments are:

BIT	MNEMONIC	MEANING	
15	EPF	Early Primary Power Fail	
14	IPF	Instruction Parity Fail	
13	DPF	Data Parity Fail	
12	IA/STF	Illegal Address and/or Start Timer Fail	
11	STF	Start Timer Fail	
10	CATN	Console Attention	
09	ARST	Auto Restart	(strap)
08	spare	spare	(strap)
05	BNKB	Bank B	(strap)
04	BNKA	Bank A	(strap)

The IPF, DPF and IA flip-flops store signals received from the Memory Bank Controller (MBC). Signals to set the EPF and STF bits are generated on the IOU board by the Power Monitor and Start Timer circuits. The composite bit, MCR12, can be strapped to represent IA, STF, or both. MCR11 is always set by STF. The testable straps are wired for logical 1 or 0 as required. A Machine Malfunction (MMF) interrupt is generated when any of the Bits 12, 13, 14 or 15 are true. The SMCR function gates MCR(12:15) to the CC Bus, MCR (08:15) to S(08:15), and MCR(04:05) to S(04:05). The CMCR operation clears MCR(11:15) where there are ONES in B(11:15). This permits selective clearing of some bits while the rest of the MCR continues to monitor other machine functions without loss of data.

Power Monitor. The Power Monitor contains the primary power fail detect circuits, the system initialize relay and the associated delay circuits used to control the relay amplifier. This logic provides an orderly system shutdown whenever the system is initialized or when power is turned off or lost.

The 12VAC input from the CPU logic supply, through an interlock on the memory supply, is monitored for low line voltage. When trouble is detected, the EPF bit is set in the MCR to create an MMF interrupt. After approximately 1 millisecond, the PPF interrupt is generated and the relay release operation is begun. The POW function also initiates the release operation.

For multi-CPU systems, the various Power Monitors may be interconnected for proper sequencing of the subsystems.

3.7 Functional Diagram Analysis

This section describes the major functional areas of the Processor. The descriptions refer to Functional Schematics 35-403D08 (CPU), 35-404D08 (ALU), and 35-405D08 (IOU); and to the charts and figures provided in this section. Unless otherwise specified, references are to the schematic for the module under discussion. Reference is by schematic sheet number and coordinate in parenthesis. For example; STRB0 (1K2), in Section 3.7.1, refers to the CPU clock signal found on Sheet 1 at coordinate K2 of CPU Functional Schematic 35-403D08. A list of mnemonic description is tabulated for each set of schematics. These descriptions do not attempt to define each mnemonic explicitly.

Note that in INTERDATA functional schematics, the last character in the mnemonic symbol designates the logic level when the signal is active. For example; TACK0 is Transmit Acknowledge and the last character (0) indicates that when TACK0 is active the line is at a logical ZERO level.

3.7.1 CPU (refer to Functional Schematic 35-403D08).

ROM State Control. The CPU control logic is governed basically by pairs of flip-flops which determine the current state of the Processor. The CPU can be in one of four states determined by the configuration of two elements RSA (1H5) and RSB (1H8).* These two elements are encoded to form ROM States RS00 thru RS03.

The four states of the Processor are represented in Figure 4.

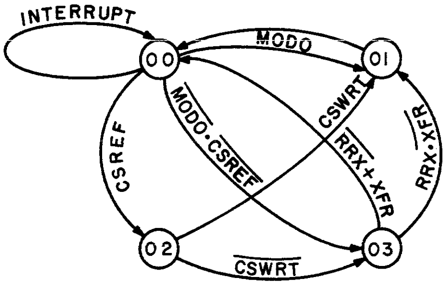
INTERRUPT
$\overline{\text{MODO}}$
00
01
02
03
CSREF
MODO.CSREF
CSWRT
$\overline{\text{RRX}}$+XFR
RRX.$\overline{\text{XFR}}$
$\overline{\text{CSWRT}}$

Figure 4. CPU State Diagram

The basic functions of the CPU can best be described by correlating the significant logical events of the Processor to this diagram.

RS00 — An instruction sequence begins in RS00. The ROM Instruction Register (RIR) is always loaded with a new instruction from the control store on the transition to RS00. This state constitutes instruction decoding time. Module number and function selects are gated to the Control Bus, the registers to be gated onto the A and B Busses are decoded and gated onto the A latch and B latch Busses. Logical decisions are made as to the next state transition, micro-control of memory and interrupt recognition. All micro-control of main memory with the exception of data read and data write is accomplished on the transition from RS00. It is also at this time that data is transferred to the A and B Busses. The CPU may enter any state when exiting RS00.

1. RS00 to RS00. When an interrupt is recognized, the current instruction is abandoned and the instruction at the interrupt vector is gated to the RIR. It is important to note that the contents of the RLR is preserved on an interrupt, and the effect is an execute of the interrupt vector instruction.
2. RS00 to RS02. The CPU always makes this transition when the current instruction calls for a read or write to control store memory (see Sections 3.5.2 and 3.5.4).
3. RS00 to RS03. This transition is made when the module to be referenced is not the CPU itself and one of the operands does not have to be retrieved from control store.
4. RS00 to RS01. When the CPU itself is referenced (branch instructions), the transition is always from RS00 to RS01.

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*To provide fan out for these signals, several versions such as RSAW, RSAX, RSAY, RSBX, and RSBY are found in the logic. Reference is only made to RSA and RSB.

RS03 — ROM State 03 is in effect Start (STRT) to the Control Bus. This state is only entered to communicate with another module. During this state, the CPU is inactive and waits for the addressed module to signal completion of its function (MFIN) (1D2). It is also during this time that the next instruction is read from the control store in anticipation of the transition to RS00. When the addressed module returns MFIN, and all events indicate that the next instruction is available to the RIR (see Clock Timing), the transition from RS03 occurs.

1. RS03 to RS01. This transition only occurs when the instruction type is a conditional transfer (RRX) and prevailing conditions indicate that the transfer will not occur (see Section 3.5.2). In this event, the transition is to RS01 to allow decoding of the next sequential instruction.

2. RS03 to RS00. This is the normal transition from RS03, it is the only possibility other than RS03 to RS01.

RS02 — ROM State 02 is only entered for the purpose of reading from or writing into control store memory. When it is entered for reading, the intent is to replace the data on the B Bus with the data stored at that address before signaling a module to Start (STRT). This is accomplished on the transition from RS02 to RS03. When this state is entered for writing, there is to be no further module communications, and the transition is to RS01 to gate the next sequential instruction from control store.

RS01 — This state may be entered from any state other than RS01. It is entered from RS00 for Module 0 (MOD0) instructions. It is entered from RS02 for Control Store Write instructions (CS WRT). It is entered from RS03 when the instruction decoded during that state is to be ignored (RRX•XFR). This state is entered solely for gating the next instruction to the RIR. The only transition from RS01 is to RS00.

ROM State Logic. The ROM State Register is initialized to RS01 by SRSC0 (1G8) on System Clear or whenever a starting address is jammed into the RLR by the test set. This register uses D type logic optimized to implement the state diagram of Figure 4. This logic implementation (Sheet 1 of 35-403D08) is tabulated in Figure 5.

TRANSITION	RSA ACTIVE D LOGIC	RSB ACTIVE D LOGIC	NOTE
RS00 to RS00	NONE	NONE	Interrupt (INT0) keeps potential logic inactive.
RS00 to RS02	NONE	INT0•RSBX0•RSAW0•MOD000	
RS00 to RS01	INT0•MOD001•RSBX0•RSAW0	NONE	Transition can only be to RS01 on MOD00 instructions.
RS00 to RS03	MOD000•RIR030•INT0•RSBX0•RSAW0	INT0•RSBX0•RSAW0•MD000	Transition can be from RS000 to RS02 or RS00 to RS03 dependent upon RIR030 (control store reference).
RS02 to RS03	RSAW0•RSBX1	RSAW0•RSBX1•RMWRT0	Any transition from RS02 sets RSA.
RS02 to RS01	RSAW0•RSBX1	NONE	
RS03 to RS01	RSAW1•RSBX1•MDSIG1•RRX1•RIR311	NONE	Conditional RRX instruction (see Section 3.5.2).
RS03 to RS00	NONE	NONE	
RS01 to RS00	NONE	NONE	

Figure 5. ROM State Control Logic

CPU Clock. The clock control for the CPU is a gated oscillator (1J2) which uses a delay line to establish the basic frequency. The basic CPU Clock (STRBO) (1K2) is adjusted for frequency and duty cycle by selectively wiring TREP0 and TWDTH0 (1F1) respectively to the delay line taps. The factory adjustment selects a 10MHz frequency with a 40% duty cycle. TWDTHA0 controls the width of the RIR strobe and is adjusted for 20 nanoseconds. This allows maximum time for the return of MSIG to the CPU on RRX type instructions (2C6). The CPU employs asynchronous communications external to itself, and as such, certain conditions inhibit the clock from free running. To inhibit the clock, KL1 (1H3) must appear active before the generation of the next active STRB0. In addition to providing for an inhibit input from the test set (INHCLB0) (1G3) and the expansion control store (INHCLA0) (1G3), KL1 may be activated by SRSC0 (1G8) on System Clear or a composite signal KLCLK0 (1F3), the memory timing and addressed module interlock. The KLCKL0 signal provides the asynchronous capability to the CPU and in effect inhibits the clock under the following conditions.

1. STRT active and the addressed module has not responded with finish (RS031· MDFIND0).
2. The Processor is waiting to begin another emulation but the control store vector is not yet available from main memory (RSAW1· D1· IWAIT1).
3. The MAR or MDR is a source or destination register and the memory is still busy (CREQ1· PK1· RS001).
4. The micro-control is attempting to manipulate memory or its registers and the memory is still busy [CREQ1· RS001 (MC001+MC011+MC021+MC031)].

Main Memory Control. Main memory, in keeping with the philosophy of asynchronous external communications, is designed to be request/response. Memory control is not implicit but rather must be explicitly designated by the micro-programmer via the MC field of the micro-instruction (see Section 3.5.3). The following constitute the memory interface.

1. CREQ0 (1R6) Control Request to Memory. Main memory recognizes a request from the CPU when CREQ0 is active. CREQ0 is made active at the transition from RS00 when the request is for a new instruction to emulate (CFTCH) or at the transition from RS01 or RS03 when the request is for data read/write. When the request is for an instruction, the memory transmits two successive words of data back to the Processor: the contents of the address specified by the MAR, plus the contents of the next sequential location. CREQ0 is held active until all the data requested is returned from memory. CREQ0 is made conditional to aid the emulation task by inhibiting the request for an instruction fetch when the request is issued by a branch micro-instruction unless the branch fails to pass (PASS0).
2. CFTCH0 (1R4) Control Fetch to Memory. CFTCH active in conjunction with CREQ informs the memory that this request is for a 32-bit instruction rather than 16-bits of data.
3. CWRT0 (1R8) Control Write to Memory. This line is active on a 16-bit data write to memory to distinguish from a read request.
4. CRDY (1K3) Control Ready from Memory. CRDY informs the Processor that data is valid on the Memory Bus during a read cycle or that the memory has completed the cycle during a write.
5. MCLR1. An internal control flip-flop used to achieve asynchronous timing.

The Memory Address Register (MAR00:15) (Sheet 9) can be loaded from the S Bus when it is designated as the destination register by an instruction or it can be jammed from the MLC by micro-control. This is achieved by multiplexing this data to the set inputs (Sheet 9) and encoding the desired clocking signals; MARCKA (9E6), MARCKB (9D7), and MARCKC (9D7). The MLC is jammed to the MAR at the transition from RS00. The S Bus is loaded at the transition from RSA. This counter is implemented in MSI logic with the exception of the least significant two digits. This configuration allows the capability of incrementing the register by either two or four by the micro-control. Incrementing the MAR is always effected when exiting RS00.

The Memory Data Register (MDR00:15) (Sheet 8) can be loaded from the S Bus at RSA when it is addressed as the destination register or it can be loaded from the Memory Bus by the logic CRDY1· MWRT0. It is bi-directionally gated onto the Memory Bus by the logic CREQ1· MWRT1.

Control Store Addressing and Latching. The control store is addressed from the ROM Address Gates (RAG04:15) (Sheet 4) which gate the proper addressing field for the data to be read. Table 4 lists the various address fields and the conditions which cause them to be gated. Note that the logic tabulated is the effective logic and may have been derived from higher encoded gating.

TABLE 4. ROM ADDRESS GATE CONDITIONING

CONDITION	RAG04•09 LOGIC	RAG10•15 LOGIC
ADDRESS LINK	RSA1•PASS1•RGLNK0 (RIR31, 20:24)	RSA1•PASS1 (RIR25:30)
REGISTER LINK	RSA1•PASS1•RIR030 (B03:08)	RSA1•PASS1•RIR030 (B09:14) RSA1•PASS1 (RIR 25:30)
READ/WRITE	RSA0•RSB1 (B03:08)	RSA•RSB1 (B09:14)
NEXT SEQUENTIAL INSTRUCTION	RSA1•PASS0•D0 (RLC04:09)	D0•PASS0•RSA1 (RSB1+RRX0) (RLC10:15)
RRX TRANSFER	RSA1•PASS•D0 (RLC04:09)	RSA1•RSB1•RRX1 (RIR25:30)
INTERRUPT VECTOR	RSA0•RSB0•INTR1	RSA0•RSB0•INTR1 (TRAP13:15)
EUMULATION VECTOR	RSA1•D1•PASS0 (UIR00:07)	RSA1•D1•PASS0 (UIR00:07)

The following peculiarities should be noted in reference to Table 4.

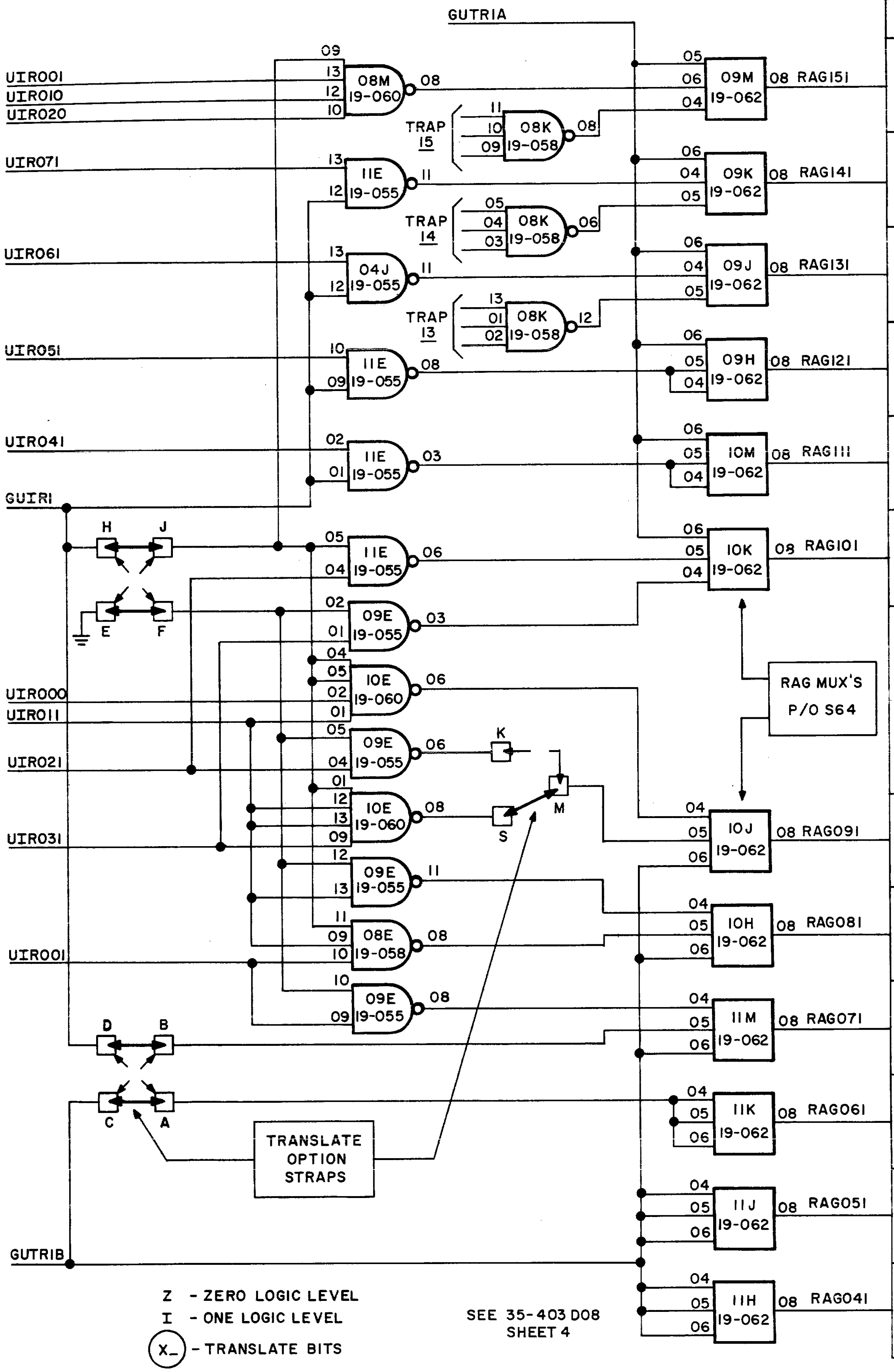
1. When gating the RIR (20:31) for Address Link, RIR31 is the MSB of the address, while the LSB to the second MSB are derived from RIR20:30 respectively.

2. When gating B03:14 for a Register Link, Bits 25:30 of the RIR are NORed into the least significant address portion to provide logical arithmetic possibilities.

3. When the emulation vector is gated to the RAG, a logical translation is performed upon the UIR in the standard option to compress the number of potential vectors from 256 to 128, while the non-standard (see simplified logic, Figure 6) provides 256 vectors (even address from '000' to '1FE' non-translated). The translated vectors can be derived from Table 5.

TABLE 5. OP-CODE TRANSLATION VECTORS

OPCODE (HEX)	CONTROL STORE VECTOR (HEX)
0n	00+2n
2n	20+2n
4n	40+2n
6n	60+2n
9n	00+2n+1
Cn	80+2n
Dn	C0+2n
En	A0+2n


GUTRIA
UIR001
UIR010
UIR020
UIR071
UIR061
UIR051
UIR041
GUIRI
UIR000
UIR011
UIR021
UIR031
UIR001
GUTRIB
08M 19-060
11E 19-055
04J 19-055
11E 19-055
11E 19-055
11E 19-055
09E 19-055
10E 19-060
09E 19-055
10E 19-060
09E 19-055
08E 19-058
09E 19-055
TRAP 15
TRAP 14
TRAP 13
08K 19-058
08K 19-058
08K 19-058
09M 19-062
09K 19-062
09J 19-062
09H 19-062
10M 19-062
10K 19-062
10J 19-062
10H 19-062
11M 19-062
11K 19-062
11J 19-062
11H 19-062
RAG151
RAG141
RAG131
RAG121
RAG111
RAG101
RAG091
RAG081
RAG071
RAG061
RAG051
RAG041
RAG MUX'S P/O S64
H
J
E
F
K
M
S
D
B
C
A
TRANSLATE OPTION STRAPS

NON TRANSLATE		TRANSLATE	
UIR	TRAP	UIR	TRAP
Z	15	(X15)	15
7	14	7	14
6	13	6	13
5	Z	5	Z
4	Z	4	Z
3	Z	2	Z
2	Z	(X9)	Z
1	Z	(X8)	Z
0	Z	Z	I
Z	I	Z	Z
Z	Z	Z	Z
Z	Z	Z	Z

Z - ZERO LOGIC LEVEL
I - ONE LOGIC LEVEL
(X_) - TRANSLATE BITS

SEE 35-403 D08 SHEET 4

Figure 6. Model 80 CPU RAG Options

The ROM Location Register (RLR) (Sheet 4) preserves the continuity of the control store program by storing the address of every instruction gated onto the RD Bus when the RIR is loaded. There are two notable exceptions to this:

1. Execute. When the instruction being performed is an execute link type instruction, the address of the instruction to be executed is inhibited from loading into the RLR. This causes the instruction following the execute link to be performed sequentially after the executed instruction (if the executed instruction is not another execute or branch type instruction).

2. Interrupts. When an interrupt is recognized, the instruction at the trap address is loaded into the RIR, but the address is not loaded into the RLR. This effectively causes the instruction at the trap address to be executed while preserving the address of the interrupted sequence if desired.

   The RLR may also be jammed through the Set/Reset inputs from the test set. The ROM Location Counter (RLC04:15) (Sheet 4) is an MSI counter gated to add one to the RLR to provide an increment to the next sequential instruction. Note that the carry into the counter (08F-07) (4B7) provides a test point which may be temporarily grounded to inhibit the counter from counting. This is provided to allow the CPU to be cycled under test on a single instruction. Note also that the RLC is gated onto the S Bus (Sheet 4) when the CPU is addressed during RSA to provide the Link address to be saved in a register. The register write gating function (REGWT1) (1F5) is active at this time to enable the writing of the selected register.

   The ROM Instruction Register (RIR) is a 32-bit register which latches the current instruction to be executed. It is loaded on every transition into RS00 with the data presented on the RD Bus by the control store.

Interrupts. The Model 80 employes a priority interrupt scheme which can acknowledge eight interrupts.

The externally generated interrupts (all except PRIV/ILEG) are latched in two registers (15T and 16T) (3G3) for the period of time they are interrogated and are input to a priority encoder (3K4), after masking with the appropriate PSW bits, to generate an address for the highest priority interrupt pending. These interrupts are enabled as a group by ENBINT0 (3N2) whenever a new instruction is to be decoded (D1·PASS0·RSA0) so that any interrupts pending are fielded before the next instruction is recognized. They are disabled when any interrupt is recognized (INTA1+INTB1) or at the beginning of a new emulation sequence (D1·RSA1). These interrupts may also be enabled/disabled by Module 0 instructions (KEB1·RIR170·RIR191, or KEB1·RIR170·RIR191) (3H1) under control of the micro-program.

The group interrupt enable (INTEBL0) (3R3) allows the Processor to recognize one of these interrupts by enabling the priority encoder (19-074) (3K3) to gate GINT1. INTEBL0 must be held active after the interrupt is recognized and ENBINT0 is removed so that the interrupt vector trap (13:15) remains present until the interrupt instruction is loaded in the RIR. This is accomplished by the logic INTEBL0=ENBINT0+INTA0.

The PRIV/ILEG interrupt is the lowest priority interrupt and can be recognized only when an instruction is decoded. A PRIV/ILEG instruction is recognized when the op-code of the instruction (UIR00:07) is applied to the PRIV/ILEG ROM (3J1) and reads out a word coded as either Privileged or Illegal. A Privileged instruction can only be detected when PSW 071 is active. When either of the two conditions is detected, INTB0 is set to activate the interrupt mechanism.

The presence of an interrupt pending is detected by INTR1=INTA1+INTB1 which causes the ROM state to remain in RS001 for an additional cycle and the trap (13:15) to be gated to the control store to fetch the interrupt instruction.

ASEL and BSEL (Sheet 5), and SSEL (Sheet 10). These control lines provide the steering for all the registers of the CPU. They control which registers are gated onto the A Bus (ASEL00:04) and B Bus (BSEL00:04) and which register receives the results from the ST Bus (SSEL00:04). It should be noted that ASEL and BSEL are only active during RSA0, and SSEL is only active during RSA1.

The conditions necessary to cause the various selections on each of these busses are tabulated in Table 6.

TABLE 6. REGISTER SELECTION

BSEL GATING	
BSEL EQUIVALENT	CONDITIONS NECESSARY
RIR(20:24)	Not immediate instruction and B field of instruction does not specify YX, YX, or YDP1.
USR(12:15)	Not immediate instruction and B field specifies YS or B field specifies YX and USR (12:15) does not contain all zeros.
UDR(08:10), 1	Not immediate instruction and B field specifies YDP1.
$K=1B_{16}$	Immediate type instruction.
$K=1F_{16}$	Not immediate instruction and B field specifies YX and USR(12:15) contains all zeros.
K=0	RSA1

ASEL GATING	
ASEL EQUIVALENT	CONDITIONS NECESSARY
RIR(11:15)	A field of instruction does not specify YD or YDP1.
UDR(08:11)	A field of instruction specifies YD.
UDR(08:10), 1	A field of instruction specifies YDP1.
K=0	RSA1

SSEL GATING	
SSEL EQUIVALENT	CONDITIONS NECESSARY
RIR(06:10)	Not module zero instruction and S field does not specify YS, YD, or YDP1.
RIR(11:15)	Module zero instruction.
USR(12:15)	Not module zero instruction and S field specifies YS.
UDR(08:11)	Not module zero instruction and S field specifies YD.
UDR(08:10), 1	Not module zero instruction and S field specifies YDP1.
K=0	RSA0

ALCH Bus/BLCH Bus (Sheet 6). Data is gated onto the A Bus and B Bus from the ALCH and BLCH registers respectively. These registers latch the data presented on the ALCH (00:15) and BLCH (00:15) Busses. These busses can have a number of sources. Data is loaded onto these busses in the CPU when the source comes from the PSW, MDR, MAR, MLC, UDR, or the USR. The CPU uses the encoded ASEL and BSEL lines to determine which registers are to be gated, and uses tri-state MSI devices to multiplex this data during RS001 (Sheet 6).

Data may also be gated onto these busses from the users general registers or the micro-registers (ASTK and BSTK) which resides on the ALU board during RS001 if the stacks are so addressed via ASEL and BSEL.

Data may be gated onto the B Bus at RS021 (within the ALU) when data is fetched from control store.

The ALU also manipulates these busses from its shift gates for multiply/divide and shift type instructions.

Processor Registers. The Memory Data Register (MDR) and Memory Address Register (MAR) have been described in this section under Main Memory Control.

The Memory Location Counter (MLC) (Sheet 9) by convention is used to preserve the memory location of the current user level instruction being emulated. This register may be loaded onto both the A and B Busses and loaded from the S Bus by micro-instruction. This register can also be jammed into the MAR or incremented by micro-control during RS001. The register may be incremented by two along with the MAR if the micro-control also requests an instruction read. (Refer to Section 3.5.3.) It may also be incremented by four under micro-control. The two LSBs of the MLC are implemented using individual flip-flops while the most significant portion uses MSI counters. This is necessary to allow the MLC to increment by two or four. When the MLC is to be incremented by four, the signal P40 (9D6) enables the CEP input, and a clock to the MSI counters (MLCCKA0) (9E1) is generated to increment the counter. When the counter is to be incremented by two, the clock for the second LSB (MLCCKB0) (9D3) is generated along with MLCCKA0, which toggles MLC14 and causes the remaining MLC bits to increment if MLC14 (9E4) is true. The counter is loaded from the ST Bus by activating LDMLC0 (9D2) and MLCCKA0 to load the MSI counters. MLC14 is loaded via the preset/clear inputs, while MLC15 is set via the D input by the clocked logic MLCCKC0 (9D3).

The Memory User Destination Register (MUDR) and Memory User Source Register (MUSR) (Sheet 8) are the primary user destination and source registers. (Refer to Figure 3.) These two registers and the User Instruction Register (UIR)(Sheet 8) are loaded from the Memory Data Bus when an instruction fetch is made from main memory. The logic IWAIT1·MRDY1 is used to strobe the data from the bus. The UIR, as was previously noted, is used to generate the vector to the starting address of the emulation sequence for that particular instruction and is in effect the op-code of the user instruction (Bits 00:07). The MUDR and MUSR store the remaining eight bits of the instruction until the beginning of the next emulation sequence.

The User Destination Register (UDR) and User Source Register (USR) (Sheet 7) are residual control registers which contain the R1 and R2 fields of the instruction being emulated. Data is strobed into these registers from the MUSR and MUDR at the beginning of an emulation sequence by the logic STRB1·REGWT1·D1. The UDR has the additional capability of being loaded from the ST Bus by the logic SSEL001·SSEL011·SSEL021·SSEL030·SSEL041·REGWT1·STROB1. This capability is necessitated by the Load/Store multiple and BXLE type instructions of the emulated language. These registers are used to select the general registers for the emulated sequence and can be gated onto the A and B Busses for arithmetic manipulation.

The Program Status Word (PSW) register (Sheet 7) contains the user Condition Code (C, V, G and L=PSW12:15) plus the interrupt masks for the user level machine (see Section 3.5.3). This register may be loaded onto the A and B Busses and loaded from the ST Bus under control of the micro-program. A peculiarity of the register exists in that the Condition Code bits may be loaded under control of the addressed module by the activation of the signal SCC0 of the Processor Control Bus when the register is not addressed as an S Bus destination and the manipulation has been enabled by the micro-control. This is accomplished by multiplexing ST 12:15 or the respective Condition Code Control Bus bits into the register via a quad 2 to 1 multiplexor (7B3) which is steered by the PSW S Bus gating signal SPSW1 (7D1).

The logic PSWCKB0=SCC1·ENFLG1·REGWRT1·STRB1+SPSW1·REGWRT1·STRB1 (7H6) controls the clocking for PSW 12:15. Control line ENFLG1 is activated when the current or a previous micro-instruction specifies the enabling of the bits via the E field of the micro-control (see Section 3.5.3). Once set, ENFLG1 remains active until it is disabled via the E field of the micro-control, or until the beginning of another emulation cycle (RSA·D1). SCC1 is activated by the addressed module when conditions determined by the design of the module require it to change the Processor flags. SPSW1 is the encoded PSW address of the S Bus destination SSEL00:04.

3.7.2 ALU (refer to Functional Schematic 35-404D08). The ALU is a standard module of the Model 80 architecture and, in fact, is one half of a sandwich board configuration linked to the other half, the CPU, by a number of inter-board connectors. Advantage of this configuration is taken by placing the A and B register stacks, the A Bus and B Bus latches, and the Processor flags of the CPU on this board and allowing the ALU to manipulate them in the implementation of its algorithms. The ALU responds to Module Number 1 when addressed over the Control Bus of the Processor. It is capable of 24 operations specified by the function select lines and KSIG of the Control Bus. These operations are listed in Table 7.

TABLE 7. ALU FUNCTION CODES

FSEL (HEX)	KSIG	OPERATION
0	X	subtract
1	X	add
2	0	subtract with carry (Processor flags)
2	1	subtract with carry (PSW flags)
3	0	add with carry (Processor flags)
3	1	add with carry (PSW flags)
4	X	unused
5	X	logical AND
6	X	Exclusive OR
7	X	logical OR
8	0	shift right
8	1	shift right extended
9	0	shift left
9	1	shift left extended
A	0	rotate right
A	1	rotate right extended
B	0	rotate left
B	1	rotate left extended
C	0	arithmetic shift right
C	1	arithmetic shift right extended
D	0	arithmetic shift left
D	1	arithmetic shift left extended
E	0	signed multiply
E	1	unsigned multiply
F	X	signed divide

Arithmetic State Register (ASR) (Sheet 6). The ALU can be in one of four states, as designated by the conditions of the state registers ASA and ASB. These are further encoded as AS001=ASA0·ASB0, AS011=ASA1·ASB0, AS021=ASA0·ASB1, and AS031=ASA1·ADB1.

When the ALU is not selected, and when it is addressed to do a simple function (FSEL000), the ALU remains in AS001. It is only when the ALU is commanded to do a complex function such as shifts, multiply or divide, (designated by FSEL001), that the ALU clock is enabled, and the arithmetic state is allowed to change from AS001. The various transitions that the counter is allowed to make are specified by the ALU algorithms in this section under ALU algorithms.

The Arithmetic State Register (ASR) is implemented in JK type logic. Obviously, the active logic must be tempered with a clock, which is only activated when the module is addressed and the function selects FSEL001 is active. It is initialized to AS001 when the ALU is not selected. The transition diagram for the ALU is shown in Figure 7 and the active logic for each transition is listed in Table 8.

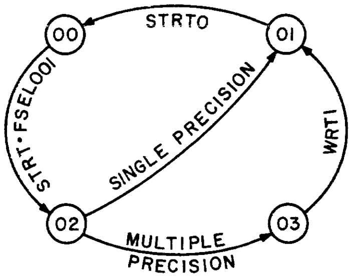


Figure 7. ALU Transition Diagram

TABLE 8. ARITHMETIC STATE REGISTER LOGIC

TRANSITION	ASA LOGIC	ASB LOGIC	COMMENT
AS001 to AS021		J=AS001	Uncondition transition when clock enables.
AS021 to AS011	J=VFLG1· AS021	K=VFLG1· AS021	Divide overflow, abort operation.
	J=ESHFT1	K=ESHFT1· KS1G0· MD0	Single precision shift and end shift count.
AS021 to AS031	J=ESHFT1		Extended shift, K (ASB) inhibited by KS1G0.
	J=ACRY1		Carry from ACNT indicates end of multiply/divide cycle.
AS031 to AS011		K=AWRT1	Most significant half of result written into destination register.
AS011 to AS001	Reset=STRT1	Reset=STRT1	Reset to AS001 when CPU removes STRT1.

ALU Clock (7K5). The ALU clock is a gated oscillator whose basic frequency and duty cycle is determined by a tapped delay line. The factory adjustment sets this at a 10MHz clock frequency with a 40% duty cycle. The clock is enabled for all of the complex operations. It may be inhibited from the test set to allow the frequency to be varied. The enable logic at Gate 19S-08 (7L2) is true when the conditions ALSTRT1· FSEL001· AS010· INHACK0 are met and the result is a clock (ACLK1) (7M9) output. If the test set inhibit (INHACK0) is low before the end of the clock, the generation of the next clock is suppressed. It can be seen from this logic that the clock is also inhibited at AS011 which causes the ALU to become static in that state until the CPU removes STRT.

Arithmetic Counter (ACNT00:03, EACNT) (Sheet 8). The sequential shifting of the ALU is controlled by a module 32 counter that is enabled during AS021. It is during AS021 that the iterative operations of shift and multiply/divide are accomplished, and this counter is used to determine when the transition from this arithmetic state should occur. The counter is used in two different manners, determined by shift or multiply/divide type operations.

1. Multiply/Divide. For these two operations, the counter is initialized to a count of zero. The counter is enabled to count during AS021, and the 16th clock in AS021, as determined by ACRY1, is used to cause the transition to AS031.
2. Shift Type. For these operations, the counter is forced to the 1's complement of the count taken from the B Bus at the transition from AS001 to AS021. The most significant bit (EACNT) is only allowed to load on extended shift operations. The transition from AS021 is thus enabled when the counter reaches the count of 30_{10}, as determined by the logic of ESHFT1=EACNT1· ACNT001· ACNT011· ACNT021· AS021· MD0. From this description, it can be seen that a count of 31_{10} can only be allowed in AS021 when a shift of zero is to be implemented. In this instance, ACRY1 is used to inhibit shifting in AS021.

A, B, and ST Busses; A and B Stacks; and A and B Latches (Sheets 1:5). The Processor busses are generated on the ALU board. The A and B Busses are generated from the ALCH(00:15) and BLCH(00:15) Busses which originate in the CPU. The CPU gates data from selected registers onto these busses during RS001 and RS021. Data may also be gated onto these busses from A and B stacks on the ALU at these times if they are selected by ASEL00:04 or BSEL00:04. (ASTKL/BSTKL contain the user general registers, ASTKH/BSTKH contain the eight micro-registers of the CPU.) In addition, data is also multiplexed onto the ALCH Bus during AS021 to provide shifting of the operand to satisfy the ALU algorithm. The clock for the ALCH/BLCH registers is generated on the ALU (8N9) and integrates the CPU clock (STRB) and arithmetic clock (ACLK) to load the registers at the required times. The ALU also direct clears the BLCH and direct set/clears the ALCH from the MQ register to gate the MQ register onto the ST Bus during AS011. Data may be gated onto these busses except when inhibited by the following logic.

ALCLK INHIBIT LOGIC	
LOGIC	COMMENT
RS000·ALSTRT0	CPU can only load A Bus during RS001.
INHS0	Inhibit shift for zero count in AS021.
AS031 (DIV0+WRT0+AZR00·AZR00)	ALCH cleared for divide correction cycle in AS031.
AS001·ALSTRT1·MD0·KSIG0	Inhibit changing single precision shift operand.

BLCLK INHIBIT LOGIC	
LOGIC	COMMENT
RSA1·ALSTRT0	BLCH can only be loaded by the CPU during RS001+RS021.
AS030·ALSTRT1	BLCH can only be manipulated by the ALU at RS031.
AS031 (DIV0+AWRT1+RZR00·AZR00) (SHFTA0+AWRT1) (MULD+AWRT1)	BLCH cleared for multiply or shift divide correction cycle in RS031.

The ST Bus (Sheet 5) is generated on the ALU. The ST Bus is the integration of the S Bus and the ALU result Bus R00:15, and is the data source for all micro-programmed S Bus destinations. When the ALU is not selected, R00:15 is made inactive by the proper gating of the arithmetic devices employed by the ALU (INTERDATA Part Number 19-067).

Processor Flags (Sheet 6). The Processor flags CFLG, VFLG, GFLG and LFLG are registered in the ALU. These flags are strobed into the appropriate registers by the CPU clock STRB1 when an addressed module activates the Control Bus line SCC0. They reflect the data presented by the addressed module on CCC1, VCC1, GCC1 and LCC1 respectively. The ALU represents these flags in the following manner.

1. VCC1 (Arithmetic Overflow). This flag can only be active on an add/subtract or divide type operation and is set when the correct results cannot be contained within 15 bits plus sign. This is determined by direct setting VFLG1 in the divide algorithm (6J6), when either of the first two iterations of the divide cycle would cause the absolute value of the quotient bit to contain one as determined by SHFTA0, with the exception that it may be subsequently corrected by the logic ACNT031·AZR01·SUM0. VFLG1 may also be set at the end of the divide algorithm if the calculated sign of the quotient is incorrect. (AS011·DSIGN1 + R000.) The flag is set for add/subtract type instructions by activating VCC1 when an overflow is determined by the logic R000·A001 (B001 ⊕ SUM0) + ST001·A000 (B001 ⊕ SUM1).

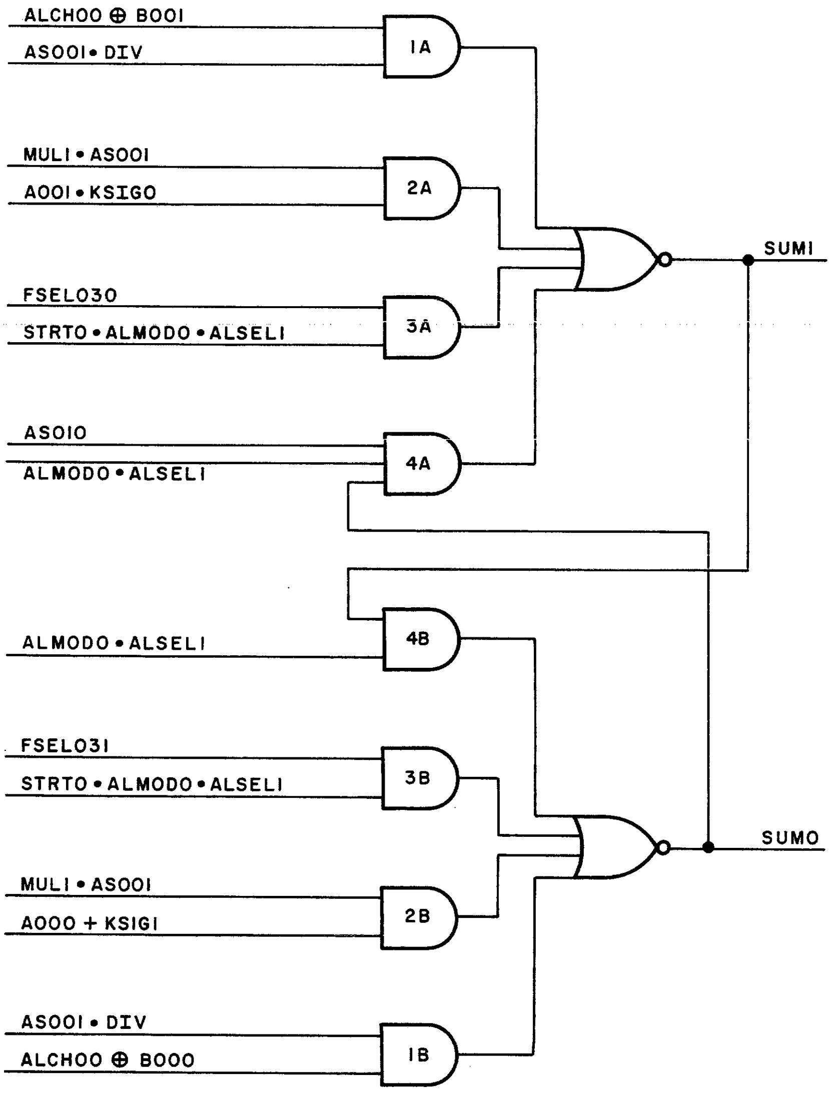
2. CCC1. CCC1 is activated by the ALU for add/subtract or shift type instructions. On shift type instructions, the last bit shifted out is reflected onto CCC1. This bit is captured by the flip-flop at location (6E6) whose input is the correct bit selected by the encoded logic for a particular type shift. For add/subtract, the logic is effectively COUT1·SUM1 and COUT0·SUM0 respectively. The logic for subtract is necessitated by the characteristics of the arithmetic devices used to form the results in that a subtract is accomplished by a 1's complement add plus carry.

   The module signal (MSIG0) from the ALU is effectively the SCC1.

3. LCC1 (6A1). The LCC1 flag represents the sign of any arithmetic operation. This flag is generated by the signal GENL1 (6D8). To accomplish this feature, the sign, plus the occurence of zero in the half of the result stored during AS031 is captured in a quad latch (6C7) when this portion is written into the stack by AWRT1. The sign of this stored half is then used to represent the LFLG for extended shifts and multiply type operations. R001 is used to represent the sign of simple type operations, single precision shifts and divide.

4. GCC1 (6B1). This flag logically represents the occurrence of LCC0 and the results not equal to zero. This is implemented by GCC1=ALSTRT1 (GENL0• ZSET0). GENL0 specifies that LCC0 occurs. ZSET1 (6E9) specifies that the results cannot be zero. This is determined for multiply/divide or extended shifts by examining AZR01 captured for the first halfword during AS031 plus AZR01 for the current half of the word being stored. For add/subtract with carry, the flags (either the PSW or the Processor, as determined by KSIG) are propagated so that ZSET1 cannot be active if the previous result was not zero. For all single precision operations, AZR01 is examined to determine if the current result is zero.

SUM, LMOD00:03, AMOD and Arithmetic Elements. The heart of the ALU is built from the four bit arithmetic/logical elements (INTERDATA Part Number 19-067) (Sheet 5) and associated control logic. The arithmetic elements are used in conjunction with a one-level carry look ahead logic (INTERDATA Part Number 19-068) (5D3). When the ALU is selected, the A and B Busses are gated through these devices onto the ST Bus. When the ALU is not selected, these devices become inactive to allow the "ORing" of the R Bus and S Bus into the ST Bus. The function that these chips perform is determined by the current operation and is selected by LMOD00:03 and AMOD as per the Table 8. During non-logical operations, LMOD00:03 are controlled by the SUM latch. As shown in Table 9, SUM1 and SUM0 are allowed to be true simultaneously for logical operations. SUM is always forced true during AS011 to allow gating the A Bus onto the ST Bus. Figure 8 depicts the simplified SUM logic.



GATES 1A,1B LATCH SUM AS PER DIVIDE ALGORITHM

GATES 2A,2B LATCH SUM AS PER MULTIPLY ALGORITHM

GATES 3A,3B LATCH SUM AS PER FSEL030 FOR ADD/SUB

GATES 4A,4B CROSS COUPLED LATCH HOLDS SUM DURING PERIOD ALU SELECTED. GATE 4A FORCES SUM = 1 DURING AS011

Figure 8. SUM Latch Logic Simplified

TABLE 9. AMOD, LMOD, SUM CONFIGURATIONS

ALU OPERATION	AMODE1	LMOD001	LMOD011	LMOD021	LMOD031	SUM1	SUM0
NOT SELECTED	1	0	0	1	1	1	1
AND	1	0	1	1	1	1	1
OR	1	1	1	0	1	1	1
EXCLUSIVE OR	1	1	0	0	1	1	1
ADD TYPE	0	≡ SUM1	≡ SUM0	≡ SUM0	≡ SUM1	1	0
SUB TYPE	0	≡ SUM1	≡ SUM0	≡ SUM0	≡ SUM1	0	1
SHIFT TYPE	0	≡ SUM1	≡ SUM0	≡ SUM0	≡ SUM1	*	$\overline{\text{SUM1}}$
MULTIPLY	0	≡ SUM1	≡ SUM0	≡ SUM0	≡ SUM1	*	$\overline{\text{SUM1}}$
DIVIDE	0	≡ SUM1	≡ SUM0	≡ SUM0	≡ SUM1	*	$\overline{\text{SUM1}}$

*As per algorithm during AS010, ≡1 during AS011.

MQ Register (Sheet 7). The Multiplier Quotient Shift Register (MQ) is used for all shift and multiply/divide operations. It is comprised of four MSI shift registers. The MQ register is loaded from the A Bus during AS001 by allowing both shift enable left (SEL1) and shift enable right (SER1) (7E6) to be high simultaneously. The appropriate shift enable (SEL1 or SER1) is gated high during AS021 to allow a 16-bit shift in the desired direction. Data is shifted in the register from SR0 (7C9) when the register is shifted right, and from SL0 (7H5) when the register is shifted left.

The MQ register is transferred onto the ST Bus during AS011 by unconditionally clearing the A latches, and conditionally presetting them to reflect the MQ states.

ALU Algorithms

Add, Subtract, AND, OR, and Exclusive OR. These arithmetic operations do not require the ALU clock to be generated and employ combinational logic to perform the required function. When one of these functions is to be performed (determined by FSEL000), STRT1 is used to gate MFIN0 back to the CPU, relying upon the basic CPU clock frequency to allow the operation to be performed by the arithmetic/logical elements and the results to appear upon the ST Bus before the data is strobed into the destination register. The proper mode is selected by the encoding of AMOD, LMOD00:03, and the SUM latch. When the operation to be performed is an add/subtract type, the carry state into the arithmetic element must be generated (5B9). Because the 19-067 device employs internal 1's complement add to perform subtraction, a carry in is generated for subtract. For this reason also, a carry in is generated for add with carry when the appropriate carry flag is true and suppressed for subtract with carry for the same condition.

Shift Type Operations. The ALU can perform both single and double precision shift type operations. When a shift is to be performed, the shift count is taken from the B Bus. At AS001, the A Bus is transferred to the MQ register, and if the operation is to be a double precision shift, the most significant half is loaded onto the A Bus. The A latch and the MQ are then shifted as a 32-bit register the required number of times. If the operation is a double precision shift, the most significant half from the A Bus is stored during AS031 and the sign and zero conditions are saved. During AS011, the MQ register is jammed into the A latches and transferred to the ST Bus and the flags are generated onto the Condition Code Bus. AS011 returns MFIN to the CPU. The shift algorithms are:

AS001 A00:15 → MQ00:15

B12:15 → ACNT00:03

If (KSIG1) B11 → EACNT, ALCH00:15 → A00:15

AS001 → AS021

IZR0 → 1, ILFLG → 1

```
AS021   If (EACNT, ACNT > 29 and KSIG1) AS021 → AS031
        If (EACNT, ACNT > 29 and KSIG0) AS021 → AS011
        If (EACNT, ACNT = 31) INHS0 → 0, CSAVE → 0
        ACNT → ACNT+1
        If (FSEL030)
            A00:14 → A01:15, MQ00:14 → MQ01:15
            If (KSIG1 or ROTATE) A15 → MQ00
            If (KSIG0 and ARITH) A00 → MQ00
            MQ15 → CSAVE
        If (FSEL031)
            A02:15 → A01:14, MQ01:15 → MQ00:14
            If (ROTATE) A00 → MQ15
            If (ARITH) A00 → A00, A01 → CSAVE
            If ($\overline{ARITH}$) A01 → A00, A00 → CSAVE

AS031   AWRT → 1, B00:15 → 0
        Σ A·B → R00:15, R00:15 → ST00:15
        AZR0 → IZR0, R00 → ILFLG
        If (AWRT1) AS031 → AS011

AS011   MQ00:15 → A00:15
        B00:15 → 0, SUM → 1
        Σ A·B → R00:15, R00:15 → ST00:15
        CSAVE1 → CCC1
        If (KSIG1) ILFLG1 → LCC1, SSEL+1 → SSEL
        If (KSIG0) R001 → LCC1
        If (LCC0 and IZR00+AZR00) GCC → 1
        CCC1 → MSIG1, MFIN → 1
```

Multiply. The ALU has the capability to perform both signed and unsigned multiplication on two 16-bit operands. The multiplier is transferred from the A Bus to the MQ register at AS001. The multiplicand is left remaining on the B Bus.

If the multiplier is positive, a product is formed by adding the multiplicand to the shifted partial product conditional upon this operand. If the multiplier is negative, the product is formed by subtracting the multiplicand from the partial product conditional upon the 2's complement of the multiplier. The COMP flip-flop (7C4) is used to complement the multiplier.

Multiplication is accomplished by examining each successive bit of the multiplier as it is shifted out of the MQ register. A 32-bit product is formed by shifting either the A Bus or the sum of A• B back onto the ALCH and into the MQ conditional upon the current multiplier bit. When the operation is completed, the most significant portion is stored during AS031 and the least significant portion is transferred from the MQ register to the ALCH at AS01. The ALU algorithms for multiply are:

```
AS001   A00:15 → MQ00:15

        AME, BME → 1

        ACNT → 0

        If (A000 or KSIG1) COMP → 0, SUM → 1

        M=MQ150• SUM0• COMP0+MQ151 (SUM1+COMP1)

        AS001 → AS021

AS021   ACNT+1 → ACNT

        Σ A• B → R00:15

        If (ACNT=15) AS021 → AS031

        If (M1) R00:14 → A01:15, R15 → MQ00

        If (M0) A00:14 → A01:15, A15 → MQ00

        If (KSIG1• M1) COUT1 → A00

        If (KSIG1• M0) 0 → A00

        If (KSIG0• M1• AZR00) SUM ⊕ B00 → A00

        If (KKIG0• M0) A00 → A00

        If (MQ151) COMP → 0

AS031   If (WRT0) B00:15 → 0

        Σ A• B → R00:15, R00:15 → ST00:15

        AWRT → 1

        R00 → ILFLG, RZR00 → IZR0

        If (AWRT1) AS031 → AS011

AS011   MQ00:15 → A00:15  Σ A• B    R00:15 → ST00:15

        B00:15 → 0

        SSEL+1 → SSEL, SUM → 1

        ILFLG → LCC1

        If (ILFLG0• IZR00+AZR00) GCC → 1

        MFIN → 1
```

Divide. The divide algorithm is implemented by subtracting the divisor from the shifted dividend to determine if it is greater or not. When the dividend is determined smaller than the divisor, the quotient digit for that test is made zero and the dividend is shifted left again to repeat the process. If the dividend is determined to be larger, the quotient digit is made 1 and the left shifted difference is saved as the new dividend. In the implementation of signed divide, if the two operands are of unlike signs, the subtraction is performed by addition of the unlike operands and the 1's complement of the quotient is accumulated. When the complemented quotient is formed, it must be corrected to the 2's complement before it is stored in the Processor.

An obstacle in performing signed division using complementary arithmetic arises when the intermediate dividend is a negative number and both the intermediate quantities (the absolute value of the dividend - divisor) and the remainder equal zero because the logic does not detect the quotient digit of 1. When this case arises, the computed result = true quotient-1, with the remainder equal to the divisor. To detect this, a flip-flop (RZR0) (6K7) monitors this condition and is used to cause a correction cycle after AS031.

Because of the difference in scaling of the divisor (2^{31}) and the dividend (2^{15}) and the fact that the quotient and remainder must both be scaled (2^{15}), an extra division cycle is performed in AS031 to compute Q15. To properly scale the remainder, the last summation is inhibited from shifting, and in fact, if the absolute value of the Q15 digit is 1, the correct remainder is on the ST Bus the first clock of AS031. If the absolute value of the Q15 digit is 0, the correct remainder is on the ALCH, and the BLCH is cleared to allow the contents of ALCH to gate to the ST Bus. It is at this time also that the ALCH may be cleared to cause a correction for the RZR0 error described previously. The algorithms for divide are:

```
AS011    A00:15 → MQ00:15, ALCH00:15 → A00:15

         ACNT → 0, RZR0 → 0

         If (ALCH00 ⊕ B00) SUM → 1

         AS011 → AS021


AS021    If (ACNT < 2 and |Q| =1)VFLG → 1

         If (ACNT=15) AS021 → AS031

         If (VFLG1) AS021 → AS011

         If (ASIGN1·AZR01·MQ000) RZR01 → 1

         If (MQ001) RZR0 → 0

         Σ A·B → R00:15

         If (COUT0 ⊕ A001) A01:15 → A00:14

         If (COUT1 ⊕ A001) R01:15 → A00:14

         MQ00 → A15

         MQ01:15 → MQ00:14

         If (COUT1 ⊕ B001) MQ15 → 1

         ACNT+1 → ACNT
```

AS031 ΣA·B → R00:15, R00:15 → ST00:15

If (AWRT0) MQ01:15 → MQ00:15

If (AWRT0 and COUT1 ⊕ B001) MQ15 → 1

If (AWRT0·AZR01·RZR01) B00:15 → 0, A00:15 →

If (AWRT0 and COUT0 ⊕ A001) B00:15 → 0

AWRT → 1

If (AWRT1) AS031 → AS011

R00 → ILFLG, AZR0 → IZR0

AS011 B00:15 → 0, ΣA·B → R00:15, R00:15 → ST00:15

SSEL+1 → SSEL, SUM → 1

If (VFLG1) AME → 1, BME → 1

If (MQ000·RZR01) CIN → 1

If (DSIGN1·RZR00) CIN → 1

If (DSIGN1 ⊕ R000) VCC1 → 1

ILFLG1 → LCC1

If (ILFLG0·IZR00+AZR00) GCC → 1

MFIN → 1

3.7.3 IOU (refer to Functional Schematic 35-405D08). This section covers all circuits on the IOU board except for the Display and TTY controllers which are covered in Sections 4 and 5. The description references the simplified drawings provided in this section and IOU Functional Schematic 35-405D08.

Multiplexor Bus. The Multiplexor Channel is a byte or halfword oriented I/O system which communicates with up to 255 peripheral devices. The Multiplexor Bus consists of 30 lines; 16 bi-directional Data Lines, 8 Control Lines, 5 Test Lines, and an Initialize Line.

The following general definitions apply to the lines in the Multiplexor Bus:

Data Lines D00:15

The data lines are used to transfer one 8-bit byte or one 16-bit halfword of data between the Processor and the device. One byte of address or command is transferred from the Processor to the device over Data Lines 8:15 (D08:15) when accompanied by either an Address (ADRS) or a Command (CMD) control line. One byte of data or one halfword of data is transferred from the Processor to the device when accompanied by the Data Available (DA) control line. The device, in response to an Acknowledge (ACK) control line or a Sense Status (SR) control line, sends one byte of address or status information to the Processor over D08:15. In response to a Data Request (DR) control line, the device sends either an 8-bit byte or a 16-bit halfword of data to the Processor. The device always sends a Synchronize (SYN) signal to the Processor to indicate that it has either received the data from the Processor or that it has sent the data to the Processor. The SYN signal is removed immediately after the Processor removes the control line.

Control Lines

SR	Status Request. The device controller must present device status to Data Lines D08:15, followed by a SYN.
DR	Data Request. The device controller presents data to Data Lines 8:15 or 0:15 (D08:15 or D00:15), followed by a SYN. If a Halfword (HW) of data is presented, the HW test line is also active.
ACK	Acknowledge. The interrupting device controller presents its address on D08:15, followed by a SYN.
DA	Data Available. The Processor presents data on D00:15 for transfer to the device. The device controller accepts the low byte or the entire halfword and responds with a SYN.
CMD	Command. The Processor presents a Command Byte on D08:15. The device controller accepts the Command Byte and responds with a SYN.
ADRS	Address. The Processor presents an Address Byte on D08:15. The device controller accepts the Address Byte and responds with a SYN.
DACK	Data Channel Acknowledge. The Processor presents an address of zero on D08:15. The ADRS control line and the DACK control line are simultaneously active. The interrupting Data Channel device controller becomes selected and responds with a SYN. As a result of addressing device zero (a null address), only the selected data channel device controller remains addressed.
CL070	This control line is activated by the Processor when a Power Fail condition is detected by the Processor if the Power Fail option is equipped. It is also activated whenever the PPF interrupt occurs.

Test Lines

ATN	Attention. Any device desiring to interrupt the Processor will activate the ATN line and hold this line until an ACK is received from the Processor.
HW	Halfword. The HW line is activated by a halfword oriented device controller whenever it is communicating normally with the Processor. The HW line is not activated when a device controller is operating in the Interleaved Data Channel mode.
DC	Data Channel Request. Any Data Channel device desiring to interrupt the Processor will activate the DC line and hold this line until a DACK is received from the Processor.
DCR	Data Channel Read. The selected Data Channel device controls the state of the DCR line. It will be low active for a Memory Read/Device Write operation.
SYN	Synchronize. This signal is generated by the device to inform the Processor that is has properly responded to a control line.

Initialize Line

SCLR	System Clear. This is a metallic contact to ground that occurs during Power Fail, Power Up or Initialize. The current carrying capability of the contact is limited. External circuits should not be connected directly to it. Refer to the bus buffer or buffered I/O channel for these applications.

NOTE

All control lines, except ACK and DACK, are connected in parallel to all devices. These lines are activated by the Processor in response to an external interrupt. The ACK line is connected in series with all devices. If no interrupt is pending in the first controller when the ACK or DACK signal arrives, the signal is passed on daisy chain fashion to the next controller, and so on until it is captured by the interrupting controller. See definition of ACK and DACK.

All busses are false type, i.e., low level is active, high level is inactive.

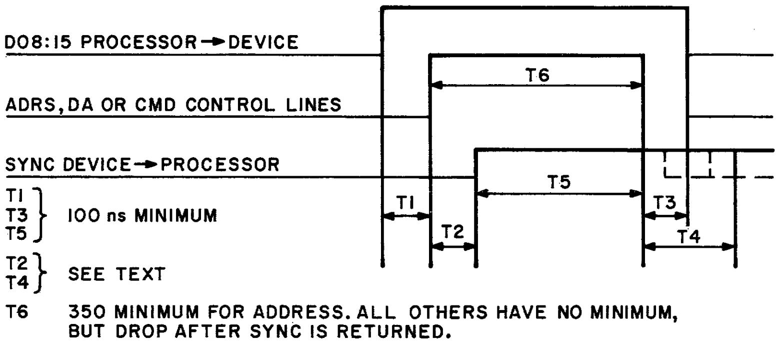
In a typical case, a device controller will receive an 8-bit Address Byte, an 8-bit Command Byte, and either an 8-bit data byte or a 16-bit data halfword from the Processor over the 16 bi-directional Data Lines (D00:15). Likewise, a device controller will send an 8-bit Address Byte, an 8-bit Status Byte, and either an 8-bit data byte or a 16-bit data halfword to the Processor over the 16 bi-directional Data Lines (D00:15). When only a byte of data is transferred, that byte is passed over the lower eight Data Lines (D08:15). The load resistors for all lines in the Multiplexor Bus are located in the Processor.

Each device controller is permitted one TTL load on any of the 16 bi-directional Data Lines, the 8 Control Lines, or the single Initialize Line. Each device controller is permitted one high power open collector TTL OR tie onto each of the 16 bi-directional Data Lines and each of the 5 Test Lines. This gives the Processor a basic Multiplexor Bus drive capability of 9 device controllers. A Multiplexor Bus Buffer is available for extending the drive capability of the Multiplexor Bus incrementally by 9.

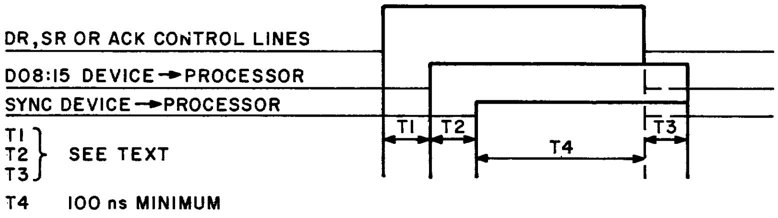
Multiplexor Channel Timing. Both the Input and Output operations on the Multiplexor Channel make use of request/response signaling. This allows the system to run at its maximum speed whenever possible, but permits a graceful slowdown if the characteristics of a particular device controller requires signals of longer duration. Device controller designs should keep Multiplexor Channel usage as fast as possible, consistent with practical circuit margins. Doing this assures the fastest computer input/output operation when a system is configured with a number of peripheral devices.

Timing for typical Input/Output operations are shown on Figure 9. On the Output operation, the Processor places a signal on the data lines followed by an appropriate control line signal. This stagger (T1) will vary, but it is guaranteed to be at least 100 nanoseconds. When the device controller has received the Output Byte, the SYN signal is returned to the Processor, which terminates the control line signal. Realizing that T5 is 100 nanoseconds minimum, the SYN delay T2 should be only long enough to guarantee proper reception of the Output Byte. The control line/data line removal time (T3) is important where singal-rail to double-rail operation is used. A minimum of 100 nanoseconds is guaranteed for T3. For SYN generation the control line signal is DC coupled through the gates to form the SYN signal. The SYN removal time (T4) should be minimized. This delay should not be unnecessarily extended since the Processor will not begin another Input/Output operation until SYN is removed.

It should be emphasized that the times shown on Figure 9 are defined for signals on the Multiplexor Channel. Within a given controller, one signal may flow through more gates than another signal and these delays must be considered.


D08:15 PROCESSOR→DEVICE
ADRS,DA OR CMD CONTROL LINES
SYNC DEVICE→PROCESSOR
T6
T5
T1
T2
T3
T4
T1 T3 T5 100 ns MINIMUM
T2 T4 SEE TEXT
T6 350 MINIMUM FOR ADDRESS. ALL OTHERS HAVE NO MINIMUM, BUT DROP AFTER SYNC IS RETURNED.

(a.) OUTPUT



(b.) INPUT

Figure 9. Multiplexor Channel Timing

For the Input operation, the Processor places a signal on a control line. The currently addressed device controller should gate signals to the data lines as soon as possible to keep T1 at a minimum. The SYN delay (T2) must guarantee that the Input Byte is on the data lines considering the slowest data gates and the fastest SYN gates. The Processor will remove the control line signal when SYN is received with a minimum delay (T4) of 100 nanoseconds. With SYN and the byte gate DC coupled to the control line, the removal delay (T3) is the sum of the corresponding gate delays. The Processor considers the operation complete when SYN falls.

When the control signal is ACK, the delay T1 will include the cumulative contention circuit delays for all the controllers between the responding controller and the Processor. This is less than the Processor time-out even with the maximum limit of 255 controllers.

NOTE

With a SYN delay of 50ns, device controllers must be designed to accept a minimum width of 170ns on all control line pulses except ADRS and DACK which are guaranteed to be 350ns minimum. The SYN delay in the device controller may be increased to effectively lengthen the control line pulses if it is absolutely necessary. It is essential to realize that after the Processor initiates a control line signal, the Processor does nothing until the SYN signal is returned by the device controller and the data transfer rates are decreased proportionally. While this may not affect a particular controller, the over-all system performance is degraded. Furthermore, if a device controller fails to respond with a SYN in the time-out period of about 15-35 microseconds, the Processor aborts the instruction.

I/O Control. Functions and S MUX. The I/O control responds to module address 2 on the MDSL000:020 lines, gating the Start (STRT0) (1R1) signal from the CPU to generate the GSTRT1 (1N4) signal. This is the master timing pulse for all operations. It initiates all Multiplexor Channel sequencing and gates data to the S Bus and CC Bus for non-D Bus functions.

Five function lines (FSL000:030 and KSIG0) are received, buffered and partially decoded as shown on Sheet 1. The final decoding for the S MUX, D MUX and CC MUX is described in the corresponding section. The function gating on Figure 10 shows the complete bit pattern for all 32 functions with the resulting byte manipulations and gating.

HEX. EQUIV. OF FSEL		FSEL				KSIG	CAI5	HW	MAI5=0 OR HW=0		MAI5=1 OR HW=1		OTHER
	FUNCTION	0	1	2	3				DESTINATION (H)	DESTINATION (L)	DESTINATION (H)	DESTINATION (L)	
0	RD	0	0	0	0	0	0/1	X	D(L) → S(H)	B(L) → S(L)	B(H) → S(H)	D(L) → S(L)	ZERO → CC
	RDR	0	0	0	0	1	X	X	ZERO → S(H)	D(L) → S(L)	NA	NA	
1	WD	0	0	0	1	0	0/1	X	ZERO → D(H)	B(H) → D(L)	B(H) → D(H)	B(L) → D(L)	ZERO → CC
	WDR	0	0	0	1	1	X	X	B(H) → D(H)	B(L) → D(L)	NA	NA	
2	SS	0	0	1	0	0	0/1	X	D(L) → S(H)	B(L) → S(L)	B(H) → S(H)	D(L) → S(L)	D(12:15) → CC
	SSR	0	0	1	0	1	X	X	ZERO → S(H)	D(L) → S(L)	NA	NA	D(12:15) → CC
3	OC	0	0	1	1	0	0/1	X	ZERO → D(H)	B(H) → D(L)	B(H) → D(H)	B(L) → D(L)	ZERO → CC
	OCR	0	0	1	1	1	X	X	B(H) → D(H)	B(L) → D(L)	NA	NA	
4	* RDH	0	1	0	0	0	X	0/1	D(L)1 → S(H)	D(L)2 → S(L)	D(H) → S(H)	D(L) → S(L)	ZERO → CC
	STBR	0	1	0	0	1	X	X	B(H) → S(H)	A(L) → S(L)	NA	NA	
5	* WDH	0	1	0	1	0	X	0/1	B(H) → D(L)1	B(L) → D(L)2	B(H) → D(H)	B(L) → D(L)	ZERO → CC
	LBR	0	1	0	1	0	X	X	ZERO → S(H)	B(L) → S(L)	NA	NA	
6	ACK	0	1	1	0	0	X	X	ZERO → S(H)	D(L) → S(L)	NA	NA	ZERO → CC
	LDWAIT	0	1	1	0	1	X	X	NA	NA	NA	NA	B(00) → FWAIT
7	SMCR	0	1	1	1	0	X	X	MCR(H) → S(H)	MCR(L) → S(L)	NA	NA	MCR(12:15) → CC
	CMCR	0	1	1	1	1	X	X	NA	NA	NA	NA	B(11:15) CLEARS MCR(11:15)
8	RDA	1	0	0	0	0	0/1	X	SAME AS RD AND RDR BUT PRECEDED BY ADDRESS CYCLE [A(L) → D(L)]				
	RDRA	1	0	0	0	1	X	X					
9	WDA	1	0	0	1	0	0/1	X	SAME AS WD AND WDR BUT WITH ADDRESS CYCLE				
	WDRA	1	0	0	1	1	X	X					
A	SSA	1	0	1	0	0	0/1	X	SAME AS SS AND SSR BUT WITH ADDRESS CYCLE				
	SSRA	1	0	1	0	1	X	X					
B	OCA	1	0	1	1	0	0/1	X	SAME AS OC AND OCR BUT WITH ADDRESS CYCLE				
	OCRA	1	0	1	1	1	X	X					
C	* RDHA	1	1	0	0	0	X	0/1	SAME AS RDH BUT WITH ADDRESS CYCLE				
	STB	1	1	0	0	1	0/1	X	A(L) → S(H)	B(L) → S(L)	B(H) → S(H)	A(L) → S(L)	
D	* WDHA	1	1	0	1	0	X	0/1	SAME AS WDH BUT WITH ADDRESS CYCLE				
	LB	1	1	0	1	1	0/1	X	ZERO → S(H)	A(H) → S(L)	ZERO → S(H)	B(L) → S(L)	
E	DACK	1	1	1	0	0	X	X	ADDRESS AND DACK; ZERO → D(H)/D(L)		D(H) → S(H)	D(L) → S(L)	AUTOMATIC RDH
	EXB	1	1	1	0	1	X	X	B(L) → S(H)	B(H) → S(L)	NA	NA	
F	POW	1	1	1	1	0	X	X	NA	NA	NA	NA	RELEASE SCLR RELAY
	POUT	1	1	1	1	1	X	X	NA	NA	NA	NA	B(12:15) → CABLE

* = FOR RDH,WDH,RDHA AND WDHA; TWO DATA CYCLES WILL BE GENERATED FOR BYTE CONTROLLERS (IE•HW=0).

Figure 10. I/O Module Function Gating

Partial decoding of RDWDH1, MACK0 and MACK1 (1L9) is performed since several circuits use these signals in common. The RDWDH1 line is active for any halfword operation, with or without an address cycle. The MACK lines are active for both the ACK and DACK functions.

Examination of Figures 3 and 10 with respect to S Bus gating shows that ten function codes define all the byte gating combinations. These are derived and listed on Figure 11. The six-to-one S MUX's are implemented with four-to-one tri-state MUX's (19-073) and open collector gates (19-056) tied together at the S Bus as shown in the simplified drawing.

S-MUX CONTROL

FUNCTION CODE	DESTINATION S(H)/S(L)	INPUT FUNCTIONS
FC1	D(L)/B(L)	(CA150) [RD1 + SS1]
FC2	B(H)/D(L)	(CA151) [RD1 + SS1]
FC3	Z/D(L)	[RDR1 + SSR1 + ACK1]
FC4	D(H)/D(L)	[RDH1 + DACK1]
FC5	B(H)/A(L)	[STBR1 + (STB1) (CA151)]
FC6	Z/B(L)	[LBR1 + (LB1) (CA151)]
FC7	A(L)/B(L)	(STB1) (CA150)
FC8	Z/A(H)	(LB1) (CA150)
FC9	B(L)/B(H)	EXB1
GM	M(H)/M(L)	SMCR1

		A	B	S-MUX HIGH	S-MUX LOW
D(L)	0	0	0	*C1	*C2+*C3+*C4
A(L)	1	1	0	C7	C5
B(L)	2	0	1	C9	*C1+C6+C7
B(H)	3	1	1	*C2+C5	C9

NOTE: FUNCTION CODES DESIGNATED WITH * ARE GATED [BY STROBE LINES STLC/STHO] WITH THE D-BUS SIGNAL TERM1.
ALL OTHERS ARE GATED WITH THE DECODED START PULSE, GSTRT1.

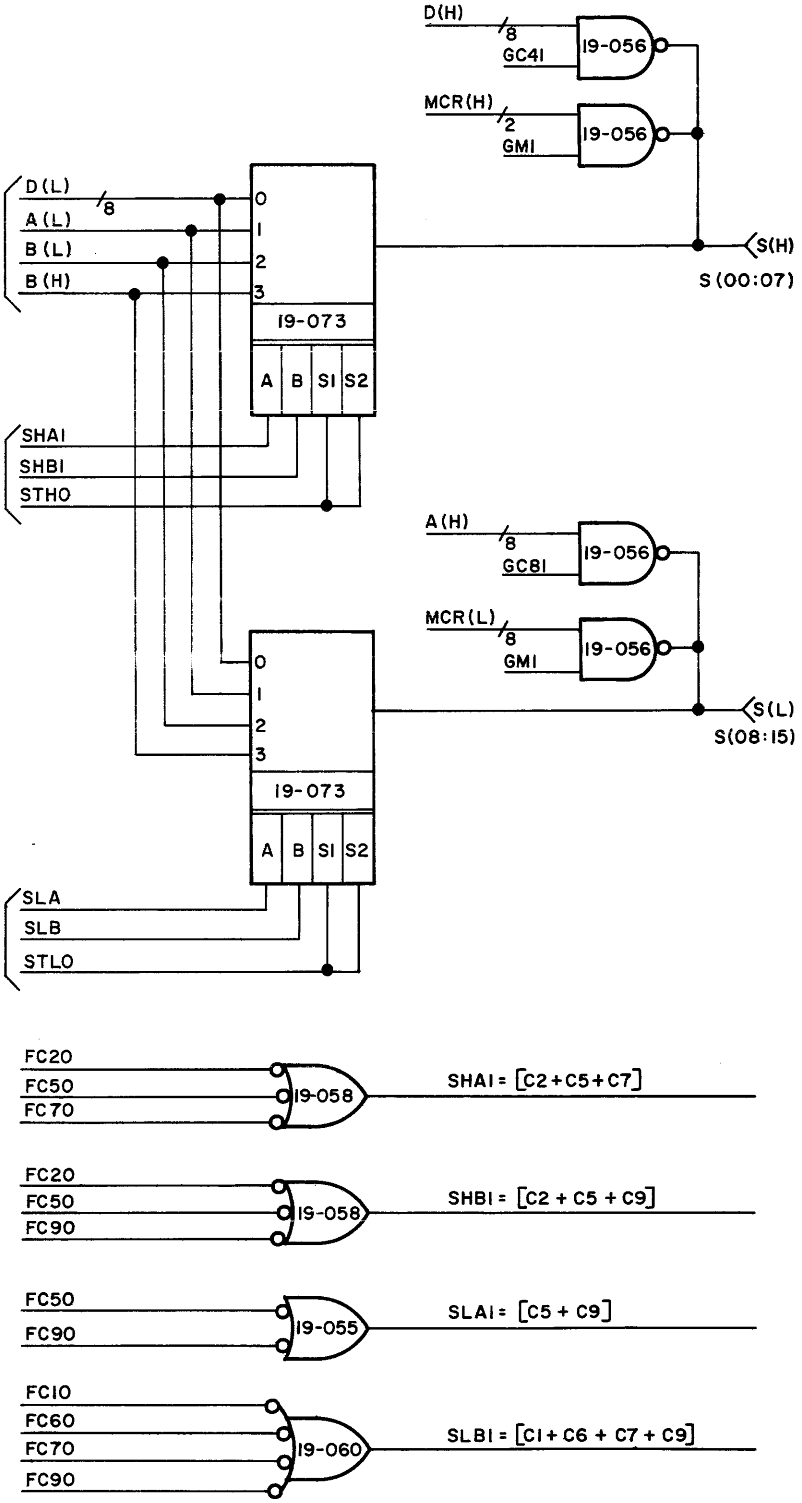

D(H)
8
GC41
19-056
MCR(H)
2
GM1
19-056
D(L)
8
A(L)
B(L)
B(H)
0
1
2
3
19-073
A
B
S1
S2
S(H)
S(00:07)
SHA1
SHB1
STH0
A(H)
8
GC81
19-056
MCR(L)
8
GM1
19-056
0
1
2
3
19-073
A
B
S1
S2
S(L)
S(08:15)
SLA
SLB
STL0
FC20
FC50
FC70
19-058
SHA1 = [C2+C5+C7]
FC20
FC50
FC90
19-058
SHB1 = [C2 + C5 + C9]
FC50
FC90
19-055
SLA1 = [C5 + C9]
FC10
FC60
FC70
FC90
19-060
SLB1 = [C1 + C6 + C7 + C9]

Figure 11. Module 80 IOU S MUX Logic

A note of explanation is in order concerning the byte designations used. Byte B(H) refers to Bits 00:07 from the corresponding B Bus receivers and A(L) refers to Bits 08:15 from the A Bus receivers. In the case of data from the D Bus, D(H) refers to Bits 00:07 in the data register and normally comes from the D Bus Bits 00:07. However, on an RDH operation with a byte oriented device, only D Bus lines 08:15 are used. The first byte is stored in Data Register 00:07 and the second byte in Data Register 08:15.

The A and B select signals for the four-to-one MUX's are generated by OR gates from the function codes (bottom of Figure 11). Any low active input on a gate drives the output high. While the S(H) and S(L) MUX's have the same data inputs, the MUX select codes are different. Input Code 0 requires no action at the OR gates since their outputs are normally low. The strobe generators for STH0 (1A9) and STL0 (1D9) must be active for all four select codes, but not when the open collector gates are used. MUX timing is provided by the GSTRT1 (1A1) signal for non D Bus operations and by the termination signal (TERM1) (1A1) when the Multiplexor Channel is used.

The receivers for the A Bus and B Bus as well as the full S MUX are shown on Sheet 3. The S MUX control is on Sheet 1.

Several partial decoders are used. The RDSS1 (1G5) line is active for indexed RD or SS functions. The STBLB1 (1F6) signal is active for STB or LB functions, both indexed and register type. Logic for FC5 and FC6 share the RM151 (1E6) signal which is true for [FSL000+(CA151) (FSL001)]. A composite function, FC123X1 (1D5) is true for FC1 or FC2 or FC3. The function code logic and MUX select gates SLA1 and SLB1 (1E9); SHA1 and SHB1 (1F9) are connected as described on Figure 11.

The timing pulses GSTRT1 (1N5) and TERM1 (1A1) are used on the four-to-one MUX strobes; STL0 (1D9) and STH0 (1A9). The function(s) decoded by each portion of the 19-062 AOI (AND, OR and Invert) circuit is written inside the gate symbol.

Function code FC41 (1B5) gates D(L) to S(L) with STL0 in addition to gating D(H) to S(H) with GC41 and the 19-056 open-collector gates.

In the case of FC8, the GC81 (1E9) signal gates A(H) to S(L) using open-collector gates; none of the four-to-one MUX's are used.

Multiplexor Channel. The circuits which generate the D Bus and the companion control/test lines are described in this section. As seen on Figure 12 there are five general circuit groups.

1. Input circuits

2. Cycle counter

3. Control line logic and bus drivers

4. Data line logic, bus drivers and data registers

5. Timing and control logic

The D Bus Enable line (DBEN1-1L9) is active for either MACK0 (1J9) (i.e., ACK or DACK) or RDWDH0 (1L6), or FSL011 (1L6) in the low active state (see Figure 10). All D Bus operations begin when DBEN1 is gated by the GSTRT1 signal (2A5) to produce the DSTRT0 and DSTRT1 signals (2A5). These signals in turn are used by the STRT Timer (6E8), the cycle counter and the timing control circuit.

The SYN0 test line is the main source of timing in the request/response signalling system used on the Multiplexor Channel. It must be carefully terminated and deglitched before being presented to the cycle counter and timing control. The leading edge of the test line is gated by KD1 (2A7) to direct set the SYN flip-flop (2D7). When the control line signal to the bus is terminated, the KD flip-flop is cleared and the test line is now connected to the clock input of the D type, edge triggered, SYN flip-flop where the trailing edge clears the flip-flop. Once the SYN flip-flop has been set or cleared, ringing or noise near the edges of the SYN0 signal is ignored. The trailing edge of XSYN1 (2C7) is extended on output operations by the low KSYN0 signal (2A7). This is described in detail later.

The Halfword test line (HW0) (2H2) produces the signals HW1 and HW0A which control data gating on the D Bus and indicate to the Multiplexor Channel circuits whether a byte oriented or halfword controller is in use. An exception is the halfword Data Channel type controller which does not activate the HW0 test line. A pseudo signal KHW0 (generated by the cycle counter) is ORed into the test line receiver to properly condition the data gating circuits.

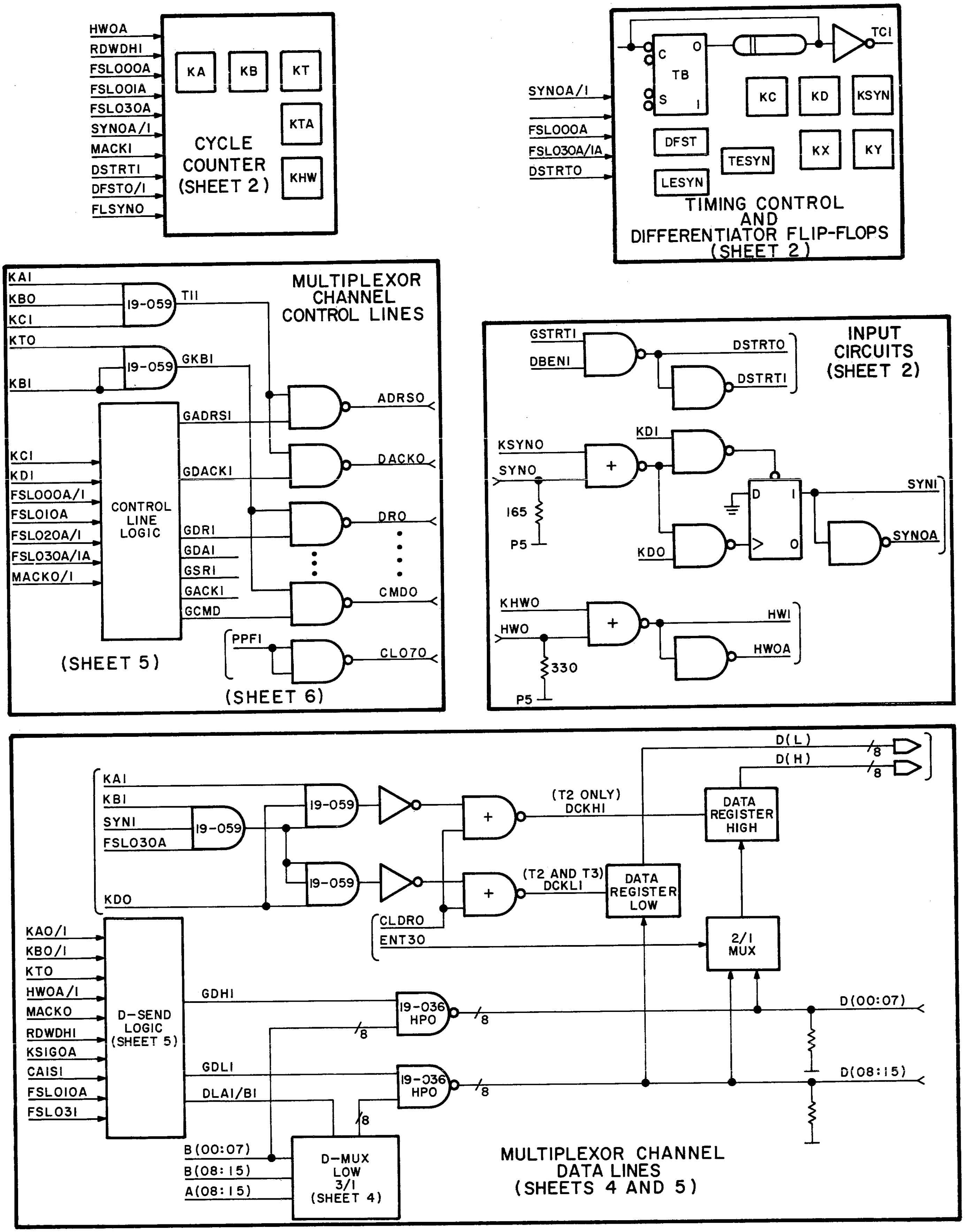
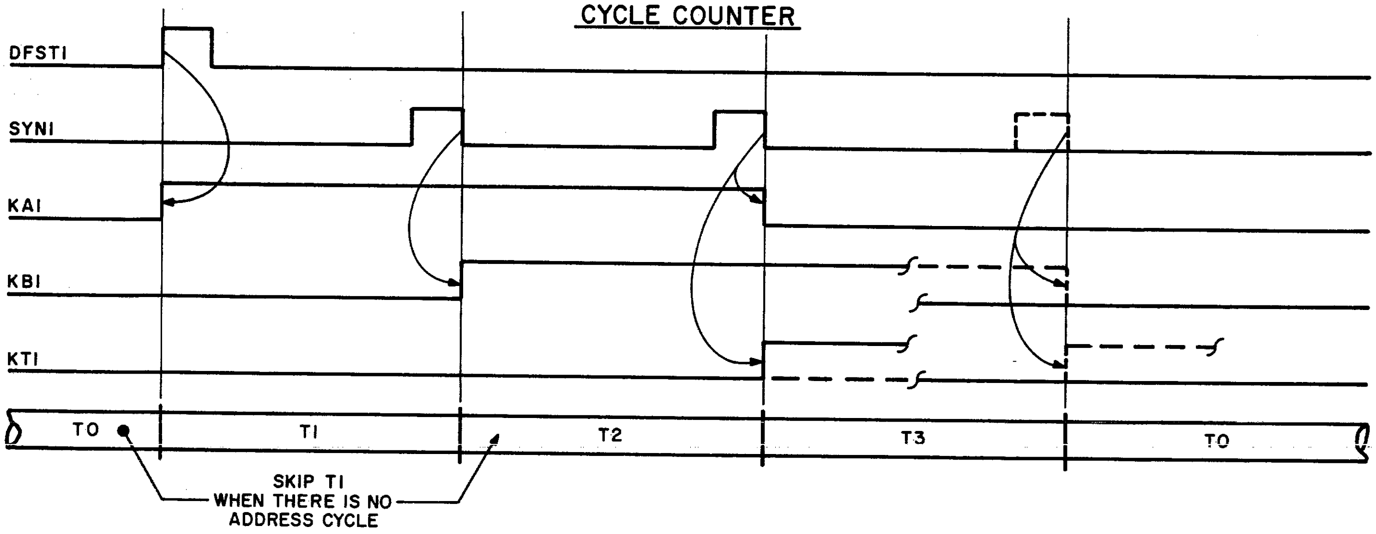

HWOA
RDWDHI
FSL000A
FSL001A
FSL030A
SYNOA/I
MACKI
DSTRTI
DFSTO/I
FLSYNO
KA
KB
KT
KTA
KHW
CYCLE COUNTER (SHEET 2)
SYNOA/I
FSL000A
FSL030A/IA
DSTRTO
C
O
TB
S
1
TCI
KC
KD
KSYN
DFST
TESYN
KX
KY
LESYN
TIMING CONTROL AND DIFFERENTIATOR FLIP-FLOPS (SHEET 2)
KAI
KBO
KCI
KTO
KBI
19-059
TII
19-059
GKBI
MULTIPLEXOR CHANNEL CONTROL LINES
GADRSI
ADRSO
KCI
KDI
FSL000A/I
FSL010A
FSL020A/I
FSL030A/IA
MACKO/I
CONTROL LINE LOGIC
GDACKI
DACKO
GDRI
DRO
GDAI
GSRI
GACKI
GCMD
CMDO
PPFI
CLO70
(SHEET 5)
(SHEET 6)
GSTRTI
DBENI
DSTRTO
DSTRTI
INPUT CIRCUITS (SHEET 2)
KSYNO
SYNO
KDI
+
165
P5
D
1
0
SYNI
KDO
SYNOA
KHWO
HWO
+
HWI
HWOA
330
P5
D(L)
D(H)
8
8
KAI
KBI
SYNI
FSL030A
19-059
19-059
+
(T2 ONLY) DCKHI
DATA REGISTER HIGH
KDO
19-059
+
(T2 AND T3) DCKLI
DATA REGISTER LOW
CLDRO
ENT30
2/1 MUX
KAO/I
KBO/I
KTO
HWOA/I
MACKO
RDWDHI
KSIGOA
CAISI
FSL010A
FSL031
D-SEND LOGIC (SHEET 5)
GDHI
19-036 HPO
8
8
D(00:07)
GDLI
DLAI/BI
19-036 HPO
8
D(08:15)
8
B(00:07)
B(08:15)
A(08:15)
D-MUX LOW 3/1 (SHEET 4)
MULTIPLEXOR CHANNEL DATA LINES (SHEETS 4 AND 5)

Figure 12. Multiplexor Channel Logic

Two edge triggered D type flip-flops KA and KB (2K5), connected as a Johnson Counter, together with the KT (2M4) and KHW flip-flops (2N4) make up the cycle counter circuit. The sequence starts with DFST0 setting the KA flip-flop (2J4). When there is no address cycle, DFST1 and FSL000A (2H3) also set the KB flip-flop (2L4). The counter advances on the trailing edge of the composite SYN1/SYN0A signals which are stretched (if necessary) on the ADRS, CMD and DA cycles. This insures that any byte gated to the D Bus remains for at least 100 nanoseconds after the associated control line signal is removed. The sequence stops when the Terminate flip-flop (KT) (2M4) is set and the MFIN line to the CPU is activated (1H1 and 1G9). Operation of the KSYN flip-flop (2G7), which provides the SYN stretch, will be described later.

A timing chart for the cycle counter is shown on Figure 13. From the idle time period T0, the counter is preset into period T1 or T2 depending upon the presence or absence of an address cycle. The sequence normally terminates at the end of T2 unless a halfword operation with a byte oriented device requires a second data cycle, T3 (ENT30) (2L2). The KHW flip-flop (2N5) is set after a DACK operation. It provides the pseudo HW1 signal (2H2) required by the next Data Channel operation (RDH or WDH) after which it is cleared.

CYCLE COUNTER



D-MUX CONTROL

FUNCTION CODE	DESTINATION D(H)/D(L)	INPUT FUNCTIONS	CYCLE PERIOD
FCA	Z/A(L)	ANY ADDRESS CYCLE EXCEPT DACK	T1
FCB	Z/B(H)	(CAI50) [WD + OC] + (HWO)(WDH)	T2
FCC	B(H)/B(L)	(CAI51) [WD + OC] + WDR + (HW1)(WDH) + OCR	T2
FCD	Z/B(L)	(HWO)(WDH)	T3

		A	B	D-MUX LOW
A(L)	0	0	0	(FCA)(T1)
GND	1	1	0	NA
B(L)	2	0	1	(FCC)(T2) + (FCD)(T3)
B(H)	3	1	1	(FCB)(T2)

DLA0 = T1 + (FCC)(T2) + (FCD)(T3)
DLB0 = T1
GDH1 = (T2)(FCC)

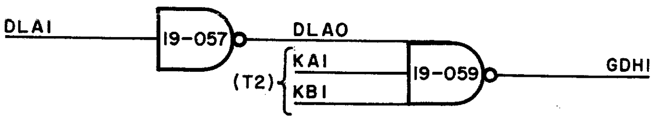


Figure 13. D Multiplexor Logic and Cycle Counter

Eight bus drivers (5M7 and 6M3) are the source of the Multiplexor Channel control lines. With the exception of CL070 (6M3), the two inputs are cycle gating and function decoder signals. The lines T11 and GKB1 (5L8) are active during the address and data cycles respectively. Function decoder gates are configured as per Figure 10 and contain the intra-cycle timing signals KC1 (2G4) and KD1 (2G6). When data is placed on the D Bus for ADRS/DACK, CMD, or DA operations, the KC1 pulse provides the control line timing, delayed 100 nanoseconds from the beginning of the cycle. For ACK, SR, or DR operations, the non-delayed KD1 pulse gates the control lines. Both KC1 and KD1 are removed 100 nanoseconds after SYN0 is received, in accordance with Multiplexor Channel timing requirements. The signal CL070 (6N3) goes low active when primary power failure is detected, PPF1 (or INIT or P0FF) high.

The D Bus consists of 16 bidirectional data lines terminated on the IOU board. The 19-036 drivers on Figure 12 are operated in two groups. Gating from B(00:07) to D(00:07) uses the high byte group. The low byte group gates the output of a three-to-one MUX onto D(08:15). Unlike the static selection of the S MUX, the D MUX selections change on every cycle of the sequence. The data registers are the D Bus receivers.

Gating to the D Bus is defined by four, time-dependent, function codes as shown on Figure 13. The periods T1, T2 and T3 are combined with the function codes FCA, FCB, FCC and FCD to generate MUX select and driver gating signals. The bus drivers, D MUX, and control circuits are located across the top of Sheet 4 with the data registers and receive MUX on the bottom. The 19-038 multiplexors are always enabled; i.e., strobes at ground. Bus gating GDL1 (4L3) and GDH1 (4G3) are controlled by FSL031 (5A7) which is only active on data output functions. When time period T1 exists for an address cycle, it generates GDL0 (5F6) for all functions except ACK and DACK (MACK0) (5A6). The GDH1 is formed as shown on Figure 13 and at location 5G8. The select codes (DLA1 and DLB1) and circuits are designed to produce low level zero states when input conditions are satisfied.

The 19-071 edge triggered D latches, used for data registers, load on the low-to-high transition of the clock leads DCKL1 and DCKH1 (4G6). The high byte register normally receives data from D(00:07) during period T2 (KA1 and KB1) gated through the two-to-one MUX by ENT30 (4H6) in the high state. For the double data cycle, ENT30 is low active so the first byte on D(08:15) enters both DR(00:07) and DR(08:15) during T2. The second byte on D(08:15), during T3, is registered in DR(08:15) only to overwrite the first byte. Clock logic for DCKL1 and DCKH1 (5M9) uses the common term KB1•SYN1•FSL030A which is active for all input functions, including ACK and DACK, during periods T2 and T3. Final gating with KD0 loads the registers at the moment the selected control line signal is removed; i.e., about 100 nanoseconds after the beginning of the SYN signal when the data lines have settled. The Data Register outputs feed the S MUX's and the CC MUX as shown on Figure 3.

The timing and control circuits provide the intra-cycle timing and SYN stretching features mentioned in earlier sections. These circuits consist of six edge triggered J/K flip-flops, a two stage counter, an R/S flip-flop, a 100 nanosecond tapped delay line, and the interconnecting logic. Three of the flip-flops, DFST (2D4), LESYN (2G2), and TESYN (2D6) detect the negative transitions of the DSTRT0, SYN0A and SYN1 signals respectively, and feed the delay line R/S flip-flop combination.

The TB flip-flop (2C3) is set by a low signal on Terminal 10, 12 or 13. A low signal on Terminal 01, 02 or 04 clears the flip-flop. When a momentary set pulse is applied, the high-to-low transition at TB0 travels down the delay line emerging after X nanoseconds as TC0 (2D2) to clear the flip-flop. This produces pulses TC0 and TC1 which are X nanoseconds wide and start X nanoseconds after the set TB pulse (where X is the tap delay plus the flip-flop transition times). Using the 50 nanosecond tap (Terminal 13 of the line), X is approximately 50 nanoseconds and the trailing edge of TC1 occurs 100 nanoseconds after the set pulse. When the set pulse is long enough to still be present after the end of TC0, TB0 again goes low to generate another pulse; i.e. the circuit acts like a gated oscillator. As seen on the timing charts which follow, both the single and multi-pulse modes are used.

The timing chart on Figure 14 shows a data output operation (CMD or DA) with an address cycle. The sequence starts with period T1 when the KA flip-flop is set. At the end of the first SYN pulse, the KB flip-flop is set and period T2 starts. The end of the second SYN pulse clears the KA flip-flop and sets the KT flip-flop. With KT0 low, gating to the D Bus/control lines is suppressed (5A7) and the pulse generator is killed (2B3).

On both address and data cycles, the data byte(s) must be on the D Bus at least 100 nanoseconds before the control line signal starts and must remain active for 100 nanoseconds after the control line signal is removed. Furthermore, the control line must remain active for 100 nanoseconds after SYN arrives. The width of the ADRS0 control line pulse must be at least 350 nanoseconds. This insures that the address flip-flop on a controller, separated from the CPU by one or more bus buffers, can be reliably cleared even with a fast SYN response from a local controller.

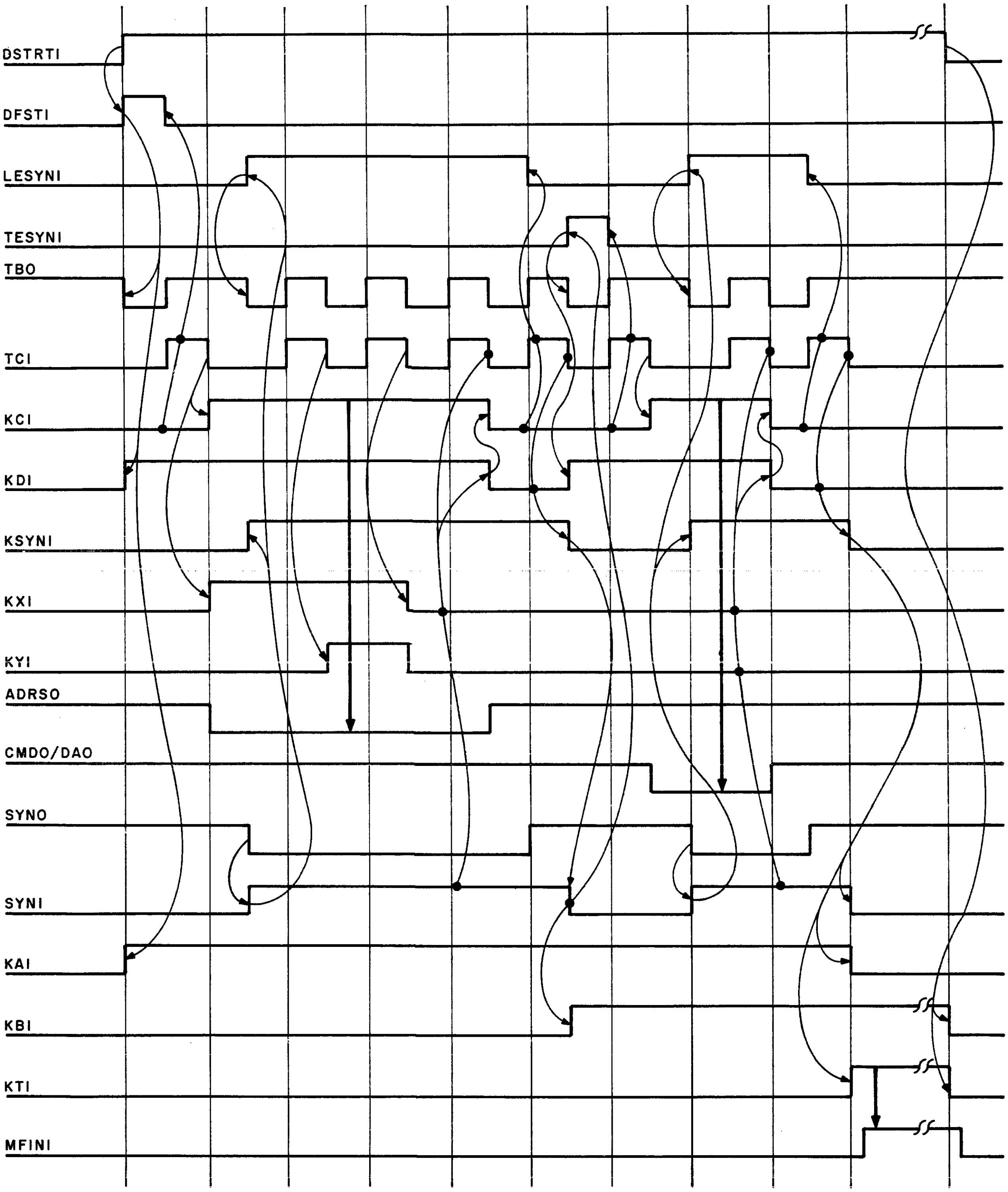

DSTRTI
DFSTI
LESYNI
TESYNI
TBO
TCI
KCI
KDI
KSYNI
KXI
KYI
ADRSO
CMDO/DAO
SYNO
SYNI
KAI
KBI
KTI
MFINI

Figure 14. Multiplexor Channel Timing, ADRS and CMD/DA

The DFST1 lead sets the delay line flip-flop (TB) (2B3) if it is either an output data cycle (FSL030A low) (2A3) or an address cycle (FSL000A low) (2A3). The KD flip-flop (2G6) is always set by DFST. Flip-flop KC (2G4) toggles set at the end of TC1 since its J input (SYN0A) and direct clear (KD1) are both high. KC1 sets the KSYN flip-flop (2G8) and gates the control lines as described earlier. The LESYN flip-flop (2G2) sets on the leading edge of SYN and sets the TB flip-flop again. The KD flip-flop toggles clear on the first TC1 pulse after its K input goes high and in turn direct clears the KC flip-flop. For non-address cycles, the K input to the KD flip-flop (KDK1) goes high as soon as SYN is received, the next TC1 pulse clears the KD flip-flop after 100 nanoseconds. On the address cycle (period T1 with the KB flip-flop cleared), the TC1 pulses are fed to a two stage Johnson Counter, flip-flops KX and KY (2N7). The KDK1 input to the KD flip-flop is held low until after three TC1 pulses have been registered on the KX and KY flip-flops. The next TC1 pulse clears the KD flip-flop. In this manner the minimum width of KC1 and the ADRS0 signal are equal to 300 nanoseconds plus the SYN return delay (KDK1=SYN1•KX0).

The KSYN flip-flop is cleared 100 nanoseconds after the KD flip-flop is cleared since its K input (KD0) is high when the next TC1 pulse arrives. KSYN0 (2A7) forces XSYN1 and SYN1 high as long as the KSYN flip-flop is set. This insures that SYN1 and SYN0A will remain active for at least 100 nanoseconds after KC1 and the control line signals, gated by KC1, are ended. A fast SYN response from a device controller will not be able to terminate the cycle prematurely and violate the timing rules for the D Bus.

Note that the LESYN flip-flop remains set until the first TC1 pulse after the KC flip-flop is cleared. This produces the multi-pulse mode of the delay line; i.e., a group of TC1 pulses at 100 nanosecond intervals. Also note that while the KD flip-flop is not used directly for control line timing, it is part of the logic for the KC and KSYN flip-flops.

The TESYN flip-flop (2D6) sets on the trailing edge of the composite SYN1 signal and sets the TB flip-flop again if an output data cycle is required (FSL031A) (2A4). The KD flip-flop is direct set by TESYN. Timing for the output data cycle is similar to the ADRS cycle with two exceptions. First, the KX and KY flip-flops are not used to stretch the control line signal and second, a double data cycle may be generated for the WDH operation to a byte oriented device. During the T2 SYN pulse, the logic that sets the KT flip-flop (2M4) also produces a low level on SKT0 (2R2). This causes the TESYN flip-flop to ignore the end of SYN1 (since both the J and K inputs are low) and the TB flip-flop is not set. When a double data cycle is needed, the set KT logic does not become active until period T3. The TESYN flip-flop sets on the end of the T2 SYN signal and thus pulses the TB/delay line circuit for timing control during period T3. It also applies to the ADRS/DACK and DR operations.

Figure 15 shows timing for a data input operation (SR or DR) with an address cycle. The TB flip-flop is set with DFST since KC1 is needed for control line gating during the address cycle. It also applies to the ADRS/DACK and DR operations. The KX and KY counter insure the minimum width of the ADRS0 signal. TESYN sets the KD flip-flop at the end of period T1 but does not set the TB flip-flop. KD1 gates the control lines for the input byte(s). The KC and KSYN flip-flops are not used on the data cycle(s). A double data cycle is produced for the RDH operation to a byte oriented device.

For non-address functions, the sequences start with period T2 since the KA and KB flip-flops are both set with DFST. The data cycles on Figures 14 and 15 are essentially the same.

Timing for the ACK function is shown on Figure 16. It consists of a single data cycle (T2). The KC and KSYN flip-flops are not required. The TB flip-flop and the delay are pulsed only by LESYN to time the removal of the control line signals.

On all timing charts, the KT flip-flop generates S Bus and CC Bus gating and eventually the MFIN0 signal. This restarts the CPU clock causing the removal of the STRT0, GSTRT1 and DSTRT0/1 signals.

A group of clear signals insures proper circuit states for initialize and other operations. CLRA0 (2L6) is low for SCLR0A low or any non-D Bus operation (DSTRT1 low). It clears the cycle counter and kills the pulse generator. The KHW flip-flop (2N4), which must remain set from the end of a DACK operation until the end of the next D Bus operation, is direct cleared only by SCLR0A. However, it is clock cleared at the end of every non-DACK operation. CLRB0 (2D8), used by DFST and TESYN, cannot use DSTRT1 for clearing due to a possible race condition when the DFST flip-flop toggles set. It combines SCLR0A, TC1/KD1 (as per timing charts), and MFIN0A; a copy of the MFIN0 generated by the IOU board. CLRC0 (2E9) is essentially a copy of CLRA0 used to reduce the load on CLRA0. CLRD0 (2G3) uses CLRC0 or TC1/KC0 (as per timing charts) to clear the LESYN flip-flop.

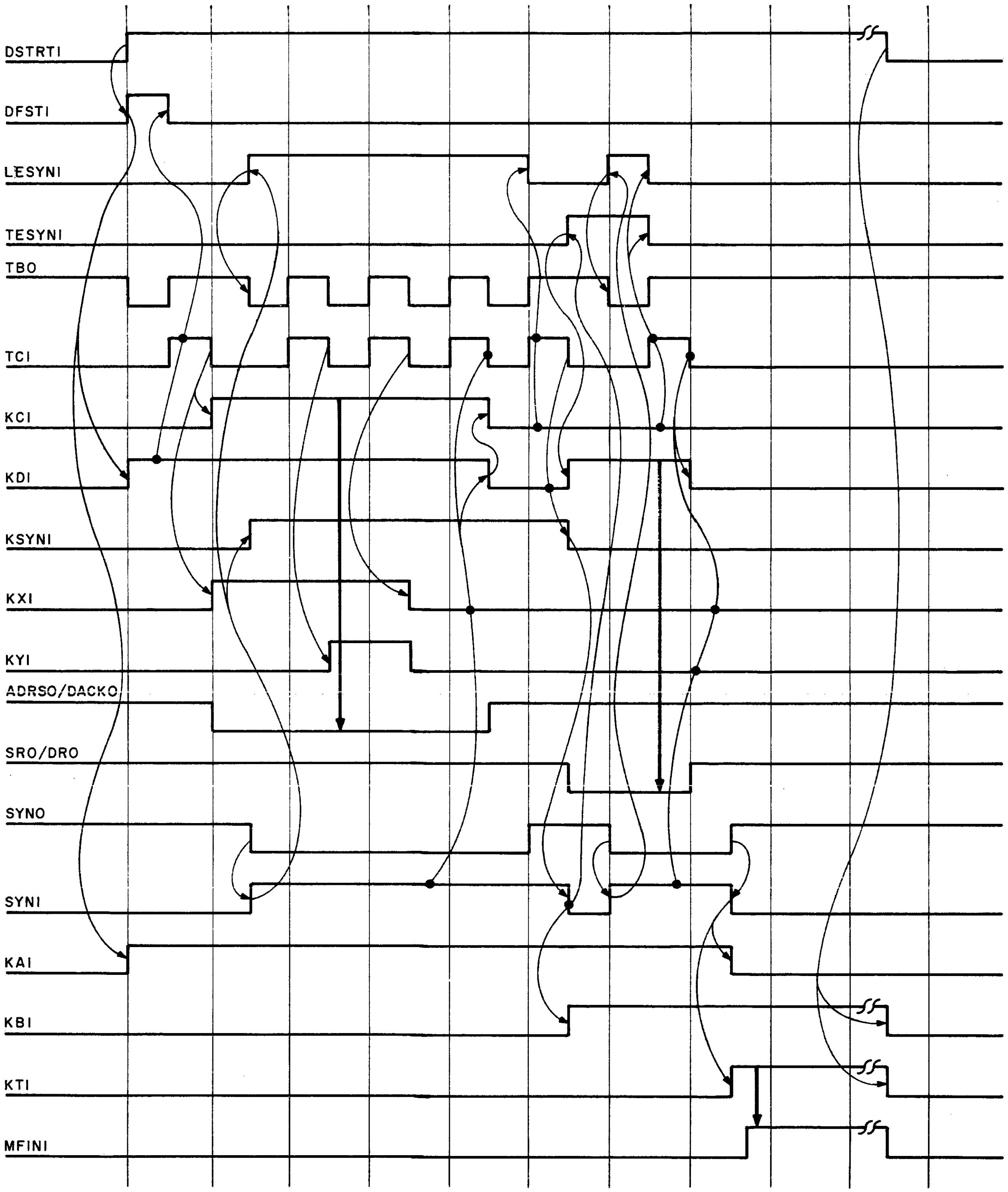

DSTRTI
DFSTI
LESYNI
TESYNI
TBO
TCI
KCI
KDI
KSYNI
KXI
KYI
ADRSO/DACKO
SRO/DRO
SYNO
SYNI
KAI
KBI
KTI
MFINI

Figure 15. Multiplexor Channel Timing, ADRS/DACK and SR/DR

Machine Control Register and CC MUX. The description and general operation of the Machine Control Register (MCR) is covered in Section 3.6.3. The five monitor flip-flops (5E1-5E5) are all connected to toggle set for a high-to-low transition on the signal lead being monitored. Separate clear leads are used. The IPF0, DPF0 and IA0 leads from the back panel are terminated as shown. A composite bit MX121 (5G4) may be strapped to M120 (IA) or M110 (STF) or to both. The five signals (M111, MX121, M131, M141, and M151) together with CATN1 (2J6) and the test straps, are gated to the S Bus by the GMI gate pulse (1N9). The MX12, M13, M14 and M15 signals are ORed to generate the MMF0 (5H3) interrupt to the CPU.

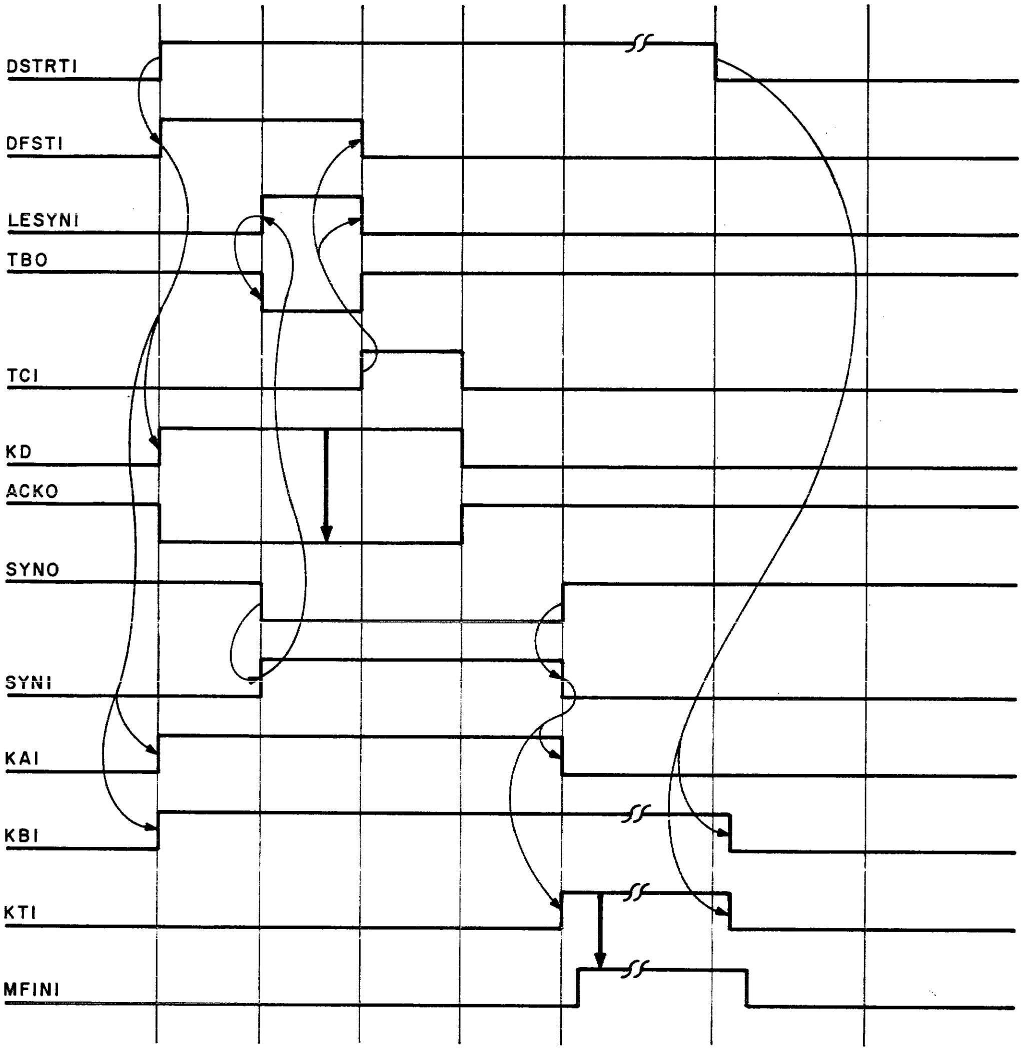


Figure 16. Multiplexor Channel Timing, ACK

The MCR clear circuit (5A3 and 5A5) provides a low active signal to any or all of the five clear leads (CM110, CM120, CM130, CM140 and CM150). When the CMCR function is decoded, both the CM0 and CMCR0 leads (5A5 and 5A3) go low to gate the high active pattern on B(11:15) to the clear lines and produce selective clearing of the monitor flip-flops. During system initialization, only CMCR0 is low (due to SCLR0A) and all five clear line go low.

The Condition Code Bus (CC Bus) is composed of five lines. When the strobe line SCC0 (5N1) is low active, the other lines (CCC1, VCC1, GCC1 and LCC1) contain a four bit Condition Code (high active). A 19-066 quad two-to-one Multiplexor (5K2) connects either DR(12:15) or MX121 with M(13:15) to a set of four bus drivers. When an SS (Status Request) function is received, the FSR0 lead (5S4) goes low to connect DR(12:15) to CX0, VX0, GX0 and LX0. At the end of the D Bus sequence, KT1 and FSR1 generate the STCC1 signal (5I5) to gate the CC MUX to the CC Bus. STCC1 also gates the bus strobe (SCC0) and the MFIN circuit (via STCC0) (5N5).

At the same time that GM1 gates the MCR to the S Bus, GM0 (5H5) generates STCC1 to gate the CC MUX to the CC Bus. However, with FSR0 now high, the CC MUX has selected the four MCR bits. The MUX outputs are ORed (19-060) (5L1) and then strobed by STCC1 to produce SIGB0 (5N1) which is returned to the CPU as MSIG0 (1H9).

On all D Bus operations except SS, FSR0 and KT1 generate a pair of signals (STA1 and STB1) (5L4) which place low levels on all five CC lines; i.e., all zero Condition Code with strobe. The false sync signal (FLSYN0) (5N5) forces only STB1 active. This produces the same result except line VCC1 is high active.

When the false sync condition occurs on input functions (RD, SS, ACK and DACK), the KT flip-flop has not been set but the S Bus gating must be completed. In the case of the status request, the false sync status byte X'04' must also be gated to S(H) or S(L) as shown on Figure 10. The auxiliary termination flip-flop (KTA) (2M1) sets on the leading edge of FLSYN0 for all input functions (FSL030A high). The S Bus gating signal (TERM1) (1A1 and 2R1) is active when either the KT or KTA flip-flop is set.

The status byte X'04' is generated by first loading the Data Register with all zeros from the idle data bus at the beginning of the operation (CLDR0) (2K4 and 5M9) and then forcing GDR130 (3L4) low to put the status byte into the S MUX. For functions other than SS, the zeroed Data Register is gated to the S Bus as per Figure 10.

Power Monitor and Initialization. The general operation of the Power Monitor circuit was described in Section 3.6.3. The following actions take place on initialization.

CPU

1. Stops clock.
2. Presets ROM State Counter to RS1.
3. Presets RIR for control module 7 and RR transfer.
4. Presets RLR so RLC is all zeros.
5. Clears Memory Control flip-flops.
6. Clears INTA, INTB, EBLINT, PWRFLD and ENFLG flip-flops.
7. Sets PVMDEN flip-flop.

ALU

1. Stops clock.
2. Clears A Counter.
3. Clears ASIGN flip-flop.
4. Sets EACNT and COMP flip-flops.

IOU

1. Kills I/O Control Delay Generator.
2. Clears the FWAIT flip-flop.
3. Clears I/O Control flip-flops.
4. Provides reset signal (SCLR0) to Multiplexor Channel Bus.

The system is initialized as a result of one of the following conditions.

1. AC input falls below minimum operating level or Memory Power Interlock opens.
2. Initialize switch on Control Console operated.
3. Key operated power switch on Console turned OFF.
4. Auxillary input EXA0 or EXB0 (6N1) goes low.

All circuits for the Power Monitor are on Sheet 6. The master reset signal SCLR0 (6A9) is active when the Initialize Relay K1 (6A5) is de-energized. During normal operating conditions, all voltages are present and the POWDN0 line (6J4) is high. This allows the delay transistor (06AQ1) (6C4) and the Darlington circuit (06AQ2/Q3) (6B4) to conduct. As long as these transistors conduct, the Initialize Relay K1 remains energized and the SCLR0 line is held high to +5 volts by a resistor (6A9).

If any of the four items listed previously occur, the STPF1 line (6L4) goes high and starts the one millisecond EPF timer (6D6). The leading edge of EPF0 (6A7) sets Bit 15 in the MCR (5D1), generating a Machine Malfunction (MMF) interrupt. In response to MMF, the user has an opportunity to do any necessary system resetting and data storage.

At the end of the one millisecond EPF delay, the trailing edge of EPF1 (6E6) toggle sets the Primary Power Fail flip-flop (PPF) (6F6) causing the PPF interrupt (6N5) to be sent to the CPU and a low active signal on CL070 (6M3). PPF1 also starts another one millisecond timer XPF (6H6). When the PPF interrupt is detected, the micro-program stores the PSW and register stack in the main memory and sends the POW function to the IOU. The Stop flip-flop (STP) (6J6) is either toggled set by the trailing edge of XPF1 or direct set by FPOW0 (6M6), whichever occurs first. When STP1 goes high, POWDN0 goes low to turn off Transistors 06AQ1, Q2 and Q3, and de-energize the Initialize Relay K1. The GSTP1 lead (6M6) is normally high. It is unused except in some multi-CPU systems.

Loss of AC or DC power also de-energizes the relay. POWDN0 goes low when the -15 volt input (N15) (6A3) to the 19-004 inverter is lost. The Darlington circuit cannot operate the relay if either the +5 volt collector supply (P5) (6B4) or the +15 volt base supply (P15) (6A3) is missing. Should the AC input (AC1 and AC3) (6A1 and 6A2) be too low or missing, the Power Fail Detector circuit operation permits Transistor 01AQ2 to conduct and remove the base drive to the Darlington circuit.

The AC input is sampled from the secondary of a 12VAC transformer and rectified with the diode bridge 02AD1, D2, D3 and D4 (6C2). The pulsating DC voltage is applied to Potentiometer 00AR1 (6E1). The potential selected by the arm of the potentiometer is applied to the Power Fail Detector via the strap A/B as shown. Strap B/C is part of the multi-CPU option to be covered later.

Transistors 01AQ3 and Q4 are connected as a differential amplifier with a +6.2 volt reference on the base of Q4 and the potentiometer signal applied to the base of Q3. The Transistors 01AQ1 and Q2 form part of their collector loads. Initially, Transistors Q1, Q2 and Q3 are off and Q4 is on. The potential at the emitters of Q3 and Q4 is approximately +7 volts (Vz + Vbe of Q4). Transistor Q2 is off with approximately +6.8 volts at the base and +6.5 volts at the emitter.

If the AC input is lost (or fluctuates enough) the potential at the base of Q3 becomes more negative, Q3 conducts and supplies base drive to Q1. The 4.7K resistor (01AR2) provides positive feedback from Q1 to Q3 causing these transistors to snap on. The emitter voltage of Q3 drops, Q4 turns off, Q2 turns on and commences to discharge the delay Capacitors 05AC1 and 06AC2 (6D4). With Q1 conducting, its collector voltage approaches ground and generates the low active signal PFDT0 (6J3). As described earlier, this forces PFDT1 high to start the sequence which puts a low level on POWDN0 and completes the capacitor discharge. The Darlington circuit has no base drive so the relay is de-energized.

The Initialize Relay K1 is a dry reed unit with Single Pole Double Throw contacts. The normally closed contact of the de-energized relay provides a metallic ground on the system Initialize Line SCLR0 (6A9).

Another delay capacitor (06BC1) (6D5) starts charging toward the high logic level when the inverter which drives it is turned off by the low SCLR0 line. The Schmidt Trigger circuit, composed of a pair of inverters and two resistors (6E5), produces the delayed SCLR0 signal, DSCLR0 (6G7), when the capacitor voltage exceeds the trigger threshold. The low level on DSCLR0 direct clears the PPF and STP flip-flops.

For a sequence due to INIT0, EXA0 or EXB0 low (6N1), clearing STP allows the POWDN0 lead to go high and the delay capacitor(s) (6D4) to charge slowly through the base resistor(s) of Transistor 06AQ1. When the threshold of the Darlington circuit is reached, the circuit conducts and the Initialize Relay K1 is energized thereby removing the ground from the SCLR0 line.

In the case where Initialize is caused by a failure to P5, N15, P15 or the AC supply, the Initialize Relay K1 de-energizes and remains in that state until the fault is corrected.

Start Timer. The Start Timer circuit is shown on Sheet 6, lower left quadrant. Section 3.6.3 covers the general operation of the circuit. With the timer-kill lead (KSTM1) (6D8) in its normally low state, the ungated STRT0 signal (6A8) enables the 35 microsecond timer STMA (6D8). When the selected module generates a MFIN0 (6A9) signal, the MFIN0B line (6C9) goes low to clear the timer and disable the timer flip-flop (STMB) (6F8).

If the MFIN signal does not occur within 35 microseconds, STMA1 goes low to toggle set the STMB flip-flop. Output STMB1 (6G8) is gated by DSTRT1, which is active on D Bus operations, to generate the FLSYN0 signal (6M7). For all other operations, DSTRT0 is high and STMB1 produces a low level on STF0 (6M7) which toggle sets Bit 11 of the MCR (5E5). Both FLSYN0 and STF0 are gated to the MFIN0 line (1G1 and 1G9) to restart the CPU clock. When the STRT0 signal is removed, STRT1 (6C8) goes low, CSTM1 (6D9) goes high and CSTM0 (6E9) direct clears the STMB flip-flop. SCLR0 (6A9) also clears the STMB flip-flop.

During initialize timing periods, the KSTM1 line (6D8) is forced high by STPF0 or PPF0A or both. When the POW function is executed, no MFIN signal is returned. The CPU waits for the initialization sequence. When the STP flip-flop is set, STP0 blocks generation of STP0 which could return an erroneous MFIN0 signal.

When the test set is in use in the single step mode, some ALU sequences require more than 35 microseconds between STRT and MFIN. The Start Timer is inhibited by a ground connected to Test Point (TP) KTM (6A8).

Miscellaneous Circuits. The Wait flip-flop (FWAIT) (1K8) controls the WAIT lamp on the Control Console. When the function LDWAIT (1K7) is decoded, the state of Bit 0 of the B Bus is loaded into FWAIT.

The MSIG0 line to the CPU (1H9) is low active whenever the I/O Control gates at least one true bit to the CC Bus; either from the CC MUX (SIGB0) (1H1) or due to the False Sync code (FLSYN0) (1G1). During a Data Channel operation, the KT1 signal gates the DCR0 line (1H1) from the Multiplexor Channel to the MSIG0 line to request a memory Read operation (see Section 3.6.3). Note the inversion between DCR0 and MSIG0.

On every I/O Control function, except FPOW0, the MFIN0 line (1G9) goes low active to restart the CPU clock. The FLSYN0 and STF0 signals also return a pseudo MFIN as described earlier. A cascaded set of OR gates (Sheet 1) is used to combine the following signals:

1. DSEND0 (1G4) - All output functions on the D Bus.
2. GC80 (1G7) - Gate pulse for FC8 (Figure 11).
3. CM0 (1H7) - Clear MCR function.
4. LDWT0 (1K7) - Load Wait function.
5. STF0 (1F1) - Start Timer Fail (non-D Bus).
6. GPX0 (1F1) - Pulse Out function.
7. FLSYN0 (1G1) - False Sync.
8. STCC0 (1G1) - CC MUX strobe.
9. STL0 (1G1) - S MUX low strobe.

Some of these signals encounter more stages of logic delay than others. This is to insure that companion signals have been gated to the busses before the MFIN0 line becomes active.

The POUT function gates Bits B12:15 to a set of board stakes (PA0, PB0, PC0 and PD0) (6N8) to be used for external signalling purposes. The pulse width is set by a timer GP (6H8) and control flip-flop (GPX) (6J8) which delay the MFIN0 signal. The width of the pulse gate POUT1 (1N9) is equal to the width of the STRT0 signal.

The strap field (6N1-6N9) provides access for 10 circuits on the IOU board to 6 terminals on the chassis front terminal strip for multi-CPU systems. The configurations of straps varies from system to system and from board to board in a given system. These inter-processor connections are not covered in this specification.

The four output pulses have been described previously. Stakes for Power Fail Master (PFM) and Power Fail Slave (PFS) are connected to the Power Fail Detect circuit (6M3). The PFM line goes low when the PFDT0 signal goes low. A decoupling diode and pullup resistor are provided. An IOU board used in the slave mode is equipped with a B/C strap (6H2) - the A/B strap is removed. This disconnects the analog supply (6C2) and provides an off bias potential for Transistor 01AQ3 by means of Resistor 00CR5 to P15 and Diodes 00AD1 and D2 to the reference Zener diode 02AD5. When the PFS line (connected to the PFM on another board or its equivalent) goes low, the slave circuit Transistors Q1 and Q3 snap on as described in Section 3.7.3. The transistors are off for the high or open condition on the PFS line.

Auxiliary initialize inputs EXA0 and EXB0 (6M2) start the initialize sequence when either input is low. The diodes in the base circuit of Transistor 00EQ1 provide a threshold such that the low PFM line from another IOU board is recognized. A low signal from a logic gate or switch contact to ground may also be used. The RC noise filter (6C1) for the POFF0 and INIT0 lines is also active for the auxiliary inputs. Note that the decoupling diode on the PFM line permits several such lines to be connected to the same auxiliary input in an OR configuration.

The gated stop input (GSTP1) (6N6) on the memory controlling (or master) CPU may be controlled by the OR tie of the STP1A (6N6) signals from all other CPU's. This delays the low active signal on the POWDN0 line of the master CPU until the rest of the system has finished its initialize/storage micro sequences.

Power sequencing may be varied by changing either the delay capacitor(s) (6E4) or resistor(s) (6D4) on various sub-system IOU boards.

4. DISPLAY SYSTEM

The Display System provides a means for reading the contents of all the system registers and any main memory location, together with the capability of manually entering data and programs. Figure 17 shows the Control Console layout. Two register displays are available. There are 16 switches which provide a means for entering memory data and addresses into the machine. The momentary EXEcute control switch requests that any operation, selected by the 12 position rotary Function switch and the SGL and RUN function switches, be executed. The Initialize (INT) control switch resets the system and peripherals. The LOCK-ON-OFF key operated security lock switch, controls power to the system and permits locking the controls. The Control Console is an input/output device interfaced with the Multiplexor Bus. The Display System is supported by a special micro-program sequence in the Read-Only-Memory. The Control Console operating procedures may be found in the Model 70 User's Manual, Publication Number 29-261.

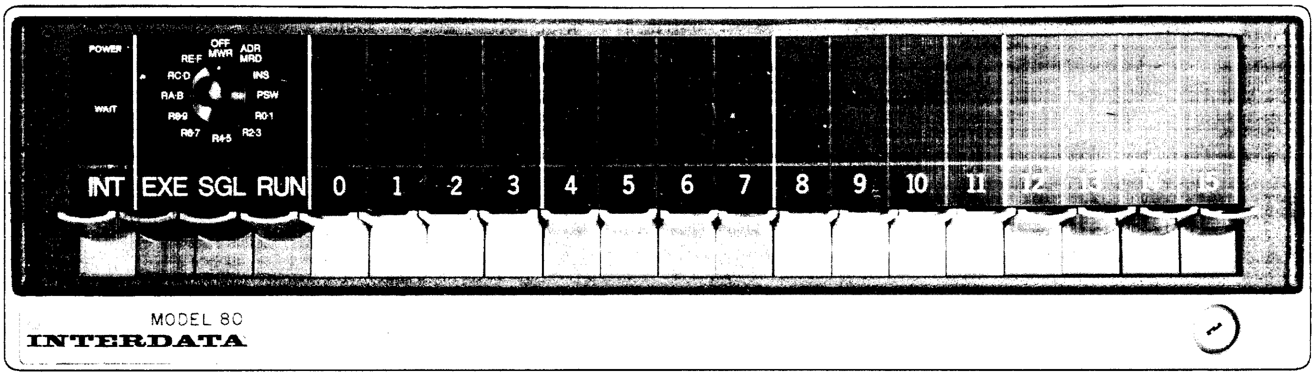


Figure 17. Control Console

4.1 Block Diagram Analysis

Refer to the block diagram on Figure 18. The Processor Multiplexor Bus with drivers and receivers is shown on the left, the Display System device controller is shown in the center, and the Control Console is shown on the right side.

The address logic is shown in the upper left area of the block diagram. On receiving a request for service via the EXEcute switch and the CATN signal, the Processor outputs the eight bit display address (X'01') on Data Lines D08:15. This is followed by the ADRS control line which causes the decoded address to be strobed into the Address Storage flip-flop. The one output from this flip-flop enables all other I/O commands into the display controller logic.

Data to the Control Console is transmitted one byte at a time. The first byte is output on Data Lines D08:15, and the Data Available (DA) control line is activated. This command causes the first byte of data to be strobed into Bits 8 through 15 of Display Register Two. The DA line is then terminated, and the two-stage byte counter is incremented. The second byte of data is then placed on Data Lines D08:15, and the DA activated again. This process is repeated four times. Each time the display is addressed, the byte counter is automatically reset to zero for the first byte of data.

Data from the Input Register data switches is read into the system one byte at a time via Data Lines D08:15. On activating the Data Request (DR) control line, Bits 8 through 15 of the data switches are read into the system. The DR command is then terminated and the one-stage byte counter is toggled, enabling the second byte of data. The DR control line is again activated and Bits 0 through 7 of the data switches are read. The one-stage byte counter is automatically reset when the display is addressed.

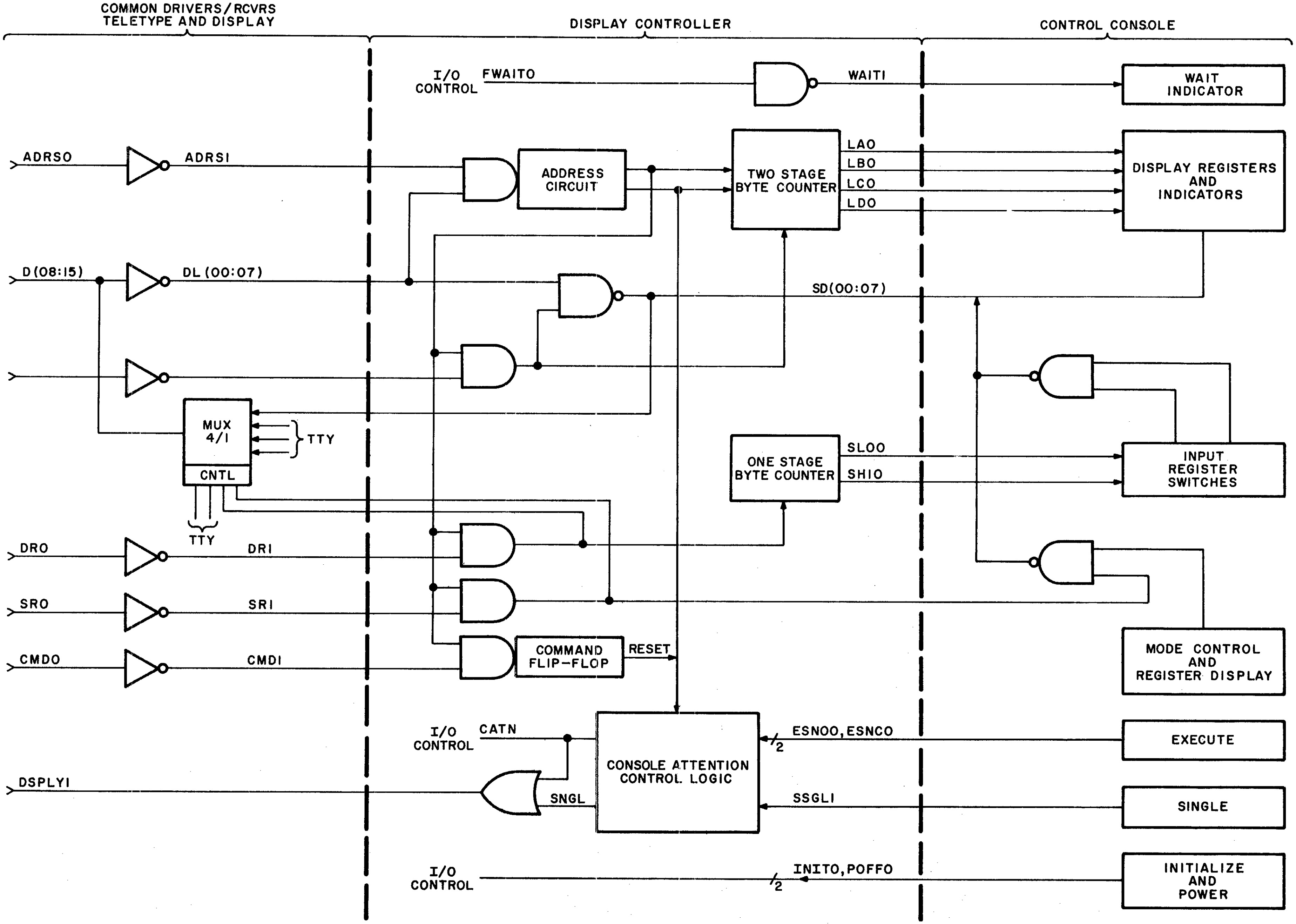

COMMON DRIVERS/RCVRS
TELETYPE AND DISPLAY
DISPLAY CONTROLLER
CONTROL CONSOLE
I/O CONTROL
FWAITO
WAITI
WAIT INDICATOR
ADRSO
ADRSI
ADDRESS CIRCUIT
TWO STAGE BYTE COUNTER
LAO
LBO
LCO
LDO
DISPLAY REGISTERS AND INDICATORS
D(08:15)
DL(00:07)
SD(00:07)
MUX 4/1
CNTL
TTY
TTY
ONE STAGE BYTE COUNTER
SLOO
SHIO
INPUT REGISTER SWITCHES
DRO
DRI
SRO
SRI
CMDO
CMDI
COMMAND FLIP-FLOP
RESET
MODE CONTROL AND REGISTER DISPLAY
I/O CONTROL
CATN
CONSOLE ATTENTION CONTROL LOGIC
ESNOO, ESNCO
2
EXECUTE
DSPLYI
SNGL
SSGLI
SINGLE
I/O CONTROL
INITO, POFFO
2
INITIALIZE AND POWER

Figure 18. Display Controller Block Diagram

The status of the control and register switches is read into the system as a single byte of encoded data by activating the Status Request (SR) control line. The twelve positions of the register display rotary Function switch are encoded into Bits 4:7 of the status byte and the control switches are encoded into Bits 0:7. The status byte is read into the system on Data Lines D08:15. The 32 register display lamps and the 16 data switches may be I/O programmed by the user. An Output Command (OC) instruction causes the CMD control line to set a flip-flop that disables the byte counters from being reset when the device is addressed.

The control logic is shown on the bottom of the block diagram. Depressing the EXEcute switch sets the CATN flip-flop in the console attention control logic. This generates a DSPLY1 interrupt to the Processor and appears as Bit 10 of the Machine Control Register (CATN). When the Processor addresses the display, the CATN flip-flop is cleared.

The Single switch (SGL) controls another flip-flop (SNGL) which is loaded when the EXEcute switch is depressed. This also generates a DSPLY1 interrupt which remains active after the CATN flip-flop is cleared. A user instruction is executed each time the EXEcute switch is depressed.

The Initialize (INT) switch starts the initialize sequence to reset the Processor, the Display Controller and all I/O devices. The WAIT indicator is under direct control of the FWAIT flip-flop in the I/O Control circuit.

The following schematic references pertain to the combined TTY/Display controller shown on Sheets 7, 8 and 9 of IOU Functional Schematic 35-405D08, and to the Control Console/Display Panel Functional Schematic 09-051D08.

4.2 Addressing Logic

The Control Console device address is wired as (X'01'). D Bus lines D08:15 are buffered and inverted by the common receiver circuits (7A1-7A5) to create the double rail data lines (DL 00:07). The decoded Display address gives active levels on B0 and B1 (7J7). The Display address flip-flop (ADB) (7K7) toggle sets on the trailing edge of the ADRS1 (7H8) signal. The ASYNB0 line (7K8) goes low to generate the return SYN0 signal (7K9). It also clears the CATN flip-flop (8D3).

If the INCR flip-flop (8B2) is reset, the function ADRS1•B1•INCR0 forces RST0 (8F2) low to reset the two-stage byte counter (8C8) and the one-stage byte counter (8C6).

4.3 Data Output

The byte of data transferred between the Display controller and the Control Console makes use of eight bi-directional shared lines (SD 00:07) as shown on the block diagram Figure 18 and at locations 7H1-7H5. Data is placed on this SD Bus when the DAGB1B line (7F8) goes high and is gated to one of the four display registers in the Control Console by one of the four load signals; LA0, LB0, LC0 or LD0 (8E8).

The load signals are selected by decoding the four states of the two-stage counter, XA and XB (8C8), and strobing with the LX1 signal (8D9). To provide proper loading of the display registers with gated data, the common strobe (LX1) is started by DAGB1A (8C9) but terminated after approximately 200 nanoseconds by the delay circuit; inverters 04E and Capacitors 04EC5 and C6 (8B9). The return SYN is generated by DAGB0 (7B7). The trailing edge of DAGB1A increments the counter.

The counter is reset by the RST0 line as described earlier on addressing. The RST0 line also goes low for either SCLR0B (8A2) or on the Output Command (OC) which sets the INCR flip-flop (7B1) (see 09-051D08, Sheet 1).

4.4 Data Input

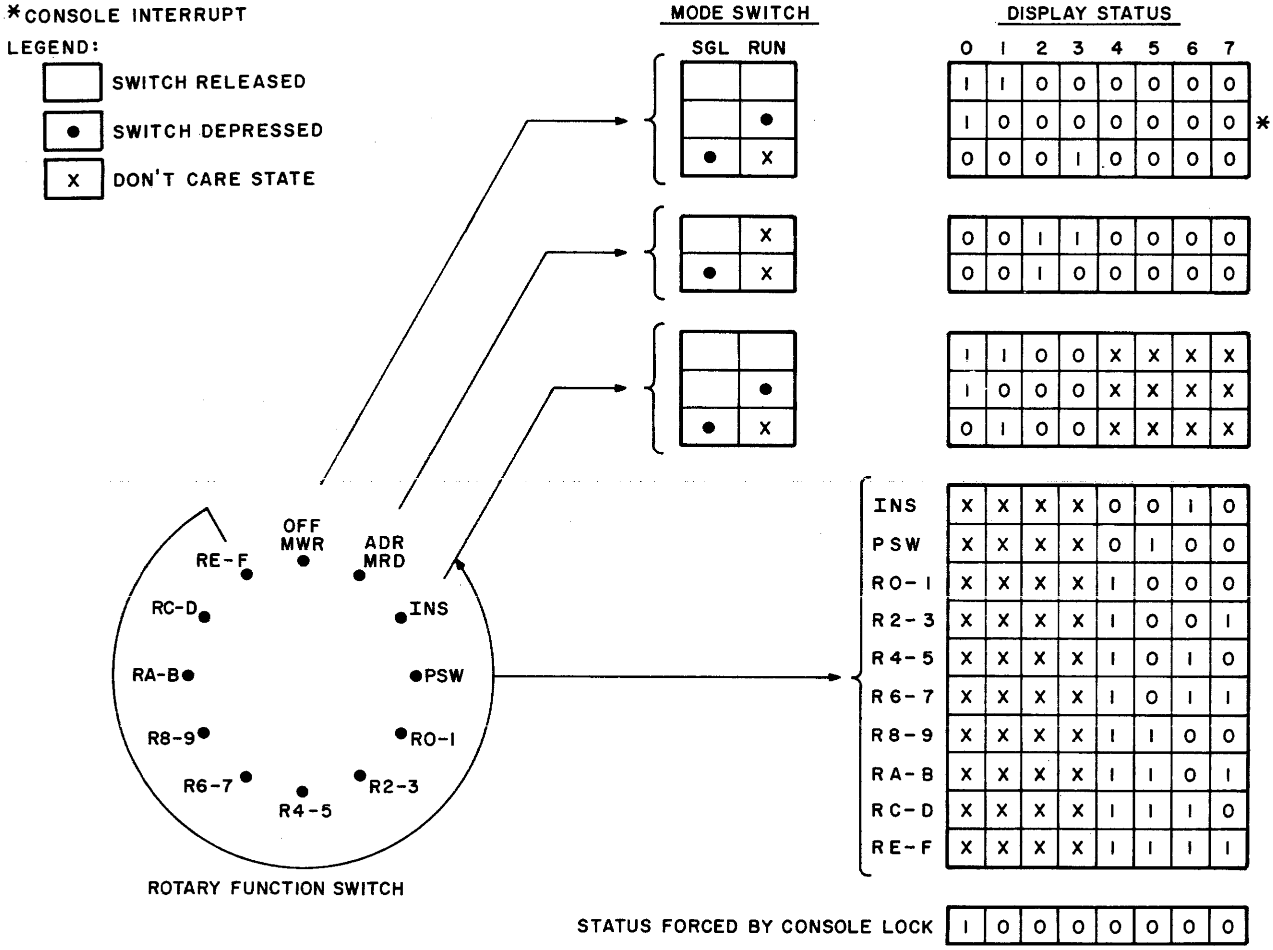
The one-stage byte counter XC (8C6) is cleared by the RST0 signal in the same manner as XA and XB. When the Data Request control line (DRGB1) is active, the least significant Byte Enable (SL00) (8E6) is active and Bits 00:15 of the Console data switches are gated to the SD Bus. The XC flip-flop toggles set on the trailing edge of DRGB1. The next time DRGB1 goes high, Bits 00:07 of the data switches are gated to the SD Bus by SH10 (8E6) in the active state. DRGB0 (8A6) generates MST0 which gates the SD Bus through the 19-038 four-to-one Multiplexors onto Bits 08:15 of the D Bus (7K1-7K5). The D MUX select lines (DMA1 and DMB1) (7H5) are both low when the Display controller is in use. The return SYN is generated by a delayed DRGB0 (DSPSYN0) (7G8) to allow for MUX and Console gating delays.

4.5 Status Input

The status byte encoding is shown on Sheet 2 of 09-051D08. The register display rotary Function switch is encoded into the least significant four bits of the status byte. The control switches, SGL and RUN, in conjunction with the first two positions of the rotary Function switch, OFF/MWR and ADR/MRD, from the most significant four bits of the status byte. The status byte is gated onto SD Bus by the SRG0 lead (7D6). SRGB0 (7D7) generates MST0 to gate SD 00:07 through the MUX's to the D Bus. The return SYN is generated by a delayed SRGB0 (DPSPYN0) (7G8) to allow for MUX and console gating delays.

The table below lists the status codes for the rotary Function switch positions.

TABLE 10. DISPLAY STATUS BYTE ENCODING



*CONSOLE INTERRUPT

LEGEND:

☐ SWITCH RELEASED

● SWITCH DEPRESSED

X DON'T CARE STATE

	MODE SWITCH		DISPLAY STATUS								
	SGL	RUN	0	1	2	3	4	5	6	7	
OFF MWR	☐	☐	1	1	0	0	0	0	0	0	
	☐	●	1	0	0	0	0	0	0	0	*
	●	X	0	0	0	1	0	0	0	0	
ADR MRD	☐	X	0	0	1	1	0	0	0	0	
	●	X	0	0	1	0	0	0	0	0	
INS … RE-F	☐	☐	1	1	0	0	X	X	X	X	
	☐	●	1	0	0	0	X	X	X	X	
	●	X	0	1	0	0	X	X	X	X	
INS			X	X	X	X	0	0	1	0	
PSW			X	X	X	X	0	1	0	0	
RO-I			X	X	X	X	1	0	0	0	
R2-3			X	X	X	X	1	0	0	1	
R4-5			X	X	X	X	1	0	1	0	
R6-7			X	X	X	X	1	0	1	1	
R8-9			X	X	X	X	1	1	0	0	
RA-B			X	X	X	X	1	1	0	1	
RC-D			X	X	X	X	1	1	1	0	
RE-F			X	X	X	X	1	1	1	1	
STATUS FORCED BY CONSOLE LOCK			1	0	0	0	0	0	0	0	

4.6 Control Logic

Outputs of the EXEcute switch (ESN00 and ESNC0) are fed to a deglitching circuit (8B4) composed of an RS flip-flop. A positive pulse (PEX1) (8C4) is generated when the EXEcute switch is depressed and released. The CATN flip-flop (8D3) toggles set on the trailing edge of PEX1. This flip-flop is reset either by ASYNB0, when the Processor addresses the Display controller, or by the initialize signal SCLR0B (8A2). The diode (5AD3) protects against a sneak path in the Console circuit during the Power-Lock mode.

When the rotary Function switch is in a position other than OFF/MWR or ADR/MRD, the SSGL1 lead represents the state of the SGL Control switch. On the trailing edge of the EX1 pulse, the logic state of the SSGL1 lead (8A5) is gated into the SNGL flip-flop (8C5). This flip-flop is direct cleared by the SCLR0B signal.

The Display controller interrupt (DSPLY1) (8E5) is active when either the CATN or the SNGL flip-flop is set. The CATN1 level (8E3) is gated to Bit 10 of the S Bus on the sense MCR function code of the I/O Control circuit.

5. TELETYPE CONTROLLER

The built-in Teletype (TTY) device controller interfaces an ASR/KSR 33 or 35 TTY to the Processor. It provides the serial/parallel conversion required for data transfer between the parallel D Bus and the serial, eight level, start/stop ASCII code signal used by the TTY (see Figure 19).

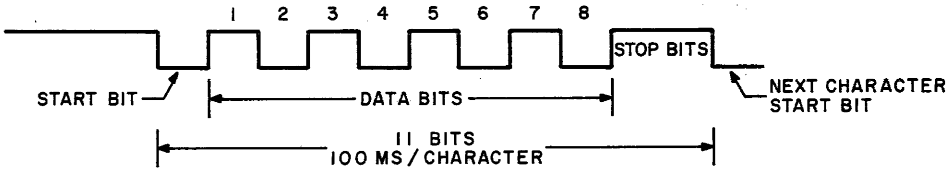


Figure 19. Serial ASCII Code U (Even Parity)

The TTY controller is shown on Sheets 7, 8 and 9 of IOU Functional Schematic 35-405D08.

5.1 Block Diagram Analysis

Figure 20 is a block diagram of the TTY controller. The data line receivers, control line receivers and data send multiplexors are shared with the Display controller. The control circuits consist of the Command flip-flops (read or write, etc.) which direct the flow of information, circuits to control ATN/ACK functions, and logic to generate the status bits and control the timer.

The serial information received from the TTY is sampled by the timer and strobed into the Shift Register. When all the data has been shifted in, the data in the Shift Register is transferred to the Buffer Register. It is then gated through the four-to-one MUX onto the D Bus, D(08:15), by the Data Request signal (DRG). A bit-by-bit copy of the received data may also be sent to the TTY printer/tape punch when the Block flip-flop (BLK) (7N8) is cleared. In the Write or (Send) mode, the data byte is placed directly (parallel) into the Shift Register and then shifted out (serially) to the TTY.

5.2 Bus Communications and Address Circuits

Communications between the Processor and the TTY controller is via the control lines, test lines, and the low order eight bits of the D Bus. The bus receivers (Sheet 7), bus drivers (7M2-7M5) and send MUX (7J2-7J5) are shared with the Display controller. The Data Lines D08:15 are buffered to form the DL(00:07) lines. When the wired address X'02' is detected, Lines A0 and A1 are active and the TTY address flip-flop (ADA) (7K7) is toggled set on the trailing edge of the ADRS1 signal (7K9)* This enables the other control lines for the TTY controller. While the ADRS1 signal is active, the ASYNA0 line goes low and generates the return SYN0 signal (7K9).

The send MUX consists of four 19-038 circuits (dual four-to-one multiplexors) which have the Display lines SD(00:07), the TTY status, TTY data, and TTY ACK address connected to corresponding sets of inputs. The select lines DMA1 and DMB1 (7H5) are generated as follows:

	DMA	DMB	
C0	0	0	Display Data Request or Status Request
C1	1	0	TTY Status Request
C2	0	1	TTY Data Request
C3	1	1	TTY Interrupt Acknowledge

Multiplexor inputs C3 are wired to high or low levels to create the TTY address X'02'* Unused status bits are wired low. The multiplexor strobe (MST0) (7H6) is low active when any of the five input signals are low; i.e., SRGB0, DRGB0, SRGA0, DRGA0, or ATSYN0. The first two are combined and delayed for DSDSYN0 while the other three form TSYN0.

*NOTE: For systems where X'02' has been assigned to another device, the TTY Controller may be strapped for X'82'. (See Sheet 7 of Schematics.)

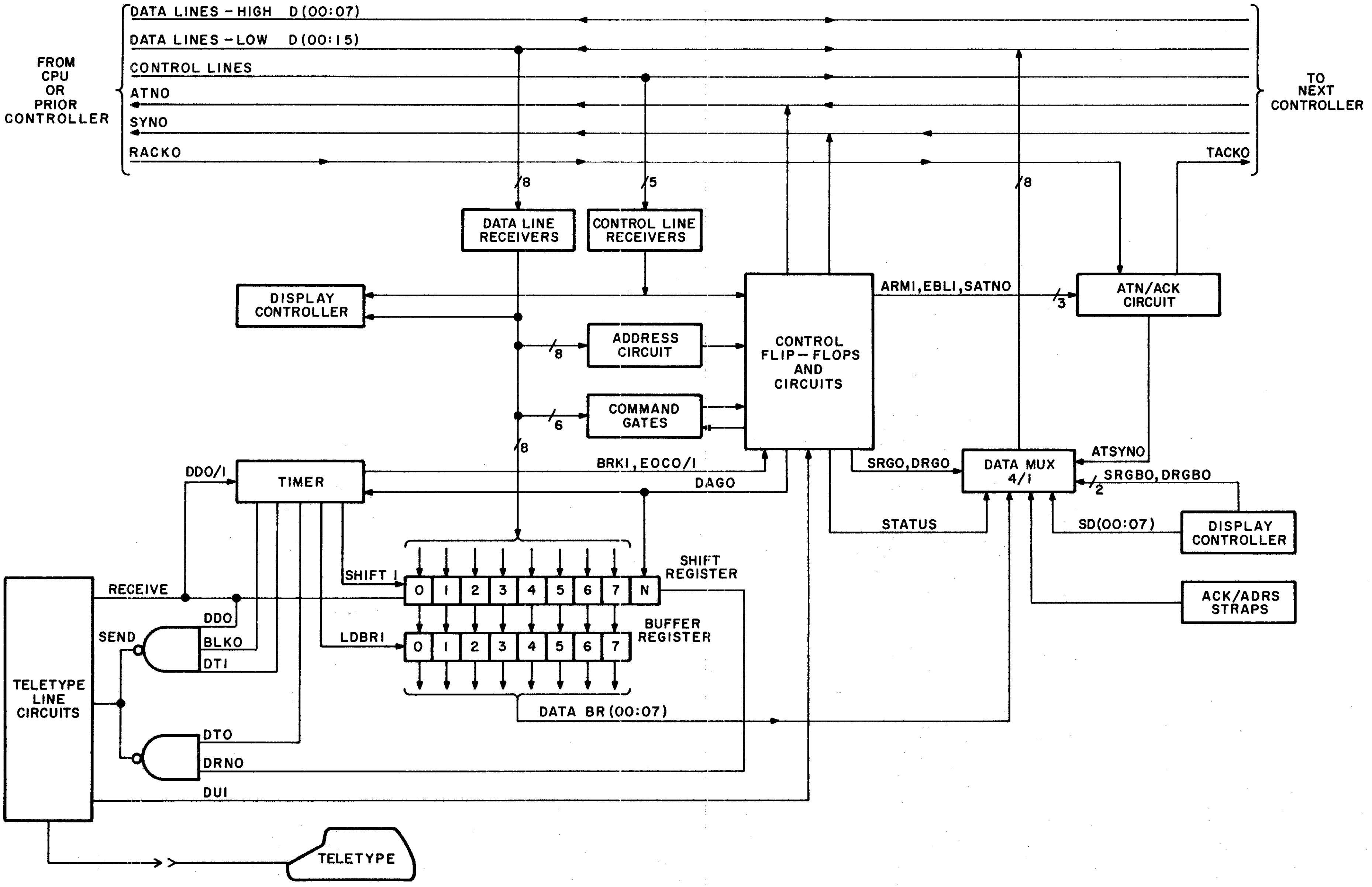

FROM CPU OR PRIOR CONTROLLER
DATA LINES - HIGH D(00:07)
DATA LINES - LOW D(00:15)
CONTROL LINES
ATNO
SYNO
RACKO
TO NEXT CONTROLLER
TACKO
8
5
8
DATA LINE RECEIVERS
CONTROL LINE RECEIVERS
DISPLAY CONTROLLER
ADDRESS CIRCUIT
8
COMMAND GATES
6
8
CONTROL FLIP-FLOPS AND CIRCUITS
ARMI, EBLI, SATNO
3
ATN/ACK CIRCUIT
ATSYNO
DATA MUX 4/1
SRGO, DRGO
SRGBO, DRGBO
2
STATUS
SD(00:07)
DISPLAY CONTROLLER
ACK/ADRS STRAPS
DDO/I
TIMER
BRKI, EOCO/I
DAGO
SHIFT I
SHIFT REGISTER
0 1 2 3 4 5 6 7 N
RECEIVE
DDO
SEND
BLKO
DTI
LDBRI
BUFFER REGISTER
0 1 2 3 4 5 6 7
DATA BR (00:07)
TELETYPE LINE CIRCUITS
DTO
DRNO
DUI
TELETYPE

Figure 20. Teletype Controller Block Diagram

5.3 Status and Commands

The bit assignments for TTY status and command bytes is shown in the following table.

TABLE 11. TELETYPE STATUS AND COMMAND BYTE

BIT NUMBER	0	1	2	3	4	5	6	7
STATUS BYTE	ERR	*	BRK	*	BSY	EX	*	DU
COMMAND BYTE	DISABLE	ENABLE	UNBLOCK	BLOCK	WRITE	READ		

*Unassigned status (will return zero).

STATUS BYTE

ERR	The Error bit is set when a character is not taken from the controller buffer before another character is assembled.
BRK	The Break bit is set at the end of one character time when the line is held in the space condition for a period greater than a character period.
BSY	Read Mode. The Busy bit is normally set and is reset when data is available for transfer to the Processor. Write Mode. The Busy bit is normally reset and is set when data is being transferred to the terminal.
EX	The Examine bit is set when BRK or ERR is set.
DU	The Device Unavailable bit is set when the terminal is powered down or in Local Mode.

COMMAND BYTE

DISABLE	Disables device interrupts; allows queuing of interrupts.
ENABLE	Enables device interrupts. Note that a command byte with both Bits 0 and 1 set Disarms the interface, no interrupt queuing.
UNBLOCK	Allows the Printer to print data entered via the keyboard or tape reader.
BLOCK	Disables the Unblock feature.
WRITE	The interface is placed in the Write Mode.
READ	The interface is placed in the Read Mode.

The command flip-flops EBL, ARM, BLK and WT (7N6-7N9) are loaded with the trailing edge of the CMGA1 signal (7L9) if the J or K input is high. The contents of the flip-flops remain unchanged if both the J and K inputs are low. The Write Storage flip-flop (WT) (7N9) unconditionally accepts the Read/Write signal from the Processor, however, the Write Execution flip-flop (WRT) (8J6) can only be updated when the timer has stopped; i.e., when TMG0 (8G5) is high.

The EBL and ARM flip-flops (7R6) are loaded from DL00 and DL01 as described in Table 10. They control the action of the interrupt flip-flop (ATN) (8N8) and the interrupt line ATN000 (8N7).

The Block flip-flop (BLK) (7N8) controls the serial feedback of data from the TTY receiver to the TTY driver. When reading a non-ASCII tape, it is inconvenient and undesirable to permit the received data to reach the printer/stunt box and operate the bell, line feed, form feed, etc., functions. This feedback is broken when the BLK flip-flop is set. Sending data to the TTY from the Shift Register is not affected by the BLK flip-flop.

The Busy (BSY) status bit is controlled by the Write Execution flip-flop not the WT flip-flop. The Break bit remains set as long as the Break key is depressed at the TTY. The Error bit (overflow) is cleared by either a Data Request, any command, or the system initialize signal SCLR0.

5.4 Timer Circuits

The timer consists of the control flip-flop (TMG) (8J3), a 440 HZ multivibrator MTA (8L3) and MTB (8N2), a two-stage clock counter MTC (8L3) and MTD (8L3), and a character counter (TA, TB, TC and TD) (8L5). In the idle or reset state with the TMG flip-flop cleared, TMG1 (8J6) is low to disable MTA and MTB, to clear MTC and MTD and to preset the character counter to the count of five.

When the TMG flip-flop is toggled set at the end of DAGA0 (8G2) in the write mode; TMG1, TMG1A and DTMG1 all go high to enable the timer. The 440Hz pulse train (MTB1) (8M3) drives the two-stage counter (MTC and MTD) and a decoder gate to generate the 110Hz train of clock pulses (CLK0 and CLK1) (8M4) and the shift pulses (SHFT1) (8R4). After the end of the ninth clock pulse, TB1, TC1 and TD1 are all high, thus forcing FSTP0 (8N5) low to terminate the train of shift pulses. During the eleventh clock pulse, EOC0 (8M4) goes low, TTMG1 (8H3) goes high and the TMG flip-flop is toggled clear on its trailing edge. This produces a train of eleven clock pulses and nine shift pulses having a period of 9.09 milliseconds (110Hz) with the trailing edge of the first pulse occuring 9.09 milliseconds (one bit period) after TMG is set. The pulse width is about 1.15 milliseconds (one-eighth of a bit period).

The idle timer is also started (by the direct set pulse ST0 (8J2)) when the received Start bit arrives from the keyboard or tape reader or due to depression of the Break key. This is not dependent on the read/write mode since the BRK condition must be detected in both modes. The width of the ST0 pulse is determined by delay Capacitor 02HC1 (8G1) which generates the delayed TMG0 signal DTMG0 (8H2). Since the MTD flip-flop is direct set by ST0, the first CLK1/SHFT1 pulse occurs 4.545 milliseconds (half of a bit period) after the TMG flip-flop is set; the period of the pulses is still 9.09 milliseconds. Received data is sampled/shifted at the center of each bit. The TMG flip-flop is toggled clear at the end of the EOC and TTMG pulses as before.

5.5 Data Output

The TTY controller is in the write mode when both the WT and WRT flip-flops are set. To send data to the TTY, the DAGA0 line (9B1) goes low to load DL(00:07) into the Shift Register, clears the Start bit flip-flop (DRN) (9G5) and toggles set the Timing Gate flip-flop (TMG) (8J3). Note that if the timer was already running when the Data Available control signal is received, the DAGA0 signal (7D9) would be blocked by TMG0 (7C9) low, no return SYN would be generated, and the false sync condition would be detected after 35 microseconds. For this reason the WDH instruction must not be used with the TTY controller.

When the timer starts, shift/clock pulses are generated as described earlier and shown on Figure 21. The bit stored in the DRN flip-flop is connected to the transmit line (TNSB1) (9K6) by the high states on the device transmitting (DT0) and the TMG1 lines. Since the DRN flip-flop is initially cleared by DAGA0, TNSB1 goes low, and the gate driving TNS0 turns off to send the open-loop Start bit condition. At the end of each shift pulse, as the eight data bits are sequentially transferred into the DRN flip-flop, a high state at the serial input of the Shift Register (DX1) (9C2) gradually loads the register with all ones (including the DRN flip-flop). During the last two clock periods, after shifting has stopped, the one stored in the DRN flip-flop is sent out as the closed-loop Stop bit condition. The EOC pulse clears the TMG flip-flop to generate the closed-loop Idle condition.

With the WRT flip-flop set, the status bit BSY1 (8J7) is active when TMG1 is active. Should a command which clears the WT flip-flop (read mode) be received while the timer is running, the WRT flip-flop (and the definition of BSY status) does not change until the TMG flip-flop is cleared and TMG0 (8F8) gates WT1 into the WRT flip-flop.

5.6 Data Input

The timer circuit can be started from the TTY receive loop in either the read or write mode as described in Section 5.4. This insures that the Break condition will always be detected. However, serial data cannot enter the Shift Register (DX1) (9C2) unless the TTY controller is in the read mode; i.e., the WRT flip-flop cleared and WRT0 high. The Load Buffer Register pulses (LDBR1) (9D5) are generated only in the read mode.

The Device Data line (DD1) (9R5) is high active when there is current flowing in the receive loop. This represents the logic ONE level and also the idle loop condition. The signal from the receive loop is filtered by an RC network (180 ohms/ 2.2mfd) (9J9) and then reshaped by the Schmidt Trigger circuit (composed of a pair of inverters and two resistors) (9G9-9K9) to generate the DD0 and DD1 signals.

When DD0 and DD1 first become active, the timer is started by the ST0 pulse (as described in Section 5.4) and the Device Transmitting flip-flop (DT) (9F7) is set. This flip-flop forces the TNSB1 line high and partially selects the TNSA1 gate, subject to a high level on the BLK0 and DD0 lines; i.e., the serial feedback circuit to the TTY Printer/Punch. The DT flip-flop also arms the Line Check flip-flop (XLC) (9G7) by placing a high level on the J input.

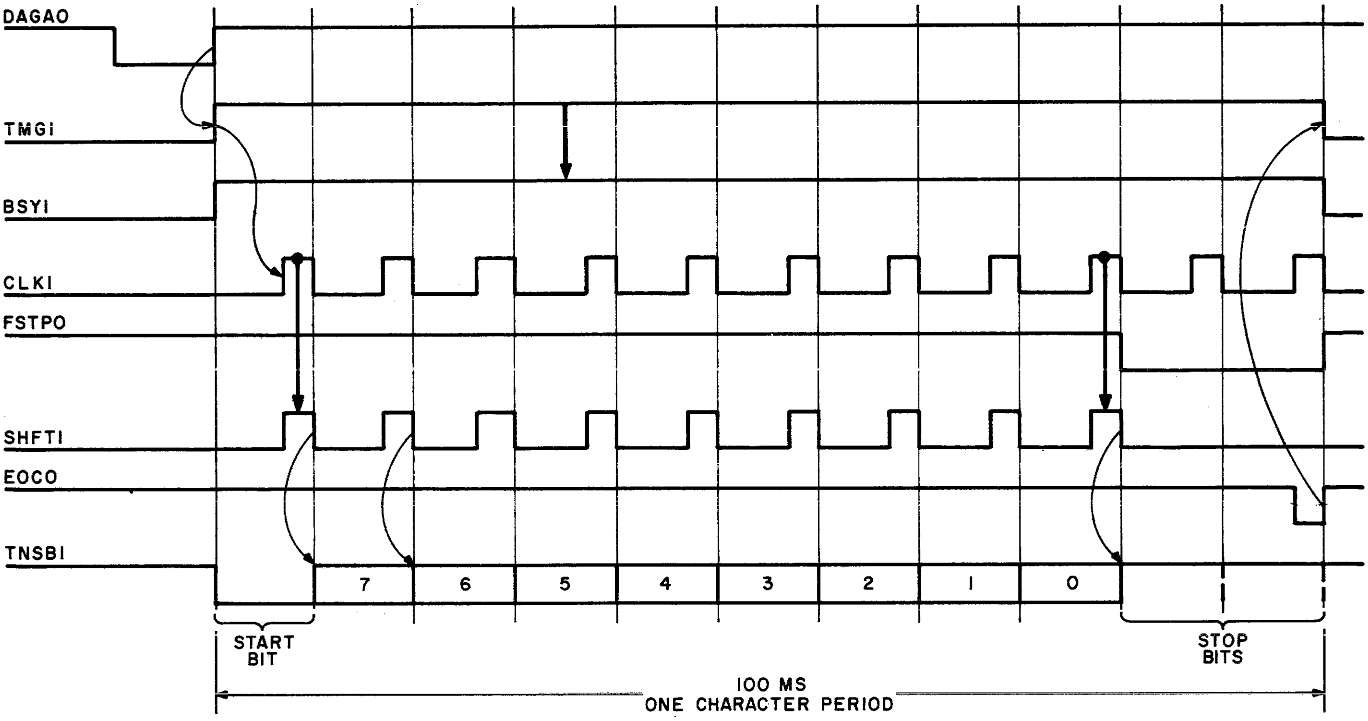
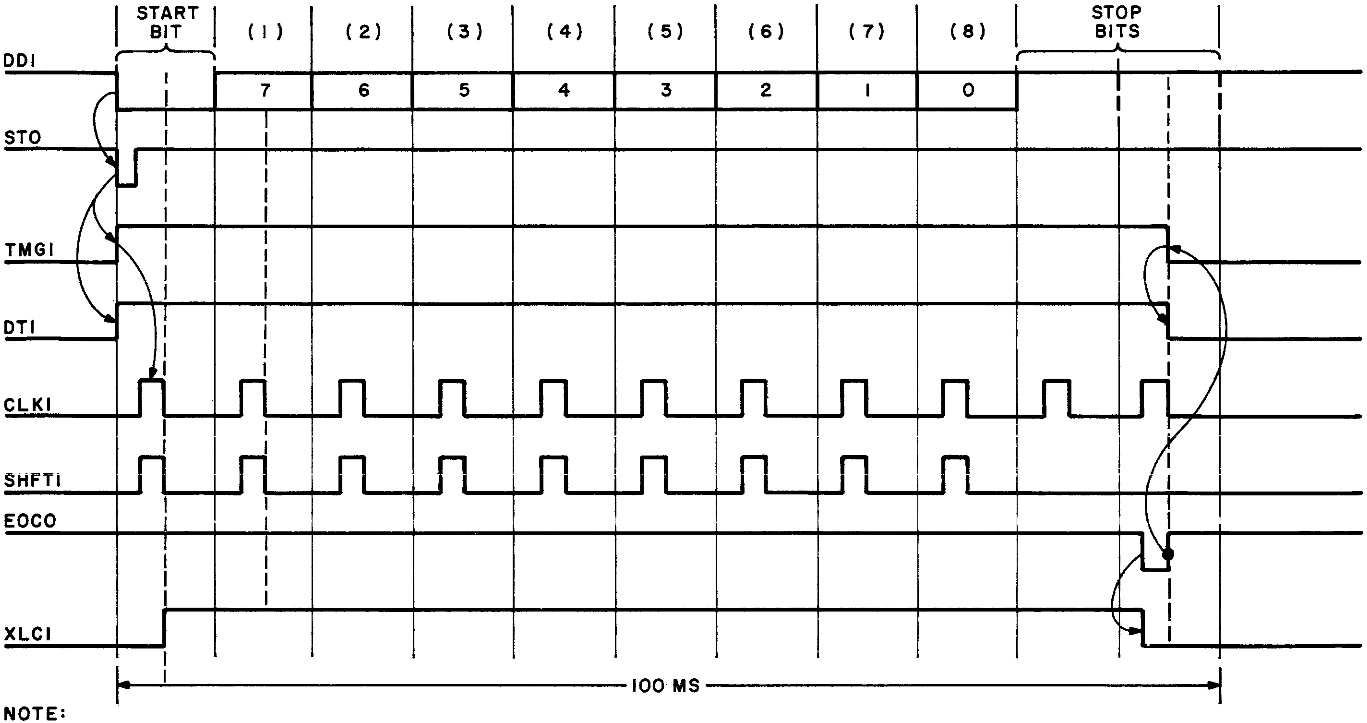

DAGAO
TMGI
BSYI
CLKI
FSTPO
SHFTI
EOCO
TNSBI
7
6
5
4
3
2
1
0
START BIT
STOP BITS
100 MS
ONE CHARACTER PERIOD

Figure 21. Write Mode (Output) Timing, Teletype

As seen on Figure 22, the XLC flip-flop is toggled set at the end of the first SHFT pulse. During the first SHFT pulse, the receive loop is checked to insure that the loop is still open; i.e., a legitimate Start bit has started the timer. If the loop is closed, DD1 is high and the Start Glitch pulse (GLTCH0) (8H3) is generated to clear the TMG flip-flop at the end of the SHFT pulse. The timer is reset, there are no EOC or LDBR pulses, the Buffer Active flip-flop (BA) (9C7) and the BSY status are unchanged.

The serial data at the Shift Register input (DX1) (9C2) is active when the DD1 line is active. The nine SHFT1 pulses move the received data into and along the Shift Register until the Start bit and the eight data bits occupy DRN and SR(00:07). Shifting occurs at the end of each SHFT1 pulse; i.e., the center of each bit.


START BIT
(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)
STOP BITS
DDI
7
6
5
4
3
2
1
0
STO
TMGI
DTI
CLKI
SHFTI
EOCO
XLCI
100 MS

NOTE:
BIT DESIGNATIONS (X) ARE PAPER TAPE CHANNEL NUMBERS.

Figure 22. Read Mode (Input) Timing, Teletype

The TMG flip-flop toggles clear at the end of the EOC pulse and clears the DT flip-flop. The XLC flip-flop is cleared by EOC if the loop is closed due to a Stop bit, DD1 high (9G8). In the case of a missing Stop bit (or Break condition), the XLC flip-flop remains set after the EOC pulse has cleared the TMG flip-flop. The function TMG0·XLC1 causes BRK0 (8H8) to go low. Lines BRK1, EX1 and EX0 will then become active. The timer cannot restart on the open loop condition since ST0=DTMG0·DD0·XLC0.

The BRK condition continues until the receive loop is closed. The DD1·TMG0 function then clears the XLC flip-flop.

In the read mode, BSY1 (8J7) is low whenever the Buffer Active flip-flop (BA) (9C7) is set. The EOC1 pulse generates the LDBR1 pulse to load the Buffer Register and toggle set the BA flip-flop. The DRGA0 signal (9B5) clears the BA flip-flop when the buffer is gated to the D Bus. An overflow or error state exists if the LDBR1 pulse finds the BA flip-flop still set, the Overflow flip-flop (OV) (9D5) is then set. The OV and BA flip-flops are cleared by the DRG pulse, any CMG pulse, or the initialize signal SCLR0B.

5.7 Interrupt Circuit

The TTY controller generates an interrupt for a negative transition on BSY1. This transition toggle sets the ATNA (8J8) flip-flop which in turn direct sets the ATN flip-flop (8N8) via the SATN0 lead. This forces GATN1 high and ATN000 (8N7) low.

The Processor responds by executing an Acknowledge Interrupt (AI). When the TTY controller has first priority, the RACK0 lead (8K6) goes low forcing RACK1 and DRACK1 high. With GATN1 high, the TACK0 gate is blocked and the ATSYN0 line goes low. This gates the controller address X'02' to the D Bus, generates the return SYN0, direct clears the ATNA flip-flop, and toggle clears the ATN flip-flop at the end of ATSYN0.

When the system uses the Memory Protect and/or the Real Time Clock controllers, the RACK0/TACK0 daisy chain is wired to the higher priority controller(s) before it reaches the TTY over the back panel.

As noted in Section 5.3, the Disable command clears the EBL flip-flop forcing the EBL1 (8K8) and GATN1 lines low. Interrupts may be queued by setting the ATN flip-flop. The Disarm command forces the ARM1 lead (8S9) low to clear the ATN flip-flops and hold them clear; interrupts are not queued.

NOTE

The ATNB flip-flop has been disabled to make the Model 80 compatible with other INTERDATA systems.

5.8 Initialization

The system initialize signal SCLR0B (7L8) conditions the TTY controller by setting the BLK flip-flop and clearing all other control flip-flops. This presets the controller in the read mode with interrupts disarmed.

6. MAINTENANCE

6.1 CPU Clock Timing (Functional Schematic 35-403D08)

The basic clock of the CPU is generated via an oscillator whose frequency is determined by a tapped delay line. This is factory adjusted for a nominal 10 MHz frequency with a 40% duty cycle and normally needs no adjustment.

The basic repetition rate is determined by 2 (5ns+5ns/TAP) where the signal TREP0 (1F1) is connected to the delay line tap required to produce the desired delay. The normal setting is therefore Tap 9 (Pin 21A-11 to produce 2 (5ns+45ns)= 100ns basic repetition rate.

The clock width is determined by the setting of TWDTH0 (1N2) on the delay line and is directly related to the delay produced by the delay line tap. Thus, a nominal 40 nanosecond clock width is produced by connecting TWDTH0 to Tap 8 (Pin 21A-06). No connection to this input results in a 50% duty cycle.

The RIR clock (RIRSTB1) (1N1) is adjusted to a nominal 20 nanosecond strobe by the positioning of TWDTHA0 on the delay line. This is normally connected to Pin 21A-14.

6.2 ALU Clock Timing (Functional Schematic 35-404D08)

The ALU clock is similar in concept to that of the CPU and is factory adjusted for a 100 nanosecond repetition rate and a 30 nanosecond pulse. AREP0 is normally connected to Pin 20K-11 (7M4). AWDTH0 is connected to Pin 20K-14.

6.3 Primary Power Fail Check (Functional Schematic 35-405D08)

The Primary Power Fail Detector is located on the IOU board. The circuit is checked and adjusted as follows:

1. Connect the Primary Power Cord of the CPU power supply into a variable voltage source (Variac or equivalent).

2. With the line voltage set at the nominal value (115.0 VAC), turn the Power on.

3. Adjust Potentiometer 00AR5 (the second pot from the left side of the IOU board) to generate the Power Fail condition on CL070 (back panel Terminal 121-0) when the AC line voltage is set for 103.5 V (i.e., 10% low). System Initialize line (SCLR0) Terminal 126-0 should become low active approximately 3 to 4 milliseconds after CL070 is active.

4. With nominal line voltage, load the Model 80 Test Program and depress the EXEcute switch. While the program is running, remove the AC line cord from the primary power source.

NOTE

The TTY will run-open if connected into a different power source.

5. Connect the AC line cord back into the power source. The TTY should stop cycling. Depress the EXEcute switch and the test program should continue to run.

6. Repeat Step 4, but turn the Console Power switch off instead of removing the AC line cord.

6.4 TTY Timer Adjustment

The only adjustment on the TTY controller controls the frequency of the 440Hz timing multivibrator. The adjustment is made in the following manner:

1. Initialize the system.

2. Connect an oscilloscope to TP-TMG1A (located on the far left side of the IOU board).

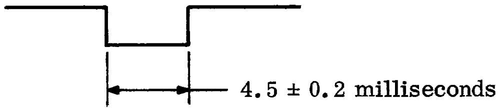
   Vertical scale: 2 volts/centimeter

   Horizontal scale: 1 milliseconds/centimeter

   Sync: Internal, negative

3. Generate a continuous stream of data from the TTY by reading a tape or by the Repeat function of the keyboard.

4. Adjust Potentiometer 00AR6 (located on the far left side of the board-next to the test point) for the waveform shown below.



7. MNEMONICS

The following sections provide a brief description of each mnemonic found in the Model 80 Processor. The source of each signal on Schematic Drawings 35-403D08 (CPU), 35-404D08 (ALU), and 35-405D08 (IOU), is also provided.

7.1 CPU Mnemonics (35-403D08)

MNEMONIC	MEANING	LOCATION
A(00:15)	A Bus	Sheet 5
ALCH(00:15)	A Bus Latch Register Input	Sheet 6
ASEL(00:04)	A Bus Source Select	Sheet 5
AST	ALCH Multiplexor Strobe	6R3
ATN(00:03)	Interrupt Attention Lines	3F3
B	B Bus	Sheet 4
BINH0	Branch and Inhibit Display Interrupt	3F7
BLCH(00:15)	B Bus Latch Register Input	Sheet 6
BSEL(00:04)	B Bus Source Select	Sheet 5
BST	BLCH Multiplexor Strobe	6N3
CA(00:15)	Control Address to Memory	Sheet 9
CCC	Condition Code C Flag from Modules	7D1
CD(M00:15)	Control Data Bus to Memory	Sheet 8
CFLG	Processor C Flag	3A9
CFTCH	Control Instruction Fetch to Memory	1R4
CMAR140	Clear MAR14	9C7
CMLC140	Clear MLC14	9A2
CRDY	Control Ready from Memory	1K4
CREQ	Control Request to Memory	1R7
CRLR(04:15)	Clear ROM Location Register Inputs from Test Set	Sheet 4
CWRT	Control Write to Memory	1R8
D	D Field of Micro Instruction	10L9
DISPLY1	Display Interrupt	3E4

7.1 CPU (continued)

MNEMONIC	MEANING	LOCATION
E	E Field of Micro Instruction	10L7
ENFLG	Enable PSW Manipulation from Condition Code	10L9
EXEC	Execute Instruction	2B4
FTCH	Instruction Fetch Decoded	1L4
FSEL(00:03)	Function Select Field or RIR	Sheet 10
GA	Gate A Field to SSEL	10G3
GBR	Gate Branch to RAG	3D4
GCC	Condition Code G Flag from Modules	7B1
GFLG	Processor G Flag	3A7
GINT	Gate Interrupt	3K4
GMDR	Gate MDR to Memory Bus	8B8
GRLCA	Gate Low RLC to RAG	3D4
GRLCB	Gate High RLC to RAG	3D5
GRSB	Gated RSB to RAG	3D3
GS	Gate S Field to SSEL	10C4
GUD	Gate UDR to SSEL	10A4
GUDR	Gate UDR to BSEL	5M5
GUS	Gate USR to SSEL	10F4
GUSR	Gate USR to BLCH(12:15)	6R3
GUIR	Gate UIR to RAG	3D3
GUTR	Gate UIR or TRAP to RAG	3D1
GXFR	Gate B Bus to RAG	3D2
ILEG	Illegal Interrupt	3L2
IHHCLA	Inhibit Clock from Control Store	1G3
INHCLB	Inhibit Clock from Test Set	1G3
INTA	Any Interrupt Bus Illegal Service	3N4
INTB	Illegal Interrupt Service	3N3
INTEBL0	Interrupt Group Enable	3L6

7.1 CPU (continued)

MNEMONIC	MEANING	LOCATION
INTR	Any Interrupt Service	3J2
IWAIT1	Flip-Flop Set when Waiting for Instruction from Memory	1N4
JAM	Jam MLC to MAR	9B5
KEB1	Encode F field for Module 0	3D6
KLCLK	Kill Clock	1G3
KSIG	Extension of F Field from Micro Control Field	10M9
LCC1	Condition Code L Flag from Modules	7A1
LDMAR0	Load MAR	7B7
LDMLC0	Load MLC	9D2
LDRLR0	Load RLR	2B5
LFLG1	Processor L Flag	3A7
LNKAD0	Gating Function for RLC to S Bus	1A5
MARCK	Composite MAR Clock	Sheet 9
MARD(00:15)	Multiplexed MAR Input Data	Sheet 9
MARP21	Increment MAR Plus Two	9C7
MC(00:03)	Memory Control Field of Micro Instruction	Sheet 10
MCENBL0	Activate MC(00:03)	10J3
MCSEL0	Select Proper MC Field from Instruction	10K3
MDR(00:15)	Memory Data Register	Sheet 8
MDRCK	MDR Clock	8B4
MDSIG1	Module Signal to CPU	2A6
MLC(00:15)	Memory Location Counter	Sheet 9
MLCCK	MLC Clock	Sheet 9
MLCP21	Increment MLC Plus Two	9B3
MMF0	Machine Malfunction Interrupt	3F4
MOD00	Module Zero Decoded	1D1
MUDR(08:11)	Memory User Destination Register	Sheet 8
MUSR(12:15)	Memory User Source Register	Sheet 8

7.1 CPU (continued)

MNEMONIC	MEANING	LOCATION
PASS	Branch Test Passed	3G8
PK	Memory Reference Kill Clock	1D3
PPF0	Primary Power Fail Interrupt	3M5
PSW(00:15)	Program Status Register	Sheet 7
PSWCK	PSW Clock	7C7
PVMD0	Privilege Mode to Memory Controller	3M1
RAG	ROM Address Gates	Sheet 4
RD(00:31)	ROM Data Bus	Sheet 2
REGWT	Enable Register Write	1F5
RGH0	Gate RD(00:15) to BLCH(00:15)	4M1
RGL0	Gate RD(16:31) to BLCH(00:15)	4M1
RIR(00:31)	ROM Instruction Register	Sheet 2
RIRCK	RIR Clock	Sheet 2
RLC	ROM Location Counter	Sheet 4
RLR	ROM Location Register	Sheet 4
RLRCK	RLR Clock	2D4
RMWP	Control Store Write Pulse	1F8
RMWRT	Decoded Control Store Write Instruction	1E8
RRX0	Decoded RRX Instruction	2B3
RS(00:03)	Decoded ROM States	1D8
RSA	ROM State Register (LSB)	1H5
RSB	ROM State Register (MSB)	1H8
S(00:15)	Module S Bus	Sheet 4
SCC0	Set Condition Code Control Line	7F6
SCLR	System Clear	1K9
SMAR	S Bus to MAR	10B9
SMAR14	Set MAR14	10B8
SMDR	S Bus to MDR	10D9
SMLC	S Bus to MLC	10C9

MNEMONIC	MEANING	LOCATION
SMLC14	Set MLC14	7S6
SPSW	S Bus to PSW	10D9
SRLR	Set RLR(00:15)	2D5
SSEL	S Bus Destination Select	Sheet 10
ST(00:15)	Composite S Bus and ALU Result Bus	Sheet 9
STRB	CPU Clock	1K2
STRT	Start to Modules (RS031)	10H9
TRAP(13:15)	Encode Interrupt Vector	3L3
TREP0	Clock Repetition Rate Adjustment	1F1
TWDTH0	Clock Width Adjustment	1F1
UDR(08:11)	Residual User Destination Control Register	7F4
UIR(00:07)	User Instruction Register	Sheet 8
USR(12:15)	Residual User Source Control Register	7M4
VCC1	Condition Code V Flag from Modules	7C1
VFLG1	Processor V Flag	3A9
ZFLG	Processor Zero Flag	3A6

7.2 ALU Mnemonics (35-404D08)

MNEMONIC	MEANING	LOCATION
A(00:15)	A Bus	Sheets 1 and 2
ACLK	Basic ALU Clock	7L9
ACNT(00:03)	Least Significant 4 Bits of Iteration Counter	8D4
ACRY	Carry from Iteration Counter (EACNT, ACNT=31)	8G5
ALCH(00:15)	A Bus Latch Register	Sheets 1 and 2
ALCLK	ALCH(00:15) Clock	8N9
ALMOD	Logical Mode	4G4
ALSEL	ALU Module Selected	7N1
ALSTRT	ALU Selected and STRT	7R6
AMEH	A Stack High (Micro-Registers) Memory Enable	8C9
AMEL	A Stack Low (General Registers) Memory Enable	8B9
AMODE1	ALU Mode	4H4
ARSH	Arithmetic Shift	7C6
ASA	Arithmetic State Register (LSB)	Sheet 6
ASB	Arithmetic State Register (MSB)	Sheet 6
ASEL(00:04)	A Bus Source Select	Sheet 8
ASIGN	A Bus Sign	7F3
ASTK(01:03)	A Stack Register Select	Sheet 8
AWE	A Stack Write Enabel	8H9
AWRT	ALU Write, Enables ALU Write to Register Stacks	6L3
AZR0	R(00:15) Zero	5D9
B(00:15)	B Bus	Sheets 3 and 4
BLCH(00:15)	B Bus Latch Register	Sheets 3 and 4
BLCLK	BLCH(00:15) Clock	8M9
BMEH	B Stack High (Micro-Registers) Memory Enable	8F9
BMEL	B Stack Low (General Registers) Memory Enable	8F9
BSEL(00:04)	B Bus Source Select	Sheet 8
BSTK(01:03)	B Stack Register Select	Sheet 8
BWE	B Stack Write Enable	8H9

MNEMONIC	MEANING	LOCATION
CFLG	Processor C Flag	6B9
CIN	Arithmetic Carry In	5B9
COUT	Arithmetic Carry Out	5C9
CSET	Composite ALU C Flag Logic	6C6
DIV	Divide Instruction	7J1
DSIGN	Divide Sign	7F5
ESHFT	Extended Shift Instruction	6N3
EACNT	Extended Iteration Count (MSB)	8G1
FCLK0	Processor Flags Clock	6C6
GENL	ALU Enable GCC	6D9
GFLG	Processor G Flag	6B9
INHACK0	Test Set ALU Clock Inhibit	7L1
INHS0	Inhibit MQ Shift	7F1
IZR0	Intermediate Zero (Most Significant Halfword)	
ILFLG	Intermediate LFLG (Most Significant Halfword)	
LFLG	Processor L Flag	6B9
LMOD(00:03)	Arithmetic Devices Mode Select	4F8
M	Composite Multiply Logic	7C9
MD	Multiply or Divide Instruction	7M2
MDSEL(00:02)	Module Select	7N1
MFIN	Module Finish	7N9
MQ(00:15)	Multiplier/Quotient Shift Register	Sheet 7
MSIG	Module Signal (ALU=CFLAG)	7R9
MUL	Multiply Signal	7B1

MNEMONIC	MEANING	LOCATION
R(00:15)	ALU Result Bus	Sheet 5
RAG(04:15)	ROM Address Gates	Sheet 9
RD(00:31)	ROM Data Bus	Sheets 3 and 4
RGH	Gate RD(00:15) to BLCH(00:15)	Sheets 3 and 4
RGL	Gate RD(16:31) to BLCH(00:15)	Sheets 3 and 4
ROT	Rotate Instruction	7A2
RZR0	R(00:15) Zero	6K9
S(00:15)	S Bus	Sheet 5
SEL	Shift Enable Left	7E6
SER	Shift Enable Right	7E6
SHFTA	Shift A Bus	1A9
SL0	Serial Left Data to MQ Register	7H5
SR0	Serial Right Data to MQ Register	7B8
SSEL	S Bus Register Designation	Sheet 8
ST(00:15)	Composite ALU Result Bus or S Bus	Sheet 5
STRB	CPU Strobe	8R1
STRT	CPU Start Signal to Modules	6D1
SUM	ALU Sum Flip-Flop	Sheet 5
VFLG	Processor Overflow Flag	6H9
ZFLG	Processor Zero Flag	6A9
ZSET	Composite ALU Z Flag Logic	6E9

7.3 IOU Mnemonics (35-405D08)

MNEMONIC	MEANING	LOCATION
A0/A1	Output of Address Decoder for TTY	7H7
A(000:070)	A Bus, High Byte	Sheet 3
A(080:150)	A Bus, Low Byte	Sheet 3
AC1	12VAC Input to Primary Power Fail Detector	6A2
AC3	12VAC Input to Primary Power Fail Detector	6A2
ACK0	Acknowledge Interrupt MPX Channel	5R7
ADA	Address Flip-Flop for TTY Controller	7K7
ADB	Address Flip-Flop for Display Controller	7K9
ADRS0	Address Control Line MPX Channel	4S9
ARM	Interrupt Arm Flip-Flop for TTY	7R7
ARST	Auto Restart, MCR Strap	2C7
ASYNA0	Address Sync for TTY Controller	7K8
ASYNB0	Address Sync for Display Controller	7L8
ATN	Interrupt Attention Flip-Flop	8N8
ATN000	Normal MPX Channel Interrupt to CPU	8N7
ATNA	Interrupt differentiator Flip-Flop for BSY1	8M8
ATNB	Interrupt differentiator Flip-Flop for EX0 (not used)	8M8
ATSYN0	Attention Sync Pulse for ACK Address	8J9
B0/B1	Output of Address Decoder for Display	7J7
B(000:070)	B Bus, High Byte	Sheet 3
B(080:150)	B Bus, Low Byte	Sheet 3
BA	Buffer Active Flip-Flop (sets when buffer is loaded, cleared when buffer is unloaded)	9A6
BLK	Serial feedback Block Flip-Flop for TTY	7R8
BNKA	Bank A, MCR Strap (Bit 05)	3G7
BNKB	Bank B, MCR Strap (Bit 04)	3F7
BR(00:07)	Buffer Register - Eight Stages, active only in Read Mode	Sheet 7
BRK0/1	Break Detect Signal - (Status Bit 2)	8H8
BSY0/1	Busy Signal (Status Bit 4)	8H7

MNEMONIC	MEANING	LOCATION
CA150	CPU - Memory Address Line (Least Significant Bit)	1E1
CATN	Console Attention Flip-Flop	8D4
CCC1	Condition Code Bus - C Bit	5N4
CL070	Primary Power Failure Control Line	4N9
CLK0/1	Timer Clock Pulses (Eleven Per Character)	8N4
CLRA0	Clear Line for Cycle Counter	2L6
CLRB0	Clear Line for DFST and TESYN Flip-Flops	2D8
CLRC0	Clear Line for KD and KSYN Flip-Flops	2E9
CLRD0	Clear Line for LESYN Flip-Flops	2G2
CM0	Clear MCR (CMCR Function)	1H9
CM(110:150)	Clear MCR Flip-Flops M11:15	Sheet 5
CMD0	Command Control Line MPX Channel	5N8
CMCR0	Clear MCR (CM0 or SCLR0A)	1J9
D(000:007)	D Bus, High Byte	Sheet 4
D(080:150)	D Bus, Low Byte	Sheet 4
DA0	Data Available Control Line MPX Channel	5N8
DACK0	Data Channel Acknowledge MPX Channel	5N6
DBEN1	D Bus Enable	1L9
DCKH1	Clock for Data Register High	4M6
DCKL1	Clock for Data Register Low	4H6
DD0/DD1	Device Data Signals From Schmidt Trigger Receiving Circuit	9G8
DFST	Timing Control Flip-Flop, Detects DSTRT	2D4
DL(00:07)	Buffered Copy of D(08:15) for TTY/Display Controllers (Double Rail)	Sheet 7
DLA1	D MUX Select A	4H1
DLB1	D MUX Select B	4G1
DMA1	Data MUX Select Line A (TTY/Display)	7H5
DMB1	Data MUX Select Line B (TTY/Display)	7H6
DPF0	Data Parity Fail Line From MBC	5D3
DR0	Data Request Control Line MPX Channel	4S9

MNEMONIC	MEANING	LOCATION
DR(00:07)	Data Register - High Byte	Sheet 4
DR(08:15)	Data Register - Low Byte	Sheet 4
DRN	Start Bit Stage of Shift Register (controls transmit line in Write Mode)	9G5
DSCLR0	Delayed SCLR0 Signal	6G7
DSPLY1	Display Controller Interrupt Line to CPU	8E5
DSPSYN0	Composite SYN for Display Controller	7G8
DSTRT0/1	Start Pulse for D Bus Operations	2C5
DT	Device Transmitting Flip-Flop (set when RCV loop starts the timer)	9G6
DTMG0	Delayed TMG0 Signal	8J1
DU1	Output of Device Unavailable Detector - Active for TTY in OFF/LOCAL Modes (Status Bit 7)	9J7
DX1	Serial Data Input to Shift Register (Line Data in Read Mode/all ONE's in Write Mode)	9C2
EBL	Interrupt Enable Flip-Flop for TTY	7R7
ENT30	Enter Time Period T3	2L2
EOC0/1	End of Character (Output of Character Counter)	8L4
EPF	Early PPF Timer (1 millisecond)	6E6
ESNC0	Normally Closed Line from EXEcute Switch	8A3
ESNO0	Normally Open Line from EXEcute Switch	8A4
EX0/1	Examine Signal - (Status Bit 5)	8H9
EX1	Examine bit of TTY Status	8H9
EXA0	Auxillary Initialize Input A	6N1
EXB0	Auxillary Initialize Input B	6N2
FLSYN0	False Sync Signal (D Bus Operation)	6M7
FPOW0	Power Down/Initialize Function	1M9
FSL00/01/02/03	Function Code Lines from CPU	Sheet 1
FSTP0	Stop Function Gate - Terminates SHFT Pulses	8M5
FWAIT	Flip-Flop for WAIT Indicator	1L8

MNEMONIC	MEANING	LOCATION
GCC1	CC Bus - G Bit	5N3
GDH1	Gate D - Bus High	5H8
GDL1	Gate D Bus Low	5H6
GKB1	Control Line Enable for Periods T2 and T3	5L9
GLTCH0	Start Glitch Signal - Clears TMG1	8H3
GM0/1	Gate MCR (SMCR function)	1N9
GP1	Timer for POUT Function	6J8
GPX	Flip-Flop for POUT Function	6J8
GSTP1	External Gate for STP Flip-Flop	6M6
GSTRT1	Gated Start (STRT signal gated by module decoding)	1R5
HW0	Halfword Test Line - MPX Channel	2H2
IA0	Illegal Address Line From MBC	5D4
INCR	Increment/Normal Flip-Flop	8C2
INIT0	Initialize Line from Console Switch	6A1
IPF0	Instruction Parity Fail Line from MBC	5D2
K1	System Initialize Relay (Dry Reed)	6A5
KA	Cycle Counter - First Stage	2K5
KB	Cycle Counter - Second Stage	2L5
KC	Timing Control Flip-Flop, Control Line Timing	2G4
KD	Timing Control Flip-Flop, Control Line Timing	2G5
KHW	Halfword Flip-Flop, DACK Operation	2R5
KSIG0	Function Code Line from CPU	1J1
KSTM1	Kill Start Timer Lead	6D8
KSYN	Timing Control Flip-Flop, SYN Stretch	2H8
KT	Cycle Counter - Terminate Flip-Flop	2N5
KTA	False Sync - Terminate Flip-Flop	2M1
KTM	Test Point - Ground to Kill Start Timer	6C7

7.3 IOU (continued)

MNEMONIC	MEANING	LOCATION
LA0	Gate Lines for Display Registers	8E8
LB0	Gate Lines for Display Registers	8E8
LC0	Gate Lines for Display Registers	8E8
LD0	Gate Lines for Display Registers	8E8
LCC1	CC Bus - L Bit	5N2
LDBR1	Load Buffer Register Pulse (active in Read Mode only)	9C7
LESYN	Timing Control Flip-Flop, Detect SYN Start	2G2
LX1	Master Gate Pulse for LA0/LB0/LC0/LD0	8D9
M11	MCR Flip-Flop Bit 11 (STF)	5E4
M12	MCR Flip-Flop Bit 12 (IA)	5E3
M13	MCR Flip-Flop Bit 13 (DPF)	5E3
M14	MCR Flip-Flop Bit 14 (IPF)	5E2
M15	MCR Flip-Flop Bit 15 (EPF)	5E2
M041	Bank B, MCR Strap	3K7
M051	Bank A, MCR Strap	3L7
M081	Spare MCR Strap	3A7
M091	Auto Restart, MCR Strap	3B7
M101	Console Attention, MCR Bit	3E7
MACK0/1	Master ACK Function (ACK or DACK)	1K9
MDSL(00:02)	Module Select Lines From CPU	1N1
MFIN0	Module Finish Line to CPU	1G9
MMF0	Machine Malfunction Interrupt Line to CPU	5H3
MSIG0	Module Finish Line to CPU (Program Branch)	1H9
MST0	Master Data Strobe for Both TTY and Display	7H6
MTA/MTB	Master TTY Timer (440Hz Output)	8L3
MTC/MTD	Timer Clock Counter (110Hz Output)	8L3
MX121	Composite MCR Bit to CC Bus and S Bus (strapped for IA and/or STF)	5H2
OV	Overflow (Error) Flip-Flop (sets when buffer is loaded twice without being unloaded)	9D5

7.3 IOU (continued)

MNEMONIC	MEANING	LOCATION
PEX1	Pulse Execute from EX switch	8C4
PFDT0/1	Power Fail Detector Output	8K3
PFM	PPF Detector Interlock - Master Unit	6M3
PFS	PPF Detector Interlock - Slave Unit	6M3
POFF0	Power Off Line from Console Switch	6A1
POUT1	Pulse Output Function	6K9
POWDN0	Power Down Line	6J4
PPF	Primary Power Fail Flip-Flop	6F6
PPF0	Primary Power Fail Interrupt Line	6M5
RACK0	Receive Acknowledge Interrupt Signal	8K7
RN	Negative Side of Receive Loop (TTY)	9M8
RP	Positive Side of Receive Loop (TTY)	9M8
RST0	Reset Line for XA, XB, and XC Counter	8F2
S(000:150)	S Bus, High Byte	Sheet 3
SATN0	Set ATN Flip-Flop Signal	8N8
SCC0	CC Bus Strobe Line	5N1
SCLR0	System Initialize Line	6A9
SCLR0	System Initialize Line - MPX Channel	6A9
SCLR0A	System Initialize Line for IOU Board (except for TTY/Display controllers)	2R6
SCLR0B	System Initialize Line for TTY/Display Controllers	7M8
SD(00:07)	Bidirectional Byte Bus to Display Panel	Sheet 7
SH10	Gate Lines for Display Switches	8E6
SL00	Gate Lines for Display Switches	8E6
SHA1	S MUX High - A Select	1F9
SHB1	S MUX High - B Select	1F9
SHFT1	Shift Register Pulses (nine per character)	8N4
SLA1	S MUX Low - A Select	1F9
SLB1	S MUX Low - B Select	1E9

7.3 IOU (continued)

MNEMONIC	MEANING	LOCATION
SNGL	Single Mode Flip-Flop	8C5
SR(00:07)	Shift Register - Eight Data Stages	Sheet 9
SR0	Status Request Control Line - MPX Channel	5N7
SSGL1	Single Mode Line from Display Panel	8A5
STA1	Strobe for CC - Code Gates	5L4
STB1	Strobe for CC - Code Gates	5L4
STCC1	Strobe for CC - MUX Gates	5N5
STF0	Start Timer Fail Signal (non D Bus operation)	6M7
STH0	S MUX Strobe - High Byte	1A9
STL0	S MUX Strobe - Low Byte	1D9
STMA	Start Timer (35us)	6E8
STMB	Start Timer Flip-Flop	6F8
STP	System Stop Flip-Flop	6J6
STP1A	Buffered Output from STP Flip-Flop	6M6
STPF1	Start Power Fail Timer	6L4
STRT0	Module Start Line From CPU	1R1
SYN0	Sync Test Line - MPX Channel	2A7
T11	Control Line Enable for Period T1	5L8
TA/TB/TC/TD	Four Stage Character Counter	8L5
TACK0	Transmit Acknowledge Interrupt Signal	8R6
TATN0/1	Clear Line for ATN/ATNA and ATNB Flip-Flops	8J9
TB	Delay Line Control Flip-Flop	2D4
TC0/1	Timing Control Delay Pulses	2F2
TDU	Device Unavailable Line From TTY	9M7
TERM1	Gating signal for S MUX	2R1
TESYN	Timing Control Flip-Flop, detect SYN end	2D6
TMG	Timing Gate Control Flip-Flop	8J3
TN	Negative Side of Send Loop (TTY)	9M6

MNEMONIC	MEANING	LOCATION
TNS0	Transmit (Send) Line to TTY	9K6
TNSA1	Transmit Signal From SR (Write Mode)	9J6
TNSB1	Transmit Signal From RCV-Loop (Read Mode)	9J6
TP	Positive Side of Send Loop (TTY)	9M5
TSYN0	Composite SYN and Data Strobe for TTY Controller	7M6
TMG1A	Timing Gate Test Point	8M1
VCC1	Condition Code Bus - V Bit	5N3
VK1	Operate Voltage for Relay K1	6A5
WAIT1	WAIT Lamp Control Line to Display Panel	8E6
WRT	Write Mode Execute Flip-Flop for TTY	8J5
WT	Write Mode Storage Flip-Flop for TTY	7N9
X1, --X6	Six Leads to Front Terminal Strip of Chassis	Sheet 6
XA	First Stage of Display Register Counter	8C7
XB	Second Stage Display Register Counter	8C8
XC	Switch Gate Counter for Display Panel	8C6
XLC	Line Check Flip-Flop (checks for START Glitches and Break conditions)	9H6
XPF	Power Fail Stop Timer (1 millisecond)	6H6
XRPA	Pull Up Resistor Networks for Unused Logic Inputs on IC's (1K to P5)	5B1
XRPB	Pull Up Resistor Networks for Unused Logic Inputs on IC's (1K to P5)	8H4
XRPC	Pull Up Resistor Networks for Unused Logic Inputs on IC's (1K to P5)	8A1

MEMORY

02-247A21
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MODEL 80 MAIN MEMORY SYSTEM MAINTENANCE SPECIFICATION

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MODEL 80 MAIN MEMORY SYSTEM MAINTENANCE SPECIFICATION

1. INTRODUCTION

This specification applies to the INTERDATA Model 80 Main Memory System components listed in Table 1.

TABLE 1. MODEL 80 MAIN MEMORY COMPONENTS

PART NUMBER	PRODUCT NUMBER	BOARD PART NUMBER	MNEMONIC	FUNCTION
Part of Basic M80 System		35-407	MBC	Memory Bank Controller (controls one to four MSUs)
02-247	M80-301	35-406	MSU	Memory Storage Unit 8K X 17 bits (Parity)
02-247F01	M80-300	35-406F01	MSU	Memory Storage Unit 8K X 16 bits (No Parity)
02-248	M80-101	35-408	MPC	Memory Protect Controller

01-xxx and 02-xxx part numbers cover hardware, software, and documentation. 35-xxx part numbers refers to plug-in circuit cards.

2. SCOPE

This specification describes the overall operation of the Model 80 Main Memory System, consisting of one MBC and up to four MSUs; and the memory system external connections to the Central Processing Unit (CPU) memory bus, the Direct Memory Access (DMA) port, and the Memory Protect Controller (MPC). The Memory Storage Unit and the Memory Bank Controller are described in separate sections of this specification. This specification also provides block diagram analysis, timing information, troubleshooting and maintenance, and a mnemonic list for the MBC and MSU.

3. SYSTEM BLOCK DIAGRAM

The main memory system and its relationship to the rest of the Model 80 System is shown in Figure 1. The MSUs contain the memory storage elements and the MBC contains most of the control circuits and all registers. Up to four, 16,384 byte, MSUs can be driven by one Memory Bank Controller (MBC) for a maximum storage capacity of 65,532 eight-bit bytes. The memory system provides two independent ports (CPU and DMA). The CPU port to memory is for the exclusive use of the Model 80 Processor. The DMA port provides access to the main memory system over a multiplexed Direct Memory Access Channel (DMAC). The DMAC Bus is compatible with the Model 70 system and accepts a New Series (NS) Selector Channel. Refer to the NS Selector Channel Installation Specification, 02-232M01A20, for detailed information. The Memory Protect Controller also interfaces to the Model 80 Main Memory System. It provides memory write protect for 64 blocks (1K bytes/block) on CPU memory operations.

The MBC controls access to the MSUs from the two asynchronous independent busses (CPU and DMA), and the MBC internal memory refresh generator. The MBC provides memory service according to a priorty scheme hardwired into the MBC Interlock circuit. Address, data, and control information from the DMA or CPU to the main memory system is processed by the MBC and directed to the designated MSU for Write or Read operation.

In addition to providing memory service to the DMA and CPU ports, the MBC must generate its own memory requests and direct the MSUs to perform refresh cycles. A refresh cycle is the same as a read cycle and must be performed at a rate of 32 cycles every 2 milliseconds (32 different addresses must be refreshed-each of the 32 addresses must be refreshed once every two milliseconds). Refresh cycles are necessary to prevent the memory cells from losing their stored information.

The MSU accepts address, data, and control information from the MBC and performs memory Read or Write cycles.

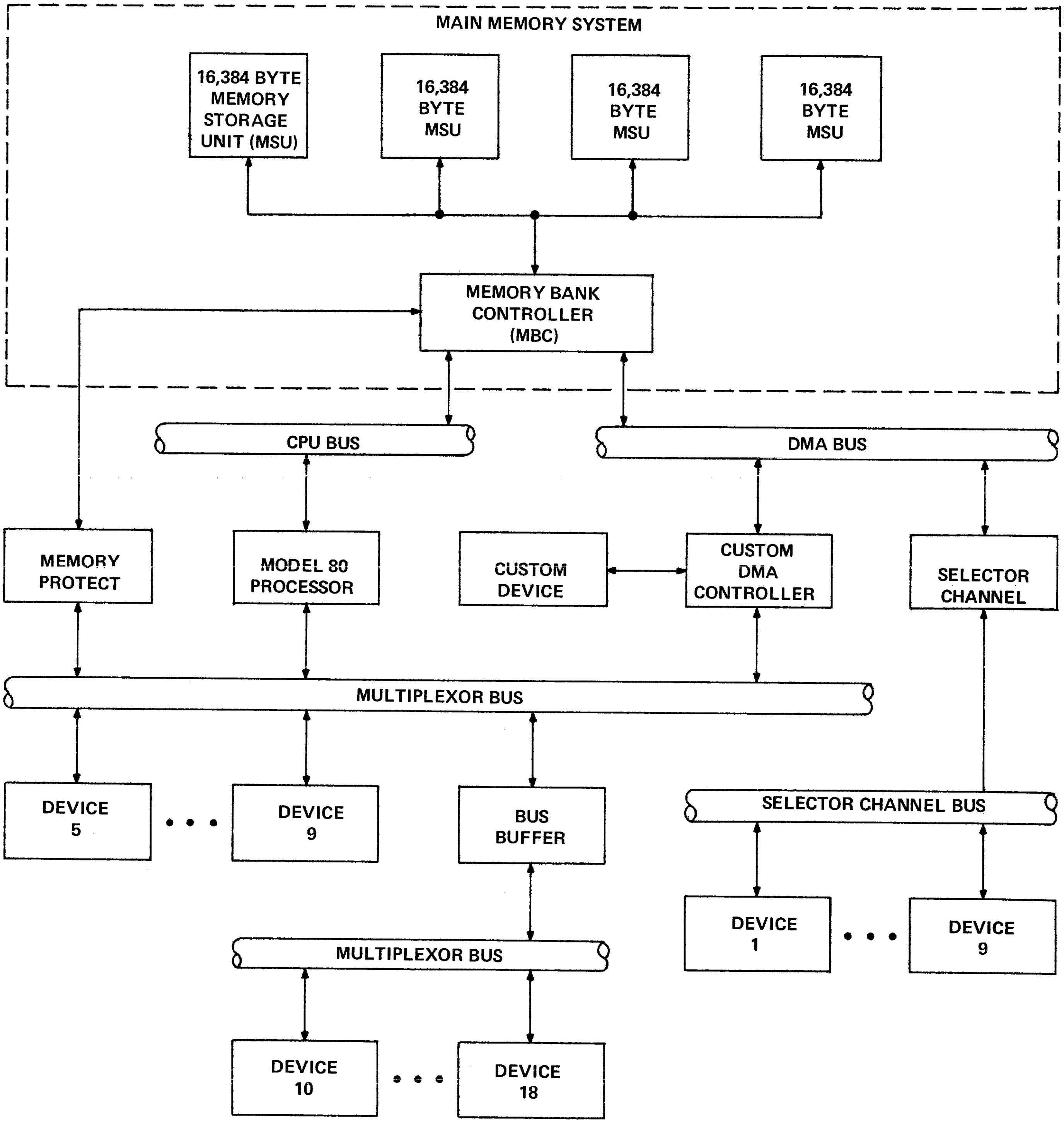
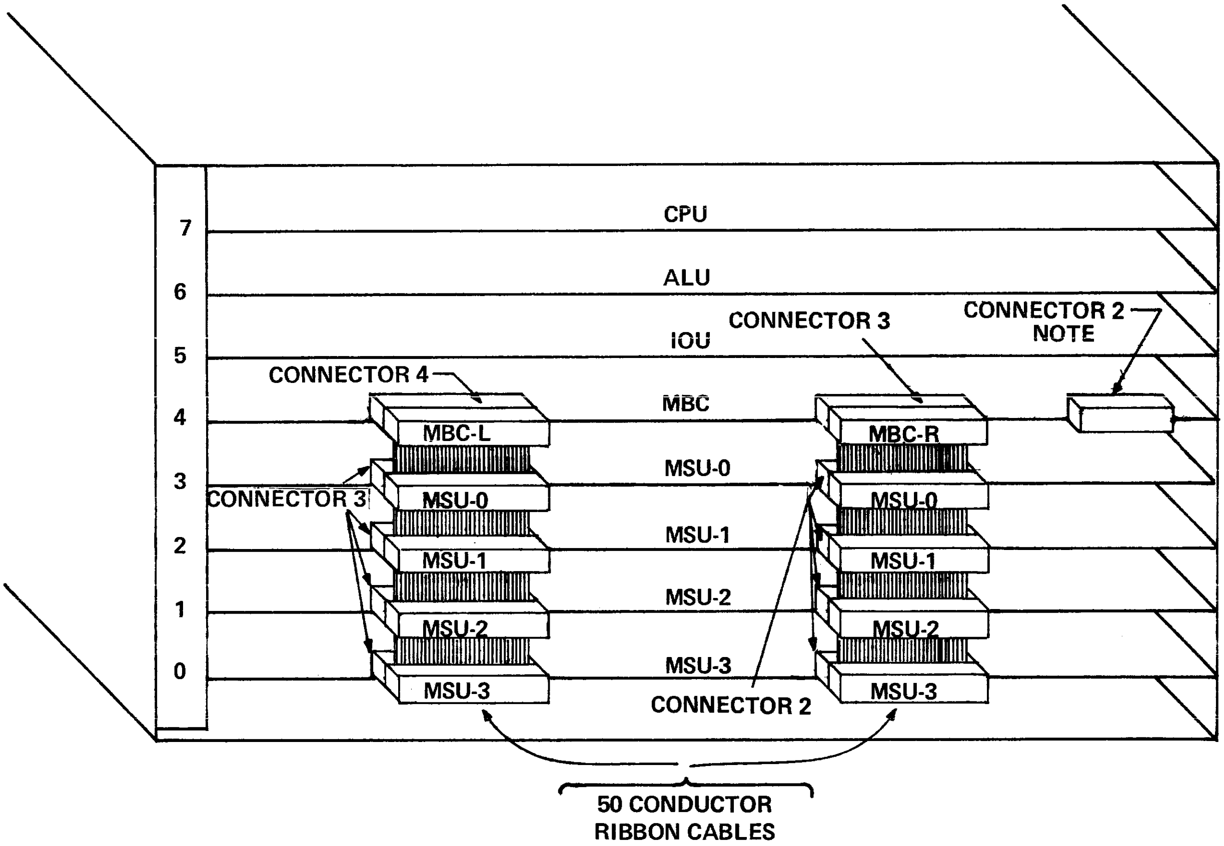

MAIN MEMORY SYSTEM
16,384 BYTE MEMORY STORAGE UNIT (MSU)
16,384 BYTE MSU
16,384 BYTE MSU
16,384 BYTE MSU
MEMORY BANK CONTROLLER (MBC)
CPU BUS
DMA BUS
MEMORY PROTECT
MODEL 80 PROCESSOR
CUSTOM DEVICE
CUSTOM DMA CONTROLLER
SELECTOR CHANNEL
MULTIPLEXOR BUS
DEVICE 5
DEVICE 9
BUS BUFFER
SELECTOR CHANNEL BUS
DEVICE 1
DEVICE 9
MULTIPLEXOR BUS
DEVICE 10
DEVICE 18

Figure 1. Model 80 System

4. MBC/MSU PHYSICAL DESCRIPTION AND INTERCONNECTION

The assembly of one MBC and one MSU constitutes one memory bank of 16K bytes plus halfword parity. Expansion of the memory bank from 16K bytes (MBC and one MSU) to 64K bytes is accomplished by plugging three additional 16K byte MSU boards into the main frame chassis. The MSU boards are referenced to the MBC. That is, the MSU in the first slot adjacent to the MBC is designated MSU0, the next MSU is designated MSU1, etc. Refer to Figure 2.


7
6
5
4
3
2
1
0
CPU
ALU
IOU
MBC
MSU-0
MSU-1
MSU-2
MSU-3
CONNECTOR 3
CONNECTOR 2
NOTE
CONNECTOR 4
MBC-L
CONNECTOR 3
MSU-0
MSU-1
MSU-2
MSU-3
MBC-R
MSU-0
MSU-1
MSU-2
MSU-3
CONNECTOR 2
50 CONDUCTOR
RIBBON CABLES

NOTE: MBC CONNECTOR 2 IS FOR MEMORY PROTECT CONTROLLER WHEN EQUIPPED.

Figure 2. Standard MBC/MSU Interconnection

One to four MSU boards are connected to the MBC through two 50 conductor ribbon cables at the front of the chassis. The two cables are identified as MBC-L (MBC-Left) and MBC-R (MBC-Right) and are plugged in accordingly. All signals between the MSUs and the MBC are bussed over these cables. Refer to the Installation Specification, 01-053A20, for cable variations.

NOTE

When configured as a full system, the four Memory Storage Unit boards must be in adjacent card file slots.

4.1 Memory Bank Controller

The Memory Bank Controller (MBC) consists of one INTERDATA standard size mother board. The MBC occupies card file Slot 4. A back panel map is shown in Functional Schematic 35-407D08, Sheet 1. The MBC plugs into back panel Connectors 0 and 1 for power, ground, and CPU and DMA interface. Connector 2 provides the interface between the Memory Protect Controller and the MBC. Connectors 3 and 4 are connected to MSU Connectors 2 and 3 respectively.

4.2 Memory Storage Unit

A Memory Storage Unit consists of one INTERDATA standard size mother board. Up to four MSUs can be installed in card file Slots 0:3. The first MSU must be in Slot 3. Model 80 MSU component locator, part of 35-406D08, shows the physical location on the mother board of the major circuit blocks comprising the Memory Storage Unit. The MSU plugs into back panel Connectors 0 and 1 for power and ground. A back panel map is shown in Functional Schematic 02-247D08, Sheet 1.

5. MEMORY TECHNOLOGY

The Model 80 Main Memory uses Metal Oxide Semiconductor (MOS) memory technology. The actual memory storage device is a 1 X 1024 Random Access Memory (RAM). This device allows fast access read and write functions. However, it requires periodic refreshing of its stored information. The refresh function is very similar to a read function, that is, a memory cycle (Refresh cycle) timed exactly as a read cycle performs the refresh function. Therefore, the memory requires power at all times to preserve its stored information.

6. MODES

The Model 80 Memory System operates in two modes, Standby and Normal. When the Model 80 System is powered down, a partially powered mode, referred to as the Standby Mode, allows all but the main system to power down thereby preventing loss of stored information. The Standby Mode is entered any time System Clear (SCLR0) goes low, the system remains in this mode for two to four milliseconds after SCLR0 goes high. The Standby Mode is active whenever Console Initialize is depressed or the Console Power switch is placed in the OFF position.

It is important to recognize that when the Console Power switch is placed in the OFF position, the memory remains in a powered state. To remove all power from the memory, the toggle switch mounted on the front panel of the 35-014 Memory Power Supply must be turned to the OFF position. This switch must be OFF whenever memory boards are inserted or removed from the card files. See Model 80 Power System Maintenance Specification, 02-261A21, for more details.

CAUTION

> Never remove or insert any memory boards or cables unless the Power switch on the 34-014 Memory Power Supply is in the OFF position.

The Standby Mode requires only the P22 and P5S voltages from the Power System, in addition to P8 from the MBC. The P22 voltage remains at its nominal voltage during the Standby Mode and keeps the memory cells "alive". However, in addition to maintenance power to the memory cells, memory Refresh cycles must continue, which is the reason why P5S must also be present. P5S powers the logic and timing required to do Refresh cycles. In the Standby Mode, P5S is turned on every two milliseconds, by the 34-014 Memory Power Supply, to do a "Burst Refresh" (32 refresh cycles). After the Burst Refresh is performed, the P5S is switched off for another two milliseconds. When the system is returned to the Normal Mode, P5S remains at a constant 5.1 volt level.

In the Burst Refresh, the required 32 cycles/2 milliseconds refresh cycle rate is performed by doing 32 cycles at maximum repetition rate followed by an inactive 2 millisecond interval followed by another 32 cycles at maximum rate, etc. The 32 cycle burst is completed in 15 microseconds.

When the system enters the Normal Mode, Burst Refresh ceases and Single Refresh cycle continues the refresh function. In Single Refresh cycle, the refresh rate is a simple one cycle per 50 microseconds.

7. CPU/MBC INTERFACE

The CPU/MBC interface consists of 39 lines; 15 Address Lines, 16 bi-directional Data Lines, 4 Control Lines, 3 Status Lines, and an Initialize Line. Refer to Figure 3.

The lines in the CPU/MBC interface are:

Address Lines	CA00:14	CPU → MBC	15 Lines
Data Lines	CD00:15	⇄	16 Lines
Control Lines	CWRT0	→	1 Line
	CFTCH0	→	1 Line
	CREQ0	→	1 Line
	PVMD0	→	1 Line
Status Lines	CRDY0	←	1 Line
	IPF0	←	1 Line
	DPF0	←	1 Line
Initialize Line	SCLR0	→	1 Line

Address Lines CA00:14

The CPU address lines transfers 15 address bits from the CPU to the MBC during CPU Read and Write operations.

Data Lines CD00:15

The bi-directional data lines are used to transfer 16 bits of data during Read or Write operations, or 32 bits of data during an Instruction Fetch operation.

Control Lines

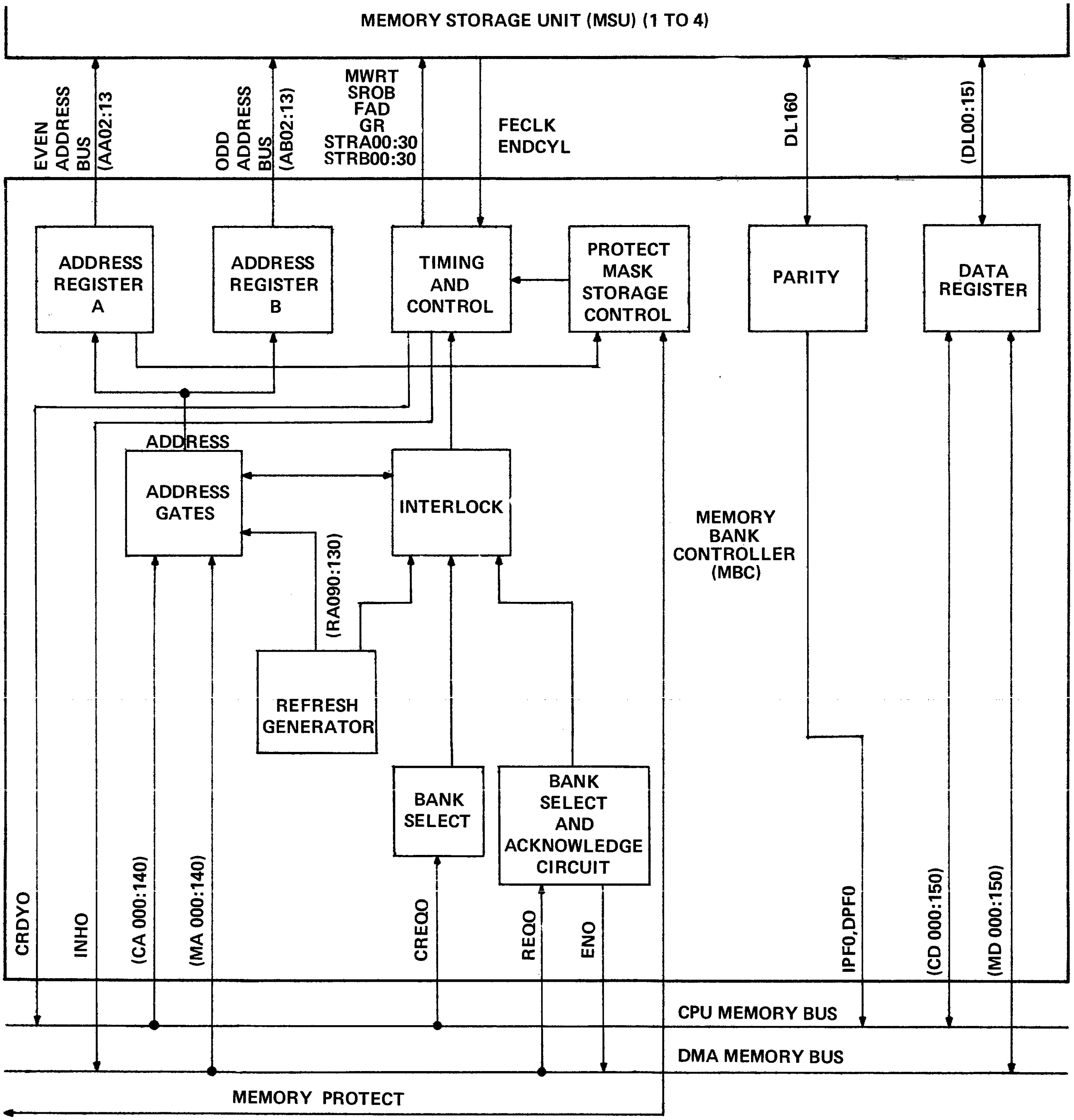
CREQ0	The CPU request signal is low-active when the CPU desires memory access.
CFTCH0	The CPU fetch signal is low-active during an Instruction Fetch operation (double read). When initialized, it accompanies CREQ0.
CWRT0	The CPU write signal is low-active during a Memory Write operation. When initialized, it accompanies CREQ0.
PVMD0	CPU privileged write signal low-active prevents writing into a protected 1K block of memory.

Status Lines

CRDY0	CPU data ready from memory. Low-active when data is valid during Read cycle, or when Write cycle no longer requires valid data and address from the CPU.
IPF0	Instruction Fetch operation (32 bits) parity fail.
DPF0	Data Read operation (16 bits) parity fail.

Initialize Line

SCLR0	The system clear signal goes low-active during Console Initialize, or Power Down. SCLR0 low produces Standby Mode operation.



MEMORY STORAGE UNIT (MSU) (1 TO 4)
EVEN ADDRESS BUS (AA02:13)
ODD ADDRESS BUS (AB02:13)
MWRT
SROB
FAD
GR
STRA00:30
STRB00:30
FECLK
ENDCYL
DL160
(DL00:15)
ADDRESS REGISTER A
ADDRESS REGISTER B
TIMING AND CONTROL
PROTECT MASK STORAGE CONTROL
PARITY
DATA REGISTER
ADDRESS
ADDRESS GATES
INTERLOCK
(RA090:130)
MEMORY BANK CONTROLLER (MBC)
REFRESH GENERATOR
BANK SELECT
BANK SELECT AND ACKNOWLEDGE CIRCUIT
CRDYO
INHO
(CA 000:140)
(MA 000:140)
CREQO
REQO
ENO
IPFO,DPFO
(CD 000:150)
(MD 000:150)
CPU MEMORY BUS
DMA MEMORY BUS
MEMORY PROTECT

Figure 3. Memory Bank Controller, Block Diagram

7.1 Types of Memory Operations

The CPU can be serviced with three different types of memory operations. They are Data Read, Write, and Instruction Fetch. A Data Read or Write operation does a simple 16 bit Read or Write operation on the address sent by the CPU.

Instruction Fetch

When the CPU lowers the CFTCH0 line along with CREQ0 and a valid address, the MBC responds with two sequential 16 bit readouts spaced by 150 nanoseconds. The first 16 bit readout is from the address sent by the CPU. The second 16 bit readout comes from the next sequential memory address (address sent by CPU plus two). Two consecutive CRDY0 signals are generated by the MBC along with the readout on the CD00:15 lines. The Processor lifts the CFTCH0 signal after receiving the first CRDY0.

7.2 CRDY0 Timing

The time between a CREQ0 and a CRDY0 can vary considerably since the memory may be queued for a DMA cycle, a Refresh cycle, both, or neither. This time delay ranges between 60 nanoseconds and 1150 nanoseconds. The width of CRDY0 is always 30 nanoseconds.

8. DMA/MBC INTERFACE

Up to four Selector Channels (SELCHs) may interface to the DMA Channel on a party line basis. Customer designed interfaces may be substituted for SELCHs on a one for one basis.

A daisy chain priority system exists, on the DMA port, which decides which one of the up to four SELCHs captures the DMA Bus when simultaneous service is desired. It should be recognized that after a SELCH competes for and captures the DMA Bus, the DMA Bus then competes for memory service with the CPU port and the memory's internal refresh requirements.

The DMA Channel permits 16 bit Memory Write or Memory Read operations but is not capable of Instruction Fetch operations.

The DMA/MBC interface consists of 35 lines; 15 Address Lines, 16 bi-directional Data Lines, 2 Control Lines, and 2 Status Lines. Refer to Figure 3. The lines in the DMA/MBC interface are:

Address Lines	MA000:140	DMA → MBC	15 Lines
Data Lines	MSD000:15	⇄	16 Lines
Control Lines	REQ0	→	1 Line
	WRT0	→	1 Line
Status Lines	EN0	←	1 Line
	INH0	←	1 Line

Address Lines MA000:140

The DMA address lines transfer 15 address bits to the MBC during DMA Memory Read and Memory Write operations. These lines cannot be activated by the SELCH register until the DMA priority scheme allows it.

Data Lines MSD000:150

The data lines are used to transfer 16 bits of data on Memory Write or Memory Read operations. These lines cannot be activated by the requester until the DMA priority scheme allows it.

Control Lines

REQ0	Up to four Selector Channels (SELCH) are OR-tied into the DMA request line (REQ0). Any SELCH may activate REQ0 any time memory service is desired.
WRT0	This line is pulled low by the requester if the type of memory service desired is a Write operation, however, the line cannot be activated until the DMA priority scheme allows it.

Status Lines

EN0	The MBC responds to a REQ0 by activating EN0. EN0 remains active for 100 nanoseconds during which time the requesting SELCH of the highest priority captures the DMA Bus. The rising edge of EN0 signals the capturing SELCH to alter the DMA Address Lines (MA000:140), the data to DMA Data Lines (MSD000:150) and DMA Write signal (WRT0), as required, within the next 100 nanoseconds.
INH0	The MBC generates INH0 for a Read cycle when data is valid on the Data Bus MSD000:150 or for a Write cycle when the memory no longer requires valid address or data on the DMA Bus. INH0 is active for 50 nanoseconds. The requesting DMAC disconnects itself from the DMA Bus within the next 100 nanoseconds.

8.1 DMA Priority

Since up to four SELCHs may be requesting memory service simultaneously, a priority system determines which one will use the DMA port. The system works in the following manner; when the system is originally configured, the SELCHs are assigned their respective priority by the card file position assigned. When a SELCH desires memory service, it pulses the Request signal (REQ0) low. The MBC responds to a REQ0 by activating the Enable signal (EN0) to the DMA Bus. EN0 remains active for 100 nanoseconds, during which time the requesting SELCH of the highest priority captures the EN0 signal and therefore the DMA Bus. The EN0 signal from the MBC is wired serially through all SELCHs with the order of connection determining the priority (first wired = highest priority). The highest priority SELCH that requests service captures the EN0 signal. A SELCH that does not request memory service relays the EN0 signal to the next SELCH of lower priority. The rising edge of EN0 signals the capturing SELCH to gate address and data and the DMA Write signal (WRT0) onto the DMA Bus within the next 100 nanoseconds. The trailing edge of EN0 also raises the REQ0 signal unless the DMA Bus has additional requests on the REQ0 line. One hundred nanoseconds after the rising edge of EN0, an internal MBC signal, DCUE1, is set to compete for memory service.

9. MEMORY STORAGE UNIT ORGANIZATION

The Model 80 Main Memory System uses 1,024 bit dynamic MOS memory devices (chips) as storage elements. Each MSU board contains 128 MOS chips (8 chips/bit) with their drivers and sense-digit circuits to provide 8,192 words by 16 bits (with optional Parity the chip count is 136). The 128 memory storage devices on an MSU board are divided into two separately addressed memory sections, each 4,096 words of 16 bits (4 chips/bit). These memory sections are designated A and B, (Address Busses A and B), with the A half of memory having the even address (i.e., A14 = 0), and B half of memory having the odd address (i.e., A14 = 1). The two memory sections (A and B) share the common 16 sense-digit and write-digit circuits on the same MSU board. Refer to Figure 4 for a simplified block diagram and reasonablly accurate physical layout of the actual MSU board. All signals to and from the MSU boards are sent to or from the MBC via Connectors 2 and 3. Back panel Connectors 0 and 1 are used for power and ground only. To initiate a memory cycle, the MSU receives a Start signal (A or B), Address, Data, and a Read/Write signal, as required. The MSU responds by returning an end of cycle pulse to the MBC along with data if a read has been performed. Other signals relating to Fetch and Refresh operations are discussed in their respective sections.

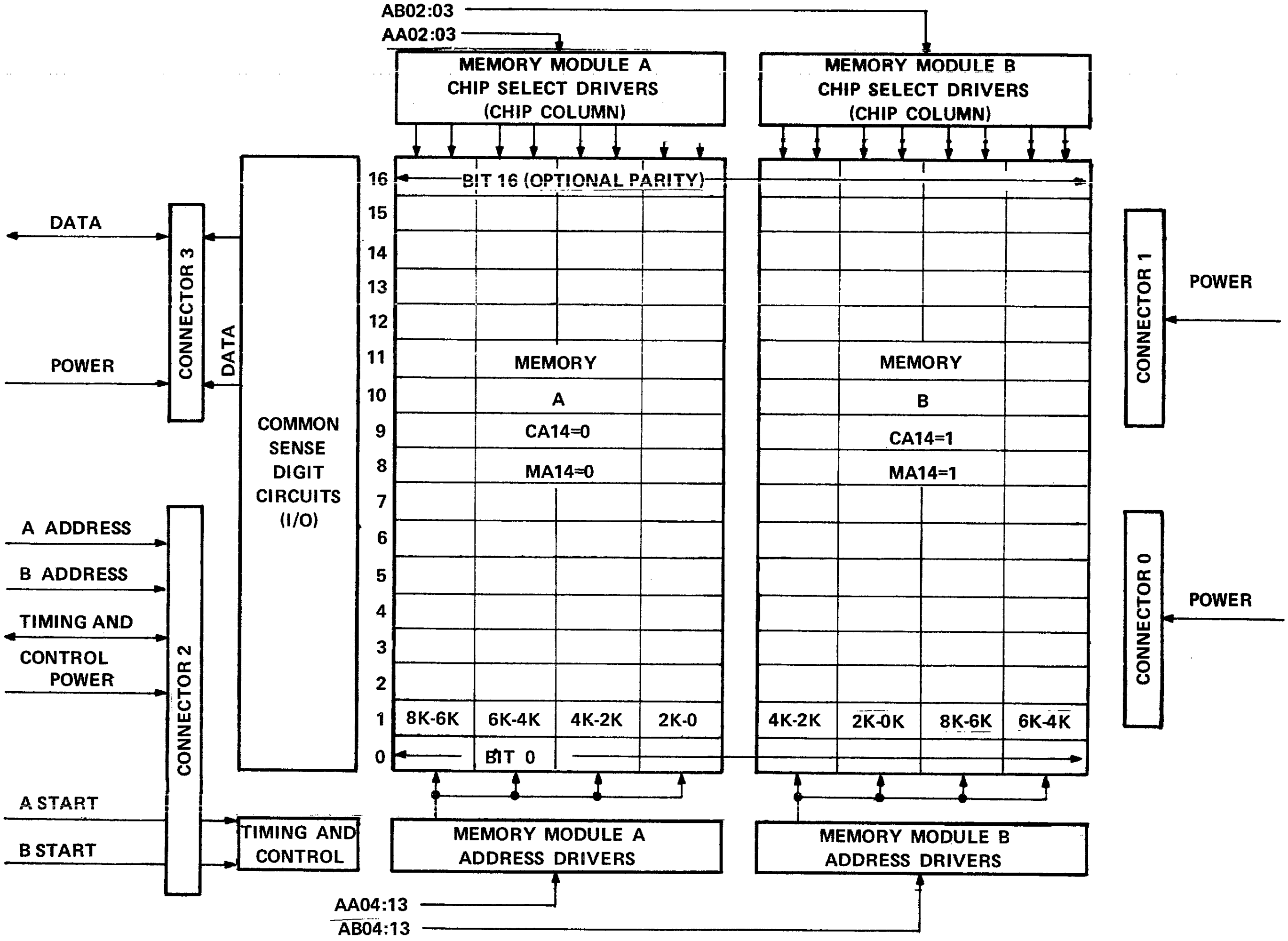

AB02:03
AA02:03
MEMORY MODULE A CHIP SELECT DRIVERS (CHIP COLUMN)
MEMORY MODULE B CHIP SELECT DRIVERS (CHIP COLUMN)
DATA
CONNECTOR 3
POWER
DATA
COMMON SENSE DIGIT CIRCUITS (I/O)
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
BIT 16 (OPTIONAL PARITY)
MEMORY
A
CA14=0
MA14=0
MEMORY
B
CA14=1
MA14=1
8K-6K
6K-4K
4K-2K
2K-0
4K-2K
2K-0K
8K-6K
6K-4K
BIT 0
CONNECTOR 1
POWER
CONNECTOR 0
POWER
A ADDRESS
B ADDRESS
TIMING AND CONTROL
POWER
CONNECTOR 2
A START
B START
TIMING AND CONTROL
MEMORY MODULE A ADDRESS DRIVERS
MEMORY MODULE B ADDRESS DRIVERS
AA04:13
AB04:13

Figure 4. Memory Storage Unit (MSU)

9.1 Address Bit Significance - MBC/MSU (Bits 00:14)

All address information is received by the MSU over the 50 conductor cable MBC-R at MSU Connector 2. The address bit significance is:

Bit 14	Address Bit 14 selects the A or B half of an MSU. Bit 14 is not received as such by the MSU but causes the generation of A or B START signals at the MBC. If address Bit 14 = 0, an A START is generated. If Bit 14 = 1, a B START is generated. See Table 2.
Bits 00 and 01	Address Bits 00 and 01 select one of four possible MSU boards (a 64 KB system would have four MSUs - 16 KB/MSU). These two bits are not received as such by the MSU but are decoded into one of four possible A STARTS or one of four possible B STARTS depending on the state of Bit 14. Decoding is done at the MBC. See Table 2. Each of the eight START signals is assigned a separate line in the ribbon cable (MBC-R). Every MSU is capable of receiving every START signal, however, the cable connects only the appropriate START signals (one A and one B) to each MSU.
Bits 02 and 03	These two address bits are received by both the A half and the B half of the MSUs as four separate signals (AA02 and AA03 to A half, and AB02 and AB03 to B half). These bits select either one of four A chip columns or one of four B chip columns for the 16 data bits. These address bits are decoded with timing to generate "Chip Select" signals.
Bits 04:13	These ten address bits are received by both the A half and the B half of the MSUs as twenty separate signals (AA04:AA13 to the A half and AB04:AB13 to the B half). Address Bits 04:13 are gated directly to the MOS chips through level shifters to perform a 1 of 1,024 select for all 16 data bits in the selected chip column. Decoding of these address bits is internal to the MOS chips.

Table 2. MSU/Memory (A or B) Select

ADDRESS BITS			START SIGNAL MBC OUTPUT TO MSU'S	MBC/MSU INTERFACE		MSU *	MEMORY
00	01	14		MBC	MSU		
0	0	0	STRA00	214-3	214-2	0	A
		1	STRB00	216-3	216-2		B
0	1	0	STRA10	114-3	114-2	1	A
		1	STRB10	116-3	116-2		B
1	0	0	STRA20	217-3	213-2	2	A
		1	STRB20	213-3	217-2		B
1	1	0	STRA30	113-3	113-2	3	A
		1	STRB30	117-3	117-2		B

*** THE MSU BOARDS ARE REFERENCED TO THE M BC.**

9.2 MSU/MBC Data Path

The memory handles 16 bits of data (17 with parity) each memory operation. All data to or from the MSUs communicates over the 16 Data Lines (DL00:DL15). These lines exist as part of the 50 conductor cable MBC-L.

10. MBC/MSU INTERFACE SIGNALS

The MBC/MSU Interface consists of 56 signal lines; 24 Address Lines, 17 Bi-directional Data Lines, 12 Control Lines, 2 Status Lines, and 1 Initialize Line. Other MBC/MSU interface lines carry voltages which are discussed in other sections of this specification. Refer to Figure 5.

The signal lines in the MBC/MSU interface are:

Address Lines	AA02:13	MBC ⟶ MSU	12 Lines
	AB02:13	⟶	12 Lines
Data Lines	DL00:16	⇄	17 Lines

Control Lines	STRA00:30	→	4 Lines
	STRB00:30	→	4 Lines
	MWRT0A	→	1 Line
	SROB	→	1 Line
	FAD0	→	1 Line
	GR1	→	1 Line
Status Lines	ENDCYL0	←	1 Line
	FECLK0	←	1 Line
Initialize Line	MRST0A	←	1 Line

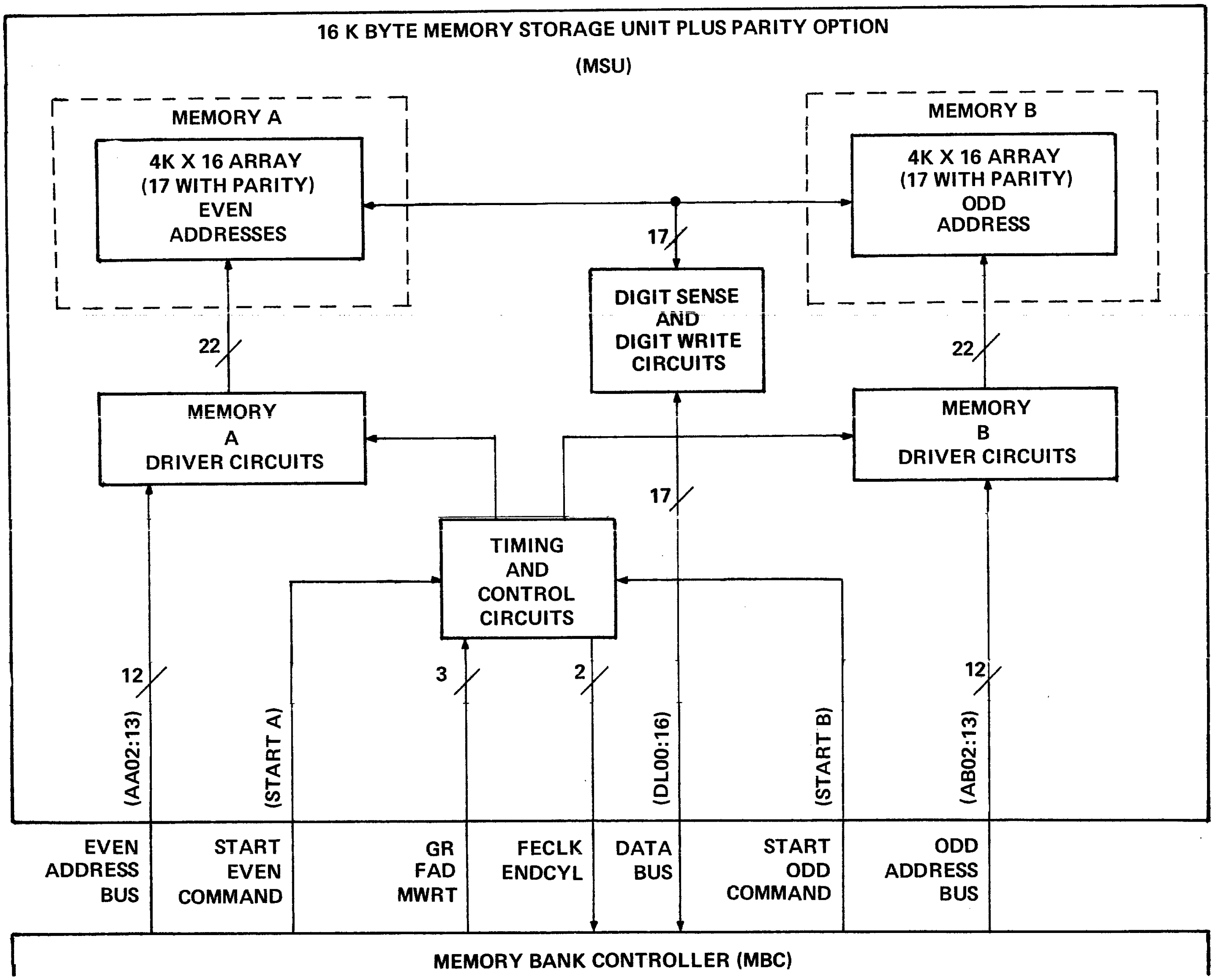

16 K BYTE MEMORY STORAGE UNIT PLUS PARITY OPTION
(MSU)
MEMORY A
4K X 16 ARRAY
(17 WITH PARITY)
EVEN
ADDRESSES
MEMORY B
4K X 16 ARRAY
(17 WITH PARITY)
ODD
ADDRESS
17
DIGIT SENSE
AND
DIGIT WRITE
CIRCUITS
22
22
MEMORY
A
DRIVER CIRCUITS
MEMORY
B
DRIVER CIRCUITS
17
TIMING
AND
CONTROL
CIRCUITS
12
3
2
12
(AA02:13)
(START A)
(DL00:16)
(START B)
(AB02:13)
EVEN
ADDRESS
BUS
START
EVEN
COMMAND
GR
FAD
MWRT
FECLK
ENDCYL
DATA
BUS
START
ODD
COMMAND
ODD
ADDRESS
BUS
MEMORY BANK CONTROLLER (MBC)

Figure 5. Memory Storage Unit, Block Diagram

Address Lines AA02:13 and AB02:13

As soon as the MBC honors a request from the DMA or CPU Port, the 15 bit address at the port being honored is loaded into the two 14 Bit Address Registers A and B (Address Bit 14 is treated differently). Twelve outputs from the A Address Register (AA02:13) and twelve outputs from the B Address Register (AB02:13) are output directly to the MSUs.

Data Lines DL00:16

Data Lines DL00:16 are actually lines which connect the "0" outputs from the MBC Data Register to the MSUs. On a Read cycle, the readout data is pulsed over these lines from the selected MSU to the MBC Data Register. The Data Register had been reset earlier in the Read cycle. On a Write cycle, the data to be written is transmitted over Data Lines DL00:16 from the MBC Data Register to the selected MSU Write Data circuits.

STRA0:3 and STRB0:3

As soon as the MBC honors a request from the CPU or DMA Port, it sets the address from the honored port into both MBC Address Registers (A and B). One of eight possible start signals is then generated and sent to the MSU that is to be selected. The start signal generated is decoded from Address Bits 00, 01 and 14 according to Table 2. The start signal is received by the MSU and triggers the MSU timing sequence which performs the desired memory cycle.

MWRT0A

When the MBC initiates a memory cycle, it sets into a flip-flop the condition on the honored ports Read/Write Line (CWRT0 for the CPU or WRT0A for the DMA port). The MWRT0A signal is derived from the flip-flop and sent to the MSU where it directs the initiated cycle to be a Read or a Write.

SROB

Select Refresh (SROB) is generated by the MBC only during Refresh cycles and sent to all MSUs where it enables all chip select signals. This allows all MOS memory chips to undergo a Refresh cycle simultaneously.

FAD0

Fetch Address (FAD0) is generated by the MBC on Instruction Fetch operations only. FAD0 directs the selected MSU to gate the second Read cycle address and Reset turn off to the MOS memory chips.

GR1

Gate Reset (GR1) is inactive only during intervals between Refresh cycles in the Standby Mode. GR1 is a constant high during the Normal Mode.

ENDCYL0

End Cycle (ENDCYL0) is generated by the MSU at the end of its timing sequence for all memory operations; Read, Write, and Refresh cycles. The ENDCYL0 signal is approximately coincident with the readout on the Data Lines (DL00:15) if the memory operation is a Read. An Instruction Fetch operation produces two ENDCYL0 signals spaced by 150 nanoseconds.

FECLK0

Fetch Clock (FECLK0) is generated by the selected MSU. Although this signal is generated by all types of memory cycles, it is only required by Instruction Fetch operations. FECLK0 tells the MBC when it may send the second START in a Fetch operation. The leading edge typically follows the leading edge of the Start signal (STRA00:30 or STRB00:30) by 130 nanoseconds.

MRST0A

Memory Reset (MRST0A) is generated by the MBC and sent to the MSU. MRST0A is a low signal whenever P5S is less than 4 volts and a high signal whenever P5S is greater than 5 volts. Its function is to guarantee that the drivers of the MSU MOS memory chips do not turn on inadvertantly during the time P5S is switching on or off in the Standby Mode.

11. MEMORY BANK CONTROLLER (MBC) BLOCK DIAGRAM ANALYSIS

The MBC controls access to the Memory Storage Units (MSUs) from the two independent busses (CPU and DMA) and the internal MBC refresh generator. When the MBC recognizes a CPU or DMA memory request, it relays data and/or address and control information from the requesting bus to the selected MSU in the main memory system. When the internal Refresh request is recognized, the MBC causes all MSU boards to perform a Refresh cycle simultaneously. The MBC also contains Memory Protect circuits, which are controlled by a Memory Protect Controller (MPC) (optional-separate board), the Parity Bit Generation/Check circuit, an eight volt regulator (P8), and a 24 volt regulator (P24).

11.1 MBC Block Diagram

The Model 80 Memory System (MBC and MSU) can be considered idle (performing no functions) until one of three Request signals is generated; CPU Request (CREQ0), DMA Request (REQ0), or the MBC internally generated Refresh Request (RREQ1).

The memory system responds to these three requests by performing a memory cycle. The memory system, in processing any of the three types of requests, must do the following key control functions (Refer to Figure 6).

1. Accept three asynchronous request signals and assign memory service according to a priority scheme wired into the MBC logic. This function is performed by the MBC Interlock circuit.
2. Load Data and/or Address and Control information into the MBC Registers from the selected port.
3. The MBC then generates and sends the appropriate Start signals (STRA00:30-STRB00:30) to the MSUs.
4. The MBC then waits for the MSU to perform the cycle and respond with an End of Cycle pulse (ENDCYL0). Data is returned to the MBC simultaneously with the ENDCYL0 pulse when the cycle is a Read.
5. The MBC, as a result of receiving the ENDCYL0 pulse, generates the END0 signals (END0, END0A, END0B, END0C, etc.) which it uses to clear itself before initiating the next cycle.
6. If the signal ENDCYL0 is caused by a Read cycle, it also causes the MBC to output data on the appropriate bus.
7. If the cycle performed is for CPU or DMA, the MBC must generate and return the CRDY0 signal to the CPU or the INH0 signal to the DMA Channel to signify the completion of a Write or that the requested data is ready on the appropriate bus.

The following paragraphs describe each functional block of Figure 6. Each block includes the sheet number of the schematic sheet pertaining to the function.

11.2 Bank Select (Figure 6)

Bank Select circuit description is beyond the scope of this manual. The circuit description in this manual always assumes that the Bank Select circuits are enabled. Therefore, consider the Bank Select function merely as an Inverter for the Request signal (CREQ0). The DMA Bank Select function can be ignored completely.

11.3 Acknowledge Request

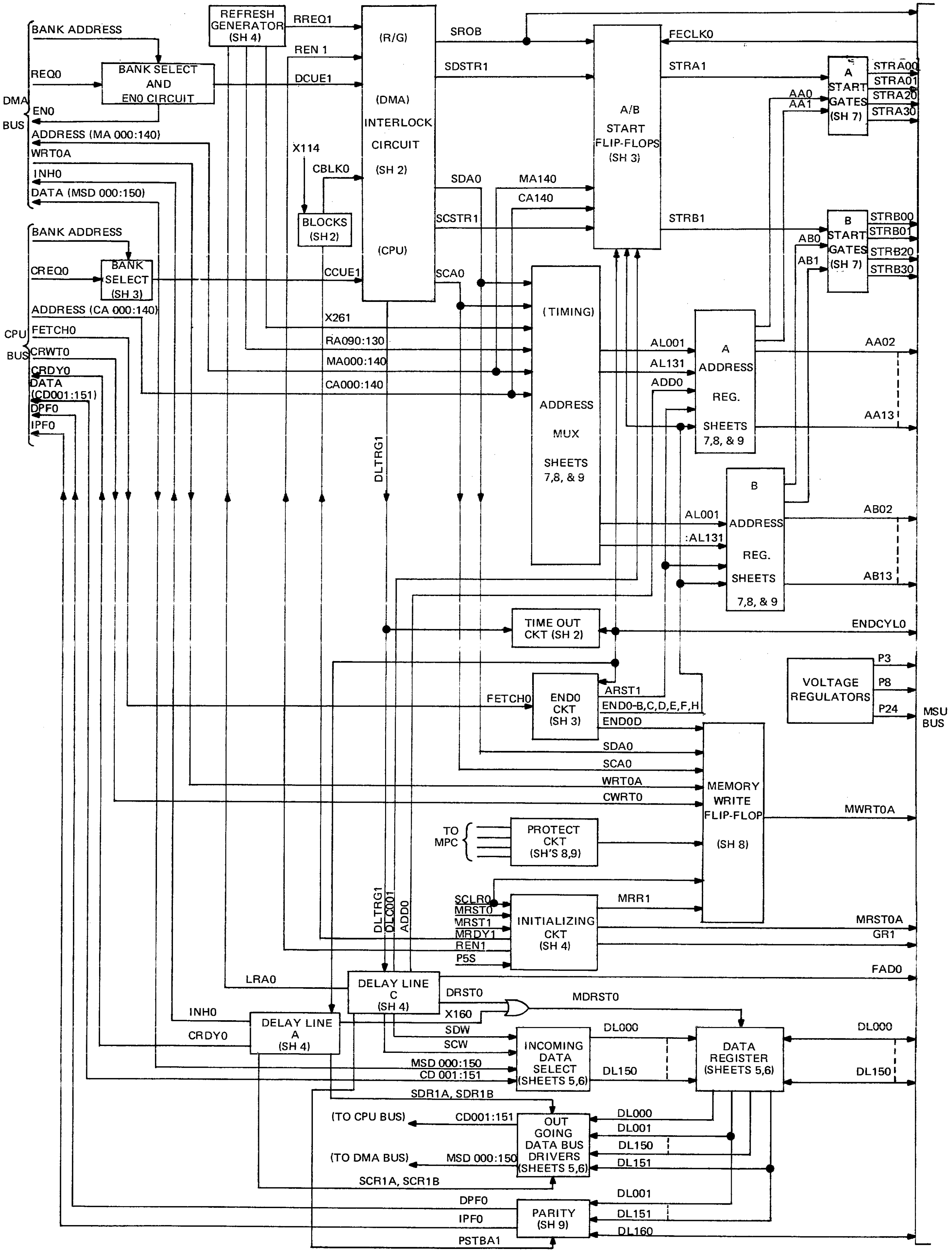
When the Acknowledge Request functional block receives a DMA Request, (REQ0), it returns an Enable signal, (EN0), to the party line DMA Bus. The rising edge of the EN0 signal signifies when the requesting party on the DMA Bus is to send Data and/or Address and Read/Write information. The DQUE1 signal is generated about 100 nanoseconds after EN0 rises and is input to the Interlock circuit.

11.4 Refresh Generator

Refresh cycles must be performed at 32 different address combinations; that is, all combinations of Address Bits AA09:13 and AB09:13. The condition of Address Bits AA00:08, AB00:08, AA14, and AB14 have no bearing on the Refresh function.

In the Normal Mode, Refresh cycles are dispersed evenly in time producing a refresh cycle at a given address combination every 2 milliseconds or less.

In the Normal Mode, the refresh generator presents a Refresh Request (RREQ1) to the Interlock circuit approximately every 50 microseconds (32 x 50 microseconds $\leq$ 2 milliseconds). The refresh generator includes a five bit address counter which is loaded into the MBC A and B Address Registers (AA09:13 and AB09:13). The loading does not take place until the Interlock circuit has responded to the Refresh Request by initiating a Refresh cycle. After the address is loaded, the refresh generator's five bit counter is incremented for the next cycle.



BANK ADDRESS
REQ0
DMA BUS
EN0
ADDRESS (MA 000:140)
WRT0A
INH0
DATA (MSD 000:150)
BANK SELECT AND EN0 CIRCUIT
REFRESH GENERATOR (SH 4)
RREQ1
REN 1
DCUE1
X114
CBLK0
BLOCKS (SH 2)
(R/G) (DMA) INTERLOCK CIRCUIT (SH 2) (CPU)
SROB
SDSTR1
FECLK0
STRA1
A/B START FLIP-FLOPS (SH 3)
A START GATES (SH 7)
STRA00
STRA01
STRA20
STRA30
AA0
AA1
SDA0
MA140
CA140
SCSTR1
STRB1
B START GATES (SH 7)
STRB00
STRB01
STRB20
STRB30
AB0
AB1
BANK ADDRESS
CREQ0
BANK SELECT (SH 3)
CCUE1
SCA0
ADDRESS (CA 000:140)
CPU BUS
FETCH0
CRWT0
CRDY0
DATA (CD001:151)
DPF0
IPF0
X261
RA090:130
MA000:140
CA000:140
(TIMING) ADDRESS MUX SHEETS 7,8, & 9
AL001
AL131
ADD0
A ADDRESS REG. SHEETS 7,8, & 9
AA02
AA13
DLTRG1
AL001
:AL131
B ADDRESS REG. SHEETS 7,8, & 9
AB02
AB13
TIME OUT CKT (SH 2)
ENDCYL0
VOLTAGE REGULATORS
P3
P8
P24
MSU BUS
FETCH0
END0 CKT (SH 3)
ARST1
END0-B,C,D,E,F,H
END0D
SDA0
SCA0
WRT0A
CWRT0
MEMORY WRITE FLIP-FLOP (SH 8)
MWRT0A
TO MPC
PROTECT CKT (SH'S 8,9)
DLTRG1
DLC001
ADD0
SCLR0
MRST0
MRST1
MRDY1
REN1
P5S
INITIALIZING CKT (SH 4)
MRR1
MRST0A
GR1
FAD0
LRA0
DELAY LINE C (SH 4)
DRST0
MDRST0
X160
INH0
CRDY0
DELAY LINE A (SH 4)
SDW
SCW
MSD 000:150
CD 001:151
INCOMING DATA SELECT (SHEETS 5,6)
DL000
DL150
DATA REGISTER (SHEETS 5,6)
DL000
DL150
SDR1A, SDR1B
(TO CPU BUS)
CD001:151
(TO DMA BUS)
MSD 000:150
OUT GOING DATA BUS DRIVERS (SHEETS 5,6)
DL000
DL001
DL150
DL151
SCR1A, SCR1B
DPF0
IPF0
PSTBA1
PARITY (SH 9)
DL001
DL151
DL160

Figure 6. Memory Bank Controller Functional Block Diagram

11.5 Interlock Circuit

The Interlock circuit receives the three Request signals (REQ1, DCUE1, and CCUE1) and assigns memory cycles to the requesting port according to a priority scheme wired into the Interlock logic. Assuming no contention, the Interlock circuit responds to request signals as follows:

1. If a CPU Request (CCUE1) is input to the Interlock circuit, the Interlock outputs DLTRG1, SCSTR1, and SCA1. Delay Line Trigger (DLTRG1) causes Delay Line "C" to output timing used to generate control signals required early in the memory cycle. The Select CPU signal (SCSTR1) is active for the entire CPU cycle and is used to generate other signals associated with the CPU cycles. The Select CPU Address signal (SCA1) loads the CPU Address Bus (CA00:15), FETCH0 and MWRT0, into the appropriate MBC Register.

2. If a DMA request (DQUE1) is input to the Interlock circuit, the Interlock outputs (DLTRG1, SDSTR1, and SDA1). Delay Line Trigger (DLTRG1) causes Delay Line "C" to output timing used to generate control signals required early in the initiated memory cycle. The Select DMA signal (SDSTR1) is active for the entire DMA cycle and is used to generate other signals associated with the DMA cycle. The Select DMA Address signal (SDA1) loads the DMA Address Bus (MSD00: 15), and the Read/Write signal (WRT0A) into the appropriate MBC registers.

3. If a Refresh Request (RREQ1) is input to the Interlock circuit, the Interlock outputs DLTRG1 and SROB. Delay Line Trigger (DLTRG1) causes Delay Line "C" to output timing used to generate control signals required early in the initiated Refresh cycle. The Select Refresh signal SROB is active for the entire Refresh cycle and is used to enable other signals associated with Refresh cycles.

11.6 A/B START

The A/B Start circuit is merely two flip-flops (A Start and B Start) with associated set and reset logic. This circuit determines if an A Start signal (STRA00:30) or a B Start signal (STRB00:30) is to be sent to the selected MSU. Early in the DMA or CPU Read or Write cycle, the condition of the requesting bus's Address Bit 14 and timing from the DLC Delay Line sets one of the Start flip-flops. Resetting is done by END0 at the end of the cycle.

On a Fetch cycle, both A and B Start flip-flops are set, however, the setting is staggered by 150 nanoseconds. The flip-flop set first (may be either A or B) is set as in a CPU Read or Write cycle. When the first End of Cycle signal (ENDCYL0) is returned to the MBC by the selected MSU, it is inverted and ANDed with the CA14 register to reset the Start flip-flop set first. However, before the first ENDCYL0, a timing signal (FECLK0) is returned by the MSU which is used to set the second Start flip-flop. When the second ENDCYL0 is returned by the selected MSU, the END0 signals are generated and cause the resetting of the second Start flip-flop.

On a Refresh cycle, both Start flip-flops are set and reset simultaneously. A timing signal from the DLC Delay Line and SROB inverted are ANDed to generate the set pulse (applied to both A and B flip-flops). The resetting is performed by END0 which is generated from the Refresh cycles ENDCYL0 signal.

11.7 A/B Start Gates

Eight three-input gates decode the address and A/B Start flip-flops to generate a Start signal (STRA00:30 or STRB00:30). When a Read or Write cycle is initiated one of these eight signals select an MSU and start the requested memory cycle. When a Refresh cycle is initiated, all eight start signals go active simultaneously.

11.8 Address MUX

The address MUX circuits set the Address Bus of both MBC Address Registers (A and B) from the requesting port. The LRA1, SCA1, and SDA1 pulses set the address for the Refresh, CPU, or DMA cycles respectively.

11.9 A/B Address Registers

The requesting port Address Bus is registered by the A and B Address Registers. The A Address Registers also functions as a counter in Fetch cycles if the first start is a B Start. The ADD0 signal causes the A Address Register to increment. ADD0 is generated early in the Fetch cycle by timing from the DLC delay line if the Address of the Fetch operation had CA14 set.

11.10 Time-Out Circuit

If a request is made for a memory cycle to an address for which no MSU is equipped, the MBC sends out the appropriate Start signal but no ENDCYL0 is returned. This condition would lock up memory indefinitely were it not for the Time-Out circuit. The Time-Out circuit generates an ENDCYL0 if the width of DLTRG1 exceeds approximately 800 nanoseconds which is longer than any normal cycle. The locally generated ENDCYL0 allows the MBC to abort the cycle by returning CRDY0 or INH0. No flag signal is generated to signify to the requesting port that the cycle is aborted. However, if the aborted cycle is a Read, all zeros data are returned.

11.11 END0 Circuits

This circuit receives End of Cycle pulses (ENDCYL0) from the accessed MSU and generates the END0 signals which are used to terminate all memory cycles at the MBC. It is important to observe that the first ENDCYL0 of a Fetch operation does not generate the END0 signals. The END0 signals include END0, END1, END0A, END0B, END0C, END0D, END0E, END0F, END0G, END0H, END0J, and ARST1.

On a Refresh cycle, ARST1 and SROB are active at the A and B Address Registers for the entire Refresh cycle forcing Address signals AA000, AA001, AB000, and AB001 all high which enables all Start signals (STRA00:30 and STRB00:30).

11.12 Memory Write Flip-Flop

The Memory Write flip-flop registers WRT0A or CWRT0 from the serviced port. Its outputs are used to enable or inhibit signals associated with Read or Write operations.

11.13 Protect Circuit (Optional Feature)

The Protect Circuit, when enabled, converts protected address locations from being written into. It does this by checking the contents of a 4 x 16 bit register. Every memory address has assigned to it a bit in the 4 x 16 bit register. On Memory Write cycles, the bit assigned to the location being accessed is examined and, if set, cause the Memory Write flip-flop to be reset, converting the intended Write to a Read operation.

11.14 Initializing Circuit

The Initializing circuit generates the Initializing signals MRST0, MRST1, MRDY1, and MRR1. Generally, MRST0 and MRST1 initialize circuits associated with the refresh operation as P5S cycles on and off in the Standby Mode. Memory Ready signals, MRDY1 and MRR1, inhibit circuits associated with normal operation during Standby Mode.

11.15 Delay Line C

Every time a memory cycle is initiated, Delay Line C is activated by Delay Line Trigger (DLTRG1). Delay Line C produces timing signals required at the beginning of memory cycles.

11.16 Delay Line A

Every time data is returned to the MBC from the selected MSU on a Read cycle, End of Cycle (ENDCYL0) causes Delay Line A to activate. Delay Line A produces the timing required to send the data to the requesting port. On a CPU Read or Fetch operation, it times the generation of CRDY0, CD00:15, Parity check (PSTBA1), and Memory Data Register Reset (MDRST0). A Memory Data Register Reset (MDRST0) is required following the first readout of a Fetch operation to clear the register for the second readout which follows.

11.17 Incoming Data Select

On a Write operation, Delay Line C causes generation of Select DMA Write (SDW1A/B) or Select CPU Write (SCW1A/B). These pulses load the appropriate data bus, (MSD00:15 or CD00:15) into the MBC Data Register.

11.18 Data Register

On CPU or DMA Write cycles, the MBC Data Register is first reset by MDRST0, then set by the Select CPU Write (SCW1A/B) or Select DMA Write (SDW1A/B) signals. The Data Register outputs to the MSUs.

On CPU or DMA Reads, the MBC Data Register is first reset by timing from Delay Line C, then set by pulses from the selected MSU readout circuits via the Data Lines (DL000:150).

11.19 Outgoing Data Bus Drivers

On DMA or CPU Read operations, data is sent out over the requesting port's data bus. Timing from Delay Line A produces the enabling signals SDR1A/B (DMA) or SCSTR1A/B (CPU).

11.20 Parity (Optional Feature)

On DMA or CPU Write operations, the Parity Bit is computed and sent to the selected MSU via DL160. On DMA or CPU Read operations, the Parity Bit is read and checked and, if a failure is detected, Data Parity Fail (DPF0) goes active for approximately 40 nanoseconds. Detected Parity Failures on either the first or second half of a CPU Fetch operation causes the Instruction Parity Fail signal (IPF0) to go active for 40 nanoseconds.

12. VOLTAGE REGULATORS

Three voltages are generated on the MBC for use by the MSU - P3, P8, and P24. In the Standby Mode, P8 and P24 maintain their regulated outputs but the P3 generator rises to approximately 8 volts.

12.1 P24 Regulator

The P24 regulator is generated by a multivibrator switching one side of a capacitor between ground and P21. The other side of the capacitor is rectified and shunt regulated to a nominal 23.8 volts. The current capability of the P24 Regulator is limited to approximately 4 milliamperes. This regulator must function in both Standby Mode and Normal Mode.

12.2 P8 Regulator

The P8 regulator is a current sinking regulator and is nominally adjusted to 7.85 volts. This regulator must function in both Standby Mode and Normal Mode.

12.3 P3 Regulator

The P3 Regulator is a string of voltage dropping diodes to ground which are disconnected from ground in the Standby Mode. P3 measures approximately 2.7 volts in the Normal Mode and between 7 volts and 8 volts in the Standby Mode.

13. MBC DETAILED FUNCTIONAL AND TIMING DESCRIPTIONS

This section describes, in detail, all times of memory operations referencing Functional Schematics (35-407D08) and timing diagrams. It is recommended that the more general sections (1 through 11) be read first. In the following descriptions, assume only one request at a time.

13.1 CPU Memory Write (Figure 7)

At the beginning of a CPU Memory Write operation, the CPU Request signal (CREQ0) (3A3) is inverted and output as CCUE1 (3E2). CCUE1 (2E9), input to the interlock circuit (Sheet 2), toggles set the CPU Request flip-flop (2H6). The flip-flop output lead, Select CPU Address Request signal (SCAR1) (2J5), pulses the select CPU Address signal (SCA1) high. SCA1 gates the CPU address on CPU Address Lines CA000:130 (Sheets 7, 8, and 9) into the A and B Address Registers. The End Address signal (ENDST0) (3H4) goes low-active approximately 30 nanoseconds after SCA1 is pulsed high, terminating the SCA1 signal. SCAR1 (2J5) and the Memory Ready signal (MRDY1-normally high) (2L6) enable the Select CPU Start signal (SCSTR0) (2L6) which activates Delay Line C Trigger (DLTRG1) (2N3) and SCSTR1A/B (2N6). DLTRG1 starts the 100 nanoseconds delay line (4B2) and the time-out circuit (3G2) which generates an End of Cycle signal if none is received from an MSU. With DLC001 and SCA1A high, the state of CPU Address Bit 14 (CA 140) (3A6) determines if Start A flip-flop (STRA1) (3E5) or Start B flip-flop (STRB1) (3E6) is enabled. The Address Bits 0 and 1 (AA00:01 or AB00:01) (Sheet 7) are ANDed with STRA1 or STRB1 to select one of four MSU boards and the half of memory to be accessed by generating one of the eight starts, STRA00:30/STRB00:30. The remaining address bits (AA020:130 or AB020:130) are output to the selected MSU. DLC001 (4F2) and DLC060 (high) pulses Data Reset (DRST0) low, which in turn pulses Memory Data Reset (MDRST0) low, resetting the 16 data line registers (Sheets 5 and 6) and the Parity Bit latch (9K5).

In a Memory Write operation, the CPU Write (CWRT0) (8F8) is active the same time as CREQ0 (3A3). CWRT0 and SCA1B (8H8) sets the memory write latch (8L8). An active output from the memory write latch enables the Memory Write signal (MWRT0A) to the MSU and the MBC Parity circuit (Sheet 9). SCSTR1A (4H3), MWRT1 (4E3), and DLC001 (4A4) enable the Select CPU Write signals (SCW1A/B) (4H3). SCW1A/B loads the 16 data bits from the CPU Data Lines CD000:151 onto the MBC Data Register. The data register outputs are also input to the Parity Generation circuit (Sheet 9). SCW1B and DLC091 pulses CRDY0 (3M4) low. The CPU raises CWRT0 and CREQ0, terminating the cycle for the CPU. When the MSU has timed through the Write cycle it returns an End of Cycle signal (ENDCYL0) (2A2) to the MBC. ENDCYL0 causes the generation of the END0 signals by toggling 07H-01 (2F1). END0 resets the selected Start flip-flop (3E4). END0 B, C, D, E, F and H are also generated but do not become active until the Selected Start flip-flop is reset (3G6). The END0 signals clear the MBC (SCSTR1, AA or AB 000:130, DLTRG1, MWRT0, and STRA or STRB), for the following memory cycle. END0H fed back to 07H-15 (2F1) terminates the END0 signals.

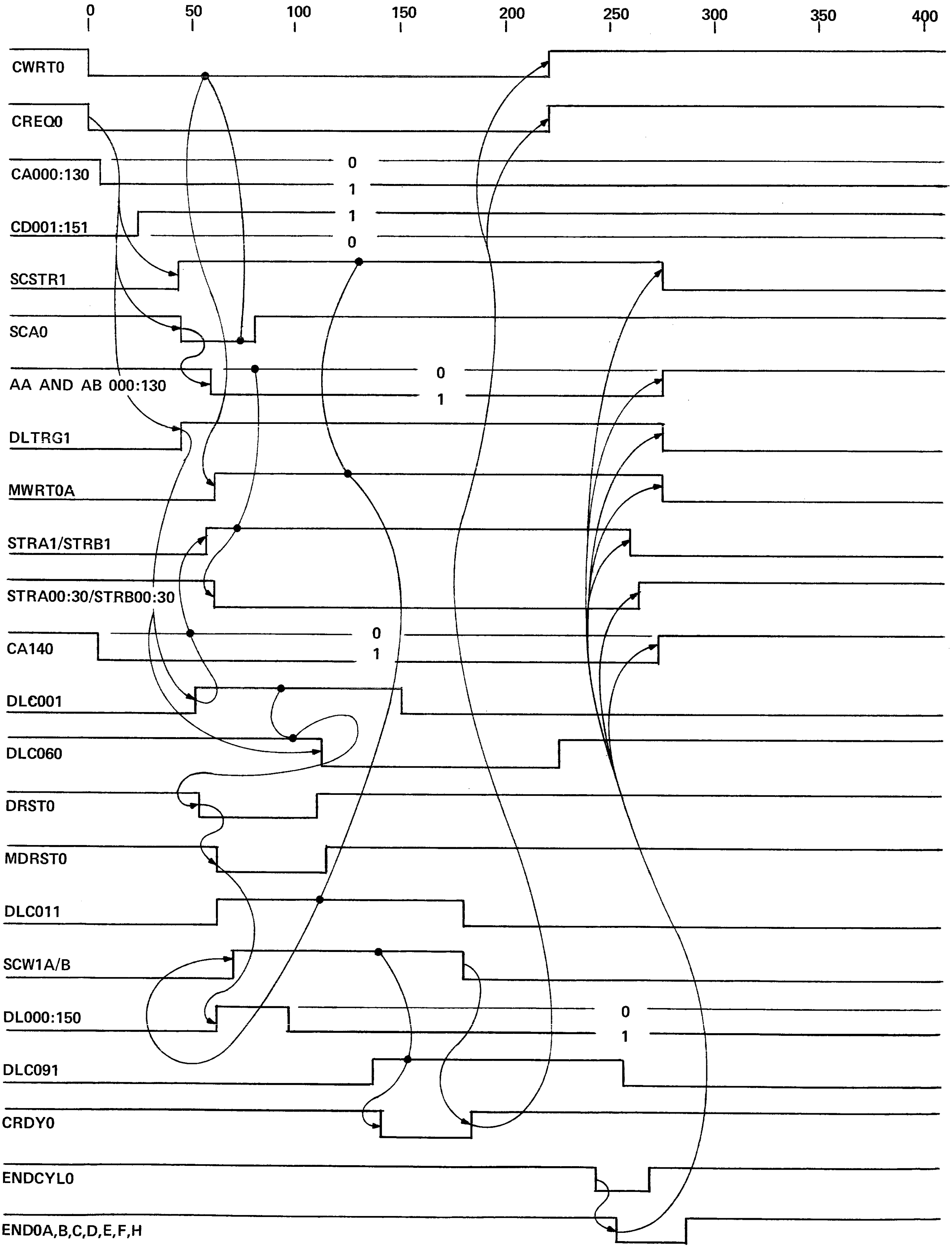

0
50
100
150
200
250
300
350
400
CWRT0
CREQ0
CA000:130
CD001:151
SCSTR1
SCA0
AA AND AB 000:130
DLTRG1
MWRT0A
STRA1/STRB1
STRA00:30/STRB00:30
CA140
DLC001
DLC060
DRST0
MDRST0
DLC011
SCW1A/B
DL000:150
DLC091
CRDY0
ENDCYL0
END0A,B,C,D,E,F,H
0
1
1
0
0
1
0
1
0
1

Figure 7. Central Processor Unit (CPU) Write Timing

13.2 CPU Memory Read (Figure 8)

In a CPU Memory Read operation, SCSTR1, SCA1, DLTRG1, MDRST0 and a start signal are generated as in a CPU Memory Write, the CPU Write signal (CWRT0) (8H8) is held high. The absence of a write signal to the MSU causes the MSU Strobe read signal (STRB1) to go high. STRB1A strobes the 16 sense digit circuits, enabling the 16 data bits to be read from the memory cells in the addressed chips. The MSUs strobe pulse gates the readout onto the corresponding Data Lines (DL00:15). The pulsed data lines set the readout into the MBC's Data Register. The MSU returns End of Cycle (ENDCYL0) (2A2) to the MBC. This indicates that the MSU has sent the requested data to the MBC. SCSTR1 and MWRT0 (high) are gated to provide a high to the input of the Read flip-flop (3K3). ENDCYL0 toggles the flip-flop set. The flip-flop's output, X163 low, is inverted to provide Select CPU Read signals (SCR1A/B) (3N9). These signals load the data on the 16-bi-directional data lines (DL000:150) (Sheets 5 and 6) onto the CPU Data Lines (CD000:151). The 16 data bits on DL000:150 are also sent to the parity circuit for even parity check. X163 low also starts Delay Line A DLA000 (50 nanoseconds) (4K2). DLA001 and DLA350 (high) pulses the CPU Ready signal (CRDY0) (3N4) low. The CPU raises the request signal. When DLA 501 goes high with DLA 201, it direct clears the Read flip-flop (3K4) raising the X163 signal, and hence terminates the gating of data to the CPU. X163 and DLA 201 (4N3) pulse X160 low, enabling the second Memory Data Reset signal (MDRST0). ENDCYL0 also enables END0, END0A, B, C, D, E, F, and H (3J7) which terminate the internal MBC control signals, SCSTR1, AA or AB 000:130, DLTRG1, and STRB1 or STRA1 as in a Write cycle.

13.3 CPU Instruction Fetch (Figure 9)

Depending on the state of CA14 either an A Start (STRA00:30) or a B Start (STRB00:30) is generated by the MBC as in a normal Read cycle. This first start selects an MSU which initiates the Read cycle. However, a second start must be generated approximately 150 nanoseconds after the first. The second start must read a memory address two greater than the address read by the first start. The address of the second Read cycle is computed by the MBC. When the first read of the Instruction Fetch is from an even address (A) (A14 = 0). The MBC merely generates the second start by setting the B Start flip-flop at the appropriate time. This produces a Read cycle at the proper address. However, if the first Read cycle is an odd address (B) (A14 = 1) the second start - an A Start - cannot be generated unless two is added to the MBC A Address Register. This addition when required is performed by ADD0 (3D8).

During an Instruction Fetch cycle, a fetch address is generated by the MBC and sent to the MSU. Its function is to gate the second read address to its corresponding half of memory. If the second read address gating were as in a normal read, timing of the switching addresses would cause noise in the first readout. FAD0 Gates the second read address earlier to reduce the noise during the first readout. A complete Instruction Fetch cycle is described as follows: Assume the address is odd (CA14 = 1).

A CPU Instruction Fetch activates the CPU Request signal (CREQ0) (3A3) and the CPU Fetch signal (CFTCH0) (2A2). The CREQ0 signal is inverted and output as CCUE1 (3F2). CCUE1 (2D9), input to the Interlock circuit (Sheet 2), toggles set the CPU request flip-flop (2F6). The flip-flop output generates the SCA1A/B signals which sets the CPU Address Lines (CA 000:130) (Sheets 7, 8 and 9) into the A and B Address Registers. SCA1 is also ANDed with CFTCH1 (2C2) to set FETCH1 (2E3).

The End Address signal (ENDST0) (3H4) goes low-active approximately 30 nanoseconds after SCA0 is pulsed low, terminating the SCA0 signal. SCAR1 (2J5) and the normally high Memory Ready signal (MRDY1) (2L6) enable the select CPU Start signal (SCSTR0) (2L6) which activates the Delay Line C Trigger (DLTRG1) (2N3), SCSTR1A/B (2N6), and the one shot timer (3G2) which generates an ENDCYL0 signal if one is not received from the MSU. When DLC001 goes high it sets the B latch by setting X264 low (3D6). The B Address Register Bits 0 and 1 are ANDed with STRB1 to generate a B Start signal (STRB00:30) (7G2) which selects one of the four MSU boards. The address bits (AB02:13) are output to the selected MSU.

DLC001 (4F2) and DLC006 (high) pulse Data Reset low (DRST0), which in turn pulses Memory Data Reset (MDRST0) (4N4) low, resetting the data registers (Sheets 5 and 6) and the Parity Bit latch (9K5).

DLC051, FETCH1 and A141 generate ADD0 which increments the A Address Register. At the same time FAD0 goes low due to the toggling of 07F-01 (3H8).

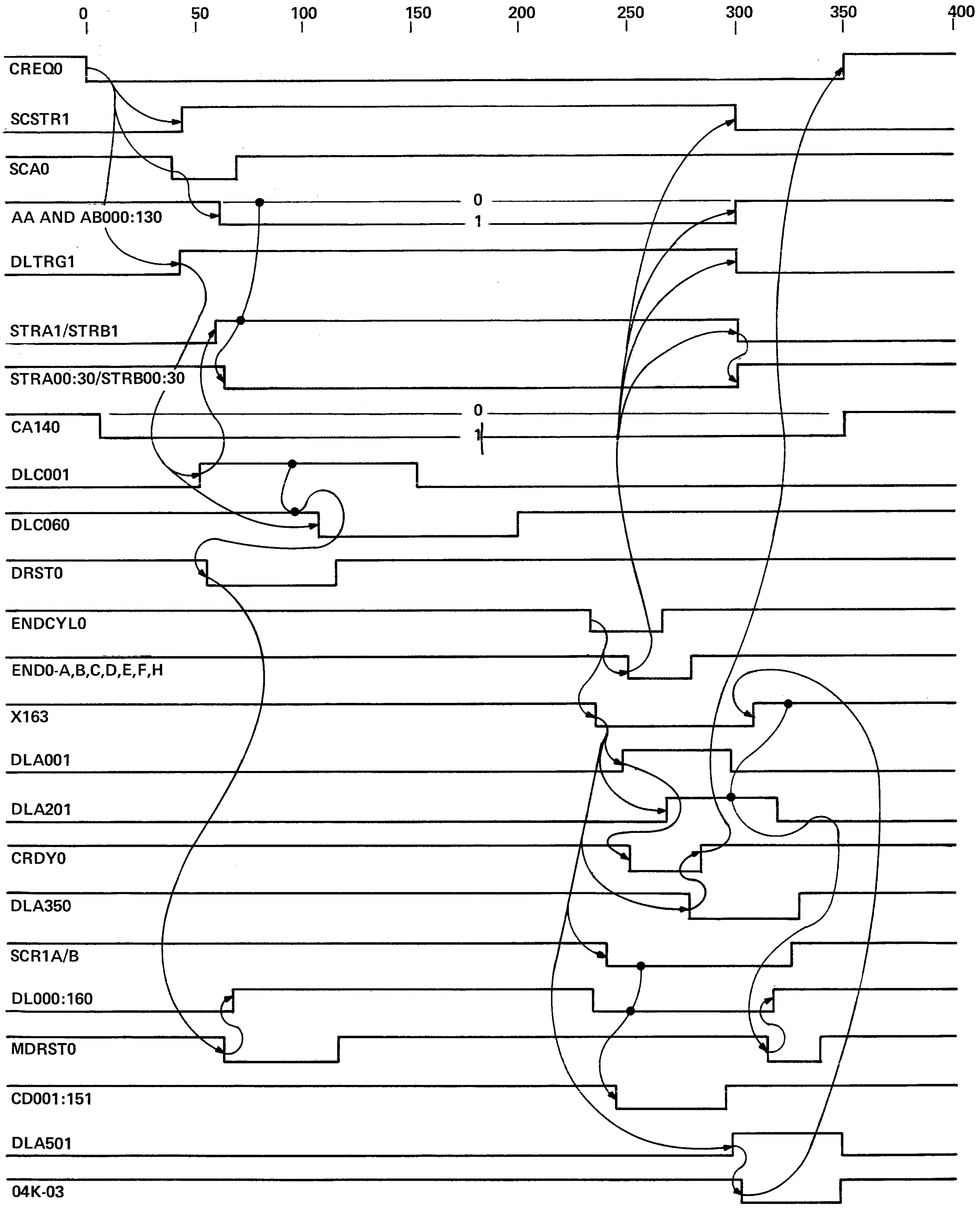

0
50
100
150
200
250
300
350
400
CREQ0
SCSTR1
SCA0
AA AND AB000:130
0
1
DLTRG1
STRA1/STRB1
STRA00:30/STRB00:30
CA140
0
1
DLC001
DLC060
DRST0
ENDCYL0
END0-A,B,C,D,E,F,H
X163
DLA001
DLA201
CRDY0
DLA350
SCR1A/B
DL000:160
MDRST0
CD001:151
DLA501
04K-03

Figure 8. Central Processing Unit (CPU) Read Timing

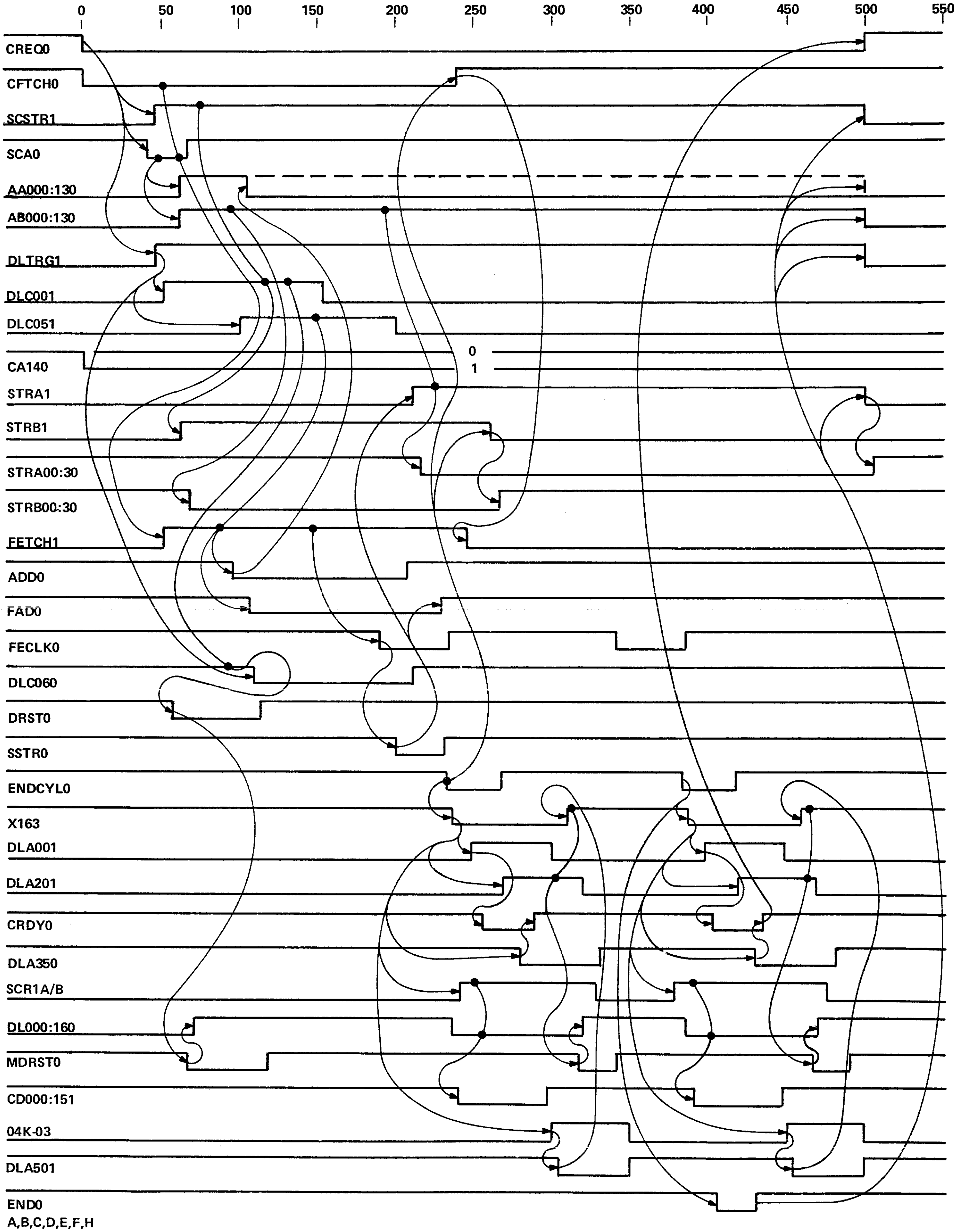

0
50
100
150
200
250
300
350
400
450
500
550
CREQ0
CFTCH0
SCSTR1
SCA0
AA000:130
AB000:130
DLTRG1
DLC001
DLC051
CA140
0
1
STRA1
STRB1
STRA00:30
STRB00:30
FETCH1
ADD0
FAD0
FECLK0
DLC060
DRST0
SSTR0
ENDCYL0
X163
DLA001
DLA201
CRDY0
DLA350
SCR1A/B
DL000:160
MDRST0
CD000:151
04K-03
DLA501
END0
A,B,C,D,E,F,H

Figure 9. CPU Instruction Fetch Timing (B Start)

The previous sequence of signals has started the first Read cycle. When Fetch Clock (FECLK0) goes low from the MSU, FETCH1 (2D3) and FECLK0 enable the Start Second cycle signal (SSTR0) (3J9). SSTR0 sets the A latch (3E4) enabling STRA1 and terminating FAD0 (3J8). STRA1 and the states of A Address Bits 0 and 1 generate the second start (A this time) which is sent to the selected MSU. Note that ADD0 has incremented the A Address Register and may change the states of the A Address Bits 0 and 1. Following the second start, ENDCYL0 (2A2) and the first 16 bits of data are received from the MSU. The B Latch is reset by a low X235 (FETCH1 • ENDCYL0 • A141). STRB1 goes low. SCSTR1A and MWRT0 (high) provide a high level to the J input of the CPU Read flip-flop (3K3). ENDCYL0 toggles the flip-flop set providing a low on X163 (3K3) whcih starts Delay Line A (DLA) (4B2), a 50 nanosecond delay line. X163 low pulses Select CPU Read (SCR1A/B) (3N8) high to enable the MBC's Data Register onto CPU Data Lines CD001:151. DLA001 pulses the CPU Ready signal (CRDY0) (3N4) low. The first ENDCYL0 terminates the FETCH0 (2F1) signal which prevented generation of the END0 signals by the first ENDCYL0. The DLA501 signal (X128) (4N1) and DLA201 direct clear the CPU Read flip-flop, X163 high (3K4), and DLA201 enables the Memory Data Reset (MDRST0) which resets the 16 data line registers. This completes the first read of an Instruction Fetch. The second ENDCYL0 follows the first by 150 nanoseconds. The signal sequencing which handles the data is identical to that generated by the first ENDCYL0. However, since the FETCH0 signal is high (2E1), END0A, B, C, D, E, F, H, and J signals are generated terminating SCSTR1, AA000:130 and AB000:130, DLTRG1, and STRA1 which terminates STRA00:30. After the second CRDY0 signal is generated the CPU terminates the CREQ0 signal. The CPU terminates FETCH0 after the first CREQ0. If the Instruction Fetch is Start A (CA140=Low) no ADD0 signal is generated and the address registers are not incremented.

13.4 DMA Memory Write (Figure 10)

On a DMA Memory Write cycle, the DMA Request signal (REQ0) (2A5) is input to the MBC. REQ0 is inverted to REQ1 and ANDed with ENT0 (high) (2C8) to activate Enable (EN0) (2A5). REQ1 drives REQ low starting the 100 nanosecond one shot (2C8). When the 100 nanosecond one shot times-out, 03K01 goes low, toggling set the JK flip-flop ENT0 low. ENT0 terminates the EN0 signal which reset the REQ0 if this is a single DMA request. ENT1 triggers the second one shot timer. When the 100 nanosecond one shot times-out, its output, MXREQ1, sets DCUE1 high. DCUE1 (2F4) input to the Interlock circuit (Sheet 2), toggles set the DMA Queue flip-flop (2H4). The flip-flop output lead, select DMA Address signal (SDA) high. SDA1 gates the DMA address or DMA Address Lines MA000:130 (Sheets 7, 8 and 9) into the A and B Address Registers; SDA0 also terminates DCUE1. The EN0 Address signal (ENDST0) (3H4) goes low-active approximately 30 nanoseconds after SDA1 is pulsed high, terminating the SDA0 signal. SDAR1 (2J4) also generates SDSTR0 (2M4) which activates Delay Line Trigger (DLTRG1) (2N3) and SDSTR1 (2N5). DLTRG1 starts the 100 nanosecond delay line (4B3) and the time-out circuit (3G2). With DLC001 and SDA1B high, the state of DMA Address Bit 14 (MA140) (3A6) determines if Start A (STRA1)(3E7) or Start B (STRB1) (3E7) is enabled. Address Bits 0 and 1 from the A and B Address Register (Sheet 7) are ANDed with STRA1 or STRB1 to select one of four MSU boards and the half of memory to be accessed, (i. e., STRA00:30/STRB00:30). The Address Bits (AA020:130 and AB020:130) are output to the selected MSU. DLC001 (4F2) and DLC060 (high) pulses Data Reset low (DRST0), which in turn pulses Memory Data Reset low (MDRST0), resetting the MBC Data Register (Sheets 5 and 6) and the Parity Bit latch (9K5).

At this time the active DRST0 and SDSTR1 cause ENT0 (2B8) to go high. A second REQ0 may be waiting which would cause a second EN0 to be generated and the one shot timer (2A8) to be triggered. If the cycle in progress (first cycle) is a Write, the trailing edge of EN0 is timed by the one shot. However, if the cycle in progress is a read, the EN0 trailing edge is timed by the flip-flop toggled by X162 (2B6).

With an active WRT0 and SDA1B (8H8), the Memory Write latch (8L8) sets. The set output from the Memory Write latch enables the Memory Write signal (MWRT0) to the MSU and the MBC Parity circuit (Sheet 9). SDSTR1A, MWRT1 (4E4), and DLC001 (4B4) enable the Select DMA Write signals (SDW1A/B) (4H3). SDW1A/B loads the 16 data bits from DMA Data Lines MSD000:150 into the MBC Data Register (DL000:150). The data register outputs are also input to the Parity Generation circuit (Sheet 9). SDW1B and DLA500 pulses INH0 (3M4) low. The DMA raises CWRT0 and CREQ0, terminating the Memory Write operation on the DMA Bus. After the MSU has written the data into memory, it returns an End of Cycle signal (ENDCYL0) (2A2). ENDCYL0 enables END0 A, B, C, D, E, F, H and J (3J7) which terminate the internal MBC control signals, SDSTR1, AA or AB 000:130, DLTRG1, MWRT0, and STRA or STRB.

13.5 DMA Memory Read (Figure 11)

A DMA Memory Read operation starts in the same sequence as a DMA Memory Write operation. That is, request for memory access, addressing the MSU, and resetting the Data Line Registers. In a Memory Read operation, the DMA Bus Write signal (WRT0) (8H9) is held high. This prevents generation of the SDW1A/B (4H3) signals which loaded the MBC Data Register in the Write cycle. Also, the absence of a Write signal (MWRT0A) (8R7) to the MSU causes the MSU Strobe Read signal (STRB1) to go high. STRB1 strobes the 16 sense digit circuits, enabling the data to be read from the memory cells in the addressed chips. The MSU returns End of Cycle (ENDCYL0) (2A2) to the MBC. This indicates that the MSU has read the addressed data out of memory. SDSTR1 (high) and MWRT0 (high) provide a high to the J input of the Read flip-flop (3K4). ENDCYL0 toggles the flip-flop set. The Q output (low) is inverted to provide Select DMA Read signals (SDR1A/B) (3N6). These signals load the MBC's Data Register onto DMA Data Lines MSD000:150. SDR0A low starts Delay Line A (DLA000) (50 nanoseconds) (4K2). DLA101, DLA500 high, and X162 (high) pulses the DMA Inhibit signal (INH0) (3N5) low. The requesting DMAC terminates MA140. When DLARST0 (derived from Delay Line A) goes low (4N2); it direct clears the DMA Read flip-flop (3K4) causing X162 to go low. DLA201 (4N3) and SDR0A (4N3) pulses X160 low, enabling the second Memory Data Reset signal (MDRST0) which resets the MBC Data Register. ENDCYL0 enables END0A, B, C, D, E, F, and J (3J7) which terminate the internal MBC control signals, SDSTR1, AA or AB000:130, DLTRG1 and STRA1 or STRB1.

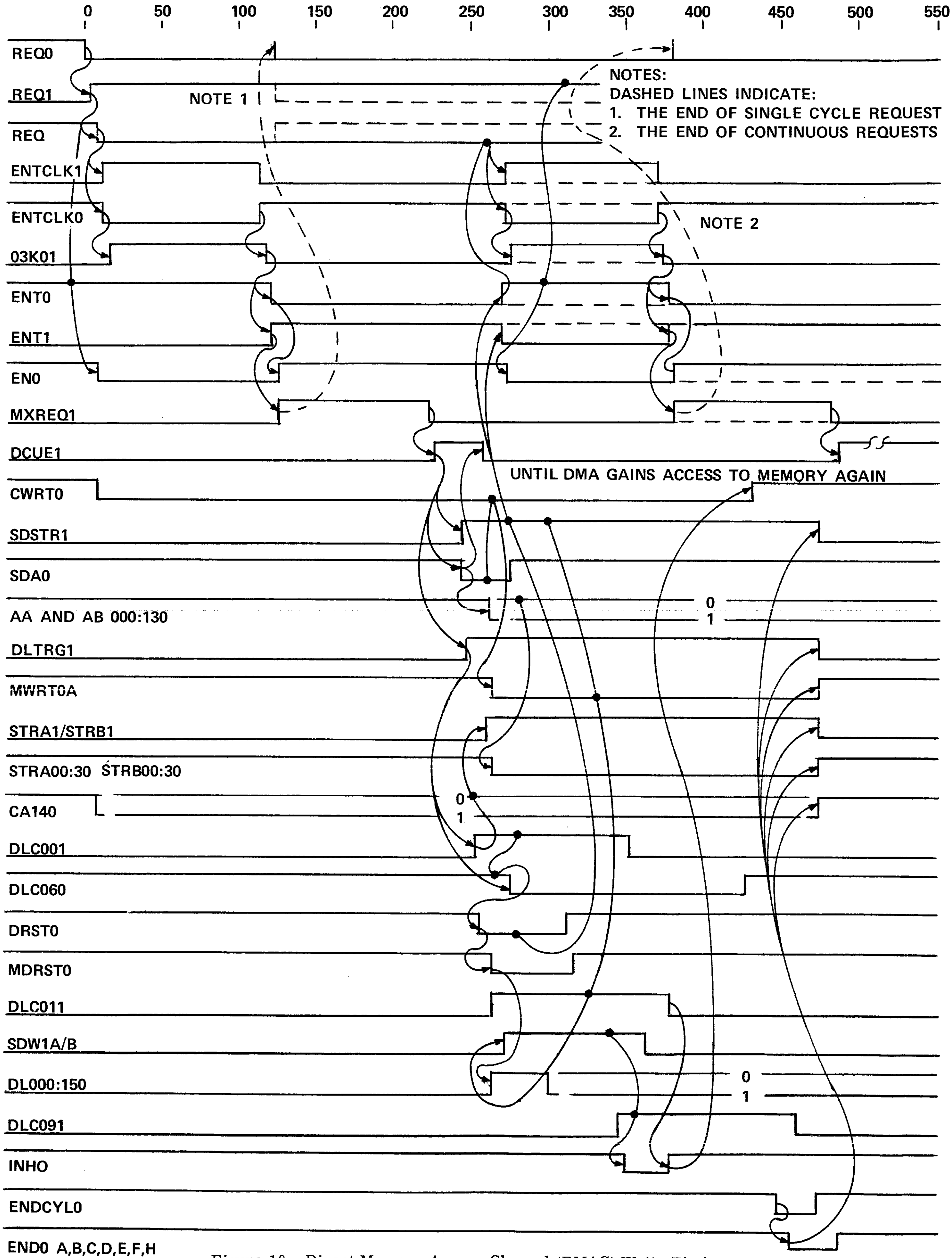

0
50
100
150
200
250
300
350
400
450
500
550
REQ0
REQ1
REQ
ENTCLK1
ENTCLK0
03K01
ENT0
ENT1
EN0
MXREQ1
DCUE1
CWRT0
SDSTR1
SDA0
AA AND AB 000:130
DLTRG1
MWRT0A
STRA1/STRB1
STRA00:30 STRB00:30
CA140
DLC001
DLC060
DRST0
MDRST0
DLC011
SDW1A/B
DL000:150
DLC091
INH0
ENDCYL0
END0 A,B,C,D,E,F,H
NOTE 1
NOTE 2
NOTES:
DASHED LINES INDICATE:
1. THE END OF SINGLE CYCLE REQUEST
2. THE END OF CONTINUOUS REQUESTS
UNTIL DMA GAINS ACCESS TO MEMORY AGAIN
0
1
0
1
0
1

Figure 10. Direct Memory Access Channel (DMAC) Write Timing

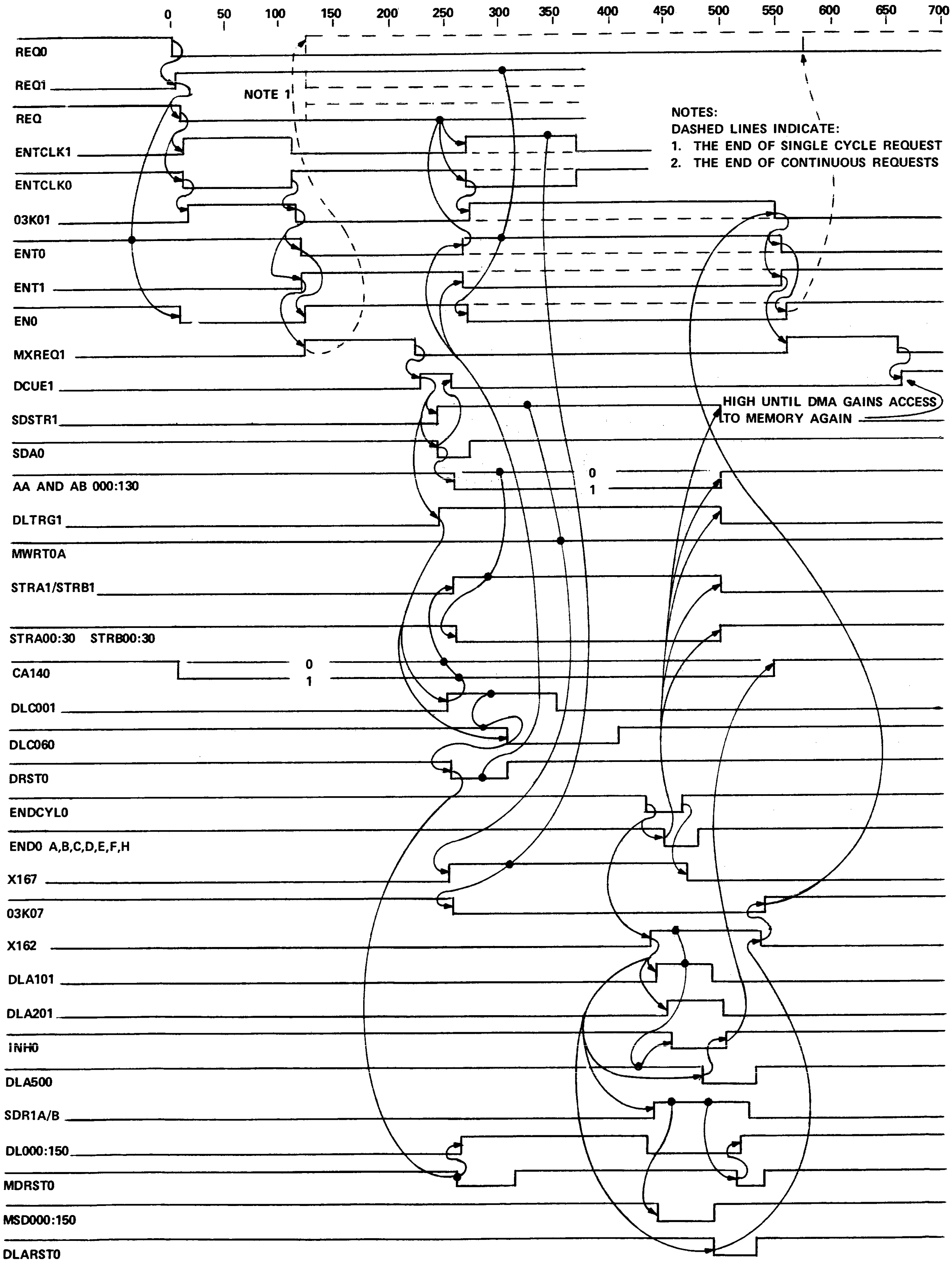

0
50
100
150
200
250
300
350
400
450
500
550
600
650
700
REQ0
REQ1
REQ
ENTCLK1
ENTCLK0
03K01
ENT0
ENT1
EN0
MXREQ1
DCUE1
SDSTR1
SDA0
AA AND AB 000:130
DLTRG1
MWRT0A
STRA1/STRB1
STRA00:30 STRB00:30
CA140
DLC001
DLC060
DRST0
ENDCYL0
END0 A,B,C,D,E,F,H
X167
03K07
X162
DLA101
DLA201
INH0
DLA500
SDR1A/B
DL000:150
MDRST0
MSD000:150
DLARST0
NOTE 1
0
1
0
1
NOTES:
DASHED LINES INDICATE:
1. THE END OF SINGLE CYCLE REQUEST
2. THE END OF CONTINUOUS REQUESTS
HIGH UNTIL DMA GAINS ACCESS
TO MEMORY AGAIN

Figure 11. Direct Memory Access Channel (DMAC) Read Timing

13.6 Refresh Cycles (Figure 12)

The MBC generates Refresh cycles in the Single Cycle Mode or the 32 Cycle Burst Mode. The 32 Cycle Burst Mode is in operation during the Standby Mode; i.e., whenever the system clear signal (SCLR0) is low and P5S is pulsing. The MBC must go in and out of the Standby Mode in an orderly manner. The key to understanding the orderly change over lies in understanding how the Memory Reset signals (MRST0 and MRST1) are generated. Discrete components are used to generate MRST0 and MRST1, (7R7).

Q18 and Q19 are connected as a differential amplifier (powered by P22). R33 and R24 form a voltage divider that generates a 4 volt reference input to the differential amplifier. Since P5S is the other input to the differential amplifier, Q18 conducts whenever P5S is greater than 4 volts and is cut off whenever P5S is less than 4 volts. The Q18 output is then amplified by Q15, Q16 and Q17 to produce the MRST0 and MRST1 signals. MRST0 is therefore low whenever P5S is below 4 volts and high whenever P5S is above 4 volts. MRST1 would be the complement of MRST0 except for two differences. First, the high for MRST1 can only be as high as P5S since the pull-up resistor is powered by P5S. Second, the timing is slightly different due to the delay caused by C13. See Figure 12 for waveforms. The negative going edge of MRST1 follows the positive going edge of MRST1 by approximately 5 micro-seconds.

During the time P5S is below 4 volts, MRST0 is holding the Refresh circuits in a reset state (initializing). After P5S reaches 4 volts, MRST0 goes high. All circuits remain in their initialized and inactive state until MRST1 goes low (see Figures 12 and 13). MRST1 going low causes Refresh Enable (REN1) (4B8) to go active. REN1 sets the Refresh Queue flip-flop and immediately generates an active SROB because the Interlock DMA and CPU Queue flip-flops are reset at this time. SROB going active generates Delay Line Trigger (DLTRG1) (2M3). About 130 nanoseconds later, X261 (4A5) goes low which causes both A and B Start latches to set; STRA1 and STRB1 (3E5) go high. About 120 nanoseconds earlier the Refresh Address counter (RA09:13) (4H7) was loaded into both MBC Address Registers (A and B). The Load Refresh Address signal (LRA1) (4G6) is generated from Delay Line C (4B2). Prior to LRA1, the Refresh counter had been initialized to all zeros (referred to as Count 0 Refresh Address). When the Load Refresh Address signal (LRA1) ends, the Refresh Address Counter is incremented for the next cycle. STRA1 and STRB1 going active generates all eight Start signals (STRA00:30 and STRB00:30) in a Refresh cycle. This is due to the forcing high of AB000, AB001, AB010, AB011, AA000, AA002, AA010, and AA011 by simultaneously setting and resetting the associated address registers (7D2). Since all start signals are generated, all equipped MSUs will do a Refresh cycle (Count 0 Address) simultaneously. At the end of the Count 0 Refresh cycle, the MSU returns an End of Cycle signal (ENDCYL0) which generates the END0 signals END0, END0 A, B, C, D, E, F, H, and J. The END0 signals reset the Refresh Queue flip-flop, SROB, DLTRG1, STRA1, STRB1, and all Start signals (STRA00:30 and STRB00:30).

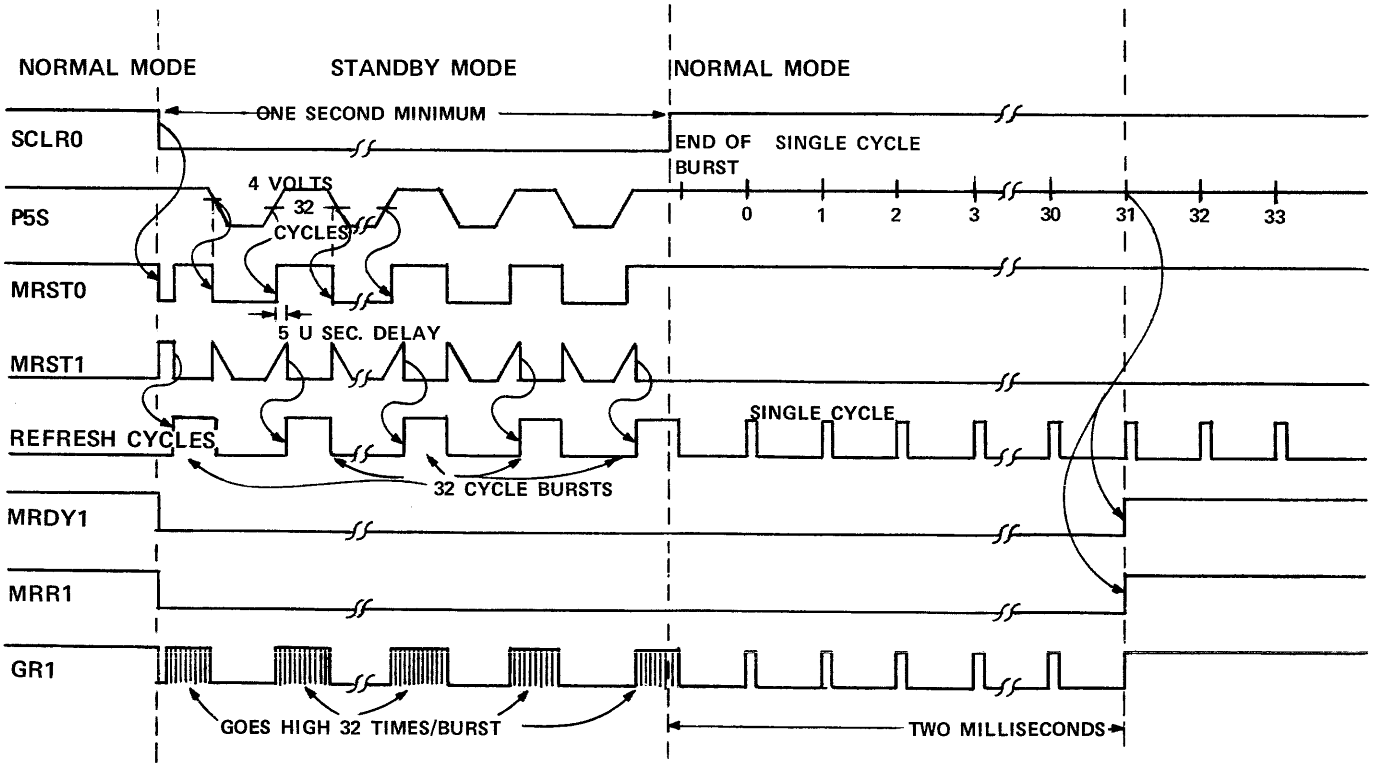


Figure 12. Standby/Normal Mode Timing Diagram

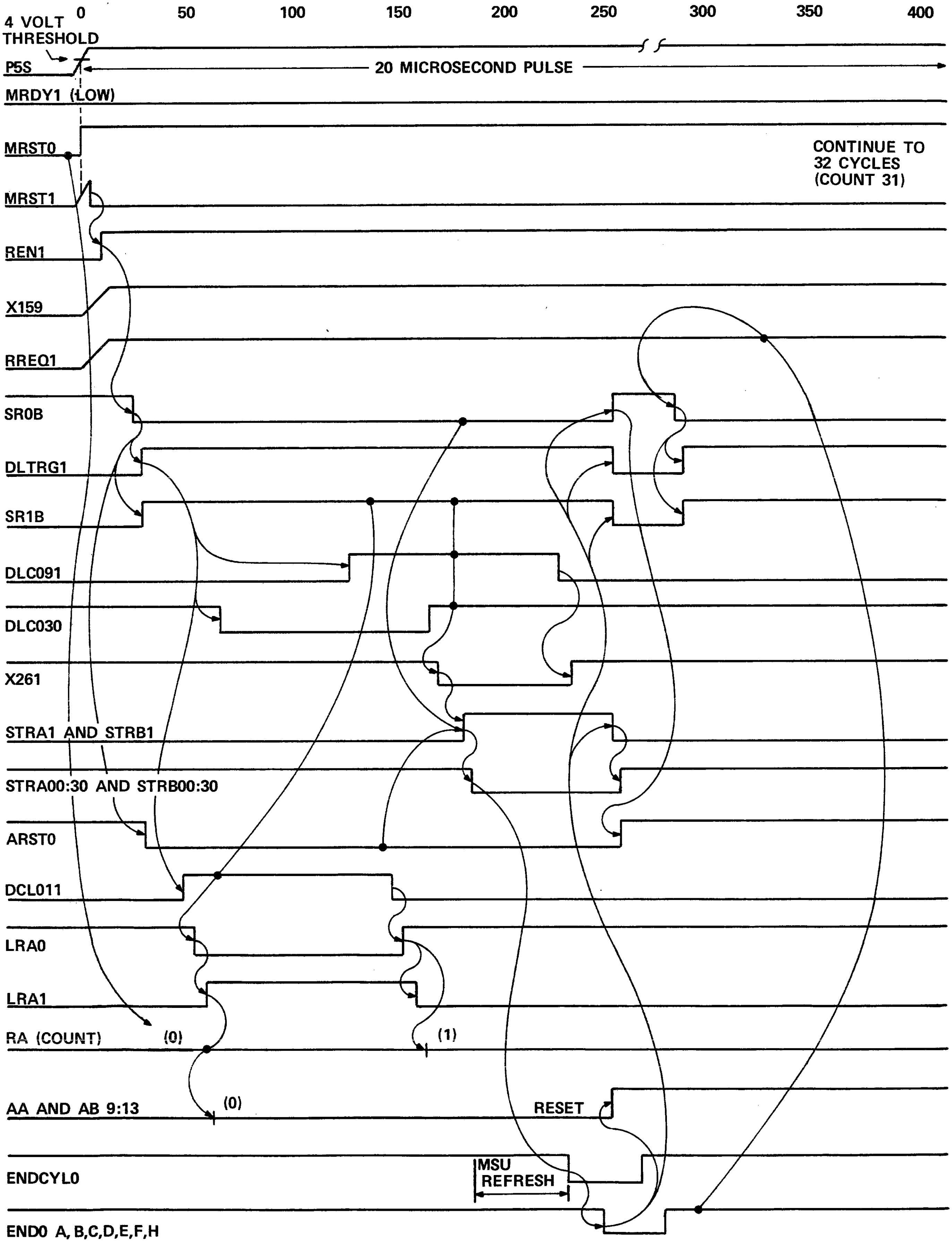

0
50
100
150
200
250
300
350
400
4 VOLT THRESHOLD
P5S
20 MICROSECOND PULSE
MRDY1 (LOW)
MRST0
CONTINUE TO 32 CYCLES (COUNT 31)
MRST1
REN1
X159
RREQ1
SR0B
DLTRG1
SR1B
DLC091
DLC030
X261
STRA1 AND STRB1
STRA00:30 AND STRB00:30
ARST0
DCL011
LRA0
LRA1
RA (COUNT)
(0)
(1)
AA AND AB 9:13
(0)
RESET
ENDCYL0
MSU REFRESH
END0 A, B,C,D,E,F,H

Figure 13. First Cycle of a 32 Cycle Refresh Burst

When the END0 signals go high, the Interlock circuit finds the Refresh Request (RREQ1) (2F3) still high and another cycle is performed identical to the first except that the Refresh Count is 1 this time. Refresh cycles are repeated in this manner at a rapid rate until the Count 31 cycle is active. During the Count 31 cycle, RA091 is set low toggling X159 (4L8) low which triggers a one shot. The one shot output (Refresh Requests-RREQ1) is set low. Following the Count 31 Refresh cycle, the Interlock finds RREQ1 in a low state and does not generate another Refresh cycle until RREQ1 goes high again. However, since the Standby Mode is in effect, before the one-shot times out to generate another Refresh Request (RREQ1), P5S is turned off causing Memory Reset (MRST0) to force all circuits to the initialized state. (see Figure 14).

No further memory activity occurs until P5S rises again activating another 32 Cycle Refresh Burst.

The Burst Refreshes continue as long as P5S continues to switch on and off (Standby Mode). After the system is switched to the Normal Mode (SCLR0 goes high), the P5S switches on and remains on for the duration of the Normal Mode.

When this occurs, P5S rises and causes a 32 Cycle Refresh Burst as before but following the Count 31 Refresh cycle of the Refresh Burst, and the triggering of the RREQ1 one shot, MRST0 does not go low (since P5S remains on). The one shot which generates RREQ1 (4M8) can time-out (50 nanoseconds) without interruption. When it does, RREQ1 goes high and causes a Refresh cycle to be generated. This Refresh cycle triggers the one shot causing the Refresh Request (RREQ1) to go inactive for another 50 micro-seconds. The Refresh circuits are now operating in the Single Cycle Mode. Refer to Figure 15.

The Memory does not respond to DMA or CPU requests as soon as the system is placed into the Normal Mode but waits until the Memory Ready signals (MRR1 and MRDY1) (4B8) go high. These signals, when low, prevent the MBC from responding to any outside request (DMA or CPU). The Memory Ready signals are low for the entire Standby Mode plus the time it takes for the memory to perform the first 32 Single Refresh cycles. See Figure 12. The Memory Ready flip-flop (4C8) is toggled set (X151 goes low) by RA091 going low. Because of the J input to the Memory Ready flip-flop (4C8), X151 cannot go low until Count 31 of the Single Refresh cycle.

It should be noted that a Refresh Burst is caused everytime P5S is switched from off to on. However, there is one additional Refresh Burst that occurs. Refer to Figure 12. When the system is placed in Standby Mode, the falling edge of System Clear (SCLR0) is differentiated (Q16 at 7M8), and forces a short (approximately 3 micro-seconds) low MRST0. This resets the memory and causes a burst refresh before P5S is switched off for the first time in the Standby Mode.

13.7 Parity Generation and Check

The Parity Bit is generated during a CPU or DMA Memory Write operation. The MBC Data Register outputs (DL000:150) are input with the active Memory Write signal (MWRT0A) (9J5) to two nine bit Parity Generation/Checkers (PG/C), (04A and 04B) (9L2 and 9L4) in the parity logic circuit. The outputs from the two nine bit PG/Cs are decoded to determine if the Parity Bit (DL160) (9R5) is to be a logic 0 or 1 to maintain even parity. Refer to Table 3 for parity bit output in relation to the decoded data bits. DLC071 sets the parity bits value into its register.

Checking parity on a CPU or DMA Memory Read operation consists of monitoring the inputs of the 16 data line registers as in parity generation and inputting the accompaning parity bit level (DL160) 0 or 1 to 04B PG/C. Refer to Table 3 for parity check of the incoming 17 data bits. If the two nine bit PG/Cs decode to any state other than those shown in Table 4, Parity Error (PERR1) (9R3) becomes active, which in turn enables the Data Parity Fail signal (DPF0) (3N7). On a CPU Instruction Fetch (32 bits) a Parity Failure on either 16 bit halfword enables the Instruction Parity Failure (IPF0) (3N7). Parity Initializing Program 06-144 is used to establish parity status of the digits in the MSUs. This program prevents parity errors from being recorded from unused memory locations.

13.8 Memory Write Protect

The protect Mask Memory Register (16 words, 4 bits per word) (8D6) is loaded from the Memory Protect Controller (MPC) by a series of 16 clock pulses, Write Clock (WCLK0) (8A7), each accompanied by a 4-bit Mask Word (MSK00:30) (8A6), 4-bit Word Addresses (WSA1, WSB1, WSC1, and WSD1) (8A3), and Write Enable (WEBL0) (8A9). During a CPU Memory Write operation the 16 words in the memory register are examined by Address A Bits 001:031 (8C4). The selected 4-bit word appears on the four outputs of the Mask Memory Register. Address A Bits 041:051 (8A2) selects one of the four outputs. If the requested Write is to a protected 1,024 bytes of memory, the Memory Protect circuit aborts Memory Write (MWRT0A) (8N7) and sends a Protect Failure signal (PRFL0) (8R8) to the MPC. The DMA port is not subject to Memory Protect.

The Memory Protect circuit is activated when both the PVMD0 (from CPU) and the PON0 (from MPC) lines are low (8F7). When either line is high it turns off the Protect Mode. While the 64 bit Mask Register is being changed (via the MPC), the CPU keeps the PVMD0 line high.

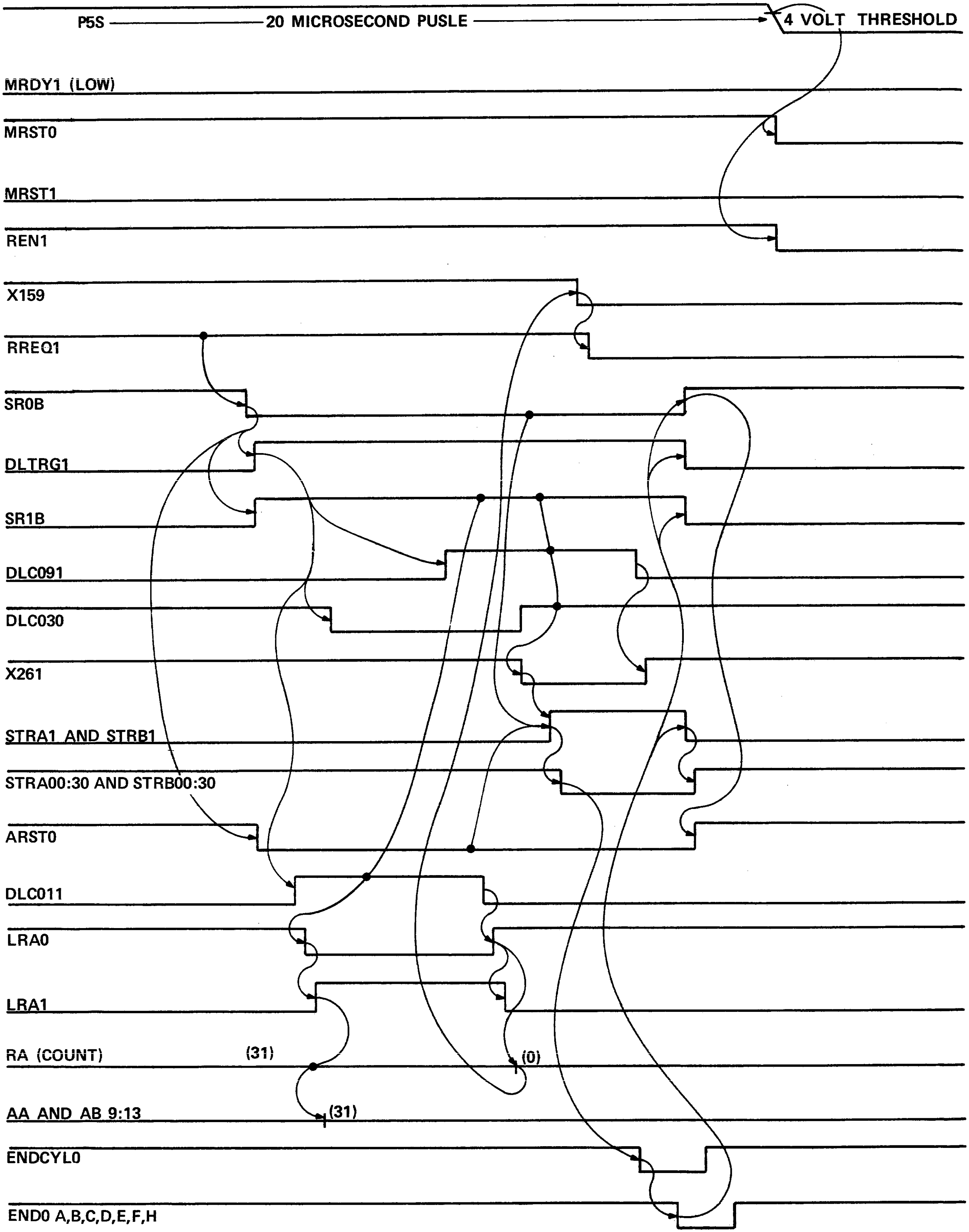
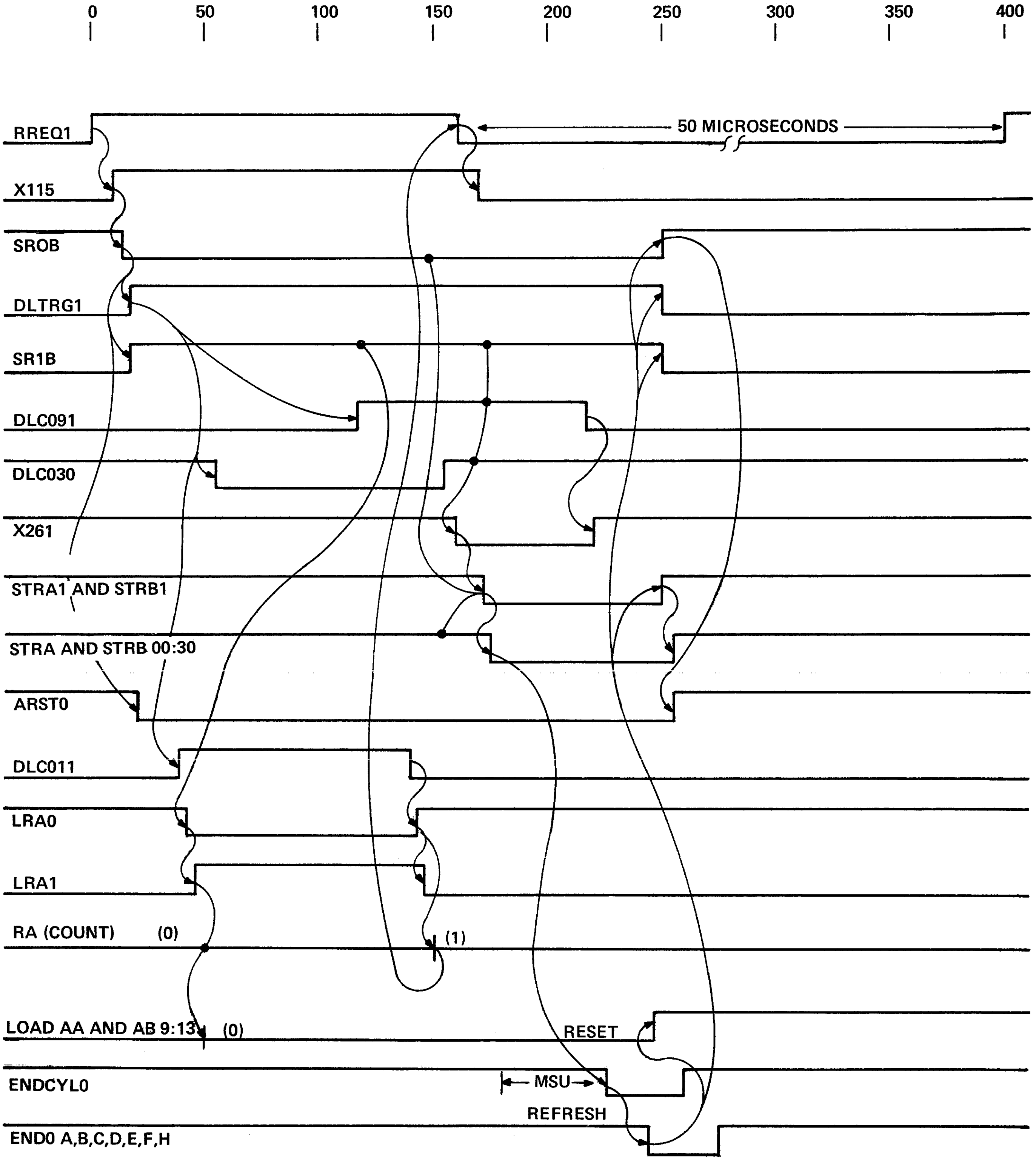

P5S
20 MICROSECOND PUSLE
4 VOLT THRESHOLD
MRDY1 (LOW)
MRST0
MRST1
REN1
X159
RREQ1
SR0B
DLTRG1
SR1B
DLC091
DLC030
X261
STRA1 AND STRB1
STRA00:30 AND STRB00:30
ARST0
DLC011
LRA0
LRA1
RA (COUNT)
(31)
(0)
AA AND AB 9:13
(31)
ENDCYL0
END0 A,B,C,D,E,F,H

Figure 14. Last Cycle of a 32 Cycle Refresh Burst



0
50
100
150
200
250
300
350
400
RREQ1
50 MICROSECONDS
X115
SROB
DLTRG1
SR1B
DLC091
DLC030
X261
STRA1 AND STRB1
STRA AND STRB 00:30
ARST0
DLC011
LRA0
LRA1
RA (COUNT)
(0)
(1)
LOAD AA AND AB 9:13
(0)
RESET
ENDCYL0
MSU
REFRESH
END0 A,B,C,D,E,F,H

Figure 15. Single Refresh Cycle

TABLE 3. PARITY BIT GENERATION

DL001:DL151	PEO0 (04F-01)	POE0 (04F02)	Parity Bit (DL16)
Even number of Digits equalling One	Low	High	Zero
	or		
	High	Low	
Odd number of Digits equalling One	High	High	One

TABLE 4. PARITY BIT CHECK

DL001:DL161 Value	PEE0 (04E-13)	POO0 (04E-01)
Even number of Digits equalling One (Not Failing)	High	High
Odd number of Digits equalling One (Failing)	High	Low
	or	
	Low	High

13.9 Interlock Contention and Priority Logic

The key signals of the MBC Interlock circuit are:

1. CCUE1	CPU Request (CREQ0) inverted.
2. DCUE1	A registered DMA Request signal.
3. RREQ1	Refresh Request
4. END0	A pulse which resets the Interlock circuits at the end of every Memory cycle.
5. SROB	Select Refresh signal-active for duration of each Refresh Memory.
6. SDSTR1	Select DMA signal-active for duration of each DMA Memory cycle.
7. SCSTR1	Select CPU signal-active for duration of each CPU Memory cycle.
8. DLTRG1	Triggers Delay Line C which generates the timing used by every Memory cycle.
9. X118	When low, prevents other Queue flip-flops from being set.

The Interlock circuit monitors the three request inputs (CCUE1, DCUE1 and RREQ1). If any one becomes active, it sets its associated Queue flip-flop provided no other cycle is in progress. Once a Queue flip-flop is set, it can generate its associated Select signal (SROB, SDSTR1 or SCSTR1). If any Select signal becomes active, the Delay Line Trigger also becomes active to generate the necessary timing signals, which initiate the cycle. As soon as one or more of the three Queue flip-flops become set, X118 prevents any more from setting until all three Queue flip-flops are reset. It is when active simultaneous request inputs two or more Queue flip-flops to be set at one time that the Interlock logic assigns priorities. When two or more Queue flip-flops are set:

1. The CPU has first priority.
2. The DMA has second priority.
3. The Refresh has third priority.

However, to guarantee the DMA Channel every other cycle, additional logic does the following:

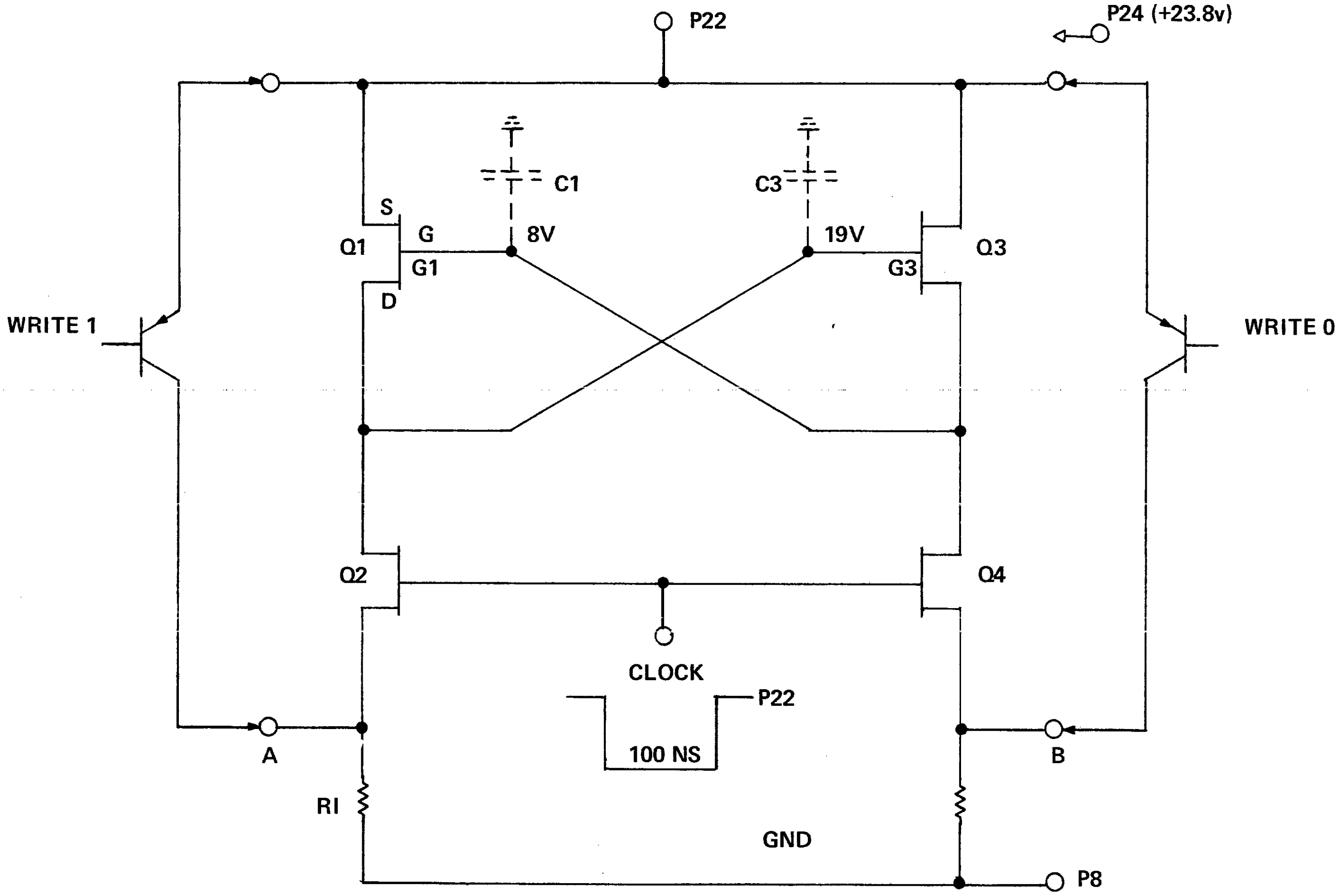
1. Following every CPU or Refresh cycle, CBLK0 goes active just long enough to allow a DCUE1 signal (if present) to set its Queue flip-flop. An active CBLK0 prevents a high CCUE1 from setting its Queue flip-flop.
2. The X267 signal (2J3) is low whenever a CPU cycle is about to end and the DMA Queue flip-flop is not set. If a CPU cycle ends with the Refresh Queue flip-flop set and the DMA Queue flip-flop set and the DMA Queue flip-flop reset, the Interlock must reset the Refresh flip-flop without having done the Refresh cycle. This prevents a waiting DCUE1 from having to wait for both the CPU and the Refresh cycle. A low X267 causes the Refresh flip-flop to reset at the end of the CPU cycle, thereby clearing all Queue flip-flops. When X118 (2F7) goes high a waiting DQUE1 sets its Queue flip-flop and the unserviced Refresh Request (RREQ1) simultaneously sets its Queue flip-flop. If CCUE1 is active also, it is prevented from setting its Queue flip-flop by CBLK0 (a CPU cycle just finished). When the Interlock circuit has both the DMA Queue flip-flop and the Refresh Queue flip-flop set, the DMA cycle is performed first, followed by the Refresh cycle.

14. MSU MEMORY STORAGE UNIT

The Model 80 Main Memory System uses 1,024 bit dynamic MOS Memory devices (chips) as storage elements. This device is commonly referred to as the 6002 type. Each MSU contains 128 chips (136 with parity). Eight 6002 chips are required by each digit to build a 16 KB Memory Storage Unit. There are actually 4 chips/digit for the A half of an MSU and an equal amount for the B half.

14.1 6002 Memory Cell Description

The 6002 type memory storage device (chip) contains an array of 1,024 P-channel dynamic memory cells along with address decoding and sense input/output circuits. The basic memory cell is shown in Figure 16. The MOS transistors are P-channel devices which conduct current if the gate terminal is more negative than the source terminal. When the clock is low (ground), the memory cell is a stable cross-coupled flip-flop. When the clock is high (P22) Q2 and Q4 are open and information is stored on the parasitic capacitance C1 or C3.



NOTES The Write 1 and Write 0 Transistors are not part of the memory cell.

Designations
S=Source
G=Gate
D=Drain
G1=Transistor Q1 Gate
G3=Transistor Q3 Gate

Figure 16. MOS Memory Cell

To write information into the memory cell, either A or B is forced to a voltage close to P22 by closing the appropriate Write switch (not part of the basic memory cell) and driving the clock to ground.

The memory cell is symmetrical so the definition of "1" and "0" is arbitrary. Suppose a Write "1" is defined by clamping point A to P22 and driving the clock to ground. With A at P22, there is no voltage across Q2, therefore, no current flow. Q4 conducts, pulling the gate of Q1 negative and charging C1 toward P8. When G1 reaches the threshold voltage (3 or 4 volts below P22, Q1 conducts, clamping the voltage of G3 (the gate of Q3) to P22, discharging C3 and keeping Q3 turned off.

At this point, the clock returns to P22, Q2 and Q4 open and information is stored as a charge on C1 with no charge on C3.

To read information from the memory cell, the clock is driven low with A and B allowed to float. Since C1 holds G1 negative with respect to P22, Q1 and Q2 conduct heavily, developing a positive voltage across R1. Q4 is on and momentarily carries current while it charges C1 back down to P8. Q1 also clamps the gate of Q3 to P22 keeping C3 discharged. Thus, the Read operation produces an output signal at A and it restores C1 to full charge.

The charge stored on C1 or C3 will leak off in time, therefore, it is necessary to "Refresh" the charge condition periodically by clocking the memory cell as in the Read operation. One cycle refreshes 32 of the 1,024 bits within a chip. By incrementing the 5 least significant Address Bits each cycle, all 1,024 bits are refreshed in 32 cycles. The rate of refresh required is highly temperature dependent. For operation up to 70°C, refresh is required every two milliseconds.

14.2 6002 Memory Device Description

Figure 17 illustrates how the 1,024 basic memory cells are connected into an array within the chip. The chip memory cell row decoder provides the clock pulse to 32 memory cells simultaneously reading and refreshing each memory cell. One pair of input/output (A/B) lines are connected to the common I/O terminals of the chip through multiplexor gates under control of the chip memory cell column decoder. The chip memory cell column decoder provides a pulse to 32 memory cells in a column simultaneously. The memory cell at the intersection of the selected row and column is enabled for Read or Write operations.

The reset (precharge) input shown on Figure 17 is used in the two-phase decoding logic. Because of the high impedance of MOS devices, resistor-transistor circuits common in DTL type logic are not generally used. High speed MOS logic uses two phase or four phase clocking schemes that charge and discharge internal capacitances through logic paths.

14.3 6002 Drive Signal Timing

Figure 18 shows the drive pulse timing required by the 1,024 bit chip. Each Read or Write operation must be preceded by a reset of the memory cells of at least 120 nanoseconds. This precharges the chip memory cell row and column decoding logic and precharges all A and B I/O lines to P8. The address must be stabilized while the reset is low (i.e., before the reset rises to its threshold level of +19 volts).

After reset goes high, 60 nanoseconds is required for the decoding logic to select the chip memory cell row and column. Then the 100 nanosecond clock and chip select can fire. In the INTERDATA Memory, Chip Select and Clock inputs are connected together and referred to as Chip Select. Also, the reset is always left on (low) except for the 160 nanosecond off time required by each memory cycle. A memory cycle normally starts at the time the address is stable (end of reset). In the Model 80 Main Memory, every chip in a given A or B half of an MSU is guaranteed 120 nanoseconds of reset following memory cycle by the MSU timing circuits.

Description of the "1" or "0" output polarity of the 6002 memory chip is arbitrary. In the Model 80 Main Memory, the output polarity varies (i.e., a positive output on Pin 19) with respect to Pin 20, is a "1" for some chips and a "0" for others). Refer to the schematic for output polarity.

Figure 18 shows the Write wave being switched from P8 to P22 during the Chip Select time. To write a "1", either Pin 19 or 20 must be switched as shown. Again, the pin assignment is arbitrary however, it must be consistent with the Readout Polarity assigned. To write a "0", the opposite Pin (19 or 20) would be switched as shown by Figure 17.

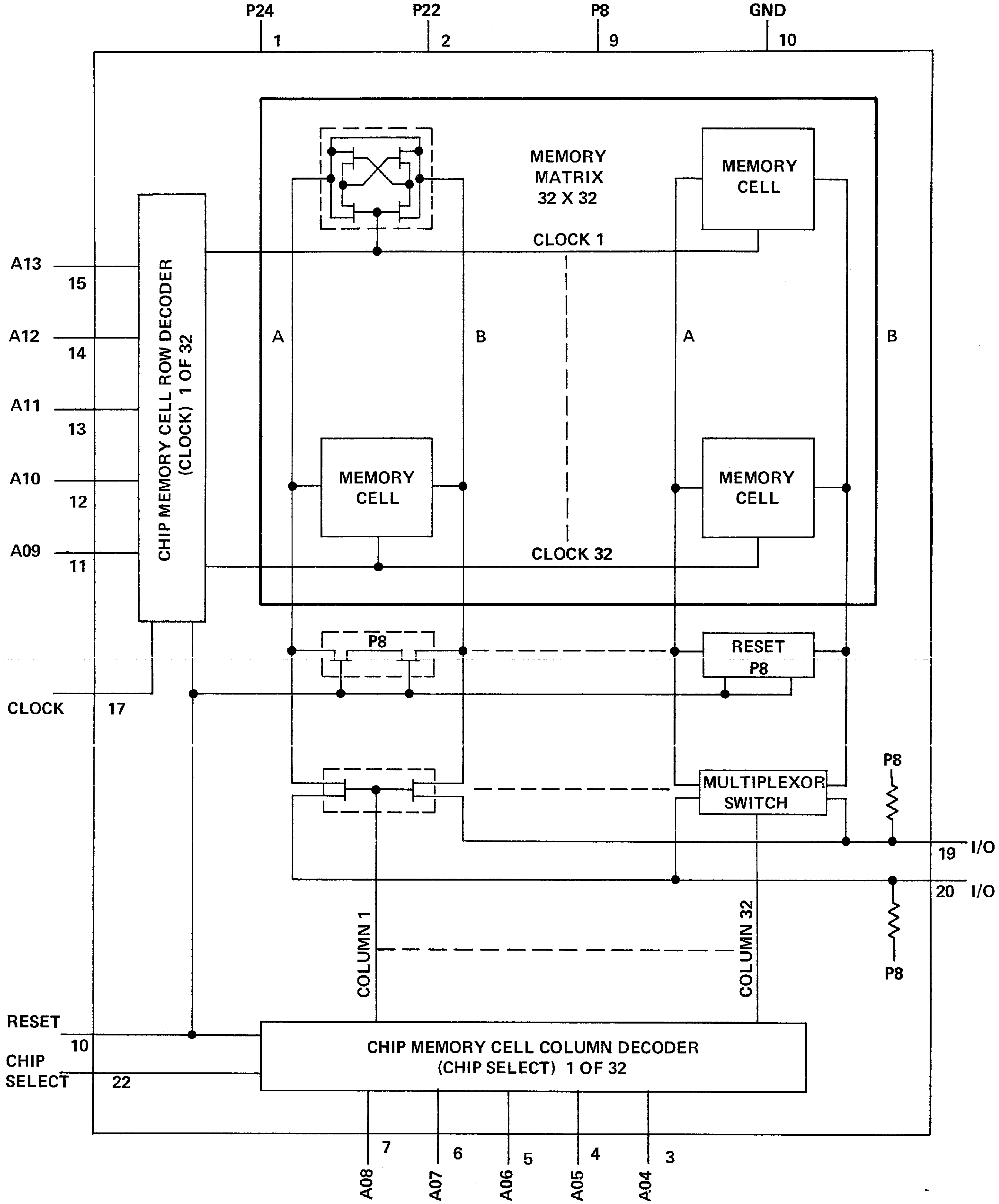

P24
1
P22
2
P8
9
GND
10
MEMORY MATRIX 32 X 32
MEMORY CELL
CLOCK 1
A
B
A
B
MEMORY CELL
MEMORY CELL
CLOCK 32
CHIP MEMORY CELL ROW DECODER (CLOCK) 1 OF 32
A13
15
A12
14
A11
13
A10
12
A09
11
P8
RESET P8
CLOCK
17
MULTIPLEXOR SWITCH
P8
19
I/O
20
I/O
P8
COLUMN 1
COLUMN 32
RESET
10
CHIP SELECT
22
CHIP MEMORY CELL COLUMN DECODER (CHIP SELECT) 1 OF 32
7
A08
6
A07
5
A06
4
A05
3
A04

Figure 17. Memory Cell Array within the Memory Storage Device (Chip)

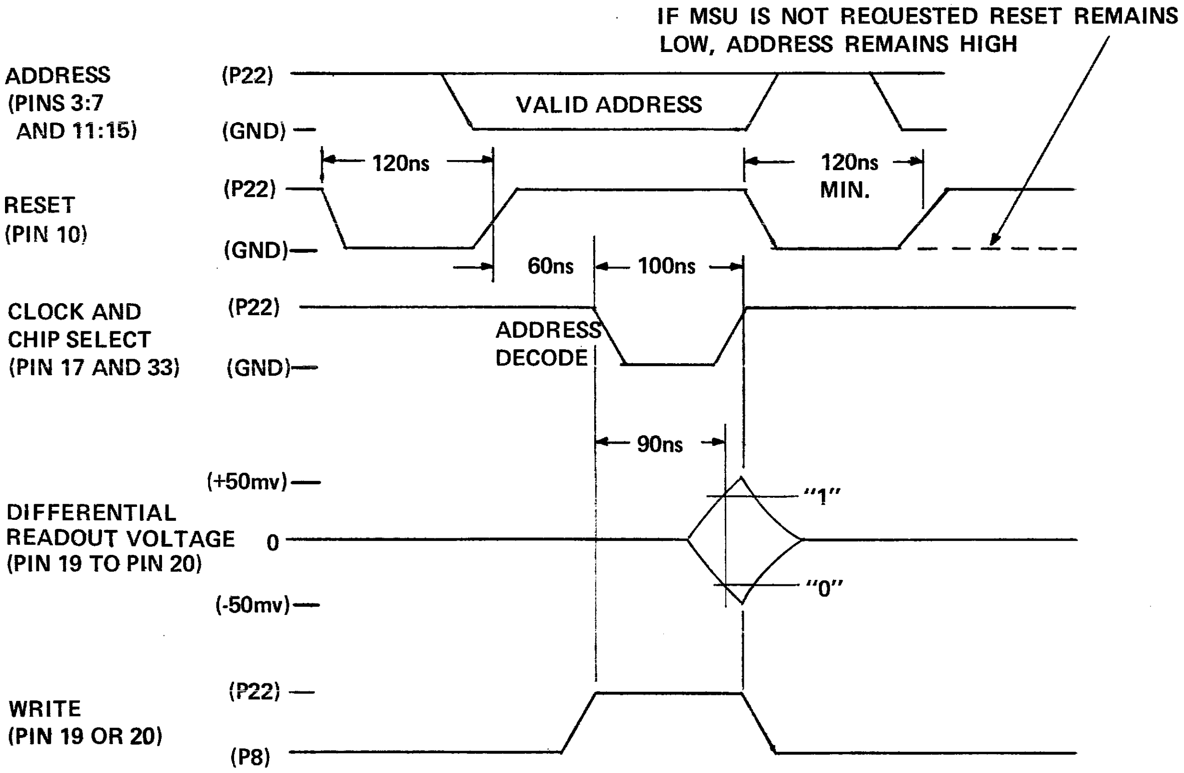

IF MSU IS NOT REQUESTED RESET REMAINS LOW, ADDRESS REMAINS HIGH
ADDRESS (PINS 3:7 AND 11:15)
(P22)
(GND)
VALID ADDRESS
120ns
120ns MIN.
RESET (PIN 10)
(P22)
(GND)
60ns
100ns
CLOCK AND CHIP SELECT (PIN 17 AND 33)
(P22)
(GND)
ADDRESS DECODE
90ns
(+50mv)
DIFFERENTIAL READOUT VOLTAGE (PIN 19 TO PIN 20)
0
(-50mv)
"1"
"0"
WRITE (PIN 19 OR 20)
(P22)
(P8)

Figure 18. 6002 Drive Signal Timing Diagram

15. MSU FUNCTIONAL BLOCK DIAGRAM

Figure 19 shows a detailed block diagram of the MSU board. Both halves of the MOS Chip Array consist of four chips for each of the 16 digits (17 with parity). Surrounding the array are the Chip Select Driver, Reset Driver, Read-out, Write Driver, and Timing circuits. A discussion of each follows.

15.1 Timing Circuit

When a Start signal (STRA00:30) or (STRB00:30) is received from the MBC by the MSU Timing circuit, a series of timing signals is generated to enable the Selected MSUs Driver circuits. These timing signals perform the following functions.

AAGT1	Enables the 10 A Address Drivers as required by AA04:13. It is active if an A Start signal (STRA00:30) is received.
ABGT1	Enables the 10 B Address Drivers as required by AB04:13. It is active if a B Start signal (STRB00:30) is received.
RAGT0	Enables A Reset Drivers (all four). This signal is active at all times except during an "A" Memory cycle.
RBGT0	Enables B Reset Drivers (all four). This signal is active at all times except during a "B" Memory cycle.
QAA0	Enables A Reset Drivers (all four). This signal goes active for 120 nanoseconds after each A Memory cycle. It also prevents a following A half Memory cycle from starting until the MOS Chips minimum 120 nanosecond reset has been satisifed.
QAB0	Enables B Reset Drivers (all four). This signal goes active for 120 nanoseconds after each B Memory cycle. It also prevents a following B half Memory cycle from starting until the MOS Chips minimum 120 nanosecond reset has been satisified.
STRB0A	This signal strobes the output of the Digit Sense Amplifiers during a Read cycle, onto the Data Lines (DL00:16).
CSAP0	Gates the A Chip Select Drivers during A Memory cycle.
CSBP0	Gates the B Chip Select Drivers during B Memory cycle.
WRTG0A	Enables the Digit Write circuits and inhibits STRB0A during Memory Write cycles.

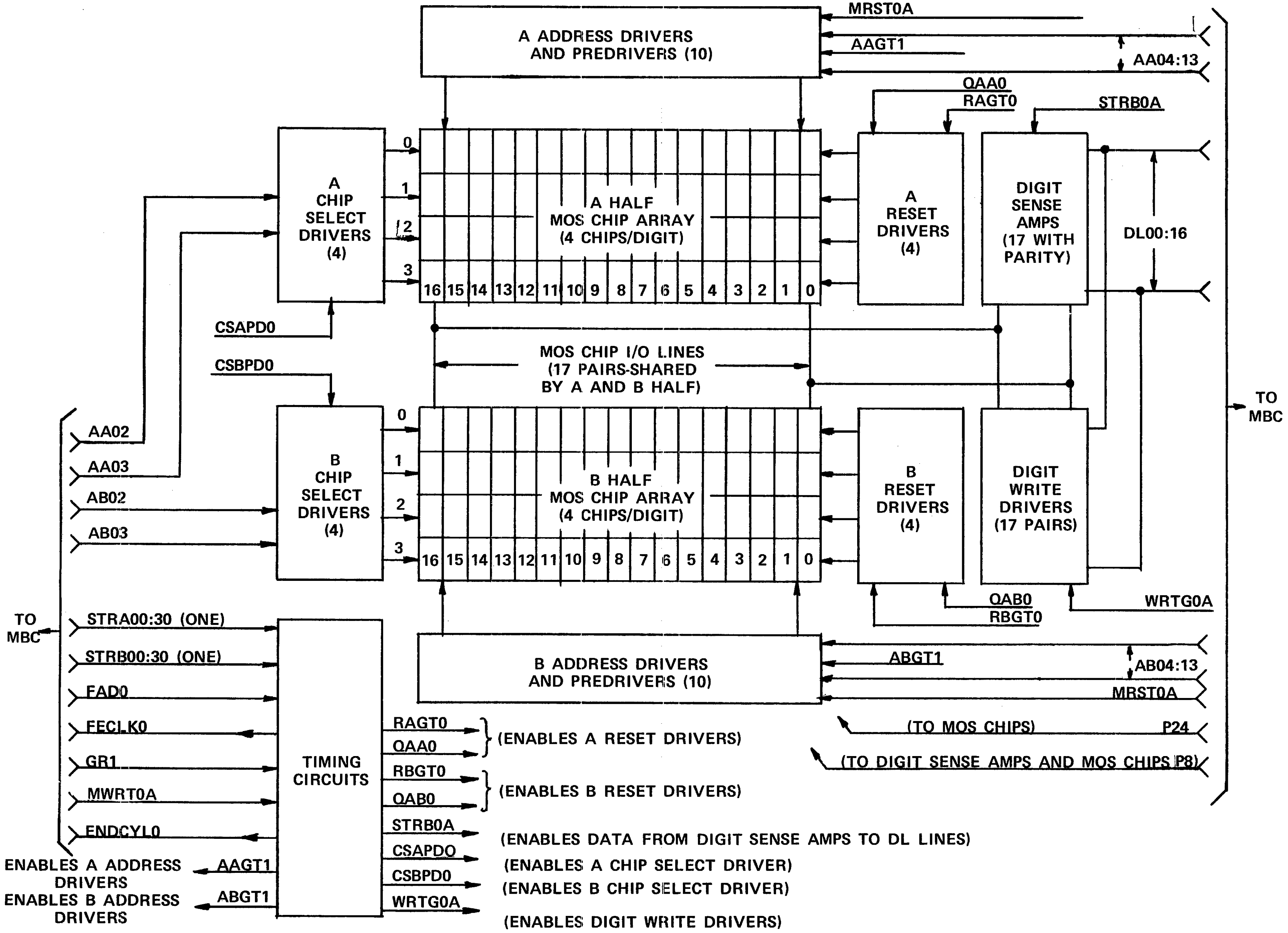

A ADDRESS DRIVERS AND PREDRIVERS (10)
MRST0A
AAGT1
AA04:13
QAA0
RAGT0
STRB0A
A CHIP SELECT DRIVERS (4)
0
1
2
3
A HALF MOS CHIP ARRAY (4 CHIPS/DIGIT)
16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
A RESET DRIVERS (4)
DIGIT SENSE AMPS (17 WITH PARITY)
DL00:16
CSAPD0
CSBPD0
MOS CHIP I/O LINES (17 PAIRS-SHARED BY A AND B HALF)
TO MBC
AA02
AA03
AB02
AB03
B CHIP SELECT DRIVERS (4)
B HALF MOS CHIP ARRAY (4 CHIPS/DIGIT)
B RESET DRIVERS (4)
DIGIT WRITE DRIVERS (17 PAIRS)
QAB0
RBGT0
WRTG0A
TO MBC
STRA00:30 (ONE)
STRB00:30 (ONE)
FAD0
FECLK0
GR1
MWRT0A
ENDCYL0
B ADDRESS DRIVERS AND PREDRIVERS (10)
ABGT1
AB04:13
MRST0A
(TO MOS CHIPS) P24
(TO DIGIT SENSE AMPS AND MOS CHIPS P8)
TIMING CIRCUITS
RAGT0
QAA0
(ENABLES A RESET DRIVERS)
RBGT0
QAB0
(ENABLES B RESET DRIVERS)
STRB0A
(ENABLES DATA FROM DIGIT SENSE AMPS TO DL LINES)
CSAPD0
(ENABLES A CHIP SELECT DRIVER)
CSBPD0
(ENABLES B CHIP SELECT DRIVER)
WRTG0A
(ENABLES DIGIT WRITE DRIVERS)
ENABLES A ADDRESS DRIVERS
AAGT1
ENABLES B ADDRESS DRIVERS
ABGT1

Figure 19. MSU Functional Block Diagram

15.2 Chip Select Drivers

For any Read or Write cycle, one of the eight Chip Select Drivers is active. The Chip Select signal (CSAP1 or CSBP1) is ANDed with the associated address input (AA02 and AA03 or AB02 and AB03) to activate the selected Chip Select Driver. It drives 16 MOS Chips (one for each digit).

15.3 Reset Drivers

Eight Read Drivers (four A and four B) are always turned on (Pin 10 of MOS Chip at ground potential) except during memory cycles. The A Reset Drivers are turned off during A Memory cycles and the B Reset Drivers are turned off during B Memory cycles. All four A Reset Drivers are switched on and off together as are all four B Reset Drivers. The four drivers (rather than one) exist because of loading considerations.

15.4 A and B Address Drivers

Ten A and ten B Address Drivers switch the ten address pins of the MOS Chips as required by the input Address Lines AA04:AA13 or AB04:AB13. For Read or Write cycles, either the A Address Drivers or the B Address Drivers (but not both) are enabled. Refresh cycles enable both A and B Drivers.

15.5 Digit Sense Amplifiers

During MSU Memory Read cycles the Digit Sense Amplifiers amplify the outputs from the 16 (17 with parity) selected MOS Chips. The outputs from the Sense Digit Amplifiers are then level shifted to normal logic levels. Sense Digit Amplifiers output are referenced to P8 rather than ground. The shifted outputs are then strobed onto the Data Lines (DL00:16).

15.6 Digit Write Drivers

During Memory Write cycles, the Digit Write drivers switch the MOS Chip I/O lines as required by the Data Lines (DL00:16). Two Digit Write drivers exist for each digit. One of the two, but not both, are turned on to Write Data into the selected MOS Chips.

16. MSU FUNCTIONAL ANALYSIS AND TIMING

Refer to Functional Schematic 02-247D08 and Figures 20 and 21 during the following analysis of the MSU logic. In Memory Read or Write cycles, the Start signal STRA00:30 (6A5) or STRB00:30 (6A6) selects one of four MSUs and enables the A or B half of memory. (During the MBC Refresh Mode, single cycle or 32 cycle bursts, all the MSUs are enabled and all memories in the MSUs are accessed.)

The STRA/B line that is pulsed low starts the sequence of timing events within the selected MSU. The major circuits affected by the start signal are described in the following sections.

16.1 Address Drivers

The low start pulse, STRA0 or STRB0 (6B4), is inverted by gate A10 (6B3). The high output signal AAGT1 (6C3) or ABGT1 (6C4) gates the address present on its corresponding address lines (AA041:131 or AB041:131) (Sheet 2) through the address gates and drivers to chips in the accessed half of memory (A or B) (Sheets 3 or 4).

16.2 Reset Drivers

The low start signal, STRA0 or STRB0 (6B4), is gated through three sets of gates (6B1, 6E1 and 6F1) to pulse RAGT0 or RBGT0 high (6F1). The high output turns off the corresponding reset drivers (A or B) in the accessed half of memory (2D1) or (2K1), if the associated one shot output signal QAA0 or QAB0 (6K2) is high. If QAA0 or QAB0 is low from a previous memory cycle, the corresponding reset drivers (Sheet 2) cannot be turned off until the one shot (QAA0 or QAB0) times out (120 nanoseconds) and the corresponding low QAA0 or QAB0 signal goes high.

16.3 Chip Select and Clock Drivers

The low start pulse, STRA0 or STRB0, is inverted by gate A15 (6B5 or 6B6) and applied to the J input of the selected Chip Select flip-flop. That is, A14 (6D8) for Memory A Chip Select and A14 (6D7) for Memory B Chip Select. The selected flip-flop is toggled set by Delay Line A21 which also provides a properly timed high to two inputs of gate A19 (6F6) and (6F7). The set output from the selected flip-flop (A14-05 or A14-09) and the high delay line input to gate A19 enables the Chip Select signal to Memory A (CSABP1) (6H9) or Memory B (CSBPD1) (6G9).

The Chip Select signal is ANDed with Address Bits 2 and 3 (4B1 or 5B1) to select the chip column in the accessed half of memory.

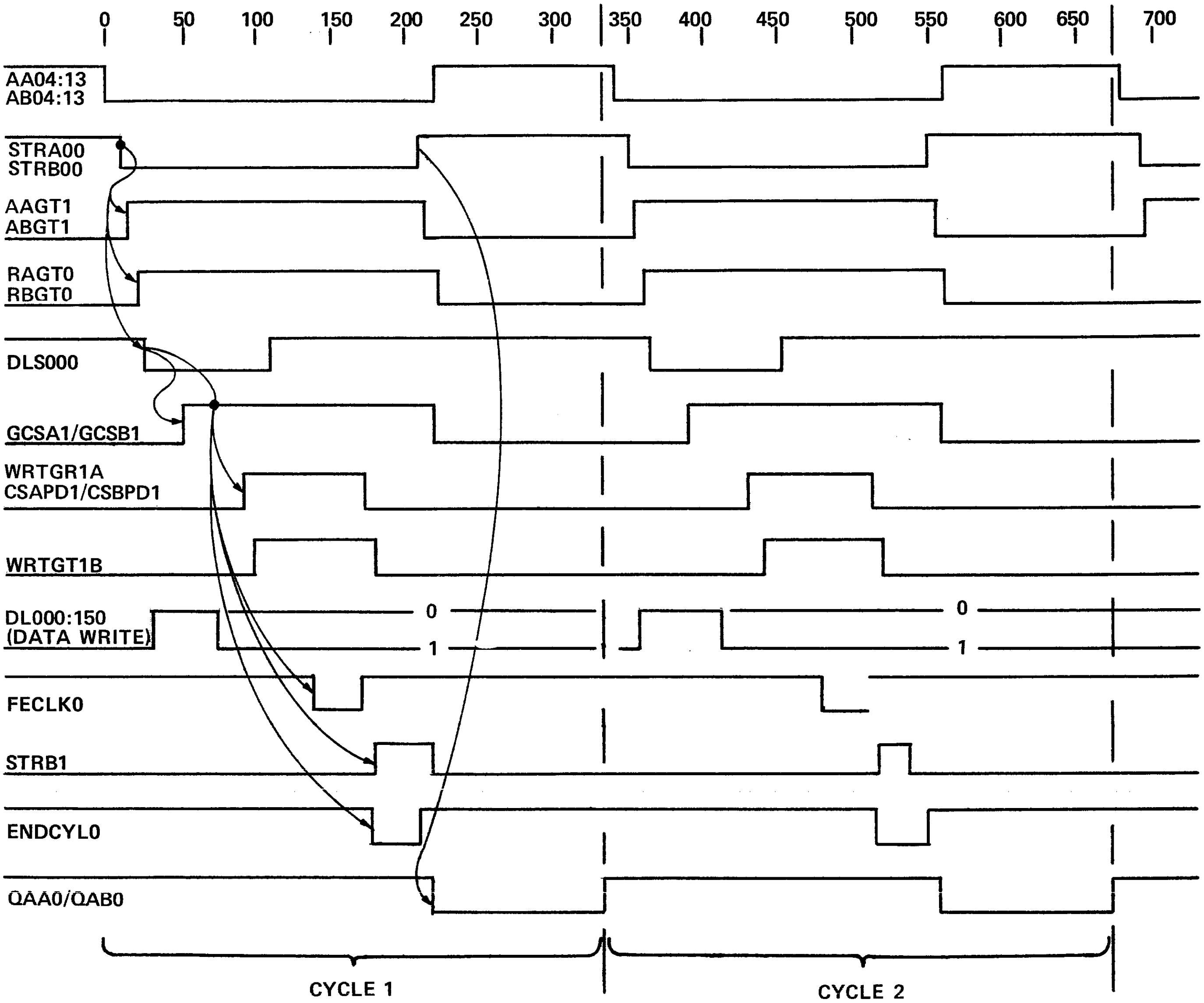

0
50
100
150
200
250
300
350
400
450
500
550
600
650
700
AA04:13
AB04:13
STRA00
STRB00
AAGT1
ABGT1
RAGT0
RBGT0
DLS000
GCSA1/GCSB1
WRTGR1A
CSAPD1/CSBPD1
WRTGT1B
DL000:150
(DATA WRITE)
0
1
0
1
FECLK0
STRB1
ENDCYL0
QAA0/QAB0
CYCLE 1
CYCLE 2

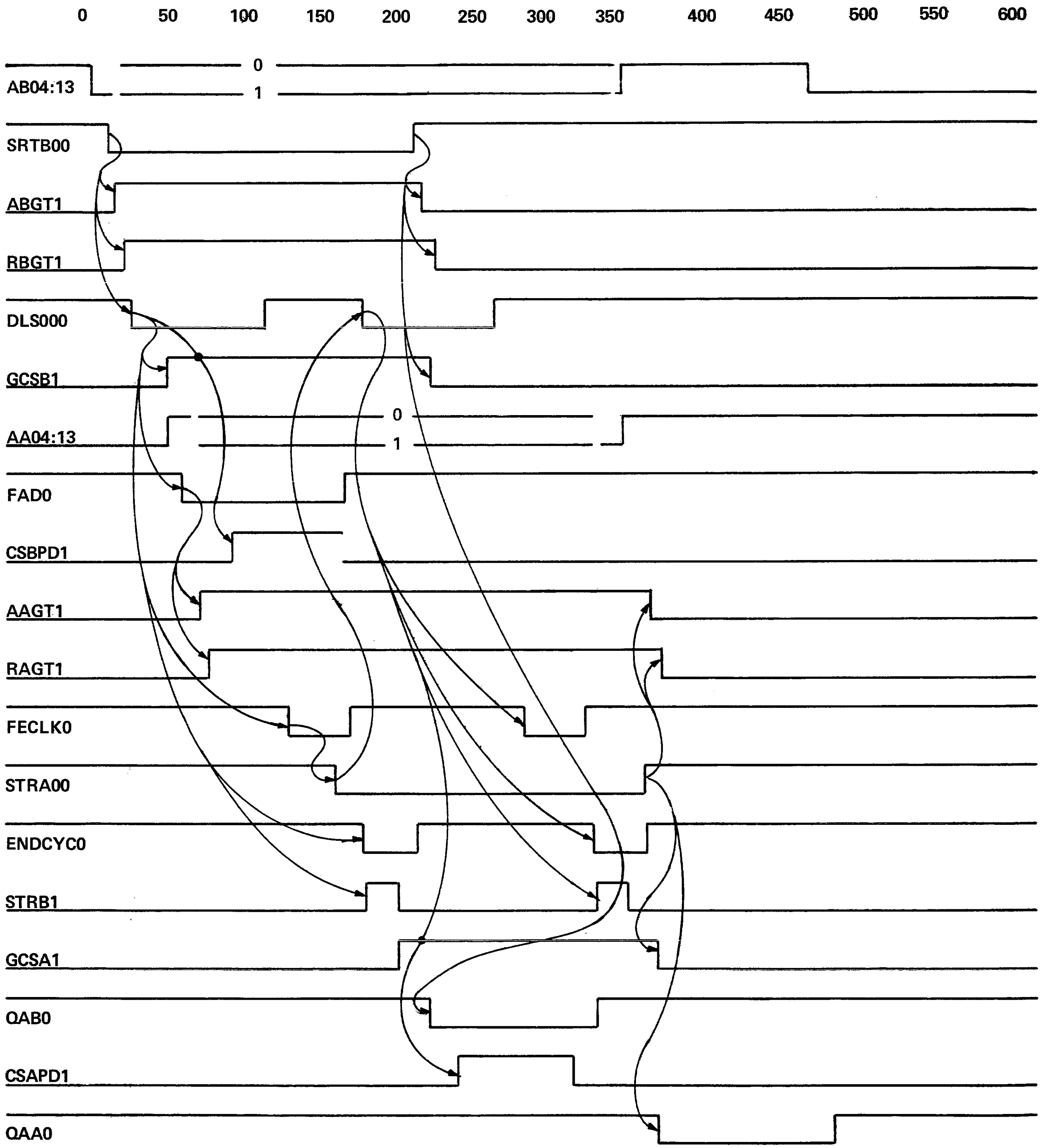
Figure 20. MSU Read or Write Cycle (Start A or Start B)

16.4 Delay Line Timing and Control

The inverted start pulse, STRA1 or STRB2, from gate A15 (6B5) or (6B6) is input to gate A10 (6K1) or (6K2). (The QAA0 and QAB0 inputs to gate A10 are considered to be inactive, that is, both high for this portion of the analysis.) The respective outputs from gate A10 (A10-03 and A10-08) are differentiated by R-C networks. The differentiator circuits pass the STRA or STRB signal as a negative 10 nanosecond pulse occurring at the negative edge of A10's output. This sets the delay line latch consisting of A18 (6M4) and A11 (6M1) and sends a negative transition (DLS000) to Delay Line A21. The 70 nanosecond tap of the delay line is fed back through gates A15 (6K4) and A17 (6K4) to reset the delay line latch and cause DLS000 to go high. When the positive transistion reaches gate A18 (6M4), the delay line latch is ready to begin another cycle. Different tap combinations of the delay line are used to generate CSABD1, CSBPD1, ENDCYL0, FECLK0, STRB1, and WRTGR1A/B. Refer to Figures 20 and 21, and to the following definitions.

CSABD1 CSBPD1	Partially enables one of four chip columns in Memory A or Memory B.
ENDCYL0	A pulse sent to the MBC at the end of Read, Write or Instruction Fetch operation. Indicates that the requested operation is complete. The MBC terminates the start signal when it receives this signal.
FECLK0	A pulse sent to the MBC during Instruction Fetch operations. Indicates to the MBC when the second start of a Fetch operation should be generated.

MWRT0A	Memory Write to the MSU.
STRB1	Strobes the 16 Sense Digit circuits in the MSU. Enables 16 data bits to be read from the 16 addressed chips.
WRTGT1A	Sends two pulses to the 16 Write Digit circuits in the MSU. Enables 16 data bits to be written into the 16 addressed chips. That is, WRTGT1A writes "0" and WRTGT1B writes "1".


0
50
100
150
200
250
300
350
400
450
500
550
600
AB04:13
0
1
SRTB00
ABGT1
RBGT1
DLS000
GCSB1
AA04:13
0
1
FAD0
CSBPD1
AAGT1
RAGT1
FECLK0
STRA00
ENDCYC0
STRB1
GCSA1
QAB0
CSAPD1
QAA0

NOTE: TIMING REFERRED TO AB LINES IN MBC

Figure 21. Instruction Fetch Cycle (B Start first)

16.5 Read or Write Cycle

During a Write operation, WRTGR1A (6M7) and WRTGT1B (6R7) are pulsed high, due to the Memory Write signal MWRT0A (6J8) being active. These signals are input to all 16 Write Digit circuits to enable any information on the 16 data lines (DL00:15) to be written into the 16 addressed chips.

During a Read operation, the Memory Write signal (MWRT0A) (6J8) to the MSU is inactive (high). This enables signal STRB1 which strobes the 16 Sense Digit circuits, gating the readout to the 16 Data Lines (DL00:15). At the end of a 16 bit Read or Write operation, ENDCYL0 (6N6) goes low, indicating to the MBC that the Read or Write operation is complete. The MBC terminates the Start signal, STRA00:30 or STRB00:30, to the selected MSU. This causes the corresponding QAA0 or QAB0 signal to go low, blocking the input (A or B) to the Delay Line latch, for 115 nanoseconds. QAA0 or QAB0 is generated by flip-flops A13 (6H3) or (6H4) and operates as a one shot. This blocks another start for the same memory designation (that is, A following A or B following B) from entering the delay line latch before it has enabled the minimum 115 nanosecond reset function required by the MOS Chips.

16.6 Instruction Fetch

The Instruction Fetch operation is nothing more to the MSU than two successive and slightly overlapping Read signals except for the active Fetch Address signal (FAD0). When doing a Instruction Fetch operation, the MBC pulses the FAD0 signal (6A2) low 50 nanoseconds after the first start signal (STRA00:30 or STRB00:30) goes low. This does two things to the second cycle of the Fetch operations that is different from a Read operation. First, FAD0 causes the second cycles Reset Gate (RAGT0 or RBGT0) (6F1) to go high, turning off the corresponding resets earlier than in a normal Read cycle. Also, the address of the second Read is gated on by FAD0 rather than wait for the second start signal. FAD0 generates FAR0 (6B2) which causes the Address Gate signal (AAGT1 or ABGT1) to go active.

16.7 Refresh

At the beginning of a Refresh cycle, the MBC pulses SROB (6A7) low allowing all chip select and clocks to be enabled. Approximately 130 nanoseconds after SROB goes active, all start signals, STRA00:30 and STRB00:30, from the MBC are pulsed together so that the A and B halves of all memories are enabled. This causes all MOS Chips on the MSU boards to undergo a Refresh cycle simultaneously. In the Normal Mode, GR1 is a constant high, leaving the resets on except during memory cycle.

The Refresh cycle is identical to a Read cycle in all other respects. When operating in the Standby Mode, GR1 (6A1) switches low between cycles to conserve power. When GR1 is low it forces all reset drivers in the main memory system off.

Conserving power in the Standby Mode saves memory for a longer period in the event of power failure (battery operation).

17. MODEL 80 MEMORY VOLTAGES

Eight voltages are used by the Model 80 Memories. Figure 22 shows their mnemonics, nominal value, location of source and if fixed or adjustable. Nominal values given are for the Normal Mode. The Standby Mode requires only P24, P22, P8 and P5S to be present. P3 in the Standby Mode should measure approximately 7 volts.

Voltage Mnemonic	Normal Mode Nominal Value	Source Location	Fixed or Adjustable	Where Measured
P24	23.8 V	MBC	Fixed	MBC
P22	21.0 V	34-014	Adjustable	Back Plane
P15	15.4 V	34-015	Adjustable	Back Plane
P13	13.2 V	MSU	Fixed	MSU
P 8	7.85 V	MBC	Adjustable	MBC
P5S	5.10 V	34-014	Adjustable	Back Plane
P 5	5.10 V	34-015	Adjustable	Back Plane
P 3	2.80 V	MBC	Fixed	MBC

Figure 22. Model 80 Memory Voltages

17.1 Voltage Margin Test

Voltages may be margined while running Part 3 of 06-003R06 Memory Test. Part 3 shall run without errors for the following voltage adjustments.

	P15	P22	P5	P5S
1.	15.3*	21.0	5.10	5.10
1.	15.5*	21.0	5.10	5.10
3.	15.4	19.5*	5.10	5.10
4.	15.4	22.5*	5.10	5.10
5.	15.4	21.0	5.10	
6.	15.4	21.0	4.85*	5.10
7.	15.4	21.0	5.35*	5.10
7.	15.4	21.0	5.10	4.85*
8.	15.4	21.0	5.10	5.35*
Normal	15.4	21.0	5.10	5.10

NOTES

1. An asterisk indicates which adjustments are margined.
2. All voltages are measured at the back panel.
3. A 1% accuracy DVM is requied to margin all voltages.

18. MODEL 80 MEMORY TEST PROGRAMS

The following test programs are recommended to check the Memory System operation.

1.	06-003R06	Memory Test Program	This tests the Memory System operation through the CPU Port only.
2.	06-143R07	Memory Retention Test Program	This program tests Refresh function of Memory System when powering system down and up.
3.	06-136R07	System Exercisor	This program tests memory operation through the DMA Port (Selector Channel is required for this test).

19. TROUBLE SHOOTING

19.1 Extender Board Operations

Use of 11-127 Extender Board allows convenient troubleshooting of the Model 80 Main Memory. It allows extended operation of an MBC with one MSU. To operate memory on the extender, the Extender Board must be plugged into the card file slots assigned to the MBC (Slot 4). The 11-127 Extender Board accepts two mother boards. Either the MBC or MSU may be plugged into the top slot of the extender. However, if an MSU is on top, it receives the ribbon cable connectors normally assigned to the MBC. See Figure 23. Extra care is recommended when probing the MSU to prevent accidential shorts from damaging memory.

CAUTION

Before plugging and unplugging any memory boards, the 34-014 Memory Power Supply Power (ON-OFF) switch must be in the OFF position. This switch is located on the front panel of the 34-014 Power Supply.

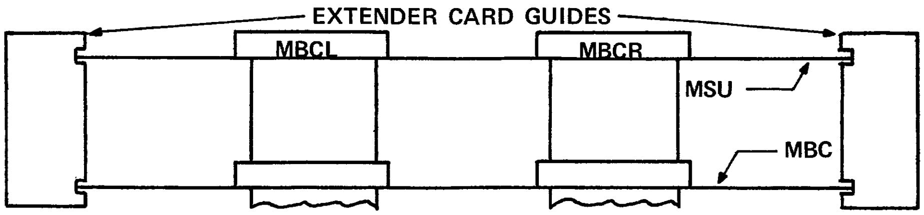


Figure 23. Cable Orientation for Memory on 11-127 Extender Board and MSU on Top

19.2 Troubleshooting Checks

If trouble develops and the Memory System is suspected, the following checks are recommended:

1. Proper seating of boards and connectors.
2. With Console Power switch in the ON position, measure all eight voltages used by the Memory System and compare them to Figure 22 in Section 17.
3. Place the system in the Standby Mode. Check P22, P5S, P8 and P3. (P3 should measure approximately 7 volts).
4. With the system in the Standby Mode, check all start signals from the MBC.

19.3 MOS Chip Waveforms

Figure 24 shows the normal waveforms present at the Driver terminals of the 6002 MOS Memory Chip.

19.4 Troubleshooting Driver Circuits

When failures occur and the drivers are suspected, using the typical resistance reading table may help to locate the problem. The most common failure occurs with a transistor being shorted or open in the particular circuit. Using an ohmmeter on its X10 range will detect these faults by checking from base to emitter, base to collector and emitter to collector for both forward and reverse conduction readings. When a transistor fails in the reset circuit, it almost always destroys the other transistor. Therefore, replacement of both transistors in the circuit when a failure occurs is usually required. Many times the damaging resistor is burned or changes value when transistor failures occur. When the driver is not functioning properly and the transistors check good, replace the over-drive or AC coupling capacitor in the circuit. If these capacitors open, they cause poor output rise and fall times. If the problem still exists, the TTL input should be compared to that of a known good driver. Difference here denotes a TTL IC replacement.

19.5 Model 80 MSU Resistance Checks

Use a Triplett 630 VOM or equivalent, with the timing daughter board installed on the MSU. The P22 to I/O reading need not be checked on every I/O as every I/O line is returned to P8 by two series connected 221 ohm resistors. Since this resistance is much lower than the 100 K normal resistance, it appears as a short from all I/O lines to P8. Therefore, checking P8 to P22 detects any faults on the I/O lines. It has been found that a 19-076 memory chip may breakdown (after running at an elevated temperature) from chip select to one of its I/O lines. This produces a resistance of 100 ohms from chip select to the affected I/O line which normally reads 100 K.

Typical resistance readings with timing board on the MSU.

+ Probe	- Probe	Reading
P22	Gnd.	50 K
	P8	200 K
	Address	2.8 K
	Reset	10 K
	Chip Select or Clock	2.6 K
	I/O	100 K (P8 will check all)
I/O	P8	400 K
Address	Gnd.	50 K
Reset		50 K
Chip Select or Clock		50 K
I/O		50 K (P8 will check all)
P8	-V (Pin 13 of Sense Amplifier)	3.7 K
+V (Pin 14 of Sense Amplifier)	P8	3.0 K
A50 Pin 14	Pin 7 (P5S-1)	100 ohms on X1 scale
A32.8 Pin 14	Pin 7 (P5)	100 ohms on X1 scale
A1-14	A1-07 (P5S-2)	50 ohms on X1 scale
A1-14	A32.8-14 (P5S to P5)	200 ohms on X1 scale
P15	Gnd.	
P8	Gnd.	20 K
Chip Select	I/O Breakdown	100 ohms on X10 scale

Notes: *All readings are on X1000 scale except noted. All readings taken with the MSU out of the system are 100 K when normal.

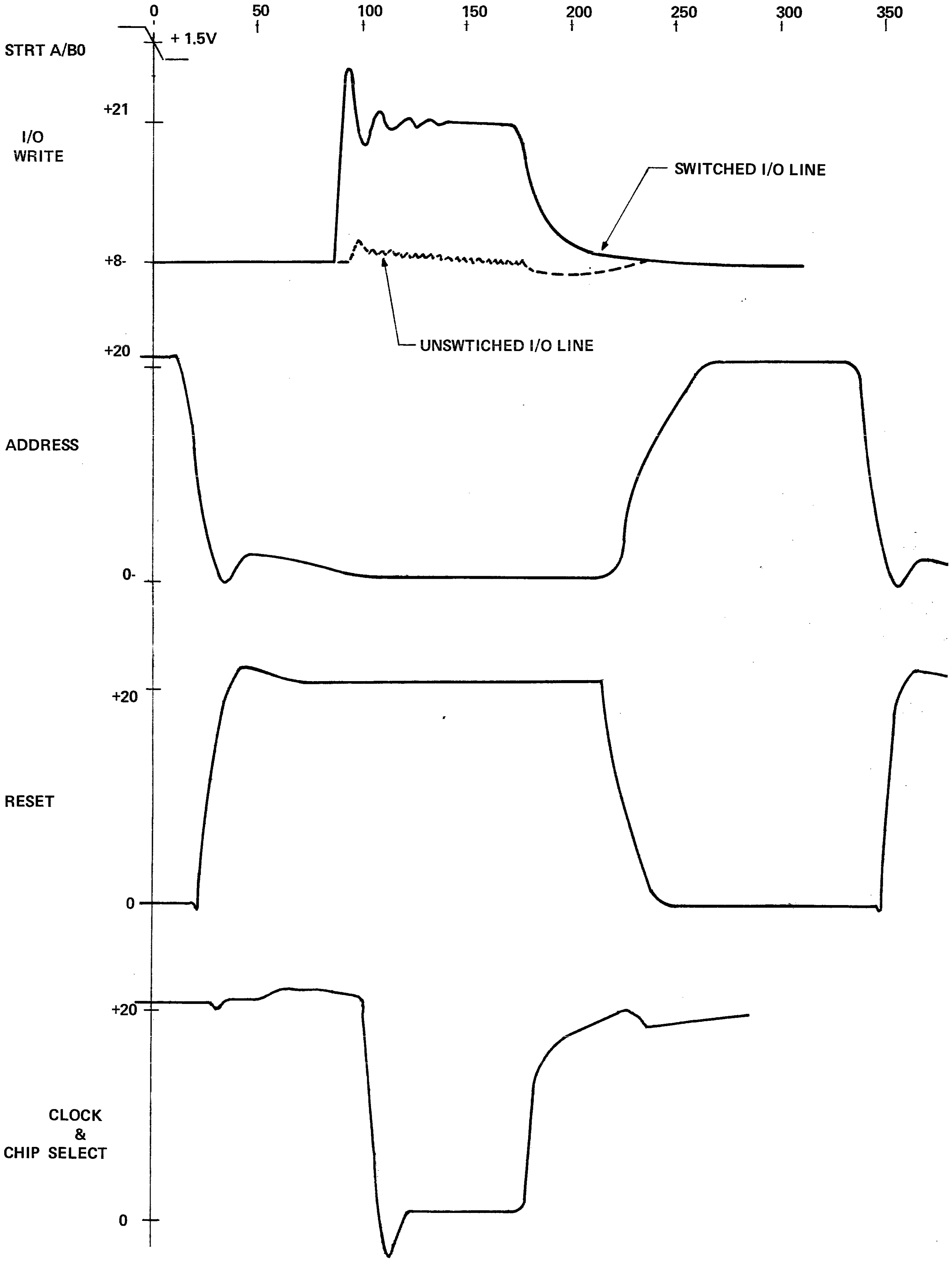
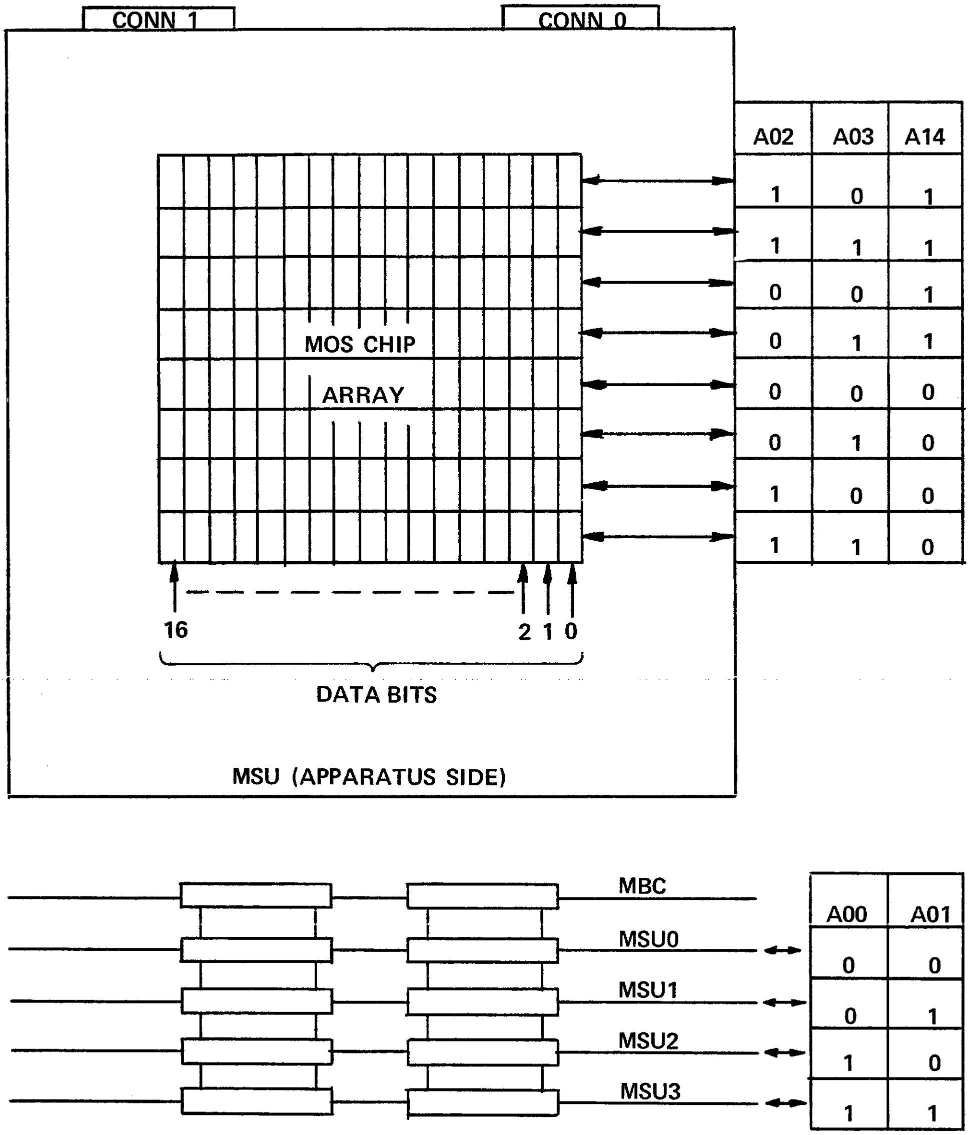


Figure 24. Driver Circuits and I/O Waveforms

19.6 Physically locating failing MOS Chips from failing address

Figure 25 shows the MSU with its MOS Chip Array. Each horizontal row of chips is associated with its accessing address condition by an arrow. Each vertical row of MOS Chips is associated with its corresponding data bit by an arrow. Each MSU is associated with its corresponding address by an arrow.



A02	A03	A14
1	0	1
1	1	1
0	0	1
0	1	1
0	0	0
0	1	0
1	0	0
1	1	0

	A00	A01
MSU0	0	0
MSU1	0	1
MSU2	1	0
MSU3	1	1

Figure 25. Physically locating failing MOS Chip from failing address

20. TIMING ADJUSTMENT

A timing adjustment is performed on all MSU boards at the factory. The timing adjustment selects one of two possible sets of wire strapping. The Timing Board Schematic (part of 02-247D08) includes a table that shows the strapping permitted. If an IC or delay line is replaced on the MSU timing board, this adjustment should be checked and re-adjusted, if necessary. The procedure is:

1. Remove Set One strapping if so wired.
2. Wire Set Two strapping.
3. Run memory with any test program.
4. Measure strobe delay. Strobe delay is measured from leading edge of STRA00 (6A6) to leading edge of STRB1 (3S7).
5. If strobe delay is less than 150 nanoseconds use Set Two.
6. If strobe delay is greater than 150 nanoseconds, use Set One strapping.

21. INSTALLTION

Mechanical installation of Model 80 memories is covered by Model 80 Installation Specification, 01-053A20. After the equipment is mounted and connected, the following checks should be performed:

1. Unplug the memory boards (MBC and MSUs).
2. Adjust the system voltages as follows:

   P5 to + 5.1 volts
   P15 to + 15.4 volts
   N15 to - 15.4 volts
   P22 to + 21.0 volts
   P5S to + 5.1 volts (Normal Mode)

3. Power down (memory power supply also), insert memory boards and plug in cables.
4. Power up and check voltages again, readjust if necessary.
5. If a parity system initialize memory with 06-144 Parity Initialize tape.
6. Run Memory Retention Test tape 06-143 at nominal voltages.
7. Run Memory Test tape 06-003 at P22 volts of 19.5 and 22.5 volts. When complete, readjust P22 to 21.0 volts.
8. If the system is equipped with a SELCH, run 06-136 System Exerciser Test tape.

22. MBC MNEMONICS

The following list provides a brief description of each mnemonic found in the MBC. The source of each signal on Functional Schematic 02-247D08 is also provided.

MNEMONICS	MEANING	SCHEMATIC LOCATION
ADD0	This signal is active only on CPU Instruction Fetch cycles when the CPU Port Address Bus Bit 14 (CA140) is low. It increments the MBC A Address Register (also a counter).	3E7
ARST1	Resets the MBC A and B Address Register Bits 00 and 01. It is active for the duration of a Refresh Memory cycle and at the end of all other memory cycles.	3J5
CBLK0	CPU Block - This signal is active for a short time (approximately 50 nanoseconds) following each CPU or Refresh cycle. When it is active, it blocks the CPU Request from being recognized by the MBC Interlock circuits.	2F7
CB000:020	CPU Bank Address - Not used by Standard Memory System.	Sheet 3
CCUE1	CPU Port Request signal (CREQ0) inverted.	3F2
DBK0	Goes low following every CPU or Refresh cycle for about 50 nanoseconds. Guarantees DMA Port a chance to get next memory cycle.	4L5
DCUE1	Output of a flip-flop which registers a DMA Request.	2E3
DLA000:500	Timing signals (11) derived from a 50 nanosecond delay line with 5 nanoseconds taps. Triggering of this line is caused by End of Cycle (ENDCYL0) received from the MSU. Delay Line A is active only on DMA or CPU Read cycles. On Instruction Fetch cycles, this line is triggered twice. (two read-outs).	Sheet 4

MNEMONICS	MEANING	SCHEMATIC LOCATION
DLC000:100	Timing signals (11) derived from a 100 nanosecond delay line with 10 nanoseconds taps. All timing from this line is referenced to the Delay Line Trigger (DLTRG1) signal which triggers the line every memory cycle.	Sheet 4
DL001:151	True output from MBC Data Register.	Sheets 5 and 6
DLTRG1	Delay Line C Trigger - This signal is active for the entire time the memory is busy doing any cycle. Its leading edge triggers Delay Line C which generates timing signals.	2M3
DRST0	This signal is active at the beginning of every cycle. It causes MDRST0 which resets the MBC Data Register.	4H3
END0	This clears the MBC circuits at the end of any memory cycle. It is derived from ENDCYL0 received from the MSU. Its duration is approximately 50 nanoseconds.	2L2
END0 B, C, D, E, F, and H	These signals are identical to END0 except they are delayed about 10 nanoseconds. Delay is derived by requiring the start flip-flops be cleared before activation.	Sheet 3
ENDST0	This signal goes low 30 nanoseconds after any Select signal (SR1B, SCSTR1 or SDSTR1). It determines the trailing edge of the Select Address signals (SCA1 or SDA1).	3H4
FETCH0	Output of flip-flop which registers the CPU Port Instruction Fetch signal (CFTCH0).	2E1
LRA1	Active every Refresh cycle. It loads the Refresh Address Counter (RA09:13) into the MBC A and B Address Registers (Bits 09:13 only).	4H6
MB000:020	DMA Bank Address - Not used by Standard Memory System.	Sheet 2
MDRST0	Memory Data Reset - This signal is active at the beginning of every cycle and the end of every Read cycle. It resets the MBC Data Register. It is active three times on a Fetch cycle - At the beginning of the cycle and following both Read-outs from the MSU.	4N4
MRDY1	Memory Ready - Enables various circuits within the MBC once the system is in the Normal Mode. In the Standby Mode, MRDY1 disables these circuits. Becomes a constant high in Normal Mode.	4D8
MRR1	Memory Ready - Enables DMA Port and CPU Port related circuits once the system is in the Normal Mode. In Standby Mode MRR1 disables communication with the CPU or DMA Ports. Becomes a constant high in Normal Mode.	4D7
MRST0	Initializing signal for P5S Power circuits within the MSU and MBC. This signal is low any time P5S is below 4 volts. It is a constant high in Normal Mode.	7S8
MRST1	Derived from P5S goes low after P5S has reached operational level (> 4.75 volts). It is a constant low in Normal Mode.	7S8
MWRT1	True output of MBC Write flip-flop which is set for DMA or CPU Write cycles.	8N8
PERR1	Parity Error - High if data in the MBC Data Register Fails the even Parity check.	9R3

MNEMONICS	MEANING	SCHEMATIC LOCATION
PFTCH1	Active on Fetch operations. Causes Parity Failures to generate IPF0 (Instruction Parity Failure) rather that DPF0 (Data Parity Failure).	3E8
PON0	This signal is low when the Memory Protect Control board enables the MBC Protect circuit (generated by Memory Protect Controller board).	8F7
PRT0	If the Protect feature is enabled, all memory address locations being accessed are checked by the MBC to see if they are a Protected location. PRT0 is a low active signal which indicates a Write cycle has been attempted at a protected address.	8N6
PVMD0	This signal is low when the Processor enables the MBC Protect circuits (Processor generated).	8F7
REN1	Refresh Enable - In Standby Mode enables Refresh Burst after P5S has reached operating level.	4C8
RREQ1	Refresh Request - Generated by MBC - causes a Refresh cycle to be generated. Goes active every 50 nanoseconds in Normal Mode.	4N8
SCA1	Select CPU Address - Loads the CPU Port's Address Bus into both MBC Address Registers (A and B).	2N7
SCR1	This signal is active on a CPU Read or Instruction Fetch cycle. It gates the MBC Data Register to the CPU Port Address Bus (CA00:14). Time duration is about 50 nanoseconds. On a Fetch, SCR1 is active twice, the second follows the first by 150 nanoseconds.	3N8
SCSTR1	Select CPU - This signal is active the entire time the memory is busy doing a CPU cycle.	2N6
SCW1	Active every CPU Write cycle. It loads the CPU Data Bus (CD00:15) into the MBC Data Register.	4H2
SDA1	Select DMA Address - Loads the DMA Port's Address Bus into both MBC Address Registers (A and B).	2M5
SDR1	This signal is active on a DMA Read cycle. It gates the Read-out registered in the MBC Data Register to the DMA Port Address Bus (MA00:14). Time duration is approximately 50 nanoseconds.	3N6
SDSTR1	Select DMA - This signal is active the entire time the memory is busy doing a CPU cycle.	2M5
SDW1	Active every DMA Write cycle. It loads the DMA Data Bus (MSD00:15) into the MBC Data Register.	4H3
SROB	Select Refresh - This signal is active the entire time the memory is busy doing a Refresh cycle.	2N2
SSTR0	Second Start - Sets Second Start in a Fetch operation - Timed by FECLK0 received from the MSU.	3J9
STRA1 STRB1	Output of the two Start latches (A and B). The start signals sent to the MSUs are derived from these two flip-flops. The states of Requesting Port's Address Bus Bit 14 determines which Start latch becomes active when a memory cycle is performed.	3E7

MNEMONICS	MEANING	SCHEMATIC LOCATION
TBA	Constant high generated by pull-up Resistor to P5.	Sheets 2:9
TBS	Constant high generated by pull-up Resistor to P5S.	
TS	Constant high generated by pull-up Resistor to P5.	
X113	A constant high in standard MBC.	2G8
X118	This signal is set low any time the MBC Interlock circuit has a Memory cycle queued in its three Queue flip-flops.	2J7
X241	This signal is set high in Fetch cycle only. It enables generation of Fetch Address (FAD0) and sets second Start (SSTR0) signals.	2G4
X162	This signal is set high by the MSU End of Cycle pulse if the cycle is a DMA Read. Delay Line A timing causes X162 to go low.	3K4
X164	This signal is set high by the MSU End of Cycle pulse if the cycle is a CPU Read or Fetch. Delay Line A timing causes X164 to go low.	3K3
X229	Time-out Signal - This signal goes low whenever MSU answers the MBC start signal with an End of Cycle pulse (ENDCYL0). For example: if a memory cycle is attempted at the address of FFFF and the system is equipped with only 32 KB of memory.	3K2
X261	Goes low in Refresh cycles causing both Start latches (A and B) to set.	4C5

23. MSU MNEMONICS

The following list provides a brief description of each mnemonic found in the Model 80 Memory Storage Unit. The source of each signal on Functional Schematic 02-247D08, is also provided.

MNEMONICS	MEANING	SCHEMATIC LOCATION
AA02:03 AB02:03	Address Bits 2 and 3 from the MBC to Memory A or B. These bits (decoded) are ANDed with Chip Select A (CSAPD1) or B (CSBPD1) to select one of four chip columns in the accessed half of memory (A or B).	6A8
AA04:13 AB04:13	Address Bits 4:13 from the MBC to Memory A or B. These bits are input to their corresponding address circuits in all MSUs in the Main Memory system.	Sheet 2
AAGT1	Gates A Address to the A half MOS Chip Array of the selected MSU.	6C3
ABGT1	Gates B Address to the B half MOS Chip Array of the selected MSU.	6C4
CSAPD1	Chip Select A when enabled is ANDed with AA02 and AA03 to select one of the four chip columns in accessed Memory A.	6G9

MNEMONICS	MEANING	SCHEMATIC LOCATION
CSBPD1	Chip Select B when enabled is ANDed with AB02 and AB03 to select one of the four chip columns in accessed Memory B.	6G9
DL00:16	Bi-directional data lines MBC/MSU Data Lines DL00:15 transfers data between the MBC and MSU. Data Line DL16 is used for parity.	Sheet 3
ENDCYL0	End of Cycle - Generated by the selected MSU and sent to the MBC. Signifies to the MBC that the MSU has finish the requested cycle.	6R6
FAD0	MBC generated pulse used by the selected MSU to initiate a second cycle during a CPU Instruction Fetch operation.	6A2
FAR0	This signal goes low to start the second cycle during an Instruction Fetch operation. Causes the inactive resets drivers to turn off and the inactive address drivers to be turned on.	6C2
FECLK0	Fetch Clock - A timing pulse generated by the MSU every cycle, but required only during Fetch cycles. Indicates to the MBC that it may send the second start signal.	6N5
GR1	Gate Reset - MBC generated pulse that forces all reset drivers off, in the main memory system, when not required. Conserves power in Standby Mode.	6A1
I0N00:16	Digit I/O line - Negative Digit I/O line - Raised to P22 when a "0" is written.	Sheet 3
IOP00:16	Digit I/O line - Negative Digit I/O line - Raised to P22 when a "1" is written.	Sheet 3
MWRT0A	Memory Write signal to the MSU.	6J8
QAA0 QAB0	Pulses low for 120 nanoseconds at the end of the cycle. This prevents consecutive A or B Memory cycles without having first provided 120 nanoseconds minimum reset time required by the MOS Chip.	6K2
RAGT0 RBGT0	Reset driver gates. When low these signals turn on the corresponding reset drivers (A or B).	6F2
RSTA0:3 RSTB0:3	Reset inputs to the MOS chips.	Sheet 2
SROB	Select Refresh - MBC generated signal which is active for the duration of all Refresh cycles. It forces all chip select drivers active.	6A7
STRA00:30 STRB00:30	Start signal from the MBC.	6A6
STRB1	Strobes the 16 sense digit circuits in the MSU. Enables 16 data bits to be read from the 16 addressed chips.	6S7
WRTGT1A WRTGR1B	These signals are input to the 16 Sense Digit circuits in the MSU. Enables Digit Write circuits on selected MSU.	6M7

MEMORY PROTECT

02-248A22
October 1972

MODEL 80 MEMORY PROTECT PROGRAMMING SPECIFICATION

1. INTRODUCTION

The 02-248 Model 80 Memory Protect provides a means of allocating selected blocks of memory to be protected from user writing. The Memory Protect Controller (MPC), in conjunction with a 64 bit mask-memory in the Memory Bank Controller (MBC), notifies the Processor via an interrupt whenever a Write operation to any location in a protected block is converted to a Read operation. A status bit in the MPC is also set. The memory is partitioned into 64 blocks with 1,024 bytes per block. Individual protect control for each block is provided by the 64 bit mask-memory. An overall protection override disables the protect function via the Memory Protect Controller. Note that the protect function is enabled at the Processor only when Bit 7 of the current Program Status Word is set. When Bit 7 is reset, all writes are treated the same as privileged writes; i.e., protect disabled.

The Model 80 MPC and the Model 70 MPC function the same except that the Model 80 MPC only operates with 1K bytes per block. Both controllers are programmed exactly the same.

2. CONFIGURATION

The Model 80 Memory Protect consists of the MPC board, a cable between the MPC and MBC boards, and the mask-memory circuits on the MBC board.

The Model 80 Memory Protect Controller is designed to operate with the Model 80 Memory Bank Controller. The Processor communicates with the MPC over the MUX-CH Bus to supply mask bytes and commands, to sense status, and to service interrupts. The MPC is normally installed as the highest priority device on the RACK0/TACK0 daisy chain including the built-in TTY Controller.

> NOTE
>
> It is imperative that the Memory Protect Controller have the highest priority on the Multiplexor Bus, to avoid ambiguity in identifying the source of a protect violation when executing interrupt routines with I/O interrupts enabled.

3. OPERATING PROCEDURES

Not applicable to the Model 80 Memory Protect.

4. DATA FORMAT

Refer to Appendix 1 for the definition of load mask bytes.

5. PROGRAMMING INSTRUCTIONS

The Output Command (OC or OCR) causes a command byte, as defined in Table 1, to be sent to the MPC. Any command causes all status except Protect On (PON) to be reset and the Load Mask Sequencer to be initialized. The Sense Status instruction (SS or SSR) is used to read the status byte, as defined in Table 1. The status byte reflects the operational state of the MPC. The least significant four bits (4:7) of the status byte are copied into the Condition Code of the current Program Status Word so they can be tested directly by the use of branch instructions.

The Write Data (WD or WDR), Write Halfword (WH or WHR), or Write Block (WB or WBR) instructions may be used to load the protect pattern into controller.

TABLE 1. MEMORY PROTECT STATUS AND COMMAND BYTES

BIT NO.	0	1	2	3	4	5	6	7
STATUS			PON	PWF		EX		
COMMAND	DISARM	ARM	PON	POFF				

STATUS

PON	Indicates that the protect is enabled at the MPC.
PWF	Indicates that an attempt was made to Write into a protected memory area. This bit is reset by any Output Command (OC), an Acknowledge Interrupt (AI) instruction or the system initialize signal SCLR0.
EX	Examine is set when PWF is set.

COMMAND

DISARM	Disarms the interrupts. They will not be queued.
ARM	Arms the interrupts.
PON	Enables the protect function at the MPC.
POFF	Disables the protect function at the MPC.

6. PROGRAMMING SEQUENCE

The setting up of the Memory Protect consists of loading the desired protect pattern into the controller, enabling the protect function, and either Arming or Disarming the interrupts. The Output Command initializes the load mask sequencer in the controller so that the first byte to the protect module, following the Output Command, loads the mask-register, Blocks 0:7. Refer to Appendix 1 for correspondence between the load mask bytes, block number and memory addresses protected. An active bit in the load mask protects the selected addresses. If more than eight bytes are used to load the mask-memory, wrap around occurs (i.e., the ninth byte once again loads Blocks 0:7).

After setting up the Memory Protect, Bit 7 of the Program Status Word must be set to enable the protect function at the Processor. When a protect failure occurs, the response to an SS or SSR instruction is X'34'.

7. INTERRUPTS

An interrupt can be used to signal the Processor that an attempt was made to write into a protected area in memory. In the Arm state, the interrupts are armed and enabled. Interrupts are blocked and not queued in the Disarm state.

When an interrupt is acknowledged by an Acknowledge Interrupt instruction (AI or AIR) the interrupt is cleared and all status bits except PON are reset. The normal status returned by an Acknowledge Interrupt is X'20'. Executing an Acknowledge Interrupt instruction when no interrupt is pending results in a device address of zero and a status of X'04 .

8. INITIALIZATION

During Power Up, Power Down, or whenever the Initialize (INT) switch on the Display Panel is depressed, the Memory Protect Controller is placed in the Disarm state with all status conditions reset. The Load Mask Sequencer is initialized, the Bank Register is cleared and the protect function is disabled at the controller.

9. DEVICE NUMBER

The Model 80 Memory Protect Controller is normally assigned device address X'AE'. This address can be reassigned by changing the address straps on the controller. Refer to the Installation Specification 02-248A20, for details.

10. SAMPLE PROGRAM(S)

Not applicable to the Model 80 Memory Protect.

APPENDIX 1
TABLE OF MEMORY ADDRESSES VS. BLOCKS

BLOCK	LOAD MASK DATA		MEMORY ADDRESSES (HEX)
	BYTE	BIT	1K BYTE
0	0	0	0000-03FF
1	0	1	0400-07FF
2	0	2	0800-0BFF
3	0	3	0C00-0FFF
4	0	4	1000-13FF
5	0	5	1400-17FF
6	0	6	1800-1BFF
7	0	7	1C00-1FFF
8	1	0	2000-23FF
9	1	1	2400-27FF
10	1	2	2800-2BFF
11	1	3	2C00-2FFF
12	1	4	3000-33FF
13	1	5	3400-37FF
14	1	6	3800-3BFF
15	1	7	3C00-3FFF
16	2	0	4000-43FF
17	2	1	4400-47FF
18	2	2	4800-4BFF
19	2	3	4C00-4FFF
20	2	4	5000-53FF
21	2	5	5400-57FF
22	2	6	5800-5BFF
23	2	7	5C00-5FFF
24	3	0	6000-63FF
25	3	1	6400-67FF
26	3	2	6800-6BFF
27	3	3	6C00-6FFF
28	3	4	7000-73FF
29	3	5	7400-77FF
30	3	6	7800-7BFF
31	3	7	7C00-7FFF
32	4	0	8000-83FF
33	4	1	8400-87FF
34	4	2	8800-8BFF
35	4	3	8C00-8FFF
36	4	4	9000-93FF
37	4	5	9400-97FF
38	4	6	9800-9BFF
39	4	7	9C00-9FFF
40	5	0	A000-A3FF
41	5	1	A400-A7FF
42	5	2	A800-ABFF
43	5	3	AC00-AFFF
44	5	4	B000-B3FF
45	5	5	B400-B7FF
46	5	6	B800-BBFF
47	5	7	BC00-BFFF

APPENDIX 1 (CONTINUED)
TABLE OF MEMORY ADDRESSES VS. BLOCKS

48	6	0	C000-C3FF
49	6	1	C400-C7FF
50	6	2	C800-CBFF
51	6	3	CC00-CFFF
52	6	4	D000-D3FF
53	6	5	D400-D7FF
54	6	6	D800-DBFF
55	6	7	DC00-DFFF
56	7	0	E000-E3FF
57	7	1	E400-E7FF
58	7	2	E800-EBFF
59	7	3	EC00-EFFF
60	7	4	F000-F3FF
61	7	5	F400-F7FF
62	7	6	F800-FBFF
63	7	7	FC00-FFFF

MODEL 80 MEMORY PROTECT CONTROLLER INSTALLATION SPECIFICATION

1. INTRODUCTION

This specification provides the necessary information for the installation of the 02-248 Memory Protect Controller (Product Number M80-101) in a Model 80 Processor System. The module assembly consists of one 35-408 7" board and one 17-192 cable. The 35-408 7" board must be strapped to a blank 7" board or an active 7" board (e.g., Universal Clock Module) by an INTERDATA 16-398 Half Board Kit, so that it may be installed in a chassis designed for standard 15" boards. The Memory Protect Controller (MPC) may be installed in either the right or left half position, depending on the system configuration. See Figure 1.

NOTE: 35-408 7" BOARD CAN BE LOCATED ON EITHER SIDE.

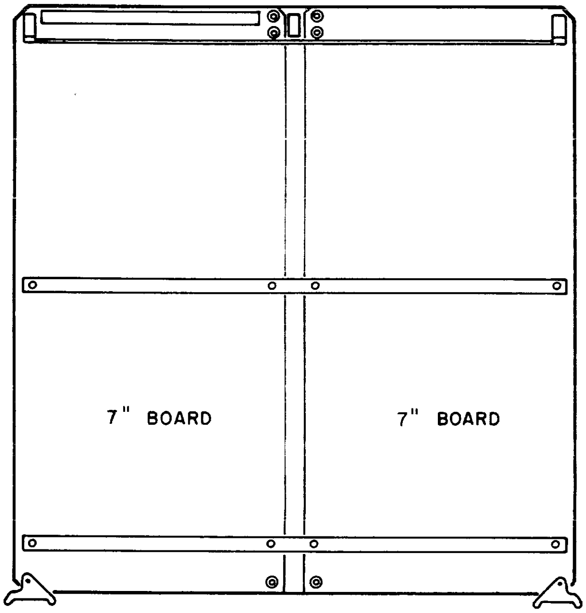


Figure 1. 7" Board Assembly

2. UNPACKING

When the Memory Protect Controller is shipped with a system, it is installed at the factory so there is no special unpacking procedure. If the module assembly is purchased separately, it should be inspected for damage prior to installation.

3. LOCATION

The 35-408 Memory Protect Controller 7" board, once assembled using a half board kit, may be installed in any available I/O slot of a standard 15" chassis which is located no more than one chassis from the Processor.

> NOTE
>
> Normally the Memory Protect Controller is installed as the highest priority device controller (with respect to interrupts) on the Multiplexor Bus to insure proper recognition and response to Memory Protect violation interrupts that may occur in the system. This is accomplished by installing the Memory Protect Module in the first available I/O slot with respect to the daisy chain priority line, and rerouting the RACK0/TACK0 line which is ordinarily connected first to the built-in Teletypewriter controller. See Section 4.

4. BACK PANEL WIRING

To insure that the Memory Protect Controller (MPC) has the highest priority on the Multiplexor Bus, the RACK0/TACK0 line on the Processor chassis back panel must be rerouted.

4.1 MPC Installed in I/O Expansion Chassis

1. Refer to Figure 2 during the following rerouting procedure. Remove the RACK0/TACK0 jumper from the slot occupied by the MPC. The jumper is located between Terminals 122 and 222 on the selected slot.
2. Break the daisy chain line from the next higher priority device controller and to the next lower priority device controller, at Terminals 122-1 and 222-1 on the MPC's selected slot. Connect the TACK0 Terminal 222-1 from the next higher priority device to the RACK0 Terminal 122-1 on the next lower priority device controller on the Multiplexor Bus. This removes the MPC from the daisy chain priority sequence, and re-establishes the daisy chain to lower priority device controllers.
3. Break the connection between Acknowledge Interrupt (ACK0) Terminal 222-0 and Teletypewriter Receive Acknowledge (RACK0) Terminal 238-1 on the I/O board, Slot 5. This disconnects the Teletypewriter device controller from the Acknowledge Interrupt (ACK0) line.
4. Connect a jumper between MPC RACK0 Terminal 122-1 and I/O board ACK0 Terminal 222-0. This connects the Memory Protect Module as the first device controller in the RACK0/TACK0 line.
5. Connect a jumper between MPC TACK0 Terminal 222-1 and I/O board Teletypewriter RACK0 Terminal 238-1. This connects the Teletypewriter as the second device controller in the RACK0/TACK0 line.

The MPC is now the highest priority device controller in the daisy chain. The built-in Teletypewriter device controller is second in priority and the remaining device controllers are as before in their required sequence.

4.2 MPC Installed in CPU Chassis

For systems with less than 64K bytes of memory, the MPC can occupy one of the I/O slots in the CPU chassis. Figure 3 shows the basic RACK0/RACK0 path normally wired onto the otherwise all copper back panel. With 48K bytes of memory, both halves of Slot 00 are available. Install the MPC as shown in Figure 4.

When the CPU chassis has less than 32K bytes of memory and a Selector Channel (SELCH) in Slot 00, the MPC is placed in Slot 01 as shown on Figure 5. In this case, both the MPC and the SELCH have higher priority than the console TTY since part of the daisy chain is in copper. With only 16K bytes of memory the MPC could occupy Slot 02, thus, permitting a priority chain of MPC/SELCH/TTY.

5. CABLE CONNECTION

Install the 17-192 cable between the 35-408 Memory Protect Controller (MPC) board and the 35-407 Memory Bank Controller (MBC) board. See Figure 6. The MBC is normally located in Slot 04 of the CPU chassis.

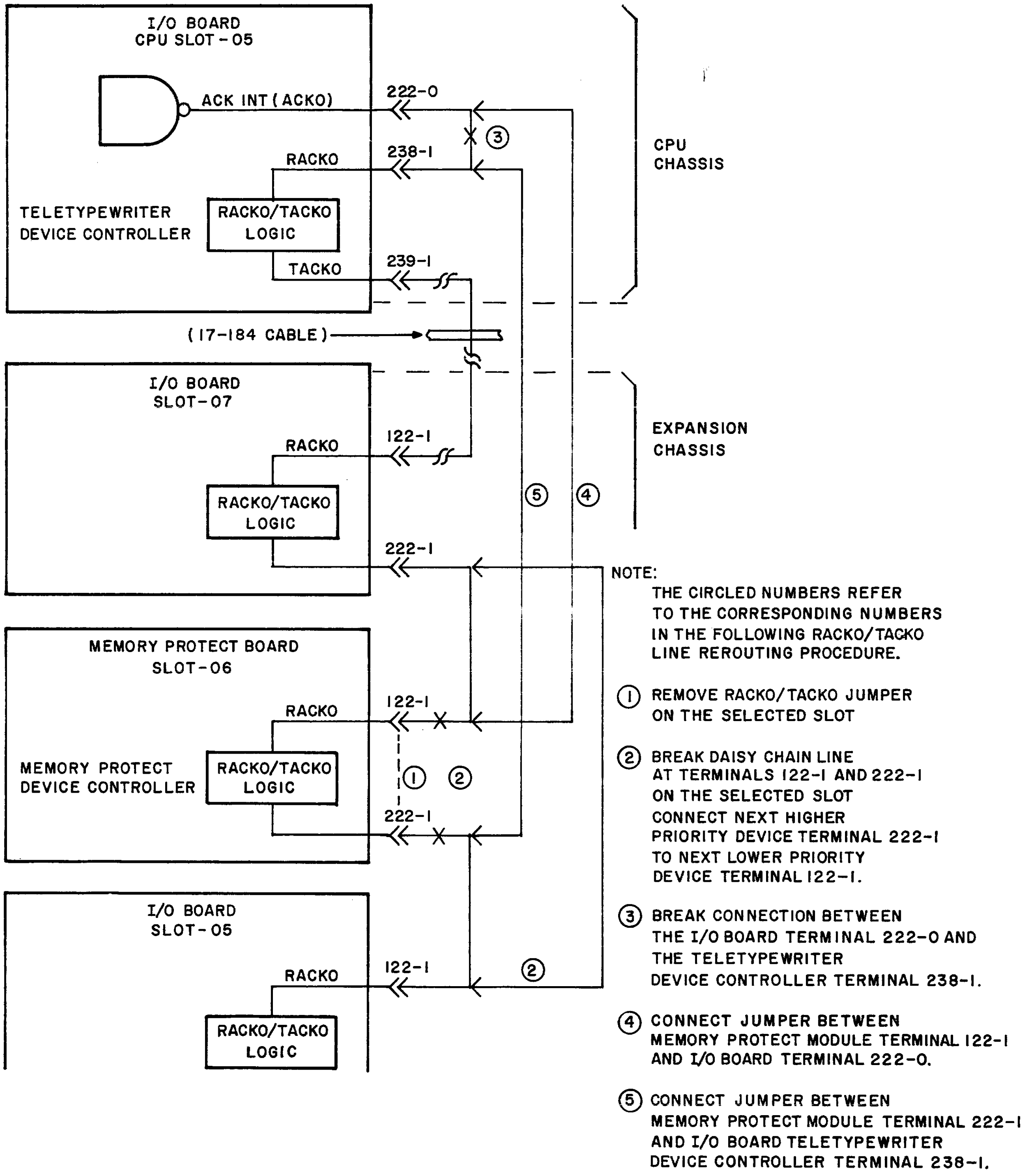
6. STRAP OPTIONS

6.1 Address Strapping

The preferred address of the Memory Protect Controller is X'AE'. The board is strapped for this address at the factory. To change the address, refer to Functional Schematic 02-248D08, Sheet 1.

NOTE

The alpha-numeric designations, referred to on the functional schematic, indicate similar designations on the apparatus side of the printed circuit board.


I/O BOARD
CPU SLOT - 05
ACK INT (ACKO)
222-0
③
RACKO
238-1
CPU
CHASSIS
TELETYPEWRITER
DEVICE CONTROLLER
RACKO/TACKO
LOGIC
TACKO
239-1
(17-184 CABLE)
I/O BOARD
SLOT-07
RACKO
122-1
EXPANSION
CHASSIS
RACKO/TACKO
LOGIC
⑤
④
222-1
MEMORY PROTECT BOARD
SLOT-06
RACKO
122-1
MEMORY PROTECT
DEVICE CONTROLLER
RACKO/TACKO
LOGIC
①
②
222-1
I/O BOARD
SLOT-05
RACKO
122-1
②
RACKO/TACKO
LOGIC

NOTE:

THE CIRCLED NUMBERS REFER TO THE CORRESPONDING NUMBERS IN THE FOLLOWING RACKO/TACKO LINE REROUTING PROCEDURE.

① REMOVE RACKO/TACKO JUMPER ON THE SELECTED SLOT

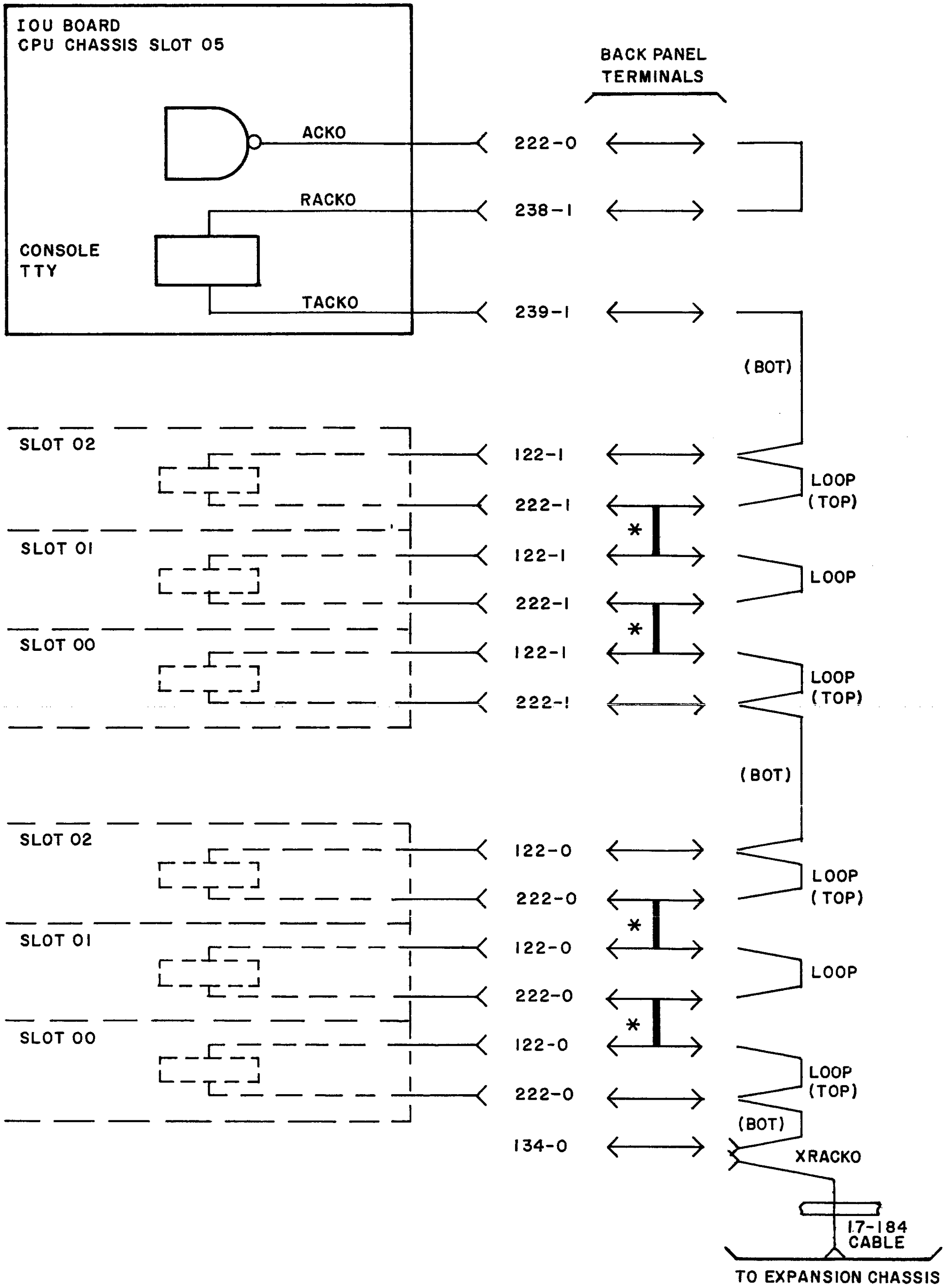
② BREAK DAISY CHAIN LINE AT TERMINALS 122-1 AND 222-1 ON THE SELECTED SLOT
CONNECT NEXT HIGHER PRIORITY DEVICE TERMINAL 222-1 TO NEXT LOWER PRIORITY DEVICE TERMINAL 122-1.

③ BREAK CONNECTION BETWEEN THE I/O BOARD TERMINAL 222-0 AND THE TELETYPEWRITER DEVICE CONTROLLER TERMINAL 238-1.

④ CONNECT JUMPER BETWEEN MEMORY PROTECT MODULE TERMINAL 122-1 AND I/O BOARD TERMINAL 222-0.

⑤ CONNECT JUMPER BETWEEN MEMORY PROTECT MODULE TERMINAL 222-1 AND I/O BOARD TELETYPEWRITER DEVICE CONTROLLER TERMINAL 238-1.

Figure 2. RACK0/TACK0 Rerouting with Memory Protect Module


IOU BOARD
CPU CHASSIS SLOT 05
BACK PANEL TERMINALS
ACKO
RACKO
CONSOLE TTY
TACKO
222-0
238-1
239-1
(BOT)
SLOT 02
122-1
222-1
LOOP (TOP)
SLOT 01
122-1
222-1
LOOP
SLOT 00
122-1
222-1
LOOP (TOP)
(BOT)
SLOT 02
122-0
222-0
LOOP (TOP)
SLOT 01
122-0
222-0
LOOP
SLOT 00
122-0
222-0
LOOP (TOP)
(BOT)
134-0
XRACKO
17-184 CABLE
TO EXPANSION CHASSIS
*
*
*
*

* PART OF COPPER BACK PANEL

Figure 3. Basic RACK0/TACK0 Wiring on Model 80 CPU Chassis

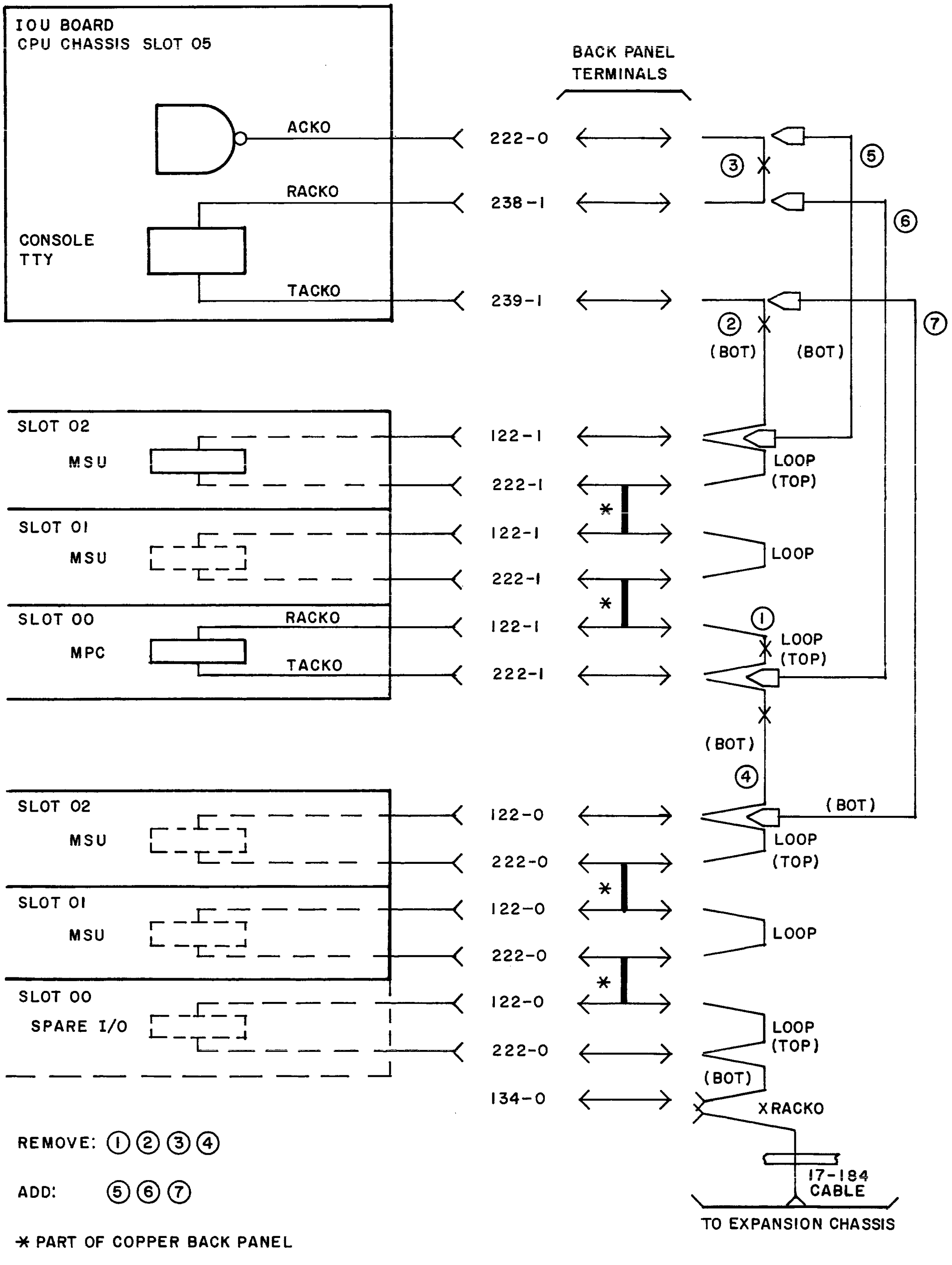

IOU BOARD
CPU CHASSIS SLOT 05
CONSOLE TTY
ACKO
RACKO
TACKO
BACK PANEL TERMINALS
222-0
238-1
239-1
③
⑤
⑥
②
⑦
(BOT)
(BOT)
SLOT 02
MSU
122-1
222-1
LOOP (TOP)
SLOT 01
MSU
122-1
222-1
LOOP
SLOT 00
MPC
RACKO
TACKO
122-1
222-1
①
LOOP (TOP)
(BOT)
④
SLOT 02
MSU
122-0
222-0
(BOT)
LOOP (TOP)
SLOT 01
MSU
122-0
222-0
LOOP
SLOT 00
SPARE I/O
122-0
222-0
LOOP (TOP)
(BOT)
134-0
XRACKO
17-184 CABLE
TO EXPANSION CHASSIS
*
REMOVE: ①②③④
ADD: ⑤⑥⑦
* PART OF COPPER BACK PANEL

Figure 4. System With 48K Bytes Memory MPC in Slot 00 (left)

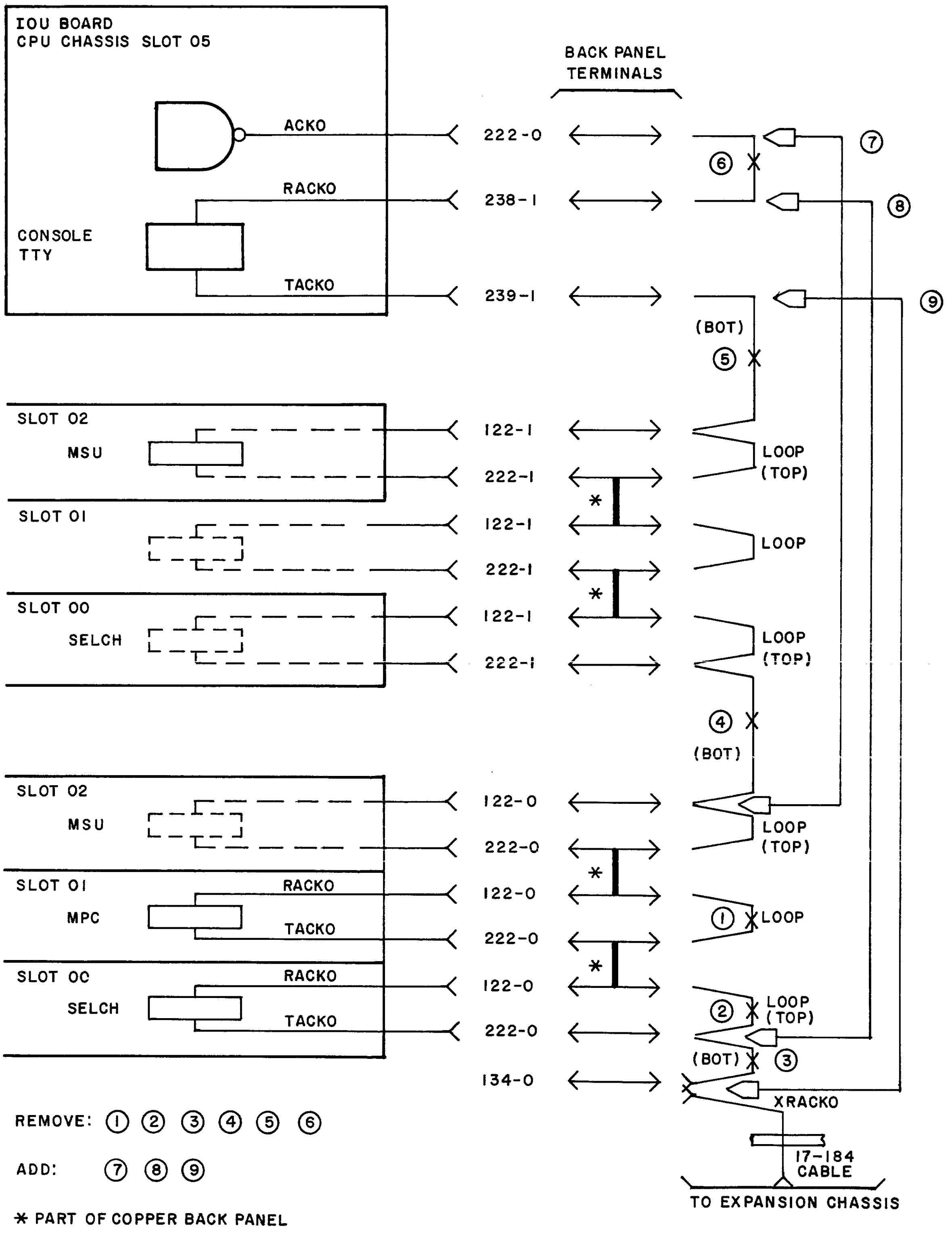

IOU BOARD
CPU CHASSIS SLOT 05
ACKO
RACKO
CONSOLE
TTY
TACKO
BACK PANEL
TERMINALS
222-0
238-1
239-1
⑥
⑦
⑧
⑨
(BOT)
⑤
SLOT 02
MSU
122-1
222-1
LOOP
(TOP)
SLOT 01
122-1
222-1
LOOP
SLOT 00
SELCH
122-1
222-1
LOOP
(TOP)
④
(BOT)
SLOT 02
MSU
122-0
222-0
LOOP
(TOP)
SLOT 01
MPC
RACKO
TACKO
122-0
222-0
①
LOOP
SLOT 00
SELCH
RACKO
TACKO
122-0
222-0
②
LOOP
(TOP)
(BOT)
③
134-0
XRACKO
17-184
CABLE
TO EXPANSION CHASSIS
*
REMOVE: ① ② ③ ④ ⑤ ⑥
ADD: ⑦ ⑧ ⑨
* PART OF COPPER BACK PANEL

Figure 5. System with 32K Bytes Memory MPC in Slot 01 (right) and SELCH in Slot 00

6.2 Block Size

There is no block size option on the Model 80 Memory Protect feature. The protect mask-memory, located on the MBC board is wired for 1,024 byte blocks.

7. INSTALLATION CHECKS

To insure proper operation of the Model 80 Memory Protect, Test Program 06-135 should be executed in accordance with its test program description.

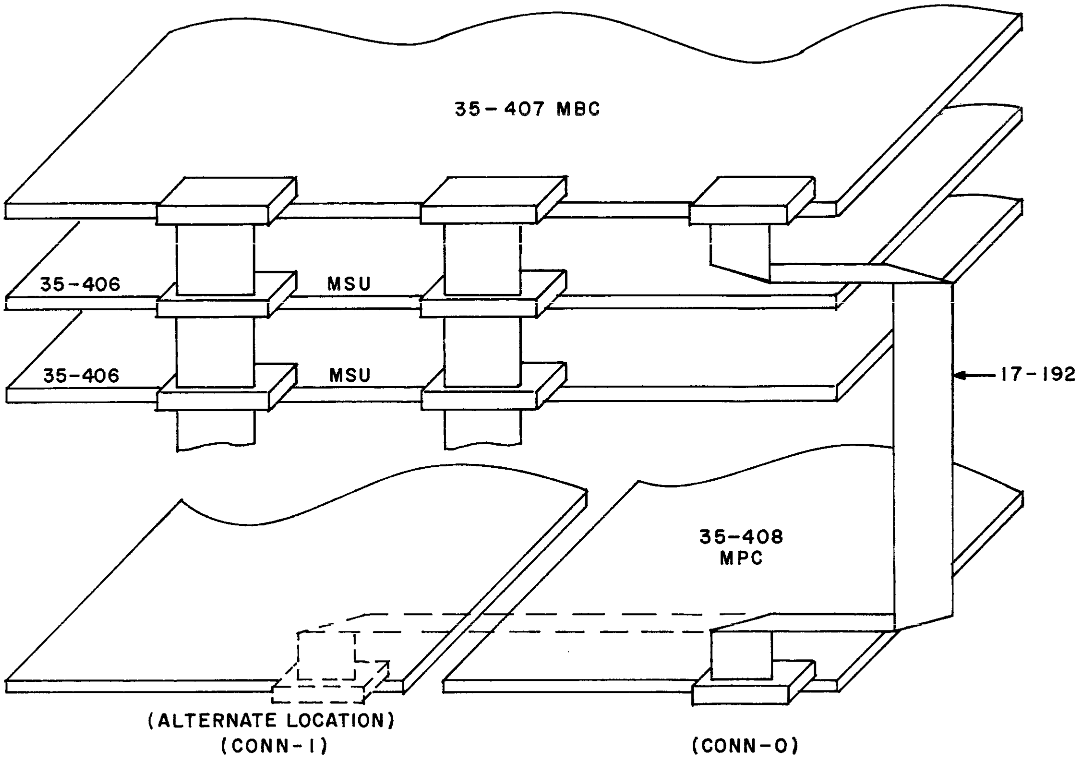

35-407 MBC
35-406
MSU
35-406
MSU
17-192
35-408
MPC
(ALTERNATE LOCATION)
(CONN-1)
(CONN-0)

Figure 6. Cable Connection

02-248A21
October 1972

MODEL 80 MEMORY PROTECT CONTROLLER MAINTENANCE SPECIFICATION

1. INTRODUCTION

The 02-248 Model 80 Memory Protect Controller (MPC) provides a means of allocating selected blocks of memory to be protected. The MPC, in conjunction with the 64 bit mask-memory located on the Memory Bank Controller (MBC) board, notifies the Processor (via an interrupt) whenever a Write operation to any location in a protected block is converted to a Read operation. A status bit in the MPC is also set. The memory is partitioned into 64 blocks of 1,024 bytes per block. Individual protect control for each block is provided by the 64 bit mask-memory on the MBC. An overall protection override permits the loading of any area in memory.

The Model 80 Memory Protect consists of the MPC board, a cable between the MPC and the MBC boards, and the mask-memory circuits on the MBC board. Refer to the Installation Specification 02-248A20, for the necessary installation information.

2. SCOPE

This specification describes the functional operation of the Memory Protect Controller; specifically, the circuits for Multiplexor (MUX) Channel communication, for loading the MBC mask-memory via a cable, and for registering protect override and failure conditions. It does not cover the operation of the mask-memory and the associated circuits located on the MBC board. Refer to Maintenance Specification 02-247A21, for this information.

3. BLOCK DIAGRAM ANALYSIS

Refer to the block diagram of the Memory Protect Controller (MPC) on Sheet 1 of Functional Schematic 02-248D08.

The protect mask-memory (16 words, 4-bits per word) is loaded by a series of 16 clock pulses, Write Clock (WCLK0), each accompanied by a 4-bit mask word, a 4-bit word address, and a 3-bit bank address. The bank address, which will be implemented on future systems, is normally all zeros. The 64 bit mask is provided by eight Data Available (DA) operations over the Multiplexor Channel (MUX-CH) Bus using normal address and synchronization sequences. Each DA loads the 8-bit Mask (Shift) Register where alternate stages feed four cable drivers. The Timer, which starts on the end of LD1, enables the cable drivers, generates two Write Clocks and then shuts off. At the end of the first clock pulse, a right shift of the Mask Register moves the other four bits into the output stages connected to the cable drivers.

The four stage address counter is cleared by any Command (CMD) signal and advances on the end of each clock pulse. If more than eight DA's are received without a CMD, the counter will "wrap around" and reload the least significant block bits.

The most significant bit of the first DA (D08) corresponds to the least significant block to be protected; i.e., the low end of memory. Bits 08, 09, 10 and 11 are sent as the first mask word and stored in the lowest address of the mask-memory. After the first clock pulse, Bits 12, 13, 14 and 15 are connected to the cable drivers to form the second mask word.

Since the protect bits are not usable until they are loaded into the MBC Mask Memory, the SYN0 signal is not returned to the Processor until the timer shuts off.

The Protect On (PON0) signal, from one of the control flip-flops, activates the protect circuits in the MBC. It is removed to permit writing in all areas of the main memory. The protect circuits in the MBC may also be deactivated independently by Bit 7 of the CPU Program Status Word (PSW).

An attempt to write in a protected block of memory produces the PRFL1 pulse from the MBC. This pulse sets the ATN and PWF control flip-flops.

Three bits of status or eight bits of device address are gated to the MUX-CH bus in response to a Status Request (SR) or an Acknowledge Interrupt (AI) operation.

4. FUNCTIONAL SCHEMATIC ANALYSIS

This section refers to Functional Schematic 02-248D08.

4.1 Multiplexor Channel Bus Communications

The MPC is a byte-oriented device which transfers data to and from the MUX-CH Bus on Data Lines D08:15. Signals from the Multiplexor Bus are received, buffered and presented in double rail form at 16 terminals (2F1-2F5) designated by letters A through S. The preferred device address (X'AE') is set up with eight straps as shown on Sheet 2. The buffered receive data lines (2C1-2C5) are also connected to the Mask Register and Bank Register (Sheet 3) and to the logic for the PRON (2L1) and ARM (2M7) control flip-flops.

When the received byte corresponds to X'AE', all Address Gate lines AG081:151 are active high producing active states on lines A0 and A1 (2K3). The Address flip-flop (AD) (2L3) toggles set on the trailing edge of the ADRS1 signal, and the ADSYN0 line (2M4) goes active to generate the SYN0 signal (2H7). With the AD flip-flop set, the other control line receivers are enabled by AD1 (2A8) and GAD1 (2C6). The GAD1 lead, which gates the CMD1 and DDA1 signals, is active when the timer is off (XB cleared) and the MPC is addressed (AD set). On all addresses other than X'AE', the Address flip-flop (AD) is toggled clear. It is also direct cleared by the system initialize signal SCLR0A (2J2).

Status and acknowledge address bits are gated to the MUX-CH lines D08:15 by 19-036 open-collector gates (e.g., 2H1, 2H2, 2M4, etc.).

4.2 Status and Commands

Table 1 shows the bit assignments for the MPC status and command bytes.

TABLE 1. MEMORY PROTECT CONTROLLER STATUS AND COMMAND BYTE DATA

BIT NO.	0	1	2	3	4	5	6	7
STATUS			PON	PWF		EX		
COMMAND	DISARM	ARM	PON	POFF				

STATUS

PON	Indicates that protect is enabled at the MPC.
PWF	Indicates that an attempt was made to Write into a protected memory area. This bit is reset by any Output Command, an Acknowledge Interrupt instruction, or the system initialize signal SCLR0.
EX	Examine is set when PWF is set.

COMMAND

DISARM	Disarms the interrupts. They will not be queued.
ARM	Arms the interrupts.
PON	Enables the protect function at the MPC.
POFF	Disables the protect function at the MPC.

The ARM flip-flop (2M7) is direct set or cleared by CMG1 depending upon the signals on D08 and D09. It is also cleared by the system initialize signal SCLR1 (2L7).

The Protect On flip-flop (PRON) (2L1) toggles set or clear at the end of CMG1 according to the state on D10 and D11. This flip-flop does not change state if both the J and K inputs are low. The PRON flip-flop is direct cleared by the SCLR0A signal. The output lead PRON1 is sent to the MBC circuits via cable line PON0 (2M2) and is gated to the MUX-CH Bus (Bit 10) (2R4 and 2M2) by the Status Request signal SRG1 (2K4). It also gates the cable receiver output PRFL1 (3L2).

When a protect failure condition is detected on the MBC, the received PRFL0 pulse forces the PRFL1 and ASATN0 lines to the active state to direct set the ATN (2J8) and PWF (2J7) flip-flops. The output lead, PWF1, is gated to the MUX-CH Bus (Bits 11 and 13) (2M5) by the SRG1 signal. The PWF flip-flop toggles clear at the end of an Acknowledge Interrupt operation (ATSYN1) or is direct cleared by the CL0 line. The latter is active when either SCLR1 or CMG1 (2G9) are in the high active state.

4.3 Acknowledge Interrupt

When the MPC is Armed and the ATN flip-flop has been set, the Gated Attention line (GATN1) (2M8) goes high to send an interrupt to the MUX-CH Bus on the ATN0 line. The Processor responds by activating its ACK0 output which is normally wired directly to the Memory Protect Controller (MPC) RACK0 (2L8) as described in the Installation Specification 02-248A20. When RACK1 (2M6) goes high, preceded by GATN1, the ATSYN0 (2S5) and ATSYN1 (2H8) lines become active and SYN0 is returned to the Processor. The TACK0 line (2S6) does not respond. Both the PWF and ATN flip-flops toggle clear at the end of ATSYN1.

While ATSYN0 (2A6) is low, the eight true Data Lines (D081:151) are forced high and the false Data Lines (D080A:150A) are forced low. These conditions passing through the address straps result in a bit pattern on the Address Gate Lines (AG081:151) which corresponds to the MPC address byte; i.e., X'AE'. The ATSYN1 signal gates the AG lines to the MUX-CH Bus to return the device address to the Processor.

When the MPC does not have an interrupt registered, the GATN1 line is low and the RACK0 signal is passed through the contention circuit (2N6) and appears on the TACK0 line. Should RACK1 and GATN1 become active at the same time, the delays in the circuit insure that either ATSYN0 or TACK0 is selected but not both.

4.4 Output Circuits

The general operation of the Timer, Address Counter, and Mask (Shift) Register is described in Section 3. During the following functional analysis refer to Functional Schematics 02-248D08 Sheet 3.

4.4.1 Mask Register. The Mask Register, composed of a pair of 19-030 Shift Registers (3H4 and 3H6), is loaded at the beginning of the DAG1 signal, by a short Load Pulse (LD1), with the data bits interleaved as shown. The four bit mask word (DM01, 11, 21 and 31) comes from every other stage of the register and is gated to the MBC cable whenever the Write Enable (WEBL0) line is activated.

4.4.2 Timer. A pair of flip-flops, XA (3D3) and XB (3D4), together with a multivibrator, TMA (3B7) and TMB (3D7), make up the Timer circuit. As shown on Figure 1, the load pulses (LD0 and LD1) are generated by the overlap of the inverted and delayed copies of DAG0 (3C1). The XB flip-flop is direct set by the leading edge of LD0 and blocks the usual return of SYN0 by a low level on the GAD1 line (2C6 and 3E6). The XA flip-flop toggles set on the trailing edge of LD1. The multivibrator, enabled by XA1 and DXA0, produces a pair of TMB pulses which increment the Address Counter (TMB0) (3H9), shift the Mask Register (SHFT1) (3F7), and generate the Write Clock (WCLK0) (3M2) signal on the cable. The Write Enable signal (WEBL0) (3M3) is active whenever the XB flip-flop is set.

The leading edge of the second TMB pulse direct clears the XA flip-flop while XB toggles clear at the end of the second TMB pulse (due to the high-to-low transition on KA1). Both XA and XB are direct cleared by CL0 or CL1 which are active when either SCLR1 or CMG1 (2K9) are active.

When the XB flip-flop is cleared, GAD1 becomes active and gates the DDA1 signal (2A7 and 3F1) to the SYN0 line of the MUX-Bus.

4.4.3 Address Counter. The Address Counter (19-035) (3H8) generates the complement of the mask word address (KA0, KB0, KC0 and KD0) which is gated to the MBC cable in true form (WSA1, WSB1, WSC1 and WSD1). This inversion is performed to eliminate a set of inverter gates on the MBC board. The CL0 pulse (3G9) loads the counter with four high levels to form the complement of the all-zeros starting address. The trailing edge of each TMB0 pulse decrements the counter (in a true sense) causing the true cable signals to increment.

4.4.4 Bank Register. The optional, three bit Bank Register (19-071) (3H1) is loaded from D13, D14 and D15 with an Output Command and is gated to the MBC cable by the XB0 output from the XB flip-flop (3E5). It is cleared by the system initialize signal SCLR0A. In the normal single bank memory system the register and cable drivers are not equipped. The cable lines BP000, BP010 and BP020 (3M4) are all high to specify Bank 0.

4.4.5 Protect Failure. When a protect failure is detected on the MBC board, the PRFL0 (3M1) line carries a low active pulse. The signal is terminated, inverted and gated to set the PWF and ATN flip-flops as described earlier.

4.5 System Initialize

The system initialize signal (SCLR0) (1A8) clears all control and timer flip-flops. This sets up the MPC as Disarmed, Protect Off, not addressed and no PWF or ATN registered. The Bank Register is cleared and the Address Counter loaded to place the all zero mask word address on the cable when enabled. The Mask Register is not affected.

5. TIMING

The components used on the MPC set the TMA and TMB pulse widths at approximately 100 nanoseconds. The Timer is active (XB set) for approximately 700 nanoseconds. Timing relationships are shown in Figure 1.

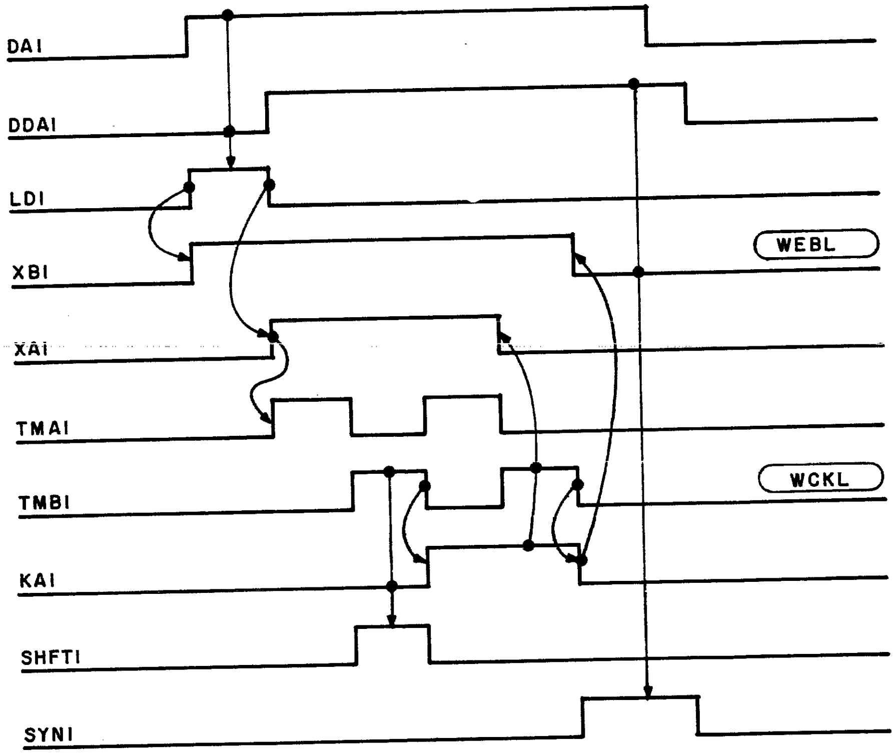


Figure 1. MPC Timing

6. MAINTENANCE AND TESTS

The Memory Protect Controller requires no adjustments. Before attempting any maintenance or testing, insure that the cable and controller are installed properly. Refer to the Installation Specification 02-248A20, for necessary installation information.

To test the Model 80 Memory Protect Controller, run the Memory Protect Test 06-135 (Model 70/80 MPC test program) in accordance with its test program description.

A list of five test points is shown on Sheet 1 of Functional Schematic 02-248D08.

7. MNEMONICS

The following list provides a brief description of each mnemonic in the Model 80 Memory Protect Controller. The source for each signal on Schematic Drawing 02-248D08 is also provided.

MNEMONIC	DESCRIPTION	LOCATION
AD	Address flip-flop	2L3
ADRS0	Address Control Line from MUX-CH Bus	2J4
ARM	Arm Interrupts flip-flop	2M7
ASATN0	Set Attention - Sets ATN and PWF flip-flops on Protect Violation	3M2
ATN	Attention flip-flop	2J8
ATN0	Attention Test Line to MUX-CH Bus	2S7
ATSYN0/1	Acknowledge Interrupt Signals	2N4
BP000:020	Bank Protect Address to MBC Cable	3M4
CL0/1	Clear Signals - True for Initialize or Command	2K9
CMD0	Command Control Line from MUX-CH Bus	2A6
D080:150	Data Lines from MUX-CH Bus	2A1-2A5
DA0	Data Available Control Line from MUX-CH Bus	2A7
GAD1	Sync Lockout Signal	2C6/3E6
KA0, KB0, KC0, KD0	Word Address Counter	3K8
LD0/LD1	Load Pulses for Mask Register-also sets XBFF	3E2
MSK00:30	Mask Word Signals to MBC Cable	3M6
PON0	Protect On Signal to MBC Cable	3M2
PRON	Protect On flip-flop	2L1
PRFL0	Protect Failure Signal from MBC Cable	3M3
PWF	Protect Write Fail flip-flop	2J7
RACK0	Receive Acknowledge-Acknowledge from a Higher Priority Device in the RACK0/TACK0 Daisy Chain	2L8

MNEMONIC	DESCRIPTION	LOCATION
SCLR0	System Initialize Signal from MUX-CH Bus	2A8
SHFT1	Shift Pulse for Mask Register	3G7
SR0	Status Request Control Line from MUX-CH Bus	2A8
SYN0	Sync Test Line to MUX-CH Bus	2G7
TACK0	Transmit Acknowledge (Acknowledge to the Next Lower Priority Device in the Daisy Chain)	2S6
TMA, TMB	Timer Multibrator	3D7
WCLK0	Write Clock Signal to MBC Cable	3M3
WEBL0	Write Enable Signal to MBC Cable	3M3
WSA1, WSB1, WSC1, WSD1 WSC1, WSD1	Word Address Signals to MBC Cable	3M8
XA, XB	Timer Control flip-flops	3D3
XRP	Pull up Resistor for Unused Inputs on Gates and flip-flops	3C2

SELECTOR CHANNEL

02-232M01A20
February 1973

M70-103
NS SELECTOR CHANNEL INSTALLATION SPECIFICATION

1. INTRODUCTION

This specification provides the necessary information for the installation of the 02-232 Selector Channel (SELCH) (Product Number M70-103) in a Model 70, 74 or 80 Processor System. The NS Selector Channel is complete on one 35-391M02 printed circuit board.

2. PHYSICAL CHARACTERISTICS

2.1 Dimensions 15 3/8 x 14 7/8"

2.2 Weight 2½ pounds maximum

3. INSTALLATION

The NS SELCH may be installed in any even numbered universal expansion slot (i.e., 0, 2, 4, or 6) in the Central Processor Unit (CPU) or in the first memory-I/O expansion chassis. See Figure 1.

NOTE

A SELCH may be installed in slots 0, 1, or 2 of a Model 80/85 CPU chassis only. In this case cutting of the multiplexor bus is not necessary.

3.1 Back Panel Wiring

3.1.1 Multiplexor Channel Bus. At the time of installation it is necessary to cut the Multiplexor Bus wiring between the even numbered slot accepting the SELCH and the next higher numbered slot on the One (1) connector only. The RACK0/TACK0 daisy chain wiring on the back panel is rerouted according to Figure 1. The lower numbered card slots in the chassis become part of the private SELCH Bus on the One (1) connector only.

For the convenience of cutting the Multiplexor Bus, the connections between every other slot are made using "top" wire wraps. (This refers to wire wrap back panels only.) This allows the cutting of the bus by simply lifting the top wraps when the SELCH is installed in an even numbered slot. Refer to Figure 1 A during the following example.

To install a SELCH in Slot 4:

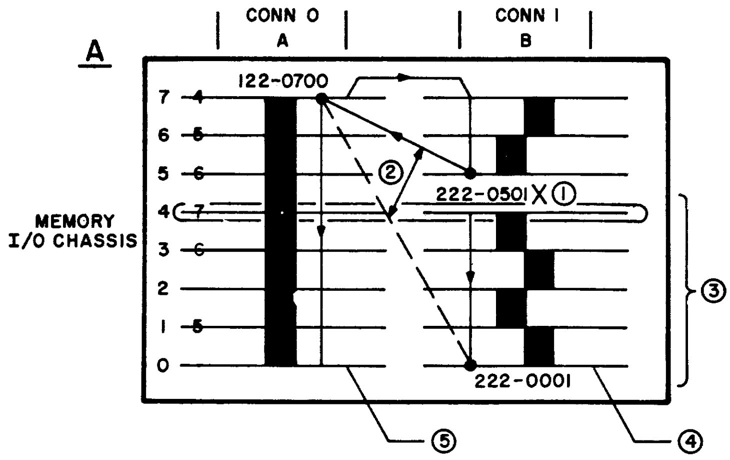
1. Remove all wires on Connector One (1), between Slots 4 and 5, on Pins 11 through 26, Rows 1 and 2. (See backpanel map in 02-232M01D08 Sheet 7.)
2. Remove the wire between 222-0001 and 122-0700.
3. Remove the RACK0/TACK0 jumper between Pins 122 and 222 on both the Zero (0) and One (1) connectors of Slot 4.
4. Connect 122-0700 to 222-0501.
5. Install the SELCH into Slot 4 of the chassis. The private SELCH Bus now appears on the Connector One (1) side of Slots 4, 3, 2, 1, and 0. All slots on the Connector Zero (0) side and Slots 7, 6, and 5 on Connector One (1) side remain as standard Multiplexor Bus slots.

To install a SELCH in any other even numbered slot of a CPU chassis or a Memory-I/O chassis, a similar procedure is followed. Refer to Figure 1 B, C, D, and E.

3.1.2 ACT0/TAC0. The ACT0/TAC0 jumper between Pins 137-0 and 237-0 must be removed from the slot used by the SELCH If the Selector Channel is not the first Direct Memory Access (DMA) channel on the Memory Bus, jumper "K" on the SELCH controller must be removed. Note that on a Model 74 CPU chassis the ACTO/TACO jumper does not exist.

NOTE: THE CIRCLED NUMBERS ON ILLUSTRATIONS A, B, AND C REFER TO THE CORRESPONDING NUMBERS IN THE FOLLOWING INSTALLATION PROCEDURES.

A



CONN 0
A
CONN 1
B
MEMORY I/O CHASSIS
7 ~~4~~
6 ~~5~~
5 ~~6~~
4 ~~7~~
3 ~~6~~
2
1 ~~5~~
0
122-0700
②
222-0501 X ①
222-0001
③
⑤
④

TO INSTALL A SELECTOR CHANNEL IN SLOT 4 OF THE MEMORY I/O CHASSIS ——

① CUT THE MULTIPLEXOR BUS BY REMOVING THE TOP WRAPS.

② JUMPER RACKO/TACKO AS SHOWN, REMOVE DASHED JUMPER.

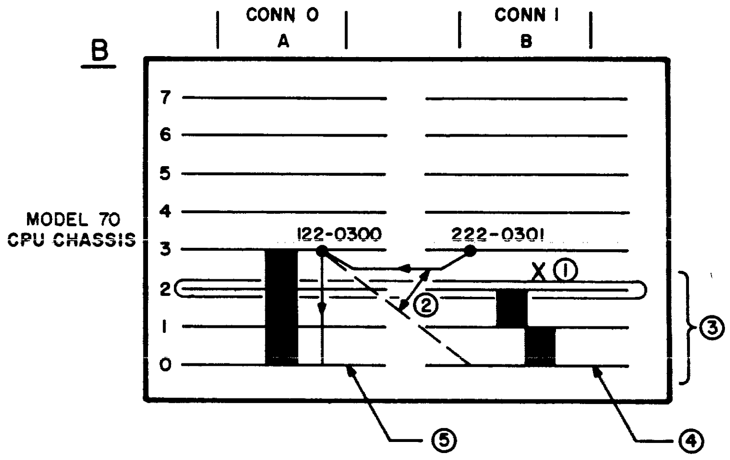
③ THIS SECTION BECOMES THE PRIVATE SELECTOR BUS ON THE CONNECTOR ONE (CONN.1) SIDE ONLY. ALL SLOTS ON THE CONNECTOR ZERO (CONN.0) SIDE, AND SLOTS 7, 6 AND 5 ON CONNECTOR ONE SIDE REMAIN AS STANDARD MULTIPLEXOR BUS SLOTS.

④ IF REQUIRED, EXTEND THE SELECTOR CHANNEL BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑤ EXTEND THE MULTIPLEXOR BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑥ MEMORY MODULE 7, IF IT EXISTS, MUST BE LOCATED IN SLOT 3.

B



CONN 0
A
CONN 1
B
MODEL 70 CPU CHASSIS
7
6
5
4
3
2
1
0
122-0300
222-0301
X ①
②
③
⑤
④

TO INSTALL A SELECTOR CHANNEL IN SLOT 2 OF THE CPU CHASSIS ——

① CUT THE MULTIPLEXOR BUS BY REMOVING THE TOP WRAPS.

② JUMPER RACKO/TACKO AS SHOWN, REMOVE DASHED JUMPER.

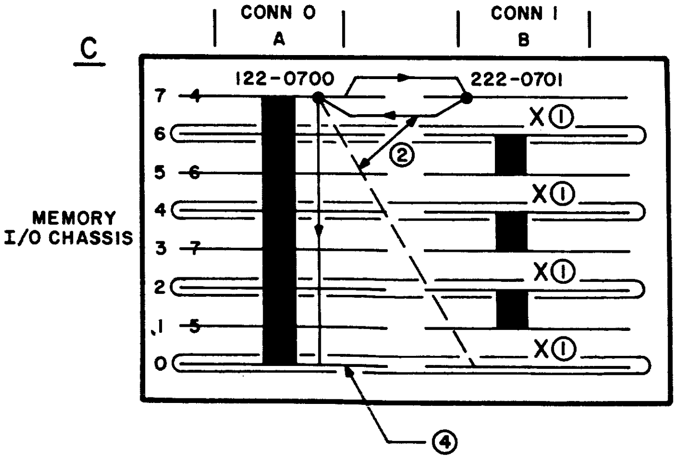
③ THIS SECTION BECOMES THE PRIVATE SELECTOR BUS ON THE CONNECTOR ONE (CONN.1) SIDE ONLY. ALL SLOTS ON THE CONNECTOR ZERO (CONN.0) SIDE REMAIN AS STANDARD MULTIPLEXOR BUS SLOTS.

④ IF REQUIRED, EXTEND THE SELECTOR CHANNEL BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑤ EXTEND THE MULTIPLEXOR BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

NOTE:
IF A MEMORY I/O CHASSIS IS USED IN THE SYSTEM, ANY SELECTOR CHANNELS MUST BE INSTALLED IN THAT CHASSIS.

C



CONN 0
A
CONN 1
B
MEMORY I/O CHASSIS
7 ~~4~~
6
5 ~~6~~
4
3 ~~7~~
2
1 ~~5~~
0
122-0700
222-0701
X①
X①
X①
X①
②
④

TO INSTALL 4 SELECTOR CHANNELS (IN SLOTS 6, 4, 2 AND 0) OF THE MEMORY I/O CHASSIS ——

① CUT THE MULTIPLEXOR BUS IN FOUR PLACES.

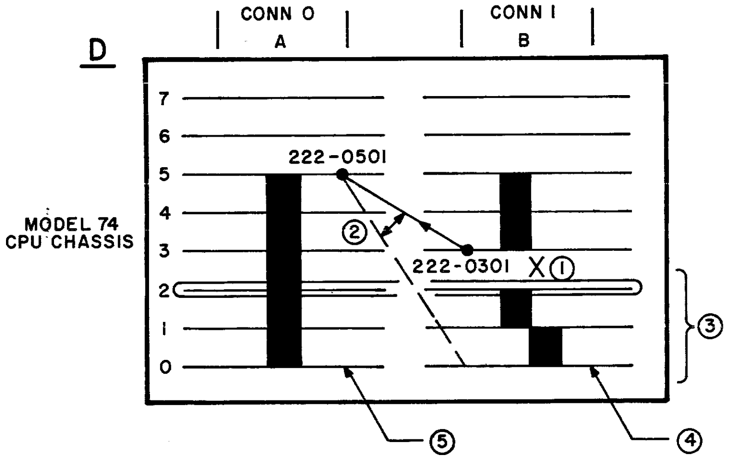
② JUMPER RACKO/TACKO AS SHOWN, REMOVE DASHED JUMPER.

③ EACH SELCH, EXCEPT THE ONE IN SLOT 0, HAS ONE SLOT AVAILABLE ON IT'S PRIVATE BUS. THE PRIVATE BUSSES CAN BE EXTENDED TO OTHER CHASSIS BY INSTALLING CABLES IN SLOT POSITIONS 0, 1, 3 AND 5 ON CONNECTOR ONE (CONN. 1) SIDE.

④ ALL SLOTS ON THE CONNECTOR ZERO (CONN.0) SIDE REMAIN AS THE STANDARD MULTIPLEXOR BUS. THIS BUS CAN BE EXTENDED BY INSTALLING A CABLE HERE.

⑤ MEMORY MODULES 5 AND 7, IF THEY EXIST, MUST BE LOCATED IN SLOTS 1 AND 3.

Figure 1. Backpanel Modifications



TO INSTALL A SELECTOR CHANNEL IN SLOT 2 OF THE CPU CHASSIS——

① CUT THE MULTIPLEXOR BUS BY REMOVING THE TOP WRAPS.

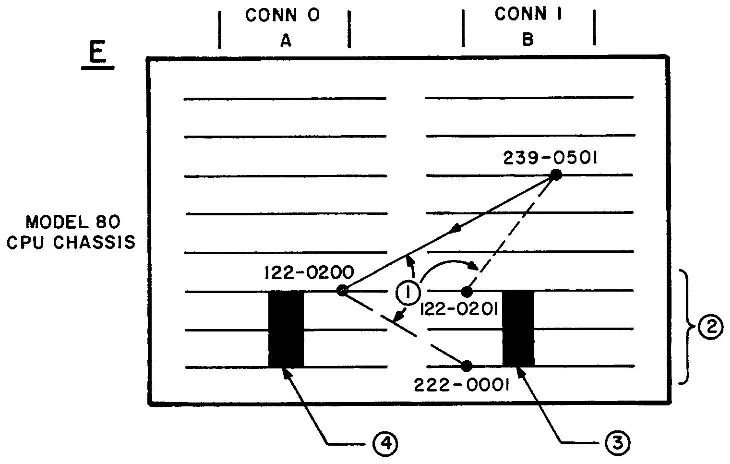
② JUMPER RACKO/TACKO AS SHOWN, REMOVE DASHED JUMPER.

③ THIS SECTION BECOMES THE PRIVATE SELECTOR BUS ON THE CONNECTOR ONE (CONN.1) SIDE ONLY. ALL SLOTS ON THE CONNECTOR ZERO (CONN.0) SIDE REMAIN AS STANDARD MULTIPLEXOR BUS SLOTS.

④ IF REQUIRED, EXTEND THE SELECTOR CHANNEL BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑤ EXTEND THE MULTIPLEXOR BUS TO OTHE CHASSIS BY INSTALLING A CABLE HERE.

NOTE:
IF A MEMORY I/O CHASSIS IS USED IN THE SYSTEM, THE SELECTOR CHANNEL MUST BE IN SLOT 0 OF THE CPU CHASSIS OR IN SOME SLOT OF THE EXPANSION.



TO INSTALL A SELECTOR CHANNEL IN SLOT 0,1 OR 2 CHASSIS——

① JUMPER RACKO/TACKO AS SHOWN, REMOVE DASHED JUMPERS.

② THIS SECTION BECOMES THE PRIVATE SELCH BUS ON THE CONNECTOR ONE (CONN.1) SIDE ONLY. ALL SLOTS ON THE CONNECTOR (CONN.0) SIDE REMAIN AS STANDARD MULTIPLEXOR SLOTS.

③ EXTEND THE SELCH BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

④ EXTEND THE MULTIPLEXOR BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

NOTES:

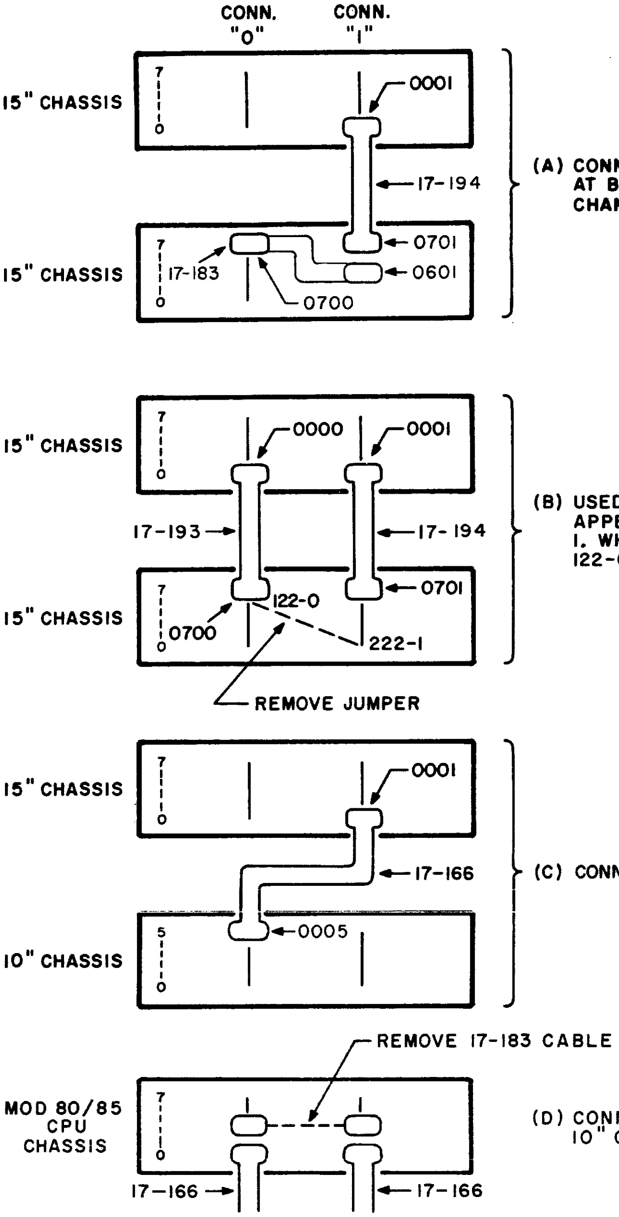
1. IF A 17-183 CABLE IS INSTALLED BETWEEN CONNECTORS ZERO AND ONE IN THE CPU CHASSIS. THIS CABLE MUST BE REMOVED PRIOR TO INSTALLING SELCH.
2. THE INSTALLATION OF A SELCTOR CHANNEL OR OTHER I/O DEVICE CONTROLLER IN THE M80 CPU CHASSIS REDUCES THE MAXIMUM MEMORY SIZE BY 16K BYTES (ONE MSU) FOR EACH SLOT USED!
3. ONLY ONE SELECTOR CHANNEL MAY BE CONFIGURED IN THE MODEL 80 PROCESSOR CHASSIS.

Figure 1. Backpanel Modifications
(Continued)

3.2 Cabling

The cabling necessary for the SELCH depends on the system's physical configuration. When the SELCH Bus does not extend outside the chassis, no cabling is required. When the SELCH Bus must be extended to another chassis, a number of cable configurations can be used. See Figure 2. Care should be taken to minimize bus lengths.

See Figure 2 for a summary of cables. Refer also to User's Manual, Publication Number 29-261, for further details on system configurations.


CONN. "0"
CONN. "1"
15" CHASSIS
15" CHASSIS
7
0
0001
17-194
0701
0601
17-183
0700
15" CHASSIS
15" CHASSIS
0000
0001
17-193
17-194
0701
122-0
0700
222-1
REMOVE JUMPER
15" CHASSIS
10" CHASSIS
0001
17-166
0005
5
REMOVE 17-183 CABLE
MOD 80/85 CPU CHASSIS
17-166
17-166

(A) CONNECTS TWO ADJACENT 15" CHASSIS. THE PRIVATE SELCH BUS APPEARS AT BOTH CONNECTORS 0 AND 1 OF THE LOWER CHASSIS. NOTE THE DATA CHANNEL DOES NOT APPEAR IN THE LOWER CHASSIS.

(B) USED TO CONNECT TWO ADJACENT 15" CHASSIS. THE MULTIPLEXOR BUS APPEARS AT CONNECTOR 0, AND THE SELCH BUS APPEARS AT CONNECTOR 1. WHEN USING THIS CONFIGURATION, THE RACKO/TACKO JUMPER FROM 122-0, SLOT 7, TO 222-1, SLOT 0, MUST BE REMOVED FROM THE LOWER CHASSIS.

(C) CONNECTS THE PRIVATE SELCH BUS TO A 10" CHASSIS ONE OR TWO CHASSIS AWAY.

(D) CONNECTS THE PRIVATE SELCH BUS AND THE MULTIPLEXOR BUS TO A 10" CHASSIS, ONE OR TWO CHASSIS AWAY.

Figure 2. Cabling

4. ADDRESS STRAPPING

The preferred address of the NS Selector Channel is X'F0'. The controller is strapped for this address at the factory. To change the address, refer to Functional Schematic 02-232M01D08. The number and letter designations shown on the schematic refer to the designations on the apparatus side of the SELCH controller board.

5. MODEL 80/85 STRAPPING

For use with the Model 80 or 85 the following options must be exercised:

1. Remove the jumper labled J located between IC 14 and 15.
2. Change the jumper, above IC 53, from (L to 1) to (L to 2).

6. INSTALLATION CHECKS

The NS SELCH is factory tested using a special high speed device. Therefore, field checks are contingent upon the user having appropriate hardware and software available with which to exercise the Selector Channel. When the SELCH is used with Model 80 or 85, insure that the strap options on the SELCH have been made according to Section 5.

02-232M01A21
February 1973

M70-103
NS SELECTOR CHANNEL
MAINTENANCE SPECIFICATION

1. INTRODUCTION

The 02-232M01 NS Selector Channel (SELCH) (Product Number M70-103) is a Direct Memory Access port (DMA) which provides block data transfer between a device controller and memory. Once initiated, the transfer is independent of the Processor. The Processor sets up the device controller, loads the SELCH with the starting and final addresses of the memory block, specifies the type of operation (Read or Write), and issues a GO Command. The SELCH then handles the transfer without further direction by the Processor.

The NS Selector Channel is complete on one printed circuit board and occupies one slot in a system chassis. The SELCH provides the drivers, receivers and termination resistors for the private SELCH Bus. This bus originates at Connector One (1) of the SELCH slot and extends to each lower numbered slot in the system chassis on the Connector One (1) side only. The private SELCH Bus can be extended to other chassis, as required. For installation information, refer to Installation Specification 02-232M01A20.

2. SCOPE

This specification describes the operation of the SELCH in its various modes; Setup, Memory Read, Memory Write, and Termination. Where necessary, this specification references the Multiplexor Channel Bus and Memory Bus operations. These buses are described in detail in the User's Manual, Publication Number 29-261.

3. BLOCK DIAGRAM ANALYSIS

Refer to the SELCH block diagram on Sheet 7 of Functional Schematic 02-232M01D08, and the SELCH Flow Chart, Figure 1, during the following analysis. Before initiating a data transfer via the SELCH, the device controller and the SELCH must be set up. The setup procedure is implemented by the Processor via the Multiplexor Bus (MPX-Bus). When the SELCH is in the Idle mode, the MPX-Bus is tied directly to the private SELCH Bus through the SELCH. This allows the Processor to communicate directly with any device on the private SELCH Bus.

To prepare the SELCH for data transfer, the Address Register (AR) and Auxiliary Address Register (AAR) must be loaded with the starting address in memory where the transfer is to begin, and the Final Address Register (FAR) must be loaded with the address of the last memory location to be accessed. These registers are loaded from the eight least significant Data Lines D080:150 by four consecutive Data Availables (DAs) from the Processor. The first two Data Availables simultaneously load the AR and AAR, which are 16-bit incrementing registers. The AR is incremented, by two, after each halfword is transferred to/from memory, and the AAR is incremented, by one, with each byte transferred to/from the device. Data transfer is terminated when the AAR is equal to the FAR or when the AAR increments past its maximum value, X'FFFF'.

Data transfer is begun by the Processor issuing a GO Command to the SELCH. Transfer to/from the device is now independent of the Processor. The GO Command also prevents communication between the Processor and any device on the private SELCH Bus until the transfer is terminated and the SELCH is addressed.

Data transfer is controlled in the Move Data circuit by inspection of the four least significant bits of the Status Byte presented by the active device on the private SELCH Bus. When any one of the three least significant bits are set, (EX, EOM, or DU), the transfer is terminated. Bit-12 (Busy) regulates the rate of data transfer. In the Memory Read mode, the actual data transfer begins with a memory request, REQ0 active, as soon as a GO Command is issued. When the memory request is serviced by the Processor, the SELCH Memory Bus Control circuit activates Select (SEL), which gates the contents of the Address Register (AR) onto the Memory Address Bus, and gates a halfword of data from memory into the Data Register (DR). At the termination of the memory transfer, the data is loaded from the DR to the Data Buffer (DB) and the AR is incremented.

NOTE

> Unless the SELCH has dropped REQ0 in time to remain selected during the next memory cycle, the SELCH is deselected by the rising edge of Inhibit (INH0) after the halfword has been transferred.

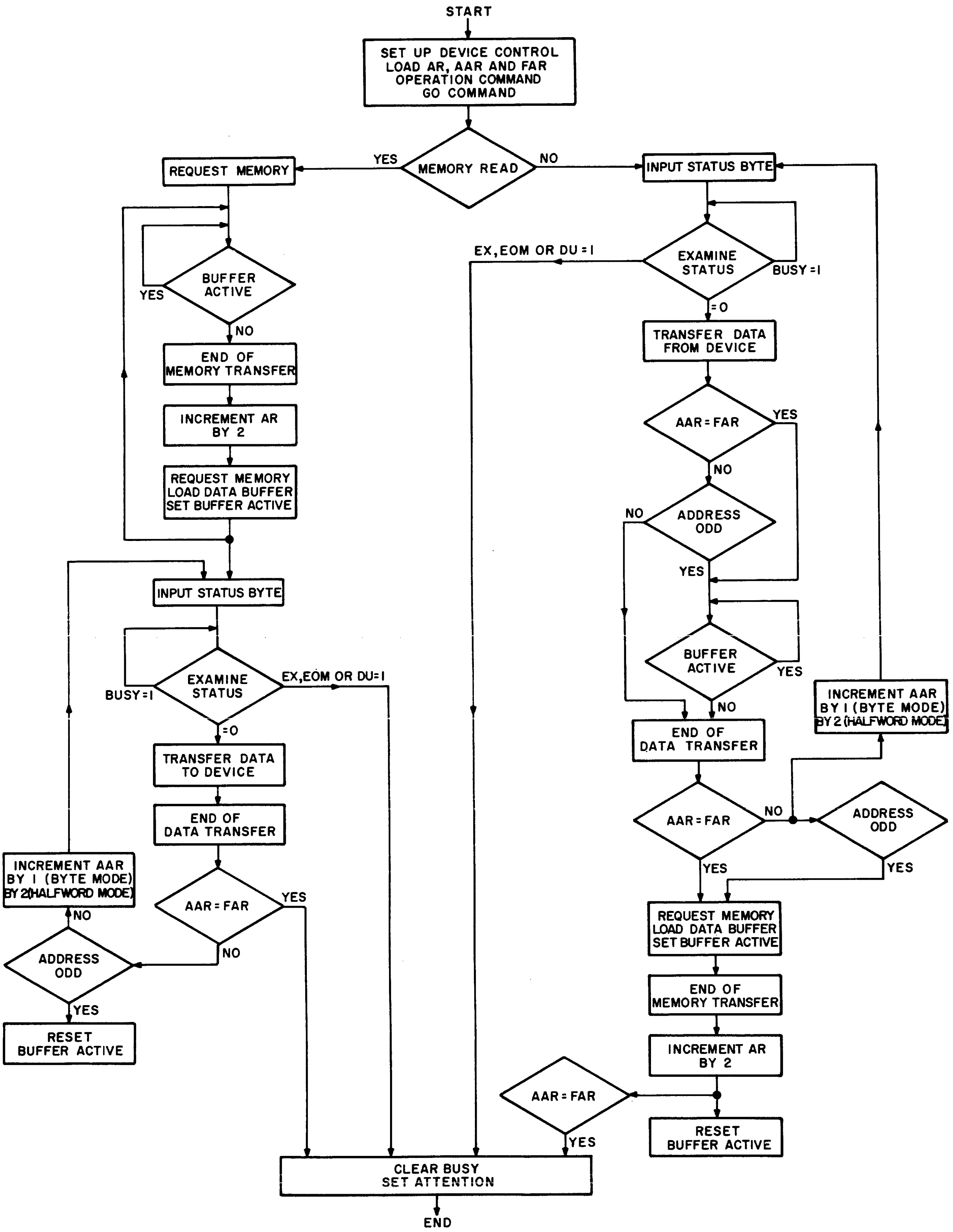

START
SET UP DEVICE CONTROL
LOAD AR, AAR AND FAR
OPERATION COMMAND
GO COMMAND
MEMORY READ
YES
NO
REQUEST MEMORY
INPUT STATUS BYTE
BUFFER ACTIVE
YES
NO
END OF MEMORY TRANSFER
INCREMENT AR BY 2
REQUEST MEMORY
LOAD DATA BUFFER
SET BUFFER ACTIVE
INPUT STATUS BYTE
EXAMINE STATUS
BUSY = I
EX, EOM OR DU = I
= 0
TRANSFER DATA TO DEVICE
END OF DATA TRANSFER
AAR = FAR
YES
NO
INCREMENT AAR
BY I (BYTE MODE)
BY 2 (HALFWORD MODE)
NO
ADDRESS ODD
YES
RESET BUFFER ACTIVE
EX, EOM OR DU = I
EXAMINE STATUS
BUSY = I
= 0
TRANSFER DATA FROM DEVICE
AAR = FAR
YES
NO
NO
ADDRESS ODD
YES
BUFFER ACTIVE
YES
NO
END OF DATA TRANSFER
INCREMENT AAR
BY I (BYTE MODE)
BY 2 (HALFWORD MODE)
AAR = FAR
NO
ADDRESS ODD
YES
YES
REQUEST MEMORY
LOAD DATA BUFFER
SET BUFFER ACTIVE
END OF MEMORY TRANSFER
INCREMENT AR BY 2
AAR = FAR
YES
RESET BUFFER ACTIVE
CLEAR BUSY
SET ATTENTION
END

Figure 1. Flow Chart

Once the DB is loaded, data transfer to the device over Private Data Lines PD000:150 is initiated and, when applicable, a request is made to fetch the next halfword from memory. This cycle continues until either a match is detected between the contents of the Auxiliary Address Register and contents of the Final Address Register, or until the transfer is aborted due to an error condition.

In the Memory Write mode, the data transfer sequence described previously for Memory Read mode is reversed. That is, two bytes of data are loaded into the DR from the device prior to a memory request and the data flow is from the device to the DR, DR to the DB, and finally into memory.

The Branch Gate circuit and the Move Data circuit control the flow of data between memory and the device. The Branch Gate supervises the overall data flow, while the Move Data circuit performs the handshaking between the SELCH and the active device on the private SELCH Bus.

Upon termination of the data transfer, the program is notified via an interrupt and by the inactive state of the SELCH Busy flip-flop which is presented to the program as Bit-12 of the SELCH Status Byte.

Selector Channel Status and Command Byte Data is shown on Table 1.

TABLE 1. SELECTOR CHANNEL STATUS AND COMMAND BYTE DATA

BIT NUMBER	0	1	2	3	4	5	6	7
STATUS BYTE					BSY			
COMMAND BYTE			READ	GO	STOP			

BSY	When this bit is set, a one shot generates the EBS1 pulse to start the appropriate SELCH operation. When this bit is cleared an interrupt is generated.
READ	This command, Bit-2, sets the Memory Write (WT) flip-flop. The controller on the SELCH Bus is setup for a device Read operation.
GO	This command, Bit-3, clears the MSC flip-flop and sets the BSY flip-flop to initiate the Data Transfer mode.
STOP	This command, Bit-4, from the Processor clears the BSY flip-flop and initializes the Load/Unload Sequencer. During the Data Transfer mode, execution of the command is delayed until the end of a memory cycle, if one is in progress.

4. FUNCTIONAL DIAGRAM ANALYSIS

4.1 Introduction

This section relates to Functional Schematic 02-232M01D08, Sheets 1 through 6. Note that in INTERDATA functional schematics, the last character in the mnemonic symbol designates the logic level when the signal is active. For example; D080 is Data Line Number 8 (D08). The last character (0) inidicates that when D080 is active, the line is at a logical Zero level.

4.2 SELCH Control Circuit

In the Idle mode, the SELCH Address (2M8), Busy (3F3), and Multiplexor-SELCH (MSC) (3FA) flip-flops are reset and the private SELCH Bus is tied directly to the Multiplexor Bus. This allows the Processor to communicate, via the Multiplexor Bus, with any device on the private SELCH Bus.

To communicate with the SELCH, it must first be addressed. The SELCH Address (X'F0' preferred) is placed on Data Lines D080:150 (1A3-8) and the Address control line is activated (ADRS0)(4B8). The SELCH Address is decoded by the four input NAND gate (1F4) and the Address flip-flop is set (2M8). The set output from the Address flip-flop (AD1)(2J7), when active, prevents the control signals on the MPX-Bus from passing onto the private SELCH Bus by holding the Control Line Gate inactive (CLG1) (1B2). Capacitors C33 and C34 (4D8) delay the propagation of the Private Address control line (PADRS0) (4F9) to the SELCH Bus, so that when the SELCH is being addressed PADRS0 does not become active. This delay allows the SELCH to be addressed without resetting the Address flip-flop of the active device on the private SELCH Bus.

The simultaneous loading of the Address Register (AR) and Auxiliary Address Register (AAR), and the loading of the Final Address Register (FAR) is accomplished by four consecutive Data Availables (DAs) from the Processor. The Load/Unload Sequencer (2L2) controls the loading of these registers (AR, AAR, and FAR) and the unloading of the AAR. The sequencer is set to its initial state by the termination of the last data transfer, a Stop Command, or a System Clear (SCLR0)(4MS) so that the first DA, through Data Available Gate (DAG0)(2L4), will activate Load Address Register High (LARH0)(2S2).

LARH0 gates Data Lines DA081:151 (1D3-8) into the eight most significant bits of the AR and AAR. The rising edge of the first and each successive Data Available Gate (DAG0)(2L4) increments the sequencer and allows the next DA to activate the next load line. The second DA loads the eight least significant bits of these registers. The third and fourth DAs will then load the Final Address Register in the same order. The contents of the AAR may be inspected, via the program, by issuing two Data Requests (DR) to the SELCH whenever the Load/Unload Sequencer is in its initial state. (e.g., Upon termination of a SELCH transfer, sequencer initialized, the FAR may be inspected to determine if the entire block of data had been transferred.)

If a Memory Write operation is desired, an Output Command with Bit-10 set must be issued to set the Write flip-flop (3F5). Since the Write flip-flop is reset by the Data Available/Request Gate (DARG1)(2L5) whenever a DA or DR is sent to the SELCH (setup procedure), no command is necessary to initiate a Memory Read operation.

Data transfer commences with a GO Command from the Processor, which is an Output Command with Bit-11 set. The GO Command sets both the Busy (3F3) and MSC (3F4) flip-flops. The setting of the Busy flip-flop causes an End of Busy Set pulse (EBS1) (3H4) to be generated. This pulse is generated from the falling edge of BSY0 (3F3), and is used by the Branch Gate circuit to initiate the transfer cycle. The Busy latch circuit remains set until the Selector Channel detects the termination of transfer and its state is presented to the program via Bit-12 of the Sense Status Byte.

The MSC flip-flop is reset by SCLR0A or by addressing the SELCH, Set Gate active (SGAD1)(2L9), when the Busy flip-flop is reset. The resetting of the MSC flip-flop, MSC0 active, clears any pending interrupt in the Selector Channel.

Information is steered from the SELCH to both the Data Lines D080:150 (1B4-9) and the Private Data Lines PD080:150 (1S4-9) by the proper gating of four each, four-to-one line multiplexors (Sheet 1). For example; with the SELCH idle, Busy reset, all Data Lines are tied directly to the Private Data Lines in both directions.

4.3 Memory Bus Control Circuit

Memory Bus Control timing relationships are shown in Figure 2. A SELCH request for memory is started by activating Set Request (SREQ0)(3S4). SREQ0 is activated by the Branch Gate circuit (3M8) when either the SELCH has received a halfword of data from the device or, in the Memory Read mode, whenever the Memory Data Register is available to accept the next halfword.

SREQ0 is applied to the direct set input of the Request flip-flop (REQ)(4L5) which sets the flip-flop and sends REQ0 to the Processor. When REQ0 is received, the Processor generates Enable (EN0). EN0, on the first DMA device, is jumpered to Accept (ACT0) which generates the daisy chain priority loop through all DMAs in the system. The daisy chain begins at the highest priority DMA as EN0, and propagates to the lower priority DMAs as Transmit Accept (TAC0) until it is captured by the first DMA requesting a memory cycle. When the REQ flip-flop is set and ACT0 (EN0) is active, the ACT0/TAC0 contention circuit (4H2) blocks the propagation of TAC0, and provide highs on the J input to the SEL flip-flop and the K input to the REQ flip-flop. Thus, on the rising edge of EN0, the Select flip-flop becomes set and the Request flip-flop is reset. When the SELCH REQ flip-flop is reset and ACT0 (EN0) is active, the ACT0 signal is propagated as TAC0 to the DMA with a lower priority.

The trailing edge of Inhibit (INH0) (4H5), from the Processor, indicates the end of the memory cycle. This edge, unless the SELCH has dropped REQ0 in time to remain selected during the next cycle, causes the SEL flip-flop to reset. Two pulses, End of Memory Transfer (EMX0) (4M7) and Inhibit (INH0P) (4M2), are generated by the leading and trailing edges of INH0 respectively. EMX0 is used by the Branch Gate circuit to indicate the end of the memory transfer. The Address Register is toggled by the AND function of SEU and INH1.

In the Memory Read mode, the Memory Data Register (MDR) is cleared by Clear Data Register (CDR0) (4R2) which is generated by the trailing edge of REQ1. Write Not (WT0A) (3F5) is ANDed with SEL1 to form Enable Memory Data Read (ENMDR1) (4R6), which gates the contents of the MDR onto the Memory Data Lines MD000:150 (Sheet 6) for the restore portion of the memory cycle. (This function is disabled when using solid state memory.) The contents of the memory location accessed is gated to the direct set inputs of the MDR by Enable Memory Strobe (ENMS1) (4R4). This function is WT•SEL•INH for use with core memory and WT•SEL•INH when using solid state memory (4R4).

When writing to memory, the contents of the Data Buffer is gated onto Memory Data Lines MD000:150 (Sheet 6) by Enable Memory Data Write (ENMDW1)(4R3), when selected. A Memory Write operation is indicated to the Processor by activating WRT0A (4S3).

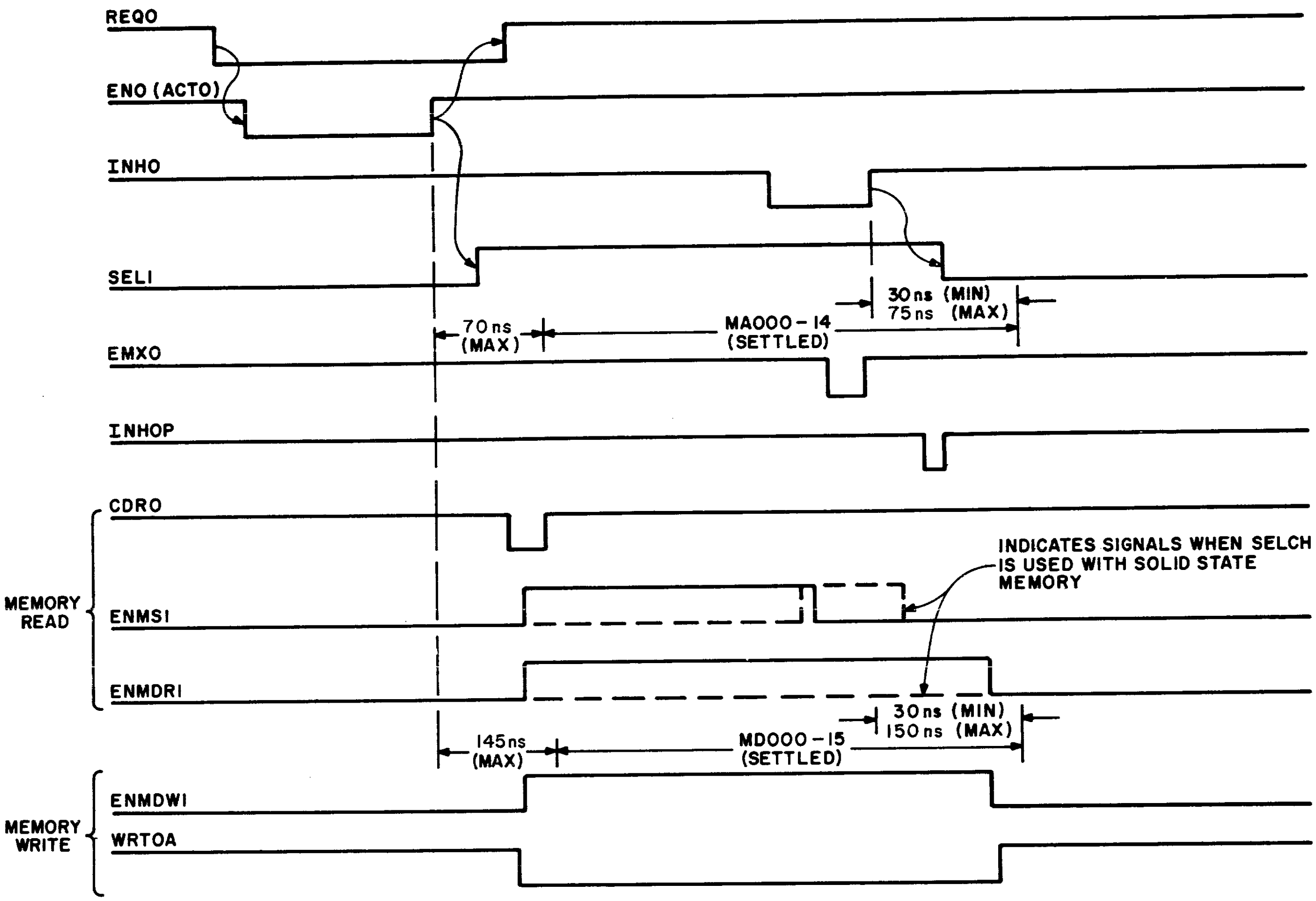

REQO
ENO (ACTO)
INHO
SELI
EMXO
INHOP
CDRO
ENMSI
ENMDRI
ENMDWI
WRTOA
MEMORY READ
MEMORY WRITE
70 ns (MAX)
MA000-14 (SETTLED)
30ns (MIN)
75ns (MAX)
INDICATES SIGNALS WHEN SELCH IS USED WITH SOLID STATE MEMORY
145ns (MAX)
MD000-15 (SETTLED)
30ns (MIN)
150ns (MAX)

Figure 2. Memory Bus Control Timing Diagram

4.4 Address Register and Auxiliary Address Register.

The Address Register (AR) and Auxiliary Address Register (AAR) (Sheet 5) each consist of four, four-bit counters. These registers are loaded simultaneously by the Processor from Data Lines D080:150 (1A3-8), under control of the Load/Unload Sequencer (as discussed in Section 4.2), with the starting address from which the block transfer is to begin. The contents of the AR (Sheet 5) is gated onto Memory Address Lines MA000:140 (5R1-8) whenever the SELCH is selected, SEL flip-flop set. The AR is incremented with each memory transfer by Select• Inhibit (SINH0) (4K8). The AAR (Sheet 5) keeps track of the transfer between the SELCH and the device. This register is incremented, by one, for each byte of data transferred by Toggle Auxiliary Address Register (TAAR0) (3M1). When the transfer is in the Halfword mode, TAAR0 is generated twice for each transfer. The outputs of the AAR are used by the Match circuit to determine the end of the data block. Its contents may be examined, via the program, by issuing two consecutive DRs to the SELCH when the sequencer is initialized. In addition, AAR151 is used in the Byte Transfer mode to determine whether the byte being transferred is odd or even, for byte steering. Carry Out from the most significant stage of the AAR (CO0) (541) terminates the transfer, clear Busy, when a transfer is attempted past the maximum memory address. This feature prevents 'wrap-around' in memory.

4.5 Final Address Register

The Final Address Register (FAR) is implemented by four quad latches (Sheet 5). This register, like AR and AAR, is loaded by the Processor under control of the Load/Unload Sequencer. The outputs of this register are used exclusively by the Match circuit to determine when the final address of the transfer is reached.

4.6 Memory Data Register and Data Buffer

The Memory Data Register (MDR)(Sheet 6) is a 16-bit register composed of 16 edge triggered JK flip-flops. In the Memory Read mode, the MDR is first cleared by Clear Data Register (CDR0) (4R2) and then direct set by each active bit on Memory Strobed Data Lines MS000:150 (Sheet 6). During a Memory Write, the data, in double rail format, present at the J and K inputs to the MDR, is toggled into the flip-flops on the trailing edge of either Load Data Register High (LDRH0)(649) or Load Data Register Low (LDRL0)(6J9).

As soon as the MDR is loaded, if the Data Buffer (DB) is empty (as determined by the inactive state of the Buffer Active flip-flop)(3H1), the MDR contents are loaded into the DB (Sheet 6) by Load Data Buffer (LDB1)(357). Information present in the DB is, in turn, either written into memory via Memory Data Lines MD000:150 or sent to the device on Private Data Lines PD000:150.

4.7 Data Transfer Circuit

Refer to Figure 3 for Memory Read timing diagrams and Figure 4 for Memory Write timing diagrams. The Memory Read timing diagram shows the timing of a three byte transfer, in the Byte mode, of 2,000,000 bytes/second. Figure 4 shows a transfer of two halfwords, in the Halfword mode, to a slower device.

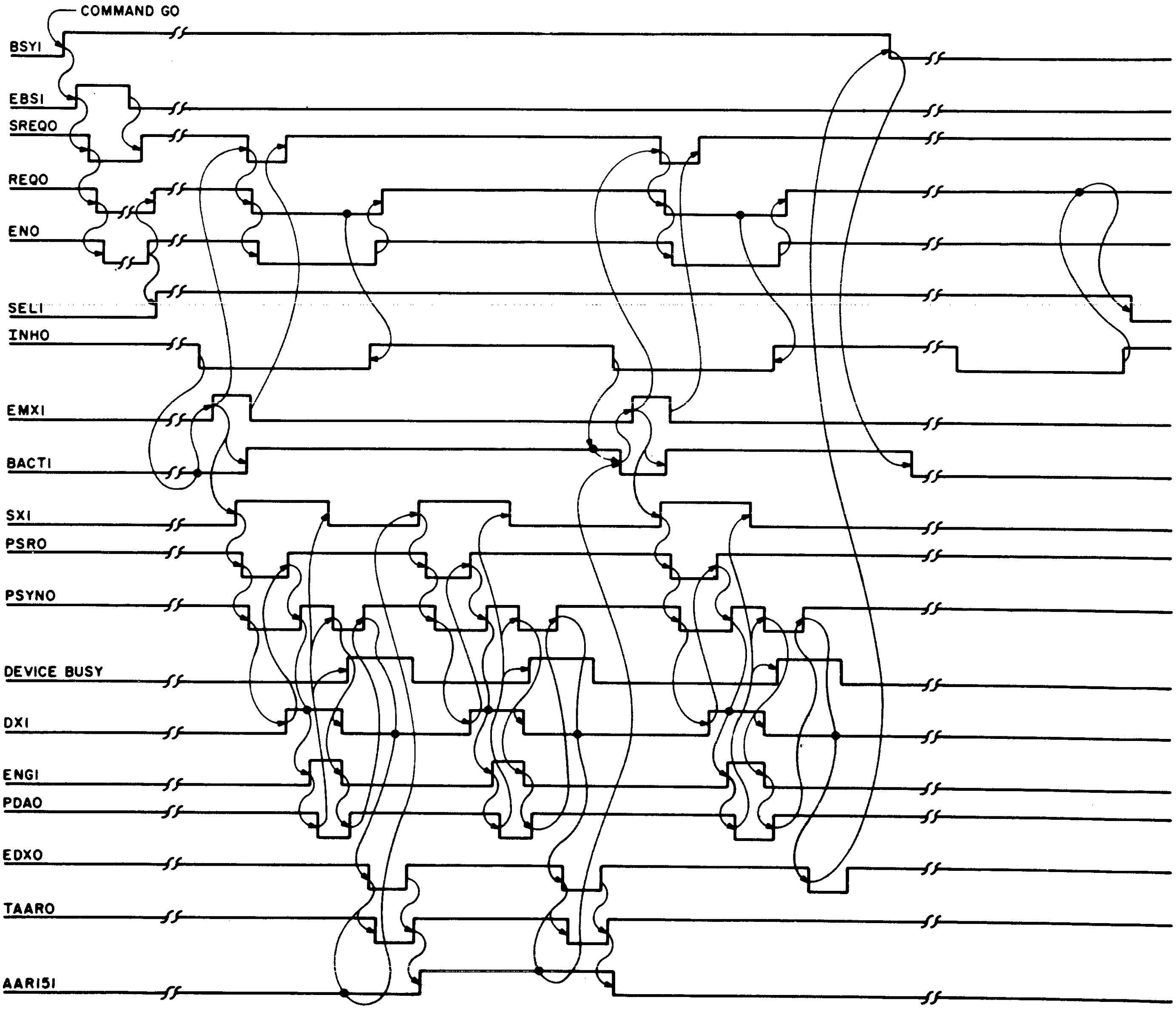


Figure 3. Memory Read (Byte Mode)

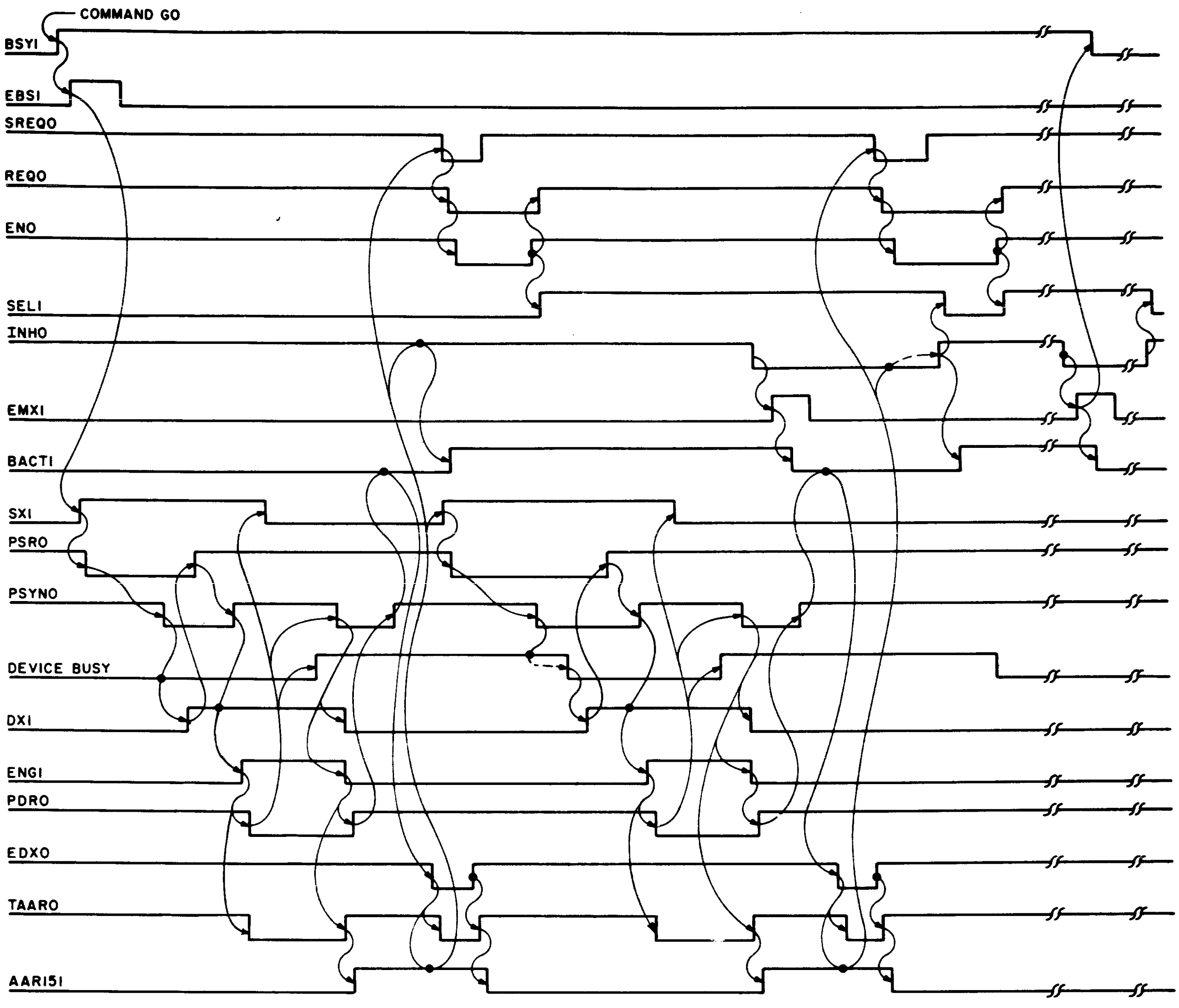


Figure 4. Memory Write (Halfword I/O Mode)

A GO Command to the Selector Channel sets the Busy flip-flop which generates the End of Busy Set pulse (EBS1)(3K8).

In the Memory Read mode, EBS1 is decoded by the Branch Gate circuit and SREQ0 is generated. Thus, a request for memory is initiated. When the halfword of data is present in the MDR, the End of Memory Transfer pulse (EMX1)(4R6) becomes active and the Branch Gate circuit once again requests memory and generates Set Status Transfer (SSX0)(3S5) and Load Data Buffer (LDB1) (3S7). These signals initiate the transfer to the device and load the Data Buffer (DB) respectively.

SSX0 sets the Status Request flip-flop (3F6) which activates the Private Status Request control line (PSR0)(3G6) to the active device on the private SELCH Bus. This Status Request examines the four least significant bits of the Status Byte. If any of the three least significant bits (EX, EOM, or DU) are set, the transfer is terminated by resetting the Busy flip-flop (3F3). The assumption is made that each of these status bits remain reset for the remainder of this discussion. With Bit-12 (Busy) of the Status Byte reset, the Data Transfer flip-flop becomes set (3F7). Data Transfer (DX0)(3E1) inhibits the generation of PSR0, which causes Private Sync (PSYN1)(4B4) from the device to become inactive. This enables Engage to go high (ENG1)(3D8), which allows the Private Data Available control line (PDA0)(3H5) to become active. The Private Data Available/Request signal (PDAR1)(3H5), generated whenever a Private Data Available (PAD0) or Private Data Request (PDR0) signal is active, will then clear the Status Request flip-flop. Upon receipt of Sync from the device, PSYN1 active, the Data Transfer flip-flop becomes reset and ENG1 goes low, disabling PAD0. When the Sync is removed by the device, an 80 nanosecond End of Data Transfer pulse is generated (EDX0) (3J8) which increments the Auxiliary Address Register and is used by the Branch Gate circuit to generate a function in accordance with the truth table for EDX on Sheet 3. This cycle continues until termination of the transfer is detected.

In the Memory Write mode, WT1 active (3F5), EBS1 is used to generate SSX0, and the Branch Gate circuit directs the loading of a halfword of data into the DB before a memory request is made. The transfer of data from the device is the same as described in the Memory Read mode, except that ENG1 is used to generate the Private Data Request control line (PDR0)(3H5) rather than PDA0. Data from the device is loaded into the MDR on the trailing edge of either Load Data Register High (LDRH0)(2R2) or Load Data Register Low (LDRL0)(2R2), depending on which eight bits are being loaded. In the Halfword Transfer mode, both LDRH0 and LDRL0 are generated simultaneously. With WT1 active, the generation of EDX1 is delayed by activating the clear input to the one-shot (3H8) when the Buffer Active flip-flop is set (BACT1)(3H1), if either the transfer to the device is on an odd boundary or when a Match is detected (MCH0)(5J2). This prevents the reloading of the Data Buffer (DB) before the last halfword has been written into memory.

4.8 RACK0/TACK0 Contention Circuit

The Selector Channel directs the propagation of the Acknowledge signal to lower priority devices on the Multiplexor Channel Bus as well as devices on the private SELCH Bus. If the Selector Channel Attention flip-flop (4B4) is set, the SELCH captures the Receive Acknowledge signal (RACK0) (4B3), place its device address on the Data Lines and return Sync to the Processor, Attention Sync (ATSYN0)(4F4) active. If the Attention flip-flop is reset, RACK0 is propagated as either Private Transmit Acknowledge (PTACK0)(4F2) or Transmit Acknowledge (TACK0)(4F3). Since devices on the private SELCH Bus have a higher interrupt priority than devices below the SELCH on the MPX Bus; if the Private Attention Test line is active (PATN0) (4B1), PTACK0 is generated rather than TACK0. Note that when MSC0 is high (3F4), PATN0 is disabled so that a device on the private SELCH Bus may not interrupt the Processor while the SELCH is active.

5. MAINTENANCE, TROUBLE SHOOTING, AND TEST

Before attempting any maintenance or testing, insure that the necessary back panel modifications and SELCH board option strapping have been made in accordance with the NS Selector Channel Installation Specification 02-232M01A20.

To insure a 2,000,000 Byte/second transfer rate in the Byte Transfer Mode, it is necessary to limit the maximum delay between PDA0, PDR0, and PSR0 and the return of Sync from the device (PSYN0), to 30 nanoseconds. In addition, the device must be ready for the next byte of data, Busy Status Bit reset, whenever a Status Request is made. Field testing of this device is contingent upon the user having appropriate software and hardware available with which to exercise the Selector Channel. There are no adjustments associated with this device. Do not install Terminator Boards 35-433 or 35-434 on the SELCH bus if a transfer rate of 2,000,000 Bytes/second is to be maintained in the Byte (8 Bit) Mode. The SELCH Bus should be contained on a single 15 inch chassis if no terminators are used.

6. MNEMONICS

The following list provides a brief description of each mnemonic found in the SELCH. The source of each signal on Functional Schematic 02-232M01D08 is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
AAR001:151	Outputs of the Auxiliary Address Register	5F1-5F9
ACT0	Accept - Request for memory accepted by Processor	4H1
AD1	Address - Active when SELCH is addressed	2K7
ADRS0	Address control line from MPX-Bus	4B8
AG081:151	Address Gated Lines - Output of Address Strap	1E3 - 1E8
ATN0	Attention - Attention to Processor	4F1
ATSYN	Attention Sync - Generated by an Acknowledge Attention from Processor	4F4
BACT1	Buffer Active - Indicates that valid data is present in the DB	3H1
BSY	Busy - Indicates a data transfer is in progress	3F3
CDR0	Clear Data Register - Clears MDR prior to loading from MS000:150	4R2
CBSY0	Clear Busy - Terminates transfer when a match is detected	3M3
CL070	Control Line 7 - Control Line from MPX-Bus	4B6
CLG1	Control Line Gate - Gates Private Control Lines	1C2

MNEMONIC	MEANING	SCHEMATIC LOCATION
CLUS0	Clear Load/Unload Sequencer - Clears Sequencer	3S2
CMD0	Command Control Line from MPX-Bus	4B8
CMG	Command Gated by AD1	2S7
CO0	Carry Out of the AAR - Prevents Memory 'Wrap-around'	5A1
D000:150	Data Lines from MPX-Bus	1A3 - 1A8 2A1 - 2A8
DA0	Data Available Control Line from MPX-Bus	4B7
DLG0	Data Line Gate - Gates Data Lines and Private Data Lines	1R2 - 1D3
DB001:151	Outputs of Data Buffer	6G2 - 6G9 6R2 - 6R9
DR0	Data Request Control Line from MPX-Bus	4B7
DRG0	Data Request Gated by AD1	2L5
DX	Data Transfer flip-flop	3F8
EBS1	End of Busy Set - Signals the start of a SELCH transfer	3J4
EDX1	End of Data Transfer - Signals the end of a device transfer	3J8
EMX1	End of Memory Transfer - Signals the end of a memory transfer	4R7
EN0	Enable from Memory Bus	4H2
ENG1	Engage - Gates either PDS0 or PDR0	3D8
ENMDR1	Enable Memory Data Register Read - Gates contents of MDR to MD000:150	4R6
ENMDW1	Enable Memory Data Register Write - Gates contents of DB to MD000:150	4R3
ENMS1	Enable Memory Strobe - Gates contents of MS000:150 to MDR	4R4
HW0	Halfword Control Line from MPX-Bus	1D2
INH0	Inhibit from Memory Bus	4H5
LARH0	Load Address Register High - Loads AAR and AR, Bits 00:07	2R2
LARL0	Load Address Register Low - Lards AAR and AR, Bits 08:15	2R2
LDB1	Load Data Buffer - Load contents of MDR to DB	3S2
LDRH0	Load Data Register High - Loads MDR Bits 00:07	3F8
LDRL0	Load Data Register Low - Loads MDR Bits 08:15	3H9
LFRH0	Load Final Address Register High - Loads FAR Bits 00:07	2S3
LFRL0	Load Final Address Register Low - Loads FAR Bits 08:15	2S3
MA000:140	Memory Address Lines to Memory Bus	5R1 - 5R8
MCH1	Match - Indicates a match between AAR and FAR	5J6

MNEMONIC	MEANING	SCHEMATIC LOCATION
MD000:150	Memory Data Lines to Memory Bus	6G1 - 6G8 6R1 - 6R8
MS000:150	Memory Strobed Data Lines from Memory Bus	6A1 - 6A8 6H1 - 6H8
MSC0	Multiplexor SELCH Control flip-flop	3F4
PADRS0	Private Address Control Line to SELCH Bus	4F8
PATN0	Private Attention from SELCH Bus	4B1
PCL070	Private Control Line 7 to SELCH Bus	4R6
PCMD0	Private Command Control Line to SELCH Bus	4F8
PD000:150	Private Data Lines - SELCH Bus	2F1 - 2F8 1S3 - 1S9
PDA0	Private Data Available Control Line to SELCH Bus	3H5
PHW0	Private Halfword Control Line from SELCH Bus	1A1
PSR0	Private Status Request Control Line to SELCH Bus	3H6
PSYN0	Private Sync from SELCH Bus	4B5
PTACK0	Private Transmit Acknowledge to SELCH Bus	4F2
RACK0	Receive Acknowledge from MPX-Bus	4B5
RBA0	Reset Buffer Active - Resets Buffer Active flip-flop	3M2
REQ0	Request - Request for memory cycle to Memory Bus	4R5
SCLR0	System Clear - Initialize Signal	4H4
SGAD1	Set Gate - Sets Address flip-flop	2LR
SR0	Status Request Control line from MPX-Bus	4B6
SREQ0	Set Request - Initiates a request for memory	3S4
SSX0	Set Status Transfer - Sets the Status Request flip-flop	3S5
SX	Status Transfer - Status Request flip-flop	3F6
SYN0	Sync to MPX-Bus	2S5
TAC0	Transmit Accept - To lower priority DMAs	4R1
TACK0	Transmit Acknowledge - To lower priority devices on MPX Bus	4F3
TAAR0	Toggle Auxiliary Address Register - Increments AAR	3M1
TAR0	Toggle Address Register - Increments AR	4S7
UAAH0	Unload Auxiliary Address Register High - Unloads AAR Bits 00:07	2R4
UAARL0	Unload Auxiliary Address Register Low - Unloads AAR Bits 08:15	2R4
WT	Write flip-flop	3F5
WRT0A	Write to Memory Bus, when selected	4R3

POWER SYSTEM

02-261A12
October 1972

MODEL 80
POWER SYSTEM

1. MODEL 80 CONFIGURATION

The minimum Model 80 System configuration consists of one card file and two power supplies. The two power supplies of the minimum system are one 34-014 memory power supply and one 34-015 system power supply (Product Number M49-022). Figure 1 shows the physical configuration of the basic system.

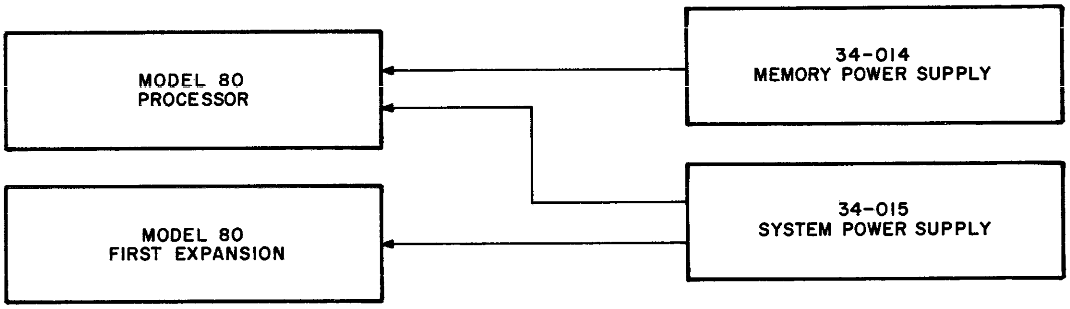


Figure 1. Typical Model 80 Configuration

2. SYSTEM VOLTAGES

Model 80 systems require five system voltages. They are:

MNEMONIC	VOLTAGE	SOURCE POWER SUPPLY
P5	+5.1V	34-015
P15	+15.4V	34-015
N15	-15.0V	34-015
P22	21.0V	34-014
P5S	+5.1V	34-014

Other voltages locally generated for peripherals or memory circuits are not considered system voltages and are not covered here.

3. 34-015 SYSTEM POWER SUPPLY

In the basic configuration this supply provides P5, P15 and N15 for the Processor and the first expansion chassis. Additional 34-015 or 34-012 power supplies are used to power additional expansions. Generally, one 34-015 supply powers two card files. In some applications one supply may power only one card file.

All three outputs (P5, P15 and N15) are short circuit protected, overvoltage protected and regulated to ±1% when normally loaded.

The schematic drawing number for this power supply is 34-015D08.

4. 34-014 MEMORY POWER SUPPLY

The 34-014 memory power supply provides P22 and P5S for the series six memories. Series six memories require continuous power to maintain stored information. Therefore, when the power switch on the Display Console is turned to the OFF position, line voltage to the memory power supply is not removed and power to the memory (P22 and P5S) is maintained preventing loss of stored information.

In the event primary power fails, a battery back up system is built into the 34-014 power supply which prevents loss of stored information for 20 minutes or more. It should be noted that the only normal way to turn off the outputs of this supply is to turn off the memory power switch.

4.1 Modes

The 34-014 memory power supply has two modes of operation; normal and standby. In the normal mode, the P22 and P5S outputs provide a steady +22 volts and +5 volts at output currents up to 7 amperes and 5 amperes respectively. The normal mode provides enough power to operate the memory at its maximum speed.

In the standby mode, the memory requires only enough power to prevent loss of stored information. The P22 load is approximately 50 milliamperes. The P5S output pulsates in the standby mode. It provides a 5 volt output every 2 milliseconds. The width of the P5S pulses is approximately 20 microseconds, however, the rise times are approximately 50 microseconds. The reason for switching the output voltage off when not needed is to conserve power when the standby mode is powered from battery.

A signal from the Processor (SCLR0) determines which mode the power supply shall operate in. A low SCLR0 (grounded) causes standby mode and a high SCLR0 (+5V) causes normal mode. Note that standby mode may be required by the Processor even though primary power has not failed. However, all primary power failures result in standby mode and battery operation. Refer to Functional Schematic 34-014D08.

Standby mode (SCLR0 low) occurs:

1. When primary power fails.
2. When powering down with console power switch.
3. When initializing the Model 80 System with console initialize switch.

4.2 Block Diagram

Figure 2 shows a simplified circuit diagram of the 34-014 power supply. It consists of three regulators; P22 regulator, P5S regulator, and battery charger. The P22 and P5S regulators receive DC from either the normal line through T1 or the battery system through the inverter. The battery charger is powered from either the normal line or a separate input line that could be an uninterruptable power source. The inverter always runs so that if the line fails no signaling is necessary to start it. However, the power which the inverter is capable of delivering is limited to that required of the standby mode only. Overloads cause the outputs to go out of regulation. Only the normal line through T1 is capable of delivering enough power to run in normal mode.

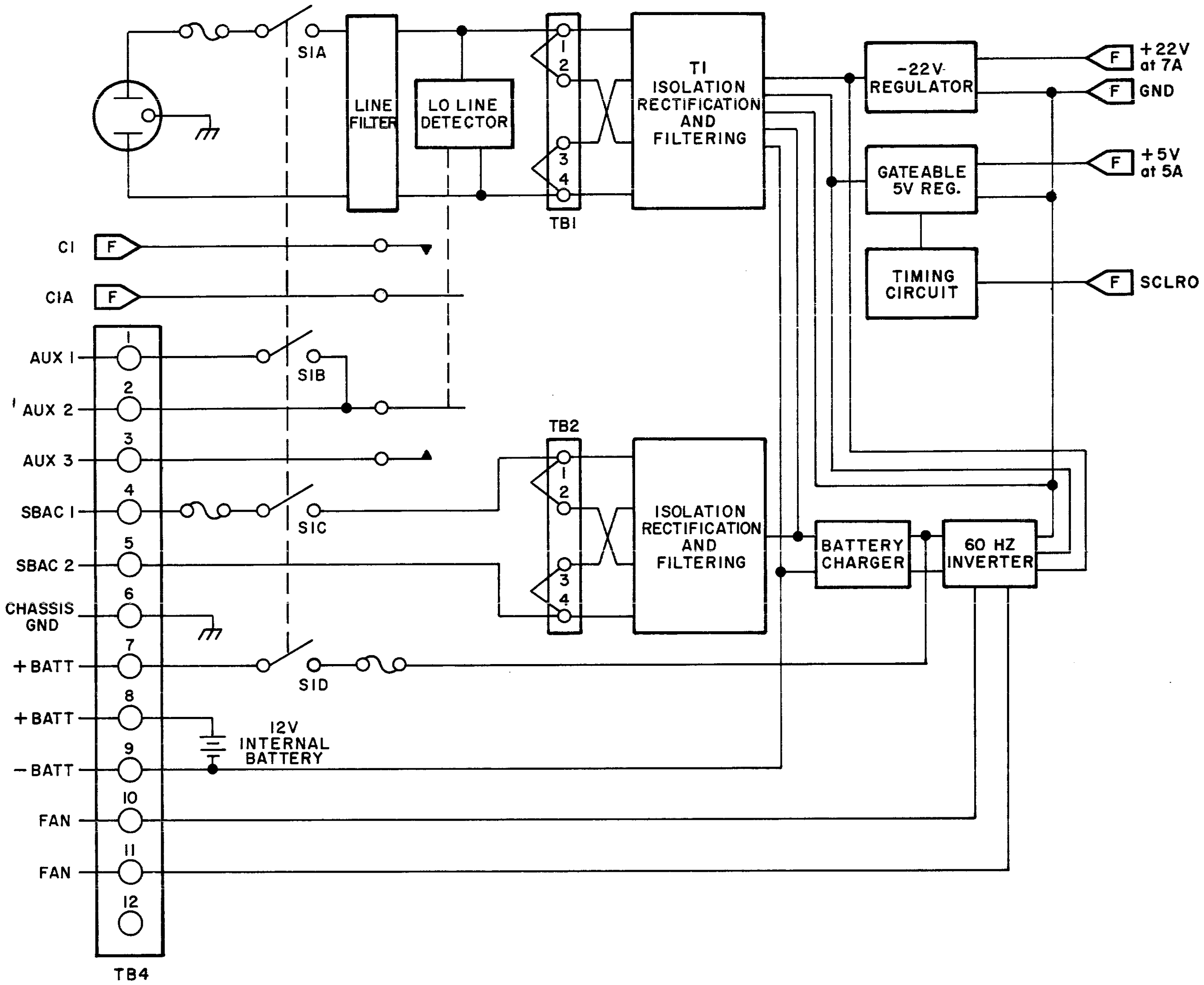
Since memory power (P5S and P22) is not turned off during normal power down intervals an independent "Memory Power Switch" (S1 on block diagram) allows memory power to be turned off to make repairs.

CAUTION

Caution should be exercised to insure that this switch is in the OFF position before removing memory boards or cables.

The P5S output is controlled by the timing circuit which causes the P5S output to pulsate when directed to do so by a grounded SCLR0 input signal.

The interlock monitors the line to the 34-014 supply and shorts the C1 and C1A lines together when the normal line is present. If the normal line is not present, the C1 and C1A lines become disconnected and shut down the normal Model 80 System power.



SIA
LINE FILTER
LO LINE DETECTOR
1
2
3
4
TB1
T1 ISOLATION RECTIFICATION AND FILTERING
-22V REGULATOR
GATEABLE 5V REG.
TIMING CIRCUIT
F
+22V at 7A
GND
+5V at 5A
SCLRO
CI
CIA
AUX 1
AUX 2
AUX 3
SBAC 1
SBAC 2
CHASSIS GND
+BATT
+BATT
-BATT
FAN
FAN
1
2
3
4
5
6
7
8
9
10
11
12
TB4
SIB
SIC
SID
TB2
ISOLATION RECTIFICATION AND FILTERING
BATTERY CHARGER
60 HZ INVERTER
12V INTERNAL BATTERY

Figure 2. 34-014 Power Supply Functional Block Diagram

4.3 Memory Power Switch

The memory power switch is located on the front panel of the 34-014 power supply (normally mounted on the rear uprights of the Model 80 enclosure). This switch is normally left in the ON position since turning this switch off would remove power to the memory causing stored information to be lost. However, there are times when power must be removed from the memory (e.g., making repairs). The memory power switch provides the only normal means of removing power from the memory.

In addition to removing power from the memory, the memory power switch also disconnects the battery from its load. Therefore, this switch is always off when the system is stored, shipped or even temporarily disconnected from any primary power source. This prevents unnecessary discharge of the batteries.

4.4 24-043 and 24-043F01 Batteries

A standard system may have as battery backup a 24-043 battery or one or more 24-043F01 batteries. The 24-043 battery is internal to the 34-014 power supply, and is capable of holding standby mode for up to 30 minutes. The 24-043F01 batteries are larger and are located in a battery compartment at the bottom of the standard equipment enclosure. Eighteen hours of standby mode can be expected for each 34-043F01 battery installed. If more than one 34-043F01 battery is installed, only a simple parallel battery connection is required. If 34-043F01 batteries are equipped, the internal battery is not equipped.

Battery Maintenance - The only maintenance required for the 24-043 batteries is to maintain proper charge. An annual replacement is recommended to maintain reliable back-up power.

4.5 Battery Connection

When the internal battery (24-043) is equipped, TB4-7 must be jumpered to TB4-8 on the 34-014 power supply. If one or more external batteries (24-043F01) are equipped, do not jumper TB4-7 to TB4-8. Connect the + and - terminals of the batteries to TB4-7 and TB4-9 respectively. An External Battery Kit (39-019) is available. The kit is complete and includes 24-043F01 battery, mounting hardware, and cable. Additional jumpering is required by the power supply when 24-043F01 batteries are equipped. See Section 4.6 and External Battery Kit Drawing 39-019C20.

4.6 Battery Charger

The 34-014 power supply provides battery charging. However, proper jumpering of the charger is required to match its characteristics to the battery selected by the customer. The jumpering is performed on the upper plug-in circuit card which is accessed by removing the front cover plate of the 34-014 power supply.

The options and required jumpering are:

BATTERY TYPE	JUMPER	JUMPERS CHARGE RATE
24-043	E2 to E3	.5 Amperes
24-043F01 (one or more)	E1 to E2	3.0 Amperes

4.7 AC Backup

If AC backup power is required instead of battery backup, the 34-014 need only to be connected to the AC source. The supply is designed to accept 115/230 VAC, 50/60Hz directly. A wide amplitude tolerance of +20-30% is acceptable on the AC backup input.

The supply is designed to accept either AC backup or battery backup or both. Both could be used if AC backup were not constantly present, but would be applied a short time following a loss of normal line power. In this system the AC backup must be applied before the battery backup became discharged. Before applying AC backup power check for the proper jumpering of TB2 in the 34-014 power supply.

INPUT	JUMPERS
115VAC	TB2-1 to TB2-2
	TB2-3 to TB2-4
230VAC	TB2-2 to TB2-3

Backup AC is connected to TB4 as follows:

Line ——— TB4-4

Neutral —— TB4-5

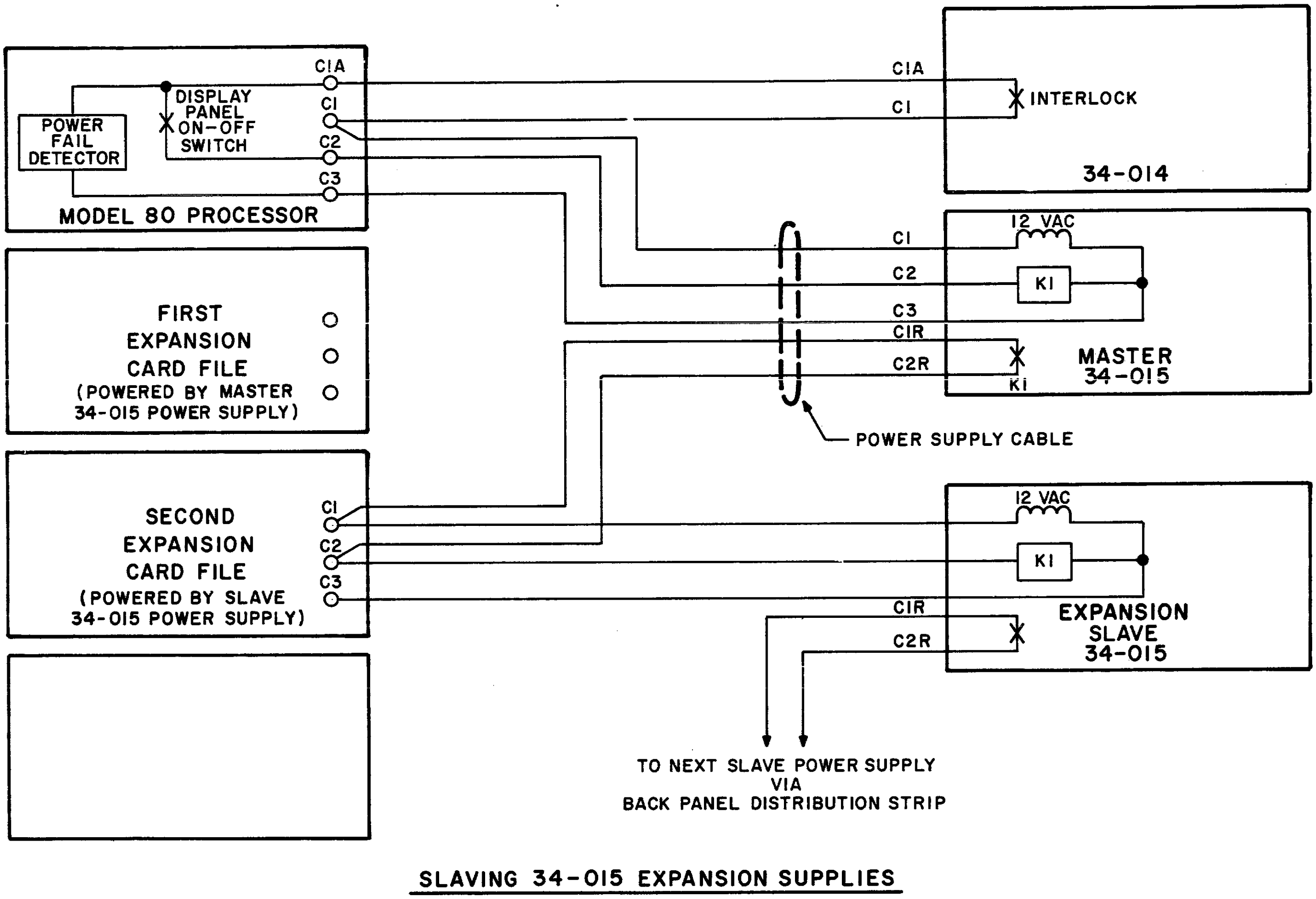
Earth ——— TB4-6

4.8 Auxiliary Fan

Some system configurations require an auxiliary fan. In the event of a power failure, heat stored in the mass of the power supplies and loads causes air temperature inside the enclosure to rise rapidly because fan power to the main blowers is also lost. Since Model 80 memories lose stored information if air temperatures rise too high, an auxiliary fan (Rotron whisper fan) can be provided to prevent this loss. This fan runs under normal power conditions and also under battery operation. The fan leads connect to the fan terminal of TB4 on the 34-014 power supply.

5. POWER CONTROL

Power control circuit diagram of the Model 80 Power System is shown in Figure 3. The leads C1 and C2 are the remote on/off switch lead. However, the C1 lead returns to the 34-014 power supply where a relay contact is placed in series with it and the C1A lead. The circuit returns to the Model 80 back-panel as "C1A". The relay contact in the 34-014 power supply is an interlock which prevents power turn on of the system if the memory power supply is not supplied primary power.



C1A
DISPLAY PANEL ON-OFF SWITCH
C1
C2
C3
POWER FAIL DETECTOR
MODEL 80 PROCESSOR
FIRST EXPANSION CARD FILE (POWERED BY MASTER 34-015 POWER SUPPLY)
SECOND EXPANSION CARD FILE (POWERED BY SLAVE 34-015 POWER SUPPLY)
C1A
C1
INTERLOCK
34-014
12 VAC
K1
C1
C2
C3
C1R
C2R
MASTER 34-015
POWER SUPPLY CABLE
12 VAC
K1
C1R
C2R
EXPANSION SLAVE 34-015
TO NEXT SLAVE POWER SUPPLY VIA BACK PANEL DISTRIBUTION STRIP
SLAVING 34-015 EXPANSION SUPPLIES

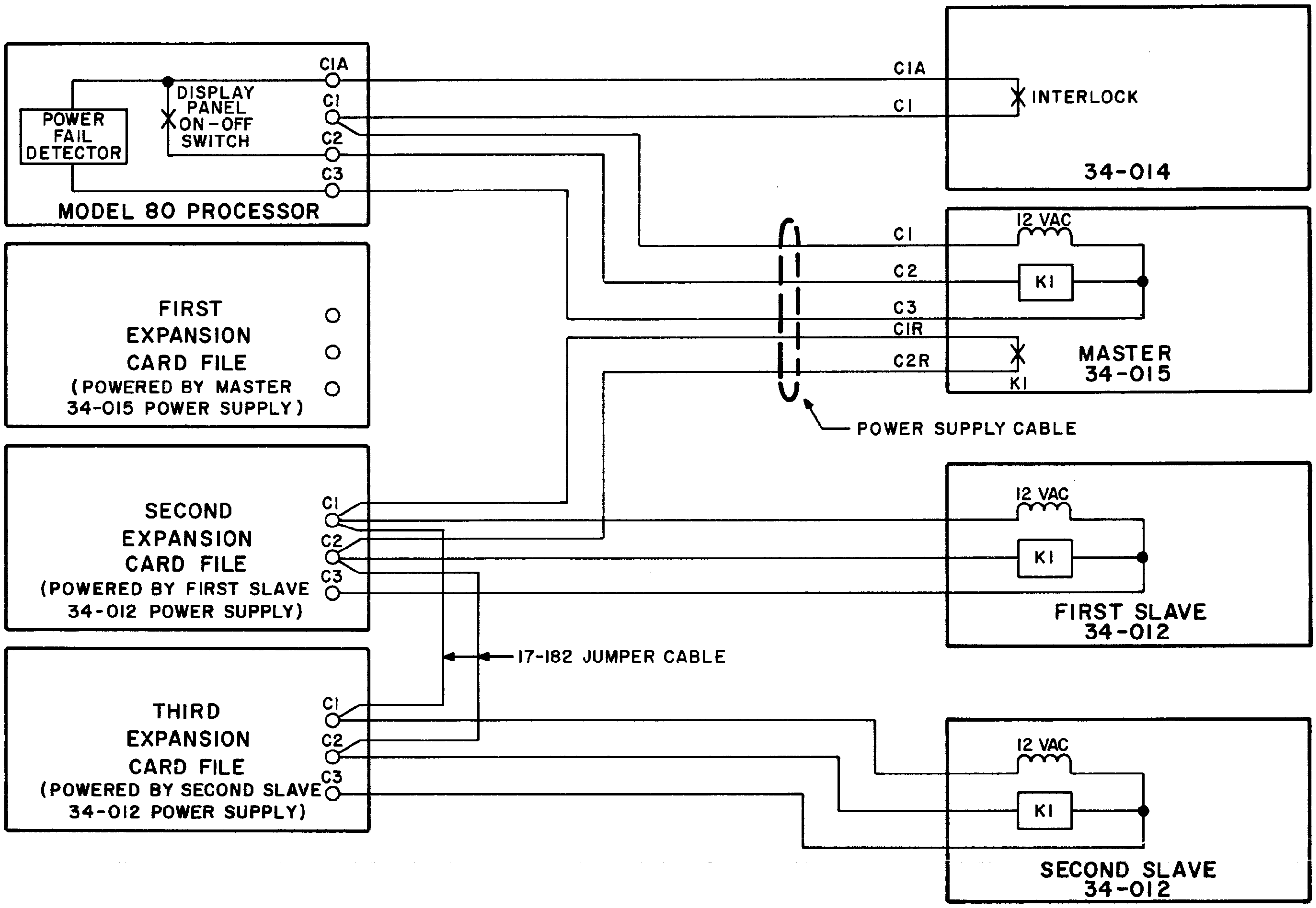
Figure 3. 34-015 Power Control Circuit Diagram

A slave contact in the first or master 34-015 power supply permits slave control of the slave expansion power supply. The leads for this contact are C1R and C2R. These leads connect to the C1 and C2 leads of the slave expansion supply thereby providing the on/off function. Additional supplies would connect in the same manner.

6. 34-012 EXPANSION POWER SUPPLY

Some system configurations may have 34-012 expansion supplies. This supply provides P5, P15, and N15. Its outputs are fused rather than electronically short circuit protected. The outputs are also overvoltage protected and regulated to ±1%. The drawing number for the circuit schematic is 34-012D08.

When expanding power with 34-012 power supplies the first slave 34-012 power supply uses the C1R and C2R leads from the master 34-015 power supply. A second slave 34-012 power supply would require a 17-182 jumper cable. Slave 34-012 power supplies all slave the one contact provided by the master 34-015 power supply.


POWER FAIL DETECTOR
DISPLAY PANEL ON-OFF SWITCH
C1A
C1
C2
C3
MODEL 80 PROCESSOR
FIRST EXPANSION CARD FILE (POWERED BY MASTER 34-015 POWER SUPPLY)
SECOND EXPANSION CARD FILE (POWERED BY FIRST SLAVE 34-012 POWER SUPPLY)
THIRD EXPANSION CARD FILE (POWERED BY SECOND SLAVE 34-012 POWER SUPPLY)
17-182 JUMPER CABLE
INTERLOCK
34-014
12 VAC
K1
C1R
C2R
MASTER 34-015
POWER SUPPLY CABLE
FIRST SLAVE 34-012
SECOND SLAVE 34-012

SLAVING 34-012 EXPANSION SUPPLIES

Figure 4. 34-012 Power Control Circuit Diagram

7. PRIMARY POWER REQUIREMENTS

Both the 34-014 and the 34-015 power supplies have 115VAC or 230VAC primary power options. Voltage range is ±10% in either case. Line frequency tolerance is 47 to 63Hz.

The 115/230 VAC option is selected by proper jumpering of the power supplies transformer primaries. See appropriate schematics (34-014D08 or 34-015D08) for jumpering information.

Line requirement is:

34-014	3.5 Amperes at 115VAC 1.6 Amperes at 230VAC
34-015	7.0 Amperes at 115VAC 3.5 Amperes at 230VAC
34-012	6.0 Amperes at 115VAC 3.0 Amperes at 230VAC

7.1 Procedure for Conversion from 115 to 230 Volt Operation

7.1.1 34-014 Power Supply Conversion. The 34-014 Power Supply is converted as follows:

1. Remove top cover plate.
2. Remove jumpers:

   TB1-1 to TB1-2
   TB1-3 to TB1-4
   TB2-1 to TB2-2
   TB2-3 to TB3-4

3. Add jumpers:

   TB1-2 to TB1-3
   TB2-2 to TB2-3

4. Replace fuse F1 with A B C - 5 fuse (5 Ampere fuse) (INTERDATA Part Number 24-042F02).
5. Replace cover plate.

7.1.2 34-015 Power Supply Conversion. The 34-015 Power Supply is converted as follows:

1. Remove eight screws as shown in Figure 5.
2. Remove top panel.
3. Loosen two screws as shown and swing rear panel down, TB101 is now exposed.
4. Remove jumpers:

   TB101-1 to TB101-2
   TB101-3 to TB101-4
   TB101-7 to TB101-8
   TB101-9 to TB101-10

5. Add jumpers:

   TB101-2 to TB101-3
   TB101-8 to TB101-9

6. Replace fuse F1 with A B C - 8 (8 Ampere fuse) (INTERDATA Part Number 24-042F01).
7. Replace panels and screws.

NOTE

It is important to recognize that the previous procedures convert only the 34-014 and 34-015 system power supplies. Any other supplies or devices that use primary power must be tailored to the systems requirements. Consult documentation of other products involved.

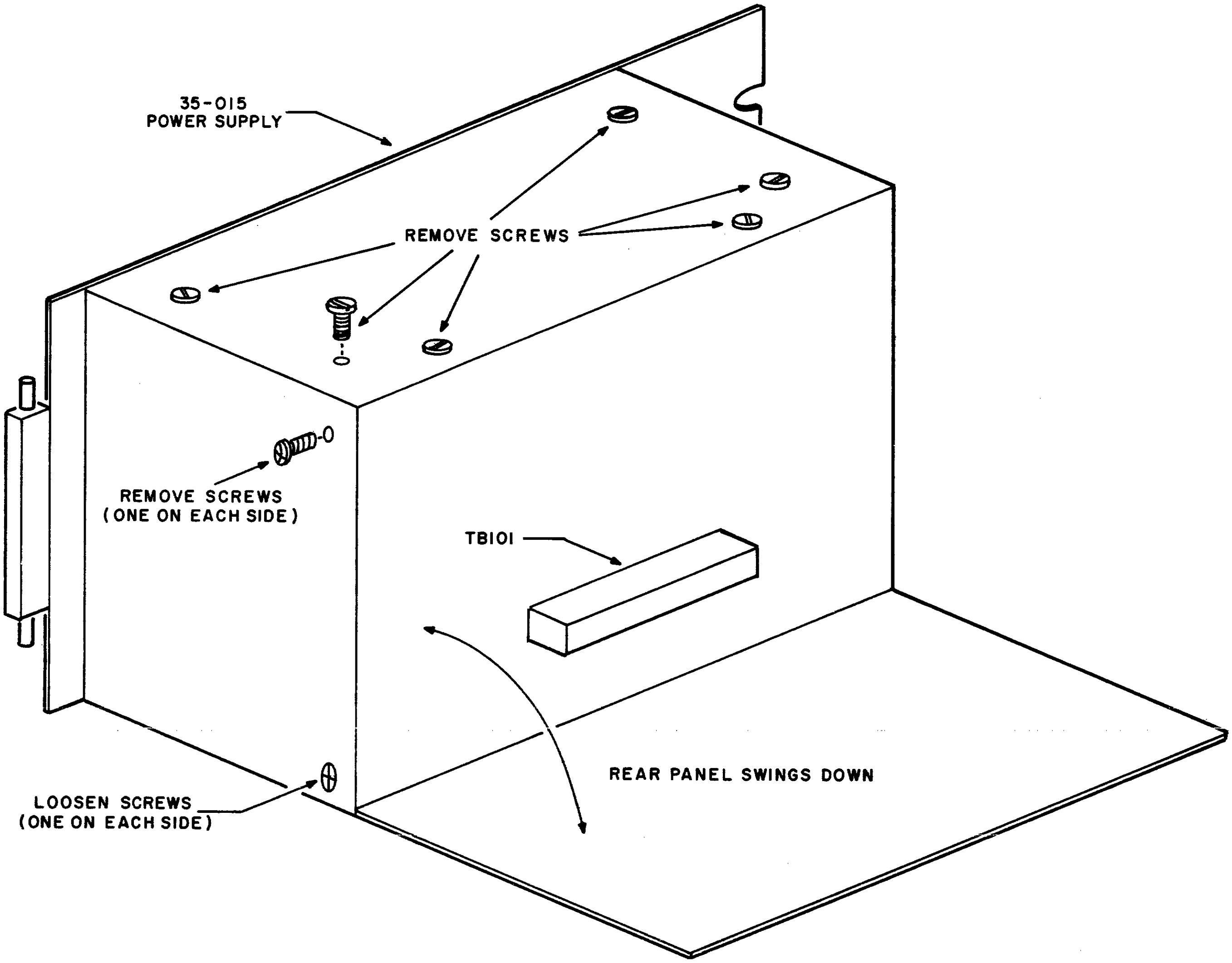

35-015
POWER SUPPLY
REMOVE SCREWS
REMOVE SCREWS
(ONE ON EACH SIDE)
TB101
REAR PANEL SWINGS DOWN
LOOSEN SCREWS
(ONE ON EACH SIDE)

Figure 5. 34-015 Power Supply 115/230 VAC Conversion

8. SYSTEM CARD FILE FANS

Fans equipped in system card files are powered by the system power supply driving the card file. The 34-015 power supply drives the fans first two card files in the standard Model 80 configuration. Two fan connectors are supplied in the 34-015 power supplies output cable and connect to the fans via the three pin mole connector equipped on the back of each card file. The power supply, supplies 115 VAC power to the fans whether the supply is connected for either 230 VAC operation or 115 VAC operation. The power supplies power transformer steps down the 230 VAC to provide the required power to the fans.

9. ADJUSTMENTS

Several adjustments exist in the Model 80 Power System. All power system adjustments are made at the factory and should never require readjustment in the field. If readjustment becomes necessary, the recommended settings are given in the following paragraphs.

9.1 Voltage Adjustments

Mnemonic	Voltage Setting	Power Supply
P5	+5.10 volts	34-012 and 34-015
P15	+15.4 Volts	34-012 and 34-015
N15	-15.00 volts	34-012 and 34-015
P5S	+5.10 volts	34-014
P22	+21.00 volts	34-014

Voltages are always measured at the back panel when making adjustments.

9.2 Crowbar Adjustments (Overvoltage)

Crowbar	Firing Voltage	Power Supply
P5	+6.3 volts	34-015
P15	+17.0 volts	34-015
N15	-17.0 volts	34-015
P5	+6.0 volts	34-012
P15	+19.0 volts	34-012
N15	-19.0 volts	34-012
P5S	+6.3 volts	34-014
P22	+26.0 volts	34-014

All firing voltages are measured at the back panel when making adjustments. All voltage adjusting potentiometers are labeled and accessed at the front panel of the power supply.

9.3 P5S Standby Mode Timing Adjustments

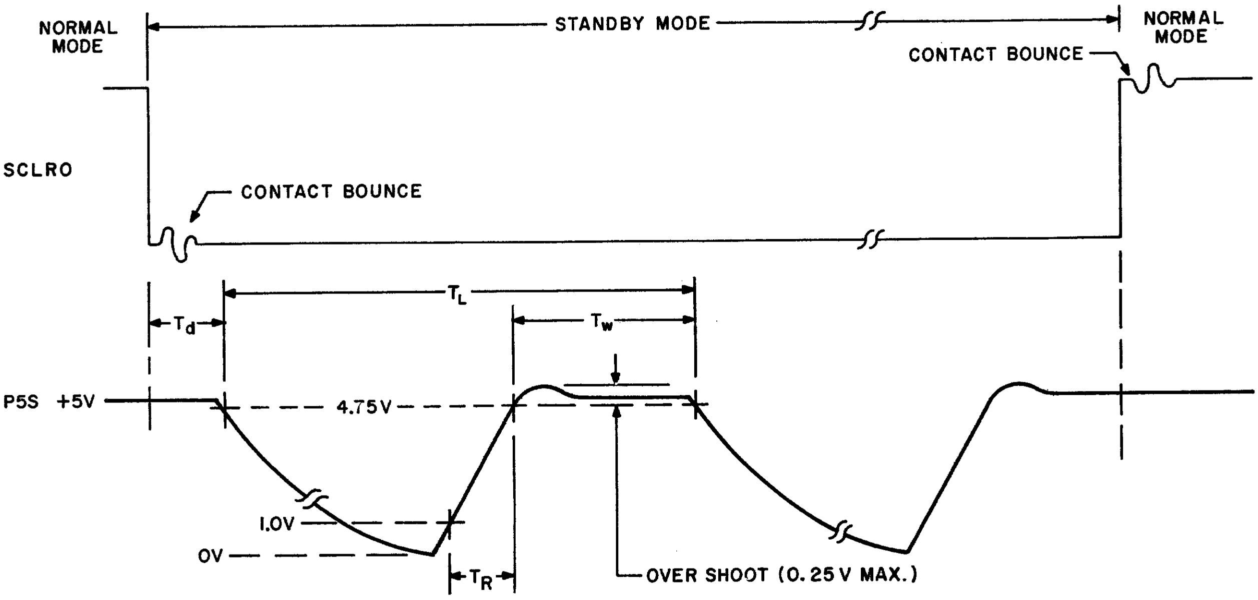
A nominal timing diagram of the P5S output while in standby mode is shown in Figure 6. If the actual timing is not within ±10% of the nominal timing, readjustment is required. The adjusting potentiometers are located on the lower plug-in circuit card of the 34-014 power supply. These potentiometers are accessed by removing the cover plate on the front panel of the supply.

The P5S timing adjustment sequence is as follows:

1. Turn the Console Power Switch to the OFF position. (This places the power system in the Standby mode).
2. Adjust T (off time) first.

   Adjust Tw (width) second.
3. Adjust Td (delay) third.

Potentiometer R157 is used to adjust Td. The circuit card cover must be removed from the power supply to provide access to this potentiometer. When adjusting Td (R157) the Console Power Switch must be in the ON position. R157 is adjusted for a measured DC voltage of 10.0 volts across C107. C107 is also located on the lower circuit card of the 34-014 power supply.



T_d = 30 μsec ± 10 μsec
T_w = 20 μsec ± 2.5 μsec
T_L = 2 m sec ± .1 millisec.
T_R = 50 μsec TYP.

NOTES:

1. IF SCLRO RISING EDGE OCCURS DURING THE T_L INTERVAL, T_L SHALL RUN IT'S SPECIFIED TIME.
2. IF SCLRO RISING EDGE OCCURS DURING THE T INTERVAL, P5S SIMPLY REMAINS AT IT'S SPECIFIED LEVEL UNTIL SCLRO GOES LOW AGAIN.
3. CIRCUITRY SHALL IGNORE CONTACT BOUNCE FOR 5 msec AFTER INITIAL TRANSITION.

Figure 6. P5S Timing Diagram

9.4 Battery Charger Adjustments

The following procedure should be used to adjust the battery charger equipped in the 34-014 power supply.

1. Disconnect battery from charger. This can be done at the battery terminals.
2. Place a 1000 ohm resistor across battery charger output.
3. Adjust voltage across the 1000 ohm resistor to 13.9 volts. This adjustment is located on the lower plug-in circuit card of the 34-014 power supply.
4. Remove the 1000 ohm resistor and reconnect battery.

10. INTERLOCK

The interlock is adjusted with a variable line transformer. Set the input voltage of the 34-014 power supply to 90 VAC. Start with R212 of the 34-014 power supply in its most clockwise position. Slowly turn R212 counter-clockwise until a short is observed between TB4-2 and TB4-3. The adjustment is then complete.

11. SHIPPING AND STORAGE

The power switch on the front panel of the 34-014 power supply should always be turned to the OFF position and the internal battery removed when the supply is shipped or stored.

MODEL 80
POWER SUPPLY
INSTALLATION SPECIFICATION

1. INTRODUCTION

This Installation Specification applies to any Model 80 Computer System which is to include one or more of the following components:

34-020 (Replaces 34-015)	50 Ampere Power Supply
New Card File	New card files are those with a fan switch mounted on their back panel as shown in Figure 1. (Old card files are shown in Figure 2.)

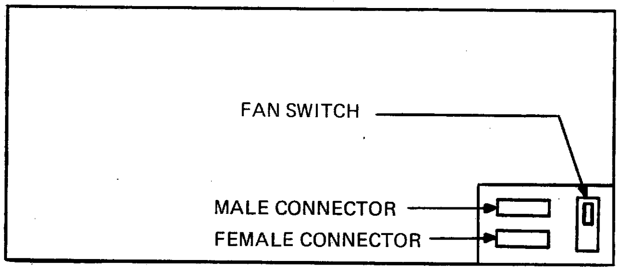


Figure 1. New Card File (Back Panel View)

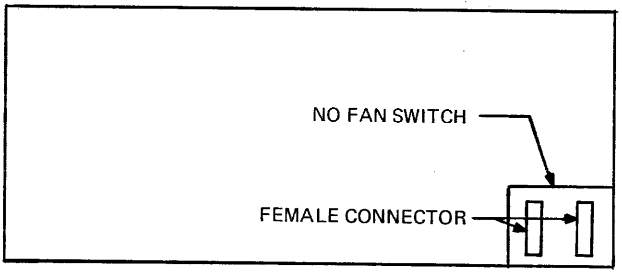


Figure 2. Old Card File (Back Panel View)

2. PROCEDURE

Table 1 lists eight possible combinations of card file (new or old), 50 Amperes Power Supply (34-015 or 34-020), and line voltage (115 or 230 VAC). Table 1 identifies installation procedures for the various possible combinations. Figures 3, 4, 5 and installation drawings for the 39-021 Modification Kit are used in conjunction with Table 1 to describe installation procedures not covered by the Model 80 02-261A12 Power System Description.

NOTE

When powering a Model 80 Processor with new card file, the C1 lead of the 34-020 or 34-015 output cable must terminate on the Processor card files C1A terminal rather than the C1 terminal. See Figures 3 and 5.

TABLE 1. INSTALLATION PROCEDURE TABLE

Mfg. Variation	Card File	Power Supply	Line Voltage	C1-C2 Jumper (17-182)	TA-TB Terminator	Card File Modifications (Kit 39-021)	Fan Switch
M01	New	34-020	115VAC	Required if expansion supply is equipped. Supplied with Expansion card file. See Figure 3.	Required. Equipped by Manufacturing. See Figure 4.	Not required.	Set to 115 VAC
Non-Standard	Old	34-020	115VAC	Required if expansion supply is equipped. Supplied by 39-021 Kit. See Figure 3.	Required. Supplied as part of Kit 39-021F02 See Figure 4 and 39-021A12.	Card file must be modified. Use Kit 39-021F02. See Figure 4 and 39-021A12.	Does not exist
Non-Standard	New	34-015	115VAC	Not required; If expansion supply is equipped use C1R-C2R. See Figure 5.	Not required. Equipped by Manufacturing.	Not required.	Set to 115 VAC
M00	Old	34-015	115VAC	Not required; If expansion supply is equipped use C1R-C2R. See Figure 5.	Not required. Not equipped.	Not required.	Does not exist
M01	New	34-020	230VAC	Required; If expansion supply is equipped Supplied with expansion card file. See Figure 3.	Required. Equipped by Manufacturing. See Figure 4.	Not Required.	Set to 230 VAC
Non-Standard	Old	34-020	230VAC	Required if expansion supply is equipped. Supplied by Kit 39-021 See Figure 3.	Required. Supplied as part of Kit 39-021F01 See Figure 4 and 39-021A12.	Note 1 Required. Use Kit 39-021F01 See Figure 4 and 39-021A12.	Set to 230 VAC
Non-Standard	New	34-015	230VAC	Not required; If expansion supply is equipped Use C1R-C2R See Figure 5.	Not required. Equipped by Manufacturing.	Not required.	Set to 115 VAC
M00	Old	34-015	230VAC	Not required; If expansion supply is equipped Use C1R-C2R See Figure 5.	Not required. Not equipped.	Not required.	Does not exist

Note 1:

Alternate is a new card file.

3. 39-021 CARD FILE MODIFICATION KIT

39-021 Card File Modification Kit is designed to make old card files compatible with new power supplies (34-020).

Old card files are those with no fan switch mounted on their back panels as shown in Figure 2.

Two functional variations of the 39-021 Kit are available:

> The 39-021F01 Modification Kit is used by any system where a 34-020 power supply is to be fitted to an old card file. The modified card file in this instance becomes a standard.
>
> The 39-021F02 Modification Kit is used by any system where a 34-020 power supply is to be fitted to an old card file and the line voltage for the system is 115 VAC rather than 230 VAC. The modified card file in this instance is compatible with the 34-020, but is non-standard. The 39-021F02 Modification is a simple plug/unplug type modification requiring only about 10 minutes, but is restricted to 115 VAC line installations only.

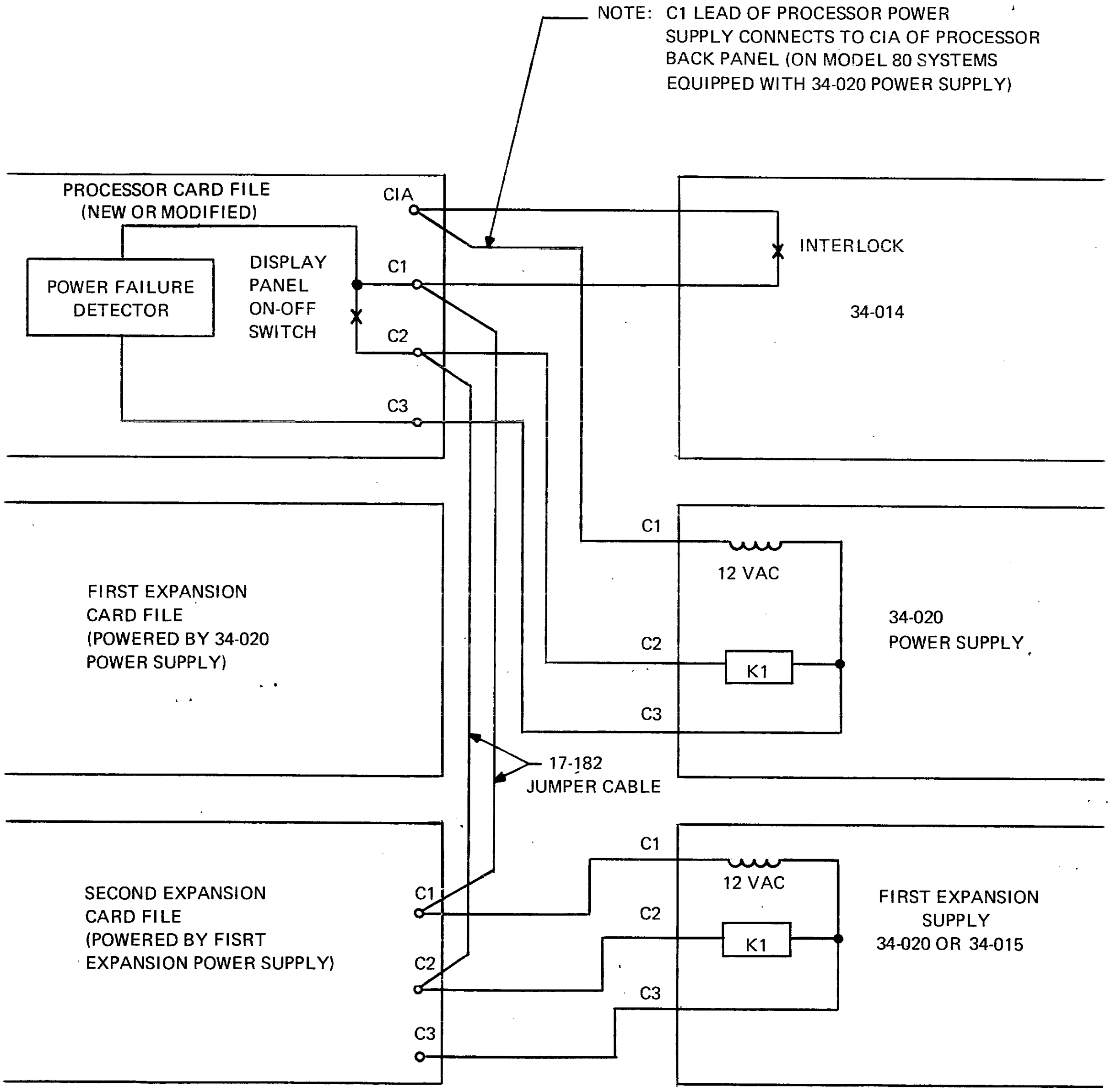

NOTE: C1 LEAD OF PROCESSOR POWER SUPPLY CONNECTS TO CIA OF PROCESSOR BACK PANEL (ON MODEL 80 SYSTEMS EQUIPPED WITH 34-020 POWER SUPPLY)
PROCESSOR CARD FILE (NEW OR MODIFIED)
CIA
POWER FAILURE DETECTOR
DISPLAY PANEL ON-OFF SWITCH
C1
C2
C3
INTERLOCK
34-014
C1
12 VAC
FIRST EXPANSION CARD FILE (POWERED BY 34-020 POWER SUPPLY)
C2
K1
34-020 POWER SUPPLY
C3
17-182 JUMPER CABLE
C1
12 VAC
SECOND EXPANSION CARD FILE (POWERED BY FISRT EXPANSION POWER SUPPLY)
C1
C2
K1
FIRST EXPANSION SUPPLY 34-020 OR 34-015
C2
C3
C3

Figure 3. C1-C2 Jumper Cable (17-182 Jumper Cable)

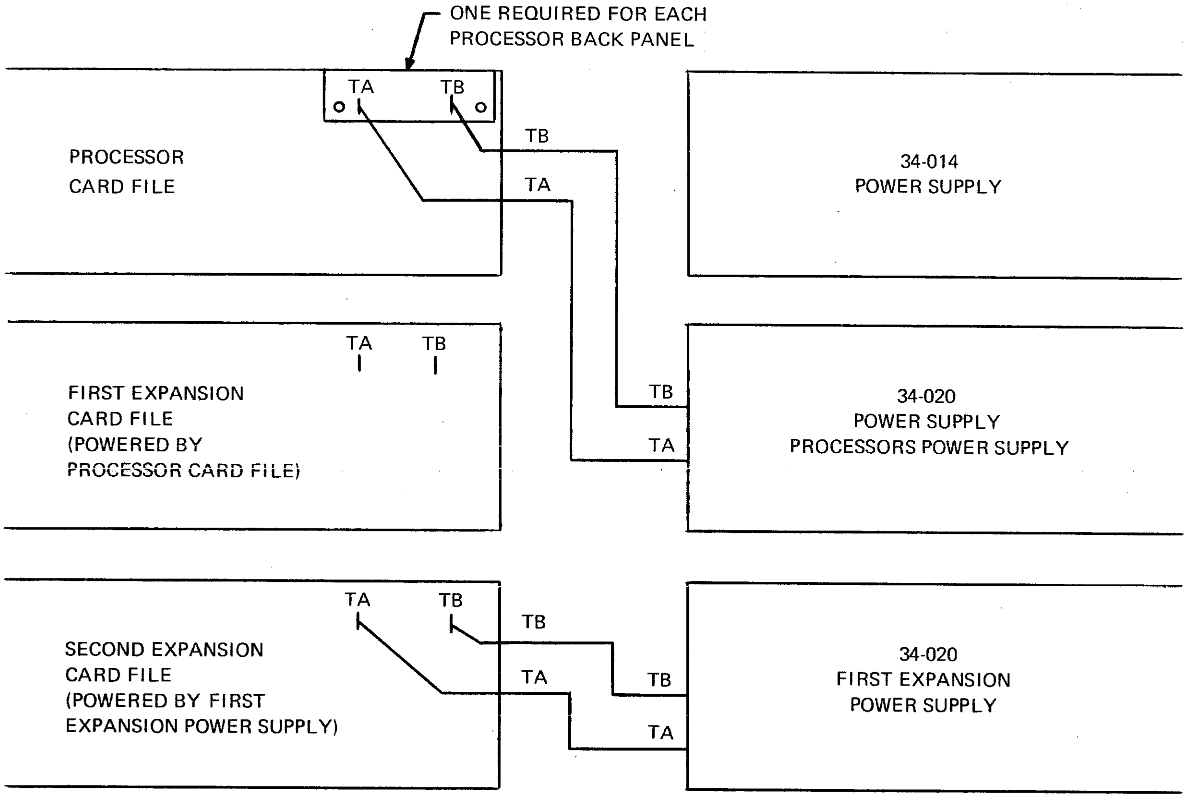

ONE REQUIRED FOR EACH
PROCESSOR BACK PANEL
TA
TB
TB
TA
PROCESSOR
CARD FILE
34-014
POWER SUPPLY
TA
TB
FIRST EXPANSION
CARD FILE
(POWERED BY
PROCESSOR CARD FILE)
TB
TA
34-020
POWER SUPPLY
PROCESSORS POWER SUPPLY
TA
TB
TB
TA
SECOND EXPANSION
CARD FILE
(POWERED BY FIRST
EXPANSION POWER SUPPLY)
TB
TA
34-020
FIRST EXPANSION
POWER SUPPLY

Figure 4. TA - TB Connections

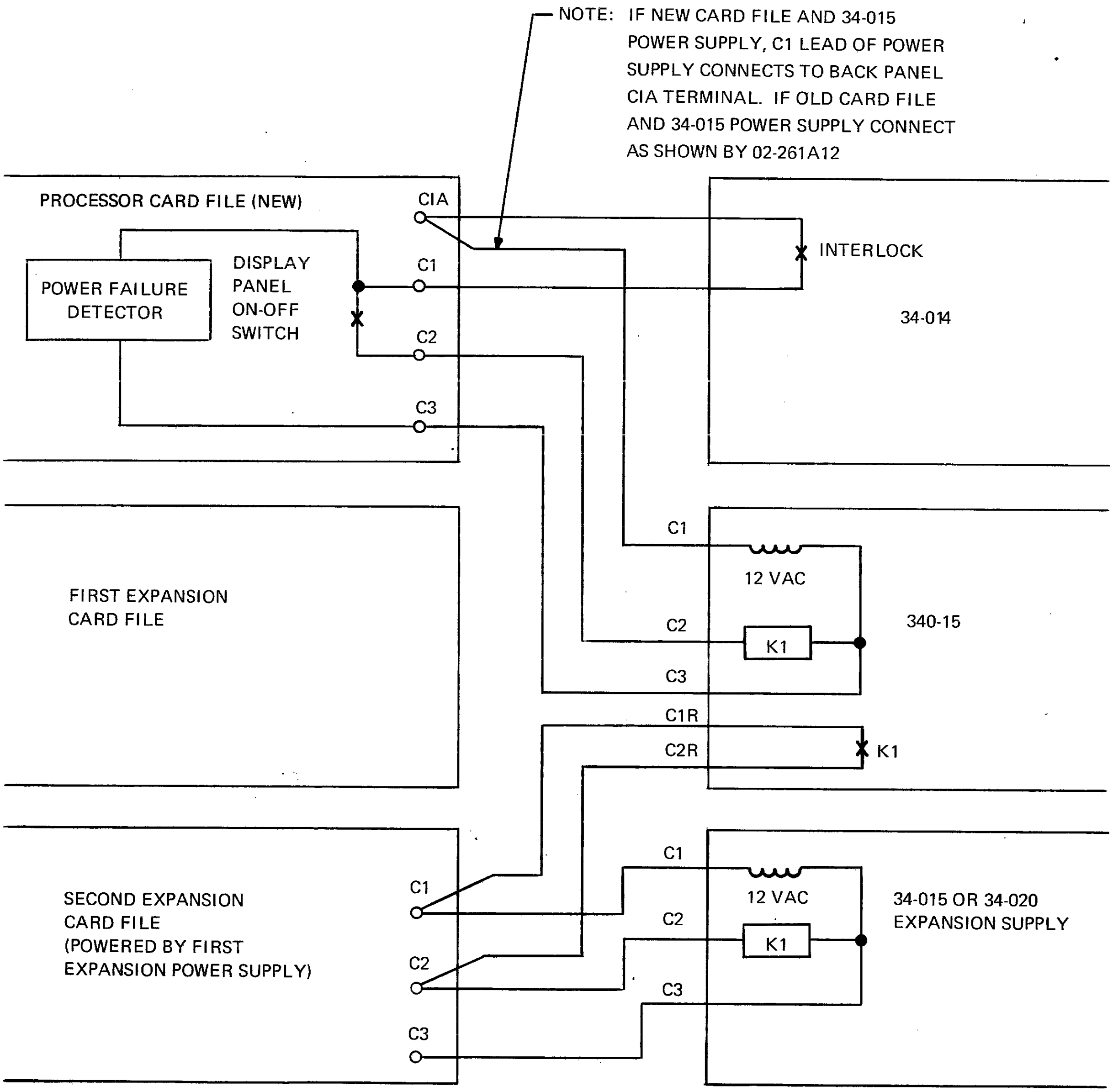

NOTE: IF NEW CARD FILE AND 34-015 POWER SUPPLY, C1 LEAD OF POWER SUPPLY CONNECTS TO BACK PANEL CIA TERMINAL. IF OLD CARD FILE AND 34-015 POWER SUPPLY CONNECT AS SHOWN BY 02-261A12
PROCESSOR CARD FILE (NEW)
CIA
POWER FAILURE DETECTOR
DISPLAY PANEL ON-OFF SWITCH
C1
C2
C3
INTERLOCK
34-014
FIRST EXPANSION CARD FILE
C1
12 VAC
C2
K1
C3
340-15
C1R
C2R
K1
SECOND EXPANSION CARD FILE (POWERED BY FIRST EXPANSION POWER SUPPLY)
C1
C2
C3
C1
12 VAC
C2
K1
C3
34-015 OR 34-020 EXPANSION SUPPLY

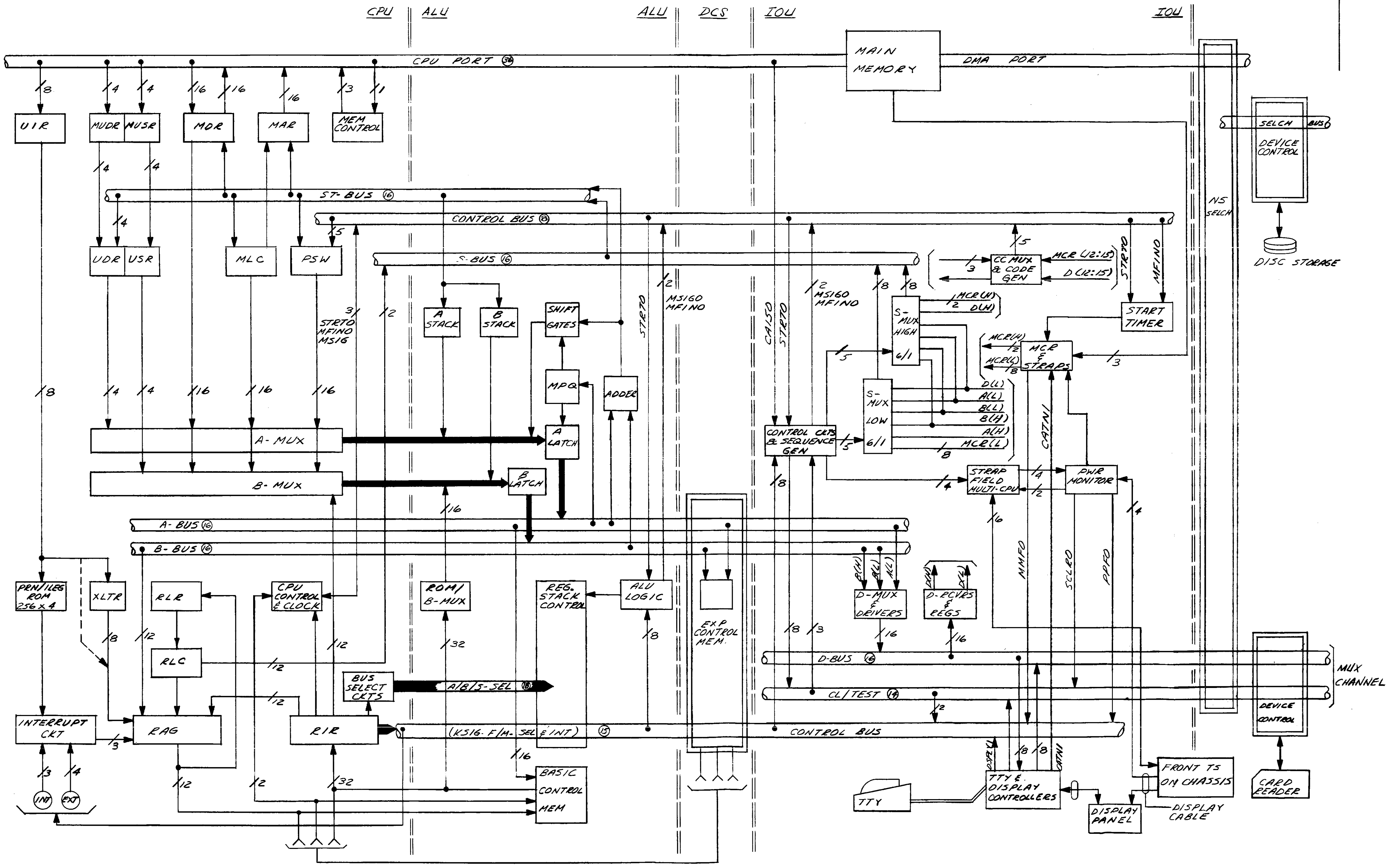
Figure 5. Power Control Using 34-015 Power Supply

DRAWINGS

INTERDATA®

REVISIONS			
PRE PRODUCTION APPROVAL		INIT.	DATE
	DEV	JW	1-29-13
	PROD		

MODEL 80 BLOCK DIAGRAM


CPU
ALU
ALU
DCS
IOU
IOU
CPU PORT (36)
MAIN MEMORY
DMA PORT
8
4
4
16
16
16
3
1
UIR
MUDR
MUSR
MDR
MAR
MEM CONTROL
4
4
ST-BUS (16)
CONTROL BUS (8)
4
5
UDR
USR
MLC
PSW
S-BUS (16)
3
STRTO MFINO MS16
2
A STACK
B STACK
SHIFT GATES
MPQ
ADDER
A LATCH
B LATCH
2
MS160 MFINO
STRTO
CAISO
STRTO
2
MS160 MFINO
8
8
S-MUX HIGH 6/1
5
S-MUX LOW 6/1
CONTROL CKTS & SEQUENCE GEN
5
8
CC MUX & CODE GEN
3
5
MCR (12:15)
D (12:15)
STRTO
MFINO
START TIMER
MCR(H)
2
D(H)
MCR(H)
2
MCR(L)
8
MCR & STRAPS
3
D(L)
A(L)
B(L)
B(H)
A(H)
MCR(L)
8
CATN1
STRAP FIELD MULTI-CPU
4
4
2
PWR MONITOR
4
6
NS SELCH
SELCH BUS
DEVICE CONTROL
DISC STORAGE
8
4
4
16
16
16
A-MUX
B-MUX
16
A-BUS (16)
B-BUS (16)
PRN/ILLEG ROM 256 x 4
XLTR
RLR
CPU CONTROL & CLOCK
ROM/ B-MUX
REG. STACK CONTROL
ALU LOGIC
EXP CONTROL MEM.
8
12
12
32
8
RLC
12
BUS SELECT CKTS
A/B/S-SEL (18)
12
INTERRUPT CKT
3
RAG
RIR
(KS16-F/M-SEL & INT) (15)
CONTROL BUS
16
3
4
INT
EXT
12
2
32
BASIC CONTROL MEM
B(H)
B(L)
A(L)
D-MUX & DRIVERS
D(H)
D(L)
D-RCVRS & REGS
16
16
8
3
D-BUS (16)
CL/TEST (14)
2
NMFO
SCLRO
PPFO
DSPLY
8
8
CATN1
TTY
TTY & DISPLAY CONTROLLERS
DISPLAY PANEL
DISPLAY CABLE
FRONT TS ON CHASSIS
MUX CHANNEL
DEVICE CONTROL
CARD READER

NOTES

NAME	TITLE	DATE
R. MEGINLEY	DRAFT	8-2-72
J. F. FLEMING	CHK	
S. MESSINA	ENGR	
D. W. YOUNG	SYS TEST	
R.E. JONES	DIR ENG	

TITLE MODEL 80 PROCESSOR

TASK NO. 03215

DWG NO. 01-053 008

SHEET OF 1-4

BRUNING 44-231 16042

INTERDATA®

BACK PANEL MAP

CONN.	TITLE	CPU-IOU		ALU-CPU		IOU-ALU		MBC-DCS		MSU-MBC		MSU-I/O		MSU-I/O		MSU-I/O	
	BD. LOC.	07		06		05		04		03		02		01		00	
	TERM. NO.	ROW 1	2	ROW 1	2	ROW 1	2	ROW 1	2	ROW 1	2	ROW 1	2	ROW 1	2	ROW 1	2
1	41	P5	GND	P5	GND	P5	GND	P5	GND	P5	GND	P5	GND	P5	GND	P5	GND
	40	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
	39	P15	TACKO	P15	TACKO	P15	TACKO	P15	P22	P15	P22	P15	P22	P15	P22	P15	P22
	38	N15	RACKO	N15	RACKO	N15	RACKO	N15	P5S	N15	P5S	N15	P5S	N15	P5S	N15	P5S
	37	CD141	CD151	CD141	CD151	CD141	CD151	CD141	CD151	CD141	CD151	MD150	SP8	MD150	SP8	MD150	SP8
	36	CD121	CD131	CD121	CD131	CD121	CD131	CD121	CD131	CD121	CD131	MD130	MD140	MD130	MD140	MD130	MD140
	35	CD101	CD111	CD101	CD111	CD101	CD111	CD101	CD111	CD101	CD111	MD110	MD120	MD110	MD120	MD110	MD120
	34	CD081	CD091	CD081	CD091	CD081	CD091	CD081	CD091	CD081	CD091	MD090	MD100	MD090	MD100	MD090	MD100
	33	CD061	CD071	CD061	CD071	CD061	CD071	CD061	CD071	CD061	CD071	MD070	MD080	MD070	MD080	MD070	MD080
	32	CD041	CD051	CD041	CD051	CD041	CD051	CD041	CD051	CD041	CD051	MD050	MD060	MD050	MD060	MD050	MD060
	31	CD021	CD031	CD021	CD031	CD021	CD031	CD021	CD031	CD021	CD031	MD030	MD040	MD030	MD040	MD030	MD040
	30	CD001	CD011	CD001	CD011	CD001	CD011	CD001	CD011	CD001	CD011	MD010	MD020	MD010	MD020	MD010	MD020
	29	CA140	CA150	CA140	CA150	CA140	CA150	CA140	CA150	CA140	CA150		MD000		MD000		MD000
	28	CA120	CA130	CA120	CA130	CA120	CA130	CA120	CA130	CA120	CA130						
	27	CA100	CA110	CA100	CA110	CA100	CA110	CA100	CA110	CA100	CA110						
	26	CA080	CA090	CA080	CA090	CA080	CA090	CA080	CA090	CA080	CA090	SCLRO	HWO	SCLRO	HWO	SCLRO	HWO
	25	CA060	CA070	CA060	CA070	CA060	CA070	CA060	CA070	CA060	CA070						
	24	CA040	CA050	CA040	CA050	CA040	CA050	CA040	CA050	CA040	CA050						
	23	CA020	CA030	CA020	CA030	CA020	CA030	CA020	CA030	CA020	CA030	SYNO	ATNO	SYNO	ATNO	SYNO	ATNO
	22											RACKO	TACKO	RACKO	TACKO	RACKO	TACKO
	21	CA000	CA010	CA000	CA010	CA000	CA010	CA000	CA010	CA000	CA010	CL070	DAO	CL070	DAO	CL070	DAO
	20	CREQO	CFTCHO	CREQO	CFTCHO	CREQO	CFTCHO	CREQO	CFTCHO	CREQO	CFTCHO	DRO	CMDO	DRO	CMDO	DRO	CMDO
	19	CRDYO	CWRTO	CRDYO	CWRTO	CRDYO	CWRTO	CRDYO	CWRTO	CRDYO	CWRTO	SRO	ADRSO	SRO	ADRSO	SRO	ADRSO
	18	A140	A150	A140	A150	A140	A150	A140	A150	A140	A150	D140	D150	D140	D150	D140	D150
	17	A120	A130	A120	A130	A120	A130	A120	A130	A120	A130	D120	D130	D120	D130	D120	D130
	16	A100	A110	A100	A110	A100	A110	A100	A110	A100	A110	D100	D110	D100	D110	D100	D110
	15	A080	A090	A080	A090	A080	A090	A080	A090	A080	A090	D080	D090	D080	D090	D080	D090
	14	A060	A070	A060	A070	A060	A070	A060	A070	A060	A070	D060	D070	D060	D070	D060	D070
	13	A040	A050	A040	A050	A040	A050	A040	A050	A040	A050	D040	D050	D040	D050	D040	D050
	12	A020	A030	A020	A030	A020	A030	A020	A030	A020	A030	D020	D030	D020	D030	D020	D030
	11	A000	A010	A000	A010	A000	A010	A000	A010	A000	A010	D000	D010	D000	D010	D000	D010
	10	S140	S150	S140	S150	S140	S150	WRTOA	MSD000	WRTOA	MSD000	WRTOA	MS000	WRTOA	MS000	WRTOA	MS000
	09	S120	S130	S120	S130	S120	S130	MSD010	MSD020	MSD010	MSD020	MS010	MS020	MS010	MS020	MS010	MS020
	08	S100	S110	S100	S110	S100	S110	MSD030	MSD040	MSD030	MSD040	MS030	MS040	MS030	MS040	MS030	MS040
	07	S080	S090	S080	S090	S080	S090	MSD050	MSD060	MSD050	MSD060	MS050	MS060	MS050	MS060	MS050	MS060
	06	S060	S070	S060	S070	S060	S070	MSD070	MSD080	MSD070	MSD080	MS070	MS080	MS070	MS080	MS070	MS080
	05	S040	S050	S040	S050	S040	S050	MSD090	MSD100	MSD090	MSD100	MS090	MS100	MS090	MS100	MS090	MS100
	04	S020	S030	S020	S030	S020	S030	MSD110	MSD120	MSD110	MSD120	MS110	MS120	MS110	MS120	MS110	MS120
	03	S000	S010	S000	S010	S000	S010	MSD130	MSD140	MSD130	MSD140	MS130	MS140	MS130	MS140	MS130	MS140
	02	GCC1	LCC1	GCC1	LCC1	GCC1	LCC1	MSD150	SP7	MSD150	SP7	MS150	SP7	MS150	SP7	MS150	SP7
	01	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
	00	P5	GND	P5	GND	P5	GND	P5	GND	P5	GND	P5	GND	P5	GND	P5	GND
		1	2	1	2	1	2	1	2	1	2	1	2	1	2	1	2
0	41	P5	GND	P5	GND	P5	GND	P5	GND	P5	GND	P5	GND	P5	GND	P5	GND
	40	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
	39	P15	SCCO	P15	SCCO	P15	SCCO	P15	REQO	P15	REQO	P15	REQO	P15	REQO	P15	REQO
	38	N15	CCC1	N15	CCC1	N15	CCC1	N15	ENO	N15	ENO	N15	ENO	N15	ENO	N15	ENO
	37	IAO	VCC1	IAO	VCC1	IAO	VCC1	IAO		IAO							TACO
	36	IPFO	DPFO	IPFO	DPFO	IPFO	DPFO	IPFO	DPFO	IPFO	DPFO						
	35	B140	B150	B140	B150	B140	B150	MB020	B150	MB020	B150						
	34	B120	B130	B120	B130	B120	B130	MB000	MB010	MB000	MB010					XRACKO	
	33	B100	B110	B100	B110	B100	B110	MA130	MA140	MA130	MA140	MA130	MA140	MA130	MA140	MA130	MA140
	32	B080	B090	B080	B090	B080	B090	MA110	MA120	MA110	MA120	MA110	MA120	MA110	MA120	MA110	MA120
	31	B060	B070	B060	B070	B060	B070	MA090	MA100	MA090	MA100	MA090	MA100	MA090	MA100	MA090	MA100
	30	B040	B050	B040	B050	B040	B050	MA070	MA080	MA070	MA080	MA070	MA080	MA070	MA080	MA070	MA080
	29	B020	B030	B020	B030	B020	B030	MA050	MA060	MA050	MA060	MA050	MA060	MA050	MA060	MA050	MA060
	28	B000	B010	B000	B010	B000	B010					RDACKO	TDACKO	RDACKO	TDACKO	RDACKO	TDACKO
	27	KSIGO	PVMDO	KSIGO	PVMDO	KSIGO	PVMDO		PVMDO		PVMDO	DCO	DCRO	DCO	DCRO	DCO	DCRO
	26	SCLRO	HWO	SCLRO	HWO	SCLRO	HWO	SCLRO		SCLRO		SCLRO	HWO	SCLRO	HWO	SCLRO	HWO
	25	CB020	DCRO	CB020	DCRO	CB020	DCRO	CB020		CB020							
	24	CB000	CB010	CB000	CB010	CB000	CB010	CB000	CB010	CB000	CB010						
	23	SYNO	ATN000	SYNO	ATN000	SYNO	ATN000					SYNO	ATNO	SYNO	ATNO	SYNO	ATNO
	22	DACKO	ACKO	DACKO	ACKO	DACKO	ACKO					RACKO	TACKO	RACKO	TACKO	RACKO	TACKO
	21	CL070	DAO	CL070	DAO	CL070	DAO					CL070	DAO	CL070	DAO	CL070	DAO
	20	DRO	CMDO	DRO	CMDO	DRO	CMDO					DRO	CMDO	DRO	CMDO	DRO	CMDO
	19	SRO	ADRSO	SRO	ADRSO	SRO	ADRSO					SRO	ADRSO	SRO	ADRSO	SRO	ADRSO
	18	D140	D150	D140	D150	D140	D150					D140	D150	D140	D150	D140	D150
	17	D120	D130	D120	D130	D120	D130					D120	D130	D120	D130	D120	D130
	16	D100	D110	D100	D110	D100	D110					D100	D110	D100	D110	D100	D110
	15	D080	D090	D080	D090	D080	D090					D080	D090	D080	D090	D080	D090
	14	D060	D070	D060	D070	D060	D070					D060	D070	D060	D070	D060	D070
	13	D040	D050	D040	D050	D040	D050					D040	D050	D040	D050	D040	D050
	12	D020	D030	D020	D030	D020	D030					D020	D030	D020	D030	D020	D030
	11	D000	D010	D000	D010	D000	D010					D000	D010	D000	D010	D000	D010
	10	PPFO	MMFO	PPFO	MMFO	PPFO	MMFO	MA030	MA040	MA030	MA040	MA030	MA040	MA030	MA040	MA030	MA040
	09	ATN010	ATN030	ATN010	ATN030	ATN010	ATN030	MA020	SP5	MA020	SP5	MA020	SP5	MA020	SP5	MA020	SP5
	08	DSPLY1	ATN020	DSPLY1	ATN020	DSPLY1	ATN020	SP6	SP4	SP6	SP4	SP6	SP4	SP6	SP4	SP6	SP4
	07	MDSL020	MSIGO	MDSL020	MSIGO	MDSL020	MSIGO	MA010	SP3	MA010	SP3	MA010	SP3	MA010	SP3	MA010	SP3
	06	MDSL000	MDSL010	MDSL000	MDSL010	MDSL000	MDSL010	MA000	SP2	MA000	SP2	MA000	SP2	MA000	SP2	MA000	SP2
	05	FSL020	FSL030	FSL020	FSL030	FSL020	FSL030	PARO	SP1	PARO	SP1	PARO	SP1	PARO	SP1	PARO	SP1
	04	FSL000	FSL010	FSL000	FSL010	FSL000	FSL010	INHO	P5S	INHO	P5S	INHO	P5S	INHO	P5S	INHO	P5S
	03	STRTO	MFINO	STRTO	MFINO	STRTO	MFINO		P22		P22		P22		P22		P22
	02	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	SP7	SP8	SP7	SP8	SP7	SP8
	01	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
	00	P5	GND	P5	GND	P5	GND	P5	GND	P5	GND	P5	GND	P5	GND	P5	GND
		1	2	1	2	1	2	1	2	1	2	1	2	1	2	1	2

NOTES

NAME	TITLE	DATE	TITLE
K. LAFFERTY	DRAFT	10-19-71	MODEL 80 PROCESSOR
	CHK		
	ENGR		TASK NO. 03215
	DIR ENG		DWG NO. 01-053 D08

SHEET 2 OF 4

D & W REPROGRAPHICS 40058-4

INTERDATA

FRONT CONNECTOR MAP

MPC (½ BD)

ROW 2	PIN NO	ROW 1

TEST POINTS

MNEMONIC	NO.
AD0	1
PRN1	2
TMB1	3
PRFL1	4
XB1	5
GND	6

CONN 2

ROW 2	PIN NO	ROW 1
GND	12	WSB1
GND	11	WSD1
GND	10	WSA1
GND	09	WSC1
GND	08	MSK30
GND	07	MSK20
GND	06	MSK00
GND	05	MSK10
GND	04	BP020
GND	03	BP010
GND	02	BP000
WEBL0	01	WCLK0
PON0	00	PRFL0

MSU (1-4 UNITS)

CONNECTOR 3

ROW 2	PIN NO.	ROW 1
GND	24	DL160
	23	DL140
	22	DL150
	21	DL130
	20	DL120
	19	DL100
	18	DL110
	17	DL090
	16	DL080
	15	DL070
	14	DL060
	13	DL050
	12	DL040
	11	DL030
	10	DL020
	09	DL010
	08	DL000
	07	P5S
GND	06	SR0B
P15	05	P15
GND	04	P5
GND	03	P5
P24	02	P24
GND	01	P22
GND	00	P22

CONNECTOR 2

ROW 2	PIN NO.	ROW 1
GND	24	GND
AB020	23	AB031
AB130	22	AB061
AB070	21	AB051
AB040	20	AB081
AB110	19	AB101
AB090	18	AB121
STRB20	17	STRB30
STRB00	16	STRB10
AA021B	15	AA031B
STRA00	14	STRA10
STRA20	13	STRA30
AA050	12	AA101
AA070	11	AA041
AA060	10	AA081
AA090	09	AA131
AA110	08	AA121
ENDCYL0	07	MWRT0
GND	06	FAD0
	05	FECLK0
	04	P3
GND	03	GR1
	02	P22
P10	01	P10
P5S	00	P5S

MBC

CONNECTOR 4

ROW 2	PIN NO	ROW 1
GND	24	DL160
	23	DL140
	22	DL150
	21	DL130
	20	DL120
	19	DL100
	18	DL110
	17	DL090
	16	DL080
	15	DL070
	14	DL060
	13	DL050
	12	DL040
	11	DL030
	10	DL020
	09	DL010
	08	DL000
	07	P5S
GND	06	SR0B
P15	05	P15
GND	04	P5
GND	03	P5
P24	02	P24
GND	01	P22
GND	00	P22

CONNECTOR 3

ROW 2	PIN NO	ROW 1
GND	24	GND
AB020	23	AB031
AB130	22	AB061
AB070	21	AB051
AB040	20	AB081
AB110	19	AB101
AB090	18	AB121
STRB20	17	STRB30
STRB00	16	STRB10
AA021B	15	AA031B
STRA00	14	STRA10
STRA20	13	STRA30
AA050	12	AA101
AA070	11	AA041
AA060	10	AA081
AA090	09	AA131
AA110	08	AA121
ENDCYL0	07	MWRT0
GND	06	FAD0
	05	FECLK0
	04	P3
GND	03	GR1
	02	P22
P10	01	P10
P5S	00	P5S

CONN. 2

GND	12	WSB1
	11	WSD1
	10	WSA1
	09	WSC1
	08	MSK30
	07	MSK20
	06	MSK00
	05	MSK10
	04	BP020
	03	BP010
GND	02	BP000
WEBL0	01	WCLK0
PON0	00	PRFL0

IOU

TEST POINTS MNEMONIC
TMG1A
KTM
GSTRT1
DSTRT1
LDBR1
ADB1
ADA1

CONNECTOR 3

ROW 2	PIN NO	ROW 1
	24	
	23	
	22	
	21	
	20	
	19	
	18	
	17	
	16	
	15	
AC1	14	LB0
AC3	13	SRG0
X1	12	SD031
X2	11	SD021
X3	10	SD011
X4	09	SD001
SD071	08	X5
LC0	07	X6
SL00	06	SSGL1
SD061	05	POFF0
SD051	04	ESN00
LA0	03	ESNC0
SD041	02	WAIT1
LD0	01	INT0
SH10	00	

CONNECTOR 2

ROW 2	PIN NO	ROW 1
	00	
	01	
GND	02	TN
RN	03	TDU
TP	04	RP
	05	
	06	
	07	
	08	
	09	
	10	
	11	
	12	
	13	
	14	
	15	
	16	
	17	
	18	
	19	
	20	
	21	
	22	
	23	
	24	

(TEST SET)

CONNECTOR 18

GND	24	GND
GND	23	GND
ACLK0	22	ACNT021
ACNT011	21	ACNT001
ACNT031	20	EACNT1
RSA1	19	INHACK0
ASA1	18	ASB1
GFLG1	17	CFLG1
RSBY1	16	VFLG1
LFLG1	15	INHCLB0
LDRLR0	14	STRB0
ST151	13	ST141
ST131	12	ST121
ST111	11	ST101
ST091	10	ST081
ST071	09	ST061
ST051	08	ST041
ST031	07	ST021
ST011	06	ST001
CRLR120	05	CRLR130
CRLR140	04	CRLR150
CRLR080	03	CRLR090
CRLR100	02	CRLR040
CRLR110	01	CRLR050
CRLR060	00	CRLR070

CONNECTOR 17

ROW 1	PIN NO	ROW 2
GND	24	
	23	RAG151
	22	RAG141
	21	RAG131
	20	RAG121
	19	RAG111
	18	RAG081
	17	RAG091
	16	RAG101
	15	RAG071
	14	RAG061
	13	RAG051
	12	RAG041
	11	RD281
	10	RD301
	09	RD291
	08	RD311
	07	RD241
	06	RD261
	05	RD251
	04	RD271
	03	RD201
	02	RD221
	01	RD211
GND	00	RD231

CONNECTOR 16

ROW 1	PIN NO	ROW 2
GND	24	RD161
	23	RD171
	22	RD181
	21	RD191
	20	RD121
	19	RD131
	18	RD141
	17	RD151
	16	RD081
	15	RD091
	14	RD101
	13	RD111
	12	RD041
	11	RD051
	10	RD061
	09	RD071
	08	RD001
	07	RD011
	06	RD021
	05	RD031
	04	INHCLA0
	03	
	02	RMWP1
	01	STRB0A
GND	00	

ALU

CONNECTOR 2

ROW 1	PIN NO.	ROW 2
GND	24	GND
GND	23	GND
ACLK0	22	ACNT021
ACNT011	21	ACNT001
ACNT031	20	EACNT1
RSA1	19	INHACK0
ASA1	18	ASB1
GFLG1	17	CFLG1
RSBY1	16	VFLG1
LFLG1	15	INHCLB0
LDRLR0	14	STRB0
ST151	13	ST141
ST131	12	ST121
ST111	11	ST101
ST091	10	ST081
ST071	09	ST061
ST051	08	ST041
ST031	07	ST021
ST011	06	ST001
CRLR120	05	CRLR130
CRLR140	04	CRLR150
CRLR080	03	CRLR090
CRLR100	02	CRLR040
CRLR110	01	CRLR050
CRLR060	00	CRLR070

FEED THRU BETWEEN CPU - ALU

PIN NO	CONN C
106	BLCH140
105	BLCH120
104	BLCH150
103	BLCH130
102	PSW150
101	PSW140
100	PSW120
99	BLCH080
98	BLCH100
97	BLCH090
96	BLCH110
95	ALCH140
94	ALCH120
93	ALCH130
92	ALCH150
91	ALCH100
90	ALCH080
89	ALCH110
88	ALCH090
87	ALCH040
86	ALCH060
85	ALCH070
84	ALCH050
83	ALCH020
82	ALCH000
81	ALCH030
80	ALCH010
79	BLCH000
78	BLCH020
77	BLCH030
76	GND
75	BLCH010
74	BLCH040
73	BLCH060
72	BLCH070
71	BLCH050
70	CRLR120
69	CRLR130
68	CRLR140
67	CRLR150
66	CRLR080
65	CRLR090
64	CRLR100

PIN NO	CONN C
63	NOT AVAIL
62	CRLR040
61	CRLR110
60	CRLR050
59	CRLR060
58	CRLR070
57	RAG151
56	RAG141
55	RAG131
54	RAG121
53	RAG111
52	RAG081
51	RAG091
50	RAG101
49	RA071
48	RAG061
47	RAG051
46	RAG041
45	RD161
44	RD171
43	RD181
42	RD191
41	RD121
40	RD131
39	RD141
38	RD151
37	RD081
36	RD091
35	RD101
34	RD111
33	RD041
32	RD051
31	RD061
30	RD071
29	RD001
28	RD011
27	RD021
26	RD031
25	GND
24	RD281
23	RD291
22	RD301
21	RD311
20	RD241
19	RD251
18	RD261
17	RD271
16	RD201
15	RD211
14	RD221
13	RD231
12	GND
11	STRB0
10	LDRLR0
09	INHCLB0
08	NOT USED
07	NOT USED
06	RS001
05	GND
04	GND
03	GND
02	GND
01	GND
00	NOT USED

PIN NO	CONN D
48	ST151
47	ST141
46	ST121
45	ST001
44	ST011
43	ST101
42	ST111
41	NOT USED
40	ST131
39	ST081
38	ST061
37	ST071
36	ST091
35	ST041
34	ST021
33	ST031
32	GND
31	ST051
30	RGL0
29	RGH0

PIN NO	CONN D
28	BSEL001
27	ASEL001
26	ASEL000
25	SSEL040
24	BSEL040
23	ASEL040
22	SSEL001
21	SSEL030
20	BSEL030
19	ASEL030
18	SSEL020
17	BSEL030
16	ASEL020
15	SSEL010
14	BSEL010
13	ASEL010
12	BSEL000
11	VFLG1
10	CFLG1
09	[illegible]FLG1
08	LFLG1
07	GFLG1
06	RSAY1
05	GND
04	NOT USED
03	SSEL000
02	RSBY1
01	REGWRT0

CONNECTOR F

ROW 2	PIN NO	ROW 1
	41	
	40	
	39	
	38	
	37	
	36	
	35	
	34	
	33	
	32	
	31	
	30	
	29	
	28	
	27	
	26	
	25	
	24	
	23	
	22	
	21	
	20	
CWRT0	19	CRDY0
A150	18	A140
A130	17	A120
A110	16	A100
A090	15	A080
A070	14	A060
A050	13	A040
A030	12	A020
A010	11	A000
S150	10	S140
S130	09	S120
S110	08	S100
S090	07	S080
S070	06	S060
S050	05	S040
S030	04	S020
S010	03	S000
ZCC1	02	GCC1
	01	
	00	

ROW 2	PIN NO	ROW 1
	41	
	40	
SCC0	39	
CCC1	38	
VCC1	37	
	36	
B150	35	B140
B130	34	B120
B110	33	B100
B090	32	B080
B070	31	B060
B050	30	B040
B030	29	B020
B010	28	B000
	27	KS160
	26	
	25	
	24	
	23	
	22	
	21	
	20	
	19	
	18	
	17	
	16	
	15	
	14	
	13	
	12	
	11	
	10	
	09	
	08	
MSIG0	07	MDSL020
MDSL010	06	MDSL000
FSEL030	05	FSEL020
FSEL010	04	FSEL000
MFIN0	03	STRT0

CONN E

CPU

CONNECTOR 3

ROW 2	PIN NO	ROW 1
GND	24	
	23	RAG151
	22	RAG141
	21	RAG131
	20	RAG121
	19	RAG111
	18	RAG081
	17	RAG091
	16	RAG101
	15	RAG071
	14	RAG061
	13	RAG051
	12	RAG041
	11	RD281
	10	RD301
	09	RD291
	08	RD311
	07	RD241
	06	RD261
	05	RD251
	04	RD271
	03	RD201
	02	RD221
	01	RD211
GND	00	RD231

CONNECTOR 2

ROW 2	PIN NO	ROW 1
GND	24	RD161
	23	RD171
	22	RD181
	21	RD191
	20	RD121
	19	RD131
	18	RD141
	17	RD151
	16	RD081
	15	RD091
	14	RD101
	13	RD111
	12	RD041
	11	RD051
	10	RD061
	09	RD071
	08	RD001
	07	RD011
	06	RD021
	05	RD031
	04	INHCLA0
	03	
	02	RMWP1
	01	STRB0A
GND	00	

DCS (EXPANSION)

CONNECTOR 3

ROW 2	PIN NO	ROW 1
GND	24	
	23	RAG151
	22	RAG141
	21	RAG131
	20	RAG121
	19	RAG111
	18	RAG081
	17	RAG091
	16	RAG101
	15	RAG071
	14	RAG061
	13	RAG051
	12	RAG041
	11	RD281
	10	RD301
	09	RD291
	08	RD311
	07	RD241
	06	RD261
	05	RD251
	04	RD271
	03	RD201
	02	RD221
	01	RD211
GND	00	RD231

CONNECTOR 2

ROW 2	PIN NO	ROW 1
GND	24	RD161
	23	RD171
	22	RD181
	21	RD191
	20	RD121
	19	RD131
	18	RD141
	17	RD151
	16	RD081
	15	RD091
	14	RD101
	13	RD111
	12	RD041
	11	RD051
	10	RD061
	09	RD071
	08	RD001
	07	RD011
	06	RD021
	05	RD031
	04	INHCLA0
	03	
	02	RMWP1
	01	STRB0A
GND	00	

NOTES

NAME	TITLE	DATE
R. MEGINLEY	DRAFT	8-7-72
	CHK	
	ENGR	
	DIR ENG	

TITLE MODEL 80 PROCESSOR

TASK NO. 03215

DWG NO. 01-053 008

SHEET OF 3 - 4

BRUNING 44-231 16042

INTERDATA®

	SCHEMATIC LOCATION				
	35-403 D08	35-404 D08	35-405 D08	35-407 D08	02-247 D08
MNEMONIC	CPU	ALU	IOU	MBC	MSU
A000	5N6	1D6	3A6		
A010	5N6	1E6	3B6		
A020	5N6	1G6	3E6		
A030	5N6	1F6	3E6		
A040	5N5	1K6	3G6		
A050	5N5	1L6	3H6		
A060	5N5	1N6	3L6		
A070	5N5	1M6	3M6		
A080	5N5	2D6	3B1		
A090	5N5	2E6	3C1		
A100	5N5	2G6	3E1		
A110	5N4	2F6	3G1		
A120	5N4	2K6	3J1		
A130	5N4	2L6	3K1		
A140	5N4	2N6	3M1		
A150	5N4	2M6	3N1		
AA021B				7F5	6A8
AA031B				7F6	6A7
AA041				7F7	2A5
AA050				7F8	2A5
AA060				7F9	2A6
AA070				8M2	2A6
AA081				8M3	2A7
AA090				9G2	2A7
AA101				9G4	2A8
AA110				9G6	2A8
AA121				9G7	2A9
AA131				9J9	2A9
AB020				7F4	6B9
AB031				7F5	6B9
AB040				7F6	2G5
AB051				7F8	2G5
AB061				7F9	2G6
AB070				8M1	2G6
AB081				8M3	2G7
AB090				9G2	2G7
AB101				9G3	2G8
AB110				9G5	2G8
AB121				9G7	2G9
AB130				9G9	2G9
AC1			6A2		
AC3			6A2		
ACLKO		8R1			
ACNT001		8D4			
ACNT011		8D4			
ACNT021		8D4			
ACNT031		8E4			
ACKO			5R7		
ADA1			7K6		
ADB1			7K7		
ADRSO			5R6		
ALCH000	6K5	1E7			
ALCH010	6K5	1E7			
ALCH020	6H5	1G7			
ALCH030	6G5	1H7			
ALCH040	6E5	1L7			
ALCH050	6D5	1L7			
ALCH060	6B5	1N7			
ALCH070	6A5	1R7			
ALCH080	6K9	2E7			
ALCH090	6J9	2E7			
ALCH100	6G9	2G7			
ALCH110	6G9	2H7			
ALCH120	6D9	2L7			
ALCH130	6D9	2L7			
ALCH140	6B9	2N7			
ALCH150	6A9	2N7			
ASA1		6R5			
ASB1		6R5			
ASEL001	5M9	8C5			
ASEL000	5M9	8A5			
ASEL010	5L9	8C5			
ASEL020	5K9	8J5			
ASEL030	5J9	8J5			
ASEL040	5H9	8K5			
ATN000	3F2		8R7		
ATN010	3F3				
ATN020	3F3				
ATN030	3F3				

	SCHEMATIC LOCATION				
	35-403 D08	35-404 D08	35-405 D08	35-407 D08	02-247 D08
MNEMONIC	CPU	ALU	IOU	MBC	MSU
B000	4N1	3A6	3A1		
B010	4N1	3B6	3B1		
B020	4N1	3D6	3D1		
B030	4R1	3C6	3F1		
B040	4M1	3E6	3H1		
B050	4L1	3F6	3J1		
B060	4K1	3H6	3L1		
B070	4J1	3G6	3N1		
B080	4H1	3K6	3B1		
B090	4G1	3K6	3C1		
B100	4F1	3M6	3E1		
B110	4D1	3M6	3F1		
B120	4C1	4A6	3H1		
B130	4B1	4B6	3K1		
B140	4A1	4D6	3M1		
B150	4M1	4C6	3N1		
BLCH000	6M5	3A9			
BLCH010	6L5	3B9			
BLCH020	6J5	3C9			
BLCH030	6H5	3D9			
BLCH040	6F5	3E9			
BLCH050	6F5	3F9			
BLCH060	6D5	3G9			
BLCH070	6C5	3H9			
BLCH080	6M9	3J9			
BLCH090	6L9	3K9			
BLCH100	6J9	3L9			
BLCH110	6H9	3M9			
BLCH120	6F9	4A9			
BLCH130	6E9	4B9			
BLCH140	6C9	4C9			
BLCH150	6B9	4D9			
BP000				8A9	
BP010				8A8	
BP020				8A8	
BSEL001	5F9	8F5			
BSEL000	5F9	8D5			
BSEL010	5E9	8F5			
BSEL020	5D9	8J5			
BSEL030	5C9	8K5			
BSEL040	5A9	8L5			
CA000	9F9			7A1	
CA010	9F9			7A7	
CA020	9H9			7A4	
CA030	9H9			7A5	
CA040	9H9			7A6	
CA050	9J9			7A8	
CA060	9K9			7A9	
CA070	9K9			8F1	
CA080	9L9			8F3	
CA090	9L9			9A1	
CA100	9M9			9A3	
CA110	9N9			9A5	
CA120	9N9			9A6	
CA130	9N9			9A8	
CA140	9D9			3A4	
CA150	9E9		1F1		
CATN			—		
CB000				3A1	
CB010				3A2	
CB020				3A3	
CCC1	7D1	6B1	5R4		
CD001	8B1			5A2	
CD011	8C1			5A4	
CD021	8D1			5A6	
CD031	8D1			5A8	
CD041	8F1			5J2	
CD051	8F1			5J4	
CD061	8G1			5J6	
CD071	8G1			5J8	
CD081	8J1			6A2	
CD091	8J1			6A4	
CD101	8K1			6A6	
CD111	8K1			6A8	
CD121	8M1			6J2	
CD131	8M1			6J4	
CD141	8N1			6J6	
CD151	8N1			6J8	

	SCHEMATIC LOCATION				
	35-403 D08	35-404 D08	35-405 D08	35-407 D08	02-247 D08
MNEMONIC	CPU	ALU	IOU	MBC	MSU
CFLG1	3A9	6B9			
CFTCHO	1R4			2A2	
CLO70			6N3		
CMDO			5R8		
CRDYO	1K3			3R4	
CREQO	1R7			3A3	
CRLR040	4N6	4N5			
CRLR050	4N6	4M5			
CRLR060	4L6	4M6			
CRLR070	4K6	4M6			
CRLR080	4J6	4M6			
CRLR090	4H6	4M6			
CRLR100	4G6	4M6			
CRLR110	4F6	4N6			
CRLR120	4E6	4M7			
CRLR130	4C6	4M7			
CRLR140	4B6	4M7			
CRLR150	4A6	4M7			
CWRTO	1R8			8F8	
D000			4B5		
D010			4C5		
D020			4C5		
D030			4D5		
D040			4H5		
D050			4J5		
D060			4K5		
D070			4L5		
D080			4E5		
D090			4F5		
D100			4F5		
D110			4G5		
D120			4M5		
D130			4M5		
D140			4N5		
D150			4R5		
DAO			5R8		
DACKO			5R7		
DCRO			1H1		
DL000				5H1	3H9
DL010				5H3	3H9
DL020				5H5	3H4
DL030				5H8	3H4
DL040				5S3	
DL050				5S5	
DL060				5S7	
DL070				5S9	
DL080				6H1	
DL090				6H3	
DL100				6H5	
DL110				6H8	
DL120				6S3	
DL130				6S5	
DL140				6S7	
DL150				6S9	
DL160				9R5	
DPFO			5D3	2A5	
DRO			5R6		
DSPLY1			8F5		
DSTRT1			2B6		
EACNT1		8G2			
ENDCYLO				2A2	6R2
ENO				2A9	
ESNOO			8A4		
ESNCO			8A3		
FADO				3K8	6A2
FECLKO				3A9	6M5
FSEL000	10R4	6C1	1M1		
FSEL010	10R4	5E1	1L1		
FSEL020	10N4	6J7	1L1		
FSEL030	10N4	5F1	1K1		
GCC1	7B1	6B1	5R3		
GFLG1	3A7	6B9			
GR1				4R6	6A1
GSTRT1			1N4		

	SCHEMATIC LOCATION				
	35-403 D08	35-404 D08	35-405 D08	35-407 D08	02-247 D08
MNEMONIC	CPU	ALU	IOU	MBC	MSU
HWO			2H2		
IAO			5D4	3N2	
INHO				3N5	
INHACKO		7L1			
INHCLAO	1G3				
INHCLBO	1G3	4M7			
INITO			6A1		
IPFO			5D2	3R7	
JRLR1	—				
KTM			6A8		
KSIGO	10M9	6K7	1J1		
LAO			8F7		
LBO			8F8		
LCO			8F8		
LCC1	7A1	6A1	5R2		
LDO			8F7		
LDBR1			9C5		
LDRLRO	2A5	4N8			
LFLG1	3A7	6B9			
MA000				7A1	
MA010				7A3	
MA020				7A4	
MA030				7A5	
MA040				7A7	
MA050				7A8	
MA060				7A9	
MA070				8F2	
MA080				8F3	
MA090				9A2	
MA100				9A3	
MA110				9A5	
MA120				9A7	
MA130				9A8	
MA140				9A7	
MB000				2A3	
MB010				2A3	
MB020				2A4	
MDSL000	10L4	7N1	1N1		
MDSL010	10L4	7N1	1N1		
MDSL020	10M4	7N1	1N1		
MEINO	1D2	7N9	1H9		
MMFO	3F4		5H3		
MSD000				5A1	
MSD010				5A3	
MSD020				5A5	
MSD030				5A8	
MSD040				5J1	
MSD050				5J3	
MSD060				5J5	
MSD070				5J7	
MSD080				6A1	
MSD090				6A3	
MSD100				6A5	
MSD110				6A8	
MSD120				6J1	
MSD130				6J3	
MSD140				6J5	
MSD150				6J8	
MSIGO	2A6	7N9	1H9		
MSK000				8A5	
MSK010				8A5	
MSK020				8A6	
MSK030				8A6	
MWRTOA				8R7	6G1
PARO					
POFFO			6A1		
PONO				8F7	
PPFO	3L5		6N5		
PRFLO				8R9	
PSW120	7D9	5D1			
PSW140	7B9	6G7			
PSW150	7A9	6G7			
PVMDO	3M1			8F7	

	SCHEMATIC LOCATION				
	35-403 D08	35-404 D08	35-405 D08	35-407 D08	02-247 D08
MNEMONIC	CPU	ALU	IOU	MBC	MSU
RACKO			8K6		
RAG041	4N5	9A1			
RAG051	4M5	9A2			
RAG061	4L5	9A3			
RAG071	4K5	9A3			
RAG081	4J5	9A3			
RAG091	4H5	9A4			
RAG101	4G5	9A4			
RAG111	4E5	9A5			
RAG121	4D5	9A5			
RAG131	4C5	9A6			
RAG141	4B5	9A6			
RAG151	4A5	9A7			
RD001	2E1	3A7			
RD011	2F1	3B7			
RD021	2G1	3C7			
RD031	2H1	3D7			
RD041	2J1	3F7			
RD051	2K1	3G7			
RD061	2L1	3G7			
RD071	2M1	3H7			
RD081	2N1	3K7			
RD091	2R1	3L7			
RD101	2E5	3M7			
RD111	2F5	3N7			
RD121	2G5	4A7			
RD131	2H5	4B7			
RD141	2J5	4C7			
RD151	2K5	4D7			
RD161	2L5	3A7			
RD171	2M5	3B7			
RD181	2N5	3C7			
RD191	2R5	3D7			
RD201	2C7	3E7			
RD211	2D7	3F7			
RD221	2E7	3G7			
RD231	2F7	3H7			
RD241	2G7	3K7			
RD251	2H7	3L7			
RD261	2J7	3L7			
RD271	2K7	3M7			
RD281	2L7	3A7			
RD291	2M7	4B7			
RD301	2N7	4C7			
RD311	2R7	4D7			
REGWRTO	1F5	8H5			
RGHO	4M3	3A7			
RGLO	4M3	3H7			
RMWP1	1F8				
RN			9N8		
RP			9N8		
RSA1		8A6			
RSAY1	1H5	8B5			
RSBY1	1J8	4M8			
RS001	1E8	8A5			
S000	4N9	5E6	3C9		
S010	4N9	5F6	3D9		
S020	4N9	5F6	3F9		
S030	4R9	5G6	3G9		
S040	4N9	5G6	3J9		
S050	4M9	5H6	3K9		
S060	4L9	5H6	3N9		
S070	4K9	5J6	3R9		
S080	4J9	5J6	3A9		
S090	4H9	5K6	3B9		
S100	4G9	5K6	3D9		
S110	4E9	5L6	3E9		
S120	4D9	5M6	3H9		
S130	4C9	5M6	3J9		
S140	4B9	5N6	3L9		
S150	4A9	5N6	3M9		
SCCO	7E6	7N9	5R1		
SCLRO	1J9		6A6	8K5	

	SCHEMATIC LOCATION				
	35-403 D08	35-404 D08	35-405 D08	35-407 D08	02-247 D08
MNEMONIC	CPU	ALU	IOU	MBC	MSU
SD001			7G1		
SD011			7G2		
SD021			7G2		
SD031			7G2		
SD041			7G3		
SD051			7G3		
SD061			7G4		
SD071			7G5		
SHIO			8F6		
SLOO			8F6		
SRO			5R7		
SROB				2N2	6B8
SRGO			7D6		
SSEL001	10H9	8C5			
SSEL000	10H9	8A5			
SSEL010	10F9	8H5			
SSEL020	10E9	8J5			
SSEL030	10C9	8K5			
SSEL040	10A9	8L5			
SSGL1			8A5		
ST001	9F1	5E9			
ST011	9F1	5F9			
ST021	9H1	5F9			
ST031	9H1	5G9			
ST041	9H1	5G9			
ST051	9J1	5H9			
ST061	9K1	5H9			
ST071	9K1	5J9			
ST081	9L1	5K9			
ST091	9L1	5K9			
ST101	9M1	5L9			
ST111	9N1	5L9			
ST121	9N1	5M9			
ST131	9N1	5M9			
ST141	9E1	5N9			
ST151	9E1	5N9			
STRA00				7G2	6A5
STRA10				7G3	6A5
STRA20				7G3	6A5
STRA30				7G3	6A5
STRBO	1K2	8R1			
STRBOA	1N1				
STRB00				7G1	6A6
STRB10				7G1	6A6
STRB20				7G2	6A6
STRB30				7G2	6A6
STRTO	10H4	5F1	1R1		
SYNO			2A7		
TACKO			8R6		
TDU			9N7		
TMG1A			8M1		
TN			9N6		
TP			9N5		
VCC1	7C1	6G9	5R4		
VFLG1	3A9	6H9			
WAIT1			8F6		
WCLKO				8A7	
WEBLO				8A9	
WRTOA				8F9	
WSA1				8A3	
WSB1				8A3	
WSC1				8A4	
WSD1				8A4	
X1			6N4		
X2			6N4		
X3			6N4		
X4			6N4		
X5			6N5		
X6			6N5		
ZFLG1	3A6	6B9			

CONNECTOR MNEMONIC INDEX

NOTES

NAME	TITLE	DATE
J.F.FLEMING	DRAFT	1-26-73
	CHK	
	ENGR	
	DIR ENG	

TITLE MODEL 80 PROCESSOR

TASK NO. 03215

DWG NO. 01-053 D08

SHEET 4 OF 4

NOTES:

1. WHEN POWERING TWO CHASSIS FROM ONE POWER SUPPLY USE JUMPER #17-182 4 REQ'D & FAN JUMPER #17-181 1 REQ'D PER DETAIL A
2. WHEN CONNECTING TWO 34-012 POWER SUPPLIES IN PARALLEL USE JUMPER 17-182 PER DETAIL B.
3. ADJACENT CHASSIS MUST USE GROUND JUMPERS #17-076 F00 AS STATED BELOW
   a. ADJACENT 15 IN. CHASSIS TO USE 4 JUMPERS
   b. CHASSIS ADJACENT TO 10 IN CHASSIS TO USE 3 JUMPERS.

[illegible]

DELETED RETAINING BAR 14-309 A02

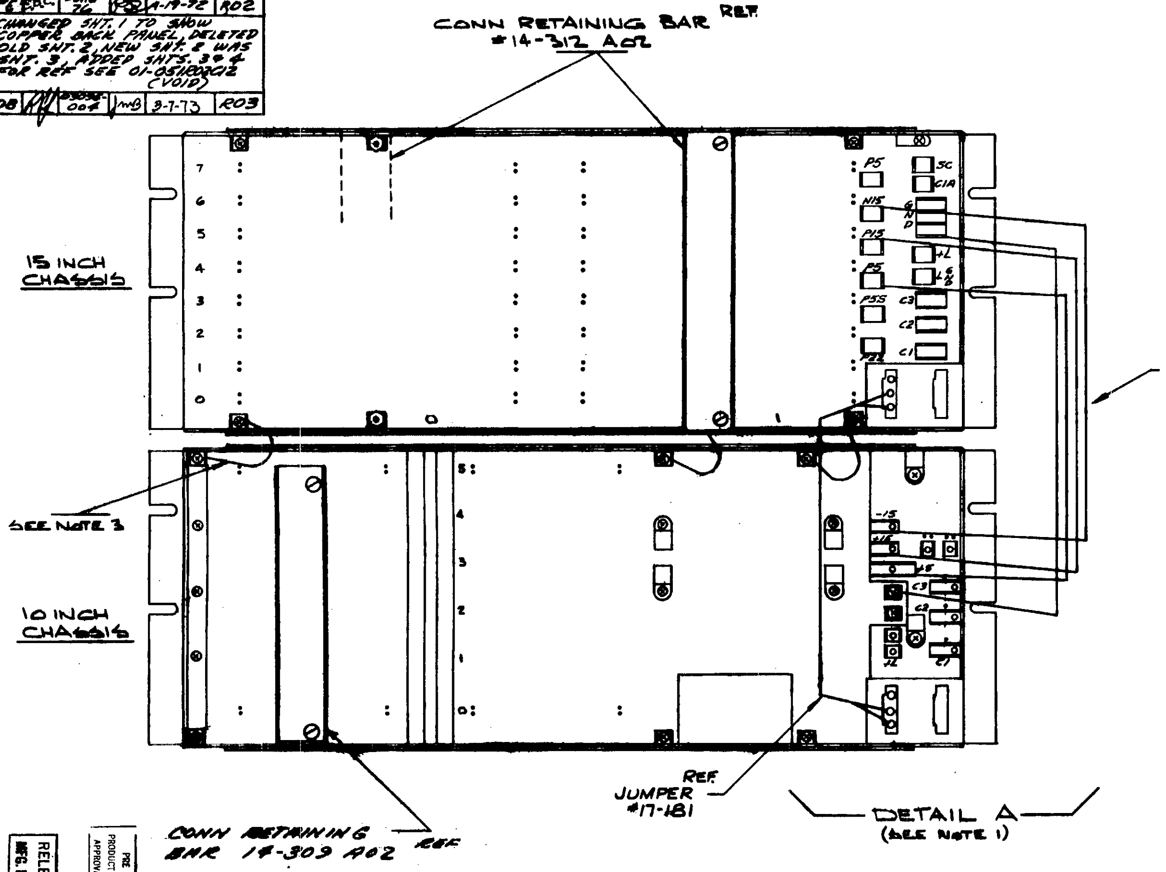
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	R01

NOTE 2 READ WHEN CONNECTING POWER SUPPLIES IN PARALLEL USE JUMPER 17-182 PER DETAIL B
SHT. 3 WAS NOT SPECIFIED

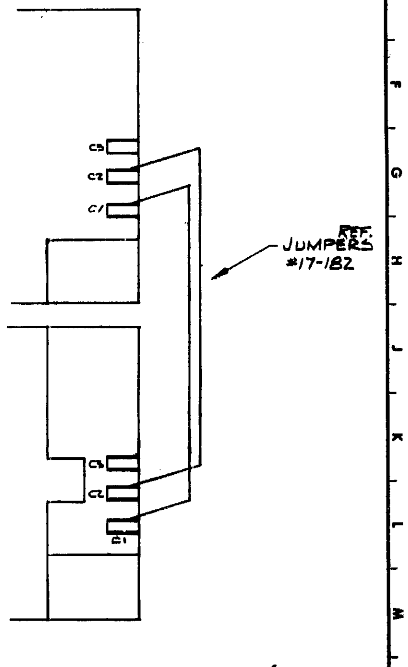
PG	E.R.C.	53118-76	RB	4-19-72	R02

CHANGED SHT. 1 TO SHOW COPPER BACK PANEL, DELETED OLD SHT. 2, NEW SHT. 2 WAS SHT. 3, ADDED SHTS. 3 & 4 FOR REF SEE 01-051R03C12 (VOID)

DB		53038-004	JMB	3-7-73	R03


CONN RETAINING BAR REF
#14-312 A02
15 INCH CHASSIS
7
6
5
4
3
2
1
0
P5
5C
C1A
N15
G N D
P15
+L
G N D
P5
P5S
C3
C2
C1
P22
JUMPERS REF.
#17-182
SEE NOTE 3
10 INCH CHASSIS
-15
+15
+5
C3
C2
+L
C1
JUMPER REF
#17-181
CONN RETAINING BAR 14-309 A02 REF

DETAIL A
(SEE NOTE 1)


C3
C2
C1
JUMPERS REF.
#17-182
C3
C2
C1

DETAIL B
(SEE NOTE 2)

REAR VIEW

NAME	TITLE	DATE
G. Welly	M.E.	21 Jan 72
G. WELLY	CHECK	
G. WELLY	ENGR	
M FUCHS	Q C	
R E JONES	MFG ENG	

TITLE CABLE INFORMATION H S

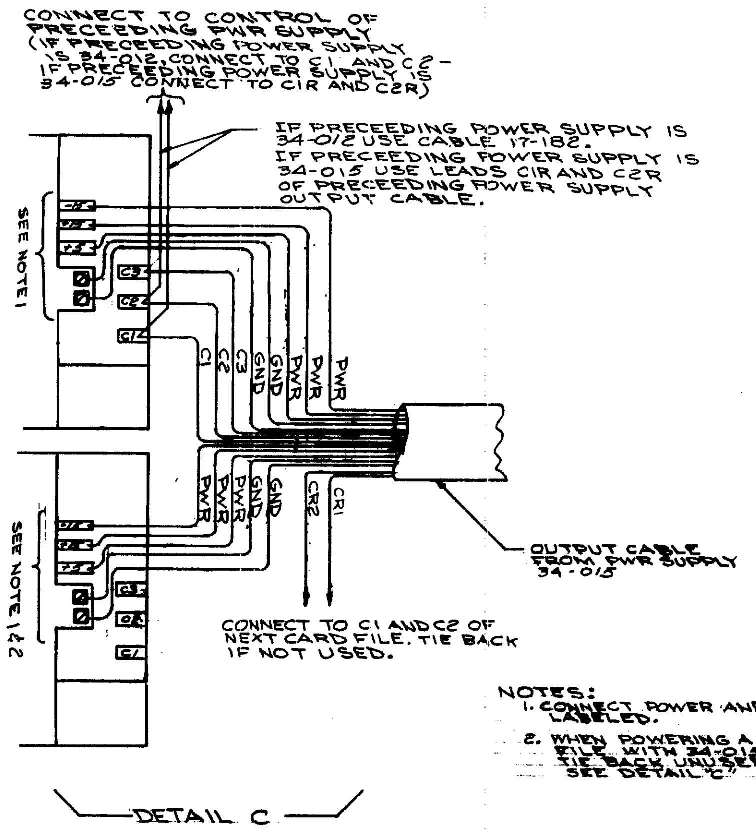
TASK NO. D3116

DWG. NO. 01-05[illegible]

SHEET 1 OF 4

PRE PRODUCT. APPROVAL

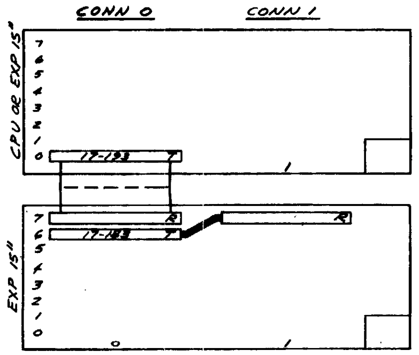
RELEASED FOR PRODUCTION
MFG. ENG. ______ DATE ______


CONNECT TO CONTROL OF PRECEEDING PWR SUPPLY (IF PRECEEDING POWER SUPPLY IS 34-012, CONNECT TO C1 AND C2 - IF PRECEEDING POWER SUPPLY IS 34-015 CONNECT TO C1R AND C2R)
IF PRECEEDING POWER SUPPLY IS 34-012 USE CABLE 17-182.
IF PRECEEDING POWER SUPPLY IS 34-015 USE LEADS C1R AND C2R OF PRECEEDING POWER SUPPLY OUTPUT CABLE.
SEE NOTE 1
C3
C2
C1
PWR
PWR
GND
GND
C3
C2
C1
PWR
PWR
PWR
GND
GND
CR2
CR1
OUTPUT CABLE FROM PWR SUPPLY 34-015
SEE NOTE 1 & 2
CONNECT TO C1 AND C2 OF NEXT CARD FILE. TIE BACK IF NOT USED.
DETAIL C

NOTES:
1. CONNECT POWER AND GROUND AS LABELED.
2. WHEN POWERING A SINGLE CARD FILE WITH 34-015 POWER SUPPLY TIE BACK UNUSED CABLES. SEE DETAIL "C"

TITLE
CABLE
INFORMATION
NS

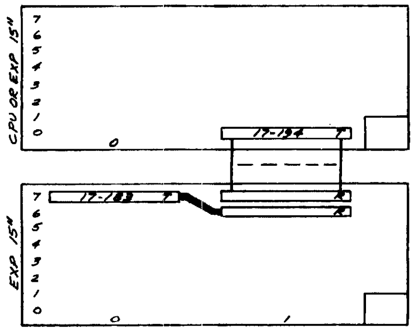
TASK NO. 03116
DWG NO. 01-051R03C12
SHEET 2 OF 4


CONN 0
CONN 1
CPU OR EXP 15"
EXP 15"
17-193
17-183
F
R
7
6
5
4
3
2
1
0

CABLE : 17-183 & 17-193

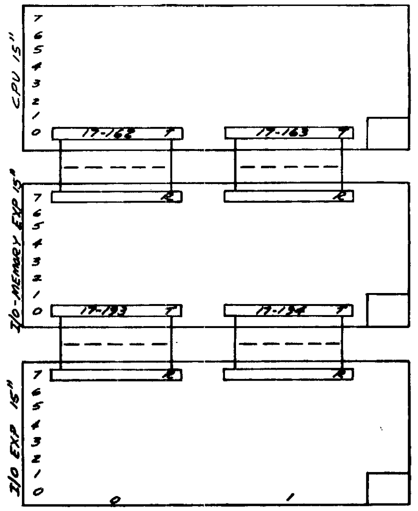
17-183 CABLE IS USED TO CONNECT CONN 0, AND CONN 1 OF THE SAME CHASSIS, IN ORDER TO REGENERATE EITHER THE MUX BUS OR THE BUFFERED OR SELCH BUS. IT USES TWISTED PAIR AND CONTAINS ONLY THE I/O BUS. IT DOES NOT HAVE RACKO/TACKO INCORPORATED.

USED ON:
MOD 80 CPU CHASSIS
UNIVERSAL EXPAN. CHASSIS


CPU OR EXP 15"
EXP 15"
17-194
17-183
F
R
7
6
5
4
3
2
1
0

CABLE : 17-183 & 17-194

THIS IS A TYPICAL CONFIGURATION USING A 17-183 & 17194 TO MAKE BOTH CONNECTORS OF A SINGLE CHASSIS THE SAME I/O BUS. THIS CONFIGURATION IS VALID ON THE MOD 80 ONLY IF THE CPU CHASSIS CONTAINS A BUS BUFFER OR SELCH.


CPU 15"
I/O-MEMORY EXP 15"
I/O EXP 15"
17-162
17-163
17-193
17-194
F
R
7
6
5
4
3
2
1
0

CABLE : 17-162 & 17-163

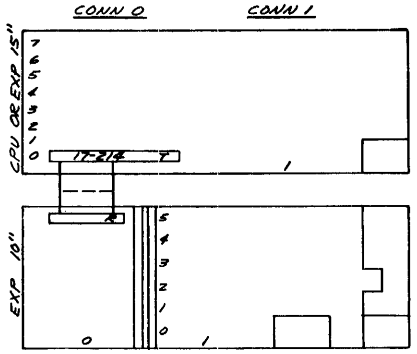
THESE CABLES ARE USED TO BRING THE I/O BUS AND MEM BUS TO THE ADJACENT CHASSIS. THEY USE TWISTED PAIR AND ARE NOT BUNDLED. THEY CAN ONLY BE USED TO CONNECT THE CPU CHASSIS TO THE FIRST EXPANSION CHASSIS. MUST BE USED INCONJUNCTION WITH 17-183 ON MOD 80.

USED ON:
MOD 70
MOD 74
MOD 80
UNIVERSAL EXPAN.

CABLE : 17-193 & 17-194

THESE CABLES ARE USED TO CONNECT THE I/O BUS ONLY TO THE ADJACENT 15" EXPANSION CHASSIS. THE 17-193 CABLE IS USED ON CONN 0 AND THE 17-194 HANDLES CONN 1. THEY USE TWISTED PAIR AND ARE NOT BUNDLED.

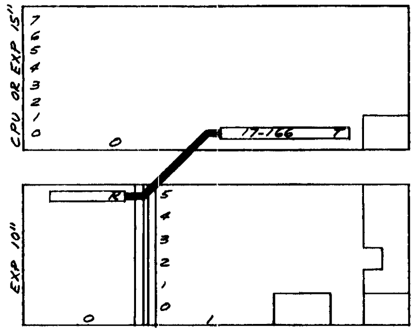
USED ON:
MOD 70
MOD 74
MOD 80
UNIVERSAL EXPAN.


CONN 0
CONN 1
CPU OR EXP 15"
EXP 10"
17-214
F
7
6
5
4
3
2
1
0

CABLE : 17-214

THIS CABLE IS USED TO CONNECT THE I/O BUS AS IT APPEARS ON CONN 0 TO AN ADJACENT 10" EXPAN CHASSIS. IT IS TWISTED PAIR AND IS NOT BUNDLED. THIS CABLE CONTAINS THE I/O BUS ONLY. D BUS BITS, D080-D150 ARE THE ONLY ONE'S CARRIED THRU WITH THIS CABLE. (BITS D000-D070 ARE TERMINATED ON THE 15" CONNECTOR END)

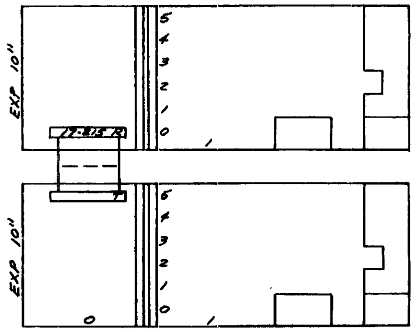
USED ON:
MOD 70
MOD 74
MOD 80
UNIVERSAL EXPAN. CHASSIS
10" EXPAN. CHASSIS


CPU OR EXP 15"
EXP 10"
17-166
F
R
7
6
5
4
3
2
1
0

CABLE : 17-166

THIS CABLE CONTAINS THE I/O BUS, D BUS BITS 8-15, ONLY. IT IS USED TO CONNECT A BUS BUFFER, OR SELCH TO A 10" EXPAN. CHASSIS. THE LENGTH OF THIS CABLE IS 36" WITH DATA LINES AND CONTROL LINES BUNDLED SEPERATELY. DUE TO IT'S LENGTH IT MUST BE DRIVEN BY A BUS BUFFER OR SELCH.

USED ON:
MOD 70
MOD 74
MOD 80
UNIVERSAL EXPAN.
10" EXPAN.


EXP 10"
EXP 10"
17-215
R
5
4
3
2
1
0

CABLE : 17-215

THIS CABLE IS USED TO CONNECT TWO ADJACENT 10" EXPAN. CHASSIS. IT CONTAINS BITS D080-D150 OF THE I/O BUS ONLY. IT IS TWISTED PAIR AND NOT BUNDLED.

USED ON:
10" EXPAN. ONLY

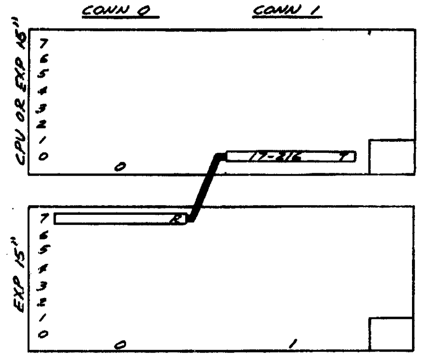
NOTES

NAME

TITLE

DATE

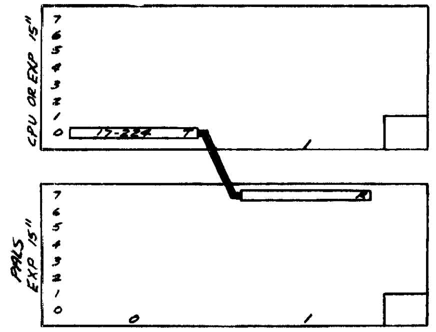
TITLE CABLE INFORMATION N/S
TASK NO. 03095
DWG. NO. 01-051R03 C12
SHEET 3 OF 4


CONN 0
CONN 1
CPU OR EXP 15"
EXP 15"
7
6
5
4
3
2
1
0
17-216
0
1

CABLE: 17-216

THIS CABLE IS USED TO CONNECT THE I/O BUS ONLY FROM A 15" CHASSIS TO A 15" CHASSIS. IT MUST BE DRIVEN BY A SELCH OR BUS BUFFER. THIS CABLE IS 36" LONG AND USES TWISTED PAIR WITH THE DATA LINES AND THE CONTROL LINES BUNDLED SEPERATELY

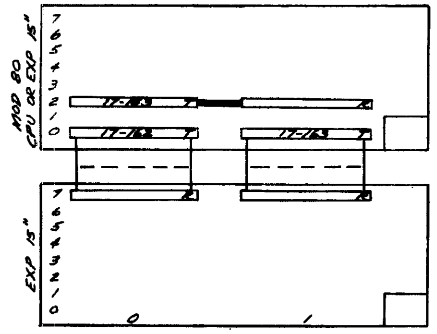
USED ON:
- MOD 70
- MOD 74
- MOD 80
- 15" EXPAN.


CPU OR EXP 15"
PALS EXP 15"
7
6
5
4
3
2
1
0
17-224
0
1

CABLE: 17-224

THIS CABLE IS THE SAME AS THE 17-183 EXCEPT FOR THE ADDITION OF RACKO/TACKO. ITS PRIMARY USE IS WITH THE PALS CHASSIS. IT CONTAINS THE I/O BUS COMPLETE WITH RACKO/TACKO ONLY.

USED ON:
- MOD 70
- MOD 74
- MOD 80
- PALS EXPAN. CHASSIS


MOD 80 CPU OR EXP 15"
EXP 15"
7
6
5
4
3
2
1
0
17-183
17-162
17-163
0
1

CABLE: 17-162, 17-163, 17-183

THIS EXAMPLE SHOWS THE TYPICAL CONFIGURATION OF THE MOD 80. THE 17-183 CABLE IS INSTALLED ON SLOT 2 CONN 0 TO CONN 1 IN THE STANDARD CPU CHASSIS. IF A SELECTOR CHANNEL OR BUS BUFFER IS INSTALLED IN THE CPU CHASSIS THE 17-183 CABLE MUST BE REMOVED.

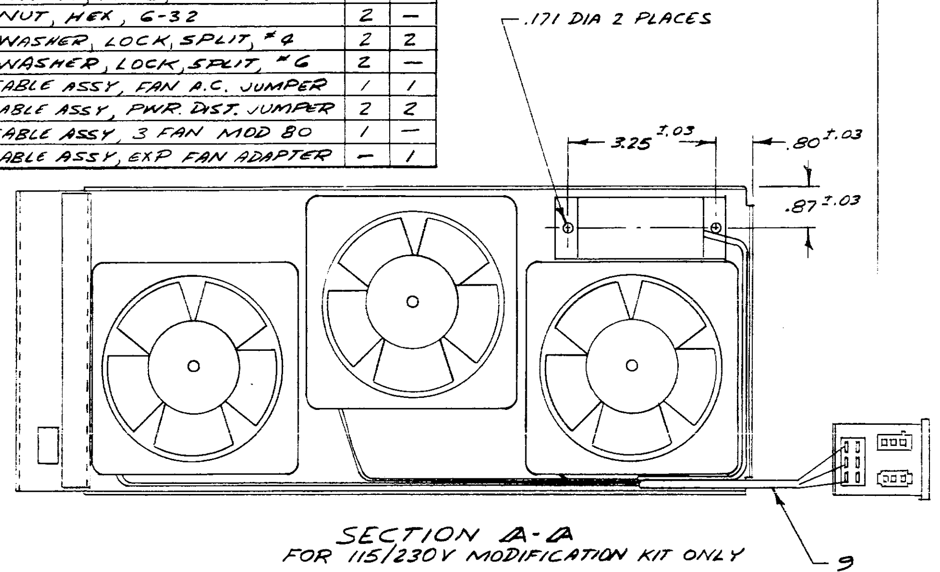
NOTE
NAME
TITLE
DATE
TITLE CABLE INFORMATION N/S
TASK NO. 03095
DWG NO. 01-051R03 C/12
SHEET 4 OF 4

INTERDATA

REFERENCE PARTS LIST

ITEM NO.	PART NO.	DESCRIPTION	QTY. F01	QTY. F02
1	35-526	P.C. BD. ASSY, TA-TB	1	1
2	16-236 F04	SCREW, PHPS, 4-40 × ½	2	2
3	16-237 F03	SCREW, PHPS, 6-32 × 3/8	2	—
4	16-058 F02	NUT, HEX, 6-32	2	—
5	16-059 F01	WASHER, LOCK, SPLIT, #4	2	2
6	16-059 F02	WASHER, LOCK, SPLIT, #6	2	—
7	17-181	CABLE ASSY, FAN A.C. JUMPER	1	1
8	17-182	CABLE ASSY, PWR. DIST. JUMPER	2	2
9	17-202 F01M01	CABLE ASSY, 3 FAN MOD 80	1	—
10	17-307	CABLE ASSY, EXP FAN ADAPTER	—	1

REVISIONS



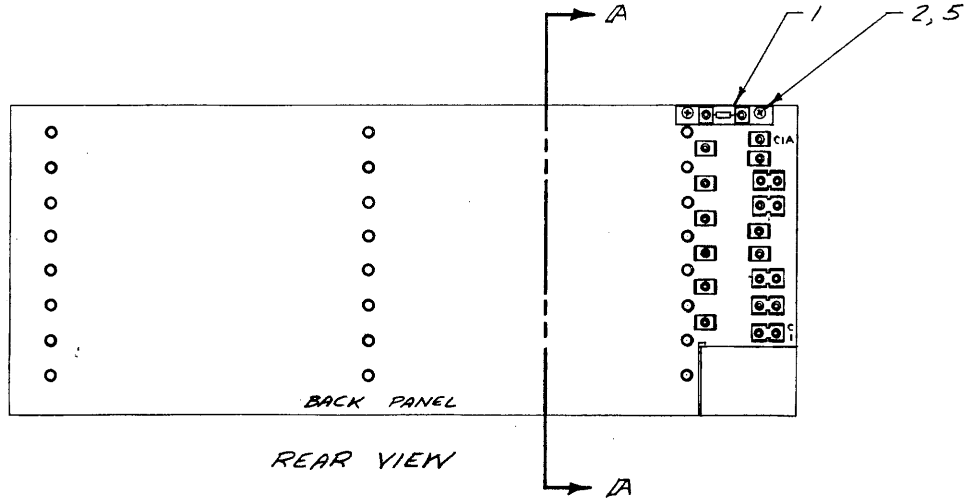
SECTION A-A

FOR 115/230V MODIFICATION KIT ONLY

INSTRUCTIONS FOR MODIFICATION KIT 39-021 F01 (115/230V)

STEP:

4. PERFORM STEPS 1, 2, & 3 OF INSTRUCTIONS BELOW
5. TO PERFORM THE FOLLOWING TWO STEPS CHASSIS MUST BE REMOVED FROM RACK AND FAN PLATE DISASSEMBLED FROM CHASSIS.
6. REMOVE EXISTING FAN CABLE AND CONNECTOR BRACKET.
7. DRILL (2) .171 HOLES AND MOUNT NEW XFMR & FAN CABLE ITEM 9 AS SHOWN USING HARDWARE ITEMS 3, 4 & 6.
8. REASSEMBLE FAN PLATE AND CONNECTOR BRACKET USING ORIGINAL HARDWARE.



REAR VIEW

INSTRUCTIONS FOR MODIFICATION KIT 39-021 F02 (115 V)

STEP:

1. REMOVE & DISCARD #4 HARDWARE & CABLE CLAMP FROM UPPER RIGHT CORNER OF BACK PANEL TO FACILITATE STEP 2.
2. MOUNT ITEM 1 (TA-TB BOARD) USING HARDWARE ITEMS 2 & 5.
3. DISCONNECT WIRE FROM C1A TAB AND CONNECT TO C1 TAB. WIRE IN POINT IS PART CARD FILE & NOT POWER SUPPLY.

INSTALLATION NOTES

1. FOR POWER SUPPLY POWERING ONE CHASSIS CONNECT FAN POWER BY USING CABLE ITEM 7.
2. FOR POWER SUPPLY POWERING TWO CHASSIS CONNECT FAN POWER BY USING CABLE ITEM 10.
3. WHEN REPLACING A MODEL 34-015 POWER SUPPLY IN A SYSTEM HAVING THREE CHASSIS USE TWO CABLES ITEM 8 TO JUMPER C1 & C2.

NOTES 1. THESE INSTRUCTIONS PERTAIN TO THE REPLACEMENT OF POWER SUPPLY MODEL 34-015 WITH A MODEL 34-020.

NAME	TITLE	DATE
W. ZILLGER	DRAFT	1-24-74
H. MATTER	CHECK	1-28-74
E. CENTOFANTI	ENG	1-28-74

TITLE INFORMATION DWG

MOD 80 CARD FILE

MODIFICATION KIT

INTERDATA®

REVISIONS

REDRAWN FROM LAYOUT; ADDED SH.0 & INCLUDED ALL CHANGES PER ECR 3215-03 & -10					
7		3215-03 3215-10		7-7-72 7-19-72	R03
REVISED SHEET 1					
DB		ECR 3215-12		7-25-72	R04
REVISED SHEET 1					
7		3215-17		9-28-72	R05
REVISED SHEET 1					
7		3215-21		10-11-72	R06
REVISED SHEET 1					
7		3215-25		10-27-72	R07
REVISED SHEET 1					
7		3215-26		11-13-72	R08
REVISED SHEET 1					
E.Q.		3215-31		1-15-73	R09
124-3 WAS NOT SPEC. 103-2 WAS SPEC. JRLRI REVISED SHEET 1					
E.Q.		3215-35		2-20-73	R10
SHT 3 WAS R08					
		3215-44		15 MAY 73	R11
REVISED SH. 4					
7		3215-46		6-30-73	R12

CONN	SHEET LOC.	MNEMONIC ROW 2	TERM NO.	MNEMONIC ROW 1	SHEET LOC.	CONN
3		GND.	24	P5	—	3
			23	RAG151	4A5	
			22	RAG141	4B5	
			21	RAG131	4C5	
			20	RAG121	4D5	
			19	RAG111	4E5	
			18	RAG081	4J5	
			17	RAG091	4H5	
			16	RAG101	4G5	
			15	RAG071	4K5	
			14	RAG061	4L5	
			13	RAG051	4M5	
			12	RAG041	4N5	
			11	RD281	2L7	
			10	RD301	2N7	
			09	RD291	2M7	
			08	RD311	2R7	
			07	RD241	2G7	
			06	RD261	2J7	
			05	RD251	2H7	
			04	RD271	2K7	
			03	RD201	2C7	
			02	RD221	2E7	
			01	RD211	2D7	
		GND	00	RD231	2F7	

CONN	SHEET LOC.	MNEMONIC ROW 2	TERM NO	MNEMONIC ROW 1	SHEET LOC.	CONN
2		GND	24	RD161	2L5	2
			23	RD171	2M5	
			22	RD181	2N5	
			21	RD191	2R5	
			20	RD121	2G5	
			19	RD131	2H5	
			18	RD141	2J5	
			17	RD151	2K5	
			16	RD081	2N1	
			15	RD091	2R1	
			14	RD101	2E5	
			13	RD111	2F5	
			12	RD041	2J1	
			11	RD051	2K1	
			10	RD061	2L1	
			09	RD071	2M1	
			08	RD001	2E1	
			07	RD011	2F1	
			06	RD021	2G1	
			05	RD031	2H1	
			04	INHCLA0	1G3	
			03	RS001	1D9	
			02	RMWR1	1E8	
			01	STRB0A	1N1	
		GND	00			

CONN. C

	SHEET LOC.	MNEMONIC
106	6C9	BLCH140
	6F9	BLCH120
	6B9	BLCH150
	6E9	BLCH130
	7A9	PSW150
	7B9	PSW140
100	7D9	PSW120
	6M9	BLCH080
	6J9	BLCH100
	6L9	BLCH090
	6H9	BLCH110
95	6B9	ALCH140
	6D9	ALCH120
	6D9	ALCH130
	6A9	ALCH150
	6G9	ALCH100
90	6K9	ALCH080
	6G9	ALCH110
	6J9	ALCH090
	6E5	ALCH040
	6B5	ALCH060
85	6A5	ALCH070
	6D5	ALCH050
	6H5	ALCH020
	6K5	ALCH000
	6G5	ALCH030
80	6K5	ALCH010
	6M5	BLCH000
	6J5	BLCH020
	6H5	BLCH030
	—	GND
75	6L5	BLCH010
	6F5	BLCH040
	6D5	BLCH060
	6C5	BLCH070
	6F5	BLCH050
70	4E6	CRLR120
	4C6	CRLR130
	4B6	CRLR140
	4A6	CRLR150
	4J6	CRLR080
	4H6	CRLR090
64	4G6	CRLR100

CONN. C

MNEMONIC	SHT LOC	
NOT USED	—	63
CRLR040	4N6	62
CELR110	4F6	
CELR050	4N6	60
CRLR060	4L6	
CKLR070	4K6	
RAG151	4A5	
RAG141	4B5	
RAG131	4C5	55
RAG121	4D5	
RAG111	4E5	
RAG081	4J5	
RAG091	4H5	
RAG101	4G5	50
RAG071	4K5	
RAG061	4L5	
RAG051	4M5	
RAG041	4N5	
RD161	2L5	45
RD171	2M5	
RD181	2N5	
RD191	2R5	
RD121	2G5	
RD131	2H5	40
RD141	2J5	
RD151	2K5	
RD081	2N1	
RD091	2R1	
RD101	2E5	35
RD111	2F5	
RD041	2J1	
RD051	2K1	
RD061	2L1	
RD071	2M1	30
RD001	2E1	
RD011	2F1	
RD021	2G1	
RD031	2H1	
GND	—	25
RD281	2L7	
RD291	2M7	
RD301	2N7	
RD311	2R7	
RD241	2G7	20
RD251	2H7	
RD261	2J7	
RD271	2K7	
RD201	2C7	
RD211	2D7	15
RD221	2E7	
RD231	2F7	
GND	—	
STRB0	1K2	
LDELR0	2A5	10
INHCLB0	1G3	
NOT USED	—	
NOT USED	—	
RS001	1E8	
GND	—	05
GND	—	
GND	—	
GND	—	
NOT USED	—	01

CONN. D

SHEET LOC.	MNEMONIC	
9E1	ST151	48
9E1	ST141	
9N1	ST121	
9F1	ST001	
9E1	ST011	
9M1	ST101	
9N1	ST111	
—	NOT USED	
9N1	ST131	40
9L1	ST081	
9K1	ST061	
9K1	ST071	
9L1	ST091	
9H1	ST041	35
9H1	ST021	
9H1	ST031	
—	GND	
9J1	ST051	
4M3	RGL0	
4M3	RGH0	29

SHEET LOC.	MNEMONIC	
5F9	BSEL001	28
5M9	ASEL001	
5M9	ASEL000	
10A9	SSEL040	25
5A9	BSEL040	
5H9	ASEL040	
10H9	SSEL001	
10C9	SSEL030	
5C9	BSEL030	20
5J9	ASEL030	
10E9	SSEL020	
5D9	BSEL020	
5K9	ASEL020	
10F9	SSEL010	15
5E9	BSEL010	
5L9	ASEL010	
5F9	BSEL000	
3A9	VFLG1	
3A9	CFLG1	10
3A6	ZFLG1	
3A7	LFLG1	
3A7	GFLG1	
1H5	RSAY1	
—	GND	05
	NOT USED	
10H9	SSEL000	
1J8	RSBY1	
1E5	REGWRT0	01

CONN	SHEET LOC.	MNEMONIC ROW 1	TERM No	MNEMONIC ROW 2	SHEET LOC	CONN
1/F		P5	41	GND		1/F
		GND	40	GND		
		P15	39			
		N15	38			
	8N1	CD141	37	CD151	8N1	
	8M1	CD121	36	CD131	8M1	
	8K1	CD101	35	CD111	8K1	
	8J1	CD081	34	CD091	8J1	
	8G1	CD061	33	CD071	8G1	
	8F1	CD041	32	CD051	8F1	
	8D1	CD021	31	CD031	8D1	
	8B1	CD001	30	CD011	8C1	
	9D9	CA140	29	CA150	9E9	
	9N9	CA120	28	CA130	9N9	
	9M9	CA100	27	CA110	9N9	
	9L9	CA080	26	CA090	9L9	
	9K9	CA060	25	CA070	9K9	
	9H9	CA040	24	CA050	9J9	
	9H9	CA020	23	CA030	9H9	
			22			
	9F9	CA000	21	CA010	9F9	
	1R7	CREQ0	20	CFTCH0	1R4	
	1K3	CRDY0	19	CWRT0	1R8	
	5N4	A140	18	A150	5N4	
	5N4	A120	17	A130	5N4	
	5N5	A100	16	A110	5N4	
	5N5	A080	15	A090	5N5	
	5N5	A060	14	A070	5N5	
	5N5	A040	13	A050	5N5	
	5N6	A020	12	A030	5N6	
	5N6	A000	11	A010	5N6	
	4B9	S140	10	S150	4A9	
	4D9	S120	09	S130	4C9	
	4G9	S100	08	S110	4E9	
	4J9	S080	07	S090	4H9	
	4L9	S060	06	S070	4K9	
	4N9	S040	05	S050	4M9	
	4N9	S020	04	S030	4R9	
	4N9	S000	03	S010	4N9	
	7B1	GCC1	02	LCC1	7A1	
		GND	01	GND		
		P5	00	GND		

CONN	SHEET LOC.	MNEMONIC (ROW 1)	TERM No	MNEMONIC (ROW 2)	SHEET LOC.	CONN
0/E		P5	41	GND		0/E
		GND	40	GND		
		P15	39	SCC0	7E6	
		N15	38	CCC1	7D1	
			37	VCC1	7C1	
			36			
	4A1	B140	35	B150	4M1	
	4C1	B120	34	B130	4B1	
	4F1	B100	33	B110	4D1	
	4H1	B080	32	B090	4G1	
	4K1	B060	31	B070	4J1	
	4M1	B040	30	B050	4L1	
	4N1	B020	29	B030	4R1	
	4N1	B000	28	B010	4N1	
	10M9	KS1G0	27	PVMD0	3M1	
	1J9	SCLR0	26			
			25			
			24			
			23	ATN000	3F2	
			22			
			21			
			20			
			19			
			18			
			17			
			16			
			15			
			14			
			13			
			12			
			11			
	3L5	PPF0	10	MMF0	3F4	
	3F3	ATN010	09	ATN030	3F3	
	3E4	DSPLY1	08	ATN020	3F3	
	10M4	MDSL020	07	MDS1G0	2A6	
	10L4	MDSL000	06	MDSL010	10L4	
	10N4	FSEL020	05	FSEL030	10N4	
	10R4	FSEL000	04	FSEL010	10R4	
	10H4	STRT0	03	MEIN0	1D2	
		P5	02	P5		
		GND	01	GND		
		P5	00	GND		

NOTE: THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION

BOARD NO.	DESCRIPTION
35-403 R11	USES 25-295 R01 COPPER PER NOTE 1 SH.1
35-403 R13	USES 25-295 R02 COPPER

SHEET INDEX	REV. LEVEL	12	10	3	4	4	3	3	3	3	3	3
	SHEET No	0	1	2	3	4	5	6	7	8	9	10

1. ALL C, D, E & F CONNECTORS ARE DIRECT CONTACTS TO THE ALU BOARD, SEE SCHEMATIC 35-404D08.

NAME	TITLE	DATE
R. MEGINNIES	DRAFT	6/23/72
J.F. FLEMING	CHK	10-9-72
R.E. SCHUNNEMAN	ENGR	
R.E. JONES	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC MODEL 80 CPU

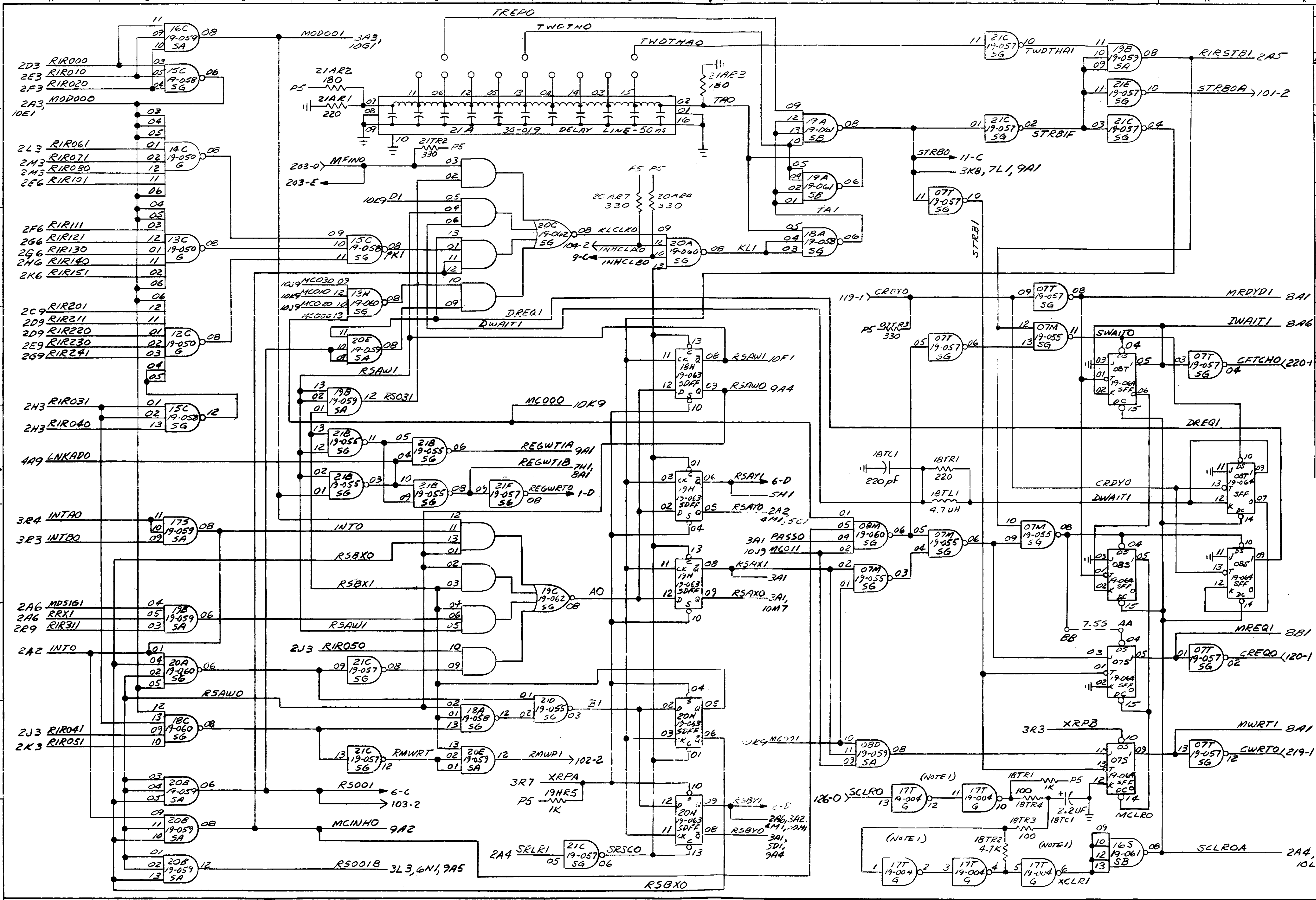
TASK NO. 03215

DWG NO. 35-403R12D08

SHEET 0 OF 10

11 SHEETS TOTAL

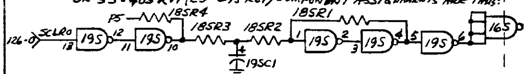
INTERDATA®



2D3 RIR000
2E3 RIR010
2F3 RIR020
2A3, 10E1 MOD000
16C 19-059 SA
15C 19-058 SG
MOD001 3A3, 10G1
TREPO
TWOTHO
TWOTHAO
21AR2 180
21AR1 220
P5
21A 30-019 DELAY LINE-50 ns
21AR3 180
TAO
21TR2 330
2L3 RIR061
2M3 RIR071
2M3 RIR080
2E6 RIR101
14C 19-050 G
2F6 RIR111
2G6 RIR121
2G6 RIR130
2H6 RIR140
2K6 RIR151
13C 19-050 G
2C9 RIR201
2D9 RIR211
2D9 RIR220
2E9 RIR230
2G9 RIR241
12C 19-050 G
2H3 RIR031
2H3 RIR040
15C 19-058 SG
203-0 MFINO
203-E
10L9 D1
20C 19-062 SG
KLCLKO
20AR7 330
20AR4 330
104-2 INHCLAO
9-C INHCLBO
20A 19-060 SG
KL1
15C 19-058 SG PK1
13H 19-060 SG
MC030 MC010 MC020 MC0013
20E 19-059 SA
RSAW1
DREQ1
DWAIT1
19B 19-059 SA RS031
MC000 10K9
21B 19-056 SG
21B 19-055 SG
REGWT1A 9A1
REGWT1B 7H1, 8A1
21F 19-057 SG REGWRTO 1-D
4A9 LNKADO
3R4 INTAO
3R3 INTBO
17S 19-059 SA
INTO
RSBXO
RSBX1
19C 19-062 SG AO
2A6 MDS161
2A6 RRX1
2R9 RIR311
19B 19-059 SA
RSAW1
2A2 INTO
20A 19-060 SG
2J3 RIR050
21C 19-057 SG
RSAWO
18A 19-058 SG
21D 19-055 SG B1
2J3 RIR041
2K3 RIR051
18C 19-060 SG
21C 19-057 SG RMWRT
20E 19-059 SA RMWP1 102-2
20B 19-059 SA
RS001 6-C 103-2
MCINHO 9A2
RS001B 3L3, 6N1, 9A5
2A4 SRLR1
21C 19-057 SG SRSCO
RSBXO
18H 19-063 SDFF RSAW1 10F1 RSAWO 9A4
19H 19-063 SDFF RSAY1 6-D 5H1 RSAYO 2A2 4M1, SC1
13H 19-063 SDFF KSAX1 3A1 RSAXO 3A1, 10M7
20N 19-063 SDFF
3R7 XRPA
19HRS 1K
20H 19-063 SDFF RSBY1 6-D 2A6, 3A2, 4M1, 0M1 RSBYO 3A1, 5D1, 9A4
21C 19-057 SG TWOTHA1
19B 19-059 SA RIRSTB1 2A5
21E 19-057 SG STRBOA 101-2
19A 19-061 SB
21C 19-057 SG STRB1F
21C 19-057 SG
STRBO 11-C 3K8, 7L1, 9A1
07T 19-057 SG
19A 19-061 SB
TA1
18A 19-058 SG
STRB1
119-1 CRDYO
07T 19-057 SG MRDY1 8A1
P5 07TR3 330
07M 19-055 SG
IWAIT1 8A6
07T 19-057 SG
SWAITO
08T 19-064 SFF
07T 19-057 SG CFTCHO 220-1
DREQ1
18TC1 220pf
18TR1 220
18TL1 4.7uH
CRDYO
DWAIT1
3A1 PASSO
10J9 MCO11
08M 19-060 SG
07M 19-055 SG
07M 19-055 SG
07M 19-059 SG
08S 19-064 SFF
7.55 AA
BB
07S 19-064 SFF
MREQ1 8B1
07T 19-057 SG CREQO 120-1
3R3 XRPB
07S 19-064 SFF
MWRT1 8A1
07T 19-057 SG CWRTO 219-1
MCLRO
08D 19-059 SA
126-0 SCLRO
17T 19-004 G
(NOTE 1)
18TR1 100 1K P5
18TR4
2.2UF 18TC1
18TR3 100
18TR2 4.7K
17T 19-004 G XCLR1
16S 19-061 SB
SCLROA 2A4, 3F4, 10L9

REVISIONS					
REMOVED CONNECTION TO PIN 126-E IN AREA K9					
DB		ECR 3215-12		7-25-72	R04
ADDED - 19-031 (19S) AND ASSOC DESCRETE COMPS. AT L9. REMOVED - 126-0 WAS TO 11S01; 11S02 WAS TO 16S09.					
7		3215-17		9-28-72	R05
CHANGED - 08T11 WAS TO 08T02, 08T13 WAS TO 08T01, 08T12 WAS TO 08T06, 08T10 WAS TO XRPB, 07M10 & 12 WERE TO 07T10, DREQ1 WAS P/O MREQ1, DWAIT1 WAS P/O MWAIT1. ADDED - CKT CONN AT 08T07, 09 & 08S09, 10, 11, 12, 13, 14.					
7		3215-21		10-11-72	R06
CHANGED - AT L9, 19S WAS 19-031 & ASSOC DESCRETE COMPS WERE PER ECR 3215-17 (R05); AT N5, 08S13 & 08T13 WERE TO 07T09 (CRDYO); ADDED 10S13 TO 07T08 & 10S12 TO 08T13. SCLRO WAS TO 19S03.					
7		3215-25		10-27-72	R07
AT N5, 08T13 & 08S13 WERE TO 10S12, 10S13 WAS TO 07T08. ADDED - 18TR1, 18TC1, 18TL1 ON DWAIT1 LINE AT K5.					
7		3215-26		11-13-72	R08
IN AREA K5, 18TC1 WAS 100PF IN AREA K4, 07TR2, 330Ω WAS SPEC BETWEEN CRDYO & GRD.					
Cg.		3215-31		1-15-73	R09
IN AREA D, E-9 103-2 WAS NOT SPEC; ADDED NOTE 1.					
Cg.	CM	3215-35		2-15-73	R10

NOTES 1. ON 35-403R12 (25-295R02) 'SCLRO' CIRCUIT IS AS SHOWN; ON 35-403R11 (25-295R01) COMPONENT ASSIGNMENTS ARE THUS:



126-0 SCLRO
19S
P5
18SR4
18SR3
18SR2
18SR1
19SC1
16S

BRUNING 44-231 15043

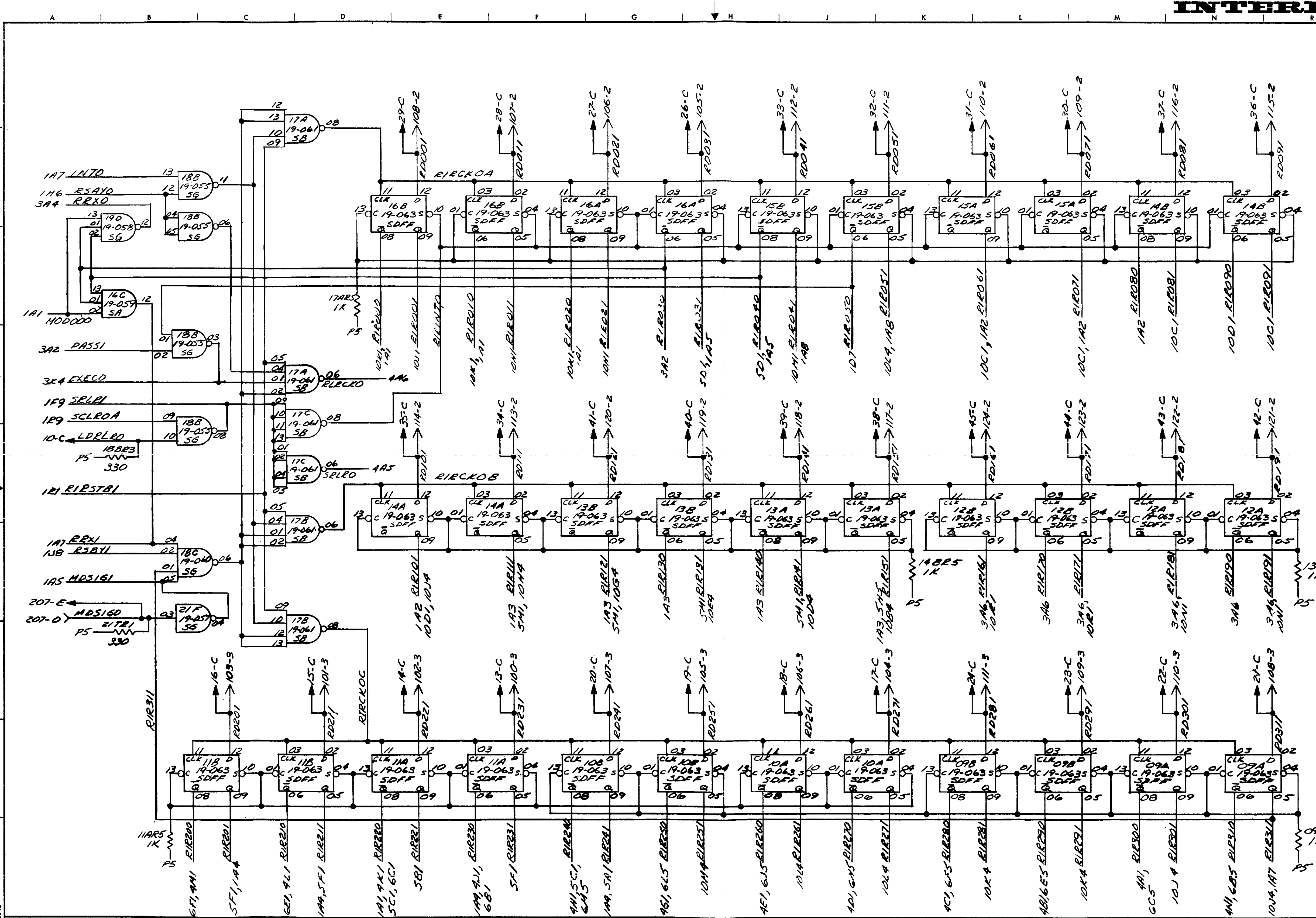
NAME	TITLE	DATE
R MEGINLEY	DRAFT	5/2/72
7	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 80 CPU

TASK NO. 03215
DWG NO. 35-403E10 D08
SHEET 1 OF 10

INTERDATA®

REVISIONS



1A7 INTO
1H6 RSAY0
3A4 RRX0
1A1 H0D000
3A2 PASS1
3K4 EXEC0
1F9 SRLR1
1B9 SCLR0A
10-C LDRLR0
P5 18BR3 330
1B1 R1RSTB1
1A7 RRX1
1J8 RSBY1
1A5 MDS161
207-E
207-D MDS160
P5 21TB1 330
18B 19-055 5G
19D 19-058 5G
16C 19-057 5A
17A 19-061 5B
17B 19-061 5B
17C 19-061 5B
18C 19-060 5G
21F 19-057 5G
RLECK0 4A6
SRLR0 4A5
R1RCK0A
R1RCK0B
R1RCK0C
17ARS 1K P5
14BR5 1K P5
13BR5 1K P5
11ARS 1K P5
09BR6 1K P5
R1R311
16B 19-063 SDFF
16A 19-063 SDFF
15B 19-063 SDFF
15A 19-063 SDFF
14B 19-063 SDFF
14A 19-063 SDFF
13B 19-063 SDFF
13A 19-063 SDFF
12B 19-063 SDFF
12A 19-063 SDFF
11B 19-063 SDFF
11A 19-063 SDFF
10B 19-063 SDFF
10A 19-063 SDFF
09B 19-063 SDFF
09A 19-063 SDFF
RD001 29-C 108-2
RD011 28-C 107-2
RD021 27-C 106-2
RD031 26-C 105-2
RD041 33-C 112-2
RD051 32-C 111-2
RD061 31-C 110-2
RD071 30-C 109-2
RD081 37-C 116-2
RD091 36-C 115-2
RD101 35-C 114-2
RD111 34-C 113-2
RD121 41-C 120-2
RD131 40-C 119-2
RD141 39-C 118-2
RD151 38-C 117-2
RD161 45-C 124-2
RD171 44-C 123-2
RD181 43-C 122-2
RD191 42-C 121-2
RD201 16-C 109-3
RD211 15-C 101-3
RD221 14-C 102-3
RD231 13-C 100-3
RD241 20-C 107-3
RD251 19-C 105-3
RD261 18-C 106-3
RD271 17-C 104-3
RD281 24-C 111-3
RD291 23-C 109-3
RD301 22-C 110-3
RD311 21-C 108-3
R1R000 R1R001 R1R010 R1R011 R1R020 R1R021 R1R030 R1R031 R1R040 R1R041 R1R050 R1R051 R1R061 R1R071 R1R080 R1R081 R1R090 R1R091
R1R101 R1R111 R1R121 R1R130 R1R131 R1R140 R1R141 R1R151 R1R161 R1R170 R1R171 R1R181 R1R190 R1R191
R1R200 R1R201 R1R210 R1R211 R1R220 R1R221 R1R230 R1R231 R1R240 R1R241 R1R250 R1R251 R1R260 R1R261 R1R270 R1R271 R1R280 R1R281 R1R290 R1R291 R1R300 R1R301 R1R310 R1R311

NOTES

BRUNING 44-231 15043

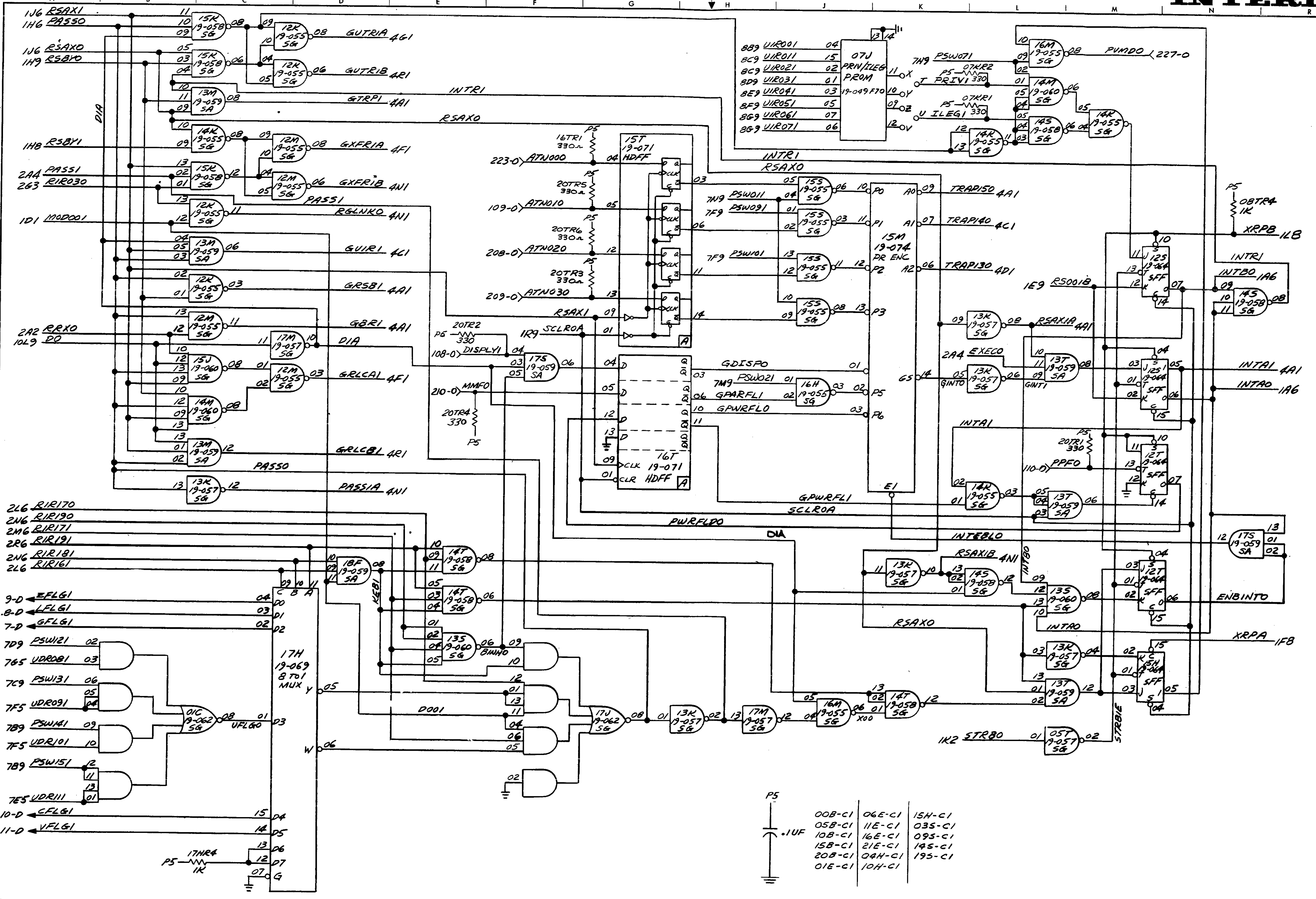
NAME	TITLE	DATE
R MCGINLEY	DRAFT	5/4/72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 80 CPU

TASK NO. 03215
DWG NO. 35-403 R03 D08
SHEET 2-10

INTERDATA®

REVISIONS				
07J WAS 19-080 F33 ADDED LOCATIONS OF .1UF DECOUPLING CAPS.				
		3215 43,44	15 MAY 13	R04



1J6 RSAX1
1H6 PASSO
1J6 RSAXO
1H9 RSB1O
1H8 RSBY1
2A4 PASS1
2G3 R1RO30
1D1 MODOO1
2A2 RRXO
10L9 DO
15K 19-058 SG
12K 19-055 SG
13M 19-059 SA
14K 19-055 SG
12M 19-055 SG
15J 19-060 SG
14M 19-060 SG
13K 19-057 SG
17M 19-057 SG
GUTR1A 4G1
GUTR1B 4R1
INTR1
GTRP1 4A1
RSAXO
GXFR1A 4F1
GXFR1B 4N1
PASS1
RGLNKO 4N1
GUIR1 4C1
GRSB1 4A1
GBR1 4A1
D1A
GRLCA1 4F1
GRLCB1 4R1
PASSO
PASS1A 4N1
P5
16TR1 330Ω
223-0 ATNOOO
20TR5 330Ω
109-0 ATNO10
20TR6 330Ω
208-0 ATNO20
20TR3 330Ω
209-0 ATNO30
15T 19-071 HDFF
RSAX1
20TR2 330
108-0 DISPLY1
1R9 SCLROA
17S 19-059 SA
210-0 MMFO
20TR4 330
16T 19-071 HDFF
CLK
CLR
GDISPO
7M9 PSWO21
16H 19-055 SG
GPARFL1
GPWRFLO
GPWRFL1
SCLROA
PWRFLDO
D1A
8B9 U1ROO1
8C9 U1RO11
8C9 U1RO21
8D9 U1RO31
8E9 U1RO41
8F9 U1RO51
8G9 U1RO61
8G9 U1RO71
07J PRIV/ILEG PROM 19-049 F70
7H9 PSWO71
07KR2
J PRIV1 330
07KR1
U ILEG1 330
16M 19-055 SG
PVMDO 227-0
14M 19-060 SG
14S 19-058 SG
INTR1
RSAXO
7N9 PSWO11
7F9 PSWO91
7F9 PSW1O1
15S 19-055 SG
15M 19-074 PR ENC
TRAP15O 4A1
TRAP14O 4C1
TRAP13O 4D1
E1
08TR4 1K
XRPB 1L8
INTR1
INTBO 1A6
1E9 RSOO1B
12S 19-064 SFF
13K 19-057 SG
RSAX1A 4A1
2A4 EXECO
G1NTO
13T 19-059 SA
G1NT1
12S1 19-064 SFF
INTA1 4A1
INTAO 1A6
INTA1
20TR1 330
110-0 PPFO
12T 19-064 SFF
INTEBLO
17S 19-059 SA
RSAX1B 4N1
INTBO
13S 19-060 SG
12T 19-064 SFF
ENBINTO
INTAO
XRPA 1F8
14S 19-058 SG
12H 19-064 SFF
STRBIE
1K2 STRBO
05T 19-057 SG
2L6 R1R170
2N6 R1R190
2M6 R1R171
2R6 R1R191
2N6 R1R181
2L6 R1R161
18F 19-059 SA
KEB1
14T 19-058 SG
13S 19-060 SG
BMHO
9-D EFLG1
8-D LFLG1
7-D GFLG1
17H 19-069 8 TO 1 MUX
7D9 PSW121
7G5 UDRO81
7C9 PSW131
7F5 UDRO91
7B9 PSW141
7F5 UDR1O1
7B9 PSW151
7E5 UDR111
01C 19-062 SG
VFLGO
10-D CFLG1
11-D VFLG1
17HR4 1K
DOO1
17J 19-062 SG
13K 19-057 SG
17M 19-057 SG
16M 19-055 SG
X00
14T 19-058 SG
P5
.1UF

00B-C1	06E-C1	15H-C1
05B-C1	11E-C1	03S-C1
10B-C1	16E-C1	09S-C1
15B-C1	21E-C1	14S-C1
20B-C1	04H-C1	19S-C1
01E-C1	10H-C1	

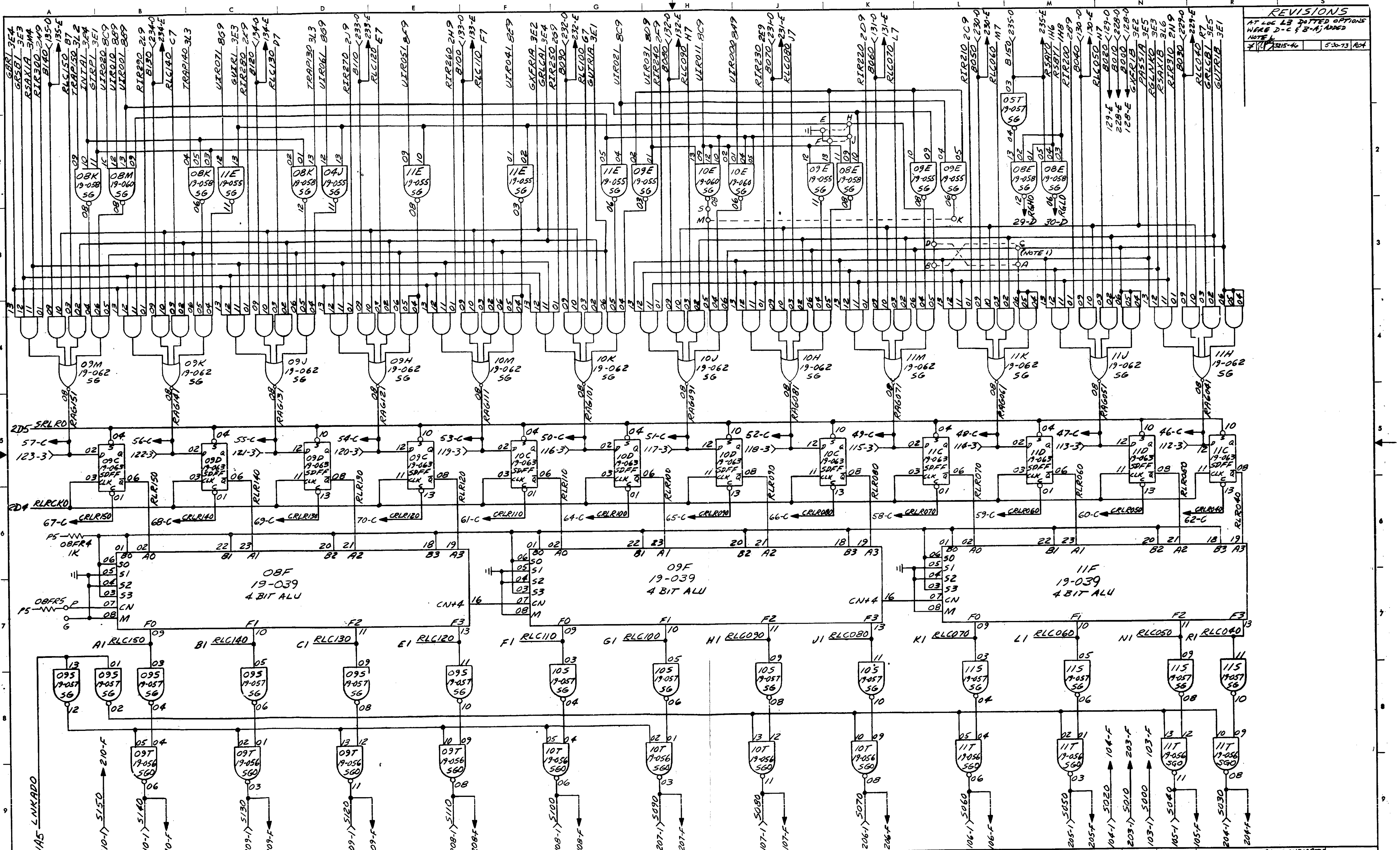
NOTES

BRUNING 44-231 16042

NAME		TITLE	DATE	TITLE FUNCTIONAL SCHEMATIC
		DRAFT		MODEL 80 CPU
		CHK		
		ENGR		TASK NO. 03215
		DIR ENG		DWG NO. 35-403R04D08 SHEET 3 OF 10

INTERDATA®

REVISIONS				
AT LOC L3 DOTTED OPTIONS WERE D-C & B-A; ADDED NOTE 1.				
7	3215-46		5-30-73	R04



09M 19-062 SG
09K 19-062 SG
09J 19-062 SG
09H 19-062 SG
10M 19-062 SG
10K 19-062 SG
10J 19-062 SG
10H 19-062 SG
11M 19-062 SG
11K 19-062 SG
11J 19-062 SG
11H 19-062 SG
08K 19-058 SG
08M 19-060 SG
11E 19-055 SG
04J 19-055 SG
10E 19-060 SG
09E 19-055 SG
08E 19-058 SG
05T 19-057 SG
09C 19-063 SDFF
09D 19-063 SDFF
10C 19-063 SDFF
10D 19-063 SDFF
11C 19-063 SDFF
11D 19-063 SDFF
08F 19-039 4 BIT ALU
09F 19-039 4 BIT ALU
11F 19-039 4 BIT ALU
09S 19-057 SG
10S 19-057 SG
11S 19-057 SG
09T 19-056 SGO
10T 19-056 SGO
11T 19-056 SGO
2D5 SRLRO
2D4 RLRCKO
P5 08FR4 1K
P5 08FR5
(NOTE 1)
29-D 30-D
1A5 LNKADO
RAG151
RAG141
RAG131
RAG121
RAG111
RAG101
RAG091
RAG081
RAG071
RAG061
RAG051
RAG041
RLC150
RLC140
RLC130
RLC120
RLC110
RLC100
RLC090
RLC080
RLC070
RLC060
RLC050
RLC040
S150
S140
S130
S120
S110
S100
S090
S080
S070
S060
S050
S040
S030
S020
S010
S000

NOTES 1. TRANSLATE OPTION COPPER STRAPS SHOWN:
E-F, H-J, M-S, A-C, B-D.
FOR NON-TRANSLATE OPTION CUT ALL COPPER STRAPS & CONNECT AS FOLLOWS:
E-J, F-H, M-K, A-D, B-C.

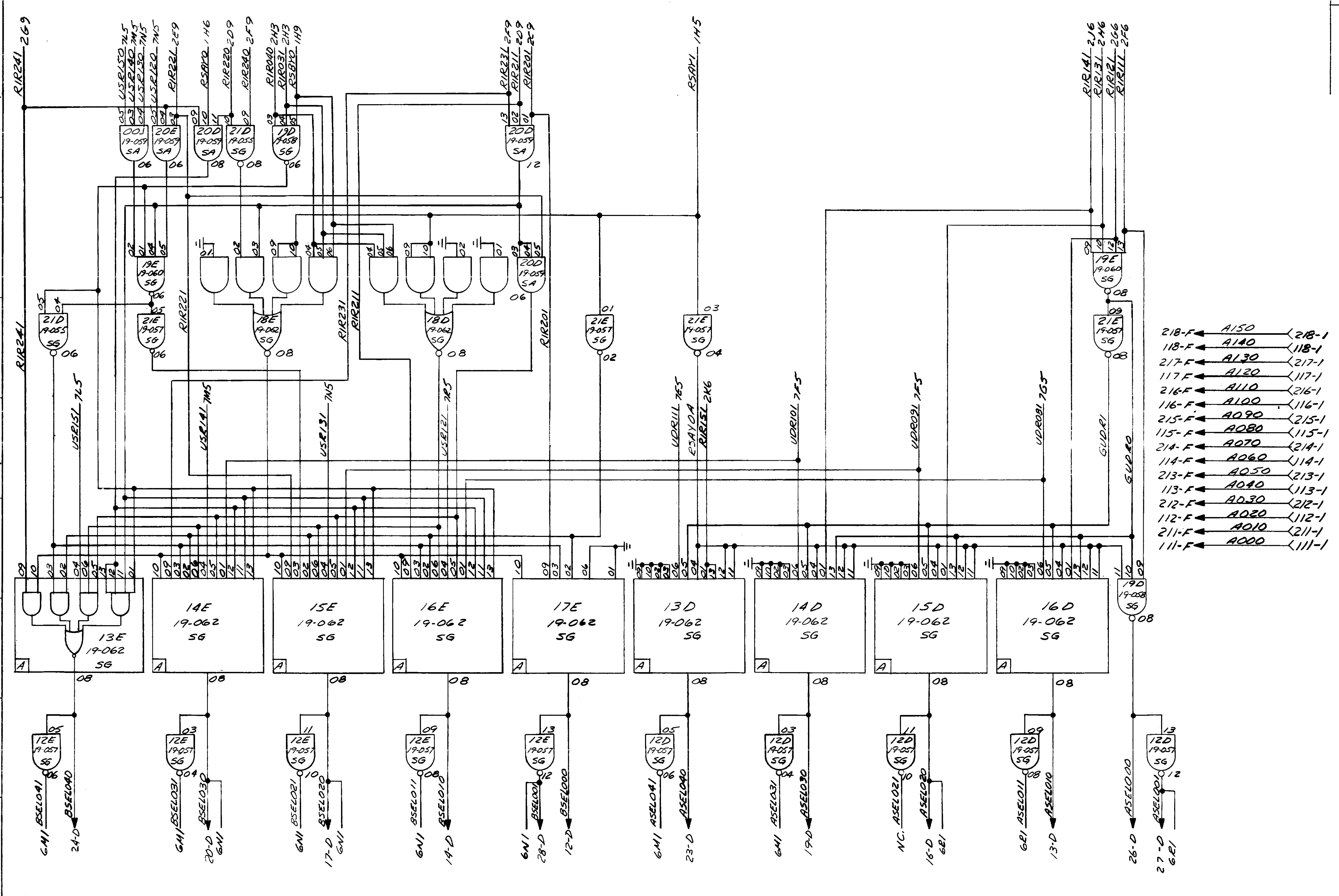
NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 80 CPU

TASK NO. 03215
DWG NO. 35-403 R04 D08
SHEET 4 OF 10

INTERDATA®

REVISIONS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USR150 7L5
USR140 7M5
USR130 7N5
USR120 7N5
RIR221 2E9
RSAY0 1H6
RIR220 2D9
RIR240 2F9
RIR040 2H3
RIR031 2H3
RSBY0 1H9
RIR231 2F9
RIR211 2D9
RIR201 2C9
RSAY1 1H5
RIR141 2J6
RIR131 2H6
RIR121 2G6
RIR111 2F6
00J 19-057 SA
20E 19-057 SA
20D 19-057 SA
21D 19-055 SG
19D 19-058 SG
19E 19-060 SG
20D 19-057 SA
21D 19-055 SG
21E 19-057 SG
18E 19-062 SG
18D 19-062 SG
21E 19-057 SG
19E 19-060 SG
USR151 7L5
USR141 7M5
USR131 7N5
USR121 7R5
UDR111 7E5
ESAY0A
RIR151 2K6
UDR101 7F5
UDR091 7F5
UDR081 7G5
GUDR1
GUDR0
13E 19-062 SG
14E 19-062 SG
15E 19-062 SG
16E 19-062 SG
17E 19-062 SG
13D 19-062 SG
14D 19-062 SG
15D 19-062 SG
16D 19-062 SG
19D 19-058 SG
12E 19-057 SG
12D 19-057 SG
218-F A150 218-1
118-F A140 118-1
217-F A130 217-1
117-F A120 117-1
216-F A110 216-1
116-F A100 116-1
215-F A090 215-1
115-F A080 115-1
214-F A070 214-1
114-F A060 114-1
213-F A050 213-1
113-F A040 113-1
212-F A030 212-1
112-F A020 112-1
211-F A010 211-1
111-F A000 111-1
BSEL041 GM1
BSEL040 24-D
BSEL031 GM1
BSEL030 20-D GN1
BSEL021 GN1
BSEL020 17-D GN1
BSEL011 GN1
BSEL010 14-D
BSEL001 GN1 28-D
BSEL000 12-D
ASEL041 GM1
ASEL040 23-D
ASEL031 GM1
ASEL030 19-D
ASEL021 NC.
ASEL020 16-D GR1
ASEL011 GR1
ASEL010 13-D
ASEL020 26-D
ASEL001 27-D GR1

NOTES

BRUNING 44-231 16042

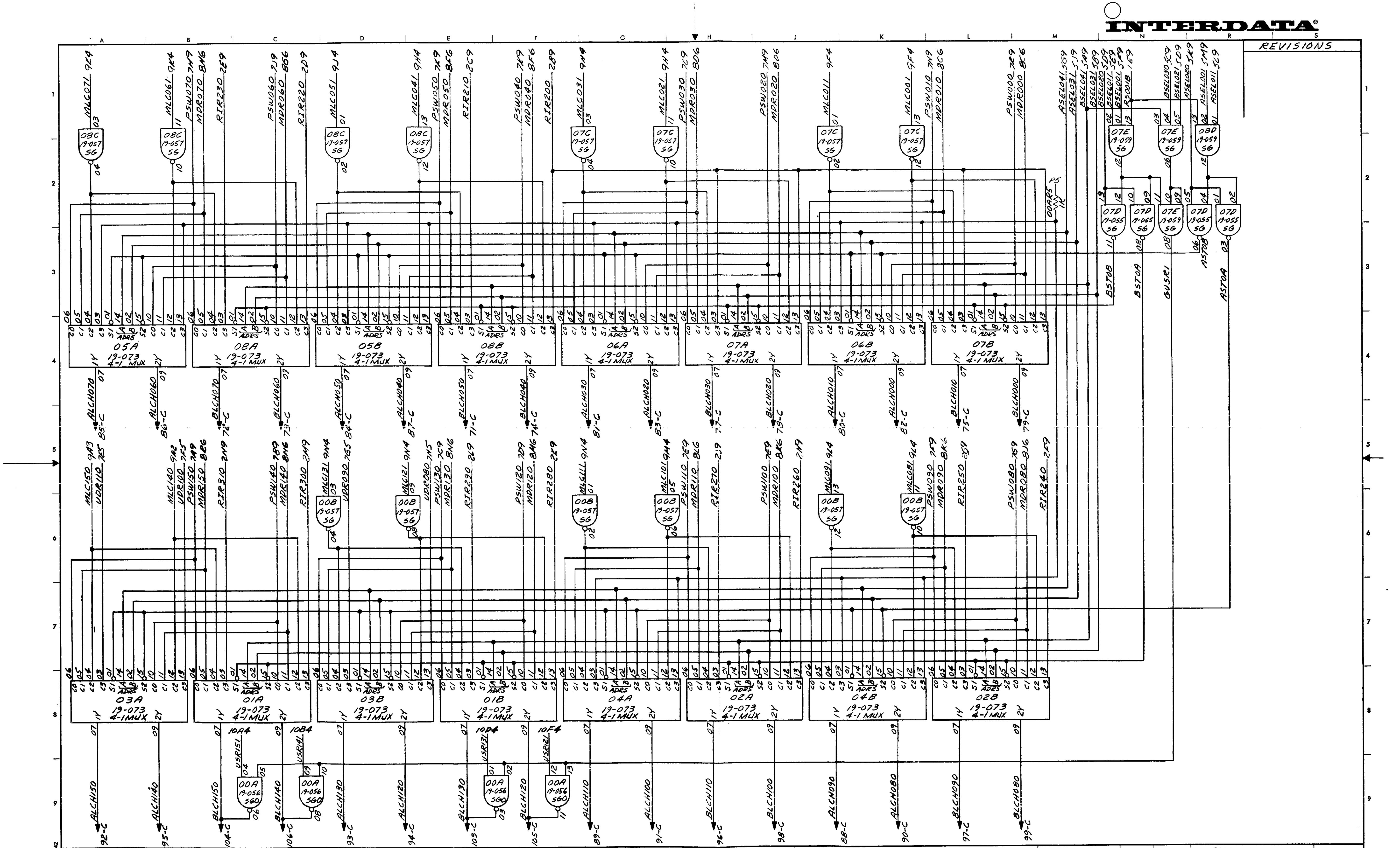
NAME	TITLE	DATE
R MEGINLEY	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 80 CPU

TASK NO. 03215
DWG NO. 35-403 R03D08
SHEET 5-10

INTERDATA®

REVISIONS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MLC061 9K4
PSW070 7H9
MDR070 8H6
RIR230 2E9
PSW060 7J9
MDR060 8B6
RIR220 2D9
MLC051 9J4
MLC041 9H4
PSW050 7K9
MDR050 8F6
RIR210 2C9
PSW040 7K9
MDR040 8F6
RIR200 2B9
MLC031 9H4
MLC021 9H4
PSW030 7L9
MDR030 8D6
PSW020 7M9
MDR020 8D6
MLC011 9F4
MLC001 9F4
PSW010 7N9
MDR010 8C6
PSW000 7P9
MDR000 8C6
ASEL041 5G9
ASEL031 5J9
BSEL041 5M9
BSEL031 5P9
BSEL020 5Q9
BSEL011 5E9
BSEL001 5F9
RS001B 1E9
BSEL030 5G9
BSEL021 5D9
ASEL020 5K9
ASEL001 5M9
ASEL011 5Q9
08C 19-057 SG
07C 19-057 SG
07E 19-059 SG
08D 19-059 SG
07D 19-055 SG
P5
DDARS 1K
BST0B
BST0A
GVSR1
AST0B
AST0A
05A 19-073 4-1 MUX
08A 19-073 4-1 MUX
05B 19-073 4-1 MUX
08B 19-073 4-1 MUX
06A 19-073 4-1 MUX
07A 19-073 4-1 MUX
06B 19-073 4-1 MUX
07B 19-073 4-1 MUX
ADRS
ALCH070 85-C
ALCH060 86-C
BLCH070 72-C
BLCH060 73-C
ALCH050 84-C
ALCH040 87-C
BLCH050 71-C
BLCH040 74-C
ALCH030 81-C
ALCH020 83-C
BLCH030 77-C
BLCH020 78-C
ALCH010 80-C
ALCH000 82-C
BLCH010 75-C
BLCH000 79-C
MLC150 9A3
UDR110 7E5
MLC140 9A2
UDR100 7F5
PSW150 7A9
MDR150 8B6
RIR310 2H9
PSW140 7B9
MDR140 8H6
RIR300 2H9
MLC131 9H4
UDR090 7E5
MLC121 9H4
UDR080 7H5
PSW130 7C9
MDR130 8N6
RIR290 2G9
PSW120 7D9
MDR120 8M6
RIR280 2E9
MLC111 9H4
MLC101 9H4
PSW110 7E9
MDR110 8L6
RIR270 2J9
PSW100 7F9
MDR100 8K6
RIR260 2H9
MLC091 9L4
MLC081 9L4
PSW090 7F9
MDR090 8K6
RIR250 2G9
PSW080 7G9
MDR080 8J6
RIR240 2F9
00B 19-057 SG
03A 19-073 4-1 MUX
01A 19-073 4-1 MUX
03B 19-073 4-1 MUX
01B 19-073 4-1 MUX
04A 19-073 4-1 MUX
02A 19-073 4-1 MUX
04B 19-073 4-1 MUX
02B 19-073 4-1 MUX
10A4 USR151
10B4 USR141
10D4 USR131
10F4 USR121
00A 19-056 SG0
ALCH150 92-C
ALCH140 95-C
BLCH150 104-C
BLCH140 106-C
ALCH130 93-C
ALCH120 94-C
BLCH130 103-C
BLCH120 105-C
ALCH110 89-C
ALCH100 91-C
BLCH110 96-C
BLCH100 98-C
ALCH090 88-C
ALCH080 90-C
BLCH090 97-C
BLCH080 99-C

NOTES

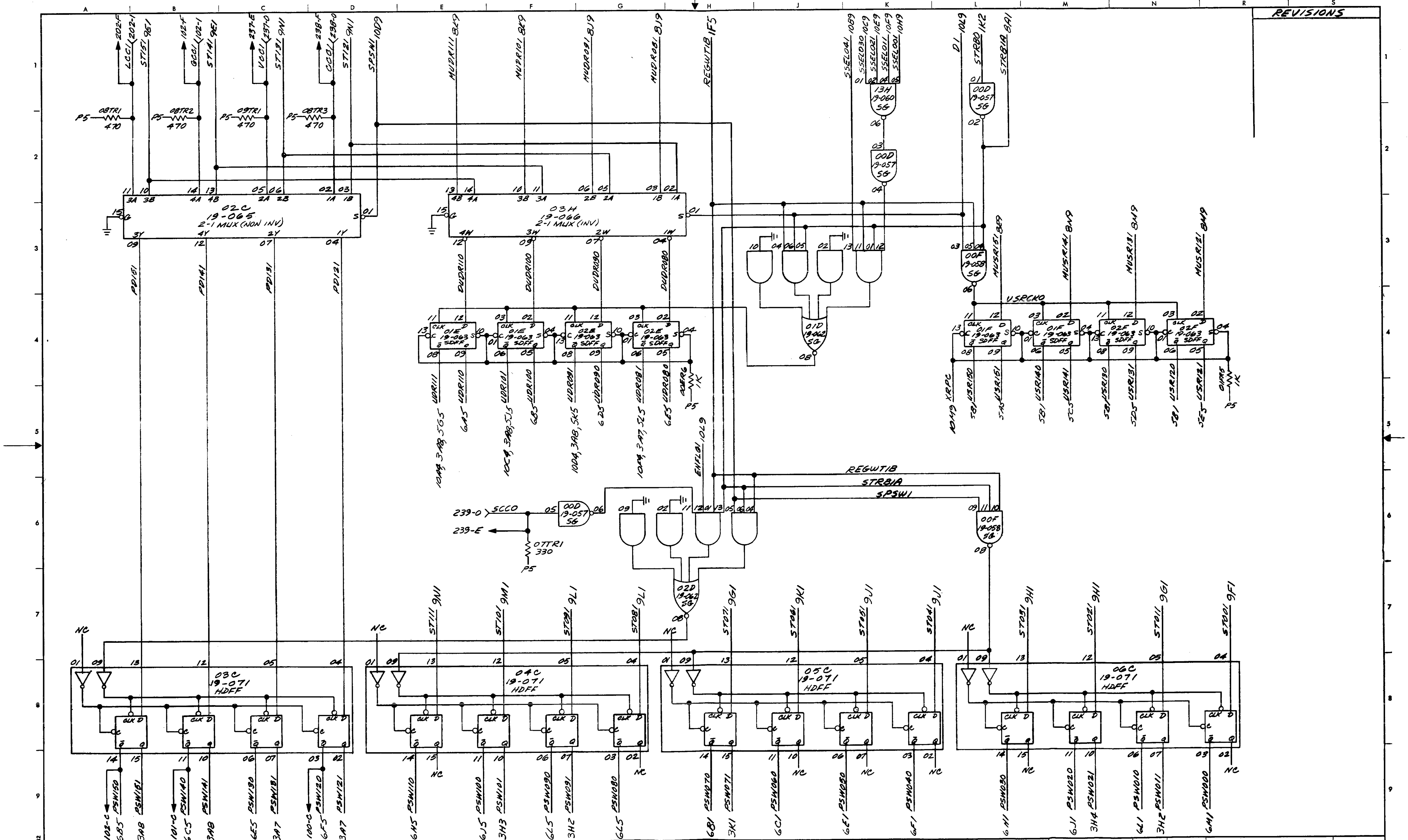
BRUNING 44-231 16042

NAME	TITLE	DATE
	DRAFT	
⅟	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 80 CPU

TASK NO. 03215
DWG NO. 35-403 R03 D08
SHEET 6 OF 10

INTERDATA


REVISIONS
02C 19-065 2-1 MUX (NON INV)
03H 19-066 2-1 MUX (INV)
01E 19-063 SDFF
02E 19-063 SDFF
01F 19-063 SDFF
02F 19-063 SDFF
13H 19-060 SG
00D 19-057 SG
00F 19-058 SG
01D 19-062 SG
02D 19-062 SG
03C 19-071 HDFF
04C 19-071 HDFF
05C 19-071 HDFF
06C 19-071 HDFF
LCC1 202-1 202-F
ST151 9G1
GCC1 102-1 102-F
ST141 9E1
VCC1 237-0 237-E
ST131 9N1
CCC1 238-0 238-F
ST121 9N1
SPSW1 10D9
MUDR111 8K9
MUDR101 8K9
MUDR091 8J9
MUDR081 8J9
REGWTIB 1F5
SSEL041 10B9
SSEL030 10C9
SSEL021 10E9
SSEL011 10F9
SSEL001 10H9
D1 10L9
STRBO 1K2
STRB1A 8A1
P5 08TR1 470
P5 08TR2 470
P5 09TR1 470
P5 08TR3 470
PD151
PD141
PD131
PD121
DUDR110
DUDR100
DUDR090
DUDR080
UDR111 10A9, 3A8, 5G5
UDR110 6A5
UDR101 10C9, 3A8, 5J5
UDR100 6B5
UDR091 10D4, 3A8, 5K5
UDR090 6D5
UDR081 10A9, 3A7, 5L5
UDR080 6E5
00FR6 1K P5
ENFL01 10L9
MUSR151 8A9
MUSR141 8N9
MUSR131 8M9
MUSR121 8M9
USRCK0
XRPC 10M9
USR150 5B1
USR151 5A5
USR140 5B1
USR141 5C5
USR130 5B1
USR131 5D5
USR120 5B1
USR121 5E5
01FR5 1K P5
239-0 SCCO
239-E
07TR1 330 P5
REGWTIB
STRB1A
SPSW1
NC
ST111 9N1
ST101 9M1
ST091 9L1
ST081 9L1
ST071 9G1
ST061 9K1
ST051 9J1
ST041 9J1
ST031 9H1
ST021 9H1
ST011 9G1
ST001 9F1
CLK D C Q
PSW150 102-C 6B5
PSW151 3A8
PSW140 101-C 6C5
PSW141 3A8
PSW130 6E5
PSW131 3A7
PSW120 100-C 6F5
PSW121 3A7
PSW110 6H5
PSW100 6J5
PSW101 3H3
PSW090 6L5
PSW091 3H2
PSW080 6L5
PSW070 6B1
PSW071 3K1
PSW060 6C1
PSW050 6E1
PSW040 6F1
PSW030 6H1
PSW020 6J1
PSW021 3H4
PSW010 6L1
PSW011 3H2
PSW000 6M1
A B C D E F G H J K L M N R S
1 2 3 4 5 6 7 8 9

NOTES

NAME	TITLE	DATE
E. ROE	DRAFT	5-26-72
✓	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC

MODEL 80 CPU

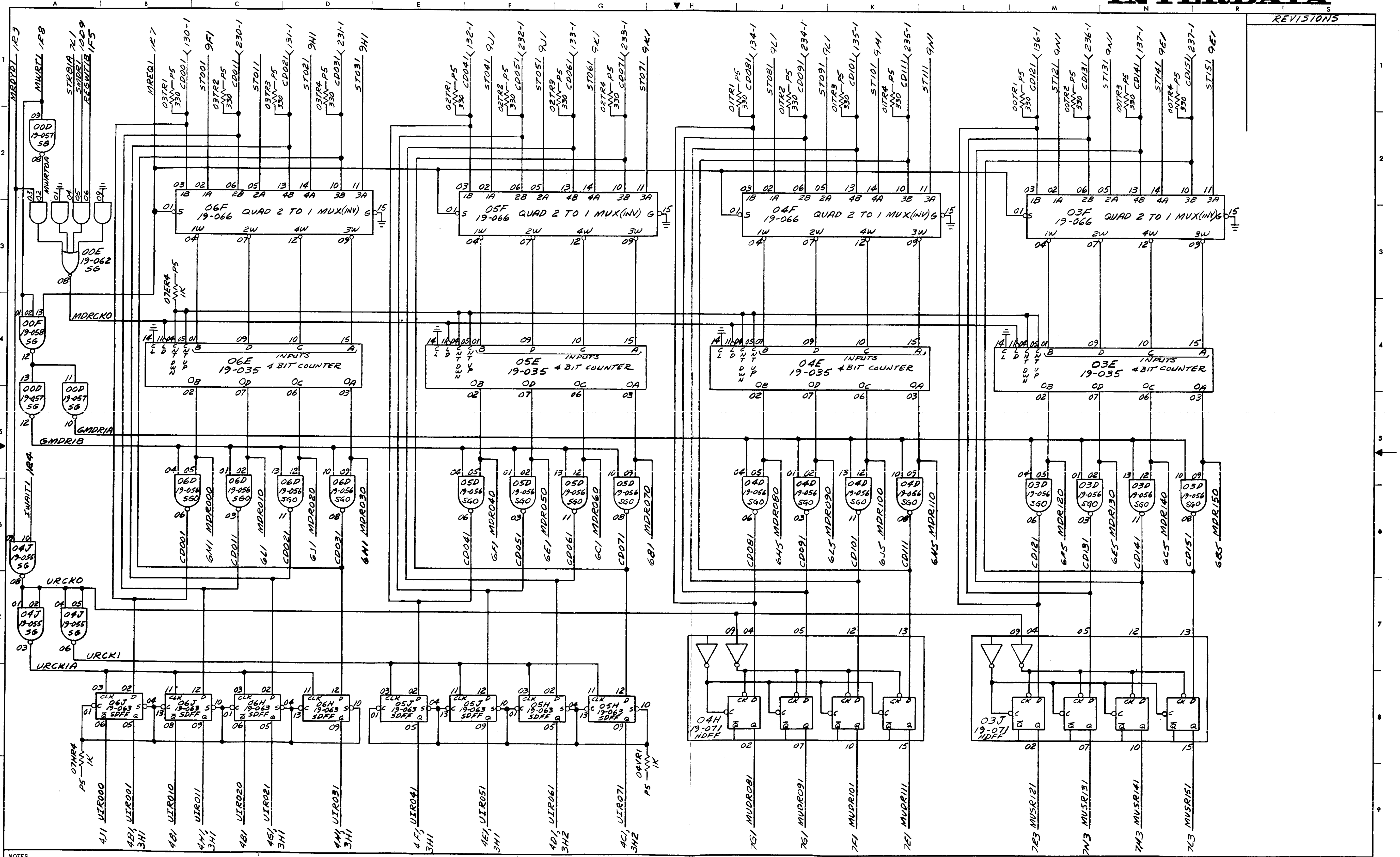
TASK NO. 03215

DWG NO. 35-403 R03 D08

SHEET 7 OF 10

BRUNING 44-231 18042

INTERDATA®


REVISIONS
MRDY01 1R3
MWRT1 1P8
STRBIA 7L1
SMDR1 10D9
REGWT1B 1F5
MREQ1 1R7
00D 19-057 SG
MWRTOA
00E 19-062 SG
MDRCK0
00F 19-058 SG
GMDR1A
GMDR1B
IWAIT1 1R4
04J 19-055 SG
URCK0
URCK1
URCK1A
06F 19-066 QUAD 2 TO 1 MUX(INV)
05F 19-066 QUAD 2 TO 1 MUX(INV)
04F 19-066 QUAD 2 TO 1 MUX(INV)
03F 19-066 QUAD 2 TO 1 MUX(INV)
06E 19-035 4 BIT COUNTER
05E 19-035 4 BIT COUNTER
04E 19-035 4 BIT COUNTER
03E 19-035 4 BIT COUNTER
INPUTS
07ER4 P5 1K
06D 19-056 SG0
05D 19-056 SG0
04D 19-056 SG0
03D 19-056 SG0
CD001 6M1 MDR000
CD011 6L1 MDR010
CD021 6J1 MDR020
CD031 6H1 MDR030
CD041 6F1 MDR040
CD051 6E1 MDR050
CD061 6C1 MDR060
CD071 6B1 MDR070
CD081 6H5 MDR080
CD091 6L5 MDR090
CD101 6J5 MDR100
CD111 6K5 MDR110
CD121 6A5 MDR120
CD131 6E5 MDR130
CD141 6C5 MDR140
CD151 6B5 MDR150
06J 19-063 SDFF
06H 19-063 SDFF
05J 19-063 SDFF
05H 19-063 SDFF
04H 19-071 HDFF
03J 19-071 HDFF
07HR4 P5 1K
04VR1 P5 1K
UIR000 4J1
UIR001 4B1, 3H1
UIR010 4B1
UIR011 4H1, 3H1
UIR020 4B1
UIR021 4G1, 3H1
UIR031 4H1, 3H1
UIR041 4F1, 3H1
UIR051 4E1, 3H1
UIR061 4D1, 3H2
UIR071 4C1, 3H2
MUDR081 7G1
MUDR091 7G1
MUDR101 7F1
MUDR111 7E1
MUSR121 7R3
MUSR131 7N3
MUSR141 7M3
MUSR151 7L3

NOTES

NAME		DATE
TITLE		
DRAFT		
CHK		
ENGR		
DIR ENG		

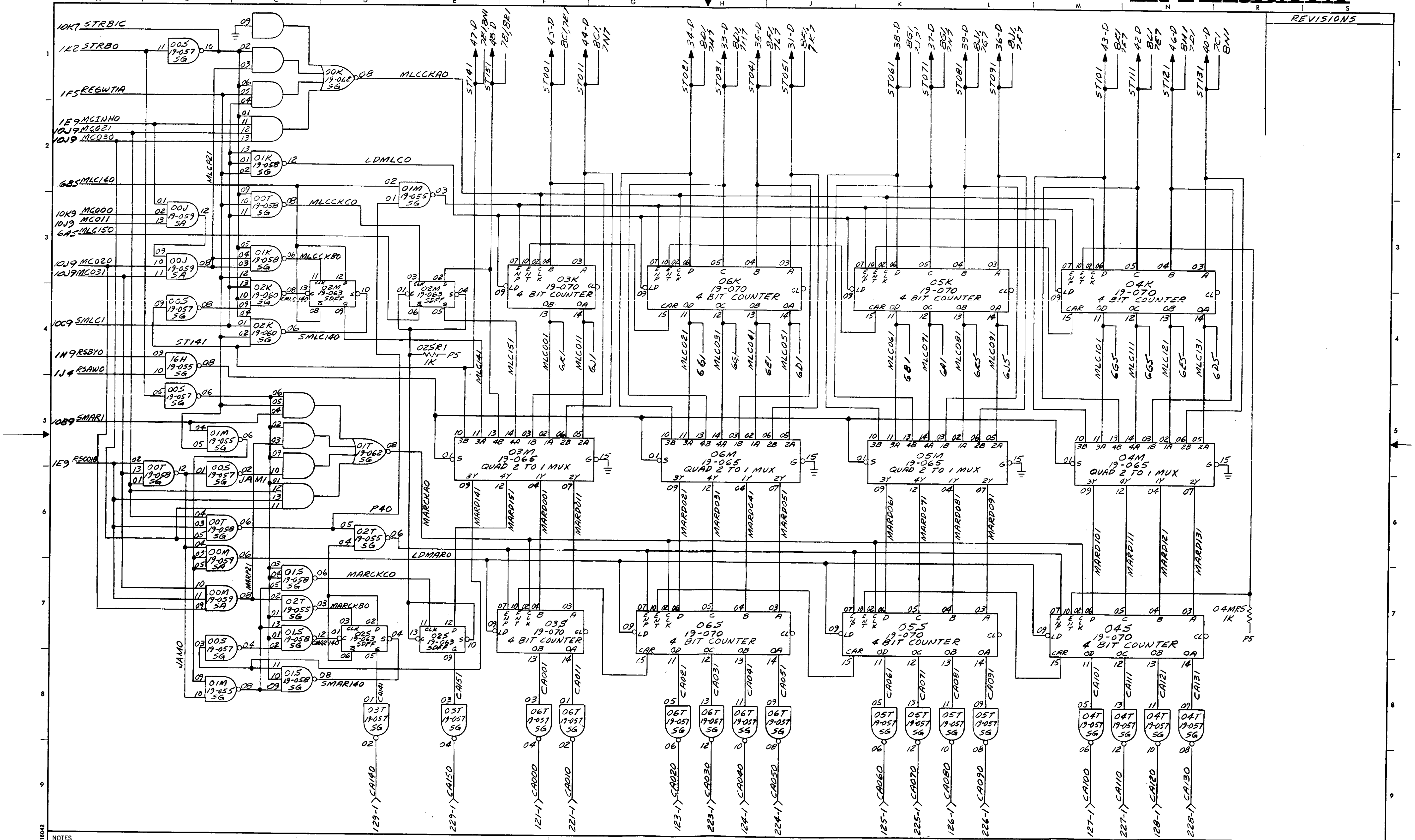
TITLE FUNCTIONAL SCHEMATIC
MODEL 80 CPU

TASK NO 03215
DWG NO 35-403 R03 D08
SHEET 8 OF 10

BRUNING 44-231 16042

INTERDATA®

REVISIONS



10K7 STRBIC
1K2 STRBO
1F5 REGWTIA
1E9 MCINHO
10J9 MC021
10J9 MC030
6B5 MLC140
10K9 MC000
10J9 MC011
6A5 MLC150
10J9 MC020
10J9 MC031
10C9 SMLC1
1H9 RSBYO
1J4 RSAWO
10B9 SMAR1
1E9 RS001B
00S 19-057 SG
00K 19-062 SG
MLCCKAO
01K 19-058 SG
LDMLCO
00T 19-058 SG
MLCCKCO
00J 19-059 SA
01M 19-055 SG
02K 19-060 SG
02M 19-063 SDFF
MLCCKBO
SMLC140
MLCP21
ST141
16H 19-055 SG
02SR1 1K P5
01T 19-062 SG
01S 19-058 SG
02T 19-055 SG
00M 19-059 SA
P40
LDMARO
MARCKCO
MARCKBO
MARCKAO
02S 19-063 SDFF
SMAR140
JAM0
JAM1
MARP21
03K 19-070 4 BIT COUNTER
06K 19-070 4 BIT COUNTER
05K 19-070 4 BIT COUNTER
04K 19-070 4 BIT COUNTER
03M 19-065 QUAD 2 TO 1 MUX
06M 19-065 QUAD 2 TO 1 MUX
05M 19-065 QUAD 2 TO 1 MUX
04M 19-065 QUAD 2 TO 1 MUX
03S 19-070 4 BIT COUNTER
06S 19-070 4 BIT COUNTER
05S 19-070 4 BIT COUNTER
04S 19-070 4 BIT COUNTER
04MR5 1K P5
ST141 47-D 7F/8N1
ST151 48-D 7B/8R1
ST001 45-D 8C/7E7
ST011 44-D 8C/7N7
ST021 34-D 8D/7H7
ST031 33-D 8D/7J7
ST041 35-D 8E/7L7
ST051 31-D 8F/7K7
ST061 38-D 8G/7J7
ST071 37-D 8G/7A7
ST081 39-D 8J/7G7
ST091 36-D 8J/7F7
ST101 43-D 8K/7K7
ST111 42-D 8L/7E7
ST121 46-D 8M/7D1
ST131 40-D 7C/8N1
MLC151 MLC141 MLC001 MLC011 6K1 6J1
MLC021 MLC031 MLC041 MLC051 6G1 6J1 6E1 6D1
MLC061 MLC071 MLC081 MLC091 6B1 6A1 6K5 6J5
MLC101 MLC111 MLC121 MLC131 6G5 6G5 6E5 6D5
MARD141 MARD151 MARD001 MARD011
MARD021 MARD031 MARD041 MARD051
MARD061 MARD071 MARD081 MARD091
MARD101 MARD111 MARD121 MARD131
CA141 CA151 CA001 CA011 CA021 CA031 CA041 CA051
CA061 CA071 CA081 CA091 CA101 CA111 CA121 CA131
03T 19-057 SG
06T 19-057 SG
05T 19-057 SG
04T 19-057 SG
CA140 129-1
CA150 229-1
CA000 121-1
CA010 221-1
CA020 123-1
CA030 223-1
CA040 124-1
CA050 224-1
CA060 125-1
CA070 225-1
CA080 126-1
CA090 226-1
CA100 127-1
CA110 227-1
CA120 128-1
CA130 228-1

NOTES

NAME	TITLE	DATE
	DRAFT	
Z	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 80 CPU

TASK NO. 03215
DWG NO. 35-403 R03 D08
SHEET 9 OF 10

BRUNING 44-231 18042

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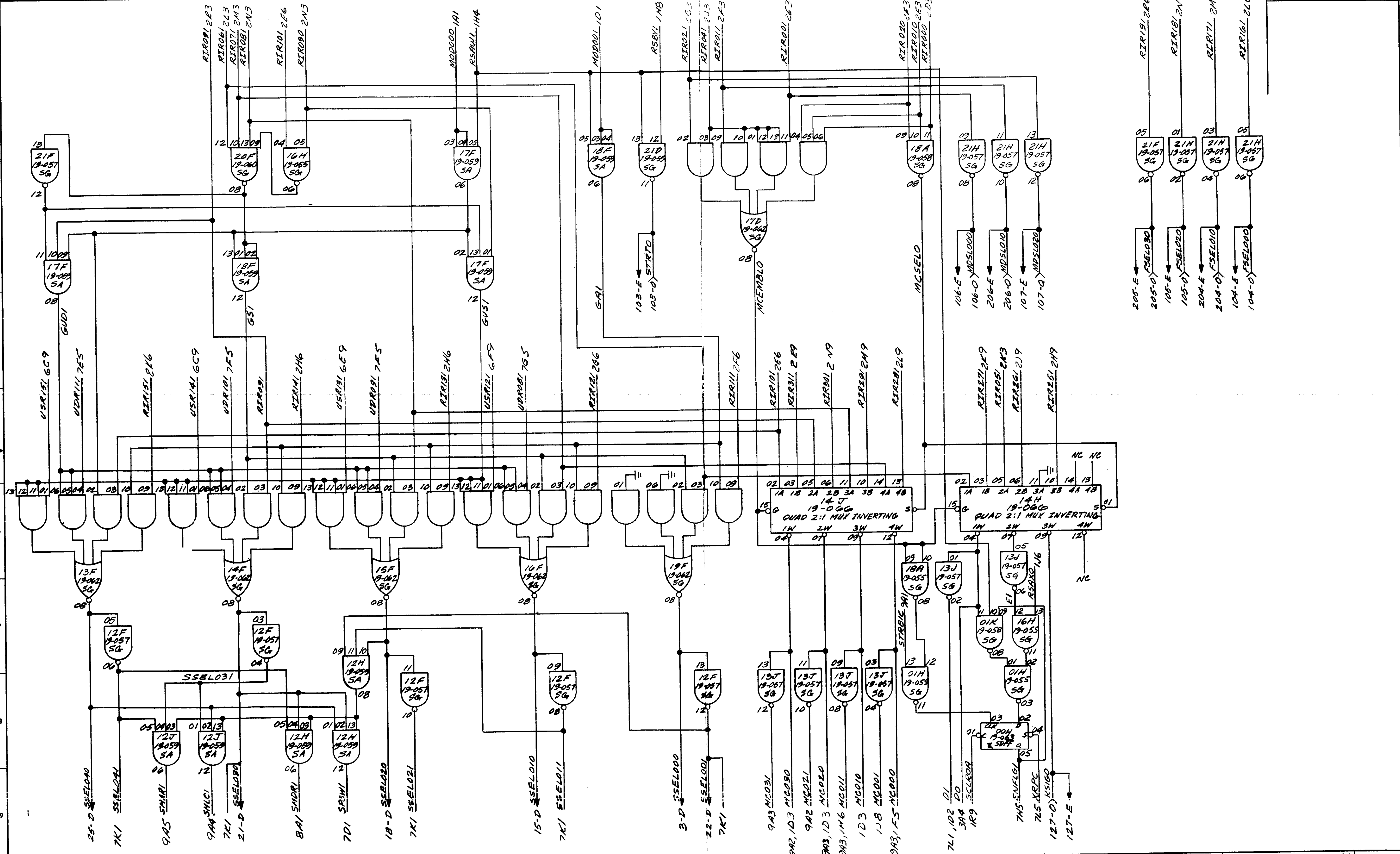

RIR081 2E3
RIR061 2E3
RIR071 2H3
RIR081 2N3
RIR101 2E6
RIR090 2N3
MOD000 1A1
RSAU1 1H4
MOD001 1D1
RSBY1 1H8
RIR021 2E3
RIR041 2J3
RIR011 2F3
RIR001 2E3
RIR020 2E3
RIR010 2E3
RIR000 2D3
RIR191 2R6
RIR181 2N6
RIR171 2M6
RIR161 2L6
21F 19-057 5G
20F 19-060 5G
16H 19-055 5G
17F 19-059 5A
18F 19-059 5A
21D 19-055 5G
17D 19-062 5G
18A 19-058 5G
21H 19-057 5G
GUD1
GS1
GUS1
GA1
STRT0
103-E
103-0
MCEMBL0
MCSEL0
MDSL000
MDSL010
MDSL020
106-E
106-0
206-E
206-0
107-E
107-0
FSEL030
FSEL020
FSEL010
FSEL000
205-E
205-0
105-E
105-0
204-E
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104-E
104-0
USR151 6C9
UDR111 7E5
RIR151 2H6
USR141 6C9
UDR101 7F5
RIR091
RIR141 2H6
USR131 6E9
UDR091 7F5
RIR131 2H6
USR121 6F9
UDR081 7G5
RIR121 2G6
RIR111 2F6
RIR101 2E6
RIR311 2E9
RIR301 2N9
RIR291 2H9
RIR281 2L9
RIR271 2K9
RIR051 2K3
RIR261 2J9
RIR251 2H9
14J 19-066 QUAD 2:1 MUX INVERTING
14H 19-066 QUAD 2:1 MUX INVERTING
1A 1B 2A 2B 3A 3B 4A 4B
1W 2W 3W 4W
G S
NC
13F 19-062 5G
14F 19-062 5G
15F 19-062 5G
16F 19-062 5G
19F 19-062 5G
12F 19-057 5G
12H 19-059 5A
12J 19-059 5A
SSEL031
18A 19-055 5G
13J 19-057 5G
13J 19-057 5G
01K 19-058 5G
16H 19-055 5G
01H 19-055 5G
00H 19-063 SDFF
STRBIG
RSAU0 1H6
SSEL040
SSEL041
SMAR1
SMLC1
SSEL030
SMDR1
SPSW1
SSEL020
SSEL021
SSEL010
SSEL011
SSEL000
SSEL001
MC031
MC030
MC021
MC020
MC011
MC010
MC001
MC000
SCLR0A
SWENFLG1
XRPC
KSIG0
25-D
7K1
9A5
9A4,5HC1
7K1
21-D
8A1
7D1
18-D
7K1
15-D
7K1
3-D
22-D
7K1
9A3,1D3
9A2,1D3
9A2
9A3,1D3
9A3,1H6
1D3
1J8
9A3,F5
7L1,1D2
3A4
1R9
7H5
7L5
127-0
127-E

REVISIONS

NOTES

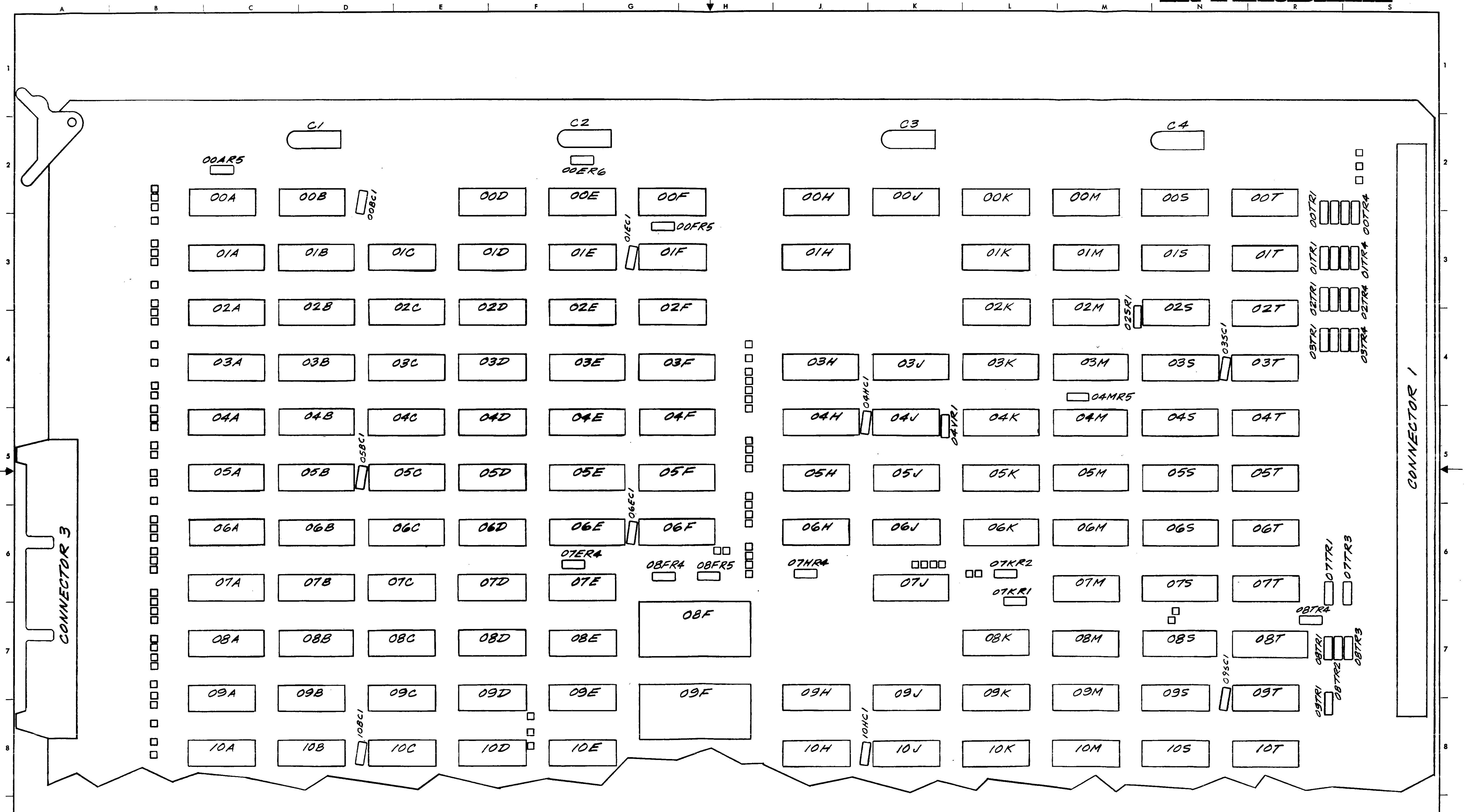
NAME	TITLE	DATE
E ROE	DRAFT	5-25-72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 80 CPU

TASK NO. 02315
DWG NO. 35-403 R03 D08
SHEET 10 OF 10

BRUNING 44-231 16042

INTERDATA®


A B C D E F G H J K L M N R S
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C1
C2
C3
C4
00AR5
00ER6
00A
00B
00BC1
00D
00E
00F
00FR5
00H
00J
00K
00M
00S
00T
00TR1
00TR4
01EC1
01A
01B
01C
01D
01E
01F
01H
01K
01M
01S
01T
01TR1
01TR4
02A
02B
02C
02D
02E
02F
02K
02M
02SR1
02S
02T
02TR1
02TR4
03A
03B
03C
03D
03E
03F
03H
03J
03K
03M
03S
03SC1
03T
03TR1
03TR4
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04B
04C
04D
04E
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04M
04S
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05H
05J
05K
05M
05S
05T
06EC1
06A
06B
06C
06D
06E
06F
06H
06J
06K
06M
06S
06T
07ER4
08FR4
08FR5
07HR4
07KR2
07KR1
07TR1
07TR3
07A
07B
07C
07D
07E
07J
07M
07S
07T
08F
08TR4
08A
08B
08C
08D
08E
08K
08M
08S
08T
08TR1
08TR2
08TR3
09SC1
09A
09B
09C
09D
09E
09F
09H
09J
09K
09M
09S
09T
09TR1
10BC1
10HC1
10A
10B
10C
10D
10E
10H
10J
10K
10M
10S
10T
CONNECTOR 1
CONNECTOR 3

NOTES

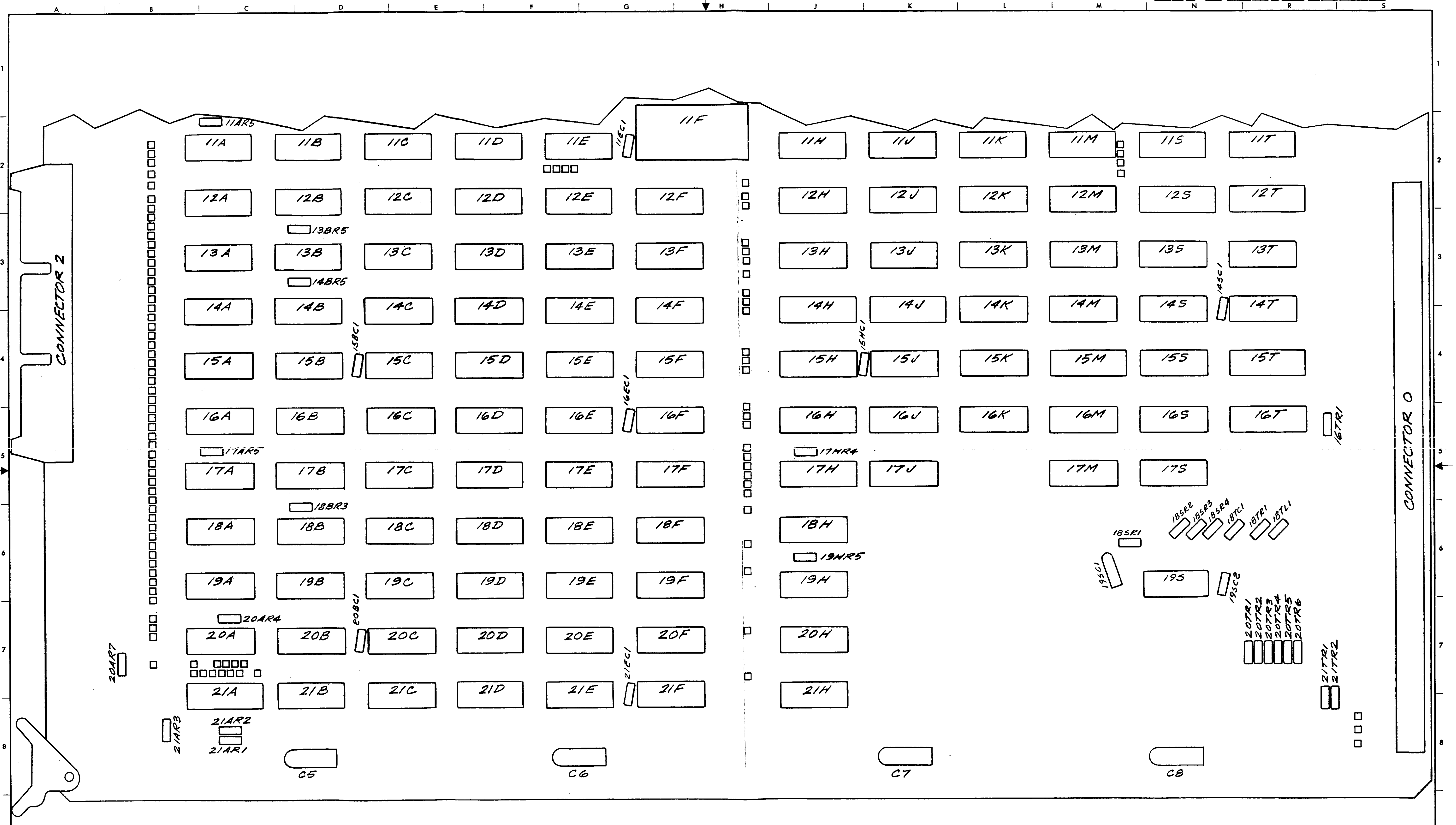
NAME	TITLE	DATE	TITLE
E. ROE	DRAFT	6-28-73	FUNCTIONAL SCHEMATIC COMPONENT LOCATER
	CHK		
	ENGR		
			TASK NO. 03215
	DIR ENG		DWG NO. 35-403 008

SHEET OF 11 - 12

A B C D E F G H J K L M N R S

BRUNING 44-231 16042

INTERDATA®



A B C D E F G H J K L M N R S
1 2 3 4 5 6 7 8 9
11AR5
11A 11B 11C 11D 11E 11EC1 11F 11H 11J 11K 11M 11S 11T
12A 12B 12C 12D 12E 12F 12H 12J 12K 12M 12S 12T
13BR5
13A 13B 13C 13D 13E 13F 13H 13J 13K 13M 13S 13T
14BR5
14A 14B 14C 14D 14E 14F 14H 14J 14K 14M 14S 14T
14SC1
15BC1 15HC1
15A 15B 15C 15D 15E 15F 15H 15J 15K 15M 15S 15T
16EC1
16A 16B 16C 16D 16E 16F 16H 16J 16K 16M 16S 16T
16TR1
17AR5 17MR4
17A 17B 17C 17D 17E 17F 17H 17J 17M 17S
18BR3
18A 18B 18C 18D 18E 18F 18H
18SR2 18SR3 18SR4 18TC1 18TR1 18TL1
18SR1
19MR5
19A 19B 19C 19D 19E 19F 19H
19SC1 19S 19SC2
20AR4 20BC1
20A 20B 20C 20D 20E 20F 20H
20TR1 20TR2 20TR3 20TR4 20TR5 20TR6
20AR7
21EC1
21TR1 21TR2
21A 21B 21C 21D 21E 21F 21H
21AR2
21AR3
21AR1
C5 C6 C7 C8
CONNECTOR 2
CONNECTOR 0

BRUNING 44-231 16042

NOTES

NAME	TITLE	DATE	TITLE
E. ROE	DRAFT	6-30-73	FUNCTIONAL SCHEMATIC COMPONENT LOCATER
	CHK		
	ENGR		
			TASK NO. 03215
	DIR ENG		DWG NO. 35-403 008

SHEET OF 12-12

A B C D E F G H J K L M N R S

INTERDATA®

CONN.	SHEET LOCATION	MNEMONIC (ROW 2)	TERM NO.	MNEMONIC (ROW 1)	SHEET LOCATION	CONN.
F			41			F
			40			
			39			
			38			
			37			
			36			
			35			
			34			
			33			
			32			
			31			
			30			
			29			
			28			
			27			
			26			
			25			
			24			
			23			
			22			
			21			
			20			
		CWRTO	19	CRDYO		
	2M6	A150	18	A140	2N6	
	2L6	A130	17	A120	2K6	
	2F6	A110	16	A100	2G6	
	2E6	A090	15	A080	2D6	
	1M6	A070	14	A060	1N6	
	1L6	A050	13	A040	1K6	
	1F6	A030	12	A020	1G6	
	1E6	A010	11	A000	1D6	
	5N6	S150	10	S140	5N6	
	5M6	S130	09	S120	5M6	
	5L6	S110	08	S100	5K6	
	5K6	S090	07	S080	5J6	
	5J6	S070	06	S060	5H6	
	5H6	S050	05	S040	5G6	
	5G6	S030	04	S020	5F6	
	5F6	S010	03	S000	5E6	
	6A1	LCC1	02	GCC1	6B1	
			01			
			00			

CONN.	SHEET LOCATION	MNEMONIC (ROW 2)	TERM NO.	MNEMONIC (ROW 1)	SHEET LOCATION	CONN.
E			41			E
			40			
	7N9	SCCO	39			
	6B1	CCC1	38			
	6G9	VCC1	37			
			36			
	4C6	B150	35	B140	4D6	
	4B6	B130	34	B120	4A6	
	3M6	B110	33	B100	3M6	
	3K6	B090	32	B080	3K6	
	3G6	B070	31	B060	3H6	
	3F6	B050	30	B040	3E6	
	3C6	B030	29	B020	3D6	
	3B6	B010	28	B000	3A6	
			27	KSIGO	6K7	
			26			
			25			
			24			
			23			
			22			
			21			
			20			
			19			
			18			
			17			
			16			
			15			
			14			
			13			
			12			
			11			
			10			
			09			
			08			
	7N9	MSIGO	07	MDSL020	7N1	
	7N1	MDSL010	06	MDSL000	7N1	
	5F1	FSEL030	05	FSEL020	6J7	
	5E1	FSEL010	04	FSEL000	6C1	
	7N9	MFINO	03	STRTO	5F1	
			02			
			01			
			00			

CONNECTOR D

	MNEMONIC	SHEET LOCATION
48	ST151	5N9
47	ST141	5N9
46	ST121	5M9
45	ST001	5E9
44	ST011	5F9
43	ST101	5L9
42	ST111	5L9
41	NOT USED	—
40	ST131	5M9
39	ST081	5K9
38	ST061	5H9
37	ST071	5J9
36	ST091	5K9
35	ST041	5G9
34	ST021	5F9
33	ST031	5G9
32	GND	—
31	ST051	5H9
30	RGLO	3H7
29	RGHO	3A7
28	BSEL001	8F5
27	ASEL001	8C5
26	ASEL000	8A5
25	SSEL040	8L5
24	BSEL040	8L5
23	ASEL040	8K5
22	SSEL001	8C5
21	SSEL030	8K5
20	BSEL030	8K5
19	ASEL030	8J5
18	SSEL020	8J5
17	BSEL020	8J5
16	ASEL020	8J5
15	SSEL010	8H5
14	BSEL010	8F5
13	ASEL010	8C5
12	BSEL000	8D5
11	VFLG1	6H9
10	CFLG1	6B9
09	ZFLG1	6B9
08	LFLG1	6B9
07	GFLG1	6B9
06	RSAY1	8B5
05	GND	—
04	NOT USED	—
03	SSEL000	8A5
02	RSBY1	4M8
01	REGWRTO	8H5

CONNECTOR C

	MNEMONIC	SHEET LOCATION
63	—	NOT USED
62	4M5	CRLR040
	4N6	CRLR110
	4M5	CRLR050
	4M6	CRLR060
	4M6	CRLR070
	9A7	RAG151
	9A6	RAG141
55	9A6	RAG131
	9A5	RAG121
	9A5	RAG111
	9A3	RAG081
	9A4	RAG091
50	9A4	RAG101
	9A3	RAG071
	9A3	RAG061
	9A2	RAG051
	9A1	RAG041
45	3A7	RD161
	3B7	RD171
	3C7	RD181
	3D7	RD191
	4A7	RD121
40	4B7	RD131
	4C7	RD141
	4D7	RD151
	3K7	RD081
	3L7	RD091
35	3M7	RD101
	3N7	RD111
	3F7	RD041
	3G7	RD051
	3G7	RD061
30	3H7	RD071
	3A7	RD001
	3B7	RD011
	3C7	RD021
	3D7	RD031
25	—	GND
	3A7	RD281
	4B7	RD291
	4C7	RD301
	4D7	RD311
20	3K7	RD241
	3L7	RD251
	3L7	RD261
	3M7	RD271
	3E7	RD201
15	3F7	RD211
	3G7	RD221
	3H7	RD231
	—	GND
	8R1	STRBO
10	4M8	LDRLRO
	4M7	INHCLBO
	—	NOT USED
	—	NOT USED
	8A5	RS001
05	—	GND
	—	GND
	—	GND
	—	GND
01	—	NOT USED

CONNECTOR C

MNEMONIC	SHEET LOCATION	
BLCH140	4C9	106
BLCH120	4A9	
BLCH150	4D9	
BLCH130	4B9	
PSW150	6G7	
PSW140	6G7	
PSW120	5D1	100
BLCH080	3J9	
BLCH100	3L9	
BLCH090	3K9	
BLCH110	3M9	
ALCH140	2N7	95
ALCH120	2L7	
ALCH130	2L7	
ALCH150	2N7	
ALCH100	2G7	
ALCH080	2E7	90
ALCH110	2H7	
ALCH090	2E7	
ALCH040	1L7	
ALCH060	1N7	
ALCH070	1R7	85
ALCH050	1L7	
ALCH020	1G7	
ALCH000	1E7	
ALCH030	1H7	
ALCH010	1E7	80
BLCH000	3A9	
BLCH020	3C9	
BLCH030	3D9	
GND	—	
BLCH010	3B9	75
BLCH040	3E9	
BLCH060	3G9	
BLCH070	3H9	
BLCH050	3F9	
CRLR120	4M7	70
CRLR130	4M7	
CRLR140	4M7	
CRLR150	4M7	
CRLR080	4M6	
CRLR090	4M6	
CRLR100	4M6	64

SHEET LOCATION	ROW 1	TERM NO.	ROW 2	SHEET LOCATION
4N8	GND	24	GND	4N9
4N8	GND	23	GND	4N8
8R1	ACLRO	22	ACNT021	8D4
8D4	ACNT011	21	ACNT001	8D4
8E4	ACNT031	20	EACNT1	8G2
8A6	RSA1	19	INHACKO	7L1
6R5	ASA1	18	ASB1	6R5
6A8	GFLG1	17	CFLG1	6A8
4N8	RSBY1	16	VFLG1	6H9
6A8	LFLG1	15	INHCLBO	4N7
4N8	LDRLRO	14	STRBO	8N1
5R8	ST151	13	ST141	5N8
5M8	ST131	12	ST121	5M8
5L8	ST111	11	ST101	5L8
5K8	ST091	10	ST081	5K8
5J8	ST071	09	ST061	5J8
5H8	ST051	08	ST041	5H8
5G8	ST031	07	ST021	5F8
5F8	ST011	06	ST001	5E8
4N7	CRLR120	05	CRLR130	4N7
4N7	CRLR140	04	CRLR150	4N7
4N6	CRLR080	03	CRLR090	4N6
4N6	CRLR100	02	CRLR040	4N5
4N6	CRLR110	01	CRLR050	4N5
4N6	CRLR060	00	CRLR070	4N6
	ROW 1		ROW 2	

CONNECTOR 2

REVISIONS

REDRAWN FROM LAYOUT; ADDED - SH 0 & INCLUDED ALL CHANGES PER ECR 3215-04 & -10					
7		3215-04 3215-10		7-7-72 7-19-72	R01
REVISED SHEET 7.					
7		3215-15		8-24-72	R02
REVISED SHEETS 1, 6 & 7					
7		3215-22		10-11-72	R03
REVISED SHEET 9					
PE		3215-26		11-22-72	R04
REVISED SHEETS 5 & 6					
PE		3215-30		1-10-73	R05
REVISED SHTS 6 & 7					
7		3215-39		3-16-73	R06

NOTE: THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION:

35-404R07

SHEET INDEX										
REV. LEVEL	6	3	1	1	1	5	6	6	1	4
SHEET NO.	0	1	2	3	4	5	6	7	8	9

NOTES 1. ALL C, D, E & F CONNECTORS ARE DIRECT CONTACTS TO THE CPU BOARD, SEE SCHEMATIC 35-403D08.

NAME	TITLE	DATE
D. BARKER	DRAFT	6-29-72
J.F. FLEMING	CHK	10-9-72
S. MESSINA	ENGR	
R.E. JONES	DIR ENG	

TITLE MODEL 80 ALU CONNECTOR MAP

TASK NO. 03215

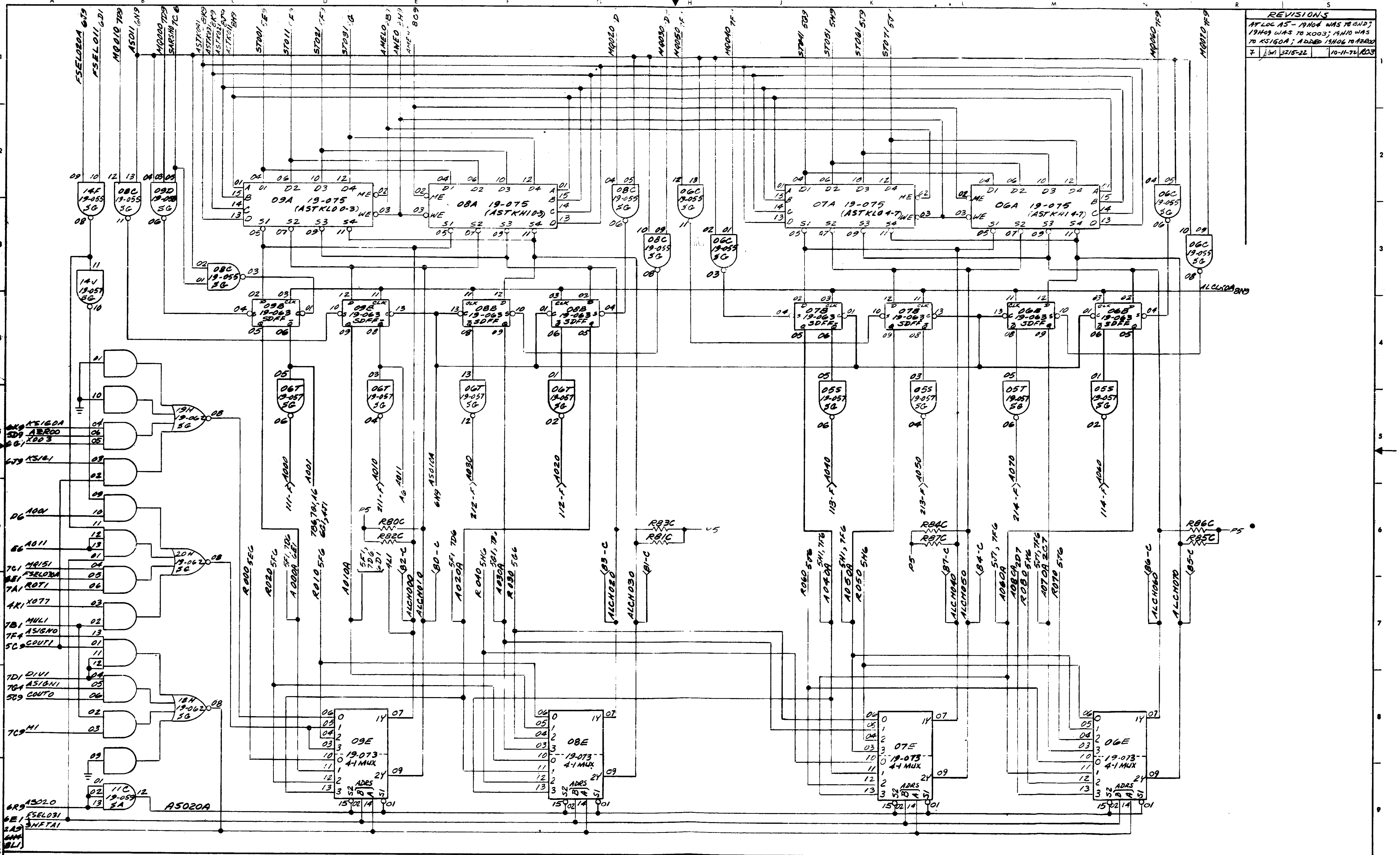
DWG NO. 35-404R06D08

SHEET 0 OF 10

BRUNING 44-231 16042

INTERDATA®

REVISIONS					
AT LOC A5 – 19H04 WAS TO GND; 19H09 WAS TO X003; 19H10 WAS TO KS1G0A; ADDED 19H06 TO AZR00					
7	JWM	3215-22		10-11-72	R03



FSEL020A 6J9
FSEL011 6D1
MQ010 7F9
AS011 6N9
MQ000 7D9
SARSH1 7C6
ASTKL01
ASTKL0
ASTKH01
ASTKH0
ST001
ST011
ST021
ST031
AMELO
AMEO
AMEN
MQ020
MQ030
MQ050
MQ040
ST041 5G9
ST051 5H9
ST061 5I9
ST071 5I9
MQ060 7F9
MQ070 7F9
14F 19-055 SG
08C 19-055 SG
09D 19-055 SG
09A 19-075 (ASTKL0 0-3)
08A 19-075 (ASTKH1 0-3)
07A 19-075 (ASTKL0 4-7)
06A 19-075 (ASTKH1 4-7)
ME
WE
D1 D2 D3 D4
S1 S2 S3 S4
08C 19-055 SG
06C 19-055 SG
14V 19-057 SG
09B 19-063 SDFF
09E 19-063 SDFF
08B 19-063 SDFF
07B 19-063 SDFF
06B 19-063 SDFF
CLK
06T 19-057 SG
05S 19-057 SG
05T 19-057 SG
ALCLK0A 8N9
19H 19-062 SG
20H 19-062 SG
18H 19-062 SG
11C 19-059 SA
KS1G0A 4K9
AZR00 5D9
X003 5G1
KS1G1 6J9
A00N D6
A011 E6
MQ1S1 7C1
FSEL02A 8E1
ROT1 7A1
X077 4K1
MUL1 7B1
ASIGN0 7F4
COUT1 5C9
DIV1 7D1
ASIGN1 7G1
COUT0 5C9
M1 7C9
AS020 6R9
AS020A
FSEL031 6E1
SHFTA1 2A9
A000 111-F
A001 7B6, 7D1, 1G 6G1, 4A1
A010 211-F
A011
AS010A 6N9
A030 212-F
A020 112-F
A040 113-F
A050 213-F
A070 214-F
A060 114-F
R80C
R82C
R83C
R81C
R84C
R87C
R86C
R85C
P5
R000 5EG
R020 5FG
A000A
R010 5FG
A010A
ALCH000
ALCH010
A020A
R040 5H6
A030A
R030 5G6
ALCH020
ALCH030
R060 5H6
A040A
A050A
R050 5H6
ALCH040
ALCH050
A060A
R080
A070A
R070 5F6
ALCH060
ALCH070
09E 19-073 4-1 MUX
08E 19-073 4-1 MUX
07E 19-073 4-1 MUX
06E 19-073 4-1 MUX
1Y
2Y
ADRS
S2 B A S1

NOTES

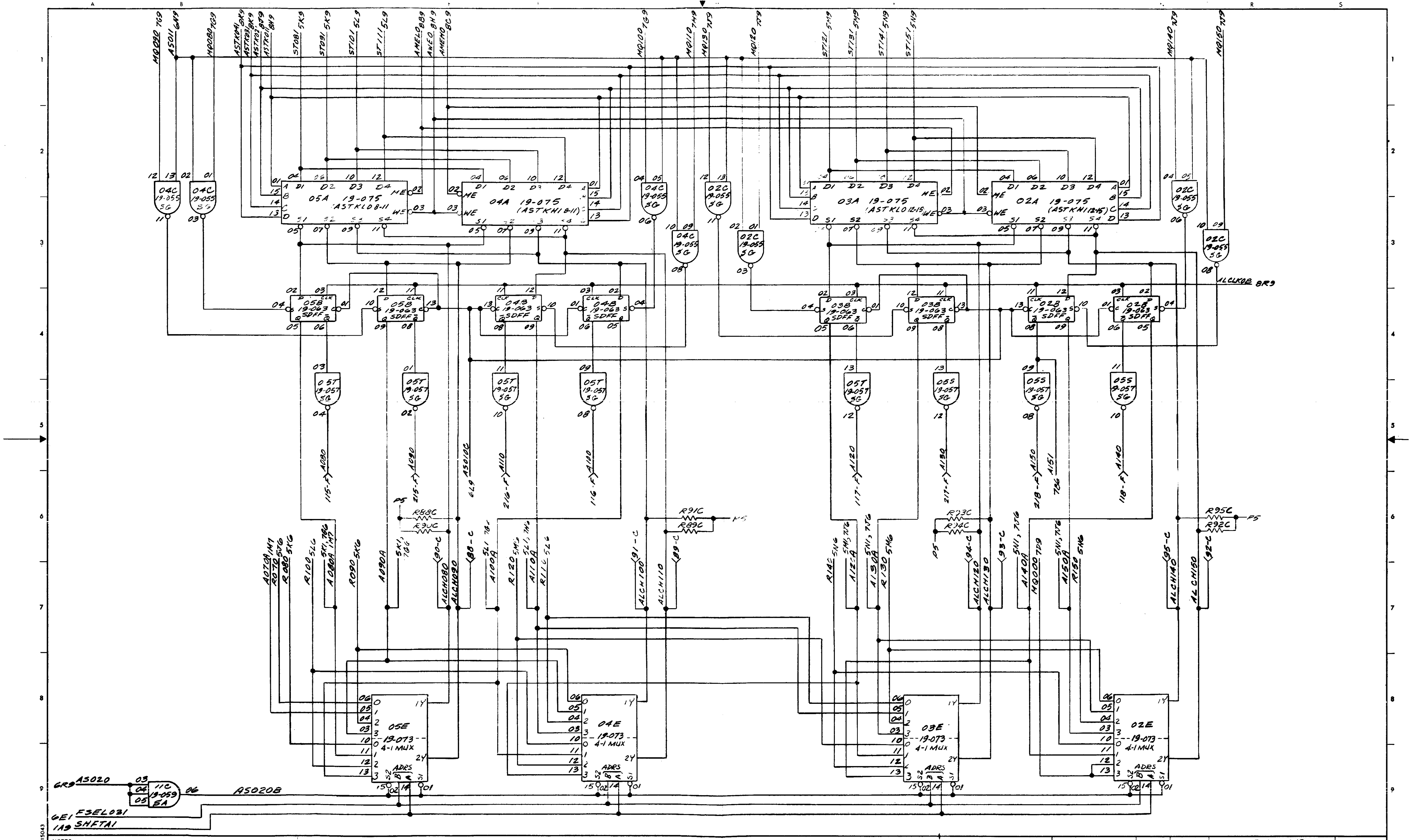
1. ALL RESISTORS 330Ω.

NAME	TITLE	DATE
E ROE	DRAFT	4-14-72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 80 ALU

TASK NO. 03215
DWG NO. 35-404 R03008
SHEET 1 OF

INTERDATA



05A 19-075 ASTKL08-11
04A 19-075 ASTKHI8-11
03A 19-075 ASTKL012-15
02A 19-075 ASTKHI12-15
04C 19-055 SG
02C 19-055 SG
05B 19-063 SDFF
04B 19-063 SDFF
03B 19-063 SDFF
02B 19-063 SDFF
05T 19-057 SG
05S 19-057 SG
05E 19-073 4-1 MUX
04E 19-073 4-1 MUX
03E 19-073 4-1 MUX
02E 19-073 4-1 MUX
ADRS
MQ090 7G9
AS011 6H9
MQ080 7G9
ASTKHI
ASTKL0
ST081 5K9
ST101 5L9
ST111 5L9
AMEL0 8B9
AMEHI 8H9
MQ100 7G9
MQ110 7H9
MQ130 7J9
MQ120 7J9
ST121 5M9
ST131 5M9
ST141 5N9
ST151 5N9
MQ140 7Q9
MQ150 7Q9
ALCLK0B 8R9
A080 115-F
A090 215-F
AS010C 6L9
A110 216-F
A100 116-F
A120 117-F
A130 217-F
A150 218-F
A151 7G6
A140 118-F
P5
R88C
R90C
R91C
R89C
R93C
R94C
R95C
R92C
90-C
88-C
91-C
89-C
94-C
93-C
95-C
92-C
ALCH080
ALCH090
ALCH100
ALCH110
ALCH120
ALCH130
ALCH140
ALCH150
A070
R070
R080
R100
A080
R090
A090A
A120A
R120
A110A
R110
A130A
R130
R140
A140A
MQ000 7D9
A150A
R150
GR9 AS020
11C 19-059 6A
AS020B
6E1 FSEL031
1A9 SHFTA1

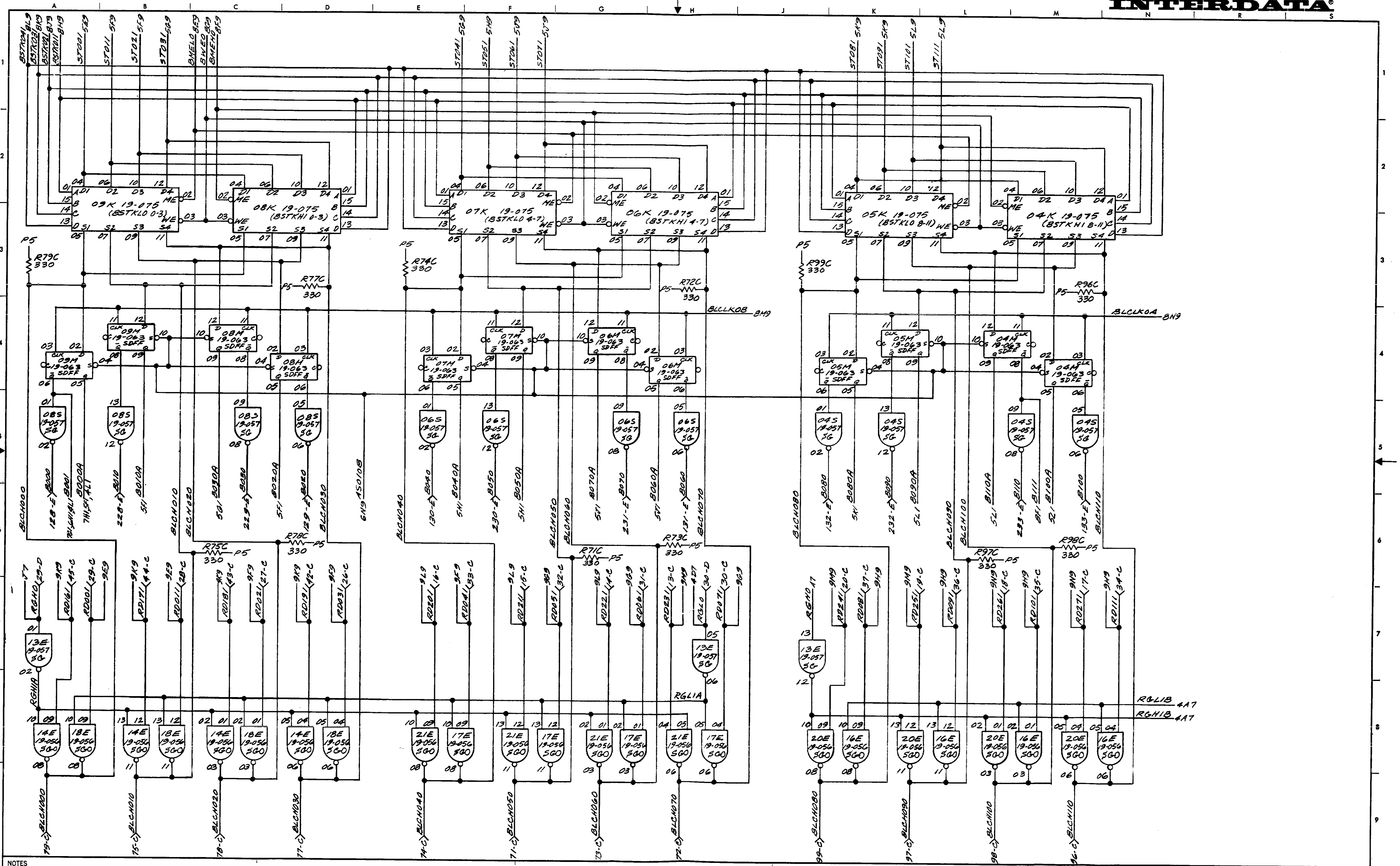
NOTES
1. ALL RESISTORS 330Ω.

NAME	TITLE	DATE
E. ROE	DRAFT	4-18-72
7	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 80 ALU

TASK NO 03215
DWG NO 35-404 R01D08
SHEET 2- OF

INTERDATA®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ST001 5J9
ST011 5F9
ST021 5F9
ST031 5G9
BMEL0 8E9
BWE0 8C9
BMEH0 8F9
ST041 5K9
ST051 5H9
ST061 5G9
ST071 5J9
ST081 5K9
ST091 5K9
ST101 5L9
ST111 5L9
09K 19-075 (BSTKL0 0-3)
08K 19-075 (BSTKHI 0-3)
07K 19-075 (BSTKL0 4-7)
06K 19-075 (BSTKHI 4-7)
05K 19-075 (BSTKL0 8-11)
04K 19-075 (BSTKHI 8-11)
P5
R79C 330
R77C 330
R74C 330
R72C 330
R99C 330
R96C 330
BLCLK0B 8H9
BLCLK0A 8N9
09M 19-063 SDFF
08M 19-063 SDFF
07M 19-063 SDFF
06M 19-063 SDFF
05M 19-063 SDFF
04M 19-063 SDFF
08S 19-057 SG
06S 19-057 SG
04S 19-057 SG
BLCH000
B000
B001
B000A
BLCH010
BLCH020
BLCH030
B010
B010A
B020
B020A
B030
B030A
AS010B
6N9
BLCH040
B040
B040A
B050
B050A
BLCH050
BLCH060
B070
B070A
B060
B060A
BLCH070
BLCH080
B080
B080A
B090
B090A
BLCH090
BLCH100
B110
B110A
B111
B100
B100A
BLCH110
R75C 330
R78C 330
R71C 330
R73C 330
R97C 330
R98C 330
RGH10
RD161
RD001
RD171
RD011
RD181
RD021
RD191
RD031
RD201
RD041
RD211
RD051
RD221
RD061
RD231
RGL0
RD071
RD241
RD081
RD251
RD091
RD261
RD101
RD271
RD111
13E 19-057 SG
RGHIA
RGL1A
RGL1B 4A7
RGHIB 4A7
14E 19-056 SG0
18E 19-056 SG0
21E 19-056 SG0
17E 19-056 SG0
20E 19-056 SG0
16E 19-056 SG0
79-C BLCH000
75-C BLCH010
78-C BLCH020
77-C BLCH030
74-C BLCH040
71-C BLCH050
73-C BLCH060
72-C BLCH070
99-C BLCH080
97-C BLCH090
98-C BLCH100
96-C BLCH110

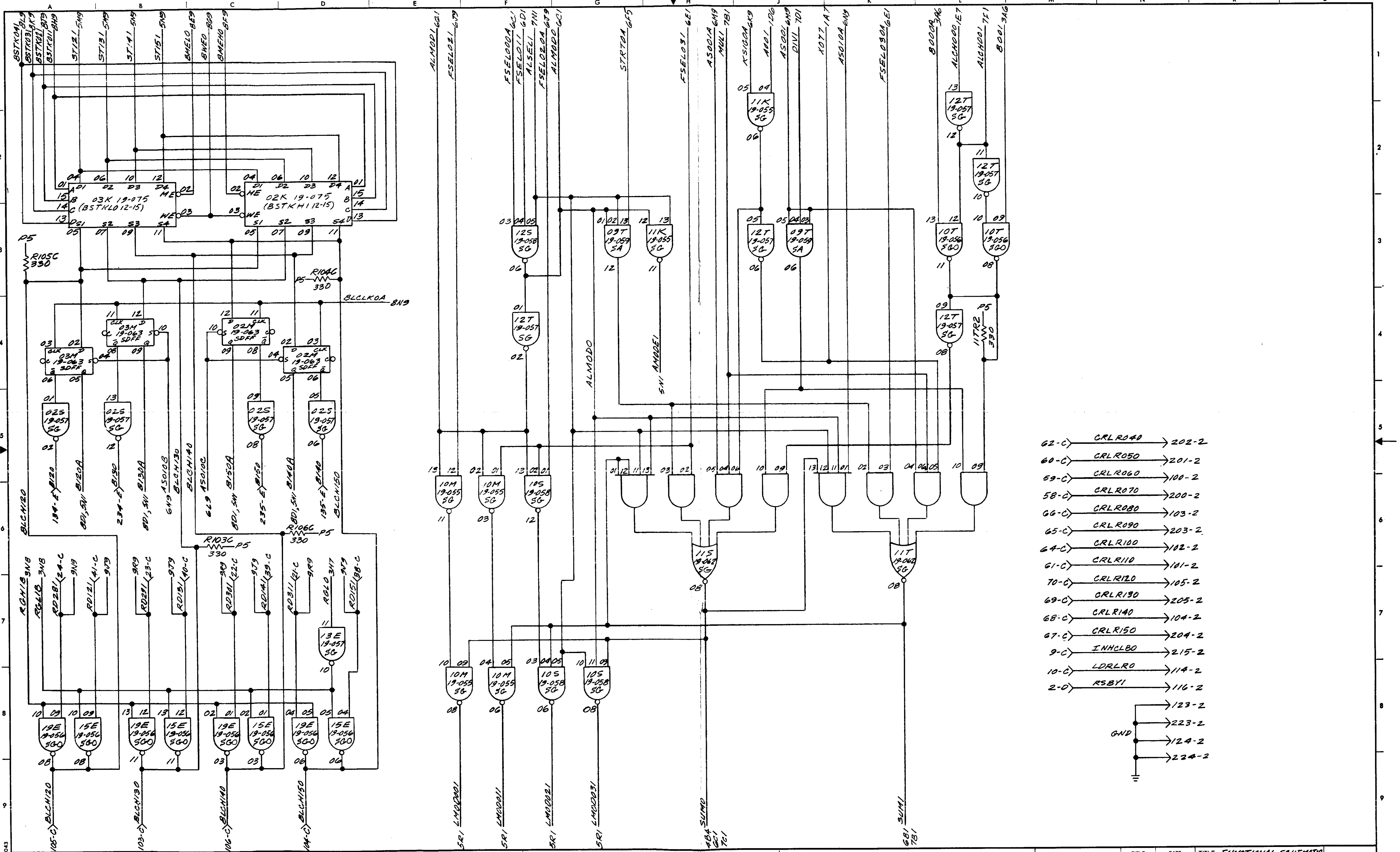
NOTES

NAME	TITLE	DATE
E. ROE	DRAFT	4-21-72
7	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 80 ALU

TASK NO. 03215
DWG NO. 35-404 R01 D08
SHEET 3 OF –

BRUNING 44-231 15043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BSTK031
BSTK021
BSTK011
ST121
ST131
ST141
ST151
BMEL0
BWE0
BMEH0
03K 19-075 (BSTKL012-15)
02K 19-075 (BSTKH112-15)
R105C 330
R104C 330
BLCLK0A 8N9
03M 19-063 SDFF
02M 19-063 SDFF
02S 19-057 SG
R103C 330
R106C 330
13E 19-057 SG
19E 19-056 SGO
15E 19-056 SGO
BLCH120
BLCH130
BLCH140
BLCH150
ALM0D1
FSEL021
FSEL00A
FSEL011
ALSEL1
FSEL02A
ALM0D2
STRT0A
FSEL031
AS001A
MUL1
KSIG0A
A001
AS201
DIV1
X077
AS010A
FSEL030A
B000A
ALCH000
ALCH001
B001
12S 19-058 SG
09T 19-059 SA
11K 19-055 SG
12T 19-057 SG
10T 19-056 SGO
ALM0D0
AM0DE1
11TR2 330
10M 19-055 SG
10S 19-058 SG
11S 19-062 SG
11T 19-062 SG
LM0D001
LM0D011
LM0D021
LM0D031
SUM0
SUM1
62-C CRLR040 202-2
60-C CRLR050 201-2
59-C CRLR060 100-2
58-C CRLR070 200-2
66-C CRLR080 103-2
65-C CRLR090 203-2
64-C CRLR100 102-2
61-C CRLR110 101-2
70-C CRLR120 105-2
69-C CRLR130 205-2
68-C CRLR140 104-2
67-C CRLR150 204-2
9-C INHCLB0 215-2
10-C LDRLR0 114-2
2-0 RSBY1 116-2
GND 123-2 223-2 124-2 224-2

NOTES

NAME	TITLE	DATE
E. ROE	DRAFT	4-28-72
✓	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 80 ALU

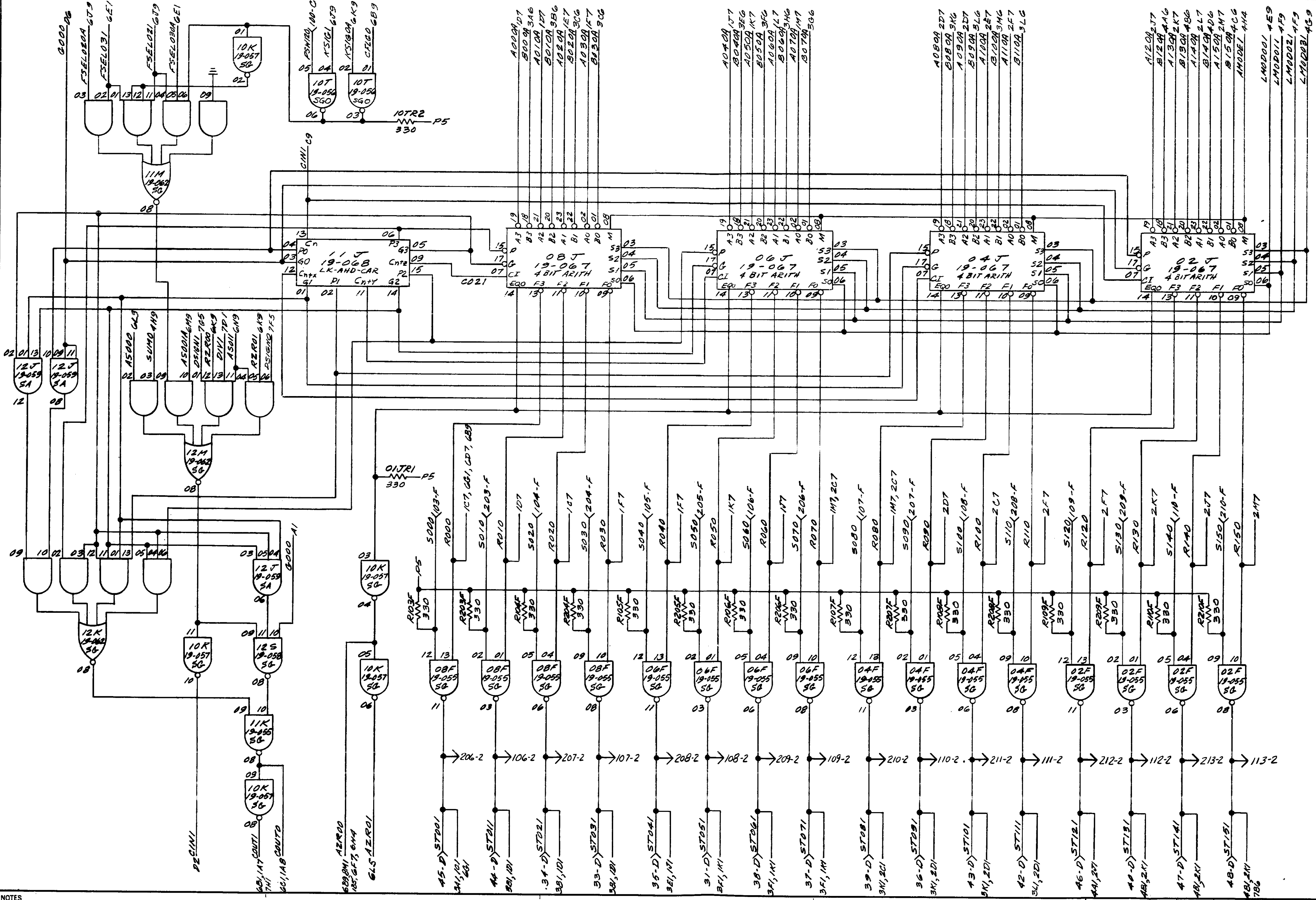
TASK NO. 03215
DWG NO. 35-404R01D08
SHEET 4 OF

BRUNING 44-231 15043

INTERDATA®

AREA C4: 12M-01 NMEM.
WAS MQ000

PC	JM	3215-30		1-10-73	R05



11J 19-068 LK-AHD-CAR
08J 19-067 4 BIT ARITH
06J 19-067 4 BIT ARITH
04J 19-067 4 BIT ARITH
02J 19-067 4 BIT ARITH
11M 19-062 SG
12M 19-062 SG
12K 19-062 SG
12J 19-059 SA
12S 19-058 SG
11K 19-055 SG
10K 19-057 SG
10T 19-056 SGO
08F 19-055 SG
06F 19-055 SG
04F 19-055 SG
02F 19-055 SG
FSEL020A 6J9
FSEL031 6E1
FSEL021 6J9
FSEL030A 6E1
G000 D6
FSW100 10-C
KS1G1 6J9
KS1G0A 6K9
CR1G0 6B9
10TR2 330 P5
01JR1 330 P5
C1N1 C9
C021
A000A 1D1
B000A 3A6
A010A 1F1
B010A 3B6
A020A 1E1
B020A 3C6
A030A 1F7
B030A 3G6
A040A 1J1
B040A 3E6
A050A 1K7
B050A 3F6
A060A 1L7
B060A 3H6
A070A 1M7
B070A 3B6
A080A 2D1
B080A 3K6
A090A 2D1
B090A 3L6
A100A 2E1
B100A 3M6
A110A 2F7
B110A 3L6
A120A 2J7
B120A 4A6
A130A 2K7
B130A 4B6
A140A 2L7
B140A 4D6
A150A 2M7
B150A 4C6
AMODE1 4H4
LMOD001 4E9
LMOD011 4F9
LMOD021 4F9
LMOD031 4G9
AS000 6L9
SUM0 4H9
AS00A 6M9
DSIGN1 7G5
RZR00 6K9
DIV1 7D1
AS011 6N9
RZR01 6K9
DSIGN0 7F5
G000 A1
S000 103-F
R000 1C7, 6G1, 6D7, 6B9
S010 203-F
R010 1D7
S020 104-F
R020 1C7
S030 204-F
R030 1F7
S040 105-F
R040 1F7
S050 205-F
R050 1K7
S060 106-F
R060 1H7
S070 206-F
R070 1M7, 2C7
S080 107-F
R080 1M7, 2C7
S090 207-F
R090 2D7
S100 108-F
R100 2C7
S110 208-F
R110 2F7
S120 109-F
R120 2F7
S130 209-F
R130 2K7
S140 110-F
R140 2J7
S150 210-F
R150 2M7
R103F 330
R203F 330
R104F 330
R204F 330
R105F 330
R205F 330
R106F 330
R206F 330
R107F 330
R207F 330
R108F 330
R208F 330
R109F 330
R209F 330
R110F 330
R210F 330
206-2
106-2
207-2
107-2
208-2
108-2
209-2
109-2
210-2
110-2
211-2
111-2
212-2
112-2
213-2
113-2
ST001 45-D 3H1, 1C1, 6G1
ST011 44-D 3B1, 1D1
ST021 34-D 3B1, 1D1
ST031 33-D 3B1, 1D1
ST041 35-D 3E1, 1C1
ST051 31-D 3F1, 1K1
ST061 38-D 3F1, 1K1
ST071 37-D 3F1, 1H1
ST081 39-D 3H1, 2C1
ST091 36-D 3K1, 2D1
ST101 43-D 3K1, 2D1
ST111 42-D 3L1, 2D1
ST121 46-D 4A1, 2J1
ST131 40-D 4B1, 2K1
ST141 47-D 4B1, 2K1
ST151 48-D 4B1, 2K1 7B6
D2 C1N1
COUT1 3B1, 1A7 7H1
COUT0 6C1, 1A8
AZR00 6B9, 8M1 1B5, 6F7, 6H4
6L5 AZR01

NOTES

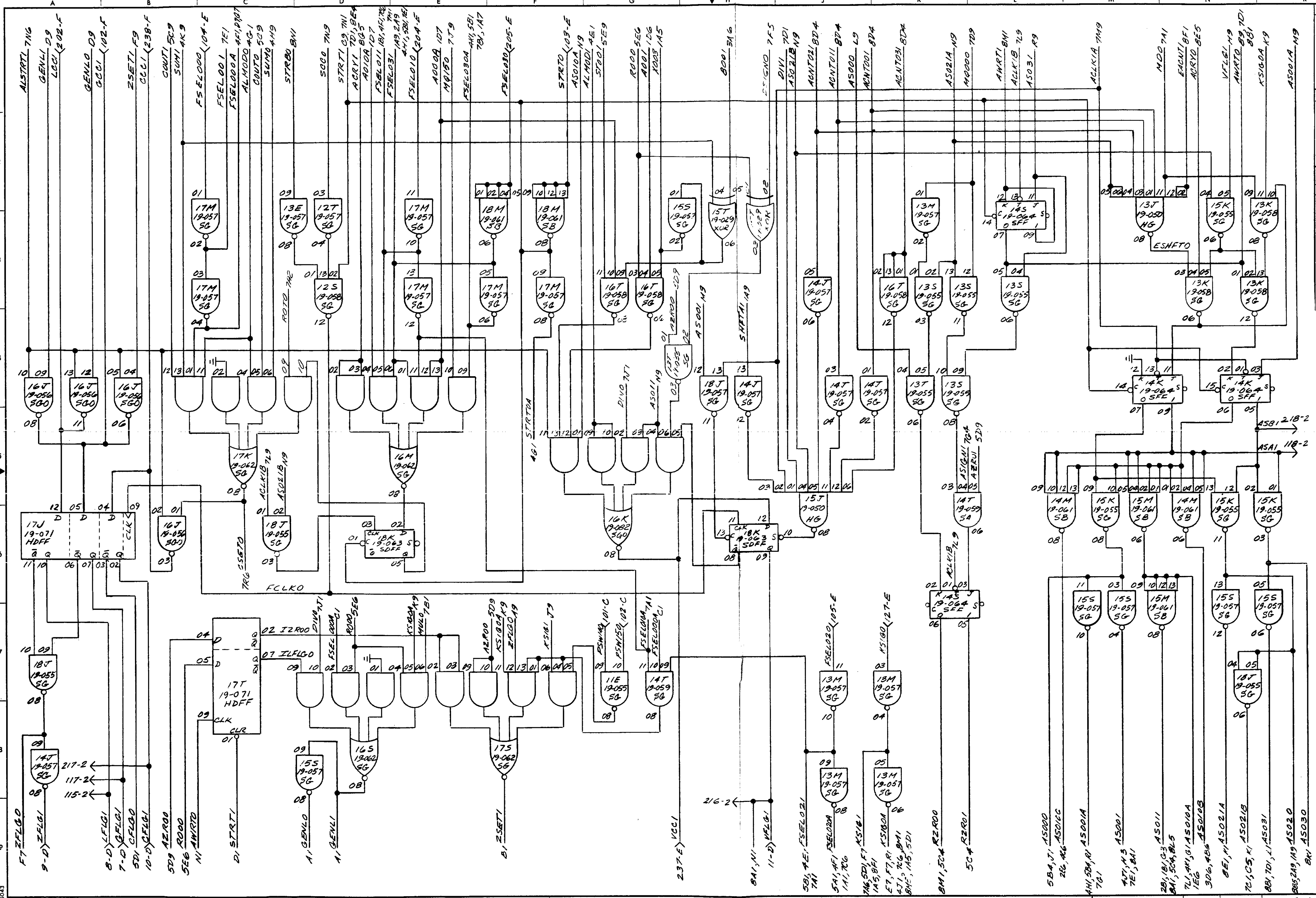
NAME	TITLE	DATE
E. ROE	DRAFT	5-4-72
7	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 80 ALU

TASK NO. 03215
DWG NO. 35-404RC5D08
SHEET 5 OF –

BRUNING 44-231 15043

INTERDATA®



ALSTRT1 7N6
GENL1 D9
CC01 202-F
GENL0 D9
CC01 102-F
ZSET1 F9
CC01 238-F
COUT1 5C9
SUM1 AK9
FSEL000 104-E
FSEL001 7E1
FSEL000A 4F1
ALMOD0 AG1
COUT0 5C9
SUM0 AH9
STRB0 BN1
S000 7N9
STRT1 C9
ACRY1 7D1
A010A 1D7
FSEL011
FSEL031
FSEL010 204-E
A000A 1D7
MR150 7T9
FSEL030A
FSEL030 205-E
STRT0 103-E
AS010A N9
ALMOD1 AE1
ST00 5E9
R000 5E6
A001 1D6
X003 1A5
B001 3A6
DSIGN0 7F5
DIV1 7D1
AS021B N9
ACNT021 8D4
ACNT011 8D4
AS000 L9
ACNT001 8D4
ACNT031 8D4
AS021A N9
M000 7D9
AWRT1 8H1
ACLK1B 7L9
AS031 R9
ACLK1A 7M9
MD0 2A1
EACN1 8F1
ACRY0 8E6
VFLG1 N9
AWRT0 89
KS100A K9
AS001A M9
17M 19-057 SG
13E 19-057 SG
12T 19-057 SG
18M 19-061 SB
15S 19-057 SG
15T 19-029 XOR
17S 19-029 XOR
13M 19-057 SG
14S 19-064 SFF
13J 19-050 HG
15K 19-055 SG
13K 19-058 SG
12S 19-058 SG
16T 19-058 SG
14J 19-057 SG
13S 19-055 SG
ESHFT0
R0T0 7H2
A2R00 5D9
AS001 N9
SHFT1 1A9
16J 19-056 SG0
17K 19-062 SG
16M 19-062 SG
18J 19-057 SG
14J 19-057 SG
14T 19-057 SG
14J 19-057 SG
13T 19-055 SG
13S 19-055 SG
14K 19-064 SFF
ASB1 218-2
ASA1 118-2
DIV0 7J1
AS011 N9
STRT0A
AG1
ACLK1B 7L9
AS021B N9
17J 19-071 HDFF
16J 19-056 SG0
18J 19-055 SG
18K 19-063 SDFF
2SET0
7K6
16K 19-062 SG0
15J 19-050 HG
18K 19-063 SDFF
ASIGN1 7G4
A2R01 5D9
14T 19-059 SA
14S 19-064 SFF
ACLK1B 7L9
FCLK0
14M 19-061 SB
15K 19-055 SG
15M 19-061 SB
15S 19-057 SG
15M 19-061 SB
18J 19-055 SG
17T 19-071 HDFF
CLK
CLR
I2R00
ILFLG0
DIV1 7J1
FSEL000A
R000 5E6
KS100A K9
MUL0 7B1
A2R00 5D9
KS100A K9
Z1FLG0 19
KS101 J9
PSW140 101-C
PSW150 102-C
FSEL030A 7A1
FSEL020A
11E 19-055 SG
14T 19-059 SG
16S 19-062 SG
17S 19-062 SG
15S 19-057 SG
FSEL020 105-E
KS100 127-E
13M 19-057 SG
18J 19-057 SG
14J 19-057 SG
217-2
117-2
115-2
216-2
F7 ZFLG0
9-D ZFLG1
8-D LFLG1
7-D GFLG1
5D1 CFLG1
10-D CFLG1
5D9 A2R00
5E6 R000
N1 AWRT0
D1 STRT1
A1 GENL0
A1 GENL1
B1 ZSET1
237-E VCC1
8A1, N1
11-D VFLG1
5B1, AE1, 7A1 FSEL021
5A1, AF1, 1A1, 7C6 FSEL020A
7A6, 5D1, F7 KS161
E7, F7, R1, 4J1, 7C6, 8H1, 1A5, 5D1 KS100A
8A1, 5C4 A2R00
5C4 A2R01
5B4, J1, 2E6, 4C6 AS000 AS010C
4H1, 5B4, R1, 7G1 AS001A
4J1, H3, 7E1, 8A1 AS001
2B1, 1B1, G3, 8A1, 5C4, 8L5 AS011
7L1, 4K1, G1, 1EG AS010A
3D6, 4B16 AS010B
8E1, K1 AS021A
7C1, C5, K1 AS021B
8B1, 7D1, L1 AS031
8B5, 2A9, 1A9 AS020
8K1 AS030
A B C D E F G H J K L M N R S
1 2 3 4 5 6 7 8 9

REVISIONS

REMOVED - AT H3, 15T08 WAS TO 15T06, 15T09 WAS P/O SUM1 (AT B2), 15T10 WAS P/O B000 (AT 3A6), PULLUP RES 15TR2-330 WAS TO 15T06; AT H4, 13T03 (19-055) WAS TO 16K06, 13T01 WAS TO 16T11, 13T03 WAS DSIGN0 TO 19T07 (AT 7F5).
CHANGED - 15T WAS 19-056 IC
ADDED 15T03 & ASSOC CKT AT H4

7		3215-22		10-11-72	R03

AREA G4: 15T02 MNEMONIC WAS DSIGN1. ADDED GATE 13T03; 15T03 WAS TO 16K05; AT 6C4 17K09 WAS TO 17K10; AT 6K3, 16T02 WAS TO 15T04 (SUM0) & 16T13 WAS TO 14T05 (AZR01).

PE		3215-30		1-10-73	R05

AT LOC H2, 15T04 WAS CONN. TO 'SUM0' (SCHEMATIC ERROR ONLY)

7		3215-39		3-16-73	R06

NOTES

NAME	TITLE	DATE
E. ROE	DRAFT	5-1-72
	CHK	
	ENGR	
	DIR ENG	

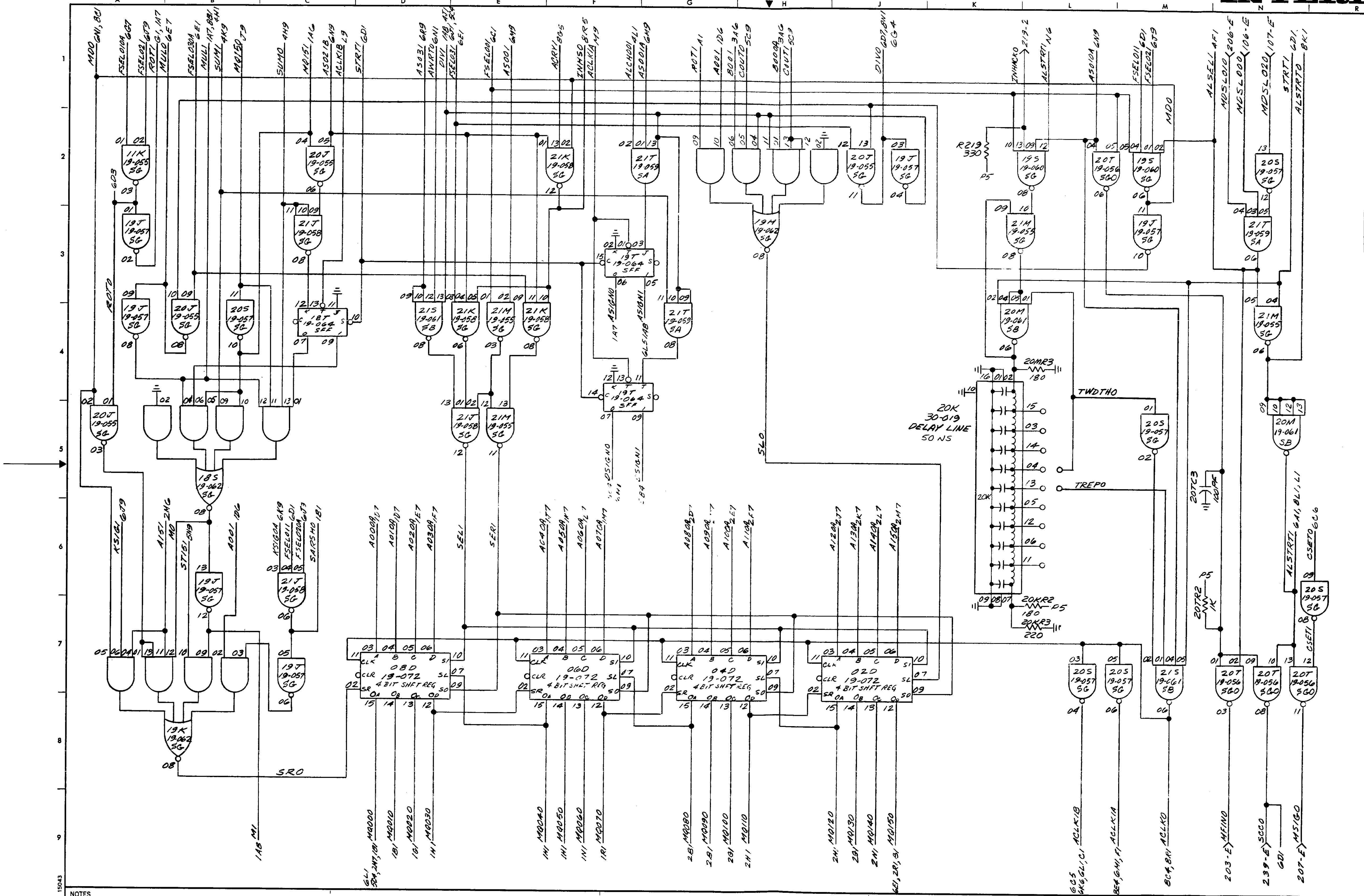
TITLE FUNCTIONAL SCHEMATIC
MODEL 80 ALU

TASK NO. 03215
DWG NO. 35-404R06D08
SHEET 6 OF -

BRUNING 44-231 15043

INTERDATA®

REVISIONS					
AT LOC N7, 20T02 WAS TO 20T10; ADDED 20T02 TO 21T06					
7	W	3215-15		8-24-72	R02
CHANGED-AT F5, DSIGNO WAS TO 13T02 (AT 6H3); ADDED DSIGN1 TO 15T02 (AT 6H3).					
7	JM	3215-22		10-11-72	R03
AT LOC L4, 20M01 WAS CONN TO 21S01 (TREPO)					
7	RM	3215-39		3-16-73	R06


A B C D E F G H J K L M N R S
1 2 3 4 5 6 7 8 9
MDO GN1, 8C1
FSEL01A 6G1
FSEL02 6G9
ROT1 G1, 1A7
MUL0 6E7
FSEL03A 6E1
MUL1 1A7, 8B1
SUM1 4K9
MR150 7J9
SUMO 4H9
MR151 1A6
A502 1B 6N9
ACLK1B 1J9
STRT GD1
A503 6R9
AWRT0 6N1
DIV1 1A8, A1
FSEL03 6E1
FSEL00 6L1
A500 6M9
ACRV1 8G5
INHSO 8R5
ACLKIA M9
ALCH00 ALL
A500A 6M9
ROT1 A1
ADD1 1D6
B001 3A6
COUTO 5C9
B000 3A6
CNUT1 5C3
DIV0 6D1, 8H1
INHRXO 219-2
ALSTRT1 N6
A501A 6N9
FSEL01 6D1
FSEL02 6J9
MDO
ALSEL AF1
MDSL010 206-E
MDSL00 106-E
MDSL020 107-E
STRT1 6D1
ALSTRTO 8K1
11K 19-055 SG
19J 19-057 SG
20J 19-055 SG
21J 19-058 SG
21K 19-058 SG
21T 19-059 SA
20T 19-055 SG
19M 19-062 SG
19S 19-060 SG
20T 19-056 SGO
20S 19-057 SG
21M 19-055 SG
20M 19-061 SB
19T 19-064 SFF
18T 19-064 SFF
21S 19-061 SB
18S 19-062 SG
19K 19-062 SG
R219 330 P5
ROTO
A1S1
DSIGNO
DSIGN1
A1S1AB
SLO
TWDTHO
TREPO
20MR3 180
20K 30-019 DELAY LINE 50 NS
20KR2 180 P5
20KR3 220
20TC3 100PF
20TR2 1K
KS161 6J9
A151 2H6
MD
ST151 5H9
A001 1D6
KSIG0A 6K9
FSEL01A 6D1
FSEL02A 6J3
SARSHO 1B1
A000A A001A A002A A003A
SEL1
SER1
ACA4A A05A A06A A07A
A08A A09A A10A A11A
A12A A13A A14A A15A
08D 19-072 4 BIT SHFT REG
06D 19-072 4 BIT SHFT REG
04D 19-072 4 BIT SHFT REG
02D 19-072 4 BIT SHFT REG
CLK CLR SR SL S1 S0 QA QB QC QD
SRO
1A8 M1
6L1 5A4, 2H7, 1B1 MQ000
1B1 MQ010
1B1 MQ020
1H1 MQ030
1H1 MQ040
1H1 MQ050
1N1 MQ060
1R1 MQ070
2B1 MQ080
2B1 MQ090
2B1 MQ100
2H1 MQ110
2H1 MQ120
2B1 MQ130
2H1 MQ140
6E1, 2R1, 3B1 MQ150
ACLK1B 6C5 6K6, 2L1, C1
ACLK1A 8E4, 6M1, F1
ACLKO 8C4, 8F1
MFINO 203-E
SCCO 239-E GD1
MSIGO 207-E
ALSTRT1 6A1, 8L1, L1
CSETO 6G6
CSET1

NOTES

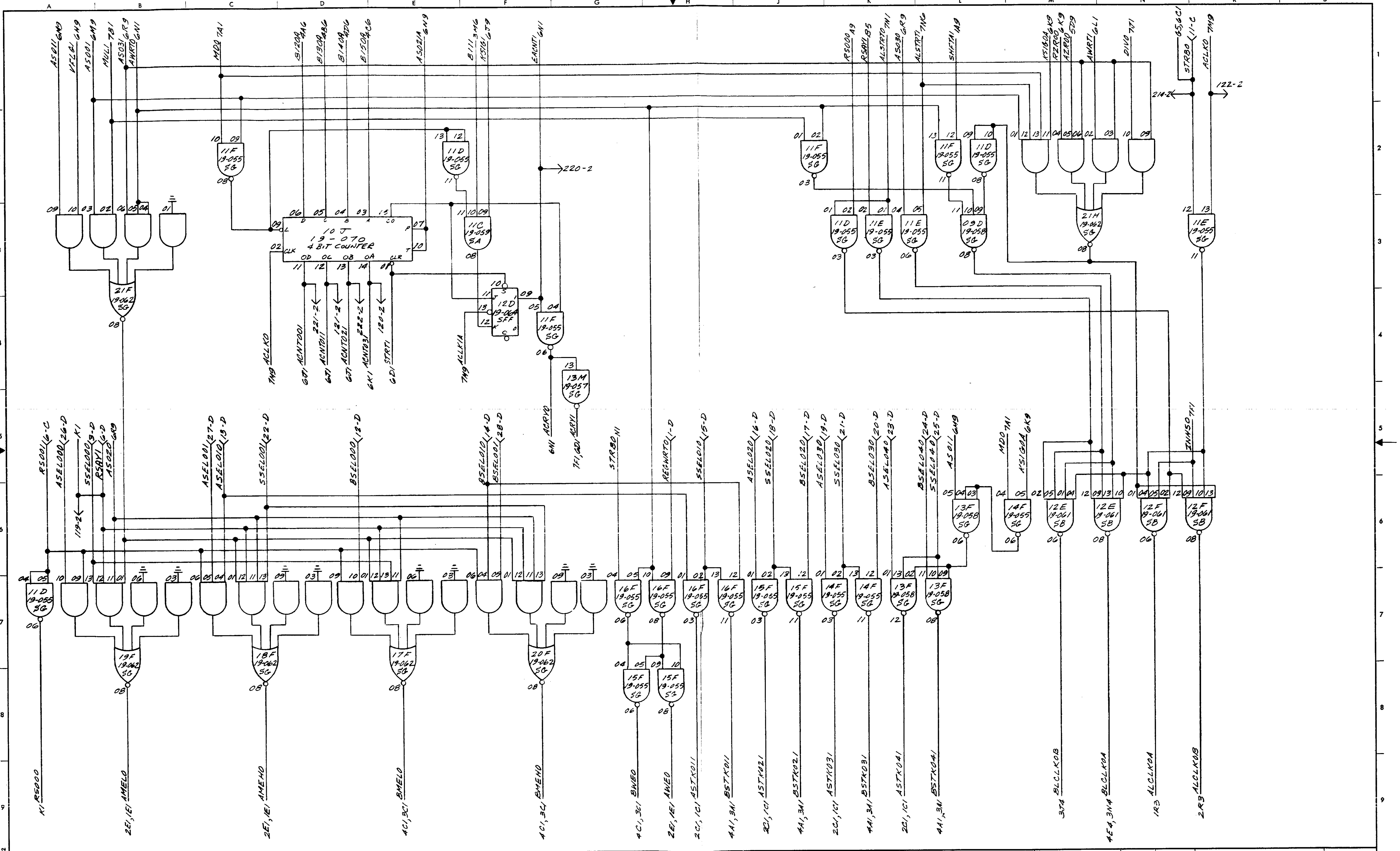
BRUNING 44-231 15043

NAME	TITLE	DATE
E. ROE	DRAFT	5-8-72
7	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 80
ALU

TASK NO. 03215
DWG NO. 35-404R06 D08
SHEET 7 OF —

INTERDATA®



AS011 GN9
VZG1 GN9
AS001 GM9
MUL1 7B1
AS031 GR9
AWRTO GN1
MDO 7A1
BI20A 4AG
BI30A 4BG
BI40A 4DG
BI50A 4CG
AS021A GN9
BI11 3MG
KSIG1 GT9
EACNT1 GN1
RS000 A9
RSAY1 B5
ALSTRO 7N1
AS030 GR9
ALSTRT 7NG
SHFTA1 A9
KSIG0A GK9
RZRO1 K9
AZRUO 5D9
AWRT1 GL1
DIVO 7T1
GSGC1
STRBO 11-C
ACLKO 7N9
214-2
122-2
220-2
11F 19-055 SG
11D 19-055 SG
10J 19-070 4 BIT COUNTER
11C 19-059 SA
12D 19-064 SFF
11E 19-055 SG
09D 19-058 SG
21H 19-062 SG
21F 19-062 SG
13M 19-057 SG
ACLKO 7N9
ACNT001 G71
ACNT011 221-2 G71
ACNT021 121-2 G71
ACNT031 222-2 GK1
STRT1 120-2 GD1
ALLK1A 7N9
ACRYO 6N1
ACRY1 7F1,GD1
RS001 16-C
ASEL000 26-D
SSEL000 K1 19-D
RSAY1 19-D
AS020 GR9
119-2
ASEL001 27-D
ASEL010 13-D
SSEL001 22-D
BSEL000 12-D
BSEL010 14-D
BSEL001 28-D
STRBO N1
REGWRTO 11-D
SSEL010 15-D
ASEL020 16-D
SSEL020 18-D
BSEL020 17-D
ASEL030 19-D
SSEL030 21-D
BSEL030 20-D
ASEL040 23-D
BSEL040 24-D
SSEL040 25-D
AS011 GN9
MDO 7A1
KSIG0A GK9
INHS0 7K1
11D 19-055 SG
19F 19-062 SG
18F 19-062 SG
17F 19-062 SG
20F 19-062 SG
16F 19-055 SG
15F 19-055 SG
14F 19-055 SG
13F 19-058 SG
14F 19-055 SG
12E 19-061 SB
12F 19-061 SB
K1 RS000
2E1,1E1 AMELO
2E1,1E1 AMEHO
4C1,3C1 BMELO
4C1,3C1 BMEHO
4C1,3C1 BWEO
2E1,1E1 AWEO
2C1,1C1 ASTK011
4A1,3A1 BSTK011
2C1,1C1 ASTK021
4A1,3A1 BSTK021
2C1,1C1 ASTK031
4A1,3A1 BSTK031
2C1,1C1 ASTK041
4A1,3A1 BSTK041
3J4 BLCLK0B
4E4,3N4 BLCLK0A
1R3 ALCLK0A
2R3 ALCLK0B

NOTES

BRUNING 44-231 16042

NAME	TITLE	DATE
E ROE	DRAFT	5-9-72
7	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 80
ALU

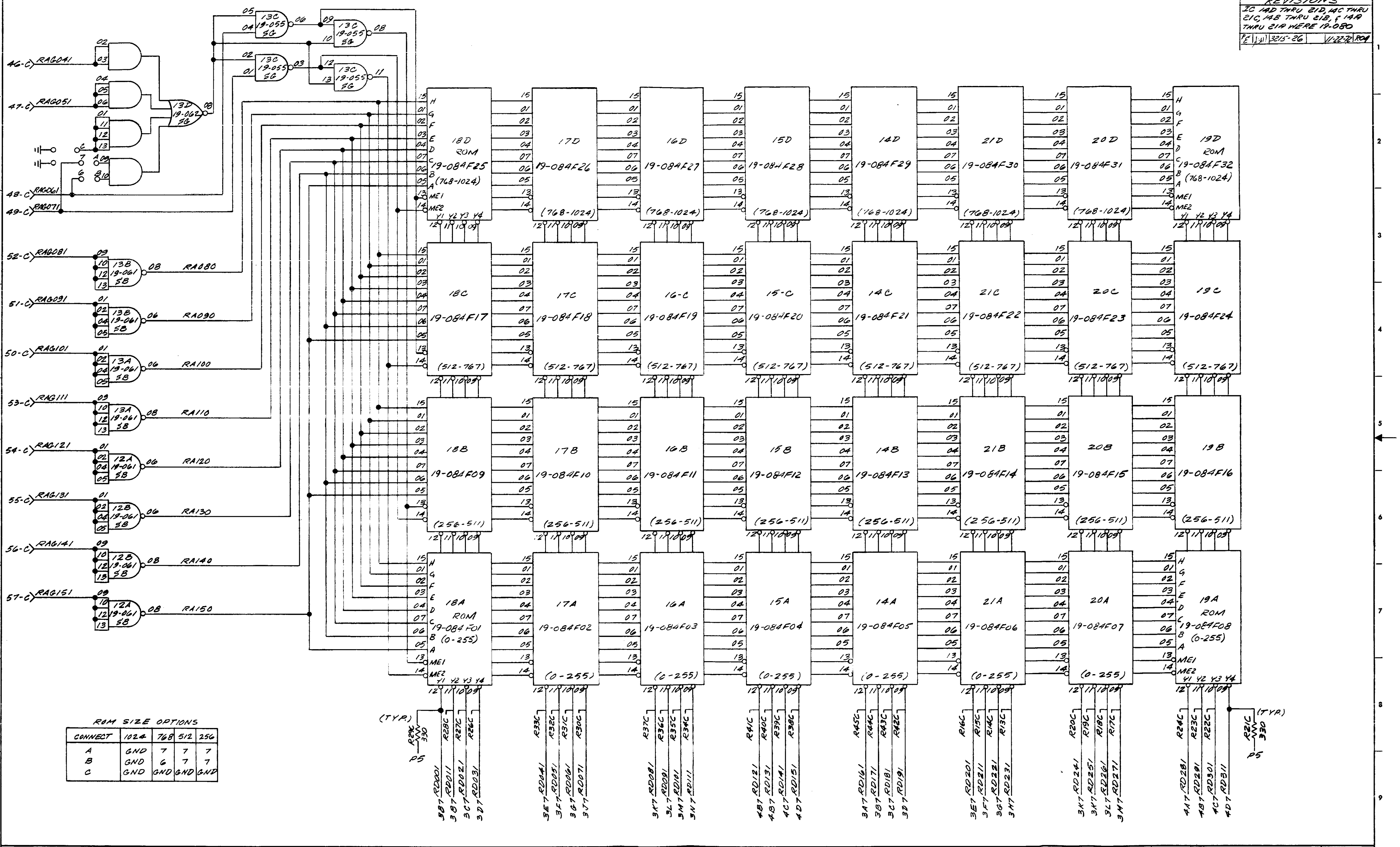
TASK NO. 03215
DWG NO. 35-404R01008
SHEET 8- OF

INTERDATA®

REVISIONS

IC 14D THRU 21D, 14C THRU 21C, 14B THRU 21B, & 14A THRU 21A WERE 19-080

PE	[illegible]	3215-26		11-22-72	R04



46-C RAG041
47-C RAG051
48-C RAG061
49-C RAG071
52-C RAG081
51-C RAG091
50-C RAG101
53-C RAG111
54-C RAG121
55-C RAG131
56-C RAG141
57-C RAG151
13D 19-062 SG
13C 19-055 SG
13B 19-061 SB
13A 19-061 SB
12B 19-061 SB
12A 19-061 SB
RA080
RA090
RA100
RA110
RA120
RA130
RA140
RA150
C
7
6
A
B
18D ROM 19-084F25 (768-1024)
17D 19-084F26 (768-1024)
16D 19-084F27 (768-1024)
15D 19-084F28 (768-1024)
14D 19-084F29 (768-1024)
21D 19-084F30 (768-1024)
20D 19-084F31 (768-1024)
19D ROM 19-084F32 (768-1024)
18C 19-084F17 (512-767)
17C 19-084F18 (512-767)
16-C 19-084F19 (512-767)
15-C 19-084F20 (512-767)
14C 19-084F21 (512-767)
21C 19-084F22 (512-767)
20C 19-084F23 (512-767)
19C 19-084F24 (512-767)
18B 19-084F09 (256-511)
17B 19-084F10 (256-511)
16B 19-084F11 (256-511)
15B 19-084F12 (256-511)
14B 19-084F13 (256-511)
21B 19-084F14 (256-511)
20B 19-084F15 (256-511)
19B 19-084F16 (256-511)
18A ROM 19-084F01 (0-255)
17A 19-084F02 (0-255)
16A 19-084F03 (0-255)
15A 19-084F04 (0-255)
14A 19-084F05 (0-255)
21A 19-084F06 (0-255)
20A 19-084F07 (0-255)
19A ROM 19-084F08 (0-255)
H G F E D C B A ME1 ME2
Y1 Y2 Y3 Y4
15 01 02 03 04 07 06 05 13 14
12 11 10 09
(TYP.)
R29C 330
P5
R28C R27C R26C
RD001 3B7
RD011 3B7
RD021 3C7
RD031 3D7
R33C R32C R31C R30C
RD041 3E7
RD051 3F7
RD061 3G7
RD071 3J7
R37C R36C R35C R34C
RD081 3K7
RD091 3L7
RD101 3M7
RD111 3N7
R41C R40C R39C R38C
RD121 4B7
RD131 4B7
RD141 4C7
RD151 4D7
R45C R44C R43C R42C
RD161 3A7
RD171 3B7
RD181 3C7
RD191 3D7
R16C R15C R14C R13C
RD201 3E7
RD211 3F7
RD221 3G7
RD231 3H7
R20C R19C R18C R17C
RD241 3K7
RD251 3K7
RD261 3L7
RD271 3M7
R24C R23C R22C
R21C 330
(TYP.)
P5
RD281 4A7
RD291 4B7
RD301 4C7
RD311 4D7
A B C D E F G H J K L M N R S
1 2 3 4 5 6 7 8 9

ROM SIZE OPTIONS

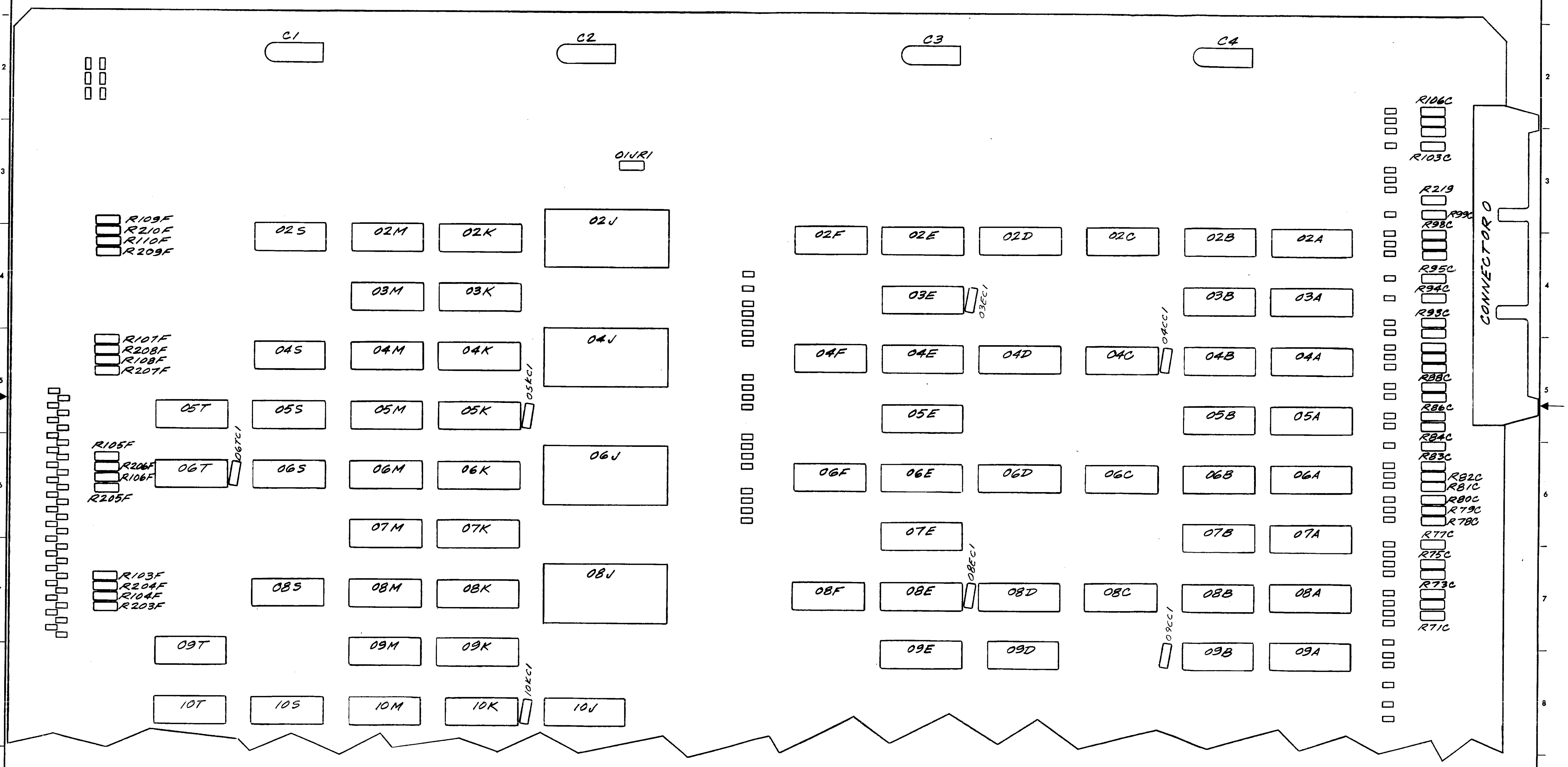
CONNECT	1024	768	512	256
A	GND	7	7	7
B	GND	6	7	7
C	GND	GND	GND	GND

NOTES

NAME	TITLE	DATE	TITLE FUNCTIONAL SCHEMATIC MODEL 80 ALU
E. ROE	DRAFT	5-11-72	
	CHK		
	ENGR		
			TASK NO. 03215 — SHEET 9 OF –
	DIR ENG		DWG NO. 35-404R04 D08

BRUNING 44-231 16042

INTERDATA®


C1
C2
C3
C4
01JR1
R109F
R210F
R110F
R209F
R107F
R208F
R108F
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R105F
R206F
R106F
R205F
R103F
R204F
R104F
R203F
02S
02M
02K
02J
03M
03K
04S
04M
04K
04J
05T
05S
05M
05K
05KC1
06T
06TC1
06S
06M
06K
06J
07M
07K
08S
08M
08K
08J
09T
09M
09K
10T
10S
10M
10K
10KC1
10J
02F
02E
02D
02C
02B
02A
03E
03EC1
03B
03A
04F
04E
04D
04C
04CC1
04B
04A
05E
05B
05A
06F
06E
06D
06C
06B
06A
07E
07B
07A
08F
08E
08EC1
08D
08C
08B
08A
09E
09D
09CC1
09B
09A
R106C
R103C
R219
R99C
R98C
R95C
R94C
R93C
R88C
R86C
R84C
R83C
R82C
R81C
R80C
R79C
R78C
R77C
R75C
R73C
R71C
CONNECTOR 0

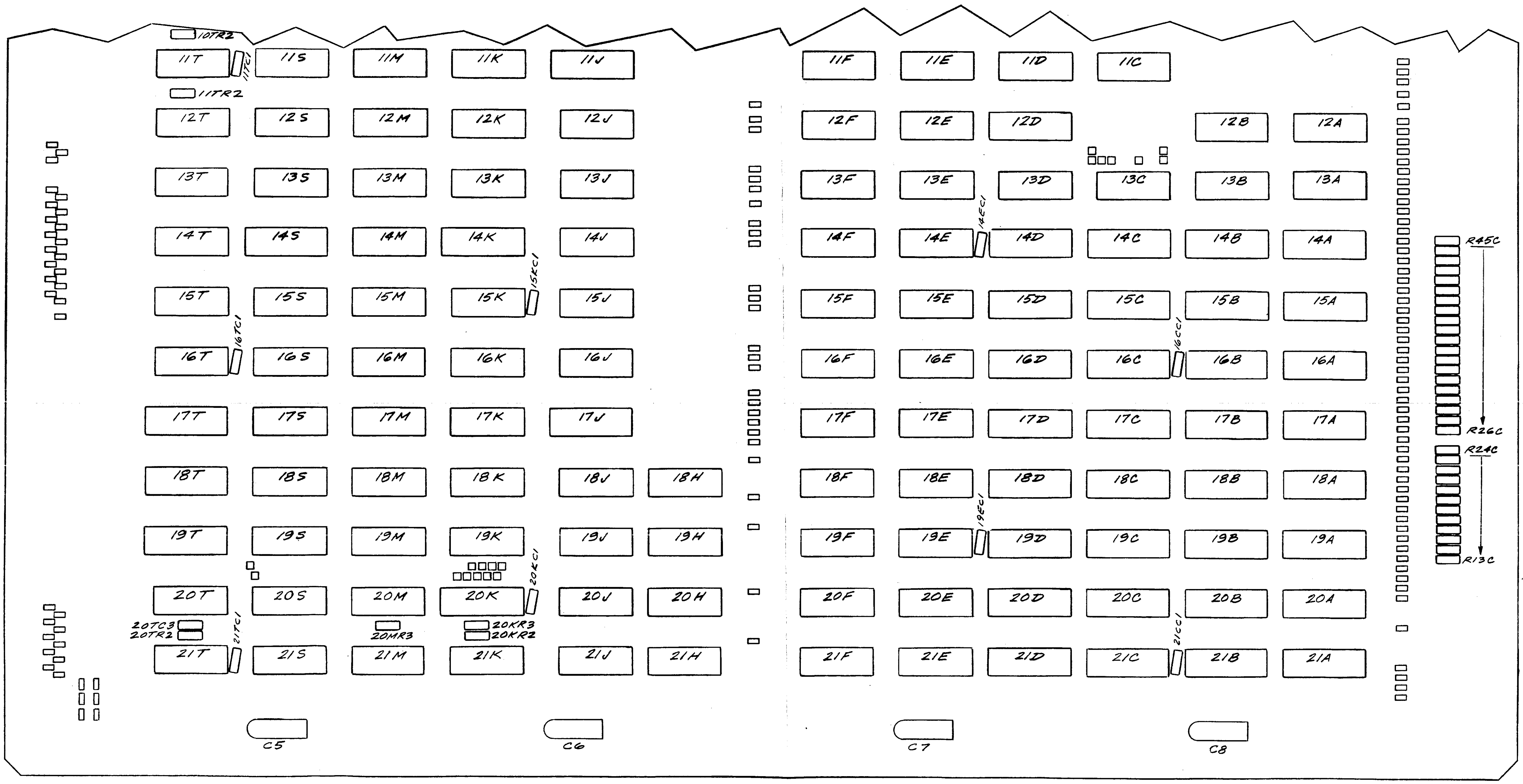
NOTES

BRUNING 44-231 16042

NAME	TITLE	DATE	TITLE
E. ROE	DRAFT	6-30-73	FUNCTIONAL SCHEMATIC COMPONENT LOCATER
	CHK		
	ENGR		TASK NO. 03215
	DIR ENG		DWG NO. 35-404 D08

SHEET 10 OF –

INTERDATA®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11T
11TC1
11S
11M
11K
11J
11F
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11C
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12J
12F
12E
12D
12B
12A
13T
13S
13M
13K
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13E
13D
13C
13B
13A
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14M
14K
14J
14F
14E
14EC1
14D
14C
14B
14A
R45C
15KC1
15T
15S
15M
15K
15J
15F
15E
15D
15C
15B
15A
16TC1
16CC1
16T
16S
16M
16K
16J
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16D
16C
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17D
17C
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17A
R26C
R24C
18T
18S
18M
18K
18J
18H
18F
18E
18D
18C
18B
18A
19EC1
19T
19S
19M
19K
19J
19H
19F
19E
19D
19C
19B
19A
R13C
20KC1
20T
20S
20M
20K
20J
20H
20F
20E
20D
20C
20B
20A
20TC3
20TR2
21TC1
20MR3
20KR3
20KR2
21CC1
21T
21S
21M
21K
21J
21H
21F
21E
21D
21C
21B
21A
C5
C6
C7
C8

NOTES

NAME	TITLE	DATE	TITLE
E. ROE	DRAFT	6-30-73	FUNCTIONAL SCHEMATIC COMPONENT LOCATER
	CHK		
	ENGR		TASK NO. 03215
	DIR ENG		DWG NO. 35-404 008

SHEET 11 OF —

BRUNING 44 231 16042

INTERDATA®

TEST POINTS	
CATN (NOTE 1)	8D2
TMGIA	8M1
KTM	6A8
GSTRTI	1N4
DSTRTI	2B6
LDBRI	9C5
ADBI	7K7
ADAI	7K6
GND (NOTE 1)	9J8
MNEMONIC	LOC.

CONSOLE OR DISPLAY

CONN	SHEET LOC.	MNEMONIC (ROW 2)	TERM NO.	MNEMONIC (ROW 1)	SHEET LOC.	CONN
3			24			3
			23			
			22			
			21			
			20			
			19			
			18			
			17			
			16			
			15			
	6A2	AC1	14	LBO	8F8	
	6A2	AC3	13	SRGO	7D6	
	6N4	X1	12	SD031	7G2	
	6N4	X2	11	SD021	7G2	
	6N4	X3	10	SD011	7G2	
	6N4	X4	09	SD001	7G1	
	7G5	SD071	08	X5	6N5	
	8F8	LCO	07	X6	6N5	
	8F6	SL00	06	SSGL1	8A5	
	7G4	SD061	05	POFFO	6A1	
	7G3	SD051	04	ESN00	8A4	
	8F7	LAO	03	ESNCO	8A3	
	7G3	SD041	02	WAITI	8F6	
	8F7	LDO	01	INITO	6A1	
	8F6	SHIO	00	GND		

TTY

CONN	SHEET LOC.	MNEMONIC (ROW 2)	TERM NO.	MNEMONIC (ROW 1)	SHEET LOC.	CONN
2			00			2
			01			
	9N9	GND	02	TN	9N6	
	9N8	RN	03	TDU	9N7	
	9N5	TP	04	RP	9N8	
			05			
			06			
			07			
			08			
			09			
			10			
			11			
			12			
			13			
			14			
			15			
			16			
			17			
			18			
			19			
			20			
			21			
			22			
			23			
			24			

CONN	SHEET LOC.	MNEMONIC (ROW 1)	TERM NO.	MNEMONIC (ROW 2)	SHEET LOC.	CONN
1		P5	41	GND		1
		GND	40	GND		
	6A3	P15	39	TACKO	8R6	
	6A3	N15	38	RACKO	8K6	
			37			
			36			
			35			
			34			
			33			
			32			
			31			
			30			
			29	CA150	1F1	
			28			
			27			
			26			
			25			
			24			
			23			
			22			
			21			
			20			
			19			
	3M1	A140	18	A150	3N1	
	3J1	A120	17	A130	3K1	
	3E1	A100	16	A110	3G1	
	3B1	A080	15	A090	3C1	
	3L6	A060	14	A070	3M6	
	3G6	A040	13	A050	3H6	
	3E6	A020	12	A030	3E6	
	3A6	A000	11	A010	3B6	
	3L9	S140	10	S150	3M9	
	3H9	S120	09	S130	3J9	
	3D9	S100	08	S110	3E9	
	3A9	S080	07	S090	3B9	
	3N9	S060	06	S070	3R9	
	3J9	S040	05	S050	3K9	
	3F9	S020	04	S030	3G9	
	3C9	S000	03	S010	3D9	
	5R3	GCCI	02	LCCI	5R2	
		GND	01	GND		
		P5	00	GND		

CONN	SHEET LOC.	MNEMONIC (ROW 1)	TERM NO.	MNEMONIC (ROW 2)	SHEET LOC.	CONN
0		P5	41	GND		0
		GND	40	GND		
		P15	39	SCCO	5R1	
		N15	38	CCCI	5R4	
	5D4	IAO	37	VCCI	5R4	
	5D2	IPFO	36	DPFO	5D3	
	3M1	B140	35	B150	3N1	
	3H1	B120	34	B130	3K1	
	3E1	B100	33	B110	3E1	
	3B1	B080	32	B090	3C1	
	3L1	B060	31	B070	3N1	
	3H1	B040	30	B050	3J1	
	3D1	B020	29	B030	3F1	
	3A1	B000	28	B010	3B1	
	1J1	KSIGO	27			
	6A6	SCLRO	26	HWO	2H2	
			25	DCRO	1H1	
			24			
	2A7	SYNO	23	ATN000	8R7	
	5R7	DACKO	22	ACKO	5R7	
	6N3	CL070	21	DAO	5R8	
	5R6	DRO	20	CMDO	5R8	
	5R7	SRO	19	ADRSO	5R6	
	4N5	D140	18	D150	4R5	
	4M5	D120	17	D130	4M5	
	4F5	D100	16	D110	4G5	
	4E5	D080	15	D090	4E5	
	4K5	D060	14	D070	4L5	
	4N5	D040	13	D050	4J5	
	4C5	D020	12	D030	4D5	
	4B5	D000	11	D010	4C5	
	6N5	PPFO	10	MMFO	5H3	
			09			
	8E5	DSPLY1	08			
	1N1	MDSL020	07	MSIGO	1H9	
	1N1	MDSL000	06	MDSL010	1N1	
	1L1	FSL020	05	FSL030	1K1	
	1M1	FSL000	04	FSL010	1L1	
	1R1	STRTO	03	MFINO	1H9	
		P5	02	P5		
		GND	01	GND		
		P5	00	GND		

REVISIONS					
REDRAWN FROM LAYOUT & REV. PER:					
DB		ECR 3215-05		7-11-72	R01
REVISED SHEETS 5,6,8 & 9					
7		3215-11		7-31-72	R02
REVISED SHEETS 1 & 8					
7		3215-14		8-23-72	R03
REVISED SHEET 5					
7		3215-18		10-3-72	R04
REVISED SHTS 1,2,3,5,6 & 8					
7		3215-20		10-11-72	R05
REVISED SHEET 6					
7		3215-24		10-23-72	R06
REVISED SHEETS 1,2,3,5,6,7					
7		3215-27		12-5-72	R07
REVISED SHEET 2					
7		3215-29		12-21-72	R08
ADDED M01 INFO; REVISED SHEETS 1,2,5,6,7,8,9					
7		3215-28		2-22-73	R09

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION:

35-405 R09
35-405F01 R09
35-405 M01 R00
35-405F01 M01 R00

NOTE:

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

SHEET INDEX	REV. LEVEL	9	9	9	7	1	9	9	9	9	9
	SHEET NO.	0	1	2	3	4	5	6	7	8	9

NOTES 1. TEST POINTS 'CATN' & 'GND' APPEAR ONLY ON 35-405M01 & F01M01 (25-368).

NAME	TITLE	DATE
D. BARKER	DRAFT	7-17-72
J.F. FLEMING	CHK	10-9-72
R.F. SCHUNNEMAN	ENGR	3-9-73
J.F. JAMES	SYS TEST	3-9-73
R.E. JONES	DIR ENG	3-9-73

TITLE FUNCTIONAL SCHEMATIC MODEL 80 IOU

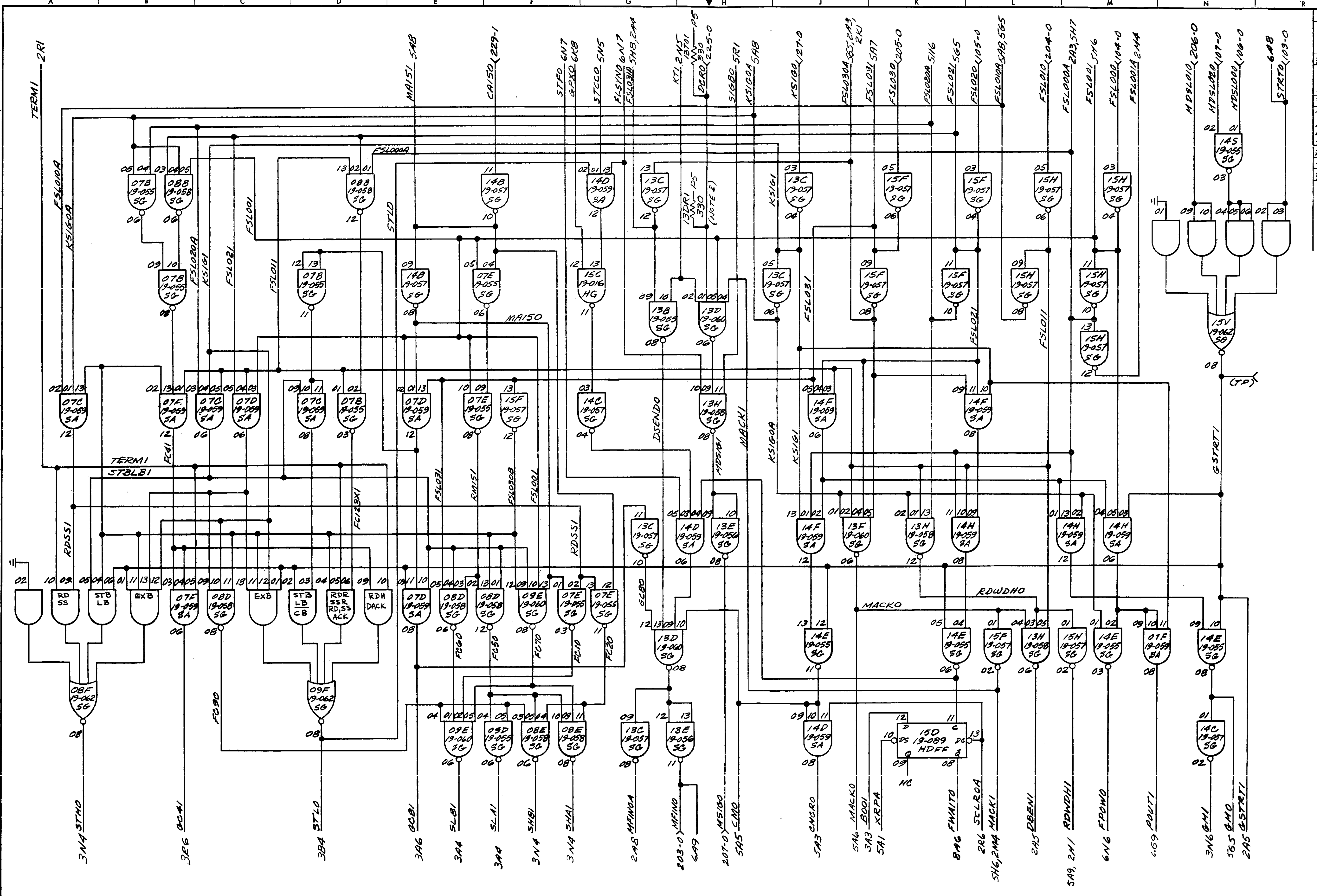
TASK NO. 03215

DWG NO. 35-405R09D08

SHEET 0 OF 10

BRUNING 44-231 16042

INTERDATA®


TERMI 2R1
FSL010A
KSIG0A
MAI51 5A8
CAI50 229-1
STFO 6N7
GPXO 6K8
STCCO 5N5
FLSYNO 6N7
FSL031A 5H8,2A4
KTI 2N5 3B01
DCRO 225-0
P5
13DR1 P5 330 (NOTE 2)
SIGBO 5R1
KSIG0A 5A8
KSIGO 127-0
FSL030A 5G5,2A3,2K1
FSL031 5A7
FSL030 206-0
FSL020A 5H6
FSL021 5G5
FSL020 105-0
FSL010A 5A8,5G5
FSL010 204-0
FSL000A 2A3,5H7
FSL001 5H6
FSL000 104-0
FSL001A 2M4
MDSL010 206-0
MDSL020 101-0
MDSL000 108-0
STRTO 103-0
6A8
07B 19-055 SG
08B 19-058 SG
08B 19-058 SG
14B 19-057 SG
14D 19-059 SA
13C 19-057 SG
15F 19-057 SG
15H 19-057 SG
14S 19-055 SG
15V 19-062 SG
FSL000A
STLO
FSL020A
KSIGI
FSL021
FSL011
FSL001
MAI50
DSENDO
MDSIGI
MACKI
KSIG0A
KSIGI
FSL031
FSL021
FSL011
GSTRTI
(TP)
TERMI
STBLBI
FC41
FC123XI
FSL031
RMI5I
FSL030B
FSL001
RDSSI
RDSSI
GCBO
MACKO
RDWDHO
RD SS
STB LB
EXB
EXB
STB LB CB
RDR SSR RD,SS ACK
RDH DACK
08F 19-062 SG
09F 19-062 SG
FCBO
FCGO
FC50
FC70
FC10
FC20
15D 19-089 HDFF
DS
DC
NC
3N4 STHO
3R6 GC41
3B4 STLO
3A6 GCBI
3A4 SLBI
3A4 SLAI
3N4 SHBI
3N4 SHAI
2A8 MFINOA
203-0 MFINO
6A9
207-0 MSIGO
5A5 CMO
5A3 CHCRO
5A6 MACKO
3A3 BOOI
5A1 XRPA
8A6 FWAITO
2R6 SCLROA
5H6,2M4 MACKI
2A5 DBENI
5A9,2H1 RDWDHI
6N6 FPOWO
6G9 POUTI
3N6 GMI
5G5 GMO
2A5 GSTRTI
A B C D E F G H J K L M N R S
1 2 3 4 5 6 7 8 9

REVISIONS

CHANGED - AT LOC K8, 15D10 WAS CONN TO SCLROA, & 15D13 WAS CONN TO XRPA.

7		3215-14		8-23-72	R03

CHANGED - AT LOC A5, TERMI LEAD WAS P/O KTI & WAS CONNECTED AT 13B10, LOC H3.

7		3215-20		10-11-72	R05

AT LOC B2, 08B04 WAS CONN TO 07C04 KSIGI; AT G3, IC 15C WAS 19-056 - REMOVED 15CR5, 330Ω TO P5 FROM 15C11; AT H2, DCRO WAS TO 13C01(19-057) - 13C02 WAS TO 13D01; AT K8, IC 15D WAS 19-063.

7		3215-27		12-5-72	R07

AT LOC H2 ADDED 13DR1 & NOTE 2.

7	RFS	3215-28		2-22-73	R09

NOTES 1. XRPA, XRPB & XRPC ARE 1K PULLUP RESISTORS TO P5 FOR UNUSED GATE/FF INPUTS.
2. 13DR1 APPEARS ONLY ON 35-405M01 & F01M01 (25-368).

NAME		TITLE	DATE
E. ROE		DRAFT	2-6-72
		CHK	
		ENGR	
		DIR ENG	

TITLE FUNCTIONAL SCHEMATIC

MODEL 80 IOU

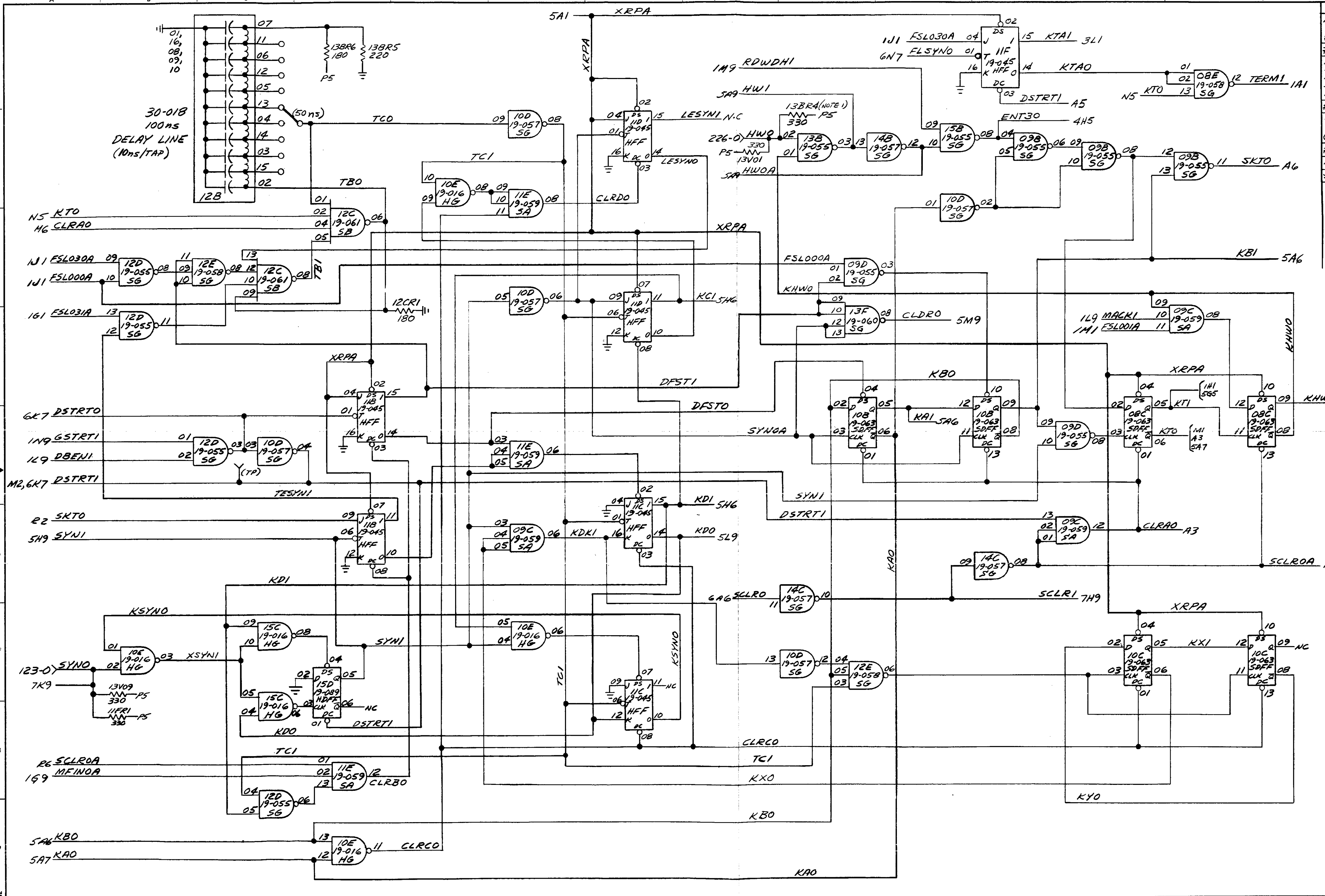
TASK NO. 03215

DWG NO. 35-405R09D08

SHEET OF 1 -

BRUNING 44-231 15043

INTERDATA®



5A1
XRPA
30-018
100ns
DELAY LINE
(10ns/TAP)
12B
13BR6 180
13BR5 220
P5
(50ns)
TCO
TBO
TC1
N5 KTO
M6 CLRAO
1J1 FSL030A
1J1 FSL000A
1G1 FSL031A
TB1
13CR1 180
6K7 DSTRTO
1N9 GSTRT1
1L9 DBEN1
M2,6K7 DSTRT1
(TP)
TESYN1
R2 SKTO
5H9 SYN1
KD1
KSYNO
123-0 SYNO
7K9
13V09 330 P5
11FR1 330 P5
XSYN1
KDO
DSTRT1
NC
TC1
R6 SCLROA
1G9 MFINOA
CLRBO
5A6 KBO
5A7 KAO
CLRCO
1M9 RDWDH1
5A9 HW1
13BR4 (NOTE 1) 330 P5
226-0 HWQ
P5 330 13V01
5A HWOA
LESYN1 N.C
LESYNO
CLRDO
KC1 5H6
DFST1
DFSTO
SYNOA
SYN1
KD1 5H6
KDO 5L9
KDK1
KSYNO
CLRCO
TC1
KXO
KBO
KAO
6A6 SCLRO
1J1 FSL030A
6N7 FLSYNO
KTA1 3L1
KTAO
DSTRT1 A5
N5 KTO
TERM1 1A1
ENT30 4H5
SKTO A6
FSL000A
KHWO
CLDRO 5M9
KB1 5A6
1L9 MACK1
1M1 FSL001A
KBO
KA1 5A6
XRPA
KT1 1H1 5G5
KTO 1M1 A3 5A7
KHW1 NC
CLRAO A3
SCLROA A8, 1L9
SCLR1 7H9
XRPA
KX1
NC
KYO

REVISIONS					
ADDED - AT LOC J4, 13F08 & ASSOC LEADS; AT L1 & N1, 11F(FF) & 08E12 & ASSOC LEADS.					
7	JCW	3215-20		10-11-72	R05
AT LOC B3, 12E11 WAS MACKO TO 13F06 SH. 1N6; AT F6, 09C04 WAS KYO TO 10C08; AT N5, 08C11 WAS KTO TO 08C06; AT D7, IC 15D WAS 19-063, IC 10E & 15C WERE 19-055.					
7	JCW	3215-27		12-5-72	R07
AT LOC C2, TCO OPTION WAS TO 12B04, 40 NS; AT B8, REMOVED SYNO TO 12DC4 (1000PF) TO 12DR5 (100 Ω) TO GND					
7	JCW	3215-29		12-21-72	R08
AT LOC J2, ADDED 13BR4 & NOTE 1.					
7	BB	3215-28		2-22-73	R09

NOTES 1. 13BR4 APPEARS ONLY ON 35-405 M01
& F01 M01 (25-348).

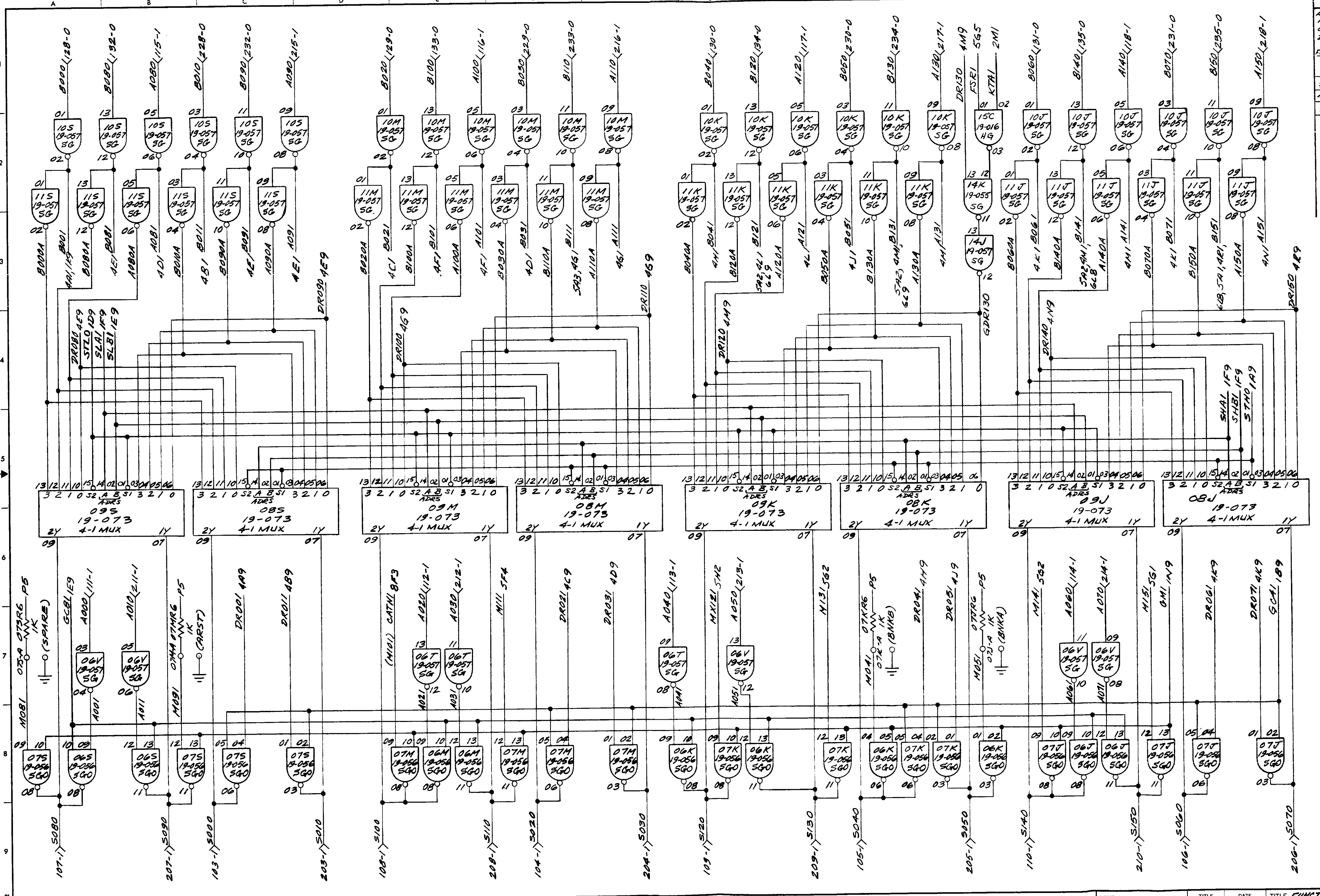
NAME	TITLE	DATE
	DRAFT	
7	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 80 IOU

TASK NO. 03215
DWG NO. 35-405R09 D08
SHEET 2 OF —

BRUNING 44-231 16042

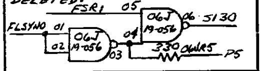
INTERDATA®



A
B
C
D
E
F
G
H
J
K
L
M
N
R
S
1
2
3
4
5
6
7
8
9
B000 128-0
B080 132-0
A080 115-1
B010 228-0
B090 232-0
A090 215-1
B020 129-0
B100 133-0
A100 116-1
B030 229-0
B110 233-0
A110 216-1
B040 130-0
B120 134-0
A120 117-1
B050 230-0
B130 234-0
A130 217-1
DR130 4M9
FSR1 5G5
KTA1 2M1
B060 131-0
B140 135-0
A140 118-1
B070 231-0
B150 235-0
A150 218-1
10S 19-057 SG
11S 19-057 SG
10M 19-057 SG
11M 19-057 SG
10K 19-057 SG
11K 19-057 SG
15C 19-016 HG
14K 19-055 SG
14J 19-057 SG
10J 19-057 SG
11J 19-057 SG
GDR130
DR080 1D9
STL0 1D9
SLA1 1F9
SLB1 1E9
DR090 4E9
DR100 4G9
DR110 4G9
DR120 4M9
DR140 4N9
DR150 4R9
SHA1 1F9
SHB1 1F9
STH0 1A9
3 2 1 0 S2 A B S1 3 2 1 0
ADRS
09S 19-073 4-1 MUX
08S 19-073 4-1 MUX
09M 19-073 4-1 MUX
08M 19-073 4-1 MUX
09K 19-073 4-1 MUX
08K 19-073 4-1 MUX
09J 19-073 4-1 MUX
08J 19-073 4-1 MUX
2Y
1Y
07S-A 07SRG 1K P5 (SPARE)
GCB1 1E9
A000 111-1
A010 211-1
07HA 07HRG 1K P5 (PRST)
DR001 4A9
DR011 4B9
(M101) CATN1 8F3
A020 112-1
A030 212-1
M111 5F4
DR021 4C9
DR031 4D9
A040 113-1
MX121 5H2
A050 213-1
M131 5G2
07K-A 07KRG 1K P5 (BNKB)
M041
DR041 4H9
DR051 4J9
07J-A 07JRG 1K P5 (BNKA)
M051
M141 5G2
A060 114-1
A070 214-1
M151 5G1
GM1 1N9
DR061 4K9
DR071 4K9
GCA1 1B9
06V 19-057 SG
06T 19-057 SG
07S 19-056 SGO
06S 19-056 SGO
07M 19-056 SGO
06M 19-056 SGO
07K 19-056 SGO
06K 19-056 SGO
07J 19-056 SGO
06J 19-056 SGO
S080 107-1
S090 207-1
S000 103-1
S010 203-1
S100 108-1
S110 208-1
S020 104-1
S030 204-1
S120 109-1
S130 209-1
S040 105-1
S050 205-1
S140 110-1
S150 210-1
S060 106-1
S070 206-1

REVISIONS

AT LOC L2, ADDED GATES 15C03, 14K11 & 14J12 & ASSOC LEADS, GDR130 WAS DR130; AT LOC J7, DELETED:



FSR1
05
06J 19-056
06
S130
FLSYNO
01
02
06J 19-056
03
04
330
OWR5
P5

7	L.M.	3215-20		10-11-72	R05

AT LOC L2, IC 15C WAS 19-055.

7	L.M.	3215-27		12-5-72	R07

NOTES

NAME	TITLE	DATE
E. ROE	DRAFT	6-5-72
7	CHK	
	ENGR	
	DIR ENG	

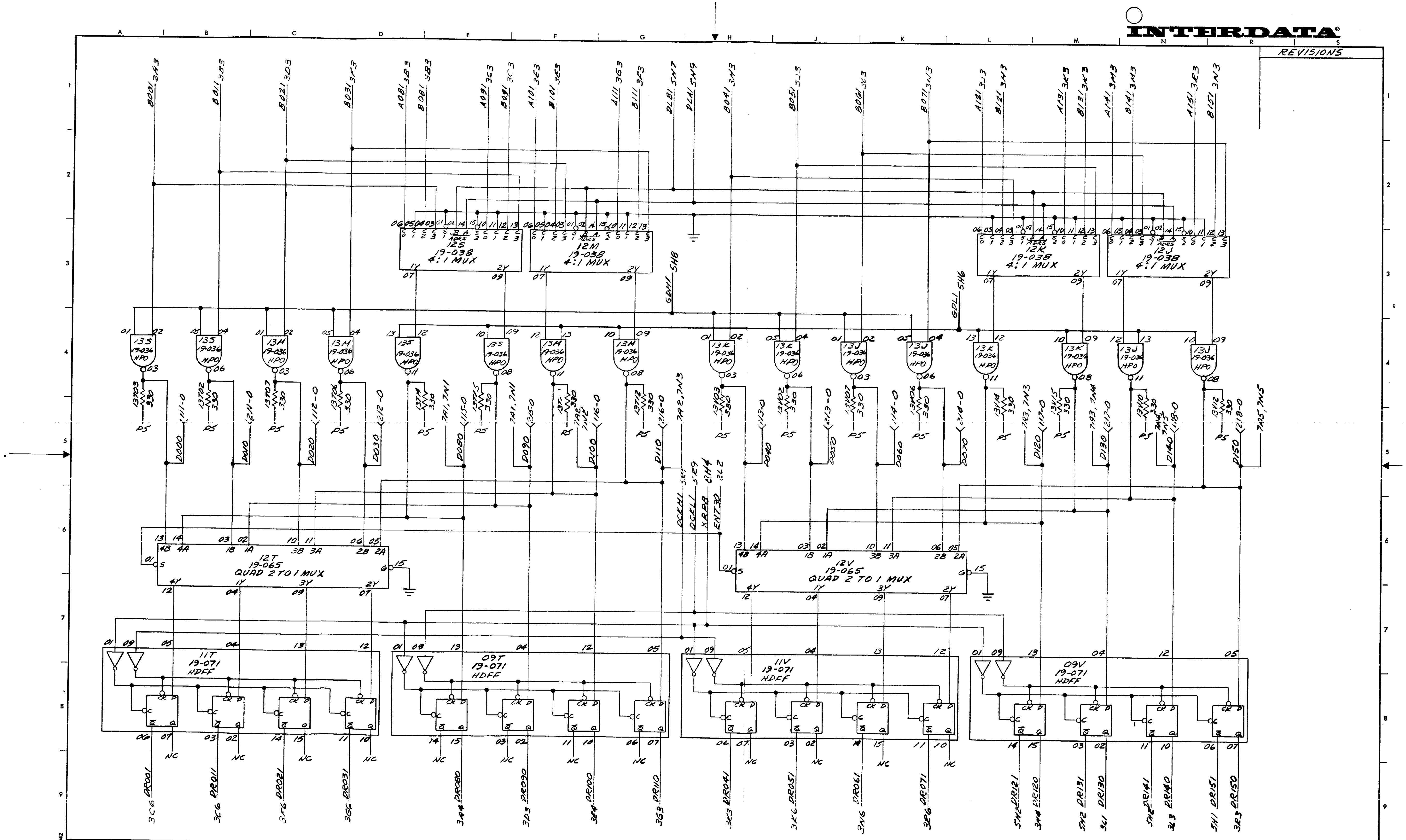
TITLE FUNCTIONAL SCHEMATIC
MODEL 80 IOU

TASK NO. 03215
DWG NO. 35-405 R07D08
SHEET 3 OF —

BRUNING 44-231 16042

INTERDATA®

REVISIONS


B001 3A3
B011 3B3
B021 3D3
B031 3F3
A081 3B3
B081 3B3
A091 3C3
B091 3C3
A101 3E3
B101 3E3
A111 3G3
B111 3F3
DLB1 5H7
DLA1 5H9
B041 3H3
B051 3J3
B061 3L3
B071 3N3
A121 3J3
B121 3H3
A131 3K3
B131 3K3
A141 3M3
B141 3M3
A151 3R3
B151 3N3
12S 19-038 4:1 MUX
12M 19-038 4:1 MUX
12K 19-038 4:1 MUX
12J 19-038 4:1 MUX
ADRS
GDH1 5H8
GDL1 5H6
13S 19-036 HPO
13M 19-036 HPO
13K 19-036 HPO
13J 19-036 HPO
330
P5
D000
D010
D020
D030
D080
D090
D100
D110
D040
D050
D060
D070
D120
D130
D140
D150
111-0
211-0
112-0
212-0
115-0
215-0
116-0
216-0
113-0
213-0
114-0
214-0
117-0
217-0
118-0
218-0
7A1, 7N1
7A2, 7N2
7A3, 7N4
7A4, 7N3
7A5, 7N5
DCKH1 5E9
DCKL1 5E9
XRPB 8H4
ENT30 2L2
12T 19-065 QUAD 2 TO 1 MUX
12V 19-065 QUAD 2 TO 1 MUX
11T 19-071 HDFF
09T 19-071 HDFF
11V 19-071 HDFF
09V 19-071 HDFF
CK D
NC
DR001 3C6
DR011 3C6
DR021 3F6
DR031 3G6
DR080 3A4
DR090 3D3
DR100 3E4
DR110 3G3
DR041 3K3
DR051 3K6
DR061 3N6
DR071 3P6
DR121 5H2
DR120 3A4
DR131 5H2
DR130 3C1
DR141 5H2
DR140 3L3
DR151 5H1
DR150 3R3

BRUNING 44-231 16042

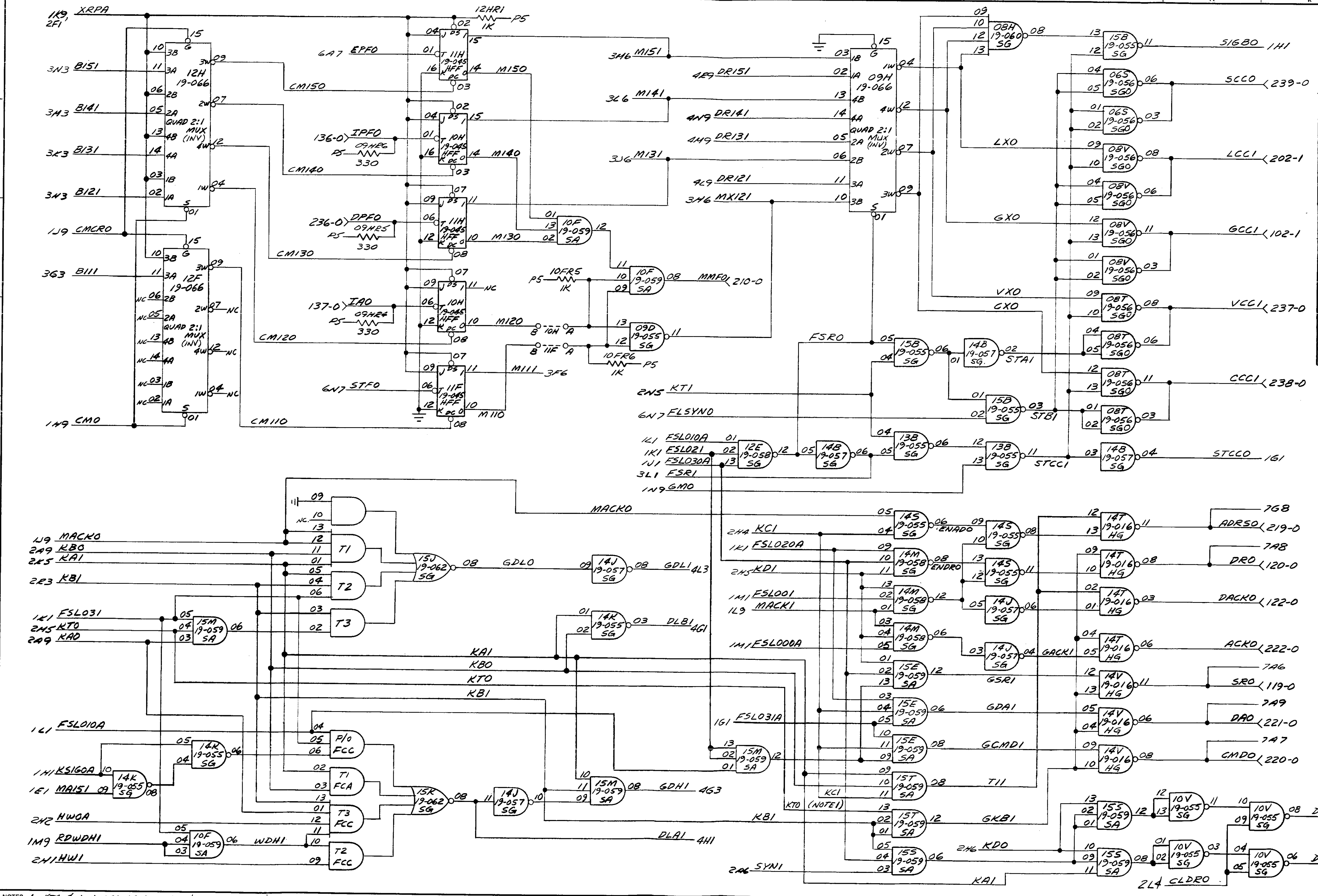
NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 80 IOU

TASK NO 03215
DWG NO 35-405 R01 D08
SHEET 4 OF -

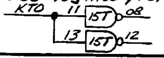
INTERDATA®



1K9 XRPA 2F1
3N3 BI51
3H3 BI41
3K3 BI31
3N3 BI21
1J9 CMCRO
3G3 BI11
1N9 CMO
12H 19-066 QUAD 2:1 MUX (INV)
12F 19-066 QUAD 2:1 MUX (INV)
CM150
CM140
CM130
CM120
CM110
12HRI 1K P5
6A7 EPFO
136-0 IPFO
236-0 DPFO
137-0 IAO
6N7 STFO
09HR6 330
09HR5 330
09HR4 330
11H 19-045 HFF
10H 19-045 HFF
11F 19-045 HFF
M150
M140
M130
M120
M111 3F6
M110
10F 19-059 SA
10FR5 1K
10FR6 1K
MMFO 210-0
09D 19-055 SG
3H6 MI51
4E9 DRI51
3L6 MI41
4N9 DRI41
4H9 DRI31
3J6 MI31
4L9 DRI21
3H6 MXI21
09H 19-066 QUAD 2:1 MUX (INV)
08H 19-060 SG
15B 19-055 SG
SIGBO 1H1
SCCO 239-0
LXO
LCCI 202-1
GXO
GCCI 102-1
VXO
CXO
VCCI 237-0
CCCI 238-0
FSRO
STAI
STBI
STCCI
STCCO 1G1
2N5 KTI
6N7 ELSYNO
1K1 FSL010A
1K1 FSL021
1J1 FSL030A
3L1 FSRI
1N9 GMO
12E 19-058 SG
14B 19-057 SG
13B 19-055 SG
MACKO
1J9 MACKO
2A9 KBO
2K5 KAI
2E3 KBI
T1
T2
T3
15J 19-062 SG
GDLO
14J 19-057 SG
GDLI 4L3
1K1 FSL031
2M5 KTO
2A9 KAO
15M 19-059 SA
14K 19-055 SG
DLBI 4G1
KAI
KBO
KTO
KBI
1L1 FSL010A
1H1 KSIGOA
1E1 MAIS1
2H2 HWOA
1M9 RDWDHI
2N1 HWI
P/O FCC
T1 FCA
T3 FCC
T2 FCC
WDHI
15K 19-062 SG
GDHI 4G3
DLAI 4H1
1G1 FSL031A
KTO (NOTE 1)
KCI
2H4 KCI
1K1 FSL020A
2H5 KDI
1M1 FSL001
1L9 MACKI
1M1 FSL000A
14S 19-055 SG
14M 19-058 SG
15E 19-059 SA
15T 19-059 SA
15S 19-059 SA
ENADO
ENDRO
GACKI
GSRI
GDAI
GCMDI
TII
GKBI
2H6 KDO
2A6 SYNI
2L4 CLDRO
14T 19-016 HG
14V 19-016 HG
ADRSO 219-0 7G8
DRO 120-0 7A8
DACKO 122-0
ACKO 222-0
SRO 119-0 7A6
DAO 221-0 7A9
CMDO 220-0 7A7
10V 19-055 SG
DCKLI 4H5
DCKHI 4G5

REVISIONS					
CHANGED 15T (19-059) INTO 14M (19-058) AND ADDED GATE 14J ON OUTPUT (GACKI) IN AREA K7. REMOVED CO-ORDINATION ON ACKO TO SHT. 8 IN AREA R7					
DB	JM	ECR 3215-11		7-31-72	R02
AT B9, ADDED 10F06 GATE; 15K10 & 11 WERE TO RDWDHI					
7	JM	3215-18		10-3-72	R04
AT N9, ADDED 10V03, 06, 08 & 11; 15S12 WAS TO DCKLI & 15S08 WAS TO DCKHI					
7	JM	3215-20		10-11-72	R05
AT LOC M6-M8, IC 14V & 14T WERE 19-036 W/ 330Ω PULLUPS TO P5 ON ALL OUTPUTS.					
7	JM	3215-27		12-5-72	R07
AT LOC J9, 15T11 WAS P/O KTO; ADDED NOTE 1.					
7	RFS	3215-28		2-22-73	R09

NOTES 1. KTO & KCI APPEAR AS SHOWN ONLY ON 35-405 M01 & F01 M01 (25-368); CIRCUIT APPEARS ON 35-405 M00 & F01 M00 (25-297) THUS:



KTO
11
15T
08
13
15T
12

NAME	TITLE	DATE
	DRAFT	
7	CHK	
	ENGR	
	DIR ENG	

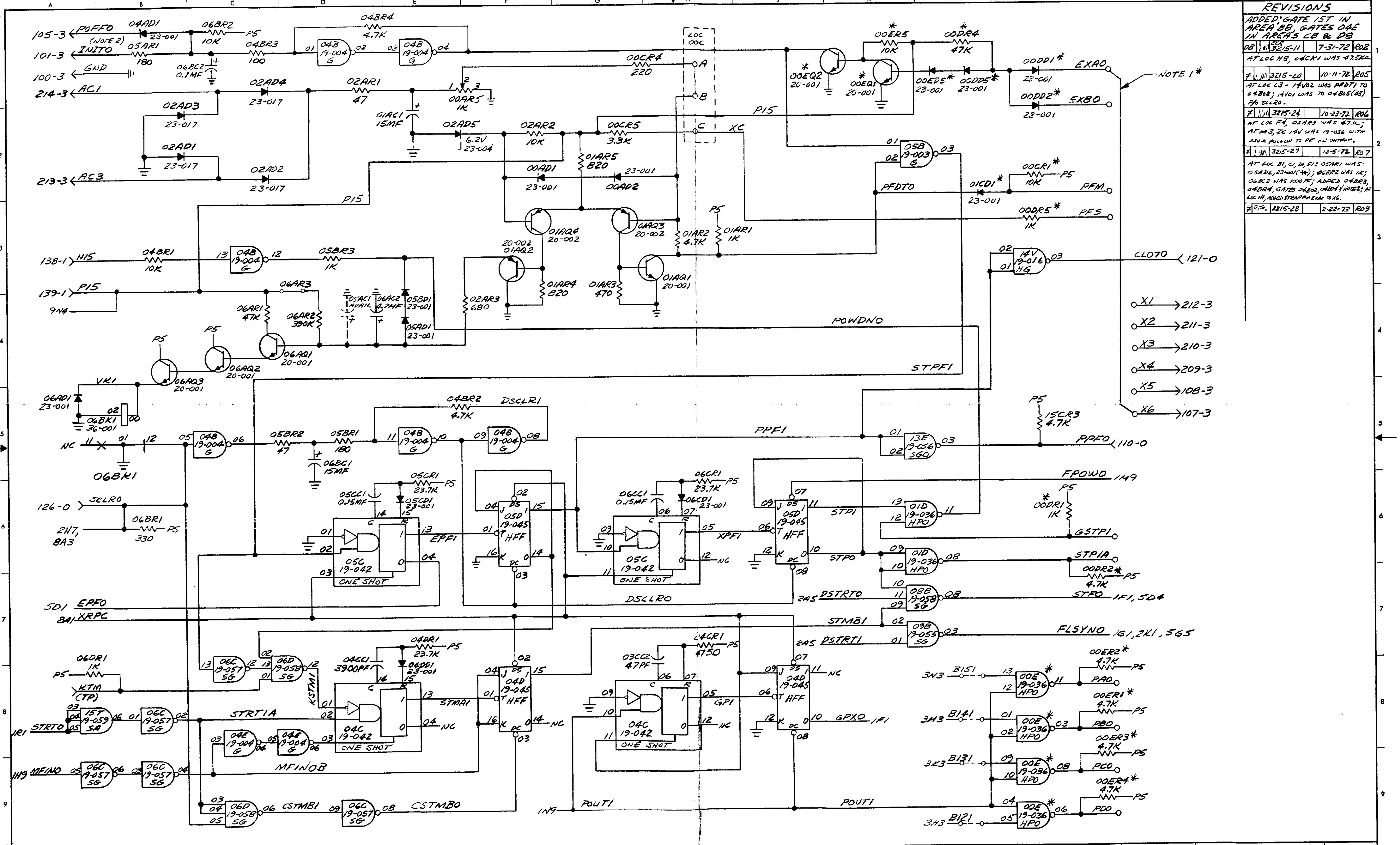
TITLE FUNCTIONAL SCHEMATIC MODEL 80 IOU

TASK NO. 03215

DWG NO. 35-405R09D08

SHEET 5 OF

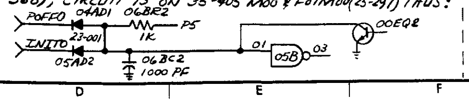
BRUNING 44-231 16042


105-3 POFFO
04AD1 23-001
06BR2 10K
P5
(NOTE 2)
101-3 INITO
05AR1 180
100-3 GND
06BC2 0.1MF
04BR3 100
04BR4 4.7K
04B 19-004 G
214-3 AC1
02AD4 23-017
02AR1 47
00AR5 1K
00CR4 220
LOC OOC
A
B
C
01AC1 15MF
02AD3 23-017
02AD1 23-017
213-3 AC3
02AD2 23-017
02AD5 6.2V 23-004
02AR2 10K
00CR5 3.3K
P15
XC
01AR5 820
00AD1 23-001
00AD2 23-001
01AQ4 20-002
01AQ3 20-002
01AR2 4.7K
01AR1 1K
01AQ2 20-002
01AQ1 20-001
01AR4 820
01AR3 470
02AR3 680
138-1 N15
04BR1 10K
05BR3 1K
139-1 P15
9N4
06AR3
06AR1 47K
06AR2 390K
05AC1 AVAIL
06AC2 4.7MF
05BD1 23-001
05AD1 23-001
06AQ1 20-001
06AQ2 20-001
06AQ3 20-001
VK1
06AD1 23-001
06BK1 36-001
POWDNO
STPF1
00ER5 10K
00DR4 47K
00EQ2 20-001
00EQ1 20-001
00ED5 23-001
00DD5 23-001
00DD1 23-001
EXA0
00DD2 23-001
EXB0
NOTE 1
05B 19-003 G
PFDTO
01CD1 23-001
00CR1 10K
PFM
00DR5 1K
PFS
14V 19-016 HG
CL0TO 121-0
X1 212-3
X2 211-3
X3 210-3
X4 209-3
X5 108-3
X6 107-3
NC
06BK1
05BR2 47
05BR1 180
06BC1 15MF
04BR2 4.7K
DSCLR1
PPF1
13E 19-056 SGO
15CR3 4.7K
PPF0 110-0
126-0 SCLRO
06BR1 330
2H7, 8A3
05CC1 0.15MF
05CR1 23.7K
05CD1 23-001
EPF1
05C 19-042 ONE SHOT
05D 19-045 HFF
06CC1 0.15MF
06CR1 23.7K
06CP1 23-001
XPF1
DSCLRO
STP1
STP0
FPOWO 1M9
01D 19-036 HPO
00DR1 1K
GSTP1
STP1A
00DR2 4.7K
08B 19-058 SG
2A5 DSTRTO
STFO 1F1, 5D4
STMB1
09B 19-055 SG
2A5 DSTRT1
FLSYNO 1G1, 2K1, 5G5
5D1 EPFO
8A1 XRPC
06DR1 1K
KTM (TP)
06C 19-057 SG
06D 19-058 SG
04CC1 3900PF
04DR1 23.7K
04DD1 23-001
KSTM1
STMA1
04C 19-042 ONE SHOT
04D 19-045 HFF
03CC2 47PF
04CR1 4750
GP1
GPXO 1F1
1R1 STRTO
15T 19-059 SA
STRT1A
04E 19-004 G
MFINOB
1H9 MFINO
CSTMB1
CSTMBO
1N9
POUT1
3N3 B151
00E 19-036 HPO
00ER2 4.7K
PAO
3M3 B141
00ER1 4.7K
PBO
3K3 B131
00ER3 4.7K
PCO
3H3 B121
00ER4 4.7K
PDO

REVISIONS					
ADDED; GATE 15T IN AREA B8, GATES 04E IN AREA'S C8 & D8					
D8		ECR 3215-11		7-31-72	R02
AT LOC H8, 04CR1 WAS 47.5KΩ					
7		3215-20		10-11-72	R05
AT LOC L3 - 14V02 WAS PFDT1 TO 04B02; 14V01 WAS TO 04B05(B5) P/O SCLRO.					
7		3215-24		10-23-72	R06
AT LOC F4, 02AR3 WAS 47Ω; AT M3, IC 14V WAS 19-036 WITH 330Ω PULLUP TO P5 ON OUTPUT.					
7		3215-27		12-5-72	R07
AT LOC B1, C1, D1, E1: 05AR1 WAS 05AD2, 23-001(→); 06BR2 WAS 1K; 06BC2 WAS 1000 PF; ADDED 04BR3, 04BR4, GATES 04B02, 04B04 & NOTE 2; AT LOC N1, ADDED STRAP FM EXA0 TO X6.					
7		3215-28		2-22-73	R09

NOTES 1. ASTERISK * INDICATES COMPONENT NOT NORMALLY EQUIPPED ON 35-405M00 & F01M00; CIRCUIT ALWAYS APPEARS ON 35-405M01 & F01M01.

2. INITO CIRCUIT APPEARS ONLY ON 35-405M01 & F01M01 (25-368); CIRCUIT IS ON 35-405M00 & F01M00(25-297) THUS:

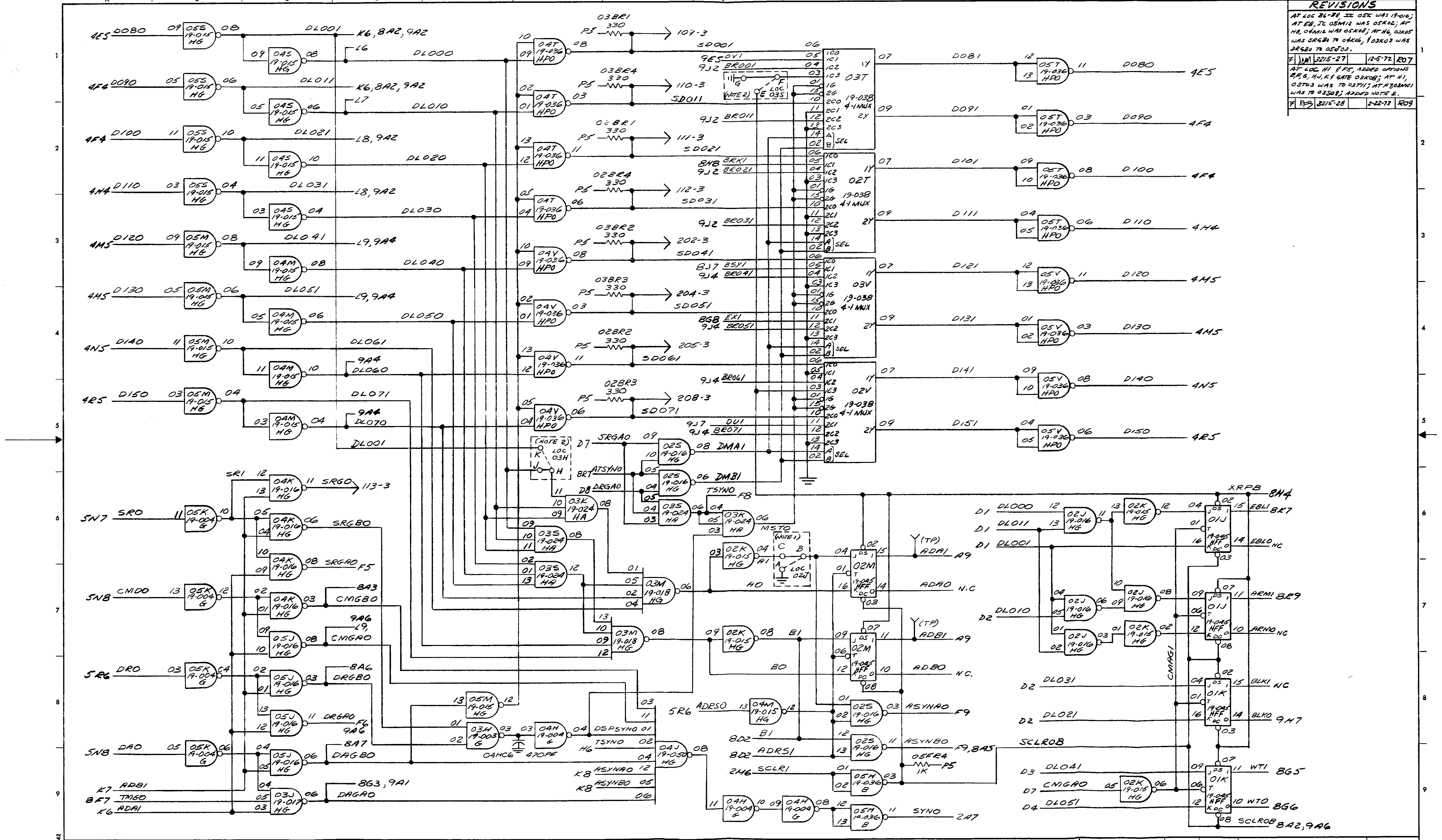

POFFO
04AD1
06BR2
P5
1K
INITO
23-001
05AD2
06BC2 1000 PF
01
05B
03
00EQ2

NAME	TITLE	DATE
	DRAFT	
Z	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 80 IOU

TASK NO. 03215
DWG NO. 35-405R09D08
SHEET 6 OF –

INTERDATA®



4E5 D080
4F4 D090
4F4 D100
4H4 D110
4M5 D120
4M5 D130
4N5 D140
4R5 D150
05S 19-015 HG
04S 19-015 HG
05M 19-015 HG
04M 19-015 HG
DL001 K6, 8A2, 9A2
DL000
DL011 K6, 8A2, 9A2
DL010
DL021 L8, 9A2
DL020
DL031 L8, 9A2
DL030
DL041 L9, 9A4
DL040
DL051 L9, 9A4
DL050
DL061
9A4 DL060
DL071
9A4 DL070
DL001
04T 19-036 HPO
04V 19-036 HPO
03BR1 P3 330 107-3 SD001
03BR4 P5 330 110-3 SD011
02BR1 P5 330 111-3 SD021
02BR4 P5 330 112-3 SD031
03BR2 P5 330 202-3 SD041
03BR3 P5 330 204-3 SD051
02BR2 P5 330 205-3 SD061
02BR3 P5 330 208-3 SD071
9E5 DV1
9J2 BR001
9J2 BR011
8H8 BRK1
9J2 BR021
9J2 BR031
8J7 BSY1
9J4 BR041
8G8 EX1
9J4 BR051
9J4 BR061
9J7 DU1
9J4 BR071
(NOTE 2) G F LOC E 03S
03T 19-038 4-1 MUX
02T 19-038 4-1 MUX
03V 19-038 4-1 MUX
02V 19-038 4-1 MUX
1Y 2Y SEL A B
D081 D091 D101 D111 D121 D131 D141 D151
05T 19-036 HPO
05V 19-036 HPO
(NOTE 2) K LOC 03H J H
D7 SRGA0
8R1 ATSYNO
D8 DRGA0
02S 19-016 HG
08 DMA1
06 DMB1
03S 19-024 HA
TSYNO F8
03K 19-024 HA
MSTO
SR1
5N7 SR0
05K 19-004 G
04K 19-016 HG
11 SRG0 113-3
SRGB0
SRGA0 F5
5N8 CMD0
8A3 CMGB0
9A6 L9 CMGA0
05J 19-016 HG
5R6 DR0
8A6 DRGB0
F6 9A6 DRGA0
5N8 DA0
8A7 DAGB0
8G3, 9A1 DAGA0
K7 ADB1
8F7 TMGO
K6 ADA1
03J 19-017 HG
03M 19-018 HG
A0
02K 19-015 HG
(NOTE 1) C B A LOC 02J
02M 19-045 HFF
Y (TP) ADA1 A9
ADA0 N.C
Y (TP) ADB1 A9
ADB0 N.C.
B1 B0
05M 19-015 HG
03H 19-003 G
04H 19-004 G
04HC6 470PF
DSPSYNO
TSYNO H6
K8 ASYNA0
K8 ASYNB0
04J 19-050 HG
5R6 ADES0
04M 19-015 HG
8D2 B1
8D2 ADRS1
2H6 SCLR1
02S 19-016 HG
ASYNA0 F9
ASYNB0 F9, 8A5
05FR4 1K P5
05H 19-036 B
04H 19-004 G
SYNO 2A7
XRPB 8H4
D1 DL000
D1 DL011
D1 DL001
02J 19-016 HG
02K 19-015 HG
01J 19-045 HFF
EBL1 8K7
EBL0 NC
D2 DL010
ARM1 8R9
ARM0 NC
CMAG1
D2 DL031
D2 DL021
01K 19-045 HFF
BLK1 NC
BLK0 9H7
SCLROB
D3 DL041
D7 CMGA0
D4 DL051
WT1 8G5
10 WT0 8G6
08 SCLROB 8A2, 9A6

REVISIONS

AT LOC B6-B8, IC 05K WAS 19-016; AT E8, IC 05M12 WAS 05K02; AT H8, 04M12 WAS 05K08; AT H6, 03K05 WAS SRGB0 TO 04K06, & 03K03 WAS DRGB0 TO 05J03.

7	JWM	3215-27		12-5-72	R07

AT LOC H1 & F5, ADDED OPTIONS E,F,G, H,J,K & GATE 03K08; AT H1, 03T03 WAS TO 03T11; AT F7, 03M01 WAS TO 03S08; ADDED NOTE 2.

7	RFB	3215-28		2-22-73	R09

NOTES
1. SOLID CONNECTION FOR NORMAL TTY CONTROLLER; DASHED OPTION WHEN DEVICE ADDRESS X'02' IS USED FOR ANOTHER I/O CONTROLLER; APPEARS ONLY ON 35-405M00 & F01M00 (25-297).
2. OPTIONS E,F,G & H,J,K & GATE 03K08 APPEAR ONLY ON 35-405M01 & F01M01; ADDRESS '02' IS CHANGED TO '82' WITH DASHED OPTION.

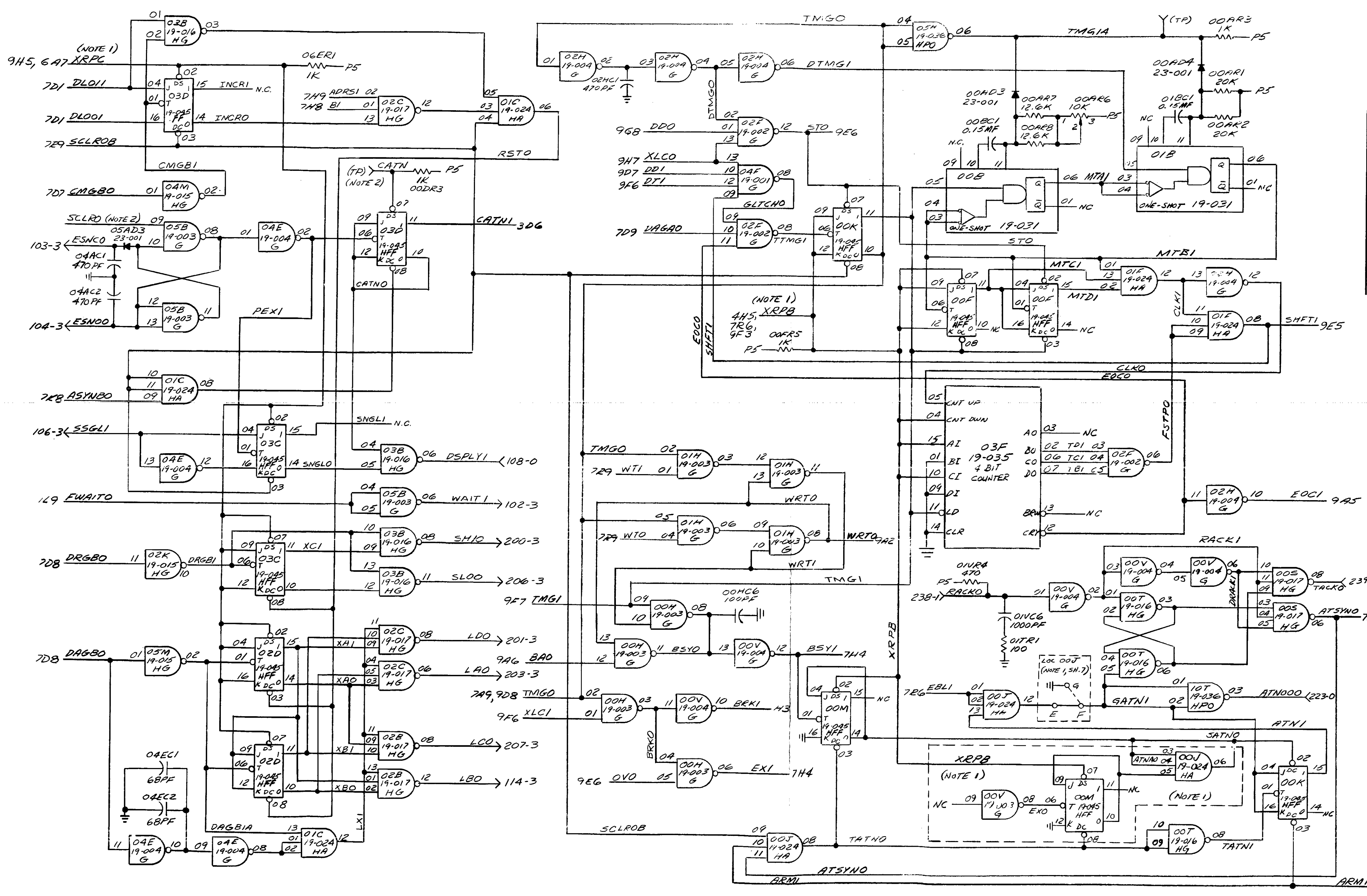
NAME	TITLE	DATE
P.EDWARDS	DRAFT	7-17-72
7	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 80 IOU

TASK NO. 03215
DWG NO. 35-405R09D08
SHEET 7- OF

BRUNING 44-231 16042

INTERDATA®



(NOTE 1)
9H5, 6A7 XRPC
7D1 DL011
7D1 DL001
7E9 SCLR0B
02B 19-016 HG
03D 19-045 FF
INCR1 N.C.
INCR0
06ER1 1K P5
7H9 ADRS1
7H8 B1
02C 19-017 HG
01C 19-024 HA
RSTO
CMGB1
7D7 CMGB0
04M 19-015 HG
SCLR0 (NOTE 2)
05AD3 23-001
103-3 ESNC0
04AC1 470PF
04AC2 470PF
104-3 ESN00
05B 19-003 G
04E 19-004 G
(TP) CATN 1K 00DR3 P5
(NOTE 2)
03D 19-045 HFF
CATN1 3D6
CATN0
PEX1
7K8 ASYNB0
01C 19-024 HA
106-3 SSGL1
03C 19-045 HFF
SNGL1 N.C.
SNGL0
03B 19-016 HG
DSPLY1 108-0
1L9 FWAIT0
05B 19-003 G
WAIT1 102-3
7D8 DRGB0
02K 19-015 HG
DRGB1
XC1
SH10 200-3
SL00 206-3
7D8 DAGB0
05M 19-015 HG
02D 19-045 HFF
XA1
XA0
XB1
XB0
02C 19-017 HG
LD0 201-3
LA0 203-3
02B 19-017 HG
LC0 207-3
LB0 114-3
04EC1 68PF
04EC2 68PF
DAGB1A
LX1
TMG0
02H 19-004 G
02HC1 470PF
DTMG1
DTMG0
9G8 DD0
STO 9E6
9H7 XLC0
9D7 DD1
9F6 DT1
04F 19-001 G
02F 19-002 G
GLTCH0
7D9 VAGA0
TTMG1
00K 19-045 HFF
(NOTE 1)
4H5, 7R6, 9F3 XRPB
00FR5 1K
P5
EOC0
SHFT1
05H 19-036 HP0
TMG1A
(TP)
00AR3 1K P5
00AD4 23-001
00AR1 20K
00AD3 23-001
00AR7 12.6K
00AR6 10K
00AR8 12.6K
00BC1 0.15MF
01BC1 0.15MF
00AR2 20K
N.C.
00B
ONE-SHOT 19-031
01B
MTA1
STO
MTC1
MTB1
00F 19-045 HFF
MTD1
01F 19-024 HA
CLK1
SHFT1 9E5
CLK0
EOC0
FSTP0
03F 19-035 4 BIT COUNTER
CNT UP
CNT DWN
TD1
TC1
TB1
02F 19-002 G
02H 19-009 G
EOC1 9A5
7Z9 WT1
01H 19-003 G
WRT0
7Z9 WT0
WRT0 9A2
WRT1
TMG1
9F7 TMG1
00H 19-003 G
00HC6 100PF
BSY0
00V 19-004 G
BSY1 7H4
7A9, 9D8 TMG0
9F6 XLC1
BEK1 H3
BRK0
EX1 7H4
9E6 OV0
SCLR0B
00J 11-024 HA
TATN0
ATSYN0
ARM1
ARM1 7R7
XRPB
00M 19-045 HFF
01VR4 470
P5
238-1 RACK0
01VC6 1000PF
01TR1 100
RACK1
00V 19-004 G
00T 19-016 HG
DRACK1
00S 19-017 HG
TACK0 239-1
ATSYN0 7F6
7E6 EBL1
00J 19-024 HA
LOC 00J (NOTE 1, SH.7)
G
E
F
GATN1
10T 19-036 HP0
ATN000 223-0
SATN0
ATN1
ATNA0
(NOTE 1)
EX0
00K 19-045 HFF
TATN1

REVISIONS

REMOVED 1000PF CAPS 04AC1 & 04AC2 IN AREA A3 FROM 103-3 & 104-3 TO GND. REMOVED STAKES 01V-A ON ACKO, 01V-B ON 00V-01, 01V-C ON RACKO. REMOVED ACKO CO-ORDINATION TO SHT. 5R7. ADDED 01VC6 & 01TR1 IN AREA K7

DB		ECR 3215-11		7-31-72	R02

AT H9 - 00V09 WAS TO 00H06 (EX1); REMOVED 00V08, 00J06 & 00M-FF.

7		3215-14		8-23-72	R03

AT A3 - ADDED 05AD3, 04AC1 & C2

7		3215-20		10-11-72	R05

AT LOC D3, 03D07 WAS A/O XRPC - ADDED TP 'CATN' & 00DR3; AT LOC A3, 05B09 WAS TO 05B10 - ADDED CONN TO 'SCLRO'; AT LOC N8, ADDED DIRECT CONN 'SATNO' 00K02 TO 00M14; ADDED NOTES 1 & 2.

7	RFS	3215-28		2-22-73	R09

NOTES 1. GATED SATNO APPEARS ONLY ON 35-405M00 & F01M00 (25-297); DIRECT CONNECTION IS MADE ONLY ON 35-405M01 & F01M01 (25-368).

2. TEST POINT 'CATN' & SCLRO CONN (05B09) APPEAR ONLY ON 35-405M01 & F01M01 (25-368); 05B09 IS CONN. TO ESNCO (05B10) ON 35-405M00 & F01M00.

NAME	TITLE	DATE
P. EDWARDS	DRAFT	7-13-72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC MODEL 80 IOU

TASK NO. 03215

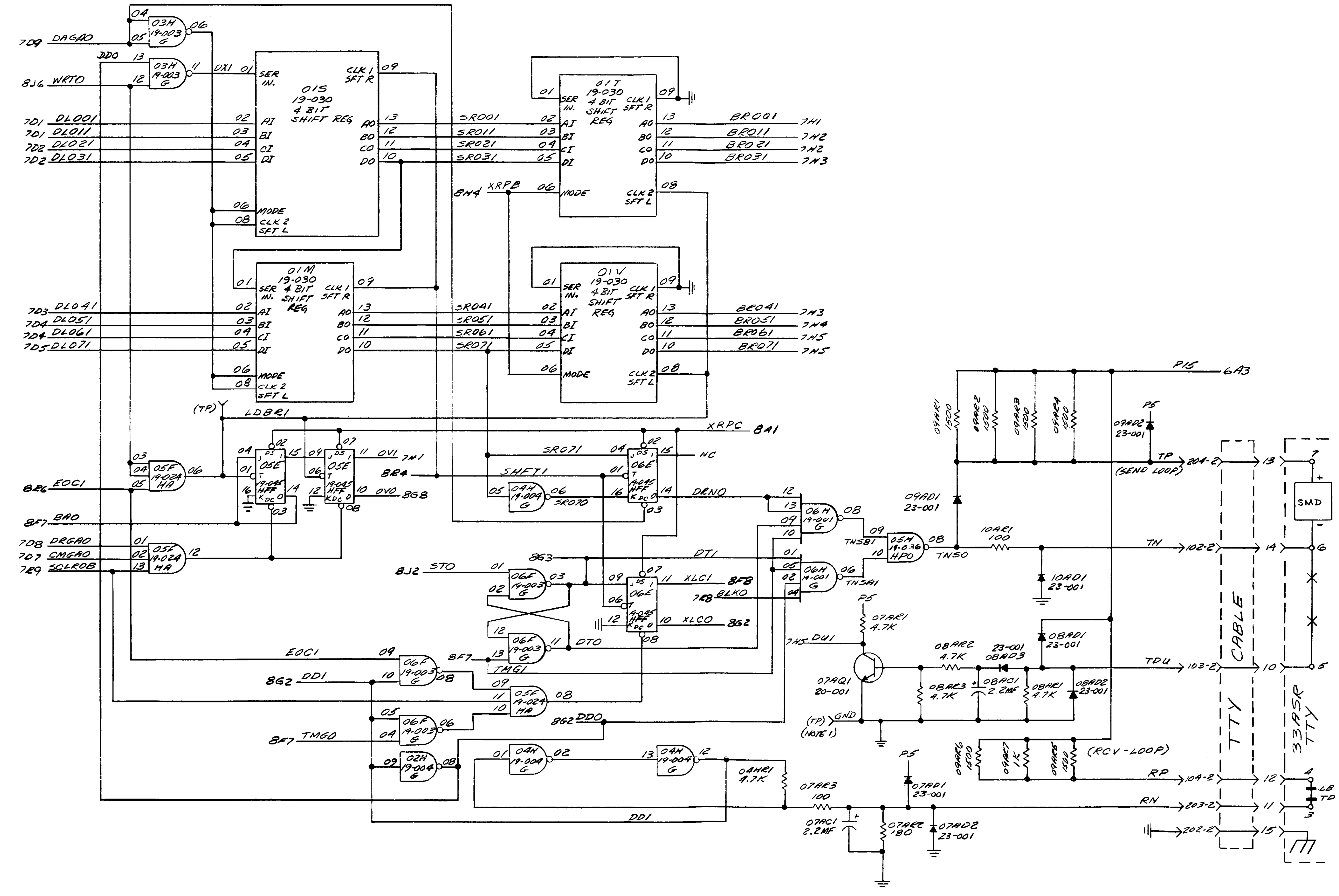
DWG NO. 35-405R09 D08

SHEET 8 OF -

BRUNING 44-231 16042

INTERDATA®

REVISIONS					
ADDED GATE 02H IN AREA E8, REMOVED CONNECTION TO DDO FROM 04H PINS 02 & 13					
DB	JM	ECR 3215-11		7-31-72	R02
AT LOC J8, ADDED (TP) GND AND ASSOC NOTE 1.					
7	RES	3215-28		2-22-73	R09



7D9 DAGAO
8J6 WRTO
DDO
03H 19-003 G
01S 19-030 4 BIT SHIFT REG
SER IN.
CLK 1 SFT R
AI BI CI DI
AO BO CO DO
MODE
CLK 2 SFT L
DX1
7D1 DL001
7D1 DL011
7D2 DL021
7D2 DL031
SR001 SR011 SR021 SR031
01T 19-030 4 BIT SHIFT REG
BR001 7H1
BR011 7H2
BR021 7H2
BR031 7H3
8H4 XRPB
01M 19-030 4 BIT SHIFT REG
7D3 DL041
7D4 DL051
7D4 DL061
7D5 DL071
SR041 SR051 SR061 SR071
01V 19-030 4 BIT SHIFT REG
BR041 7H3
BR051 7H4
BR061 7H5
BR071 7H5
(TP) LDBR1
XRPC 8A1
8E6 EOC1
05F 19-024 HA
05E 19-045 HFF
OV1 7H1
8E4
OVO 8G8
8F7 BAO
7D8 DRGAO
7D7 CMGAO
7E9 SCLROB
SR071
SHFT1
04H 19-004 G
SR070
06E 19-045 HFF
NC
DRNO
06H 19-001 G
TNSB1
05H 19-036 HPO
TNSO
TNSA1
8J2 STO
8G3
06F 19-003 G
DT1
XLC1 8F8
7E8 BLKO
XLCO 8G2
DTO
TMG1
EOC1
8F7
8G2 DD1
8G2 DDO
8F7 TMGO
02H 19-004 G
7H5 DU1
07AQ1 20-001
07AR1 4.7K
P5
(TP) GND (NOTE 1)
08AR2 4.7K
23-001 08AD3
08AR3 4.7K
08AC1 2.2MF
08AR1 4.7K
08AD1 23-001
08AD2 23-001
P15 6A3
09AR1 1500
09AR2 1500
09AR3 1500
09AR4 1500
09AD2 23-001
09AD1 23-001
TP (SEND LOOP)
10AR1 100
10AD1 23-001
TN
TDU
09AR6 1500
09AR7 1K
09AR8 1500
(RCV-LOOP)
RP
RN
04HR1 4.7K
07AR3 100
07AC1 2.2MF
07AR2 180
07AD1 23-001
07AD2 23-001
DD1
204-2
102-2
103-2
104-2
203-2
202-2
TTY CABLE
13 14 10 12 11 15
7 6 5 4 3
SMD
LB TD
33ASR TTY

NOTES / 1. TEST POINT 'GND' APPEARS ONLY ON 35-405M01 & F01M01 (25-368)

NAME	TITLE	DATE
P.EDWARDS	DRAFT	7-14-72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 80 IOU

TASK NO. 03215
DWG NO. 35-405R09D08
SHEET 9 OF -

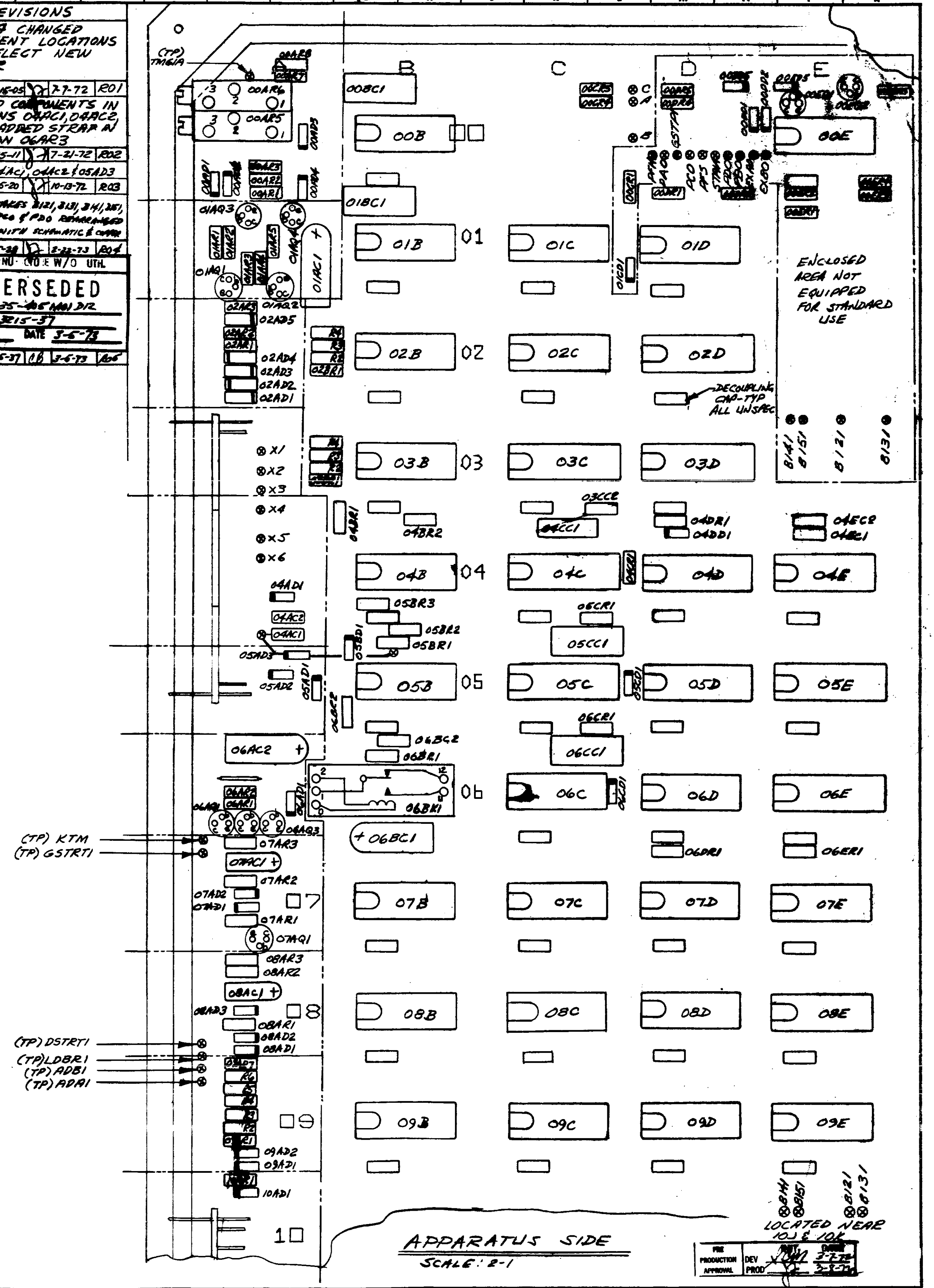
BRUNING 44-231 16042

INTERDATA

REVISIONS					
ADDED & CHANGED COMPONENT LOCATIONS TO REFLECT NEW COPPER					
08	AW	3215-05		7-7-72	R01
REMOVED COMPONENTS IN POSITIONS 04AC1, 04AC2, 06AR3. ADDED STRAP IN POSITION 06AR3					
08		3215-11		7-21-72	R02
ADDED 04AC1, 04AC2 & 05AD3					
		3216-20		10-13-72	R03
OPTION STAKES B121, B131, B141, B151, PA0, PB0, PC0 & PD0 REARRANGED TO AGREE WITH SCHEMATIC & CHART					
7		3215-28		2-22-73	R04
7		3216-37	CB	3-6-73	R05

DO NOT MANUFACTURE W/O AUTH.

SUPERSEDED
BY PART NO. 35-405 M01 D12
PER ECN NO. 3215-37
BY
DATE 3-6-73



A
B
C
D
E
F
G
H
J
K
L
M
N
P
R
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
(TP) TMGIA
00AR6
00AR5
00AR8
00BC1
00B
01BC1
B
C
D
E
00E
01B
01C
01D
01
01AC1
01AQ1
01AQ2
01AQ3
02AR5
02AD4
02AD3
02AD2
02AD1
02B
02C
02D
02
DECOUPLING CAP-TYP ALL UNSPEC
ENCLOSED AREA NOT EQUIPPED FOR STANDARD USE
B141
B151
B121
B131
X1
X2
X3
X4
X5
X6
03B
03C
03D
03
03CC2
04CC1
04DR1
04DD1
04EC2
04EC1
04BR2
04AD1
04AC2
04AC1
04B
04C
04D
04E
04
05BR3
05BR2
05BR1
05AD3
05AD2
05AD1
05CR1
05CC1
05B
05C
05D
05E
05
06AC2
06BC2
06BR1
06CR1
06CC1
06BK1
06B
06C
06D
06E
06
06AQ1
06AQ2
06AQ3
06BC1
06DR1
06ER1
(TP) KTM
(TP) GSTRT1
07AR3
07AC1
07AR2
07AD2
07AD1
07AR1
07AQ1
07B
07C
07D
07E
07
08AR3
08AR2
08AC1
08AD3
08AR1
08AD2
08AD1
08B
08C
08D
08E
08
(TP) DSTRT1
(TP) LDBR1
(TP) ADB1
(TP) ADA1
09AD2
09AD1
10AD1
09B
09C
09D
09E
09
10
B141
B151
B121
B131
LOCATED NEAR 10J & 10K

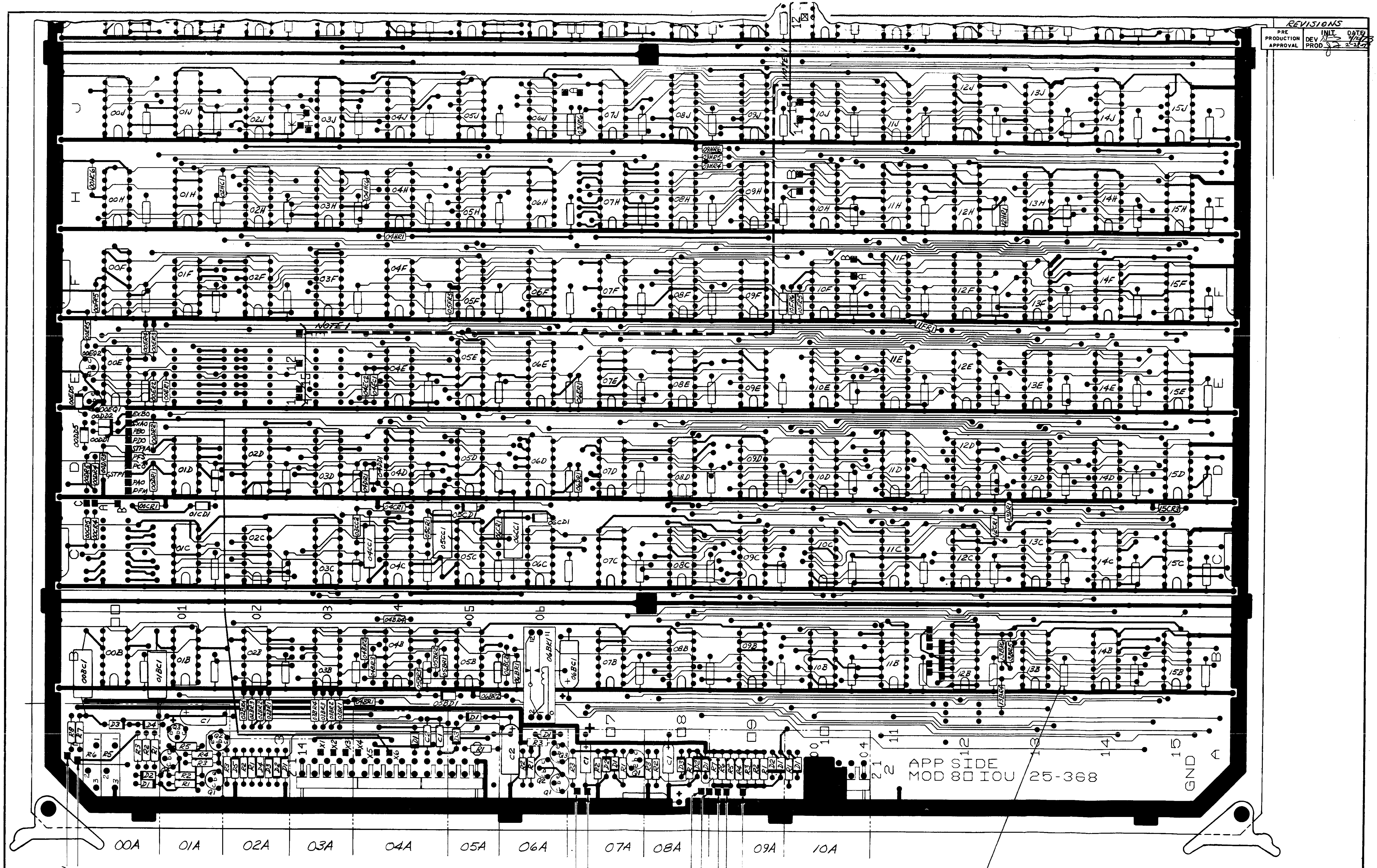
APPARATUS SIDE

SCALE: 2-1

PRE PRODUCTION APPROVAL		INIT.	DATE
	DEV		3-7-73
	PROD		3-8-73

NOTES

NAME	TITLE	DATE		
	DRAFT	3-3-72	TITLE INFORMATION REFERENCE DESIGNATIONS MODEL 80 IOU	
J.F. FLEMING	CHK	6-30-72		
S. MESSINA	ENGR			
M. FUCHS	Q.C.		TASK NO. 03215	SHEET OF
R.E. JONES	DIR. ENG.		DWG. NO. 35-405R08F12	1-1


APP SIDE
MOD 8□ IOU 25-368
J
H
F
E
D
C
B
A
GND
00J
01J
02J
03J
04J
05J
06J
07J
08J
09J
10J
11J
12J
13J
14J
15J
00H
01H
02H
03H
04H
05H
06H
07H
08H
09H
10H
11H
12H
13H
14H
15H
00F
01F
02F
03F
04F
05F
06F
07F
08F
09F
10F
11F
12F
13F
14F
15F
00E
04E
05E
06E
07E
08E
09E
10E
11E
12E
13E
14E
15E
01D
02D
03D
04D
05D
06D
07D
08D
09D
10D
11D
12D
13D
14D
15D
01C
02C
03C
04C
05C
06C
07C
08C
09C
10C
11C
12C
13C
14C
15C
00B
01B
02B
03B
04B
05B
07B
08B
09B
10B
11B
12B
13B
14B
15B
NOTE 1
00A
01A
02A
03A
04A
05A
06A
07A
08A
09A
10A
(TP) CATN
(TP) TMGIA
(TP) KTM
(TP) GSTRT1
(TP) DSTRT1
(TP) LDBR1
(TP) ADB1
(TP) ADA1
(TP) GND

REVISIONS

PRE PRODUCTION APPROVAL

	INIT	DATE
DEV		3/14/73
PROD		2-2-73

NOTE 1- PATH SHOWN IS FOR B-BUS STRAPS USED ON "POUT" OPTION (NOT NORMALLY EQUIPPED).

DECOUPLING CAP. TYP - ALL UNSPEC.

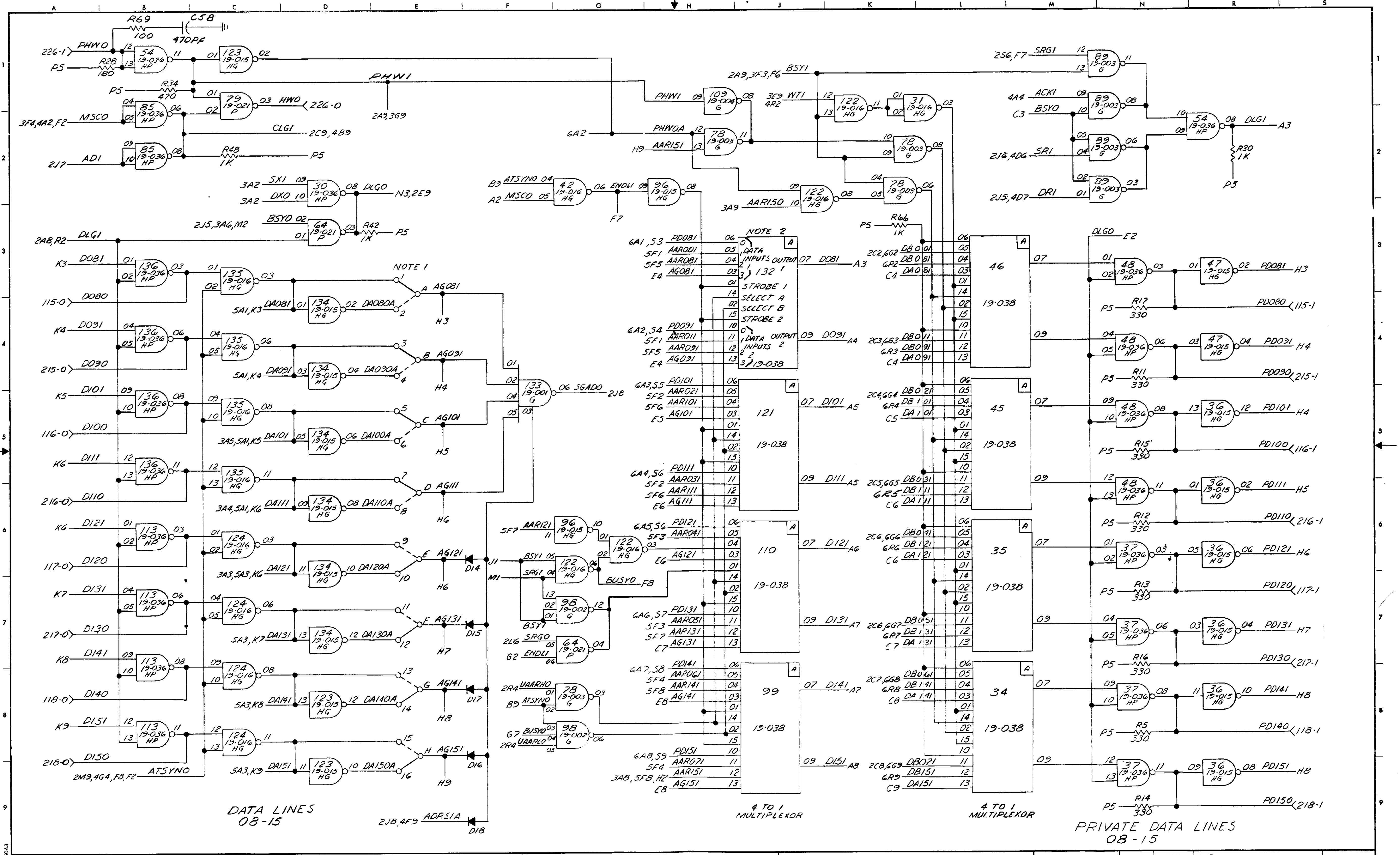
NOTE: DIODES EQUIV = ⊣▷⊢

NAME	TITLE	DATE
J.F. FLEMING 7	DRAFT	2-15-73
H. MATTER GEH	CHK	3-8-73
R.F. SCHUNNEMAN	ENGR	3-9-73
H. ROSS	Q.C.	3-26-73
R.E. JONES	DIR ENG	3-26-73

TITLE
COMPONENT LOCATER
MOD 80 IOU

TASK NO. 03029
DWG NO 35-405M01 D12
SHEET OF 1 - 1

INTERDATA®


DATA LINES 08-15
4 TO 1 MULTIPLEXOR
4 TO 1 MULTIPLEXOR
PRIVATE DATA LINES 08-15
NOTE 1
NOTE 2
SGADO
BUSYO
DLGI
DLGO
PHWI
HWO
CLGI

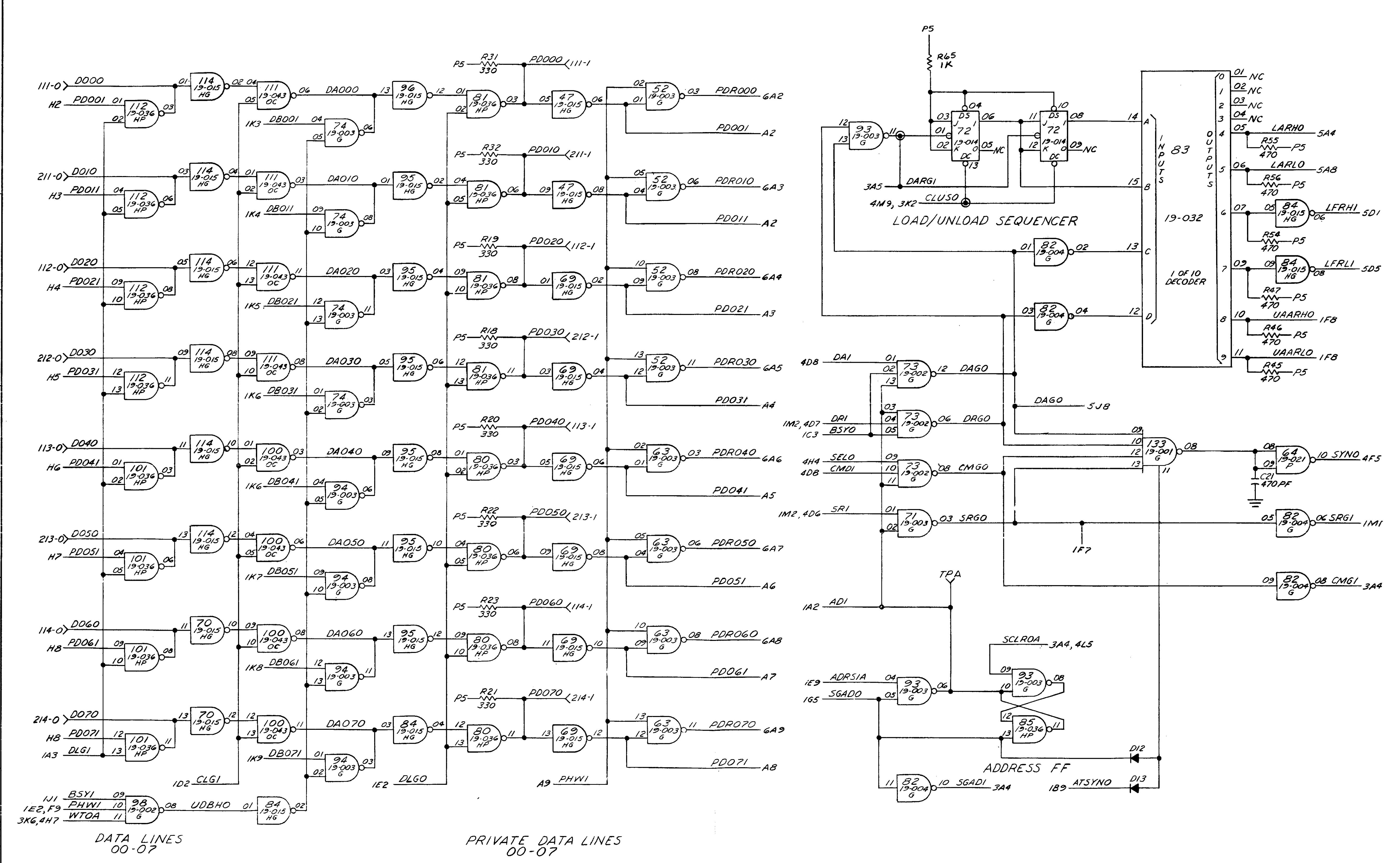
NOTES / PREFERRED ADDRESS X'F0'
ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-391M02 SELECTOR CHANNEL.

NAME	TITLE	DATE
W ZILLGER	DRAFT	10-5-71
R CERO	CHK	2-6-73
D FRANKENBERGER	ENGR	2-7-73
N. MASI	SY. TST	2-7-73
R.E. JONES	DIR ENG	

TITLE NS SELECTOR CHANNEL
TASK NO. 03075
DWG NO. 02-232M01 D08
SHEET 1 OF 7

BRUNING 44-231 15043

INTERDATA


D000
PD001
D010
PD011
D020
PD021
D030
PD031
D040
PD041
D050
PD051
D060
PD061
D070
PD071
DLG1
BSY1
PHW1
WTOA
UDBHO
CLG1
DLGO
DA000
DA010
DA020
DA030
DA040
DA050
DA060
DA070
DB001
DB011
DB021
DB031
DB041
DB051
DB061
DB071
PD000
PD010
PD020
PD030
PD040
PD050
PD060
PD070
PDR000
PDR010
PDR020
PDR030
PDR040
PDR050
PDR060
PDR070
PD001
PD011
PD021
PD031
PD041
PD051
PD061
PD071
PHW1
DATA LINES 00-07
PRIVATE DATA LINES 00-07
LOAD/UNLOAD SEQUENCER
DARG1
CLUSO
83
19-032
1 OF 10 DECODER
INPUTS
OUTPUTS
LARHO
LARLO
LFRH1
LFRL1
UAARHO
UAARLO
DAGO
DRGO
CMGO
SRGO
DA1
DR1
BSYO
SELO
CMD1
SR1
AD1
TPA
SYNO
C21 470PF
SRG1
CMG1
SCLROA
ADRS1A
SGADO
SGAD1
ADDRESS FF
ATSYNO
D12
D13
R65 1K
P5

NOTES
ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-391 M02 SELECTOR CHANNEL.

NAME	TITLE	DATE
W ZILLGER	DRAFT	10-5-71
	CHK	
	ENGR	
	DIR ENG	

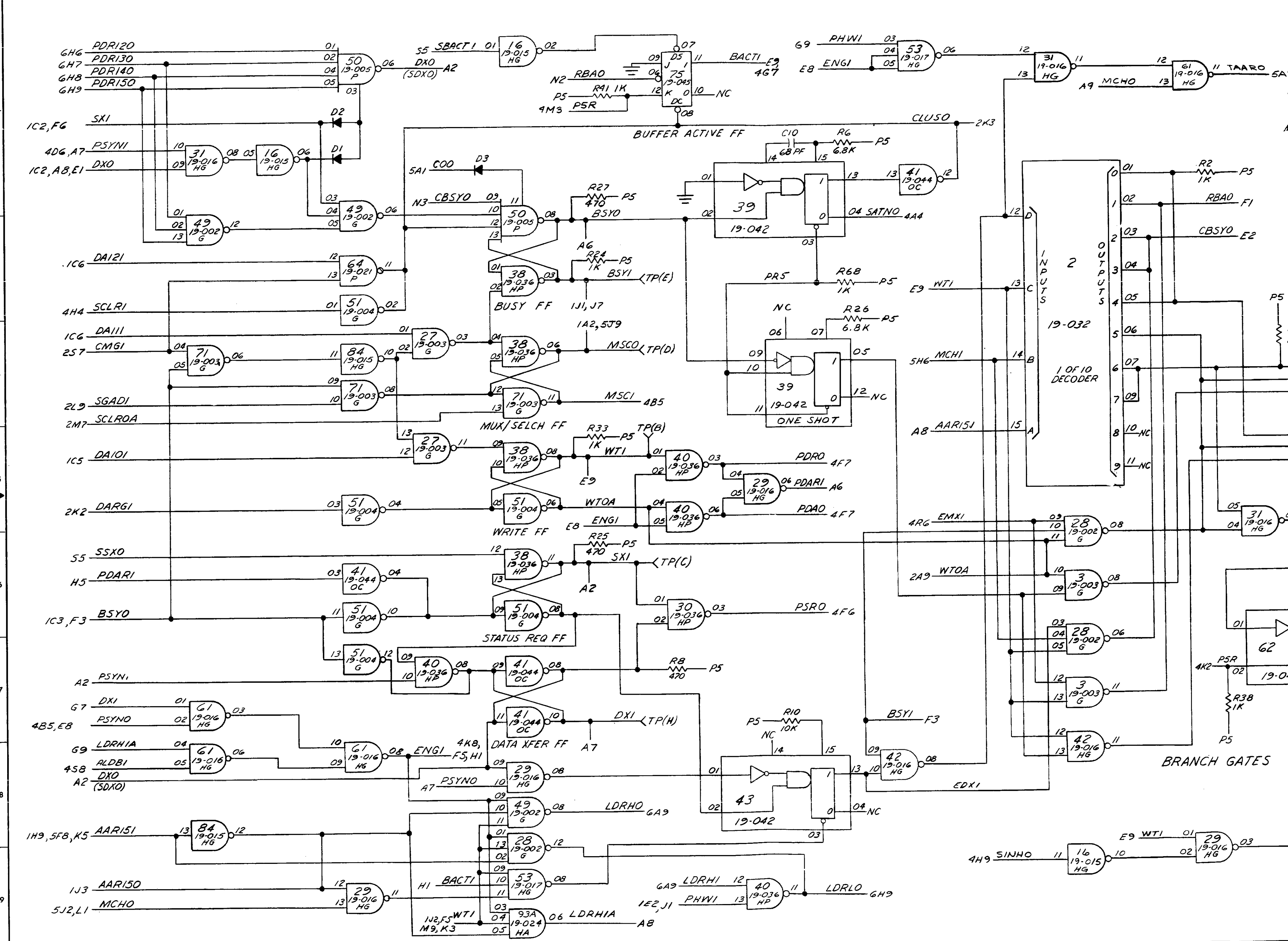
TITLE NS SELECTOR CHANNEL

TASK NO. 03075

DWG NO. 02-232M01D08

SHEET 2 OF 7

INTERDATA®


BUFFER ACTIVE FF
BUSY FF
MUX/SELCH FF
WRITE FF
STATUS REQ FF
DATA XFER FF
ONE SHOT
BRANCH GATES
1 OF 10 DECODER
INPUTS
OUTPUTS
19-032
19-042
PDR120
PDR130
PDR140
PDR150
SX1
PSYN1
DXO
(SDXO)
SBACT1
BACT1
RBAO
PSR
CLUSO
PHWI
ENGI
MCHO
MCHI
TAARO
C00
CBSYO
BSYO
BSY1
DA121
SCLR1
DA111
CMGI
SGADI
SCLROA
DA101
DARGI
SSXO
PDARI
MSCO
MSCI
WTI
WTO
WTOA
PDRO
PDAO
PSRO
SATNO
DXI
AAR151
AAR150
EMXI
EDXI
SREQO
LDBIA
LDBI
SINHO
PSYNO
LDRHIA
ALDBI
LDRHO
LDRHI
LDRLO
TP(B)
TP(C)
TP(D)
TP(E)
TP(H)

CIRCUIT NOTES

MAP FOR EDX (END OF DATA XFER)

	WTO	WTI	
MCHO	000 SSX	100 SSX	AAR150 (EVEN)
MCHO	001 RBA	101 SREQ,SSX,LDB	AAR151 (ODD)
MCHI	011 CBSY	111 SREQ,LDB	AAR151 (ODD)
MCHI	010 CBSY	110 SREQ,LDB	AAR150 (EVEN)

MAP FOR EMX (END MEM. XFER)

	WTO	WTI
MCHO	SREQ,SSX,LDB	RBA
MCHI	SREQ,SSX,LDB	RBA

MAP FOR EBS (END BSY SET)

WTO	WTI
SREQ	SSX

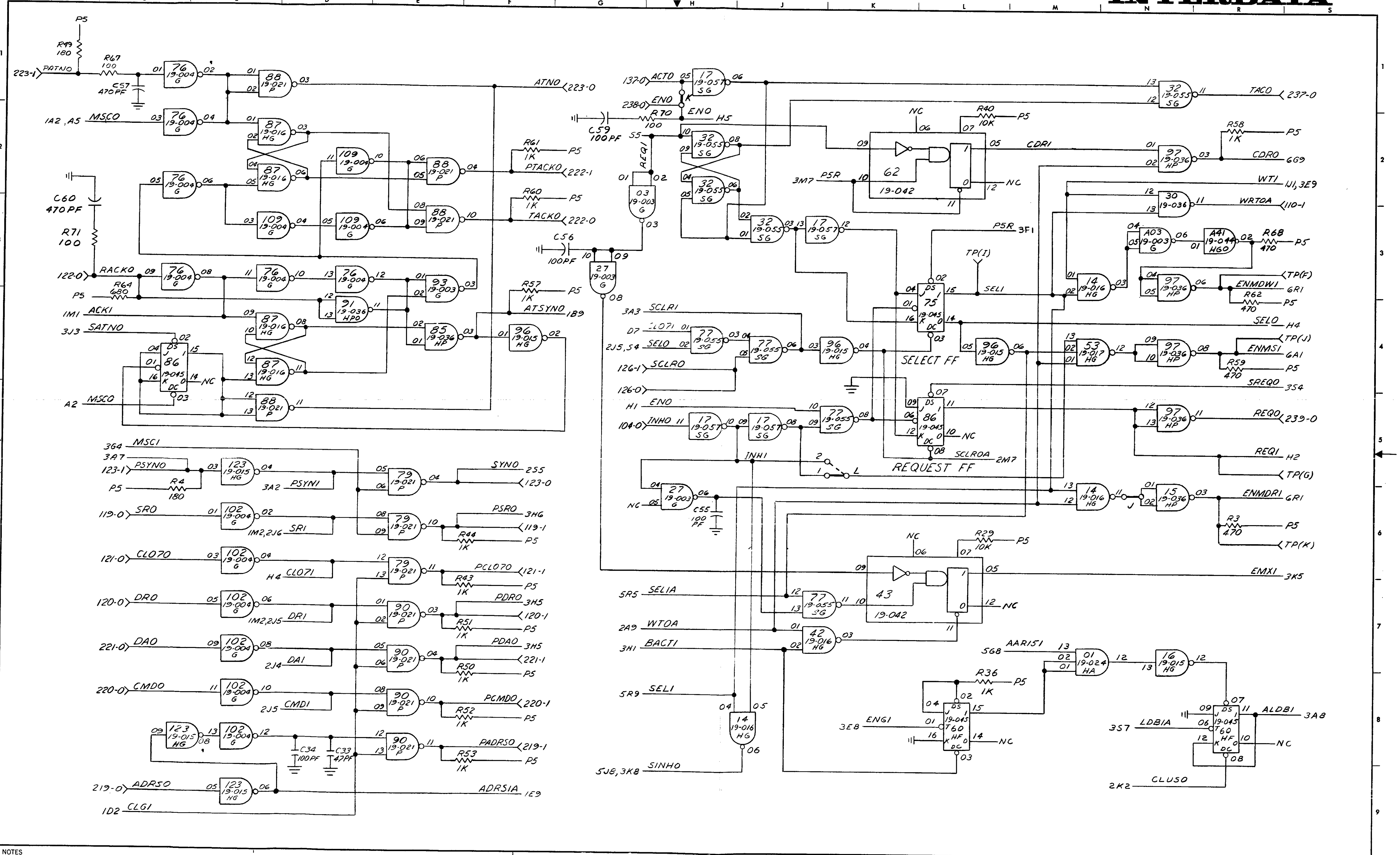
NOTES
ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-391 M02 SELECTOR CHANNEL.

NAME	TITLE	DATE
W ZILLGER	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE NS SELECTOR CHANNEL

TASK NO. 03075
DWG NO. 02-232M01D08
SHEET 3 OF 7

INTERDATA


PATNO
223-1
MSCO
1A2, A5
ATNO 223-0
PTACKO 222-1
TACKO 222-0
C60 470PF
R71 100
RACKO
122-0
ACKI
1M1
SATNO
3J3
A2
ATSYNO 1B9
MSCI
3G4
3A7
PSYNO
123-1
P5
SYNO 255
123-0
PSYNI
3A2
SRO
119-0
PSRO 3H6
119-1
SRI
1M2, 2J6
CLO7O
121-0
PCLO7O 121-1
CLO7I
H4
DRO
120-0
PDRO 3H5
120-1
DRI
1M2, 2J5
DAO
221-0
PDAO 3H5
221-1
DAI
2J4
CMDO
220-0
PCMDO 220-1
CMDI
2J5
PADRSO 219-1
ADRSO
219-0
ADRSIA 1E9
CLGI
1D2
ACTO
137-0
ENO
238-0
HS
C59 100PF
S5
REQI
C56 100PF
SCLRI
3A3
CLO7I
D7
SELO
2J5, S4
SCLRO
126-1
126-0
ENO
H1
INHO
104-0
INHI
SELECT FF
REQUEST FF
SCLROA 2M7
C55 100PF
NC
3M7
PSR
62
19-042
CDRI
TACO 237-0
CDRO 6G9
WTI 1J1, 3E9
WRTOA 110-1
P5R 3F1
TP(I)
SELI
R68 470
ENMDWI
TP(F)
6RI
R62 470
SELO H4
TP(J)
ENMSI
6AI
R59 470
SREQO 3S4
REQO 239-0
REQI H2
TP(G)
ENMDRI
6RI
R3 470
TP(K)
EMXI 3K5
SELIA
5R5
43
19-042
WTOA
2A9
BACTI
3H1
AARIS1
5G8
SELI
5R9
ENGI
3E8
LDBIA
3S7
ALDBI 3A8
CLUSO
2K2
SINHO
5J6, 3K8

NOTES
ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-391 M02 SELECTOR CHANNEL

NAME	TITLE	DATE
N ZILLGER	DRAFT	10-5-71
	CHK	
	ENGR	
	DIR ENG	

TITLE NS SELECTOR CHANNEL

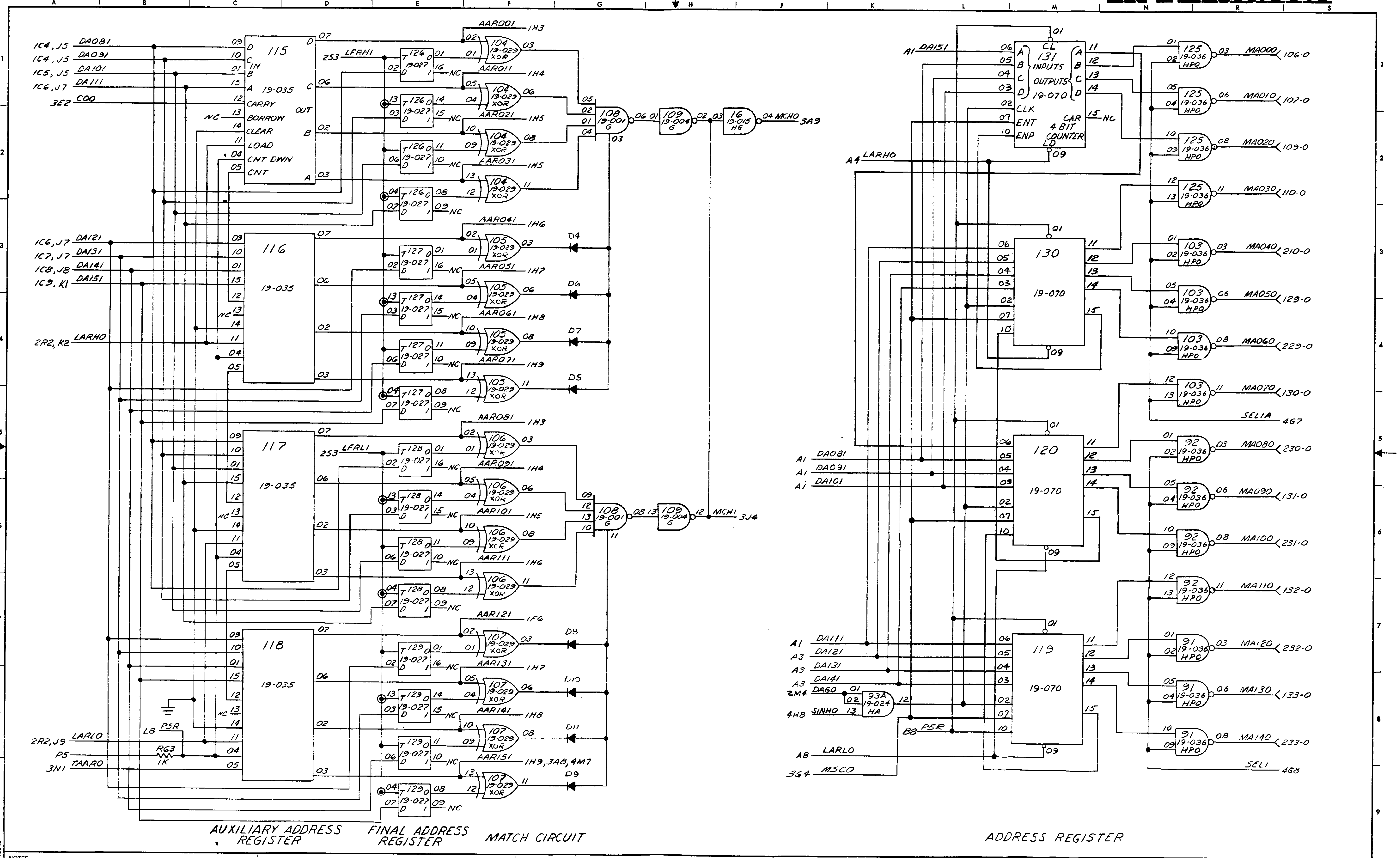
TASK NO. 03075

DWG NO. 02-232 M01D08

SHEET 4 OF 7

BRUNING 44 231 15043

INTERDATA



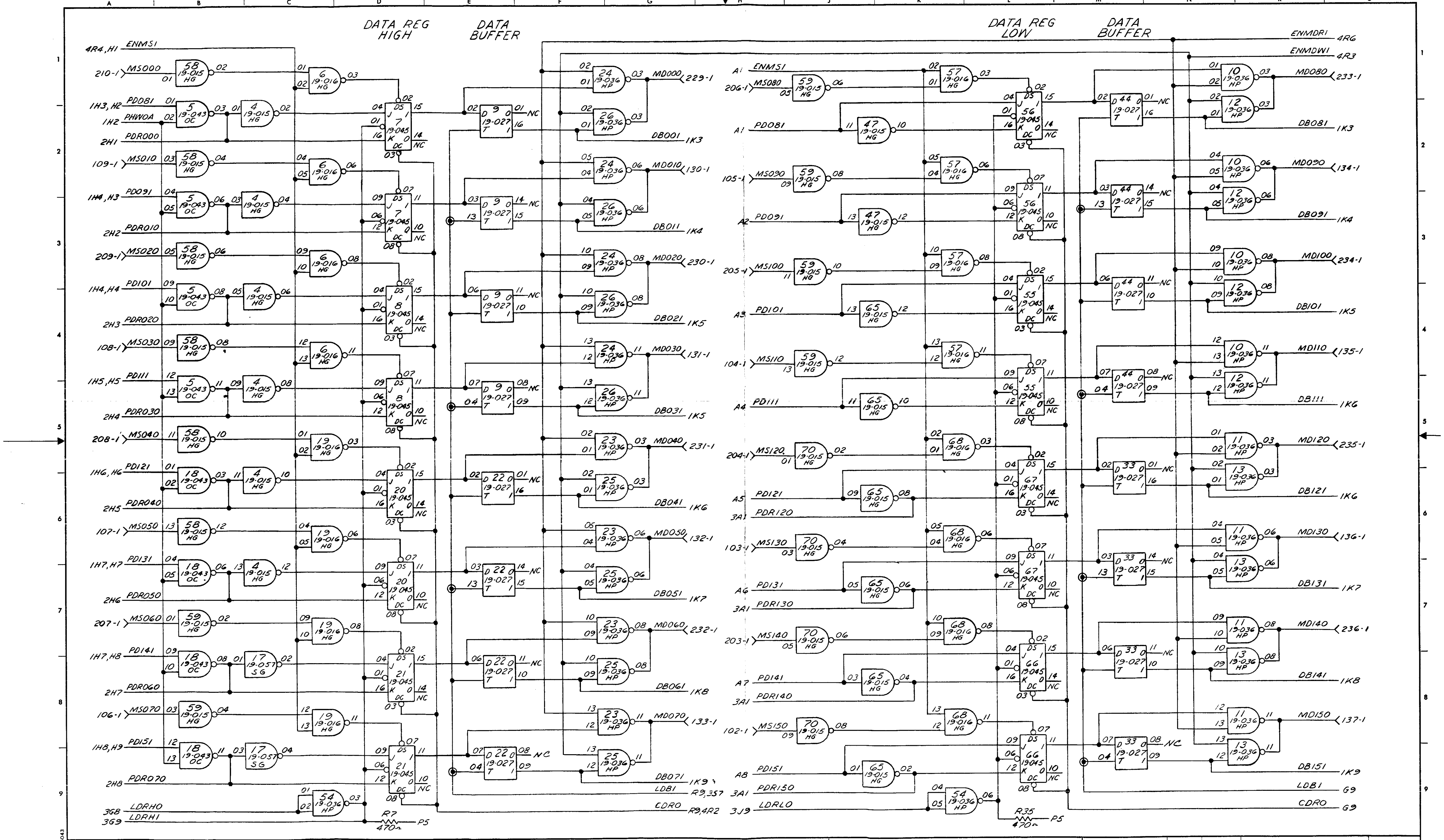
115 19-035
116 19-035
117 19-035
118 19-035
126 19-027
127 19-027
128 19-027
129 19-027
104 19-029 XOR
105 19-029 XOR
106 19-029 XOR
107 19-029 XOR
108 19-001 G
109 19-004 G
16 19-015 H6
MCHO 3A9
MCHI 3J4
131 INPUTS OUTPUTS 19-070 4 BIT COUNTER
130 19-070
120 19-070
119 19-070
125 19-036 HPO
103 19-036 HPO
92 19-036 HPO
91 19-036 HPO
93A 19-024 HA
1C4, J5 DA081
1C4, J5 DA091
1C5, J5 DA101
1C6, J7 DA111
3E2 C00
1C6, J7 DA121
1C7, J7 DA131
1C8, J8 DA141
1C9, K1 DA151
2R2, K2 LARHO
2R2, J9 LARLO
P5
3N1 TAARO
L8 PSR
RG3 1K
LFRHI
LFRLI
AAR001 1H3
AAR011 1H4
AAR021 1H5
AAR031 1H5
AAR041 1H6
AAR051 1H7
AAR061 1H8
AAR071 1H9
AAR081 1H3
AAR091 1H4
AAR101 1H5
AAR111 1H6
AAR121 1F6
AAR131 1H7
AAR141 1H8
AAR151 1H9, 3A8, 4M7
D4
D6
D7
D5
D8
D10
D11
D9
A1 DA151
A4 LARHO
A1 DA081
A1 DA091
A1 DA101
A1 DA111
A3 DA121
A3 DA131
A3 DA141
2M4 DA60
4H8 SINHO
B8 PSR
A8 LARLO
3G4 MSCO
MA000 106-0
MA010 107-0
MA020 109-0
MA030 110-0
MA040 210-0
MA050 129-0
MA060 229-0
MA070 130-0
SEL1A 4G7
MA080 230-0
MA090 131-0
MA100 231-0
MA110 132-0
MA120 232-0
MA130 133-0
MA140 233-0
SEL1 4G8
AUXILIARY ADDRESS REGISTER
FINAL ADDRESS REGISTER
MATCH CIRCUIT
ADDRESS REGISTER

NOTES
ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-391 M02 SELECTOR CHANNEL.

NAME	TITLE	DATE	TITLE
W ZILLGER	DRAFT	10-5-71	SELECTOR CHANNEL
	CHK		
	ENGR		TASK NO 03075
	DIR ENG		02-232M01D08 SHEET 5-7

BRUNING 44 231 15043

INTERDATA


DATA REG HIGH
DATA BUFFER
DATA REG LOW
DATA BUFFER
4R4, H1 ENMS1
210-1 MS000
1H3, H2 PD081
1H2 PHWOA
2H1 PDR000
109-1 MS010
1H4, H3 PD091
2H2 PDR010
209-1 MS020
1H4, H4 PD101
2H3 PDR020
108-1 MS030
1H5, H5 PD111
2H4 PDR030
208-1 MS040
1H6, H6 PD121
2H5 PDR040
107-1 MS050
1H7, H7 PD131
2H6 PDR050
207-1 MS060
1H7, H8 PD141
2H7 PDR060
106-1 MS070
1H8, H9 PD151
2H8 PDR070
3G8 LDRHO
3G9 LDRH1
R7 470Ω P5
MD000 229-1
DB001 1K3
MD010 130-1
DB011 1K4
MD020 230-1
DB021 1K5
MD030 131-1
DB031 1K5
MD040 231-1
DB041 1K6
MD050 132-1
DB051 1K7
MD060 232-1
DB061 1K8
MD070 133-1
DB071 1K9
LDB1 R9, 3S7
CDRO R9, 4R2
A1 ENMS1
206-1 MS080
A1 PD081
105-1 MS090
A2 PD091
205-1 MS100
A3 PD101
104-1 MS110
A4 PD111
204-1 MS120
A5 PD121
3A1 PDR120
103-1 MS130
A6 PD131
3A1 PDR130
203-1 MS140
A7 PD141
3A1 PDR140
102-1 MS150
A8 PD151
3A1 PDR150
3J9 LDRLO
R35 470Ω P5
ENMDR1 4R6
ENMDW1 4R3
MD080 233-1
DB081 1K3
MD090 134-1
DB091 1K4
MD100 234-1
DB101 1K5
MD110 135-1
DB111 1K6
MD120 235-1
DB121 1K6
MD130 136-1
DB131 1K7
MD140 236-1
DB141 1K8
MD150 137-1
DB151 1K9
LDB1 G9
CDRO G9
19-015 HG
19-016 HG
19-043 OC
19-045
19-027
19-036 HP
19-057 SG
A B C D E F G H J K L M N R S
1 2 3 4 5 6 7 8 9

NOTES
ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-391 M02 SELECTOR CHANNEL.

NAME	TITLE	DATE
W ZILLGER	DRAFT	10-5-71
	CHK	
	ENGR	
	DIR ENG	

TITLE NS SELECTOR CHANNEL

TASK NO 03075

DWG NO. 02-232M01D08

SHEET 6 OF 7

BRUNING 44-231 15043

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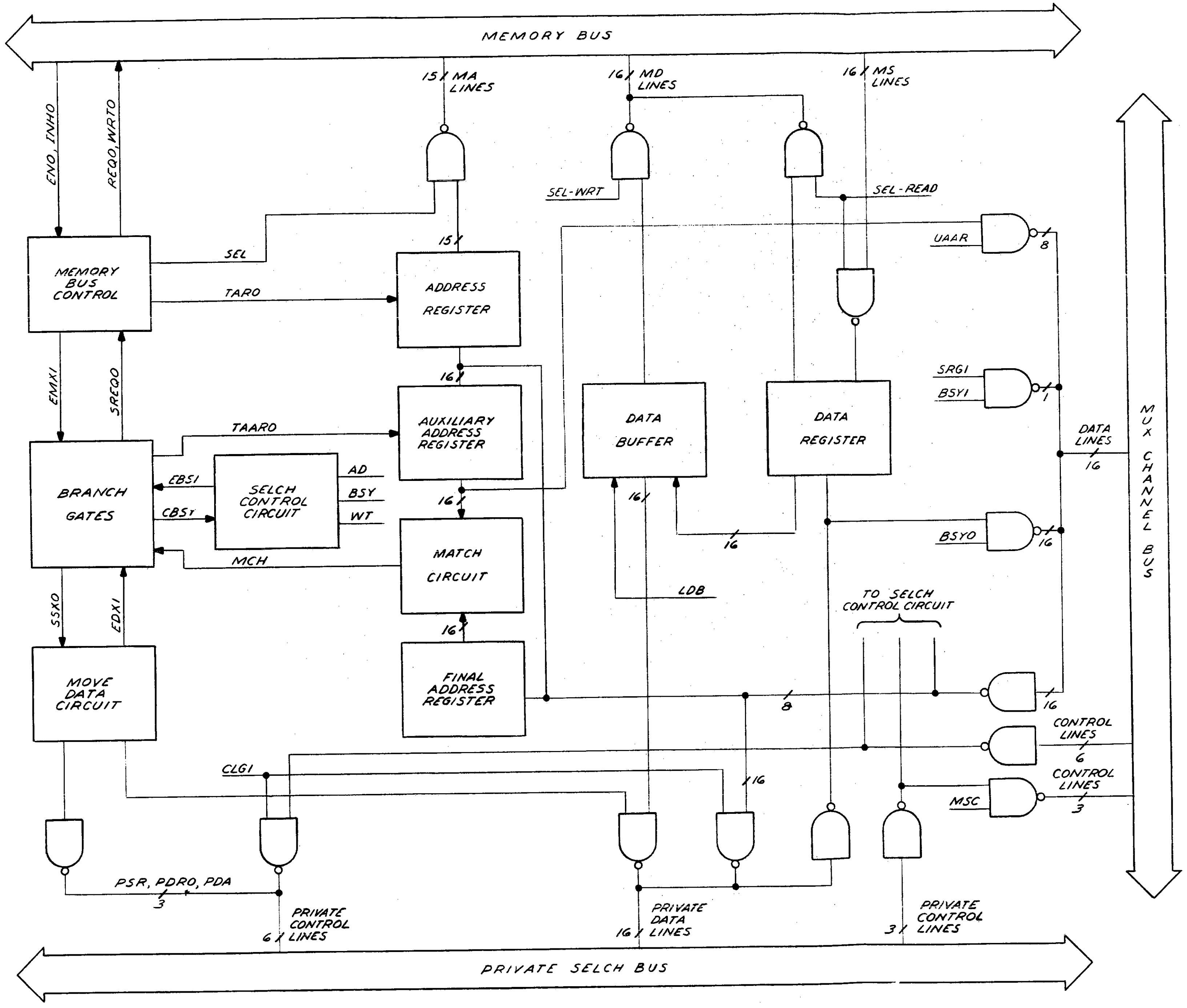

MEMORY BUS
ENO, INHO
REQO, WRTO
15/ MA LINES
16/ MD LINES
16/ MS LINES
SEL-WRT
SEL-READ
MEMORY BUS CONTROL
SEL
TARO
15/
ADDRESS REGISTER
16/
AUXILIARY ADDRESS REGISTER
UAAR
8
SRGI
BSYI
1
DATA BUFFER
DATA REGISTER
DATA LINES
16
EMXI
SREQO
TAARO
BRANCH GATES
CBSI
CBSY
SELCH CONTROL CIRCUIT
AD
BSY
WT
16/
MATCH CIRCUIT
MCH
BSYO
16
LDB
16/
MUX CHANNEL BUS
SSXO
EDXI
MOVE DATA CIRCUIT
16/
FINAL ADDRESS REGISTER
TO SELCH CONTROL CIRCUIT
8
16
CONTROL LINES
6
CLGI
16
MSC
CONTROL LINES
3
PSR, PDRO, PDA
3
PRIVATE CONTROL
6/ LINES
PRIVATE DATA
16/ LINES
PRIVATE CONTROL
3/ LINES
PRIVATE SELCH BUS

BACK PANEL PIN INDEX			
MNEM.	LOC.	MNEM.	LOC.
ACTO	4H1	MD130	6R6
ADRSO	4B8	MD140	6R7
ATNO	4F1	MD150	6R8
CLO70	4B6	MS000	6A1
CMDO	4B8	MS010	6A2
D000	2A1	MS020	6A3
D010	2A2	MS030	6A4
D020	2A3	MS040	6A5
D030	2A4	MS050	6A6
D040	2A5	MS060	6A7
D050	2A6	MS070	6A8
D060	2A7	MS080	6H1
D070	2A8	MS090	6H2
D080	1A3	MS100	6H3
D090	1A4	MS110	6H4
D100	1A5	MS120	6H5
D110	1A6	MS130	6H6
D120	1A6	MS140	6H7
D130	1A7	MS150	6H8
D140	1A8	PADRSO	4F8
D150	1A8	PATNO	4B1
DAO	4B7	PCLO70	4F6
DRO	4B7	PCMDO	4F8
ENO	4H1	PD000	2F1
HWO	1D1	PD010	2F2
INHO	4H5	PD020	2F3
MA000	5R1	PD030	2F4
MA010	5R1	PD040	2F5
MA020	5R2	PD050	2F6
MA030	5R2	PD060	2F7
MA040	5R3	PD070	2F8
MA050	5R3	PD080	1R4
MA060	5R4	PD090	1R4
MA070	5R4	PD100	1R5
MA080	5R5	PD110	1R6
MA090	5R6	PD120	1R7
MA100	5R6	PD130	1R7
MA110	5R7	PD140	1R8
MA120	5R7	PD150	1R9
MA130	5R8	PDAO	4F7
MA140	5R8	PDRO	4F8
MD000	6G1	PHWO	1A1
MD010	6G2	PSRO	4F6
MD020	6G3	PSYNO	4B5
MD030	6G4	PTACKO	4F2
MD040	6G5	RACKO	4B3
MD050	6G6	REQO	4P5
MD060	6G7	SCLRO	4H4
MD070	6G8	SRO	4B6
MD080	6R1	SYNO	4F5
MD090	6R2	TACKO	4H3
MD100	6R3	TACO	4R1
MD110	6R4	WRTOA	4R3
MD120	6R5		

BACK PANEL MAP			
ROW		TERM NO.	CONN.
1	2		
P5	GND	41	
GND	GND	40	
		39	
		38	
MD150		37	
MD130	MD140	36	
MD110	M120	35	
MD090	MD100	34	
MD070	MD080	33	
MD050	MD060	32	
MD030	MD040	31	
MD010	MD020	30	
	MD000	29	
		28	
		27	
SCLRO	PHWO	26	
		25	
		24	
PSYNO	PATNO	23	
	PTACKO	22	
PCLO70	PDAO	21	1
PDRO	PCMDO	20	
PSRO	PADRSO	19	
PD140	PD150	18	
PD120	PD130	17	
PD100	PD110	16	
PD080	PD090	15	
PD060	PD070	14	
PD040	PD050	13	
PD020	PD030	12	
PD000	PD010	11	
WRTOA	MS000	10	
MS010	MS020	09	
MS030	MS040	08	
MS050	MS060	07	
MS070	MS080	06	
MS090	MS100	05	
MS110	MS120	04	
MS130	MS140	03	
MS150		02	
GND	GND	01	
P5	GND	00	
P5	GND	41	
GND	GND	40	
	REQO	39	
	ENO	38	
ATCO	TACO	37	
		36	
		35	
		34	
MA130	MA140	33	
MA110	MA120	32	
MA090	MA100	31	
MA070	MA080	30	
MA050	MA060	29	
		28	
		27	
SCLRO	HWO	26	
		25	
		24	
SYNO	ATNO	23	
RACKO	TACKO	22	
CLO70	DAO	21	0
DRO	CMDO	20	
SRO	ADRSO	19	
D140	D150	18	
D120	D130	17	
D100	D110	16	
D080	D090	15	
D060	D070	14	
D040	D050	13	
D020	D030	12	
D000	D010	11	
MA030	MA040	10	
MA020		09	
		08	
MA010		07	
MA000		06	
		05	
INHO		04	
		03	
		02	
GND	GND	01	
P5	P5	00	

TEST POINT INDEX		
DESIG	MNEM	LOC.
A	ADI	2L6
B	WTI	3G5
C	SXI	3G6
D	MSCO	3G4
E	BSYO	3G3
F	ENMDWI	4S3
G	REQI	4S5
H	DXI	3G7
I	SELI	4L3
J	ENMSI	4S4
K	ENMDRI	4S6

SUPPLEMENTARY INFORMATION

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION	
NS SELCH	35-391M02

NOTES

NAME	TITLE	DATE
W ZILLGER	DRAFT	10-13-71
	CHK	
	ENGR	
	DIR ENG	

TITLE NS SELECTOR CHANNEL

TASK NO. 03075

DWG NO. 02-232 M01D08

SHEET 7 OF 7

BRUNING 44-231 · 15043

INTERDATA®

SHEET LOCATION	ROW 2	TERM LOC	ROW 1	SHEET LOCATION
1N4	GND	24	DL160	9R5
		23	DL140	6S7
		22	DL150	6S9
		21	DL130	6S5
		20	DL120	6S3
		19	DL100	6H5
		18	DL110	6H8
		17	DL090	6H3
		16	DL080	6H1
		15	DL070	5S9
		14	DL060	5S7
		13	DL050	5S5
		12	DL040	5S3
		11	DL030	5H8
		10	DL020	5H5
		09	DL010	5H3
		08	DL000	5H1
		07	P5S	1N6
1N4	GND	06	SROB	2N2
1N2	P15	05	P15	1N2
1N4	GND	04	P5	1N3
1N4	GND	03	P5	1N3
1N3	P24	02	P24	1N3
1N4	GND	01	P22	1N2
1N4	GND	00	P22	1N1

CONN 4

SHEET LOCATION	ROW 2	TERM LOC	ROW 1	SHEET LOCATION
1N4	GND	24	GND	1N4
7F4	AB020	23	AB031	7F5
9G9	AB130	22	AB061	7F9
8M1	AB070	21	AB051	7F8
7F6	AB040	20	AB081	8M3
9G5	AB110	19	AB101	9G3
9G2	AB090	18	AB121	9G7
7G2	STRB20	17	STRB30	7G2
7G1	STRB00	16	STRB10	7G1
7F5	AA021B	15	AA031B	7F6
7G2	STRA00	14	STRA10	7G3
7G3	STRA20	13	STRA30	7G3
7F8	AA050	12	AA101	9G4
8M2	AA070	11	AA041	7F7
7F9	AA060	10	AA081	8M3
9G2	AA090	09	AA131	9J9
9G6	AA110	08	AA121	9G7
2A2	ENDCYL0	07	MWRT0A	8R7
1N4	GND	06	EAD0	3K8
		05	FECLK0	3A9
		04	P3	9N9
		03	GR1	4R6
9R6	MRST0A	02	P22	1N1
1N2	P8	01	P8	1N3
1N5	P5S	00	P5S	1N5

CONN 3

SHEET LOCATION	ROW 2	TERM LOC	ROW 1	SHEET LOCATION
1N5	GND	12	WSB1	8A3
		11	WSD1	8A4
		10	WSA1	8A3
		09	WSC1	8A4
		08	MSK30	8A6
		07	MSK20	8A6
		06	MSK00	8A5
		05	MSK10	8A5
		04	BP020	8A8
		03	BP010	8A8
1N5	GND	02	BP000	8A9
8A9	WEBL0	01	WCLK0	8A7
8F7	PON0	00	PREL0	8R9

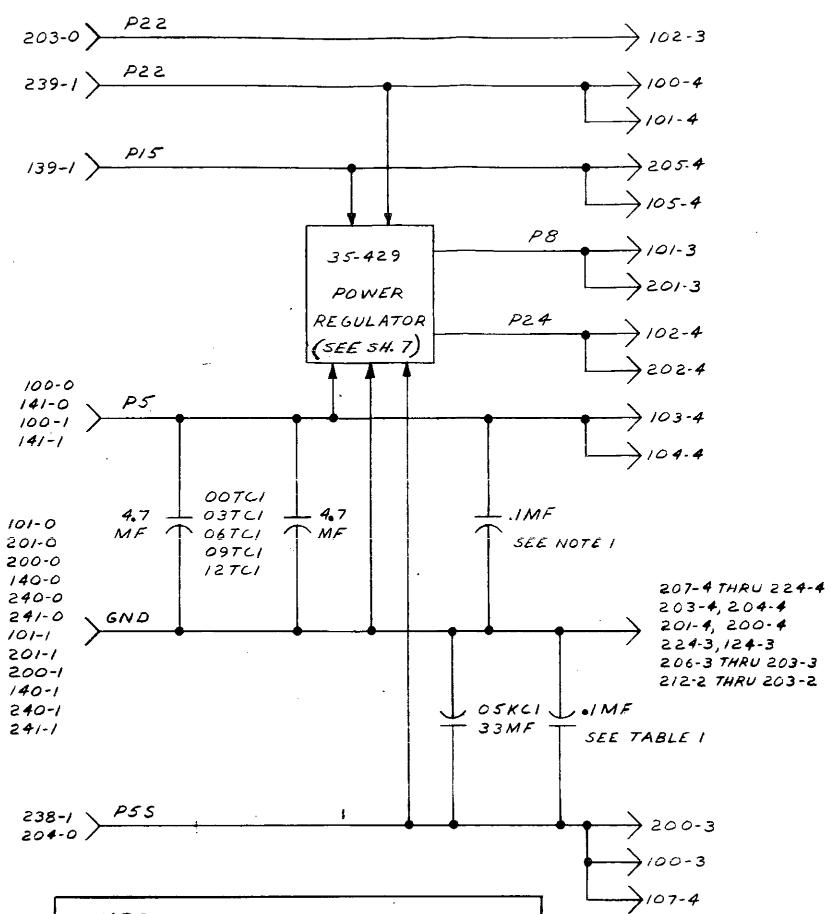
CONN 2

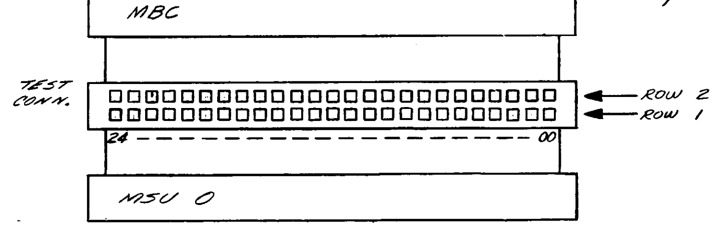
SHEET LOCATION	ROW 1	TERM LOC	ROW 2	SHEET LOCATION
1K3	P5	41	GND	1K5
1K4	GND	40	GND	1K5
1K2	P15	39	P22	1K2
—	N15	38	P5S	1K5
6J6	CD141	37	CD151	6J8
6J2	CD121	36	CD131	6J4
6A6	CD101	35	CD111	6A8
6A2	CD081	34	CD091	6A4
5J6	CD061	33	CD071	5J8
5J2	CD041	32	CD051	5J4
5A6	CD021	31	CD031	5A8
5A2	CD001	30	CD011	5A4
3A4	CA140	29	CA150	—
9A6	CA120	28	CA130	9A8
9A3	CA100	27	CA110	9A5
8F3	CA080	26	CA090	9A1
7A9	CA060	25	CA070	8F1
7A6	CA040	24	CA050	7A8
7A4	CA020	23	CA030	7A5
		22		
7A1	CA000	21	CA010	7A7
3A3	CREQ0	20	CFTCH0	2A2
3R4	CRDY0	19	CWRT0	8F8
—	A140	18	A150	—
—	A120	17	A130	—
—	A100	16	A110	—
—	A080	15	A090	—
—	A060	14	A070	—
—	A040	13	A050	—
—	A020	12	A030	—
—	A000	11	A010	—
8F9	WRT0A	10	MSD000	5A1
5A3	MSD010	09	MSD020	5A5
5A8	MSD030	08	MSD040	5J1
5J3	MSD050	07	MSD060	5J5
5J7	MSD070	06	MSD080	6A1
6A3	MSD090	05	MSD100	6A5
6A8	MSD110	04	MSD120	6J1
6J3	MSD130	03	MSD140	6J5
6J8	MSD150	02	SP7	—
1K4	GND	01	GND	1K4
1K3	P5	00	GND	1K4

CONN 1

SHEET LOCATION	ROW 1	TERM LOC	ROW 2	SHEET LOCATION
1K3	P5	41	GND	1K5
1K4	GND	40	GND	1K5
1K2	P15	39	REQ0	2A5
—	N15	38	EN0	2A9
3N2	IA0	37		
3R7	IPF0	36	DPF0	3R7
~~2A4~~	~~MB020~~	35	B150	—
~~2A3~~	~~MB000~~	34	~~MB010~~	~~2A3~~
9A8	MA130	33	MA140	3A7
9A5	MA110	32	MA120	9A7
9A2	MA090	31	MA100	9A3
8F2	MA070	30	MA080	8F3
7A8	MA050	29	MA060	7A9
		28		
		27	PVMD0	8F7
9K7	SCLR0	26		
~~3A3~~	~~CB020~~	25		
~~3A1~~	~~CB000~~	24	~~CB010~~	~~3A2~~
7A5	MA030	10	MA040	7A7
7A4	MA020	09	SP5	—
—	SP6	08	SP4	—
7A3	MA010	07	SP3	—
7A1	MA000	06	SP2	—
	PAR0	05	SP1	—
3N5	INH0	04	P5S	1K5
		03	P22	1K1
1K3	P5	02	P5	1K3
1K4	GND	01	GND	1K3
1K3	P5	00	GND	1K3

CONN 0





TEST POINT DIAGRAM

MBC/MSU CABLE

DESCRIPTION	CABLE PART NO.
LEFT	17-191FXX
RIGHT	17-212FXX

F01 - 16KB
F02 - 32KB
F03 - 48KB
F04 - 64KB

TABLE 1

.1MF CAPACITORS TO P5S			
06AC1 08AC1 10AC1 05BC1 07BC1 09BC1 11BC1	06CC1 08CC1 10CC1 05DC1 07DC1 09DC1 11DC1	06EC1 08EC1 10EC1 07FC1 06HC1 08HC1 07JC1	10KC1 07MC1 09MC1 11MC1

SUPPLEMENTARY INFORMATION

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION

35-407R16

NOTE:

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT

REVISIONS

PRE PRODUCTION APPROVAL: DEV / PROD — INIT. — DATE

DESCRIPTION			TASK		DATE	REV
REVISED TO AGREE WITH CHANGES ON 35-407 & 35-429.	HM		3214-23 & 24		12-26-72	R01
REVISED SHEET 3.			3214-27		1-19-73	R02
REVISED SHEETS 1,2,4 & 7	CG.	CVC	3214-28		1-31-73	R03
REVISED SHTS 2,3,4,7,8	HM		3214-30		3-30-73	R04
FUNCTION FOR 202-3 WAS NOT SPEC. REVISED SHTS 2,3,4,8 & 9	HM		3214-31		3-30-73	R05
ADDED: SHEET 10, 11, NOTE 2, CABLE INFO. REVISED SHTS. 2,3,4,8 & 9	DB		3214-35		[illegible]	R06
ADDED: SHEET 9 AREA L2 ADDED NOTE CONCERNING 19-038; SHEET 7 ADDED NOTE 2; SHEET 10 ADDED NOTE 2; SHEET 2 AREA G2 ADDED FETCH1; SHEET 3 AREA A4 ADDED FETCH1	PC	KVC	3214-40		5-25-73	R07
REVISED SHTS 2,3 & 4	PC	HCH	A 05	HH	8-9-73	R08
REVISED SHTS 3,4,& 7	PC		1918	HHM	9-5-73	R09
REVISED SHTS 1,2,3,4,& 8	TP	HCH	1968	HH	10-18-73	R10
REVISED SHT 10	PC	HCH	2018	HH	12-10-73	R11
REVISED SHTS 1,2 & 3	BG	HCH	2047	HG	[illegible]	R12

SHEET INDEX											
REV. LEVEL	12	9	10	8	1	1	5	5	4	2	0
SHEET NO.	1	2	3	4	5	6	7	8	9	10	11

NOTES
1. .1MF CAPACITORS NOT SPECIFIED IN TABLE 1 WILL GO TO P5
2. ALL P.C. BOARD ASSYS BUILT PRIOR TO 35-407R11 SHALL BE EQUIPPED WITH 35-429 DAUGHTER BOARDS (SHT. 7). ALL ASSYS BUILT 35-407R11 OR HIGHER REV. SHALL BE EQUIPPED WITH 35-478 DAUGHTER BOARDS (SHEET 10).

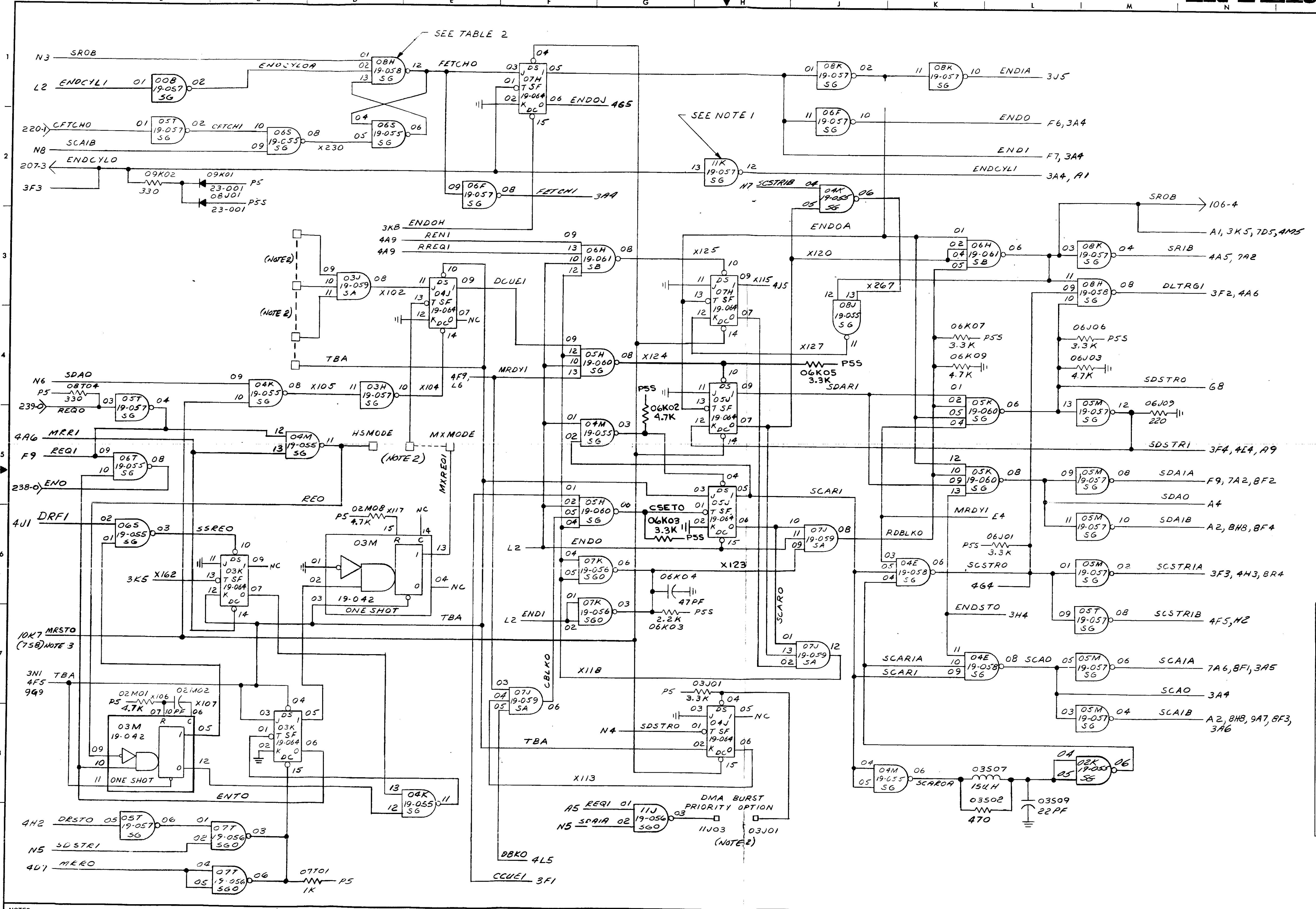
NAME	TITLE	DATE
B GRAY	DRAFT	10-17-72
J F FLEMING	CHK	7-2-73
L PEZZI	ENGR	7-2-73
N. MASSI	TEST	7-2-73
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MOD 80
MBC WW

TASK NO. 03214
DWG NO. 35-407 R12 D08
SHEET OF 1-11

BRUNING 44-231 16042

INTERDATA®


SEE TABLE 2
N3 SROB
L2 ENDCYL1
ENDCYL0A
08H 19-058 SG
FETCH0
07H 19-064 T SF
ENDOJ 4G5
220-1 CFTCH0
CFTCH1
N8 SCAIB
06S 19-055 SG
X230
207-3 ENDCYL0
3F3
09K02 330
09K01 23-001 P5
08J01 23-001 P5S
06F 19-057 SG
FETCH1 3A4
SEE NOTE 1
11K 19-057 SG
ENDCYL1 3A4, A1
N7 SCSTRIB
04K 19-055 SG
08K 19-057 SG
ENDIA 3J5
06F 19-057 SG
ENDO F6,3A4
ENDI F7,3A4
SROB 106-4
A1, 3K5, 7D5, 4M5
3K8 ENDOH
4A9 REN1
4A9 RREQ1
06H 19-061 SB
ENDOA
X125
X120
X115 4J5
X267
08J 19-055 SG
06H 19-061 SB
08K 19-057 SG
SR1B 4A5, 7A2
08H 19-058 SG
DLTRG1 3F2, 4A6
(NOTE 2)
03J 19-059 SA
X102
04J T SF 19-064
DCUE1
TBA
N6 SDA0
08T04 330
P5
239-0 REQ0
05T 19-057 SG
04K 19-055 SG
X105
03H 19-057 SG
X104
4F9, L6
MRDY1
05H 19-060 SG
X124
06K05 3.3K P5S
06K07 3.3K P5S
06K09 4.7K
06J06 3.3K P5S
06J03 4.7K
SDSTR0 G8
SDARI
P5S 06K02 4.7K
05J T SF 19-064
05K 19-060 SG
05M 19-057 SG
06J09 220
SDSTR1 3F4, 4E4, A9
4A6 MRR1
F9 REQ1
06T 19-055 SG
04M 19-055 SG
HSMODE
MXMODE
(NOTE 2)
MXREQ1
238-0 ENO
REO
04M 19-055 SG
SCAR1
05K 19-060 SG
05M 19-057 SG
SDA1A F9, 7A2, 8F2
SDA0 A4
SDA1B A2, 8H8, 8F4
4J1 DRF1
06S 19-055 SG
SSREQ
02M08 X117 4.7K
03M
19-042 ONE SHOT
03K T SF 19-064
3K5 X162
CSETO
06K03 3.3K P5S
05J 19-064
MRDY1 E4
RDBLK0
07J 19-059 SA
06J01 3.3K P5S
04E 19-058 SG
SCSTR0
4G4
05M 19-057 SG
SCSTR1A 3F3, 4H3, 8R4
L2 ENDO
07K 19-056 SGO
06K04 47PF
X123
L2 END1
07K 19-056 SGO
2.2K 06K03 P5S
ENDSTO 3H4
05T 19-057 SG
SCSTRIB 4F5, H2
10K7 MRSTO
(7S8) NOTE 3
SCAR0
07J 19-059 SA
SCARIA
SCAR1
04E 19-058 SG
SCA0
05M 19-057 SG
SCA1A 7A6, 8F1, 3A5
SCA0 3A4
05M 19-057 SG
SCA1B A2, 8H8, 9A7, 8F3, 3A6
3N1 4F5 9G9 TBA
02M01 X106 02M02
P5 4.7K 10PF X107
03M 19-042 ONE SHOT
03K T SF 19-064
X118
CBLK0
07J 19-059 SA
03J01 3.3K P5
N4 SDSTR0
04J T SF 19-064
TBA
X113
04K 19-055 SG
ENT0
04M 19-055 SG
SCAR0A
03S07 154H
03S02 470
03S09 22PF
02K 19-055 SG
4H2 DRST0
05T 19-057 SG
07T 19-056 SGO
N5 SDSTR1
4D7 MERO
07T 19-056 SGO
07T01 1K P5
DMA BURST PRIORITY OPTION
A5 REQ1
N5 SPAIA
11J 19-056 SGO
11J03 03J01 (NOTE 2)
DBK0 4L5
CCUE1 3F1

REVISIONS

REDRAWN FOR REDESIGN FOR PREVIOUS REVISIONS SEE VOID R02 COPY IN FILE.

HM		3214-30		3-30-73	R03

AREA D1, 08H-02 WAS CONNECTED TO 06S-10 00B WAS NOT SPEC.

AREA F9, 'DBK0' WAS 'X114'.
AREA F1, 07H-06 WAS NC.
AREA L8, 03S-07, 03S-02, 03S-09 WERE NOT SPEC.

HM		3214-31		3-30-73	R04

ADDED: CO-ORDINATIONS FOR MRSTO IN AREA A7 GOING TO SHT. 10.
ADDED NOTE 2
CHANGED: SCSTRIA IN AREA N6 CO-ORDINATION 3F3 WAS 3B5. ADDED CO-ORDINATION 3A5 TO SCA1A IN AREA N7. SDSTR1 IN AREA N5 CO-ORDINATION 3F4 WAS 3A6. ADDED CO-ORDINATION 3A6 TO SCA1B IN AREA N8.

DB		3214-35		5-1-73	R05

AREA G2; IC 06F PIN 08, WAS N.C.

PE		3214-40		5-25-73	R06

AREA M8: IC 02K WAS 06F, PINS 12 & 13, 19-057

PE		1905		8-9-73	R07

AREA A6 4J1 WAS 3H4, DRF1 WAS X167

TCP		1968		10-18-73	R08

LOC. B3 DELETED 3 GATES OUTPUTS, 05S-10, 12 & 8, ALSO RUNS MB000, MB010, MB020 MB001, MB011 & MB021

BG		2047		1/24/74	R09

TABLE 2

LOCATIONS OF IC'S POWERED BY P5S		
08B	10D	07H
05B	09B	08H
06B	05E	10H
07B	06D	07J
10B	07E	08J
11B	08E	07C
05C	09E	07K
06C	10E	08K
10C	11E	06M
11C	06F	08M
06D	08F	09M
07D	09F	09S
08D	11F	10S
09D	06H	11S
05M	09A	10M
08C	07F	07S
09C	10F	08S
10D	12F	05J
11D	08A	
06E	07M	

NOTES
1. POWER PINS OF IC'S NOT SPECIFIED IN TABLE 2 WILL GO TO P5
2. STANDARD OPTION SHOWN.
3. CO-ORDINATIONS IN PARENTHESIS APPLY TO MOTHER BOARDS EQUIPPED WITH A 35-429 DAUGHTER BOARD.

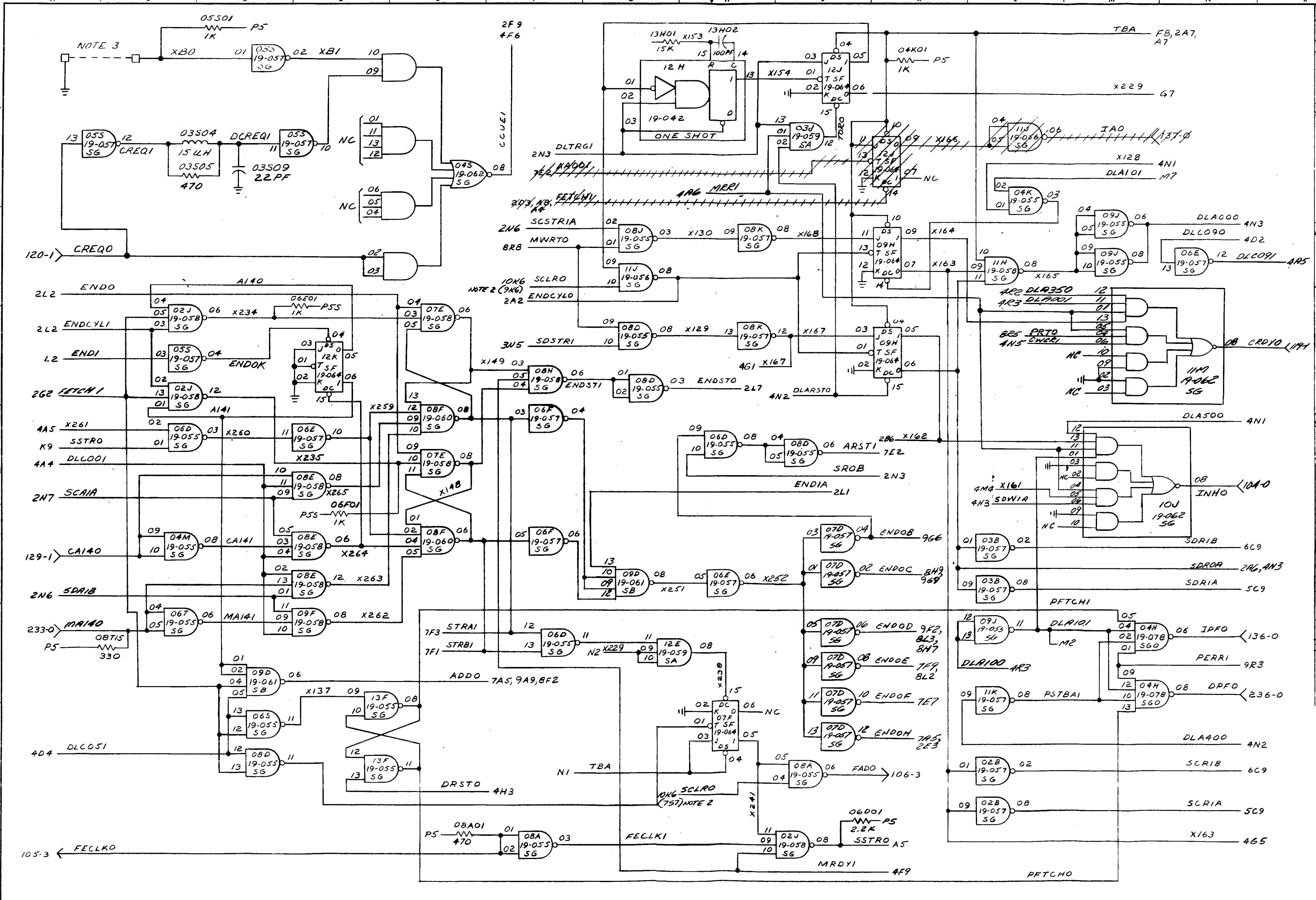
NAME | TITLE | DATE
DRAFT
CHK
ENGR
DIR ENG

TITLE FUNCTIONAL SCHEMATIC
MOD 80
MBC WW

TASK NO. 03214
DWG NO. 35-407R09D08
SHEET 2 OF 11

BRUNING 44-231 16042

INTERDATA®


NOTE 3
05S01 1K P5
XB0
XB1
05S 19-057 SG
2F9 4F6
CCUE1
13 05S 19-057 SG 12 CREQ1
03S04 15 uH
03S05 470
DCREQ1
03S09 22 PF
05S 19-057 SG
NC
04S 19-062 SG
120-1 CREQ0
13H01 X153 15K
13H02 100PF
12H
19-042
ONE SHOT
X154
03J 19-059 SA
12J T SF 19-064
TORO
TBA F8, 2A7, A7
04K01 P5 1K
X229 G7
11J 19-056
IAO X137-0
X128 4N1
DLA101 M7
04K 19-055 SG
DLTRG1
2N3
X4001
7E2
FETCHV
2A3, A8, A4
4A6 MRR1
2N6 SCSTRIA
8R8 MWRTO
08J 19-055 SG
X130
08K 19-057 SG
X168
09H T SF 19-064
X164
X163
11H 19-058 SG
X165
09J 19-055 SG
DLA000 4N3
DLC090 4D2
06E 19-057 SG
DLC091 4A5
10K6 (9K6) NOTE 2 SCLRO
2A2 ENDCYLO
11J 19-056 SG
4R2 DLA350
4R3 DLA001
8R5 PRTO
4N5 CWCR1
11M 19-062 SG
CRDYO 119-1
2L2 ENDO
A140
2L2 ENDCYL1
02J 19-058 SG
X234
06E01 1K P5S
12K T SF 19-064
07E 19-058 SG
L2 END1
05S 19-057 SG
ENDOK
3N5 SDSTR1
08D 19-055 SG
X129
08K 19-057 SG
X167
4G1 X167
2G2 FETCH1
X149
08H 19-058 SG
END371
08D 19-055 SG
ENDSTO 2L7
4N2 DLARSTO
A141
X259
08F 19-060 SG
06F 19-057 SG
06D 19-055 SG
08D 19-055 SG
ARST1 7E2
SROB 2N3
4A5 X261
K9 SSTRO
06D 19-055 SG
X260
06E 19-057 SG
X235
4A4 DLC001
2N7 SCAIA
08E 19-058 SG
X265
P5S 06F01 1K
X148
DLA500 4N1
ENDIA 2L1
4M4 X161
4H3 SDWIA
10J 19-062 SG
INHO 10A-0
129-1 CA140
04M 19-055 SG
CA141
08E 19-058 SG
X264
X263
06F 19-057 SG
09D 19-061 SB
X251
06E 19-057 SG
X252
07D 19-057 SG
ENDOB 9G6
ENDOC 8H9, 9G9
03B 19-057 SG
SDRIB 6C9
SDROA 2A6, 4N3
SDRIA 5C9
2N6 SDAIB
233-0 MA140
P5 08T15 330
06T 19-055 SG
MA141
09F 19-058 SG
X262
7F3 STRA1
7F1 STRB1
06D 19-055 SG
N2 X229
12E 19-059 SA
ENDOD 9F2, 8L3, 8H7
ENDOE 7F9, 8L2
ENDOF 7E7
ENDOH 7A5, 2E3
PFTCH1
DLA101
M2
DLA100 4R3
09J 19-055 SG
04H 19-078 SGO
IPFO 136-0
PERR1 9R3
DPFO 236-0
11K 19-057 SG
PSTBA1
DLA400 4N2
ADDO 7A5, 9A9, 8F2
09D 19-061 SB
X137
13F 19-055 SG
06S 19-055 SG
08D 19-055 SG
4D4 DLC051
X238
07F T SF 19-064
DRSTO 4H3
N1 TBA
08A 19-055 SG
FADO 106-3
10K6 (7S7) NOTE 2 SCLRO
X241
02B 19-057 SG
SCR1B 6C9
SCR1A 5C9
06D01 P5 2.2K
SSTRO A5
02J 19-058 SG
P5 08A01 470
08A 19-055 SG
FECLK1
MRDY1 4F9
X163 4G5
PFTCHO
105-3 FECLKO

REVISIONS

REV	DESCRIPTION	ECO	DATE
R02	AT LOC J2, 03J01 WAS P/O DLARSTO & WAS CONN TO 03J02	3214-27	1-19-73
R03	AREA J9, ADDED 06D01 AREA M5, 10J-03 WAS 'MRR1' 10J-02 WAS 'SDWIA' 10J-04, 05 WERE N.C. 10J-06 WAS GND.	3214-30	3-30-73
R04	AREA B3 DELETED 03S02, 470; 03S07, 15 uH IN SERIS/PARALLEL WITH 120-1 & 04S-02. DELETED 03S09, 22 PF FROM 04S02, 03 TO GND. DELETED 11J & 12J, AREA K, L-2. AREA J3, 'X168' WAS 'X163' AREA C6, CONNECTION FROM 08E-02 TO 08E-04 WAS NOT SPEC.	3214-31	3-30-73
R05	ADDED: CO-ORDINATIONS FOR SCLRO GOING TO SHT. 10 IN AREAS F3 & H9. ADDED NOTE 2 CHANGED: SCAIA IN AREA A5 WAS SCSTRIA GOING TO F3 & 2N6. SCSTRIA IN AREA F3 WAS GOING TO B5. SDAIB IN AREA A6 WAS SDSTR1 GOING TO 2N5 & F4. SDSTR1 IN AREA F4 WAS GOING TO A6 CHANGED: REVERSED TRUE AND FALSE SYMBOLS ON FLOPS 12K-AREA D4, 12J-AREA J1, 09H-AREA K3, 09H-AREA K4.	3214-35	5-1-73
R06	AREA A4; IC 02J PINS 05 & 13, WAS NOT CONNECTED TO 06F PIN 08	3214-40	5-25-73
R07	AREA M4; IC 11M WAS 19-078. PIN CONNECTIONS WERE: 13-DLC091, 12-PRTO, 10-MRR1, 9-SCWIB, 5-MRR1, 4-X164, 2-DLA001, 1-DLA350, 6 & 8-CRDYO	1905	8-9-73
R08	AREA L2; DLA101 WAS DLA201 TO 4N5	1918	9-4-73
R09	AREA H4 4G1 WAS 2A6	1968	10-18-73
R10	ADDED NOTE 3, LOC'S A, B, C, 1, 2, 3 DELETED 3 GATES OUTPUTS, 05S-02, 04, 06, ALSO RUNS CB000, CB010, CB020, CB001, CB011 & CB021, ADDED NEW CIRCUITRY SAME LOC'S	2047	1/13/74

NOTES

1. STANDARD OPTION SHOWN
2. CO-ORDINATIONS SHOWN IN PARENTHESIS APPLY TO MOTHER BOARDS EQUIPPED WITH A 35-429 DAUGHTER BOARD.
3. GROUNDING 05S03 IS RECOMMENDED WHEN MBC, CPU OR IOU BOARD IS PLUGGED INTO EXTENDER BOARD. AT ALL OTHER TIMES 05S01 MUST BE A LOGIC HIGH (5V).

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MOD 80
MBC WW

TASK NO. 03214
DWG NO. 35-407R10D08
SHEET 3 OF 11

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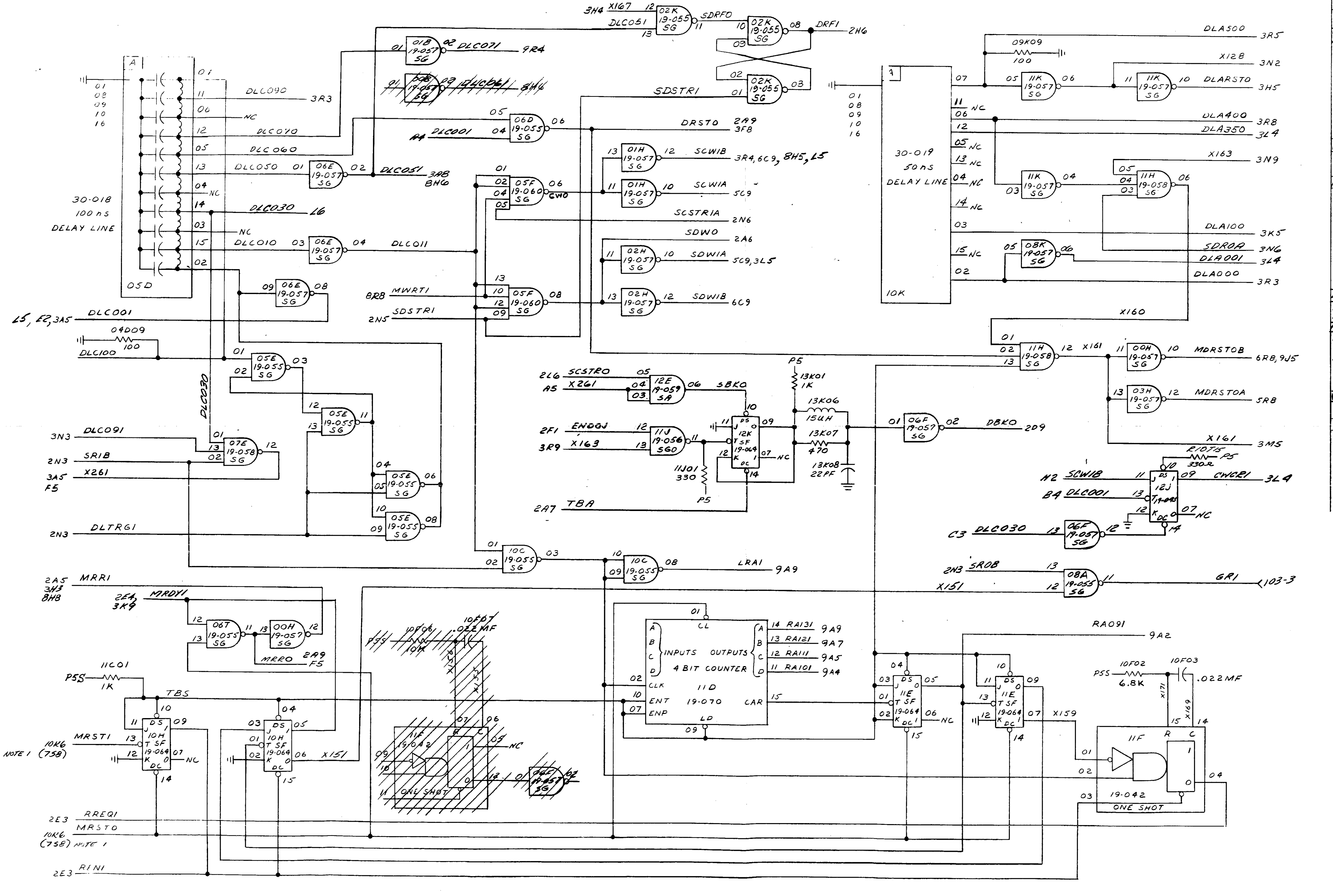
3H4 X167
DLC051
SDRFO
DRF1 2H6
01B 19-057 SG
DLC071 9R4
~~01 00B 19-057 SG 02 DLC061 8H6~~
30-018 100 ns DELAY LINE
OSD
DLC090 3R3
DLC070
DLC060
DLC050
DLC051 3A8 8H6
DLC030 L6
DLC010
DLC011
SDSTR1
06D 19-055 SG
DLC001
DRST0 2A9 3F8
SCW1B 3R4, 6C9, 8H5, L5
SCW1A 5C9
SCSTR1A 2N6
SDW0 2A6
SDW1A 5C9, 3L5
SDW1B 6C9
05F 19-060 SG
CWO
8R8 MWRT1
2N5 SDSTR1
L5, E2, 3A5 DLC001
04D09 100
DLC100
DLC091 3N3
SR1B 2N3
X261 3A5 F5
DLTRG1 2N3
07E 19-058 SG
05E 19-055 SG
10C 19-055 SG
LRA1 9A9
2L6 SCSTR0
A5 X261
12E 19-059 SA
SBK0
2F1 ENDGJ
3R9 X163
11J 19-056 SG0
12K 19-064
11J01 330
P5
13K01 1K
13K06 15uH
13K07 470
13K08 22PF
06F 19-057 SG
DBK0 2D9
2A7 TBA
30-019 50 ns DELAY LINE
10K
DLA500 3R5
09K09 100
X128 3N2
11K 19-057 SG
DLARST0 3H5
DLA400 3R8
DLA350 3L4
X163 3N9
11H 19-058 SG
DLA100 3K5
SDR0A 3N6
DLA001 3L4
DLA000 3R3
08K 19-057 SG
X160
X161
MDRST0B 6R8, 9J5
00H 19-057 SG
03H 19-057 SG
MDRST0A 5R8
X161 3M5
R1075 330Ω P5
H2 SCW1B
B4 DLC001
12J 19-064
CWCR1 3L4
C3 DLC030
2N3 SR0B
X151
08A 19-055 SG
GR1 103-3
2A5 3H3 8H8 MRR1
2E4, 3K9 MRDY1
06T 19-055 SG
00H 19-057 SG
MRR0 2A9 F5
P5S 11C01 1K
TBS
10K6 (7S8) NOTE 1 MRST1
10H 19-064
X151
10F06 10K
10F07 .022MF
11F 19-042 ONE SHOT
06F 19-057 SG
INPUTS OUTPUTS 4 BIT COUNTER 11D 19-070
CLK ENT ENP LD CAR CL
RA131 9A9
RA121 9A7
RA111 9A5
RA101 9A4
RA091 9A2
11E 19-064
P5S 10F02 6.8K
10F03 .022MF
X171 X169
X159
11F 19-042 ONE SHOT
2E3 RREQ1
10K6 (7S8) NOTE 1 MRST0
2E3 R1N1

REVISIONS

INITIAL ISSUE WAS R01 IN AREA M7 10F02 WAS 4.7K

C9 | 03214-28 | 1-31-73 | R02

AREA C8, 10H-05 WAS N.C.
AREA E, F8, DELETED 11F & 06F.
11F-09 WAS 'X151'
11F-10 WAS 'RREQ1'
11F-11 WAS 'MRST0'
06F-02 WAS 'MRDY1'
AREA G5, 07F-12 WAS GND.
AREA E1, DELETED 00B
00B-01 WAS 'DLC060'

HM | 3214-30 | 3-30-73 | R03

REVISED AREA G, H, J-5. SEE ECR 3214-31 FOR PREVIOUS CIRCUIT.

HM | 3214-31 | 3-30-73 | R04

CHANGED: REVERSED TRUE AND FALSE SYMBOLS ON FLOPS 10H-AREA B9, 10H-AREA C9.
ADDED: CO-ORDINATIONS FOR MRST1 GOING TO SHT. 10 IN AREA A8 AND FOR MRST0 GOING TO SHT. 10 IN AREA A9
ADDED NOTE 1

DB | 3214-35 | 5 1 1 | R05

AREA M5: ADDED GATES 12J & 06F

PE | 1905 | 8-9-73 | R06

AREA L2: 10K PIN 04 WAS DLA200 AND CONN. TO 11K PIN 03. AREA M2: 11N PIN 04 WAS DLA201 TO 3N2 ; ADDED CONN BETWEEN 10K PIN 06 AND 11K PIN 03

PE | 1918 | 8-9-73 | R07

AREA G1, ADDED IC PACK 02K (3 GATES)

1968 | 10-18-73 | R08

NOTES
1. CO-ORDINATIONS SHOWN IN PARENTHESIS APPLY TO MOTHER BOARDS EQUIPPED WITH A 35-429 DAUGHTER BOARD.

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MOD 80
MBC WW

TASK NO. 03214
DWG NO. 35-407R08D008
SHEET OF 4-11

BRUNING 44-231 16042

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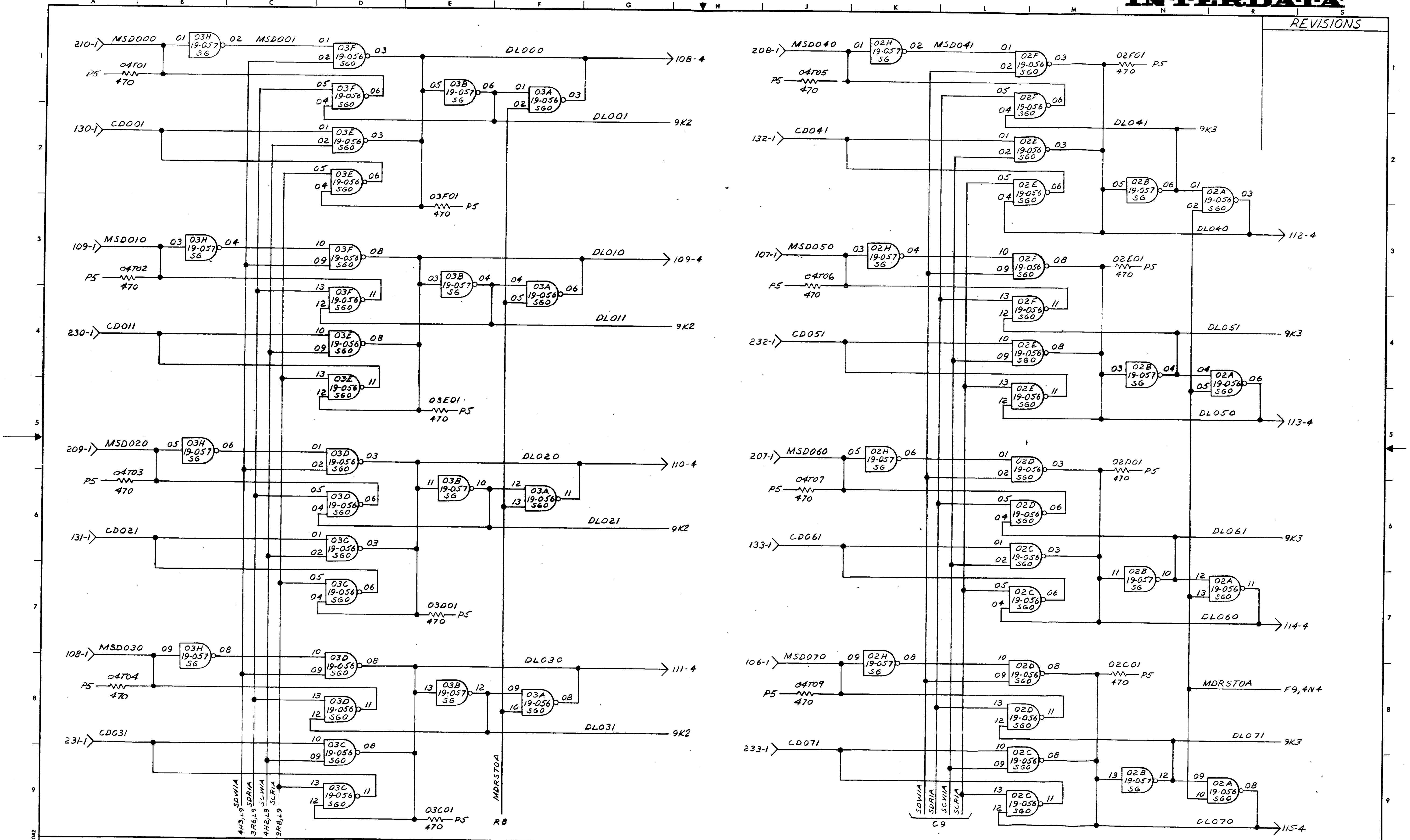
REVISIONS


210-1
MSD000
03H 19-057 SG
MSD001
03F 19-056 SG0
DL000
108-4
P5
04T01
470
03B 19-057 SG
03A 19-056 SG0
DL001
9K2
130-1
CD001
03E 19-056 SG0
03F01
109-1
MSD010
03H 19-057 SG
04T02
DL010
109-4
230-1
CD011
DL011
03E01
209-1
MSD020
04T03
03D 19-056 SG0
DL020
110-4
131-1
CD021
03C 19-056 SG0
DL021
03D01
108-1
MSD030
04T04
DL030
111-4
231-1
CD031
DL031
03C01
SDW1A
SDR1A
SCW1A
SCR1A
4H3,L9
3R6,L9
4H2,L9
3R8,L9
MDRST0A
R8
208-1
MSD040
02H 19-057 SG
MSD041
02F 19-056 SG0
02F01
04T05
132-1
CD041
02E 19-056 SG0
DL041
9K3
02B 19-057 SG
02A 19-056 SG0
DL040
112-4
107-1
MSD050
04T06
02E01
232-1
CD051
DL051
DL050
113-4
207-1
MSD060
04T07
02D 19-056 SG0
02D01
133-1
CD061
02C 19-056 SG0
DL061
DL060
114-4
106-1
MSD070
04T09
02C01
MDRST0A
F9,4N4
233-1
CD071
DL071
DL070
115-4
C9

NOTES

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MOD 80
MBC WW

TASK NO. 03214
DWG NO. 35-407R01D08
SHEET OF 5-11

BRUNING 44-231 16042

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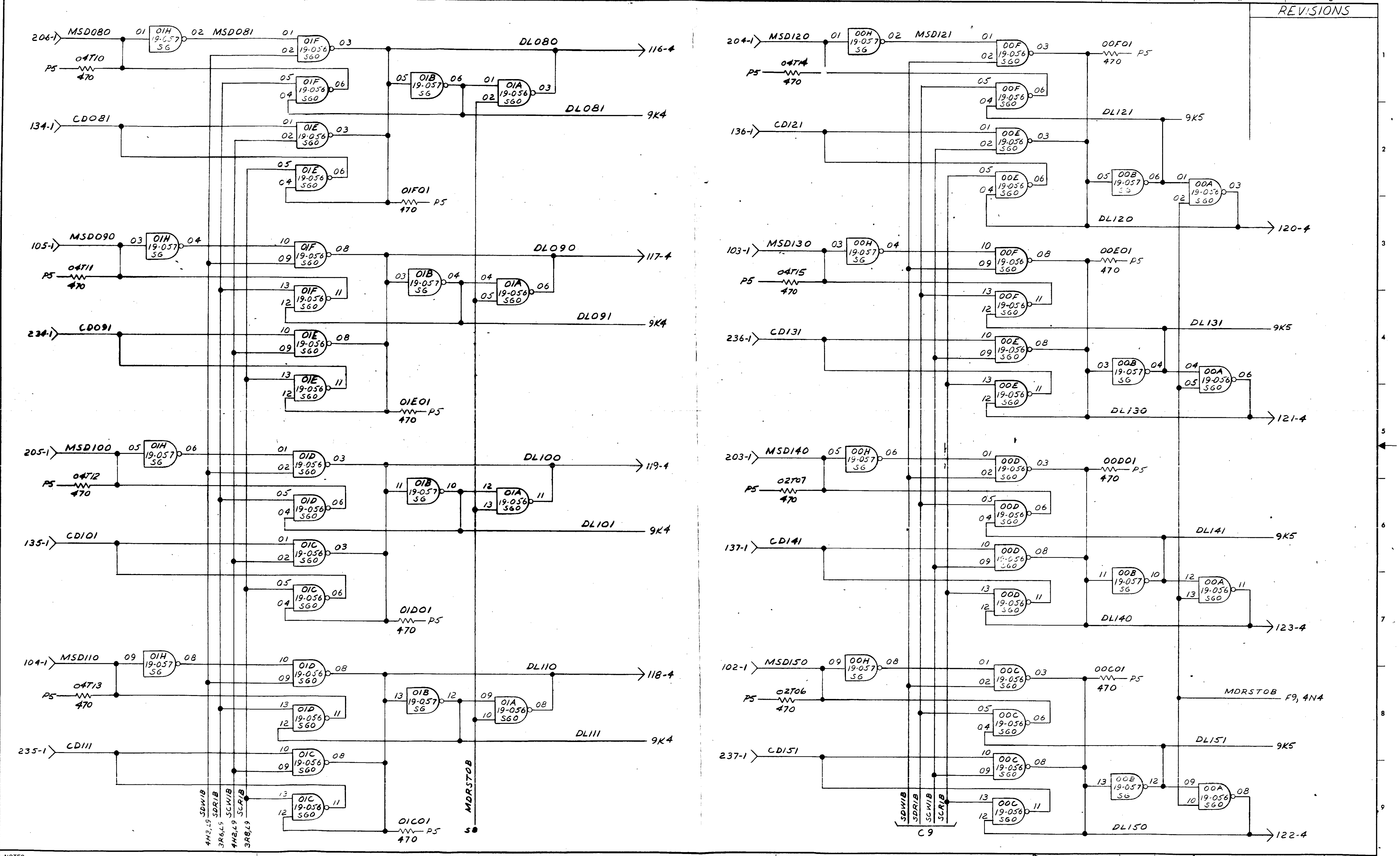
REVISIONS


206-1 MSD080
O1H 19-057 SG
MSD081
O1F 19-056 S60
DL080
116-4
P5 04T10 470
O1B 19-057 SG
O1A 19-056 S60
DL081
9K4
134-1 CD081
O1E 19-056 S60
O1FO1 470 P5
105-1 MSD090
04T11
DL090
117-4
DL091
234-1 CD091
O1E01 470 P5
205-1 MSD100
04T12
O1D 19-056 S60
DL100
119-4
DL101
135-1 CD101
O1C 19-056 S60
O1D01 470 P5
104-1 MSD110
04T13
DL110
118-4
DL111
235-1 CD111
O1C01 470 P5
MDRSTOB
S8
SDW1B 4H3,L9
SDR1B 3R6,L9
SCW1B 4H2,L9
SCR1B 3R8,L9
204-1 MSD120
OOH 19-057 SG
MSD121
04T14 470
OOF 19-056 S60
OOFO1 470 P5
DL121
9K5
136-1 CD121
OOE 19-056 S60
OOB 19-057 SG
OOA 19-056 S60
DL120
120-4
103-1 MSD130
04T15
OOE01 470 P5
236-1 CD131
DL131
9K5
DL130
121-4
203-1 MSD140
02T07
OOD 19-056 S60
OOD01 470 P5
137-1 CD141
DL141
9K5
DL140
123-4
102-1 MSD150
02T06
OOC 19-056 S60
OOC01 470 P5
MDRSTOB F9, 4N4
237-1 CD151
DL151
9K5
DL150
122-4
SDW1B SDR1B SCW1B SCR1B
C9

NOTES

BRUNING 44-231 16042

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MOD 80
MBC WW

TASK NO. 03214
DWG NO. 35-407R01D08
SHEET 6 OF 11

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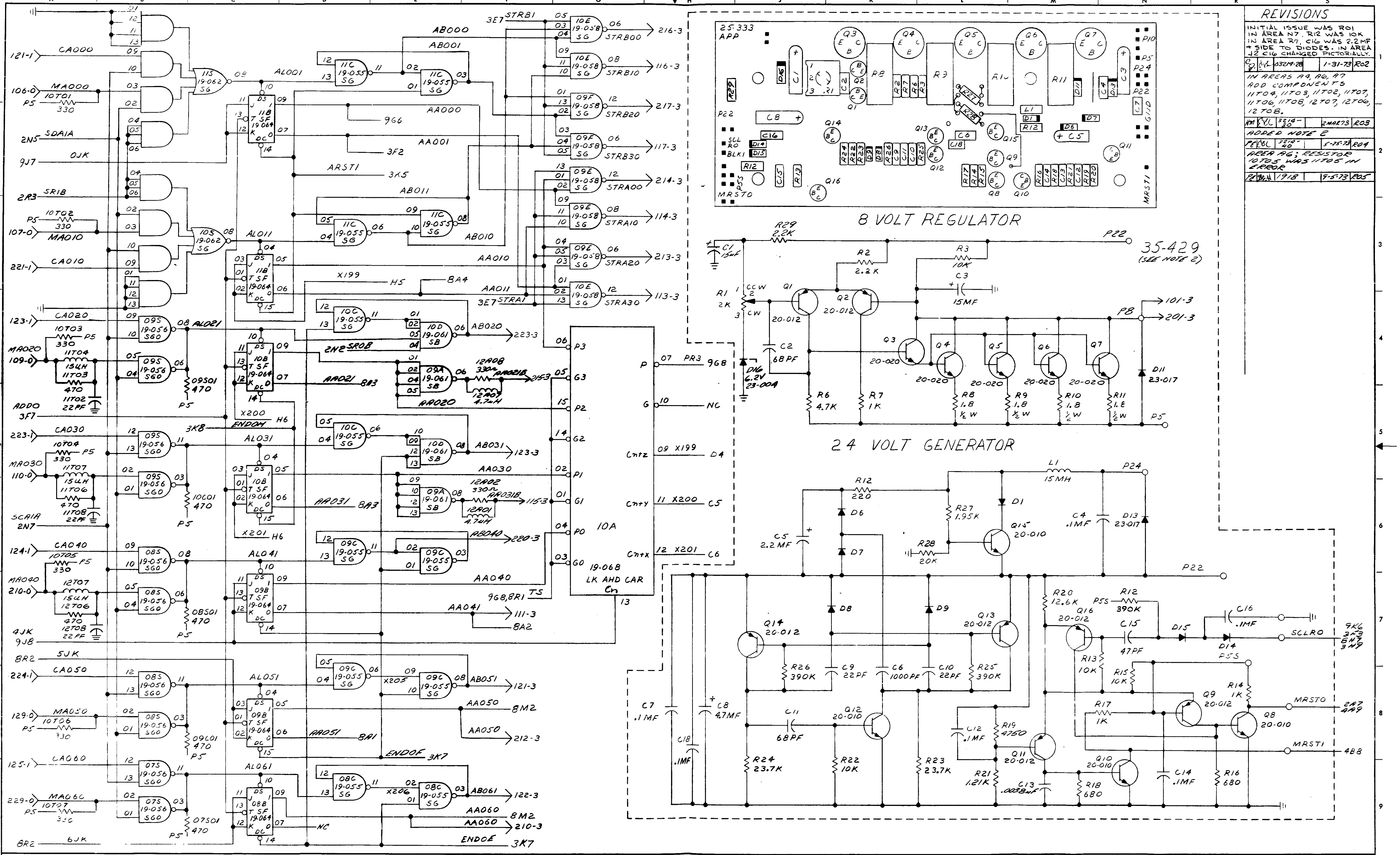

8 VOLT REGULATOR
24 VOLT GENERATOR
35-429 (SEE NOTE 2)
25-333 APP
10A 19-068 LK AHD CAR Cn
P3
G3
P2
G2
P1
G1
P0
G0
Cn+z
Cn+y
Cn+x
PR3 9G8
X199 D4
X200 C5
X201 C6
STRB00 216-3
STRB10 116-3
STRB20 217-3
STRB30 117-3
STRA00 214-3
STRA10 114-3
STRA20 213-3
STRA30 113-3
CA000
MA000
SDA1A
OJK
SR1B
CA010
MA010
CA020
MA020
CA030
MA030
SCA1A
CA040
MA040
CA050
MA050
CA060
MA060
AL001
AL011
AL021
AL031
AL041
AL051
AL061
AB000
AB001
AB010
AB011
AB020 223-3
AB031 123-3
AB040 220-3
AB051 121-3
AB061 122-3
AA000
AA001
AA010
AA011
AA020 215-3
AA021 8B3
AA030
AA031 8A3 115-3
AA040
AA041 111-3 8A2
AA050 8M2 212-3
AA051 8A1
AA060 8M2 210-3
ENDOC
ENDOD
ENDOE 3K7
ENDOF 3K7
ARST1 3K5
P22
P8 101-3 201-3
P24
P5
SCLRO
MRSTO
MRST1
Q1 Q2 20-012
Q3 Q4 Q5 Q6 Q7 20-020
D16 6.2V 23-004
D11 23-017
D13 23-017
L1 15MH
C3 15MF
Q15 20-010
Q14 20-012
Q13 20-012
Q16 20-012
Q12 20-010
Q11 20-012
Q10 20-010
Q9 20-012
Q8 20-010

REVISIONS

INITIAL ISSUE WAS R01
IN AREA N7, R12 WAS 10K
IN AREA R7, C16 WAS 2.2MF
+ SIDE TO DIODES. IN AREA
J2 C16 CHANGED PICTORIALLY.

CP	CVL	03214-28		1-31-73	R02

IN AREAS A4, A6, A7
ADD COMPONENTS
11T04, 11T03, 11T02, 11T07,
11T06, 11T08, 12T07, 12T06,
12T08.

HM	CVL	3214-30		2MAR73	R03

ADDED NOTE 2

PE	EBL	3214-40		5-25-73	R04

AREA A6; RESISTOR
10T05 WAS 11T05 IN
ERROR

PE	McH	1918		9-5-73	R05

NOTES

1. UNLESS OTHERWISE SPECIFIED ALL DIODES ARE [illegible]

2. 35-407 R10 WAS ORIGINALLY EQUIPPED WITH 35-429.

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MOD 80
MBC WW

TASK NO. 03214
DWG NO. 35-407 K051.08
SHEET 7 OF 11

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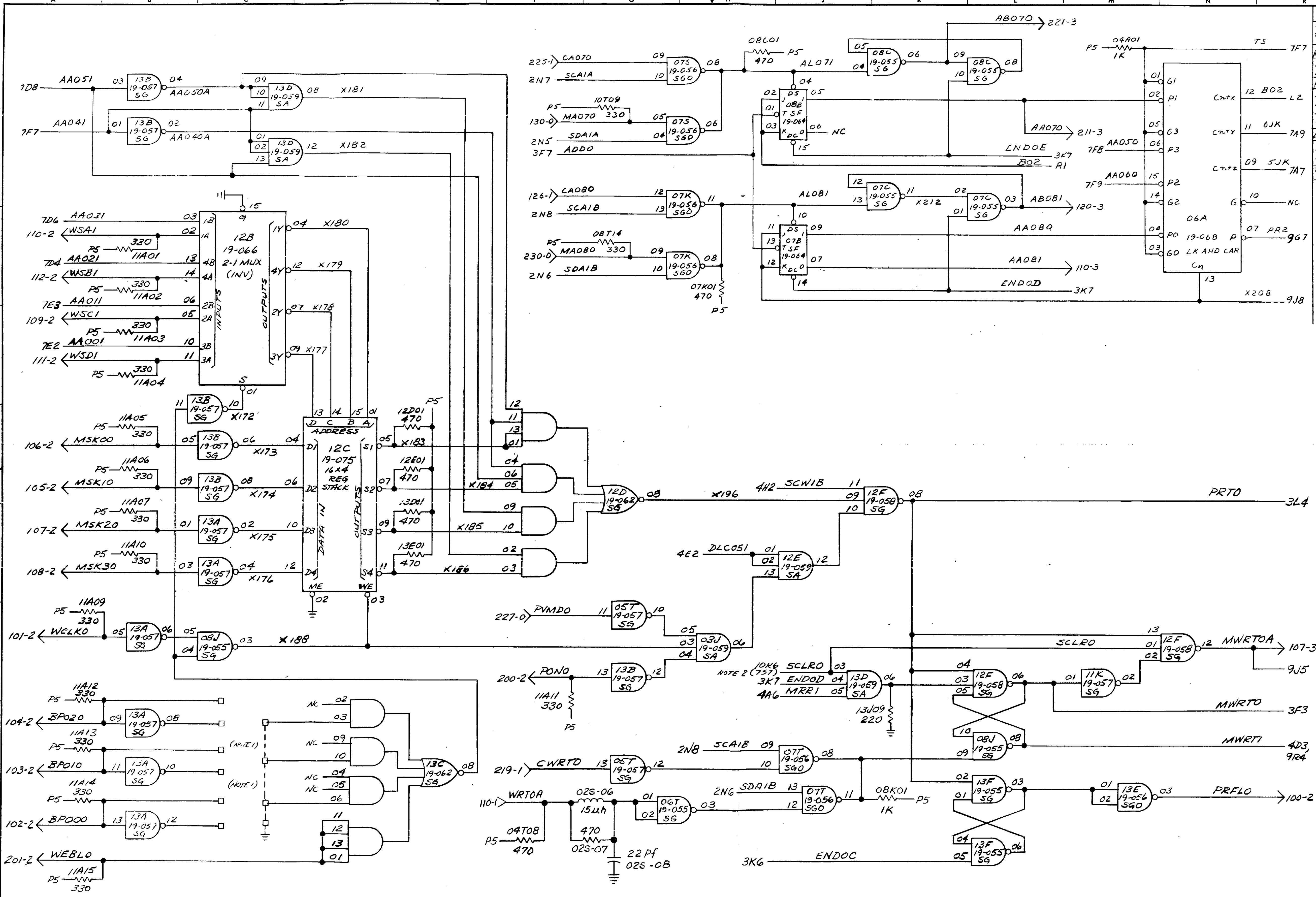


7D8
AA051
7F7
AA041
13B 19-057 SG
AA050A
AA040A
13D 19-059 SA
X181
X182
7D6 AA031
110-2 WSA1
7D4 AA021
112-2 WSB1
7E3 AA011
109-2 WSC1
7E2 AA001
111-2 WSD1
P5
330
11A01
11A02
11A03
11A04
12B 19-066 2-1 MUX (INV)
INPUTS
OUTPUTS
X180
X179
X178
X177
X172
106-2 MSK00
105-2 MSK10
107-2 MSK20
108-2 MSK30
11A05
11A06
11A07
11A10
13B 19-057 SG
13A 19-057 SG
X173
X174
X175
X176
12C 19-075 16x4 REG STACK
ADDRESS
DATA IN
OUTPUTS
ME
WE
12D01 470
12E01 470
13D01 470
13E01 470
X183
X184
X185
X186
12D 19-062 SG
X196
101-2 WCLKO
11A09
08J 19-055 SG
X188
104-2 BP020
103-2 BP010
102-2 BP000
201-2 WEBLO
11A12
11A13
11A14
11A15
(NOTE 1)
13C 19-062 SG
NC
225-1 CA070
2N7 SCA1A
130-0 MA070
10T09 330
2N5 SDA1A
3F7 ADDO
07S 19-056 SGO
08C01 470
AL071
08C 19-055 SG
AB070 221-3
08B T SF 19-064
AA070 211-3
ENDOE 3K7
B02 R1
126-1 CA080
2N8 SCA1B
230-0 MA080
08T14 330
2N6 SDA1B
07K 19-056 SGO
07K01 470
AL081
07C 19-055 SG
X212
AB081 120-3
AA08Q
07B T SF 19-064
AA081 110-3
ENDOD 3K7
P5 04A01 1K
TS 7F7
7F8 AA050
7F9 AA060
06A 19-068 LK AHD CAR
Cn+x 12 B02 L2
Cn+y 11 6JK 7A9
Cn+z 09 5JK 7A7
G 10 NC
P 07 PR2 9G7
Cn 13
X208 9J8
4H2 SCW1B
12F 19-058 SG
PRTO 3L4
4E2 DLC051
12E 19-059 SA
227-0 PVMDO
05T 19-057 SG
03J 19-059 SA
200-2 PONO
11A11 330
NOTE 2 (757)
10K6 SCLRO
3K7 ENDOD
4A6 MRR1
13D 19-059 SA
13J09 220
SCLRO
MWRTOA 107-3
9J5
11K 19-057 SG
MWRTO 3F3
08J 19-055 SG
MWRT1 4D3, 9R4
219-1 CWRTO
2N8 SCA1B
07T 19-056 SGO
2N6 SDA1B
08K01 1K P5
110-1 WRTOA
02S-06 15μh
470 02S-07
22 Pf 02S-08
06T 19-055 SG
04T08 470
13F 19-055 SG
13E 19-056 SGO
PRFLO 100-2
3K6 ENDOC

REVISIONS					
INITIAL ISSUE WAS R01 AREA H6, 'DLC051' WAS 'DLC061'					
HM		3214-30		3 30-73	R02
AREA M1, 04A01 WAS NOT SPEC. AREA C7, 08J-06 WAS -03.					
HM		3214-31		3-30-73	R03
ADDED: CO-ORDINATION FOR SCLRO GOING TO SHT. 10 IN AREA J7. ADDED NOTE 2					
DB		3214-35		5-1-73	R04
IN AREA G9 ADDED 02S-06, 02S-07 & 02S-08 TO WRTOA					
Tcp		1968		10-18-73	R05

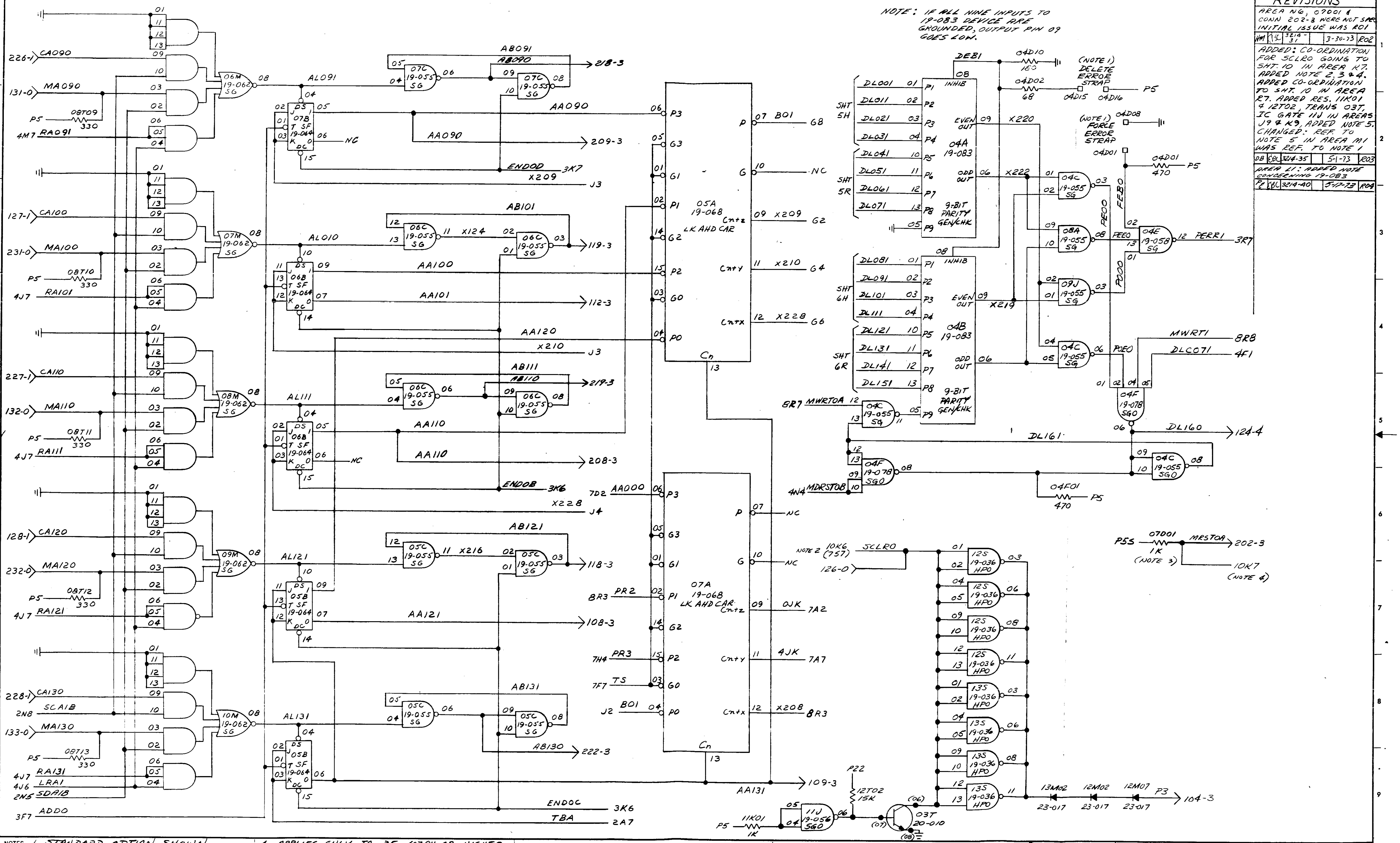
NOTES 1. STANDARD OPTION SHOWN.
2. CO-ORDINATIONS SHOWN IN PARENTHESIS APPLY TO MOTHER BOARDS EQUIPPED WITH A 35-429 DAUGHTER BOARD.

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MOD 80
MBC WW

TASK NO. 03214
DWG NO. 35-407R05D08
SHEET 8 OF 11

INTERDATA®



NOTE: IF ALL NINE INPUTS TO 19-083 DEVICE ARE GROUNDED, OUTPUT PIN 09 GOES LOW.

226-1 CA090
131-0 MA090
P5 08T09 330
4M7 RA091
06M 19-062 SG
AL091
AB091
AB090
07C 19-055 SG
→ 218-3
07B T SF 19-064
AA090
→ 209-3
ENDOD 3K7
X209 J3
127-1 CA100
231-0 MA100
P5 08T10 330
4J7 RA101
07M 19-062 SG
AL010
AB101
06C 19-055 SG
X124
→ 119-3
06B T SF 19-064
AA100
AA101
→ 112-3
AA120
X210 J3
227-1 CA110
132-0 MA110
P5 08T11 330
4J7 RA111
08M 19-062 SG
AL111
AB111
AB110
→ 219-3
AA110
→ 208-3
ENDOB 3K6
X228 J4
128-1 CA120
232-0 MA120
P5 08T12 330
4J7 RA121
09M 19-062 SG
AL121
AB121
05C 19-055 SG
X216
→ 118-3
05B T SF 19-064
AA121
→ 108-3
228-1 CA130
2N8 SCAIB
133-0 MA130
P5 08T13 330
4J7 RA131
4J6 LRAI
2N5 SDAIB
3F7 ADDO
10M 19-062 SG
AL131
AB131
AB130
→ 222-3
AA131
→ 109-3
ENDOC 3K6
TBA 2A7
05A 19-068 LK AHD CAR
P3 G3 G1 P1 G2 P2 G0 P0
P 07 B01 G8
G 10 NC
Cn+z 09 X209 G2
Cn+y 11 X210 G4
Cn+x 12 X228 G6
Cn 13
07A 19-068 LK AHD CAR
7D2 AA000
8R3 PR2
7H4 PR3
7F7 TS
J2 B01
07 NC
10 NC
09 0JK 7A2
11 4JK 7A7
12 X208 8R3
SHT 5H
SHT 5R
DL001 DL011 DL021 DL031 DL041 DL051 DL061 DL071
04A 19-083 9-BIT PARITY GEN/CHK
INHIB
EVEN OUT
ODD OUT
DEBI
04D10 1K
04D02 68
(NOTE 1) DELETE ERROR STRAP
04D15 04D16 P5
(NOTE 1) FORCE ERROR STRAP
04D08
04D01 470 P5
X220
X222
SHT 6H
SHT 6R
DL081 DL091 DL101 DL111 DL121 DL131 DL141 DL151
04B 19-083 9-BIT PARITY GEN/CHK
X219
04C 19-055 SG
08A 19-055 SG
09J 19-055 SG
04E 19-058 SG
PERRI 3R7
FEBO
FEEO
PEEO
POOO
POEO
MWRTI 8R8
DLC071 4F1
04F 19-078 SGO
DL160 → 124-4
DL161
8R7 MWRTOA
04F 19-078 SGO
4N4 MDRSTOB
04F01 470 P5
04C 19-055 SGO
P5S 07D01 1K (NOTE 3)
MRSTOA → 202-3
10K7 (NOTE 4)
NOTE 2 10K6 (757) SCLRO
126-0
12S 19-036 HPO
13S 19-036 HPO
13M02 12M02 12M07 P3
23-017 23-017 23-017
→ 104-3
P22
12T02 15K
03T 20-010
P5 11K01 1K
11J 19-056 SGO

REVISIONS

AREA N6, 07D01 & CONN 202-3 WERE NOT SPEC. INITIAL ISSUE WAS R01

HM		3214-31		3-30-73	R02

ADDED: CO-ORDINATION FOR SCLRO GOING TO SHT. 10 IN AREA K7. ADDED NOTE 2, 3 & 4. ADDED CO-ORDINATION TO SHT. 10 IN AREA R7. ADDED RES. 11K01 & 12T02, TRANS 03T, IC GATE 11J IN AREAS J9 & K9, ADDED NOTE 5. CHANGED: REF. TO NOTE 5 IN AREA M1 WAS REF. TO NOTE 1

DB	EBC	3214-35		5-1-73	R03

AREA L1: ADDED NOTE CONCERNING 19-083

PE	EBC	3214-40		5-17-73	R04

NOTES
1. STANDARD OPTION SHOWN.
2. CO-ORDINATIONS SHOWN IN PARENTHESIS APPLY TO MOTHER BOARDS EQUIPPED WITH A 35-429 DAUGHTER BOARD.
3. RESISTOR 07D01 EQUIPPED ON 35-407R10 ONLY.
4. APPLIES ONLY TO 35-407R11 OR HIGHER REV. LEVEL.

BRUNING 44-231 16042

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

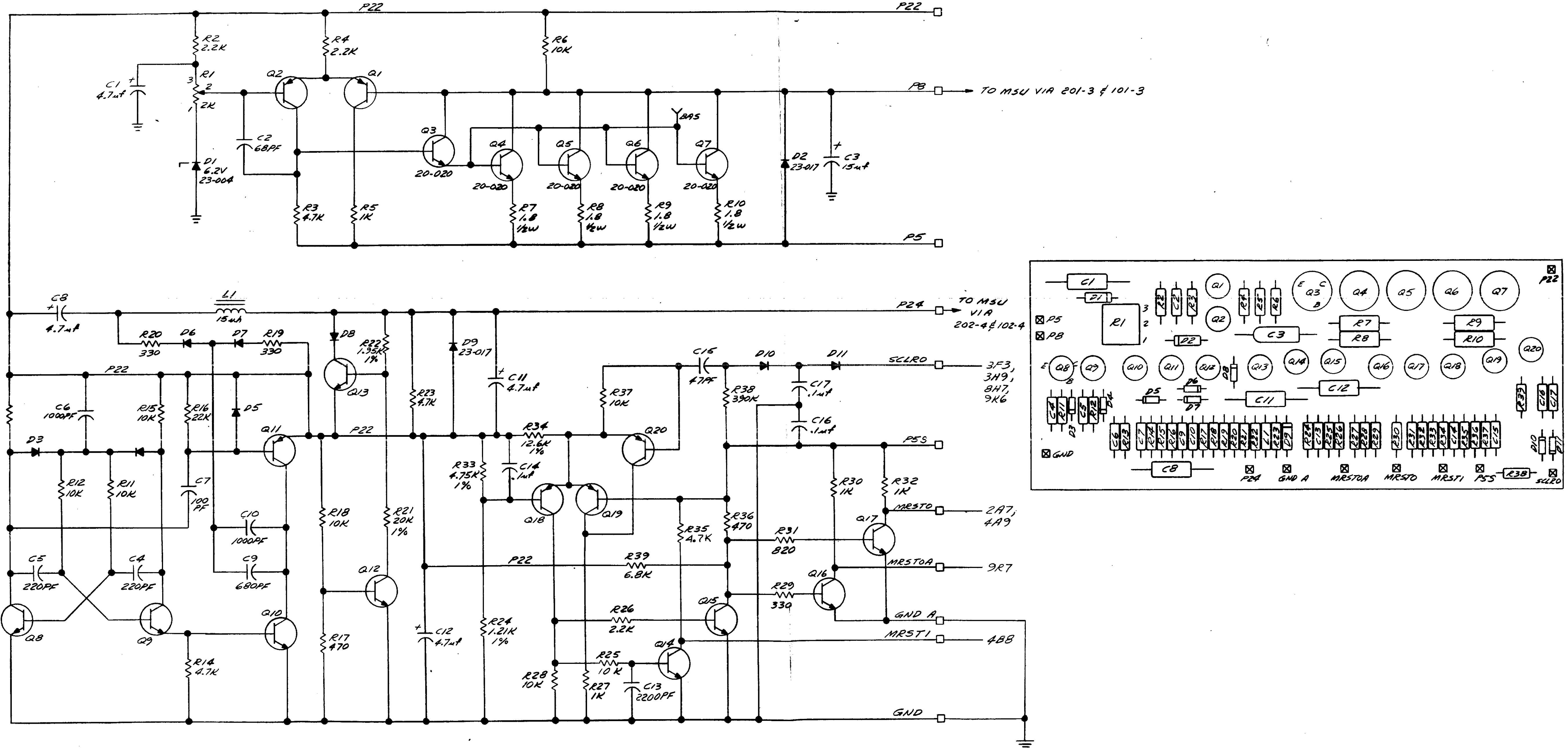
TITLE FUNCTIONAL SCHEMATIC
MOD 80
MBC WW

TASK NO. 03214
DWG NO. 35-407R04D08
SHEET 9 OF 11

INTERDATA®

REVISIONS					
ADDED NOTE 2					
PE	CVL	3214-40		5-25-73	R01
AREA G7 & G8: R35 WAS 1K, R25 WAS 22K, C13 WAS 1000PF					
PE	JH	2018		12-10-73	R02

35-478
(SEE NOTE 2)


P22
R2 2.2K
R4 2.2K
R6 10K
C1 4.7uf
R1 2K
3
2
1
Q2
Q1
C2 68PF
D1 6.2V 23-004
Q3 20-020
Q4 20-020
Q5 20-020
Q6 20-020
Q7 20-020
BAS
R3 4.7K
R5 1K
R7 1.8 1/2W
R8 1.8 1/2W
R9 1.8 1/2W
R10 1.8 1/2W
D2 23-017
C3 15uf
P8
TO MSU VIA 201-3 & 101-3
P5
C8 4.7uf
L1 15uh
P24
TO MSU VIA 202-4 & 102-4
R20 330
D6
D7
R19 330
D8
R22 1.95K 1%
Q13
D9 23-017
C11 4.7uf
R13 10K
C6 1000PF
R15 10K
R16 22K
D5
D3
R12 10K
R11 10K
C7 100 PF
Q11
R23 4.7K
C10 1000PF
C9 680PF
C5 220PF
C4 220PF
Q8
Q9
Q10
R14 4.7K
R18 10K
R21 20K 1%
Q12
R17 470
C12 4.7uf
R33 4.75K 1%
R34 12.6K 1%
C14 .1uf
Q18
Q19
Q20
R37 10K
C15 47PF
D10
D11
SCLR0
3F3, 3H9, 8H7, 9K6
R38 390K
C17 .1uf
C16 .1uf
P5S
R30 1K
R32 1K
MRST0
2A7, 4A9
R36 470
R35 4.7K
R31 820
Q17
R39 6.8K
MRST0A
9R7
R29 330
Q16
Q15
R26 2.2K
GND A
MRST1
4B8
R24 1.21K 1%
R28 10K
R25 10K
R27 1K
C13 2200PF
Q14
GND
C1
D1
R1
R2
C2
R3
Q1
Q2
D2
R4
R5
R6
C3
Q3
E
C
B
Q4
Q5
Q6
Q7
R7
R8
R9
R10
P22
P5
P8
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
C4
R11
D3
C5
R12
D4
D5
D6
D7
D8
C11
C12
R39
C16
C17
C6
R13
C7
R14
R15
R16
C9
C10
R17
R18
R19
R20
R21
R22
L1
R23
D9
R24
C13
R25
R26
R27
R28
R29
R30
R31
R32
R33
R34
C14
R35
R36
R37
C15
D10
D11
GND
C8
P24
GND A
MRST0A
MRST0
MRST1
P5S
R38
SCLR0

NOTES
1. UNLESS OTHERWISE SPECIFIED ALL DIODES ARE 23-001, NPN TRANS. ARE 20-010, PNP TRANS. ARE 20-012.

2. 35-407 R11 IS EQUIPPED WITH 35-478.

BRUNING 44-231 16042

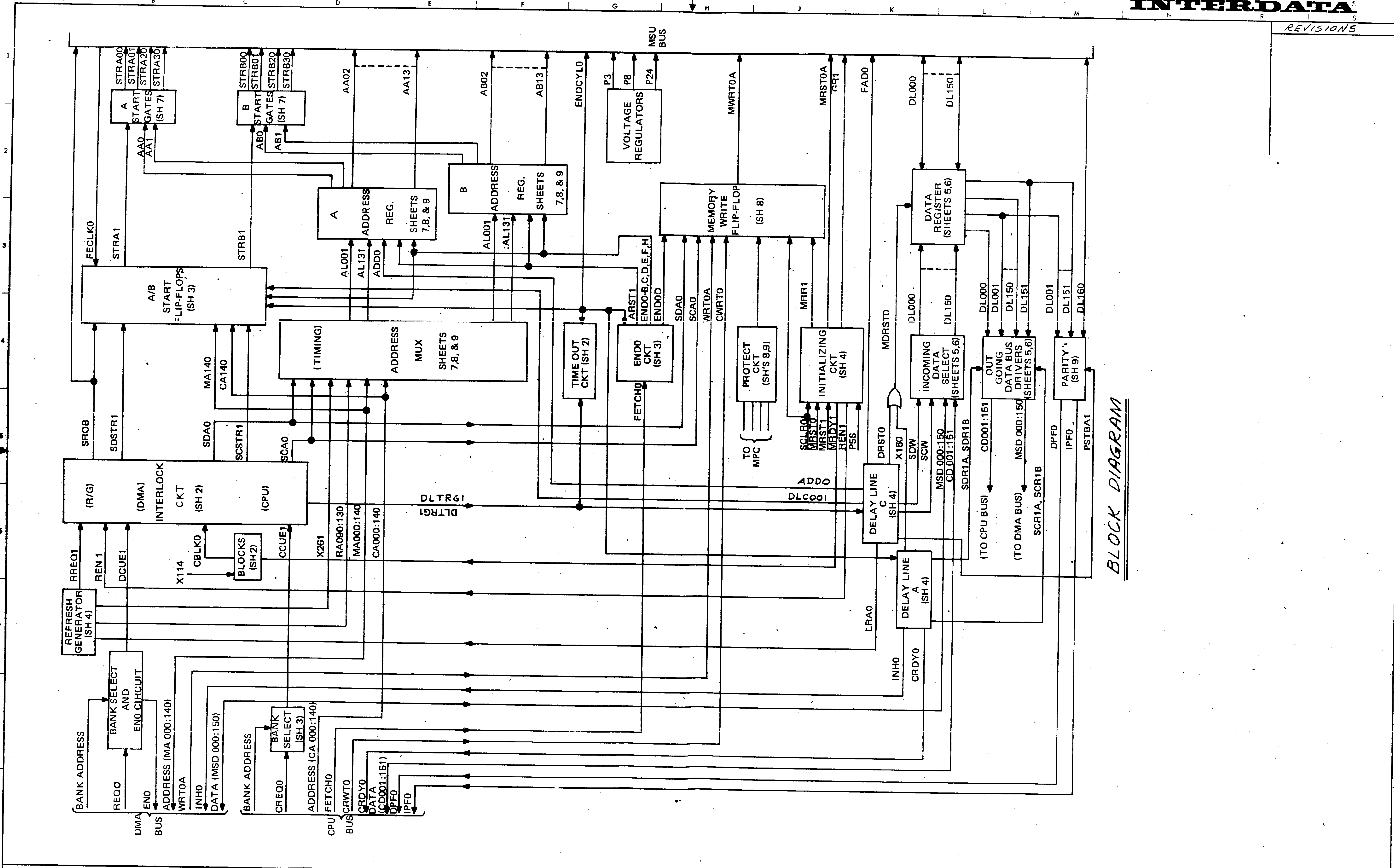
NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MOD 80
MBC WW

TASK NO. 03214
DWG NO. 35-407R02 D08
SHEET OF 10-11

INTERDATA

REVISIONS


BLOCK DIAGRAM
MSU BUS
A START GATES (SH 7)
B START GATES (SH 7)
STRA00 STRA01 STRA20 STRA30
STRB00 STRB01 STRB20 STRB30
AA0 AA1 AB0 AB1
AA02 AA13 AB02 AB13
A ADDRESS REG. SHEETS 7,8, & 9
B ADDRESS REG. SHEETS 7,8, & 9
ENDCYL0
VOLTAGE REGULATORS
P3 P8 P24
MWRT0A
MEMORY WRITE FLIP-FLOP (SH 8)
MRST0A CR1
FAD0
DL000 DL150
DATA REGISTER (SHEETS 5,6)
FECLK0 STRA1 STRB1
A/B START FLIP-FLOPS (SH 3)
AL001 AL131 ADD0
(TIMING) ADDRESS MUX SHEETS 7,8, & 9
TIME OUT CKT (SH 2)
ARST1 END0-B,C,D,E,F,H END0D
END0 CKT (SH 3)
FETCH0
SDA0 SCA0 WRT0A CWRT0
PROTECT CKT (SH'S 8,9)
TO MPC
MRR1
INITIALIZING CKT (SH 4)
SCLR0 MRST0 MRST1 MBDY1 REN1 P5S
MDRST0
INCOMING DATA SELECT (SHEETS 5,6)
OUT GOING DATA BUS DRIVERS (SHEETS 5,6)
PARITY (SH 9)
DL000 DL001 DL150 DL151 DL160
MA140 CA140
SROB SDSTR1 SDA0 SCSTR1 SCA0
(R/G) (DMA) INTERLOCK CKT (SH 2) (CPU)
DLTRG1
ADD0
DLC001
DELAY LINE C (SH 4)
DRST0 X160 SDW SCW
MSD 000:150 CD 001:151
SDR1A, SDR1B
CD001:151 (TO CPU BUS)
MSD 000:150 (TO DMA BUS)
SCR1A, SCR1B
DPF0 IPF0 PSTBA1
DELAY LINE A (SH 4)
LRA0 INH0 CRDY0
RREQ1 REN 1 DCUE1
CBLK0 X114 BLOCKS (SH2)
CCUE1 X261 RA090:130 MA000:140 CA000:140
REFRESH GENERATOR (SH 4)
BANK SELECT AND EN0 CIRCUIT
BANK SELECT (SH 3)
BANK ADDRESS REQ0 EN0 ADDRESS (MA 000:140) WRT0A INH0 DATA (MSD 000:150)
DMA BUS
BANK ADDRESS CREQ0 ADDRESS (CA 000:140) FETCH0 CRWT0 CRDY0 DATA (CD001:151) DPF0 IPF0
CPU BUS
A B C D E F G H J K L M N R S
1 2 3 4 5 6 7 8 9

NOTES

NAME

TITLE DATE

DRAFT

CHK

ENGR

DIR ENG

TITLE *FUNCTIONAL SCHEMATIC*

MOD 80
MBC WW

03214 SHEET OF

35-407 *208* *11* *11*

BRUNING 44 231 16042

INTERDATA®

SHEET LOCATION	ROW 2	TERM. NO.	ROW 1	SHEET LOCATION
——	GND	24	DL160	3J1
——		23	DL140	3H1
——		22	DL150	3H1
——		21	DL130	3J2
——		20	DL120	3J2
——		19	DL100	3H2
——		18	DL110	3H2
——		17	DL090	3J3
——		16	DL080	3J3
——		15	DL070	3H3
——		14	DL060	3H3
——		13	DL050	3J4
——		12	DL040	3J4
——		11	DL030	3H4
——		10	DL020	3H4
——		09	DL010	3H9
——		08	DL000	3H9
——		07	P5S	4N4
——	GND	06	SR0B	4D2
3A1	P15	05	P15	3A1
——	GND	04	P5	3M2
——	GND	03	P5	3M2
4A6	P24	02	P24	4A6
——	GND	01	P22	4A6,3K1
——	GND	00	P22	4A6,3K1

CONN 3

SHEET LOCATION	ROW 1	TERM. NO.	ROW 2	SHEET LOCATION
3N2	P5	41	GND	——
——	GND	40	GND	——
3A1	P15	39	P22	4A6
N.C.	N15	38	P5S	2B3
——	GND	01	GND	——
N.C.	P5	00	GND	——

CONN 1

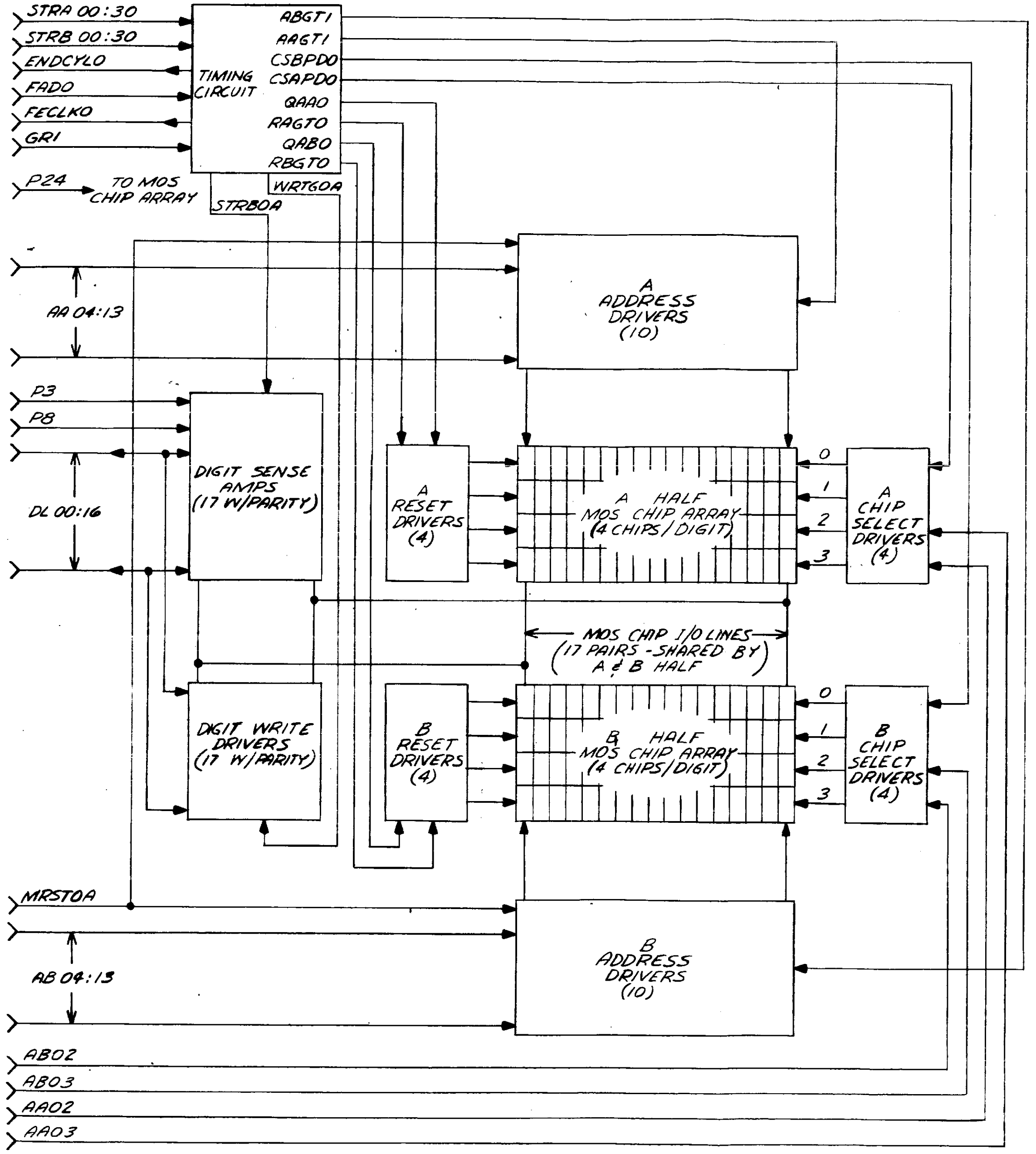
SHEET LOCATION		ROW 2	TERM. NO.	ROW 1	SHEET LOCATION	
M00	M01				M01	M00
——	——	GND	24	GND	——	——
5A2	5A2	AB020	23	AB031	5A2	5A2
9G9	2G9	AB130	22	AB061	2G6	9G6
9G6	2G6	AB070	21	AB051	2G5	9G5
9G5	2G5	AB040	20	AB081	2G7	9G7
9G8	2G8	AB110	19	AB101	2G8	9G8
9G7	2G7	AB090	18	AB121	2G9	9G9
10A6	6A7	STRB20	17	STRB30	6A7	10A6
10A6	6A7	STRB00	16	STRB10	6A7	10A6
4A2	4A2	AA021B	15	AA031B	4A2	4A2
10A5	6A6	STRA00	14	STRA10	6A6	10A5
10A5	6A6	STRA20	13	STRA30	6A6	10A5
9A5	2A5	AA050	12	AA101	2A8	9A8
9A6	2A6	AA070	11	AA041	2A5	9A5
9A6	2A6	AA060	10	AA081	2A7	9A7
9A7	2A7	AA090	09	AA131	2A9	9A9
9A8	2A8	AA110	08	AA121	2A9	9A9
10R6	6R7	ENDCYL0	07	MWRTOA	6J9	10J8
——	——	GND	06	FADO	6A4	10A2
——	——		05	FECLKO	6R7	10R5
——	——		04	P3	3A1	3A1
——	——	GND	03	GR1	6D1	10A1
——	2A4	MRSTOA	02	P22	4A6,3K1	4A6,3K1
4A6,3D1	4A6,3D1	P10	01	P10	4A6,3D1	4A6,3K1
4N4	4N4	P5S	00	P5S	4N4	4N4

CONN 2

SHEET LOCATION	ROW 1	TERM. NO.	ROW 2	SHEET LOCATION
N.C.	P5	41	GND	——
——	GND	40	GND	——
N.C.	P15	39	——	——
N.C.	N15	38	——	——
——	——	04	P5S	2B3
——	——	03	P22	2D4
N.C.	P5	02	P5	N.C.
——	GND	01	GND	——
N.C.	P5	00	GND	——

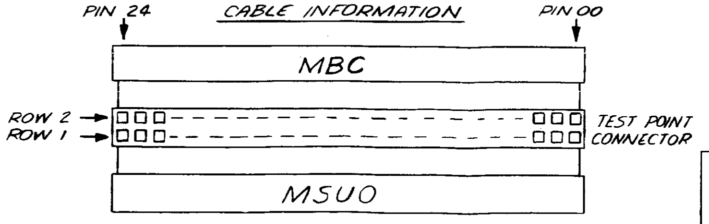
CONN 0

BLOCK DIAGRAM



STRA 00:30
STRB 00:30
ENDCYL0
FADO
FECLKO
GR1
TIMING CIRCUIT
ABGT1
AAGT1
CSBPD0
CSAPD0
QAA0
RAGT0
QAB0
RBGT0
P24
TO MOS CHIP ARRAY
STRB0A
WRTG0A
AA 04:13
A ADDRESS DRIVERS (10)
P3
P8
DL 00:16
DIGIT SENSE AMPS (17 W/PARITY)
A RESET DRIVERS (4)
A HALF MOS CHIP ARRAY (4 CHIPS/DIGIT)
0
1
2
3
A CHIP SELECT DRIVERS (4)
MOS CHIP I/O LINES (17 PAIRS - SHARED BY A & B HALF)
DIGIT WRITE DRIVERS (17 W/PARITY)
B RESET DRIVERS (4)
B HALF MOS CHIP ARRAY (4 CHIPS/DIGIT)
B CHIP SELECT DRIVERS (4)
MRSTOA
AB 04:13
B ADDRESS DRIVERS (10)
AB02
AB03
AA02
AA03

CABLE INFORMATION



PIN 24
PIN 00
MBC
ROW 2
ROW 1
TEST POINT CONNECTOR
MSUO

MBC/MSU CABLE	CABLE PART NO.
LEFT	17-191 FXX
RIGHT	17-212 FXX

F01 - 16KB, F02-32KB, F03-48KB, F04-64KB

35-406	M00	X		X	X	X		X	X	X	X
	M01 & M02	X	X	X	X	X	X	X	X		
SHEET INDEX	REV. LEVEL	11	7	10	7	7	10	2		7	10
	SHEET NO.	1	2	3	4	5	6	7	8	9	10

REVISIONS

CHANGED - SH. 2-6 WERE SH. 1-5
ADDED SHT 1; REVISED SHTS 3 & 6

KL	ECR 3214-06	6-20-72		LP	R02

REDRAWN - DOC # WAS 35-406 D08

PRE PRODUCTION APPROVAL		TEST	DATE
	DEV	LP	
	PROD		

CHANGED - SH. 1, 2, 3 & 6; IN CONN. 2, STRA00, 10, 21 & 31 WERE AA000, 001, 010 & 011 RESP.; STRB00, 10, 21 & 31 WERE AB000, 001, 010 & 011 RESP.

JF	LP	3214-07 3214-08		9-19-72	R03

CHANGED - SH. 1, 4, 5 & 6; CONN 2 MNEMONICS FOR COMPATABILITY WITH MBC BD - AA020A, AA030A, AB021 & AB031 WERE AA020, AA030, AB020 & AB030 RESPECTIVELY

7	LP	ECR 3214-15		9-25-72	R04

CHANGED - SH. 1 & 6. REMOVED FROM CONN 2 - STRTA1 @ 103-2 & STRTB1 @ 104-2. ADDED - MRSTO @ 103-2

7	LP.	3214-18		10-30-72	R05

CHANGED SH. 1, 2, 4, 5, 6; SHT. LOC. CORRECTED FOR P5 & P15 ON CONN. 3; CONN 2 MNEMONICS FOR COMPATABILITY WITH MBC BD - 215-2 WAS AA020A, 115-2 WAS AA030A; 208-2 THRU 212-2 & 218-2 THRU 223-2 - ALL MNEm WERE AXXX1 (MBC PER 3214-24)

7	LP	3214-21 & 22		12-4-72	R06

REVISED SHEETS 1 & 6

7	LP.	3214-25		12-21-72	R07

REVISED SHEETS 1, 3 & 6; CHANGED - 103-2 WAS MRSTO; DELETED - 202-2 WAS GND; ADDED - 104-2 → P3.

7	LP.	3214-26		1-11-73	R08

ADDED BLOCK DIAGRAM & CABLE INFO. REVISED CONN 2 SHT LOCATIONS. REVISED SHTS 2, 6, 9, 10.

WZ	EBC	3214-34		4-19-73	R09

REVISED SHTS 3, 6, 7 & 10

Hm	EBC	3214-42		7-16-73	R10

RELEASED FOR PRODUCTION
MFG. ENG. L. Pezzi DATE 8-8-73

REVISED SHTS 1, 3, 4, 5 & 7
LOC. H9 M02 WAS NOT SPECIF

BG	JEA	1964		11/16/73	R11

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION:

35-406	R12	35-406 M01	R02
35-406 F01	R11	35-406 F01 M01	R02
		35-406 M02	R01
		35-406 F01 M02	R01

THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

NOTES

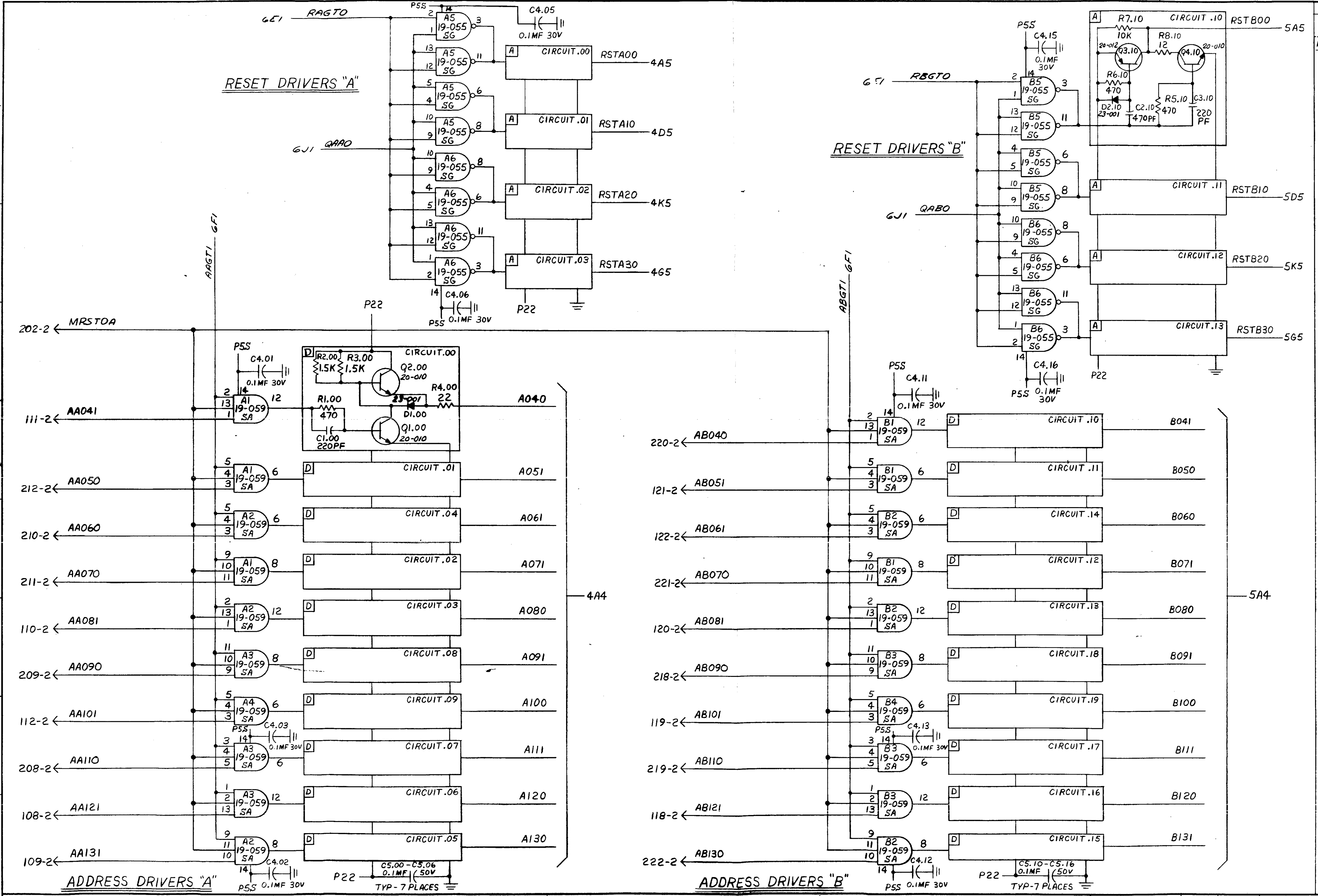
NAME	TITLE	DATE
K. LAFFERTY	DRAFT	6-14-72
F. FLEMING	CHK	1-23-73
L. PEZZI	ENGR	8-3-73
N. MASSI	TEST	8-8-73
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 80 MSU

TASK NO. 03214
DWG NO. 02-247 R11 D08
SHEET 1 OF 10

BRUNING 44-231 16042

INTERDATA®



RESET DRIVERS "A"
GE1 RAGTO
GJ1 QAAO
P5S
C4.05 0.1MF 30V
A5 19-055 SG
A6 19-055 SG
CIRCUIT.00 RSTA00 4A5
CIRCUIT.01 RSTA10 4D5
CIRCUIT.02 RSTA20 4K5
CIRCUIT.03 RSTA30 4G5
C4.06 0.1MF 30V
P22
RESET DRIVERS "B"
GE1 RBGTO
GJ1 QABO
C4.15 0.1MF 30V
B5 19-055 SG
B6 19-055 SG
CIRCUIT.10 RSTB00 5A5
R7.10 10K
R8.10 12
Q3.10 20-012
Q4.10 20-010
R6.10 470
D2.10 23-001
C2.10 470PF
R5.10 470
C3.10 220 PF
CIRCUIT.11 RSTB10 5D5
CIRCUIT.12 RSTB20 5K5
CIRCUIT.13 RSTB30 5G5
C4.16 0.1MF 30V
AAGT1 GF1
ABGT1 GF1
202-2 MRSTOA
C4.01 0.1MF 30V
R2.00 1.5K
R3.00 1.5K
Q2.00 20-010
R1.00 470
C1.00 220PF
R4.00 22
D1.00 23-001
Q1.00 20-010
111-2 AA041 A1 19-059 SA CIRCUIT.00 A040
212-2 AA050 A1 19-059 SA CIRCUIT.01 A051
210-2 AA060 A2 19-059 SA CIRCUIT.04 A061
211-2 AA070 A1 19-059 SA CIRCUIT.02 A071
110-2 AA081 A2 19-059 SA CIRCUIT.03 A080
209-2 AA090 A3 19-059 SA CIRCUIT.08 A091
112-2 AA101 A4 19-059 SA CIRCUIT.09 A100
208-2 AA110 A3 19-059 SA CIRCUIT.07 A111
108-2 AA121 A3 19-059 SA CIRCUIT.06 A120
109-2 AA131 A2 19-059 SA CIRCUIT.05 A130
4A4
C4.03 0.1MF 30V
C4.02 0.1MF 30V
C5.00-C5.06 0.1MF 50V
TYP-7 PLACES
ADDRESS DRIVERS "A"
C4.11 0.1MF 30V
220-2 AB040 B1 19-059 SA CIRCUIT.10 B041
121-2 AB051 B1 19-059 SA CIRCUIT.11 B050
122-2 AB061 B2 19-059 SA CIRCUIT.14 B060
221-2 AB070 B1 19-059 SA CIRCUIT.12 B071
120-2 AB081 B2 19-059 SA CIRCUIT.13 B080
218-2 AB090 B3 19-059 SA CIRCUIT.18 B091
119-2 AB101 B4 19-059 SA CIRCUIT.19 B100
219-2 AB110 B3 19-059 SA CIRCUIT.17 B111
118-2 AB121 B3 19-059 SA CIRCUIT.16 B120
222-2 AB130 B2 19-059 SA CIRCUIT.15 B131
5A4
C4.13 0.1MF 30V
C4.12 0.1MF 30V
C5.10-C5.16 0.1MF 50V
TYP-7 PLACES
ADDRESS DRIVERS "B"

REVISIONS					
REVISED THIS SHEET TO REFLECT 35-406M01					
WZ	[illegible]	3214-34		4-19-73	R07

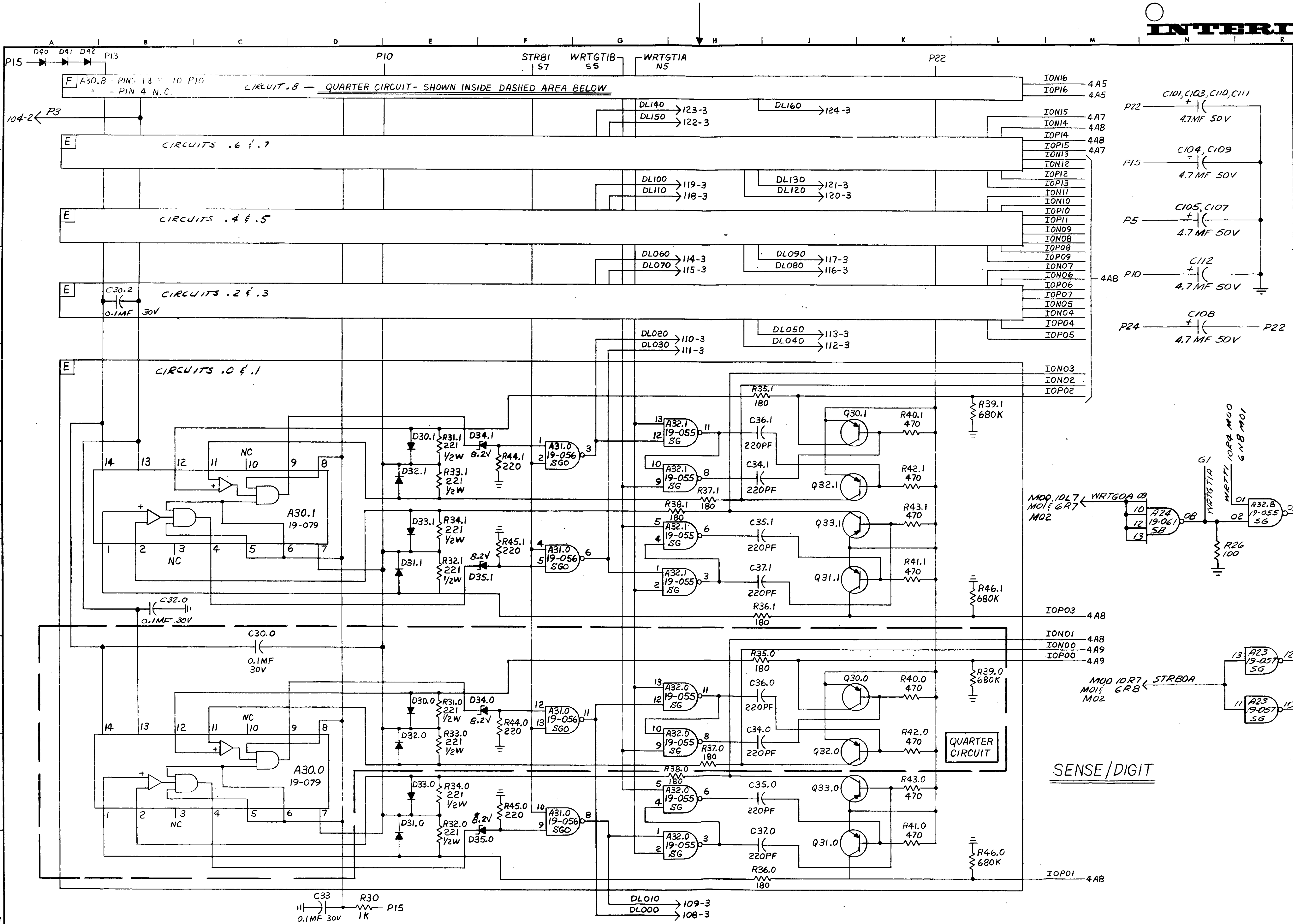
NOTES

NAME	TITLE	DATE
K. LAFFERTY	DRAFT	5-2-72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 80 MSU

TASK NO. 03214
DWG NO. 02-247 R07 D08
SHEET 2 - OF

BRUNING 44 231 15043


INTERDATA
D40 D41 D42 P13
P15
P10
STRB1 S7
WRTGTIB S5
WRTGTIA N5
P22
F A30.8 - PINS 14 & 10 P10
" - PIN 4 N.C.
CIRCUIT .8 — QUARTER CIRCUIT - SHOWN INSIDE DASHED AREA BELOW
104-2 P3
E CIRCUITS .6 & .7
E CIRCUITS .4 & .5
E CIRCUITS .2 & .3
C30.2 0.1MF 30V
E CIRCUITS .0 & .1
DL140 123-3
DL150 122-3
DL160 124-3
DL100 119-3
DL110 118-3
DL130 121-3
DL120 120-3
DL060 114-3
DL070 115-3
DL090 117-3
DL080 116-3
DL020 110-3
DL030 111-3
DL050 113-3
DL040 112-3
ION16 4A5
IOP16 4A5
ION15 4A7
ION14 4A8
IOP14 4A8
IOP15 4A7
ION13
ION12
IOP12
IOP13
ION11
ION10
IOP10
IOP11
ION09
ION08
IOP08
IOP09
ION07
ION06 4A8
IOP06
IOP07
ION05
ION04
IOP04
IOP05
ION03
ION02
IOP02
IOP03 4A8
ION01 4A8
ION00 4A9
IOP00 4A9
IOP01 4A8
C101, C103, C110, C111 4.7MF 50V P22
C104, C109 4.7MF 50V P15
C105, C107 4.7MF 50V P5
C112 4.7MF 50V P10
C108 4.7MF 50V P24 P22
A30.1 19-079
A30.0 19-079
D30.1 D32.1 D33.1 D31.1
R31.1 221 1/2W
R33.1 221 1/2W
R34.1 221 1/2W
R32.1 221 1/2W
D34.1 8.2V
D35.1 8.2V
R44.1 220
R45.1 220
A31.0 19-056 SGO
A32.1 19-055 SG
C36.1 220PF
C34.1 220PF
C35.1 220PF
C37.1 220PF
R35.1 180
R37.1 180
R38.1 180
R36.1 180
Q30.1 Q32.1 Q33.1 Q31.1
R40.1 470
R42.1 470
R43.1 470
R41.1 470
R39.1 680K
R46.1 680K
C32.0 0.1MF 30V
C30.0 0.1MF 30V
D30.0 D32.0 D33.0 D31.0
R31.0 221 1/2W
R33.0 221 1/2W
R34.0 221 1/2W
R32.0 221 1/2W
D34.0 8.2V
D35.0 8.2V
R44.0 220
R45.0 220
A32.0 19-055 SG
C36.0 220PF
C34.0 220PF
C35.0 220PF
C37.0 220PF
R35.0 180
R37.0 180
R38.0 180
R36.0 180
Q30.0 Q32.0 Q33.0 Q31.0
R40.0 470
R42.0 470
R43.0 470
R41.0 470
R39.0 680K
R46.0 680K
QUARTER CIRCUIT
NC
C33 0.1MF 30V
R30 1K P15
DL010 109-3
DL000 108-3
M00, 10L7, M01 & 6R7, M02 WRTGOA 09
A24 19-061 SB 08
R26 100
G1 WRTGTIA
WRTT1 10P4 M00 6N8 M01
A32.8 19-055 SG 03
A24 19-061 SB 06
G1 WRTGTIB
R25 100
M00 10R7, M01 & 6R8, M02 STRB0A
A23 19-057 SG
STRB1 F1
R22 100
SENSE/DIGIT

REVISIONS					
ADDED-D40 THRU D46; R31 THRU R34 WERE 340Ω.					
KL	ECR 3214-06			7-17-72	R02
DELETED-C100, C102, C106 & C113 WERE 4.7MF DECOUPLERS BETWEEN P5S & GND.					
JF		3214-07		9-19-72	R03
REMOVED - C32.8 DELETED FROM CIRCUIT .8					
7		3214-22		12-4-72	R06
REMOVED - C32.0 FRM CKT .0 & .1; AT LOC A1, P3 WAS TO DIODES IN SERIES 23-017: D43 D44 D45 D46					
7		3214-26		1-11-73	R08
AREA R5, A32.8 WAS A23, 19-057. "WRTT1" WAS NOT SPEC.					
		3214-42		7-16-73	R09
LOC'S L5 & M7 M02 WAS NOT SPECIFIED					
B		1964		11/1/73	R10

NOTES 1. UNLESS OTHERWISE SPECIFIED, ALL DIODES ARE 23-001 & ALL TRANSISTORS ARE 20-012.

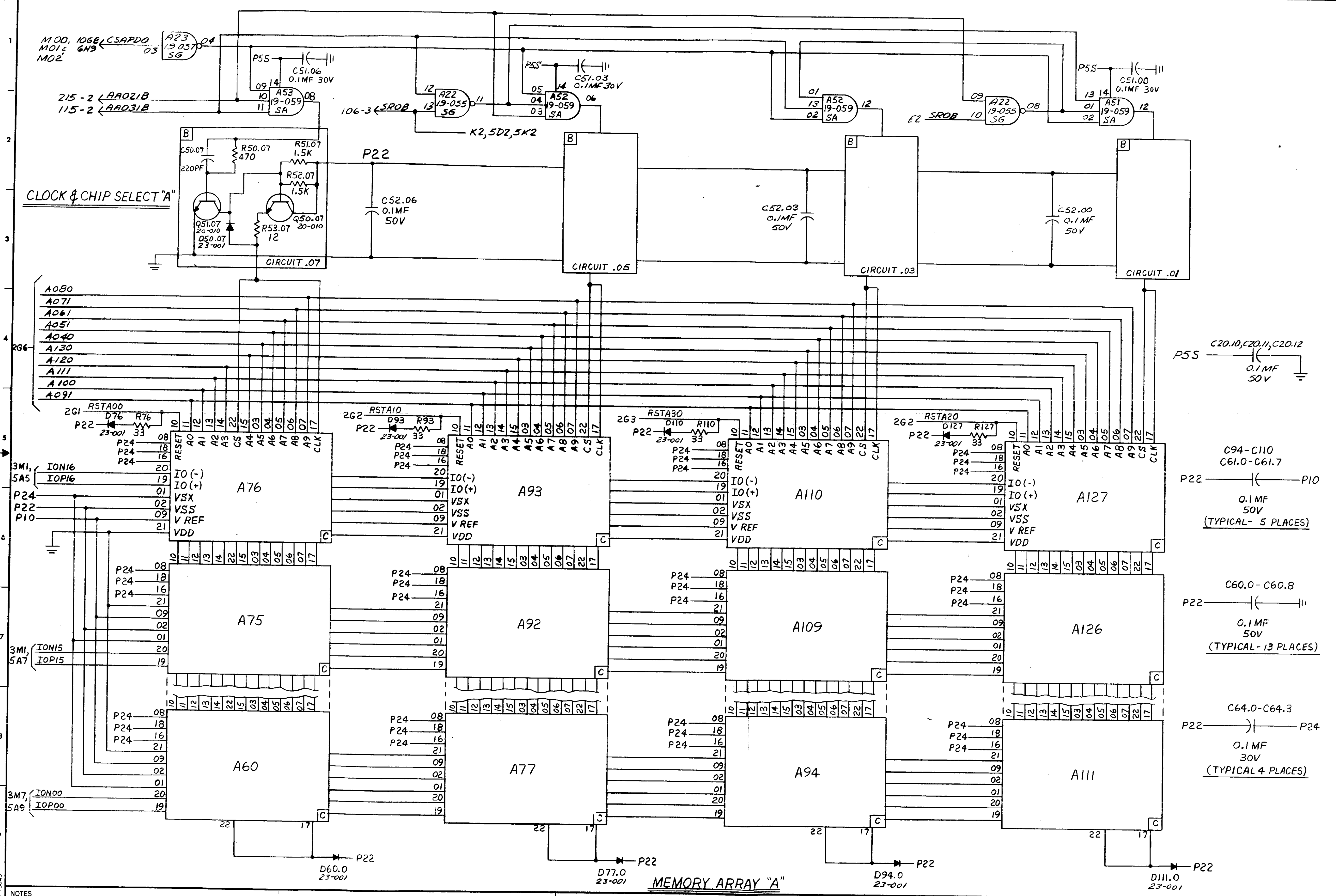
NAME	TITLE	DATE
K. LAFFERTY	DRAFT	5-15-72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 80 MSU

TASK NO. 03214
DWG NO. 02-247 R10 D08
SHEET OF 3-10

BRUNING 44-231 15043

INTERDATA®



M00, 10G8 CSAPD0
M01 & 6H9
M02
A23 19-057 SG
215-2 AA021B
115-2 AA031B
A53 19-059 SA
P5S
C51.06 0.1MF 30V
106-3 SROB
A22 19-055 SG
K2, 5D2, 5K2
A52 19-059 SA
C51.03 0.1MF 30V
E2 SROB
A22 19-055 SG
A51 19-059 SA
C51.00 0.1MF 30V
C50.07 220PF
R50.07 470
R51.07 1.5K
R52.07 1.5K
Q51.07 20-010
Q50.07 20-010
D50.07 23-001
R53.07 12
CLOCK & CHIP SELECT "A"
CIRCUIT .07
P22
C52.06 0.1MF 50V
CIRCUIT .05
C52.03 0.1MF 50V
CIRCUIT .03
C52.00 0.1MF 50V
CIRCUIT .01
2G6
A080
A071
A061
A051
A040
A130
A120
A111
A100
A091
2G1 RSTA00
D76 23-001
R76 33
2G2 RSTA10
D93 23-001
R93 33
2G3 RSTA30
D110 23-001
R110 33
2G2 RSTA20
D127 23-001
R127 33
RESET A0 A1 A2 A3 CS A4 A5 A6 A7 A8 A9 CLK
IO(-) IO(+) VSX VSS V REF VDD
3M1, 5A5 ION16 IOP16
3M1, 5A7 ION15 IOP15
3M7, 5A9 ION00 IOP00
P24
P22
P10
A76
A93
A110
A127
A75
A92
A109
A126
A60
A77
A94
A111
D60.0 23-001
D77.0 23-001
D94.0 23-001
D111.0 23-001
MEMORY ARRAY "A"
P5S C20.10, C20.11, C20.12 0.1MF 50V
C94-C110
C61.0-C61.7
P22 P10
0.1MF 50V
(TYPICAL- 5 PLACES)
C60.0-C60.8
P22
0.1MF 50V
(TYPICAL- 13 PLACES)
C64.0-C64.3
P22 P24
0.1MF 30V
(TYPICAL 4 PLACES)

REVISIONS					
CHANGED AT LOC B1: AA020A & AA030A WERE AA020 & AA030 RESPECTIVELY					
7		ECR 32H-15		9-25-72	R04
REMOVED - B CIRCUITS .06, .04, .02 & .00 & RELATED INPUT GATES A53-06, A52-08, A51-06 & A51-08; A76-17, A93-17, A110-17 & A127-17 WERE TO CKT .06, .04, .02, .00 OUTPUTS RESP; AT LOC C9, F9, J9 & M9, A60-22 & -17, A77-22 & -17, A94-22 & -17, A111-22 & -17, EACH HAD 33Ω RESISTOR IN SERIES TO RELATED DIODE ANODE; AT LOC A4, A051, A061, A071, A091 & A111 WERE AXX0 (SEE SH. 2).					
7		32H-21		12-4-72	R06
LOC A1 M02 WAS NOT SPECIFIED					
G	JEH	1964		11/1-73	R07

NOTES

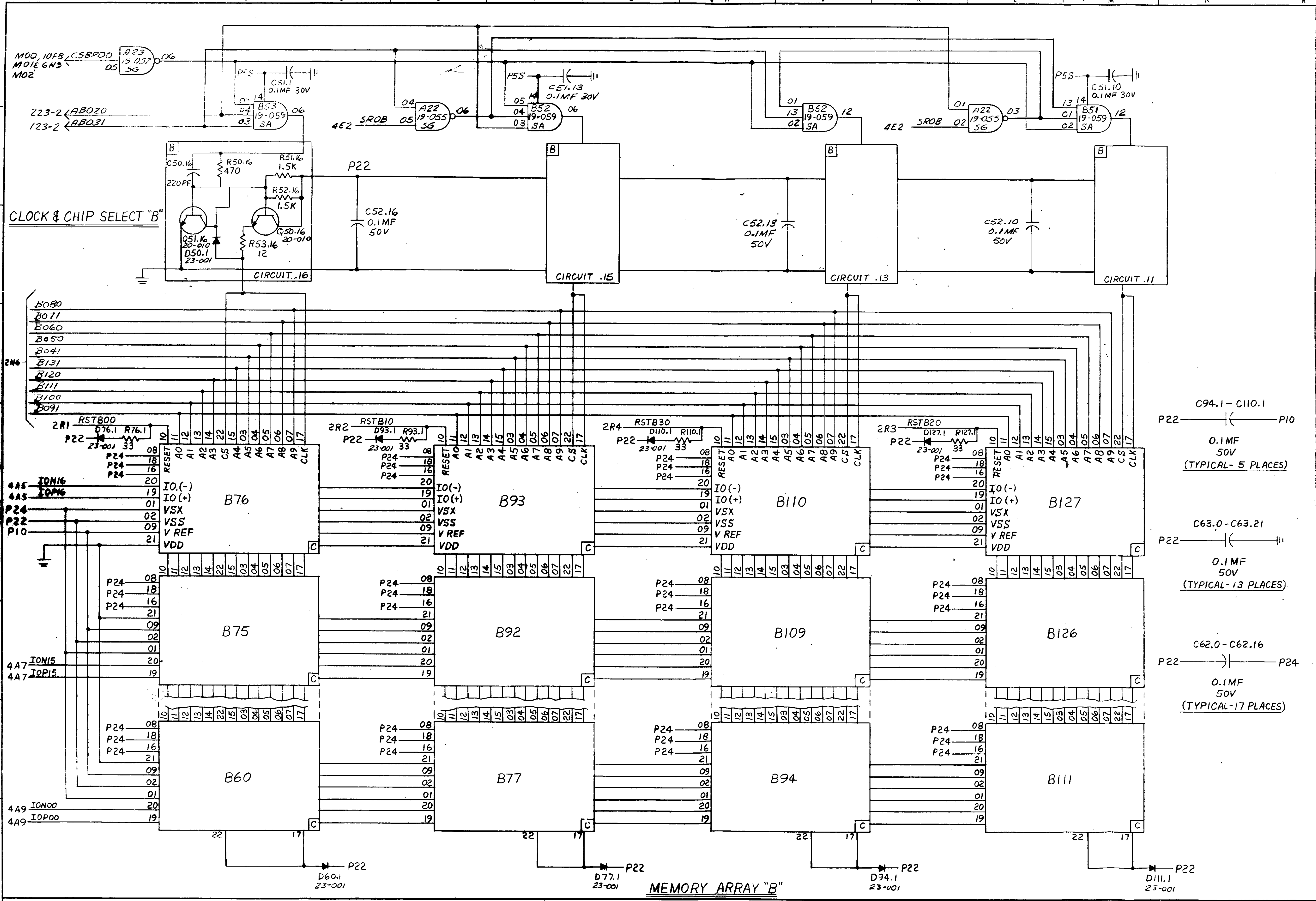
NAME	TITLE	DATE
K. LAFFERTY	DRAFT	5-5-72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 80 MSU

TASK NO. 03214
DWG NO. 02-247 R07 D08
SHEET 4 OF 10

BRUNING 44-231 15043

INTERDATA®


CLOCK & CHIP SELECT "B"
MOO, 10FB
MO1E 6HS
MO2
CSBPDO
A23 19-057 SG
223-2 AB020
123-2 AB031
B53 19-059 SA
C51.1 0.1MF 30V
P5S
4E2 SROB
A22 19-055 SG
B52 19-059 SA
C51.13 0.1MF 30V
B51 19-059 SA
C51.10 0.1MF 30V
C50.16 220PF
R50.16 470
R51.16 1.5K
R52.16 1.5K
Q51.16 20-010
Q50.16 20-010
D50.1 23-001
R53.16 12
CIRCUIT .16
P22
C52.16 0.1MF 50V
CIRCUIT .15
C52.13 0.1MF 50V
CIRCUIT .13
C52.10 0.1MF 50V
CIRCUIT .11
2N6
B080
B071
B060
B050
B041
B131
B120
B111
B100
B091
2R1 RSTB00 D76.1 R76.1 33 23-001
2R2 RSTB10 D93.1 R93.1 33 23-001
2R4 RSTB30 D110.1 R110.1 33 23-001
2R3 RSTB20 D127.1 R127.1 33 23-001
RESET A0 A1 A2 A3 CS A4 A5 A6 A7 A8 A9 CLK
IO(-) IO(+) VSX VSS V REF VDD
4A5 ION16
4A5 IOP16
P24
P22
P10
B76
B93
B110
B127
B75
B92
B109
B126
4A7 ION15
4A7 IOP15
B60
B77
B94
B111
4A9 IONOO
4A9 IOPOO
D60.1 23-001
D77.1 23-001
D94.1 23-001
D111.1 23-001
C94.1 – C110.1
P22 P10
0.1MF 50V (TYPICAL- 5 PLACES)
C63.0 - C63.21
0.1MF 50V (TYPICAL- 13 PLACES)
C62.0 - C62.16
P22 P24
0.1MF 50V (TYPICAL-17 PLACES)

MEMORY ARRAY "B"

REVISIONS					
CHANGED AT LOC B1: AB020, 031, 021 & 030 WERE AB021, 030, 020 & 031 RESPECTIVELY.					
X	LP	ECR 3214-15		9-25-72	R04
REMOVED – B CIRCUITS .17, .14, .12 & .10 & RELATED INPUT GATES B53-08 B52-08, B51-08 & B51-06; B76-17, B93-17, B110-17 & B127-17 WERE TO CKT. 17, .14, .12 & .10 RESP.; AT LOC C9, F9, J9 & M9, B60-22 & -17, B77-22 & -17, B94-22 & -17, B111-22 & -17, EACH HAD 33Ω RESISTOR IN SERIES TO RELATED DIODE ANODE; AT LOC A4, B041, B071, B091, B111 & B131 WERE BXX0 (SEE SH. 2)					
X	LP.	3214-21		12-4-72	R06
LOC. A1 M02 WAS NOT SPECIFIED					
BG	JCH	1964	V/L	11/16/73	R07

NOTES

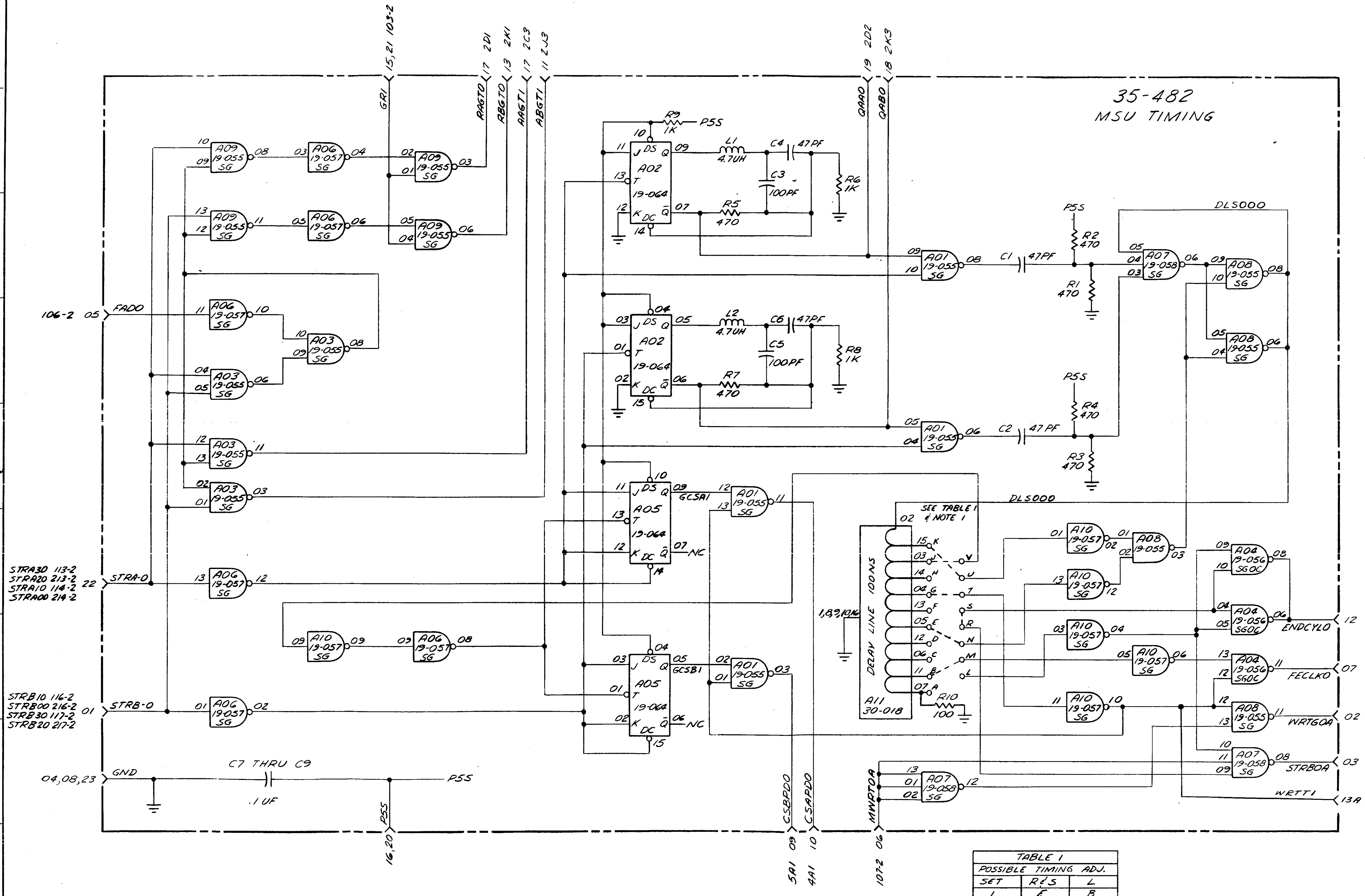
NAME	TITLE	DATE
K. LAFFERTY	DRAFT	5-5-72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 80 MSU

TASK NO. 03214
DWG NO 02-247 R07 D08
SHEET OF 5 -10

INTERDATA®

REVISIONS					
REVISED THIS SHEET TO REFLECT 35-406 M01					
WZ		3214-34		4-19-73	R09
ADDED TERM 13A, AREA R8					
HM		3214-42		7-16-73	R10



35-482
MSU TIMING
GR1 15,21 103-2
RAGT0 17 2D1
RBGT0 13 2K1
RAGT1 17 2C3
RBGT1 11 2J3
QAA0 19 2D2
QAB0 18 2K3
106-2 05 FAD0
STRA30 113-2
STRA20 213-2
STRA10 114-2
STRA00 214-2
22 STRA-0
STRB10 116-2
STRB00 216-2
STRB30 117-2
STRB20 217-2
01 STRB-0
04,08,23 GND
C7 THRU C9
.1 UF
P5S
16,20
A09 19-055 SG
A06 19-057 SG
A03 19-055 SG
A10 19-057 SG
A02 19-064
A05 19-064
A01 19-055 SG
A07 19-058 SG
A08 19-055 SG
A04 19-056 SG0C
DS J T K DC Q Q̄
R9 1K P5S
L1 4.7UH
C4 47PF
C3 100PF
R6 1K
R5 470
L2 4.7UH
C6 47PF
C5 100PF
R8 1K
R7 470
C1 47PF
R2 470
R1 470
C2 47PF
R4 470
R3 470
DLS000
GCSA1
GCSB1
NC
SEE TABLE 1 & NOTE 1
DELAY LINE 100NS
A11 30-018
1,8,9,10,16
15 K
03 J
14 H
04 G
13 F
05 E
12 D
06 C
11 B
07 A
V U T S R N M L
R10 100
CSBP00 09 5A1
CSAP00 10 4A1
MWRT0A 06 107-2
ENDCYL0 12 207-2
FECLK0 07 105-2
WRTG0A 02 3M5
STRB0A 03 3M7
WRTT1 13A 3N5

TABLE 1		
POSSIBLE TIMING ADJ.		
SET	R & S	L
1	E	B
2	D	A

NOTES 1. FIXED STRAPPING IS AS SHOWN - ADDITIONAL STRAPPING IS REQUIRED AND DETERMINED AT FACTORY. FACTORY WILL EQUIP SET 1 OR SET 2 STRAPPING SHOWN BY TABLE 1.

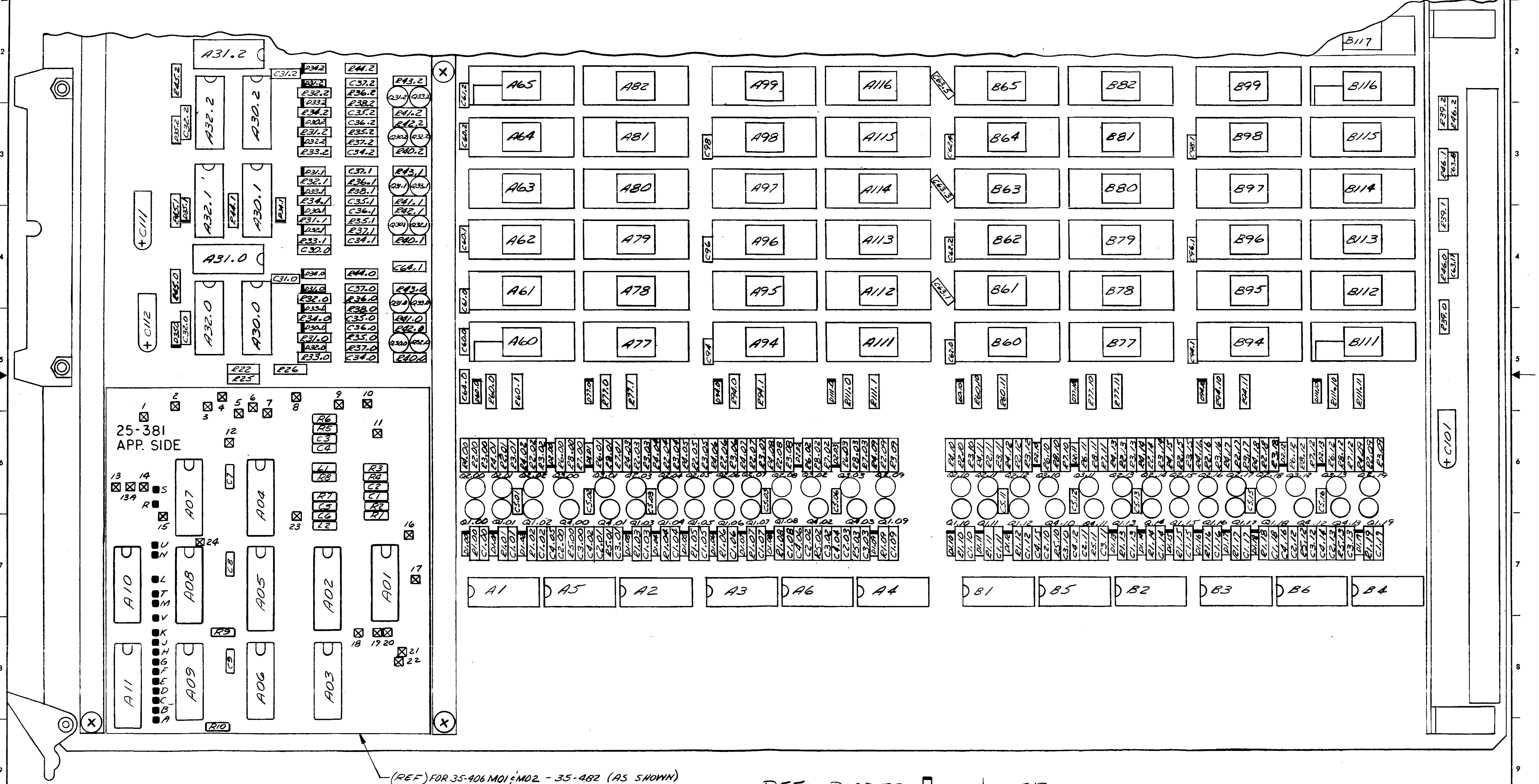
BRUNING 44-231 16042

NAME	TITLE	DATE
W. ZILLGER	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 80 MSU
TASK NO. 03214
DWG NO. 02-247 R10 D08
SHEET OF 6-10

INTERDATA®

REVISIONS					
ADDED PIN LOCATIONS ON TIMING BOARD.					
MM		3214-42		7-16-73	R01
LOC. F9 M02 WAS NOT SPECIFIED					
BG		1964		11/1/73	R02


A31.2
A32.2
A30.2
A32.1
A30.1
A31.0
A32.0
A30.0
C31.2
C31.0
C111
C112
A65
A82
A99
A116
B65
B82
B99
B116
A64
A81
A98
A115
B64
B81
B98
B115
A63
A80
A97
A114
B63
B80
B97
B114
A62
A79
A96
A113
B62
B79
B96
B113
A61
A78
A95
A112
B61
B78
B95
B112
A60
A77
A94
A111
B60
B77
B94
B111
B117
C101
R22
R25
R26
25-381
APP. SIDE
A07
A04
A10
A08
A05
A02
A01
A11
A09
A06
A03
R9
R10
A1
A5
A2
A3
A6
A4
B1
B5
B2
B3
B6
B4

(REF) FOR 35-406 M01 & M02 - 35-482 (AS SHOWN)
FOR 35-406 - 35-432 (SEE SHT 10)

REF: DIODES ▯ = ▲ TYP

NOTES

NAME	TITLE	DATE
R MEGINLEY (KL)	DRAFT	9-18-72
J. F. FLEMING	CHK	9-18-72
	ENGR	
	DIR ENG	

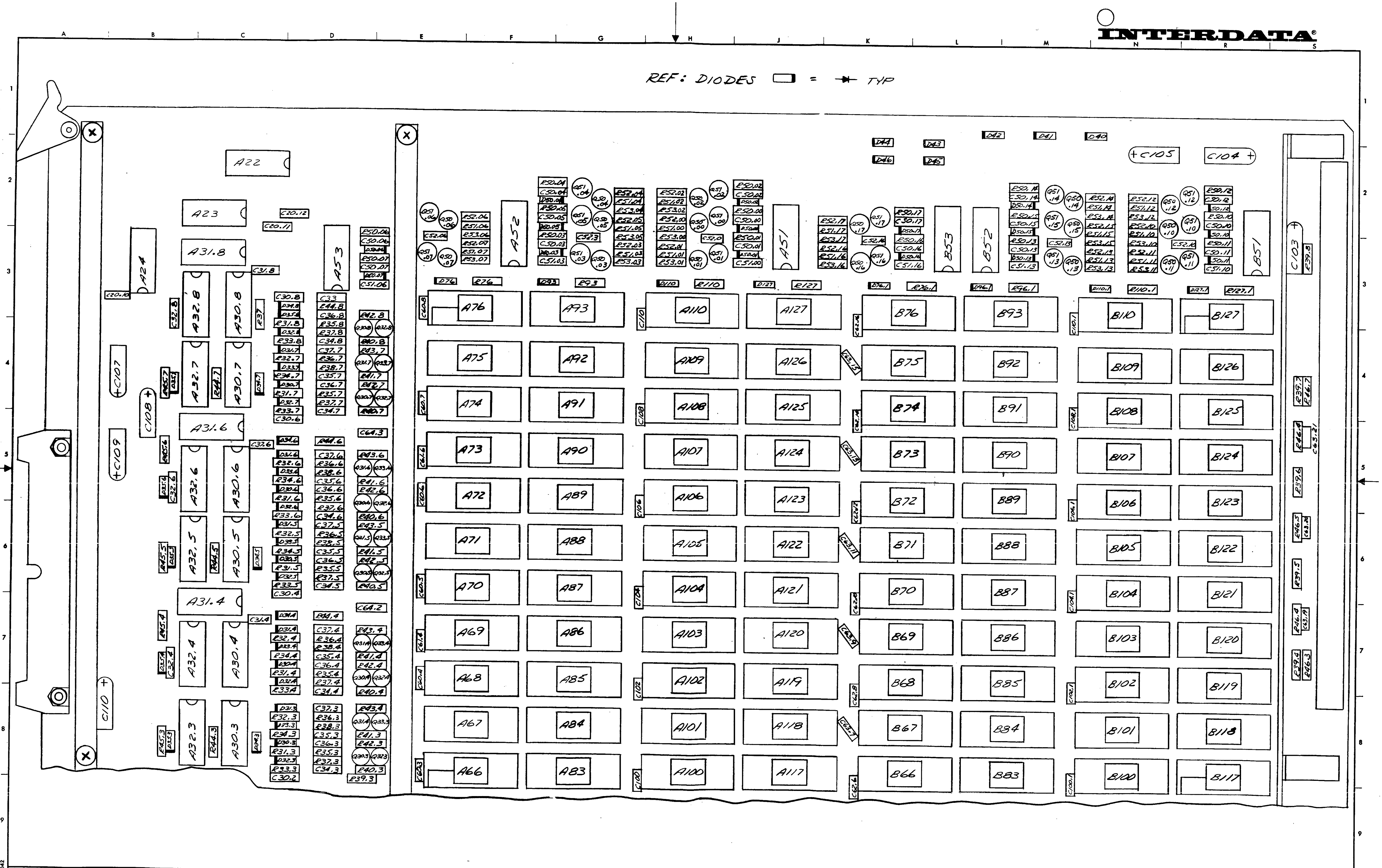
TITLE MODEL 80 MSU COMPONENT LOCATOR

TASK NO. 03214

DWG NO. 02-247 R02 D08

SHEET 7 OF 10

INTERDATA®


REF: DIODES ▭ = ⊳| TYP
A22
A23
A31.8
A24
A32.8
A30.8
A32.7
A30.7
A31.6
A32.6
A30.6
A32.5
A30.5
A31.4
A32.4
A30.4
A32.3
A30.3
A53
A52
A51
B53
B52
B51
C103
+C105
C104+
C107
C108+
+C109
C110+
D40
D41
D42
D43
D44
D45
D46
A76
A75
A74
A73
A72
A71
A70
A69
A68
A67
A66
A93
A92
A91
A90
A89
A88
A87
A86
A85
A84
A83
A110
A109
A108
A107
A106
A105
A104
A103
A102
A101
A100
A127
A126
A125
A124
A123
A122
A121
A120
A119
A118
A117
B76
B75
B74
B73
B72
B71
B70
B69
B68
B67
B66
B93
B92
B91
B90
B89
B88
B87
B86
B85
B84
B83
B110
B109
B108
B107
B106
B105
B104
B103
B102
B101
B100
B127
B126
B125
B124
B123
B122
B121
B120
B119
B118
B117
A
B
C
D
E
F
G
H
J
K
L
M
N
R
S
1
2
3
4
5
6
7
8
9

NOTES

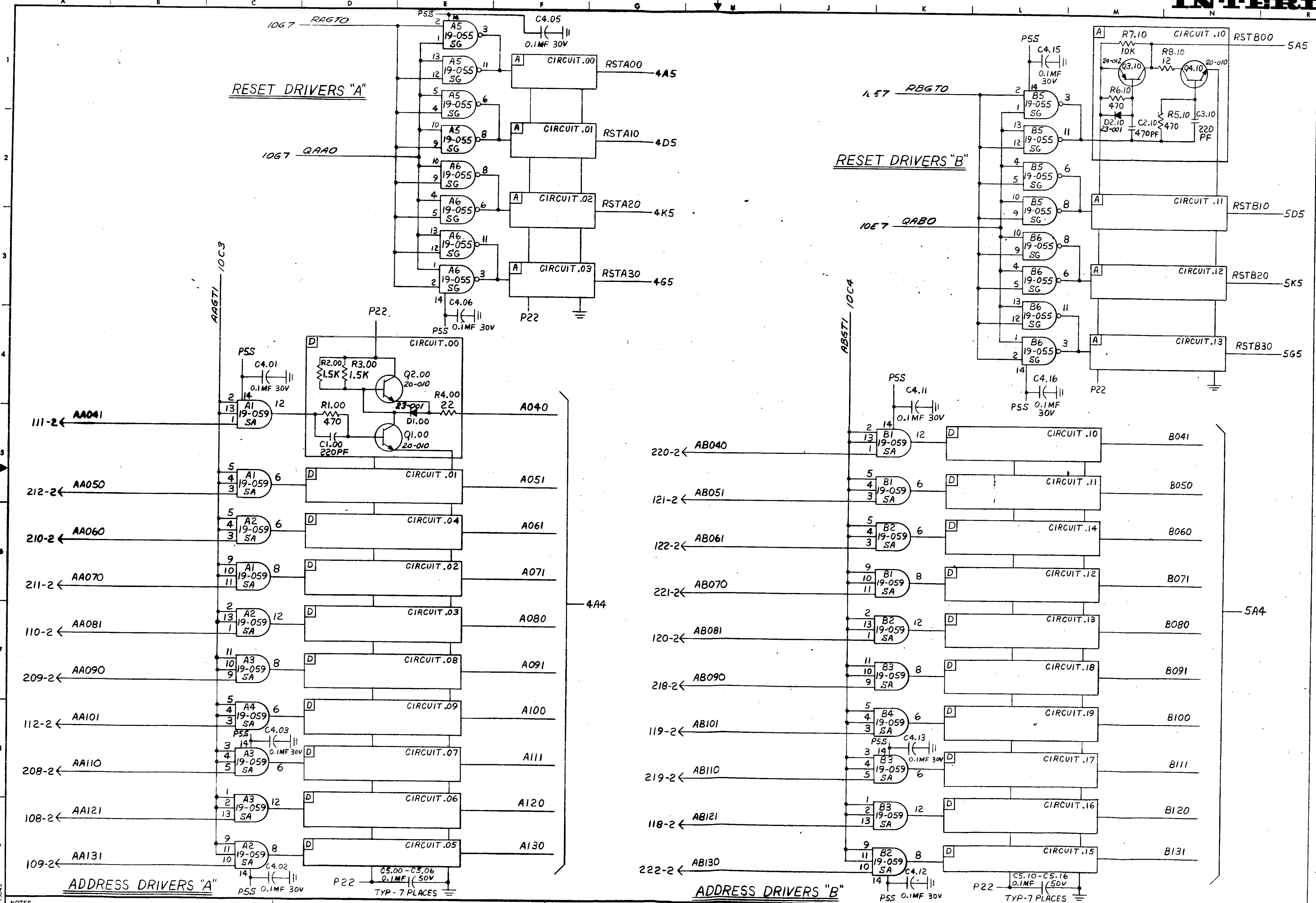
NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE
MODEL 80 MSU
COMPONENT
LOCATOR

TASK NO. 03214
DWG NO. 02-247 D08
SHEET OF 8-10

BRUNING 44-231 16042

INTERDATA



RESET DRIVERS "A"
RESET DRIVERS "B"
ADDRESS DRIVERS "A"
ADDRESS DRIVERS "B"
10G7 RAGTO
10G7 QAAO
1E7 RBGTO
10E7 QABO
A5 19-055 SG
A6 19-055 SG
B5 19-055 SG
B6 19-055 SG
CIRCUIT .00
CIRCUIT .01
CIRCUIT .02
CIRCUIT .03
CIRCUIT .10
CIRCUIT .11
CIRCUIT .12
CIRCUIT .13
RSTA00 4A5
RSTA10 4D5
RSTA20 4K5
RSTA30 4G5
RSTB00 5A5
RSTB10 5D5
RSTB20 5K5
RSTB30 5G5
C4.05 0.1MF 30V
C4.06 0.1MF 30V
C4.15 0.1MF 30V
C4.16 0.1MF 30V
P5S
P22
R7.10 10K
R8.10 12
Q3.10 20-012
Q4.10 20-010
R6.10 470
D2.10 23-001
C2.10 470PF
R5.10 470
C3.10 220 PF
AAGT1 10C3
ABGT1 10C4
C4.01 0.1MF 30V
C4.11 0.1MF 30V
A1 19-059 SA
A2 19-059 SA
A3 19-059 SA
A4 19-059 SA
B1 19-059 SA
B2 19-059 SA
B3 19-059 SA
B4 19-059 SA
R2.00 1.5K
R3.00 1.5K
Q2.00 20-010
R1.00 470
R4.00 22
23-001 D1.00
C1.00 220PF
Q1.00 20-010
111-2 AA041
212-2 AA050
210-2 AA060
211-2 AA070
110-2 AA081
209-2 AA090
112-2 AA101
208-2 AA110
108-2 AA121
109-2 AA131
A040
A051
A061
A071
A080
A091
A100
A111
A120
A130
CIRCUIT .04
CIRCUIT .08
CIRCUIT .09
CIRCUIT .07
CIRCUIT .06
CIRCUIT .05
4A4
C4.03 0.1MF 30V
C4.02 0.1MF 30V
C5.00 - C5.06 0.1MF 50V
TYP - 7 PLACES
220-2 AB040
121-2 AB051
122-2 AB061
221-2 AB070
120-2 AB081
218-2 AB090
119-2 AB101
219-2 AB110
118-2 AB121
222-2 AB130
B041
B050
B060
B071
B080
B091
B100
B111
B120
B131
CIRCUIT .14
CIRCUIT .18
CIRCUIT .19
CIRCUIT .17
CIRCUIT .16
CIRCUIT .15
5A4
C4.13 0.1MF 30V
C4.12 0.1MF 30V
C5.10 - C5.16 0.1MF 50V
TYP - 7 PLACES

REVISIONS

REMOVED: B4-08 WAS TO B3-11 ETC, B4-12 WAS TO B1-2 ETC, A4-08 WAS TO A3-11 ETC, A4-12 WAS TO A1-2 ETC, ASSOC ADDRESS INPUT OPTIONS; STRTA1 (103-2) WAS TO A4-11 & 13, STRTB1 (104-2) WAS TO B4-11 & 13.

CHANGED: MNEMONICS - RBGTO WAS RBGHTO, RAGTO WAS RAGHTO, AAGT1 WAS AAGHT1A, ABGT1 WAS AAGHT1A; C2.00 - .03 & C2.10 - .13 WERE 220PF.

ADDED: CONN FROM A2-13 TO A3-11 & FROM B2-13 TO B3-11

3	LP	ECR 3214-07		9-19-72	R03

CHANGED - AT LOC A5-A9, MNEMONICS AA050, 060, 070, 090 & 110 WERE AAXX1, & RELATED OUTPUTS WERE AXX0; AT LOC H5-H9, MNEM AB040, 070, 090, 110 & 130 WERE ABXX1, & RELATED OUTPUTS WERE BXX0

4	LP	3214-21 & 22		12-4-72	R06

THIS WAS SHEET 2.

WZ	EBL	3214 - 34		4-16-73	R07

NOTES

NAME	TITLE	DATE
K. LAFFERTY	DRAFT	5-2-72
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MODEL 80 MSU

TASK NO. 03214
DWG NO. 02-247 R07 D08
SHEET 9 OF 10

BRUNING 44 231 15043

INTERDATA®

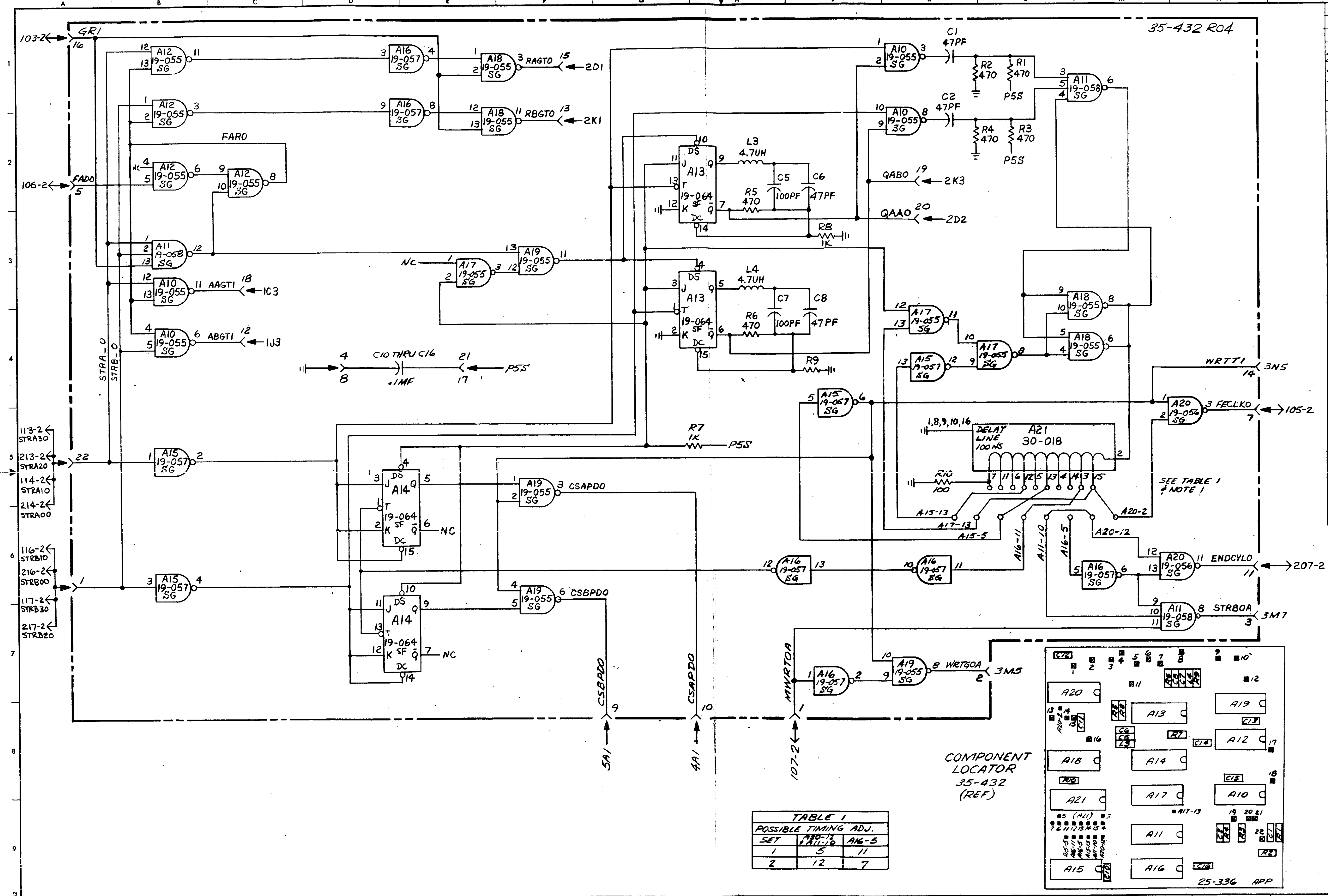

35-432 R04
103-2 GR1 16
A12 19-055 SG
A16 19-057 SG
A18 19-055 SG RAGTO 15 2D1
RBGTO 13 2K1
FARO
106-2 FADO 5
A11 19-058 SG
A10 19-055 SG AAGT1 18 1C3
ABGT1 12 1J3
STRA_0
STRB_0
NC
A17 19-055 SG
A19 19-055 SG
A13 19-064 SF DS J T K Q DC
L3 4.7UH
C5 100PF
C6 47PF
R5 470
R8 1K
L4 4.7UH
C7 100PF
C8 47PF
R6 470
R9
C1 47PF
C2 47PF
R1 470
R2 470
R3 470
R4 470
P5S
A11 19-058 SG
QABO 19 2K3
QAAO 20 2D2
4 8 C10 THRU C16 .1MF 21 17 P5S
R7 1K P5S
113-2 STRA30
213-2 STRA20
114-2 STRA10
214-2 STRA00
116-2 STRB10
216-2 STRB00
117-2 STRB30
217-2 STRB20
A15 19-057 SG
A14 19-064 SF
CSAPDO
CSBPDO
A18 19-055 SG
A15 19-067 SG
A21 30-018 DELAY LINE 100NS
1,8,9,10,16
R10 100
SEE TABLE 1 & NOTE 1
A15-13
A17-13
A15-5
A20-2
A16-11
A11-10
A16-5
A20-12
WRTT1 14 3N5
A20 19-056 SG FECLKO 7 105-2
A20 19-056 SG ENDCYLO 11 207-2
A11 19-058 SG STRBOA 3 3M7
A16 19-057 SG
A19 19-055 SG WRTGOA 2 3M5
MWRTOA 1 107-2
CSBPDO 9 5A1
CSAPDO 10 4A1
COMPONENT LOCATOR 35-432 (REF)
A20 A13 A19 A12 A18 A14 A21 A17 A10 A11 A15 A16
25-336 APP

TABLE 1		
POSSIBLE TIMING ADJ.		
SET	A20-12 & A11-10	A16-5
1	5	11
2	12	7

NOTES 1. FIXED STRAPPING IS AS SHOWN- ADDITIONAL STRAPPING IS REQUIRED AND DETERMINED AT FACTORY. FACTORY WILL EQUIP SET 1 OR SET 2 STRAPPING SHOWN BY TABLE 1.

REVISIONS

REDRAWN DUE TO REDESIGN

KL	LP.	3214-07		8-10-72	R03

REMOVED: A17(19-042) & ASSOC CIRCUITRY; L1 & L2 WERE 4.7UH; C3 & C4 WERE 22 PF.
CHANGED: A18-2 & -13 WERE TO A17-13; A19-12 WAS TO A17-4; A14-4 WAS TO A17-3; A11-12 WAS TO A17-1

7	LP.	3214-11		9-19-72	

CHANGED - 35-432 WAS R01; C6 & C8 WERE 47PF; A20-2 WAS TO A21-2; A18-4 WAS TO OPTION TERM; A18-13 WAS TO R11-1K TO P5S; A19-12 WAS TO GND; A12-4 WAS TO A12-2.
ADDED - A15-12 & -13; A17 & ASSOC LEADS.
DOC. CHANGE ONLY - AT 6B8, ALL AB--0 & AB--1 MNEMONICS WERE REVERSED (4 EA)

7	LP.	3214-15		9-25-72	R04

CHANGED - AT LOC (A3), A11-13 WAS TO SROB 106-3 (A1); AT (E...) A18-02 & 13 WERE TO A17-02; AT (G4) A17-10 WAS TO A16-10 (K6).
ADDED - AT (A1) MRSTO TO 103-2; AT (K4) A17-11 TO A17-10 & A17-13 TO OPTION. 35-432 WAS R02

7	LP.	3214-18		10-30-72	R05

AT LOC A7, AA021B WAS AA020A, AA020B WAS AA021; AA031B WAS AA030A, AA030B WAS AA031; AB020 AND AB021 WERE REVERSED.

7	LP.	3214-21		12-4-72	R06

AT LOC J2 & J4 CAPS C6 & C8 WERE 68 PF; AT N1, 35-432 WAS R02.

7	LP.	3214-25		12-21-72	R07

AT LOC A1, MNEM. GR1 WAS MRSTO.

7	LP.	3214-26		1-11-73	R08

THIS WAS SHEET 6 ADDED COMPONENT LOCATOR, TABLE 1 & NOTE 1. REVISED STRAPPING.

WZ	CBC	3214-34		4-19-73	R09

ADDED 'WRTT1' AREA N4

	CBC	3214-42		7-16-73	R10

NAME	TITLE	DATE
K. LAFFERTY	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC MODEL 80 MSU

TASK NO. 03214

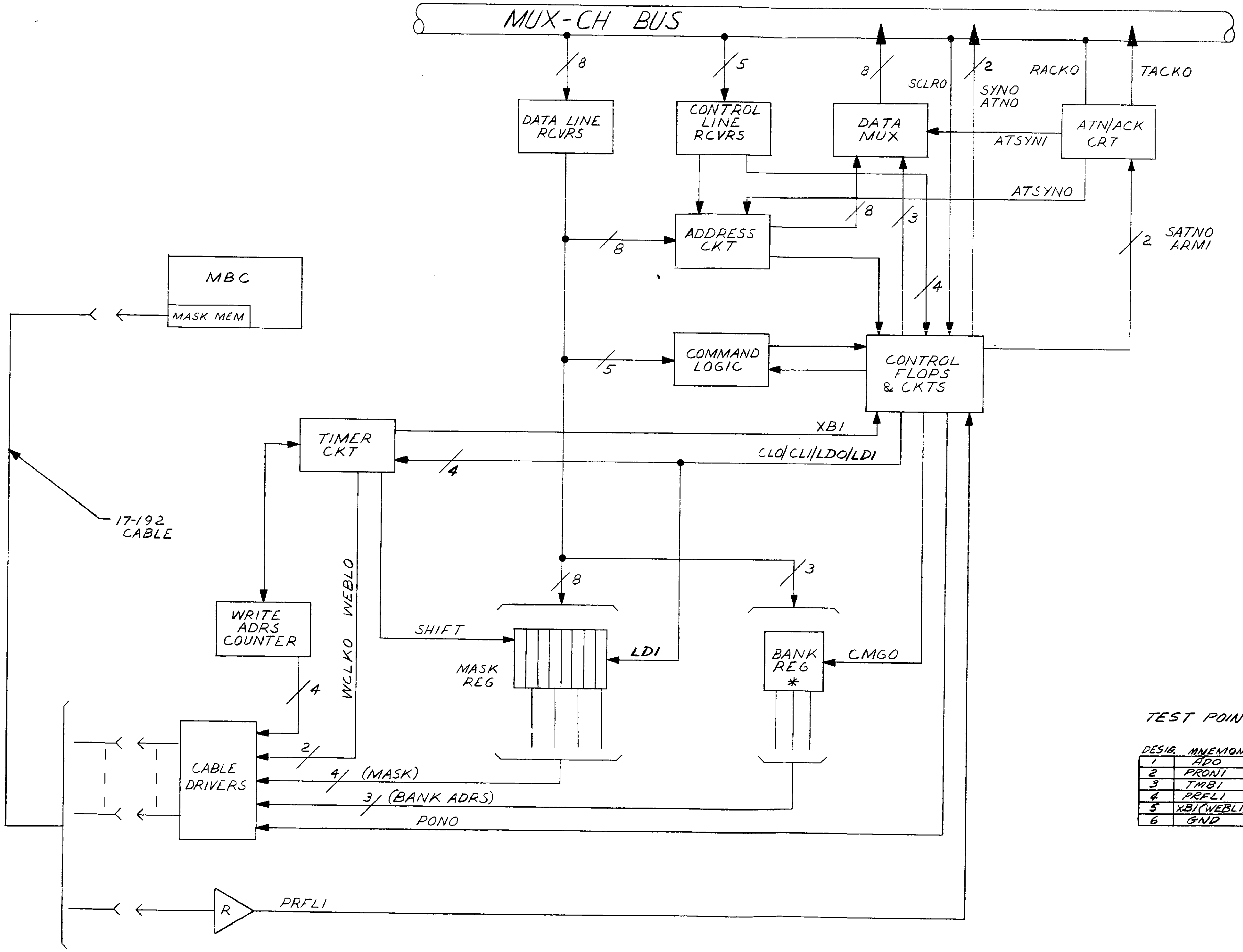
DWG NO. 02-247 R10 D08

SHEET OF 10-10

BRUNING 44-231 16042

INTERDATA®

REVISIONS					
PRE PRODUCTION APPROVAL	DEV LP				
	PROD				
CHANGED SH. 1, 2 & 3 (SEE IND. SHT. FOR REV NOTES); AT G6, LDI WAS DAGI; AT H5, REMOVED DAGI & ADDED LDO/LDI, LINE QTY WAS 3.					
7	LP	3214-20		11-22-72	R01



MUX-CH BUS
8
5
8
SCLRO
2
SYNO
ATNO
RACKO
TACKO
DATA LINE RCVRS
CONTROL LINE RCVRS
DATA MUX
ATN/ACK CRT
ATSYNI
ATSYNO
ADDRESS CKT
8
8
3
2
SATNO
ARMI
MBC
MASK MEM
4
COMMAND LOGIC
5
CONTROL FLOPS & CKTS
TIMER CKT
XBI
CLO/CLI/LDO/LDI
4
17-192 CABLE
8
3
WEBLO
WCLKO
SHIFT
WRITE ADRS COUNTER
MASK REG
LDI
BANK REG *
CMGO
4
2
CABLE DRIVERS
4 (MASK)
3 (BANK ADRS)
PONO
R
PRFLI

CONN 0/1

	2	1
41	GND	P5
	GND	GND
35		
30		
25		
	ATNO	SYNO
	TACKO	RACKO
	DAO	
20	CMDO	DRO
	ADRSO	SRO
	D150	D140
	D130	D120
	D110	D100
15	D090	D080
10		
05		
	GND	GND
00	GND	P5

TEST POINTS

DESIG.	MNEMONIC	
1	ADO	3C6
2	PRONI	3L2
3	TMBI	3L3
4	PRFLI	3L1
5	XBI(WEBLI)	3L3
6	GND	3K1

CONN 2

	2	1
12	GND	WSBI
	↓	WSDI
	↓	WSAI
09	↓	WSCI
	↓	MSK30
	↓	MSK20
06	↓	MSK00
	↓	MSK10
	↓	BP020
03	↓	BP010
	GND	BP000
	WEBLO	WCLKO
00	PONO	PRFLO

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION:

35-408 R02

NOTES 1. ASTERISK * INDICATES PORTION NOT NORMALLY EQUIPPED.

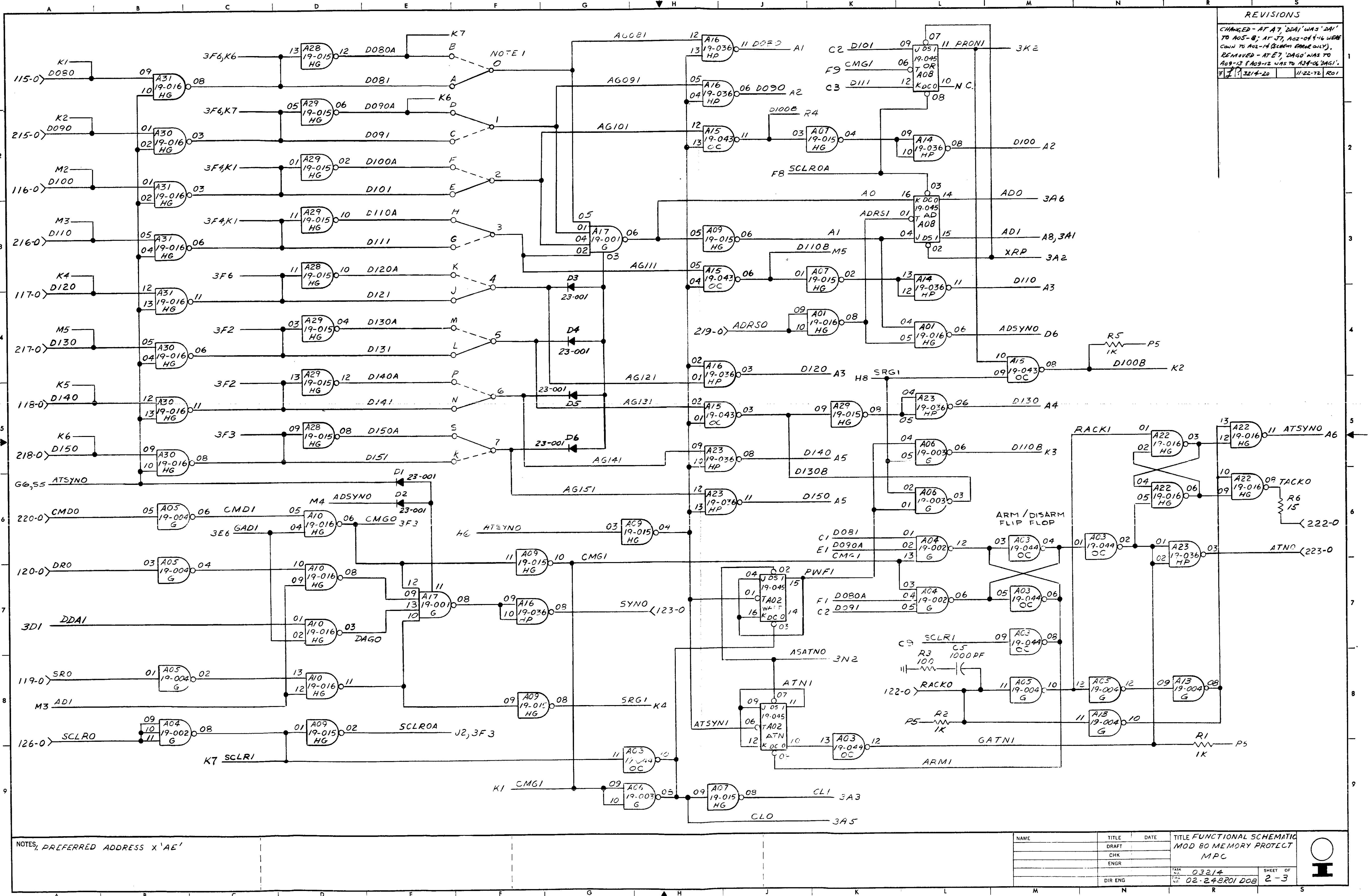
NAME	TITLE	DATE
B GRAY	DRAFT	6-16-72
J F FLEMING	CHK	8-3-72
R SCHUNNEMAN	ENGR	
M FUCHS	QC	
R E JONES	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MOD 80 MEMORY PROTECT
MPC

TASK NO. 03214
DWG NO. 02-248R01D08
SHEET OF 1-3

BRUNING 44-231 16042

INTERDATA®



115-0 K1 D080
215-0 K2 D090
116-0 M2 D100
216-0 M3 D110
117-0 K4 D120
217-0 M5 D130
118-0 K5 D140
218-0 K6 D150
A31 19-016 HG
A30 19-016 HG
A28 19-015 HG
A29 19-015 HG
3F6,K6
3F6,K7
3F4,K1
3F6
3F2
3F3
D080A
D081
D090A
D091
D100A
D101
D110A
D111
D120A
D121
D130A
D131
D140A
D141
D150A
D151
K7
K6
NOTE 1
D3 23-001
D4 23-001
D5 23-001
D6 23-001
A17 19-001 G
AG081
AG091
AG101
AG111
AG121
AG131
AG141
AG151
A16 19-036 HP
A15 19-043 OC
A07 19-015 HG
A14 19-036 HP
A09 19-015 HG
A01 19-016 HG
A23 19-036 HP
A06 19-003 G
D080 A1
D090 A2
D100B R4
D100 A2
SCLR0A F8
C2 D101
F9 CMG1
C3 D111
A08 19-045 OR
PRON1 3K2
N.C.
A0
ADRS1
AD0 3A6
AD1 A8,3A1
XRP 3A2
D110B M5
D110 A3
219-0 ADRS0
ADSYNO D6
R5 1K P5
D100B K2
D120 A3
H8 SRG1
D130 A4
D140 A5
D130B
D110B K3
D150 A5
RACK1
A22 19-016 HG
ATSYNO A6
TACKO
R6 15
222-0
ARM / DISARM FLIP FLOP
AC3 19-044 OC
A04 19-002 G
C1 D081
E1 D090A
CMG1
F1 D080A
C2 D091
ATNO 223-0
G6,S5 ATSYNO
D1 23-001
M4 ADSYNO
D2 23-001
220-0 CMD0
A05 19-004 G
CMD1
A10 19-016 HG
CMG0 3F3
3E6 GAD1
120-0 DR0
3D1 DDA1
DAGO
119-0 SR0
M3 AD1
126-0 SCLR0
A04 19-002 G
SCLR0A J2,3F3
K7 SCLR1
H6 ATSYNO
AC9 19-015 HG
A09 19-015 HG
CMG1
A16 19-036 HP
SYNO 123-0
SRG1 K4
PWF1
A02 19-045 WAIT
ASATNO 3N2
ATN1
A02 19-045 ATN
ATSYN1
C9 SCLR1
R3 100
C5 1000 PF
122-0 RACK0
P5 R2 1K
AC5 19-004 G
A13 19-004 G
GATN1
R1 1K P5
A03 19-044 OC
ARM1
K1 CMG1
AC6 19-003 G
A07 19-015 HG
CL1 3A3
CL0 3A5

REVISIONS

CHANGED - AT A7, 'DDA1' WAS 'DA1' TO A05-8; AT J7, A02-04 & -16 WERE CONN TO A02-14 (SCHEM ERROR ONLY). REMOVED - AT E7, 'DAGO' WAS TO A09-13 & A09-12 WAS TO A34-06 'DAG1'.

7	L	P	3214-20		11-22-72	R01

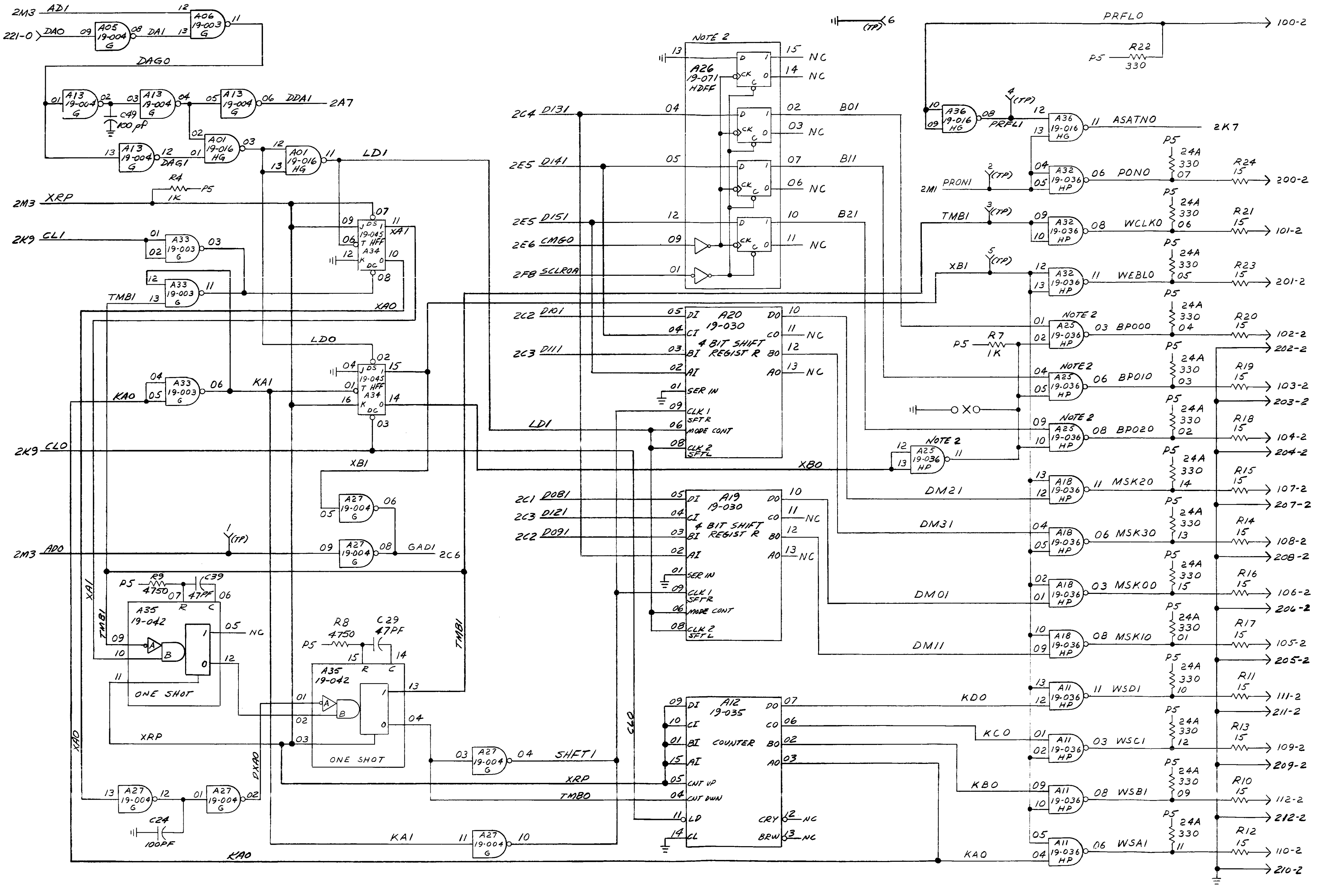
NOTES: 1. PREFERRED ADDRESS X'AE'

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC MOD 80 MEMORY PROTECT
MPC

TASK NO. 03214
DWG NO. 02-248R01 D08
SHEET 2 OF 3

INTERDATA®



2M3 ADI
221-0 DAO
A05 19-004 G
DAI
A06 19-003 G
DAGO
A13 19-004 G
C49 100 pF
DDAI 2A7
A01 19-016 HG
DAG1
LDI
R4 1K P5
2M3 XRP
2K9 CL1
A33 19-003 G
TMB1
A34 19-045 T HFF
XA1
XAO
LDO
KA1
KAO
XB1
2K9 CLO
2M3 ADO
A27 19-004 G
GADI 2C6
R9 4750 C39 47PF
A35 19-042 ONE SHOT
R8 4750 C29 47PF
XRP
TMB1
SHFT1
TMBO
DXAO
C24 100PF
NOTE 2
A26 19-071 HDFF
2C4 D131
2E5 D141
2E5 D151
2E6 CMGO
2F8 SCLROA
B01
B11
B21
NC
2C2 D101
2C3 D111
A20 19-030 4 BIT SHIFT REGIST R
SER IN
CLK 1 SFT R
MODE CONT
CLK 2 SFT L
XBO
2C1 D081
2C3 D121
2C2 D091
A19 19-030 4 BIT SHIFT REGIST R
A12 19-035 COUNTER
CNT UP
CNT DWN
LD
CL
CRY
BRW
PRFLO 100-2
R22 330 P5
A36 19-016 HG
PRFLI
ASATNO 2K7
2M1 PRONI
A32 19-036 HP
PONO
WCLKO
WEBLO
A25 19-036 HP
BP000
BP010
BP020
R7 1K
A18 19-036 HP
DM21 MSK20
DM31 MSK30
DM01 MSK00
DM11 MSK10
A11 19-036 HP
KDO WSDI
KCO WSCI
KBO WSBI
KAO WSAI
24A 330
R24 15 200-2
R21 15 101-2
R23 15 201-2
R20 15 102-2 202-2
R19 15 103-2 203-2
R18 15 104-2 204-2
R15 15 107-2 207-2
R14 15 108-2 208-2
R16 15 106-2 206-2
R17 15 105-2 205-2
R11 15 111-2 211-2
R13 15 109-2 209-2
R10 15 112-2 212-2
R12 15 110-2 210-2

REVISIONS

REMOVED - AT B4, A33-10 WAS 'KAO' TO A33-04, A33-09 WAS 'XA1' TO A34-11, A33-08 WAS TO A34-02; AT N1, C40-1000PF & R25-100Ω WERE IN SERIES FROM 'PRFLO' TO GND. CHANGED - AT B6 & D7, R8 & R9 WERE 12.6K, AND C29 & C39 WERE 100PF; AT F5, 'LDI' WAS 'DAG1' & CKT WAS CONN TO A09-12. ADDED - NOTE 2; GATES A06-11, A33-02, A33-04, -06 & -12, A01-03 & -11, C49 AND ALL ASSOC CKT CONN FROM ADI & DAI TO LDO & LDI.

7	LP.	3214-20		11-22-72	R01

NOTES 2. A25 & A26 ARE NOT NORMALLY EQUIPPED.

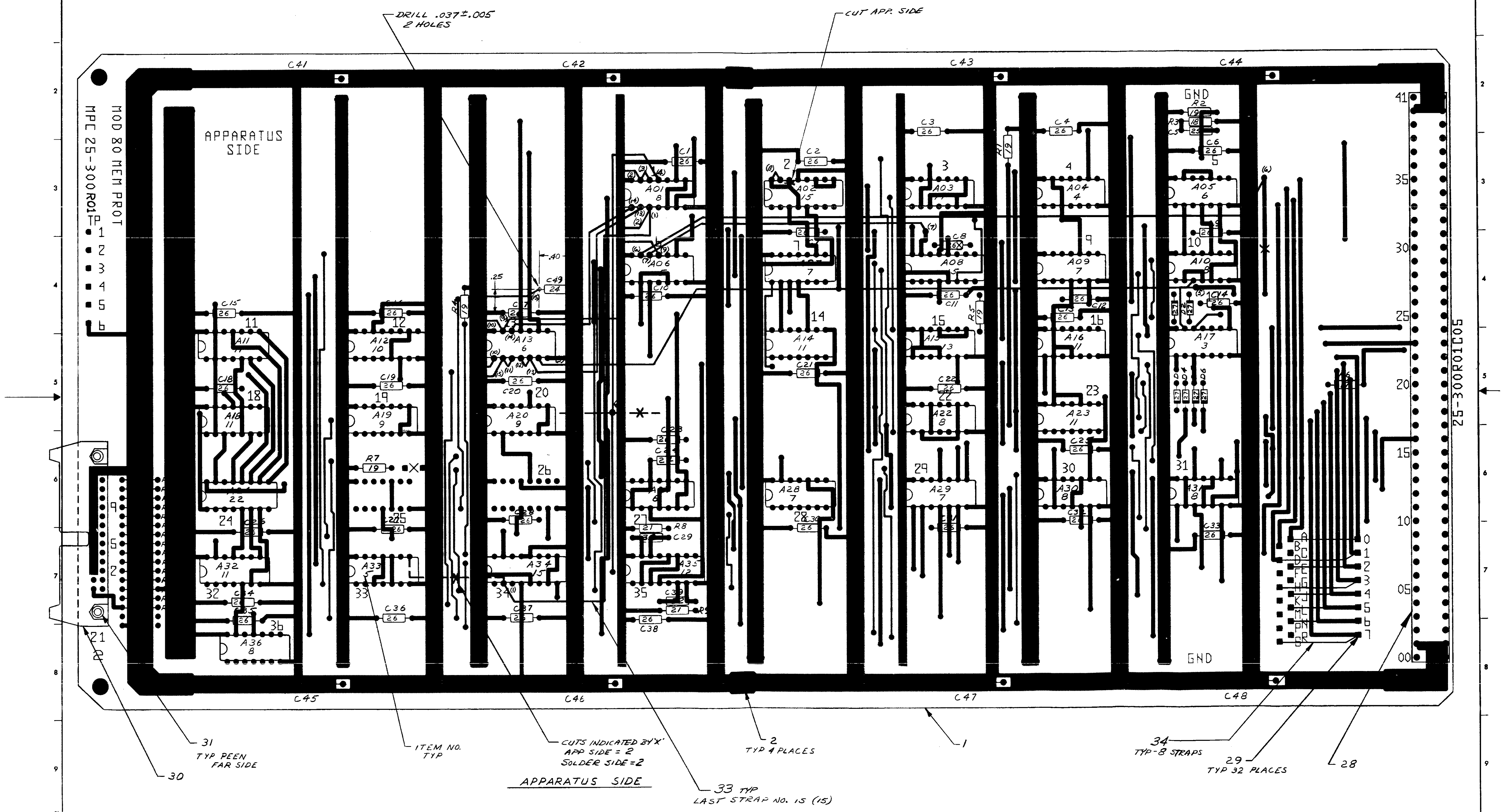
NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC
MOD 80 MEMORY PROTECT
MPC

TASK NO. 03214
DWG NO. 02-248R01 D08
SHEET OF 3-3

BRUNING 44-231 16042

INTERDATA®


DRILL .037±.005
2 HOLES
CUT APP. SIDE
MOD 80 MEM PROT
MPC 25-300R01
APPARATUS SIDE
TP
1
2
3
4
5
6
C41
C42
C43
C44
C45
C46
C47
C48
GND
25-300R01L05
41
35
30
25
20
15
10
05
00
31
TYP PEEN
FAR SIDE
30
ITEM NO.
TYP
CUTS INDICATED BY 'X'
APP SIDE = 2
SOLDER SIDE = 2
33 TYP
LAST STRAP NO. IS (15)
2
TYP 4 PLACES
1
34
TYP-8 STRAPS
29
TYP 32 PLACES
28

APPARATUS SIDE

REVISIONS

PRE PRODUCTION APPROVAL		INIT.	DATE
	DEV	RHck	8/17/72
	PROD		8/24/72

REMOVED – A25 WAS ITEM 11; A26 WAS ITEM 16; AT CONN 2, BOTTOM 2 POSITIONS WERE C46 ITEM 25 TO 100-2 & R25 ITEM 18 TO GND BUS. CHANGED – C29 & C39 WERE ITEM 24. ADDED – 2 APP. CUTS & 2 SOLDER CUTS; 15 STRAPS ITEM 33; 8 STRAPS ITEM 34; C49 (ITEM 24) & ASSOC. DIMS.

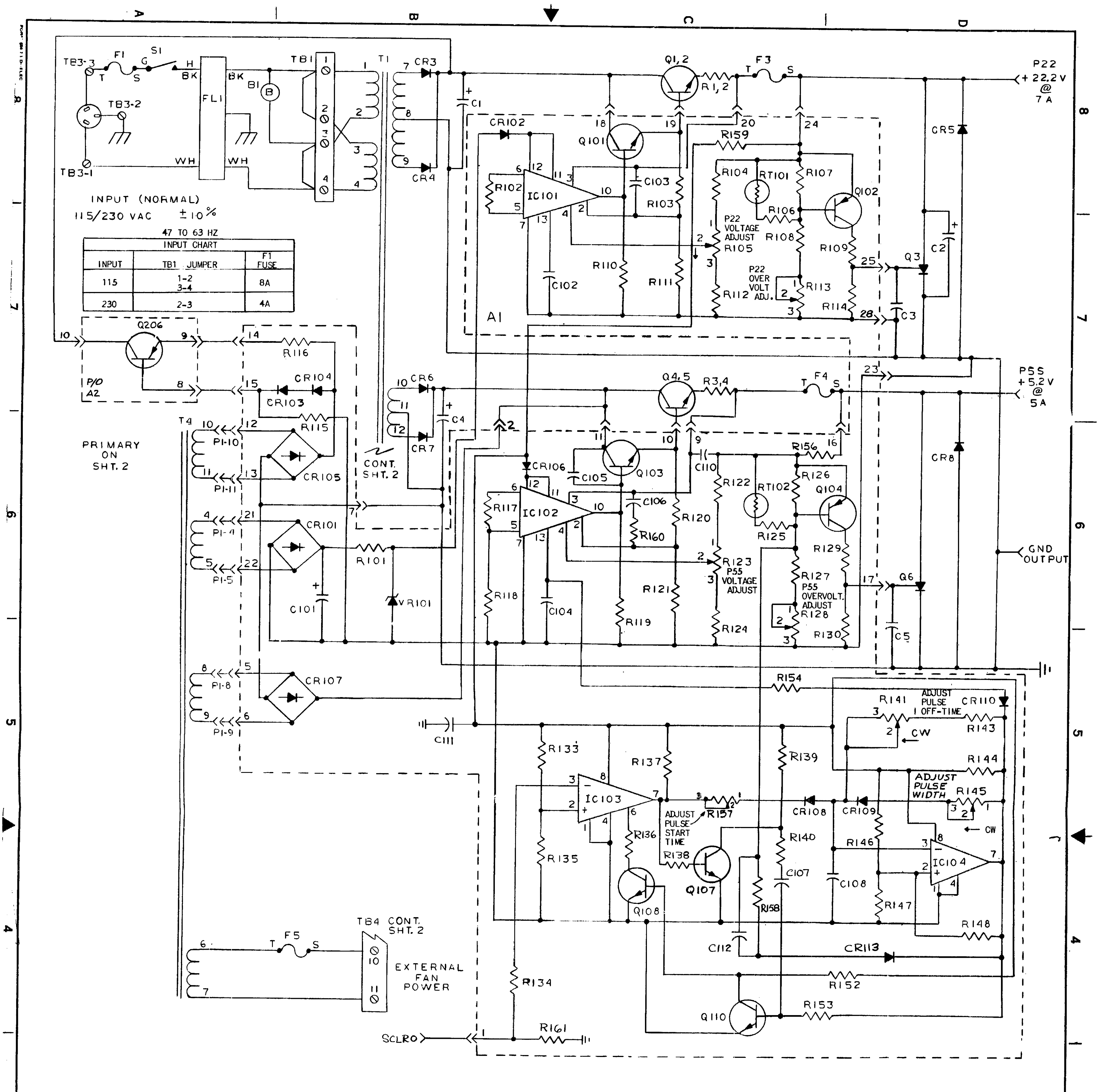
Y	PFS	3214-20	CP	11-22-72	R01

NAME		DATE
B GRAY		7-28-72
J F FLEMING		8-3-72
S MESSINA		
M FUCHS	QC	
R E JONES	DIR ENG	

TITLE
ASSEMBLY PRINTED CIRCUIT
MEMORY PROTECT
MOD 80 MPC

TASK NO. 03214
35-408R01D03
SHEET 1 OF 1

BRUNING 44-231 16042


P22
+22.2V @ 7A
P5S
+5.2V @ 5A
GND OUTPUT
TB3-3
TB3-2
TB3-1
F1
S1
FL1
B1
TB1
T1
CR3
CR4
C1
Q1,2
R1,2
F3
CR5
C2
Q3
C3
CR102
IC101
R102
Q101
C103
R103
R110
R111
C102
A1
R159
R104
RT101
R107
R106
Q102
P22 VOLTAGE ADJUST R105
R108
R109
R112
P22 OVER VOLT ADJ.
R113
R114
Q206
P/O A2
R116
CR104
CR103
R115
CR105
T4
P1-10
P1-11
P1-4
P1-5
P1-8
P1-9
PRIMARY ON SHT. 2
CR6
CR7
C4
CONT. SHT. 2
CR101
R101
C101
VR101
CR107
Q4,5
R3,4
F4
CR106
C105
Q103
IC102
R117
C106
R160
R120
R121
R118
C104
R119
C110
R122
RT102
R156
R126
Q104
R125
R123
P55 VOLTAGE ADJUST
R124
R129
R127
P55 OVERVOLT. ADJUST
R128
R130
Q6
C5
CR8
C111
R154
R141
ADJUST PULSE OFF-TIME
CR110
R143
CW
R144
ADJUST PULSE WIDTH
R145
R133
R137
R139
IC103
R135
R136
ADJUST PULSE START TIME
R157
R138
Q107
Q108
CR108
CR109
R140
C107
R146
C108
IC104
R147
R158
R148
C112
CR113
R152
Q110
R153
R134
R161
SCLRO
TB4 CONT. SHT. 2
F5
EXTERNAL FAN POWER

INPUT (NORMAL)
115/230 VAC ±10%
47 TO 63 HZ

INPUT CHART		
INPUT	TB1 JUMPER	F1 FUSE
115	1-2 3-4	8A
230	2-3	4A

*NOTE: ASTERISK * BY PART NUMBER DESIGNATES INTERDATA PART NUMBER*

COMPONENT CHART

CIRCUIT REF.	DESCRIPTION	PART NO.
B1	FAN	312 0020
C1	CAP. 40,000 MFD @ 50 VDC	304 2181
C2	CAP. 300 MFD @ 25 VDC	304 1502
C3	CAP. 1 MFD @ 35 VDC	304 1299
C4	CAP. 50,000 MFD @ 25 VDC	304 2153
C5	CAP. 2 MFD @ 50 VDC	304 0972
CR3-8	DIODE 1N1201A	337 1405
F1,4	FUSE 8A ABC	315 0182
F3	FUSE 10A AGC	315 0101
F5	FUSE 1.5A AGC	315 0144
S1	SWITCH 4 POLE	366 0514
FL1	LINE FILTER	375 0441
Q1,2,4,5	TRANSISTOR 2N3055	370 0202
Q3,6	SCR	337 1562
Q206	TRANSISTOR 2N3740	370 0160
T1	TRANSFORMER	602 2670
R1-4	RES. .2Ω, 1% 3W	340 5321
A1	PRINTED WIRING BOARD	620 0832
C110	CAP. .1 MFD @ 100 VDC	304 1655
C111	CAP. 15 MFD @ 25 VDC	* 22-031
C106, C112	CAP. .1 MFD @ 30 VDC	* 22-033
C101	CAP. 150 MFD @ 50 VDC	304 1503
C102,103	CAP. .01 MFD @ 50 VDC	304 1346
C105	CAP. .0022 MFD @ 100 VDC	304 1048
C107	CAP. 220 PF @ 100VDC	*22-007F14
C108	CAP. .0022 MFD @ 100 VDC	*22-021F01
CR113	DIODE HI-SPEED	*23-001
CR101,105,107	DIODE BRIDGE	337 1674
CR102,106	DIODE 1N645	337 1363
CR103,104,108-110	DIODE	0533978
C104	CAP. .001 UF @ 100 VDC	304 1862
IC101,102	IC REG.	371 3002
IC103,104	VOLTAGE COMPARATOR LM311	371 0014
Q101,103	TRANS. 2N3054	370 0223
Q102,104	TRANS. 2N3133	370 0144
Q107-108,110	TRANS. 2N2218	0533802
R105,113	POTENTIOMETER 5KΩ, 10% 3/4W	341 0837
R101	RES. 600Ω, 5%, 5W	340 8028
R102,111	RES. 5100Ω, 2%, 1/4W	340 2349
R103	RES. 270Ω, 2% 1/4W	340 2318

CIRCUIT REF.	DESCRIPTION				PART NO.
R104	RES.	17.4K,	1%,	1/4W	340 8668
R128	POT.	2K,	10%	3/4W	341 0836
R106	RES.	475Ω,	1%	1/4W	340 0061
R107,126	RES.	200Ω,	1%	1/4W	340 0007
R108	RES.	5.49K,	1%	1/4W	340 5217
R109	RES.	120Ω,	2%	1/2W	340 6651
R110	RES.	12KΩ,	2%	1/4W	340 2358
R112	RES.	6810Ω,	1%	1/2W	340 6292
R114,130	RES.	510Ω,	2%	1/2W	340 6613
R115,	RES.	1600Ω,	2%	2W	340 6851
R116	RES.	4.02Ω,	1%	3W	340 6312
R117,118	RES.	1KΩ,	1%	1/4W	340 0014
R119	RES.	3.3KΩ,	2%	1/2W	340 6669
R161	RES.	4.7KΩ	5%	1/4W	*21-001F10
R121	RES.	820Ω,	2%	1/2W	340 6611
R122	RES.	249Ω,	1%	1/2W	340 6109
R123	POT.	500Ω,	10%	3/4W	341 0834
R124	RES.	1150Ω,	1%	1/4W	340 0064
R125	RES.	475Ω,	1%	1/4W	340 0061
R127	RES.	698Ω,	1%	1/4W	340 0011
R129,156	RES.	10Ω,	2%	1/2W	340 6626
R158	RES.	2.2KΩ,	5%	1/4W	*21-001F21
R133,137	RES.	100KΩ,	2%	1/4W	340 2380
R134,135	RES.	7.5KΩ,	2%	1/4W	340 2353
R136	RES.	6.8KΩ,	5%	1/4W	*21-001F13
R138	RES.	240KΩ,	2%	1/2W	340 6710
R139	RES.	18KΩ,	2%	1/4W	340 2362
R141, 157	POT.	200KΩ,	10%	3/4W	341 0842
R140	RES.	390KΩ,	5%	1/4W	*21-001F15
R143	RES.	1.2 MEGOHM	5%	1/4W	~
R144	RES.	12KΩ,	2%	1/4W	340 2358
R145	POT.	100KΩ,	10%	3/4W	341 0841
R146-148	RES.	110KΩ,	2%	1/4W	340 2381
R159	RES.	47Ω,	5%	1/4W	*21-001F02
R154	RES.	1.8K,	2%	1/2W	340 6604
R152	RES.	750KΩ,	2%	1/2W	340 6722
R153	RES.	680KΩ,	2%	1/2W	340 6721
R120	RES.	180Ω,	2%	1/2W	340 6655
R160	RES.	470Ω,	5%	1/4W	*21-001F06
RT101,102	THERMISTOR	1KΩ	@	25C	369 0014
VR101	ZENER DIODE	1W	33V	1N4752	337 1483

REVISIONS

DELETED - C109, CR111, & R112, Q109, R149, R150, R151 & R155; ADDED - R158, R159, R160, C111, C112, CR113 (Could TERM #28); CHANGED - VALUES FOR C106, C107, C108, R136, R140 & R143; SEE 'VOID' R01 (8 ADJUST) with 2, ADDED STRAP TB4-7 E8.

★	E	C	3213-04	QB	3-6-73	R02
ADDED R161 ON PC BOARD A1 (SK.1C4)						
★	A	L	3213-06	GL	5-2-73	R03

ENG. LEVEL	DATE
8511493	10-3-72
M 8511420	9-11-72 CB
8511415	9-11-72 CB
M 8511282	6-6-72
8500050	5-15-72

N.E.C. REF. CODE
INTERDATA APPROVAL ENGR: DATE: 10/18/72

DRAWN	R. Thompson	2-15-72
CHECKED	D. Mulder	5-11-72
APPROVED	Ron Cook	6-6-72
APPROVED	J.S. Shaw	6 June 72

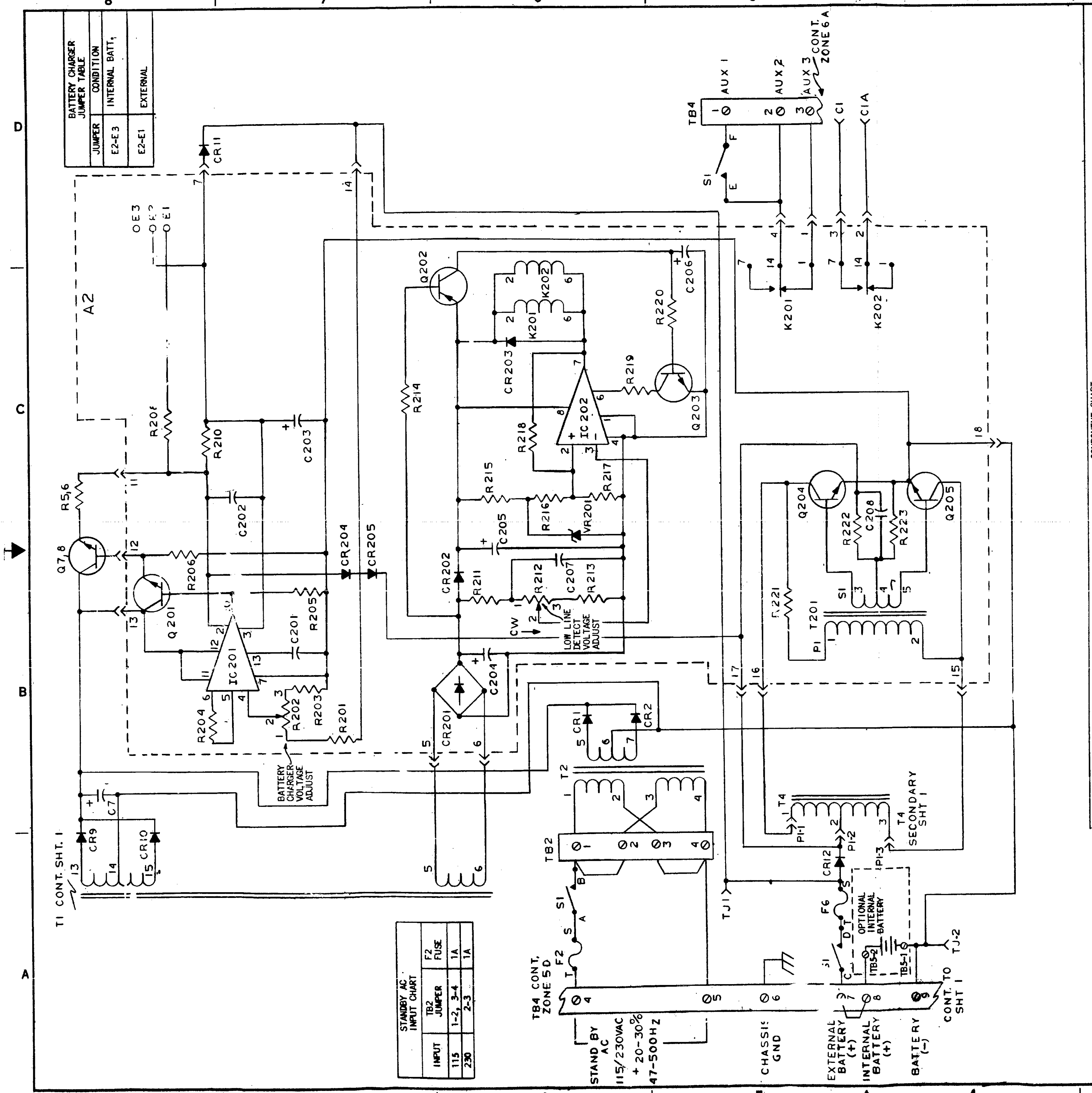
PEC-3588

NORTH ELECTRIC COMPANY ELECTRONICS DIVISION

SCHEMATIC
POWER SYSTEM
(N.E.#4392025)

CODE IDENT. NO. SIZE D 34-014R03D08
SCALE NONE UNIT WEIGHT SHEET 1 OF 2

[UNONOWA]


A2
OE3
OE2
OE1
CR11
R20
R210
C203
C202
R5,6
Q7,8
Q201
R206
R205
C201
IC201
R204
R202
R203
R201
BATTERY CHARGER VOLTAGE ADJUST
CR204
CR205
R214
Q202
CR202
CR203
K201
K202
IC202
R215
R216
R217
R218
VR201
C205
R211
R212
R213
C207
CW
LOW LINE DETECT VOLTAGE ADJUST
C204
CR201
R219
R220
Q203
C206
Q204
Q205
R222
R223
C208
R221
T201
S1
P1
CR9
CR10
C7
T1 CONT. SHT. 1
T2
CR1
CR2
TB2
S1
F2
T4
T4 SECONDARY SHT 1
CR12
F6
OPTIONAL INTERNAL BATTERY
TB5-2
TB5-1
TJ1
TJ-2
TB4
AUX 1
AUX 2
AUX 3
CONT. ZONE 6 A
C1
C1A
TB4 CONT. ZONE 5 D
STAND BY AC
115/230VAC
+ 20-30%
47-500HZ
CHASSIS GND
EXTERNAL BATTERY (+)
INTERNAL BATTERY (+)
BATTERY (-)
CONT. TO SHT 1

BATTERY CHARGER JUMPER TABLE	
JUMPER	CONDITION
E2-E3	INTERNAL BATT.
E2-E1	EXTERNAL

STANDBY AC INPUT CHART		
INPUT	TB2 JUMPER	F2 FUSE
115	1-2, 3-4	1A
230	2-3	1A

COMPONENT CHART

CIRCUIT REF.	DESCRIPTION	PART NO.	CIRCUIT REF.	DESCRIPTION	PART NO.
C7	CAP. 4,900 MFD @ 50 VDC	304 2176	R201,203	RES. 6.2KΩ, 2% 1/4W	340 2351
			R202	POT. 2KΩ, 10% 3/4W	341 0836
			R204	RES. 3.6KΩ, 2% 1/4W	340 2345
CR1,2,9-12	DIODE 1N1201A	337 1405	R205,206	RES. 7.5KΩ, 2% 1/4W	340 2353
			R208	RES. .3Ω, 1% 3W	340 5307
F2	FUSE 1A AGC	315 0045	R210	RES. 1.5Ω, 1% 3W	340 5395
F6	FUSE 4A AGC	315 0360	R211,214	RES. 11KΩ, 2% 1/4W	340 2357
			R212	POT. 5K, 10% 3/4W	341 0837
			R213,217	RES. 8.2K, 2% 1/4W	340 2354
Q7,8	TRANSISTOR 2N3055	370 0202	R215	RES. 680Ω, 2% 1W	340 4241
			R216	RES. 1.8KΩ, 2% 1/4W	340 2338
R5,6	RESISTOR .2Ω, 1% 3W	340 5321	R218	RES. 30KΩ, 2% 1/4W	340 2367
T2	TRANSFORMER	601 2671	R219	RES. 2.7K, 2% 1/4W	340 2342
T4	TRANSFORMER	601 2673	R220	RES. 4.3KΩ, 2% 1/4W	340 2347
			R221	RES. 1KΩ, 2% 1/4W	340 2332
			K222	RES. 220Ω, 2% 1W	340 4230
			R223	RES. 62Ω, 2% 1/4W	340 2303
A2	PRINTED WIRING BOARD	620 0833			
C201,202	CAP. .01 MFD @ 50 VDC	304 1346			
C203	CAP. 220 MFD @ 15 VDC	304 1145	T201	TRANSFORMER	601 2672
Q204	CAP. 10 MFD @ 50 VDC	304 1222			
C205	CAP. 400 MFD @ 50 VDC	304 1509			
C2[illegible]	CAP. 5 MFD @ 50 VDC	304 1473	VR201	ZENER DIODE 1N758A	337 1490
C207	CAP. .47 MFD @ 100 VDC	304 1415			
C208	CAP. .1 MFD @ 100 VDC	304 1655			
CR201	RECTIFIER BRIDGE	337 1674			
CR202,203	DIODE 1N645	337 1363			
CR204,205	DIODE 1N5402	337 1641			
IC201	REGULATOR μA723C - DIP	371 3002			
IC202	VOLTAGE COMPARATOR LM311	371 0014			
K201,202	RELAY SIGMA 191-TE1C1-24L	339 0643			
Q201	TRANSISTOR 2N3054	370 0223			
Q202	TRANSISTOR 2N3133	370 0144			
Q203	TRANSISTOR 2N2218	0533802			
Q204,205	TRANSISTOR 2N3055	370 0202			

4392025

	8511493	10-3-72
M	8511420	9-11-72
	8511415	9-11-72
M	8511292	6-6-72
	8500050	5-15-72
	ENG. LEVEL	DATE

N.E.C. REF. CODE

NORTH
ELECTRIC COMPANY
ELECTRONETICS DIVISION

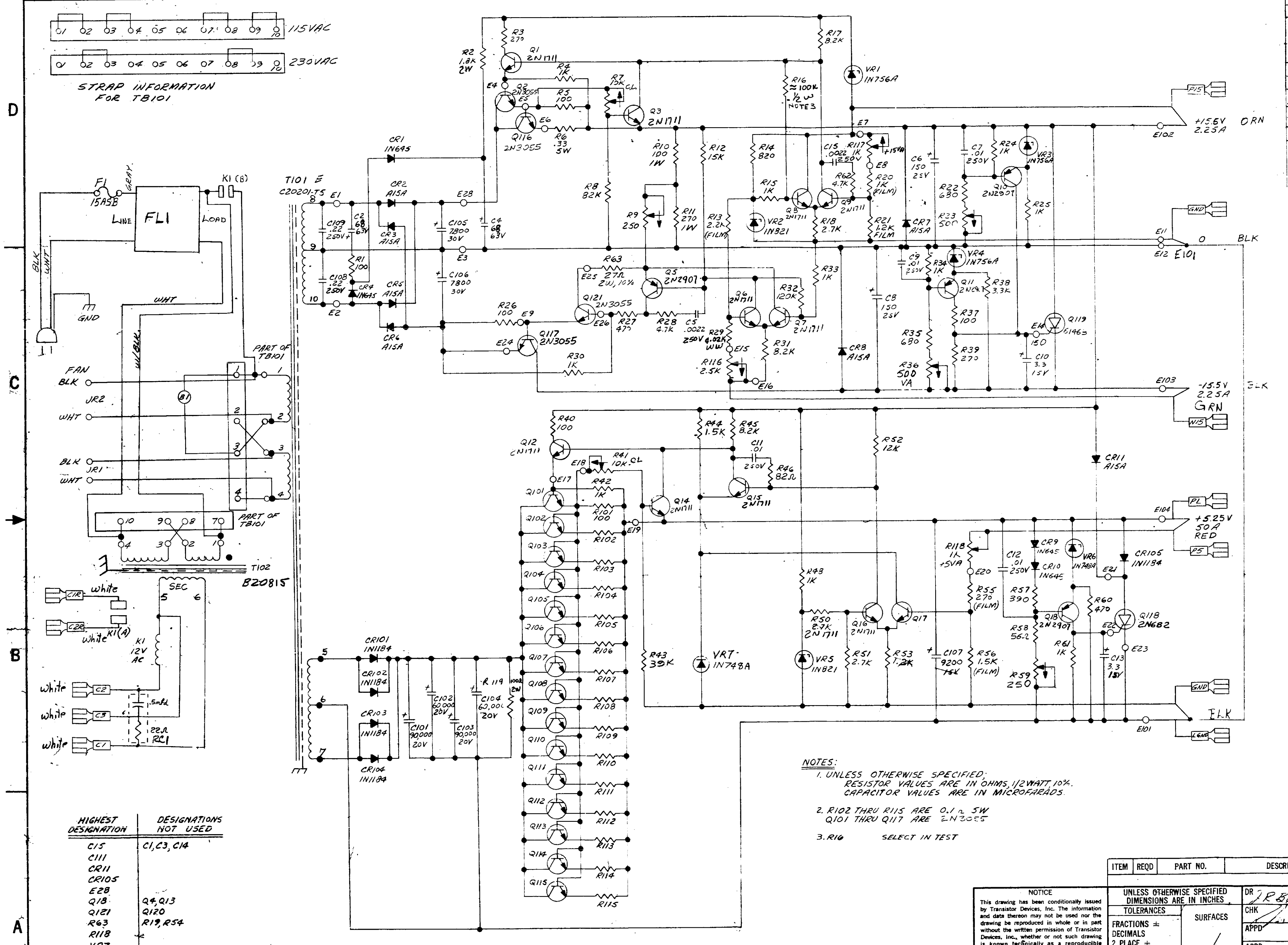
DRAWN	R Thompson	2-16-72
CHECKED	D Mulder	5-11-72
APPROVED	[illegible]	6-6-72
APPROVED	J.S. Shead	6 Jun 72

SCHEMATIC
POWER SYSTEM
(N.E.#4392025)

PEC-3588

CODE IDENT. NO. | SIZE D | 34-014R03D08

SCALE None | UNIT WEIGHT | SHEET 2 OF 2


STRAP INFORMATION FOR TB101
115VAC
230VAC
F1 1.5ASB
FL1
LINE
LOAD
K1 (B)
GRAY
BLK
WHT
GND
FAN
JR2
JR1
B1
PART OF TB101
T101 E C20201-TS
T102 B20815
SEC
K1 12V AC
K1(A)
C1R
C2R
.5mfd
22Ω
RC1
white
CR1 1N645
CR2 A15A
CR3 A15A
CR4 1N645
CR5 A15A
CR6 A15A
C109 .22 250V
C108 .22 250V
C2 68 63V
C4 68 63V
R1 100
C105 2800 30V
C106 7800 30V
E1
E2
E3
E28
R2 1.8K 2W
R3 270
Q1 2N1711
Q2 2N3055
Q116 2N3055
R4 1K
R5 100
R6 .33 5W
R7 10K CL
Q3 2N1711
R8 82K
R9 250
R10 100 1W
R11 270 1W
R12 15K
R13 2.2K (FILM)
R14 820
R15 1K
R16 ≈100K ½W NOTE3
R17 8.2K
VR1 1N756A
VR2 1N821
Q8 2N1711
Q9 2N1711
R18 2.7K
C15 .0022 250V
R117 1K +15VA
R62 4.7K
R20 1K (FILM)
R21 1.2K FILM
C6 150 25V
CR7 A15A
C7 .01 250V
R24 1K
VR3 1N756A
Q10 2N2907
R22 680
R23 500
R25 1K
R63
E25 27Ω 2W, 10%
Q5 2N2907
Q121 2N3055
R26 100
R27 470
R28 4.7K
C5 .0022 250V
Q117 2N3055
R30 1K
Q6 2N1711
Q7 2N1711
R32 120K
R29 6.02K WW
R31 8.2K
R116 2.5K
R33 1K
C8 150 25V
CR8 A15A
C9 .01 250V
R34 1K
VR4 1N756A
Q11 2N2907
R38 3.3K
R37 100
R35 680
R36 500 VA
R39 270
Q119 S1463
C10 3.3 15V
E4
E5
E6
E7
E8
E9
E14
E15
E16
E24
E26
+15.6V 2.25A ORN
E102
P15
GND
E11
E12
E101
0
BLK
E103
-15.5V 2.25A GRN
W15
CR11 A15A
R40 100
Q12 2N1711
R41 10K CL
E18
E17
R42 1K
Q14 2N1711
R44 1.5K
R45 8.2K
C11 .01 250V
R46 82Ω
Q15 2N1711
R52 12K
Q101 – Q115
R101 100
R102 – R115
E19
E104
PL
+5.25V 50A RED
P5
R118 1K +5VA
E20
C12 .01 250V
CR9 1N645
CR10 1N645
VR6 1N748A
CR105 1N1184
E21
R43 1K
R43 39K
VR7 1N748A
R50 2.7K 2N1711
VR5 1N821
Q16 2N1711
Q17
R51 2.7K
R53 1.2K
C107 9200 15V
R55 270 (FILM)
R56 1.5K (FILM)
R57 390
R58 56Ω
Q18 2N2907
R61 1K
R59 250
R60 470
Q118 2N682
E22
E23
C13 3.3 15V
ELK
CR101 1N1184
CR102 1N1184
CR103 1N1184
CR104 1N1184
C101 90,000 20V
C102 62,000 20V
C103 90,000 20V
C104 62,000 20V
R119 100Ω 2W
5
6
7

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED
A		R43 was 27K · R54 was [illegible], R23 was 1K removed res. added primary transformer, added K1 & fill in all values for R's	7-20-72	
B		ADDED NOTE '3", CHANGED OUTPUT, R119 WAS 27@2W. REVISED R16-R63	8-22-72	Gill
C		Q101 – Q117 WERE G12CS	8/29/72	
D		DELETED R63 FROM NOTES. ECN 2228 MA	3/21/73	
E		REVISED E101 - E104 MA	3/29/73	
F		CHG TO SPS1504A & REVISED TB-101 MA	4/10/73	
G		CHG C5&C15 WAS 200V MA	9/28/73	

REV.

REVISIONS					
CHANGED: REFLECTED REVISIONS D, E, F & G. ADDED: SHEET 2					
DB		3213-07	EBC	5-17-73	R02

NOTES:
1. UNLESS OTHERWISE SPECIFIED;
RESISTOR VALUES ARE IN OHMS, 1/2 WATT, 10%.
CAPACITOR VALUES ARE IN MICROFARADS.

2. R102 THRU R115 ARE 0.1 Ω 5W
Q101 THRU Q117 ARE 2N3055

3. R16 SELECT IN TEST

HIGHEST DESIGNATION	DESIGNATIONS NOT USED
C15	C1, C3, C14
C111	
CR11	
CR105	
E28	
Q18	Q4, Q13
Q121	Q120
R63	R19, R54
R118	
VR7	

ITEM	REQD	PART NO.	DESCRIPTION	MATERIAL	SPECIFICATION	VENDOR OR APPD EQUIV

PARTS LIST

NOTICE
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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
FRACTIONS ±
DECIMALS
2 PLACE ±
3 PLACE ±
ANGLES ±
SURFACES √ MICRO INCHES
FINISH
MATERIAL
NEXT ASSEMBLY
MODEL

DR J R Bialeki DATE 1-25-72
CHK 1-20-72
APPD
APPD
INTERDATA APPD
ENG. J.L. Langben DATE 1/26/73

Transistor Devices Inc.
Cedar Knolls, New Jersey

DIAGRAM, SCHEMATIC
SPS-1504-A (20769)

CODE IDENT 09004
SIZE D
34-015R02D08
SCALE ~
SHEET 1 OF 2

INTERDATA

COMPONENT CHART

CKT. REF.	DESCRIPTION	PART NO.	MFR.
C1	CAP. NOT USED		
C2	CAP. .68 @ 63 V	ET680X063A00	MEPCO.
C3	CAP. NOT USED		
C4	CAP. .68 @ 63Vq	ET680X063A00	MEPCO.
C5	CAP. .0022 @ 250V	C280AE/A2K2	QPL.
C6	CAP. 150 @ 25V	76F02KM151	G. E.
C7	CAP. .01 @ 250V	C280AE/A10K	MEPCO.
C8	CAP. 150 @ 25V	76F02KM151	G. E.
C9	CAP. .01 @ 250V	C280AE/A10K	MEPCO.
C10	CAP. 3.3 @ 15V	CSR13D335KM	QPL.
C11	CAP. .01 @ 250V	C280AE/A10K	MEPCO.
C12	CAP. .01 @ 250V	C280AE/A10K	MEPCO.
C13	CAP. 3.3 @ 15V	CSR13D335KM	QPL.
C14	CAP. NOT USED		
C15	CAP. .0022 @ 250V	C280AE/A2K2	QPL.
C101	CAP. 90,000 @ 20V	86F135M1	G. E.
C102	CAP. 60,000 @ 20V	86F134M1	↓
C103	CAP. 90,000 @ 20V	86F135M1	↓
C104	CAP. 60,000 @ 20V	86F134M1	↓
C105	CAP. 7,800 @ 30V	86F148M1	↓
C106	CAP. 7,800 @ 30V	86F148M1	↓
C107	CAP. 9,200 @ 15V	86F120M2	G. E.
C108	CAP. .22 @ 250	CSR13E225KL	JACO.
C109	CAP. .22 @ 250	CSR13E225KL	JACO.
CR1	DIODE	1N645	G. E.
CR2	DIODE	A-15-A	↓
CR3	DIODE	A-15-A	↓
CR4	DIODE	1N645	↓
CR5	DIODE	A-15-A	↓
CR6	DIODE	A-15-A	↓
CR7	DIODE	A-15-A	↓
CR8	DIODE	A-15-A	↓
CR9	DIODE	1N645	↓
CR10	DIODE	1N645	↓
CR11	DIODE	A-15-A	G. E.
CR101	DIODE	1N1184	G. E.
CR102	DIODE	1N1184	↓
CR103	DIODE	1N1184	↓
CR104	DIODE	1N1184	↓
CR105	DIODE	1N1184	G. E.
F1	FUSE 15A S. B.	MDX - 15	BUSSMAN
XF1	FUSE HOLDER	342002	BUSSMAN
Q1	TRANSISTOR	2N1711	QPL.
Q2	TRANSISTOR	2N3055	RCA
Q3	TRANSISTOR	2N1711	QPL.
Q4	TRANSISTOR	NOT USED	↓
Q5	TRANSISTOR	2N2907	↓
Q6	TRANSISTOR	2N1711	↓
Q7	TRANSISTOR	↓	↓
Q8	TRANSISTOR	↓	↓
Q9	TRANSISTOR	2N1711	↓
Q10	TRANSISTOR	2N2907	↓
Q11	TRANSISTOR	2N2907	↓
Q12	TRANSISTOR	2N1711	↓
Q13	TRANSISTOR	NOT USED	↓
Q14	TRANSISTOR	2N1711	↓
Q15	TRANSISTOR	2N1711	↓
Q16	TRANSISTOR	2N1711	↓
Q17	TRANSISTOR	2N1711	↓
Q18	TRANSISTOR	2N2907	QPL.
Q101	TRANSISTOR	2N3055	RCA
Q102	↓	↓	↓
Q103	↓	↓	↓
Q104	↓	↓	↓
Q105	↓	↓	↓
Q106	↓	↓	↓
Q107	↓	↓	↓
Q108	↓	↓	↓
Q109	↓	↓	↓
Q110	↓	↓	↓
Q111	↓	↓	↓
Q112	↓	↓	↓
Q113	↓	↓	↓
Q114	↓	↓	↓
Q115	↓	↓	↓
Q116	↓	↓	↓
Q117	TRANSISTOR	2N3055	↓
Q118	SCR	2N682	↓
Q119	SCR	61463	↓
Q120	NOT USED		↓
Q121	TRANSISTOR	2N3055	RCA
R1	RESISTOR 100	RCR20G101KS	ALLEN-BRADLEY
R2	RESISTOR 1.8K, 2W	RC40G182K	↓
R3	RESISTOR 270	RCR20G271KS	↓
R4	RESISTOR 1K	RCR20G102KS	↓
R5	RESISTOR 100	RCR20G101KS	ALLEN-BRADLEY
R6	RESISTOR .33 ohms, 5W	PW5	HAMILTON-HALL
R7	POT 10K	BK64204	
R8	RESISTOR 82K	RCR20G823KS	ALLEN-BRADLEY
R9	POT 250 ohms	BK64199	
R10	RESISTOR 100 1 W	RC32G101KS	ALLEN-BRADLEY
R11	RESISTOR 270 1 W	RC32G271KS	ALLEN-BRADLEY
R12	RESISTOR 15 K	RCR20G153KS	ALLEN-BRADLEY
R13	RESISTOR 2.2K FILM		
R14	RESISTOR 820	RCR20G821KS	ALLEN-BRADLEY
R15	RESISTOR 1 K	RCR20G102KS	ALLEN-BRADLEY
R16	RESISTOR 100 K	RCR20G104KS	ALLEN-BRADLEY
R17	RESISTOR 8.2K	RCR20G822KS	ALLEN-BRADLEY
R18	RESISTOR 2.7 K	RCR20G272KS	ALLEN-BRADLEY
R19	RESISTOR NOT USED		
R20	RESISTOR 1 K FILM		
R21	RESISTOR 1.2 K FILM		
R22	RESISTOR 680	RCR20G681KS	ALLEN-BRADLEY
R23	POT 500 ohms	BK64200	
R24	RESISTOR 1 K	RCR20G102KS	ALLEN-BRADLEY
R25	RESISTOR 1 K	RCR20G101KS	ALLEN-BRADLEY
R26	RESISTOR 100	RCR20G101KS	ALLEN-BRADLEY
R27	RESISTOR 470	RCR20G471KS	ALLEN-BRADLEY
R28	RESISTOR 4.7 K	RCR20G472KS	ALLEN-BRADLEY
R29	RESISTOR 4.02K 3W 1%	RW79U4022F	
R30	RESISTOR 1 K	RCR20G102KS	ALLEN-BRADLEY
R31	RESISTOR 8.2 K	RCR20G822KS	ALLEN-BRADLEY
R32	RESISTOR 120 K	RCR20G124KS	ALLEN-BRADLEY
R33	RESISTOR 1 K	RCR20G102KS	ALLEN-BRADLEY
R34	RESISTOR 1 K	RCR20G102KS	ALLEN-BRADLEY
R35	RESISTOR 680	RCR20G631KS	ALLEN-BRADLEY
R36	POT 500 ohms	BK64200	
R37	RESISTOR 100	RCR20G101KS	ALLEN-BRADLEY
R38	RESISTOR 3.3 K	RCR20G332KS	ALLEN-BRADLEY
R39	RESISTOR 270	RCR20G271KS	ALLEN-BRADLEY
R40	RESISTOR 100	RCR20G101KS	ALLEN-BRADLEY
R41	POT 10 K	BK64204	
R42	RESISTOR 1 K	RCR20G102KS	ALLEN-BRADLEY
R43	RESISTOR 39 K	RCR20G393KS	ALLEN-BRADLEY
R44	RESISTOR 1.5 K	RCR20G152KS	ALLEN-BRADLEY
R45	RESISTOR 8.2 K	RCR20G822KS	ALLEN-BRADLEY
R46	RESISTOR 82 ohms	RCR20G820KS	ALLEN-BRADLEY
R47	RESISTOR NOT USED		
R48	RESISTOR 1 K	RCR20G102KS	ALLEN-BRADLEY
R49	RESISTOR NOT USED		
R50	RESISTOR 2.7 K	RCR20G272KS	ALLEN-BRADLEY
R51	RESISTOR 2.7 K	RCR20G272KS	ALLEN-BRADLEY
R52	RESISTOR 12 K	RCR20G123KS	ALLEN-BRADLEY
R53	RESISTOR 1.2 K	RCR20G122KS	ALLEN-BRADLEY
R54	RESISTOR NOT USED		
R55	RESISTOR 270 ohms FILM		
R56	RESISTOR 1.5 K FILM		
R57	RESISTOR 390	RCR20G391KS	ALLEN-BRADLEY
R58	RESISTOR 56	RCR20G560KS	ALLEN-BRADLEY
R59	POT 250 ohms	BK64199	
R60	RESISTOR 470 ohms	RCR20G471KS	ALLEN-BRADLEY
R61	RESISTOR 1 K	RCR20G102KS	ALLEN-BRADLEY
R62	RESISTOR 4.7 K	RCR20G472KS	ALLEN-BRADLEY
R63	RESISTOR 2.7, 2 W	RC42G270KS	ALLEN-BRADLEY
R101	RESISTOR 100 ohms		
R102	RESISTOR .1 ohm, 5 W	PW5	HAMILTON-HALL
R103	↓	↓	↓
R104	↓	↓	↓
R105	↓	↓	↓
R106	↓	↓	↓
R107	↓	↓	↓
R108	↓	↓	↓
R109	↓	↓	↓
R110	↓	↓	↓
R111	↓	↓	↓
R112	↓	↓	↓
R113	↓	↓	↓
R114	↓	↓	↓
R115	RESISTOR .1 ohm, 5 W	PW5	HAMILTON-HALL
R116	POT 2.5 K	R1506	TDI
R117	POT 1 K	R1404	TDI
R118	POT 1 K	R1404	TDI
R119	RESISTOR 100 ohms, 2 W 10%	RCH2G101K	
VR1	ZENER DIODE	1N756A	QPL.
VR2	↓	1N821	↓
VR3	↓	1N756A	↓
VR4	↓	1N756A	↓
VR5	↓	1N821	↓
VR6	↓	1N748A	↓
VR7	ZENER DIODE	1N748A	QPL.
T101	TRANSFORMER	C20201E-T5	TDI
T102	RELAY TRANSFORMER	B20815	TDI
B1	BLOWER	CENTAUR CT3AZ	ROTRON
F61	AC LINE FILTER	2031	COMPONENTS CORP.
K1	RELAY	W88AX-6DPDT	MAGNACRAFT
TB1	TERMINAL STRIP	863	H. H. SMITH
RC1	RC NETWORK	PMR2026	RIFA
	LINE CORD	174085 TYPE SJ	BELDEN

NOTES

NAME D. BARKER

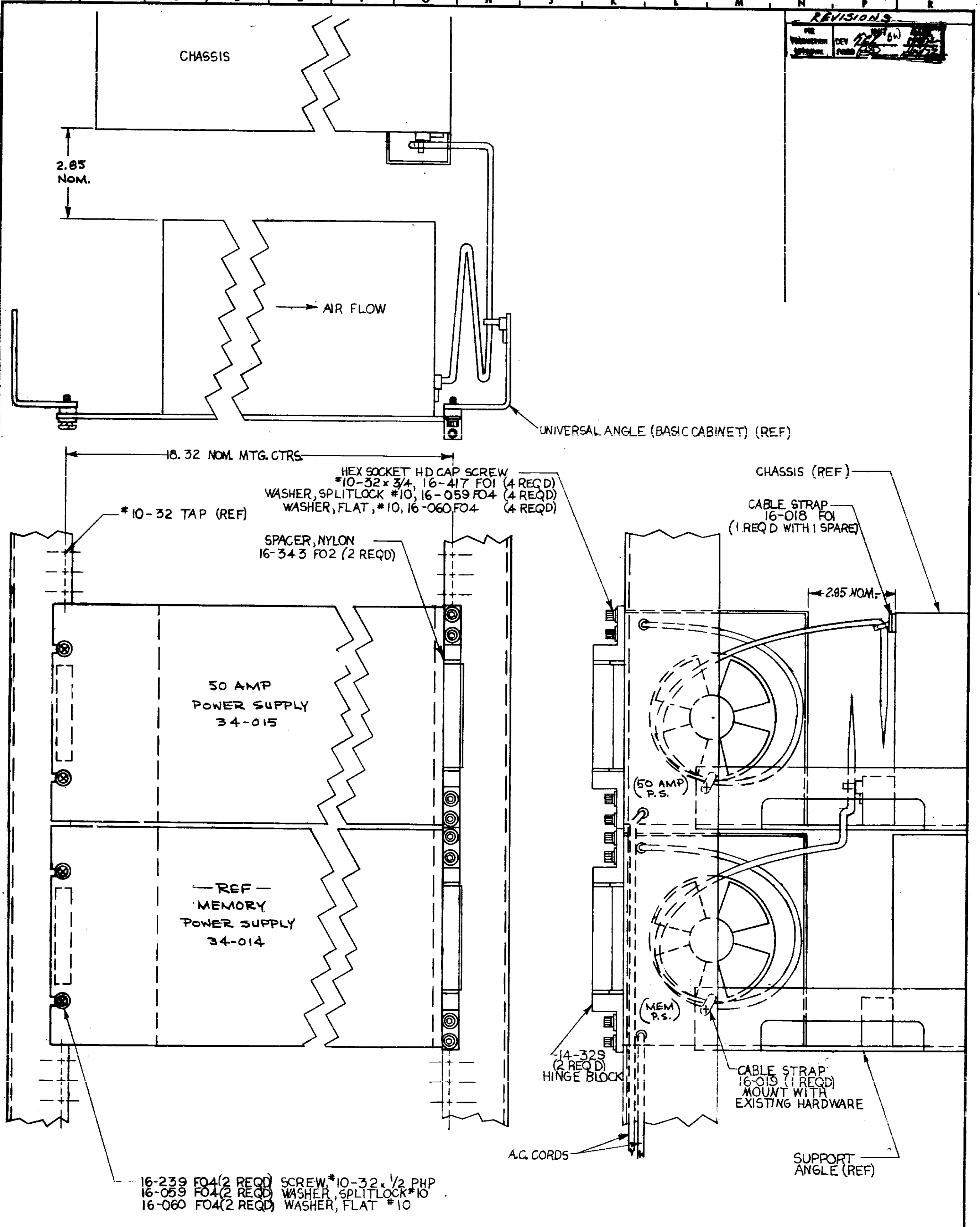
DRAFT 5-17-73

TITLE FUNCTIONAL SCHEMATIC SPS-1504-A

34-015R02D08

SHEET 2 OF 2

BRUNING 44 231 16042


INTERDATA
REVISIONS
CHASSIS
2.85 NOM.
AIR FLOW
UNIVERSAL ANGLE (BASIC CABINET) (REF)
18.32 NOM. MTG. CTRS.
HEX SOCKET HD CAP SCREW
*10-32 x 3/4, 16-417 F01 (4 REQD)
WASHER, SPLITLOCK #10, 16-059 F04 (4 REQD)
WASHER, FLAT, #10, 16-060 F04 (4 REQD)
*10-32 TAP (REF)
SPACER, NYLON
16-343 F02 (2 REQD)
50 AMP
POWER SUPPLY
34-015
— REF —
MEMORY
POWER SUPPLY
34-014
CHASSIS (REF)
CABLE STRAP
16-018 F01
(1 REQ D WITH 1 SPARE)
2.85 NOM.
(50 AMP P.S.)
(MEM P.S.)
14-329
(2 REQ D)
HINGE BLOCK
CABLE STRAP
16-019 (1 REQD)
MOUNT WITH
EXISTING HARDWARE
A.C. CORDS
SUPPORT
ANGLE (REF)
16-239 F04(2 REQD) SCREW, #10-32 x 1/2 PHP
16-059 F04(2 REQD) WASHER, SPLITLOCK #10
16-060 F04(2 REQD) WASHER, FLAT #10

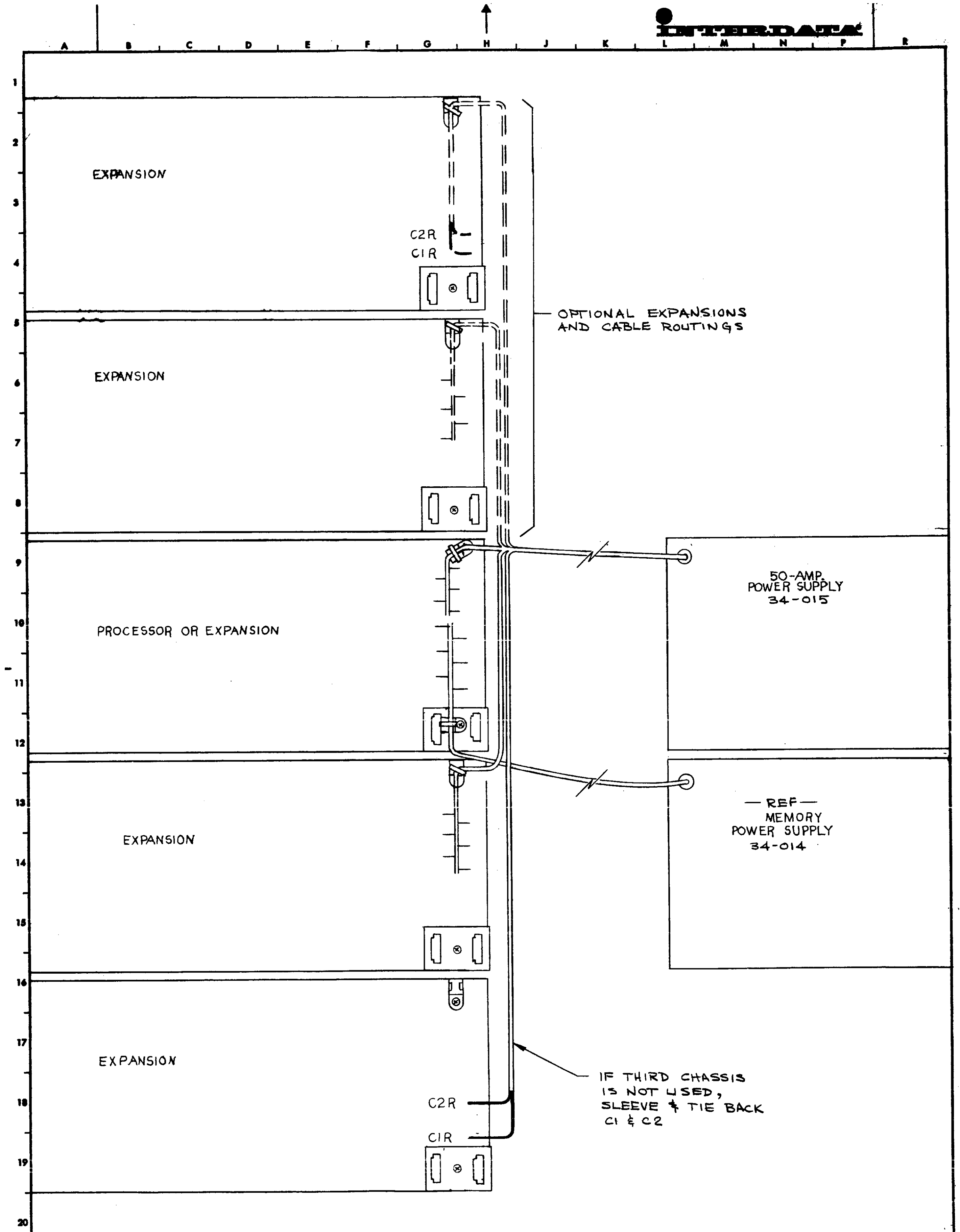
SCALE - NONE

NOTES
1. ALL HARDWARE REQUIREMENTS ARE ON A ONE UNIT BASIS ONLY.

NAME	TITLE	DATE
L. TOWNSEND	DRAFT	5-18-72
J.F. FLEMING	CHK	6-5-72
T. LAUGESEN	ENGR	
H. ROSS	Q.C.	
R.E. JONES	DIR. DEV.	

TITLE INFORMATION DRAWING
POWER SUPPLY
CABINET INSTALLATION

TASK NO. 03213
DWG. NO. 02-261 C12
SHEET 1 OF 2


EXPANSION
C2R
C1R
OPTIONAL EXPANSIONS AND CABLE ROUTINGS
EXPANSION
PROCESSOR OR EXPANSION
50-AMP. POWER SUPPLY 34-015
— REF — MEMORY POWER SUPPLY 34-014
EXPANSION
EXPANSION
IF THIRD CHASSIS IS NOT USED, SLEEVE & TIE BACK C1 & C2
C2R
C1R

SCALE – HALF SIZE

NOTES

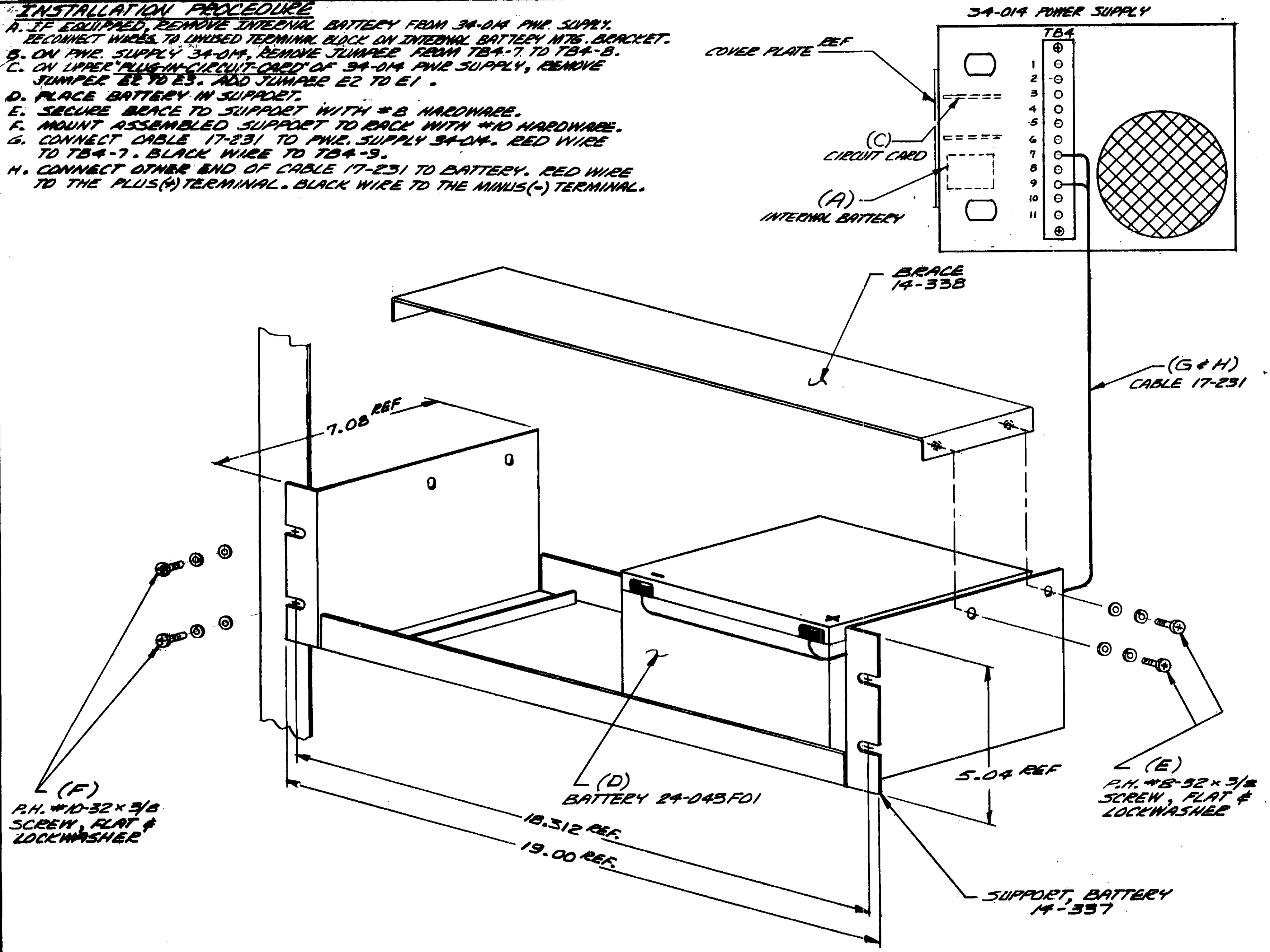
NAME	TITLE	DATE
L. TOWNSEND	DRAFT	5-19-72

TITLE INFORMATION DRAWING
POWER SUPPLY
CABINET INSTALLATION

TASK NO. 03213
DWG. NO. 02-261 C12
SHEET OF 2-2

INSTALLATION PROCEDURE

A. IF EQUIPPED, REMOVE INTERNAL BATTERY FROM 34-014 PWR. SUPPLY. RECONNECT WIRES TO UNUSED TERMINAL BLOCK ON INTERNAL BATTERY MTG. BRACKET.
B. ON PWR. SUPPLY 34-014, REMOVE JUMPER FROM TB4-7 TO TB4-8.
C. ON UPPER "PLUG-IN-CIRCUIT-CARD" OF 34-014 PWR SUPPLY, REMOVE JUMPER E2 TO E3. ADD JUMPER E2 TO E1.
D. PLACE BATTERY IN SUPPORT.
E. SECURE BRACE TO SUPPORT WITH #8 HARDWARE.
F. MOUNT ASSEMBLED SUPPORT TO RACK WITH #10 HARDWARE.
G. CONNECT CABLE 17-231 TO PWR. SUPPLY 34-014. RED WIRE TO TB4-7. BLACK WIRE TO TB4-9.
H. CONNECT OTHER END OF CABLE 17-231 TO BATTERY. RED WIRE TO THE PLUS(+) TERMINAL. BLACK WIRE TO THE MINUS(-) TERMINAL.


34-014 POWER SUPPLY
TB4
1
2
3
4
5
6
7
8
9
10
11
COVER PLATE REF
(C) CIRCUIT CARD
(A) INTERNAL BATTERY
BRACE 14-338
(G & H) CABLE 17-231
7.08 REF
(D) BATTERY 24-043F01
5.04 REF
18.312 REF.
19.00 REF.
(E) P.H. #8-32 × 3/8 SCREW, FLAT & LOCKWASHER
(F) P.H. #10-32 × 3/8 SCREW, FLAT & LOCKWASHER
SUPPORT, BATTERY 14-337
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
A
B
C
D
E
F
G
H
J
K
L
M
N
P
R

NAME	TITLE	DATE
V. PEGRI	DFT	3 MAY 73
H. MATTIE	CHK	3 MAY 73
G. WEEKLY	ENG	
H. ROSS	Q.C.	
R.E. JONES	PR. ENG	

PRODUCTION APPROVAL	QUANT.	DATE
DEV	3	3 MAY 73
PROD.	C.A.	3 MAY 73

TITLE INSTALLATION DWG MOD 80 EXTERNAL BATTERY KIT

TAB. 03213
DWG NO. 39-019 C20
SHEET 1 OF 1

INTERDATA

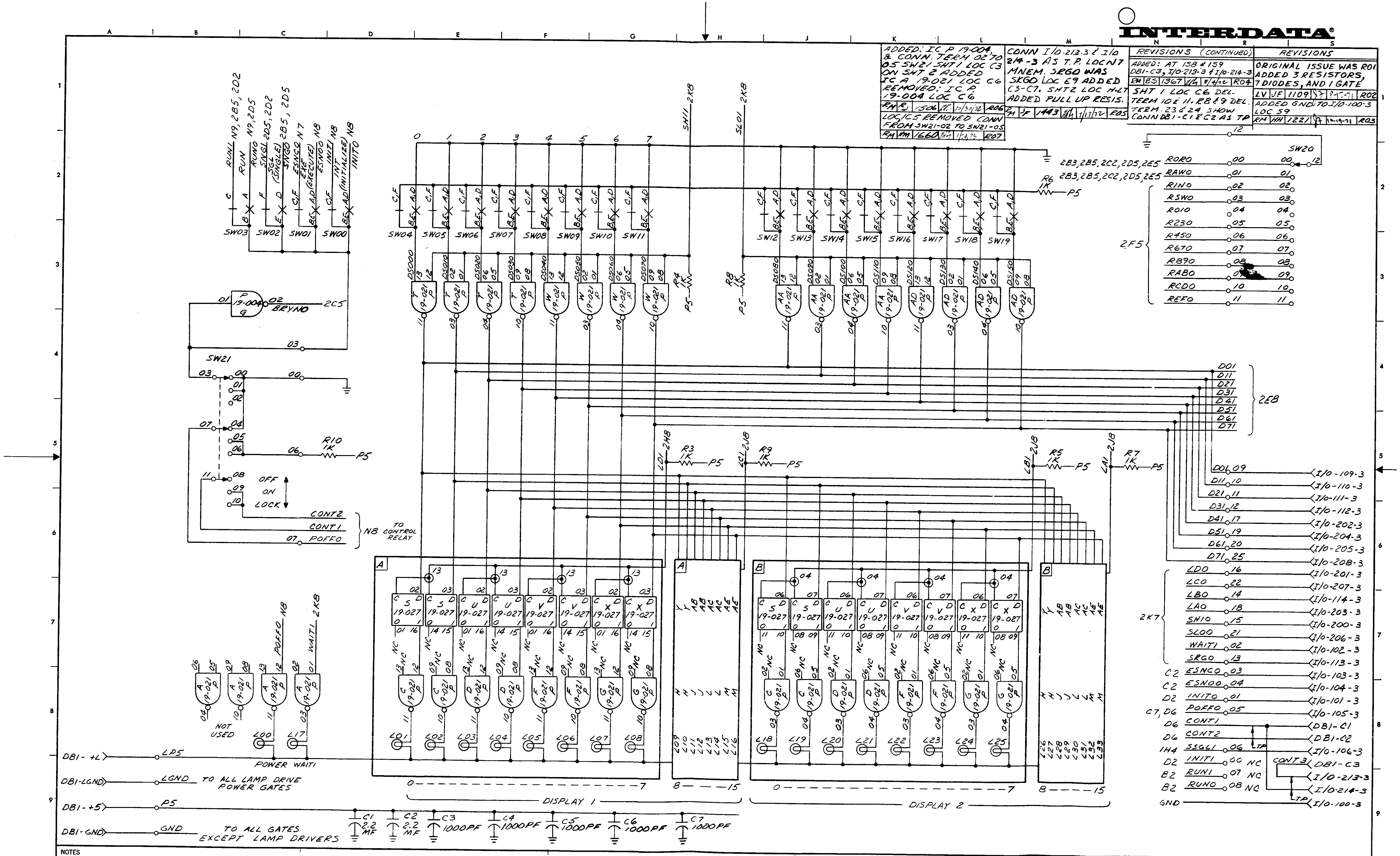
INTERDATA®

REVISIONS					
ORIGINAL ISSUE WAS R01 ADDED 3 RESISTORS, 7 DIODES, AND 1 GATE					
LV	JF	1109		8-13-71	R02
ADDED GND TO I/O-100-3 LOC S9					
RM	HH	1221		10-19-71	R03

REVISIONS (CONTINUED)					
ADDED: AT 158 & 159 DB1-C3, I/O-213-3 & I/O-214-3					
RM	BS	1367		1/4/72	R04
SHT 1 LOC C6 DEL. TERM 10 & 11. R8 & 9 DEL. TERM. 23 & 24 SHOW CONN DB1-C1 & C2 AS TP					

CONN I/O-213-3 & I/O 214-3 AS T.P. LOC N7 MNEM. SRGO WAS SKGO LOC E9 ADDED C3-C7. SHT 2 LOC H-L7 ADDED PULL UP RESIS.					
RM	JF	1443		1/17/72	R05

ADDED: IC P 19-004, & CONN. TERM 02 TO 05 SW21 SHT 1 LOC C3 ON SHT 2 ADDED IC A 19-021 LOC C6 REMOVED: IC P 19-004 LOC C6					
RM	RJ	1506		10/30/72	R06
LOGIC 5 REMOVED CONN FROM SW21-02 TO SW21-05					
RM	HM	1660		1/31/73	R07


RUN1 N9, 2B5, 2D2
RUN N9, 2D5
RUN0 2D5, 2D2
SGL (SINGLE) 2B5, 2D5
SRGO N7
EXE (EXECUTE) N8
ESNC0 N8
INT (INITIALIZE) N8
INIT0 N8
SW03
SW02
SW01
SW00
SW04
SW05
SW06
SW07
SW08
SW09
SW10
SW11
SW12
SW13
SW14
SW15
SW16
SW17
SW18
SW19
SW20
SW21
SH11 2K8
SL01 2K8
P 19-004
BRYNO
2C5
R10 1K
P5
OFF
ON
LOCK
CONT2
CONT1
POFFO
N8 TO CONTROL RELAY
DS000
DS010
DS020
DS030
DS040
DS050
DS060
DS070
DS080
DS090
DS100
DS110
DS120
DS130
DS140
DS150
19-021
R4 1K
R8 1K
R6 1K
2B3, 2B5, 2C2, 2D5, 2E5
R0R0
RAW0
RIN0
RSW0
R010
R230
R450
R670
R890
RAB0
RCD0
REF0
2F5
D01
D11
D21
D31
D41
D51
D61
D71
2E8
LD1 2H8
R3 1K
LC1 2J8
R9 1K
LB1 2J8
R5 1K
LA1 2J8
R7 1K
I/O-109-3
I/O-110-3
I/O-111-3
I/O-112-3
I/O-202-3
I/O-204-3
I/O-205-3
I/O-208-3
I/O-201-3
I/O-207-3
I/O-114-3
I/O-203-3
I/O-200-3
I/O-206-3
I/O-102-3
I/O-113-3
I/O-103-3
I/O-104-3
I/O-101-3
I/O-105-3
DB1-C1
DB1-C2
I/O-106-3
DB1-C3
I/O-213-3
I/O-214-3
I/O-100-3
LD0
LC0
LB0
LA0
SH10
SL00
WAIT1
SRGO
ESNC0
ESN00
INIT0
POFFO
CONT1
CONT2
SSGL1
INIT1
RUN1
RUN0
GND
2K7
TP
CONT3
NC
19-027
A
B
NOT USED
POWER WAIT1
L00
L17
L01
L02
L03
L04
L05
L06
L07
L08
L18
L19
L20
L21
L22
L23
L24
L25
DB1- +L
LPS
DB1-LGND
LGND TO ALL LAMP DRIVE POWER GATES
DB1- +5
P5
DB1-GND
GND TO ALL GATES EXCEPT LAMP DRIVERS
C1 2.2 MF
C2 2.2 MF
C3 1000PF
C4 1000PF
C5 1000PF
C6 1000PF
C7 1000PF
0 - - - - - 7
8 - - - 15
DISPLAY 1
DISPLAY 2
NOTES

NAME	TITLE	DATE
H TERHUNE	DRAFT	10 AUG 71
R F JERO	CHK	10 AUG 71
B.W. SATHMARY	ENGR	2 JUNE 71
M. FUCHS	Q C	2 JUNE 71
R.E. JONES	DIR ENG	2 JUNE 71

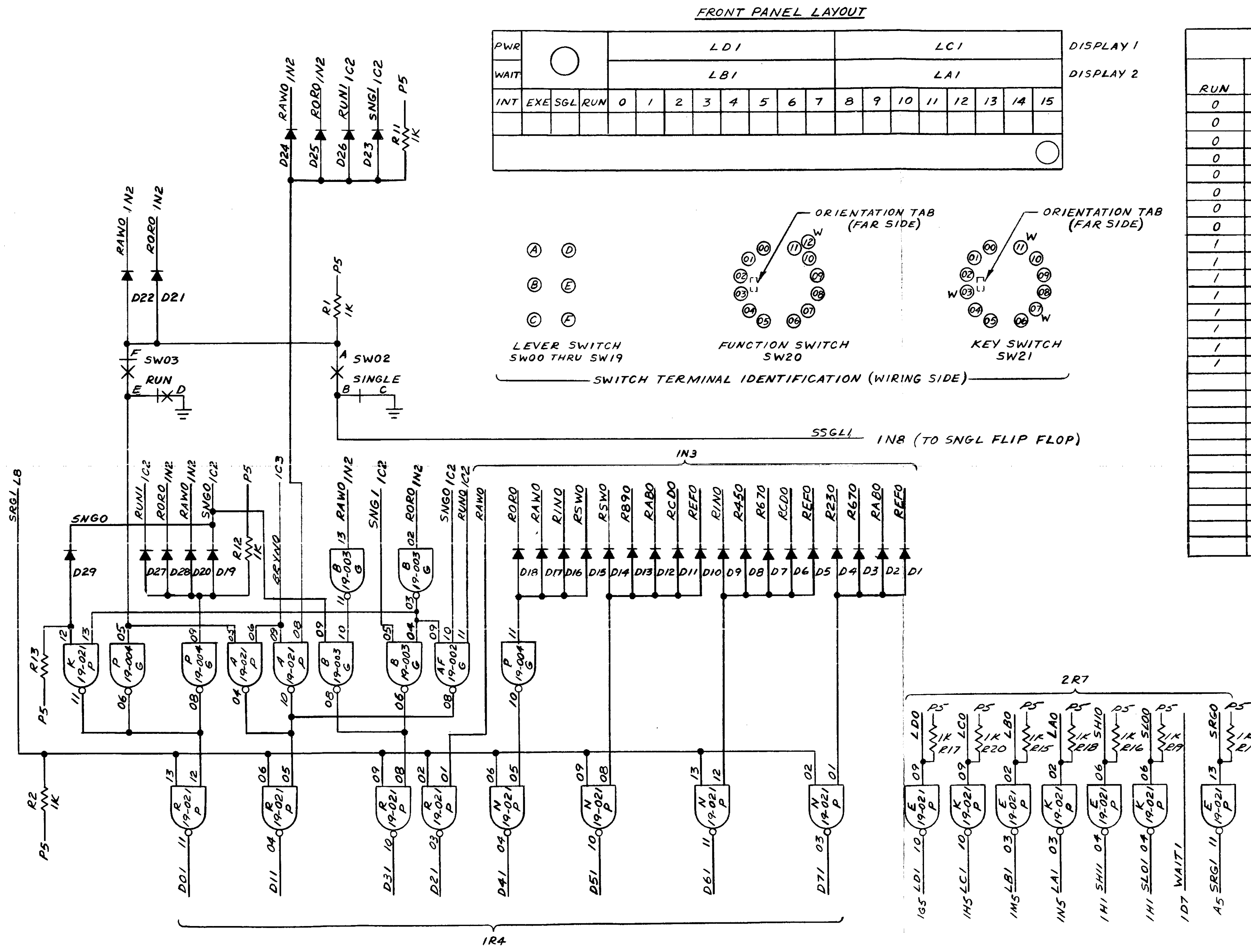
TITLE SCHEMATIC DISPLAY PANEL (NS1)

TASK NO. 03116

DWG NO. 09-051R07D08

SHEET 1 OF 2

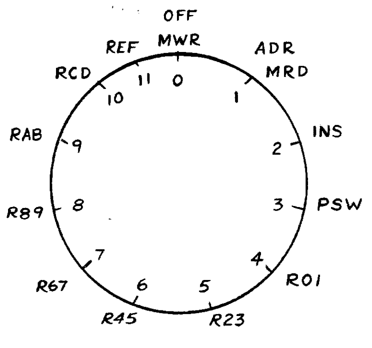
INTERDATA®


RAWO IN2
RORO IN2
RUNI IC2
SNGI IC2
P5
R11 1K
D24
D25
D26
D23
RAWO IN2
RORO IN2
D22
D21
R1 1K
P5
SW03
RUN
SW02
SINGLE
SSGLI
IN8 (TO SNGL FLIP FLOP)
SRGI LB
SNGO
D29
RUNI IC2
RORO IN2
RAWO IN2
SNGO IC2
P5
IC3
D27
D28
D20
D19
R12 1K
RAWO IN2
SNGI IC2
RORO IN2
SNGO IC2
RUNO IC2
RAWO
IN3
RORO
RAWO
RINO
RSWO
RSWO
R890
RABO
RCDO
REFO
RINO
R450
R670
RCDO
REFO
R230
R670
RABO
REFO
D18
D17
D16
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
R13
P5
R2 1K
P5
D01
D11
D31
D21
D41
D51
D61
D71
IR4
2R7
LDO
LCO
LBO
LAO
SHIO
SLOO
SRGO
R17
R20
R15
R18
R16
R19
R14
LDI
LCI
LBI
LAI
SHII
SLOI
WAITI
SRGI
IG5
IH5
IM5
IN5
IH1
IH1
ID7
A5

FRONT PANEL LAYOUT

PWR
WAIT
LDI
LCI
DISPLAY 1
LBI
LAI
DISPLAY 2
INT
EXE
SGL
RUN
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
ORIENTATION TAB (FAR SIDE)
ORIENTATION TAB (FAR SIDE)
A
B
C
D
E
F
LEVER SWITCH
SW00 THRU SW19
FUNCTION SWITCH
SW20
KEY SWITCH
SW21
SWITCH TERMINAL IDENTIFICATION (WIRING SIDE)

STATUS												
RUN	OFF WRT RORO	ADRS RD RAWO	SINGLE	MODE	0	1	2	3	4	5	6	7
0	0	0	0	HALT	1	1	0	0	X	X	X	X
0	0	0	1	HALT	1	1	0	0	X	X	X	X
0	0	1	0	ADR	0	0	1	1	0	0	0	0
0	0	1	1	MRD	0	0	1	0	0	0	0	0
0	1	0	0	HALT	1	1	0	0	0	0	0	0
0	1	0	1	MWR	0	0	0	1	0	0	0	0
0	1	1	0									
0	1	1	1									
1	0	0	0	RUN	1	0	0	0	X	X	X	X
1	0	0	1	VAR	0	1	0	0	X	X	X	X
1	0	1	0	ADR	0	0	1	1	0	0	0	0
1	0	1	1	MRD	0	0	1	0	0	0	0	0
1	1	0	0	RUN	1	0	0	0	0	0	0	0
1	1	0	1	MWR	0	0	0	1	0	0	0	0
1	1	1	0									
1	1	1	1									
				OFF					0	0	0	0
				INS					0	0	1	0
				PSW					0	1	0	0
				0/1					1	0	0	0
				2/3					1	0	0	1
				4/5					1	0	1	0
				6/7					1	0	1	1
				8/9					1	1	0	0
				A/B					1	1	0	1
				C/D					1	1	1	0
				E/F					1	1	1	1


OFF
MWR
ADR
MRD
INS
PSW
R01
R23
R45
R67
R89
RAB
RCD
REF
0
1
2
3
4
5
6
7
8
9
10
11

FRONT VIEW ROTARY

NOTES

NAME	TITLE	DATE
L. VALENTY	DRAFT	28JUL71
	CHK	
	ENGR	
	DIR ENG	

TITLE SCHEMATIC
DISPLAY PANEL
(NS1)
TASK NO. 03116
DWG NO. 09-051R07D08
SHEET OF 2-2

BRUNING 44-231 15043

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