Publication Number 29-470R03

M71-SERIES
MODEL 6/16
MAINTENANCE MANUAL

CONSISTS OF:

M71-Series Model 6/16 Processor General Description	29-470A12
M71-Series Model 6/16 Processor Installation Specification	01-094A20
M71-Series Model 6/16 Processor Maintenance Specification	01-094A21
M71-094 Multiply/Divide Card Information Specification	02-403A12
Selector Channel Installation Specification	02-232M01R03A20
Selector Channel Maintenance Specification	02-232M01R01A21
Test and Information Specification	02-276R02A12
Hexadecimal Display Information Specification	09-065R01A12
Model 6/16 Micro-Program Listing	05-061R01A13
Model 6/16 DROM Listing without MPY-DIV	05-062F01A13
Model 6/16 DROM Listing with MPY-DIV	05-062F02A13
Parity Option Board Schematic Drawing	02-368C08
Hexadecimal Display Panel Schematic Drawing	09-065R01D08
Functional Schematic Drawing	02-232M01R04D08
Functional Schematic Drawing	35-448C08
Functional Schematic Drawing	01-094R02D08
Functional Schematic Drawing	02-403R01D08
Functional Schematic Drawing	02-405R02D08
Assembly Drawing	35-391M02R03E03
Assembly Drawing	35-605D03
Assembly Drawing	35-604R04E03
Assembly Drawing	35-601R01D03
Assembly Drawing	35-602R01D03
Assembly Drawing	35-603R02D03
Memory Adapter Schematic	35-608R01D08
Memory Adapter Component Locator	35-608R01C03

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INTERDATA®

Subsidiary of PERKIN-ELMER
Oceanport, New Jersey 07757, U.S.A.

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May 1976

MANUAL UPDATE PACKAGE COVER SHEET

THIS PACKAGE UPDATES THE FOLLOWING PUBLICATIONS

PUB. NO.	OLD REV.	NEW REV.	TITLE
29-470	R02	R03	6/16 Maintenance Manual

This revision includes changes reflecting:

ECNs 2839

SCNs

Briefly, the changes are as follows:

This package consists of:
This instruction sheet
New Title page
01-094R02D08 1 and 2, 19
35-604R04E03 Sheet 1 of 1

This change corrects the failure of Q1 in the Initialize circuit which was causing the SCLRO Relay to remain in the initialized state.

PAGE REVISION STATUS SHEET

PUBLICATION NUMBER 29-470

TITLE M71-Series Model 6/16 Maintenance Manual

REVISION R03 DATE 5/76

PAGE	REV.	DATE
29-470 A12 M71-Series Model 6/16 General Description		
1 thru A1-4	R00	10/75
01-094 A20 M71-Series Installation Specification		
1 thru 16	R00	8/75
01-094 A21 M71-Series Model 6/16 Maintenance Specification		
1 thru 36	R00	9/75
02-403 A12 M71-094 Multipy/Divide Card Information Specification		
1 thru A1-2	R00	10/75
02-232 M01 R03 A20 M70-103 NS Selector Channel Installation Specification		
1 thru 4	R03	6/74

PAGE	REV.	DATE
02-232 M01 R01 A21 M70-103 NS Selector Channel Maintenance Specification		
1 thru 10	R01	6/74
02-276 R02 A12 M49-410 Test Aid Information Specification		
1 thru 6	R02	7/74
09-065 R01 A12 M71-102 Hexadecimal Display Information Specification		
1 thru 10	R01	7/74
05-061 R01 A13 Model 6/16 Micro-Program Listing		
1 thru 25	R01	3/76
05-062 F01 A13 Model 6/16 Drom Listing Without Mpy-Div		
1 thru 20	R00	10/75

PAGE	REV.	DATE
05-062 F02 A13 Model 6/16 Drom Listing With Mpy-Div		
1 thru 20	R00	10/75

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS			
PRE PROD. ACTION APPROVAL	INIT DEV	DATE 11/21/75	
SHTS 2,4,5,11,13 & 17 WERE SPEC AS REV LEVEL R00. REV LEVEL OF BOTH BOARDS WERE R00 RESP.			
WP	INIT 02145-3	JB 12-11-75	R01
RELEASED FOR PRODUCTION ENG. [illegible] DATE 12-16-75			
REVISED SHT 19 REV. LEVEL OF BOTH BOARDS WERE R00 RESP.			
WP	VRB 2839	- 5-10-76	R02

LSI MICRO PROCESSOR

S-BUS

I/O BUS

REPEAT COUNTER

DROM1 256x8

DROM2 256x8

RAR

ROM 512 x 32

IMM (16-23)

BRANCH (15-23)

MAR

LOC

MAS

MAIN MEMORY 8KB-64KB

IR OP YD YS

MDR

FLR

PSW CC

JAM

YD

MASK

SHIFTER

GR0 GR1 GR2 GR3 GR4 GR5 GR6 GR7 GR8 GR9 GR10 GR11 GR12 GR13 GR14 GR15

YD

YS

SHIFTER

Q

ALU

MRO

CROSS SHIFTER

B BUS

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION.

6/16 CPU W/O M-D	35-604 F01 R04
6/16 CPU W/M-D	35-604 F02 R04

NOTE:
THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

MODEL 6/16 BLOCK DIAGRAM

SHEET INDEX	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
REV LEVEL	02	01		01	01						01		01				01		01
SHEET NO.																			

NOTE:
ALL COMPONENTS IN THIS SCHEMATIC LOCATED ON 35-604

BRUNING 44-231 24538

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SCALE — TOLERANCES: XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
B. SCHAIBLE	DRAFT	11-4-75
P. CERO	CHK	11-21-75
D. FRANKENBERGER	ENGR	12-16-75
B. MILLER		12-16-75
S. SAMESSIMM	MGR	12-16-75

TITLE FUNCTIONAL SCHEMATIC 6/16 CPU PROCESSOR

TASK NO. 03145

DWG NO. 01-029 R02DOB

SHEET OF 1 — 19

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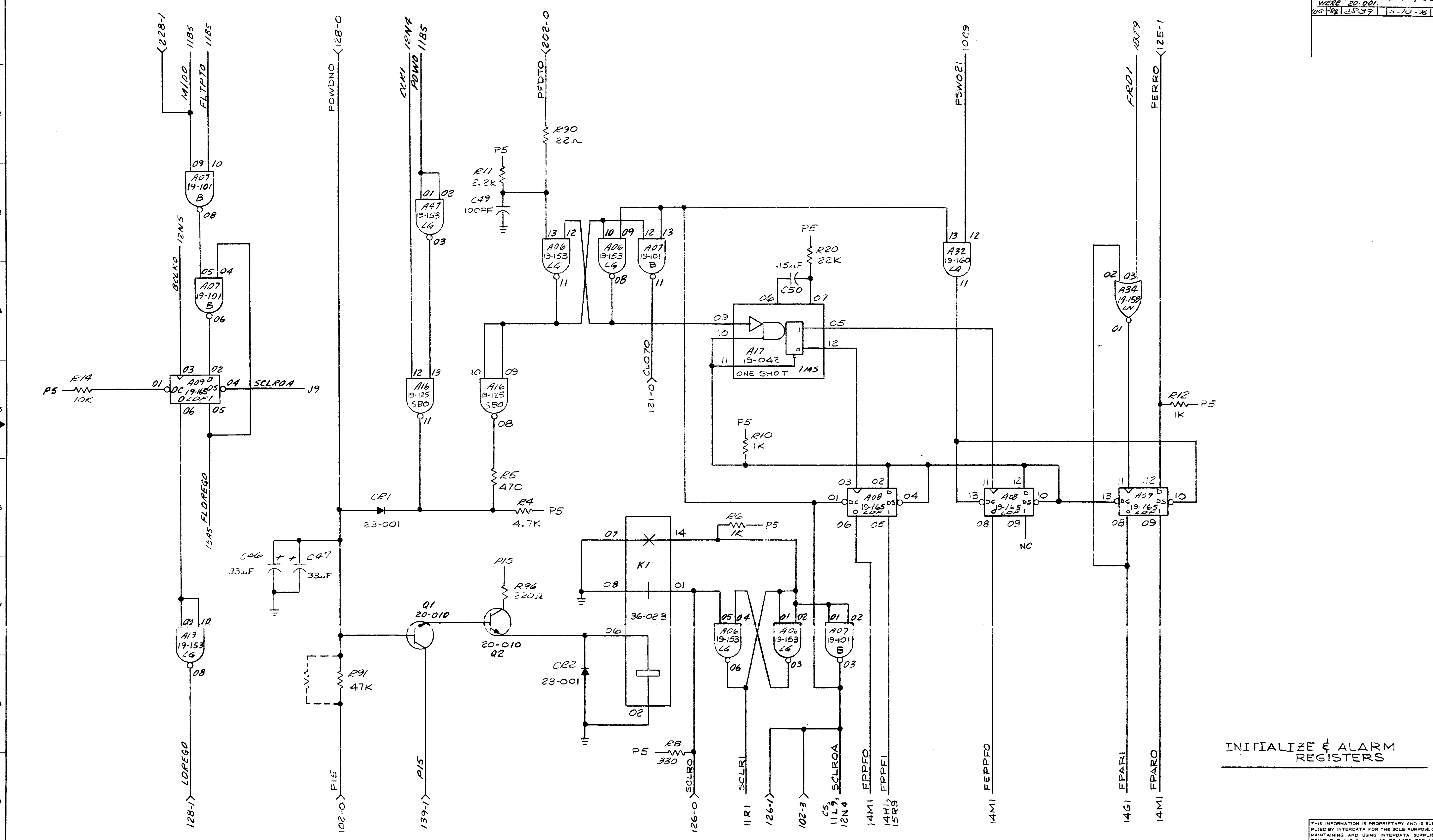
REVISIONS

AREA F7: R96 WAS NOT SPEC'D. COLLECTOR OF Q2 WAS TO P5. Q1 & Q2 WERE 20-001. | 2539 | 5-10-76



INITIALIZE & ALARM REGISTERS

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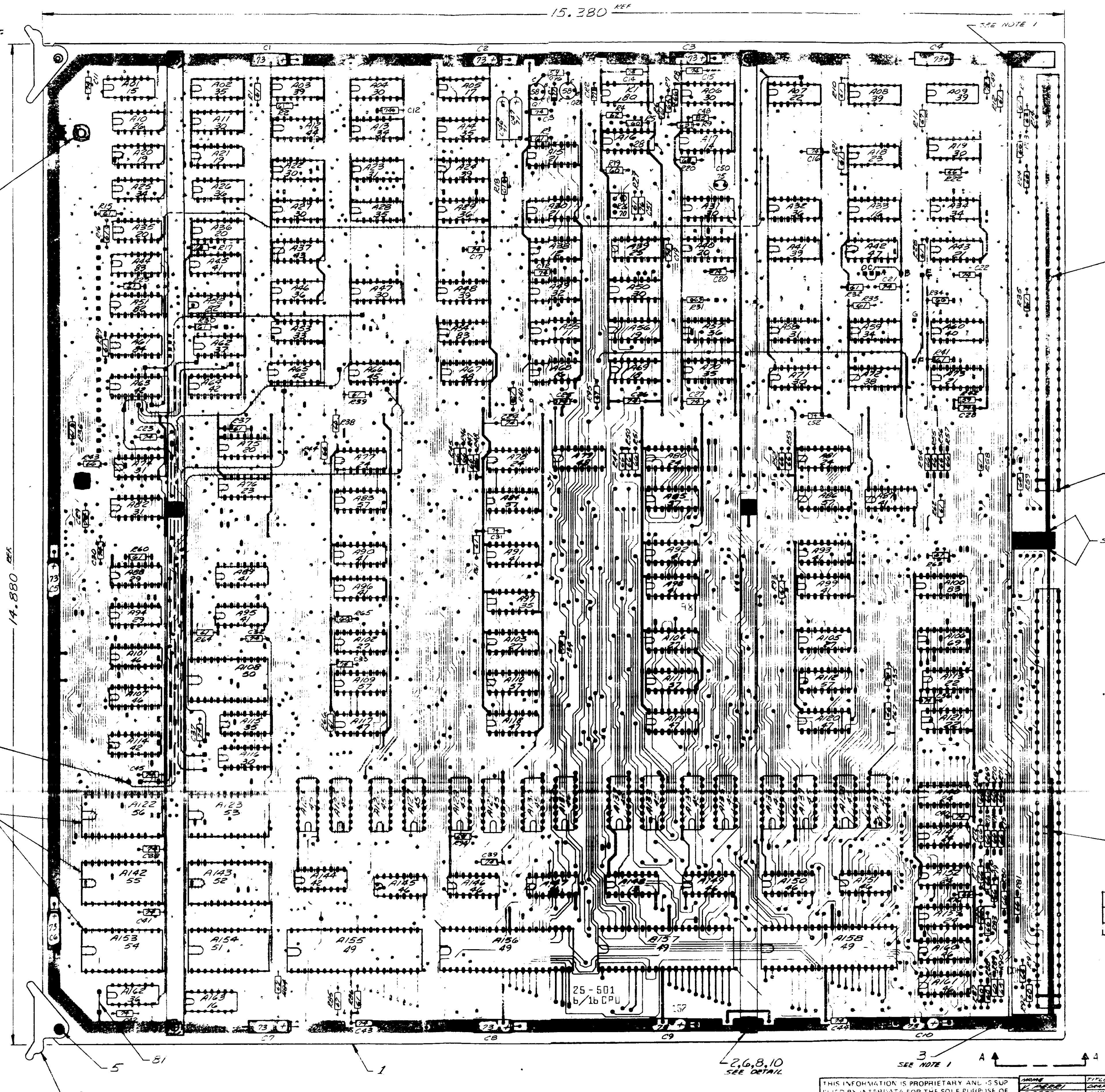
SCALE— | NAME | TITLE | DATE
DRAFT
CHK
ENGR

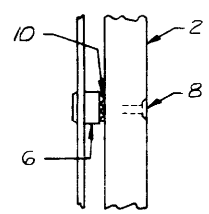
TITLE

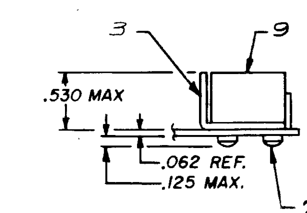
TASK NO. 03145
DWG NO. 01-094R01D08
SHEET 19 OF 19

BRUNING 44-231 24538

NOTES:
1. STIFFENER BAR (ITEM 3) SHALL BE SOLDERED TO GND BUS AT 2 END POINTS & CENTER POINT.
2. CONNECTOR PINS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.
3. NOTE POSITIONS OF I.C. IN LOCATIONS A39 & A33 THEY MUST BE ORIENTED TO THE RIGHT.







PARTIAL VIEW A-A

REVISIONS

PRE PRODUCTION APPROVAL — INIT. / DATE — DEV D.F. 11/21/75 — PROD [illegible] 12/1/75

A16 WAS SPEC AS ITEM # 17.
A97 WAS SPEC AS ITEM # 17.
A116 WAS SPEC AS ITEM # 33.
R95 WAS SPEC AS ITEM 61
C31 C33 C52 & R61 WERE NOT SPEC.

DJR	DP	ECR 03145-3		12-11-75	R01

RELEASED FOR PRODUCTION
MFG. ENG. JMB DATE 12-16-75

AREA A06, C48 ITEM NUMBER WAS 79.

[illegible]	RC	2773	—	3-16-76	R02

REVISED CIRCUITRY TO REFLECT NEW COPPER

WS	[illegible]	2772	—	3-[illegible]	[illegible]

AREA A15: R96 WAS NOT SPEC'D, REVISED CIRCUITRY TO REFLECT NEW COPPER.

WS	JRB	2839	-	5-10-76	R04

35-604 F02	AS SHOWN
35-604 F01	AS SHOWN LESS ITEMS 54,55 & 56
VARIATION	DESCRIPTION

COMPONENT	REF DESIGNATION
I.C.	A01 THRU A163
RESISTOR	R1 THRU R96
CAPACITOR	C1 THRU C52
TRANSISTOR	Q1 & Q2
DIODE	CR1 & CR2
RELAY	K1

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NAME	TITLE	DATE
V. PERRI	DRAFT	11-17-75
R. CERO	CHK	12-16-75
J. LEMAIR	ENGR.	12-16-75
R.A. BARKER	Q.C.	12-16-75
D. FORNKENBERGER	MGR	12-16-75

TITLE: ART. CKT ASSEMBLY 6/16 CPU
03145
35-604 R04F03
SHT OF 1-1

C-01

Publication Number 29-470R02

M71-SERIES
MODEL 6/16
MAINTENANCE MANUAL

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Selector Channel Maintenance Specification	02-232M01R01A21
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Functional Schematic Drawing	02-232M01R04D08
Functional Schematic Drawing	35-448C08
Functional Schematic Drawing	01-094R01D08
Functional Schematic Drawing	02-403R01D08
Functional Schematic Drawing	02-405R02D08
Assembly Drawing	35-391M02R03E03
Assembly Drawing	35-605D03
Assembly Drawing	35-604R02E03
Assembly Drawing	35-601R01D03
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Memory Adapter Schematic	35-608R01D08
Memory Adapter Component Locator	35-608R01C03

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March 1976

M71-SERIES
MODEL 6/16
GENERAL DESCRIPTION

INTRODUCTION

The Model 6/16 combines advanced circuits and packaging designs to give the user a price/performance optimized machine. The Model 6/16 is completely upward compatible with INTERDATA Models 3, 4, 74, 7/16 Basic Processor user instruction, interrupt handling, input-output formats and control sequencing. In addition, many of the powerful features of the INTERDATA Models 5, 70 and 80 are included. Because of this compatibility, the Model 6/16 can use the wide range of existing software and peripheral devices.

The Model 6/16 offers a comprehensive set of 96 instructions making the system both easy to program and efficient to operate. Through multi-function instructions and direct core addressing, coding and debugging time is reduced to a minimum.

Memory is addressable to the eight-bit byte level. Memory is expandable from the basic 8,192 bytes to 65,536 bytes. All memory is directly addressable with the primary instructions, no paging or indirect addressing is required. Sixteen 16-Bit General Registers can be used as Accumulators, fifteen of which can also be used as Index Registers. Register-to-Register instructions permit operations between any of the sixteen General Registers, eliminating redundant loads and stores.

The Model 6/16 also provides a flexible Input/Output system in addition to conventional means of programmed I/O. In the Automatic I/O Service Mode, the Processor acknowledges all I/O interrupts and automatically performs much of the overhead prior to activating the Interrupt Service Routine.

Up to four Direct Memory Access Devices can be added to a Model 6/16 Memory System. This channel operates over the common Memory Bus, on a cycle stealing basis, through a Direct Memory Access Port which is built into the Processor. Two types of Direct Memory Access Channels can be used with the Model 6/16 System: The Selector Channel, which permits direct data transfer between any standard oriented INTERDATA device controller and memory; and the Direct Memory Access Channel custom designed by the user for special applications. In addition, an Instruction Steal DMA is supported which allows high speed burst transfer over the I/O Bus.

SCOPE

This document is intended to enable the digital technician to understand the INTERDATA documentation system. Number Notation, the Part Numbering System, and the Drawing System are described. Illustrations are provided to help understand these systems. Other publications which may be of interest to Model 6/16 users are shown in Table 1.

A cross reference between INTERDATA part numbers and standard industry part numbers for the ICs and transitors found in the Model 6/16 may be found in Appendix 1.

TABLE 1. RELATED PUBLICATIONS

TITLE	PUBLICATION NUMBER
16-Bit Reference Manual	29-398
Model 6/16 Maintenance Manual	29-470
Multiplexor Bus Buffer Instruction Manual	29-267

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BLOCK DIAGRAM

A block diagram of the Model 6/16 is shown in Figure 1. The Model 6/16 is a 16-Bit digital computer.

Part No.	Description	Card File Position
35-604	CPU	7
	MEMORY	6

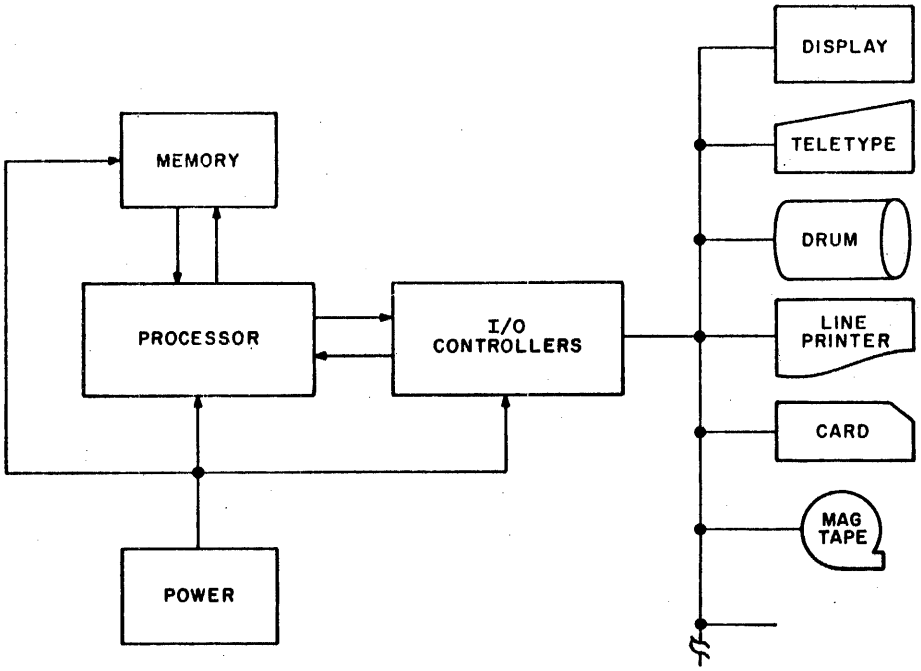

Figure 1. Model 6/16 Simplified Block Diagram

DOCUMENTATION

This section describes the style and conventions used with INTERDATA documentation.

Number Notation

The most common form of number notation used in INTERDATA documentation is hexadecimal notation. In this system, groups of four binary digits are represented by a single hexadecimal digit. Table 2 lists the hexadecimal characters employed.

TABLE 2. HEXADECIMAL NOTATION DATA

Binary	Decimal	Hexadecimal	Binary	Decimal	Hexadecimal	Binary	Decimal	Hexadecimal
0000	0	0	0110	6	6	1100	12	C
0001	1	1	0111	7	7	1101	13	D
0010	2	2	1000	8	8	1110	14	E
0011	3	3	1001	9	9	1111	15	F
0100	4	4	1010	A	A			
0101	5	5	1011	B	B			

To differentiate between decimal and hexadecimal numbers, hexadecimal numbers are preceded by the letter "X", and the number is enclosed in single quotation marks. Examples of hexadecimal numbers are X'1234', X'2EC6', X'A340', X'EEFA', and X'10B9'.

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Part Numbering System

INTERDATA parts, drawings, and publications use a common numbering system. The part number and drawing numbers for drawings which describe the part are related. The publication number is often related to the part number of the device or program described. Figure 2 shows the format used for INTERDATA part numbers. The fields are described in the following paragraphs.

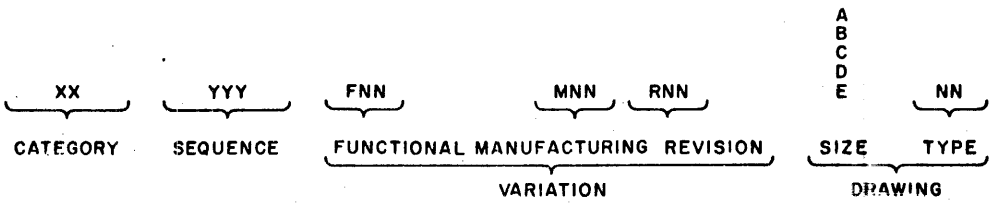

Figure 2. Part Number Format

Category Field

The two-digit Category Number indicates the board class or category to which a part belongs. Typical examples of category number assignments are:

01 – Basic Hardware Systems
02 – Basic Hardware Expansions
03 – Basic Software Systems
04 – Software Packages
05 – Micro-programs
06 – Test Programs
07 – Subroutines of General Utility
10 – Spare Parts Packages
12 – Card File Assemblies
13 – Panels
17 – Wire and Cables
19 – Integrated Circuits
20 – Transistors
27 – Peripheral Equipment
29 – Manuals
34 – Power Supplies
35 – Assembled Printed Circuit Boards
36 – Electro-Mechanical Devices

Sequence Field

The Sequence number identifies a particular item within the category. Sequence numbers are assigned serially, and have no other significance.

NOTE

The Sequence Field, like all other part number fields, may be lengthened as required. The field lengths shown on Figure 2 are minimum lengths (insignificant zeros must be added to maintain these minimums).

Functional Variation Field

The optional Functional Variation Field consists of the letter "F" followed by two digits. The F field is used to distinguish between parts which are not necessarily electrically or mechanically equivalent, but which are described by the same set of drawings. For example, a power supply may be strapped internally to operate on either 110 VAC or 220 VAC. Except for this strap, all power supplies of this type are identical. The strapping option is easily described by a note on the assembly and test specification drawings. Therefore, this is a functional variation.

Manufacturing Variation Field

The optional Manufacturing Variation Field consists of the letter "M" followed by two digits.

The M Field is used to distinguish between parts which are electrically and mechanically equivalent (interchangeable), but which vary in method of manufacture. For example, if leads are welded instead of soldered on an assembly, the M Field changes.

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An important exception to the meaning of the M Field exists for categories related to software. In software, the M Field number, when used, indicates the form in which a particular program is presented. For example, define a program as a set of machine instructions. These same identical instructions may be presented on punched cards, paper tape, or magnetic tape; and for any of these they can be in symbolic form or in relative or absolute binary form. Thus, there are many ways to present the same identical program.

The format for the M Field and its meaning for software is:

Mxy

where x identifies the media selection (i.e., Paper Tape, Magnetic Tape, Cassette, etc.) and y identifies object or source and the format.

Meaning of x		Meaning of y	
Conceptual	0	1	Object program standard format 32-Bit Processor
Paper Tape	1		
Cassette	2	4	Memory image
Magnetic Tape (800 BPI)	3	6	Object Program standard format 16-Bit Processor
Cards	4	7	Object non-standard format
Disc (2.5 MB)	5	8	Object established task
Disc (10 MB)	6	9	Source program
Magnetic Tape (1600 BPI)	7		

These numbers refer to the physical program placed on an approved media for INTERDATA Software. A Paper Tape Object program is standard format and for a 16-Bit Processor has an M16 identifier. A Magnetic Tape Object program is standard format and for a 32-Bit Processor has an M31 identifier.

In addition to the foregoing, there are three unique M numbers which have special meaning:

00	Conceptual Object
91	32 Bit Object Listing
92	Programming Specifications
95	Program Description
96	16 Bit Object Listing
98	Operating Procedures
99	Documentation and Manuals

Revision Field

The optional Revision Field consists of the letter "R" followed by two digits. The R Field is used to indicate minor electrical or mechanical changes to a part which do not change the part's original character. The R field changes often reflect improvements. A part with a revisions level *HIGHER* than the one specified can be used; however, a part with a revision level *LOWER* than specified should not be used.

NOTE

A part number must contain a Category number and a Sequence number. All other fields are optional.

Drawing Field

The optional Drawing Field consists of a letter from "A" to "E" followed by two digits. The letter indicates the size of the original drawing. The sizes for each letter are:

A – 8½" x 11"
B – 11" x 17"
C – 17" x 22"
D – 22" x 34"
E – 34" x 44"

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The two digits indicate the drawing type as follows:

01 – Parts List
02 – Machine Details
03 – Assembly Details
05 – Art Details
06 – Wire Run List
08 – Schematic
09 – Test Specification
10 – Purchase Specification
11 – Bill of Material
12 – Information
13 – Program Listing
14 – Abstracts
15 – Program Description
16 – Operating Instructions
17 – Program Design Specifications
18 – Flow Charts
19 – Product Specification
20 – Installation Specification
21 – Maintenance Specification
22 – Programming Specification
23 – Replaceable Parts List
24 – Application Information
25 – Functional Specifications

Examples

The following list provides some examples of the part numbering system. The numbers were arbitrarily selected, and in most cases are fictitious.

35-060	The 60th printed circuit board assigned a part number under this system.
35-060M01	A printed circuit board electrically and mechanically interchangeable with the 35-060, but differing in method of manufacture.
35-060F01	A printed circuit board not electrically and mechanically interchangeable with the 35-060, but described by the same set of drawings.
35-060-R01	A revised 35-060 printed circuit board which probably supercedes the 35-060.
35-060A01	The 8½ by 11 inch parts list for a 35-060.
35-060B08	The 11 by 17 inch schematic for a 35-060.
06-072	An 8½ by 11 inch listing of the 06-072 program.
06-072A12	An 8½ by 11 inch information drawing on the 06-072 program. Probably a part of the program.
29-060	The 60th manual assigned a number under this system. Note that this number is not referenced in any way to the part number of equipment described in the manual.

Drawing System

This section describes the drawings provided with INTERDATA equipment. Drawings provided with peripheral devices and other purchased items may vary from the system described in this section.

A digital system may be divided into a collection of functionally independent circuits such as Memory, Processor, and I/O Device Controllers. These circuits may or may not be saleable units in their own right, but in the electrical sense they are essentially self contained and capable of performing their function with minimum dependence on other functional circuits in the system. Hence a functional circuit is treated as a building block. Each schematic contains a variety of information including type and location of discreet Integrated Circuits (IC's), pin connections, all interconnections within the schematic, connector pin numbers and connections to other schematics. Further, the schematics are drawn to reflect, in an orderly fashion, all logical operations performed by the circuits. Generally, symbols used on schematics conform to MIL-STD-806B.

Registers are named according to the following rules:

1. The register mnemonic name has a maximum of three letters, excluding "I, O, Q, and Z".
2. Each bit in the register is numbered, usually starting at 00 on the left, or most significant positions, and continuing to N-1 on the right, where N is the number of bits in the register.
3. The 00 bit is the Most Significant Bit and the N-1 is the Least Significant Bit.

The IC's mounted directly on the logic board are represented on the schematic drawings by logic symbols. Each symbol contains the reference designation, device part number (category and sequence), and symbol mnemonic designation. Refer to Figure 3.

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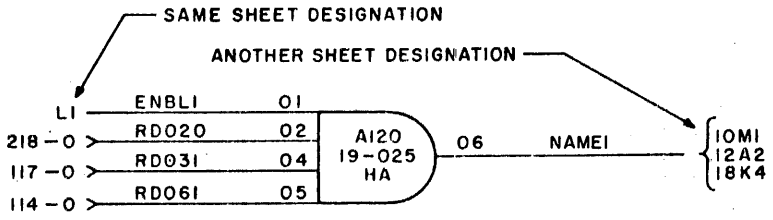

Figure 3. Example of a High Speed AND Gate

The designations, numbers, and references shown in Figure 3 are:

A20 – This shows the components location on the logic board. Figure 4 illustrates the method generally used to determine component location on a logic board. With the logic board oriented so that the header connnectors (Conn 0 and Conn 1) are on the right, the components are numbered from left to right starting in the upper left corner. That is, the first IC in the upper left corner is 01 and the first capacitor is C1.

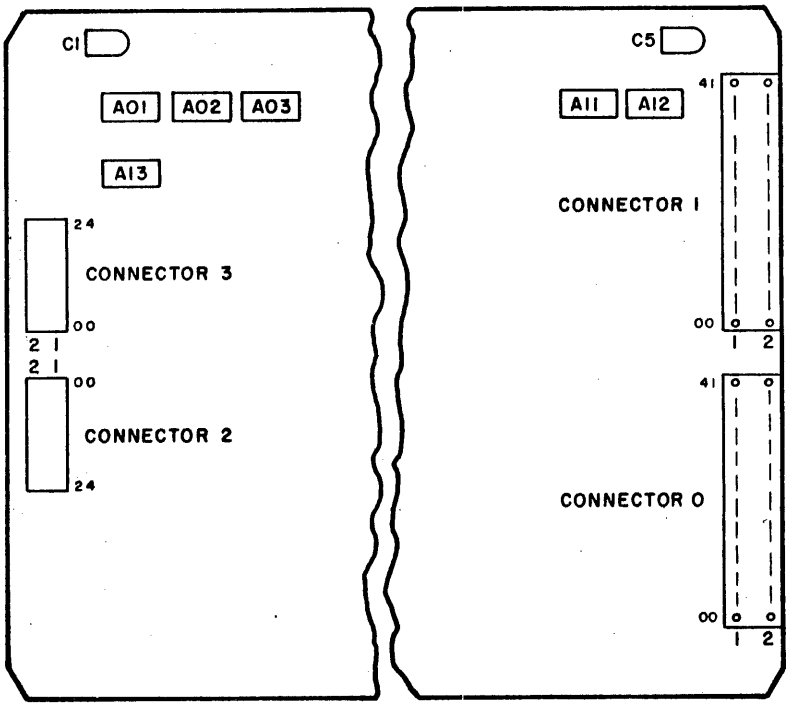

Figure 4. Example of a Logic Board Layout

19-025 – The number 19 is the category number of ICs, and the 025 is the sequence number of the component.

HA – Designates that this component is a high speed AND gate. Some other common designators used are:

P	–	Power Gate
SB	–	Schottky High Speed Power Gate
SG	–	Schottky Gate
SGO	–	Schottky High Speed Gate, Open Collector
SO	–	Schottky High Speed Gate, Open Collector
B	–	Buffer
SB	–	Schottky High Speed Buffer
LOR	–	Low Power Schottky OR
LN	–	Low Power Schottky NOR

L1 – This input lead is from area L1 on the same schematic sheet.
10M1, 1242, 18K4 – Designate outputs to another logic schematic sheet.
218-0,117-0, 114-0 – Designate inputs from Connector 0.
Pin numbers (01, 02, 04, 05 and 06) correspond directly to the actual IC pin numbers.

Figure 4 also shows the locations of the header connectors (Conn 0 and Conn 1) and the cable connectors (Conn 2 and Conn 3). All logic boards always contain Header Connectors 0 and 1, however, any combination (either, both, or none) of cable connectors (Conn 2 and Conn 3) may be provided.

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Whenever possible, the immediate output from a flip-flop (1 or 0 side) has a mnemonic name preceded by an F. A flip-flop whose name is PSEL (Processor selected) has an output mnemonic, on the 0 side, FPSEL0 (see Figure 5). This provides the digital technician with an indication, when observing a mnemonic at the terminal end of a net, that the signal is the output of a flip-flop rather than a decoded function.

Clocked devices, flip-flops, and counters in particular, are drawn in a manner which indicates information concerning their inputs. An input which has a circle adjacent to the pin designation implies a low active signal is required to perform the specified operation. In addition, an inverted V at the clock input shows that the device changes state on an edge. Thus, if no circle is present the chip is positive edge triggered. Refer to Figure 5 for examples.

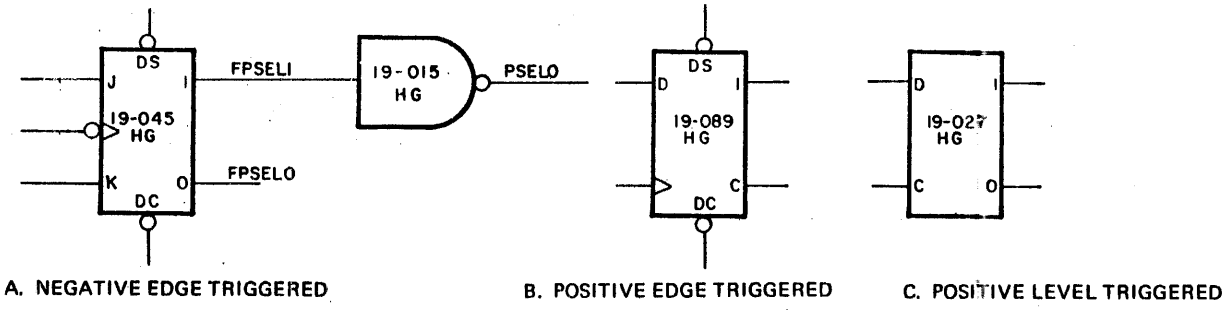

Figure 5. Examples of Clocked Devices

Figure 6 shows the pin numbering scheme for the header and cable connectors. Header connectors always have 2 rows of pins and 42 positions. Cable connectors always have 2 rows of pins but may vary in the number of positions. The number of positions may only vary in increments of five positions (10 contacts). For instance, if 24 positions are desired, five blocks of five positions each (25 positions) must be used.

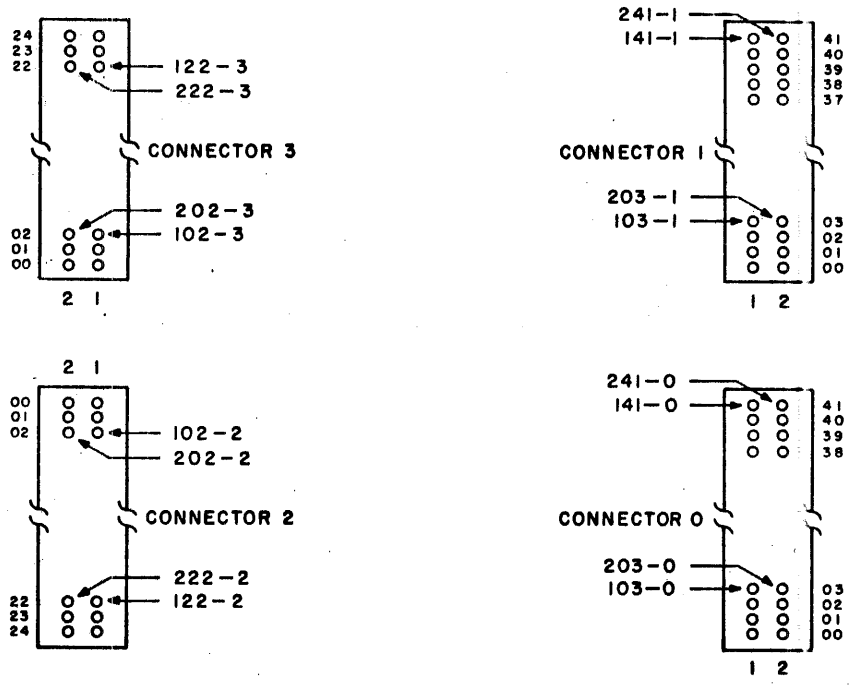

Figure 6. Connector Pin Numbering

A net is defined as an electrical connection between two or more points in a circuit. Ordinarily, a net has an originating end (usually a collector where the signal is generated) and one or more terminating ends. Often it is convenient to assign descriptive mnemonic names to nets as a way of identifying them on schematics. Whether a net is named or not is sometimes arbitrary. However, a net is always assigned a name if:

1. The net is contained on one drawing sheet but is not shown as a complete solid line on that sheet.
2. Part of the net appears on more than one sheet.
3. Part of the net connects with a different schematic.
4. Part of the net leaves a logic board.

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If a net is named, the following rules are observed.

1. All mnemonic names are a maximum of six characters.

2. All decimal digits and upper case letters except the letters "I, O, Q, and Z" are permitted.

3. No other characters are permitted.

4. Where possible, mnemonics are descriptive. However, it should be recognized that descriptive names are not always possible and a danger of misinterpreting a mnemonic exists.

5. Mnemonic names are not repeated within a schematic.

6. Every mnemonic is suffixed by a state indicator. This indicator consists of the digit "1" for the logically true state, or the digit "0" for the logically false state. For example, the set side of a flip-flop has the "1" state indicator, while the reset side has the "0" state indicator. The state indicator for a function changes each time that function is inverted. Thus, the state indicator permits assigning the same mnemonic to functions that are identical except for an inversion. Logic 0 = .4VDC or less, Logic 1 - 2.4VDC or more.

7. When a logical function is inverted, an inversion indicator is added after the state indicator. This allows for functionally equivalent, but electrically different nets to have the same mnemonic name. For example, assume a signal NAME1 which may be inverted to produce NAME0. If NAME0 is then inverted, NAME1A is produced. NAME1 and NAME1A are functionally equivalent, but physically different nets.

There are times when a net fans-out to many sheets of a schematic. It is also possible for a net to fan-out to sheets on different schematics. In such situations, the net is assigned a mnemonic name. The net is also "zoned" from sheet to sheet to allow for properly identifying the originating and terminating ends of the net. The originating end of a net is defined as the collector at which a signal is generated. All other points to which the net connects are called terminating ends. When a lead leaves a sheet at the originating end, it is zoned to each and every sheet on which the net reappears, by indicating first the page number, followed by the schematic number that contains the page. For example, assume that the gate shown on Figure 3 is on a schematic, Sheet 20. The output NAME0, appears on Sheets 10, 12 and 18 of the schematic. Note that the schematic number is implied. When a net enters a sheet from another sheet, it is labeled with the same mnemonic name, and is zoned back to the originating end of the net only. Thus, on Figure 3, the ENABL1 may have many other terminations in addition to the one shown. Generally, when a net leaves the sheet where it originates, it is zoned to every other sheet where the net terminates, while the terminating end is zoned only to the originating sheet. Note that on schematics, signals are coordinated between sheets only when the sheets are related to the same board. When a signal leaves a board, the Back Panel Map must be used.

When a lead leaves a logic board, it usually does so through a logic board back panel connector pin. These connector pins must be shown on the schematic even if the complete net is shown on one drawing sheet. Only the connector pin number need be indicated under the pin symbol, since the connector number itself is implied by the logic board location number in the logic symbol or in the footnote. Thus, on Figure 3, RD061 enters the logic board on Pin 114 of Header Connector 0.

Figure 7 is a typical schematic sheet with call-outs illustrating many of the conventions described in this section.

The schematic drawings for the basic Digital System and some of the more common expansions are commonly included in the rear of the appropriate Digital System Maintenance Manual. Schematic drawings for other expansions are included with the expansion or with the publications that describe the expansion.

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Figure 7. Functional Schematic Format Drawing

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01-094A20
August 1975

M71-SERIES
MODEL 6/16
INSTALLATION SPECIFICATION

INTRODUCTION

The INTERDATA Model 6/16 Digital System features a highly modular structure which permits configurations to suit the user's exact needs. The Model 6/16 provides the means for convenient expansion as the user's requirements grow. This document describes the Processor and System Expansion Chassis, Power Supply Mounting, Filler and Display Panel Mounting, and the interconnecting cables. Printed circuit boards are discussed with respect to cabling and location only. Circuit descriptions of these boards are provided in the appropriate maintenance or instruction manuals. The following descriptions assume that the equipment is mounted in standard INTERDATA cabinets.

MECHANICAL COMPONENTS

This section is intended to familiarize the reader with the mechanical components that are discussed in this document (i.e., Cabinet, Chassis Support Rails, and Filler Panels). Figures 1 through 4 provide the dimensions and mounting configurations for the Cabinet, Chassis Support Rails, and Filler/Display Panels. It is shown in Figure 4, that while 5¼ inch, 7 inch, 8¾ inch and 10½ inch Filler Panels and the Display Panel mount in the same way (via retaining brackets), the smaller 1¾ inch Filler Panel mounts with spring clips.

PROCESSOR AND EXPANSION CHASSIS MOUNTING

Two Processor Chassis (7 inch and Twin Versions) are available. In addition, a 7 inch Expansion Chassis is available for expanding the Model 6/16 Digital System. Two different Expansion chassis are available, one for mounting either 7 inch or 15 inch controllers and one for mounting 10 inch controllers. The Expansion Chassis has the same over-all dimensions as the 7 inch Processor Chassis (refer to Figure 12).

The Expansion or Processor Chassis slides into the rack on two Chassis support rails (refer to Figures 2 and 3) from the front of the rack.

CAUTION

NO CHASSIS SHOULD BE MOUNTED IN CANTILEVER FASHION. CHASSIS SUPPORT RAILS MUST BE USED. IF A RACK CABINET OTHER THAN AN INTERDATA CABINET IS USED, CONSULT THE RACK MANUFACTURER FOR PROPER SUPPORT RAILS.

The Chassis support rails are fastened to the mounting uprights at the front and rear of the rack. The Expansion or Processor Chassis are fastened in place, with screws, to the mounting uprights in front of the rack. All Expansion Chassis mount below the Processor Chassis. Expansion Chassis cabling is discussed later in this document. Expansion Chassis location with respect to the Filler Panel and Power Supply is shown in Figure 14.

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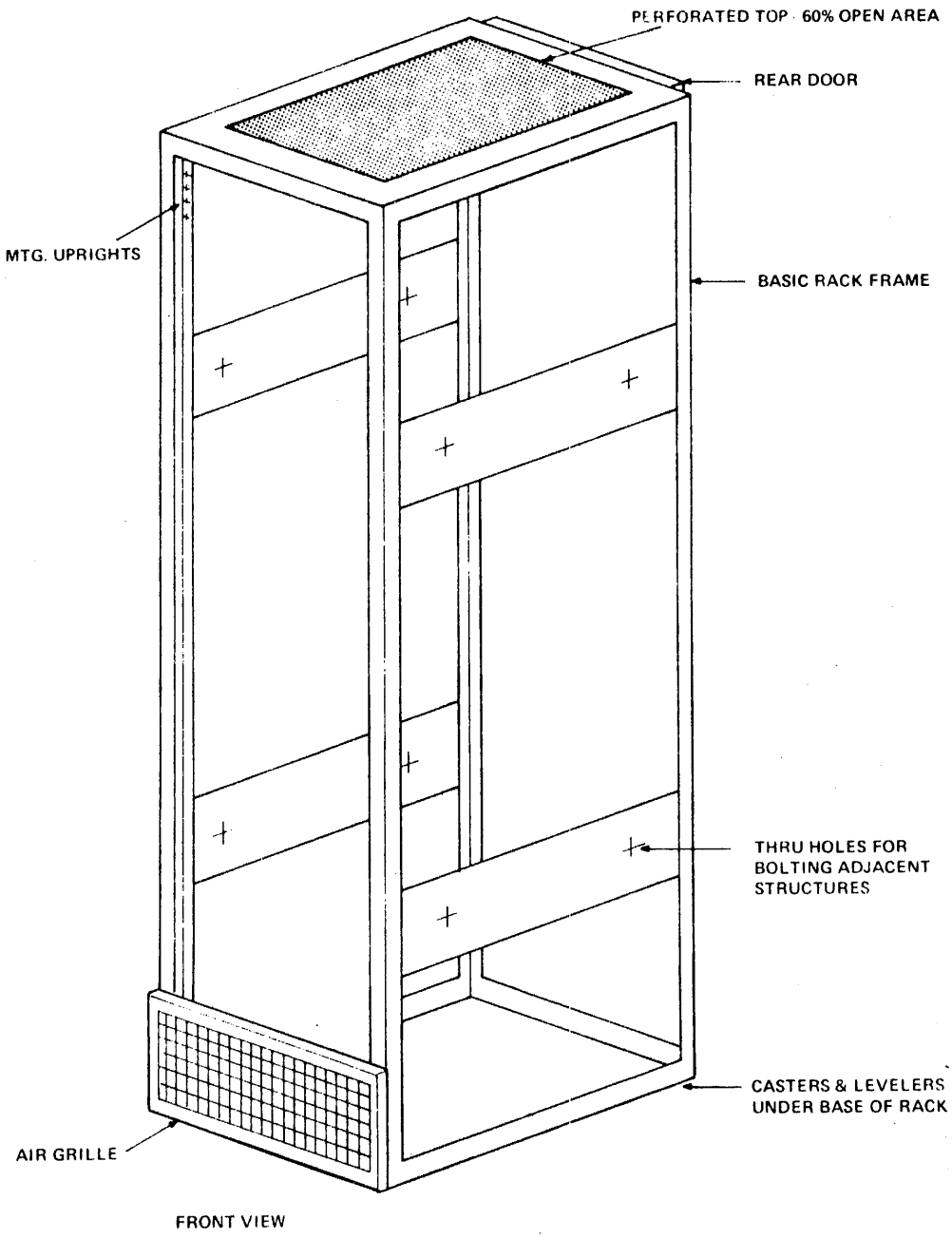

Figure 1. Basic Cabinet

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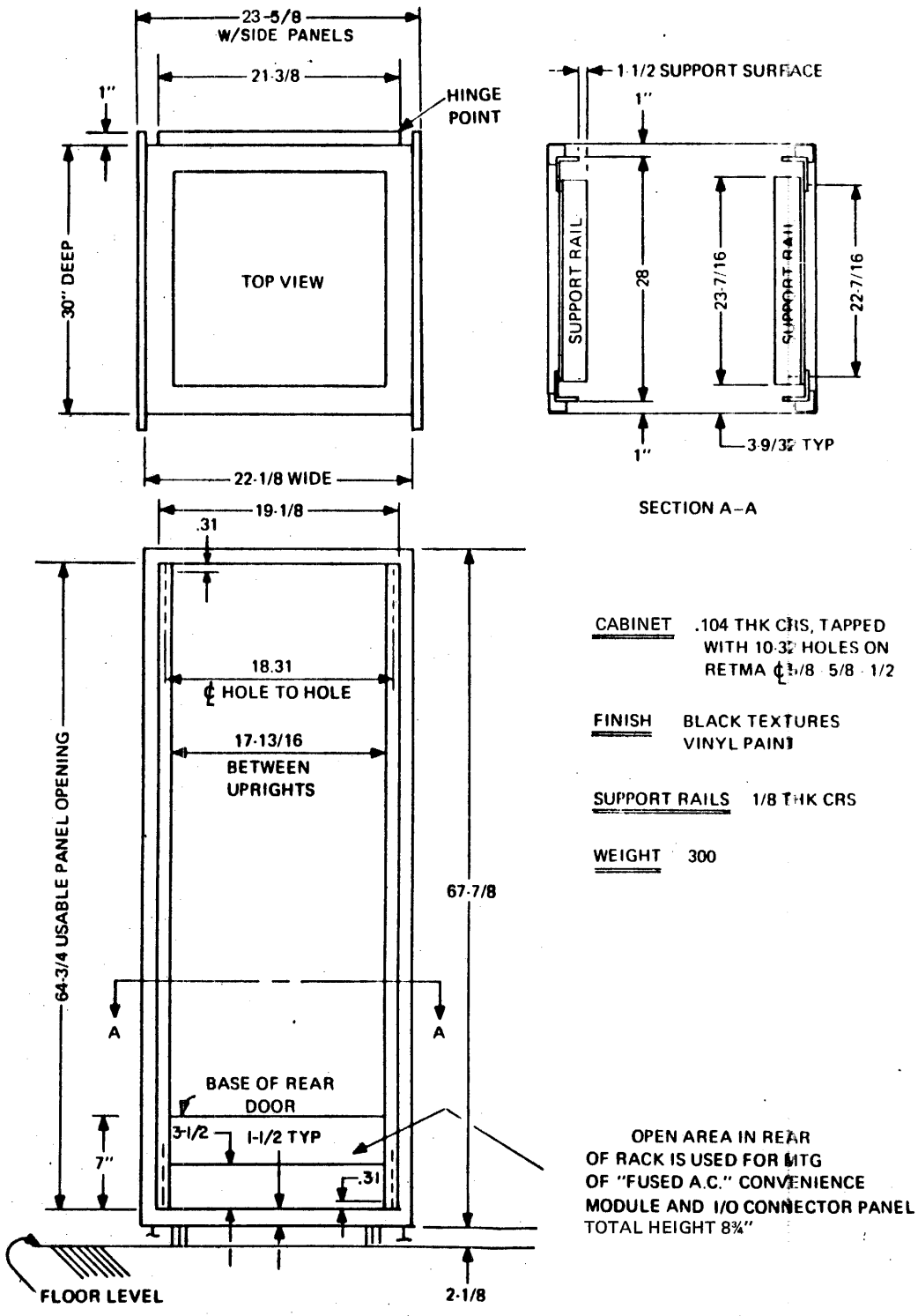

Figure 2. Basic Cabinet Physical Dimensions

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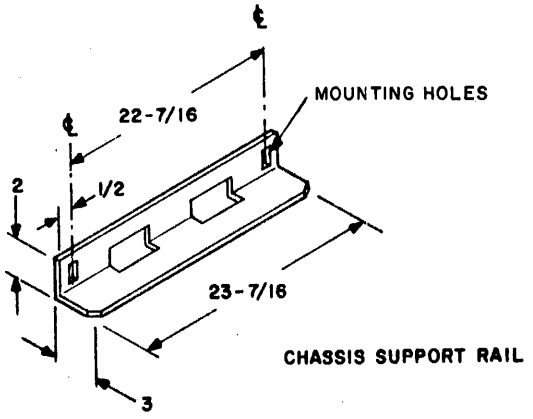

Figure 3. Chassis Support Rail

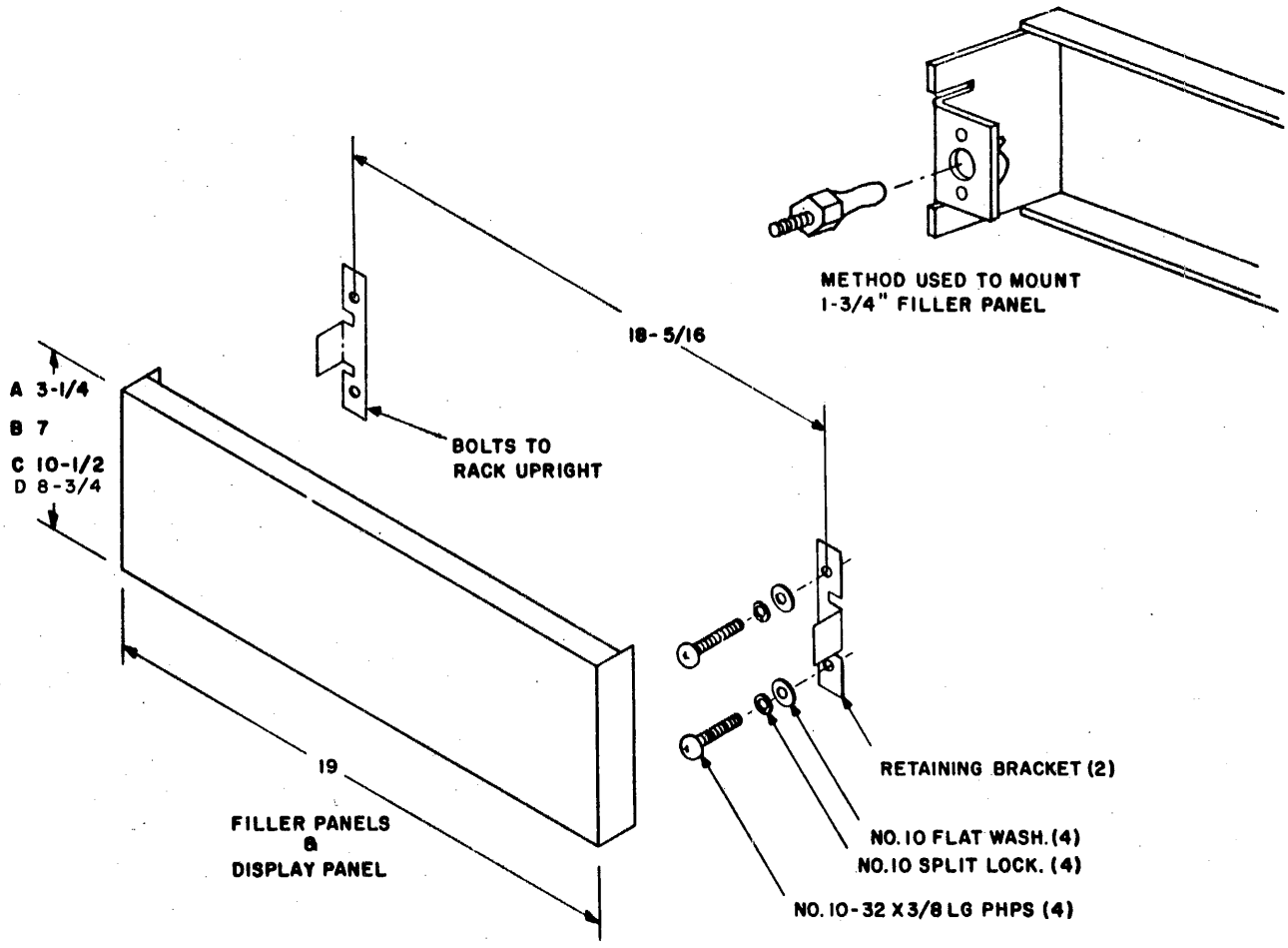

Figure 4. Typical Mounting Configuration for Display and Filler Panels

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Expansion Chassis

The Expansion Chassis for 7 inch and 15 inch controllers contains eight universal expansion slots which can accept combinations of single board peripheral controllers, system modules, Selector Channel, or user designed interfaces. Included with this 7 inch Chassis are the cooling fans and interconnecting cables. The chassis may be ordered with or without a power supply.

A 10 inch I/O controller (provided it does not use Connector 1) may be inserted in this chassis via the 02-234 I/O Adapter Kit (see Figure 5).

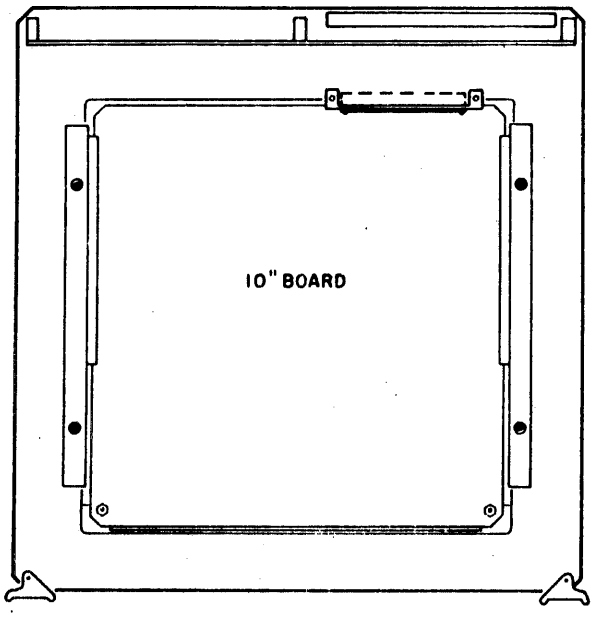

Figure 5. 02-234 I/O Adapter (Top View)

One or two 7 inch boards (half-boards) may be inserted into this Chassis via the 16-398 Half-Board Adapter Kit (see Figure 6). The Half-Board Adapter Kit may hold two active 7 inch boards or one active and one blank 7 inch board, depending on requirements.

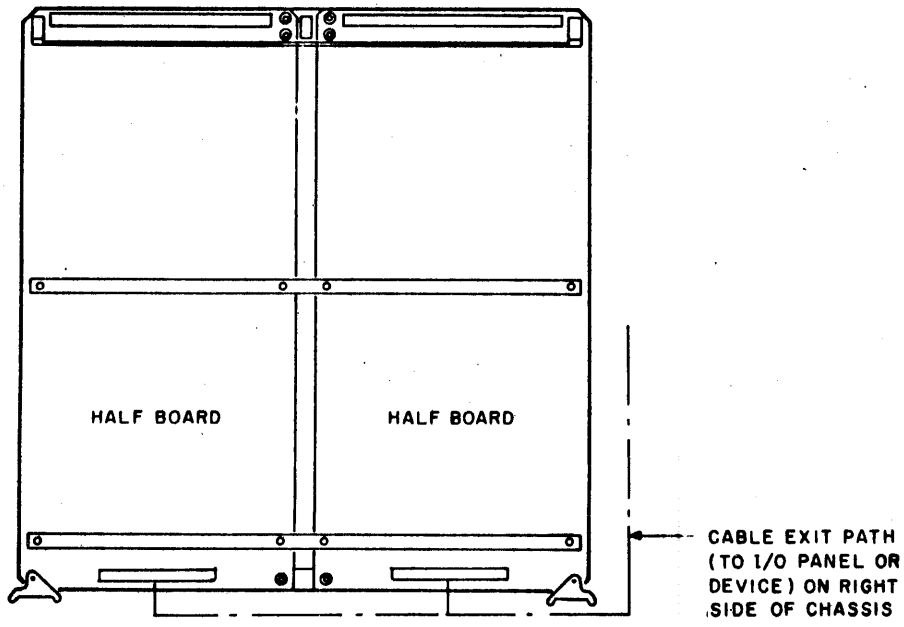

Figure 6. 16-398 Half Board Adapter

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No wiring takes place between the boards and the adapters. The adapters are designed such that the connectors on the board plug directly into the Expansion Chassis.

The Expansion Chassis for 10 inch controllers contains six 10 inch I/O expansion slots which can accept any combination of up to six 10 inch wire-wrap or copper peripheral controllers, systems, modules, or user designed interfaces. Included with the Chassis are the cooling fans and system interconnecting cables. The Power Supply is separate.

POWER SUPPLY MOUNTING

The Power Supply mounts in the rear of the cabinet, behind the Processor or Expansion Chassis. It is attached to the right mounting upright (looking from the rear). One of three Power Supplies may be supplied with the Model 6/16 System.

These Power Supplies attach to the mounting upright via four 10-32 x ½ lg PHPS screws (refer to Figure 7).

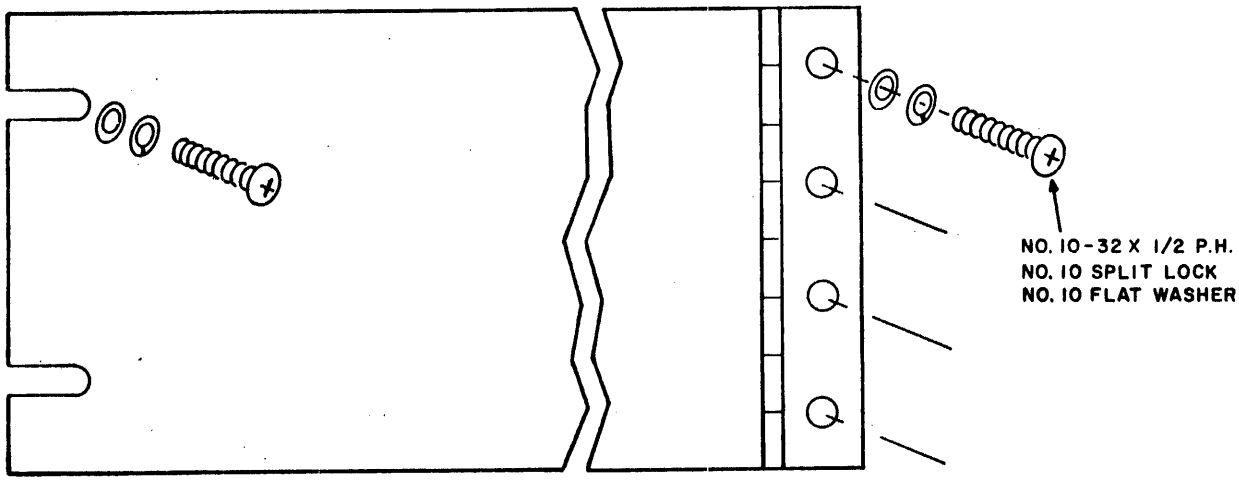

Figure 7. Power Supply Mounting

WARNING

BEFORE HINGING OUT THE POWER SUPPLIES, THE RACK LEVELLING FEET SHOULD BE LOWERED. AFTER THE LEVELLERS ARE IN CONTACT WITH THE FLOOR SURFACE, UP TO THREE POWER SUPPLIES MAY BE HINGED OUT AT ONE TIME. IF THE LEVELLERS ARE NOT DOWN, AND THREE POWER SUPPLIES ARE HINGED OUT, THE RACK MAY TIP DUE TO THE WEIGHT OF THE POWER SUPPLIES.

When any Power Supply is in the installed operating position, it is secured to the left rear upright by two 10-32 screws. The power supply cable connects to terminal lugs at the right rear (looking from the rear) of its respective Processor or Expansion Chassis via Faston lugs and a connector for AC fan power (refer to Figure 8).

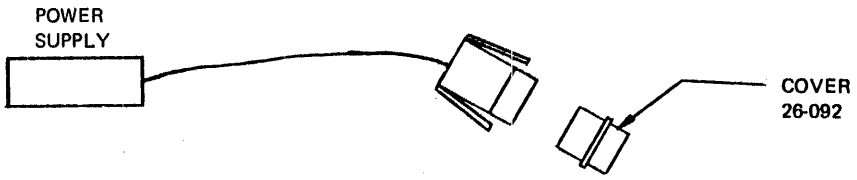

Figure 8. Fan Connector Caps

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There is adequate slack provided in the cable to allow the Power Supply to hinge out freely. In order to prevent the cable from being pinched between the Power Supply and Chassis Support Rails, a service loop is required. A maximum of five Power Supplies may be mounted in one rack.

WARNING

ALL AC FAN CONNECTORS ON POWER SUPPLIES WHICH ARE NOT CONNECTED TO MATING RECEPTACLES MUST REMAIN COVERED OR SHORTING MAY OCCUR. SEE FIGURE 8.

The 115/230 volt fan switch on the chassis must be matched with the 115 volt or 230 volt strapping on the Power Supply (refer to Figure 9).

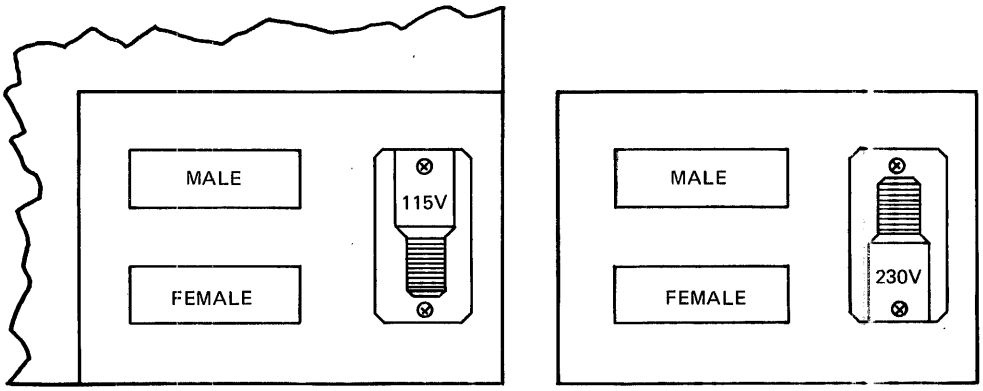

Figure 9. Fan Power Switch Match

Exhaust fan plates are equipped with a switch to provide either 115 volt or 230 volt AC operation as shown in Figure 10.

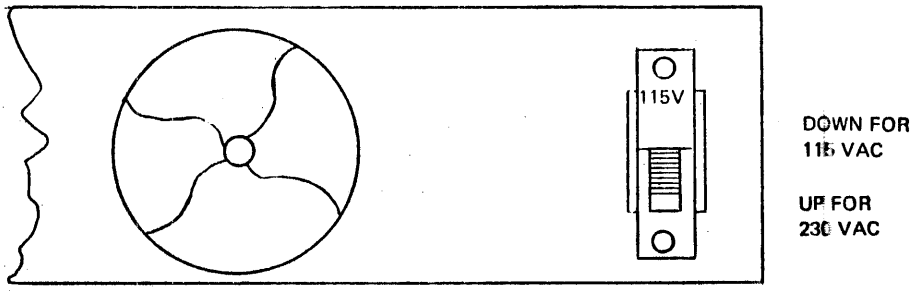

Figure 10. Exhaust Fan Switch Setting

A third supply (34-023) designed to meet VDE specifications required by some International installations, is also available. The mounting procedure for this power supply is different than the procedure for the standard supplies. Refer to *Power Supply Maintenance Manual,* Publication Number 29-452, for installation information.

DISPLAY PANEL INSTALLATION

The optional Model 6/16 Hexadecimal or Binary Display Panel is electrically tied to the system via one connector and seven Faston lugs. The connector is installed on Connector A of the 35-601 or 35-602 Display Controller Board and the seven terminal lugs mate into a terminal strip on the left side of the Processor Chassis. The terminal lugs are identified at the Faston Connector and are mated to their corresponding terminal pin (C1, C2, etc.) on the Chassis, see Figure 11.

The Hexadecimal Display Panel is physically mounted to the brackets provided on the Processor Chassis. The 1¾ inch Filler Panel is mounted directly below the Hexadecimal Display Panel on this same Chassis (see Figure 12.)

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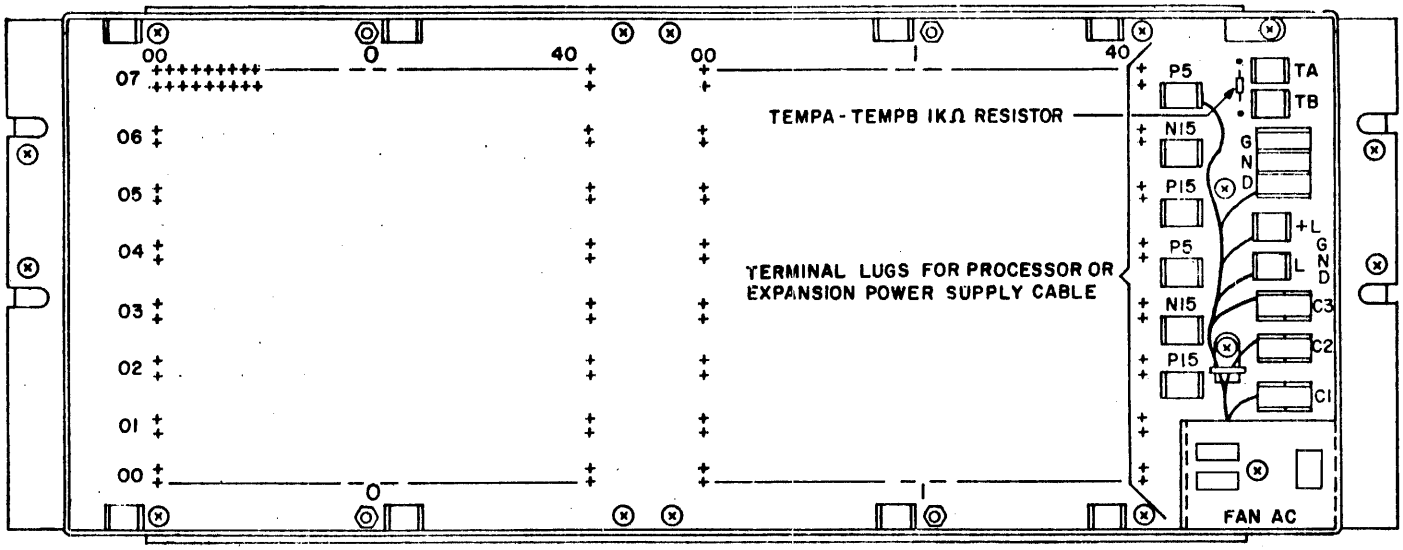
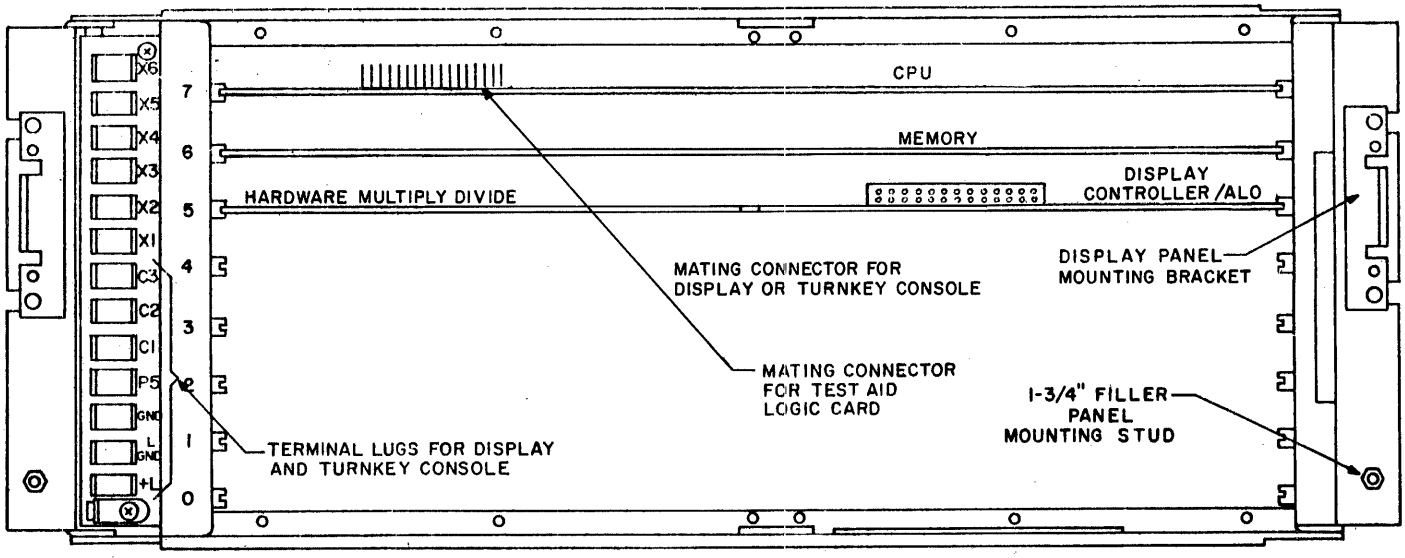


Rear View



Front View

Figure 11. View of the Processor and 15 Inch Expansion Chassis

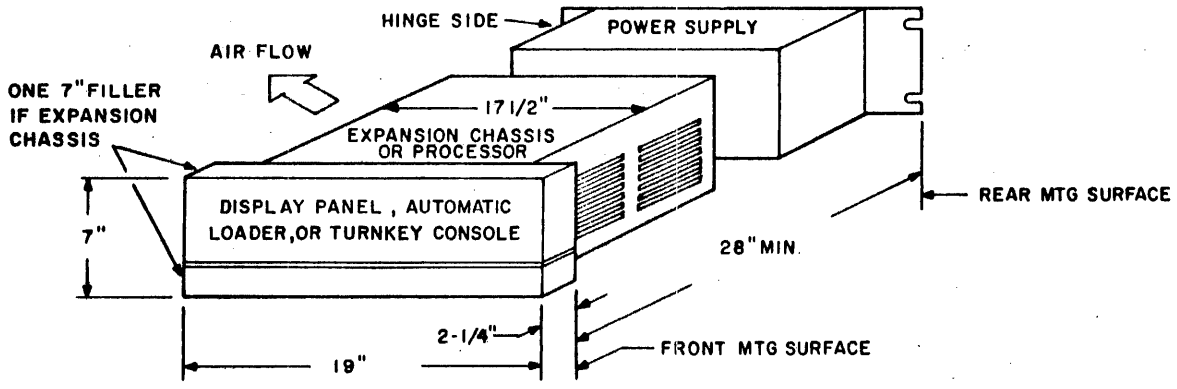


Figure 12. Processor or Expansion Chassis

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TURNKEY CONSOLE PANEL INSTALLATION

The Turnkey Console is connected to the Processor in the same manner as the Hexadecimal Display Panel previously discussed. Only two Faston connectors are provided with this assembly, but their installation is the same (see Figure 13).

The panel on which the switches are installed is mounted in the same manner as the display panel.

The Hexadecimal Display Panel option, and the Turnkey Console option may not be installed together in the same system.

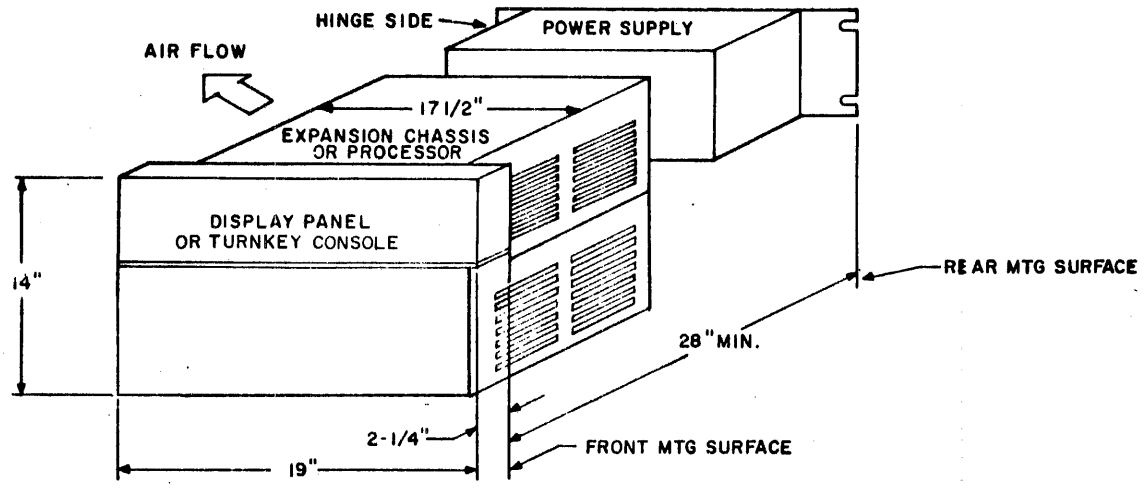

Figure 13. Twin Chassis Processor

MEMORY INSTALLATION

A single slot is allocated to Memory on the Model 6/16. Memory must be installed in Slot 6 of the Processor Backpanel.

NOTE

When installing either an 8KB or 16KB Memory Module on the Model 6/16 the Memory Adapter Card, 35-608, must be installed at the Processor Backpanel on Slot 6. In addition jumpers must be added between 135-0007 and 235-0006, between 128-0106 and TEMPA, and between 227-0106 and TEMPB on this same Backpanel. Remove the 1K OHM Resister between TEMPA and TEMPB. The 16KB Memory Module must be at revision M02R02 or higher.

INSTALLATION OF CPU OPTIONS

Display Controller/Automatic Load Option

Install the Display Controller, 35-601, the Display Controller with Automatic Load Option, 35-602, or Automatic Load Option, 35-603, in Slot 5 Connector "0" of the Processor Backpanel. A Half-Board Adapter 16-398, must be used to mount this board (see discussion on Expansion Chassis).

The Hexadecimal or Binary Display cable or the Turnkey Console cable mounts to the connector on the outer edge of the Display Controller PC board.

Hardware Multiply/Divide Option

Install the Hardware Multiply/Divide PC board, 35-605, in Slot 5 Connector "1" of the Processor Backpanel. A Half-Board Adapter, 16-398, must be used to mount this board (see the discussion on the Expansion Chassis).

NOTE

The Multiply/Divide Option may only be used on Processors equipped to support this option. The Processor PC board must be stamped 35-604F02.

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Primary Power Fail/Auto-Restart Option

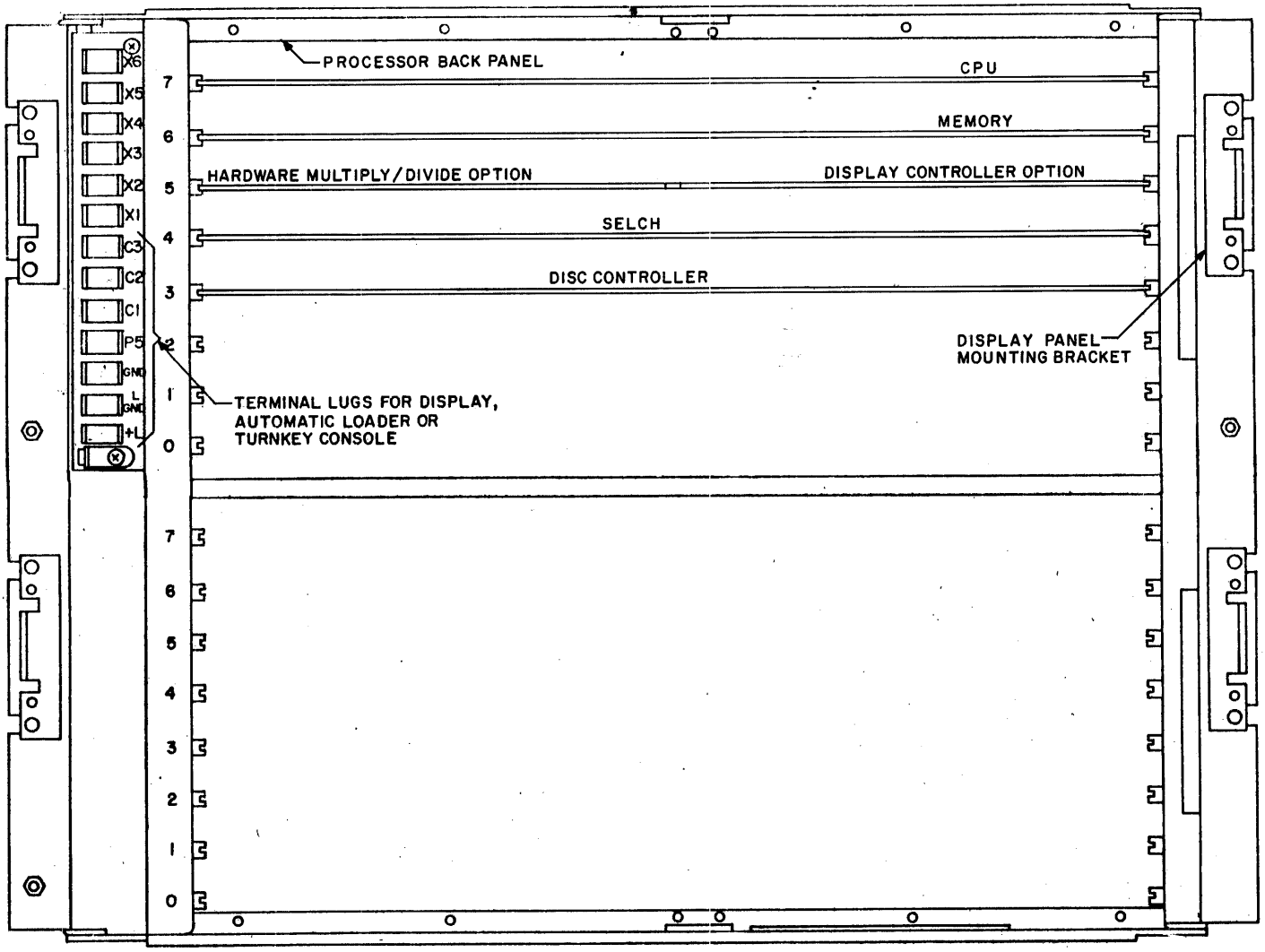
Install the 35-448 logic card for the Primary Power Fail/Auto-Restart option on the wire wrap side of the Processor Backpanel at Slot 7, Connector 0 with the apparatus side up. The 17-182F01 and 17-182F02 cables which supply 12 VAC to the logic card, connect between C1 on the logic card and C1 on the backpanel and C3 on the logic card and C3 on the backpanel as indicated on the cables (see Figures 14 and 15). The Primary Power Fail option card is adjusted at the factory.

Memory Parity Option Card

The 35-533 Memory Parity Option card is used with parity memory modules only. The Memory Parity option card mounts on the wire wrap side of the Processor Backpanel, Slot 7, Connector 1 (see Figure 15).

Selector Channel (SELCH) Installation

The 35-391 Selector Channel may be installed in Slot 4, 2, or 0 of the Processor Backpanel or in Slot 6 or Slot 4 of the Expansion Backpanel on a Twin Chassis version of the Processor. The maximum number of Selector Channels in a system is 4 for a Twin Chassis Processor or 3 for a 7 inch Chassis (refer to Figure 16). Also see the Selector Channel Installation Specification 02-232M01A20, for further information on installing SELCHs.



Front View

Figure 14. Front View of the 6/16 Twin Chassis

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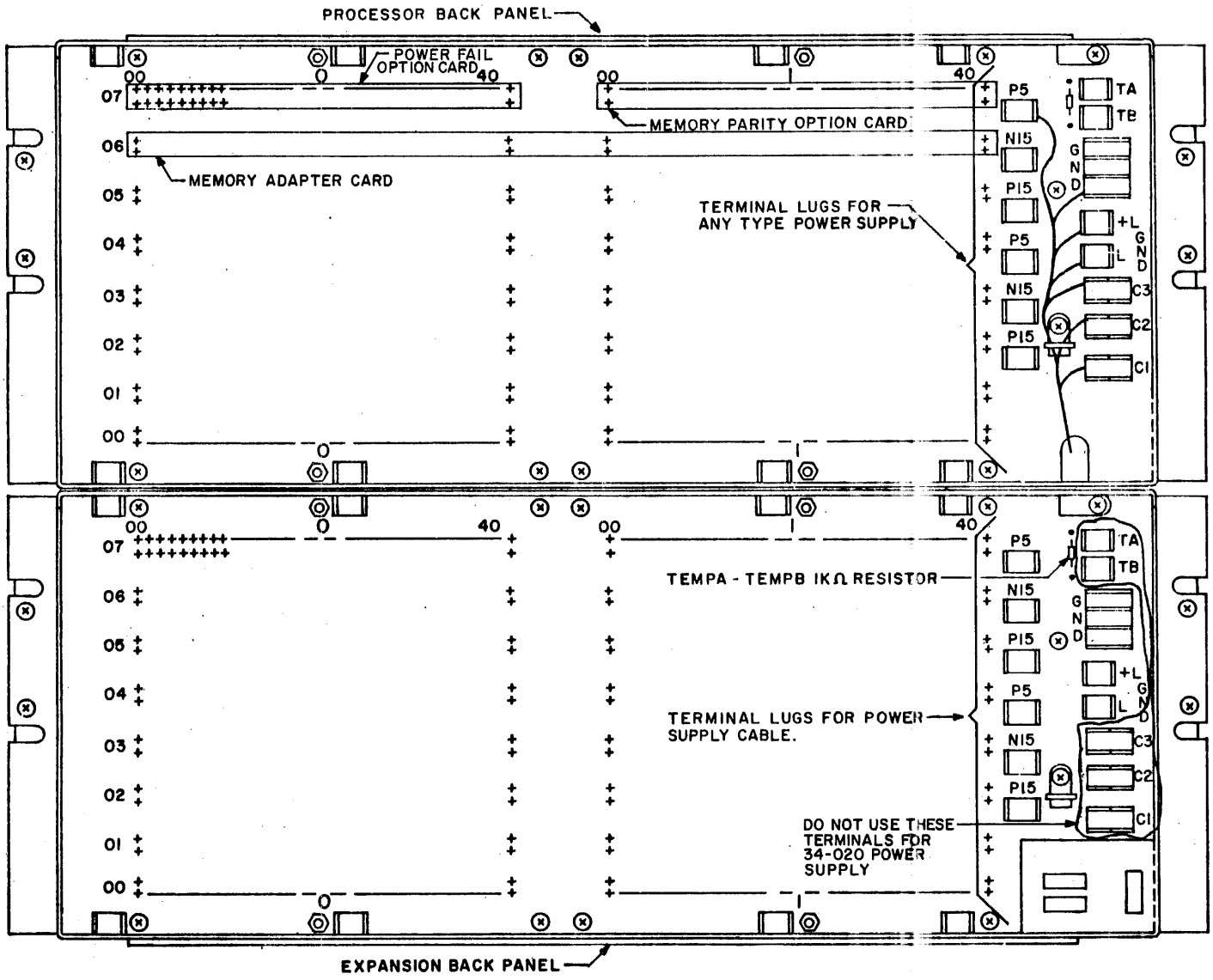

Rear View

Figure 15. Rear View Model 6/16 Twin Chassis

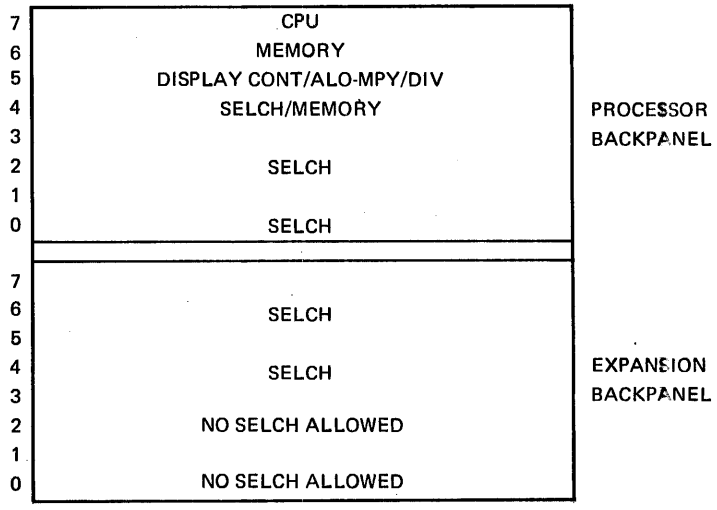

Figure 16. System Configuration (Front View)

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Basic Switch Panel Option

For systems not equipped with either the Hexadecimal or Binary Display or Turnkey Console the Basic Switch Panel is used to start the system. The Installation Procedure for this Option is as follows:

1. Connect the four Faston lugs to the terminal strip located on the left side of the Processor Chassis. The terminal lugs are identified at the Faston connector and are mated to their corresponding terminal pin (C1, C2, etc.) on the chassis. (see Figure 11).

2. Remove the Faston connection on the Rear of the Processor Chassis labeled L-GND which comes from the Power Supply and connect this lug to a spare GND lug. Install a wire between the L-GND male receptacle, just vacated, and Back Panel pin INITO (136-0501). The panel on which the switch is installed may be mounted to the chassis uprights with standard 10-32 hardware. This panel is intended to mount behind a door or filler panel to prevent easy accessibility when the system is running. This option may not be used on a system on which a Display Panel is installed.

CONFIGURATION

System Expansion Chassis

When configuring a multi-chassis system there are four rules that must be followed:

1. The system Expansion Chassis must be mounted below the basic Processor Chassis.

2. All Chassis must be Contiguous.

3. All 15 inch system Expansion Chassis must be mounted above any 10 inch system Expansion Chassis.

4. Multiboard peripheral device Controllers (on 10 inch circuit boards) can only be used in the 10 inch system Expansion Chassis.

Circuit Board Distribution

The Model 6/16 Digital System may be configured in a variety of ways. However, the following factors must be considered when determining circuit board distribution within the basic Processor and system Expansion Chassis (see Figure 16).

1. The Selector Channel or Selector Channels must be installed in the slots described under SELCH Installation.

2. All device addresses are hard-wired on the device controller cards (device addresses may be changed at option), so that the distribution of I/O device controllers in the chassis normally need be considered as a matter of priority in the RACK0/TACK0 "daisy-chain".

3. The 15 inch system Expansion Chassis, and the basic Processor Chassis may only be used for single board I/O device controllers unless the interconnection between boards takes place via cables installed on the outer edge of the board. For multi-board 10 inch device controllers, the 10 inch system Expansion Chassis must be used.

4. The interrupt priority of a given device controller is determined by its physical location on the serial RACK0/TACK0 line. Refer to Interrupt Priority Back Panel Wiring to determine which physically located controller has what priority. When deciding which devices should have a higher or lower priority, devices that must be serviced in a certain amount of time or loss of data access should be given a higher priority than a device with a high interrupt rate and no data loss if not serviced.

Interrupt Priority Backpanel Wiring

The Acknowledge Control line from the Processor carries the Interrupt Acknowledge (ACK) signal. This line breaks up into a series of short lines to form the "daisy-chain" priority system. The ACK signal must pass through every controller that is equipped with Interrupt Control circuits. Refer to Figure 17 to determine order of priority.

Back panel wiring for interrupt control at a given position is: The Received ACK (RACK0) at Pin 122-0 or 1 and the Transmitted ACK (TACK0) at Pin 222-1 or 0. The daisy-chain bus is formed by a series of isolated lines which connect Terminal 222-1 or 0 of a given position to Terminal 122-1 or 0 of the next position (lower priority). On unequipped positions, a jumper shorts 122-1 or 0 and 222-1 or 0 of the same connector to complete the bus. Back panels are wired with jumpers on all positions. Whenever a card chassis position is equipped with a controller that has an interrupt capability, the jumper from 122-1 or 0 and 222-1 or 0 must be removed from the back panel at that position.

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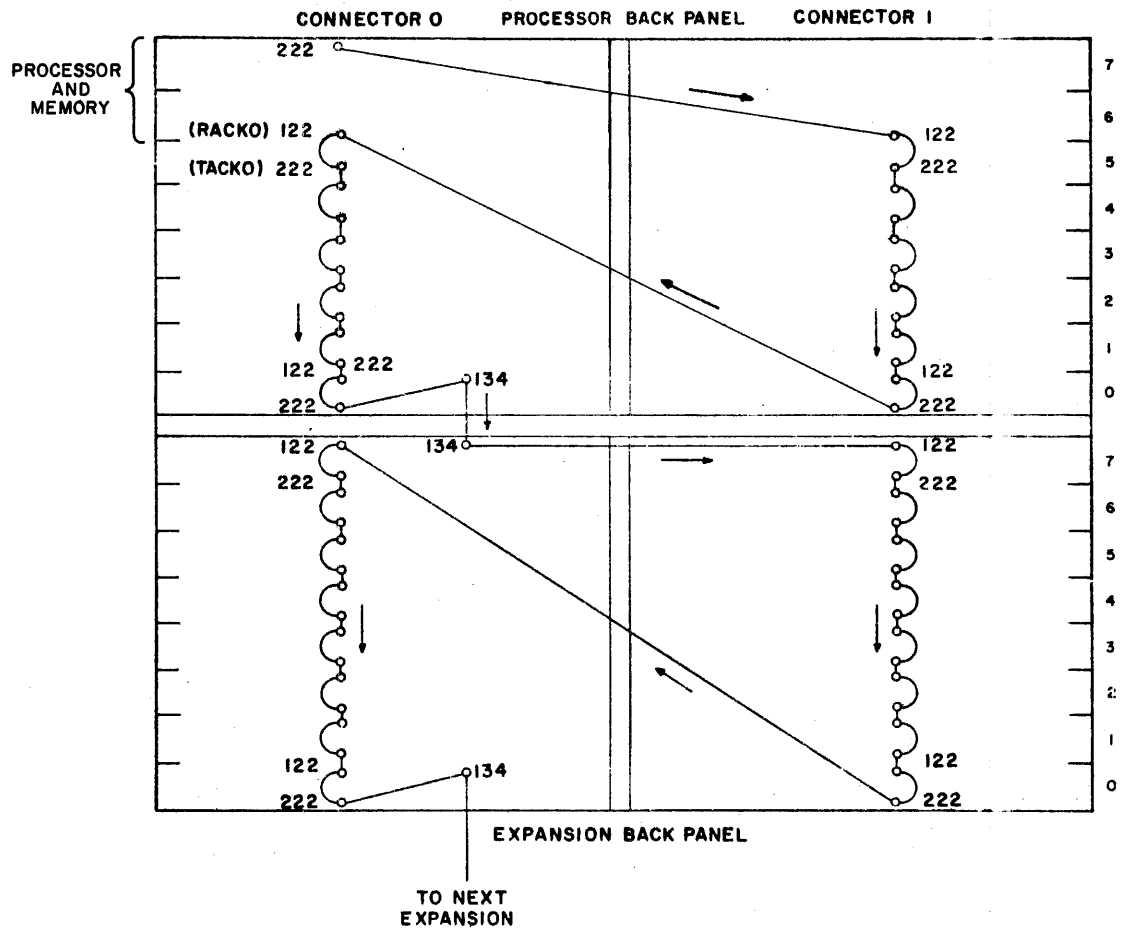

Figure 17. Standard Interrupt Priority

Figure 17, showing the standard interrupt priority wiring, assumes a Model 6/16 Processor and memory. The arrows indicate the direction of priority from the highest priority to the lowest. By changing the wires crossing from Side 0 to Side 1 of the PROC and/or Expansion Panels, interrupt priorities may be rearranged. An example of this is shown in Figure 18, Modified Interrupt Priority. Slot 5 on Side 1 of the Processor panel has the highest priority. When Selector Channels (SELCHs) or Bus Buffers are installed, the standard interrupt priority must be modified. Refer to Figure 19, Interrupt Priority with SELCH Installed.

For controllers that occupy several positions, the jumper is removed only at the position where the controller board has ATN/ACK circuits. For details on the various devices, see the appropriate installation specification.

Terminators

The termination end of both legs, Connector 0 and 1, of the Multiplexor Bus must have a standard INTERDATA termination card (35-433) installed if the bus is extended beyond a single 7 inch chassis or backpanel. These cards are installed on the back panel at the lowest numbered slot of both connectors on the Multiplexor Bus that exists; e.g., if a Selector Channel or bus buffer is installed in Slot 4 on the first expansion chassis and only the Processor Chassis and one Expansion Chassis is used in the system, the Multiplexor Bus must be terminated at Slot 0, Connector 0, and Slot 5, Connector 1 of the Expansion Chassis. In addition, the buffered bus or the SELCH Bus should be terminated at Slot 0, Connector 1 of this chassis.

Depending upon system configuration, any SELCH Bus or Buffered Bus may be terminated by a 15 inch Terminator (35-433) or a 10 inch Terminator (35-434). The choice of terminators depends on the type of chassis in which the last slot of the bus is present.

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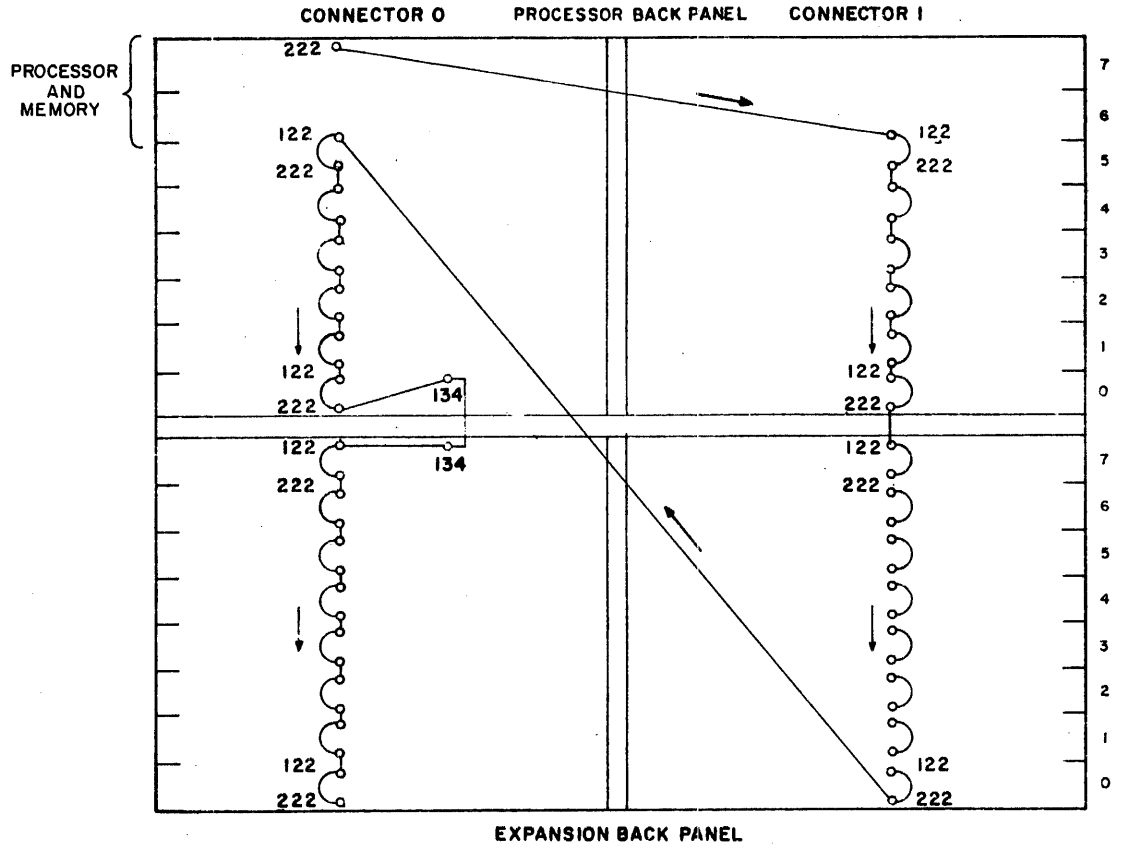

Figure 18. Modified Interrupt Priority

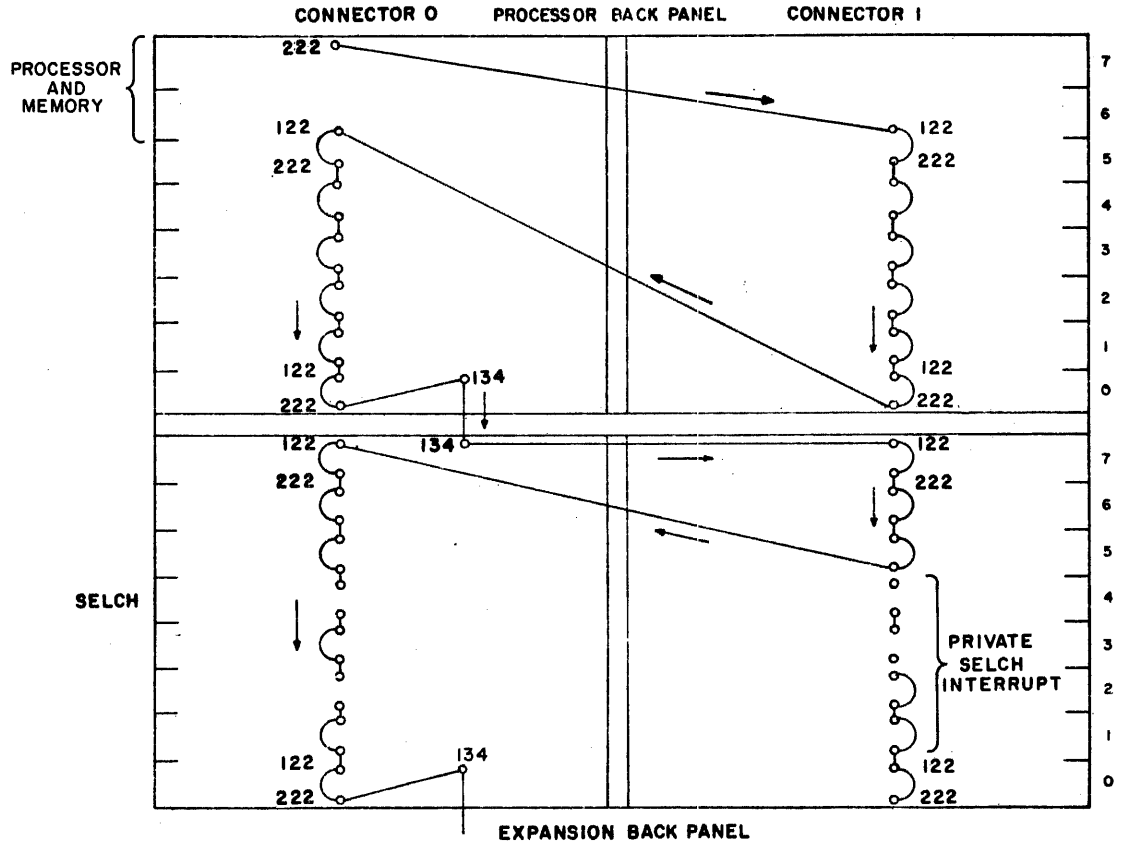

Figure 19. Interrupt Priority with SELCH Installed

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CABLES

Power Cable

The standard INTERDATA Cabinet is wired for 30 Ampere service. On the main power cable (part of the AC Distribution Panel), there is a three wire, twist lock, grounding, 125VAC, 30 Ampere, UL, (Hubbel No. 2610) plug. A three wire grounding, 30 Ampere, 125 VAC receptacle (Hubbel No. 2611 or equivalent) is required to accept this plug.

System Expansion Cable

A number of standard cables are available for configuring systems made up of an INTERDATA Expansion Chassis. The choice of cables is dependent upon system configuration. The following cables are available:

1. 17-193: I/O Expansion Cable, Connector "0"

This cable is used to connect the "0" connector field between two adjacent 15 inch card files.

2. 7-194: I/O Expansion Cable (see note)

This cable is used to connect the "1" connector I/O fields between two adjacent 15 inch card files.

3. 17-216: I/O Expansion Cable, 36 Inch Long

This cable is used to connect two 15 inch files that are not adjacent. It must not be used to extend the basic Processor Multiplexor Bus.

It can be used to extend a buffered bus or a SELCH Bus. It plugs into a "1" side connector. The "receiving" end can plug into the "0" or "1" side of the expansion file.

4. 17-214: 15 inch to 10 inch Expansion Cable

This cable is used to connect the "0" connector field of a 15 inch card file to a lower adjacent 10 inch card file. It provides an 8 bit I/O bus to the 10 inch card file.

5. 17-166: 15 inch to 10 inch I/O Expansion Cable, 36 Inches Long

This cable is used to connect the "1" side of a 15 inch expansion file to a 10 inch expansion file. It provides an 8 bit I/O bus to a 10 inch card file.

It must not be connected to the basic Processor Multiplexor Bus.

It may be driven either by an Extended Selector Channel or a bus buffer.

It can be used on the older 10 inch card file (13 I/O slot).

6. 17-183: "0" to "1" Connector

This cable can be used to interconnect the I/O Multiplexor Bus of the "0" field and the "1" field within a 15 inch card file.

There is no RACK0/TACK0 wire in this cable.

It can also be used to connect a "0" side (Slot 0) of a file, to the "1" side (Slot 7) of the next adjacent file, or vice versa.

7. 17-215: 10 inch to 10 inch I/O Expansion Cable

This cable is used to connect two adjacent 10 inch card files.

NOTE

A strap is installed at the factory on the receive end of either a 17-327 or 17-194 cable. This strap must be removed unless the cable is being used to jumper a private I/O Bus (ESELCH or Bus Buffer). This strap jumpers Pin 222-0001 of the upper chassis to Pin 122-0701 of the first expansion chassis. If these cables are used to extend a SELCH or Bus Buffer the following wiring changes are required on the lower chassis:

Remove the strap from Pin 134-0700 to Pin 122-0701

Add a strap from Pin 134-0700 to Pin 122-0700

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CONFIGURATION RULES

1. A maximum of 16 device controllers may be installed on the Multiplexor Bus of the Model 6/16. This assumes all drivers in the system are capable of sinking 48 milliamps or more and no more than one TTL load (2 milliamps max.) on any Control Line or Data Line on the device controllers. The Display Controller and Multiply/Divide option are considered one load each.

2. The Multiplexor Bus must be contained within the Processor Chassis and three adjacent 7 inch Expansion Chassis (two adjacent chassis if the Processor Chassis is a Twin Chassis). The Multiplexor Bus must be buffered by a Bus Buffer or the equivalent for systems which require the Multiplexor Bus to be extended beyond these limits or in the case where the Bus must be extended by any 36 inch cable.

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M71-SERIES
MODEL 6/16
MAINTENANCE SPECIFICATION

INTRODUCTION

The Model 6/16 Processor is a low cost, 16-Bit general purpose minicomputer. The latest MSI and LSI Integrated Circuit technology is used to construct a processor suitable for use in data communications, process control, or stand-alone scientific computer applications. The Model 6/16 Processor is modularly constructed for ease of maintenance and is compatible with all building blocks in the INTERDATA product line.

SCOPE

This specification describes the functional operation of the Model 6/16 Processor and provides maintenance information useful to digital technicians maintaining this processor. A block diagram analysis, a micro-program description, and a functional analysis of major processor areas are included.

BLOCK DIAGRAM ANALYSIS

The following sections make reference to Figure 1.

System Organization

The Model 6/16 is organized between two 16-bit buses. The B Bus is used to present data to the Arithmetic Logic Unit (ALU). The S Bus then transfers the ALU output to the appropriate destination. The source and destination of data on the B Bus and S Bus as well as the functions performed by the ALU are controlled by micro-instructions contained in the Read-Only-Memory (ROM).

Read Only Memory (ROM)

The Read-Only-Memory is a high speed, solid state, non-destructive memory organized into one page of 512 words. An additional page of 512 words is available for expansion (e.g., Multiply/Divide option). Each word in ROM is 24 bits long and represents one micro-instruction. Each micro-instruction read out of ROM is latched at the ROM output by latches internal to the ROM. Most micro-instructions are executed in one machine cycle. The ROM bits are decoded to select a Source to be statically unloaded to the B Bus as well as a second Source to be directed to the ALU (see Figure 1). The ALU then forms a result on the S Bus. This result becomes available some time before the end of the machine cycle and is deposited in the appropriate destination register at the start of the next machine cycle as the next micro-instruction is fetched. The meaning of the micro-instruction word bits is explained later.

Locations in the ROM are addressed by the 10-bit ROM Address Register (RAR). Micro-instructions are normally located at sequential addresses in the ROM. The RAR is an up-counter which increments by one before each new micro-instruction is fetched. The RAR therefore holds the address of the micro-instruction presently being executed. When it becomes necessary to jump out of sequence, the RAR can be loaded with a new address from the ROM, from the Decoder ROM (DROM), or it can be preset by hardware.

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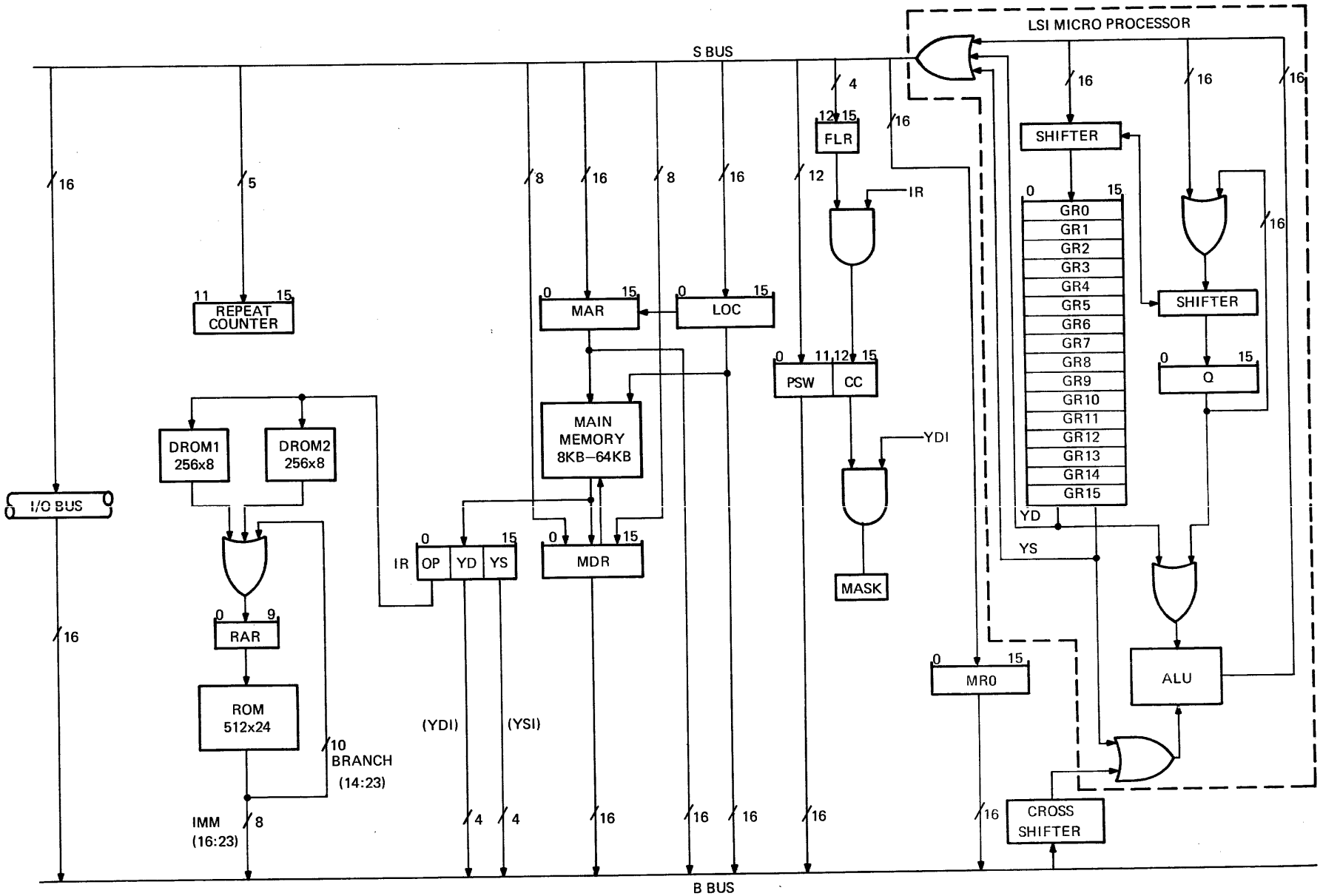

Figure 1. Block Diagram 6/16 IWLM

Repeat Counter

The Repeat Counter is a 5-bit counter which can be loaded from the S Bus. The purpose of this counter is to allow a micro-instruction to be executed n number of times (where $n \leqslant 31$) before the next micro-instruction is fetched. The next micro-instruction in sequence following the micro-instruction which loads the Repeat Counter is the one which is automatically repeated n-times.

Flag Register (FLR)

The Flag Register (FLR) is a four-bit register containing the following flags: Carry (C), Overflow (V), Greater Than Zero (G), and Less Than Zero (L). These flags are modified at the conclusion of arithmetic and logical micro-operations to reflect the result of the operation. The FLR is loaded from Bits 12 through 15 of the S Bus when either the FLR or the Program Status Word (PSW) is the specified Destination Register.

Program Status Word (PSW)

The Program Status Word (PSW) is a 16-Bit register used to indicate the system status relative to the user program being executed. Bits-0 through 6 of the PSW define enabled interrupts and the operational status or mode of the user level processor. PSW Bits-7 through 11 are not defined. Some of the PSW bits have hardware significance while others are of significance only to the micro-program. Bits-12 through 15 of the PSW make up the Condition Code field (CC) which reflects the result of the most recent user instruction. Bits-8 through 11 are not provided.

The Condition Code may only be updated from the FLR. When PSW is the Specified Destination Register Bits-0 through 7 of the S Bus are loaded into Bits-0 through 7 of the PSW and S Bus Bits-12 through 15 are captured in the FLR. The Condition Code field is then updated from the FLR on the next Processor clock. Instruction Read operations also copy the contents of the FLR into the Condition Code.

Location Counter

The Location Counter (LOC) is a 16-bit appendum to the PSW which holds the main memory address of the next user instruction to be performed. The Location Counter is an up-counter which automatically increments by 2 following each Instruction Read micro-instruction or D1 option in the micro-instruction (unless the op-code indicates an RR or SF format instruction). Bit-15 of this register is not implemented.

Memory Address Register (MAR)

The Memory Address Register (MAR) is a 16-bit register which is loaded with the address of main memory locations. It is automatically loaded from the Location Counter each time LOC is incremented. It can also be loaded from the S Bus whenever LOC or MAR is the specified Destination Register.

Main Memory

The Main Memory consists of random access memory providing storage for user instructions and data. Memory is addressed through the Memory Address Buffer (MAB). The MAB is constructed using 2:1 Multiplexors. On Instruction Reads the contents of the Location Counter is presented as the address to Main Memory. On all other memory operations the contents of the MAR is presented as the address for Main Memory. Data read from or written into memory is buffered in the Memory Data Register (MDR). The micro-program initiates a main memory cycle by using a Memory Read, Memory Write, or Instruction Read command. After issuing a memory command, the micro-program is free to perform other instruction. The memory cycle is accomplished asynchronous of other processor activity. If the micro-program, however, attempts to use the contents of MDR after a Memory Read or Instruction Read operation, before memory data become available, or attempts to load MDR or issue another Memory command before the current memory cycle is complete, the processor stops until the desired function can be performed.

Instruction Register (IR)

On Instruction Read operations data on the Memory Register Receive Bus (MRR), MRR Bits-0 through 7 are placed in the register labeled OP, Bits -8 through 11 are placed in the register labeled YD, and Bits-12 through 15 are placed in the register labeled YS. These three registers (OP, Yd, and YS) comprise the user's Instruction Register.

Decoder Read-Only Memory (DROM)

The OP register is used to address locations in the Decoder Read-Only-Memory (DROM). The DROM consists of two halves: DROM 1 and DROM 2. Each half contains 256 8-bit words. The micro-program interrogates either DROM 1 or DROM 2 at appropriate times and the 8 bits of the resulting read-out are jammed into the RAR, resulting in an automatic branch to an address that is related to the user's operation code. The most significant bit of DROM 1 is used to suppress unnecessary memory reads and Location Counter increments. The DROM also decodes all illegal user instructions.

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Micro Register (MR)

A 16-bit register labeled MR0 is available to the micro-program for general purpose use.

Input/Output (I/O)

Input/Output operations are achieved by gating S Bus data onto the I/O Bus and activating an I/O Control Line, or by activating an I/O Control Line and gating the I/O Bus data onto the B Bus.

LSI Micro-processor

The LSI Micro-processor is comprised of four Large Scale Integrated (LSI) Circuits, each of which is a 4-bit wide slice of the Central Processing Unit (CPU). Four of these CPU slices make up the 16-bit wide CPU. The combined slices contain a 16-bit Arithmetic Logic Unit (ALU), a two port Random Access Memory (RAM) Stack forming sixteen 16-bit General Registers, a 16-bit temporary storage register Q, shift circuits for right, left, and no shift for the RAM stack and Q register. By external circuits connecting the Q shift and RAM shift circuits 32-bit shifts and rotates are made possible with Q as one of the registers and one of the sixteen general registers as the second register.

It is most often the case that the micro-program accesses the User's General Register without caring which of the 16 General Registers is accessed. Consequently, no provision has been made in the Model 6/16 for the micro-program to randomly access an explicit General Register. Since after Instruction Read, one or more register addresses specified by the user instruction, are in the YD and YS register, the micro-program can access the appropriate General Register by specifying the YD or YS Register. The hardware then selects the General Register whose number is in the YD or YS Register.

The YD Register is an up/down-counter so that sequential General Registers can be accessed. The micro-program can also clear the YD Register when it needs to access a specific General Register.

MICRO-PROGRAM DESCRIPTION

Introduction

Micro-programming is a means for implementing the control logic of a digital processor. At INTERDATA, micro-programming has been effectively used to maintain upward program compatibility in a family of processors whose internal hardware varies from one member to the next.

The Model 6/16 Processor is designed to execute micro-instructions stored in a Control Store or Read-Only Memory (ROM). A micro-instruction is an elemental step or instruction to the actual hardware of the machine. Each micro-instruction causes one or more hardware functions to be performed, such as transferring the contents of one register to another, arithmetic or logical operations between two specified operands, controlling input/output operations or performing memory functions.

A series of micro-instructions is called a micro-program. The complete Model 6/16 micro-program is, by definition, an emulator, causing the Model 6/16 to react to a user program in main memory and to external events as does the Model 7/16 Processor, described in the *INTERDATA 16-Bit Reference Manual,* Publication Number 29-398. Every user level instruction, interrupt handling feature, etc. is simulated by some portion of the Model 6/16 Processor micro-program.

The following pages outline the Model 6/16 hardware from a micro-programmer's point of view, data and instruction formats, instruction repertoire and interrupt system.

DATA AND INSTRUCTION FORMATS

Data Formats

All internal data paths are 16-bits wide. Hence the basic machine operand is a 16-bit halfword. In arithmetic operations, the most significant bit is interpreted as the sign bit of the number in the least significant 15 bits of a halfword: Positive fixed-point data is expressed in true binary form with a sign bit of Zero. Negative fixed-point data is expressed in twos complement notation with a sign bit of One.

Binary information is represented in hexadecimal notation, base 16, for simplicity.

Instruction Formats

Model 6/16 Processor micro-instructions can be one of five formats designated Register-to-Register, Register-to-Immediate, Input/Output, Branch and Exchange Byte. The Instruction word formats are shown in Table 1 and Figure 2. Instruction word fields are explained in the following sections. (Refer to Table 2.)

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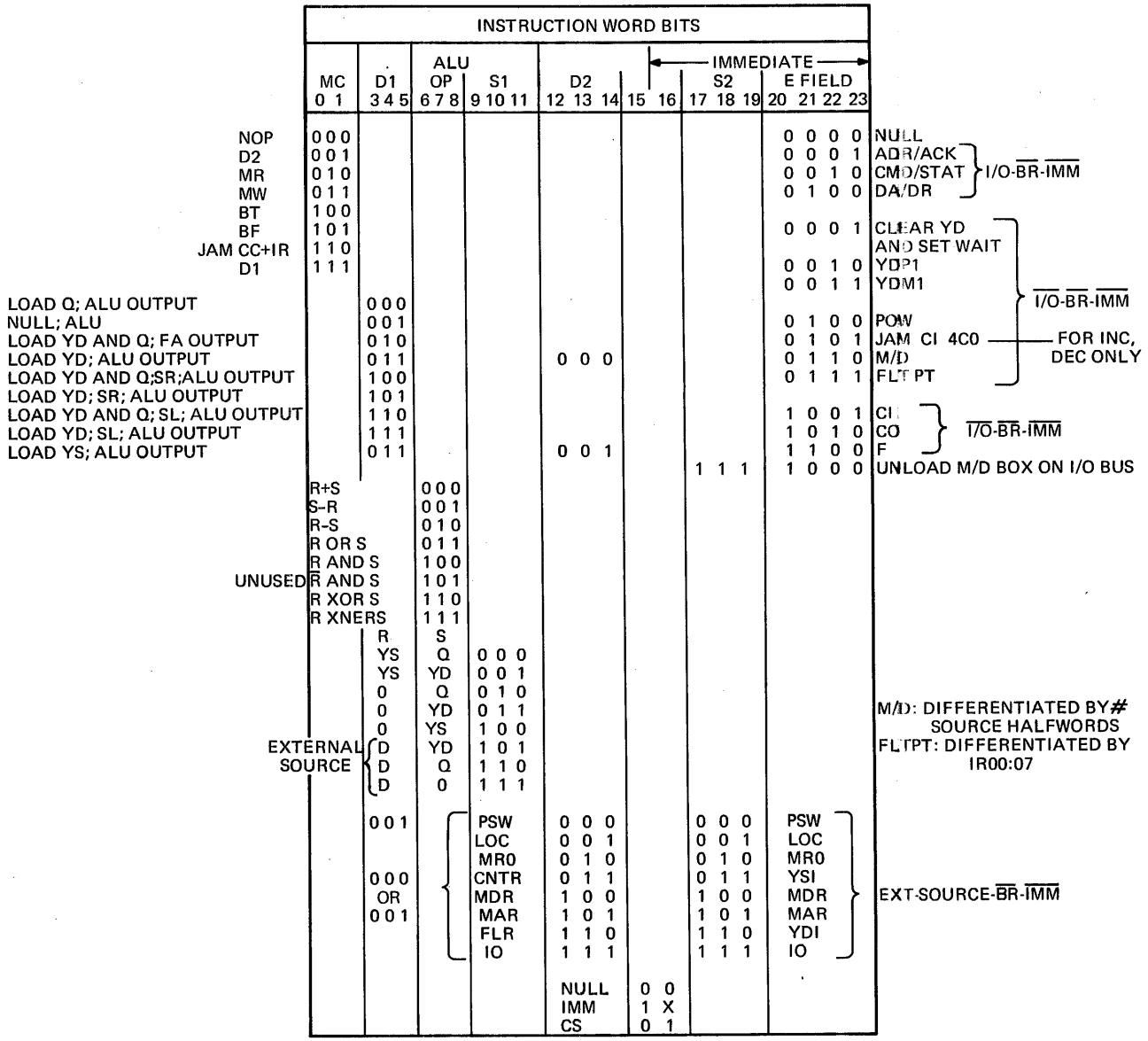
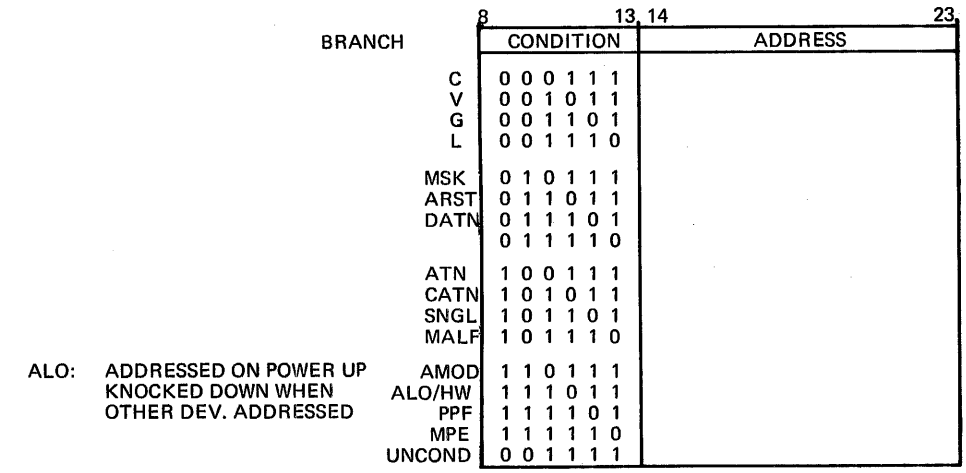
TABLE 1. INSTRUCTION WORD CHART





ALO: ADDRESSED ON POWER UP
KNOCKED DOWN WHEN
OTHER DEV. ADDRESSED

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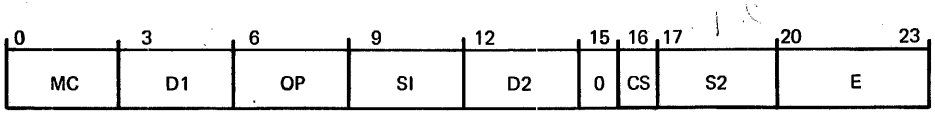
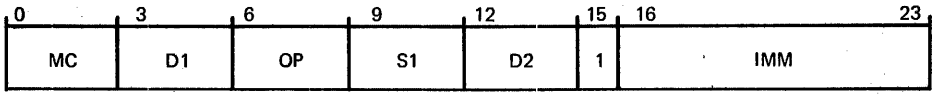
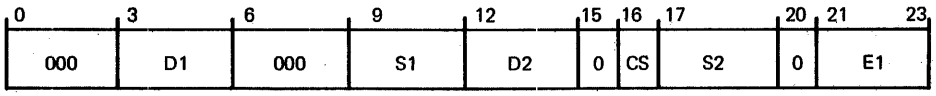
REGISTER TO REGISTER



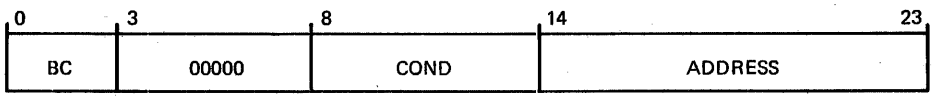
REGISTER TO IMMEDIATE



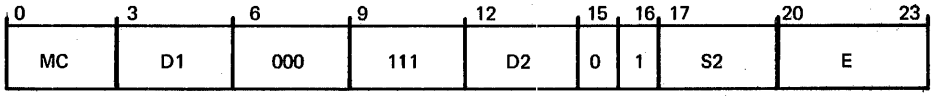
INPUT/OUTPUT



BRANCH



EXCHANGE BYTE



INSTRUCTION WORD FIELDS

FIELD	MEANING
MC/BC	MAIN MEMORY CONTROL/BRANCH CONTROL
D1	SHIFT LEFT/SHIFT RIGHT OPERATION
D1 AND D2	DESTINATION FIELD
OP	ALU OPERATION
S1	SELECTS TWO SOURCES FOR ALU
S2	SELECT EXTERNAL (TO ALU) SOURCE
E	EXTENSION FIELD
E1	SPECIFIED TYPE OF I/O OPERATION
COND	BRANCH CONDITION(S)
ADDRESS	BRANCH ADDRESS
CS	SPECIFIES CROSS-SHIFT

Figure 2. Instruction Word Formats

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Memory Control (MC)

The processor's main memory is the source of user's instructions and data. The Register-to-Register and Register-to-Immediate micro-instructions can specify one of the following options to perform main memory operations or to use the Decoder Read-Only-Memory (DROM).

TABLE 2. MC/BC FIELD

Instruction Word Bits 0 1 2	Meaning
000	No operation
001	D2—Vector through DROM2
010	MR—Data Read Halfword
011	MW—Data Write Halfword
100	BT—Branch on True Condition
101	BF—Branch on False Condition
110	IR—Instruction Read and Jam CC
111	D1—Vector through DROM1

D2: The user's instruction op-code, IR (0:7), is used to vector through DROM2. The unique word from DROM2 is jammed into RAR, causing a branch in the micro-program sequence.

MR: A main memory read operation is started using the contents of MAR as the memory address. Then the micro-instruction execution starts. The halfword is read from memory and is loaded into this MDR for use by the micro-program when the data is available.

MW: A Main Memory Write operation is started. The current content of MDR is written into the halfword of memory currently addressed by the content of MAR.

BT: If any of the specified conditions are true, a branch is taken to the address specified in the address field.

BF: If all of the specified conditions are false, a branch is taken to the address specified in the address field. An unconditional branch micro-instruction assembles as a branch on false micro-instruction with no conditions specified.

IR: An Instruction Read operation is started prior to execution of the current micro-instruction. The halfword addressed by the current contents of LOC is read and placed in both the MDR and the Instruction Register (IR). LOC is then incremented by two and the incremented LOC is jammed into the MAR. The current content of FLR is copied into the condition code field of PSW. (LOC must not be the destination register in the micro-instruction specifying the IR option.) The FLR is cleared and the micro-instruction at ROM location '000' is executed.

D1: The address of the next micro-instruction is extracted from DROM1 using the user's instructions op-code, IR (0:7), as an index.

Commands (E)

A Register-to-Register or Exchange Byte micro-instruction can specify one of the following six commands to perform the desired hardware function. These commands are executed at the end of the micro-instruction.

Word Word Bits				Meaning	
20	21	22	23		
0	0	0	1	CYD and SWA	Clear YD field and set Wait FF
0	0	1	0	YDP1	Increment YD field
0	0	1	1	YDM1	Decrement YD field
0	1	0	0	POW	Power down, Generate System Clear
0	1	1	0	M/D	Load data into M/D box
0	1	1	1	FLTPT	Specify Floating Point operation

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Condition Code Options (E)

A Register to Register or Exchange Byte micro-instruction can specify up to three options in this category.

Instruction Word Bits				Meaning	
20	21	22	23		
1	0	0	1	CI	Carry In
1	0	1	0	CO	Carry Out
1	1	0	0	F	Set Test Flags in FLR

CI: In a Load micro-instruction specifying this option, the Carry Flag (P/O FLR) is shifted into the most significant bit of the result if Shift Right is also specified. If Shift Left is specified, the Carry Flag is shifted into the least significant bit of the result. While executing an Add micro-instruction, the Carry Flag is added to the least significant bit of the sum.

In a subtract micro-instruction, the Carry Flag represents a borrow situation from the least significant bit of the subtraction. This borrow participates in the subtraction operation.

CO: In a Load micro-instruction specifying this option, the Carry Flag in FLR stores the bit shifted out, if a Shift Right or Shift Left is also specified. If shift is not specified, the Carry Flag is reset.

In an Add micro-instruction, the Carry Flag is set if a carry is generated. In the subtraction, carry is reset if a borrow is not generated. If a micro-instruction specifying CO performs a logical operation, the Carry Flag in FLR is reset.

F: If a micro-instruction specifying this option performs addition or subtraction, V, G and L Flags in FLR are adjusted to reflect the result of the operation. The V Flag reflects the overflow condition and Flags G and L reflect the algebraic value of the result.

In an I/O instruction, the V Flag is set if the addressed device does not return a SYNC in approximately 14 microseconds. If a micro-instruction specifying this option performs a load or logical operation, the V Flag is reset and the G and L Flags are adjusted to reflect the algebraic value of the result.

The hardware provides a cumulative flag effect to facilitate multi-precision operations. The following table shows how the G and L Flags in FLR are adjusted to reflect the algebraic value of the result. Note that once the G or L Flag becomes set, the G and L Flags will never again both be Zero unless the FLR is explicitly cleared (e.g., an Instruction Read operation).

Result	Flags before Execution		Flags after Execution	
	G	L	G	L
Zero	0	0	0	0
	0	1	1	0
	1	0	1	0
Positive	0	0	1	0
	0	1	1	0
	1	0	1	0
Negative	0	0	0	1
	0	1	0	1
	1	0	0	1

Shift Options

A Register-to-Register or Register-to-Immediate micro-instruction can specify either the Shift Left or Shift Right option. There are no specific bits in the micro-instruction word for the SL or SR options. However, this information is included in Bits-3, 4 and 5. The micro-instruction must specify YD or YD&Q as the destination register or registers. Other desired options may be specified.

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SL: The 16-Bit Arithmetic Logic Unit result is shifted left one bit position. If CI is also specified, the state of the Carry Flag in FLR is shifted into the least significant bit position, otherwise, the least significant bit is forced to Zero. If CO is also specified, the most significant bit of the ALU result, which is shifted out, is shifted into the Carry Flag of the FLR; otherwise, that bit is lost. The 16-bit result thus obtained is copied into the destination register or registers.

SR: The 16-bit ALU result is shifted right one bit position. If CI is also specified, the state of the Carry Flag in FLR is shifted into the most significant bit position; otherwise, the most significant bit is forced to Zero. If CO is specified, the least significant bit of the ALU result, which is shifted out, is shifted into the Carry Flag of FLR; otherwise, that bit is lost. The 16-bit result, thus obtained, is copied into the destination register or registers.

Branch Conditions

A Branch micro-instruction can specify up to four conditions from Group 0, Group 1, Group 2 or Group 3. Conditions from different groups cannot be mixed in the same instruction. The micro-instruction word bits, symbolic conditions and their meanings are shown below.

GROUP	WORD BITS 8 9 10 11 12 13	SYMBOLIC CONDITION	MEANING OF TRUE CONDITION
0	0 0 0 1 1 1	C	CARRY FLAG SET
	0 0 1 0 1 1	V	OVERFLOW FLAG SET
	0 0 1 1 0 1	G	GREATER THAN ZERO FLAG SET
	0 0 1 1 1 0	L	LESS THAN ZERO FLAG SET
	0 0 1 1 1 1		UNCONDITIONAL BRANCH
1	0 1 0 1 1 0	MSK	(YD) AND (CONDITION CODE FIELD) 0
	0 1 1 0 1 1	ARST	AUTO-RESTART PRESENT
	0 1 1 1 0 1	DATN	DMA ON I/O BUS IS REQUESTING ATTENTION
2	1 0 0 1 1 0	ATN	I/O ATTENTION AND PSW BIT 1 ARE SET OR DMA ON I/O BUS IS REQUESTING ATTENTION
	1 0 1 0 1 1	CATN	CONSOLE ATTENTION REQUESTED
	1 0 1 1 0 1	SNGL	CONSOLE IS IN SINGLE MODE
	1 0 1 1 1 0	MALF	MACHINE MALFUNCTION DETECTED
3	1 1 0 1 1 1	AMOD	ADDRESS MODIFICATION IS NECESSARY
	1 1 1 0 1 1	HW	HALFWORD I/O LINE IS ACTIVE/ALO PRESENT INDICATION ON POWER UP
	1 1 1 1 0 1	PPF	PRIMARY POWER FAIL DETECTED
	1 1 1 1 1 0	MPE	MEMORY PARITY ERROR DETECTED

THE MICRO-PROGRAM

The Model 6/16 Processor micro-program can be divided into three major functional areas. These are: user instruction fetch; user instruction execution; and interrupt support. Refer to Figure 3.

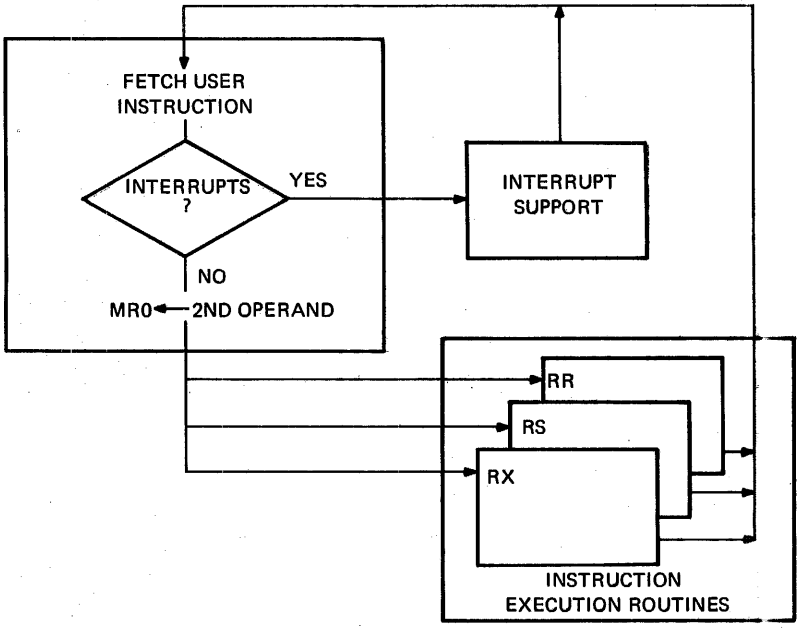

Figure 3. Micro-Program Functional Areas

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System Initialization

On power up, or following initialize, when the System Clear signal (SCLR0) goes high, the Processor starts executing micro-instructions. SCLR0 presets the ROM Address Register (RD) to X'100'.

Referring to Figure 4, address X'100' corresponds to the symbolic label PWRUP on the flow chart.

The micro-program checks if Automatic Loader Option (ALO) is present. If the ALO exists, the HW line is active. The test for HW passes and routine ALO1 is entered. If the HW test fails, the micro-program continues the normal power-up sequence.

NOTE

The Automatic Loader Option (ALO) is a halfword oriented device but it does not have a specific device address. If it is present in the system and enabled then on power-up or initialize, the HW line is activated. The micro-program detects this and loads new PSW and LOC and up to 4K bytes of main memory from the ALO. Depending on the new PSW, the user level Processor goes into the Wait State or user instruction execution starts.

In the Auto Load Option route (AL01), the micro-program reads in a new PSW and LOC, a starting Memory Address and an ending Memory Address from the ALO. The micro-program then forms in YD the difference between the ending address and the starting address. If a carry is produced, the end address was less than the start address. Routine IDLE is entered. If the end address is not less than the start address, the data input loop, AL02, is entered. The data halfwords are read from the ALO and stored in consecutive halfword locations in main memory until the difference count in YD is decremented from X'000' to X'FFFF'. When this happens, all the data has been loaded into Main Memory. Then Bit-0 of the PSW (Wait Bit) is tested. If it is set WAIT routine is entered. Otherwise, user instruction fetch is started. (See Figure 5.)

In the normal power-up sequence, the PSW and LOC are restored from their power fail save locations, X'0024' and X'0026' in main memory, and the user's General Registers are restored from their main memory power fail save locations. The General Register save area is a 32-byte block of memory whose starting address is contained in memory location X'0022'.

After restoring the registers, Bits-13, 14, and 15 of location X'20' are examined to determine the last display panel status. If non-Zero, the Hexadecimal Display Panel was not in the Run mode when power went down. LOCDIS is entered. If Zero, the Hexadecimal Display Panel was in the Run mode. The Auto-Restart, ARST, option is tested. If set, routine MMF is entered to do the Machine Malfunction interrupt if PSW Bit-2 is set. If the ARST option is absent, routine LOCDIS is entered to display the present values of the location Counter. The IDLE loop is then entered.

Hexadecimal Display Panel Support

The Hexadecimal Display Panel is serviced by two major routines: CONSER and DISPLY. Routine CONSER is entered, if during user instruction execution, the micro-program determines that CATN is active; or if in the IDLE loop or the WAIT loop, CATN becomes active but SNGL is not active. See Figure 6.

In the CONSER routine, the Display Controller is addressed and its status is sensed. It is put into the normal mode and addressed to reset byte counter. The most significant four bits of the status byte are stored as the least significant four bits of location X'20'. If the SNGL signal is active, the LOC is incremented by two, the FLR is cleared and the micro-program returns to the user instruction fetch routine at START 1. If SNGL is not active, the Hexadecimal Display status is examined.

If status Bit-1 is set a function or a register has been selected. Routine FNREG is entered. If status Bits-0, 4, 5, 6 and 7 are all reset, Function 0 was selected. If PSW Bit-4 is also set, the micro-code simulates an interrupt from device number 1 (Hexadecimal Display Panel Interrupt). If PSW Bit 4 is reset, routine CLRWT is entered to fetch the next user instruction.

If status Bit-1 is reset, MDR gets data from memory location specified by LOC. If the Display status indicates Address or Memory Write, routine ADWRT is entered. The Switch Register is read into MDR and if the mode is Address, routine ADD is entered; where the data in MDR is copied to LOC and routine LOCDIS is entered. If the mode is Memory Write, routine RDKEY is entered, where the data in MDR is written to the memory location specified by LOC. LOC is then incremented by two and copied to MAR. The data written is copied into MR0 and MDR is set equal to X'80' to light the Memory Address/Memory Data lamp. Routine OUTDIS is entered.

If the mode is Memory Read, the RDKEY routine is entered.

Display status Bits-1, 2, and 3 being reset indicate Run mode. Routine CLRWT is entered to fetch the next user instruction.

Routine DISPLY is entered from routine CONSER if the status indicates that a function other than Function 0 or a Register was selected; or before the interruptable Wait loop is entered, if SNGL is active. See Figure 7.

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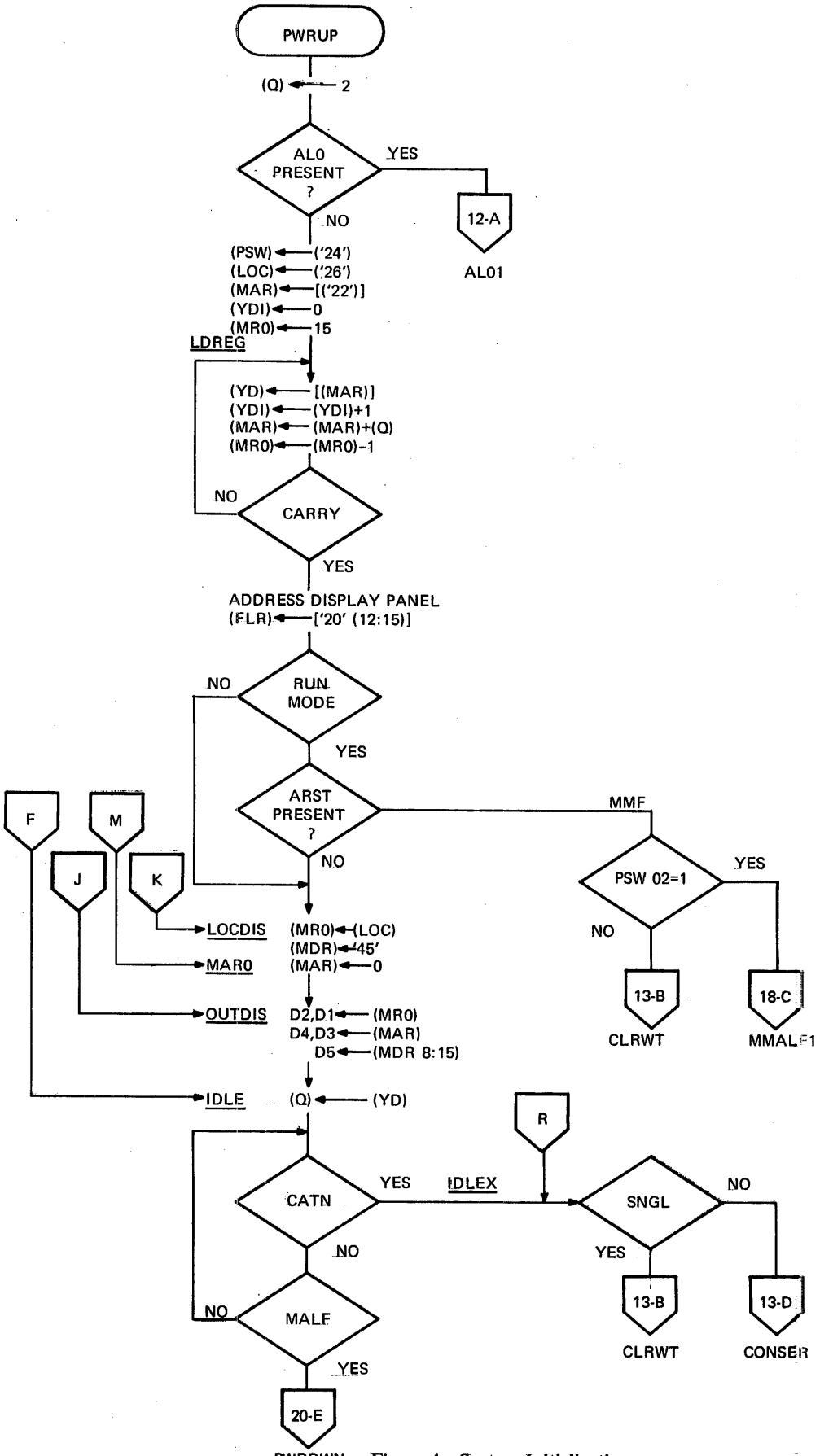

Figure 4. System Initialization

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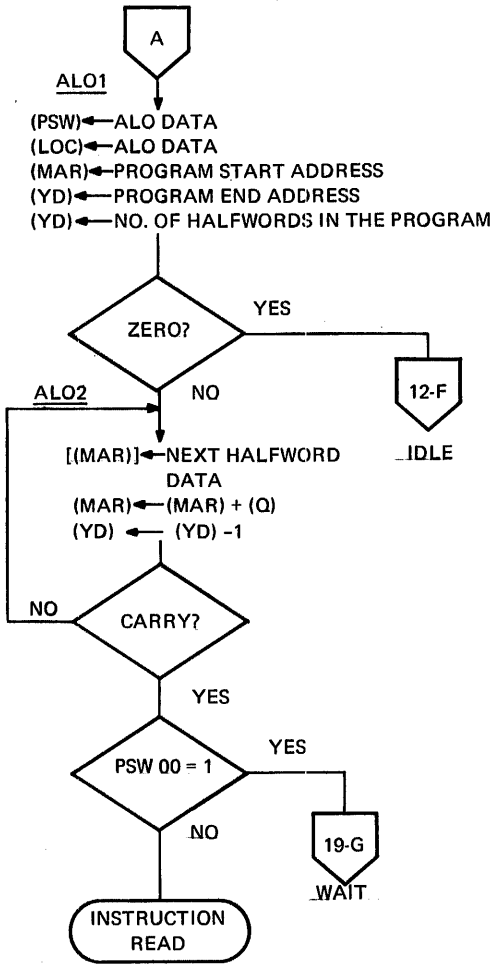

Figure 5. Auto Load Option

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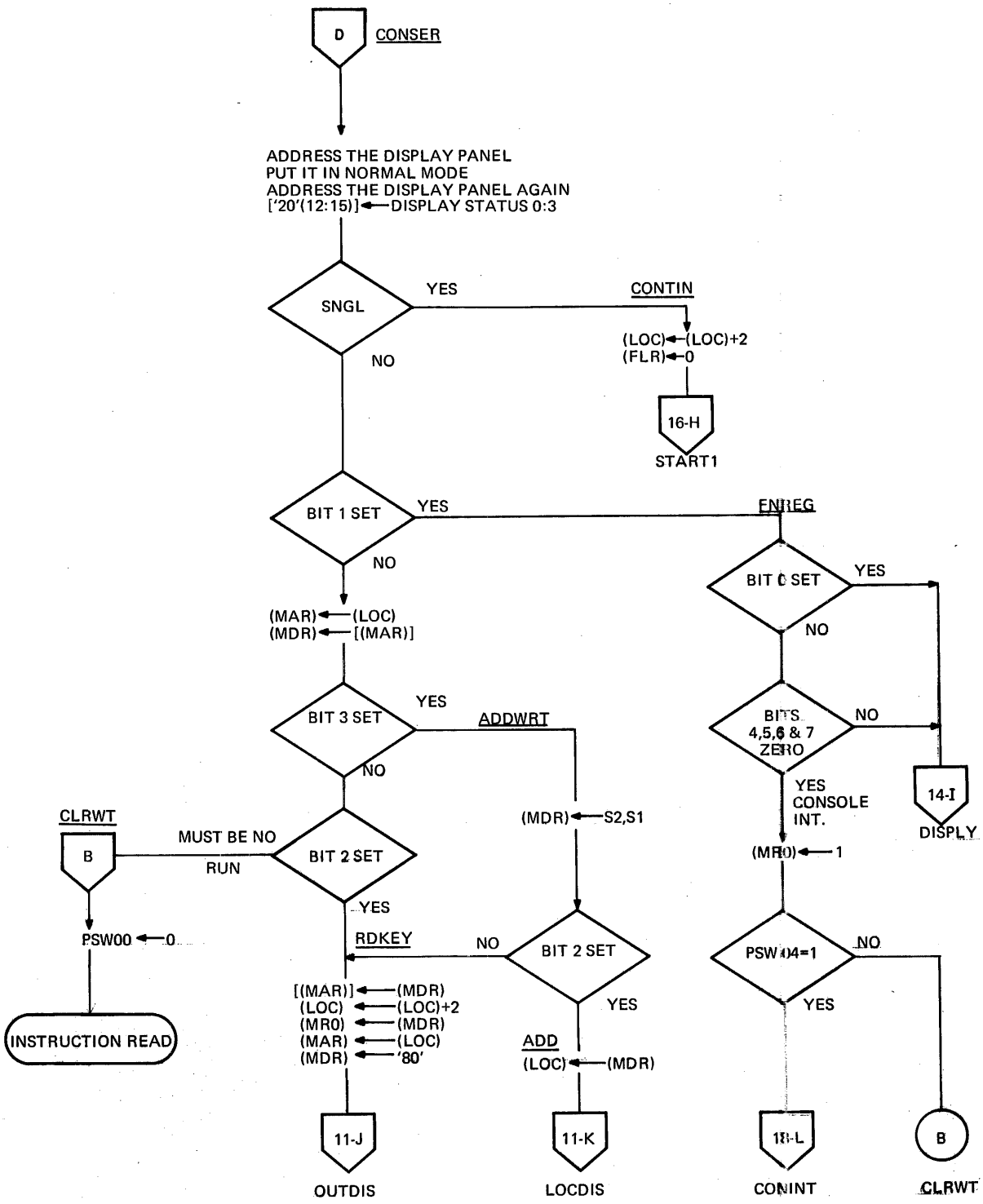

Figure 6. Routine CONSER

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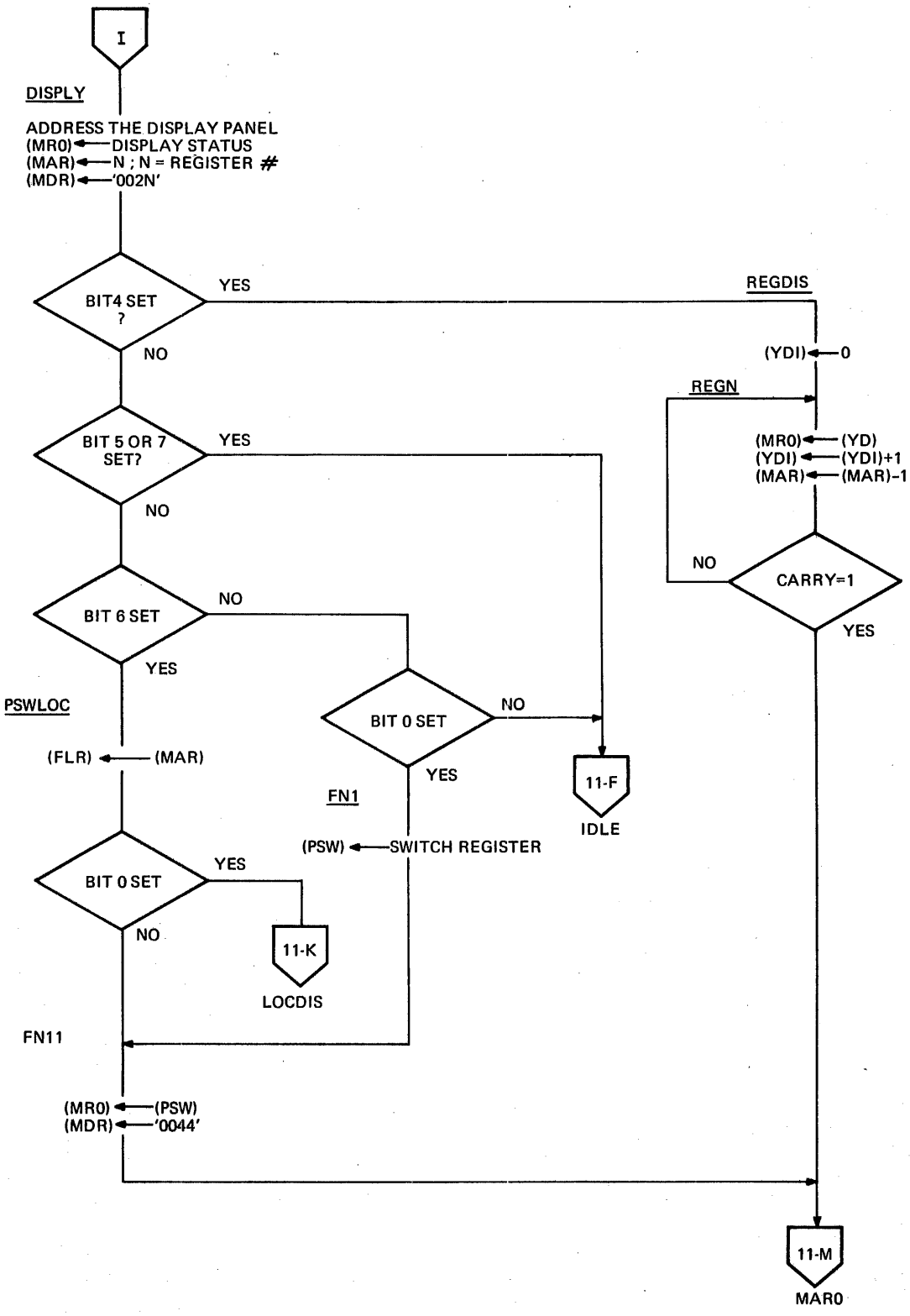

Figure 7. Display Routine

This information is proprietary and is supplied by INTERDATA for the sole purpose of using and maintaining INTERDATA supplied equipment and shall not be used for any other purpose unless specifically authorized in writing.

In the DISPLY routine, the Display Controller is addressed and its status is sensed. Then the register number n is obtained in MAR and MDR is set equal to X'2n'. If a General Register is selected, routine REGDIS is entered. If Function codes 4 or 5 are indicated, routine PSWLOC is entered. If Function code 1 is indicated, routine FN1 is entered. Otherwise, the uninterruptable IDLE loop is entered.

At REGDIS, the YD field is cleared and incremented until it equals the register number specified by MAR. The specified General Register is copied to MR0. Routine MAR0 is then entered.

At PSWLOC, status Bit-0 is examined to differentiate between Functions 4 and 5. If status Bit-0 is set, the Function 5 is indicated and routine LOCDIS is entered. Otherwise, the PSW is copied to MR0, and MDR is set equal to X'44', and the MAR0 routine is entered.

At FN1, the switch register data is copied into PSW and a branch is taken to FN11.

Routine LOCDIS copies LOC to MR0, sets MDR equal to X'45' and clears MAR. Routine OUTDIS is then entered.

Routine OUTDIS outputs the five bytes contained in MDR8:15, MAR and MR0 to the Display Controller. Then the uninterruptable IDLE loop is entered.

The IDLE loop is a high speed loop that can only be exited if a power failure occurs or a CATN is detected.

Instruction Fetch

A user's Instruction Fetch begins when a micro-instruction specifying Instruction Read is performed. The hardware sets the ROM Address Register to '000', which corresponds to the label START on the flowchart, see Figure 8. If any interrupts are pending, the micro-program branches to routine HELP. If no interrupts are pending, the LOC is incremented by two. The hardware copies the instruction word from MDR into the Instruction Register (OP, YD, and YS). The General Register specified by YS is loaded into MR0 and Q and DROM1 is interrogated. If the most significant bit of DROM1 is false, a memory read is initiated from the address specified by the new contents of LOC, and LOC is incremented by two. If this bit is active (RR type user instructions), no memory read occurs.

Depending on the user's operation code, DROM1 supplies an appropriate address to resume micro-code execution. If the user's operation code is not legal, the DROM1 sets the ROM Address Register to 082 causing a branch to routine ILEG. There, the LOC is decremented by two, the MAR is set to 0030 and routine GENSWP is entered.

User Instructions Emulation

The ROM address supplied by DROM1, in a way, categorizes the user instructions into those that require operand set-up and those that do not. Table 3 shows the legal instruction mnemonics and the corresponding symbolic ROM address for DROM1. For those instructions that do not require any operand set-up, the micro-program goes directly to the appropriate execution routine via DROM1 and DROM2 is not used. For those instructions that do require pre-processing, DROM 2 is interrogated to get the starting address of the execution routine. Table 4 shows the legal instruction mnemonics and the corresponding symbolic ROM addresses for DROM2.

Interrupt Support

During user Instruction Fetch, the micro-program tests for interrupts. If any of the tested interrupts (MALF, ATN, CATN, SNGL) are active, routine HELP is entered, and LOC is decremented by two. See Figure 9.

Machine Malfunction

If MALF is active, routine MMALF is entered. MALF can be caused by Memory Parity Error or Early Power Fail if PSW Bit-2 is set; or by Primary Power Fail. At routine MMALF, if the Primary Power Fail signal is active, Routine PWRDWN is entered. There, the PSW and LOC are stored in their core memory save locations and the user's General Registers are saved in the area of core whose starting address is contained in location X'0022'. The command Power down (POW) micro-instruction is then performed which stops the processor and deactivates the initialize (SCLR) relay.

If Primary Power Fail was not causing MALF, the micro-program checks for CATN. This test allows microprogram to exit from a continuous repetition of machine malfunction PSW swap because of repetitive memory parity error. If CATN test fails, the micro-program does a Machine Malfunction PSW swap with location X'0038'. Routine GENSWP, the common PSW swap routine, is discussed later.

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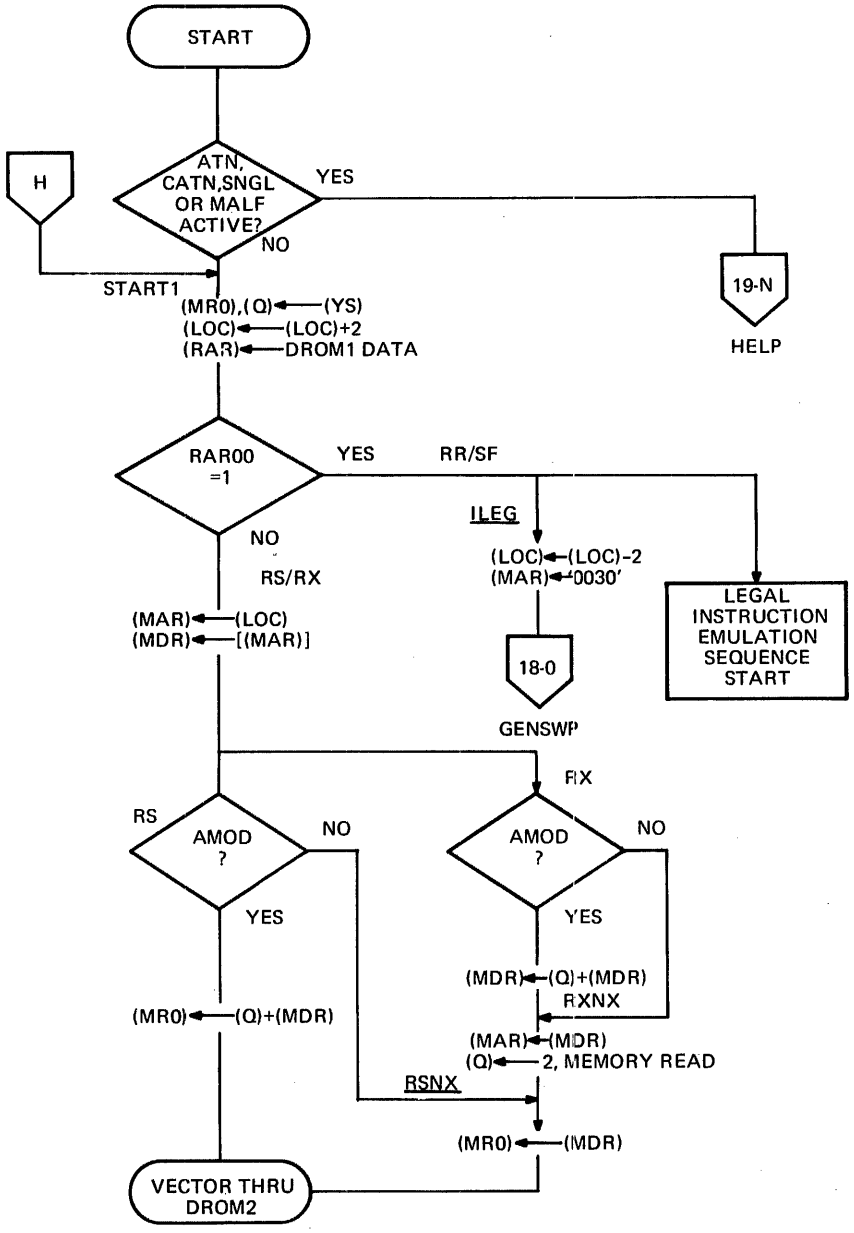

Figure 8. Instruction Fetch

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TABLE 3. DROM–1 DATA

	00		20		40		60		80		A0	C0		E0	
0		ILEG	BTBS	BTS	STH	RS		ILEG		ILEG	ILEG	BXH	BX		ILEG
1	BALR	BALR	BTFS		BAL		AHM	RX				BXLE	BX	SVC	RS
2	BTCR	BTCR	BFBS	BFS	BTC			ILEG				LPSW	RX	SINT	RS
3	BFCR	BFCR	BFFS		BFC							THI	RS		ILEG
4	NHR	NHR	LIS	IMM	NH	RX						NHI			
5	CLHR	CLHR	LCS	LCS	CLH							CLHI			
6	OHR	OHR	AIS	IMM	OH							OHI			
7	XHR	XHR	SIS		XH							XHI			
8	LHR	LHR		ILEG	LH							LHI			
9	CHR	CHR			CH							CHI			
A	AHR	AHR			AH							AHI		RRL	SLL
B	SHR	SHR			SH							SHI		RLL	
C	MHR	MHR*			MH	RX*						SRHL	SLHL	SRL	
D	DHR	DHR*			DH	RX*						SLHL		SLL	
E	ACHR	ACHR			ACH	RX						SRHA	SLHA	SRA	SLA
F	SCHR	SCH			SCH	RX						SLHA		SLA	
0		ILEG		ILEG		ILEG			SRLS	SLLS		STM	LMSTM		ILEG
1									SLLS			LM			
2									STBR	STBR		STB	RX		
3									LBR	LBR		LB			
4									EXBR	EXBR		CLB			
5									EPSR	EPSR		AL	AL		
6									WBR	RBRWBR		WB	RBWB		
7									RBR			RB			
8									WHR	IORR		WH	IORX		
9									RHR			RH			
A									WDR			WD			
B									RDR			RD			
C									MHUR	MHUR*		MHU	RX*		
D									SSR	IORR		SS	IORX		
E									OCR			OC			
F									AIR	AIR		AI	AI		

* FOR M/D OPTION ONLY, OTHERWISE IT IS ILEG

TABLE 4. DROM–2 DATA

	00		20		40		60		80		A0	C0		E0	
0		0	BTBS	BKWORD	STH	STH		0		0	0	BXH	BXH		0
1	BALR		BTFS	FRWORD	BAL	BALR	AHM	AHM				BXLE	BXLE	SVC	SVCD2
2	BTCR		BFBS	BKWORD	BTC	BTCR		0				LPSW	LPSW	SINT	SINT
3	BFCR		BFFS	FRWORD	BFC	BFCR						THI	THI		0
4	NHR		LIS	LHR	NH	NHR						NHI	NHR		
5	CLHR		LGS	0	CLH	CLHR						CLHI	CLHR		
6	OHR		AIS	AHR	OH	OHR						OHI	OHR		
7	XHR		SIS	SHR	XH	XHR						XHI	XHR		
8	LHR			0	LH	LHR						LHI	LHR		
9	CHR				CH	CHR						CHI	CHR		
A	AHR				AH	AHR						AHI	AHR	RRL	RRLD2
B	SHR				SH	SHR						SHI	SHR	RLL	RLLD2
C	MHR				MH	MHR*						SRHL	SRHLD2	SRL	SRLD2
D	DHR				DH	DHR*						SLHL	SLHLD2	SLL	SLLD2
E	ACHR				ACH	ACH						SRHA	SRHAD2	SRA	SRAD2
F	SCHR				SCH	SCH						SLHA	SLHAD2	SLA	SLAD2
0						0			SRLS	SRHLD2	0	STM	STM		0
1						0			SLLS	SLHLD2		LM	LM		
2						0			STBR	NOB		STB	STB		
3						0			LBR	0		LB	LB		
4						0			EXBR	NOB		CLB	CLB		
5						0			EPSR	0		AL	RBR		
6						0			WBR	WBR		WB	WBR		
7						0			RBR	RBR		RB	RBR		
8						0			WHR	WHR		WH	WHR		
9						0			RHR	RHR		RH	RH		
A						0			WDR	WDR		WD	WD		
B						0			RDR	RDR		RD	RD		
C						0			MHUR	0		MHU	MHUR*		
D						0			SSR	SSR		SS	SS		
E						0			OCR	OCR		OC	OC		
F						0			AIR	SSR		AI	SS		

* FOR M/D OPTION ONLY, OTHERWISE IT IS 0

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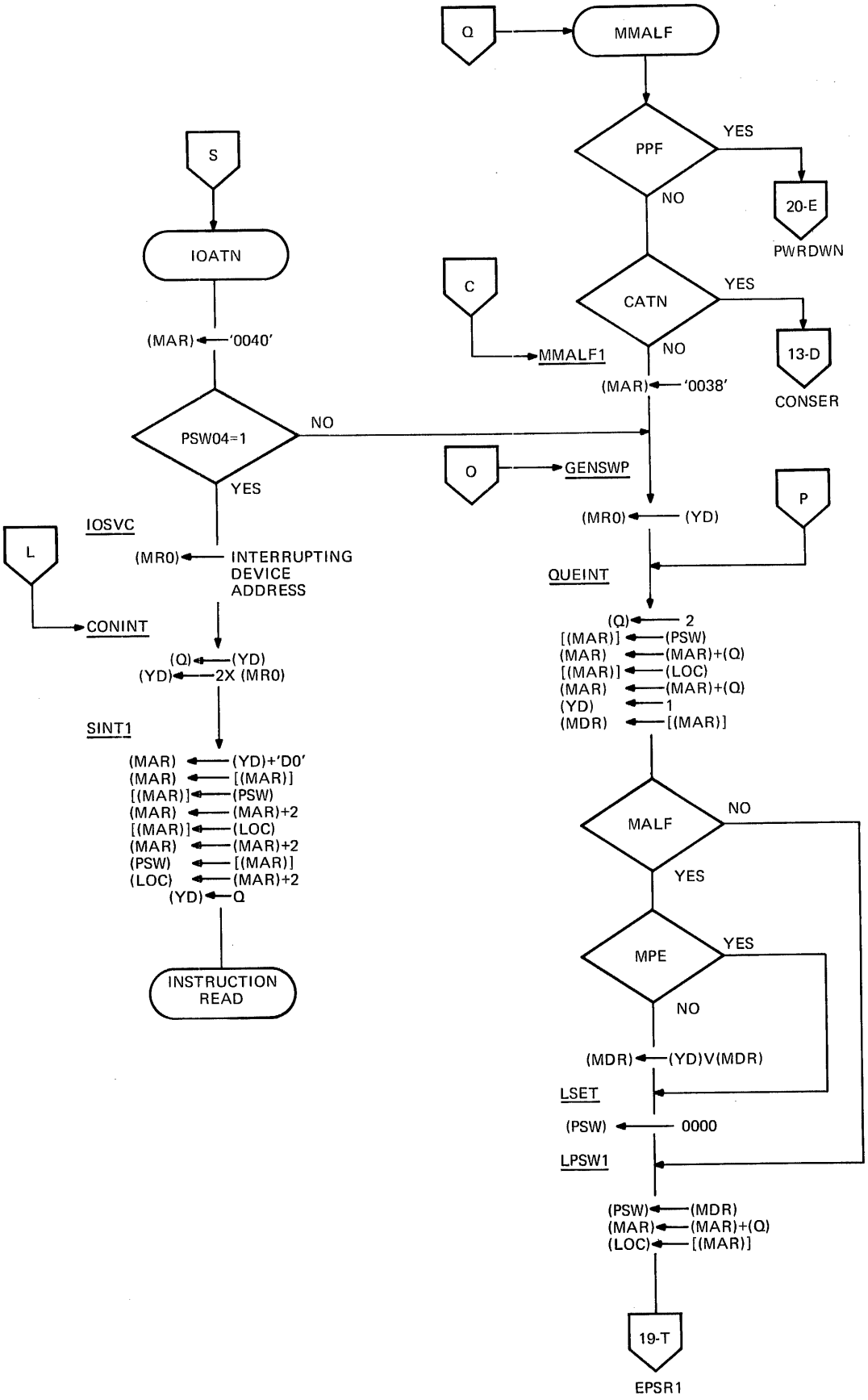

Figure 9A. Interrupt Support

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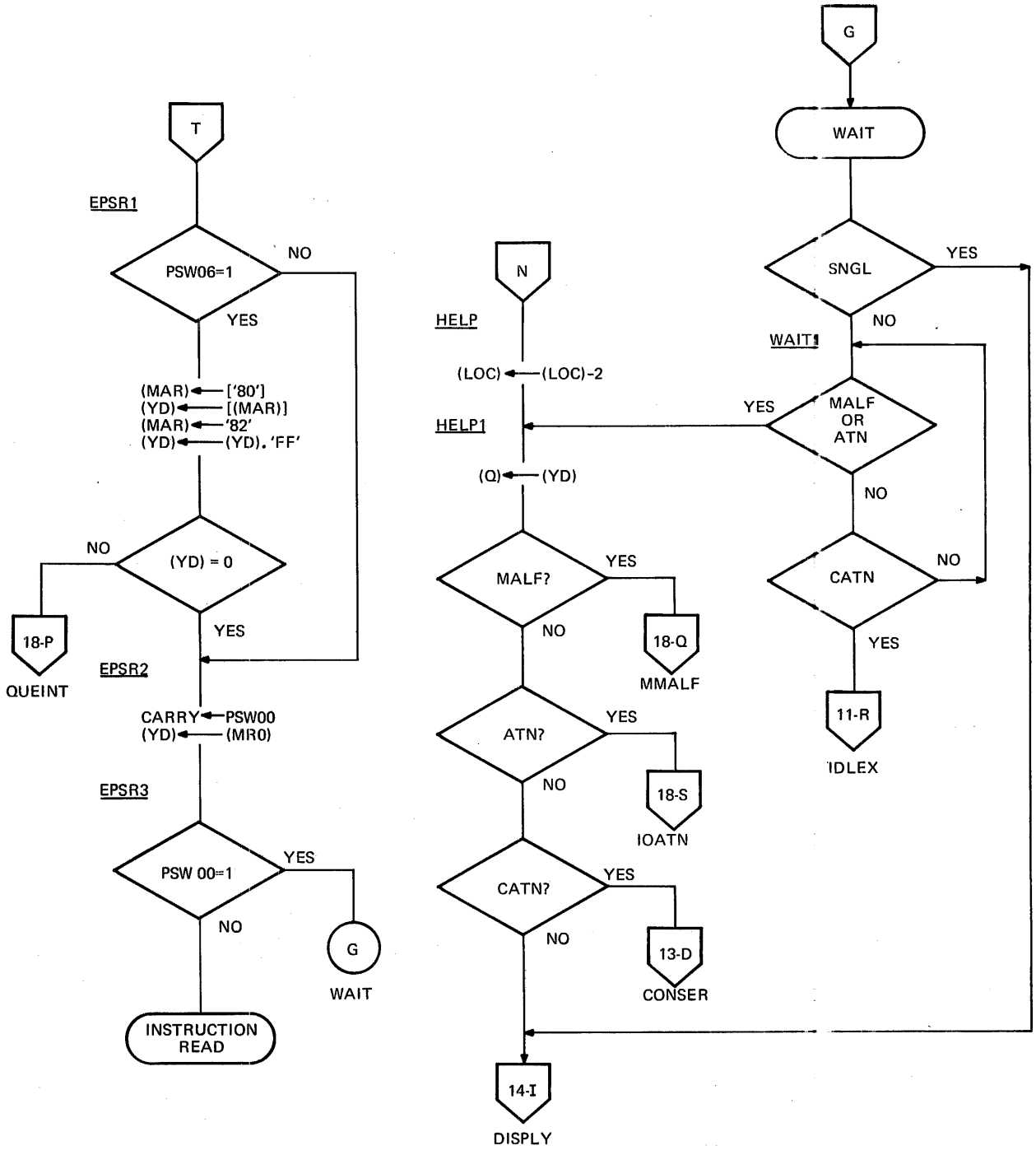

Figure 9A. (Continued) Interrupt Support

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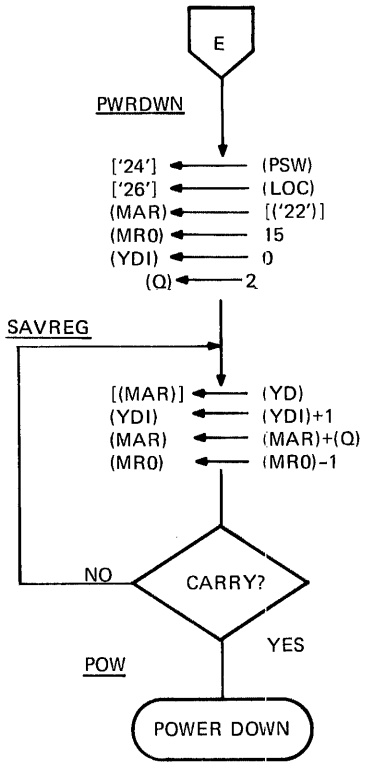

Figure 9B. Power Down Routine

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I/O Attention

If MALF is not active, the micro-program tests for I/O attention (ATN). If ATN is active, the IOATN routine is entered. In IOATN routine, if DATN is active, IODMA routine is entered; otherwise, PSW bit 4 is tested. If PSW Bit-4 is set, routine IOSVC is entered; otherwise, a PSW swap is performed with location X'0040'.

In IODMA routine, device zero is addressed to knock down any addressed device. Then one halfword is read from the DMA on I/O Bus. This halfword is the start memory address for the requested data transfer. If memory address is odd, DMARD routine is entered, where halfwords are read from the DMA device and stored in consecutive memory halfwords. If memory address is even, DMAWRT routine is entered, where consecutive halfwords from the start memory address are written to the DMA device. A DMA device must be a halfword oriented device. The DMARD or the DMAWRT routine is exited when DATN is dropped. The next user instruction is then fetched.

Routine IOSVC acknowledges the I/O interrupt. The returned device number times two is used to index into the Service Pointer table beginning at core location X'00D0'. The halfword contained in the selected location is fetched and placed in MAR. The micro-program then stores the PSW in the location whose address is (MAR) and the LOC in the location whose address is (MAR)+2. The contents of the location whose address is (MAR)+4 is fetched and placed in the PSW, LOC is set equal to (MAR)+6, and the user instruction now pointed to is fetched and executed.

Console Attention

If neither MALF nor ATN is active, the micro-program tests for Console Attention (CATN). If not active, the interrupt must have been SNGL, and routine DISPLY is entered. There, the selected register or registers are output to the Display Console and the Idle loop is entered.

If CATN is active, routine CONSER is entered. There, the Display Console is addressed, which resets the CATN indication. If SNGL is also active, the micro-program continues the user instruction emulation. When the next user instruction fetch begins, CATN is inactive and SNGL is active, causing routine DISPLY to be entered.

Routine GENSWP

Routine GENSWP is the common PSW swap routine, entered with MAR containing the address of the swap area. The PSW is stored in the location whose address is (MAR). LOC is stored in the location whose address is (MAR)+2. The PSW is loaded with the contents of the location addressed by (MAR)+4. The L flag in the new PSW is set to 1 if the PSW swap is due to an Early Power Fail. LOC is then loaded from location (MAR)+6.

If Bit-6 of the new PSW is set, the micro-program examines Bits-8:15 of the halfword whose address is in location X'0080'. If this byte is non-Zero, another PSW swap is performed with location X'0082'. If Bit-6 of the new PSW is not set, the micro-program tests PSW Bit-0. If not set, user instruction execution begins with the instruction specified by LOC. If Bit-0 is set, the interruptable WAIT loop is entered. The WAIT loop tests for MALF, ATN, or CATN. If any interrupt occurs, routine HELP is re-entered.

Interrupt System

The interrupt structure provides rapid response to external and internal events that require special software attention. The descriptions that follow are oriented towards the emulator.

Internal Interrupts

Five different internal interrupts may be generated. Of these, the Illegal Instructions, Fixed-Point Divide Fault, Queue Service, and Supervisor Call Interrupts are created by the Emulator, and the Machine Malfunction Interrupt is generated in the hardware.

Illegal Instruction Interrupt

The illegal instruction interrupt occurs when an instruction not in the user's repertoire is fetched. Table 5 shows the Model 6/16 user's instruction repertoire. All 256 combinations of Op Codes are available in the DROM. For illegal Op-Codes, the data in DROM1 equals '082', starting address of Illegal Instruction interrupt micro-routine. In case of illegal op-codes, when DROM1 is interrogated, a branch to ILEG routine occurs where an Illegal Instruction PSW swap, location X 30 , is performed.

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TABLE 5. USER'S INSTRUCTION REPERTOIRE

OP CODE	OP-CODE BITS 0:3							
BITS 4:7	0	2	4	6	9	C	D	E
0		BTBS	STH		SRLS	BXH	STM	
1	BALR	BTFS	BAL	AHM	SLIS	BXLE	LM	SVC
2	BTCR	BFBS	BTC		STBR	LPSW	STB	SINT
3	BFCR	BFFS	BFC		LBR	THI	LB	
4	NHR	LIS	NH		EXBR	NHI	CLB	
5	CLHR	LCS	CLH		EPSR	CLHI	AL	
6	OHR	AIS	OH		WBR	OHI	WB	
7	XHR	SIS	XH		RBR	XHI	RB	
8	LHR		LH		WHR	LHI	WH	
9	CHR		CH		RHR	CHI	RH	
A	AHR		AH		WDR	AHI	WD	RRL
B	SHR		SH		RDR	SHI	RD	RLL
C	MHR*		MH*		MHUR*	SRHL	MHU*	SRL
D	DHR*		DH*		SSR	SLHL	SS	SLL
E	ACHR		ACH		OCR	SRHA	OC	SRA
F	SCHR		SCH		AIR	SLHA	AI	SLA

*Available only with Multiply/Divide option.

Machine Malfunction Interrupt

The Machine Malfunction Interrupt occurs on a memory parity error or early power fail if PSW Bit-2 is set. The emulator also performs a Machine Malfunction PSW swap on Power-Up if PSW Bit-2 is set, Auto-Restart is present, and the Run mode is specified.

If the Memory Parity option is present, the parity bit of each halfword in main memory is set or reset to maintain odd parity. The parity bit is generated on every Memory Write and checked on every Memory Read or Instruction Read. If a Memory Parity Error (MPE) occurs, and PSW Bit-2 is set, the testable signal MALF goes active. During the user instruction fetch part of the micro-program, MALF, along with other interrupts, is tested. If any interrupt is pending, the micro-program branches to a routine to sort interrupts by priority.

The Early Power Fail condition (EPF) exists if the optional power fail detector determines that the line voltage is low. The condition also occurs when the Initialize key is depressed or when the Power switch is turned OFF. One millisecond after Early Power Fail, the testable Primary Power Fail signal (PPF) goes active. The testable signal MALF is active if EPF is active and PSW Bit-2 is set or if PPF is active. When the micro-program loads Zero into PSW, the MPE and EPF Flags are reset.

External Interrupts

If individually enabled by the user's program, a peripheral device controller is allowed to request Processor service when the device itself is ready to transfer data. If PSW Bit-1 is reset, I/O device interrupt signals are ignored but queued, the signal (ATN) remains pending. However, when PSW Bit-1 is set the interrupt is acknowledged.

The processor may service an I/O interrupt in one of two ways, depending on the state of PSW Bit-4. Refer to Figure 9.

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FUNCTIONAL DIAGRAM ANALYSIS

Introduction

This section relates to Functional Schematic 01-094D08, Sheets 1 through 19. The last character of the mnemonic symbol on INTERDATA Functional Schematics designates the logic level at the time the signal is active. For example; D050 is data line number 5 (D05). The last character (0) indicates that when D05 is active, the line is at a logic level of ZERO. Refer to the General Description section of the *Model 6/16 Maintenance Manual,* Publication Number 29-470 for further information concerning the INTERDATA documentation system.

CLOCK CONTROL

The Clock Generator is shown on Sheet 12. The Clock System employs a free running 20MHz oscillator. The oscillator is adjusted by variable resistor R26. (For the semi conductor version of the machine the oscillator is adjusted for 1.66 MHZ to compensate for a memory cycle time which is not divisable by 250ns.)

Signal OSC0 is used as the clock input to three flip-flops arranged as a feedback delay counter. The delay counter generates three overlapping clocks, CLK1, DCLK1, and DDCLK1. All Processor Clocks are derived from CLK1, DCLK1, and DDCLK1. The counter is initialized and held in the initialized state by SCLR0A, on a Power-Down or Power-Up to inhibit clocks. A delayed system clear ACLR0 is generated for the processor to assure that the processor receives clocks in the proper sequence (refer to Figure 10 for clock timing).

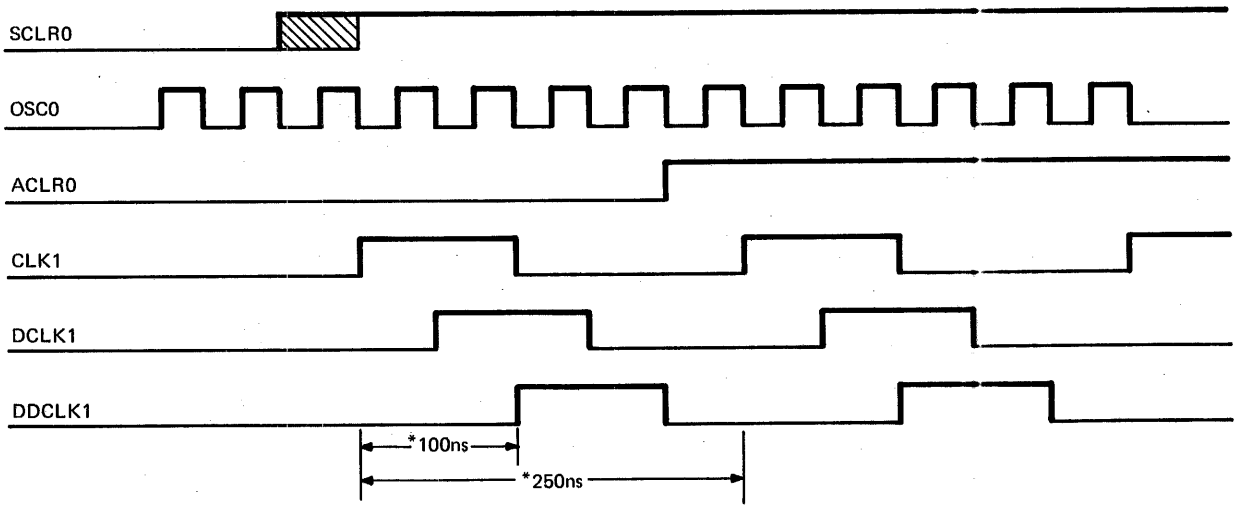

Figure 10. Clock Timing Nominal

The Clock Control Logic is also shown on Sheet 12. Two basic Processor Clocks are derived from CLK1. The first, the CPU clock (CPUCLK0), is the clock for the LSI micro-processor chips. It is disabled for I/O operations, and memory operations whenever MSTP0 is active.

The second Processor Clock generated is the ROM Data Clock (CKRDO, CKRD1). This clock is disabled by I/O operations (IOSTPO), memory operations (MSTPO), and RDSTPO which is a signal from the Repeat Counter which disables the ROM Data Clock for a fixed count n (n< 31), allowing a specific micro-instruction to be repeated n times. Refer to Figure 11 for a description of a clock cycle. The ROM Data Clock also serves as a destination clock. Clocks CLK1, DCLK1, and DDCLK1 are used to synchronize memory and I/O operations.

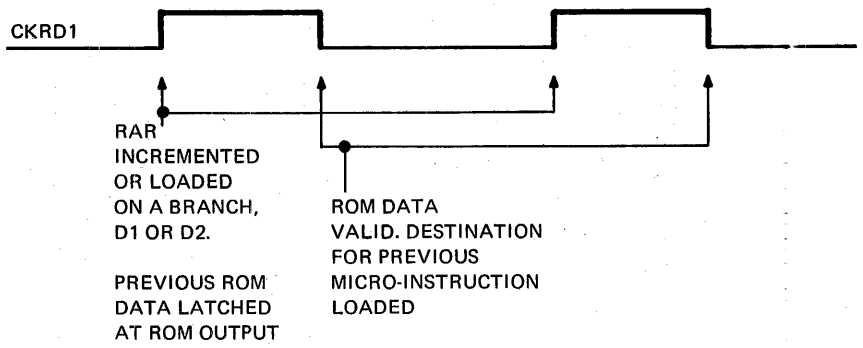

Figure 11. Specific Clock Functions

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INITIALIZE CONTROL

System Initialize is performed by de-energizing the System Clear (SCLR) relay (19G7). This relay is de-energized as a result of the following:

1. Placing the processor in an OFF condition.
2. Operating the processor INIT (Initialize) switch.
3. Activating PFDTO by an external source.
4. Activating PFDTO from the optional Primary Power Fail detector if the input falls below the minimum operating level.
5. Loss of either +5VDC or (+12 0R 15VDC) from the processor power supply.

The SCLR function provides an orderly shut down of the processor as well as a reset signal to both the memory and the Multiplexor Bus. On a power up, the SCLR relay remains de-activated until all DC Voltages are within regulation. This assures predictable initial states of latched functions.

An early Power Fail indication is provided to the user program if Bit-2 of the Program Status Word (PSW) is set. This indication is provided by the micro-program by means of a machine malfunction interrupt swap.

Upon receipt of a Power-Down indication by the hardware, PFDTO (19F1) active, the one millisecond timer (19J4) is triggered. The leading edge of this pulse sets the Early Power Fail flip-flop (19L5) which in turn enables, if PSW Bit-2 is set, a branch on Machine Malfunction to be taken by the micro-program. The micro-program tests to determine which condition caused the Machine Malfunction (MMALF) interrupt. If the Early Power Fail flip-flop (FEPF) is set, the micro-program signals the user program by means of a Machine Malfunction PSW swap. On the trailing edge of the pulse from the one millisecond timer, the Primary Power Fail flip-flop (19J6) is set, initiating a Power-Down sequence.

The optional Primary Power Fail detector monitors the AC input by sampling the secondaries of a 12 VAC transformer, C1 and C3 from the processor power supply. If the AC is lost or if the AC falls below a predetermined level PFDTO (19F1) and POWDNO (19D1) become active. Signal PFDTO initiates the Power-Down sequence and POWDN0 provides a fast discharge path for capacitors C-46 and C-47 which de-energizes the SCLR relay and holds the relay OFF in the event that the AC voltage is fluctuating about its preset Power-Down level.

NOTE

With a semi-conductor memory system the Primary Power Fail detector is built into the Power Supply.

READ ONLY MEMORY (ROM)

The Read Only Memory (ROM) is a high speed, solid state, non-destructive memory which holds the micro-program. The ROM is organized into a single page of 512 words and each word is 24 bits in length. An additional page of ROM can be added to support optional features. Each page of ROM contains 3 Integrated Circuit (IC) packages arranged such that each IC holds 8 bits of each word on the associated page. An additional ROM chip (512 x 8) comprises the Decoder ROM (DROM).

Each ROM IC contains two enable leads (CE1 and CE2), and a strobe lead (see Sheet 6). To enable the ROM chip CE1 must be Low and CE2 must be High. The strobe (CKRD0) is used to latch the data at the output of the ROM. The ROM contains internal latches which are used to hold the ROM Data (RD), refer to Figure 12 for ROM timing. The RD register is internal to the ROM ICs.

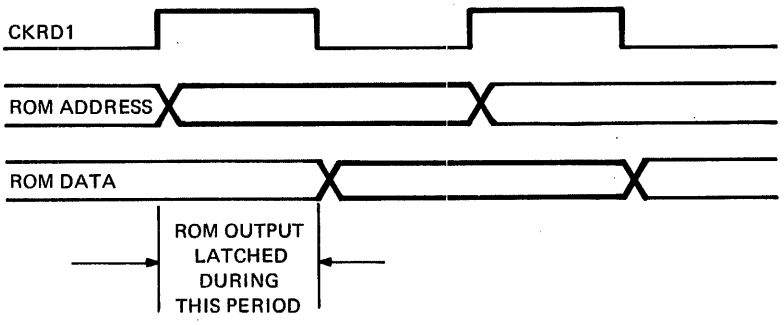

Figure 12. ROM Timing

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Decoder ROM (DROM)

The Decoder ROM (DROM) is a single ROM Integrated circuit, refer to Sheet 5. It contains 512 eight bit words. The DROM is addressed by the most significant eight bits of the Instruction Register (OP Code Field). Each of the 256 possible combinations of this decoded function may address two locations in the DROM, depending on the state of D10 (5D1), a decoded function of RD0, RD1, and RD2. When D10 is low, one of the first 256 words of the DROM is selected, corresponding to a micro-code D1. Illegal instructions are decoded in the DROM.

ROM Address Register (RAR)

The ROM Address Register (RAR), sheets 5 and 6, is a 10 bit register which is loaded on the positive edge of CKRD1 from the DROM during a decode micro-operation or the ROM Data bits during a branch micro-operation. The eight least significant bits of this register are arranged as a counter to allow sequential ROM addresses in a given half page to be selected. The RAR is initialized on Power Up to address X'100' and the micro-program begins execution at this location. Address Clear (ACLR0) is used to hold the ROM Address at X'100' allowing the ROM to latch the RD information accessed from ROM Address X'100', refer to Figure 10 for ACLR0 timing.

PROCESSOR REGISTERS

The majority of the instructions contained in the micro-program are concerned with relocating data from one processor register to another. Most of the processor registers are general purpose registers, however, some do perform special functions. Each register is described in the following sections.

Location Counter, Memory Address Register, and Memory Address Buffer (Refer to Sheet 17).

The Location Counter is an up-counter which automatically increments by 2 on each Instruction Read or D1 (non-RR or SF referenced) micro-instruction. The Location Counter can also be loaded directly from the S Bus. Anytime the Location Counter is loaded from the S Bus, the Memory Address Register (MAR) is also loaded with the same data.

The Memory Address Register (MAR) is a two to one (2:1) multiplexer, with storage latches. The clock following an increment of the Location Counter causes the contents of the Location Counter to be copied into the Memory Address Register.

The Memory Address Buffer (MAB) is a two-to-one (2:1) multiplexer, the inputs of which are the Location Counter and the Memory Address Register. During an Instruction Read, the contents of the Location Counter is gated onto the Memory Address Bus. During all other memory operations the contents of the Memory Address Register are present on the Memory Address Bus. The Memory Address Buffer outputs are disabled (high impedance state) whenever the processor is not selected such as during DMA operations. The Memory Address Buffer is also disabled by EXMBSY0 (19) if a memory adapter card (35-608) is used.

The Location Counter is a 15-Bit register and the Memory Address Register is a 16-Bit register.

Memory Data Register (MDR)

The Memory Data Register (MDR) is shown on Sheet 16. The MDR is a two-to-one (2:1) multiplexer with storage latches and is 16 bits wide. The inputs to the multiplexer originate from the S Bus and the Memory Data Receive Bus. The storage latches are edge triggered which are loaded by signals LDMDRH and LDMDRL. When the MDR is to be loaded from the S Bus the LDMDRH and LDMDRL signals are a combination of the MDR being selected and CKRD. When a Memory Read Operation is specified the LDMDRH and LDMDRL signals are generated by a combination of FRD and the removal of the Data Unavailable (DUA) signal by the memory.

The MDR is divided into a High and Low half. The High half is loaded by the LDMDRH signal and the Low half is loaded by the LDMDRL signal. If Cross Shift is specified by the micro-code, only MDR High is loaded when Bit-15 of the MAR is set and only MDR Low is loaded when Bit-15 is reset.

The outputs of the MDR are presented to memory during the Write portion of a memory cycle.

Instruction Register (IR)

The Instruction Register (IR) is a 16-Bit register which stores the user instruction currently being executed. The IR is divided into three parts or fields; OP code field (Bits-0-7), YD field (Bits-8-11), and YS field (Bits-12-15). The IR is loaded directly from the Memory Data Receive Bus (MRR) during an Instruction Read Memory operation.

The OP code field (sheet 5), contains the encoded instruction to be performed. The OP code field outputs are presented as address to the Decoder Read Only Memory. Ninety-Six of the possible 256 combinations are defined as legal instructions (when Multiply, Divide option is included) and have unique entry points in the micro-program. The remaining 160 combinations are directed by Direct the Read-Only-Memory (DROM) to the illegal instruction entry point in the micro-program.

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The YD field is defined as the User Destination field. The YD field selects one of the 16 general registers, located in the LSI micro-controller chips (sheet 4), in which the result of the user instruction is to be stored. This portion of the IR (sheet 11) is arranged as an up/down-counter. If YDP1 is specified in a micro-instruction the YD field of the IR is incremented by one at the end of the instruction. In the same manner, if YDM1 is specified, the YD field of the IR is decremented by one at the end of the instruction. The YD field is also set to ZERO when Clear YD is specified by the micro-program.

The YS field is the User Source field of the instruction being emulated. The second operand of the instruction is contained in the general register specified by YS for RR format instruction. This field also contains the number of the general register being used as the index register on an RX or RS instruction or data in SR instruction.

Flag Register (FLR) and Condition Code (CC)

The Flag Register (FLR) (sheet 13), is a four bit register which contains the Carry Flag (C), the Overflow Flag (V), the Greater Than Flag (G), and the Less Than Flag (L). The Flag Register outputs are copied into another four bit register, the Condition Code (Sheet 10), at the end of each user instruction being emulated. These flags represent results of instructions which are not otherwise indicated.

The FLR is loaded from the S Bus whenever either the FLR or Program Status Word (PSW) register is specified as a destination. The contents are copied into the Condition Code (CC) on an Instruction Read or after a Load PSW micro-instruction. The outputs from the FLR are also used by the Branch Circuit (sheet 14) for conditional branches. The contents of the CC are copied onto the B Bus (Bits-12-15) when the PSW is specified as the source register.

The FLR (the Carry Flag, Overflow Flag, and Greater/Less Than Flags) are also modifier as follows:

The Carry Flag (C) is affected by any Arithmetic, Boolean, Shift, or Load micro-instruction if Carry Out (CO) is specified. The Carry Flag sets on a Shift if the bit shifted from the appropriate port on the LSI micro-controller (sheet 4) is set, if Carry (Carry 1) from the LSI micro-controller (sheet 4) is set on an Add, or if Carry 1 is inactive on a Subtract. In all other cases the Carry Flag is reset.

The Overflow Flag (V) is directly set if false SYNC is detected on an I/O operation and is changed on any Add or Subtract micro-instruction if Flag (F1) is specified. Overflow (OVL1) is a direct output of the most significant slice of the Central Processing Unit (CPU) (sheet 4) and is valid only on an Add or Subtract micro-instruction.

The Greater Than (G) and Less Than (L) Flags change on any Load, Arithmetic, or Boolean micro-instruction providing Flag (F1) is specified. The G Flag is set if the result of the operation is positive or if the result is Zero and either the G or L Flag were set from a previous operation. The L Flag is set if the resulting sign is negative. Either flag is reset if these conditions are not met.

Shift Control

The LSI micro-controller components making up the processor (Sheet 4) have the capability of shifting 16 or 32-Bits of data right or left under micro-program control. The ports on these chips associated with this capability are SLOSRI (Shift Left Out, Shift Right In), and SROSLI (Shift Right Out, Shift Left In) for shifting the general purpose register left or right. Signals QLOQRI (Q Register Left Out, Q Register Right In) and QROQLI (Q Register Right Out, Q Register Left In) are associated with a 16-Bit internal extension register for double precision shifting capability. The controls for this are shown on sheet 13. For single and double precision shifts, Carry Out (CO) is specified to load the C flag. Carry In (CI) is used as a control to determine whether data is rotated or shifted by the control logic.

Table 6 shows the states of the shift ports of the processor.

TABLE 6. PROCESSOR SHIFT PORT STATUS.

FUNCTION	SLISRO1	QLOQRI1	SLOSRI1	QLIQRO1
Shift Left	0	Z	Z	0
Shift Right	Z	0	0	Z
Double Precision Shift Left	Z	Z	Z	0 or Z*
Double Precision Shift Right	Z	Z	0 or Z*	Z

Z = Open collector output state, equal to bits being shifted out of these ports.

* 0 or Z depends on the state of Carry In (CI).
CI = 1 for a rotate, and the port state is Z.
CI = 0 for a shift, and the port state is 0.

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CPU, Data Multiplexer, and Cross Shift

The CPU (sheet 4) is comprised of four Large Scale Integration (LSI) chips forming a 16-Bit wide data path. Internal to these chips are an ALU (Arithmetic Logic Unit), a 16 x 16 general purpose register stack with dual port accessibility to the ALU, a 16-Bit extension register, and circuits to control shifts, both single and double precision.

Data is presented to the CPU through a Data Multiplexer (sheets 8 and 9). The Data Multiplexer, under ROM Control, selects one of 8 inputs (16-Bits wide), unless it is an Immediate function. An Immediate function disables the outputs of the Data Multiplexer (sheet 8), and passes the data from the Data Multiplexer through a second multiplexer network. The second multiplexer network either cross shifts the data or passes it through depending on the state of MAR 15 and whether or not Cross Shift is specified by the microcode.

On Immediate micro-instructions, the output of the Cross Shift Multiplexer is disabled (High Z state) and the output of the Immediate Multiplexer is enabled. The outputs of these Multiplexers are OR-tied and present data to the Data Inputs of the CPU chips.

The Data Outputs of the CPU chips form the S Bus.

I/O CONTROL

An I/O operation is initiated if I/O is the Source or Destination of a micro-instruction. The I/O control logic is shown on Sheet 15. If I/O is a source, then an Input operation is initiated or if I/O is a destination, an output operation is indicated. I/O Timing is discussed separately for input and output.

Input

Refer to Figure 13 for Timing information. When I/O is specified as a source, unload I/O (UIO0) (15G6) and IOSTOP0 goes active. On the trailing edge of the next clock (CLK1) The Control In flip-flop (15G8) sets. On receipt of SYN0 from the selected I/O device or the detection of False SYNC, the 14 millisecond Timer (15N7) times out, the SYNC flip-flop (15L8) sets which deactivates IOSTOP0. On The Trailing edge of the next CLK1 the destination register is loaded and both the Control In flip-flop and the SYNC Flip-Flop resets completing the operation.

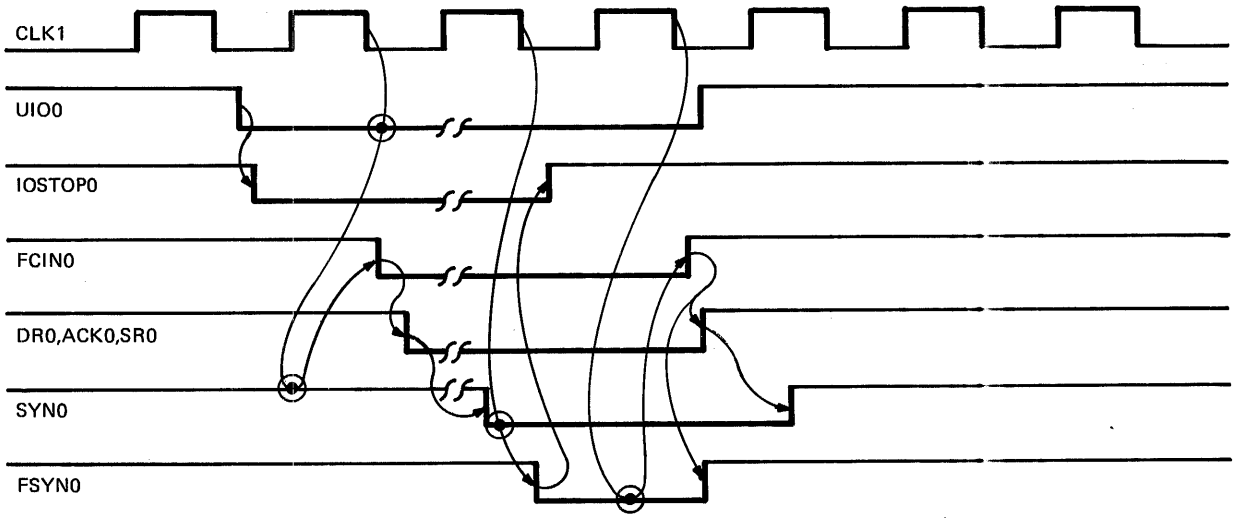

Figure 13. I/O Input

Output

Refer to Figure 14 for Output Timing information. An I/O out operation is very similar to the input operation. When Load I/O LDI00 (15J6) is detected, IOSTOPO goes active and on the leading edge of the next CLK1 the Data flip-flop (15K8) sets. The output of the Data flip-flop is used to gate data To The Data Bus, D000:160. On the trailing edge of the next DDCLK1 the Control Out flip-flop (15H8) is set which activates the specified output control line. The output operation now progresses in the same manner as the I/O Input operation discussed previously.

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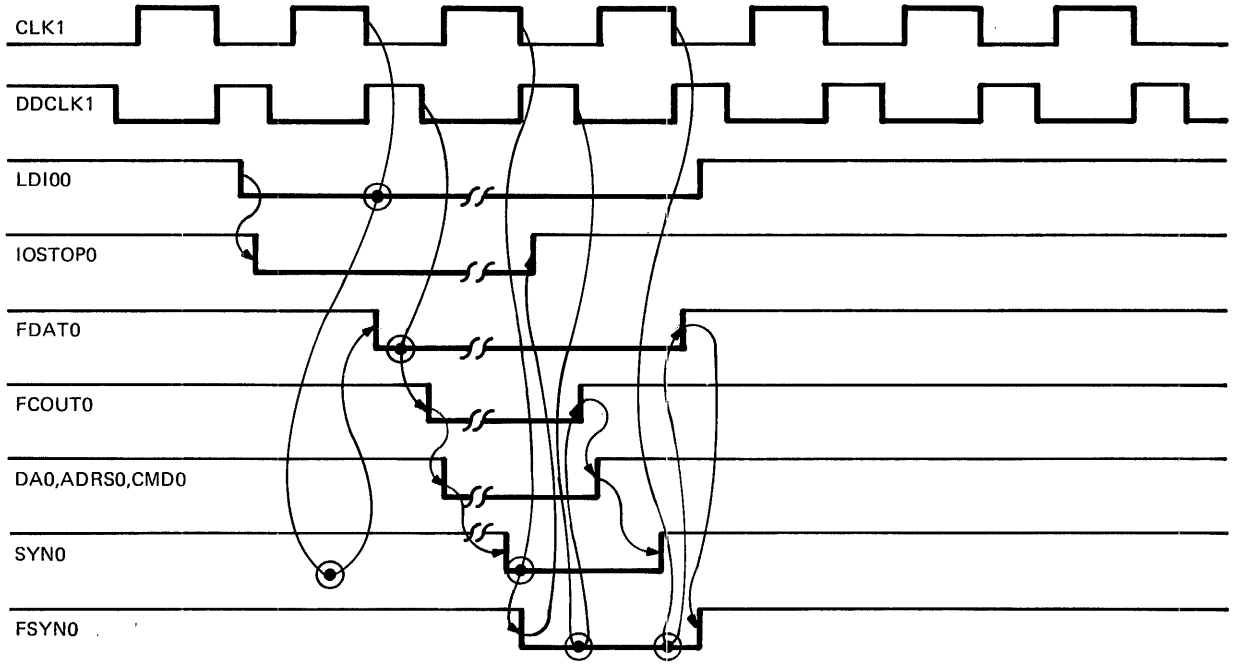
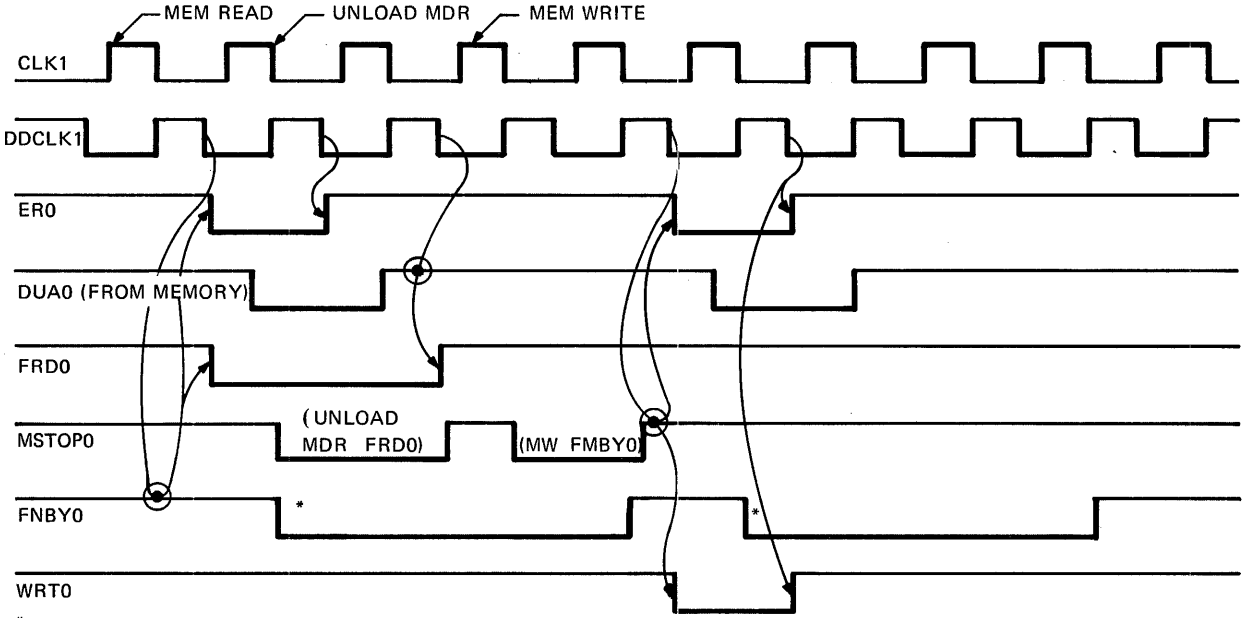


Figure 14. I/O Output

Memory Timing and Control

A memory operation can be initiated by the micro-program by specifying a Memory Read, Memory Write or an Instruction Read. An Instruction Read and a Memory Read Operation is identical except that an Instruction Read causes both the MDR and the Instruction Register to be loaded from the Memory Bus. In addition, a memory cycle can be commenced by a DMA Request, REQO (18F1) active. (The semi-conductor memory uses a DMA request in order to insure that the Processor does not attempt a memory operation during the time that an internal memory refresh operation is taking place.)

Figure 15 depicts the memory timing and control functions for Processor initiated cycles. MEMI (18F1) indicates a memory operation is requested by the Processor. If the memory is not busy, FMBY0 (18G1) inactive and a DMA request is not latched, FREQO (28F8) inactive, a processor memory operation is initiated, the Early Read flip-flop (18C5) is set on the trailing edge of Double Delayed Clock (DDCLKO). On this same edge, either the Write flip-flop (18D6) or the Read flip-flop (18J6) is set to differentiate between a memory read or a memory write operation. On the trailing edge of the next CLK1 the four bit counter (18M6) is loaded with a value, which is dependent on the memory cycle time of the memory being used. (Refer to the strap option Table on Sheet 18 of the Function Schematics for strapping information for specific memory cycle times.) The output of the FMBY1 counter is used for clock stops and memory timing control. The counter is incremented by one on each CLK1 until the count goes from X'F' to X'0'. This deactivates FMBY1.



* FMBY0 = 3 CLOCKS (1.0 us CYCLE), 2 CLOCKS (0.75 us CYCLE), OR 1 CLOCK (SEMI MEMORY)

Figure 15. Processor Memory Timing (1.0 usec)

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DMA memory timing, Figure 16, is similar to Processor Timing except that the sequence is started by a DMA request, REQO active. This signal is synchronized to the Processor clocks by the request flip-flop (18F6). Once this request is latched the DMA device requesting memory gets the next avilable memory cycle. Prior to generating ERO to the memory the Processor generates an Enable command (ENO) (18H8) to the DMA Bus. This signal is used by DMA devices to resolve contention during the active period of this line and on its trailing edge the DMA with the highest priority which is requesting memory becomes selected.

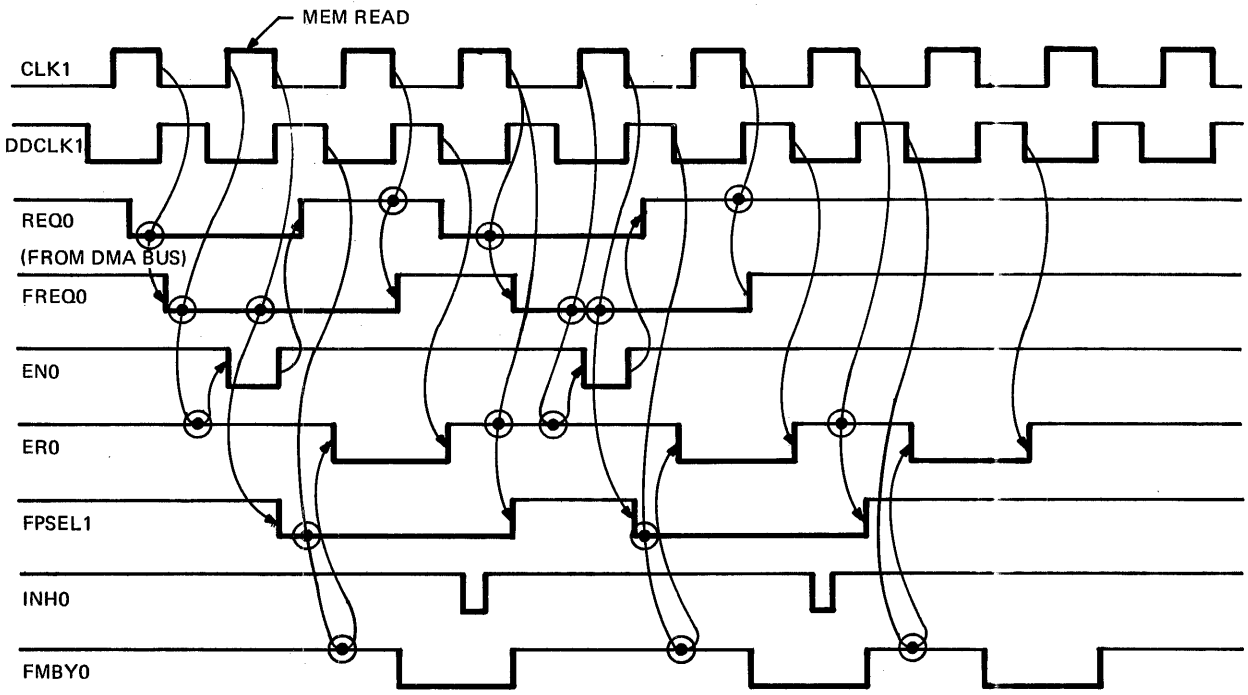

Figure 16. DMA Memory Timing

On the trailing edge of ENO the Processor Select flip-flop (18G6) becomes reset which causes the Memory Address and Memory Data Busses to be forced to a high impedence state by the Processor allowing the selected DMA device to present its address and data to the memory. The first half of the CLK1 following ERO generates INHO (18J6). INHO may be used by the DMA device to indicate that data is available and that the address and data information is latched in the memory. INHO, therefore, should be used to deselect the DMA device.

Figure 16 shows two DMA transfers to a semi-conductor memory at the maximum transfer rate. During the first DMA memory cycle a Processor memory request is queued. Since the Processor has a lower priority than any DMA device, its memory request is not honored until both DMA requests are honored.

Display System

The Display System provides, if the Hexadecimal Display Panel is present, a means for reading the contents of all the system registers and any core memory location, together with the capability of manually entering data and programs. Figure 17 shows the Hexadecimal Display Panel layout. Within the Hexadecimal Display Panel are five eight-bit byte Display Registers, D1 through D5, that hold data output from the Processor, and a 20-bit Switch Register which stores data input from the Hexadecimal Keyboard.

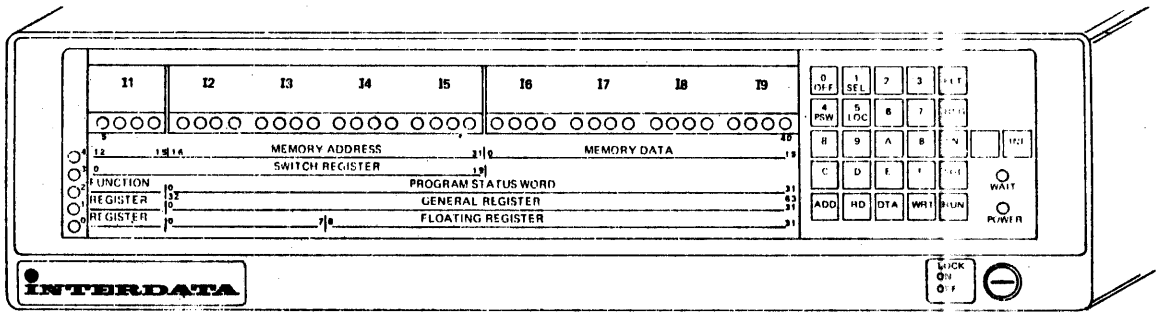

Figure 17. Hexadecimal Display Panel

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Associated with each Display Register D1 through D4 are eight indicator lamps that provide a binary readout and two optional hexadecimal read-out indicators. Associated with Display Register 5 are four indicator lamps for binary display and one optional hexadecimal read-out indicator.

The most significant four bits of Display Register D5 (Bits 0:3) control four of the five indicator lamps along the left edge of the Hexadecimal Display Panel. The fifth indicator lamp is controlled by logic internal to the Hexadecimal Display Panel. To the right of each of these five lamps is a diagram that defines what is being displayed. In general, only one of the diagram lamps is on at a time. If none of the diagram lamps are on, a user program has written data to the display registers.

The most significant 20-bits of the display show the contents of Display Registers D3 and D4 and the least significant four bits of Display Register D5 (Bits 4:7) or the contents of the 20-bit Switch Register. When the Switch Register is being displayed, the lamp next to the Switch Register diagram is turned ON. Any other diagram lamp that may have been ON, remains ON. When the Switch Register is no longer displayed, its diagram lamp goes out and the most significant 20-bits of the display again shows the contents of Display Registers D3 and D4 and the least significant four bits of Display Register D4 (Bits 4:7) (refer to Table 7).

TABLE 7. DISPLAY STATUS AND COMMAND ENCODING

STATUS

	0	1	2	3	4	5	6	7
Run	X	0	0	0	X	X	X	X
Memory Write	X	0	0	1	X	X	X	X
Memory Read	X	0	1	0	X	X	X	X
Address	X	0	1	1	X	X	X	X
Fixed Register	X	1	0	0	X	X	X	X
Floating Register	X	1	0	1	X	X	X	X
Function	X	1	0	0	X	X	X	X

General Register	0	0	1	0	X	1	0	0	0
	1	1	1	0	X	1	0	0	0
	2	0	1	0	X	1	0	0	1
	3	1	1	0	X	1	0	0	1
	4	0	1	0	X	1	0	1	0
	5	1	1	0	X	1	0	1	0
	6	0	1	0	X	1	0	1	1
	7	1	1	0	X	1	0	1	1
	8	0	1	0	X	1	1	0	0
	9	1	1	0	X	1	1	0	0
	A	0	1	0	X	1	1	0	1
	B	1	1	0	X	1	1	0	1
	C	0	1	0	X	1	1	1	0
	D	1	1	0	X	1	1	1	0
	E	0	1	0	X	1	1	1	1
General Register	F	1	1	0	X	1	1	1	1

Floating Register 0, 2, 4, 6, 8, A, C, E

Function	0	0	1	0	0	0	0	0	0
	1	1	1	0	0	0	0	0	0
	2	0	1	0	0	0	0	0	1
	3	1	1	0	0	0	0	0	1
	4	0	1	0	0	0	0	1	0
	5	1	1	0	0	0	0	1	0
	6	0	1	0	0	0	0	1	1
	7	1	1	0	0	0	0	1	1
	8	0	1	0	0	0	1	0	0
	9	1	1	0	0	0	1	0	0
	A	0	1	0	0	0	1	0	1
	B	1	1	0	0	0	1	0	1
	C	0	1	0	0	0	1	1	0
	D	1	1	0	0	0	1	1	0
	E	0	1	0	0	0	1	1	1
Function	F	1	1	0	0	0	1	1	1

Console Interrupt
PSW Select
PSW
LOC

COMMAND

Normal	1	0	0	0	0	0	0	0
Incremental	0	1	0	0	0	0	0	0

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The Key Operated Security Lock is a three-position, OFF-ON-LOCK, key operated locking switch, which controls the primary power to the system. This switch can also disable the Hexadecimal Display Panel, thereby preventing any accidental manual input to the system. The power indicator lamp (PWR) associated with the key lock is located in the lower right corner of the Hexadecimal Display Panel. The PWR positions, primary power, the Control keys, and the Hexadecimal keys are (see Figure 18):

OFF	The primary power is OFF.
ON	The primary power is ON and the Control keys and Hexadecimal keys are enabled.
LOCK	The primary power is ON and the Control keys and Hexadecimal keys are disabled.

The Hexadecimal Display Panel operating procedures may be found in the appropriate User's Manual.

The Display Controller, 35-601, or the Display Controller with ALO, 35-602, must be used to support the Binary or Hexadecimal Display Console or the Turnkey Console. Refer to Display Contoller Functional Schematic 02-405D08 during the following desciption.

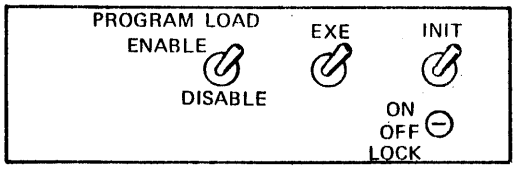

Figure 18. Turnkey Console

Data Transfer

When the display is in the Normal mode, all data outputs are directed into Display Register D1. Conditioning the controller to the incremental mode, via an Output command, causes the two bit counter (2M9) to be incremented at the trailing edge of DAG1. The output of this counter is decoded to activate LA0, in response to the first DAG1 and then LB0 for all subsequent DAG1's until the counter is initialized. In this mode, the first DA loads Display Register D1, the next DA loads Display Register D2. The next two DAs load Display Registers D3 and D4. This counter is initialized by SCLRO, by an Output command placing the controller in the incremental mode, or whenever the display is addressed and the Normal mode is selected.

Input data from the Switch Register to the Hexadecimal Display Panel is handled in a similar manner as output data. In the Normal mode or on the first Data Request (DR), if in the Incremental mode, Switch Register Bits 12:19 are read. The second DR, in the incremental mode, reads Switch Register Bits 4:11. The two bit counter (2M7) directs the DR to the appropriate group of Switch Registers. This counter is initialized by the same function as the four bit counter discussed previously and is incremented at the trailing edge of DRG1.

NOTE

Bits 0:3 of the Switch Register are gated out as part of the status byte when address is read.

Control Logic

When the display requires micro-program support, it generates two outputs, ESNO0 and ESNC0, which are latched in the RS flip-flop at 2K2. The output of this flip-flop sets the Console Attention flip-flop (CATN) at 2L2. This flip-flop is reset by GADR0 when the Processor addresses the display or by SCLRO.

When the SGL function switch is depressed, SSGL1 becomes active (2G4) and ESNCO AND ESNO0 are generated which cause the Single flip-flop (2L3) to become set. This flip-flop remains set until another execute is generated and the SGL function is not selected.

Status Input

The status byte encoding is shown in Table 8. The status byte is gated onto the SD00:07 lines by the SRG0 lead. SRG0 gates the SD00:07 lines onto Bits 08:15 of the D Bus.

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TURNKEY CONSOLE

This panel provides a means of controlling the system power, initializing the system, and generating a Console Attention (FCATN) to start program execution, if the Primary Power Fail/Auto Restart option is not installed.

This option conditions the Processor to the Run mode by grounding SSGL1, SD011, SD021, and SD031 at the Control Console connector. The Display Controller, when addressed by the micro-program in the power up sequence, indicates the Run mode. With the Auto-Restart option present, program execution commences at the address specified in the Location Counter (LOC), when the system is turned on and without the Auto-Restart option the micro-program performs a normal power sequence and then goes to the un-interruptable idle Loop until the Execution (EXE) switch is operated.

BASIC SWITCH PANEL

The Basic Switch Panel provides a means of controlling system power if an optional Display Controller is not equipped. The switch on this option is a single throw double pole switch. One set of contacts is used to jumper C1 and C2, which turns on the power supply or supplies in the system, while the other set of contacts grounds PFDTO (19) going to the Processor to provide an early power fail indication which enables the controlled power down sequence.

Automatic Load Option (ALO)

Refer to Functional Schematics, 02-405 D08, Sheet 3 during this discussion. This option is present on 35-602, Display Controller with ALO, or 35-603, ALO.

The Automatic Load Option is used to store program information in non-destructive Read-Only-Memory (ROM) integrated circuits. A maximum of eight-4K-Bit ROM chips may be installed on a single option board. This provides a storage capability of up to 4K-bytes of information. The ALO is a halfword device which transfers data 16-Bits at a time. Eight-bits of data come from one 512x8-bit ROM while the other 8-bits come from another 512x8-bit ROM. Due to this, ROM chips must be used in pairs (i.e. ROMOA and ROMOB, ROM1A and ROM1B, etc.)

The ALO is enabled, ALEN1 (3F3), by SCLRO. Upon power up the micro-program tests the Halfword Control Line (HWO) (354), if active ALEN1 high and S1 in the Enable position, the micro-program loads the data contained in the ROM devices on the ALO. The data format is shown in Table 8.

TABLE 8. ALO DATA FORMAT

WORD	0	PSW
WORD	1	LOC
WORD	2	START ADDRESS
WORD	3	END ADDRESS
WORD	4	DATA
WORD	.	.
WORD	.	.
WORD	N	DATA

The eleven-bit counter (3D5-3H5) is initialized to X'000' by SCLRO and is incremented following each Data Request on the trailing edge of FDATO (3B5). The micro-program continues to read the ROM data until all data between the start and end addresses is loaded into memory.

The ALO is disabled, ALEN1 inactive, on the leading edge of the first Address Control Line (ADRS0), independently of the device address.

MAINTENANCE

This section describes maintenance procedures which may be used to check and, if necessary, adjust the Processor.

There is only one adjustment associated with the Processor. Check Basic Clock (BCLK0) found on connector 104-3, the Test Aid connector, for a clock period of 250, 300 nanoseconds for the semi-conductor memory version of the Processor. This adjustment is very stable and need only be made if a check indicates that it is out of tolerance. Adjust variable resistor, R26, to bring it into tolerance.

Use the 06-106 Processor Test to perform a comprehensive test of the 6/16 Processor.

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MNEMONICS

The following list provides a brief description of each mnemonic found in the Model 6/16 Processor. The source of each signal on Schematic Drawing 01-094DO8, is also provided.

MNEMONIC	DESCRIPTION	LOCATION
ACK0	Acknowledge Control Line to MPX Bus	15D9
ACLR0	Delayed System Clear	12N3
ADD	Add	7J7
ADRS0	Address Control line to MPX Bus	15F9
AMOD1	YS Equals Zero	11H9
ATN0	Attention Request Line	14L2
B0	YD, YS Address Control	7L7
B000-B150	Data From B Bus	Sheet 8
BCLK0	Buffered Processor Clock	12N4
BRSEL0	Branch Select	14E9
CARRY1	Carry from CPU	4A5
CATN0	Console Attention Request Line	14M2
CBRSEL0	Clocked Branch Select	5K8
CI1	Carry In Enable	1356
CKRD1	ROM Data Clock	12N8
CLK0	Processor Clock	12N5
CLO70	Control Line 7 from MPX Bus	19G5
CLR0	Clear RAR	5N8
CLRFLR0	Clear Flag Register	11D9
CLRYD0	Clear YD Address Register	11C4
CMD0	Command Control Line To MPX Bus	15D9
DA0	Data Available Control Line to MPX Bus	15E9
DB000-DB151	Outputs of Data Buffer	15B1, C1, D1, E1, F1, G1, H1, J1, K1, L1, M1, N1
DBF0	Decoded Branch on False Condition	7D7
DBRCH0	Decoded Branch	7E7
DCLK0	Delayed Processor Clock	12N1
DDCCK0	Clock Delayed from DCLK0	12N1
DI000-DI151	Data in Bus to CPU	4F9, 4G9, 4H9,4J9, 4K9, 4L9
DIR0	Decode Instruction Read	7D7
DMR0	Decoded Memory Read	7D7
DMW0	Decoded Memory Write	7D7
DO001-DO151	Bus Outputs of the CPU Elements	4F3, 4G3, 4J3, 4K3, 4L3
DR0	Data Request Control Line to MPX Bus	15C9

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MNEMONIC	DESCRIPTION	LOCATION
DR081	DROM Output Bit 8	SE9
DR081-DR151	DROM DATA	5E3, SE5, 5E6
D10	DROM Decode 1	7D7
D20	DROM Decode 2	7D7
EN0	Enable From Memory Bus	1848
ER0	Memory Read or Write Enable	18C8
EXBSY0	External Busy to Processor From Memory	18S2
EXDUA0	Data Unavailable From Memory	18H1
EXSTP0	External Clock Stop	12B7
FDAT0	Data Flip-Flop to MPX Bus	15K9
FINR0	Instruction Read Flip-Flop	11E1
FEPF0	Early Power Fail Flip-Flop	19L9
FLDREG0	Load External Register Flip-Flop	19C6
FLPT0	Floating Point Control	11B5
FLR121-FLR151	Flag Register Outputs	13G9, J9, L9, N9
FLRSEL0	Destination Select for Flag Register	7F7
FMBY1	Memory Busy Flip-Flop	18K8
FPAR1	Parity Error Flip-Flop	19M9
FPPF1	Power Fail Flip-Flop	19K9
FPSEL1	Processor Select Flip-Flop	18G8
FRD1	Read Flip-Flop	16A1
FREQ0	Request Flip-Flop	18F8
FTIT0	Clock Stop Test Point	12B7
FWAIT	Wait Flip-Flop	11C9
F1	Set Flags Enable	13Rg
HW0	Halfword Control Line from MPX Bus	14B1
INH0	Inhibit From Memory Bus	18J8
I01	Decoded I/O Operation	15J9
IODMA0	I/O DMA Request Line	14G2
IOSTP0	Clock Stop for I/O	15G9
IO001-IO151	I/O Inputs From MPX Bus	15B1, C1, D1, E1, F1, G1, H1, J1, K1, L1, M1, N1, R1
JAMCC0	Jam Condition Code	7C8
JCICO0	Jam Carry In and Carry Out	11B5

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MNEMONIC	DESCRIPTION	LOCATION
LDCC0	Load Condition Code	11A1
LDCT0	Load Repeat Counter	7G7
LDDEST0	Decoded Load Function (Load Destination)	13C4
LDIO0	Load I/O	7F7
LDREG	Load External Registers	19B9
LMDRH1	Load High Order Byte of MDR	11D9
LMDRL1	Load Low Order Byte of MDR	11D9
LOC001-LOC151	Location Counter Outputs	17B8, E8, H8, L8
LOCSEL0	Destination Selector for LOC	7C7
MA000-MA150	Memory Address Bus	17C9, D9, F9, G9, J9, K9, M9, N9
MAR001-MAR151	MAR Outputs	17D6, 17G6, 17K6, 17N6
MARSEL0	Destination Select for MAR	7F7
MRR001-MRR151	Memory Register Receive Bus	16D1, 16E1, 16G1, 16K1
MSK1	Mask on Condition Code	10N1
MSTP0	Clock Stop For Memory	12J9
OVL0	Overflow	4A5
PERR0	Parity Fail Detected	19M2
PFDT0	Power Fail Detector	19F2
POW0	Power Down Command	11B5
POWDN0	Power Down Signal	19D2
PSW001-PSE151	PSW Outputs	10A6, B6, G6, S5
PSWSEL0	Destination Select for PSW	7C8
QLIQRO1	Shift Q Left In, Shift Q Right Out	4A7
QLOQRI1	Shift Q Left Out, Shift Q Right In	4A7
RAR061-RAR151	ROM ADDRESS Registers	5K1, 5N4, 5N6, 6C6
RD001-RD231	ROM Data Bus	8L3, 8L4, 8L5, 8L6, 8L7, 8L8
RDSP0	ROM Data Clock Stop	11N9
REQ0	DMA Request for Memory Cycle	18F2
SCLR	System Clear	19H9
SINGL0	Single Step Request Line	
SH1	Decoded Shift	13A9
SLISRO1	Shift Left In, Shift Right Out	4A7
SLOSRI1	Shift Left Out, Shift Right In	4A7
SR0	Status Request Control Line to MPX Bus	15B9
SUB0	Subtract	7L7

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MNEMONIC	DESCRIPTION	LOCATION
SUPINC0	Suppress Location Counter Increment	7A7
SV0	Set Overflow on False SYNC	15N9
SYN0	SYNC to MPX Bus	15M9
UIO0	Unload I/O	7N7
UMDR0	Unload MDR	7R7
WT0	Write Signal to Memory	18D8
XIMM1	Immdiate Control Line	9A1
YD01-YD31	Outputs of the User Destination Register	11K9
YDI0	YD Immediate	7R7
YDMI0	Decrement YD	11D4
YDPI0	Increment YD	11D4
YS01-YS31	Outputs of the User Source Register	11F9
ZERO1	Zero Result on S Bus	4A5

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M71-094
MULTIPLY/DIVIDE CARD INFORMATION SPECIFICATION

INTRODUCTION

The Multiply/Divide card is a half-board which resides in the Model 6/16 Processor chassis. The Multiply/Divide card provides the means for executing Multiply or Divide instructions under micro-program control. The processor provides operands to the Multiply/Divide card which in turn processes the operands and returns an answer to the processor.

INSTALLATION

Refer to the appropriate processor installation specification for applicable installation information.

BLOCK DIAGRAM ANALYSIS

Refer to the block diagram of the Multiply/Divide option, Sheet 1 of the Multiply/Divide Functional Schematic 02-403D08.

Inputs to and outputs from the Multiply/Divide card are over the standard I/O Multiplexor Bus and are under micro-program control. Special signals to the card from the processor are: MDO, which selects the card for receiving data over the I/O Bus; LDREG0, which is data from the processor to the option card; EXSTP0, a signal from the card to the Processor to stop the clocks while the card is performing its operations.

CLOCK AND CONTROL

This portion of the card circuit controls the loading of registers from the I/O Bus, the unloading of registers to the I/O Bus, synchronizing the on-board clock stop, and controlling the data paths on the card.

B-REGISTER

The B-Register contains the positive operand for Multiply operations and the two's complement negative operand for Divide operations.

SRH and SRL

SRH and SRL is a 32-Bit register with Shift Left, Shift Right, and Load capability. For Multiply operations SRH is initialized to Zero and SRL contains the Multiplier. SRL is shifted left for Divide operations and shifted right for Multiply operations. SRH is either loaded and shifted left or just shifted left on Divide operations. The Divide Shift Network provides the load and shift function on Divide operations. The decision to just shift or to load and shift is made by the Control Section. SRH is either shifted right by direction of the Control Section on Multiply operations or the output of the adder is loaded. The Multiply Shift Network provides a pre-shift to the partial product contained in SRH so that the Multiply and Divide operations are completed in the same number of clocks (16).

At the completion of an operation, the results are stored in SRH and SRL. The 32-Bit result of a Multiply operation is stored in SRH and SRL or, in the case of a Divide, the quotient is stored in SRL and the remainder is stored in SRH.

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FUNCTIONAL ANALYSIS

When reading this section, refer to Functional Schematic 02-403D08.

Loading SRH,SRL and B Registers

Data is placed on the common BD Bus (BD001-151) from the I/O Bus when the M/D0 signal from the processor is active. When the data to be transferred is valid on the I/O Bus, the LDREG0 control line from the processor is activated for one processor clock. Signals LDREG0 and BCLK0 provide a load clock for the B, SRL, and SRH registers according to a sequence determined by a counter at 4C2, 4D2, 4E2 and 4F2. The LDA0 signal (4H4) loads data from the BD Bus into the B-Register, and also clears SRH. The LDB0 signal load SRL from the DB Bus, and LDC0 loads SRH. If the LDC0 clock is not generated, the operation to be performed is assumed to be a Multiply and the Divide flip-flop (4H5) is not set.

CLOCK CONTROL

The removal of MD0 by the processor causes EXSTP0 to be activated stopping all processor clocks except the Basic Clock (BCLK0). On the BCLK, following the activation of EXSTP0, the local clock is started and 16 clock pulses are generated on the Multiply/Divide Option Board. At the end of the 16 clock period the Multiply or Divide operation is complete and EXSTP0 is deactivated. (This signal is synchronized to the Processor clocks by BCLKO.) For one processor clock period following the removal of EXSTP0, the contents of SRL is gated to the I/O Bus and, during the following processor clock period, the contents of SRH is gated to the I/O Bus.

MULTIPLY

Prior to the commencement of the Multiply operation, the B-Register has been loaded with the multiplicand, SRL has been loaded with the multiplier, and SRH is set to zero. All operands are positive in form. (If negative the micro-program two's complements the numbers prior to loading.) The control lines for SRL (SRLS01 and SRLS11) are set for shift right. The control line for SRH (SRH01 and SRHS11) will either be set for load SRH, if the least significant bit of SRL (SRL151) is a logical One, or will be set for a shift right, if SRL151 is a logical Zero. The Divide Shift Network is disabled and passes the sum of the addition between the content of the B-Register and shifted left partial product contained in the SRH directly to the BD Bus. SRL is shifted right 16 times so that all 16 bits of the multiplier are tested. At the end of this time, SRH contains the most significant 16 bits of the result and SRL contains the least significant 16 bits of the result.

DIVIDE

Prior to the start of the Divide operation SRH and SRL contain the dividend in positive form (if negative the two's complement of the dividend is loaded by the micro-program) and the divisor is loaded into the B-Register in two's complement form. The quotient bit is the carry formed by the addition of SRH and B. Whenever the carry is positive (logical one) the partial remainder at the outputs of the adder is gated into SRH shifted left. Signal SRL is also shifted left and the carry is shifted into the least significant bit of SRL (SRL151). If carry is a logical zero SRH and SRL are shifted left one position and the outputs of the adder are ignored. Carry is again shifted into SRL. SRL is shifted left 16 times at the end of which SRL contains the quotient and SRH contains the remainder of the division.

Figures 1 and 2 are timing diagrams representing the timing of the Multiply/Divide Option Board 35-605.

ADJUSTMENTS

The only adjustment on the M71-094 Multiply/Divide card is that of the on-board oscillator. The oscillator frequency is adjusted by means of potentiometer R2, which is adjusted for an 80 nanosecond period (12.5 megahertz) as measured at the test point on the outer edge of the Multiply/Divide Option card.

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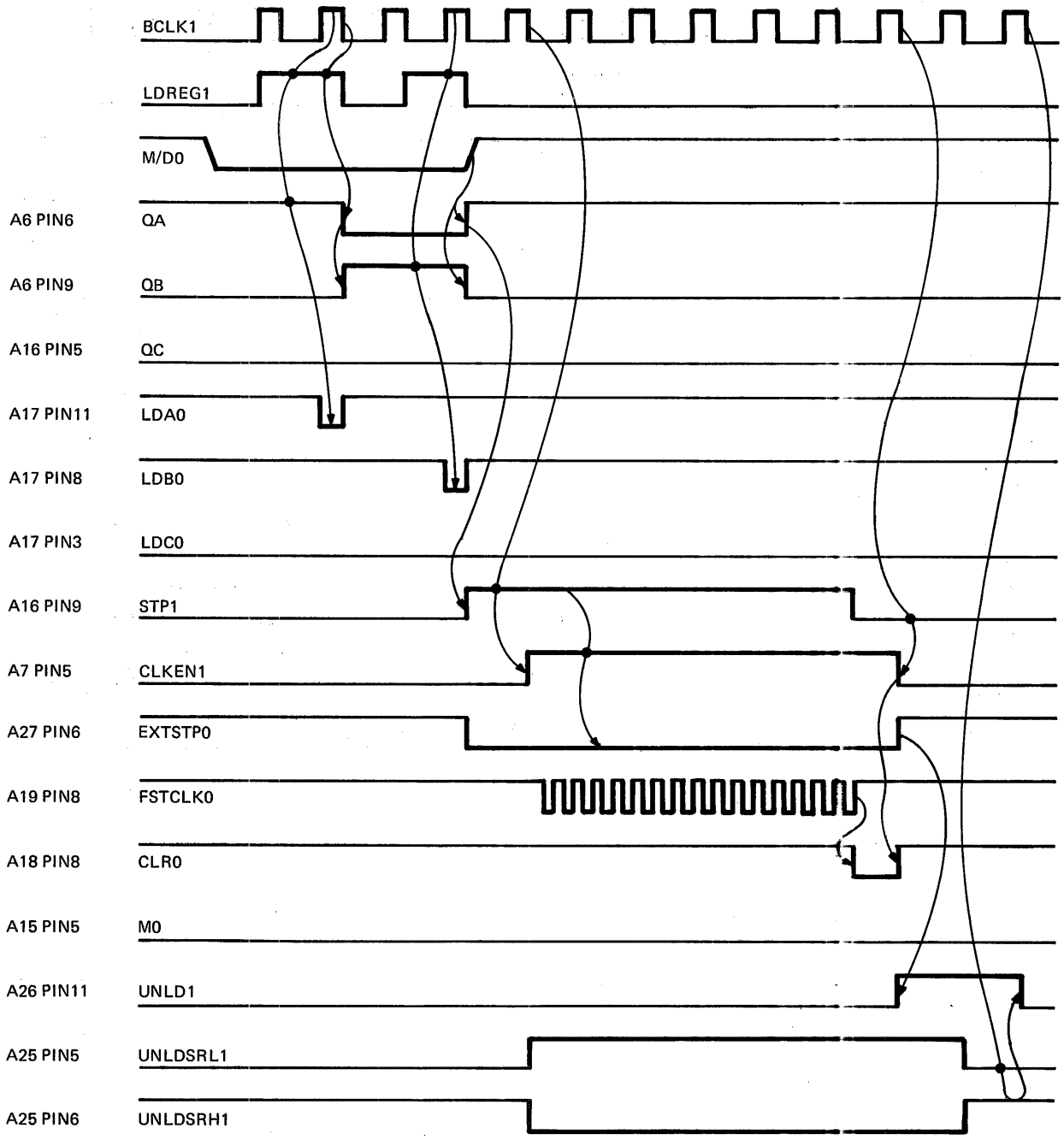

Figure 1. Multiply Timing

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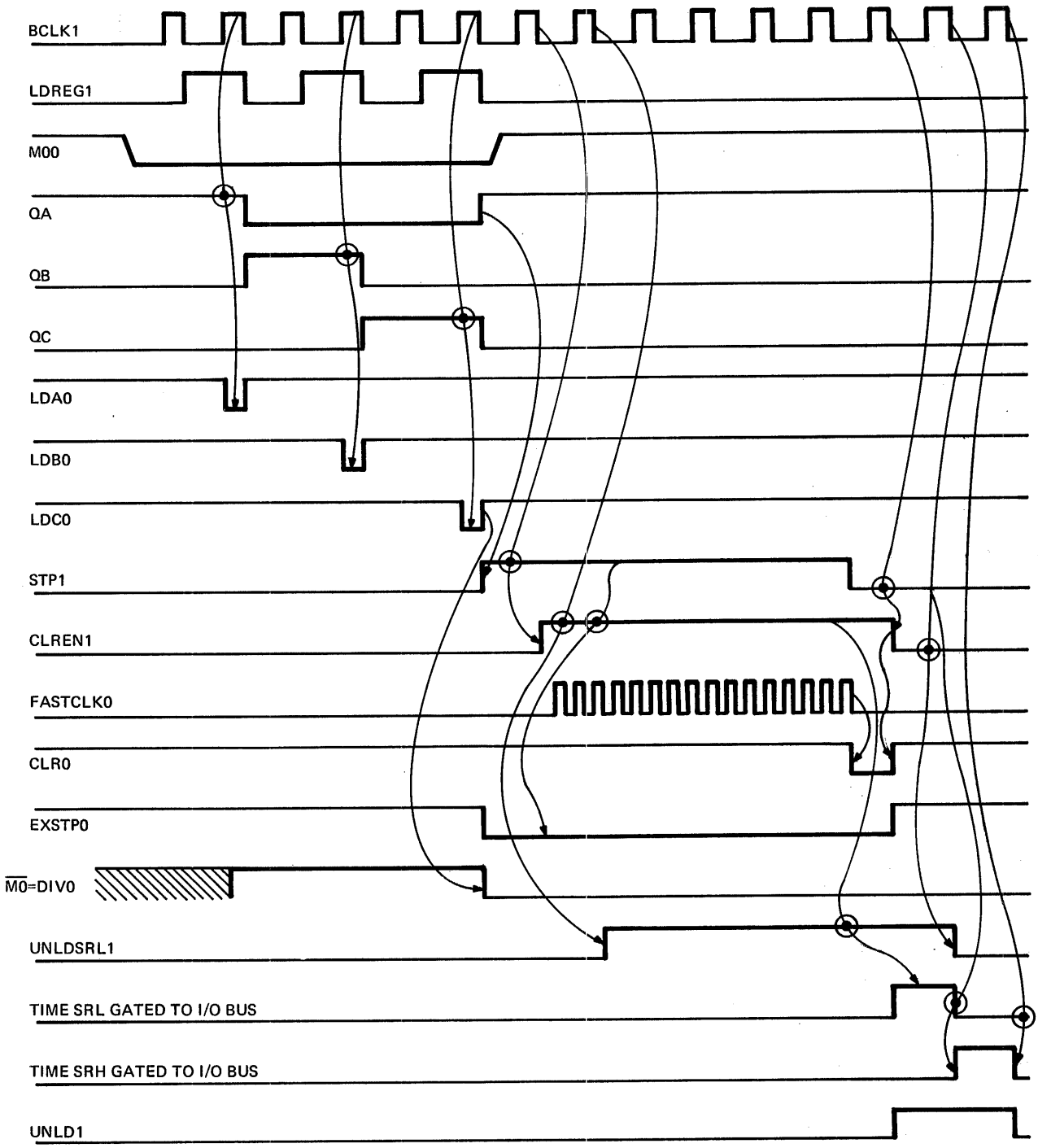

Figure 2. Divide Timing

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MNEMONICS

The following list provides a brief description of each mnemonic found in the Multiply/Divide Option Board. The source of each signal on Functional Schematic 02-403D08, is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
B001:151	Outputs of B-Register	Sheet 3
BCLKO	Basic Clock From CPU	4A2
BD001:151	The Outputs of either the 2:1 MUX following the Adder or the Inverted D-Bus data	Sheets 2, 3
CARRY1	Carry out of the 16-Bit Adder	3B4
CLKEN0	Enables the Clock System of the M/D Board	4A5
CLR0	The OR of SCLR0 and MRESET0	4N8
D000:150	Processor's Bidirectional Data Bus	Sheet 2
DB00:150	Outputs of either SRH,OR SRL to the D-Bus	Sheet 2
DIVO	Divide output of the Multiply/Divide flip-flop	4H5
EXSTP0	External Stop to Processor Clock Stop Logic	4RZ
FSTCLK0	Fast Clock used to perform the Multiply or Divide Functions on the Option Board	4F5
LDA0	A Output of Load Sequencer loads the B-Reg and clears SRH	4H3
LDBO	B Output of Load Sequencer. Loads SRL	4H3
LDCO	C Output of Load Sequencer. Loads SRH	4H3
LDREG0	Load Register Signal from Processor. Indicates Data available.	4A2
MD0	Multiply/Divide select line from Processor	4A2
M0	Multiply output of Multiply/Divide flip-flop	4L4
MRESET0	Master Reset. Initialize function for M/D Option	4K8
SCLR0	System Clear from Processor	4K8
SRH001:151	Outputs of SRH	
SRHCLK0	Clock to SRH	4K3
SRHX1	Conditions SRH to either the Shift Right, Shift Left, or Load Mode.	4N4
SRI01	Shift Right into SRL	3L8
SRL001:151	Outputs of SRL	4K3
SRLX1	Conditions SRL to either the Shift Right, Shift Left or Load Mode.	4K4
STP1	Output of Stop flip-flop	4J2
UNLD1	Enables D-Bus drivers to unload results	4R6
UNLDSRL1	Selects the contents of either SRH or SRL to be gated onto the D-Bus.	4K6
Z001:Z151	Outputs of the 16-Bit Adder	Sheet 3

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APPENDIX 1

EXAMPLE MULTIPLY/DIVIDE OPERATION

Appendix 1 shows an example of a multiply operation, Table A1-1, and a sample of a divide operation, Table A1-2.

TABLE A1-1. Sample Multiplication X'1111'*X'1111'=X'01234321'

B-Reg = 0001 0001 0001 0001

	SRH				SRL			
0	0000	0000	0000	0000	0001	0001	0001	0001
1	0000	1000	1000	1000	1000	1000	1000	1000
2	0000	0100	0100	0100	0100	0100	0100	0100
3	0000	0010	0010	0010	0010	0010	0010	0010
4	0000	0001	0001	0001	0001	0001	0001	0001
5	0000	1001	0001	0001	0000	1000	1000	1000
6	0000	0100	1000	1000	1000	0100	0100	0100
7	0000	0010	0100	0100	0100	0010	0010	0010
8	0000	0010	0010	0010	0010	0001	0001	0001
9	0000	1001	0001	1001	1001	0000	1000	1000
10	0000	0100	1000	1100	1100	1000	0100	0100
11	0000	0010	0100	0110	0110	0100	0010	0010
12	0000	0001	0010	0011	0011	0010	0001	0001
13	0000	1001	0001	1010	0001	1001	0000	1000
14	0000	0100	1000	1101	0000	1100	1000	0100
15	0000	0010	0100	0110	1000	0110	0100	0010
16	0000	0001	0010	0011	0100	0011	0010	0001

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TABLE A1-2. Sample Divide X'3FFF7FFF'/X'7FFF' =X'7FFE'X'7FFF'

B = 1000 0000 0000 0001

	SRH				SRL				CARRY
0	0011	1111	1111	1111	0111	1111	1111	1111	0
1	0111	1111	1111	1110	1111	1111	1111	1110	1
2	0111	1111	1111	1110	1111	1111	1111	1101	1
3	0111	1111	1111	1110	1111	1111	1111	1011	1
4	0111	1111	1111	1110	1111	1111	1111	0111	1
5	0111	1111	1111	1110	1111	1111	1110	1111	1
6	0111	1111	1111	1110	1111	1111	1101	1111	1
7	0111	1111	1111	1110	1111	1111	1011	1111	1
8	0111	1111	1111	1110	1111	1111	0111	1111	1
9	0111	1111	1111	1110	1111	1110	1111	1111	1
10	0111	1111	1111	1110	1111	1101	1111	1111	1
11	0111	1111	1111	1110	1111	1011	1111	1111	1
12	0111	1111	1111	1110	1111	0111	1111	1111	1
13	0111	1111	1111	1110	1110	1111	1111	1111	1
14	0111	1111	1111	1110	1101	1111	1111	1111	1
15	0111	1111	1111	1110	1011	1111	1111	1111	1
16	0111	1111	1111	1110	0111	1111	1111	1111	X

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M70-103
NS SELECTOR CHANNEL
INSTALLATION SPECIFICATION

1. INTRODUCTION

This specification provides the necessary information for the installation of the 02-232 Selector Channel (SELCH) (Product Number M70-103) in a Model 70, 74, 80, 7/16 or 7/16 HSALU Processor System. The NS Selector Channel is complete on one 35-391M02 printed circuit board.

2. PHYSICAL CHARACTERISTICS

2.1 Dimensions 15 3/8 x 14 7/8"

2.2 Weight $2\frac{1}{2}$ pounds maximum

3. INSTALLATION

The NS SELCH may be installed in any even numbered universal expansion slot (i.e., 0, 2, 4, or 6) in the Central Processor Unit (CPU) or in the first memory-I/O expansion chassis. See Figure 1. On 7/16 HSALU the NS SELCH may only be installed in Slot 0 of the CPU back panel.

To install a NS Selector Channel on a Model 74 or a 7/16 BASIC, the Selector Channel must be a 35-391M02. To install a Selector Channel on a 7/16 HSALU the Selector Channel must be a 35-391M02, R02 or higher.

NOTE

A SELCH may be installed in slots 0, 1, or 2 of a Model 80/85 CPU chassis only. In this case cutting of the Multiplexor Bus is not necessary.

3.1 Back Panel Wiring

3.1.1 Multiplexor Channel Bus. **At the time of installation it is necessary to cut the Multiplexor Bus wiring between the even numbered slot accepting the SELCH and the next higher numbered slot on the One (1) connector only. The RACK0/TACK0 daisy chain wiring on the back panel is rerouted according to Figure 1. The lower numbered card slots in the chassis become part of the private SELCH Bus on the One (1) connector only.**

For the convenience of cutting the Multiplexor Bus, the connections between every other slot are made using "top" wire wraps. (This refers to wire wrap back panels only.) This allows the cutting of the bus by simply lifting the top wraps when the SELCH is installed in an even numbered slot. Refer to Figure 1 A during the following example.

To install a SELCH in Slot 4:

1. **Remove all wires on Connector One (1), between Slots 4 and 5, on Pins 11 through 26, Rows 1 and 2. (See backpanel map in 02-232M01D08 Sheet 7.)**
2. **Remove the wire between 222-0001 and 122-0700.**
3. **Remove the RACK0/TACK0 jumper between Pins 122 and 222 on both the Zero (0) and One (1) connectors of Slot 4.**
4. **Connect 122-0700 to 222-0501.**
5. **Install the SELCH into Slot 4 of the chassis. The private SELCH Bus now appears on the Connector One (1) side of Slots 4, 3, 2, 1, and 0. All slots on the Connector Zero (0) side and Slots 7, 6, and 5 on Connector One (1) side remain as standard Multiplexor Bus slots.**

To install a SELCH in any other even numbered slot of a CPU chassis or a Memory-I/O chassis, a similar procedure is followed. Refer to Figure 1 B, C, D, and E.

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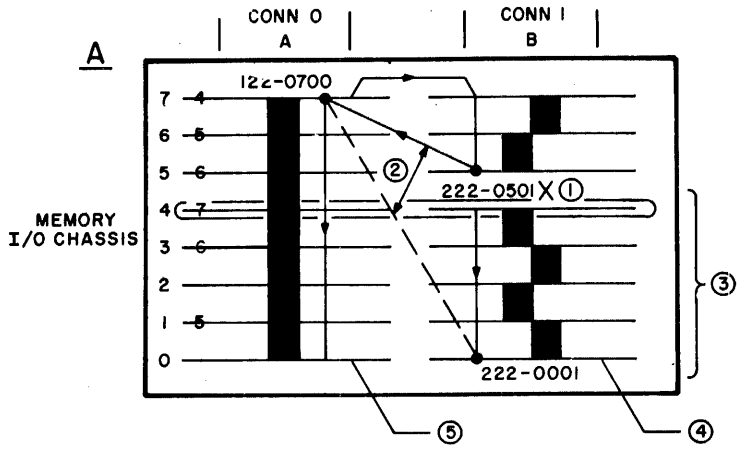
NOTE: THE CIRCLED NUMBERS ON ILLUSTRATIONS A, B, AND C REFER TO THE CORRESPONDING NUMBERS IN THE FOLLOWING INSTALLATION PROCEDURES.



TO INSTALL A SELECTOR CHANNEL IN SLOT 4 OF THE MEMORY I/O CHASSIS ——

① CUT THE MULTIPLEXOR BUS BY REMOVING THE TOP WRAPS.

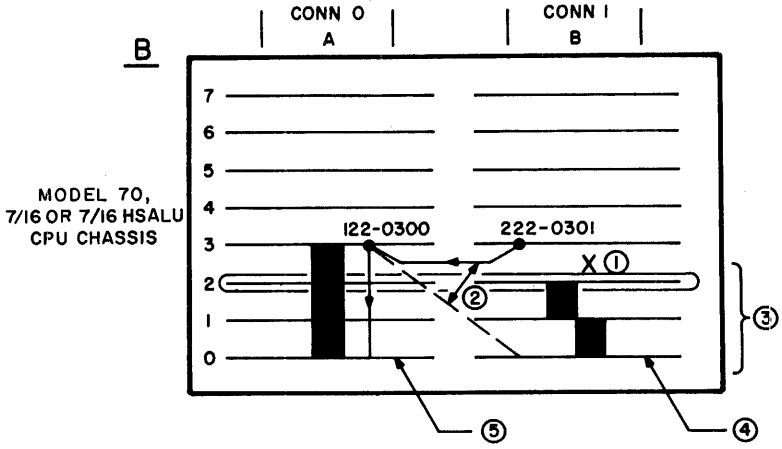
② JUMPER RACKO/TACKO AS SHOWN, REMOVE DASHED JUMPER.

③ THIS SECTION BECOMES THE PRIVATE SELECTOR BUS ON THE CONNECTOR ONE (CONN.1) SIDE ONLY. ALL SLOTS ON THE CONNECTOR ZERO (CONN.0) SIDE, AND SLOTS 7, 6 AND 5 ON CONNECTOR ONE SIDE REMAIN AS STANDARD MULTIPLEXOR BUS SLOTS.

④ IF REQUIRED, EXTEND THE SELECTOR CHANNEL BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑤ EXTEND THE MULTIPLEXOR BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑥ MEMORY MODULE 7, IF IT EXISTS, MUST BE LOCATED IN SLOT 3.



TO INSTALL A SELECTOR CHANNEL IN SLOT 2 OF THE CPU CHASSIS ——

① CUT THE MULTIPLEXOR BUS BY REMOVING THE TOP WRAPS.

② JUMPER RACKO/TACKO AS SHOWN, REMOVE DASHED JUMPER.

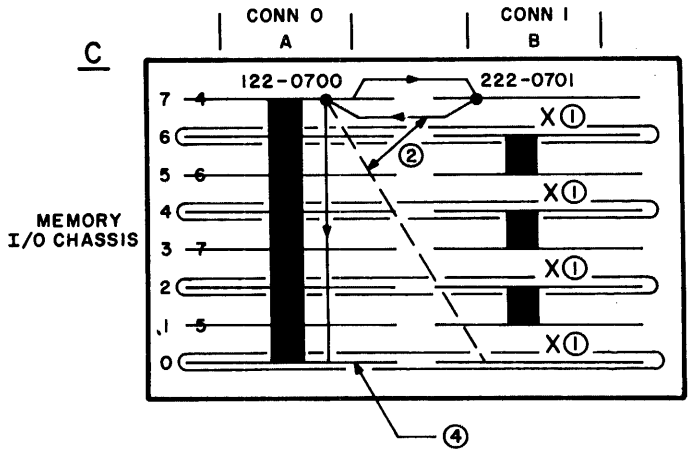
③ THIS SECTION BECOMES THE PRIVATE SELECTOR BU ON THE CONNECTOR ONE (CONN.1) SIDE ONLY. ALL SLOTS ON THE CONNECTOR ZERO (CONN.0) SIDE REMAIN AS STANDARD MULTIPLEXOR BUS SLOTS.

④ IF REQUIRED, EXTEND THE SELECTOR CHANNEL BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑤ EXTEND THE MULTIPLEXOR BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

NOTE: 1
IF A MEMORY I/O CHASSIS IS USED IN THE SYSTEM ANY SELECTOR CHANNELS MUST BE INSTALLED IN THAT CHASSIS.

NOTE: 2
A SELECTOR CHANNEL MAY NOT BE INSTALLED IN SLOT 2 OF THE 7/16 HSALU. SLOT 0 IS THE ONLY SLO IN WHICH A SELCH MAY BE INSTALLED.



TO INSTALL 4 SELECTOR CHANNELS (IN SLOTS 6, 4, 2 AND 0) OF THE MEMORY I/O CHASSIS ——

① CUT THE MULTIPLEXOR BUS IN FOUR PLACES.

② JUMPER RACKO/TACKO AS SHOWN, REMOVE DASHED JUMPER.

③ EACH SELCH, EXCEPT THE ONE IN SLOT 0, HAS ONE SLOT AVAILABLE ON IT'S PRIVATE BUS. THE PRIVATI BUSSES CAN BE EXTENDED TO OTHER CHASSIS BY INSTALLING CABLES IN SLOT POSITIONS 0, 1, 3 AND 5 ON CONNECTOR ONE (CONN.1) SIDE.

④ ALL SLOTS ON THE CONNECTOR ZERO (CONN.0) SIDE REMAIN AS THE STANDARD MULTIPLEXOR BUS. THIS BUS CAN BE EXTENDED BY INSTALLING A CABLE HERE

⑤ MEMORY MODULES 5 AND 7, IF THEY EXIST, MUST BE LOCATED IN SLOTS 1 AND 3.

Figure 1. Backpanel Modifications

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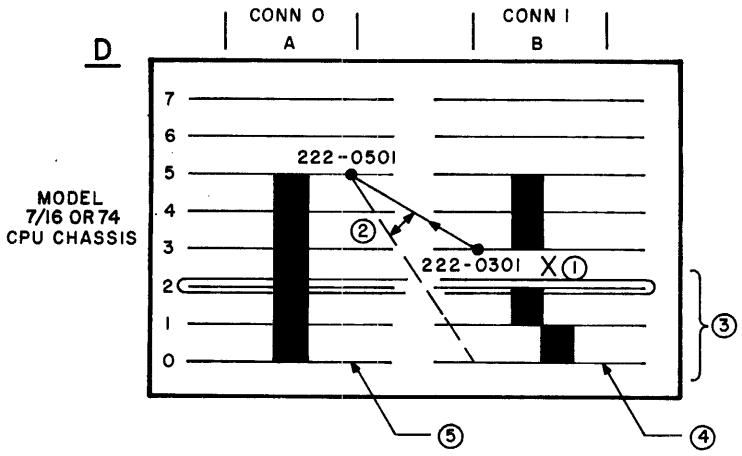


TO INSTALL A SELECTOR CHANNEL IN SLOT 2 OF THE CPU CHASSIS——

① CUT THE MULTIPLEXOR BUS BY REMOVING THE TOP WRAPS.

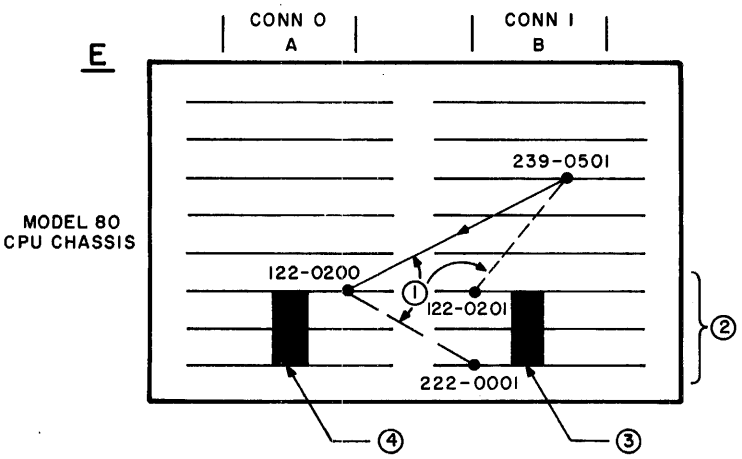
② JUMPER RACKO/TACKO AS SHOWN, REMOVE DASHED JUMPER.

③ THIS SECTION BECOMES THE PRIVATE SELECTOR BUS ON THE CONNECTOR ONE (CONN.1) SIDE ONLY. ALL SLOTS ON THE CONNECTOR ZERO (CONN.O) SIDE REMAIN AS STANDARD MULTIPLEXOR BUS SLOTS.

④ IF REQUIRED, EXTEND THE SELECTOR CHANNEL BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

⑤ EXTEND THE MULTIPLEXOR BUS TO OTHE CHASSIS BY INSTALLING A CABLE HERE.

NOTE:
IF A MEMORY I/O CHASSIS IS USED IN THE SYSTEM, THE SELECTOR CHANNEL MUST BE IN SLOT O OF THE CPU CHASSIS OR IN SOME SLOT OF THE EXPANSION.



TO INSTALL A SELECTOR CHANNEL IN SLOT 0,1 OR 2 CHASSIS——

① JUMPER RACKO/TACKO AS SHOWN, REMOVE DASHED JUMPERS.

② THIS SECTION BECOMES THE PRIVATE SELCH BUS ON THE CONNECTOR ONE (CONN.1) SIDE ONLY. ALL SLOTS ON THE CONNECTOR (CONN.O) SIDE REMAIN AS STANDARD MULTIPLEXOR SLOTS.

③ EXTEND THE SELCH BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

④ EXTEND THE MULTIPLEXOR BUS TO OTHER CHASSIS BY INSTALLING A CABLE HERE.

NOTES:
1. IF A 17-183 CABLE IS INSTALLED BETWEEN CONNECTORS ZERO AND ONE IN THE CPU CHASSIS. THIS CABLE MUST BE REMOVED PRIOR TO INSTALLING SELCH.
2. THE INSTALLATION OF A SELCTOR CHANNEL OR OTHER I/O DEVICE CONTROLLER IN THE M80 CPU CHASSIS REDUCES THE MAXIMUM MEMORY SIZE BY 16K BYTES (ONE MSU) FOR EACH SLOT USED!
3. ONLY ONE SELECTOR CHANNEL MAY BE CONFIGURED IN THE MODEL 80 PROCESSOR CHASSIS.

Figure 1. Backpanel Modifications
(Continued)

3.1.2 ACT0/TAC0. **The ACT0/TAC0 jumper between Pins 137-0 and 237-0 must be removed from the slot used by the SELCH controller. If the Selector Channel is not the first Direct Memory Access (DMA) channel on the Memory Bus, jumper "K" on the SELCH controller must be removed.** Note that on a Model 74 only one DMA device is permitted.

NOTE (Not Applicable on Model 74)

On installations with Multiple SELCH's, remove the "EN0" and the "INH0" filters on all but the last SELCH (Remove the following: R70, R72, C59 and C61).

3.2 Cabling

The cabling necessary for the SELCH depends on the system's physical configuration. When the SELCH Bus does not extend outside the chassis, no cabling is required. When the SELCH Bus must be extended to another chassis, a number of cable configurations can be used. See Figure 2. Care should be taken to minimize bus lengths.

See Figure 2 for a summary of cables.

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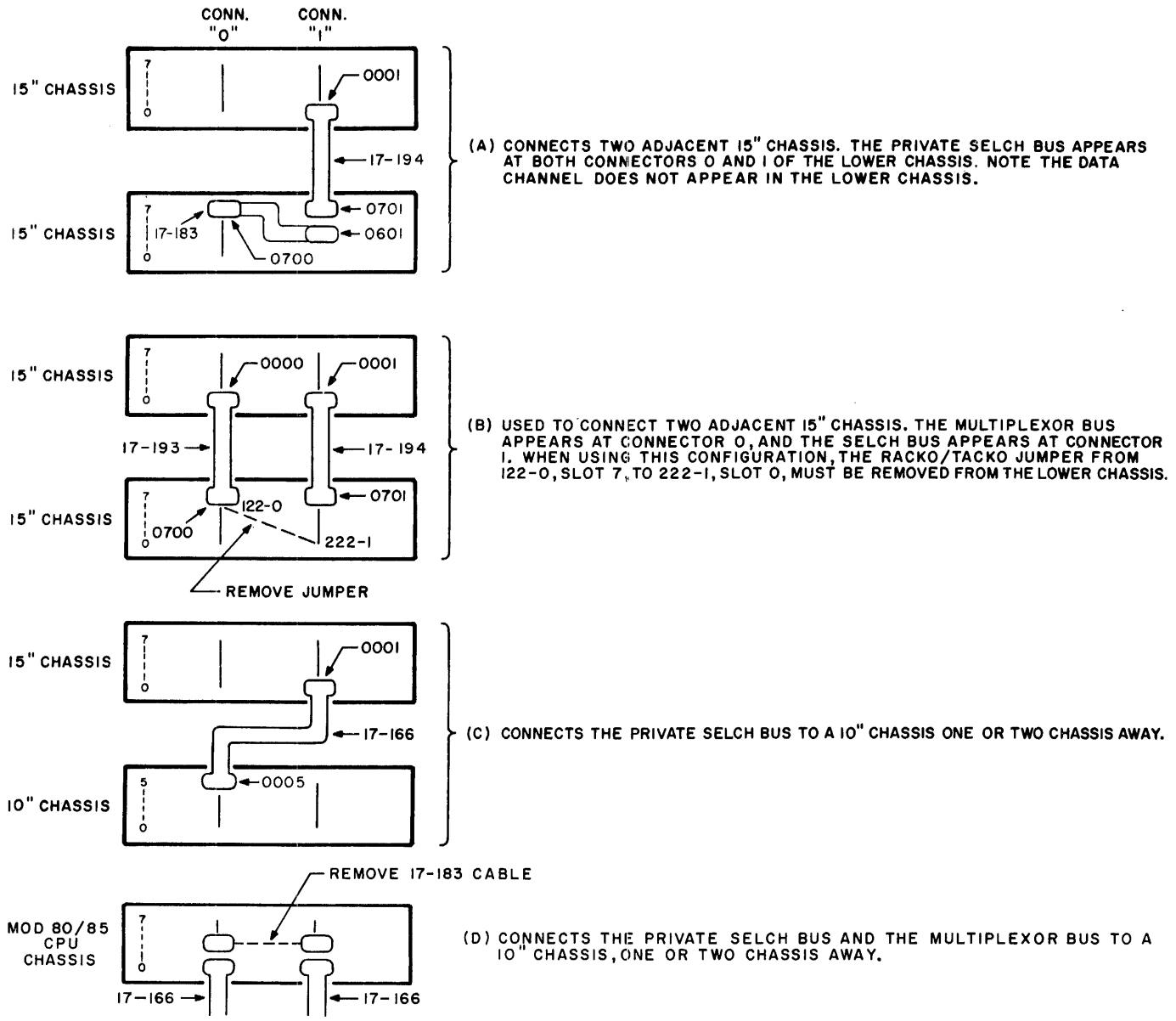

Figure 2. Cabling

4. ADDRESS STRAPPING

The preferred address of the NS Selector Channel is X'F0'. The controller is strapped for this address at the factory. To change the address, refer to Functional Schematic 02-232M01D08. The number and letter designations shown on the schematic refer to the designations on the apparatus side of the SELCH controller board.

5. MODEL 80/85 STRAPPING

For use with the Model 80 or 85 the following options must be exercised:

1. Remove the jumper labled J located between IC 14 and 15.
2. Change the jumper, above IC 53, from (L to X) to (L to 2).

6. INSTALLATION CHECKS

The NS SELCH is factory tested using a special high speed device. Therefore, field checks are contingent upon the user having appropriate hardware and software available with which to exercise the Selector Channel. When the SELC is used with Model 80 or 85, insure that the strap options on the SELCH have been made according to Section 5.

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02-232M01R01A21
June 1974

M70-103
NS SELECTOR CHANNEL
MAINTENANCE SPECIFICATION

1. INTRODUCTION

The 02-232M01 NS Selector Channel (SELCH) (Product Number M70-103) is a Direct Memory Access port (DMA) which provides block data transfer between a device controller and memory. Once initiated, the transfer is independent of the Processor. The Processor sets up the device controller, loads the SELCH with the starting and final addresses of the memory block, specifies the type of operation (Read or Write), and issues a GO Command. The SELCH then handles the transfer without further direction by the Processor.

The NS Selector Channel is complete on one printed circuit board and occupies one slot in a system chassis. The SELCH provides the drivers, receivers and termination resistors for the private SELCH Bus. This bus originates at Connector One (1) of the SELCH slot and extends to each lower numbered slot in the system chassis on the Connector One (1) side only. The private SELCH Bus can be extended to other chassis, as required. For installation information, refer to Installation Specification 02-232M01A20.

2. SCOPE

This specification describes the operation of the SELCH in its various modes; Setup, Memory Read, Memory Write, and Termination. Where necessary, this specification references the Multiplexor Channel Bus and Memory Bus operations. These buses are described in detail in the User's Manual, Publication Number 29-261.

3. BLOCK DIAGRAM ANALYSIS

Refer to the SELCH block diagram on Sheet 7 of Functional Schematic 02-232M01D08, and the SELCH Flow Chart, Figure 1, during the following analysis. Before initiating a data transfer via the SELCH, the device controller and the SELCH must be set up. The setup procedure is implemented by the Processor via the Multiplexor Bus (MPX-Bus). When the SELCH is in the Idle mode, the MPX-Bus is tied directly to the private SELCH Bus through the SELCH. This allows the Processor to communicate directly with any device on the private SELCH Bus.

To prepare the SELCH for data transfer, the Address Register (AR) and Auxiliary Address Register (AAR) must be loaded with the starting address in memory where the transfer is to begin, and the Final Address Register (FAR) must be loaded with the address of the last memory location to be accessed. These registers are loaded from the eight least significant Data Lines D080:150 by four consecutive Data Availables (DAs) from the Processor. The first two Data Availables simultaneously load the AR and AAR, which are 16-bit incrementing registers. The AR is incremented, by two, after each halfword is transferred to/from memory, and the AAR is incremented, by one, with each byte transferred to/from the device. Data transfer is terminated when the AAR is equal to the FAR or when the AAR increments past its maximum value, X'FFFF'.

Data transfer is begun by the Processor issuing a GO Command to the SELCH. Transfer to/from the device is now independent of the Processor. The GO Command also prevents communication between the Processor and any device on the private SELCH Bus until the transfer is terminated and the SELCH is addressed.

Data transfer is controlled in the Move Data circuit by inspection of the four least significant bits of the Status Byte presented by the active device on the private SELCH Bus. When any one of the three least significant bits are set, (EX, EOM, or DU), the transfer is terminated. Bit-12 (Busy) regulates the rate of data transfer. In the Memory Read mode, the actual data transfer begins with a memory request, REQ0 active, as soon as a GO Command is issued. When the memory request is serviced by the Processor, the SELCH Memory Bus Control circuit activates Select (SEL), which gates the contents of the Address Register (AR) onto the Memory Address Bus, and gates a halfword of data from memory into the Data Register (DR). At the termination of the memory transfer, the data is loaded from the DR to the Data Buffer (DB) and the AR is incremented.

NOTE

Unless the SELCH has dropped REQ0 in time to remain selected during the next memory cycle, the SELCH is deselected by the rising edge of Inhibit (INH0) after the halfword has been transferred.

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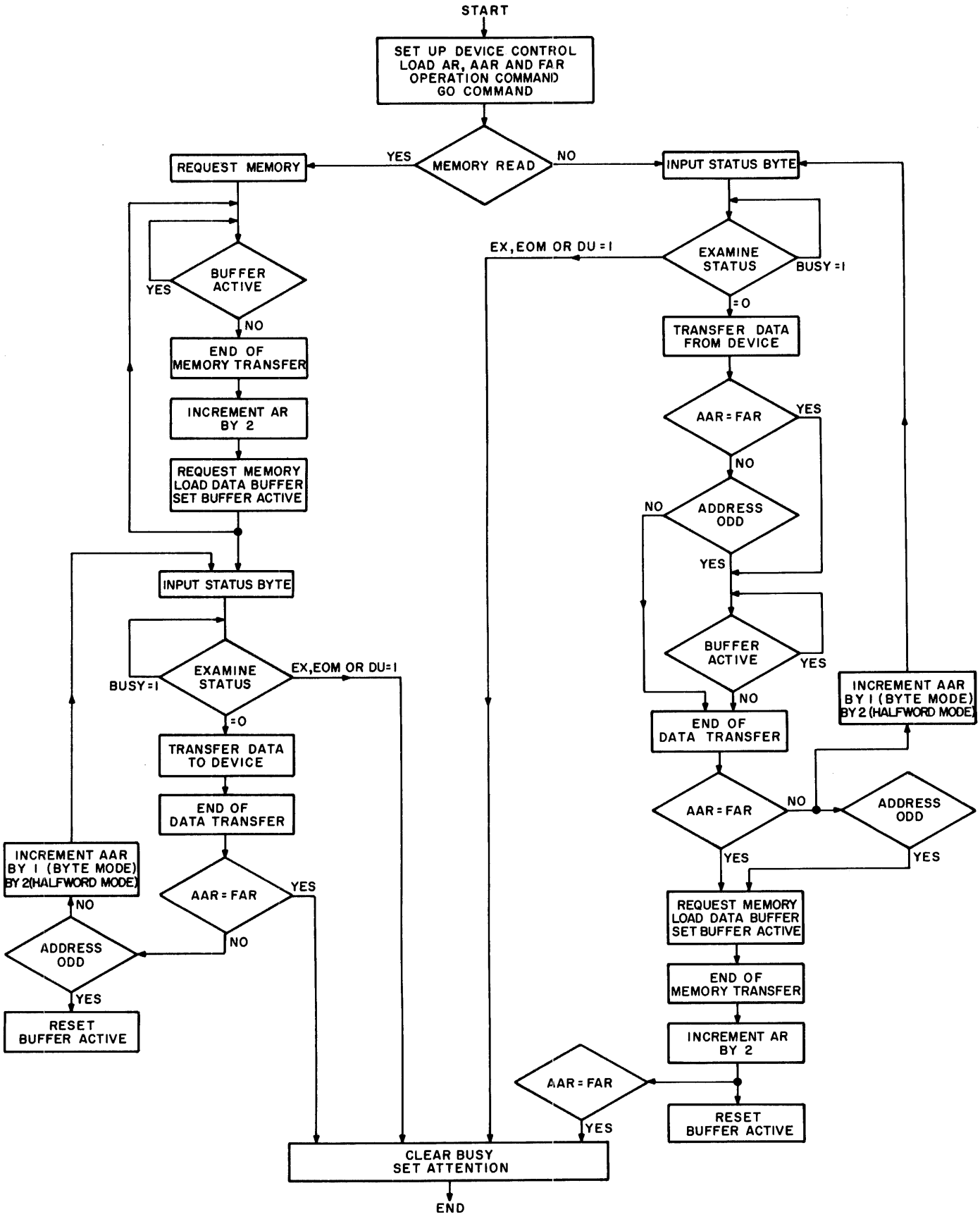

Figure 1. Flow Chart

This information is proprietary and is supplied by INTERDATA for the sole purpose of using and maintaining INTERDATA supplied equipment and shall not be used for any other purpose unless specifically authorized in writing.

Once the DB is loaded, data transfer to the device over Private Data Lines PD000:150 is initiated and, when applicable, a request is made to fetch the next halfword from memory. This cycle continues until either a match is detected between the contents of the Auxiliary Address Register and contents of the Final Address Register, or until the transfer is aborted due to an error condition.

In the Memory Write mode, the data transfer sequence described previously for Memory Read mode is reversed. That is, two bytes of data are loaded into the DR from the device prior to a memory request and the data flow is from the device to the DR, DR to the DB, and finally into memory.

The Branch Gate circuit and the Move Data circuit control the flow of data between memory and the device. The Branch Gate supervises the overall data flow, while the Move Data circuit performs the handshaking between the SELCH and the active device on the private SELCH Bus.

Upon termination of the data transfer, the program is notified via an interrupt and by the inactive state of the SELCH Busy flip-flop which is presented to the program as Bit-12 of the SELCH Status Byte.

Selector Channel Status and Command Byte Data is shown on Table 1.

TABLE 1. SELECTOR CHANNEL STATUS AND COMMAND BYTE DATA

BIT NUMBER	0	1	2	3	4	5	6	7
STATUS BYTE					BSY			
COMMAND BYTE			READ	GO	STOP			

BSY — When this bit is set, a one shot generates the EBS1 pulse to start the appropriate SELCH operation. When this bit is cleared an interrupt is generated.

READ — This command, Bit-2, sets the Memory Write (WT) flip-flop. The controller on the SELCH Bus is setup for a device Read operation.

GO — This command, Bit-3, clears the MSC flip-flop and sets the BSY flip-flop to initiate the Data Transfer mode.

STOP — This command, Bit-4, from the Processor clears the BSY flip-flop and initializes the Load/Unload Sequencer. During the Data Transfer mode, execution of the command is delayed until the end of a memory cycle, if one is in progress.

4. FUNCTIONAL DIAGRAM ANALYSIS

4.1 Introduction

This section relates to Functional Schematic 02-232M01D08, Sheets 1 through 6. Note that in INTERDATA functional schematics, the last character in the mnemonic symbol designates the logic level when the signal is active. For example; D080 is Data Line Number 8 (D08). The last character (0) inidicates that when D080 is active, the line is at a logical Zero level.

4.2 SELCH Control Circuit

In the Idle mode, the SELCH Address (2M8), Busy (3F3), and Multiplexor-SELCH (MSC) (3FA) flip-flops are reset and the private SELCH Bus is tied directly to the Multiplexor Bus. This allows the Processor to communicate, via the Multiplexor Bus, with any device on the private SELCH Bus.

To communicate with the SELCH, it must first be addressed. The SELCH Address (X'F0' preferred) is placed on Data Lines D080:150 (1A3-8) and the Address control line is activated (ADRS0)(4B8). The SELCH Address is decoded by the four input NAND gate (1F4) and the Address flip-flop is set (2M8). The set output from the Address flip-flop (AD1)(2J7), when active, prevents the control signals on the MPX-Bus from passing onto the private SELCH Bus by holding the Control Line Gate inactive (CLG1) (1B2). Capacitors C33 and C34 (4D8) delay the propagation of the Private Address control line (PADRS0) (4F9) to the SELCH Bus, so that when the SELCH is being addressed PADRS0 does not become active. This delay allows the SELCH to be addressed without resetting the Address flip-flop of the active device on the private SELCH Bus.

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The simultaneous loading of the Address Register (AR) and Auxiliary Address Register (AAR), and the loading of the Final Address Register (FAR) is accomplished by four consecutive Data Availables (DAs) from the Processor. The Load/Unload Sequencer (2L2) controls the loading of these registers (AR, AAR, and FAR) and the unloading of the AAR. The sequencer is set to its initial state by the termination of the last data transfer, a Stop Command, or a System Clear (SCLR0)(4MS) so that the first DA, through Data Available Gate (DAG0)(2L4), will activate Load Address Register High (LARH0)(2S2).

LARH0 gates Data Lines DA081:151 (1D3-8) into the eight most significant bits of the AR and AAR. The rising edge of the first and each successive Data Available Gate (DAG0)(2L4) increments the sequencer and allows the next DA to activate the next load line. The second DA loads the eight least significant bits of these registers. The third and fourth DAs will then load the Final Address Register in the same order. The contents of the AAR may be inspected, via the program, by issuing two Data Requests (DR) to the SELCH whenever the Load/Unload Sequencer is in its initial state. (e.g., Upon termination of a SELCH transfer, sequencer initialized, the FAR may be inspected to determine if the entire block of data had been transferred.)

If a Memory Write operation is desired, an Output Command with Bit-10 set must be issued to set the Write flip-flop (3F5). Since the Write flip-flop is reset by the Data Available/Request Gate (DARG1)(2L5) whenever a DA or DR is sent to the SELCH (setup procedure), no command is necessary to initiate a Memory Read operation.

Data transfer commences with a GO Command from the Processor, which is an Output Command with Bit-11 set. The GO Command sets both the Busy (3F3) and MSC (3F4) flip-flops. The setting of the Busy flip-flop causes an End of Busy Set pulse (EBS1) (3H4) to be generated. This pulse is generated from the falling edge of BSY0 (3F3), and is used by the Branch Gate circuit to initiate the transfer cycle. The Busy latch circuit remains set until the Selector Channel detects the termination of transfer and its state is presented to the program via Bit-12 of the Sense Status Byte.

The MSC flip-flop is reset by SCLR0A or by addressing the SELCH, Set Gate active (SGAD1)(2L9), when the Busy flip-flop is reset. The resetting of the MSC flip-flop, MSC0 active, clears any pending interrupt in the Selector Channel.

Information is steered from the SELCH to both the Data Lines D080:150 (1B4-9) and the Private Data Lines PD080:150 (1S4-9) by the proper gating of four each, four-to-one line multiplexors (Sheet 1). For example; with the SELCH idle, Busy reset, all Data Lines are tied directly to the Private Data Lines in both directions.

4.3 Memory Bus Control Circuit

Memory Bus Control timing relationships are shown in Figure 2. A SELCH request for memory is started by activating Set Request (SREQ0)(3S4). SREQ0 is activated by the Branch Gate circuit (3M8) when either the SELCH has received a halfword of data from the device or, in the Memory Read mode, whenever the Memory Data Register is available to accept the next halfword.

SREQ0 is applied to the direct set input of the Request flip-flop (REQ)(4L5) which sets the flip-flop and sends REQ0 to the Processor. When REQ0 is received, the Processor generates Enable (EN0). EN0, on the first DMA device, is jumpered to Accept (ACT0) which generates the daisy chain priority loop through all DMAs in the system. The daisy chain begins at the highest priority DMA as EN0, and propagates to the lower priority DMAs as Transmit Accept (TAC0) until it is captured by the first DMA requesting a memory cycle. When the REQ flip-flop is set and ACT0 (EN0) is active, the ACT0/TAC0 contention circuit (4H2) blocks the propagation of TAC0, and provide highs on the J input to the SEL flip-flop and the K input to the REQ flip-flop. Thus, on the rising edge of EN0, the Select flip-flop becomes set and the Request flip-flop is reset. When the SELCH REQ flip-flop is reset and ACT0 (EN0) is active, the ACT0 signal is propagated as TAC0 to the DMA with a lower priority.

The trailing edge of Inhibit (INH0) (4H5), from the Processor, indicates the end of the memory cycle. This edge, unless the SELCH has dropped REQ0 in time to remain selected during the next cycle, causes the SEL flip-flop to reset. Two pulses, End of Memory Transfer (EMX0) (4M7) and Inhibit (INH0P) (4M2), are generated by the leading and trailing edges of INH0 respectively. EMX0 is used by the Branch Gate circuit to indicate the end of the memory transfer. The Address Register is toggled by the AND function of SEU and INH1.

In the Memory Read mode, the Memory Data Register (MDR) is cleared by Clear Data Register (CDR0) (4R2) which is generated by the trailing edge of REQ1. Write Not (WT0A) (3F5) is ANDed with SEL1 to form Enable Memory Data Read (ENMDR1) (4R6), which gates the contents of the MDR onto the Memory Data Lines MD000:150 (Sheet 6) for the restore portion of the memory cycle. (This function is disabled when using solid state memory.) The contents of the memory location accessed is gated to the direct set inputs of the MDR by Enable Memory Strobe (ENMS1) (4R4). This function is WT•SEL•CDR0 for use with core memory and WT•SEL•INH when using solid state memory (4R4).

When writing to memory, the contents of the Data Buffer is gated onto Memory Data Lines MD000:150 (Sheet 6) by Enable Memory Data Write (ENMDW1)(4R3), when selected. A Memory Write operation is indicated to the Processor by activating WRT0A (4S3).

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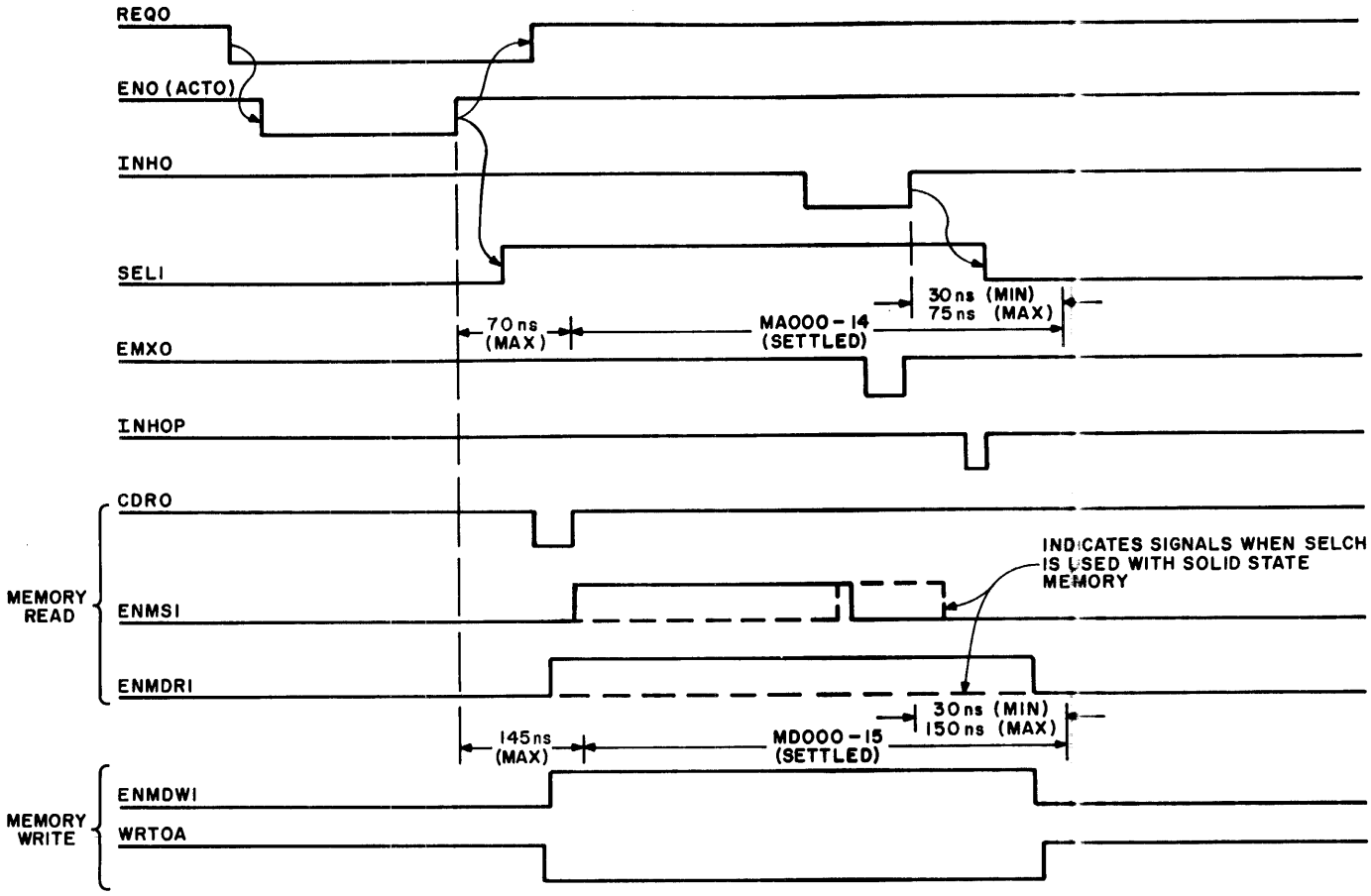

Figure 2. Memory Bus Control Timing Diagram

4.4 Address Register and Auxiliary Address Register.

The Address Register (AR) and Auxiliary Address Register (AAR) (Sheet 5) each consist of four, four-bit counters. These registers are loaded simultaneously by the Processor from Data Lines D080:150 (1A3-8), under control of the Load/Unload Sequencer (as discussed in Section 4.2), with the starting address from which the block transfer is to begin. The contents of the AR (Sheet 5) is gated onto Memory Address Lines MA000:140 (5R1-8) whenever the SELCH is selected, SEL flip-flop set. The AR is incremented with each memory transfer by Select Inhibit (SINH0) (4K8). The AAR (Sheet 5) keeps track of the transfer between the SELCH and the device. This register is incremented, by one, for each byte of data transferred by Toggle Auxiliary Address Register (TAAR0) (3M1). When the transfer is in the Halfword mode, TAAR0 is generated twice for each transfer. The outputs of the AAR are used by the Match circuit to determine the end of the data block. Its contents may be examined, via the program, by issuing two consecutive DRs to the SELCH when the sequencer is initialized. In addition, AAR151 is used in the Byte Transfer mode to determine whether the byte being transferred is odd or even, for byte steering. Carry Out from the most significant stage of the AAR (CO0) (541) terminates the transfer, clear Busy, when a transfer is attempted past the maximum memory address. This feature prevents 'wrap-around' in memory.

4.5 Final Address Register

The Final Address Register (FAR) is implemented by four quad latches (Sheet 5). This register, like AR and AAR, is loaded by the Processor under control of the Load/Unload Sequencer. The outputs of this register are used exclusively by the Match circuit to determine when the final address of the transfer is reached.

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4.6 Memory Data Register and Data Buffer

The Memory Data Register (MDR)(Sheet 6) is a16-bit register composed of 16 edge triggered JK flip-flops. In the Memory Read mode, the MDR is first cleared by Clear Data Register (CDR0) (4R2) and then direct set by each active bit on Memory Strobed Data Lines MS000:150 (Sheet 6). During a Memory Write, the data, in double rail format, present at the J and K inputs to the MDR, is toggled into the flip-flops on the trailing edge of either Load Data Register High (LDRH0)(649) or Load Data Register Low (LDRL0)(6J9).

As soon as the MDR is loaded, if the Data Buffer (DB) is empty (as determined by the inactive state of the Buffer Active flip-flop)(3H1), the MDR contents are loaded into the DB (Sheet 6) by Load Data Buffer (LDB1)(357). Information present in the DB is, in turn, either written into memory via Memory Data Lines MD000:150 or sent to the device on Private Data Lines PD000:150.

4.7 Data Transfer Circuit

Refer to Figure 3 for Memory Read timing diagrams and Figure 4 for Memory Write timing diagrams. The Memory Read timing diagram shows the timing of a three byte transfer, in the Byte mode, of 2,000,000 bytes/second. Figure 4 shows a transfer of two halfwords, in the Halfword mode, to a slower device.

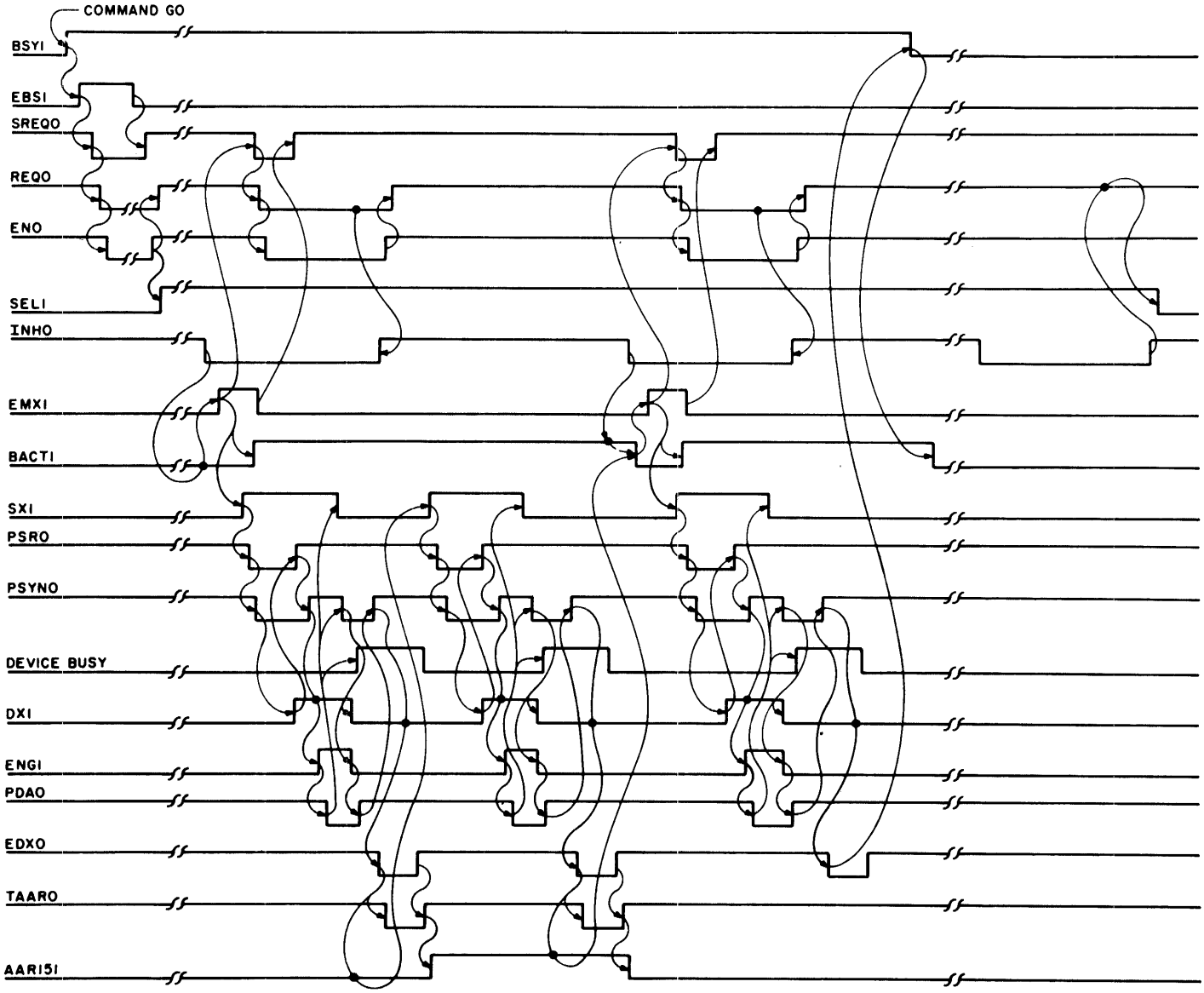

Figure 3. Memory Read (Byte Mode)

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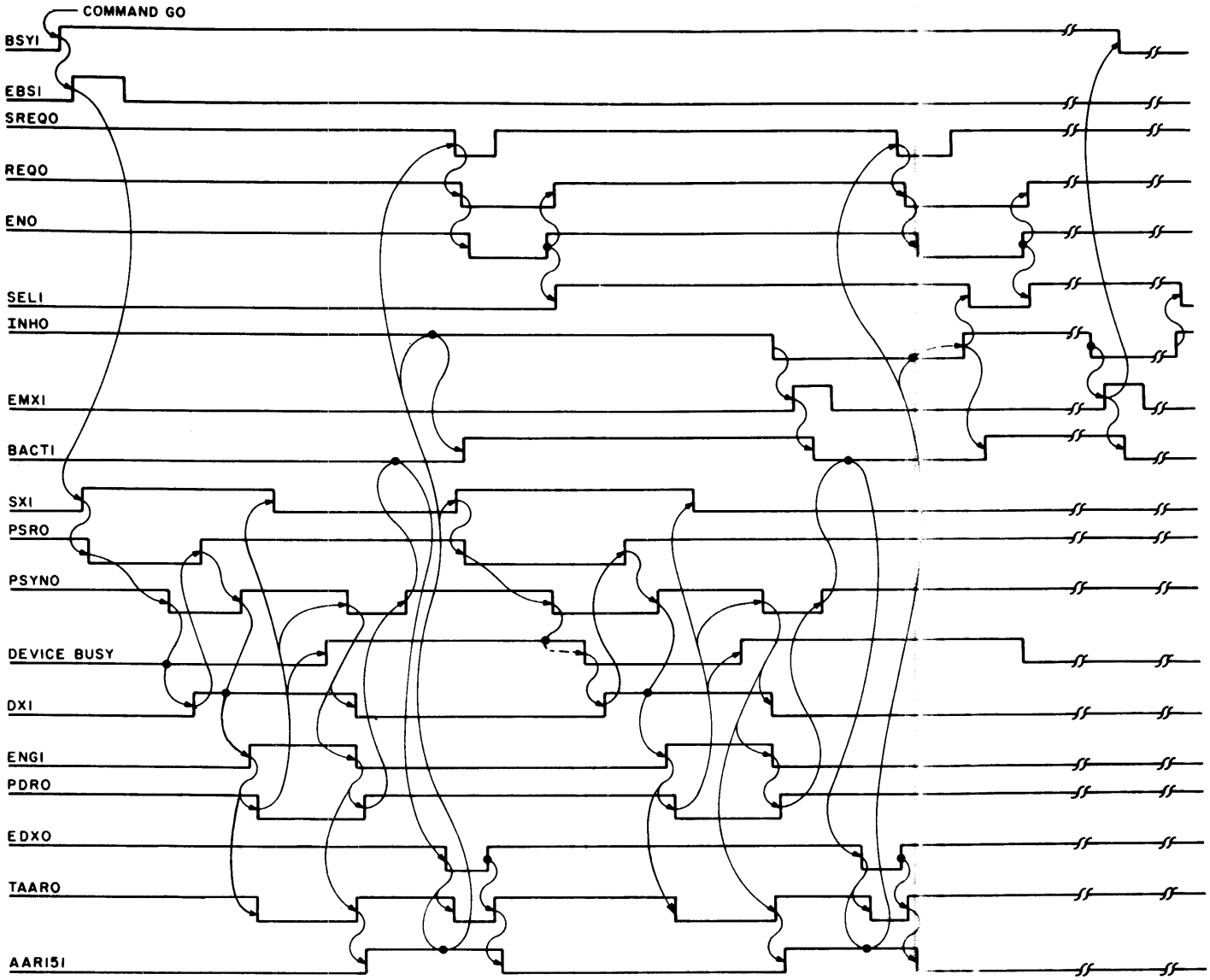

Figure 4. Memory Write (Halfword I/O Mode)

A GO Command to the Selector Channel sets the Busy flip-flop which generates the End of Busy Set pulse (EBS1)(3K8).

In the Memory Read mode, EBS1 is decoded by the Branch Gate circuit and SREQ0 is generated. Thus, a request for memory is initiated. When the halfword of data is present in the MDR, the End of Memory Transfer pulse (EMX1)(4R6) becomes active and the Branch Gate circuit once again requests memory and generates Set Status Transfer (SSX0)(3S5) and Load Data Buffer (LDB1) (3S7). These signals initiate the transfer to the device and load the Data Buffer (DB) respectively.

SSX0 sets the Status Request flip-flop (3F6) which activates the Private Status Request control line (PSR0)(3G6) to the active device on the private SELCH Bus. This Status Request examines the four least significant bits of the Status Byte. If any of the three least significant bits (EX, EOM, or DU) are set, the transfer is terminated by resetting the Busy flip-flop (3F3). The assumption is made that each of these status bits remain reset for the remainder of this discussion. With Bit-12 (Busy) of the Status Byte reset, the Data Transfer flip-flop becomes set (3F7). Data Transfer (DX0)(3E1) inhibits the generation of PSR0, which causes Private Sync (PSYN1)(4B4) from the device to become inactive. This enables Engage to go high (ENG1)(3D8), which allows the Private Data Available control line (PDA0)(3H5) to become active. The Private Data Available/Request signal (PDAR1)(3H5), generated whenever a Private Data Available (PAD0) or Private Data Request (PDR0) signal is active, will then clear the Status Request flip-flop. Upon receipt of Sync from the device, PSYN1 active, the Data Transfer flip-flop becomes reset and ENG1 goes low, disabling PAD0. When the Sync is removed by the device, an 80 nanosecond End of Data Transfer pulse is generated (EDX0) (3J8) which increments the Auxiliary Address Register and is used by the Branch Gate circuit to generate a function in accordance with the truth table for EDX on Sheet 3. This cycle continues until termination of the transfer is detected.

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In the Memory Write mode, WT1 active (3F5), EBS1 is used to generate SSX0, and the Branch Gate circuit directs the loading of a halfword of data into the DB before a memory request is made. The transfer of data from the device is the same as described in the Memory Read mode, except that ENG1 is used to generate the Private Data Request control line (PDR0)(3H5) rather than PDA0. Data from the device is loaded into the MDR on the trailing edge of either Load Data Register High (LDRH0)(2R2) or Load Data Register Low (LDRL0)(2R2), depending on which eight bits are being loaded. In the Halfword Transfer mode, both LDRH0 and LDRL0 are generated simultaneously. With WT1 active, the generation of EDX1 is delayed by activating the clear input to the one-shot (3H8) when the Buffer Active flip-flop is set (BACT1)(3H1), if either the transfer to the device is on an odd boundary or when a Match is detected (MCH0)(5J2). This prevents the reloading of the Data Buffer (DB) before the last halfword has been written into memory.

4.8 RACK0/TACK0 Contention Circuit

The Selector Channel directs the propagation of the Acknowledge signal to lower priority devices on the Multiplexor Channel Bus as well as devices on the private SELCH Bus. If the Selector Channel Attention flip-flop (4B4) is set, the SELCH captures the Receive Acknowledge signal (RACK0) (4B3), place its device address on the Data Lines and return Sync to the Processor, Attention Sync (ATSYN0)(4F4) active. If the Attention flip-flop is reset, RACK0 is propagated as either Private Transmit Acknowledge (PTACK0)(4F2) or Transmit Acknowledge (TACK0)(4F3). Since devices on the private SELCH Bus have a higher interrupt priority than devices below the SELCH on the MPX Bus; if the Private Attention Test line is active (PATN0) (4B1), PTACK0 is generated rather than TACK0. Note that when MSC0 is high (3F4), PATN0 is disabled so that a device on the private SELCH Bus may not interrupt the Processor while the SELCH is active.

5. MAINTENANCE, TROUBLE SHOOTING, AND TEST

Before attempting any maintenance or testing, insure that the necessary back panel modifications and SELCH board option strapping have been made in accordance with the NS Selector Channel Installation Specification 02-232M01A20.

To insure a 2,000,000 Byte/second transfer rate in the Byte Transfer Mode, it is necessary to limit the maximum delay between PDA0, PDR0, and PSR0 and the return of Sync from the device (PSYN0), to 30 nanoseconds. In addition, the device must be ready for the next byte of data, Busy Status Bit reset, whenever a Status Request is made. Field testing of this device is contingent upon the user having appropriate software and hardware available with which to exercise the Selector Channel. There are no adjustments associated with this device. Do not install Terminator Boards 35-433 or 35-434 on the SELCH bus if a transfer rate of 2,000,000 Bytes/second is to be maintained in the Byte (8 Bit) Mode. The SELCH Bus should be contained on a single 15 inch chassis if no terminators are used.

6. MNEMONICS

The following list provides a brief description of each mnemonic found in the SELCH. The source of each signal on Functional Schematic 02-232M01D08 is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
AAR001:151	Outputs of the Auxiliary Address Register	5F1-5F9
ACT0	Accept - Request for memory accepted by Processor	4H1
AD1	Address - Active when SELCH is addressed	2K7
ADRS0	Address control line from MPX-Bus	4B8
AG081:151	Address Gated Lines - Output of Address Strap	1E3 - 1E8
ATN0	Attention - Attention to Processor	4F1
ATSYN	Attention Sync - Generated by an Acknowledge Attention from Processor	4F4
BACT1	Buffer Active - Indicates that valid data is present in the DB	3H1
BSY	Busy - Indicates a data transfer is in progress	3F3
CDR0	Clear Data Register - Clears MDR prior to loading from MS000:150	4R2
CBSY0	Clear Busy - Terminates transfer when a match is detected	3M3
CL070	Control Line 7 - Control Line from MPX-Bus	4B6
CLG1	Control Line Gate - Gates Private Control Lines	1C2

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MNEMONIC	MEANING	SCHEMATIC LOCATION
CLUS0	Clear Load/Unload Sequencer - Clears Sequencer	3S2
CMD0	Command Control Line from MPX-Bus	4B8
CMG	Command Gated by AD1	2S7
CO0	Carry Out of the AAR - Prevents Memory 'Wrap-around'	5A1
D000:150	Data Lines from MPX-Bus	1A3 - 1A8 2A1 - 2A8
DA0	Data Available Control Line from MPX-Bus	4B7
DLG0	Data Line Gate - Gates Data Lines and Private Data Lines	1R2 - 1D3
DB001:151	Outputs of Data Buffer	6G2 - 6G9 6R2 - 6R9
DR0	Data Request Control Line from MPX-Bus	4B7
DRG0	Data Request Gated by AD1	2L5
DX	Data Transfer flip-flop	3F8
EBS1	End of Busy Set - Signals the start of a SELCH transfer	3J4
EDX1	End of Data Transfer - Signals the end of a device transfer	3J8
EMX1	End of Memory Transfer - Signals the end of a memory transfer	4R7
EN0	Enable from Memory Bus	4H2
ENG1	Engage - Gates either PDS0 or PDR0	3D8
ENMDR1	Enable Memory Data Register Read - Gates contents of MDR to MD000:150	4R6
ENMDW1	Enable Memory Data Register Write - Gates contents of DB to MD000:150	4R3
ENMS1	Enable Memory Strobe - Gates contents of MS000:150 to MDR	4R4
HW0	Halfword Control Line from MPX-Bus	1D2
INH0	Inhibit from Memory Bus	4H5
LARH0	Load Address Register High - Loads AAR and AR, Bits 00:07	2R2
LARL0	Load Address Register Low - Lards AAR and AR, Bits 08:15	2R2
LDB1	Load Data Buffer - Load contents of MDR to DB	3S2
LDRH0	Load Data Register High - Loads MDR Bits 00:07	3F8
LDRL0	Load Data Register Low - Loads MDR Bits 08:15	3H9
LFRH0	Load Final Address Register High - Loads FAR Bits 00:07	2S3
LFRL0	Load Final Address Register Low - Loads FAR Bits 08:15	2S3
MA000:140	Memory Address Lines to Memory Bus	5R1 - 5R8
MCH1	Match - Indicates a match between AAR and FAR	5J6

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MNEMONIC	MEANING	SCHEMATIC LOCATION
MD000:150	Memory Data Lines to Memory Bus	6G1 - 6G8 6R1 - 6R8
MS000:150	Memory Strobed Data Lines from Memory Bus	6A1 - 6A8 6H1 - 6H8
MSC0	Multiplexor SELCH Control flip-flop	3F4
PADRS0	Private Address Control Line to SELCH Bus	4F8
PATN0	Private Attention from SELCH Bus	4B1
PCL070	Private Control Line 7 to SELCH Bus	4R6
PCMD0	Private Command Control Line to SELCH Bus	4F8
PD000:150	Private Data Lines - SELCH Bus	2F1 - 2F8 1S3 - 1S9
PDA0	Private Data Available Control Line to SELCH Bus	3H5
PHW0	Private Halfword Control Line from SELCH Bus	1A1
PSR0	Private Status Request Control Line to SELCH Bus	3H6
PSYN0	Private Sync from SELCH Bus	4B5
PTACK0	Private Transmit Acknowledge to SELCH Bus	4F2
RACK0	Receive Acknowledge from MPX-Bus	4B5
RBA0	Reset Buffer Active - Resets Buffer Active flip-flop	3M2
REQ0	Request - Request for memory cycle to Memory Bus	4R5
SCLR0	System Clear - Initialize Signal	4H4
SGAD1	Set Gate - Sets Address flip-flop	2LR
SR0	Status Request Control line from MPX-Bus	4B6
SREQ0	Set Request - Initiates a request for memory	3S4
SSX0	Set Status Transfer - Sets the Status Request flip-flop	3S5
SX	Status Transfer - Status Request flip-flop	3F6
SYN0	Sync to MPX-Bus	2S5
TAC0	Transmit Accept - To lower priority DMAs	4R1
TACK0	Transmit Acknowledge - To lower priority devices on MPX Bus	4F3
TAAR0	Toggle Auxiliary Address Register - Increments AAR	3M1
TAR0	Toggle Address Register - Increments AR	4S7
UAAH0	Unload Auxiliary Address Register High - Unloads AAR Bits 00:07	2R4
UAARL0	Unload Auxiliary Address Register Low - Unloads AAR Bits 08:15	2R4
WT	Write flip-flop	3F5
WRT0A	Write to Memory Bus, when selected	4R3

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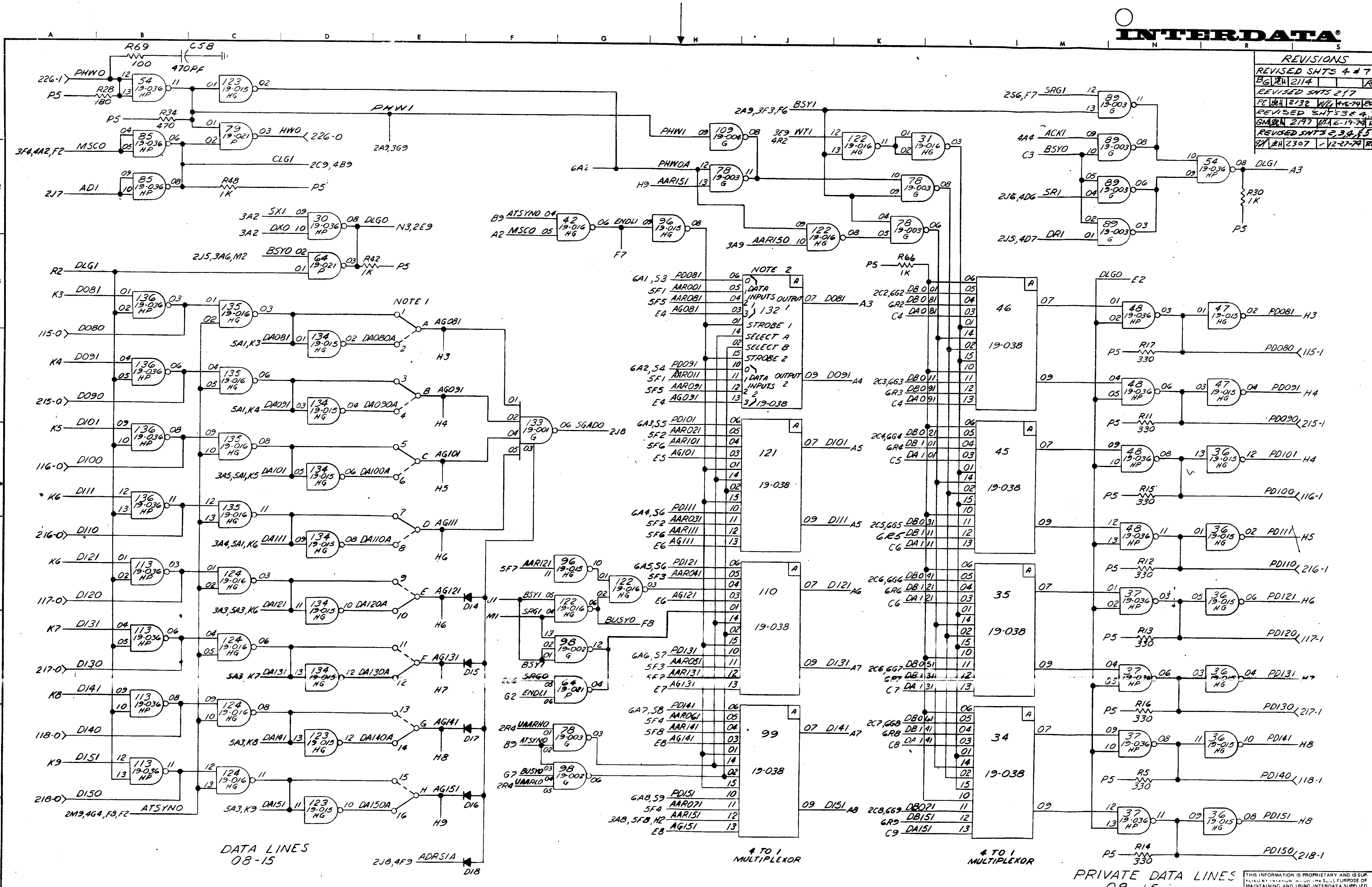

REVISIONS					
REVISED SHTS 4 & 7					
BG	JCH	2114			R01
REVISED SHTS 2 & 7					
PE	JCH	2132		4-16-74	R02
REVISED SHTS 3 & 4, 7					
GM	JCH	2197		6-19-74	R03
REVISED SHTS 2,3,4, & 5					
	JCH	2307		12-27-74	R04

NOTES 1. PREFERRED ADDRESS X'FO'

ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-391 M02 SELECTOR CHANNEL.

SHEET INDEX	SHEET	1	2	3	4	5	6	7
	REV NO.	4	3	3	3	2	1	8

REVISION LEVEL OF SHEET 1 IS CONSIDERED TO BE THE REVISION LEVEL OF THIS DOCUMENT.

NAME	TITLE	DATE
W ZILLGER	DRAFT	10-5-71
R CERO	CHK	2-6-73
D. FRANKENBERGER	ENGR	2-7-73
N. MASI	SYS TST	2-7-73
R.E. JONES	DIR ENG	

TITLE NS SELECTOR CHANNEL

TASK NO. 03075

DWG NO. 02-232M01D08

SHEET 1 OF 7

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BRUNING 44-231 15043

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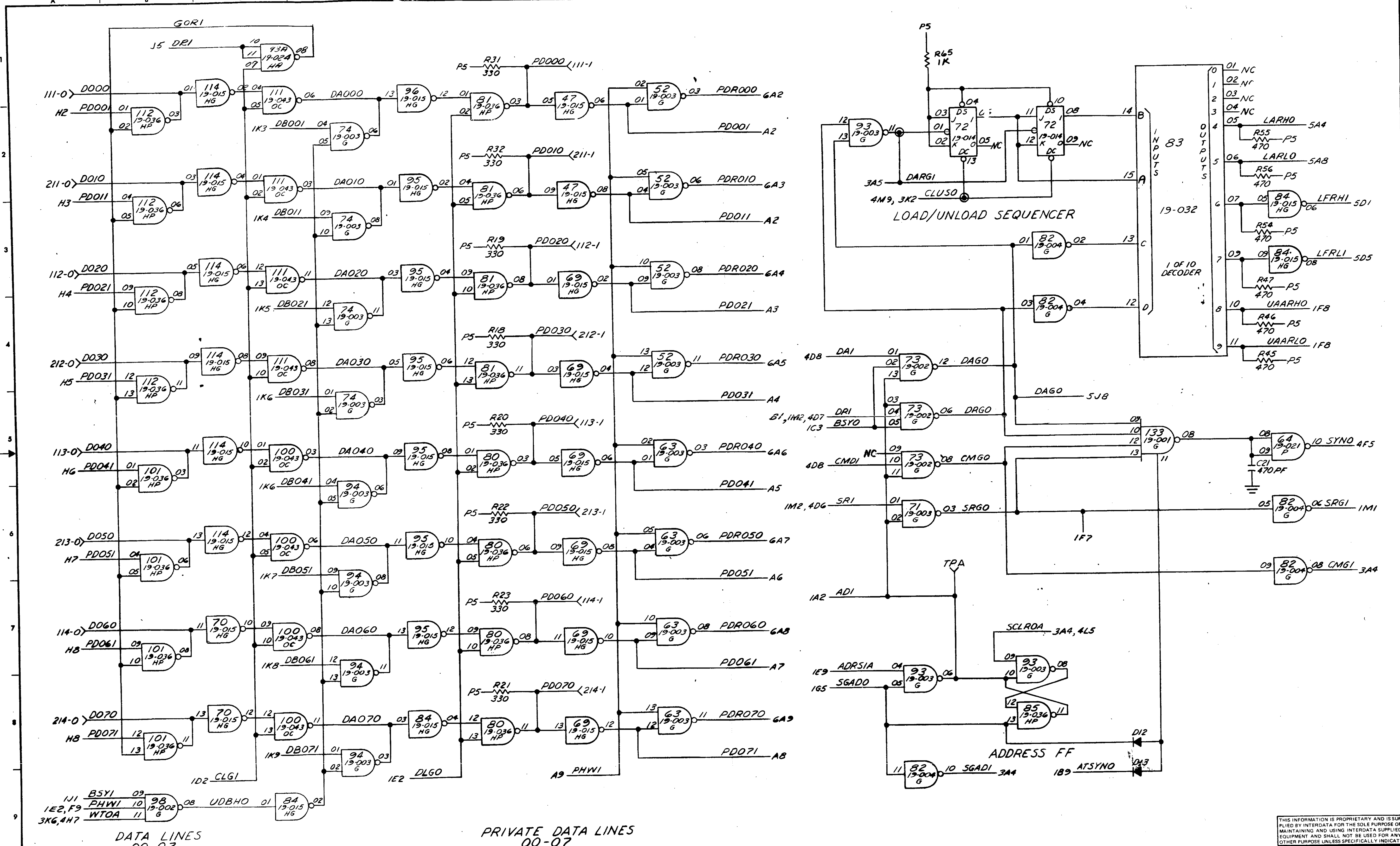

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NOTES
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AREA K5 DELETED "SELO", TO A73-09 — MA2307 — 12-27-79 — R03

AREA 81: ADDED, 93A. AREA A8: A101-13, DLG1, WAS CONN TO DLG1 @ 1A3 — 2132 — 4-16-74

AREA N2, A, F8 WERE REVERSE.

NAME		DATE
W ZILLGER	DRAFT	10-5-71
	CHK	
	ENGR	
	DIR ENG	

TITLE NS SELECTOR CHANNEL

TASK NO. 03075

DWG NO. 02-232M01R08 D08

SHEET 2-7

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CIRCUIT NOTES

MAP FOR EDX (END OF DATA XFER)

	WTO	WTI	
MCH0	000 SSX	100 SSX	(EVEN) AARI5O
	001 RBA	101 SREQ,SSX,LDB	(ODD) AARI5I
MCH1	011 CBSY	111 SREQ,LDB	
	010 CBSY	110 SREQ,LDB	(EVEN) AARI5O

MAP FOR EMX (END MEM. XFER)

	WTO	WTI
MCH0	SREQ,SSX,LDB	RBA
MCH1	SREQ,SSX,LDB	RBA

MAP FOR EBS (END BSY SET)

WTO	WTI
SREQ	SSX

BUFFER ACTIVE FF

BUSY FF

MUX/SELCH FF

WRITE FF

STATUS REQ FF

DATA XFER FF

ONE SHOT

1 OF 10 DECODER

BRANCH GATES

NOTES
ALL APPARATUS ON THIS SHEET IS LOCATED ON 35-391 MO2 SELECTOR CHANNEL.

REVISIONS

CHANGED: LEAD FROM 71-05 TO 71-11 WAS FROM 71-05 TO 71-09	2307	12-27-74	003
2197	6-19-74	002	
AGRA J9, EBSI NOT USE.			

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NAME	TITLE	DATE
W ZILLGER	DRAFT	
	CHK	
	ENGR	
	DIR ENG	

TITLE: NS SELECTOR CHANNEL

TASK NO. 03075 | DWG NO. 02-232 | REV 8 | SHEET OF 3-7

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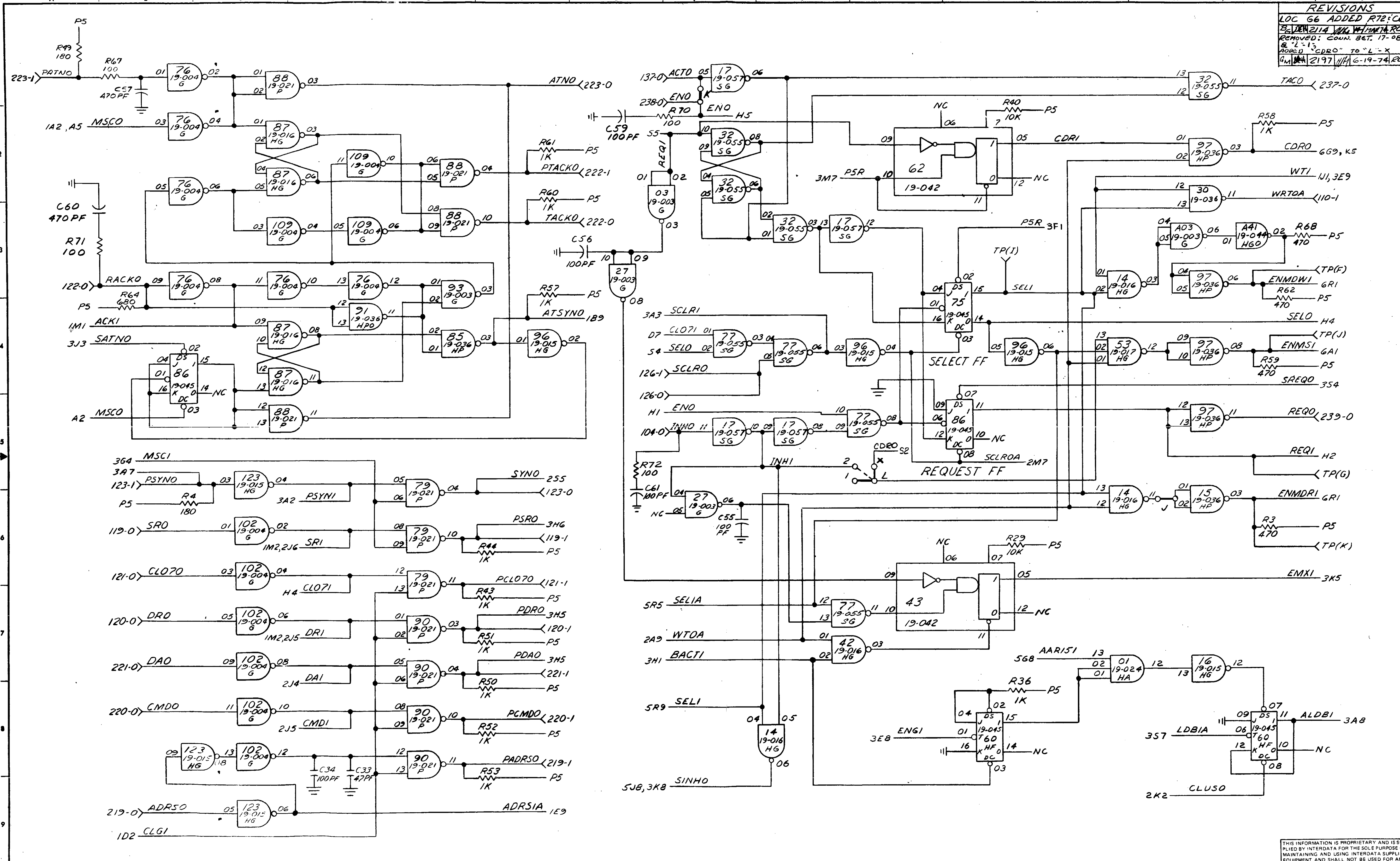
REVISIONS
LOC G6 ADDED R72 & C61
B [illegible] 2114 [illegible] R01
REMOVED: CONN. BET. 17-08 & "L"-1; ADDED "CDRO" TO "L"-X
C M [illegible] 2197 [illegible] 6-19-74 R02



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NOTES

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REVISIONS
AREA H4, DELETED CONN. 2J5 FROM SELO
[illegible] 2307 [illegible] R03

NAME		DATE
N ZILLGER	DRAFT	10-5-71
	CHK	
	ENGR	
	DIR ENG	

TITLE NS SELECTOR CHANNEL

TASK NO 03075

DWG NO 02-232M01R03D08

SHEET 4 OF 7

INTERDATA®

IC4, J5 DA08I
IC4, J5 DA09I
IC5, J5 DA10I
IC6, J7 DA11I
3E2 COO

115
19-035
CARRY OUT
BORROW
CLEAR
LOAD
CNT DWN
CNT

253 LFRH1

AAR001 1H3
AAR011 1H4
AAR021 1H5
AAR031 1H5
AAR041 1H6
AAR051 1H7
AAR061 1H8
AAR071 1H9
AAR081 1H3
AAR091 1H4
AAR101 1H5
AAR111 1H6
AAR121 1F6
AAR131 1H7
AAR141 1H8
AAR151 1H9, 3A8, 4M7

T 126/127/128/129 19-027 D

104/105/106/107 19-029 XOR

108 19-001 G
109 19-004 G
16 19-015 H6

MCH0 3A9
MCH1 3J4

D4 D5 D6 D7 D8 D9 D10 D11

116 19-035
117 19-035
118 19-035

IC6, J7 DA12I
IC7, J7 DA13I
IC8, J8 DA14I
IC9, K1 DA15I
2R2, K2 LARH0

2R2, J9 LAR10
P5
3N1 TAAR0
LB P5R
RG3 1K

AUXILIARY ADDRESS REGISTER
FINAL ADDRESS REGISTER
MATCH CIRCUIT

A1 DA15I
A4 LARH0

131 INPUTS OUTPUTS 19-070
CLK ENP ENT CAR LD
4 BIT COUNTER

125 19-036 HPO
MA000 106-0
MA010 107-0
MA020 109-0
MA030 110-0

130 19-070
103 19-036 HPO
MA040 210-0
MA050 129-0
MA060 229-0
MA070 130-0
SEL1A 4G7

120 19-070
92 19-036 HPO
MA080 230-0
MA090 131-0
MA100 231-0
MA110 132-0

A1 DA08I
A1 DA09I
A1 DA10I

119 19-070
91 19-036 HPO
MA120 232-0
MA130 133-0
MA140 233-0
SEL1 4G8

A1 DA11I
A3 DA12I
A3 DA13I
A3 DA14I
2M4 DA60
4H8 SUMM0
934 19-024 HA
B8 P5R
A8 LAR10
3G4 MSC0

ADDRESS REGISTER

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NOTES
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REVISIONS
AREA MI, DESIG WAS PIN 6 TO A, PIN 5 TO B, PIN 4 TO C, PIN 3 TO D, PIN 7 TO ENT, & PIN 10 TO ENP.
2307 | 12-27-74 | B02

NAME	TITLE	DATE
W ZILLGER	DRAFT	10-5-71
	CHK	
	ENGR	
	DIR ENG	

TITLE: SELECTOR CHANNEL

TASK NO. 03075
DWG NO. 02-232M01/R2008
SHEET OF 5-7

BRUNING 44 231 15043

INTERDATA®

DATA REG HIGH

DATA BUFFER

DATA REG LOW

DATA BUFFER

4R4,H1 ENMS1

210-1 MS000 — 1H3,H2 PD081 — 1H2 PHWOA — 2H1 PDR000

109-1 MS010 — 1H4,H3 PD091 — 2H2 PDR010

209-1 MS020 — 1H4,H4 PD101 — 2H3 PDR020

108-1 MS030 — 1H5,H5 PD111 — 2H4 PDR030

208-1 MS040 — 1HG,HG PD121 — 2H5 PDR040

107-1 MS050 — 1H7,H7 PD131 — 2H6 PDR050

207-1 MS060 — 1H7,H8 PD141 — 2H7 PDR060

106-1 MS070 — 1H8,H9 PD151 — 2H8 PDR070

3GB LDRH0 — 3G9 LDRH1 — R7 470Ω — P5

MD000 (229-1) — DB001 1K3

MD010 (130-1) — DB011 1K4

MD020 (230-1) — DB021 1K5

MD030 (131-1) — DB031 1K5

MD040 (231-1) — DB041 1KG

MD050 (132-1) — DB051 1K7

MD060 (232-1) — DB061 1K8

MD070 (133-1) — DB071 1K9 — LDB1 R9,357 — CDR0 R9,4R2

A1 ENMS1

206-1 MS080 — A1 PD081

105-1 MS090 — A2 PD091

205-1 MS100 — A3 PD101

104-1 MS110 — A4 PD111

204-1 MS120 — A5 PD121 — 3A1 PDR120

103-1 MS130 — AG PD131 — 3A1 PDR130

203-1 MS140 — A7 PD141 — 3A1 PDR140

102-1 MS150 — AB PD151 — 3A1 PDR150 — 3J9 LDRL0

R35 470Ω — P5

ENMDR1 4RG

ENMDW1 4R3

MD080 (233-1) — DB081 1K3

MD090 (134-1) — DB091 1K4

MD100 (234-1) — DB101 1K5

MD110 (135-1) — DB111 1KG

MD120 (235-1) — DB121 1KG

MD130 (136-1) — DB131 1K7

MD140 (236-1) — DB141 1K8

MD150 (137-1) — DB151 1K9 — LDB1 G9 — CDR0 G8

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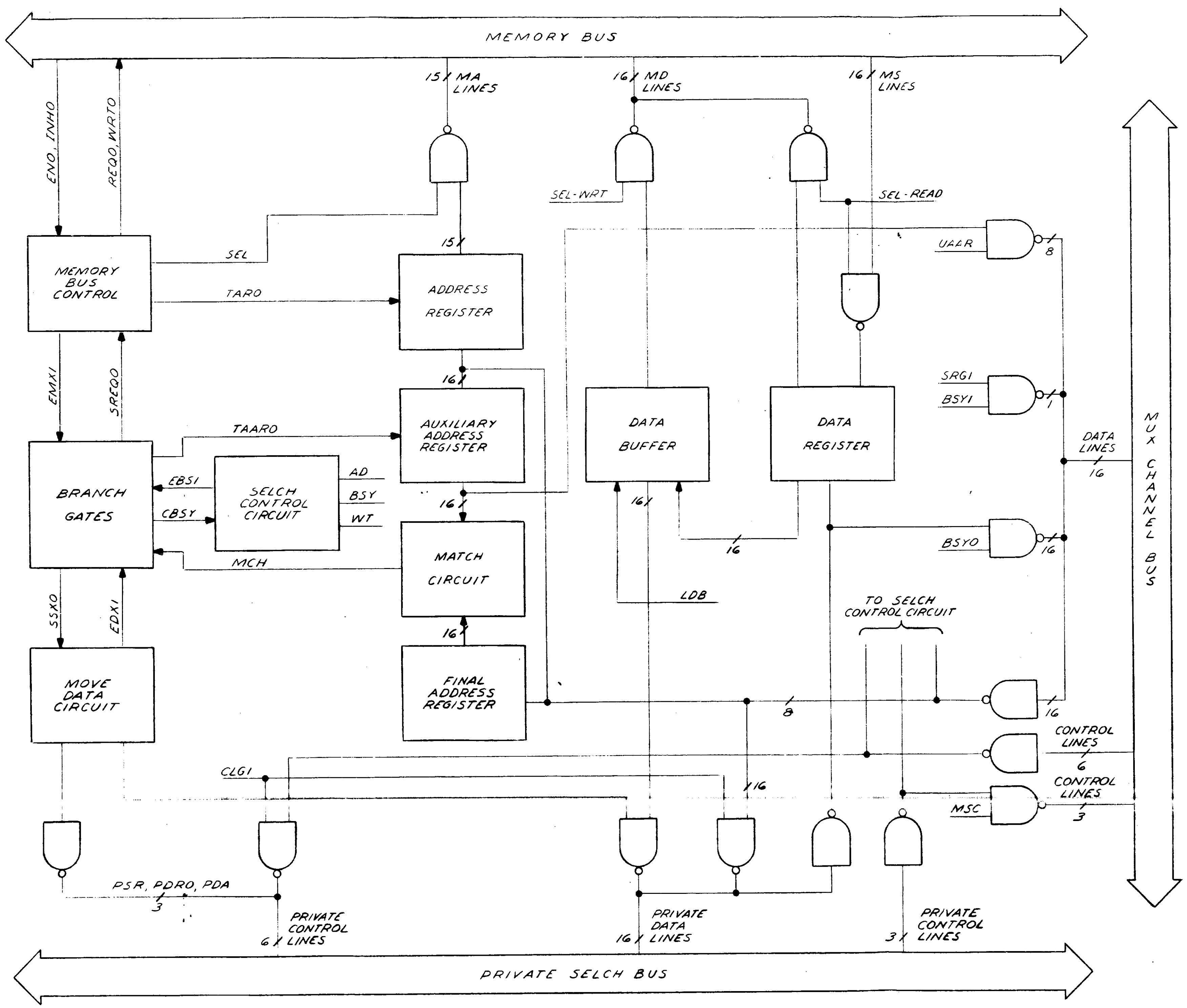
NAME	TITLE	DATE	TITLE
W ZILLGER	DRAFT	10-5-71	NS SELECTOR CHANNEL
	CHK		
	ENGR		
	DIR ENG		TASK NO. 03075 — DWG NO. 02-232M01/R01D08 — SHEET OF 6-7

BRUNING 44 231 15043



BACK PANEL PIN INDEX			
MNEM	LOC.	MNEM.	LOC.
ACTO	4H1	MD130	6R6
ADRSO	4B8	MD140	6R7
ATNO	4F1	MD150	6R8
CLO70	4B6	MS000	6A1
CMDO	4B8	MS010	6A2
D000	2A1	MS020	6A3
D010	2A2	MS030	6A4
D020	2A3	MS040	6A5
D030	2A4	MS050	6A6
D040	2A5	MS060	6A7
D050	2A6	MS070	6A8
D060	2A7	MS080	6H1
D070	2A8	MS090	6H2
D080	1A3	MS100	6H3
D090	1A4	MS110	6H4
D100	1A5	MS120	6H5
D110	1A6	MS130	6H6
D120	1A6	MS140	6H7
D130	1A7	MS150	6H8
D140	1A8	PADRSO	4F8
D150	1A8	PATNO	4B1
DAO	4B7	PCLO70	4F6
DRO	4B7	PCMDO	4F8
ENO	4H1	PD000	2F1
HWO	1D1	PD010	2F2
INHO	4H5	PD020	2F3
MA000	5R1	PD030	2F4
MA010	5R1	PD040	2F5
MA020	5R2	PD050	2F6
MA030	5R2	PD060	2F7
MA040	5R3	PD070	2F8
MA050	5R3	PD080	1R4
MA060	5R4	PD090	1R4
MA070	5R4	PD100	1R5
MA080	5R5	PD110	1R6
MA090	5R6	PD120	1R7
MA100	5R6	PD130	1R7
MA110	5R7	PD140	1R8
MA120	5R7	PD150	1R9
MA130	5R8	PDAO	4F7
MA140	5R8	PDRO	4F8
MD000	6G1	PHWO	1A1
MD010	6G2	PSRO	4F6
MD020	6G3	PSYNO	4B5
MD030	6G4	PTACKO	4F2
MD040	6G5	RACKO	4B3
MD050	6G6	REQO	4R5
MD060	6G7	SCLRO	4H4
MD070	6G8	SRO	4B6
MD080	6R1	SYNO	4F5
MD090	6R2	TACKO	4H3
MD100	6R3	TACO	4R1
MD110	6R4	WRTOA	4R3
MD120	6R5		

BACK PANEL MAP			
ROW 1	ROW 2	TERM NO.	CONN.
P5	GND	41	
GND	GND	40	
		39	
		38	
MD150		37	
MD130	MD140	36	
MD110	M120	35	
MD090	MD100	34	
MD070	MD080	33	
MD050	MD060	32	
MD030	MD040	31	
MD010	MD020	30	
	MD000	29	
		28	
		27	
SCLRO	PHWO	26	
		25	
		24	
PSYNO	PATNO	23	
	PTACKO	22	
PCLO70	PDAO	21	1
PDRO	PCMDO	20	
PSRO	PADRSO	19	
PD140	PD150	18	
PD120	PD130	17	
PD100	PD110	16	
PD080	PD090	15	
PD060	PD070	14	
PD040	PD050	13	
PD020	PD030	12	
PD000	PD010	11	
WRTOA	MS000	10	
MS010	MS020	09	
MS030	MS040	08	
MS050	MS060	07	
MS070	MS080	06	
MS090	MS100	05	
MS110	MS120	04	
MS130	MS140	03	
MS150		02	
GND	GND	01	
P5	GND	00	
P5	GND	41	
GND	GND	40	
	REQO	39	
	ENO	38	
ATCO	TACO	37	
		36	
		35	
		34	
MA130	MA140	33	
MA110	MA120	32	
MA090	MA100	31	
MA070	MA080	30	
MA050	MA060	29	
		28	
		27	
SCLRO	HWO	26	
		25	
		24	
SYNO	ATNO	23	
RACKO	TACKO	22	
CLO70	DAO	21	0
DRO	CMDO	20	
SRO	ADRSO	19	
D140	D150	18	
D120	D130	17	
D100	D110	16	
D080	D090	15	
D060	D070	14	
D040	D050	13	
D020	D030	12	
DQ00	D010	11	
MA030	MA040	10	
MA020		09	
		08	
MA010		07	
MA000		06	
		05	
INHO		04	
		03	
		02	
GND	GND	01	
P5	P5	00	

TEST POINT INDEX		
DESIG	MNEM	LOC.
A	ADI	2L6
B	WTI	3G5
C	SXI	3G6
D	MSCO	3G4
E	BSYO	3G3
F	ENMDWI	4S3
G	REQI	4S5
H	DXI	3G7
I	SELI	4L3
J	ENMSI	4S4
K	ENMDRI	4S6

SUPPLEMENTARY INFORMATION

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION	
NS SELCH	35-391M02R03

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NOTES

REVISIONS	
IN SUPP INFO 35-392 M02 WAS R00	AREA M9: REV LEV OF 35-391 M02 WAS R02 — 2132 — 4-16-74 — R02
- 2114 — 3/14/74 — R01	2197 — 6/22/74 — R03
IN SUPP INFO 35-392M02 WAS R01	

NAME	TITLE	DATE
W ZILLGER	DRAFT	10-13-71
	CHK	
	ENGR	
	DIR ENG	

TITLE NS SELECTOR CHANNEL

TASK NO. 03075

DWG NO. 02-232M01R03D08

SHEET 7 OF 7

BRUNING 44-231 15043

M49-410
TEST AID
INFORMATION SPECIFICATION

1. INTRODUCTION

This Information Specification covers installation, operation, and maintenance of the M49-410 Test Aid (02-276) and the associated logic in the Processor. Refer to 02-276D08 for schematics of the M49-410 Test Aid.

2. GENERAL DESCRIPTION

The Test Aid consists of a switch display panel and a 17-283 logic card which attaches to the following boards:

35-446 CPU-HI Model 74 Processor
35-446F01 and 35-446F02 CPU-HI 7/16 Basic Processor
35-524 CPU-B Model 7/16 HSALU Processor
35-523F01 and 35-523F02 CPU-B Model 7/32 Processor

The Test Aid provides the ability to examine the address of the micro-code and to stop Processor clocks at option.

3. INSTALLATION

This section provides the information necessary to install the Test Aid on the Processor. The 02-276R01 or higher revision level Test Aid may be used on the Model 74, 7/16 Basic, 7/16 HSALU, and 7/32 Processors. The 02-276R00 Test Aid may be used on the Model 74 and the Model 7/16 Basic. The installation procedure is:

1. Remove the display from the chassis.

2. Place Test Aid logic card over pins on CPU-HI board or CPU-B board (installed in Slot 6 of the Processor back panel, refer to Figure 1) and press down until Test Aid logic card rests on spacers on the Processor board. The switch/display panel assembly may be placed on a table or mounted on the chassis as shown in Figure 2.

3. On the 7/16 HSALU Processor, a jumper must be installed between TP1 on the 35-544 CPU-B board and TP1 on the 35-522 CPU-A board.

4. On the 7/32 Processor, a jumper must be installed between TP1 on the 35-523F01 or F02 CPU-B board and TP1 on the 35-522 CPU-A board.

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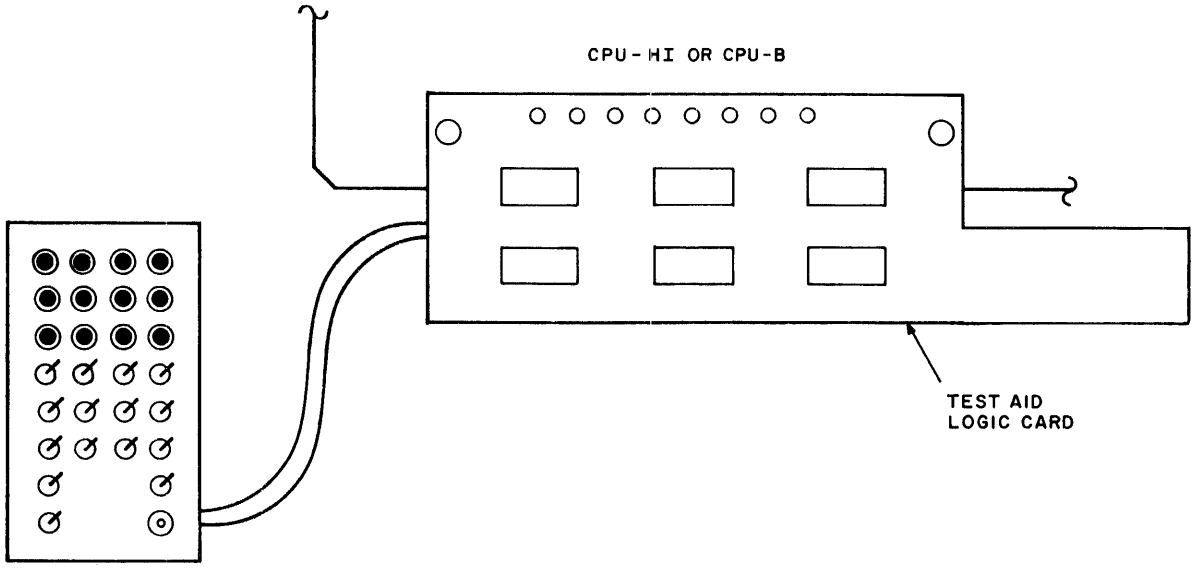

Figure 1. Test Aid Installation

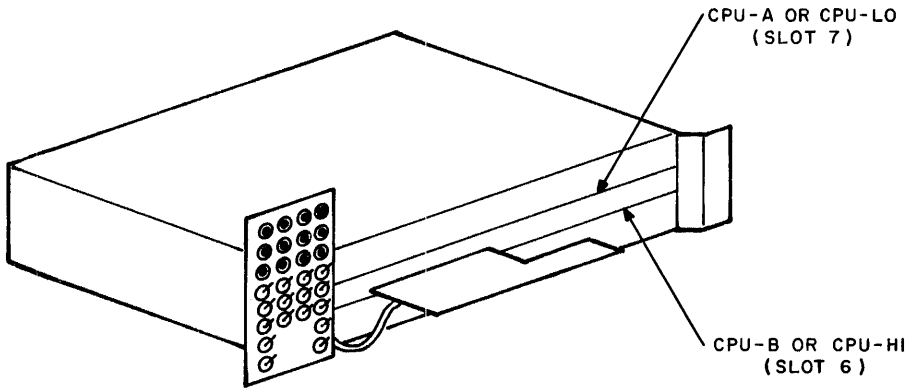

Figure 2. Switch Panel Mounting

4. POWER

Power and ground are supplied by the Processor board. There are no other power requirements.

5. OPERATION

Refer to Figure 3 during the operating description. The 12 Light-Emitting Diodes (LEDs) numbered 4:15 display the con tents of the ROM Address Register. The numbers assigned to the LEDs correspond to the ROM Address Register bits. The 12 toggle switches labelled 4:15 provide the ability to set-up a match address. The Test Aid logic stops the Process clocks when the selected "match address" is in the ROM Address Register and the Address Match switch is in the ON (up position.

6. ADDRESS MATCH SWITCH

After selecting an address on the Address switches, place the Address Match switch in the ON (up) position. When the ROM Address Register of the Processor contains the "match address", the Processor clocks are stopped on the next clock. The Address Match switch feature can also be used to interrupt and continue micro-code loops. Follow the procedure for address matching. Select an address within a micro-code loop. Once the match has been found, depressing the Clock Advance (ADV) switch once allows the micro-code to go through the loop and match on the selected address again.

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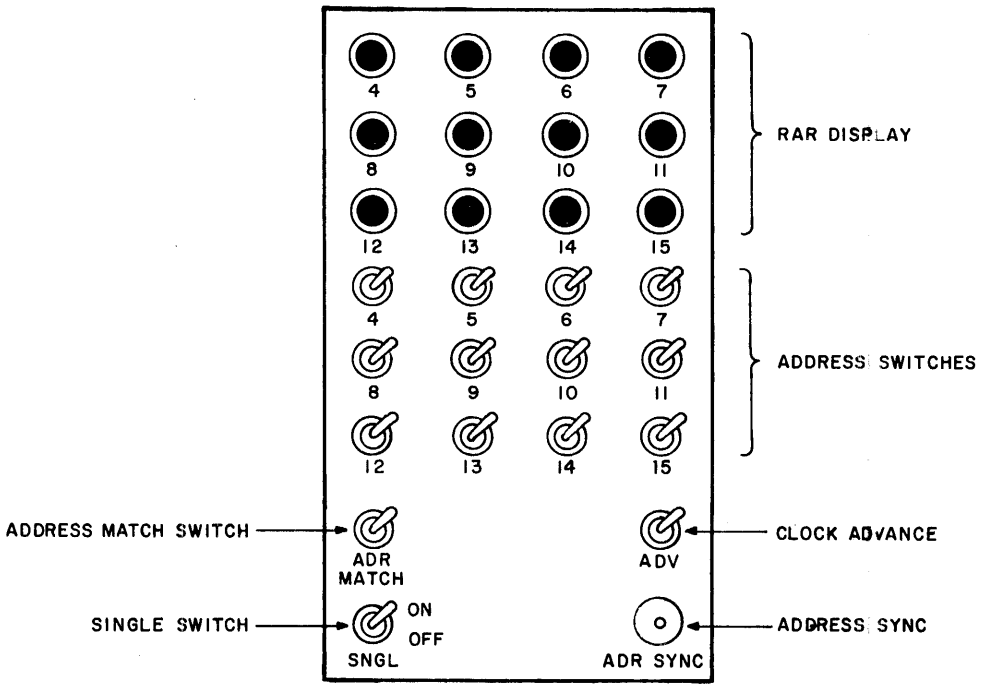

Figure 3. Switch Panel

NOTE

The LED display in most cases is one increment ahead of the match address. The micro-code instruction at the address selected has been executed or is one clock into execution when the match occurs and the Processor clocks stop.

7. CLOCK ADVANCE SWITCH

The Clock Advance switch allows the Processor to generate one clock each time it is depressed when the Address Match or Single switch is in the ON (up) position.

8. SINGLE SWITCH

When the Single switch is in the ON (up) position, the Processor clocks are stopped. With this switch ON, the micro-program may be executed one micro-instruction at a time by depressing the Clock Advance switch.

9. ADDRESS SYNC

Address Sync is a BNC connector whose output is a low going signal that becomes active when the Address switches and the contents of the ROM Address Register compare. The contents of the ROM (specified by the ROM Address Register) will not be loaded into the ROM Data Register until the next Clock which loads the ROM Data Register.

10. OPTION

Pins 'A' and 'B' are normally wired together. Pin 'A' is the output of a comparator that compares the ROM Address Register and the Address switches. When they compare, the signal on Pin A goes high (+5 VDC) causing Processor clocks to stop. Removing the wire between Pins 'A' and 'B' provides a means to bring in any high active signal on Pin 'B' to stop Processor clocks. To match on any high active signal, the Address Match switch must still be placed in the ON (up) position when a match is desired. Removing the wire between 'A' and 'B' will remove the capability to stop Processor clocks on address match. See Figure 4.

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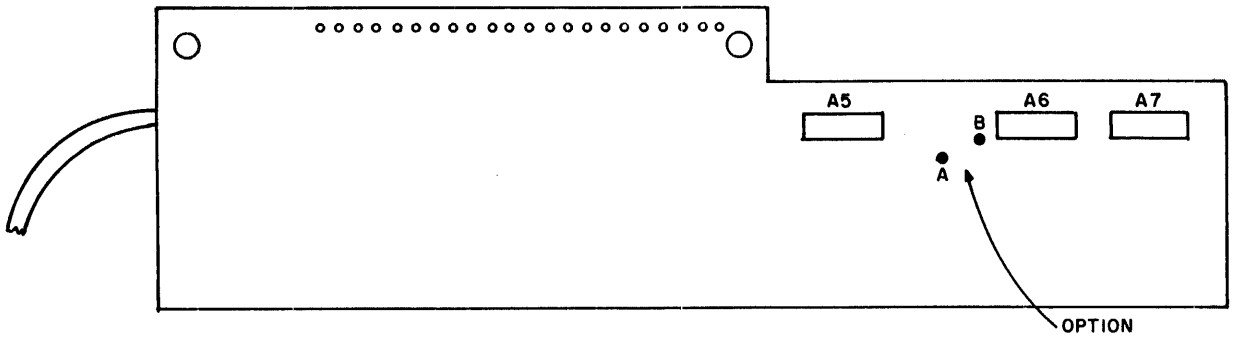
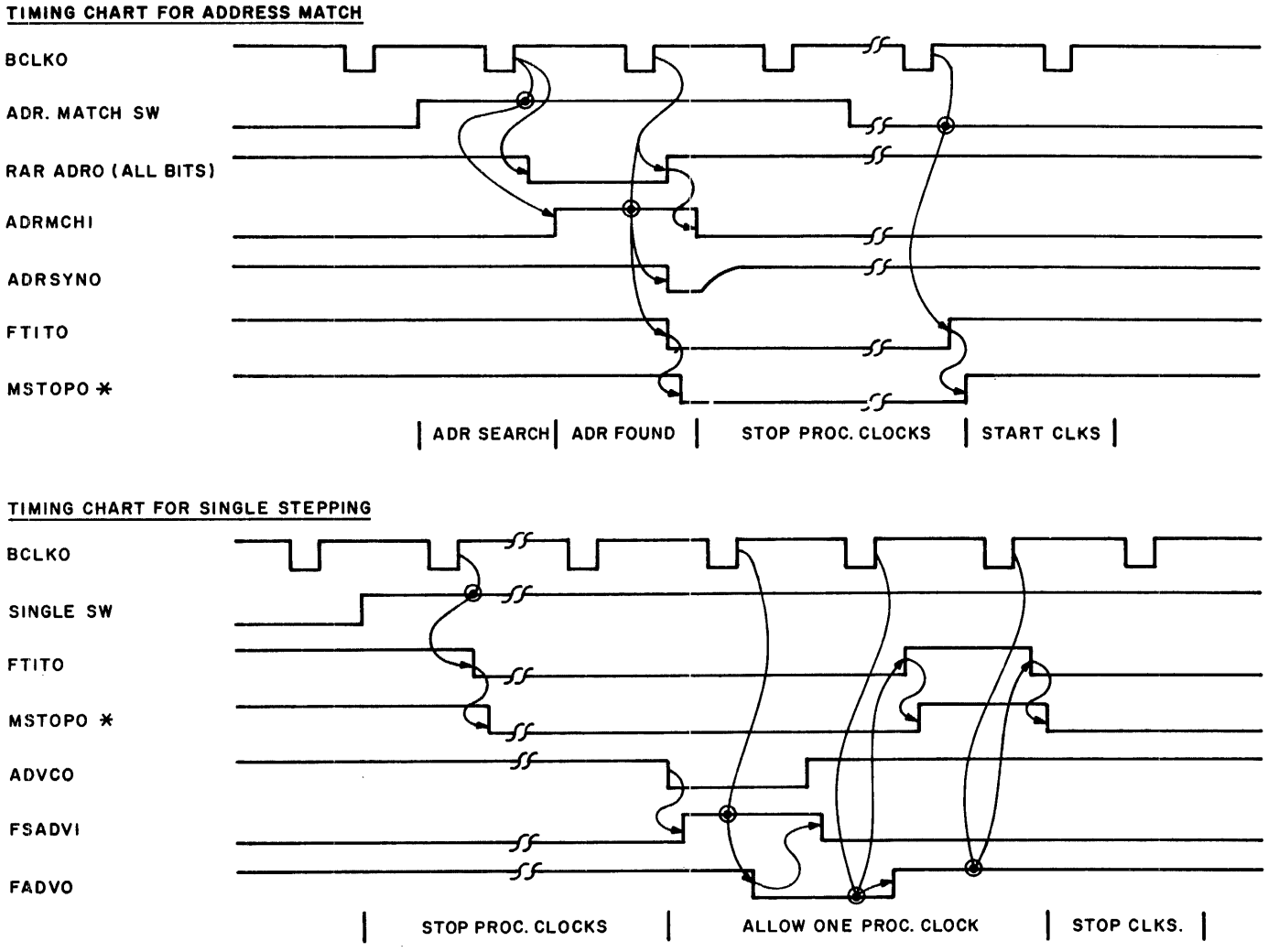


Figure 4. Option Connections

11. TEST AID MAINTENANCE

11.1 Timing

This section defines timing sequences (Figure 5) in the logic of the Test Aid and associated logic in the Processor. Refer to the Processor Functional Schematic, Clock Control sheet, for logic detail of the clock stop.



* MSTOPO IS A CLOCK STOPPING SIGNAL INTERNAL TO THE MODEL PROCESSOR. WHEN ACTIVE ALL PROCESSOR CLOCKS EXCEPT CLKI, BCLKI AND BCLKO ARE STOPPED.

Figure 5. Test Aid Timing

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11.2 Mnemonic Definitions

ADRMCH1 - This signal is active when the contents of the ROM Address Register and the Address switches are equal.

ADVC0 - Flip-flop output which goes active when the ADV switch is depressed, inactive when the ADV switch is released.

BCLK0 - Derived from the Processor. This is a clock that cannot be stopped by any clock stop in the Processor. BCLK0 width is typically 60 nanoseconds and the period is typically 250 nanoseconds.

FADV0 - When active, allows FTIT0 to be inactive for one clock period. If ADVC0 and BCLK0 are active at the same time, the FADV0 flip-flop sets.

FTIT0 - This flip-flop is reset by Single switch ON, Address Match switch ON, and a match address.

MCH04-150 - When active, indicates that a particular address switch has been selected.

RAR04-150 - ROM Address Register outputs which indicates the address of the micro-instruction to be executed on the next clock.

12. USE OF MODEL 70 EXTENDER BOARD (11-103) ON THE PROCESSOR

12.1 Hazards

All Model 70 extender boards, below revision level 11-103R02, when used to extend Processor boards, present two hazards.

1. All stiffening metal on the extender board when being plugged in becomes +5VDC. This hazard exists with either Processor board on the extender.

2. When the Test Aid is installed and the CPU-LO or CPU-A is on the extender board, a stiffening bar located on the underside of the extender board rests on top of the Test Aid logic card and forces it down possibly causing a short.

12.2 Modification

The following information describes how to modify the 11-103R01 extender board:

1. Pins 200-0, 200-1, 241-0 and 241-1 are tied into the ground bus of the extender board. These pins in the Processor are +5VDC. Both ends of the extender board tie these pins to the extender board ground but via feedthrough holes causing the ground bus to become +5VDC. Cut the copper between these feed-through holes and the extender board ground bus. Add a strap from the copper run of Pins 101-0, 101-1, 140-0 and 140-1 to the adjacent ground shield to restore the continuity of back panel ground to extender board ground.

2. Remove stiffening bar on underside of extender board. Three new clearance holes must be drilled so that the stiffening bar mounts horizontally rather than vertically. The original screws may bottom out; if so, use #4-40 x 5/8 screws. Refer to Figure 6.

   After this change is made, care should still be taken to insure that the Test Aid logic card is not shorting to the stiffening bar.

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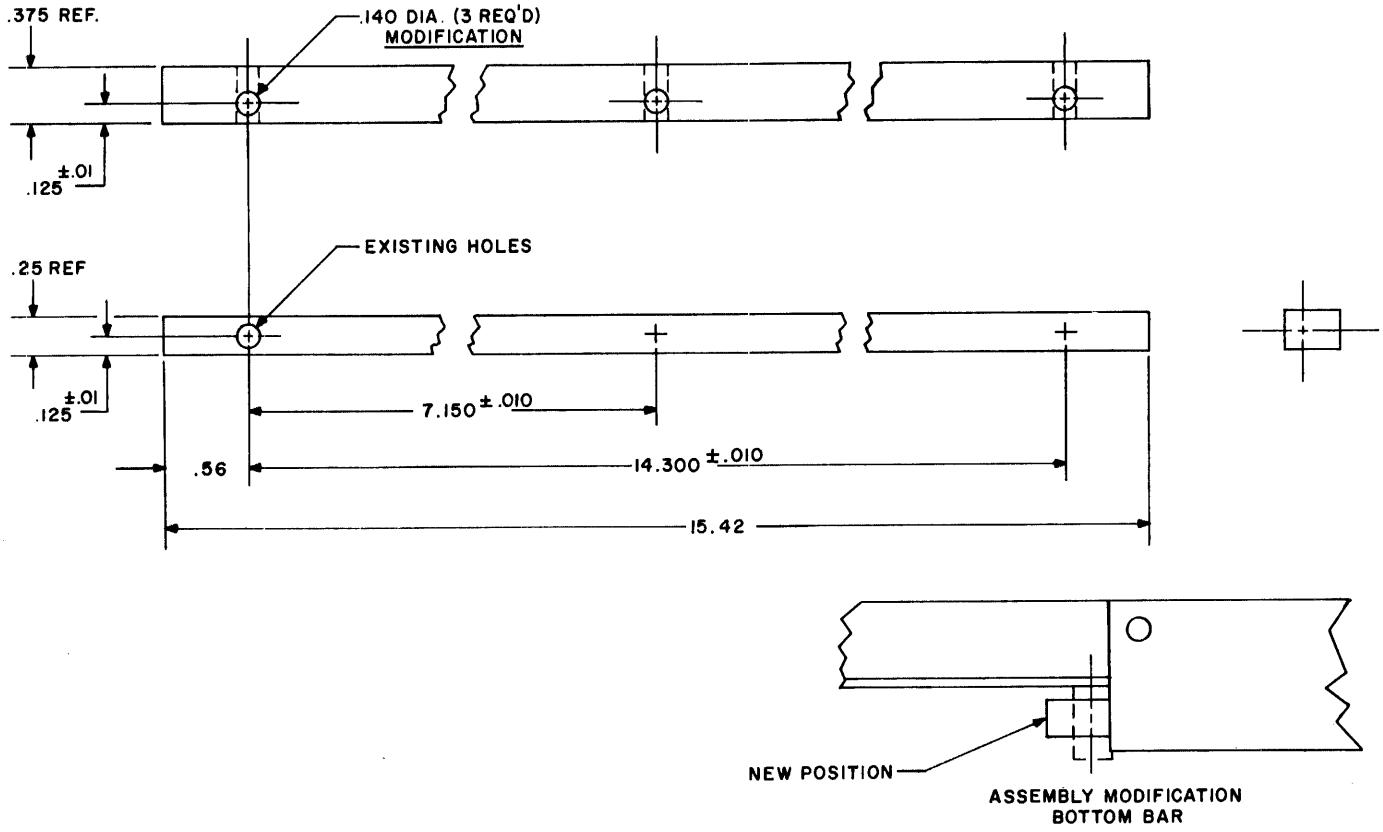

Figure 6. Stiffening Bar

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09-065R01A12
July 1974

M71-102
HEXADECIMAL DISPLAY
INFORMATION SPECIFICATION

1. INTRODUCTION

The optional Hexadecimal Display Panel provides a means to manually control the Processor, interrogate and display various Processor registers and machine status, set and display Processor memory locations, and may be programmed as an I/O device by the user.

This specification describes the 09-065F02 Hexadecimal Display Panel (Product Number M71-102). It is also applicable to the 09-065F01 Binary Display Panel (Product Number M71-101), which is identical to the Hexadecimal Display Panel except for the omission of the hexadecimal indicators. The Hexadecimal Display Panel provides the following functions:

Displays five bytes of programmable digital information.

Registers and displays five hexadecimal digits of manually entered keyboard data.

Displays the WAIT and Power (PWR) indicators for the Processor.

Provides a 26 key control keyboard for manual input to the display.

Provides two bytes of unbuffered Switch Register data to the Processor.

Provides one byte of status to the Processor.

Provides a three position OFF-ON-LOCK key type switch capable of switching three separate power supply control lines.

Provides a control signal to the Processor that the display requires micro-program support.

2. GENERAL DESCRIPTION

A complete description of the operation of the Hexadecimal Display Panel is provided in the appropriate User's Manual. This specification describes the display from a maintenance view point. Figure 1 shows the Hexadecimal Display Panel.

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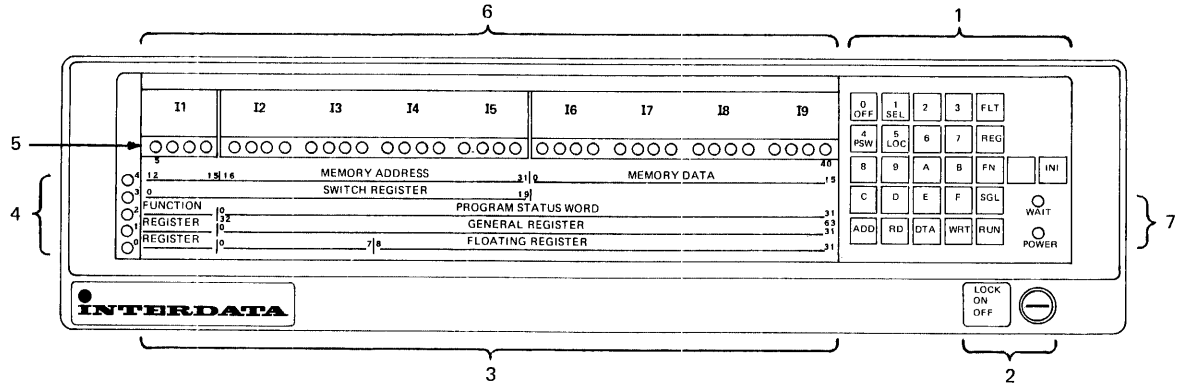

Figure 1. Hexadecimal Display Panel

Various parts of the Hexadecimal Display Panel in Figure 1 are numbered to correlate to the following descriptions.

1. Control Keyboard. The keyboard is the operators manual input to the Processor. The function of the specific keys are:

DTA — The function of the Data (DTA) key is to clear the Switch Register, connect the Switch Register to the display indicators, and enable hexadecimal data to be entered into the register. The Switch Register remains enabled and connected to the display indicators until any non-hexadecimal key other than DTA is depressed.

Hexadecimal Keys 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, and F supply data to the Switch Register when it is enabled, and the function number or register number for the Processor supported display (see Section 2.2).

ADD — The Address (ADD) key causes the Processor to read the five hexadecimal characters of the Switch Register, store them in the address portion of the Program Status Word (PSW), and display PSW 32:63 on the indicators.

RD — The Read (RD) key causes the Processor to read the memory location specified by the PSW, increment the PSW address by two, and display on the indicators the new address and the data read from memory.

WRT — Depressing the Write (WRT) key causes the data contained in the Switch Register to be written into the address specified by the PSW, the PSW to be incremented by two, and the new address and the data written to be displayed on the indicators.

FLT — Depressing the Floating-Point Register (FLT) key, followed by any hexadecimal key n, causes Floating-Point Register n to be displayed on the indicators.

REG — Depressing the Register (REG) key, followed by any hexadecimal key n, causes general register n to be displayed.

FN — Depressing the Function (FN) key, followed by any hexadecimal key n, causes the Processor to perform "Function n" as described in the appropriate User's Manual.

SGL — Depressing the Single Step (SGL) key causes the Processor to execute one user instruction and display the last register or function selected.

RUN — Depressing the Run (RUN) key causes the Processor to enter the Run mode at the address specified by the PSW.

INI — Depressing the Initialize (INI) key initializes the Processor.

NOTE

The display requires support from the micro-program for all functions other than entering or displaying Switch Register data.

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2. OFF-ON-LOCK Key Operated Locking Switch. This switch controls the power to the Processor and allows the keyboard to be completely disabled in the LOCK position.

3. Indicator Formats. These formats aid the user in interpreting the display indicators.

4. Format Selectors L0:4. Light Emitting Diode (LED) indicators L0:4 determine the format to be used to interpret display indicators L5:40.

5. Display Indicators L5:40. These LED indicators are used to display the PSW, general registers, etc., as described by the indicator formats.

6. Display Indicators I1:9. These indicators display the corresponding values displayed on L5:40 in the hexadecimal format.

7. WAIT and PWR. These indicators are illuminated when Processor is in the Wait state and Power is supplied to the Processor.

2.1 Switch Register Entries

When the operator is manipulating the Switch Register, there is no interaction between the display and the Processor. Data is entered into this register by first depressing the DTA key. This operation clears the Switch Register; connects the Switch Register to L5:24 of the display, and allows subsequent hexadecimal keyboard entries to be left shifted into the least significant digit of the resigter. The register is disconnected from the display and disabled when any non-hexadecimal key other than DTA is depressed. The register can be momentarily examined when it is disabled without affecting the Processor operation by depressing any hexadecimal key.

2.2 Processor Intervention

Depressing the following single keys causes the signals ESNC0 and ESNO0 to be complimentarily pulsed (ESNC0 is a positive going pulse):

ADD
RD
WRT
SGL
RUN

Depressing one of the following sequences of two keys causes a similar action:

FLT n (n is any hexadecimal digit)
REG n
FN n

3. FUNCTIONAL DIAGRAM ANALYSIS AND CIRCUIT DESCRIPTION

Refer to Figure 2. Hexadecimal Display Panel Block Diagram and Functional Schematic 09-065D08.

3.1 OFF-ON-LOCK Switch

This switch (2K1) controls power to the Processor by completing the circuit between CONT2 and CONT1 in the ON and LOCK positions. The switch is factory wired to provide one set of closures, but two additional sets are available for switching power supplies connected to different phased AC power. This switch also provides a hard ground to the Processor as POFF0 in the OFF position which may be used as an early power down indication. When the switch is in the ON position, LP5 (2L1) is provided to the keyboard to enable the sensing of these switch closures.

3.2 Keyboard

The keyboard (Sheet 2) has a 5 x 5 switch array which is used to enter information to the Hexadecimal Display Panel logic, plus an Initialize (INI) key used to transmit this condition to the Processor (2G1). The keyboard is a self-contained unit and connects to the 35-520 logic board by 27 stakes 00-1 through 26-1. These normally open switches are encoded by diode logic (Sheet 2) to form HEX01:31 (2B8) and FUN00:30 (2C8), plus a few additional control signals mentioned later in this description. The switches are designed to be high active when a switch is depressed by biasing all receiving gates low with a 220 ohm input resistor. A switch being depressed causes an input gate to go high by supplying LP5 through a current limiting resistor from the common input, Pin 0, if the OFF-ON-LOCK switch is in the ON position. There is no keyboard rollover protection and if more than one key is simultaneously depressed, the result is unspecified.

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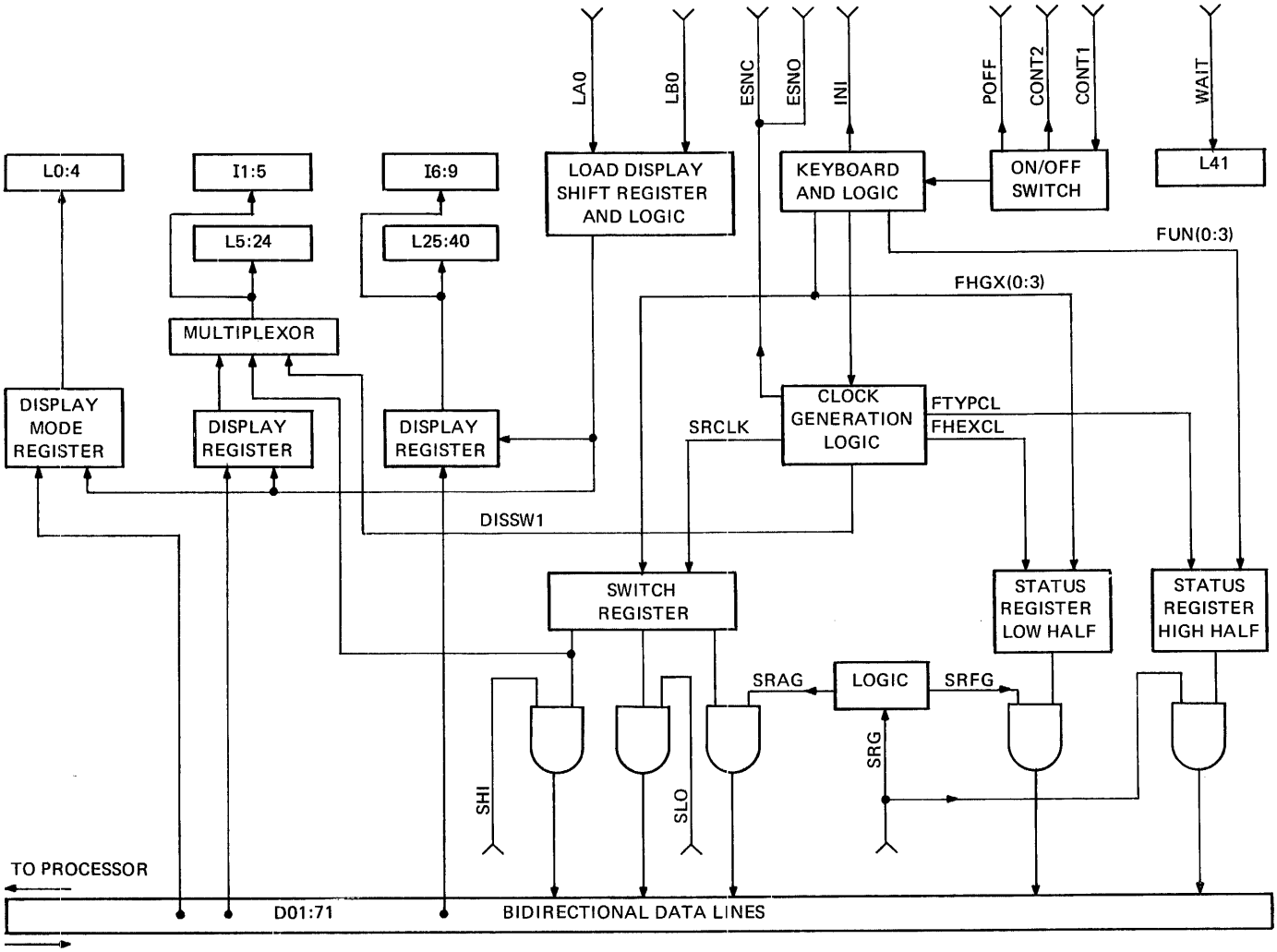

Figure 2. Hexadecimal Display Panel Block Diagram

3.3 Matrix Encoding

The diode matrix is encoded to drive signals HEX01:31 to the hexadecimal equivalent of the respective key 0:F (HEX31 is the LSB) when it is depressed. Depressing any function key other than DTA causes FUN00:30 to yield the codes specified by Table 1.

TABLE 1. FUNCTION KEY ENCODING (FUN00:30)

Key Depressed	FUN00	FUN10	FUN20	FUN30
SGL	0	1	1	1
RUN	1	1	1	1
WRT	1	1	0	1
RD	1	0	1	1
ADD	1	0	0	1
REG	0	1	1	0
FLT	0	1	0	0
FN	0	1	1	1

3.4 Clocking

Depressing any keyboard key other than DTA or INI generates one of three types of clocks used by the Hexadecimal Display Panel logic. This is accomplished by a positive transition of signal KEY1 (2F8) whenever one of these keys is depressed. The one shot triggered by this transition (2G8) is used to allow a one to two millisecond interval for switch bounce to subside before triggering the second one shot STRB1 (2K8) which is used to generate one of the three clocks. Since contact bounce is likely to retrigger these one shots when a key is released, the occurrence of signal KEY1 (any key depressed), HKEY1 (2F9 a hexadecimal key depressed), or FKEY1 (2H7 a function key depressed) being true in coincedence with the one shot is used to derive the clocks.

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3.5 Switch Register Clocks

The Switch Register is enabled for clocking by depressing the DTA key. This is accomplished by direct clearing the Switch Register Enable flip-flop (SRENB) (2L6) when DTA is depressed and ANDing the zero output of the flip-flop plus HKEY1 and STRB1 to drive the Switch Register Clock (SRCLK0) (2M7). This clock is disabled by setting SRENB with the occurrence of FKEY1 when any function key is depressed.

3.6 Status Register Clocks

Two different clocks are used to load the status register. FTYPCL0 (2M8) is generated whenever any function key other than DTA is depressed and is used to load FUN00:30 into one half of the status register. The second clock FHEXCL0 (2N8) is generated whenever a hexadecimal key is depressed if the previously depressed key was FN, REG, or FLT. In this case, the hexadecimal input would be the register number or function number desired and FHEXCL0 is used to clock HEX01:31 into the second half of the status register.

3.7 Processor Intervention

The logic of the display signals the Processor that a response is necessary to a console function by signal ESNC0 (2R7) and its compliment ESNO0 (2R7). These signals are complimentarily pulsed whenever a function key other than DTA, FN, REG, or FLT is depressed, or whenever a hexadecimal key is depressed following FN, REG, or FLT (the occurrence of FHEXCL0).

3.8 Switch Register Loading

The Switch Register (4B1, 4D1, 4G1, 4J1, and 4M1) is loaded with a hexadecimal character with the occurrence of each SRCLK0 as mentioned previously. Data is entered into the least significant character (4B1) from the switches (HEX01:31) and left shifted through the register with each clock. The register is cleared whenever the DTA key is depressed.

3.9 Status Register

The status register is loaded in two parts as described previously. One half is loaded from FUN00:30 when a Function (FN) key is depressed by the occurrence of FTYPCL0. The least significant bit of this register is re-circulated on SGL or RUN and the second LSB is re-circulated on SSL to conform to the status codes indicated in Table 2. The second half of the register is loaded from HEX01:31 with the occurrence of FHEXCL0. These registers are initialized by SCLR0 from the Processor.

TABLE 2. STATUS CODES

KEY	DL1	DL2	DL3	DL4	DL5	DL6	DL7	DL0
SGL	1	U	X	X	X	X	X	X
INITIALIZE	U	U	U	U	U	U	O	U
RUN	0	0	0	X	X	X	X	X
WRT	0	0	1	U	U	U	U	U
RD	0	1	0	U	U	U	U	U
ADR	0	1	1	U	A_1	A_2	A_3	A_4
REG n	1	0	0	1	n_1	n_2	n_3	n_4
FLT n	1	0	1	1	n_1	n_2	n_3	n_4
FN n	1	0	0	0	n_1	n_2	n_3	n_4

A = Most significant hexadecimal digit of Switch Register
U = Unspecified
X = Unchanged
n = Hexadecimal digit associated with function (see Section 6)

The display status is presented to the Processor on the data lines (DL01:71) for the duration of time that control signal SRG0 is at a logical zero level. The data presented for status is in accordance with Table 2.

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3.10 Display Register Loading

The Hexadecimal Display Panel registers and displays five bytes of data transmitted from the Processor. Two control signals are transmitted from the Processor to direct the loading of these registers. LA0 (2K5) is a low active pulse which signifies that data is available on bi-directional Data Lines D01:71 and it is to be loaded into the least significant byte of the display register. LA0 is used to initialize a four bit shift register (2M4) to 1000_2 which is used to load subsequent bytes, and generate a load pulse LA1 which is used to load the data into the LSB of the display register (2B6 and 3E6). Four subsequent LB0 pulses sent from the Processor gates data from D01:71 into successive bytes of the display register (3G6 and 3J6, 4C5 and 4E5, 4G5 and 4K5, 4N5 and 3N2). This is accomplished as each LB0 pulse is inverted and gated as LDB1, LDC1, LDD1 and LDE1 (2N4) respectively as controlled by the sequencing shift register (2M4) which is right shifted with each LB0 pulse.

3.11 Display Indicators

The two least significant bytes of the display register are gated directly to LEDs L25:40 and the hexadecimal indicators I6:9 (Sheet 3). LEDs L5:24 and hexadecimal indicators I1:5 are used to display either the most significant bytes of the display registers or the Switch Register. These sets of registers are selected through the 2:1 multiplexors (4C6, 4E6, 4H6, 4K6 and 4N6) as determined by the state of the DISSW1 (2N6). DISSW1 is high whenever the Switch Register is enabled (SRENB1) or a hexadecimal key is depressed (HKEY1).

3.12 Processor Inputs

Data is gated to the Processor in response to control signals SHI0, SLO0 or SRG0. SLO0 gates the two least significant digits of the Switch Register onto the bi-directional Data Lines D01:71 (4C3 and 4C4). SHI0 gates the next two Switch Register digits onto the bi-directional Data Lines D01:71 (4H3 and 4K3). SRG0 causes the status register bits to be gated (3D4) as per Table 2. Note that either the most significant Switch Register character is gated (4N3) if DL11 is low or the hexadecimal portion of the status register if DL11 is high (3H4).

4. PROCESSOR INTERFACING

4.1 Processor Connector

Signals from the display are terminated at a 26-080F06 type connector per the following list:

SIGNAL	PIN	SIGNAL	PIN	
D01	109	LA0	203	
D11	110	LB0	114	
D21	111	SHI0	200	
D31	112	SLO0	206	
D41	202	WAIT1	102	
D51	204	SRG0	113	
D61	205	ESNC0	103	
D71	208	ESNO0	104	
POFF0	105	INIT0	101	
CONT1	DB1-C1	SSGL1	106	
CONT2	DB1-C2	GND	100-3	
CONT3	213	GND	108	
SCLR0	107	GND	212	twisted with 114
		GND	201	twisted with 203

4.2 Timing

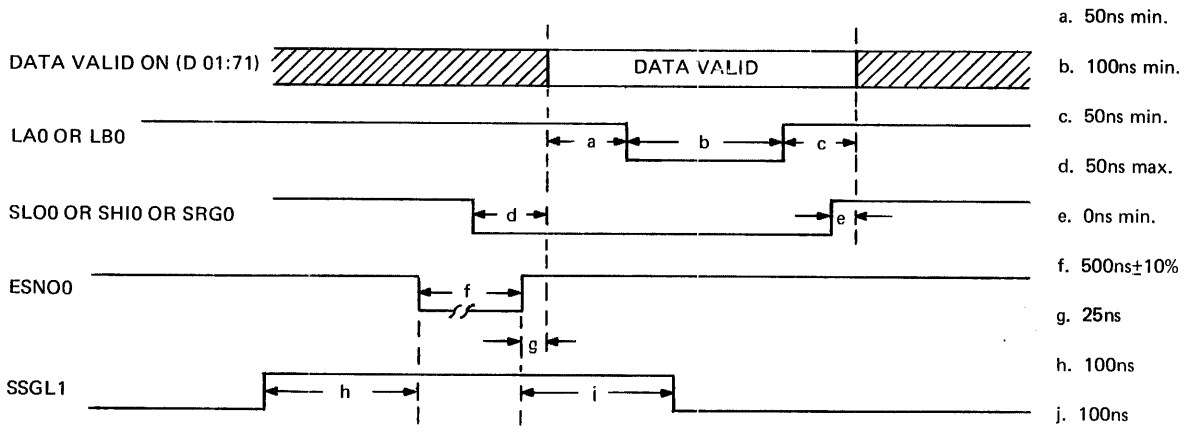

Figure 3. Hexadecimal Display Panel Timing

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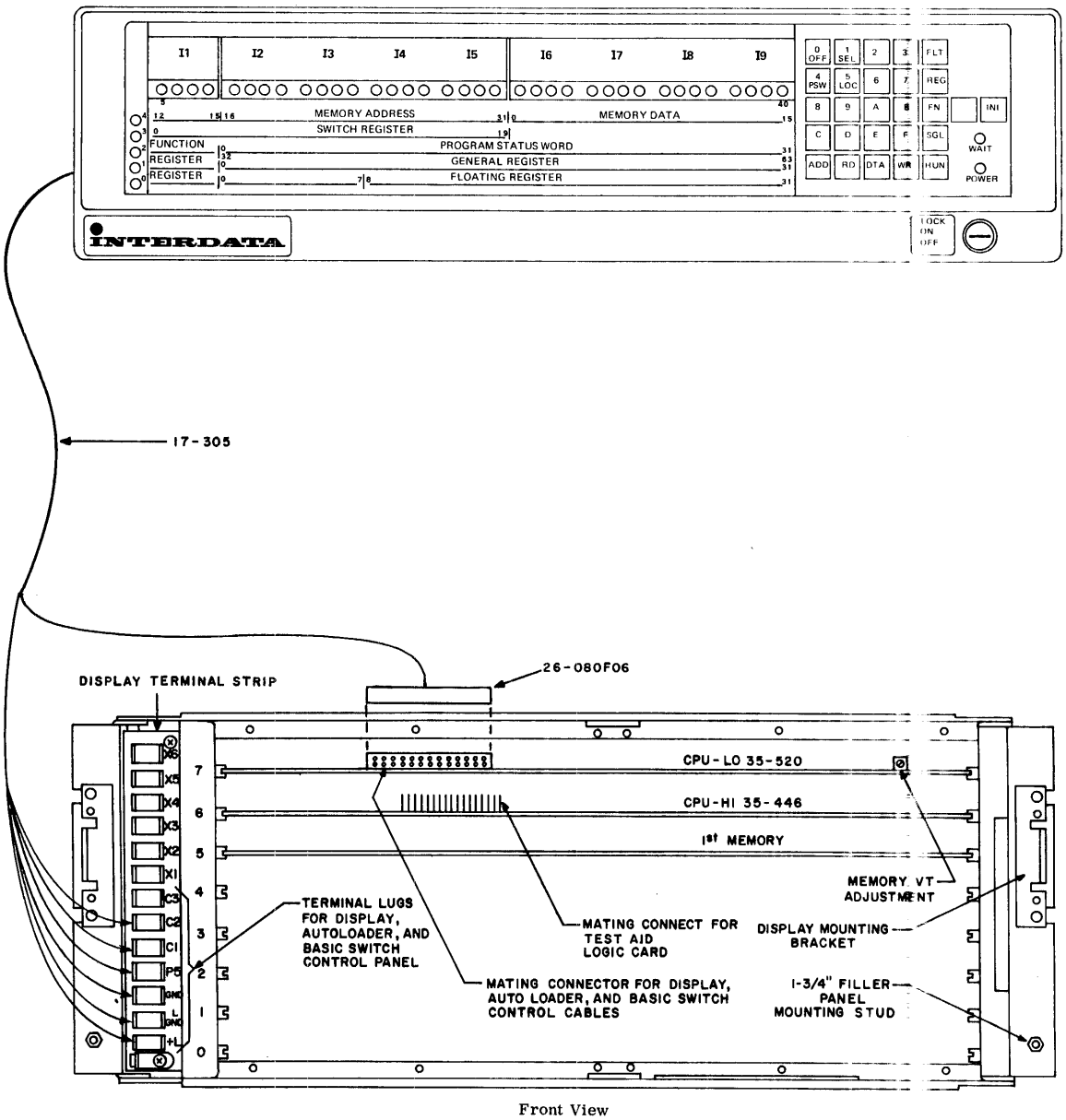
5. INSTALLATION PROCEDURE

The Hexadecimal Display Panel is connected to the Processor via a 17-305 cable. The 26-080F06 30-pin connector of the Hexadecimal Display Panel plugs into the mating connector as shown in Figure 4.

CNTL1, CNTL2, P5, GND, LGND, +L jumpers go to corresponding lugs on the Processor chassis display terminal strip as shown in Figure 4.

6. POWER

The Hexadecimal Display Panel draws its power from the P5 and +L lugs on the Processor chassis display terminal strip. See Figure 4.



Front View

Figure 4. Typical Hexadecimal Display Installation

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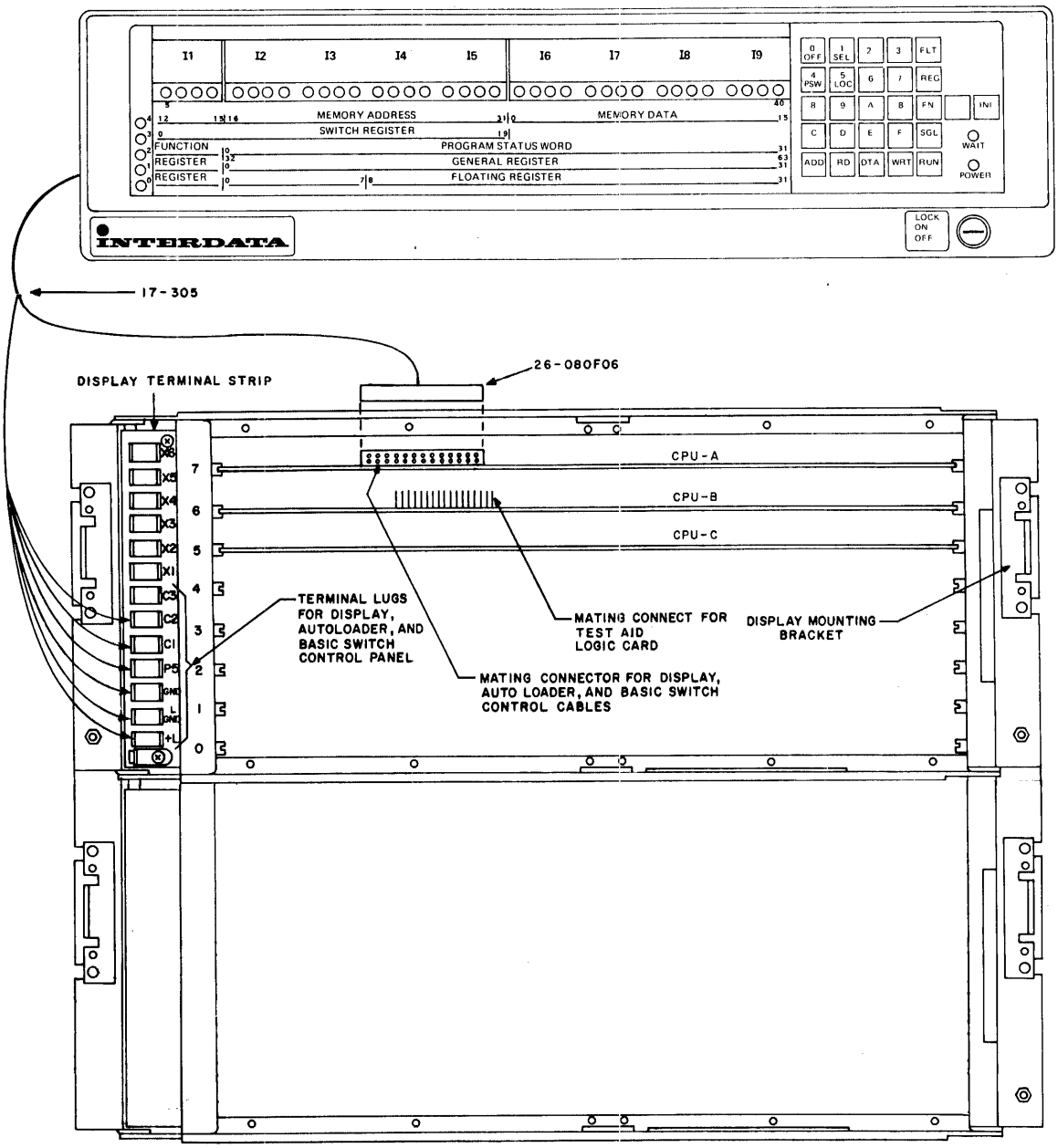

7/32 TWIN CHASSIS INSTALLATION

Figure 5. Model 7/16 HSALU or 7/32 Installation

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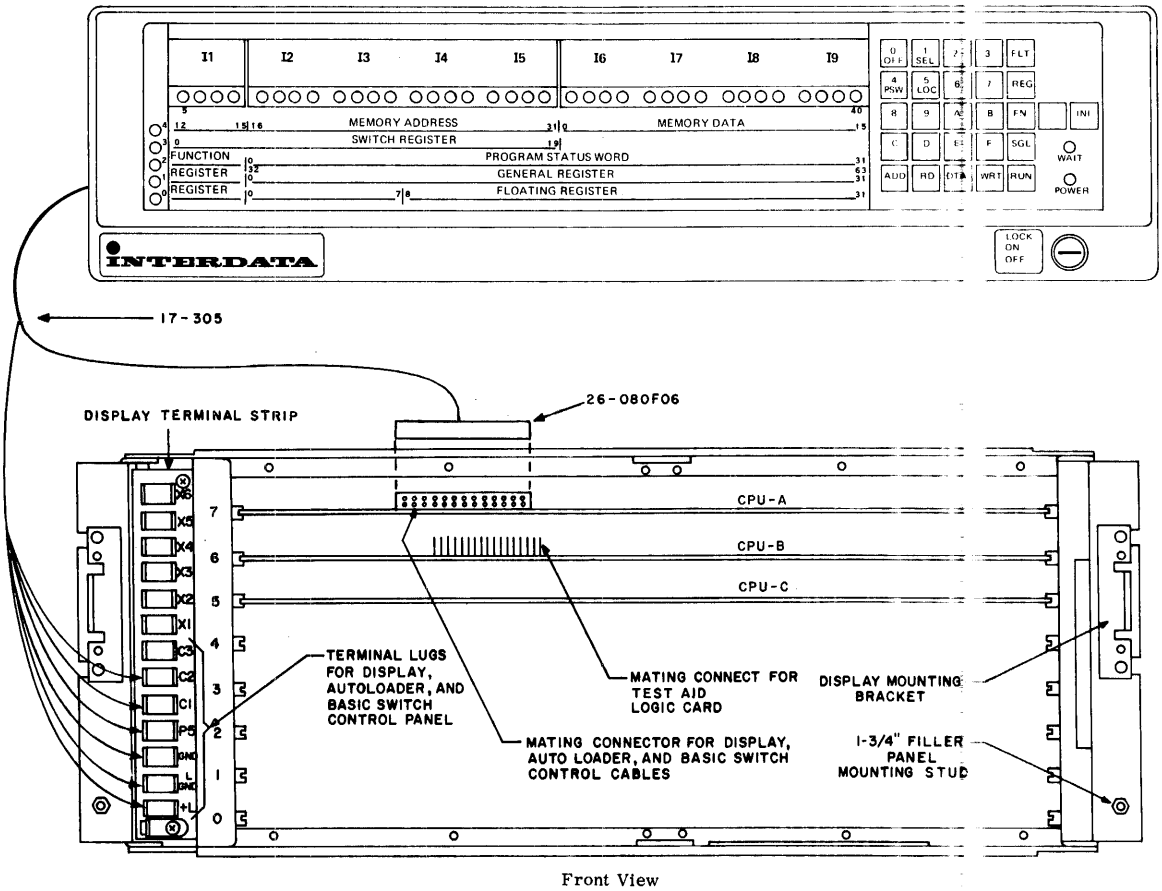

Front View

7/16 HSALU INSTALLATION

Figure 5. Model 7/16 HSALU or 7/32 Installation (Continued)

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7. MNEMONICS

The following list provides a brief description of each mnemonic found in the Hexadecimal Display Panel. The source of each signal on Functional Schematic 09-065D08 is also provided.

MNEMONIC	MEANING	SCHEMATIC LOCATION
CONT1	12 VAC to turn on power supply	2L1
CONT2	12 VAC to turn off power supply	2M1
DISSW1	Controls Display Multiplexors for L5:24	2R6
ESNC0	Execute switch normally open	2R7
ESNO0	Execute switch normally closed	2R7
FTYPCL0	Function type status register clock	2N7
FHEXCL0	Hexadecimal type status register clock	2N8
FUN00:30	Encoded functional keys	Sheet 2
HEX01:31	Encoded hexadecimal keys	Sheet 2
INIT0	Initialize Processor	2H2
LA0	Low active signal from Processor which initializes the loading sequence and loads the least significant byte of the Hexadecimal Display Panel	2K5
LB0	Low active signal from Processor used to control loading of display registers by generating LDB1, LDC1, LDD1, LDE1	2L5
LDB1	Load display registers	2R3
LDC1		2R4
LDD1		2R4
LDE1	Loads display mode register and most significant hexadecimal digit of the display	2R4
POFF0	Early power OFF failure	2K1
SCLR0	System Clear, initialize status registers	3J1
SDA0	DTA key depressed	2J2
SHI0	Switch Register high half gate command	2M2
SLO0	Switch Register low half gate command	2L3
SOR0	SGL or RUN keys depressed	2K2
SRAG1	Switch Register most significant hexadecimal digit gate command	2R2
SRCLK0	Switch Register clock	2M7
SRFG1	Status Register Function high half gate command	2R2
SRG1	Status Register low half gate command	2M2
SSL1	SGL key depressed	2J6
WAIT1	Wait light control	2M6

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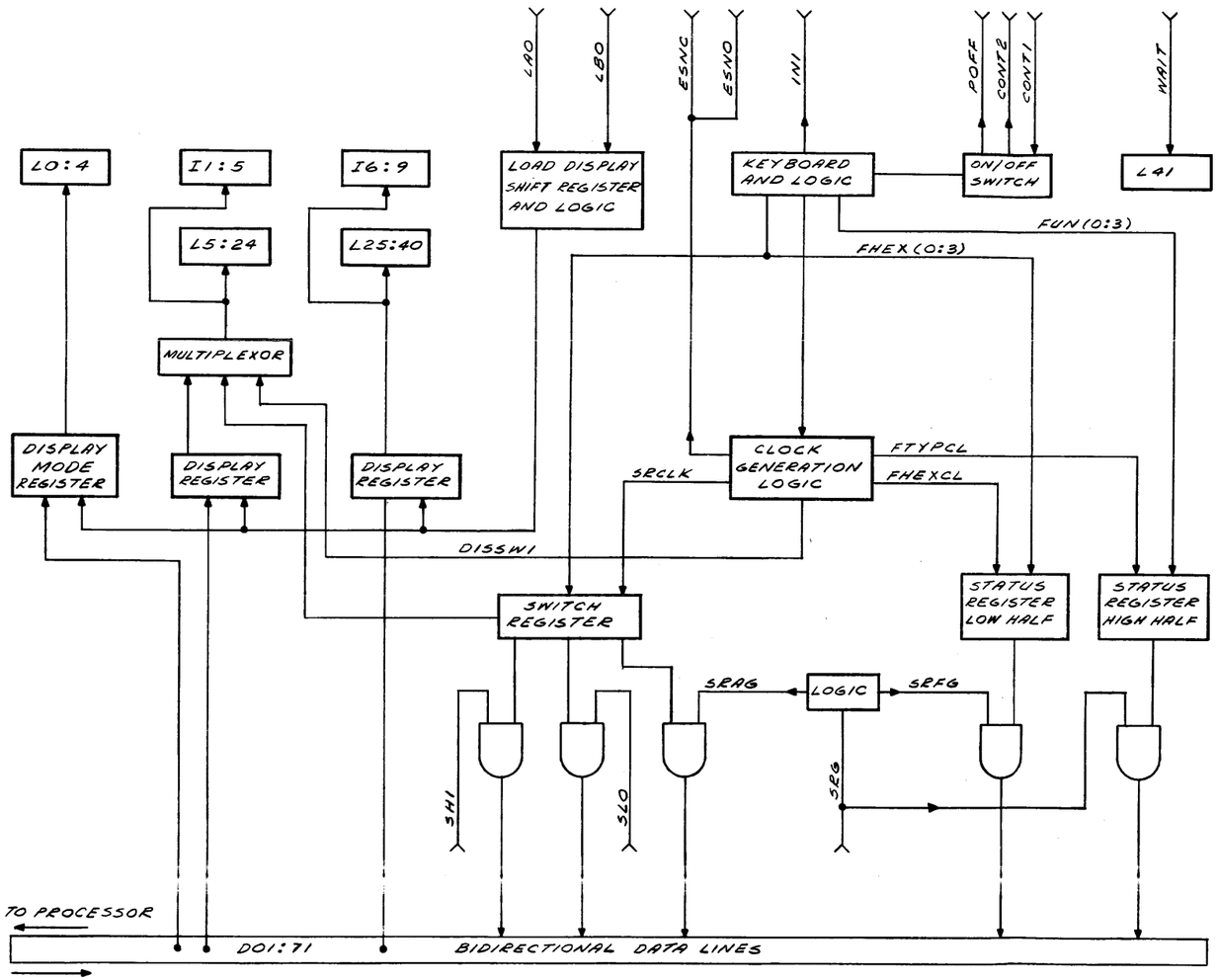
REVISIONS			
RELEASED FOR PRODUCTION MFG. ENGR. [illegible] DATE 2/1/74			
REVISED SHTS 2 & 3			
N. MATTA	2323	-	1-31-75 R01
REVISED SHTS 2 & 3			
WS	F	2635	- 12-10-75 R02



BLOCK DIAGRAM

CONN-3		
TERM	ROW 1	ROW 2
00	GND	SHIO
01	INITO	GND
02	WAITI	D41
03	ESNCO	LAO
04	ESNOO	D51
05	POFFO	D61
06	SSGLI	SLOO
07	SCLBO	
08	GND	D71
09	D01	
10	D11	
11	D21	
12	D31	GND
13	SRGO	CONT3
14	LBO	

REVISION LEVEL OF THIS SHEET IS CONSIDERED THE REVISION LEVEL OF THE DOCUMENT

SHEET INDEX	REV	2	2	0
	SHT	2	3	4

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NOTES

NAME	TITLE	DATE
N. MATTER	DRAFT	1-28-74
N. MATTER	CHK	1-28-74
S. MESSINA	ENGR	1-31-74
L. JOHMANN	TEST	1-31-74
	DIR ENG	

TITLE: FUNCTIONAL SCHEMATIC HEXADECIMAL DISPLAY

TASK NO. 03081 SHEET OF 1-4

DWG NO. 09-065P02 D08

BRUNING 44-231 16042

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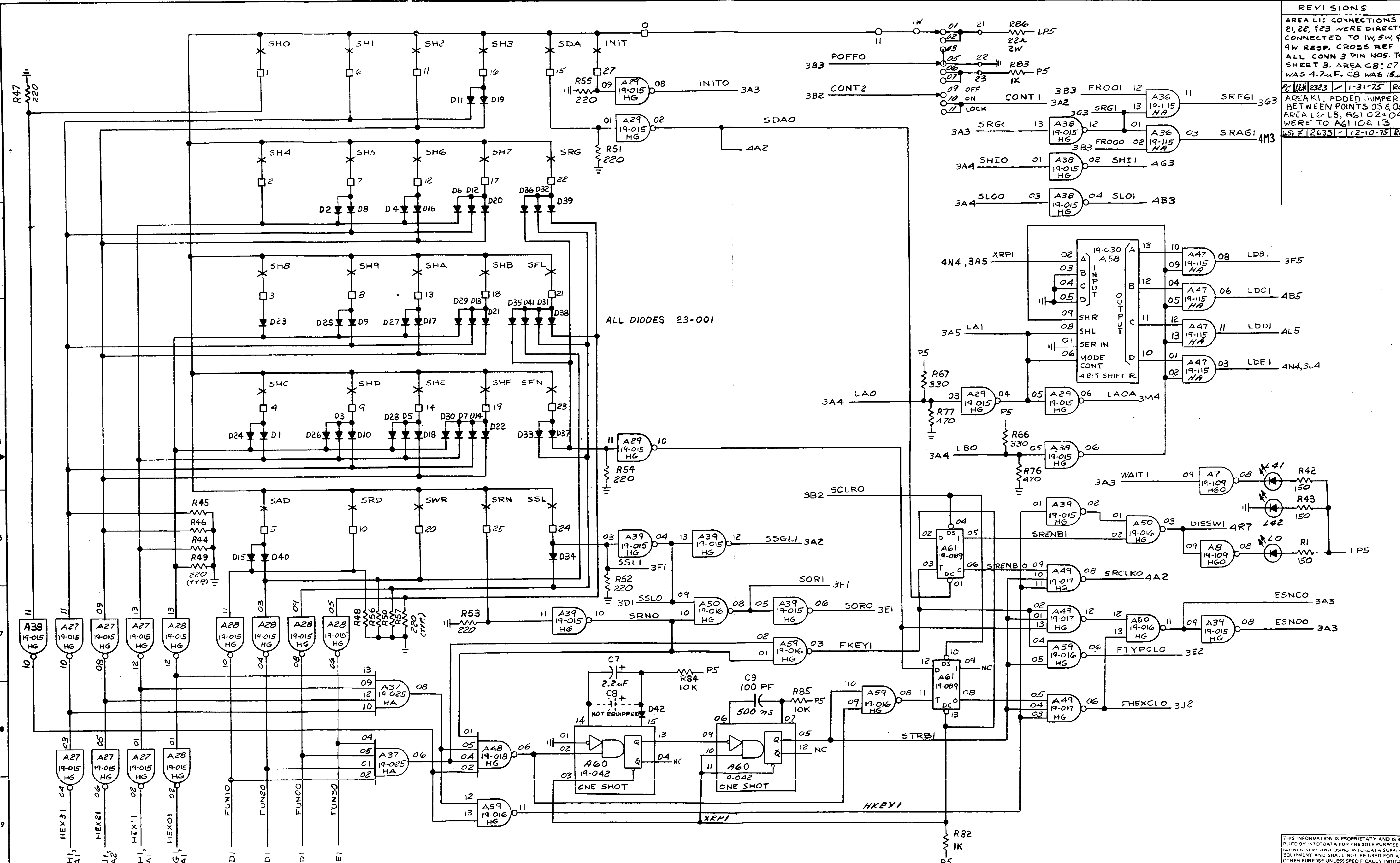

REVISIONS

AREA L1: CONNECTIONS 21, 22, & 23 WERE DIRECTLY CONNECTED TO 1W, 5W, & 9W RESP. CROSS REF ALL CONN 3 PIN NOS. TO SHEET 3. AREA G8: C7 WAS 4.7uF. C8 WAS 15uF

	ECN 2323	1-31-75	R01

AREA K1: ADDED JUMPER BETWEEN POINTS 03 & 05. AREA L6-L8, A61 02+04 WERE TO A61 10 & 13

	2635	12-10-75	R02

NOTES

1. L0 THRU L42 ARE 33-027

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	ENGR	
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TITLE FUNCTIONAL SCHEMATIC HEXADECIMAL DISPLAY

TASK NO. 03081

DWG NO. 09-065 R02 D08

SHEET 2 OF 4

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REVISIONS			
AREA A1-A4, B1-B4: ADDED CROSS REF. FROM SHT. 2.			
PE	2323	—	1-31-75 R01
AREA B2, ADDED SCLRO REF. FROM SHT. 2			
WS	2635	—	12-11-75 R02

DBI-C3 > CONT3
213-3 > TP
214-3 > TP
DBI-C2 > 23 CONT2 2J1
DBI-C1 > CONT1 2L2
106-3 > 14 SSGLI 2J6
107-3 > 9 SCLRO J1, 2J6
105-3 > 22 POFFO 2J1
101-3 > 12 INITO 2H1
103-3 > 15 ESNCO 2S7
104-3 > 16 ESNOO 2S7
113-3 > 17 SRGO 2L2
102-3 > 10 WAITI 2M5
206-3 > 18 SLOO 2L3
200-3 > 20 SHIO 2L3
114-3 > 19 LBO 2L5
203-3 > 13 LAO 2K5
208-3 > D71
205-3 > D61
204-3 > D51
202-3 > D41
112-3 > D31
111-3 > D21
110-3 > D11
109-3 > D01
2L3 XRPI
2L4 LAI

FUNOO 2D9
FUN10 2C9
SSLO 2G7
FUN20 2C9
SORO 2K7
FUN30 2D9
FTYPCLO 2N7
SCLRO J1
SORI 2J7
SSLI 2G7

A46 19-071
A57 19-043 HGO
R81 1K P5
R80 1K P5

2M2 FRO01
2M2 FRO00
2M2 SRGI
A35 19-036 HPO

HEX01 2B9
HEX11 2B9
HEX21 2A9
HEX31 2A9
FHEXCLO 2N8
SCLRO B2
R78 1K P5
E1
A56 19-071
2R2 SRFGI
A45 19-036 HPO

A1 19-071
NC
A8 19-109 HGO
L1 L2 L3 L4
R2 R3 R4 R7 150
LP5
LAOA 2N5
LDE1 2R4

P5
R64 R63 R65 R62 R61 R60 R59 R58 330 (TYP.)
R68 R69 R70 R71 R72 R75 R73 R74 470 (TYP.)
D71 4A4
D61 4A4
D51 4A4
D41 4A4
D31 4A4
D21 4A4
D11 4A4
D01 4A4

2R4 LDBI
R79 1K P5

A26 19-030 4 BIT SHIFT REG.
A25 19-030 4 BIT SHIFT REG.
A24 19-030 4 BIT SHIFT REG.
A23 19-030 4 BIT SHIFT REG
SHR SHL SER IN MODE CONT

A8 19-109 HGO
L40 L39 L38 L37
L36 L35 L34 L33
L32 L31 L30 L29
L28 L27 L26 L25
R38 R39 R41 R40 150
R34 R35 R37 R36 150
R30 R31 R33 R32 150
R26 R27 R29 R28 150
LP5 4A8

A17 33-029 HEX DISPLAY
A16 33-029 HEX DISPLAY
A15 33-029 HEX DISPLAY
A14 33-029 HEX DISPLAY

LP5 — L GND
33MF, 10V
C1 & C2

P5 — GND
33MF, 10V
C3 TO C6

P5 — L GND
0.1MF, 30V
C10 TO C14

P5 — GND
0.1MF, 30V
C15 TO C39

DECOUPLING CAPACITORS

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	DIR ENG	

TITLE FUNTIONAL SCHEMATIC
HEXADECIMAL DISPLAY
TASK NO. 03081
DWG NO. 09-065R02D08
SHEET OF 3-4

BRUNING 44-231 16042

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REVISIONS

2B9 HEX01 — 2B9 HEX11 — 2A9 HEX21 — 2A9 HEX31 — 2M7 SRCLKO — 2H2 SDAO

SW161 SW171 SW181 SW191 — A55 19-071 — SW121 SW131 SW141 SW151 — A54 19-071 — SW081 SW091 SW101 SW111 — A53 19-071 — SW041 SW051 SW061 SW071 — A52 19-071 — SW001 SW011 SW021 SW031 — A51 19-071

2N3 SL01 — 2N2 SHI1 — 2R2 SRAS1

A44 19-036 HPO — A43 19-036 HPO — A42 19-036 HPO — A41 19-036 HPO — A40 19-036 HGO

3R4 D71 — 3R4 D61 — 3R5 D51 — 3R5 D41 — 3R5 D31 — 3R5 D21 — 3R5 D11 — 3R5 D01

2R4 LDC1 — LDD1 2R4 — LDE1 2R3 — XRP1 2L3

A34 19-030 4 BIT SHIFT REG — A33 19-030 4 BIT SHIFT REG — A32 19-030 4 BIT SHIFT REG — A31 19-030 4 BIT SHIFT REG — A30 19-030 4 BIT SHIFT REG

A22 19-053 2:1 MUX. — A21 19-053 2:1 MUX. — A20 19-053 2:1 MUX — A19 19-053 2:1 MUX — A18 19-053 2:1 MUX — DISSWI 2N6

A5 A4 A3 A2 A8 19-109 HGO — L24 L23 L22 L21 — L20 L19 L18 L17 — L16 L15 L14 L13 — L12 L11 L10 L9 — L8 L7 L6 L5 — R23 R24 R25 R22 — R19 R18 R20 R21 — R16 R15 R14 R17 — R12 R11 R10 R13 — R8 R9 R6 R5 — 150

3L8 LP5

A13 33-029 HEX DISPLAY — A12 33-029 HEX DISPLAY — A11 33-029 HEX DISPLAY — A10 33-029 HEX DISPLAY — A9 33-029 HEX DISPLAY

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TITLE FUNCTIONAL SCHEMATIC HEXADECIMAL DISPLAY

TASK NO 03081 — DWG NO 09-065 D08 — SHEET OF 4-4

BRUNING 44-231 16042

```
INTERDATA MODEL 6/16 MICRO-PROGRAM 05-061R01A13          PAGE   1
                OPT   SCRT,CROSS,SQCHK,GO
                *                                                          61600020
                * COPYRIGHT INTERDATA INC.   MARCH, 1976                   61600030
                *                                                          61600040
                * MARCH 12, 1976                                           61600050
                * DHEMA MAHAJAN                                            61600060
                *                                                          61600070
                *                                                          61600080
                *                                                          61600090
                * PAGE 0 MICROPROGRAM IS COMPRISED OF THE FOLLOWING ROM CHIPS 61600100
                *              19-186R00F02  :  WORD BITS  0:7              61600120
                *              19-186R00F03  :  WORD BITS  8:15             61600130
                *              19-186R01F04  :  WORD BITS 16:23             61600140
                *                                                          61600150
                * PAGE 1 (MPY/DIV) MICROPROGRAM IS COMPRISED OF THE FOLLOWING ROM CHIPS 61600160
                *                                                          61600170
                *              19-186R00F05  :  WORD BITS  0:7              61600180
                *              19-186R00F06  :  WORD BITS  8:15             61600190
                *              19-186R00F07  :  WORD BITS 16:23             61600200
                *                                                          61600210
                *                                                          61600220
                *                                                          61600230
                *  LOCATION EQUATES                                        61600240
                *                                                          61600250
                *                                                          61600260
          0022  PNTR   EQU   '22'                                          61600270
          0024  APSW   EQU   '24'                                          61600280
          0026  ALOC   EQU   '26'                                          61600290
          0030  ILGPSW EQU   '30'                                          61600300
          0038  OMMPSW EQU   '38'                                          61600310
          0040  OIPSW  EQU   '40'                                          61600320
                *                                                          61600330
                *                                                          61600340
                * INSTRUCTION READ IS IN PROGRESS                          61600350
                * LOC IS INCREMENTED BY 2 & JAMMED IN MAR                  61600360
                *                                                          61600370
                *                                                          61600380
000   848170    START  BT    ATN+CATN+SNGL+MALF,HELP IF ANY INT., GO TO HELP 61600390
001   E04400    START1 L     MR0&Q,YS,D1          VECTOR THRU DROM1.      61600400
                *                                 INITIATE MEMORY READ.    61600410
                *                                 IF RR OR SF, SUPRESS MEMORY READ 61600420
                *                                                          61600430
                *                                                          61600440
                * COMMON RS                                                61600450
                *                                                          61600460
                *                                                          61600470
002   A4DC0A    RS     BF    AMOD,RSNX                                     61600480
003   246440           A     MR0,Q,MDR,D2         (MR0) = A+(X2)  VECTOR THRU DROM2 61600490
                *                                                          61600500
                *                                                          61600510
                * RX TYPE I/O INSTRUCTIONS                                 61600520
                *                                                          61600530
                *                                                          61600540
                * COME HERE THRU DROM1                                     61600550
                *                                                          61600560
004   0C7071    AI     ACK   YD                   GET INTERRUPTING DEV ADR IN R1 61600570
                *                                                          61600580
                * COME HERE THRU DROM1 FOR RD, WD, RH, WH, SS & OC         61600590
```

```
                *
005  043E01     IORX    ADR    YD                    ADDRESS THE DEVICE
                *
                *
                *
                * COMMON RX
                *
                *
006  A4DC08     RX      BF     AMOD,RXNX
007  046840             A      MDR,Q,MDR
008  047A40     RXNX    L      MAR,MDR
009  407102             LI     Q,2,MR
00A  247440     RSNX    L      MR0,MDR,D2            (MR0) = SECOND OPERAND
                *
                * COME HERE THRU DROM1 FOR AL
                *
00B  A43DDA     AL      B      ALI
                *
                * COME HERE THRU DROM1 FOR LM & STM
                *
                *
                *
00C  A4DC0E     LMSTM   BF     AMOD,LMNX
00D  046840             A      MDR,Q,MDR
00E  047A40     LMNX    L      MAR,MDR               (MAR) = ADDRESS OF 2ND OPERATOR
                *
00F  00710F             LI     Q,15
010  04E460             S      MR0,Q,YDI             (MR0) = COMPLEMENT OF YD FIELD
011  207102             LI     Q,2,D2
                *
                * COME HERE THRU DROM1 FOR BXH, BXLE
                *
012  A4DC14     BX      BF     AMOD,BXNX
013  046840             A      MDR,Q,MDR             (MDR) = A + (X2)
014  043402     BXNX    L      MR0,YDPI              (MR0) = (R1) = START INDEX
015  045423             A      MR0,YDM1,MR0          (MR0) = INCREMENTED OR
                                                             DECREMENTED INDEX
                *
016  0C7022             L      YDP1,MR0
017  2C3002             L      YDP1,YD,D2            BUMP YD FIELD
                *
                *
                * INPUT / OUTPUT INSTRUCTIONS
                *
                *
                * COME HERE THRU DROM2
                *
018  0478F4     RD      RD     MDR,CS                READ A BYTE
019  602000     RD2     L      Q,Q,MW                WRITE A BYTE/HW INTO MEMORY
01A  C02000             L      Q,Q,IR
                *
                * COME HERE THRU DROM2
                *
01B  047EC4     WD      WD     MDR,CS                WRITE A BYTE
01C  C02000             L      Q,Q,IR
                *
                * COME HERE THRU DROM2
                *
```

```
01D  007100    RH      LI     Q,0                                          61601170
01E  84EC20            BT     HW,RHH          FOR HW DEVICE, GO TO RHH     61601180
01F  0070F4            RD     Q,CS            (Q 0:7)     = MS BYTE        61601190
020  047874    RHH     RD     MDR             (MDR 8:15) = LS BYTE         61601200
021  046840            A      MDR,Q,MDR                                    61601210
022  A43C19            B      RD2                                          61601220
                  *                                                       61601230
                  * COME HERE THRU DROM2                                  61601240
                  *                                                       61601250
023  84EC25    RHR     BT     HW,RDR          FOR HW DEVICE, GO TO RDR     61601260
024  0070F4            RD     Q,CS            (Q 0:7) = MS BYTE            61601270
                  *                                                       61601280
                  * COME HERE THRU DROM2 FOR RDR                           61601290
                  *                                                       61601300
025  047474    RDR     RD     MR0                                          61601310
026  CC6220            A      YS,Q,MR0,IR                                  61601320
                  *                                                       61601330
                  * COME HERE THRU DROM2 FOR WH & WHR                      61601340
                  *                                                       61601350
027  84EC29    WHR     BT     HW,WDR          FOR HW DEVICE, GO TO WDR     61601360
028  047EA4            WD     MR0,CS                                       61601370
                  *                                                       61601380
                  * COME HERE THRU DROM2 FOR WDR                           61601390
                  *                                                       61601400
029  047E24    WDR     WD     MR0             WRITE A BYTE/HW TO DEVICE    61601410
02A  C02000            L      Q,Q,IR                                       61601420
                  *                                                       61601430
                  * COME HERE THRU DROM2 FOR SS & AI                       61601440
                  *                                                       61601450
02B  0478F2    SS      SS     MDR,CS          SENSE STATUS INTO MDR        61601460
02C  047CC0            L      FLR,MDR,CS                                   61601470
02D  A43C19            B      RD2                                          61601480
                  *                                                       61601490
                  * COME HERE THRU DROM2 FOR SSR & AIR                     61601500
                  *                                                       61601510
02E  0C7272    SSR     SS     YS              SENSE STATUS INTO R2         61601520
02F  C44C00            L      FLR,YS,IR                                    61601530
                  *                                                       61601540
                  * COME HERE THRU DROM2                                   61601550
                  *                                                       61601560
030  047EC2    OC      OC     MDR,CS          OUTPUT COMMAND FROM MDR      61601570
031  C02000            L      Q,Q,IR                                       61601580
                  *                                                       61601590
                  * COME HERE THRU DROM2 FOR OCR                           61601600
                  *                                                       61601610
032  047E22    OCR     OC     MR0             (MR0 7:15) = COMMAND         61601620
033  C02000            L      Q,Q,IR                                       61601630
                  *                                                       61601640
                  *                                                       61601650
                  * COME HERE THRU DROM1 FOR RB & WB                       61601660
                  *                                                       61601670
                  *                                                       61601680
034  043E01    RBWB    ADR    YD                                           61601690
035  047A40            L      MAR,MDR         (MAR) = A                    61601700
036  A4DC38            BF     AMOD,RBWBNX                                  61601710
037  046A40            A      MAR,Q,MDR       (MAR) = A + (X2)             61601720
038  447A55    RBWBNX  INC    MAR,MAR,MR                                   61601730
```

```
039  047A55          INC   MAR,MAR                                          61601740
03A  007040          L     Q,MDR          (Q) = BLOCK START ADDRESS         61601750
03B  442A00          L     MAR,Q,MR       (MAR) = BLOCK START ADDRESS       61601760
                     *                    (MDR) = BLOCK END ADDRESS         61601770
03C  A43CD9          B     BLKI01                                           61601780
                     *                                                      61601790
                     *                                                      61601800
                     *                                                      61601810
                     * SHIFT / ROTATE INSTRUCTIONS                          61601820
                     *                                                      61601830
                     *                                                      61601840
                     * COME HERE FROM D1 FOR SRHL, SLHL                     61601850
                     *                                                      61601860
03D  047B0F  SLHL    LI    MAR,15                                           61601870
03E  047500  SLHL2   LI    MR0,0          (MR0) = 0 FOR LOGICAL SHIFTS/ROTATES 61601880
03F  047D00  SLHL3   LI    FLR,0                                            61601890
                     *                                                      61601900
040  A4DC42          BF    AMOD,SLHLNX                                      61601910
041  046840          A     MDR,Q,MDR                                        61601920
042  007052  SLHLNX  L     Q,MAR,YDP1     (Q) = SHIFT / ROTATE MASK          61601930
                     *                    BUMP YD FIELD                     61601940
043  06684C          N     MDR,Q,MDR,F    (MDR) = SHIFT / ROTATE COUNT = 0:31 61601950
                     *                    (YD)  = (R1)                      61601960
044  003003          L     Q,YDM1         (Q) = (R1+1)                      61601970
045  A434EC          BF    G,SHIFT0       ABORT IF COUNT = 0                61601980
046  247D00  THRUD2  LI    FLR,0,D2                                         61601990
                     *                                                      61602000
                     * COME HERE FROM D1 FOR SRHA, SLHA                     61602010
                     *                                                      61602020
047  047B0F  SLHA    LI    MAR,15                                           61602030
048  0C300C  SLHA1   L     YD,YD,F                                          61602040
049  A4383E          BF    L,SLHL2                                          61602050
04A  047580          LI    MR0,'80'                                         61602060
04B  0474A0          EXB   MR0,MR0        (MR000) = SIGN BIT                61602070
04C  A43C3F          B     SLHL3                                            61602080
                     *                                                      61602090
                     * COME HERE FROM D1 FOR SRA, SLA                       61602100
                     *                                                      61602110
04D  047B1F  SLA     LI    MAR,31                                           61602120
04E  A43C48          B     SLHA1                                            61602130
                     *                                                      61602140
                     * COME HERE FROM D1 FOR RRL, RLL, SRL, SLL             61602150
                     *                                                      61602160
04F  047B1F  SLL     LI    MAR,31                                           61602170
050  A43C3E          B     SLHL2                                            61602180
                     *                                                      61602190
                     * COME HERE FROM D2 FOR SLLS, SLHL                     61602200
                     *                                                      61602210
051  047640  SLHLD2  L     CNTR,MDR                                         61602220
052  1C300A          L     YD,YD,SL+C0    SET C FLAG                        61602230
053  CC300C          L     YD,YD,F+IR     SET CC                            61602240
                     *                                                      61602250
                     *                                                      61602260
                     *                                                      61602270
054  047640  SLLD2   L     CNTR,MDR                                         61602280
055  18300A          L     YD&Q,YD,SL+C0                                    61602290
056  0C3002  SLL1D2  L     YD,YDP1        TO INCREASE YD FIELD              61602300
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057  0C200C          L      YD,Q,F                                          61602310
058  0C3003          L      YDM1,YD                                         61602320
059  CDD02C          O      YD,YD,MR0,F+IR        OR IN SIGN BIT, SET CC    61602330
                     *                                                      61602340
                     *                                                      61602350
                     *                                                      61602360
05A  047640     RLLD2  L      CNTR,MDR                                        61602370
05B  183009            L      YD&Q,YD,SL+CI                                   61602380
05C  A43C56            B      SLL1D2                                          61602390
                     *                                                      61602400
                     *                                                      61602410
                     *                                                      61602420
05D  047645     SLHAD2 INC    CNTR,MDR              (MDR) = SHIFT COUNT       61602430
05E  1C300A            L      YD,YD,SL+CO           SET C                     61602440
05F  143000            L      YD,YD,SR                                        61602450
060  CDD02C            O      YD,YD,MR0,F+IR        SET CC                    61602460
                     *                                                      61602470
                     * COME HERE THRU DROM2 FOR SRHA                        61602480
                     *                                                      61602490
061  0C300C     SRHAD2 L      YD,YD,F                                         61602500
062  03F100            INVI   Q,0                   (Q) = 'FFFF'              61602510
063  843865            BT     L,SRHL1                                         61602520
                     *                                                      61602530
                     * COME HERE THRU DROM2 FOR SRLS & SRHL                 61602540
                     *                                                      61602550
064  007D00     SRHLD2 LI     FLR&Q,0                                         61602560
065  047640     SRHL1  L      CNTR,MDR                                        61602570
066  14300B            L      YD,YD,SR+CI+CO                                  61602580
067  CC300C     NLONG  L      YD,YD,F+IR            SET CC                    61602590
                     *                                                      61602600
                     *                                                      61602610
                     *                                                      61602620
068  047640     SRLD2  L      CNTR,MDR                                        61602630
069  10300A     SRL1D2 L      YD&Q,YD,SR+CO                                   61602640
06A  A43C56            B      SLL1D2                                          61602650
                     *                                                      61602660
                     *                                                      61602670
                     *                                                      61602680
06B  047640     RRLD2  L      CNTR,MDR                                        61602690
06C  103009            L      YD&Q,YD,SR+CI                                   61602700
06D  A43C56            B      SLL1D2                                          61602710
                     *                                                      61602720
                     * COME HERE THRU DROM2 FOR SRA                         61602730
                     *                                                      61602740
06E  057845     SRAD2  DEC    MDR,MDR               (MDR) = SHIFT COUNT - 1 (0:30)  61602750
06F  04784C            L      MDR,MDR,F                                       61602760
070  A43469            BF     G,SRL1D2              GO DO LAST SHIFT          61602770
071  103000            L      YD&Q,YD,SR            SHIFT RIGHT R1 & R1+1 ONCE  61602780
072  0DD020            O      YD,YD,MR0             OR IN SIGN BIT            61602790
073  247D00            LI     FLR,0,D2              LOOP THRU D2              61602800
                     *                                                      61602810
                     *                                                      61602820
                     *                                                      61602830
074  047640     SLAD2  L      CNTR,MDR                                        61602840
075  183000            L      YD&Q,YD,SL                                      61602850
076  18300A            L      YD&Q,YD,SL+CO         SET C                     61602860
077  103000            L      YD&Q,YD,SR                                      61602870
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078 A43C56          B     SLL1D2                                                61602880
                    *                                                           61602890
                    *                                                           61602900
                    *                                                           61602910
079 047A20  STH     L     MAR,MR0           (MAR) = EFFCTIVE 2ND OPERAND        61602920
07A 043800          L     MDR,YD            (MDR) = (R1)                        61602930
07B 602000  STH2    L     Q,Q,MW            WRITE HW TO MEMORY                  61602940
07C C47C00          L     FLR,PSW,IR                                            61602950
                    *                                                           61602960
                    *                                                           61602970
                    *                                                           61602980
07D 04584E  AHM     A     MDR,YD,MDR,F+C0   SET FLAGS                           61602990
07E A43C19          B     RD2                                                   61603000
                    *                                                           61603010
                    * COME HERE IF SIGNS DIFFER FOR CH, CHI & CHR               61603020
                    *                                                           61603030
07F 00300C  DIFFER  L     Q,YD,F            SAVE YD IN Q, SET G,L FLAGS         61603040
080 1C300A          L     YD,YD,SL+C0       SET/RESET CARRY                     61603050
081 CC2000          L     YD,Q,IR           SET CC.                             61603060
                    *                                                           61603070
                    *                                                           61603080
                    *                                                           61603090
                    *                                                           61603100
                    * ILLEGAL INSTRUCTION OP-CODE DETECTED                      61603110
                    *                                                           61603120
082 057215  ILEG    DEC   LOC,LOC           DECREMENT LOC BY 2                  61603130
083 047B30          LI    MAR,ILGPSW                                            61603140
084 A43DBC          B     GENSWP            SWAP PSW                            61603150
                    *                                                           61603160
                    *  COMMON FOR NHR (D1) & NH, NHI (D2)                       61603170
                    *                                                           61603180
085 CE502C  NHR     N     YD,YD,MR0,F+IR                                        61603190
                    *                                                           61603200
                    * COMMON OHR (D1) & OH, OHI (D2)                           61603210
                    *                                                           61603220
086 CD002C  OHR     O     YD,YD,MR0,F+IR                                        61603230
                    *                                                           61603240
                    * COMMON XHR (D1) & XH, XHI (D2)                           61603250
                    *                                                           61603260
087 CF502C  XHR     X     YD,YD,MR0,F+IR                                        61603270
                    *                                                           61603280
                    * COMMON LHR (D1) & LH, LHI, LIS (D2)                      61603290
                    *                                                           61603300
088 CC702C  LHR     L     YD,MR0,F+IR                                           61603310
                    *                                                           61603320
                    *                                                           61603330
                    *                                                           61603340
089 CCF03C  LCS     TCMP  YD,YSI,F+IR                                           61603350
                    *                                                           61603360
                    * COMMON CHR (D1) & CH, CHI (D2)                           61603370
                    *                                                           61603380
08A 03502C  CHR     X     Q,YD,MR0,F        COMPARE SIGNS OF BOTH OPERANDS      61603390
08B 84387F          BT    L,DIFFER          IF DIFFERENT, GO TO DIFFER          61603400
                    *                                                           61603410
                    * COMMON CLHR (D1) & CLH, CLHI (D2)                        61603420
                    *                                                           61603430
08C C0D02E  CLHR    S     Q,YD,MR0,C0+F+IR                                      61603440
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                        *                                                                    61603450
                        * COME THER THRU DROM1 FOR LIS, AIS & SIS                            61603460
                        *                                                                    61603470
08D  247430             IMM     L       MR0,YSI,D2                                           61603480
                        *                                                                    61603490
                        * COME HERE FOR ACHR (D1) & ACH (D2)                                 61603500
                        *                                                                    61603510
08E  047C00             ACH     L       FLR,PSW                 GET OLD CC IN FLR            61603520
                        *                                                                    61603530
                        * COMMON AHR (D1) & AH, AHI, AIS (D2)                                61603540
                        *                                                                    61603550
08F  CC502F             AHR     A       YD,YD,MR0,CI+CO+F+IR                                 61603560
                        *                                                                    61603570
                        * COME HERE FOR SCHR (D1) & SCH (D2)                                 61603580
                        *                                                                    61603590
090  047C00             SCH     L       FLR,PSW                 GET OLD CC IN FLR            61603600
                        *                                                                    61603610
                        * COMMON SHR (D1) & SH, SHI,SIS (D2)                                 61603620
                        *                                                                    61603630
091  CCD02F             SHR     S       YD,YD,MR0,CI+CO+F+IR                                 61603640
                        *                                                                    61603650
                        *                                                                    61603660
092  C2502C             THI     N       Q,YD,MR0,F+IR                                        61603670
                        *                                                                    61603680
                        *                                                                    61603690
                        *  RR & RS BRANCHES                                                  61603700
                        *                                                                    61603710
                        *                                                                    61603720
                        * COMMON BALR (D1) & BAL (D2)                                        61603730
                        *                                                                    61603740
093  0C7010             BALR    L       YD,LOC                  (YD) = INCREMENTED LOC       61603750
094  047220             BRANCH  L       LOC,MR0                                              61603760
095  C47C00             NOB     L       FLR,PSW,IR                                           61603770
                        *                                                                    61603780
                        * COMMON BTCR (D1) & BTC (D2)                                        61603790
                        *                                                                    61603800
096  845C94             BTCR    BT      MSK,BRANCH                                           61603810
097  C47C00                     L       FLR,PSW,IR                                           61603820
                        *                                                                    61603830
                        * COMMON BFCR (D1) & BFC (D2)                                        61603840
                        *                                                                    61603850
098  A45C94             BFCR    BF      MSK,BRANCH                                           61603860
099  C47C00                     L       FLR,PSW,IR                                           61603870
                        *                                                                    61603880
                        *                                                                    61603890
                        * SHORT BRANCHES                                                     61603900
                        *                                                                    61603910
                        *                                                                    61603920
                        * COMMON FOR BTBS, BTFS (D1)                                         61603930
                        *                                                                    61603940
09A  845C9D             BTS     BT      MSK,SHORTB              IF ANY CONDITION TRUE, BRANCH 61603950
09B  C47C00                     L       FLR,PSW,IR                                           61603960
                        *                                                                    61603970
                        * COMMON FOR BFBS, BFFS (D1)                                         61603980
                        *                                                                    61603990
09C  845C95             BFS     BT      MSK,NOB                 IF ANY CONDITION TRUE, DON'T BRANCH 61604000
09D  057215             SHORTB  DEC     LOC,LOC                 DECREMENT LOC BY 2           61604010
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09E  007030          L     Q,YSI                                          61604020
09F  206030          A     Q,Q,YSI,D2          (Q) = DISPLACEMENT IN # OF BYTES 61604030
                                                                          61604040
                   * COME HERE THRU DROM2 FOR BTBS, BFBS                  61604050
                   *                                                      61604060
0A0  012000  BKWORD TCMP  Q,Q                 GET TWO'S COMPLEMENT       61604070
                   *                                                      61604080
                   * COME HERE THRU DROM2 FOR BTFS, BFFS                  61604090
                   *                                                      61604100
0A1  046210  FRWORD A     LOC,Q,LOC           INCREMENT OR DECREMENT LOC 61604110
0A2  C47C00          L     FLR,PSW,IR                                     61604120
                   *                                                      61604130
                   *                                                      61604140
                   *  BRANCH ON INDEX INSTRUCTIONS                        61604150
                   *                                                      61604160
                   *                                                      61604170
                   * COME HERE THRU DROM2                                 61604180
                   *                                                      61604190
0A3  015025  BXH     S     Q,MR0,YD,JAMCI&C0   (Q) = DECREMENTED INDEX - LIMIT - 1 61604200
0A4  A43CA6          B     BX1                                            61604210
                   *                                                      61604220
                   * COME HERE THRU DROM2                                 61604230
                   *                                                      61604240
0A5  00D02A  BXLE    S     Q,YD,MR0,C0         (Q) = LIMIT - INCREMENTED INDEX 61604250
                   *                                                      61604260
0A6  841CA8  BX1     BT    C,BXNOB                                        61604270
0A7  047240          L     LOC,MDR                                        61604280
0A8  C47C00  BXNOB   L     FLR,PSW,IR                                     61604290
                   *                                                      61604300
                   *                                                      61604310
                   * BYTE HANDLING INSTRUCTIONS                           61604320
                   *                                                      61604330
                   *                                                      61604340
                   *                                                      61604350
                   * COME HERE THRU DROM2 FOR LB                          61604360
                   *                                                      61604370
0A9  0474C0  LB      L     MR0,MDR,CS          (MR0 7:15) = BYTE TO BE LOADED 61604380
                   *                                                      61604390
                   * COME HERE THRU DROM1 FOR LBR                         61604400
                   *                                                      61604410
0AA  0C7020  LBR     L     YD,MR0                                         61604420
0AB  0E51FF          NI    YD,YD,'FF'          ISOLATE BYTE               61604430
0AC  C47C00          L     FLR,PSW,IR                                     61604440
                   *                                                      61604450
                   * COME HERE THRU DROM2                                 61604460
                   *                                                      61604470
0AD  0655FF  CLB     NI    MR0,YD,'FF'         (MR0) = LS BYTE OF 1ST OPERAND 61604480
0AE  0071FF          LI    Q,'FF'                                         61604490
0AF  0260C0          N     Q,Q,MDR,CS          (Q) = LS BYTE OF 2ND OPERAND 61604500
0B0  C5642E          S     MR0,MR0,Q,F+C0+IR   SET CC                     61604510
                   *                                                      61604520
                   * COME HERE THRU DROM2                                 61604530
                   *                                                      61604540
0B1  043400  STB     L     MR0,YD                                         61604550
0B2  0478A0          EXB   MDR,MR0                                        61604560
0B3  A43C7B          B     STH2                                           61604570
                   *                                                      61604580
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                   *
                   *
0B4  047820   STBR    L     MDR,MR0            (MDR) = SECOND OPERAND
0B5  047B01           LI    MAR,1              (MAR) = ODD
0B6  043400           L     MR0,YD             (MR0) = 1ST OPERAND
0B7  0478A0           EXB   MDR,MR0            GET LS BYTE FROM 1ST OPERAND
0B8  2C7240           L     YS,MDR,D2          INSTRUCTION READ THRU DROM2
                   *
                   *
                   *
0B9  2C70A0   EXBR    EXB   YD,MR0,D2          IR THRU DROM2
                   *
                   *
                   *
                   *
                   *
                   * COME HERE THRU DROM2
                   *
0BA  841C95   LM      BT    C,NOB
0BB  457425           DEC   MR0,MR0,MR         DECREMENT COUNT
0BC  046A50           A     MAR,Q,MAR
0BD  2C7042           L     YDP1,MDR,D2        LOAD GENERAL REGISTER
                   *
                   * COME HERE THRU DROM2
                   *
0BE  043802   STM     L     MDR,YDP1
0BF  657425           DEC   MR0,MR0,MW         STORE GENERAL REGISTER INTO MEMORY
0C0  841C95           BT    C,NOB
0C1  246A50           A     MAR,Q,MAR,D2       INCREMENT MAR. LOOP THRU D2
                   *
                   * COME HERE THRU DROM2 FOR LPSW
                   *
0C2  043400   LPSW    L     MR0,YD             SAVE YD IN MR0
0C3  A43DC7           B     LPSW1
                   *
                   * COME HERE THRU DROM1 FOR EPSR
                   *
0C4  047400   EPSR    L     MR0,PSW
0C5  0C7020           L     YD,MR0             (YD) = OLD PSW
0C6  044000           L     PSW,YS             NEW PSW
0C7  A43DCB           B     EPSR1
                   *
                   * COME HERE THRU DROM2
                   *
0C8  003000   SINT    L     Q,YD               SAVE YD IN Q.
0C9  0C71FF           LI    YD,'FF'            (MR0) = 2ND OPERAND = DEV ADR
0CA  1E5020           N     YD,YD,MR0,SL       (YD) = 2 X DEV ADR
0CB  A43DA0           B     SINT1
                   *
                   * COME HERE THRU DROM2
                   *
0CC  A43DEA   SVCD2   B     SVC1
                   *
                   *
                   * SHORT SHIFTS
                   *
                   *
```

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                        *                                                                    61605160
                        *                                                                    61605170
                        * COMMON FOR SRLS, SLLS (D1)                                         61605180
                        *                                                                    61605190
0CD  04783C     SLLS    L       MDR,YSI,F       (MDR) = SHIFT COUNT                          61605200
0CE  843446             BT      G,THRUD2                                                     61605210
0CF  CC300C             L       YD,YD,F+IR      ABORT IF COUNT IS ZERO                       61605220
                        *                                                                    61605230
                        *                                                                    61605240
                        * RR TYPE I/O INSTRUCTIONS                                          61605250
                        *                                                                    61605260
                        *                                                                    61605270
                        * COME HERE THRU DROM1 FOR AIR                                      61605280
                        *                                                                    61605290
0D0  0C7071     AIR     ACK     YD              GET INTERRUPTING DEV ADR IN R1               61605300
                        *                                                                    61605310
                        * COMMON FOR RDR, WDR, RHR, WHR, SSR, OCR                           61605320
                        *                                                                    61605330
0D1  043E01     IORR    ADR     YD              ADDRESS THE DEVICE                           61605340
0D2  207100             LI      Q,0,D2          (Q) = 0                                      61605350
                        *                                                                    61605360
                        *                                                                    61605370
                        *  BLOCK I/O                                                         61605380
                        *                                                                    61605390
                        *                                                                    61605400
                        * COME HERE FOR RBR, WBR                                            61605410
                        *                                                                    61605420
0D3  043E01     RBRWBR  ADR     YD              ADDRESS THE DEVICE                           61605430
0D4  047431             L       MR0,YSI,CYD&SWA                                              61605440
0D5  003A02     BLKRR1  L       MAR&Q,YDP1      (MAR) = BLOCK START ADDRESS                  61605450
0D6  057425             DEC     MR0,MR0                                                      61605460
0D7  A41CD5             BF      C,BLKRR1                                                     61605470
0D8  043800             L       MDR,YD          (MDR) = BLOCK END ADDRESS                    61605480
                        *                                                                    61605490
                        * COMMON TO WB,RB,WBR,RBR                                          61605500
                        *                                                                    61605510
00D9    0D9     BLKIO1  EQU     *               (MAR) = BLOCK START ADDRESS                  61605520
0D9  016040             S       Q,MDR,Q         (Q) = # OF BYTES TO BE TRANSFERRED           61605530
0DA  00200C     BLKIO2  L       Q,Q,F           SET FLAGS HERE                               61605540
0DB  8439D8             BT      L,FINISH                                                     61605550
0DC  402000             L       Q,Q,MR                                                       61605560
0DD  047C72     BLKIO3  SS      FLR                                                          61605570
0DE  8421D9             BT      V+G+L,TERMIN    IF BAD STATUS / TIME-OUT, TERMINATE          61605580
0DF  841CDD             BT      C,BLKIO3        LOOP TILL BSY DROPS                          61605590
0E0  202000             L       Q,Q,D2          GO TRANSFER THE BYTE                         61605600
                        *                                                                    61605610
                        * COME HERE THRU DROM2 FOR WB & WBR                                61605620
                        *                                                                    61605630
0E1  047EC4     WBR     WD      MDR,CS          WRITE A BYTE TO THE DEVICE                   61605640
0E2  00A005             DEC     Q,Q             DECREMENT BYTE COUNT                         61605650
0E3  A43CE7             B       RB1                                                          61605660
                        *                                                                    61605670
                        * COME HERE THRU DROM2 FOR RB & RBR                                 61605680
                        *                                                                    61605690
0E4  047474     RBR     RD      MR0             READ A BYTE FROM DEVICE                      61605700
                        *                                                                    61605710
                        * COME HERE FROM EMULATION SEQUENCE FOR AL                          61605720
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                      *                                                                    61605730
 0E5  0478A0      FROMAL EXB   MDR,MR0                                                     61605740
 0E6  60A005             DEC   Q,Q,MW             WRITE THE BYTE INTO MEMORY               61605750
 0E7  047A55      RB1    INC   MAR,MAR                                                     61605760
 0E8  A43CDA             B     BLKIO2                                                      61605770
                      *                                                                    61605780
                      *                                                                    61605790
                      *                                                                    61605800
                      * COME HERE THRU DROM1 FOR DHR; THRU DROM2 FOR DH                    61605810
                      *                                                                    61605820
 0E9  A43E00      DHR    B     DHR1                                                        61605830
                      *                                                                    61605840
                      * COME HERE THRU DROM1 FOR MHR; THRU DROM2 FOR MH                    61605850
                      *                                                                    61605860
 0EA  A43E32      MHR    B     MHR1                                                        61605870
                      *                                                                    61605880
                      * COME HERE THRU DROM1 FOR MHUR; THRU DROM2 FOR MHU                  61605890
                      *                                                                    61605900
 0EB  A43E48      MHUR   B     MHUR1                                                       61605910
                      *                                                                    61605920
                      * SHIFT COUNT FOUND TO BE ZERO                                       61605930
                      *                                                                    61605940
 0EC  043800      SHIFT0 L     MDR,YD             SAVE YD IN MDR                           61605950
 0ED  0C7110             LI    YD,16                                                       61605960
 0EE  0E505C             N     YD,YD,MAR,F        SEE IF LONG SHIFTS                       61605970
 0EF  0C7040             L     YD,MDR             RESTORE YD                               61605980
 0F0  A43467             BF    G,NLONG                                                     61605990
 0F1  047D00             LI    FLR,0              YES, CLEAR FLR                           61606000
 0F2  A43C56             B     SLL1O2             GO SET CC                                61606010
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                        ORG   '100'                                                    61606020
                    *                                                                  61606030
                    *                                                                  61606040
                    * ON POWER UP, '100' IS JAMMED INTO RAR                           61606050
                    *                                                                  61606060
                    *                                                                  61606070
100  007102         PWRUP  LI    Q,2                                                   61606080
101  84ED47                BT    HW,ALOI          'HW' ACTIVE ON POWER UP IF           61606090
                    *                             ALO IS IN THE SYSTEM                 61606100
                    *                                                                  61606110
                    * ALO IS NOT HOOKED UP IN THE SYSTEM                              61606120
                    *                                                                  61606130
102  047B24                LI    MAR,APSW                                              61606140
103  447B26                LI    MAR,ALOC,MR                                           61606150
104  047041                L     PSW,MDR,CYD&SWA  LOAD PSW, CLEAR YD FIELD             61606160
105  44750F                LI    MR0,15,MR                                             61606170
106  047240                L     LOC,MDR          LOAD LOC                             61606180
107  047B22                LI    MAR,PNTR                                              61606190
108  402000                L     Q,Q,MR                                                61606200
109  047A40                L     MAR,MDR                                               61606210
10A  457425         LDREG  DEC   MR0,MR0,MR                                           61606220
10B  0C7042                L     YDP1,MDR         LOAD GENERAL REGISTER                61606230
10C  046A50                A     MAR,Q,MAR        INCREMENT MAR BY 2                   61606240
10D  A41D0A                BF    C,LDREG          LOOP TILL ALL REGISTERS ARE LOADED   61606250
                    *                                                                  61606260
10E  047501                LI    MR0,1                                                 61606270
10F  047E21                ADR   MR0              ADDRESS THE DISPLAY PANEL            61606280
110  047B20                LI    MAR,'20'                                              61606290
111  403000                L     Q,YD,MR          SAVE YD IN Q FOR MMF                 61606300
                    *                                                                  61606310
112  047C40                L     FLR,MDR          (FLR) = SAVED DISPLAY STATUS 0:3     61606320
113  842115                BT    V+G+L,LOCDIS     IF WAS NOT IN RUN MODE, DISPLAY LOC  61606330
                    *                                                                  61606340
                    * DISPLAY PANEL WAS IN RUN MODE                                   61606350
                    *                                                                  61606360
114  846D53                BT    ARST,MMF         IF PROCESSOR IS EQUIPPED WITH AN     61606370
                    *                             AUTO-RESTANT OPTION, DO MMF PSW SWAP 61606380
115  047410         LOCDIS L     MR0,LOC          DISPLAY LOC IN D1 & D2               61606390
116  047945                LI    MDR,'45'         INDICATE  FN 5                       61606400
117  047B00         MAR0   LI    MAR,0            DISPLAY 0    IN D3 & D4              61606410
                    *                                                                  61606420
118  047E24         OUTDIS WD    MR0              D1 = (MR0 8:15)                      61606430
119  047EA4                WD    MR0,CS           D2 = (MR0 0:7)                       61606440
11A  047E54                WD    MAR              D3 = (MAR 8:15)                      61606450
11B  047ED4                WD    MAR,CS           D4 = (MAR 0:7)                       61606460
11C  047E44                WD    MDR              D5 = (MDR 8:15)                      61606470
                    *                                                                  61606480
                    *                                                                  61606490
                    * UN-INTERRUPTABLE IDLE LOOP                                      61606500
                    *                                                                  61606510
11D  002001         IDLE   L     Q,Q,CYD&SWA                                           61606520
11E  003001                L     Q,YD,CYD&SWA     SAVE YD IN Q, WAIT LIGHT ON          61606530
11F  84AD2F         IDLE1  BT    CATN,IDLEX                                            61606540
120  A4F51F                BF    PPF,IDLE1                                             61606550
                    *                                                                  61606560
                    *                                                                  61606570
                    *                                                                  61606580
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                    * POWER IS GOING DOWN                                                    61606590
                    *                                                                        61606600
 121  047B24    PWRDWN LI    MAR,APSW                                                       61606610
 122  047800           L     MDR,PSW                                                        61606620
 123  647B26           LI    MAR,ALOC,MW      SAVE CURRENT PSW                              61606630
 124  047810           L     MDR,LOC                                                        61606640
 125  647B22           LI    MAR,PNTR,MW      SAVE CURRENT LOC                              61606650
 126  44750F           LI    MR0,15,MR                                                      61606660
 127  047A41           L     MAR,MDR,CYD&SWA  (MAR) = REGISTER SAVE AREA START              61606670
 128  007102           LI    Q,2                                                            61606680
 129  043802    SAVREG L     MDR,YDP1                                                       61606690
 12A  657425           DEC   MR0,MR0,MW       SAVE GENERAL REGISTER                         61606700
 12B  046A50           A     MAR,Q,MAR                                                      61606710
 12C  A41D29           BF    C,SAVREG         LOOP TILL ALL REGISTERS ARE SAVED             61606720
                    *                                                                       61606730
 12D  047844    POW    L     MDR,MDR,POW      WAIT FOR MEMORY WRITE COMPLETION              61606740
                    *                         SYSTEM CLEAR                                  61606750
 12E  A43D2D           B     POW                                                            61606760
                    *                                                                       61606770
                    *                                                                       61606780
 12F  84B543    IDLEX  BT    SNGL,CLRWT       IF SNGL, RESET WAIT BIT IN PSW THEN           61606790
                    *                         DO USER'S INSTRUCTIONS.                       61606800
                    *                                                                       61606810
                    * CONSOLE SERVICE                                                       61606820
                    *                                                                       61606830
                    * ADD, RD, WRT, RUN, REG N OR FN N KEY(S) DEPRESSED.                    61606840
                    *                                                                       61606850
 130  047501    CONSER LI    MR0,1                                                          61606860
 131  047E21           ADR   MR0              ADDRESS THE DISPLAY PANEL                     61606870
                    *                         YD IS SAVED IN Q                              61606880
 132  0C7180           LI    YD,'80'                                                        61606890
 133  043E02           OC    YD               NORMAL MODE                                   61606900
 134  047E21           ADR   MR0                                                            61606910
 135  0C7072           SS    YD                                                             61606920
 136  043400           L     MR0,YD           (MR0 8:15) = DISPLAY STATUS 0:7               61606930
 137  047704           LI    CNTR,4                                                         61606940
 138  143000           L     YD,YD,SR         SHIFT RIGHT YD 4 TIMES.                       61606950
 139  047B20           LI    MAR,'20'                                                       61606960
 13A  043800           L     MDR,YD           X'20'(12:15) = DISPLAY STATUS 0:3             61606970
 13B  643C00           L     FLR,YD,MW        (FLR) = DISPLAY STATUS 0:3                    61606980
 13C  0C2000           L     YD,Q             RESTORE YD                                    61606990
                    *                                                                       61607000
 13D  84B559           BT    SNGL,CONTIN      IF SNGL, GO TO CONTIN                         61607010
 13E  842D5D           BT    V,FNREG          FN N OR REG N KEYS DEPRESSED                  61607020
 13F  047A10           L     MAR,LOC                                                        61607030
 140  402000           L     Q,Q,MR           READ HW SPECIFIED BY LOC                      61607040
 141  843964           BT    L,ADDWRT         ADD OR WRT KEY DEPRESSED                      61607050
 142  843568           BT    G,RDKEY          RD KEY DEPRESSED                              61607060
                    *                         IF NONE ABOVE, RUN KEY IS DEPRESSED.          61607070
                    *                                                                       61607080
        0143  CLRWT  EQU   *                  YD IS SAVED IN Q                              61607090
 143  0CF101           TCMPI YD,1                                                           61607100
 144  143000           L     YD,YD,SR         (YD) = '7FFF'                                 61607110
 145  065000           N     PSW,YD,PSW       RESET WAIT BIT IN PSW                         61607120
 146  A43DA9           B     SINT2                                                          61607130
                    *                                                                       61607140
                    * SUPPORT ROUTINES                                                     61607150
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                    *                                                                    61607160
                    * ALO SUPPORT : LOAD PROGRAM FROM ALO INTO MEMORY. START EXECUTION.  61607170
                    *                                                                    61607180
          0147      ALO1    EQU     *                   THE ALO (HW DEVICE) IS ADDRESSED   61607190
                    *                                   ON POWER UP.                       61607200
 147  047074              RD      PSW                 GET PSW                            61607210
 148  047274              RD      LOC                 GET LOC                            61607220
 149  047A74              RD      MAR                 (MAR) = PROGRAM START ADDRESS      61607230
 14A  0C7074              RD      YD                  (YD) = PROGRAM FINAL ADDRESS       61607240
 14B  14D05C              S       YD,YD,MAR,SR+F      ((YD)) = # OF HALFWORDS IN PROGRAM 61607250
 14C  A4351D              BF      G,IDLE              IF NON-POSITIVE, ABORT UNLOADING ALO61607260
                    *                                                                    61607270
 14D  047874        ALO2  RD      MDR                 (MDR) = NEXT HW OF PROGRAM         61607280
 14E  6CB005              DEC     YD,YD,MW            WRITE THAT HW INTO MEMORY          61607290
 14F  046A50              A       MAR,Q,MAR           INCREMENT MAR BY 2                 61607300
 150  A41D40              BF      C,ALO2                                                 61607310
                    *                                                                    61607320
 151  1C700A        LSU3  L       YD,PSW,SL+C0        LOOK @ PSW WAIT BIT                61607330
 152  A43DD6              B       EPSR3                                                  61607340
                    *                                                                    61607350
                    * ON POWER UP, CONSOLE WAS IN RUN MODE & AUTO-RESTART PRESENT       61607360
                    *                                                                    61607370
          0153      MMF     EQU     *                   YD IS SAVED IN Q                   61607380
 153  1C7000              L       YD,PSW,SL           LOOK @ PSW02                       61607390
 154  1C3000              L       YD,YD,SL                                               61607400
 155  1C300A              L       YD,YD,SL+C0                                            61607410
 156  0C2000              L       YD,Q                RESTORE YD                         61607420
                    *                                                                    61607430
 157  841DB8              BT      C,MMALF1            DO MACHINE MALFUNCTION INT PSW SWAP61607440
 158  A43D43              B       CLRWT                                                  61607450
                    *                                                                    61607460
                    * SNGL IS SET                                                       61607470
                    *                                                                    61607480
 159  007102        CONTIN LI     Q,2                                                    61607490
 15A  046210              A       LOC,Q,LOC           INCREMENT LOC BY 2                 61607500
 15B  047D00              LI      FLR,0                                                  61607510
 15C  A43C01              B       START1              DO USER'S INSTRUCTION              61607520
                    *                                                                    61607530
                    * FN N OR REG N KEYS DEPRESSED                                      61607540
                    *                                                                    61607550
 15D  841D75        FNREG BT      C,DISPLY            STATUS = 11XXXXXX = NOT FN 0       61607560
 15E  047C20              L       FLR,MR0                                                61607570
 15F  840175              BT      C+V+G+L,DISPLY                                         61607580
                    *                                                                    61607590
 160  047501              LI      MR0,1               CONSOLE INT.(FN 0)                 61607600
 161  047C80              EXB     FLR,PSW                                                61607610
 162  841D9E              BT      C,CONINT            PSW04 = 1. SIMULATE CONSOLE INT.   61607620
 163  A43D43              B       CLRWT                                                  61607630
                    *                                                                    61607640
                    *  ADD OR WRT KEY DEPRESSED                                        61607650
                    *                                                                    61607660
 164  047874        ADDWRT RD     MDR                 (MDR 0:15) = (S1 SWITCH REGISTER)  61607670
 165  0070F4              RD      Q,CS                (Q 0:7 )   = (S2 SWITCH REGISTER)  61607680
 166  046840              A       MDR,Q,MDR           (MDR) = S2,S1                      61607690
 167  84356E              BT      G,ADD                                                  61607700
                    *                                                                    61607710
                    * RD KEY DEPRESSED                                                  61607720
```

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                 *
168  607102      RDKEY  LI    Q,2,MW
169  046210             A     LOC,Q,LOC              INCREMENT LOC BY 2
16A  047440             L     MR0,MDR                DISPLAY MDR IN D1 & D2
16B  047A10             L     MAR,LOC                DISPLAY LOC IN D3 & D4
16C  047980             LI    MDR,'80'               INDICATE MEMORY ADDRESS/DATA
16D  A43D18             B     OUTDIS
                 *
                 * ADD KEY DEPRESSED
                 *
16E  047240      ADD    L     LOC,MDR                (LOC) = S2,S1 SWITCH REG.
16F  A43D15             B     LOCDIS                 DISPLAY SWITCH REG DATA
                 *
                 * TO HELP DISTINGUISH I/O ATN, CATN, SNGL & MACHINE MALFUNCTION
                 *
170  057215      HELP   DEC   LOC,LOC                DECREMENT LOC BY 2
                 *
171  003000      HELP1  L     Q,YD                   SAVE YD IN Q
172  84B9B9             BT    MALF,MMALF             MACHINE MALFUNCTION HAS OCCURED
173  849D99             BT    ATN,IOATN              REQUEST FOR ATTENTION FROM I/O BUS
174  84AD30             BT    CATN,CONSER            CONSOLE SERVICE DESIRED
                 *                                   USER PROGRAM BEING SINGLE-STEPPED.
                 *                                   DISPLAY REG N OR PSW OR LOC.
                 *
                 * TO DISPLAY REG N OR PSW OR LOC ETC.
                 *
175  047501      DISPLY LI    MR0,1
176  047E21             ADR   MR0                    ADDRESS THE DISPLAY PANEL
177  047472             SS    MR0
                 *
178  007020             L     Q,MR0
179  046A20             A     MAR,Q,MR0
17A  0070D0             EXB   Q,MAR
17B  046A50             A     MAR,Q,MAR
17C  00710F             LI    Q,15
17D  026A50             N     MAR&Q,Q,MAR            (MAR) = N = REGISTER NUMBER
17E  05E920             OI    MDR,Q,'20'             (MDR) = '2N'
                 *
17F  047C20             L     FLR,MR0                (FLR) = DISPLAY STATUS 4:7
180  841D8E             BT    C,REGDIS               BIT 4 SET  (REG N)
181  042C00             L     FLR,Q                  (FLR) = STATUS BITS 5,6,7,0
182  84151D             BT    C+G,IDLE
183  842D89             BT    V,PSWLOC               BIT 6 SET  (FN 4 OR FN 5)
184  A4391D             BF    L,IDLE
                 *                                   MUST BE FN 1
                 *
                 * FN 1 KEYS DEPRESSED
                 *
185  047874      FN1    RD    MDR
186  0070F4             RD    Q,CS
187  046040             A     PSW,Q,MDR              (PSW) = SWITCH REGISTER
188  A43D8B             B     FN11
                 *
                 * FN 4 OR FN 5 KEYS DEPRESSED
                 *
189  047C50      PSWLOC L     FLR,MAR                (MAR) = 4 FOR PSW, 5 FOR LOC
18A  843915             BT    L,LOCDIS
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18B  047400      FN11   L      MR0,PSW                DISPLAY PSW IN D1 & D2          61608300
                 *                                    DISPLAY 0     IN D3 & D4        61608310
18C  047944             LI     MDR,'44'               INDICATE FN 4                   61608320
18D  A43D17             B      MAR0                                                   61608330
                 *                                                                   61608340
                 * REG N KEYS ARE DEPRESSED                                          61608350
                 *                                                                   61608360
18E  002001      REGDIS L      Q,Q,CYD&SWA            CLEAR YD FIELD                  61608370
18F  057A55      REGN   DEC    MAR,MAR                                                61608380
190  043402             L      MR0,YDP1               DISPLAY REG N IN D1 & D2        61608390
191  A41D8F             BF     C,REGN                                                 61608400
                 *                                    DISPLAY 0     IN D3 & D4        61608410
192  A43D17             B      MAR0                   MDR INDICATES REG N             61608420
                 *                                                                   61608430
                 * INTERRUPTABLE WAIT LOOP                                           61608440
                 *                                                                   61608450
193  002001      WAIT   L      Q,Q,CYD&SWA                                            61608460
194  003001             L      Q,YD,CYD&SWA           SAVE YD IN Q, WAIT LIGHT ON     61608470
195  848575             BT     SNGL,DISPLY                                            61608480
196  849971      WAIT1  BT     MALF+ATN,HELP1                                         61608490
197  84AD2F             BT     CATN,IDLEX                                             61608500
198  A43D96             B      WAIT1                                                  61608510
                 *                                                                   61608520
                 *                                                                   61608540
          0199   IOATN  EQU    *                                                      61608550
199  8475AB             BT     DATN,IODMA             HW ORIENTED DMA ON I/O BUS      61608560
                 *                                    IS REQUESTING ATTENTION.        61608570
19A  047B40             LI     MAR,'40'                                               61608580
19B  047C80             EXB    FLR,PSW                LOOK @ PSW04                    61608590
19C  A41DBC             BF     C,GENSWP                                               61608600
                 *                                                                   61608610
                 * AUTOMATIC I/O SERVICE                                             61608620
                 *                                                                   61608630
19D  047471      IOSVC  ACK    MR0                    (MR0) = INTERRUPTING DEV ADR    61608640
                 *                                                                   61608650
                 *                                                                   61608660
                 * CONSOLE INTERRUPT                                                 61608670
                 *                                                                   61608680
          019E   CONINT EQU    *                                                      61608690
19E  003000             L      Q,YD                   SAVE YD IN Q                    61608700
19F  1C7020             L      YD,MR0,SL              [(YD)] = 2XDEV ADR              61608710
          01A0   SINT1  EQU    *                      FROM SINT EMULATION ROUTINE     61608720
1A0  045BD0             AI     MAR,YD,'D0'                                            61608730
1A1  4C7102             LI     YD,2,MR                                                61608740
1A2  047A40             L      MAR,MDR                (MAR) = I/O SERVICE TABLE ENTRY 61608750
1A3  047800             L      MDR,PSW                                                61608760
1A4  645A50             A      MAR,YD,MAR,MW          STORE OLD PSW                   61608770
1A5  047810             L      MDR,LOC                                                61608780
1A6  645A50             A      MAR,YD,MAR,MW          STORE OLD LOC                   61608790
1A7  445250             A      LOC,YD,MAR,MR          NEW LOC                         61608800
1A8  047040             L      PSW,MDR                NEW PSW                         61608810
1A9  0C2000      SINT2  L      YD,Q                   RESTORE YD                      61608820
1AA  C47C00             L      FLR,PSW,IR             DO USER'S INSTRUCTION           61608830
                 *                                                                   61608840
                 * TO SERVICE DATA TRANSFER REQUEST FROM DMA ON I/O BUS              61608850
                 *                                                                   61608860
          01AB   IODMA  EQU    *                                                      61608870
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1AB  047500          LI    MR0,0                                          61608880
1AC  047E21          ADR   MR0                 KNOCK DOWN A ADDRESSED DEVICE 61608890
1AD  047A74          RD    MAR                 FIRST HW IS MEMORY ADDRESS   61608900
1AE  047C50          L     FLR,MAR                                          61608910
1AF  007102          LI    Q,2                                              61608920
1B0  8439B5          BT    L,DMARD             READ IF MEMORY ADDRESS IS ODD 61608930
                     *                                                      61608940
1B1  446A50  DMAWRT  A     MAR,Q,MAR,MR        INCREMENT MAR.               61608950
1B2  047E44          WD    MDR                 WRITE TO DMA DEVICE          61608960
1B3  8475B1          BT    DATN,DMAWRT                                      61608970
1B4  C47C00          L     FLR,PSW,IR          FETCH NEXT INSTRUCTION       61608980
                     *                                                      61608990
1B5  047874  DMARD   RD    MDR                 READ HW FROM DMA DEVICE      61609000
1B6  646A50          A     MAR,Q,MAR,MW        WRITE INTO MEMORY            61609010
1B7  8475B5          BT    DATN,DMARD          LOOP TILL 'DATN' ACTIVE      61609020
1B8  C47C00          L     FLR,PSW,IR                                       61609030
                     *                                                      61609040
                     * MACHINE MALFUNCTION DETECTED                         61609050
                     *                                                      61609060
          01B9 MMALF EQU   *                                                61609070
1B9  84F521          BT    PPF,PWRDWN          PRIMARY POWER FAIL           61609080
1BA  84AD30          BT    CATN,CONSER         TO EXIT IF MICROPROGRAM HANGS UP 61609090
                     *                          IN MACHINE MALFUNCTION PSW SWAPS 61609100
1BB  047B38  MMALF1  LI    MAR,OMMPSW                                       61609110
                     *                                                      61609120
                     * COMMON PSW SWAP ROUTINE                              61609130
                     *                                                      61609140
1BC  043400  GENSWP  L     MR0,YD              SAVE YD IN MR0               61609150
                     *                                                      61609160
1BD  047800  QUEINT  L     MDR,PSW                                          61609170
1BE  007102          LI    Q,2                                              61609180
1BF  646A50          A     MAR,Q,MAR,MW        SAVE OLD PSW                 61609190
1C0  047810          L     MDR,LOC                                          61609200
1C1  646A50          A     MAR,Q,MAR,MW        SAVE OLD LOC                 61609210
1C2  4C7101          LI    YD,1,MR                                          61609220
1C3  A4B9C7          BF    MALF,LPSW1                                       61609230
                     *                                                      61609240
1C4  84F9C6          BT    MPE,LSET                                         61609250
1C5  05D840          O     MDR,YD,MDR          OR IN L FLAG                 61609260
1C6  047100  LSET    LI    PSW,0               RESET MPE & EPF              61609270
                     *                                                      61609280
          01C7 LPSW1 EQU   *                   FROM LPSW                    61609290
1C7  047040          L     PSW,MDR             NEW PSW                      61609300
1C8  046A50          A     MAR,Q,MAR                                        61609310
1C9  402000          L     Q,Q,MR                                           61609320
1CA  047240          L     LOC,MDR             NEW LOC                      61609330
          01CB EPSR1 EQU   *                   FROM EPSR                    61609340
1CB  047C80          L     FLR,PSW,CS          LOOK @ PSW06                 61609350
1CC  A435D4          BF    G,EPSR2                                          61609360
                     *                                                      61609370
1CD  047B80  QUENBL  LI    MAR,'80'                                         61609380
1CE  447D00          LI    FLR,0,MR                                         61609390
1CF  047A40          L     MAR,MDR             (MAR) = QUEUE ADDRESS        61609400
1D0  447B82          LI    MAR,'82',MR                                      61609410
1D1  0C71FF          LI    YD,'FF'                                          61609420
1D2  0E504C          N     YD,YD,MDR,F         SEE IF LIST IS EMPTY         61609430
1D3  8435BD          BT    G,QUEINT            TAKE QUEUE SERVICE INTERRUPT 61609440
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                      *
1D4  1C700A    EPSR2  L     YD,PSW,SL+CO          CARRY = PSW00
1D5  0C7020           L     YD,MR0                RESTORE YD
                      *
1D6  841D93    EPSR3  BT    C,WAIT
1D7  C47C00           L     FLR,PSW,IR            DO USER'S INSTRUCTION
                      *
                      *
                      *
                      *  USER INSTRUCTIONS EMULATION CONTINUED HERE
                      *
                      *
1D8  047D00    FINISH LI    FLR,0
1D9  C02000    TERMIN L     Q,Q,IR
                      *
                      * ROUTINE FOR AL
                      *
1DA  84DDDC    AL1    BT    AMOD,ALX
1DB  007100           LI    Q,0
1DC  006040    ALX    A     Q,Q,MDR               AL TO (Q) ADDRESS
1DD  047B78           LI    MAR,'78'
1DE  447B80           LI    MAR,'80',MR           READ BINDV ENTRY @ X'78'
1DF  00E05A           S     Q,Q,MAR,CO            (Q) = # OF BYTES TO BE TRANSFERRED.
1E0  841DD8           BT    C,FINISH              ABORT IF LESS THAN ZERO
1E1  047EC1           ADR   MDR,CS                ADDRESS THE DEVICE
1E2  047E42           OC    MDR                   SET UP THE DEVICE
                      *
1E3  047C72    LEADER SS    FLR
1E4  8421D9           BT    V+G+L,TERMIN          TERMINATE IF BAD STATUS/TIME-OUT
1E5  841DE3           BT    C,LEADER              LOOP TILL BSY DROPS
1E6  047474           RD    MR0
1E7  44742C           L     MR0,MR0,F+MR
1E8  8434E5           BT    G,FROMAL              NON-ZERO BYTE IS READ
1E9  A43DE3           B     LEADER                LOOP
                      *
                      * ROUTINE FOR SVC
                      *
1EA  047820    SVC1   L     MDR,MR0               (MDR) = SECOND OPERAND
1EB  047B94           LI    MAR,'94'
1EC  647B96           LI    MAR,'96',MW           WRITE IT @ X'94'
1ED  047800           L     MDR,PSW
1EE  647B98           LI    MAR,'98',MW           WRITE OLD PSW @ X'96'
1EF  047810           L     MDR,LOC
1F0  647B9A           LI    MAR,'9A',MW           WRITE OLD LOC @ X'98'
                      *
1F1  007460           L     MR0&Q,YDI
1F2  406020           A     Q,Q,MR0,MR            READ NEW PSW FROM X'9A'
1F3  046B9C           AI    MAR,Q,'9C'            (MAR) = '9C' + 2(YDI)
1F4  047040           L     PSW,MDR               NEW PSW
1F5  402000           L     Q,Q,MR
1F6  047240           L     LOC,MDR               NEW LOC
1F7  C47C00           L     FLR,PSW,IR
                      *
                      *
```

```
                        ORG   '200'                                                    61609990
                  *                                                                    61610000
                  * DIVIDE                                                            61610010
                  *                                                                    61610020
            0200  DHR1  EQU   *                                                        61610030
200   047B00            LI    MAR,0       RESET REMAINDER FLAG ( +VE OR 0 )          61610040
201   07F900            INVI  MDR,0       SET QUOTIENT FLAG    ( -VE )               61610050
202   04742C            L     MR0,MR0,F   LOOK @ DIVISOR                             61610060
203   843A07            BT    L,MRONEG                                               61610070
204   A4362A            BF    G,OV1       IT IS ZERO                                 61610080
                  *                                                                    61610090
205   04F420      MR0POS TCMP   MR0,MR0     MAKE DIVISOR NEGATIVE                      61610100
206   047900            LI    MDR,0       RESET QUOTIENT FLAG                        61610110
                  *                                                                    61610120
            0207  MRONEG EQU   *                                                      61610130
207   0C300C            L     YD,YD,F     LOOK @ DIVIDEND                            61610140
208   A43A0D            BF    L,YDNNEG                                               61610150
                  *                       DIVIDEND IS NEGATIVE                       61610160
209   07FA52            INV   MAR,MAR,YDP1 SET REMAINDER FLAG  ( -VE )               61610170
20A   0D300A            TCMP  YD,YD,C0    COMPLEMENT LS PORTION OF  DIVIDEND         61610180
20B   07F843            INV   MDR,MDR,YDM1 INVERT QUOTIENT FLAG                      61610190
20C   0D3009            TCMP  YD,YD,CI    COMPLEMENT MS PORTION OF DIVIDEND          61610200
            020D  YDNNEG EQU   *                                                      61610210
20D   00502A            A     Q,YD,MR0,C0                                            61610220
20E   003002            L     Q,YDP1      (Q) = MS PORTION OF DIVIDEND               61610230
                  *                       YD NOW POINTS TO  R1+1                     61610240
20F   841E25            BT    C,OV        QUOTIENT TOO LARGE FOR 16 BITS             61610250
                  *                                                                    61610260
210   047426            L     MR0,MR0,M/D LOAD DIVISOR INTO M/D BOX                  61610270
211   047426            L     MR0,MR0,M/D                                            61610280
212   0C3006            L     YD,YD,M/D   LOAD LS PORTION OF DIVIDEND                61610290
213   0C3006            L     YD,YD,M/D                                              61610300
214   002006            L     Q,Q,M/D     LOAD MS PORTION OF DIVIDEND                61610310
215   002006            L     Q,Q,M/D                                                61610320
                  *                                                                    61610330
                  * DIVISION IS DONE BY THE M/D BOX ON THE I/O BUS                    61610340
                  *                                                                    61610350
216   007078            L     Q,IO        GET QUOTIENT                               61610360
217   047478            L     MR0,IO      GET REMAINDER                              61610370
                  *                                                                    61610380
218   047A5C            L     MAR,MAR,F   REMAINDER EXPECTED TO BE NEGATIVE ?        61610390
219   A43A1B            BF    L,RNNEG                                                61610400
21A   04F420            TCMP  MR0,MR0     YES, ADJUST REMAINDER                      61610410
            021B  RNNEG EQU   *                                                      61610420
21B   04784C            L     MDR,MDR,F   QUOTIENT EXPECTED TO BE POSITIVE ?         61610430
21C   843A22            BT    L,QNEG                                                 61610440
21D   00200C            L     Q,Q,F       YES, NOW LOOK @ THE QUOTIENT               61610450
21E   843A25            BT    L,OV        QUOTIENT > +32767                          61610460
                  *                                                                    61610470
21F   0C2003      QOK   L     YDM1,Q      (R1+1) = QUOTIENT                          61610480
220   0C7020            L     YD,MR0      (R1) = REMAINDER                           61610490
221   C47C00            L     FLR,PSW,IR                                             61610500
                  *                                                                    61610510
            0222  QNEG  EQU   *                                                      61610520
222   047D00            LI    FLR,0                                                  61610530
223   01200C            TCMP  Q,Q,F       COMPLEMENT THE QUOTIENT & EXAMINE          61610540
224   A4361F            BF    G,QOK       QUOTIENT OK                                61610550
```

```
                    *                                   QUOTIENT < -32768                   61610560
                    *                                                                       61610570
          0225      OV      EQU     *                   QUOTIENT OVERFLOW DETECTED          61610580
225 047A5C                  L       MAR,MAR,F                                               61610590
226 A43A2A                  BF      L,OV1               DIVIDEND IS NOT ALTERED             61610600
                    *                                                                       61610610
                    * RESTORE DIVIDEND TO ITS ORIGINAL VALUE. YD POINTS TO  R1+1           61610620
                    *                                                                       61610630
227 0D300A                  TCMP    YD,YD,C0                                                61610640
228 0C3003                  L       YDM1,YD             POINT TO R1                         61610650
229 0D3009                  TCMP    YD,YD,CI                                                61610660
                    *                                                                       61610670
22A 047B48          OV1     LI      MAR,'48'                                                61610680
22B 043400                  L       MR0,YD              SAVE YD IN MR0                      61610690
22C 1C7000                  L       YD,PSW,SL                                               61610700
22D 047703                  LI      CNTR,3              LOOK @ PSW03                        61610710
22E 1C300A                  L       YD,YD,SL+C0                                             61610720
22F 841DBD                  BT      C,QUEINT            DO PSW SWAP IF SET                  61610730
                    *                                                                       61610740
230 0C7020                  L       YD,MR0              RESTORE YD                          61610750
231 C47C00                  L       FLR,PSW,IR                                              61610760
                    *                                                                       61610770
                    *                                                                       61610780
                    * SIGNED MULTIPLY                                                      61610790
                    *                                                                       61610800
          0232      MHR1    EQU     *                                                       61610810
232 047B00                  LI      MAR,0               RESET FLAG                          61610820
233 0C3002                  L       YDP1,YD             BUMP YD FIELD                       61610830
234 0C300C                  L       YD,YD,F             LOOK @ MULTIPLICAND                 61610840
235 A43A38                  BF      L,NNEG1                                                 61610850
236 0D3000                  TCMP    YD,YD               NEGATIVE, COMPLEMENT IT.            61610860
237 07FB00                  INVI    MAR,0               SET FLAG                            61610870
238 04742C          NNEG1   L       MR0,MR0,F           LOOK @ MLLTIPLIER                   61610880
239 A43A3C                  BF      L,NNEG2                                                 61610890
23A 04F420                  TCMP    MR0,MR0             NEGATIVE, COMPLEMENT IT.            61610900
23B 07FA50                  INV     MAR,MAR             INVERT FLAG                         61610910
                    *                                                                       61610920
23C 0C3006          NNEG2   L       YD,YD,M/D           LOAD MULTIPLICAND INTO M/D BOX      61610930
23D 0C3006                  L       YD,YD,M/D                                               61610940
23E 047426                  L       MR0,MR0,M/D         LOAD MULTIPLIER                     61610950
23F 047426                  L       MR0,MR0,M/D                                             61610960
                    *                                                                       61610970
                    * MULTIPLICATION IS DONE BY THE M/D BOX ON THE I/O BUS                 61610980
                    *                                                                       61610990
240 0C7078                  L       YD,IO               (R1+1) = LS PORTION OF THE RESULT   61611000
241 007078                  L       Q,IO                GET MS PORTION OF RESULT            61611010
                    *                                                                       61611020
242 047A5C                  L       MAR,MAR,F           RESULT EXPECTED TO BE NEGATIVE ?    61611030
243 A43A4F                  BF      L,QOK1              NO, GO SET UP (R1) = MS PORTION     61611040
244 0D300A                  TCMP    YD,YD,C0            YES, COMPLEMENT IT                  61611050
245 0C3003                  L       YDM1,YD                                                 61611060
246 0D2009                  TCMP    YD,Q,CI             (R1) = MS PORTION OF THE RESULT     61611070
247 C47C00                  L       FLR,PSW,IR          FETCH NEXT USER INSTRUCTION         61611080
                    *                                                                       61611090
                    * UNSIGNED MULTIPLY                                                    61611100
                    *                                                                       61611110
          0248      MHUR1   EQU     *                                                       61611120
```

```
248  003002          L     Q,YDP1                                          61611130
249  0C3006          L     YD,YD,M/D          LOAD MULTIPLICAND INTO M/D BOX 61611140
24A  0C3006          L     YD,YD,M/D                                       61611150
24B  047426          L     MR0,MR0,M/D        LOAD MULTIPLIER              61611160
24C  047426          L     MR0,MR0,M/D                                     61611170
                                                                           61611180
                     *                                                     61611190
                     * MULTIPLICATION IS DONE BY THE M/D BOX ON THE I/O BUS 61611200
                     *                                                     61611210
24D  0C7078          L     YD,IO              (R1+1) = LS PORTION OF THE RESULT 61611220
24E  007078          L     Q,IO               GET MS PORTION OF THE RESULT  61611230
24F  047C03    GOK1  L     FLR,PSW,YDM1                                    61611240
250  CC2000          L     YD,Q,IR                                         61611250
251                  END
```

NO ERRORS

ACH	008E	
ADD	016E	14
ADDWRT	0164	13
AHM	007D	
AHR	008F	
AI	0004	
AIR	00D0	
AL	0005	
AL1	01DA	2
AL01	0147	12
AL02	014D	14
ALOC	0026	12, 13
ALX	01DC	18
APSW	0024	12, 13
BALR	0093	
BFCR	0098	
BFS	009C	
BKWORD	00A0	
BLKI01	00D9	4
BLKI02	00DA	10
BLKI03	00DD	10
BLKRR1	00D5	10
BRANCH	0094	7, 7
BTCR	0096	
BTS	009A	
BX	0012	
BX1	00A6	8
BXH	00A3	
BXLE	00A5	
BXNOB	00A8	8
BXNX	0014	2
CHR	008A	
CLB	00AD	
CLHR	008C	
CLRWT	0143	13, 14, 14
CONINT	019E	14
CONSER	0130	15, 17
CONTIN	0159	13
DHR	00E9	
DHR1	0200	11
DIFFER	007F	6
DISPLY	0175	14, 14, 16
DMARD	01B5	17, 17
DMAWRT	01B1	17
EPSR	00C4	
EPSR1	01CB	9
EPSR2	01D4	17
EPSR3	01D6	14
EXBR	00B9	
FINISH	01D8	10, 18
FN1	0185	
FN11	018B	15
FNREG	0150	13

FROMAL	00E5	18
FRWORD	00A1	
GENSWP	01BC	6, 16
HELP	0170	1
HELP1	0171	16
IDLE	011D	14, 15, 15
IDLE1	011F	12
IDLEX	012F	12, 16
ILEG	0082	
ILGPSW	0030	6
IMM	008D	
IOATN	0199	15
IODMA	01AB	16
IORR	00D1	
IORX	0005	
IOSVC	019D	
LB	00A9	
LBR	00AA	
LCS	0089	
LDREG	010A	12
LEADER	01E3	18, 18
LHR	0088	
LM	00BA	
LMNX	000E	2
LMSTM	000C	
LOCDIS	0115	12, 15, 15
LPSW	00C2	
LPSW1	01C7	9, 17
LSET	01C6	17
LSU3	0151	
MAR0	0117	15, 16
MHR	00EA	
MHR1	0232	11
MHUR	00E8	
MHUR1	0248	11
MMALF	01B9	15
MMALF1	01BB	14
MMF	0153	12
MRONEG	0207	19
MROPOS	0205	
NHR	0085	
NLONG	0067	11
NNEG1	0238	20
NNEG2	023C	20
NOB	0095	7, 9, 9
OC	0030	
OCR	0032	
OHR	0086	
OIPSW	0040	
OMMPSW	0038	17
OUTDIS	0118	15
OV	0225	19, 19
OV1	022A	19, 20
PNTR	0022	12, 13
POW	012D	13
PSWLOC	0189	15
PWRDWN	0121	17

PWRUP	0100	
QNEG	0222	19
QOK	021F	19
QOK1	024F	20
QUEINT	018D	17, 20
QUENBL	01CD	
RB1	00E7	10
RBR	00E4	
RBRWBR	00D3	
RBWB	0034	
RBWBNX	0038	3
RD	0018	
RD2	0019	3, 3, 6
RDKEY	0168	13
RDR	0025	3
REGDIS	018E	15
REGN	018F	16
RH	001D	
RHH	0020	3
RHR	0023	
RLLD2	005A	
RNNEG	021B	19
RRLD2	006B	
RS	0002	
RSNX	000A	1
RX	0006	
RXNX	0008	2
SAVREG	0129	13
SCH	0090	
SHIFT0	00EC	4
SHORTB	009D	7
SHR	0091	
SINT	00C8	
SINT1	01A0	9
SINT2	01A9	13
SLA	004D	
SLAD2	0074	
SLHA	0047	
SLHA1	0046	4
SLHAD2	005D	
SLHL	003D	
SLHL2	003E	4, 4
SLHL3	003F	4
SLHLD2	0051	
SLHLNX	0042	4
SLL	004F	
SLLID2	0056	5, 5, 5, 5, 11
SLLD2	0054	
SLLS	00CD	
SRAD2	006E	
SRHAD2	0061	
SRHL1	0065	5
SRHLD2	0064	
SRLID2	0069	5
SRLD2	0068	
SS	002B	
SSR	002E	

START	0000	
START1	0001	14
STB	00B1	
STBR	00B4	
STH	0079	
STH2	007B	8
STM	00BE	
SVC1	01EA	9
SVCD2	00CC	
TERMIN	01D9	10, 18
THI	0092	
THRUD2	0046	9
WAIT	0193	17
WAIT1	0196	16
WBR	00E1	
WD	001B	
WDR	0029	3
WHR	0027	
XHR	0087	
YDNNEG	020D	19

```
                 *
                 *
                 *
                 *
                 * COPYRIGHT INTERDATA INC.    OCTOBER, 1975
                 *
                 *
                 * OCTOBER 17, 1975
                 * DHEMA MAHAJAN
                 *
                 *
                 * DROM SOURCE IS ASSEMBLED IN CONJUNCTION WITH THE MICROPROGRAM SOURCE
                 * OPERAND FIELD IS THE SYMBOLIC ROM ENTRY POINT FOR 01
                 * COMMENT FIELD SHOWS OP-CODE AND VALID INSTRUCTION MNEMONIC
                 * ONLY THE LEAST SIGNIFICANT BYTE OF THE CODE GENERATED IS USED
                 * THE DROM DATA IS CONTAINED IN THE FOLLOWING ROM CHIP
                 *
                 *        19-186F09
                 *
                 *
                 *
000  0000 0082          DC     ILEG                    00
001  0000 0093          DC     BALR                    01   BALR
002  0000 0096          DC     BTCR                    02   BTCR
003  0000 0098          DC     BFCR                    03   BFCR
004  0000 0085          DC     NHR                     04   NHR
005  0000 008C          DC     CLHR                    05   CLHR
006  0000 0086          DC     OHR                     06   OHR
007  0000 0087          DC     XHR                     07   XHR
008  0000 0088          DC     LHR                     08   LHR
009  0000 008A          DC     CHR                     09   CHR
00A  0000 008F          DC     AHR                     0A   AHR
00B  0000 0091          DC     SHR                     0B   SHR
00C  0000 0082          DC     ILEG                    0C
00D  0000 0082          DC     ILEG                    0D
00E  0000 008E          DC     ACH                     0E   ACHR
00F  0000 0090          DC     SCH                     0F   SCHR
                 *
                 * OP-CODES  10 - 1F  ARE ILLEGAL
                 *
010  0000 0082          DC     ILEG
011  0000 0082          DC     ILEG
012  0000 0082          DC     ILEG
013  0000 0082          DC     ILEG
014  0000 0082          DC     ILEG
015  0000 0082          DC     ILEG
016  0000 0082          DC     ILEG
017  0000 0082          DC     ILEG
018  0000 0082          DC     ILEG
019  0000 0082          DC     ILEG
01A  0000 0082          DC     ILEG
01B  0000 0082          DC     ILEG
01C  0000 0082          DC     ILEG
01D  0000 0082          DC     ILEG
01E  0000 0082          DC     ILEG
01F  0000 0082          DC     ILEG
```

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```
020  0000 009A         DC    BTS               20  BTBS      D6160580
021  0000 009A         DC    BTS               21  BTFS      D6160590
022  0000 009C         DC    BFS               22  BFBS      D6160600
023  0000 009C         DC    BFS               23  BFFS      D6160610
024  0000 008D         DC    IMM               24  LIS       D6160620
025  0000 0089         DC    LCS               25  LCS       D6160630
026  0000 008D         DC    IMM               26  AIS       D6160640
027  0000 008D         DC    IMM               27  SIS       D6160650
028  0000 0082         DC    ILEG              28            D6160660
029  0000 0082         DC    ILEG              29            D6160670
02A  0000 0082         DC    ILEG              2A            D6160680
02B  0000 0082         DC    ILEG              2B            D6160690
02C  0000 0082         DC    ILEG              2C            D6160700
02D  0000 0082         DC    ILEG              2D            D6160710
02E  0000 0082         DC    ILEG              2E            D6160720
02F  0000 0082         DC    ILEG              2F            D6160730
                 *                                           D6160740
                 * OP-CODES  30 - 3F  ARE ILLEGAL            D6160750
                 *                                           D6160760
030  0000 0082         DC    ILEG                            D6160770
031  0000 0082         DC    ILEG                            D6160780
032  0000 0082         DC    ILEG                            D6160790
033  0000 0082         DC    ILEG                            D6160800
034  0000 0082         DC    ILEG                            D6160810
035  0000 0082         DC    ILEG                            D6160820
036  0000 0082         DC    ILEG                            D6160830
037  0000 0082         DC    ILEG                            D6160840
038  0000 0082         DC    ILEG                            D6160850
039  0000 0082         DC    ILEG                            D6160860
03A  0000 0082         DC    ILEG                            D6160870
03B  0000 0082         DC    ILEG                            D6160880
03C  0000 0082         DC    ILEG                            D6160890
03D  0000 0082         DC    ILEG                            D6160900
03E  0000 0082         DC    ILEG                            D6160910
03F  0000 0082         DC    ILEG                            D6160920
```

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```
                     *
                     * OP-CODES  80 - 8F  ARE ILLEGAL
                     *
080  0000 0082            DC      ILEG
081  0000 0082            DC      ILEG
082  0000 0082            DC      ILEG
083  0000 0082            DC      ILEG
084  0000 0082            DC      ILEG
085  0000 0082            DC      ILEG
086  0000 0082            DC      ILEG
087  0000 0082            DC      ILEG
088  0000 0082            DC      ILEG
089  0000 0082            DC      ILEG
08A  0000 0082            DC      ILEG
08B  0000 0082            DC      ILEG
08C  0000 0082            DC      ILEG
08D  0000 0082            DC      ILEG
08E  0000 0082            DC      ILEG
08F  0000 0082            DC      ILEG
                     *
                     *
090  0000 00C0            DC      SLLS                 90   SRLS
091  0000 00C0            DC      SLLS                 91   SLLS
092  0000 00B4            DC      STBR                 92   STBR
093  0000 00AA            DC      LBR                  93   LBR
094  0000 00B9            DC      EXBR                 94   EXBR
095  0000 00C4            DC      EPSR                 95   EPSR
096  0000 00D3            DC      RBRWBR               96   WBR
097  0000 00D3            DC      RBRWBR               97   RBR
098  0000 00D1            DC      IORR                 98   WHR
099  0000 00D1            DC      IORR                 99   RHR
09A  0000 00D1            DC      IORR                 9A   WDR
09B  0000 00D1            DC      IORR                 9B   RDR
09C  0000 0082            DC      ILEG                 9C
09D  0000 00D1            DC      IORR                 9D   SSR
09E  0000 00D1            DC      IORR                 9E   OCR
09F  0000 00D0            DC      AIR                  9F   AIR
```

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```
                        *                                                    D6162040
                        * OP-CODES  A0 - AF  ARE ILLEGAL                     D6162050
                        *                                                    D6162060
0A0  0000 0082              DC     ILEG                                      D6162070
0A1  0000 0082              DC     ILEG                                      D6162080
0A2  0000 0082              DC     ILEG                                      D6162090
0A3  0000 0082              DC     ILEG                                      D6162100
0A4  0000 0082              DC     ILEG                                      D6162110
0A5  0000 0082              DC     ILEG                                      D6162120
0A6  0000 0082              DC     ILEG                                      D6162130
0A7  0000 0082              DC     ILEG                                      D6162140
0A8  0000 0082              DC     ILEG                                      D6162150
0A9  0000 0082              DC     ILEG                                      D6162160
0AA  0000 0082              DC     ILEG                                      D6162170
0AB  0000 0082              DC     ILEG                                      D6162180
0AC  0000 0082              DC     ILEG                                      D6162190
0AD  0000 0082              DC     ILEG                                      D6162200
0AE  0000 0082              DC     ILEG                                      D6162210
0AF  0000 0082              DC     ILEG                                      D6162220
                        *                                                    D6162230
                        * OP-CODES  B0 - BF  ARE ILLEGAL                     D6162240
                        *                                                    D6162250
0B0  0000 0082              DC     ILEG                                      D6162260
0B1  0000 0082              DC     ILEG                                      D6162270
0B2  0000 0082              DC     ILEG                                      D6162280
0B3  0000 0082              DC     ILEG                                      D6162290
0B4  0000 0082              DC     ILEG                                      D6162300
0B5  0000 0082              DC     ILEG                                      D6162310
0B6  0000 0082              DC     ILEG                                      D6162320
0B7  0000 0082              DC     ILEG                                      D6162330
0B8  0000 0082              DC     ILEG                                      D6162340
0B9  0000 0082              DC     ILEG                                      D6162350
0BA  0000 0082              DC     ILEG                                      D6162360
0BB  0000 0082              DC     ILEG                                      D6162370
0BC  0000 0082              DC     ILEG                                      D6162380
0BD  0000 0082              DC     ILEG                                      D6162390
0BE  0000 0082              DC     ILEG                                      D6162400
0BF  0000 0082              DC     ILEG                                      D6162410
```

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```
0C0  0000 0012        DC    BX        C0  BXH          D6162430
0C1  0000 0012        DC    BX        C1  BXLE         D6162440
0C2  0000 0006        DC    RX        C2  LPSW         D6162450
0C3  0000 0002        DC    RS        C3  THI          D6162460
0C4  0000 0002        DC    RS        C4  MHI          D6162470
0C5  0000 0002        DC    RS        C5  CLHI         D6162480
0C6  0000 0002        DC    RS        C6  OHI          D6162490
0C7  0000 0002        DC    RS        C7  XHI          D6162500
0C8  0000 0002        DC    RS        C8  LHI          D6162510
0C9  0000 0002        DC    RS        C9  CHI          D6162520
0CA  0000 0002        DC    RS        CA  AHI          D6162530
0CB  0000 0002        DC    RS        CB  SHI          D6162540
0CC  0000 003D        DC    SLHL      CC  SRHL         D6162550
0CD  0000 003D        DC    SLHL      CD  SLHL         D6162560
0CE  0000 0047        DC    SLHA      CE  SRHA         D6162570
0CF  0000 0047        DC    SLHA      CF  SLHA         D6162580
                 *                                    D6162590
                 *                                    D6162600
0D0  0000 000C        DC    LMSTM     D0  STM          D6162610
0D1  0000 000C        DC    LMSTM     D1  LM           D6162620
0D2  0000 0006        DC    RX        D2  STB          D6162630
0D3  0000 0006        DC    RX        D3  LB           D6162640
0D4  0000 0006        DC    RX        D4  CLB          D6162650
0D5  0000 000B        DC    AL        D5  AL           D6162660
0D6  0000 0034        DC    RBWB      D6  WB           D6162670
0D7  0000 0034        DC    RBWB      D7  RB           D6162680
0D8  0000 0005        DC    IORX      D8  WH           D6162690
0D9  0000 0005        DC    IORX      D9  RH           D6162700
0DA  0000 0005        DC    IORX      DA  WD           D6162710
0DB  0000 0005        DC    IORX      DB  RD           D6162720
0DC  0000 0082        DC    ILEG      DC               D6162730
0DD  0000 0005        DC    IORX      DD  SS           D6162740
0DE  0000 0005        DC    IORX      DE  OC           D6162750
0DF  0000 0004        DC    AI        DF  AI           D6162760
```

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```
0E0  0000 0082          DC    ILEG                    E0                    D6162780
0E1  0000 0002          DC    RS                      E1  SVC               D6162790
0E2  0000 0002          DC    RS                      E2  SINT              D6162800
0E3  0000 0082          DC    ILEG                    E3                    D6162810
0E4  0000 0082          DC    ILEG                    E4                    D6162820
0E5  0000 0082          DC    ILEG                    E5                    D6162830
0E6  0000 0082          DC    ILEG                    E6                    D6162840
0E7  0000 0082          DC    ILEG                    E7                    D6162850
0E8  0000 0082          DC    ILEG                    E8                    D6162860
0E9  0000 0082          DC    ILEG                    E9                    D6162870
0EA  0000 004F          DC    SLL                     EA  RRL               D6162880
0EB  0000 004F          DC    SLL                     EB  RLL               D6162890
0EC  0000 004F          DC    SLL                     EC  SRL               D6162900
0ED  0000 004F          DC    SLL                     ED  SLL               D6162910
0EE  0000 004D          DC    SLA                     EE  SRA               D6162920
0EF  0000 004D          DC    SLA                     EF  SLA               D6162930
                        *                                                   D6162940
                        * OP-CODES  F0 - FF  ARE ILLEGAL                    D6162950
                        *                                                   D6162960
0F0  0000 0082          DC    ILEG                                          D6162970
0F1  0000 0082          DC    ILEG                                          D6162980
0F2  0000 0082          DC    ILEG                                          D6162990
0F3  0000 0082          DC    ILEG                                          D6163000
0F4  0000 0082          DC    ILEG                                          D6163010
0F5  0000 0082          DC    ILEG                                          D6163020
0F6  0000 0082          DC    ILEG                                          D6163030
0F7  0000 0082          DC    ILEG                                          D6163040
0F8  0000 0082          DC    ILEG                                          D6163050
0F9  0000 0082          DC    ILEG                                          D6163060
0FA  0000 0082          DC    ILEG                                          D6163070
0FB  0000 0082          DC    ILEG                                          D6163080
0FC  0000 0082          DC    ILEG                                          D6163090
0FD  0000 0082          DC    ILEG                                          D6163100
0FE  0000 0082          DC    ILEG                                          D6163110
0FF  0000 0082          DC    ILEG                                          D6163120
```

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```
                        *                                                       D6163140
                        *                                                       D6163150
                        *  DROM2 DATA FOLLOWS                                   D6163160
                        *                                                       D6163170
                        *                                                       D6163180
100  0000 0000              DC    0                    00                      D6163190
101  0000 0000              DC    0                    01  BALR                D6163200
102  0000 0000              DC    0                    02  BTCR                D6163210
103  0000 0000              DC    0                    03  BFCR                D6163220
104  0000 0000              DC    0                    04  NHR                 D6163230
105  0000 0000              DC    0                    05  CLHR                D6163240
106  0000 0000              DC    0                    06  OHR                 D6163250
107  0000 0000              DC    0                    07  XHR                 D6163260
108  0000 0000              DC    0                    08  LHR                 D6163270
109  0000 0000              DC    0                    09  CHR                 D6163280
10A  0000 0000              DC    0                    0A  AHR                 D6163290
10B  0000 0000              DC    0                    0B  SHR                 D6163300
10C  0000 0000              DC    0                    0C                      D6163310
10D  0000 0000              DC    0                    0D                      D6163320
10E  0000 0000              DC    0                    0E  ACHR                D6163330
10F  0000 0000              DC    0                    0F  SCHR                D6163340
                        *                                                       D6163350
                        * OP-CODES  10 - 1F  ARE ILLEGAL                       D6163360
                        *                                                       D6163370
110  0000 0000              DC    0                                            D6163380
111  0000 0000              DC    0                                            D6163390
112  0000 0000              DC    0                                            D6163400
113  0000 0000              DC    0                                            D6163410
114  0000 0000              DC    0                                            D6163420
115  0000 0000              DC    0                                            D6163430
116  0000 0000              DC    0                                            D6163440
117  0000 0000              DC    0                                            D6163450
118  0000 0000              DC    0                                            D6163460
119  0000 0000              DC    0                                            D6163470
11A  0000 0000              DC    0                                            D6163480
11B  0000 0000              DC    0                                            D6163490
11C  0000 0000              DC    0                                            D6163500
11D  0000 0000              DC    0                                            D6163510
11E  0000 0000              DC    0                                            D6163520
11F  0000 0000              DC    0                                            D6163530
```

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```
120  0000 00A0          DC     BKWORD          20  BTBS       D6163550
121  0000 00A1          DC     FRWORD          21  BTFS       D6163560
122  0000 00A0          DC     BKWORD          22  BFBS       D6163570
123  0000 00A1          DC     FRWORD          23  BFFS       D6163580
124  0000 0088          DC     LHP             24  LIS        D6163590
125  0000 0000          DC     0               25  LCS        D6163600
126  0000 008F          DC     AHR             26  AIS        D6163610
127  0000 0091          DC     SHR             27  SIS        D6163620
128  0000 0000          DC     0               28             D6163630
129  0000 0000          DC     0               29             D6163640
12A  0000 0000          DC     0               2A             D6163650
12B  0000 0000          DC     0               2B             D6163660
12C  0000 0000          DC     0               2C             D6163670
12D  0000 0000          DC     0               2D             D6163680
12E  0000 0000          DC     0               2E             D6163690
12F  0000 0000          DC     0               2F             D6163700
                  *                                           D6163710
                  * OP-CODES  30 - 3F  ARE ILLEGAL            D6163720
                  *                                           D6163730
130  0000 0000          DC     0                              D6163740
131  0000 0000          DC     0                              D6163750
132  0000 0000          DC     0                              D6163760
133  0000 0000          DC     0                              D6163770
134  0000 0000          DC     0                              D6163780
135  0000 0000          DC     0                              D6163790
136  0000 0000          DC     0                              D6163800
137  0000 0000          DC     0                              D6163810
138  0000 0000          DC     0                              D6163820
139  0000 0000          DC     0                              D6163830
13A  0000 0000          DC     0                              D6163840
13B  0000 0000          DC     0                              D6163850
13C  0000 0000          DC     0                              D6163860
13D  0000 0000          DC     0                              D6163870
13E  0000 0000          DC     0                              D6163880
13F  0000 0000          DC     0                              D6163890
```

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```
140  0000 0079          DC    STH                    40  STH          D6163910
141  0000 0093          DC    BALR                   41  BALR         D6163920
142  0000 0096          DC    BTCR                   42  BTCR         D6163930
143  0000 0098          DC    BFCR                   43  BFCR         D6163940
144  0000 0085          DC    NHR                    44  NH           D6163950
145  0000 008C          DC    CLHR                   45  CLH          D6163960
146  0000 0086          DC    OHR                    46  OH           D6163970
147  0000 0087          DC    XHR                    47  XH           D6163980
148  0000 0088          DC    LHR                    48  LH           D6163990
149  0000 008A          DC    CHR                    49  CH           D6164000
14A  0000 008F          DC    AHR                    4A  AH           D6164010
14B  0000 0091          DC    SHR                    4B  SH           D6164020
14C  0000 0000          DC    0                      4C               D6164030
14D  0000 0000          DC    0                      4D               D6164040
14E  0000 008E          DC    ACH                    4E  ACH          D6164050
14F  0000 0090          DC    SCH                    4F  SCH          D6164060
                   *                                                 D6164070
                   * OP-CODES  50 - 5F  ARE ILLEGAL                  D6164080
                   *                                                 D6164090
150  0000 0000          DC    0                                      D6164100
151  0000 0000          DC    0                                      D6164110
152  0000 0000          DC    0                                      D6164120
153  0000 0000          DC    0                                      D6164130
154  0000 0000          DC    0                                      D6164140
155  0000 0000          DC    0                                      D6164150
156  0000 0000          DC    0                                      D6164160
157  0000 0000          DC    0                                      D6164170
158  0000 0000          DC    0                                      D6164180
159  0000 0000          DC    0                                      D6164190
15A  0000 0000          DC    0                                      D6164200
15B  0000 0000          DC    0                                      D6164210
15C  0000 0000          DC    0                                      D6164220
15D  0000 0000          DC    0                                      D6164230
15E  0000 0000          DC    0                                      D6164240
15F  0000 0000          DC    0                                      D6164250
```

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```
160  0000 0000          DC    0                          60                    D6164270
161  0000 007D          DC    AHM                        61  AHM               D6164280
162  0000 0000          DC    0                          62                    D6164290
163  0000 0000          DC    0                          63                    D6164300
164  0000 0000          DC    0                          64                    D6164310
165  0000 0000          DC    0                          65                    D6164320
166  0000 0000          DC    0                          66                    D6164330
167  0000 0000          DC    0                          67                    D6164340
168  0000 0000          DC    0                          68                    D6164350
169  0000 0000          DC    0                          69                    D6164360
16A  0000 0000          DC    0                          6A                    D6164370
16B  0000 0000          DC    0                          6B                    D6164380
16C  0000 0000          DC    0                          6C                    D6164390
16D  0000 0000          DC    0                          6D                    D6164400
16E  0000 0000          DC    0                          6E                    D6164410
16F  0000 0000          DC    0                          6F                    D6164420
                   *                                                          D6164430
                   * OP-CODES  70 - 7F  ARE ILLEGAL                           D6164440
                   *                                                          D6164450
170  0000 0000          DC    0                                              D6164460
171  0000 0000          DC    0                                              D6164470
172  0000 0000          DC    0                                              D6164480
173  0000 0000          DC    0                                              D6164490
174  0000 0000          DC    0                                              D6164500
175  0000 0000          DC    0                                              D6164510
176  0000 0000          DC    0                                              D6164520
177  0000 0000          DC    0                                              D6164530
178  0000 0000          DC    0                                              D6164540
179  0000 0000          DC    0                                              D6164550
17A  0000 0000          DC    0                                              D6164560
17B  0000 0000          DC    0                                              D6164570
17C  0000 0000          DC    0                                              D6164580
17D  0000 0000          DC    0                                              D6164590
17E  0000 0000          DC    0                                              D6164600
17F  0000 0000          DC    0                                              D6164610
```

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```
                    *                                                                   D6164630
                    * OP-CODES  80 - 8F  ARE ILLEGAL                                   D6164640
                    *                                                                   D6164650
180  0000 0000            DC    0                                                      D6164660
181  0000 0000            DC    0                                                      D6164670
182  0000 0000            DC    0                                                      D6164680
183  0000 0000            DC    0                                                      D6164690
184  0000 0000            DC    0                                                      D6164700
185  0000 0000            DC    0                                                      D6164710
186  0000 0000            DC    0                                                      D6164720
187  0000 0000            DC    0                                                      D6164730
188  0000 0000            DC    0                                                      D6164740
189  0000 0000            DC    0                                                      D6164750
18A  0000 0000            DC    0                                                      D6164760
18B  0000 0000            DC    0                                                      D6164770
18C  0000 0000            DC    0                                                      D6164780
18D  0000 0000            DC    0                                                      D6164790
18E  0000 0000            DC    0                                                      D6164800
18F  0000 0000            DC    0                                                      D6164810
                    *                                                                   D6164820
                    *                                                                   D6164830
190  0000 0064            DC    SRHLD2          90  SRLS                               D6164840
191  0000 0051            DC    SLHLD2          91  SLLS                               D6164850
192  0000 0095            DC    NOB             92  STBR                               D6164860
193  0000 0000            DC    0               93  LBR                                D6164870
194  0000 0095            DC    NOB             94  EXBR                               D6164880
195  0000 0000            DC    0               95  EPSR                               D6164890
196  0000 00E1            DC    WBR             96  WBR                                D6164900
197  0000 00E4            DC    RBR             97  RBR                                D6164910
198  0000 0027            DC    WHR             98  WHR                                D6164920
199  0000 0023            DC    RHR             99  RHR                                D6164930
19A  0000 0029            DC    WDR             9A  WDR                                D6164940
19B  0000 0025            DC    RDR             9B  RDR                                D6164950
19C  0000 0000            DC    0               9C                                     D6164960
19D  0000 002E            DC    SSR             9D  SSR                                D6164970
19E  0000 0032            DC    OCR             9E  OCR                                D6164980
19F  0000 002E            DC    SSR             9F  AIR                                D6164990
```

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```
                        *                                                    D6165010
                        * OP-CODES  A0 - AF  ARE ILLEGAL                     D6165020
                        *                                                    D6165030
1A0  0000 0000            DC    0                                            D6165040
1A1  0000 0000            DC    0                                            D6165050
1A2  0000 0000            DC    0                                            D6165060
1A3  0000 0000            DC    0                                            D6165070
1A4  0000 0000            DC    0                                            D6165080
1A5  0000 0000            DC    0                                            D6165090
1A6  0000 0000            DC    0                                            D6165100
1A7  0000 0000            DC    0                                            D6165110
1A8  0000 0000            DC    0                                            D6165120
1A9  0000 0000            DC    0                                            D6165130
1AA  0000 0000            DC    0                                            D6165140
1AB  0000 0000            DC    0                                            D6165150
1AC  0000 0000            DC    0                                            D6165160
1AD  0000 0000            DC    0                                            D6165170
1AE  0000 0000            DC    0                                            D6165180
1AF  0000 0000            DC    0                                            D6165190
                        *                                                    D6165200
                        * OP-CODES  B0 - BF  ARE ILLEGAL                     D6165210
                        *                                                    D6165220
1B0  0000 0000            DC    0                                            D6165230
1B1  0000 0000            DC    0                                            D6165240
1B2  0000 0000            DC    0                                            D6165250
1B3  0000 0000            DC    0                                            D6165260
1B4  0000 0000            DC    0                                            D6165270
1B5  0000 0000            DC    0                                            D6165280
1B6  0000 0000            DC    0                                            D6165290
1B7  0000 0000            DC    0                                            D6165300
1B8  0000 0000            DC    0                                            D6165310
1B9  0000 0000            DC    0                                            D6165320
1BA  0000 0000            DC    0                                            D6165330
1BB  0000 0000            DC    0                                            D6165340
1BC  0000 0000            DC    0                                            D6165350
1BD  0000 0000            DC    0                                            D6165360
1BE  0000 0000            DC    0                                            D6165370
1BF  0000 0000            DC    0                                            D6165380
```

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```
1C0  0000 00A3        DC    BXH          C0  BXH          D6165400
1C1  0000 00A5        DC    BXLE         C1  BXLE         D6165410
1C2  0000 00C2        DC    LPSW         C2  LPSW         D6165420
1C3  0000 0092        DC    THI          C3  THI          D6165430
1C4  0000 0085        DC    NHR          C4  NHI          D6165440
1C5  0000 008C        DC    CLHR         C5  CLHI         D6165450
1C6  0000 0086        DC    OHR          C6  OHI          D6165460
1C7  0000 0087        DC    XHR          C7  XHI          D6165470
1C8  0000 0088        DC    LHR          C8  LHI          D6165480
1C9  0000 008A        DC    CHR          C9  CHI          D6165490
1CA  0000 008F        DC    AHR          CA  AHI          D6165500
1CB  0000 0091        DC    SHR          CB  SHI          D6165510
1CC  0000 0064        DC    SRHLD2       CC  SRHL         D6165520
1CD  0000 0051        DC    SLHLD2       CD  SLHL         D6165530
1CE  0000 0061        DC    SRHAD2       CE  SRHA         D6165540
1CF  0000 005D        DC    SLHAD2       CF  SLHA         D6165550
                 *                                       D6165560
                 *                                       D6165570
1D0  0000 00BE        DC    STM          D0  STM          D6165580
1D1  0000 00BA        DC    LM           D1  LM           D6165590
1D2  0000 00B1        DC    STB          D2  STB          D6165600
1D3  0000 00A9        DC    LB           D3  LB           D6165610
1D4  0000 00AD        DC    CLB          D4  CLB          D6165620
1D5  0000 00E4        DC    RBR          D5  AL           D6165630
1D6  0000 00E1        DC    WBR          D6  WB           D6165640
1D7  0000 00E4        DC    RBR          D7  RB           D6165650
1D8  0000 0027        DC    WHR          D8  WH           D6165660
1D9  0000 001D        DC    RH           D9  RH           D6165670
1DA  0000 001B        DC    WD           DA  WD           D6165680
1DB  0000 0018        DC    RD           DB  RD           D6165690
1DC  0000 0000        DC    0            DC               D6165700
1DD  0000 002B        DC    SS           DD  SS           D6165710
1DE  0000 0030        DC    CC           DE  CC           D6165720
1DF  0000 002B        DC    SS           DF  AI           D6165730
```

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```
1E0  0000 0000          DC    0              E0                     D6165750
1E1  0000 00CC          DC    SVCD2          E1   SVC               D6165760
1E2  0000 00C8          DC    SINT           E2   SINT              D6165770
1E3  0000 0000          DC    0              E3                     D6165780
1E4  0000 0000          DC    0              E4                     D6165790
1E5  0000 0000          DC    0              E5                     D6165800
1E6  0000 0000          DC    0              E6                     D6165810
1E7  0000 0000          DC    0              E7                     D6165820
1E8  0000 0000          DC    0              E8                     D6165830
1E9  0000 0000          DC    0              E9                     D6165840
1EA  0000 006B          DC    RRLD2          EA   RRL               D6165850
1EB  0000 005A          DC    RLLD2          EB   RLL               D6165860
1EC  0000 0068          DC    SRLD2          EC   SRL               D6165870
1ED  0000 0054          DC    SLLD2          ED   SLL               D6165880
1EE  0000 006E          DC    SRAD2          EE   SRA               D6165890
1EF  0000 0074          DC    SLAD2          EF   SLA               D6165900
               *                                                    D6165910
               * OP-CODES  F0 - FF  ARE ILLEGAL                     D6165920
               *                                                    D6165930
1F0  0000 0000          DC    0                                     D6165940
1F1  0000 0000          DC    0                                     D6165950
1F2  0000 0000          DC    0                                     D6165960
1F3  0000 0000          DC    0                                     D6165970
1F4  0000 0000          DC    0                                     D6165980
1F5  0000 0000          DC    0                                     D6165990
1F6  0000 0000          DC    0                                     D6166000
1F7  0000 0000          DC    0                                     D6166010
1F8  0000 0000          DC    0                                     D6166020
1F9  0000 0000          DC    0                                     D6166030
1FA  0000 0000          DC    0                                     D6166040
1FB  0000 0000          DC    0                                     D6166050
1FC  0000 0000          DC    0                                     D6166060
1FD  0000 0000          DC    0                                     D6166070
1FE  0000 0000          DC    0                                     D6166080
1FF  0000 0000          DC    0                                     D6166090
               *                                                    D6166100
200                     END                                         D6166110
```

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NO ERRORS

ACH	008E
ADD	016E
ADDWRT	0164
AHM	007D
AHR	008F
AI	0004
AIR	00D0
AL	000B
AL1	01DA
ALO1	0147
ALO2	014D
ALOC	0026
ALX	01DC
APSW	0024
BALR	0093
BFCR	0098
BFS	009C
BKWORD	00A0
BLKIO1	00D9
BLKIO2	00DA
BLKIO3	00DD
BLKRR1	00C5
BRANCH	0094
BTCR	0096
BTS	009A
BX	0012
BX1	00A6
BXH	00A3
BXLE	00A5
BXNOB	00A8
BXNX	0014
CHR	008A
CLB	00AD
CLHR	008C
CLRWT	0143
CONINT	019E
CONSER	0130
CONTIN	0159
DHR	00E9
DHR1	0200
DIFFER	007F
DISPLY	0175
DMARD	0185
DMAWRT	0181
EPSR	00C4
EPSR1	01CB
EPSR2	01D4
EPSR3	01D6
EXBR	00B9
FINISH	01D8
FN1	0185
FN11	018B
FNREG	015D

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```
FRGMAL  00E5
FRWORD  00A1
GENSWP  018C
HELP    0170
HELP1   0171
IDLE    011D
IDLE1   011F
IDLEX   012F
ILEG    0082
ILGPSW  0030
IMM     006D
IOATN   0199
IODMA   01AB
IORR    00D1
IOPX    0065
IOSVC   019D
LB      00A9
LBR     00AA
LCS     0089
LDREG   010A
LEADER  01E3
LHR     0084
LM      00BA
LMNX    000E
LMSTM   000C
LOCDIS  0115
LPSW    00C2
LPSW1   01C7
LSET    01C6
LSU3    0151
MAPG    0117
MHR     00EA
MHR1    0232
MHUR    00E6
MHUR1   0248
MMALF   0189
MMALF1  018B
MMF     0153
MRONEG  0207
MRPOS   0205
NHR     0085
NLONG   0067
NNEG1   0238
NNEG2   023C
NOP     0095
OC      0030
OCR     0032
OHR     0086
OIPSW   0040
OMMPSW  0038
OUTDIS  0118
OV      0225
OV1     022A
PNTR    0022
POW     012D
PSNLOC  0189
PWRDWN  0121
```

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PWRUP	0100
QNEG	0222
QOK	021F
QOK1	024F
QUEINT	016D
QUENBL	01CD
RB1	00E7
RBR	00E4
RBRWBR	0063
RBWB	0034
RBWBNX	0068
RD	0018
RD2	0019
RDKEY	0168
RDR	0025
REGDIS	018E
RESN	018F
RH	0010
RHH	0020
RHR	0023
RLLD2	005A
RNEG	021B
RRLD2	006B
RS	0002
RSNX	000A
RX	0006
RXNX	0008
SAVREG	0129
SCH	0090
SHIFTO	00EC
SHORTB	009D
SHR	0091
SINT	00C8
SINT1	01A0
SINT2	01A9
SLA	004D
SLAD2	0074
SLHA	0047
SLHA1	0048
SLHAD2	005D
SLHL	003D
SLHL2	003E
SLHL3	003F
SLHLD2	0051
SLHLNX	0042
SLL	004F
SLL1D2	0056
SLLD2	0054
SLLS	00CD
SRAD2	006E
SRHAD2	0061
SRHL1	0065
SRHLD2	0064
SRL1D2	0069
SRLD2	0068
SS	002B
SSR	002E

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START	0000
START1	0001
ST[illegible]	0081
STBR	0084
ST[illegible]	0079
ST[illegible]2	007B
ST[illegible]	00BE
SVC1	01EA
SVC02	00CC
TE[illegible]IN	01D9
TH1	0092
THR002	0046
WAIT	0193
WAIT1	0196
WB[illegible]	00E1
WD	01B
WD[illegible]	0029
WHR	0027
XHR	0087
YONNEG	020D

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```
                          *                                                                      D6160010
                          *                                                                      D6160020
                          *                                                                      D6160030
                          *                                                                      D6160040
                          * COPYRIGHT INTERDATA INC.   OCTOBER, 1975                             D6160050
                          *                                                                      D6160060
                          *                                                                      D6160070
                          * OCTOBER 17, 1975                                                     D6160080
                          * DHEMA MAHAJAN                                                        D6160090
                          *                                                                      D6160100
                          *                                                                      D6160110
                          * DROM SOURCE IS ASSEMBLED IN CONJUNCTION WITH THE MICROPROGRAM SOURCE D6160120
                          * OPERAND FIELD IS THE SYMBOLIC ROM ENTRY POINT FOR 01                 D6160130
                          * COMMENT FIELD SHOWS OP-CODE AND VALID INSTRUCTION MNEMONIC           D6160140
                          * ONLY THE LEAST SIGNIFICANT BYTE OF THE CODE GENERATED IS USED        D6160150
                          * THE DROM DATA IS CONTAINED IN THE FOLLOWING ROM CHIP                 D6160160
                          *                                                                      D6160170
                          *        19-186F01                                                     D6160180
                          *                                                                      D6160190
                          *                                                                      D6160200
                          *                                                                      D6160210
000    0000 0082                 DC      ILEG                       00                           D6160220
001    0000 0093                 DC      BALR                       01   BALR                    D6160230
002    0000 0096                 DC      BTCR                       02   BTCR                    D6160240
003    0000 0098                 DC      BFCR                       03   BFCR                    D6160250
004    0000 0085                 DC      NHR                        04   NHR                     D6160260
005    0000 008C                 DC      CLHR                       05   CLHR                    D6160270
006    0000 0086                 DC      OHR                        06   OHR                     D6160280
007    0000 0087                 DC      XHR                        07   XHR                     D6160290
008    0000 0088                 DC      LHR                        08   LHR                     D6160300
009    0000 008A                 DC      CHR                        09   CHR                     D6160310
00A    0000 008F                 DC      AHR                        0A   AHR                     D6160320
00B    0000 0091                 DC      SHR                        0B   SHR                     D6160330
00C    0000 00EA                 DC      MHR                        0C   MHR                     D6160340
00D    0000 00E9                 DC      DHR                        0D   DHR                     D6160350
00E    0000 008E                 DC      ACH                        0E   ACHR                    D6160360
00F    0000 0090                 DC      SCH                        0F   SCHR                    D6160370
                          *                                                                      D6160380
                          * OP-CODES  10 - 1F  ARE ILLEGAL                                       D6160390
                          *                                                                      D6160400
010    0000 0082                 DC      ILEG                                                    D6160410
011    0000 0082                 DC      ILEG                                                    D6160420
012    0000 0082                 DC      ILEG                                                    D6160430
013    0000 0082                 DC      ILEG                                                    D6160440
014    0000 0082                 DC      ILEG                                                    D6160450
015    0000 0082                 DC      ILEG                                                    D6160460
016    0000 0082                 DC      ILEG                                                    D6160470
017    0000 0082                 DC      ILEG                                                    D6160480
018    0000 0082                 DC      ILEG                                                    D6160490
019    0000 0082                 DC      ILEG                                                    D6160500
01A    0000 0082                 DC      ILEG                                                    D6160510
01B    0000 0082                 DC      ILEG                                                    D6160520
01C    0000 0082                 DC      ILEG                                                    D6160530
01D    0000 0082                 DC      ILEG                                                    D6160540
01E    0000 0082                 DC      ILEG                                                    D6160550
01F    0000 0082                 DC      ILEG                                                    D6160560
```

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```
020  0000 009A          DC    BTS                20  BTBS            D6160580
021  0000 009A          DC    BTS                21  BTFS            D6160590
022  0000 009C          DC    BFS                22  BFBS            D6160600
023  0000 009C          DC    BFS                23  BFFS            D6160610
024  0000 008D          DC    IMM                24  LIS             D6160620
025  0000 0089          DC    LCS                25  LCS             D6160630
026  0000 008D          DC    IMM                26  AIS             D6160640
027  0000 008D          DC    IMM                27  SIS             D6160650
028  0000 0082          DC    ILEG               28                  D6160660
029  0000 0082          DC    ILEG               29                  D6160670
02A  0000 0082          DC    ILEG               2A                  D6160680
02B  0000 0082          DC    ILEG               2B                  D6160690
02C  0000 0082          DC    ILEG               2C                  D6160700
02D  0000 0082          DC    ILEG               2D                  D6160710
02E  0000 0082          DC    ILEG               2E                  D6160720
02F  0000 0082          DC    ILEG               2F                  D6160730
                  *                                                  D6160740
                  * OP-CODES  30 - 3F  ARE ILLEGAL                   D6160750
                  *                                                  D6160760
030  0000 0082          DC    ILEG                                   D6160770
031  0000 0082          DC    ILEG                                   D6160780
032  0000 0082          DC    ILEG                                   D6160790
033  0000 0082          DC    ILEG                                   D6160800
034  0000 0082          DC    ILEG                                   D6160810
035  0000 0082          DC    ILEG                                   D6160820
036  0000 0082          DC    ILEG                                   D6160830
037  0000 0082          DC    ILEG                                   D6160840
038  0000 0082          DC    ILEG                                   D6160850
039  0000 0082          DC    ILEG                                   D6160860
03A  0000 0082          DC    ILEG                                   D6160870
03B  0000 0082          DC    ILEG                                   D6160880
03C  0000 0082          DC    ILEG                                   D6160890
03D  0000 0082          DC    ILEG                                   D6160900
03E  0000 0082          DC    ILEG                                   D6160910
03F  0000 0082          DC    ILEG                                   D6160920
```

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```
040  0000 0002          DC    RS                40  STH     D6160940
041  0000 0002          DC    RS                41  BAL     D6160950
042  0000 0002          DC    RS                42  BTC     D6160960
043  0000 0002          DC    RS                43  BFC     D6160970
044  0000 0006          DC    RX                44  NH      D6160980
045  0000 0006          DC    RX                45  CLH     D6160990
046  0000 0006          DC    RX                46  OH      D6161000
047  0000 0006          DC    RX                47  XH      D6161010
048  0000 0006          DC    RX                48  LH      D6161020
049  0000 0006          DC    RX                49  CH      D6161030
04A  0000 0006          DC    RX                4A  AH      D6161040
04B  0000 0006          DC    RX                4B  SH      D6161050
04C  0000 0006          DC    RX                4C  MH      D6161060
04D  0000 0006          DC    RX                4D  DH      D6161070
04E  0000 0006          DC    RX                4E  ACH     D6161080
04F  0000 0006          DC    RX                4F  SCH     D6161090
                   *                                       D6161100
                   * OP-CODES  50 - 5F  ARE ILLEGAL        D6161110
                   *                                       D6161120
050  0000 0082          DC    ILEG                          D6161130
051  0000 0082          DC    ILEG                          D6161140
052  0000 0082          DC    ILEG                          D6161150
053  0000 0082          DC    ILEG                          D6161160
054  0000 0082          DC    ILEG                          D6161170
055  0000 0082          DC    ILEG                          D6161180
056  0000 0082          DC    ILEG                          D6161190
057  0000 0082          DC    ILEG                          D6161200
058  0000 0082          DC    ILEG                          D6161210
059  0000 0082          DC    ILEG                          D6161220
05A  0000 0082          DC    ILEG                          D6161230
05B  0000 0082          DC    ILEG                          D6161240
05C  0000 0082          DC    ILEG                          D6161250
05D  0000 0082          DC    ILEG                          D6161260
05E  0000 0082          DC    ILEG                          D6161270
05F  0000 0082          DC    ILEG                          D6161280
```

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```
060  0000 0082         DC    ILEG                   60                          D6161300
061  0000 0006         DC    RX                     61   AHM                    D6161310
062  0000 0082         DC    ILEG                   62                          D6161320
063  0000 0082         DC    ILEG                   63                          D6161330
064  0000 0082         DC    ILEG                   64                          D6161340
065  0000 0082         DC    ILEG                   65                          D6161350
066  0000 0082         DC    ILEG                   66                          D6161360
067  0000 0082         DC    ILEG                   67                          D6161370
068  0000 0082         DC    ILEG                   68                          D6161380
069  0000 0082         DC    ILEG                   69                          D6161390
06A  0000 0082         DC    ILEG                   6A                          D6161400
06B  0000 0082         DC    ILEG                   6B                          D6161410
06C  0000 0082         DC    ILEG                   6C                          D6161420
06D  0000 0082         DC    ILEG                   6D                          D6161430
06E  0000 0082         DC    ILEG                   6E                          D6161440
06F  0000 0082         DC    ILEG                   6F                          D6161450
                *                                                               D6161460
                * OP-CODES  70 - 7F  ARE ILLEGAL                                D6161470
                *                                                               D6161480
070  0000 0082         DC    ILEG                                               D6161490
071  0000 0082         DC    ILEG                                               D6161500
072  0000 0082         DC    ILEG                                               D6161510
073  0000 0082         DC    ILEG                                               D6161520
074  0000 0082         DC    ILEG                                               D6161530
075  0000 0082         DC    ILEG                                               D6161540
076  0000 0082         DC    ILEG                                               D6161550
077  0000 0082         DC    ILEG                                               D6161560
078  0000 0082         DC    ILEG                                               D6161570
079  0000 0082         DC    ILEG                                               D6161580
07A  0000 0082         DC    ILEG                                               D6161590
07B  0000 0082         DC    ILEG                                               D6161600
07C  0000 0082         DC    ILEG                                               D6161610
07D  0000 0082         DC    ILEG                                               D6161620
07E  0000 0082         DC    ILEG                                               D6161630
07F  0000 0082         DC    ILEG                                               D6161640
```

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```
                    *                                                                   D6161660
                    * OP-CODES  80 - 8F  ARE ILLEGAL                                   D6161670
                    *                                                                   D6161680
080  0000 0082           DC    ILEG                                                     D6161690
081  0000 0082           DC    ILEG                                                     D6161700
082  0000 0082           DC    ILEG                                                     D6161710
083  0000 0082           DC    ILEG                                                     D6161720
084  0000 0082           DC    ILEG                                                     D6161730
085  0000 0082           DC    ILEG                                                     D6161740
086  0000 0082           DC    ILEG                                                     D6161750
087  0000 0082           DC    ILEG                                                     D6161760
088  0000 0082           DC    ILEG                                                     D6161770
089  0000 0082           DC    ILEG                                                     D6161780
08A  0000 0082           DC    ILEG                                                     D6161790
08B  0000 0082           DC    ILEG                                                     D6161800
08C  0000 0082           DC    ILEG                                                     D6161810
08D  0000 0082           DC    ILEG                                                     D6161820
08E  0000 0082           DC    ILEG                                                     D6161830
08F  0000 0082           DC    ILEG                                                     D6161840
                    *                                                                   D6161850
                    *                                                                   D6161860
090  0000 00CD           DC    SLLS                 90  SRLS                            D6161870
091  0000 00CD           DC    SLLS                 91  SLLS                            D6161880
092  0000 00B4           DC    STBR                 92  STBR                            D6161890
093  0000 00AA           DC    LBR                  93  LBR                             D6161900
094  0000 00B9           DC    EXBR                 94  EXBR                            D6161910
095  0000 00C4           DC    EPSR                 95  EPSR                            D6161920
096  0000 00D3           DC    RBRWBR               96  WBR                             D6161930
097  0000 00D3           DC    RBRWBR               97  RBR                             D6161940
098  0000 00D1           DC    IORR                 98  WHR                             D6161950
099  0000 00D1           DC    IORR                 99  RHR                             D6161960
09A  0000 00D1           DC    IORR                 9A  WDR                             D6161970
09B  0000 00D1           DC    IORR                 9B  RDR                             D6161980
09C  0000 00EB           DC    MHUR                 9C  MHUR                            D6161990
09D  0000 00D1           DC    IORR                 9D  SSR                             D6162000
09E  0000 00D1           DC    IORR                 9E  OCR                             D6162010
09F  0000 00D0           DC    AIR                  9F  AIR                             D6162020
```

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```
                        *                                                    D6162040
                        * OP-CODES  A0 - AF  ARE ILLEGAL                     D6162050
                        *                                                    D6162060
0A0  0000 0082          DC    ILEG                                           D6162070
0A1  0000 0082          DC    ILEG                                           D6162080
0A2  0000 0082          DC    ILEG                                           D6162090
0A3  0000 0082          DC    ILEG                                           D6162100
0A4  0000 0082          DC    ILEG                                           D6162110
0A5  0000 0082          DC    ILEG                                           D6162120
0A6  0000 0082          DC    ILEG                                           D6162130
0A7  0000 0082          DC    ILEG                                           D6162140
0A8  0000 0082          DC    ILEG                                           D6162150
0A9  0000 0082          DC    ILEG                                           D6162160
0AA  0000 0082          DC    ILEG                                           D6162170
0AB  0000 0082          DC    ILEG                                           D6162180
0AC  0000 0082          DC    ILEG                                           D6162190
0AD  0000 0082          DC    ILEG                                           D6162200
0AE  0000 0082          DC    ILEG                                           D6162210
0AF  0000 0082          DC    ILEG                                           D6162220
                        *                                                    D6162230
                        * OP-CODES  B0 - BF  ARE ILLEGAL                     D6162240
                        *                                                    D6162250
0B0  0000 0082          DC    ILEG                                           D6162260
0B1  0000 0082          DC    ILEG                                           D6162270
0B2  0000 0082          DC    ILEG                                           D6162280
0B3  0000 0082          DC    ILEG                                           D6162290
0B4  0000 0082          DC    ILEG                                           D6162300
0B5  0000 0082          DC    ILEG                                           D6162310
0B6  0000 0082          DC    ILEG                                           D6162320
0B7  0000 0082          DC    ILEG                                           D6162330
0B8  0000 0082          DC    ILEG                                           D6162340
0B9  0000 0082          DC    ILEG                                           D6162350
0BA  0000 0082          DC    ILEG                                           D6162360
0BB  0000 0082          DC    ILEG                                           D6162370
0BC  0000 0082          DC    ILEG                                           D6162380
0BD  0000 0082          DC    ILEG                                           D6162390
0BE  0000 0082          DC    ILEG                                           D6162400
0BF  0000 0082          DC    ILEG                                           D6162410
```

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```
0C0  0000 0012        DC    BX          C0  BXH          D6162430
0C1  0000 0012        DC    BX          C1  BXLE         D6162440
0C2  0000 0006        DC    RX          C2  LPSW         D6162450
0C3  0000 0002        DC    RS          C3  THI          D6162460
0C4  0000 0002        DC    RS          C4  NHI          D6162470
0C5  0000 0002        DC    RS          C5  CLHI         D6162480
0C6  0000 0002        DC    RS          C6  OHI          D6162490
0C7  0000 0002        DC    RS          C7  XHI          D6162500
0C8  0000 0002        DC    RS          C8  LHI          D6162510
0C9  0000 0002        DC    RS          C9  CHI          D6162520
0CA  0000 0002        DC    RS          CA  AHI          D6162530
0CB  0000 0002        DC    RS          CB  SHI          D6162540
0CC  0000 003D        DC    SLHL        CC  SRHL         D6162550
0CD  0000 003D        DC    SLHL        CD  SLHL         D6162560
0CE  0000 0047        DC    SLHA        CE  SRHA         D6162570
0CF  0000 0047        DC    SLHA        CF  SLHA         D6162580
                  *                                      D6162590
                  *                                      D6162600
0D0  0000 000C        DC    LMSTM       D0  STM          D6162610
0D1  0000 000C        DC    LMSTM       D1  LM           D6162620
0D2  0000 0006        DC    RX          D2  STB          D6162630
0D3  0000 0006        DC    RX          D3  LB           D6162640
0D4  0000 0006        DC    RX          D4  CLB          D6162650
0D5  0000 000B        DC    AL          D5  AL           D6162660
0D6  0000 0034        DC    RBWB        D6  WB           D6162670
0D7  0000 0034        DC    RBWB        D7  RB           D6162680
0D8  0000 0005        DC    IORX        D8  WH           D6162690
0D9  0000 0005        DC    IORX        D9  RH           D6162700
0DA  0000 0005        DC    IORX        DA  WD           D6162710
0DB  0000 0005        DC    IORX        DB  RD           D6162720
0DC  0000 0006        DC    RX          DC  MHU          D6162730
0DD  0000 0005        DC    IORX        DD  SS           D6162740
0DE  0000 0005        DC    IORX        DE  DC           D6162750
0DF  0000 0004        DC    AI          DF  AI           D6162760
```

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```
0E0  0000 0082        DC    ILEG           E0              D6162780
0E1  0000 0002        DC    RS             E1   SVC        D6162790
0E2  0000 0002        DC    RS             E2   SINT       D6162800
0E3  0000 0082        DC    ILEG           E3              D6162810
0E4  0000 0082        DC    ILEG           E4              D6162820
0E5  0000 0082        DC    ILEG           E5              D6162830
0E6  0000 0082        DC    ILEG           E6              D6162840
0E7  0000 0082        DC    ILEG           E7              D6162850
0E8  0000 0082        DC    ILEG           E8              D6162860
0E9  0000 0082        DC    ILEG           E9              D6162870
0EA  0000 004F        DC    SLL            EA   RRL        D6162880
0EB  0000 004F        DC    SLL            EB   RLL        D6162890
0EC  0000 004F        DC    SLL            EC   SRL        D6162900
0ED  0000 004F        DC    SLL            ED   SLL        D6162910
0EE  0000 004D        DC    SLA            EE   SRA        D6162920
0EF  0000 004D        DC    SLA            EF   SLA        D6162930
               *                                           D6162940
               * OP-CODES  F0 - FF  ARE ILLEGAL            D6162950
               *                                           D6162960
0F0  0000 0082        DC    ILEG                           D6162970
0F1  0000 0082        DC    ILEG                           D6162980
0F2  0000 0082        DC    ILEG                           D6162990
0F3  0000 0082        DC    ILEG                           D6163000
0F4  0000 0082        DC    ILEG                           D6163010
0F5  0000 0082        DC    ILEG                           D6163020
0F6  0000 0082        DC    ILEG                           D6163030
0F7  0000 0082        DC    ILEG                           D6163040
0F8  0000 0082        DC    ILEG                           D6163050
0F9  0000 0082        DC    ILEG                           D6163060
0FA  0000 0082        DC    ILEG                           D6163070
0FB  0000 0082        DC    ILEG                           D6163080
0FC  0000 0082        DC    ILEG                           D6163090
0FD  0000 0082        DC    ILEG                           D6163100
0FE  0000 0082        DC    ILEG                           D6163110
0FF  0000 0082        DC    ILEG                           D6163120
```

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```
                        *                                                       D6163140
                        *                                                       D6163150
                        *  DROM2 DATA FOLLOWS                                   D6163160
                        *                                                       D6163170
                        *                                                       D6163180
100  0000 0000              DC    0                        00                   D6163190
101  0000 0000              DC    0                        01  BALR             D6163200
102  0000 0000              DC    0                        02  BTCR             D6163210
103  0000 0000              DC    0                        03  BFCR             D6163220
104  0000 0000              DC    0                        04  MHR              D6163230
105  0000 0000              DC    0                        05  CLHR             D6163240
106  0000 0000              DC    0                        06  OHR              D6163250
107  0000 0000              DC    0                        07  XHR              D6163260
108  0000 0000              DC    0                        08  LHR              D6163270
109  0000 0000              DC    0                        09  CHR              D6163280
10A  0000 0000              DC    0                        0A  AHR              D6163290
10B  0000 0000              DC    0                        0B  SHR              D6163300
10C  0000 0000              DC    0                        0C  MHR              D6163310
10D  0000 0000              DC    0                        0D  DHR              D6163320
10E  0000 0000              DC    0                        0E  ACHR             D6163330
10F  0000 0000              DC    0                        0F  SCHR             D6163340
                        *                                                       D6163350
                        * OP-CODES  10 - 1F  ARE ILLEGAL                       D6163360
                        *                                                       D6163370
110  0000 0000              DC    0                                            D6163380
111  0000 0000              DC    0                                            D6163390
112  0000 0000              DC    0                                            D6163400
113  0000 0000              DC    0                                            D6163410
114  0000 0000              DC    0                                            D6163420
115  0000 0000              DC    0                                            D6163430
116  0000 0000              DC    0                                            D6163440
117  0000 0000              DC    0                                            D6163450
118  0000 0000              DC    0                                            D6163460
119  0000 0000              DC    0                                            D6163470
11A  0000 0000              DC    0                                            D6163480
11B  0000 0000              DC    0                                            D6163490
11C  0000 0000              DC    0                                            D6163500
11D  0000 0000              DC    0                                            D6163510
11E  0000 0000              DC    0                                            D6163520
11F  0000 0000              DC    0                                            D6163530
```

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```
120  0000 00A0          DC    BKWORD              20  BTBS          D6163550
121  0000 00A1          DC    FRWORD              21  BTFS          D6163560
122  0000 00A0          DC    BKWORD              22  BFBS          D6163570
123  0000 00A1          DC    FRWORD              23  BFFS          D6163580
124  0000 0088          DC    LHR                 24  LIS           D6163590
125  0000 0000          DC    0                   25  LCS           D6163600
126  0000 008F          DC    AHR                 26  AIS           D6163610
127  0000 0091          DC    SHR                 27  SIS           D6163620
128  0000 0000          DC    0                   28                D6163630
129  0000 0000          DC    0                   29                D6163640
12A  0000 0000          DC    0                   2A                D6163650
12B  0000 0000          DC    0                   2B                D6163660
12C  0000 0000          DC    0                   2C                D6163670
12D  0000 0000          DC    0                   2D                D6163680
12E  0000 0000          DC    0                   2E                D6163690
12F  0000 0000          DC    0                   2F                D6163700
                    *                                               D6163710
                    * OP-CODES  30 - 3F  ARE ILLEGAL                D6163720
                    *                                               D6163730
130  0000 0000          DC    0                                     D6163740
131  0000 0000          DC    0                                     D6163750
132  0000 0000          DC    0                                     D6163760
133  0000 0000          DC    0                                     D6163770
134  0000 0000          DC    0                                     D6163780
135  0000 0000          DC    0                                     D6163790
136  0000 0000          DC    0                                     D6163800
137  0000 0000          DC    0                                     D6163810
138  0000 0000          DC    0                                     D6163820
139  0000 0000          DC    0                                     D6163830
13A  0000 0000          DC    0                                     D6163840
13B  0000 0000          DC    0                                     D6163850
13C  0000 0000          DC    0                                     D6163860
13D  0000 0000          DC    0                                     D6163870
13E  0000 0000          DC    0                                     D6163880
13F  0000 0000          DC    0                                     D6163890
```

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```
140  0000 0079          DC    STH                  40  STH          D6163910
141  0000 0093          DC    BALR                 41  BALR         D6163920
142  0000 0096          DC    BTCR                 42  BTCR         D6163930
143  0000 0098          DC    BFCR                 43  BFCR         D6163940
144  0000 0085          DC    NHR                  44  NH           D6163950
145  0000 008C          DC    CLHR                 45  CLH          D6163960
146  0000 0086          DC    OHR                  46  OH           D6163970
147  0000 0087          DC    XHR                  47  XH           D6163980
148  0000 0088          DC    LHR                  48  LH           D6163990
149  0000 008A          DC    CHR                  49  CH           D6164000
14A  0000 008F          DC    AHR                  4A  AH           D6164010
14B  0000 0091          DC    SHR                  4B  SH           D6164020
14C  0000 00EA          DC    MHR                  4C  MH           D6164030
14D  0000 00E9          DC    DHR                  4D  DH           D6164040
14E  0000 008E          DC    ACH                  4E  ACH          D6164050
14F  0000 0090          DC    SCH                  4F  SCH          D6164060
                   *                                               D6164070
                   * OP-CODES  50 - 5F  ARE ILLEGAL                 D6164080
                   *                                               D6164090
150  0000 0000          DC    0                                    D6164100
151  0000 0000          DC    0                                    D6164110
152  0000 0000          DC    0                                    D6164120
153  0000 0000          DC    0                                    D6164130
154  0000 0000          DC    0                                    D6164140
155  0000 0000          DC    0                                    D6164150
156  0000 0000          DC    0                                    D6164160
157  0000 0000          DC    0                                    D6164170
158  0000 0000          DC    0                                    D6164180
159  0000 0000          DC    0                                    D6164190
15A  0000 0000          DC    0                                    D6164200
15B  0000 0000          DC    0                                    D6164210
15C  0000 0000          DC    0                                    D6164220
15D  0000 0000          DC    0                                    D6164230
15E  0000 0000          DC    0                                    D6164240
15F  0000 0000          DC    0                                    D6164250
```

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```
160  0000 0000          DC    0                          60                    D6164270
161  0000 007D          DC    AHM                        61  AHM               D6164280
162  0000 0000          DC    0                          62                    D6164290
163  0000 0000          DC    0                          63                    D6164300
164  0000 0000          DC    0                          64                    D6164310
165  0000 0000          DC    0                          65                    D6164320
166  0000 0000          DC    0                          66                    D6164330
167  0000 0000          DC    0                          67                    D6164340
168  0000 0000          DC    0                          68                    D6164350
169  0000 0000          DC    0                          69                    D6164360
16A  0000 0000          DC    0                          6A                    D6164370
16B  0000 0000          DC    0                          6B                    D6164380
16C  0000 0000          DC    0                          6C                    D6164390
16D  0000 0000          DC    0                          6D                    D6164400
16E  0000 0000          DC    0                          6E                    D6164410
16F  0000 0000          DC    0                          6F                    D6164420
                   *                                                          D6164430
                   * OP-CODES  70 - 7F  ARE ILLEGAL                           D6164440
                   *                                                          D6164450
170  0000 0000          DC    0                                              D6164460
171  0000 0000          DC    0                                              D6164470
172  0000 0000          DC    0                                              D6164480
173  0000 0000          DC    0                                              D6164490
174  0000 0000          DC    0                                              D6164500
175  0000 0000          DC    0                                              D6164510
176  0000 0000          DC    0                                              D6164520
177  0000 0000          DC    0                                              D6164530
178  0000 0000          DC    0                                              D6164540
179  0000 0000          DC    0                                              D6164550
17A  0000 0000          DC    0                                              D6164560
17B  0000 0000          DC    0                                              D6164570
17C  0000 0000          DC    0                                              D6164580
17D  0000 0000          DC    0                                              D6164590
17E  0000 0000          DC    0                                              D6164600
17F  0000 0000          DC    0                                              D6164610
```

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```
                    *                                                                D6164630
                    * OP-CODES  80 - 8F  ARE ILLEGAL                                 D6164640
                    *                                                                D6164650
180  0000 0000            DC    0                                                    D6164660
181  0000 0000            DC    0                                                    D6164670
182  0000 0000            DC    0                                                    D6164680
183  0000 0000            DC    0                                                    D6164690
184  0000 0000            DC    0                                                    D6164700
185  0000 0000            DC    0                                                    D6164710
186  0000 0000            DC    0                                                    D6164720
187  0000 0000            DC    0                                                    D6164730
188  0000 0000            DC    0                                                    D6164740
189  0000 0000            DC    0                                                    D6164750
18A  0000 0000            DC    0                                                    D6164760
18B  0000 0000            DC    0                                                    D6164770
18C  0000 0000            DC    0                                                    D6164780
18D  0000 0000            DC    0                                                    D6164790
18E  0000 0000            DC    0                                                    D6164800
18F  0000 0000            DC    0                                                    D6164810
                    *                                                                D6164820
                    *                                                                D6164830
190  0000 0064            DC    SRHLD2             90   SRLS                         D6164840
191  0000 0051            DC    SLHLD2             91   SLLS                         D6164850
192  0000 0095            DC    NOB                92   STBR                         D6164860
193  0000 0000            DC    0                  93   LBR                          D6164870
194  0000 0095            DC    NOB                94   EXBR                         D6164880
195  0000 0000            DC    0                  95   EPSR                         D6164890
196  0000 00E1            DC    WBR                96   WBR                          D6164900
197  0000 00E4            DC    RBR                97   RBR                          D6164910
198  0000 0027            DC    WHR                98   WHR                          D6164920
199  0000 0023            DC    RHR                99   RHR                          D6164930
19A  0000 0029            DC    WDR                9A   WDR                          D6164940
19B  0000 0025            DC    RDR                9B   RDR                          D6164950
19C  0000 0000            DC    0                  9C   MHUR                         D6164960
19D  0000 002E            DC    SSR                9D   SSR                          D6164970
19E  0000 0032            DC    OCR                9E   OCR                          D6164980
19F  0000 002E            DC    SSR                9F   AIR                          D6164990
```

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```
                        *                                                    D6165010
                        * OP-CODES  A0 - AF  ARE ILLEGAL                     D6165020
                        *                                                    D6165030
1A0  0000 0000            DC    0                                            D6165040
1A1  0000 0000            DC    0                                            D6165050
1A2  0000 0000            DC    0                                            D6165060
1A3  0000 0000            DC    0                                            D6165070
1A4  0000 0000            DC    0                                            D6165080
1A5  0000 0000            DC    0                                            D6165090
1A6  0000 0000            DC    0                                            D6165100
1A7  0000 0000            DC    0                                            D6165110
1A8  0000 0000            DC    0                                            D6165120
1A9  0000 0000            DC    0                                            D6165130
1AA  0000 0000            DC    0                                            D6165140
1AB  0000 0000            DC    0                                            D6165150
1AC  0000 0000            DC    0                                            D6165160
1AD  0000 0000            DC    0                                            D6165170
1AE  0000 0000            DC    0                                            D6165180
1AF  0000 0000            DC    0                                            D6165190
                        *                                                    D6165200
                        * OP-CODES  B0 - BF  ARE ILLEGAL                     D6165210
                        *                                                    D6165220
1B0  0000 0000            DC    0                                            D6165230
1B1  0000 0000            DC    0                                            D6165240
1B2  0000 0000            DC    0                                            D6165250
1B3  0000 0000            DC    0                                            D6165260
1B4  0000 0000            DC    0                                            D6165270
1B5  0000 0000            DC    0                                            D6165280
1B6  0000 0000            DC    0                                            D6165290
1B7  0000 0000            DC    0                                            D6165300
1B8  0000 0000            DC    0                                            D6165310
1B9  0000 0000            DC    0                                            D6165320
1BA  0000 0000            DC    0                                            D6165330
1BB  0000 0000            DC    0                                            D6165340
1BC  0000 0000            DC    0                                            D6165350
1BD  0000 0000            DC    0                                            D6165360
1BE  0000 0000            DC    0                                            D6165370
1BF  0000 0000            DC    0                                            D6165380
```

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```
1C0  0000 00A3        DC    BXH                C0  BXH          D6165400
1C1  0000 00A5        DC    BXLE               C1  BXLE         D6165410
1C2  0000 00C2        DC    LPSW               C2  LPSW         D6165420
1C3  0000 0092        DC    THI                C3  THI          D6165430
1C4  0000 0085        DC    NHR                C4  NHI          D6165440
1C5  0000 008C        DC    CLHR               C5  CLHI         D6165450
1C6  0000 0086        DC    OHR                C6  OHI          D6165460
1C7  0000 0087        DC    XHR                C7  XHI          D6165470
1C8  0000 0088        DC    LHR                C8  LHI          D6165480
1C9  0000 008A        DC    CHR                C9  CHI          D6165490
1CA  0000 008F        DC    AHR                CA  AHI          D6165500
1CB  0000 0091        DC    SHR                CB  SHI          D6165510
1CC  0000 0064        DC    SRHLD2             CC  SRHL         D6165520
1CD  0000 0051        DC    SLHLD2             CD  SLHL         D6165530
1CE  0000 0061        DC    SRHAD2             CE  SRHA         D6165540
1CF  0000 005D        DC    SLHAD2             CF  SLHA         D6165550
                *                                               D6165560
                *                                               D6165570
1D0  0000 00BE        DC    STM                D0  STM          D6165580
1D1  0000 00BA        DC    LM                 D1  LM           D6165590
1D2  0000 00B1        DC    STB                D2  STB          D6165600
1D3  0000 00A9        DC    LB                 D3  LB           D6165610
1D4  0000 00AD        DC    CLB                D4  CLB          D6165620
1D5  0000 00E4        DC    RBR                D5  AL           D6165630
1D6  0000 00E1        DC    WBR                D6  WB           D6165640
1D7  0000 00E4        DC    RBR                D7  RB           D6165650
1D8  0000 0027        DC    WHR                D8  WH           D6165660
1D9  0000 001D        DC    RH                 D9  RH           D6165670
1DA  0000 001B        DC    WD                 DA  WD           D6165680
1DB  0000 0018        DC    RD                 DB  RD           D6165690
1DC  0000 00EB        DC    MHUR               DC  MHU          D6165700
1DD  0000 002B        DC    SS                 DD  SS           D6165710
1DE  0000 0030        DC    OC                 DE  OC           D6165720
1DF  0000 002B        DC    SS                 DF  AI           D6165730
```

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```
1E0  0000 0000          DC    0                E0              D6165750
1E1  0000 00CC          DC    SVCD2            E1   SVC        D6165760
1E2  0000 00C8          DC    SINT             E2   SINT       D6165770
1E3  0000 0000          DC    0                E3              D6165780
1E4  0000 0000          DC    0                E4              D6165790
1E5  0000 0000          DC    0                E5              D6165800
1E6  0000 0000          DC    0                E6              D6165810
1E7  0000 0000          DC    0                E7              D6165820
1E8  0000 0000          DC    0                E8              D6165830
1E9  0000 0000          DC    0                E9              D6165840
1EA  0000 006B          DC    RRLD2            EA   RRL        D6165850
1EB  0000 005A          DC    RLLD2            EB   RLL        D6165860
1EC  0000 0068          DC    SRLD2            EC   SRL        D6165870
1ED  0000 0054          DC    SLLD2            ED   SLL        D6165880
1EE  0000 006E          DC    SRAD2            EE   SRA        D6165890
1EF  0000 0074          DC    SLAD2            EF   SLA        D6165900
                   *                                           D6165910
                   * OP-CODES  F0 - FF  ARE ILLEGAL            D6165920
                   *                                           D6165930
1F0  0000 0000          DC    0                                D6165940
1F1  0000 0000          DC    0                                D6165950
1F2  0000 0000          DC    0                                D6165960
1F3  0000 0000          DC    0                                D6165970
1F4  0000 0000          DC    0                                D6165980
1F5  0000 0000          DC    0                                D6165990
1F6  0000 0000          DC    0                                D6166000
1F7  0000 0000          DC    0                                D6166010
1F8  0000 0000          DC    0                                D6166020
1F9  0000 0000          DC    0                                D6166030
1FA  0000 0000          DC    0                                D6166040
1FB  0000 0000          DC    0                                D6166050
1FC  0000 0000          DC    0                                D6166060
1FD  0000 0000          DC    0                                D6166070
1FE  0000 0000          DC    0                                D6166080
1FF  0000 0000          DC    0                                D6166090
                   *                                           D6166100
200                     END                                    D6166110
```

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NO ERRORS

ACH	008E
ADD	016E
ADDWRT	0164
AHM	007D
AHR	008F
AI	0004
AIR	00D0
AL	000B
AL1	01DA
ALQ1	0147
ALQ2	014D
ALQC	0026
ALX	01DC
APSW	0024
BALR	0093
BFCR	0098
BFS	009C
BKWORD	00A0
BLKIO1	00D9
BLKIO2	00DA
BLKIO3	00DD
BLKRR1	00D5
BRANCH	0094
BTCR	0096
BTS	009A
BX	0012
BX1	00A6
BXH	00A3
BXLE	00A5
BXNOB	00A8
BXNX	0014
CHR	008A
CLB	00AD
CLHR	008C
CLRWT	0143
CONINT	019E
CONSER	0130
CONTIN	0159
DHR	00E9
DHR1	0200
DIFFER	007F
DISPLY	0175
DMARD	01B5
DMAWRT	01B1
EPSR	00C4
EPSR1	01CB
EPSR2	01D4
EPSR3	01D6
EXBR	00B9
FINISH	01D8
FN1	0185
FN11	018B
FNREG	015D

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FROMAL	00E5
FRWORD	00A1
GENSWP	013C
HELP	0170
HELP1	0171
IDLE	011D
IDLE1	011F
IDLEX	012F
ILEG	0082
ILGPSW	0030
IMM	008D
IOATN	0199
IODMA	01AB
IORR	00D1
IORX	0005
IOSVC	019D
LB	00A9
LBR	00AA
LCS	0089
LDREG	010A
LEADER	01E3
LHR	0088
LM	00BA
LMNX	000E
LMSTM	000C
LOCDIS	0115
LPSW	00C2
LPSW1	01C7
LSET	01C6
LSU3	0151
MAR0	0117
MHR	00EA
MHR1	0232
MHUR	00EB
MHUR1	0248
MMALF	0189
MMALF1	01B8
MMF	0153
MRONEG	0207
MRUPOS	0205
NHR	0085
NLONG	0067
NNEG1	0238
NNEG2	023C
NOB	0095
OC	0030
OCR	0032
OHR	0086
OIPSW	0040
OMMPSW	0038
OUTDIS	0118
OV	0225
OV1	022A
PNTR	0022
POW	012D
PSWLOC	0189
PWRDWN	0121

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PWRUP	0100
QNEG	0222
QOK	021F
QOK1	024F
QUEINT	01BD
QUENBL	01CD
RB1	00E7
RBR	00E4
RBRWBR	00D3
RBWB	0034
RBWBNX	0038
RD	0018
RD2	0019
RDKEY	0168
RDR	0025
REGDIS	018E
REGN	018F
RH	001D
RHH	0020
RHR	0023
RLLD2	005A
RNNEG	0218
RRLD2	006B
RS	0002
RSNX	000A
RX	0006
RXNX	0008
SAVREG	0129
SCR	0090
SHIFTU	00EC
SHORTB	009D
SHR	0091
SINT	00C8
SINT1	01A0
SINT2	01A9
SLA	004D
SLAD2	0074
SLHA	0047
SLHA1	0048
SLHAD2	005D
SLHL	003D
SLHL2	003E
SLHL3	003F
SLHLD2	0051
SLHLNX	0042
SLL	004F
SLL1D2	0056
SLLD2	0054
SLLS	00CD
SRAD2	006E
SRHAD2	0061
SRHL1	0065
SRHLD2	0064
SRL1D2	0069
SRLD2	0068
SS	002B
SSR	002E

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START	0000
START1	0001
STR	00B1
STRR	00B4
STH	0079
STH2	007B
STM	00BE
SVC1	01EA
SVCD2	00CC
TERMIN	01D9
THI	0092
THRUD2	0046
WAIT	0193
WAIT1	0196
WBR	00E1
WD	001B
WDR	0029
WHR	0027
XHR	0087
YDNNEG	020D

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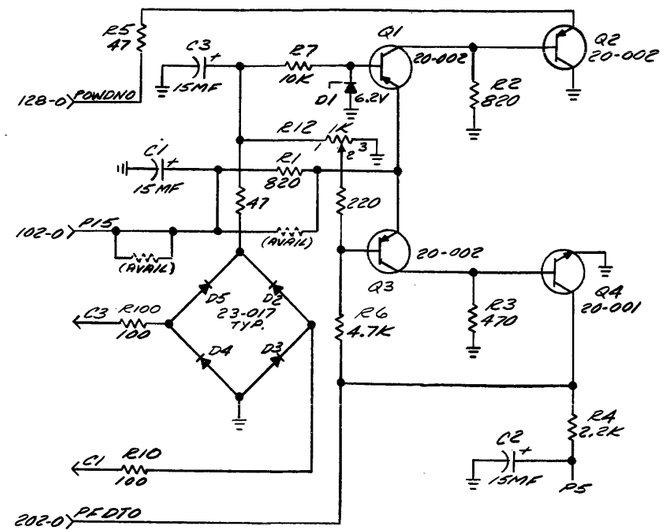

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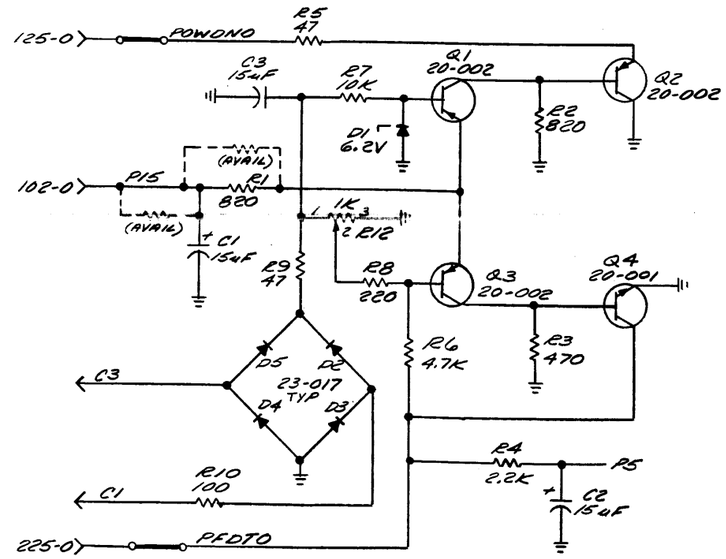

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TOLERANCE: .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	P.EDWARDS	DRAFT	1-19-75
	R.CERO	CHK	
	D.FRANKENBERGER	ENGR	
	R. BARKER	Q.C.	
	S.MESSINA	M&P.	

TITLE: PRIMARY POWER FAIL

DWG. NO. 03145 REV. NO. 35-448 C08 SHEET 1—

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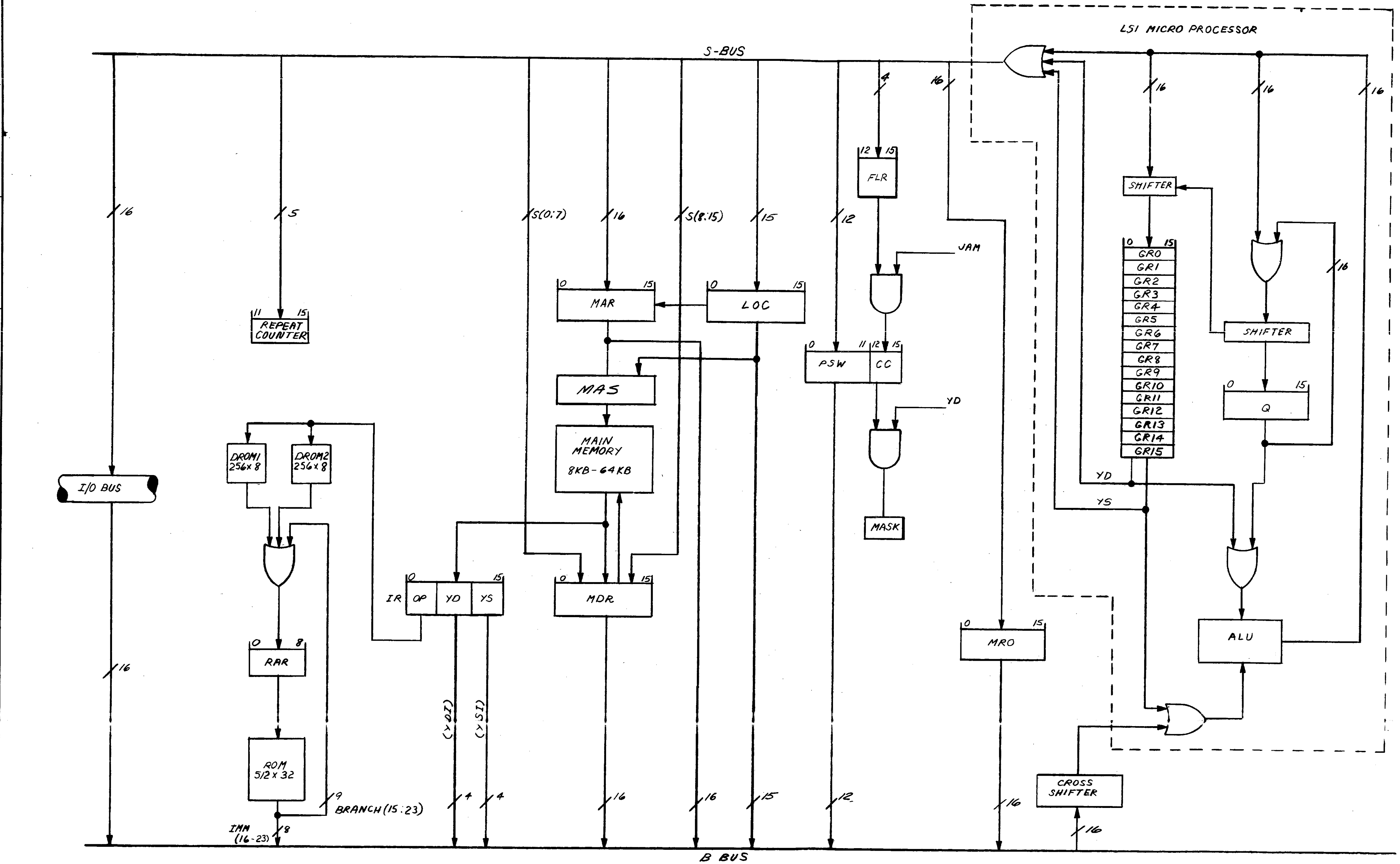
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS					
PRE PRODUCTION APPROVAL	DEV INIT DJF DATE 11/21/75				
SHTS 2,4,5,11,13 & 17 WERE SPEC AS REV LEVEL R00. REV LEVEL OF BOTH BOARDS WERE R00 RESP.					
02 P	DJF	ECR 01945-3	JB	12-11-75	R01
RELEASED FOR PRODUCTION ENG. DJF DATE 12-16-75					



MODEL 6/16 BLOCK DIAGRAM

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION.

6/16 CPU W/O M-D	35-604 F01 R01
6/16 CPU W/M-D	35-604 F02 R01

NOTE:
THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

SHEET INDEX																				
REV LEVEL	01	01		01	01						01		01				01		
SHEET NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19

NOTE:
ALL COMPONENTS ON THIS SCHEMATIC LOCATED ON 35-604.

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SCALE–	NAME	TITLE	DATE
TOLERANCE .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	B. SCHAIBLE	DRAFT	11-4-75
	R. CERO	CHK	11-21-75
	D. FRANKENBERGER	ENGR	12-16-75
	B. MULLER		12-16-75
	S. MESSINA	MGR	12-16-75

TITLE FUNCTIONAL SCHEMATIC 6/16 CPU PROCESSOR

TASK NO. 03145
DWG. NO. 01-094 R01 D08
SHEET 1 OF 19

BACK PANEL MAP

CONN. 1

TITLE	CPU		MEM I/O		MPY-DIV I/O		I/O		I/O		I/O		I/O		I/O	
BD. LOC.	07		06		05		04		03		02		01		00	
TERM. NO. / ROW	1	2	1	2	1	2	1	2	1	2	1	2	1	2	1	2
41	P5	GND	P5	GND	P5	GND	P5	GND							P5	GND
40	GND	GND	GND	GND	GND	GND	GND	GND							GND	GND
39	P15/P12	P15/P12	P15/P12	P15/P12	P15/P12	P15/P12	P15/P12	P15/P12							P15/P12	P15/P12
38	N15	N15	N15	N15	N15	N15	N15	N15							N15	N15
37	MDS150	MDS160	MDS150	MDS160	MDS150	MDS160	MDS150	MDS160							MDS150	MDS160
36	MDS130	MDS140	MDS130	MDS140	MDS130	MDS140	MDS130	MDS140							MDS130	MDS140
35	MDS110	MDS120	MDS110	MDS120	MDS110	MDS120	MDS110	MDS120							MDS110	MDS120
34	MDS090	MDS100	MDS090	MDS100	MDS090	MDS100	MDS090	MDS100							MDS090	MDS100
33	MDS070	MDS080	MDS070	MDS080	MDS070	MDS080	MDS070	MDS080							MDS070	MDS080
32	MDS050	MDS060	MDS050	MDS060	MDS050	MDS060	MDS050	MDS060							MDS050	MDS060
31	MDS030	MDS040	MDS030	MDS040	MDS030	MDS040	MDS030	MDS040							MDS030	MDS040
30	MDS010	MDS020	MDS010	MDS020	MDS010	MDS020	MDS010	MDS020							MDS010	MDS020
29		MDS000		MDS000		MDS000		MDS000								MDS000
28	LDREGO	M/DO	TEMPA		LOREGO	M/DO										
27	WTO	BCLKO	WRTO	TEMPB		BCLKO										
26	SCLROA	HWO	SCLROA	HWO	SCLRO	HWO	SCLRO	HWO							SCLRO	HWO
25	PERRO	GLRO	PERRO													
24	GND	GND			EXSTPO											
23	SYNO	ATNO	SYNO	ATNO	SYNO	ATNO	SYNO	ATNO							SYNO	ATNO
22	EXSTPO				RACKO	TACKO	RACKO	TACKO							RACKO	TACKO
21	GDATO	DAO	CL070	DAO	CL070	DAO	CL070	DAO							CL070	DAO
20	DISOSCO	CMDO	DRO	CMDO	DRO	CMDO	DRO	CMDO							DRO	CMDO
19	SRO	ADRSO	SRO	ADRSO	SRO	ADRSO	SRO	ADRSO							SRO	ADRSO
18			D140	D150	D140	D150	D140	D150							D140	D150
17			D120	D130	D120	D130	D120	D130							D120	D130
16			D100	D110	D100	D110	D100	D110							D100	D110
15			D080	D090	D080	D090	D080	D090							D080	D090
14			D060	D070	D060	D070	D060	D070							D060	D070
13			D040	D050	D040	D050	D040	D050							D040	D050
12			D020	D030	D020	D030	D020	D030							D020	D030
11			D000	D010	D000	D010	D00	D010							D000	D010
10	WRTOA	MDS000	WRTOA	MDS000	WRTOA	MDS000	WRTOA	MDS000							WRTOA	MDS000
09	MDS010	MDS020	MDS010	MDS020	MDS010	MDS020	MDS010	MDS020							MDS010	MDS020
08	MDS030	MDS040	MDS030	MDS040	MDS030	MDS040	MDS030	MDS040							MDS030	MDS040
07	MDS050	MDS060	MDS050	MDS060	MDS050	MDS060	MDS050	MDS060							MDS050	MDS060
06	MDS070	MDS080	MDS070	MDS080	MDS070	MDS080	MDS070	MDS080							MDS070	MDS080
05	MDS090	MDS100	MDS090	MDS100	MDS090	MDS100	MDS090	MDS100							MDS090	MDS100
04	MDS110	MDS120	MDS110	MDS120	MDS110	MDS120	MDS110	MDS120							MDS110	MDS120
03	MDS130	MDS140	MDS130	MDS140	MDS130	MDS140	MDS130	MDS140							MDS130	MDS140
02	MDS150	MDS160	MDS150	MDS160	MDS150	MDS160	MDS150	MDS160							MDS150	MDS160
01	GND	GND	GND	GND	GND	GND	GND	GND							GND	GND
00	P5	GND	P5	GND	P5	GND	P5	GND							P5	GND

CONN. 0

TERM. NO. / ROW	07-1	07-2	06-1	06-2	05-1	05-2	04-1	04-2	03-1	03-2	02-1	02-2	01-1	01-2	00-1	00-2
41	P5	GND	P5	GND	P5	GND	P5	GND							P5	GND
40	GND	GND	GND	GND	GND	GND	GND	GND							GND	GND
39	P15/P12	REQO	P15/P12	REQO	P15/P12	REQO	P15/P12	REQO							P15/P12	REQO
38	N15	ENO	N15	ENO	N15	ENO	N15	ENO							N15	ENO
37				TACO	ACTO	TACO	ACTO	TACO							ACTO	TACO
36	SINGLO	CATNO			INITO											
35	EXBYSO	EXDUAO	EXDUAO	EXBSYO	CATNO	SINGLO										
34					FWAITI										XRACKO	
33	MA130	MA140	MA130	MA140	MA130	MA140	MA130	MA140							MA130	MA140
32	MA110	MA120	MA110	MA120	MA110	MA120	MA110	MA120							MA110	MA120
31	MA090	MA100	MA090	MA100	MA090	MA100	MA090	MA100							MA090	MA100
30	MA070	MA080	MA070	MA080	MA070	MA080	MA070	MA080							MA070	MA080
29	MA050	MA060	MA050	MA060	MA050	MA060	MA050	MA060							MA050	MA060
28																
27	DMATNO		DMATNO		DMATNO		DMATNO								DMATNO	
26		HWO	SCLRO	HWO	SCLRO	HWO	SCLRO	HWO							SCLRO	HWO
25																
24																
23	SYNO	ATNO	SYNO	ATNO	SYNO	ATNO	SYNO	ATNO							SYNO	ATNO
22		ACKO	RACKO	TACKO	RACKO	TACKO	RACKO	TACKO							RACKO	TACKO
21		DAO	CL070	DAO	CL070	DAO	CL070	DAO							CL070	DAO
20	DRO	CMDO	DRO	CMDO	DRO	CMDO	DRO	CMDO							DRO	CMDO
19	SRO	ADRS	SRO	ADRSO	SRO	ADRSO	SRO	ADRSO							SRO	ADRSO
18	DB140	DB150	D140	D150	D140	D150	D140	D150							D140	D150
17	DB120	DB130	D120	D130	D120	D130	D120	D130							D120	D130
16	DB100	DB110	D100	D110	D100	D110	D100	D110							D100	D110
15	DB080	DB090	D080	D090	D080	D090	D080	D090							D080	D090
14	DB060	DB070	D060	D070	D060	D070	D060	D070							D060	D070
13	DB040	DB050	D040	D050	D040	D050	D040	D050							D040	D050
12	DB020	DB030	D020	D030	D020	D030	D020	D030							D020	D030
11	DB000	DB010	D000	D010	D000	D010	D000	D010							D000	D010
10	MA030	MA040	MA030	MA040	MA030	MA040	MA030	MA040							MA030	MA040
09	MA020		MA020	MA021	MA020	MA021	MA020	MA021							MA020	MA021
08																
07	MA010		MA010		MA010		MA010								MA010	
06	MA000		MA000		MA000		MA000								MA000	
05																
04	INHO	ERO	INHO	ERO	INHO	ERO	INHO	ERO							INHO	ERO
03																
02	P15/P12	PFDTO	P15/P12	N15	P15/P12	N15	P15/P12	N15							P15/P12	N15
01	GND	GND	GND	GND	GND	GND	GND	GND							GND	GND
00	P6	GND	P5	GND	P5	GND	P5	GND							P5	GND

NOTES

UPD	DF	03145-3	MB	12-11-75	R01

REVISIONS

SLOT 05 122-1 WAS EXSTPO 124-1 WAS NOT SPECIFIED SLOT 06 122-1 WAS RACKO, 222-1 WAS TACKO, SLOT 07 222-1 WAS TACKO

NAME	TITLE	DATE
V. PERRI	DRAFT	11-12-75
R. CERO	CHK	
I. LEMAIR	ENGR	
R.A. BARKER	Q.C.	
D. FRANKENBERGER	DIR ENG	

TITLE FUNCTIONAL SCHEMATIC 6/16 CPU PROCESSOR

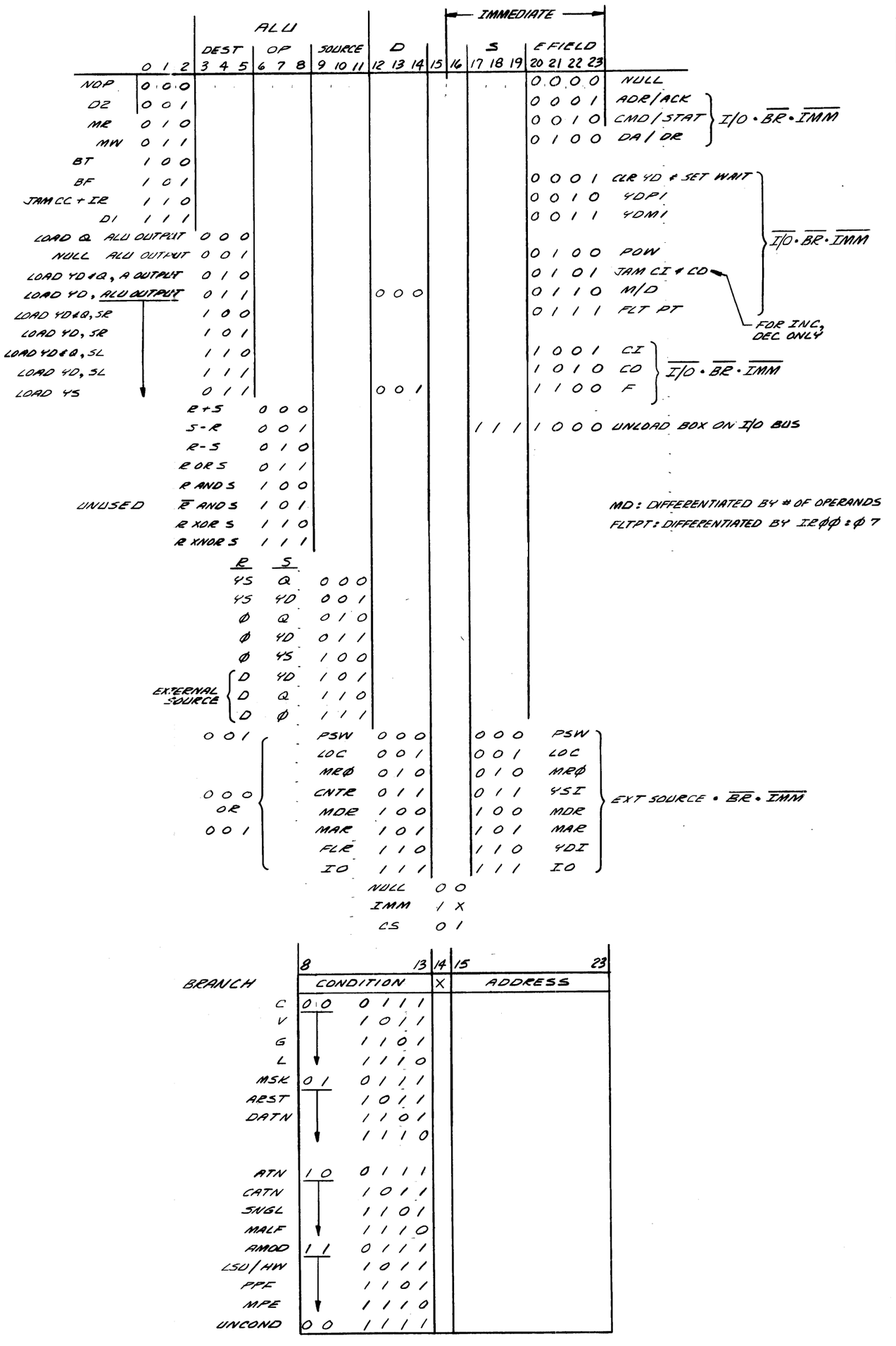
TASK NO. 03145

DWG NO. 01-094 R01D08

SHEET 2-19

INTERDATA®

BRUNING 44-231 24838



BRANCH

	8 9 10 11 12 13 CONDITION	14 X	15 16 17 18 19 20 21 22 23 ADDRESS
C	0 0 0 1 1 1		
V	1 0 1 1		
G	1 1 0 1		
L	1 1 1 0		
MSK	0 1 0 1 1 1		
AEST	1 0 1 1		
DATN	1 1 0 1		
	1 1 1 0		
ATN	1 0 0 1 1 1		
CATN	1 0 1 1		
SNGL	1 1 0 1		
MALF	1 1 1 0		
AMOD	1 1 0 1 1 1		
LSU/HW	1 0 1 1		
PPF	1 1 0 1		
MPE	1 1 1 0		
UNCOND	0 0 1 1 1 1		

LSU: ADDRESSED ON POWER UP
KNOCKED DOWN WHEN OTHER
DEV. ADDRESSED

SCALE—
NAME
DRAFT
CHK
ENGR
TITLE
DATE
SIZE 03745
DWG NO. 01-0994
REV
SHEET 3 OF 19

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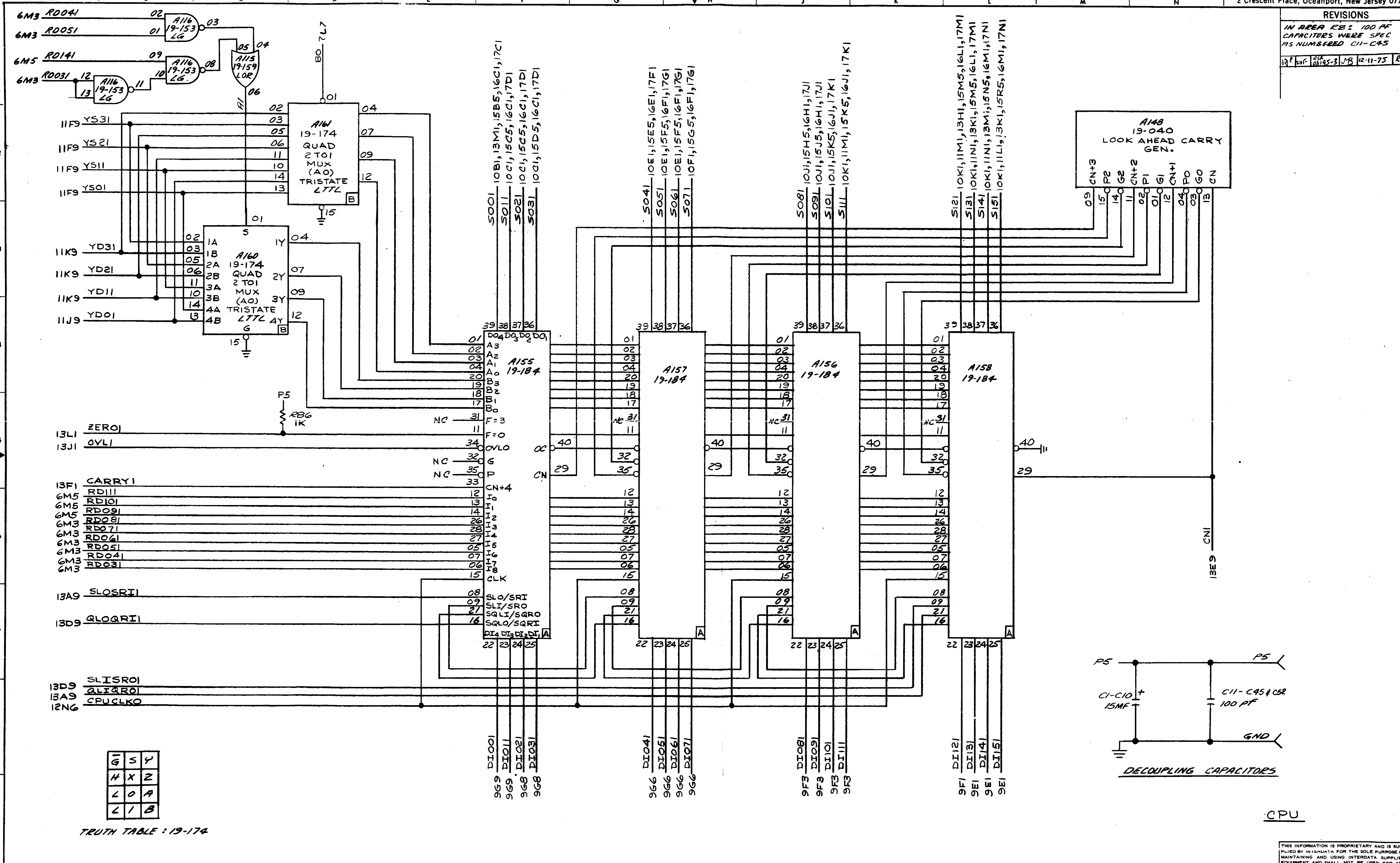
INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS
IN AREA E8: 100 PF CAPACITORS WERE SPEC AS NUMBERED C11-C45
R01



CPU

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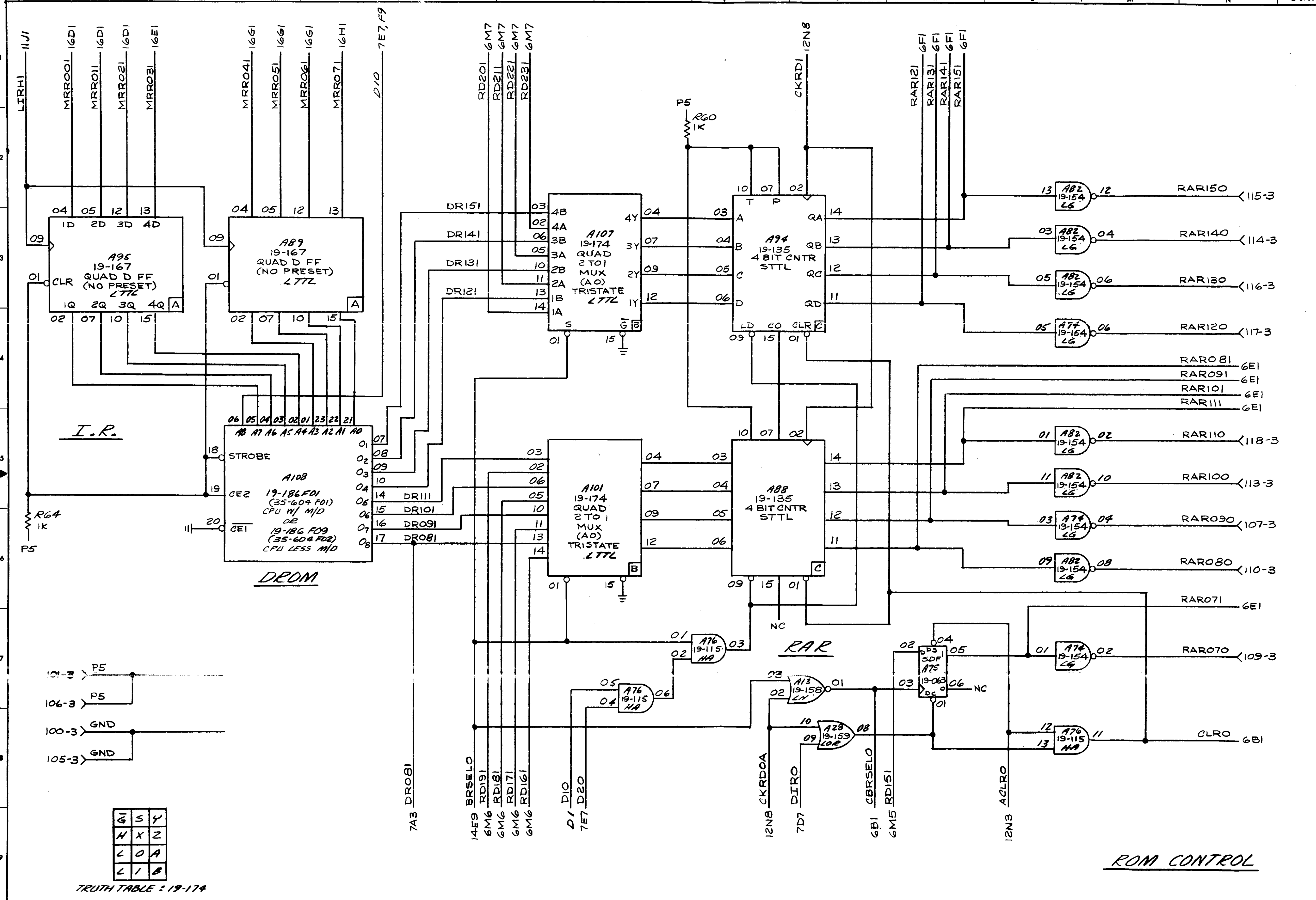
SCALE— | NAME | TITLE | DATE | TITLE
DRAFT / CHK / ENGR

TASK NO. 03145
DWG. NO. 01-094D08
SHEET 4 OF 19

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS
ON A108 AREA C5; PIN 21 WAS SPEC AS MNEMONIC D10 AND REFERENCED TO F9 & 7F7. PIN 22 WAS CONNECTED TO A89-15. PIN 23 WAS CONNECTED TO A89-10. PIN 1 WAS CONNECTED TO A89-07. PIN 2 WAS CONNECTED TO A89-02. PIN 3 WAS CONNECTED TO A95-15. PIN 4 WAS CONNECTED TO A95-10. PIN 5 WAS CONNECTED TO A95-07. PIN 6 WAS CONNECTED TO A95-02.
13P DF ECR 05185-3 J-8 12-11-75 R01



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SCALE—	NAME	TITLE	DATE	TITLE
TOLERANCE XXX ± .005 XX ± .02 X ± .03 ANGLES ± 1/2° UNLESS OTHERWISE SPECIFIED		DRAFT		
		CHK		
		ENGR		
				TASK NO. 03145
				DWG NO. 01-094 R01 D08 — SHEET 5 OF 19

BRUNING 44-231 24538

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

RAR060 H1
CLRO 5N8
CBRSELO 5J9
RD141 M5

CKRDOA 12N8
RAR071 5N6
RAR081 5R4
RAR091 5R4
RAR101 5R4
RAR111 5R5
RAR121 5K1
RAR131 5K1
RAR141 5K1
RAR151 5K1

RAR060 A1

P5
P37
1K

A75 19-063 SDF1

A74 19-154 L6

RAR060A
108-3

A153 19-186F05 STTL (35-609 F02 ONLY)
CE1 CE2 STROBE A8 A7 A6 A5 A4 A3 A2 A1 A0
O8 O7 O6 O5 O4 O3 O2 O1

A154 19-186F02 STTL
O8 O7 O6 O5 O4 O3 O2 O1

RD001 7D3, 17S2
RD011 7D3, 17S2
RD021 7E3
RD031 4A6, 4A1, 7E3, 13C1
RD041 4A6, 4A1, 7F3, 13C1
RD051 4A6, 4A1, 13C1
RD061 4A6, 7J3
RD071 4A6, 7J3

A142 19-186F06 STTL (35-609 F02 ONLY)
O8 O7 O6 O5 O4 O3 O2 O1

A143 19-186F03 STTL
O8 O7 O6 O5 O4 O3 O2 O1

RD081 14C1, 4A6, 7J3
RD091 4A6, 7L3, 14C1
RD101 4A6, 7L2, 14D1
RD111 4A6, 7L3, 14A1
RD121 7E3, 14J1
RD131 7F3, 14F1
RD141 B1, 7G3, 4A1
RD151 5K9, 7N3, 9C8, 11A1

A122 19-186F07 STTL (35-604 F02 ONLY)
O8 O7 O6 O5 O4 O3 O2 O1

A123 19-186F04 STTL
O8 O7 O6 O5 O4 O3 O2 O1

RD161 5F9, 9F8, 9A7
RD171 5F9, 7R3, 8A7, 9A8
RD181 5F9, 7R3, 8A7, 9A7
RD191 5E9, 7R3, 8A7, 9A5
RD201 5E1, 9A4, 7N6, 11A1, 13S2
RD211 5F1, 9A4, 11B1, 13R2, 15C6
RD221 5F1, 9A3, 11B1, 13S2, 15B6
RD231 5F1, 9A3, 11B1, 13S2, 15D6

ADDRESS 200-3FF

ADDRESS 000-1FF

ROM

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SCALE—
TOLERANCE: XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	

TITLE

TASK NO. 03145
DWG NO. 01-094 008
SHEET 6 OF 19

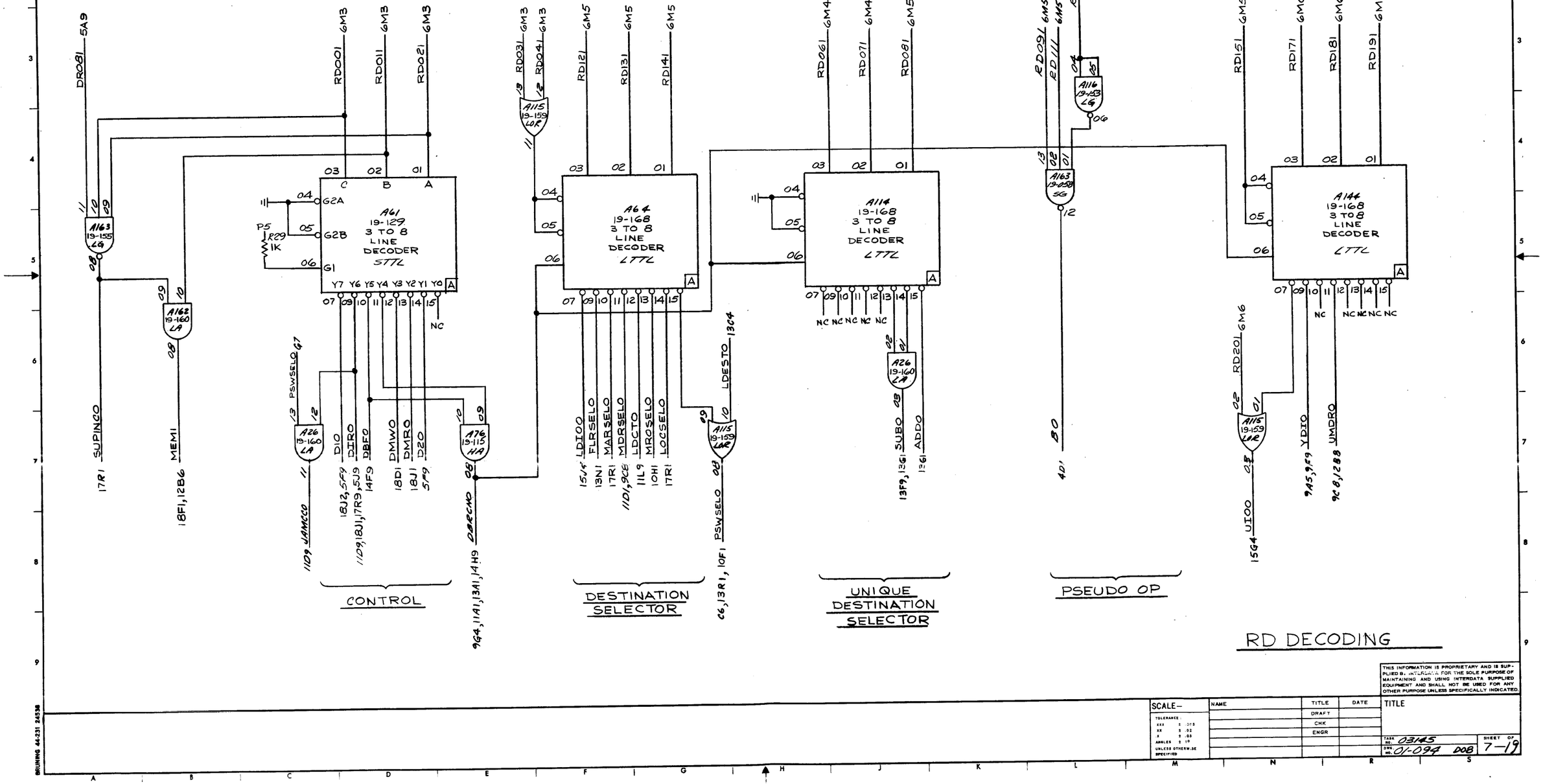
BRUNING 44-231 24538

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
0	0	0	L	H	H	H	H	H	H	H
0	0	1	H	L						
0	1	0	H	H	L					
0	1	1	H	H		L				
1	0	0	H	H			L			
1	0	1	H	H				L		
1	1	0	H	H					L	
1	1	1	H	H						L

TRUTH TABLE : 19-129 & 19-168



RD DECODING

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SCALE–	NAME	TITLE	DATE
TOLERANCE: XXX ± .010, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

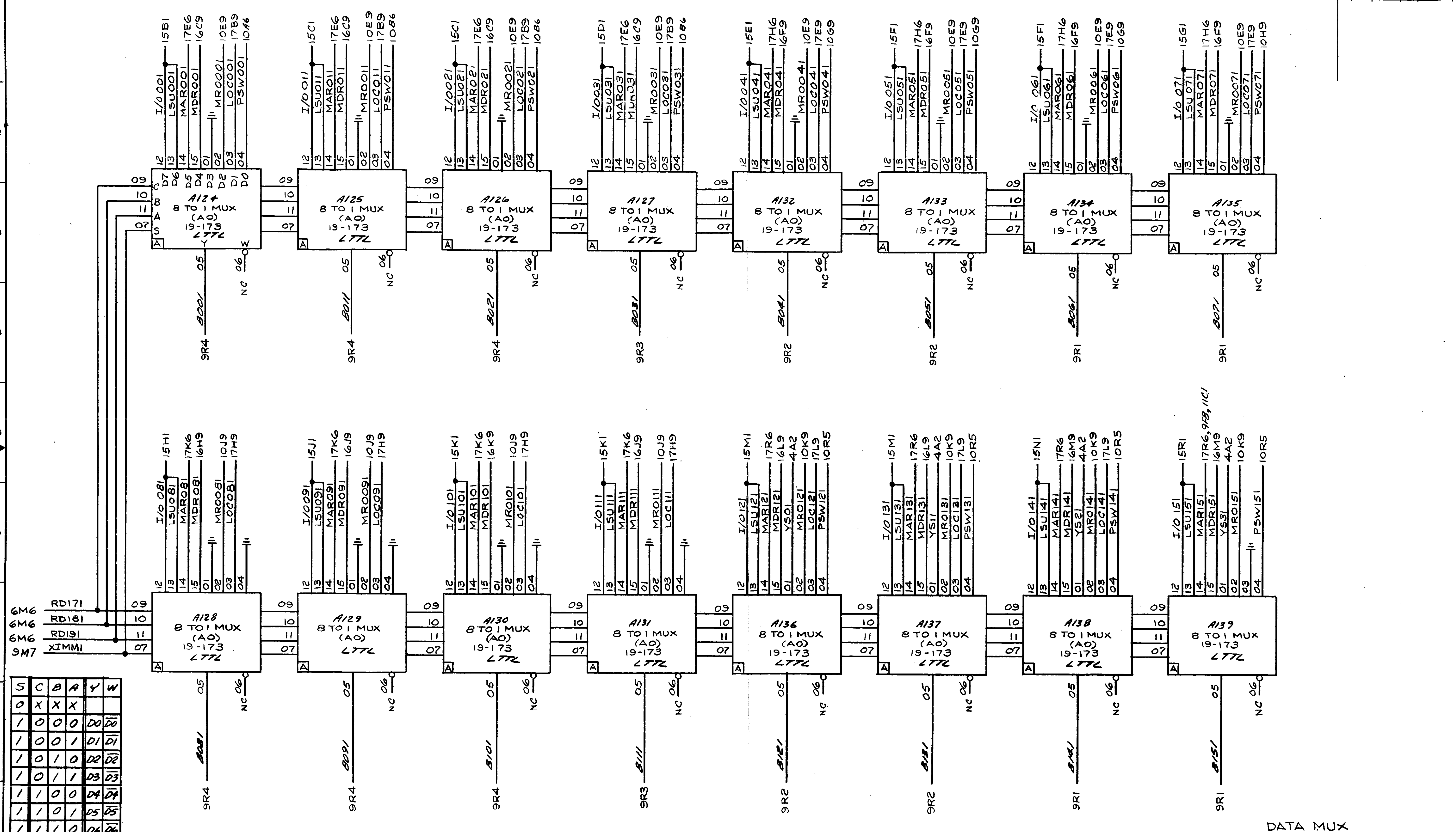
TITLE

TASK NO. 03145
DWG. NO. 01-094 D08
SHEET 7 OF 19

BRUNING 44-231 24536

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS



S	C	B	A	Y	W
0	X	X	X		
1	0	0	0	D0	$\overline{D0}$
1	0	0	1	D1	$\overline{D1}$
1	0	1	0	D2	$\overline{D2}$
1	0	1	1	D3	$\overline{D3}$
1	1	0	0	D4	$\overline{D4}$
1	1	0	1	D5	$\overline{D5}$
1	1	1	0	D6	$\overline{D6}$
1	1	1	1	D7	$\overline{D7}$

TRUTH TABLE : 19-173

DATA MUX

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SCALE— | NAME | TITLE | DATE | TITLE
DRAFT / CHK / ENGR

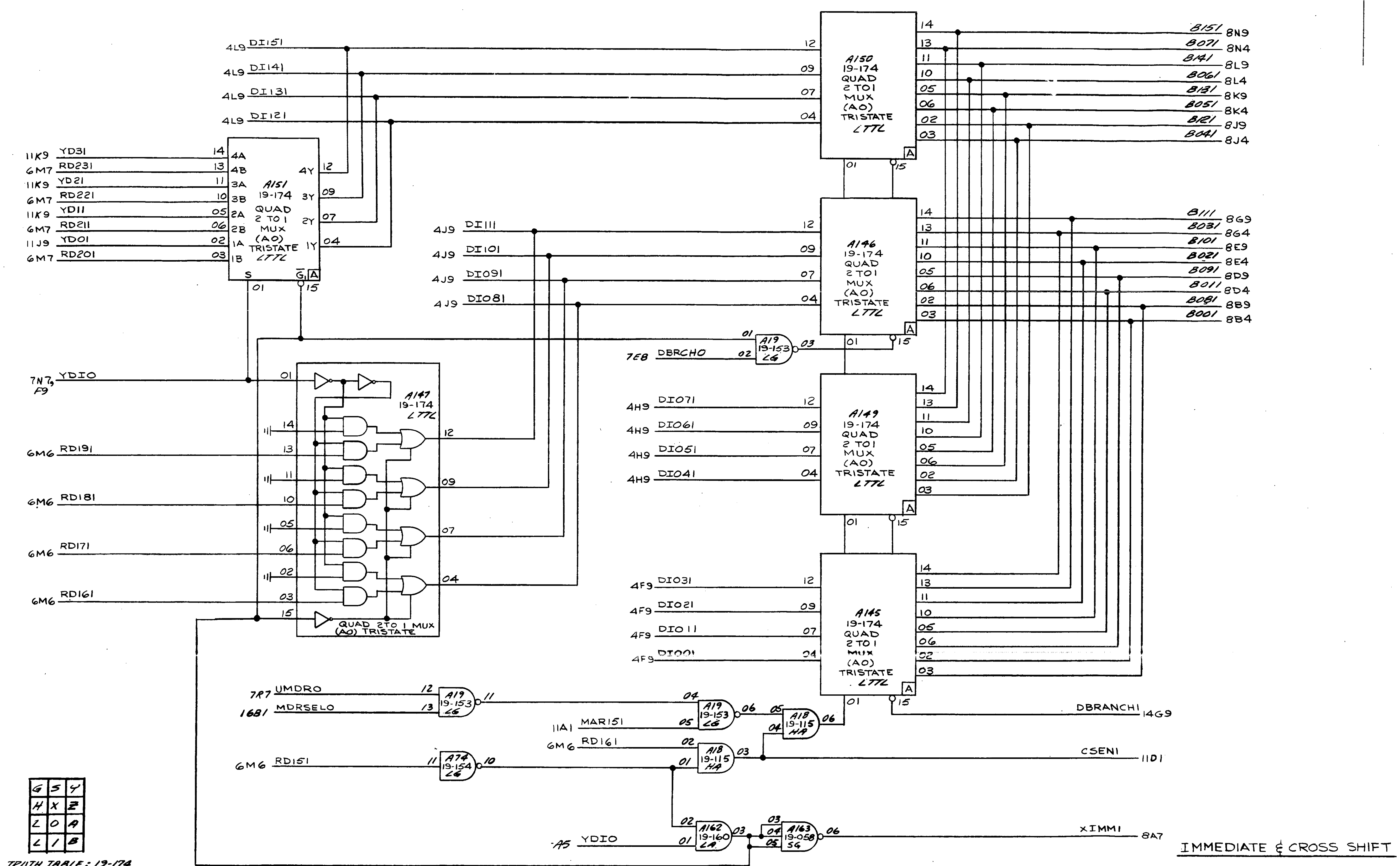
TOLERANCE: .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED

TABS NO. 03145
DWG NO. 01-094 D08 SHEET 8 OF 19

BRUNING 44-231 24538

INTERDATA®
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS



IMMEDIATE & CROSS SHIFT

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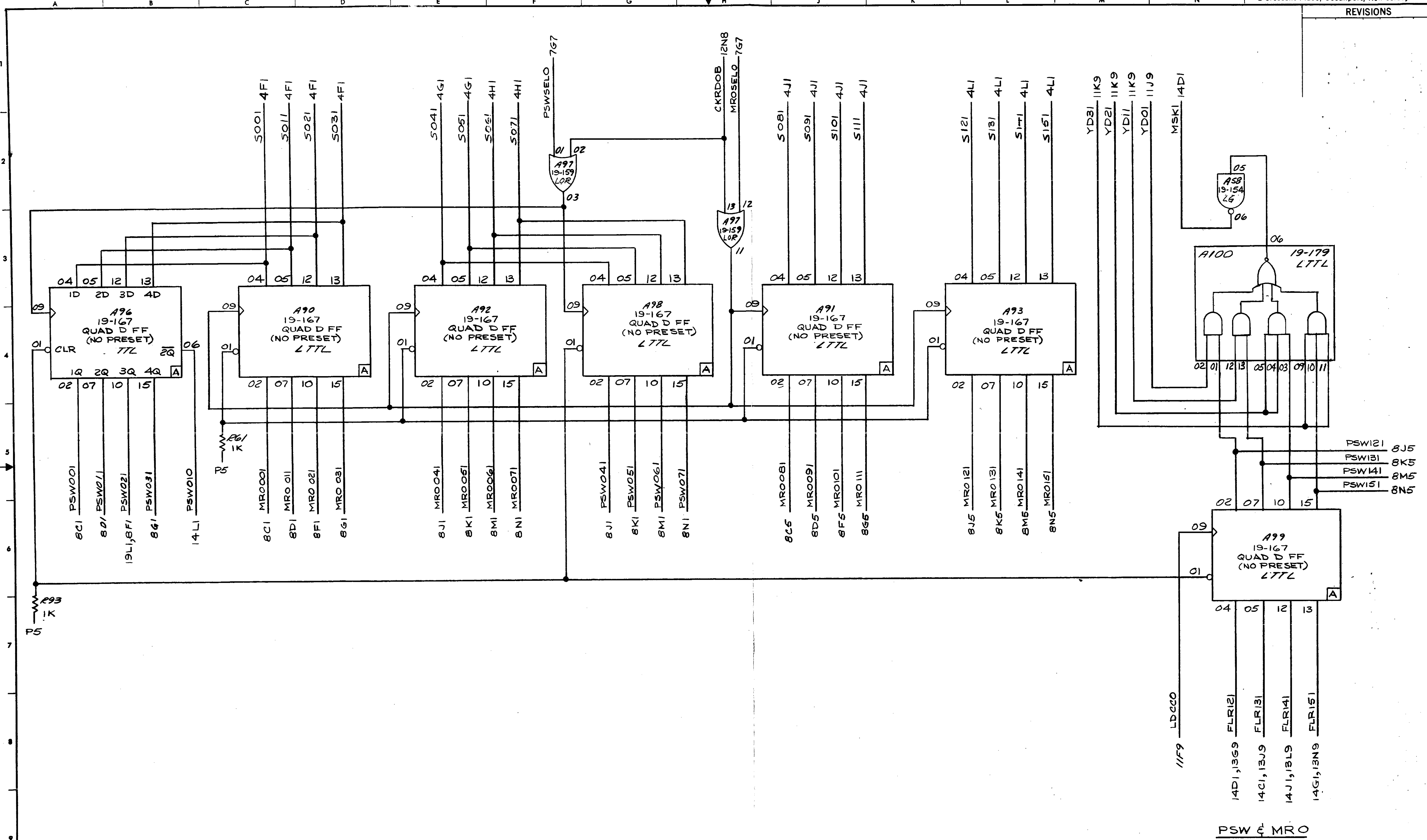
SCALE–	NAME	TITLE	DATE	TITLE
TOLERANCE .XXX ± .005 .XX ± .02 .X ± .03 ANGLES ± 1° UNLESS OTHERWISE SPECIFIED		DRAFT		TASK NO. 03143
		CHK		DWG. NO. 01-094 D08
		ENGR		SHEET 9 OF 19

BRUNING 44-231 24530

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS



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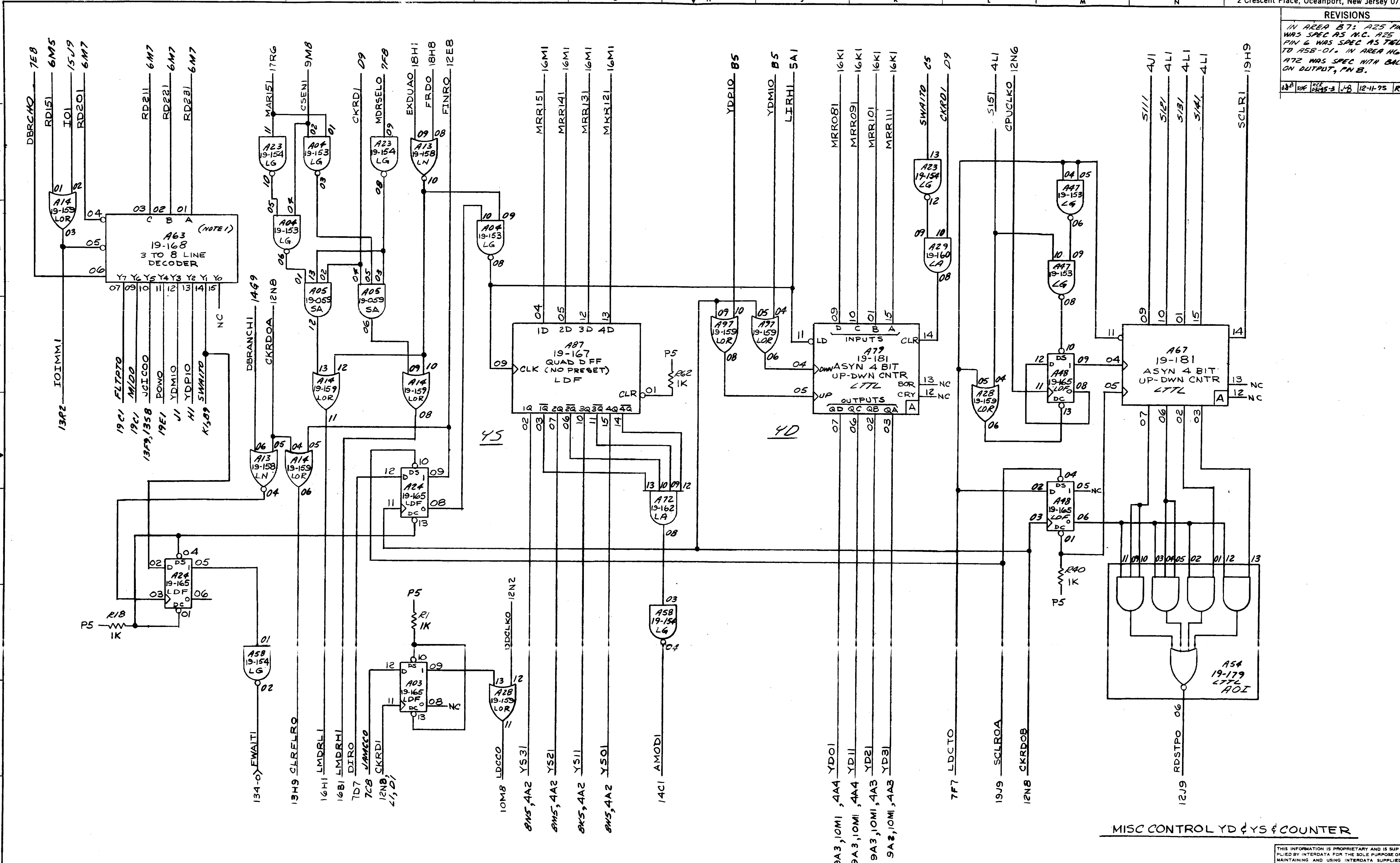
SCALE–	NAME	TITLE	DATE	TITLE
TOLERANCE: .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED		DRAFT		
		CHK		
		ENGR		
				TASK NO. 03165
				DWG NO. 01-094 D08 — SHEET 10 OF 19

BRUNING 44-231 24838

REVISIONS

IN AREA B7: A25 PINS WAS SPEC AS N.C. A25 PIN 6 WAS SPEC AS TIED TO A58-01. IN AREA H6; A72 WAS SPEC WITH BALL ON OUTPUT, PIN 8.

ECO 0845-3 J-B 12-11-75 R01



MISC CONTROL YD & YS & COUNTER

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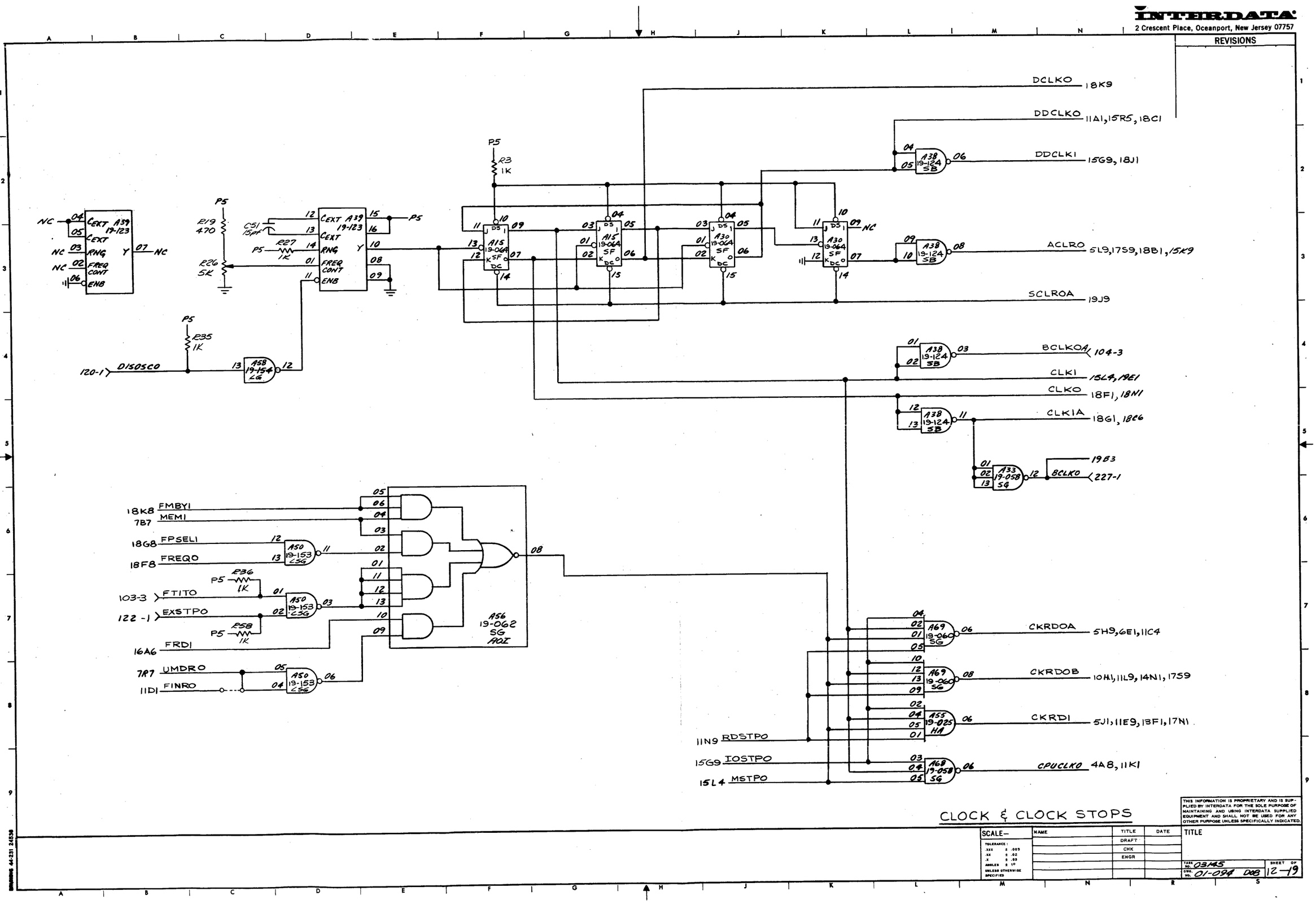
NOTES:
1. SEE TRUTH TABLE ON SHEET 7.

TASK NO. 03145
DWG NO. 01-094R01D08
SHEET 11 OF 19

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS



CLOCK & CLOCK STOPS

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SCALE—	NAME	TITLE	DATE
TOLERANCE: .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

TITLE

TABS NO. 03145 DWG. NO. 01-094 D08 SHEET 12 OF 19

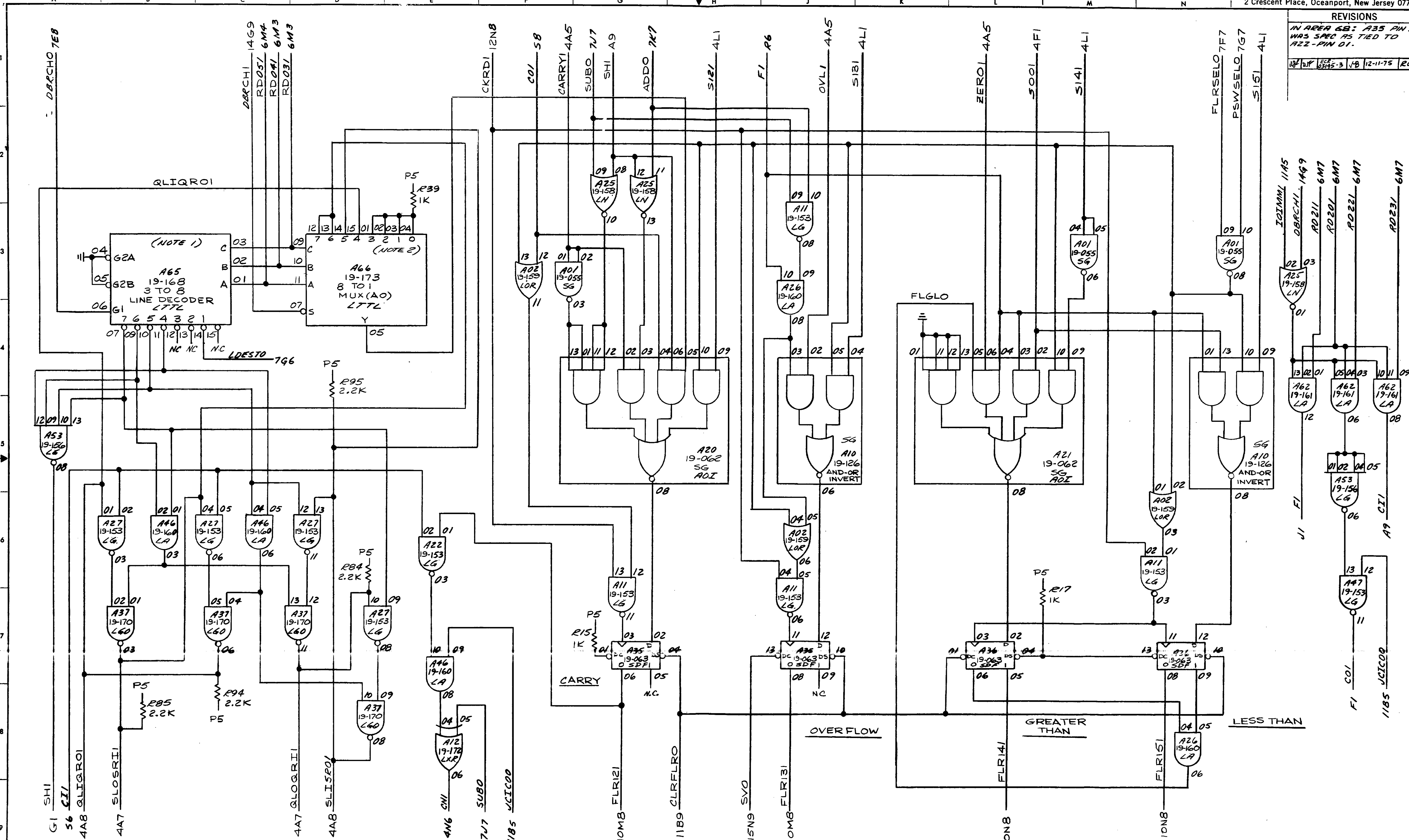
DRAWING 44-231 24538

INTERDATA®
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

IN AREA 6B: A35 PIN 5 WAS SPEC AS TIED TO A22-PIN 01.

R01	ECR 03195-3			12-11-75	R01



FLAG REGISTER & SHIFT CONTROL

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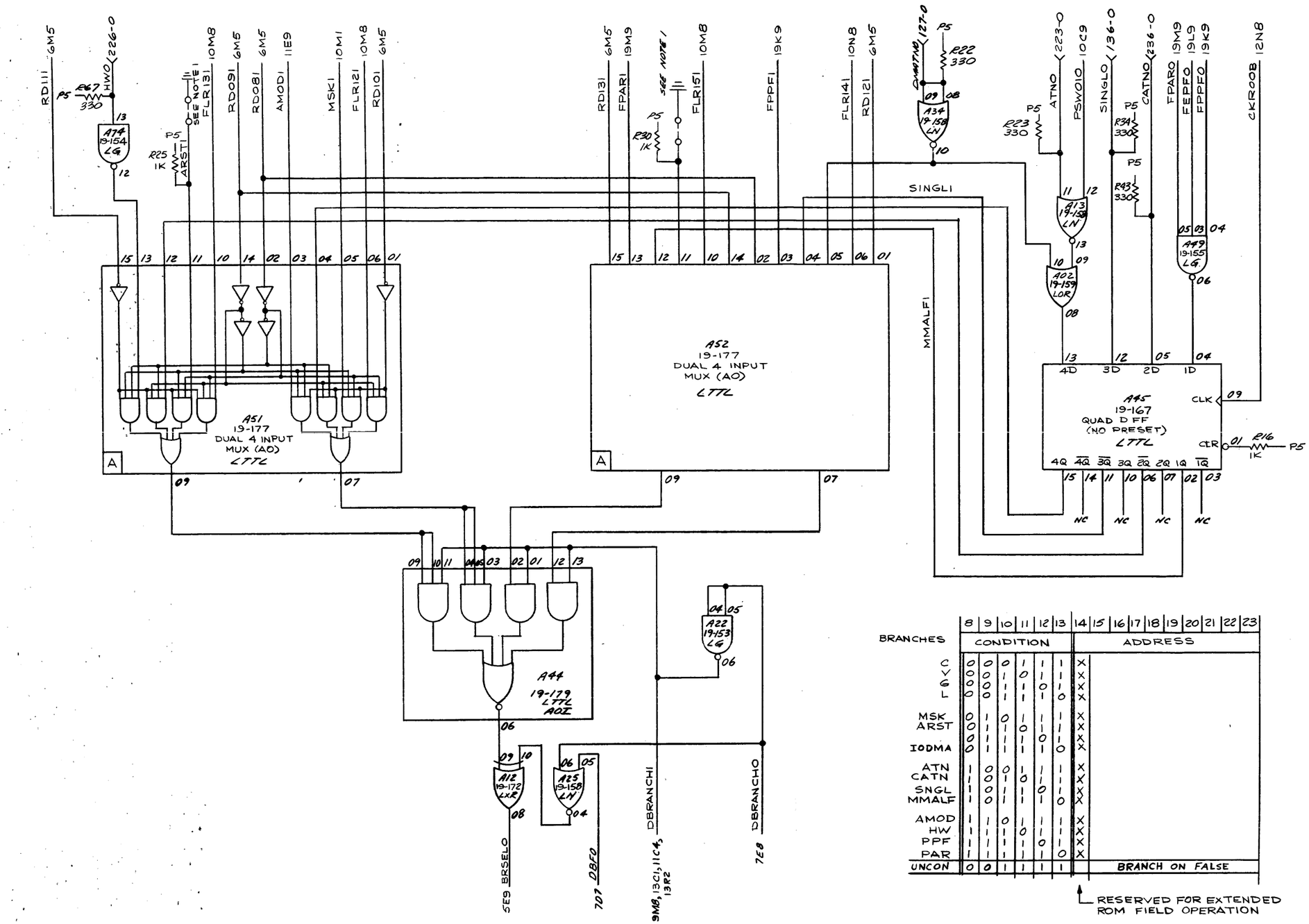
NOTES:
1. SEE TRUTH TABLE ON SHEET 7.
2. SEE TRUTH TABLE ON SHEET 8.

SCALE–	NAME	TITLE	DATE
TOLERANCE		DRAFT	
XXX ± .005		CHK	
XX ± .02		ENGR	
X ± .03			
ANGLES ± 1/2°			
UNLESS OTHERWISE SPECIFIED			

TITLE

TASK NO. 03145
DWG NO. 01-094R01D08
SHEET 13 OF 19

REVISIONS



BRANCHES	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
	CONDITION						ADDRESS									
CYL	0	0	0	1	1	1	X									
	0	0	0	0	1	1	X									
	0	0	0	1	0	1	X									
	0	0	0	0	0	1	X									
	0	0	0	1	1	0	X									
MSK	0	1	0	1	1	1	X									
ARST	0	1	1	0	1	1	X									
	0	1	1	1	0	1	X									
IODMA	0	1	1	1	1	0	X									
ATN	1	0	0	1	1	1	X									
CATN	1	0	0	0	1	1	X									
SNGL	1	0	0	1	0	1	X									
MMALF	1	0	0	0	0	1	X									
AMOD	1	1	0	1	1	1	X									
HW	1	1	1	0	1	1	X									
PPF	1	1	1	1	0	1	X									
PAR	1	1	1	1	1	0	X									
UNCON	0	0	1	1	1	1	BRANCH ON FALSE									

RESERVED FOR EXTENDED ROM FIELD OPERATION

BRANCH LOGIC

NOTES:
1. RESISTOR & STAKES NOT EQUIPPED ON THIS ASSY.

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SCALE—

TOLERANCE: XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	

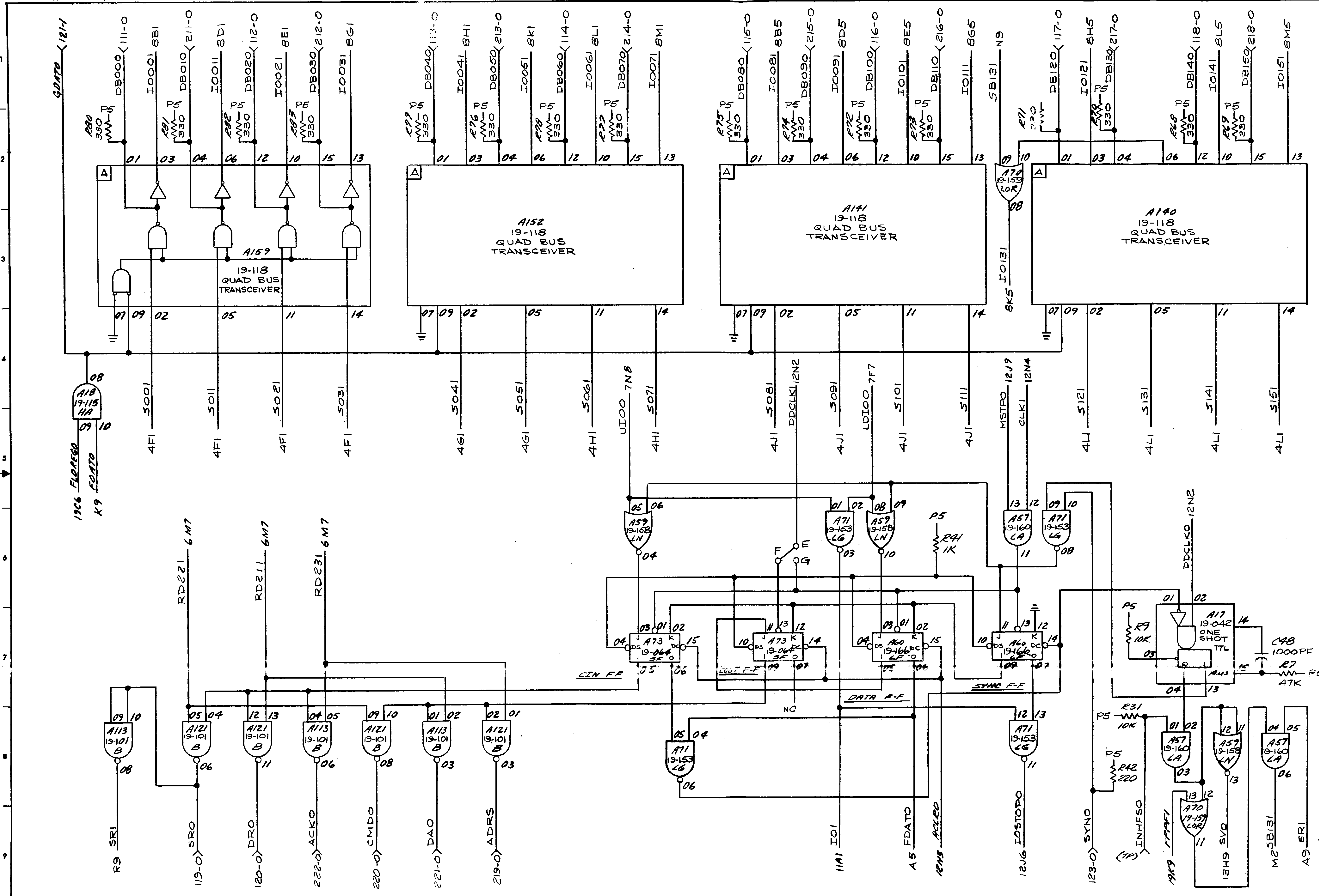
TITLE

TASK NO. 03145
DWG NO. 01-094 D0B
SHEET OF 14—19

BRUNING 44-231 24838

INTERDATA®
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS



IO BUFFER & CONTROL

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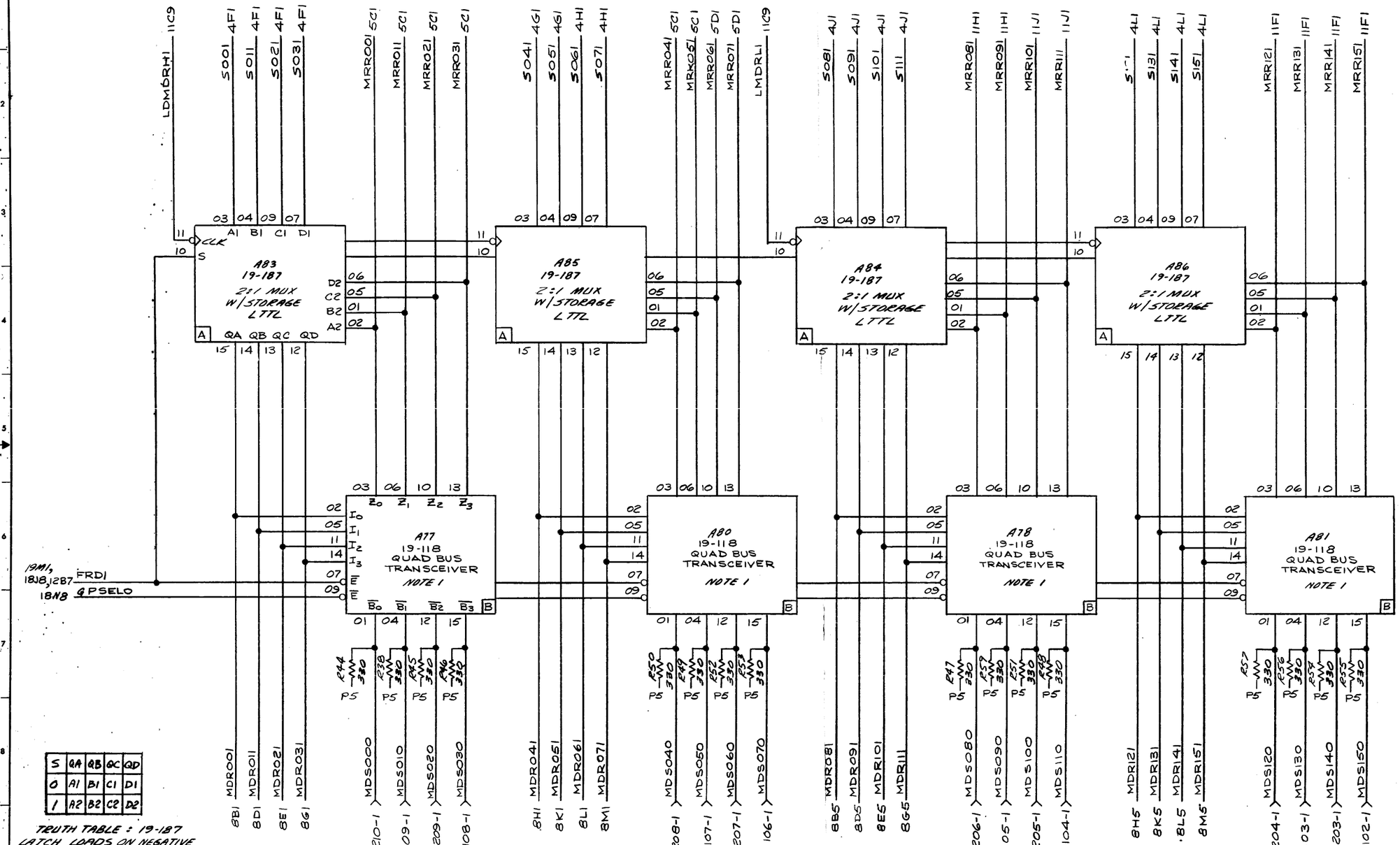
SCALE–	NAME	TITLE	DATE	TITLE
TOLERANCE		DRAFT		
UNLESS OTHERWISE SPECIFIED		CHK		
		ENGR		

TASK NO. 03145
DWG NO. 01-094 D08
SHEET 15 OF 19

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS



S	QA	QB	QC	QD
0	A1	B1	C1	D1
1	A2	B2	C2	D2

MDR & MEMORY BUS DRIVERS

NOTES :
1. SEE INTERNAL LOGIC SHEET 15.

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SCALE—
TOLERANCE : XXX ± .005, XX ± .02, .X ± .05, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
	DRAFT	
	CHK	
	ENGR	

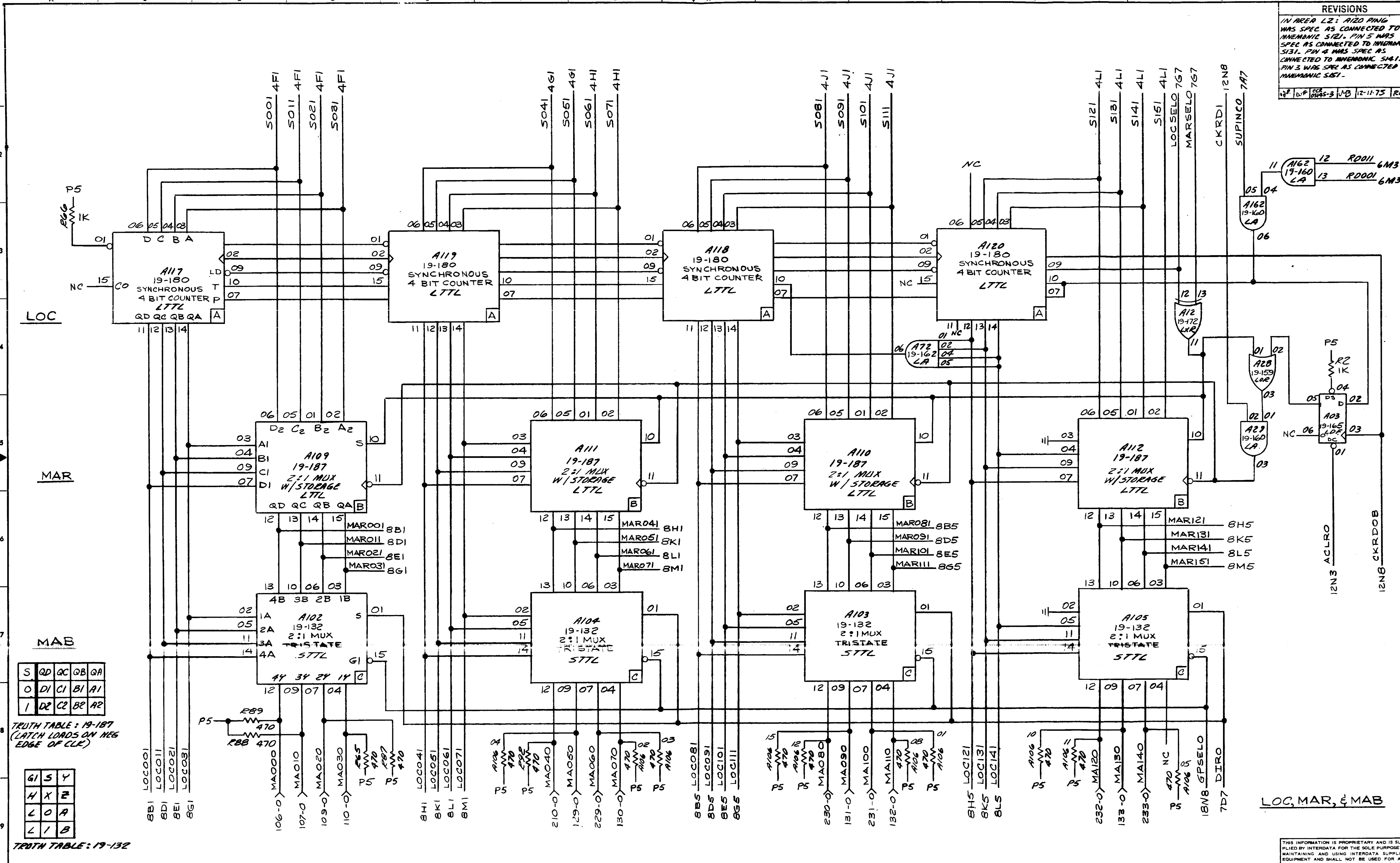
TITLE

TASK NO. 23145
DWG NO. 01-094 D08
SHEET OF 16-19

BRUNING 44-231 24536

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS					
IN AREA L2: A120 PIN 6 WAS SPEC AS CONNECTED TO MNEMONIC S121. PIN 5 WAS SPEC AS CONNECTED TO MNEMONIC S131. PIN 4 WAS SPEC AS CONNECTED TO MNEMONIC S141. PIN 3 WAS SPEC AS CONNECTED TO MNEMONIC S151.					
13ª	D.F.	ECR 03145-3	JB	12-11-75	R01



LOC
MAR
MAB
A117 19-180 SYNCHRONOUS 4 BIT COUNTER LTTL
A119 19-180 SYNCHRONOUS 4 BIT COUNTER LTTL
A118 19-180 SYNCHRONOUS 4 BIT COUNTER LTTL
A120 19-180 SYNCHRONOUS 4 BIT COUNTER LTTL
A109 19-187 2:1 MUX W/STORAGE LTTL
A111 19-187 2:1 MUX W/STORAGE LTTL
A110 19-187 2:1 MUX W/STORAGE LTTL
A112 19-187 2:1 MUX W/STORAGE LTTL
A102 19-132 2:1 MUX TRISTATE STTL
A104 19-132 2:1 MUX TRISTATE STTL
A103 19-132 2:1 MUX TRISTATE STTL
A105 19-132 2:1 MUX TRISTATE STTL
A162 19-160 LA
A72 19-162 LA
A12 19-172 LXR
A28 19-159 LOR
A29 19-160 LA
A03 19-165 LDF
S001 4F1 S011 4F1 S021 4F1 S031 4F1
S041 4G1 S051 4G1 S061 4H1 S071 4H1
S081 4J1 S091 4J1 S101 4J1 S111 4J1
S121 4L1 S131 4L1 S141 4L1 S151 4L1
LOCSEL0 7G7 MARSEL0 7G7 CKRD1 12N8 SUPINC0 7A7
R0011 6M3 R0001 6M3
MAR001 8B1 MAR011 8D1 MAR021 8E1 MAR031 8G1
MAR041 8H1 MAR051 8K1 MAR061 8L1 MAR071 8M1
MAR081 8B5 MAR091 8D5 MAR101 8E5 MAR111 8G5
MAR121 8H5 MAR131 8K5 MAR141 8L5 MAR151 8M5
ACLR0 12N3 CKRD0B 12N8
LOC001 LOC011 LOC021 LOC031 8B1 8D1 8E1 8G1
MA000 106-0 MA010 107-0 MA020 109-0 MA030 110-0
LOC041 LOC051 LOC061 LOC071 8H1 8K1 8L1 8M1
MA040 210-0 MA050 129-0 MA060 229-0 MA070 130-0
LOC081 LOC091 LOC101 LOC111 8B5 8D5 8E5 8G5
MA080 230-0 MA090 131-0 MA100 231-0 MA110 132-0
LOC121 LOC131 LOC141 8H5 8K5 8L5
MA120 232-0 MA130 133-0 MA140 233-0
GPSEL0 18N8 DIR0 7D7
P5 R66 1K R89 470 R88 470 R2 1K
S	QD	QC	QB	QA
0	D1	C1	B1	A1
1	D2	C2	B2	A2
TRUTH TABLE: 19-187 (LATCH LOADS ON NEG EDGE OF CLK)
G1	S	Y
H	X	Z
L	0	A
L	1	B
TRUTH TABLE: 19-132
LOC, MAR, & MAB

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SCALE— TOLERANCE .XXX ± .005 .XX ± .02 .X ± .03 ANGLES ± 1° UNLESS OTHERWISE SPECIFIED

NAME | TITLE | DATE: DRAFT, CHK, ENGR

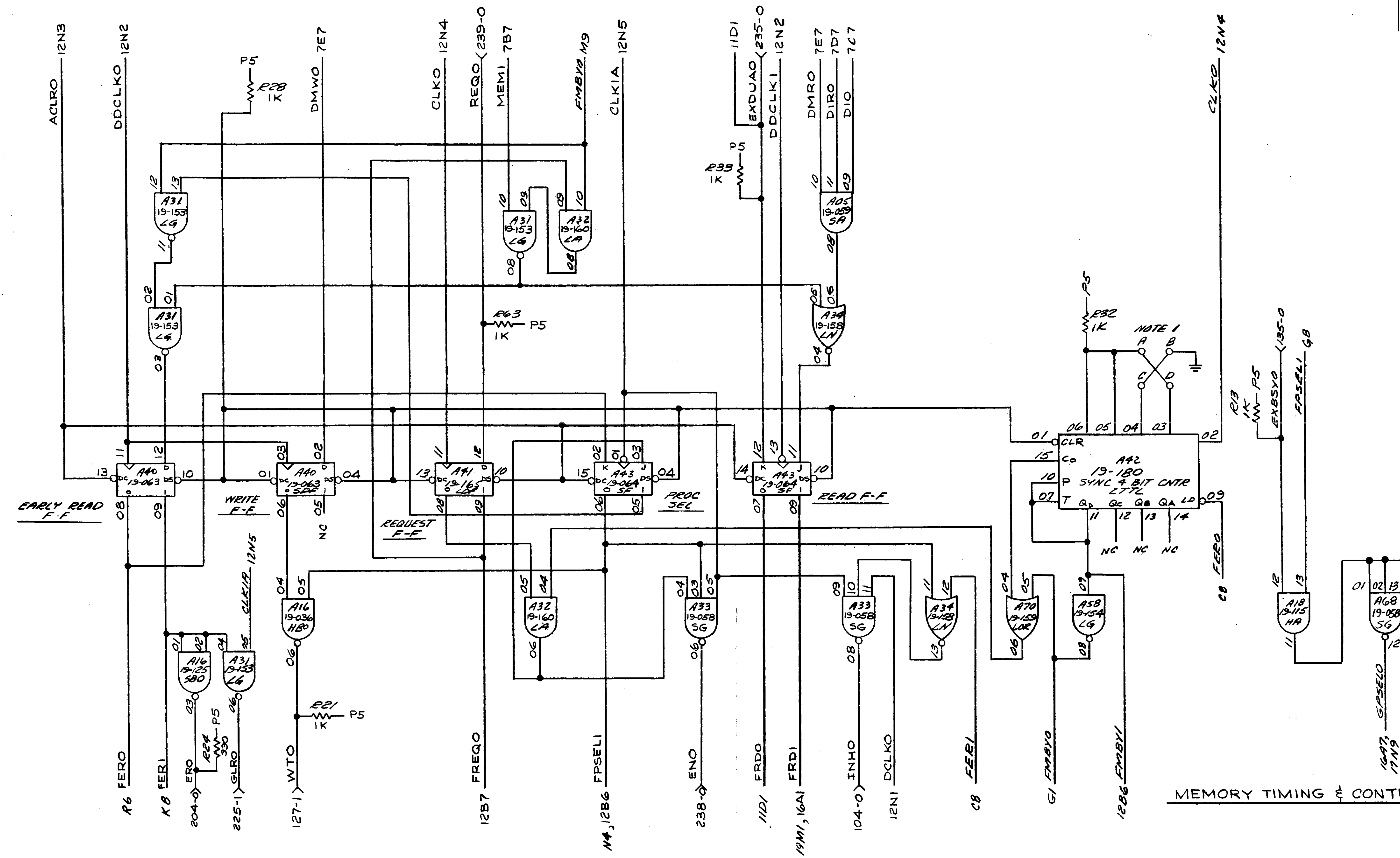
TITLE

TASK NO. 03145 — DWG. NO. 01-094 R01D08 — SHEET 17 OF 19

BRUNING 44-231 24536

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS



MEMORY TIMING & CONTROL

NOTES:

1. THE FOLLOWING STRAPPING OPTIONS ARE MADE ACCORDING TO TYPE OF MEMORY TO BE INSTALLED IN PROCESSOR:

TYPE OF MEMORY	STRAPPING OPTION
SEMI	A-C-D
.75 µS CORE	A-C & B-D
1.0 µS CORE NORMALLY BUILT	A-D & B-C

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SCALE—	NAME	TITLE	DATE	TITLE
TOLERANCE: XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED		DRAFT		
		CHK		
		ENGR		TASK NO. 03145
				DWG NO. 01-094 D08 — SHEET 18 OF 19

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

INITIALIZE & ALARM REGISTERS

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SCALE–	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED		DRAFT	
		CHK	
		ENGR	

TITLE

TASK NO. 03185

DWG NO. 01-094 208

SHEET 19 OF 19

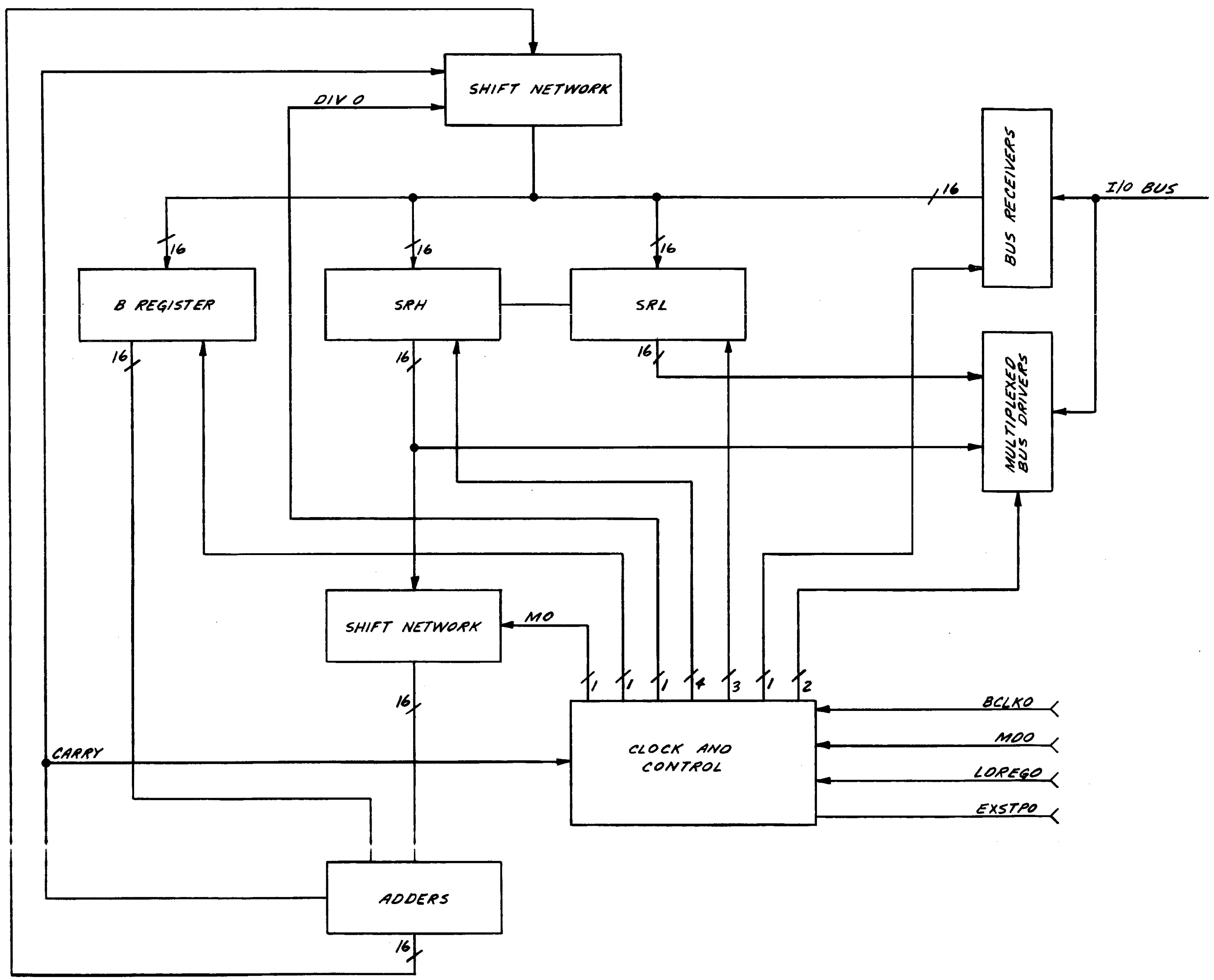
INTERDATA®
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS		
PRE PRODUCTION APPROVAL	DEV	INIT DJF DATE 10-3-75

REVISIED SHT. 4,
35-605 WAS R01,
CONN TABLE EXTSTPO
WAS PIN 122

B	G	DJF	03145-A	KC	12-10-75	R01

RELEASED FOR PRODUCTION
ENG. DJF DATE 12-16-75



TERM NO	ROW 1	ROW 2
41	P5	GND
40	GND	GND
39		
38		
37		
36		
35		
34		
33		
32		
31		
30		
29		
28	LDREG0	M/D0
27		BCLK0
26	SCLR0	
25		
24	EXSTP0	
23		
22		
21		
20		
19		
18	D140	D150
17	D120	D130
16	D100	D110
15	D080	D090
14	D060	D070
13	D040	D050
12	D020	D030
11	D000	D010
10		
09		
08		
07		
06		
05		
04		
03		
02		
01	GND	GND
00	P5	GND

PRINTED CIRCUIT BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL

MULT./DIV.	35-605 R02

NOTE: THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

SHEET INDEX	REV. LEVEL	01			01
	SHEET NO.	1	2	3	4

THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED.

SCALE—

TOLERANCE
XXX ± .005
XX ± .02
.X ± .03
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
J.R. BIELSKIE	DRAFT	9-25-75
R F CERO	CHK	10-3-75
D. FRANKENBERGER	ENGR	12-16-75
B MULLER	SYS TEST	12-16-75
S. MESSINA	MGR.	12-16-75

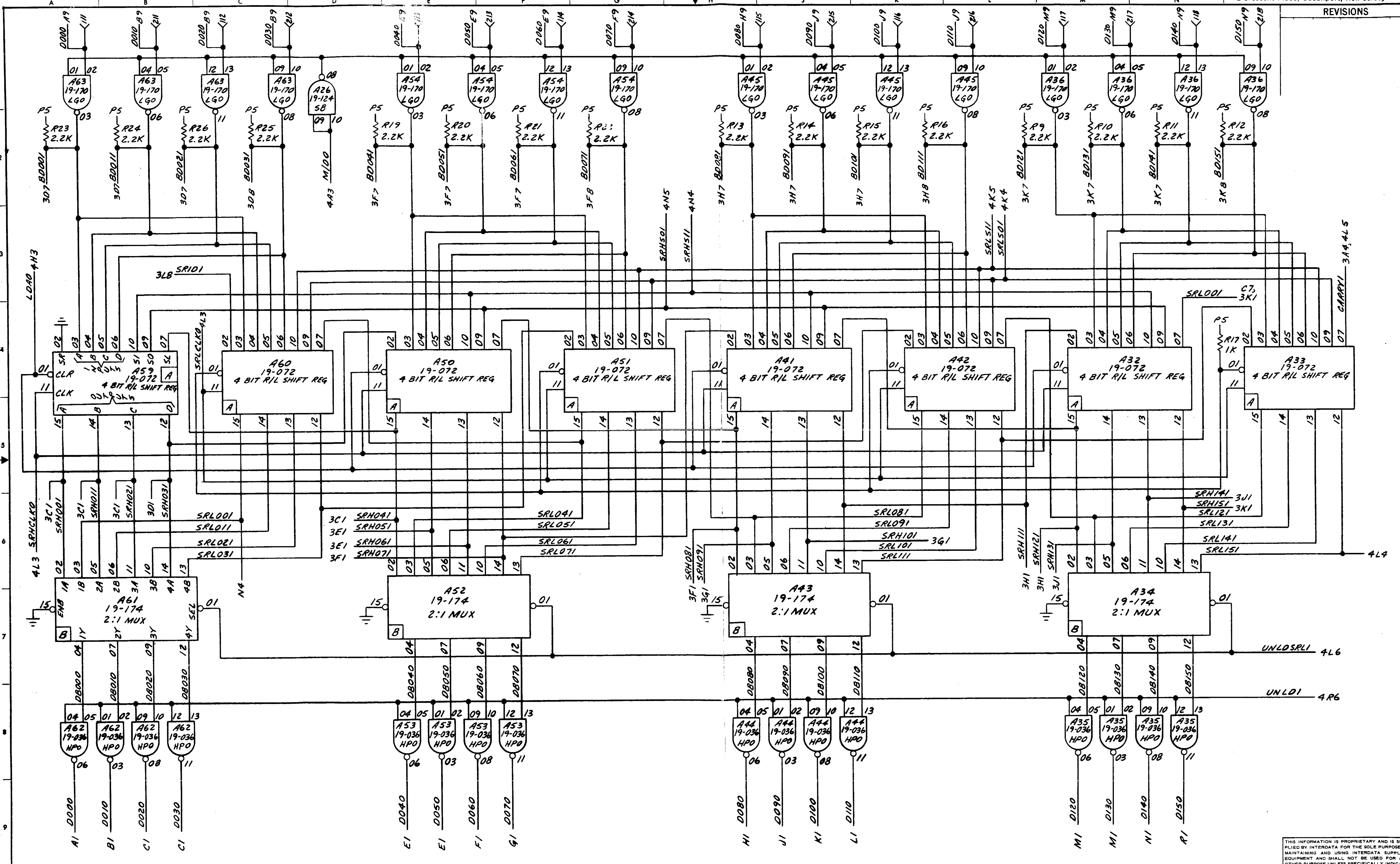
TITLE FUNCTIONAL SCHEMATIC MULTIPLY/DIVIDE

TASK NO. 03145
DWG. NO. 02-403 R01 D08
SHEET 1 OF 4

BRUNING 44-231 24836

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS



THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED.

SCALE–	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	J.R. BIELSKIE	DRAFT	7-24-75
		CHK	
		ENGR	

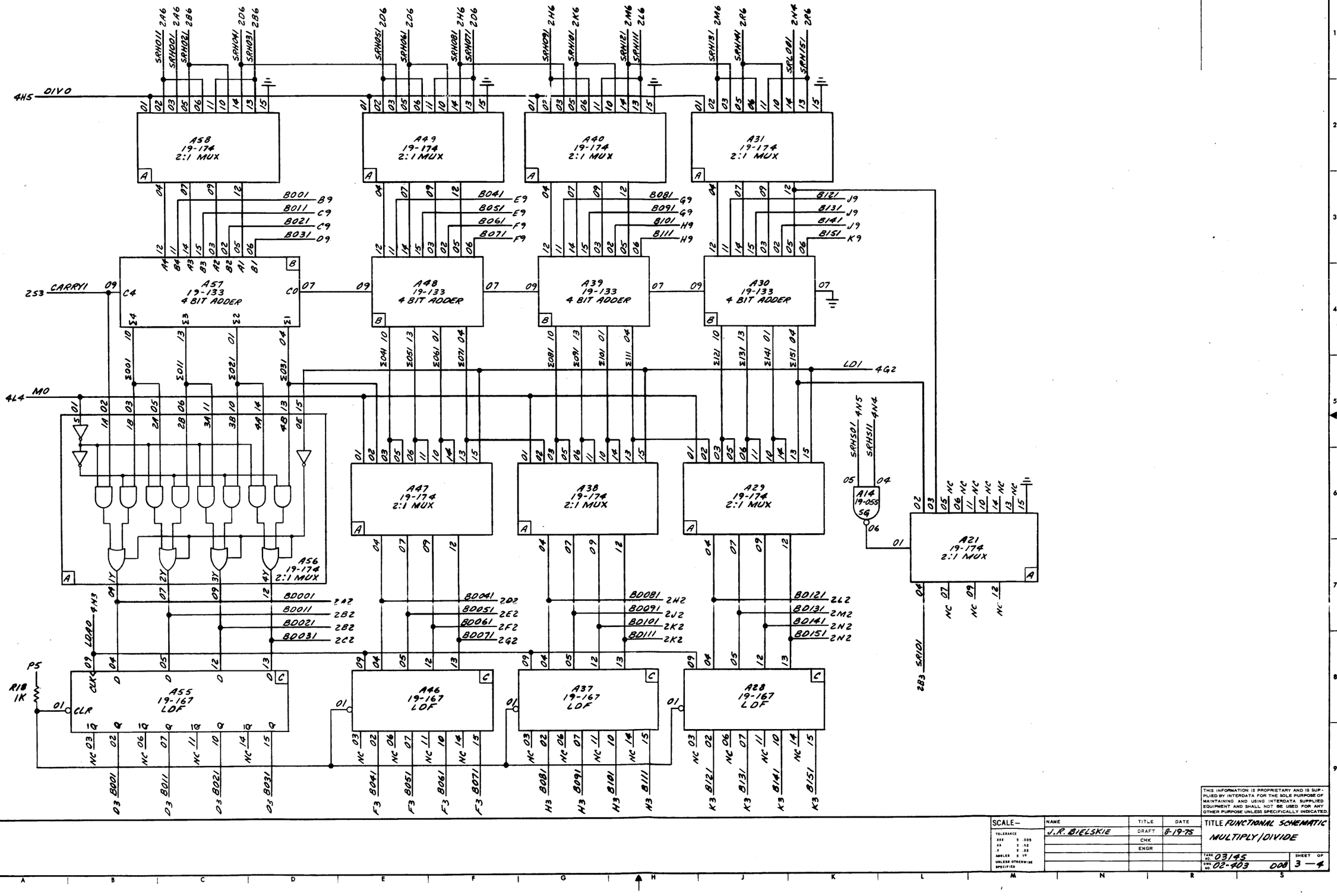
TITLE FUNCTIONAL SCHEMATIC MULTIPLY/DIVIDE

TASK NO. 03145
DWG NO. 02-403 D08
SHEET 2 OF 4

BRUNING 44-231 24538

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS



THIS INFORMATION IS PROPRIETARY AND IS SUPPLIED BY INTERDATA FOR THE SOLE PURPOSE OF MAINTAINING AND USING INTERDATA SUPPLIED EQUIPMENT AND SHALL NOT BE USED FOR ANY OTHER PURPOSE UNLESS SPECIFICALLY INDICATED.

SCALE–	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	J.R. BIELSKIE	DRAFT	8-19-75
		CHK	
		ENGR	

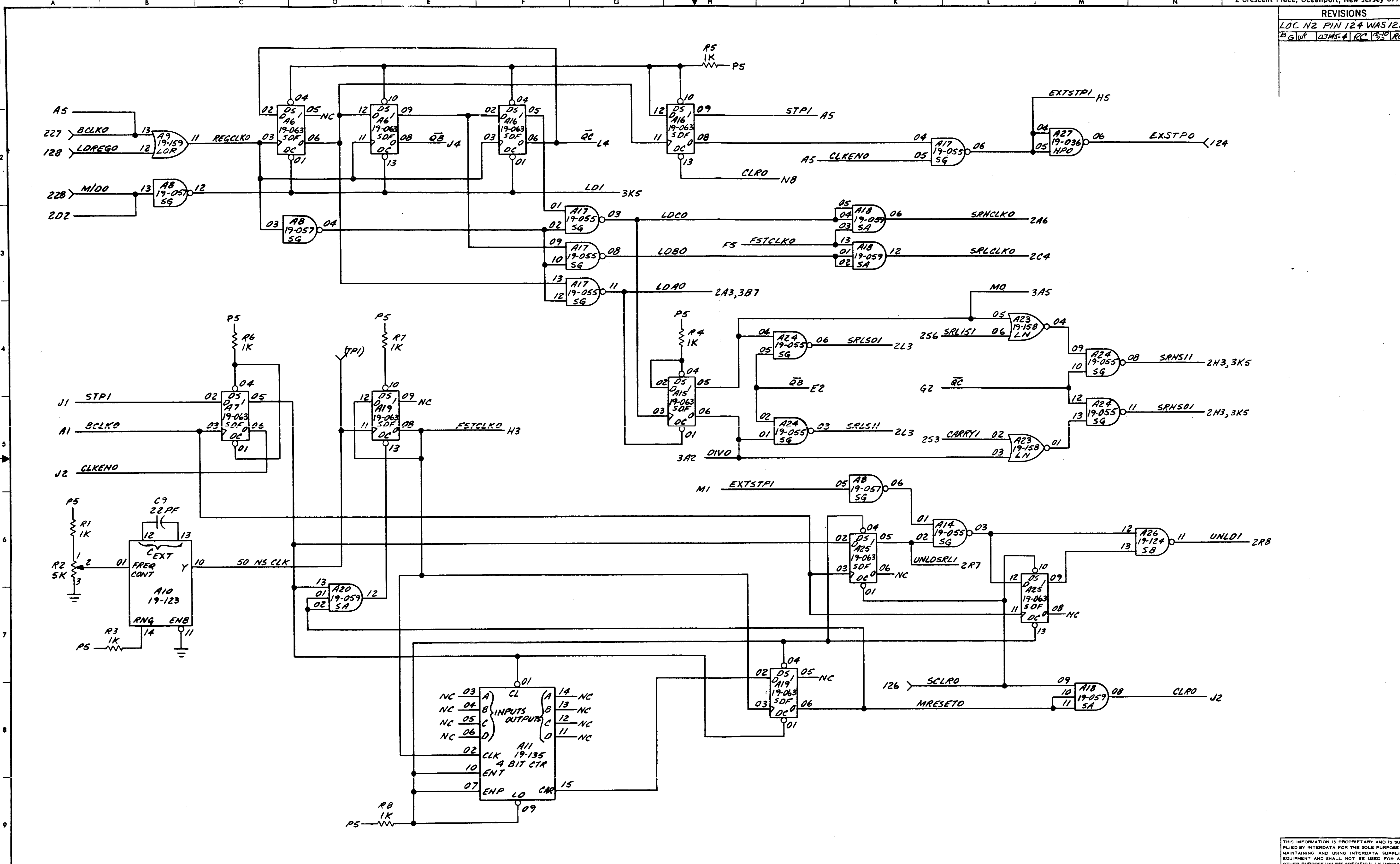
TITLE FUNCTIONAL SCHEMATIC
MULTIPLY/DIVIDE

TASK NO. 03145
DWG NO. 02-403 008
SHEET OF 3 — 4

DRAWING 44-231 24830

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS
LOC N2 PIN 124 WAS 122
B G 03145-4 RC R01



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SCALE—	NAME	TITLE	DATE
TOLERANCE: .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	J.R. BIELSKIE	DRAFT	9-3-75
		CHK	
		ENGR	

TITLE FUNCTIONAL SCHEMATIC MULTIPLY/DIVIDE

TASK NO. 03145
DWG NO. 02-403R01D08
SHEET 4 OF 4

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS			
PRE PRODUCTION APPROVAL	DEV	INIT DJF	DATE 11-18-75

REVISED SHT 3, 35-601 & 35-603 WERE R00, 35-602 WAS R01

B	G	DJF	23145-5	MB	12-17-75	R01

RELEASED FOR PRODUCTION
ENG DJF DATE 12/16/75

REVISED SHTS 2 & 3. 35-603 WAS R01.

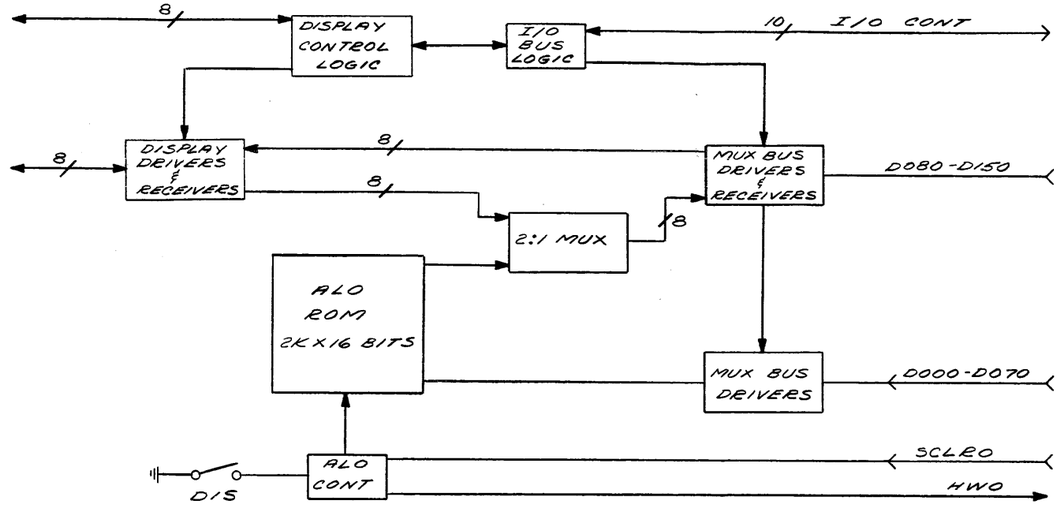
DJF	7	2774	—	3-17-76	R02

BACK PANEL MAP

ROW 1	ROW 2	TERM NO.	CONN
		41	0
		40	
		39	
		38	
		37	
INITO		36	
CATNO	SINGLO	35	
WAITI		34	
		33	
		32	
		31	
		30	
		29	
		28	
		27	
SCLRO	HWO	26	
		25	
		24	
SYNO		23	
		22	
	DAO	21	
DRO	CMDO	20	
SRO	ADRSO	19	
D140	D150	18	
D120	D130	17	
D100	D110	16	
D080	D090	15	
D060	D070	14	
D040	D050	13	
D020	D030	12	
D000	D010	11	
		10	
		09	
		08	
		07	
		06	
		05	
		04	
		03	
		02	
		01	
		00	

ROW 2	ROW 1	TERM NO.	CONN
SHIO	GND	00	A
GND	INITO	01	
D41	WAITI	02	
LAO	ESNCO	03	
D51	ESNOO	04	
D61	POFFO	05	
SLOO	SSGLI	06	
	SCLROD	07	
D71	GND	08	
	D01	09	
	D11	10	
P5	D21	11	
GND	D31	12	
	SRGOA	13	
	LBO	14	
		15	
		16	

BLOCK DIAGRAM



PRINTED CIRCUIT BOARD AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL

DISPLAY CONT. LESS ALO	35-601 R01
DISPLAY CONT. W/ALO	35-602 R02
ALO LESS DISPLAY CONT.	35-603 R02

NOTE: THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

SHEET INDEX					
REV LEVEL	2	1	2		
SHEET NO.	1	2	3		

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SCALE—

TOLERANCE
XXX ± .005
XX ± .02
X ± .03
ANGLES ± 1°
UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
B. GRAY	DRAFT	9-4-75
R. CERO	CHK	12-16-75
D. FRANKENBERGER	ENGR	12-16-75
B. MILLER	SYS TEST	12-16-75
S. MESSINA	MGR	12-16-75

TITLE: DISPLAY CONTROLLER

TASK NO. 03145
DWG NO. 02-405R02D08
SHEET OF 1—3

BRUNING 44-231 24538

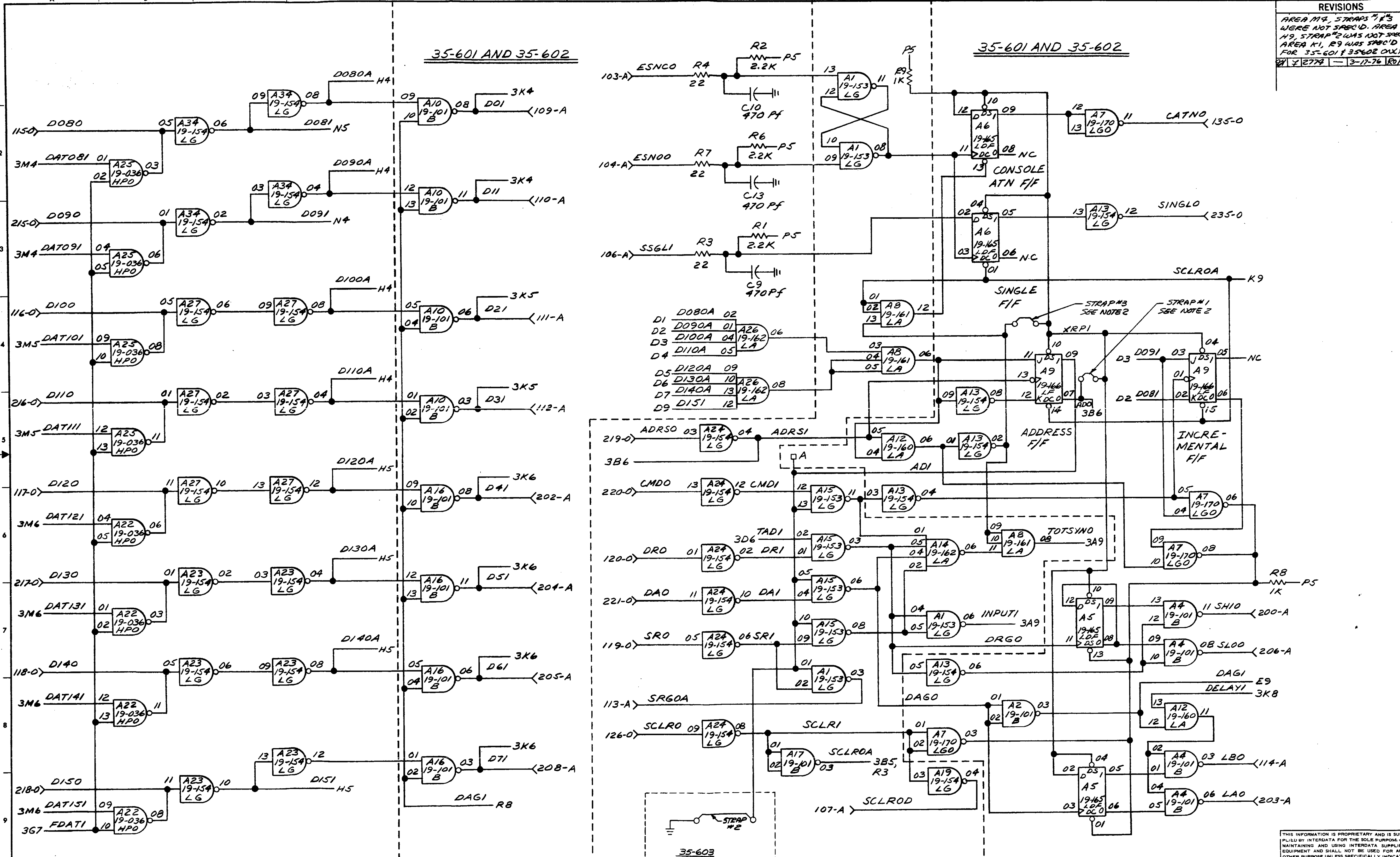
INTERDATA

2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

AREA M9, STRAPS #1 & #3 WERE NOT SPEC'D. AREA H9, STRAP #2 WAS NOT SPEC'D AREA K1, R9 WAS SPEC'D FOR 35-601 & 35602 ONLY.

2774 — 3-17-76 R01



NOTE:
1. UNLESS OTHERWISE SPECIFIED ALL COMPONENTS ON THIS SHEET ARE LOCATED ON 35-601, 35-602 & 35-603
2. ADD STRAPS 1 & 3 ON 35-603 ONLY. (SEE AREA M-4)

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SCALE—	NAME	TITLE	DATE
	B GRAY	DRAFT	
		CHK	
		ENGR	

TITLE: DISPLAY CONTROLLER

TASK NO. 03145

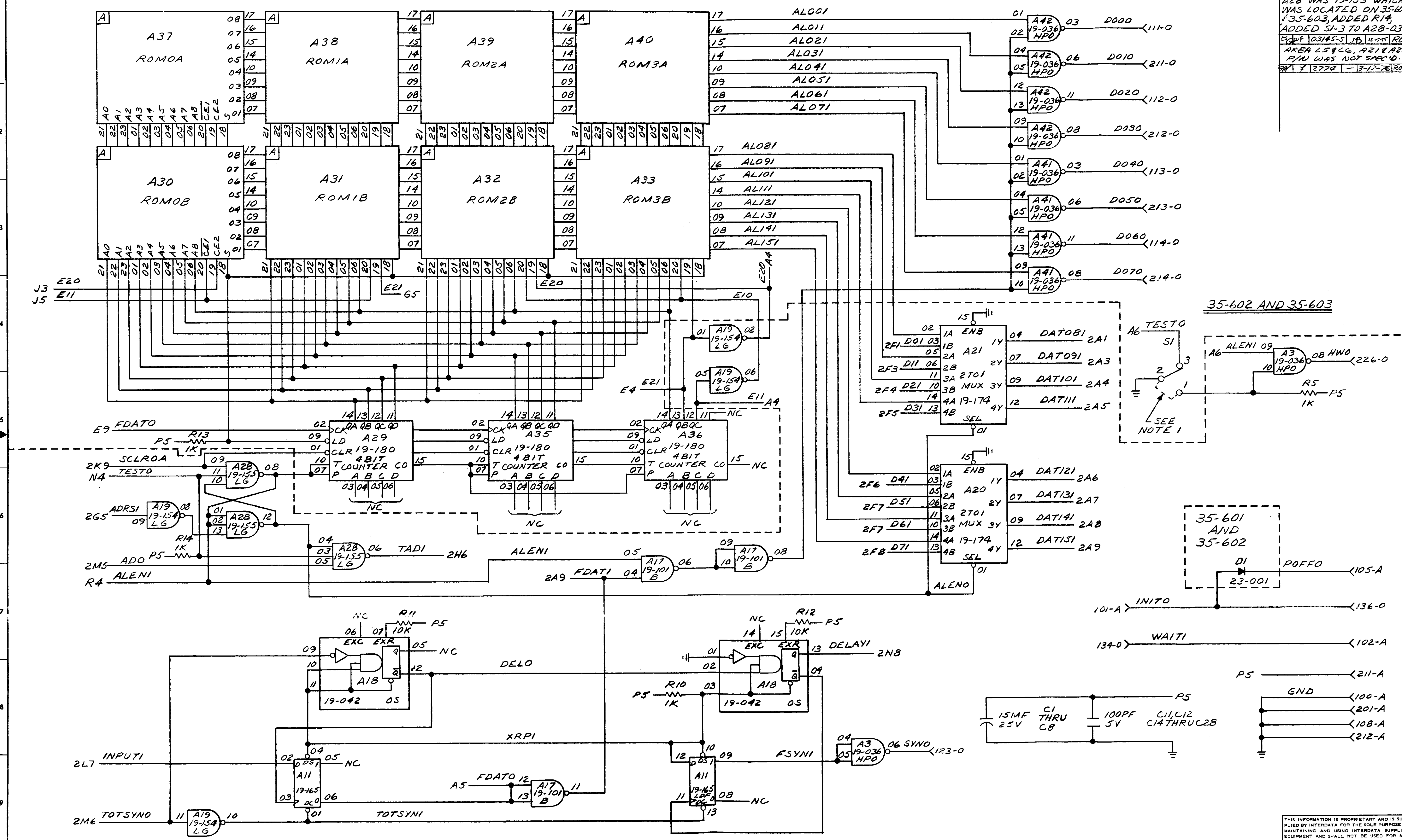
DWG NO. 02-405R01D08

SHEET 2 OF 3

BRUNING 44-231 24538

INTERDATA®
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS				
A28 WAS 19-153 WHICH WAS LOCATED ON 35-602 & 35-603, ADDED R14, ADDED S1-3 TO A28-03				
B	03145-5			R01
AREA L5 & L6, A21 & A20 P/N WAS NOT SPEC'D.				
	2774	–	3-17-76	R02



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NOTES

1. STRAP CONNECTIONS S1-1&2 FOR 35-601 ONLY
2. ROM0A-ROM3A, ROM0B-ROM3B INDICATES LOCATIONS FOR CUSTOM WRITTEN PROM, THEY MAY OR MAY NOT BE EQUIPPED.
3. UNLESS OTHERWISE SPECIFIED ALL COMPONENTS ON THIS SHEET ARE LOCATED ON 35-601, 35-602 & 35-603

SCALE– NAME: B. GRAY

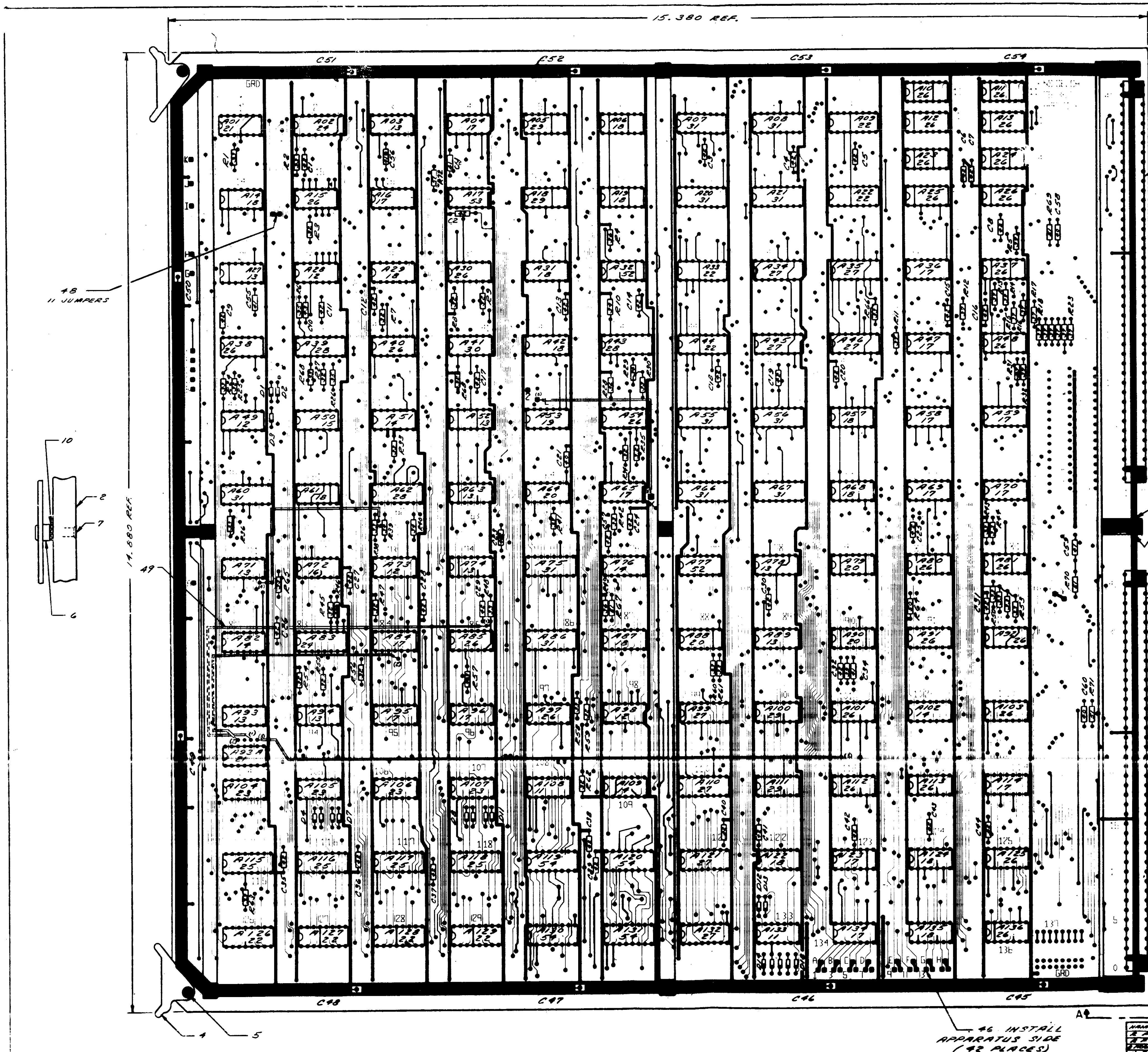
TITLE: DISPLAY CONTROLLER

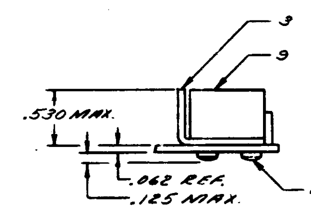
TASK NO. 03145
DWG NO. 02-405R02D08
SHEET 3 OF 3

BRUNING 44-231 24538

RELEASED FOR PRODUCTION
MFG. ENG. [signature] DATE [illegible]

REVISIONS					
ADDED R72 & C61					
PC	[illegible]	2119	[signature]	3-14-74	R01
ADDED STRAPS 1, 2 & 3. REVISE TO REFLECT R02 COPPER					
PC	[illegible]	2132	[signature]	4-16-74	R02
ADDED: STRAPS 4 & 5					
[illegible]	[illegible]	2197	[signature]	[illegible]	R03





PARTIAL VIEW A-A

NOTES:

1. UNLESS OTHERWISE SPECIFIED ALL DIODES ARE ITEM 44.
2. STIFFENER BAR (ITEM 3) TO BE SOLDERED TO GROUND BUS AT 2 END POINTS AND CENTER POINT.
3. CONNECTOR PINS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.

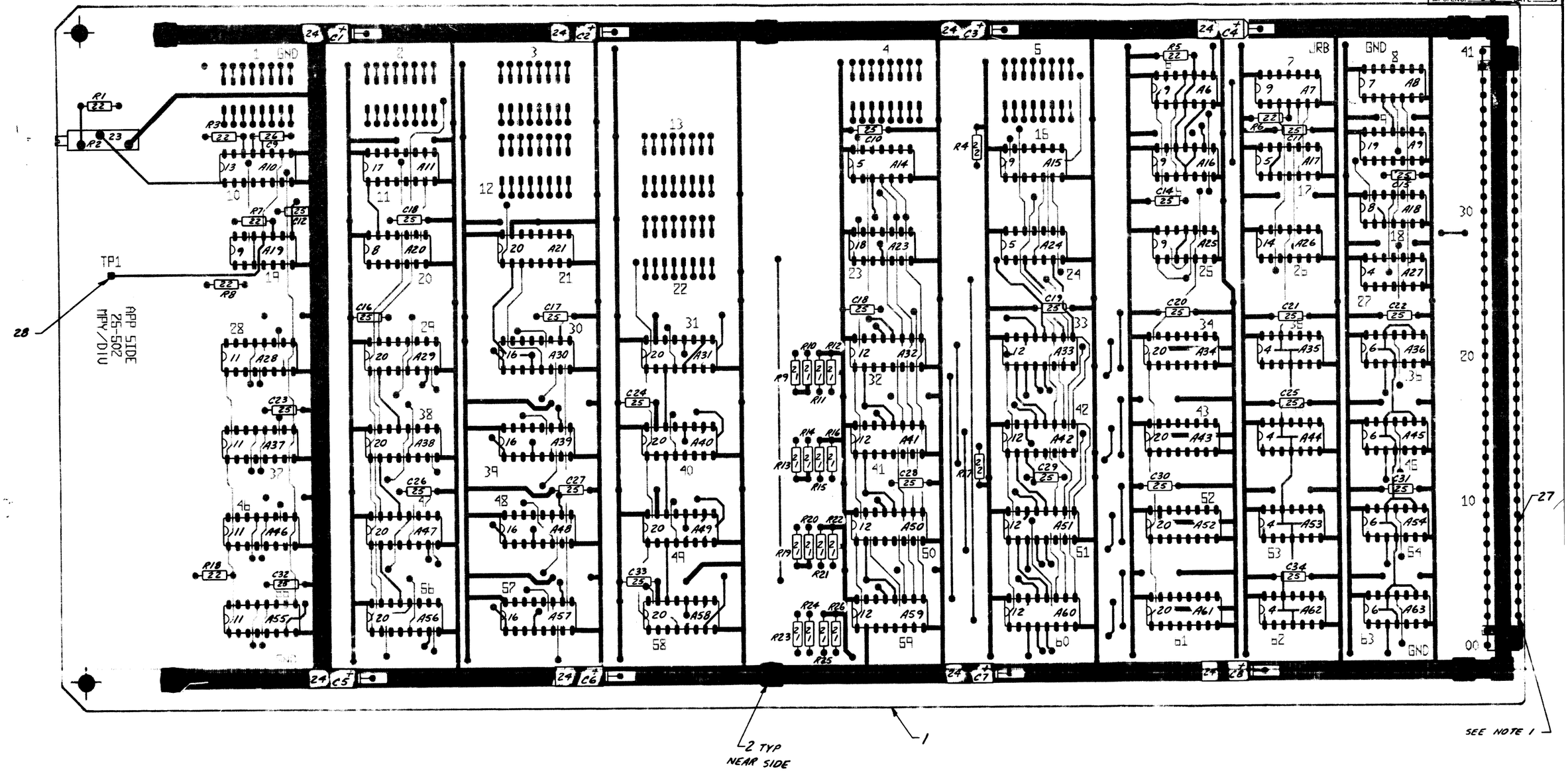
COMPONENT	REF. DESIGNATION
CAPACITOR	C1-21 & 23-60
RESISTOR	R1-36, 38-65 & 67-71
DIODE	D1 THRU D18
IC	A01 THRU A136 & 93A

LAST STRAP NO. 15 (5)

SCALE 2:1

NAME	TITLE	DATE		
R. F. CERO	DRAFT	1-15-73	ASSEMBLY N.S. SELECTOR CHANNEL	
R. F. CERO	CHECK	[illegible]		
[illegible]	[illegible]	[illegible]		
N. ROSS	[illegible]	[illegible]	03078	SHEET 1 OF 1
R. E. JONES	[illegible]	[illegible]	[illegible]	

PRE PRODUCTION APPROVAL	INIT	DATE
	DEV	
	PROD	
RELEASED FOR PRODUCTION		
MFG. ENG.		DATE



NOTES:
1. PINS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.

RESISTORS	R1-R26
CAPACITORS	C1-C34
I.C.s	A6-A11, A14-A21, A23-A63

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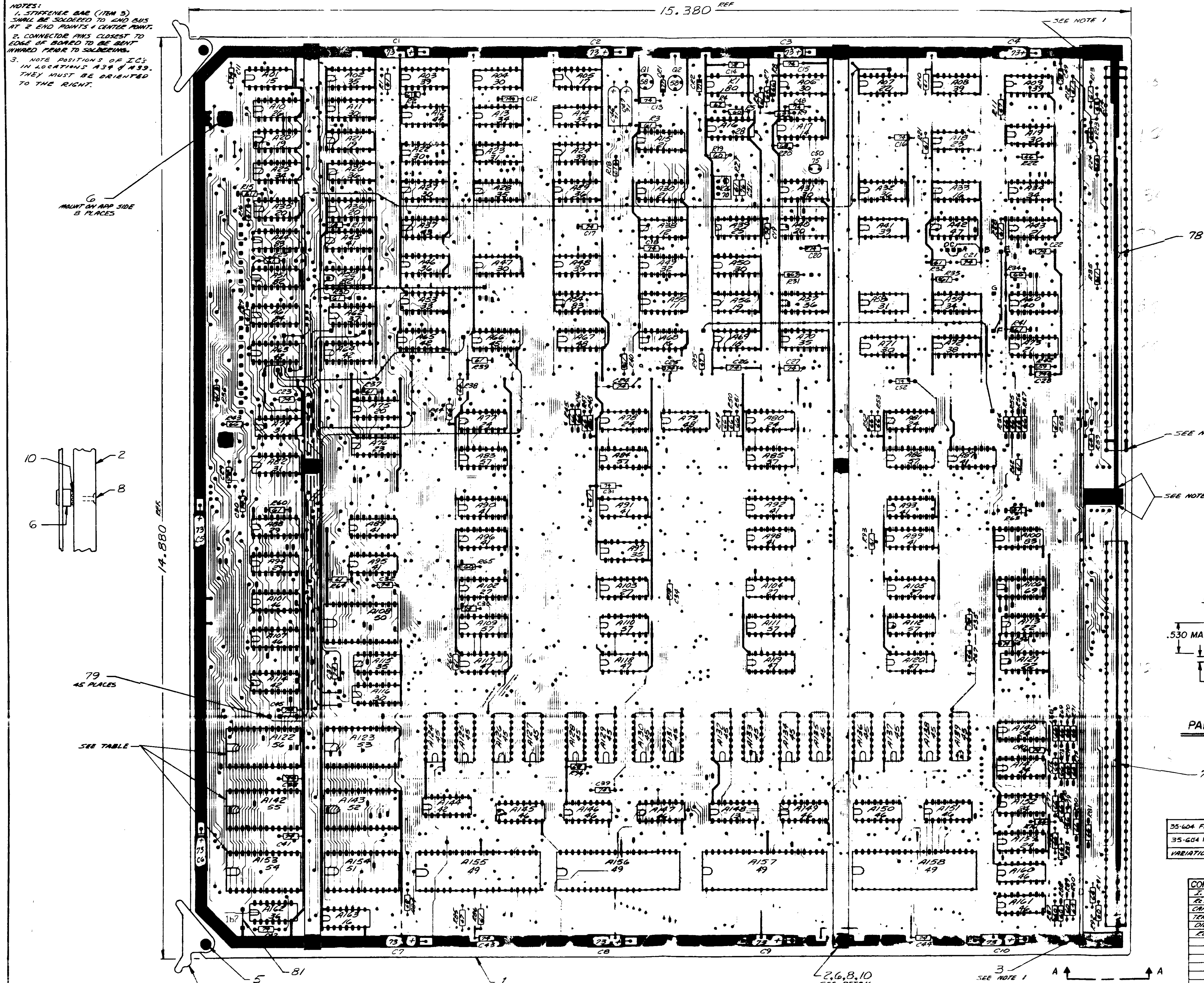
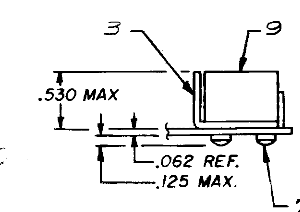
J.A. BIELSKIE	DRAFT.	9-16-75	ASSEMBLY MULTIPLY/DIVIDE 6/16R	
N. MATTER	CHK.	12-16-75		
O. FRANKENBERGER	ENG.	12-16-75		
R. BARKER	Q.C.	12-16-75	03145	SH. OF 1-1
S. MESSINA	MGR.	12-16-75	35-605 003	

NOTES:
1. STIFFENER BAR (ITEM 3) SHALL BE SOLDERED TO END BUS AT 2 END POINTS & CENTER POINT.
2. CONNECTOR PINS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.
3. NOTE POSITIONS OF IC'S IN LOCATIONS A34 & A39. THEY MUST BE ORIENTED TO THE RIGHT.





PARTIAL VIEW A-A

REVISIONS		
PRE PRODUCTION APPROVAL	DEV DJF	11/21/75
	PROD	11/21/75

A16 WAS SPEC AS ITEM # 17. A97 WAS SPEC AS ITEM # 17. A116 WAS SPEC AS ITEM # 33. R93 WAS SPEC AS ITEM 61. C31 C33 C52 & R61 WERE NOT SPEC.

	DJF	05148-2		12-11-75	R01

RELEASED FOR PRODUCTION
MFG. ENG. MB DATE 12-16-75

VARIATION	DESCRIPTION
35-604 F02	AS SHOWN
35-604 F01	AS SHOWN LESS ITEMS 54, 55 & 56

COMPONENT	REF DESIGNATION
I.C.	A01 THRU A163
RESISTOR	R1 THRU R95
CAPACITOR	C1 THRU C52
TRANSISTOR	Q1 & Q2
DIODE	CR1 & CR2
RELAY	K1

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NAME	TITLE	DATE
V. PERRI	DRAFT	11-17-75
R. CERO	CHK	12-16-75
I. LEMAIR	ENGR.	12-16-75
R.A. BARKER	Q.C.	12-16-75
D. FORNENBURGER	MGR	12-16-75

TITLE: PRT. CKT ASSEMBLY 6/16 CPU

03145

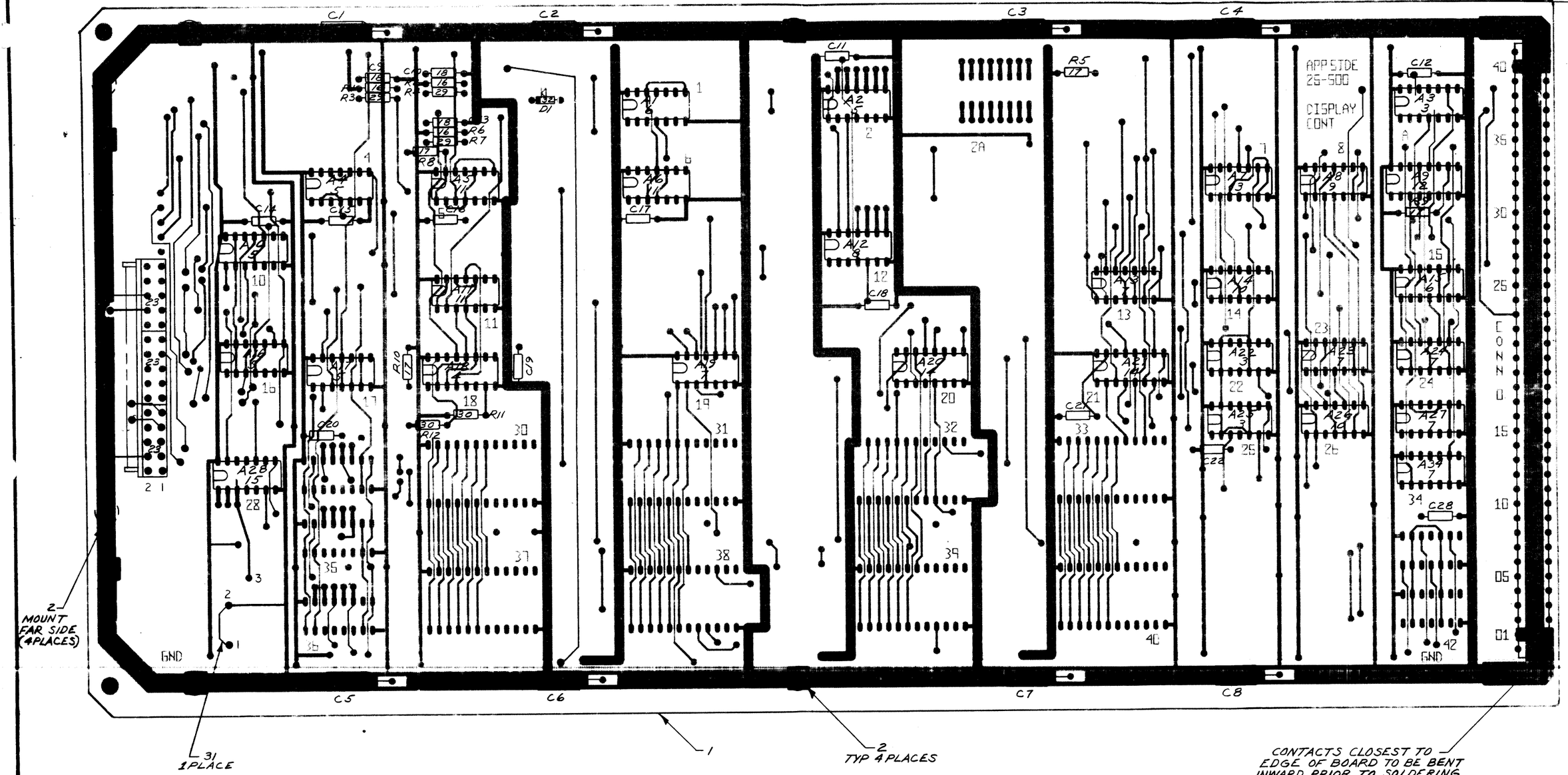
35-604 R01 F03

SHT OF 1-1

C-01

PRE PRODUCTION APPROVAL	INIT	DATE
	DEV	12-15-75
	PROD	

RELEASED FOR PRODUCTION
MFG. ENG. JB DATE 12-16-75



(APP SIDE)

NOTE:
UNLESS OTHERWISE SPECIFIED ALL CAPACITORS ARE ITEM 20

REVISIONS			
REVISIED DRAWING TO REFLECT NEW COPPER, ADDED A28 ITEM 15			
ECO	03145-S	MB	12-15-75	R01

COMPONENT	REF DESIGNATION
ICS	A1, A2, A3 THRU A27, A34
RESISTORS	R1 THRU R12
CAPACITORS	C1 THRU C22, C28
DIODE	D1
SWITCH	S1

B. GRAY	DRAFT	9-23-75	TITLE
R. CERO	CHK	10-8-75	ASSEMBLED PRINTED CIRCUIT DISPLAY CONTROLLER LESS ALO
D.FRANKENBERGER	ENG	12-16-75	
R. BARKER	QC	12-16-75	
S. MESSINA	MGR	12-16-75	
			TASK NO. 03145
			35-601R01 D03
			SHEET 1-1

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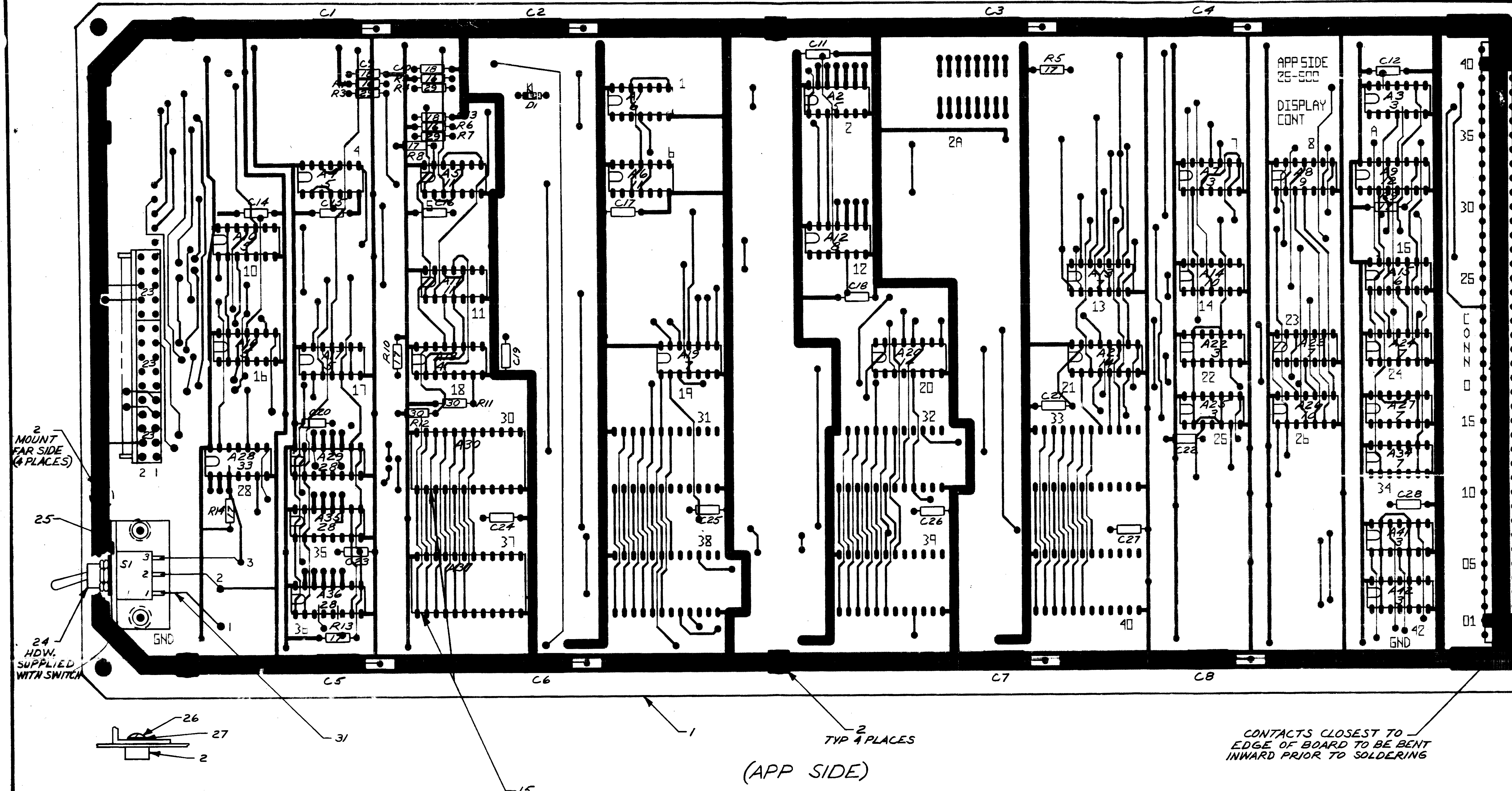
PRE PRODUCTION APPROVAL	INIT	DATE
DEV	[illegible]	10-[illegible]
PROD	[illegible]	[illegible]

RELEASED FOR [illegible]

MFG. ENG. MB DATE 12-16-75



(APP SIDE)

NOTE:
UNLESS OTHERWISE SPECIFIED ALL CAPACITORS ARE ITEM 20

REVISIONS	COMPONENT	REF DESIGNATION
A28 WAS ITEM 6, ITEM 15 WAS 8 PLACES, ADDED R14 ITEM 17, REVISIED DRAWING TO REFLECT NEW COPPER	ICS	A1, A2, A3 THRU A29, A34, A35, A36, A41, A42
	RESISTORS	R1 THRU R14
	CAPACITORS	C1 THRU C28
	DIODE	D1
G DF 03145-5 MB 12-15-75 R01	SWITCH	S1

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B. GRAY	DRAFT	9-17-75	TITLE ASSEMBLED PRINTED CIRCUIT DISPLAY CONTROLLER W/ALO
R. CERO	CHK	10-8-75	
D. FRANKENBERGER	ENG	12-16-75	
R. BARKER	QC	12-16-75	
S. MESSINA	MGR	12-16-75	PASR NO. 03145
			35-602R01D03 SHEET 1-1

PRE PRODUCTION APPROVAL	INIT	DATE
	DEV ENG	10-8-75
	PROD	
RELEASED FOR PRODUCTION		
MFG. ENG.		DATE 12-16-75

C1 C2 C3 C4

APP SIDE 25-500 DISPLAY CONT

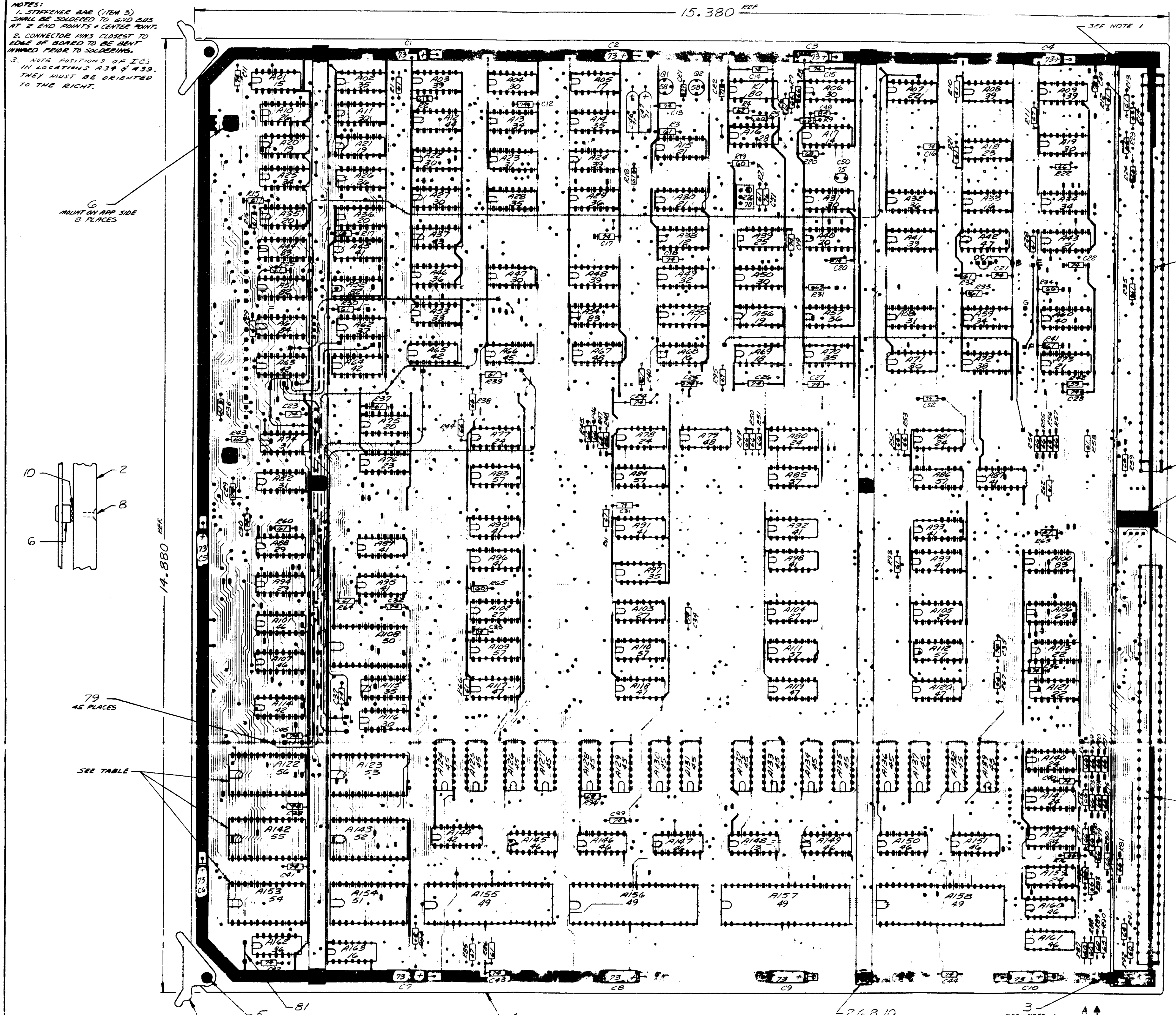
2 MOUNT AR SIDE (4 PLACES)

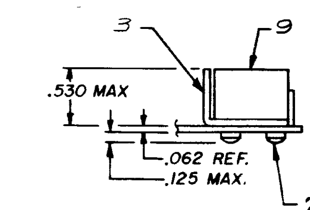
25

S1

CONN D

NOTES:
1. STIFFENER BAR (ITEM 3) SHALL BE SOLDERED TO GND BUS AT 2 END POINTS & CENTER POINT.
2. CONNECTOR PINS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.
3. NOTE POSITIONS OF IC'S IN LOCATIONS A34 & A39. THEY MUST BE ORIENTED TO THE RIGHT.





PARTIAL VIEW A-A

REVISIONS

PRE PRODUCTION APPROVAL — DEV DJF — PROD

A16 WAS SPEC AS ITEM # 12.
A97 WAS SPEC AS ITEM # 12.
A116 WAS SPEC AS ITEM # 32.
R95 WAS SPEC AS ITEM 61
C31 C33 C52 & R61 WERE NOT SPEC.

RELEASED FOR PRODUCTION — MFG. ENG. MB — DATE

AREA A06, C48 ITEM NUMBER WAS 74.

ECR 2773

35-604 F02	AS SHOWN
35-604 F01	AS SHOWN LESS ITEMS 54,55&56
VARIATION	DESCRIPTION

COMPONENT	REF DESIGNATION
I.C.	A01 THRU A163
RESISTOR	R1 THRU R95
CAPACITOR	C1 THRU C52
TRANSISTOR	Q1 & Q2
DIODE	CR1 & CR2
RELAY	K1

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NAME	TITLE	DATE
V. PERRI	DRAFT	11-17-75
R. CERO	CHK	12-16-75
I. LEMAIR	ENGR.	12-16-75
R.A. BARKER	Q.C.	12-16-75
D. FRANKENBERGER	MGR	12-16-75

TITLE: PRT. CKT ASSEMBLY 6/16 CPU

03M5 — 35-604 R02M03 — SHT OF 1-1

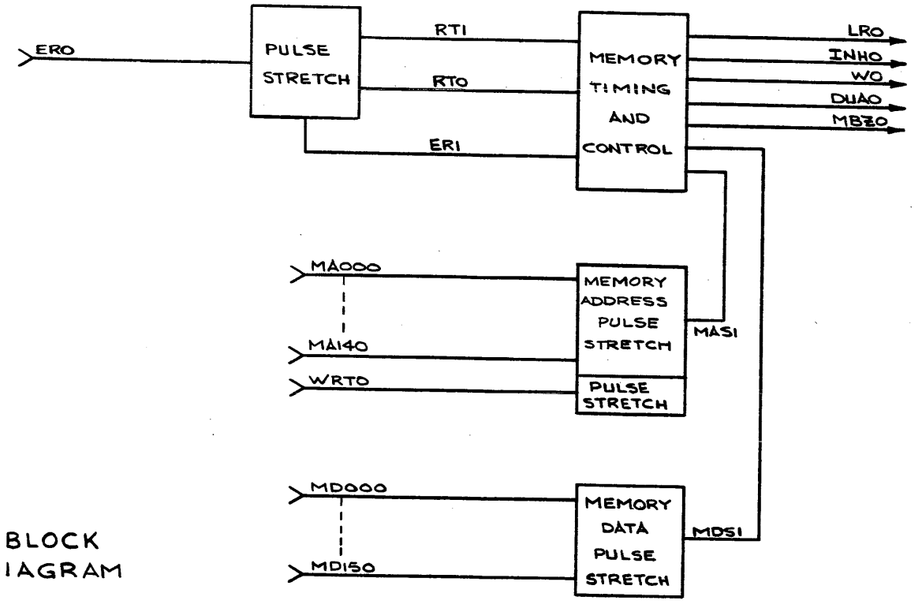
INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS			
INITIAL ISSUE R01			
09		12-08-75	R01

	INIT.	DATE
PRE PRODUCTION APPROVAL	DEV	12-8-75
	PROD	3-31-76

RELEASED FOR PRODUCTION
MFG. ENG. [signature] DATE 4-9-76

BLOCK DIAGRAM



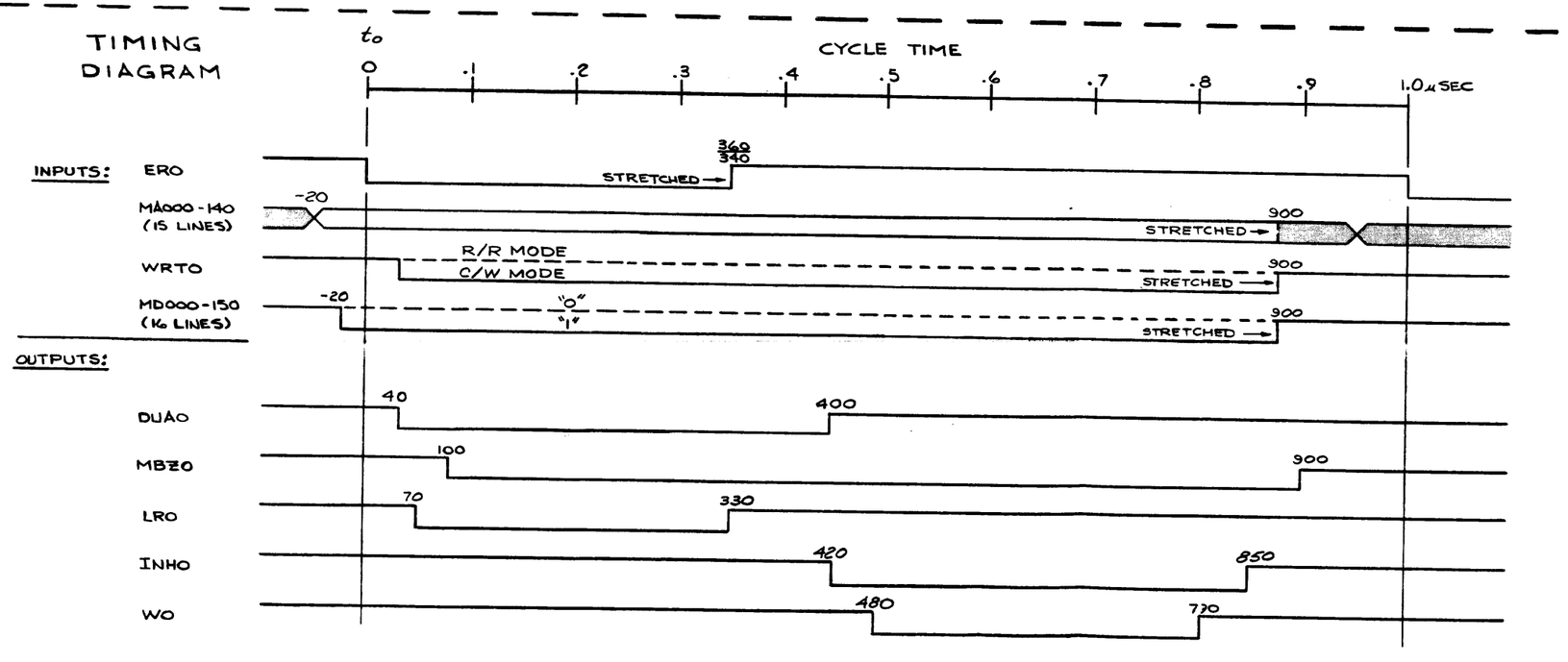
THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT.

BOARDS AGREEING WITH THIS SCHEMATIC MUST BE AT LEAST THE FOLLOWING REVISION LEVEL

BOARD	REV
35-608	R01

ROW 1	ROW 2	TERM NO.	J0ZN
P5	GND	41	
	GND	40	
		39	
		38	
MD150		37	
MD130	MD140	36	
MD110	MD120	35	
MD090	MD100	34	
MD070	MD080	33	
MD050	MD060	32	
MD030	MD040	31	
MD010	MD020	30	
	MD000	29	
		28	
WRTO		27	
		26	
		25	
		24	
		23	
		22	
		21	1
		20	
		19	
		18	
		17	
		16	
		15	
		14	
		13	
		12	
		11	
		10	
		09	
		08	
		07	
		06	
	MA00	05	
INHO	ERO	04	
WO	LRO	03	
		02	
GND	GND	01	
P5	GND	00	
P5	GND	41	
GND	GND	40	
		39	
		38	
		37	
		36	
DUAO	MBZO	35	
		34	
MA130	MA140	33	
MA110	MA120	32	
MA090	MA100	31	
MA070	MA080	30	
MA050	MA060	29	
		28	
		27	
		26	
		25	
		24	
		23	
		22	
		21	0
		20	
		19	
		18	
		17	
		16	
		15	
		14	
		13	
		12	
		11	
MA030	MA040	10	
MA020	MA021	09	
MA01	MA02	08	
MA010		07	
MA000		06	
	MA00	05	
INHO	ERO	04	
WO	LRO	03	
		02	
GND	GND	01	
P5	GND	00	

TIMING DIAGRAM



NOTES:
1. SHADED AREA (▨) INDICATES "CAN CHANGE" OR "DO NOT CARE" INTERVAL.
2. UNLESS INDICATED OTHERWISE THE TIME IS IN NANOSECONDS.
3. THE NUMBER ABOVE THE LINE INDICATES - MAXIMUM TIME.
   THE NUMBER BELOW THE LINE INDICATES - MINIMUM TIME.
4. ALL SIGNAL INDICATED ARE OF STANDARD "TTL" LEVELS AND TIMING IS REFERENCED TO 1.5 V LEVEL.

SCALE–	NAME	TITLE	DATE
TOLERANCE: XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	C. JENSEN	DRAFT	18 SEPT 75
	H. MATTER	CHK	3-31-76
	P. OBRDA	ENGR	3-31-76
	R. BARKER	Q.C.	3-31-76
	S. MESSINA	MGR	3-31-76

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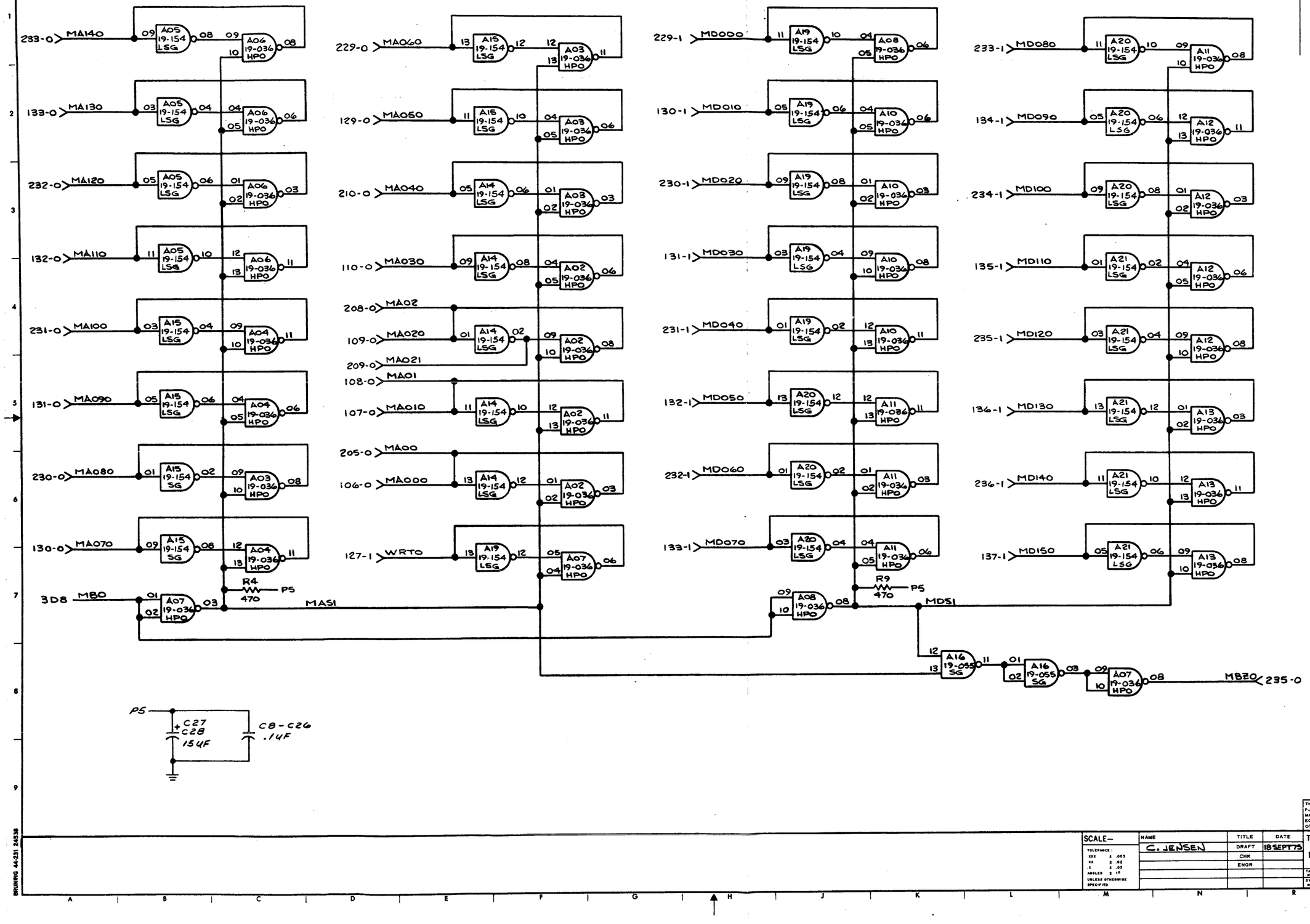
TITLE FUNCTIONAL SCHEMATIC
MEMORY ADAPTER

TAPE NO. 03141 | SHEET OF 1 – 3
DWG NO. 35-608 R01 D08

BRUNING 44-231 24538

REVISIONS



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SCALE—	NAME	TITLE	DATE
TOLERANCE: XXX ± .005, XX ± .02, X ± .03, ANGLES ± 1° UNLESS OTHERWISE SPECIFIED	C. JENSEN	DRAFT	18SEPT73
		CHK	
		ENGR	

TITLE FUNCTIONAL SCHEMATIC
MEMORY ADAPTER

TABS NO. 03048 SHEET OF 2-3
DWG NO. 35-608 R01D08

BRUNING 44-231 24538

INTERDATA
2 Crescent Place, Oceanport, New Jersey 07757

REVISIONS

INH0 <104-0

P5
R3 470
NC
R17 4.7K
A18 19-042 ONE SHOT
C6 68PF ±1%
R15 10K
R11 10K
A09 19-042 ONE SHOT
A01 19-055 SG
R1 100
C1 330PF
C7 68PF ±1%
R16 6.8K
R12 5K
A09 19-042 ONE SHOT
A01 19-055 SG
W0 <103-0
XRP
204-0 >ERO
A08 19-034 HPO
R7 470
ERI
C4 68PF ±1%
R8 7.5K
R10 5K
A17 19-042 ONE SHOT
A08 19-034 HPO
RT1
RTO
A16 19-055 SG
R2 100
C2 330 PF
LRO <203-0
C3 150PF ±1%
R6 47K
R5 20K ±1%
A17 19-042 ONE SHOT
MB0 2A7
C5 68PF ±1%
R13 22K
R14 22K
A18 19-042 ONE SHOT
A07 19-034 HPO
DUA0 <135-0

NOTES:
1. UNLESS OTHERWISE SPECIFIED:
   a) RESISTORS ARE ±5%, 1/4W
   b) CAPACITORS ARE ±10%.

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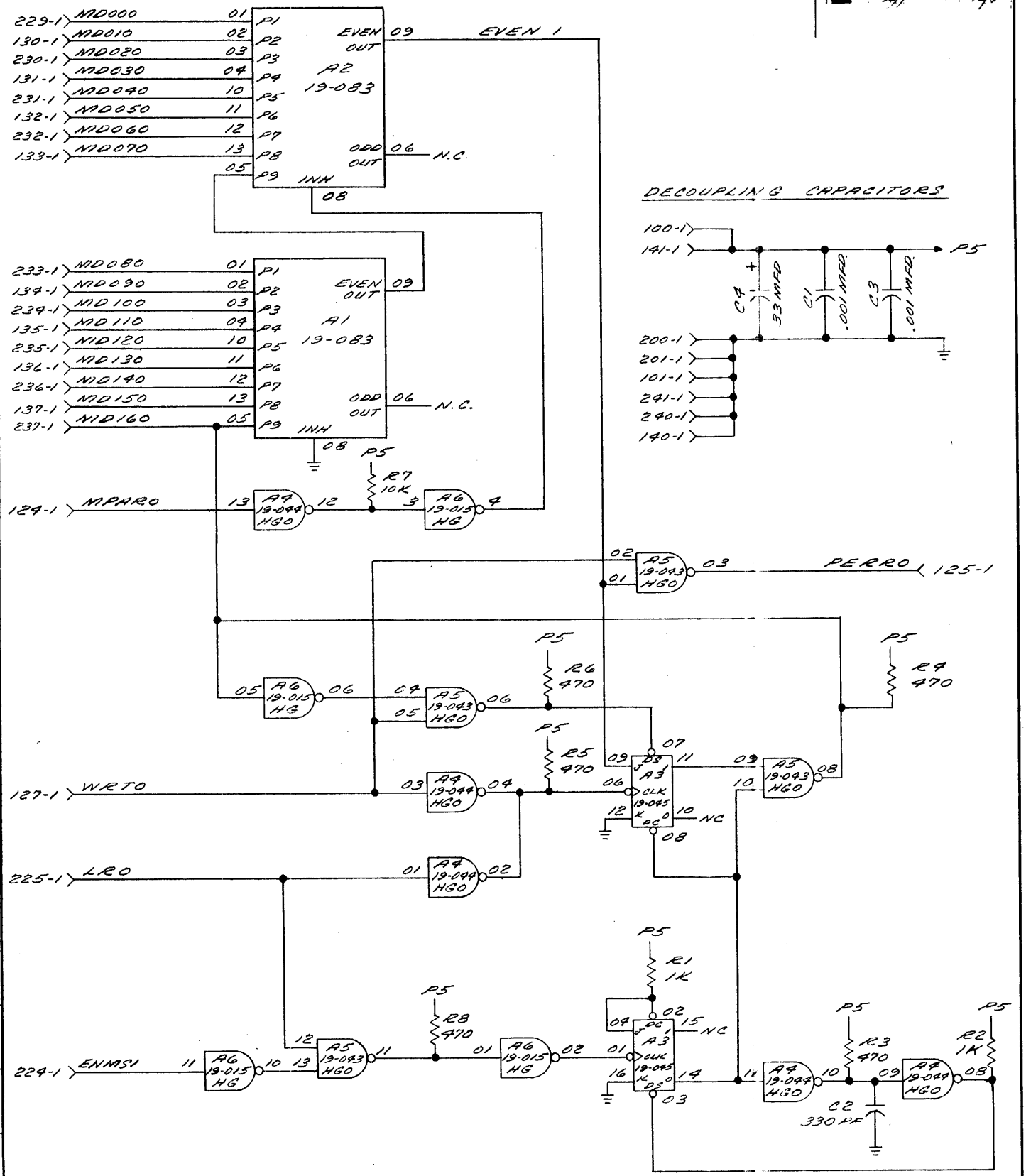
SCALE–	NAME	TITLE	DATE
TOLERANCE XXX ± .005, XX ± .02, X ± .05, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED	C. JENSEN	DRAFT	18 SEPT 75
		CHK	
		ENGR	

TITLE FUNCTIONAL SCHEMATIC
MEMORY ADAPTER

TASK NO. 03048
DWG NO. 35-608 Rev D08
SHEET 3 OF 3

BRUNING 44-231 24538



NOTES
1. UNLESS OTHERWISE SPECIFIED ALL APPARATUS THIS SHEET LOCATED ON 35-368.
2. THIS OPTION, WHEN EQUIPPED IS INSTALLED AT THE BACKPANEL ON SLOT 3, CONNECTOR 1.

NAME	TITLE	DATE
R F CERO	DRAFT	11-1-74
R F CERO	CHK	11-1-74
G JOYCE	ENGR	12-5-74
S MALLORY	QC	12-5-74
D FRANKENBERGER	MGR	12-5-74

TITLE SCHEMATIC PARITY OPTION BOARD 9/32
TASK NO. 03132
DWG. NO. 02-368 C08
SHEET 1 OF 1

D D & W REPROGRAPHICS 40059-3

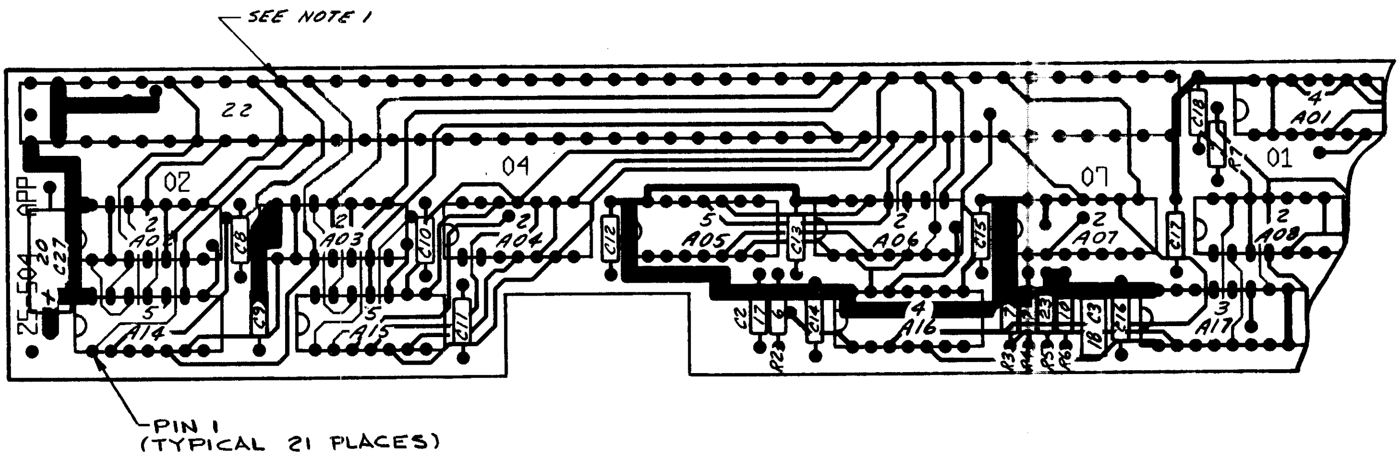
INTERDATA

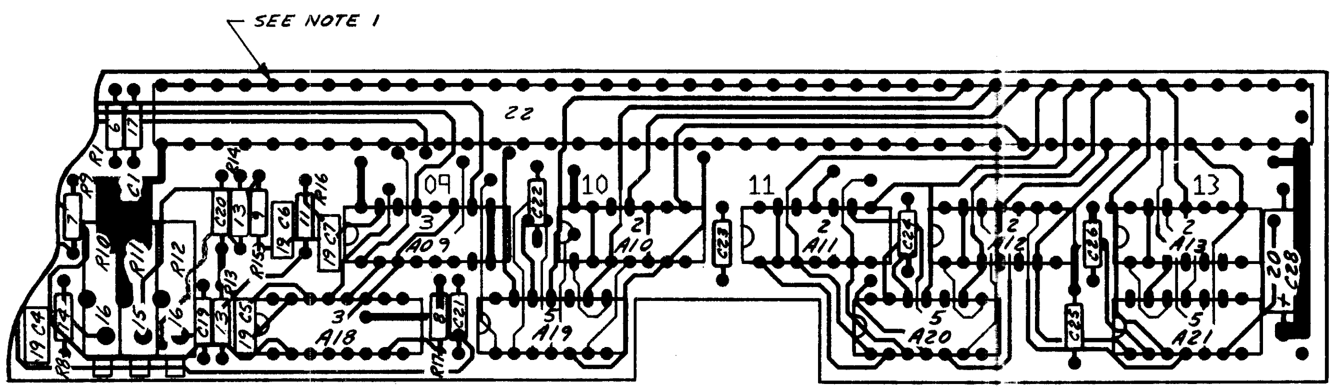
REVISIONS			
INITIAL ISSUE R01			
	—	12-23-75	R01

PRE PRODUCTION APPROVAL	INIT.	DATE
DEV		2-5-76
PROD		2/5/76

RELEASED FOR PRODUCTION
MFG. ENG. [signature] DATE 4-9-76

NOTES:
1. PINS CLOSEST TO EDGE OF BOARD TO BE BENT INWARD PRIOR TO SOLDERING.
2. ALL UNMARKED CAPACITORS TO BE ITEM 21.





CAPACITORS	C1-C28
I.C.'s	A01-A21
RESISTORS	R1-R17
COMPONENT	REF. DESIGNATION

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SCALE– 2:1

TOLERANCE: .XXX ± .005, .XX ± .02, .X ± .03, ANGLES ± 1°, UNLESS OTHERWISE SPECIFIED

NAME	TITLE	DATE
J.R. BIELSKIE	DRAFT	10-1-75
H. MATTER	CHK	12-30-75
P. OBRDA	ENGR	3-31-76
R. BARKER	Q.C	3-31-76
S. MESSINA	MGR	3-31-76

TITLE ASSEMBLY MEMORY ADAPTER

TASK NO. 03141

DWG. NO. 35-608 R01 C03

SHEET OF 1 — 1