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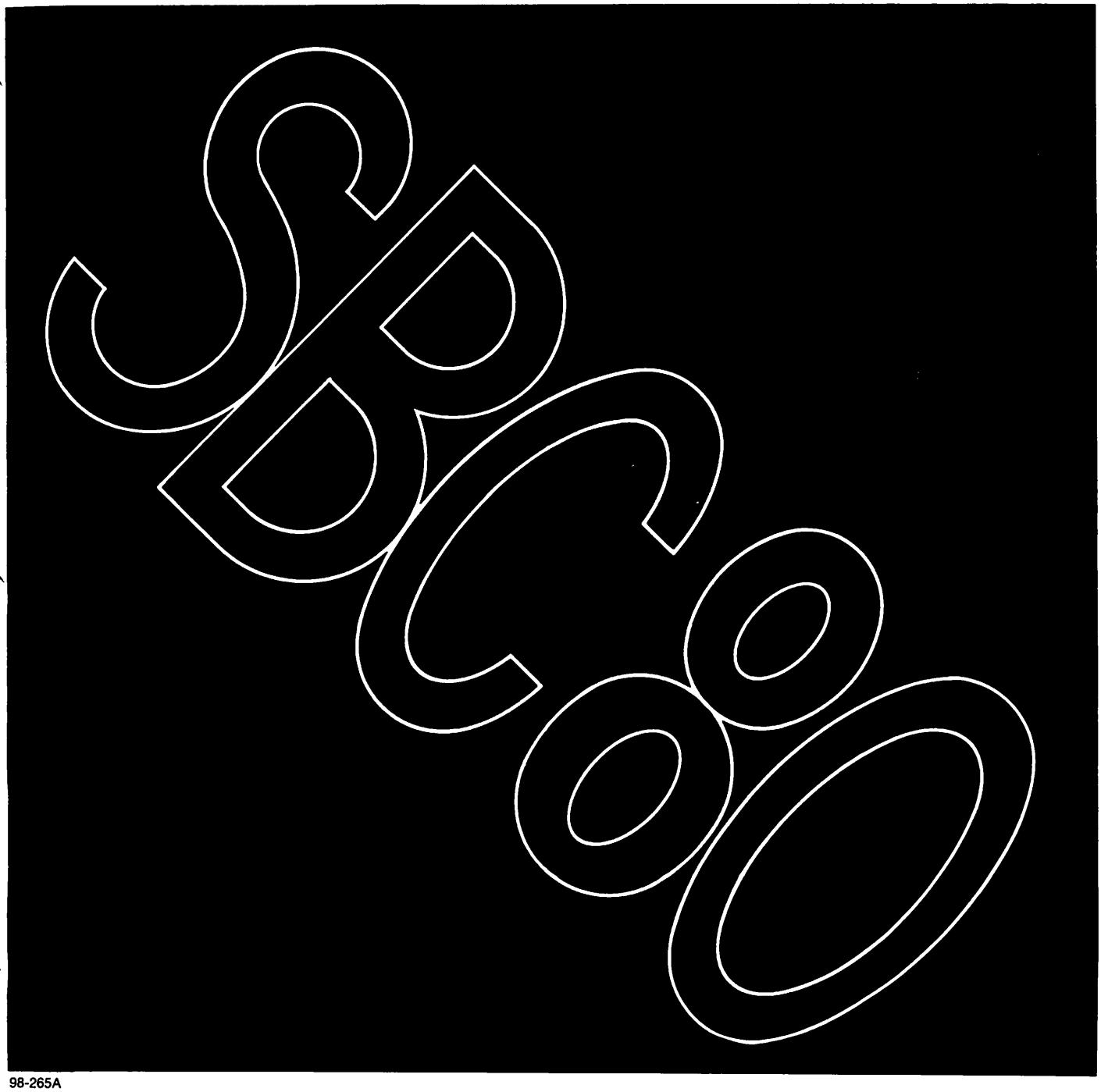
SBC 416 16K PROM/ROM EXPANSION BOARD HARDWARE REFERENCE MANUAL



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SBC 416
16K PROM/ROM BOARD
HARDWARE REFERENCE MANUAL

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98-265A

SBC 416

16K PROM/ROM EXPANSION BOARD

HARDWARE REFERENCE MANUAL

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16K PROM/ROM BOARD

The PROM/ROM Board has been designed to provide up to 16,384 (16K) X 8-bit words of PROM/ROM storage for 8-bit computer systems or 8,192 (8K) X 16-bit words of storage for 16-bit computer systems. Up to sixteen 8708 erasable and electrically programmable read-only-memory (PROM) devices can be inserted on the board. Each PROM provides 1024 X 8 bits of storage.

Intel's 2708 PROMs or 8308 ROMs can also be used on the board in place of the 8708s. The 16 PROM elements are organized into two 8K memory banks. The address range of each bank can be set independently. Each bank can occupy any address block within the maximum 64K range. The selected address block must, however, begin on 8K boundary.

The address assigned to the two banks on the board can coincide. This configuration can be used to implement 8,192 X 16-bit PROM storage capacity. This capability is implemented on a single 12 in. X 6.75 in. printed circuit board. The SBC 416 requires DC power at levels of +5VDC, +12 VDC and -5VDC.

This manual is supplemental to the SBC 80 series of OEM Hardware Reference Manuals (e.g., SBC 80/10 Hardware Reference Manual, 98-230).

1.0 FUNCTIONAL ORGANIZATION

For descriptive purposes, the 16K PROM/ROM board can be viewed as consisting of four functional blocks:

Memory storage block
Address control block
Timing and control block
Byte selection block

These functional units are illustrated in Figure 1.

The memory storage block consists of up to 16 8708 erasable and electrically programmable-read-only-memory (PROM) elements. Each 8708 stores 1024 X 8 bits of data (8,192 bits). The 16 elements are organized in two switch-selectable banks of 8,192 (8K) X 8 bits of PROM storage.

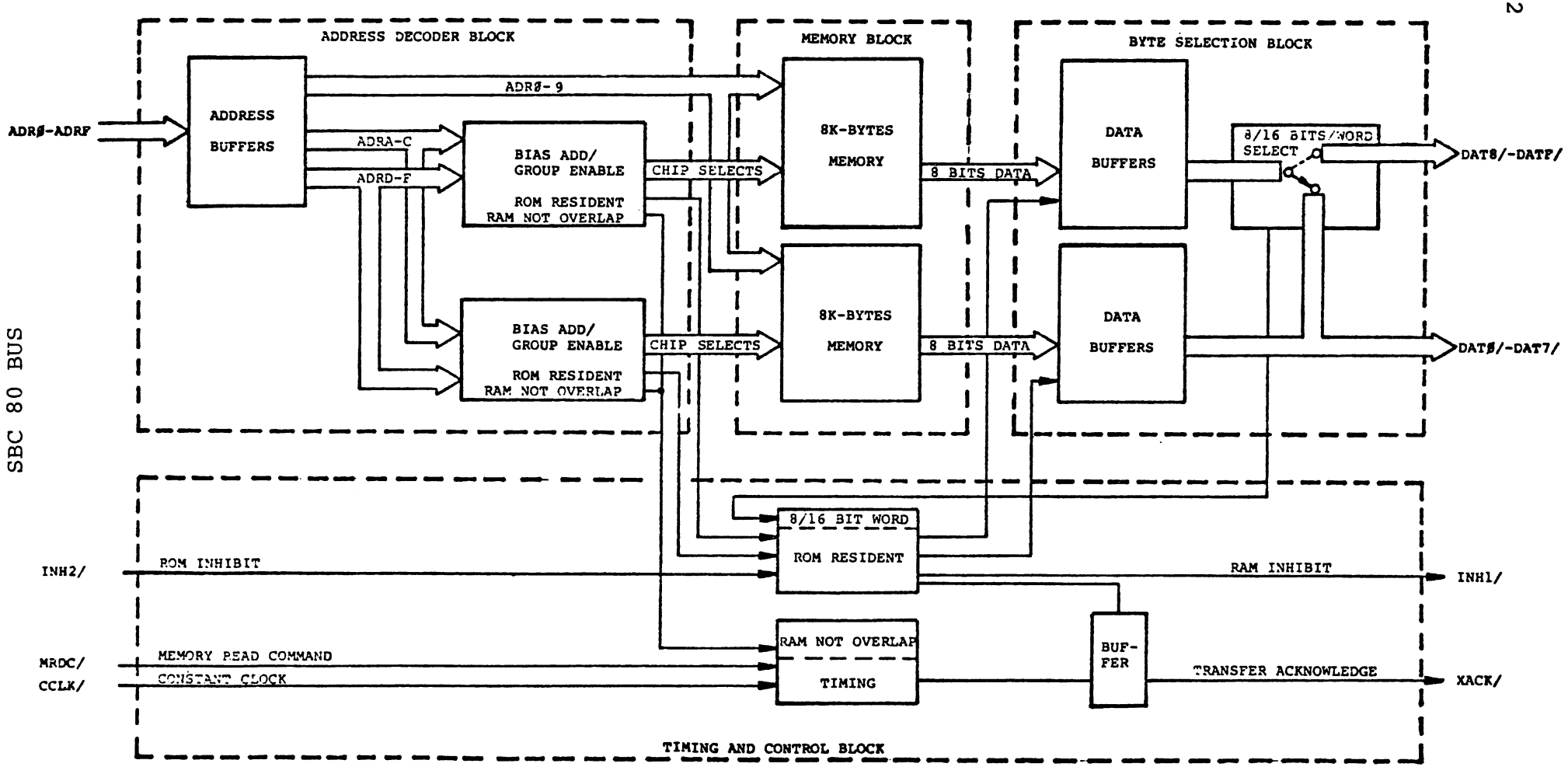


FIGURE 1

FUNCTIONAL BLOCK DIAGRAM

2.0 THEORY OF OPERATION

In this section, we provide a detailed theory of operation description for the 16K PROM/ROM board. Figure 2 shows the printed wiring assembly of the board. The schematic (3 sheets) for the 16K PROM/ROM board is provided in Figure 3 located in Section 2.4.

2.1 PHYSICAL MEMORY IMPLEMENTATION

The actual memory on the 16K PROM/ROM board consists of up to sixteen 8708 programmable-read-only-memory (PROM) elements. Each 8708 element has a 1024 X 8-bit capacity. The 16 PROM elements are partitioned into two memory banks. Each bank includes 8,192 (8K) X 8 bits of storage (8 PROM elements). The address ranges for the two banks are jumper-selectable as described in Section 2.2. In addition, one bank can be used with 8,192 words in the other bank to implement 8K X 16-bit word storage; as previously described.

The 8708 PROMs are shown on sheet 2 of the board schematic, Figure 3. ROM elements 8308 with CS2/ option (negative true chip select 2) may also be used.

2.2 MEMORY ADDRESS DECODING

The address control block is responsible for decoding the 16-bit address output by the CPU during PROM/ROM read operations. These 16 address bits are used as follows: the three highest bits (ADRF, ADRE AND ADRD) are group bias address; the next three bits (ADRC, ADRB, AND ADRA) select 1 of 8 chips in a group; and the remaining 10 bits (ADR9 through ADR0) address one of the 1024 memory locations in a chip.

The memory space of the board is divided into two groups - X group and Y group. The following jumpers and switches are used to select a desired mode of operation.

2.2.1 GROUP BIAS ADDRESS JUMPERS

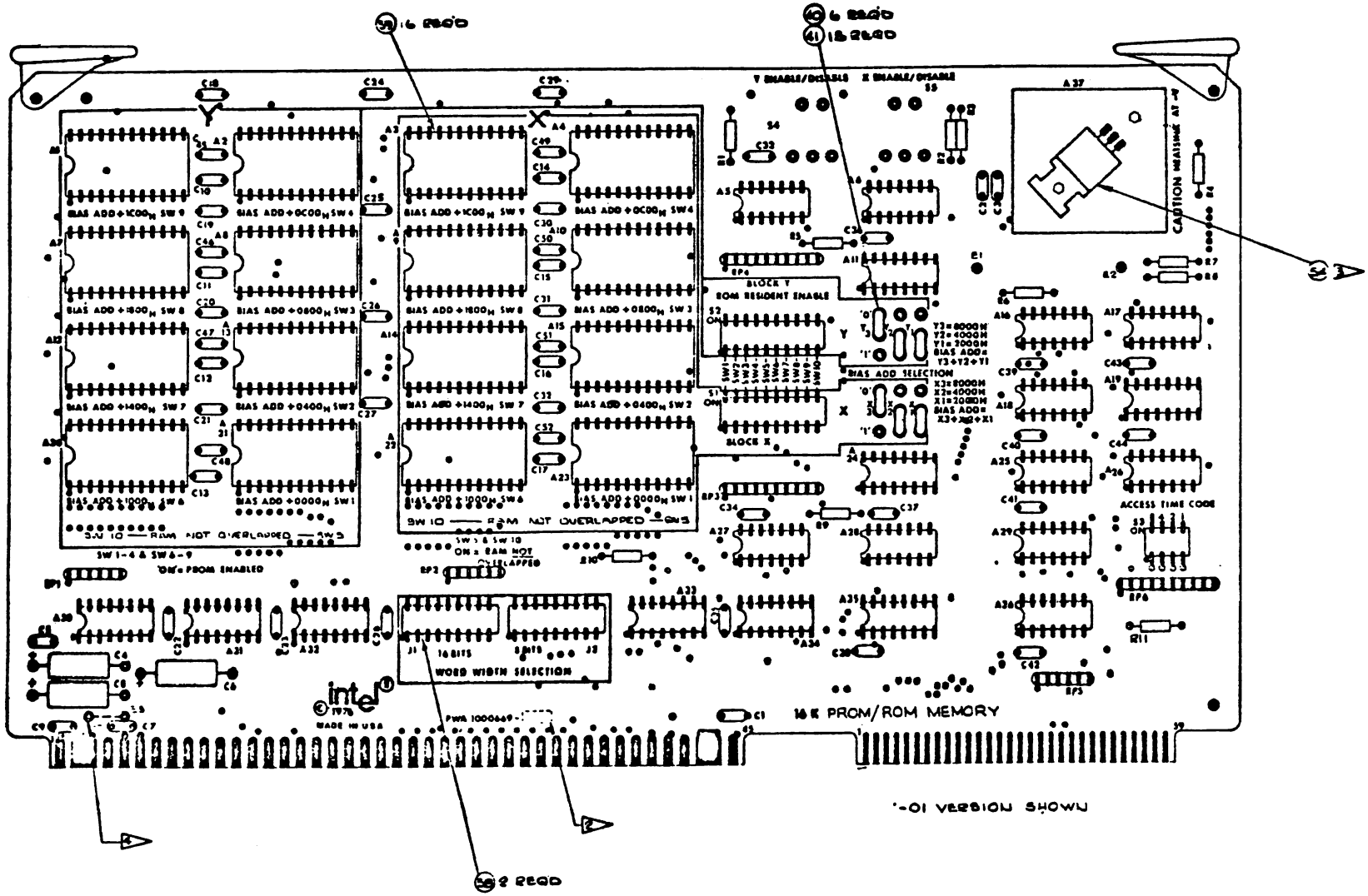
The starting address of X group or Y group is called group bias address. The group bias address is jumper-programmable by setting the jumpers on the jumper pads called "BIASED ADD SELECTION". The bias address of the X group is set by X3, X2 and X1 jumpers, while the bias address of the Y group is set by Y3, Y2 and Y1 jumpers. Selecting 1 or 0 with each jumper determines the value of a group bias address bit. See Table 1 for memory

locations for PROM/ROMs in X-group and Table 2 for PROM/ROM memory locations in Y-group.

Example: To set the group bias address of X group as C000, the jumpers X3, X2 and X1 should be programmed as "1", "1" and "0", respectively, because C000 = 1 (8000) +1 (4000) + 0 (2000). The X group memory space now begins at C000, and ends at DFFF.

Example: To set the group bias address of Y group as E000, the jumpers Y3, Y2 and Y1 should be programmed as "1", "1" and "1", respectively, because E000 = 1 (8000) + 1 (4000) +1 (2000). The Y group memory space then begins at E000, and ends at FFFF.

Note that there are 8 possible group bias addresses that can be selected by the three jumpers. Consequently, the memory space of a group must begin at one of the boundaries 0000, 2000, 4000, 6000, 8000, A000, C000 and E000.



NOTE: UNLESS OTHERWISE SPECIFIED

1. ASSEMBLY NO. IS 1000669-XX.

2 MARK DASH NO. IN POSITION SHOWN.

3 APPLY COMPOUND (ITEM 54) BETWEEN A37 & HEATSINK.

4 STRAP FROM E5-E4 ON -02 VERSION ONLY.

FIGURE 2

* SCHEMATIC - PRINTED WIRING ASSEMBLY
16K PROM/ROM MEMORY BOARD

*NOTE: SBC 416 IS "-02" VERSION

TABLE 1

MEMORY LOCATION OF A PROM/ROM CHIP IN X-GROUP

X-GROUP BIAS ADDRESS	X-GROUP PROM/ROM CHIP SOCKET NUMBER								
JUMPERS: $X_3X_2X_1$	A_{23}	A_{15}	A_{10}	A_4	A_{22}	A_{14}	A_9	A_3	
000	0000	0400	0800	0C00	1000	1400	1800	1C00	
001	2000	2400	2800	2C00	3000	3400	3800	3C00	
010	4000	4400	4800	4C00	5000	5400	5800	5C00	
011	6000	6400	6800	6C00	7000	7400	7800	7C00	
100	8000	8400	8800	8C00	9000	9400	9800	9C00	
101	A000	A400	A800	AC00	B000	B400	B800	BC00	
110	C000	C400	C800	CC00	D000	D400	D800	DC00	
111	E000	E400	E800	EC00	F000	F400	F800	FC00	
	SW1	SW2	SW3	SW4	SW6	SW7	SW8	SW9 ←	"ROM Resident Enable" Switch for X-Group

NOTE: SW5, SW10 are used as "RAM NOT OVERLAPPED" switch.

TABLE 2

MEMORY LOCATION OF A PROM/ROM CHIP IN Y-GROUP

Y-GROUP BIAS ADDRESS JUMPERS: $Y_3Y_2Y_1$	Y-GROUP PROM/ROM CHIP SOCKET NUMBER								
	A_{21}	A_{13}	A_8	A_2	A_{20}	A_{12}	A_7	A_1	
000	0000	0400	0800	0C00	1000	1400	1800	1C00	
001	2000	2400	2800	2C00	3000	3400	3800	3C00	
010	4000	4400	4800	4C00	5000	5400	5800	5C00	
011	6000	6400	6800	6C00	7000	7400	7800	7C00	
100	8000	8400	8800	8C00	9000	9400	9800	9C00	
101	A000	A400	A800	AC00	B000	B400	B800	BC00	
110	C000	C400	C800	CC00	D000	D400	D800	DC00	
111	E000	E400	E800	EC00	F000	F400	F800	FC00	
	SW1	SW2	SW3	SW4	SW6	SW7	SW8	SW9 ←	"ROM Resident Enable" Switch for Y-Group

NOTE: SW5, SW10 are used as "RAM NOT OVERLAPPED" switch.

2.2.2 CHIP SOCKET

The next three address bits indicate one of the eight chip sockets within a group. The location of a chip is determined by the magnitude of the difference between the chip address and the group bias address.

Example: Assume the memory space of a PROM/ROM chip begins at D400, and the group bias address for X group is C000. Then, the difference = D400 - C000 = 1400. This PROM/ROM chip should be located at the chip socket labelled as "BIAS ADD + 1400".

2.2.3 ROM RESIDENT ENABLE SWITCH

When a group bias address is jumper programmed for a group, a memory space of 8K bytes is occupied by the group. For many applications, this memory space is often partially populated by some PROM/ROM chips. For example, only 2K bytes are occupied by two PROM/ROM chips and the other 6K bytes remain unused. It may be desired to allow this unused memory space to be used by other memory types, such as RAM. If a PROM/ROM overlaps a RAM at a specific memory location, the PROM/ROM should take higher priority over RAM. In other words, a memory access to the memory location will access PROM/ROM rather than the overlapped RAM. Therefore, user must indicate to PROM/ROM memory board that there exists a PROM/ROM chip on a specific socket. This is accomplished by setting "ROM RESIDENT ENABLE" switches.

A "ROM Resident Enable" switch number is assigned to each PROM/ROM socket. For example, the socket labelled as "BIAS ADD + 1400" is also labelled with "SW 7". When a PROM/ROM chip is inserted into this socket, the ROM RESIDENT ENABLE switch SW 7 should be set to "ON" position. See Tables 1 and 2.

If a socket is not occupied by a PROM/ROM chip, the associated "ROM RESIDENT ENABLE" switch of the socket should be reset to "OFF" position, for enabling that 1K byte memory space to be used by other types of memory.

2.2.4 RAM NOT OVERLAPPED SWITCH

If a PROM/ROM overlaps a RAM at some memory locations, the PROM/ROM board must be so notified

by resetting the associated "RAM NOT OVERLAPPED" switch.

The SW5 and SW10 "ROM RESIDENT ENABLE" switches are used as "RAM NOT OVERLAPPED" switches. SW5 must be reset to "OFF" position, if PROM/ROM and RAM are overlapped at some memory locations within the 4K byte memory space of the four sockets labelled as:

BIAS ADD + 0000
BIAS ADD + 0400
BIAS ADD + 0800
BIAS ADD + 0C00

SW5 should be set to "ON" position, if PROM/ROM and RAM are not overlapped at any of the memory locations within this memory space.

Similarly, SW10 must be reset to "OFF" position, if PROM/ROM and RAM are overlapped at some memory locations within the 4K byte memory space of the four sockets labelled as:

BIAS ADD + 1000
BIAS ADD + 1400
BIAS ADD + 1800
BIAS ADD + 1C00

SW 10 should be set to "ON" position, if PROM/ROM and RAM are not overlapped at any of the memory locations within this memory space.

2.2.5 WORD WIDTH SELECTION PLUG

If the "Word Width Selection" plug is inserted at J1, the board is operated at 16 bit mode. Two bytes will be delivered to the data bus for each read operation. If the "Word Width Selection" plug is loaded at J2, the board is operated at 8 bit mode. One byte will be delivered to the data bus for each read operation.

When the board is programmed at 16 bit mode, the "Group Bias Address", of X group and Y group must be identical. Otherwise, the board will not respond to a read access.

2.2.6 GROUP ENABLE/DISABLE SWITCH

The X group and Y group of PROM/ROM can be enabled or disabled by flipping two switches. These two

switches are not physically mounted on the board. If this feature is required, a switch of "C K" part no. 101A can be installed on the board area designated as "S4" and "S5". If the switch is at DISABLE position, the board will not respond to a read access to any memory location within the group.

2.3 TIMING CONTROL

When a ROM is accessed, the timing and control block is notified by the address decoder logic to a) send out the RAM inhibit signal and b) enable the "Transfer Acknowledge" (XACK) delay counter to count the number of clock pulses by which the XACK/ must be delayed. The XACK/ will then be sent upon, either the counter value being equal to the code in the "Access Time Switch", if the "RAM NOT OVERLAPPED" switch is set, or to the count of 15.

Example: If the user sets the access time switches to code of 4 and the "RAM NOT OVERLAP" is set at "on" position then the transfer acknowledge (XACK/) will be sent shortly after the falling edge of the fourth CCLK/. But if the switch is not set at "on" position, the XACK/ signal shall be delayed until the falling edge of the 15th CCLK/.

The period of CCLK/ from the SBC 80/10 is 0.101 microseconds, making the timing of the above example 0.404 microseconds, and 1.5 microseconds, respectively.

The control logic is also responsible for indicating to the bytes selection logic when to enable the data buffers. In the event the ROM board is operating in 8 bit mode and, two chips in X and Y groups have mistakenly been assigned the same location, the control logic will prevent the read cycle. (For example, in order to avoid erratic operation or damage to the data drivers, INH1/ is sent; XACK is not sent).

Whenever a ROM is assigned to locations already occupied by RAM, the RAM board must be prevented from driving the data bus whenever the overlapped locations are accessed. This is accomplished by the ROM module sending an inhibit signal (INH1/) upon being selected. However, as both RAM and ROM board receive the address code and command simultaneously and INH1/ happens with some delay with respect to command address, it is possible for the RAM to begin an irreversible operation.

One of the four RAM overlap switches (4) indicates to the timing logic that the current read operation is for ROM and that INH1/ has to be maintained until RAM has terminated its internal process.

In systems with dynamic RAMs, such as SBC 016 16K RAM Board the longest time occurs if the RAM module had begun a refresh cycle prior to the read command. The refresh operation must then be completed, before the read operation is executed (at the end of which, transfer aknowledge is sent). The maximum access delay imposed by this operation is 1.5 microseconds. During this time, INH1/ must be maintained in the asserted state: otherwise XACK/ may be resulted which will cause a possible conflict.

Generation of INH1 by the control logic is based on the receiving of any RSn/ signal. This signal is in turn generated when the address of a resident ROM is contained in the address lines. The signal path is A29, 1, 2, 4, 5, -6 and A29 10, 12, 13, 8 (Figure 3).

If INH2 is active, however, no action is required to occur in the ROM module. If INH2 is not active and a memory read command (MRDC) occurs, a module select signal is generated (MS/. The signal path is A25 4, 2, 5 -6; A16 3-4).

When signal RS0 or RS1 is active while MS/ is true, the "low byte enable" is generated, (signal path is A36 Pin 12, 13, -11; A36 Pins 1, 2-3; Figure 3, Sheet 3. The high byte signal path is A36 pins 9, 10, 8 and A34 pin 12, 15 and 11. Note that A36 4, 5-6 detects that both bytes are selected. If the paths across J2 is established by the presence of the shorting plug, the output of this gate prevents generation of MS signal.

When MS is false (low) the delay counter is held cleared when MS is true, this counter (A19) will count the clock pulses.

A26 and A17 form a four bit comparator. The output of the counter is matched with the setting of the "access time" code switches. A high at the counter will compare equal with a closed switch when all four bits are equal to the switches and RAMOV/ is not present. The comparator output will be true (A17 pin 8 is low).

If RAMOV/ is active (low), no output occurs. The counter will proceed to the count of 15 which satisfies A18, 1, 2, 4, 5 -6. When either of these signals (A17 pin 8 or 18 pin 6) is true, the count enable at the pins 5 and 6 counter input goes false (signal path A25 pins

12, 13, 9, 10, 8; A16 pins 5 and 6).

If RAM is not overlapped A17 pin 11 will be high and the access time comparator enabled. The counter stops when its output is identical to the code in the "access time" switches. If RAM is overlapped A17 will have no output and the counter proceeds to the fixed code that satisfied A18 (code 15).

Note that as MS/ becomes true, A34 will be enabled with its input in false state (low). XACK/ line is first driven high, then low (true) at the proper count of A19 counter.

The timing logic is cleared directly by the requesting master removing MRCD/, upon INH2/ becoming true, or changed in the address that is generating MS/.

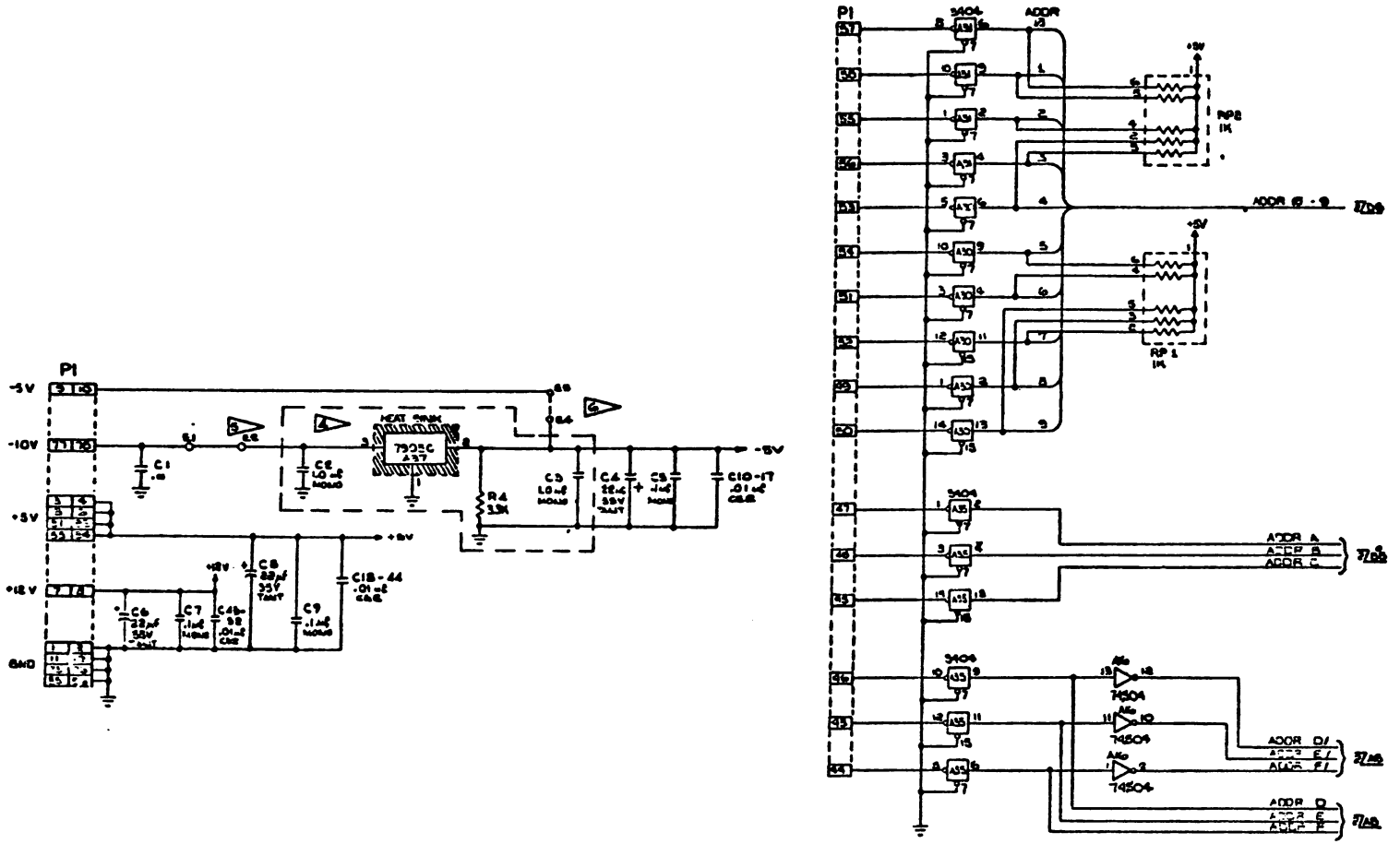
If positions SW5 and SW10 of S1 and S2 are open, the ROM resident signal (A27-6, 27-8, 5-6, 5-8) will propagate through A28-6, 28-8. The connection of these gate outputs effectively being an OR gate for RAMOV/ signal to the control logic.

The byte selection block places data on the bus as directed by the control logic. It supplies the control logic with the word selection status.

Two internal data busses collect data from each memory group, and feed the input of the data bus drivers (A32, 33, 34). These drivers are in two groups corresponding to the high and low bytes of the 16 bits data word. Data drivers also form a 16 to 8 multiplexer in the 8 bit word operation when J2 is installed.

2.4 LOGIC SCHEMATIC

Figure 3, sheets 1, 2 and 3 show the logic schematic of the board.



NOTES:
UNLESS OTHERWISE SPECIFIED

1. ARTWORK REVISION LEVEL IS REV A.
2. RESISTOR VALUES ARE IN OHMS, ¼W, ±5%.
3. POWER PINS FOR THIS DEVICE (2708) ARE AS FOLLOWS:
   VCC (+5V) - PIN 24
   VDD (+12V) - PIN 19
   VEE (-5V) - PIN 21
   VSS (GND) - PINS 12,18 (8508 CHIP SHOULD HAVE C58/ OPTION)
4. COMPONENTS A37, C2, C5 & R4 USED ON PWA 1000669-01 ONLY. *
5. S4, S5, S6, & RESISTOR ACROSS E1-E2 ARE CUSTOMER INSTALLED.
6. STRAP FROM E3 TO E4 ON PWA 1000669-02 ONLY.

FIGURE 3

SCHEMATIC - 16K PROM/ROM MEMORY BOARD
(1 of 3)

*(i.e., used on MDS, not used on OEM SBC)

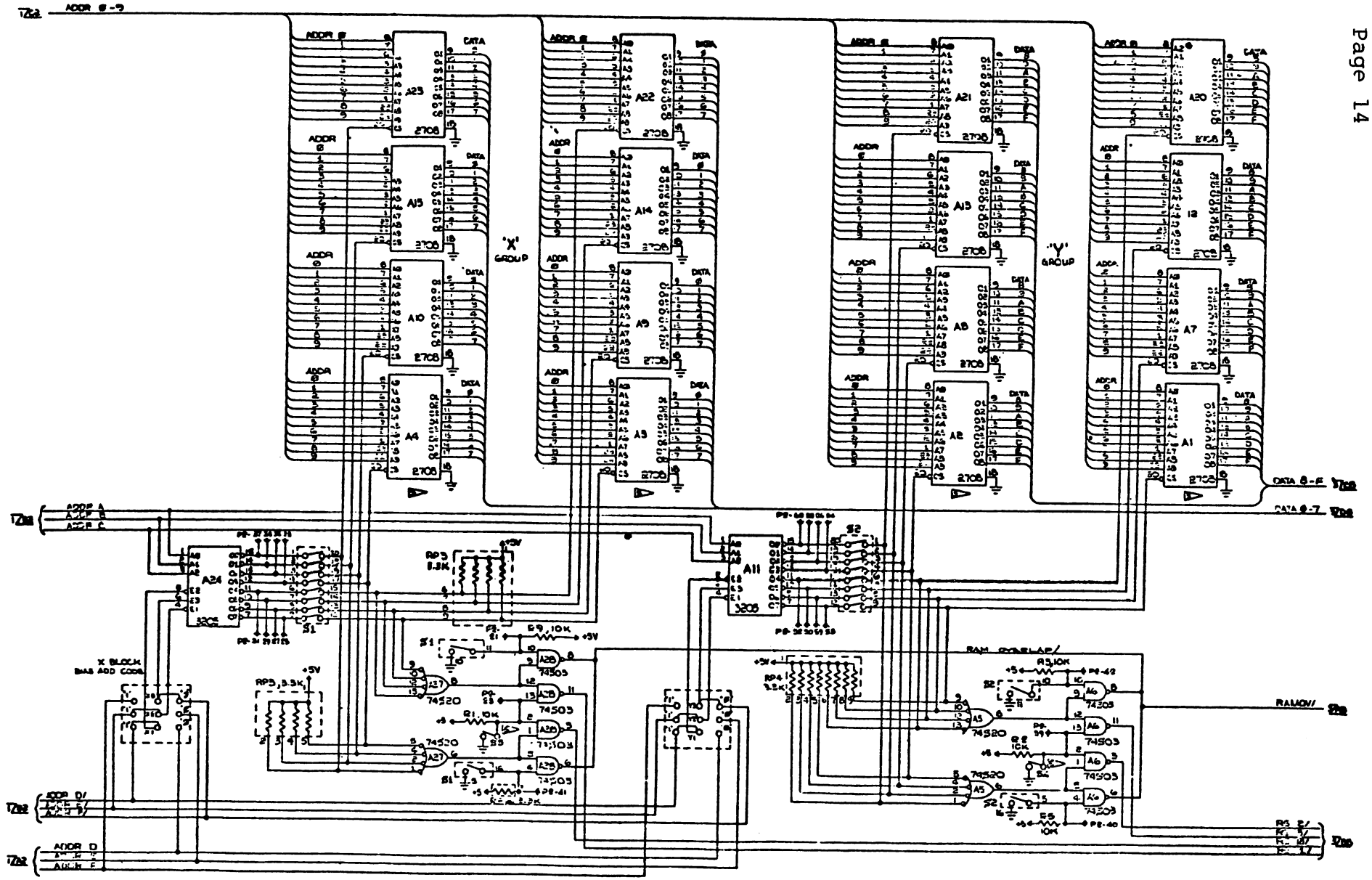


FIGURE 3

(Continued - 2 of 3)

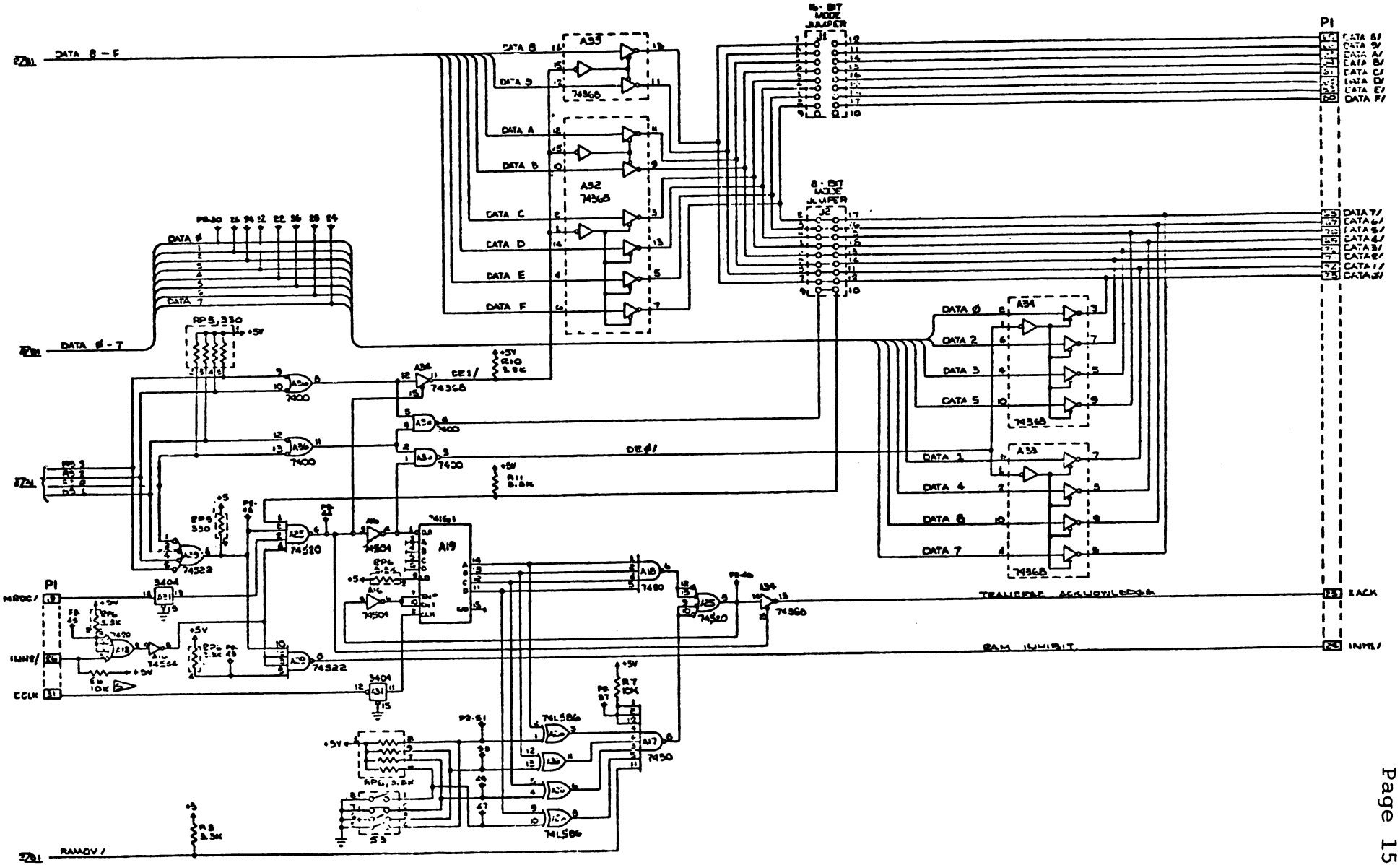


FIGURE 3

(Continued - 3 of 3)

3.0 HARDWARE INSTALLATION

3.1 INSTALLATION OF SWITCHES AND JUMPERS

The switches and jumpers may be installed in the following sequence:

Step 1: "Word Width Selection" Plug - to select 16 bit mode or 8 bit mode.

Step 2: "Group Bias Address" Jumpers - to assign a group bias address for X group and Y group.

Step 3: Insert PROM/ROM chip in a socket according to Tables 1 and 2.

Step 4: "ROM Resident Enable" Switch - to indicate the residency of a PROM/ROM chip to the board.

Step 5: "RAM NOT OVERLAP" Switch - to indicate to the board that the PROM/ROM overlaps RAM at some memory locations.

Step 6: "Access Time Code" Switch - to set the read access time of the board such that the board can accommodate the slowest PROM/ROM chip currently resident on the board.

Step 7: If "Group Enable/Disable Switch" is installed, the X group or Y group PROM/ROM memory on the board can be masked out or unmasked by flipping the switch.

3.2 INSTALLATION OF BOARD

In installing the board, the user must take account of:

(a) environmental extremes
(b) mounting considerations
(c) electrical connections
(d) power requirements
(e) signal requirements
(f) address assignments
(g) access timer selection
(h) byte selection

ENVIRONMENT

Temperature extremes can cause instability, or result in permanent damage to the circuits on the module. Ambient temperature must therefore be maintained within the limits of 0 degrees Centigrade and 55 degrees Centigrade. Remember that the module itself, when installed, will contribute some heat to the environment. Maintain an adequate clearance, to permit the convective dissipation of heat from the elements on the card.

Relative humidity should not exceed 90% noncondensing.

MOUNTING

Avoid locating the module near vibrating machinery. Exposure to prolonged or violent vibration may cause fatigue or impact failure of connections on the board, resulting in abnormally high noise levels or outright failure of the assembly.

Dimensions of the module are 12 in. X 6.75 in. Be sure to allow enough additional clearance to ensure adequate cooling.

The board is designed to plug directly into the SBC 604 or SBC 614 cardcage/backplanes or into two standard, double-sided PC edge connectors; an 86-pin connector and a 60-pin auxiliary connector. The connectors can serve as a mounting, as well as an electrical junction, if the environment is not too severe. Card guide slots are desirable, for the additional protection they afford. Should vibration be a problem, however, or should the assembly be used in a portable equipment application, an additional retaining bracket will have to be provided.

ELECTRICAL CONNECTIONS

The 16K PROM/ROM board communicates with the motherboard and, consequently, the rest of the system, through a standard 86-pin, double-sided PC edge connector (P1),

0.156 in. contact centers, as shown in Figure 4. Control Data VPB01E43A00A1 is one suitable type of connector. Pin allocations on this connector are given in Table 4. The auxiliary 60-pin, double-sided PC edge connector (P2), 0.1 in. contact centers (see Figure 4) is used for test purposes. Pin allocations for this connector (primarily used for test points) are listed in Table 5. Refer to Table 3 for DC Power Requirements. Refer to the pin list in Table 4 for power connections.

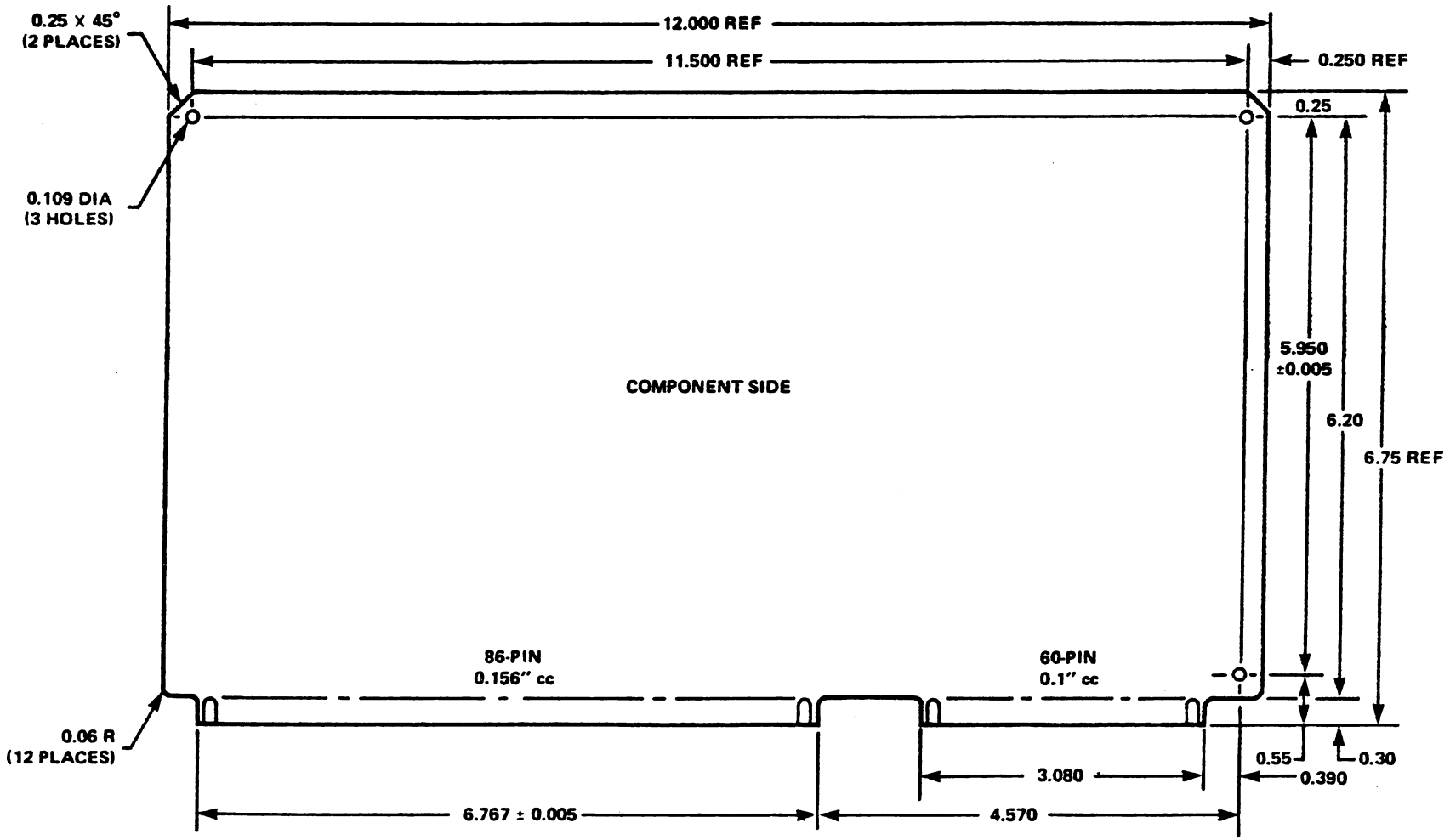


FIGURE 4

BOARD CONNECTORS

3.3 POWER REQUIREMENTS

The SBC 416 uses +5, +12 and -5V at levels listed in Table 3.

3.4 PIN LISTS

The pin list for the PROM/ROM board is shown in Tables 4 and 5.

4.0 OPERATING CHARACTERISTICS

4.1 AC CHARACTERISTICS

The AC characteristics are described in Table 6, and Figure 5.

4.2 DC CHARACTERISTICS

The DC characteristics are described in Table 7.

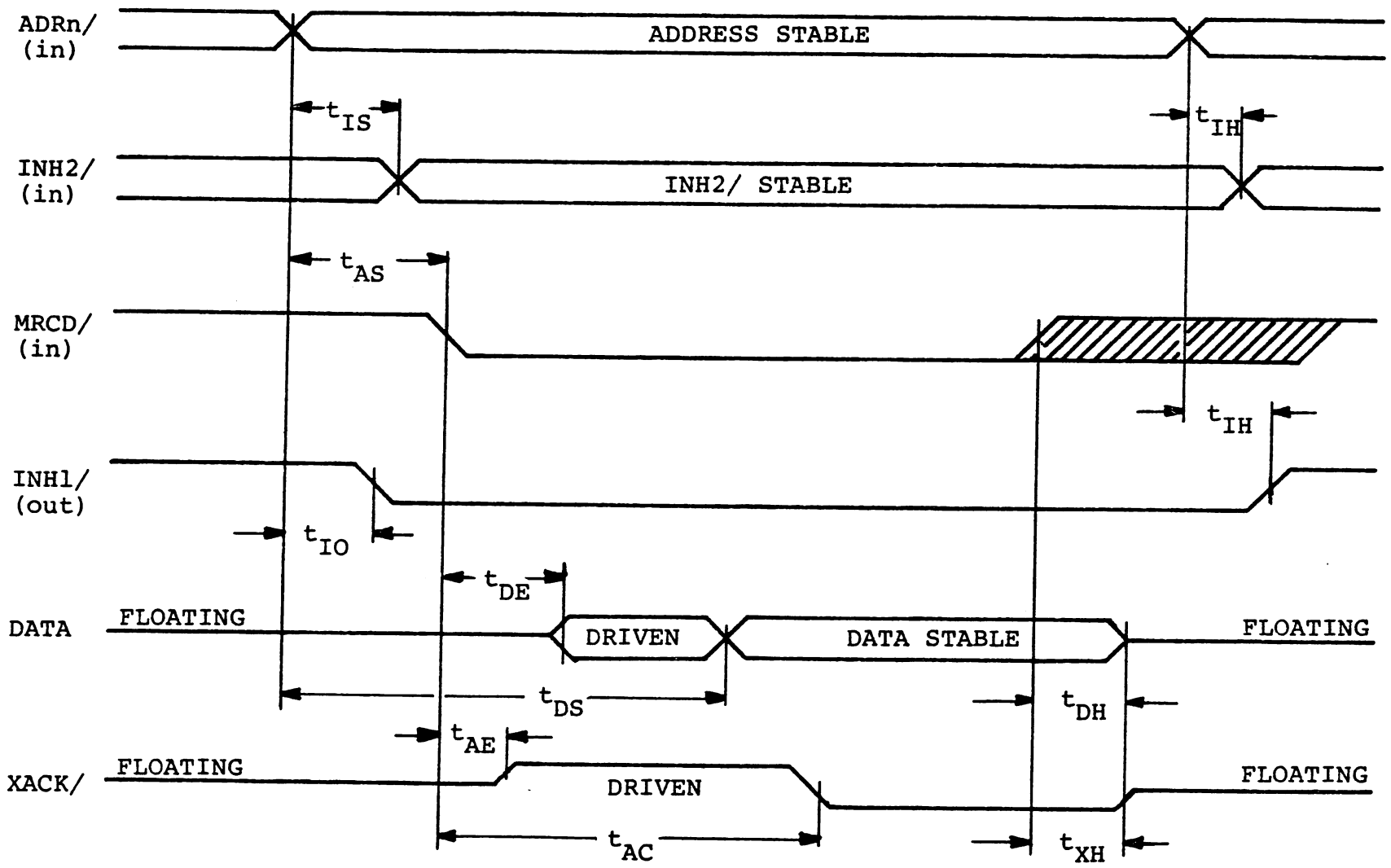


FIGURE 5

TIMING DIAGRAM

TABLE 3

DC POWER REQUIREMENTS

USING 16 8708 PROMs
(Fully loaded with 16 8708 PROMs)

POWER	CURRENT (AMPs)	
	TYPICAL CASE	WORST CASE
+5V	.7	.972
+12V	.8	1.04
-5V	.480	.720

USING 16 8308
(Fully loaded with 16 8308 PROMs)

POWER	CURRENT (AMPs)	
	TYPICAL CASE	WORST CASE
+5V	-	.9
+12V	.512	.96
-5V	-	.020

NO PROMs INSERTED

POWER	CURRENT (AMPs)
	WORST CASE
+5V	.700
+12V	Ø
-5V	Ø

TABLE 4

P1 CONNECTOR PIN LIST

PIN	SIGNAL	FUNCTION
1	GND	Ground
2	GND	
3	+5 VDC	Power inputs
4	+5 VDC	
5	+5 VDC	
6	+5 VDC	
7	+12 VDC	Power inputs
8	+12 VDC	
9	-5 VDC	
10	-5 VDC	
11	GND	Ground
12	GND	
13		
14		
15		
16		
17		
18		
19	MRDC/	Memory read command
20		
21		
22		
23	XACK/	Transfer acknowledge
24	INH1/	Inhibit RAM
25	AACK/	Advance acknowledge
26	INH2/	Inhibit ROM
27		
28		
29		
30		
31	CCLK/	Common clock
32		
33		
34		
35		
36		
37		
38		
39		
40		
41		
42		
43	ADRE/	Address bus

PIN	SIGNAL	FUNCTION
44	ADRF/	Address bus
45	ADRC/	
46	ADRD/	
47	ADRA/	
48	ADRB/	
49	ADR8/	
50	ADR9/	
51	ADR6/	
52	ADR7/	
53	ADR4/	
54	ADR5/	
55	ADR2/	
56	ADR3/	
57	ADRØ/	
58	ADR1/	
59	DATE/	Data bus
60	DARF/	
61	DATC/	
62	DATD/	
63	DATA/	
64	DATB/	
65	DAT8/	
66	DAT9/	
67	DAT6/	
68	DAT7/	
69	DAT4/	
70	DAT5/	
71	DAT2/	
72	DAT3/	
73	DATØ/	
74	DAT1/	
75	GND	Ground
76	GND	
77	-10 VDC	Power inputs
78	-10 VDC	
79		
80		
81	+5 VDC	Power inputs
82	+5 VDC	
83	+5 VDC	
84	+5 VDC	
85	GND	Ground
86	GND	

TABLE 5

P2 CONNECTOR PIN LIST

PIN	SIGNAL	FUNCTION
1	S4-10	RESERVED PINS FOR BACK-UP POWER
2		
3	CSA30	
4	S3-10	
5	CSA27	
6	CSA26	
7	CSA28	
8		
9	CSA25	
10	CSA29	
11	CSA23	
12	CSA24	
13	CSA19	
14		
15	CSA17	
16	CSA18	
17	CSA16	
18		
19	CSA14	
20	CSA15	
21	CSA13	
22		
23	CSA23	INH X/
24	CSA12	
25	CSA6	
26	CSA7	
27	CSA4	
28	CSA5	
29	CSA2	
30	CSA3	

PIN	SIGNAL	FUNCTION
31	S1-1	
32	CSA1	
33	S1-3	
34	S1-2	
35	S3-8	
36	S2-13	
37	S3-7	
38	S3-6	
39	S3-5	INH Y/
40	S3-4	
41	S3-2	
42	S3-4	
43	S2-15	
44	S3-1	
45	S2-14	INH ALL/
46	S2-16	
47	S2-11	
48	S2-12	
49	S2-9	
50	S2-10	
51	S4-2	
52	S4-1	
53	S4-4	
54	S4-3	
55	S4-8	
56	S4-3	
57	S4-6	
58		
59	S4-7	
60		

Note: Pins 21 through 60 are reserved for test points.

TABLE 6

AC CHARACTERISTICS

DESCRIPTION	MINIMUM (nsec)	MAXIMUM (nsec)
t_{AS} = Address Set-up Time	43*1	-
t_{IS} = INH2/ After Address		20
t_{IH} = INH2/ Hold Time	27.5	
t_{IO} = INH1/ Out From Address		62.5
t_{CCY} = Constant Clock Cycle	92	
CCLK/ Pulse width	30	
t_{DS} = Data Stable from Address if $t_{AS} \leq 50$ nsec behind Address	(2708: 309 / 8308: 229)	479
t_{AC}*2*3 = Module Access Time	55+(n)t_{CY}	79+(n+1)t_{CY}
t_{DH} = Data Hold after MDRC/ Removal	-	91
t_{IH} = Inhibit 1 Hold from Address		62.5
t_{XH} = XACK/Hold		44
t_{DE} = Data ENABLE		81
t_{AE} = XACK Line Driven		54
t_{CY} = CCLK/Period	101.72 MDS 186.5 SBC 80/20	

NOTE: n = the number set by switch S3.

*1 There is no required relation between MRDC/ and address for this board, but t_{AE} is dependent on the latest arriving signal. If MRDC/ precedes the address, add 43 nsec to t_{AC} as described. Also, if the cycle is terminated by an address change before MDRC/ is removed, add 43 nsec to t_{DH}.

*2 Minimum: based on all involved devices having minimum propagation and the clock edge is coincident with the counter being enabled. Maximum: based on all involved devices having maximum propagation and the clock edge just preceded the instant the counter was enabled.

*3 No response if addressed PROM is disabled or if the PROM inhibit (INH2/) is invoked.

TABLE 7

DC CHARACTERISTICS OF THE 16K PROM/ROM BOARD

SIGNALS (DEVICE)	PARAMETERS	MIN.	MAX.	UNIT	TEST CONDITIONS
ADR0/-ADRF/	V_{IL}-Input low voltage		0.85	V	V_{CC}=5.0V
RD CMD/CCLK/	V_{IH}-Input high voltage	2.0		V	V_{CC}=5.0V
	I_R-Input leakage current		10	µA	V_{CC}=V_R=5.25V
	I_F-Input load current		-0.25	mA	V_{CC}=5.25,V_R=0.45V
INH2/	V_{IL}-Input low voltage		0.8	V	
	V_{IH}-Input high voltage	2.0		V	
	I_R-Input leakage current		1	mA	V_{CC}=5.25V,V_R=5.5V
	I_F-Input load current		-1.6	mA	V_{CC}=5.25V
INH1/	V_{OL}-Low level output voltage		0.4	V	I_{OL}=20 mA
	V_{OH}-High level output voltage	2.4			Open collector
XACK/	V_{OL}-Low level output voltage		0.4	V	V_{CC}=4.5V,I_{OL}=32 mA
	V_{OH}-High level output voltage	2.4		µA	V_{CC}=4.5V,I_{OH}=-5.2 mA
DATØ/-DATF/	I_{LH}-Input current at high voltage		-40	µA	V_{CC}=5.25V,High Z,V_R=0.5,DIS=2.0V
	I_{LL}-Input current at low voltage		40	µA	V_{CC}=5.25V,High Z,V_0=2.4V

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